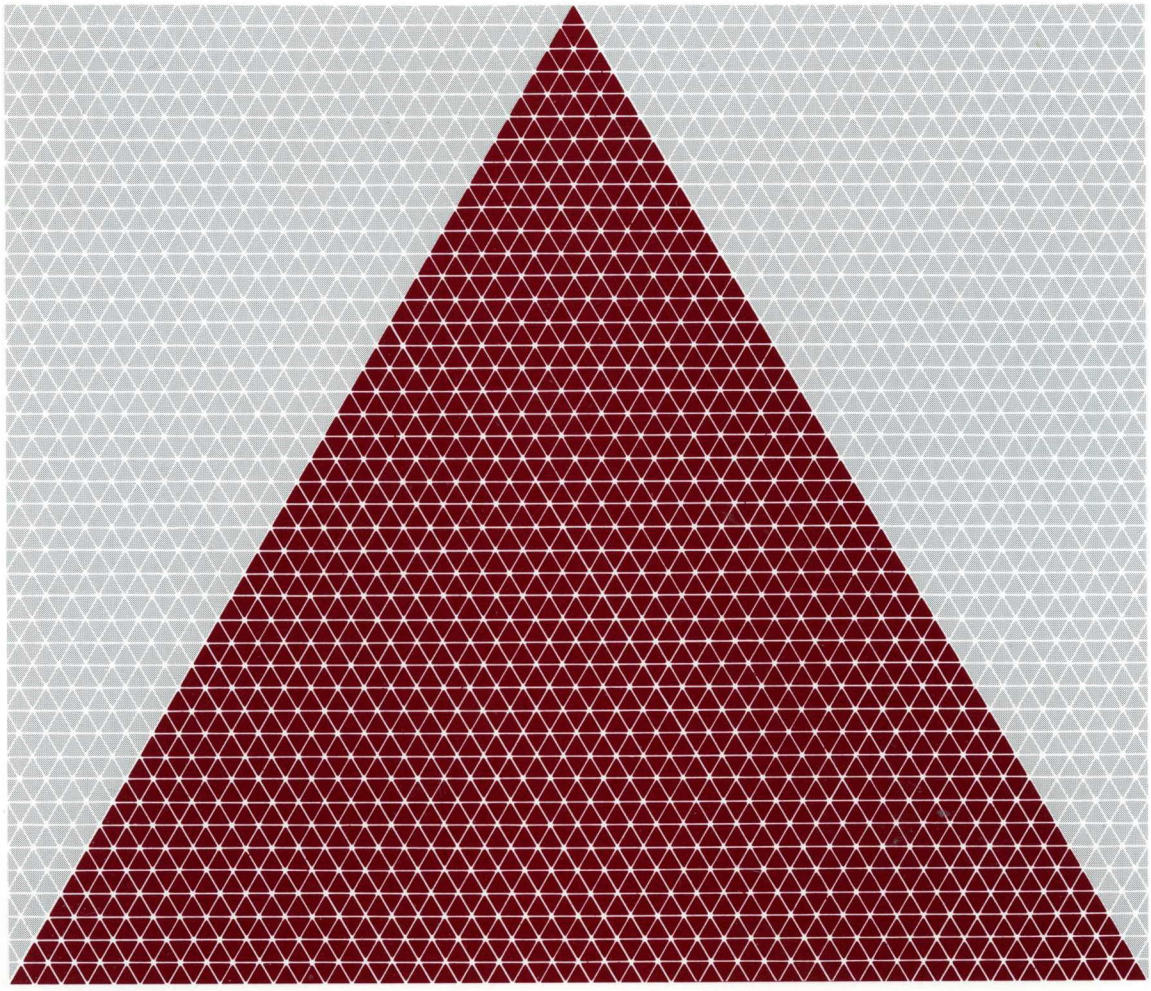
Altos Computer Systems

1086/2086
Maintenance



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This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

ABOUT THIS MANUAL

This manual contains detailed service information for the technician who is trained in digital electronics, microcomputers, and operating systems.

The purpose of this manual is to describe the operation of the 1086/2086 Computer System and provide specific instructions to enable the technician to effectively service the 1086/2086.

Careful attention to the preventive and corrective maintenance information contained in this manual will ensure maximum trouble-free operation from the Altos 1086/2086 Computer System.

This manual is organized into the following chapters:

Chapter 1 System Overview

- describes the features and capabilities of the system
- provides a hardware overview of the major circuits and peripherals
- lists and shows the location of the field replaceable assemblies comprising the system
- describes and shows the dedicated and recommended expansion plug-in printed circuit board (PCB) locations
- describes and shows the locations of the front and rear-panel controls, connectors, and indicators
- discusses the software available for the system

Chapter 2 Specifications

- lists the pertinent electrical, environmental, and physical specifications for the system

- shows the overall physical dimensions of the system

Chapter 3 Principles of Operation

- explains how the plug-in PCB subsystems interface to the system through the system bus
- describes how the system is initialized or programmed at power-up
- describes the programmed steps performed in the main operational sequences
- lists the addresses for each device that can be accessed
- includes bit definitions for the ports and external registers
- includes pertinent timing diagrams and general programmable array logic (PAL) information

Chapter 4 Maintenance

- includes 115/230 VAC conversion instructions
- provides cleaning procedures
- provides removal and replacement procedures.
- provides shipping information

Chapter 5 Troubleshooting

- discusses troubleshooting aids and techniques
- includes detailed troubleshooting procedures using power-up, system-confidence, and field-service diagnostics

Appendices

Includes jumper pinning, loopback connector assembly, storage device specifications, and utility program information.

Glossary

Includes an alphabetical list and definitions of specialized terms and acronyms used in this manual.

Index

Includes an alphabetical list of names, subjects, or topics contained in this manual with the page numbers where they occur.

RELATED PUBLICATIONS

The following is a list of publications that contain additional information relating to the 1086/2086 system. The **1086/2086 Owner's Guide** is shipped with the system. The remaining publications are optional and are divided into three types: (1) basic (run-time) system manuals that contain information for installing and using the operating system, (2) development system manuals that include reference and tutorial material for programs available in the development system, (3) supplemental information manuals that are referenced in the text of this manual and contain additional information required to understand the operation of the 1086/2086 system. The publications listed here are available through your Altos distributor or directly from integrated circuit manufacturers.

Shipped with 1086/2086

Altos 1086/2086 Owner's Guide (Altos part no. 690-16447-XXX)

Basic System

- Installing XENIX on Your 1086/2086 System (Altos part no. 690-16630-XXX)
- Introduction to XENIX (Altos part no. 690-13449-XXX)
- Directory of XENIX Commands (Altos part no. 690-1664- XXX)

Development System

Altos Development System Set (Altos part no. 583-13801-XXX)

Supplemental Information

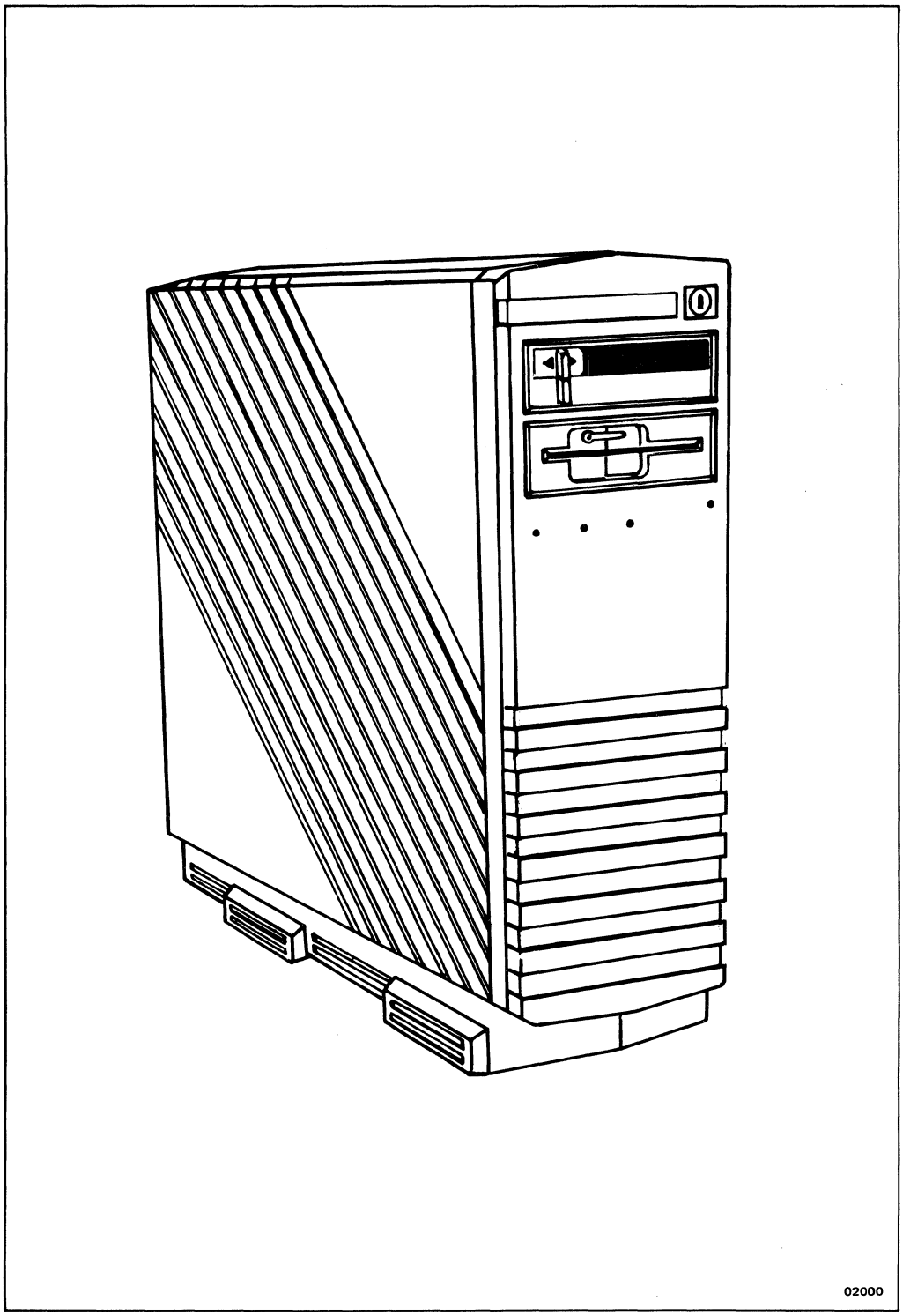
- Altos 1086/2086 System Reference Manual (Altos part no. 690-15623-XXX)
- Altos 1086/2086 Illustrated Parts List (Altos part no. 690-15625-XXX)
- Altos 1086/2086 Remote Diagnostics Instructions (Altos part no. 690-17072-001)
- IEEE 796 System Bus Specification (Multibus)
- Intel IAPX 286 Programmer's Reference Manual
- Intel Microsystem Components Handbook
- Intel Microprocessor and Peripheral Handbook
- Intel 8254 Data Book (Mode 2)
- National Semiconductor 58167 Applications Note Data Handbook
- Advanced Micro Devices 9517 Technical Reference Manual
- Zilog Data Handbook/Technical Manual

- Hitachi HD6845Ø Data Book
- Hitachi Microcomputer Handbook
- National Cash Register 5385 SCSI Protocol Controller Data Sheet
- Archive QIC-Ø2 1/4-Inch Tape Drive Interface Standard
- Archive QIC-24 1/4-Inch Cartridge Tape Drive Format Standard
- Archive QIC-36 Basic 1/4-Inch Cartridge Streaming Tape Drive Interface Standard
- NEC PD765 Data Sheet
- NEC Data Handbook
- ANSI X3T9.2/82-2 SCSI Small Computer System Interface
- National Cash Register Data Handbook

SPECIAL SYMBOLS AND NOTATIONS

The following is a list of the special symbols and notations used in this manual.

Symbol/Notation	Description
* (Asterisk)	Used following a capitalized mnemonic or signal name to indicate a "not" (complement) function or an active low signal. Example: PERR*
h	Used after a number to indicate that the number is a hexadecimal notation. Example: 25h
d	Used after a number to indicate that the number is a decimal notation. Example: 16d
b	Used after a number to indicate that the number is a binary notation. Example: Ø1b



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SYSTEM DESCRIPTION

The Altos 1086/2086 Computer System is a floor-standing computer designed for general processing, office automation, and network fileserver applications. The system contains a CPU, system memory, I/O connections, mass storage, streaming tape backup, and a floppy disk drive.

Characteristics

The following are some of the main characteristics of the 1086/2086:

- exceptional modularity for easy system expansion
- 8 MHz Intel 80286 main microprocessor
- optional high-speed Intel 80287 floating-point processor
- up to 451M bytes of formatted internal hard disk storage
- up to 8M bytes of RAM system memory
- 60M byte streaming cartridge tape drive
- storage expansion beyond 451M bytes via a small computer system interface (SCSI) channel. (-002 version of file processor subsystem only.)
- high-speed 32-bit expanded Multibus[tm]
- remote diagnostics (with optional modem) for rapid fault isolation to field replaceable units

Architecture

The modular system architecture allows for convenient service. The printed circuit boards (PCBs) are easily removed or replaced without disassembling the system.

The cartridge tape, floppy disk, and hard disk drive mass storage subassemblies are easily installed or replaced by removing the front panel and sliding the subassemblies in or out of the chassis. The three available hard disk drive subassemblies plug directly into the backplane.

The system can contain up to eight plug-in PCB subsystems (five PCBs are used for a minimum 10-user system) and five magnetic media storage subassemblies. All of the plug-in PCBs slide into the back of the chassis and connect to the system backplane PCB located in the center of the chassis. The mass storage subassemblies slide into the front of the chassis and also connect to the backplane PCB. The backplane PCB serves as the medium for data interchange between the processors, system memory, and mass storage subassemblies.

Configurations

The 1086/2086 system can be configured in a variety of ways. The smallest possible configuration (or minimum system) could be made with 1M byte of random access memory (RAM), 10 RS-232 ports, a 50M byte hard disk drive, and a 1.6M byte floppy disk drive. More system memory, hard disk capacity, and RS-232 ports can be added.

A larger system configured to support 20 or 30 users could contain a 2M byte or 4M byte memory PCB, two or three 10-port communications PCBs, a 190M byte hard disk drive, a 1.6M byte floppy disk drive, and a 60M byte cartridge streaming tape drive.

Networking

The 1086/2086 hardware supports local area networking (LAN). The networking hardware runs at two speeds: 750K and 1.4M bits per second. The slower speed allows the 1086/2086 to talk to Altos 186, 486, 586/586T, and 986/986T networks. The higher speed allows the 1086/2086 to talk to other 1086/2086 systems. A simple low-cost, twisted-pair, RS-422 interface is used at the hardware level.

The 1086/2086 uses the same type of WorkNet software that runs on most Altos systems. The WorkNet software allows transparent remote file access and remote processor execution.

Communications

The 1086/2086 system supports several serial communications protocols which are down-loaded to the serial communications PCB. These communications protocols are run by the 8086 microprocessor on the communications PCB, which removes this burden from the main CPU. By using multiple communications PCBs, multiple communications protocols can be run at the same time. The software for running the communications protocols is downloaded into the RAM on the communications PCB.

The software for 3270, 3780, X.25, and SNA protocols will run on the 1086/2086. The system is capable of supporting asynchronous modems for dial-up data base services or offsite communications and bisynchronous modems for IBM 3780 emulation. WorkNet can also be supported through one port via a software command communicating at 1.4M bits per second or 750K bits per second (used to connect compatibles to Altos processors). The optional communications PCB subsystem, configured with 32K bytes of RAM, supports certified X.25 or IBM/SNA software protocols.

Diagnostics

The 1086/2086 performs three major categories of diagnostic tests. The first category is the built-in hardware tests contained in the power-up monitor program. (Refer to **System Software** in this chapter for additional diagnostics information.)

The second category of tests is the user system-confidence tests. The final category is the field-service diagnostics (SDX) tests which can be run either from a floppy disk or remotely with the optional communications modem. (Refer to the **1086/2086 Remote Diagnostics** manual for remote diagnostics information.)

Power-Up Tests

The power-up tests are ROM-based and reside on the CPU, communications, and file processor PCBs. These power-up tests are always performed when power is applied to the system to check the minimum hardware configuration on its particular PCB, identify any missing or failed assemblies, and then confirm communication with the system. These tests are always performed on power-up.

The CPU power-up tests include programmable read-only memory (PROM), cache memory, translation and tag RAM memory, clock, floating-point numeric processor, interrupt, and system bus checks. The file processor power-up tests include local RAM and PROM, interval timer, system bus, DMA controller, and magnetic media controller checks. The communications PCB power-up tests consist of local RAM and PROM, I/O integrated circuits, DMA controller, interrupt, and system bus checks.

User System-Confidence Tests

The user system-confidence tests allow a system user to test the functionality of the system. These tests are menu driven. A full set of tests can be run with only one or two keystrokes on the system console. More detailed and flexible tests are also available for the service technician. A full set of system utilities for handling system configuration and mass storage devices is included.

Field Service Diagnostics

The field-service diagnostics can be run either from the SDX floppy disk supplied with the system or from a remote service depot through the optional communications modem. The principle advantage of the remote method of performing diagnostics is that only one PCB (one of the communications PCBs) needs to be working in order to begin testing. In most multi-board systems, the CPU PCB, system memory PCB, controller PCB, and communications PCB must be working before diagnostic testing can start.

In the 1Ø86/2Ø86, the communications (SIO) PCB contains a full 16-bit microprocessor that acts as a diagnostic controller on the system bus.

Thus, each PCB can be called up and tested separately, or the full system can be enabled and exercised to isolate and identify failures for repair or replacement.

Another advantage of the remote diagnostic method is that the tests are run by highly trained technicians at the main Altos facility or at designated service centers. The full expertise of Altos is available on the spot to evaluate a problem without waiting for a service technician to arrive.

The remote facility can call up specific PCB monitors or debuggers, or transmit the latest circuit-level diagnostics, with no interaction required from the user. The failed unit can, upon isolation, be easily replaced by the user or by the system administrator.

Hardware

The system hardware is partitioned so that each major function is performed by a single PCB. The five required PCBs for the minimum 1Ø-user system are the CPU, system memory, communications, file processor, and controller. All of these PCBs, except the controller, connect to the 32-bit system bus. Refer to Chapter 3 for a description of the system hardware operation.

System Bus

The system bus is asynchronous and has 32 data lines and 24 address lines that can support a maximum data transfer rate of 3ØM bytes per second. Up to 16M bytes of RAM can be accessed and data transfers can be 8-, 16-, or 32-bits wide. The system bus supports one of up to eight bus masters. All the processors in the system communicate with each other via system memory and I/O channel attentions and interrupts.

Central Processing Unit (CPU) PCB

The CPU PCB contains an 80286 microprocessor (running at 8 MHz), an interrupt controller, and a calendar clock with battery backup.

Also available on the -002 version of the CPU PCB is an optional 80287 floating-point numeric processor. The 80286 is aided by a 4K byte instruction and data cache memory. When operating out of cache memory, the 80286 runs with zero wait states.

When a memory write on the system bus occurs, the cache control hardware searches the cache. If there is a cache hit, then that location in the cache is marked as invalid. This feature of the cache makes it fully coherent with system memory at all times. The cache hit rate has been measured at 88% under typical use environments.

The CPU PCB contains memory mapping hardware that splits up system memory into 4K byte pages to speed up task switching and prevent memory fragmentation problems.

Memory PCB

The memory PCB comes in three sizes: 1M, 2M, or 4M bytes. The system memory is organized into long words of 32 bits and memory transfers can be made in 8, 16, or 32-bit quantities.

The memory PCB uses 150 nanosecond dynamic RAM integrated circuits (ICs) and features a typical access time of 240 nanoseconds with a typical cycle time of 400 nanoseconds. Multiple memory PCBs can be installed in the 1086/2086 system.

Communications PCB

The communications PCB handles all of the serial communications for the 1086/2086 system and supports asynchronous and synchronous RS-232, and RS-422 network communications.

The communications PCB supports up to 10 asynchronous ports; three of which can be software-switchable to support two synchronous channels and one networking port.

The operating software for the communications processor is down-loaded at boot time so that the communications PCB becomes fully programmable.

The networking port is fully compatible with Altos 800K bit WorkNet, 186, 486, 586, and 986 systems and can run at a faster 1.4M bit per second rate when communicating with other 1086/2086 and Altos 3068 systems. Several synchronous communications packages, which include the X.25 and SNA protocols, are available to run on the communications PCB. An Intel 8086 microprocessor (running at 8 MHz) manages all the data flow, I/O interrupts, DMA channels, and communications with the CPU.

File Processor PCB

The file processor PCB manages the data flow to/from the Centronics parallel port and all of the mass storage devices in the system. The mass storage devices include the floppy disk, hard disk, and cartridge streaming tape drives, and all the peripherals connected to the SCSI channel.

NOTE

The -001 version of the file processor PCB does not support small computer system interface (SCSI) operation. The -002 version of the file processor PCB includes SCSI.

Some of the main characteristics of the file processor are:

- supports up to three internal hard disk drives and additional drives connected via the SCSI channel
- supports a DMA-driven Centronics parallel port for high-speed line and laser printers

- concurrent transfer of the printer, tape, floppy disk, and hard disk data (only one hard disk at a time)
- performs overlapped seeks when more than one disk drive is connected
- performs reads and writes to consecutive sectors on the hard disk, even though data may be scattered in system memory.

Controller PCB

The controller PCB contains the device controllers for the floppy disk, hard disk, and streaming tape drives. All of these device controllers take commands from the file processor.

The hard disk controller accommodates disk drives with ST506 or ST412HP interfaces and can handle data transfer rates up to 5M bits per second. The hard disk controller can support up to three internal hard disk drives.

The tape controller can interface with Altos cartridge streaming tape drives with the QIC-36 interface and uses the QIC-24 format for putting data on the tape. The tape streams at 90 inches per second and has a maximum capacity of 60M bytes.

The floppy disk controller interfaces with a dual-speed floppy disk drive which uses either normal or high capacity disks. The normal disks are fully compatible with the floppy disks used on the Altos 186, 486, and 586 systems.

FIELD REPLACEABLE UNITS

The 1Ø86/2Ø86 Computer System contains the following field replaceable units (FRUs) (see Figure 1-1):

- main power supply
- streaming tape drive
- hard disk drive
- floppy disk drive
- central processing unit (CPU) PCB
- memory PCB
- communications PCB
- file processor PCB
- controller PCB
- backplane PCB
- light-emitting diode (LED) PCB
- low-pass filter PCB (early versions only)

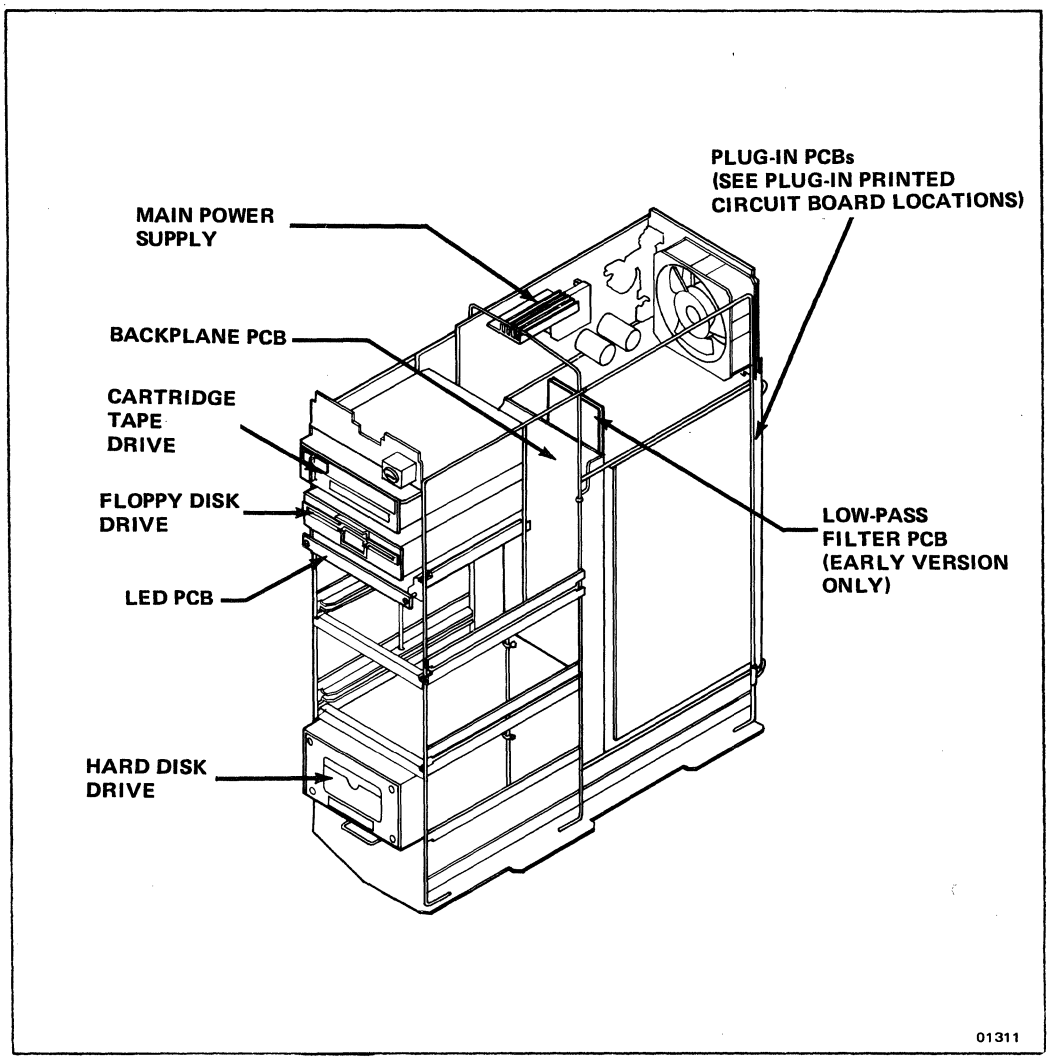

Figure 1-1. Field Replaceable Units

CONTROLS, CONNECTORS, AND INDICATORS

Refer to Figure 1-2 for the locations of the front and rear-panel controls, connectors, and indicators. The following is a description of the controls, connectors, and indicators indexed to the numbers in Figure 1-2:

Front Panel

1 **RESET/RUN Switch.** Key-operated switch that resets (boots) the system when turned to RESET and back to RUN. Allows normal system operation when set to RUN. If the key is turned to RESET and removed, the system will remain in the reset condition and will not operate.

2 **POWER Indicator.** Green light-emitting diode (LED) indicator that lights when power is applied to the system (rear panel POWER switch is in the on position).

3 **HD 1, HD 2, and HD 3.** Yellow LED indicators that light to indicate which hard disk drive is selected.

Rear Panel

4 **POWER Switch.** Rocker switch that applies power to the system when placed in the on position (green LED indicator 2 on the front panel is lit). The system will boot when the POWER switch is placed in the off, then on, position while the RESET/RUN switch 1 on the front panel is in the RUN position.

5 **Fuse Holder.** Holder that contains the main line-voltage fuse (Refer to Chapter 2 for the proper fuse rating).

6 **AC INPUT Connector.** Three pin AC connector for attaching an AC power cord to the system.

7 **UPS Jack.** Jack for connecting a power fail status signal from an external uninterruptable power source device to the system.

8 **PRINTER Connector.** Connector for attaching a printer with a Centronics parallel interface to the system.

9 **Serial I/O Ports.** Ports Ø through 9 on the communications PCB provide 1Ø asynchronous RS-232 ports for connecting terminals or printers to the system. Refer to the communications PCB description in Chapter 3 for details on the serial I/O port capabilities.

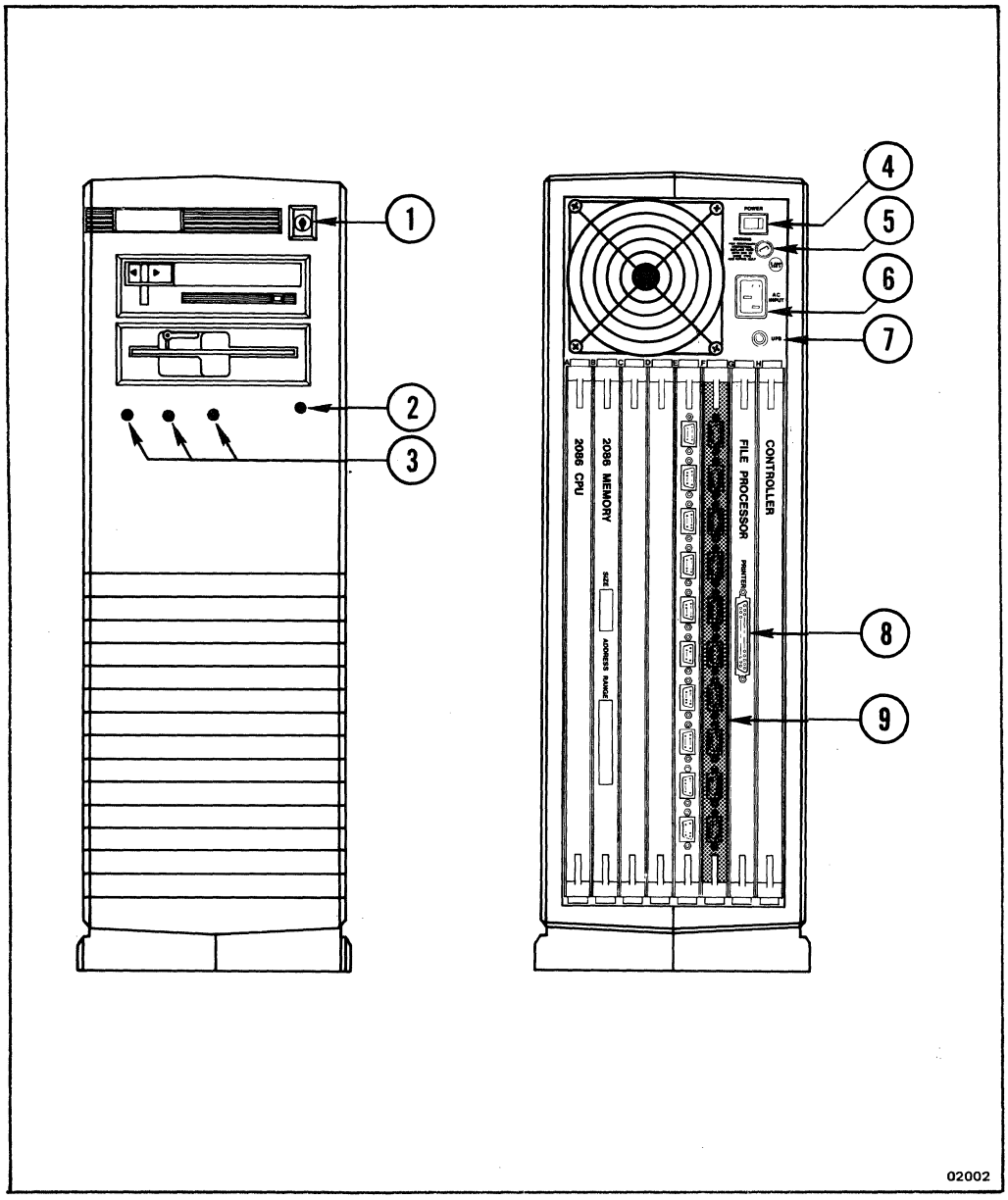

Figure 1-2. Controls, Connectors, and Indicators

PLUG-IN PRINTED CIRCUIT BOARD LOCATIONS

The CPU, file processor, and controller PCBs are dedicated to slots A, G, and H respectively in the back of the 1086/2086. The remaining slots, B through F, are electrically identical which allows memory and communications PCBs to be installed in any order in these five slots. However, software requires that the memory and communications PCBs be jumpered according to their logical assignment in the system (see jumper description information in Chapter 3 and Appendix A).

SYSTEM SOFTWARE

The system software supplied with the 1086/2086 consists of the operating system, utility, and diagnostic programs.

Operating System Program

The 1086/2086 Computer System is specifically designed for the XENIX 3.2 operating system.

The XENIX operating system supports the following development tools and programming functions:

- large Model C compiler with 1M byte of address space per program
- shared data that allows programs to share a common memory space
- semaphores that provide a synchronization tool for cooperating programs
- source code control system for easy program maintenance
- full suite of development tools, such as, vi, csh, nroff, lint, and adb

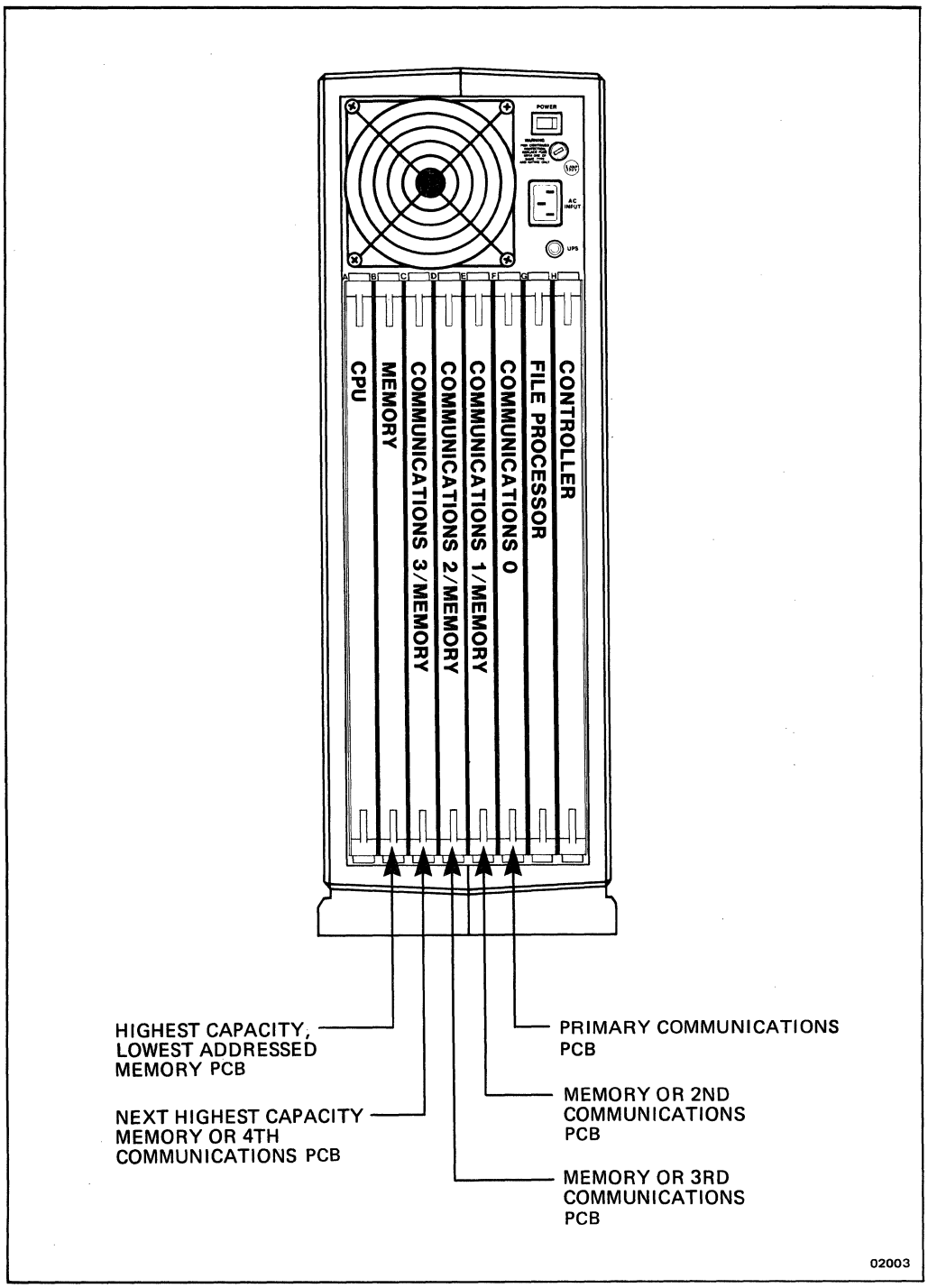

Figure 1-3. Recommended Plug-In PCB Locations

Address Translation

XENIX uses the sophisticated address translation logic on the 1086/2086 to improve performance as follows:

- Scatter Loading. Loads user programs into noncontiguous 4K byte pages of system memory for more efficient use with less swapping
- Faster Context Switching. When context switching, the per process data area is mapped by loading a table entry instead of copying the data around memory as in standard XENIX
- Dynamic Stack Growth. Programs do not preallocate stack space

Disk Performance

The 1086/2086 hard and floppy disks are controlled by the file processor PCB which removes much of the processing work from XENIX. The Altos XENIX also supports a 1K byte block file system that maximizes disk throughput.

Serial Port Performance

The 1086/2086 serial ports are controlled by the communications PCB which offloads interrupts and processing from XENIX. Each communications PCB is down-loaded with a code that handles the asynchronous ports, WorkNet, and any other communication protocols (SNA, X.25, 3780, and 3270).

Compatibility

The XENIX operating system on the 1086/2086 can read and write floppy disks and execute programs that run on the most Altos systems. Tapes created on the Altos 986T can also be read on the 1086/2086.

Diagnostics

The System Diagnostic Executive (SDX) Program is on a floppy disk included with the 1Ø86/2Ø86 system. The SDX program performs a series of user system-confidence tests. Refer to Chapter 5 for information on the SDX user system-confidence tests.

Field-service diagnostics are also available on the SDX floppy disk. Additional information on the SDX field-service diagnostics is provided in Chapter 5. (Refer to the **1Ø86/2Ø86 Remote Diagnostics** manual for detailed remote diagnostics procedures.)

CHAPTER 2
SPECIFICATIONS

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INTRODUCTION

The electrical specifications listed in Table 2-1 apply when the 1086/2086 Computer System has been operating for at least 15 minutes at an ambient temperature between +40 and +95 degrees Fahrenheit (+5 and +35 degrees Celsius). The environmental and physical specifications are listed in Tables 2-2 and 2-3.

ELECTRICAL SPECIFICATIONS

Table 2-1 lists the electrical specifications for the Altos 1086/2086 Computer System.

Table 2-1. Electrical Specifications

Characteristic	Performance Requirement
Subsystem	
Central Processing Unit (CPU)	
Microprocessor	80286
Floating-Point Micro-processor (Optional)	80287
Clock Frequency	8 MHz
System Data Size	32 bits
System Address Size	24 bits
CPU Data Size	16 Bits
CPU Address Size	24 Bits
Data and Instruction Cache Data Block Size	32 Bits
Data and Instruction Cache Memory Size	4K bytes
CPU to Memory Transfer Rate	10M bytes/second

Table 2-1. Electrical Specifications (Cont.)

Characteristic	Performance Requirement
Subsystem (Cont.)	
System Memory	
Addressable Space	1M, 2M, or 4M bytes/board
Standard	1086: 1M byte; 2086: 2M bytes
Optional	8M bytes, maximum*
Transfer Word Length	Capable of 1, 2, or 4 byte (32 bit) parallel transfers
Access Time From Memory Read/Write Command	
Typical	240 nanoseconds
Maximum	550 nanoseconds (with refresh)
Typical Cycle Time	390 nanoseconds
SIO Communications	
Microprocessor	8086
Clock Frequency	8 MHz
Total I/O Ports	10
Configurable Synchronous Ports	2
Configurable Network Ports	1
RAM	
Standard	128K bytes
Optional	512K bytes
WorkNet Data Transfer	
Maximum Rate/Distance	750K bits/second: 2500 feet/trunk segment 1.4M bits/second: 1500 feet/trunk segment. Extendable to 4500 feet with repeaters

* Hardware can support up to 16M bytes of system memory. Currently, Altos supports up to 8M bytes of system memory.

Table 2-1. Electrical Specifications (Cont.)

Characteristic	Performance Requirement
Subsystem (Cont.)	
File Processor	
Microprocessor	8086
Clock Frequency	8 MHz
Total External Ports	2
Parallel Printer Port	1
SCSI Port (-002 Only)	1
Total Internal Ports	5
Tape	1
Floppy Disk	1
Hard Disk	3
Maximum Transfer Rates	
Tape	90K bytes/second
Floppy Disk	63K bytes/second
Hard Disk	5M bits/second
SCSI	1.5M bytes/second
Printer	50K bytes/second
Storage Devices	
(See Appendix B for additional drive specifications)	
Cartridge Tape Drive	
Number of Drives	1
Number of Tracks	9
Number of Channels	2
Capacity	60M bytes/cartridge
Backup Time	15 minutes (60M byte tape)
Media	1/4 inch Scotch[tm] DC-600A cartridge
Recording Mode	NRZI (nonreturn-to-zero invert)
Data Transfer Rate (Tape Speed)	90 inches/second
Format	QIC-24
Interface	QIC-36

Table 2-1. Electrical Specifications (Cont.)

Characteristic	Performance Requirement
Storage Devices (Cont.)	
Floppy Disk Drive	
Number of Drives	1 dual-speed, double-sided, double-density drive
Form Factor Size	5-1/4 inches
Formatted Size	
High Density	1.2M bytes
Low Density	720K bytes
Unformatted Size	
High Density	1.6M bytes
Low Density	1M byte
Data Transfer Rate	250K or 500K bits/second
Hard Disk Drive	
Number of Drives	1 to 3
Form Factor Size	5-1/4 inches
Formatted Capacity	1086 / 2086
Standard	40M bytes / 63M bytes
Optional	63M bytes / 150M bytes
Unformatted Capacity	1086 / 2086
Minimum	50M bytes / 80M bytes
Maximum	80M bytes / 190M bytes
Interface	ST-506
Data Transfer Rate	5M bits/second
Average Seek Time (Includes Settling Time)	
50M Byte Drive	28 milliseconds
80M Byte Drive	28 milliseconds
190M Byte Drive	30 milliseconds

Table 2-1. Electrical Specifications (Cont.)

Characteristic	Performance Requirement		
Main Power Supply			
DC Output Voltages	+5	+12	-12
Accuracy	Adj.	±5%	±10%
Current (Continuous)			
Maximum	40 A	4 A	0.5 A
Minimum	15 A	0.1 A	0.05 A
Peak (300 ms, Pulsed Load)	N/A	6 A	N/A
Regulation (Line/ Load/Temp.)	±3%	±5%	±10%
Ripple/Noise (P-P)	50 mV	100 mV	150 mV
Overvoltage	Shutdown & cycle	Shutdown & cycle	N/A
AC Power			
Line Voltage Range			
115 VAC (Nominal)	90-125 VAC		
230 VAC (Nominal)	195-250 VAC		
Line Frequency Range	47-63 Hz		
Power Consumption			
Maximum	768 W		
Continuous	550 W		
Maximum BTU Output	1,876		
Maximum Current (RMS)	6.4 A at 60 Hz, nominal 115 VAC line 3.6 A at 60 Hz, nominal 230 VAC line		
Fuse Type			
115 VAC (Nominal)	10 A, normal-blowing type		
230 VAC (Nominal)	5 A, normal-blowing type		
Power Fail Status	Logic signal input from uninterruptable power source via UPS phone jack on rear panel. UPS monitor must be non-conducting when AC power is present and conducting when UPS is on		
Voltage (Vce)	0.5 V maximum		
Current (Ic)	1.6 mA DC		

ENVIRONMENTAL SPECIFICATIONS

Table 2-2 lists the environmental specifications for the Altos 1086/2086 Computer System.

Table 2-2. Environmental Specifications

Characteristic	Performance Requirement
Temperature	
Operating	+40 to +95 degrees Fahrenheit (+5 to +35 degrees Celsius)
Storage	-4 to +140 degrees Fahrenheit (-20 to +60 degrees Celsius)
Gradient	Not to exceed 10 degrees Fahrenheit/hour (5 degrees Celsius/hour)
Maximum Wet Bulb	+78 degrees Fahrenheit (+26 degrees Celsius)
Relative Humidity	20 to 80% non-condensing

PHYSICAL SPECIFICATIONS

Table 2-3 lists the physical specifications for the Altos 1086/2086 Computer System.

Table 2-3. Physical Specifications

Characteristic	Description
Weight	
Net (Operating)	Approximately 68 to 86 lbs (31 to 38.5 kg)
Shipping	95 lbs (43 kg) maximum (includes peripherals and container)
Dimensions	See Figure 2-1

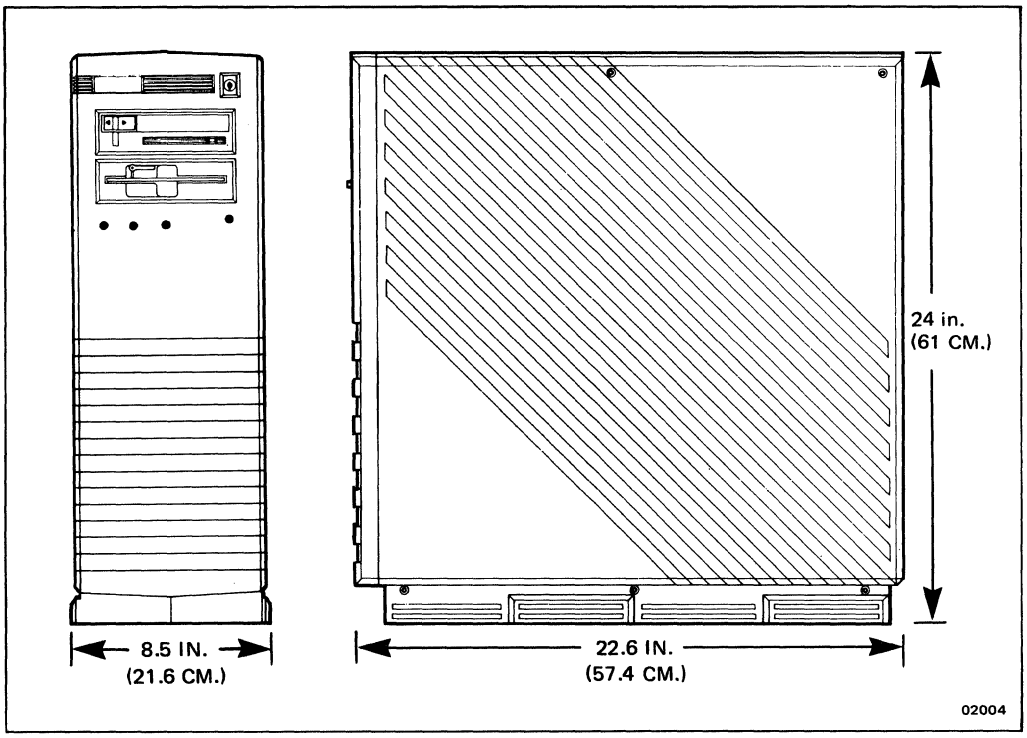

Figure 2-1. Maximum Overall Dimensions

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For convenience, each of the following PCB subsystem descriptions have a red locator tab on the right edge of the first page.

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INTRODUCTION

This chapter describes the operation of the Altos 1086/2086 Computer System and begins with a general description of the system operation and continues with a detailed description of the system bus interface and the plug-in printed circuit board (PCB) subsystems.

Where applicable, the manufacturer's publications are referenced for additional information concerning the integrated circuits used on the subsystems.

The 1086/2086 uses the following major subsystems. Each of these subsystems is contained on a single PCB except the system bus.

- system bus
- central processing unit (CPU)
- system memory
- communications (SIO)
- file processor
- controller

BLOCK DIAGRAM DESCRIPTION

The following block diagram description discusses the overall operation of the 1086/2086 system. Refer to the block and schematic diagrams in the **Schematic Diagrams** supplement to this manual.

System Bus

The system bus is a 32-bit data, 24-bit address bus which is an extension of the IEEE 796 system bus (Multibus). The system bus has separate memory and I/O address spaces and can handle asynchronous signal transfers between multiple masters or master and slave.

A bus master can perform either single or unlimited system bus transfers. A bus slave decodes addresses and acts upon commands from bus masters. The memory PCB is the only slave.

Eight bus masters (subsystem PCBs) are supported by prioritized parallel bus arbitration. A bus clock provides bus arbitration and general-purpose timing. Different master-slave subsystems can operate at different clock rates.

The CPU, file processor, and communications PCBs are bus masters which can acquire the system bus through bus exchange logic and generate command, address, and data signals (during writes).

The bus signals are divided into the following signal lines:

- control lines
- address lines
- data lines
- interrupt lines
- bus exchange lines

Central Processing Unit (CPU)

The CPU PCB executes all the system and applications programs. The CPU PCB contains an 80286 16-bit microprocessor, programmable read-only memory (PROM), a cache memory, and a system bus interface.

Also included is a calendar clock with battery backup that keeps time and generates system time-slice interrupts.

The 80286 microprocessor includes memory management and supports an optional 80287 floating-point microprocessor. The 80286 microprocessor can operate at 8 MHz and executes code out of either PROM, cache memory,

or system memory. The microprocessor mainly operates out of the cache memory which eliminates most wait states.

The local bus on the CPU PCB transfers address, data, status, and control signals to/from the PROM, calendar clock, interrupt controller, input status port, and control-bit output port.

System Memory

The memory PCB contains either 1M, 2M, or 4M bytes of memory depending on whether 64K byte or 256K byte RAMS are used. Memory is organized into 32-bit long words or 64-bit double long words, depending upon which version of the memory PCB is used. (There are two versions of the memory PCB as described in the **Memory PCB** section of this chapter.) Data transfer is in 8-, 16-, or 32-bit quantities.

Communications

The communications (SIO) PCB is an intelligent input/output (I/O) processor that relieves the CPU of all communications functions. The communications PCB contains an 8086 microprocessor, a system bus interface, a four-channel DMA controller, a local bus controller, 32K to 512K bytes of dynamic RAM, 16 to 256K bytes of PROM, a general-purpose counter/timer, and up to 10 serial ports.

Seven of the serial ports are dedicated to RS-232 asynchronous communications, one is independently software selectable between asynchronous RS-232 and synchronous RS-422 networks, and the remaining two can support either asynchronous or synchronous RS-232 communications.

Functionally, the communications PCB is a complete computer with the necessary initial program load (IPL)/diagnostic firmware, RAM, and serial I/O ports.

Since the communications PCB is closest to the terminal(s), its on-board firmware has several diagnostic functions that provide power-up confidence

tests of all local functions and low-level tests on other parts of the system (on the system bus), including system memory.

File Processor

The file processor PCB is an intelligent controller that manages data flow to/from a floppy disk drive, a cartridge tape drive, up to three hard disk drives, the Centronics parallel printer interface, and additional disk or tape drives through the Small Computer System Interface (SCSI) channel.

The file processor PCB contains an 8086 microprocessor, a four-channel DMA controller, a system bus interface, a local bus controller, 32K to 512K bytes of dynamic RAM, 16 bytes to 256K bytes of PROM, a counter/timer, a disk and printer interface, and a SCSI controller.

Controller

The controller PCB contains three independent controllers for hard disk, floppy disk, and cartridge tape drives. All controllers receive commands from the file processor PCB.

The hard disk controller can support three internal disk drives with either ST506 or ST412HP interfaces and can accommodate serial data rates to 5M bits per second. The hard disk controller is capable of seek-overlap operation when multiple devices are used.

The floppy disk controller supports one internal, double-density, double-sided, 96 track per inch (TPI), floppy disk drive.

The tape drive controller supports Altos cartridge tape drives with QIC-36 interfaces, and uses the QIC-24 format to input data on the tape.

DETAILED CIRCUIT OPERATION

The remainder of this chapter provides a more detailed description of the system bus and plug-in PCB subsystem operation.

To help locate the integrated circuits in the schematic diagrams and on the PCB, the location designation for certain integrated circuits is included in parenthesis after the first mention. Refer to **Locating a PCB Part** in the front of the **Schematic Diagrams** supplement in the back of this manual for instructions on how to use the part location designations.

NOTE

Use the red index tabs on the outside edge of the page to quickly locate the desired subsystem description.

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System Bus Interface

The 1086/2086 system bus is an extension of the IEEE 796 system bus (Multibus). The following are the major differences between the 1086/2086 system bus and the IEEE 796 system bus:

- data bus expanded to 32 bits
- address bus is 24 bits
- parallel bus arbitration
- additional control signals

The system bus has separate address spaces for memory and I/O. For memory operations, up to 16M bytes can be directly addressed. For I/O operations, a minimum of 64K 8-bit I/O ports or 32K 16-bit I/O ports can be addressed. The bus can handle asynchronous signal transfers between multiple masters or master and slave.

Eight bus masters (PCBs) are supported by prioritized parallel bus arbitration. A 9.83 MHz bus clock is provided for bus arbitration and general-purpose use.

Due to the asynchronous bus structure, different master-slave subsystems can operate at different clock rates. The maximum bus data transfer rate is 30M bytes per second.

There are four subsystem PCBs that interface through the system bus:

- central processing unit (CPU) PCB
- memory PCB
- file processor PCB
- communications (SIO) PCB

The floppy disk, hard disk, and tape controllers on the controller PCB are connected to the file processor PCB by a dedicated interconnect bus and not to the system bus.

Bus Masters

The CPU, file processor, and communications PCBs are bus masters. These three subsystems can acquire the system bus through bus exchange logic and generate command, address, and data signals (during writes).

A bus master can operate in two modes: mode 1 for single bus transfer per bus connect and mode 2 for unlimited bus transfers per bus connect by keeping the BUSY* signal asserted. See **Bus Lock Timing** for the maximum time the bus can be held.

Bus Slaves

The memory PCB is a bus slave. This subsystem decodes addresses and acts upon commands from bus master subsystems.

Bus Signals

The bus signals are divided into five groups based upon the function performed. The five groups are:

- control lines
- address lines
- data lines
- interrupt lines
- bus exchange lines

Control Lines. The following signals are classified as control lines:

BCLK* Bus Clock. A 9.83 MHz 50/50 duty cycle clock used to synchronize the bus contention logic. Only one master can generate this clock. The CPU PCB contains the bus clock generation circuitry.

MWT* Memory Write. Asserted by the bus master. Indicates a valid memory address is on the bus. The data can have -30 nanoseconds setup time to the command. See **Timing.**

MRD* Memory Read. Asserted by the bus master. Indicates a valid memory address is on the bus.

IOWT* I/O Write. Asserted by the bus master. Indicates a valid I/O address and data is on the bus.

IORD* I/O Read. Asserted by the bus master. Indicates a valid I/O address is on the bus.

XACK* Transfer Acknowledge. Asserted by the addressed slave to acknowledge that data has been placed or accepted on the data lines.

AACK* Advance Transfer Acknowledge. Asserted by the addressed slave before the transfer is completed. AACK* helps eliminate wait states due to control synchronization. See **Timing.**

ERR* Error. On memory read operations, ERR* is asserted if a parity error is detected by the memory PCB. ERR* is asserted by the 80286 microprocessor on the CPU PCB if a bus timeout occurs.

MRST* Manual Reset. Input from front panel reset switch. The 80286 microprocessor on the CPU PCB generates a system reset on the REST* signal line when MRST* is asserted.

REST* System Reset. Asserted during power-up and in response to a manual reset. Asserted for at least 5 milliseconds after power supplies are within tolerance. Only the 80286 microprocessor on the CPU PCB may drive this line.

PF* Power Fail. Asserted by the power supply when AC line falls below 90 VAC for 115V systems and 180 VAC for 220V systems. This signal is asserted at least 5 milliseconds before the +5V supply falls out of tolerance.

UPSS* Uninterruptible Power Supply Status. Asserted by an optional UPS when loss of input power is detected. This signal is asserted a minimum of 20 minutes before the system input power is out of tolerance.

LOCK* Lock. Asserted by the master in control of the bus during read-modify-write operations. The current master keeps the bus by holding BUSY* asserted. Only the bus owner can access a multiported memory when LOCK* is asserted. Lock can be asserted for a maximum of 8 microseconds.

Address Lines. The following signals are classified as address lines:

A00*-A23* Address bits 00-23. A00* is the least significant bit (LSB) and A23* is the most significant bit (MSB). Address lines are driven by bus masters. The 24 address bits can directly address 16M bytes.

HBEN* High Byte Enable. Used with A00*, A01*, and HWEN* for data transfer width and byte steering.

HWEN* High Word Enable. Used with A00*, A01*, and HBEN* for data transfer width and byte steering.

See **Data Transfer Width** for decoding A00*, A01*, HWEN*, and HBEN*.

Data Lines. The following signals are classified as data lines:

D00*-D31* Data bits 00 through 31. D00* is the LSB and D31* is the MSB. Eight, sixteen, and thirty-two bit transfers are allowed. The bus master drives data lines on write operations while the addressed slave drives the data lines on read operations.

Interrupt Lines. The following signals are classified as interrupt lines:

INT0*-INT6* Interrupt Requests 0-6. Interrupts are divided into seven prioritized classes with INT0* having the highest priority. Interrupts are requested by asserting one of the seven interrupt request lines.

Bus Exchange Lines. The following signals are classified as bus exchange lines:

BRQ0*-BRQ7* Bus Requests 0-7. A master wanting control of the bus asserts a bus request. A parallel priority resolution circuit on the CPU PCB is used to resolve the highest priority bus request. BRQ0* has the highest priority.

BPN0*-BPN7* Bus Priority In 0-7. A master receives a BPNx when it is the highest priority master requesting the bus. A master looks for the same level bus grant as bus request (a master requesting on BRQ3* looks for the grant on BPN3*).

CBRQ* Common Bus Request. Any master wanting the bus but does not own it, asserts CBRQ*. If CBRQ is clear, the current bus owner can keep the bus until it is set.

BUSY* Busy*. Asserted by the master in control of the bus to indicate the bus is in use. All other masters monitor BUSY* to determine the state of the bus.

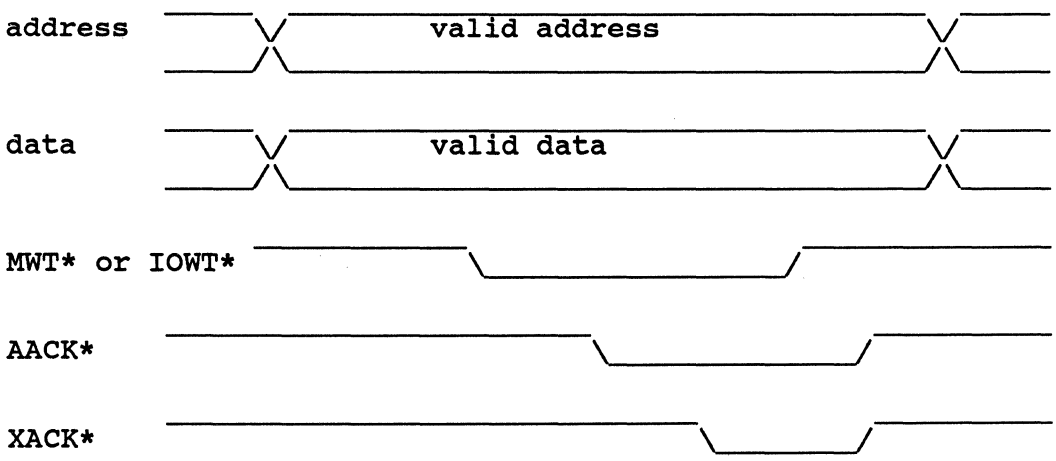
Data Transfer Operations

There are four types of data transfer operations:

- memory read
- memory write
- I/O read
- I/O write

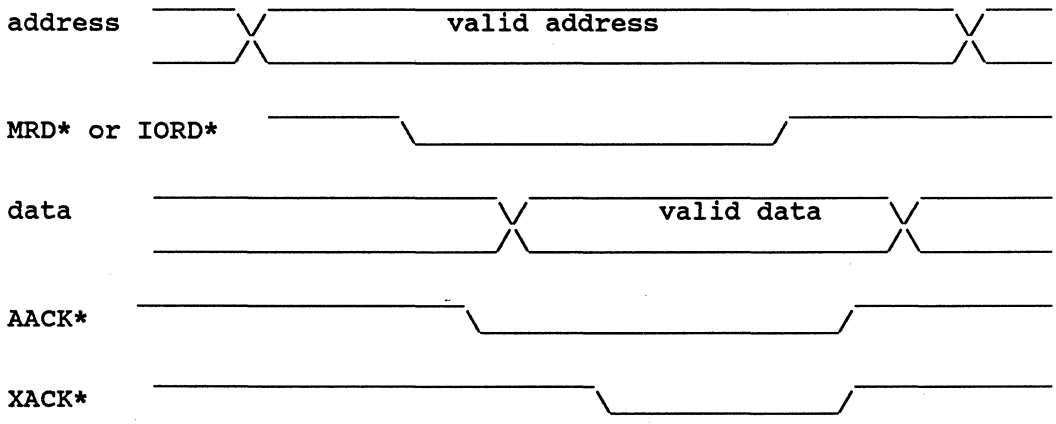
Write Operations. The bus master starts the operation by placing the memory or I/O address on the address lines and the data on the data lines.

When the address and data are valid , the bus master asserts a MWT* (memory write) or IOWT* (I/O write) command which activates the appropriate bus slave. The addressed slave accepts the data from the data lines and asserts XACK* (transfer acknowledge) and AACK* (advance transfer acknowledge). The bus master then removes the command and clears the address and data lines to complete the data transfer. The following is the basic write timing:



Slaves must assert both AACK* and XACK*.

Read Operations. The bus master starts the operation by placing the memory or I/O address on the address lines. When the address is valid, the bus master asserts a MRD* (memory read) or IORD* (I/O read) command which activates the appropriate bus slave. The addressed slave places the data on the data lines then asserts XACK* and AACK*. The bus master completes its cycle by reading the data from the data lines, removes the command, and clears the address lines. The following is the basic read timing:



Slaves must assert both AACK* and XACK*.

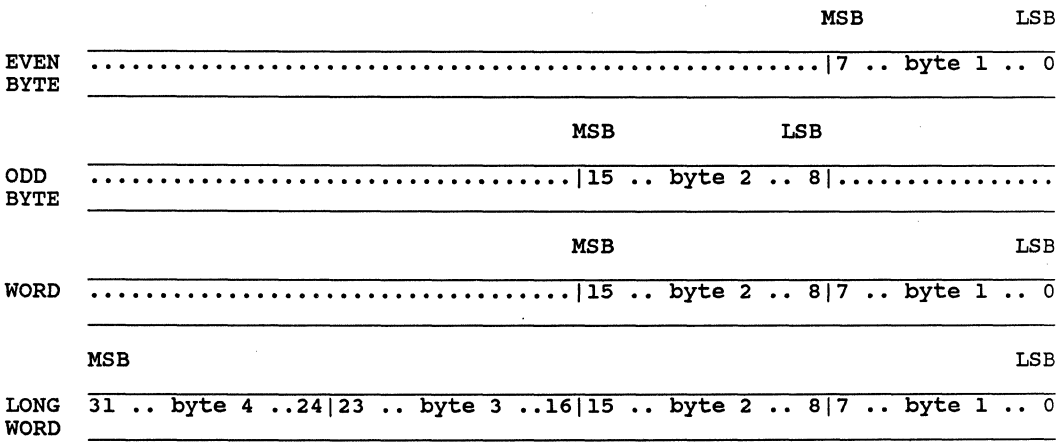
Bus Timeout. The 80286 microprocessor on the CPU PCB will monitor data transfer operations and generate a bus timeout and assert ERR*, AACK* and XACK* if any command (MRD*, MWT*, IORD*, or IOWT*) is active for more than 4 microseconds.

Data Transfer Width. There are two 8-bit, one 16- bit, and one 32-bit data transfer widths. HWEN*, HBEN*, A01* and A00* decode which byte(s) the data is transferred on:

HWEN	HBEN	A01	A00	WIDTH	DATA BYTES ACTIVE
0	0	X	0	8	1
0	1	X	1	8	2
0	1	X	0	16	2,1
1	1	0	0	32	4,3,2,1

1 = true or active state
0 = false or inactive state
X = either state

Data Formats. The following are the data formats:



Interrupt Operation

The system bus uses nonbus vectored interrupts and is not used because no interrupt vector address is placed on it. An interrupting PCB asserts one of the interrupt request lines (INT0*-INT6*) to generate an interrupt request. The interrupt requests are prioritized with INT0* the highest and INT6* the lowest. Two interrupt acknowledge methods can be used:

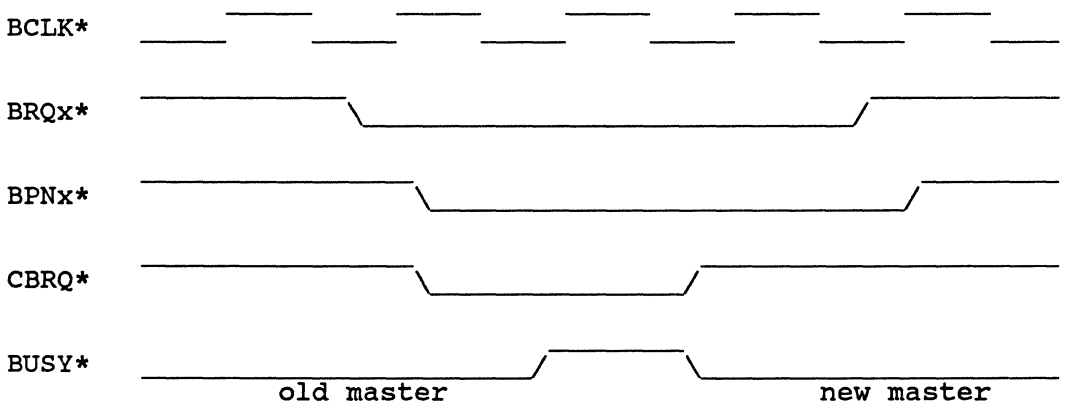
1. The CPU PCB can write to the bus slave to reset the interrupt.

2. Software handshaking. The interrupt request indicates an interrupt vector is in memory. The CPU PCB would read the vector and set a flag indicating the slave can reset the interrupt request.

Bus Exchange

The system bus can accommodate eight bus masters. Each master requests the bus on a bus request line (BRQx*). BRQØ* has the highest priority while BRQ7* has the lowest. Parallel priority arbitration is used.

The highest priority request receives its bus priority in signal (BPNx*). When BUSY* is cleared and BPNx* is asserted, the bus switches to the new master. The following is the basic bus exchange timing:



All bus exchange lines are asserted on the falling edge of BCLK*.

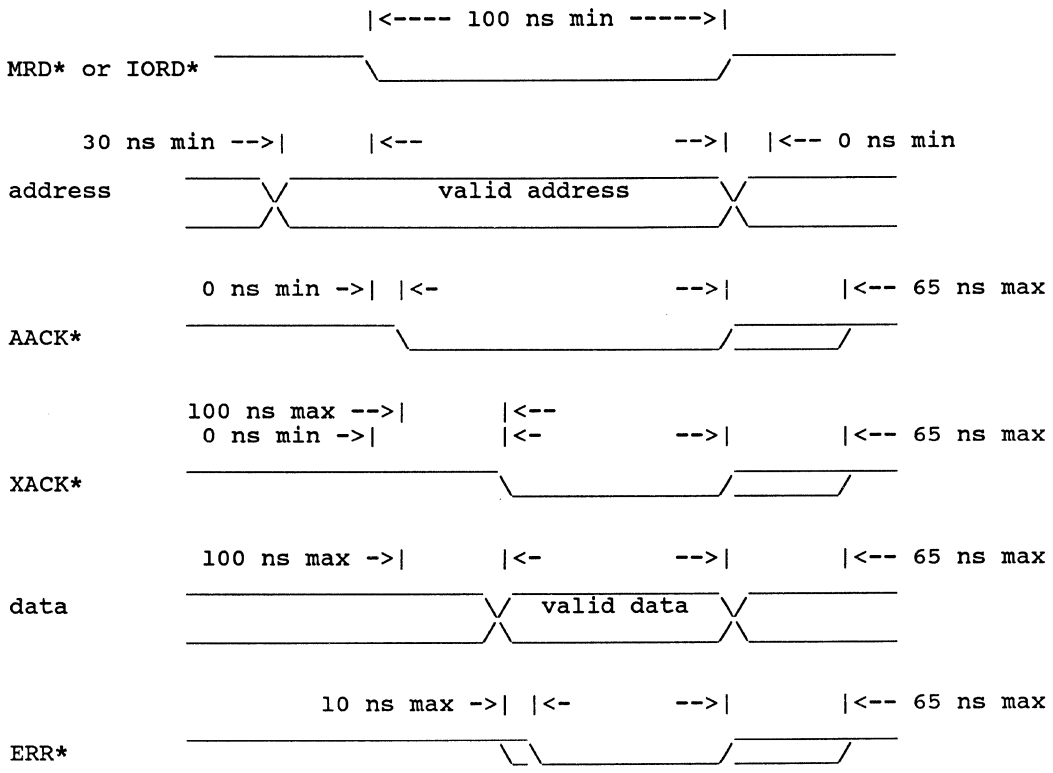
Lock Operation

The system bus may be locked for a maximum of 8 microseconds. The LOCK* signal is set and BUSY* is held asserted during locked bus operations. BUSY* held asserted is the mechanism for locking the system bus. LOCK* is required during read-modify-write operations to multiported memories to hold off accesses by other processors.

Timing

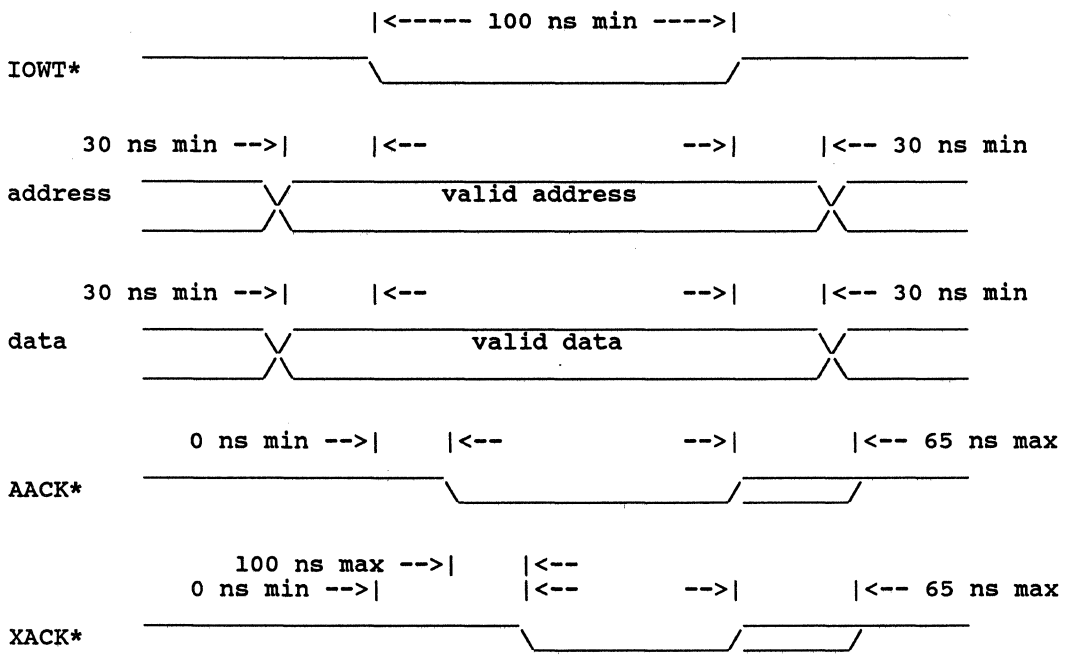
All timing is referenced at the input/output pins of the backplane PCB slot. The bus propagation and settling time of 4 nanoseconds is added to ALL timing calculations. Slaves drive both AACK* and XACK*.

Read Timing. The following is the read timing diagrams:

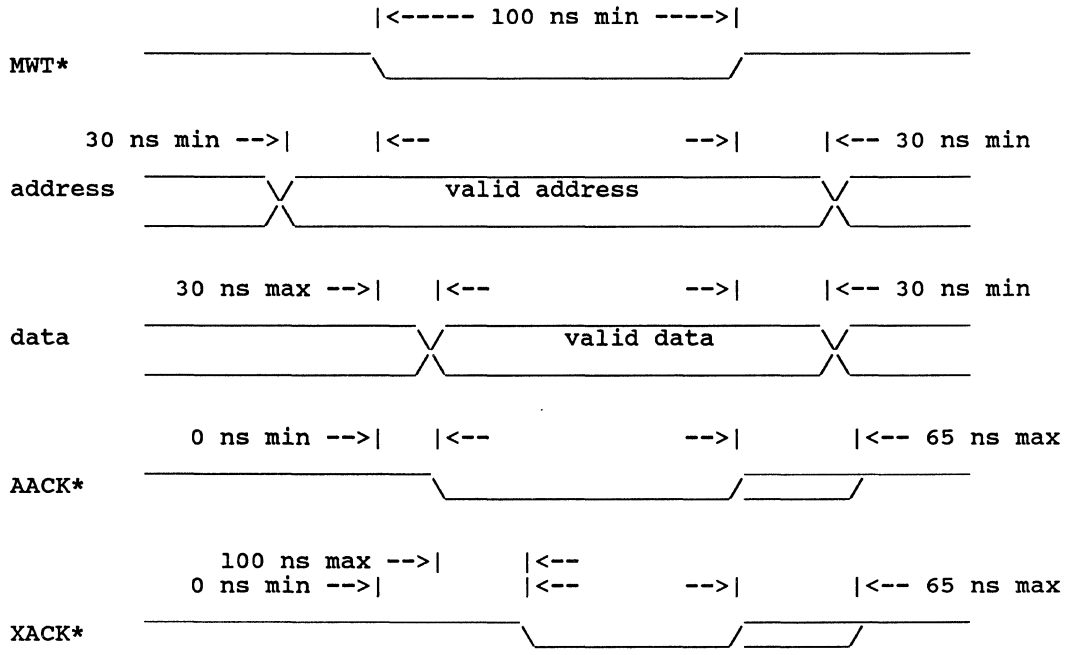


(asserted by slave on MRD* if parity error occurs)

I/O Write Timing. The following is the I/O write timing diagrams:



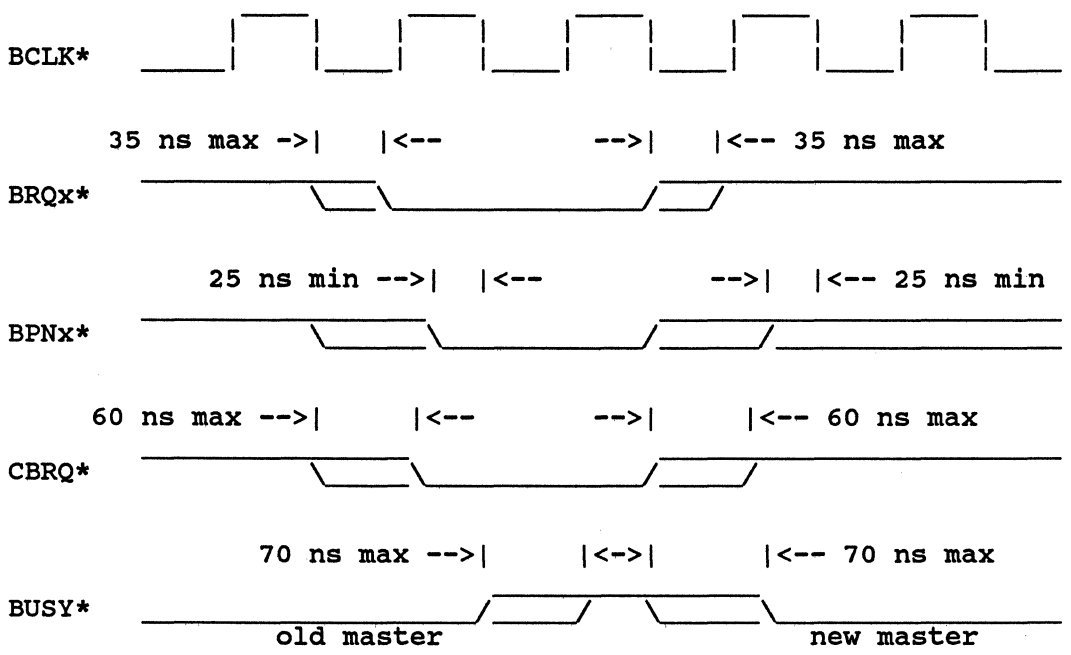
Memory Write Timing. The following is the memory write timing diagrams:



NOTE

Data can have -30 nanoseconds setup to MWT*.

Bus Exchange Timing. A 9.83 MHz bus clock is used for bus control timing. All bus exchange timing is referenced by the falling edge of BCLK*. The following is the bus exchange timing diagrams:



NOTE

1. A bus requester can receive bus priority and then lose bus priority before the bus is released (BUSY* deasserted) if a higher priority bus master has requested the bus before BUSY* was deasserted.

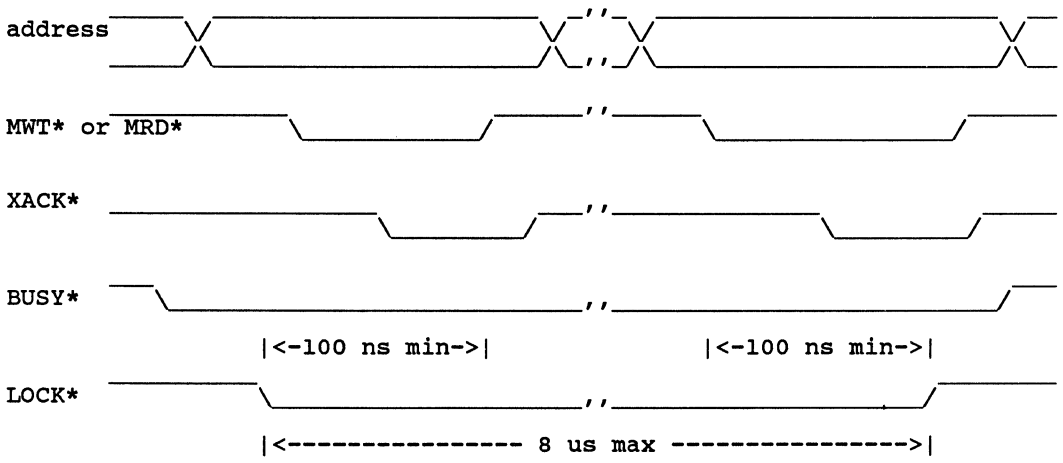
2. A bus master can assert its bus request, then deassert its bus request without taking ownership of the bus.

Bus Lock Timing. The current bus owner can keep the system bus indefinitely, by holding BUSY* asserted, if no other bus master requests the bus. If another bus master requests the bus, by asserting CBRQ*, the current bus master must release the bus within 8 microseconds.

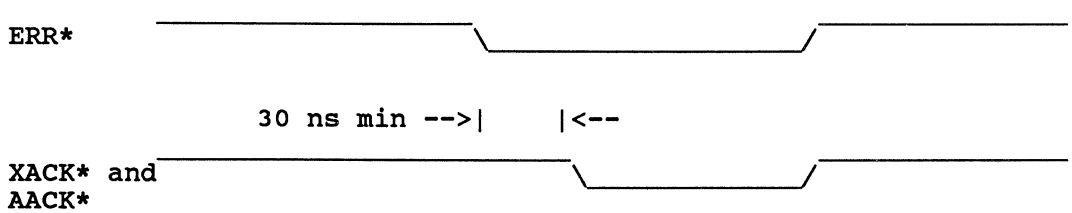
NOTE

The file processor is the only exception to releasing the bus in 8 microseconds. The file processor can hold the bus up to 200 microseconds regardless of how long the CBRQ* signal is asserted.

The LOCK* signal is used during read-modify-write operations to multiported memories. The addressed slave only allows access to the system bus owner when LOCK* is asserted. The following is the bus lock timing diagram:



Bus Timeout Timing. The following is the bus timeout timing diagram:



(BLANK)

Central Processing Unit (CPU) PCB

The function of the CPU PCB is to execute all the system and applications programs. Refer to the **Schematic Diagrams** supplement to this manual for the block and schematic diagrams of the CPU PCB.

The CPU PCB uses an 80286 microprocessor, an optional 80287 80-bit floating-point numeric processor extension (installed on the -002 version of the CPU PCB), PROM, local RAM, a calendar clock with battery back up, and a system bus interface.

The CPU PCB uses four major circuits: 80286 (and optional 80287 numeric processor), three independent controller units that control the local bus interface; translation table and tag RAM memory interfaces; and the cache and 32-bit system bus interface.

CPU Initialization

The 80286 microprocessor operates in two modes: real address and protected mode. When power-up or system reset occurs, the 80286 microprocessor powers up in the real address mode. The 80286 cannot be fully initialized without first switching to protected mode because the 80286 has no knowledge of the 16M byte addressing space and cannot access all of the areas of the memory map. Refer to the **Intel IAPX 286 Programmer's Reference Manual** for additional details on the 80286 initialization and protected-mode operation.

The cache, tag, and translation table memories all contain random data at power-up and must be initialized. To initialize the cache, all the valid bits of the tag RAM are written as invalid, which invalidates all data in the cache. The address translation table RAM must be written to assure proper system memory accesses.

All of the control bits in the output latch port are set low at power-up. Only one bit enables/disables the cache memory. Thus, all accesses to system memory will not use the cache until these bits are enabled.

The clear error status (CLR ERR STATUS*) bit will also be low which means that no nonmaskable interrupts (NMIs) can occur until this bit is set high.

Microprocessor

The CPU PCB uses a 16-bit 80286 microprocessor that provides memory management and support for the optional 80287 floating-point numeric processor. The 80286 microprocessor runs at 8 MHz and executes programs out of either PROM, cache, or system memory. The 80286 runs out of the cache memory with no wait states most of the time because most system and application programs address memory sequentially.

Microprocessor Address Decoder Logic

The address decoder PAL (7A) decodes the microprocessor address space into seven major decodes. The local bus decodes (LBS) signal is further decoded into four select signals. All input/ output (I/O), local and system, is memory mapped. All decodes except the bus I/O (BIO) are latched. The READY signal provides the window for the mapped address latch enable (MALE) signal to latch the proper decode. Refer to **Timing Diagrams** at the back of this section for detailed timing information.

80286 Memory Map

The 80286 memory map is shown in Figure 3-1. The local peripherals include the calendar clock, interrupt controller, output latch port, and input status port. The memory map also contains areas that include the translation table, cache memory, and tag RAMs. The accessibility of these RAMs provides the ability to change the address map and perform cache diagnostics.

The two remaining areas in the memory map are the system bus I/O space and the system bus memory space. When accessing the system bus I/O space, the I/O address is formed by using the lower 16 bits of the 80286 24-bit address. System memory accessing is discussed later.

Local Bus Control Logic

The local bus is controlled by the local bus controller PAL (19C). This PAL is a state machine with eight operating states. Any Ts bus state starts the state machine. In state one, the cycle is qualified by the EPROM, LBS (local bus select), INTA (interrupt acknowledge), or 80287 numeric processor decodes.

The state machine continues to operate if a local bus cycle is detected, otherwise it returns to the idle state. The controller asserts the local bus synchronous ready (LBSR) signal when finished and waits for the READY signal to be asserted and terminate the cycle. The LBS signal decode includes the clock/calendar, status port, control port, and interrupt controller. Refer to **Timing Diagrams** at the back of this section for detailed timing information.

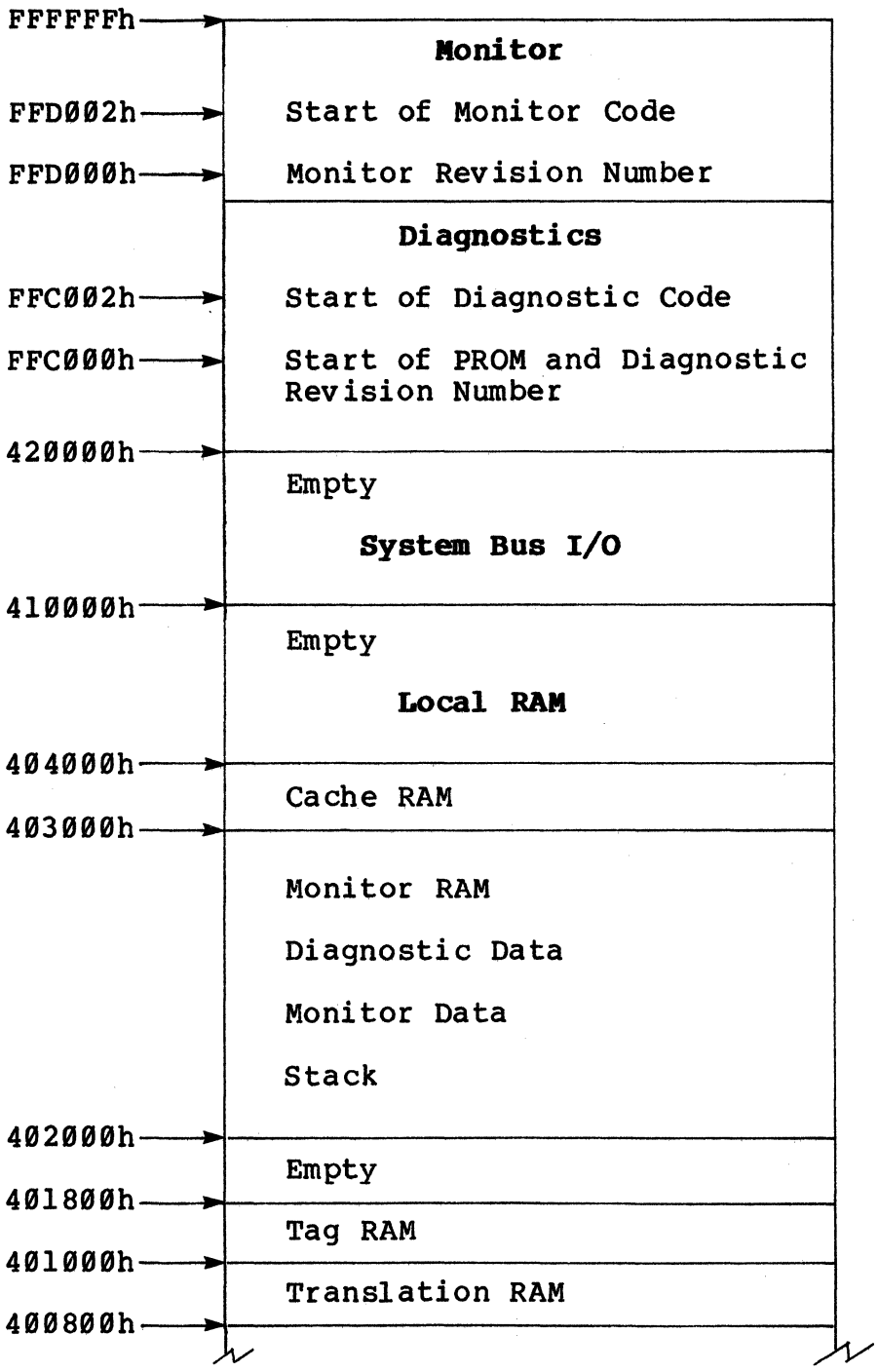


Figure 3-1. 80286 Memory Map

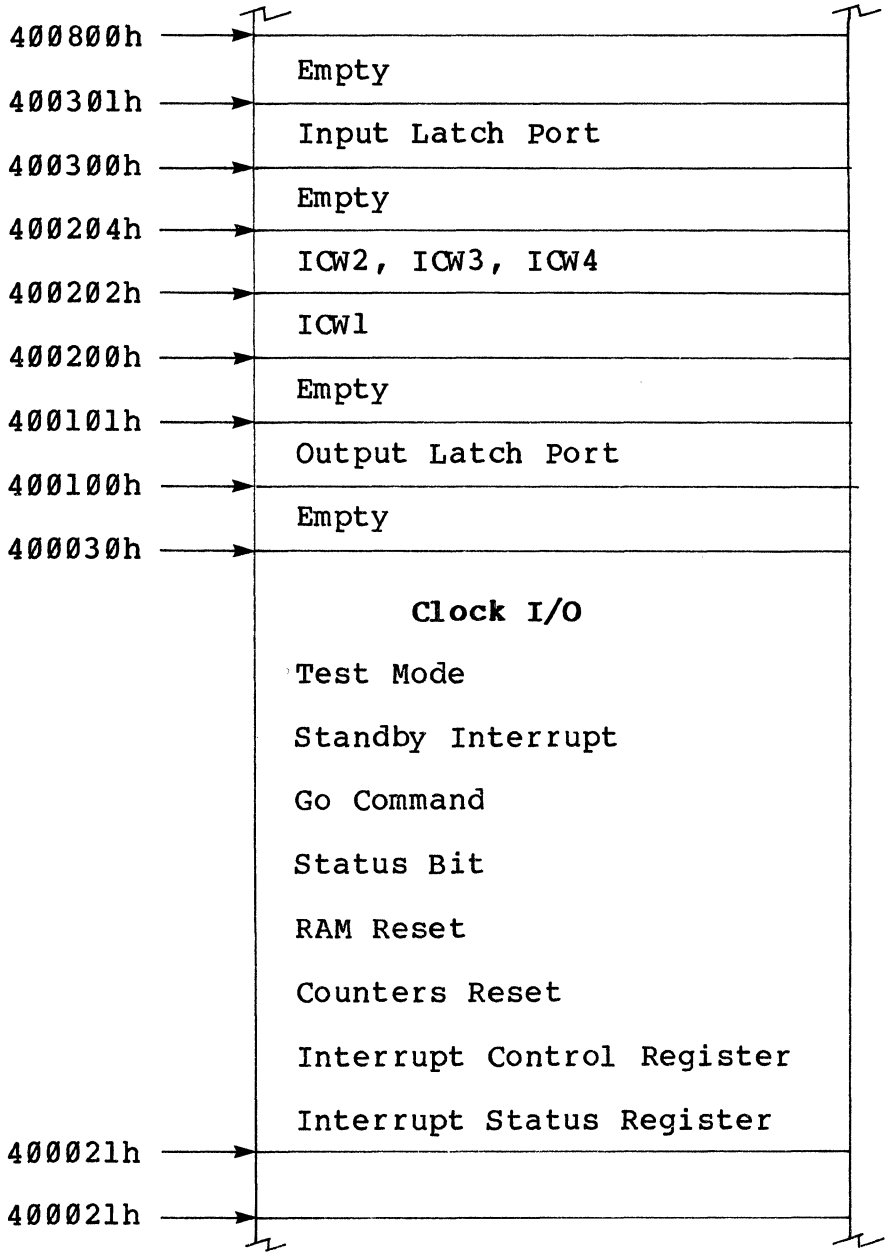


Figure 3-1. 80286 Memory Map (Cont.)
Clock RAM

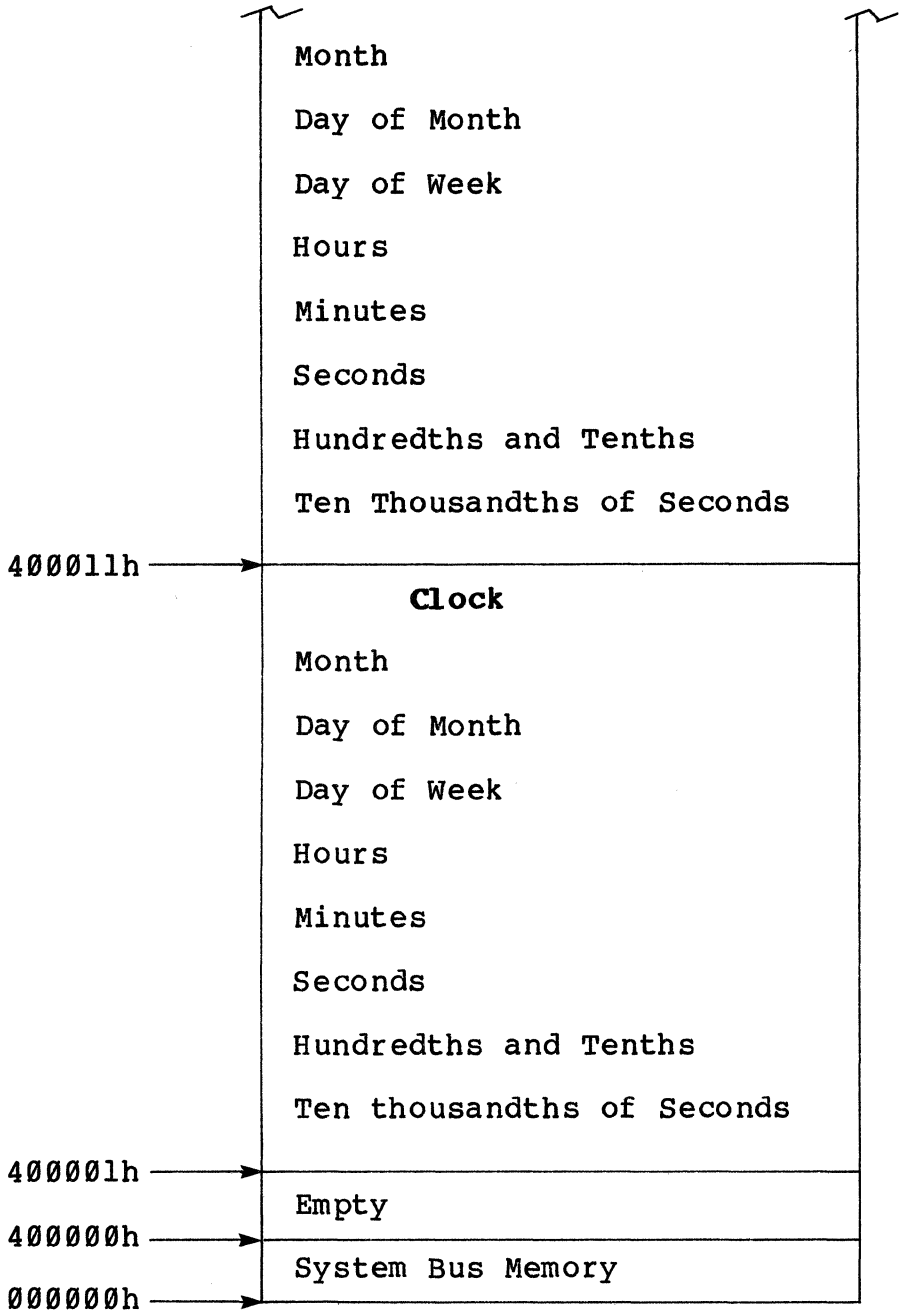


Figure 3-1. 80286 Memory Map (Cont.)

Local Bus

The local bus on the CPU PCB handles data transfers for the PROM, calendar clock IC, interrupt controller, input status port, and output latch port. The bit definitions of the input status port and the output latch port are listed in Tables 3-1 and 3-2.

Boot and initialization programs are contained in the PROM. The CPU PCB can support either 16K or 32K bytes of boot program (use 32K bytes when out of program space on 16K bytes).

Table 3-1. Input Status-Port Bit Definitions

Bit	Logic Level	Description
DO	Ø	Jumper installed between pins 7 and 8 of connector E2. Enables diagnostic loop-on-error
	1	No jumper between pins 7 and 8 of E2
D1	Ø	Jumper installed between pins 5 and 6 of connector E2
	1	No jumper between pins 5 and 6 of E2
D2	Ø	Jumper installed between pins 3 and 4 of connector E2
	1	No jumper between pins 3 and 4 of E2
D3	Ø	Jumper installed between pins 1 and 2 of connector E2
	1	No jumper between pins 1 and 2 of E2
D4	Ø	System bus timeout* bit inactive
	1	System bus timeout bit active (bus timeout occurred)
D5	Ø	Uninterruptable power source (UPS) supplying power (normal operation)
	1	Uninterruptable power source (UPS) supplying power (power-fail condition)

Table 3-1. Input Status-Port Bit Definitions (Cont.)

Bit	Logic Level	Description
D6	Ø	Latched UPS power-fail condition inactive
	1	Latched UPS power-fail condition active (power-fail occurred)
D7	Ø	Latched bus error bit inactive
	1	Latched bus error bit active (bus error occurred)**

* Timeout occurs when any bus command (IORD, IOWT, MRD, MWT) exceeds 4 microseconds.

** Bus error set: (1) by memory PCB on a read if a parity error is detected, or (2) when a CPU generated bus timeout has occurred on memory operations only.

Table 3-2. Output-Latch Bit Definitions

Bit*	Level	Description
DO	Ø	Cache disabled
	1	Cache enabled
D1	Ø	System bus INT6 inactive
	1	System bus INT6 active
D2	Ø	System bus INT5 inactive
	1	System bus INT5 active
D3 D4 D5		Not connected
D6		Forces system bus write on cache search
D7	Ø	CLR ERR STATUS active
	1	CLR ERR STATUS inactive

* All these bits are used by power-up diagnostics.

Calendar Clock

The calendar clock is a National 58167 IC that keeps time and generates system time slice interrupts. Refer to the **National 58167 Applications Note Data Handbook** for operating details.

Interrupt Controller

The interrupt controller is an Intel 8259A-2 IC. Refer to the **Intel Microsystem Components Handbook** for additional operating details. The interrupt controller takes interrupts from the calendar clock IC and system bus interrupt lines. The interrupt request levels are described in Table 3-3.

Table 3-3. Interrupt Request Levels

Priority	IC Pin	Description
1	1RO	Calendar clock interrupt
2	1R1	System bus INTØ
3	1R2	System bus INT1
4	1R3	System bus INT2
5	1R4	System bus INT3
6	1R5	System bus INT4
7	1R6	System bus INT5
8	1R7	System bus INT6

System Memory Accessing and Address Translation

The 8Ø286 microprocessor, in protected mode, has a virtual address space of 1G (giga) byte and physical address space of 16M bytes. The 8Ø286 internal memory management makes the translation from virtual to physical memory. Refer to the **Intel IAPX 286 Programmer's Reference Manual** for a description of the 8Ø286 memory management operation.

The 16M byte physical address space is used for all I/O and memory accessing except transfer to/from the optional 8Ø287 floating-point processor.

A memory map for the physical address space is shown in Figure 3-2. The translation RAM can be set up to access memory anywhere within the 16M byte physical address space. Note that the low 4M bytes of the 80286 physical address space is mapped into the system bus memory address space.

The system-bus memory address is formed by concatenating the lower 12 bits of the 80286 physical address with the 12-bit output of the translation RAM. The low order bits of the 80286 form bits 0-11 of the system bus address and the 12 bits from the translation RAM form bits 12-24 of the system bus address. Each location in the translation table covers 4K bytes of the system memory address space. There are 1024 locations in the translation table.

The contents of the translation table are treated as memory mapped and are accessible as part of the 80286 address space. The translation table memory must be read and written with 16 bit transfers; no byte transfers are allowed. The translation table contents are initialized as described in Table 3-4. Table 3-5 lists the translation-table bit definitions.

Table 3-4. Translation-Table Addresses

Block	Port Address (Hex)	80286 Address Range (Hex)
000	400800	000000 - 000FFF
001	400802	001000 - 001FFF
002	400804	002000 - 002FFF
.	.	.
.	.	.
.	.	.
.	.	.
.	.	.
3FF	400FFE	3FF000 - 3FFFFF

NOTE

During system operation, the block numbers and 80286 address range are not mapped one-to-one.

Table 3-5. Translation-Table Bit Definitions

Bit	Description
0	System bus memory address bit 12
1	System bus memory address bit 13
2	System bus memory address bit 14
3	System bus memory address bit 15
4	System bus memory address bit 16
5	System bus memory address bit 17
6	System bus memory address bit 18
7	System bus memory address bit 19
8	System bus memory address bit 20
9	System bus memory address bit 21
10	System bus memory address bit 22
11	System bus memory address bit 23

Tag and Translation RAM Control Logic

The tag and translation RAM control logic is contained in the tag and translation RAM controller PAL (2B). The state machine PAL (1B) starts on CPU system memory, tag and translation RAM I/O, and non-CPU system memory write operations. During CPU memory operations, the tag and translation table data are compared for a match (hit) which indicates that the cache is saving that address.

On CPU reads, a hit indicates that the cache data is valid and, thus, the cache data is read instead of system memory. A miss causes system memory to be accessed. On CPU writes, no operation is performed.

System bus memory writes (non-CPU) are monitored for a CPU cache hit. If a hit occurs, the corresponding tag for the cache data is invalidated because cache data and system memory are not the same. During tag and translation table I/O operations, the appropriate

address and data buffer enable, and RAM control signals are generated. Refer to **Timing Diagrams** at the back of this section for detailed timing information.

Cache Memory Organization

The cache memory on the CPU PCB is a 4K byte singleset associating cache (directly mapped) with a block size of 4 bytes that includes both instructions and data. The cache memory will cache data from anywhere in the 16M byte address space of the system bus (if the translation table is appropriately set up).

The cache memory uses three bit fields of the 24 bit system bus memory address as shown in Figure 3-2. These bit fields are the tag field, the offset field, and the byte-select field.

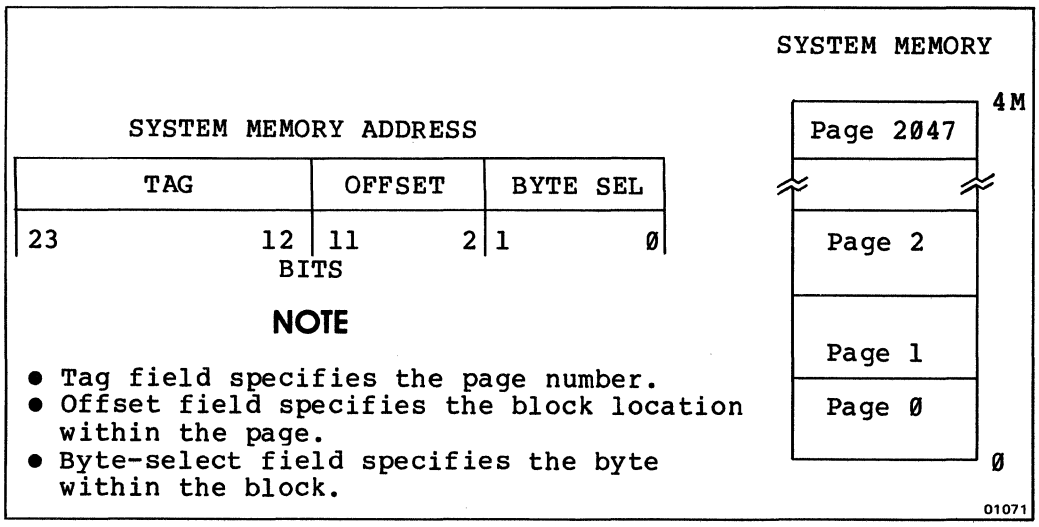


Figure 3-2. Cache Memory Organization

The tag field effectively breaks up the memory space into a number of pages. The byte location within a page is specified by the offset and byte-select fields.

When a block from system memory is stored in the cache memory, the offset field specifies where in the cache that particular block will be stored. The offset field also specifies where in the tag memory the tag for the memory location should be stored. The value loaded into the tag memory is the page number from which the memory block came.

When a memory read occurs, the offset field will specify a location in the tag memory. If the page number in the tag memory matches the page number in the translation table, then a hit occurs and a copy of the desired memory location resides in the cache memory. This operation is called a cache memory search as shown in Figure 3-3.

A write-through technique keeps the data in cache memory identical to the data in system memory during CPU writes. The cache memory is written whenever a memory write with a cache hit occurs or when a memory read with a cache miss occurs. When a memory-read cache miss occurs, a 4 byte block is loaded into the cache memory. Since the 80286 fetches instructions 16 bits at a time, sequential accesses should produce a cache hit for every other memory read.

The cache control logic is contained in the cache control PALs (17C, 18C). The state machine PAL (17C) starts on a cache RAM I/O, bus memory, or bus I/O operation and finishes when the READY signal is asserted. There are 8K bytes of local RAM memory with 4K bytes used for the cache memory and the remaining 4K bytes are for general-purpose use. All 8K bytes of local memory are accessible with a cache RAM I/O (CIO) operation.

If a hit occurs during a memory read, the cache RAM is read instead of system memory. If a miss occurs during a memory read, system memory is read and the tag RAM is updated. If a hit occurs during a memory write, both the cache RAM and system memory are written. If a miss occurs during a memory write, only system memory is written.

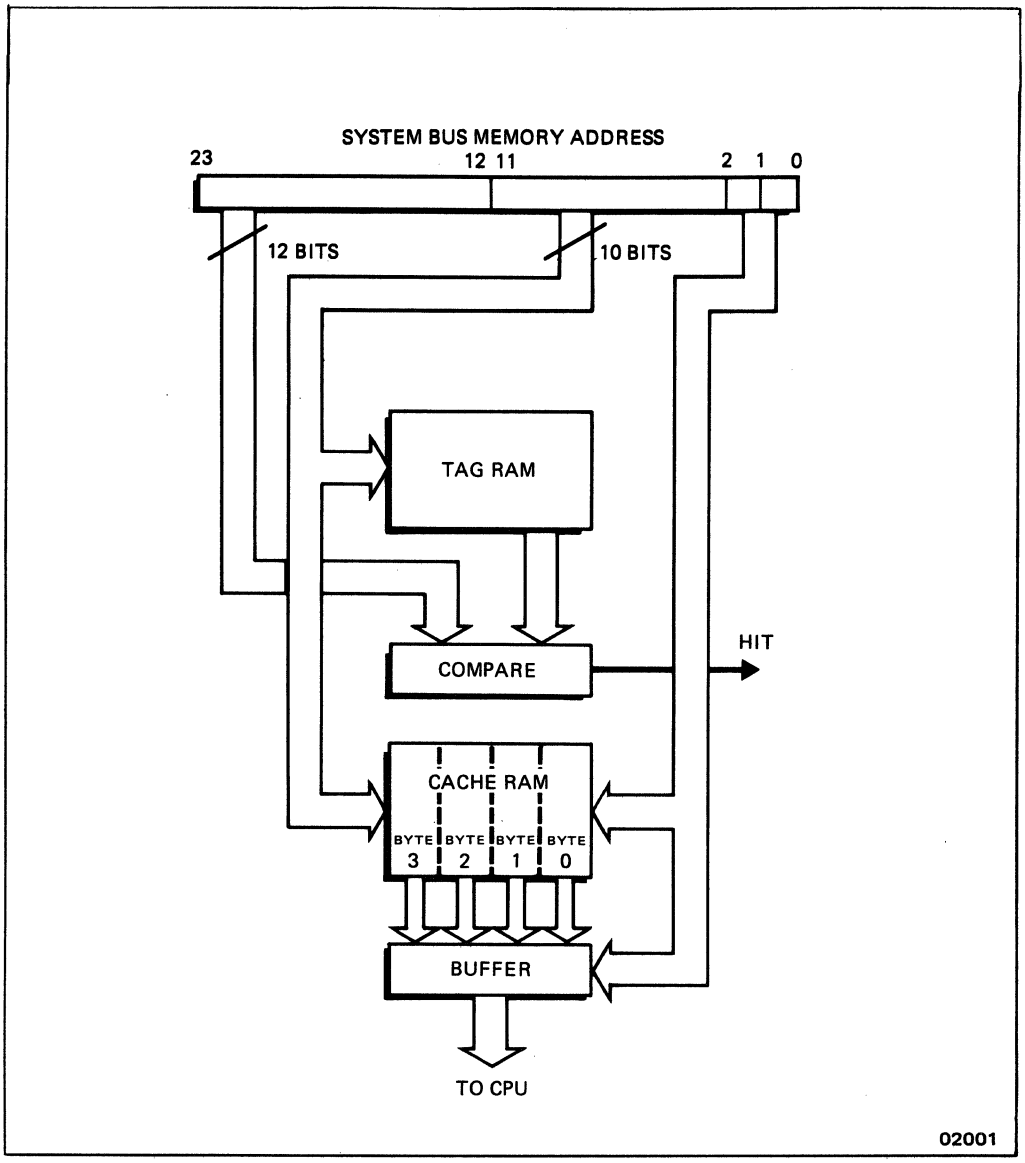


Figure 3-3. Cache Memory Search

If the CPU does not own the system bus, a bus request (BUSREQ) signal is generated for all bus I/O and system memory write and read (miss) operations. Refer to **Timing Diagrams** at the back of this section for detailed timing information.

The cache control logic also guarantees cache data coherency with system memory by performing cache searches for all system memory writes generated by other system bus masters, such as, I/O serial or file processors. If such a cache search produces a hit, then that cache memory location will be marked as invalid which guarantees that only valid data can be read from the cache.

The tag and cache memories can be directly read and written by the 80286 for diagnostic and initialization purposes. The address locations of the tag and cache memories are shown in Figure 3-2. The tag memory must be read and written with 16-bit transfers, no byte transfers are allowed. The cache memory can be accessed as either bytes or words. The bit definitions for accessing the tag memory are listed in Table 3-6.

Table 3-6. Tag-Memory Bit Definitions

Bit	Description
D0	Page number bit 0
D1	Page number bit 1
D2	Page number bit 2
D3	Page number bit 3
D4	Page number bit 4
D5	Page number bit 5
D6	Page number bit 6
D7	Page number bit 7
D8	Page number bit 8
D9	Page number bit 9
D10	Page number bit 10
D11	Page number bit 11
D12	Valid bit *

* The cache data is valid when the valid bit is 0 and invalid when the valid bit is 1.

System Bus Arbiter and Priority Encoding Logic

The system bus arbiter and priority encoder PAL (11D) arbitrates and encodes the system bus requests from the bus masters.

When a bus master wants the bus, its bus request and common bus request signals are asserted. The highest priority request is encoded in the A, B, and C outputs and decoded externally to give a bus grant to the requesting master. While the bus master has the bus, the BUSY signal is asserted. The common bus request (CBRQ) signal is used to determine if another bus master wants the bus. When BUSY is cleared and a bus grant (BPNØ-7) signal is asserted the bus can be acquired by another bus master. Refer to **Timing Diagrams** at the back of this section for detailed timing information.

Microprocessor Ready Generator

The ready generator for the 8Ø286 microprocessor is contained in the ready generator PAL (9D). Clock 1 and 2 are phase synchronized with the mapped address latch enable (MALE) and READY signals.

The READY signal is asserted when either the local bus ready (LBSR), tag or translation table synchronous ready (TTSR), or cache synchronous ready (CSR) signals is asserted or, on the second phase of Tc, when the advanced transfer acknowledge (AACK) signal from the system bus is asserted.

Jumper Descriptions

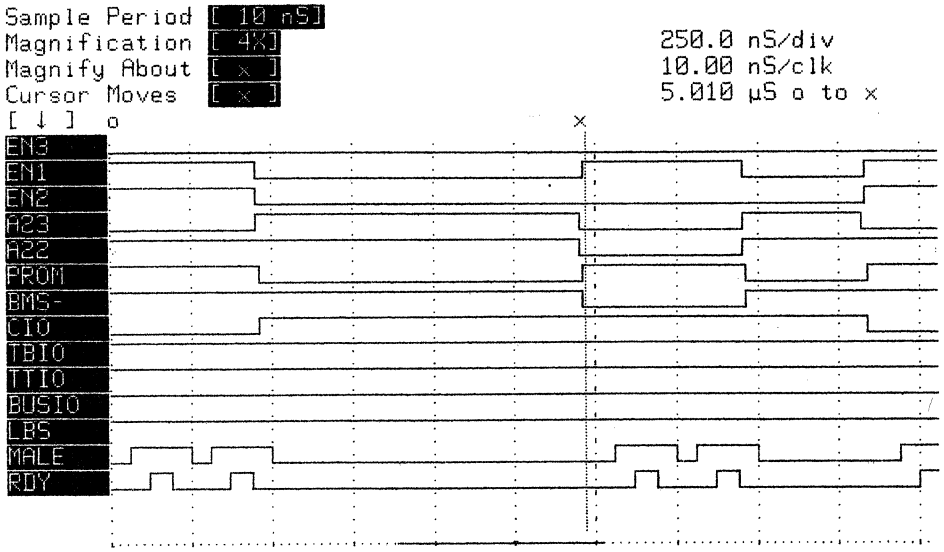
The CPU PCB has eight jumper connectors designated E1 through E8. These jumpers are properly installed at the factory and should not be changed. Table 3-7 describes the functions of the jumper connectors. The descriptions apply for both the -ØØ1 and -ØØ2 versions of the CPU PCB unless specified otherwise. Refer to Appendix A for detailed jumpering information.

Table 3-7. Jumper Descriptions

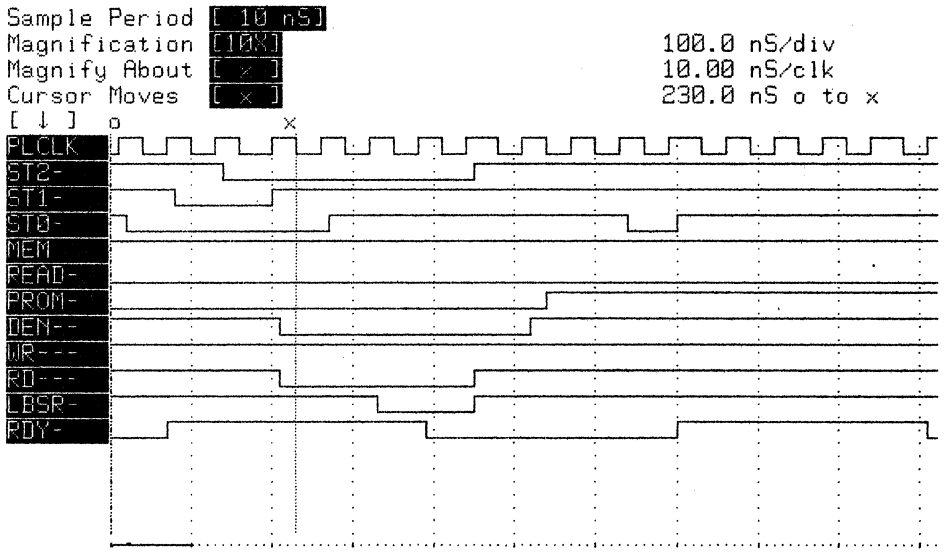
Connector Designation	Description
E1	Generates a manual NMI (pins 1 and 2 jumpered)
E2	Used by software. Provides configuration bit 3 (pins 1 and 2 jumpered); configuration bit 2 (pins 3 and 4 jumpered); configuration bit 1 (pins 5 and 6 jumpered); forces power-up diagnostics to loop on error (pins 7 and 8 jumpered)
E3	Enables priority bus arbiter for the system (pins 1 and 3 jumpered). Disables priority bus arbiter for the slave CPU (pins 2 and 4, and 5 and 6 jumpered)
E4	Enables the CPU reset to drive the system reset (pins 1 and 2 jumpered)
E5	Adds bus grant no. 6 to the priority bus arbiter for the slave CPU (pins 1 and 2 jumpered)
E6	**-ØØ2 version only.** Divides the 8Ø286 clock by 3 (5.33 MHz) for use by the 8Ø287-3 numeric processor (pins 1 and 2, and 4 and 6 jumpered). Supplies the clock generated by the 8284, which is 24 MHz divided by 3 (8 MHz) for use by the 8Ø287-8 numeric processor (pins 1 and 3, and 5 and 6 jumpered)
E7	Enables the system bus clock (pins 1 and 2 jumpered)
E8	Testability jumper. Automatic test equipment (ATE) generates an 8Ø286 microprocessor clock during testing

Timing Diagrams

The major timing diagrams for the CPU PCB are shown in Figure 3-4.

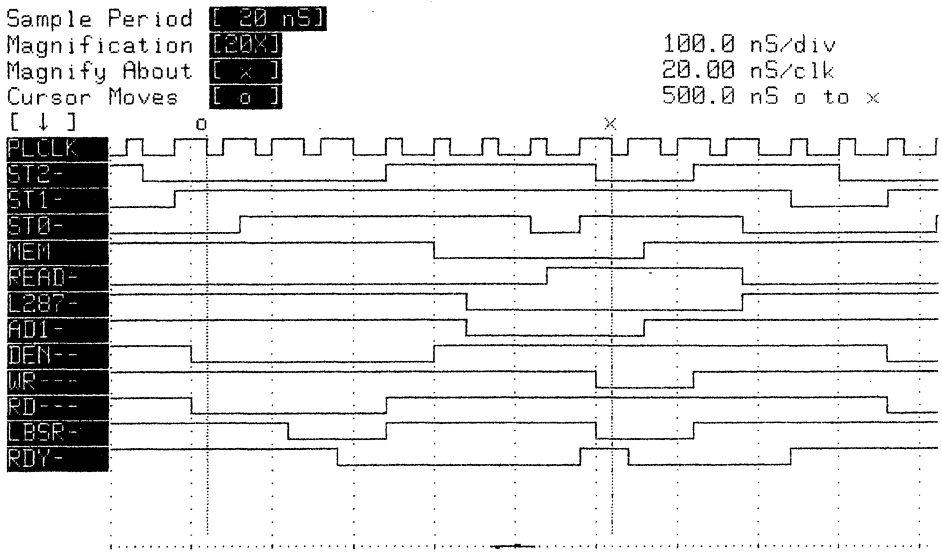


7A - Address Decoder PAL

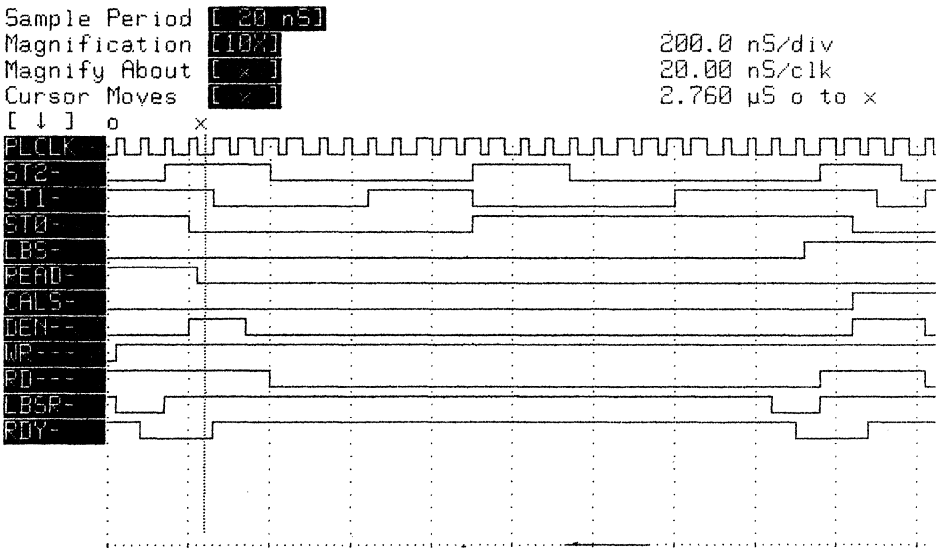


19C - Local Bus State Machine PAL (PROM Read Cycle)

Figure 3-4. CPU PCB Timing Diagrams

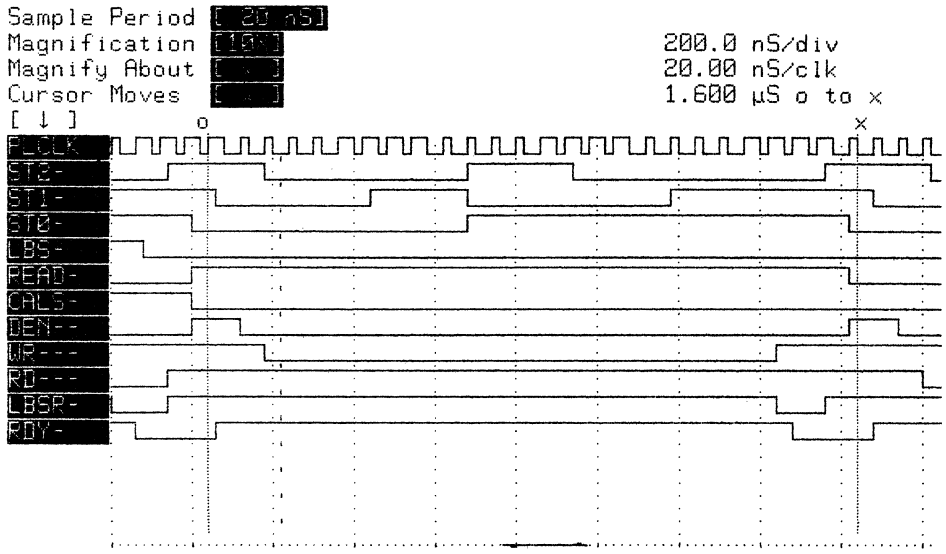


19C - Local Bus State Machine PAL (80287 Write Cycle)

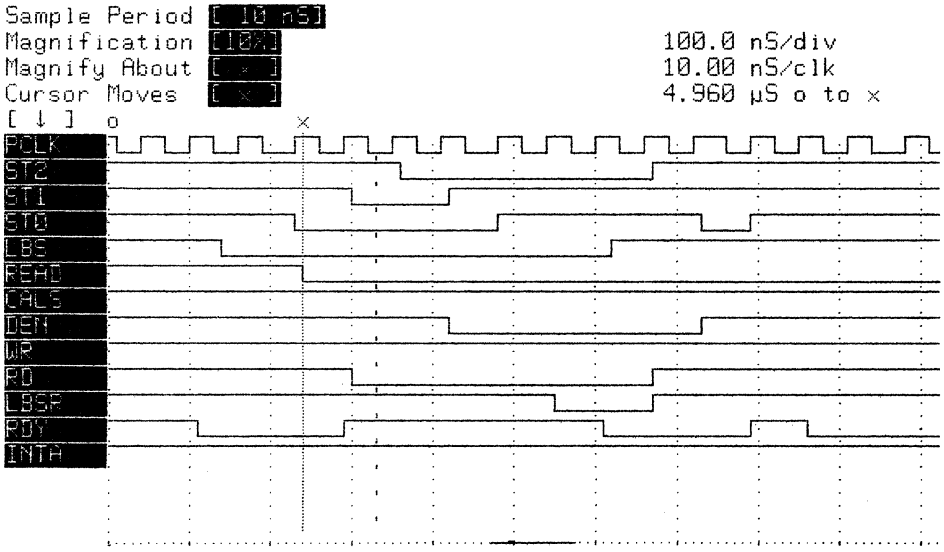


19C - Local Bus State Machine PAL (Calendar Clock Read Cycle)

Figure 3-4. CPU PCB Timing Diagrams (Cont.)

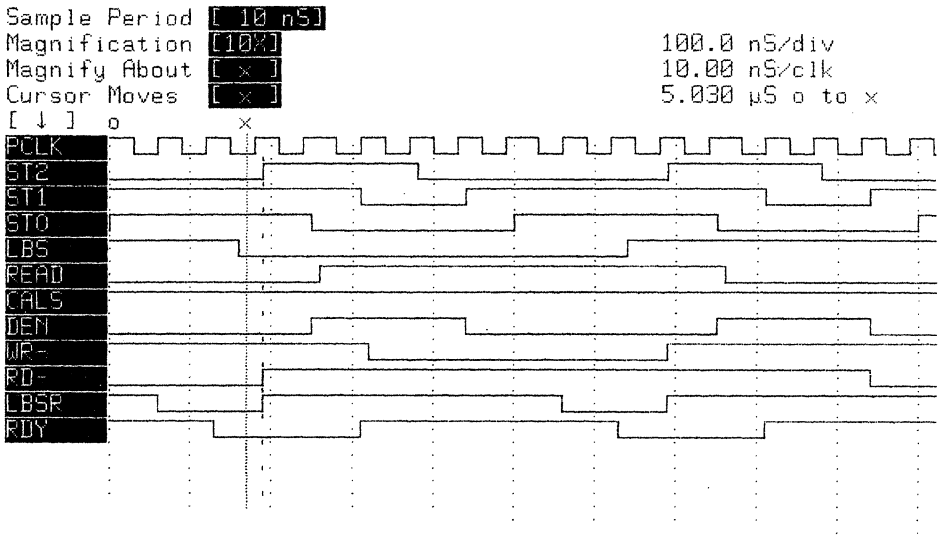


19C - Local Bus State Machine PAL
(Calendar Clock Write Cycle)

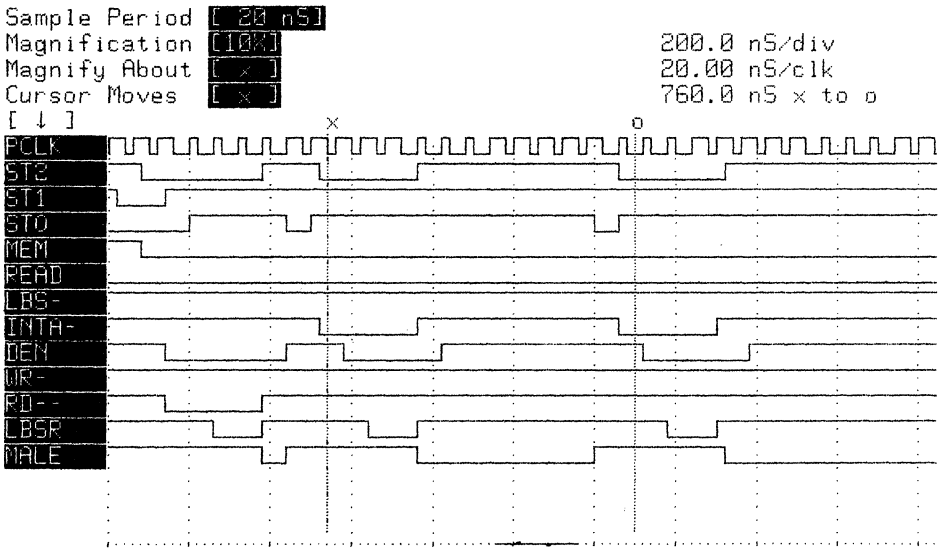


19C - Local Bus State Machine PAL
(Status Port/Control Port/Priority Interrupt Controller Read Cycle)

Figure 3-4. CPU PCB Timing Diagrams (Cont.)

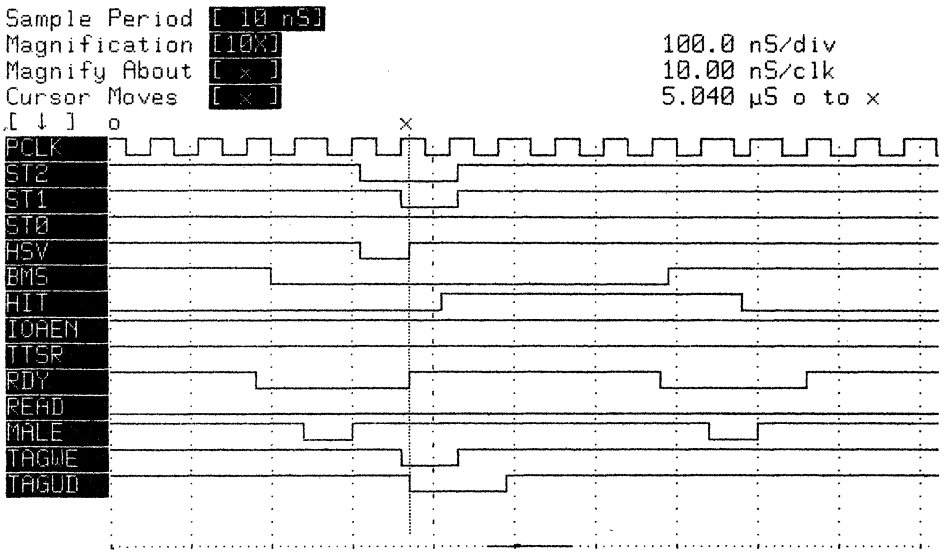


19C - Local Bus State Machine PAL (Status Port/Control Port/Priority Interrupt Controller Write Cycle)

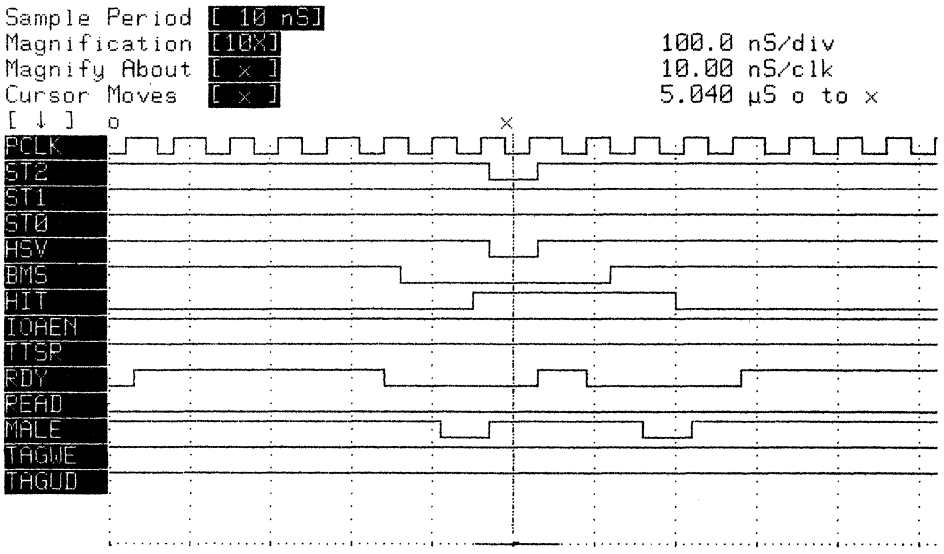


Interrupt Acknowledge Cycle

Figure 3-4. CPU PCB Timing Diagrams (Cont.)

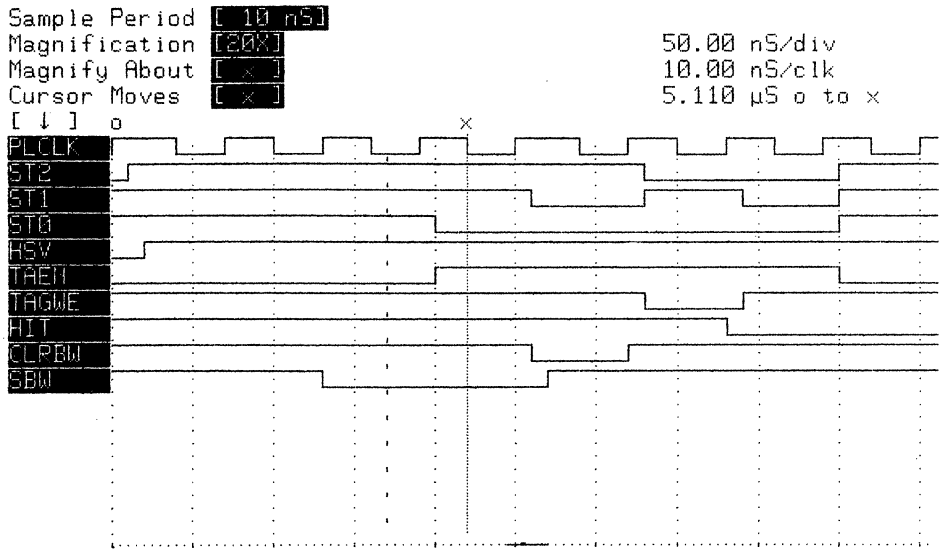


1B, 2B - Tag State Machine PALs (System Memory Read Miss)

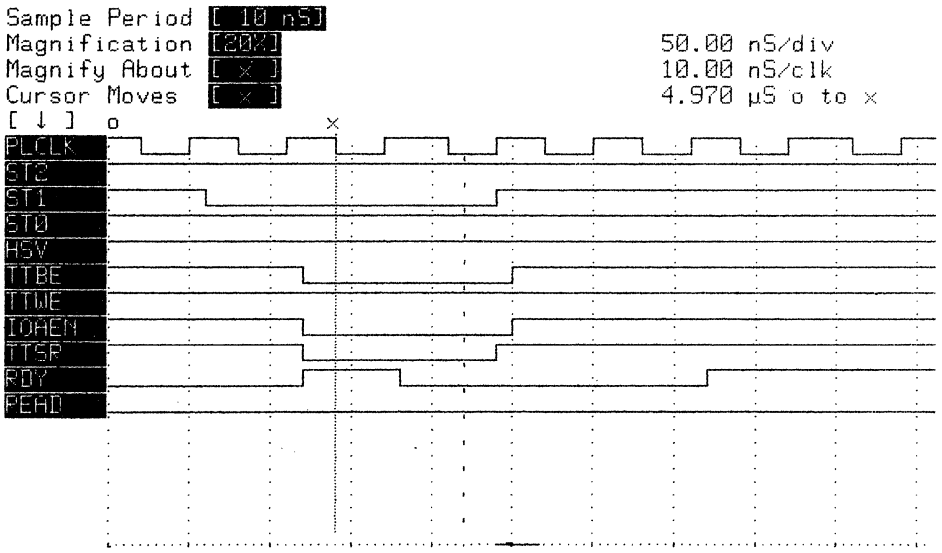


1B, 2B - Tag State Machine PALs (System Memory Read Hit)

Figure 3-4. CPU PCB Timing Diagrams (Cont.)

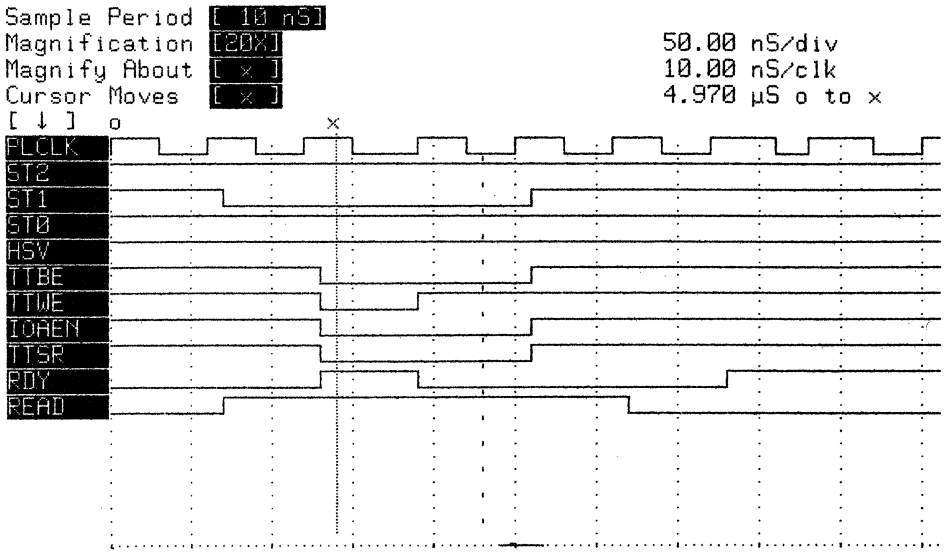


1B, 2B - Tag State Machine PALs
(System Bus Write Monitoring)

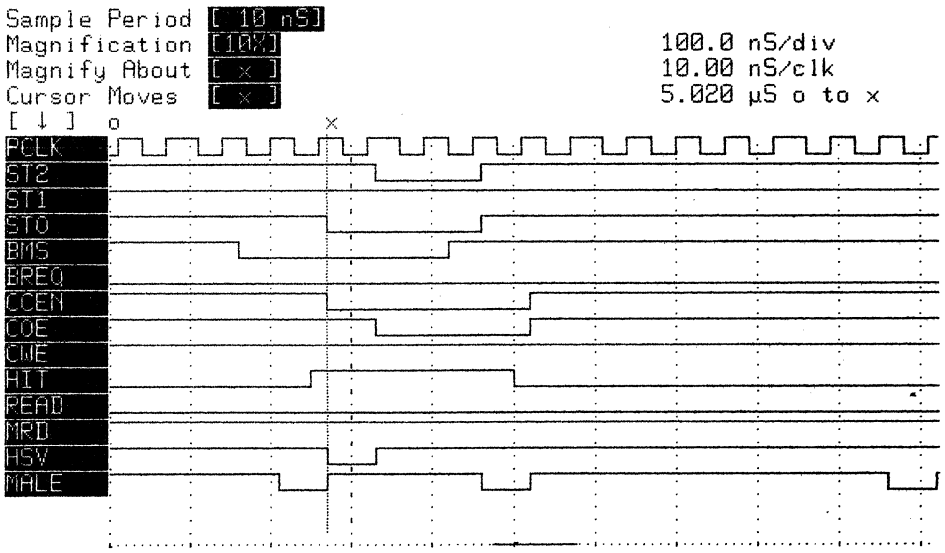


1B, 2B - Tag State Machine PALs
(Tag/Translation Table I/O Read Cycle)

Figure 3-4. CPU PCB Timing Diagrams (Cont.)

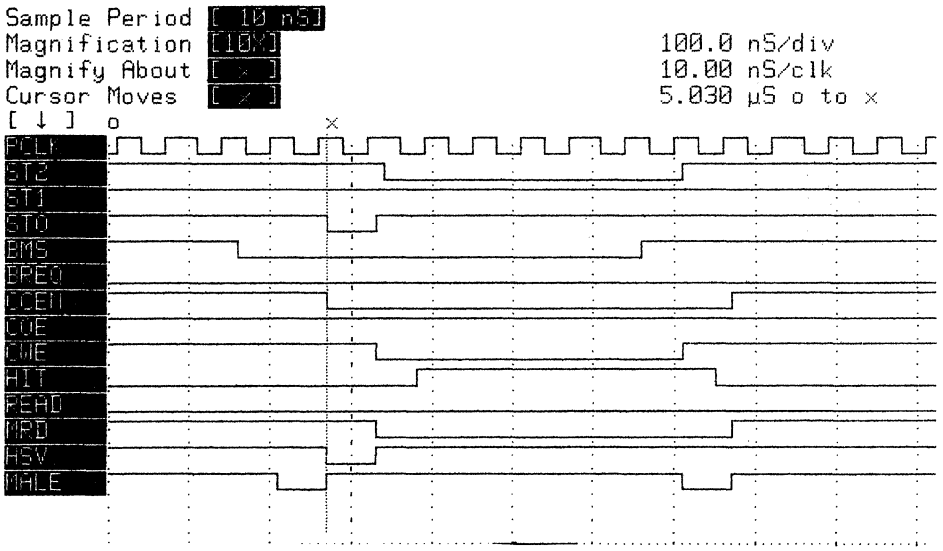


1B, 2B - Tag State Machine PALs
(Tag/Translation Table I/O Write Cycle)

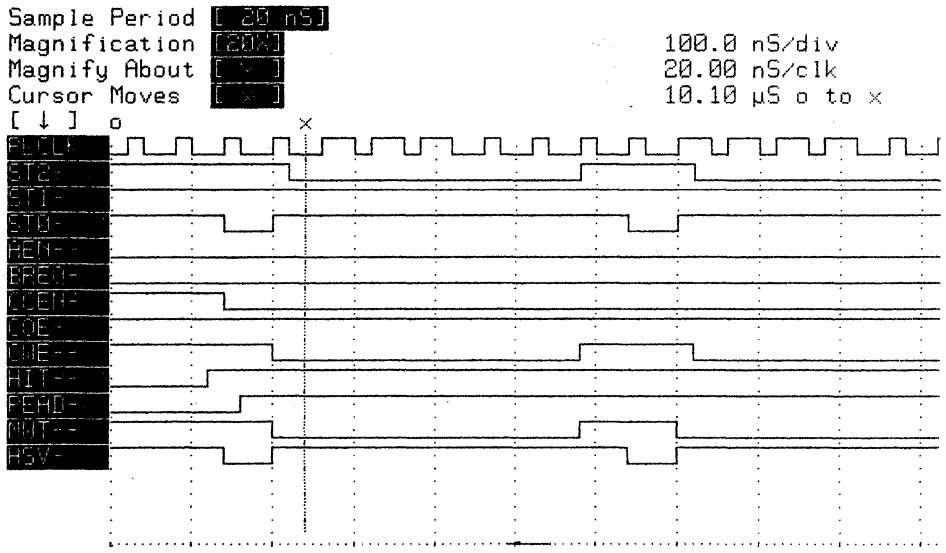


17C, 18C - Cache State Machine PALs
(System Memory Read Hit Cycle)

Figure 3-4. CPU PCB Timing Diagrams (Cont.)

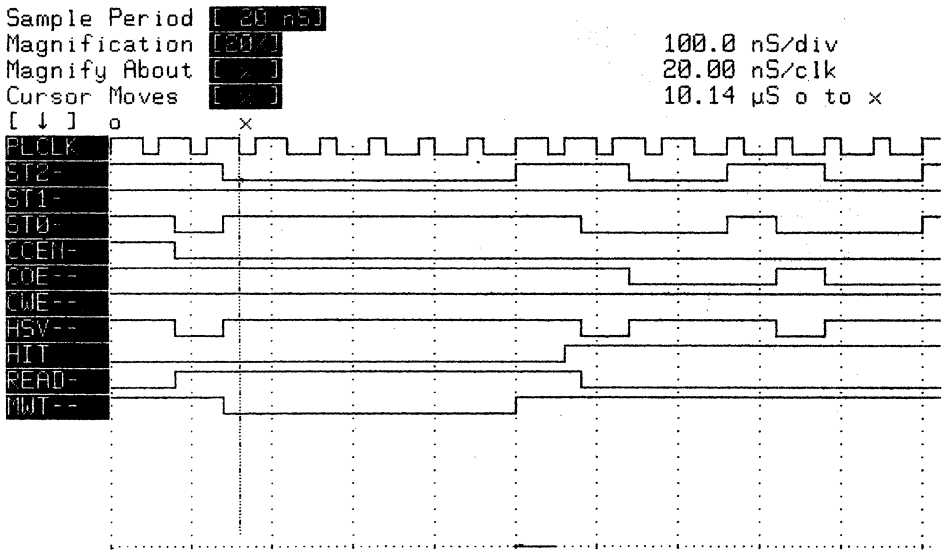


17C, 18C - Cache State Machine PALs
(System Memory Read Miss Cycle)

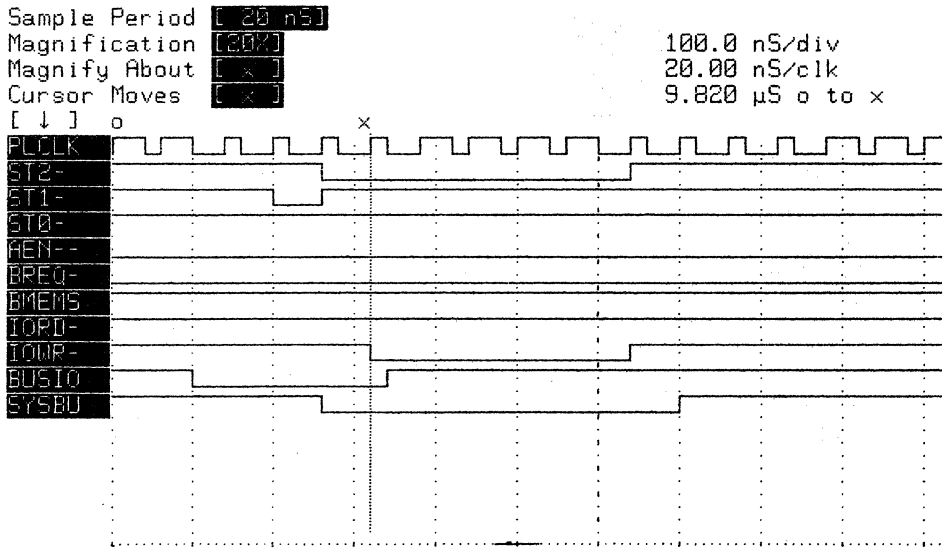


17C, 18C - Cache State Machine PALs
(System Memory Write Hit Cycle)

Figure 3-4. CPU PCB Timing Diagrams (Cont.)

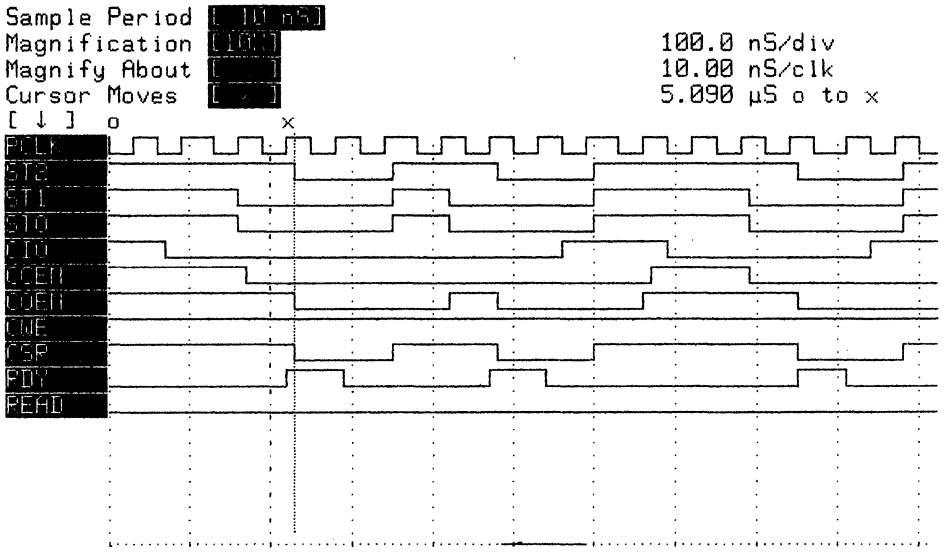


17C, 18C - Cache State Machine PALs (System Memory Write Miss Cycle)

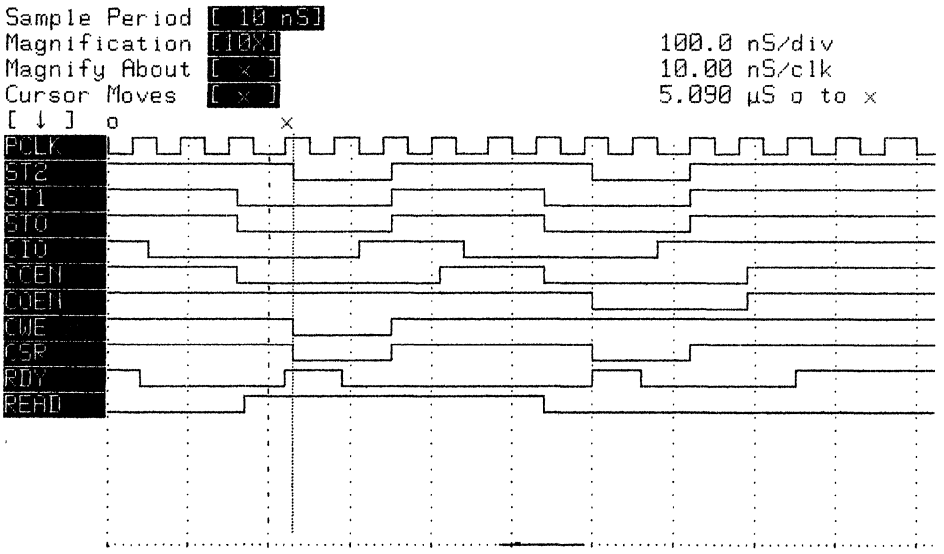


17C, 18C - Cache State Machine PALs (System Bus I/O Write Cycle)

Figure 3-4. CPU PCB Timing Diagrams (Cont.)

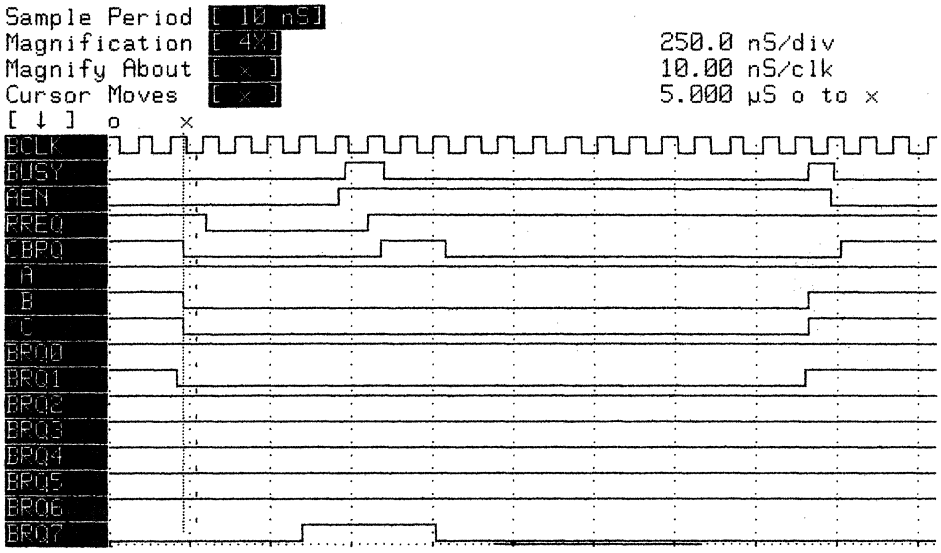


17C, 18C - Cache State Machine PALs (Cache I/O Read Cycle)

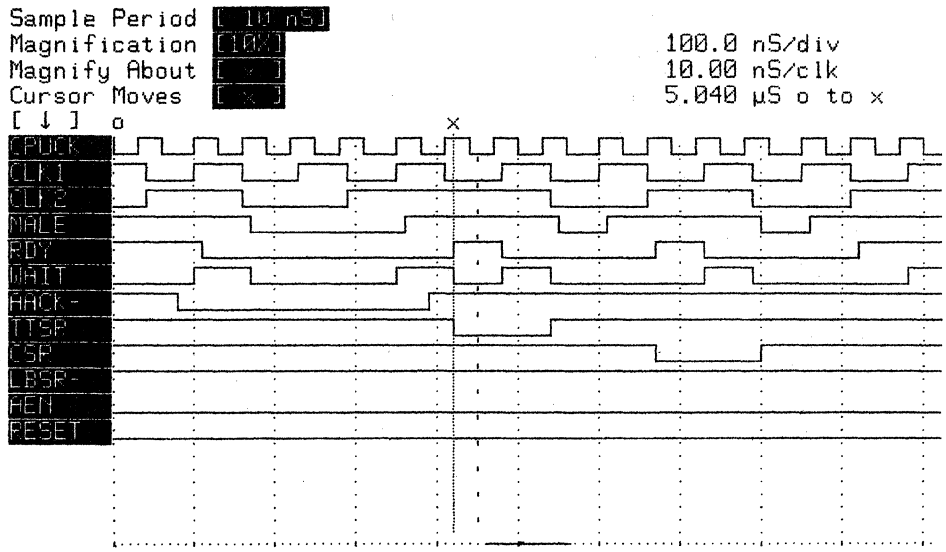


17C, 18C - Cache State Machine PALs (Cache I/O Write Cycle)

Figure 3-4. CPU PCB Timing Diagrams (Cont.)



System Bus Arbitration



9D - Ready Generator PAL

Figure 3-4. CPU PCB Timing Diagrams (Cont.)

Memory PCB

The function of the memory PCB is to provide 1M, 2M, or 4M bytes of dynamic RAM for the system. There are two versions of the the memory PCB used in this system: version 1 (part no. 615-15146-XXX) and version 2 (part no. 615-16509-XXX). Both versions are nearly identical. The following information applies to both versions with information for version 2 included in parenthesis. Refer to the **Schematic Diagrams** supplement to this manual for the block and schematic diagrams of the applicable memory PCB.

The memory PCB uses 64K x 1 bit dynamic RAMs to provide 1M byte of system memory or 256K x 1 bit dynamic RAMs to provide 2M or 4M bytes of system memory. Multiple memory PCBs with different capacities can be used to expand system memory to 16M bytes (provided the necessary PCB slots are available in the existing configuration). Each version of the memory PCB is fully compatible with the others, which allows the system to be upgraded in the field.

System memory is organized into long words of 32 bits with byte parity detection. (Version 2 is organized into double long words of 64 bits with byte parity detection. The double long words are multiplexed onto the system bus by two sets of 32-bit transceivers.) Transfers to/from memory can be made in 8, 16, or 32-bit widths as required by the bus master. Each memory read cycle causes all 32 (or 64) bits to be checked for proper parity, although not all the bits may be transferred to the bus master.

Refresh for the dynamic RAMs is handled on each memory PCB, and is fully transparent to the bus master. This makes the memory look static to the requestor.

System Bus Interface

Since it is possible to have multiple memory PCBs in the system, a board-select comparator on each memory PCB is set (by jumpers on connectors E1 and E2) to uniquely address each PCB within the system memory space.

When multiple PCBs are used, the proper jumper configuration ensures that, when viewed from any bus master, a single contiguous memory space exists regardless of the number or type of memory PCBs.

Data transfer to/from a memory PCB is initiated by either a memory read command and a board-select address match or a memory write command and a board-select address match.

Once the transfer is initiated, 1, 2, or 4M bytes of data are transferred to/from the memory PCB depending upon the state of four bus signals: HWEN* (high word enable), HBEN* (high byte enable), A1* (address bit 1), and A0* (address bit 0). These four signals control the data transceivers to/from the system bus, as well as the write-enable lines to the RAMs. (Version 2 has six bus signals: HWEN*, HBEN*, HLWEN* (high long word enable), A0, A1, and A0.)

The selected memory PCB also produces three signals to indicate the status of the data transfer:

1. AACK* - Advanced data transfer acknowledge

2. XACK* - Data transfer acknowledge

3. ERR* - Error

Signal AACK* goes true before the transfer of valid data is complete, and acts as an advanced version of XACK* to signal the bus master when the requested bus transaction is about to be completed. Signal AACK* is used by some bus masters (CPU, file processor, or communications subsystems) to reduce wait states. Signal XACK* goes true to acknowledge transfer and signal the bus master that valid data has been placed or accepted on the bus.

Signal ERR* is the general bus error signal, which the selected memory PCB drives with the results of the on-board parity checkers. Signal ERR* is only active during memory read cycles when a parity error is detected, and will be valid about 25 nanoseconds after XACK* goes true. Signal ERR* is monitored by each bus master to determine if an error occurred during the bus cycle.

NOTE

Four bytes (version 2 - eight bytes) are parity checked during each memory read, regardless of the state of HWEN* and HBEN*. This means that, during memory initialization, a group of 4 (or 8) bytes at a time must be initialized (written to) before reading any of them back. Failure to observe this precaution will generate false parity errors.

Row/Column Address Decoder

The row/column address decoder PAL (14C) (version 2 - 16C) inputs system bus addresses A18-A2Ø and generates two 1-of-4 memory block enables; one for the row address strobe and one for the column address strobe. The memory PCB is divided into four blocks of memory that get enabled one at a time depending upon the address. (Version 2 is divided into two half-blocks of memory that get enabled one half-block at a time depending upon the address.)

Input signals HALF and 64KS are jumper selectable to indicate the size of the RAMs installed and whether the PCB is fully or partially populated. The HALF and 64KS signals determine which two of the four address lines will be decoded.

Memory Transceiver Control

The memory transceiver control PAL (11F) (version 2 - 19F and 2ØF) inputs signals AØ, A1, (and A2 for version 2), HBEN (high byte enable), HWEN (high word enable), (HLWEN*, high long word enable, for version 2), and MWT* (memory write) from the system bus. This PAL enables one, two, or four of the data transceivers between the memory array and the system data bus.

Signals AØ and A1, (and A2 and HLWEN* for version 2), HBEN, HWEN, and MWT* control the four (or eight for version 2) write enable signals (WENØ*-WEN3*) (or WENØ*-WEN7* for version 2) to the RAM array. Together, the signals select either 1, 2, or 4 bytes for transfer to/from the system bus.

The byte-swap enable outputs (BSENØ* and BSEN1*) (or BSENØ*-BSEN3* for version 2) enable two (or four for version 2) data transceivers to do byte swapping so that data from bits DØ through D15 on the system data bus is transferred to address MD16 through MD31 (and, depending on A2 and HLWEN*, MD48 through MD63 for version 2) in the memory array.

Memory Arbiter

The memory arbiter PAL (15C) (version 2 - 17C) is a state machine that generates timing signals for the memory PCB. Memory read or write commands from the system bus produce outputs at the row address strobes RAS and RASØ, advanced acknowledge clock ACKCLK, and write transfer acknowledge clock WXACK.

Refresh cycles, identified by input signal RFCY true, generate RAS, RASØ, and RFEN (refresh enable) signals to the memory PCB. Refer to **Timing Diagrams** at the back of this section for detailed timing information.

RAM Refresh

Each memory PCB has its own refresh control logic that ensures that the entire RAM array on each PCB is refreshed about every 4 milliseconds. Refresh is accomplished by simply dividing down the system bus clock (about 1Ø MHz) to a 15 microsecond rate, which ensures that all of the 256 rows within the RAM get refreshed within 4 milliseconds.

Since the refresh timer is free-running, a bus master may request a memory transfer at the same time a refresh cycle is taking place (or is about to take place).

On-board arbitration ensures that the potential conflict between refresh and system-bus-cycle request is properly cued and executed. The arbitration is totally transparent to the requesting bus master, except for the additional wait-states that may occur as a result of waiting for a refresh cycle to complete.

Address Space Allocation

The memory PCB has two jumper connectors designated E1 and E2 located near the top center of the board. Each of these connectors has 10 pins (five positions).

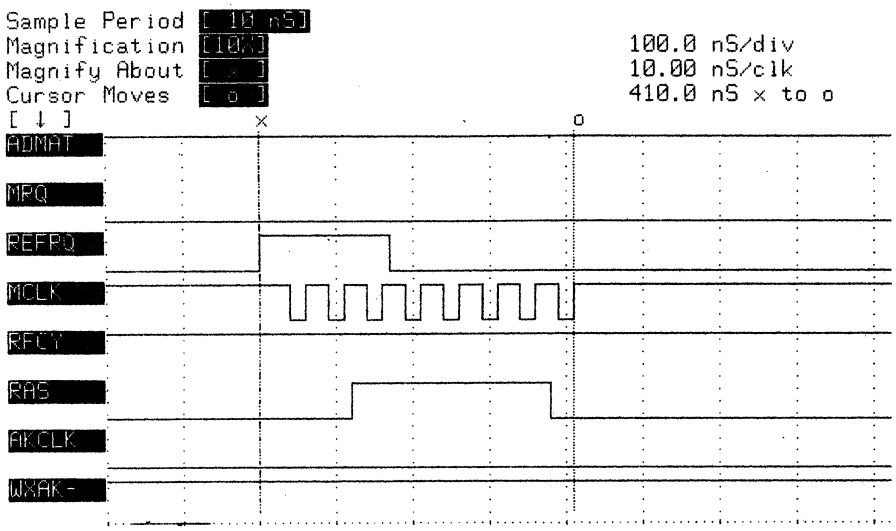
Jumper connector E1 is jumpered according to the type of memory PCB (1M, 2M, or 4M bytes of RAM on the PCB). Jumper connector E2 is jumpered to set the address space that the memory PCB will occupy within the system.

The jumpers are properly installed at the factory for the shipped configuration, and should not need to be changed unless additional memory PCBs are added or the type of memory PCBs are changed in the field.

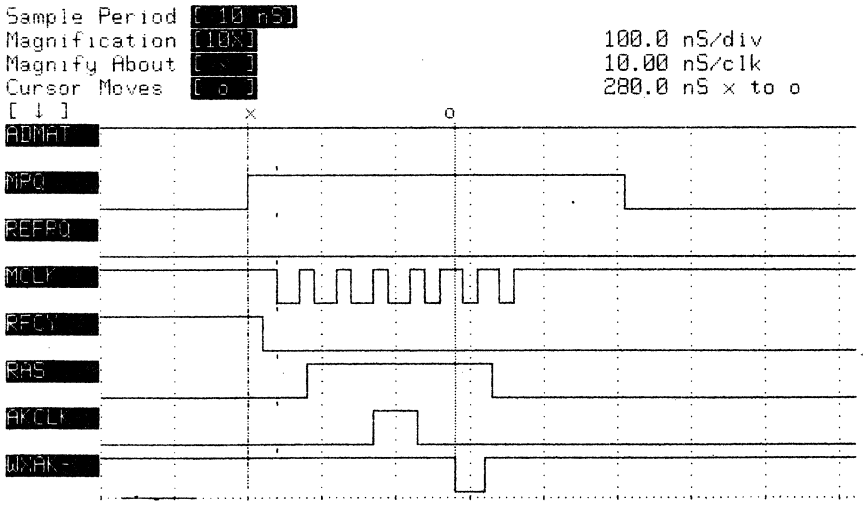
The jumpers should be installed so that: (1) the sum of all the address space available on the memory PCBs present a single, contiguous, memory space to the CPU, and (2) address space is allocated beginning with the memory PCB that has the largest memory capacity and progressing contiguously to the memory PCB with the smallest memory capacity (refer to **Plug-In Printed Circuit Board Locations** in Chapter 1 for the recommended memory PCB locations). Refer to Appendix A for specific jumpering information.

Timing Diagrams

The major memory PCB timing diagrams are shown in Figure 3-5.

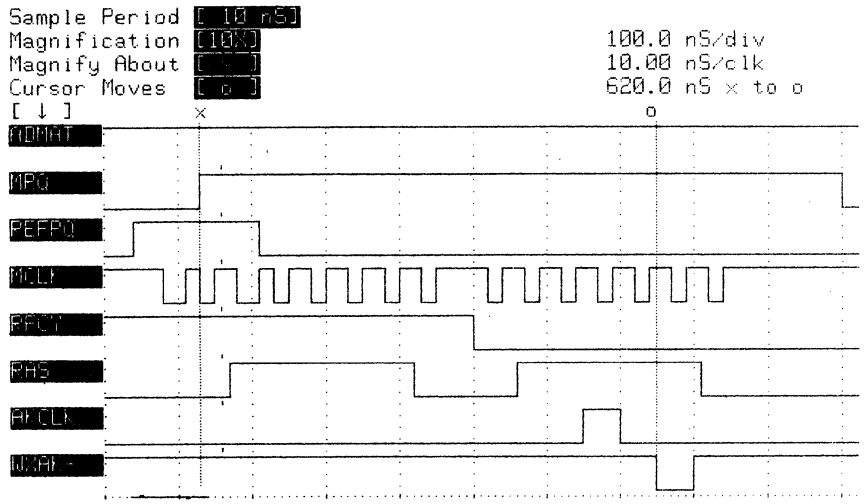


15C (17C)- Memory Arbiter PAL
(Normal Refresh Cycle - No Arbitration)

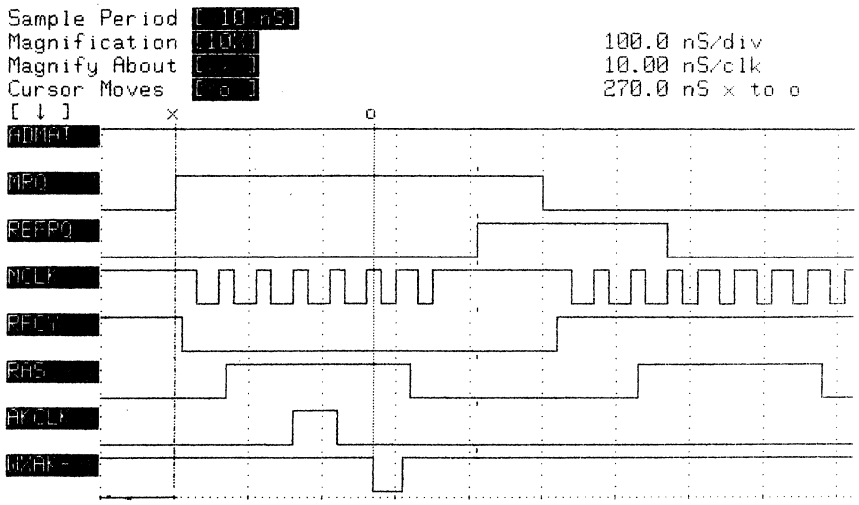


15C (17C) - Memory Arbiter PAL
(Memory Cycle - No Refresh Arbitration)

Figure 3-5. Memory PCB Timing Diagrams



15C (17C) - Memory Arbiter PAL (Memory/Refresh Request Arbitration - Refresh Runs First)



15C (17C) - Memory Arbiter PAL (Memory/Refresh Request Arbitration - Refresh Runs Second)

Figure 3-5. Memory PCB Timing Diagrams (Cont.)

(BLANK)

Communications PCB

The function of the communications (SIO) PCB is to manage all of the serial communications for the 1086/2086 system. Refer to the **Schematic Diagrams** supplement to this manual for the block and schematic diagrams of the communications (SIO) PCB.

I/O Microprocessor

The communications (SIO) PCB uses an Intel 8086 microprocessor (running at 8 MHz) as an input/output processor (IOP) that initializes and maintains all the functions on the communications (SIO) PCB. The IOP performs interrupt processing from the direct memory access (DMA) controller and each serial channel, and I/O buffer management and communication with the rest of the system.

Local Arbiter

The local arbiter resolves contention between the 8086 IOP, dynamic RAM refresh, and DMA controller for the local bus and decodes IOP bus cycles targeted for the system bus. There are three possible conditions which require concurrent management to ensure that only one device gets the local bus at a time:

1. IOP wants access to the local bus.

2. DMA controller wants access to the local bus.

3. Refresh controller wants the local RAM for refresh.

The IOP is permitted to access the system bus at the same time the previous three conditions are taking place (since they are occurring on separate buses). These three conditions must be made mutually exclusive since they each take control of the local bus.

The local arbiter PAL integrated circuit (11C) monitors the refresh and DMA requests, and decodes the IOP bus cycle to determine if the IOP bus cycle is intended for the local or system buses. This PAL establishes the following priorities for the local bus requests:

1. DMA controller.

2. Refresh.

3. Local bus cycles initiated by the IOP.

Refer to **Timing Diagrams** at the back of this section for detailed timing diagrams.

System Bus Interface

The IOP has the capability to become a system bus master and perform memory reads and writes to system memory. Input/output (I/O) reads and writes to any I/O device (addressed lower than 8000h) on the system bus can also be performed which permits the communications PCB to generate channel attention signals. Channel attention signals from the system bus intended for the communications (SIO) PCB generate a maskable, vectored, interrupt to the IOP.

The system bus interface also allows the IOP to access the system bus for communicating with system memory. The 8086 IOP is the ONLY means of communication.

It is NOT possible for any device on the system bus to directly affect the operation of anything on the communications (SIO) PCB, nor is it possible for any other device on this board (such as the local DMA controller) to access the system bus.

IOP access to the system bus is controlled first through the local arbiter PAL (11C) and then via the 8289 system bus arbiter. The 8289 arbiter manages IOP requests for the system bus. The system bus is essentially like the Intel Multibus but with wider data and address paths. Although the system bus is capable of double-word (32-bit) transfers, data transfers to/from the communications (SIO) PCB are restricted to 8 or 16 bits.

Local Bus Controller

The local bus controller PAL (15C) generates the necessary timing for the strobes that are the result of any IOP-generated I/O reads or writes, memory reads or writes, or interrupt acknowledge. This PAL is enabled only when the IOP grant signal (IOPGNT*) is low which gives the IOP access to the local bus.

The local bus controller PAL monitors the IOP latched status lines (LSØ* - LS2*) and provides IO read and IO write strobes for the I/O cycles. The memory cycle (MEMCY*) signal is low for any local memory cycle; memory write (MEMW*) is the status line that signals a read or write to local memory. Data strobe (DS*) is used by other logic to control the data transceiver enables. Refer to **Timing Diagrams** at the back of this section for detailed timing diagrams.

Local Bus Interface

The wait-state generator PAL (1ØC) is only active for IOP-generated local bus cycles. This PAL monitors the IOP latched status lines and various chip select lines to determine the number of wait states for a local bus cycle. The RAM read and write cycles require one wait state; PROM accesses require two wait states; I/O write cycles to the SCCs require one wait state; I/O read cycles to the SCCs require three wait states. The number of wait states for the SCC accesses may be increased by the recovery wait (RWAIT*) signal if a given SCC's recovery time has not elapsed.

Interrupt acknowledge cycles cause two wait states for the interrupt acknowledge 1 (INTA1) signal (allows the interrupt daisy chain to settle) and one wait state for the interrupt acknowledge 2 (INTA2) signal (the cycle that actually reads the interrupt vector from the highest priority device). Refer to **Timing Diagrams** at the back of this section for detailed timing diagrams.

Local Bus Transceiver Controller

The local transceiver controller PAL (14C) performs the following functions:

- monitors which device has control over the local bus (IOP, DMA, and refresh)
- manages the data transceiver enables and directions between the local bus and the IOP
- performs byte swaps between the upper and lower local data bus
- controls write enable and two column address strobe (CAS*) enable signals to the local RAM

Byte swapping occurs only during the bus cycles generated by the DMA controller for those data transfers between an odd memory addresses and an I/O device.

Write enable (WE*) is a status line that is true throughout the entire memory write cycle. The two column address strobe (CAS*) signals enable data to be read or written from even and/or odd memory.

Local Memory

Initial Program Load (IPL) PROM. The communications PCB can support up to 256K bytes of PROM. Upon communications (SIO) PCB (or system) power-up or reset, the IOP begins execution at address FFFFØh (16 bytes from the absolute top of the IOP 1M byte memory space) which is at the top of the PROM. Address FFFFØh contains a jump instruction to the actual location of the initialization code, also within PROM. This code is executed upon system (or PCB) power-up or reset to perform local power-up confidence tests and initialization of the communications (SIO) PCB. Then the PROM attempts to load the actual communications executive program from system memory into local RAM. See Figure 3-6 for the local memory map.

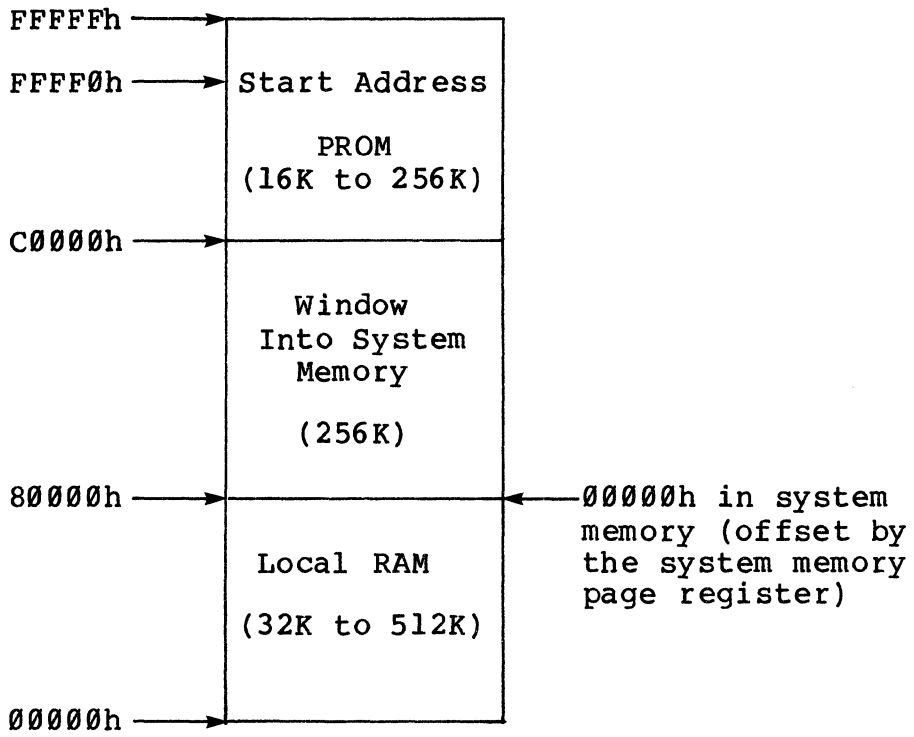


Figure 3-6. Local Memory Map

If the entire system does not power-up, or if any error is detected within the communications (SIO) PCB, a small set of interactive diagnostics are available which may be run from the channel 0 serial port (which the PROM has initialized to 9600 baud). Once the operating system has been loaded, channel 0 will be reconfigured to whatever the system software dictates. The IPL PROM also contains the necessary code to handle memory parity errors. Local and system RAM generate and check parity.

Several PROM sizes are supported, depending upon software requirements. Type 2732, 2764, or 27128 PROMs can all be supported by simply changing a jumper (see **Jumper Selectable Options** in this section for additional jumper information).

Local RAM. The local RAM is used by the IOP for program execution and also as a buffer to support communications and terminal/printer I/O. The basic system contains 32K bytes (16K words) of local RAM comprised of four 16K x 4 bit dynamic RAMs. Optional 64K x 4 bit dynamic RAMs can increase the memory to 512K bytes (256K words).

Byte parity is also present. No error correction is done, nor is there any hardware to log the error address. Parity errors cause an NMI at the IOP. The NMI causes an error-handling routine to take control.

At system initialization, the IOP firmware will attempt to load the actual IOP communications software from system memory into local RAM.

Local Memory Decoder

The local memory decoder PAL (19E) performs the following functions:

- monitors local bus control lines, memory cycle (MEMCY*), memory write (MEMWR*), and the five high order address lines (A15-A19)
- decodes four equal-sized blocks of RAM to provide row address strobe Ø through 3 (RASØ* - RAS3*) signals
- provides a PROM chip select (PROMCS*) signal when accessing PROM

The refresh grant (REFGNT*) signal is also input, which forces all four blocks of RAM to be refreshed. Jumper connector E8 is an input that determines the size of the address space that each block of RAM occupies.

System Memory Page Register

The system memory page register is a 6-bit write-only register which provides address bits A18 through A23 for IOP accesses to system memory as illustrated in Figure 3-7.

Accessing System Memory

To access system memory, the system memory page register determines the position of a 256K byte window into system memory.

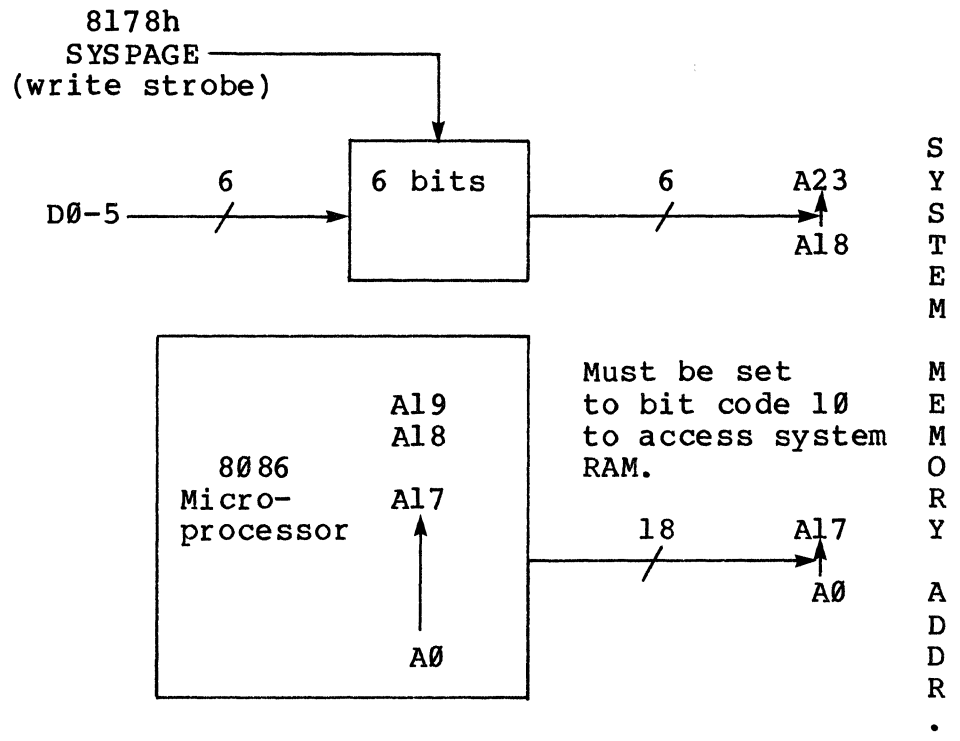


Figure 3-7. System Memory Page Register Block Diagram

For any value of the page register, the IOP can only access system memory within a 256K byte range. To determine the value to be programmed into the page register, use the following formula:

Page register value=
integer portion of (system memory address/256K)

Expressed in binary:

Page register value=
(system memory address) shifted right 18 bits

For example:

System memory address= 80,000h= 1000 0000 , 0000 0000 0000b
shifted right 18 bits= 0000,0010b= 2d

Thus, the page register should be programmed with 2d.

To determine the system memory address, the IOP will access with a given page register value:

System memory address=
(IOP address) - (80,000h) + (page register * 40,000h)
or (IOP address) - (512K) + (page register * 256K)

For example:

Assuming:

1. Page register= 3.

2. IOP addresses memory at 81,000h.

Then system memory will be accessed at address -
(81, 000h - (80,000h) + (3 * 40,000h) =
1,000h + C0,000h = C1,000h

I/O Port Addressing

The I/O port addressing space is allocated as illustrated in Figure 3-8.

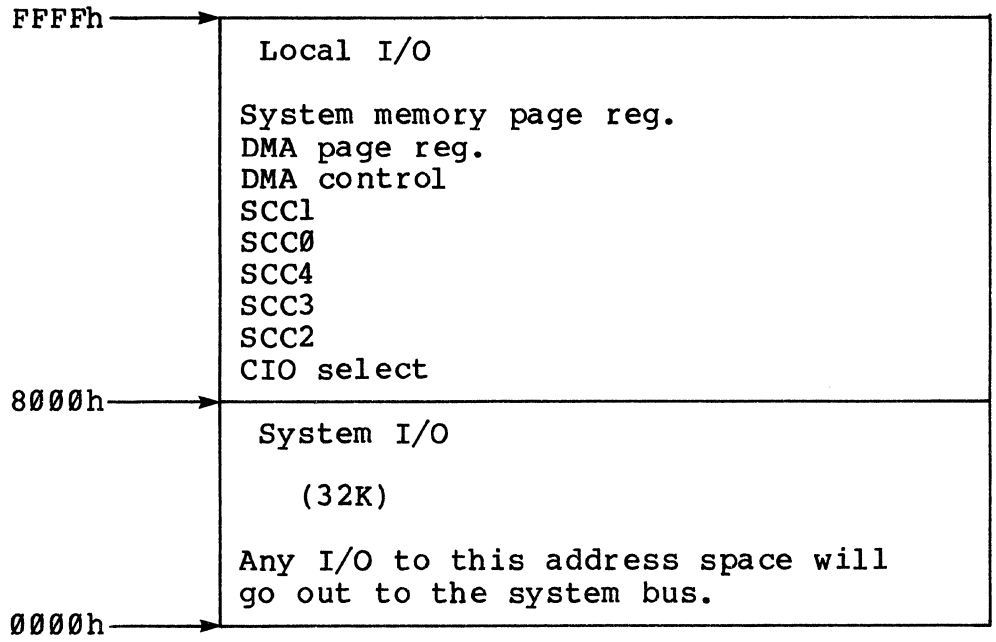


Figure 3-8. Local I/O Map

NOTE

The local I/O space is not fully decoded. Accessing I/O space other than those described in Table 3-8 is not recommended.

Table 3-8. I/O Port Assignments

Port (Hex)	R/W	Description
0000 - 7FFF		System I/O ports
8000 - 80FF		Reserved for future use
		CIO (miscellaneous I/O control bits and counters/timers)
8100	R/W	Port C data register
8101	R/W	Port B data register (used for output flags)

Table 3-8. I/O Port Assignments (Cont.)

Port (Hex)	R/W	Description
81Ø2	R/W	Port A data register (used for input bits)
81Ø3	R/W	Control registers for CIO
81Ø4 - 81ØF		Do not use
		SCC2 (first group of asynchronous ports)
811Ø	R/W	Channel B control register(s)
8111	R/W	Channel B data register (channel 4)
8112	R/W	Channel A control register(s)
8113	R/W	Channel A data register (channel 5)
8114 - 811F		Do not use
		SCC3 (second group of asynchronous ports)
812Ø	R/W	Channel B control register(s)
8121	R/W	Channel B data register (channel 2)
8122	R/W	Channel A control register(s)
8123	R/W	Channel A data register (channel 3)
8124 - 812F		Do not use
		SCC4 - (third group of asynchronous ports)
813Ø	R/W	Channel B control register(s)
8131	R/W	Channel B data register (channel Ø)
8132	R/W	Channel A control register(s)
8133	R/W	Channel A data register (channel 1)

Table 3-8. I/O Port Assignments (Cont.)

Port (Hex)	R/W	Description
8134 - 813F		Do not use
		SCCØ (network and 1st RS-232 ports)
8140	R/W	Channel B control register(s)
8141	R/W	Channel B data register (channel 8 - asynchronous/ sysnchronous channel with half-duplex DMA support)
8142	R/W	Channel A control register(s)
8143	R/W	Channel A data register (network/channel 9)
8144 - 814F		Do not use
		SCC1 (synchronous and asynchronous ports)
8150	R/W	Channel B control register(s)
8151	R/W	Channel B data register (channel 6)
8152	R/W	Channel A control register(s)
8153	R/W	Channel A data register (channel 7 - asynchronous/ synchronous channel with full-duplex DMA support)
8054 - 805F		Do not use
		DMA (DMA controller)
8160		Channel Ø - Used for network channel (SCCØ-A):
	W	Base and current address
	R	Current address
8161	W	Base and current word count
	R	Current word count

Table 3-8. I/O Port Assignments (Cont.)

Port (Hex)	R/W	Description
		DMA (DMA controller) (Cont.)
8162		Channel 1 - Used for half-duplex synchronous channel (SCCØ-B):
	W	Base and current address
	R	Current address
8163	W	Base and current word count
	R	Current word count
8164		Channel 2 - Used for receive side of full-duplex synchronous channel (SCCl-A):
	W	Base and current address
	R	Current address
8165	W	Base and current word count
	R	Current word count
8166		Channel 3 - Used for transmit side of full-duplex channel (SCCl-A):
	W	Base and current address
	R	Current address
8167	W	Base and current word count
	R	Current word count
8168		DMA Status Registers:
	W	Command register
	R	Status register
8169	W	Request register
816A	W	Single mask register bit
816B	W	Mode register
816C	W	Clear byte pointer flip flop
816D	W	Master clear
	R	Temporary register
816E	W	Clear mask register
816F	W	Write all mask register bits

Table 3-8. I/O Port Assignments (Cont.)

Port (Hex)	R/W	Description
		Miscellaneous Registers
817Ø - 8177		Not used
8178	W	System memory page register (provides memory addresses A18-A23 during access to system memory). See **System Memory Page Register** in this section
8179	W	DMA memory page register (provides memory addresses A16-A19 during DMA to system memory). See **DMA Page Register** in this section
817A - 817F		Reserved for future use
818Ø - FFFF		Do not use

DMA Controller

The DMA controller is a four-channel device capable of simultaneously managing DMA to/from four separate I/O sources through serial communications controllers (SCCs) as follows:

- high-speed network on channel A of SCCØ
- RS-232 serial port on channel B of SCCØ
- receive side of the synchronous channel on SCC1-A
- transmit side of the synchronous channel on SCC1-A

The local bus and its arbiter are designed so that data transfers on the local bus (between I/O devices and memory that are controlled by the DMA controller) and data transfers on the system bus (initiated by the IOP) can occur simultaneously.

This capability is necessary since the IOP may experience significant delays (on the order of milliseconds) before gaining access to the system bus. Thus, DMA transfers on the local bus (as the result of network data or synchronous communications) can continue uninterrupted. To conserve local bus bandwidth and latency, a hidden refresh is performed at the beginning of each DMA cycle. This does not delay any DMA transfer because hiding the refresh within the DMA cycle reduces the likelyhood of IOP-refresh contention. Because of the hardware implementation, the following must be observed:

1. The back of the **Advanced Micro Devices 9517 Technical Data Sheet** lists a number of common problems, some of which can be caused by improper software management of the DMA controller. Read the list!

2. The DMA controller operates in the fly-by mode, which means that data is transferred from the peripheral to memory in the same cycle. Thus, it is not possible to do a DMA transfer to just any I/O device. The only devices supported are serial communications controllers SCCØ-A, SCCØ- B, and SCCl-A as follows:

   - DMA Channel Ø: SCCØ-A, the network
   - DMA Channel 1: SCCØ-B, RS-232 channel 8
   - DMA Channel 2: SCCl-A, the receive side of the synchronous port
   - DMA Channel 3: SCCl-A, the transmit side of the synchronous port

3. Because of restrictions in the hardware implementation, it is not possible to perform memory-to-memory transfers.

4. Because of the time-critical nature of the high-speed network channel, it is recommended that fixed-priority mode be used.

5. The DMA controller should be programmed for the single-cycle transfer mode which transfers only

one byte per DMA bus cycle. (Block-transfer mode should NOT be used, since it would totally tie up the local bus during the time the block was being transferred.)

6. All DMA request (DREQ) inputs from the I/O devices are active low. The DMA controller must be programmed to accept this polarity.

7. All DMA acknowledge (DMAK) outputs to the I/O devices must be programmed active low.

8. Use normal cycle timing and late write timing.

9. There is no automatic power-up reset to the DMA controller IC. Software is responsible for generating a DMA reset using the control output bit from the counter/input/output (CIO) to reset the DMA controller at power-up and/or initialization.

DMA Synch/Refresh Controller

The DMA synch/refresh controller PAL (15D) synchronizes the DMA grant (DMAGNT*) signal, the DMA ready line, and the DMA hold request (HRQ) line. This PAL also generates one wait state for most I/O cycles (or more if SCC recovery is necessary when RWAIT* is low).

Refresh requests that occur because of a 15 microsecond timer are latched and presented to the local bus arbiter. The beginning of every DMA cycle also generates a refresh request and resets the 15 microsecond refresh timer to allow a hidden refresh cycle to be executed.

Refer to **Timing Diagrams** at the back of this section for detailed timing diagrams.

DMA Read/Write Controller

The DMA read/write controller PAL (16C) synchronizes the DMA controller I/O read (IORD*), I/O write (IOWR*), memory read (MRD*), and memory write (MWR*) command lines to the 8 MHz system clock.

This PAL also generates bus control signals similar to those generated by the local bus controller PAL.

Refer to **Timing Diagrams** at the back of this section for detailed timing diagrams.

DMA Page Register

The DMA page register is a four-bit write-only register which provides address bits A16 through A19 during DMA accesses to local memory as illustrated in Figure 3-9. Since the DMA controller only generates 16 bits of address, the DMA page register removes the 64K byte address space restriction and allows the DMA controller to access local memory in 64K byte pages that start on any 64K byte boundary. There is only one page register that functions identically for all four DMA channels.

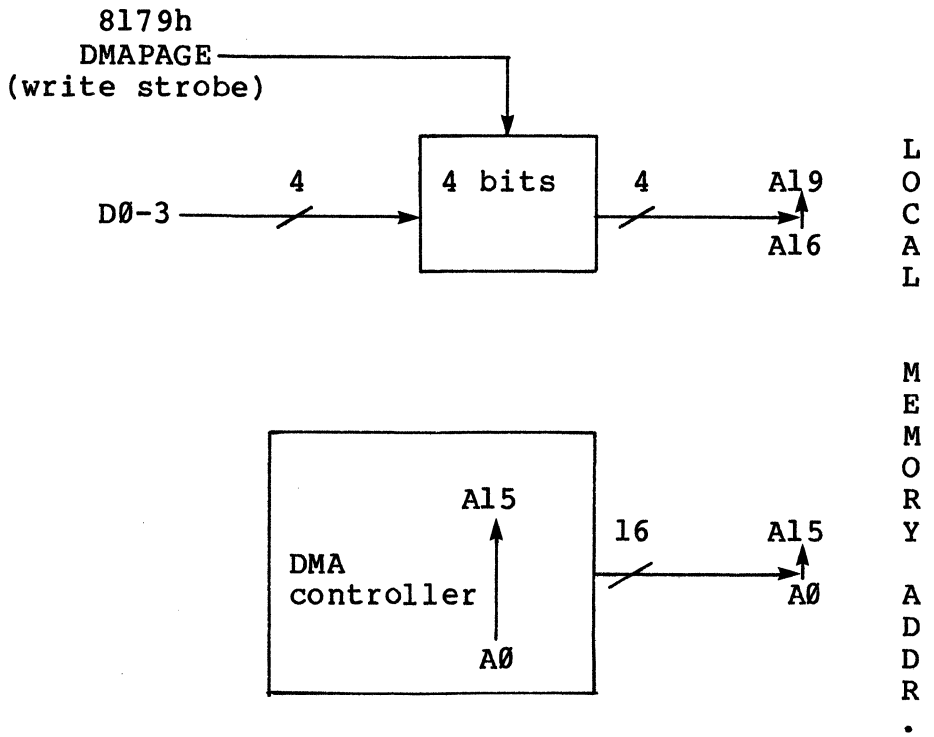


Figure 3-9. DMA Page Register Block Diagram

Serial I/O Ports

There are a total of 10 serial I/O ports on the communications (SIO) PCB that are supported by five 8530 SCCs. The 8530 serial communications controllers are capable of both synchronous and asynchronous support, although this design only provides enough RS-232 line drivers and receivers to support two synchronous channels.

Each of the controllers has two complete communication channels, including independently programmable baud-rate generators for each channel. Each controller is also capable of generating vectored interrupts to the IOP. Refer to the **Zilog Data Handbook/ Technical Manual** for detailed information on the SCCs. The controllers are referenced as described in Table 3-9.

Table 3-9. Communications Controller References

Channel	IC	Capability
0	SCC4-B	Asynchronous RS-232 (boot channel)
1	SCC4-A	Asynchronous RS-232
2	SCC3-B	Asynchronous RS-232
3	SCC3-A	Asynchronous RS-232
4	SCC2-B	Asynchronous RS-232
5	SCC2-A	Asynchronous RS-232
6	SCC1-B	Asynchronous RS-232
7	SCC1-A	Synchronous or asynchronous RS-232 (full duplex DMA)
8	SCC0-B	Synchronous or asynchronous RS-232
9	SCC0-A	Asynchronous RS-232 or high-speed network RS-422

Each port has the following capabilities:

- interrupt driven
- baud-rate programmable from 75 to 19,200 baud (other baud rates possible, if desired):

19,200	2,400	600	134.5
9,600	2,000	300	110
4,800	1,200	150	75

- selectable number of stop bits: 1, 1-1/2, or 2
- selectable number of bits/character: 5, 6, 7, or 8
- TxD input (transmitted data)
- RxD output (received data)
- DTR input (e.g., device busy)
- DSR output (input buffer full)

NOTE

CTS, RTS and DCD are NOT supported on channels 0 through 6 or 9.

The synchronous ports support all of the above, plus:

- RxC input (synchronous receive clock)
- TxC input (synchronous transmit clock)
- RTS input (request to send)
- CTS output (clear to send)

Channel 7 (SCC1-A) has the ability to be full-duplex DMA driven. Channel 9 can be run at 1.4M baud (half-duplex mode only) supported by the highest-priority channel of the DMA controller.

It is possible to have all four DMA channels (channel Ø through 3) running simultaneously. For example:

1. 1.4M baud on SCCØ-A.

2. Up to 19,2ØØ baud RS-232 (half duplex) on SCCØ-B.

3. 96ØØ baud (full duplex) on SCCl-A.

The asynchronous RS-232 I/O ports are implemented with the data terminal ready (DTR) and full data set ready (DSR) handshake lines as described in Table 3-1Ø. Input and output (I/O) are referenced to the communications (SIO) PCB.

Table 3-1Ø. Asynchronous-Channel Handshake Lines

RS-232 Signal	I/O	SCC IC Signal Name
Transmitted Data	I	RxD (receive data)
Received Data	O	TxD (transmit data)
Data Terminal Ready	I	CTS (clear to send)
Data Set Ready	O	RTS (request to send)
Signal Ground		

The serial communications controller CTS and RTS (instead of DCD and DTR) signals are used as the handshaking lines for two reasons:

1. Although it is desirable to make all serial channels consistent in their use of control signals, DTR is used for the second DMA request line for the receive side of SCCl-A. This eliminates the possibility of using DTR to control the RS-232 DSR line.

2. Using the CTS and RTS lines permits the software to take advantage of the auto-enables feature of the SCC.

Handshaking is the same for the synchronous channels with the addition of several more signals as described in Table 3-11. Input and output (I/O) are referenced to the communications (SIO) PCB.

Table 3-11. Synchronous-Channel Handshake Lines

RS-232 Signal	I/O	SCC IC Signal Name
Transmitted Data	I	RxD (receive data)
Received Data	O	TxD (transmit data)
Data Terminal Ready	I	CTS (clear to send)
Data Set Ready	O	RTS (request to send)
Sync Rx Clock	I	RTxC (external receiver clock)
Sync Tx Clock	I	TRxC (external transmitter clock)
Request To Send	I	DCD (data carrier detect)
Clear To Send	O	Provided by the CIO
Signal Ground		

Network Channel

Channel 9 (which uses SCCØ-A) works the same as any other asynchronous channel when the RS-422 control flag in the CIO is cleared. Whenever the RS-422 flag is set, the RS-232 line receiver is disabled and the RS-422 line receiver for RxD of that channel is enabled.

In addition, software selects the external transmit and receive clocks to the SCC as the baud-rate source, and sets the network clock enable (NETCLKEN*) bit (from the CIO) low to enable the 1.4 MHz oscillator, which is used as the transmit clock source.

The SCC's DTR output requests that the network data and clock line drivers be enabled. When the SCC DTR bit is high (DTR* pin is low) and the carrier sense circuit (a 5 microsecond timer) has determined that there is no carrier presently on the network, the drivers are automatically enabled (regardless of the state of the RS-422 flag from the CIO). Therefore, software ensures that the SCC's DTR bit is low, except during network transmit.

When the network channel line drivers are driving the network, the DCD* input will go high (DCD bit in the register will go to Ø). Software uses this bit to determine when it has gained access to the network.

Setting the DTR bit in the register low will cause the line drivers to disable immediately, which will also cause the DCD* pin to go low and possibly generate an interrupt if external/status interrupts were enabled.

No attempt is made to hardware-disable the RS-232 DTR, DSR, and received data lines (CTS, RTS, and TxD at the SCC). The network port must NOT be plugged into an RS-232 and RS-422 device at the same time.

SCC Recovery

The SCC recovery PAL (3C) monitors the I/O accesses to SCCØ and SCC1 that occur because of IOP or DMA cycles. This PAL ensures that successive accesses to a given SCC do not violate the SCC recovery requirement of 1.3 microseconds.

After each valid SCC access, a counter is reset. A later access to the same SCC is prohibited by this PAL until the SCC's associated counter has counted for 1.3 microseconds. Refer to **Timing Diagrams** at the back of this section for detailed timing diagrams.

Programming Precautions

The following precautions must be considered when programming the communications (SIO) PCB:

1. The SCCs and CIO have a recovery requirement which means that successive selects to a given IC must not occur within 1.25 microseconds of each other (this does not apply to interrupt acknowledge). To meet this requirement, hard ware has been added to SCCØ and SCC1 (only) to prevent violating the recovery specification because conditions can arise (especially with DMA) that software cannot guard against.

   However, for the remaining SCCs and the CIO, it is the responsibility of software to insure the recovery specification is met. Thus, it is NOT possible to do the following since it would violate the recovery specification:

```
MOV:  DX,<portnum>              ;Setup port no.
OUT   AL,DX  or  IN   AL,DX ;Do I/O
OUT   AL,DX  or  IN   AL,DX ;  twice

MOV:  DX,<portnum>
OUT   AL,DX
NOP                ; This may not work either!
NOP
OUT   AL,DX
```

This will work properly:

```
MOV:  DX,<portnum>
OUT   AL,DX
PUSH  AX      ; Make sure there is a bus cycle
POP   AX      ; between the output
OUT   AL,DX   ; instructions
```

2. All I/O ICs are on the local D0-7 data bus. Unlike normal 8086 microprocessor convention, A0 DOES participate in the port selection process. (Normally all I/O would be done to all even or all odd addresses.)

Byte-swap logic on the communications (SIO) PCB takes care of this transparently. MINOR SOFTWARE PRECAUTION: any I/O reads or writes must be BYTE operations using AL. For example:

```
MOV:   DX,<portnum> ;Setup port number
OUT    AL,DX    ;Send out data
```

The following will produce unpredictable results:

```
MOV:   DX,<portnum>
OUT    AX,DX    ; A 16-bit data transfer
```

So will this:

```
MOV:   DX,<portnum>
OUT    AH,DX   ;Output the high byte only
```

3. Although it is documented in the **Zilog SCC Technical Manual**, be sure to leave the internal byte pointers in such a state that the ICs internal interrupt logic is not left disabled.

4. Do not use the published baud-rate generator divisors. Those numbers apply only when a 4 MHz clock is being used. You must recalculate all divisors based upon a 6 MHz clock. (This will produce a 2.4% error at 19,200 baud.)

Counter/Input/Output

The 8536 CIO is used for general-purpose counter(s)/timer(s) and also provides bit set/test functions. The CIO acts as an interrupt controller for miscellaneous inputs, such as, system channel attention, RAM parity error flags (one for local RAM, one for system RAM), system bus timeout error, DMA end-of-process interrupt, and three general-purpose inputs (jumper selectable) for software-determined use. One of the general-purpose inputs is used to identify the PCB that contains the boot channel for computer systems that have more than one communications (SIO) PCB. Refer to Table 3-12 for CIO port descriptions.

There are three internal counter/timers that can generate vectored interrupts. Two of these are unimplemented and are reserved for any uses that software may determine (implementing timeouts, etc.).

These counter/timers are only accessible through software and can be used individually or cascaded.

The third counter/timer is accessible on I/O signal lines PC0-PC3 (currently undefined, but reserved for future use by hardware). Refer to the **Zilog Technical Reference Manual** for detailed information on the 8536 CIO operation.

Table 3-12. CIO Port Descriptions

Bit	Signal Name	Pulse/ Level	Description
			Port A (inputs)
PAØ	BTIMEOUT*	pulse	A system bus timeout error has occurred
PA1	CHANATTN*	pulse	Channel attention from system bus
PA2	DMAEOP*	pulse	DMA end-of-process interrupt
PA3	LOCPERR*	pulse	A parity error has occurred in local RAM
PA4	SYSERR*	pulse	Either a system RAM parity error or a system bus timeout error has occurred while accessing the system bus
PA5	LOOPERR*	level	Jumper installed between pins 3 and 4 of connector E1 (logic Ø) indicates that the IPL PROM firmware should enter a stand-alone mode
PA6	PRIMARY*	level	Jumper installed between pins 1 and 2 of connector E1 (logic Ø) indicates that this is the master (Ø) communications (SIO) PCB
PA7	-------	level	Not used

Table 3-12. CIO Port Descriptions (Cont.)

Bit	Signal Name	Pulse/ Level	Description
			Port B (outputs)
PBØ	NMICLR	level	A logic 1 will clear the parity error NMI. Must be set to Ø to allow more parity errors (and NMI) to be detected
PB1	SYSINT	Ø-1-Ø	Causes a system bus interrupt to be generated. Software must drive this line to logic Ø to 1 to Ø
PB2	DMARESET	Ø-1-Ø	Causes a hardware reset of the DMA controller. Software must drive this line from logic Ø to 1 to Ø
PB3	RS422A	level	A logic 1 causes SCCØ-A to disable the RS-232 RxD receiver and enable the RS-422 RxD receiver
PB4	NETCLKEN*	level	A logic Ø enables the 1.4 MHz oscillator for the network transmit clock
PB5	CSTA*	level	A logic Ø asserts the RS-232 CTS output for the SCC1-A channel.
PB6	CSTB*	level	A logic Ø asserts the RS-232 CTS output for the SCCØ-B channel.
PB7	REDLED	level	A logic 1 turns on the red LED.

Table 3-12. CIO Port Descriptions (Cont.)

Bit	Signal Name	Pulse/ Level	Description
			Port C (I/O or counter/timer)
PCØ-PC3			(reserved for future use)

CIO Programming Notes

PAØ - BTIMEOUT*

This CIO input must be programmed to "catch" a 1-to-Ø-going pulse, and generate a vectored interrupt. If true, it indicates that an attempt was made to access some device (memory or I/O) on the system bus that did not respond within 1ØØ milliseconds. This condition may be caused by attempting to access a nonexistent device/PCB or attempting to access a nonfunctional device/PCB.

Normally this error should not occur since the CPU PCB also monitors excessively long bus transactions and asserts the bus error signal after about 1Ø microseconds.

PA1 - CHANATTN*

This CIO input must be programmed to catch a 1-to-Ø-going pulse and generate a vectored interrupt. If true, it indicates that some device on the system bus has generated a channel attention signal intended for the communications (SIO) PCB. (Multiple communications (SIO) PCBs in the system each have their own unique channel attention signal.)

PA2 - DMAEOP*

This CIO input must be programmed to catch a 1-to-Ø-going pulse and generate a vectored interrupt. If true, it indicates that the end-of-process (EOP) signal from the DMA controller has gone true.

Since there is only one EOP output from the DMA controller, software must further test the condition of the DMA status registers to determine which DMA channel caused the interrupt.

PA3 - LOCPERR*

This CIO input must be programmed to catch a 1-to-Ø-going pulse and should not generate a vectored interrupt. When this signal is true, it indicates that a parity error has been detected while accessing local RAM and an NMI has been generated to the 8Ø86 microprocessor.

The CIO input should be used only as a status bit to determine the source of the NMI. Once the source of the NMI is determined, the NMICLR signal must be driven false to clear the NMI latch.

PA4 - SYSERR*

This CIO input must be programmed to catch a 1-to-Ø-going pulse. It should not generate a vectored interrupt since SYSERR* also generates an NMI to the 8Ø86 microprocessor. If this signal is true, it indicates that a bus error has occurred while attempting to access the system bus. A bus error can occur:

1. If a system memory parity error is detected while accessing system memory.

2. The host CPU has determined that a system bus timeout has occurred (the bus transaction has not been acknowledged within about 1Ø microseconds).

This input should be used only as a status bit to determine the source of the NMI. Once the source of

the NMI is determined, the NMICLR signal must be driven true, then false to clear the NMI latch.

PA5 and PA6 (General-Purpose Inputs)

These CIO inputs are simple status inputs which sense the state of a three-position jumper connector.

These inputs may be used for any use software may dictate. Input PA5 is used during power-up initialization for hardware debug to indicate that the firmware should should enter a stand-alone mode. Input PA6 is used to indicate the master (Ø) communications (SIO) PCB in the system.

Interrupt Priorities

Interrupt priorities are organized in a daisy-chain as described in Table 3-13.

Table 3-13. Interrupt Daisy Chain

Priority (Highest-Lowest)	IC	Description
1	CIO	Counter/timer 3 Port Port A (inputs) Counter/timer 2 Port B (outputs) Counter/timer 1
2	SCCØ	Channel A (the network channel, or RS-232 channel 9) Rx Tx External/status Channel B (the half-duplex DMA-driven synchronous channel) - (channel 8)

Table 3-13. Interrupt Daisy Chain, (Cont.)

Priority (Highest-Lowest)	IC	Description
3	SCC1	Channel A (the full-duplex DMA-driven synchronous channel) - (channel 7) Channel B - (channel 6)
4	SCC2	Channel A (channel 5) Channel B (channel 4)
5	SCC3	Channel A (channel 3) Channel B (channel 2)
6	SCC4	Channel A (channel 1) Channel B (channel Ø - boot channel)

Each of the ICs listed in Table 3-13 can be programmed to interrupt with an eight-bit vector unique to that IC. All of the ICs in Table 3-13 have a status-affects-vector capability which allows the specific cause of the interrupt to participate in generating a unique vector. Refer to the **Zilog and Advanced Micro Devices** data books and technical manuals for specific capabilities.

The 8Ø86 microprocessor allows up to 256 unique interrupt vectors. The use of certain vectors has been predefined by the microprocessor as follows:

Vector	Use
Ø	Divide by zero error
1	Single-step interrupt
2	Nonmaskable interrupt
3	One-byte interrupt instruction
4	Overflow

Intel further reserves a block of 27 interrupt vectors (5 through 31d) for its use. The remaining vectors are available for any use software may dictate. Vector 255

(ØFFh) is reserved as a general-purpose hardware error trap, since a hardware failure in the interrupt vector-generating mechanism generally causes this vector.

Jumper Selectable Options

Table 3-14 describes the jumper selectable options for the communications (SIO) PCB. Refer to Appendix A for specific jumpering information.

Table 3-14. Jumper Descriptions

Connector Designation	Description
E1	General-purpose input port. Jumpered only on the master (Ø) communications PCB. Not jumpered on any other communications PCBs installed in the 1Ø86/2Ø86 system.
E2	Selects the size of PROMs installed (2732, 2764, or 27128). 2764 PROMs are normally installed.
E3	AACK. Enables the advanced acknowledge (AACK) signal from the system memory (reduces wait states). Also used for local reset (testing only). Normally jumpered for enabling AACK.
E4	BPRN (Bus Priority Input). Used to determine the arbitration priority when the communications (SIO) PCB(s) wish to access the system bus.
E5	BPRO (Bus Priority Output). See BPRN.
E6	CHANATTN. Selects the port number that the communications (SIO) PCB responds to for channel attention signals generated on the system bus.

Table 3-14. Jumper Descriptions (Cont.)

Connector Designation	Description
E7	INT. Selects the bus interrupt vector level that the communications (SIO) PCB generates.
E8	LARGE*. Must be jumpered if 256K dynamic RAMs are installed.

I/O Connectors

The communications (SIO) PCB has 10 rear-panel serial I/O connectors (port 0 through 9) supported by five serial communications controller (SCC) ICs.

All channels use a 9-pin, D-type, subminiature connector (DE-9P male plug). Table 3-15 describes the connector/controller configuration.

Table 3-15. Connector/Controller Configuration

Connector Designation	Serial Channel	Description
P10	0	Asynchronous RS-232 (Boot Channel)
P11	1	Asynchronous RS-232
P12	2	Asynchronous RS-232
P13	3	Asynchronous RS-232
P14	4	Asynchronous RS-232
P15	5	Asynchronous RS-232
P16	6	Asynchronous RS-232
P17	7	Synchronous or Asynchronous RS-232 (with full-duplex DMA support)
P18	8	Synchronous or Asynchronous RS-232
P19	9	Asynchronous RS-232 or High-Speed Network RS-422

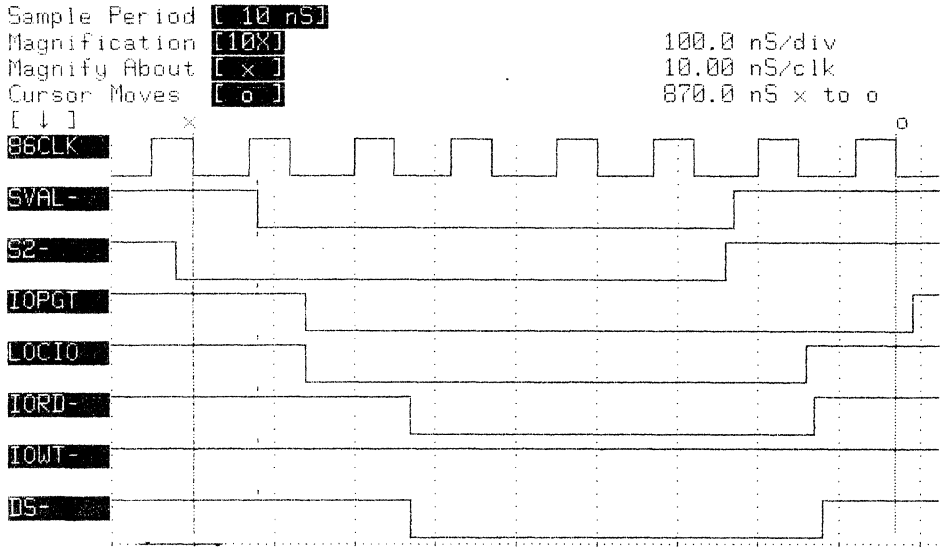
Depending upon how the channel is configured, the connector pins have slightly different functions as described in Table 3-16. I (input) and O (output) are referenced to the communications (SIO) PCB.

Table 3-16. Connector Pin Assignments

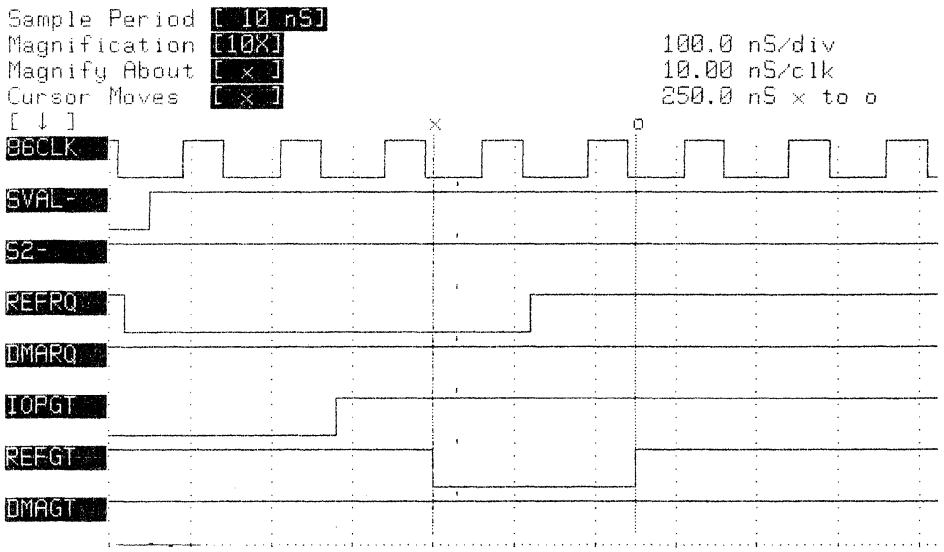
Pin	I/O	Signal Name
		P1Ø Through P16-Asynchronous Channel
1		(Do Not Use)
2	I	Transmitted Data
3	O	Received Data
4	O	Data Set Ready
5	--	Signal Ground
6	I	Data Terminal Ready
7	O	Pullup to +12V
8		Not Used
9		Not Used
		P17 or P18-Synchronous Channel
1	I	Synchronous Receive Clock
2	I	Transmitted Data
3	O	Received Data
4	O	Data Set Ready
5	--	Signal Ground
6	I	Data Terminal Ready
7	O	Clear to Send
8	I	Request to Send
9	I	Synchronous Transmit Clock
		P19-Network Channel
1	I/O	ANET Clock +
2	I	RS-232 Transmitted Data
3	O	RS-232 Received Data
4	O	RS-232 Data Set Ready
5	--	Signal Ground
6	I	RS-232 Data Terminal Ready
7	I/O	ANET Data +
8	I/O	ANET Data -
9	I/O	ANET Clock -

Timing Diagrams

The major communications PCB timing diagrams are shown in Figure 3-10.

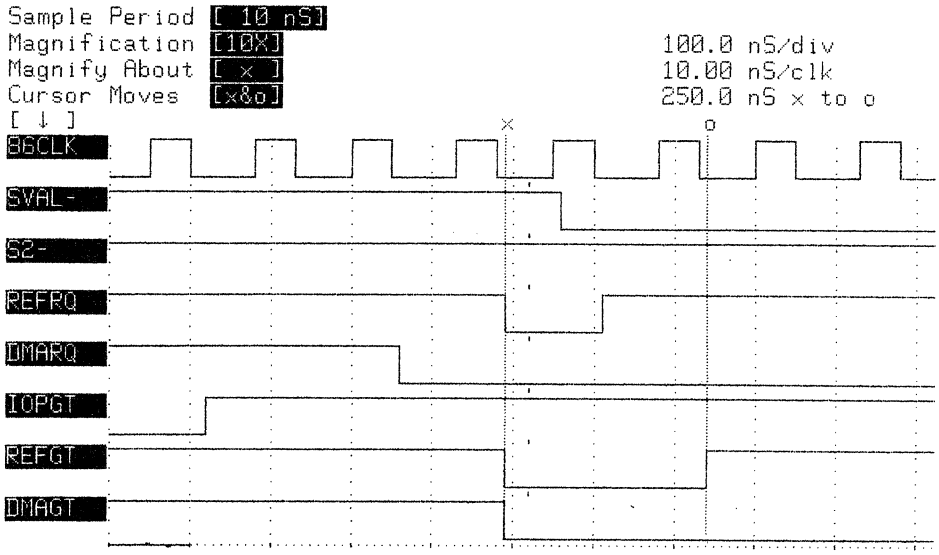


11C - Local Arbiter PAL
(Local Bus Cycle - I/O Read)

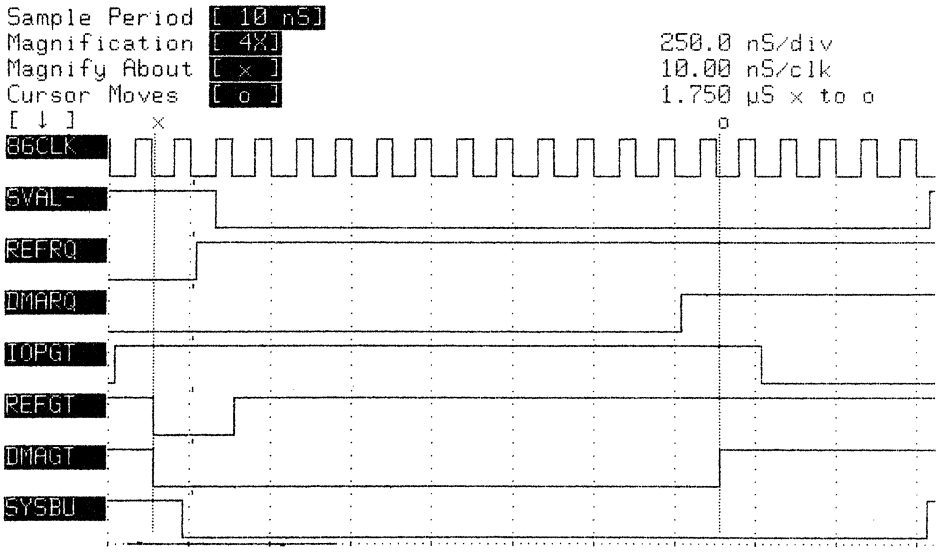


11C - Local Arbiter PAL
(Refresh Grant After IOP Cycle)

Figure 3-10. Communications PCB Timing Diagrams

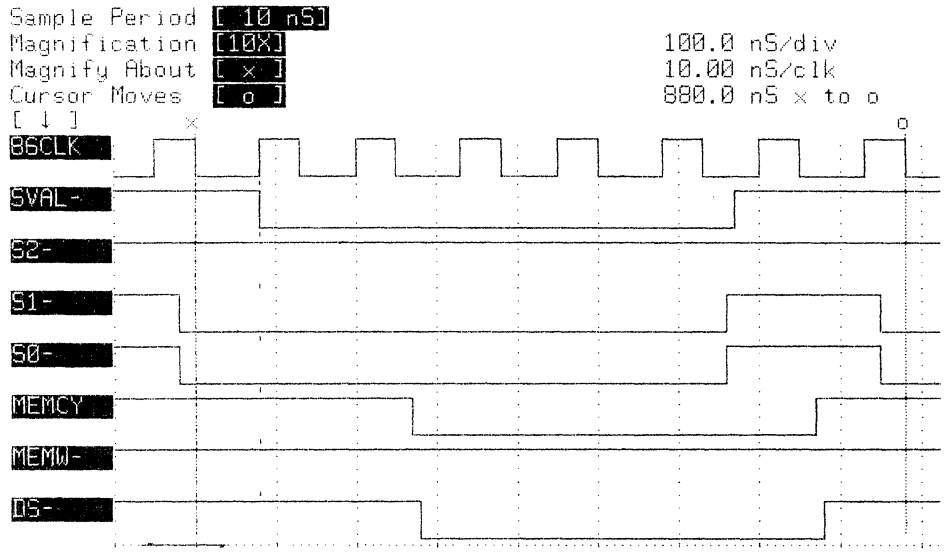


11C - Local Arbiter PAL
(DMA-Induced - Refresh Cycle)

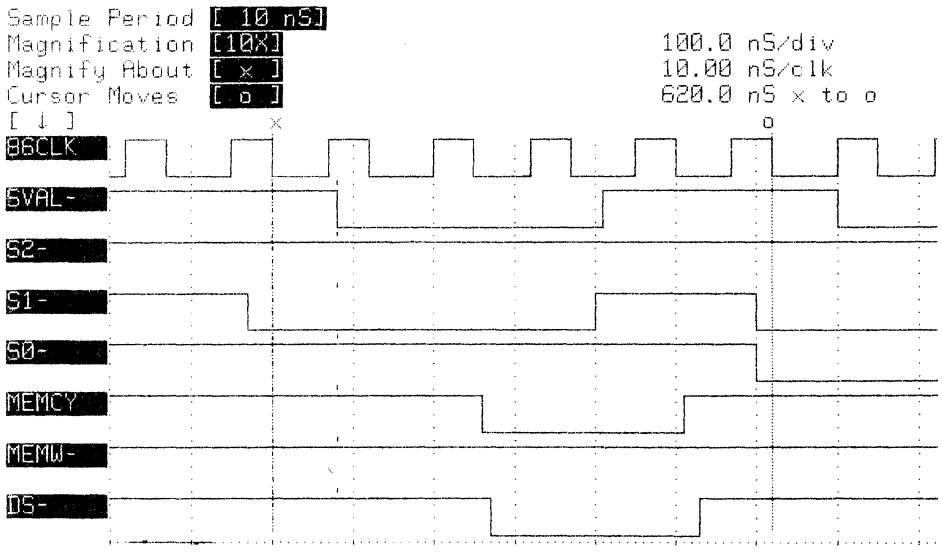


11C - LOCAL ARBITER PAL
(Simultaneous DMA, Refresh, and System Bus Cycle)

Figure 3-10. Communications PCB Timing Diagrams (Cont.)

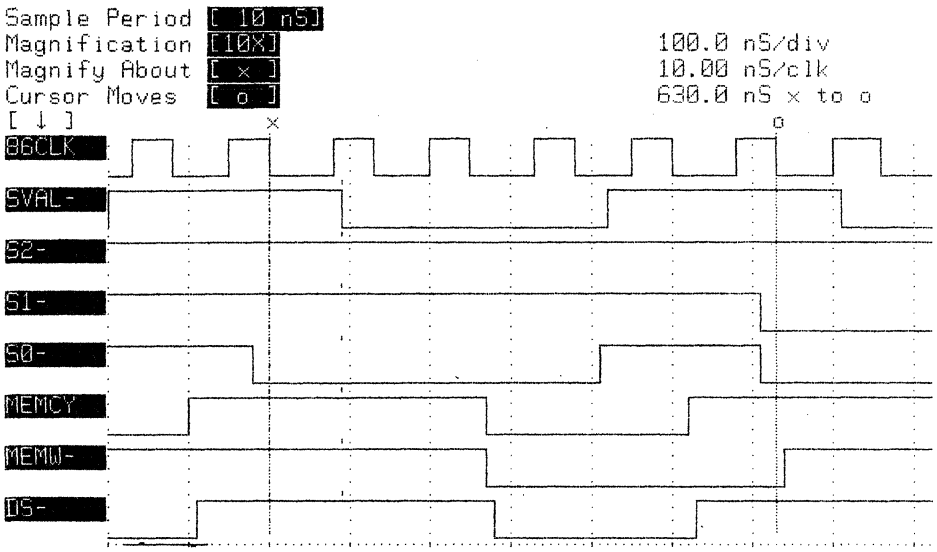


15C - Local Bus Controller PAL (PROM - Read)

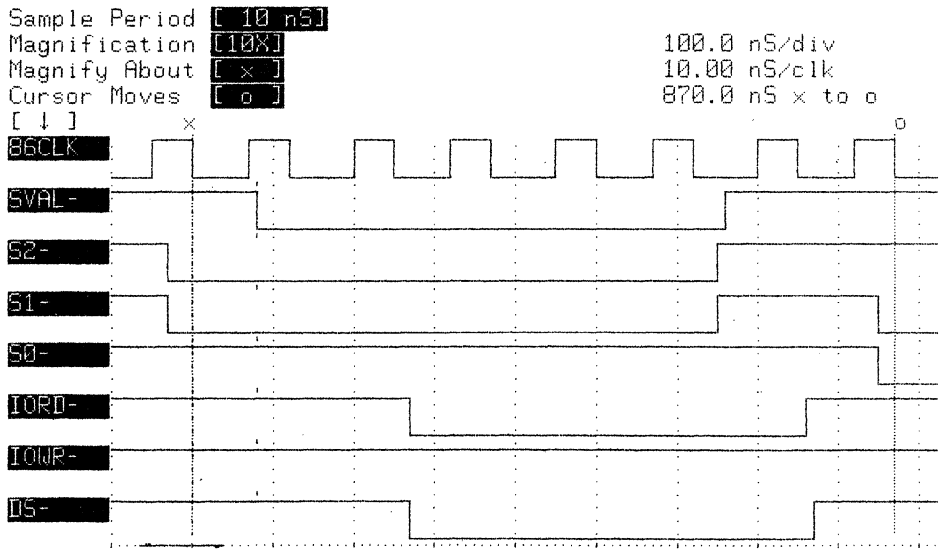


15C - Local Bus Controller PAL (Local RAM - Read)

Figure 3-10. Communications PCB Timing Diagrams (Cont.)

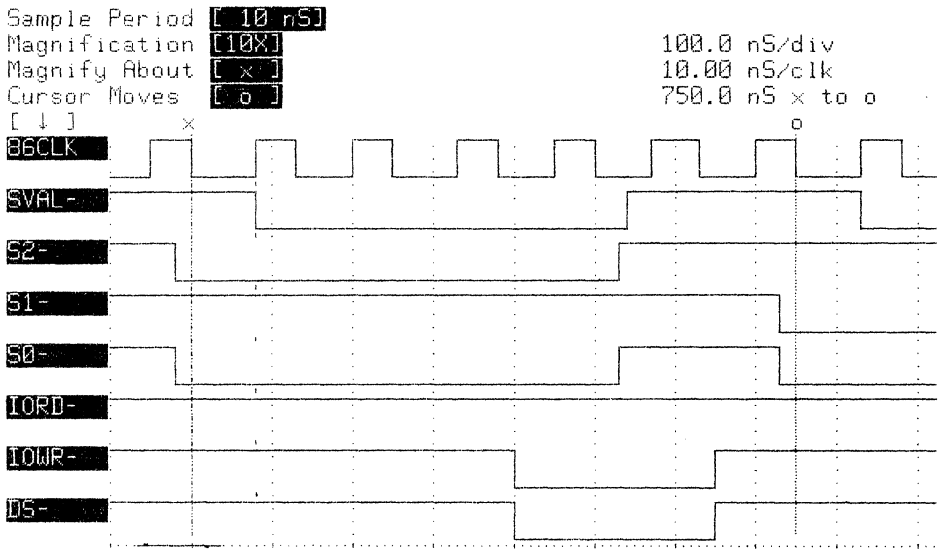


15C - Local Bus Controller PAL
(Local RAM - Write)

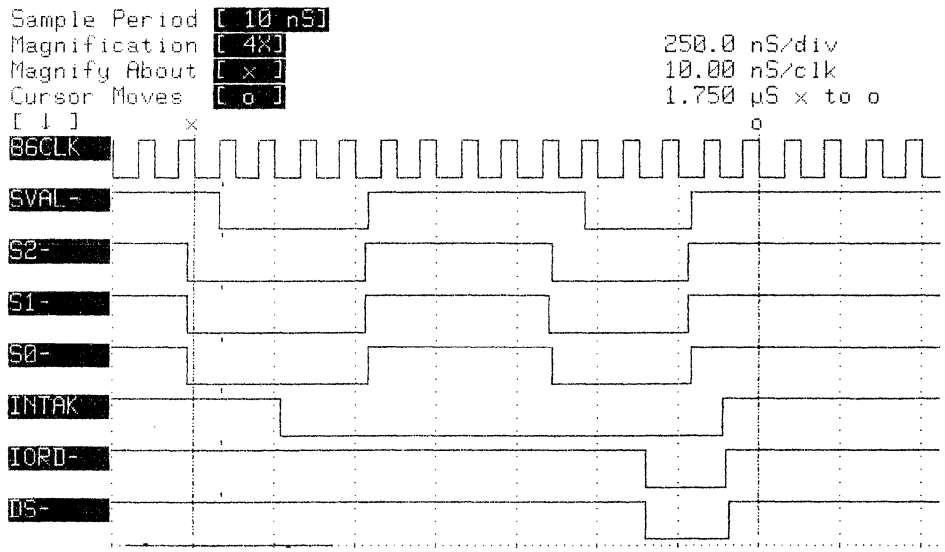


15C - Local Bus Controller PAL
(Local I/O - Read)

Figure 3-10. Communications PCB Timing Diagrams (Cont.)

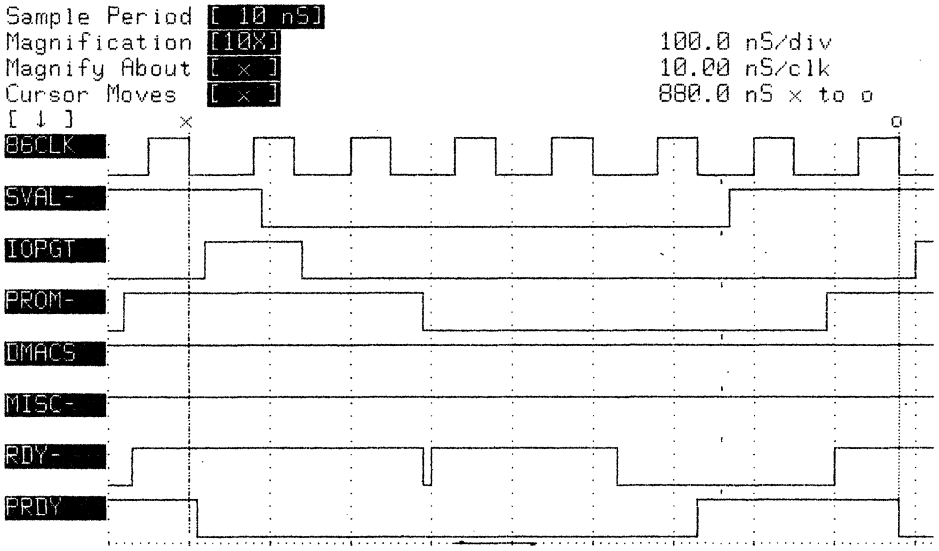


15C - Local Bus Controller PAL
(Local I/O - Write)

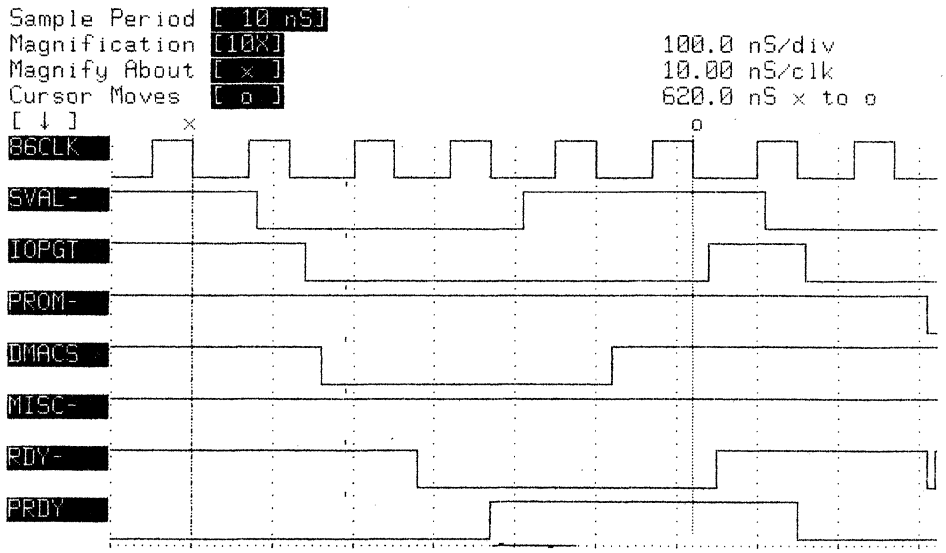


15C - Local Bus Controller PAL
(Interrupt Acknowledge Cycle)

Figure 3-10. Communications PCB Timing Diagrams (Cont.)

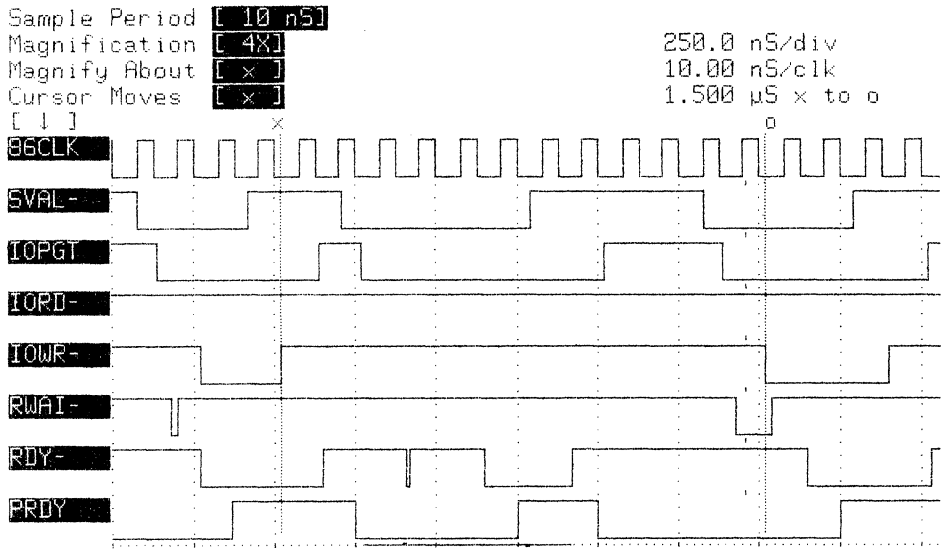


10C - Wait-State Generator PAL
(PROM - Two Wait States)

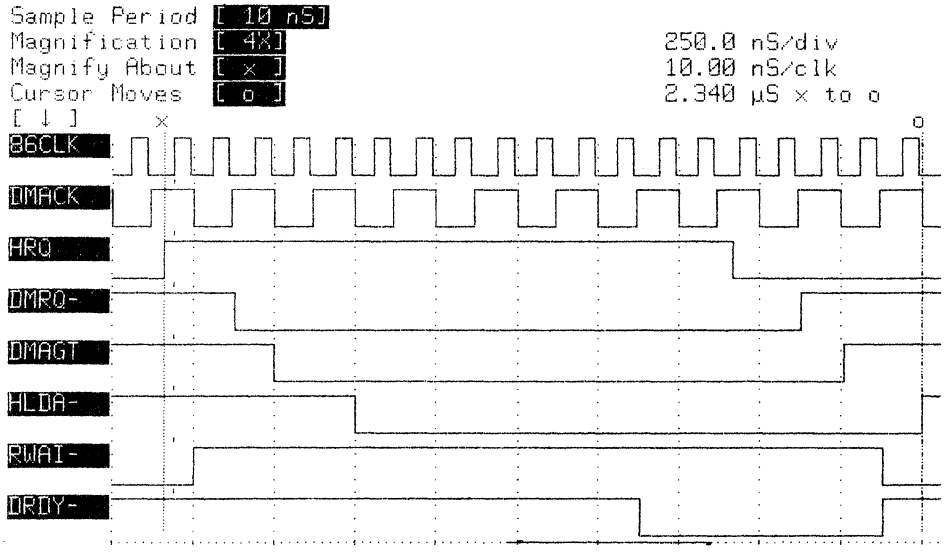


10C - Wait-State Generator PAL
(DMA Chip Select - One Wait State)

Figure 3-10. Communications PCB Timing Diagrams (Cont.)

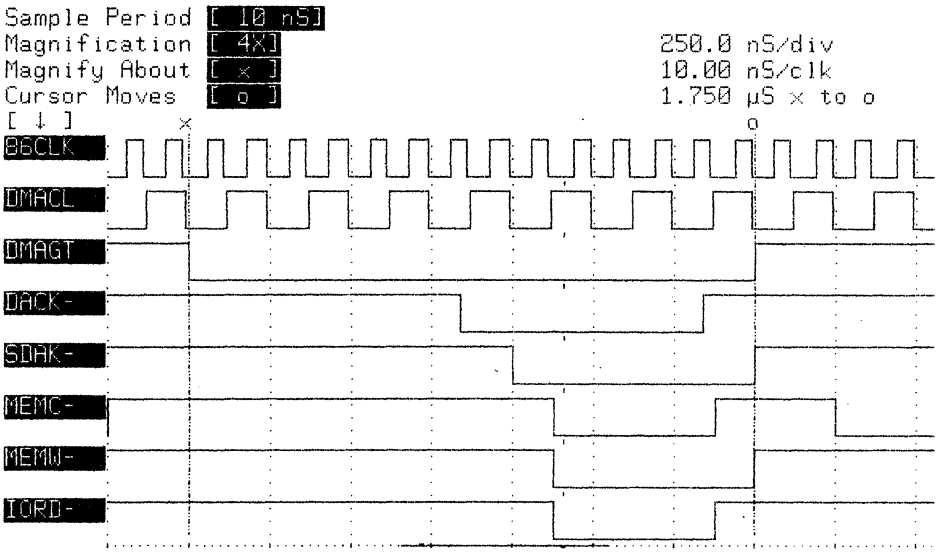


1ØC - Wait-State Generator PAL
(SCC I/O Cycle With Recovery)

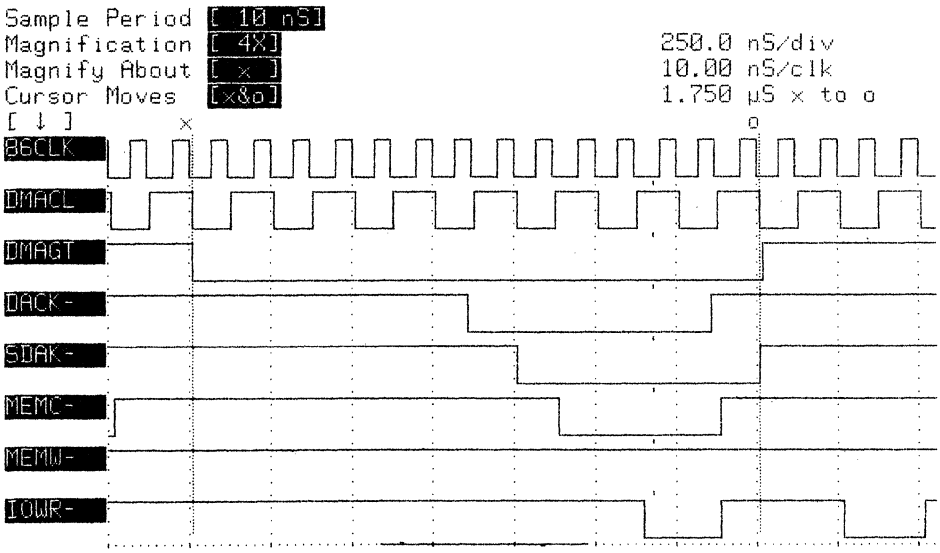


15D - DMA Refresh PAL
(DMA Request/Grant Synchronization)

Figure 3-1Ø. Communications PCB Timing Diagrams (Cont.)

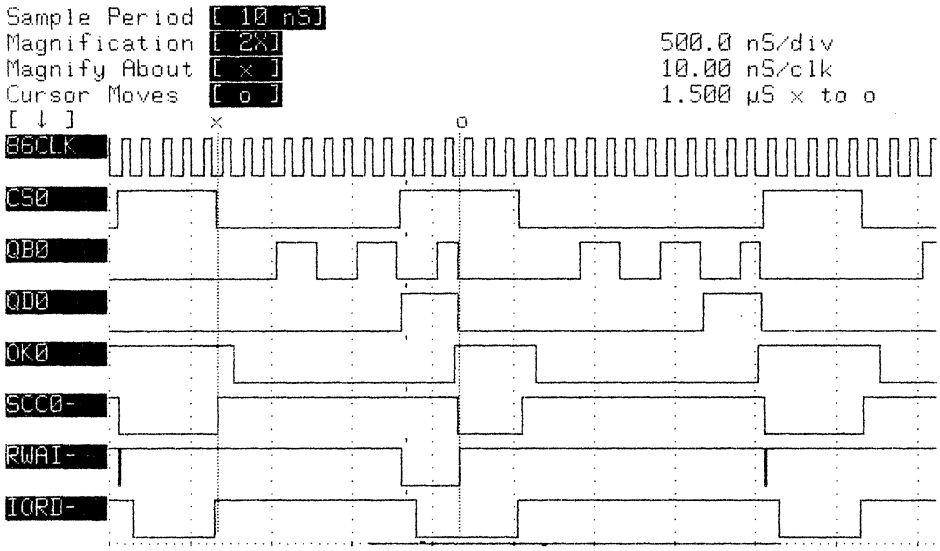


16C - DMA Read/Write PAL
(DMA I/O Read/Memory Write Cycle)



16C - DMA Read/Write PAL
(DMA I/O Read/I/O Write Cycle)

Figure 3-10. Communications PCB Timing Diagrams (Cont.)



3C - Recovery PAL
(Three Consecutive I/O Reads - Second Read Required Recovery)

Figure 3-10. Communications PCB Timing Diagrams (Cont.)

(BLANK)

File Processor PCB

The function of the file processor is to manage the data transfer between system memory and the tape, floppy, printer, hard disk, and small computer system interface (SCSI) peripheral devices. Refer to the **Schematic Diagrams** supplement to this manual for the block and schematic diagrams of the file processor PCB.

NOTE

The -001 version of the file processor PCB DOES NOT support SCSI operation. The -002 version of the file processor PCB includes SCSI.

System Interface

The file processor uses 16 of the available 32 data lines on the system bus. The file processor has the highest system bus priority (0) and uses bus request line 0 for bus requests and interrupt line 0 to interrupt the host 80286 microprocessor. The 80286 uses channel attention (address 000Eh) to interrupt the file processor.

The file processor contains an Intel 8086 microprocessor and a Hitachi 68450 direct-memory access (DMA) controller that can read or write anywhere in system memory with 24-bit addressing. The 8086 uses a 6-bit system memory page register to specify the upper address bits when accessing system memory.

NOTE

The file processor PCB has the highest system bus priority. Thus, the file processor 8086 system-bus accesses should be kept to a minimum to allow sufficient bandwidth for the PCBs with lower bus priority.

The DMA controller allows concurrent transfer of data for tape, floppy, printer, and either hard disk or

SCSI. The maximum transfer rates for tape, floppy, printer, and hard disk/SCSI are 90K, 32K, 50K, and 1.5M bytes per second respectively.

System Bus Control Logic

There are two system bus control PALs (16D and 18B) that perform system bus interface logic functions.

The system bus controller PAL 1 (16D) generates memory read or write, high byte enable (HBEN), high word enable (HWEN), and address (A00) signals. The combination of HWEN, HBEN, and A00 determines the data transfer widths. Refer to **System Bus Interface** at the front of this chapter for additional details.

The system bus controller PAL 2 (18B) handles the bus exchange control and provides data steering to the system bus by enabling the appropriate transceivers.

Refer to **Timing Diagrams** at the back of this section for 8086 read from/write to system memory timing. Also refer to **Timing Diagrams** for data transfer between system memory and tape, floppy, printer controllers, or ping-pong buffer timing.

Microprocessor

The file processor 8086 microprocessor runs at 8 MHz in Minimum Mode and manages the printer and SCSI controllers on the file processor PCB, and also the floppy, tape, and hard disk controllers on the controller PCB. The 8086 runs continuously except when the DMA controller is using system memory.

The 8086 executes out of PROM for file processor confidence tests and booting, out of local RAM for normal processing, and out of system memory to receive file processor commands and to report status.

Refer to **Timing Diagrams** at the back of this section for 8086 read/write timing.

Interrupts

The 8086 responds to nonmaskable interrupts (NMIs) such as, power failure, system memory error, and local memory parity error; and lower priority maskable interrupts such as the host 80286, DMA controller, real-time clock, and peripheral controllers.

Memory Organization

Both the DMA controller and the 8086 microprocessor use memory, but only one can address memory at a time. In case of ties between the 8086 and DMA controller, the DMA controller has priority over the 8086. Both the DMA controller and the 8086 have byte and word addressing capability.

The 8086 can address PROM, RAM, and system memory while the DMA controller can only address the system memory.

The 8086 has 20 address lines. The two most significant bits select which memory type the 8086 will access: bit code 00 will access local RAM, bit code 10 will access system memory, and bit code 11 will access PROM (bit code 01 is not used).

The memory space of the 8086 is organized as shown in Figure 3-11. The addresses between 40000h and 80000h are mapped into system memory and are movable by changing a value stored in the system memory page register.

Figure 3-12 shows the 8086 system memory address logic and the function of the system memory page register.

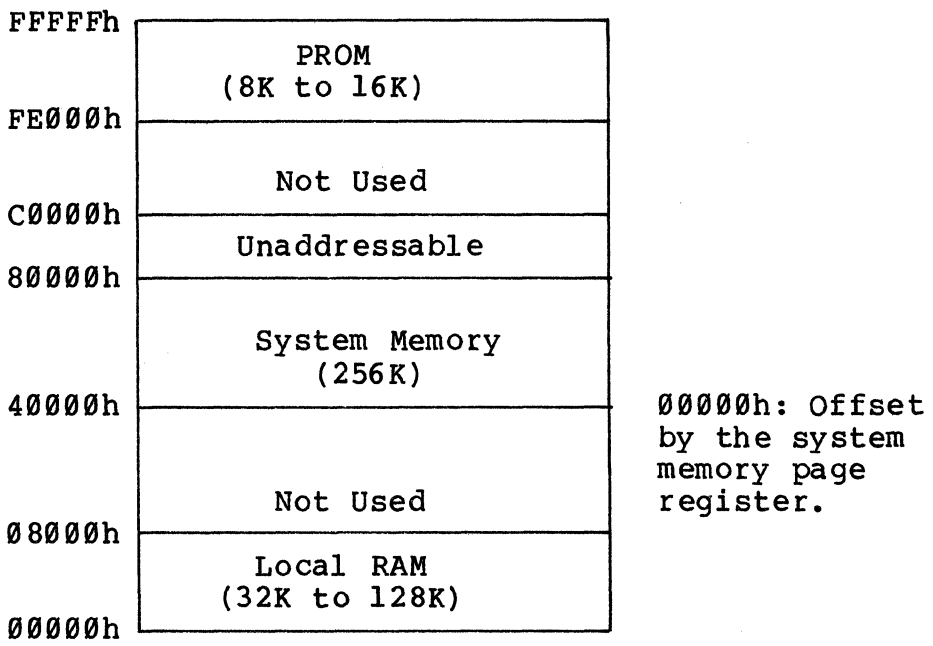


Figure 3-11. 8086 Memory Address Map

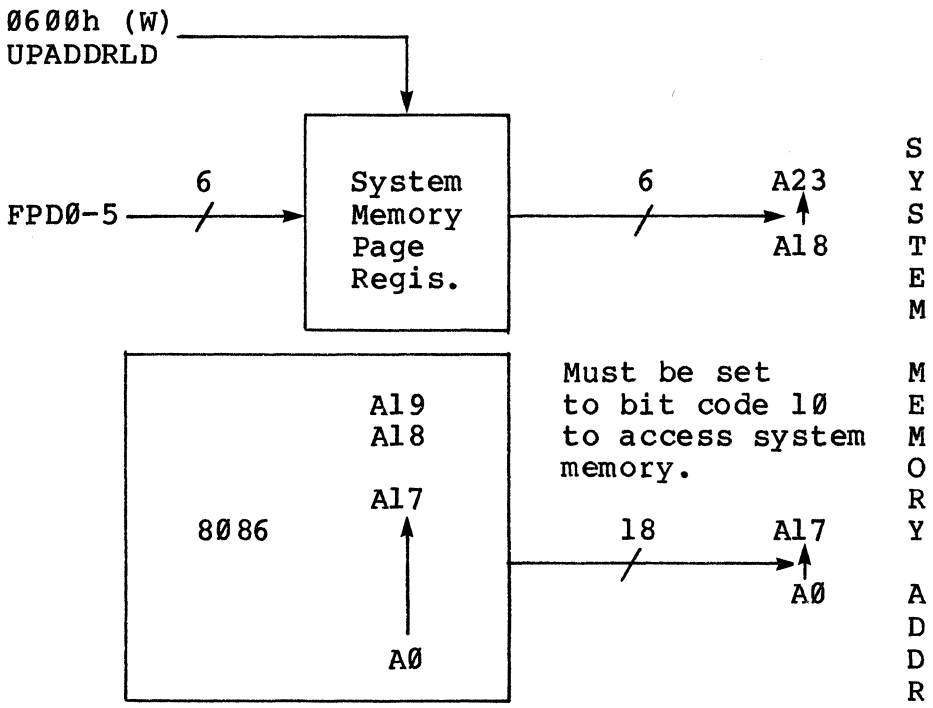


Figure 3-12. 8086 System Memory Addressing

Memory Options

In the basic system, the address space for the PROM memory is 8K bytes and 32K bytes for the RAM memory. The PROM memory in the basic system is composed of two 4K x 8 bit PROMs and the local RAM is composed of four 16K x 4 bit RAMs. The PROM memory is expandable to 16K bytes with two 8K x 8 bit PROMs and the RAM memory is expandable to 128K bytes with four 64K x 4 bit RAMs.

RAM Control Logic

The RAM control logic is contained in the RAM controller PAL (24B) which performs the following functions:

- generates row address strobe (RAS) and column address strobe (CAS) signals for the RAM
- arbitrates the local memory access and refresh cycles
- inserts wait states to the 8086 microprocessor
- decodes the upper two address bits of the 8086 microprocessor for access to either the local RAM or system memory

Refer to **Timing Diagrams** at the back of this section for 8086 read from/write to local memory timing.

Parity Errors

Local RAM parity errors cause an NMI at the 8086 microprocessor. System memory parity error and system memory access out-of-bounds error also cause an NMI at the 8086.

Common Control and Status

The common control and status ports are the file processor command register, disk mode register, and file processor status port. Refer to Tables 3-17 and

3-18 for the control and status port assignments and control and status bit assignments.

Table 3-17. Control and Status Port Assignments

Address (Hex)	R/W	Signal	Assignment
0608	W	CMDLD*	File processor command register
060C	W	DSKLD*	Disk mode register
0700	R	FPSTATUS*	File processor status port

Table 3-18. Control and Status Bit Assignments

Bits	Signal	Function
		File Processor Command Register
FPD00-FPD07	-----	Not used
FPD08	CLRST*	Clears controller PCB. Duration at least 25 microseconds
FPD09	-----	Not used
FPD10	INT286	Interrupts 80286 on interrupt line 0
FPD11	ENNMI	Enables nonmaskable interrupt (NMI) to 8086
FPD12	BURSTEN	Enables DMA controller burst logic
FPD13	MBLOCK	System bus lock (debugging aid)

Table 3-18. Control and Status Bit Assignments (Cont.)

Bits	Signal	Function
FPD14	INPUT PRIME*	Causes printer to be prepared for operation
FPD15	PENABLE	Enables data to be transferred from printer controller to printer
		Disk Mode Register
FPD00-FPD07	-----	Not used
FPD08	MBREAD	System bus read mode. Sets mode for information to flow from system bus to file processor
FPD09	SCSIMD	SCSI mode; connects SCSI controller to ping-pong buffer; when low, connects hard disk controller to ping-pong buffer
FPD10	INITBUF*	Initializes ping-pong buffer
FPD11 FPD12	BUFMD1 BUFMD0	FPD12 FPD11 Buffer Size 0 0 2K bytes 0 1 1K bytes 1 0 1.5K bytes 1 1 512 bytes
FPD13	SCSICTLRST*	Resets SCSI controller; no minimum pulse duration
FPD14	SCSIBUSRST*	Resets devices on SCSI bus; duration at least 25 microseconds
FPD15	-----	Not used

Table 3-18. Control and Status Bit Assignments (Cont.)

Bits	Signal	Function
		File Processor Status Port
FPDØØ-FPDØ7	-----	Not used
FPDØ8	PWRFAIL	Power-failure interrupt occurred
FPDØ9	MEMERR	Memory parity-error or memory address out-of-bounds interrupt occurred
FPDlØ	PERR	Local RAM parity-error interrupt occurred
FPDll	SCSIRST	External reset on SCSI bus occurred
FPDl2	MBDONE*	System bus data transfer done
FPDl3	SCSIAVAIL	SCSI controller present on file processor PCB
FPDl4,15	Ø	Grounded

Interrupt Logic

The interrupts used by the file processor are divided into two classes: nonmaskable and maskable.

Nonmaskable Interrupts. At initialization time, a reset causes the ENNMI signal (bit 11 at the file processor command register) to be low, which blocks the NMI.

After initialization, the ENNMI signal goes high to allow normal operation. When a nonmaskable interrupt occurs, the 8Ø86 samples the file processor status port to determine the type of NMI.

Then the 8086 takes appropriate action and, if possible, clears the error conditions by generating an ERRCLR signal with I/O write address 0606h. Table 3-19 lists the nonmaskable interrupts.

Table 3-19. Nonmaskable Interrupts

Type	Signal	Description
Power failure	PWRFAIL	Power supply reports marginal or no power; causes 8086 to halt processing at earliest opportunity.
System memory	MEMERR	System memory reports parity error or circuit on CPU PCB reports system memory out-of-bounds error.
File processor local RAM parity error	PERR	File processor reports local RAM parity error.

Maskable Interrupts. The maskable interrupts are handled by programmable interrupt controller 8259A operating in the edge mode. Table 3-20 lists the interrupt controller port assignments and Table 3-21 lists the maskable interrupts. Refer to the **Intel Microsystems Components Handbook** for the 8259A bit assignments and programming information.

Table 3-20. Interrupt Controller Port Assignments

Address (Hex)	Mode	R/W	Description
0500	OWC3 (RR=1,RIS=0)	W	ICW1,ICW2,ICW3
0500	OWC3 (RR=1,RIS=1)	R	Interrupt request register (IRR)
0500		R	In-service request (ISR)
0502		W	ICW2,ICW3,1CW4, OCW1
0502		R	Interrupt mask request (IMR)

Table 3-21. Maskable Interrupts

Priority	Type	Signal	Description
0	Hard disk controller interrupt	DINT	Asserted by hard disk controller WD2010 on completion of a command; remains high until status register is read or a new command is written into the WD2010 command register
1	HD68450 DMA interrupt	DMAINT	Indicates termination of channel operation for one of the four channels. Refer to **Hitachi Microcomputer Data Book** for additional information

Table 3-21. Maskable Interrupts (Cont.)

Priority	Type	Signal	Description
2	SCSI controller interrupt	SCSINT	Interrupt for SCSI bus conditions that require service. Refer to **National Cash Register NCR 5385 SCSI Protocol Controller Data Sheet** for additional information
3	Tape controller interrupt	TINT	Indicates tape ready or tape exception condition. Refer to **Archive QIC-Ø2 1/4-Inch Cartridge Tape Drive Interface Standard** for additional information
4	Timer Ø interrupt	TMRØ*	Real-time interrupt. Refer to **Intel Microsystem Components Handbook** for additional 8254 (mode 2) information
5	8Ø286 microprocessor interrupt	286INT	Attention interrupt (ØØØEh) to file processor PCB

Table 3-21. Maskable Interrupts (Cont.)

Priority	Type	Signal	Description
6	Floppy controller interrupt	FINT	Indicates floppy disk controller needs serivce. Refer to **NEC PD765 Data Sheet** for additional information
7	----------	Ø	Grounded

Timer

Timer 8254 contains three programmable timers (Ø, 1, and 2). The addresses of timers Ø, 1, and 2 are 4ØØh, 4Ø2h, and 4Ø4h respectively. (Refer to the **Intel Microsystem Components Handbook** for the 8254 programming details.) Timer Ø is a real-time clock that decrements each microsecond. Timer Ø should be used in mode Ø or 3 only. When timer Ø reaches its limit, it interrupts programmable interrupt controller 8259A-2 (see Table 3-22).

Timer 1 limits the number of consecutive DMA accesses to the system bus when it is operating in the burst mode and decrements each time the file processor is granted a bus cycle until the timer's limit is reached (called burst-on time). Then timer 1 switches control to timer 2. Timer 1 should be programmed in mode 2 only.

Timer 2 determines how long the file processor DMA remains off the system bus when operating in the burst mode and decrements during the burst-off time until the timer's limit is reached. Then timer 2 switches control back to timer 1. Timer 2 should be programmed in mode 2 only.

Burst Logic

The burst logic limits the use of the system bus by the file processor, since the file processor could lock out the lower priority PCBs.

When the burst enable (BURSTEN) signal (bit 12 from the file processor command register) is low, the file processor operates normally. When BURSTEN is high, the file processor accesses system memory in bursts. The burst logic is automatically turned off at reset.

The burst logic uses the two timers located in the 8254 timer. Timer 1 is a burst-on timer that regulates the number of system memory cycles, stops when the timer limit is reached, and then passes control to timer 2. Timer 2 is a burst-off timer that decrements each microsecond until its limit is reached, and then passes control back to timer 1. The address of timer 1 and 2 is 402h and 404h respectively. (Refer to the **Intel Microsystem Components Handbook** for the 8254 programming details.)

DMA Controller

The DMA controller is a four-channel, 8 MHz, Hitachi HD68450-8 integrated circuit that operates in single-addressing mode (data is transferred around rather than through the DMA controller). The channel assign ments beginning with the highest priority are: Channel 0 = tape, channel 1 = floppy disk, channel 2 = printer, and channel 3 = hard disk/SCSI.

The DMA controller performs byte transfers on channels 0 through 2 with byte steering to the upper or lower byte position accomplished on the fly. The DMA controller performs word transfers on channel 3 in bursts governed by the burst logic. Table 3-22 lists the DMA controller port assignments for the internal registers. Refer to the **Hitachi Microcomputer Data Book** for register bit assignments and additional programming information.

Refer to **Timing Diagrams** in the back of this section for data transfer between system memory and tape, floppy, printer, and hard disk controllers timing.

Also, refer to **Timing Diagrams** for 8086 read from/write to DMA controller timing.

Table 3-22. DMA Controller Port Assignments

Address (Hex)					
Ch 0	Ch 1	Ch 2	Ch 3	R/W	Registers
0200	0240	0280	02C0	R/W	Channel status register (CSR)
0201	0241	0281	02C1	R	Channel error register (CER)
0204	0244	0284	02C4	R/W	Device control register (DCR)
0205	0245	0285	02C5	R/W	Operation control register (OCR)
0206	0246	0286	02C6	R/W	Sequence control register (SCR)
0207	0247	0287	02C7	R/W	Channel control register (CCR)
020A	024A	028A	02CA	R/W	Memory transfer counter (MTC)--Word
020C	024C	028C	02CC	R/W	Memory address register (MAR)--high word
020E	024E	028E	02CE	R/W	Memory address register (MAR)--low word
0214	0254	0294	02D4	R/W	Device address register (DAR)--high word
0216	0256	0296	02D6	R/W	Device address register (DAR)--low word
021A	025A	029A	02DA	R/W	Base transfer counter (BTC)--high word
021C	025C	029C	02DC	R/W	Base address register (BAR)--high word
021E	025E	029E	02DE	R/W	Base address register (BAR)--low word
0225	0265	02A5	02E5	R/W	Normal interrupt vector (NIV)
0227	0267	02A7	02E7	R/W	Error interrupt vector (EIV)
022D	026D	02AD	02ED	R/W	Channel priority register (CPR)
0229	0269	02A9	02E9	R/W	Memory function code (MFC)
0231	0271	02B1	02F1	R/W	Device function code (DFC)
0239	0279	02B9	02F9	R/W	Base function code (BFC)
02FF				R/W	General control register (GCR)

Ping-Pong Buffer

The ping-pong buffer has a pair of sector buffers that are used for hard disk and SCSI traffic. The main function of the ping-pong buffer is to provide contin-

uous data transfer by allowing one buffer to load while the other is unloading data.

There are four independent control devices that interact with the ping-pong buffer: system bus sequencer, hard disk controller WD2010, SCSI sequencer, and disk buffer sequencer. When the ping-pong buffer is operating, the system bus and buffer sequencers are active and either the hard disk controller or the SCSI sequencer is active.

The system bus sequencer controls the transfer of bytes between the ping-pong buffer and the system bus by packing bytes into words and unpacking words into bytes.

The hard disk controller loads or unloads its side of the ping-pong buffer. In addition, the hard disk controller may edit the data before relinquishing the buffer.

The SCSI sequencer loads and unloads its side of the ping-pong buffer for the SCSI controller.

The disk buffer sequencer waits for the sequencers on both sides of the ping-pong buffer to finish loading or unloading their respective buffer, then the disk buffer sequencer flips the ping-pong buffer. Bits FPD08 through FPD12 of the disk mode register control the ping-pong buffer. Refer to Table 3-18 for the disk mode register control-bit assignments. The definitions of the control signals described in Table 3-18 are discussed in more detail as follows.

The system bus read (MBREAD) signal (bit 8) determines the direction of data flow for the ping-pong buffer. When MBREAD is high, data is read from the system bus into the ping-pong buffer and then written to the hard disk or SCSI controller. When the SCSI mode (SCSIMD) signal (bit 9) is high, the SCSI controller is connected to the ping-pong buffer. When SCSIMD is low, the hard disk controller is connected to the ping-pong buffer. When the initialize buffer (INITBUF*) signal is low, the ping-pong buffer is initialized. The buffer mode (BUFMD0 and 1) signals select the size of the ping-pong buffer (512, 1K, 1.5K, or 2K bytes).

Ping-Pong Buffer Control Logic

The majority of the control logic for the ping-pong buffer is implemented by the following PALs:

- disk register gating PAL (13D)
- disk buffer sequencer PAL (14D)
- disk buffer gating PAL 1 and 2 (12C and 12D)
- DMA arbitration PAL (11C)

The heart of the ping-pong buffer control logic is contained in the disk buffer sequencer PAL. In addition to the state sequence logic, the disk buffer sequencer contains an AFF, disk-done (DISKDONE), SCSI-done (SCSIDONE), and system-bus-done (MBDONE) flip-flop. The purpose of this PAL is to manage the toggling of the ping-pong buffer.

When initialized (via the INITBUF signal), the sequencer goes to the idle state and the AFF is reset (for read) or set (for write). When AFF is set, the A side of the ping-pong buffer is facing the disk controller (WD2010) and the SCSI controller. The B side of the ping-pong buffer is facing the system bus.

Also, at initialization time, the ping-pong buffer counters are loaded with a count specified by the BUFMD0 and BUFMD1 signals. When each buffer counter reaches its limit (as a result of the buffer being loaded or emptied), the appropriate DONE flip-flops are set. When the MBDONE flip-flop and either the DISKDONE or the SCSIDONE flip-flops are set, the sequencer generates a flip-buffer signal which toggles the buffer, loads the counters, resets the DONE flip-flops, and changes the state of the AFF flip-flop. Then the process repeats.

Another section of the ping-pong buffer is called the system bus sequencer. The system bus sequencer uses a combination shift-register and disk-register gating PAL to move data between the ping-pong buffer and the disk register. The system bus sequencer begins operation when the DTACK signal occurs to indicate that a system memory cycle is complete. The sequencer then starts to

move two bytes between the disk register and the ping-pong buffer. When finished, the sequencer waits for another DTACK signal to repeat the cycle.

The SCSI sequencer operates the same as the system bus sequencer, except that the cycle begins when the SCSIDREQ signal occurs. Then the SCSI sequencer transfers one byte between the SCSI controller and the ping-pong buffer.

The method of data transfer between the disk controller (WD2010) and the ping-pong buffer is determined by the WD2010 protocol. Refer to the **Western Digital WD2010 Data Handbook** for additional details.

The disk-buffer gating PALs use the signals generated by the various sequencers to make the read, write, and increment signals for the ping-pong buffer.

The data transfer between the ping-pong buffer and system memory is pipelined. Thus, the first and last words transferred require special handling by the DMA arbitration PAL. The DMA arbitration PAL performs this function by raising and dropping the DMA request at precise times determined by the states of the registers.

Refer to **Timing Diagrams** at the back of this section for ping-pong buffer timing.

Controller Interface

The controller interface provides the interface between the file processor and controller PCBs. The controller interface has two data buses and a set of miscellaneous control lines. The primary data bus (BD0-7) is an 8-bit bidirectional bus used for sending commands and receiving status from the tape, floppy disk, and hard disk controllers on the con troller PCB. In addition, the primary data bus is used to transfer data between the file processor and the tape or floppy disk controllers.

The secondary data bus (DD0-7) is an 8-bit bidirec tional bus used by the hard disk controller to transfer data to/from the ping-pong buffer.

The control lines can be divided into three groups. The first group contains the interrupt lines (DINT*, TINT*, and FINT*) that are connected between the hard disk, tape, and floppy disk controllers respectively. When asserted, these control signals indicate which controller is interrupting the file processor.

The second group contains the address latch enable and controller reset (ALE and CTLRST*) signals that load the address latch and reset the controller PCB.

The third group contains the controller read, write, and chip select (CTLRD*, CTLWR*, and DFTCS*) lines that are used to access all the controllers and ports on the controller PCB. Refer to the Controller PCB discussion later in this chapter for addressing and programming the hard disk, floppy disk, and tape controllers.

Controller PCB Read/Write Control Logic

The controller PCB read/write control logic is contained in the DMA read/write control PAL (12B) which performs the following functions:

- generates read and write signals for the controller PCB
- controls the DMA data transfer for the floppy disk and tape drives
- controls the direction of the controller data transceiver

Refer to **Timing Diagrams** in the back of this section for data transfer between system memory and floppy disk or tape controller timing. Also, refer to **Timing Diagrams** for 8086 read from/write to hard disk controller timing.

Printer Controller

The printer controller contains the printer logic PAL (21A) which generates the DATA STROBE signal to the parallel printer interface. The printer logic PAL keeps the DMA data transfer rate for the printer under

50K bytes per second so that enough bandwidth remains for ping-pong buffer data transfers.

The printer controller has a Centronics interface that allows any peripheral device with a centronics interface to connect to the system. The interface consists of the printer data register for transmitting information and the printer status port for receiving status from a peripheral device. The printer data can be loaded via programmed I/O or from the DMA controller.

The transfer rate, when connected to the DMA controller, is a maximum of 50K bytes per second. The programmed I/O is used during boot diagnostics to report the file processor hardware status. Refer to Tables 3-23 and 3-24 for the printer port and status port bit assignments.

Refer to **Timing Diagrams** at the back of this section for data transfer between system memory and printer timing.

Table 3-23. Printer Port Assignments

Addresses (Hex)	R/W	Description
0602	W	Printer data register
0704	R	Printer status port

Table 3-24. Printer Status Port Bit Assignments

Bits	Signal	Function
FPD00	ACK	Acknowledge pulse (2-5 microseconds) which indicates either the receipt of a data character by a peripheral device or the end of a functional operation

Table 3-24. Printer Status Port Bit Assignments (Cont.)

Bits	Signal	Function
FPDØ1	BUSY	Level which indicates that the peripheral device cannot receive data
FPDØ2	PE (Paper Empty)	Level which indicates that the printer is out of paper
FPDØ3	SELECT	Level which indicates that the peripheral is selected
FPDØ4	FAULT* (Page Fault*)	Level which indicates a paper empty, light detect, or deselect condition
FPDØ5	PREQ*	Not-printer request; when low, requests the printer data register to be refilled; when high, the printer data register is full
FPDØ6, FPDØ7	Ground	Always low
FPDØ8-FPDl5	-----	Not used

SCSI Controller

The SCSI controller is a general-purpose controller that provides an external connection to the industry standard SCSI bus. The SCSI bus allows a maximum of seven peripheral devices to be connected to the SCSI controller at the same time, provided software drivers are in place. The peripheral devices may consist of disk drives, tape drives, printers, etc. The maximum transfer rate of the SCSI bus is 1.5M bytes per second. Refer to the **ANSI X3T9.2/82-2 SCSI Small**

Computer System Interface specification for detailed characteristics of the SCSI bus.

The heart of the SCSI controller is a National Cash Register (NCR) 5385E SCSI protocol controller integrated circuit. The 5385E integrated circuit has address Ø on the SCSI bus and performs all the SCSI protocols on the SCSI bus for the 8Ø86 microprocessor. The 5385E interrupts the 8Ø86 microprocessor after completion of each task.

The reset logic for the SCSI controller and bus is external to the SCSI controller integrated circuit. Two control signals for resetting the SCSI controller and bus are described in the Disk Mode Register portion of Table 3-18. Also, logic is provided to detect any external reset pulse that occurs on the SCSI bus.

When an external reset occurs, a latch presets which causes bit 12 of the file processor status port to go high (see the File Processor Status Port portion of Table 3-18).

Thus, the software can detect a reset on the SCSI bus by sampling the file processor status port. After the status is noticed, the software can clear the latch by performing a read to address Ø7Ø2h (see Table 3-25 for the SCSI port assignments).

The SCSI controller does not directly notify the ping-pong buffer that data transfer has been completed. Instead, the SCSI controller interrupts the 8Ø86 microprocessor via the SCSI interrupt integrated circuit. Then the software must generate a SCSI-done strobe (see Table 3-24 for the printer status port bit assignments) which causes the ping-pong buffer to finish the SCSI bus data transfer.

Table 3-25 describes the SCSI controller port assignments. Refer to the **National Cash Register (NCR) Data Handbook** for additional programming information on the NCR 5385E SCSI protocol controller.

Refer to **Timing Diagrams** at the back of this section for data transfer between SCSI controller and ping-pong buffer timing.

Table 3-25. SCSI Controller Port Assignments

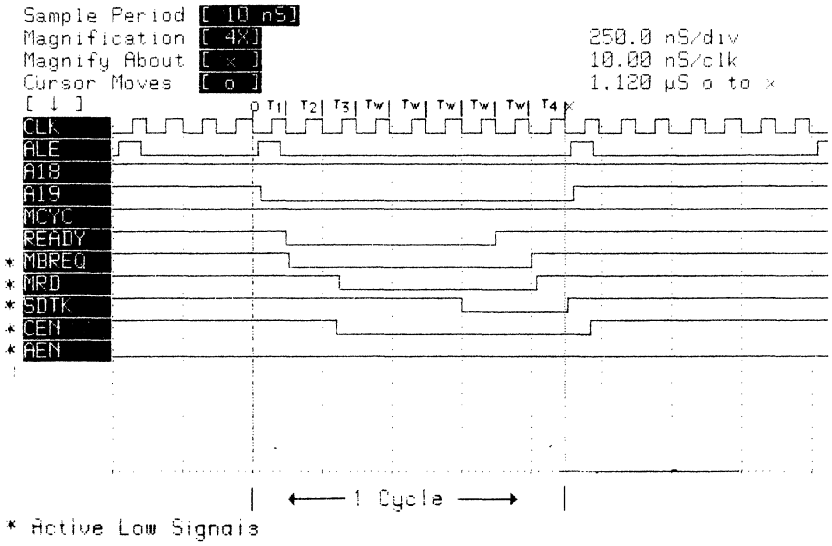
Address (Hex)	R/W	Assignment
Ø3ØØ	R/W	Data register
Ø3Ø2	R/W	Command register
Ø3Ø4	R/W	Control register
Ø3Ø6	R/W	Destination ID register
Ø3Ø8	R	Auxiliary status register
Ø3ØA	R	ID register
Ø3ØC	R	Interrupt register
Ø3ØE	R	Source ID register
Ø312	R	Diagnostic status
Ø318	R/W	Transfer counter (MSB)
Ø31A	R/W	Transfer counter (2nd byte)
Ø31C	R/W	Transfer counter (LSB)
Ø6Ø4	W	SCSI done strobe
Ø7Ø2	R	Clear SCSI reset status

File Processor Initial Program Load (IPL) Process

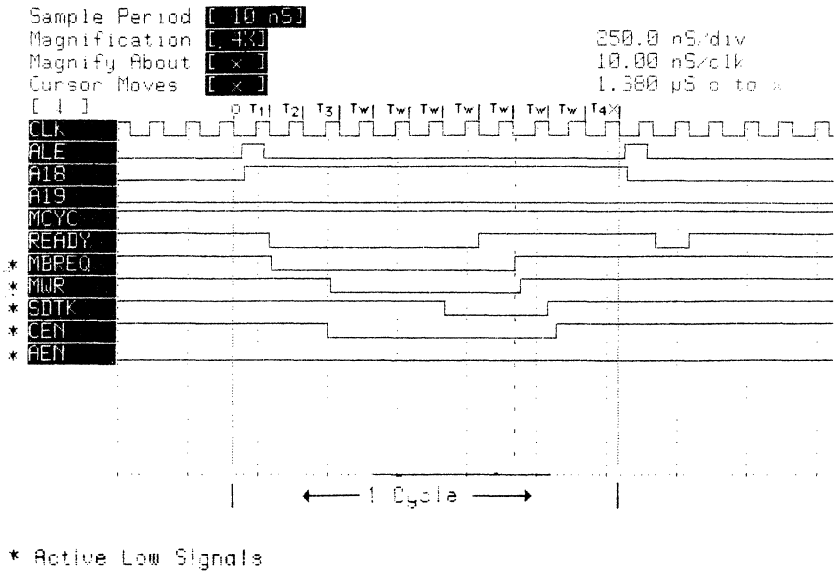
At power-up time, a reset occurs that clears all logic, blocks the nonmaskable interrupts, and causes the 8Ø86 microprocessor to jump to location FFFFØh of the PROM. Then firmware determines the boot process.

Timing Diagrams

The major timing diagrams for the file processor PCB are shown in Figure 3-13.

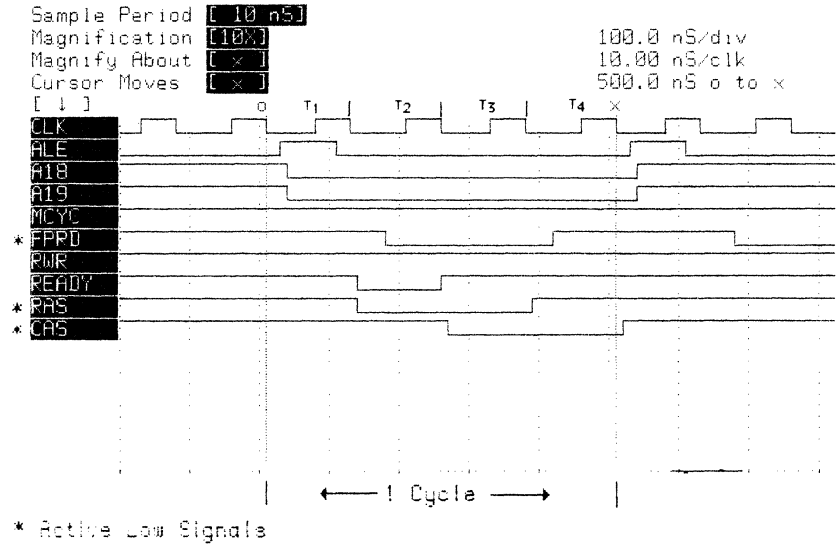


8086 Read From System Memory

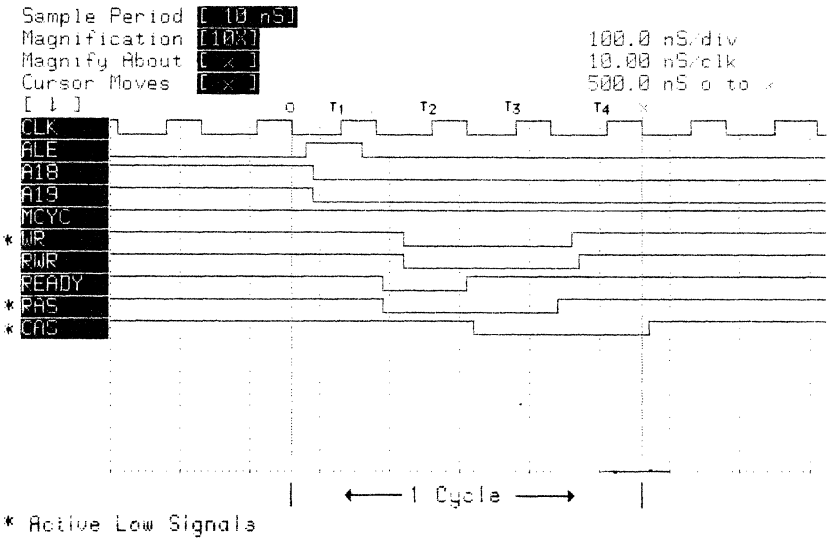


8086 Write to System Memory

Figure 3-13. File Processor PCB Timing Diagrams

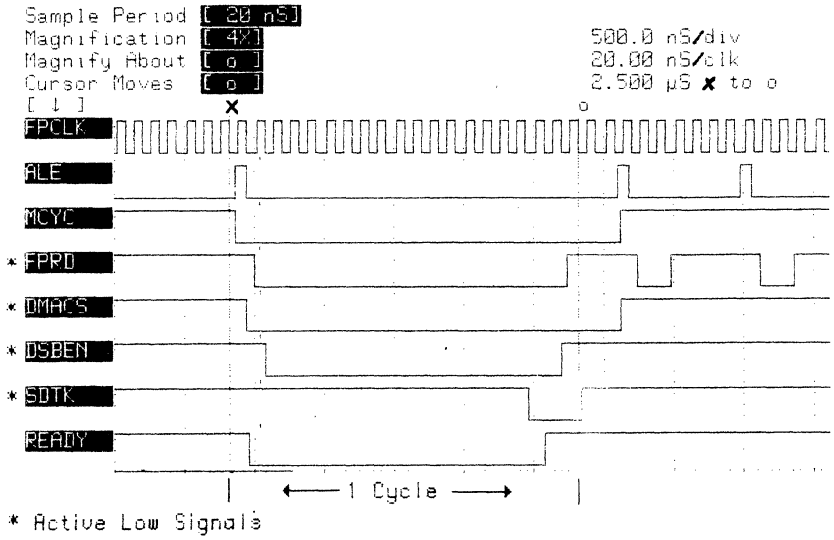


8086 Read From Local RAM

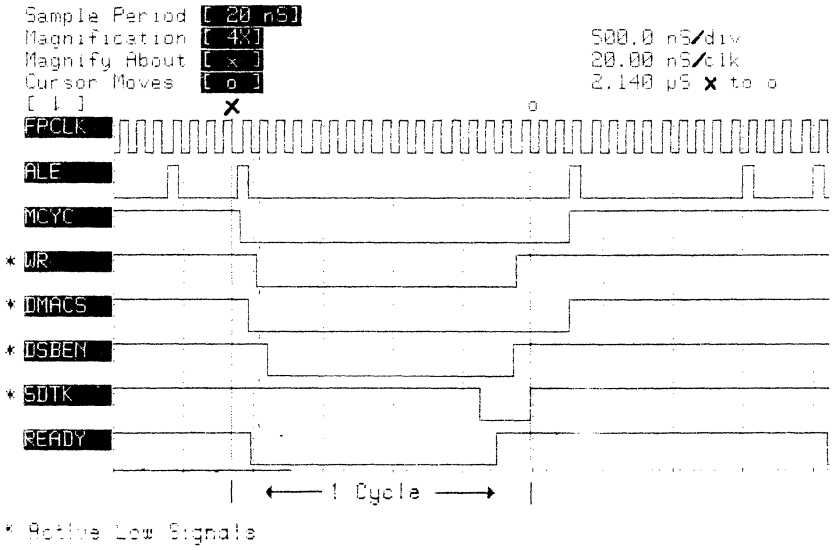


8086 Write to Local RAM

Figure 3-13. File Processor PCB Timing Diagrams (Cont.)

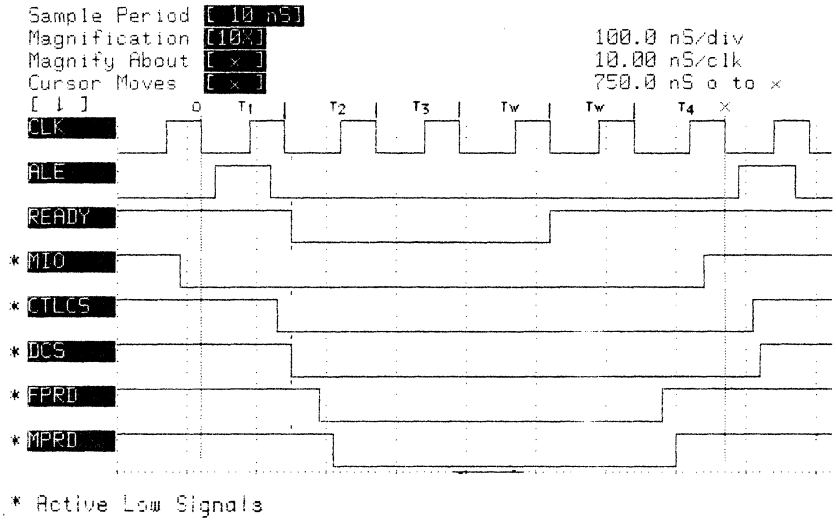


8086 Read From DMA Controller

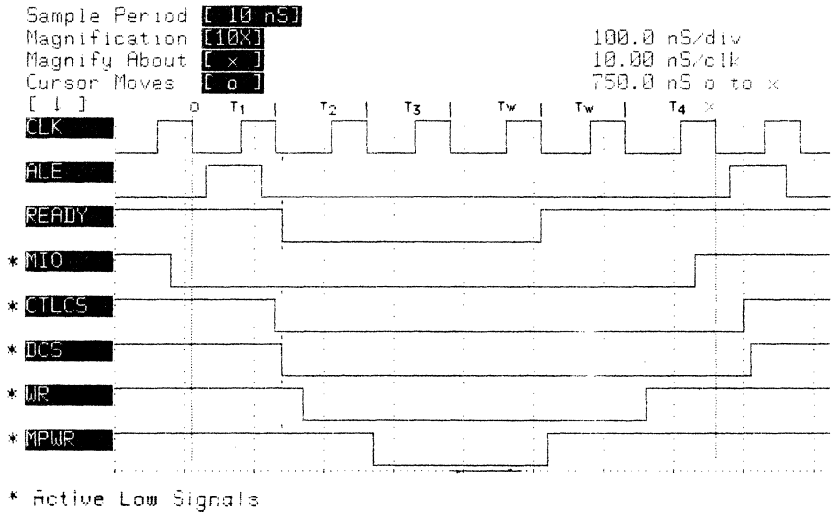


8086 Write to DMA Controller

Figure 3-13. File Processor PCB Timing Diagrams (Cont.)

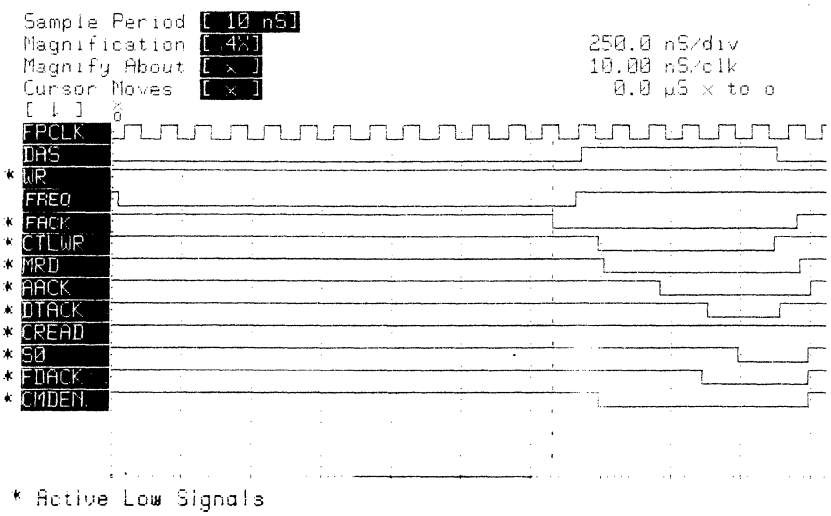


8086 Read From Hard Disk Controller

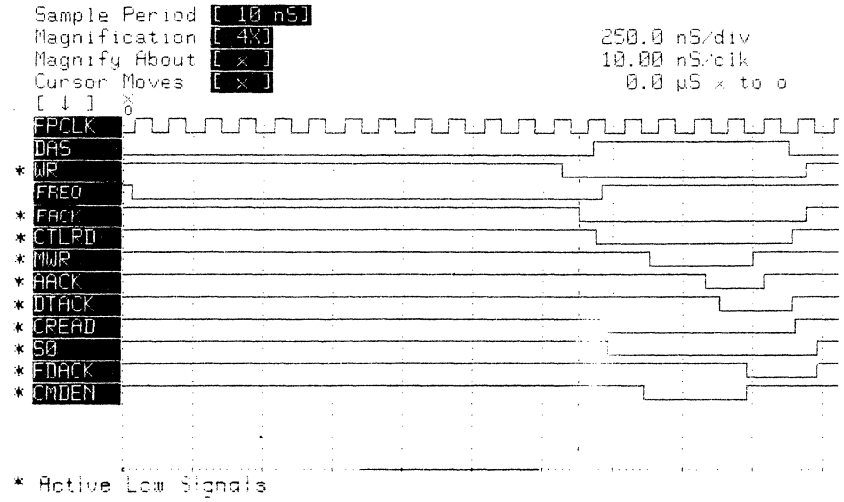


8086 Write to Hard Disk Controller

Figure 3-13. File Processor PCB Timing Diagrams (Cont.)

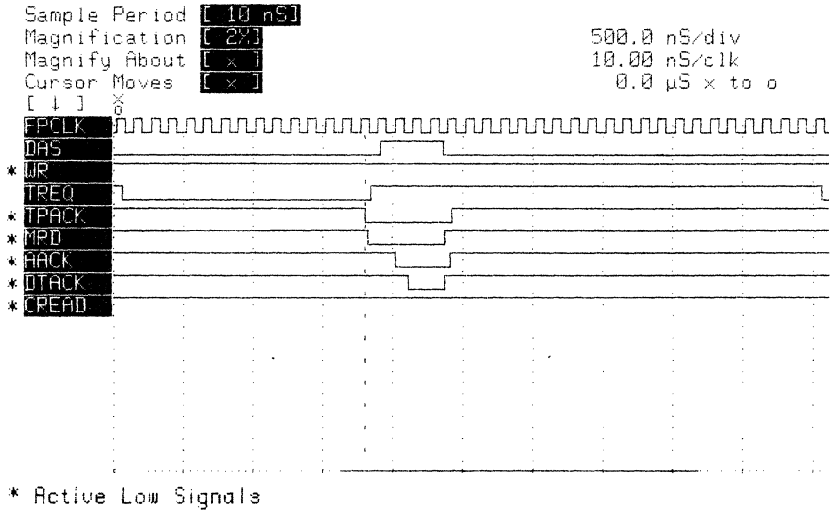


Data Transfer From System Memory to Floppy Disk Controller

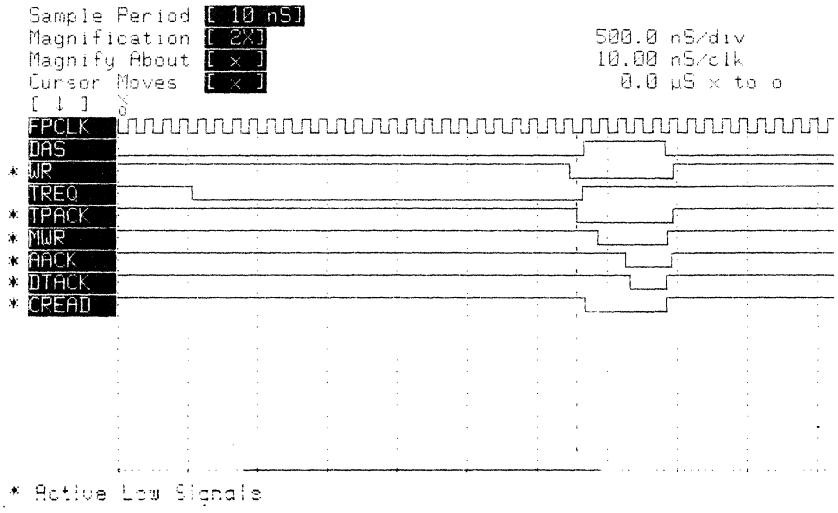


Data Transfer From Floppy Disk Controller to System Memory

Figure 3-13. File Processor PCB Timing Diagrams (Cont.)

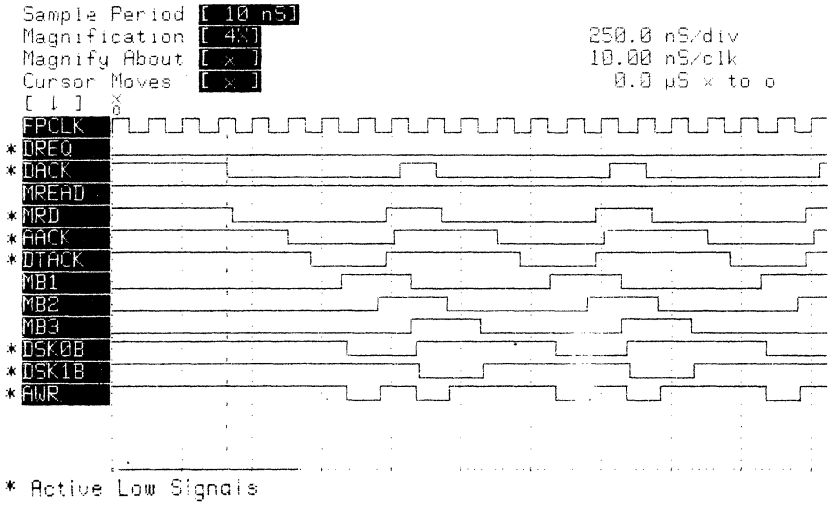


Data Transfer From System Memory to Tape Controller

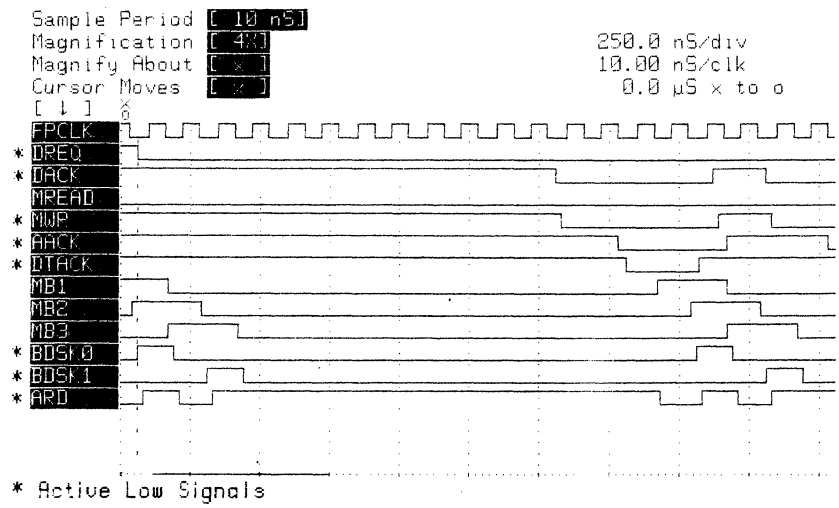


Data Transfer From Tape Controller to System Memory

Figure 3-13. File Processor PCB Timing Diagrams (Cont.)

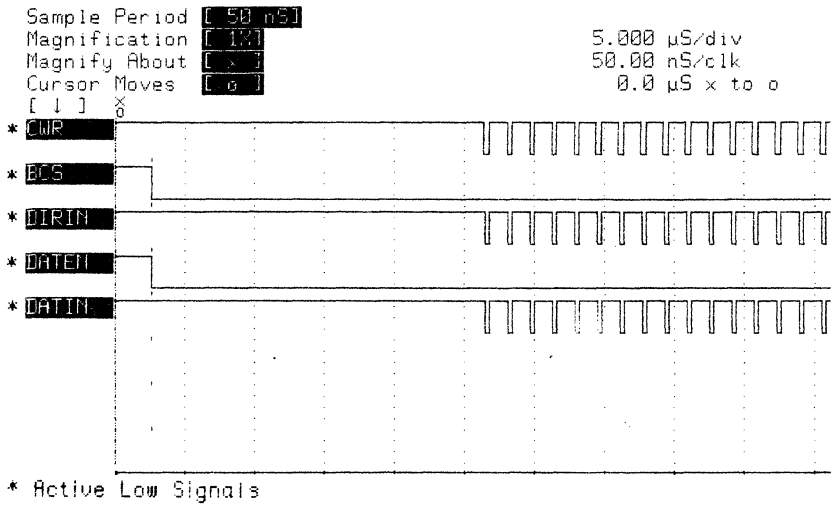


Data Transfer from System Memory to Ping-Pong Buffer

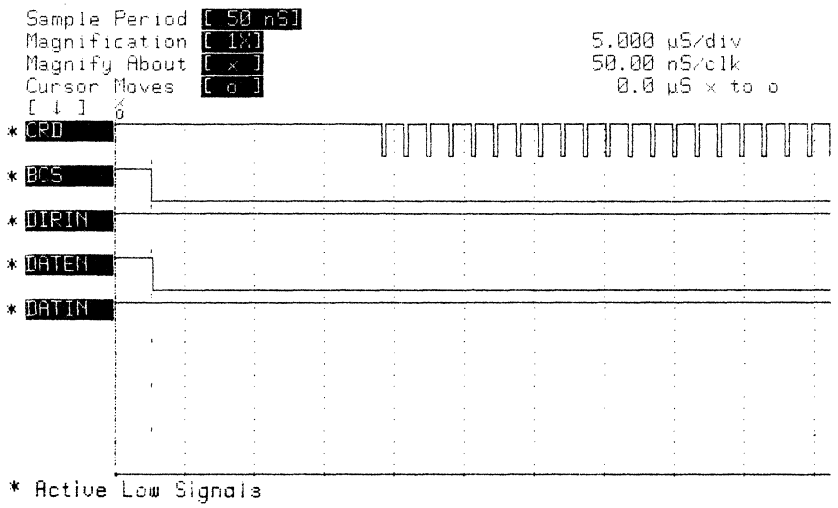


Data Transfer From Ping-Pong Buffer to System Memory

Figure 3-13. File Processor PCB Timing Diagrams (Cont.)

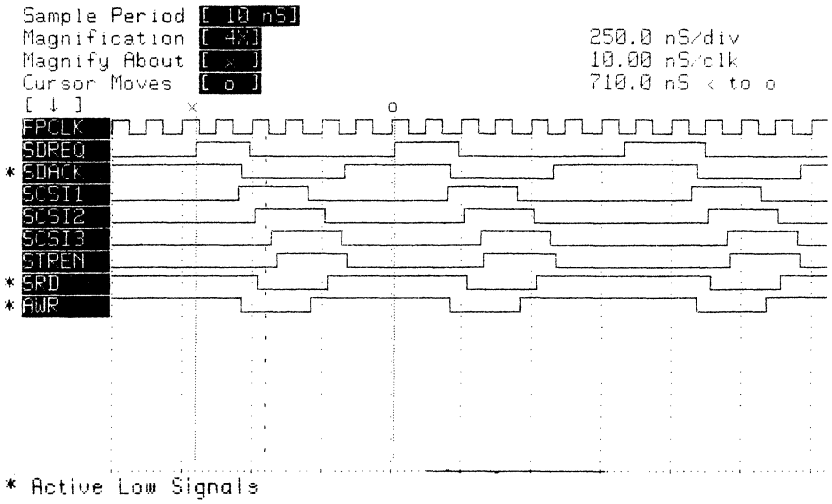


Data Transfer From Hard Disk Controller to Ping-Pong Buffer

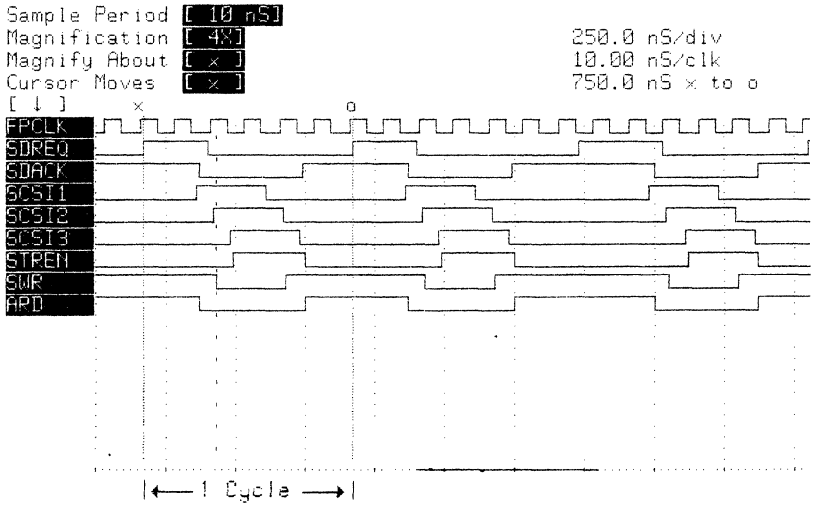


Data Transfer From Ping-Pong Buffer to Hard Disk Controller

Figure 3-13. File Processor PCB Timing Diagrams (Cont.)

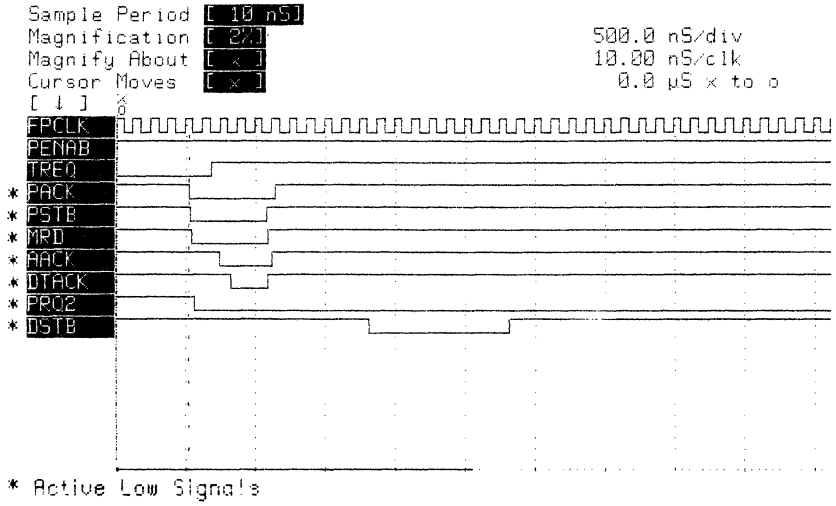


Data Transfer From SCSI Controller to Ping-Pong Buffer



Data Transfer From Ping-Pong Buffer to SCSI Controller

Figure 3-13. File Processor PCB Timing Diagrams (Cont.)



Data Transfer From System Memory to Printer Controller

Figure 3-13. File Processor PCB Timing Diagrams (Cont.)

Controller PCB

The function of the controller PCB is to provide the device controllers for the floppy disk, hard disk, and streaming tape drives. Refer to the **Schematic Diagrams** supplement to this manual for the block and schematic diagrams for the controller PCB.

The controller PCB contains three independent controllers that are managed by the file processor PCB to provide fast data transfer between the system and the hard disk, floppy disk, and streaming tape drives. All three controllers can operate concurrently.

Controller Initialization

The controller circuits are reset after power-up (system reset), manual reset, or when the file processor issues a reset. The file processor PCB clears all of the controllers by toggling the reset controller board bit (DØ8) in the file processor command register which generates a controller reset (CTLRST*) signal. Reset must be asserted for at least 25 microseconds.

The tape controller can be independently reset by toggling the reset tape controller bit (BD4) in the tape control register (reset must be asserted for at least 25 microseconds). Likewise, the hard disk controller can be independently reset by toggling the reset hard disk controller bit (BD6) in the sector/drive/head register (reset must be asserted for at least 5 microseconds).

Hard Disk Controller

The hard disk controller interfaces up to three ST5Ø6-type Winchester disk drives to the system and provides the following capabilities:

- seek overlap on all three drives
- reads or writes on one drive at a time
- program selected automatic transparent retries

- selects up to 16 heads with the programmable sector/drive/head (SDH) register
- provides a 32-bit error correction code (ECC) that either corrects data in the sector buffer automatically, supplies software with the error location and pattern, or takes no action other than setting the error flag and lets software do the entire error correction

The hard disk controller contains three programmable devices: a Western Digital WD2010 hard disk controller, an SDH register, and a controller PCB status port. See Tables 3-26 and 3-27 for the controller port and bit assignments. Refer to the **Western Digital Handbook** for details on the WD2010 hard disk controller.

Refer to **Timing Diagrams** at the back of the previous file processor PCB section for 8086 read from/write to hard disk controller timing. Also, refer to **Timing Diagrams** for data transfer between ping-pong buffer and hard disk controller timing.

Table 3-26. Hard Disk Controller Port Assignments

Address (Hex)	R/W	Signal	Description
			WD2010 Internal Ports
0002	R		Error register
	W		Precomp cylinder
0004	R/W		Sector count
0006	R/W		Sector number
0008	R/W		Cylinder low
000A	R/W		Cylinder high
000C	R/W		SDH register
000E	R		Status register
	W		Command register

Table 3-26. Hard Disk Controller Port Assignments (Cont.)

Address (Hex)	R/W	Signal	Description
			External Ports
0050	R	INPORTCS*	Controller PCB status port
0060	W	WRSDH*	SDH register

Table 3-27. Hard Disk Controller Bit Assignments

Bit	Signal	Description
		SDH Register
BD0-BD3	HEADSEL0-3	Head select (0-15)
BD4-BD5	SELA,SELB	Drive select BD5 BD4 Drive Select 0 0 Drive 1 0 1 Drive 2 1 0 Drive 3 1 1 None
BD6*	DRESET*	Reset hard disk controller
BD7	-------	Not used
		Controller PCB Status Port
BD0	TEXCEPT	Tape except. Not used for hard disk - see Table 3-31
BD1	TRDY	Tape ready. Not used for hard disk - see Table 3-31
BD2	TDIR	Tape direction. Not used for hard disk - see Table 3-31

Table 3-27. Hard Disk Controller Bit Assignments (Cont.)

Bit	Signal	Description
BD3	DRIVE SELD1	Drive 1 selected. Signal goes high when drive 1 is selected and drive 1 is installed
BD4	DRIVE SELD2	Drive 2 selected. Signal goes high when drive 2 is selected and drive 2 is installed
BD5	DRIVE SELD3	Drive 3 selected. Signal goes high when drive 3 is selected and drive 3 is installed
BD6	GND	Always low
BD7	SELD	Tape drive select. Not used for hard disk - see Table 3-31

Floppy Disk Controller

The floppy disk controller uses a NEC uPD765 integrated circuit (IC) which interfaces the file processor to one floppy disk drive. The floppy disk controller has a built-in data separator that supports a single or double-density, single or dual speed, 5-1/4 inch drive.

Handshaking signals are provided to interface the floppy-disk controller to the DMA controller IC. Thus, the file processor only needs to load the command into the floppy disk controller after which the data transfer occurs under control of the disk controller and the DMA controller. The floppy disk controller is capable of multisector transfers.

Fifteen commands can be executed by the floppy disk controller including the basic read, write, scan,

format, seek, recalibrate, sense status, and their variations. Refer to the **NEC Data Handbook** for details on each command.

The floppy disk controller contains a status register and a data register that may be accessed by the file processor. The eight-bit status register may be read at any time. The data register consists of a stack of 8-bit registers, only one of which can be latched to the bus at one time.

The track stepping rate, head load time, and head unload time are not programmable in this application but are hardwired into the controller circuitry.

The data record length (sector size) used in this application is 512 bytes. See Chapter 4 for additional details on the floppy disk format.

See Tables 3-28 and 3-29 for the floppy disk controller port and bit assignments. Refer to the **NEC Data Handbook** for details on the NEC uPD765 floppy disk controller.

Refer to **Timing Diagrams** at the back of the previous file processor PCB section for data transfer between system memory and floppy disk controller timing.

Table 3-28. Floppy Disk Controller Port Assignments

Address	R/W	Description
0012	R/W	Data register
0020	W	Floppy disk control register

Table 3-29. Floppy Disk Control-Register Bit Assignments

Bit	Signal	Description
BDØ	PLCT	Write precompensation enable. Allows file processor to write precompensation on all floppy tracks. (Floppy controller IC must be disabled during this operation)
BDl	SOFT READY	Soft ready. Floppy disk drive will not go ready without a disk installed and drive motor turned on. Soft ready makes floppy drive appear ready so that drive can be recalibrated
BD2	--------	Not used
BD3	QDEN	Quad density enable. When low, selects normal recording (720K bytes per disk). When high, selects high density recording (1.2M bytes per disk)
BD4	MOTOR ON	Turn on motor. 500 milli-seconds after this signal is true, floppy disk can be read or written. Signal is deactivated if no commands have been sent to the floppy for 10 seconds (increases motor life)
BD5	--------	Not used
BD6	--------	Not used
BD7	INUSE	In use. If floppy drive jumper is in place, this signal lights the activity LED on the floppy drive

Tape Controller

The tape controller contains an Intel 8031 eight-bit microcomputer and 8K bytes of external PROM to perform tape reads, writes, and movement commands.

The tape controller communicates on one side with the file processor through an interface similar to the standard QIC-02 and on the other side with the streaming tape drive through a QIC-36 interface. (See Chapter 1 for a list of the related publications that describe the QIC interfaces.) The QIC-02-type interface is asynchronous and provides handshaking with a minimum number of control lines.

When the file processor is ready to write data on the tape, it begins transferring the data in 512 byte blocks via the DMA controller. (The tape controller has three 512 byte buffers for temporary storage.) When the first of the three buffers is filled, the tape controller simultaneously starts tape motion, begins writing to the tape, and accepts data for the second and third buffers. The data is written on the tape one track at a time in bit-serial format.

The controller writes a gap and sync mark preceding each 512-byte block of user data. After writing the data block, the tape controller records a one-byte block address, which indicates the number of the block. The address is incremented by one after each block of data. The controller writes the cyclical redundancy check (CRC) character following the block address. The process is repeated for each block of data to be written. (If the data blocks are written to the tape without stopping the tape drive, the method is called streaming tape operation.)

Seven 8-bit commands can be programmed into the tape controller command register by the file processor as described in Table 3-31. The three most significant bits, 7, 6, and 5 define the type of command. Bits 4, 3, 2, 1, and 0 contain the command bits. See Table 3-31 for the tape controller bit assignments.

Refer to **Timing Diagrams** in the back of the previous file processor PCB section for data transfer between system memory and tape controller timing.

Table 3-30. Tape-Controller Port Assignments

Address (Hex)	R/W	Description
0030	R	Tape status port
	W	Tape command register
0040	W	Tape control register
0050	R	Controller PCB status port

Table 3-31. Tape-Controller Bit Assignments

Bit	Signal	Description
		Tape Control Register
BD0	TREQUEST	Tape request. File processor request to tape controller indicating that a command is on data bus in command mode or that status was taken from data bus in status input mode. TREQUEST is asserted only when TRDY or TEXCEPT is asserted by tape controller
BD1	TDMA	Tape DMA. When asserted, enables data transfer between tape controller and file processor. When not asserted, blocks data transfer
BD2	TWR	Tape write. Enables data path for writing on tape and initiates first data byte request
BD3	ENRDYINT	Enable tape ready interrupt. Allows tape ready to cause an interrupt

Table 3-31. Tape-Controller Bit Assignments (Cont.)

Bit	Signal	Description
BD4*	TRESET*	Tape reset not. When low, resets tape controller
BD5	THD	Threshold. When asserted, invokes 35% qualifying amplitude threshold for read
BD6	--------	Not used
BD7	--------	Not used
		Controller PCB Status Port
BDØ	TEXCEPT	Tape except. Indicates an exception condition exists in the tape controller. 8Ø86 must issue status command and perform status input to determine cause
BDl	TRDY	Tape ready. Tape controller reports one of the following: 1. Data has been taken from the data bus in command transfer mode 2. Data has been placed on the data bus in status input mode 3. A BOT, cartridge initialization, or erase command is completed after being issued

Table 3-31. Tape-Controller Bit Assignments (Cont.)

Bit	Signal	Description
		Controller PCB Status Port (Cont.)
		4. Device is ready to receive the next block or ready to receive a write or WFM command from the host in write mode 5. WFM command is completed in write file mark mode 6. Device is ready to transmit the next block to the host or ready to receive a read or REM command from the host in read mode 7. Otherwise, device is ready to receive a new command
BD2	TDIR	Tape direction. When asserted, tape controller selected data path direction is from controller to file processor PCB. When not asserted, data transfer direction is from file processor PCB to controller
BD3	DRIVE SELD1	Drive 1 selected. Not used for tape drive - see Table 3-27
BD4	DRIVE SELD2	Drive 2 selected. Not used for tape drive - see Table 3-27

Table 3-31. Tape-Controller Bit Assignments (Cont.)

Bit	Signal	Description
		Controller PCB Status Port (Cont.)
BD5	DRIVE SELD3	Drive 3 selected. Not used for tape drive - see Table 3-27
BD6	GND	Always low
BD7	SELD	Tape drive select

The tape controller will accept a command when the tape ready bit is high. The read status command will be accepted when the tape ready bit is low provided the tape-except bit is also low. This allows the file processor to read the tape-controller status when there is an error condition. The on-line command is always high and forces the tape controller to remain on-line at all times.

CHAPTER 4
MAINTENANCE

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INTRODUCTION

This chapter includes the procedure for converting the 1086/2086 to 115 or 230 VAC nominal line voltage operation, and procedures for performing preventive and corrective maintenance. Also included are instructions for shipping field replaceable units to the factory for service or replacement.

Preventive maintenance consists of cleaning the dust filters, the cabinet exterior, the interior electrical components, and the cartridge tape and floppy disk drives. Corrective maintenance consists of removal/ replacement procedures for the field replaceable units (FRUs).

NOTE

Altos recommends that the procedures in this chapter be performed by qualified service personnel.

SELECTING 115/230 VAC OPERATION

Perform the following procedure to select 115 or 230 VAC operation for the 1086/2086. Converting to 115 or 230 VAC nominal operation requires a jumper change to the main power supply and a switch change to the hard disk drive(s).

1. Turn off the 1086/2086 power and unplug the AC power cord. (See **Controls, Connectors, and Indicators** in Chapter 1 for the locations of the power switch and power cord connectors.)

2. Remove the front panel as described under **Corrective Maintenance.**

3. Remove the right-hand side panel as described under **Corrective Maintenance.**

4. Connect the main power supply line-voltage jumper to select 115 or 230 VAC nominal operation as shown in Figure 4-1.

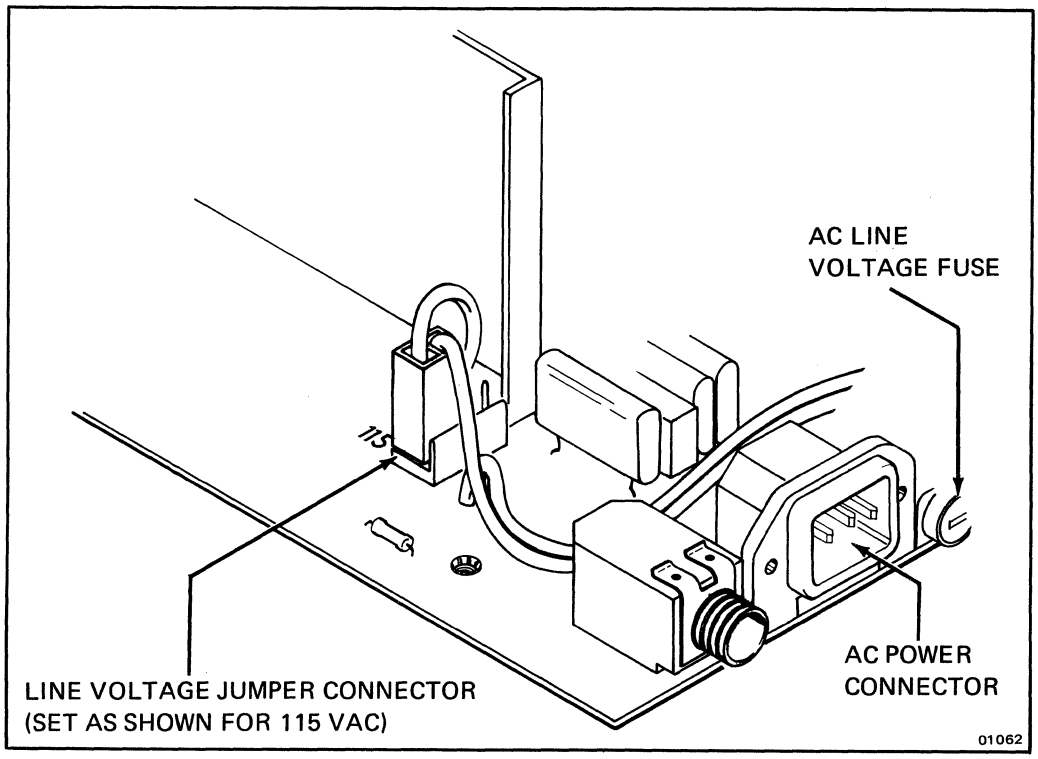

Figure 4-1. 115/230 VAC Selection (Main Power Supply)

5. Remove the hard disk drive(s) as described under **Corrective Maintenance.**

6. Set the power supply line-voltage selector switch for 115 or 230 VAC operation as shown in Figure 4-2.

7. Replace the AC line voltage fuse with the proper fuse for 115 or 230 VAC operation. Refer to Chapter 2 for the proper fuse rating.

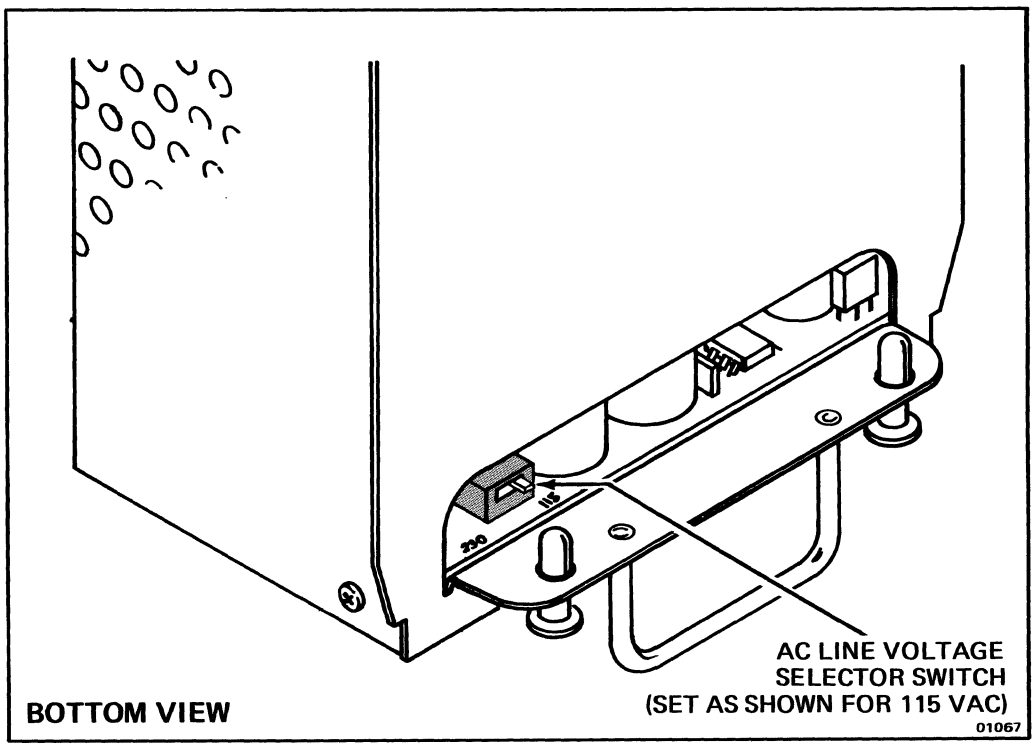

Figure 4-2. 115/230 VAC Selection (Hard Disk Drive)

PREVENTIVE MAINTENANCE

To assure maximum trouble-free operation, regular preventive maintenance should be performed. Dust accumulation on the electrical components can act as a heat-insulating blanket or create an electrical conduction path that can cause component failure. A coating of dust and tape particles can accumulate on the tape heads and cause faulty tape operation. The clock battery on the CPU PCB can lose power and cause faulty clock operation.

The following preventive maintenance should be performed at the specified intervals:

- dust filters should be cleaned at least every three months

- cartridge tape heads should be cleaned after initial pass of a new cartridge or each eight hours of tape contact
- interior electrical components should be visually inspected and cleaned at least every six months or as often as operating conditions require
- floppy disk head assembly should be cleaned and belts checked every twelve months
- clock battery should be replaced every 36 months

WARNING

Dangerous potentials exist inside the cabinet. Turn off the 1086/2086 power and unplug the AC power cord before performing the following preventive maintenance procedures.

Cleaning

Perform the following procedures to clean the filters, the exterior and interior components, and the cartridge tape and floppy disk heads. Altos does not recommend that the hard disk drive(s) be removed or disassembled for cleaning.

CAUTION

Do not use chemical or abrasive cleaning agents that can damage the plastics used in the component parts of the system.

Dust Filters

A #1 or #2 Phillips screwdriver and some mild household detergent are required to clean the dust filters.

(Order an extra set of filters so you always have clean filters available.)

Perform the following procedure to remove and clean the dust filters (see Figures 4-3 and 4-4):

1. Turn off the 1086/2086 power and unplug the AC power cord. (See **Controls, Connectors, and Indicators** in Chapter 1 for the locations of the power switch and power cord connector.)

2. Remove the cabinet front panel as described under **Corrective Maintenance.**

3. Grasp one corner of the filter located behind the front panel and pull it toward you until all velcro pads are released.

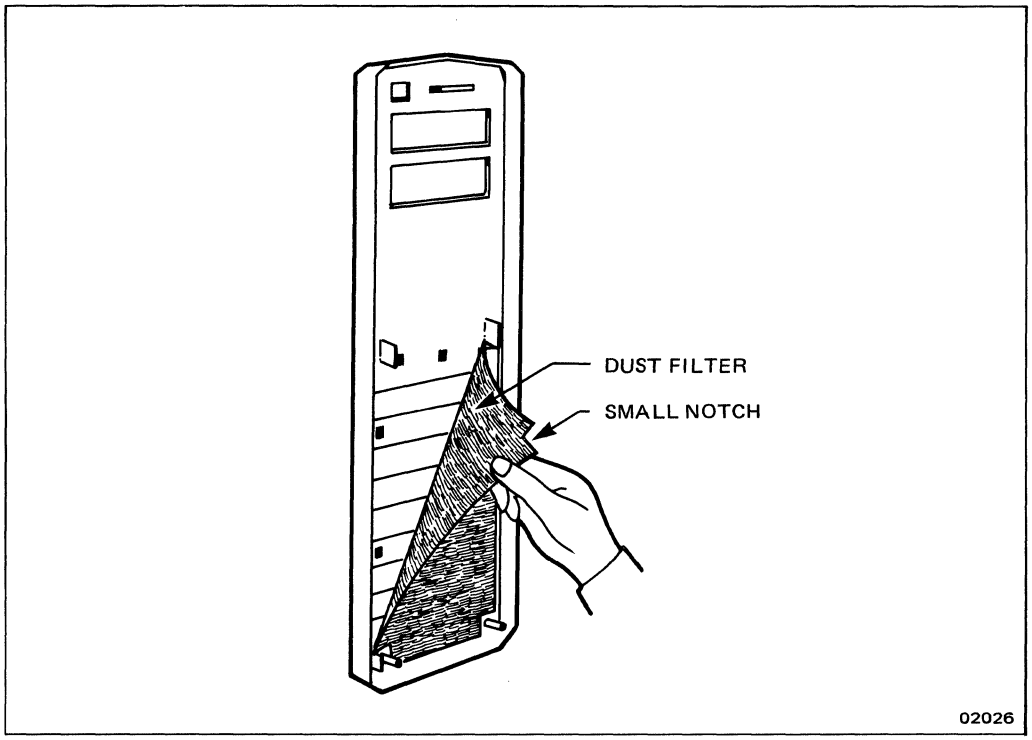

Figure 4-3. Removing/Replacing the Front Panel Filter

4. Pull the filter located under the bottom hard disk drive toward you until it comes completely out of the chassis.

NOTE

Early models of the 1086/2086 do not have a filter under the bottom hard disk drive. Instead, a filter is attached to the inside bottom of each side panel with velcro pads. Remove the side panels as described under **Corrective Maintenance.** Remove the filters as described in step 3 and clean them as described in step 5.

5. Clean the filters by soaking them in a mild solution of water and household detergent. Rinse them thoroughly with clean water. Gently pat the filters with a dry towel to remove excess water, but do not twist or bend them.

CAUTION

Let the filters dry for at least six hours before replacing them in the chassis. Never install damp filters in the cabinet!

6. Replace the front filter with the smooth side up. Press firmly on the velcro pads to secure the filter. Slide the bottom filter into its rails at the bottom of the chassis.

7. Replace the front panel in the reverse order of removal.

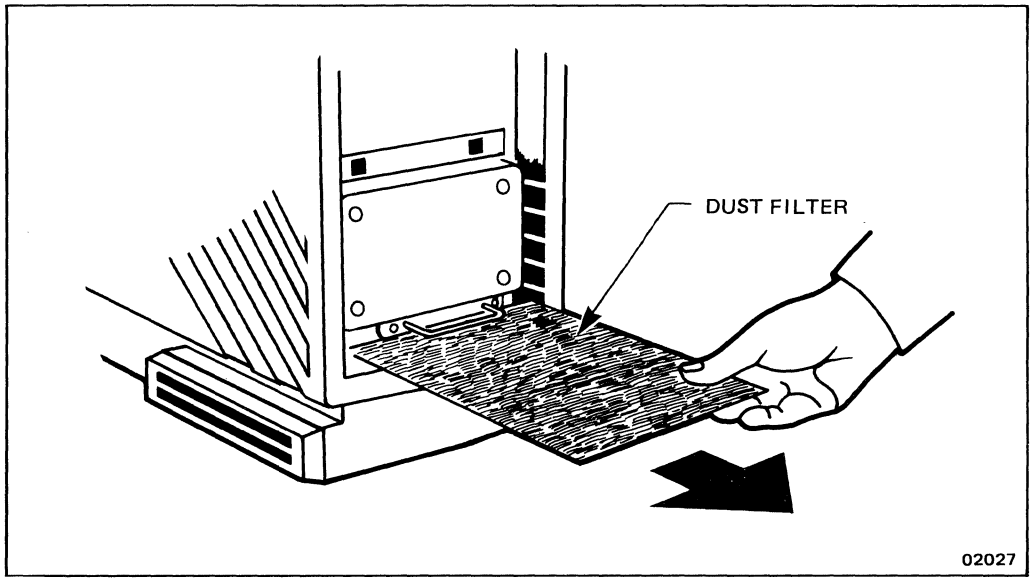

Figure 4-4. Removing/Replacing the Bottom Filter

Tape Heads

The cartridge tape drive read/write/erase heads should be cleaned and the soft error statistics checked to determine tape or tape drive deterioration after every eight hours of actual tape motion. Read or write error statistics are available to the operating system through the Read Status command. The Read Status command should be executed after each cartridge is used. Refer to Appendix B for additional information on tape commands.

The drive should also be cleaned after an initial pass of a new cartridge or, if only new cartridges are used, after every eight hours of tape motion.

The recommended method for cleaning is to use a cartridge cleaner kit, available from electronics suppliers. An alternative method is to gently wipe the head area with a six-inch long cotton swab lightly dipped in a 95% isopropyl alcohol solution or standard tape head cleaning solution (Miller-Stephenson MS-200 or equivalent).

While this alternative method is acceptable when a cleaning cartridge is not available, it is more likely to leave an unwanted residue in the head area. Ensure that drive power is off when applying an alcohol or head cleaning solution.

Perform the following procedure to clean the tape heads (see Figure 4-5):

1. Remove the tape cartridge from the drive by moving the lever to the left. If your drive does not have a lever, press in on the cartridge to release the tape.

2. Expose the tape heads by pressing the tape lever to the right, if you have a lever-style drive. If you do not have a lever, press in firmly on the plate at the bottom of the tape slot. When you press in on the bottom plate, the tape head assembly pops out.

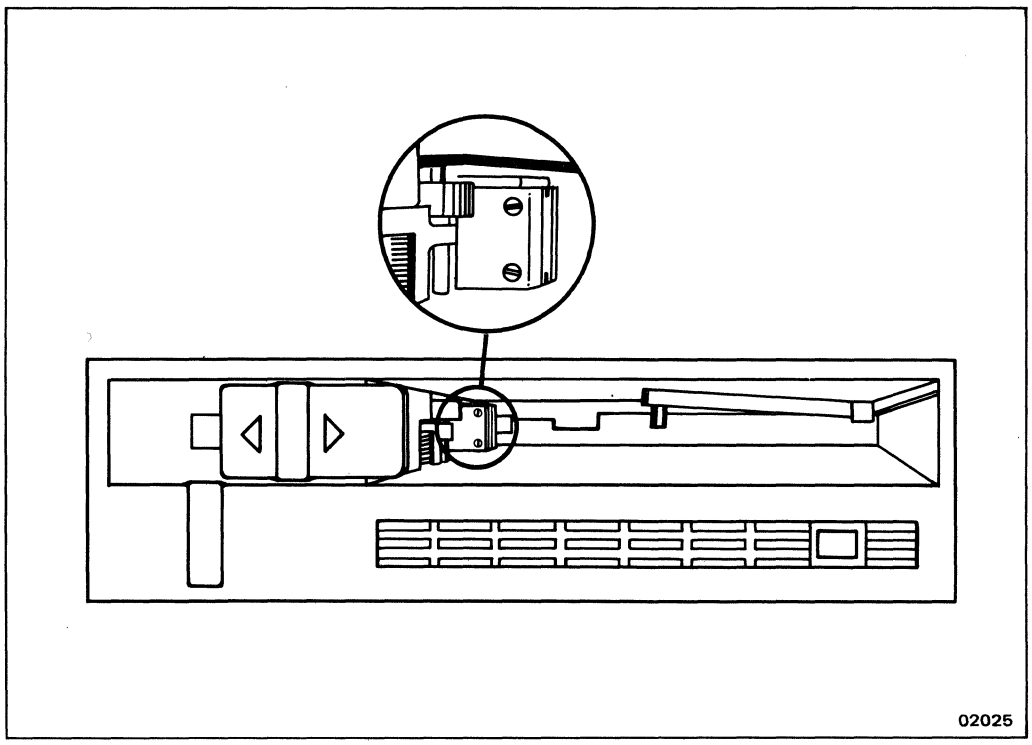

Figure 4-5. Cleaning the Tape Head

3. Dip the cotton swab in the cleaning solution.

4. Gently wipe the brass and porcelain parts of the head assembly.

5. Use a dry swab to wipe off any excess solution.

CAUTION

Make sure you allow the heads to dry completely before using the tape drive.

6. If you have a lever-type unit, move the lever to the left. If you pressed in on the bottom plate to expose the tape heads, press in on the plate again until it clicks back into place.

Floppy Disk Drive

The floppy disk drive belt and disk head drive should be checked and the head and pressure pad assembly cleaned every 12 months in average use and dust environments. The frequency of preventive maintenance depends entirely on the amount of use and, most important, on the amount of dust in the operating environment. The head and pressure pad assembly are the most critical parts to maintain.

A cleaning disk for floppy disk drives is the recommended method for cleaning the head and pressure pad assembly. If read/write problems persist, it may be necessary to remove and disassemble the drive, clean the head, and replace the pressure pad. **(This should only be done by qualified service personnel.)** Refer to the appropriate floppy disk drive service manual for detailed procedures.

Check the belt for excessive wear and the disk head drive assembly for proper alignment. Head alignment should only be attempted by qualified service personnel. Refer to the appropriate floppy disk drive service amnual for detailed procedures.

Exterior

Use a soft-bristled brush or soft cloth to remove loose dust or foreign material from the side panels and exterior of the cabinet.

Stubborn dirt can be removed with a soft cloth dampened with a mild solution of non-abrasive household detergent and water.

Interior

Check the interior of the cabinet for dust or dirt accumulation (especially on the electrical components). If there is visible dust or dirt accumulation on the interior components, clean as described in the following procedure:

1. Turn off the 1086/2086 power and unplug the AC power cord. (See **Controls, Connectors, and Indicators** in Chapter 1 for the locations of the power switch and power cord connector.)

2. If applicable, remove the cabinet side panels as described under **Corrective Maintenance.**

3. Remove the printed circuit boards (PCBs) as described under **Corrective Maintenance.**

4. Use low-velocity air (approximately 5 psi) or a soft-bristled brush to remove loose dust from the interior of the cabinet and from the PCBs.

   A cotton-tipped applicator is useful for cleaning in narrow spaces. Be careful when cleaning around electrical components.

5. Replace the PCBs and side panels in the reverse order of removal.

CORRECTIVE MAINTENANCE

Corrective maintenance information in this section includes removal and replacement procedures for the field replaceable units. Refer to Chapter 1 for a description of the field replaceable units.

WARNING

Dangerous potentials exist inside the cabinet. Turn off the 1086/2086 AC power and unplug the AC power cord before performing the following procedures.

NOTE

Altos recommends that the following procedures be performed by qualified service personnel.

Removal and Replacement

The following procedures describe how to remove and replace field replaceable units. If a field replaceable unit is to be shipped for repair or replacement, refer to **Shipping a Field Replaceable Unit** at the back of this chapter.

Removing the Front Panel

Perform the following procedure to remove/replace the front panel (see Figure 4-6):

1. Turn off the 1086/2086 power and unplug the AC power cord. (See **Controls, Connectors, and Indicators** in Chapter 1 for the locations of the power switch and power cord connector.)

2. Use a #2 Phillips screwdriver to turn the two fasteners on the bottom of the front panel 1/4-turn counterclockwise.

3. Gently pull the bottom of the front panel about two inches away from the cabinet.

4. Push the front panel up to disengage the retaining hook at the top. Then, pull the front panel toward you to free the front panel from the cabinet.

5. Replace the front panel by inserting the retaining hook into the slot at the top of the front panel and pivoting the panel down into position.

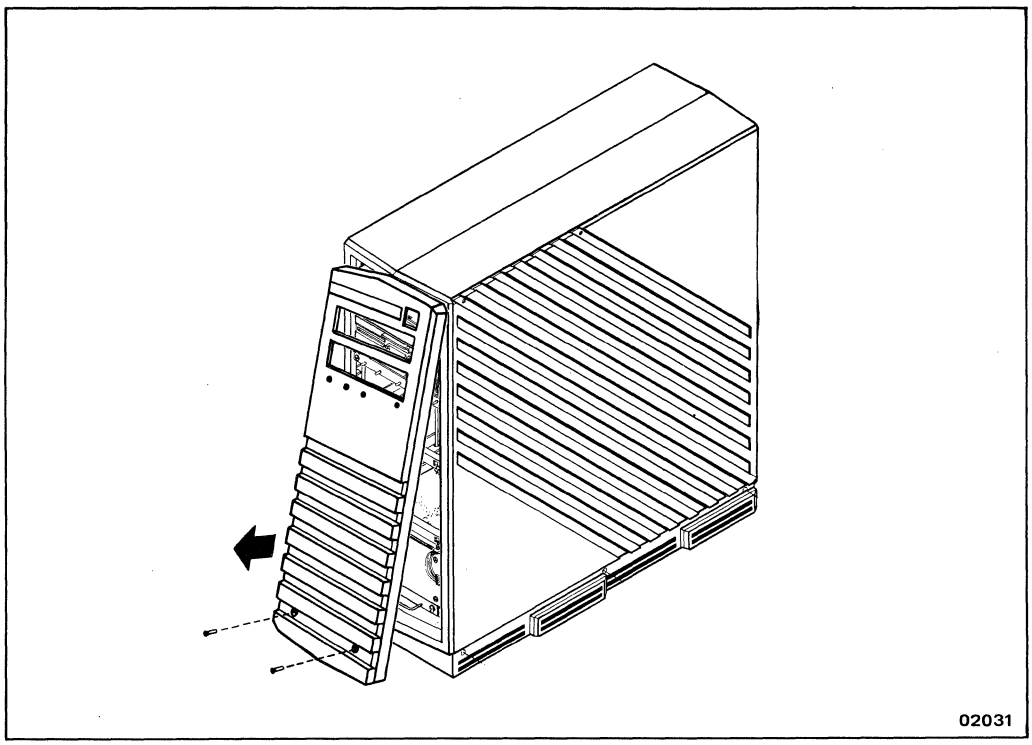

Figure 4-6. Removing/Replacing the Front Panel

Removing the Side Panels

Perform the following procedure to remove/replace the cabinet side panels (see Figure 4-7):

1. Turn off the 1086/2086 power and unplug the AC power cord. (See **Controls, Connectors, and Indicators** in Chapter 1 for the locations of the power switch and power cord connector.)

2. Remove the front panel as described previously.

3. Use a #2 Phillips screwdriver to remove the two screws on the top and three screws on the bottom securing the left and right side panels to the chassis.

4. Gently remove the side panel from the chassis.

5. Replace the side panels in the reverse order of removal.

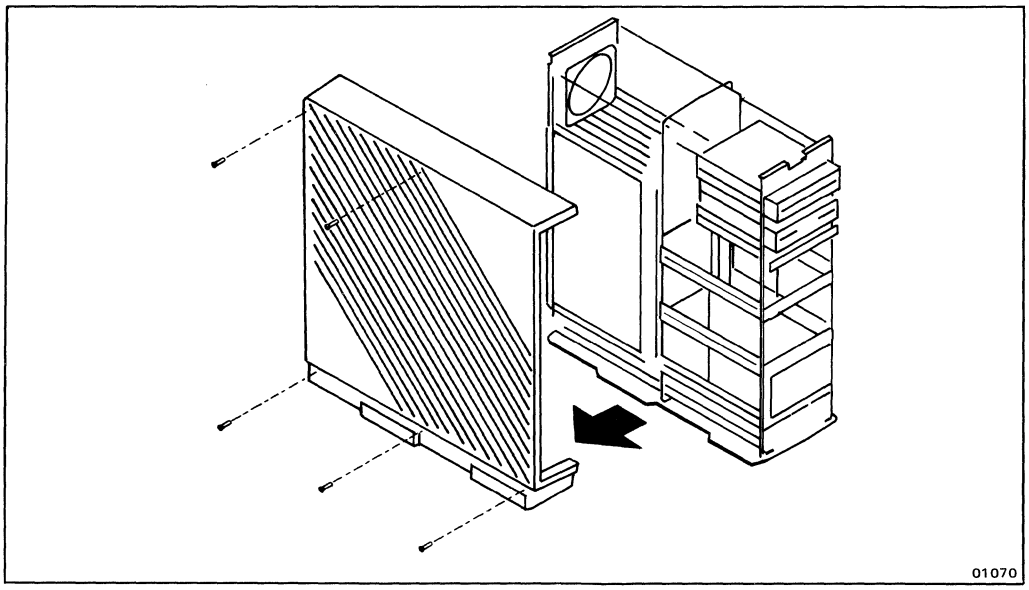

Figure 4-7. Removing/Replacing the Side Panels

Removing the Tape Drive

Perform the following procedure to remove the cartridge-tape drive (see Figures 4-8 and 4-9):

1. Turn off the 1086/2086 power and unplug the AC power cord. (See **Controls, Connectors, and Indicators** in Chapter 1 for the locations of the power switch and power cord connector.)

2. Remove the front panel as described previously.

3. Use a #2 Phillips screwdriver to turn the screw on the drive mounting bracket a quarter-turn counterclockwise as shown in Figure 4-8.

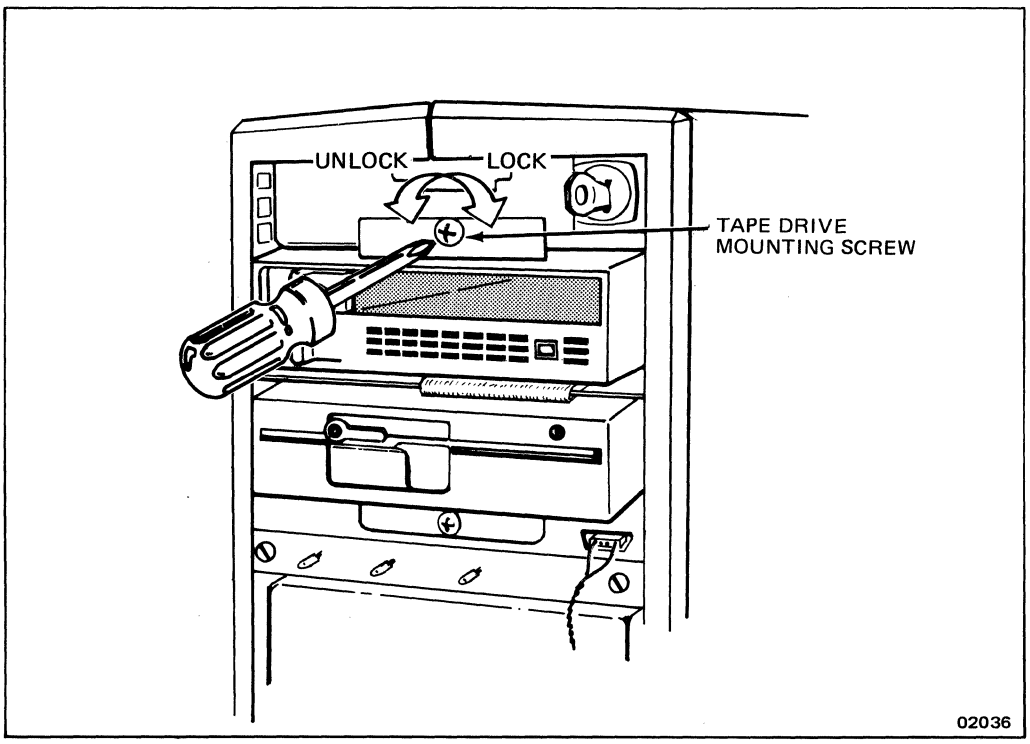

Figure 4-8. Locking/Unlocking the Tape Drive Mounting Screw

4. Slide the tape drive out of the chassis. Notice the two cables connected to the back of the drive and the steel dust cover that protects the cables as shown in Figure 4-9.

5. Remove the dust cover by popping one side out of the grooves.

6. Unplug the two cables and set the drive on a flat surface. **Do not remove the cables from the cabinet.**

7. Replace the tape drive as described in the following procedure.

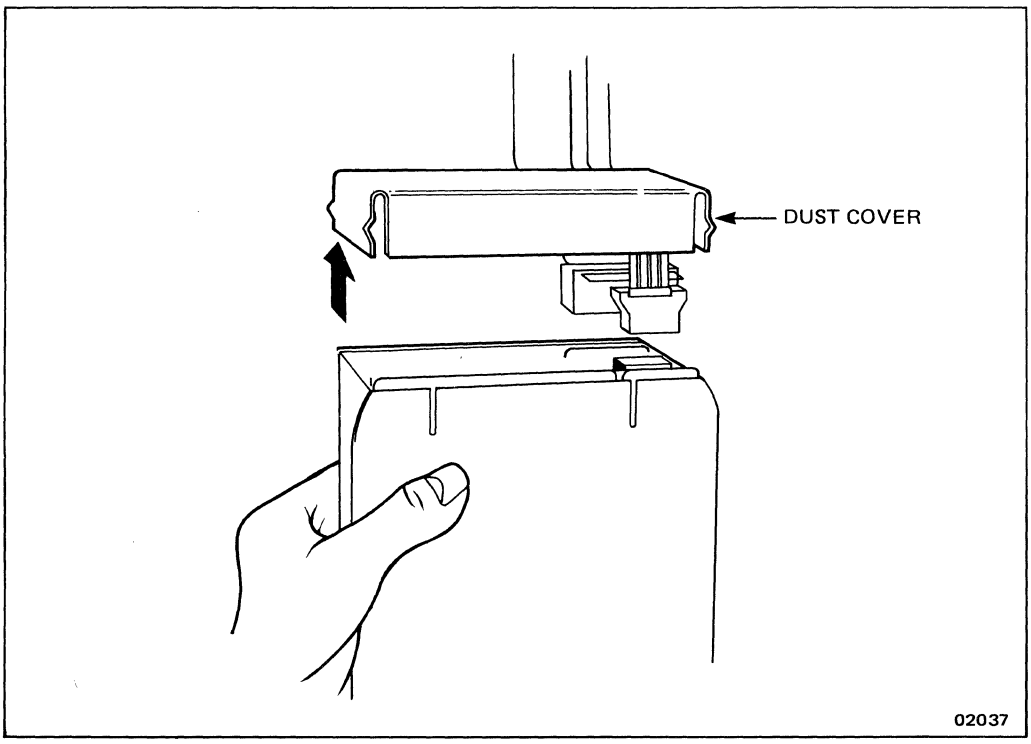

Figure 4-9. Removing/Replacing the Tape Drive

Replacing the Tape Drive

Perform the following procedure to replace the cartridge-tape drive (see Figures 4-8 and 4-9):

1. Turn off the 1086/2086 power and unplug the AC power cord. (See **Controls, Connectors, and Indicators** in Chapter 1 for the locations of the power switch and power cord connector.)

2. Position the tape drive with the mounting bracket facing up.

3. Connect the 4-pin power cable connector to the corresponding connector on the back of the drive. (The connector is keyed for the proper orientation.) Be careful not to damage the yellow capacitor on the cable.

4. Connect the 57-pin connector to the corresponding connector on the back of the drive as shown in Figure 4-9. Do not twist the cable -- keep the red cable stripe to your right as you face the back of the system.

5. Install the steel dust cover by placing one end into the grooves at the cable end and pulling the other end over until it pops into place.

6. Slide the drive into the chassis. Guide the cables back into the chassis as you slide the drive into the slot.

7. Gently press the drive until it seats firmly in the chassis.

8. Use a #2 Phillips screwdriver to press in and turn the locking screw a quarter-turn clockwise as shown in Figure 4-8.

9. Replace the front panel in the reverse order of removal.

Removing the Floppy Drive

Perform the following procedure to remove the floppy disk drive (see Figures 4-10 and 4-11):

1. Turn off the 1086/2086 power and unplug the AC power cord. (See **Controls, Connectors, and Indicators** in Chapter 1 for the locations of the power switch and power cord connector.)

2. Remove the front panel as described previously.

3. Use a #2 Phillips screwdriver to turn the screw on the drive mounting bracket a 1/4-turn counterclockwise as shown in Figure 4-10.

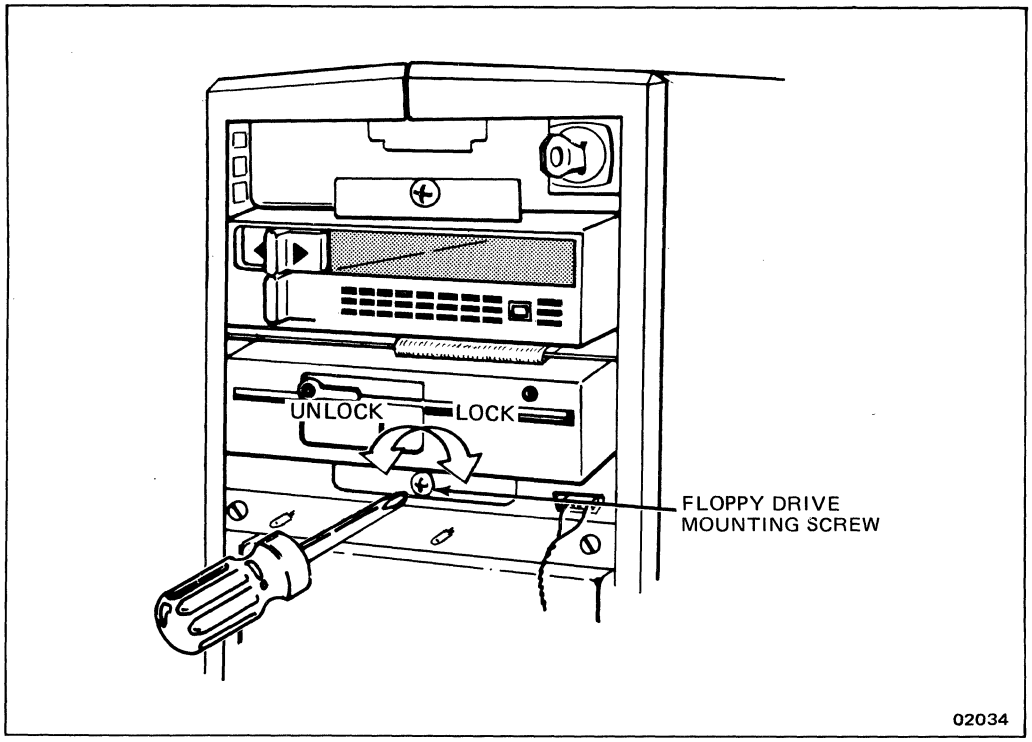

Figure 4-10. Locking/Unlocking the Floppy Drive Mounting Screw

4. Slide the floppy drive out of the chassis. Notice the two cables connected to the back of the drive and the steel dust cover that protects the cables as shown in Figure 4-11.

5. Remove the dust cover by popping one side out of the grooves.

6. Unplug the two cables and set the drive on a flat surface. **Do not remove the cables from the cabinet.**

7. Replace the floppy drive as described in the following procedure.

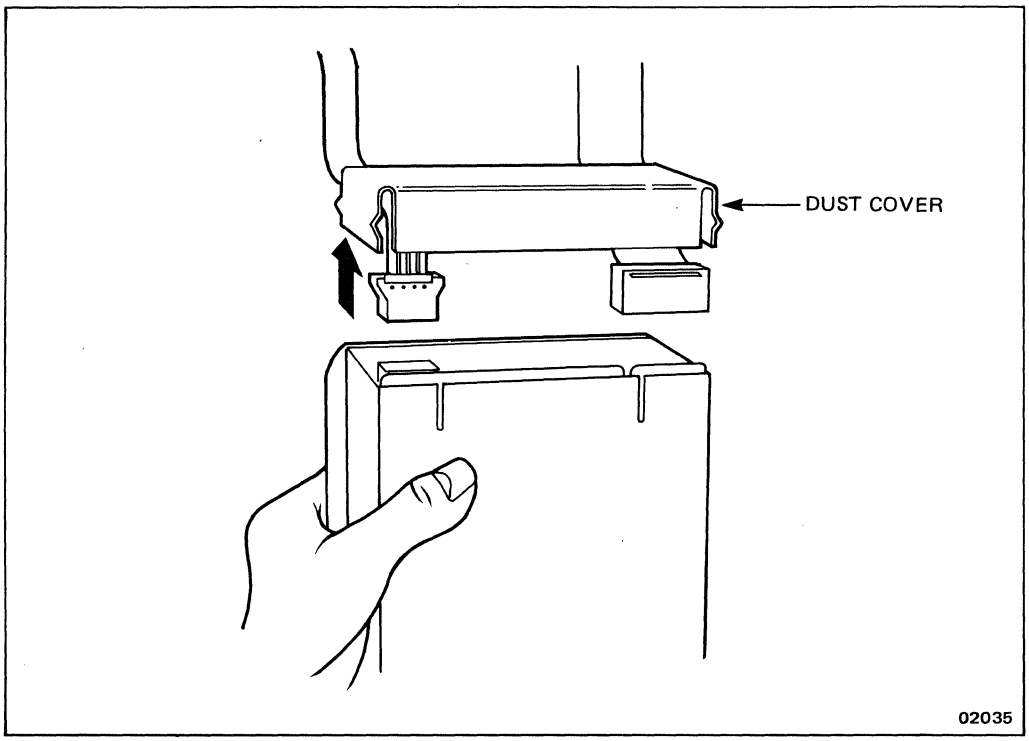

Figure 4-11. Removing/Replacing the Floppy Drive

Replacing the Floppy Drive

Perform the following procedure to replace the floppy disk drive (see Figures 4-10 and 4-11):

1. Turn off the 1086/2086 power and unplug the AC power cord. (See **Controls, Connectors, and Indicators** in Chapter 1 for the locations of the power switch and power cord connector.)

2. Position the floppy drive with the mounting bracket facing down.

3. Connect the 4-pin power cable connector to the corresponding connector on the back of the drive. (The connector is keyed for the proper orientation.)

4. Connect the 25-pin connector to the corresponding connector on the back of the drive as shown in Figure 4-11. Do not twist the cable -- keep the red cable stripe to your right as you face the back of the system.

5. Install the steel dust cover by placing one end into the grooves at the cable end and pulling the other end over until it pops into place.

6. Slide the drive into the chassis. Guide the cables back into the chassis as you slide the drive into the slot.

7. Gently press the drive until it seats firmly in the chassis.

8. Use a #2 Phillips screwdriver to press in and turn the locking screw a 1/4-turn clockwise as shown in Figure 4-10.

9. Replace the front panel in the reverse order of removal.

Removing the Hard Disk Drive

Perform the following procedure to remove the hard disk drive (see Figures 4-12 and 4-13):

1. Turn off the 1086/2086 power and unplug the AC power cord. (See **Controls, Connectors, and Indicators** in Chapter 1 for the locations of the power switch and power cord connector.)

2. Remove the front panel as described previously.

CAUTION

The hard disk drive is sensitive to shock and vibration. Do not drop or jar the drive. Wait at least 30 seconds after powering off the system before removing a hard disk drive.

3. Unplug the small AC connector located near the upper right corner of the hard disk drive by pressing down on the latch as shown in Figure 4-12.

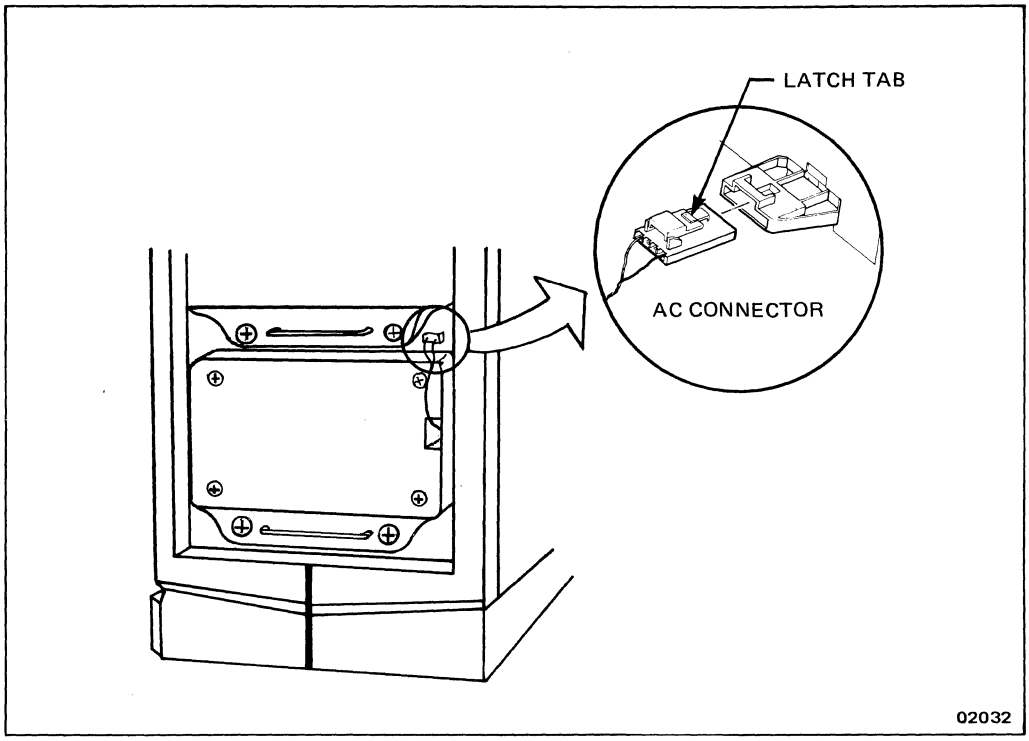

Figure 4-12. Removing/Replacing the Hard Disk AC Connector

4. Use a #2 Phillips screwdriver to turn the two screws on the drive mounting bracket a 1/4-turn counterclockwise as shown in Figure 4-13.

5. Grasp the handle and pull it toward you to slide the drive out of the chassis.

6. Replace the hard disk drive as described in the following procedure.

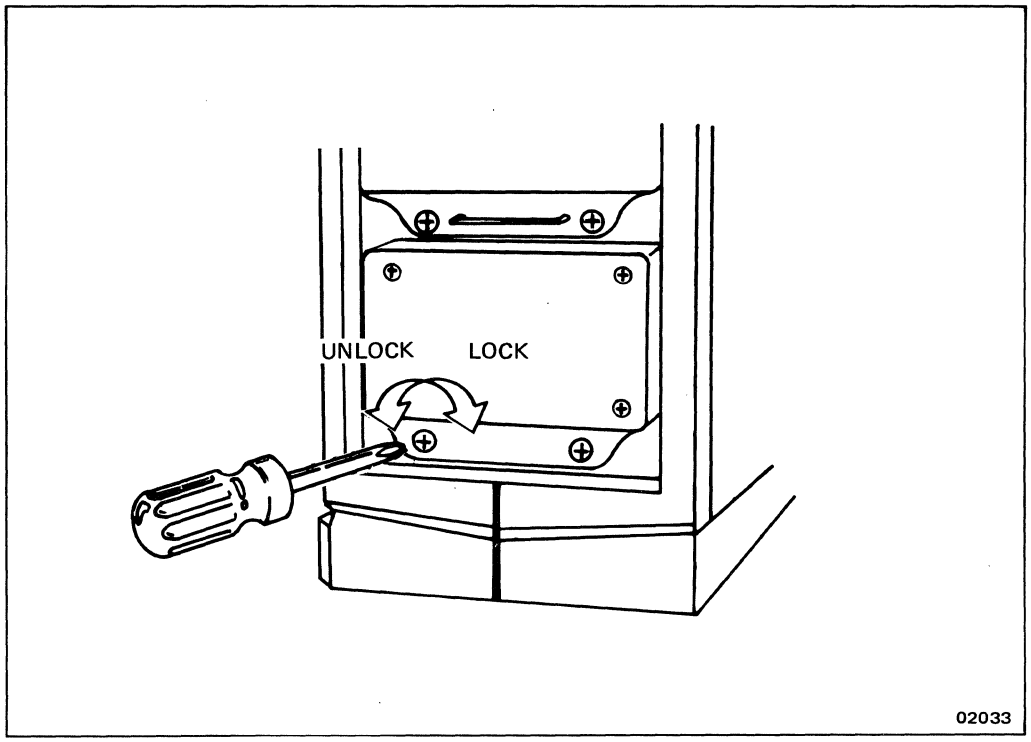

Figure 4-13. Unlocking/Locking the Hard Disk Drive Mounting Screws

Replacing a Hard Disk Drive

Perform the following procedure to replace a hard disk drive (see Figures 4-12 and 4-13):

1. Turn off the 1086/2086 power and unplug the AC power cord. (See **Controls, Connectors, and Indicators** in Chapter 1 for the locations of the power switch and power cord connector.)

2. Remove the front panel as described previously.

CAUTION

The hard disk drives are sensitive to shock and vibration. Do not drop or jar a drive. Wait at least 30 seconds after powering off the system before replacing a hard disk drive.

NOTE

Hard disk drives are installed from the bottom up. If there is one hard disk drive, install it in the bottom slot. If there are two hard disk drives, install them in the bottom two slots. If there are three hard disk drives, install one drive in each of the available hard disk slots.

3. Position the drive with the handle and mounting bracket on the bottom. Place the flanged sides of the drive into the grooves of the correct drive slot.

4. Press evenly against the front of the drive until it is completely seated in the slot.

5. Use a #2 Phillips screwdriver to turn the two screws on the mounting bracket a 1/4-turn clockwise as shown in Figure 4-13.

6. Plug the hard disk AC connector into the corresponding connector located in the upper right-hand corner of the drive slot as shown in Figure 4-12.

7. Replace the front panel in the reverse order of removal.

Removing the Plug-In Printed Circuit Boards

Perform the following procedure to remove/replace the plug-in PCBs (see Figure 4-14):

1. Turn off the 1Ø86/2Ø86 power and unplug the AC power cord. (See **Controls, Connectors, and Indicators** in Chapter 1 for the locations of the power switch and power cord connector.)

2. Grasp each PCB-extractor ring located at the bottom and top of the PCB.

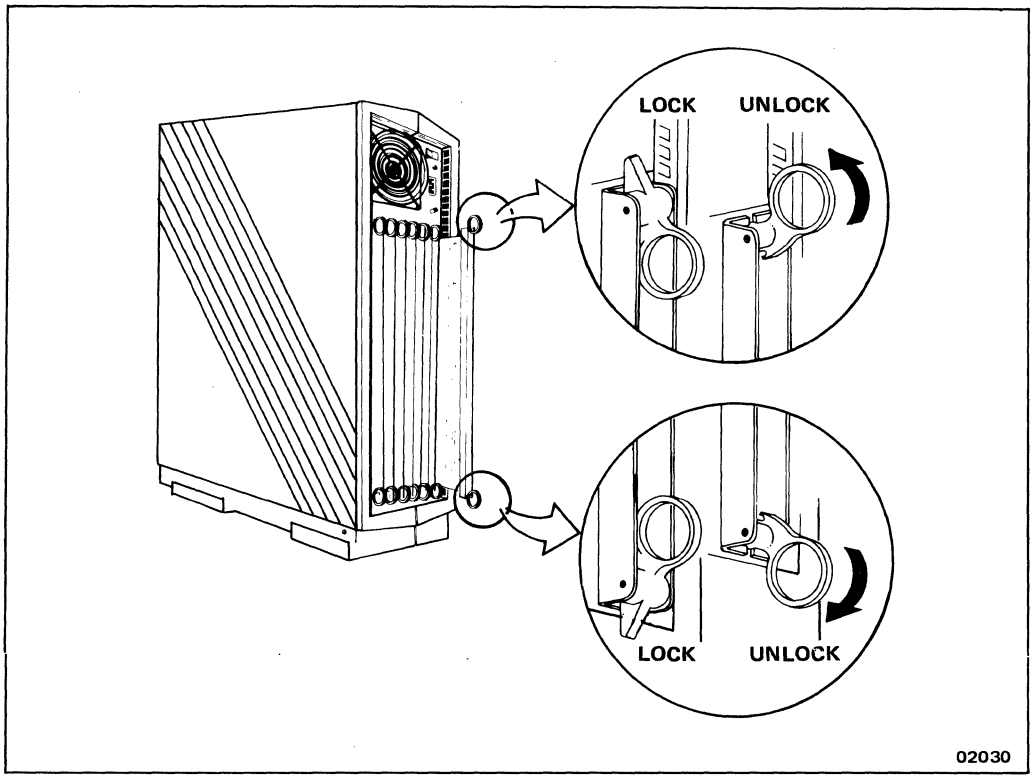

Figure 4-14. Removing/Replacing the Plug-In PCBs

3. Gently pull straight out on both extractor rings simultaneously and slide the PCB out of the chassis.

4. Replace the PCB by positioning both extractor rings straight out from the channel bracket. Slide the PCB part way into the appropriate slot and push firmly in the center of the channel bracket. The extractor rings should automatically lock the PCB in place. However, make sure that the PCBs are locked in place by pressing the extractor rings down tight against the PCB channel bracket.

Removing the Main Power Supply

Perform the following procedure to remove/replace the main power supply (see Figure 4-15):

1. Turn off the 1086/2086 power and unplug the AC power cord. (See **Controls, Connectors, and Indicators** in Chapter 1 for the locations of the power switch and power cord connector.)

2. Remove the front panel as described previously.

3. Remove the left-hand side panel as described previously.

4. Disconnect the power supply harness connector from the backplane PCB and the power connector from the fan. (If there are three hard disk drives installed, remove the top drive to gain access to the power supply harness connector.)

5. Use a #2 Phillips screwdriver to remove the four screws securing the main power supply PCB to the chassis as shown in Figure 4-15. (The power on/off switch, line-voltage receptacle, and fuse holder are removed with the power supply.)

6. Slide the power supply toward the front of the chassis, then tilt the back of the power supply up and remove.

7. Replace the main power supply PCB in the reverse order of removal. Make sure that the grounding washers are properly installed.

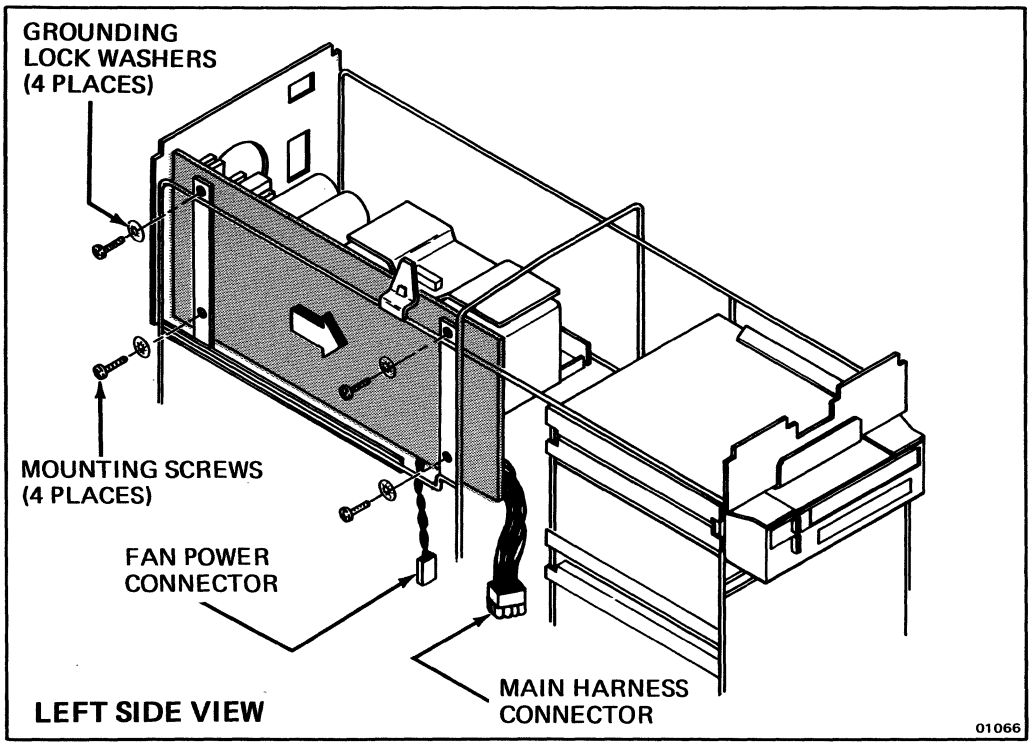

Figure 4-15. Removing/Replacing the Main Power Supply

Removing the Backplane PCB

Perform the following procedure to remove/replace the backplane PCB (see Figure 4-16 and 4-17):

1. Turn off the 1Ø86/2Ø86 power and unplug the AC power cord. (See **Controls, Connectors, and Indicators** in Chapter 1 for the locations of the power switch and power cord connector.)

2. Remove the front panel as described previously.

3. Remove the right-hand side panel as described previously.

4. Remove the cartridge tape, floppy, and hard disk drives as described previously.

5. Remove the plug-in PCBs as described previously.

6. Unplug the harness connectors from the backplane and, if applicable, from the low-pass filter PCB. (Early versions had a low-pass filter PCB mounted to the top of the backplane.)

7. Use a #2 Phillips screwdriver to remove the three top and three bottom screws and washers securing the backplane PCB with its mounting frame to the chassis as shown in Figure 4-16. (Early versions had a low-pass filter PCB attached to the backplane PCB with two of the top three screws.)

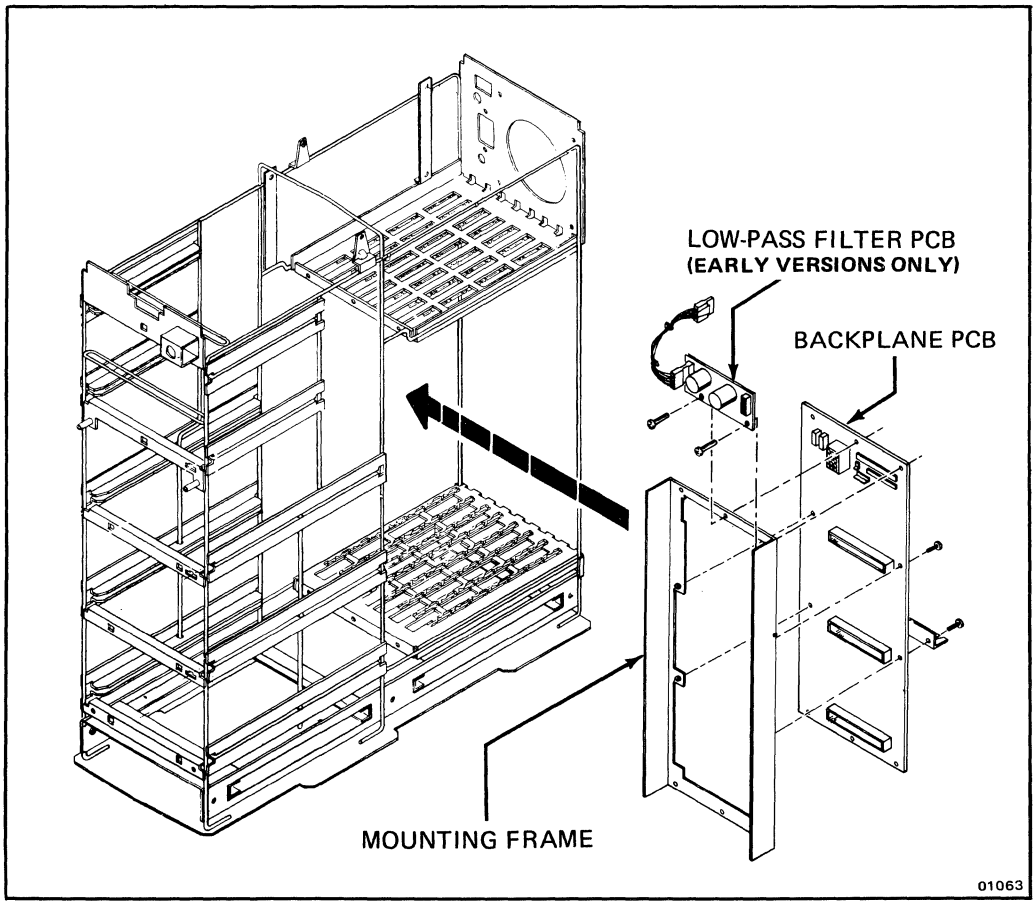

Figure 4-16. Removing/Replacing the Backplane PCB

8. Gently lift the backplane PCB up and slide it out from the right-hand side of the cabinet.

9. Use a #2 Phillips screwdriver to remove the four screws and washers securing the backplane PCB to the mounting frame.

10. Replace the backplane PCB in the reverse order of removal. Make sure that all the mounting washers are properly installed and that the harness connectors are attached to the proper backplane PCB connectors. Refer to Figure 4-18 for the proper cable connections to the backplane and low-pass filter PCBs.

Removing the Low-Pass Filter PCB (Early Version Only)

Perform the following procedure to remove/replace the low-pass filter PCB:

1. Turn off the 1086/2086 power and unplug the AC power cord. (See **Controls, Connectors, and Indicators** in Chapter 1 for the locations of the power switch and power cord connector.)

2. Remove the front panel as described previously.

3. Remove the right-hand side panel as described previously.

4. Disconnect the harness connectors from the low-pass filter PCB.

5. Use a #2 Phillips screwdriver to remove the two screws and washers securing the low-pass filter PCB to the top of the backplane PCB.

6. Replace the low-pass filter PCB in the reverse order of removal. Refer to Figure 4-18 for the proper cable connections to the low-pass filter PCB.

Removing the LED PCB

Perform the following procedure to remove/replace the light-emitting diode (LED) PCB:

1. Remove the front panel as described previously.

2. Disconnect the harness connector from the LED PCB.

3. Use a #2 Phillips screwdriver to remove the two screws securing the LED PCB to the chassis.

4. Replace the LED PCB in the reverse order of removal.

Removing the Clock Battery

Perform the following procedure to remove/replace the clock battery (see Figure 4-17):

1. Turn off the 1086/2086 power and unplug the AC power cord. (See **Controls, Connectors, and Indicators** in Chapter 1 for the locations of the power switch and power cord connector.)

2. Remove the CPU PCB as described previously.

CAUTION

Do not handle the clock battery with your bare hands. Use a cloth or paper towel. Moisture and oil residue from you skin can corrode the battery contact surfaces.

3. Gently pry up the retaining clip and remove the clock battery from the CPU PCB as shown in Figure 4-17.

4. Replace the clock battery (Altos part no. 183-12568-001) and CPU PCB in the reverse order of removal.

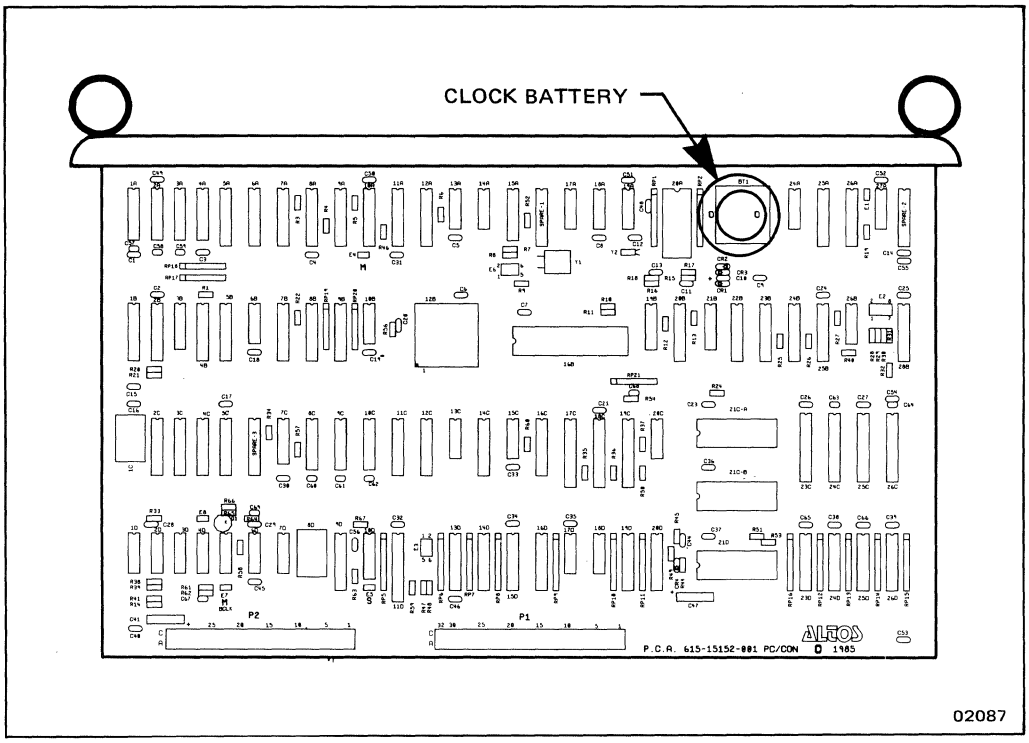

Figure 4-17. Removing/Replacing the Clock Battery

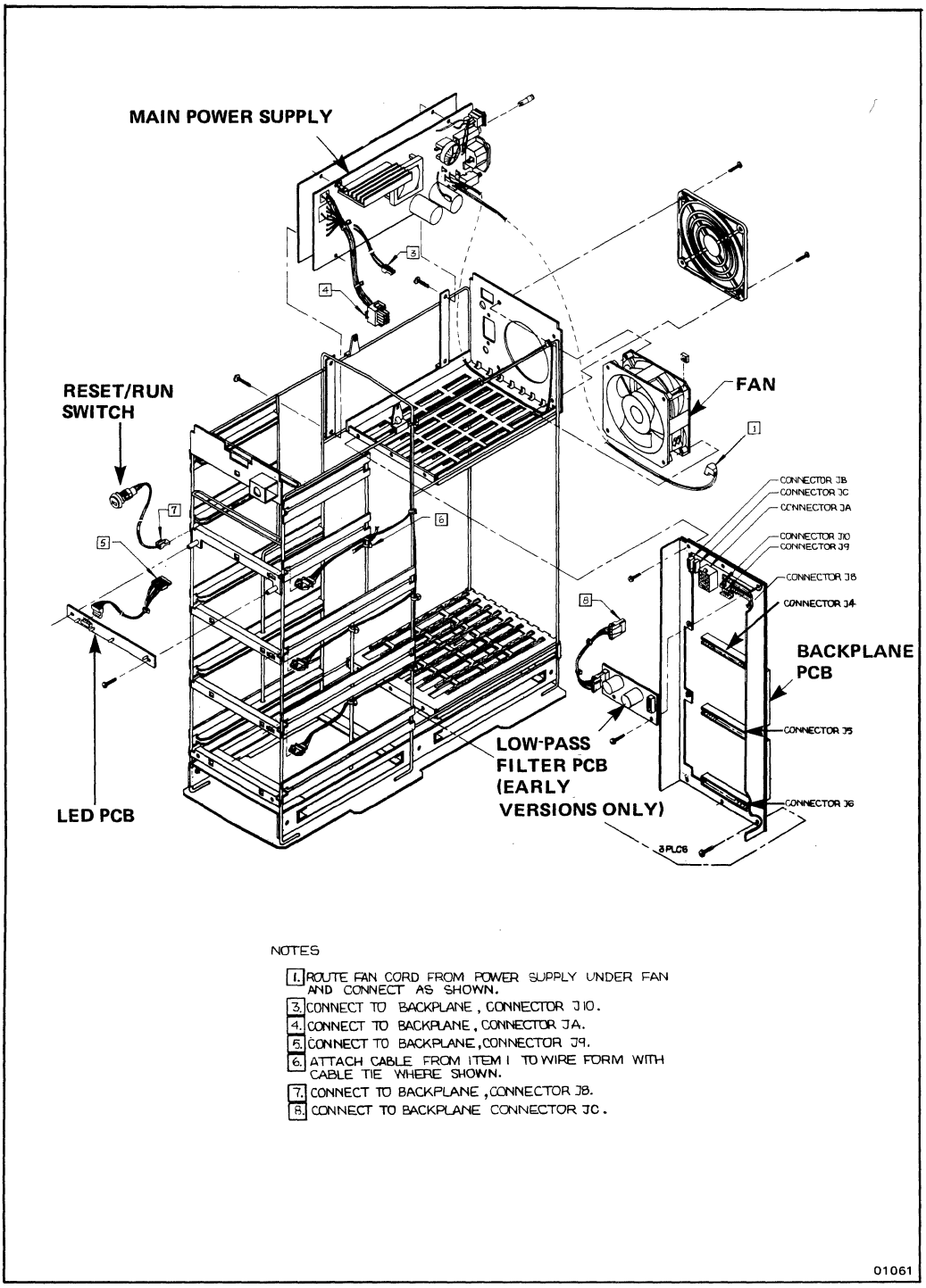

Figure 4-18. Cable Interconnections

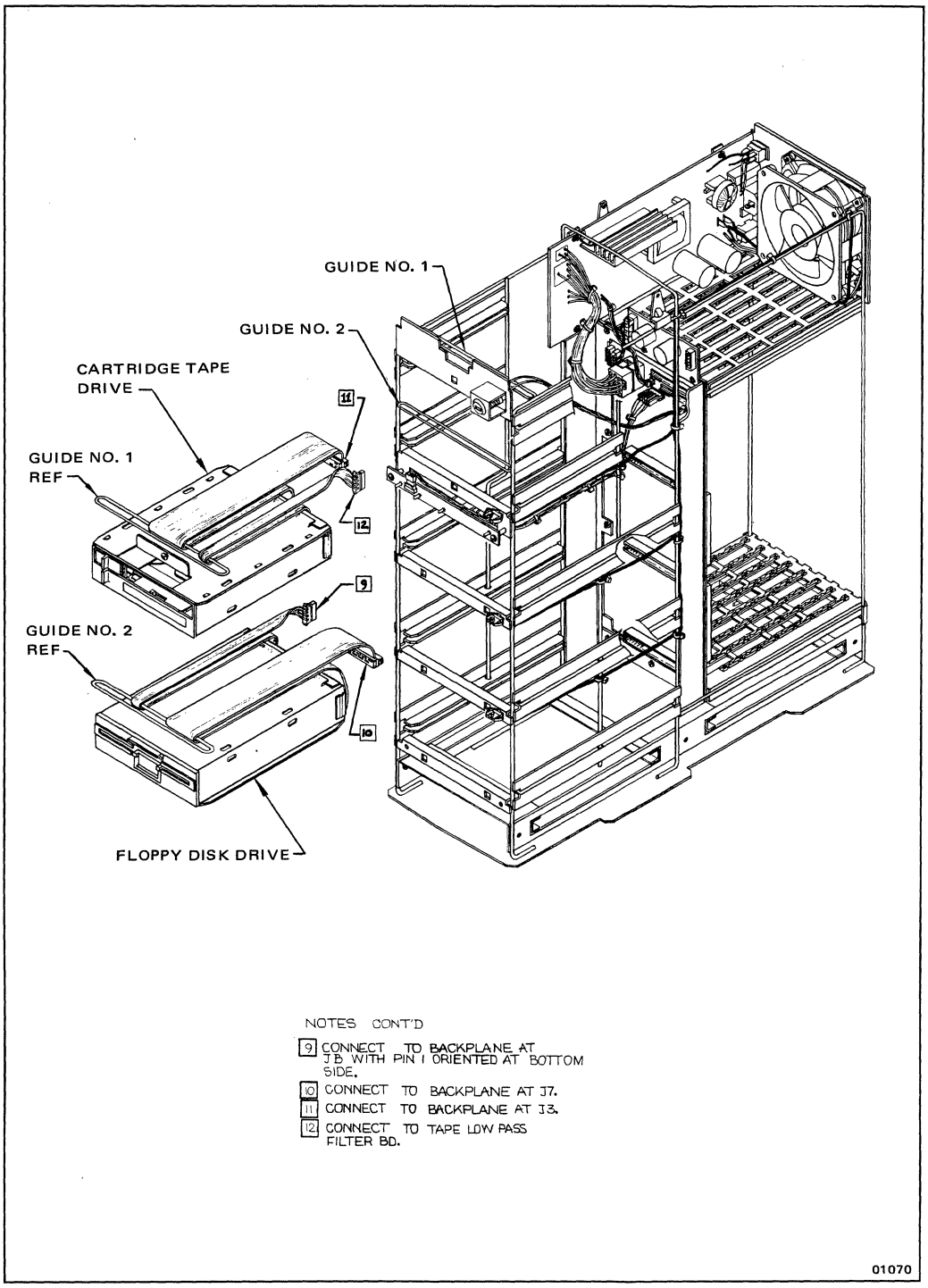

Figure 4-18. Cable Interconnections (Cont.)

SHIPPING A FIELD REPLACEABLE UNIT

Always contact Altos Customer Service before returning a unit for factory service. If service is required, a customer service technician will assign you a Return Authorization (RA) number.

Do not send in a unit for repair without an RA number. Also supply the following:

- model number of your system
- serial number of your system
- date purchased or sent for service
- specific problem
- name, address and telephone/telex number of your company and name of a responsible technical person whom Altos service may contact if necessary

CAUTION

Make sure you back up any hard disk data you wish to save before sending the hard disk drive for repair. The test procedure destroys the data on the hard disk. Altos cannot guarantee the integrity of data on hard disks which are sent for repair.

Packaging the System Unit

Use the original shipping container and packing if possible. If you do not have an Altos container, contact your dealer to see if one is available. If you still cannot obtain the correct container, ship the unit in a foam-padded heavy-duty corrugated shipping carton. Place a head protection sheet (shipped with the floppy drive) over the drive heads. Seal the carton securely and mark it FRAGILE. Remember to write the Return Authorization (RA) number on the outside and to insure the package. Altos cannot be responsible for lost or damaged shipments.

Packaging the Storage Devices

For best results, package tape, floppy disk, or hard disk drives in a sturdy foam-padded shipping carton if you do not have Altos packaging.

If you are shipping a floppy drive, insert a head protection sheet over the drive heads. Seal the carton securely and mark it FRAGILE. Remember to write the Authorization number on the outside and to insure the package. Altos cannot be responsible for lost or damaged shipments.

Packaging Printed Circuit Boards

If you are shipping a printed circuit board (PCB) and you do not have Altos packaging, wrap the unit in an anti-static cushioning material (such as Air Cap TH-240 available from Sealed Air Corporation, Hawthorne, New Jersey). Do not package PCBs using foam padding. Enclose the PCB in a heavy-duty corrugated shipping carton. Seal the carton securely and mark it FRAGILE. Remember to write the Return Authorization (RA) number on the outside and to insure the package. Altos cannot be responsible for lost or damaged shipments.

CHAPTER 5
TROUBLESHOOTING

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INTRODUCTION

This chapter contains a discussion of troubleshooting aids, techniques, and detailed procedures to assist service personnel when a trouble is suspected in the Altos 1086/2086 Computer System. Most troubles can be located quickly by following the troubleshooting information in this chapter. However, if problems persist, contact your nearest Altos distributor for assistance.

NOTE

Altos supports repair to the field-replaceable unit (FRU) level only. Printed circuit board repair should be performed by qualified service personnel.

TROUBLESHOOTING AIDS

Troubleshooting aids are included throughout this manual and in related publications. The following information is intended to acquaint service personnel with portions of this manual and related publications that contain useful troubleshooting and repair information.

System Overview

A thorough understanding of the 1086/2086 system operation is the most important aid when troubleshooting.

The system overview information in Chapter 1 includes an introduction to the 1086/2086 system and a list of related publications that contain additional operation information.

Principles of Operation

Detailed electrical operation of each circuit is described in Chapter 3. Additional details on integrated circuit (IC) operation are contained in the integrated circuit manufacturer's data handbooks referenced in Chapter 3.

Diagnostics

Power-up, system-confidence, and field-service diagnostic test programs are available in the system firmware and on the System Diagnostics Executive (SDX) floppy disk supplied with the system. These programs are designed to quickly locate a faulty field replaceable unit (FRU) or a failed part.

The troubleshooting procedures in this chapter provide detailed instructions for performing the diagnostic tests.

Remote diagnostic capability is also available with the optional Altos modem. Complete instructions for performing remote diagnostic tests are provided in the **1086/2086 Remote Diagnostics** manual (see **Related Publications** in the front of this manual for information about obtaining this manual).

Diagrams

Block, schematic, and PCB assembly diagrams are contained in the **Schematic Diagrams** supplement at the back of this manual.

PCB assembly diagrams are provided to help you rapidly locate the electrical parts shown on the schematic diagram(s).

Field Replaceable Unit Locations

The locations of all the field replaceable units (FRUs) are shown in Chapter 1. The **1086/2086 Illustrated Parts List** manual also shows the FRU locations and lists all of the component parts of the 1086/2086 system.

TROUBLESHOOTING CONSIDERATIONS

Consider the following information before troubleshooting the 1086/2086 Computer System.

Handling Static-Sensitive Devices

Certain precautions must be taken when working with static-sensitive devices, such as, microprocessors, field-effect transistors (FET), complimentary metal-oxide semiconductors, (CMOS), and other large-scale integration (LSI) devices that use metal-oxide semiconductor (MOS) technology. Static charge buildup in a person's body or leakage from an improperly grounded soldering iron can cause static-sensitive device failure.

Before handling a static-sensitive device or a PCB with such devices attached to it, ground any static voltage that may have accumulated in your body by touching an object that has been earth grounded.

A bare wire wrapped around your wrist and attached to an earth ground is effective when working extensively with static-sensitive devices. When soldering on a static-sensitive device, use a soldering iron with a properly grounded three-wire cord. (Refer to **Soldering Techniques and Equipment** for a discussion of recommended soldering irons and procedures.)

A static-sensitive device may appear defective due to leakage on a PCB. Observe the precautions for grounding static voltages described in the preceding paragraph and clean both sides of the PCB with flux remover or an eraser before replacing what may be a good static-sensitive device. For discrete FET devices, clean thoroughly between the gate, drain, and source leads.

Static-sensitive devices may be packaged in conductive foam or have a protective shorting wire attached to the pins.

Remove the conductive foam just prior to inserting the device in its socket or soldering to a PCB. Remove the shorting wire only after the device is inserted in its socket or after all the leads are soldered in place.

Soldering Techniques and Equipment

Observe the following recommendations when removing or replacing components soldered to a PCB. Poor soldering practices can damage a PCB or heat-sensitive electrical components.

Choosing the proper soldering iron is essential before attempting to remove or replace soldered-in components. Excessive heat is a common cause of damage to a component or PCB. However, transient voltages from solder guns or improperly grounded soldering irons can also damage certain voltage-sensitive semiconductor devices. Refer to **Static-Sensitive Devices** for more specific information.

A 15- to 27-watt pencil-tip soldering iron is recommended to avoid separating the etched circuit wiring from the board material and to avoid damaging active components. A temperature-controlled soldering station rated at 700 degrees Fahrenheit with a fine cone or a very fine chisel tip can also be used.

CAUTION

Solder guns are not recommended for removing or replacing soldered-in components on a printed-circuit board. The added possibility for over-heating and the large transient voltage induced by the soldering gun could cause damage to heat- or voltage-sensitive devices.

The following additional equipment is recommended for removing and replacing soldered-in components.

- Solder Sucker - Hand-operated vacuum tool used to remove liquified solder from the PCB.
- Solder Wick - Resin-soaked copper braid used for removing excess solder from the lead connections on the PCB. See **Removing Integrated Circuits** for precautions relating to the use of a solder wick on a multilayer PCB with plated-through holes.
- Flux Remover - Non-corrosive chemical used to clean foreign material from the PCB before soldering, and to remove any flux residue where components have been replaced. Flux remover is also used to clean any foreign material from the PCB during preventive maintenance. Isopropyl alcohol is also recommended as a cleaner.
- Acid Brush - Small stiff-bristled paint or toothbrush used with flux remover to clean flux and other foreign material from the PCB.

Removing Integrated Circuits

The easiest and safest method for removing soldered-in integrated circuits (ICs) from a PCB is to cut off each pin as close to the IC case as possible with a tip dyke (diagonal cutter) as shown in Figure 5-1.

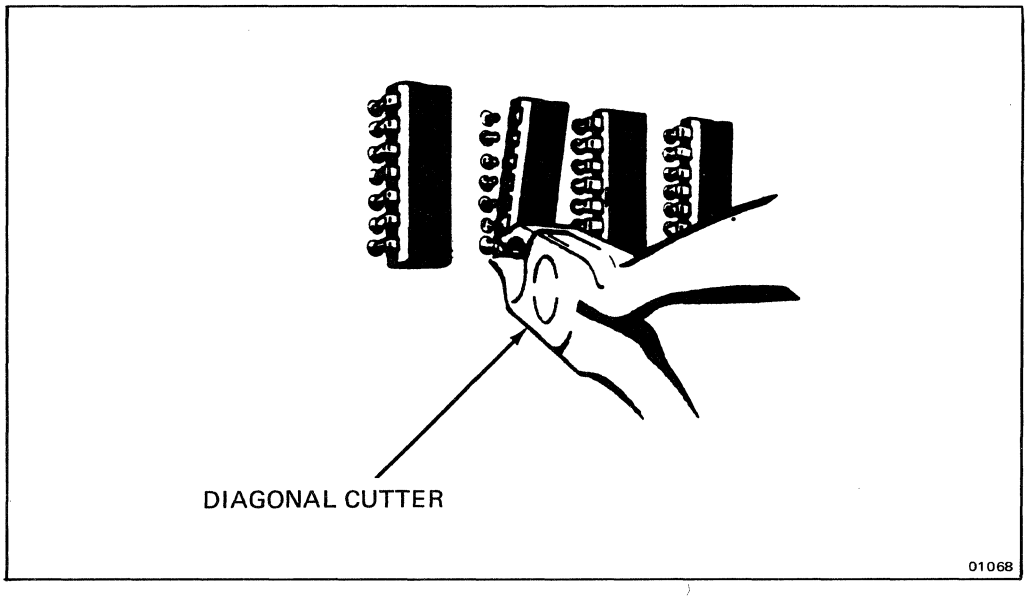

Figure 5-1. Removing ICs (Cut Pin Method)

Use the proper soldering iron as previously described under **Soldering Techniques and Equipment.** Then, to avoid excessive heat buildup in one area of the PCB, apply heat directly to each pin in a random order. Remove the loosened pin with the tip of the soldering iron or with the needle-nose pliers as shown in Figure 5-2. Allow a moment for the PCB to cool before proceeding to the next pin. Apply just enough heat to remove any stubborn pins.

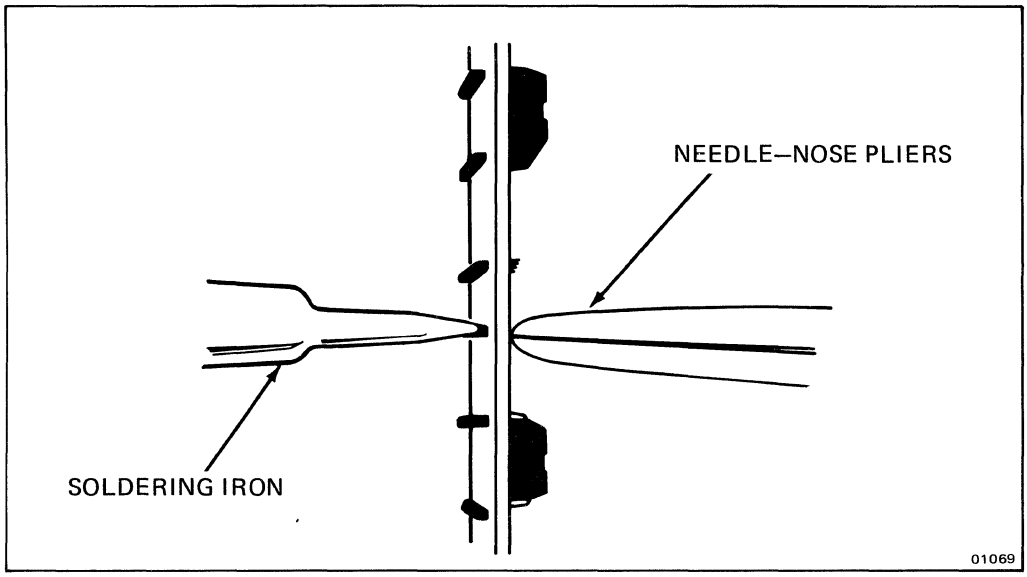

Figure 5-2. Removing IC Pins

For a multilayer PCB with plated-through holes, use a solder sucker to remove the remaining solder from inside each hole as shown in Figure 5-3. If possible, suck the solder from the opposite side of the PCB from where the heat is applied.

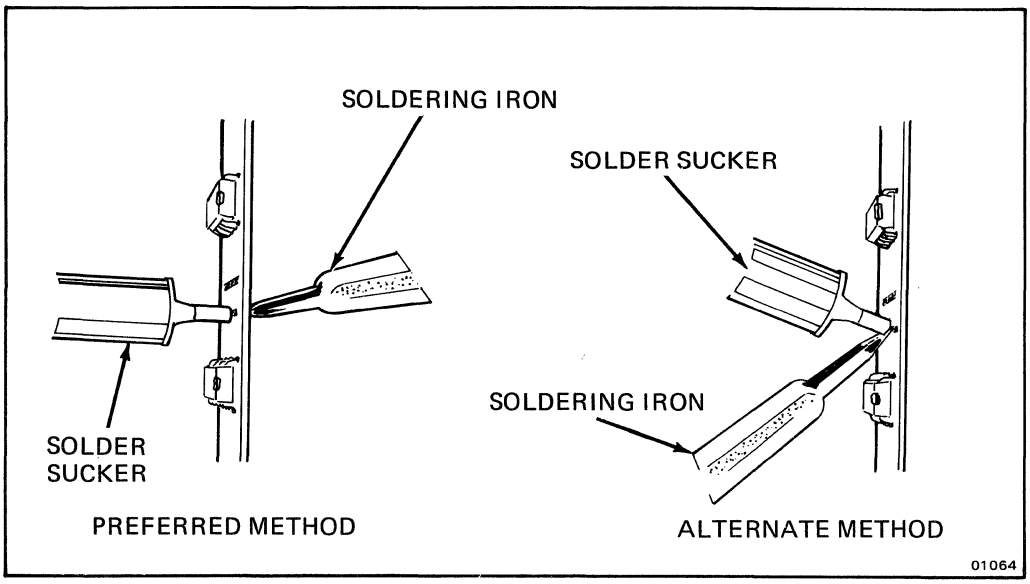

Figure 5-3. Removing Solder from Plated-Through Holes

Use a solder wick to remove excess solder from around the lead connection pads on the top and/or bottom surface of the PCB as shown in Figure 5-4.

CAUTION

Do not use a solder wick to remove solder from inside plated-through holes. The heat required for the solder wick to remove the solder from inside the hole could damage the PCB.

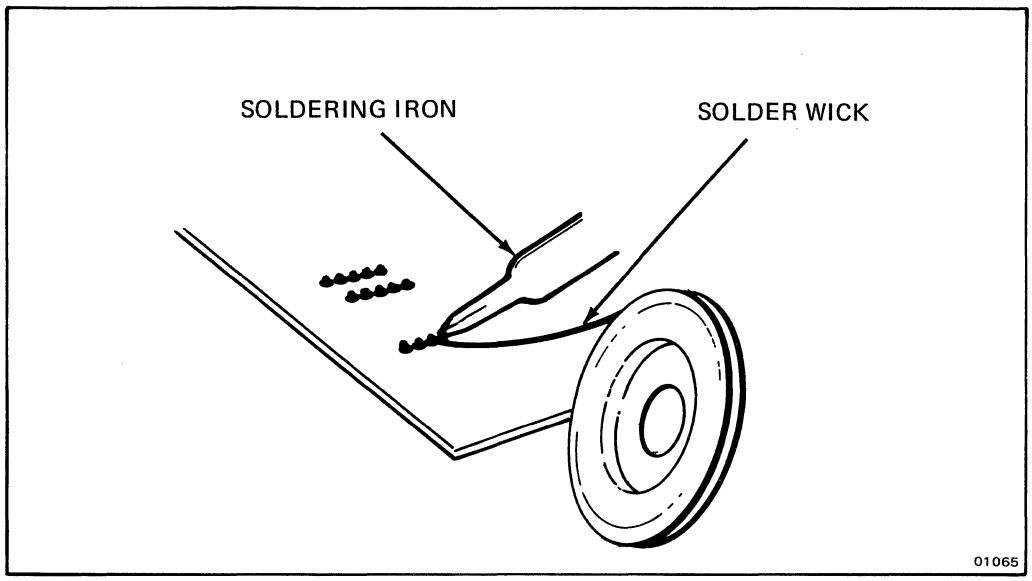

Figure 5-4. Removing Solder from Lead Connection Pads

TROUBLESHOOTING PROCEDURES

This section contains detailed troubleshooting procedures that use diagnostic programs available in the 1086/2086 system firmware or from the Altos Service Diagnostics Executive (SDX) floppy disk included with the system. These procedures are divided into low-level, power-up, system-confidence, field-service and debugger tests.

In addition to these five tests, remote diagnostic tests can also be performed with an optional Altos communications modem. The remote diagnostic tests are not included in this manual but are in the **1086/2086 Remote Diagnostics** manual (see **Related Publications** in the **About This Manual** section for information on obtaining this manual).

Which of the test procedures described here will quickly locate a trouble depends on the type of trouble and whether you wish to locate a faulty FRU or electrical component of the FRU. Carefully read the test procedures to help determine which one is most applicable for you.

Refer to the **Schematic Diagrams** supplement to this manual to help troubleshoot the 1086/2086 system.

CAUTION

Before attempting to troubleshoot, be sure that the main power supply and hard-disk drive power supply are set for the proper AC line voltage. (Refer to Chapter 4 for the main and hard-disk power supply conversion instructions.)

NOTE

To quickly locate the test procedures, look for the red tab along the right-hand edge of the first page of each procedure.

Low-Level Tests

Use Table 5-1 to perform the low-level tests. These tests are appropriate when the system fails to power-up or boot and the diagnostic tests will not run. Most of these tests do not require qualified service personnel.

Table 5-1. Low-Level Trouble Analysis

Symptom	Probable Cause	Remedy
No display on terminal. System seems dead	a. Screen has cycled off	Press return key
	b. Brightness or contrast too low	Adjust controls
	c. No power to system	Plug in a lamp or appliance to verify the power source
	d. Power cable loose or defective, or fuse blown.	Replace fuse or power cord.

CAUTION

If the fuse blows repeatedly, there is a short circuit in the system. Refer this trouble to qualified service personnel.

Display appears on terminal, but no response from keyboard	a. System "hung"	Push system reset switch.
	b. Terminal or system trouble	Verify terminal by plugging into another system, or checking other terminals on the system.
Terminal operation normal, but system seems dead.	a. Power cable loose or defective, or fuse blown.	Replace fuse or power cord.

WARNING

Hazardous voltages are present in the power supply. Use extreme caution when measuring voltages. Only qualified service personnel should attempt to check the power supply.

Table 5-1. Low-Level Trouble Analysis (Cont.)

Symptom	Probable Cause	Remedy
	NOTE The power supply is a switching type and must be checked under load to ensure accurate results.	
Terminal operation normal, but system seems dead. (Cont.)	b. Power supply DC voltages out of tolerance.	Check power supply voltages with a digital voltmeter. (Refer to Table 5-2 for power supply output voltages.)
Power supply malfunctions.	Power supply defective.	Repair or replace power supply.

If the power supply output voltages are out of tolerance, we recommend that the power supply be returned to the factory for repair or replacement.

Table 5-2. Power Supply DC Voltages

Voltage	Measured At	Range
+5	J5, Pin 4	+5.Ø to +5.2
+12	J5, Pin 6	+11.4 to +12.6
-12	J5, Pin 3	-11.4 to +12.6

Refer to Chapter 4 for detailed assembly removal and replacement procedures.

Power-Up Tests

The power-up tests use the ROM-based diagnostic tests contained on the CPU, communications, and file processor PCBs. The power-up tests are always performed when power is applied or the system is reset. Refer to Figure 5-5 for a block diagram of the power-up test sequence. These tests check the hardware configuration on each PCB, identify any missing or failed assemblies, and then confirm communication with the system as follows:

- communications (SIO) tests check local RAM and PROM, I/O integrated circuits, DMA controller, interrupts, system bus, and initialize memory
- CPU tests check the PROM, cache RAM, local RAM, translation and tag RAM, clock, optional floating-point processor, interrupts, and system bus
- file-processor tests check the local RAM and PROM, interval timer, system bus, DMA controller, and magnetic-media controllers

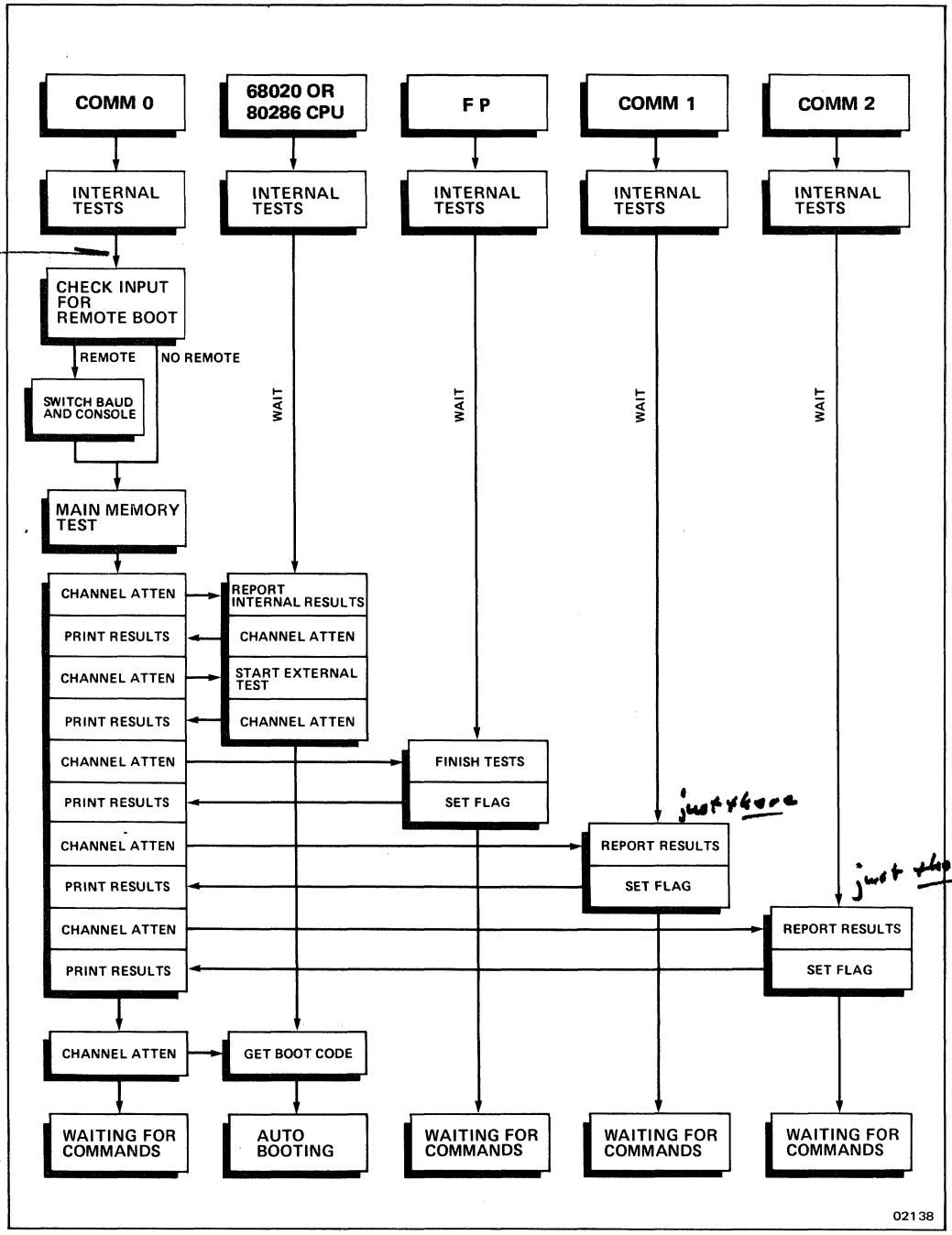

Figure 5-5. System Power-Up Test Sequence

System Power-Up Sequence

During power-up, the master communications (SIO) PCB firmware proceeds in the following sequence.

1. After internal verification, the communications PCB firmware sends a **COMMUNICATIONS BOARD POWER-UP TESTS** message to port Ø (main console).

2. After internal verification, the master communications PCB tests the system memory.

3. After the internal and external tests are completed, the master communications PCB sets up a firmware protocol block and sends a channel attention to the CPU PCB. The communications PCB will timeout if the CPU does not respond in a few seconds.

4. After receiving acknowledgement from the CPU PCB, the communications PCB displays its power-up test results on the main console (port Ø).

5. The master communications PCB performs the same test requests for the file processor PCB. If there is a file processor error, a corresponding error message is displayed.

6. Other communications (SIO) PCBs are checked for availability.

7. The auto boot from the hard disk (highest logical priority device) is performed, unless the user presses a key to interrupt the process.

8. If the boot operation is successful, control is transferred. Otherwise, an error message is displayed with a new menu to allow the user to either boot from a particular device or enter the debugger routine (see **Debugger Program** for additional details).

9. If a floppy disk boot is requested, the CPU PCB tries a slow-speed check for dual-speed floppy disk drives. If this fails, then a high-speed check is attempted. If both of these checks fail, then the boot menu is displayed.

Communications Power-Up Tests

The communications monitor program has two menus: one for debugging the hardware, and the other for debugging software. At power-up time the monitor is in the software mode. The hardware mode is a hostile environment and is not intended for normal use. To switch modes, type the <**break**> key, then the <**return**> key at the command level.

1. **Checksum the PROMs**

   The PROMs are summed separately to determine which one(s) to replace. A failure of the checksums is considered a major failure because the integrity of the PROMs is in doubt. No other tests can be trusted since they may pass from unknown changes in the firmware.

2. **Local Bus Data Ripple**

   The main RAM is on a 16-bit bus. The first word is used to test the data lines. A 1 bit is rippled through the data lines, then a Ø bit is rippled through.

3. **Local Bus Content March**

   The local RAM is tested with two patterns, 5555 and AAAA. This test simply marches through RAM one word at a time. After each location is tested, it is cleared with a Ø.

4. **CIO**

   The internal registers are loaded and checked for valid data.

5. **SCC1**

   The internal registers are loaded and checked for valid data.

6. **SCC2**

   The internal registers are loaded and checked for valid data.

7. **SCC3**

   The internal registers are loaded and checked for valid data.

8. **SCC4**

   The internal registers are loaded and checked for valid data.

9. **SCC5**

   The internal registers are loaded and checked for valid data.

10. **DMA Controller**

    The internal registers are loaded and checked for valid data.

11. **System Memory**

    The system memory is sized in 64K byte blocks. Then each block is tested with the standard patterns of 5555 and AAAA. After a location is tested it is cleared.

CPU Power-Up Tests

The monitor program is executed whenever the system is powered up or reset. The power-up sequence starts with a series of tests that validate the system as follows:

1. **Checksum the PROMs**

   The PROMs are summed separately. A failure of the checksums is considered a major failure because the integrity of the PROMs is in doubt. No other tests can be trusted. If any other tests pass, it may be from some unknown change in the firmware.

2. Cache RAM Data Ripple

The cache RAM is organized as two sets of words. The data ripple test must read and write a test word to locations 0 and 2. The cache RAM is located from 402000 to 403FFE.

Thirty-two data bits are tested. A 1 bit is rippled through the data lines, then a 0 bit is rippled through.

3. Cache RAM Address Ripple

The cache RAM is loaded with a background pattern. Then selected locations are tested for this pattern. It should be noted that a bad RAM can look like a bad address bus. Therefore, this test assumes the cache RAM is good. There are four RAMs in the cache memory, and they are addressed with the two lower address lines.

Then the next 11 addresses select the byte in the cache RAM. Each RAM is tested individually to check the addresses going to each one.

4. Cache RAM Content March

The cache RAM is tested with two patterns: 00 and FF. This test marches through RAM one byte at a time. If a particular address location fails, then the test loops on that address location. This test leaves all zeros in the cache RAM.

5. Translation RAM Data Ripple

The translation RAM is located from address 400800 to 400FFE. Twelve data bits are tested. The first location is used to test the data lines. A 1 bit is rippled through the data lines, then a 0 bit is rippled through.

6. Translation RAM Address Ripple

The translation RAM is loaded with a background pattern of incrementing words. Then selected locations are tested for this pattern. It should be noted that a bad RAM can look like a bad address bus. There fore, this test assumes the translation RAM is good. There are only nine address lines to test. Address line Ø is not toggled here because all translation RAM addresses are even.

7. Translation RAM Content March

The translation RAM is tested with two patterns: ØØØØ and FFFF. If the test passes, then the translation RAM is initialized for a one-to-one mapping. This test marches through RAM one word at a time. If a particular location fails, then the test loops on that location. If the system has additional translation RAM, then it is also tested and initialized.

8. Tag RAM Data Ripple

The tag RAM is 1K words long and is located from address 4Ø1ØØØ to 4Ø1FFE. Twelve data bits are tested.

The first location is used to test the data lines. A 1 bit is rippled through the data lines, then a Ø bit is rippled through.

9. Tag RAM Address Ripple

The tag RAM is loaded with a background pattern of incrementing words, then selected locations are tested for this pattern.

It should be noted that a bad RAM can look like a bad address bus. Therefore, this test assumes the tag RAM is good. There are only nine address lines to test.

NOTE

Address line Ø is not toggled here because all tag RAM addresses are even.

1Ø. Tag RAM Content March

The tag RAM is tested with two patterns: ØØØØ and FFFF. If the test passes, then the tag RAM is initialized for a one-to-one mapping. This test marches through RAM one word at a time.

If a particular location fails, then the test loops on that location. This test leaves all ones in the tag RAM to invalidate all tags.

11. Not Performed

12. Not performed.

13. Not performed.

14. Not performed.

15. 8Ø287 Numeric Processor Extension

The 8Ø287 is initialized and the status is read. The status will be all zeros if 8Ø287 is functioning. If the status is good, two BCD numbers in memory are added and the result placed in another location. The result is then checked for the correct answer.

internal / external

16. Interrupt Controller Test Using Clock

The interrupt controller is set up for the normal mode of operation, then interrupts 6 and 7 are introduced through the hardware output port. After these two interrupts pass, the clock interrupt is tested. Interrupts 1 through 5 are not tested because there is no way to produce them. The clock-control register is set to interrupt every 1/1Øth of a second, then the clock is reset.

17. Write Cache Miss

The tags are made invalid by setting the invalid bits. Then 4K of system-bus memory is written to with an FFFF pattern while the cache is disabled. The cache has already been set to zeros from the cache content test. After the system-bus memory is written, the cache is disabled and checked to verify that it still contains the zeros. The cache should never be updated during a write to system-bus memory.

18. Read Cache Miss

The cache is enabled from the start of the test. The tag invalid bits are set to invalid for all the tags. A 4K byte block of system-bus memory is initialized to all ones. The system-bus memory block is then read at every fourth location. The cache is then compared to verify that it contains all ones like the memory block. Then the tags are checked for the proper addresses and the valid bits are set.

19. Write Cache Hit

The tags are all valid from the previous test. The cache is enabled and a 4K byte block of system-bus memory is initialized with a 9090 data pattern. The cache is then disabled. The system-bus memory block is read, but the data is ignored. Then the cache memory is read and compared to the 9090 data pattern. If the cache compares, then this test fails.

20. Read Cache Hit

The tags are valid. The cache is disabled and loaded with a F4F4 data pattern. The cache is then enabled. The system bus memory is read again, but the data should come from cache RAM instead of system-bus memory. The data read back should equal the F4F4 data pattern.

21. Cache Execution

A 4K byte block of system bus memory is loaded with "inc dx" instructions and a far return at the end. The cache is enabled, then a call is made to the code and it executes. Then cache is disabled and checked to verify that it matches the code in memory. The dx register is also checked for the proper value.1.

22. Tag Update With Diagnostic Bit Settings

The cache is enabled from the start of the test. The tag invalid bits are reset to validate all the tags. The diagnostic test bit is set to simulate a write from another bus master. A 4K byte block of system bus memory is initialized to all ones. The tags are checked to verify that the valid bits are set to invalid.

23. Alternating I/O and Memory Read Cache

This test is intended to check the hardware as different machine states are introduced. The cache is enabled and a sequence of reads are done. The translation RAM is read from, then the system bus memory is read from, and the cache RAM is checked to verify that the data was transferred. This sequence is repeated for the monitor and tag RAMs also. Then the order is reversed so that the system bus memory is read from first and the other RAMs second. The cache is always checked last to ensure that the data was transferred.

Once the preceding tests have been performed, the CPU waits until the communications (SIO) PCB is ready to get the results.

If the power-up tests pass, the first test summary messages to appear on the system console should be:

```
Communications System Powerup Tests Passed
Initializing system memory
..............
```

Each dot on the bottom line of the displayed message equals 256K bytes of system memory. After about 35 seconds, the next test summary messages similar to the following should appear:

```
Communications System Powerup Tests Passed
System memory size = xxxxx.
Main CPU internal test passed.
Main CPU external test passed.
Initializing file processor... ver. x.x passed.
SIO #1 passed.*

Type any key to interrupt autoboot.
```

* If there is a second SIO installed.

NOTE

If your system has more than two communications PCBs, you will see more than one SIO message, such as **SIO #2 passed,** etc. (SIO is an abbreviation for serial input/output.)

If the CPU power-up test failed, the following message appears:

No response from the CPU

Table 5-3 lists the power-up test failure status monitored at the output latch port at location 25A on the CPU PCB.

Table 5-3. CPU Failure Status at Output Latch Port

Test No.	2 7	5 6	6 5	9 4	12 3	15 2	16 1	19 Ø	Pin Numbers Bit Positions
1	Ø	Ø	Ø	Ø	Ø	1	1	Ø	PROM checksum test
2	Ø	Ø	Ø	Ø	1	Ø	Ø	Ø	Cache data ripple
3	Ø	Ø	Ø	Ø	1	Ø	1	Ø	Cache address ripple
4	Ø	Ø	Ø	Ø	1	1	Ø	Ø	Cache content
5	Ø	Ø	Ø	Ø	1	1	1	Ø	Translation data ripple
6	Ø	Ø	Ø	1	Ø	Ø	Ø	Ø	Translation address ripple
7	Ø	Ø	Ø	1	Ø	Ø	1	Ø	Translation content
8	Ø	Ø	Ø	1	Ø	1	Ø	Ø	Tag data ripple
9	Ø	Ø	Ø	1	Ø	1	1	Ø	Tag address ripple
10	Ø	Ø	Ø	1	1	Ø	Ø	Ø	Tag content
11	X	X	X	X	X	X	X	X	Not performed (illegal)
12	X	X	X	X	X	X	X	X	Not performed (illegal)
13	X	X	X	X	X	X	X	X	Not performed (illegal)
14	X	X	X	X	X	X	X	X	Not performed (illegal)
15	Ø	Ø	1	Ø	Ø	Ø	1	Ø	80287 NPX test
16	1	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Interrupt controller test
17	1	Ø	1	Ø	1	Ø	Ø	Ø	Write cache miss
18	1	Ø	1	Ø	1	Ø	1	1	Read cache miss
19	1	Ø	1	Ø	1	1	Ø	Ø	Write cache hit
20	1	Ø	1	Ø	1	1	1	Ø	Read cache hit
21	1	Ø	1	1	Ø	Ø	Ø	Ø	Cache execution test
22	1	1	1	1	Ø	Ø	Ø	1	Tag update
23	1	Ø	1	1	Ø	1	Ø	1	Alternate I/O and memory

If all power-up tests have passed, the message **Type any character to interrupt autoboot** appears. Press any key within the next five seconds. The screen then displays a boot menu similar to:

```
Enter [1] to Boot from Hard Disk
Enter [2] to Boot from Floppy Disk
Enter [3] to enter the main CPU Monitor
Enter [4] to enter the main SIO Monitor
```

If you did not press a key within five seconds, the system will attempt a default boot (autoboot) from the hard disk. This is normal start-up procedure after you install the operating system software.

If the autoboot failed or if you entered a **1**, and the boot from the hard disk failed, a message similar to the following will appear:

```
Booting from hard disk
File system not supported
Boot failed, status: 00 00 00 00 00

Select [1> to boot from HD
Select [2> to boot from FD
Select [3> to enter debugger
```

Status bytes 1 through 5 in the preceding **Boot failed, status: 00 00 00 00 00** message indicates the hard disk status as follows:

RESULTS BYTE 1:

```
    0 = No error
    1 = General error
    2 = Device not supported
    3 = Device not present
    4 = Invalid command
    5 = Interrupt/DMA operations error
    6 = Western Digital WD2010 hard disk
        controller command error
   FF = Command accepted, but not yet finished
```

RESULTS BYTE 2: Contains the contents of the WD2010 error register. Refer to Table 5-4 for a detailed description of the error register bits.

RESULTS BYTE 3: Contains the contents of the WD2010 status register. Refer to Table 5-4 for a detailed description of the status register bits.

RESULTS BYTE 4: Cylinder.

RESULTS BYTE 5: Cylinder.

Tables 5-4 and 5-5 provide a detailed description of the hard disk controller (WD2010) error and status register bits. Refer to the **Western Digital WD2010 Data Book** for additional information.

Table 5-4. Hard-Disk Controller Error Register Bit Descriptions

Bit No.	Bit Name	Symbol	Description
7	Bad Block Detect	BBD	Set when an ID field has been found with a bad block mark (used for bad sectors)
6	CRC/ECC Data Field Error	CRC/ECC	Set when a CRC error occurs in the data field
5	Reserved		0
4	ID Not Found	ID	Set to indicate that the correct cylinder head, sector, and size parameter could not be found
3	Reserved		0
2	Abort Command	AC	Command is aborted and this bit is set if; DRDY has not been asserted, or WF has been asserted, or the command issued has an unidentified command code
1	Track Zero Command	TK	Set during Restore command when TK00 input has not indicated that the head has reached track 00 (in 2047 steps)

Table 5-4. Hard-Disk Controller Error Register Bit Descriptions (Cont.)

Bit No.	Bit Name	Symbol	Description
Ø	Data	DM	Set during a Read sector command if the data address mark is not found following the proper sector ID

Table 5-5. Hard-Disk Controller Status Register Bit Descriptions

Bit No.	Bit Name	Symbol	Description
7	Busy	BSY	Asserted when a command is written to the command register and, except for the Read command, is deasserted at the end of the command
6	Ready	RDY	Reflects the status of DRDY. When zero (Ø), the command is aborted and the status of the bit is latched
5	Write Fault	WF	Reflects the status of the write fault. When one (1), the command is aborted, INTRQ is asserted, and the status of the bit is latched
4	Seek Comp.	SC	Tells the hard disk controller that the seeking drive has finished seek and informs the controller that the seek has been completed

Table 5-5. Hard-Disk Controller Status Register Bit Descriptions (Cont.)

Bit No.	Bit Name	Symbol	Description
3	Data Request	DRQ	Asserted by the hard disk controller when the sector buffer is written to or read from
2	Data Corrected	DWC	When one (1), and error has been detected during the ECC mode and the data in the sector buffer has been corrected
1	Command in Progress	CIP	Set by the hard disk controller to indicate that a command is being executed and indicates to the file processor that no other commands should be loaded
Ø	Error	ERR	Indicates that a nonrecoverable error has occurred. When the host reads the status and finds this bit set, it must read the error register to determine the type of error

If you entered a **2** and the boot from floppy disk failed, a message similar to the following will appear:

```
Booting from floppy (low speed)
Boot failed, status: 00 00 00 00 00

Select [1> to boot from HD
Select [2> to boot from FD
Select [3> to enter debugger
```

Status bytes 1 through 5 in the preceding **Boot failed, status: XX XX XX XX XX** message indicate the following floppy disk status:

RESULTS BYTE 1:

Error other than 2, 3, 4 points away from FD

- 0 = No error
- 1 = General error
- 2 = Device not supported
- 3 = Device not present
- 4 = Invalid command — File processor problem
- 5 = Interrupt/DMA operations error
- 6 = NEC PD765 floppy disk controller command/ status error
- FF = Command accepted, but not yet finished

RESULTS BYTE 2: Contains the contents of the PD765 status register 0. Refer to Table 5-6 for a detailed description of the status register bits.

RESULTS BYTE 3: Contains the contents of the PD765 status register 1. Refer to Table 5-7 for a detailed description of the status register bits.

RESULTS BYTE 4: Contains the contents of the PD765 status register 2. Refer to Table 5-8 for a detailed description of the status register bits.

RESULTS BYTE 5: Not used.

Tables 5-6 through 5-9 provide a detailed description of the floppy disk controller (PD765) status register Ø through 3 bits. Refer to the **NEC PD765 Data Book** for additional information.

Table 5-6. Floppy Disk Controller Status Register Ø Bit Descriptions

Bit No.	Bit Name	Symbol	Description
7	Inter-rupt Code	IC	D7 and D6 = Ø. Normal termination of command (NT). Command complete and properly executed
6	------		D7 = Ø and D6 = 1. Abnormal termination of command (AT). Execution of command started but not success-fully completed D7 = 1 and D6 = Ø. Invalid command issued. Command was issued but not started D7 and D6 = 1. Abnormal termination caused by the Ready line from FDD changing states during command execution
5	Seek End	SE	When the FDC has completed a seek, the SEEK command line = 1
4	Equipment Check	EC	Asserted if the fault signal is received from the FDD, or if the track Ø signal fails to occur after 77 step pulses (recalibrate)

Table 5-6. Floppy Disk Controller Status Register Ø Bit Descriptions (Cont.)

Bit No.	Bit Name	Symbol	Description
3	Not Ready	NR	Asserted when FDD is in the not ready state and a read or write bit is set. Command occurs if a read or write is issued to side 1 of a single-sided drive, then flag is set
2	Head Address	HD	Flag used to indicate the state of the head at interrupt
1	Unit Select 1	US1	Flag used to indicate a drive unit at interrupt
Ø	Unit Select Ø	USØ	Flag used to indicate a drive unit at interrupt

Table 5-7. Floppy Disk Controller Status Register 1 Bit Descriptions

Bit No.	Bit Name	Symbol	Description
D7	End of Cylinder	EN	Set when FDC tries to access a sector beyond the final sector of a cylinder
D6	-------		Not used. Always zero (Ø)
D5	Data Error	DE	Set when FDC detects a CRC error in either the (ID) or data fields
D4	Overrun	OR	Set if the FDC is not serviced within a certain time during data transfers by the main system

Table 5-7. Floppy Disk Controller Status Register 1 Bit Descriptions (Cont.)

Bit No.	Bit Name	Symbol	Description
D3	-------		Not used. Always zero (Ø)
D2	No Data	ND	Set if, during execution of the READ DATA, WRITE DELETED, or SCAN commands, the FDC cannot find the sector specified in the IDR register
D2	(Cont.)		Set if, during execution of the READ ID command, the FDC cannot read the ID field without an error Set if, during execution of the READ or CYLINDER commands, the starting sector cannot be found
D1	Not Writable	NW	Set if, during execution of WRITE DATA, WRITE DELETED DATA, or FORMAT A CYLINDER, the FDC detects a write protect signal from FDD
DØ	Missing Address	MA	Set if the FDC cannot detect the data address mark or deleted data address mark. Also, at the same time, the MD (missing address mark in data field) in status register 2 is set. Also set if FDC cannot detect ID address mark during two index pulses

Table 5-8. Floppy Disk Controller Status Register 2 Bit Descriptions

Bit No.	Bit Name	Symbol	Description
7	------		Not used. Always zero (Ø)
6	Control Mark	CM	Set if, during execution of the READ DATA or SCAN commands, the FDC encounters a sector that contains a deleted data address mark
5	Data Error Data Field	DD	Set if the FDC detects a CRC error in the data field
4	Wrong Cylinder	WC	Related to ND. Set when the content of C on the medium is different from that stored in IDR
3	Scan Equal Hit	SH	Set if, during execution of the SCAN command, the condition of "equal" is satisfied
2	Scan Not Satisfied	SN	Set if, during execution of the SCAN command, the FDC cannot find a Sector on the cylinder that meets the condition of "equal" in the above command
1	Bad Cylinder	BC	Related to ND. Set when the content of C on the medium is different from that stored in the IDR and the content of C is FF
Ø	Missing Address Mark in Data Field	MD	Set if, when data is read from the medium, the FDC cannot find a Data Address Mark or Deleted Data Address Mark

Table 5-9. Floppy Disk Controller Status Register 3 Bit Descriptions

Bit No.	Bit Name	Symbol	Description
			NOTE The following data is available in the parameter block and is not written to the screen
D7	Fault	FT	Indicates the status of the Fault signal from FDD
D6	Write Protect	WP	Indicates the status of the Write Protect signal from FDD
D5	Ready	RY	Indicates the status of the Ready signal from FDD
D4	Track Ø	TØ	Indicates the status of the Track Ø signal from FDD
D3	Two Side	TS	Indicates the status of the Two Side signal from FDD
D2	Head Address	HD	Indicates the status of the Side Select signal to FDD
D1	Unit Select 1	US1	Indicates the status of the Unit Select 1 signal to the FDD
DØ	Unit Select Ø	USØ	Indicates the status of the Unit Select Ø signal to the FDD

Entering a **3** from the boot menu (or from the menu that appears when the boot fails) gets you into the CPU monitor debugger and a message from the communications PCB similar to the following appears:

```
2086 CPU-Debugger        X.609
Type ? For Help Menu
CS:IP = 0018:26B2
```

Entering a **4** from the boot menu gets you the SIO monitor debugger and a message from the communications PCB similar to the following will appear:

```
Communications Monitor/Debugger-Version X.X
Type ? for the Menu
SIO Memory Size = 32KB
```

If a **failed** message appears in the power-up test summary, determine which tests in the SDX Field Service Menu are applicable and run the tests. If desired, use the boot menu to select the CPU or SIO debuggers (monitors) and perform the debugger procedures as described at the back of this chapter in the **Debugger Tests** section.

File Processor and Controller Power-Up Tests

The file processor and controller firmware consists of power-up diagnostic tests that verify the operation of major components on the file processor and controller PCBs.

The firmware performs the following tests upon power up. Tests 1 through 12 are done internally within the

file processor PCB while tests 13 and 14 are performed after the file processor gets the first channel attention signal. For tests 1 through 4, the firmware loops on each failed test, and will not proceed to the next test.

For the rest of the tests, the firmware will not loop on each failed test. The firmware attempts to report the power-up status via the printer port (0602h). The upper four bits of the printer port are used for indicating the test number of the first failed test, while the lower four bits are for displaying the test number of the the last test.

1. **PROM Checksum**

   The firmware is located on two 4K x 8 bit PROMS. The checksum byte is written to the last byte of each PROM. Each PROM is checked separately. The sum should be 0 by adding up all the bytes of each PROM.

2. **Local RAM Data Bus Ripple**

   This test checks the integrity of the local RAM data bus. A 0 bit pattern is written to location 0000. It then ripples a 1 bit across the data bus to ensure adjacent bits are not stuck.

3. **Local RAM Address Bus Ripple**

   This test checks the integrity of the local RAM address bus. A data pattern of decimal 14 is written to local memory location 4000h. Then the data pattern is decremented by 1 and written to the next location by rippling a 1 bit across the address line.

   The last location written is 0000h. Each written byte is checked by reading out the written data pattern, writing the complement of that data pattern, and reading back again to verify.

4. Local RAM Content March

Each memory word is first filled with a data pattern of 5555h. Each of the 16K words is checked for the data pattern and the complement AAAAh is written back to the same word and verified.

5. Local Memory Parity Error

This test checks the local memory parity. For each location tested, an even data pattern (already writ ten during the content march) is read, then the odd data pattern (7676h) is written and dummy read back to verify that a parity error has been generated.

6. 8254

This test programs counter Ø of interval timer 8254 for mode Ø, loads counter Ø, and starts the count. After a short delay, the counter is read back to verify that the counter has been decremented.

7. DMA Controller

This test programs interval timer 8254 to generate an interrupt signal to the IRO pin of the interrupt controller 8259. The interrupt controller is then verified.

8. SCSI Controller

Upon power-up or reset, the controller will perform self-diagnostics. When self-diagnostics are complete and if no error was detected, the diagnostic-status register is checked for bit pattern 10000000 which verifies the SCSI controller.

9. DMA Controller

This test first clears each channel-status register by writing FFh into the register. Then a 5678h pattern is written to the memory-transfer counter for each DMA channel and each memory-transfer counter is verified later.

10. Floppy Disk Controller

To verify the floppy-disk interface, the firmware first issues a SPECIFY command to set the initial values for each of the three internal timers (head unload time, step rate time, and head load time). Then it issues a RECALL command to initialize the drive and retract the heads. If no error is detected, the interface is verified.

11. Hard Disk Controller

This test first writes a Ø pattern to the SDH register of the hard disk controller on the controller PCB and reads it back to verify. Then the complement is written back to the SDH register and read to verify again.

12. Streaming Tape Controller

The interface is verified by checking that reset/power (bit Ø) is set in status byte 1.

13. System RAM Data-Bus Ripple

This test checks the system RAM data bus. A Ø pattern is written to system-memory word ØØØØØ. Then a 1 bit is rippled across the data bus to ensure that adjacent bits are not stuck.

14. System RAM Address-Bus Ripple

This test checks the system RAM address bus. A data pattern of decimal 19 is written to local memory location 8ØØØØh. Then the data pattern is decremented by 1 and written to the next location by rippling a 1 bit across the address line. The last location written is ØØØØØh. Then each byte is checked by reading the data pattern, writing the complement of that data pattern, and reading back again to verify.

CPU and File Processor Communication

Software interface between the CPU PCB and file processor PCB is by means of a parameter block. At initialization, location 1FFFCh to 1FFFFh in system memory may contain a pointer to this parameter block.

The first time the file processor is interrupted, the pointer is read to locate the parameter block.

Interrupt Signals

The basic communications interface between the CPU PCB and file processor PCB is via two signals:

1. 286INT (channel attention to file processor). When this signal is asserted, the file processor is informed that a control block created by the CPU PCB is available or the previous command request from the file processor has been executed.

2. INT286 (channel attention to CPU PCB). When this signal is asserted, the CPU PCB is informed that a control block created by the file processor is available or the previous command request from the CPU PCB has been executed.

Communication Protocol

Upon completion of all internal tests, the file processor waits for the first channel attention from the communications (SIO) PCB. As soon as channel attention occurs, the file processor gets the control block pointer in system memory location 1FFFC and obtains all the information from the control block.

The device number (word) and the command (word) should be 12 (file processor) and Ø (power-up initialization) respectively.

The file processor writes a hexadecimal value of FF to the result (word) indicating that the command has been accepted. Then the file processor performs a system data-bus and system address-bus ripple test.

Upon completion, the file processor puts the power-up test result message in the message buffer, stores the status in the result word, clears the command pending bit (bit 15 of the command word).

The file processor then remains in an idle state and waits for the subsequent CPU attention.

When the next CPU attention occurs, the file processor obtains the command information from the control block, writes a hexadecimal value of FF to the result word for acknowledging, branches to the appropriate routine for executing the command, puts the status in the result word, clears the command pending bit, and sends an interrupt to the CPU PCB. Then the file processor goes back to the idle state and waits for a channel attention from the CPU PCB.

System-Confidence Tests

The system-confidence tests use diagnostic programs contained on the Altos Service Diagnostic Executive (SDX) floppy disk included with the 1086/2086. The system-confidence tests are designed for the more experienced technician to perform a series of menu-driven tests that are more thorough than the previous power-up tests. The system-confidence tests contain a set of system utilities for handling system configuration and magnetic media.

The system-confidence tests dynamically test the following:

- floppy disk drive
- hard disk drive
- controller
- serial communication channels
- central processing unit (CPU)
- system memory
- file processor
- interrupt controller

System-confidence tests should be run if you are not sure there is a problem, or to determine if a problem is hardware or software related. System-confidence tests take about 15 minutes and verify most of the hardware, but only give a pass-fail indication.

Booting the SDX Disk

Perform the following procedure to boot the SDX floppy into memory to enable you to run the system-confidence tests:

1. Insert the SDX disk into the floppy drive and obtain the boot menu as described in the preceding **Power-Up Tests** section.

2. Type **2** to boot from the SDX floppy disk. Wait for the SDX menu to appear as follows:

```
ACS xxxx SYSTEM DIAGNOSTIC EXECUTIVE (SDX)
                                Version x.xx

Main Menu:

        R:  Run system confidence tests

        U:  Utility programs

        S:  Display test summary

        X:  Exit SDX

*** Enter command and press <CR>:
```

3. Type **R** and press <**CR**> to begin the system confidence tests. If you want to stop the test process, press <**ESC**>. The testing will stop with the current test (sometimes it takes a while).

   The Main Memory Refresh Test takes two minutes. If you want to bypass this test, be prepared to press <**ESC**> immediately after you see the message:

```
Memory Refresh Test in progress, press
<ESC> to abort this test.
```

NOTE

You do not need to monitor the test process. The program saves the test results in a test summary which you can review after the tests are completed.

4. Take a break while the tests complete. The test summary is ready when you see the following message:

```
Do you wish to review test summary (y or n):
```

After you type **y**, the screen displays information similar to:

```
                System Confidence Tests Summary

PROM Checksum Test.........................Passed
Cache RAM Test.............................Passed
Translation RAM Test ......................Passed
Memory Management Unit Test................Passed
Main Memory March Test.....................Passed
Main Memory Refresh Test...................Passed
Floppy Random Seek Test....................Passed
Hard Disk Random Seek Test.................Passed
Streaming Tape Append Test.................Passed
SIO Checksum Test..........................Passed
SIO Memory March and Refresh Test..........Passed
SIO LSI Chips Access Test..................Passed
SIO Interrupt Vector Test..................Passed
SIO DMA Test...............................Passed
SIO Timer Test.............................Passed
```

If you need to stop the system-confidence tests before they are completed, press <**ESC**>. The message **Interrupted** appears and you will return to the Main Menu.

You can also review the test summary by selecting **S** from the Main Menu.

If the test summary reports any tests as **Failed**, note the test description in the test summary and replace the failed field-replaceable unit (FRU) or perform the appropriate tests in the SDX field-service menu as described in the **Field-Service Tests** section.

Field-Service Tests

The field-service tests are contained on the System Diagnostics Executive (SDX) floppy disk supplied with the 1086/2086. These tests are the most thorough and flexible tests available to service personnel (other than remote diagnostics). The system can be tested extensively by running the field-service tests individually and repeatedly.

Unlike the previous system-confidence tests, the field-service tests include commands for looping tests, changing parameters, and selecting debugger routines (refer to the **Debugger Tests** section for a description of the debugger routines).

The field-service tests can be individually selected and report pass/fail messages to the terminal. Four different test menus are accessed through the SDX Field Service Menu to provide options for testing the CPU, file processor, controller, and communications (SIO) circuits. Detailed error messages are saved in a history buffer that allows you to recall them from the SDX Field Service Menu at any time.

SDX Field Service Menu

Perform the following procedure to boot the SDX disk and obtain the SDX Field Service Menu:

1. Boot the SDX floppy disk as described under **Booting the SDX Disk** in the previous **System-Confidence Test** section. When the main menu appears, press the **CONTROL** key and type **F**.

2. The displayed message prompts you for a password. Type **sotla** and press <**CR**>. The following SDX Field Service Menu will appear:

```
SDX Field Service Menu:

        b (brief)     Brief description of all tests
        c (clear)     Clear pass count, error count, and history
        d (disable)   Disable test
        e (enable)    Enable test
        h (halt)      Halt on error
        l (loop)      Loop on command line
        m (menu)      Menu level selection
        p (parameter) Change parameters
        r (report)    Display error history
        s (summary)   Display error summary
        t (test)      Execute test (s)
        u (utility)   Call utility programs
        ? (help)      Display this menu
        x (exit)      Exit to main menu
        z (debugger)  Enter debugger

        ***Enter Command and Press <CR>
```

3. Type the appropriate command from the Field Service Menu to perform the following test functions:

   b (brief). Displays a brief description of all the SDX tests with their test number and enabled or disabled status.

   c (clear). Clears the error history buffer and resets the pass count and error count to zero.

   d (disable). Allows you to disable any selected tests executed by the t command as follows:

   a. Enter the test number(s), separated by commas.

   b. Press <**CR**>.

   e (enable). Allows you to enable tests to be executed by the **t** command as follows:

   a. Enter the test number(s), separated by commas.

   b. Press <**CR**>.

   h (halt). Allows you to choose from two options for running the t tests: (a) the tests halt when an error occurs and (b) the program continues after an error is discovered or until the end of the test.

l (loop). Allows you to select the number of times a test will run by pressing the **<esc>** key to end the test.

m (menu). Allows you to select from four menu options which are displayed during the execution of the **t** tests: (a) displays all the menus, (b) stops the help menu from appearing after each command is entered, (c) stops the test menus from being displayed after the **t** command has been typed, and (d) allows the test or help menus to be displayed if a **?** or **b** is typed.

p (parameter). Allows you to change the floppy drive or SIO parameters from their default settings as follows:

a. The following Parameter Menu appears after the **p** is typed.

```
Parameter Menu:

Parameter # Parameter Description

    1         SIO Parameters
    2         Floppy Disk Test Parameters
    3         Return to previous menu

Enter Selection:
```

b. To change the floppy disk test parameters, press **2** to obtain the following Floppy Disk Test Parameters display:

```
Enter the floppy drive speed:
(A) Low Speed     (B) High Speed
Enter:
```

c. To change the SIO parameters, press **1** to obtain the following SIO Parameters display:

```
SIO Parameters

 SIO BOARD  PORT NUMBER  BAUD RATE  STOP BIT  PARITY
     x          x          xxxx        x     on/off
 Is everything correct? (Y,N or <ESC>)
```

d. Press **N**. The following prompt will appear:

```
Please type in the new information followed by <CR>:
SIO Board Number (0,1,2,3,A=All):
```

e. Enter the number of the communications (SIO) PCB that you want to test followed by a <CR>. The following display will then appear:

```
Port Number (0,1,2,...,9,A=All):

Baud Rate (110,300,600,1200,2400,4800,9600,19200):

Stop Bit (1 or 2):

Parity (0 = OFF, 1 = ODD, 2 = EVEN):
```

f. Answer the prompts in the order presented and follow each entry with a <CR>. When the last prompt is answered, the SIO Parameters display will then appear so that you can recheck your SIO parameter changes.

If you made a mistake or need to change any of the entries, repeat steps **a** through **f**.

r (report). Displays the error history of specified tests.

s (summary). Displays the name and number of all tests run, the number of passes run, and the number of errors detected.

t (test). Begins running any tests in the order specified.

u (utility). Displays the utility menu.

? (help). Displays the SDX Field Service Menu.

x (exit). Returns to the Main Menu.

z (debugger). Enters the debugger.

CPU Test Menu

Perform the following procedure to obtain the CPU Test Menu:

1. Press **t** while in the SDX Field Service Menu. The first menu displayed is the CPU Test Menu:

```
      CPU Test Menu:

 Test #     Description                    Status

      1      PROM Checksum Test ..............  Enabled
      2      Cache RAM Test ..................  Enabled
      3      Translation RAM Test ............  Enabled
      4      CPU Timer and Interrupt Test.....  Enabled
      5      Memory Management Unit Test......  Enabled
      6      Numerical Processor Test .........Enabled
      7      Main Memory Parity Test .........  Enabled
      8      Main Memory March Test ..........  Enabled
      9      Main Memory Refresh Test. .......  Enabled

      N      Display Next Test Menu...........  Enabled
      R      Return to Main Menu..............  Enabled
 Enter test numbers, separated by commas, followed by <CR>
 or press <CR> to execute all tests
    press <ESC> to exit
    Enter:
```

2. Type the appropriate command from the CPU Test Menu to perform the following test functions:

   1 PROM Checksum Test. Verifies the firmware for the correct checksum.

   2 Cache RAM Test. Writes data patterns of AAAAh and 5555h into cache RAM, and checks the data integrity word by word.

   3 Translation RAM Test. Fills each of the addresses in the translation RAM with the locations of a 4K page of physical memory. The addresses are written to the translation RAM, read back, and verified.

There are 1Ø24 word entries in the translation RAM. Each word represents a 4K byte page for a total of 16M bytes of system memory. This test runs for about 8 minutes per loop and, during the test, the physical and logical addresses are each displayed as the test runs.

4 CPU Timer and Interrupt Test. Generates an interrupt to the CPU every 3 milliseconds via a software loop and measures the response time. If the response time is excessive, the test will fail. This test also checks the real-time clock (displays the time when the operating system is installed). The following clock verification display will appear:

```
        Real Time Clock Verification:

(A) Display Clock          (B) Set Clock
(C) Exit
Enter:
```

5 Memory Management Unit Test. Tests the ability of the circuitry to detect violations in the access rights to mapped pages of memory. This test first creates an access to memory which is not allowed, and then tests to see whether the violation is detected. If the interrupt indicates that the violation was detected, the test passes.

6 Numerical Processor Test. Tests the optional 8Ø287 numerical processor. The first part of this test involves detection of the numerical processor, followed by initialization if the optional numerical processor is present.

Then the diagnostic has the numerical processor do arithmetic operations on 6 different data types including: word integer (16 bits), short integer (32 bits), long integer (64 bits), packed decimal

(72 bits), short real (32 bits), and long real (64 bits).

7 Main Memory Parity Test. Uses the DMA circuitry to write 8K of random data patterns from the hard disk into 8K of system memory. The data is then read back and checked for parity errors. If there were any errors, a message reports the location of the errors. Next, another 8K block of data from the hard disk is written into the next 8K of system memory. This process is repeated until the entire system memory is tested. This test shows the pass count, and the memory address of any failures.

8 Main Memory March Test. Writes a pattern of AAAA into system memory, reads it back, and verifies. Next, a pattern of 5555 is written, then read back, and verified to ensure that each of the memory cells can store a digital high or low, and are not open or grounded. As the test runs, this message is displayed:

```
Memory March Test In Progress,
press <esc> to abort this Test

Memory Size = xxxx KB
```

If the test fails, this error message is displayed:

```
Failed at memory address = xxxxxx

Expected Data <nn:nn> = xxxx,xxxx
Received Data <nn:nn> = xxxx,xxxx
```

As an example of how the memory march test displays a failure: Assume that the address pins of the RAM at location 21H were shorted together. The test detects the problem and displays the message:

```
Failed at memory address 200060h,

Expected data:  5555h, AAAAh
Received data:  5555h, AAAAh.
```

Next, the test will display:

```
Would you like detection to chip level? (y/n)
```

a. Press **y** and the unit asks for further information:

```
Enter the memory configuration in MB (4,2,1,...)
Enter larger memory configuration first.
```

b. Enter the size of the memory in the memory PCB that you are testing. The location of the failed RAM will be shown by a representation of the PCB. The failed RAM will be shown by two Xs at the failed RAM location.

c. Replace the failed RAM and press **8** to repeat the test.

9 Main Memory Refresh Test. Tests the refresh capability of the dynamic RAMs. This test runs for approximately two minutes. If there are failures, the physical address of the failure is displayed, along with the data pattern which could not be stored at the given location in memory.

File Processor and Controller Board Test Menu

Perform the following procedure to obtain the File Processor and Controller Test Menu:

1. Press **N** and <**CR**> and note that the second menu displayed is the File Processor and Controller Test Menu:

```
File Processor and Controller Board Test Menu

Test # Description                        Status

10      Floppy Random Seek Test           Enabled
11      Floppy Write/ Read Test           Enabled
12      Hard Disk Random Seek Test        Enabled
13      Hard Disk Write/ Read Test        Enabled
14      Streaming Tape Write/ Read Test   Enabled
15      Streaming Tape Append Test        Enabled
16      Concurrent DMA Test               Enabled
17      Parallel Printer Test             Enabled
 N      Display Next Test Menu            Enabled
 R      Return to Main Menu               Enabled

Enter:
```

2. Type the appropriate command from the File Processor and Controller Board Test Menu to perform the following tests:

10 Floppy Random Seek Test. Verifies that the floppy disk drive is working.

The Floppy Random Seek Test does 100 seeks and lists the number of cylinder and head errors at the end of the test. Three retries are allowed. Error messages for this test list the number of seek errors, but not the location of the errors. For example: Assume that the Seek Complete signal at the disk controller (uPD765) was shorted to ground. The following error message would be displayed:

```
operation timeout error (DMA or INT)
cmd=3 cyl=71 head=[0/1/2/3] FFFFh FFFFh FFFFh FFFFh
```

11 Floppy Write/Read Test. Determines if the floppy disk drive can transfer data correctly. To run this test you need a formatted disk that does not contain any valuable data. This test destroys any data on the floppy disk. However, you can also run this as a read-only test by pressing **n** in reply to the prompt at the start of this test:

```
Do you wish to write on the media? (y or n)
```

If the test fails, the error message gives the failing cylinder, head, and sector. The data pattern that was expected to be found, and the data pattern that was actually found is also listed. For example: Assume that the Write Data line for the 7406 on the controller PCB was shorted to ground. This test would then display the error message:

```
Compare err.  cyl.  =Øh head =Øh sec =Øh exp.
=A5h found =FAh
```

12 Hard Disk Random Seek Test. Verifies that the hard disk drive is working. Press the appropriate number from the following display to select which drive is to be tested:

```
Hard Disk Random Seek Test

Ø - Drive Ø
1 - Drive 1
2 - Drive 2

Enter a drive selection from the above
```

The Hard Disk Random Seek Test does 1ØØ seeks and lists the number of hard and soft errors at the end of the test. Three retries are allowed. Error messages for this test list the number of seek errors, but not the location of the errors.

For example: Assume that the Seek Complete signal at the disk controller (WD2Ø1Ø) was shorted to ground. The following error message would be displayed:

```
Total seeks:  1ØØ
Soft errors:  6Ø3
Hard  errors:  2Ø1
```

13 Hard Disk Write/Read and Append Test. This test writes over and destroys any operating system that has been installed on the hard disk (e.g. XENIX). The following prompt will appear to warn you:

```
***THIS TEST WILL ERASE FILES ON THE HARD DISK***

to continue press <CR>, otherwise press <ESC> to
   quit
```

14 Streaming Tape Write/Read Test. Tests the streaming tape drive using all nine tracks. For example: Assume that the Write Data line on the controller integrated circuit was open. Then the following error message will appear:

```
Tape Error ..., 1H unrecoverable data error
```

15 Streaming Tape Append Test. A failed Streaming Tape Append Test is indicated by an error message specifying the location of any unrecoverable data errors. The test first seeks to the beginning of the tape, then erases the tape. Next, the test writes 1 block of test data and a file mark. Then, the test writes another 1 block of test data and goes back to verify the filemark.

16 Concurrent DMA Test. Tests to determine if the DMA can read from hard disk and write to streaming tape at the same time. Ability to transfer is tested, but the data itself is not checked.

Error messages might state that the data was transferred but not received, or display a general

message and then lock up the unit to further input. For example: Assume that an address pin on the communications PCB was floating. The test might display the following error message:

```
Hard Disk (Streaming Tape): DMA or INT Failure
```

17 Printer Test. Tests a parallel printer. This test starts with the following message about the setup:

```
Parallel Printer Verification Test

Please connect printer to the parallel port and
press 'y'...  or <ESC> to quit
```

SIO Test Menu

Perform the following procedure to obtain the SIO Test Menu:

1. Press **N** and **<CR>** and note that the third menu displayed is the SIO Test Menu:

```
SIO Test Menu

Test #  Description                          Status

18      SIO PROM Checksum Test               Enabled
19      SIO Memory March and Refresh Test    Enabled
20      SIO LSI Chips Access Test            Enabled
21      SIO Internal Loopback Test           Enabled
22      SIO Barber Pole Test                 Enabled
23      Echo Visual Verification Test        Enabled
24      SIO External Loopback Test           Enabled
25      SIO Interrupt Vector Test            Enabled
26      SIO DMA Test                         Enabled
27      SIO Worknet Loopback Test            Enabled
28      SIO Timer Test                       Enabled

 N      Display Next Test Menu
 R      Return to Main Menu
```

2. Type the appropriate command from the SIO Test Menu to perform the following tests:

   18 SIO PROM Checksum Test. Checks whether the 8086 can execute the code out of local memory. During this test the PROMs are summed separately so that the individual failing PROM can be isolated. A PROM failure is considered a major failure since the integrity of the firmware is in doubt.

19 SIO Memory March and Refresh Test. Tests the 16K x 4 bit local dynamic RAM memory and refresh on the communications PCB. A data pattern of 5555h is written into memory and verified. Then a data pattern of AAAAh is written into memory and verified. Finally, parity is checked by toggling the parity bit through the memory.

20 SIO LSI Chips Access Test. Ports 0 to port 9 of the SCC integrated circuits (ICs), the DMA IC and the CIO IC registers are tested to see whether they can be accessed (except the port where the modem is connected). Failures in this test are shown as a channel address location, which is to be changed to a message detailing the failing address and port number.

For example, if a data pin of any SCC was open, the error message displayed would be:

```
SIO SCC Chip Register Write/Read Error at Port 2
Port address = 8120h.
```

Or another example: If a data pin of the DMA controller on the communications PCB was open, the error message displayed would be:

```
SIO DMA Chips Register Write/Read Error.
```

21 SIO Internal Loopback Test. Alternates data patterns between 00 and FF, and uses 256 bytes of the above data patterns to test the selected port internal loopback mode at a default baud rate setting of 9600. The maximum number of errors using this method is 511 errors. If you receive

this error count, the internal SIO circuitry is not working.

For example, if a data pin of the SCC1 or SCC2 or SCC3 IC was open, the error message displayed would be **Compare Error = 51Ø** or **Compare Error = 511.**

NOTE

You should test the ports at various baud rates in the following tests 21,22, and 24. To change the baud rate, obtain the Field Service Menu and select the **p** (parameter) command as described under **SDX Field Service Menu** at the front of this section. Then follow the procedure for changing the SIO parameters.

22 Barber Pole Test. Runs a complete set of characters across the terminal screen. This test requires you to connect a terminal to the port that you wish to test. If the test is running correctly, the complete character set streams continuously across the terminal screen. Watch the test carefully for the character set to be complete.

There are no error messages in this test; if there is a hardware problem, the test will not run.

23 Echo Visual Verification Test. Echos whichever character is typed in at a baud rate of 96ØØ. This test also requires you to hook up a terminal to the port that you wish to test. While the test is being run, the following message is displayed:

```
ECHO VISUAL VERIFICATION TEST

1.  press <esc> to abort this test
2.  press <cntrl-a> to show the status
```

Press **2** to display the characters received and those not received:

```
Character(s) received:
Character(s) not received:
```

All the characters and functions received (typed in) are displayed after the **Characters(s) received:** message. The remaining available characters and functions are displayed after the **Characters(s) not received:** message.

24 SIO External Loopback Test. This test requires the use of a loopback connector which connects the DTR/DSR and Tx/Rx data signals as the following prompt informs you:

```
Please plug in a loopback connector before
running this test.
```

Refer to Appendix D for the loopback connector assembly instructions. This test checks the handshake signals, then transmits and verifies 512 bytes through a selected port. An error count is kept and the maximum number of failures is 510.

25 SIO Interrupt Vector Test. Checks the ability of the SIO IC group to respond to different levels of interrupt priorities. Specifically, the SIO Rxbuf received interrupt, the SIO Txbuf empty interrupt, the SIO ext/status interrupt and timer A,B,C interrupt are each tested.

If the test passes, then the flag is greater than zero. But if the test fails, then the flag equals zero. The failed interrupt will be displayed, as well as the port location at which it failed.

26 SIO DMA Test. Uses port 7 in full duplex, internal loopback mode. The DMA IC uses two channels of its four channel capability to first transmit, then receive, a test data pattern. Channel 3 transmits the data, and channel 2 receives the data back from the SCC.

The test data pattern increments between ØØ and FF four times with 256 bytes of test data. The test data is stored in local memory by the DMA IC. Two buffers are used to compare and verify that the test data patterns were transferred correctly. The test also verifies that the DMA end-of-process (EOP) interrupt is working correctly.

Error messages in this test state that data was transmitted but not received. For example, if an address pin on the DMA controller is open on the communications (SIO) PCB, the SIO DMA test displays the message:

```
Errors:  TX data = Ølh - edh ;  Rx data = Øh
```

Other error messages are less complete. For example, if an address pin of the DMA address latch is open, the following error message is displayed:

```
Testing...  Local Parity Error
```

And then the system locks up. Reboot (reset) the system to continue these tests.

27 SIO WorkNet Loopback Test. Tests the ability of port 9 to handle asynchronous and synchronous data link control (SDLC) data transmissions via RS-422. This port must work correctly for the local area network (LAN) to function. Disconnect the WorkNet cable, if one is connected, as the displayed prompt informs you:

```
Please disconnect the WorkNet cable (if connected)
before running this test.
Hit <CR> when ready:
```

This test consists of two parts. In the first part, external clock circuitry clocks data out of port 9 at 1.42 MHz and the asynchronous data transmission mode is tested.

In the second part, an internal clock for port 9 clocks data out at 38.4 kHz and the SDLC data transmissions are tested.

The error messages in this test show the first test as a high speed test and the second test as a low speed test. Error messages also give compare error (CMP) messages and framing errors (a SCC error message in which the SCC internally detects a wrong bit within a SDLC message format). For example, if the ANETCLK buffer (LS125) is removed from the communications (SIO) PCB, the SIO WorkNet Loopback Test fails, and the following error message appears:

```
High speed:  TX empty out = 256
```

Or another example: If the the ANETD lines were grounded, the following error message appears:

```
High speed:  CMP err = 765, framing err = 258,
received char Tout = 95

Low speed :  receive char Tout = 255
```

28 CIO Timer Test. Tests the parallel input/ output device as well as the internal timers. The error message for this test might be:

```
CIO Timer Registers Write/Read Error
                or
CIO Timer Count Down Error
```

File Processor and Controller PCB Circuit Level Test Menu

Perform the following procedure to obtain the File Processor and Controller Board Circuit Level Test Menu:

1. Press **N** and <**CR**> and note that the last menu displayed is the File Processor and Controller Board Circuit Level Test Menu:

```
  File Processor and Controller Board Circuit
  Level Test Menu

Test # Description                          Status

 29      Hard Disk Controller Chip Test     Enabled
 30      File Processor SCSI Chip Test      Enabled
 31      File Processor Timer Test          Enabled
 32      File Processor PROM Checksum Test  Enabled
 33      Printer Port Loopback Test         Enabled
 34      Tape Controller Chip Set Test      Enabled
 35      File Processor Interrupt Test      Enabled
 36      Ping Pong Buffer Test              Enabled
 37      DMA Burst Logic Test               Enabled
  N      Display Next Test Menu
  R      Return to Main Menu
```

2. Type the appropriate command from the File Processor and Controller Circuit Level Test Menu to perform the following tests:

   29 Hard Disk Controller Chip Test. This test has two parts. The first part writes an 01 data pattern into the registers of the Western Digital 2010 IC. Then, the pattern is read back and compared to ensure that the two patterns match.

   The pattern is rotated and the previous procedure is repeated for all possible bit positions in the pattern.

   The second part tests the drive select circuitry. The first part of this test involves attempting to select a non-existent drive 3. If the status shows any drive selected, an error will be displayed showing that drive as being selected. The test then tries to select an installed drive, and gives an error message if any other drive was mistakenly selected.

30 File Processor SCSI Chip Test. Tests the 5385E SCSI protocol controller on the file processor PCB. First the 5385E is reset, and then the status of the diagnostic status register is read. The 5385E SCSI protocol controller must pass its internal power-up tests which include: (1) attempting an unconditional branch, (2) setting and resetting the data register full status bit in the interrupt register, (3) testing initial conditions and initial command registers, (4) resetting the internal diagnostic flag, and (5) flushing several bytes of data through the data paths of the IC.

If the previous sequence of tests passes, the test goes on to try writing and then reading data patterns of 55 and AA into the data registers.

31 File Processor Timer Test. Tests the file processor timing with the following messages:

```
checking channel 0 counter for all bits on...
checking channel 0 counter for all bits off...
checking that channel 0 doesn't count too slow
checking that channel 0 doesn't count too fast
```

32 File Processor PROM Checksum Test. Sums the PROMS in the file processor PCB, and checks for correct checksums.

33 Printer Port Test. This test requires a printer port loopback connector to be placed over the loopback port as the following prompt informs you:

```
Checking for the printer port loopback connector...
Waiting to run test (type y for yes, any key to
skip)...
```

This test checks the printer port signals using the loopback connector to loop back the signals so they can be read. Refer to Appendix D for instructions on assembling the parallel printer loopback connector.

If you do not connect a loopback connector, the test fails with the following error message:

```
ERROR:  printer data line x or x was logic high
and should have been logic low.
```

34 Tape Controller Chip Set Test. Initializes the tape LSI controller, then resets, and the status of the controller board is read. The test begins with the following prompt:

```
Sending reset to the tape controller.
```

If this process is working correctly you should hear the streaming tape unit reset. If an error was detected, an error message will be displayed, and if not the test will continue.

Next, the test sends a self test command 1 to the tape controller. Self test 1 consists of four parts: (1) LSI controller chip test, (2) 16K RAM chip buffer test, (3) data separator logic test, and (4) 8155 PIA chip test.

35 File Processor Interrupt Test. Saves the firmware interrupt vectors and installs the test routine vectors. Next, the first interrupt to be tested is the channel Ø interrupt vector followed by the hard disk, SCSI, tape, DMA, and floppy interrupt.

Each of these interrupts must have been successfully acknowledged, and the results are displayed. At the end of the test, the firmware interrupt vectors are re-installed and the test is finished.

36 Ping Pong Buffer Test. Tests a pair of sector buffers for the ability to handle hard disk and SCSI traffic. The ping-pong buffer's principle advantage is its capacity to provide continuous data transfer by allowing one buffer to load while the other is unloading data.

This test consists of two parts. First, a 512-word data pattern is set up in system memory and a DMA transfer is performed from the system memory to the ping-pong buffer.

If an error occurs, a message is displayed and the test stops. Then the system memory segment is cleared.

Next, a SCSI-done (SCSIDONE) signal is issued to reset the buffer sequencer. A DMA transfer is performed from the ping-pong buffer to system memory. The contents of system memory is verified with the original 512-word data pattern.

37 Burst Logic Test. Verifies the ability of the burst logic circuitry to limit the file processor's use of the system bus. This test consists of two parts. First, a 512-word DMA transfer is performed with the burst logic disabled from system memory to the ping-pong

buffer. If an error occurs, a message is displayed and the test stops. Then the system memory segment is cleared.

Next, a DMA transfer is performed, with the burst logic enabled, from the ping-pong buffer to system memory. The burst-on time is set for 64 words and the transfer is terminated after one burst on/off cycle. The contents of system memory is verified to be a pattern with the same length as the burst-on time.

Table 5-10. SDX Trouble Analysis

Test	Error Message	Probable Cause
		CPU and System Memory PCBs
(1) PROM Checksum	(high/low/both) **byte**(s) **of CPU PROM failed**	PROMs (21C-A, 21C-B)
(2) Cache RAM	**Cache failed at 0010:x**	Cache RAM (23C-26C) Tag RAM (1A-4A) Cache data buffer (23B-25B, 28B) Tag data buffer (6A, 11A)
(3) Translation RAM	**Failed at Translation RAM Location = 40xxxxh (logical page = xxxxh) Memory Address = xxxxxxh (physical page = xxxxh Expected Data = xxxxh Received Data = xxxxh**	Translation RAM (8C-10C) System memory Table data buffers (12A, 16C)

Table 5-10. SDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
		CPU and System Memory PCBs (Cont.)
(4) CPU Timer and Interrupt	**Clock chip** (address/ data) **failure**	Clock (20A)
	Clock chip internal RAM failure	Clock (20A)
	Clock chip counter/ interrupt failure	8259 interrupt controller (21D) Clock (20A)
(5) Memory Management Unit	**Wrong exception interrupt occurred in response to MMU violation**	80286 processor (16B) 8259 interrupt controller (21D)
	General protection exception did not occur	80286 processor (16B) 8259 interrupt controller (21D)
(6) Numerical Processor	**Arithmetic error from numerical processor**	80287 processor (12B)
(7) Main Memory Parity	**Hard disk read error**	WD2010 controller (6C) Hard disk drive **NOTE** Some early systems used the hard disk for random data. If this error message appears, test the file processor/controller hard disk circuitry.

Table 5-10. SDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
		CPU and System Memory PCBs (Cont.)
(7) Main Memory Parity (Cont.)	**Memory parity error**	Parity checker/generators (11E-14E, 15E) Data buffers (12F-17F) System memory RAM
(8) Main Memory March	**Failed at memory address = x**	System memory RAM Address buffers (10C, 20C, 10E, 10F, 20F, 20J) Data buffers (12F-17F)
	The RAM I.C. in the xxx memory board row x column x of main memory does not contain the expected data	System memory RAM Address buffers (10C, 20C, 10E, 10F, 20F, 20J) Data buffers (12F-17F)
		Communications (SIO) PCB
(18) SIO PROM Checksum	**SIO PROM checksum error** **Odd Checksum = xxxxh** **Even Checksum = xxxxh**	SIO PROM (20C-A or 20C-B) Address buffers (13F
(19) SIO Memory March and Refresh	**SIO local memory fail at x = xh** **Expected Data = xxxxh** **Received Data = xxxxh**	Address buffers (16F, 17F, 19E) RAM (2J-9J, 11J-18J)
	SIO local memory parity error at x	Memory parity (1J, 10J) RAM (2J-9J, 11J-18J) Address buffers (16F, 17F, 19E)

Table 5-10. SDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
		Communications (SIO) PCB (Cont.)
(20) SIO LSI Chips Access	**SIO DMA chip registers write/read error**	DMA controller (17D) Address latch (13D, 15F) Local bus control (15D, 16C, 20C, 17C)
	SIO SCC chip registers write/read error at port x (Port Address = xxxxh	SCCs (1B, 3B-6B)
	SIO CIO chip registers write/read error at port x	CIO (2B)
(21) SIO Internal Loopback	**Receive character time-out at the xxxx character**	SCCs (1B, 3B-6B, 1A-10A)
	Compare error = x	SCCs (1B, 3B-6B)
(24) SIO External Loopback	**RTS/CTS handshake not responding**	SCCs (1B, 3B-6B, 1A-10A) No loopback connector
	Receive character time-out at the xxxx character	SCCs (1B, 3B-6B, 1A-10A) No loopback connector
	Compare error = x	SCCs (1B, 3B-6B)
	Handshake signal changed unexpectedly xx time(s)	SCCs (1B, 3B-6B, 1A-10A)

Table 5-10. SDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
		Communications (SIO) PCB (Cont.)
(25) SIO Interrupt Vector	**Port x Tx interrupt fail**	SCCs (1B, 3B-6B, 1A-10A) SIO memory (interrupt vector area)
	Port x Rx interrupt fail	SCCs (1B, 3B-6B, 1A-10A) SIO memory (interrupt vector area)
	Port x ext/status interrupt fail	SCCs (1B, 3B-6B, 1A-10A) SIO memory (interrupt vector area)
	Timer xx interrupt fail	CIO (2B)
(26) SIO DMA	**SIO DMA Test Has Compare Errors (DMA Tx and Rx 1K Byte Data)** **1. Tx Data = xxxxh Rx Data = xxxxh** **2. Tx Data = xxxxh Rx Data = xxxxh**	DMA controller (17D) SCCs (1B, 3B) SIO memory (Rx or Tx buffers) (1A-6A)
	DMA EOP interrupt fail	DMA controller (17B) CIO (2B)
(27) SIO WorkNet Loopback	**High speed WorkNet loop-back (transmit 768 bytes) Compare error = x**	DMA controller (17D) SCC0 (1B) RS-422 loopback ckt. (3A, 4A, 1C) External clock (2E, 4E, 3D, 4C)

Table 5-10. SDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
		Communications (SIO) PCB (Cont.)
(27) SIO WorkNet Loopback (Cont.)	**High speed WorkNet Parity error=x**	DMA controller (17D) SCC0 (1B) RS-422 loopback ckt. (3A, 4A, 1C)
	High speed WorkNet Overrun error = x	DMA controller (17D) SCC0 (1B) RS-422 loopback ckt. (3A, 4A, 1C) External clock (2E, 4E, 3D, 4C)
	High speed WorkNet Framing error = x	DMA controller (17D) SCC0 (1B) RS-422 loopback ckt. (3A, 4A, 1C) External clock (2E, 4E, 3D, 4C)
	High speed WorkNet DTR timeout = x	DMA controller (17D) SCC0 (1B) RS-422 loopback ckt. (3A, 4A, 1C) Carrier sense ckt. (1D, 2D, 8D)
	High speed WorkNet Tx empty timeout = x	DMA controller (17D) SCC0 (1B) RS-422 loopback ckt. (3A, 4A, 1C) External clock (2E, 4E, 8D, 3D, 4C)
	High speed WorkNet Receive character timeout = x	SCC0 (1B) RS-422 loopback ckt.

Table 5-10. SDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
		Communications (SIO) PCB (Cont.)
(27) SIO WorkNet Loopback (Cont.)	**Low speed WorkNet loop-back(transmit 256 bytes) CRC error = x**	SCC0 (1B) RS-422 loopback ckt.
	Low speed WorkNet Compare error = x	SCC0 (1B) RS-422 loopback ckt.
	Low speed WorkNet Overrun error = x	SCC0 (1B) RS-422 loopback ckt.
	Low speed WorkNet DTR timeout = x	SCC0 (1B) RS-422 loopback ckt. Carrier sense ckt. (1D, 2D, 8D)
	Low speed WorkNet Tx empty timeout = x	SCC0 (1B) RS-422 loopback ckt.
	Low speed WorkNet Underrrun timeout = x	SCC0 (1B) RS-422 loopback ckt.
	Low speed WorkNet Receive character timeout = x	RS-422 loopback ckt. SCC0 (Port 9) (1B)
(28) CIO Timer	**CIO timer registers write/read error**	CIO (2B)
	CIO timer countdown error	CIO (2B)

Table 5-10. SDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
		File Processor and Controller PCBs
(10) Floppy Random Seek	**Operation timeout error (DMA or INT)**	Floppy disk Floppy drive Circuitry between floppy and DMA controllers
(11) Floppy Write/Read	**Compare error cyl= x, head= x sector= x**	Floppy disk Floppy drive Circuitry between floppy and DMA controllers System memory
	(read/write) **error: cyl = x, head = x, sector = x**	Floppy disk Floppy drive Circuitry between floppy and DMA controllers System memory
	Diskette is write protected	Protected floppy disk Floppy drive
(12) Hard Disk Random Seek	**Operation timeout error** (DMA or INT)	Hard disk Circuitry between WD2010 and DMA controllers
(13) Hard Disk Write/ Read	**No hard disks detected** **Recalibration error**	Hard disk power Hard disk

Table 5-10. SDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
		File Processor and Controller PCBs (Cont.)
(14) (15) Streaming Tape Write/ Read and Append	**Unrecoverable data error**	Streaming tape Streaming tape drive CPU 8031 tape controller (21A) File processor DMA controller (21D)
	Cartridge is write protected	Streaming tape write protected
	Cartridge is not in place	Tape drive Tape missing
	Read error, no data detected	Tape drive CPU 8031 tape controller (21A)
(16) Concurrent DMA	**Streaming tape error**	Tape missing Streaming tape Streaming tape drive
	Hard disk DMA or INT error	DMA controller (21D) WD2010 controller (6C) Hard disk
(29) Hard Disk Controller	**Verify error checking 2010 sector** (count/ number) **register**	WD2010 controller (6C) WD2010 command or data transceivers (6E, 7E) WD2010 local bus

Table 5-10. SDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
		File Processor and Controller PCBs (Cont.)
(29) Hard Disk Controller (Cont.)	**Status port failed to detect a select for drive**	Ext.SDH latch (5E) Drive select drivers (3C, 9C, 12E, 14E) System backplane (pins P1-A27, A29, C27) Hard disk Controller status port
	Detected drive select	Ext. SDH latch (5E) Drive select drivers (3C, 9C, 12E, 14E) System backplane (pins P1-A27, A29, C27) Hard disk Controller status port
	External sdh register written with 30 hex to select non-existent drive 3, status port detected a select for drive	Ext. SDH latch (5E) Drive select drivers (3C, 9C, 12E, 14E) System backplane (pins P1-A27, A29, C27) Hard disk Controller status port
(30) File Processor SCSI Chip	**Unconditional branch failure in internal sequencer**	SCSI controller (1C) SCSI command or data transceivers (2B, 4A, 3A, 7A, 9A, 7B, 10C, 10A)
	Data register full bit failure in interrupt register	SCSI controller (1C) SCSI command or data transceivers (2B, 4A, 3A, 7A, 9A, 7B, 10C, 10A)

Table 5-10. SDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
		File Processor and Controller PCBs (Cont.)
(30) File Processor SCSI Chip (Cont.)	**Initial conditions in wrong state**	SCSI controller (1C) SCSI command or data transceivers (2B, 4A, 3A, 7A, 9A, 7B, 10C, 10A)
	Initial command bits **incorrect**	SCSI controller (1C) SCSI command or data transceivers (2B, 4A, 3A, 7A, 9A, 7B, 10C, 10A)
	Diagnostic flag failure	SCSI controller (1C) SCSI command or data transceivers (2B, 4A, 3A, 7A, 9A, 7B, 10C, 10A)
	Data turnaround failure	SCSI controller (1C) SCSI command or data transceivers (2B, 4A, 3A, 7A, 9A, 7B, 10C, 10A)
	Unused error bit setting in status register	SCSI controller (1C) SCSI command or data transceivers (2B, 4A, 3A, 7A, 9A, 7B, 10C, 10A)
	SCSI chip status shows self diagnostic not complete	SCSI controller (1C) SCSI command or data transceivers (2B, 4A, 3A, 7A, 9A, 7B, 10C, 10A)

Table 5-10. SDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
		File Processor and Controller PCBs (Cont.)
(30) File Processor SCSI Chip (Cont.)	**SCSI auxiliary status register not reset**	SCSI controller (1C) SCSI command or data transceivers (2B, 4A, 3A, 7A, 9A, 7B, 10C, 10A)
	SCSI interrupt not detected	8259 interrupt controller (8H) SCSI controller (1C) SCSI interrupt line to 8259 interrupt controller Interrupt latch or gate (25C and 4B)
	SCSI status shows command not complete	8259 interrupt controller (8H) SCSI controller (1C) SCSI interrupt line to 8259 interrupt controller Interrupt latch or gate (25C and 4B)
	SCSI data register not full after completion of diagnostic command	8259 interrupt controller (8H) SCSI controller (1C) SCSI interrupt line to 8259 interrupt controller Interrupt latch or gate (25C and 4B)

Table 5-10. SDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
		File Processor and Controller PCBs (Cont.)
(30) File Processor SCSI Chip (Cont.)	**Internal turnaround failure with data pattern (AA/55)**	8259 interrupt controller (8H) SCSI controller (1C) SCSI interrupt line to 8259 interrupt controller Interrupt latch or gate (25C and 4B)
	SCSI chip unknown status error code	8259 interrupt controller (8H) SCSI controller (1C) SCSI interrupt line to 8259 interrupt controller Interrupt latch or gate (25C and 4B)
	SCSI chip (initial/final) **turnaround miscompare failure**	SCSI controller (1C) SCSI command or data transceivers (2B, 4A, 3A, 7A, 9A, 7B, 10C, 10A)
	SCSI chip turnaround bad parity failure	SCSI controller (1C) SCSI command or data transceivers (2B, 4A, 3A, 7A, 9A, 7B, 10C, 10A)
	SCSI data register returned incorrect data pattern	SCSI controller (1C) SCSI command or data transceivers (2B, 4A, 3A, 7A, 9A, 7B, 10C, 10A)

Table 5-10. SDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
		File Processor and Controller PCBs (Cont.)
(31) File Processor Timer	**Channel 0 counter failed to** (set/clear) **all bits**	8254 timer (25B) Clock divider (33B)
	Channel 0 counter was too (slow/fast) **or problem with timer interrupt logic**	8254 timer (25B) Clock divider (33B)
(32) File Processor PROM Checksum	**File processor** (odd/even) **checksum error**	PROM (9H, 33D)
(33) Printer Port	**Data strobe, input prime, or printer status acknowledge stuck**	Printer port pins shorted or open Loopback connector Printer drivers (16A, 17A) Printer data port (19A) Printer status port (20A)
	Input prime * or printer status acknowledge stuck high	Printer port pins shorted or open Loopback connector Printer drivers (16A, 17A) Printer data port (19A) Printer status port (20A)

Table 5-10. SDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
		File Processor and Controller PCBs (Cont.)
(33) Printer Port (Cont.)	**Printer data line** (1 or 2/3 or 4/5 or 6/7 or 8) **logic** (high/low), **should be logic** (low/high)	Printer port pins shorted or open Loopback connector Printer drivers (16A, 17A) Printer data port (19A) Printer status port (20A)
(35) File Processor Interrupt	**Timer channel 0 interrupt not detected**	8259 interrupt controller (8H) 8254 timer (25B) Interrupt line from timer to interrupt controller
	Hard disk interrupt not detected	WD2010 controller (6C) 8259 interrupt controller (8H) Interrupt line from WD2010 to 8259 interrupt controller (8H) on file processor PCB Interrupt line driver (10C) on controller PCB
	Hard disk controller is busy and unable to accept a command	WD2010 controller (6C)

Table 5-10. SDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
		File Processor and Controller PCBs (Cont.)
(35) File Processor Interrupt (Cont.)	**SCSI status shows self diagnostic not complete**	SCSI controller (1C)
	SCSI interrupt not detected	SCSI controller (1C) Interrupt line from SCSI controller to 8259 interrupt controller Interrupt latches and gates (4B and 25C) on file processor PCB
	Unable to test the tape interrupt logic	Unable to perform read tape status command
	Floppy disk controller interrupt not detected	Floppy disk controller (8C) Interrupt line to 8259 interrupt controller from file processor to controller PCB 8259 interrupt controller (8H) on file processor PCB
	DMA controller interrupt not detected	8259 interrupt controller (8H) DMA controller (21D) DMA interrupt line
	Hot interrupt detected	8259 interrupt controller (8H) on file processor PCB
	Interrupt controller mask register verify error with data = (00/FF)	8259 interrupt controller (8H) on file processor PCB

Table 5-10. SDX Trouble Analysis (Cont.)

Test	Error Message	Probable Cause
		File Processor and Controller PCBs (Cont.)
(36) Ping-Pong Buffer	**DMA controller operation not complete**	DMA controller (21D) DMA bus
	Data miscompare on transfer from ping-pong buffer	DMA controller (21D) Ping-pong buffer (7D, 4D, 5D, 3D, 2D, 1D, 6B, 9D, 9C, 6D, 8D, 8C, 7C, 8B, 13A, 12D, 12C, 14D, 2H, 13D, 11D, 11A, 11C)
	DMA error	DMA controller (21D)
(37) DMA Burst Logic	**Burst** (on/off) **logic error**	Burst logic ICs (31B, 32B, 26D) 8254 timer controller (25B)
	DMA controller operation not complete	DMA controller (21D)

Debugger Tests

The debugger test program is a development tool included in the monitor for troubleshooting user programs by allowing the user to single step a code segment and control execution by means of a breakpoint.

A breakpoint allows the user to control execution by placing a software interrupt in the object code at locations specified by the user.

The breakpoint transfers control to the debugger and allows the user to replace the original object code at any location and to view the current status.

CPU Debugger Commands

The CPU debugger commands are:

A	Alter Memory
B	Breakpoint
C	CPU Register
D	Display Memory
F	Fill Memory
G	Go
H	Go to SIO Monitor for Remote Downloading
I	Input From Port
L	Remote Download
M	Move Memory
O	Output To Port
R	Read From Device
S	Single Step
U	CATS Download
W	Write To Device
Z	Pass Control To SIO Monitor
?	Display Command Menu

<esc> Repeat the previous request

NOTE

The following conventions are used in the debugger command description:

- Underscore (_) denotes a space in the command lines.
- Unless otherwise indicated, all values are specified in hexadecimal form.
- <CR> denotes a carriage return.
- Upper or lower case letters are accepted.
- All memory addresses are six hexadecimal digits long.
- All I/O addresses are four hexadecimal digits long.

The CPU debugger commands are executed as follows:

A Alter Memory

This command allows the user to change the memory contents beginning with the given address.

Syntax:

```
a_xxxxxx_hh_hh_..._..<CR>

a:       Alter command
xxxx:    Beginning memory address to be altered
hh:      Hex byte values
. . .:   Up to 22 bytes at a time
```

B Display/Change/Clear Breakpoint

This command allows the user to either view, change, or clear the current breakpoint address.

Syntax:

```
b<CR>          <Display breakpoint address>
b_xxxxxx<CR>   <Set breakpoint to a memory
               address>

bc<CR>         <Clear all breakpoints 1 & 2>
bc1<CR>        <Clear breakpoint 1>
bc2<CR>        <Clear breakpoint 2>

b:       Breakpoint command
xxxxxx:  Breakpoint memory address
```

C CPU Register Contents

This command allows the user to either view or change current register contents.

Syntax:

```
c<CR>          <Display all register contents>
crr_hhhh       <Change particular register>
cad_xxxxxx     <Change next execution address
               (registers cs and ip together)>

c:       Register command
rr:      Only one register of the following is
         allowed: (ax, bx, bx, dx, di, si, bp,
         sp, cs, ds, es, ss, mw, ip, fl)
hhhh:    Word value
xxxxxx:  Six digit memory address
```

D Display Memory Contents

This command displays the memory contents starting with the given address. It will display at least 16 bytes, or one page at a time.

Syntax:

d_xxxxxx_ll<CR> <Display memory>

d: Display memory command
xxxxxx: Beginning memory address to be displayed

ll: Byte count (module 16)

For example:

d_xxxxxx<CR>:

Display one line (16 bytes) of memory data.

d_xxxxxx_ff<CR>:

Display one screen full of memory data.

d_xxxxxx_ffff<CR>:

This command displays the entire 65K bytes of memory data on a full-screen and pause. Pressing the spacebar will continue to display another full screen of memory data. However, entering any other keys will complete the command and return to the debugger. Also, the display will wrap around on the same segment.

F Fill Memory Contents

This command fills the memory contents starting at the given address with the given byte count.

Syntax:

f_xxxxxx_llll_hh<CR> <Fill memory>

f: Fill memory command
xxxxxx: Beginning memory address to be filled
llll: Byte count (0000=maximum of 64K bytes)
hh: Hex character

G Go

This command allows user to start executing program based on the values in the code segment (cs) and instruction pointer (ip) registers.

Syntax:

```
g<CR>   <Go/Start execution>
```

H Go to SIO Monitor for Remote Downloading

This command is for remote diagnostics.

I Input From Port

This command allows the user to read in the word value of the port, designated in the given address.

Syntax:

```
i:      Input port command
xxxx:   Port address

is_xxxx<CR>      <Input from system port>
ilc_xxxx<CR>     <Input from CPU local port>
ilf_xxxx<CR>     <Input from file processor local port>
```

L Remote Download

This command is for remote diagnostics.

M Move Memory

This command moves memory data from a source to any destination in system memory.

Syntax:

```
m:  xxxxxx_yyyyyy_zzzz
```

O Output To Port

This command allows the user to output a word value to the port designated by the given address.

Syntax:

```
o:      Output port command
xxxx:   I/O port address
yyyy:   Word value to be written
yy:     Byte value to be written

os_xxxx_yy<CR>          <Output to system port>
olc_xxxx_yyyy<CR>       <Output to CPU local port>
olf_xxxx_yyyy<CR>       <Output to file processor
                         local port>
```

R Read From Device

This command allows the user to read in block(s) of data from any mass-storage device supported by the file processor.

Syntax:

```
rf:     Read floppy (regular speed) command
rfl:    Read floppy (low speed) command
rfh:    Read floppy (high speed) command
rh:     Read hard disk command

rt:     Read tape command

rf_xxxxxx_tr_hd_se_nm   <Read from floppy
                         (regular speed)>
rfl_xxxxxx_tr_hd_se_nm  <Read from floppy (low
                         speed)>
rfh_xxxxxx_tr_hd_se_nm  <Read from floppy (high
                         speed)>
xxxxxx: Beginning memory address where disk data
        is to be stored

tr:     Track number (hexadecimal)
hd:     Head number (0-1)
se:     Beginning sector number (floppy starts
        at sector 1, but enter 0 for compati-
        bility with hard disk)
```

nm: (Optional) Sector count (up to 9 for low speed and up to 15 for high speed, but default to be one sector)

rh_xxxxxx_dh_ch_cl_se_nm <Read from hard disk>

rh: Read hard disk command

xxxxxx: Beginning memory address where disk data is to be stored
d: Drive number (0-3)
h: Head number (0-7)
ch: Cylinder number (high byte in hexadecimal)
cl: Cylinder number (low byte in hexadecimal 0-7)
se: Beginning sector number (hard disk starts at sector 0)
nm: (Optional) Sector count (up to 16, but default to be one sector)

For example:

rh_001000_01_00_20_00_10,<CR>:

Read in hard-disk drive 0, head 1, cylinder 32, head 1, sector 0 to 15, and store the data in buffer area starting at location 1000h.

rt_xxxxxx_llll <Read from tape>

rt: Read tape command
xxxxxx: Beginning memory address where tape data is to be stored
llll: Number of blocks

S Single Step

This command allows the user to execute one instruc tion, pointed by code segment (cs) and instruction pointer (ip) registers, then return to debugger.

Syntax:

s<CR>

U CATS Download

This command is for Altos computer assisted test system (CATS) downloading.

W Write To Device

This command allows the user to write in block(s) of data from any mass-storage device supported by the file processor.

Syntax:

```
wf:     Write floppy (regular speed) command
wfl:    Write floppy (low speed) command
wfh:    Write floppy (high speed) command
wh:     Write hard disk command

wt:     Write tape command
wp:     Write printer command
```

All syntaxes are the same as the r command, in addition to the write printer command as follows:

```
wp_xxxxxx_llll   <Write printer command>

xxxxxx: Beginning memory address where tape data
        is to be
llll:   Block number
```

Z Pass Control to SIO Monitor

This command passes control to the SIO Monitor.

? Display Command Menu

This command displays the debugger menu and its required syntaxes.

Syntax:

```
?<CR>   <Display debugger menu>
```

Communications Debugger Commands (Software Mode)

The communications debugger commands (software mode) are:

A	Alter Memory
C	Set Registers
D	Display Memory
F	Fill Memory
G	Go and Execute User Code
H	Remote Download
I	Input From Port
L	Remote Load to CPU
O	Output to Port
R	Hex Download
S	Single Step
U	Users Console into Memory Buffer
W	Send the W Character to Ports Ø and 1 (FCC RF Test)
X	Execute Users Memory Buffer
Z	Go to Main CPU Monitor
?	Display Command Menu

<BREAK> Switch to hardware mode

The communications debugger commands (software mode) are executed as follows:

A Alter Memory

Syntax:

a<address> <data> <data> <data>...<data> <CR>

Alter local memory. Enter data in hexadecimal. No delimiter is needed between the command character and the address. All other parameters need a delimiter.

C Set Registers

Syntax:

c|cxx <data> <CR>

Set or display the users CPU registers. At power-up these are all set to the Ø default value. A hexa decimal download will set the CS:IP if there is a start record. The following is a list of the registers:

CS, IP, AX, BX, CX, DX, FL, SS, SP, BP, DS, SI, ES, and DI.

To display all the registers just type C <CR>.

To change a register, type C followed by the register name from above, a space character, then the hexa decimal data, and finally a cursor return. Enter data in hexadecimal. No delimiter is needed between the command character and the register name. The data needs a delimiter.

D Display Memory

Syntax:

d<address> <length> <CR>

Display local or system memory. Length can be any hexadecimal number from Ø to FFFF, where Ø = 65536. A <control+D> will repeat the command until a <control+C>. System memory can be displayed from the window at 8ØØØØØ to BFFFF. The window page register can be changed by outputing to port 8178. No delimiter is needed between the command character and the address. The length needs a delimiter.

F Fill Memory

Syntax:

f<address> <length> <data> <CR>

Fill local or system memory. Same as hardware mode.

G Go and Execute User Code

Syntax:

g<CR>

Go from the CS:IP setup in the users registers.

NOTE

You can set as many breakpoints as you like by replacing the code with the CC instruction.

H Remote Download

Proprietary format. Used for remote diagnostics.

I Input From Port

Syntax:

i<port> <CR>

Input from local or system port. A <control+I> will input continuously until stopped by a <control+C>. No delimiter is needed between the command character and the port address.

L Load to CPU

Proprietary format. Used for remote diagnostics.

O Output to Port

Syntax:

o<port> <data> <data>... <data> <CR>

Output to local or system port. A <control+O> will output continuously until stopped by a <control+C>. No delimiter is needed between the command character and the port address. The data needs delimiters.

R Hex Download

Syntax:

h<TTYport> <CR>

Hexadecimal file download. Uses Intel hexadecimal file format. The TTY port can be any number from Ø to 9, where Ø is the console.

S Single Step

Syntax:

s<CR>

Single step one instruction. The CS:IP must already be pointing to some valid users code. Instructions that move to/from the segment registers may cause the next instruction to be executed automatically. There is nothing the monitor can do about this and it is not a bug.

U Users Console Into Memory Buffer

Syntax:

u<address> <CR>

W Send the W Character to Ports Ø and 1.

Syntax:

w<CR>

This is an FCC test to check for proper RF noise levels. This is not a debug command. To stop this test type <control+C>>.

X Execute Users Memory Buffer

Syntax:

x<address> <CR>

Z Go to Main CPU Monitor

If the main CPU is running, this command will appear in the menu. If there are problems with the main CPU, then this command will not appear in the menu. If this command is functioning, control will pass to the main CPU.

Communications Debugger Commands (Hardware Mode)

The communications debugger commands (hardware mode) are:

A	Strobe All I/O Integrated Circuits
B	Set Baudrate
C	Checksum Memory
D	Display Memory
F	Fill Memory and Verify
H	High-Speed DMA Test
I	Input From Port
L	Serial Port Loopback Test (requires loopback connectors)
N	Network Test
O	Output To Port
S	SCC Recovery Exerciser (scope loop)
T	Timer Exerciser
U	Enter User-Defined Macro
W	Memory Write Without Verify
X	Execute User-Defined Macro
?	Display Command Menu

<BREAK> Switch to software mode

<control+C> Aborts any test and returns to command level.

<control+S> Suspends printout.

<control+Q> Resumes printout.

NOTE

Most commands will repeat if entered as a control character. A <control+C> will stop the test.

The communications debugger commands (hardware mode) are executed as follows:

A Strobe All I/O Integrated Circuits

This command does a sequential INP , NOP, OUT to the base port of all the I/O integrated circuits (ICs) on the local bus. Then repeats until interrupted by <esc>. The NOP ensures that this test does not violate any recovery specifications.

B Set Baudrate

Syntax:

b<channel> <baudrate> <CR>

This command sets up the baudrate where <channel> ranges from Ø to 9 and <baudrate> can be any value from 1ØØ to 99999 baud.

C Checksum Memory

Syntax:

c<address> <length> <CR>

This command checksums memory from <address> up to and including <length>. The hexadecimal values of each pass of the checksum is displayed across the screen.

D Display Memory

Syntax:

c<address> <length> <CR>

This command displays the contents of memory <address> up to and including <length>. Both hexa decimal and ASCII values are displayed at 16 bytes per line.

F Fill Memory and Verify

Syntax:

f<address> <length> <data> <CR>

This command fills memory from <address> through and including <length> with <data>. The command will write then verify a byte at a time. If <data> = I, then an incrementing byte pattern (starting at Ø) is used.

H High-Speed DMA Test

Syntax:

h<channel> <CR>

This command sets up <channel> to move bytes to/from the associated SCC IC.

HØ uses DMA channel Ø and SCCØ-A to transmit data at 1.4M baud and transmits the contents of RAM from Ø to 64K.

Hl uses DMA channel 1 and SCCØ-B to receive data at 96ØØ baud. The DMA byte count is set to 1ØØØh bytes and received data is placed in memory starting at 1ØØØh.

H2 uses DMA channels 2 and 3, and SCCl-A in a fullduplex interrupt driven configuration. This test places the SCC in an internal loopback mode which transfers 1ØØØh bytes from memory at location 2ØØØh to the SCCl-A transmitter. Then the 1ØØØh bytes are looped back in the SCC, direct-memory accessed back to memory starting at location 3ØØØh, and compared to verify that the transfer back to memory was accomplished properly.

Once started, this test runs until stopped by entering H. (HØ, Hl, and H2 can all be running simultaneously.) These tests are intended to check hardware timing.

I Input From I/O Port

Syntax:

i<port> <CR>

This command inputs and displays a byte from <port>.

NOTE

Problems may result if input for this test is done from the console port. Unusual results may occur by reading ports that have interrupts enabled.

L Loopback Test

Syntax:

l<channel> <CR>

This test requires an external loopback connector (wired TxD to RxD, and DTR to DSR) to function properly. <channel> can range from Ø through 9. This test outputs a barber-pole pattern on the Tx register and compares the results from the Rx register. (The baud rate is not preset to any particular value.) The RS-232 DSR output is also wiggled and the RS-232 DTR line is checked for the proper response.

NT Network Test
NR

Syntax:

NT<data> <CR>
NR <CR>

NR sets up the DMA controller and SCCØ-A to receive a 1K synchronous data link communications (SDLC) packet

(buffered at location 3000h) from another communications PCB. Once the packet is received, it is retransmitted back to the sender and no error checking is performed.

NT <data> fills 1K of memory (starting at location 3000h) with <data> and sets up the DMA controller and SCC0-A to transmit 1K SDLC packets to another communications PCB.

After the SDLC packet is transmitted, the SCC0-A and DMA controller are reprogrammed to receive a 1K packet (buffered at location 4000h) returned by the second communications PCB and compared to the buffer at location 3000h. Errors are logged, but only reported when <control+C> stops the test.

<data> may be I (which creates an incrementing pattern), a byte, or a word value. A word value of DB6C is recommended since this is a worst-case data pattern. If <data> is not specified, the buffer at location 3000h is used as is.

O Output To I/O Port

Syntax:

o<port> <data> <data> <data>.....<CR>

This command outputs from 1 to 16 bytes of <data> to the port specified by <port>.

NOTE

A carelessly done output can make the console port unusable. It may be necessary to reset to correct the problem.

S SCC Recovery Exerciser

Syntax:

s<port> <CR>

This command performs a high-speed group of 3 reads, and then 3 writes of the specified I/O port. The data is treated as don't cares.

T Timer Exerciser

Syntax:

t<timer> <count> <CR>

This command loads timer <timer>, which ranges from 1 to 3, with <count> which ranges from 500h to 0FFFFh, and starts the timer.

Upon timeout, an interrupt is generated and the timer is restarted. A single digit corresponding to <timer> is printed each time the timer times out. The timer is stopped by entering T <timer>. A T stops all timers.

The timers can be run while other tests are running, since the timers are interrupt driven.

U Enter User-Defined Macro

Syntax:

u<address> <CR>

This command accepts the keyboard entry of a block of monitor commands starting at <address> into memory for later execution. Macro entry is terminated with <esc>.

When in this mode, the monitor prompt changes to . (period) to indicate that commands are not being executed, but are being entered into the userspecified buffer. The macro can be recalled and executed with the X command.

RESTRICTIONS: <address> must not be within the 0 to 7FFh range. Each macro can be any length up to the maximum number of bytes in memory. All input is redirected into the memory until ESCAPE is typed to return to the command execution mode. The only restriction to the number of macros that can be stored is the size of the memory.

W Memory Write Exerciser

Syntax:

w<address> <length> <data> <CR>

This command performs a memory write that writes <data> to each memory location specified. No data is read back and only bytes are written.

W will perform this test continuously as a scope loop. A <control+C> will stop the test.

X Execute User-Defined Macro

Syntax:

x<address> <CR>

This command executes the macro at <address>, which was previously stored with the U command.

APPENDIX A
JUMPERING

INTRODUCTION. A-3
MEMORY PCB JUMPERING. A-3
COMMUNICATIONS (SIO) PCB JUMPERING. A-12

INTRODUCTION

This appendix describes the proper jumpering for the memory and communications (SIO) printed circuit boards (PCBs). The following information is discussed:

- when to change the memory and communications jumpers
- how to set the memory PCB jumpers
- how to set the communications PCB jumpers
- how to select the recommended slot for a memory or communications PCB

NOTE

Installing the memory or communications PCBs with incorrect jumper settings will not damage the equipment, but the system will not operate properly.

After you jumper the PCB and determine the suggested slot location as described in this appendix, refer to **Removal and Replacement** in Chapter 4 for the proper installation procedures for the PCB.

The jumpers were placed in the correct positions and the PCBs were installed in the recommended slots when the 1Ø86/2Ø86 was shipped from the factory. Check and possibly move jumpers when you replace the memory or communications PCBs, or when you install additional memory or communications PCBs.

MEMORY PCB JUMPERING

When you replace or add a memory PCB, check and possibly change the jumpers. The jumpers select which memory addresses each PCB will decode.

The memory address spaces must be contiguous (the addresses on the second PCB must start where the addresses on the first PCB end, etc.). Refer to the available system address space in Figure A-3 for an example.

In addition to checking the jumpers, check that the memory PCB with the largest memory capacity (for example, 4M bytes) is installed in slot location **B**, the next largest memory capacity (for example, 2M bytes) in slot **C**, down to the memory PCB with the smallest capacity. Using the recommended slots substantially reduces troubleshooting time during diagnostic testing.

The memory PCB has two jumper connectors at PCB locations **E1** and **E2** near the top center of the PCB. Each jumper connector has 10 pins as shown in Figure A-1. You can jumper each connector in five different positions.

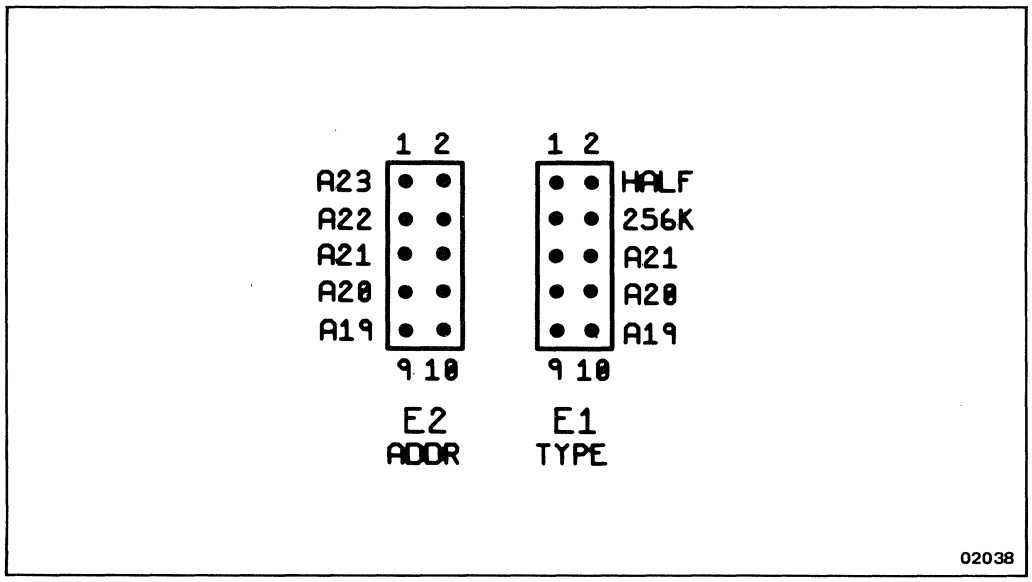

Figure A-1. Memory PCB Jumper-Pin Connectors

The memory jumper at location **E1** describes the size of the memory PCB (1M, 2M, or 4M bytes). The memory jumper at **E2** describes the address spaces which the memory PCB occupies within the system.

Figures A-2 through A-12 illustrate eleven of the many possible memory PCB combinations. Figures A-13 through A-15 summarize the remaining memory configurations.

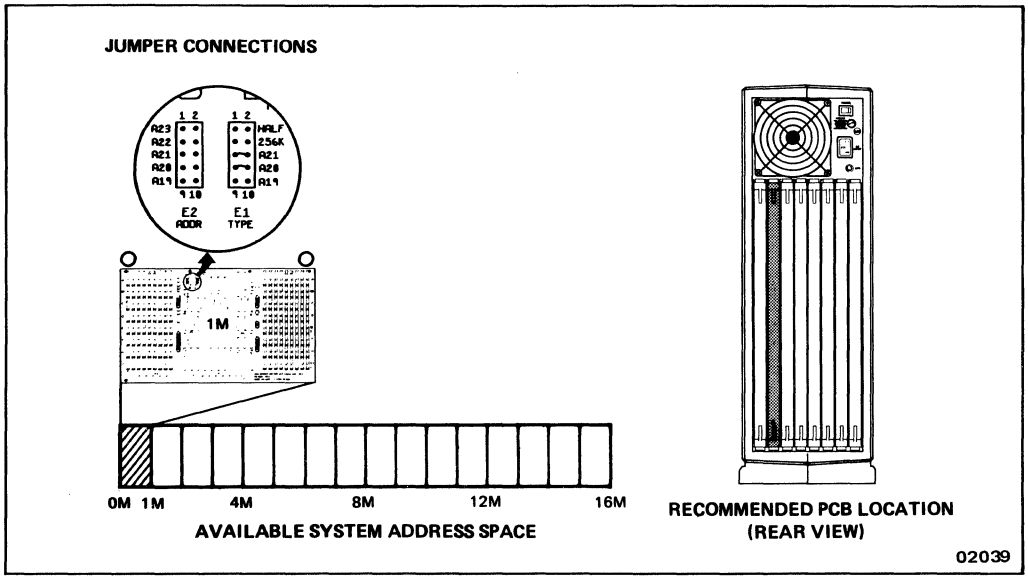

Figure A-2. Jumpers For One 1M Byte Memory PCB

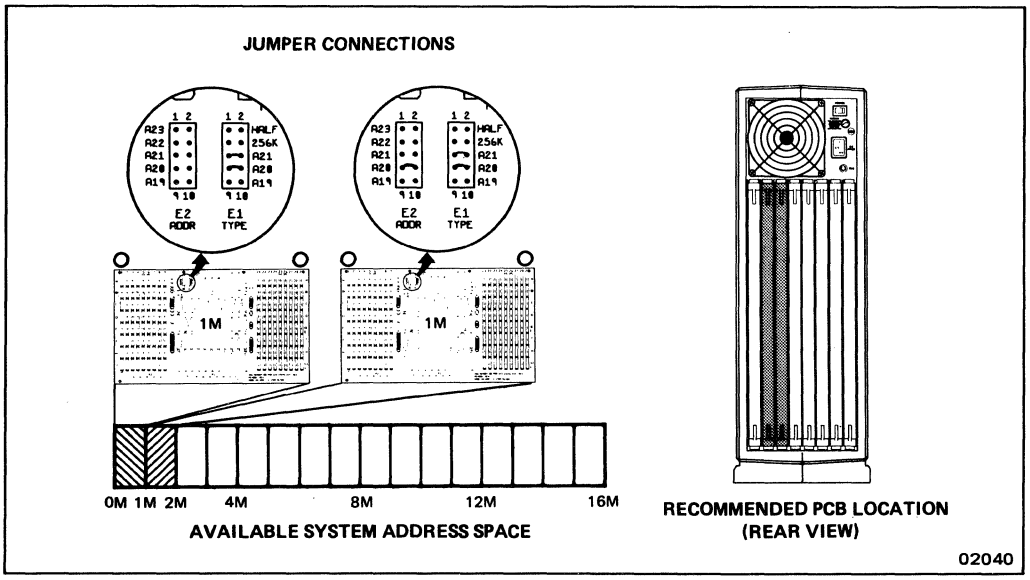

Figure A-3. Jumpers For Two 1M Byte Memory PCBs

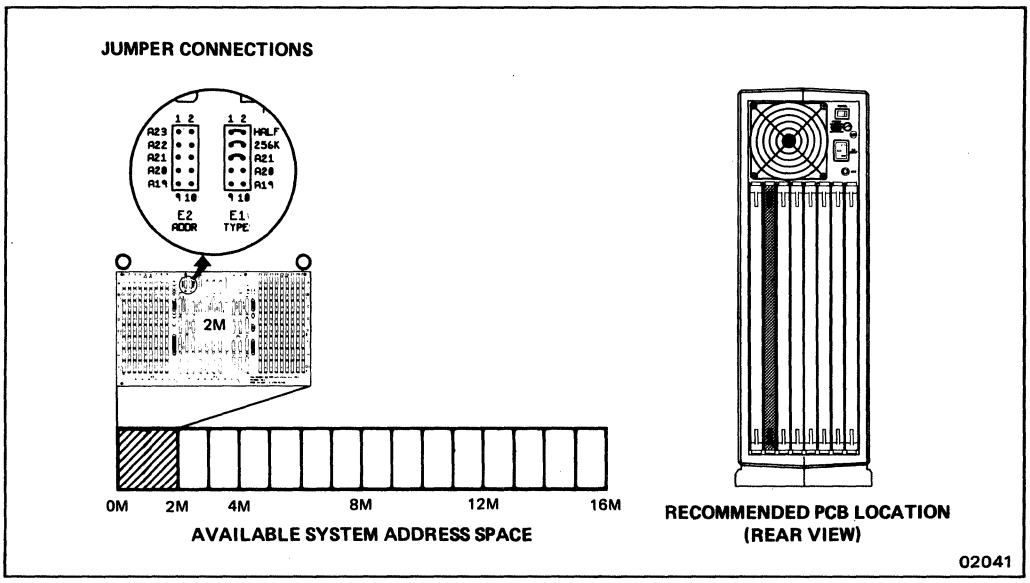

Figure A-4. Jumpers For One 2M Byte Memory PCB

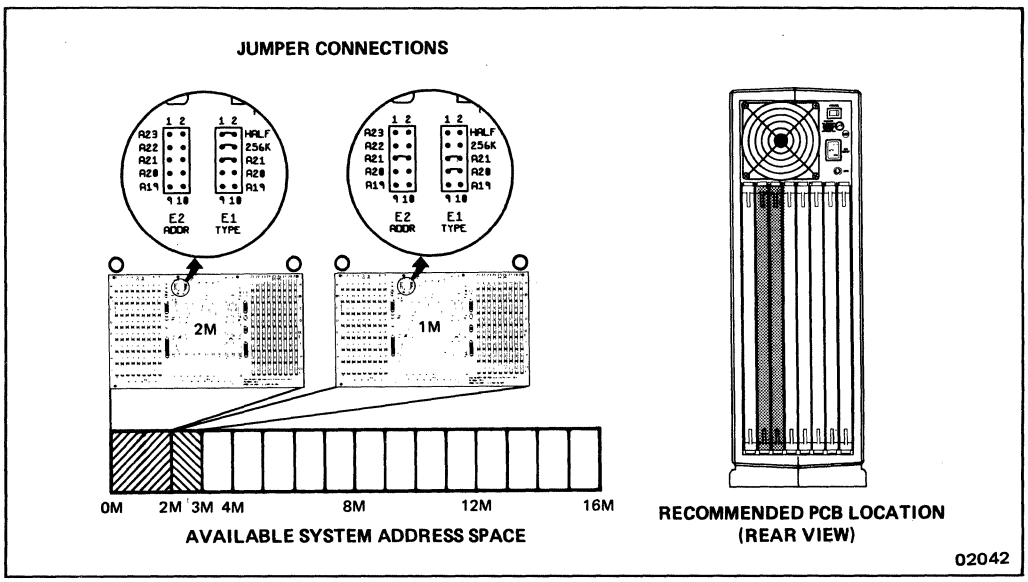

Figure A-5. Jumpers For 2M and 1M Byte Memory PCBs

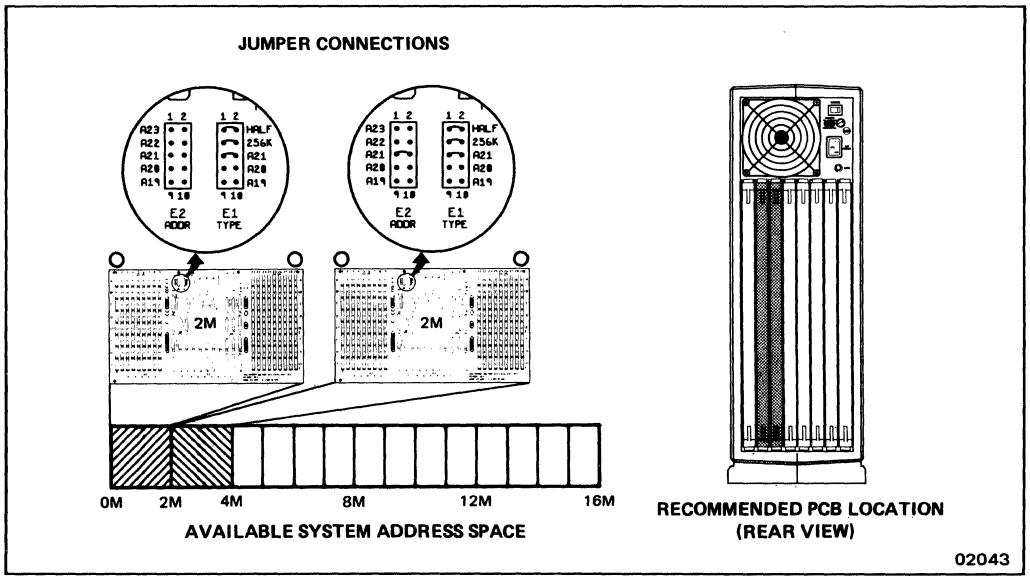

Figure A-6. Jumpers For Two 2M Byte Memory PCBs

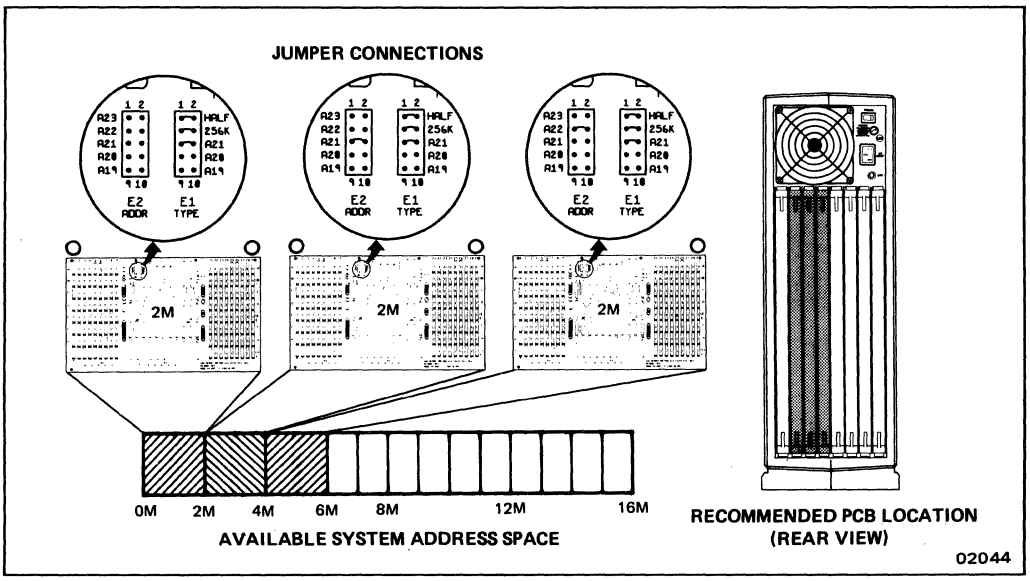

Figure A-7. Jumpers For Three 2M Byte Memory PCBs

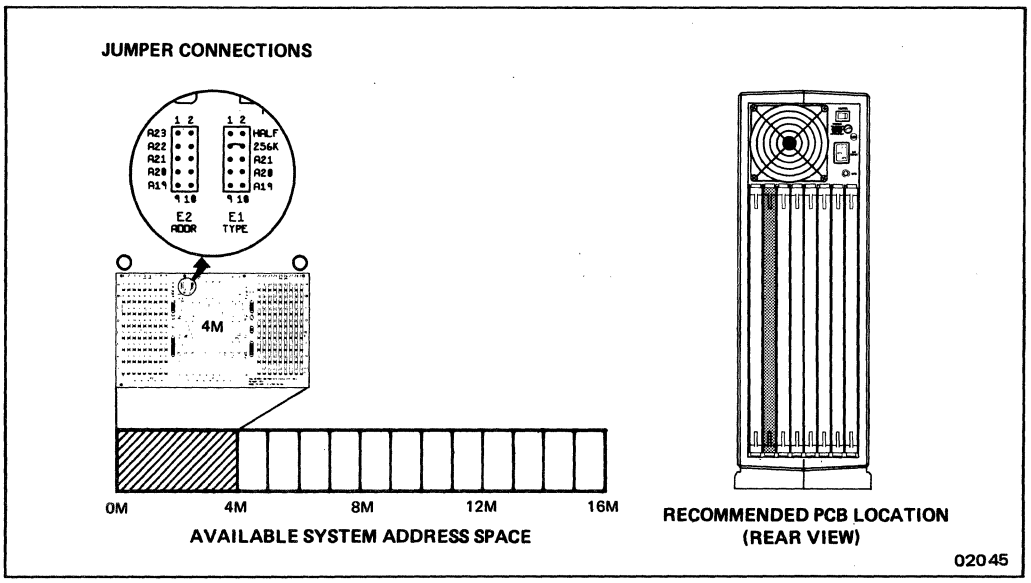

Figure A-8. Jumpers For One 4M Byte Memory PCB

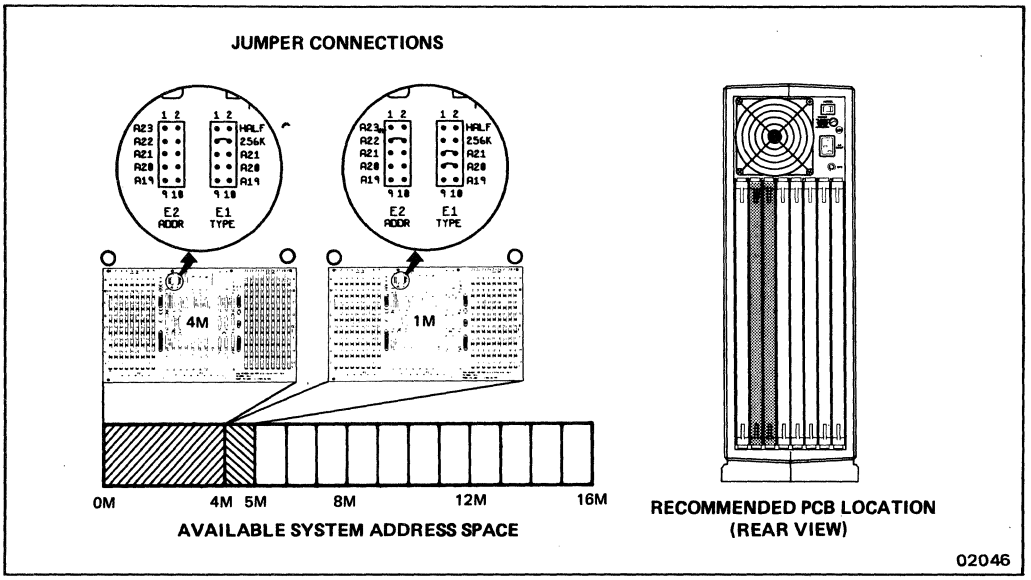

Figure A-9. Jumpers For 4M and 1M Byte Memory PCBs

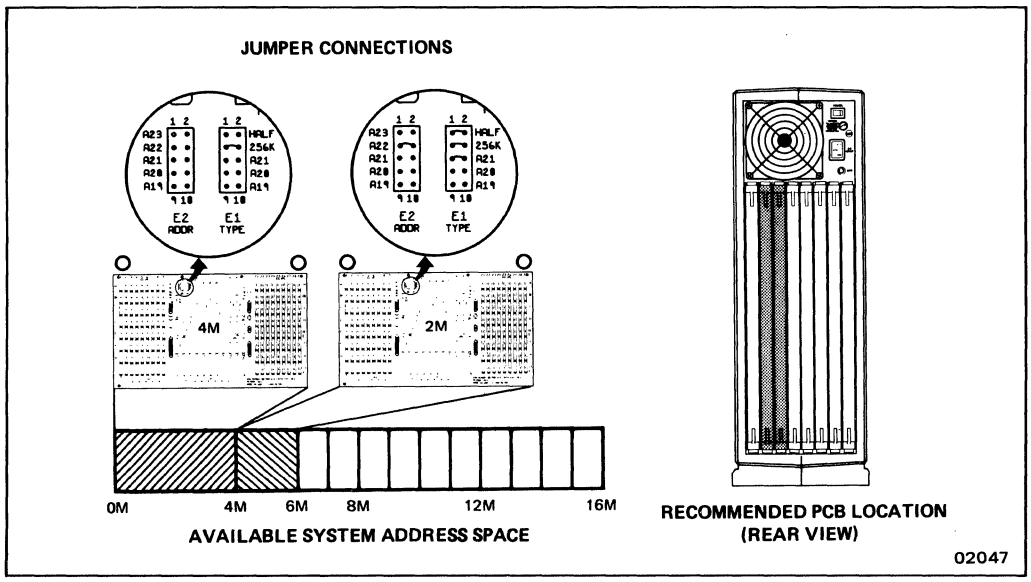

Figure A-1Ø. Jumpers For 4M and 2M Byte Memory PCBs

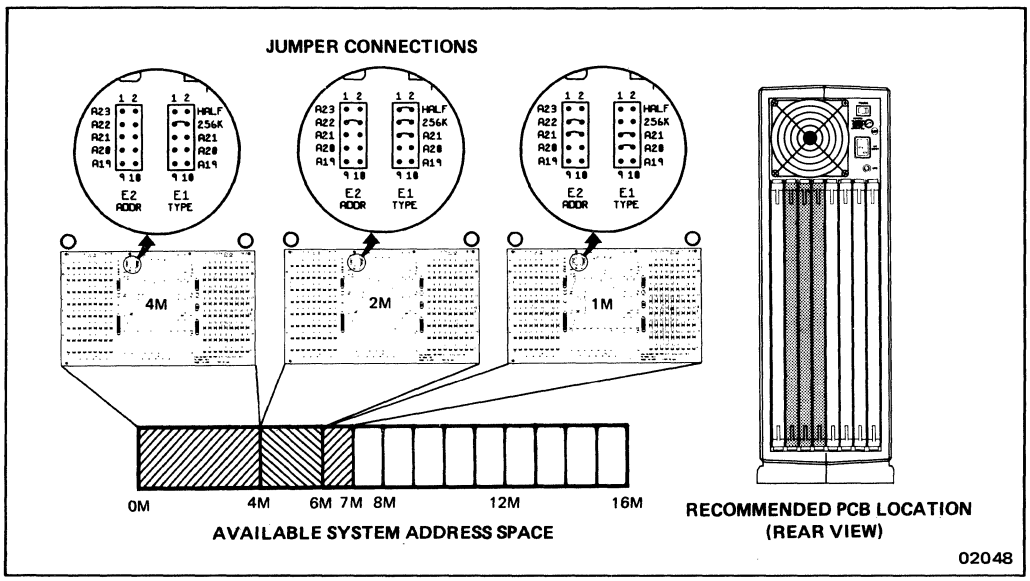

Figure A-11. Jumpers For 4M, 2M, and 1M Byte Memory PCBs

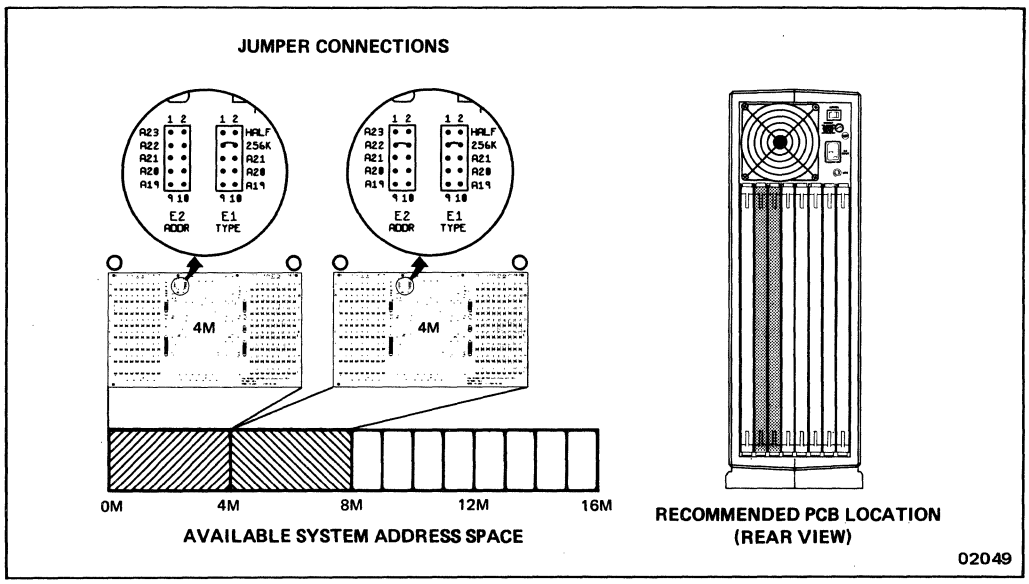

Figure A-12. Jumpers For Two 4M Byte Memory PCBs

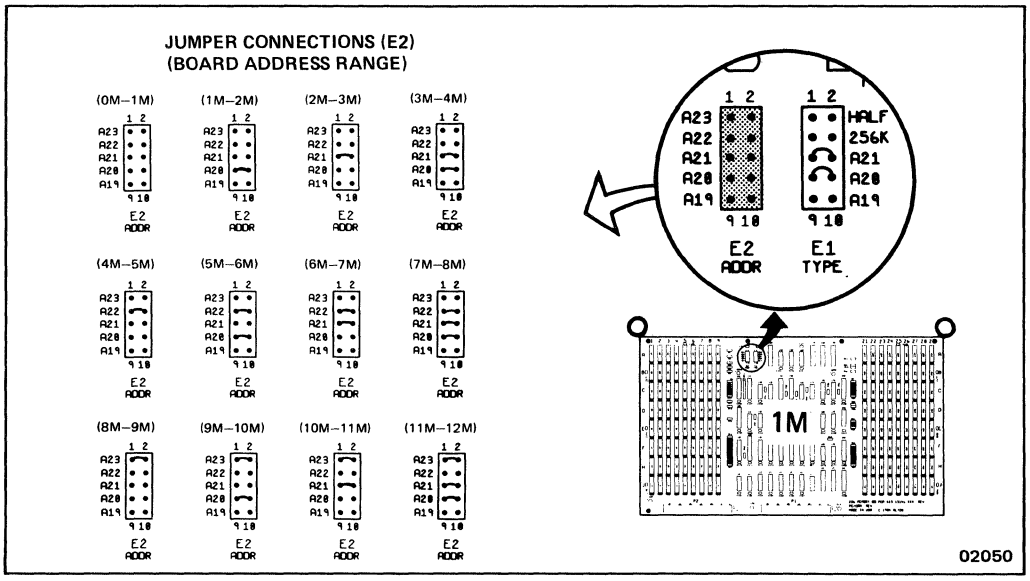

Figure A-13. Reference Jumpers For 1M Byte Memory PCBs

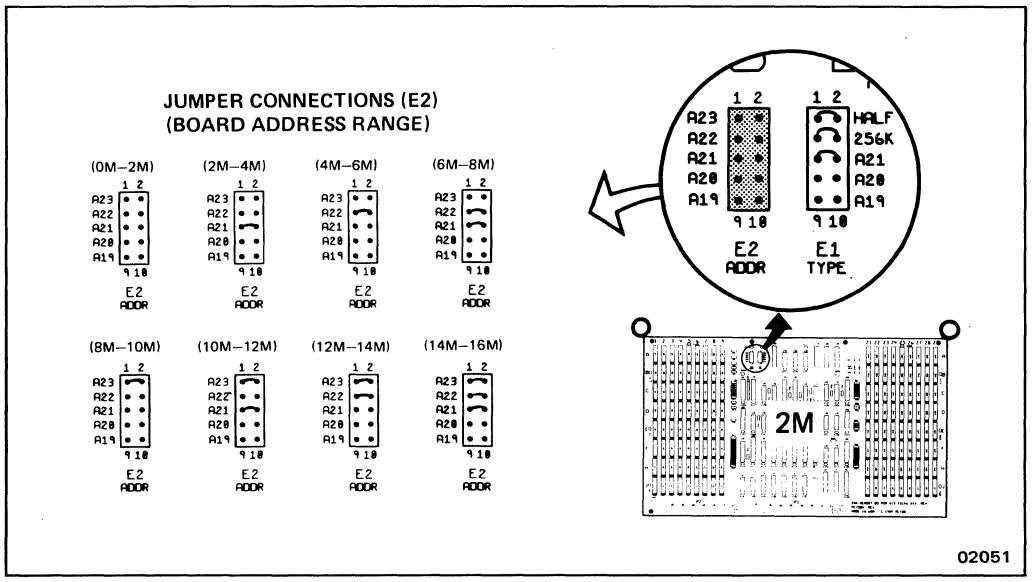

Figure A-14. Reference Jumpers For 2M Byte Memory PCBs

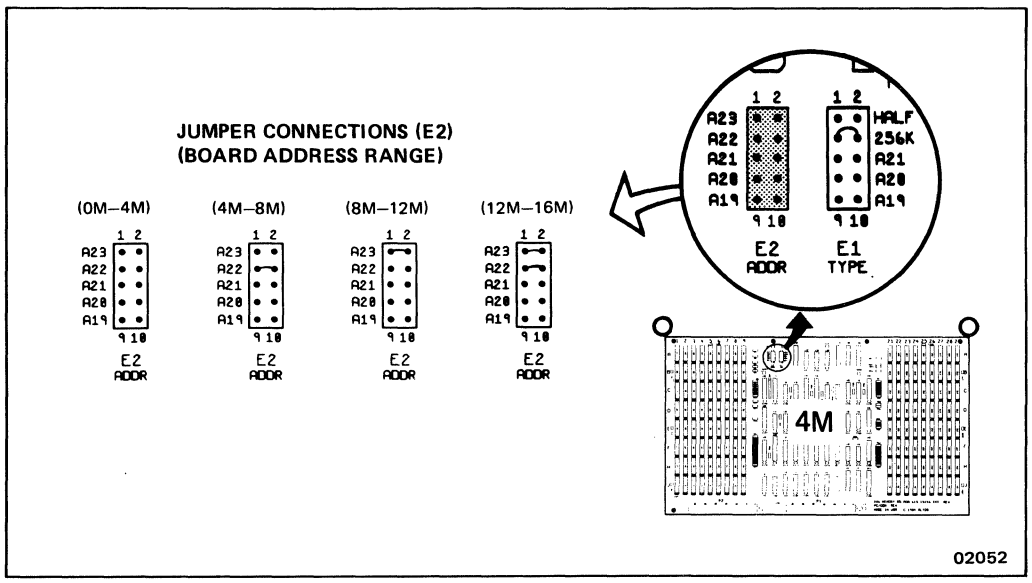

Figure A-15. Reference Jumpers For 4M Byte Memory PCBs

COMMUNICATIONS (SIO) PCB JUMPERING

The communications (SIO) PCB has eight jumper connectors that are used to select the options described in Table A-1. Figures A-16 through A-20 illustrate the proper jumper connections and recommended slot locations for primary and secondary SIO communications PCBs.

Table A-1. SIO PCB Jumper Descriptions

Connector Designation	Description
E1	General-purpose input port. Jumpered only on the primary (COMM 0) SIO communications PCB. Not jumpered on any other communications PCBs installed in the 1086/2086 system
E2	Selects the size of PROMs installed (2732, 2764, or 27128). 2764 PROMs are normally installed
E3	AACK (Advanced Acknowledge). Enables the advanced acknowledge signal from system memory (reduces wait states). Also used for local reset (testing only). Normally jumpered for enabling AACK
E4	BPRN (Bus Priority Input). Used to determine the arbitration priority when the communications PCB(s) wish to access the system bus
E5	BPRO (Bus Priority Output). See BPRN
E6	CHANATTN (Channel Attention). Selects the port number that the communications PCB responds to for channel attention signals generated on the system bus

Table A-1. SIO PCB Jumper Descriptions (Cont.)

Connector Designation	Description
E7	INT. Selects the bus interrupt vector level that the communications PCB generates
E8	LARGE*. Must be jumpered if 256K dynamic RAMs are installed

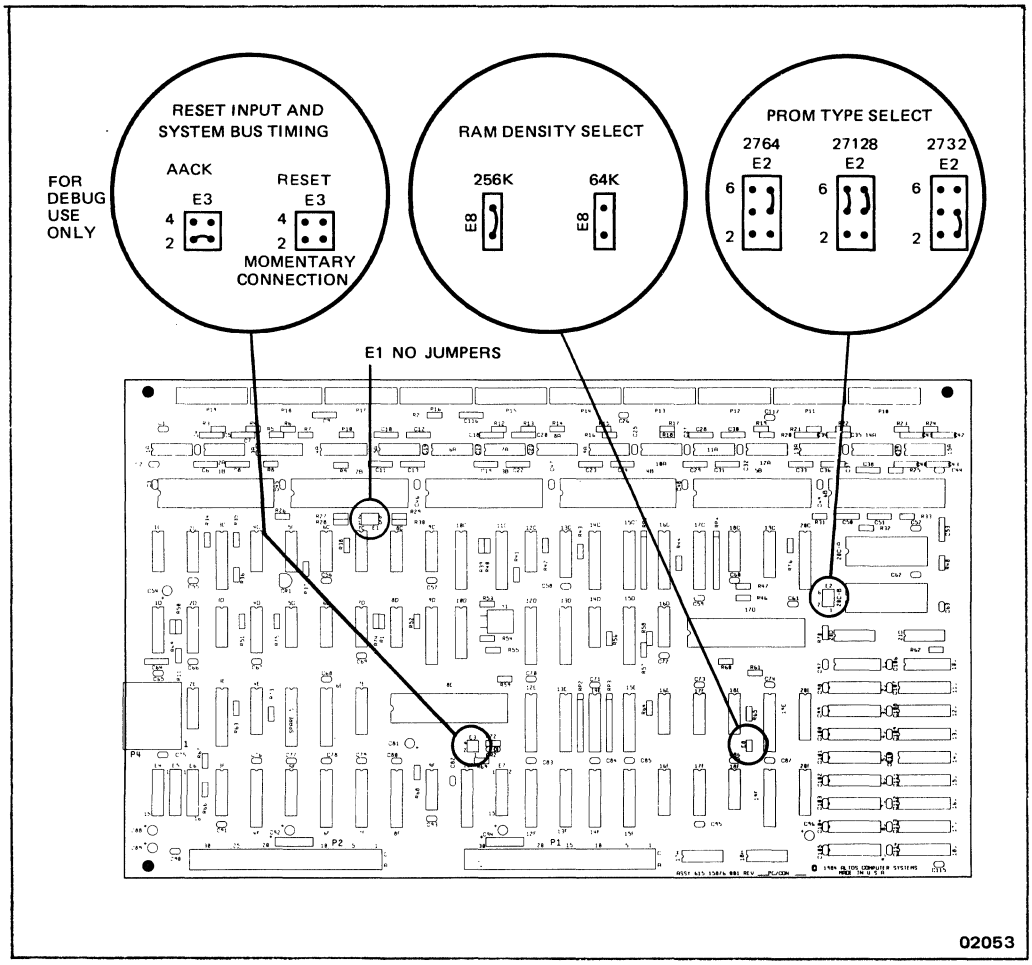

Figure A-16. Jumpers For SIO Communications PCBs (Factory Setting)

Figures A-16 through A-20 illustrate the jumper locations and settings for one primary SIO communications PCB (COMM 0) and three secondary SIO communications PCBs (COMM 1, 2, and 3). Jumper **E1** is installed only on the primary SIO PCB.

If there is more than one communications PCB, set jumpers **E4** through **E7** to indicate COMM 0 (primary), COMM 1, COMM 2, or COMM 3. The settings are shown in Figures A-16 through A-20.

Refer to the **Recommended PCB Location** illustrations in Figures A-16 through A-20 and the **Plug-In Printed Circuit Board Locations** discussion in Chapter 1 to determine the proper SIO communications PCB locations. Installing the PCBs in the recommended slots makes it easier to troubleshoot and upgrade the system.

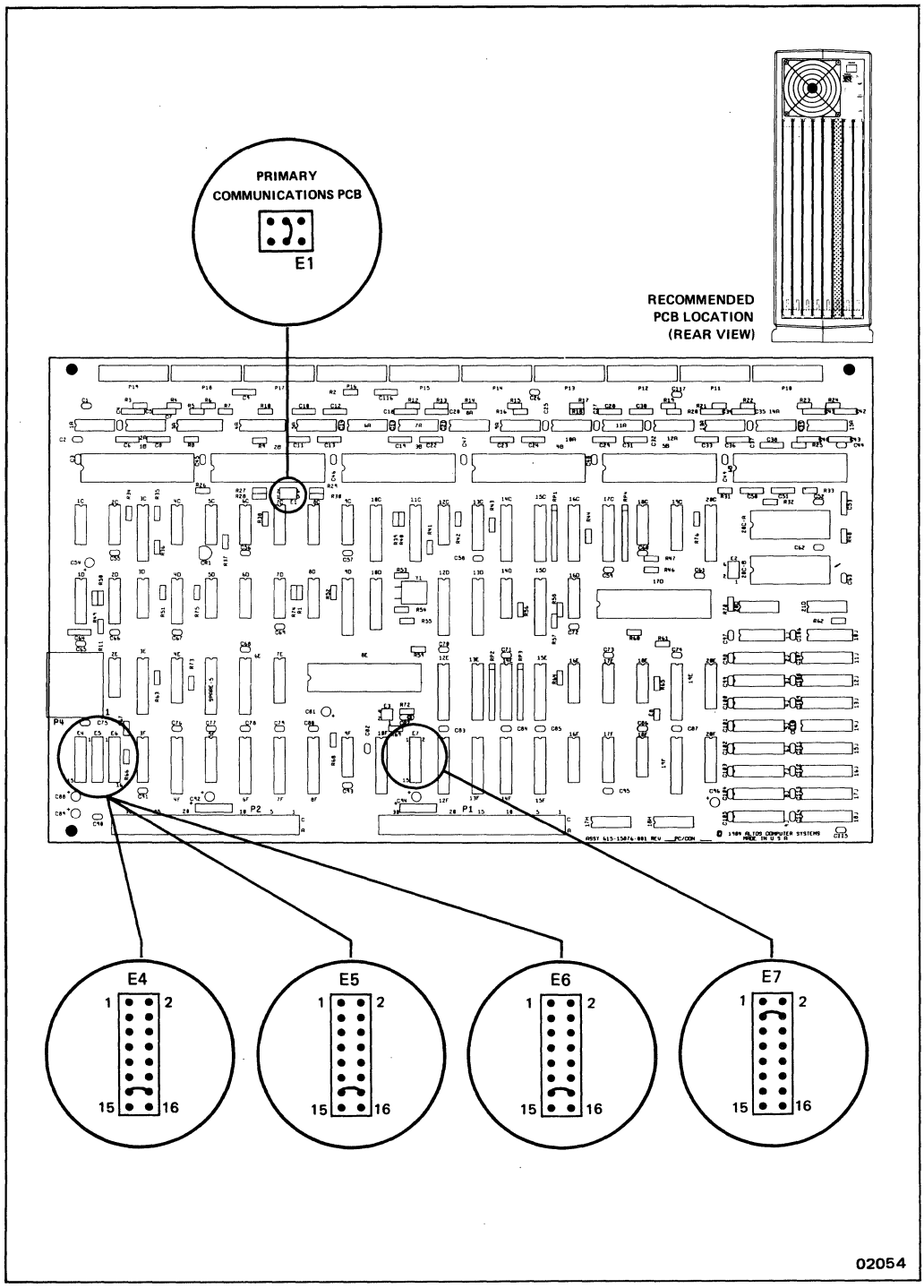

Figure A-17. Jumpers For SIO As Primary Communications PCB (COMM Ø)

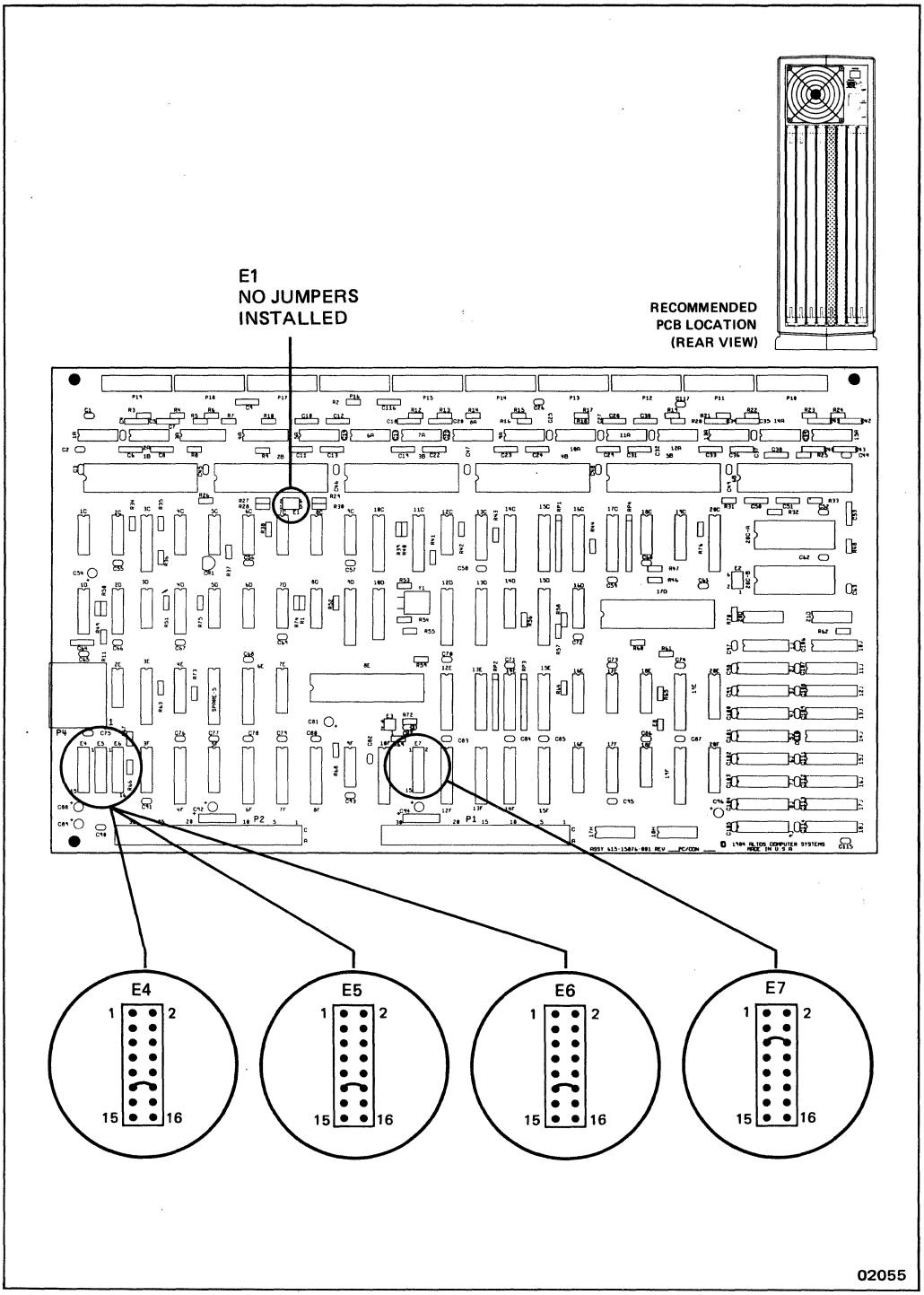

Figure A-18. Jumpers For SIO As Second Communications PCB (COMM 1)

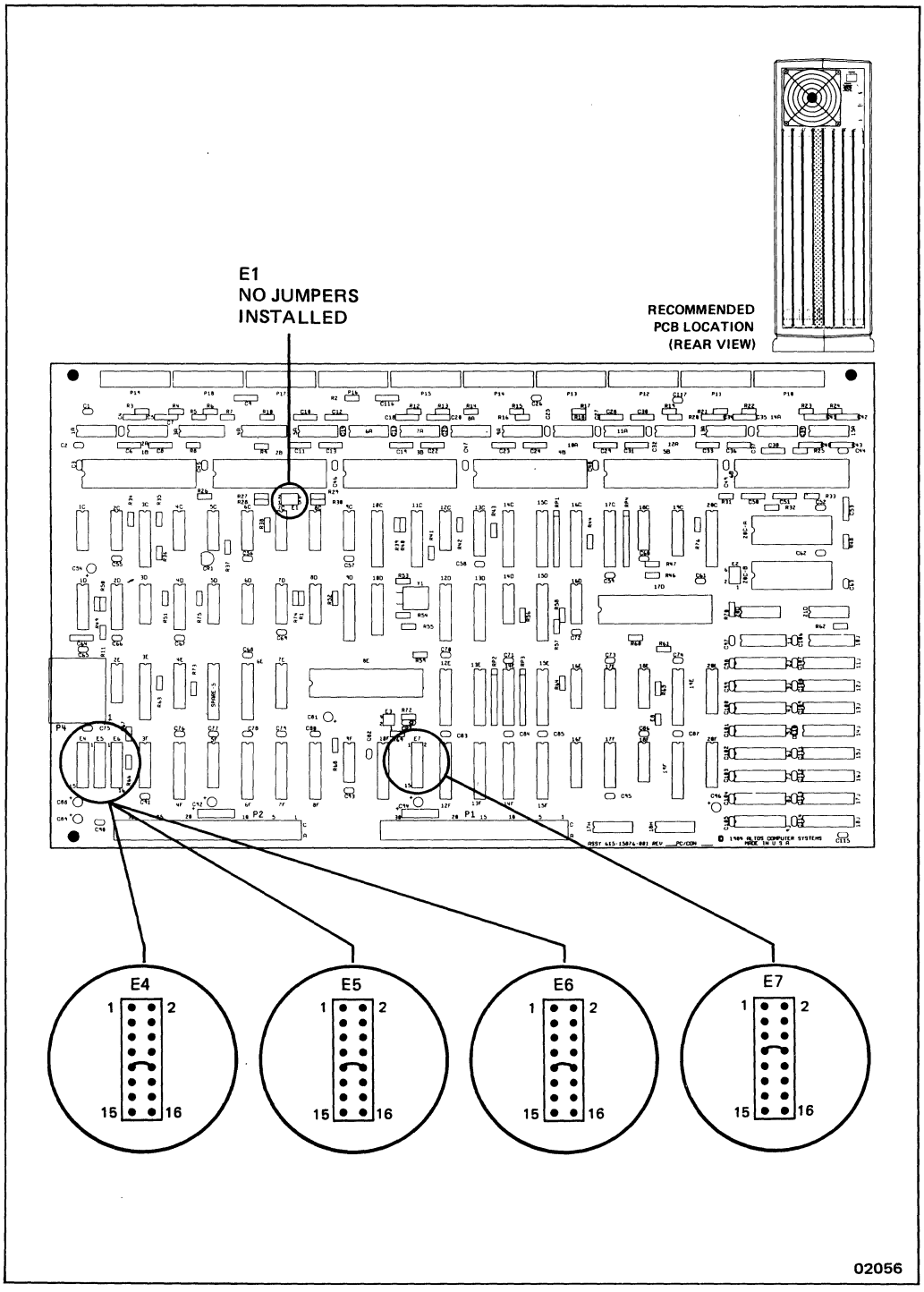

Figure A-19. Jumpers For SIO As Third Communications PCB (COMM 2)

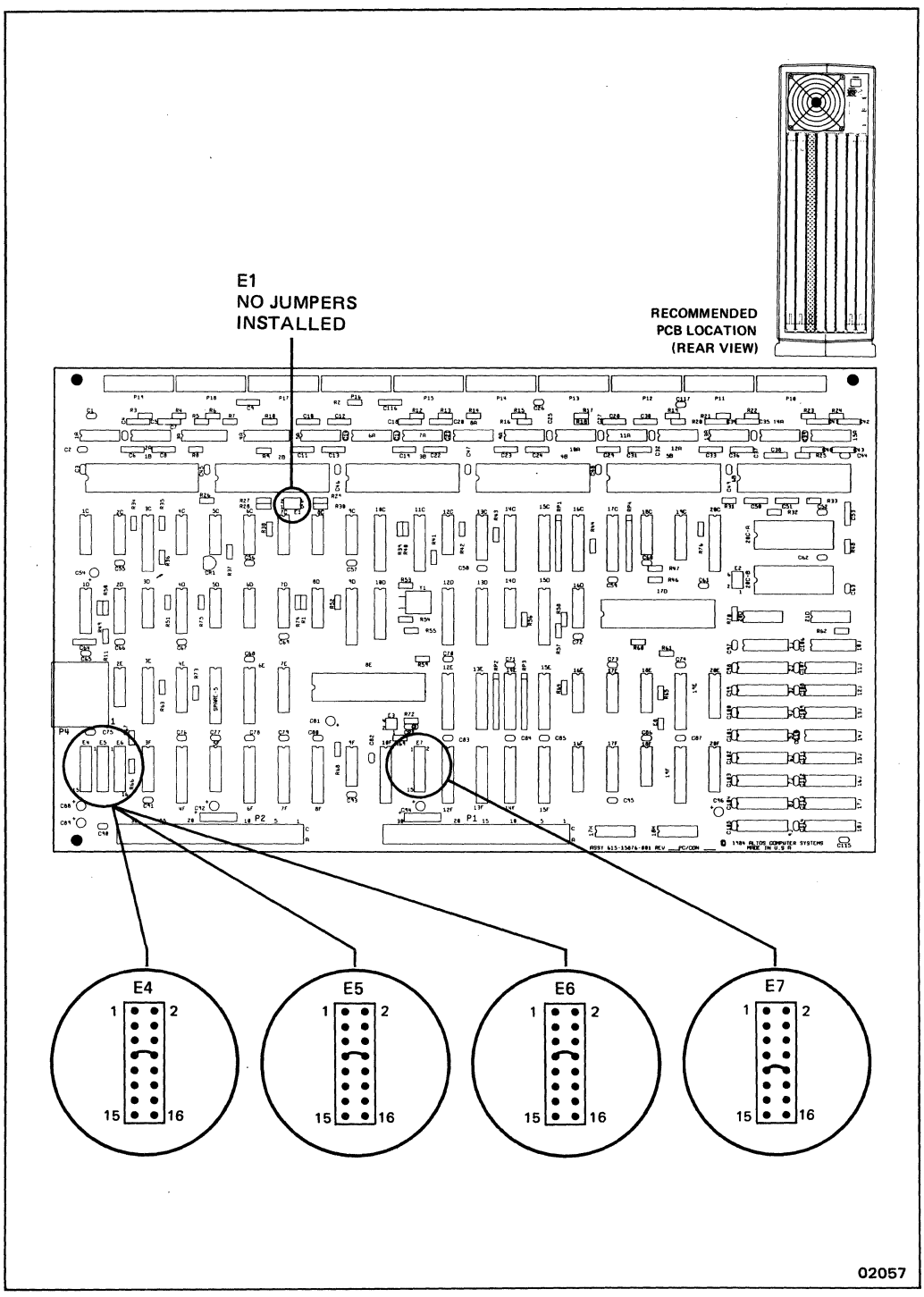

Figure A-20. Jumpers For SIO As Fourth Communications PCB (COMM 3)

APPENDIX B
STORAGE DEVICES

INTRODUCTION. B-3
CARTRIDGE TAPE DRIVE. B-3
   Electrical Specifications. B-3
FLOPPY DISK DRIVE B-4
   Electrical Specifications. B-4
HARD DISK DRIVE B-5
   Electrical Specifications. B-6

INTRODUCTION

This appendix includes detailed specifications for the Altos 1Ø86/2Ø86 Computer System cartridge tape, floppy disk, and hard disk drives that have been qualified and approved by Altos (at the time this manual was printed) for use in this system.

CAUTION

The drives specified in this appendix are those that have been tested and approved by Altos for use in this system. Altos is not responsible for the proper performance or subsequent service of any 1Ø86/2Ø86 that does not have Altos-approved drives installed. Contact your Altos dealer or distributor for other drives that may have been approved since this manual was printed.

CARTRIDGE TAPE DRIVE

The cartridge tape drives approved by Altos for use in the 1Ø86/2Ø86 are the Archive Scorpion and the WangTek Model 5ØØØE or an equivalent. These drives use a 1/4 inch streaming cartridge tape packaged in a 5-1/4 inch footprint. The primary function of the cartridge tape drive is to provide backup for the hard disk drive.

The tape drive is connected to the controller PCB via a single 5Ø-conductor ribbon cable to the backplane. The drive may be moved a maximum of 3 meters (9 feet 1Ø inches) away from the controller.

Electrical Specifications

The cartridge tape drive specifications listed in Table B-1 apply for both the Archive and WangTek drives.

Table B-1. Cartridge Tape Drive Specifications

Characteristic	Performance Requirement
Tracks	9
Channels*	2
Capacity (DC 600A)	60M bytes
Backup Time (DC 600A)	12 minutes
Recording Mode	NRZI (nonreturn-to-zero invert)
Recording Data Density	8000 bpi (bits per inch)
Encoding Method	4-to-5 RLL (run-length limited)
Flux Density	10,000 ftpi (flux transitions per inch)
Track Capacity DC 600A	6.6M bytes
Data Transfer Rate	90K bytes/second
Tape Speed	90 inches/second
Start/Stop Time	300 milliseconds

* Channels are defined as one write head gap followed by one read head gap.

As shown in Table B-1, when an industry-standard 1/4 inch magnetic tape cartridge is loaded into the tape drive 60M bytes of data can be stored or backed up in one 1/4 inch tape cartridge.

FLOPPY DISK DRIVE

The floppy disk drive approved by Altos for use in the 1086/2086 is a Panasonic Model 475-2 or an equivalent.

The Panasonic drive is a half-height, 5-1/4 inch, double-sided drive that is selectable from low speed to high speed by a control signal from the interface.

Electrical Specifications

The specifications listed in Table B-2 apply to the Panasonic Model 475-2.

Table B-2. Floppy Disk Drive Specifications

Characteristic	Performance Requirement
Storage Capacity (Unformatted)	
Per Disk	
Low Density	1M byte
High Density	1.6M bytes
Storage Capacity (Unformatted)	
Per Track	
Low Density	6,250 bytes
High Density	10K bytes
Storage Capacity (Formatted)	
Per Disk	
Low Density	720K bytes
High Density	1.2M bytes
Heads	2
Tracks	80
Seek Settle Time	At least 18 milliseconds
Head Switching Time	At least 3.1 milliseconds
Write Gate Delay	0 millisecond after seek

HARD DISK DRIVE

The hard disk drives approved by Altos for use in the 1086/2086 are the following:

50M Byte	80M Byte	190M Byte
Hitachi	**Micropolis**	**Maxtor**
Model DK 511-5	Model 1325	Model XT 2190
Micropolis		
Model 1323A		
Vertex		
Model V150		

The operating system is programmed with drive information (number of heads, cylinders, etc.) when the drive is installed. This configuration stays with the system as long as the drive is not changed. Number of sectors per track and sector size is determined by the operating system.

Electrical Specifications

The hard disk drive specifications listed in Table B-3 apply for the 50M byte Hitachi Model DK 511-5, Micropolis Model 1323A, and Vertex Model V150.

Table B-3. 50M Byte Hard Disk Drive Specifications

Characteristic	Performance Requirement
Hitachi Model DK 511-5	
Storage Capacity	
Unformatted	51M bytes (50M bytes)
Formatted	40.08M bytes
Sectors/Track	16
Cylinders	699
Tracks	4893
Heads	7
Track Skew	2
Sector Interleave	0
Bytes/Sector	512
Precomp Track	None
Data Transfer Rate	50M bits/second
Recording Density	Not applicable
Recording Method	MFM (modified frequency modulation)
Transfer Method	MFM (modified frequency modulation)
Seek Time (Includes Settling Time)	
Single Track	6 milliseconds, maximum
Average	28 milliseconds, maximum
Full Stroke	62 milliseconds, maximum
Interface	ST-506/412
Technology	Winchester

Table B-3. 50M Byte Hard Disk Drive Specifications (Cont.)

Characteristic	Performance Requirement
Micropolis Model 1323A	
Storage Capacity	
Unformatted	53.3M bytes (50M bytes)
Formatted	41.94M bytes
Sectors/Track	16
Cylinders	1024
Tracks	5120
Heads	5
Track Skew	2
Sector Interleave	0
Bytes/Sector	512
Precomp Track	None
Data Transfer Rate	5M bits/second
Recording Density	Not applicable
Recording Method	MFM (modified frequency modulation)
Transfer Method	MFM (modified frequency modulation)
Seek Time (Includes Settling Time)	
Single Track	6 milliseconds, maximum
Average	23 milliseconds, maximum
Full Stroke	45 milliseconds, maximum
Interface	ST-506/412
Technology	Winchester

Table B-3. 50M Byte Hard Disk Drive Specifications (Cont.)

Characteristic	Performance Requirement
Vertex Model V150	
Storage Capacity	
Unformatted	51.4M bytes (50M bytes)
Formatted	40.42M bytes
Sectors/Track	16
Cylinders	987
Tracks	4935
Heads	5
Track Skew	2
Sector Interleave	0
Bytes/Sector	512
Precomp Track	None
Data Transfer Rate	5M bits/second
Recording Density	Not applicable
Recording Method	MFM (modified frequency modulation)
Transfer Method	MFM (modified frequency modulation)
Seek Time (Includes Settling Time)	
Single Track	6 milliseconds, maximum
Average	23 milliseconds, maximum
Full Stroke	45 milliseconds, maximum
Interface	ST-506/412
Technology	Winchester

The hard disk drive specifications listed in Table B-4 apply for the 80M byte Micropolis Model 1325

Table B-4. 80M Byte Hard Disk Drive Specifications

Characteristic	Performance Requirement
Micropolis Model 1325	
Storage Capacity	
Unformatted	85.3M bytes (80M bytes)
Formatted	67.1M bytes
Sectors/Track	16
Cylinders	1024
Tracks	8192
Heads	8
Track Skew	2
Sector Interleave	0
Bytes/Sector	512
Precomp Track	None
Data Transfer Rate	5M bits/second
Recording Density	Not applicable
Recording Method	MFM (modified frequency modulation)
Transfer Method	MFM (modified frequency modulation)
Seek Time (Includes Settling Time)	
Single Track	6 milliseconds, maximum
Average	28 milliseconds, maximum
Full Stroke	62 milliseconds, maximum
Interface	ST-506/412
Technology	Winchester

The hard disk drive specifications listed in Table B-5 apply for the 190M byte Maxtor Model XT 2190.

Table B-5. 190M Byte Hard Disk Drive Specifications

Characteristic	Performance Requirement
Maxtor Model XT 2190	
Storage Capacity	
Unformatted	191.24M bytes (190M bytes)
Formatted	150.41M bytes
Sectors/Track	16
Cylinders	1224
Tracks	18,360
Heads	15
Track Skew	2
Sector Interleave	0
Bytes/Sector	512
Precomp Track	None
Data Transfer Rate	5M bits/second
Recording Density	Not applicable
Recording Method	MFM (modified frequency modulation)
Transfer Method	MFM (modified frequency modulation)
Seek Time (Includes Settling Time)	
Single Track	5 milliseconds, maximum
Average	30 milliseconds, maximum
Full Stroke	54 milliseconds, maximum
Interface	ST-506/412
Technology	Winchester

APPENDIX C
UTILITY PROGRAMS

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INTRODUCTION

This appendix includes procedures for using the utility programs available on the System Diagnostics Executive (SDX) disk included with the 1086/2086. The utility programs enable you to:

- prepare a floppy disk for use
- copy a floppy disk
- display the bad sectors on the hard disk
- flag additional bad sectors on the hard disk
- remove bad sector flags on the hard disk
- format the hard disk
- reconfigure the hard disk drive

Before you can use the SDX utility programs, boot from the SDX disk as described in the following procedure. The SDX utilities are available only from the system console terminal.

BOOTING THE SDX DISK

Perform the following procedure to boot the SDX disk:

1. Turn on the system power. If the system power is on, turn the reset key to **RESET** and back to **RUN.**

2. Press the <space bar> when you see the prompt:

```
Press any key to interrupt autoboot
```

The following menu appears:

```
Enter [1] to Boot from Hard Disk
Enter [2] to Boot from Floppy Disk
Enter [3] to enter the main CPU Monitor
Enter [4] to enter the main SIO Monitor
Enter option:
```

3. Insert the SDX disk into the floppy disk drive.

4. Type **2** to select the floppy disk boot. A message similar to the following appears:

```
Booting from floppy  . . . loading xxxx SDX
```

5. Wait for the SDX Main Menu to appear:

```
ACS xxxx SYSTEM DIAGNOSTIC EXECUTIVE (SDX)
                                Version x.xx

Main Menu:

        R:  Run system confidence tests

        U:  Utility programs

        S:  Display test summary

        X:  Exit SDX

*** Enter command and press <CR>:
```

If the Main Menu does not appear, repeat steps 3 and 4.

6. When the Main Menu appears, press the **CONTROL** key and type **F**.

7. The displayed prompt asks you for a password. Type **sotla** and press <**CR**>. The following SDX Field Service Menu will appear:

```
SDX Field Service Menu:

        b (brief)     Brief description of all tests
        c (clear)     Clear pass count, error count, and history
        d (disable)   Disable test
        e (enable)    Enable test
        h (halt)      Halt on error
        l (loop)      Loop on command line
        m (menu)      Menu level selection
        p (parameter) Change parameters
        r (report)    Display error history
        s (summary)   Display error summary
        t (test)      Execute test (s)
        u (utility)   Call utility programs
        ? (help)      Display this menu
        x (exit)      Exit to main menu
        z (debugger)  Enter debugger

        ***Enter Command and Press <CR>
```

8. Type **u** to select the utility programs. The following Utilities Menu appears:

```
Utilities Menu:

1           Floppy Format
2           Floppy Copy
3           Display Hard Disk Configuration Table
4           Flag Hard Disk Bad Sectors
5           Scan Hard Disk Bad Sectors
6           Hard Disk Format
7           Reconfigure Hard Drive
8           Return to Previous Menu

Enter Selection:
```

9. Select the utility you want by typing in the program number. Then find the procedure for your selection in the remainder of this appendix.

NOTE

If you need to stop a program before it completes, press the <**ESC**> key. Pressing <**ESC**> cancels the operation and returns you to the Main Menu.

FLOPPY FORMAT

The floppy drive operates at two speeds: high speed and low speed. When you use the SDX Floppy Format and Floppy Copy utilities, the display asks whether you want to format at high or low speed, and adjusts the speed accordingly.

Use high speed to read and write to floppy disks created at high speed. Use low speed to read and write to disks created at low speed (e.g., on earlier Altos systems, and on IBM PC and XT computers). Refer to your software documentation for information on accessing floppy disks created on other floppy drives.

NOTE

Make sure you use certified, high-density, double-sided, soft-sectored, 96 tpi (tracks per inch) disks if you plan to format a disk at high speed.

Always format a floppy before trying to use it under the operating system. If you try to use the operating system to access information on an unformatted disk, you will receive an error message similar to:

dev_stat [Ø/1/2/3] xxh xh xh xxxxh general error

CAUTION

Formatting a floppy disk erases all data on the diskette. Do not format a disk that contains any valuable data.

1. Select **1** from the Utilities Menu. The screen displays:

```
Floppy Format                    Please wait...

Enter the floppy speed:

 (A) Low Speed        (B) High Speed

Enter:
```

If you have the optional dual-speed floppy, you can format the disk at high or low speed.

2. Enter the floppy speed. The following prompt asks if you want each track to be verified:

```
Do you want track verification?  (y/n)
```

3. Enter **y** (yes) to verify each track as it is formatted to assure that the formatting process is successful.

   Track verification increases the execution time of the formatting process to approximately three minutes for each disk. Without track verificaation, the process takes approximately one

minute. After responding to the track verification prompt, the screen displays:

```
Insert diskette to be formatted and press "Y"
```

4. Remove the disk from the drive and insert the disk to be formatted. Then press **Y**.

   As the disk is formatting, the screen displays the number of each cylinder. If you select track verification, the screen also displays the number of each cylinder as it is verified. After formatting is completed, the screen displays:

```
                Format completed.

  Do you wish to run this program again? (y or n)
```

5. Select **y** (yes) if you want to format additional floppy disks.

   To return to the Utilities Menu, enter **n** and follow the instructions.

FLOPPY COPY

You do not have to format a disk before using the Floppy Copy utility. The display asks you to select which speed you want to use. You can use high speed to copy a high-speed disk to an unformatted certified high-speed disk. You can use low speed to copy one standard disk to another standard disk.

You can also use low speed to copy information from a low-speed disk onto a high-speed disk, but the program automatically formats the destination disk at low-speed before copying the information.

If you select high speed and try to copy information from a high-speed disk onto a low-speed destination disk, you will receive an error message. If you have to transfer information from a high-speed disk to a low-speed disk, use the operating system software to copy the disk to the hard disk. Then transfer it onto the low-speed disk.

NOTE

To copy a high-speed disk, you must use a high-speed certified disk as the destination disk (the disk you copy to). Standard disks do not work correctly when used at high speed.

Return to the Utility Menu and perform the following procedure to copy a disk:

1. Type **2** to select Floppy Copy from the Utilities Menu.

2. Wait for the screen to display:

```
Floppy Copy                          Please wait...
```

3. Wait for the following display to appear:

```
Enter the floppy drive speed:

   (A) Low Speed          (B) High Speed

Enter:
```

4. If you want to copy information from a low-speed disk to another low-speed disk, answer **A** and press <**CR**>. If you want to copy information from a high-speed disk to another formatted high-speed disk, answer **B** and press <**CR**>. The screen displays:

```
Insert diskette to be copied from and press 'y'
```

5. Insert the disk to be copied from and type **y**. The screen displays:

```
*** Reading cyl:  nn
```

6. Wait for the first read cycle to complete. The screen displays:

```
Insert diskette to be copied to and press 'y'
```

7. Insert the disk to be copied to and type **y**. The screen displays:

```
*** Writing cyl:  nn
```

When the copy is complete, the screen displays:

```
Copy completed.  Do you wish to run this program
again?  (y/n)
```

8. Type **y** to continue copying disk until you have no more disks to copy. To exit from Floppy Copy, type **n**. The screen displays:

```
Floppy Copy.........................Executed

Press any key to return to the Utilities Menu.
```

9. Press any key, such as the <space bar> to return to the Utility Menu.

10. Type **8** to exit from the Utility Menu.

WORKING WITH HARD DISK BAD SECTORS

Terminology

The remaining utilities in the Utilities Menu deal with the hard disk drive bad sectors. The following information is intended to help explain some of the hard-disk terminology relating to these utilities.

The hard disk stores data in hundreds of circular tracks, which are further divided into sectors. Hundreds of thousands of individual sector areas are available on each hard disk. Figure C-1 shows the differences between hard-disk sectors, cylinders, and heads.

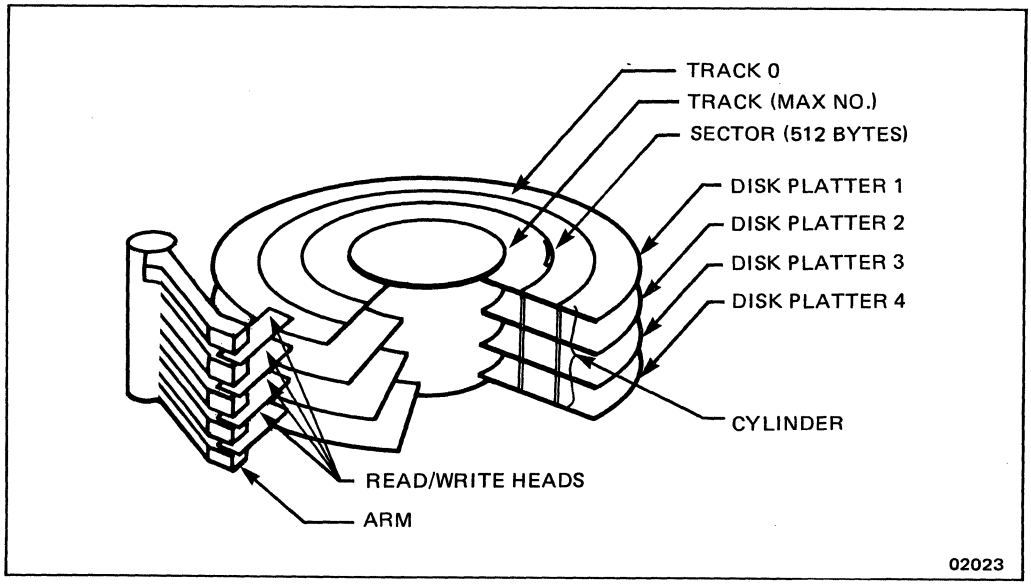


Figure C-1. Hard-Disk Terminology

Occasionally a sector develops a flaw in the magnetic media. These bad (flawed) sectors do not noticeably reduce hard disk storage, but the system needs to identify the bad sectors, so that no data is stored on them.

Each hard disk drive is carefully tested at the factory and any bad sectors are flagged before shipment. A hard copy printout of the flaw list is included for each hard disk drive. An identical list is also stored on track Ø of each hard disk. If there is more than one hard disk drive, match the lists with the correct drives.

To do this, compare the serial number on the printout with the serial number written on the round label in the front of the drive. (Remove the front panel to check the round labels -- refer to Chapter 4 for removal procedures.)

When you use the utility programs to display the current list of bad sectors, the program gets the list from track Ø. Use the Scan Hard Disk for Bad Sectors utility to scan the disk and list any bad sectors that do not correspond to the current list. Make sure you use the Flag Bad Sector utility to flag any unflagged bad sectors immediately.

At some time, you may receive a message from your operating system software that a new bad sector has been found. The message is similar to:

```
hard disk error drv x cyl xxxx hd x sec xx, or
marginal sector drv x cyl xxxx hd x sec xx
```

Make sure you write down the drive (drv), cylinder (cyl), head (hd), and sector (sec) numbers accurately. Then use the Flag Bad Sector utility to flag the new bad sector. The flag bad sector utility allows you to update the track Ø information.

Make a copy of the flaw list printout and keep it. If new bad sectors occur while you use the system, update the list with the drive, cylinder, head, and sector locations. You may need the entire list if the information on track Ø is ever destroyed.

Determining the Drive Number

Before you can use the following utilities, you need to understand how the hard disk drives are numbered in your system. The first drive is installed in the bottom drive slot, and is called drive Ø. The second drive, if you have one, is installed in the middle slot and called drive 1.

The third drive, if present, is installed in the top slot and is numbered drive 2. When the following hard-disk utility programs ask you to specify which drive(s) you want to test, enter a **Ø**, **1**, or **2**.

DISPLAY HARD DISK CONFIGURATION TABLE

The Display Hard Disk Configuration Table utility program from the Utilities Menu allows you to view technical information about the hard disk(s). This utility lists the number of cylinders, heads, sectors, sector size, track skew, sector interleave, manufacturer, size in megabytes, and precompensation information. It also gives you the option of seeing the current bad sector list which is stored on track Ø. Perform the following procedure to use this utility:

1. Type **3** and press <**CR**> to select the Display Hard Disk Configuration Table utility. The following screen appears (the information in square brackets does not appear on one-drive systems):

```
Display Hard Disk Configuration Table   Please wait..

 Ø - Drive - Ø
[1 - Drive - 1]
[2 - Drive - 2]

 Enter a drive number from the above selection
 ->
```

2. Type a **Ø**, **1**, or **2** to indicate which drive you are checking. For example, type **Ø** for a one-drive system. Information similar to the following appears:

```
Drive x configuration information:

Maximum cylinders.....................xxxx
Maximum heads.........................x
Maximum sectors.......................xx
Sector size...........................xxx
Track skew............................x
Sector interleave.....................x
Maker.................................manufacturer
Megabytes.............................xx
Precomp...............................xxxx

Would you liked to see the bad sector list on
drive x? (y/n)
```

3. Type **y** to see the list; type **n** to return to the Utilities Menu. If you type **y**, press any key when you see the message:

```
Press any key to continue
```

When the last screen displays, you will see information similar to the following:

```
Bad Sector List Size On Drive x is xx

Display Hard Disk Configuration Table.......Executed

Press any key to return to the Utilities Menu.
```

NOTE

Due to the large capacity of the hard disks, it is not unusual to have a bad sector list with one hundred or more entries.

4. Press any key to go back to the Utilities Menu.

SCAN HARD DISK FOR BAD SECTORS

The Scan Hard Disk for Bad Sectors utility allows you to:

- scan the hard disk(s) for bad sector information
- list any bad or marginal sectors not on the current bad sector list

Use the **Flag Hard Disk Bad Sector** utility to flag any new bad sectors, and to update the list on track Ø.

This utility allows you to scan the disk for bad sectors, list all bad sectors (flagged or unflagged), or list only the unflagged sectors discovered during the scanning.

Perform the following procedure to scan any hard disk in the system:

1. Type **5** and press <**CR**> to select **Scan Hard Disk for Bad Sectors.** The following screen appears (you may not see the information in square brackets):

```
 Scan Hard Disk for Bad Sectors

 Ø - Drive - Ø
[1 - Drive - 1]
[2 - Drive - 2]

Enter a drive number from the above selection
->
```

2. Enter a **Ø, 1,** or **2** to indicate which hard disk drive you are checking. For example, type **Ø** for a one-drive system. The screen displays:

```
Drive x configuration: xxxx cylinders  x heads

Flagged sectors and bad sectors are displayed at the
  end of program pass.
Press <CR> to begin or <ESC> to quit
```

3. Press <**CR**> to start scanning the disk. The system counts through all cylinders and heads. One pass takes approximately four minutes.

4. Watch the screen (or take a four minute break) while the program scans the hard-disk drive number you selected. The program displays both flagged and unflagged bad sectors as it finds them. The message **Record not found** indicates an unflagged bad sector, for example:

```
cyl:187   hd:2

Hard Disk error ....  1h
Record not found
on drive 0 at cylinder 0 head 0 logical sector 9
physical sector 9
```

5. Wait for the following choices to appear:

```
Select one of the following:

1 - display all bad sectors found
2 - display bad sectors which correspond to drive
     bad sector list
3 - display bad sectors which don't correspond
     to drive bad sector list
4 - execute scan for bad sectors program again
5 - exit

->
```

6. To view the bad sector list, type **1**. The program identifies the bad sectors by drive number, cylinder, head, logical sector, physical sector, and status (such as **FLAGGED, STATUS ID,** or **UNFLAGGED.** The **STATUS ID** message indicates an unflagged bad sector.

7. To view the bad sector list currently stored on track Ø, type **2**.

8. To view sectors that are bad but not entered on the current list, type **3**. When you type **3**, make a note of any unflagged bad sectors, and flag them immediately.

9. To flag a new bad sector, type **5** to exit this utility. After the Main Menu appears, type **4** to select the **Flag Hard Disk Bad Sectors** utility. Then follow the steps in the next subsection.

1Ø. Keep an up-to-date hard copy list of all bad sectors by copying the bad sector printout for each drive unit and updating it as necessary. You will need the information if you ever have to reflag the sectors as described in the next subsection.

11. Type **5** to exit; then press any key, such as the <space bar>, to return to the Utilities Menu. You may select another utility, or exit from the program.

FLAG HARD DISK BAD SECTORS

CAUTION

If there are any files on the hard disk, make a backup copy of the files before you continue. Setting a bad sector flag blocks off any information in the sector you flag.

There are two occasions when you may need to flag hard disk bad sectors:

1. If you need to mark (flag) new bad sectors which occur on the hard disk during operation. (A new bad sector is a disk flaw area that develops after the original list was created at the factory.) This may never occur, but if it does you will receive an operating system message similar to:

```
hard disk error drv x cyl xxxx hd x sec xx

                    or

marginal sector drv x cyl xxxx hd x sec xx
```

2. If you experience a serious problem with the hard disk which requires recalibrating the drive. (Recalibration involves reformatting track Ø on the hard disk.)

Drive Serial Number

A hard copy printout of the bad sectors is included with each hard disk drive. Each drive has a sticker with a serial number (to see the serial numbers you must remove the front panel as described in Chapter 4). The flaw list printout has the same serial number.

Entry Mode

Some hard disk suppliers identify sectors using the number of bytes offset from index, while others use physical sector numbers. The SDX software lets you enter sector information using any of these methods.

NOTE

You may have to reinstall the operating system software if you flag a hard disk sector in a swap area. Refer to your operating system manual for details.

Perform the following procedure to flag a hard disk bad sector:

1. Type **4** to select the **Flag Hard Disk Bad Sectors** utility. The following information appears (you may not see the information in square brackets):

```
 Flag Hard Disk Bad Sectors

 Ø - Drive - Ø
[1 - Drive - 1]
[2 - Drive - 2]

 Enter a drive number from the above selection
 ->
```

2. Enter a **Ø**, **1**, or **2** to indicate which hard disk drive you are checking. For example, type **Ø** for a one-drive system. The screen displays:

```
Select one of the following:

1 - display bad sector list
2 - add an entry to the bad sector list
3 - delete an entry form the bad sector list
4 - save the bad sector list to disk and exit
5 - exit


->
```

3. Type **2** to select **add an entry to the bad sector list.**

4. Wait for the following display to appear and select the mode you will use to enter the bad sector locations. If you don't know what mode you

need, refer to the previous paragraph titled **Entry Mode.**

```
Select which mode you will use to enter bad
sector data:

1 - decimal number in bytes from index
2 - hexadecimal number in bytes from index
3 - decimal number for logical sector number
4 - decimal number for physical sector number
```

5. Type in a **1, 2, 3,** or **4.**

6. Type in the bad sector information after the appropriate prompt in the following display. (Only one of the prompts in the square brackets will appear.)

```
Enter Cylinder Number (0 - 511):
Enter Head Number (0 - 7):
Enter Logical Sector Number (0 - 7):
[Enter Physical Sector Number (0 - 7):]
[Enter Bytes Offset from Index (10240):]
```

NOTE

If you decide that you do not want to flag a bad sector, press <**ESC**> and <**CR**>. Pressing <**ESC**> will take you out of the **Flag Hard Disk Bad Sectors** utility and return you to the Main Menu without changing the sector information on the hard disk.

7. Wait for the following prompts to appear:

```
Entry accepted and added to list...
Enter information followed by <Retn>
  or press <ESC> to quit
```

8. If you do not wish to enter another sector, press <**ESC**>. If you wish to continue flagging bad sectors, press <**Retn**> .

9. If you are sure that you want to add this bad sector to the list on cylinder Ø, type **4** to select **save the bad sector list to disk and exit.** The screen displays:

```
Are you sure?  (y/n)?
```

If you are sure, answer **y** (yes). The program will not add the new bad sector to the list unless you take this step!

10. If you do not want to add this the sector to the list on cylinder Ø, type **5** to select **exit without change.** The screen asks: **Are you sure? (y/n)?.** If you are sure, answer **y.** The program will not add the new bad sector to the list if you answer **y.**

NOTE

If you mistakenly flagged a sector or wish to remove the flag from a sector that has proven to be good, perform the following procedure for unflagging a bad sector.

Unflagging a Bad Sector

Perform the following procedure to remove the flag from a flagged bad sector:

1. Type **4** to select **Flag Hard Disk Bad Sectors** from the Utilities Menu.

2. Type in the number of the hard disk drive you wish to access (Ø, 1, or 2).

3. Type **1** to display the current bad sector list. Make a note of the number in the leftmost column on your screen. You will enter this number to delete the flag.

4. Type **3** to select **delete an entry from the bad sector list.** Enter the number of the sector you want to unflag.

5. If you are sure you want to revise the bad sector list, you must type **4** to select the option **save the bad sector list to disk and exit.** The program will not change the bad sector list unless you take this step!

HARD DISK FORMAT

Use the **Hard Disk Format** utility to reformat the hard disk.

CAUTION

This utility destroys all data on the hard disk and requires that you back up all files onto tape or floppy disks before you format the hard drive. Once the hard disk has been formatted, the operating system will have to be reinstalled onto the hard disk.

Perform the following procedure to format the hard disk:

1. Press **6** to select the **Hard Disk Format** utility. The following display appears:

```
Hard Disk Format
Ø - Drive - Ø
1 - Drive - 1
2 - Drive - 2

Enter a drive number from the above selection

->
```

2. Enter the number of the drive that you wish to format. The display asks:

```
Would you like to reconfigure the drive information
on Drive? y/n
->
```

3. Press **y** (yes). A warning appears:

```
Warning - This utility will overwrite the contents
of the hard disk. Do you want to continue? (y/n)
```

4. Press **y** again to format the hard disk. The program counts sequentially through the cylinders as they are formatted and displays:

```
Formatting Hard Disk Drive Ø

Cylinder XXXX

Press any key to return to the utility menu.
```

5. When the hard disk drive has finished formatting all the cylinders, press any key to return to the Utilities Menu.

RECONFIGURE HARD DRIVE

Use the **Reconfigure Hard Drive** utility to change the hard disk drive configuration. This utility will reconfigure a hard disk drive that is configured incorrectly, or one that is added to the system.

Perform the following procedure to reconfigure a hard disk drive:

1. Press **7** to select the **Reconfigure Hard Drive** utility. The following display appears:

```
Reconfigure Hard Drive

Ø - Drive Ø
1 - Drive 1
2 - Drive 2

Enter a drive number from the above selection
->
```

2. Enter the number of the drive that you wish to reconfigure. The following display appears:

```
Drive x configuration information:

Maximum cylinders..................  xxxx
Maximum heads......................  x
Maximum sectors....................  xx
Sector size........................  xxx
Track skew.........................  x
Sector Interleave..................  x
Maker..............................  manufacturer
Megabytes..........................  xx
Precomp............................  xxxx

Would you like to see the bad sector list on drive x?
```

3. Press **y** (yes) to display the bad sector list for the drive you selected:

```
        Bad Sector List on Drive X
  # Cylinder Head Logical Sector Physical Sector Byte Range
  x   xxx     x          xx            xx        xxxx-xxxx
        Bad Sector List on Drive x is x
        Press any key to continue.
```

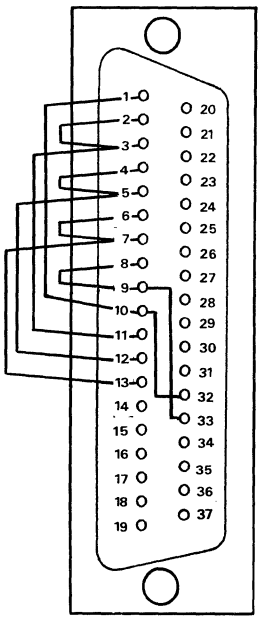
4. Press any key to return to the Utilities Menu.

APPENDIX D
LOOPBACK CONNECTORS

INTRODUCTION. D-3

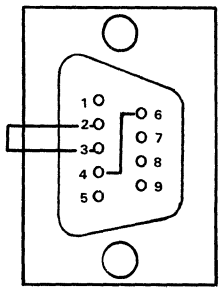
INTRODUCTION

This appendix shows the proper jumper connections for assembling the loopback connectors required to perform the parallel printer and serial communications (SIO) diagnostic tests described in Chapter 5, Troubleshooting. The parallel printer loopback connector uses a Centronix 37-pin connector (see Figure D-1) and the serial communications (SIO) connector uses a 9-pin D-type (DE-9P) subminiature connector (see Figure D-2).



REAR VIEW

Figure D-1. Parallel Printer Port Loopback Connector



REAR VIEW

Figure D-2. Serial Communications (SIO) Loopback Connector

APPENDIX E
ADJUSTMENT PROCEDURES

TAPE PHASE LOCK LOOP ADJUSTMENT.....E-1

TAPE PHASE LOCK LOOP ADJUSTMENT

CAUTION

The phase lock loop adjustments on the controller PCB are performed at the factory and normally do not require readjustment. If you cannot read from or write to the streaming tape, the phase lock loop MAY be out of adjustment. However, DO NOT make any adjustments before first checking to determine if adjustment is necessary.

Perform the following procedure to adjust the streaming tape phase lock loop reference level (refer to Figure E-3 for jumper and adjustment locations):

1. With the tape drive inactive, set R21 and R22 to nominal center.

2. Connect the channel A and B probes of a 50 MHz dual-channel oscilloscope as follows:

   a. Channel A to pin 10 of IC at location 14B.
   b. Channel B to test point D.

3. Set the oscilloscope horizontal time base to trigger on the rising edge of the signal on channel B. Set the oscilloscope trigger for minimum holdoff and the sweep rate for 0.1 microsecond/division.

4. Set the oscilloscope for an uncalibrated sweep and adjust the variable sweep rate so that the rising edge to rising edge of the channel B waveform is 8 major divisions with the first rising edge on the first major graticule line.

5. Adjust R21 so that the leading edge of the negative-going pulse on channel A is on the center graticule line as shown in Figure E-1.

6. Connect jumper C and adjust R22 so that the duration of the jitter on the the second rising edge of the channel B waveform is Ø.8 major division as shown in Figure E-2.

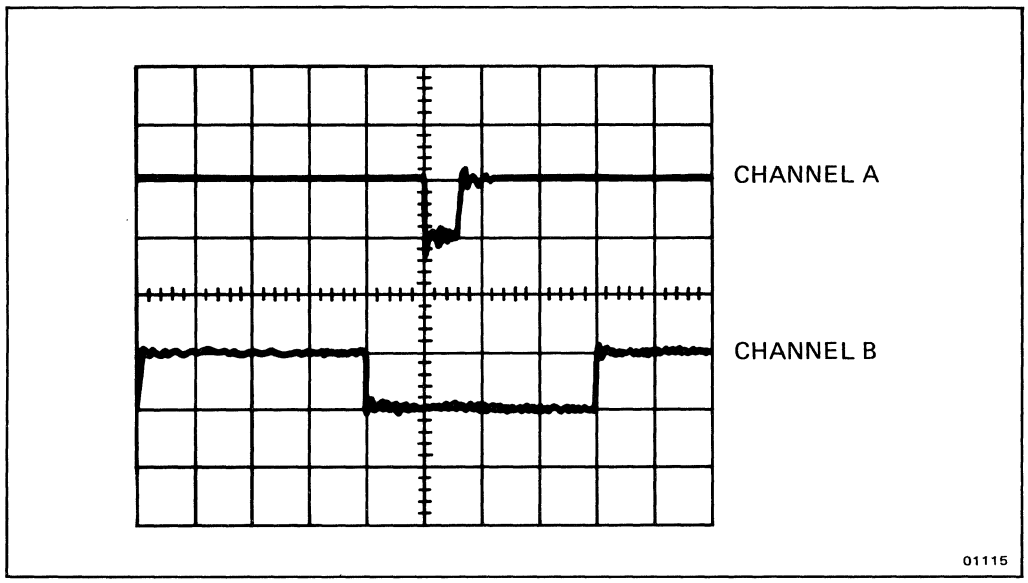


Figure E-1. Channel A and B Waveforms

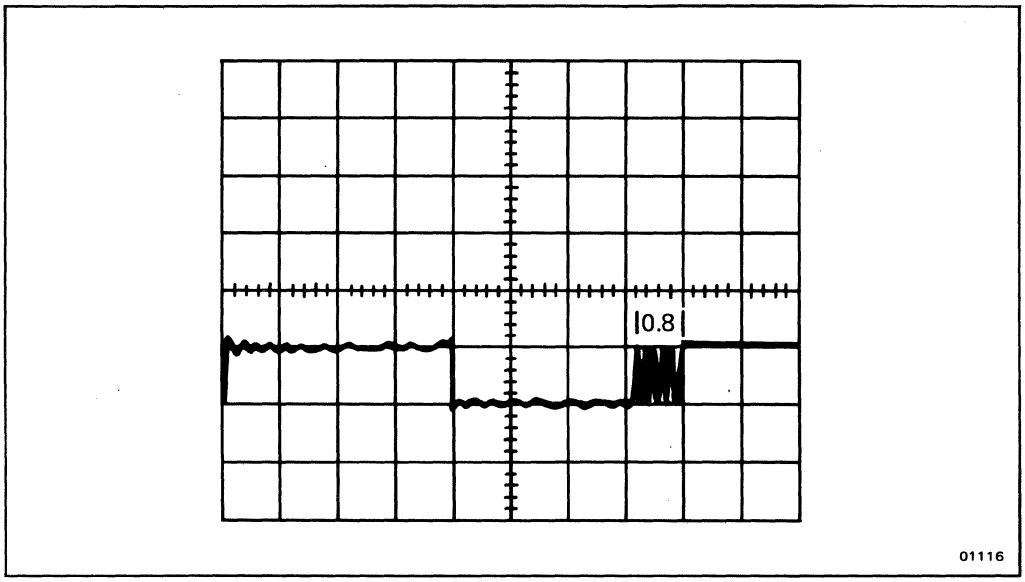


Figure E-2. Channel B Waveform

7. Disconnect jumper C and check that the leading edge of the negative pulse on channel A is on the center graticule line as shown in Figure E-1. If not, readjust R21.

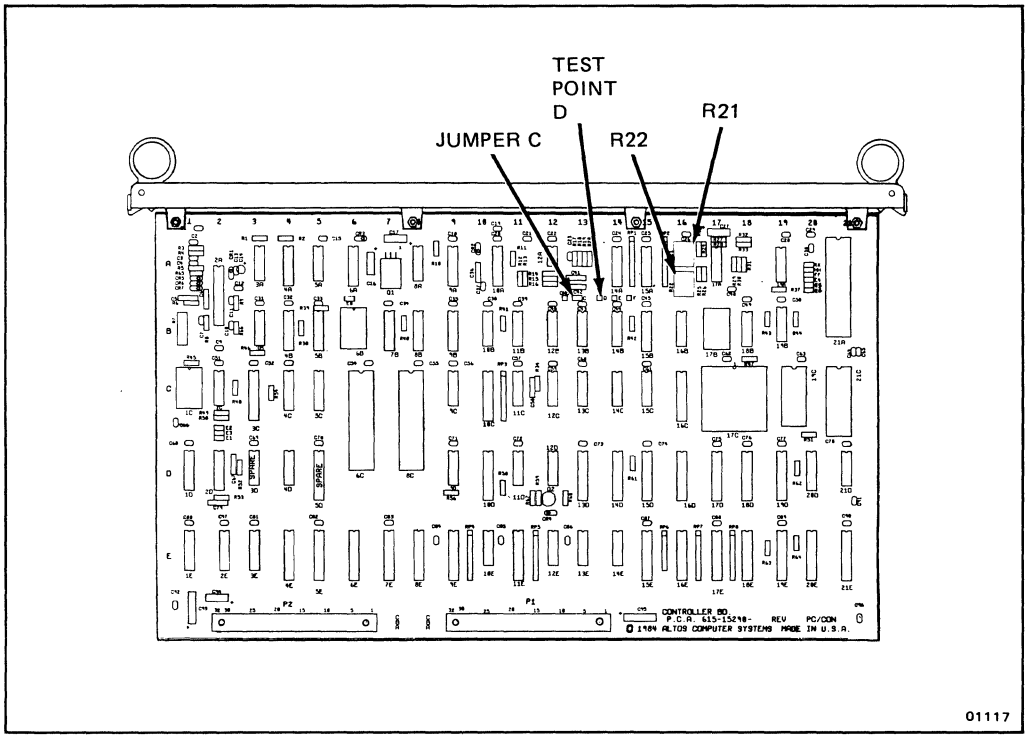


Figure E-3. Jumper and Test Point Locations (Controller PCB)

GLOSSARY

A

Accessing: The act of entering data into or retrieving data from a memory device.

Application Program: A program written to perform a specific user task as opposed to development or utility programs.

Architecture: A design or orderly arrangement.

ASCII: American Standard Code for Information Exchange. A standard 7-bit digital code (8 bits including parity check) for each of 96 graphic characters and 32 control characters.

Associating Cache: A type of memory in which data is retrieved by comparing a key against the contents of each location rather than first accessing the address of each location. The key is a copy of all or part of the data being retrieved. This type of search is faster over limited amounts of data.

Asynchronous: A nonclocked method for data transmission where the interval between the data is variable. For RS-232, the transmitted characters are preceded by a start bit and followed by a stop bit which permits a variable interval between characters.

B

Backplane: A printed circuit board that contains the system bus and provides the interconnections between the PCBs, main power supply, and drives. The PCBs and drives plug into the backplane.

Bandwidth: Relates to the speed of transmission through a channel; the greater the bandwidth, the higher the transmission speed (usually measured as the baud rate).

Baud: The number of signal events per second. One baud equals one bit per second in a train of binary signals.

Bit-Serial Format: A method of sequentially transfer ring a contiguous set of bits, one at a time, over a single line.

Block-Transfer Mode: A mode where the I/O processor moves a block program.

Boot: Prepare the computer for use by loading the operating system into memory from either a floppy disk or a hard disk.

Breakpoint: A specific stopping point in a program (usually indicated by a breakpoint flag) that inter rupts the program to permit checking, cor- recting, or modifying the program before con- tinuing execution.

Buffer: A device inserted between two other devices or program elements for the purpose of matching the electrical interfaces. Buffers are also used for matching two different data rates by providing intermediate storage.

Burst Mode: A file processor mode that causes data transfer in short bursts followed by periods of inactivity. This mode prevents the file proces- sor from locking the system bus for excessive periods of time.

Bus Master: The device controlling the current system bus transactions.

Byte-Select Field: Refers to the particular byte or bytes within a block of memory which is to be read/written to the cache memory.

Byte-Swap Logic: A logic concept where the two bytes in a 16-bit word are interchanged (swapped).

C

Cache Memory: A high-speed low-capacity memory used as a buffer between the CPU and system memory to allow faster access for instructions and data.

Call: Refers to the process of bringing a program, routine, or subroutine into effect by specifying the entry conditions and jumping to an entry point.

Cascade: Refers to two or more similar devices arranged in tandem; the output of one connected to the input of the other.

CIO: Counter/Input/Output. A device that acts as a general-purpose counter/timer to provide bit set/test functions and acts as an interrupt controller for miscellaneous inputs.

Code: A system of characters and rules for representing information.

Coercivity: A measure of how tightly two adjacent bits can be recorded on magnetic media and still be read; the higher the coercivity, the better the quality.

Coherency: On the CPU PCB, the cache memory is considered coherent when the data in the cache is in agreement with the data in system memory. Thus, the cache can be trusted by the CPU.

Complement: The opposite of a given quantity.

Concatenate: To join two or more character strings or bits end-to-end to form a larger word or string.

Concurrent: Refers to the handling of multiple instructions or the operations of different instructions simultaneously.

Context Switching: Refers to switching from one process to another. Context switching is per formed by the operating system.

Contiguous: Sharing a common boundary or edge.

CPU: Central Processing Unit. The primary functioning device of the computer that synchronizes the operation of the computer system. It fetches control instructions stored in memory and then decodes, interprets, and performs the programmed instructions. The term CPU is used to describe a single integrated circuit (microprocessor) and also the expanded CPU subsystem (PCB) that contains memory, timing, control logic, and communications interface to other subsystems.

CRC: Cyclic Redundancy Check. A method for detecting transmission errors in serial data streams. A check bit is appended to the data stream and then the resulting bit stream is divided by a selected poly nomial. If there are no errors, the remainder should be zero.

Cued: Refers to waiting for service based on the order of arrival.

D

Daisy Chain: Refers to an interconnect method where several devices share the same signal path. The daisy chain method reduces the cost of interconnection and requires that the devices timeshare the signal path.

Data Block: A contiguous group of data bytes.

Data Pattern: A sequence of characters that are repeated throughout a memory area.

Debugger: A software program that performs tests of computer routines for locating software errors and correcting them.

Decode: To disassemble or translate a code into its meaning. For example, a decoder assigns a one bit meaning to each of the eight possible three-bit codes.

Decrement: To decrease the value of a number.

Delimiter: A character that limits a string of characters or separates and organizes items of data.

Development System: A computer system especially designed for developing firmware and software.

Diagnostics: Refers to a user-inserted test program for isolating hardware malfunctions to a subsystem or major circuit.

Direct Map: Refers to a type of storage medium that provides dynamic allocation of memory.

DMA: Direct Memory Access. A method to gain direct access to system memory without involving the CPU.

Download: The process of moving a program from the primary to the secondary controlling device, which results in the secondary device becoming activated.

E

Execute: The process of interpreting an instruction and performing the indicated operation(s).

F

False: Refers to the zero (Ø) or low state in Boolean algebra.

Fileserver: A device that manages controllers which, in turn, create, delete, or retrieve data files from storage devices, such as disks or tapes.

Firmware: Refers to software programs or instructions that have been permanently stored in a ROM control block.

Flag: An indicator, usually a single binary bit, used to inform a later section of a program that a condition had occurred.

Footprint: Refers to the physical space provided in the chassis to accommodate a subassembly (module).

Formatted: Disks are considered formatted after a pattern has been written on the disk that divides the disk storage area into addressable sectors.

Fragmentation: A condition resulting from some dynamic storage-allocation algorithms, in which unallocated storage is dispersed in many small areas.

Full-Duplex: Refers to an operation that allows simultaneous communication in both directions between two points.

H

Half-Duplex: Refers to an operation that allows communication in either direction, but not simultaneously, between two points.

Handshake: Exchange of predetermined signals between a transmitting and receiving device to establish synchronization.

Hit: Refers to a cache search operation. When an address in the tag memory matches a read address from the CPU, a cache hit occurs which indicates that the data wanted by the CPU is stored in the cache memory. See Miss.

Host: Refers to the primary or controlling device.

I

Increment: To increase in quantity or value.

Initialize: To set a program, system, or device to an original state.

Interactive Diagnostics: Refers to diagnostics procedures where the user can communicate directly with the operating program.

IOP: Input/Output Processor. Refers to a device that is capable of moving data between main memory and peripheral devices while the CPU is performing other tasks.

IPL: Initial Program Load. Refers to the program stored in the PROM that performs local power-up and initialization of the file processor and communications PCBs during the boot process.

L

LAN: Local Area Network. A system for interconnecting computers within a limited area using data-link control to establish paths, manage message transactions, and free lines for other users. WorKnet is an LAN system.

Latency: The time required by the computer to deliver information from memory. In a disk drive, the average time required for a sector to come under the read/write head once the heads are on track (for a 3600 rpm disk, latency is 8.33 milliseconds).

Long Word: A 32-bit unit of information.

Loop: A self-contained series of instructions in which the last instruction can modify and repeat itself until a terminal condition is reached.

Loopback Mode: A mode of operation where transmitted data is returned to the sending end for comparison with the original data.

M

Macro: A form of instruction used to generate a debugging program testing capability that is completely under the user's control.

Main CPU: The central processing unit on the CPU PCB.

Main Console: The console connected to serial communications port Ø from which diagnostic testing is performed. Also called master or system console.

Map: A listing of the variable names, array names, and constants used by the program, with their relative address assignments.

Maskable Interrupt: A single interrupt request input that can be masked by software with the reset ting of the interrupt-enable status (flag) bit.

Mass Storage Device: Refers to a peripheral storage device with a large storage capacity (magnetic disk and tape).

Master: Refers to a controlling device (console, CPU, etc.).

Minicomputer: Refers to the classification of computers with higher performance than microcomputers. Generally these computers are characterized by a proliferation of high-level languages, operating systems, and networking methodologies.

Miss: Refers to a cache search operation. When an address stored in the tag memory does not match the read address from the CPU, a cache miss occurs which indicates that the data wanted by the CPU is stored in system memory and not in the cache memory. See Hit.

Model C Compiler: A high level programming language designed to optimize run time, size, and efficiency. C compiler supports the basic data types, such as bytes, long and short integers, floating-point numbers, and pointers to all data types.

Modem: Refers to a MODulation/DEModulation device that modulates digital signals to enable the computer to communicate over telephone circuits.

MULTIBUS: Refers to a type of intel bus similar to the 32-bit bus used by the Altos 2086.

Multisector Transfer: A transfer of more than one sector at a time.

N

Networking: Refers to the interconnecting of computers through network communications channels.

NMI: Nonmaskable Interrupt. An external interrupt that cannot be ignored by the microprocessor.

Nonmaskable Interrupt: See NMI.

O

Offset Field: Refers to the cache memory address of the block location within a page of memory.

Operating System: A basic group of programs that perform computer debugging, input/output, accounting, compilation, and storage assignment tasks.

Out-Of-Bounds Error: A logical address, for which no matching physical address is found, generates an out-of-bounds error.

Overlapped Seeks: A hard disk controller with this capability can initiate a seek on a second (or third) drive before the first drive has completed a seek operation.

P

PAL: Programmable Array Logic. An array of logic circuits that are custom programmed by the factory to process input signals.

Packet: Refers to a group of bits, including data and control elements, that are transmitted as a whole.

Page: A subdivision of physical memory into equal sized blocks called frames. The logical address space of a task is divided into pages. The operating system controls the allocation of pages into page frames. Paging is used in virtual memory systems.

PCB: Printed Circuit Board. Sometimes called etched circuit board or printed circuit assembly (PCA).

Peripheral: Refers to an external device that enables the computer to communicate with the outside world, but is not part of the basic computer unit (storage devices, modems, terminals, etc.).

Phase-Locked Loop: A circuit that is synchronized in phase and frequency with a recieved signal.

Physical Address Space: Refers to the addressable storage sites or locations available in a memory device.

Pointer: A word that gives the address location of another memory location.

Port: A collection of individual I/O lines. Device terminals that provide electrical access to a system or circuit.

Power-Up: Refers to the orderly initialization of the CPU at power-on time so that the proper sequence of events can occur.

Protocol: A set of conventions, or rules, between communicating processes relating to the format and content of messages to be exchanged.

R

Real Time: Refers to a task that must be started and completed within a certain time limit or the task will fail.

Refresh: A process of constantly reactivating or restoring information that decays or fades when idle. Pertains to dynamic memory devices.

Register: A memory device capable of containing one or more computer bits or words. A register has zero-memory latency time and negligible memory access time.

Remote Diagnostics: Refers to a method for diagnostic testing the computer system via a communications modem through a main or master console located some distance away.

Reset: To restore a storage device to a prescribed state.

Resident Program: Refers to a program that is permanently located in memory.

Ripple: Slang for shifting data patterns (used by diagnostics).

RS-232: The Electronic Industries Association (EIA) interface standard for transmitting asynchronous binary serial data between the computer and data terminal equipment (printers, terminals, modems, etc.).

RS-422: The Electronic Industries Association (EIA) interface standard for transmitting high-speed digital data between the computer and data terminal equipment (printers, terminals, modems, etc.).

S

Scatter Loading: A process for loading a program into system memory in such a way that each section or segment of the program occupies a single connected memory area (page), but the several sections of the program need not be adjacent to each other.

SCC: Serial Communications Controller. A dual-channel multifunction peripheral component designed to satisfy a wide variety of serial data communications requirements. The SCC is capable of handling synchronous or asynchronous protocols.

SCSI: Small Computer System Interface. Generally used for connecting additional peripheral devices to a computer.

Scroll: Refers to the method of viewing extra lines or pages of nondisplayed data on a terminal by pressing the appropriate keys.

SDLC: Synchronous Data Link Control. A protocol for the management of data transfer via a data communications link.

SDX: Service Diagnostics. Refers to a field service diagnostics program contained on a floppy disk included with the 1086/2086.

Sector: Refers to the short segments (cones) in which tracks of data are stored on a floppy disk.

Segmented: Refers to a program that is divided into an integral number of parts, each of which performs a part of the total program and is short enough to be completely stored in memory.

Semaphores: Conditional input/output used to synchronize the data transfer between the computer and a peripheral device.

Serial Port: Refers to an I/O port through which data is transmitted and recieved in a digit-by-digit time sequence.

Single-Address Mode: A method of transferring data, used by the Hitachi HD6845Ø, in which data is transferred around the DMA integrated circuit rather than through it. In contrast, dual-address mode first transfers data into the DMA integrated circuit and then to the destination (sometimes called fetch deposit cycle).

Software: Refers to the programs or routines, usually supplied on a disk or in software documents, that are prepared to simplify programming and computer operations (operating systems, assemblers, compilers, utility, and application programs).

Source Code: Refers to the high level code in which the software is written. Source code is generally considered proprietary.

Stack: A reserved area of memory where the CPU auto matically saves the program counter and the contents of working registers when a program interrupt occurs.

Standalone: Refers to an independent system that does not depend on another system for its operation.

Strobe: A pulse used for loading registers or flip-flops.

Subassembly: Refers to a subordinate assembly that comprises a part of the computer system. Subassemblies include mass storage devices, power supplies, backplane, and plug-in PCBs.

Subsystem: Refers to the portion of a subassembly that performs one of the major system functions. Subsystems include the major circuits contained on the plug-in PCBs.

Synchronous: Refers to an operation that occurs at regularly timed intervals, usually synchronized by a clock.

Syntax: Refers to a the structure or arrangement of characters, such as spaces and commas, that gives a language control information.

System Console: Also called the master or main console. Refers to the controlling terminal or console for performing diagnostic tests or programming operations.

System Memory: Refers to the internal main memory contained on the memory PCB.

T

Tag Field: A portion of a data or address word that contains the key to the word. The key is used to locate the word during a cache search operation. Sometimes called key field.

Tag Memory (RAM): A random access memory which contains the necessary address information for determining the presence of data in the CPU cache memory.

Throughput: Refers to the speed with which problems, programs, or segments are performed by the system.

Timeout: Refers to the time interval allotted for certain operations to occur before the system is interrupted and must be started again.

Time Slice: Refers to a portion of the total available time allocated to a particular task to allow other tasks to be performed.

Toggle: Refers to a change of states.

Transceivers: A device that can both transmit and recieve signals.

Translation Memory: Also called translation table memory. Refers to the memory device that correlates relocated addresses with real addresses.

Transparent: Refers to the moving of information through a device in such a way that the content of the data does not affect the processing operation.

True: Refers to the one (1) or high state in Boolean algebra.

U

UPS: Uninterruptable Power Source. Refers to a device that automatically switches to utility power when the AC line power is interrupted without disturbing computer operation.

Unformatted: Refers to magnetic media (tapes or disks) that have no data and no track or sector format information stored on them.

Universal Parameter Block: A temporary storage area in system memory used for passing instructions and status between the CPU and its slave microprocessors.

V

Vector Interrupt: A type of interrupt that uses a vector (pointer) which points to the starting address of a specific interrupt service routine.

Virtual Address Space: The total memory space allocated on peripheral storage devices that maps directly into system memory.

Virtual Memory: Refers to a technique which allows the programmer to use a larger address space than is available in system memory. The operating system automatically uses secondary memory (usually a disk) to store and retrieve parts of the currently executing program when the address space in system memory is exceeded.

W

Wait State: Refers to the insertion of a state while waiting for an event to occur.

Window: A rectangular portion of memory which acts as a logical subterminal.

Word: A 16-bit unit of information usually occupying one storage location in memory.

Write-Through: Refers to a write operation whereby the CPU writes to system memory and to cache memory in the same operation. Thus, it appears that the CPU is writing through the cache memory. Write-through is one of the methods required to assure that the cache memory matches the system memory.

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ALTOS 1086/2086
SCHEMATIC DIAGRAMS

NOTE

Additional copies of this schematic diagram supplement to the maintenance manual are available by ordering part number 690-19942-XXX. Contact your Altos distributor or Altos Customer Services for availability of updated revisions to this supplement.

SYSTEM BLOCK DIAGRAM

CENTRAL PROCESSING UNIT (CPU) PCB DIAGRAMS
ASSY. NO. 615-18035-XXX & 615-15152-XXX

MEMORY PCB DIAGRAMS
ASSY. NO. 615-16509-XXX & 615-15146-XXX

COMMUNICATIONS (SIO) PCB DIAGRAMS

FILE PROCESSOR PCB DIAGRAMS

CONTROLLER PCB DIAGRAMS

BACKPLANE PCB DIAGRAMS

LOW-PASS FILTER PCB DIAGRAMS

LED PCB DIAGRAMS

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HOW TO USE THE DIAGRAMS

The diagrams contained in this document are provided to supplement the information in the **1086/2086 Maintenance** manual. The **1086/2086 Maintenance** manual references these diagrams to help service personnel troubleshoot the 1086/2086 circuitry.

The first sheet in this supplement is the system block diagram. Each block represents a single plug-in PCB or subsystem. The system block diagram identifies the plug-in PCBs in the system.

The diagrams are grouped by PCB. Each group of plug-in PCB diagrams is preceded by a block diagram for that PCB. (Block diagrams are not included for the backplane, low-pass filter, and LED PCBs.)

Earlier versions of the PCBs are included by PCB assembly part number and are identified by the black index tabs.

The following information describes how to quickly locate diagrams in this supplement.

Locating the PCB Diagrams

Perform the following procedure to quickly locate all the diagrams for a PCB:

1. Determine the name of the PCB (from the system block diagram for plug-in PCBs) that contains the circuit you want.

2. Find the name of the subsystem PCB you want in the contents on the preceding page.

3. Follow the red arrow to the edge of the diagrams and look for the red (or black for earlier versions) index tabs where the arrow points. These tabbed pages are all the diagrams for the PCB you want.

Locating a Schematic Diagram

Perform the following procedure to quickly locate a specific schematic diagram:

NOTE

This procedure covers the plug-in PCBs which have a number of schematic diagrams. The backplane, low-pass filter, and LED PCBs have one schematic diagram and are easily located by an index tab.

1. Locate the desired group of diagrams as described under **Locating the PCB Diagrams.**

2. Find the subsystem PCB block diagram on the first page of the group of diagrams you located in step 1.

3. Locate the block for the circuit you want. Note that inside or over each block is the sheet number(s) of the diagrams for that circuit as shown in the following example:

4. Flip through the diagrams and watch the index tabs for the sheet number of the diagrams you want.

Locating a PCB Part

To make it easier to locate electrical parts, there are letter and number (X-Y) coordinates etched on the PCBs.

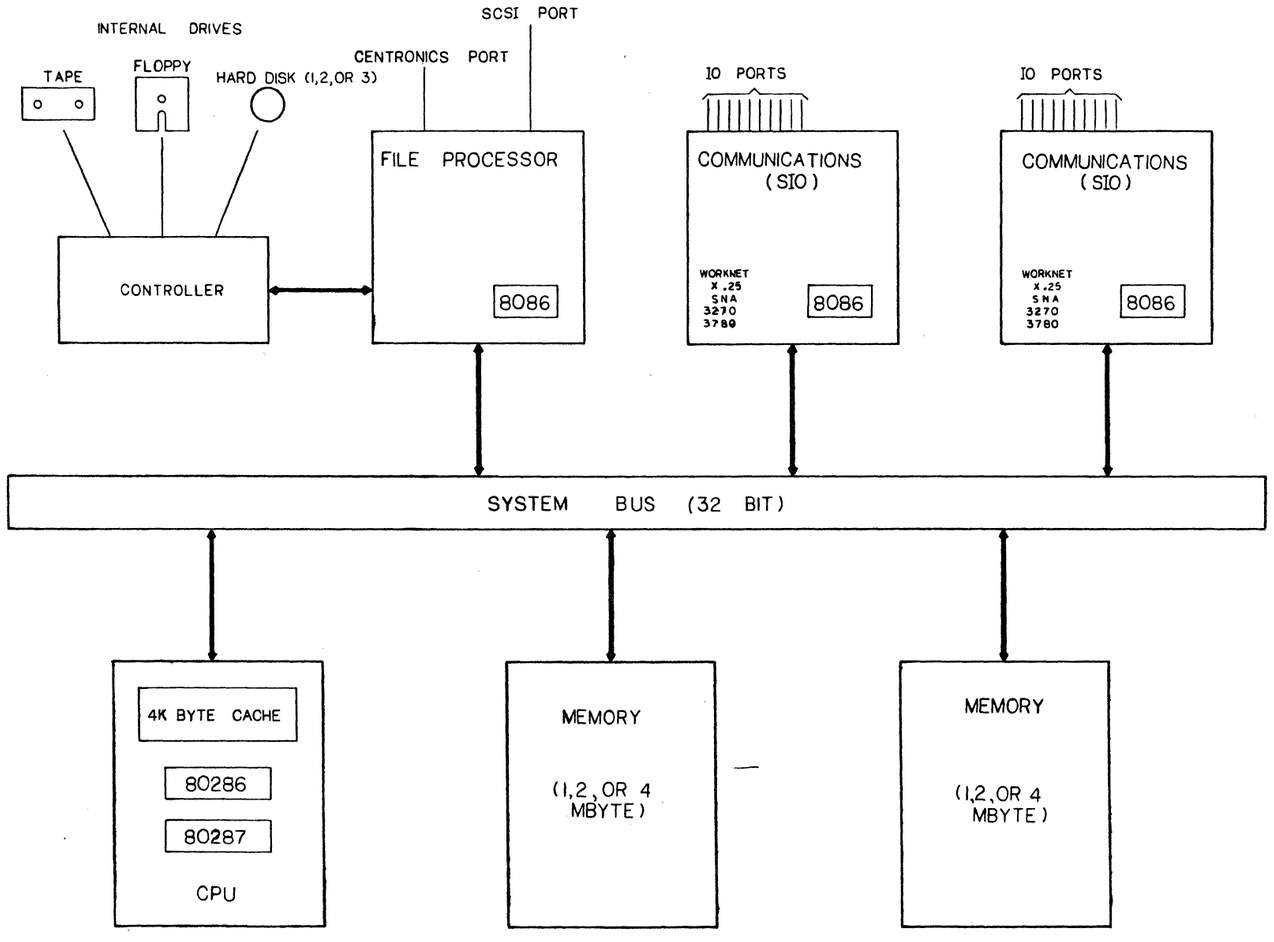
These coordinates are used on the schematic diagrams and parts lists to identify the integrated circuits (ICs). When convenient, row and column coordinates are etched on the edges of the PCB. For very densely populated PCBs, the ICs may be individually identified with a location number etched on the PCB near the IC.

For example, an IC identified as **B1Ø** on the schematic diagram is located in the area intersected by row B and column **1Ø** on the PCB. Sometimes more than one coordinate system is used on the same PCB due to the part density. If so, the coordinates are clearly etched either near the ICs or around the edge of a specific area on the PCB. All other parts are identified on the PCB in the conventional manner (R=resistor, C=capacitor, J=connector, etc.).

SYSTEM BLOCK DIAGRAM

DWG NO	SH	REV
625-16724-001	1	A

REVISIONS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
X1A		PROTOTYPE	2-26-85	
1A		PRE-PRODUCTION EO 3155	30 MAR 85	
A		PROD. REL. EO 3544-H	8-29-85	



SYSTEM BLOCK DIAGRAM

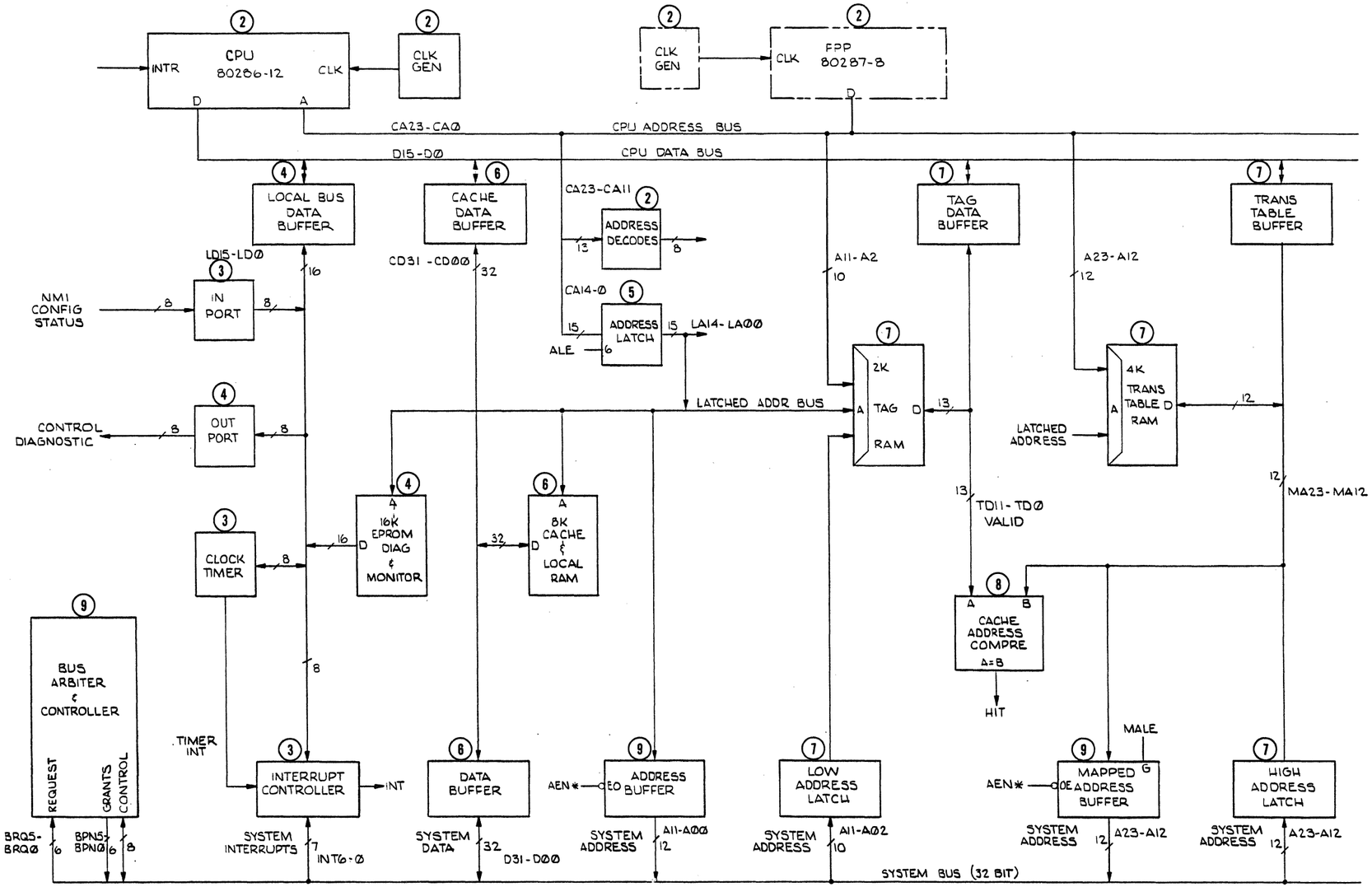
ALTOS COMPUTER SYSTEMS

CPU PCB
BLOCK DIAGRAM
615-18035-XXX

12.5 MHz

DWG. NO. 625-18037-XXX	SH	REV. 3A

REVISIONS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1 OF SCHEM.		



CPU PCB BLOCK DIAGRAM

ALTOS COMPUTER SYSTEMS

CPU PCB SCHEMATIC DIAGRAMS 615-18035-XXX

1 1

DEVICE LOCATION CHART

REF DESIG.	DEVICE TYPE	POWER PINS GRD	POWER PINS +5V	SPARE ELEMENT OUTPUT PINS	DEVICE LOCATION SHT NO.
1A	SRAM 1KX4	9	18		7
2A	SRAM 1KX4	9	18		7
3A	SRAM 1KX4	9	18		7
4A	SRAM 1KX4	9	18		7
5A	74F244	10	20		7
6A	74ALS245	10	20	11,12,13	7
7A	PAL20L8A	12	24		2
8A	74F521	10	20		8
9A	74F373	10	20		3
10A	74F244	10	20	3,7	3,4,7
11A	74ALS245	10	20		7
12A	74ALS245	10	20		7
13A	74F04	7	14	10	3,4,7
14A	74LS30	7	14		2
15A	8284A	9	18		2
16A	74F174	7	14		5
17A	74F08	7	14	8	5
18A	74F139	8	16		8
19A	74S157	8	16		8
20A	58167A	12	24		3
21A					
22A					
23A					
24A	74ALS32	7	14		2,3,4
25A	74LS273	10	20		4
26A	74LS244	10	20		3
27A	74ALS74	7	14		3
28A	SP-2				
1B	PAL16R8A	10	20		5
2B	PAL20R8A	12	24		5
3B	SP-1				
4B	74F373	10	20		3
5B	74F373	10	20		7
6B					
7B	74F244	10	20	12,14	7
8B	74F373	10	20		7
9B	74F373	10	20		3
10B	74AS27	7	14		2
11B					
12B	80286	9,35 60	30 62		2
14B					
15B					
16B	80287	9,30	10		2
17B					
18B					
19B	74F138	8	16		4
20B	74ALS245	10	20		4
21B	74LS161A	8	16		4
22B	74ALS245	10	20		4
23B	74ALS640	10	20		6
24B	74ALS640	10	20		6
25B	74ALS640	10	20		6
26B	74F74	7	14		3,4
27B					
28B	74ALS640	10	20		6

DEVICE - LOCATION CHART

REF DESIG.	DEVICE TYPE	POWER PINS GRD	POWER PINS +5V	SPARE ELEMENT OUTPUT PINS	DEVICE LOCATION SHT NO.
1C	OSC 19.66MHz				9
2C	74F521	10	20		8
3C	74F244	10	20		7
4C	74F244	10	20		7
5C	74F373	10	20		7
6C	SP-3				
7C	74F174	7	14		5
8C	SRAM 4KX4	10	20		7
9C	SRAM 4KX4	10	20		7
10C	SRAM 4KX4	10	20		7
11C	74F534	10	20		7
12C	74F534	10	20		7
13C	74ALS08	7	14		3,4,5
14C	74F534	10	20		7
15C	7406	7	14		4,7
16C	74ALS245	10	20		7
17C	PAL20R8A	12	24		5
18C	PAL20R8A	12	24		5
19C	PAL20R8A	12	24		4
20C	74ALS04	7	14	12	3,4,5,6
21C	2764A	14	28		4
22C	2764A	14	28		11
23C	SRAM 2KX8	12	24		6
24C	SRAM 2KX8	12	24		6
25C	SRAM 2KX8	12	24		6
26C	SRAM 2KX8	12	24		6
27C					
28C					
1D	74F74	7	14		5,9
2D	74F74	7	14		5
3D	74F74	7	14		3,5
4D	74F02	7	14		3,5,8
5D	74AS1004	7	14		2,5,7,9
6D	74F74	7	14		2
7D	74F10	7	14		2
8D	OSC	7	14		2
9D	PAL16R8B	10	20		2
10D	PAL16L8A	10	20		9
11D	PAL16R4A	10	20		9
12D					
13D	74ALS240-1	10	20		9
14D	74ALS240-1	10	20	12,14,16,18	9
15D	74AS533	10	20		9
16D	74AS533	10	20		9
17D	74LS14	7	14	4,6,8,10,12	2
18D	74LS20	7	14		3,5
19D	74F244	10	20		5,9
20D	74LS240	10	20		3
21D	8259A	14	28		3
22D					
23D	74ALS645-1	10	20		6
24D	74ALS645-1	10	20		6
25D	74ALS645-1	10	20		6
26D	74ALS645-1	10	20		6
27D					
28D					

DEVICE LOCATION CHART

REF DESIG.	DEVICE TYPE	POWER PINS GRD	POWER PINS +5V	SPARE ELEMENT OUTPUT PINS	DEVICE LOCATION SHT NO.

DWG. NO. 625- 18037-XXX	SH 1	REV. 3A

REVISIONS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
X1A		PROTOTYPE	9 JAN 86	
X2A		PROTOTYPE		
X3A		PROTOTYPE	6 MAR 86	
3A		PRE-PROD RELEASE EO 4221-A SR	10 MAR 86	

VERSION TABLE	
-001	6MHZ W/O NUM PRCSR
-002	8MHZ NUM PRCSR
-003	12.5 MHZ W/O NUM PRCSR
-004	12.5 MHZ NUM PRCSR

16 55 NS FOR -001,-002
25 NS FOR -003,-004

15 120 NS FOR -001,-002
55 NS FOR -003,-004

14 32.0 MHZ FOR -001, -002
50.0 MHZ FOR -003,-004.

13 5.0 MHZ 80287 FOR -002 ONLY
8.0 MHZ 80287 FOR -004 ONLY.

12 IC 8284A IS USED ON -004 ONLY.

11 8MHZ FOR -001,-002.
12.5 MHZ FOR -003,-004.

10. FOR PC CONFIGURATION SEE DRAWING NO. 610-18034-001
9. FOR PCB FABRICATION DRAWING SEE DRAWING NO. 630-18038-001
8. FOR PCB ASSEMBLY DRAWING SEE DRAWING NO. 615-18035-001
7. ABBREVIATIONS ARE PER ALTOS DRAFTING MANUAL SECTION 1.0 .
6. REFERENCE DESIGNATIONS ARE PER ALTOS DRAFTING MANUAL SECTION 2.0
5. GRAPHIC SYMBOLS ARE PER ALTOS DRAFTING MANUAL SECTION 3.0 AND 3.1 .
4. TRANSISTORS ARE 2N3906
3. DIODES ARE IN6263
2. CAPACITOR VALUES ARE IN MICROFARADS .
1. RESISTORS ARE 1/4 W ,±5%. RESISTANCE IS IN OHMS .

NOTES: UNLESS OTHERWISE SPECIFIED .

REFERENCE DESIGNATION BLOCK	
LAST USED	NOT USED
C69	C22,42,43
CR4	
E12	E5
R82	R2,12,21,23 R42,43,48, R55,68,69, R10
RP21	RP3,4,14
Q1	
P2	

CPU PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV.
625-18037-XXX	2	3A

REVISIONS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

SHT 3 P/U-1
SHT 4 AACK *
SHT 5 P/U-2
SHT 10 MRST *
SHT 5 ACK *
SHT 9 AEN *
SHT 5 MALE
SHT 4 LBSR *
SHT 5 CSR *
SHT 5 TTSR *
SHT 5 ACK2 *
SHT 5 MWT
SHT 3 INT
SHT 3 NMI
SHT 3 LAT 287 SEL *
SHT 3 LAT ADDR BUS LA1, LA2
SHT 4 RD *
SHT 4 WR *
SHT 5 P/U-3

OSC 8D 14 MHz
F74 6D
AS1004 5D
R66 33
R65 1K
C69 33 PF
R64 4.7K
Q1 2N3906
R56 27
CR4 IN4148
R45 10K
R44 51Ω
C44 68UF 6V
F244 10A
R46 100
C31 33PF
E8
LS14 17D
R67 33
PAL16R8 9D
READY
CLK3
CLK2
CLK1
RESET
OE
R63 390
F10 7D
F11 7D
R7 510
R8 510
Y1 24 MHz
R9 1K
E6
R52 1K
8284A 15A
ASYNC *
RES *
RDY 2
CSYNC
AEN1 *
RDY 1
AEN2 *
F/C
R81 27
E6
82288 16B
NPSI
CMD1
CMD0
NPRD *
NPWR *
NPS2
CKM
PEREQ
PEACK *
ERROR *
BUSY *
82286 12B
C20 .047UF
SO *
S1 *
COD/INTA
PEREQ
PEACK *
ERROR *
BUSY *
HLDA
HOLD
BHE *
M/IO *
LOCK *
R11 20K
R10 20K

CPU CLK * SHT 3,5
CLK 3 SHT 4
SAACK 1 * SHT 5
WAIT SHT 4
READY * SHT 4,5
RESET SHT 4,5
CPU ADDR BUS A0-A14 SHT 3
A2-A23 SHT 7
A0, A1 SHT 9
AD1 * SHT 3,4
ULC10 * SHT 3
EPROM * SHT 3,4
BMEM * SHT 5,9
C10 * SHT 5
T10 * SHT 5
TT10 * SHT 5
B10 * SHT 5
LBS * SHT 4
CAD * SHT 5
BHE * SHT 3
MEM SHT 4
PLOCK * SHT 3
COD SHT 4
S1 * SHT 4,5,9
S0 * SHT 4,5,9
CPU DATA BUS D0-D12, D0-D15 SHT 4,6,7

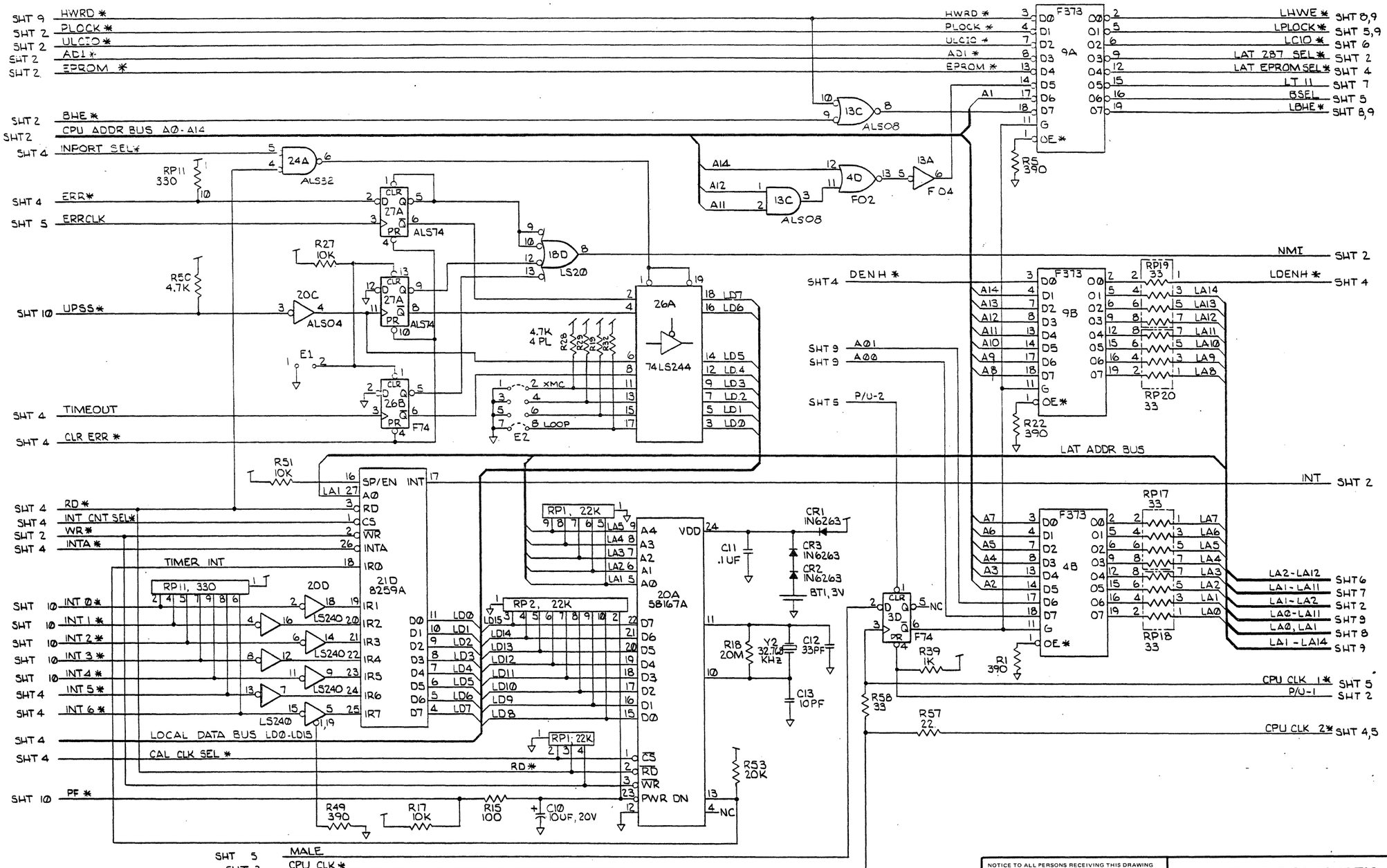
LS30 14A
ALS32 24A
AS27 10B
PAL20L8 7A
CADDEC
EP
MALE
MEM
RDY *

CPU PCB SHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO. 625-18037-XXX	SH. 3	REV. 3A

REVISIONS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



CPU PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV.
625-18037-XXX	4	3A

REVISIONS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

SHT 3 LAT ADDR BUS LA1- LA14

SHT 2 LBS *
SHT 2 AD1 *
SHT 2 READY *
SHT 2 MEM
SHT 2 COD
SHT 2 S0 *
SHT 2 S1 *
SHT 3 CPU CLK 2 *
SHT 2 WAIT
SHT 2 EPROM *
SHT 5 READ1 *
SHT 2 CLK 3
SHT 5 ENTIME
SHT 3 LAT EPROM SEL *
SHT 5 READ 2 *

LA7 LA8 LA9 LA10

198 F138

RP21 33

LBCONT PAL20R8 19C

LA9 LBS* AD1* RDY* CALS* MEM COD/INTA SO* SI* CK RD*

RD* WR* 1B DEN* NC NC NC

RP21 33

R37 390

LDENH* SHT 3

R54 100
C68 33PF

R30 10K R31 10K R26 10K R25 10K
D12 D13 D14 D15

20B ALS245

22B ALS245

D15 D14 D13 D12 D11 D10 D9 D8
D7 D6 D5 D4 D3 D2 D1 D0

LD15 LD14 LD13 LD12 LD11 LD10 LD9 LD8
LD7 LD6 LD5 LD4 LD3 LD2 LD1 LD0

SHT 2,6,7 D0- D15 CPU DATA BUS
SHT 2 RESET

13A F04

R24 10K

MONITOR HI 21C-A 2764A
MONITOR LO 21C-B 2764A

LA14 LA13 LA12 LA11 LA10 LA9 LA8 LA7 LA6 LA5 LA4 LA3 LA2 LA1

ALS32 24A
13C ALS08

CAL CLK SEL * SHT 3
INT CNT SEL * SHT 3
IN PORT SEL * SHT 3
DENH * SHT 3
INTA * SHT 3
LBSR * SHT 2
RD * SHT 2,3
WR * SHT 2,3

R13 4.7K
R40 4.7K
20C AL504
15C 7406
ENP ENT A0 LOAD * 21B LS161A CLK CLR *
Z6B CLK CLR F74

ERR * SHT 3,10
XACK * SHT 10
AACK * SHT 2,5
TIMEOUT SHT 3

24A ALS 32

LD7 LD6 LD5 LD4 LD3 LD2 LD1 LD0
25A LS273 CLR *

CLR ERR * SHT 3
DB6 SHT 5
INT 5 * SHT 3,10
INT 6 * SHT 3,10
CACHE ENA SHT 5

10A F244
E4

REST * SHT 10

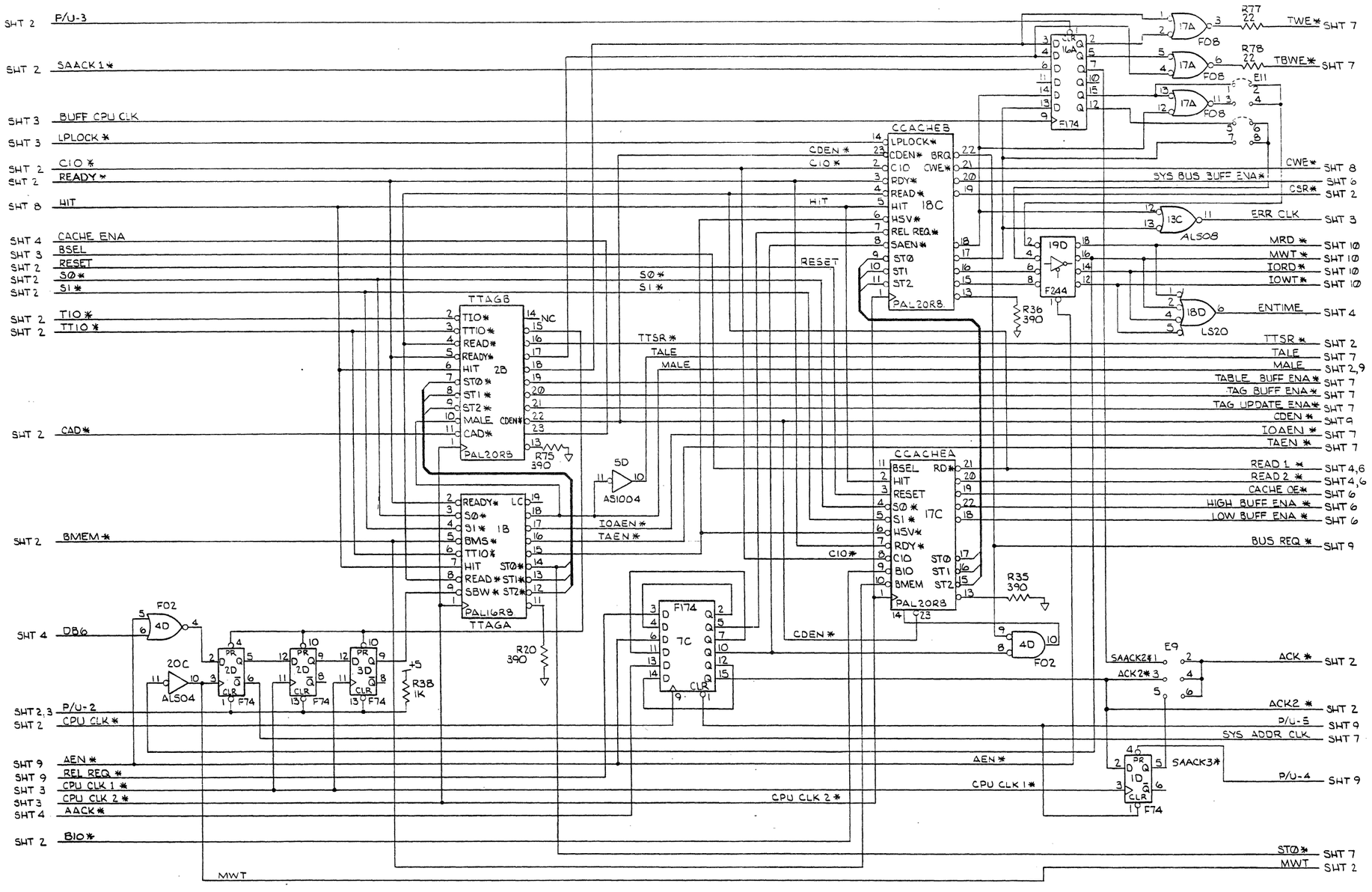
LD0 - LD15 LOCAL DATA BUS SHT 3

CPU PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH.	REV.
625-16037-XXX	5	3A

REVISIONS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

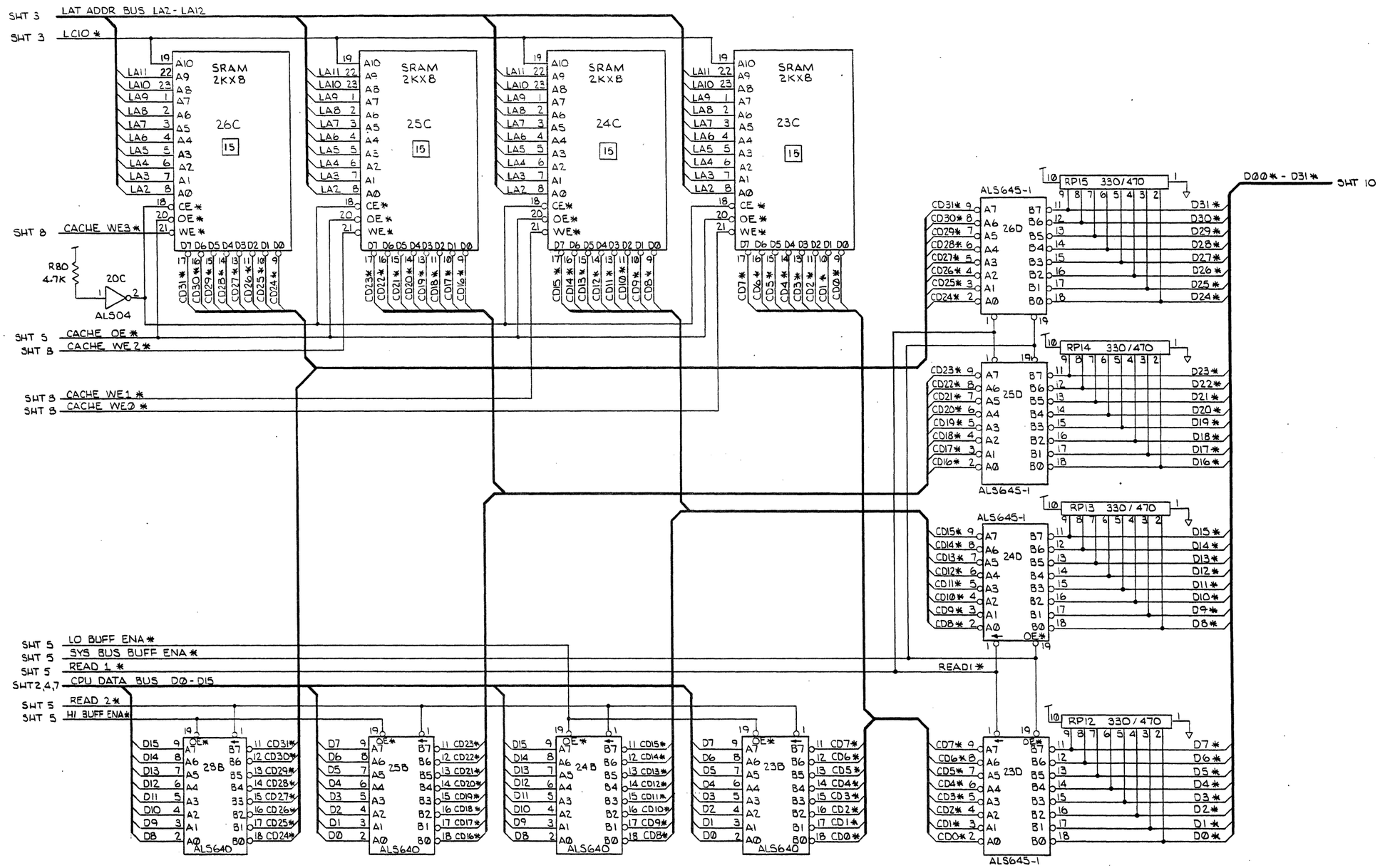


CPU PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO. 625-15037-XXX	SH. 6	REV. 3A

REVISIONS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

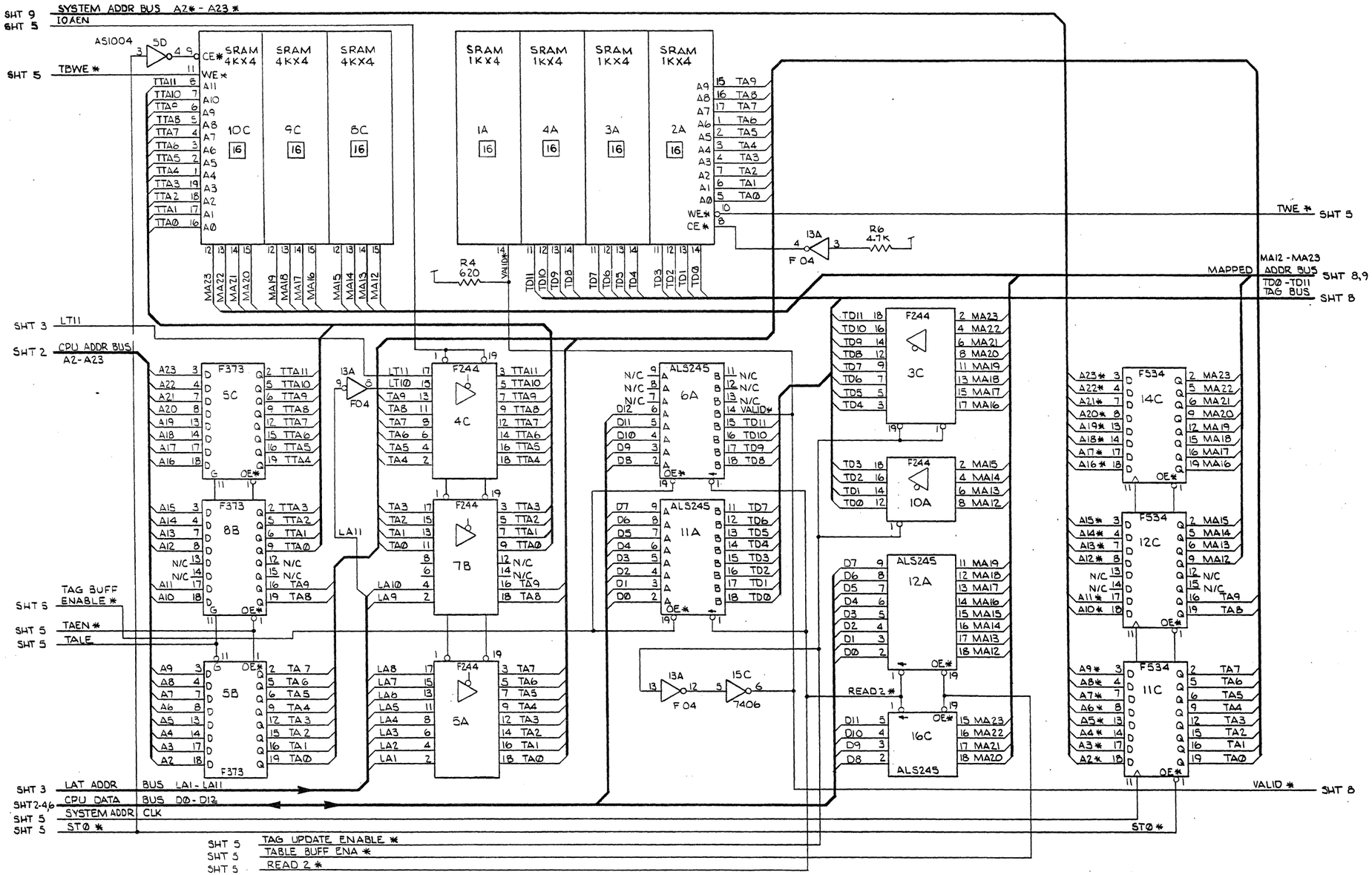


CPU PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV.
625-18037-XXX	7	3A

REVISIONS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

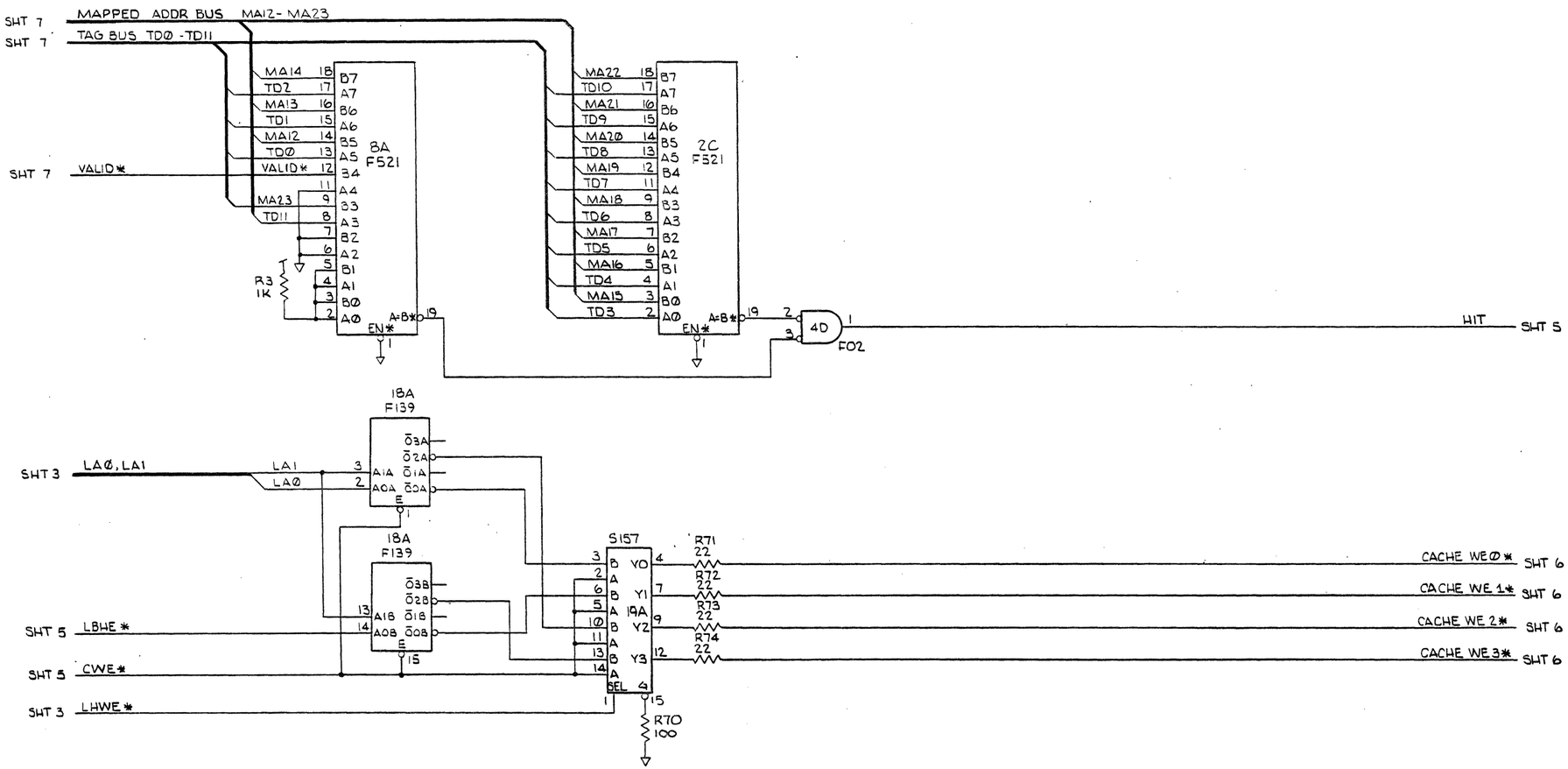


CPU PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO. 625-18037-XXX	SH. 8	RFV. 3A

REVISIONS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

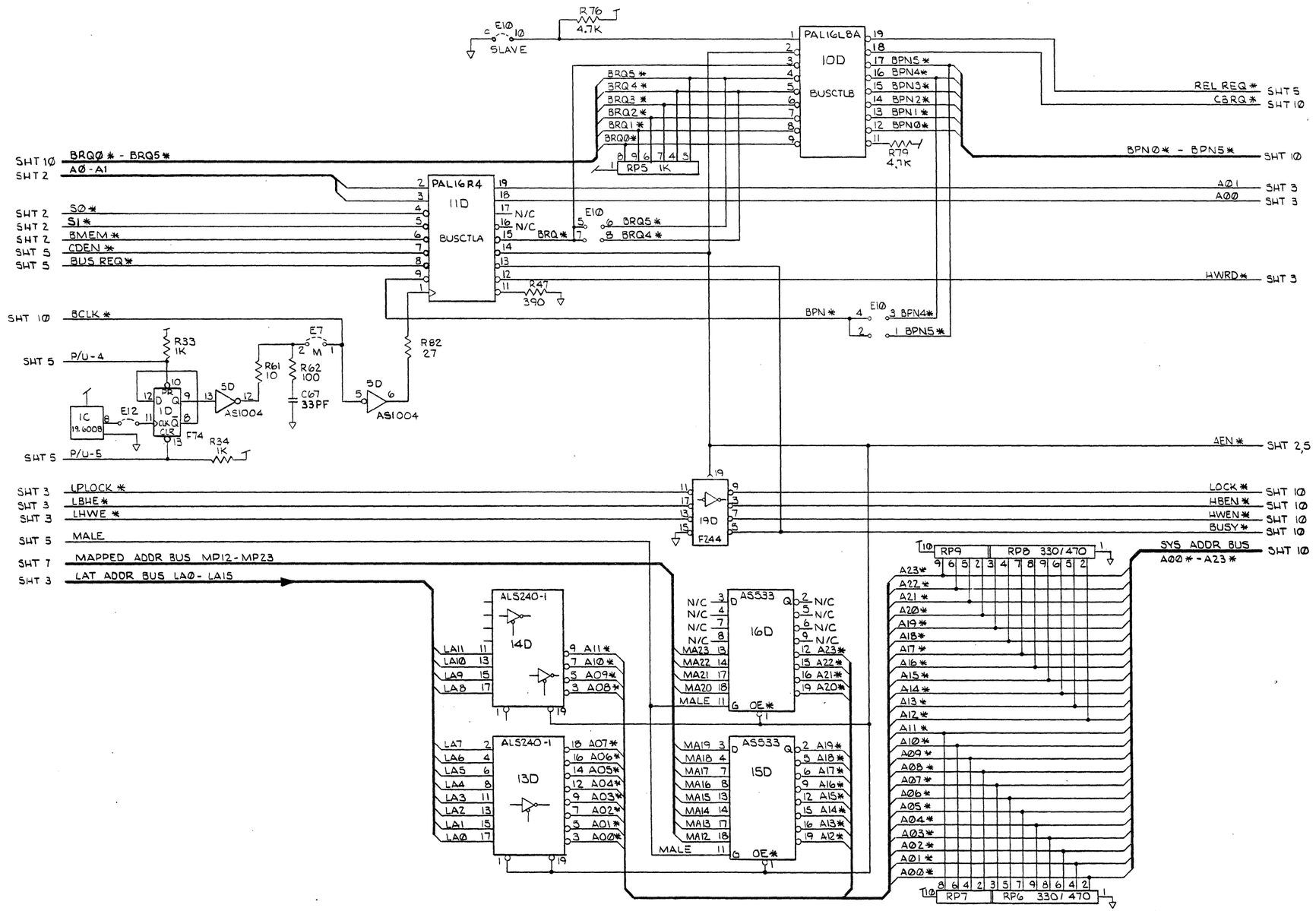


CPU PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO. 625-18037-XXX	SH 9	REV 3A

REVISIONS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

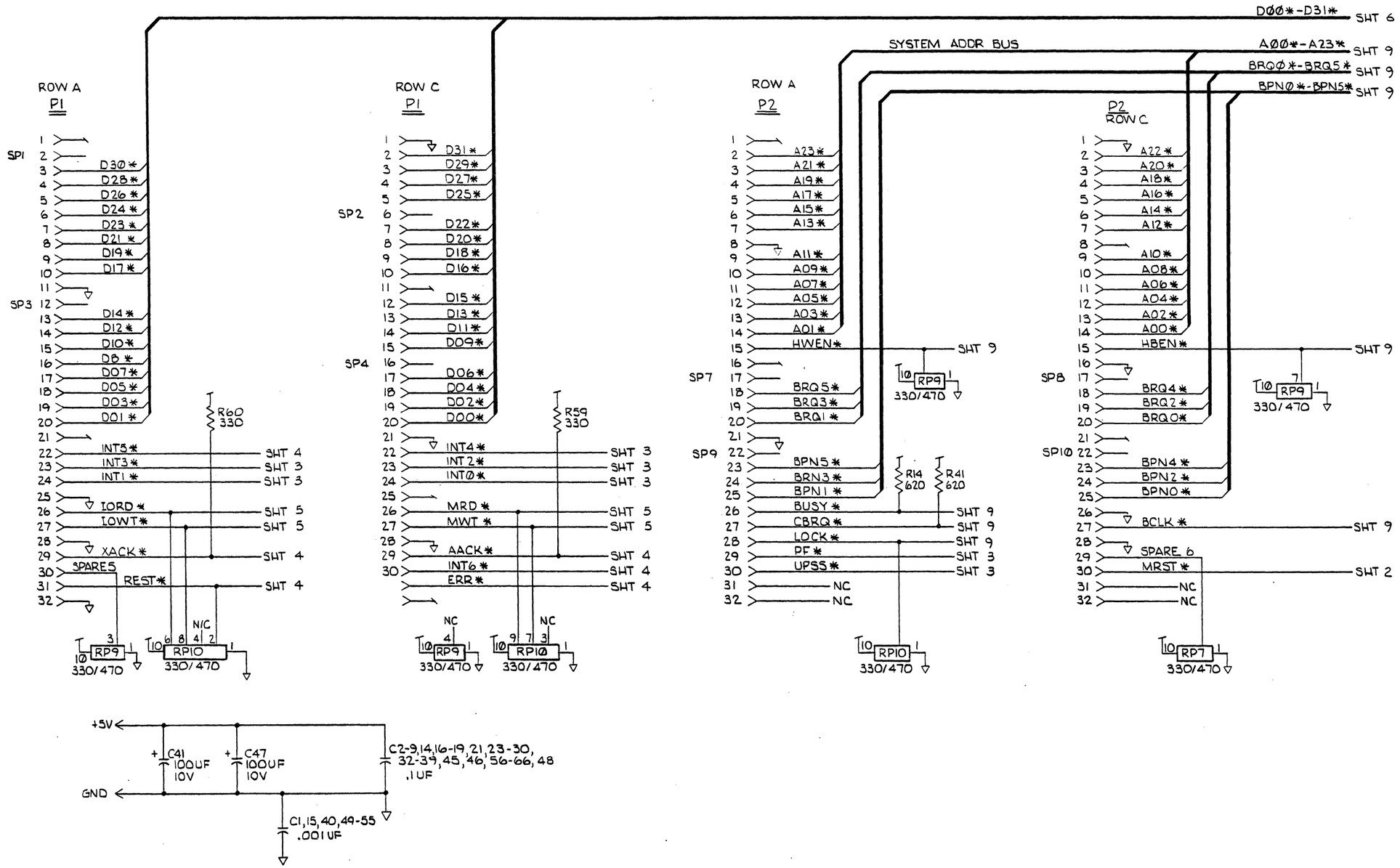


CPU PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV.
625-18037-XXX	10	3A

REVISIONS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



CPU PCB SCHEMATIC DIAGRAM

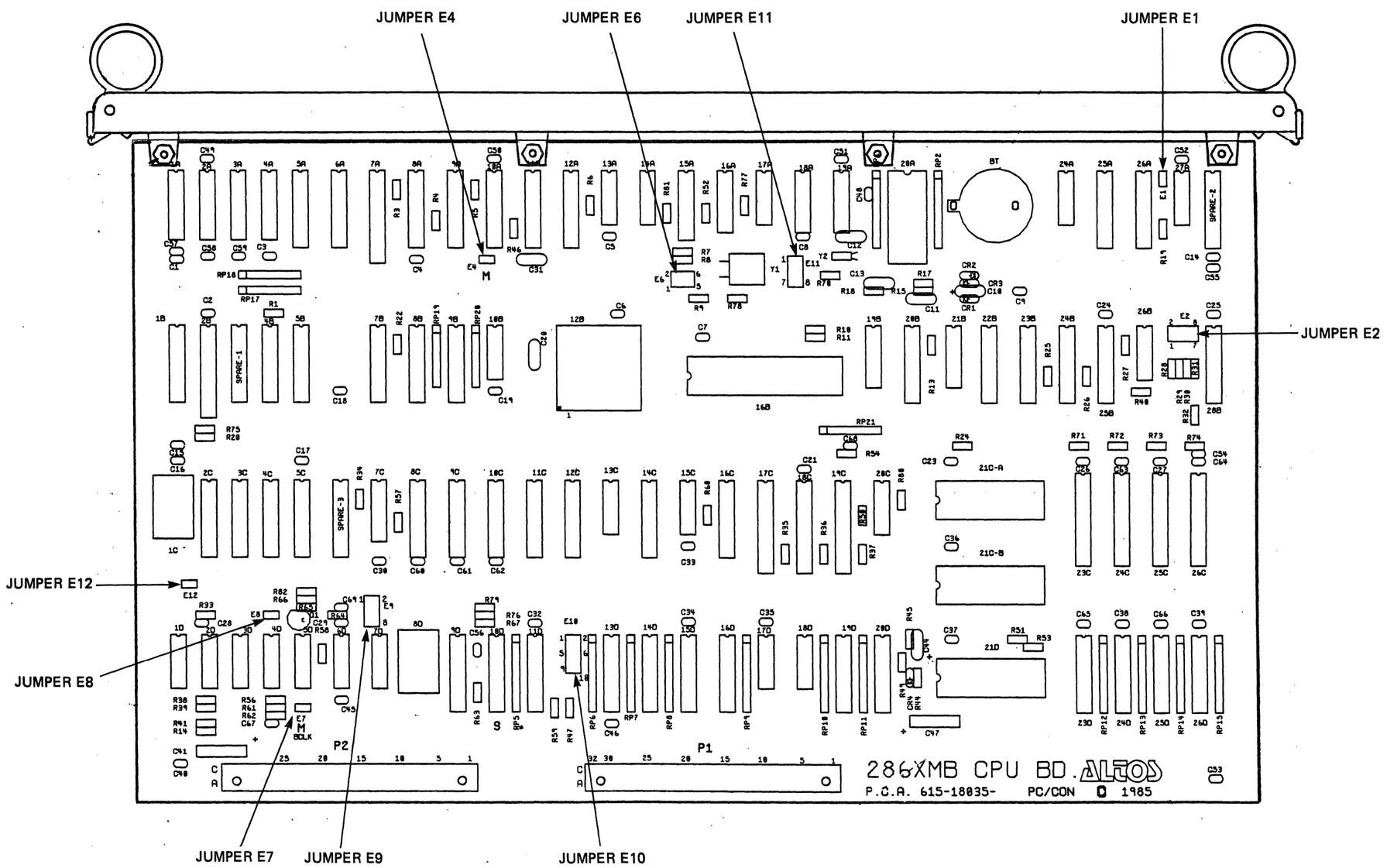
ALTOS COMPUTER SYSTEMS

CPU PCB
PART LOCATIONS
615-18035-XXX

DWG. NO.	SH	REV.
615-18035-XXX	1	4A

REVISIONS

REV.	ZONE	DESCRIPTION	DATE	APPROVED
X1A		PROTOTYPE	10-7-85	
X2A		PROTOTYPE		
X3A		PROTOTYPE	6 MAR 86	
3A		PRE-PROD RELEASE SO# 4221-H	10 MAR 86	
4A		REVISED PER EO# 4475-H	5 JUN 86	



CPU PCB PART LOCATIONS

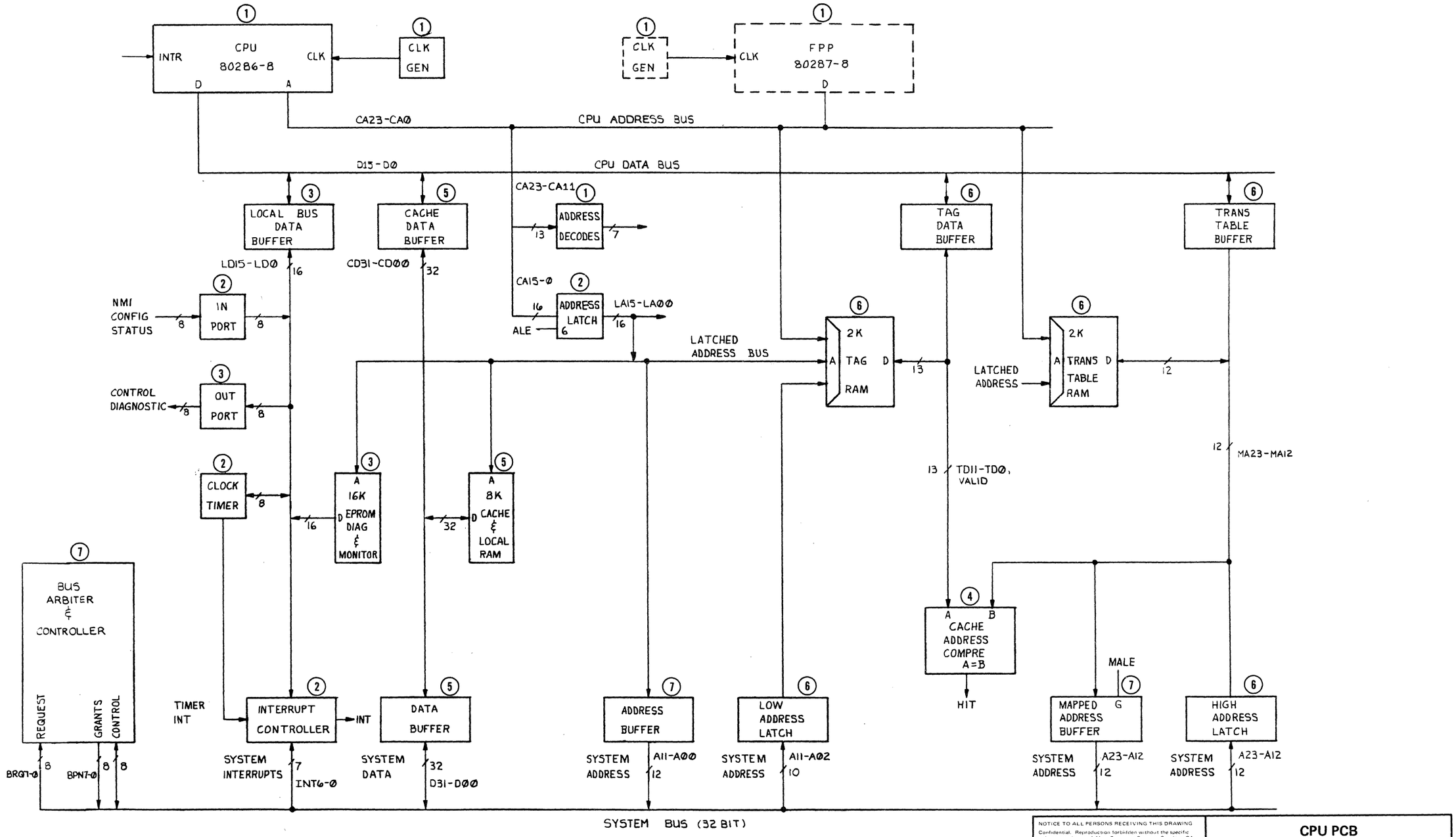
ALTOS COMPUTER SYSTEMS

CPU PCB
BLOCK DIAGRAM
615-15152-XXX

8 MHz.

DWG. NO	SH	REV
625-15154-001	9	8B

REVISIONS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
–		SEE SHEET 1 OF SCHEM.		



CPU PCB BLOCK DIAGRAM

ALTOS COMPUTER SYSTEMS

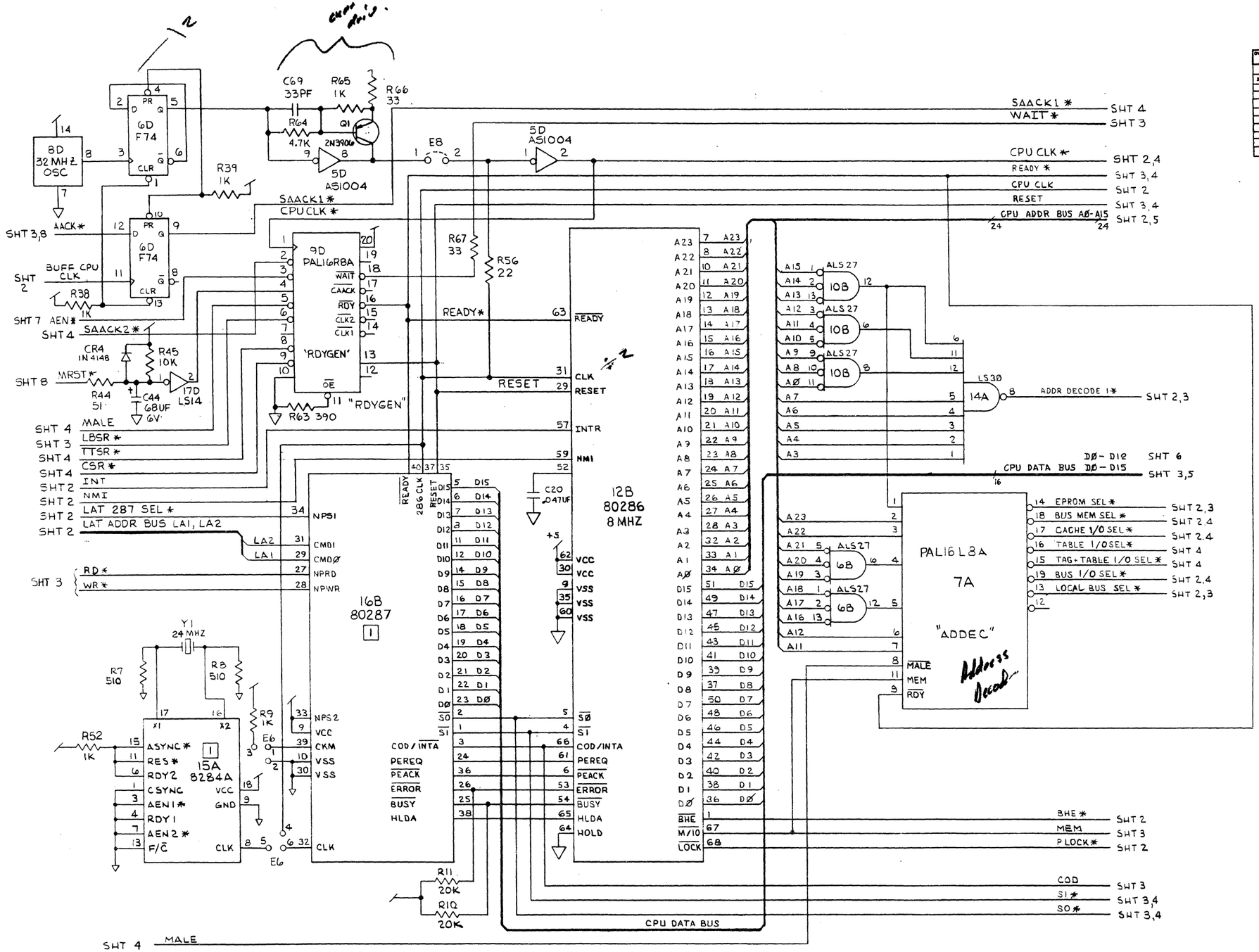
CPU PCB SCHEMATIC DIAGRAMS 615-15152-XXX

1 1

DWG. NO. 6 25-15154-XXX | SH 1 | REV B-4

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	X3A	PROTOTYPE		
	3A	PRE-PRODUCTION EO#2307	3-1-85	
	4A	CHANGES PER EO# 2932	4-19-85	
	5A	REVISED PER EO # 3079	5-30-86	
	6A	REVISED PER EO # 3110	5-30-85	
	7A	REVISED PER EO # 3134	5-30-86	
	8A	REVISED PER EO # 3226	7-10-85	
	A	PROD. REL. EO 3544-H	8-27-85	
	B	REVISED PER EO # 4606-H	CK 6-18-86	



NOTES: UNLESS OTHERWISE SPECIFIED.

[1] USED ON -002 VERSION ONLY.

2. FOR JUMPER PINNING SEE SPECIFICATION 660-16643-001

CPU PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG NO. 625-15154-XXX | SH. 2 | REV 8D

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

SHT 1 LOCAL BUS SEL *
PLOCK *
CACHE I/O SEL *
ADDR DECODE 1 *
BUS MEM SEL *
BUS I/O SEL *
BHE *
CPU ADDR BUS A0-A15
SHT 1 EPROM SEL *
SHT 3 INT PORT SEL *
system mem parity error
SHT 8 ERR *
SHT 4 ERRCLK
clocks flops
SHT 8 UPSS *
ups fail
SHT 3 TIMEOUT
SHT 3 CLR ERR *
SHT 1 RD *
SHT 3 INT CNT SEL *
SHT 1 WR *
SHT 1 INTA *
SHT 3
TIMMER INT
SHT 8 INT0 *
INT1 *
INT2 *
INT3 *
INT4 *
SHT 3,8 INT5 *
INT6 *
SHT 3 LOCAL DATA BUS LD0-LD15
CAL CLK SEL *
RD *
WR *
SHT 8 PF * active low
SHT 1 MALE
CPU CLK *
CPU CLK

24A F32
27A ALS74
20C ALS04
26B F74
LS20 18D
NAND gate (low in → hi out)
26A 74LS244
Input status port
R37 4.7K
R27 10K
4.7K (4 PL) R20 R21 R22 R24
E1 E2
R51 10K
21D 8259-2
System Interrupt Controller
IR0 Clock
IR1 - File Acc.
IR2 - $10 0
IR3 - $10 1
IR4 - $10 2
IR5 - $10 3
IR6 IR7 output port
LS240
RP11 330
R49 390
R53 20K
RP1, 22K
RP2, 22K
C10 10UF 50V
R15, 100
R17 10K
20A 58167A
Calendar /Clock
CR1 IN6263
CR3 IN6263
CR2 IN6263
BT1 3V LI MN 02
C11 .1UF
R16 200K
R18 20M
C12 43PF
Y2 32.768 KHz
C13 15PF
TIMMER INT
F373 9A
LAT LOC BUS SEL * SHT 3
LPLOCK * SHT 4,7
LC10 * SHT 5
LAT 287 SEL * SHT 1
LAT EPROM SEL * SHT 3
LAT SYS MEMSEL * SHT 7
LAT BUS I/O SEL * SHT 7
LAT BHE * SHT 4,7
R5 390
NMI SHT 1
F373 9B
RP19 33
RP20 33
R22 390
INT SHT 1
LAT ADDR BUS
F373 4B
RP17 33
RP18 33
LA0,LA1 SHT 4
LA1,LA2 SHT 1
LA2-LA12 SHT 5
LA1-LA14 SHT 3
LA0-LA15 SHT 7
LA1-LA10 SHT 6
R1 390
SHT 4 2D-1
MALE
F74 3D
R39 1K
CPU CLK * R58 33 CPU CLK1 * SHT 4
R57 22 CPU CLK2 * SHT 3,4
CPU CLK F244 10A BUFF CPU CLK SHT 1,4
R46 100
C31 47PF

CPU PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO. 625-15132-XXX	SH 3	REV 8B

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

SHT 2 LAT ADDR BUS LA1-LA14

SHT 2 LAT LOCAL BUS SEL *

R12 10K

19B F138 — LA8 1, LA9 2, LA10 3 → A, B, C; E, E, E ← 6, 5, 4; Ø 15, 1 14, 2 13, 3 12; 4 11, 5 10, 6 9, 7 7 NC

RP21 2 47; RP21 4 47

CAL CLK SEL *
INT CNT SEL *
INT PORT SEL *
} SHT 2

LBSR * SHT 1
INTA * SHT 2
RD * }
WR * } SHT 1,2

"LOCBUS" PAL20R8A 19C

SHT 1
LOCAL BUS SEL * 2 LBS
ADDR DECODE 1 * 3 ADI
READY * 4 RDY
5 CALS
MEM 6 MEM
COD 7 COD/INTA
S Ø * 9 SD
S 1 * 8 ST
SHT 2 CPU CLK 2 * 1 CK
SHT 1 WAIT * 10
SHT 1 EPROM SEL * 14 RD

22, 21, 20 RD *, 19 WR *, 18 DEN *; ST Ø 17, ST 1 16, ST 2 15, 13 NC

RP21 6 47; RP21 8 47

RD *, WR *

R50 390

SHT 4 ENTIME
SHT 2 LAT EPROM SEL *
SHT 4 READ *

R54 100, C68 47PF

R13 4.7K, R40 4.7K

20C ALS04: 8 → 9

21B LS161A: 7 ENP, 10 ENT, 9 LOAD, 15 RCO, 2 CLK, 1 CLR

26B F74: 12 D, 9 Q, 11 CLK, 13 CLR

15C 7406: 9 → 8 ERR * (PIC-31) SHT 8; 13 → 12 XACK * ((P1A-29) SHT 8; 11 → 10 AACK * (PIC-29) SHT 8 SHT 1

TIMEOUT SHT 2

24A F32: 1, 2 → 3

20B ALS245: D15 9, D14 8, D13 7, D12 6, D11 5, D10 4, D9 3, D8 2 ← A7 … AØ; OE 1, CE 19; A7 … AØ → B7 … BØ: 11 LD15, 12 LD14, 13 LD13, 14 LD12, 15 LD11, 16 LD10, 17 LD9, 18 LD8

22B ALS245: D7 9, D6 8, D5 7, D4 6, D3 5, D2 4, D1 3, DØ 2 ← A7 … AØ; OE 1, CE 19; A7 … AØ → B7 … BØ: 11 LD7, 12 LD6, 13 LD5, 14 LD4, 15 LD3, 16 LD2, 17 LD1, 18 LDØ

+5V R24 10K

R30 10K D12, R31 10K D13, R26 10K D14, R25 10K D15

8K x 8 EPROMS

21C-A 2764A, 21C-B 2764A

OE 22, CE 20, 27; LA14 26, LA13 2, LA12 23, LA11 21, LA10 24, LA9 25, LA8 3, LA7 4, LA6 5, LA5 6, LA4 7, LA3 8, LA2 9, LA1 10 → A13 … A0; D7 … DØ → 19 LD15, 18 LD14, 17 LD13, 16 LD12, 15 LD11, 13 LD10, 12 LD9, 11 LD8 | 19 LD7, 18 LD6, 17 LD5, 16 LD4, 15 LD3, 13 LD2, 12 LD1, 11 LDØ

25A LS273 output latch: LD7 3, LD6 4, LD5 7, LD4 8, LD3 13, LD2 14, LD1 17, LDØ 18 → D; 11 CLK; 1 CLR; Q → 2 CLR ERR * SHT 2, 5 DB6 SHT 4, 6, 9, 12 NC, 15, 16, 19 CACHE ENA SHT 4,7

7406: 15C 3 → 4 INTA 5 * SHT 2; 15C 16 → 2 INTA 6 * SHT 2

F244: 11 → 9, 10 → 19; E4 2 → 1 REST * SHT 8 (MASTER)

RESET * SHT 7

LDØ – LD15 LOCAL DATA BUS SHT 2

DØ – D15 CPU DATA BUS SHT 1

RESET 1 → 13A 2 ALS04

CPU PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV
625-15154-XXX	4	88

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

SHT 4,6 MAPPED ADDR BUS MA12-MA23
SHT 4 VALID *
SHT 6 TAG BUS TD0-TD11

R3 1K

8A 74F521

2C 74F521

SHT 1 SAACK1 *
SHT 2 LAT BHE *

SHT 3 CACHE ENA

F02 4D

SHT 2 LPLOCK *

HIT

SHT 1 RESET
SHT 1 CACHE I/O SEL *
SHT 1 SØ *
S1 *
READY *

TABLE I/O SEL *
TAG + TABLE I/O SEL *

"TAG B" 2B 16R8A

NC
TAG UPDATE ENA * } SHT 6
TAG BUFF ENA *
TABLE BUFF ENA *
TAG WE *
TABLE WE *
TTSR * SHT 1
CLR SBUS WR *

R21 390

"TAG A" 1B 16R8A

AS1004 5D TALE SHT6

MALE SHT 1,2,7
IOAEN * } SHT 6
TAEN *
HSV *

R20 390

SHT 1 BUS MEM SEL *

AEN *

F02 4D

SHT 3 DB6

20C ALS04

PR D 2D F74 CLR

PR D 3D Q F74 Q CLR

SHT 2 3D-1

MWT *

R38 1K

SYS ADDR CLK

F174 7C

SHT 7 REL REQ *
SHT 7 AEN *
SHT 2 CPU CLK 1 *
SHT 1 CACHE I/O SEL *
SHT 1 BUS I/O SEL *
CPU CLK 2 *
SHT 1 CPU CLK *

LA1
LAØ

18A LS00
19A LS00
17A LS00
13A ALS04

"CACHE B" 18C 20R8A

LPLOCK
CACHE EN
C10
READY
READ
HIT
HSV
REL REQ
SAEN
STØ
ST1
ST2
BRQ

"CACHE A" 17C 20R8A

HIT
RESET
SØ
S1
HSV
READY
STØ
ST1
ST2
RD

F175 3B

TWE * } SHT 6
TBWE *
SAACK2 * SHT 1
BUFF CPU CLK SHT 2
BUS REQ * SHT 7
SYS BUS BUFF ENA * SHT 5
CSR * SHT 1
ERRCLK SHT 2

F08 13C

F244 19D

R36 390

R35 390

R34 SHT 7

ST Ø * SHT 6
SYS ADDR CLK SHT 6

CACHE WE 3 *
CACHE WE 2 *
CACHE WE 1 *
CACHE WE Ø *
SHT 5

MRD * SHT 8
MWT * SHT 8
IORD * } SHT 8
IOWT *

LS20 18D

ENTIME SHT 3

READ * SHT 3,5,6,7

CACHE CE * } SHT 5
CACHE OE *
HIGH BUFF ENA *
LOW BUFF ENA *

CACHE I/O SEL *
BUS I/O SEL *
BUS MEM SEL *
MWT *

CPU PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO. 625-15154-XXX	SH 5	REV SB

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

SHT 2 — LA12 — LC10* — 24A F32 — _AT ADDR BUS LA2- LA12

2K X 8 Cache RAM: 26C, 25C, 24C, 23C

CACHE CE *
CACHE OE *
CACHE WE 3 *
CACHE WE 2 *
CACHE WE 1 *
CACHE WE Ø *
SHT4

SHT4 SYS BUS BUFF ENA *

SHT4 LO BUFF ENA *
SHT4 HI BUFF ENA *
SHT 4 READ *

SHT1 CPU DATA BUS DØ - D15

ALS645-1 26D — CD31*–CD24* → D31*–D24*
ALS645-1 25D — CD23*–CD16* → D23*–D16*
ALS645-1 24D — CD15*–CD08* → D15*–D08*
ALS645-1 23D — CD7*–CD0* → D07*–D00*

RP15 330/470
RP14 330/470
RP13 330/470
RP12 330/470

ALS640 28B — CD31*–CD24* → D15–D8
ALS640 25B — CD23*–CD16* → D7–D0
ALS640 24B — CD15*–CD08* → D15–D8
ALS640 23B — CD7*–CD0* → D7–D0

DØØ*–D31* SHEET 8

CPU PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO	625-15154-XXX	SH 6	REV 88

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

SHT 7, SHT 4

SYS ADDR BUS A2 * – A23 *
SYS ADDR CLK
ST Ø *
TBWE *

AS1004

1KX4 2148 10C — Translation RAM
1KX4 2148 9C — Translation RAM
1KX4 8C — Translation RAM
1KX4 1A — Valid bit
1KX4 4A — Tag RAM
1KX4 3A — Tag
1KX4 2A — Tag

TTA9 TTA8 TTA7 TTA6 TTA5 TTA4 TTA3 TTA2 TTA1 TTAØ
MA23 MA22 MA21 MA20 MA19 MA18 MA17 MA16 MA15 MA14 MA13 MA12
VALID *
TD11 TD10 TD9 TD8 TD7 TD6 TD5 TD4 TD3 TD2 TD1 TDØ
TA9 TA8 TA7 TA6 TA5 TA4 TA3 TA2 TA1 TAØ

+5V — R4 620 — VALID *

13A ALS04 — R6 1K

MAPPED ADDR BUS MA12-MA23 — SHT 4,7
TAG BUS TDØ-TD11 — SHT 4
TWE * — SHT 4

14C F534: A23 * A22 * A21 * A20 * A19 * A18 * A17 * A16 * → MA23 MA22 MA21 MA20 MA19 MA18 MA17 MA16
12C F534: A15 * A14 * A13 * A12 * NC NC A11 * A10 * → MA15 MA14 MA13 MA12 NC NC TA9 TA8
11C F534: A9 * A8 * A7 * A6 * A5 * A4 * A3 * A2 * → TA7 TA6 TA5 TA4 TA3 TA2 TA1 TAØ

SHT 1 CPU ADDR BUS A2 – A21

5C F373: NC NC A21 A20 A19 A18 A17 A16 → NC NC TTA9 TTA8 TTA7 TTA6 TTA5 TTA4
8B F373: A15 A14 A13 A12 NC NC A11 A10 → TTA3 TTA2 TTA1 TTA0 NC NC TA9 TA8
5B F373: A9 A8 A7 A6 A5 A4 A3 A2 → TA7 TA6 TA5 TA4 TA3 TA2 TA1 TAØ

4C F244: NC NC TA9 TA8 TA7 TA6 TA5 TA4 → NC NC TA8 TA7 TA6 TA5 TA4 LA10
7B F244: TTA3 TTA2 TTA1 TTA0 NC NC TA9 TA8 → TA3 TA2 TA1 TA0 NC NC LA10 LA9
5A F244: TA7 TA6 TA5 TA4 TA3 TA2 TA1 TAØ → LA8 LA7 LA6 LA5 LA4 LA3 LA2 LA1

3C F244: MA23 MA22 MA21 MA20 MA19 MA18 MA17 MA16 → TD11 TD10 TD9 TD8 TD7 TD6 TD5 TD4
10A F244: MA15 MA14 MA13 MA12 → TD3 TD2 TD1 TDØ

ALS04 13A — 7406 15C

SHT 4 TAEN *
SHT 4 TALE

SHT 4 IOAEN
SHT 2 LAT ADDR BUS LA1 – LA10
SHT 4 TABLE BUFF ENA *
SHT 4 READ *
SHT 1 CPU DATA BUS DØ – D12

16C ALS245: MA23 MA22 MA21 MA20 → DI1 DI0 DO5 DO8
12A ALS245: MA19 MA18 MA17 MA16 MA15 MA14 MA13 MA12 → DO7 DO6 DO5 DO4 DO3 DO2 DO1 DOØ
6A ALS245: VALID * TD11 TD10 TD9 TD8 NC → NC NC NC NC DI12
11A ALS245: TD7 TD6 TD5 TD4 TD3 TD2 TD1 TDØ → DI7 DI6 DI5 DI4 DI3 DI2 DI1 DIØ

VALID * — SHEET 4

SHT 4 TAG UPDATE ENABLE *
SHT 4 TAG BUFF ENABLE *

CPU PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH.	REV.
025-15154-XXX	7	BB

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

SHT 3 RESET *

330/470 RP7

E3 M S

R48 1K

"BUSARB"

11D 20R4A

BRQ7*
BRQ6*
3RQ5*
BRQ4*
BRQ3*
BRQ2*
BRQ1*
BRQØ*

SHT 8 BRQØ*-BRQ7*

RP5 1K

Bus Clock Dwt.

SHT 8 BCLK*

AS1004 5D

R61 Ø

R62 100

C67 47pf

R33 1K

R47 390

Bus Clock Osc.

1C 19.6608

10D F74

AS1004 5D

R34 1K

SHT 4 R34

SHT 2 LPLOCK *

SHT 4 BUS REQ*

E5

F138 10D

SHT 8 BPNØ*-BPN7*

CBRQ* SHT 8

AEN* SHT 1,4

REL REQ* SHT 4

LOCK*
HBEN*
HWEN*
BUSY*
SHT 8

F244 19D

AS533 16D

AS533 15D

NC
MA23
MA22
MA21
MA20
MA19
MA18
MA17
MA16
MA15
MA14
MA13
MA12

A23* A22* A21* A20* A19* A18* A17* A16* A15* A14* A13* A12*

330/470 RP9 RP8

A0*-A23* SHT 8
SYS ADDR BUS A2*-A23* SHT 6

A23* A22* A21* A20* A19* A18* A17* A16* A15* A14* A13* A12* A11* A10* A9* A8* A7* A6* A5* A4* A3* A2* A1* AØØ*

330/470 RP7 RP8

SHT 1 MALE
SHT 6 MAPPED ADDR BUS MA12-MA23

SHT 2 LAT SYS MEM SEL *
LAT BUS I/O SEL *
SHT 2 LAT BHE*

SHT 2 LAT ADDR BUS LAØ-LA15

F32 7D

F08 13C

ALS04 20D

SHT 3 CACHE ENA
SHT 4 READ*

LAØ LA1 LA2 LA3 LA4 LA5 LA6 LA7 LA8 LA9 LA10 LA11 LA12 LA13 LA14 LA15

13D ALS240-1

14D ALS240-1

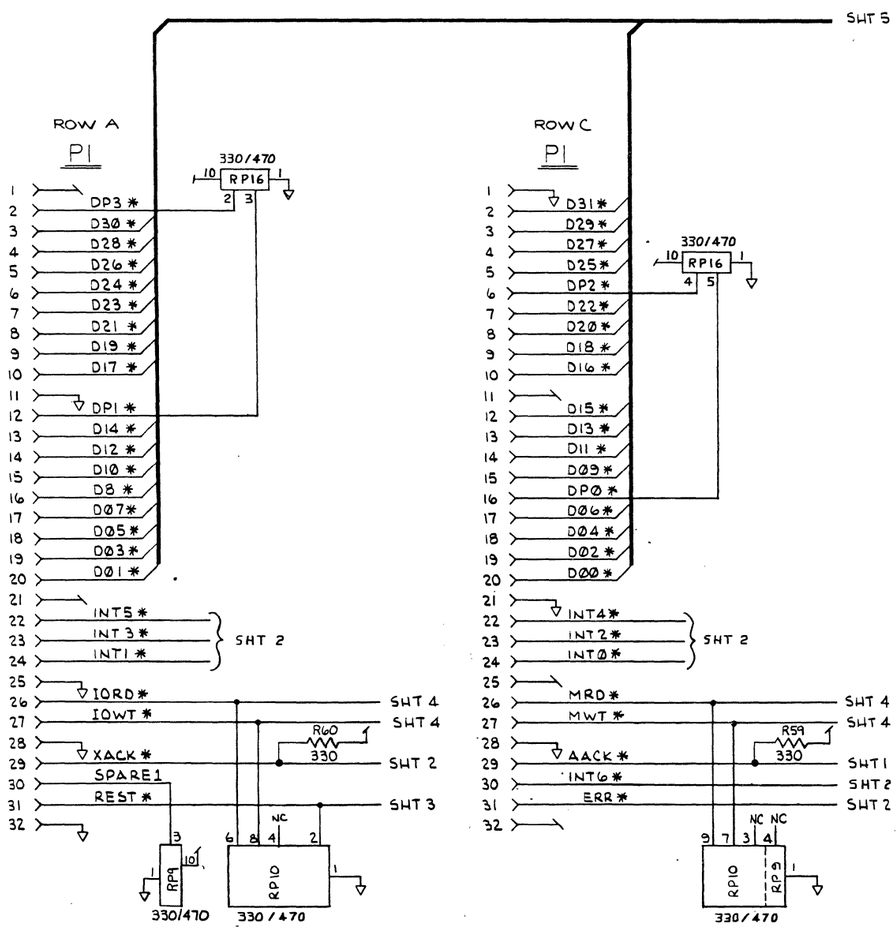
AØØ* AØ1* AØ2* AØ3* AØ4* AØ5* AØ6* AØ7* A08* A09* A10* A11* A12* A13* A14* A15*

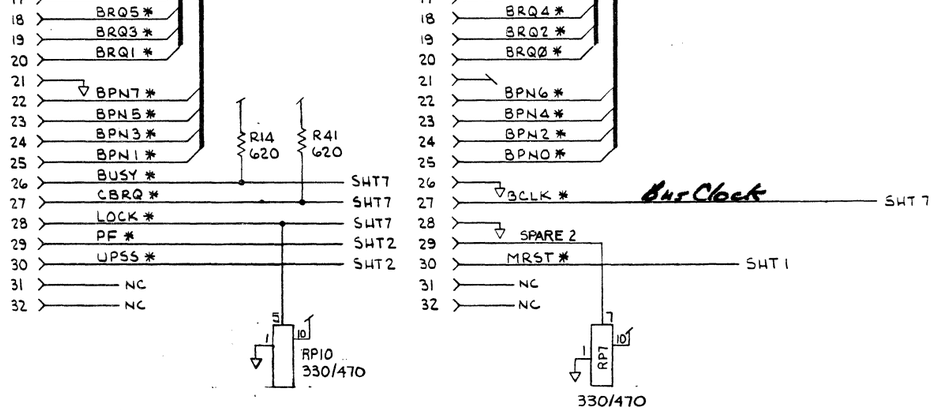
CPU PCB SCHEMATIC DIAGRAM

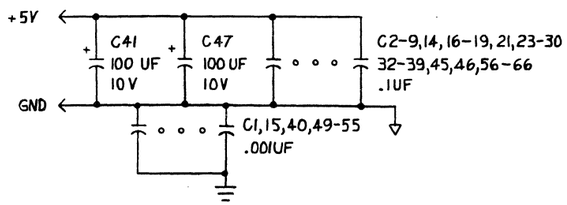
ALTOS COMPUTER SYSTEMS

DWG. NO.	SH.	REV.
625-15154-XXX	3	8D

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		







CPU PCB SCHEMATIC DIAGRAM

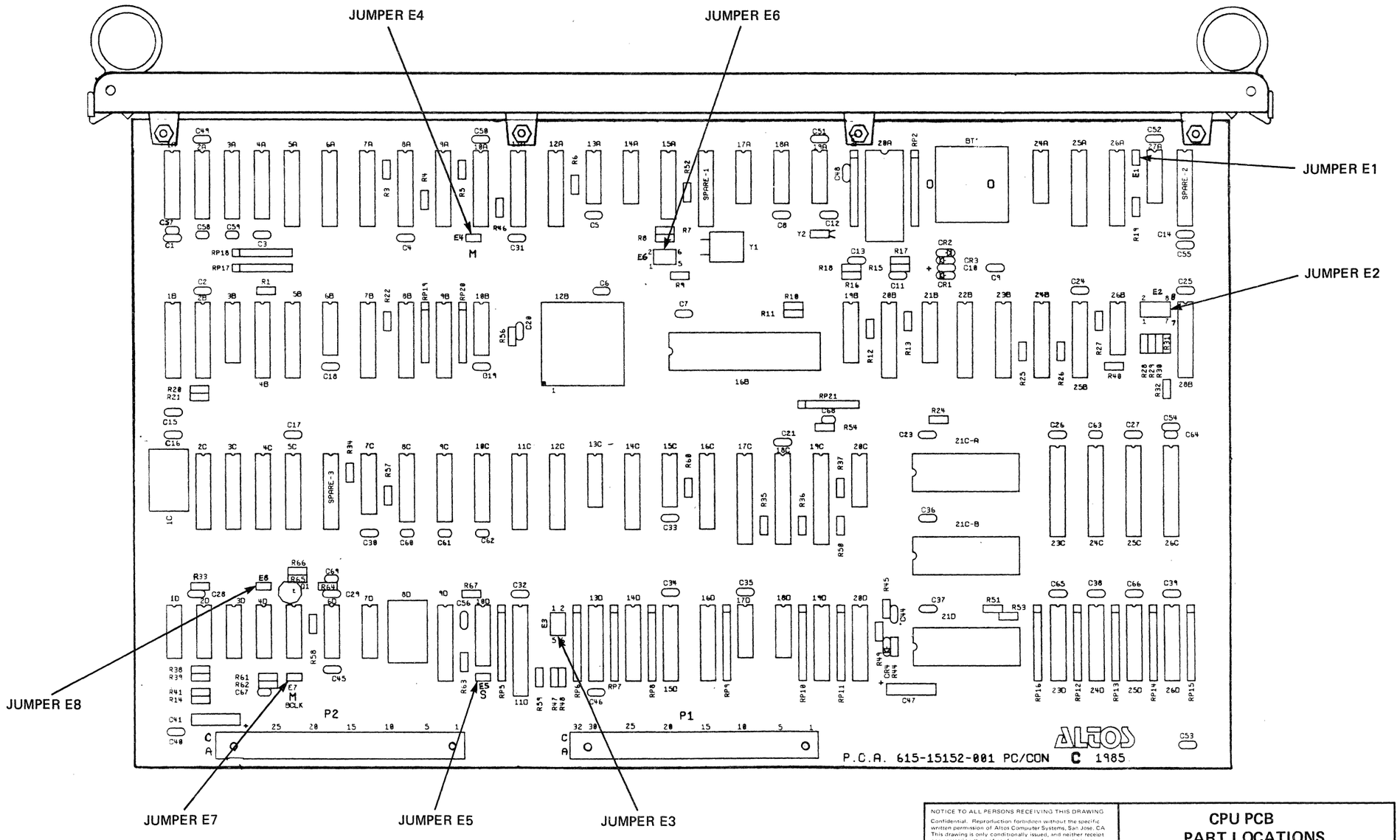
ALTOS COMPUTER SYSTEMS

CPU PCB
PART LOCATIONS
615-15152-XXX

DWG NO	SH	REV
615-15152-XXX	1	12A

REVISIONS

ZONE	REV	DESCRIPTION		DATE	APPROVED
	XIA	PROTOTYPE			
	12A	PROTOTYPE			
	X3A	PROTOTYPE			
	3A	PRE-PRODUCTION EO# 2900		3-1-85	
	4A	EO# 2932		4-19-85	
	5A	REVISED PER EO # 3125-H		5-14-85	
	6A	REVISED PER EO # 3075-H	SR	5.29.85	
	7A	REVISED PER EO # 3110-H	SR	5-29-85	
	8A	REVISED PER EO # 3166-H	SR	5.29.85	
	9A	REVISED PER EO # 3134-H	SR	5.29.85	
	10A	REVISED PER EO# 3228-H		7-10-85	
	11A	EO # 3340-H		7-25-85	
	12A	EO # 3420		7-25-85	



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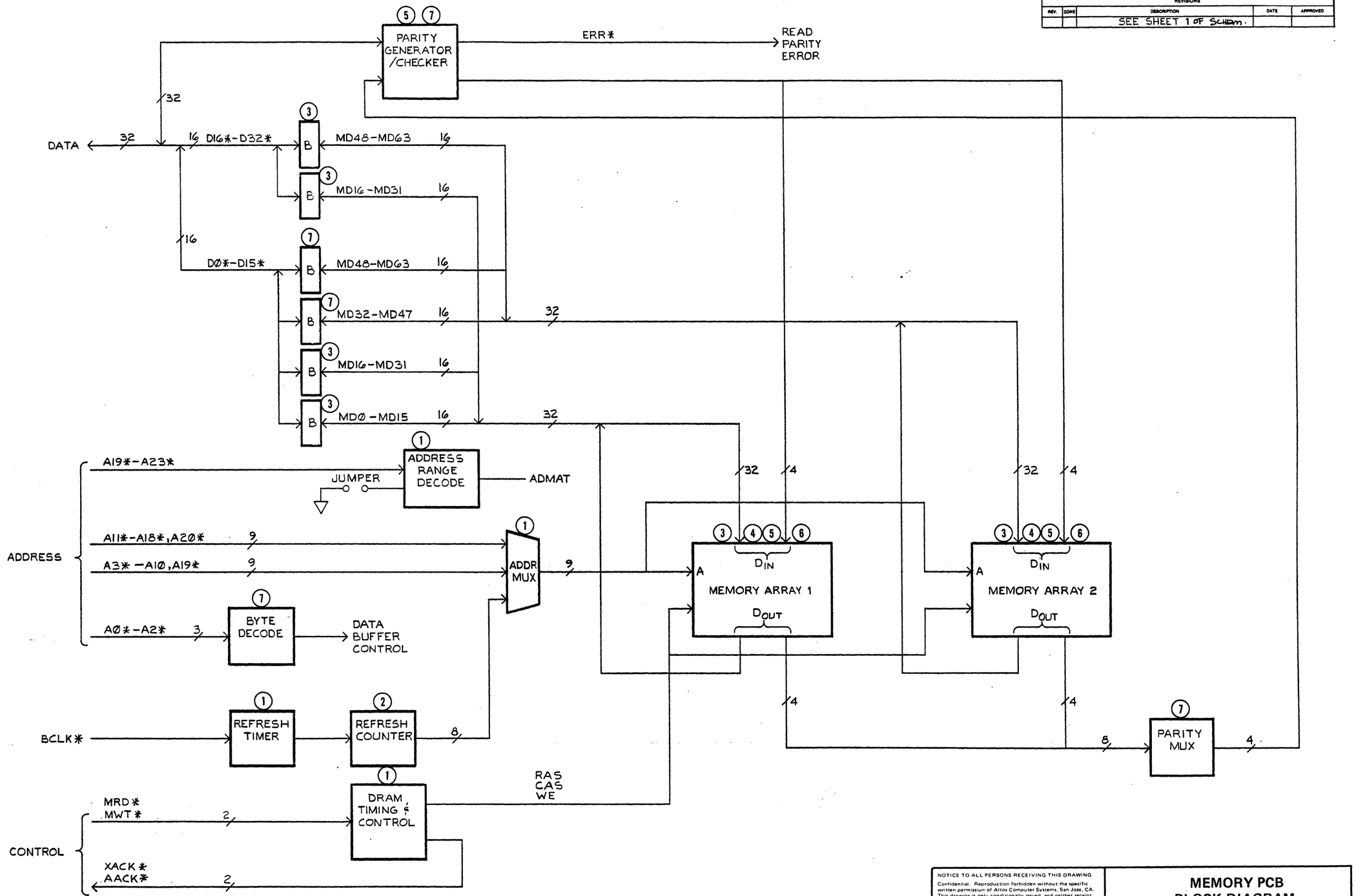
CPU PCB PART LOCATIONS

ALTOS COMPUTER SYSTEMS

MEMORY PCB
BLOCK DIAGRAM
615-16509-XXX

DWG. NO.	SH	REV.
625-16511-XXX	B.D.	A

REVISIONS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1 OF SCHEM.		



MEMORY PCB BLOCK DIAGRAM

ALTOS COMPUTER SYSTEMS

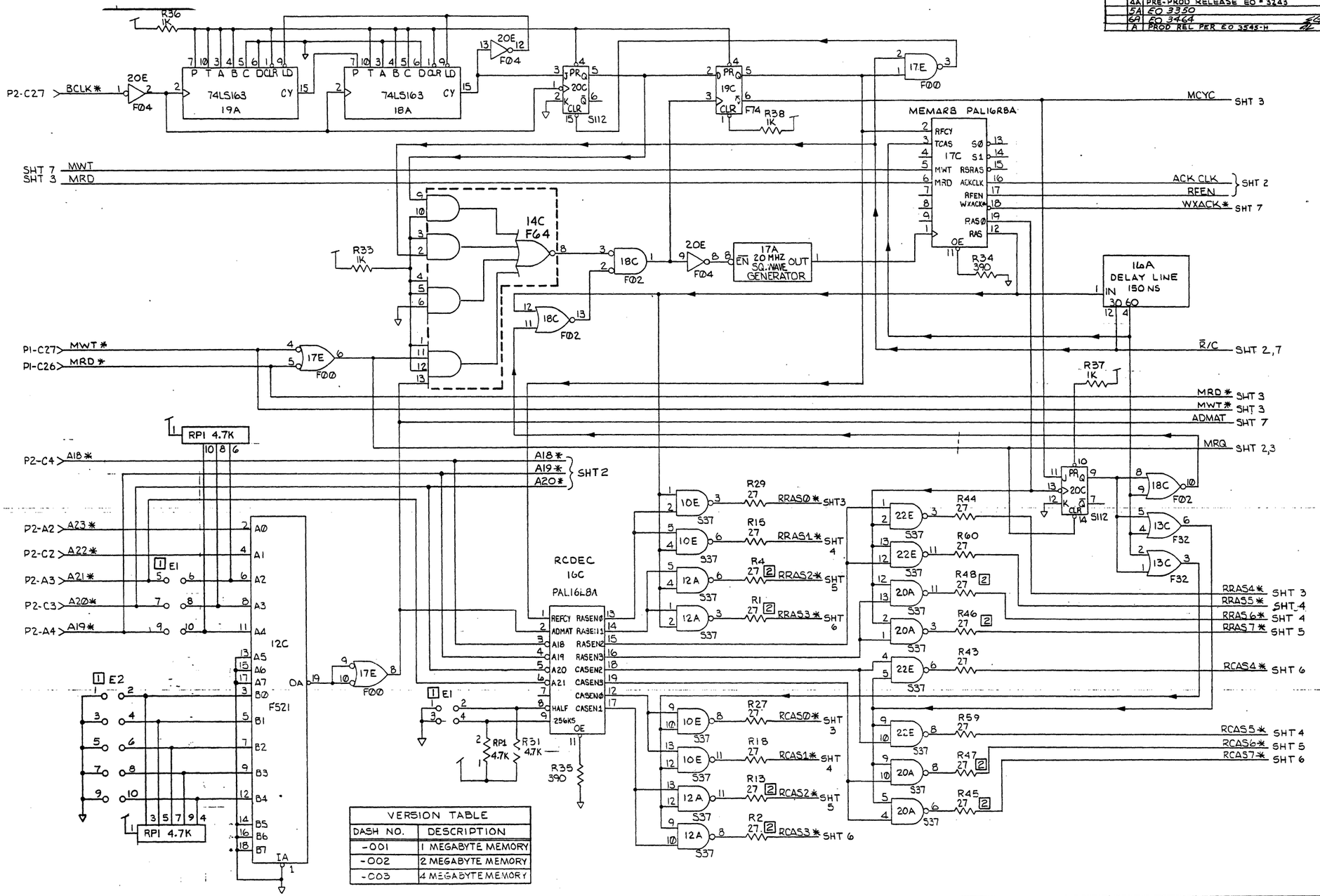
MEMORY PCB SCHEMATIC DIAGRAMS 615-16509-XXX

11

DWG. NO.	SH	REV
625-16511-XXX	1	A

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	X2A	PROTOTYPE		
	X3A	PROTOTYPE	5-31-85	
	X4A	PROTOTYPE	6-17-85	
	4A	PRE-PROD RELEASE EO # 3243	6-28-85	
	5A	EO 3350	8-5-85	
	6A	EO 3464	10-3-85	
	A	PROD REL PER EO 3545-H	11-26-86	



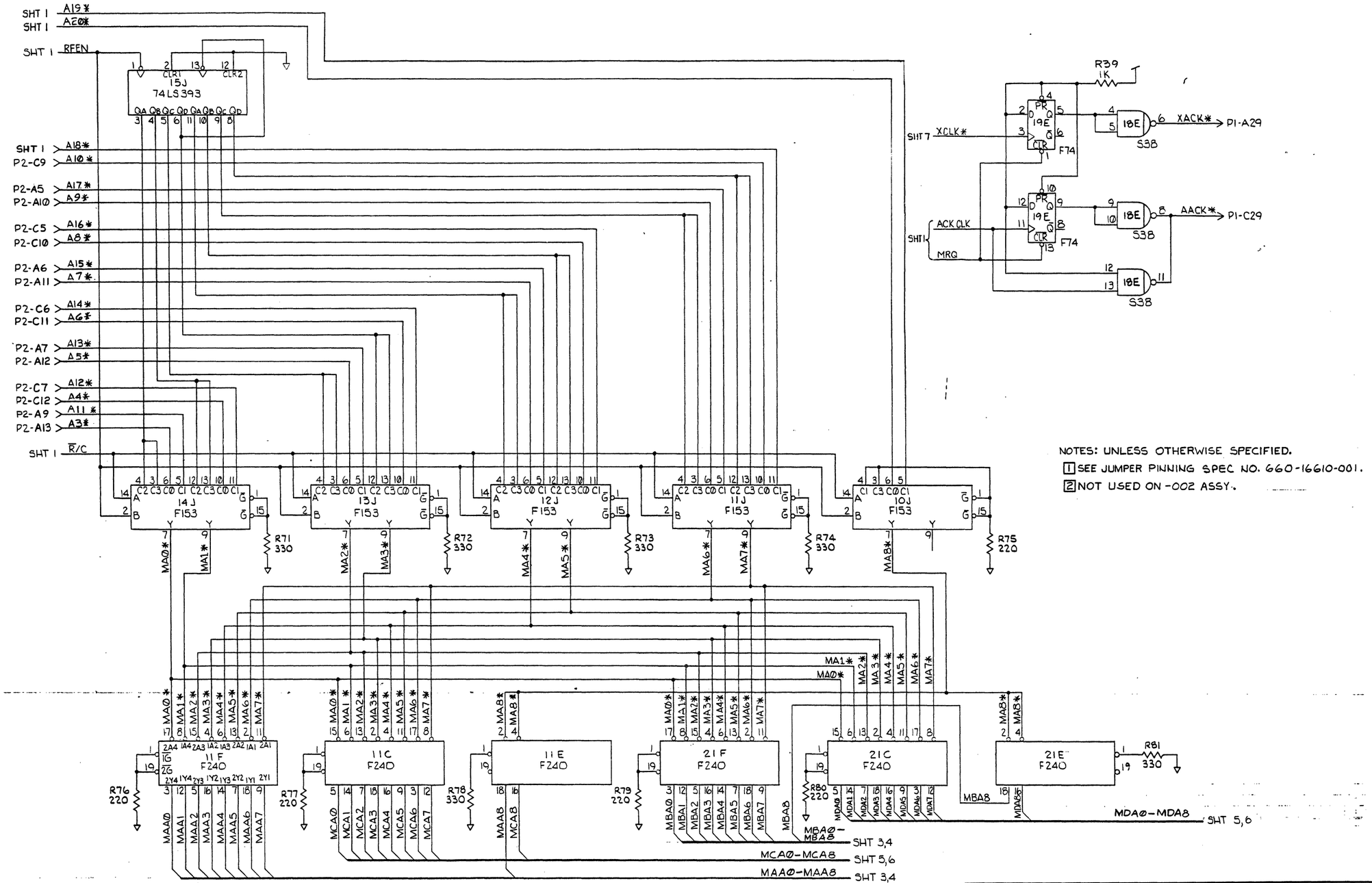
VERSION TABLE	
DASH NO.	DESCRIPTION
-001	1 MEGABYTE MEMORY
-002	2 MEGABYTE MEMORY
-003	4 MEGABYTE MEMORY

MEMORY PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH.	REV
625-16511-XXX	2	A

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



NOTES: UNLESS OTHERWISE SPECIFIED.

1. SEE JUMPER PINNING SPEC NO. 660-16610-001.
2. NOT USED ON -002 ASSY.

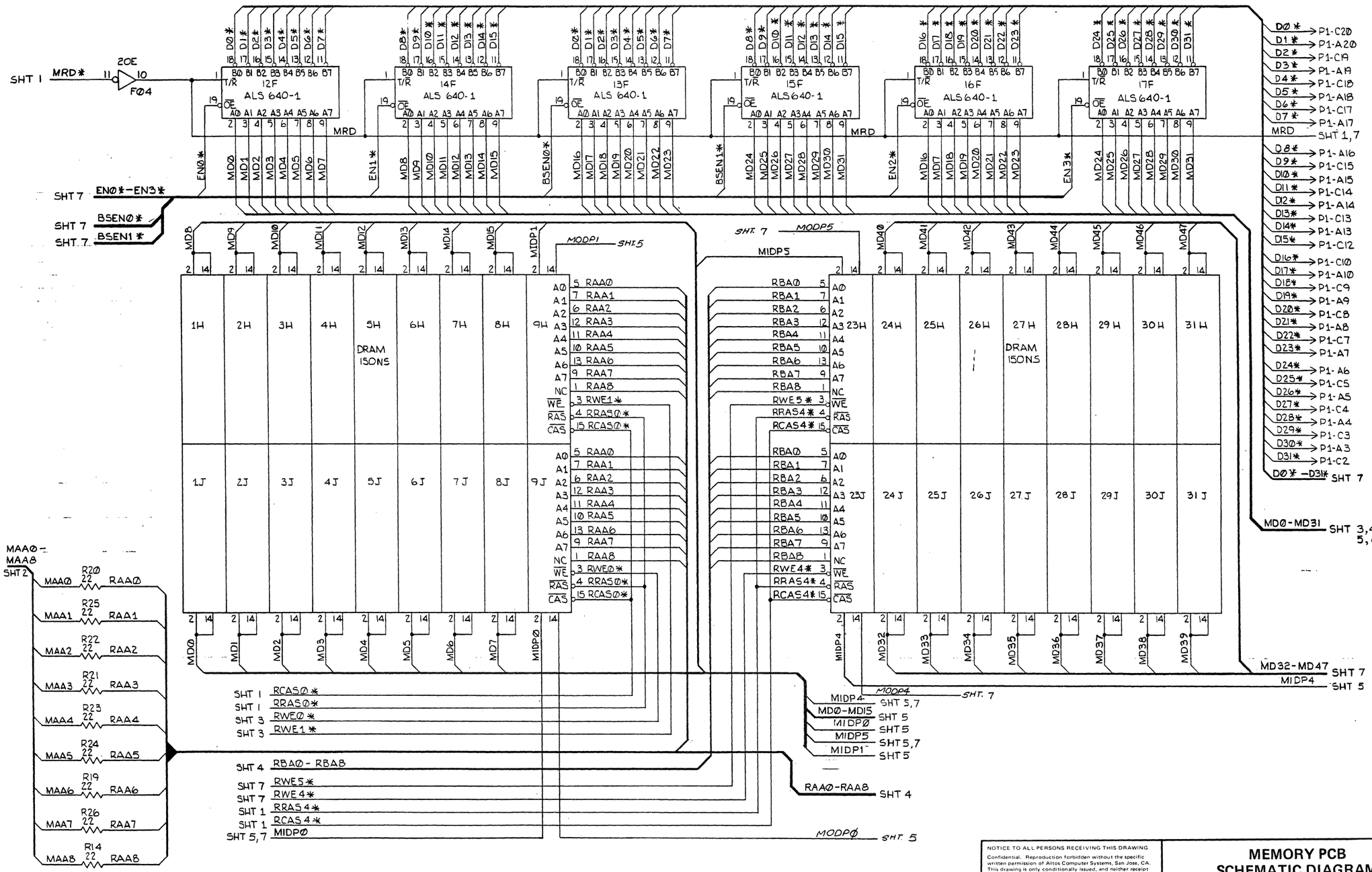
MEMORY PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV.
625-16511-XXX	3	A

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



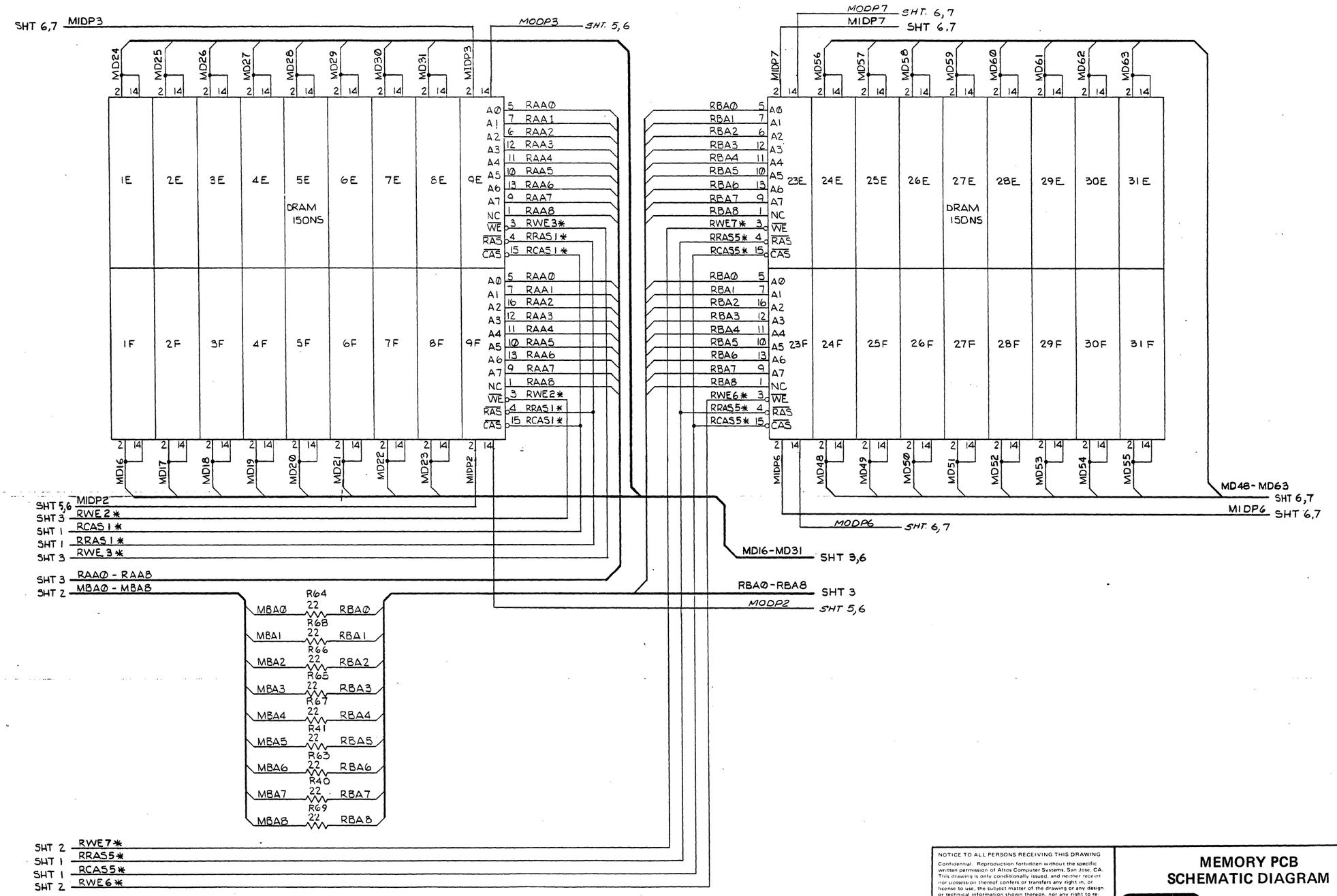
MEMORY PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO. 625-16511-XXX	SH. 4	REV. A

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



MEMORY PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH.	REV.
625-16511-XXX	5	A

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

SHT 3 RWE5*
SHT 3 RWE4*
SHT 1 RRAS6*
SHT 1 RCAS6*
SHT 2 MCA0 - MCA8

R6 [2] MCA0 22 RCA0
R9 [2] MCA1 22 RCA1
R8 [2] MCA2 22 RCA2
R3 [2] MCA3 22 RCA3
R7 [2] MCA4 22 RCA4
R10 [2] MCA5 22 RCA5
R5 [2] MCA6 22 RCA6
R11 [2] MCA7 22 RCA7
R12 [2] MCA8 22 RCA8

SHT 3 RWE1*
SHT 3 RWE0*
SHT 1 RRAS2*
SHT 1 RCAS2*

SHT 2 MDA0 - MDA8

R51 [2] MDA0 22 RDA0
R54 [2] MDA1 22 RDA1
R53 [2] MDA2 22 RDA2
R50 [2] MDA3 22 RDA3
R52 [2] MDA4 22 RDA4
R55 [2] MDA5 22 RDA5
R49 [2] MDA6 22 RDA6
R56 [2] MDA7 22 RDA7
R57 [2] MDA8 22 RDA8

MD8 MD9 MD10 MD11 MD12 MD13 MD14 MD15 MIDP1
MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7 MIDP0

RCA0 RCA1 RCA2 RCA3 RCA4 RCA5 RCA6 RCA7 RCA8
A0 A1 A2 A3 A4 A5 A6 A7 A8 NC
WE RAS CAS

1C 2C 3C 4C 5C 6C 7C 8C 9C
1D 2D 3D 4D 5D 6D 7D 8D 9D
DRAM 150NS

MIDP5 MD40 MD41 MD42 MD43 MD44 MD45 MD46 MD47
MIDP4 MD32 MD33 MD34 MD35 MD36 MD37 MD38 MD39

RDA0 RDA1 RDA2 RDA3 RDA4 RDA5 RDA6 RDA7 RDA8
RWE5* RRAS6* RCAS6*
RWE4* RRAS6* RCAS6*

23C 24C 25C 26C 27C 28C 29C 30C 31C
23D 24D 25D 26D 27D 28D 29D 30D 31D
DRAM 150NS

MODP1 SHT. 3
MODP5 SHT. 7
MODP0 SHT. 3

MIDP5 SHT 3,7
RCA0 - RCA8 SHT 6
MIDP1 SHT 3
MD32-MD47 SHT 3,7
MIDP4 SHT 3,7
MIDP0 SHT 3,
MIDP2 SHT 4
MIDP1 SHT 3
MODP4 SHT 7

MIDP0

SHT 3,7 MD0 - MD31

MODP3 SHT. 3
MODP1 SHT. 3
MODP2 SHT. 4,6
MODP3 SHT. 4,6

MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7 MIDP0
MD8 MD9 MD10 MD11 MD12 MD13 MD14 MD15 MIDP1
MD16 MD17 MD18 MD19 MD20 MD21 MD22 MD23 MIDP2
MD24 MD25 MD26 MD27 MD28 MD29 MD30 MD31

R82 2.2K
R83 2.2K
R84 2.2K
R85 2.2K

12E AS280 EVEN
14E AS280 EVEN
13E AS280 EVEN
15E AS280 EVEN

MIDP2
MIDP3
MIDP3 SHT 4

RDA0-RDA8 SHT 6

11E F240
16E F20
MIDP1
MIDP0
PERR
ERR* → PI-C31

SHT 7 ENLERR*

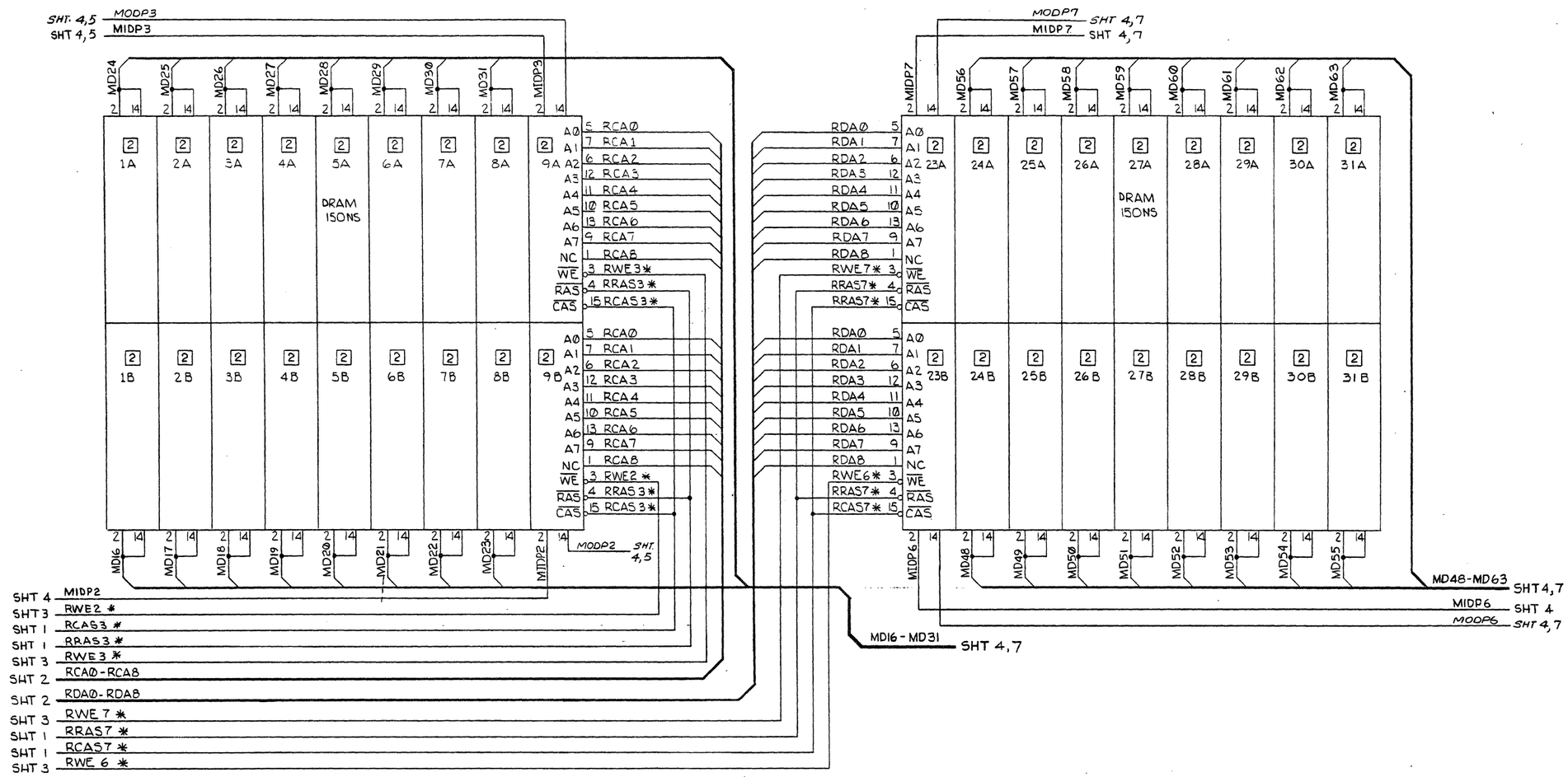
MEMORY PCB SCHEMATIC DIAGRAM

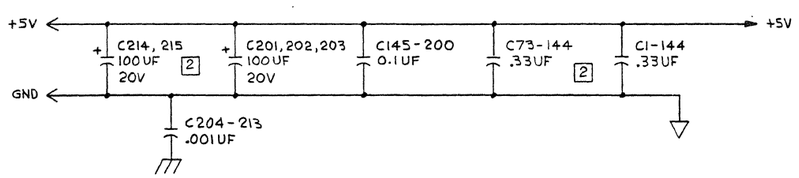
ALTOS COMPUTER SYSTEMS

DWG. NO.	SH.	REV.
625-16511-XXX	6	A

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		





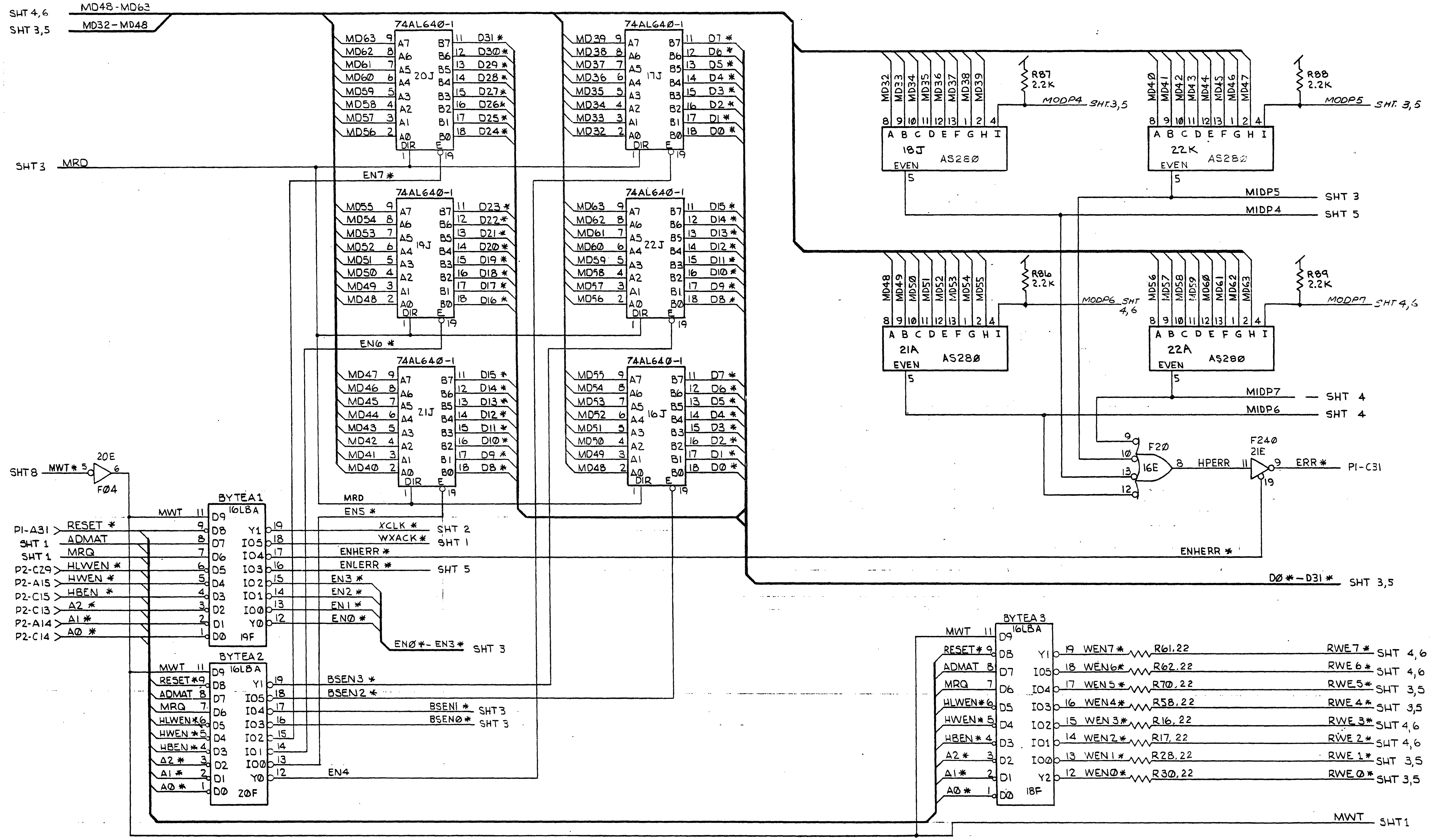
MEMORY PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV.
625-16511-XXX	7	A

REVISIONS

REV.	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



MEMORY PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO. 625-16511-XXX	SH. 8	REV. A

REVISIONS

REV.	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

ROW A
P1

	1	
	2	
SHT 7	3	D30 *
SHT 7	4	D28 *
SHT 7	5	D26 *
SHT 7	6	D24 *
SHT 7	7	D23 *
SHT 7	8	D21 *
SHT 7	9	D19 *
SHT 7	10	D17 *
	11	
	12	
SHT 7	13	D14 *
SHT 7	14	D12 *
SHT 7	15	D10 *
SHT 7	16	D8 *
SHT 7	17	D7 *
SHT 7	18	D5 *
SHT 7	19	D3 *
SHT 7	20	D1 *
	21	
	22	
	23	
	24	
	25	
	26	
	27	
	28	
XACK *	29	
	30	
RESET *	31	
	32	

ROW C
P1

	1	
SHT 7	2	D31 *
SHT 7	3	D29 *
SHT 7	4	D27 *
SHT 7	5	D25 *
	6	
SHT 7	7	D22 *
SHT 7	8	D20 *
SHT 7	9	D18 *
SHT 7	10	D16 *
	11	
SHT 7	12	D15 *
SHT 7	13	D13 *
SHT 7	14	D11 *
SHT 7	15	D9 *
	16	
SHT 7	17	D6 *
SHT 7	18	D4 *
SHT 7	19	D2 *
SHT 7	20	D0 *
	21	
	22	
	23	
	24	
	25	
MRD *	26	
MWT *	27	
	28	
AACK *	29	
	30	
ERR *	31	
	32	

ROW A
P2

	1	
	2	A23 *
SHT 2	3	A21 *
SHT 2	4	A19 *
SHT 2	5	A17 *
SHT 2	6	A15 *
SHT 2	7	A13 *
	8	
SHT 2	9	A11 *
SHT 2	10	A9 *
SHT 2	11	A7 *
SHT 2	12	A5 *
SHT 2	13	A3 *
SHT 2	14	A1 *
SHT 2	15	HWEN *
	16	
	17	
	18	
	19	
	20	
	21	
	22	
	23	
	24	
	25	
	26	
	27	
	28	
	29	
	30	
	31	
	32	

ROW C
P2

	1	
SHT 2	2	A22 *
SHT 2	3	A20 *
SHT 2	4	A18 *
SHT 2	5	A16 *
SHT 2	6	A14 *
SHT 2	7	A12 *
	8	
SHT 2	9	A10 *
SHT 2	10	A8 *
SHT 2	11	A6 *
SHT 2	12	A4 *
SHT 2	13	A2 *
SHT 2	14	A0 *
SHT 2	15	HBEN *
	16	
	17	
	18	
	19	
	20	
	21	
	22	
	23	
	24	
	25	
	26	
BCLK *	27	
	28	
HLWEN *	29	
	30	
	31	
	32	

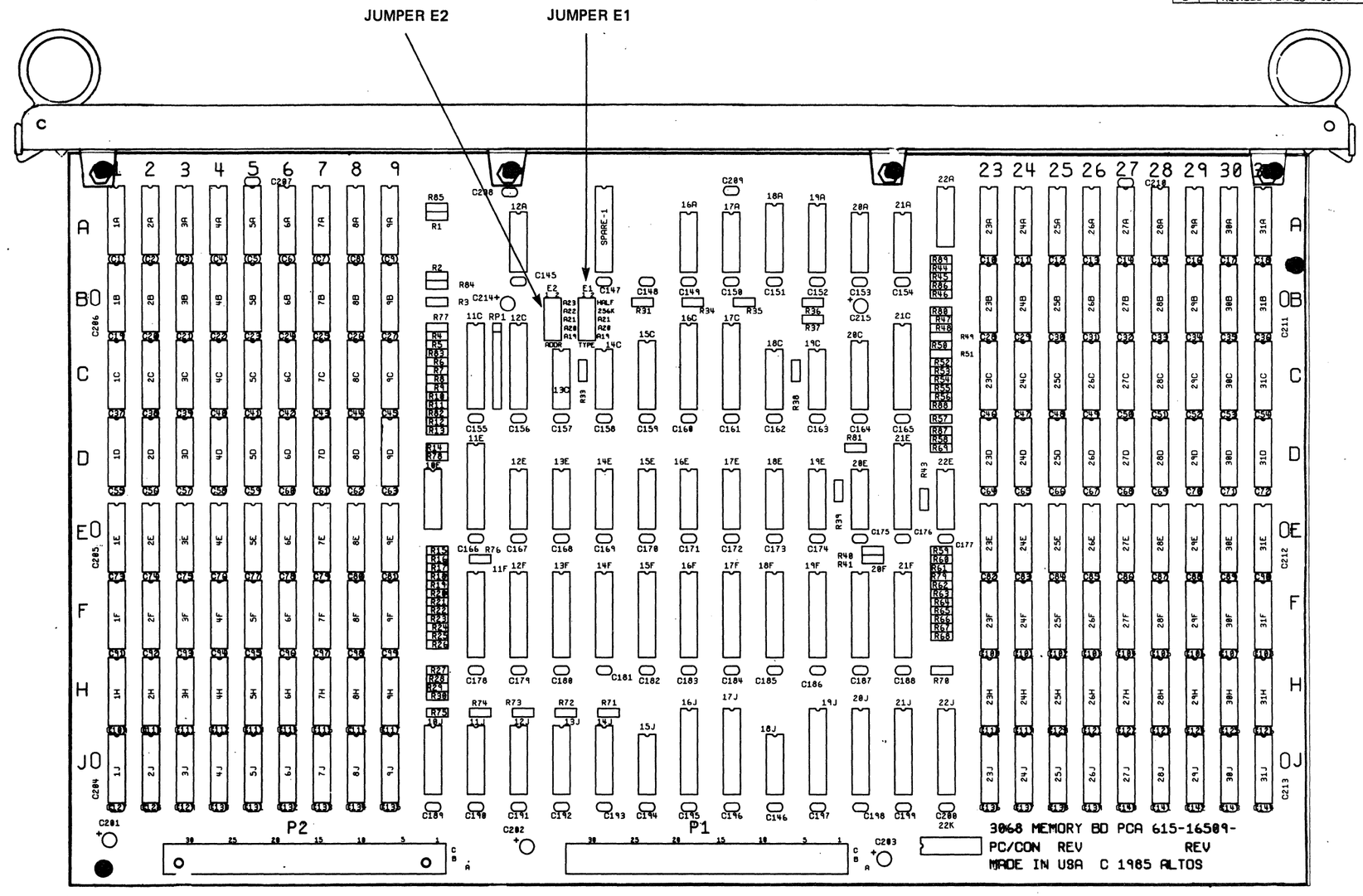
MEMORY PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

MEMORY PCB
PART LOCATIONS
615-16509-XXX

DWG. NO.	SH	REV
615-16509-XXX	1	D

REVISIONS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
X1A		PROTOTYPE	1-28-85	
X2A		PROTOTYPE		
X3A		PROTOTYPE	5-31-85	
X4A		PROTOTYPE	6-17-85	
4A		PRE-PROD RELEASE EO # 3243	6-25-85	
5A		EO 3350	8-5-85	
6A		EO # 3464	10-3-85	
7A		EO # 4060 PART LIST UPDATE.	1-20-86	
8A		REVISED PER EO 4058-H	24JAN86	
A		PROD REL PER EO 3545-H	1-28-86	
B		EO # 4040-H	20 FEB 86	
C		REVISED PER EO 4215-H	18MAR86	
D		REVISED PER EO 4301-H	24JUN86	



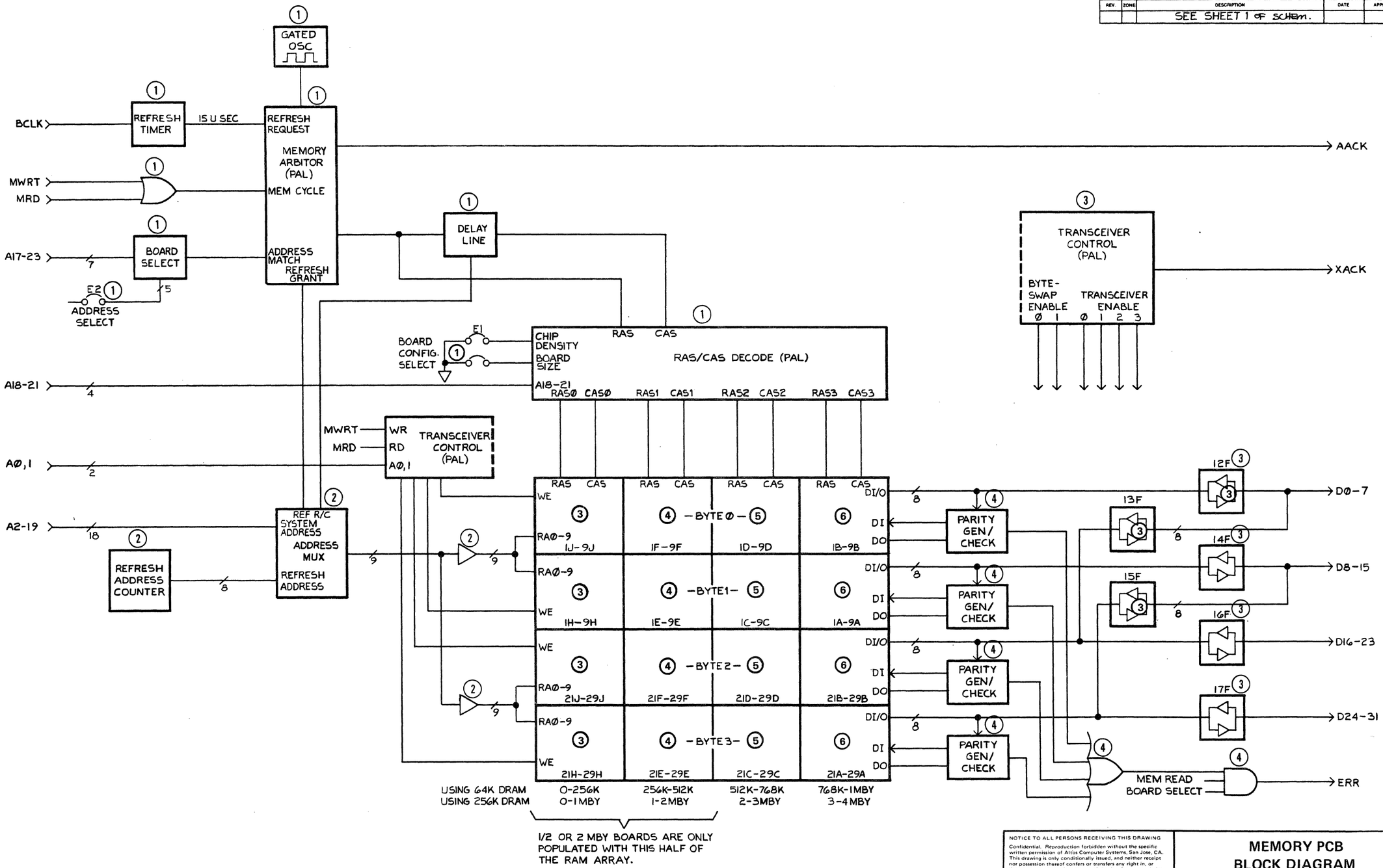
MEMORY PCB PART LOCATIONS

ALTOS COMPUTER SYSTEMS

MEMORY PCB BLOCK DIAGRAM 615-15146-XXX

DWG. NO.	SH.	REV.
625-15148-XXX	7	5A

REVISIONS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1 OF SCHEM.		



MEMORY PCB BLOCK DIAGRAM

ALTOS COMPUTER SYSTEMS

MEMORY PCB SCHEMATIC DIAGRAMS 615-15146-XXX

11

DWG. NO.	SH	REV.
625-15148-XXX	1	5A

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	1AA	PROTOTYPE 2.5@25MD		
	15A	EO 3275-H	22 MAR 85	CMR

236 1K

19E FØ4

P2-C27 > 3CLK* 19E FØ4

74LS163 20E

74LS163 19C

19E FØ4

5112

17C F74

R34 1K

16E FØØ

MCYC SHT 3

PAL16R8A

RFCY TCAS 15C MWT MRD

SØ S1 RSRAS ACKCLK RFEN WXACK RASØ RAS OE

ACK CLK RFEN SHT 2

WXACK* SHT 3

SHT 3 MWT

SHT 3 MRD

R31 1K

F64

13C 16C FØ2

19E FØ4

16A 20 MHZ OSC OUT

R33 390Ω

17E DELAY LINE IN 30 60 150NS

P1-C27 > MWT*

P1-C26 > MRD*

16E FØØ

R35 1K

R/C SHT 2

MWT* SHT 3

MRD* SHT 3

ADMAT SHT 3,5

MRQ SHT 2,3

SHT 2

P2-C4 > A18*

P2-A2 > A23*

P2-C2 > A22*

P2-A3 > A21*

P2-C3 > A20*

P2-A4 > A19*

SHT 2

2 E1 T1

RP1 4.7K

2 E2

A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7 11C F521

OA IA

16E FØØ

E1

RP1 4.7K R30 4.7K

R32 390Ω

14C PAL16L8A

REFCY ADMAT A18 A19 A20 A21 64KS

RASEN0 RASEN1 RASEN2 RASEN3 CASEN2 CASEN3 CASEN0 CASEN1 OE

10J 19F S37

R29 27Ω RRAS0*

R69 27Ω RRAS1*

R60 27Ω RRAS2*

R41 27Ω RRAS3*

SHT 3

SHT 4

R27 27Ω RCAS0*

R39 27Ω RCAS1*

R17 27Ω RCAS2*

R58 27Ω RCAS3*

SHT 3

SHT 4

14A 15A S37

R2 27Ω 1

R43 27Ω 1

R5 27Ω 1

R46 27Ω 1

R3 27Ω 1

R44 27Ω 1

R4 27Ω 1

R45 27Ω 1

16C FØ2

12C F32

RRAS4* RRAS5* SHT 5

RRAS6* RRAS7* SHT 6

RCAS4* SHT 5

RCAS5* SHT 5

RCAS6* SHT 6

RCAS7* SHT 6

VERSION TABLE	
DASH NO.	DESCRIPTION
-001	1 MEGABYTE MEMORY
-002	2 MEGABYTE MEMORY
-003	4 MEGABYTE MEMORY

MEMORY PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO. 625-15148-XXX	SH. 2	REV. 5A

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

SHT 1 A18 *
SHT 1 A19 *
SHT 1 RFEN

17J 74LS393 (CLR1, CLR2; QA QB QC QD QA QB QC QD)

P2-A5 > A17 *
P2-A10 > A09 *
P2-C5 > A16 *
P2-C10 > A08 *
P2-A6 > A15 *
P2-A11 > A07 *
P2-C6 > A14 *
P2-C11 > A06 *
P2-A7 > A13 *
P2-A12 > A05 *
P2-C7 > A12 *
P2-C12 > A04 *
P2-A9 > A11 *
P2-A13 > A03 *
P2-C9 > A10 *
P2-C13 > A02 *
SHT 1 R/C

16J F153 (MA0*, MA1*) · 15J F153 (MA2*, MA3*) · 14J F153 (MA4*, MA5*) · 13J F153 (MA6*, MA7*) · 12J F153 (MA8*)

0F F240 (MAA0–MAA7) · 10C F240 [1] (MCA0–MCA7) · 10E F240 (MAA8, MCA8) · 20F F240 (MBA0–MBA7) · 20C F240 [1] (MBA8) · 20J F240

MBA0–MBA8 SHT 4
MCA0–MCA8 SHT 5
MAA0–MAA8 SHT 3
MDA0–MDA8 SHT 5

R40 1K

SHT 3 XCLK → F74 (18E) → 18F (S38) → XACK* → P1-A29

ACK CLK, SHT 1, MRQ → F74 (18E) → 18F (S38) → AACK* → P1-C29

18F (S38)

NOTES: UNLESS OTHERWISE SPECIFIED
1. NOT USED ON -002 VERSION
2. JUMPER PINNING SEE MAINTENANCE MANUAL, APPENDIX A

MEMORY PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV.
625-1519-XXX	3	5A

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

P2-C14 A00* 9 → 11J FØ4 → 8 A00
P2-A14 A01* 5 → 11J FØ4 → 6 A01
P2-C15 HBEN* 3 → 11J FØ4 → 4 HBEN
P2-A15 HWEN* 1 → 11J FØ4 → 2 HWEN
SHT 1 MWT* 11 → 11J FØ4 → 10 MWT
SHT 1 MWT
SHT 1 MRD* 13 → 11J FØ4 → 12

12F, 13F, 14F, 15F, 16F, 17F: ALS 640-1 (T/R, OE, A0 A1 A2 A3 A4 A5 A6 A7 / B0 B1 B2 B3 B4 B5 B6 B7)

12F	D00*	D01*	D02*	D03*	D04*	D05*	D06*	D07*
13F	D08*	D09*	D10*	D11*	D12*	D13*	D14*	D15*
14F	D00*	D01*	D02*	D03*	D04*	D05*	D06*	D07*
15F	D08*	D09*	D10*	D11*	D12*	D13*	D14*	D15*
16F	D16*	D17*	D18*	D19*	D20*	D21*	D22*	D23*
17F	D24*	D25*	D26*	D27*	D28*	D29*	D30*	D31*

EN0* MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7
EN1* MD8 MD9 MD10 MD11 MD12 MD13 MD14 MD15
BSEN0* MD16 MD17 MD18 MD19 MD20 MD21 MD22 MD23
BSEN1* MD24 MD25 MD26 MD27 MD28 MD29 MD30 MD31
EN2* MD16 MD17 MD18 MD19 MD20 MD21 MD22 MD23
EN12* MD24 MD25 MD26 MD27 MD28 MD29 MD30 MD31

D00* → P1-C20
D01* → P1-A20
D02* → P1-C19
D03* → P1-A19
D04* → P1-C18
D05* → P1-A18
D06* → P1-C17
D07* → P1-A17
MRD — SHT 1,5
D08* → P1-A16
D09* → P1-C15
D10* → P1-A15
D11* → P1-C14
D12* → P1-A14
D13* → P1-C13
D14* → P1-A13
D15* → P1-C12
D16* → P1-C10
D17* → P1-A10
D18* → P1-C9
D19* → P1-A9
D20* → P1-C8
D21* → P1-A8
D22* → P1-C7
D23* → P1-A7
D24* → P1-A6
D25* → P1-C5
D26* → P1-A5
D27* → P1-C4
D28* → P1-A4
D29* → P1-C3
D30* → P1-A3
D31* → P1-C2
XCLK — SHT 2
MODP0-MODP3
MIDP0-MIDP3
MD0-MD31
SHT 4,5,6

11F PAL20L10

A00	1	14	EN0*
A01	2	15	EN1*
HBEN	3	16	EN2*
HWEN	4	17	XCLK
MWT	5	18	BSEN0*
SHT 1 MRQ	6	19	BSEN1*
SHT 1 ADMAT	7	20	WEN0*
SHT 1 REST*	8	21	WEN1*
SHT 1 MCYC	9	22	WEN2*
SHT 1 R/C	10	23	WEN3*
SHT 1 WXACK*	11		
	13		OE

R42 390Ω

MD0 MD9 MD10 MD11 MD12 MD13 MD14 MD15 MIDP1 MODP1

1H	2H	3H	4H	5H RAM 150ns	6H	7H	8H	9H	RAA0 RAA1 RAA2 RAA3 RAA4 RAA5 RAA6 RAA7 RAA8
1J	2J	3J	4J	5J RAM 150ns	6J	7H	8J	9J	RAA0 RAA1 RAA2 RAA3 RAA4 RAA5 RAA6 RAA7 RAA8

RAA0 RAA1 RAA2 RAA3 RAA4 RAA5 RAA6 RAA7 RAA8 — WE — RWE1* — RRAS0* — RCAS0*

MIDP3 MODP3 MD24 MD25 MD26 MD27 MD28 MD29 MD30 MD31

21H	22H	23H	24H	25H RAM 150ns	26H	27H	28H	29H	RBA0 RBA1 RBA2 RBA3 RBA4 RBA5 RBA6 RBA7 RBA8
21J	22J	23J	24J	25J RAM 150ns	26J	27J	28J	29J	RBA0 RBA1 RBA2 RBA3 RBA4 RBA5 RBA6 RBA7 RBA8

RBA0 RBA1 RBA2 RBA3 RBA4 RBA5 RBA6 RBA7 RBA8 — WE — RWE3* — RRAS1* — RCAS1*

MIDP2 MODP2 MD16 MD17 MD18 MD19 MD20 MD21 MD22 MD23

MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7 MIDP0 MODP0

R20 22Ω MAA0 — RAA0
R25 22Ω MAA1 — RAA1
R22 22Ω MAA2 — RAA2
R21 22Ω MAA3 — RAA3
R23 22Ω MAA4 — RAA4
R24 22Ω MAA5 — RAA5
R19 22Ω MAA6 — RAA6
R26 22Ω MAA7 — RAA7
R16 22Ω MAA8 — RAA8

R18 22 — RWE0*
R28 22 — RWE1*
R56 22 — RWE2*
R59 22 — RWE3*
RWE0* RWE1* RWE2* RWE3* — SHT 5,6

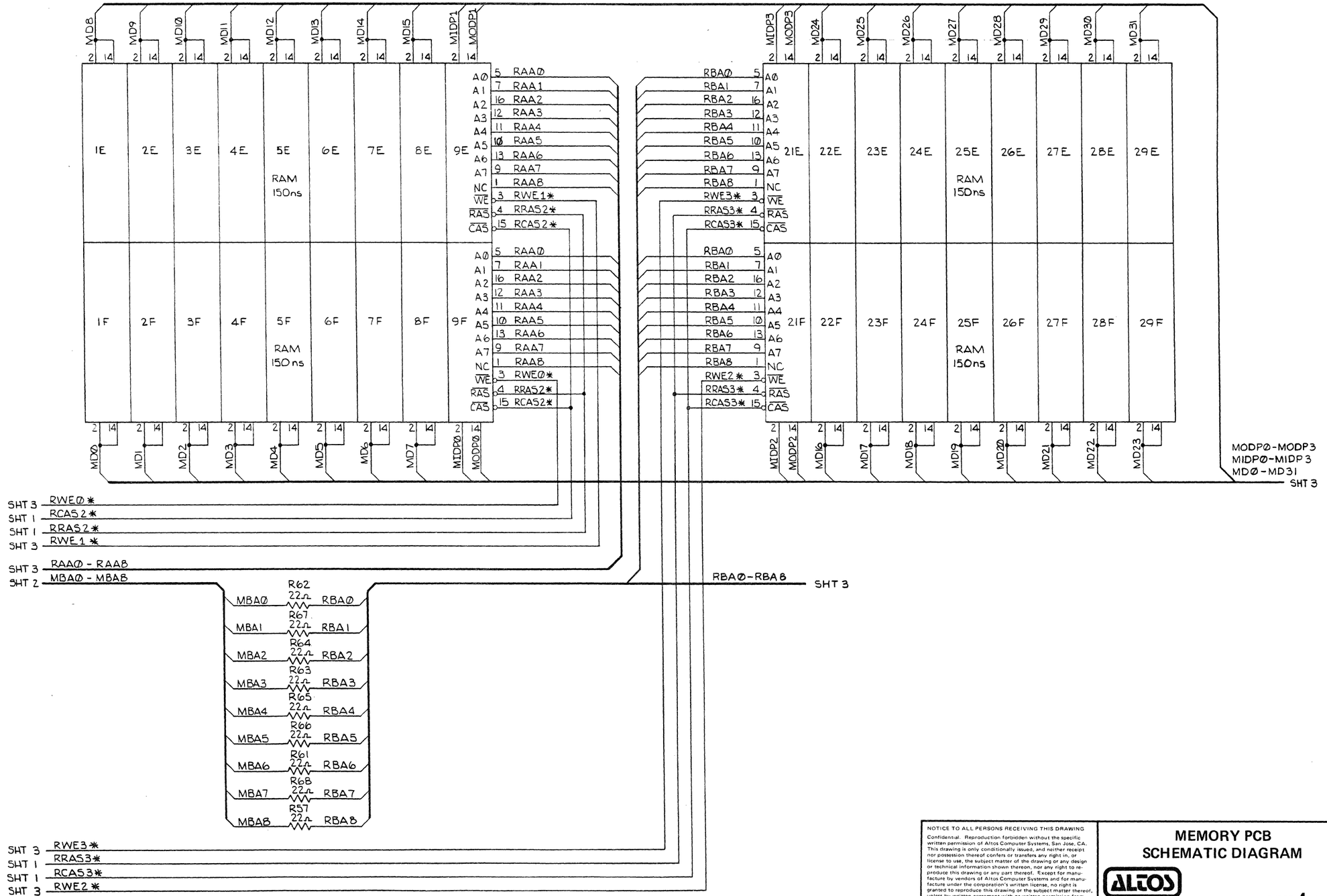
RAA0-RAA8 — SHT 4
SHT 4 RBA0-RBA8
SHT 1 RCAS0*
SHT 1 RRAS0*
SHT 1 RRAS1*
SHT 1 RCAS1*

MEMORY PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV
625-15148-XXX	4	5A

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



MEMORY PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO. 625-15148-XXX | SH. 5 | REV. 5A

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

SHT 3 RWE3*
SHT 3 RWE2*
SHT 1 RRAS5*
SHT 1 RCAS5*
SHT 2 MCA0 - MCA8
RCA0 - RCA8 SHT 4

R9 22Ω MCA0 RCA0
R10 22Ω MCA1 RCA1
R11 22Ω MCA2 RCA2
R6 22Ω MCA3 RCA3
R8 22Ω MCA4 RCA4
R13 22Ω MCA5 RCA5
R7 22Ω MCA6 RCA6
R12 22Ω MCA7 RCA7
R14 22Ω MCA8 RCA8

SHT 3 RWE1*
SHT 3 RWE0*
SHT 1 RRAS4*
SHT 1 RCAS4*

MD8 MD9 MD10 MD11 MD12 MD13 MD14 MD15 MIDP1 MODP1
MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7 MIDP0 MODP0
MIDP3 MODP3 MD24 MD25 MD26 MD27 MD28 MD29 MD30 MD31
MIDP2 MODP2 MD16 MD17 MD18 MD19 MD20 MD21 MD22 MD23

RCA0 RCA1 RCA2 RCA3 RCA4 RCA5 RCA6 RCA7 RCA8
RDA0 RDA1 RDA2 RDA3 RDA4 RDA5 RDA6 RDA7 RDA8
A0 A1 A2 A3 A4 A5 A6 A7 A8 NC
WE RAS CAS

1C 2C 3C 4C 5C 6C 7C 8C 9C
21C 22C 23C 24C 25C 26C 27C 28C 29C
1D 2D 3D 4D 5D 6D 7D 8D 9D
21D 22D 23D 24D 25D 26D 27D 28D 29D

RAM 150 ns

MDA0 - MDA8
R49 22Ω MDA0 RDA0
R52 22Ω MDA1 RDA1
R51 22Ω MDA2 RDA2
R48 22Ω MDA3 RDA3
R50 22Ω MDA4 RDA4
R53 22Ω MDA5 RDA5
R47 22Ω MDA6 RDA6
R54 22Ω MDA7 RDA7
R55 22Ω MDA8 RDA8

MIDP0 MIDP1 MIDP2 MIDP3
R15 4.7K R1 4.7K R37 4.7K R38 4.7K
11E 13E 12E 14E
AS280 EVEN

MODP0 - MODP3
MIDP0 - MIDP3
MD0 - MD31 SHT 3

15E F20 PERR
20J F240 ERR* P1-C31
MRCY*

RDA0 - RDA8 SHT 6
SHT 1 ADMAT
SHT 3 MRD

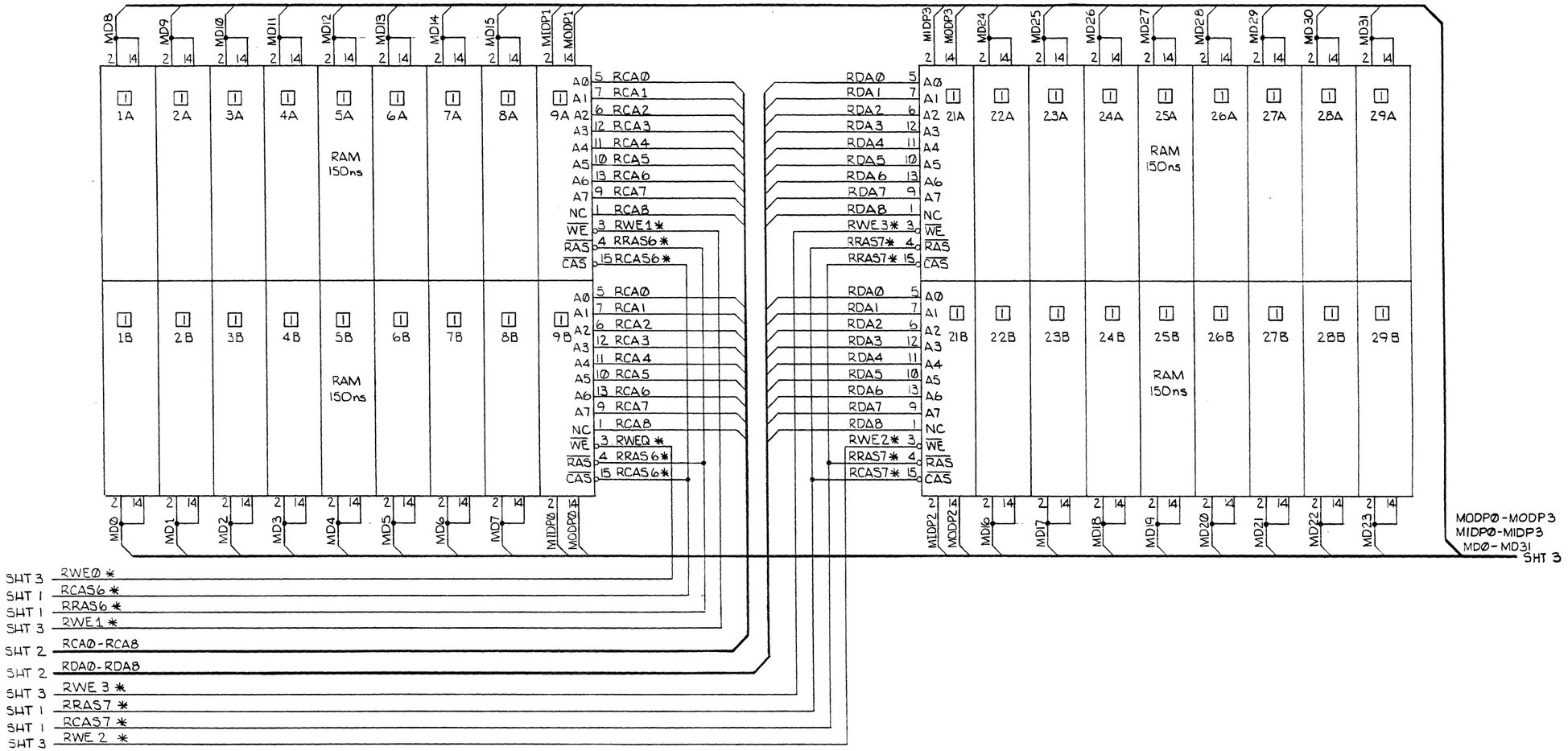
MEMORY PCB SCHEMATIC DIAGRAM

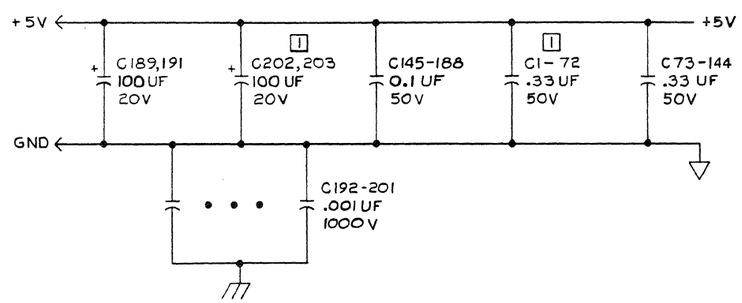
ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV.
625-5148-XXX	6	5A

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	1	SEE SHEET 1		

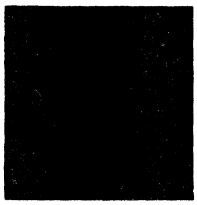




MEMORY PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

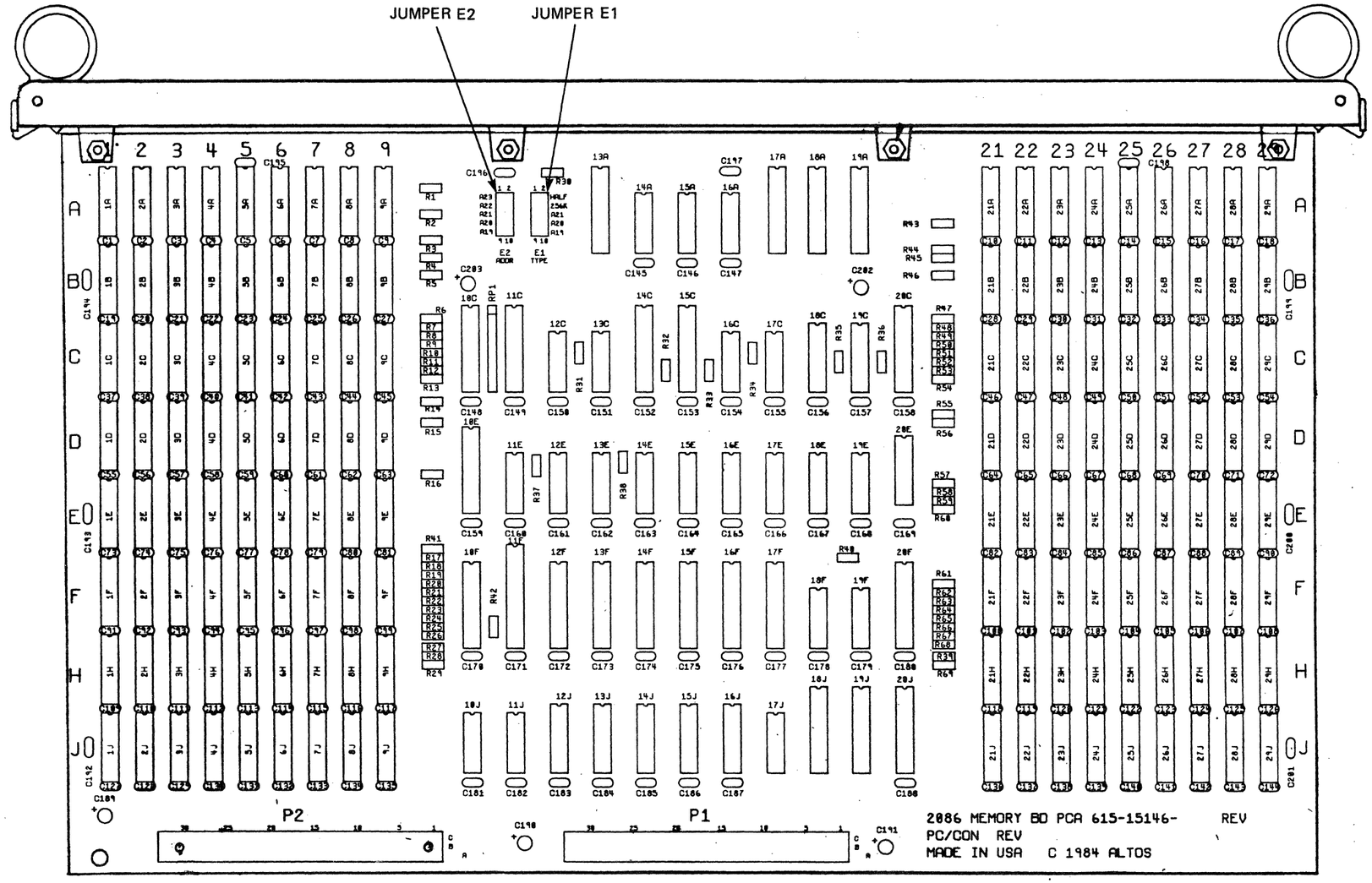
MEMORY PCB
PART LOCATIONS
615-15146-XXX



DWG. NO.	SH	REV.
615-15146-XXX	1	7A

REVISIONS

REV.	ZONE	DESCRIPTION	DATE	APPROVED
x1A		PROTOTYPE	7-15-84	
x2A		PROTOTYPE	8-15-84	
x3A		PROTOTYPE	9-21-84	
x4A		PROTOTYPE	2-16-85	
4A		PRE-PRODUCTION EO# 2200	1-12-85	
5A		REVISED PER EO # 3165-H	24 MAY 95	
6A		EO 3323-H	22 JUL 95	
7A		EO 3420	7-25-95	



VERSION TABLE	
DASH NO.	DESCRIPTION
-001	1 MEGABYTE MEMORY
-002	2 MEGABYTE MEMORY
-003	4 MEGABYTE MEMORY

MEMORY PCB PART LOCATIONS

ALTOS COMPUTER SYSTEMS

COMMUNICATIONS (SIO) PCB BLOCK DIAGRAM

DWG. NO. 625-15878-XXX	SH	REV. D

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1 OF SCHEM.		

CPU Section

RS 232 / Memory Section

WAITGEN PAL
RDY

8284 CLK GEN
RDY IN
RDY RESET CLK
8MHz

8086 - 2 µP (8 MHz)
READY RESET CLK
AD Ø-15
A S 16-19
SØ-2
20

RS 422 NETWORK PORT

RS-232 INTERFACE

SYNC/ASYNC CHANNELS

CHANNEL 9 CHANNEL 8 | CHANNEL 7 CHANNEL 6 | CHANNEL 5 CHANNEL 4 | CHANNEL 3 CHANNEL 2 | CHANNEL 1 CHANNEL Ø

SCC Ø | SCC 1 | SCC 2 | SCC 3 | SCC 4
A B
D Ø-7 RD,WR, INTACK A Ø,1 CS

CARRIER DETECT

CIO COUNTER /TIMER/ PARALLEL IO
D Ø-7 RD,WR, INTACK A Ø,1

BYTEWORD PAL

RECOVERY PAL

LOCAL BUS

AD Ø-15
D8-15

ADDR. & STATUS LATCH
A 19,18,15
LS Ø,1,2

LOCAL BUS CONTROL (PAL)

IOA Ø,1
MUX

ADDR. BUFF
AD Ø-19
A Ø-19

LA 19,18,15
LS Ø,1,2

REFRESH TIMER

ARBITER (PAL)
REFREQ
SYSBUS DMAREQ
IOPGNT
REFGNT
DMAGNT

SCC Ø SCC 1

REQUEST/ HOLD/READY SYNC

DRQ SYNC

DACK/STROBE SYNC/SYNC

A8-A20 ADDR LATCH

RAM TIMING
CAS

ADDR.MUX & REF CTR MUX

HRQ HLDA RDY DRQ Ø-3 DACK Ø-3 IORD IOWR MRD MWR A Ø-7 D Ø-7

DMA CONTROLLER
AMD 9517 OR INTEL 8237

CAS RAM A Ø-A8 D Ø-15 RAS

RAM ARRAY
32K TO 512K + PARITY

A15-19

MEM DEC PAL

A1-15 RD D Ø-15 CS

PROM

SØ,1,2

8289 SYSTEM BUS ARBITER
BCLK CBRQ BUSY BREQ BPRN

8288 SYSTEM BUS CONTROLLER
IORD MEMRD
IOWR MEMWR

ADDRESS BUFFERS
A Ø-A23

D Ø-15

Data Bus Receivers

Pages in schematics where circuits are located

Systems Bus Interface Sec.

Arbitrates & control of system bus

Arbitrate & control of local bus

Interface between DMA (9517) IOA (8086) REFRESH

NOTICE TO ALL PERSONS RECEIVING THIS DRAWING	COMMUNICATIONS (SIO) PCB BLOCK DIAGRAM
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	SHEET 1 OF 1

COMMUNICATIONS (SIO) PCB SCHEMATIC DIAGRAMS

11

DWG. NO.	SH	REV.
625-15878-XXX	1	D

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
	3A	PROTOTYPE	1-28-85	
	3A	PRE-PRODUCTION EO# 3909	3-1-85	
	4A	EO 3011-H	5-29-85	
	5A	REVISED PER EO# 3284-H	7-25-85	
	A	ARCO REL EO 3544-H	8-29-85	
	B	REVISED PER EO 3750	11-4-85	
	C	REV PER SO # 3878-H SR	11 FEB 86	
	D	EO# 4722-H	7-17-86	

SHT 8 NT
SHT 2 NMI
SHT 2 ALE
P1-A31 REST*
P1-C29 AACK*
P1-A29 XACK*
SHT 2 XMBDEN*
SHT 7 PROMCS*
SHT 6 DMACS*
SHT 6 MISCCS*
SHT 8 RWAIT*
SHT 5 DMAREQ*
SHT 6 REFREQ*

R49 33K 10 ms
C54 .1µf 25V
LS123
RP1 4.7K
R53 510Ω
Y1 24 MHz
R54 510Ω
CR2 1N4004
R72 10K
R68 220Ω
C81 10µf 20V
E3
P.U.
R69 10K
LS32
LS10
R77 220
R78 220
8284 10D
CSYNC CLK
RES RESET
READY
RDY1
RDY2
F/C
EFI
ASYNC
X1 X2
OSC
PCLK
E9
R75,22Ω
R55 51Ω
R59 2.2K
8086-2 8E
RESET
READY
MAX LOCK BHE/S7 S2 S1 S0
A19/S6 A18/S5 A17/S4 A16/S3
AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
NMI INT
RQ/GT0 RQ/GT1 TEST
QS0 QS1 RD
BHE* S2* S1* S0*
BHE*
AS16-AS19
AD0-AD15
S0*,S1*,S2*
LOCK*
RESET*
86CLKa
TIMEOUT
OSC
PCLK
86CLK
86CLK*
AS04
LS04
15C BUS CONT 16R6A
LOCK RESET
IORD IOWR MEMCY MEMW INTAK T23W
STVAL IOPGNT OE DS
SIP RPAK
IORD* IOWR* MEMCY* MEMW* INTAK*
DS*
LOCAL BUS CONTROLLER
LS08
LS2*-LS0*
PROMCS DMACS MISCCS RWAIT READY
W1 W2 W3 W4
OE T23W S2 S1 S0 IOPGNT DS LOCK
PAL*3 16R4A 10C WAIT GENERATOR
ALS373 9D
AS19 AS18 AS17 AS16 AD15
LA19 LA18 LA15 NC NC
R52 220Ω
LS74 7D
11C PAL#1 ARBITOR 16R6A
S2 S1 S0 A19 A18 A15 LOCK STVAL
IOPGNT DMAGNT REFGNT SYSBUS T23W LOCIO
DMAREQ REFREQ
R41 220Ω
IOPGNT* DMAGNT* REFGNT* SYSBUS*
LOCIO*

VERSION TABLE	
DASH NO.	DESCRIPTION
-001	2086/3068 COMM. CB.
-002	STAND ALONE COMM. BD.
-003	128K RAM

NOTES: UNLESS OTHERWISE SPECIFIED.

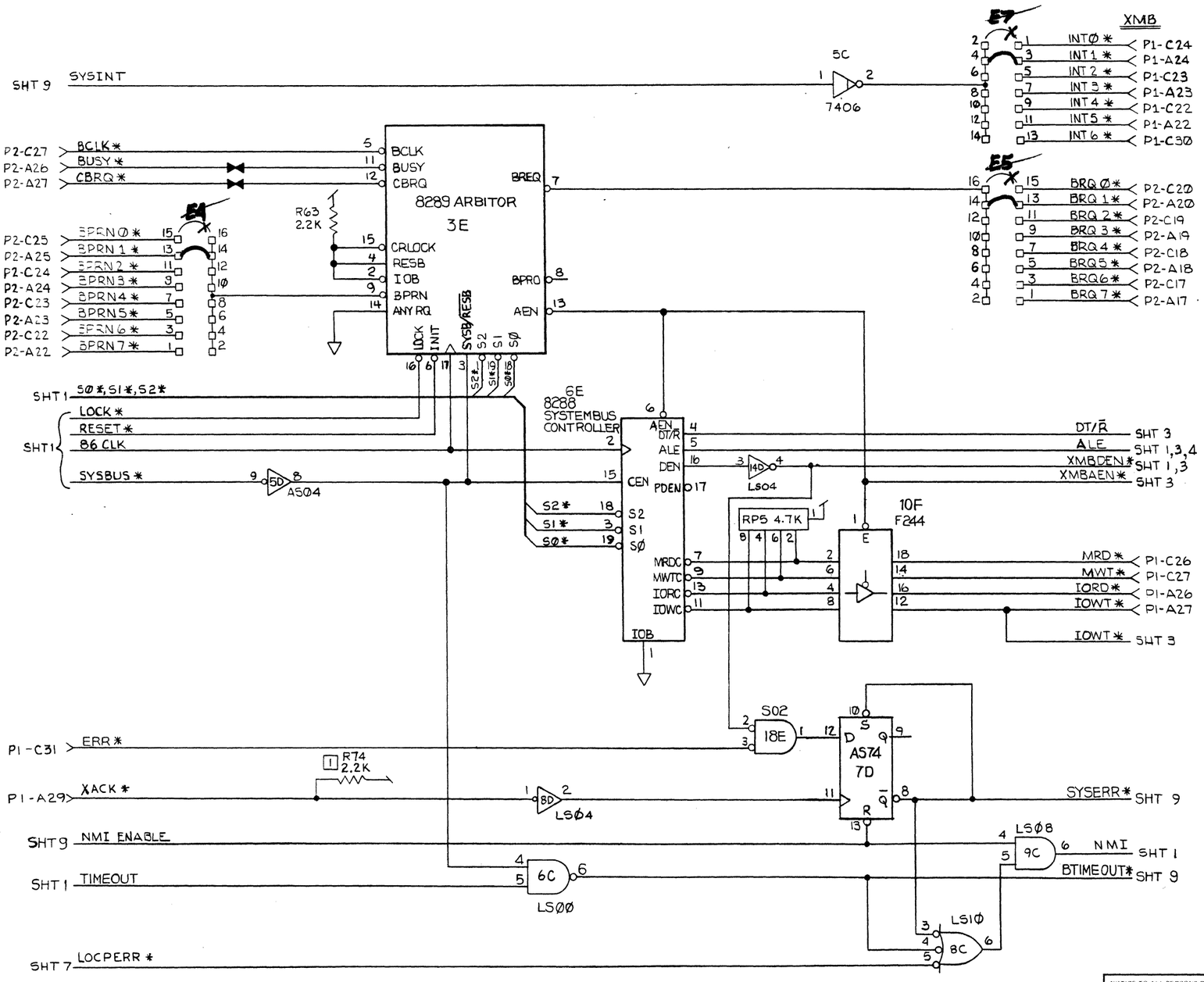
1. USED ONLY ON -002.
2. 2732 AND 27128 ARE OPTIONAL I.C.'S.
3. FOR JUMPER PINNING SEE MAINTENANCE MANUAL' APPENDIX A
4. 47 OHM DIP ON -001 AND -002
   33 OHM DIP ON -003

COMMUNICATIONS (SIO) PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH.	REV.
625-15878-XXX	2	D

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



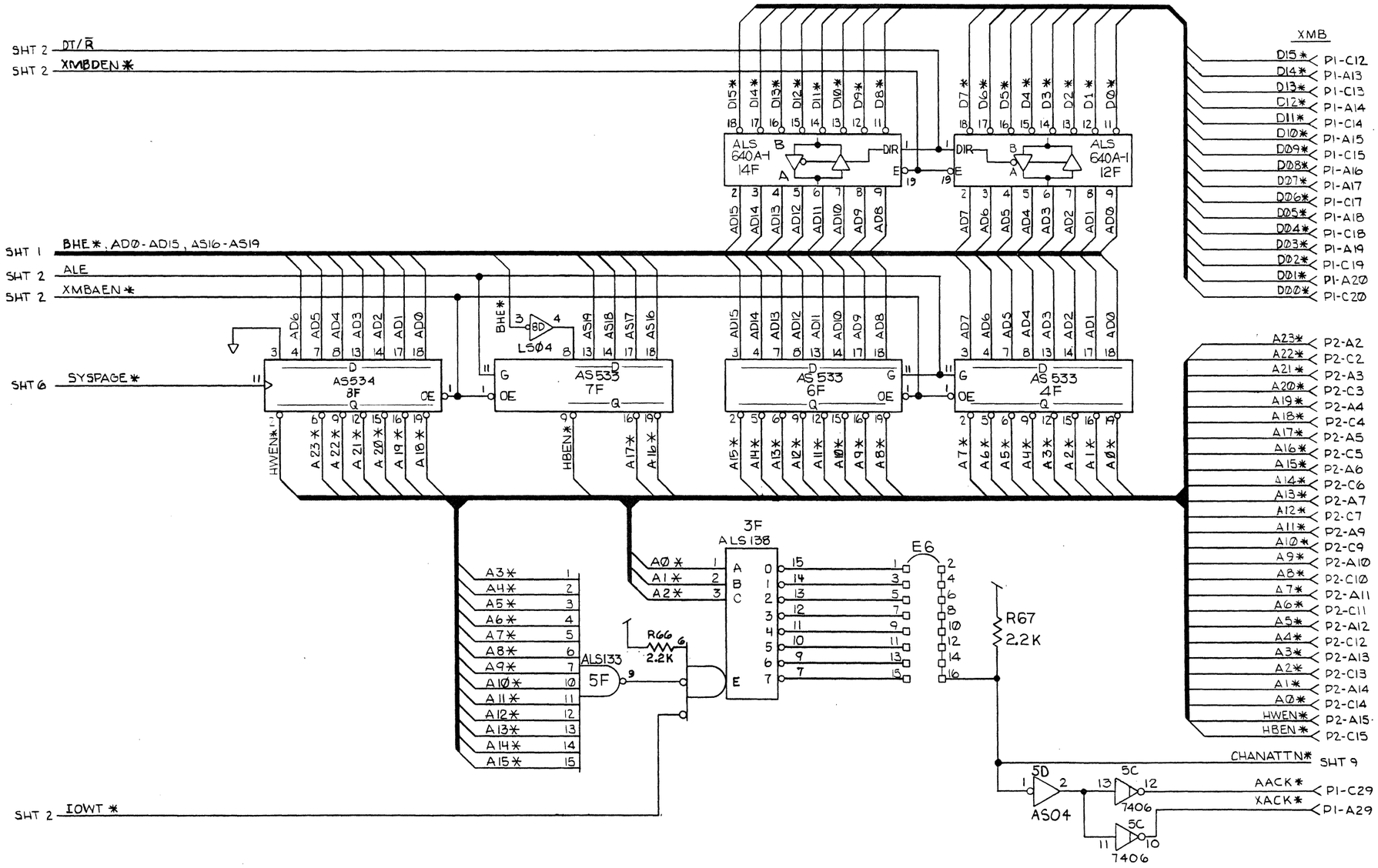
COMMUNICATIONS (SIO) PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH.	REV.
625-15878-XXX	3	D

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

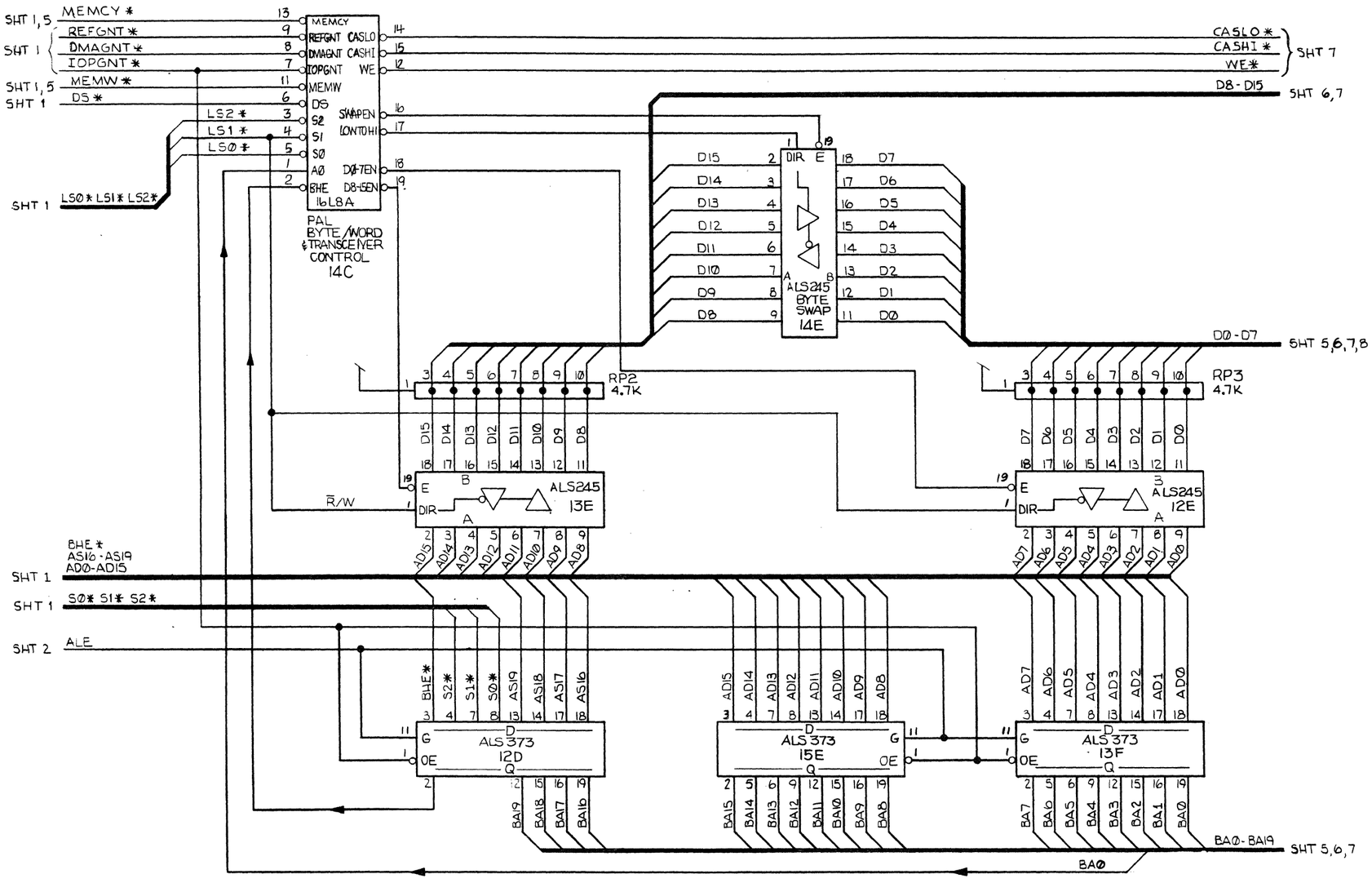


COMMUNICATIONS (SIO) PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	625-15878-XXX	SH.	REV
		4	D

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

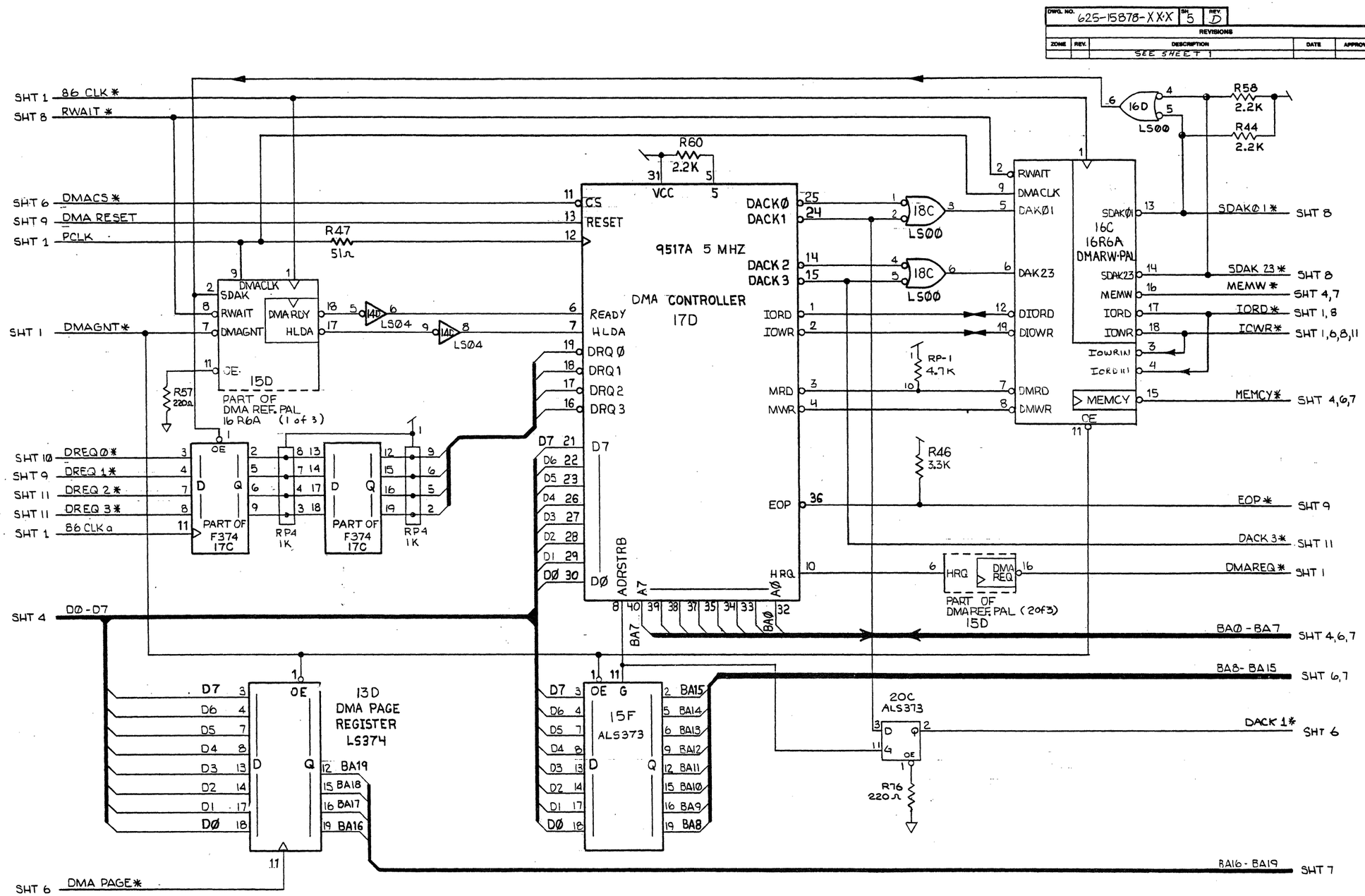


COMMUNICATIONS (SIO) PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH.	REV.
625-15878-XXX	5	D

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



DMA CONTROLLER

COMMUNICATIONS (SIO) PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO. 025-15878-XXX	SH. 6	REV. D

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

SHT 1 LOCIO*

SHT 1,5 IOWR*

SHT 1 DMAGNT*

SHT 5 DACK 1*

SHT 1 OSC

SHT 4,5 BA0-BA7

SHT 4,5 BA8-BA15

SHT 7 PROMCS*

SHT 1,5 MEMCY*

SHT 1 86CLKa

SHT 1 REFGNT*

ALS138 E 19C

CIO* SCC2* SCC3* SCC4* SCC0* SCC1* SHT 8

DMACS* SHT 1,5

MISCCS* SHT 1

ALS138 E 7E

SYSPAGE* SHT 3

DMAPAGE* SHT 5

13C LS157

IOA1 SHT 8

IOA0 SHT 8

RP1 4.7KΩ

R43 220Ω

R51 2.2K

4D LS163

6 MHz SHT 8,11

2764 "HIGH" 20C-B

2764 "LOW" 20C-A

4.7K R32

D0-D7 SHT 4

D8-D15 SHT 4

7C LS393

1mSEC

8C LS10

15D 16R6A

PART OF DMAREF.PAL (3 OF 3)
(REFRESH REQUEST CONTROL)

REFREQ* SHT 1

I/O PORT DECODE, REFRESH, PROM

COMMUNICATIONS (SIO) PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO. 025-15878-XXX	SH. 7	REV. D

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

SHT 4 CASHI* 1 — 17H — 2 — LS04

SHT 4 CASLO* 3 — 17H — 4 — LS04

SHT 4 WE*

SHT 2&6 MEMCY*

SHT 1 86 CLKa

SHT 1 86 CLK*

SHT 1,5 MEMW*

SHT 5&6 BA15 - BA19

SHT 1 REFGNT*

SHT 4,5 BA1-BA7

SHT 4,5 BA8-BA18

SHT 9 NMIENABLE

R64 2.2K

17E AS74

16E AS74

P.U.

18H — S00

INSTALL JUMPER FOR 256K dRAMS

R65 2.2K

E8 — E2

PAL #7 16L8A MEMORY DECODE 19E

PROMCS

LARGE RAM

RASPAR

MEMCY — RAS 3

MEMW

BA19 — A19
BA18 — A18
BA17 — A17
BA16 — A16
BA15 — A15

RAS 2

RAS 1

REFGNT

REFRAS

RAS0

PECLK

4 20E

PROMCS* SHT 1,6

RAMA0 14
RAMA1 13
RAMA2 12
RAMA3 11
RAMA4 8
RAMA5 7
RAMA6 6
RAMA7 10

RAMA0-RAMA7

CAS RAS W

9J — 8J — 7J — 6J

5J — 4J — 3J — 2J

18J — 17J — 16J — 15J

14J — 13J — 12J — 11J

4J: 4416 16K x4 16PL

4164 64K x 1 1J

4164 64K x 1 10J

13 RAMA0
12 RAMA1
11 RAMA2
10 RAMA3
7 RAMA4
6 RAMA5
5 RAMA6
9 RAMA7
1 RAMA8

103 102 101 100 G

DO DI

D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0

D8-D15 SHT 4

D0-D7 SHT 4

R70 2.2K

R62 2.2K

AS280 20D — Σ ODD

AS280 21D — Σ EVEN — Σ ODD

18H — S00

LOCPERR* SHT 2,9

16E AS74

RAM

ALS258 17F

ALS258 16F

SELB OE

BA1 BA16 BA2 BA9 BA3 BA10 BA4 BA11

BA5 BA12 BA6 BA13 BA7 BA14 BA8 BA15

BA17

BA18

18E — S02

17H — LS04

÷16 ÷16 — 18F LS393

QA QB QC QD

LS240 19F

20F 22Ω DIP

RAMA0 RAMA1 RAMA2 RAMA3 RAMA4 RAMA5 RAMA6 RAMA7

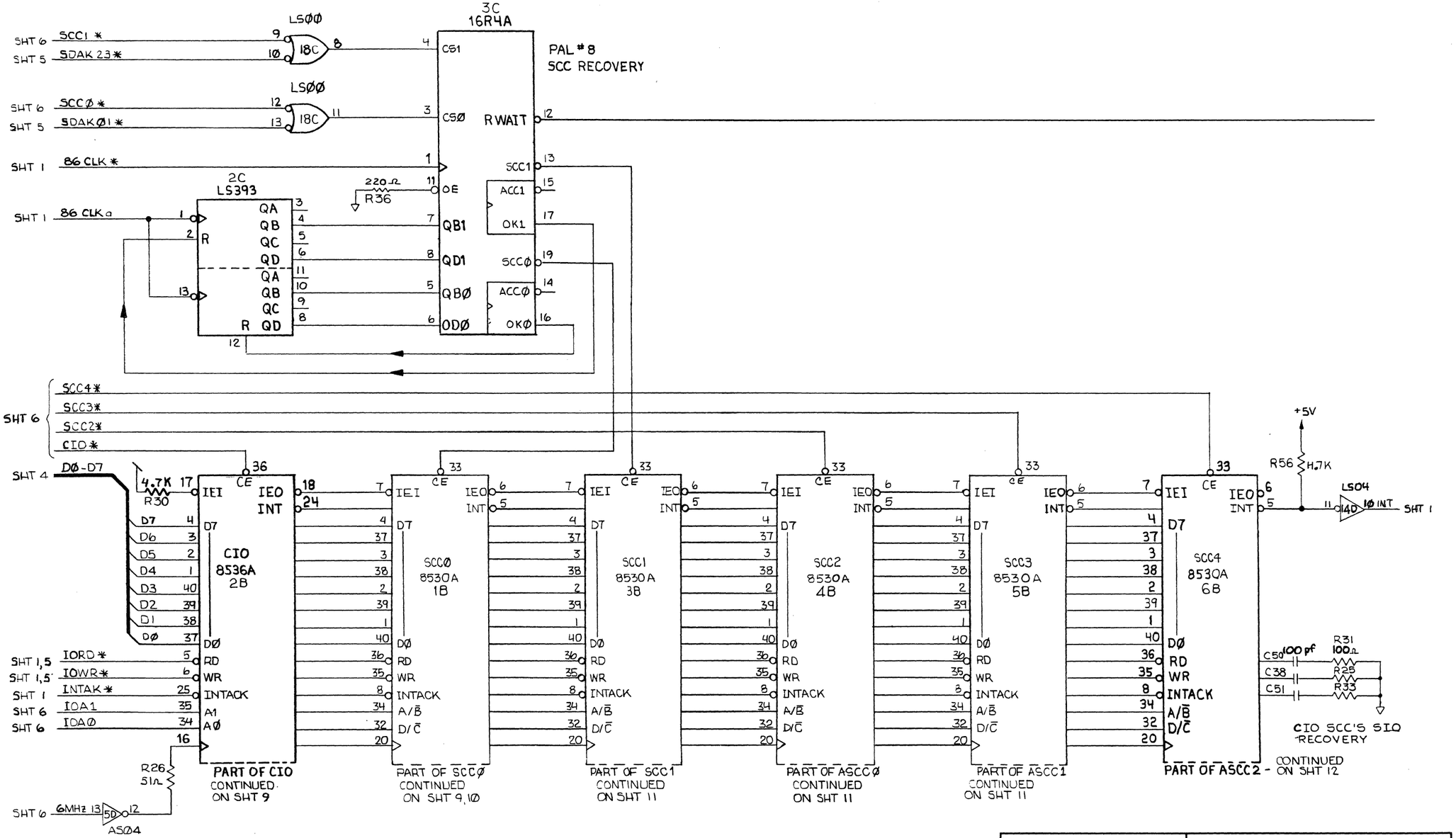
R61 39Ω RAMA8

COMMUNICATIONS (SIO) PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO. 625-1587B-XXX	SH. 8	REV. D

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



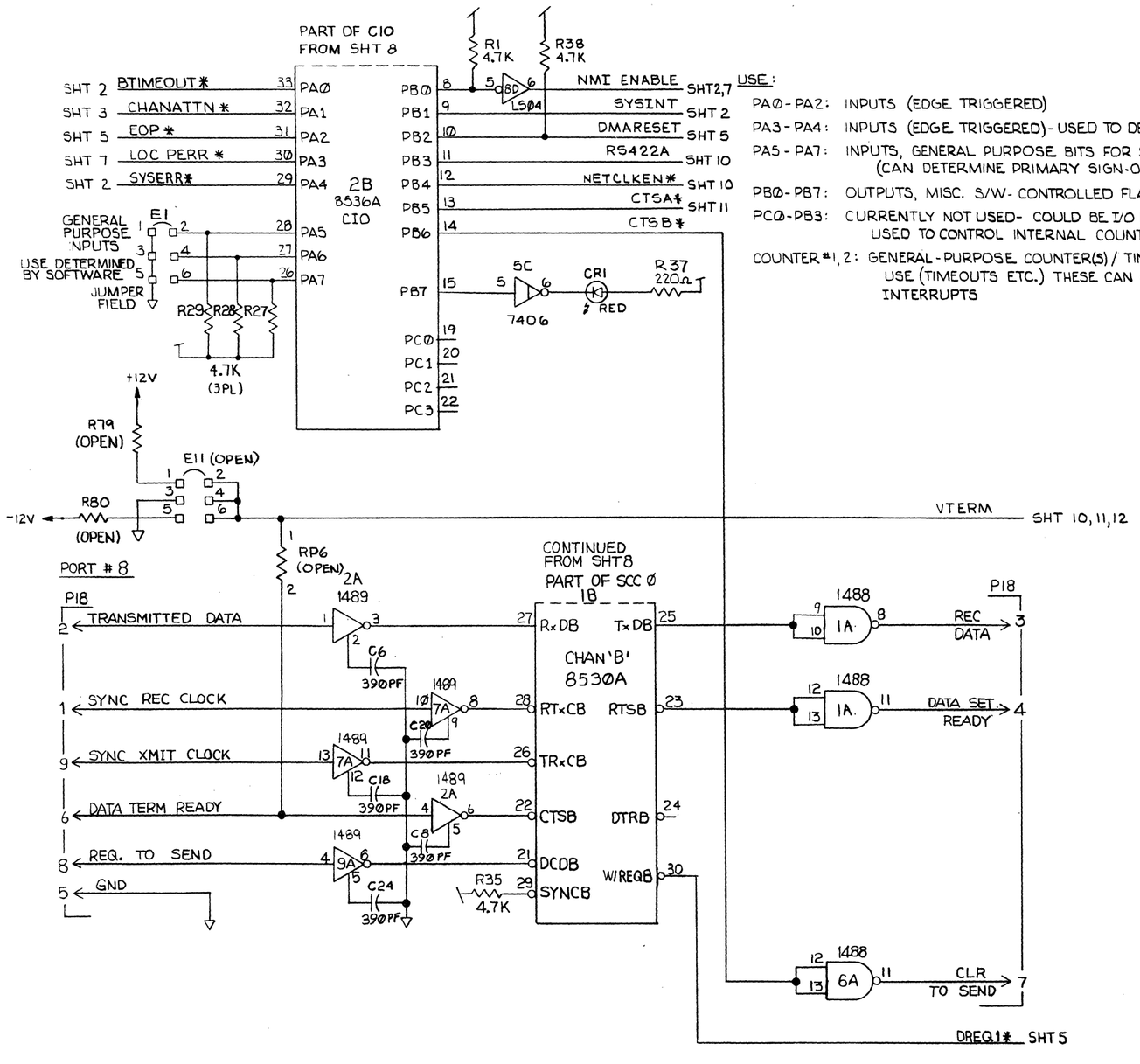
COMMUNICATIONS (SIO) PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV.
625-15878-XXX	9	D

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



USE:

PA0 - PA2: INPUTS (EDGE TRIGGERED)

PA3 - PA4: INPUTS (EDGE TRIGGERED) - USED TO DETERMINE NMI SOURCE

PA5 - PA7: INPUTS, GENERAL PURPOSE BITS FOR S/W USE (CAN DETERMINE PRIMARY SIGN-ON CHANNEL)

PB0 - PB7: OUTPUTS, MISC. S/W - CONTROLLED FLAGS

PC0 - PB3: CURRENTLY NOT USED - COULD BE I/O PINS, OR USED TO CONTROL INTERNAL COUNTER / TIMER #3.

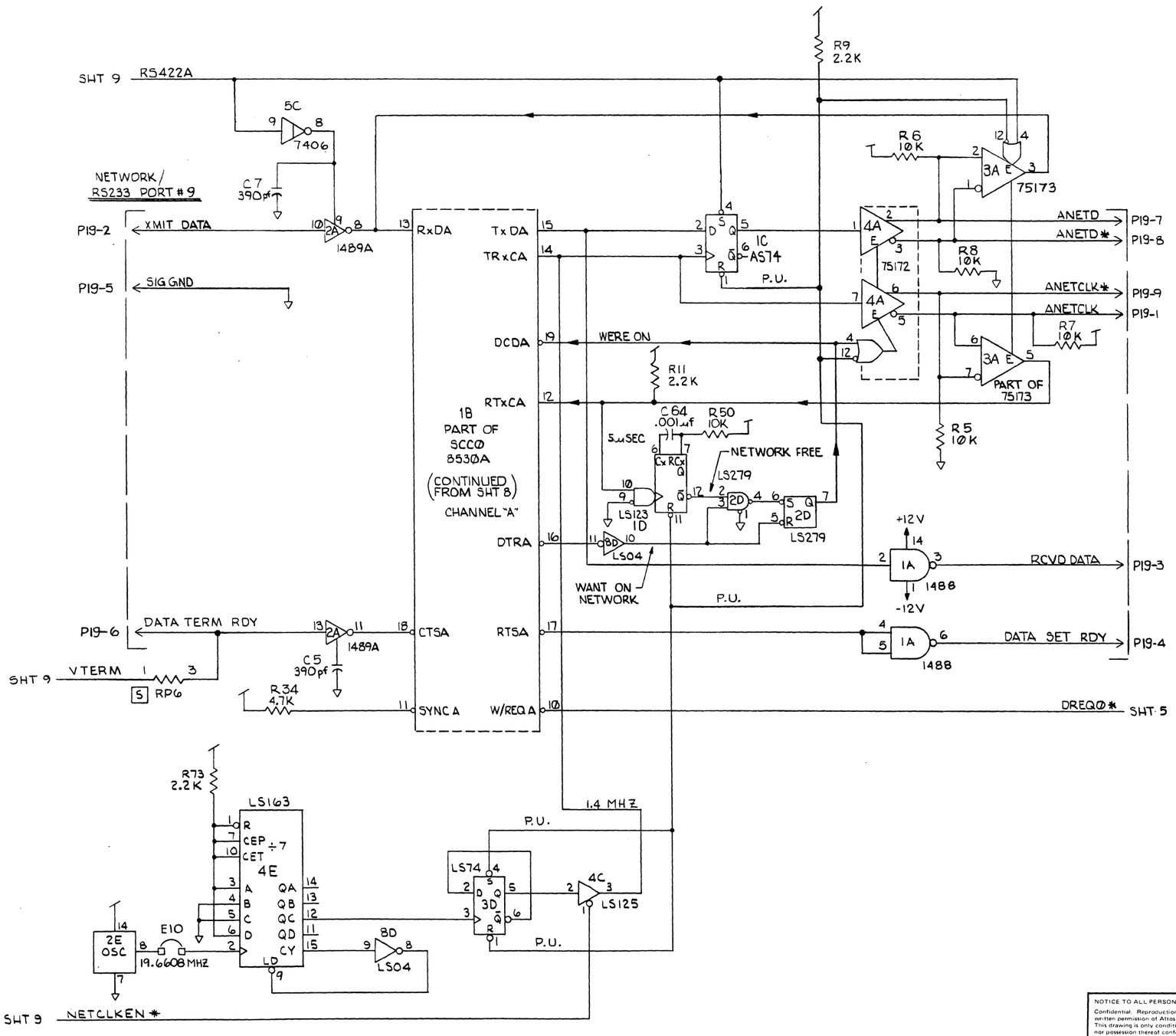
COUNTER #1, 2: GENERAL - PURPOSE COUNTER(S) / TIMER(S) FOR SOFTWARE USE (TIMEOUTS ETC.) THESE CAN GENERATE VECTORED INTERRUPTS

COMMUNICATIONS (SIO) PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV.
625-15878-XXX	10	D

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

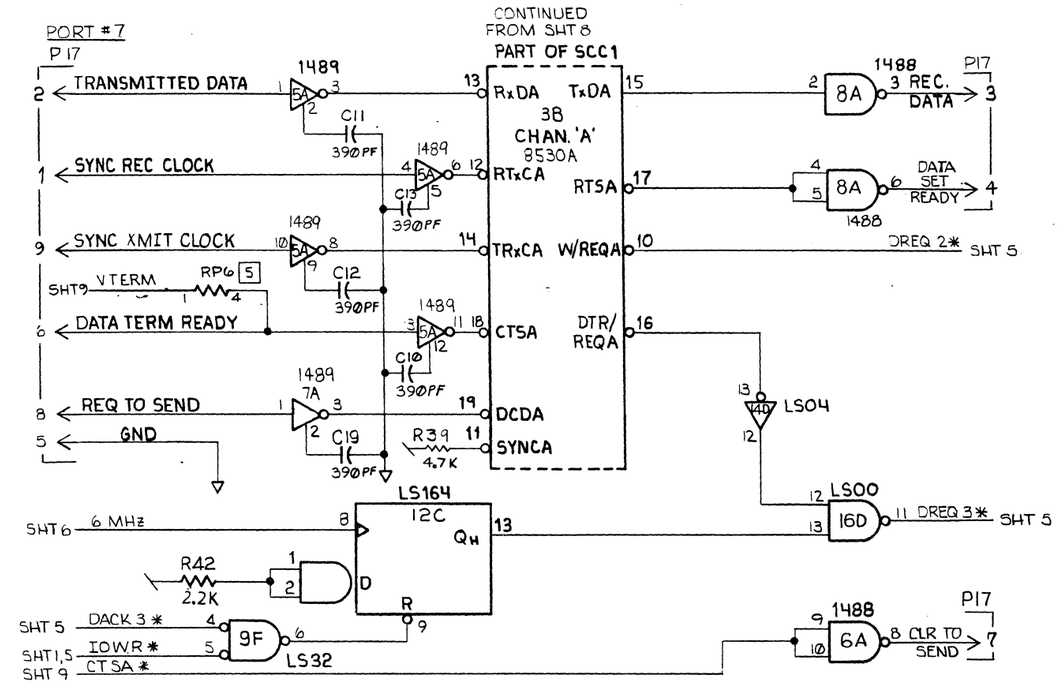


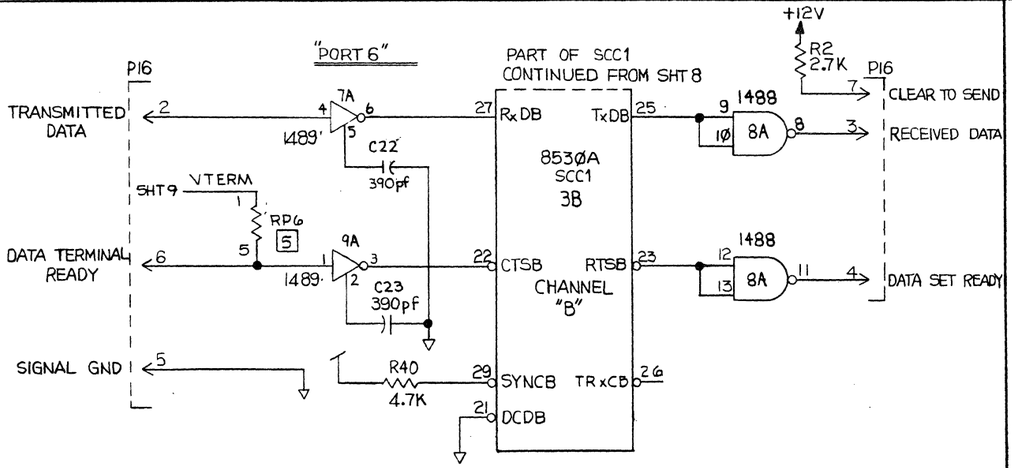
COMMUNICATIONS (SIO) PCB SCHEMATIC DIAGRAM

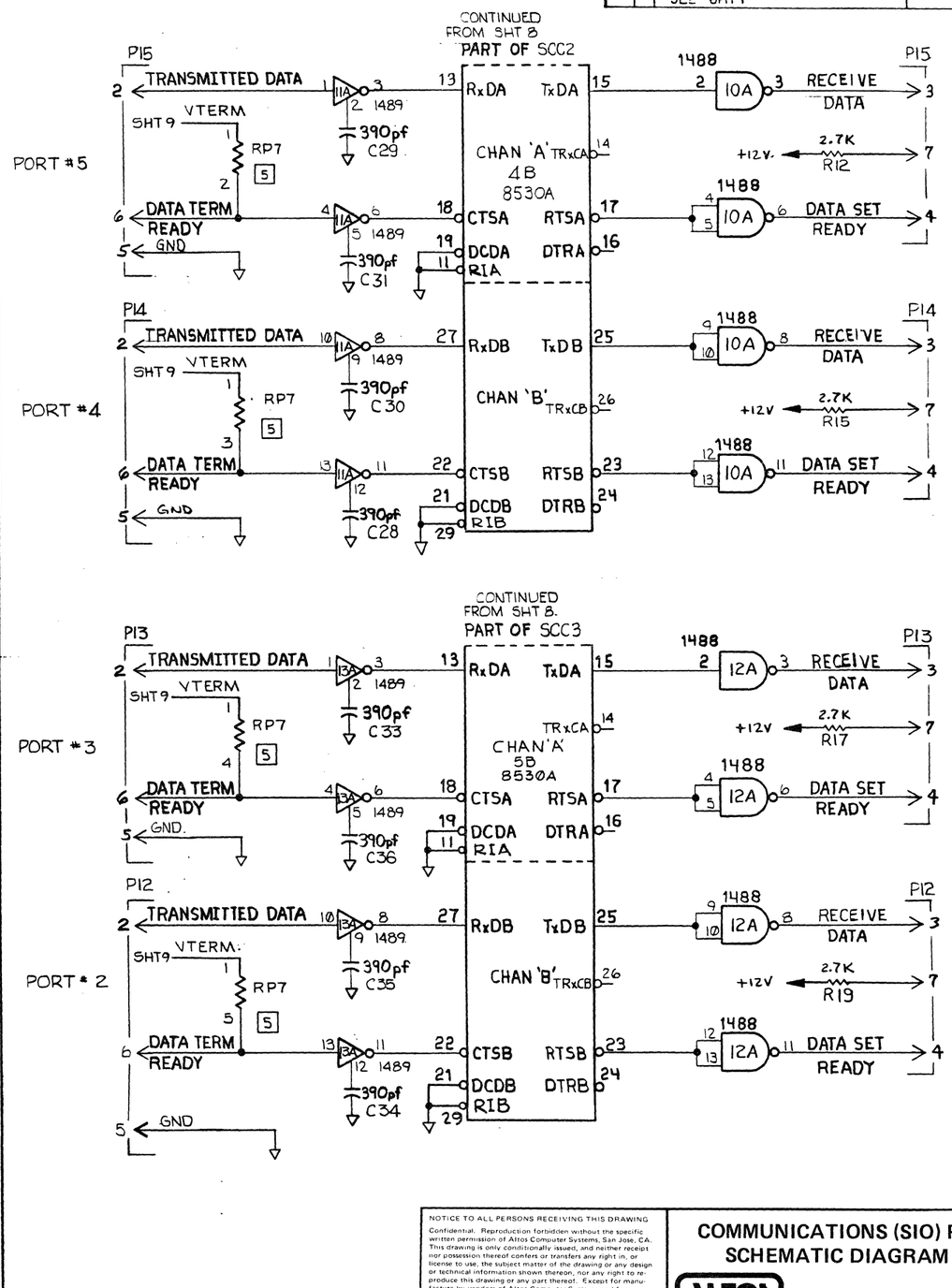
ALTOS COMPUTER SYSTEMS

DWG NO	SH	REV
625-15878-XXX	11	D

REVISIONS				
REV	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHT1		





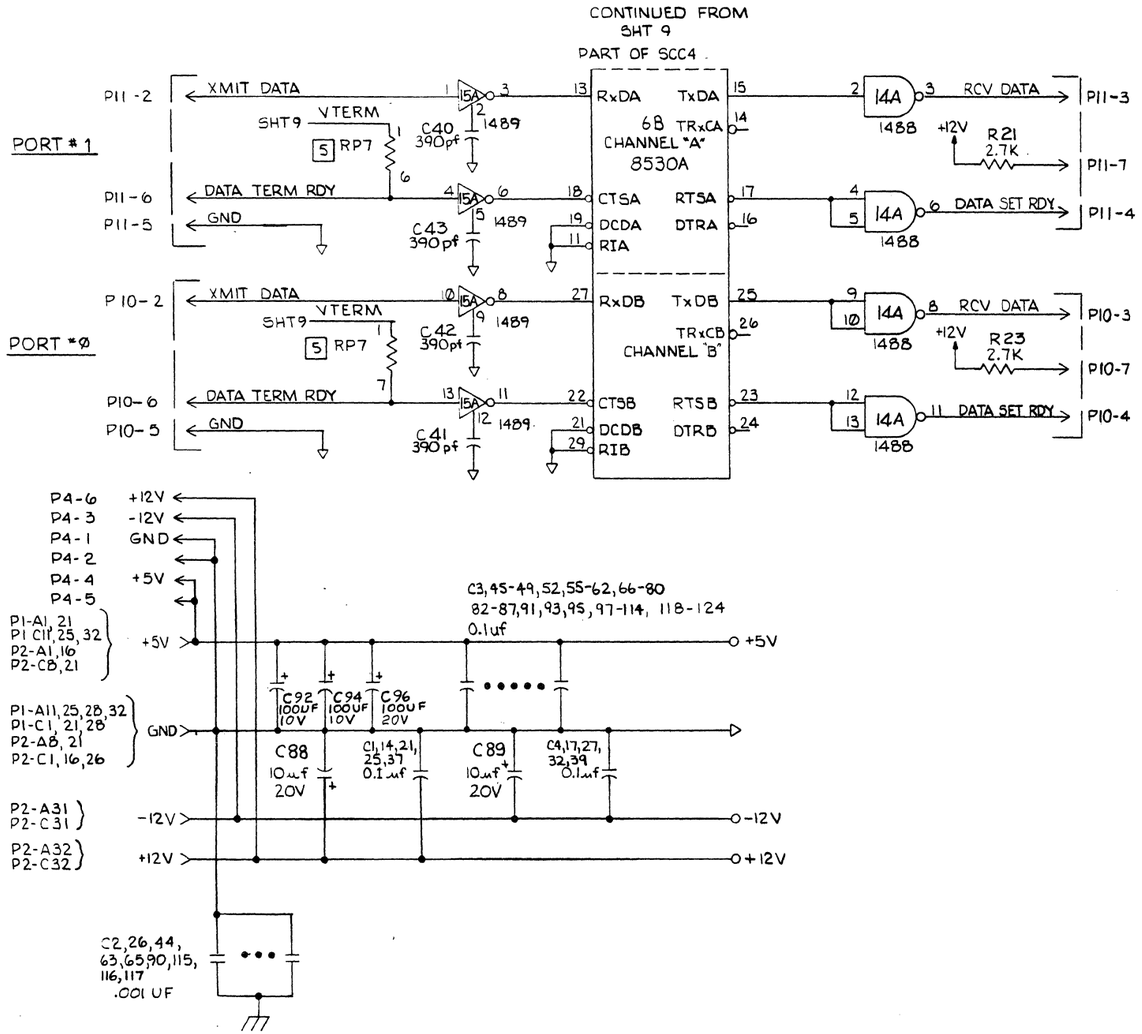


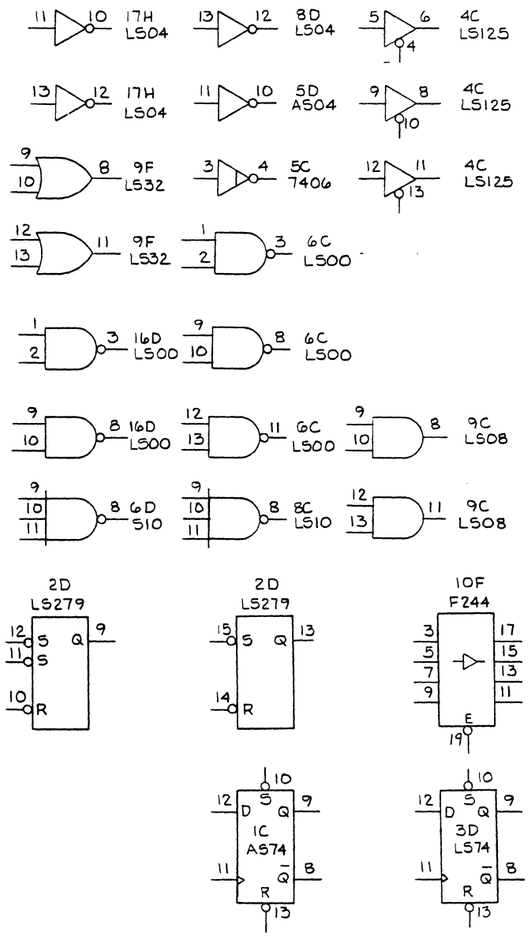
COMMUNICATIONS (SIO) PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV
625-15878-XXX	12	D

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



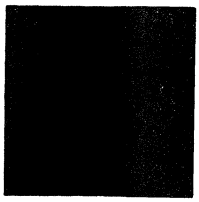


R5232 INTERFACE
POWER / GND DISTRIBUTION
SPARE GATES

COMMUNICATIONS (SIO) PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

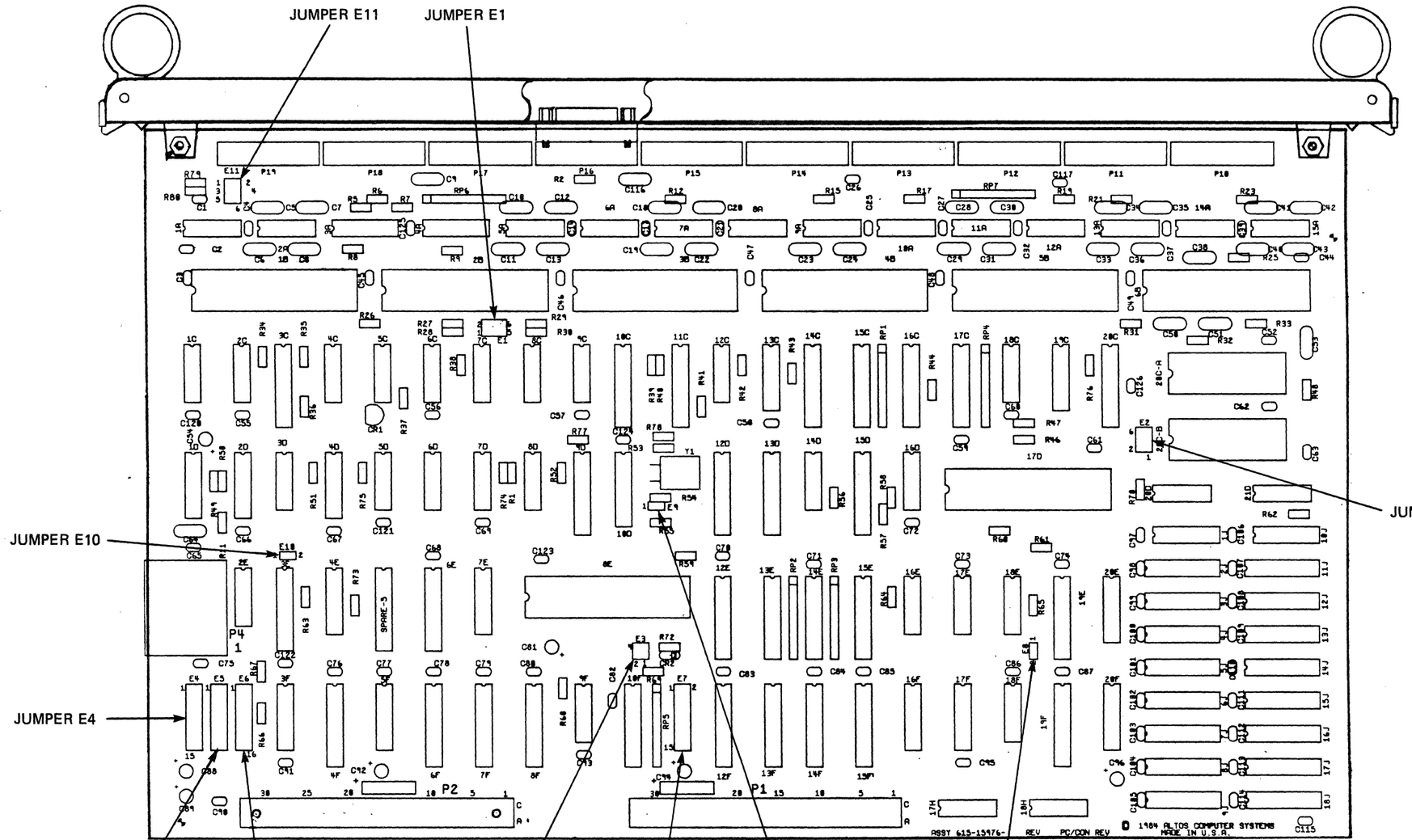
COMMUNICATIONS (SIO) PCB PART LOCATIONS



DWG. NO.	SH	REV
615-15876-XXX	1	9A

REVISIONS

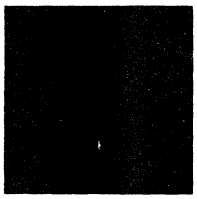
ZONE	REV	DESCRIPTION	DATE	APPROVED
	X1A	PROTOTYPE	10-28-84	
	X2A	PROTOTYPE	1-22-85	
	X3A	PROTOTYPE	2-26-85	
	3A	PRE- PRODUCTION EC# 2900	3-1-85	
	4A	EO 3071-H ACD-003 VERSION	23 MAY 84	
	5A	REVISED PER EO # 3165-H	29 MAY 85	
	6A	REVISED PER EO # 3168-H	6-10-85	
	7A	REVISED PER EO# 3284-H	7-22-85	
	8A	REVISED PER EO # 3334-H	7-25-85	
	9A	REVISED PER EO# 3420	7-29-85	



COMMUNICATIONS (SIO) PCB PART LOCATIONS

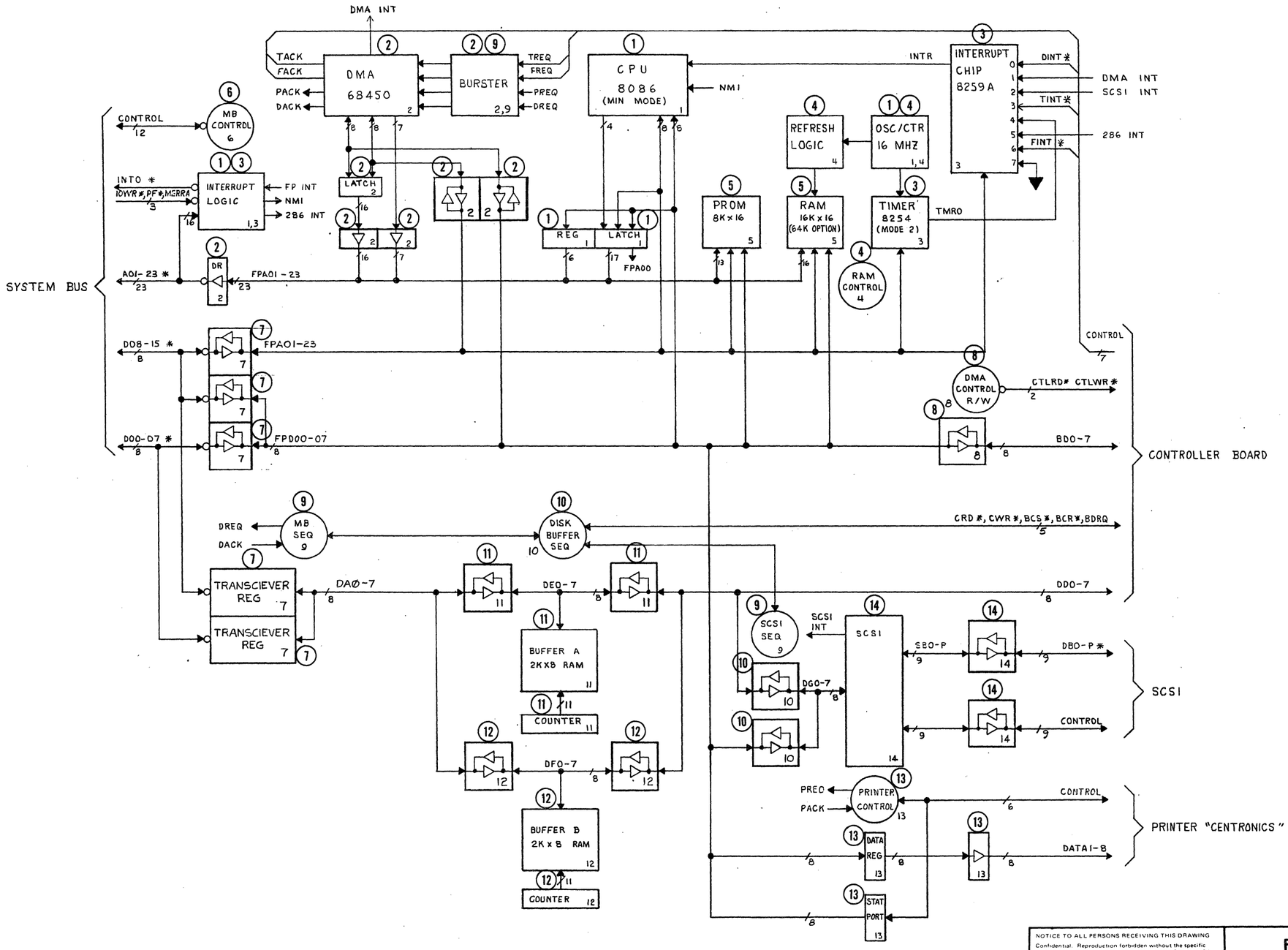
ALTOS COMPUTER SYSTEMS

FILE PROCESSOR PCB BLOCK DIAGRAM



DWG. NO. 625-15818-XXX	SH	REV. F

REVISIONS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1 OF SCHEM.		



FILE PROCESSOR PCB BLOCK DIAGRAM

ALTOS COMPUTER SYSTEMS

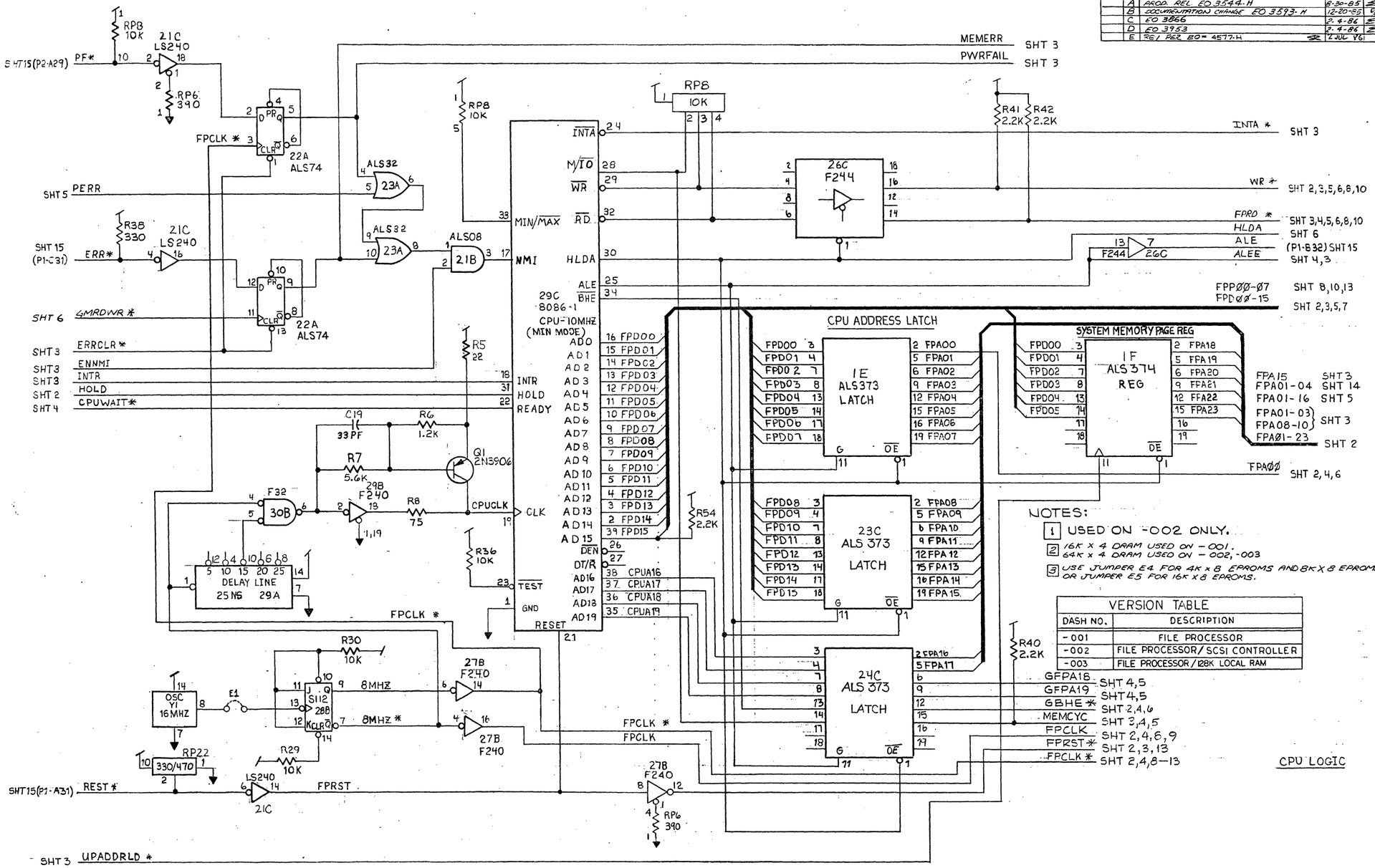
FILE PROCESSOR PCB SCHEMATIC DIAGRAMS

1 1

DWG. NO.	SH.	REV.
625-15818-XXX	1	F

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	F	REVISED PER EO 4759-H		
	A	PROD. REL EO 3544-H	8-30-85	
	B	DOCUMENTATION CHANGE EO 3593-H	12-20-85	
	C	EO 3866	2-4-86	
	D	EO 3953	2-4-86	
	E	REL PER EO# 4577-H	2 JUL 86	



NOTES:

1. USED ON -002 ONLY.
2. 16K x 4 DRAM USED ON -001. 64K x 4 DRAM USED ON -002, -003
3. USE JUMPER E4 FOR 4K x 8 EPROMS AND 8K X 8 EPROMS, OR JUMPER E5 FOR 16K x 8 EPROMS.

VERSION TABLE

DASH NO.	DESCRIPTION
-001	FILE PROCESSOR
-002	FILE PROCESSOR/SCSI CONTROLLER
-003	FILE PROCESSOR/128K LOCAL RAM

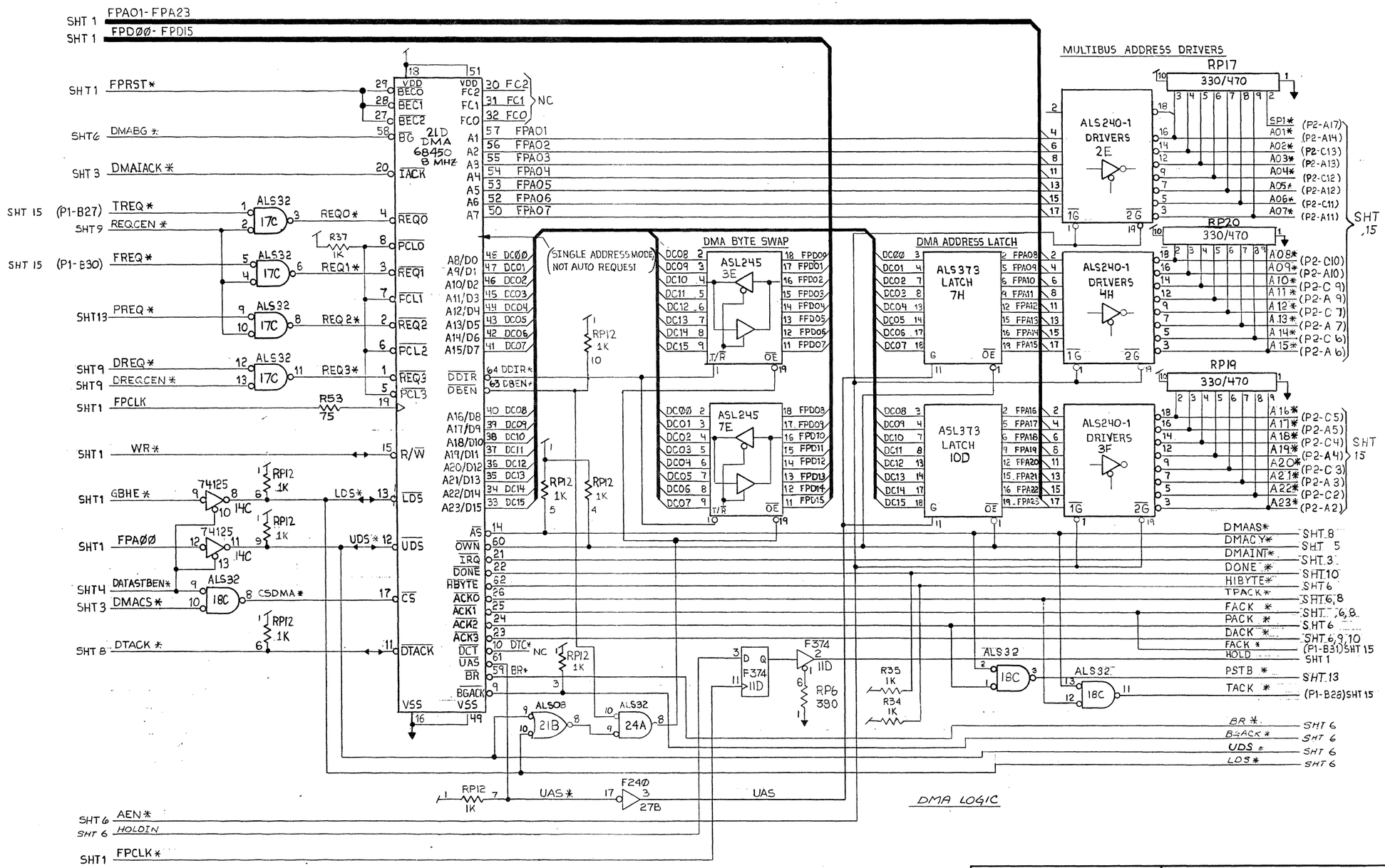
CPU LOGIC

FILE PROCESSOR PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV
625-15818-XXX	2	F

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



FILE PROCESSOR PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH.	REV.
625-1581B-XXX	3	F

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

FA: Processor Address

ALEE
FFAIB
(FPA01-03,08-10)
MEMCYC
MBDONE*
PWRFAIL
MEMERR
PERR
SCSIAVAIL
PRO1
SCSIRSTSTAT
WR*
(FPD00-15)
ALS32 24A
FP STATUS 22C LS244 PORT
27B
F240
5V.
RP8 10K
ALS74 25C
PU

I/O DECODE
DECODE F138 20B
FPA06
FPA09
FPA10
CTLCS*
CTLCS* (P2-B19)
DMACS*
SCSICS*
SHT 8
SHT 15
SHT 2,4
SHT 10,14
TMR CS*
INTCS*
DEC1*
DEC2*

SCSIRST*
SHT 14

DECODE ALS138 20C
FPA01
FPA02
FPA03
UPADDRLD*
PCOMMAND*
SCSIDN*
ERRCLR*
CMDLD*
DSKLD*
SHT 1
SHT 13
SHT 10
SHT 1,5

DMAIACK*
INTR
SHT 2,4
SHT 1

PSTATUS*
SHT 13

CLRSCSIRST*
FPSTATUS*
DECODE ALS138 19C

FP CMD REG
ALS 273 REG 22B
CTLRST*
INT 286
ENNMI
BURSTEN
MBLOCK
INPUT PRIME*
PENABLE
(P2-B18)
SHT 15
SHT 6
SHT 1
SHT 9
SHT 6
SHT 13
SHT 13

DISK MODE REG
ALS273 REG 7F
MBREAD
SCSIMD
INITBUF*
BUFMD1
BUFMD0
SCSICTLRST*
SCSIBUSRST*
SHT 9-12
SHT 9,10
SHT 9,10
SHT 11,12
SHT 11,12
SHT 14
SHT 14

RP15 10K
LS240 26D
DINT*
DMAINT*
SCSIINT
TINT*
FINT*
INTA*
FPRD*
RP6 390
ALS32 4B
SCSIRST
286INT
INTERRUPT 8259A-2 (EDGE MODE) 8H
CS
IR0
IR1
IR2
IR3
IR4
IR5
IR6
IR7
SP/EN
INTA
A0
WR
RD
D0
D1
D2
D3
D4
D5
D6
D7
INT
CAS0
CAS1
CAS2
FPD00
FPD01
FPD02
FPD03
FPD04
FPD05
FPD06
FPD07
286 INTRST*

2F DECODE ALS138
ALS133 4F
A00*
A01*
A02*
A03*
A04*
A05*
A06*
A07*
A08*
A09*
A10*
A11*
A12*
A13*
A14*
A15*
RP22 330/470
1MHZ
IOWT*
IORD*
BURST*
TMR 1 EN
TMR 2 EN
DMAAS*
FPRST*
HLWEN*

25B TIMER 8254
CLK0
CLK1
CLK2
G0
G1
G2
OUT0
OUT1
OUT2
TMR0*
TMR1*
TMR2*
AACK*
(BURST ON DELAY)
(BURST OFF DELAY)
S38 16C
R43 330

I/O DECODE, INTERRUPT & TIMER

File Processor Data Bus

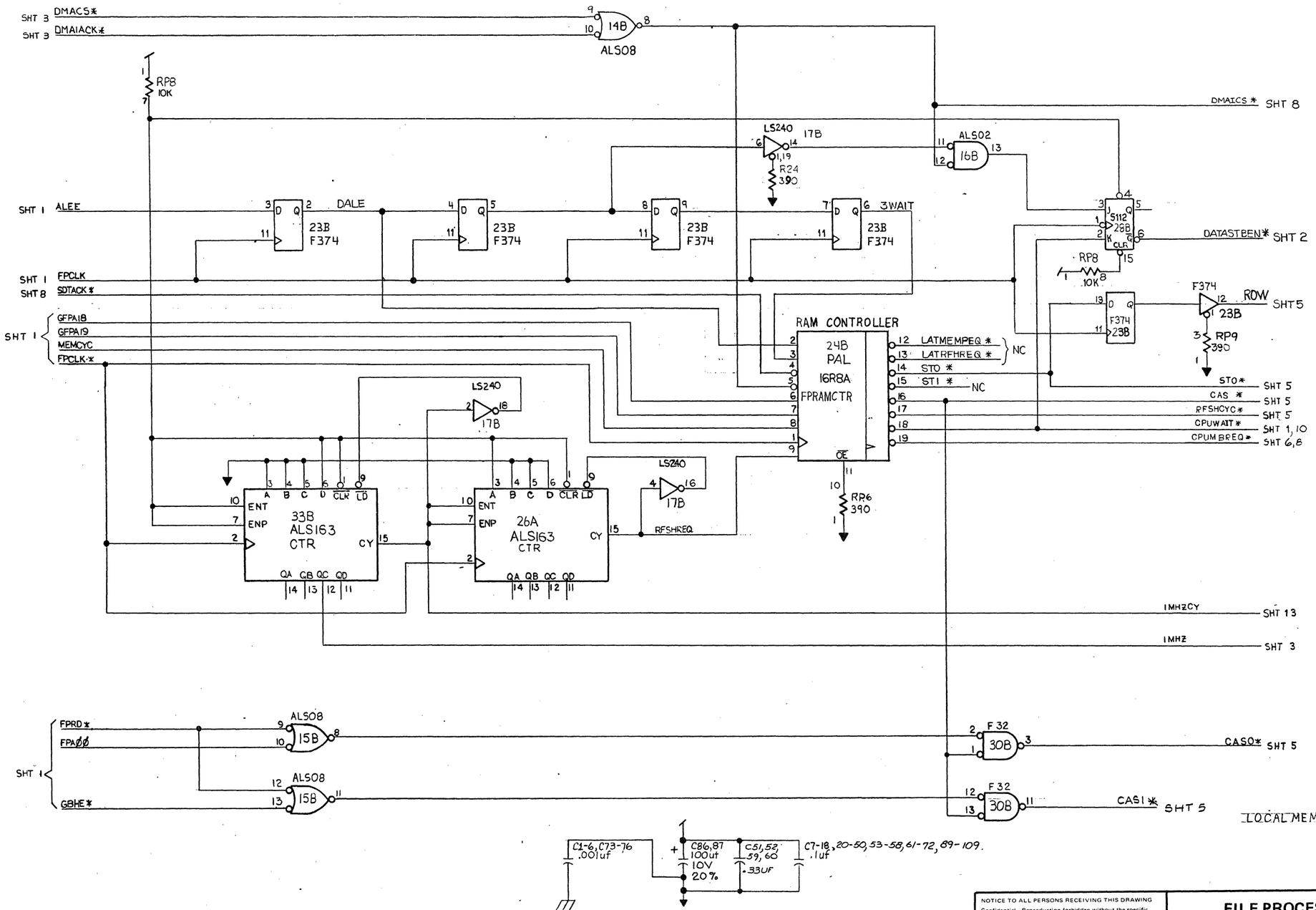
FP Accesses bus in burst to avoid "hanging" bus.

FILE PROCESSOR PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	625-15818-XXX	SH.	4	REV.	F

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



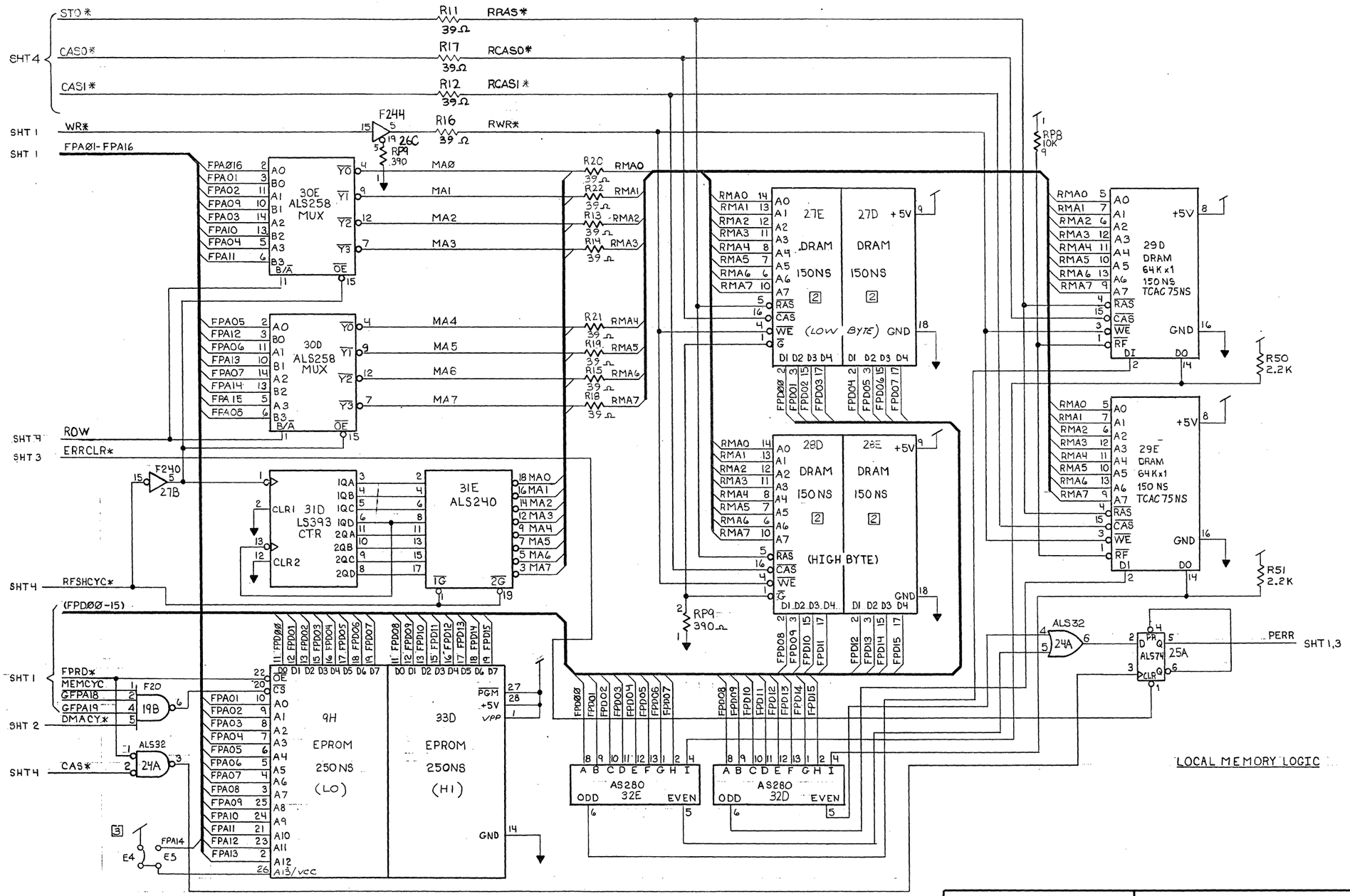
LOCAL MEMORY LOGIC

FILE PROCESSOR PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV
625-15818-XXX	5	F

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

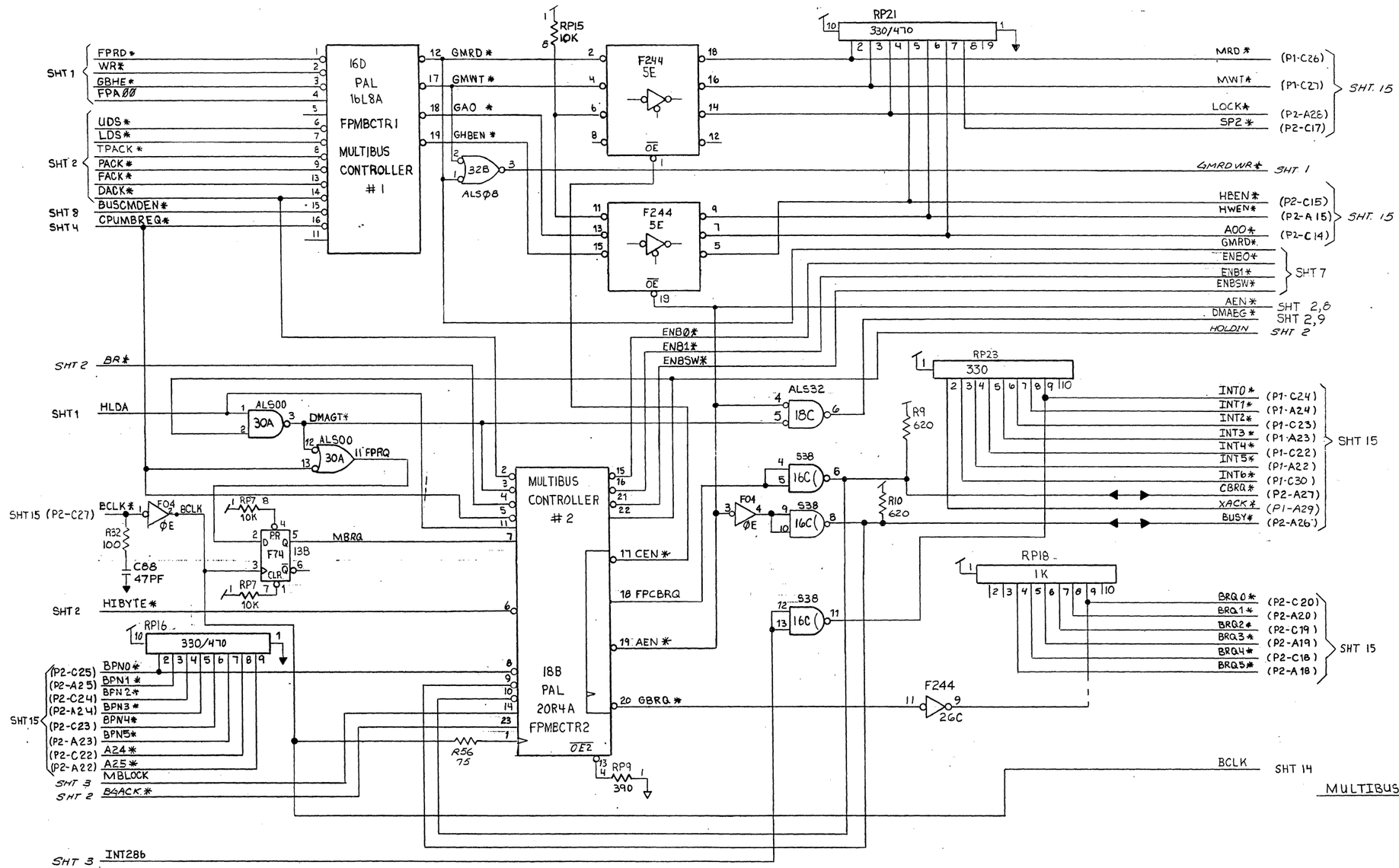


FILE PROCESSOR PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV
625-15818-XXX	6	F

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

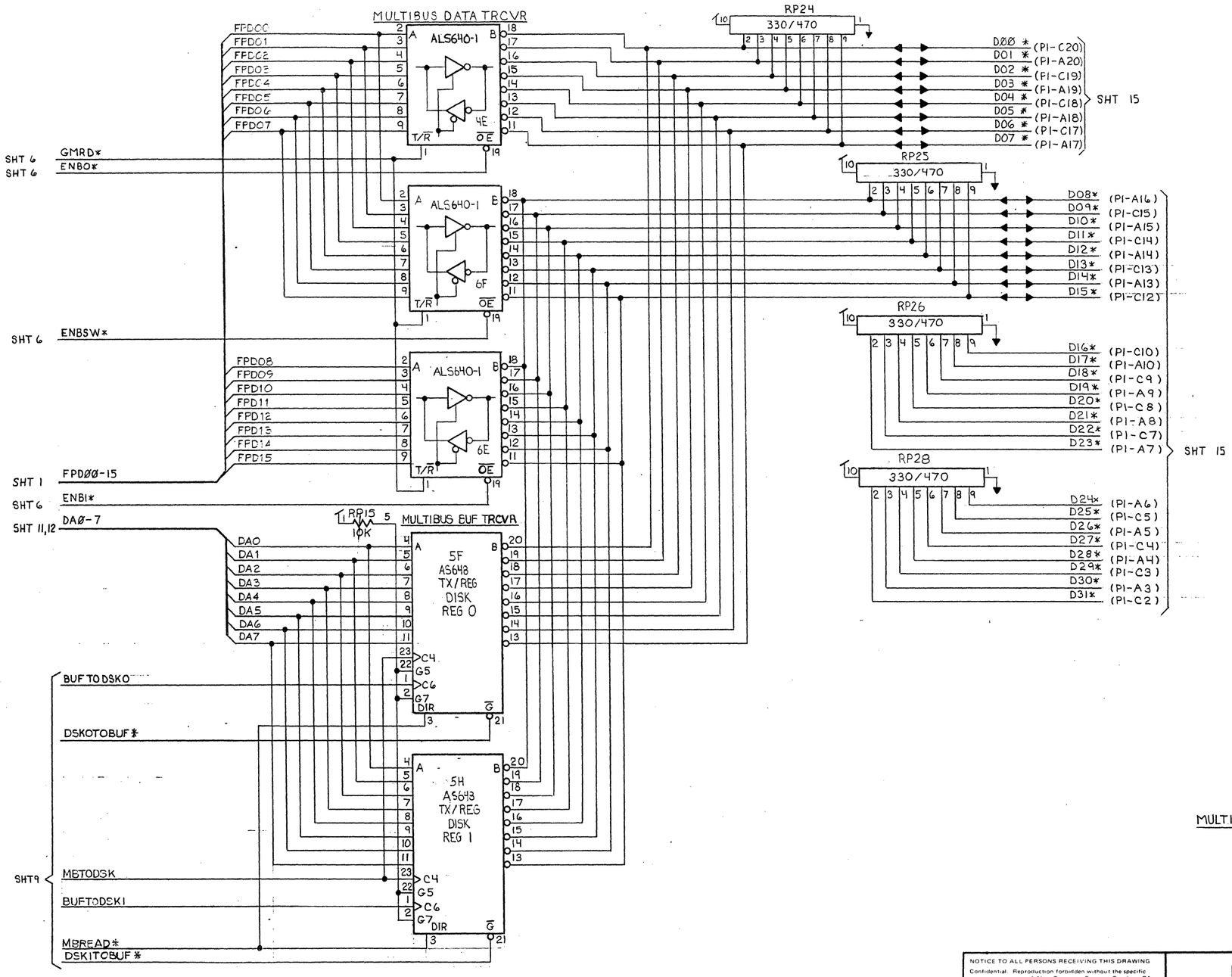


FILE PROCESSOR PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	625-15818-XXX	SH	7	REV	F

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



MULTIBUS INTERFACE

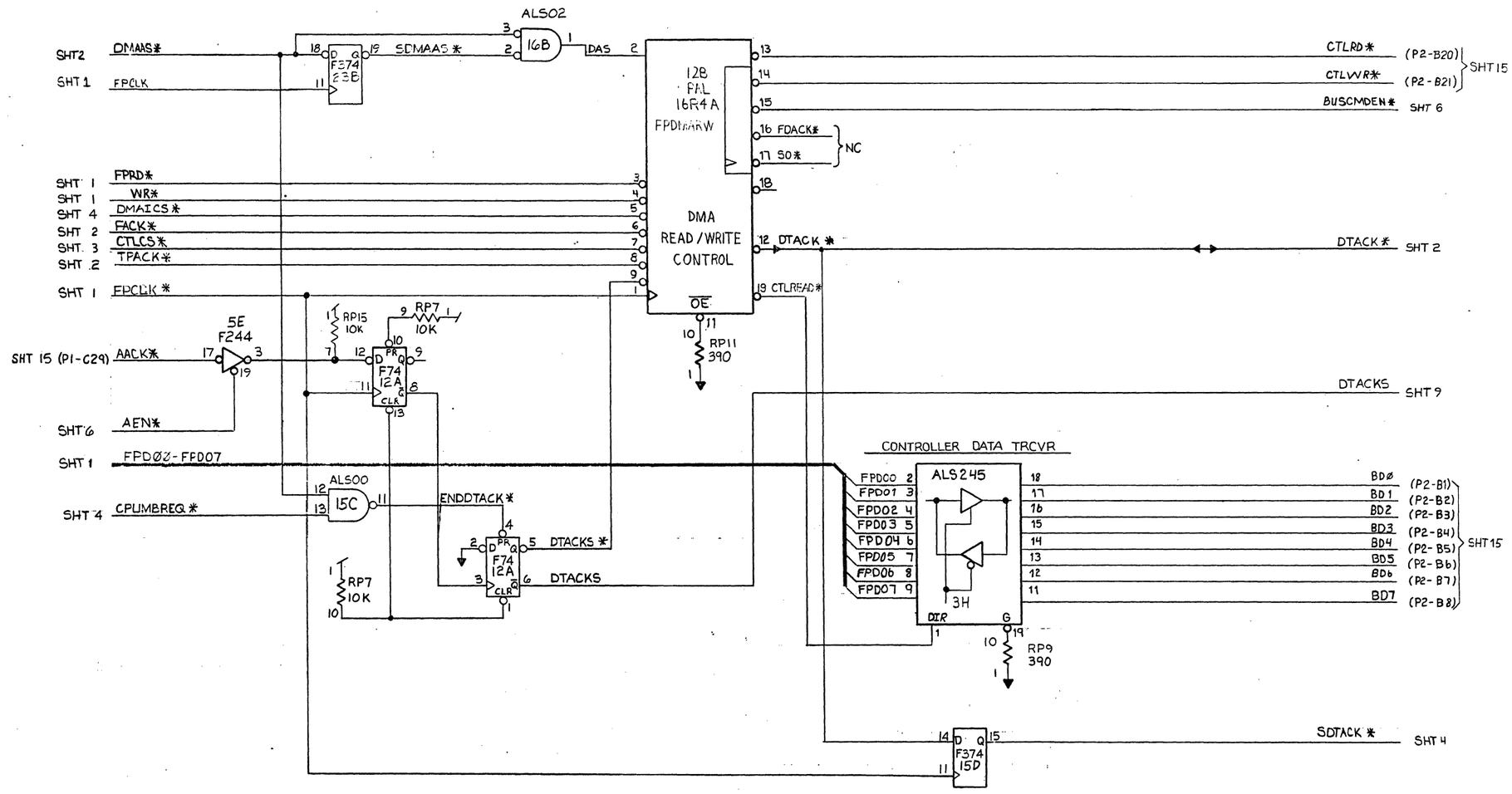
FILE PROCESSOR PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV
625-15818-XXX	8	F

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



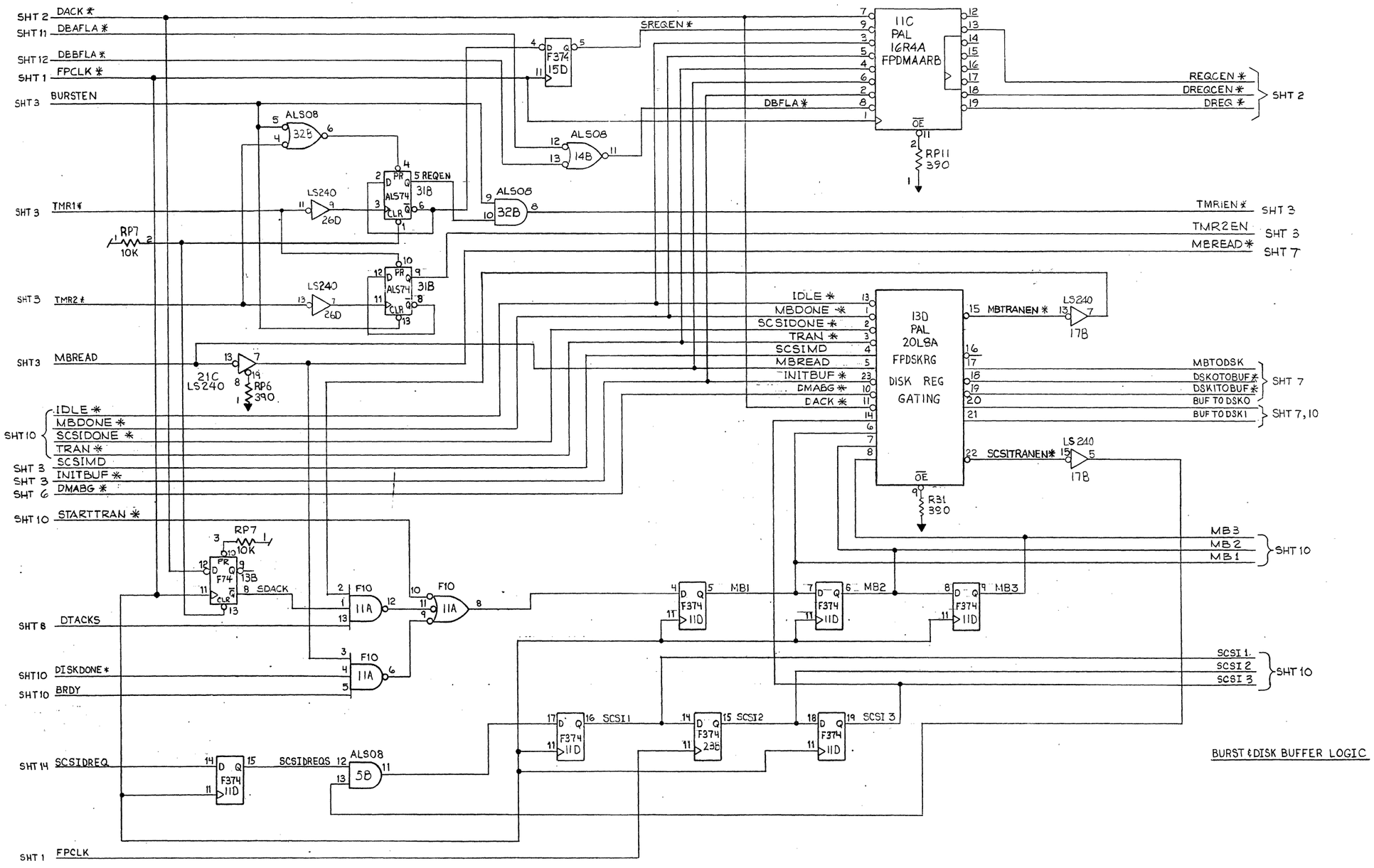
FILE PROCESSOR PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV
625-15818-XXX	9	F

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



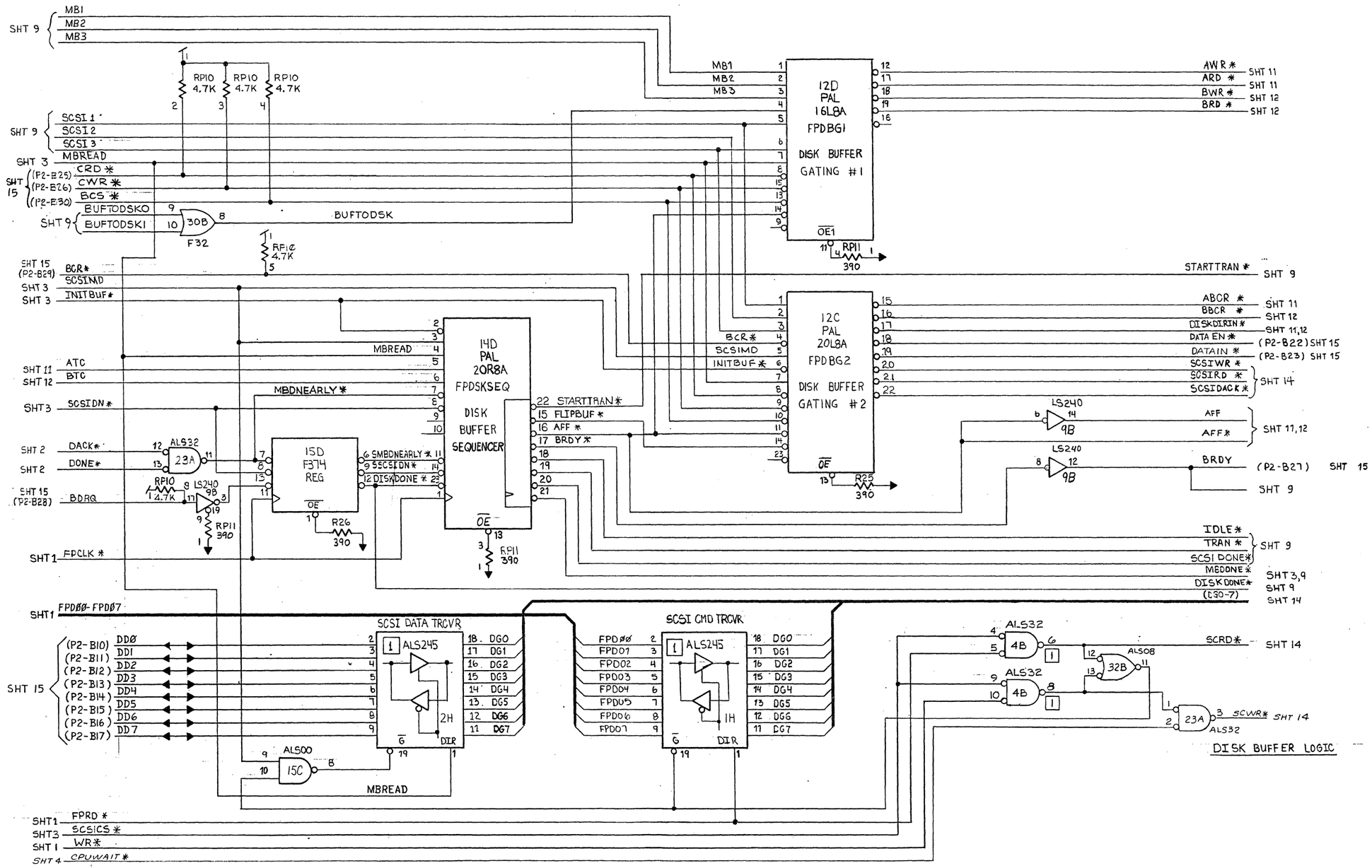
FILE PROCESSOR PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO. 625-15818-XXX	SH 10	REV F

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



FILE PROCESSOR PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV.
625-15818-XXX	11	F

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

1/2 "ping pong" buffer

SHT 7,12 DA0-7

HOST TRCVR A — ALS245 — 7D

DISK BUFFER A — 4D — 2015 RAM 2K X 8 120 NS

DISK TRCVR A — ALS245 — 5D

DD0 (P2-B10)
DD1 (P2-B11)
DD2 (P2-B12)
DD3 (P2-B13)
DD4 (P2-B14)
DD5 (P2-B15)
DD6 (P2-B16)
DD7 (P2-B17)
} SHT 15

SHT3 MBREAD
AFF

SHT10 AWR*
ARD*

DISKDIRIN*
AFF*

RP10 4.7K

SHT 3 BUFMDI
SHT 3 BUFMDO

ALS08 15B — 3 AINC*

SHT 10 ABCR*

3D ALS191 CTR — AC10 AC9 AC8

2D ALS161 CTR — AC7 AC6 AC5 AC4

1D ALS161 CTR — AC3 AC2 AC1 AC0

RP11 390

LS240 26D

RP6 390

ALS133 6B — 15D F374 — DBAFLA* SHT9

ATC SHT 10

ALS08 14B — ALS74 13A

SHT 1 FPCLK*

DISK BUFFER LOGIC

FILE PROCESSOR PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	G25-15818-XXX	SH	12	REV	F

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

s/a "ping pong" buffer

SHT 7,11 DA0-7

HOST TRCVR B — ALS245 9D

DA0 2, DA1 3, DA2 4, DA3 5, DA4 6, DA5 7, DA6 8, DA7 9 → DF0 18, DF1 17, DF2 16, DF3 15, DF4 14, DF5 13, DF6 12, DF7 11

DIR 1, OE 19

DISK BUFFER B

DF0 9, DF1 10, DF2 11, DF3 13, DF4 14, DF5 15, DF6 16, DF7 17

9C 2015 RAM 2K X 8 120NS

A10 19, A9 22, A8 23, A7 1, A6 2, A5 3, A4 4, A3 5, A2 6, A1 7, A0 8, WE 21, OE 20, CS 18

RP11 1 8 390

DISK TRCVR B — ALS245 6D

DF0 2, DF1 3, DF2 4, DF3 5, DF4 6, DF5 7, DF6 8, DF7 9 → DD0 18, DD1 17, DD2 16, DD3 15, DD4 14, DD5 13, DD6 12, DD7 11

DIR 1, OE 19

DD0 (P2-B10), DD1 (P2-B11), DD2 (P2-B12), DD3 (P2-B13), DD4 (P2-B14), DD5 (P2-B15), DD6 (P2-B16), DD7 (P2-B17) — SHT 15

SHT 3 MBREAD, AFF *

SHT 10 BWR *, BRD *

DISKDIRIN *, AFF

SHT 3 BUFMD1, BUFMD0

SHT 10 BBCR *

RP15 1 10K 6

ALS08 15B: 4, 5 → 6 BINC*

12C 8D ALS191 CTR: D3 9, D2 10, D1 1, D0 15, DN/UP 5, LD 11, G 14, CLK 4 → TC 12, Q3 7, Q2 6, Q1 2, Q0 3, RC 13 — BC10, BC9, BC8

15C 8C ALS161 CTR: D3 6, D2 5, D1 4, D0 3, LD 9, ENP 7, CLR 1, CLK 2 → TC 15, Q3 11, Q2 12, Q1 13, Q0 14 — BC7, BC6, BC5, BC4; ENT 10

15C 7C ALS161 CTR: D3 6, D2 5, D1 4, D0 3, LD 9, ENP 7, CLR 1, CLK 2 → TC 15, Q3 11, Q2 12, Q1 13, Q0 14 — BC3, BC2, BC1, BC0; ENT 10

LS240 26D: 15 → 5

ALS08 14B: 4, 5 → 6

ALS74 13A: D 12, PR 10, CLK 11, CLR 13 → Q 9, Q̄ 8

ALS133 8B: 15, 5, 6, 7, 10, 11, 12, 13, 14, 1, 2, 3, 4 → 9

11D F374: D 13, CLK 11 → Q 12

DBBFLA* SHT 9

BTC SHT 10

SHT 1 FPCLK*

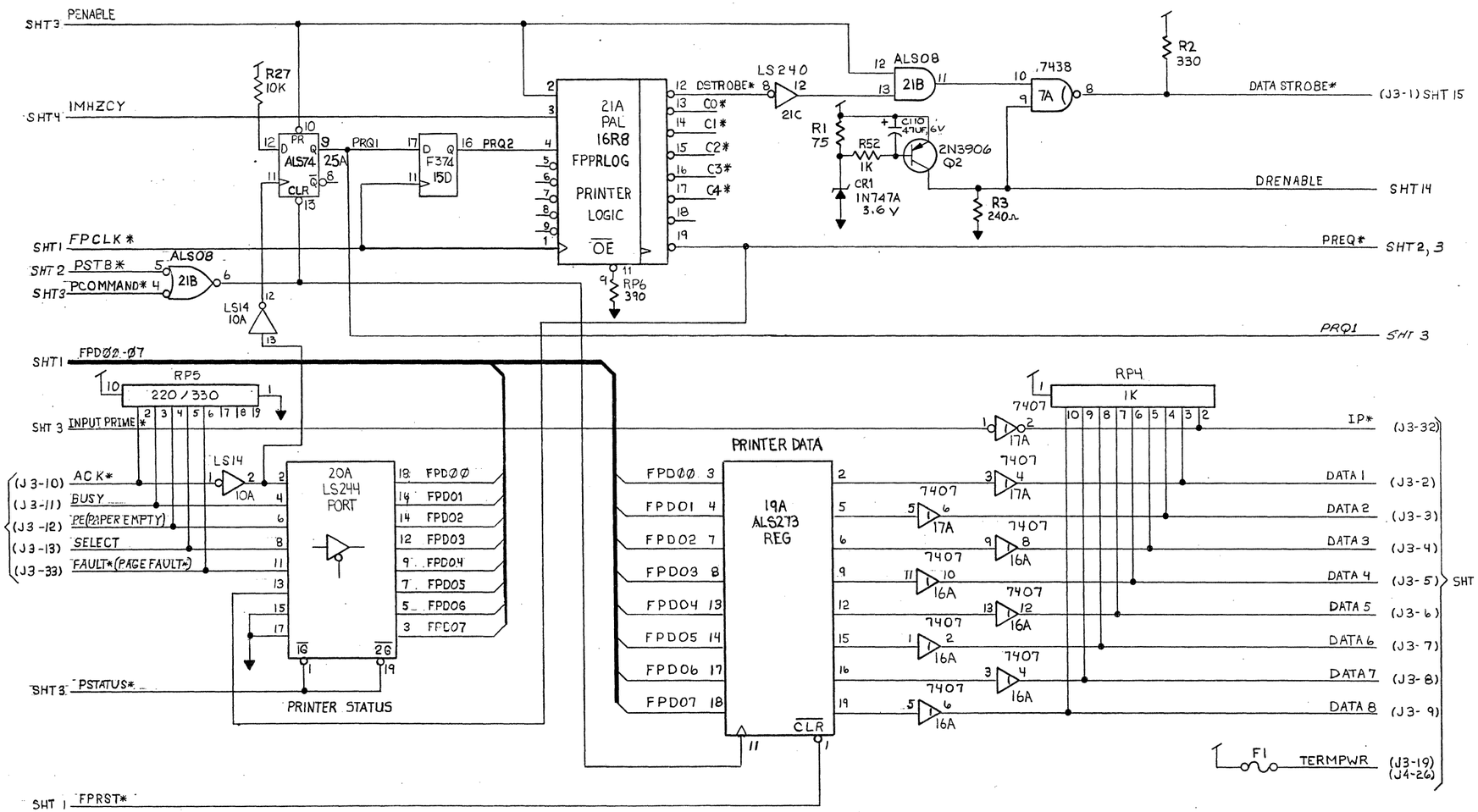
DISK BUFFER LOGIC

FILE PROCESSOR PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS®

DWG. NO.	SH.	REV
625-15818-XXX	13	F

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



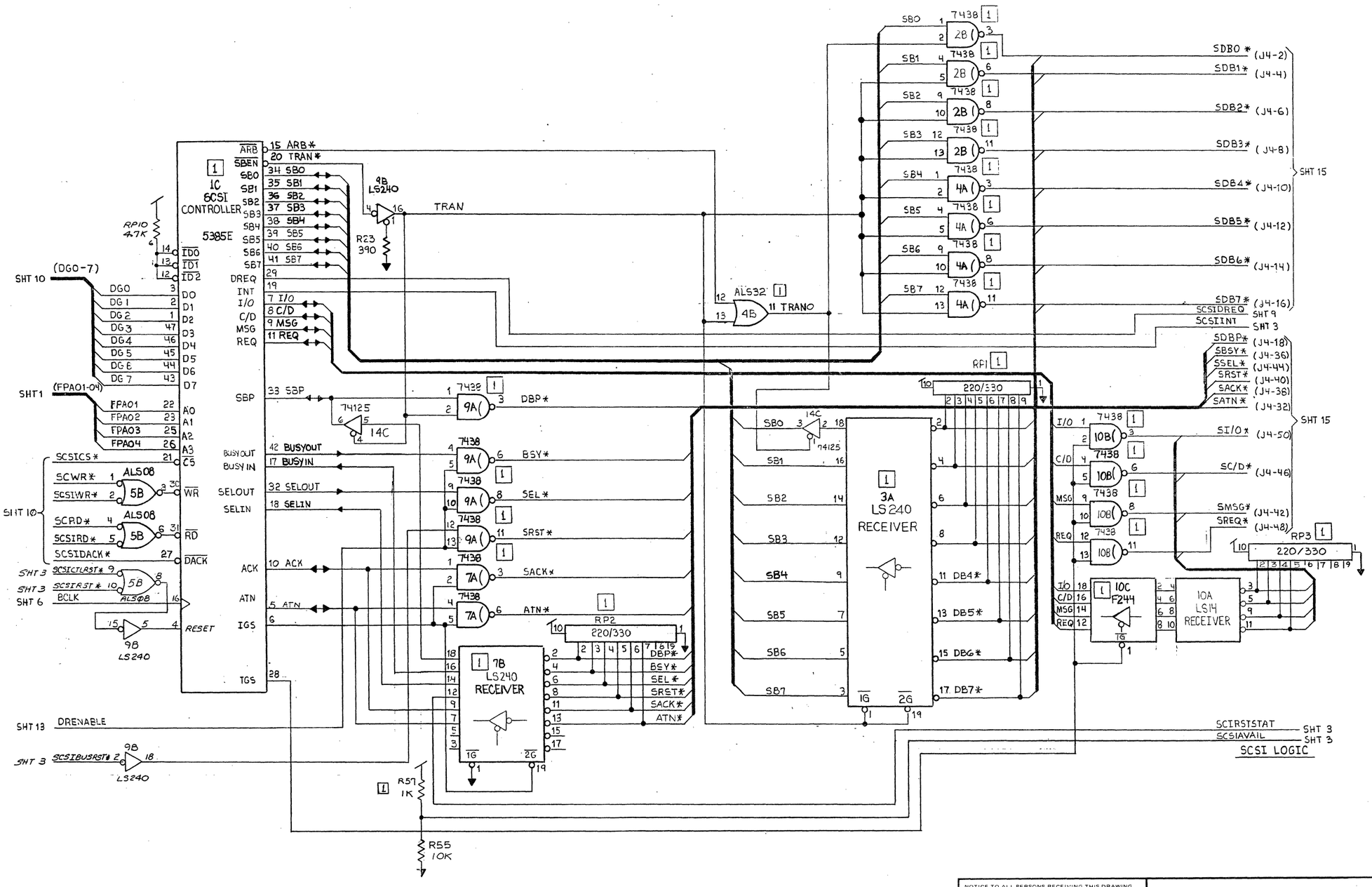
PRINTER LOGIC

FILE PROCESSOR PCB SCHEMATIC PIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV
625-15818-XXX	14	F

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

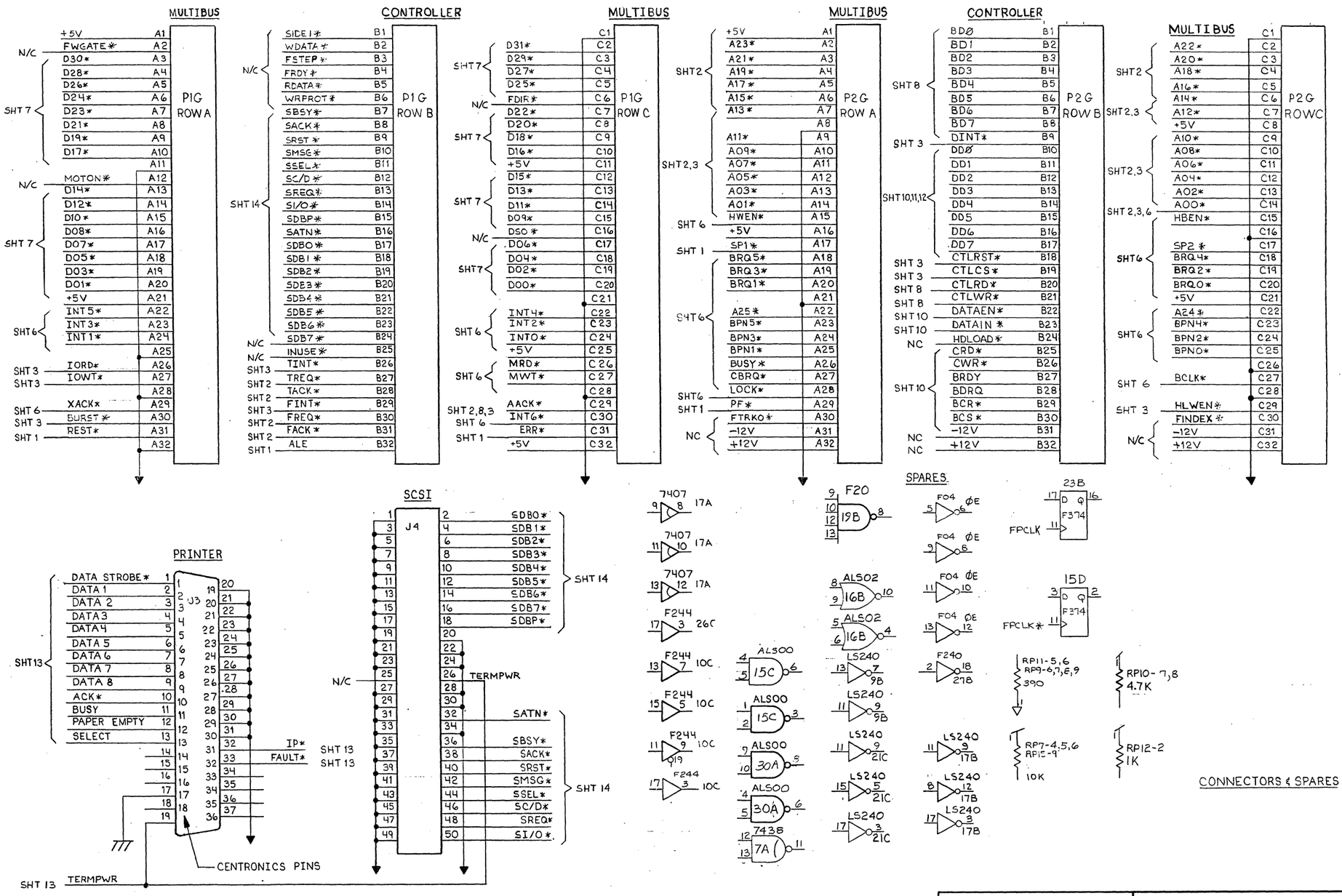


FILE PROCESSOR PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV.
625-15818-XXX	15	E

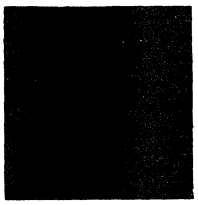
REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED



FILE PROCESSOR PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

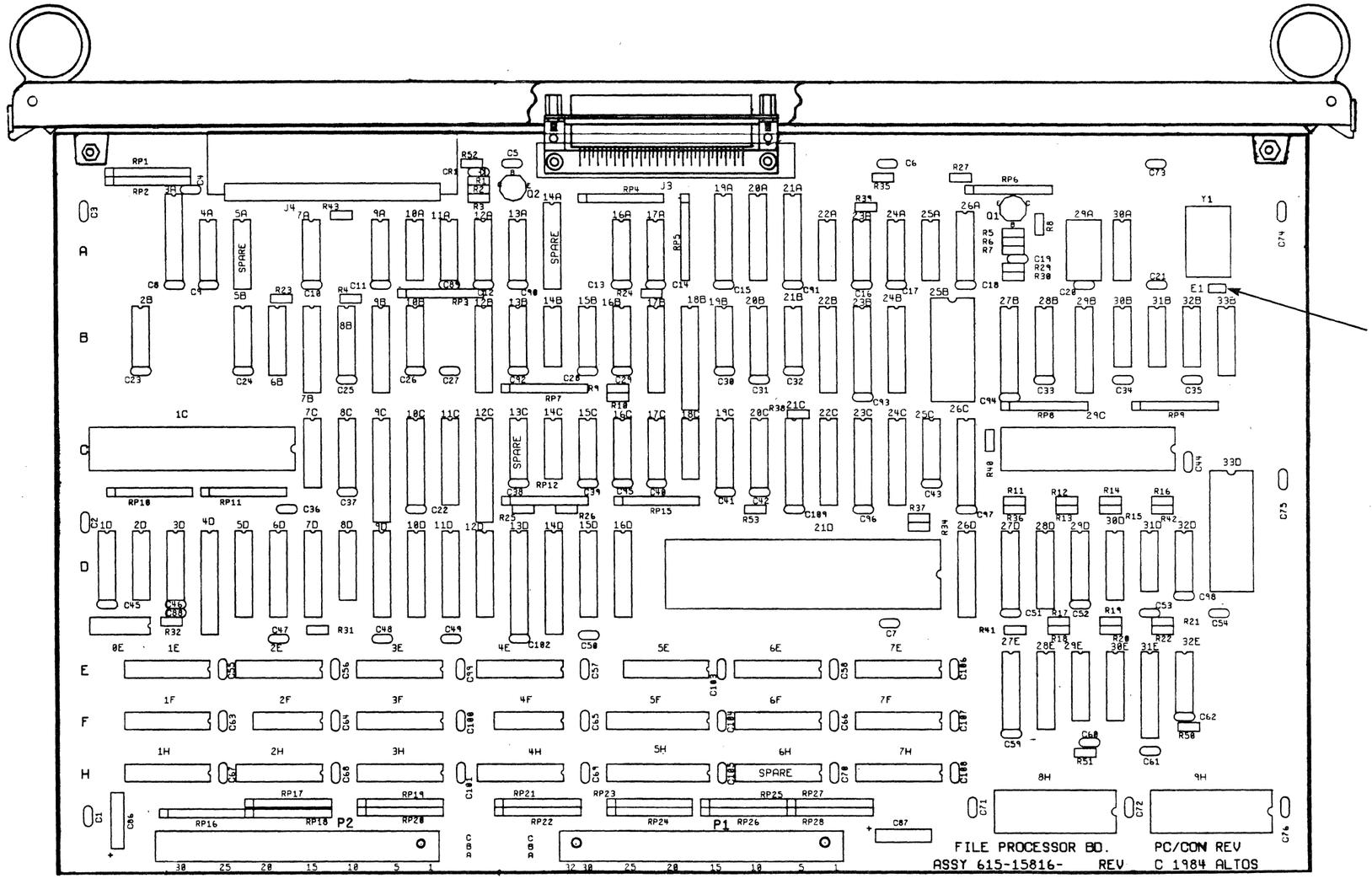
FILE PROCESSOR PCB PART LOCATIONS



DWG. NO. 615-15816-XXX	SH 1	REV F

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	X1A	PROTOTYPE	9-27-84	
	X2A	PROTOTYPE	12-3-84	
	X3A	PROTOTYPE	8-15-85	
	3A	PRE-PRODUCTION EO# 2900	3-1-85	
	4A	REVISED PER EO# 2924	3-20-85	
	5A	REVISED PER EO# 2980-H	4-19-85	
	6A	REVISED PER EO# 3069-H	7-5-85	
	7A	REVISED PER EO # 3165-H	7-29-85	
	8A	EO 3326 (CANCELLED)	7-25-85	
	9A	EO 3420	7-25-85	



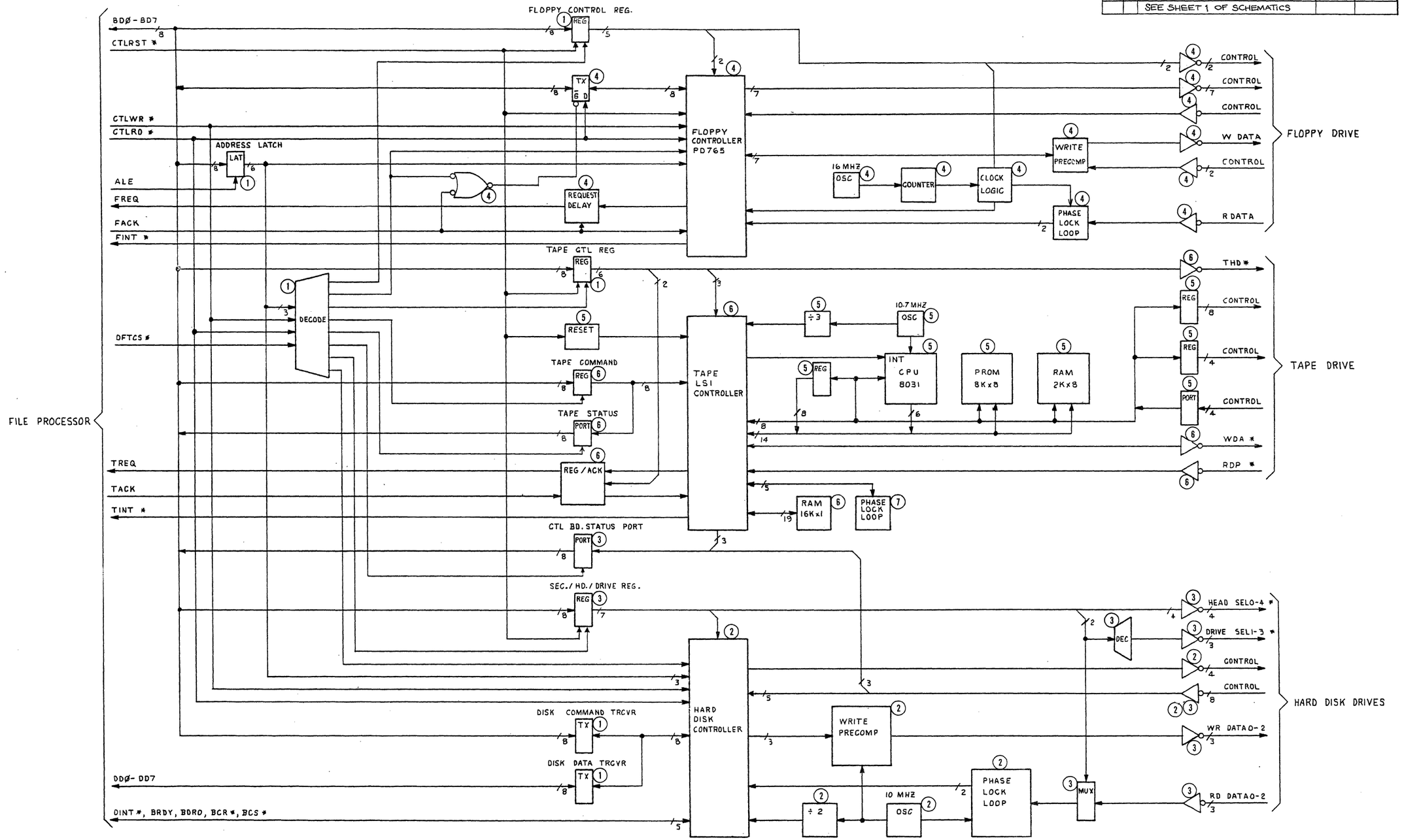
FILE PROCESSOR PCB PART LOCATIONS

ALTOS COMPUTER SYSTEMS

CONTROLLER PCB BLOCK DIAGRAM

DWG. NO. 625-15292-001	SH B.D.	REV L

REVISIONS				
REV.	ZONE	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1 OF SCHEMATICS		



CONTROLLER PCB BLOCK DIAGRAM

ALTOS COMPUTER SYSTEMS

SHEET 1 OF 1

CONTROLLER PCB SCHEMATIC DIAGRAMS

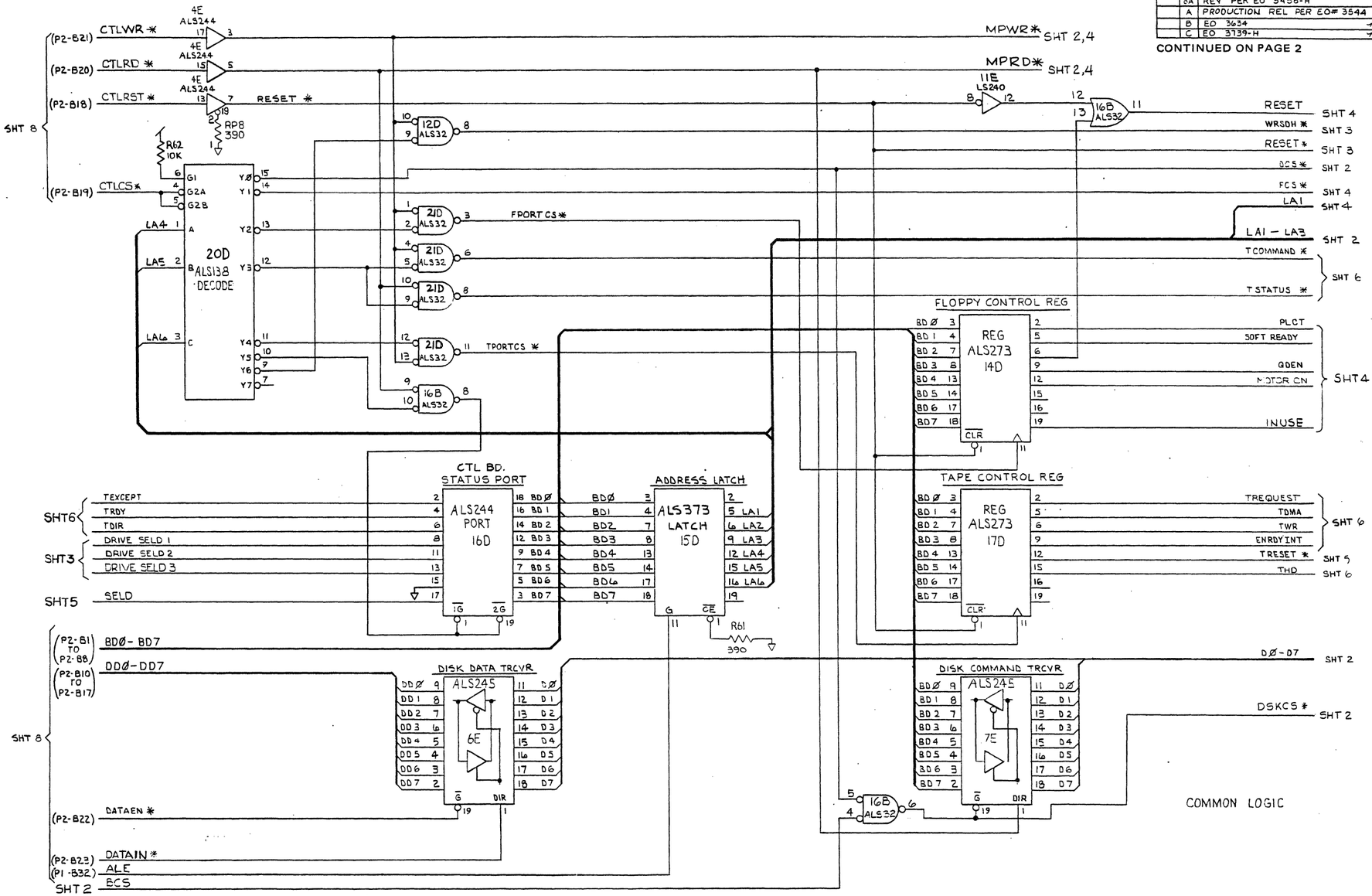
11

DWG. NO.	SH	RFV
625-15292-001	1	L

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	X4A	PROTOTYPE	2-12-85	
	4A	PRE-PRODUCTION EO# 2900	3-1-85	
	5A	INCORP PER EO 2923	3-19-85	
	6A	REVISED PER EO# 3068	25 APR 85	
	7A	CHNG 2IC TO 2704-2 (SHT 5) EO # 3174-H	6.10.85	
	8A	REV PER EO 3458-H	9-19-86	
	A	PRODUCTION REL PER EO# 3544	9-19-85	
	B	EO 3634	3 JAN 86	
	C	EO 3739-H	3 JAN 86	

CONTINUED ON PAGE 2



NOTES:
1. ADD JUMPER PLUGS TO E3, E4, E5 AND E8.
2. COMPONENTS NOT INSTALLED.

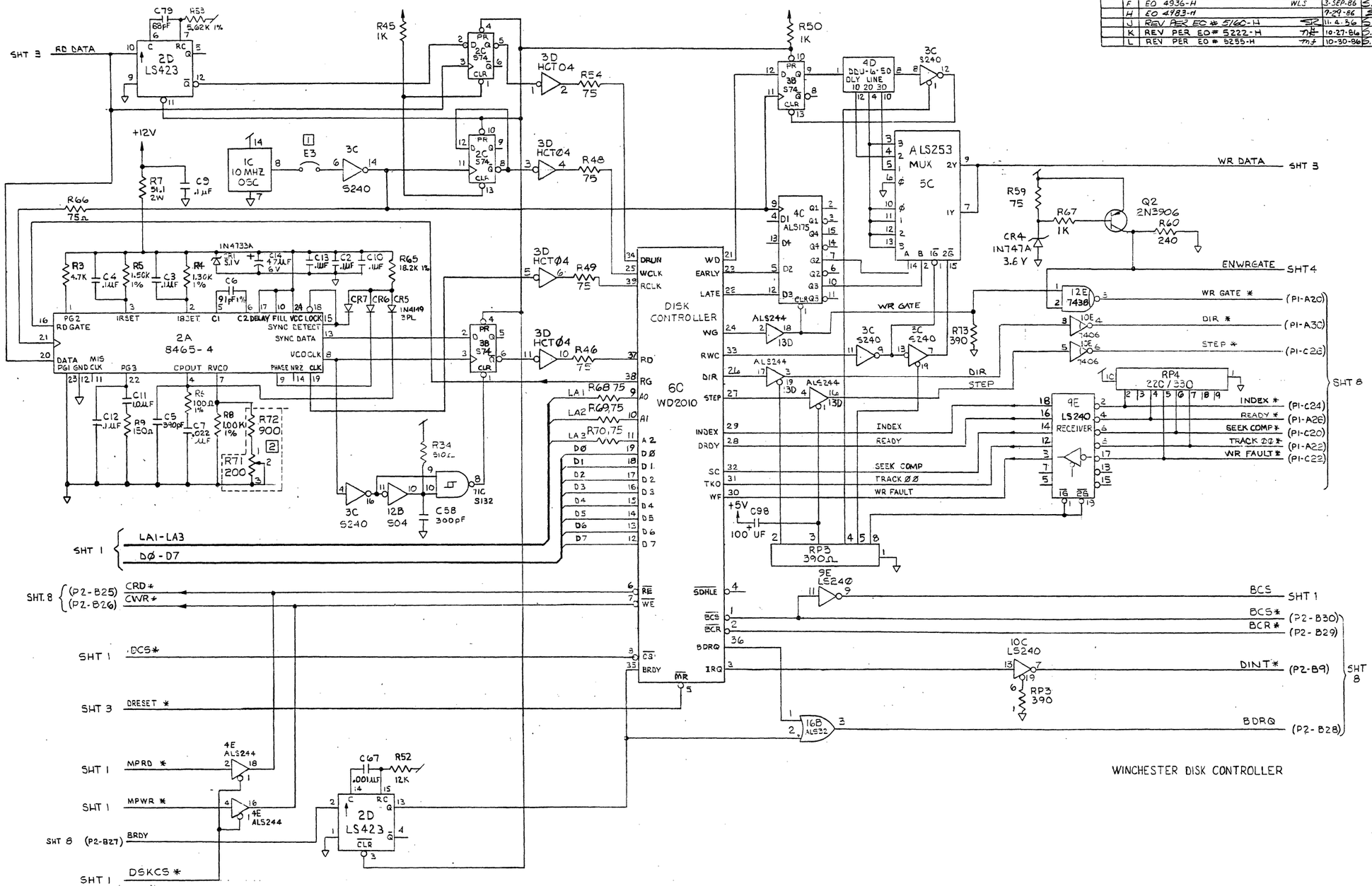
CONTROLLER PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH.	REV
625-15292-001	2	L

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	D	EO 4150-H mf	5-1-86	
	E	EO 4298-H mf	5-1-86	
	F	EO 4936-H WLS	3-SEP-86	
	H	EO 4983-H	9-29-86	
	J	REV PER EO # 5160-H	11.4.86	
	K	REV PER EO # 5222-H mf	10-27-86	
	L	REV PER EO # 5255-H mf	10-30-86	



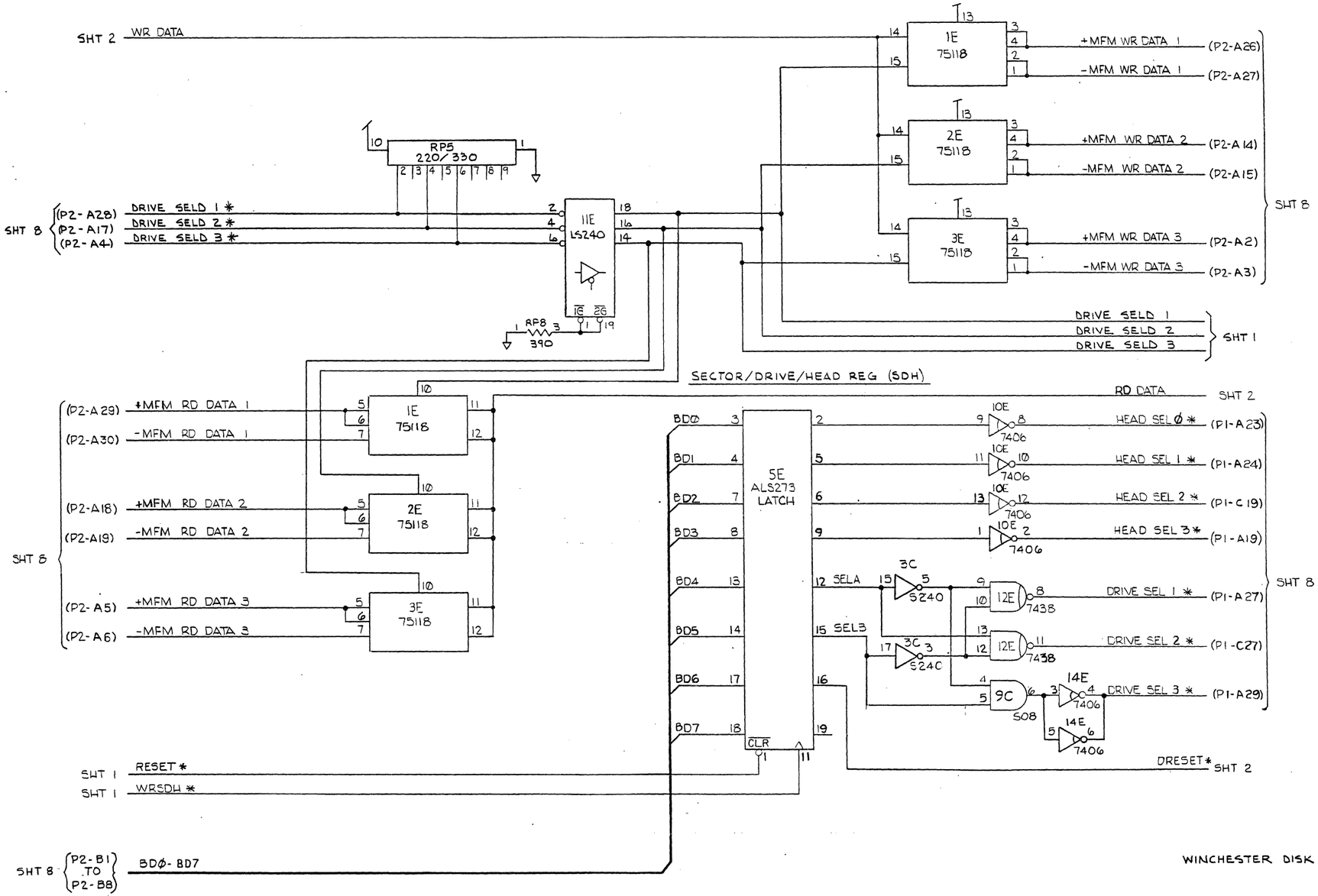
WINCHESTER DISK CONTROLLER

CONTROLLER PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH.	REV
625-15292-001	3	L

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



WINCHESTER DISK CONTROLLER

CONTROLLER PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV
625-15292-001	4	L

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

SHT 1 SOFT READY

SHT 8 (P2-81 TO P2-88) BD0 - BD7

ALS245 8E

PD765 FLOPPY CONTROLLER 8C

FINT

HDLOAD NC

HD SEL

US1

STEP

SEEK

LCTDIR

READY

WP/TWO SD

FAULT/TR0

WRDATA

PS0

WREN

PS1

VCO

RD-DATA

INDEX

RD DWIN

WRCLK

US0

MFM

SHT 1: FCS *, MPWR *, MPRD *, RESET, LA1

SHT 8 (P1-B30) FREQ *

R2 1K

SHT 6: 1 MHZ

SHT 1: PLCT

R1 1K

FACK *

SHT 8 P1-B31

R40 1K

ALS161 8B CTR: 250 KHZ, 500 KHZ

ALS161 7B CTR: 1 MHZ, 4 MHZ, 8 MHZ

OSC 16MHZ 6B

16 MHZ

ALS153 9B MUX: 7 MCLK, 9 FDCLK

ALS153 6A MUX: 7 SEQCLK

ALS32 12D

11D ALS08

LS240 10C: LOW SPEED

LS240 11E: FINT (P1-B29) SHT 8

FSTEP

FDIR

WPTS

FLTTR0

ALS175 4A

9C S08

10D PAL16R4A WCMP PAL

NC

FWRCLK

R58 390

F READY

INDEX

WRPROT

TRK00

R DATA

15E LS240 RECEIVER

FRD DATA

RP8 390

13E 7406: HD LOAD * (P1-A17), SIDE 1 * (P1-A12), DS1 * (P1-B15), DS0 * (P1-C15), F STEP * (P1-A14)

14E 7406: F DIR * (P1-B14), W DATA * (P1-C13), MOTOR ON * (P1-C14), INUSE * (P1-C16)

7438 12E: FWRGATE * (P1-B13)

RP6 150Ω

15E LS240 RECEIVER: FREADY * P1-B11, FINDEX * P1-A18, WRPROT * P1-C12, FTRK00 * P1-A13, RDATA * P1-B12

SHT 8

MCA3, MCA2, MCA1, MCA0

3283 PROM DRCV 4B

5B S174 REG

R39 390

R39 10K

ALS08 11D

LS240 15E

FRD DATA *

FLOPPY CONTROLLER

5A ALS74: RDATAP, RDATAP *

5A ALS74: FRDWIN

SHT 1: Q DEN, MOTOR ON, INUSE

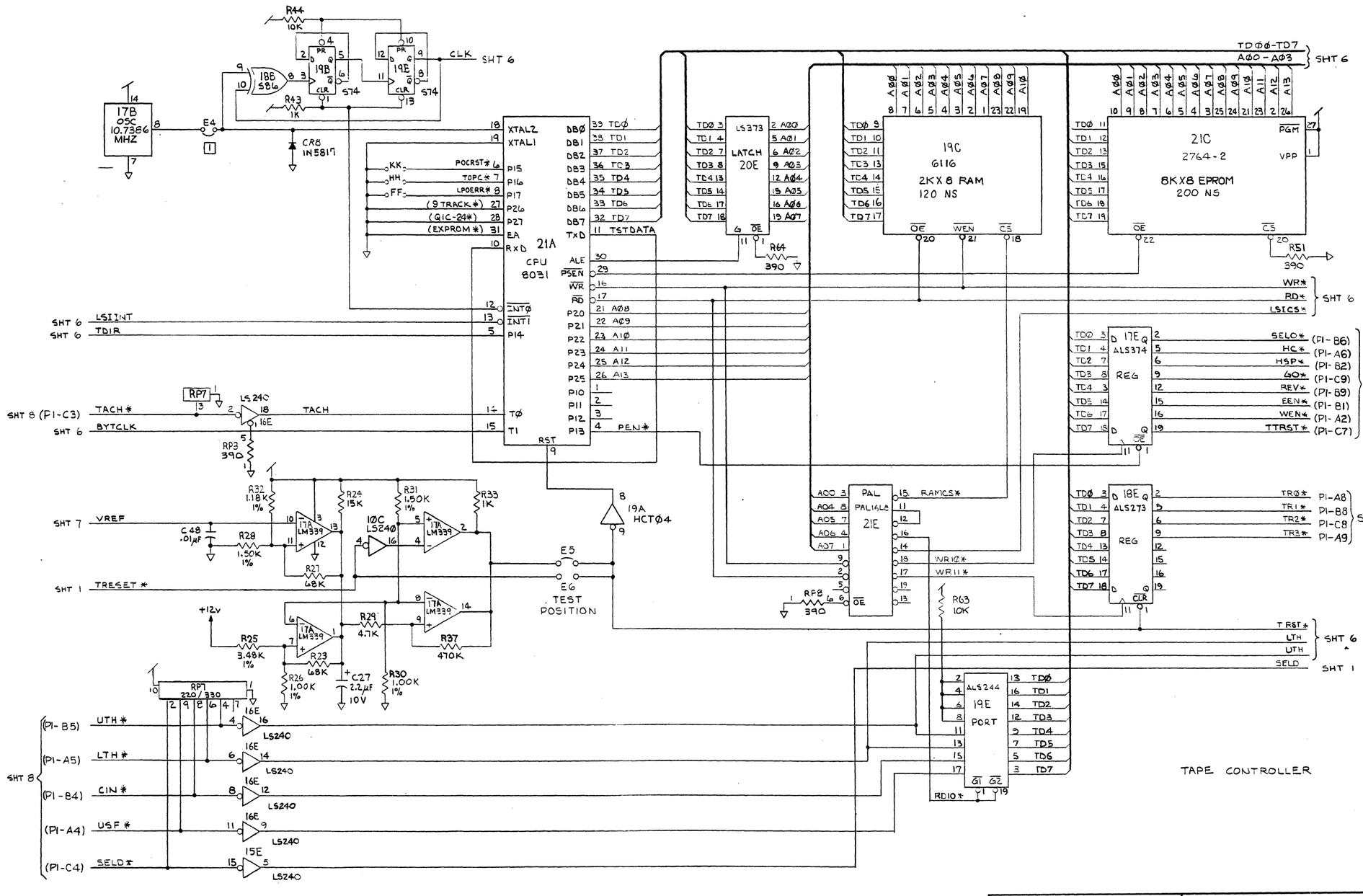
SHT 2: ENWRGATE

CONTROLLER PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH.	REV
625-15292-001	5	L

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



CONTROLLER PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH	REV.
625-15292-001	6	L

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

SHT 1 THC

R56 1K

18B S86

THD* (P1-C2) SHT8

SHT 8 (P1-C 5) RDP*

RP7 5 1

16E LS240

SHT 7 { READ DATA, READ CLOCK

SHT 5 { LTH, UTH, LSICS*, WR*, RD*, TRST*, CLK

A00-A03

TD0-TD7

SHT 8 { P2-B1 TO P2-B8 } BD0-BD7

TAPE STATUS

TAPE COMMAND

19D REG ALS374

PORT ALS244 18D

SHT 8 (P1-B28) TACK*, TCOMMAND*, TSTATUS*, TREQUEST

15C ALS08

LS240 10C

12C S00

SHT 1 TDMA, TWR, ENRDYINT

18B S86

11C S132

LS240 10C

15C ALS08

SHT 4 1MHZ

END*

XFER

RP3 390

R47 10K

R55 10K

RP8 390

68

170 LSI CONTROLLER 2,3D

RDP, RDATA, RCLK, LTH, UTH, CS, WR, RD, RST, CLK, A00-A03, TD0-TD7, PARITY, REQ, ONL, XFER, HB0-HB7, VSS

LOCK*, REF*, MARGIN, INT, WCLK/IO

RAMIN, RAMOUT, WE, RA0-RA14

16C 2167 RAM 16K x 1 70 NS

DIN, DOUT, WE, A0-A13, CS

LOCK*, REF*, MARGIN SHT 7

LSIINT SHT 5

BYTCLK SHT 5, 7

WD, WD

LS240 16E

WDA* (P1-B3) SHT8

WDA (P1-A3)

EXCEPT, RDY, RDYHBUS, DIR, UNITEN, ACK

ALS244

TEXCEPT, TRDY SHT1

TINT* P1-B26 SHT8

TDIR SHT 1, 5

ACK

TREQ* (P1-B27) SHT8

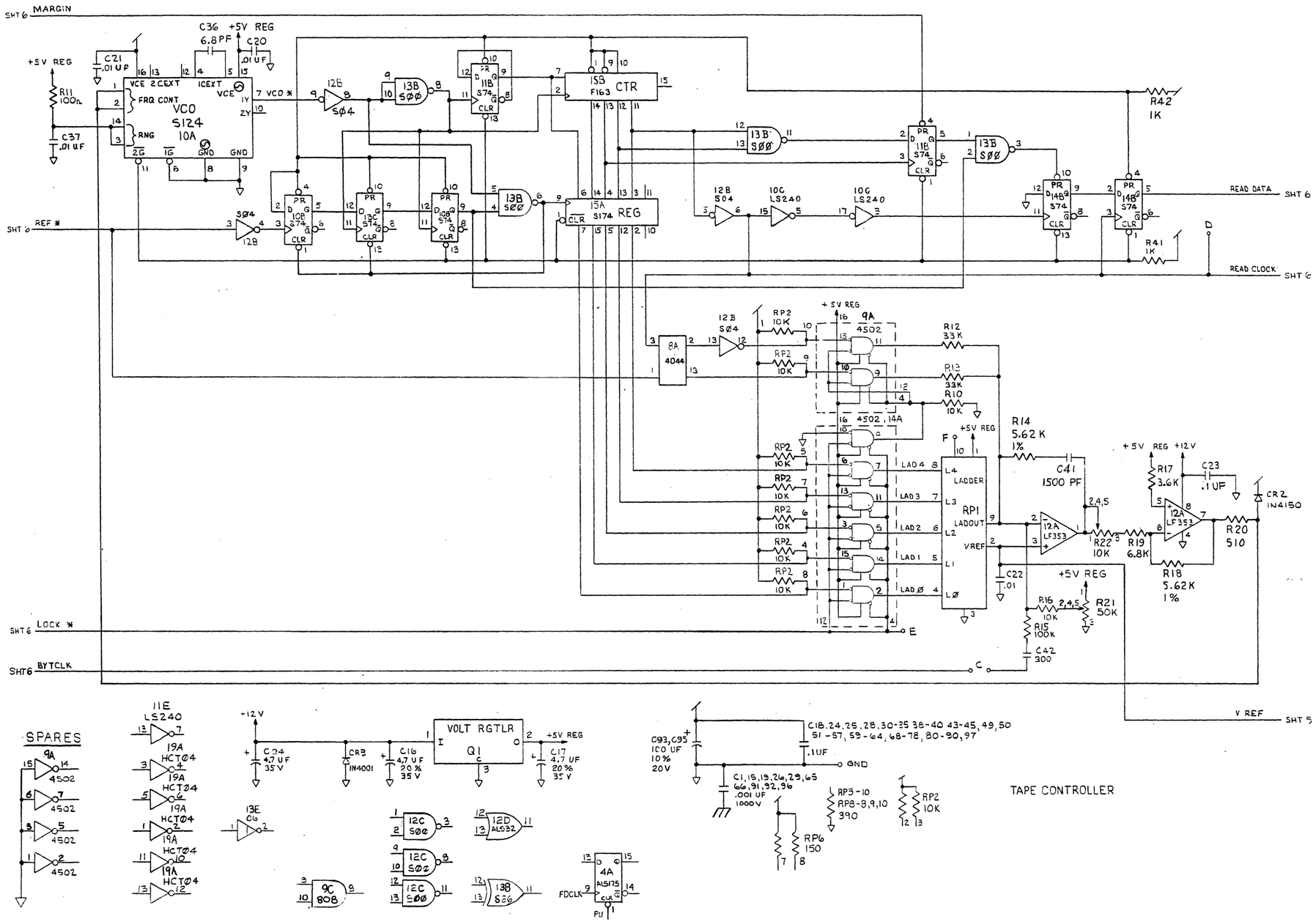
TAPE CONTROLLER

CONTROLLER PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO.	SH.	REV
625-15292-001	7	L

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

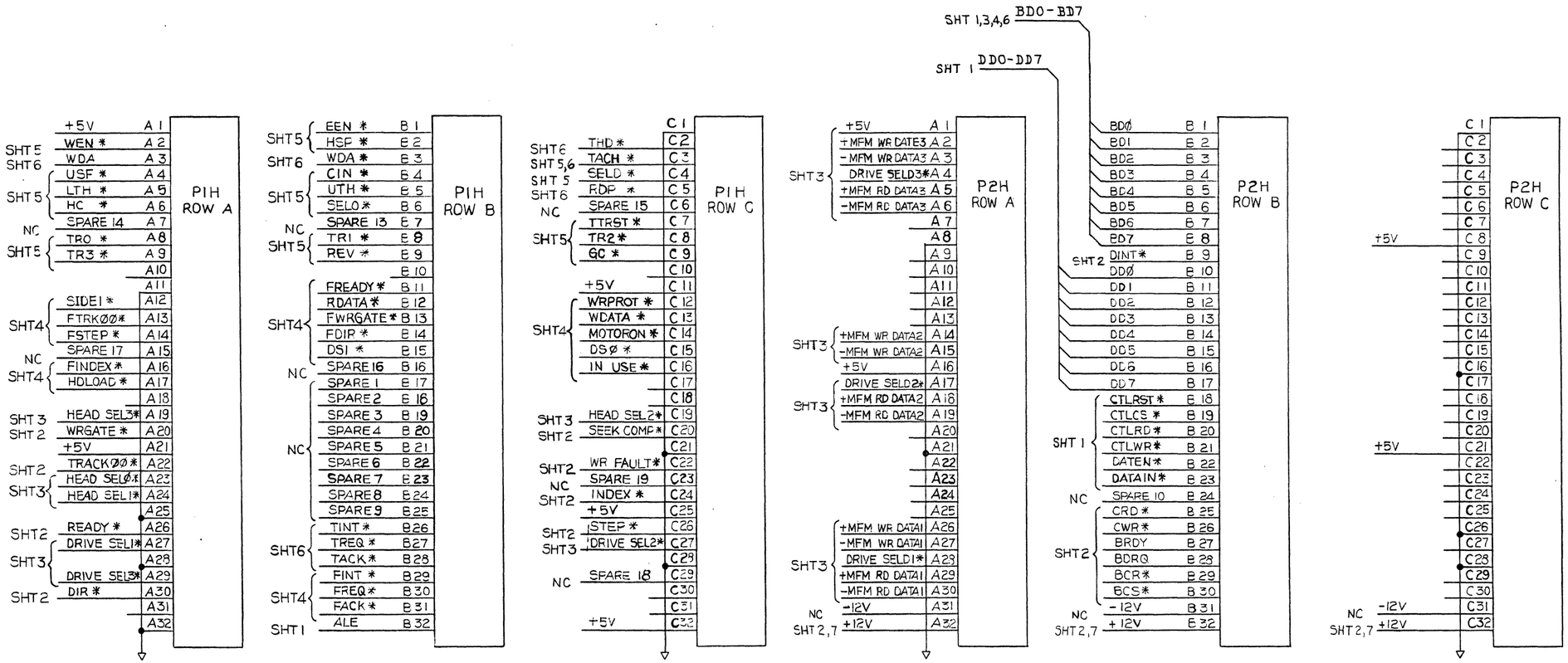


CONTROLLER PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

DWG. NO. 625-15292-001	SH 8	REV. L

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		



CONTROLLER PCB SCHEMATIC DIAGRAM

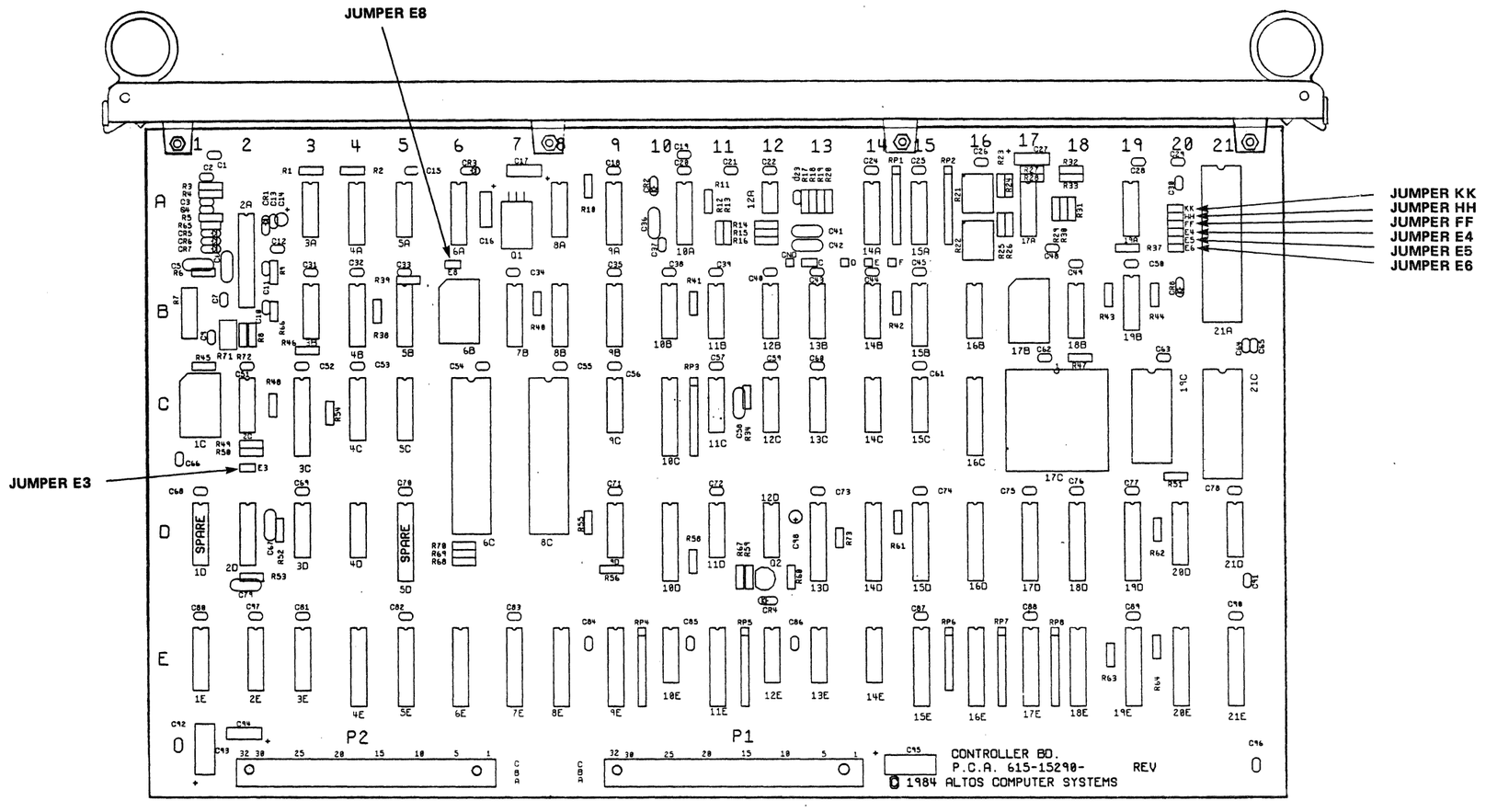
ALTOS COMPUTER SYSTEMS

CONTROLLER PCB PART LOCATIONS

DWG. NO.	SH	REV.
615-15290-001 609-15290-001	1	P

REVISIONS

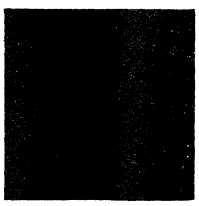
ZONE	REV.	DESCRIPTION		DATE	APPROVED
	X1A	PROTOTYPE			
	X2A	PROTOTYPE		10-17-84	
	X4A	PROTOTYPE		1-15-85	
	4A	PRE-PRODUCTION EO #2900		5-1-85	
	5A	REVISED PER EO # 2923		5-19-85	
	6A	REVISED PER EO # 3068-H		25 APR 85	
	7A	REVISED PER EO # 3165-H		13 MAY 85	
	8A	REVISED PER EO # 3174-H		6-10-85	
	9A	REVISED PER EO # 3349		17 JUL 85	
	10A	REVISED PER EO # 3458-H		9-19-85	
	A	PRODUCTION RELEASED PER EO # 3544		9-19-85	
	B	EO # 3739-H	mm	3 JAN 86	
	C	EO # 4139-H	c.k	14 MAR 86	
	D	EO 4298-H	mj	5-1-86	
	E	EO # 4478-H	ck	19 MAY 86	
	F	REVISED PER EO 4230-H		9.22.86	
	H	REVISED PER EO 4936-H	L.S.	9.3.86	
	J	REV PER EO # 4983-H		9.29.86	
	K	REV PER EO # 4914-H	mj	9.22.86	
	L	REV PER EO # 5113-H		10-16-86	
	M	REV PER EO # 5160-H		10.27.86	
	N	REV PER EO # 5222-H		10-27-86	
	P	REV PER EO # 5255-H	mj	10-30-86	



CONTROLLER PCB PART LOCATIONS

ALTOS COMPUTER SYSTEMS

BACKPLANE PCB SCHEMATIC DIAGRAM



DWG. NO.	SH	REV.
625-15102-001	1	A

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	B	ECO 3288	10-JAN-85	
	1AA	PROTO	6-25-85	
	AA	PRE-PRODUCTION ECO# 2600	7-1-85	
	5A	ECO# 2983-H	7-17-85	
	A	ANCO. REL. ECO 3544-H	8-27-85	

XMB
J1A-J1F

+5V	A1		A1
(DP3*)	A2		A2
D30*	A3		A3
D28*	A4		A4
D26*	A5		A5
D24*	A6		A6
D23*	A7		A7
D21*	A8		A8
D19*	A9		A9
D17*	A10		A10
	A11		A11
(DP1*)	A12		A12
D14*	A13		A13
D12*	A14		A14
D10*	A15		A15
D08*	A16		A16
D07*	A17		A17
D05*	A18		A18
D03*	A19		A19
D01*	A20		A20
+5V	A21		A21
INT5*	A22		A22
INT3*	A23		A23
INT1*	A24		A24
	A25		A25
IORD*	A26		A26
IOWT*	A27		A27
	A28		A28
XACK*	A29		A29
SP1	A30		A30
REST*	A31		A31
	A32		A32
N/C	B1	N/C	B1
N/C	B2	N/C	B2
N/C	B3	N/C	B3
N/C	B4	N/C	B4
N/C	B5	N/C	B5
N/C	B6	N/C	B6
N/C	B7	N/C	B7
N/C	B8	N/C	B8
N/C	B9	N/C	B9
N/C	B10	N/C	B10
N/C	B11	N/C	B11
N/C	B12	N/C	B12
N/C	B13	N/C	B13
N/C	B14	N/C	B14
N/C	B15	N/C	B15
N/C	B16	N/C	B16
N/C	B17	SP3	B17
N/C	B18	SP4	B18
N/C	B19	SP5	B19
N/C	B20	SP6	B20
N/C	B21	SP7	B21
N/C	B22	SP8	B22
N/C	B23	SP9	B23
N/C	B24	SP10	B24
N/C	B25	SP11	B25
N/C	B26	TINT*	B26
N/C	B27	TREQ*	B27
N/C	B28	TACK*	B28
N/C	B29	FINT*	B29
N/C	B30	FREQ*	B30
N/C	B31	FACK*	B31
N/C	B32	ALE	B32
	C1		C1
D31*	C2		C2
D29*	C3		C3
D27*	C4		C4
D25*	C5		C5
(D32*)	C6		C6
D22*	C7		C7
D20*	C8		C8
D18*	C9		C9
D16*	C10		C10
+5V	C11		C11
D15*	C12		C12
D13*	C13		C13
D11*	C14		C14
(DP0*)	C15		C15
D09*	C16		C16
D06*	C17		C17
D04*	C18		C18
D02*	C19		C19
D00*	C20		C20
	C21		C21
INT4*	C22		C22
INT2*	C23		C23
INT0*	C24		C24
+5V	C25		C25
MRD*	C26		C26
MWT*	C27		C27
	C28		C28
AACK*	C29		C29
INT6*	C30		C30
ERR*	C31		C31
+5V	C32		C32

XMB
J1G

	A1		A1
	A2		A2
	A3		A3
	A4		A4
	A5		A5
	A6		A6
	A7		A7
	A8		A8
	A9		A9
	A10		A10
	A11		A11
	A12		A12
	A13		A13
	A14		A14
	A15		A15
	A16		A16
	A17		A17
	A18		A18
	A19		A19
	A20		A20
	A21		A21
	A22		A22
	A23		A23
	A24		A24
	A25		A25
	A26		A26
	A27		A27
	A28		A28
	A29		A29
	A30		A30
	A31		A31
	A32		A32
N/C	B1	N/C	B1
N/C	B2	N/C	B2
N/C	B3	N/C	B3
N/C	B4	N/C	B4
N/C	B5	N/C	B5
N/C	B6	N/C	B6
N/C	B7	N/C	B7
N/C	B8	N/C	B8
N/C	B9	N/C	B9
N/C	B10	N/C	B10
N/C	B11	N/C	B11
N/C	B12	N/C	B12
N/C	B13	N/C	B13
N/C	B14	N/C	B14
N/C	B15	N/C	B15
N/C	B16	N/C	B16
N/C	B17	N/C	B17
N/C	B18	N/C	B18
N/C	B19	N/C	B19
N/C	B20	N/C	B20
N/C	B21	N/C	B21
N/C	B22	N/C	B22
N/C	B23	N/C	B23
N/C	B24	N/C	B24
N/C	B25	N/C	B25
N/C	B26	N/C	B26
N/C	B27	N/C	B27
N/C	B28	N/C	B28
N/C	B29	N/C	B29
N/C	B30	N/C	B30
N/C	B31	N/C	B31
N/C	B32	N/C	B32
	C1		C1
	C2		C2
	C3		C3
	C4		C4
	C5		C5
	C6		C6
	C7		C7
	C8		C8
	C9		C9
	C10		C10
	C11		C11
	C12		C12
	C13		C13
	C14		C14
	C15		C15
	C16		C16
	C17		C17
	C18		C18
	C19		C19
	C20		C20
	C21		C21
	C22		C22
	C23		C23
	C24		C24
	C25		C25
	C26		C26
	C27		C27
	C28		C28
	C29		C29
	C30		C30
	C31		C31
	C32		C32

CONTR
J1H

+5V	A1		A1
WEN*	A2		A2
WDA	A3		A3
USF*	A4		A4
LTH*	A5		A5
HC*	A6		A6
SP14	A7		A7
TRO*	A8		A8
TR3*	A9		A9
N/C	A10		A10
	A11		A11
SIDE1*	A12		A12
FTRKO*	A13		A13
FSTEP*	A14		A14
SP17	A15		A15
FINDEX*	A16		A16
HDLOAD*	A17		A17
N/C	A18		A18
HDSEL3*	A19		A19
WGATE*	A20		A20
+5V	A21		A21
TRACK0*	A22		A22
HDSEL0*	A23		A23
HDSEL1*	A24		A24
	A25		A25
RDY*	A26		A26
DRSEL1*	A27		A27
	A28		A28
DRSEL3*	A29		A29
DIR*	A30		A30
N/C	A31		A31
	A32		A32
EEN*	B1		B1
HSP*	B2		B2
WDA*	B3		B3
CIN*	B4		B4
UTH*	B5		B5
SEL0*	B6		B6
SP13	B7		B7
TRI*	B8		B8
REV*	B9		B9
N/C	B10		B10
FRDY*	B11		B11
RDATA*	B12		B12
FWGAT*	B13		B13
FDIR*	B14		B14
DSI*	B15		B15
SP16	B16		B16
	B17		B17
	B18		B18
	B19		B19
	B20		B20
	B21		B21
	B22		B22
	B23		B23
	B24		B24
	B25		B25
	B26		B26
	B27		B27
	B28		B28
	B29		B29
	B30		B30
	B31		B31
	B32		B32
	C1		C1
THD*	C2		C2
TACH*	C3		C3
SEL0*	C4		C4
RDP*	C5		C5
SP15	C6		C6
TTRST*	C7		C7
TR2*	C8		C8
GO*	C9		C9
N/C	C10		C10
+5V	C11		C11
WRPRT*	C12		C12
WDATA*	C13		C13
NOTSWX	C14		C14
DSO*	C15		C15
INUSE*	C16		C16
N/C	C17		C17
N/C	C18		C18
HDSEL2*	C19		C19
SKCOMP*	C20		C20
	C21		C21
WFAULT*	C22		C22
SP19	C23		C23
INDEX*	C24		C24
+5V	C25		C25
STEP*	C26		C26
DRSEL2*	C27		C27
	C28		C28
SP18	C29		C29
N/C	C30		C30
N/C	C31		C31
+5V	C32		C32

XMB
J2A-J2F

+5V	A1		A1
A23*	A2		A2
A21*	A3		A3
A19*	A4		A4
A17*	A5		A5
A15*	A6		A6
A13*	A7		A7
	A8		A8
A11*	A9		A9
A09*	A10		A10
A07*	A11		A11
A05*	A12		A12
A03*	A13		A13
A01*	A14		A14
HWEN*	A15		A15
+5V	A16		A16
BRQ7*	A17		A17
BRQ5*	A18		A18
BRQ3*	A19		A19
BRQ1*	A20		A20
	A21		A21
BPN7*	A22		A22
BPN5*	A23		A23
BPN3*	A24		A24
BPN1*	A25		A25
BUSY*	A26		A26
CBRQ*	A27		A27
LOCK*	A28		A28
PF*	A29		A29
UPSS*	A30		A30
-12V	A31		A31
+12V	A32		A32
N/C	B1	BD0	B1
N/C	B2	BD1	B2
N/C	B3	BD2	B3
N/C	B4	BD3	B4
N/C	B5	BD4	B5
N/C	B6	BD5	B6
N/C	B7	BD6	B7
N/C	B8	BD7	B8
N/C	B9	DINT*	B9
N/C	B10	DDO	B10
N/C	B11	DD1	B11
N/C	B12	DD2	B12
N/C	B13	DD3	B13
N/C	B14	DD4	B14
N/C	B15	DD5	B15
N/C	B16	DD6	B16
N/C	B17	DD7	B17
N/C	B18	CTLRST*	B18
N/C	B19	CTLCS*	B19
N/C	B20	CTLRD*	B20
N/C	B21	CTLWR*	B21
N/C	B22	DATENX	B22
N/C	B23	DATT/R*	B23
N/C	B24	SP12	B24
N/C	B25	CRD*	B25
N/C	B26	CWR*	B26
N/C	B27	BRDY	B27
N/C	B28	BDRQ	B28
N/C	B29	BCR*	B29
N/C	B30	BCS*	B30
N/C	B31	-12V	B31
N/C	B32	+12V	B32
	C1		C1
A22*	C2		C2
A20*	C3		C3
A18*	C4		C4
A16*	C5		C5
A14*	C6		C6
A12*	C7		C7
+5V	C8		C8
A10*	C9		C9
A08*	C10		C10
A06*	C11		C11
A04*	C12		C12
A02*	C13		C13
A00*	C14		C14
HBEN*	C15		C15
	C16		C16
BRQ6*	C17		C17
BRQ4*	C18		C18
BRQ2*	C19		C19
BRQ0*	C20		C20
+5V	C21		C21
BPN6*	C22		C22
BPN4*	C23		C23
BPN2*	C24		C24
BPN0*	C25		C25
	C26		C26
BCLK*	C27		C27
	C28		C28
SP2	C29		C29
MRST*	C30		C30
-12V	C31		C31
+12V	C32		C32

XMB
J2G

	A1		A1
	A2		A2
	A3		A3
	A4		A4
	A5		A5
	A6		A6
	A7		A7
	A8		A8
	A9		A9
	A10		A10
	A11		A11
	A12		A12
	A13		A13
	A14		A14
	A15		A15
	A16		A16
	A17		A17
	A18		A18
	A19		A19
	A20		A20
	A21		A21
	A22		A22
	A23		A23
	A24		A24
	A25		A25
	A26		A26
	A27		A27
	A28		A28
	A29		A29
	A30		A30
	A31		A31
	A32		A32
BD0	B1		B1
BD1	B2		B2
BD2	B3		B3
BD3	B4		B4
BD4	B5		B5
BD5	B6		B6
BD6	B7		B7
BD7	B8		B8
DINT*	B9		B9
DDO	B10		B10
DD1	B11		B11
DD2	B12		B12
DD3	B13		B13
DD4	B14		B14
DD5	B15		B15
DD6	B16		B16
DD7	B17		B17
CTLRST*	B18		B18
CTLCS*	B19		B19
CTLRD*	B20		B20
CTLWR*	B21		B21
DATENX	B22		B22
DATT/R*	B23		B23
SP12	B24		B24
CRD*	B25		B25
CWR*	B26		B26
BRDY	B27		B27
BDRQ	B28		B28
BCR*	B29		B29
BCS*	B30		B30
-12V	B31		B31
+12V	B32		B32
	C1		C1
	C2		C2
	C3		C3
	C4		C4
	C5		C5
	C6		C6
	C7		C7
	C8		C8
	C9		C9
	C10		C10
	C11		C11
	C12		C12
	C13		C13
	C14		C14
	C15		C15
	C16		C16
	C17		C17
	C18		C18
	C19		C19
	C20		C20
	C21		C21
	C22		C22
	C23		C23
	C24		C24
	C25		C25
	C26		C26
	C27		C27
	C28		C28
	C29		C29
	C30		C30
	C31		C31
	C32		C32

CONTR
J2H

+5V	A1		A1
+MFMWD3	A2		A2
-MFMWD3	A3		A3
DSELD3*	A4		A4
+MFMRD3	A5		A5
-MFMRD3	A6		A6
SP25	A7		A7
	A8		A8
SP27	A9		A9
SP29	A10		A10
N/C	A11		A11
SP30	A12		A12
SP31	A13		A13
+MFMWD2	A14		A14
-MFMWD2	A15		A15
+5V	A16		A16
DSELD2*	A17		A17
+MFMRD2	A18		A18
-MFMRD2	A19		A19
SP37	A20		A20
	A21		A21
SP40	A22		A22
SP42	A23		A23
SP44	A24		A24
SP46	A25		A25
+MFMWD1	A26		A26
-MFMWD1	A27		A27
DSELD1*	A28		A28
+MFMRD1	A29		A29
-MFMRD1	A30		A30
-12V	A31		A31
+12V	A32		A32
	B1		B1
	B2		B2
	B3		B3
	B4		B4
	B5		B5
	B6		B6
	B7		B7
	B8		B8
	B9		B9
	B10		B10
	B11		B11
	B12		B12
	B13		B13
	B14		B14
	B15		B15
	B16		B16
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	B18		B18
	B19		B19
	B20		B20
	B21		B21
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	B24		B24
	B25		B25
	B26		B26
	B27		B27
	B28		B28
	B29		B29
	B30		B30
	B31		B31
	B32		B32
	C1		C1
SP20	C2		C2
SP21	C3		C3
SP22	C4		C4
SP23	C5		C5
SP24	C6		C6
SP26	C7		C7
+5V	C8		C8
SP28	C9		C9
N/C	C10		C10
N/C	C11		C11
SP32	C12		C12
SP33	C13		C13
SP34	C14		C14
SP35	C15		C15
	C16		C16
N/C	C17		C17
SP36	C18		C18
SP38	C19		C19
SP39	C20		C20
+5V	C21		C21
SP41	C22		C22
SP43	C23		C23
SP45	C24		C24
SP47	C25		C25
	C26		C26
SP48	C27		C27
	C28		C28
SP49	C29		C29
N/C	C30		C30
-12V	C31		C31
+12V	C32		C32

DRIVE 3
J4

	A1		C1 HDSEL3*
	A2		C2 HDSEL2*
	A3		C3 WGATE*
	A4		C4 SKCOMP*
	A5		C5 TRACK0*
	A6		C6 WFAULT*
	A7		C7 HDSELD*
	A8		C8 SP19
	A9		C9 HDSEL1*
	A10		C10 INDEX*
	A11		C11 RDY*
	A12		C12 STEP*
	A13		C13 DRSEL3*
	A14		C14 DRSEL1*
	A15		C15 DRSEL2*
	A16		C16 SP18
DSELD3*	A17		C17 DIR*
N/C	A18		C18
N/C	A19		C19
N/C	A20		C20
N/C	A21		C21 N/C
N/C	A22		C22
	A23		C23
+MFMWD3	A24		C24 -MFMWD3
	A25		C25
+MFMRD3	A26		C26 -MFMRD3
	A27		C27
SP20	A28		C28 SP21
SP22	A29		C29 SP23
SP24	A30		C30 SP25
SP26	A31		C31 SP27
SP28	A32		C32 SP29

DRIVE 2
J5

	A1		C1 HDSEL3*
	A2		C2 HDSEL2*
	A3		C3 WGATE*
	A4		C4 SKCOMP*
	A5		C5 TRACK0*
	A6		C6 WFAULT*
	A7		C7 HDSELO*
	A8		C8 SP19
	A9		C9 HDSEL1*
	A10		C10 INDEX*
	A11		C11 RDY*
	A12		C12 STEP*
	A13		C13 DRSEL2*
	A14		C14 DRSEL3*
	A15		C15 DRSEL1*
	A16		C16 SP18
DSELD2*	A17		C17 DIR*
N/C	A18		C18
N/C	A19		C19
N/C	A20		C20
N/C	A21		C21 N/C
N/C	A22		C22
	A23		C23
+MFMWD2	A24		C24 -MFMWD2
	A25		C25
+MFMRD2	A26		C26 -MFMRD2
	A27		C27
SP30	A28		C28 SP31
SP32	A29		C29 SP33
SP34	A30		C30 SP35
SP36	A31		C31 SP37
SP38	A32		C32 SP39

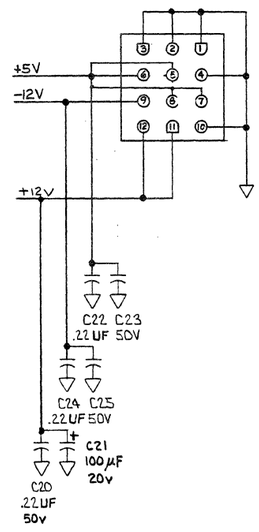
DRIVE 1
J6

	A1		C1 HDSEL3*
	A2		C2 HDSEL2*
	A3		C3 WGATE*
	A4		C4 SKCOMP*
	A5		C5 TRACK0*
	A6		C6 WFAULT*
	A7		C7 HDSELO*
	A8		C8 SP19
	A9		C9 HDSEL1*
	A10		C10 INDEX*
	A11		C11 RDY*
	A12		C12 STEP*
	A13		C13 DRSEL1*
	A14		C14 DRSEL2*
	A15		C15 DRSEL3*
	A16		C16 SP18
	A17		C17 DIR*
DSELD1*	A18		C18
N/C	A19		C19
N/C	A20		C20
N/C	A21		C21
N/C	A22		C22 N/C
	A23		C23
+MFMWD1	A24		C24 -MFMWD1
	A25		C25
+MFMRD1	A26		C26 -MFMRD1
	A27		C27
SP40	A28		C28 SP41
SP42	A29		C29 SP43
SP44	A30		C30 SP45
SP46	A31		C31 SP47
SP48	A32		C32 SP49

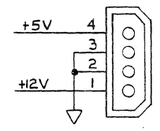
TAPE
J3

	1		2 GO*
	3		4 REV*
	5		6 TR3*
	7		8 TR2*
	9		10 TRI*
	11		12 TRO*
	13		14 TTRST*
	15		16 SP13
	17		18 SP14
	19		20 SP15
	21		22 SELO*
	23		24 HC*
	25		26 RDP*
	27		28 UTH*
	29		30 LTH*
	31		32 SELD*
	33		34 CIN*
	35		36 USF*
	37		38 TACH*
	39		40 WDA*
	41		42 WDA
	43		44 THD*
	45		46 HSP*
	47		48 WEN*
	49		50 EEN*

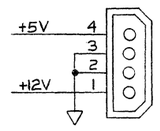
DC POWER
JA



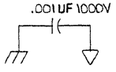
TAPE POWER
JB



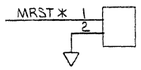
FLOPPY POWER
JC



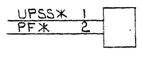
C4-C15
.001 UF 1000V



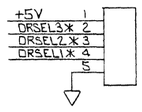
RESET SWITCH
J8



POWER FAIL # SENSE
J10

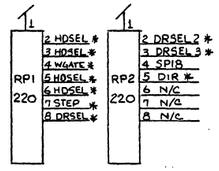


J9



FLOPPY
J7

	1		2 HDLOAD*
	3		4 INUSE*
	5		6 SP16
	7		8 FINDEX*
	9		10 DSO*
	11		12 DSI*
	13		14 SP17
	15		16 MOTON*
	17		18 FDIR*
	19		20 FSTEP*
	21		22 WDATA*
	23		24 FWGAT*
	25		26 FTRKO*
	27		28 WRPRT*
	29		30 RDATA*
	31		32 SIDE1*
	33		34 FRDY*

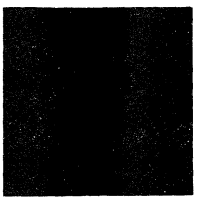


BACKPLANE PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

SHEET 1 OF 1

BACKPLANE PCB PART LOCATIONS

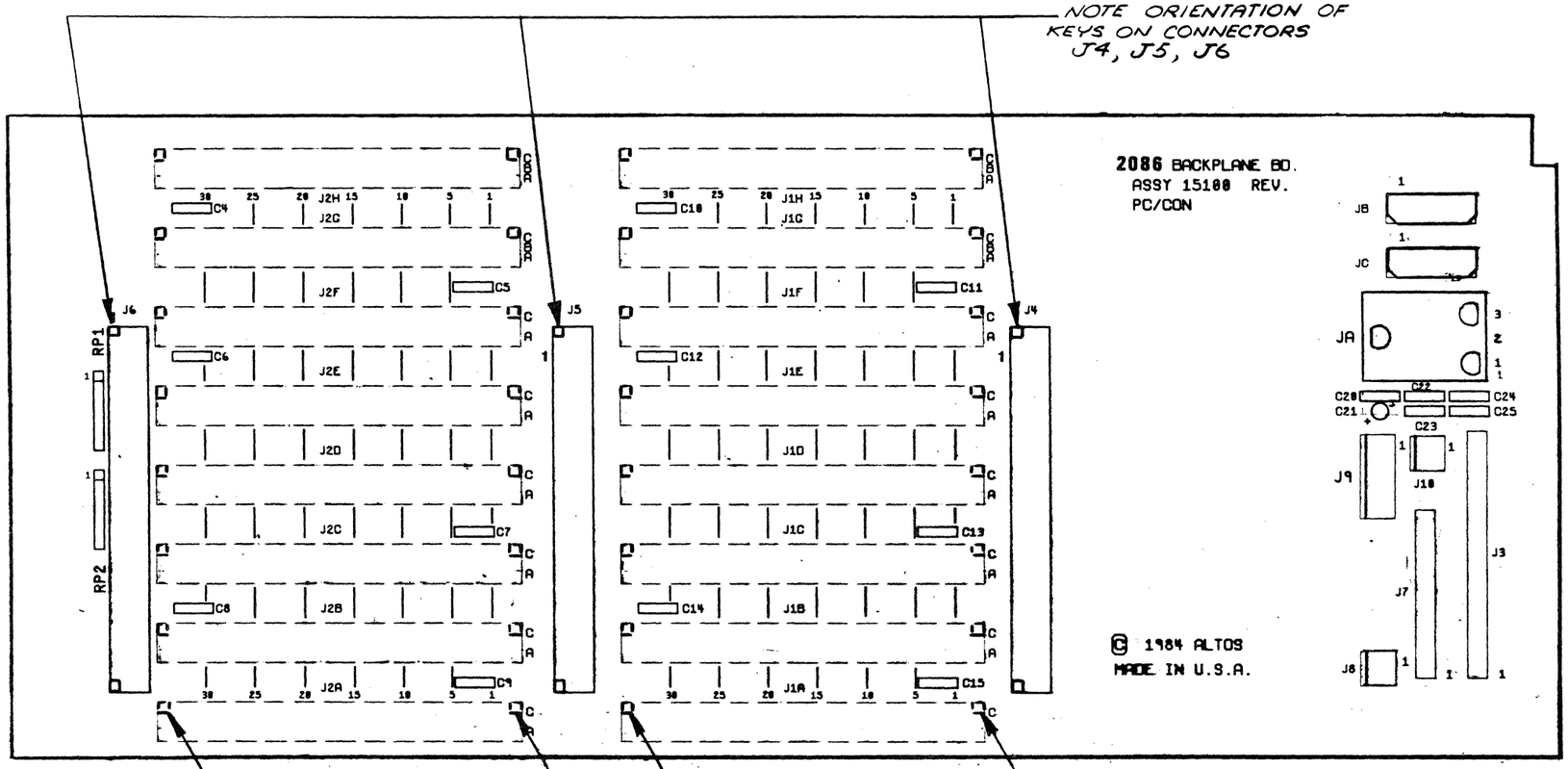


DWG. NO.	SH	REV.
615-15100-001		C

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	X1	PROTOTYPE		
	X2A	PROTOTYPE	10-22-84	
	X3A	PROTOTYPE	12-12-84	
	X4A	PROTOTYPE		
	4-A	PRE- PRODUCTION EO#2900	3-1-85	
	5A	EO # 2983-H mf	3-27-85	
	A	PROD. REL. EO 3544-H	6-27-85	
	B	EO # 3588-H mf	10 JAN 86	
	C	EO # 3862-H mf	10 JAN 86	

NOTE ORIENTATION OF KEYS ON CONNECTORS J4, J5, J6



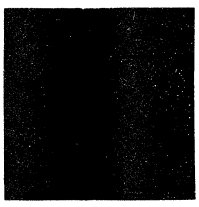
COMPONENT SIDE

NOTE ORIENTATION OF KEYS ON CONNECTORS J1A THROUGH J1H AND J2A THROUGH J2H. (FAR SIDE)

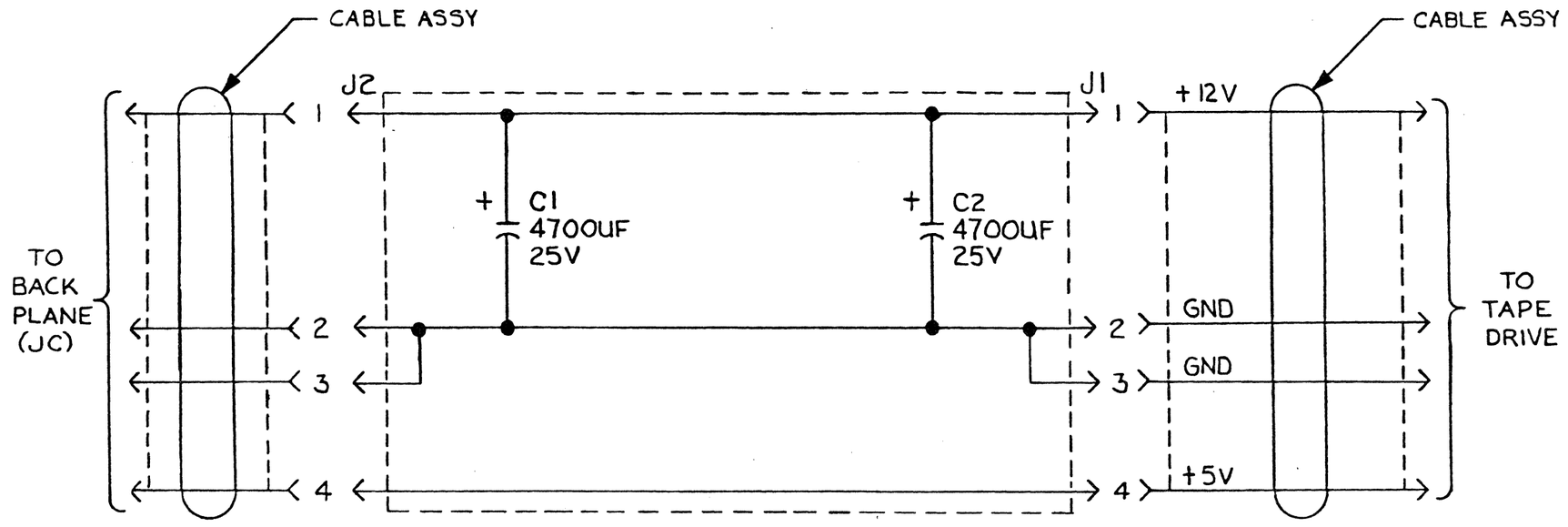
BACKPLANE PCB PART LOCATIONS

ALTOS COMPUTER SYSTEMS

LOW-PASS FILTER PCB SCHEMATIC DIAGRAM



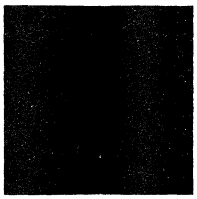
REVISIONS				
REV	ZONE	DESCRIPTION	DATE	APPROVED
X1A		PROTOTYPE	9 MAY 85	
1A		PRE-PRODUCTION EO3155	30 MAY 85	



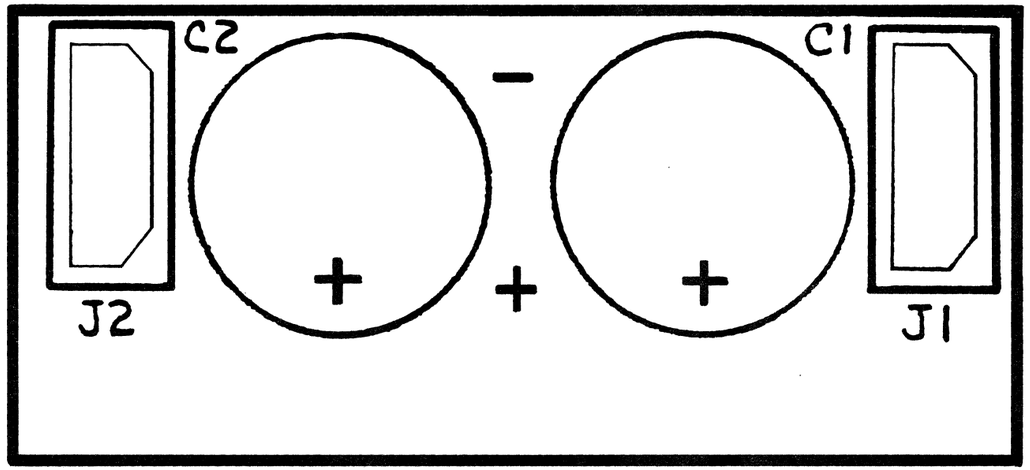
LOW-PASS FILTER PCB SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

LOW-PASS FILTER PCB PART LOCATIONS



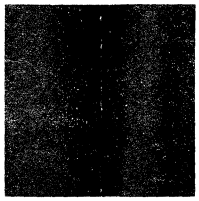
REVISIONS				
REV	ZONE	DESCRIPTION	DATE	APPROVED
X1A		PROTOTYPE	24 Nov 85	
1A		PRE-PRODUCTION EO 3155	30 Nov 85	



LOW-PASS FILTER PCB PART LOCATIONS

ALTOS COMPUTER SYSTEMS

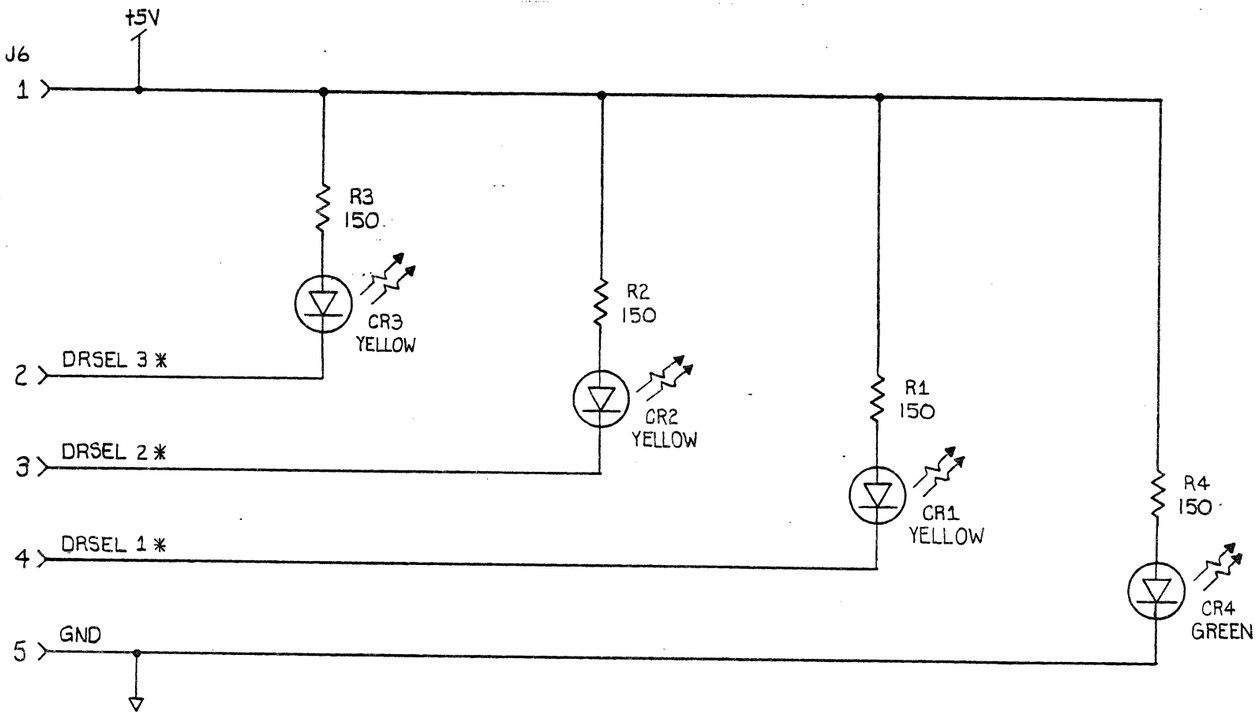
LED PCB SCHEMATIC DIAGRAM



DWG. NO.	SH	REV.
625-16338-001	1	A

REVISIONS

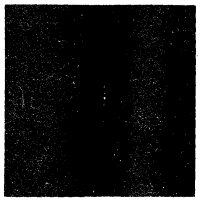
REV.	ZONE	DESCRIPTION	DATE	APPROVED
X1A		PROTOTYPE		
X2A		PROTOTYPE	12-18-84	
2A		PRE- PRODUCTION EO# 2900	3-1-85	
3A		REVISED PER EO#3005-H	8-28-85	
A		PROD. REL. EO# 3544-H	9-29-85	



LED PCB
SCHEMATIC DIAGRAM

ALTOS COMPUTER SYSTEMS

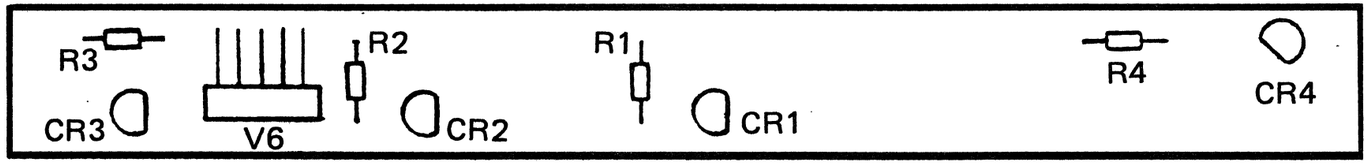
LED PCB PART LOCATIONS



DWG. NO.	SH	REV.
615-16336-001	1	A

REVISIONS

REV.	ZONE	DESCRIPTION	DATE	APPROVED
X1A		PROTOTYPE		
X2A		PROTOTYPE	2-26-85	
2A		PRE-PRODUCTION EO# 2900	3-1-85	
3A		EO 2928	3-12-85	
4A		REVISED PER EO # 3005-H	8-28-85	
A		PROD. REL EO 3544-H	9-29-85	



LED PCB
PART LOCATIONS

ALTOS COMPUTER SYSTEMS

MANUAL CHANGE INFORMATION

Change information in this section may include:

- changes that occurred too late to include in this manual
- changes that occurred since the first printing and have been incorporated in this revision of the manual
- change information that was provided by a separate change package publication

NOTE

Change information is sometimes provided to our customers by a change package publication. If you receive a change package for this manual, make the changes as instructed in the package and insert a summary of the changes (or, if you wish, the entire change package) in this section.

CHANGE INFORMATION

The following summarizes the specific changes that have been made to the previous version of this manual.

Title: 1086/2086 Maintenance Manual

Revised Part Number: 690-18365-002

Previous Part Numbers: 690-15624-001, 690-17472-001

Date: September 1986

Changes:

- **All Affected Pages.** Changed all references to the 2086 to read **1086/2086.**

- **Page vi.** Added the following to the list under **Supplemental Information:**

  Altos 1086/2086 Remote Diagnostics Instructions (Altos part no. 690-17072-001)

- **Page 1-3.** Changed the following item in the list under **Characteristics:**

  up to 451M bytes of formatted internal hard disk storage

- **Page 1-3.** Deleted the following item under **Characteristics:**

  up to 40 synchronous communication ports

- **Page 1-5.** Changed the second paragraph under **Communications** as follows:

  The software for 3270, 3780, X.25, and SNA protocols runs on the 1086/2086. The 1086/2086 is capable of supporting asynchronous

modems for dial-up data base services or off-site communications and bisynchronous modems for IBM 378Ø emulation. WorkNet can also be supported through one port via a software command communicating at 1.4M bits per second or 75ØK bits per second (used to connect IBM PCs or compatibles to Altos processors). The optional communications PCB subsystem, configured with 32K bytes of RAM, supports certified X.25 or IBM/SNA software protocols.

- **Page 2-1 through 2-9.** Replaced all of **Chapter 2, Specifications.**

- **Page 3-7.** Replaced the paragraph under **System Memory** with the following:

  The memory PCB contains either 1M, 2M, or 4M bytes of memory depending upon whether 64K byte or 256K byte RAMs are used. Memory is organized into 32-bit long words or 64-bit double long words depending upon which version of the memory PCB is used. (There are two versions of the memory PCB as described in the Memory PCB section of this chapter.) Data transfer is in 8-, 16-, or 32-bit quantities.

- **Page 3-25.** Replaced the **NOTE** at the top of the page with the following:

  NOTE

  The file processor is the only exception to releasing the bus in 8 microseconds. The file processor can hold the bus up to 2ØØ microseconds regardless of how long the CBRQ* signal is asserted.

- **Page 3-55 through 3-62.** Rewrote the memory PCB information to include a new modified version of the memory PCB.

- **Page 3-65.** Changed the last sentence in the first paragraph under **Local Bus Interface** to read as follows:

  The number of wait states for the SCC accesses may be increased by the recovery wait (RWAIT*) signal if a given SCC's recovery time has not elapsed.

- **Page 3-87.** Changed the description for bit PBØ in **Table 3-12** to read as follows:

  A logic 1 will clear the parity error NMI. Must be set to Ø to allow more parity errors (and NMI) to be detected

- **Page 3-112.** Added the following bit to **Table 3-18** and changed bits FPD13-FPD15 as follows:

FPD13	**SCSIAVAIL**	**SCSI controller present on file processor PCB**
FPD14,15	**Ø**	**Grounded**

- **Pages 5-15 through 5-42.** Rewrote all of the **Power-Up Tests** section.

- **Page 5-57.** Changed the reference from WD2Ø1Ø to uPD765 in parenthesis in the seventh line of the paragraph under **1Ø Floppy Random Seek Test.**

- Added Table 5-1Ø, SDX Trouble Analysis, pages 5-72 through 5-78.

- **Page 5-89.** Changed the list of CPU debugger commands under **CPU Debugger Commands.**

- **Page 5-89 through 5-96.** Changed the command descriptions as listed under **CPU Debugger Commands.**

- **Page 5-97.** Changed the debugger commands under **Communications Debugger Commands (Software Mode):**

- **Page 5-101.** Added the following debugger commands after command **X** in the list under **Communications Debugger Commands (Hardware Mode):**

  ? Display Command Menu

  <BREAK> Switch to software mode

- **Page 5-104.** Changed the syntax under **L Loopback Test.**

- **Page 5-106.** Changed the paragraph titled **RESTRICTIONS:** as follows:

  RESTRICTIONS: [address] must not be within the 0 to 7FFh range. Each macro can be any length up to the maximum number of bytes in memory. All input is redirected into the memory until ESCAPE is typed to return to the command execution mode. The only restriction to the number of macros that can be stored is the size of the memory.

- **Pages A-15, A-16, and A-17.** Changed **PRIMARY COMMUNICATIONS PCB** to **EXPANSION COMMUNICATIONS PCB** for jumper connector E1 in Figures A-18, A-19, and A-20.

- **Pages B-1 through B-10.** Changed Appendix B to include 50M, 80M, and 190M byte drives.

- Added Appendix E, Adjustment Procedures, after page D-4 in the **Appendices** section.

READER COMMENT FORM

1086/2086 MAINTENANCE MANUAL

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January 1987