7X54 DISC STORAGE CONTROLLER

STUDENT MANUAL

REVISION RECORD

REVISION	DESCRIPTION

Publication No.
75440773

This manual contains all necessary Student Materials for the subject course and is to be retained by the student.

The following sections will normally be included in this manual. However, if they are not included, it is because they have not been developed at this time.

- Course and Learning Objectives - The Course Objectives identify student performance, and the Learning Objectives identify the steps needed to accomplish the Course Objectives.
- Course Chart - This is a layout of the course on a daily basis, and can be used by the student in planning his time in the course.

  Handouts - These are normally drawings that are used for clarification or to provide supplementary information.
- Workbook - This is assigned by the instructor either as homework or work to be done in the lab while waiting for machine time. The workbook is not assigned as "Busy Work," but is an integral part of the course.
- Student Lab Manual - This is used by the student as a guide in the lab. There may be projects to perform, questions to answer or reading assignments to complete, and like the workbook this is another important element of the course and should be completed in a timely manner.

CONTENTS

7x54 COURSE AND LEARNING OBJECTIVES

NOTE: EXCEPT WHERE OTHERWISE STATED, EVIDENCE OF SUCESSFULLY MEETING THE LEARNING OBJECTIVES WILL BE INDICATED BY SATISFACTORILY COMPLETING LAB. WORKSHEET AND/OR HOMEWORK SHEETS AND/OR THE CORRECT SELECTION OF ONE OF FOUR POSSIBLE ANSWERS TO A TEST ITEM. SATISFACTORY COMPLETION IS DEMONSTRATED BY ANSWERING AT LEAST 70% OF THE HOMEWORK AND EXAMINATION ITEMS CORRECTLY. IN DEMONSTRATING ACHIEVEMENT OF ALL COURSE/LEARNING OBJECTIVES EACH STUDENT WILL BE ABLE TO USE ALL MATERIAL DISTRIBUTED DURING THE COURSE.

Upon successful completion of this course the student will be able to:

C.O. 1 Install the FA722 using the procedures in the C.E. Manual No. 60428500.

E.S.W.B.A.T.

L.O. 1 Describe the block diagram of the subsystem configuration including:

A. The cables used to connect the P.P.U. to the FA722.

B. The cables used to connect the FA722 to the 844.

L.O. 1.2 List the A.C. power requirements of the FA722.

L.O. 1.3 Perform, in lab, coupler clock tuning within 30 min.

C.O. 2 Check out the FA722 using the procedures in C.E. Manual No. 60428500.

E.S.W.B.A.T.

*L.O. 2.1 Identify proper switch settings on FA722 for operation with a Cyber 70 or Cyber 170 Computer System.

*L.O. 2.2 Prepare, in lab, FA722 for power up operation within 10 min.

A. Setting C.R.'s on.

B. Setting auxiliary operator panel switches to the specified positions.

C. Adjusting power supply voltages to specified values.

C.O. 3 Run the 844/7x54 diagnostics on the Cyber 70 or Cyber 170 Computer System and on the Buffer Controller Maintenance Console and determine if the 844 and 7x54 are functioning properly using all sections of the diagnostics.

E.S.W.B.A.T.

L.O. 3.1 List the parameter words and the purpose of each.

L.O. 3.2 List the purposes of the parameter display.

L.O. 3.3 Interpret and explain error codes using Buffer Controller Diagnostic Reference Manual Pub. No. 60400300.

L.O. 3.4 Run, in lab, all 844/7x54 subsystem diagnostics within 4 hours.

L.O. 3.5 Insert parameters to limit tests to specific tracks and/or heads within 10 min.

L.O. 3.6 Given subsystem hardware failure indications list probable causes of the failure as indicated by running 844/7x54 subsystem diagnostics.

C.O. 4 Perform operator functions on the FA722, using the procedures in the C.E. Manual No. 60428500.

E.S.W.B.A.T.

L.O. 4.1 Perform, in lab, FA722 power on operation within 3 min.

L.O. 4.2 Use, in lab, auxiliary operator panel on FA722. Within 5 min. perform the following operations.

A. Master clear the FA722.

B. Clear memory parity error.

C. Set selective stop switch on.

L.O. 4.3 Select, in lab, proper setting of channel parity switch for operation with a Cyber 70 or Cyber 170.

C.O. 5 Perform preventive maintenance on the FA722 using the procedures in the C.E. Manual No. 60428500.

E.S.W.B.A.T.

L.O. 5.1 Monthly (level 2) demonstrates his ability, in lab, to perform Monthly P.M. as outlined in the P.M. portions of the C.E. Manual within 35 min.

L.O. 5.2 Quarterly, (level 3) demonstrate his ability, in lab, to perform Quarterly P.M. as outlined in the P.M. portion of the C.E. Manual within 5 min.

L.O. 5.3 Semi-annually (level 4) demonstrates his ability, in lab, to perform Quarterly P.M. as outlined in the P.M. portion of the C.E. Manual within 70 min.

C.O. 6 Explain and identify all portions of the FA722 logic using C.E. Manuals No. 60428500, 60364500, and 60363900.

E.S.W.B.A.T.

L.O. 6.1 Trace the data path from the P.P.U. to the disk interface.

L.O. 6.2 Trace the data path from the disk interface to the P.P.U.

L.O. 6.3 Trace the data path from the P.P.U. to the subsystem memory.

L.O. 6.4 Trace the data path from the subsystem memory to the P.P.U.

L.O. 6.5 State how the basic clocks are derived and their relationship to write and read timing.

L.O. 6.6 Define all normal input and output channels.

C. O. 7 Explain and identify all subsystem instructions using C. E. Manuals No. 60428500, 60364500, and 60363900.

E. S. W. B. A. T.

*L. O. 7. 1 Define all buffer controller instructions including:

A. Instruction block diagram flow.

B. Command timing logic sequences.

L. O. 7. 2 Define all hardware controller directions including;

A. Director block diagram flow.

B. Director logic sequences.

L. O. 7. 3 Define all P. P. U. function codes including:

A. Controlware interpretation of functions.

B. Coupler logic response.

C. O. 8 Perform emergency maintenance on the FA722 using available documentation including diagrams and procedures in the C. E. Manuals No. 60428500, 60364500, and 60363900.

E. S. W. B. A. T.

*L. O. 8. 1 Demonstrate, in lab, his ability to recognize, diagnose and correct instructor induced logic problem's to the module within 90 min. using when necessary, test equipment, including off-line diagnostics.

C. O. 9 Perform equipment modification on the FA722 using the procedure provided with the F. C. O.

E. S. W. B. A. T.

L. O. 9. 1 Perform, in lab, mechanically and electrically secure wire wrap installation using the special tool provided, within 15 min.

DENNIS WEISGRAM

	DAY 1	DAY 2	DAY 3	DAY 4	DAY 5
1	Introduction to Buffer Controller	Review	Review	Buffer Controller Trouble-shooting LAB	Review
2		Format 2 Instructions	Buffer Controller Logic Overview		System Overview
3	Format 1 Instructions		Instruction Command Timing		P.P.U Commands
4					
5		B.C. Logic Overview			Coupler Block Diagrams
6					
7	Home Study	Home Study	Home Study		Home Study
8					

	DAY 6	DAY 7	DAY 8	DAY 9	DAY 10
1	Review	Review		Review	Review
2	Continued Coupler Block Diagrams and Channel Descriptions	Coupler Logic Sequences	Introduction to H. C. Includes: 1. Block Diagram 2. NOC 8 & 9 Functions 3. Memory Requests 4. Basic Description of Director	Logic Overview	NOC 8 & 9 Function Flow and Logic Description
3		FA 722 Coupler Difference			Support Directors Block Diagram and Logic Description
4	Coupler Logic Overview	B. C. and Coupler Test and Critique			
5				NOC 8 & 9 Function Flow and Logic Description	
6					
7	Home Study	Home Study	Home Study	Home Study	Home Study
8					

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	DAY	DAY	DAY	DAY	DAY
1	Review	Review	H. C. and Coupler Trouble- shooting LAB	H. C. and Coupler Trouble- shooting LAB	H. C. and Coupler Trouble- shooting LAB
2	Controlware 1. Introduction 2. Initialization	Data Directors Block Diagrams and Logic Description			
3	3. Monitor Loops 4. General Status 5. Seek				
4	Data Directors				
5	1. Read Time Sector Sequence Controlware	H. C. Test and Critique			
6	3. Read Sequence Controlware				
7	Home Study	Home Study			
8					

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7×54 SUBSYSTEM PROCESSOR

STUDENT HANDOUTS

TABLE VI CONVERSION

HEX.	DEC.	HEX.	DEC.	HEX.	DEC.	HEX.	DEC.	HEX.	DEC.
1	1	10	16	100	256	1000	4096	10000	65536
2	2	20	32	200	512	2000	8192	20000	131072
3	3	30	48	300	768	3000	12288	30000	196608
4	4	40	64	400	1024	4000	16384	40000	262144
5	5	50	80	500	1280	5000	20480	50000	327680
6	6	60	96	600	1536	6000	24576	60000	393216
7	7	70	112	700	1792	7000	28672	70000	458752
8	8	80	128	800	2048	8000	32768	80000	524288
9	9	90	144	900	2304	9000	36864	90000	589824
A	10	A0	160	A00	2560	A000	40960	A0000	655360
B	11	B0	176	B00	2816	B000	45056	B0000	720896
C	12	C0	192	C00	3072	C000	49152	C0000	786432
D	13	D0	208	D00	3328	D000	53248	D0000	851968
E	14	E0	224	E00	3584	E000	57344	E0000	917504
F	15	F0	240	F00	3840	F000	61440	F0000	983040

HEX.	DEC.	HEX.	DEC.	HEX.	DEC.
100000	1048576	1000000	16777216	10000000	268435456
200000	2097152	2000000	33554432	20000000	536870912
300000	3145728	3000000	50331648	30000000	805306368
400000	4194304	4000000	67108864	40000000	1073741824
500000	5242880	5000000	83886080	50000000	1342177280
600000	6291456	6000000	100663296	60000000	1610612736
700000	7340032	7000000	117440512	70000000	1879048192
800000	8388608	8000000	134217728	80000000	2147483648
900000	9437184	9000000	150994944	90000000	2415919104
A00000	10485760	A000000	167772160	A0000000	2684354560
B00000	11534336	B000000	184549376	B0000000	2952790016
C00000	12582912	C000000	201326592	C0000000	3221225472
D00000	13631488	D000000	218103808	D0000000	3489660928
E00000	14680064	E000000	234881024	E0000000	3758096384
F00000	15728640	F000000	251658240	F0000000	4026531840

POWERS OF SIXTEEN	
16^0	1
16^1	16
16^2	256
16^3	4096
16^4	65536
16^5	1048576
16^6	16777216
16^7	268435456

TABLE IV

HEXADECIMAL ADDITION

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10
2	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11
3	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12
4	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13
5	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14
6	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15
7	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16
8	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17
9	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18
A	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19
B	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A
C	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B
D	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
E	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D
F	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

HEX	BINARY
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
A	1010
B	1011
C	1100
D	1101
E	1110
F	1111

TABLE V

HEXADECIMAL MULTIPLICATION

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
2	00	02	04	06	08	0A	0C	0E	10	12	14	16	18	1A	1C	1E
3	00	03	06	09	0C	0F	12	15	18	1B	1E	21	24	27	2A	2D
4	00	04	08	0C	10	14	18	1C	20	24	28	2C	30	34	38	3C
5	00	05	0A	0F	14	19	1E	23	28	2D	32	37	3C	41	46	4B
6	00	06	0C	12	18	1E	24	2A	30	36	3C	42	48	4E	54	5A
7	00	07	0E	15	1C	23	2A	31	38	3F	46	4D	54	5B	62	69
8	00	08	10	18	20	28	30	38	40	48	50	58	60	68	70	78
9	00	09	12	1B	24	2D	36	3F	48	51	5A	63	6C	75	7E	87
A	00	0A	14	1E	28	32	3C	46	50	5A	64	6E	78	82	8C	96
B	00	0B	16	21	2C	37	42	4D	58	63	6E	79	84	8F	9A	A5
C	00	0C	18	24	30	3C	48	54	60	6C	78	84	90	9C	A8	B4
D	00	0D	1A	27	34	41	4E	5B	68	75	82	8F	9C	A9	B6	C3
E	00	0E	1C	2A	38	46	54	62	70	7E	8C	9A	A8	B6	C4	D2
F	00	0F	1E	2D	3C	4B	5A	69	78	87	96	A5	B4	C3	D2	E1

HEX	BINARY
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
A	1010
B	1011
C	1100
D	1101
E	1110
F	1111

TABLE VII

LOGICAL PRODUCT
(∧)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
2	0	0	2	2	0	0	2	2	0	0	2	2	0	0	2	2
3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
4	0	0	0	0	4	4	4	4	0	0	0	0	4	4	4	4
5	0	1	0	1	4	5	4	5	0	1	0	1	4	5	4	5
6	0	0	2	2	4	4	6	6	0	0	2	2	4	4	6	6
7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
8	0	0	0	0	0	0	0	0	8	8	8	8	8	8	8	8
9	0	1	0	1	0	1	0	1	8	9	8	9	8	9	8	9
A	0	0	2	2	0	0	2	2	8	8	A	A	8	8	A	A
B	0	1	2	3	0	1	2	3	8	9	A	B	8	9	A	B
C	0	0	0	0	4	4	4	4	8	8	8	8	C	C	C	C
D	0	1	0	1	4	5	4	5	8	9	8	9	C	D	C	D
E	0	0	2	2	4	4	6	6	8	8	A	A	C	C	E	E
F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

EXCLUSIVE OR
(⊻)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	1	0	3	2	5	4	7	6	9	8	B	A	D	C	F	E
2	2	3	0	1	6	7	4	5	A	B	8	9	E	F	C	D
3	3	2	1	0	7	6	5	4	B	A	9	8	F	E	D	C
4	4	5	6	7	0	1	2	3	C	D	E	F	8	9	A	B
5	5	4	7	6	1	0	3	2	D	C	F	E	9	8	B	A
6	6	7	4	5	2	3	0	1	E	F	C	D	A	B	8	9
7	7	6	5	4	3	2	1	0	F	E	D	C	B	A	9	8
8	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
9	9	8	B	A	D	C	F	E	1	0	3	2	5	4	7	6
A	A	B	8	9	E	F	C	D	2	3	0	1	6	7	4	5
B	B	A	9	8	F	E	D	C	3	2	1	0	7	6	5	4
C	C	D	E	F	8	9	A	B	4	5	6	7	0	1	2	3
D	D	C	F	E	9	8	B	A	5	4	7	6	1	0	3	2
E	E	F	C	D	A	B	8	9	6	7	4	5	2	3	0	1
F	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

INCLUSIVE OR
(∨)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	1	1	3	3	5	5	7	7	9	9	B	B	D	D	F	F
2	2	3	2	3	6	7	6	7	A	B	A	B	E	F	E	F
3	3	3	3	3	7	7	7	7	B	B	B	B	F	F	F	F
4	4	5	6	7	4	5	6	7	C	D	E	F	C	D	E	F
5	5	5	7	7	5	5	7	7	D	D	F	F	D	D	F	F
6	6	7	6	7	6	7	6	7	E	F	E	F	E	F	E	F
7	7	7	7	7	7	7	7	7	F	F	F	F	F	F	F	F
8	8	9	A	B	C	D	E	F	8	9	A	B	C	D	E	F
9	9	9	B	B	D	D	F	F	9	9	B	B	D	D	F	F
A	A	B	A	B	E	F	E	F	A	B	A	B	E	F	E	F
B	B	B	B	B	F	F	F	F	B	B	B	B	F	F	F	F
C	C	D	E	F	C	D	E	F	C	D	E	F	C	D	E	F
D	D	D	F	F	D	D	F	F	D	D	F	F	D	D	F	F
E	E	F	E	F	E	F	E	F	E	F	E	F	E	F	E	F
F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F

00XX SELECTIVE STOP

M	(M)
000	1ST INSTRUCTION
001	2ND "
002	3RD "
003	0000
004	INSTRUCTION
005	003A
006	INSTRUCTION
007	"
008	"
009	"
00A	00F0
00B	0005

010X SELECTIVE SET BIT T OF A

	INSTRUCTION	AI	AF
A.	0105	0000	0400
B.	010F	F002	F003
C.	0100	1000	9000
D.	0107	0300	0300
E.	010A	0000	0020
F.	0101	00FF	40FF

020X SELECTIVE CLEAR BIT T OF A

	INSTRUCTION	AI	AF
A.	0205	0F00	0B00
B.	020B	1234	1224
C.	0200	F234	7234
D.	0209	8888	8888
E.	0206	FFFF	FDFF
F.	020F	0211	0210

030X SELECTIVE COMPLEMENT BIT T OF A

	INSTRUCTION	AI	AF
A.	0307	FFFF	FEFF
B.	030C	0000	0008
C.	0300	A000	2000
D.	030A	0080	00A0
E.	0302	3210	1210
F.	030F	0001	0000

0400 SCALE A

	INSTRUCTION	AI	AF
A.	0400	0123	0007
B.	0400	2400	0002
C.	0400	00F0	0008
D.	0400	8310	0000
E.	0400	0000	0010
F.	0400	0004	000D

050X, 058X SHIFT A RIGHT T PLACES

	INSTRUCTION	AI	AF
A.	0504	1234	0123
B.	0584	1234	4123
C.	050A	FFFF	003F
D.	0500	4321	4321
E.	0501	0003	0001
F.	0581	0003	8001

06XX TRANSFER A TO B1
07XX TRANSFER A TO B2

	INSTRUCTION	A	B DESIG. & BF	
A.	0600	4321	1	4321
B.	0601	4321	1	4322
C.	06F4	0000	1	00F4
D.	0712	FFFF	2	0011
E.	07BA	1234	2	12EE
F.	0736	7FF0	2	8026

ST T = SHIFT COUNT

08XX SET CONDITION EQUAL: INTERNAL TESTS

	INSTRUCTION	ADD GEN BIT	A	CONDITION BIT F
A.	0820	1	XXXX	TRUE
B.	0820	0	XXXX	FALSE
C.	0840	X	1234	TRUE
D.	0840	X	1334	FALSE
E.	081C	X	1234	TRUE
F.	081C	X	2234	FALSE

09XX SET CONDITION EQUAL: BIT T, CHANNEL S

	INSTRUCTION	CHANNEL & CONTENTS		CONDITION BIT F
A.	093B	3	1234	TRUE
B.	093B	3	1224	FALSE
C.	09A5	A	FOFO	FALSE
D.	0991	NOT PRESENT	all ones in	TRUE
E.	09F0	F	8000	TRUE
F.	0900	0	4000	FALSE

OAXX SELECTIVE SET BIT T OF CHANNEL S
OBXX SELECTIVE CLEAR BIT T OF CHANNEL S

Channel "0" only one used

	INSTRUCTION	CHANNEL	CONTENTS I	CONTENTS F
A.	OA50	5	1234	9234
B.	OA95	9	F43A	F43A
C.	OAAB	A	2222	2232
D.	OBF3	F	1234	0234
E.	OB32	3	5678	5678
F.	OBOF	0	FFFF	FFFE

OCXO INPUT TO A FROM CHANNEL s

	INSTRUCTION	CHANNEL & CONTENTS		AF
A.	OC10	1	1234	1234
B.	OC50	5	5678	5678
C.	OCF0	F	39AB	39AB
D.	OCB0	NOT PRESENT		FFFF
E.	OC00	0	050A	050A
F.	OC90	9	0000	0000

ODX0,ODX8 SET CHANNEL s FROM A
OEX0,OEX8 CLEAR CHANNEL s FROM A

	INSTRUCTION	A	CI	CF
A.	OD10	1234	6ABB	7ABF
B.	ODF0	8888	3085	B88D
C.	OD58	89AB	1359	775D
D.	OEA0	3445	FA30	3000
E.	OE00	F012	C25A	C012
F.	OE98	BAC5	1234	0030

OFX0, OFX8 TRANSFER A TO CHANNEL S

	INSTRUCTION	A	CHANNEL & CONTENTS F	
A.	OF10	129F	1	129F
B.	OF50	F306	5	F306
C.	OFB0	D314	B	D314
D.	OF48	0000	4	FFFF
E.	OF38	51EB	3	AE14
F.	OFD8	85A0	D	7A5F

10XX ADD NO ADDRESS
11XX SUBTRACT NO ADDRESS

	INSTRUCTION	A_I	A_F	ADD GEN BIT
A.	10B7	1234	12EB	0
B.	109A	FF5B	FFF5	0
C.	1035	FFF0	0025	1
D.	1101	1234	1233	1
E.	1120	FFF7	FFD7	1
F.	1107	0005	FFFE	0

BOOLEAN FUNCTIONS

EXCLUSIVE OR $X \veebar Y = Z$

BIT N OF X	0	1	0	1
BIT N OF Y	0	0	1	1
RESULT BIT N OF Z	0	1	1	0

LOGICAL PRODUCT $X \wedge Y = Z$

BIT N OF X	0	1	0	1
BIT N OF Y	0	0	1	1
RESULT BIT N OF Z	0	0	0	1

12XX EXCLUSIVE OR NO ADDRESS
13XX LOGICAL PRODUCT NO ADDRESS

	INSTRUCTION	A_I	A_F
A.	1200	FA39	FA39
B.	1232	6157	6165
C.	12F0	196A	199A
D.	1300	1234	0000
E.	13F3	8DA5	00A1
F.	13A9	6034	0020

14XX TEST B1 NO ADDRESS
15XX TEST B2 NO ADDRESS

	INSTRUCTION	B_I	B_F	CONDITION BIT F
A.	1426	C026	C026	TRUE
B.	14F3	0008	0009	FALSE
C.	1400	FFFF	0000	FALSE
D.	150B	000B	000B	TRUE
E.	156D	756D	756D	TRUE
F.	153F	03F0	03F1	FALSE

16XX LOAD A COMPLEMENT NO ADDRESS

2's complement

	INSTRUCTION	A_F
A.	1601	FFFF
B.	1628	FFD8
C.	16FF	FF01
D.	16A7	FF59
E.	1600	0000
F.	160A	FFF6

17XX LOAD FROM A

	INSTRUCTION	A_I	EXECUTION ADDRESS	A_F
A.	1700	0234	234	(234)
B.	1700	5678	678	~~(678)~~ FFFF
C.	1701	0515	516	(516)
D.	17A3	0000	0A3	(0A3)
E.	17FF	1201	300	~~(300)~~ FFFF
F.	1725	0001	026	(026)

A 4K WORD MEMORY IS ASSUMED

FORMAT TWO

INSTRUCTION DESCRIPTION	Direct	Index B1	Index B2	Relative Forward	Indirect	Indirect/Index B1	Indirect/Index B2	Relative Backward
See Format One	00	01	02	03	04	05	06	07
	08	09	0A	0B	0C	0D	0E	0F
	10	11	12	13	14	15	16	17
Enter A with Address	18	19	1A	1B	1C	1D	1E	1F
Enter B1 with Address	20	21	22	23	24	25	26	27
Enter B2 with Address	28	29	2A	2B	2C	2D	2E	2F
Test Index B1	30	31	32	33	34	35	36	37
Test Index B2	38	39	3A	3B	3C	3D	3E	3F
Load A	40	41	42	43	44	45	46	47
Load A Complement	48	49	4A	4B	4C	4D	4E	4F
Load Left-most Byte	50	51	52	53	54	55	56	57
Load Right-most Byte	58	59	5A	5B	5C	5D	5E	5F
Add	60	61	62	63	64	65	66	67
Subtract	68	69	6A	6B	6C	6D	6E	6F
Exclusive OR	70	71	72	73	74	75	76	77
Logical Product	78	79	7A	7B	7C	7D	7E	7F
Replace Add	80	81	82	83	84	85	86	87
Replace Add One	88	89	8A	8B	8C	8D	8E	8F
Replace Left-most Byte	90	91	92	93	94	95	96	97
Replace Right-most Byte	98	99	9A	9B	9C	9D	9E	9F
Store	A0	A1	A2	A3	A4	A5	A6	A7
Store Zeroes	A8	A9	AA	AB	AC	AD	AE	AF
Destructive Load	B0	B1	B2	B3	B4	B5	B6	B7
Unconditional Jump	B8	B9	BA	BB	BC	BD	BE	BF
A Zero Jump	C0	C1	C2	C3	C4	C5	C6	C7
A Nonzero Jump	C8	C9	CA	CB	CC	CD	CE	CF
A Positive Jump	D0	D1	D2	D3	D4	D5	D6	D7
A Negative Jump	D8	D9	DA	DB	DC	DD	DE	DF
Condition True Jump	E0	E1	E2	E3	E4	E5	E6	E7
Condition False Jump	E8	E9	EA	EB	EC	ED	EE	EF
Input Block Transfer	F0	F1	F2	F3	F4	F5	F6	F7
Output Block Transfer	F8	F9	FA	FB	FC	FD	FE	FF

18XX-1FXX ENTER A WITH ADDRESS

	INSTRUCTION	REG. & CONTENTS		(MEMORY)	A_F
A.	1800	XXXX		XXXX	0000
B.	18F3	XXXX		XXXX	00F3
C.	1900	B1 – 2000		XXXX	2000
D.	1915	B1 – 1220		XXXX	1235
E.	1A00	B2 – 0CE1		XXXX	0CE1
F.	1AAA	B2 – 3502		XXXX	35AC
G.	1B00	P – 0005		XXXX	0005
H.	1B30	P – 0230		XXXX	0260
I.	1CAB	(0AB)	=	2304	2304
J.	1D53	B1 – 6015		1234	7249
K.	1EFA	B2 – FFFF		0987	0986
L.	1F02	P – 0A15		XXXX	0A13

20XX-27XX ENTER B1 WITH ADDRESS

	INSTRUCTION	REG. & CONTENTS	$B1_I$	(MEMORY)	$B1_F$
A.	2000	XXXX	XXXX	XXXX	0000
B.	20A6	XXXX	XXXX	XXXX	00A6
C.	2104	XXXX	2353	XXXX	2357
D.	2200	B2-503A	XXXX	XXXX	503A
E.	22F0	B2-1222	XXXX	XXXX	1312
F.	2300	P-F3C	XXXX	XXXX	0F3C
G.	2302	P-F02	XXXX	XXXX	0F04
H.	2417	XXXX	XXXX	CA45	CA45
I.	253A	XXXX	3405	2100	5505
J.	26C2	B2-A003	XXXX	1233	B236
K.	2610	B2-0000	XXXX	ABCD	ABCD
L.	2720	P-1AA	XXXX	XXXX	018A

28XX-2FXX ENTER B2 WITH ADDRESS

	INSTRUCTION	REG. & CONTENTS	$B2_1$	(MEMORY)	$B2_F$
A.	28FF	XXXX	XXXX	XXXX	00FF
B.	29AB	XXXX	A141	XXXX	A1EC
C.	2901	XXXX	FFFF	XXXX	0000
D.	2A01	B1-123B	XXXX	XXXX	123C
E.	2B30	P-924	XXXX	XXXX	0954
F.	2C75	XXXX	XXXX	1FF0	1FF0
G.	2C01	XXXX	XXXX	1031	1031
H.	2DFE	B1-0500	XXXX	1234	1734
I.	2D33	B1-FACE	XXXX	1000	0ACE
J.	2E41	XXXX	0001	CABB	CABC
K.	2F15	P-005	XXXX	XXXX	FFF0
L.	2FFF	P-200	XXXX	XXXX	0101

30XX-37XX TEST INDEX B1
38XX-3FXX TEST INDEX B2

	INSTRUCTION	(MEMORY)	REG.-INITIAL-FINAL	COND.BIT
A.	3045	6774	B1-6774-6774	TRUE
B.	3306	0504	B1-0503-0504	FALSE
C.	31AB	F3B6	B1-ABCD-ABCE	FALSE
D.	3817	8642	B2-8642-8642	TRUE
E.	3F08	1000	B2-1000-1000	TRUE
F.	3D00	0000	B2-FFFF-0000	FALSE

40XX-47XX LOAD A
48XX-4FXX LOAD A COMPLEMENT

2's Complement

INSTRUCTION	(MEMORY)	A_F
A. 4012	133A	133A
B. 4134	0509	0509
C. 4356	A034	A034
D. 4800	2A47	D5B9
E. 4C78	8000	8000
F. 4E9A	FFFE	0002

50XX-57XX LOAD LEFT-MOST BYTE
58XX-5FXX LOAD RIGHT-MOST BYTE

INSTRUCTION	(MEMORY)	A_F
A. 5013	1234	0012
B. 5259	5678	0056
C. 54BD	9ABC	009A
D. 58F1	DEF0	00F0
E. 5B21	0123	0023
F. 5F43	4567	0067

P3035

HO-31

60XX-67XX ADD
68XX-6FXX SUBTRACT

INSTRUCTION	(MEMORY)	A_I	A_F	A.G.BIT
A. 6019	2345	1492	37D7	FALSE
B. 6156	FFFF	0105	0104	TRUE
C. 64AB	AE17	6123	0F3A	TRUE
D. 6812	5321	A1A1	4E80	TRUE
E. 692A	0045	FEED	FEA8	TRUE
F. 6E69	8350	1492	9142	FALSE

P3035

HO-32

70XX-77XX EXCLUSIVE OR
78XX-7FXX LOGICAL PRODUCT

INSTRUCTION		(MEMORY)	A_I	A_F
A.	7036	FF00	5678	A978
B.	7223	8003	90AB	10A8
C.	74C6	0FF7	345B	3BAC
D.	78AB	0F00	6543	0500
E.	7C3A	3333	B217	3213
F.	7DFE	8000	1234	0000

80XX-87XX REPLACE ADD
88XX-8FXX REPLACE ADD ONE

	INSTRUCTION	A_1	$(MEMORY)_1$	A_F & $(MEMORY)_F$	A.G. BIT
A.	80A8	0200	1234	1434	FALSE
B.	83B6	FFFF	AEF3	AEF2	TRUE
C.	84C0	8000	7FFF	FFFF	FALSE
D.	88D4	XXXX	4567	4568	FALSE
E.	89E2	XXXX	FFFF	0000	TRUE
F.	8EF2	XXXX	0001	0002	FALSE

90XX-97XX REPLACE LEFT-MOST BYTE
98XX-9FXX REPLACE RIGHT-MOST BYTE

INSTRUCTION	A_1	$(MEMORY)_1$	A_F & $(MEMORY)_F$
A. 9014	1234	3A27	3427
B. 9121	59AE	1476	AE76
C. 9305	FFBB	680A	BB0A
D. 9861	24CE	0000	00CE
E. 9ECC	61AB	CDEF	CDAB
F. 9F11	29D0	3049	30D0

A0XX-A7XX STORE
A8XX-AFXX STORE ZEROS
B0XX-B7XX DESTRUCTIVE LOAD

INSTRUCTION	A_I	A_F	$(MEMORY)_I$	$(MEMORY)_F$
A. A025	1234	1234	XXXX	1234
B. A1F3	F302	F302	XXXX	F302
C. A86C	XXXX	XXXX	XXXX	0000
D. AB03	XXXX	XXXX	XXXX	0000
E. B0AC	XXXX	6FB3	6FB3	0000

B8XX-BFXX	UNCONDITIONAL JUMP
C0XX-C7XX	A ZERO JUMP
C8XX-CFXX	A NONZERO JUMP
D0XX-D7XX	A POSITIVE JUMP
D8XX-DFXX	A NEGATIVE JUMP
E0XX-E7XX	CONDITION TRUE JUMP
E8XX-EFXX	CONDITION FALSE JUMP

INSTRUCTION	A→ 0000	FFFF	1234	EDCC	8000	C.B.→ T	F
B800	M	M	M	M	M	M	M
C105	M	P+1	P+1	P+1	P+1	X	X
CA33	P+1	M	M	M	M	X	X
D3F0	M	P+1	M	P+1	P+1	X	X
DC21	P+1	M	P+1	M	M	X	X
E504	X	X	X	X	X	M	P+1
EE67	X	X	X	X	X	P+1	M

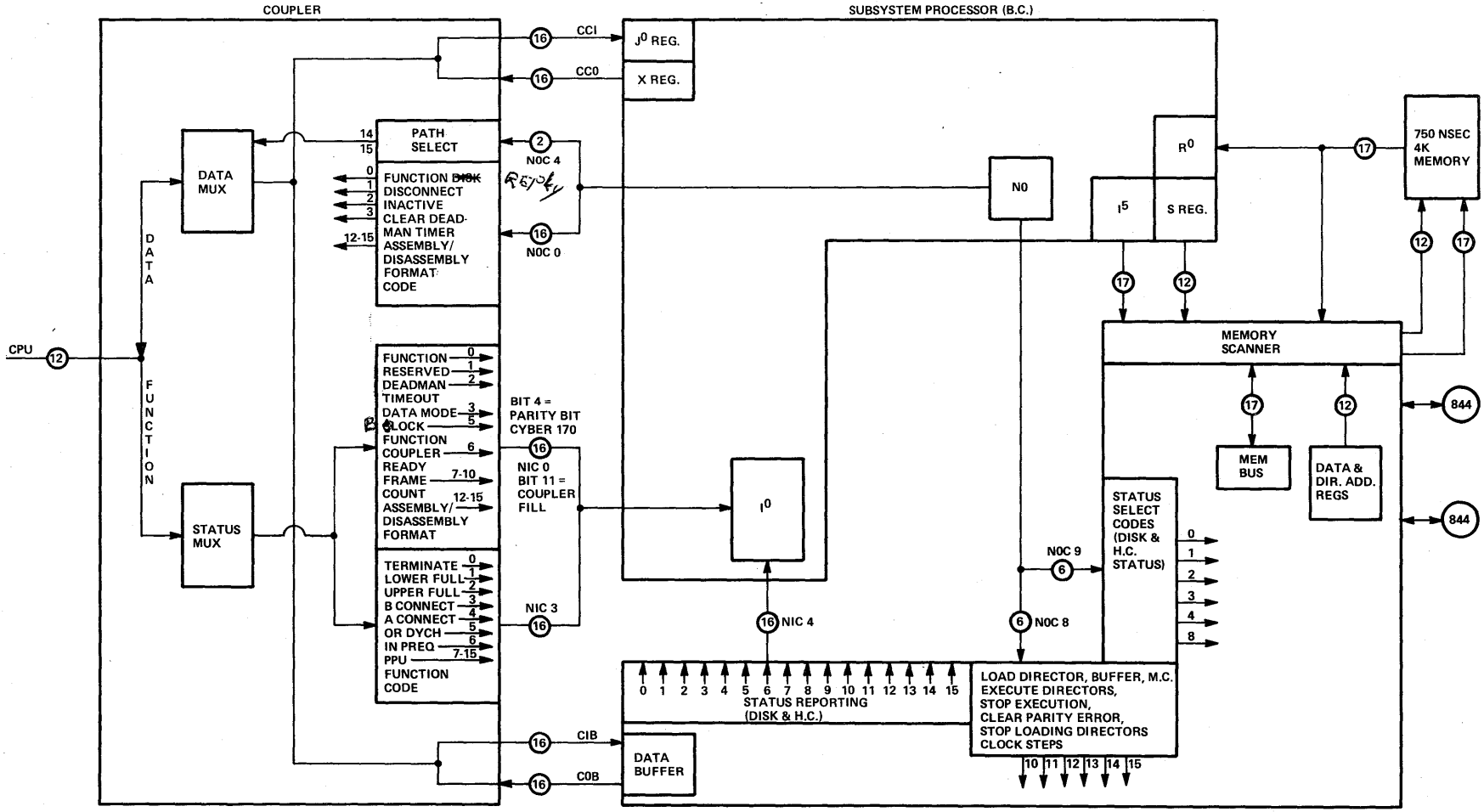
F0XX-F7XX INPUT BLOCK TRANSFER
F8XX-FFXX OUTPUT BLOCK TRANSFER

INSTRUCTION	READY	TERMINATE	A_I	A_F	TRANSFERS	COND BIT
A. F01A	YES	NO	FFFA	0000	6	TRUE
B. F130	NO	NO	FFFE	FFFE	0	FALSE
C. F3FE	YES	YES	FFF0	FFF3	3	FALSE
D. F800	YES	NO	FF00	0000	100_{16}	TRUE
E. FC07	DROPS	NO	FFF1	0000	F	TRUE
F. FEB0	YES	YES	0000	1234	1234	FALSE

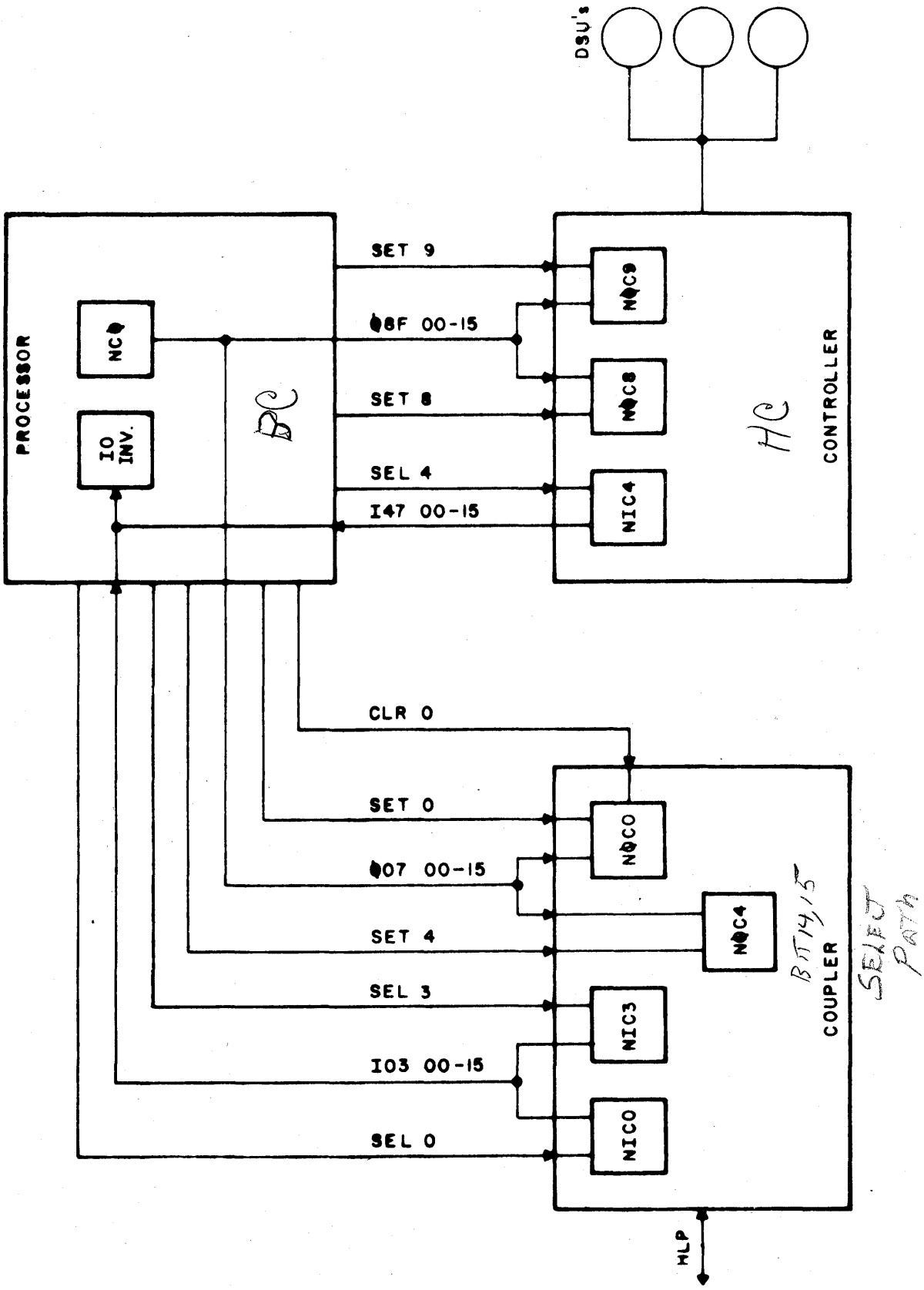
FA 722

6000 COUPLER

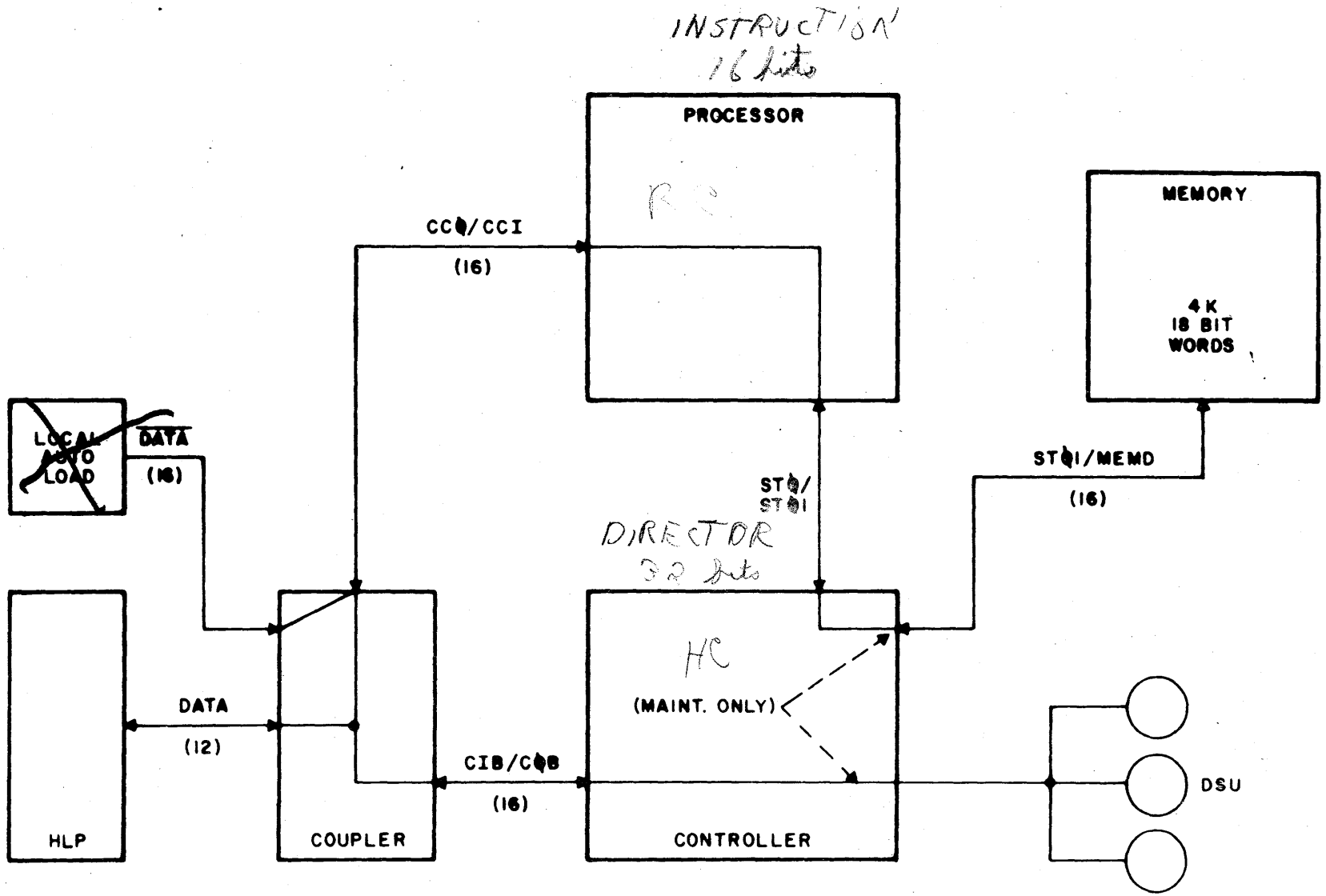
STUDENT HANDOUTS


COUPLER
SUBSYSTEM PROCESSOR (B.C.)
CCI
CC0
J0 REG.
X REG.
PATH SELECT
NOC 4
NOC 0
DATA MUX
FUNCTION DISK
DISCONNECT
INACTIVE
CLEAR DEAD-MAN TIMER
ASSEMBLY/ DISASSEMBLY FORMAT
CODE
DATA
FUNCTION
CPU
STATUS MUX
FUNCTION
RESERVED
DEADMAN TIMEOUT
DATA MODE
CLOCK
FUNCTION CODE
COUPLER READY
FRAME COUNT
ASSEMBLY/ DISASSEMBLY FORMAT
BIT 4 = PARITY BIT CYBER 170
NIC 0 BIT 11 = COUPLER FILL
TERMINATE
LOWER FULL
UPPER FULL
B CONNECT
A CONNECT
OR DYCH
IN PREQ
PPU
FUNCTION CODE
NIC 3
NIC 4
N0
I0
I5
S REG.
R0
750 NSEC 4K MEMORY
MEMORY SCANNER
MEM BUS
DATA & DIR. ADD. REGS
844
844
NOC 9
NOC 8
STATUS SELECT CODES (DISK & H.C. STATUS)
STATUS REPORTING (DISK & H.C.)
LOAD DIRECTOR, BUFFER, M.C.
EXECUTE DIRECTORS,
STOP EXECUTION,
CLEAR PARITY ERROR,
STOP LOADING DIRECTORS
CLOCK STEPS
CIB
C0B
DATA BUFFER

844 SYS NORMAL CHANNEL INTERFACE

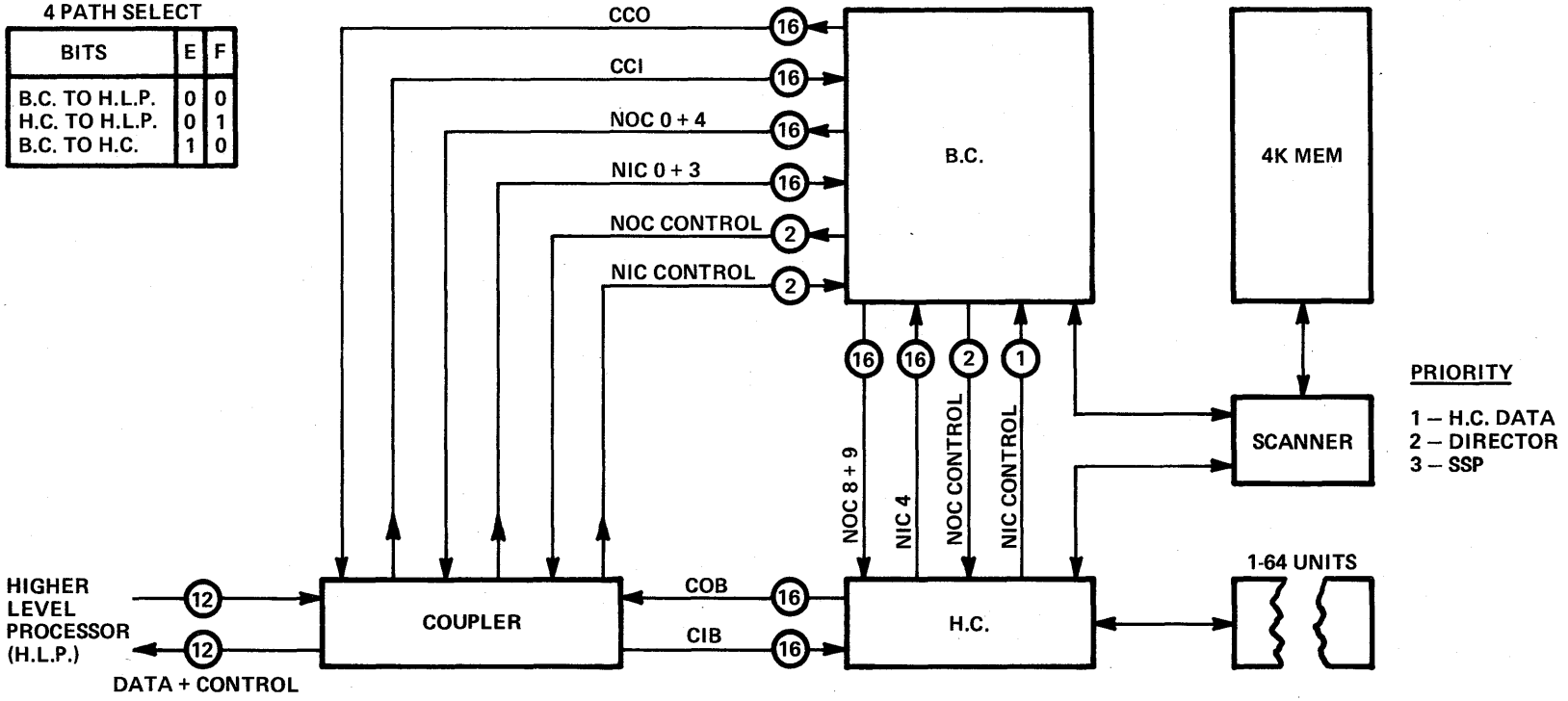


844 SYSTEM DATA PATHS

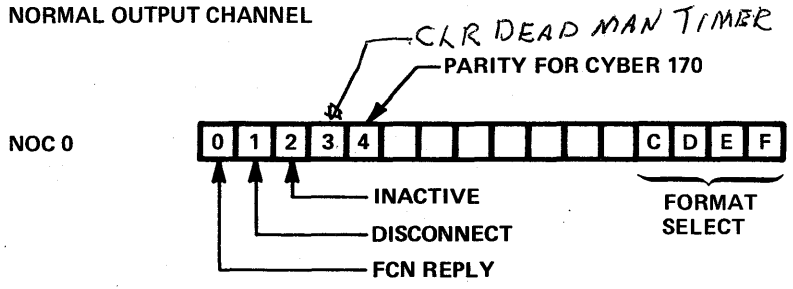


4 PATH SELECT

BITS	E	F
B.C. TO H.L.P.	0	0
H.C. TO H.L.P.	0	1
B.C. TO H.C.	1	0



NORMAL OUTPUT CHANNEL



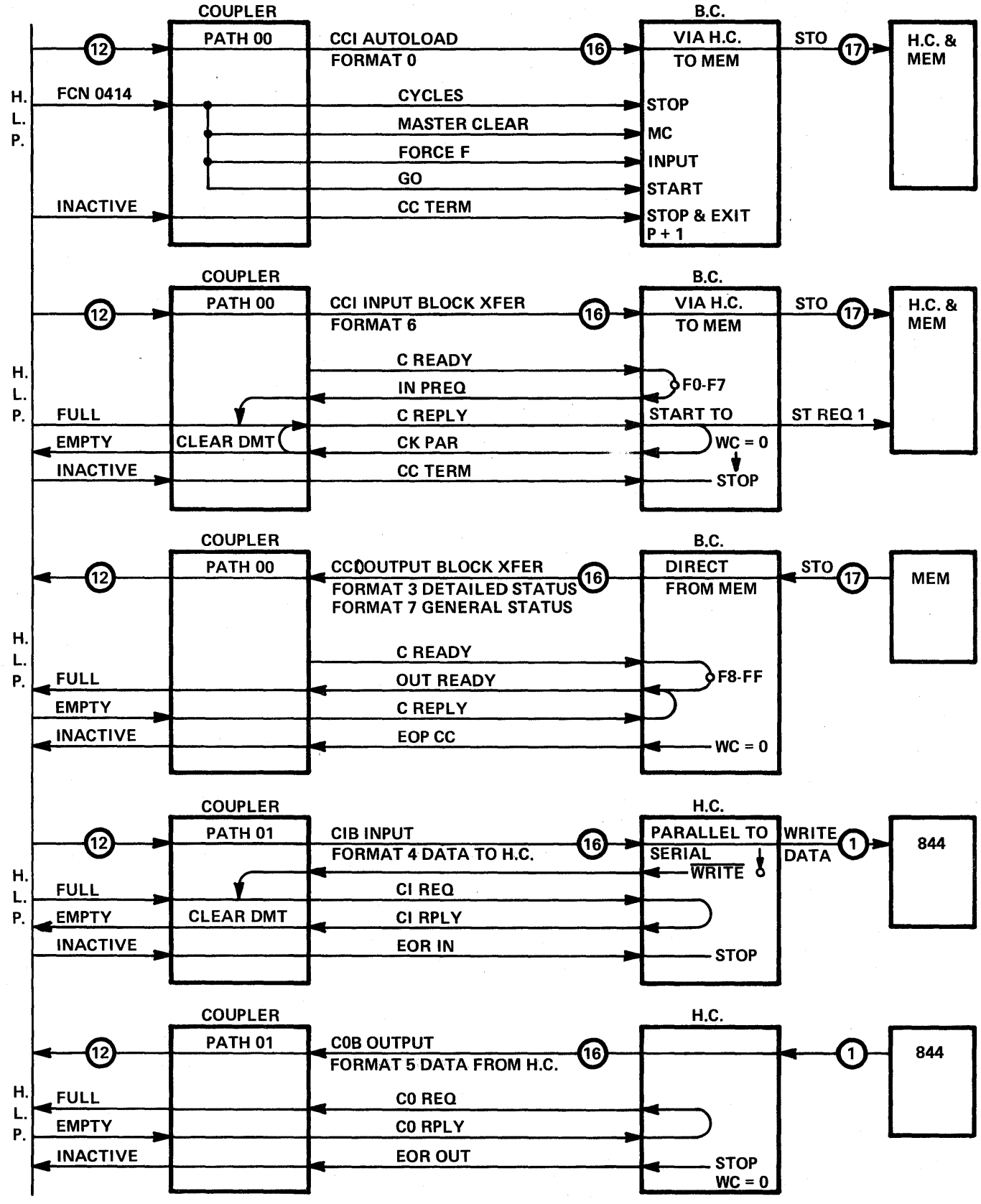
NOC 4 PATH SELECT
NOC 8 H.C. FUNCTION (BITS 10-15)
NOC 9 H.C. STATUS SELECT CODE

NORMAL INPUT CHANNEL

NIC 0 COUPLER STATUS
BIT 0 = FCN PRESENT
BIT 1 = RESERVED
BIT 2 = DEADMAN TIMEOUT
BIT 6 = COUPLER READY
NIC 3 H.L.P. FUNCTION CODE (BITS 7-F)
NIC 4 H.C. STATUS TO SSP

B-C

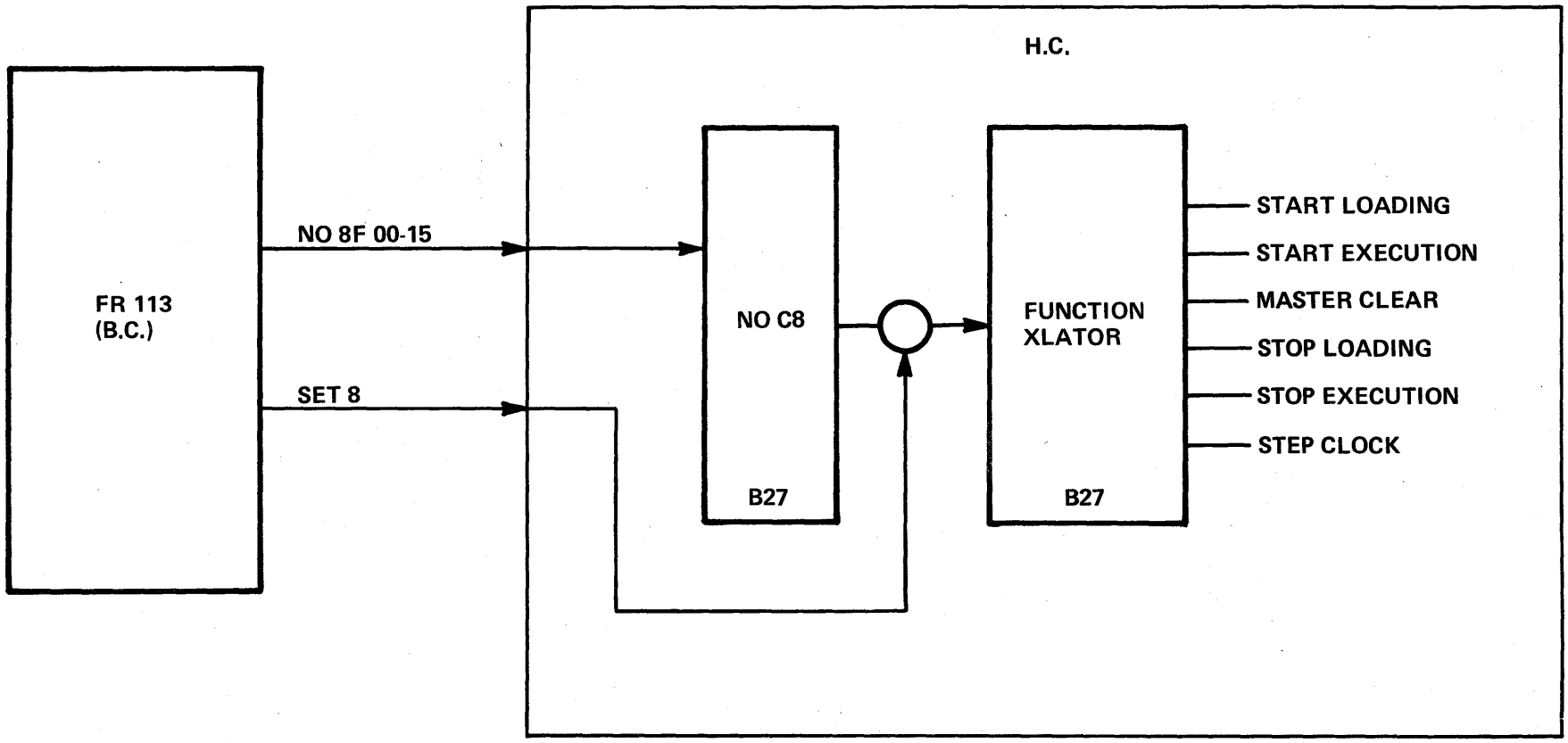
BIT 4 PARITY ERROR (170)


COUPLER
PATH 00
B.C.
VIA H.C.
TO MEM
STO
H.C. & MEM
12
16
17
CCI AUTOLOAD
FORMAT 0
H.
L.
P.
FCN 0414
CYCLES
STOP
MASTER CLEAR
MC
FORCE F
INPUT
GO
START
INACTIVE
CC TERM
STOP & EXIT
P + 1
CCI INPUT BLOCK XFER
FORMAT 6
C READY
IN PREQ
F0-F7
FULL
C REPLY
START TO
ST REQ 1
EMPTY
CLEAR DMT
CK PAR
WC = 0
STOP
CCO OUTPUT BLOCK XFER
FORMAT 3 DETAILED STATUS
FORMAT 7 GENERAL STATUS
DIRECT
FROM MEM
MEM
OUT READY
F8-FF
EOP CC
PATH 01
H.C.
CIB INPUT
FORMAT 4 DATA TO H.C.
PARALLEL TO
SERIAL
WRITE
WRITE
DATA
1
844
CI REQ
CI RPLY
EOR IN
C0B OUTPUT
FORMAT 5 DATA FROM H.C.
C0 REQ
C0 RPLY
EOR OUT

HARDWARE CONTROLLER

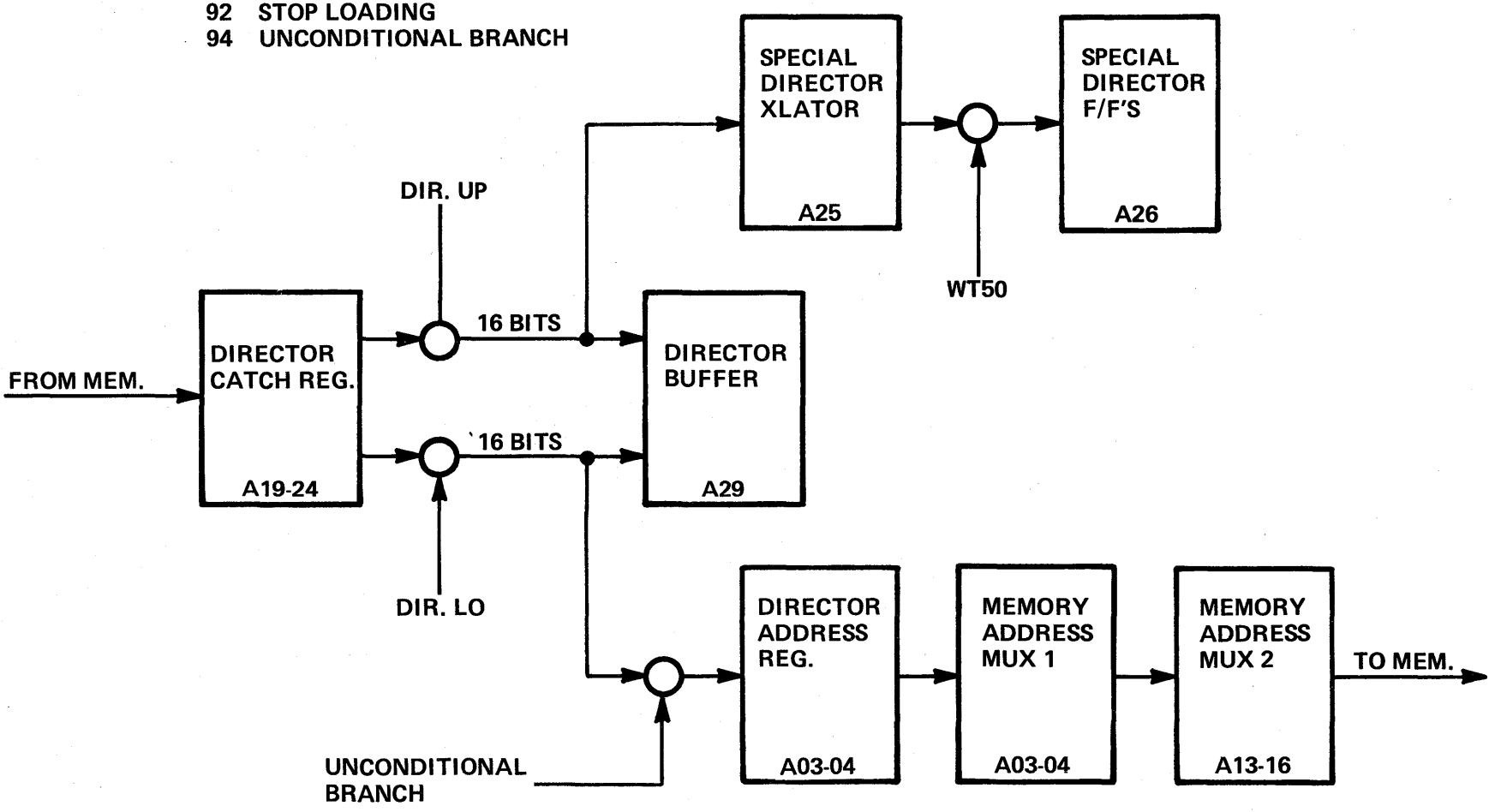
HANDOUTS

B.C./H.C. FUNCTIONS

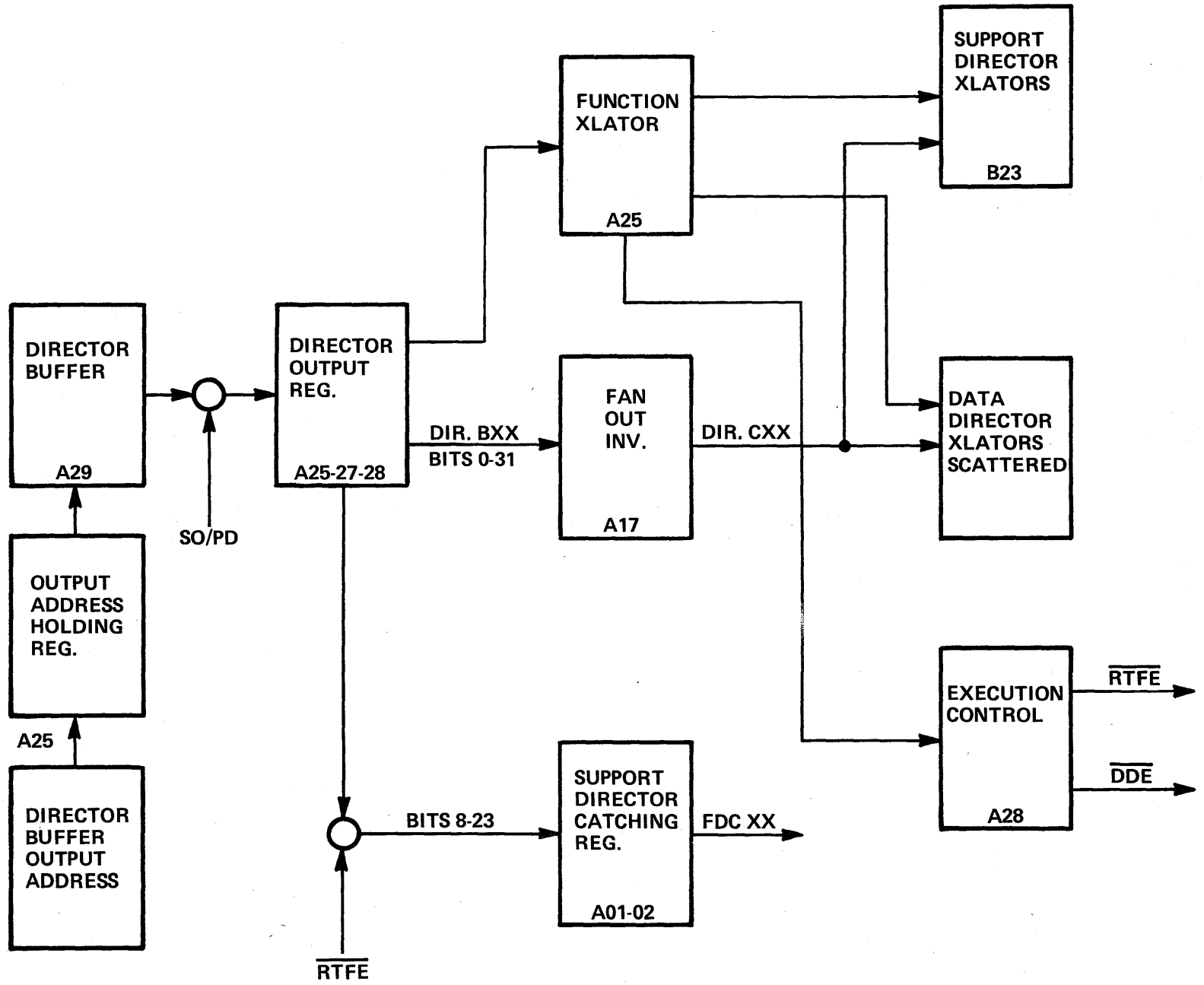


SPECIAL DIRECTOR LOADING

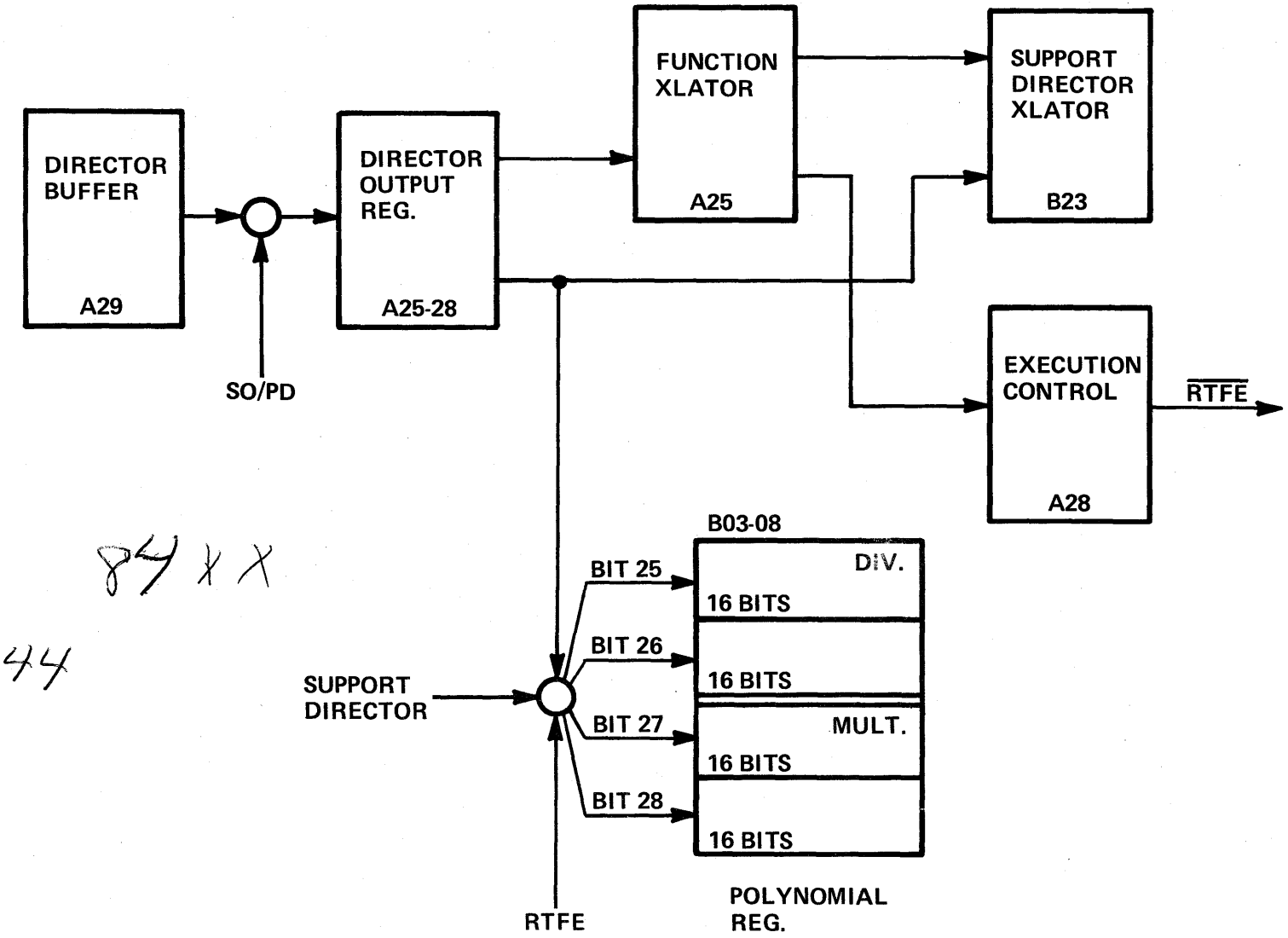
02 ADDRESS
08 TERMINATE
92 STOP LOADING
94 UNCONDITIONAL BRANCH



DIRECTOR EXECUTE



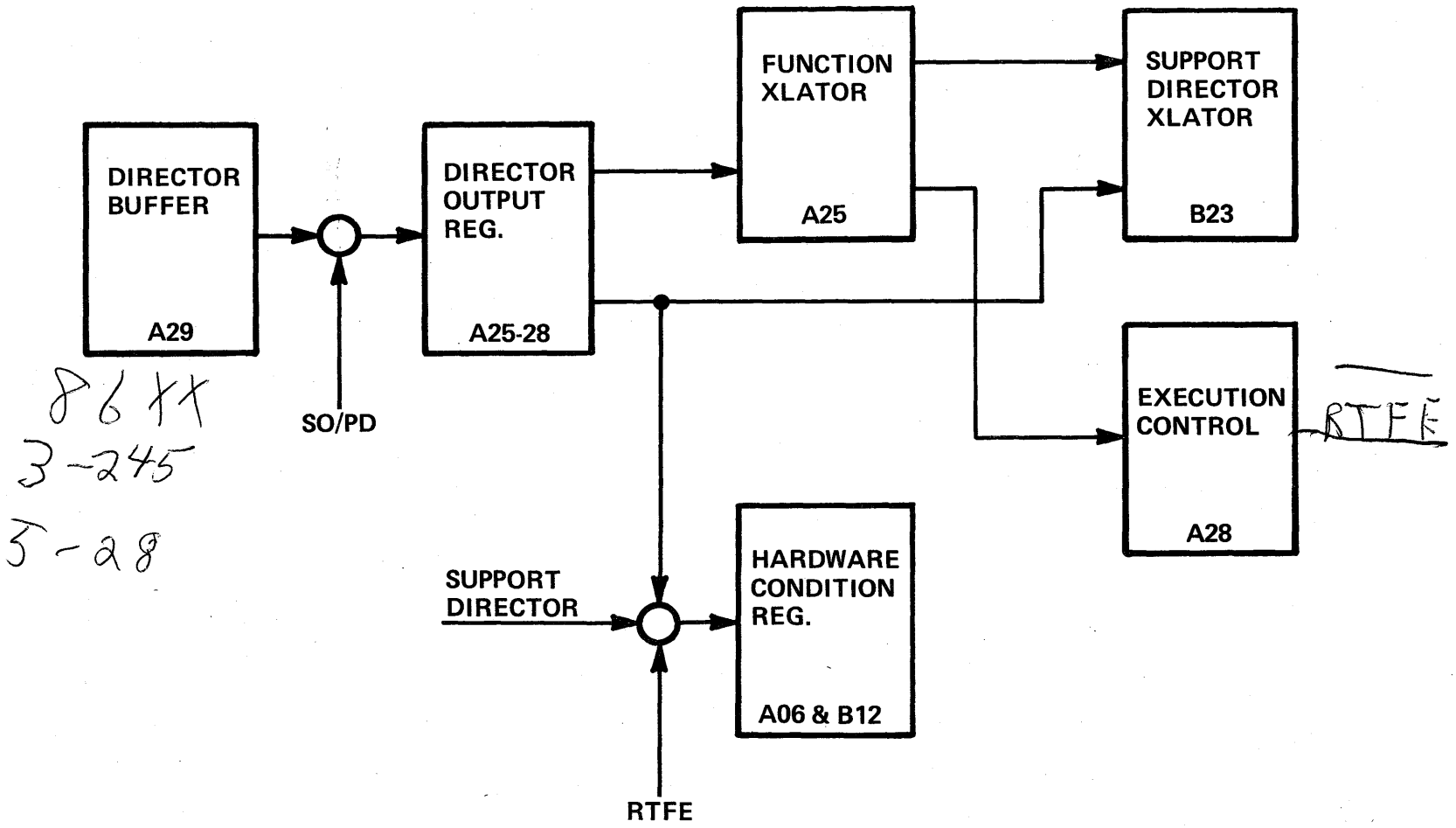
LOAD POLYNOMIAL



84 X X

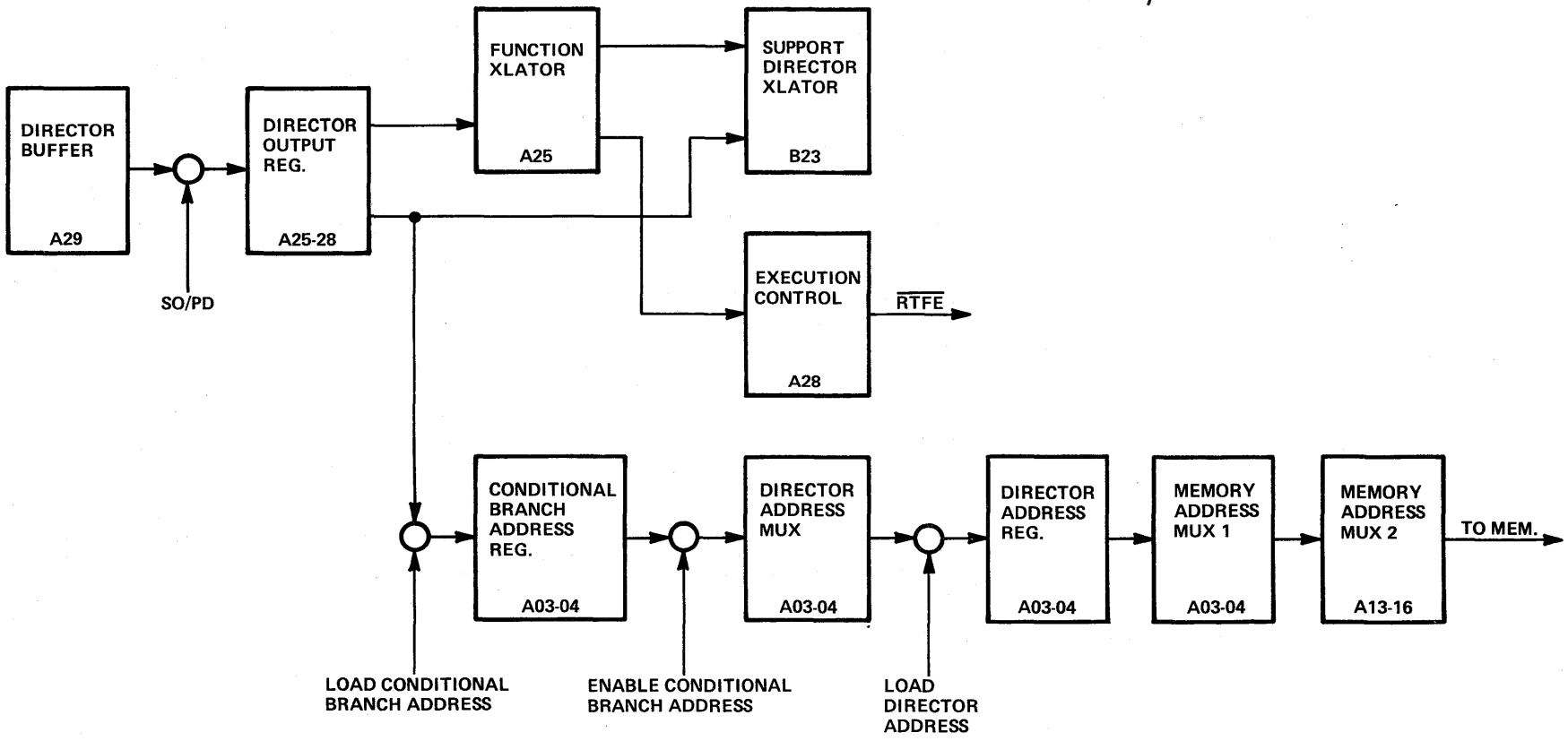
3-244

LOAD HARDWARE CONDITION



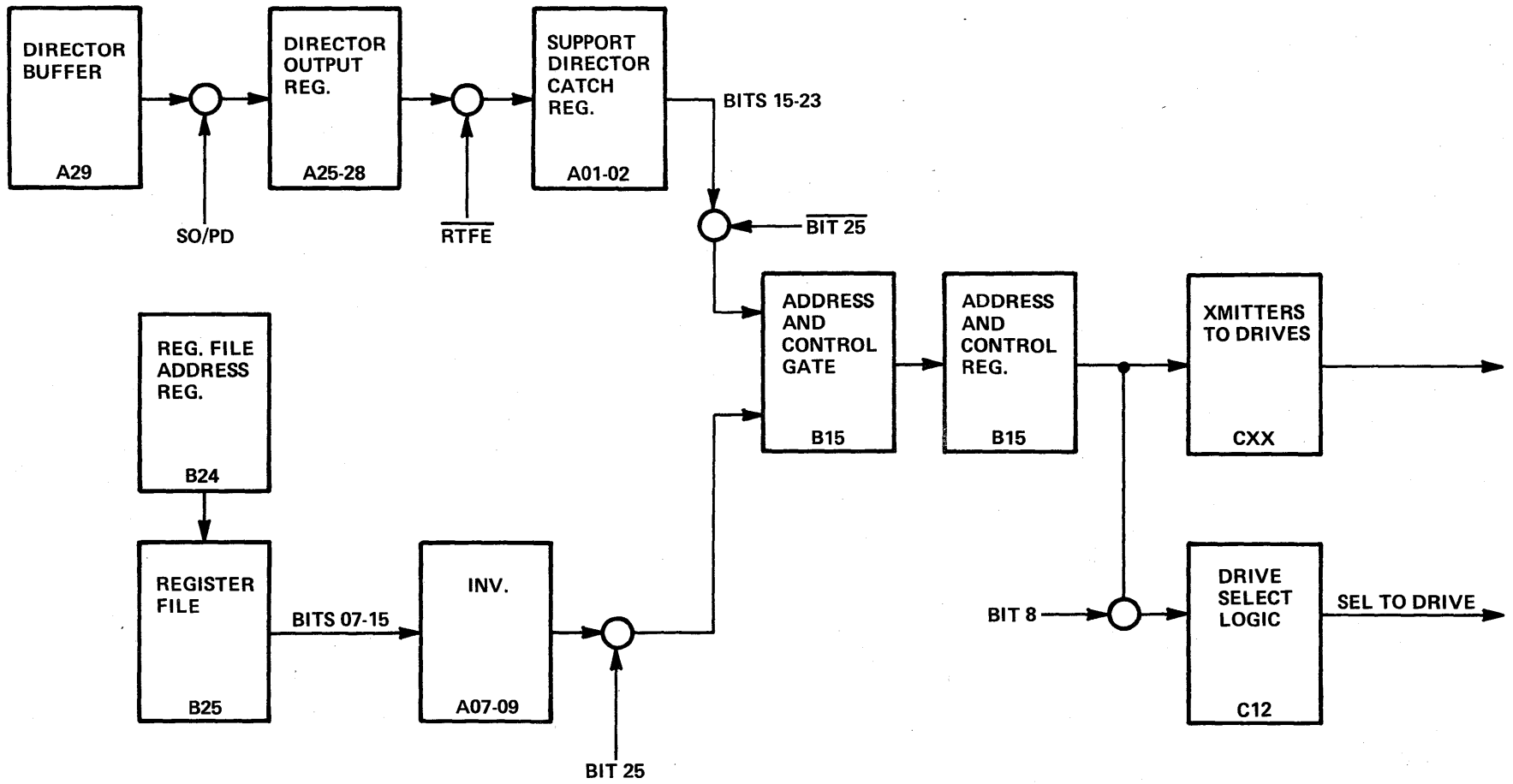
CONDITIONAL BRANCH

04 XX
5-21
3-229



Co 5-37
3-250

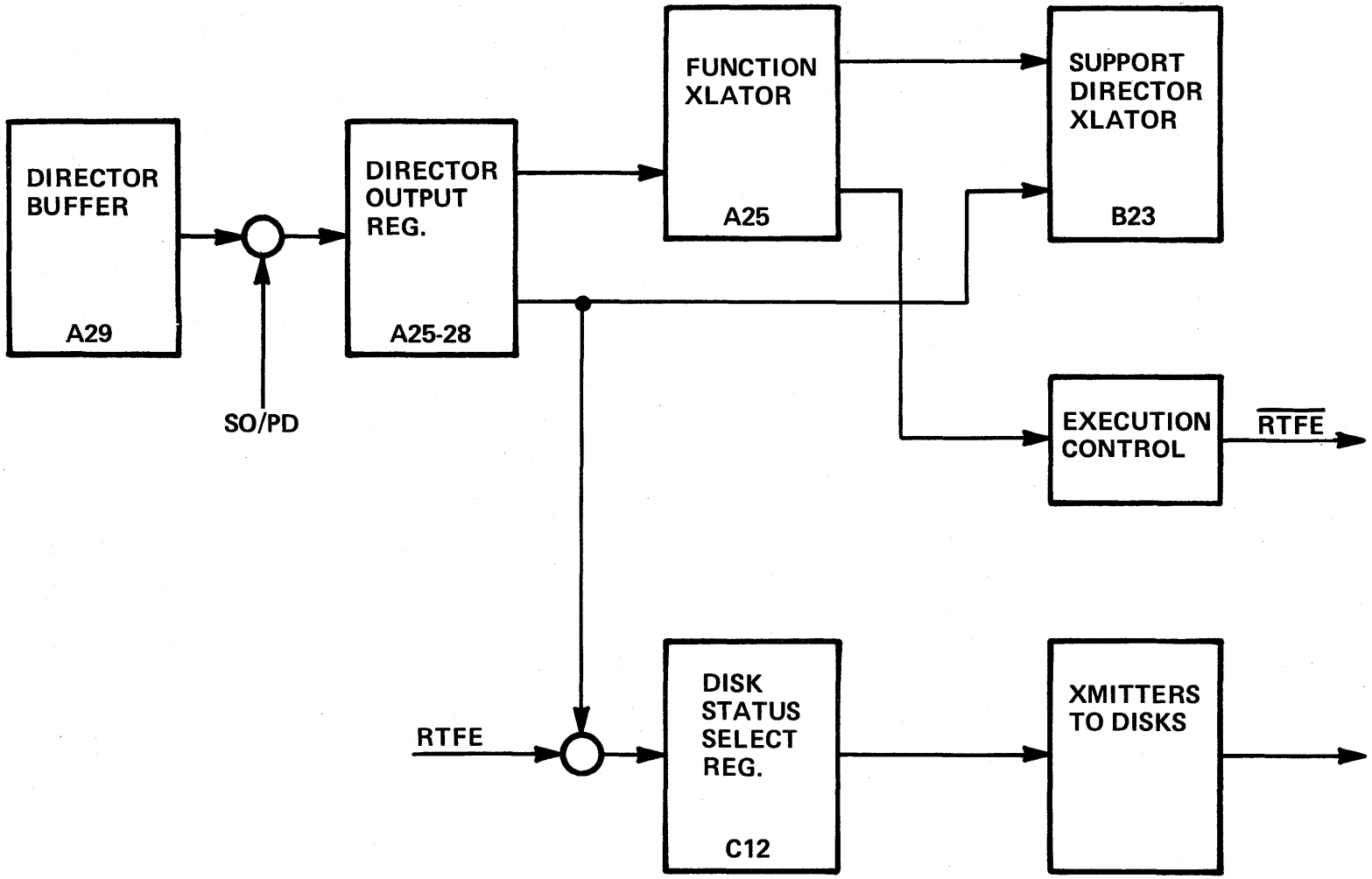
ENABLE DISK FUNCTION
(ALSO DISABLE CONTROL SEL) = C8



ENABLE/DISABLE DISK STATUS

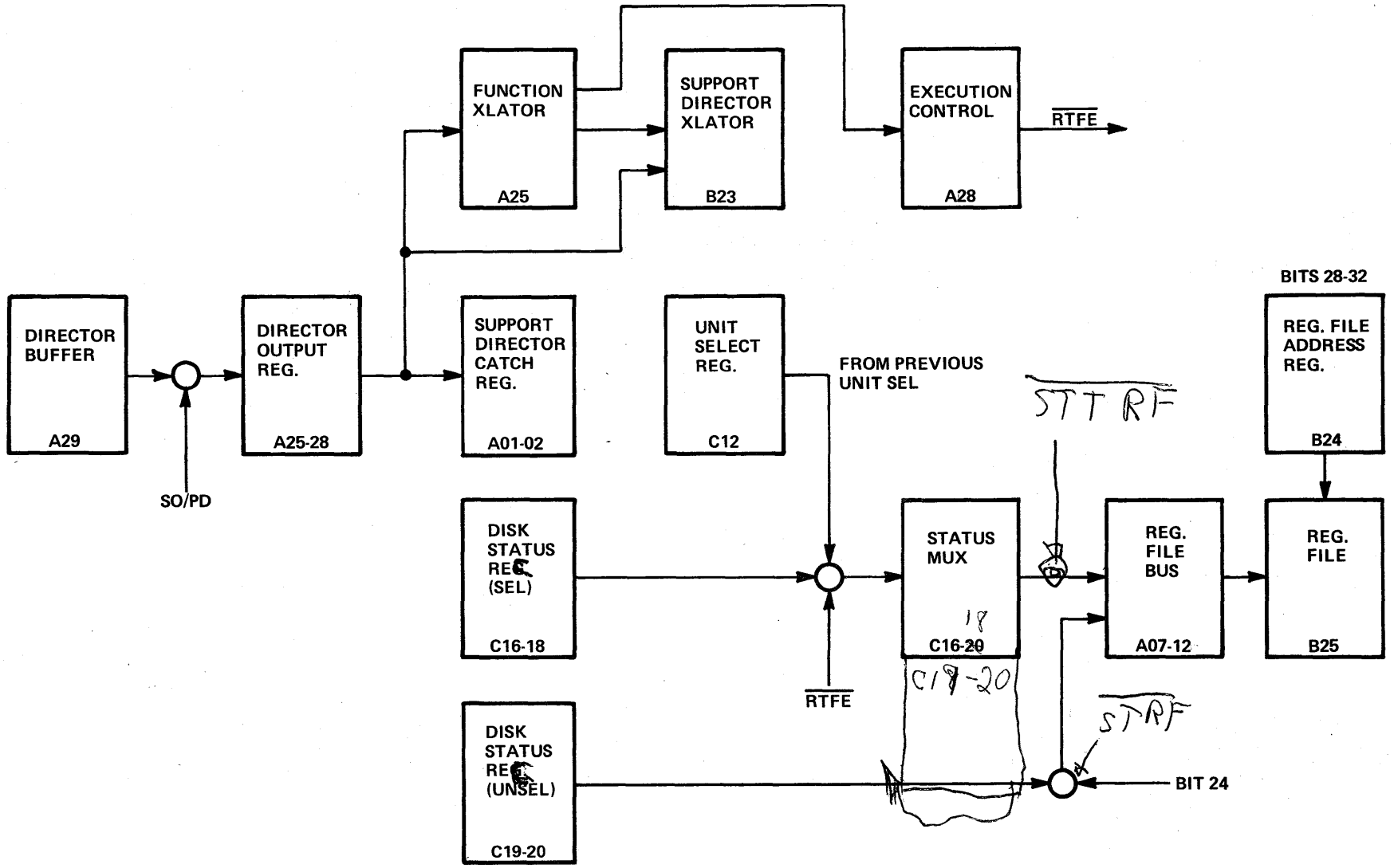
E 0
E 8

5 - 40
3 - 256

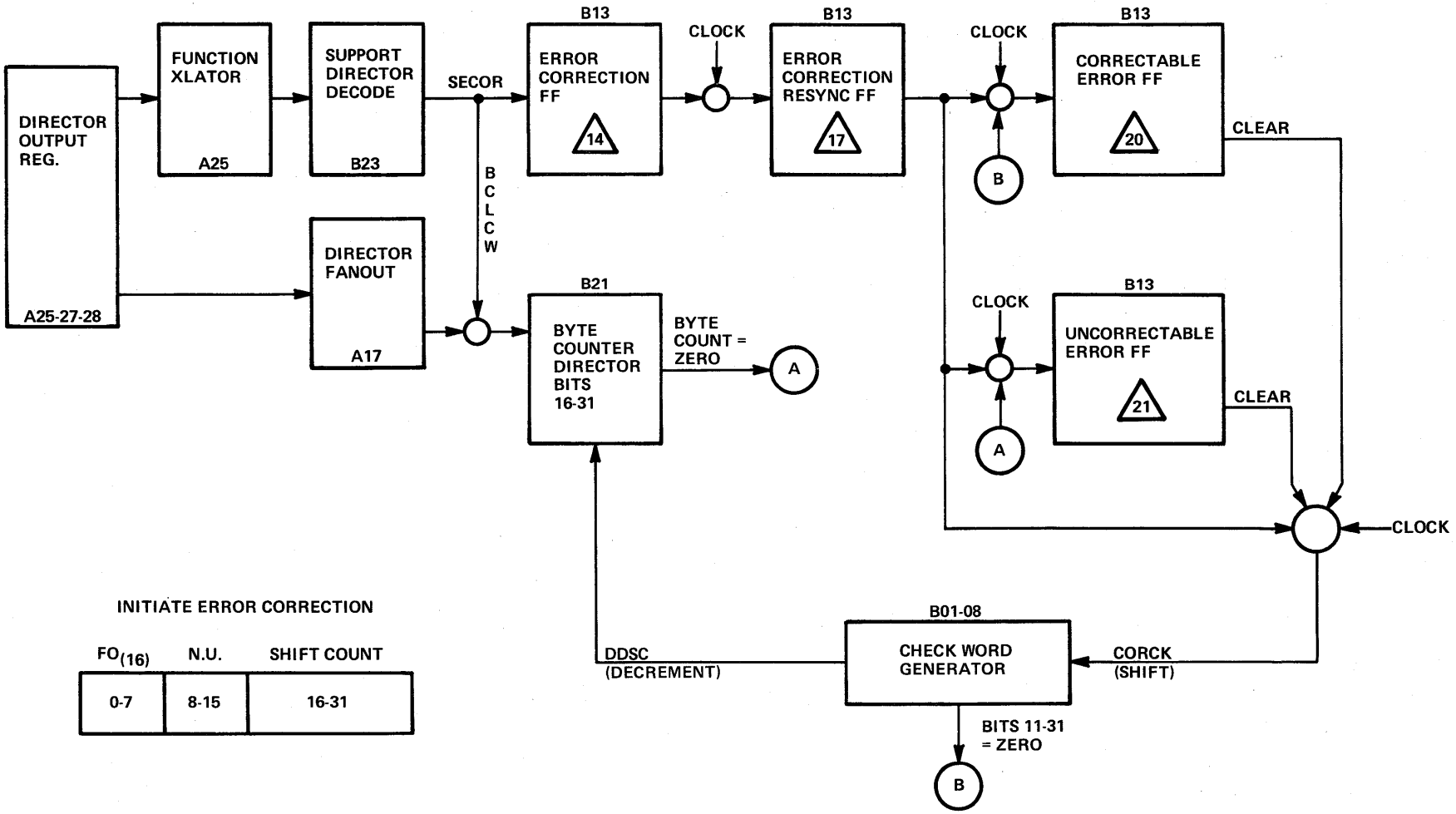


COPY DISK STATUS 88

5-28



5-41
3-256



HO-54

P3035

PROGRAM TO LOAD & EXECUTE DIRECTORS
ALREADY IN B.C. MEMORY AT LOCATION 0000

```
1820
0F80   M.C.                                  Load in at any location
                                             above 007F

1818   Start Loading                         Load Directors you want
0F80   Directors                             starting at 0000

2000
14XX   Delay
EF01

1822   Start Executing
0F80   Directors

2000
14XX   Delay
EF01

BF0C   Uncond. Jump to M.C.
```

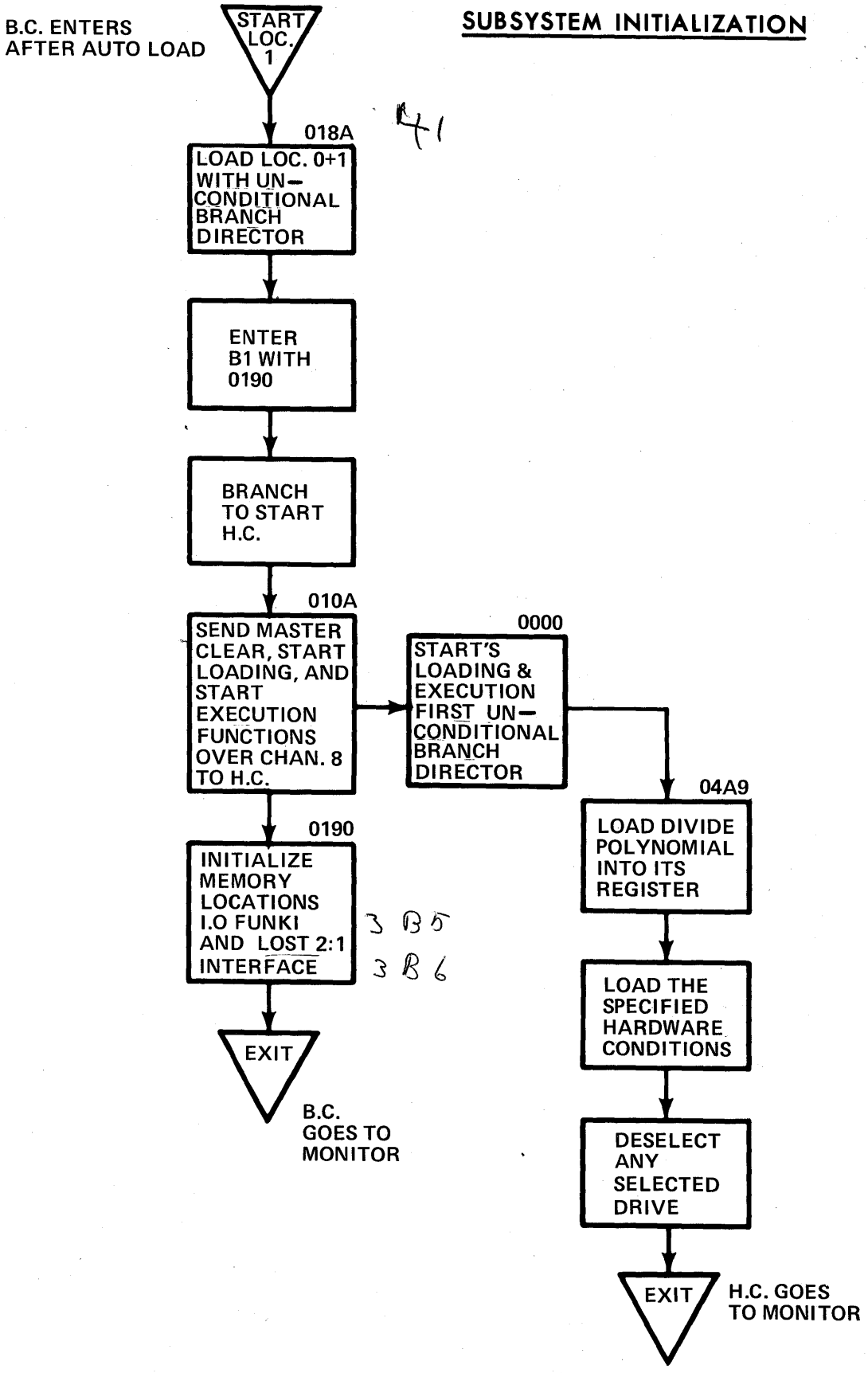
1820 - Enters A to equal 0020
0F80 - Transfers A to Output Channel 8 where 0020 tells DDS to Master Clear

1818 - Enters A to equal 0018
0F80 - Transfers A to Output Channel 8 where 0018 tells DDC to start loading Directors.
2000 - Enters B1 to equal 0000
14XX - Tests Index Reg. B, adding 1 to B, 1RNI to jump inst., and adding
EF01 1 to B, again until B, equals XX of 14XX inst. Delay is to allow Director Buffer Register to fill somewhat.
1822 - Enters A to equal 0022.
0F80 - Transfers A to Output Channel 8 where 0022 tells DDC to start executing first Director loaded
2000
14XX - Delay to allow execution of Directors.
EF01
BF0C - Unconditional jump backwards to 1820 (M.C. Inst.)

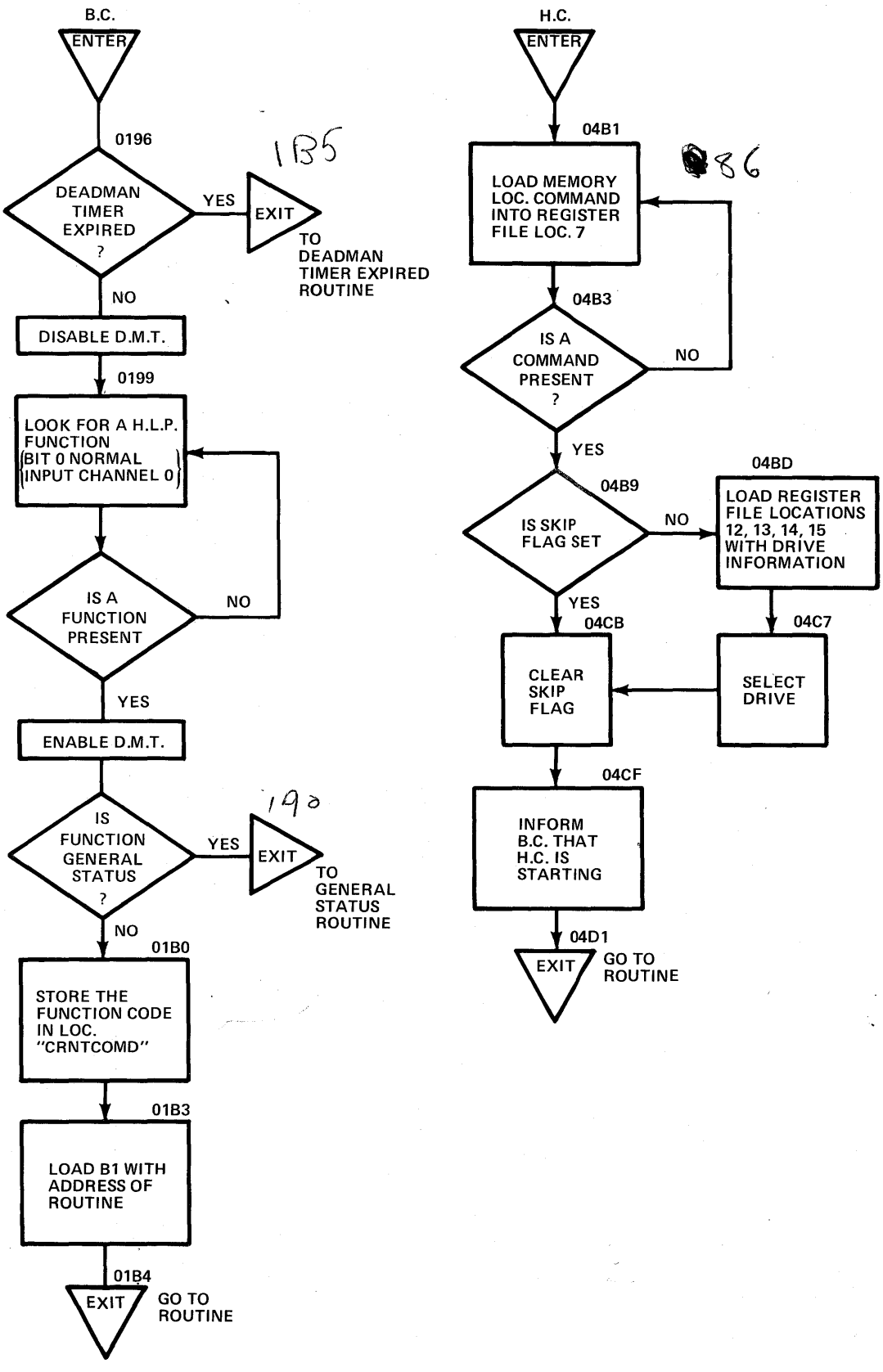
CORE MAP "A05" CONTROLWARE

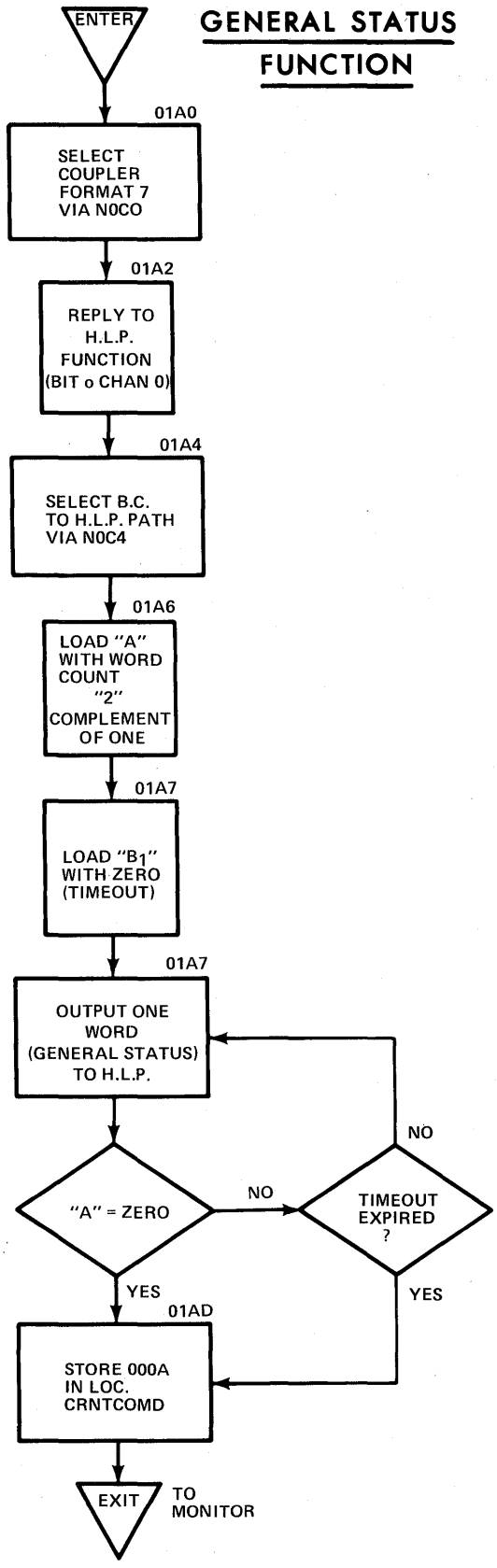
MEM. ADD.	MEMORY LOCATION CONTENTS	LISTING PAGE NO.
000 001	START UP INSTRUCTIONS	25
	RESERVED FOR AUTO DUMP	26
016	SELECTED DRIVE INFORMATION (DRIVE NUMB., CYL, TRACK, SECTOR)	26
01F	PREVIOUS OPERATION DRIVE INFORMATION	26
024	DETAILED STATUS WORDS	26
02D	B.C. ROUTING POINTERS	27
04F	H.C. ROUTINE POINTERS	27
	DIRECT CELLS AND FLAG WORDS	28
05A	GENERAL STATUS WORD	
05B	D.C. FLAG	
063	COMMAND	
074	H.L.P. FUNCTION POINTERS	30
094	MISCELLANEOUS DIRECT CELLS	31
099	CRNTCOMD	
100	RESTART	33
101	B.C. AND H.C. FUNCTION ROUTINES	34
10A	MASTER CLEAR AND START H.C.	35
18A	B.C. INITIALIZATION	41
196	B.C. MONITOR	42
4B1	H.C. MONITOR	86
663	ERROR RECOVERY ROUTINES	109
ACD	FORMAT ROUTINES	166
FFB	CONTROLWARE I.D.	217

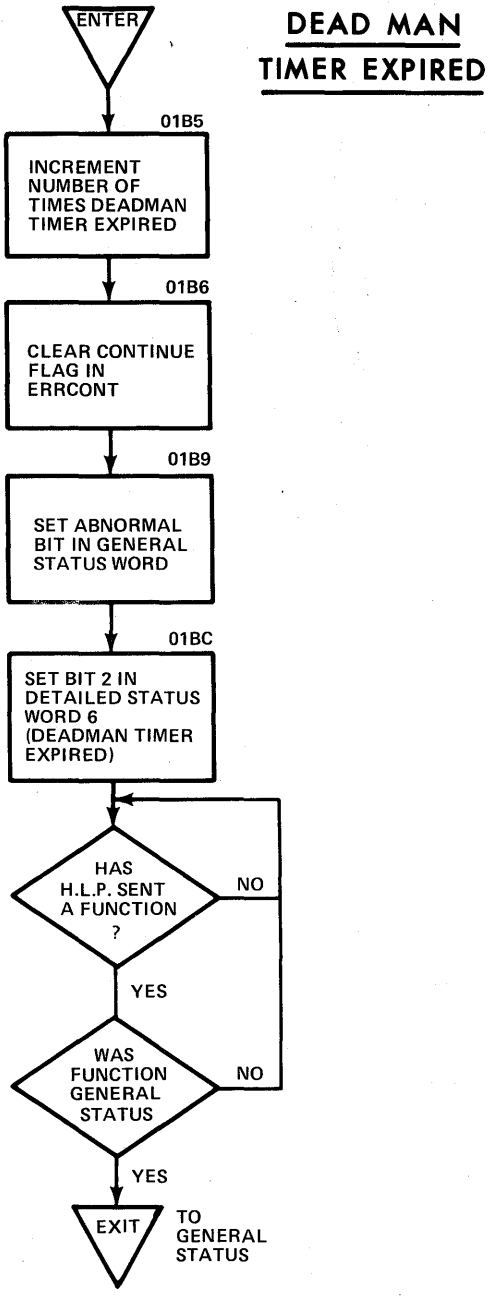
SUBSYSTEM INITIALIZATION



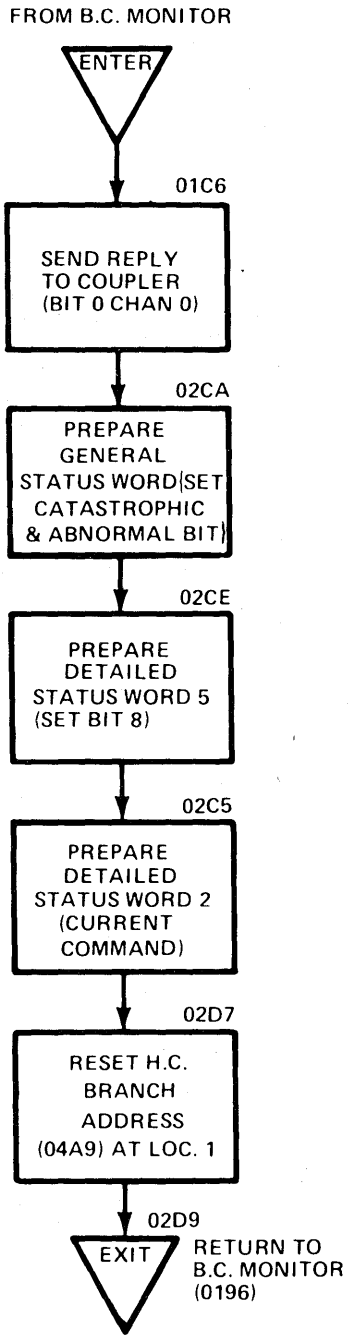
MONITOR LOOPS



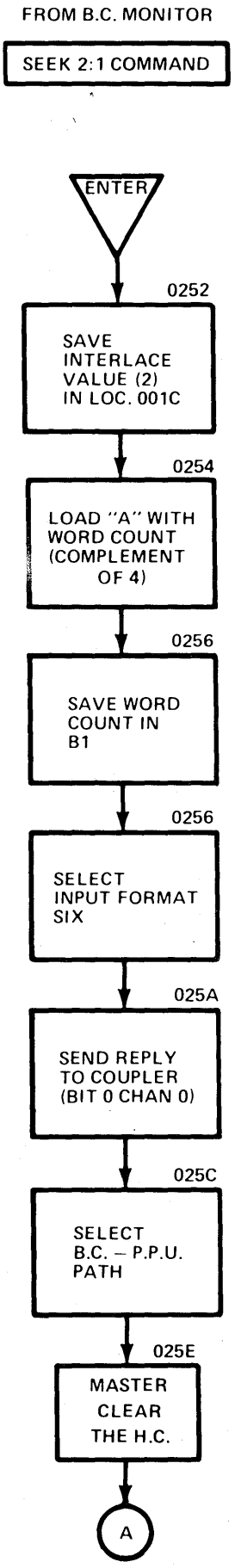

ENTER
GENERAL STATUS FUNCTION
01A0
SELECT COUPLER FORMAT 7 VIA N0CO
01A2
REPLY TO H.L.P. FUNCTION (BIT o CHAN 0)
01A4
SELECT B.C. TO H.L.P. PATH VIA N0C4
01A6
LOAD "A" WITH WORD COUNT "2" COMPLEMENT OF ONE
01A7
LOAD "B1" WITH ZERO (TIMEOUT)
01A7
OUTPUT ONE WORD (GENERAL STATUS) TO H.L.P.
"A" = ZERO
NO
TIMEOUT EXPIRED ?
NO
YES
YES
01AD
STORE 000A IN LOC. CRNTCOMD
EXIT
TO MONITOR

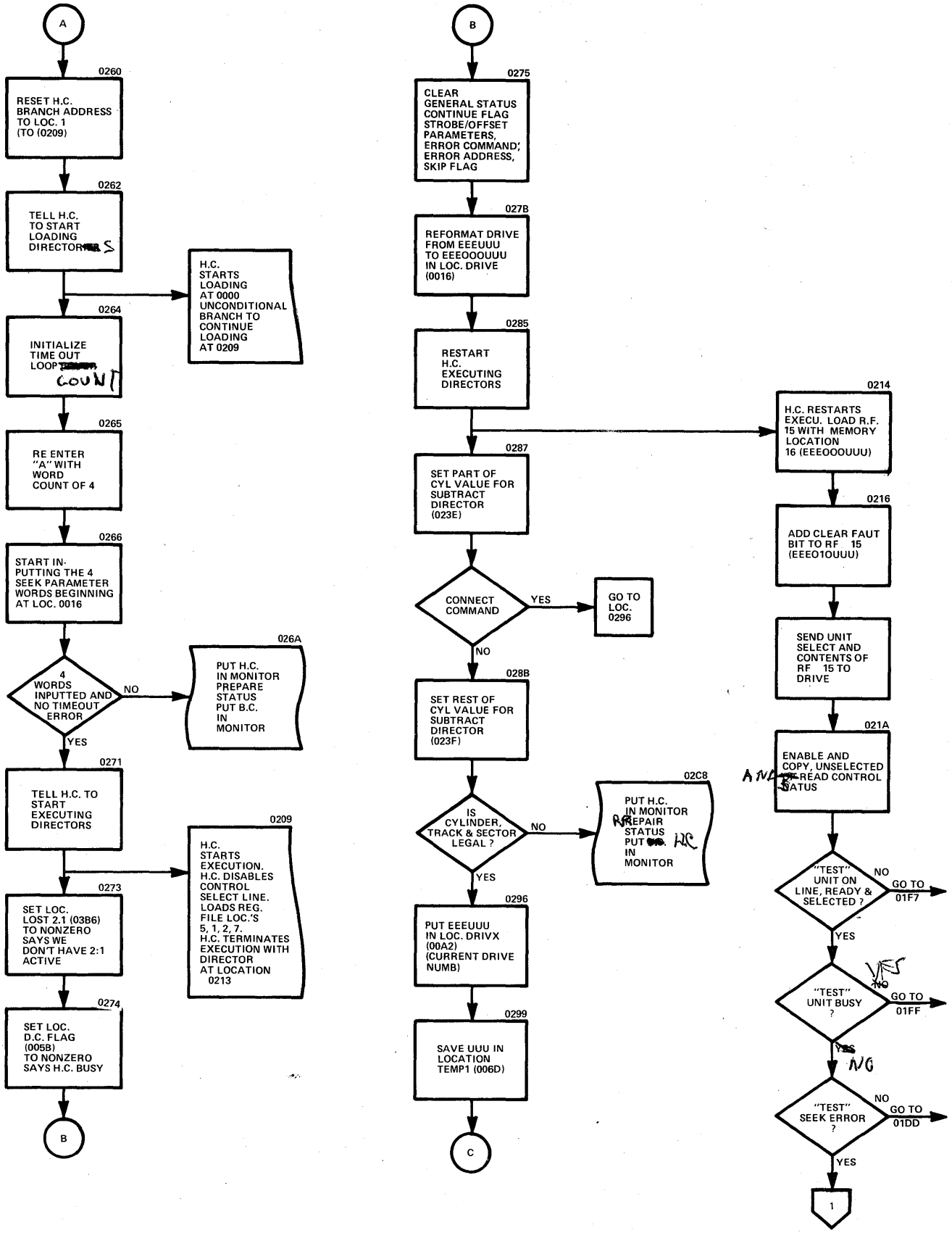

ENTER
DEAD MAN TIMER EXPIRED
01B5
INCREMENT NUMBER OF TIMES DEADMAN TIMER EXPIRED
01B6
CLEAR CONTINUE FLAG IN ERRCONT
01B9
SET ABNORMAL BIT IN GENERAL STATUS WORD
01BC
SET BIT 2 IN DETAILED STATUS WORD 6 (DEADMAN TIMER EXPIRED)
HAS H.L.P. SENT A FUNCTION ?
NO
YES
WAS FUNCTION GENERAL STATUS
NO
YES
EXIT
TO GENERAL STATUS

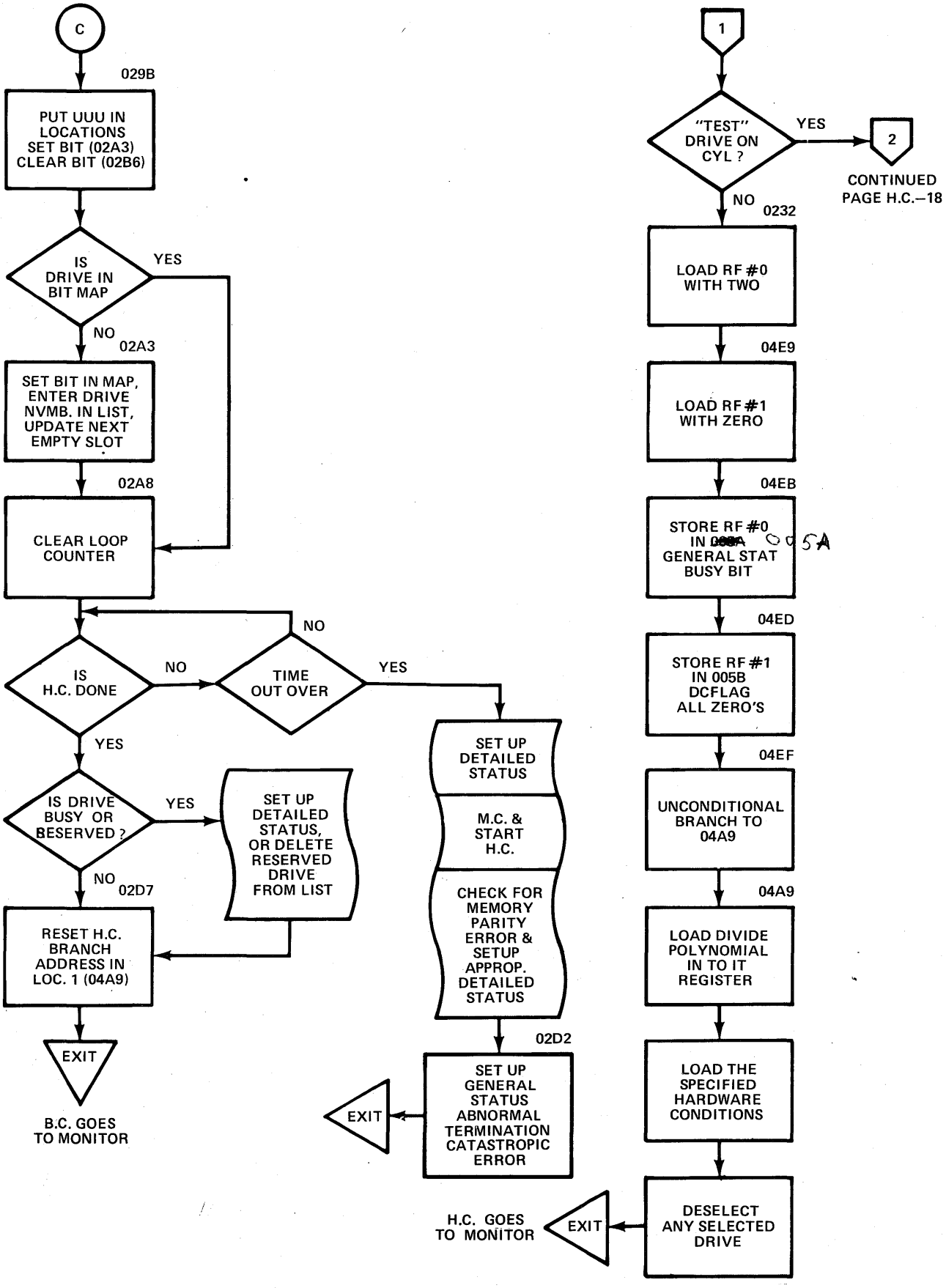
INVALID COMMAND

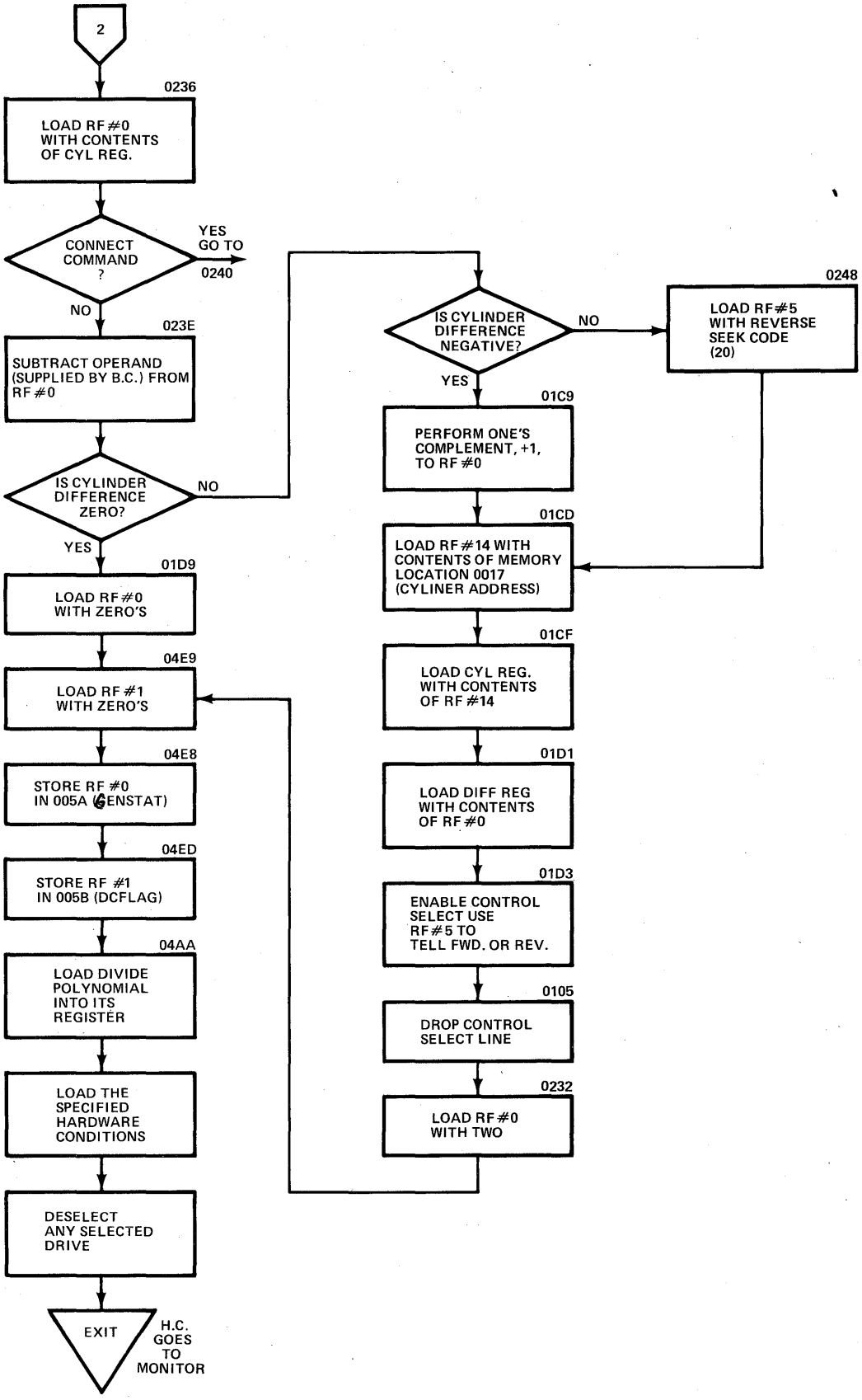


LEGAL COMMAND




A
0260
RESET H.C. BRANCH ADDRESS TO LOC. 1 (TO (0209)
0262
TELL H.C. TO START LOADING DIRECTORS
H.C. STARTS LOADING AT 0000 UNCONDITIONAL BRANCH TO CONTINUE LOADING AT 0209
0264
INITIALIZE TIME OUT LOOP COUNT
0265
RE ENTER "A" WITH WORD COUNT OF 4
0266
START IN-PUTTING THE 4 SEEK PARAMETER WORDS BEGINNING AT LOC. 0016
4 WORDS INPUTTED AND NO TIMEOUT ERROR
NO
026A
PUT H.C. IN MONITOR PREPARE STATUS PUT B.C. IN MONITOR
YES
0271
TELL H.C. TO START EXECUTING DIRECTORS
0209
H.C. STARTS EXECUTION. H.C. DISABLES CONTROL SELECT LINE. LOADS REG. FILE LOC.'S 5, 1, 2, 7. H.C. TERMINATES EXECUTION WITH DIRECTOR AT LOCATION 0213
0273
SET LOC. LOST 2.1 (03B6) TO NONZERO SAYS WE DON'T HAVE 2:1 ACTIVE
0274
SET LOC. D.C. FLAG (005B) TO NONZERO SAYS H.C. BUSY
B
B
0275
CLEAR GENERAL STATUS CONTINUE FLAG STROBE/OFFSET PARAMETERS, ERROR COMMAND, ERROR ADDRESS, SKIP FLAG
027B
REFORMAT DRIVE FROM EEEUUU TO EEEOOOUUU IN LOC. DRIVE (0016)
0285
RESTART H.C. EXECUTING DIRECTORS
0214
H.C. RESTARTS EXECU. LOAD R.F. 15 WITH MEMORY LOCATION 16 (EEEOOOUUU)
0287
SET PART OF CYL VALUE FOR SUBTRACT DIRECTOR (023E)
0216
ADD CLEAR FAUT BIT TO RF 15 (EEEO1OUUU)
CONNECT COMMAND
YES
GO TO LOC. 0296
NO
SEND UNIT SELECT AND CONTENTS OF RF 15 TO DRIVE
028B
SET REST OF CYL VALUE FOR SUBTRACT DIRECTOR (023F)
021A
ENABLE AND COPY, UNSELECTED READ CONTROL STATUS
02C8
IS CYLINDER, TRACK & SECTOR LEGAL ?
NO
PUT H.C. IN MONITOR REPAIR STATUS PUT IN MONITOR
"TEST" UNIT ON LINE, READY & SELECTED ?
NO
GO TO 01F7
YES
YES
0296
PUT EEEUUU IN LOC. DRIVX (00A2) (CURRENT DRIVE NUMB)
"TEST" UNIT BUSY ?
NO
GO TO 01FF
YES
0299
SAVE UUU IN LOCATION TEMP1 (006D)
"TEST" SEEK ERROR ?
NO
GO TO 01DD
YES
C
1


C
029B
PUT UUU IN LOCATIONS SET BIT (02A3) CLEAR BIT (02B6)
IS DRIVE IN BIT MAP
YES
NO
02A3
SET BIT IN MAP, ENTER DRIVE NVMB. IN LIST, UPDATE NEXT EMPTY SLOT
02A8
CLEAR LOOP COUNTER
IS H.C. DONE
NO
TIME OUT OVER
NO
YES
YES
IS DRIVE BUSY OR BESERVED ?
YES
SET UP DETAILED STATUS, OR DELETE RESERVED DRIVE FROM LIST
NO
02D7
RESET H.C. BRANCH ADDRESS IN LOC. 1 (04A9)
EXIT
B.C. GOES TO MONITOR
SET UP DETAILED STATUS
M.C. & START H.C.
CHECK FOR MEMORY PARITY ERROR & SETUP APPROP. DETAILED STATUS
02D2
SET UP GENERAL STATUS ABNORMAL TERMINATION CATASTROPIC ERROR
EXIT
H.C. GOES TO MONITOR
1
"TEST" DRIVE ON CYL ?
YES
2
CONTINUED PAGE H.C.–18
NO
0232
LOAD RF #0 WITH TWO
04E9
LOAD RF #1 WITH ZERO
04EB
STORE RF #0 IN 005A GENERAL STAT BUSY BIT
04ED
STORE RF #1 IN 005B DCFLAG ALL ZERO'S
04EF
UNCONDITIONAL BRANCH TO 04A9
04A9
LOAD DIVIDE POLYNOMIAL IN TO IT REGISTER
LOAD THE SPECIFIED HARDWARE CONDITIONS
DESELECT ANY SELECTED DRIVE
EXIT


2
0236
LOAD RF#0 WITH CONTENTS OF CYL REG.
CONNECT COMMAND ?
YES GO TO 0240
NO
023E
SUBTRACT OPERAND (SUPPLIED BY B.C.) FROM RF#0
IS CYLINDER DIFFERENCE ZERO?
NO
YES
01D9
LOAD RF#0 WITH ZERO'S
04E9
LOAD RF#1 WITH ZERO'S
04E8
STORE RF#0 IN 005A (GENSTAT)
04ED
STORE RF#1 IN 005B (DCFLAG)
04AA
LOAD DIVIDE POLYNOMIAL INTO ITS REGISTER
LOAD THE SPECIFIED HARDWARE CONDITIONS
DESELECT ANY SELECTED DRIVE
EXIT
H.C. GOES TO MONITOR
IS CYLINDER DIFFERENCE NEGATIVE?
NO
0248
LOAD RF#5 WITH REVERSE SEEK CODE (20)
YES
01C9
PERFORM ONE'S COMPLEMENT, +1, TO RF#0
01CD
LOAD RF#14 WITH CONTENTS OF MEMORY LOCATION 0017 (CYLINER ADDRESS)
01CF
LOAD CYL REG. WITH CONTENTS OF RF#14
01D1
LOAD DIFF REG WITH CONTENTS OF RF#0
01D3
ENABLE CONTROL SELECT USE RF#5 TO TELL FWD. OR REV.
0105
DROP CONTROL SELECT LINE
0232
LOAD RF#0 WITH TWO

7 X 54 STUDENT LAB GUIDE

SUBJECT: Cyber System Lab Exercise

REFERENCE SOURCE: Volume 2 Hardware Maintenance Manual, Section 4

OBJECTIVE: The student will become familiar with the clock tuning procedure for the coupler

1. Locate the coupler that you are going to use for this exercise.

   Prepare a dual trace scope and locate it next to the coupler.

   It is a _____type coupler.

2. To check the clocks, you must cause the PPU to send repeated functions to the coupler. The easiest way to do this is to use the Deadstart Panel. Create a deadstart program to do this. Record it below and set it into the deadstart switches. Start it running.

3. Go to the coupler. Locate the clock tuning procedure in Section 4 of the manual.

4. Instructor will place problems in coupler. Use C.I.D. and C.D.M. and coupler isolation guide to find problem.

SUBSYSTEM PROCESSOR - WORKSHEETS

1. Solve the following Hexidecimal Addition problems.

{1}	5002 0227 5229	{2}	AF02 1245 C147	{3}	2377 15FF 3976	{4}	8100 9011 11111	{5}	ABCD 1234 BE01
{6}	0006 FFFE 10004	{7}	0105 CCCC CPD1	{8}	CAFE BCDE 187DC	{9}	FACE 4333 13E01	{10}	F07A C5D3 1564D

2. Solve the following Hexidecimal Subtraction problems.

{1}	3210 1022 21EE	{2}	1600 00FF 1501	{3}	F07A 609F 8FDB	{4}	3789 308D 06FC	{5}	FFFF 7ACE 8531
{6}	CAFE ABCE 1F30	{7}	4567 3F4D 061A	{8}	FACE 9D6B 5063	{9}	2D6E 1A7F 12EF	{10}	5BD6 3A21 2185

3. What is the 2's complement of "F638"?
09C8

4.
000	0103
001	010B
002	0107
003	010F
004	0302
005	030B
006	0300
007	0306
008	0201
009	0209
00A	020B
00B	020F
00C	0000

{A}F= B200

SUBSYSTEM PROCESSOR - WORKSHEET

5. What will be the $\{A\}_F$ when executing A "0400" in each case?

	$\{A\}_I$	$\{A\}_F$
a.	0123	0007
b.	FEED	0000
c.	0008	000C
d.	0034	000A
e.	0000	0010
f.	24A0	0002

6. What will be the $\{A\}_F$?

	Instruction	$\{A\}_I$		$\{A\}_F$
a.	0503	3402	=	0680
b.	050A	1234	=	0004
c.	0506	AB40	=	2AD0
d.	0581	0001	=	8000
e.	058D	0600	=	0000
f.	0585	0015	=	8000

7.

000	0308	
001	0605	$\{A\}_F$ = 0080
002	0713	$\{B1\}_F$ = 0004
003	1485	$\{B2\}_F$ = 0094
004	1596	Condition
005	0000	Bit = Clear

SUBSYSTEM PROCESSOR - WORKSHEET

8. Given: NIC No. 9 = 0123 NOC No. A = 00FF

000	10F0	
001	0820 → C.B. =	
002	099F → C.B. =	
003	0840 → C.B. =	
004	0BAC	
005	0EA8	
006	1101	
007	0820 → C.B. =	
008	0811 → C.B. =	
009	0000	

{A}F = 00EF

{NOCA}F = 0007

ADD GEN BIT =

9.

000	B802
001	0000
002	C004
003	0000
004	C806
005	B807
006	0000
007	D009
008	0000
009	D80B
00A	D80C
00B	0000
00C	000D

{P}F = 000C

SUBSYSTEM PROCESSOR - WORKSHEET

10.

000	1000
001	6106
002	3309
003	EF02
004	A40A
005	0000
006	ABCD
007	1576
008	FF2F
009	3105
00A	000C
00B	0003
00C	0000

{P}F = 0006
{A}F = ABCD
{B1}F = 0001
Cond. Bit = Clr
Add. Gen. Bit = Clr
{00A}F = 000C
{00B}F = 0003
{00C}F = ABCD

11. To transfer data from "X" register to "A" register the data flow would be through?

X → I2 → I4 → I45 → A

12. To input data from the coupler to memory, the data path would be?

JO → I5 DATA REG

13. To shift the "A" register the data flow would be from "A" to shift network to "A" register.

14. The following arithmetic will set or clear the Adder Gen. Bit.

8F32	0325	FFFE	0006
+9032	-0002	+0001	-0053
{SET/CLR}	{SET/CLR}	{SET/CLR}	{SET/CLR}
SET	SET	CLR	SET

SUBSYSTEM PROCESSOR - WORKSHEET

15. The two internal flags in the subsystem processor are?

16. The adder generate bit denotes? over flow

17. The Data Flow for a "06XX" instruction is?

18. If the subsystem processor reads up the instruction "1106" the "X" register would contain _____.

19.

000	2408
001	1900
002	13FF
003	0840
004	E302
005	7304
006	0F20
007	0000
008	1234
009	0100

{A}F = _____

{B1}F = _____

{NOC2}F = _____

{P}F = _____

Condition Bit = _____

20.

000	4001
001	6905
002	2101
003	D702
004	0000
005	0123
006	1234
007	2345
008	3456
009	4567

{A}F = _____

{B1}F = _____

{P}F = _____

Add. Gen. Bit = _____

SUBSYSTEM PROCESSOR - WORKSHEET

21. The sequences for the following instructions are:

    a. 60XX = RNI ROP
    b. 61XX = RNI ROP
    c. A0XX = RNI STO
    d. A4XX = RADR STO
    e. 8CXX = RNI RADR-ROP-STO

22. In order to set a "175H" clocked flip-flop the "D" input must be a logical one/zero and a up clock/down clock on "C" input. one up clock

23. A "507" {1 of 10 decoder} output is active with a one/zero.

24. To have the sequence active the state of the following flip-flops must be. {Set or Clear} {A20}

    a. RNI-1 and RNI-2 clr.
    b. RADR set.
    c. ROP-1 and ROP-2 set.
    d. STO-1 and STO-2 set.

25. To enable setting the "RADR"FF {A20} the function register must contain? X 4 5 6 7 XX

26. $\overline{\text{RNI-NX}}$ will equal a logic one when? {A20}
RADR ROP STO = 1

27. In the direct address mode what terms enable "M" to the adder?
X RF 122

28. During relative addressing why is "M" added or subtracted from "S" register and not "P" register?
S has current address and can be gated to the adder

29. The "strip" term {A23} will output a logic one for a {050X/058X} instruction.

058X

30. For the instruction "058A" terms {A23}

RSI-SN will = 1

RS2-SN will = 0

RS4-SN will = 1

ENRS8 will = 0

31. List the format one instructions that use the shift register gates.

010X 05 08

32. During format one instructions "CLKAR" {A19} will be active at time T10 when ENI4AR term is a zero.

33. During no address instructions {except for "17XX" instruction} RNI-1 and RNI-2FF are always Set/Clear.

Clear

34. If the subsystem processor executes a load "A" complement instruction, with the contents of a memory location containing "56B2", what will the result in "A" be?

A94E

35. The Data Flow for a "90XX" instruction is:

mem → X I2.ADRER = I4

A shift network - I45 A I5 MEM

36. What are the three basic functions of the load byte FF? (A20)

1. RS8-SN Right shift 8
2. Enable By Clock A reg at time 5
3. Load By Gate Rank 4 → Rank 5 of shift network

SUBSYSTEM PROCESSOR - WORKSHEET

37. The Data Flow for a "40XX" instruction is "X" register To I2 To ADDR To F4 To I45 To "A" register.

38. On a conditional jump indirect, there is no use wasting time getting a jump address, if the condition is not met. What term stops entering the RADR cycle?

ENRAQ = 0

39. What term stops "CLKB1" from going to a zero during a "30XX" instruction if B1 equals the contents of the execution address?

ENI4B1 = 1

40. During a "17XX" instruction ROP-1 {A20} sets at time 9. What input pin on the or gate at TP-2 is a zero?

I2

41. During a test B1 instruction "+1" to adder is done by?

Carry 4 = 1

42. During a block xfer instruction the "A" register is used for?

word count

43. The term "CARRY 4" is high all during the block xfer, why?

add 1 to a when adding
add 1 to 5 when adding ch.

44. On a input block xfer, what term disables the timing chain from going from T10 to T0?

IO-OP

45. Other then M.C. the I/O operation FF{A22} can only be cleared two ways. They are?

1 cleared = FF-F
external

46. "CLKSR" is high every V100 except when ROP-2 is high at the same time as ST0-1 is high. Under these conditions why is "CLKSR" inhibited? {A19}

it holds address for the ST0 cycle

47. The breakpoint address originates at the maintenance console.

COUPLER WORKSHEET - 1

1. What assembly format is used on an autoload operation?

0000

2. What signals are sent from the coupler to the subsystem processor upon detection of a 0414(8) function code?

Start autoload seq., Stop cycle, Master clear, Force function, Computer ready

3. What is the purpose of bit zero on normal input channel zero?

function available on MIC 3

4. How does the B.C. receive the cylinder address following a seek function?

by inputting a 4 word input as a result of the function

5. What effect will a P.P.U. command of 0014(8) have if there was an address field correctable checkword error?

Read skip the address field on the next disk revolution and begin processing in the data field

6. What operation uses format 4?

data output from PPU

7. How is the data path through the coupler selected?

Bits 14, 15, of MIC 4

8. Is there a parity check on data transferred between the coupler and B.C.?

NO

9. How does the B.C. move the general status word from core memory to the coupler?

FORMAT 7

10. What P.P.U. function word connects the P.P.U. to the DT220 Dual Access Coupler?

any function Connects to the DT220

COUPLER WORKSHEET - 2

1. What is the purpose of bit zero on normal output channel zero?
function reply

2. What signal gates the 16 bit data word into the hardware controller? PATH SELECT CODE 01
C/REQ - B.J. 14 or 15 of NOC 4

3. When is the signal "Inpreq" used?
when the B.C. or H.C. is ready to accept a word and that the coupler is able to supply it

4. What is the initial frame count with format six?
0001

5. With format four, frame count of one, what bits of data Register are gated through the write MUX?
LOWER $2^4 \rightarrow 2^7$ 2^{10} - & 15

6. With a read MUX decode of ten, what input pins to board B13 are used for data? Pin 21 A26 A27 A28 A29.
A39 B31 B30 B29

7. What is the purpose of the board in Location B09?
STATUS GENERATION

8. The Deadman Timer = "Terminate" when the counter chip (B19) reaches a count of 8 ?

9. What is the purpose of normal output channel four?
PATH SELECT CODE

10. When the P.P.U. is outputting, the data register is effectively a 24 bit register.

11. Under what conditions will the latch at TP11 (B08) set?
F/C NO. 0 DEADMAN TERMINATE
or B.C. DISCONNECT CODE BIT 1 NOC 0

12. How is the assembly/disassembly code sent to the coupler?
NOC 0 BITS 12-15

13. What causes the deadman timer to expire?
no transfers on m.c. for 4.16 sec

14. What code on pins 2 and 14 of the MUX chip at Location 33 (B16) will select the path from the H.C. to P.P.U.?
code 1 2 0
14 1

15. When is the FF at TP16 (B22) set?
When PPU activates the channel

H.C. WORKSHEET-1

1. What three ways may a memory request be initiated?
   Data reference from control logic Interface processor reference
   Director reference from control logic
2. Which memory request can block the scanner for more than one memory cycle?
   data buffer request
3. How many words can the director buffer hold?
   16 directors
4. How many ranks in the data buffer?
   4 rank
5. What is the purpose of normal output channel 8?
   to sends functions on
6. List the "Special" directors.
   02 address 92 stop loading director
   08 terminate 94 unconditional branch
7. What is the data path from memory to the director buffer?
   Mem. – Mem. bus – Dir. catch reg – director bus – director buffer
8. What is the data path from the disk to the coupler?
   Read cable – shift reg. – catch reg – Data buffer mux
   Data buffer – to coupler
9. What supplies the address for loading the director buffer?
   Director address register
   input address counter (load pointer) 807
10. How many bits is the checkword that is recorded after the data field on the disk? 32. After the address field? 32.
11. How does status get from the H.C. to the B.C.?
    9 IC. 4
12. List the two kinds directors and describe what they do.
    support directors – establish hardware conditions
    data director – control data transfers

H.C. WORKSHEET-2

1. What director is used for reading the address field of the sector?

01100 Compare normal director

2. What is the director $0201422000000000_{[16]}$
What does it say to do?

3. Decode this director $38008483_{[16]}$.

What path does it use?
What does it say to do?

4. Make a director list to

C0800400
E0001000
80000080
80000400

   a. select drive No. 4
   b. select read control status
   c. place the status in core memory location $400_{[16]}$.

5. What is the path for unloading the director buffer?

6. What is the HEX. code of the director that finds the sync $\{11\,00\,11\}$ byte? 38000713 Rap 2

20003300
38010000

7. As the H.C. leaves its monitor loop, how does it know what subroutine to branch to?

0402 B.C. loads

8. What is memory address $005A_{[16]}$ used for?

General status word

9. How does the P.P.U. know that the drive is "On Cyl." after a seek is initiated?

By checking general status and finding bit

10. At what memory location does the B.C. connect subroutine start?

0256

H. C. WORKSHEET - 3

1. During a write operation, what Register is the input to the checkword generator?
shift register

2. What is the HEX code loaded into the divide Poly. Register?
00A0 0805

3. What is the shift count, loaded into the _____ counter, with the Initiate Error Correction director for the address field?
Byte 18 hex

4. What registers can be gated through memory address MUX I? Data address reg Director address reg _____. What is gated through MUX II?
MUX I B C address

5. What is a Channel 9 code of 0080?
Clear internal status

6. If the FF at TP1 (A05) is clear, what is the source or destination of the data Xfer?
Complex
What FF on (A05) tells direction of Xfer?
FF AT TP5 SET = FROM Disk CLR. TO DISK

7. Under what conditions would the FF at TP1 (A06) set?
counter Equal to zero, R/P or W/P and sector mark

8. How many possible status are available on NIC No. 4 to the B.C?
13

9. If a director request is being made to memory, what is the state of:

data scanner latch? clear

director scanner latch? set

processor scanner latch? set

director request 2 latch? set

processor request 2 latch? clr

processor request 1FF? clr

processor request 3FF? set (B26)

10. Under what conditions would TP27 (B27) equal a logic one?
data buffer on R.F. transmitting to memory and reply received

H. C. WORKSHEET - 3 (Continued)

11. What happens if the FF at TP8 (B27) clears?
stop loading buffer

12. (A26) How many passes down the timing chain will be needed to increment:

    A. The director memory address register?
    1 Pass

    B. The director buffer input address?
    0 Passes

13. When the stop loading FF, TP5 (A26) sets: what FFs will be cleared?
memory request memory Reply write timing initiate

14. What signal (A27) initially starts the read timing chain?
ENDEX STEXC

15. What signal (A27) loads the director output register?
S Φ / PD

H. C. WORKSHEET - 4

1. The first director in the director buffer is a support director.

   What input pin on the "And" gate at TP24 (A22) is used to generate RTFE from a channel Noc8 function of 002 (Pin 2).

2. With the 6000 controlware, what will be the first director loaded into the director buffer after an autoload? C400 A040 Load register Divide Polynomial

3. On a Write operation, how many bits are loaded into the shift register? 8 - 6 bits used

4. The JKFF, location 10, by TP3 (B24), will be set by the decode of a CO director.

5. Setting the mark start FF (B22) will clear the delay byte counter. (B16)

6. Disregarding the timing chain, what FFs (B14) will be set if bit 14 = one, with a "CO" director?

   one

7. With the 6000 Controlware, what conditions will be selected by the register chip on B12?

   Clear checkword generator not Zero fill not 8 bit mode

   What director does this?

   86

8. When will the write checkword data shift enable FF, TP8, B13, set? after the last data is written and write check word has been decoded

9. How often is the bit counter (B16) incremented? for each bit by SRCL2.

   Which RAP director loads it?

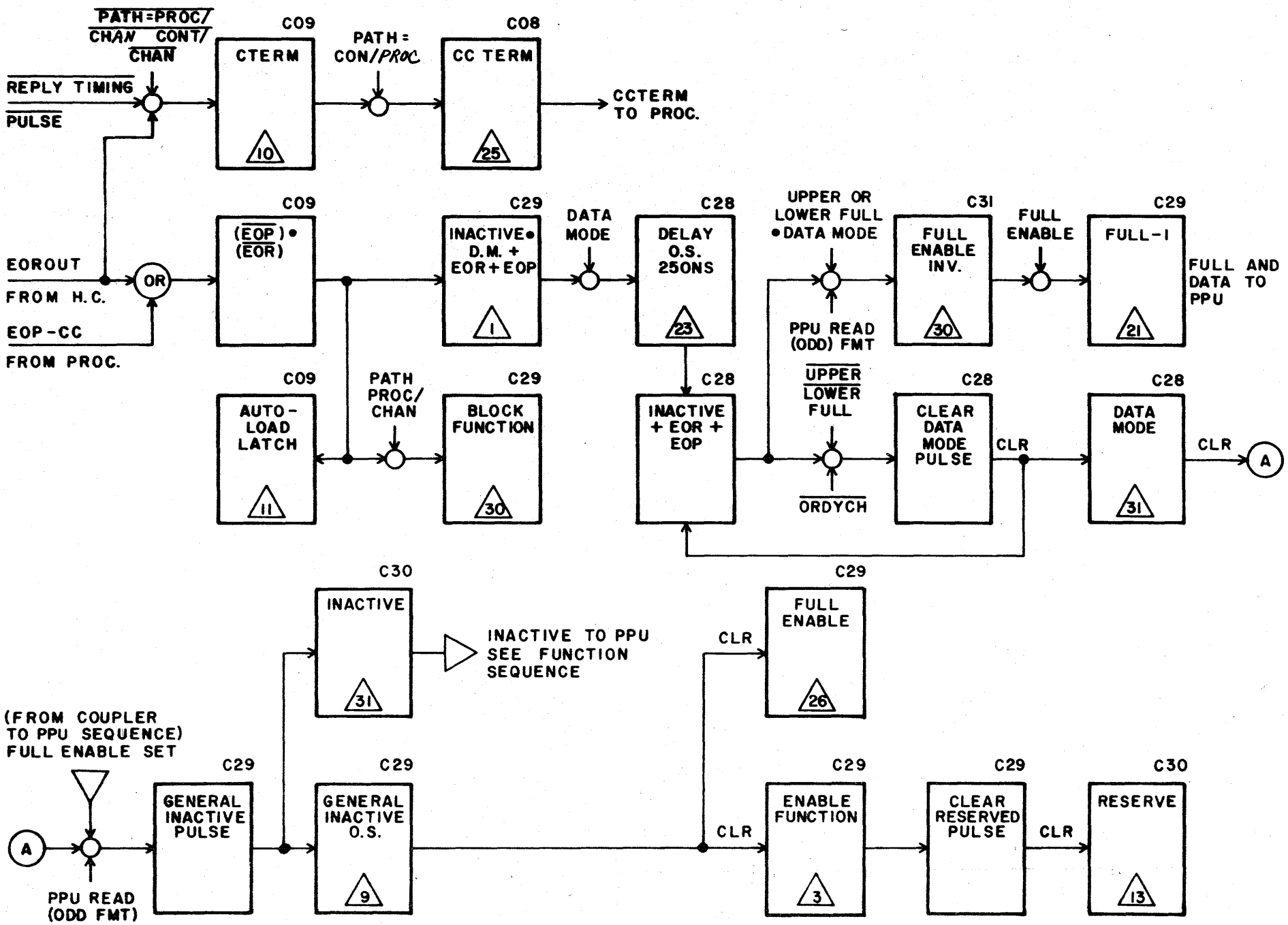
   Read Rac 38000713

10. How many outputs of the unit select decoder (C12) will equal a "one" when the H.C. is trying to select a drive?

    7 High
    1 Low.

6000 COUPLER
STUDENT HANDOUTS

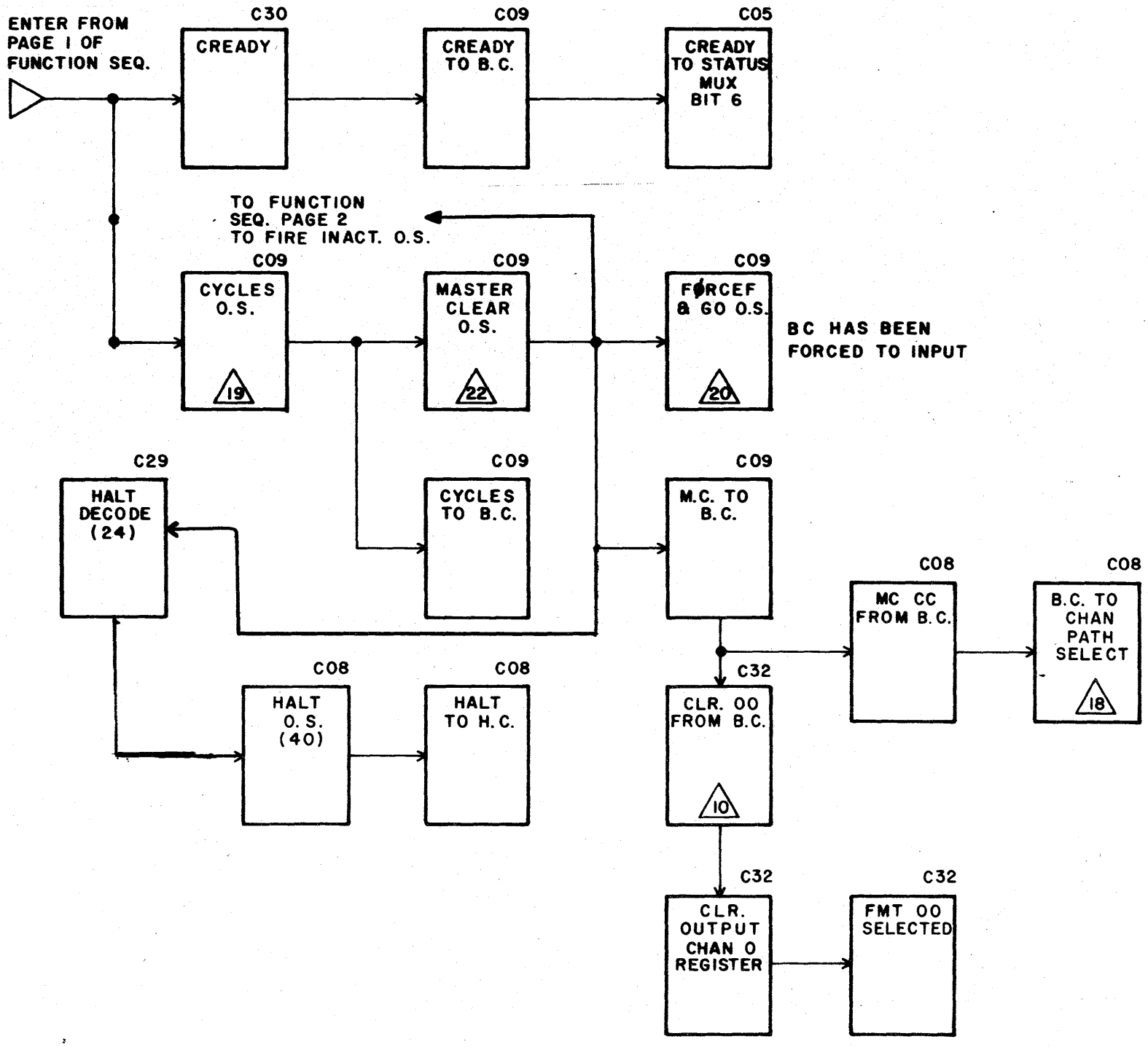
TERMINATE (PROC. EOP•CC OR H.C. EOROUT)



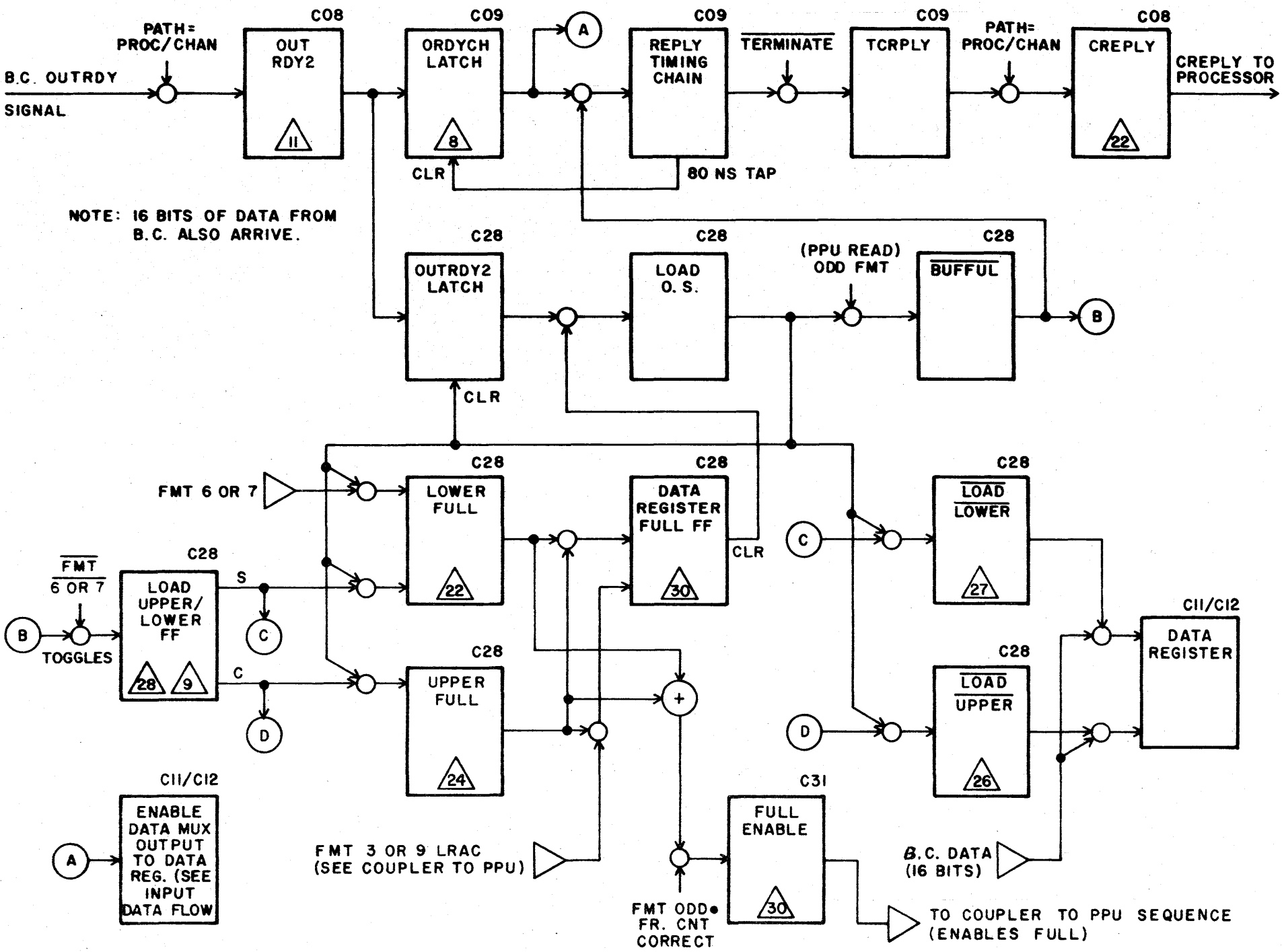
P8038

HO-1

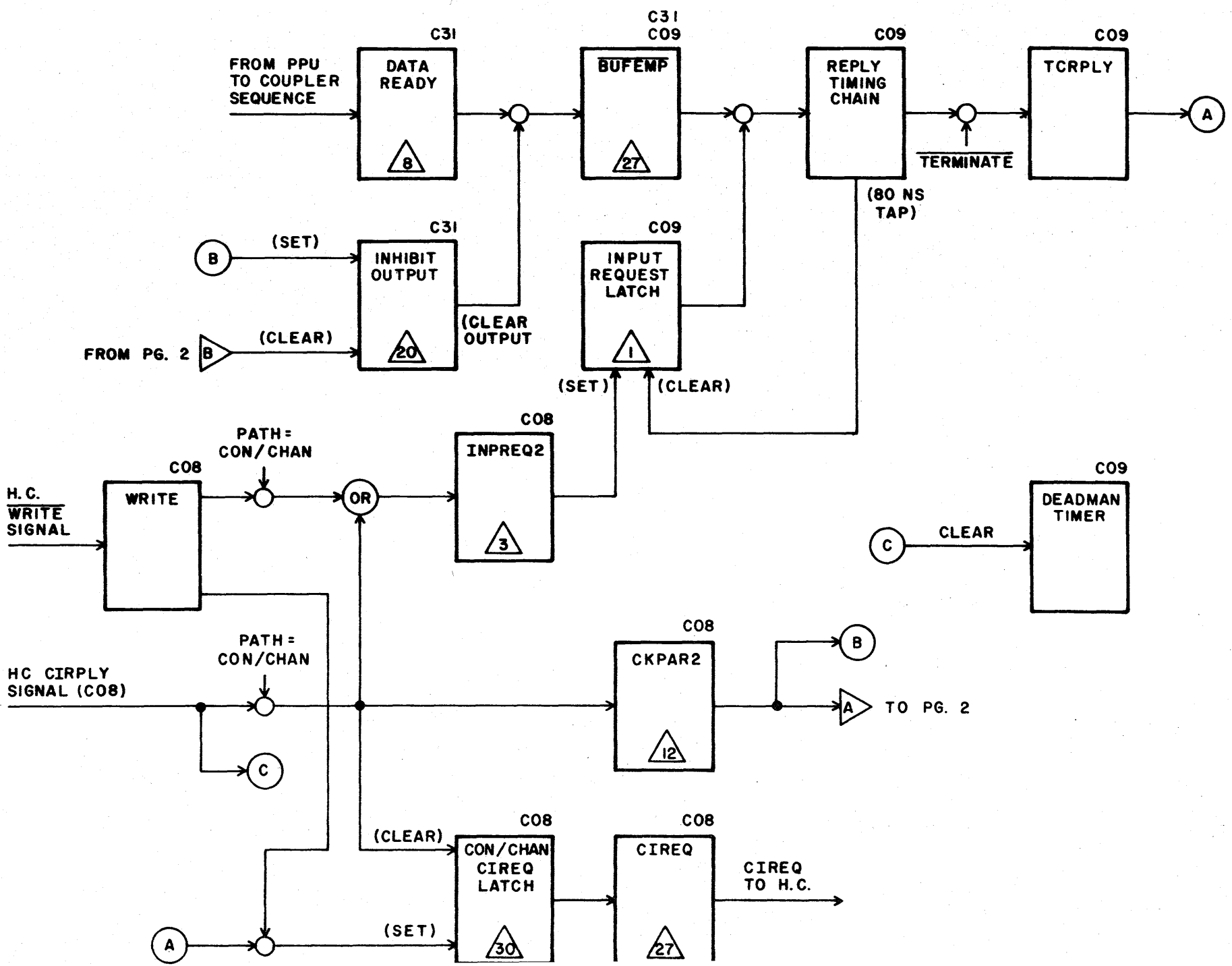
AUTOLOAD FUNCTION (0414_8)



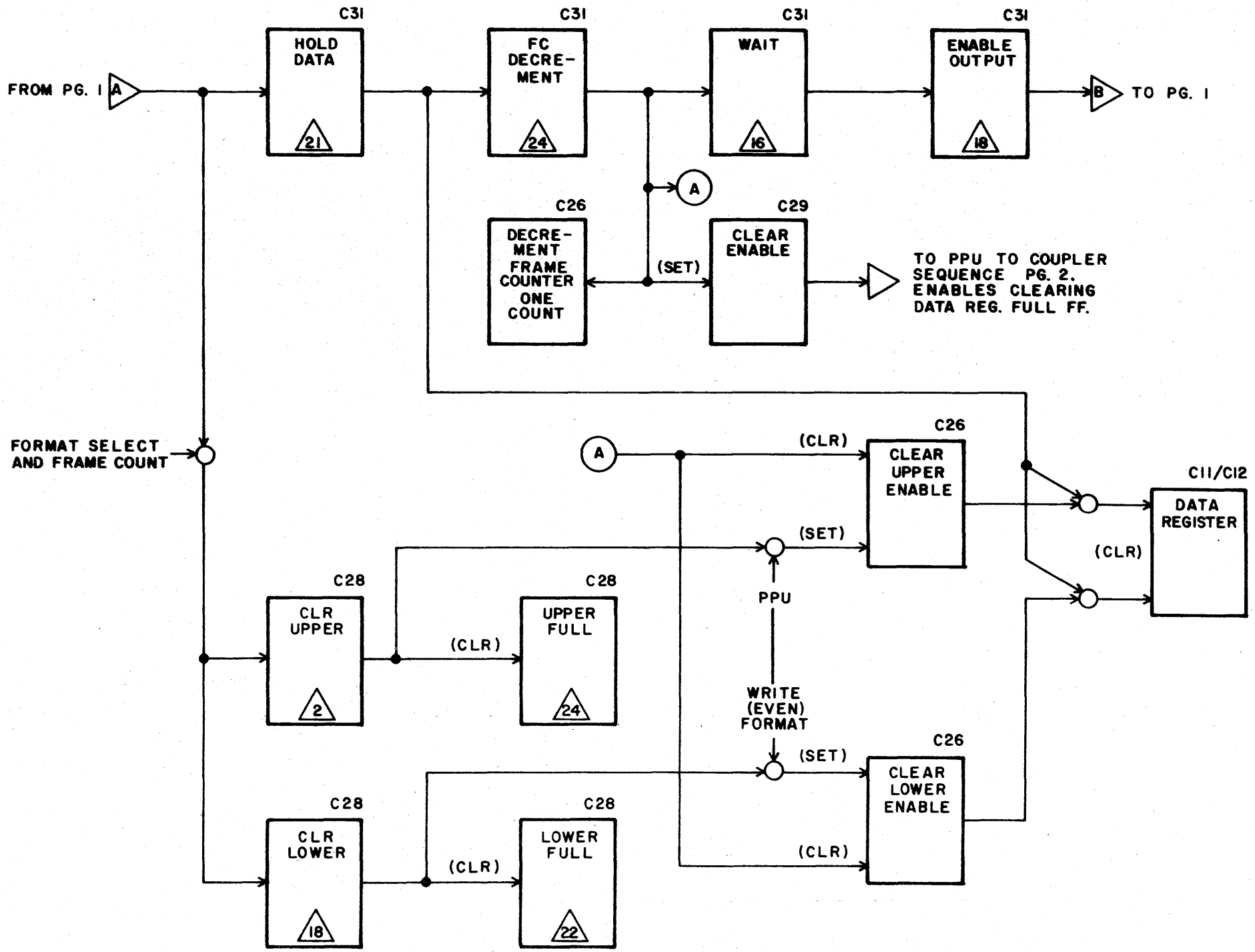
PROCESSOR TO COUPLER



COUPLER TO CONTROLLER PAGE 1 OF 2

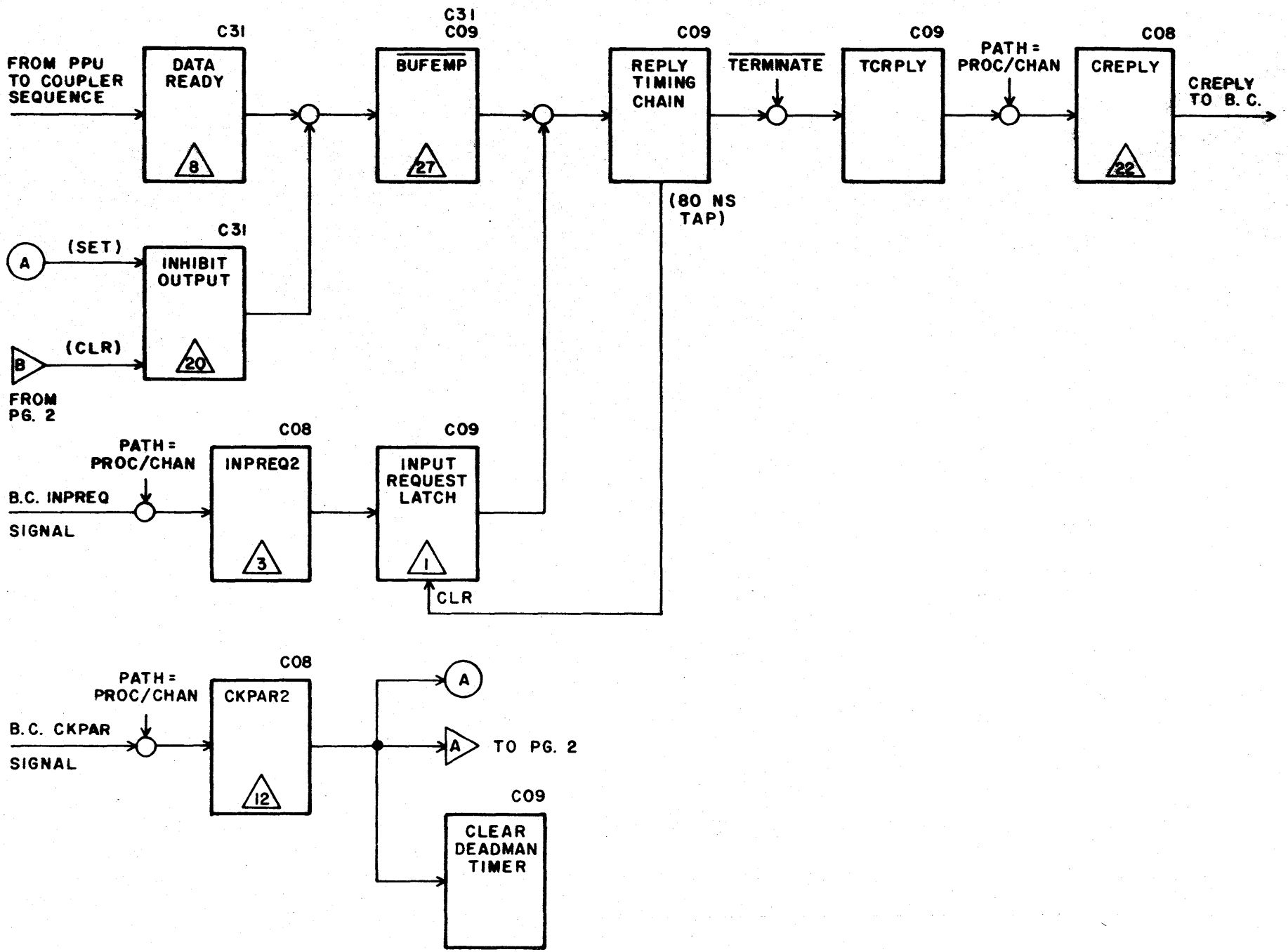


COUPLER TO CONTROLLER PAGE 2 OF 2

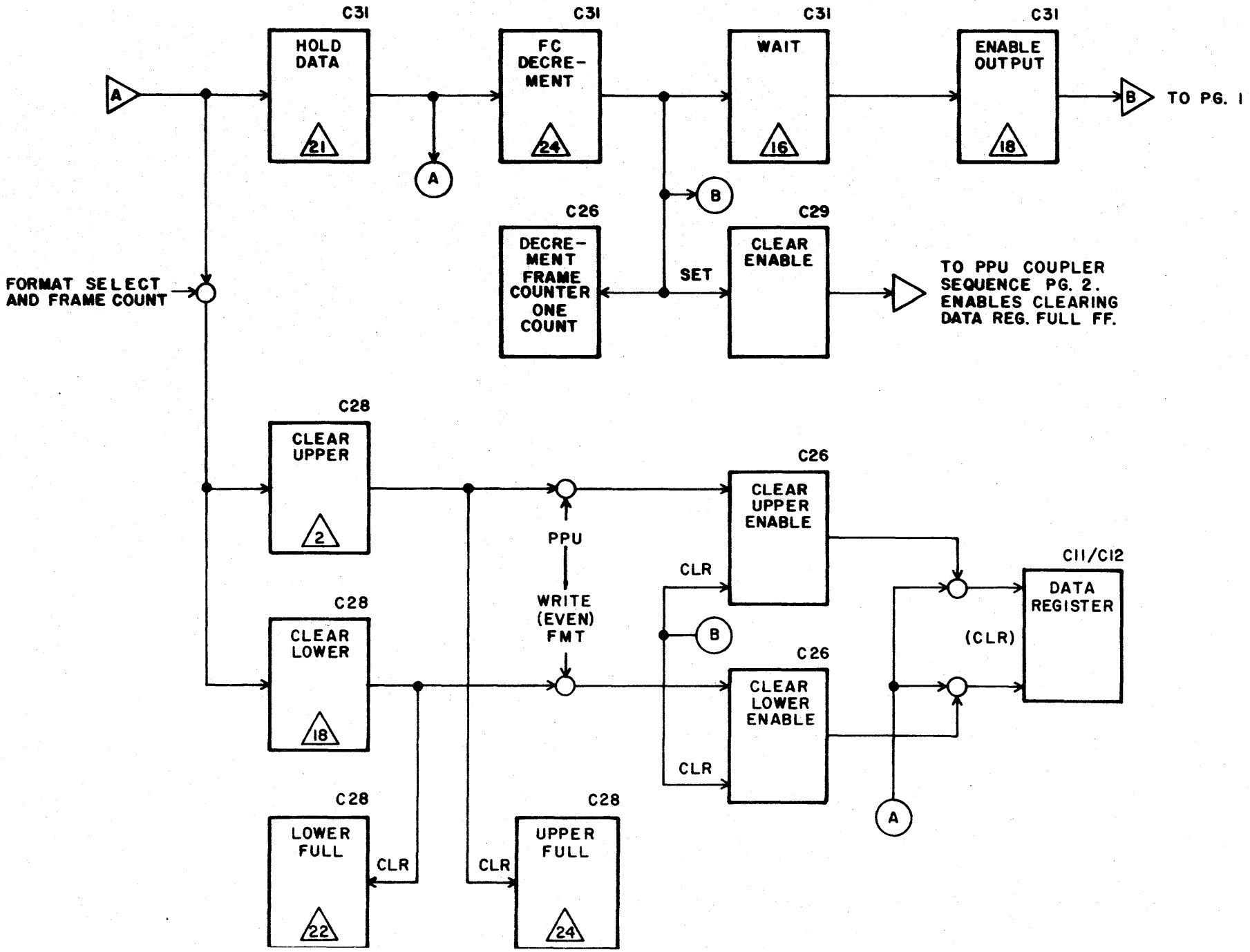


COUPLER TO B.C.

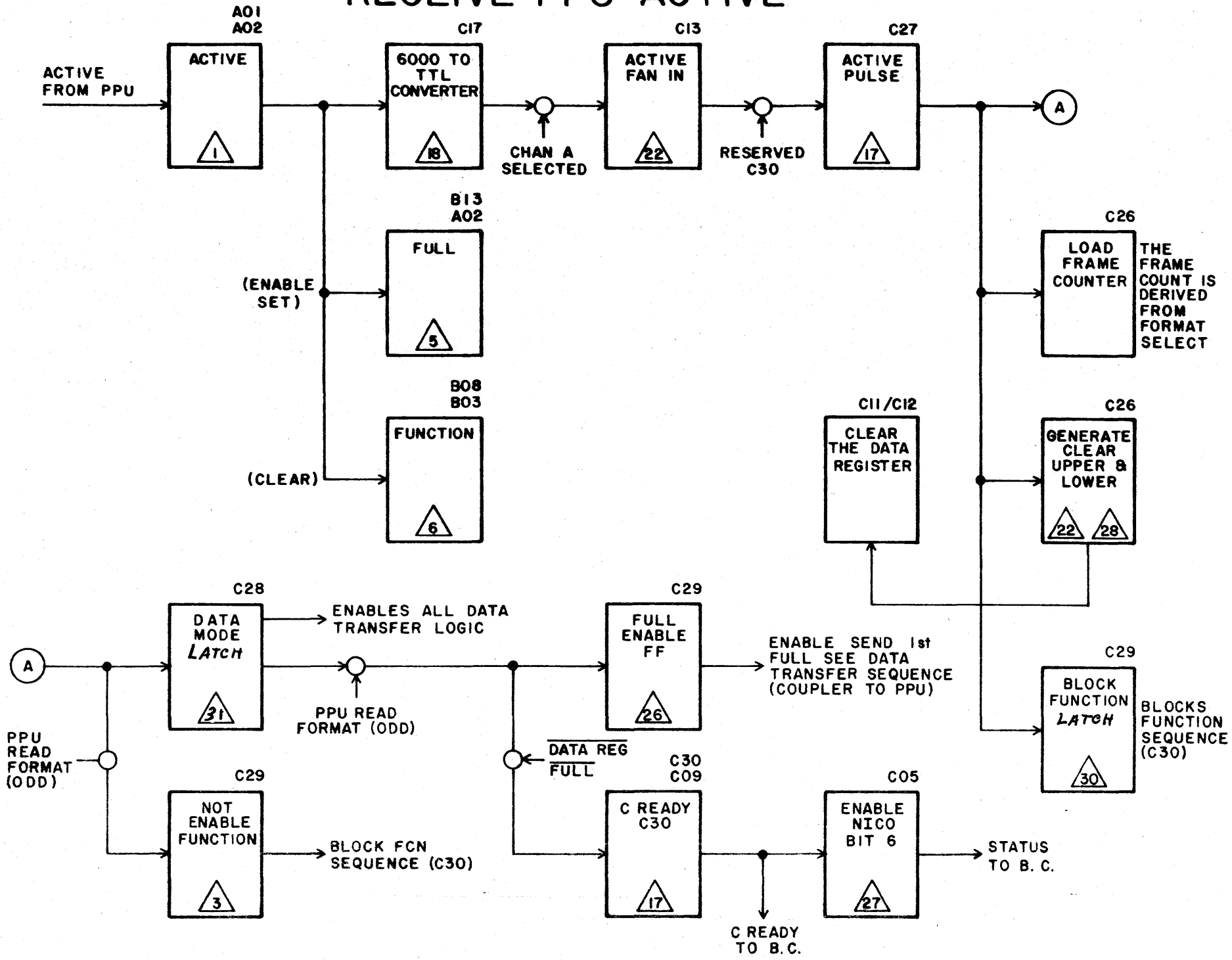
PAGE 1 OF 2



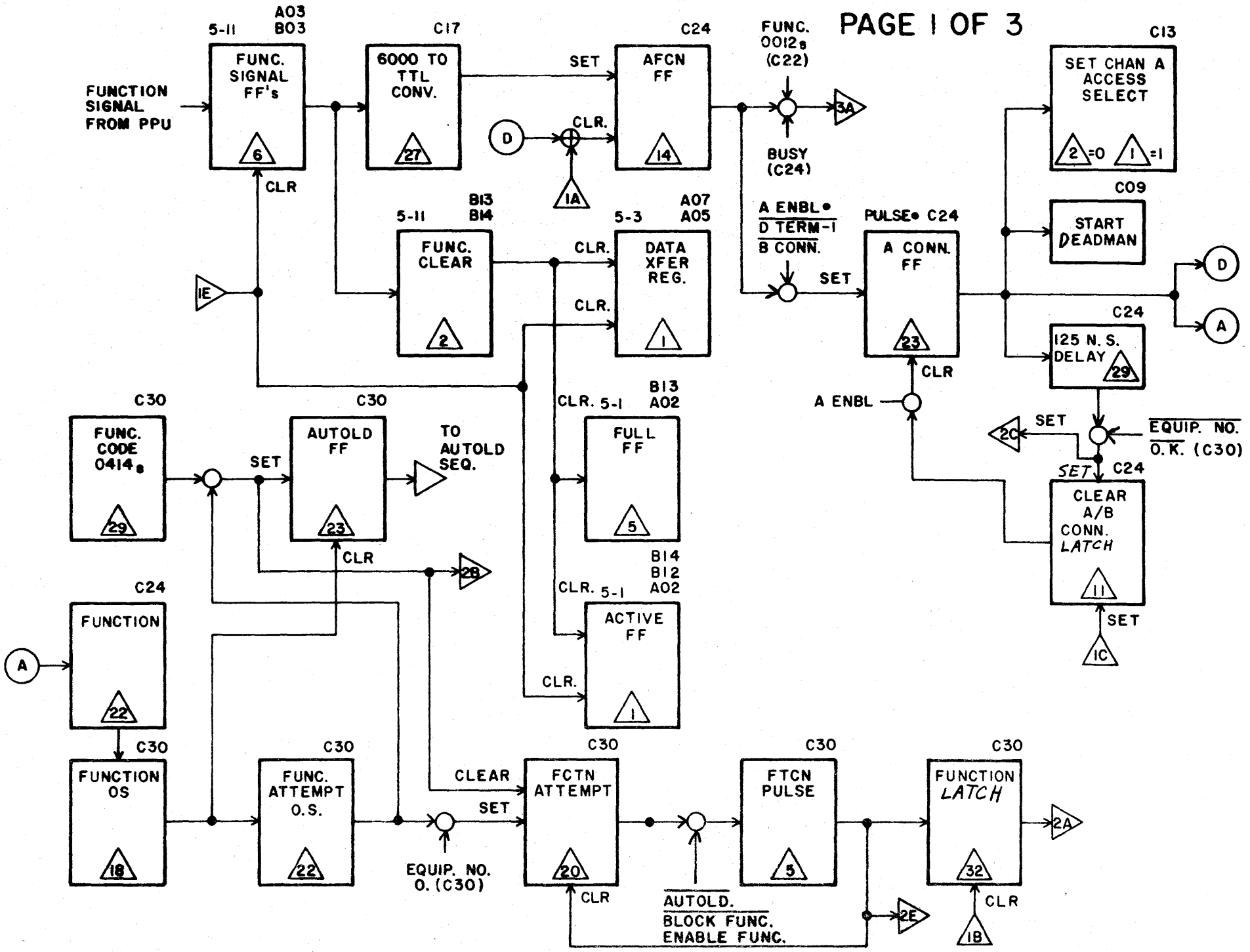
COUPLER TO B.C.
PAGE 2 OF 2



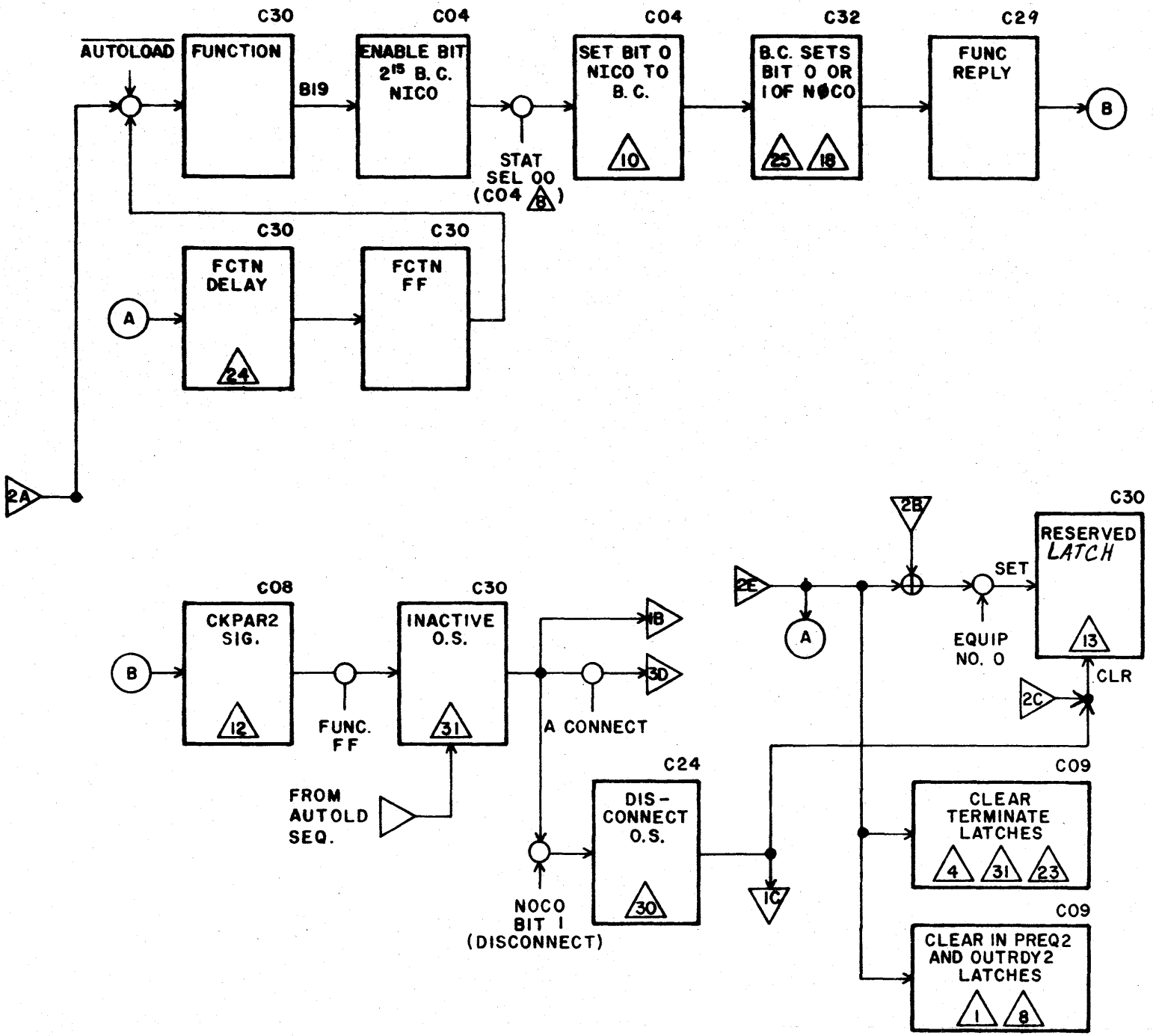
RECEIVE PPU ACTIVE



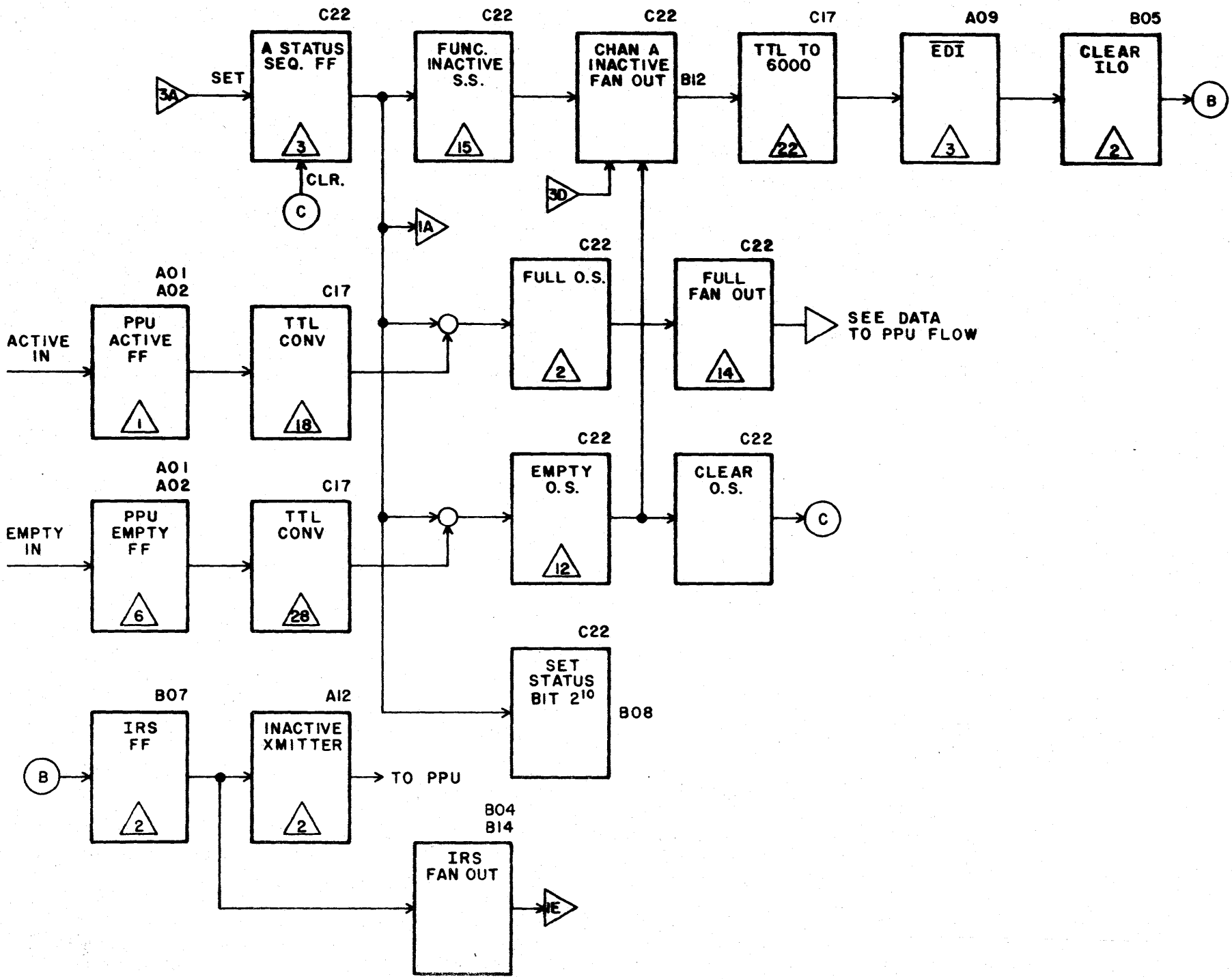
FUNCTION SEQUENCE (INCLUDING CONNECT)



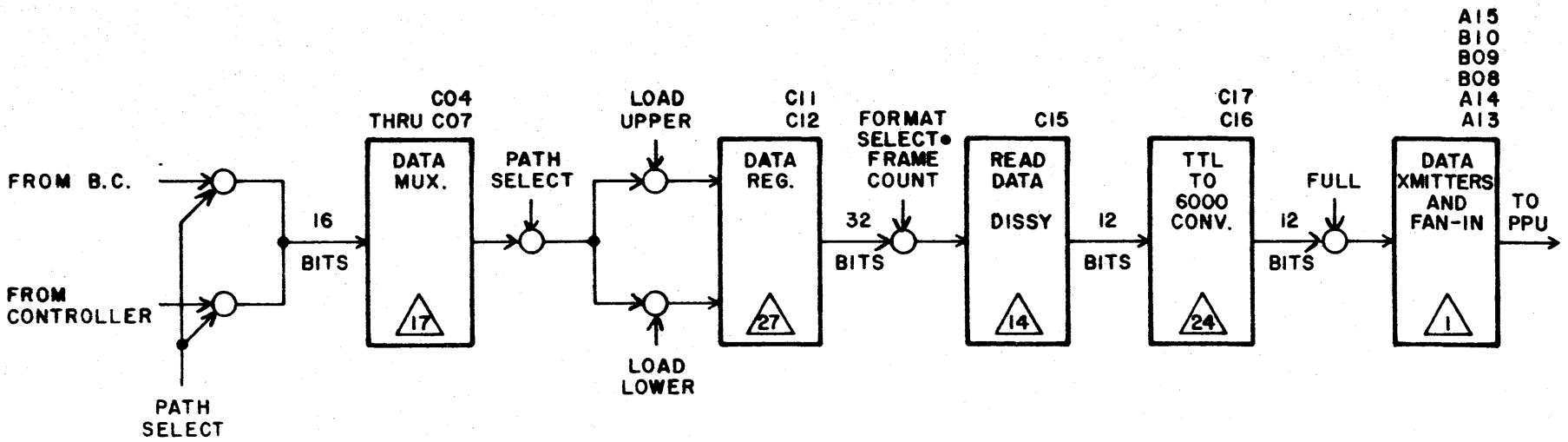
FUNCTION SEQUENCE



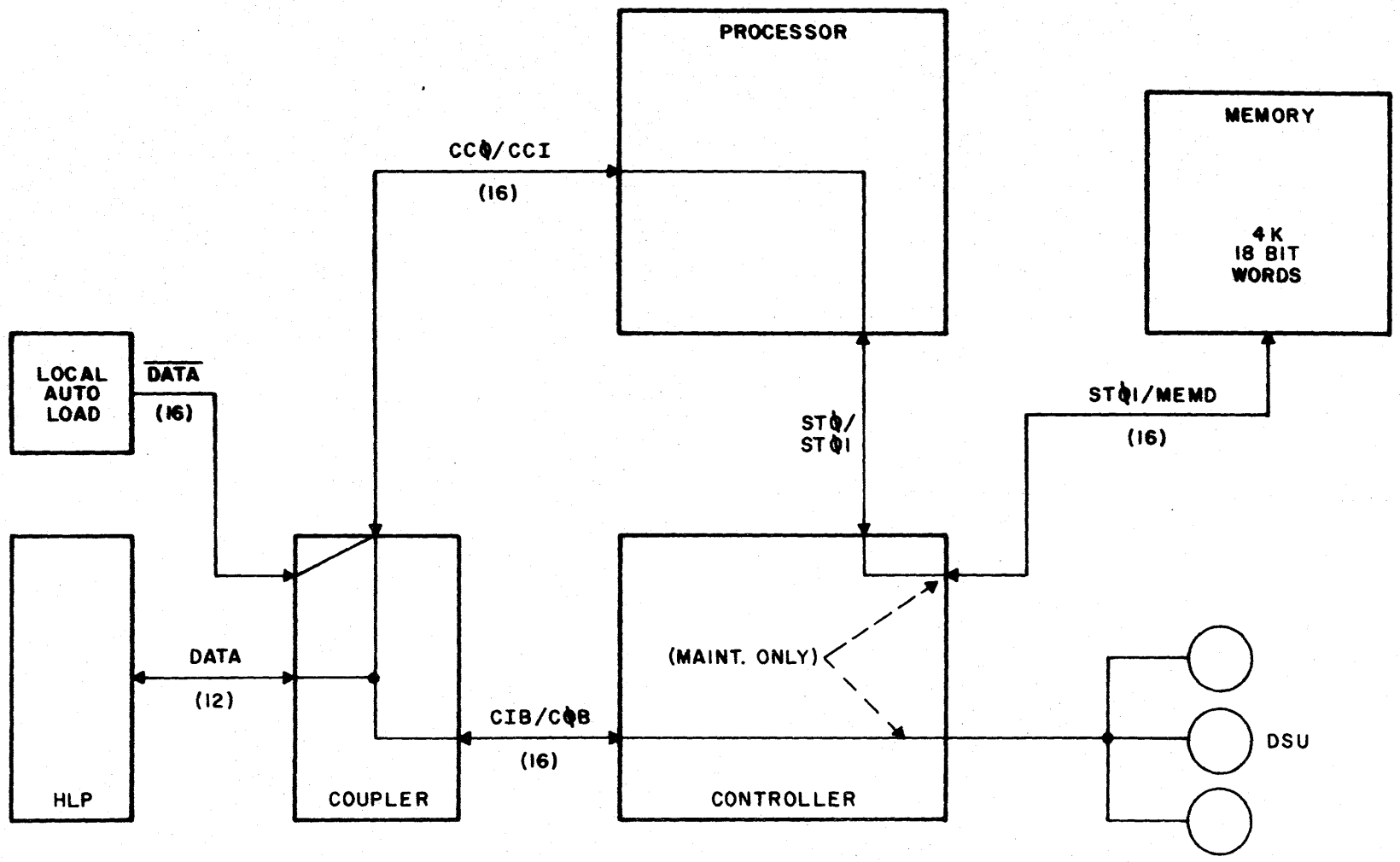
FUNCTION SEQUENCE



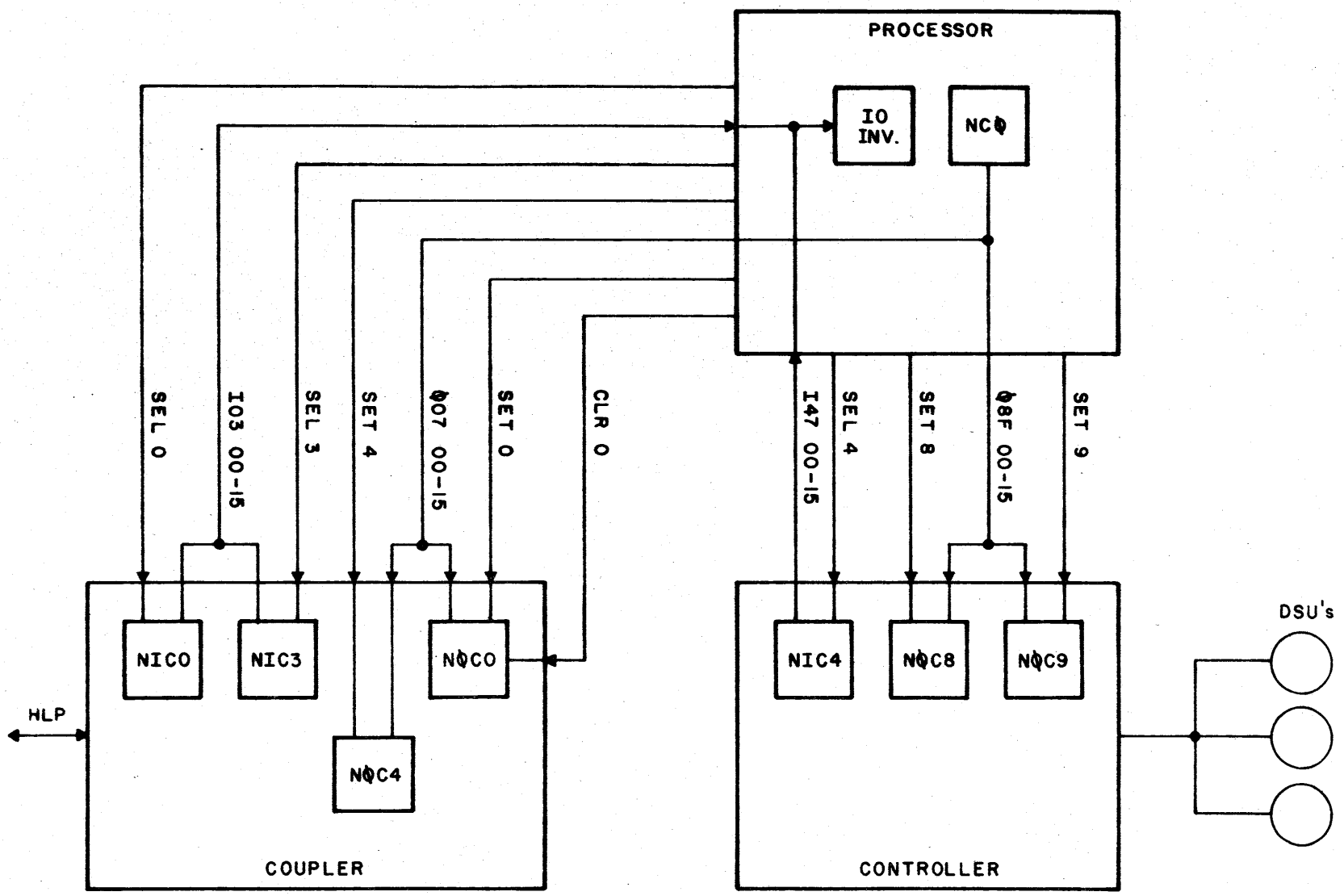
INPUT TO PPU DATA PATH



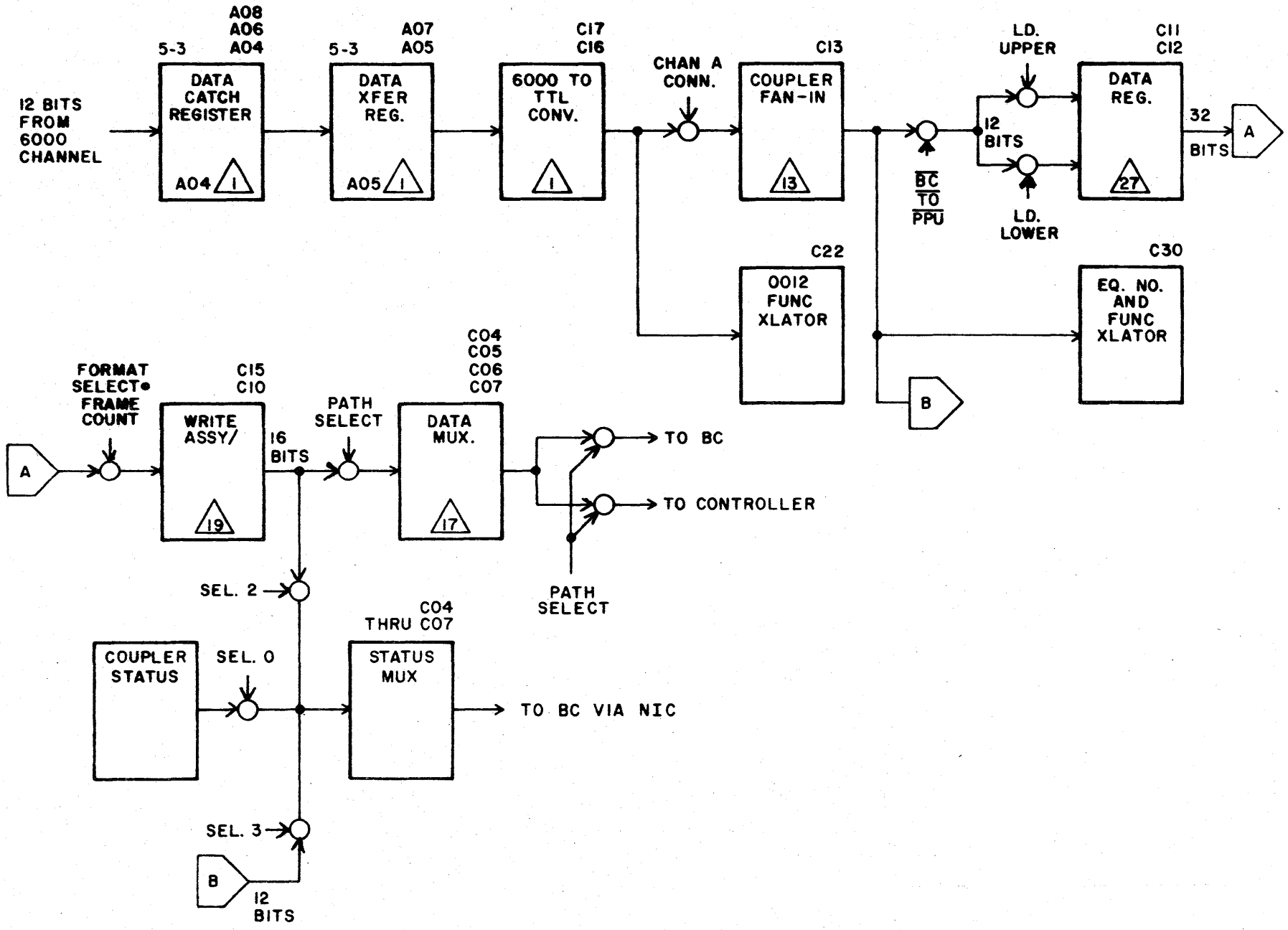
844 SYSTEM DATA PATHS



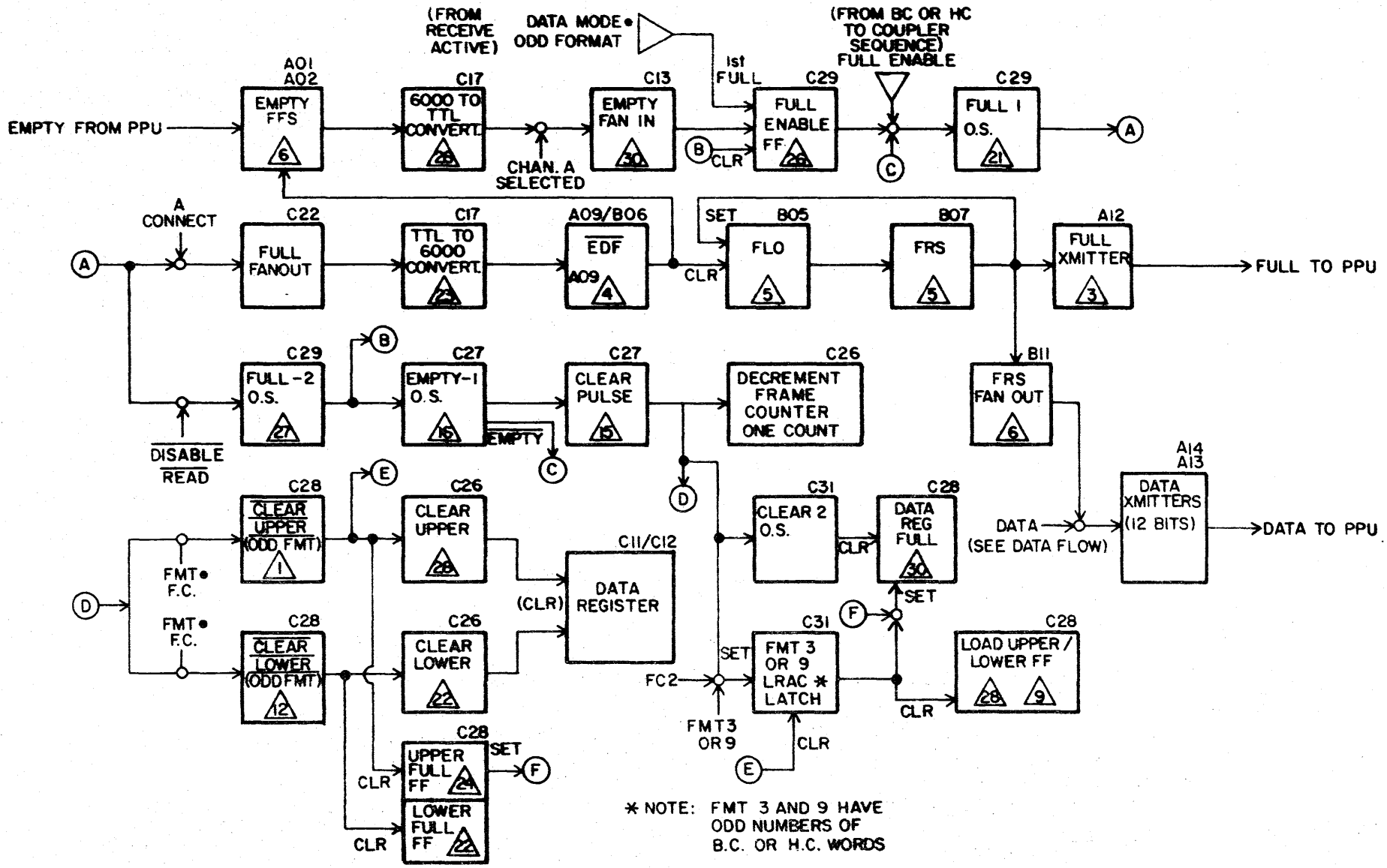
844 SYS NORMAL CHANNEL INTERFACE



OUTPUT FROM PPU DATA PATH

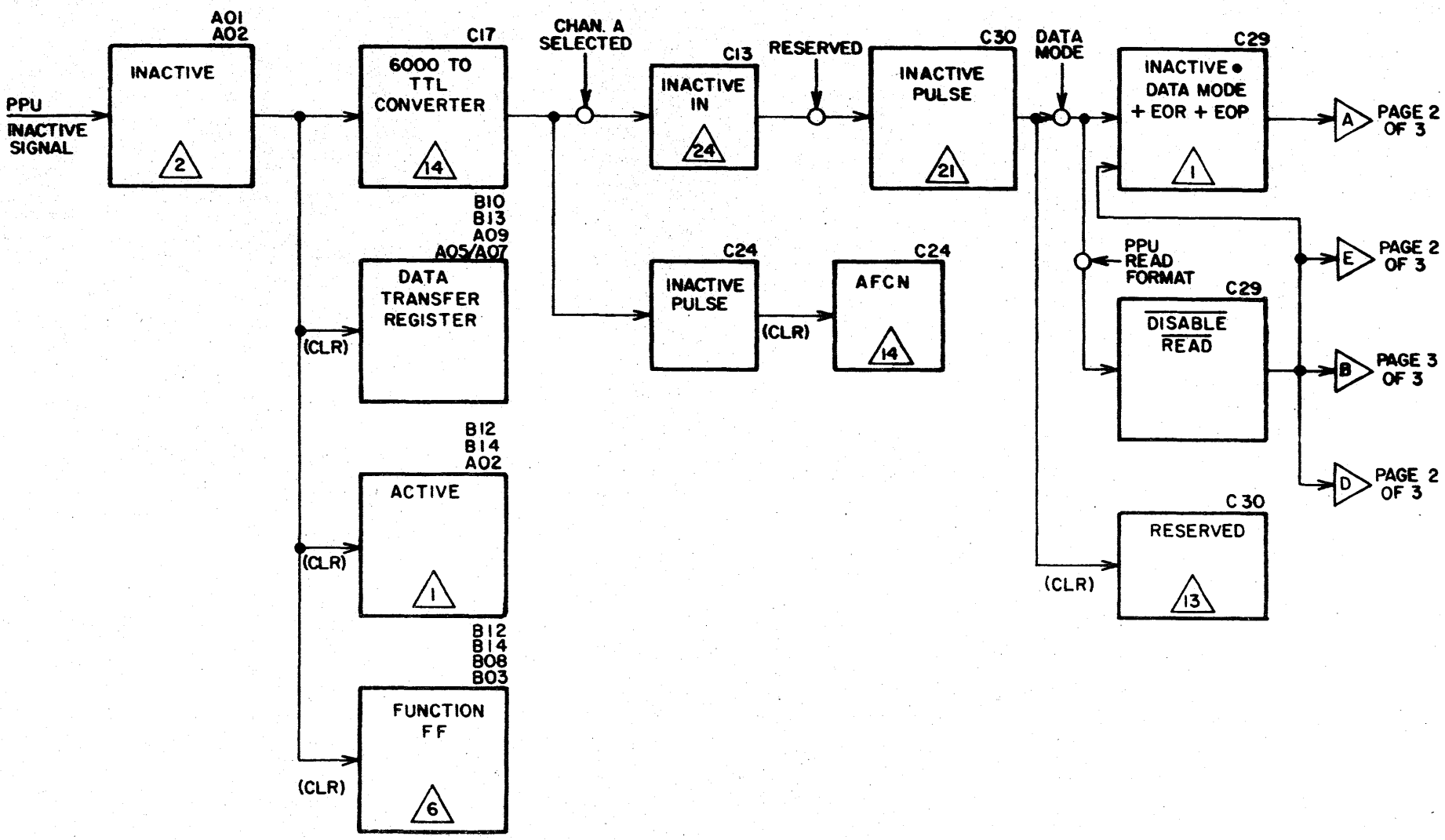


COUPLER TO PPU



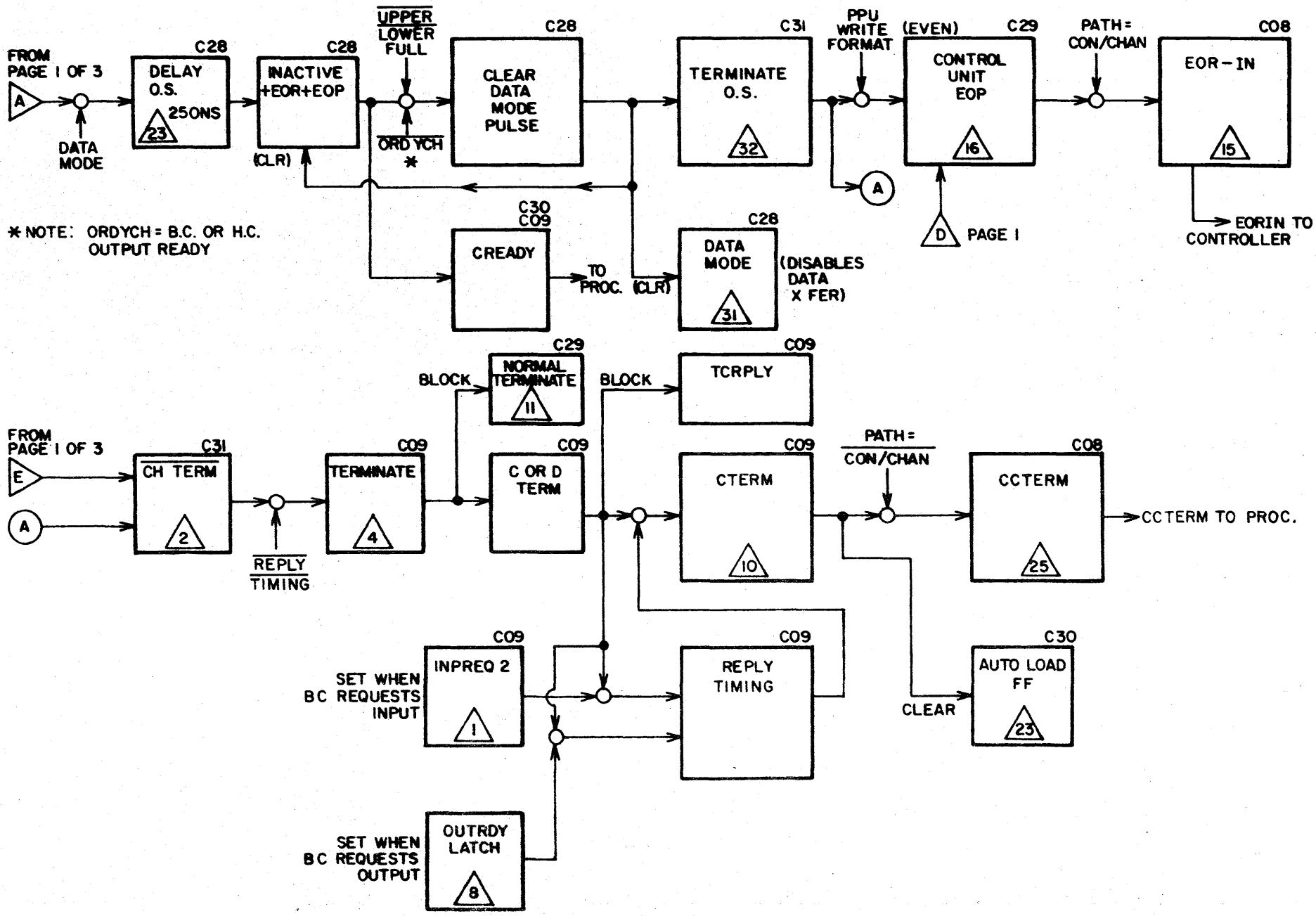
TERMINATE (PPU SENDS INACTIVE)

PAGE 1 OF 3



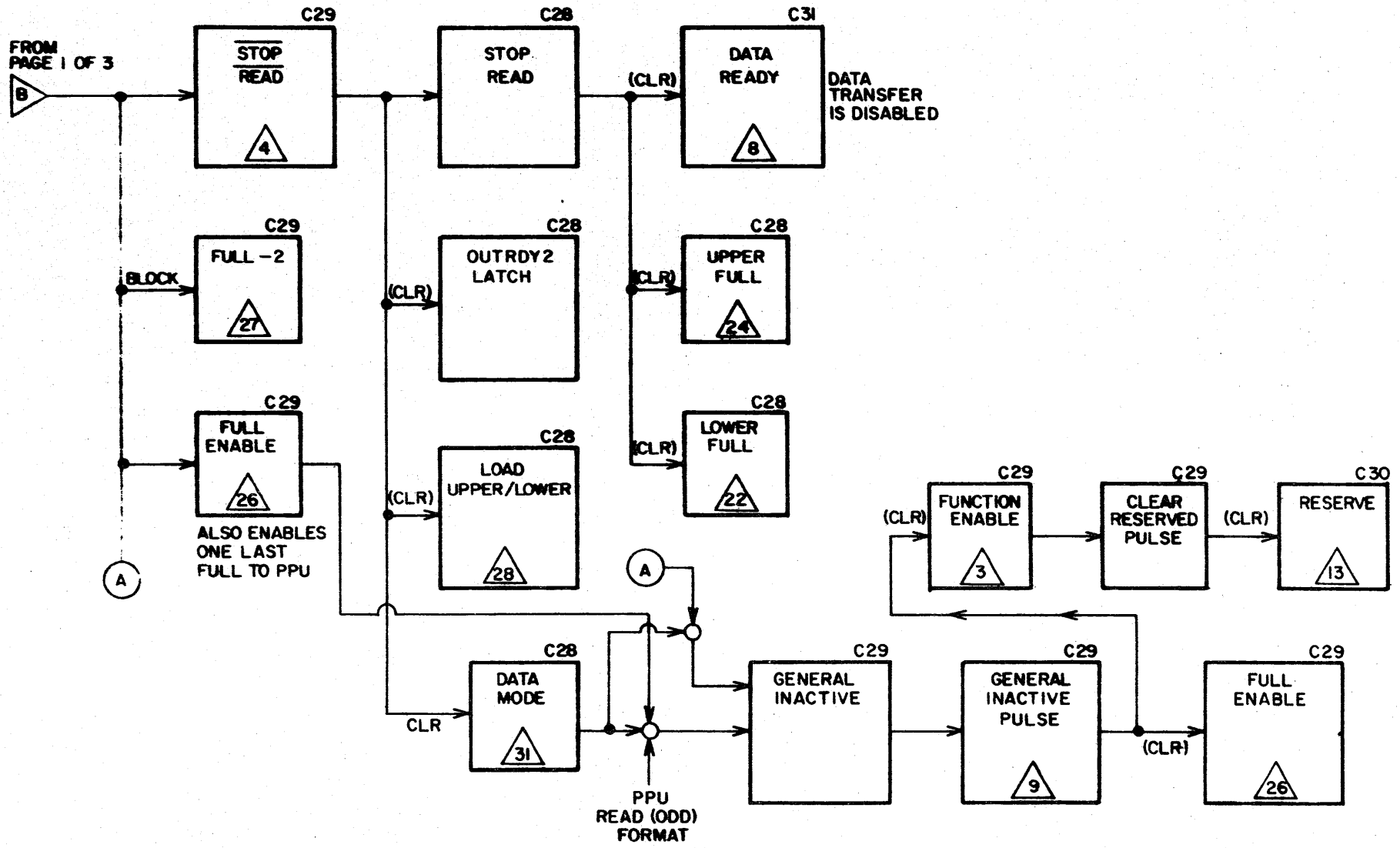
TERMINATE (PPU SENDS INACTIVE)

PAGE 2 OF 3

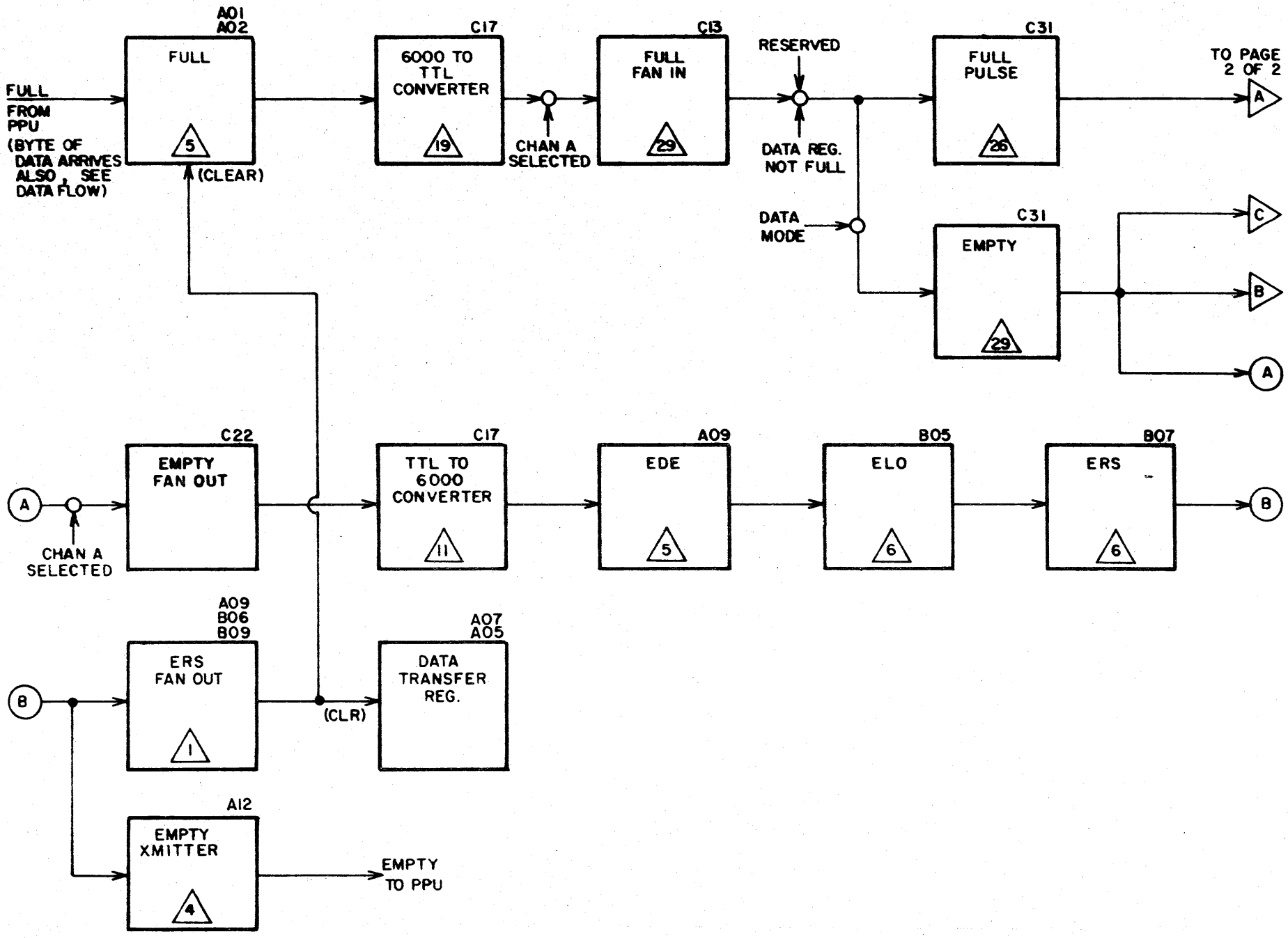


TERMINATE (PPU SENDS INACTIVE)

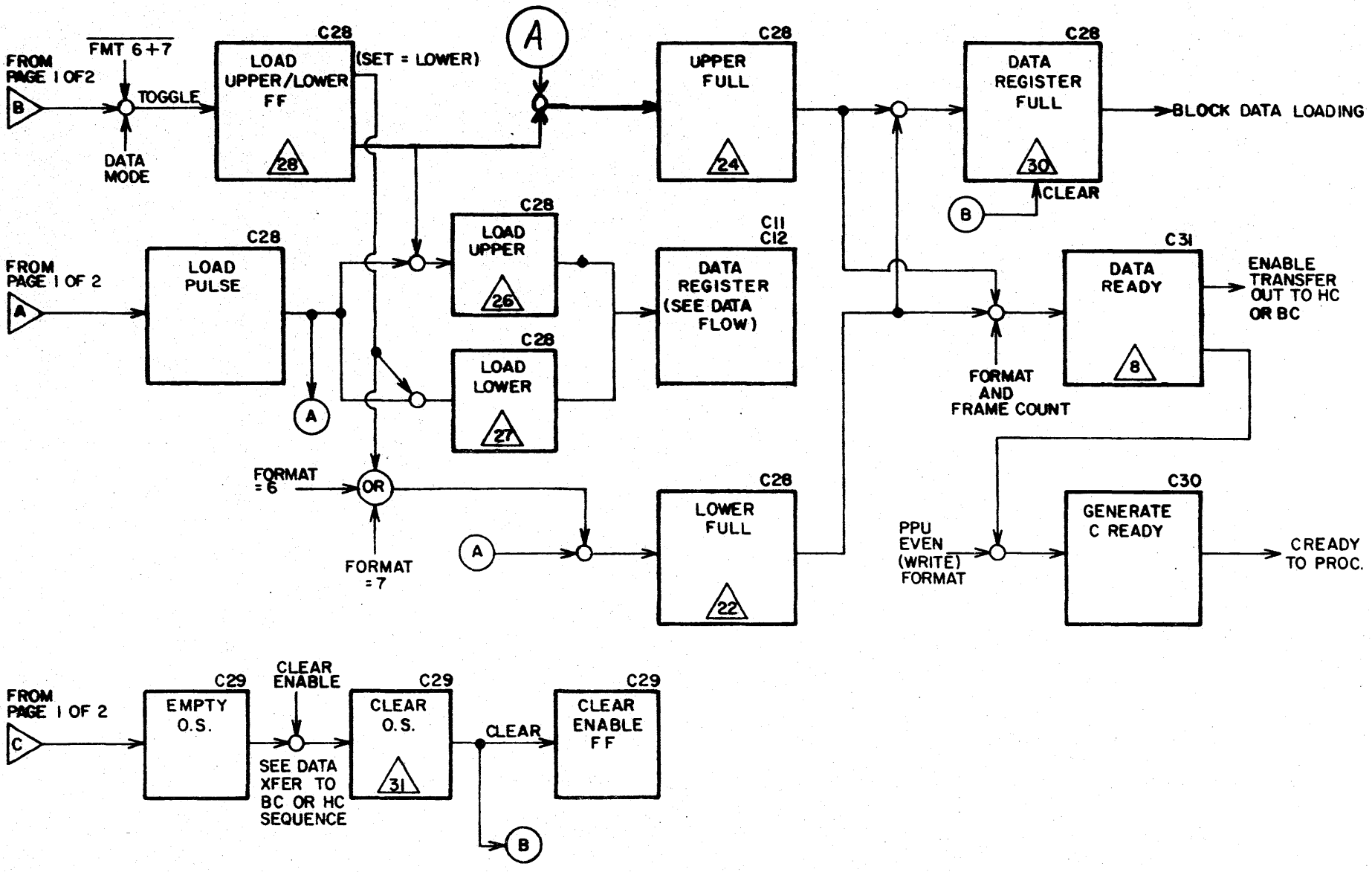
PAGE 3 OF 3



PPU TO COUPLER
PAGE 1 OF 2

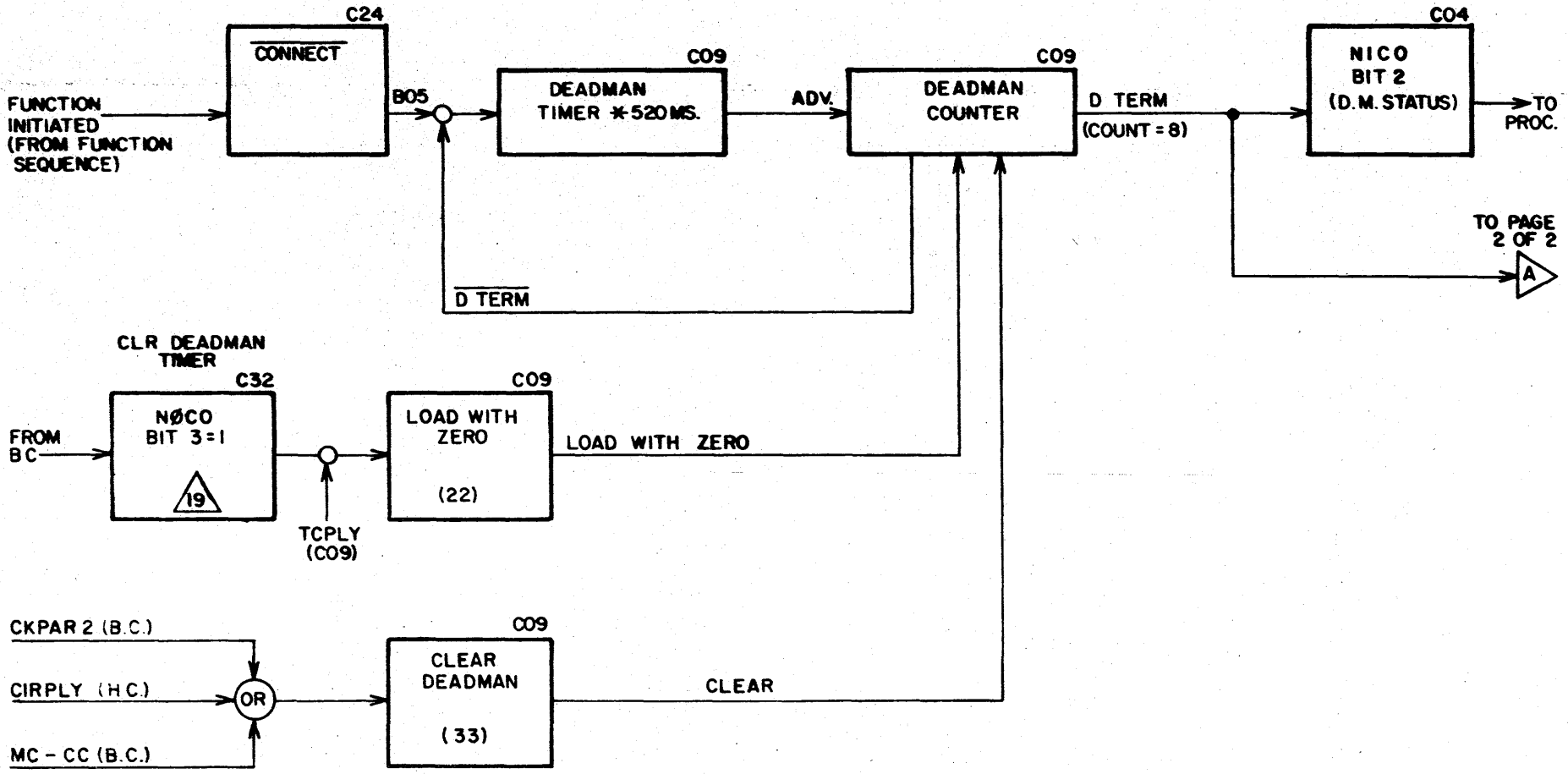


PPU TO COUPLER
PAGE 2 OF 2



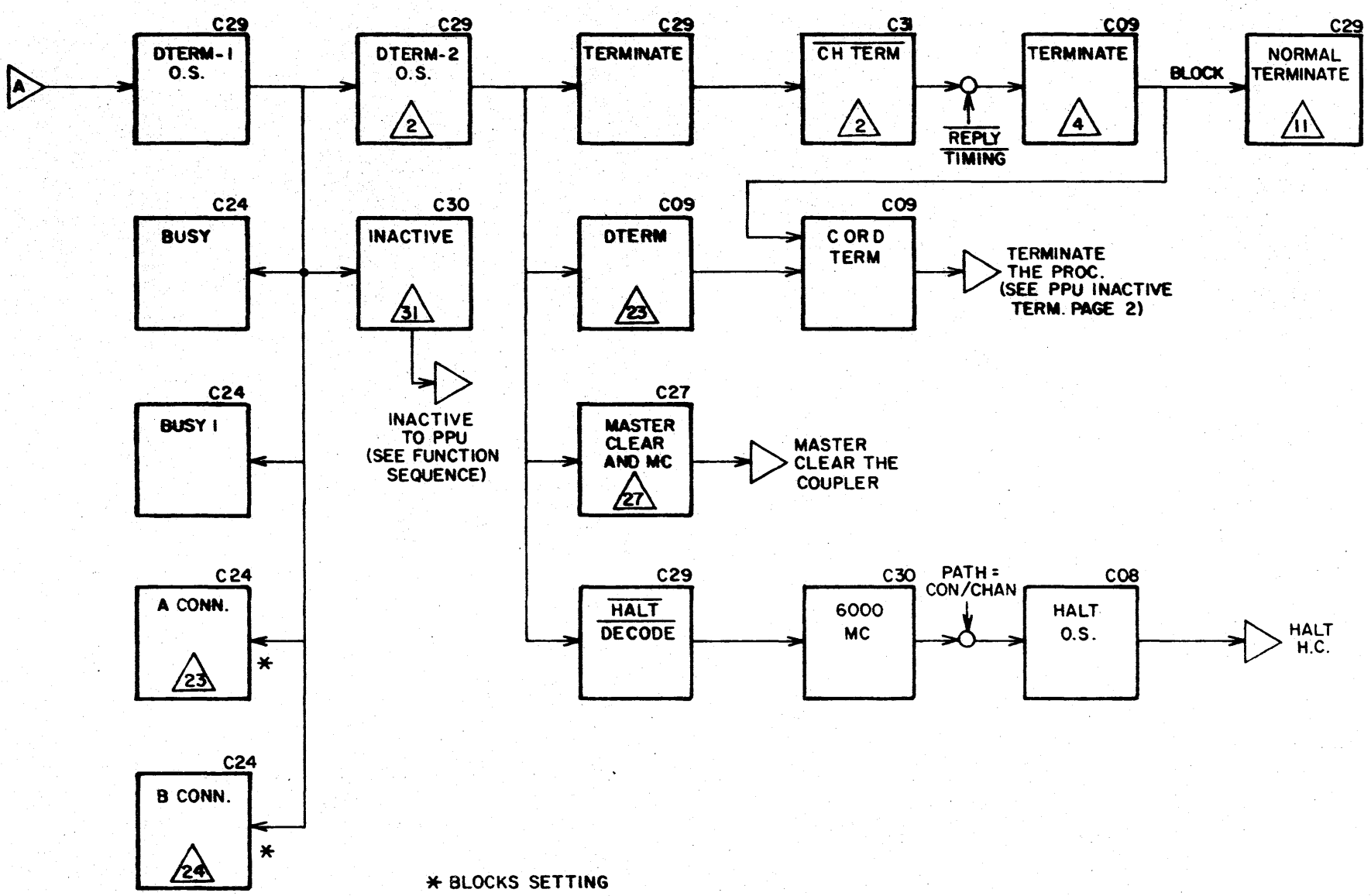
DEADMAN TERMINATE

PAGE 1 OF 2

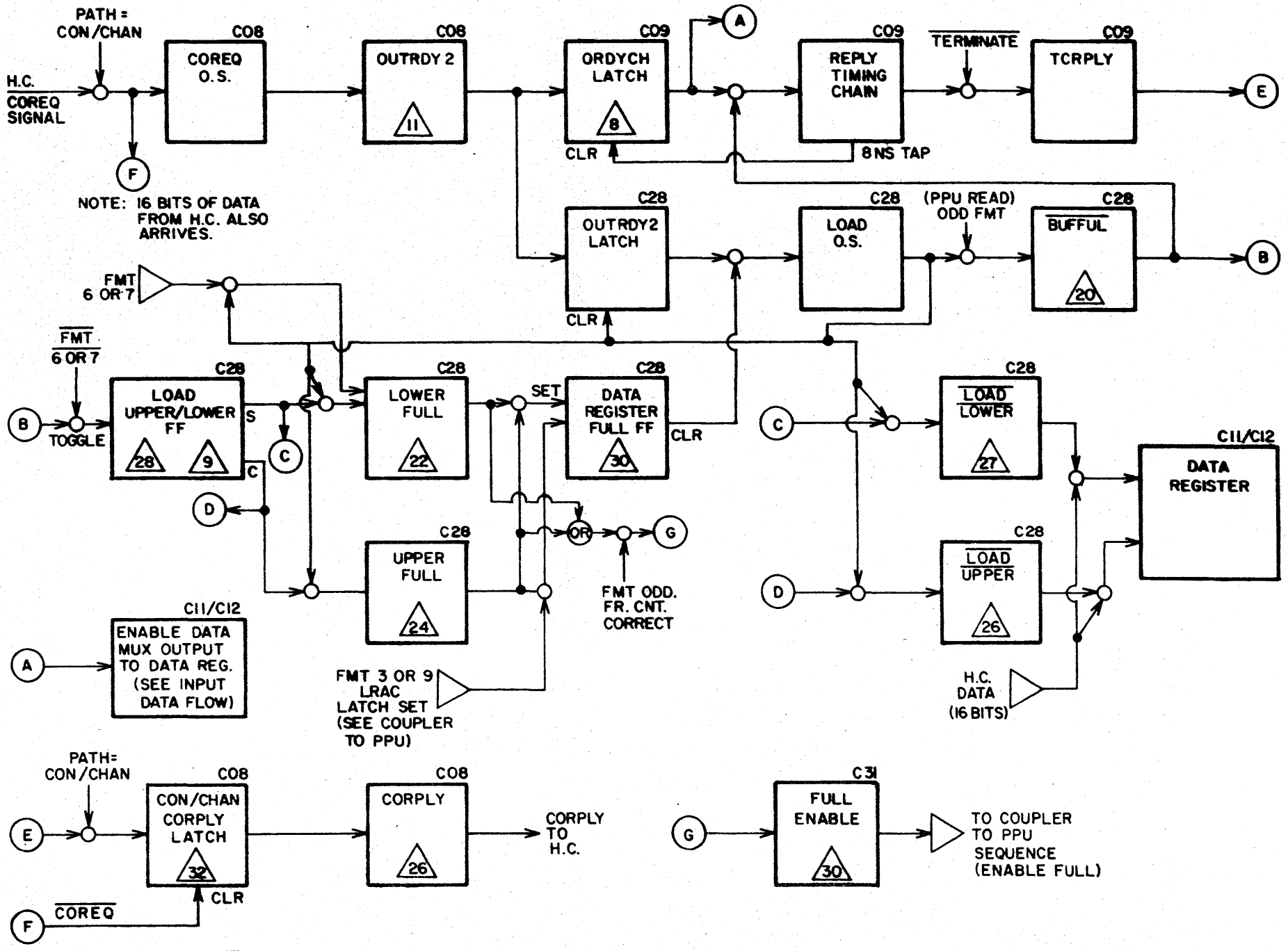


DEADMAN TERMINATE

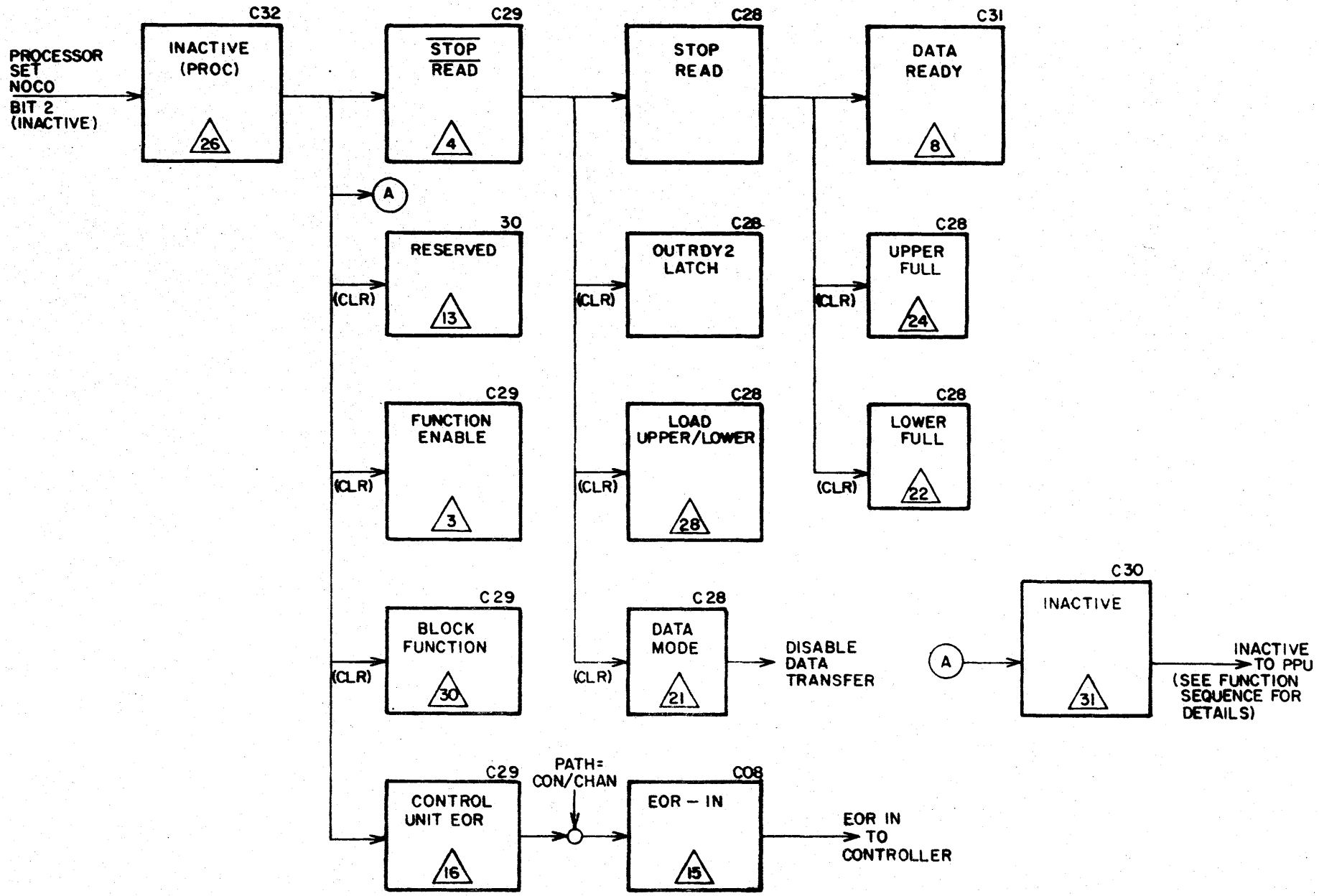
PAGE 2 OF 2



CONTROLLER TO COUPLER



TERMINATE (BC SENDS INACTIVE)



COUPLER WORKSHEET-1

1. What assembly format is used on a autoload operation?

2. What signals are sent from the coupler to the subsystem processor upon detection of a $0414_{(8)}$ function code?

3. What is the purpose of bit zero on normal input channel zero?

4. How does the B.C., receive the cylinder address following a seek function?

5. What effect will a P.P.U., command of $0014_{(8)}$ have if there was a address field correctable checkword error?

6. What operation uses format 4?

7. How is the data path through the coupler selected?

8. Is there a parity check on data transferred between the coupler and B.C.

9. How does the B.C., move the general status word from core memory, to the coupler?

10. What P.P.U., function word connects the P.P.U., to the DT220 Dual Access Coupler?

COUPLER WORKSHEET-2

1. What is the purpose of bit zero on normal output channel zero?

2. What signal gates the 16 bit data word, into the hardware controller?

3. When is the signal "Inpreq" used?

4. What is the initial frame count with format six?

5. With format four, frame count of one, what bits of data Reg., are gated through the write mux?

6. With a read mux decode of ten, what input pins to board C15 are used for data?

7. What is the purpose of the board in Loc. C22?

8. The Deadman Timer = "Terminate"; when the counter chip {C09} reaches a count of?

9. What is the purpose of normal output channel four?

10. When the P.P.U., is outputing, the data reg. is effectively a _____bit register.

11. Under what conditions will the latch at TP11 {C24} set?

12. How is the assembly/disassembly code sent to the coupler?

13. What causes the deadman timer to expire?

14. What code on pins 2 & 14 of the mux. chip at loc. 33 {C05}, will select the path from the H.C., to P.P.U.?

15. When is the FF at TP31 {C28} set?

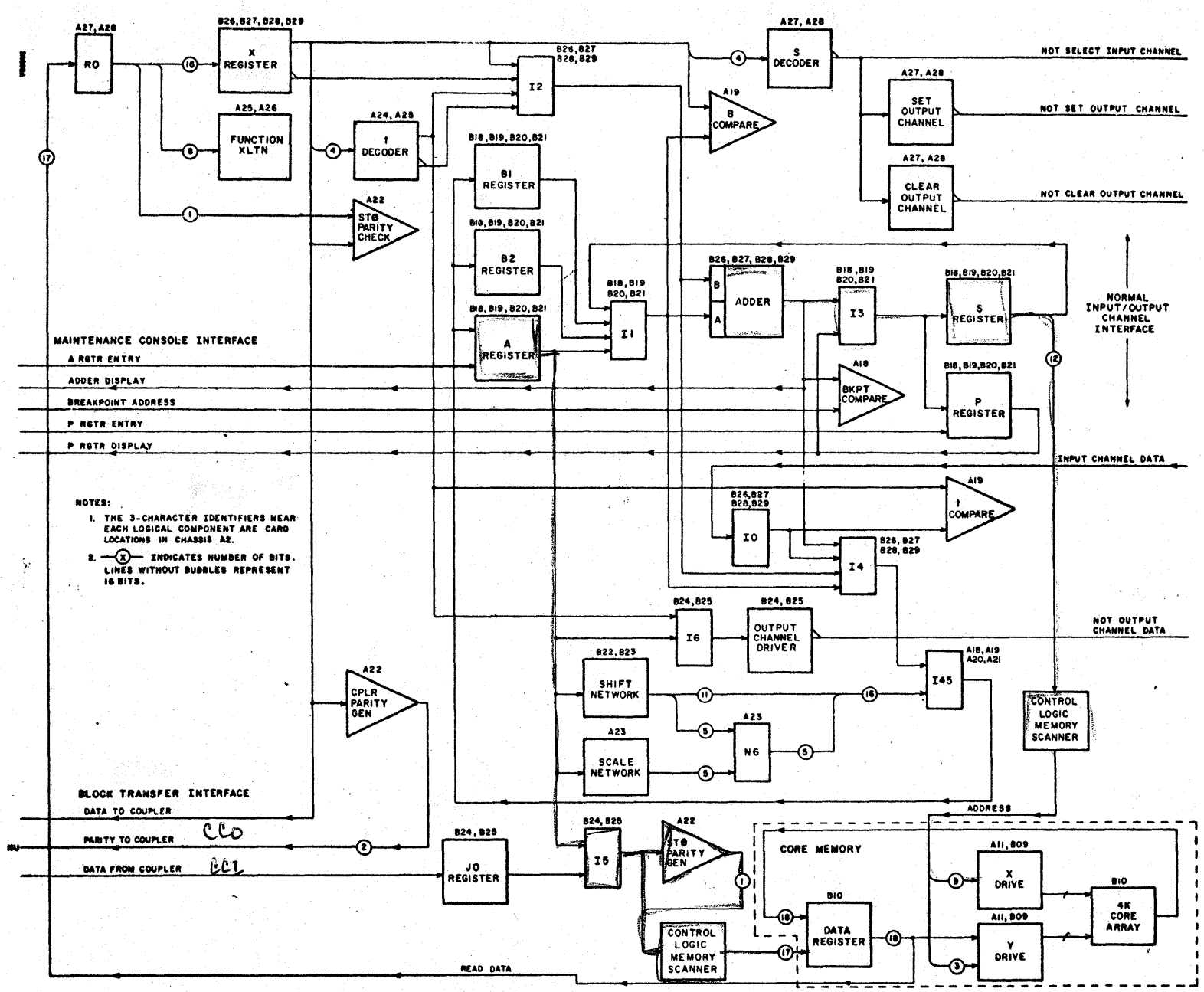


Figure 3-19. Subsystem Processor/Core Memory Data Flow

FA722 —— FA719

DIFFERENCE HANDOUTS

FA710

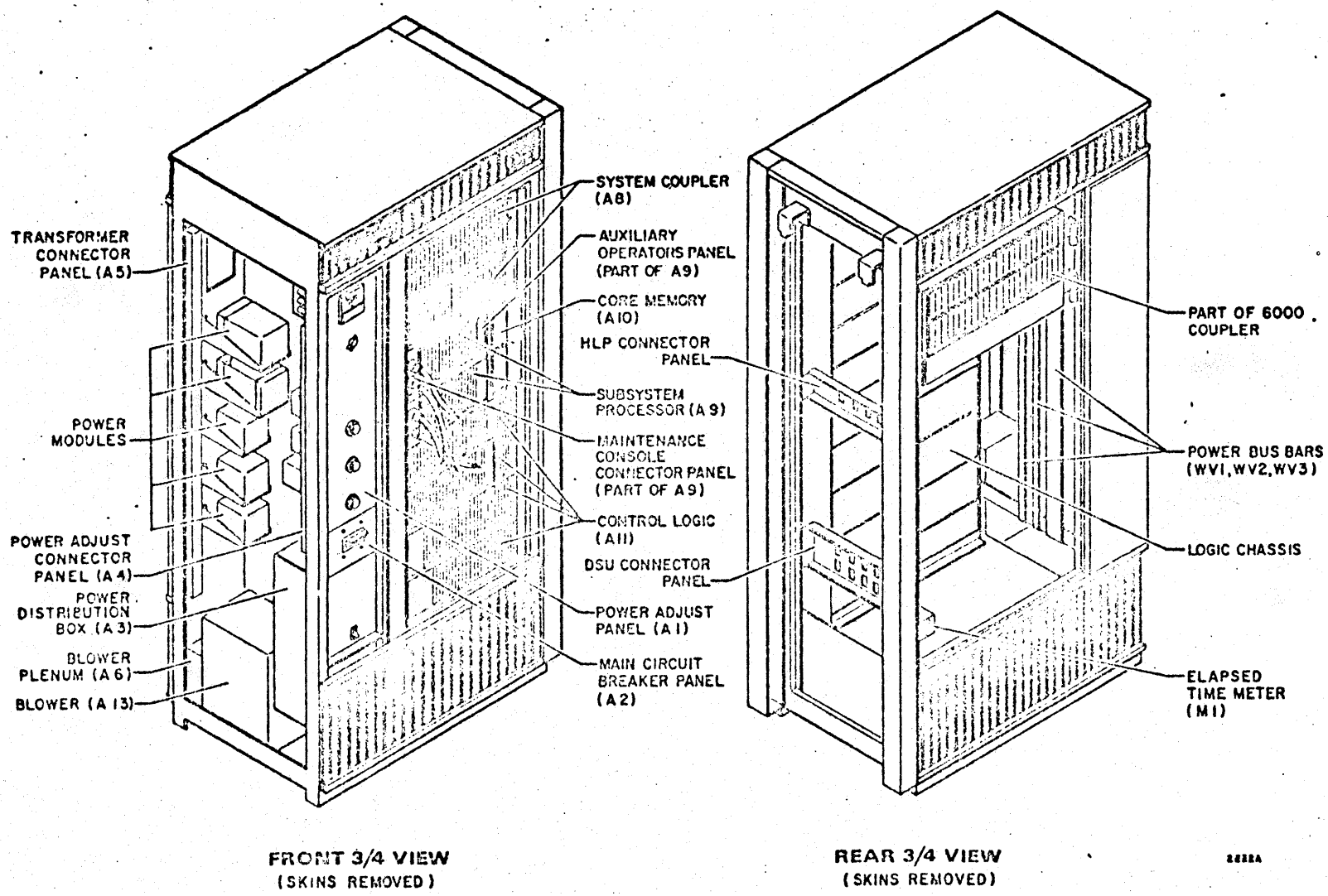
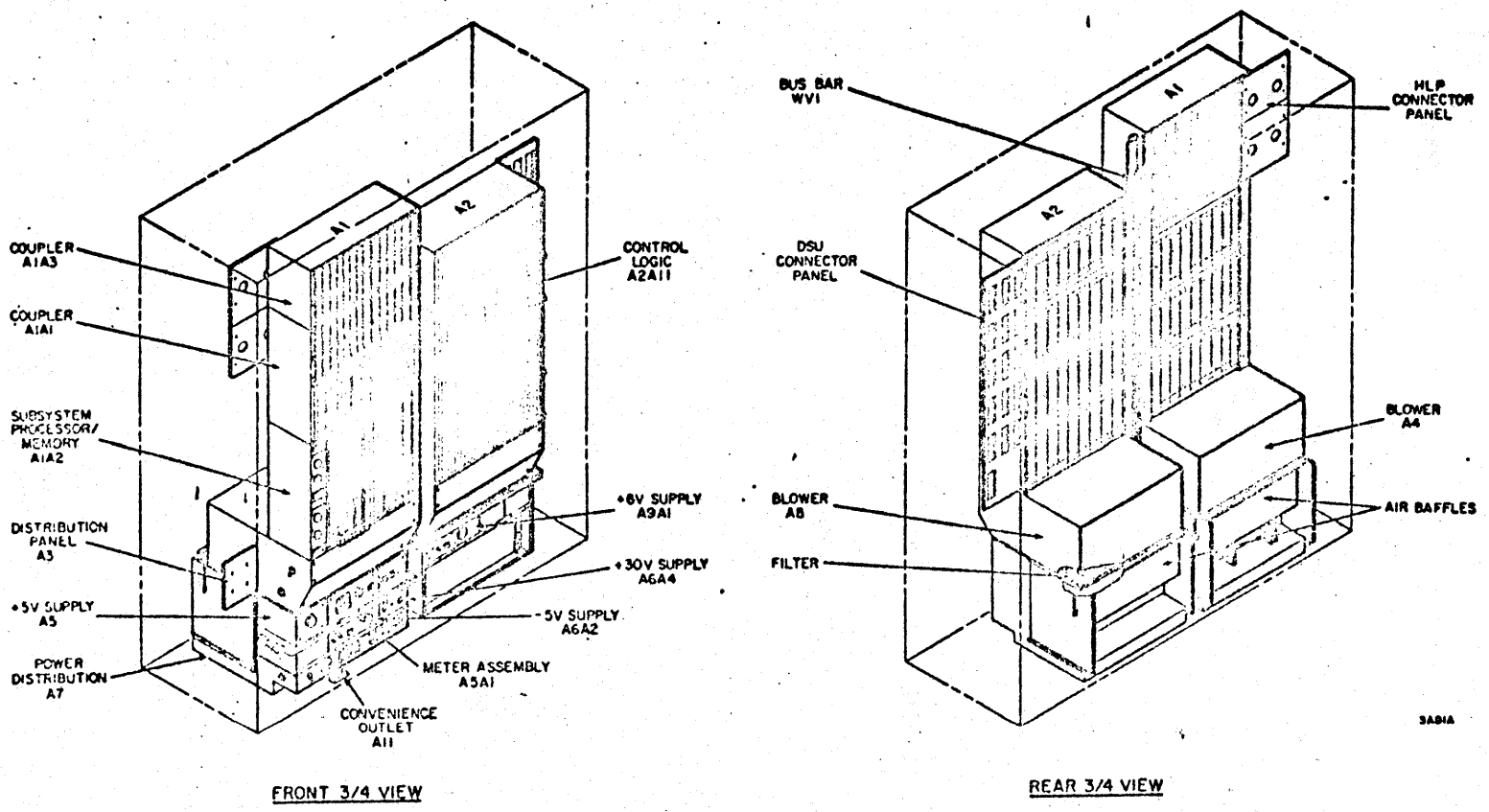


Figure 1-2. Component Location Diagram

FA719



NOTE

The coupler configuration shown is for the FA719. For the FA720, chassis A1A1 contains one row of TTL 25 PAKs and chassis A1A3 is omitted. The FA710 does not contain a coupler.

Figure 1-2. Component Location Diagram

CHANNEL ADAPTER CLOCK TUNING PROCEDURE

1. Refer to the data channel adapter clock diagram in Section 5, and to Figure 2-1. All pulse widths should be adjusted to within ± 2 nanoseconds unless otherwise noted.
2. Send a function signal to the channel adapter.
3. Check the relationship between the function signal and the 10MHZ clock. Be certain that the leading edge of function follows the leading edge of clock by 25 nanoseconds (±5 nanoseconds). If it does not, check the channel ouput to find the source of the problem.
4. Check $\overline{t55}$ (A11-TP5) and $\overline{t55}$ (A11-TP6) to be certain that both leading edges go high at the same time. If they do not, use one of the following procedures.
   a. If TP5 goes high after TP6, replace wire between A10-20 and A11-20 with a longer wire.
   b. If TP5 goes high before TP6, replace wire between A10-18 to A11-17 with a longer wire.

NOTE

Seven inches of wire equals 1 nanosecond of delay.

5. Check the function pulse width from A03-TP1. The pulse width should be 88 nanoseconds; if not, use one of the following procedures.
   a. If A03-TP1 is low for less than 88 nanoseconds, replace the wire between A10-3 and A11-14 with a longer wire.
   b. If A03-TP1 is low for more than 88 nanoseconds, shorten the wire between A10-3 and A11-14.
   c. If A03-TP1 is low for more than 88 nanoseconds, and the wire between A10-3 and A11-14 cannot be shortened, shorten the wire between A10-27 and B14-3.
6. Check the pulse width from A11-TP1. This should be 45 nanoseconds wide. If it is not, change the wire length between A10-4 and A11-10.

D.H.O. 3

7. Using $\overline{t55}$ (A11-TP5) as a reference, check $\overline{t20}$ (A11-TP3). Adjust the wire length between A10-19 and A11-18 so that $\overline{t20}$ comes up 35 nanoseconds before $\overline{t55}$.

8. Using $\overline{t55}$ (A11-TP5) as a reference, check $\overline{t35}$ (B11-TP2). Adjust the wire length between A10-2 and A11-11 so that $\overline{t35}$ comes up 20 nanoseconds before $\overline{t55}$.

9. Be sure that $\overline{t20}$, $\overline{t35}$, and $\overline{t55}$ are all 25-nanosecond pulses. If they are not, adjust the length of the following wires.

   $\overline{t20}$ - B04-14 to A11-13

   $\overline{t35}$ - A10-23 to A11-16

   $\overline{t55}$ - A10-21 to A11-15

   $\overline{t55}$ - A10-22 to A11-19

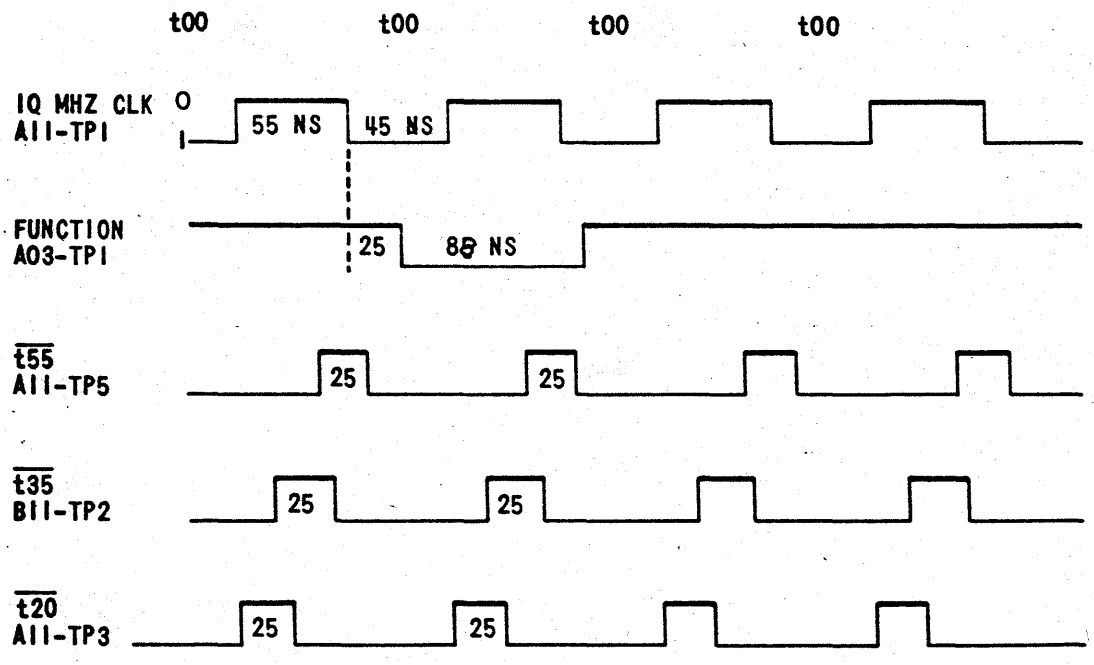
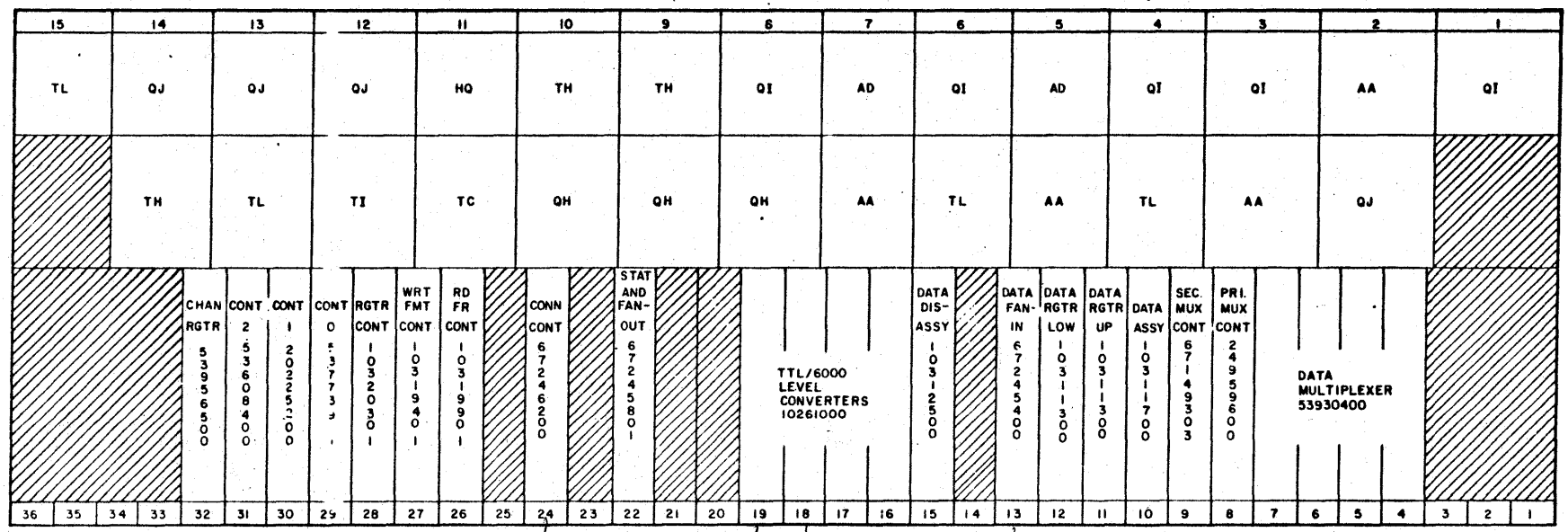


Figure 3-1. Clock Tuning Timing Diagram

D. H. O. -4

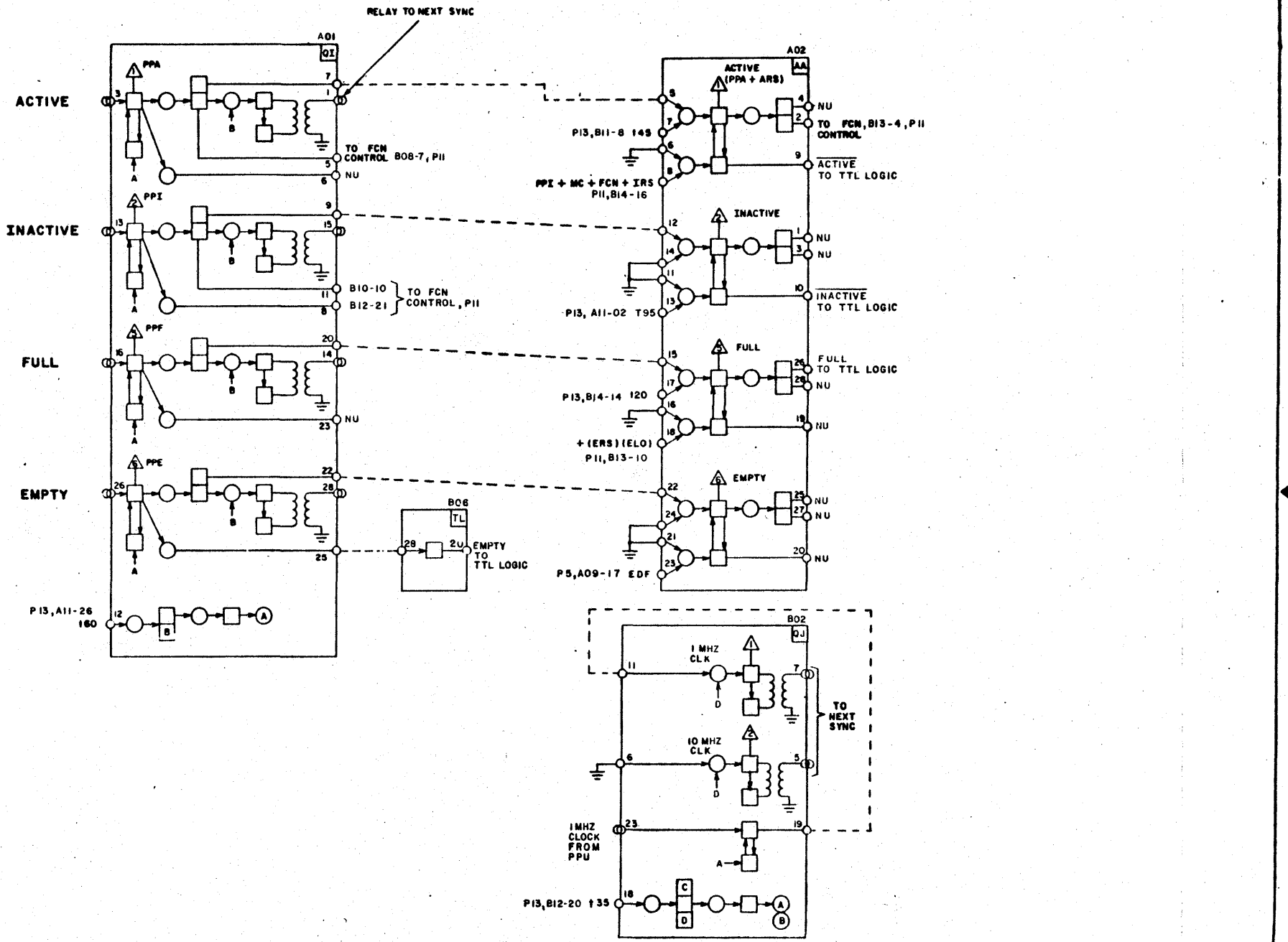
D. H.O. -5

FA719/FA401/FA402/DT220 COUPLER①



NOTES

① LOCATIONS C13, C18, C19, C22, AND C24 ARE PART OF THE DT220 ONLY. DT220 ALSO ADDS TWO ROWS IDENTICAL TO A AND B (ABOVE).



DEVELOPMENT DIVISION

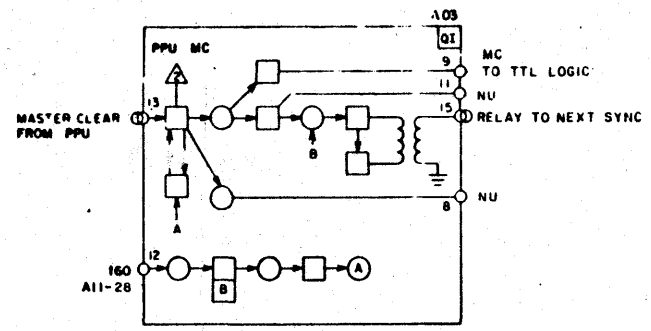
DATA CHANNEL ADAPTER CONTROL TO DEVICE

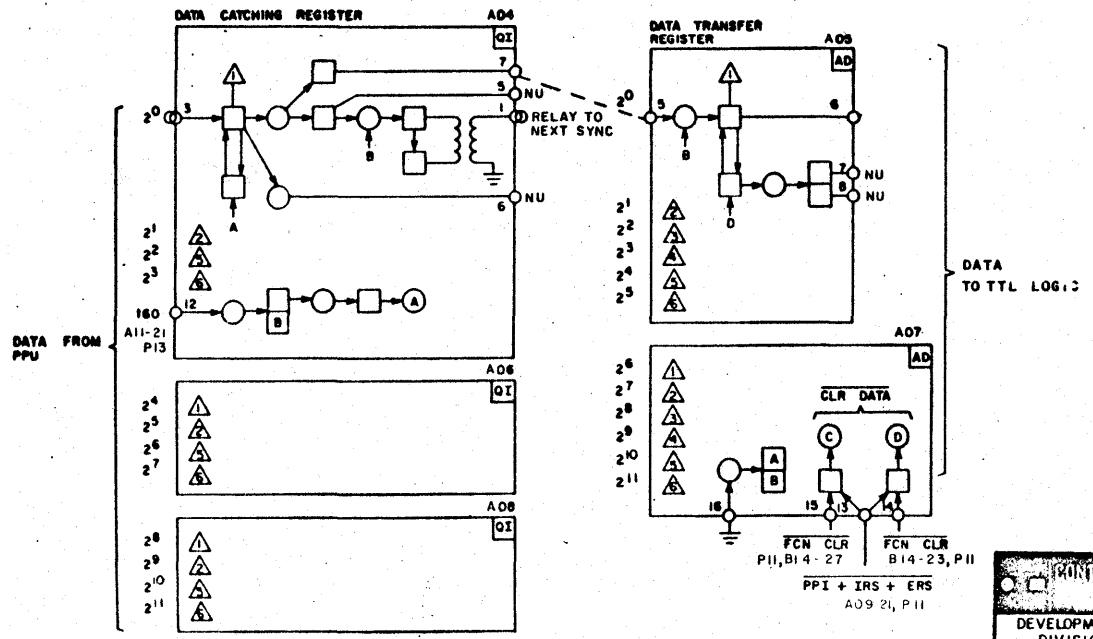
PRODUCT: 6000 COUPLER

SIZE: C | DRAWING NO: 60416400 | REV

SHEET | PAGE: 1

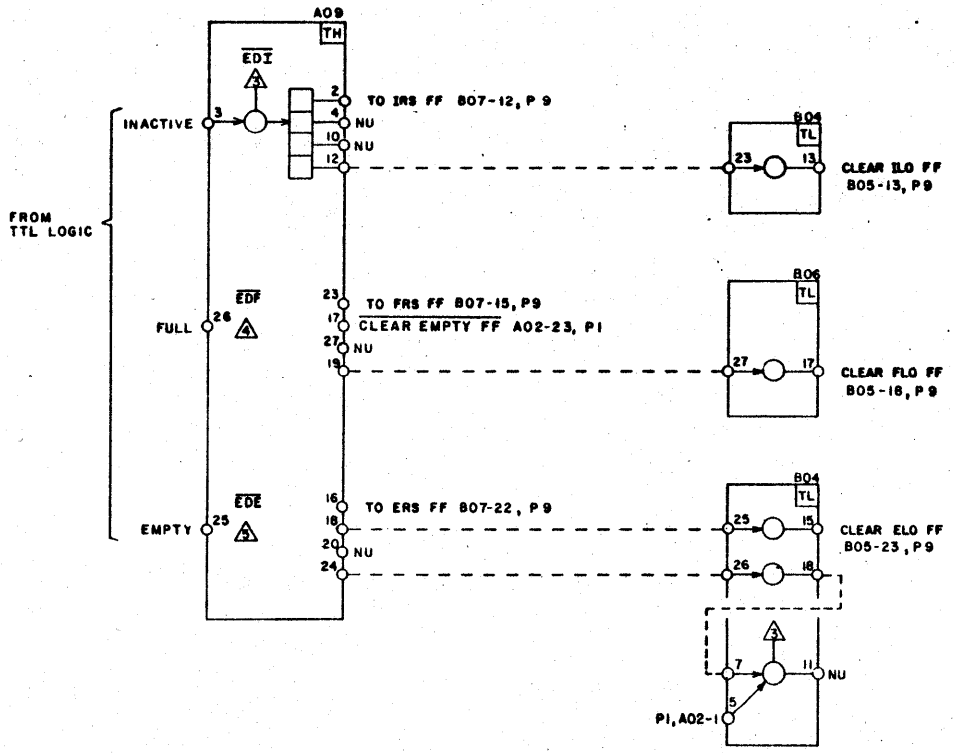
D.H.O.-6





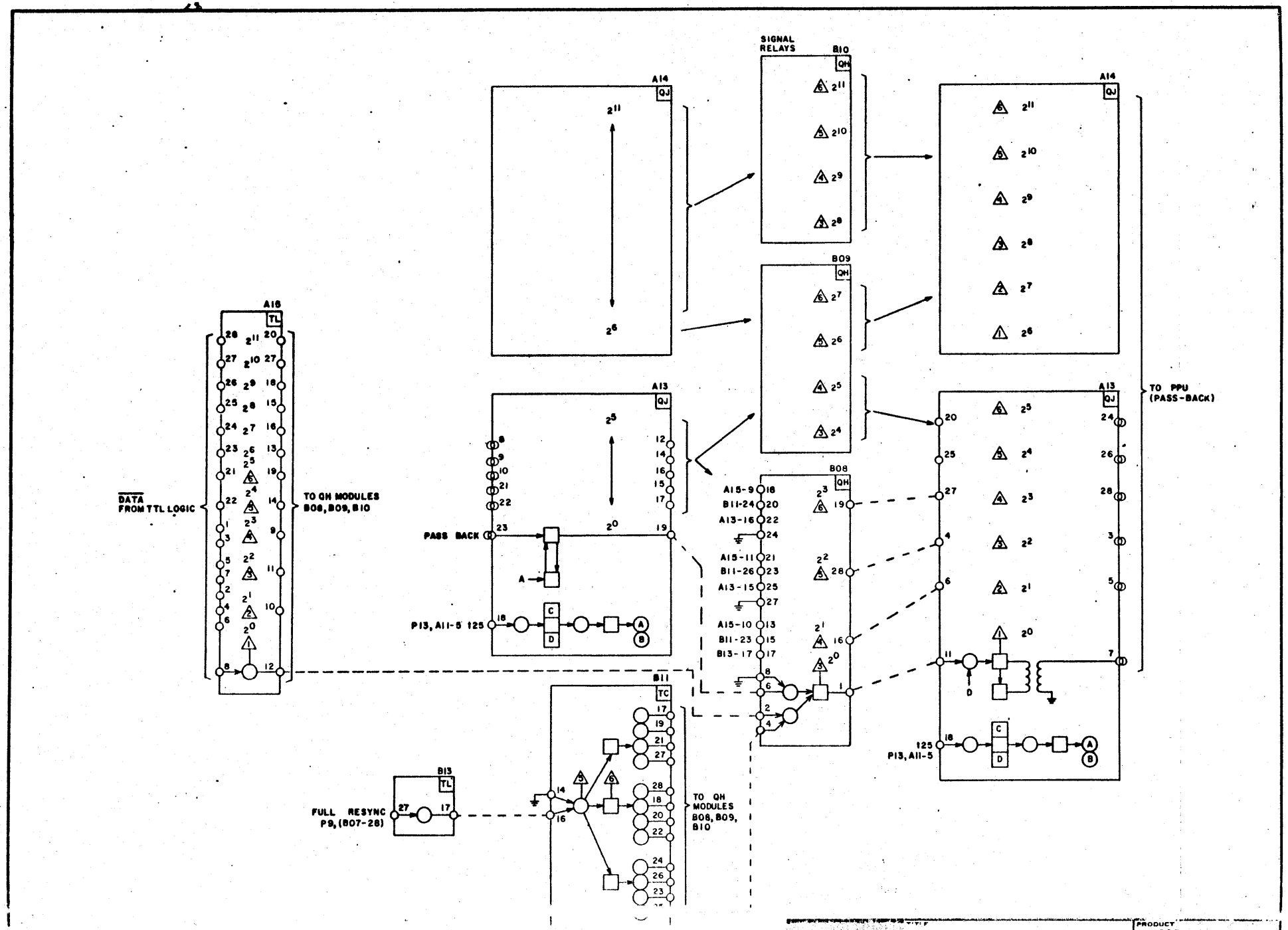
CONTROL DATA DEVELOPMENT DIVISION	DATA CHANNEL ADAPTER MASTER CLEAR AND DATA REGISTERS	6000 COUPLER	
		C 60416400	

D.H.O. -7

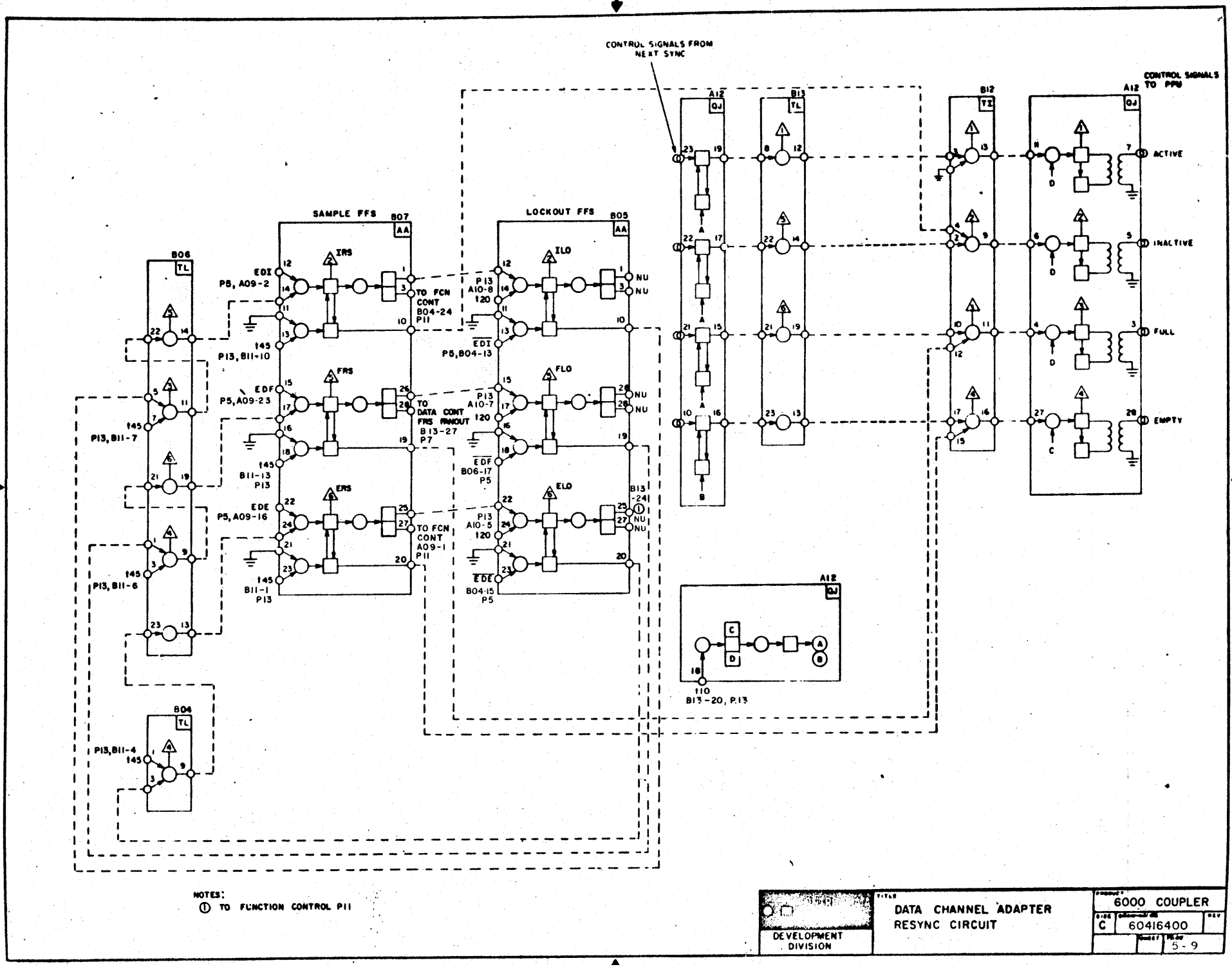


CONTROL DATA DEVELOPMENT DIVISION	TITLE DATA CHANNEL ADAPTER EXTERNAL DEVICE CONTROL SIGNAL FANOUTS	PRODUCT 6000 COUPLER	
		SIZE C	DRAWING NO 60416400
		SHEET	PAGE 5-5

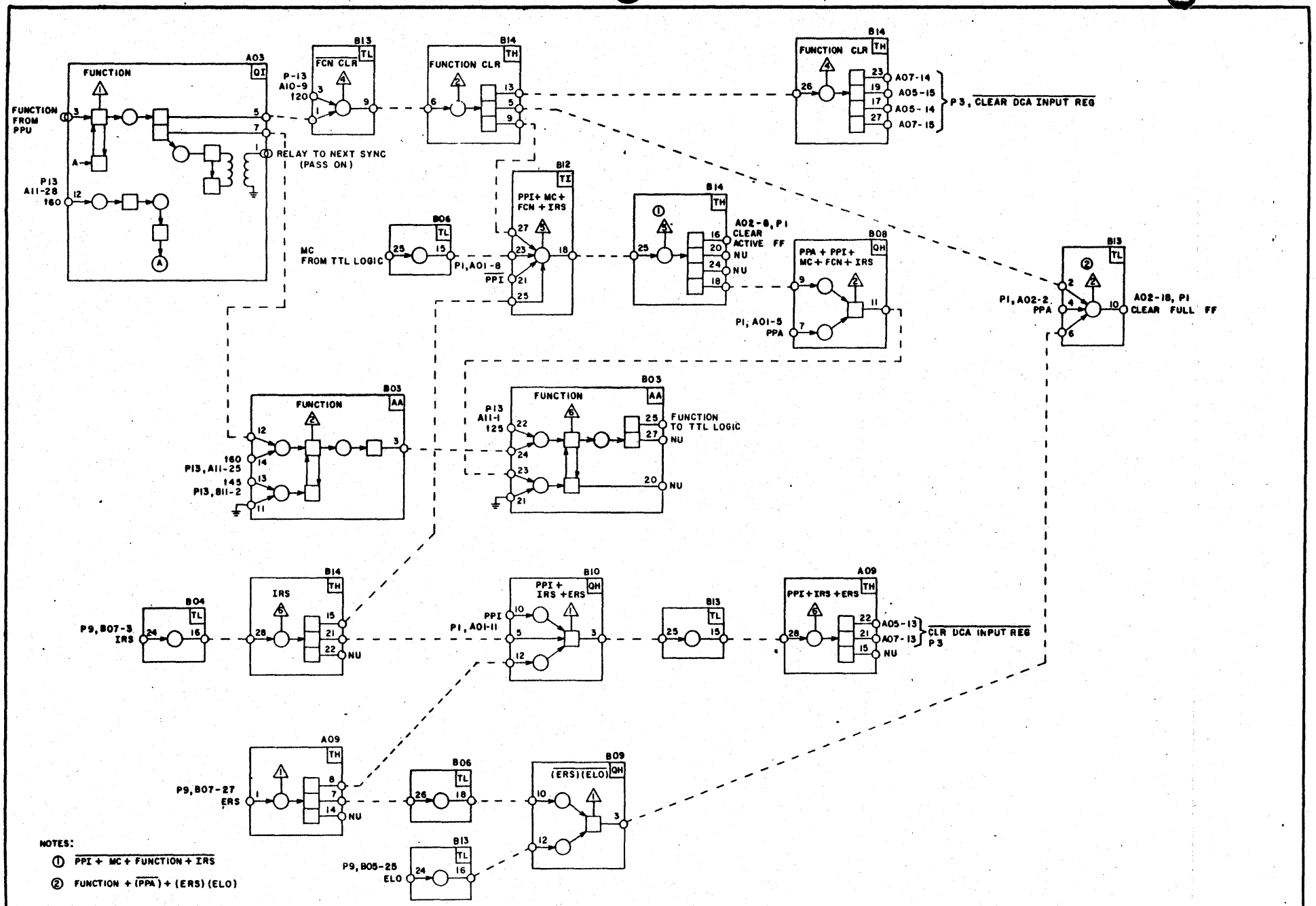
8-10.4.1


SIGNAL RELAYS
B10
QH
A14
QJ
B09
A13
B08
A16
TL
B11
TC
B13
DATA FROM TTL LOGIC
TO QH MODULES B08, B09, B10
PASS BACK
P13, A11-5 125
FULL RESYNC P9, (B07-28)
TO QH MODULES B08, B09, B10
TO PPU (PASS-BACK)
125 P13, A11-5

D.H.O. - 9


CONTROL SIGNALS FROM NEXT SYNC
CONTROL SIGNALS TO PPU
SAMPLE FFS
LOCKOUT FFS
ACTIVE
INACTIVE
FULL
EMPTY
TO FCN CONT B04-24 P11
TO DATA CONT FRS FANOUT B13-27 P7
TO FCN CONT A09-1 P11
NOTES:
① TO FUNCTION CONTROL P11
DEVELOPMENT DIVISION
DATA CHANNEL ADAPTER
RESYNC CIRCUIT
6000 COUPLER
C
60416400
5-9

D.H.O.-10



CONTROL DATA
DEVELOPMENT DIVISION

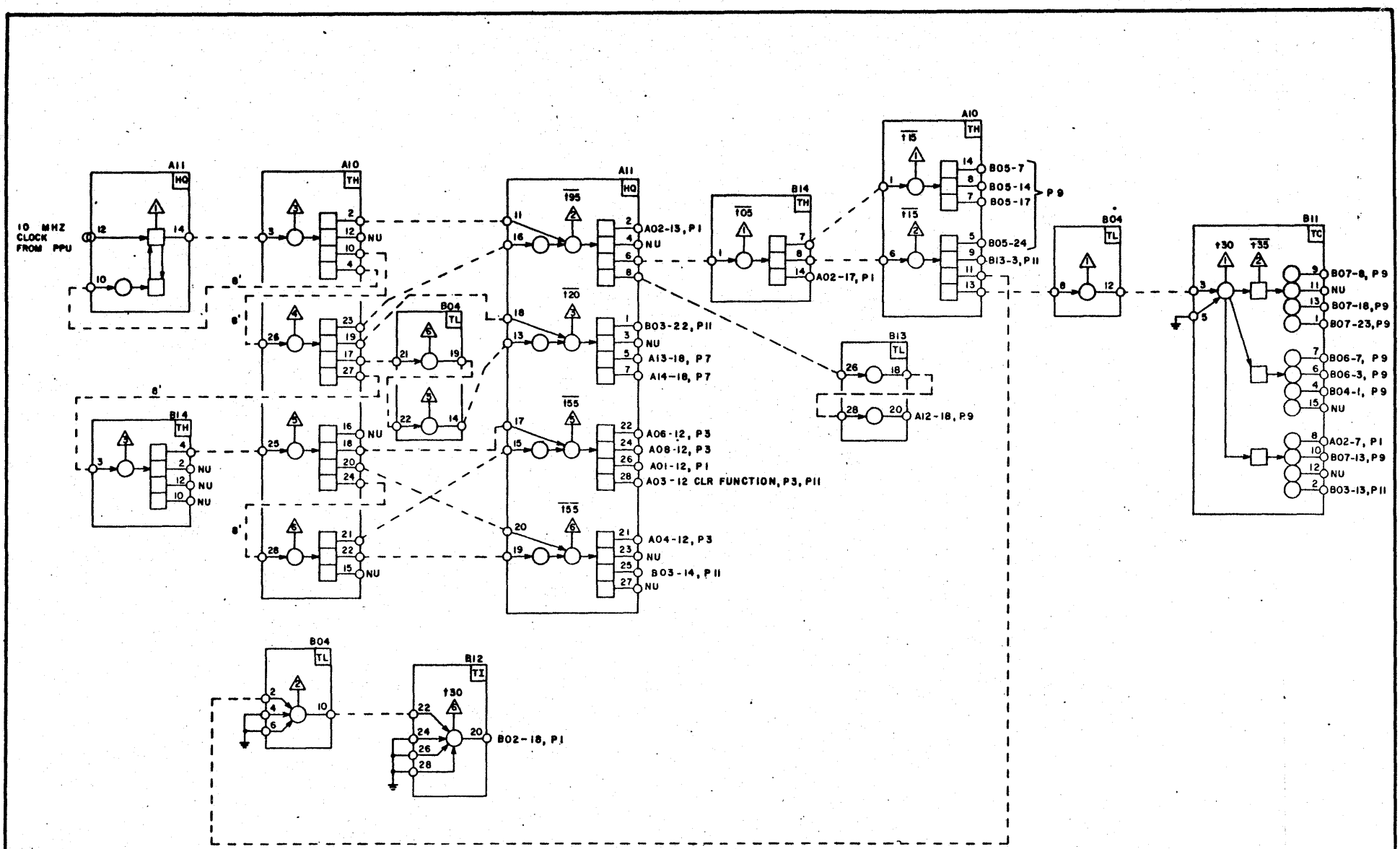
TITLE
DATA CHANNEL ADAPTER
FUNCTION CONTROL

PRODUCT
6000 COUPLER

SIZE C | DRAWING NO 60416400 | REV

SHEET | PAGE 5-11

D.H.0-11



CONTROL DATA DEVELOPMENT DIVISION

TITLE: DATA CHANNEL ADAPTER CLOCK

PRODUCT: 6000 COUPLER

SIZE C | DRAWING NO 60416400 | REV

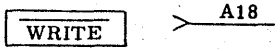
SHEET | PAGE 5.13

D 40-12

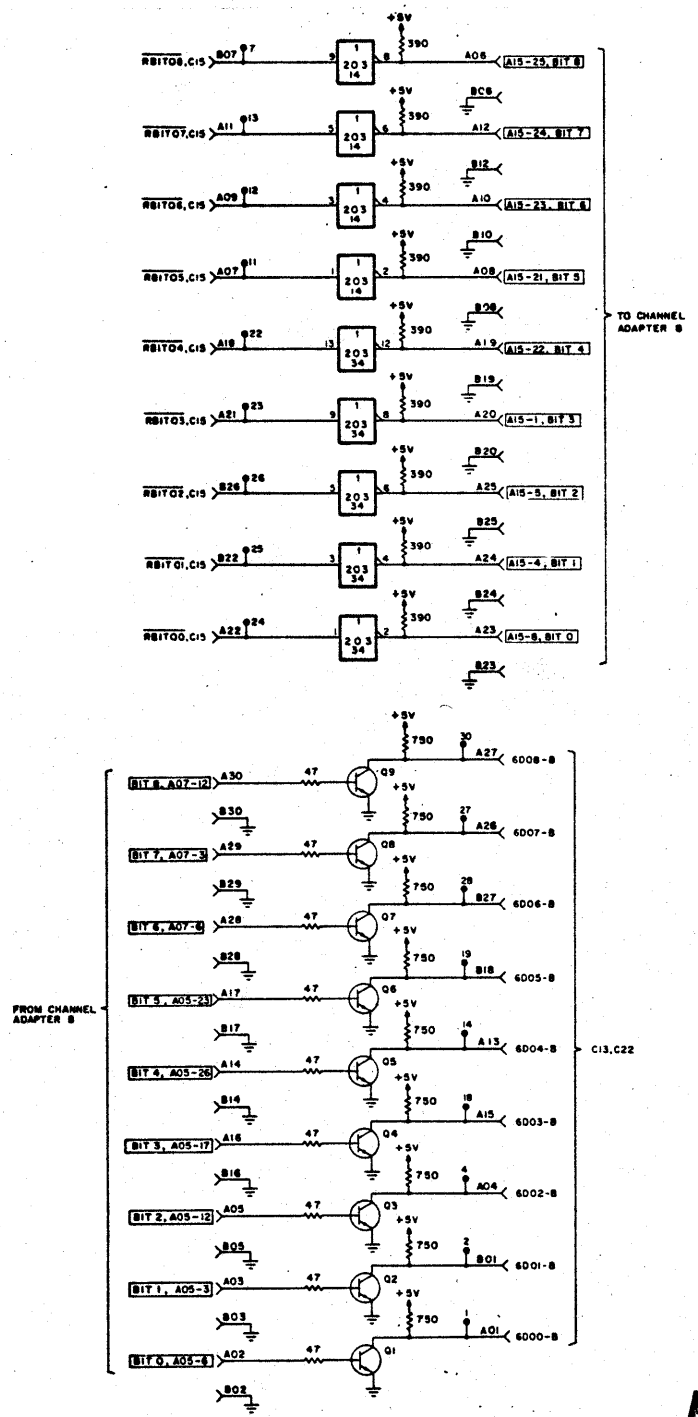
COUPLER INTERCHASSIS WIRES

Table 5-1 lists all signals which are sent between the coupler and the subsystem processor and between the coupler and the subsystem control logic. The top of each column indicates the direction of the signal. The location of the 25-pak and the connector pin number of the origin and destination are shown. In most cases, the location in the FA719 processor is the same as the location in the FA401/FA402 processor.

In the coupler logic diagrams, all signals listed on this sheet are enclosed in a rectangle to indicate that they are interchassis signals. For example, on the logic diagram for the 25-pak at location CO8, this signal appears as follows:



D.H.O.-13



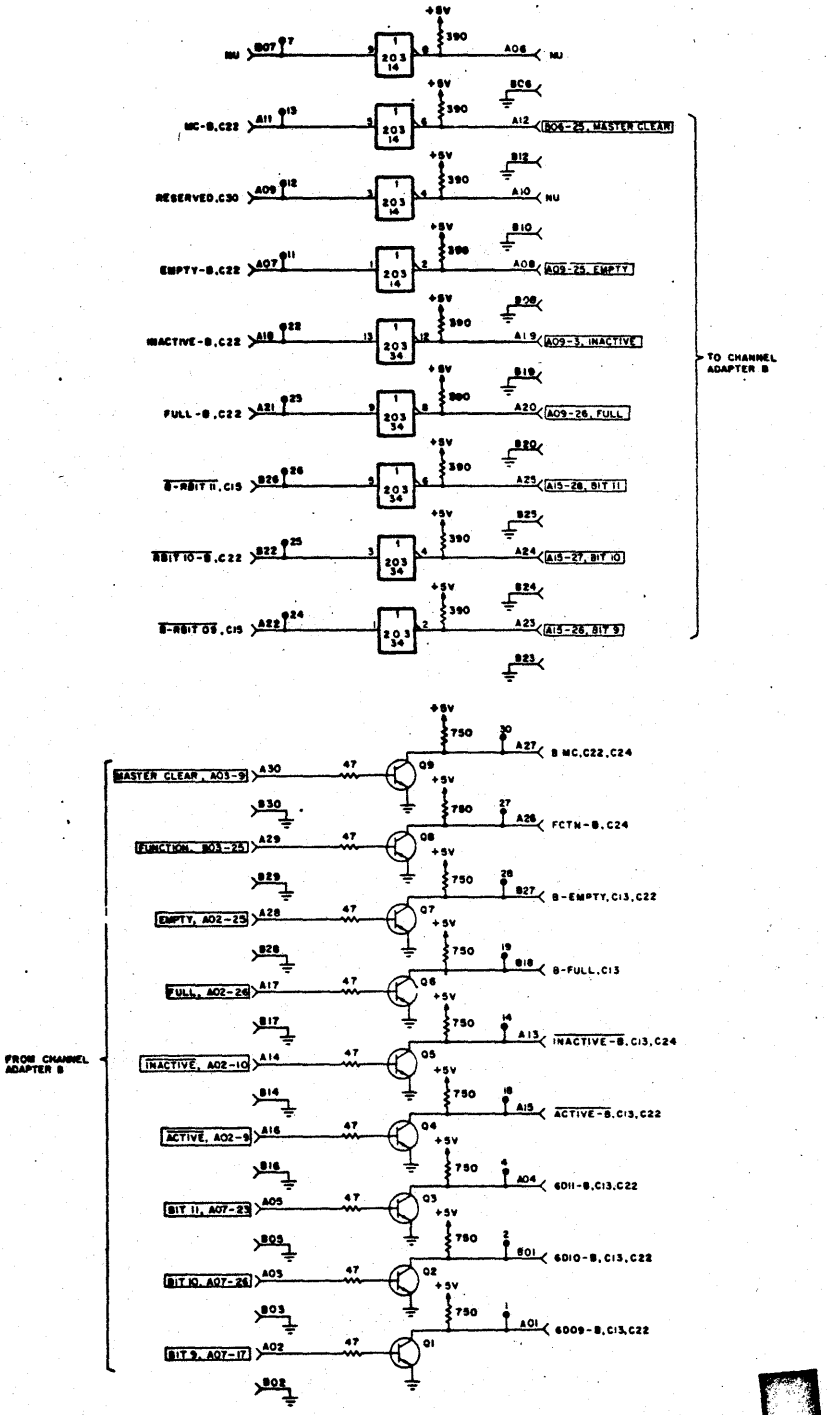
TTL/6000 LEVEL TRANSLATORS (B)
(DT220 ONLY)

PUB NO: 60416400

ASSY NO: 1026000 LOC: C15

60416400 C

D.H.O. — 14



PUB NO: 60416400

TTL/6000 LEVEL TRANSLATORS (B)
(DT220 ONLY)

ASSY NO: 1026000 LOC: C19

60416400 C

D.H.O.-15

WRITE/FORMAT CONTROL (C27)

FORMAT SELECTION

The processor selects the assembly/disassembly format by sending a code in normal output channel 0, bits 2^0-2^3. The format decode chip at location 24 translates this code. A function code from the channel automatically selects format 6 (0110). When the function sequence is complete, the format returns to the previous selection.

WRITE MUX DECODE

The write mux decode bits sent from connector pins B19, B20, B22, and B23 are used to control assembly of data during a transfer from the channel. The write mux decode bits form a dynamic code which enables one of several combinations of input bits into the assembly chips at chassis location C10 and C15.

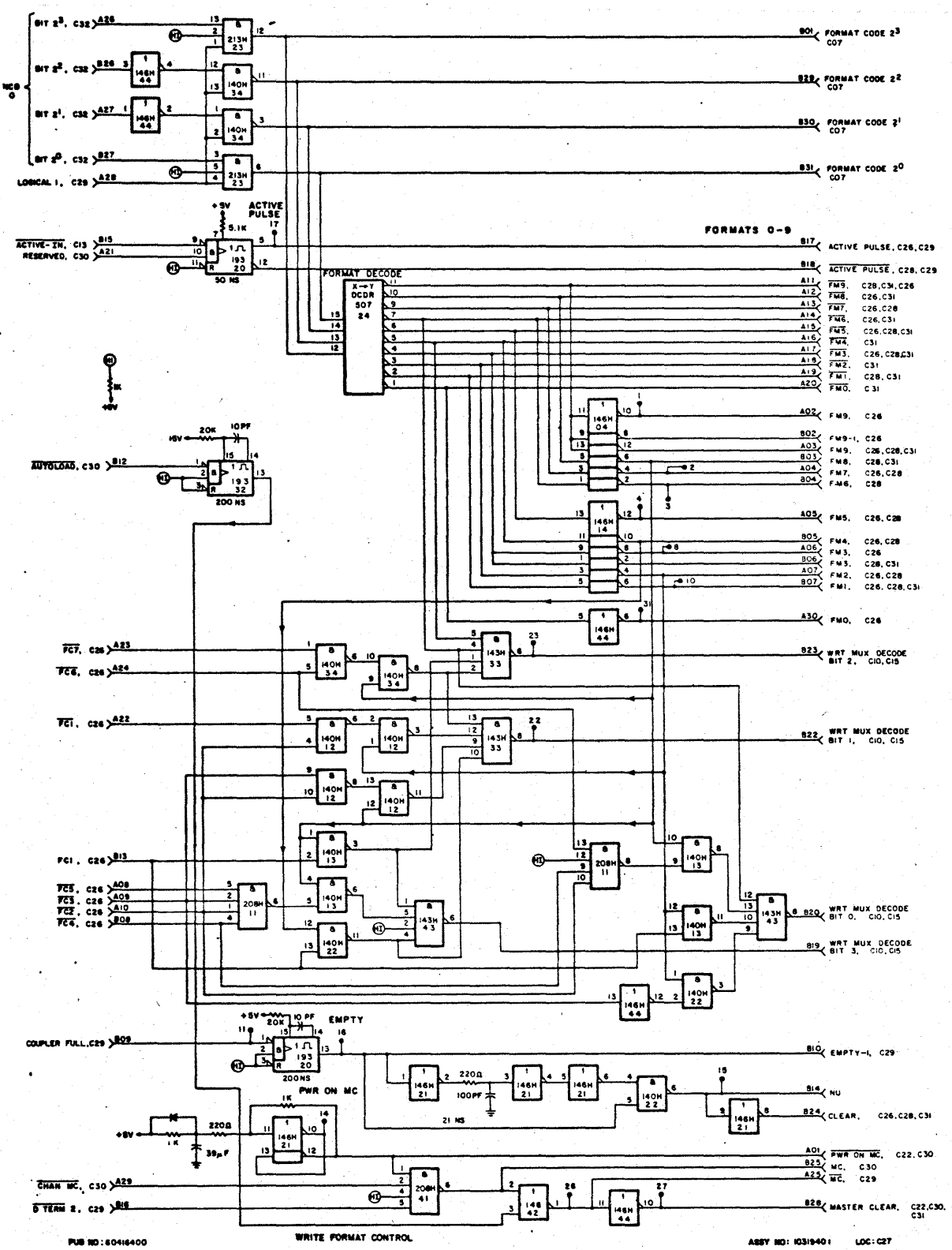
The write mux decode is determined by format and frame count. The format sets a count in the frame counter at chassis location C26. As the counter decrements, the mux decode changes to enable the assembly procedure.

MASTER CLEAR

Any one of the following conditions will master clear the coupler.

1. Applying power to the coupler provides a PWR ON MC
2. Receiving a master clear signal from the channel (CHAN MC) (if the coupler is connected)
3. Expiration of the deadman timer (DTERM 2)
4. Initiating an autoload sequence

04.0-16



PUB NO: 60416400

ASSY NO: 10319401 LOC: C27

60416400 C

B24

D. H.O. - 17

REGISTER CONTROL (C28)

The circuits on this board control the loading of data into the upper and lower data registers (locations C11 and C12). They determine if the registers are full or empty, determine which register should be loaded, control the timing, and clear the registers. These items are described below.

LOAD

A 1 from pin 8 of the 208 chip at location 44 enables loading data into the data register. A 1 is caused by one of the following conditions.

1. The coupler receives a function pulse from the PPU.
2. The coupler receives a full pulse from the PPU. This indicates that the PPU has transferred a data byte to the adapter holding register.
3. The coupler receives an output ready signal from the processor or a COREQ signal from the control logic. Either of these will set the OUTRDY2 latch, causing pin 4 of the 193 chip at location 42 to go to 0 for 50 nanoseconds when TP 30 changes from a 1 to a 0. This indicates that the coupler data register is not full and can receive a data byte from the processor or control logic.

The J/K flip-flop at location 32 determines whether the data byte will be loaded into the data register upper (C11) or the data register lower (C12). If TP 28 is a 1 when the load enable comes up, data will be gated into the lower register; if TP9 is a 1, data will be gated into the upper register. If format 6 or 7 is selected, data is always gated into the upper register. A 1 to 0 transition at pin 1 of the flip-flop toggles it. The flip-flop toggles when the coupler is in data mode (TP31 = 1), and one of the following conditions occurs.

1. The coupler returns an empty to the PPU.
   (This is a response to a full signal from the PPU during a PPU to coupler transfer if the data register is not full and the channel is reserved.)
2. The coupler generates a $\overline{\text{BUFFUL}}$ signal.
   (This indicates that the coupler received an output ready signal or an output data request, and the data register is not full.)

The upper full or lower full flip-flop sets when a data byte is gated into the upper data register (C11) or the lower data register (C12). This occurs when the $\overline{\text{LOADUPPER}}$ or $\overline{\text{LOADLOWER}}$ (connector pin B22 or A27) signal is generated.

The upper full or lower full flip-flop clears. One of the following conditions clears the register and flip-flop.

The coupler receives a CKDAP from the processor or a CIRDLY from the control logic. This indicates that the coupler has been [illegible] from the PPU. The clear occurs when the frame count and format enable it.

The correlation between format, frame count, and clearing the register is shown below.

Write (From the PPU)

Clear Upper		Clear Lower	
Format	Count	Format	Count
0	1	0	1
2	1 and 3	2	1 and 2
4	2	4	1
6	1	6	--
8	1, 3, 4, 6, and 7	8	1, 2, 4, 5, and 6

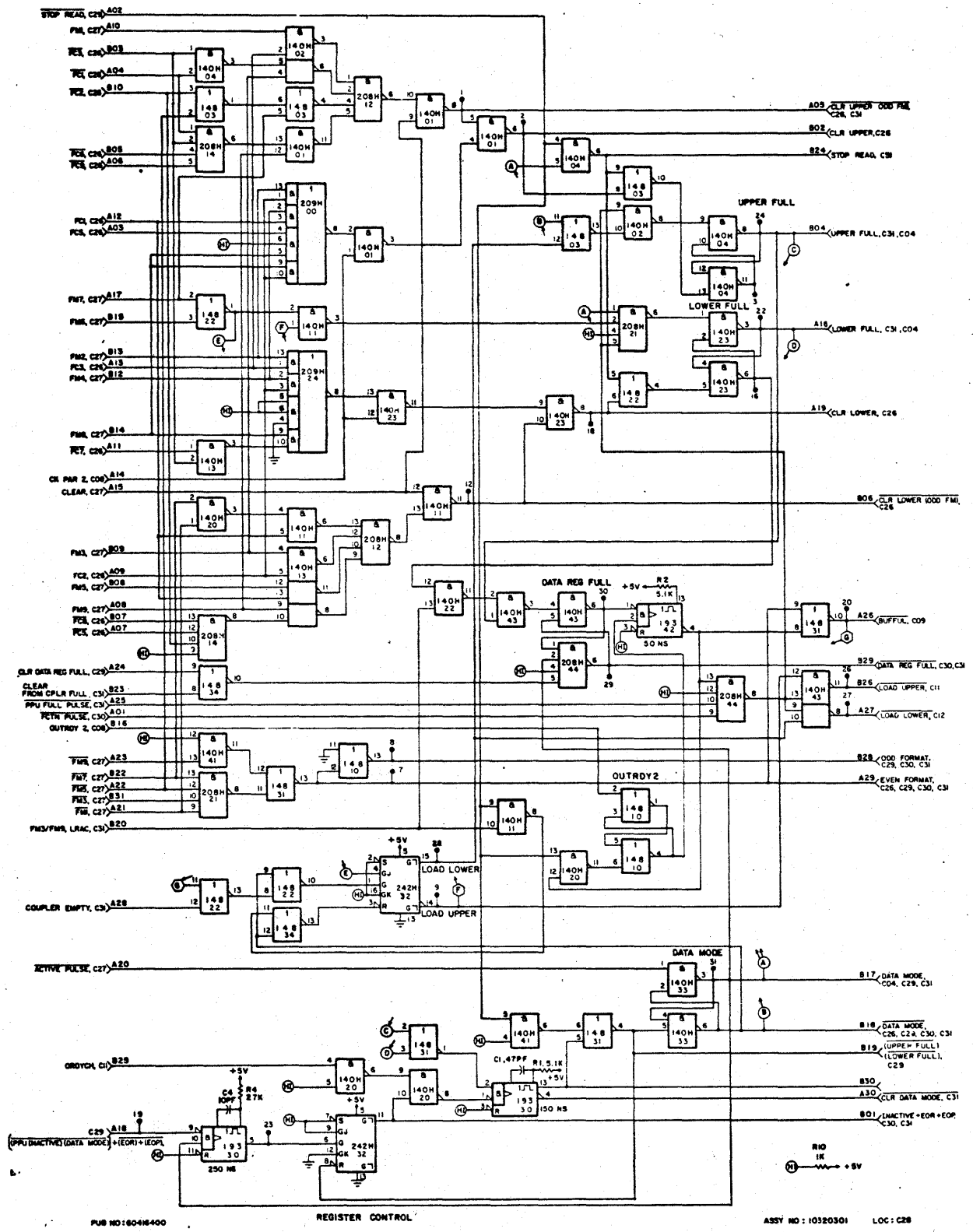
Read (To the PPU)

Clear Upper		Clear Lower	
Format	Count	Format	Count
1	3	1	1
3	1	3	2
5	2	5	1
7	-	7	1
9	1, 3, 6, and 9	9	2, 5, and 8

Data Mode

The data mode flip-flop sets when the coupler has been reserved by a PPU and the coupler receives an active pulse from the PPU. This indicates that the coupler has been properly functioned and is ready to transfer data. Data mode flip-flop clears when coupler receives one of the following signals.

1. Inactive from the processor
2. EOR CC from the processor
3. EOR IN from the control logic
4. Initialize pulse from PPU
5. Power clear


STOP READ, C29) A02
FM6, C27) A10
FC1, C26) B03
FC7, C26) A04
FC2, C26) B10
FC4, C26) B05
FC5, C26) A06
FC1, C26) A12
FC3, C26) A03
FM7, C27) A17
FM8, C27) B19
FM2, C27) B13
FC3, C26) A13
FM4, C27) B12
FM5, C27) B14
FC7, C26) A11
CK PAR 2, C08) A14
CLEAR, C27) A15
FM3, C27) B09
FC2, C26) A09
FM5, C27) B08
FM9, C27) A08
FC6, C26) B07
FC5, C26) A07
CLR DATA REG FULL, C29) A24
CLEAR FROM CPLR FULL, C31) B23
PPU FULL PULSE, C31) A25
PCTN PULSE, C30) A01
OUTRDY 2, C08) B16
FM5, C27) A23
FM7, C27) B22
FM6, C27) A22
FM3, C27) B31
FM1, C27) A21
FM3/FM9, LRAC, C31) B20
COUPLER EMPTY, C31) A28
ACTIVE PULSE, C27) A20
GROYCH, C11) B29
C29) A18 (PPU INACTIVE) (DATA MODE) + (EOR) + (EOP)
A09 CLR UPPER ODD FM, C26, C31
B02 CLR UPPER, C26
B24 STOP READ, C31
UPPER FULL
B04 UPPER FULL, C31, C04
LOWER FULL
A16 LOWER FULL, C31, C04
A19 CLR LOWER, C26
B06 CLR LOWER (ODD FM), C26
DATA REG FULL
+5V
R2 5.1K
50 NS
A26 BUFFUL, C09
B29 DATA REG FULL, C30, C31
B26 LOAD UPPER, C11
A27 LOAD LOWER, C12
B28 ODD FORMAT, C29, C30, C31
A29 EVEN FORMAT, C26, C29, C30, C31
OUTRDY2
LOAD LOWER
LOAD UPPER
DATA MODE
B17 DATA MODE, C04, C29, C31
B18 DATA MODE, C26, C2A, C30, C31
B19 (UPPER FULL) (LOWER FULL), C29
B30 A30 CLR DATA MODE, C31
B01 (INACTIVE + EOR + EOP, C30, C31
C1 .47PF
R1 5.1K
150 NS
C4 10PF
R4 27K
250 NS
R10 1K
PUB NO: 60416400
REGISTER CONTROL
ASSY NO: 10320301
LOC: C28

B22

D. H-O. 19

CONTROL 0 (C29)

FULL TO PPU/COUPLER FULL

Full to PPU is the pulse sent through the status and data fan-in (C22) and channel adapter to the PPU to indicate that the coupler has data on the lines for the PPU.

Full to PPU is generated when the coupler data register is full (that is, has data available), the format and frame count is correct, and one of the following occurs.

1. The coupler receives an empty from the PPU during a read operation.
2. The read operation is disabled; this empties the remaining data from the coupler read registers.

Coupler full generates an empty signal (at C27) which prevents generation of further full-1 pulses until the first one dissipates. Coupler full also generates a clear signal which decrements the frame counter.

GENERATE EOP

The end of operation signal is sent to the control logic when the processor sends an inactive (sets bit 2^2 of NCO 0) signal, when the channel sends an inactive during a PPU data read, or when a PPU write operation is terminated.

CLEAR DATA MODE

A 0 from connector pin B12 clears the data mode flip-flop at chassis location C28. This is caused by the termination of a data transfer. When this flip-flop is clear, the coupler cannot transfer data. The 0 from B12 occurs when the data mode flip-flop is set, and the coupler receives one of the following signals.

1. Inactive from the PPU
2. EOP-CC from the processor
3. EOR-IN from the control logic

STOP READ/DISABLE READ

A read operation (odd format) is stopped when the signal from connector pin B04 goes to a 0. This is caused by one of the following conditions.

1. PPU sends an inactive to the coupler
2. Processor sends an inactive to the coupler
3. The coupler receives a master clear

$\overline{\text{Stop Read}}$ clears the data mode flip-flop at C28.

A 0 from A20 is caused by an inactive from the PPU. This signal initiates a terminate sequence, and disables a read operation.

CLEAR ENABLE

A 100-nanosecond pulse from pin 5 of the one-shot at location 42 clears the data register full flip-flop. This is generated when the decrement signal sets the clear enable latch if the coupler is not returning an empty to the PPU. If the coupler is returning an empty to the PPU, a 200-nanosecond pulse from pin 13 of the one-shot at location 42 disables the clear until the empty has been processed. This allows the data sent to the channel adapter from the register to stabilize before being cleared out.

NORMAL TERMINATE

During a PPU write, the PPU inactive pulse generates a normal terminate which clears data mode when the data register is empty. During a PPU read, an EOR from the control logic or an EOP from the processor generates a normal terminate pulse which clears data mode when the data register is empty.

HALT DECODE

The halt decode signal generates a master clear in the coupler when an autoload is initiated or when the deadman timer expires.

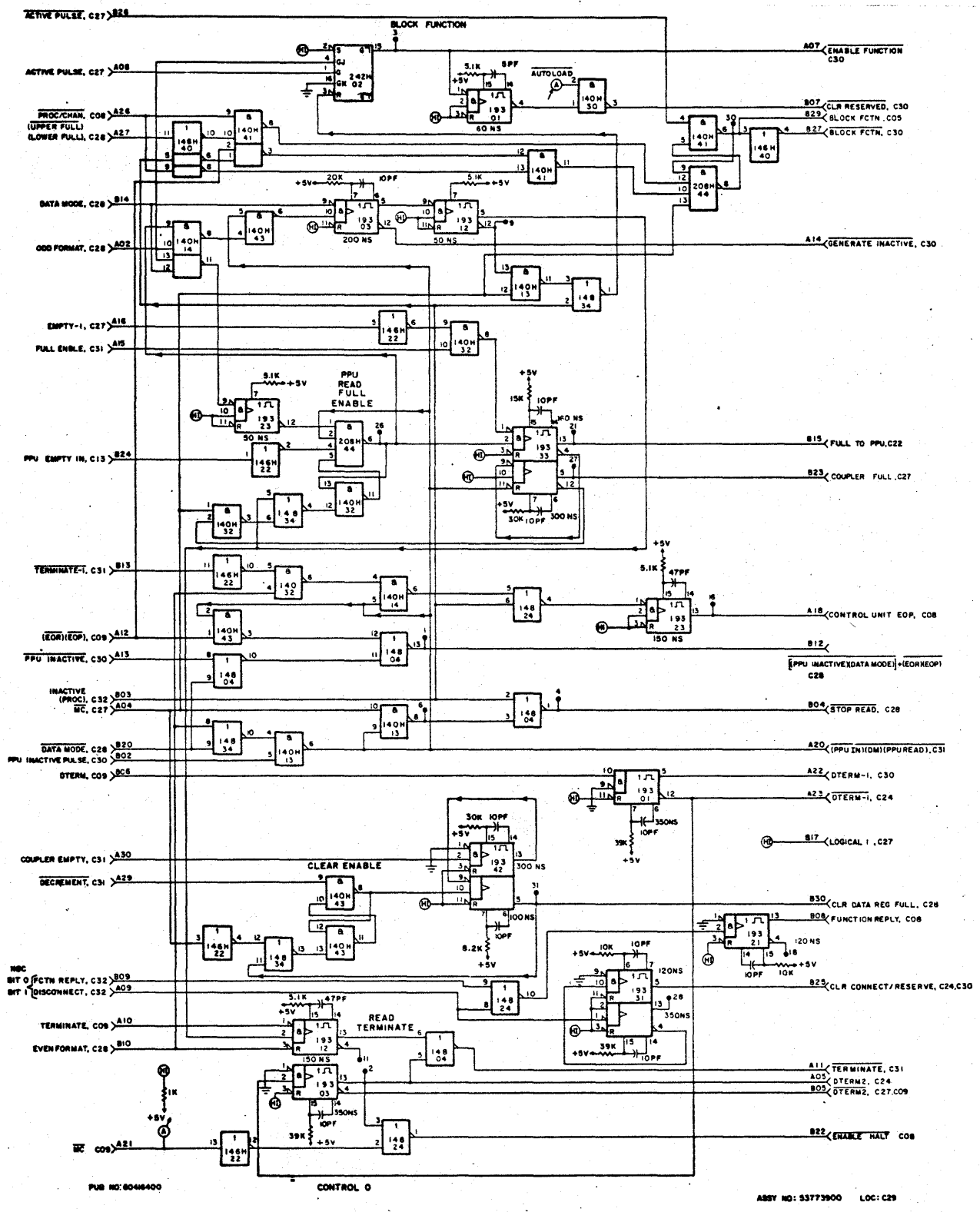
BLOCK FCN/ENABLE FUNCTION

To allow the function timing chain (at C30) to start, the $\overline{\text{BLOCK}}$ $\overline{\text{FCN}}$ signal from connector pin B27 must be a 1, and the enable function signal from A07 must be a 0.

The enable function signal disables the chain after a read operation has been initiated. When the read operation has been terminated and cleared, or when a write is initiated, this signal goes to a 0 and does not disable the chain.

The BLOCK FCN signal goes to a 0 when an active sets the latch (indicating that a function has been sent). The latch must be cleared to allow the next function to be processed. The latch is cleared by one of the following:

1. Master clear
2. An EOP from the processor
3. An inactive (bit 2^1 of NCO 0) from the processor
4. Clearing coupler data mode by terminating an operation in any way


ACTIVE PULSE, C27
BLOCK FUNCTION
ENABLE FUNCTION C30
CLR RESERVED, C30
BLOCK FCTN, C05
BLOCK FCTN, C30
PROC/CHAN, C08
(UPPER FULL)
(LOWER FULL), C28
DATA MODE, C28
ODD FORMAT, C28
GENERATE INACTIVE, C30
EMPTY-I, C27
FULL ENBLE, C31
PPU READ FULL ENABLE
FULL TO PPU, C22
PPU EMPTY IN, C13
COUPLER FULL, C27
TERMINATE-I, C31
CONTROL UNIT EOP, C08
(EOR)(EOP), C09
PPU INACTIVE, C30
[PPU INACTIVE•(DATA MODE)]+(EOR•EOP) C28
INACTIVE (PROC), C32
MC, C27
STOP READ, C28
DATA MODE, C28
PPU INACTIVE PULSE, C30
DTERM, C09
(PPU IN•(DM)(PPU READ), C31
DTERM-I, C30
DTERM-I, C24
LOGICAL 1, C27
COUPLER EMPTY, C31
DECREMENT, C31
CLEAR ENABLE
CLR DATA REG FULL, C28
FUNCTION REPLY, C08
CLR CONNECT/RESERVE, C24,C30
MBC
BIT 0 (FCTN REPLY, C32
BIT 1 (DISCONNECT, C32
TERMINATE, C09
EVEN FORMAT, C28
READ TERMINATE
TERMINATE, C31
DTERM2, C24
DTERM2, C27,C09
MC, C09
ENABLE HALT, C08
PUB NO: 60416400
CONTROL 0
ASSY NO: 53773900 LOC: C29

B27

D.H.O. -21

RESERVED (C30)

A legal function code sent to the coupler sets the reserved flip-flop if the coupler is not in data mode. To be legal, a function code must be equal to or less than 0477_8, and the equipment number must be zero (bits 9, 10, and 11 equal 0). The reserved flip-flop clears when the coupler receives an inactive signal from the PPU, the processor deactivates the coupler (sets bit 2^{13} of NCO 0), the coupler receives a master clear, or the deadman timer expires.

FUNCTION TIMING CHAIN

The function timing chain starts when the A-connect or B-connect flip-flop (at C24) is set, and a function signal is sent to the coupler from the connected PPU.

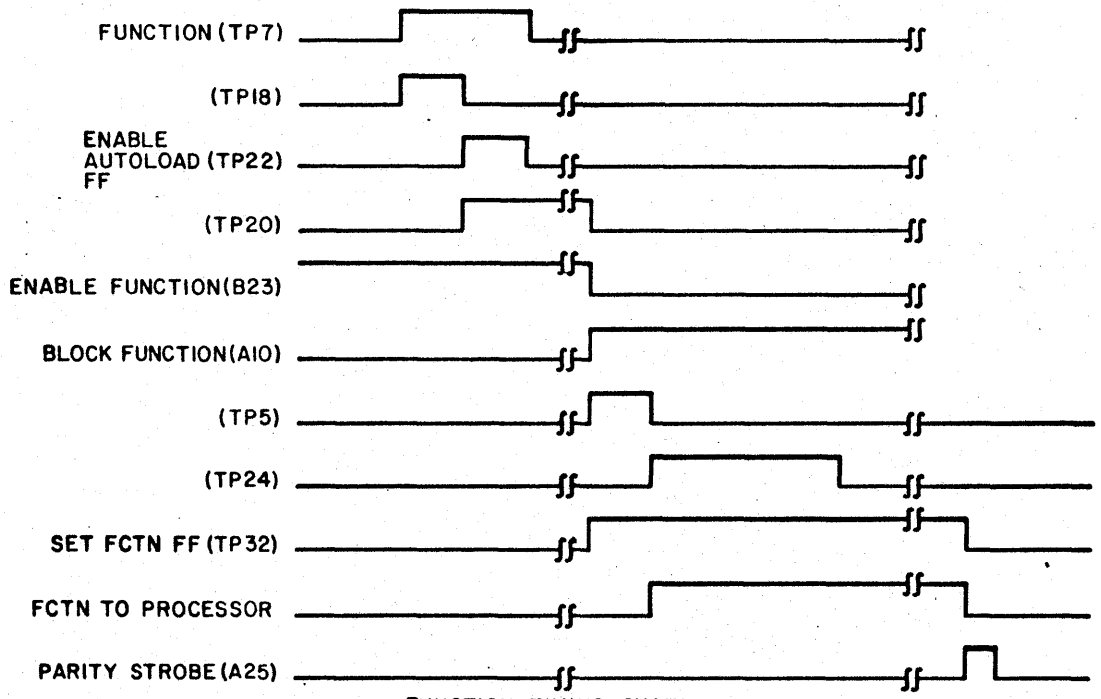
The first 50-nanosecond pulse clears the autoload flip-flop; the second 50-nanosecond pulse enables setting the autoload flip-flop if the autoload function (0414_8) is decoded; it also sets the J/K flip-flop at location 33 if the function code is legal. When TP 20 goes to a 1, it indicates that a function is being attempted.

To allow the timing chain to continue, the $\overline{\text{BLOCK FCN}}$ signal (connector pin A10) must be a 1, and $\overline{\text{ENABLE FUNCTION}}$ signal must be a 0 (connector pin B23). The $\overline{\text{ENABLE FUNCTION}}$ disables the chain by going to a 1 after a read operation has been initiated. When the read operation has been terminated and cleared, or when a write operation is initiated, the signal goes to a 0.

The $\overline{\text{BLOCK FUNCTION}}$ signal goes to a 0 following an active signal from the PPU. The active indicates that a function has been sent to the coupler. The $\overline{\text{BLOCK FUNCTION}}$ signal goes to a 1 when the function has been cleared. This prevents a second function from being processed until the preceding one has been cleared.

When $\overline{\text{BLOCK FCN}}$ is a 1, $\overline{\text{ENABLE FUNCTION}}$ is a 0, and the J/K is set, a function pulse (FCTN PULSE) enables setting the reserved flip-flop, sets the function flip-flop, and enables the load pulse (at C28). The function flip-flop remains set until cleared by a master clear, parity strobe, local autoload, or deadman terminate.

Following the pulse from TP5, a 150-nanosecond pulse from TP24 sets the J/K flip-flop at location 33. This generates a function signal which is sent through the coupler multiplexer to the processor to indicate that a function word is available.



FUNCTION TIMING CHAIN

AUTOLOAD (C30)

The autoload flip-flop sets when an autoload function code (0414_8) is processed or when the autoload switch is pressed to start a local autoload. (Local autoload may not be a part of the system.)

When this flip-flop sets, all other operations are terminated, the appropriate data path is selected, and the coupler sends the necessary signals to the processor station control interface.

MASTER CLEAR

A 6000 master clear is sent to the coupler only during PPU deadstart. This clears the coupler.

Halt decode causes a halt to be sent to the control logic. Halt decode comes from a master clear or a deadman terminate.

INACTIVE

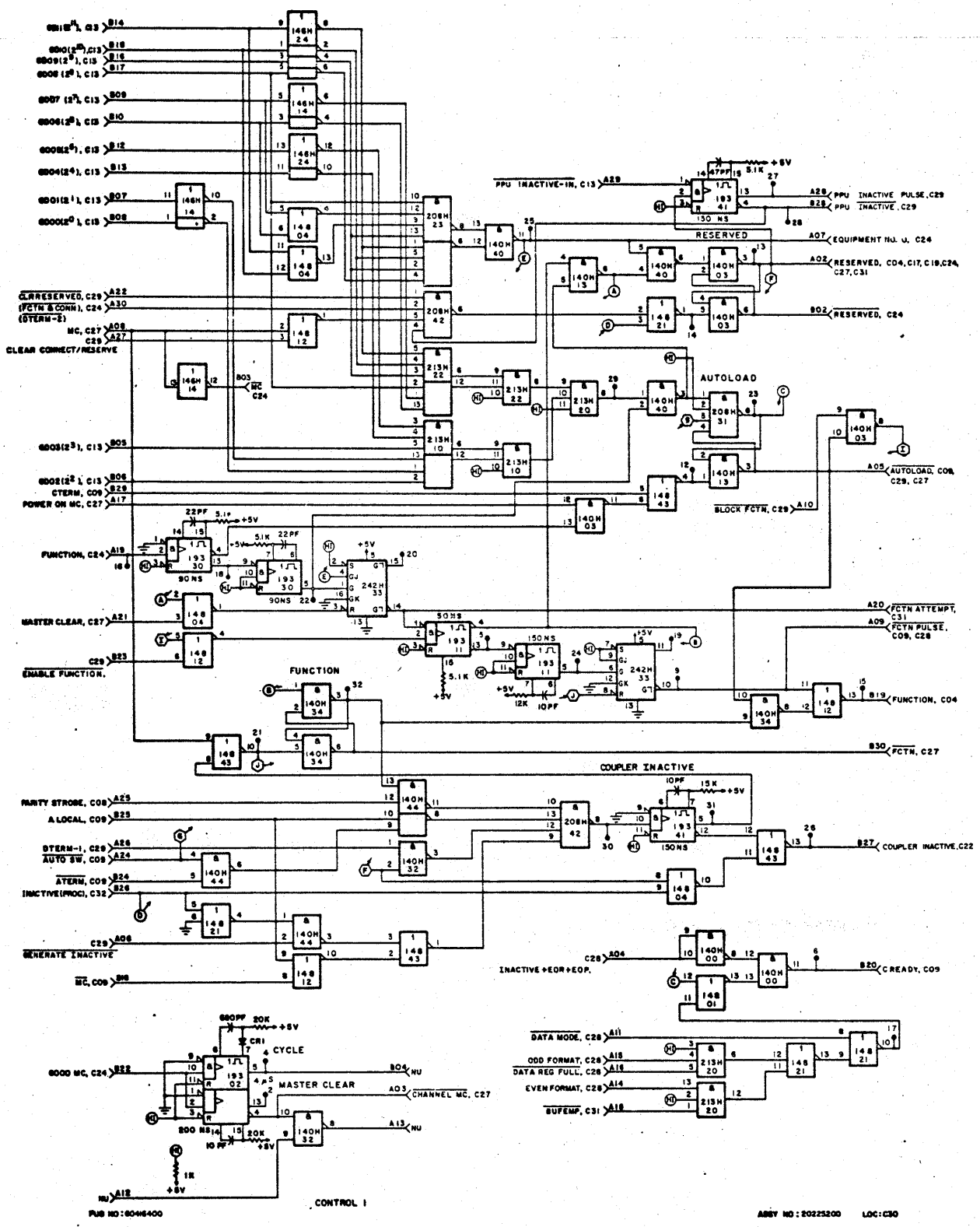
The one-shot at location 41 (TP 31) generates a 150-nanosecond pulse when a parity strobe is responding to a function code (function flip-flop set), an autoload is initiated, deadman terminate times out, the processor inactivates the coupler, or data mode clears in the coupler.

COUPLER READY (CREADY)

Coupler ready is sent to the processor when the autoload flip-flop sets, when a PPU sends an inactive signal, when the control logic sends an EOR-IN, or when the processor sends an EOP.

The coupler will also generate CREADY during a data transfer when the coupler is in da mode and the coupler can accept data during a read (odd format and $\overline{\text{data reg full}}$), or th coupler has a data byte available during a write (even format and $\overline{\text{bufemp}}$).

D.H.O. - 83


PPU INACTIVE-IN, C13
PPU INACTIVE PULSE, C29
PPU INACTIVE, C29
RESERVED
EQUIPMENT NO. U, C24
RESERVED, C04, C17, C19, C24, C27, C31
RESERVED, C24
AUTOLOAD
AUTOLOAD, C08, C29, C27
BLOCK FCTN, C29
CLR RESERVED, C29
(FCTN & CONN), C24
(STERM-2)
MC, C27
C28
CLEAR CONNECT/RESERVE
MC C24
POWER ON MC, C27
CTERM, C09
FUNCTION, C24
MASTER CLEAR, C27
C29
ENABLE FUNCTION.
FUNCTION
FCTN ATTEMPT, C31
FCTN PULSE, C09, C28
FUNCTION, C04
FCTN, C27
COUPLER INACTIVE
COUPLER INACTIVE, C22
PARITY STROBE, C09
A LOCAL, C09
STERM-1, C29
AUTO SW, C09
ATERM, C09
INACTIVE (PROC), C32
GENERATE INACTIVE
MC, C09
INACTIVE + EOR + EOP.
C READY, C09
DATA MODE, C28
ODD FORMAT, C28
DATA REG FULL, C28
EVEN FORMAT, C28
BUFEMP, C31
CYCLE
MASTER CLEAR
CHANNEL MC, C27
CONTROL I
PUB NO: 60416400
ASSY NO: 20225200
LOC: C30

B21

D. H. O. -24

CONTROL 2 (C31)

TIMING CHAIN

The timing chain provides timing pulses during a transfer from the PPU to the processor or control logic. The chain is enabled by data mode and starts when the processor sends a parity strobe or the control logic sends a CIRPLY. The chain enables clearing of the data register, decrementing of the frame counter, and outputting the next word.

CLEAR 2

The 50-nanosecond pulse from TP 11 clears the data register full flip-flop (C28). This occurs when the coupler generates a full signal (C29) which is sent to the PPU during a read.

EMPTY

The 150-nanosecond pulse from TP29 toggles the LD upper/LD lower flip-flop (C28), enables clearing data register full, and is sent through the channel adapter to the PPU. The pulse is sent during a PPU write operation when the data register is empty and the PPU sends a full and a data byte to the coupler.

DATA READY

The data ready flip-flop sets only during PPU write operations (format 0, 2, 4, 6, or 8). When set, the flip-flop indicates that the data register contains data which is ready to be transferred to the processor or control logic.

The data ready flip-flop is set by one of the following conditions:

1. (Register full) (Format 0 + format 6)
2. (Format 2 + 4 + 8) (Lower full · frame count 1 + 3 + 4 + 7)
3. (Format 2 + 4 + 8) (Upper full · frame count 2 + 5 + 6)
4. (Function + $\overline{\text{active}}$) (Write) (Data mode) (Upper full and lower full)

Ordinarily, the flip-flop is cleared by a pulse from the timing chain (TP 16). The flip-flop may also be cleared by the STOP READ signal which goes to a 1 if data mode clears, or when the processor deactivates the coupler, the coupler receives a master clear or the PPU deactivates the coupler.

D,4-0,-25

INHIBIT OUTPUT

The inhibit output latch sets when the coupler is in data mode and CKPAR2 goes to a 1. This indicates that the processor has returned a parity strobe signal or the control logic has returned a CIRPLY during a PPU write operation. When TP 20 goes to a 1, the coupler reply timing chain (C09) is disabled. This prevents the transfer of another word to the processor or control logic until data ready is set and inhibit output is clear.

FULL ENABLE

A 1 at TP30 provides one of the enables which allows the coupler to send a full signal to the PPU during a read operation (odd format). One of the following conditions causes TP 30 to go to a 1.

1. [Lower full] [(Format 1) + (Format 5) + (Format 3 · FC3) (Format 9 · FC 3+5+6+8+9)]
2. [Upper full] [(Format 1) + (Format 5) + (Format 7) + (Format 3 · FC1+2+4+7+10) + (Format 9 · FC1+2+4+7+10)]
3. (Odd format) (Data mode) (Upper full + lower full) (Inactive + EOR + EOP)

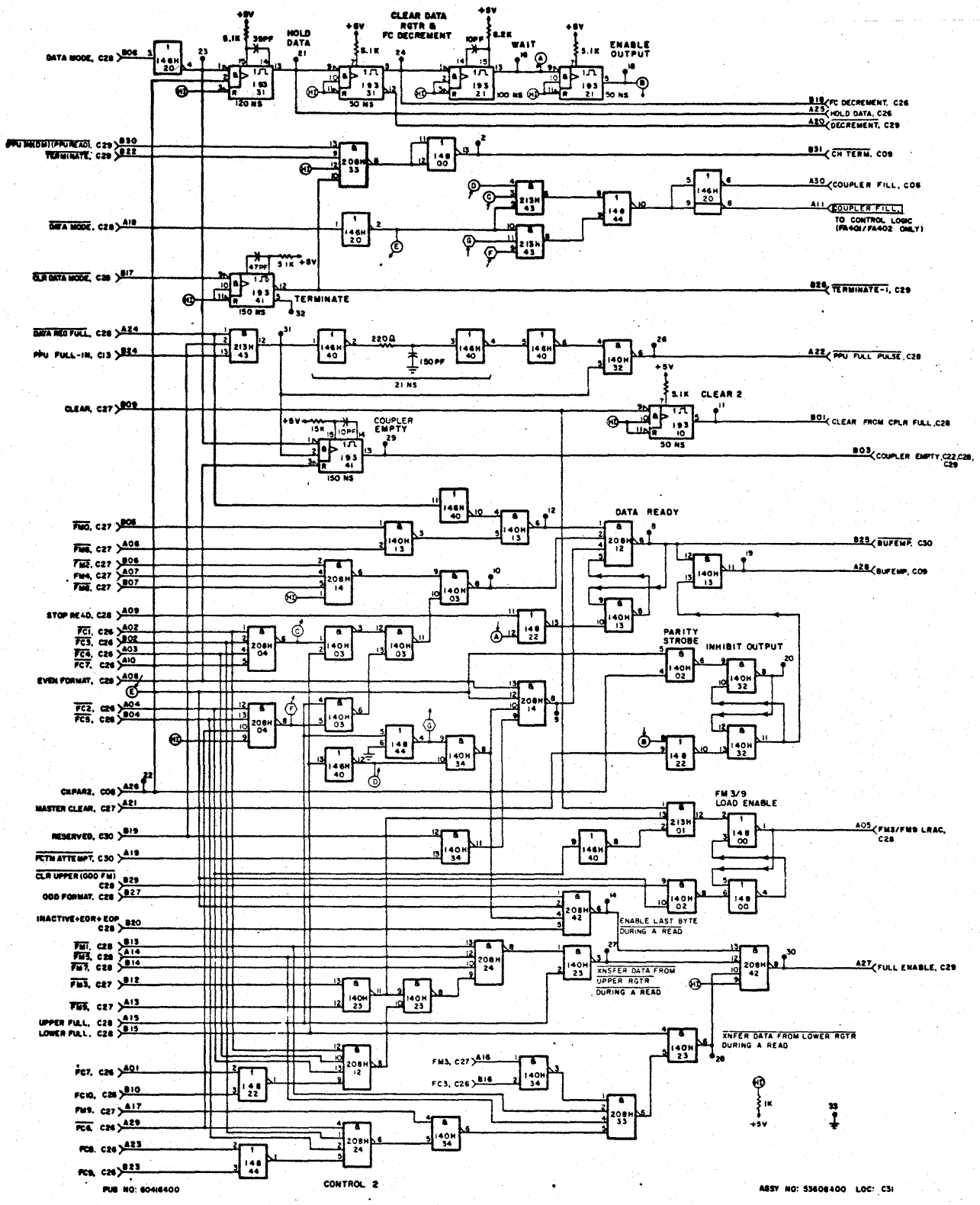
The last condition empties the data register when inactive, EOR, or EOP has stopped the read.

FM 3/9

This flip-flop sets when format 3 or 9 is selected, the frame count is 2, and a clear is generated at C27. (The clear at C27 is generated when the coupler generates a full pulse during a read, Coupler Full, C29). A 0 from connector pin A05 clears the LD UP/LD LWR flip-flop at C28 to allow the byte from the processor or control logic to be loaded into the upper part of the data register. This is necessary to allow for the register loading pattern used by formats 3 and 9.

NOTE

Signal names enclosed in a rectangle XXX-XX are interchassis signals.

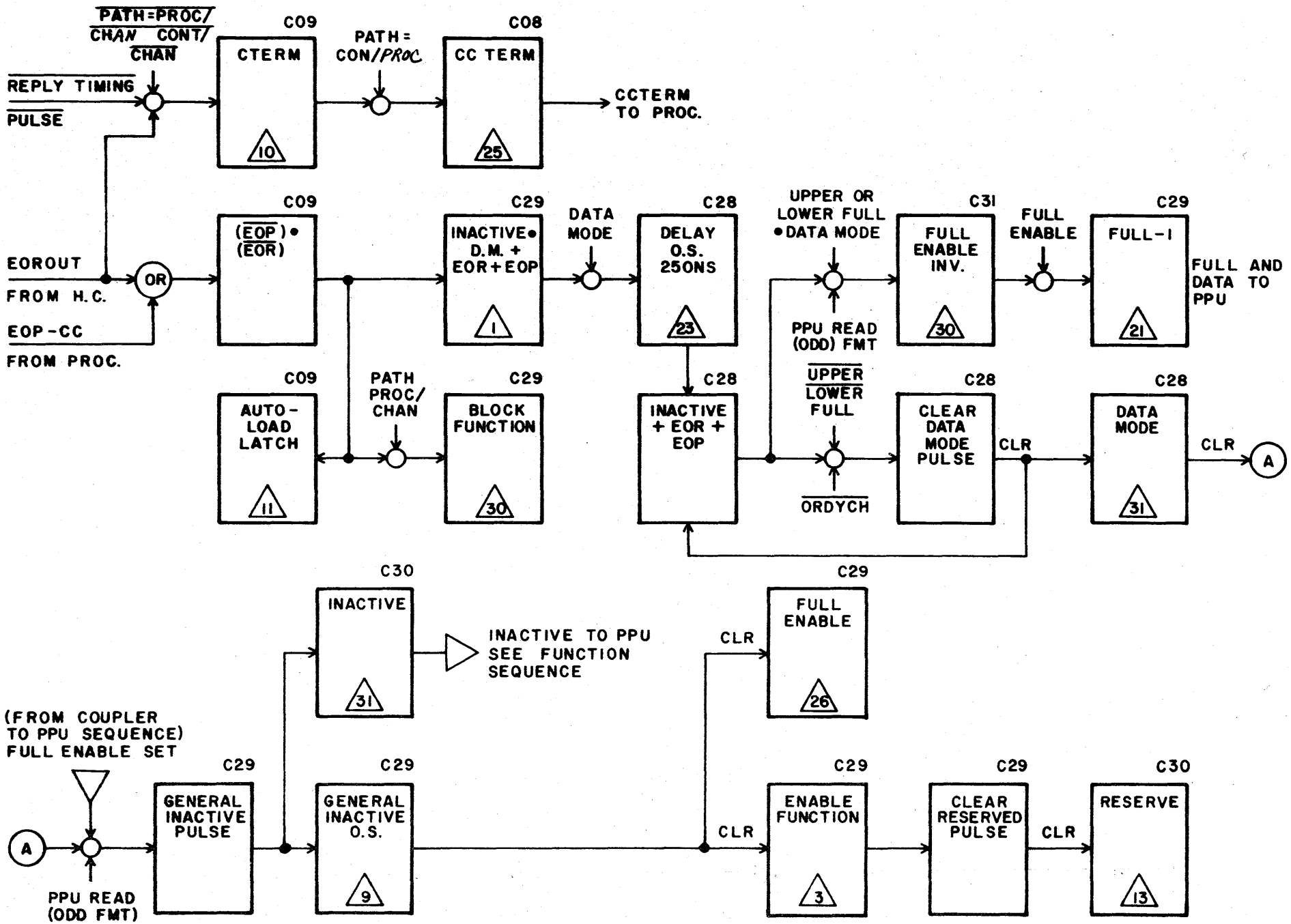

CLEAR DATA
RGTR &
FC DECREMENT
HOLD DATA
WAIT
ENABLE OUTPUT
DATA MODE, C28
TERMINATE, C29
DATA MODE, C28
CLR DATA MODE, C28
TERMINATE
DATA REQ FULL, C26
PPU FULL-IN, C13
CLEAR, C27
COUPLER EMPTY
DATA READY
STOP READ, C28
EVEN FORMAT, C28
PARITY STROBE
INHIBIT OUTPUT
CLPAR2, C06
MASTER CLEAR, C27
RESERVED, C30
FCTN ATTEMPT, C30
ODD FORMAT, C28
FM3/9 LOAD ENABLE
ENABLE LAST BYTE DURING A READ
XNSFER DATA FROM UPPER RGTR DURING A READ
XNFER DATA FROM LOWER RGTR DURING A READ
UPPER FULL, C28
LOWER FULL, C28
CONTROL 2
PUB NO: 60416400
ASSY NO: 53608400 LOC: C51

B27

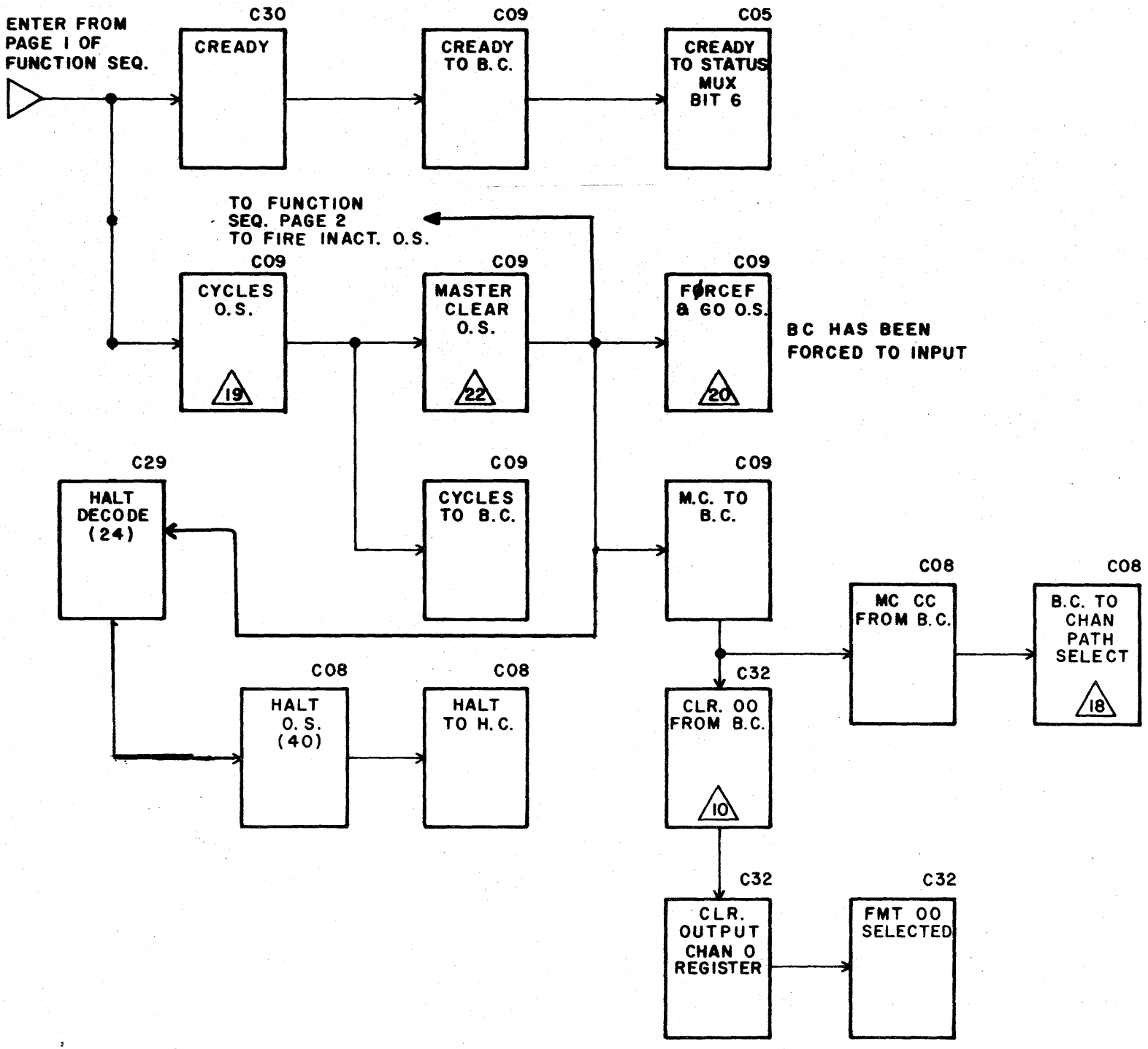
D.H.O.-26

6000 COUPLER
STUDENT HANDOUTS

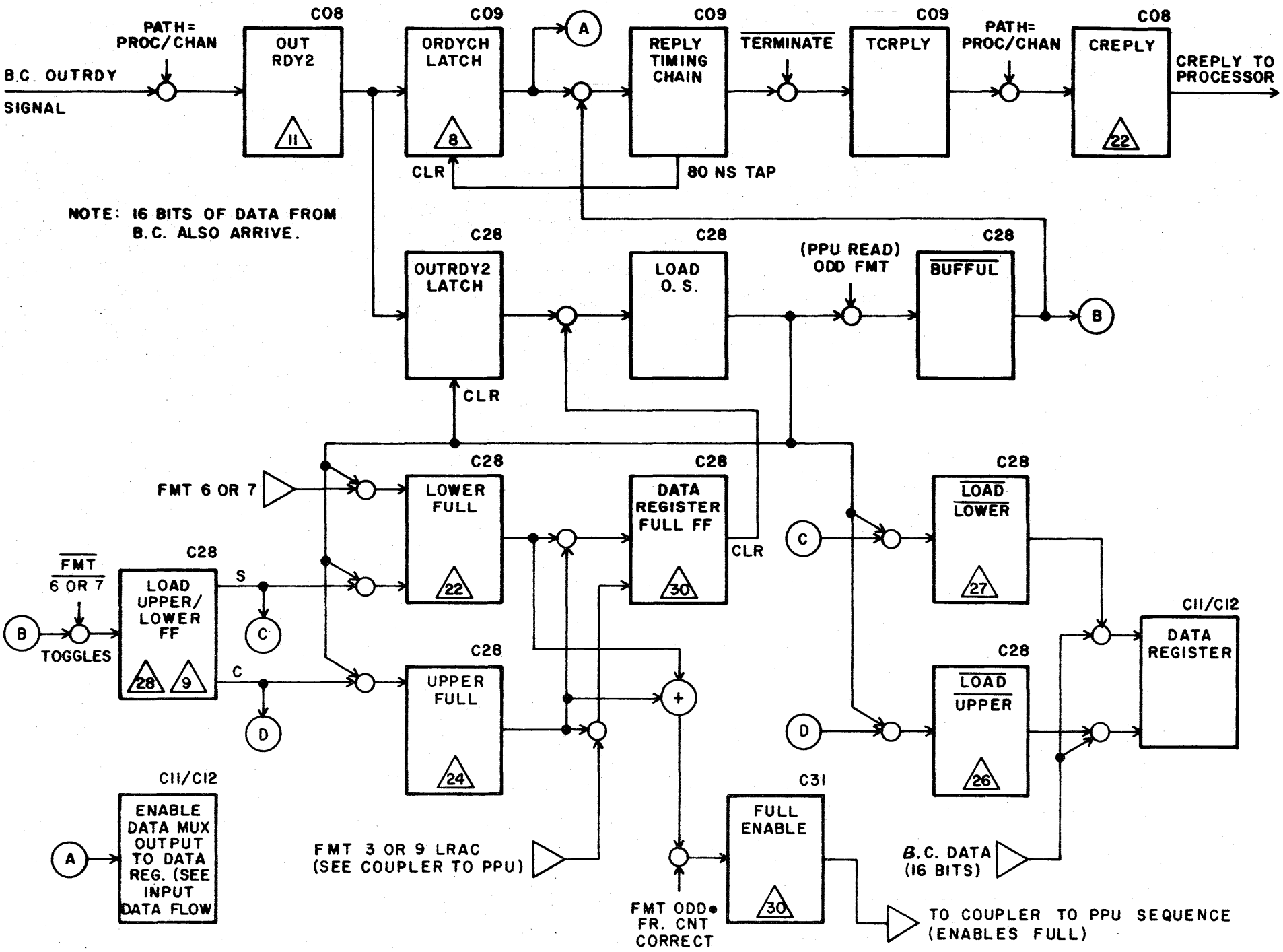
TERMINATE (PROC. EOP•CC OR H.C. EOROUT)



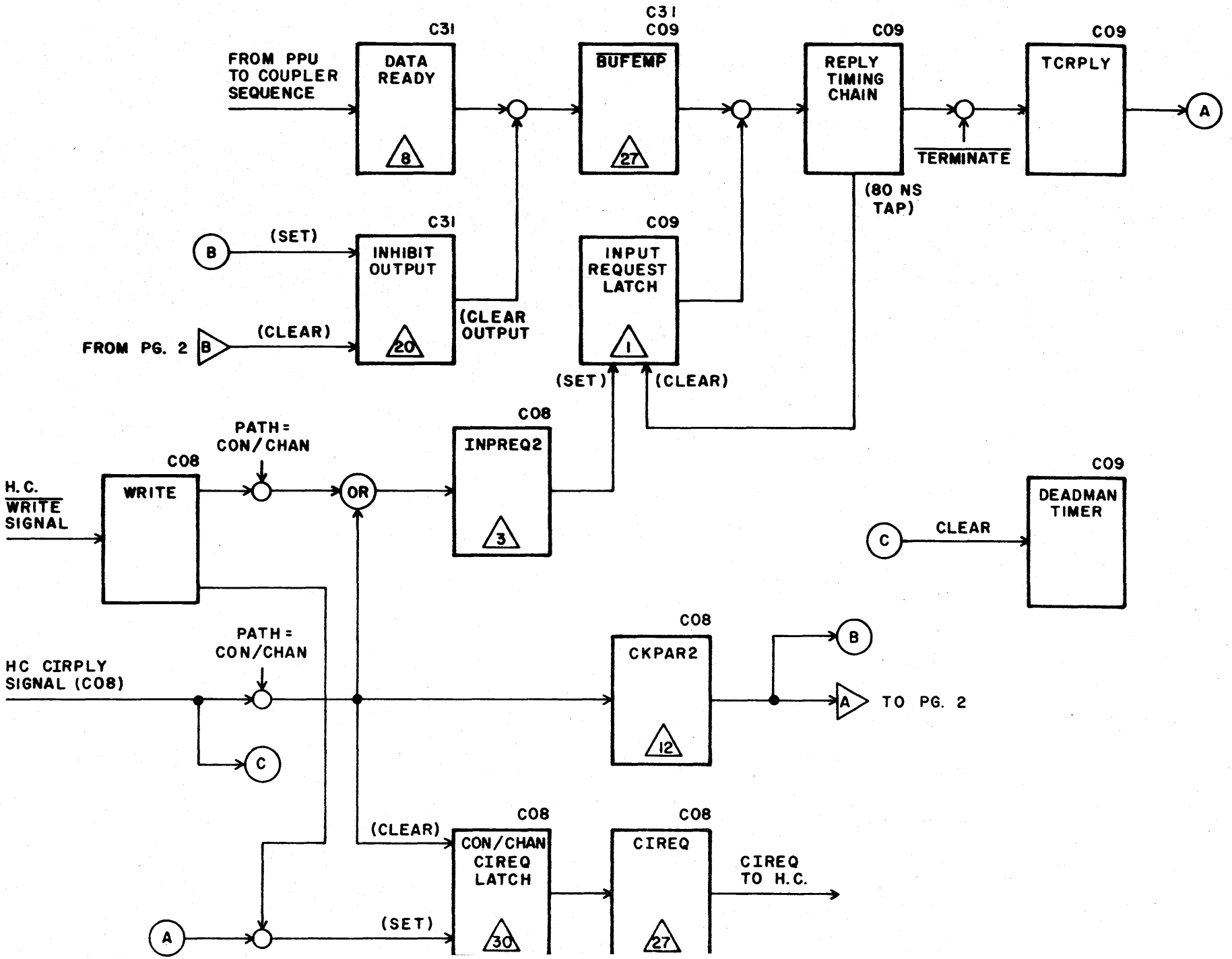
AUTOLOAD FUNCTION (0414_8)



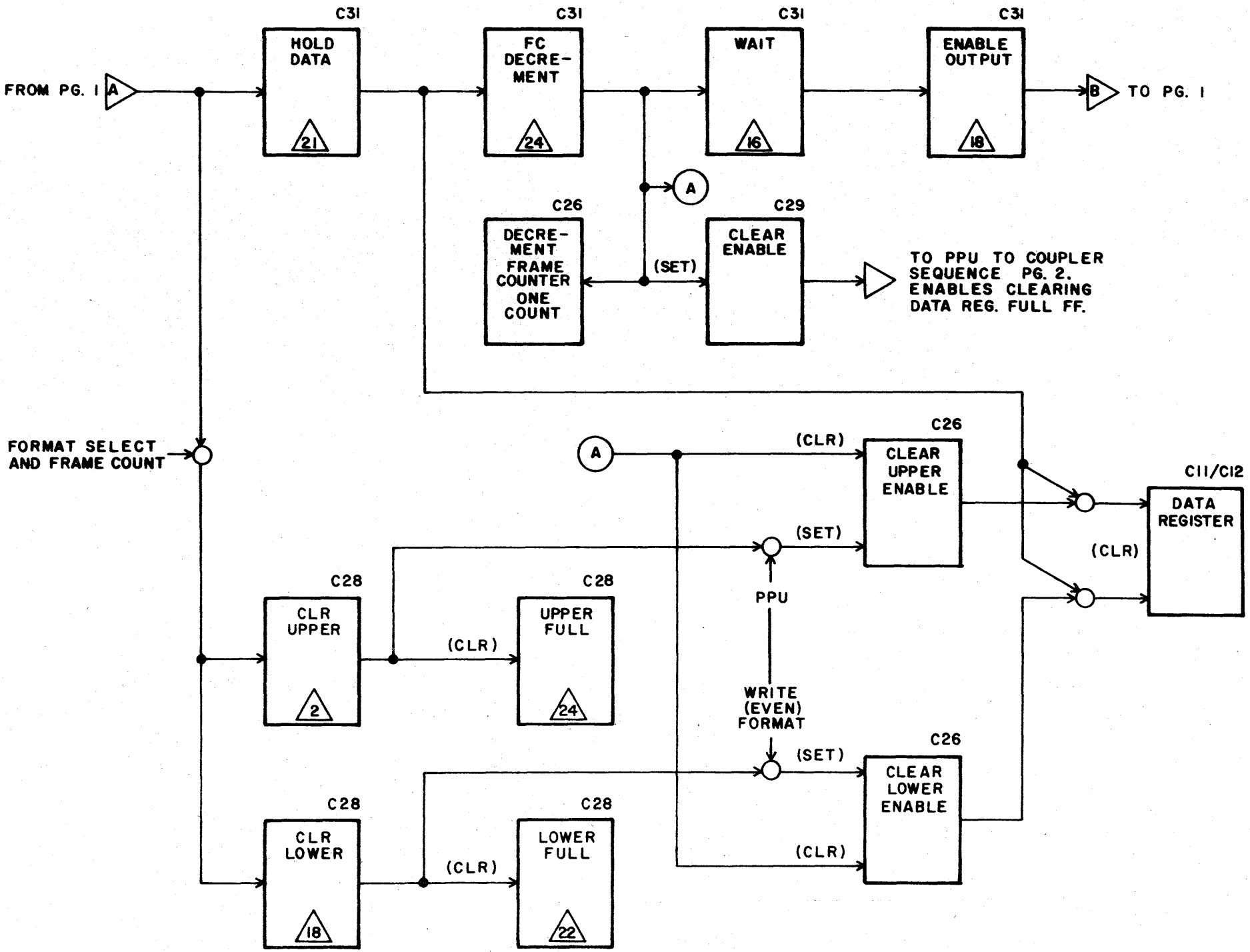
PROCESSOR TO COUPLER



COUPLER TO CONTROLLER PAGE 1 OF 2

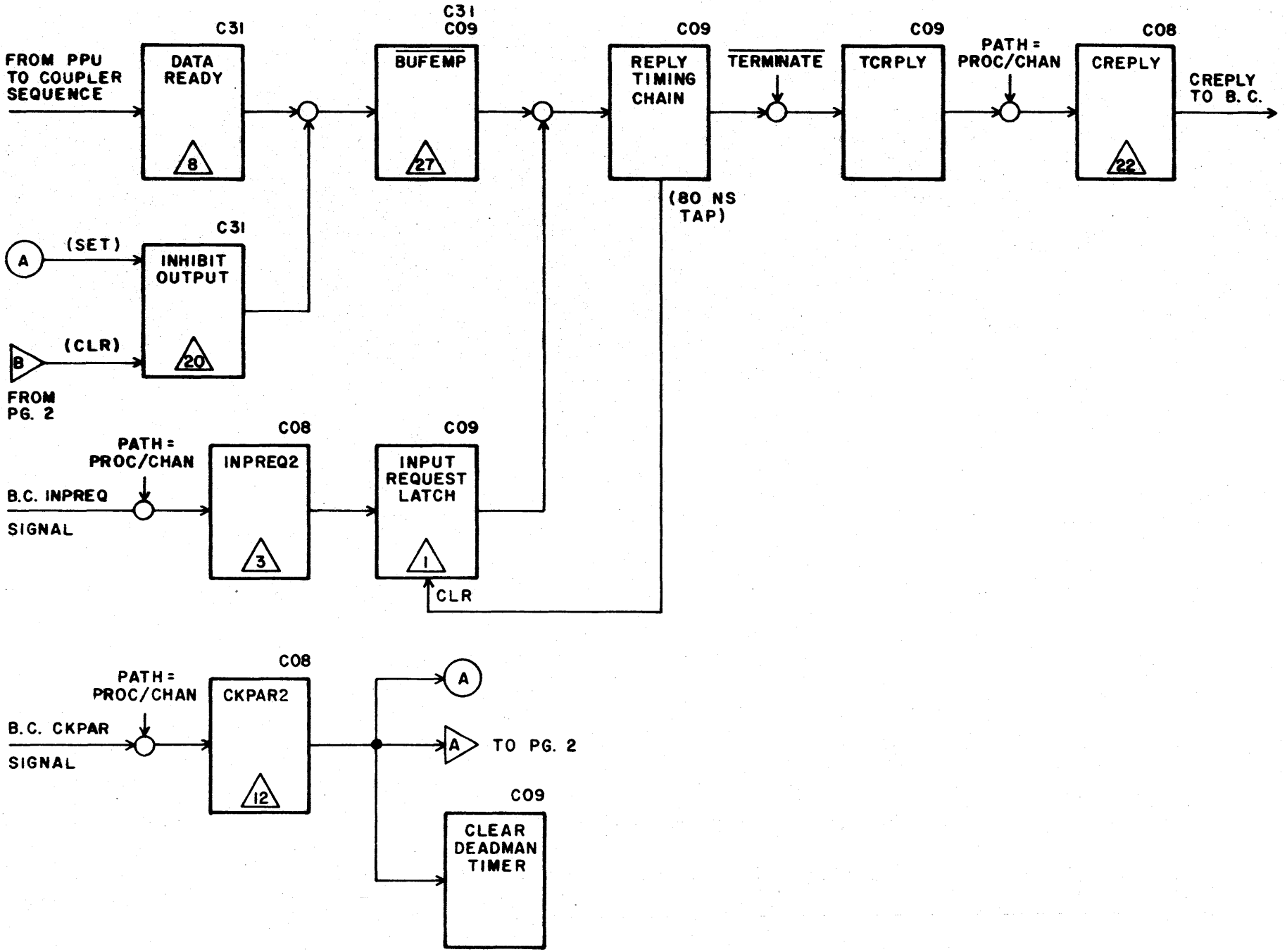


COUPLER TO CONTROLLER PAGE 2 OF 2

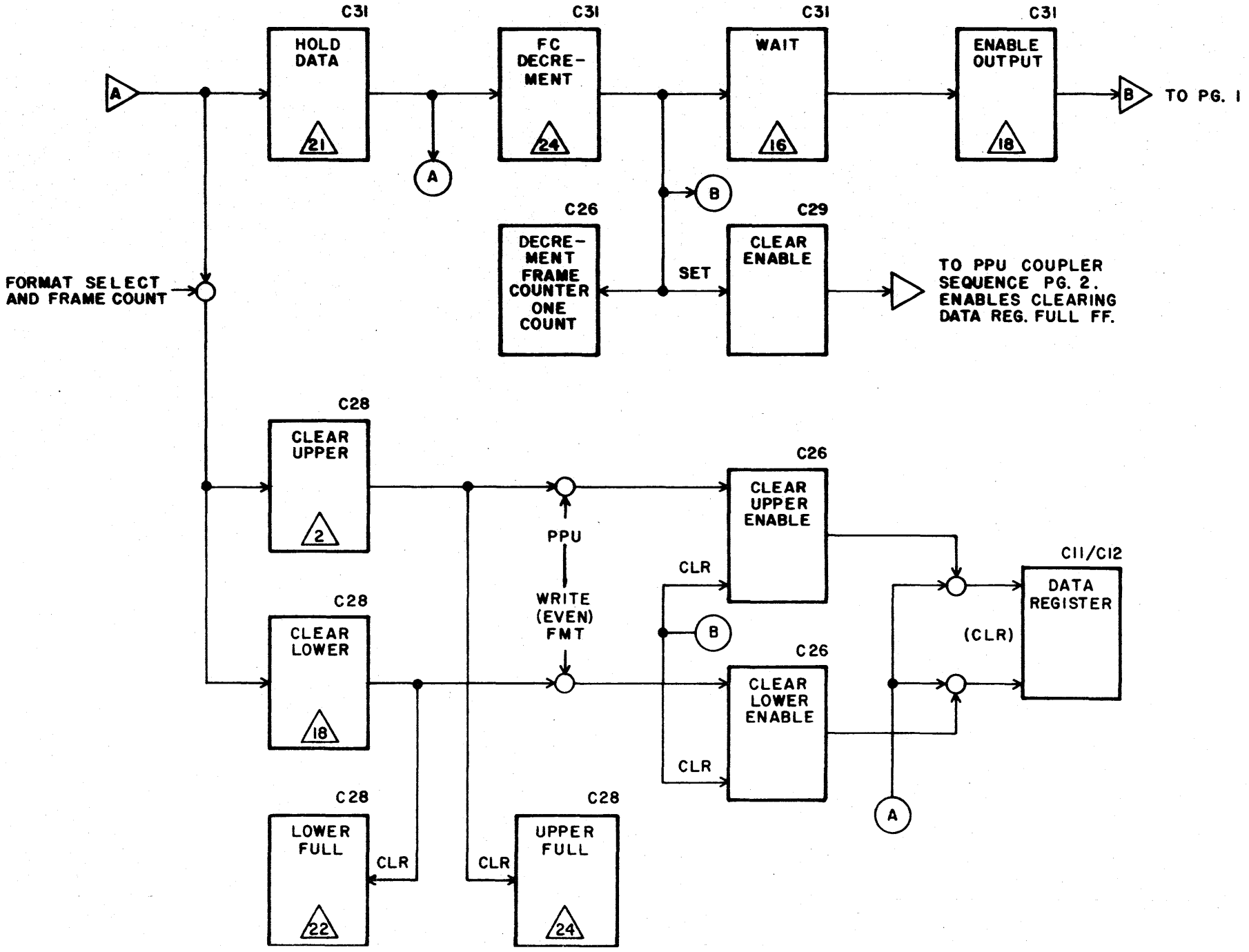


COUPLER TO B.C.

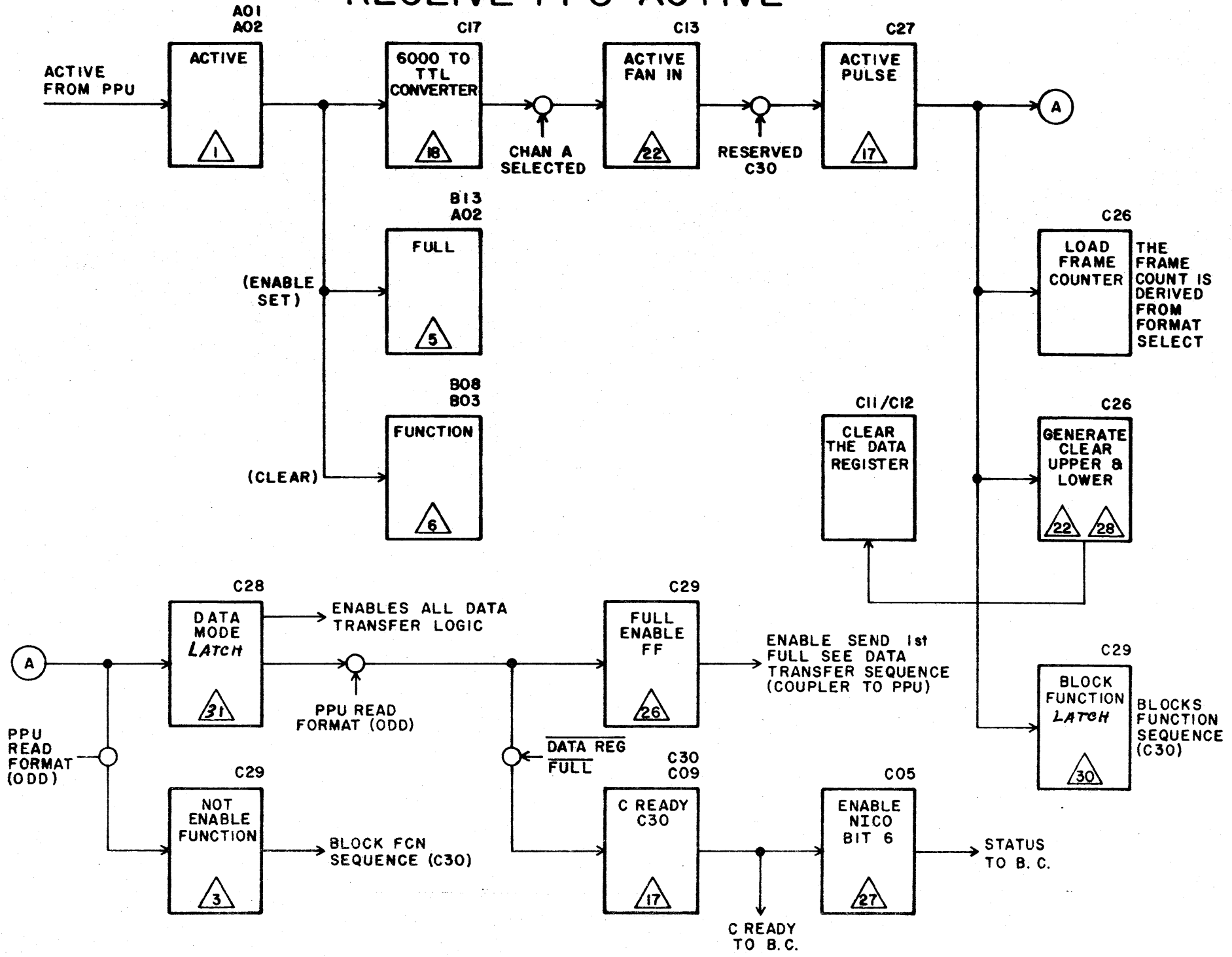
PAGE 1 OF 2



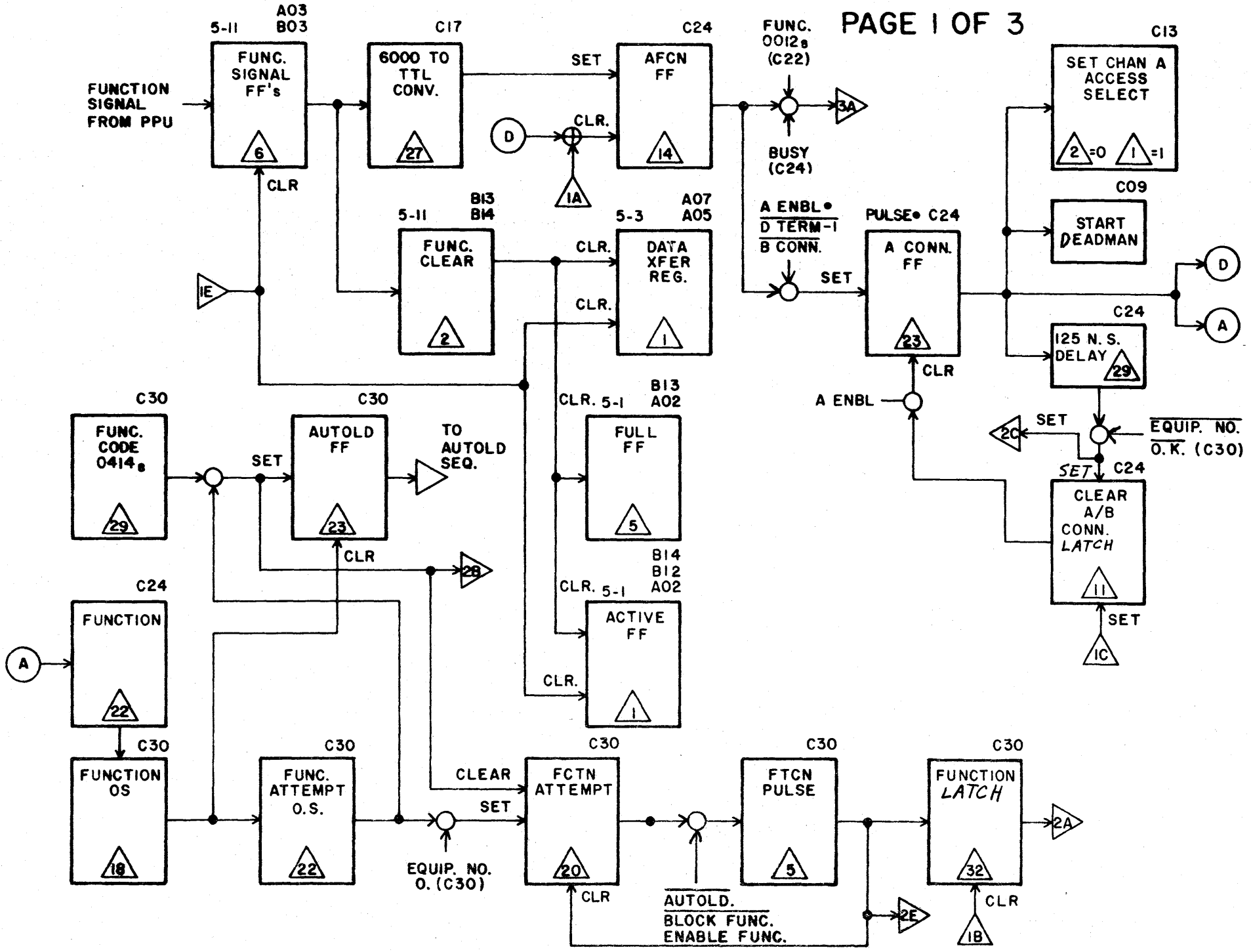
COUPLER TO B.C.
PAGE 2 OF 2



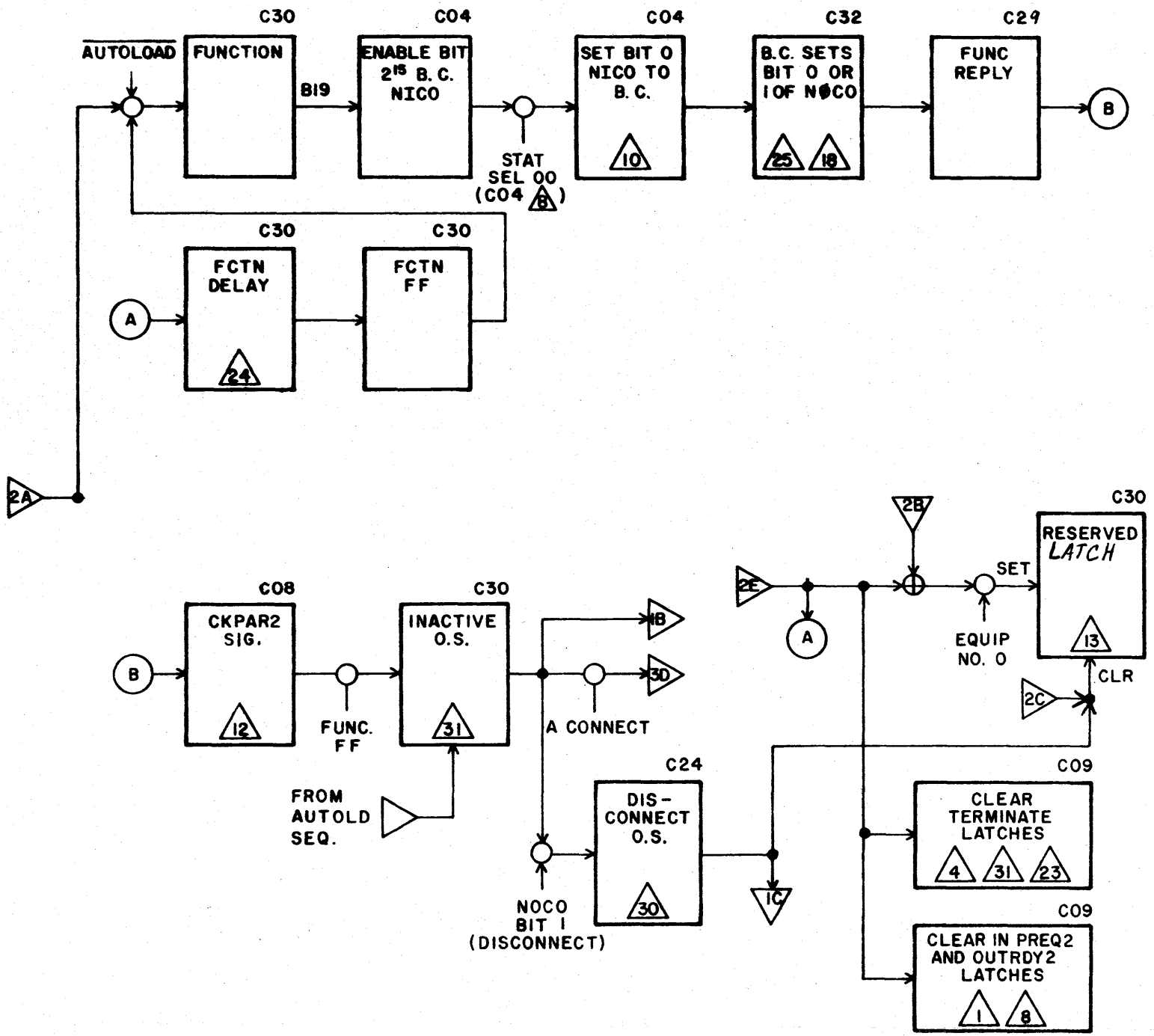
RECEIVE PPU ACTIVE



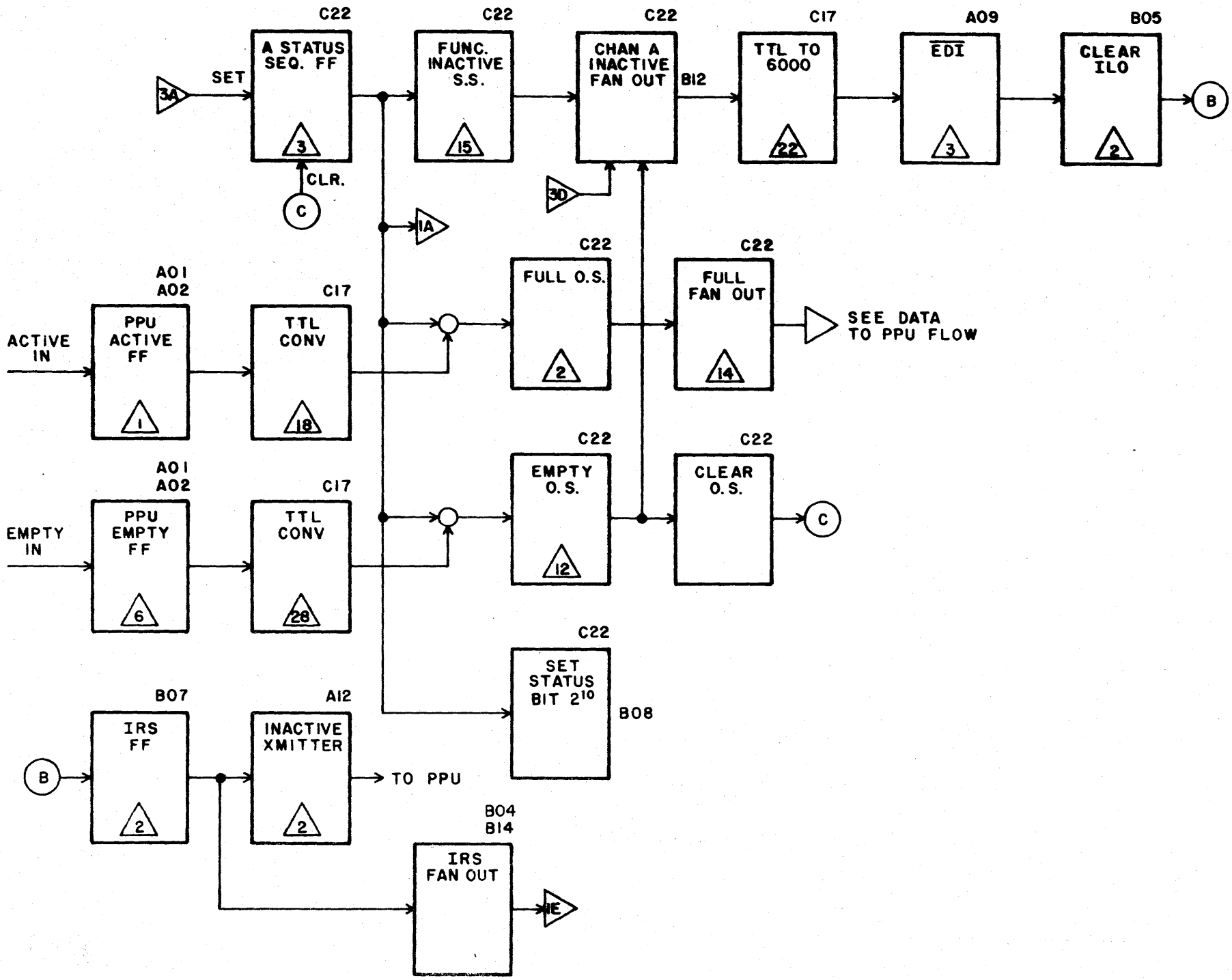
FUNCTION SEQUENCE (INCLUDING CONNECT)



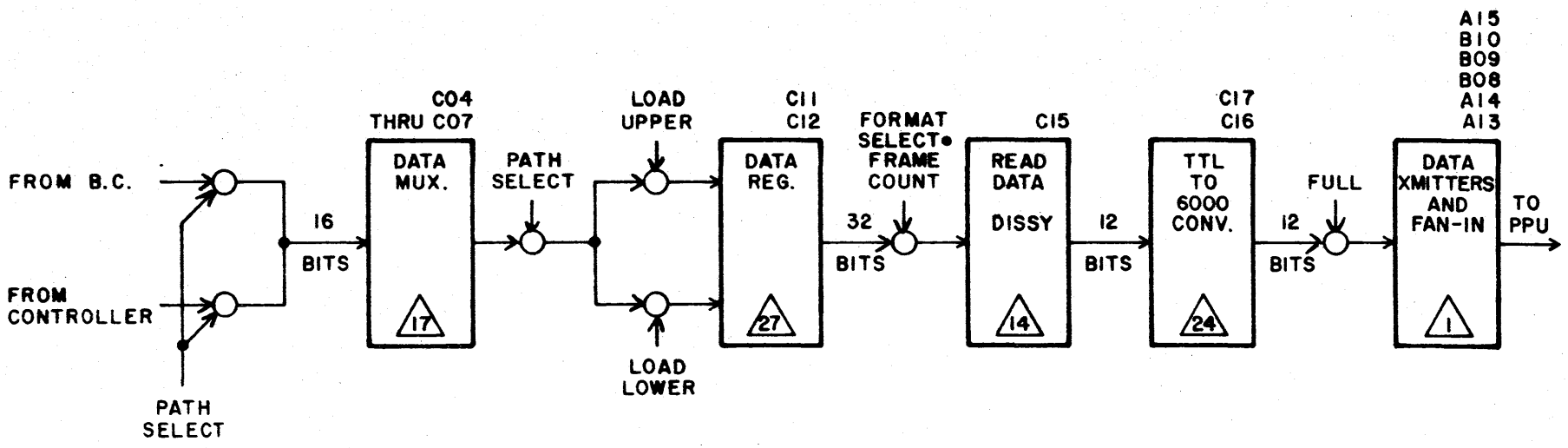
FUNCTION SEQUENCE



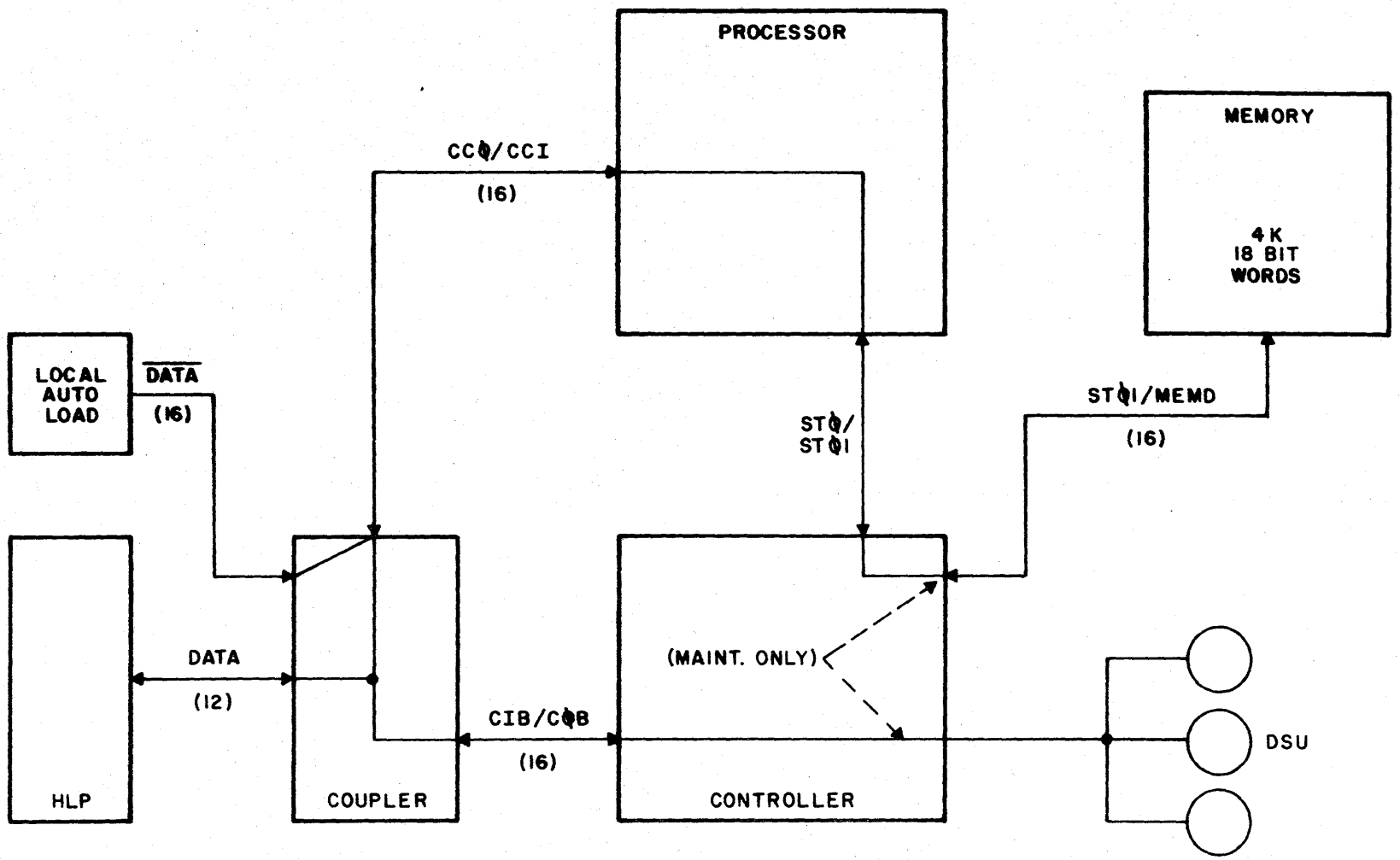
FUNCTION SEQUENCE



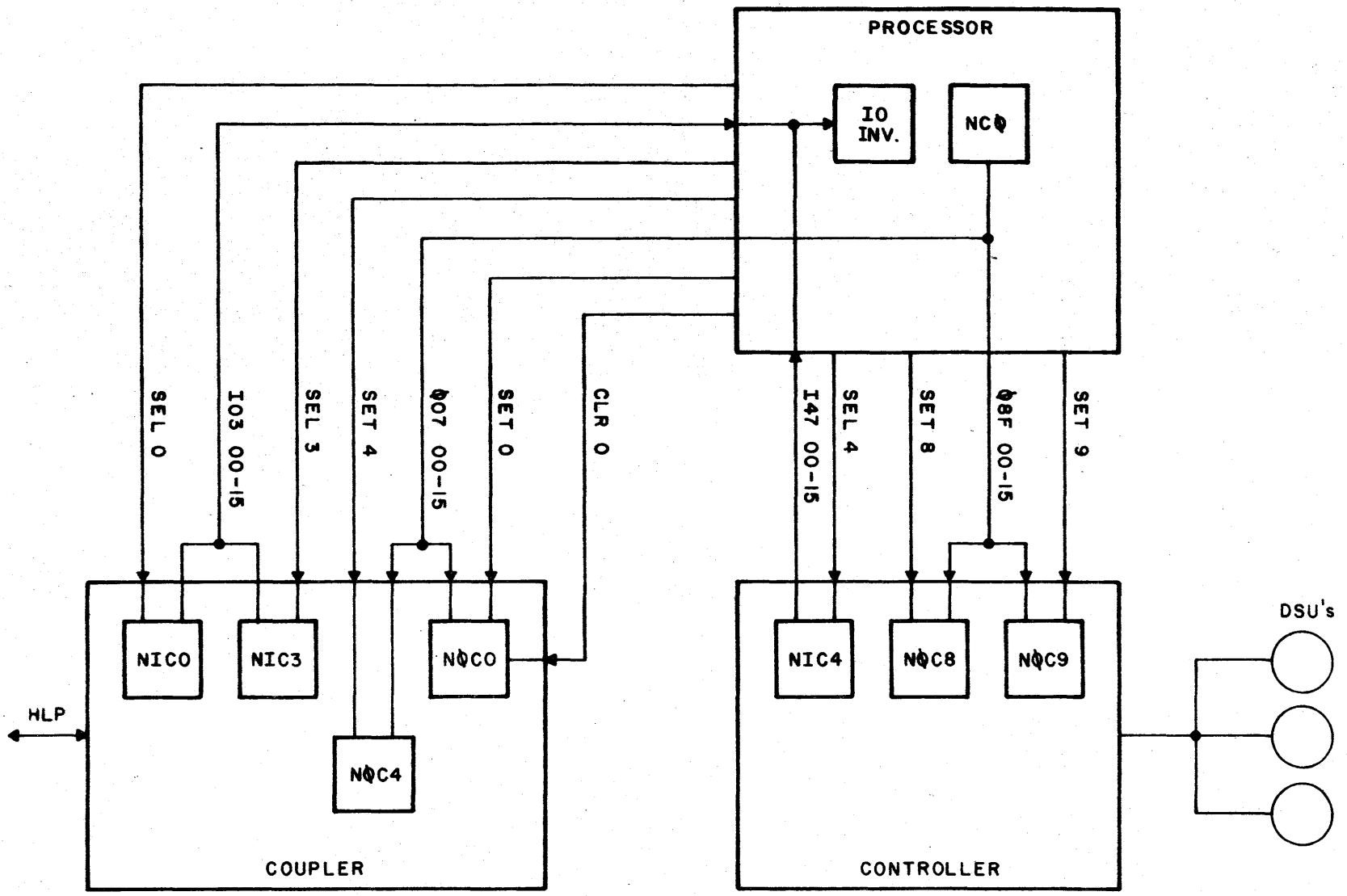
INPUT TO PPU DATA PATH



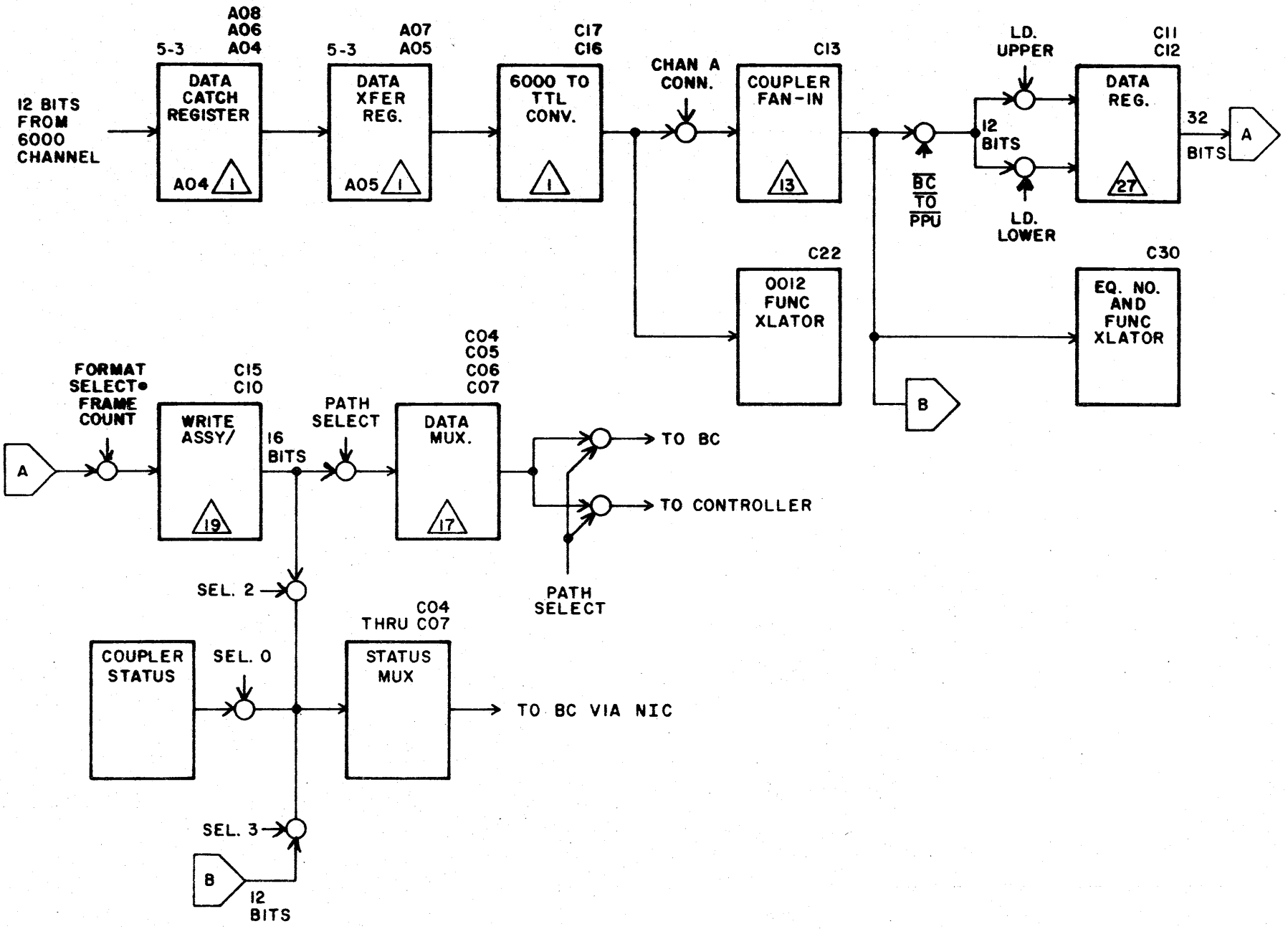
844 SYSTEM DATA PATHS



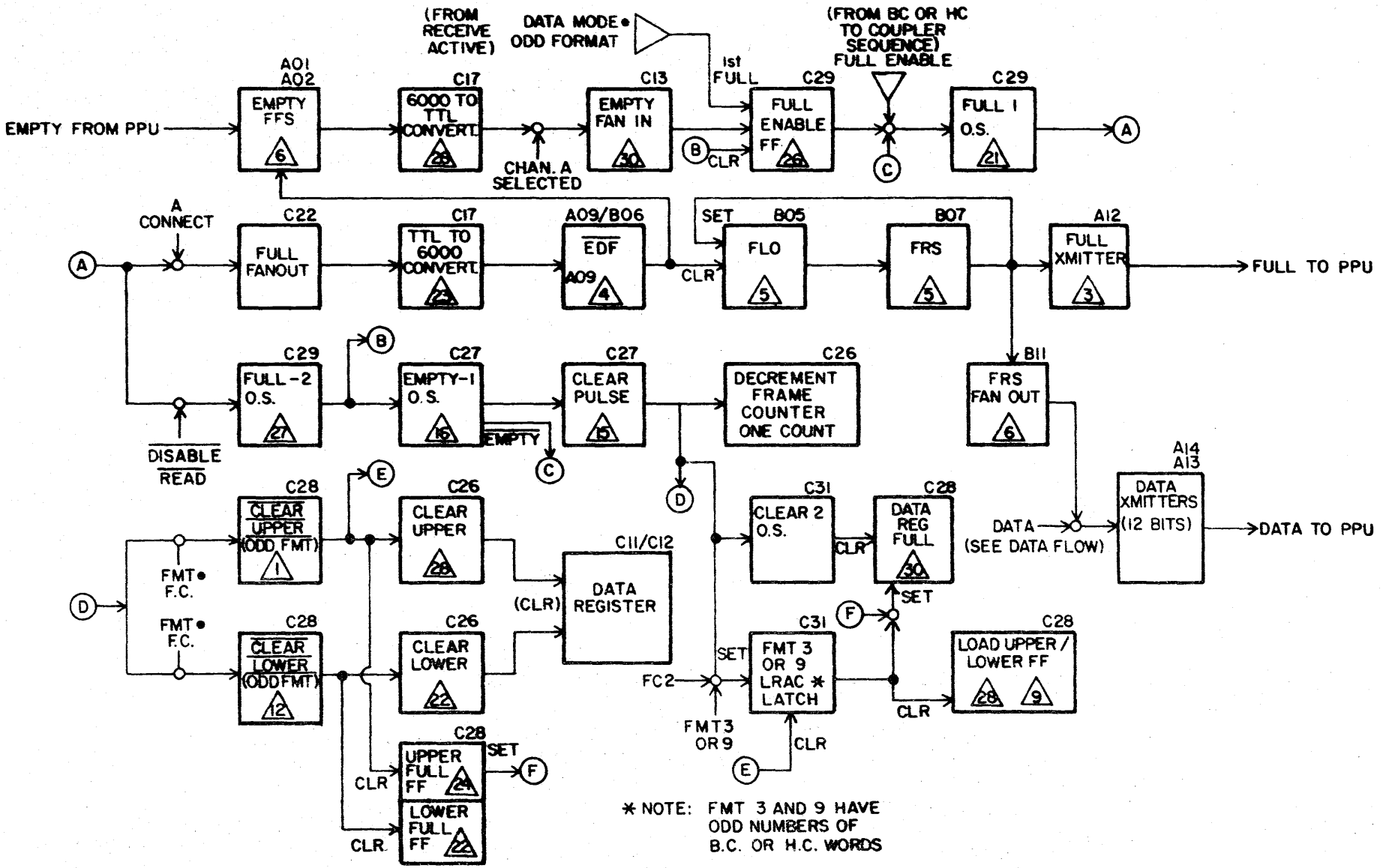
844 SYS NORMAL CHANNEL INTERFACE



OUTPUT FROM PPU DATA PATH

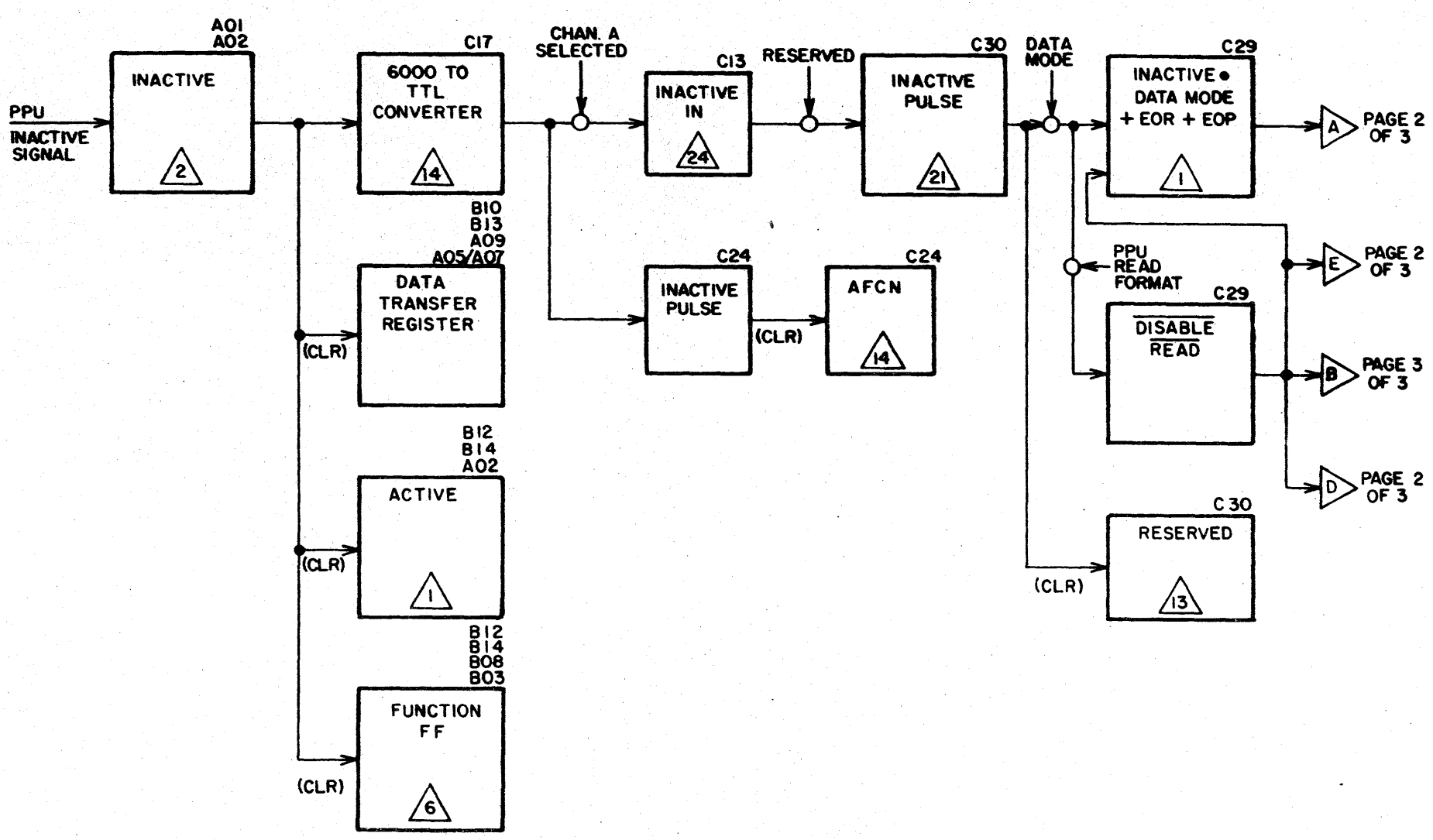


COUPLER TO PPU



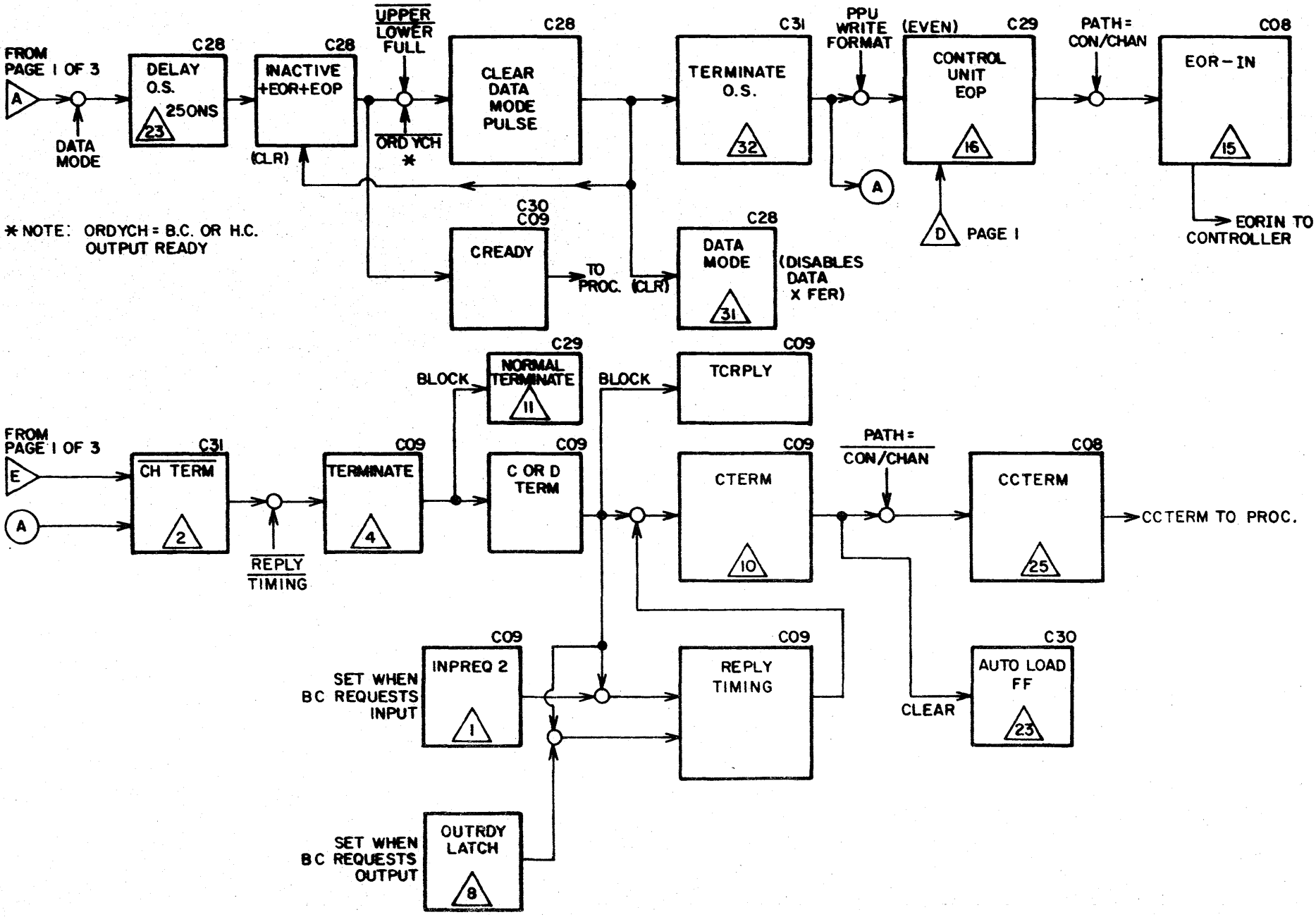
TERMINATE (PPU SENDS INACTIVE)

PAGE 1 OF 3



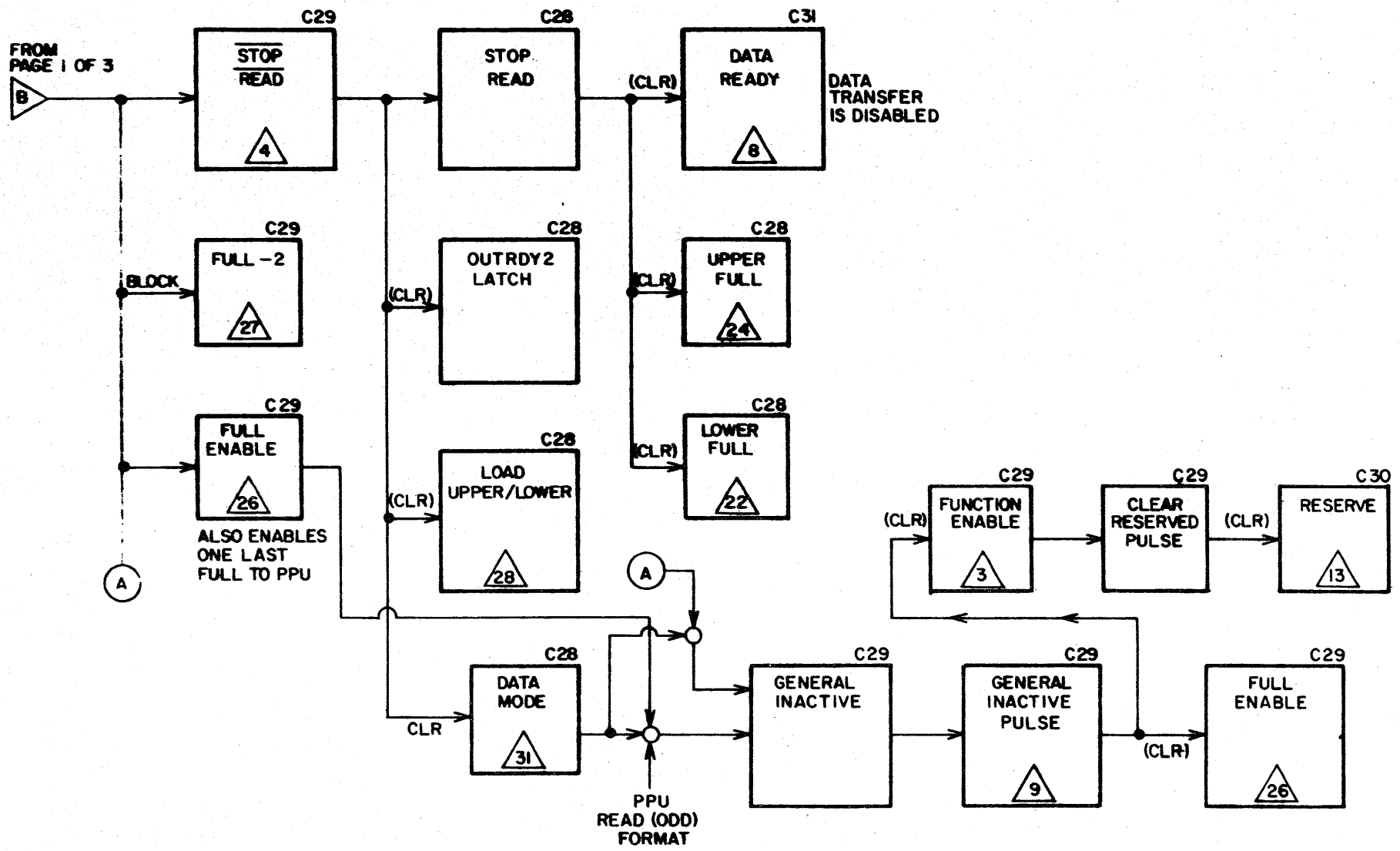
TERMINATE (PPU SENDS INACTIVE)

PAGE 2 OF 3

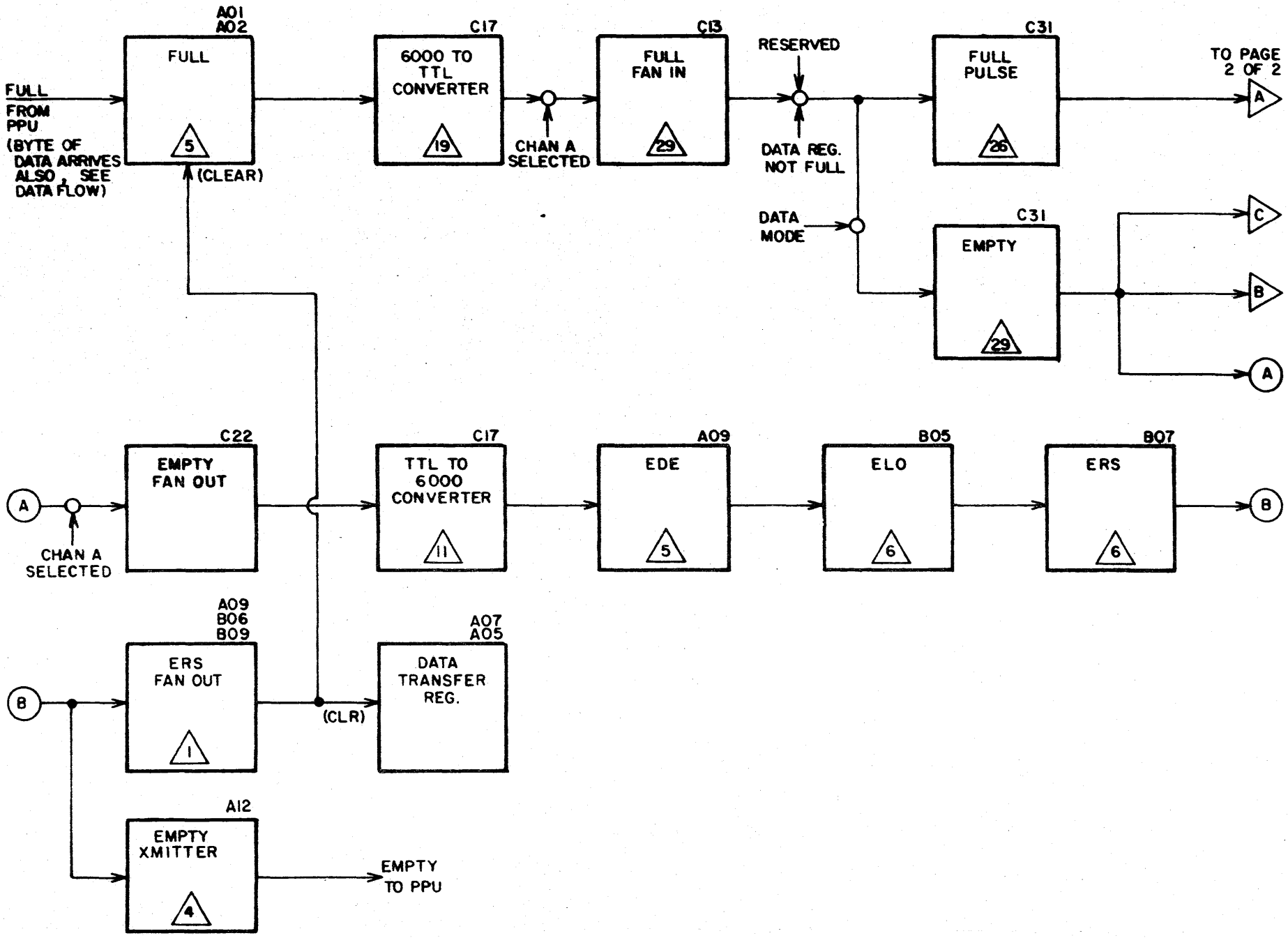


TERMINATE (PPU SENDS INACTIVE)

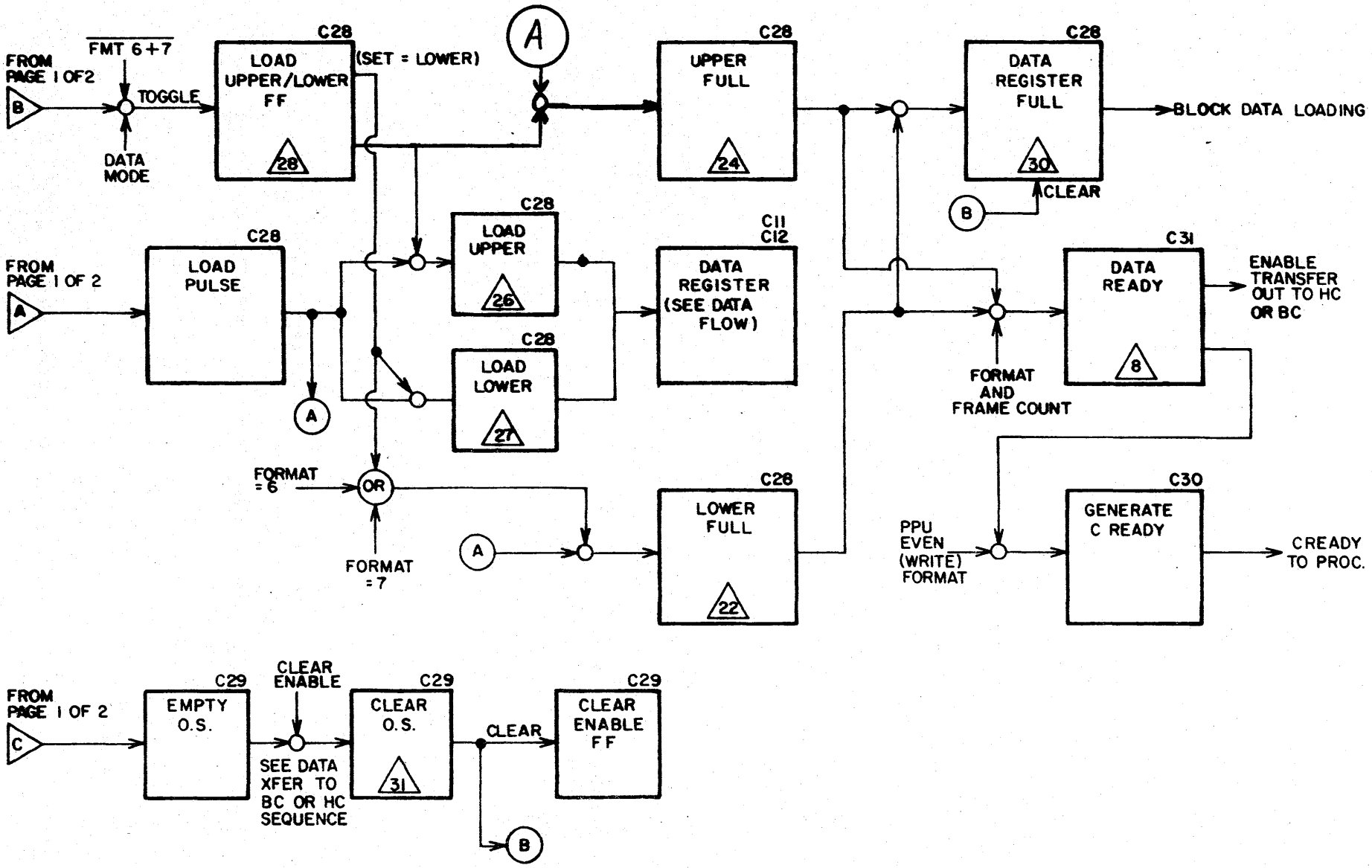
PAGE 3 OF 3



PPU TO COUPLER
PAGE 1 OF 2

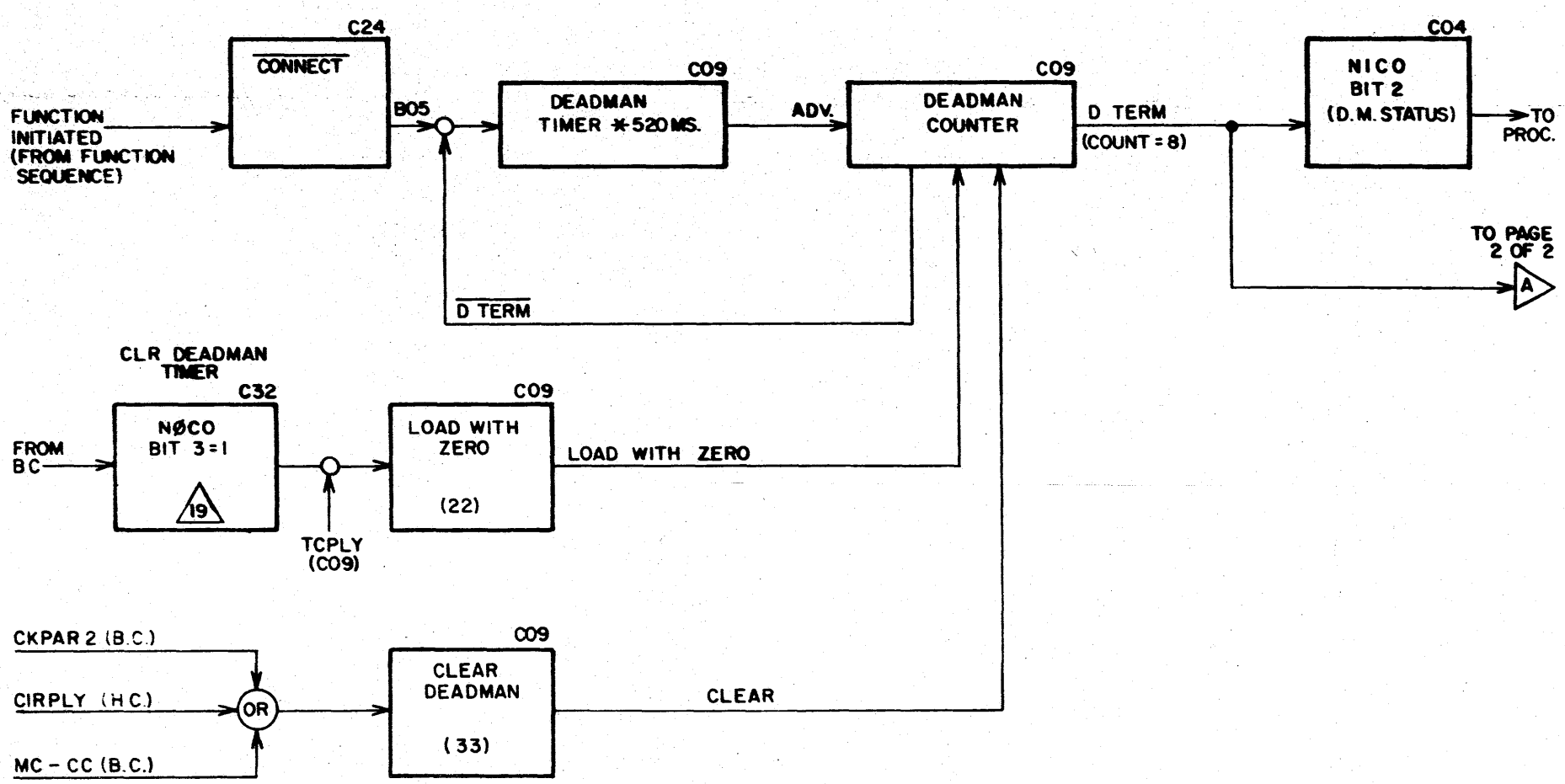


PPU TO COUPLER
PAGE 2 OF 2



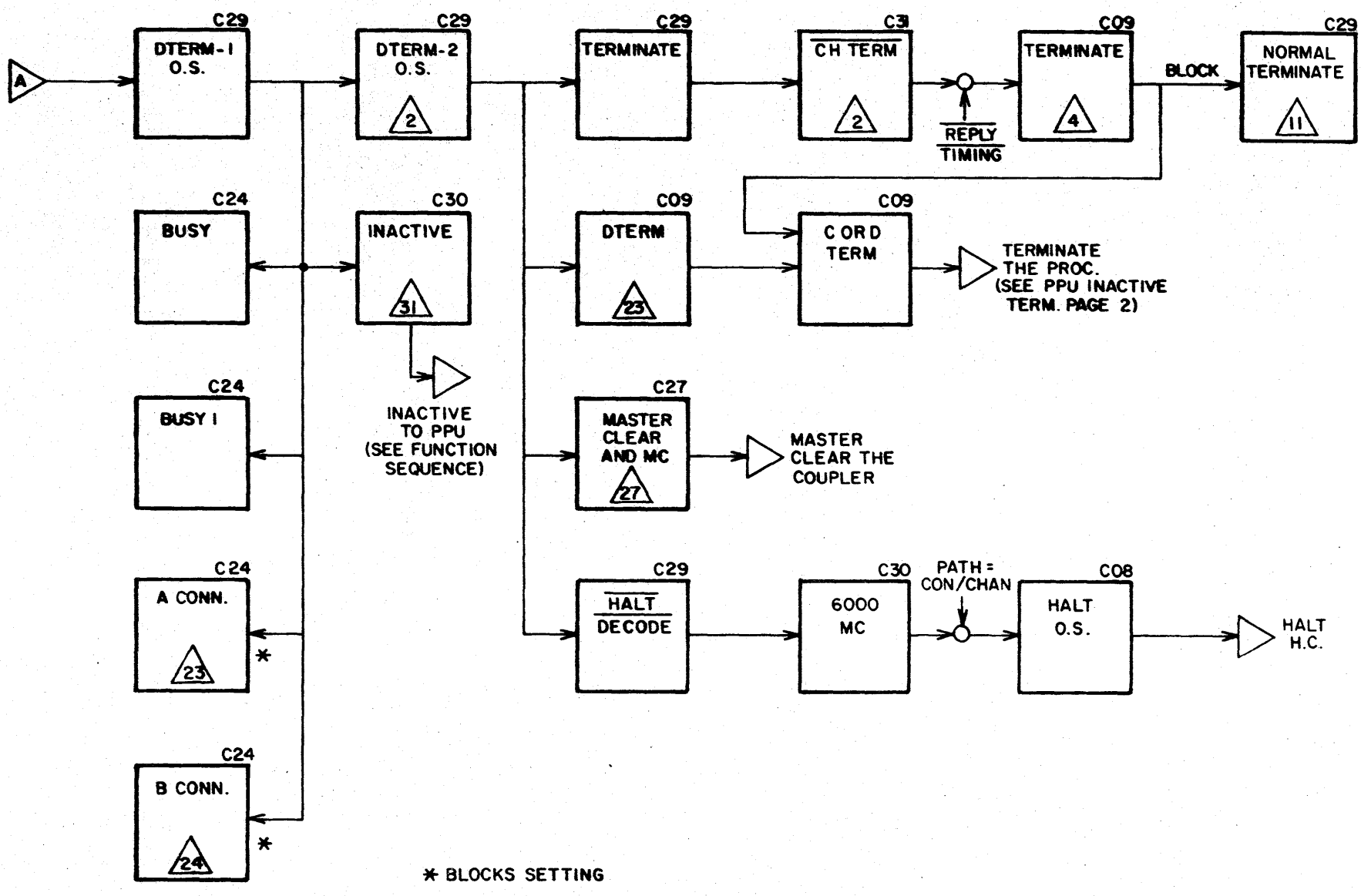
DEADMAN TERMINATE

PAGE 1 OF 2

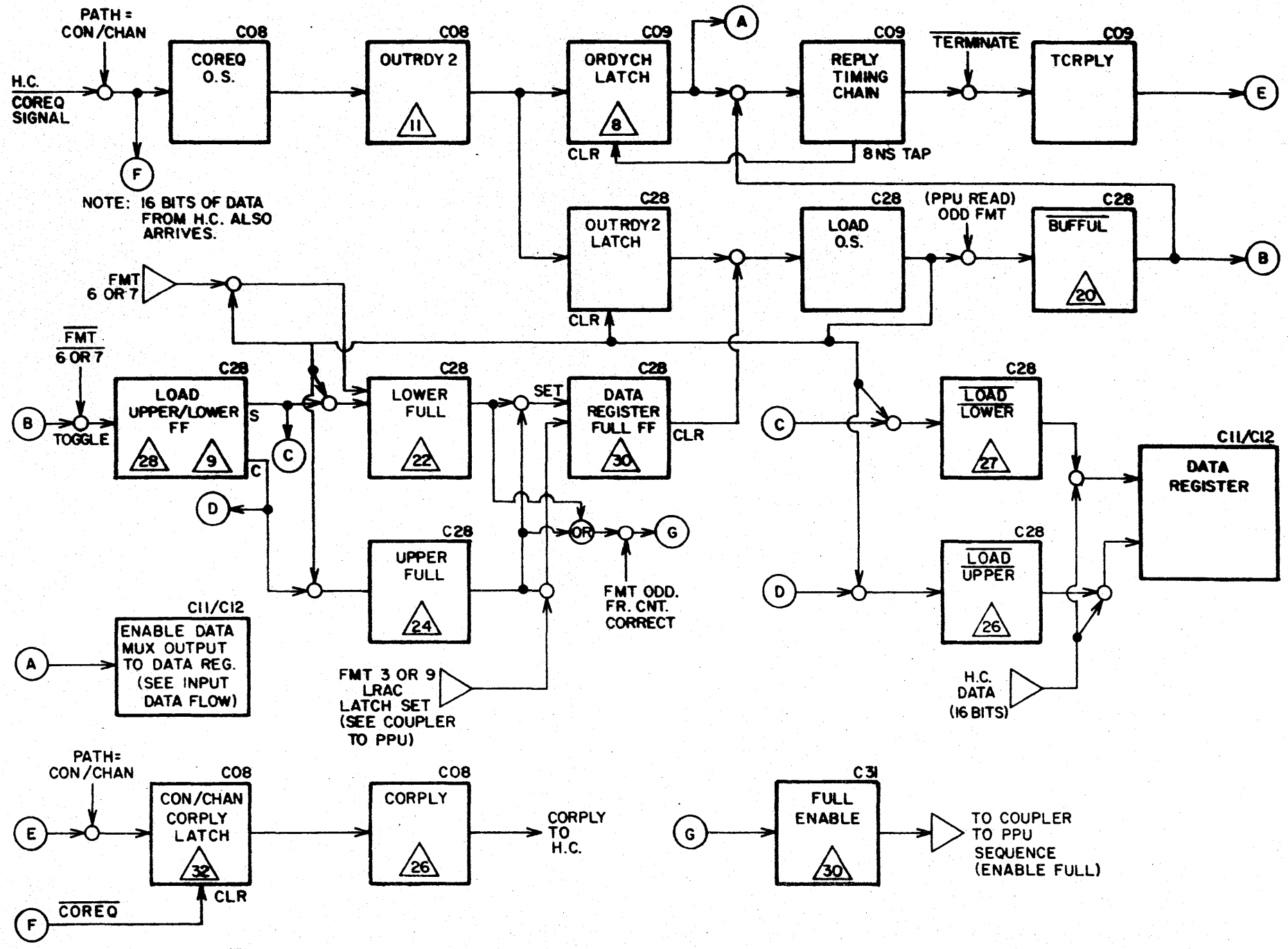


DEADMAN TERMINATE

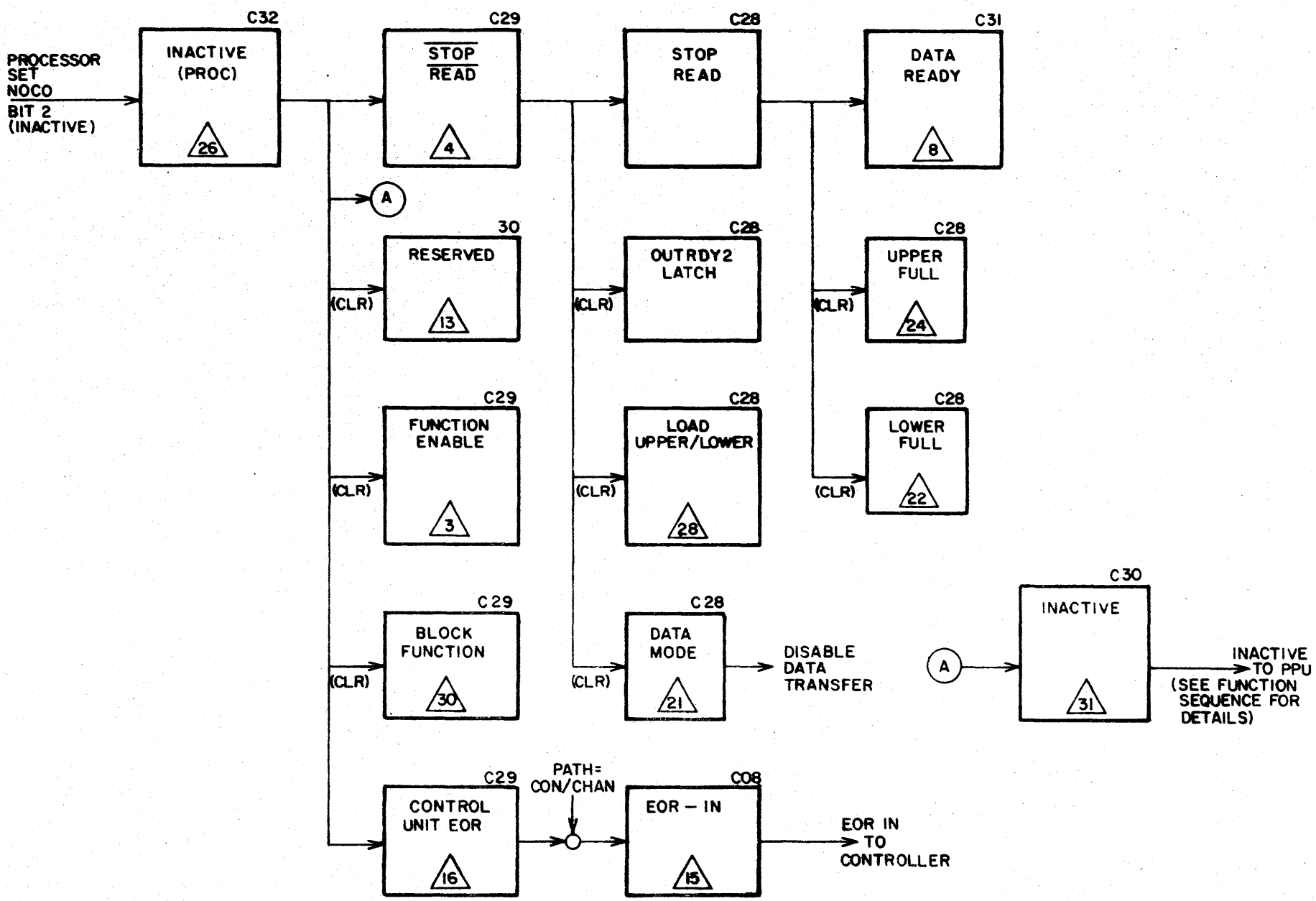
PAGE 2 OF 2



CONTROLLER TO COUPLER



TERMINATE (BC SENDS INACTIVE)



COUPLER WORKSHEET-1

1. What assembly format is used on a autoload operation?

2. What signals are sent from the coupler to the subsystem processor upon detection of a $0414_{(8)}$ function code?

3. What is the purpose of bit zero on normal input channel zero?

4. How does the B.C., receive the cylinder address following a seek function?

5. What effect will a P.P.U., command of $0014_{(8)}$ have if there was a address field correctable checkword error?

6. What operation uses format 4?

7. How is the data path through the coupler selected?

8. Is there a parity check on data transferred between the coupler and B.C.

9. How does the B.C., move the general status word from core memory, to the coupler?

10. What P.P.U., function word connects the P.P.U., to the DT220 Dual Access Coupler?

COUPLER WORKSHEET-2

1. What is the purpose of bit zero on normal output channel zero?

2. What signal gates the 16 bit data word, into the hardware controller?

3. When is the signal "Inpreq" used?

4. What is the initial frame count with format six?

5. With format four, frame count of one, what bits of data Reg., are gated through the write mux?

6. With a read mux decode of ten, what input pins to board C15 are used for data?

7. What is the purpose of the board in Loc. C22?

8. The Deadman Timer = "Terminate"; when the counter chip {C09} reaches a count of?

9. What is the purpose of normal output channel four?

10. When the P.P.U., is outputing, the data reg. is effectively a _____ bit register.

11. Under what conditions will the latch at TP11 {C24} set?

12. How is the assembly/disassembly code sent to the coupler?

13. What causes the deadman timer to expire?

14. What code on pins 2 & 14 of the mux. chip at loc. 33 {C05}, will select the path from the H.C., to P.P.U.?

15. When is the FF at TP31 {C28} set?

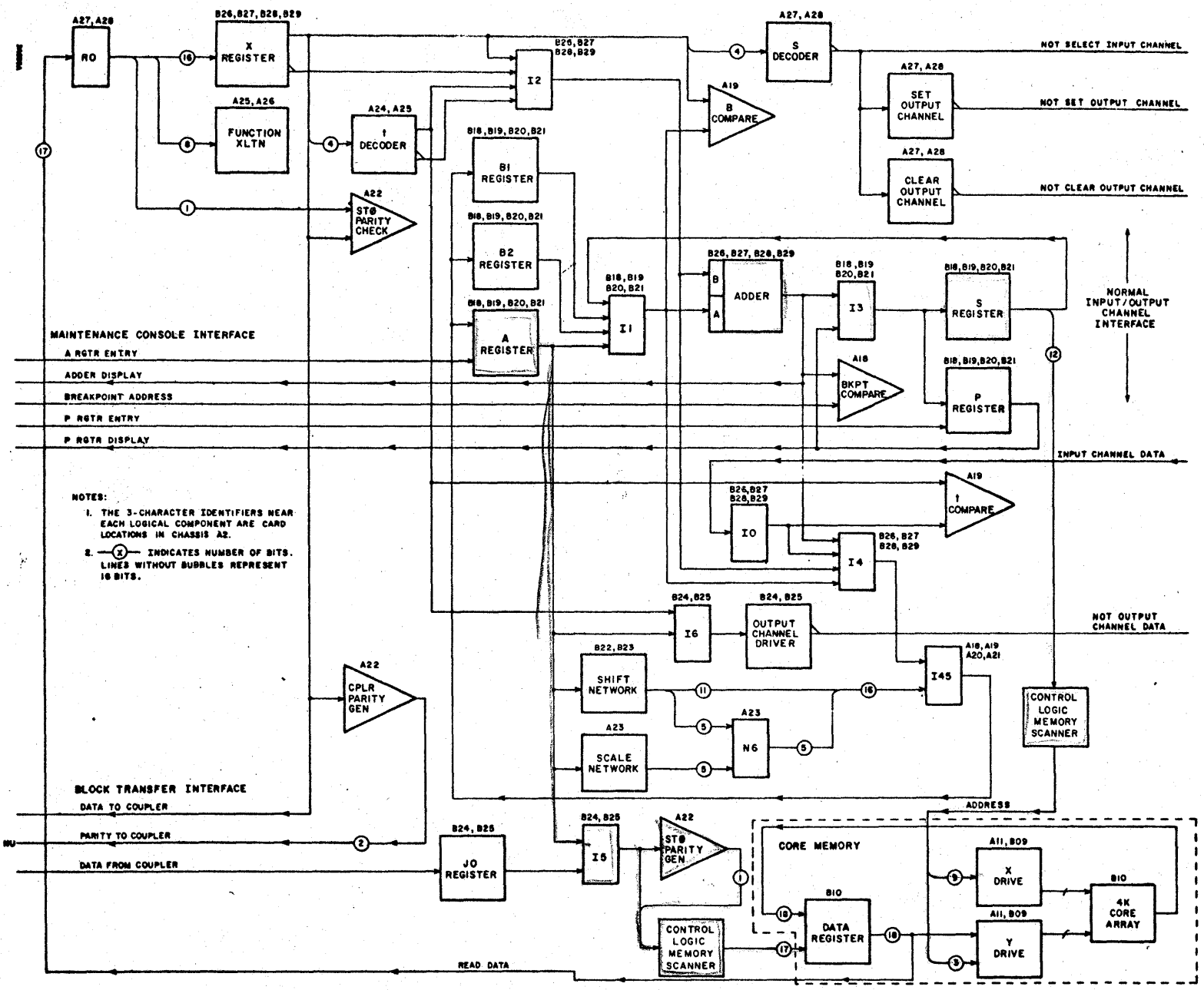


Figure 3-19. Subsystem Processor/Core Memory Data Flow

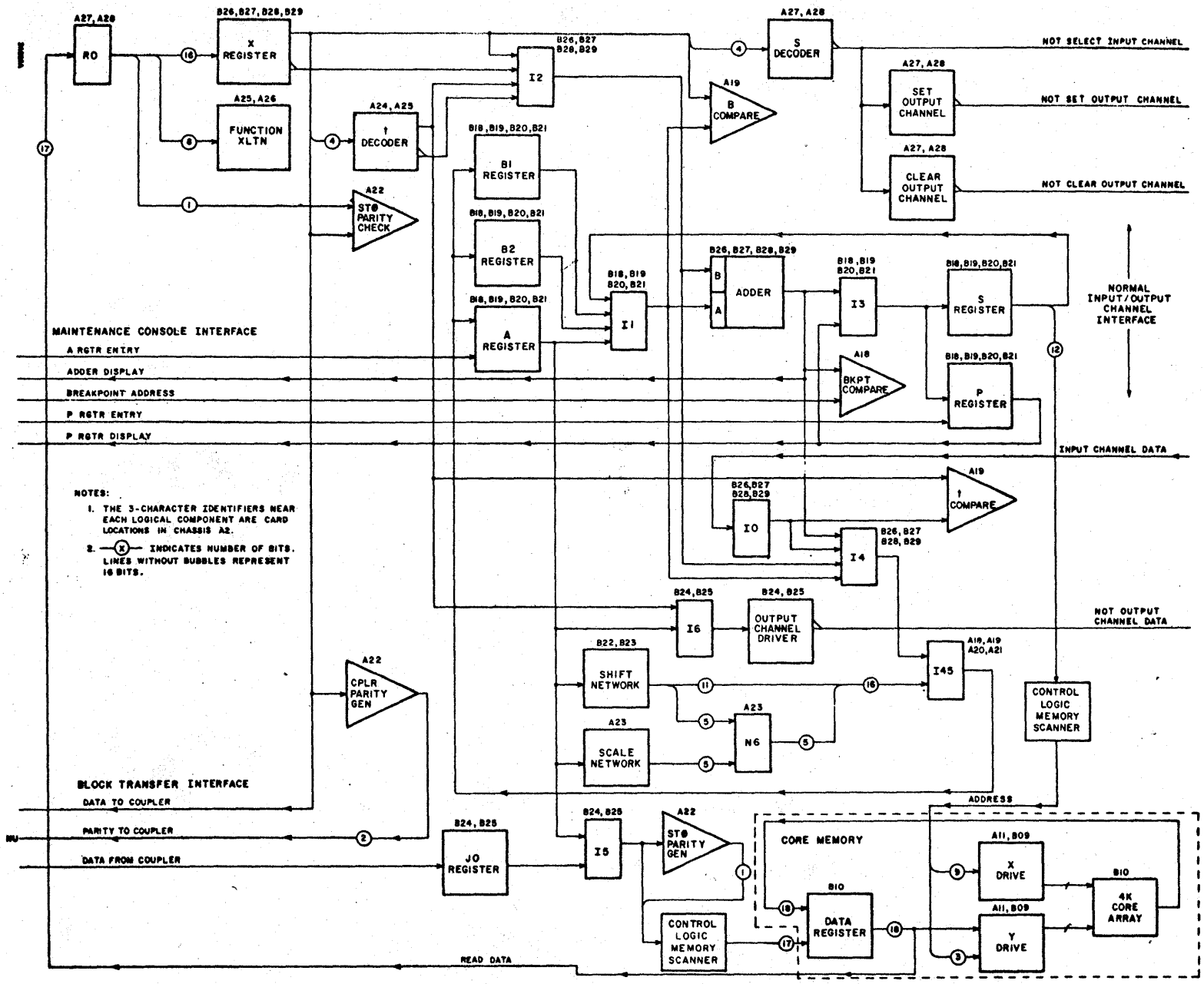


Figure 3-19. Subsystem Processor/Core Memory Data Flow

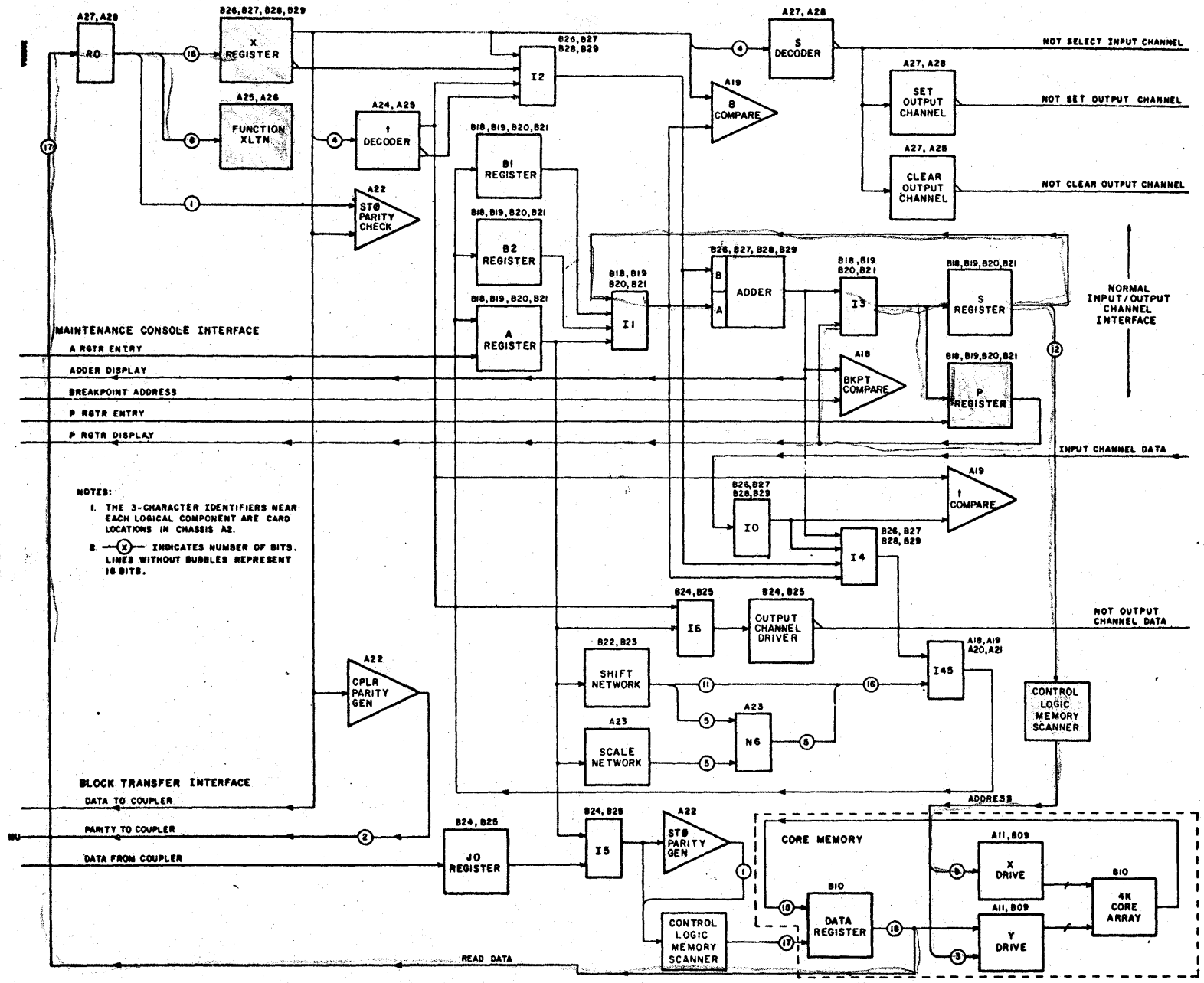


Figure 3-19. Subsystem Processor/Core Memory Data Flow

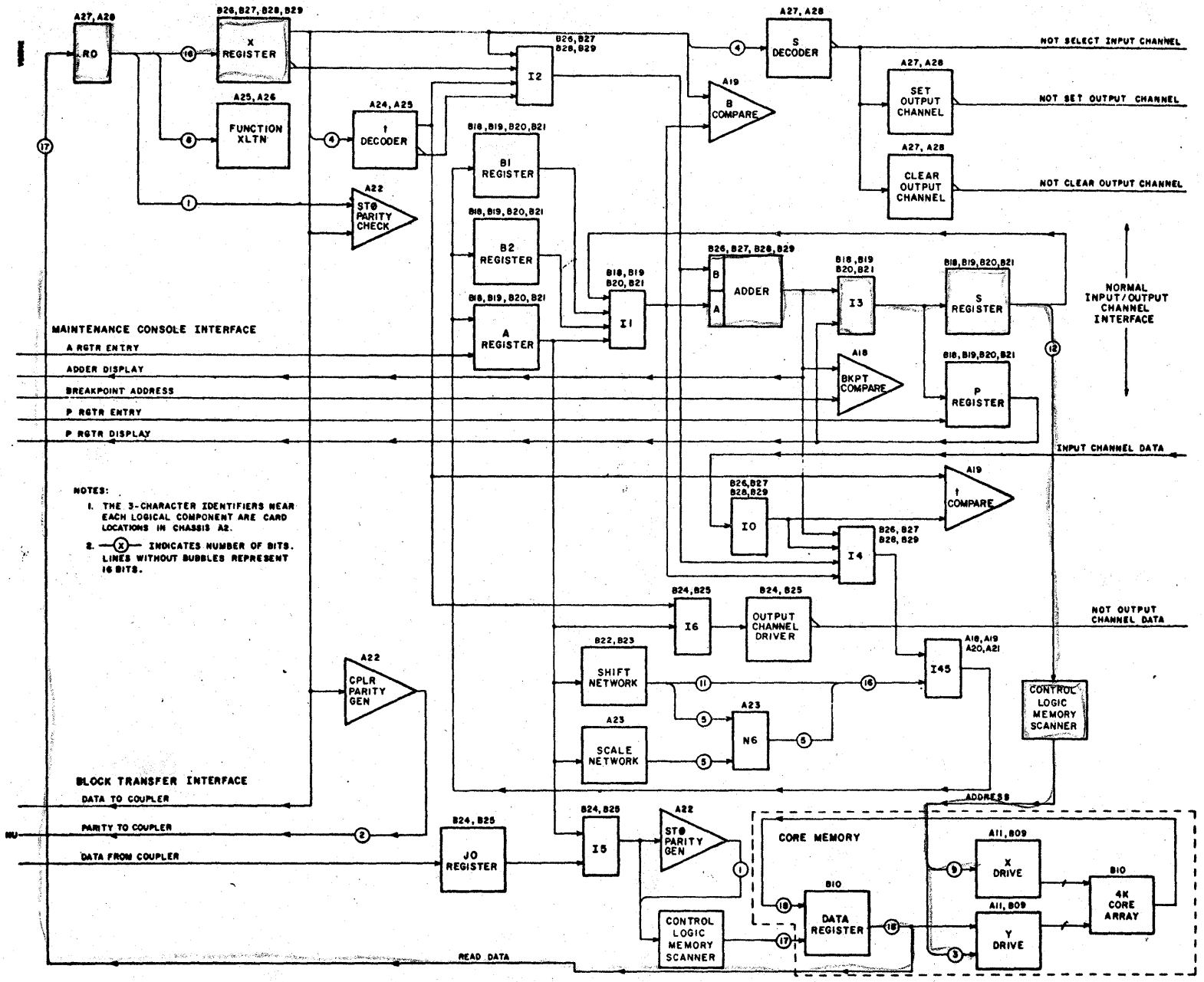


Figure 3-19. Subsystem Processor/Core Memory Data Flow

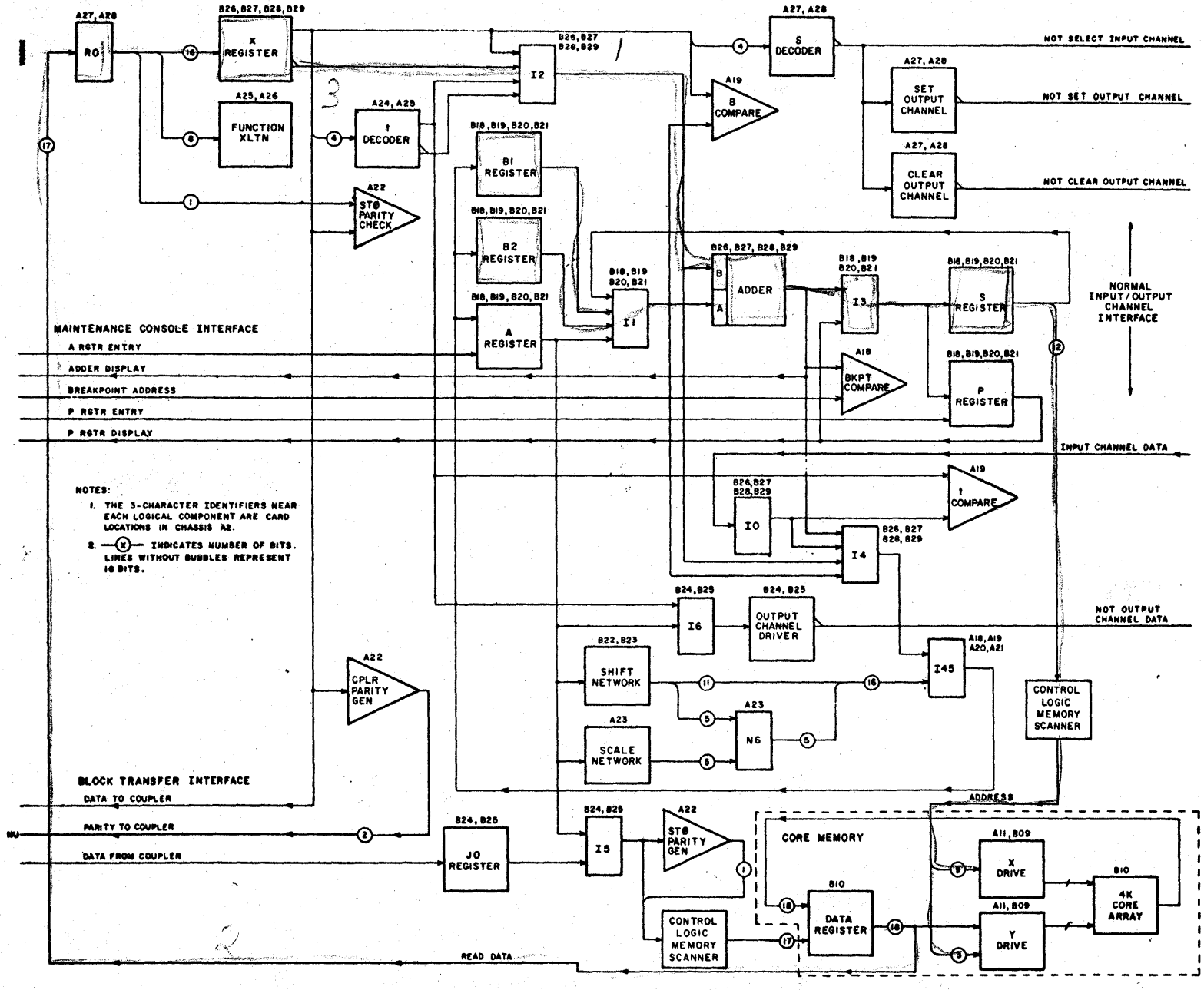


Figure 3-19. Subsystem Processor/Core Memory Data Flow

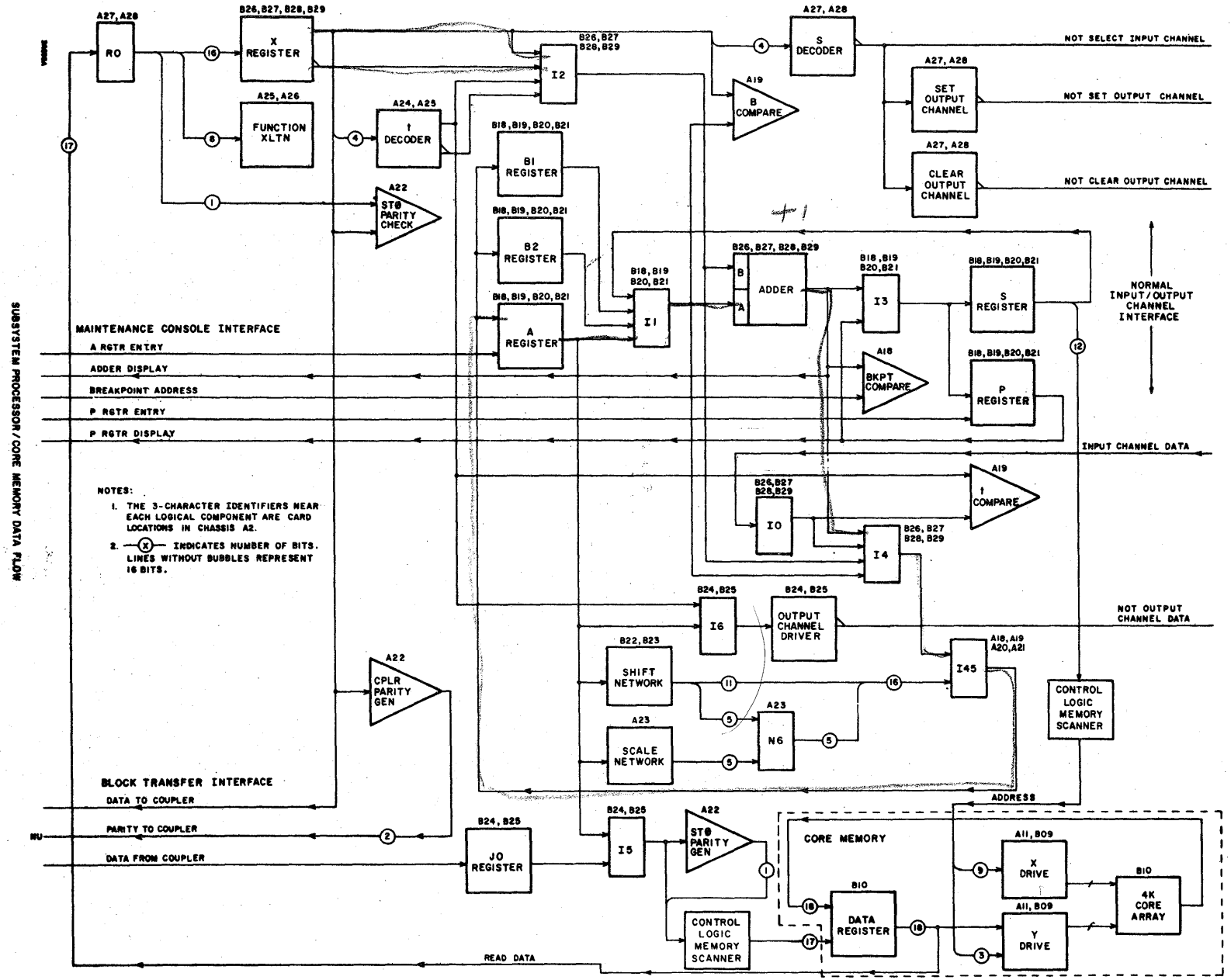


Figure 3-19. Subsystem Processor/Core Memory Data Flow

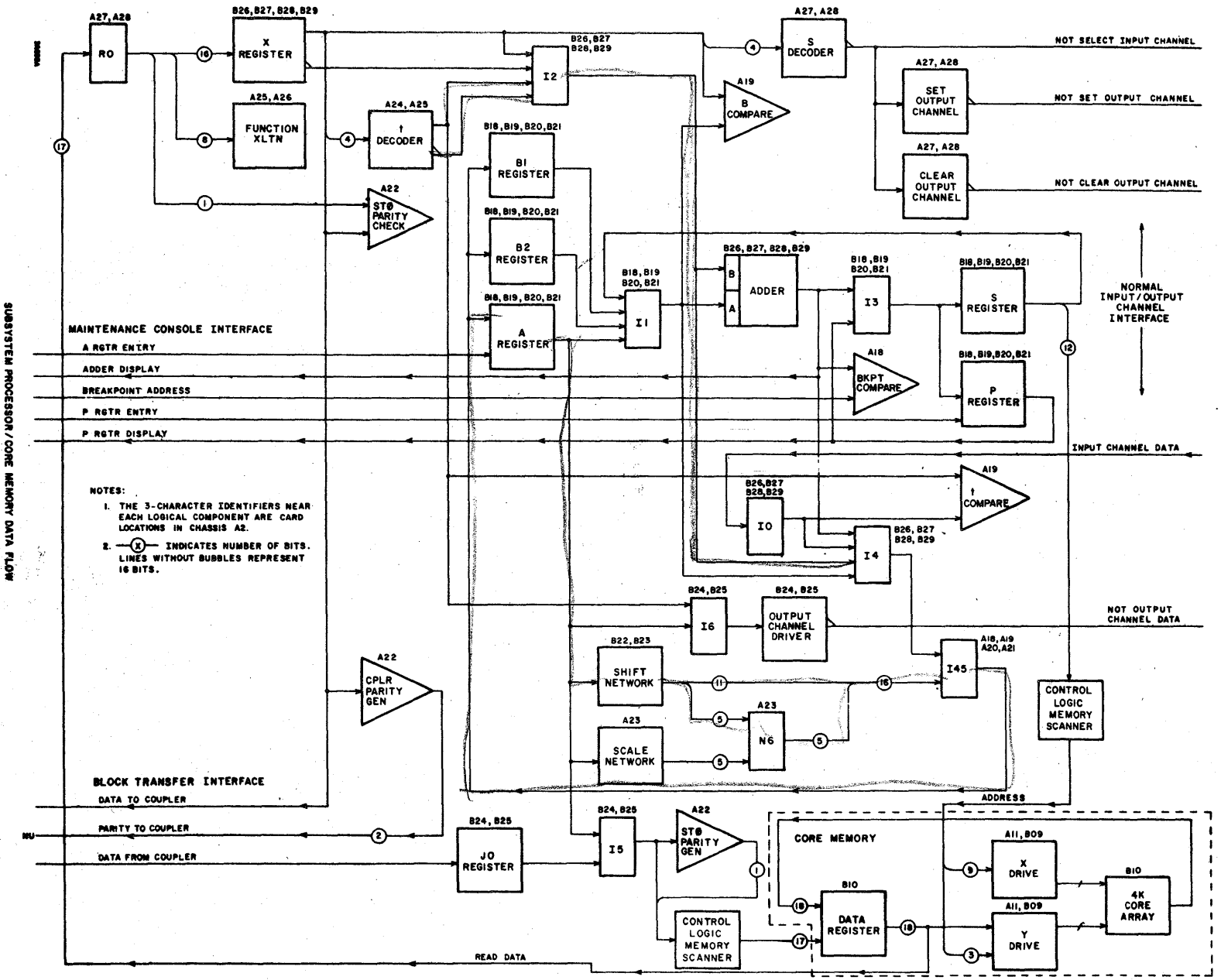


Figure 3-19. Subsystem Processor/Core Memory Data Flow

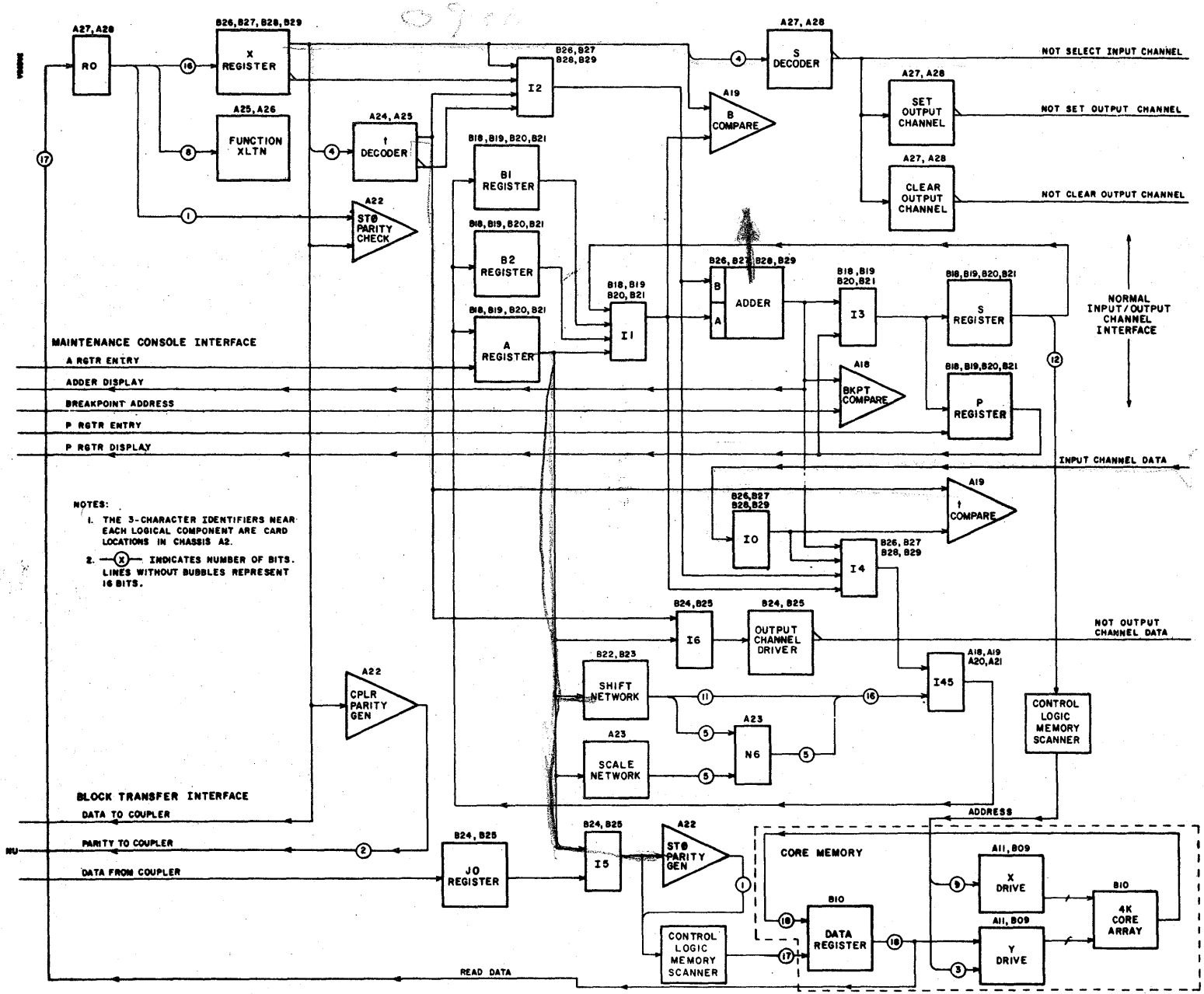


Figure 3-19. Subsystem Processor/Core Memory Data Flow

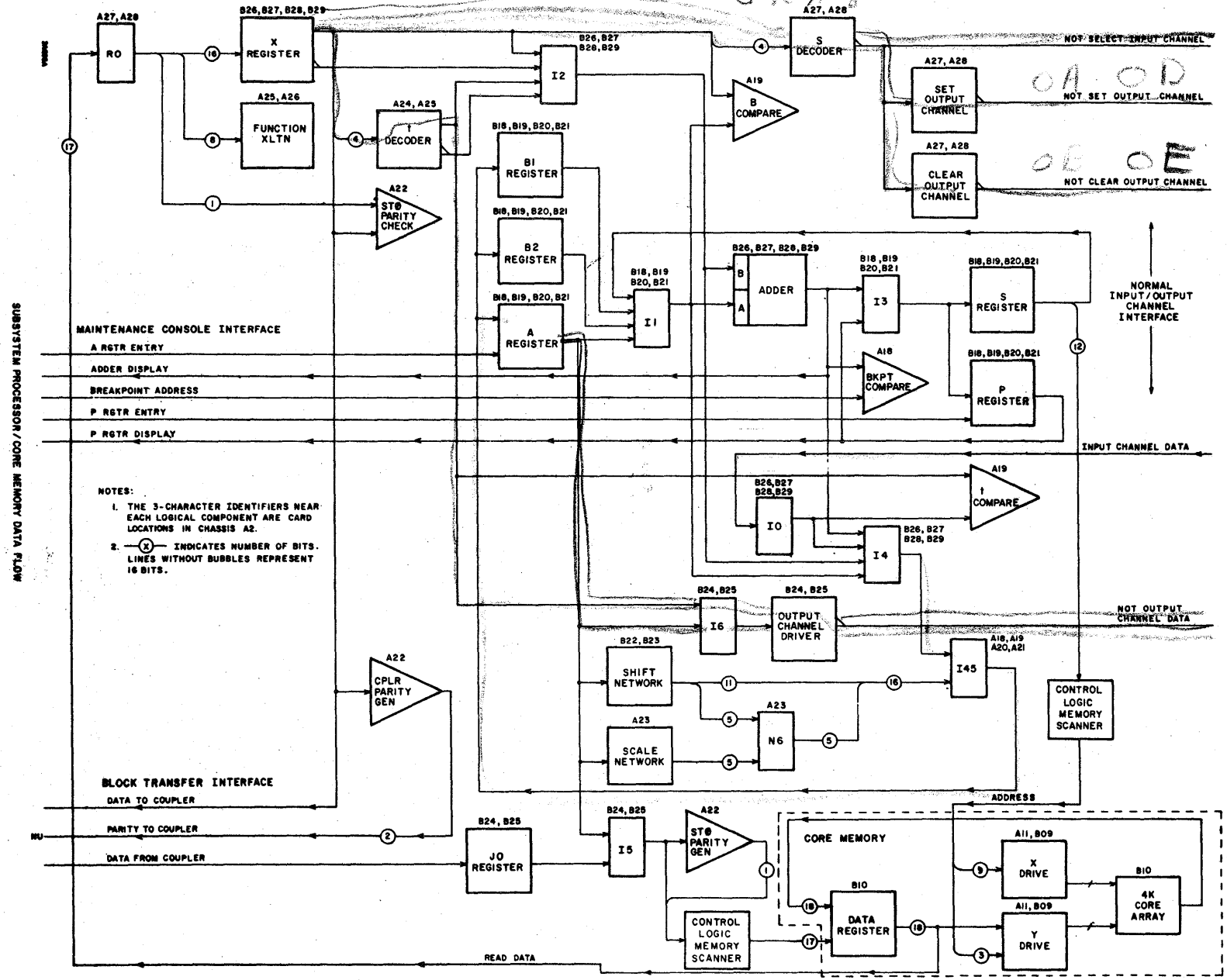


Figure 3-19. Subsystem Processor/Core Memory Data Flow

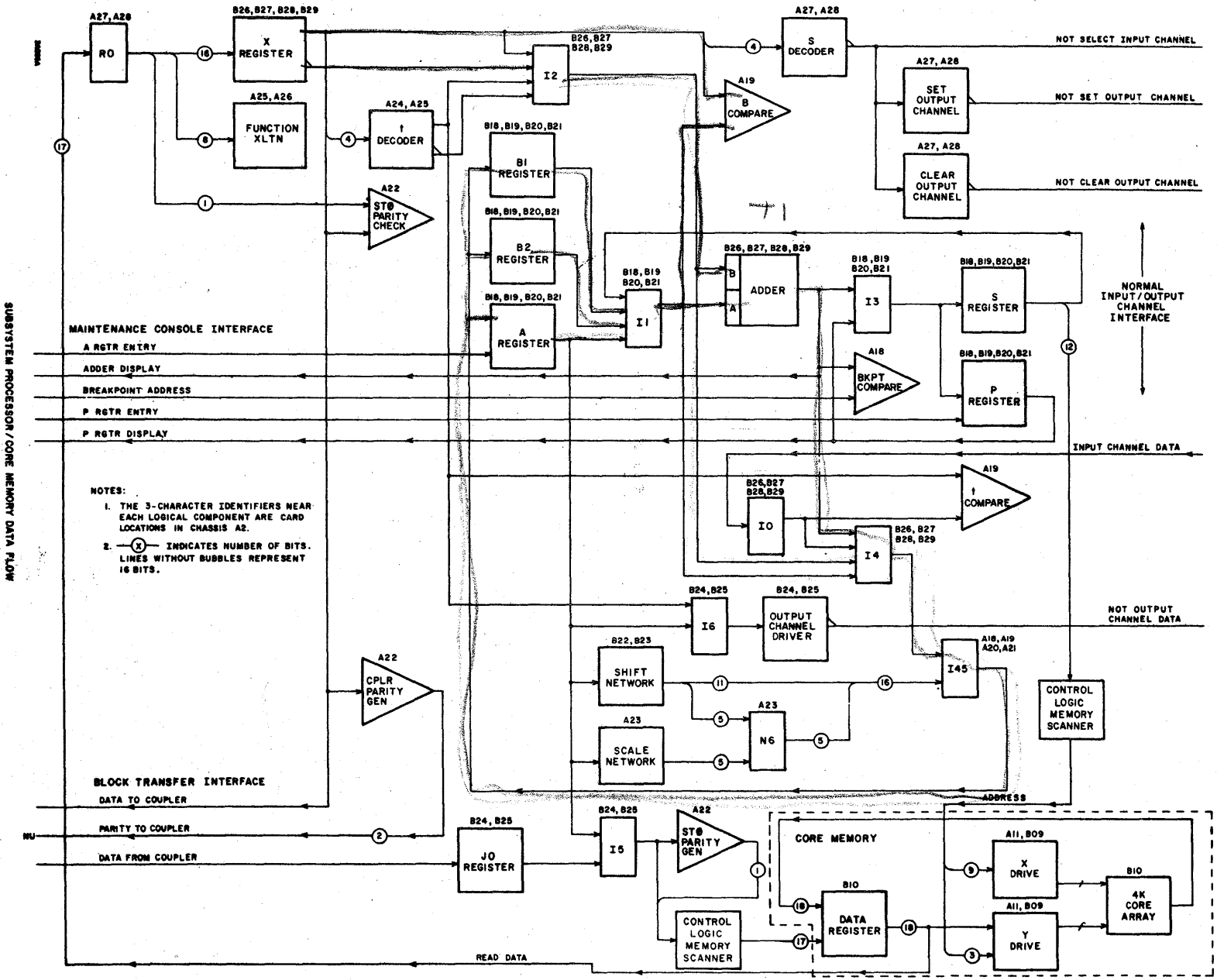


Figure 3-19. Subsystem Processor/Core Memory Data Flow

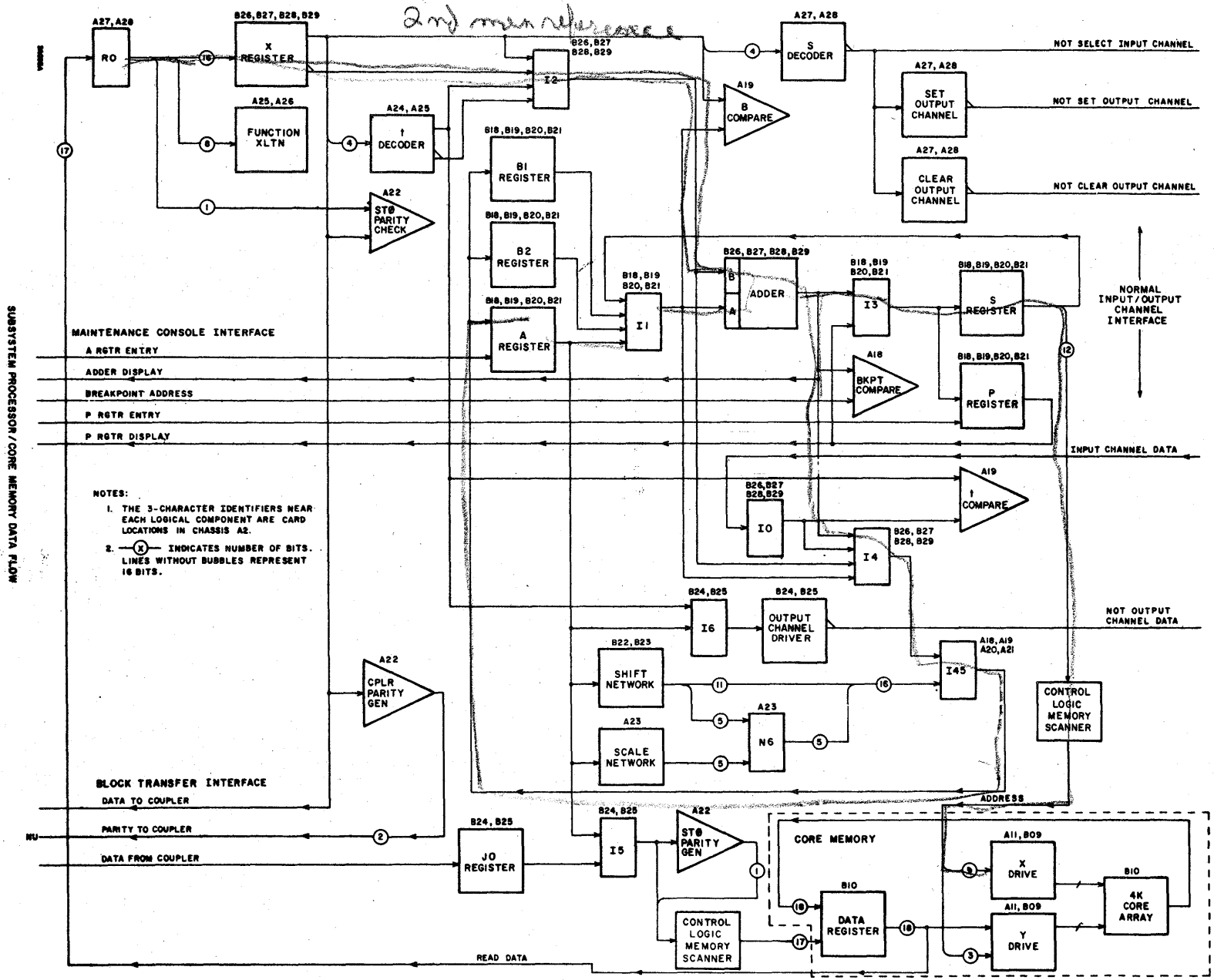


Figure 3-19. Subsystem Processor/Core Memory Data Flow

DP8 Section Number	DTA Section Number	DTB Section Number
0	0	
1	1	
2	2	
3	3	
15 *	31	31
16 *	12	1
17		9
18		8
19		20
20		21
21		10
22		12
23		11
24		15
25		4
26 *	13	2
27		6
29		22
30		23
31 ***		29
32		14
33	6	
34	7	
35 *	11	0
36 *	30	30
37	17	
40 **	18, 19, 20	
41 **	21	
42	22	
43	23	
44	24	
45	25	
46	26	
47	27	

* These sections are in both DTA and DTB.

** The testing done by sections 40 and 41 of DP8 have been split up into sections 18, 19, 20, and 21 of DTA. See ERS for DTA for further information.

*** The pack format test (section 29 of DTB) will not work unless the section procedure address is stored in the section 29 location of the section scheduler table. (Field service personnel should not need this information.)

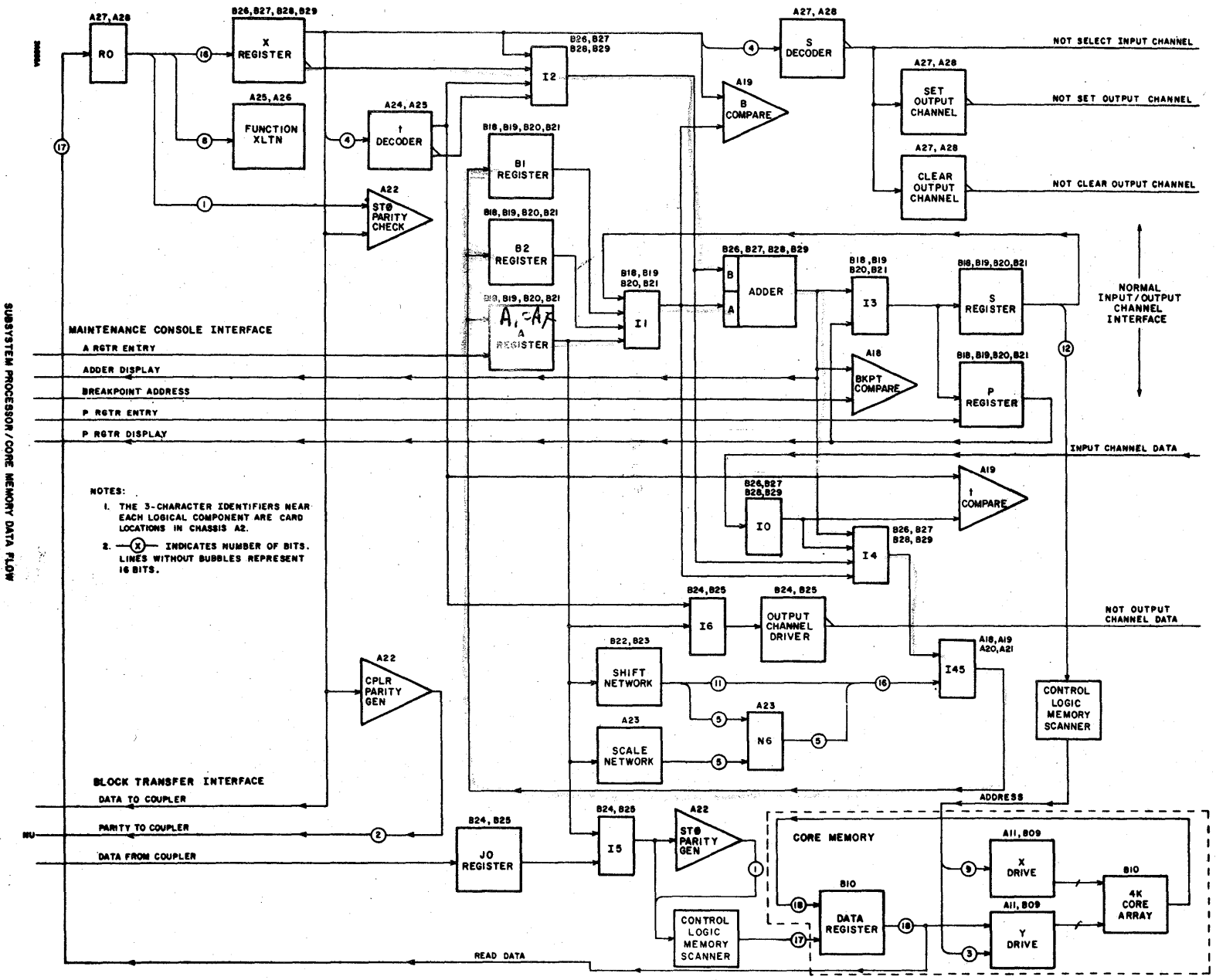


Figure 3-19. Subsystem Processor/Core Memory Data Flow

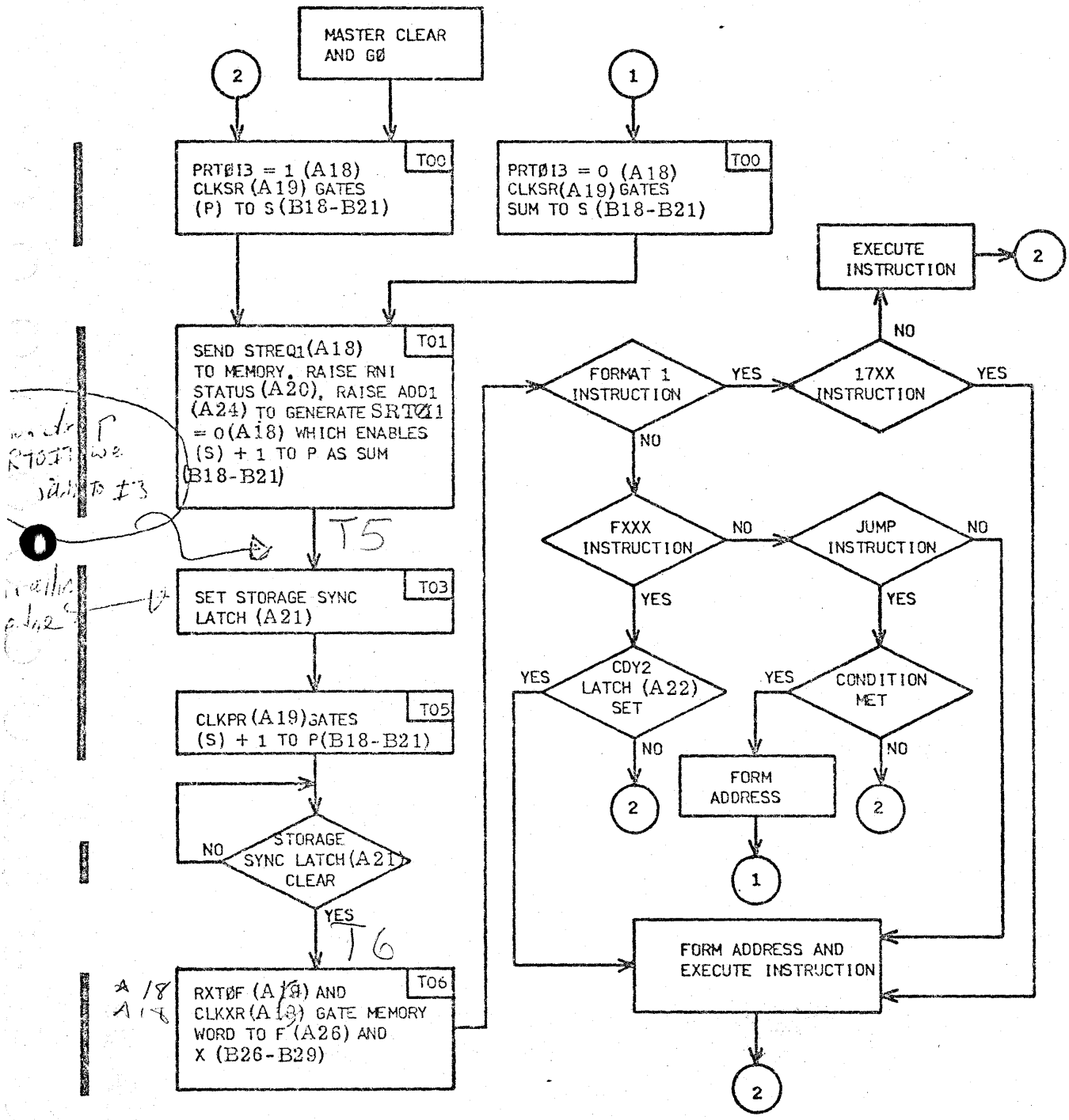


Figure 4-4. Common RNI Activity

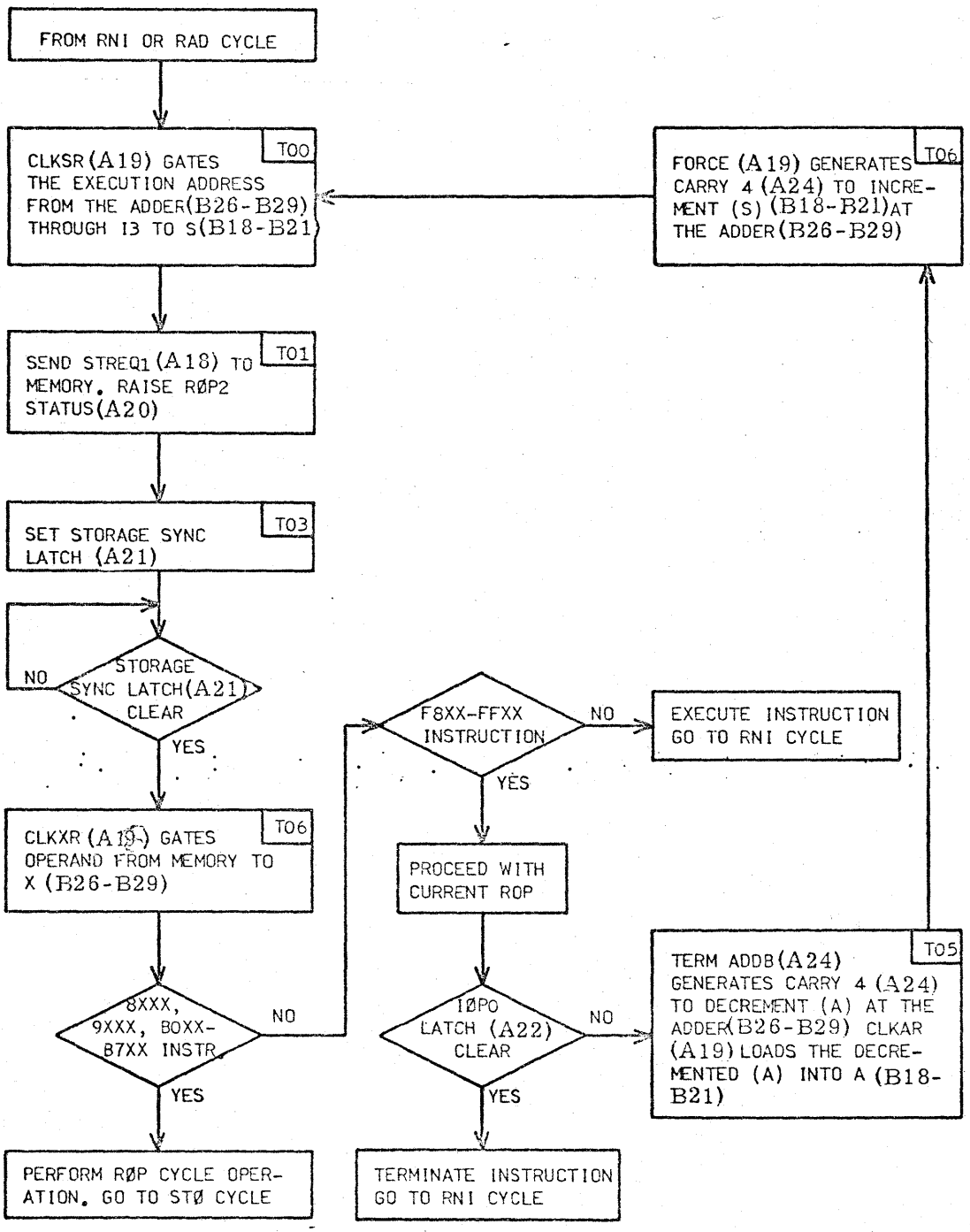


Figure 4-5. Common ROP Activity

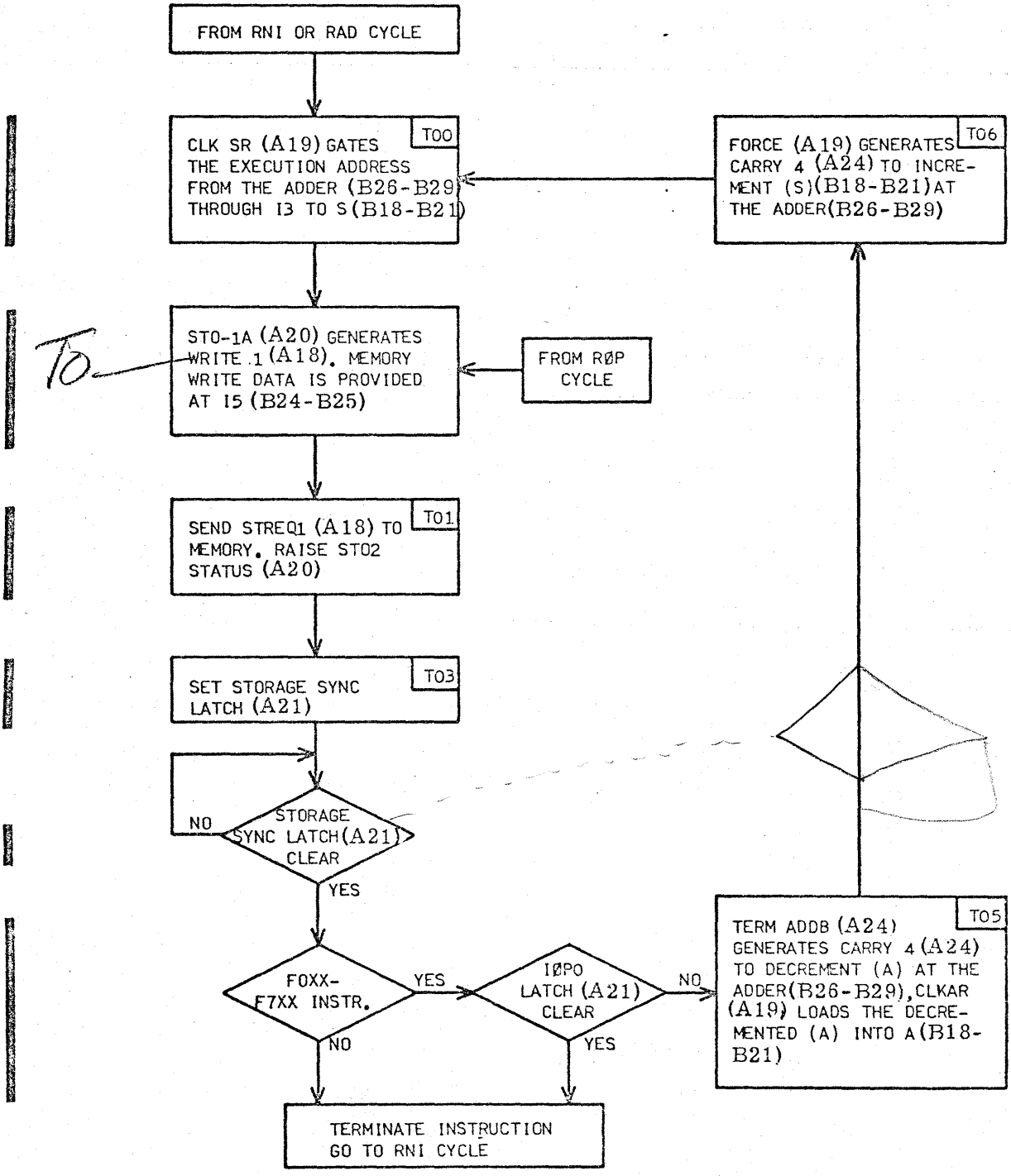


Figure 4-6. Common STO Activity