PRO-LOG
CORPORATION

STD 7000

7801
8085A Processor Card

USER'S MANUAL

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7801 USER'S MANUAL

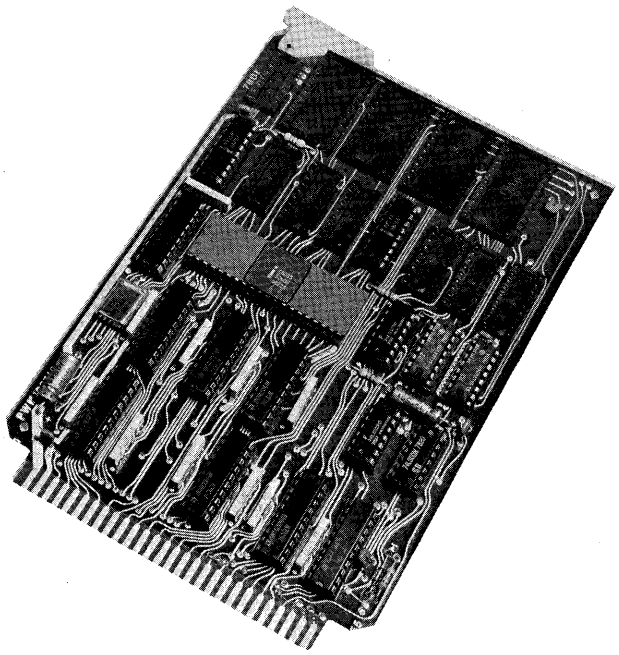
TABLE OF CONTENTS

FORM NO. 101905

8085A PROCESSOR CARD

This card combines a buffered and fully expandable 8085A microprocessor with onboard RAM and PROM sockets.

The 7801 includes 1K byte of RAM with sockets for up to 4K, and sockets for up to 8K bytes of ROM or EPROM. An STD BUS system using the 7801 card can be expanded to full 8085A memory and I/O capability. The 7801 STD BUS interface may be disabled for DMA.



FEATURES

- **8085A Processor**
- **4096 bytes RAM capacity onboard**
- **1024 bytes RAM included** (2114L type)
- **8192 bytes ROM capacity onboard** (2716 type)
- **3 State Address, Data, Control Buses**
-
- **Power-on reset or pushbutton reset input**
- **Five interrupts**
- **Serial I/O lines**
- **All IC's socketed**
- **Single +5V operation**
- 7801: 6.25 MHz crystal, 320ns time states
- 7801-1: 6.144MHz crystal, 325.5ns time states
- External clock input option

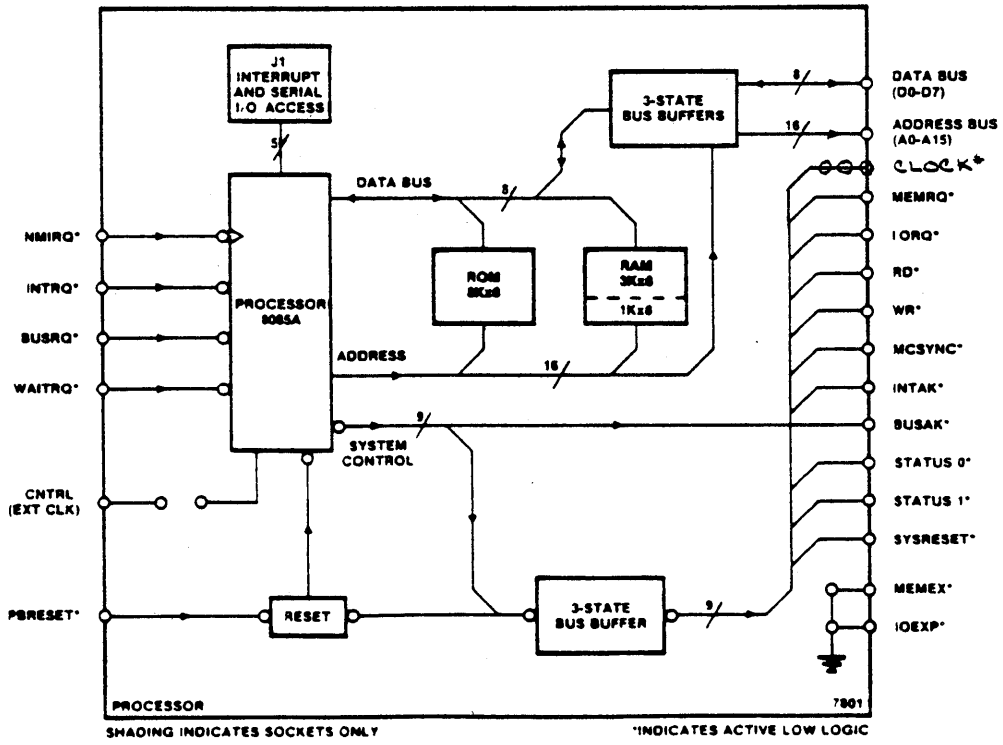


FIGURE ONE: 7801 BLOCK DIAGRAM

SECTION TWO - THE STD BUS

The STD BUS standardizes the physical and electrical aspects of modular 8-bit microprocessor card systems, providing a dedicated, orderly interconnect scheme. The STD BUS is dedicated to internal communication and power distribution between cards, with all external communication made via I/O connectors which are suitable to the application. The standardized pinout and 56-pin connector lends itself to a bussed motherboard that allows any card to work in any slot.

As the system processor and primary system control card, the 7801 is responsible for maintaining the signal functionality defined by the STD BUS standard.

A complete copy of the STD BUS standard is contained in the SERIES 7000 STD BUS TECHNICAL MANUAL, available from Pro Log Corporation, 2411 Garden Road, Monterey, California 93940.

STD BUS Summary

The 56-pin STD BUS is organized into five functional groups of backplane signals:

1. Logic Power Bus pins 1-6
2. Data Bus pins 7-14
3. Address Bus pins 15-30
4. Control Bus pins 31-52
5. Auxilary Power pins 53-56

Figure 2 shows the organization and pinout of the STD BUS with mnemonic function and signal flow relative to the 7801 Processor card:

	COMPONENT SIDE				CIRCUIT SIDE			
	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION
LOGIC POWER BUS	1	+5V	In	+5 Volts DC (Bussed)	2	+5V	In	+5 Volts DC Bussed)
	3	GND	In	Digital Ground (Bussed)	4	GND	In	Digital Ground Bussed)
	5	-5V		-5 Volts DC	6	-5V		-5 Volts DC
DATA BUS	7	D3	In/Out	Low Order Data Bus	8	D7	In/Out	High Order Data Bus
	9	D2	In/Out	Low Order Data Bus	10	D6	In/Out	High Order Data Bus
	11	D1	In/Out	Low Order Data Bus	12	D5	In/Out	High Order Data Bus
	13	D0	In/Out	Low Order Data Bus	14	D4	In/Out	High Order Data Bus
ADDRESS BUS	15	A7	Out	Low Order Address Bus	16	A15	Out	High Order Address Bus
	17	A6	Out	Low Order Address Bus	18	A14	Out	High Order Address Bus
	19	A5	Out	Low Order Address Bus	20	A13	Out	High Order Address Bus
	21	A4	Out	Low Order Address Bus	22	A12	Out	High Order Address Bus
	23	A3	Out	Low Order Address Bus	24	A11	Out	High Order Address Bus
	25	A2	Out	Low Order Address Bus	26	A10	Out	High Order Address Bus
	27	A1	Out	Low Order Address Bus	28	A9	Out	High Order Address Bus
	29	A0	Out	Low Order Address Bus	30	A8	Out	High Order Address Bus
CONTROL BUS	31	WR*	Out	Write to Memory or I/O	32	RD*	Out	Read to Memory or I/O
	33	IORQ*	Out	I/O Address Select	34	MEMRQ*	Out	Memory Address Select
	35	IOEXP*	Out	I/O Expansion	36	MEMEX*	Out	Memory Expansion
	37	REFRESH*		Refresh Timing	38	MCSYNC*	Out	CPU Machine Cycle Sync
	39	STATUS 1*	Out	CPU Status	40	STATUS 0*	Out	CPU Status
	41	BUSAK*	Out	Bus Acknowledge	42	BUSRQ*	In	Bus Request
	43	INTAK*	Out	Interrupt Acknowledge	44	INTRQ*	In	Interrupt Request
	45	WAITRQ*	In	Wait Request	46	NMIRQ*	In	Non-Maskable Interrupt
	47	SYSRESET*	Out	System Reset	48	PBRESET*	In	Push Button Reset
	49	CLOCK*	Out	Clock from Processor	50	CNTRL*	In	AUX Timing
	51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
POWER BUS	53	AUXGND		AUX Ground (Bussed)	54	AUXGND		AUX Ground Bussed)
	55	AUX +V		AUX Positive (+12 Volts DC)	56	AUX -V		AUX Negative -12 Volts DC)

*Low Level Active Indicator

FIGURE 2: THE STD BUS

STD BUS Pin Utilization by 7801

Since the STD BUS standard does not specify timing or require that all available pins be used, the timing and signal allocation assumes many of the characteristics of the microprocessor type used. The characteristics of the 7801 are dictated by its 8085A microprocessor, with LSTTL buffering added to enhance the card's drive capability. The buffers decrease memory and I/O access time slightly.

The allocation of STD BUS lines for the 7801 is given below.

1. Logic Power Bus: +5V (pins 1,2) and Logic Ground (Pins 3,4) supply operating power to the 7801. Pins 5 and 6 are open.

2. Data Bus: Pins 7 through 14 form an 8-bit bidirectional 3-state data bus as shown in Figure 2 . High level active data flows between the 7801 and its peripheral cards over this bus. When the 7801 fetches data from its onboard memory sockets, this data also appears on the STD Data Bus.

   With the exception of Direct Memory Access (DMA) operations, the 7801 controls the direction of data flow with its MEMRQ*, IORQ*, RD*, WR*, and INTAK* control signal outputs. Peripheral cards are required to release the data bus to the high impedance state except when addressed and directed to drive the data bus by the 7801. Note that the low-order address bits (A0-A7) are multiplexed on the Data Bus.; A0-A7 appear on D0-D7 while MCSYNC* is active. The 7801 releases the Data Bus when BUSAK* is active in response to BUSRQ*, as in DMA operations.

3. Address Bus: Pins 15 through 30 form a 16-bit 3-state address bus as shown in Figure 2 . The 7801 drives high level active 16-bit memory addresses over these lines, and 8-bit I/O port addresses over the eight low-order address lines (A0 through A7 on pins 15, 17, 19, 21, 23, 25, 27 and 29).

   The 7801 releases the Address Bus when BUSAK* is active in response to BUSRQ*, as in DMA operations.

4. Control Bus: Pins 31 through 52 provide control signals for memory, I/O, interrupt, and fundamental system operations. Figure 3 summarizes these signals and shows how they are derived from 8085A signals.

   The 7801 releases the Control Bus during BUSAK* in response to BUSRQ*, except for the following output signals: MEMEX*, IOEXP*, BUSAK*, CLOCK*, PCO.

5. Auxilary Power Bus: Pins 53 through 56 are not used by the 7801 and are electrically open.

The 7801 meets all of the signal requirements of the STD BUS standard. Detailed timing information and specifications are in Section 3.

MNEMONIC	PIN	IN/OUT	FUNCTION	HOW DERIVED; 8085A NAME
WR*	31	Out#	Write to memory or I/O	[WR*]
RD*	32	Out#	Read from memory or I/O	[RD*]
IORQ*	33	OUT#	A0-A7 hold valid I/O address	[IO/M*]*
MEMRQ*	34	OUT#	A0-A15 hold valid memory address	[IO/M*]
IOEXP*	35	OUT	I/O expansion control	User-removable ground
MEMEX*	36	OUT	Memory expansion control	User-removable ground
REFRESH*	37	-	(Not used)	Electrically open
MCSYNC*	38	OUT#	One transition per machine cycle; undecoded status	[ALE]*
STATUS 1*	39	OUT#	Undecoded status; Note 1	[S1]*
STATUS 0*	40	OUT#	Undecoded status; Note 1	[S0]*
BUSAK*	41	OUT	Acknowledges BUSRQ*	[HLDA]*
BUSRQ*	42	IN	Bus request (DMA); synchronous processor halt and 3-state driver disable	[HOLD]*
INTAK*	43	OUT#	Acknowledges INTRQ* and replaces (MEMRQ* · RD*) to read interrupt vector	[INTA*]
INTRQ*	44	IN	Maskable interrupt request	[INTR]*
WAITRQ*	45	IN	Synchronous processor halt	[RDY]
NMIRQ*	46	IN	Nonmaskable interrupt request	[TRAP]*
SYSRESET*	47	OUT#	System power-on and pushbutton reset one-shot output	[RST]*
PBRESET*	48	IN	Pushbutton reset input	[R*]
CLOCK*	49	OUT	Time State Clock (1/2 crystal frequency)	[CLOCK]* - user optional jumper connection
CNTRL*	50	IN	External clock input (2 times Time State Clock frequency)	Ø1 - user optional jumper connection
PCI/PCO	52/51	IN/OUT	Priority chain	Note 2

* Low level active
\# Output buffer disabled when BUSAK* active
[] Denotes equivalent 8085A signal name

NOTES: 1. See Figure 4 for status information.
2. Trace on 7801 connects PCI to PCO to maintain chain continuity.

FIGURE 3 : 7801 CONTROL BUS SIGNALS

7801 Processor Status: MCSYNC*, STATUS 0*, STATUS 1* Signals

MCSYNC*, STATUS 0*, and STATUS 1* signals provide encoded status information which is peculiar to the 8085A microprocessor. These signals are useful for displaying processor status in logic signal analyzers, and can be used to drive certain peripheral chips and systems designed to work with the 8085A specifically. The use of these signals is not recommended in systems where microprocessor device-type independence is a design goal.

MCSYNC* serves a dual function. Its leading edge denotes the approximate start of a machine cycle (Section 3). Counting the MCSYNC* transitions allows a logic signal analyzer to select a specific machine cycle within a multi-cycle instruction for analysis.

The lagging edge of MCSYNC* occurs when a stable memory line address or I/O port address is present on the STD Data Bus. The 8085A device multiplexes its low order address lines (A0-A7) during time state T1; the address information is followed by data in subsequent time states within the machine cycle. The lagging (rising) edge of MCSYNC* is used on the 7801 to latch the low order address.

MCSYNC* is equivalent to the 8085A's ALE (Address Latch Enable) output signal.

STATUS 0* and STATUS 1* can be decoded externally to identify the type of machine cycle in progress as shown in Figure 4:

SEE NOTE	MACHINE CYCLE TYPE	STATUS 0*	STATUS 1*	MEMRQ*	IORQ*	RD*	WR*	INTAK*
	Read instruction opcode	0	0	0	1	0	1	1
	Read memory except opcode	1	0	0	1	0	1	1
	Write in memory	0	1	0	1	1	0	1
1	Acknowledge INTRQ*	0	0	1	0	1	1	0
1	Acknowledge NMIRQ* and interrupts 5.5,6.5,7.5	0	0	1	0	1	1	1
2	Bus idle during ADP (Add to H,L pair) instruction	1	0	0	1	1	1	1
3	HALT instruction	1	1	1	0	1	1	1

FIGURE 4: MACHINE CYCLE STATUS SIGNALS *low active: Active = 0 Inactive = 1

NOTES:
1. The states shown for MEMRQ* and IORQ* during interrupt acknowledge cycles are those produced by the 8085A device. For the earlier 8085, the MEMRQ* and IORQ* states are reversed.
2. The Data Bus is idle during the second and third machine cycles machine cycles for the ADP instruction (Intel mnemonic is DAD). No MCSYNC* (ALE*) signal is generated during these cycles. ((8085A only).
3. Processor pins IO/M*, RD*, WR* are in the high impedance state.
4. Timing for STATUS 0* and STATUS 1* is similar to Address Bus timing (Section 3). For additional information, refer to the 8085A manufacturer's literature.

SECTION 3 - 7801 SPECIFICATIONS

Power Requirements

RECOMMENDED OPERATING LIMITS				ABSOLUTE NONOPERATING LIMITS		
PARAMETER	MIN	TYP	MAX	MIN	MAX	UNITS
Vcc (Note 1)	4.75	5.00	5.25	0	5.50	Volts
Icc (Note 2)		1.00	1.40			Ampere

FIGURE 5: 7801 POWER SUPPLY SPECIFICATION

NOTES:
1. In order to guarantee correct operation, the following power supply considerations apply:
   a. Vcc rise must be monotonic, rising from +0.50 Volt to +4.75 Volts in 10 ms or less.
   b. If Vcc drops below +4.75 Volts at any time it must be returned to less than +0.50 Volt before restoration to the specified operating range.
2. Icc specification assumes that all EPROM and RAM sockets on the 7801 are loaded. Subtract 75 mA per 2716 EPROM and 50mA per 2114L RAM for each device not used. (typical values)

Both the 8085A and 2114L devices require 10 milliseconds minimum after initial power-on for stabilization of internal bias oscillators. The 7801's power-on reset one-shot provides adequate stabilization delay, only if Vcc risetime is less than 10 milliseconds.

Drive Capability and Loading

The 7801's STD BUS Edge Connector Pin List (Figure 6) and Serial I/O and Interrupt Socket J1 (Figure 7) give input loading and output drive capability in LSTTL loads as defined by the SERIES 7000 TECHNICAL MANUAL.

In general, input lines and disabled 3-state outputs present 5 LSTTL loads maximum (one LSTTL or MOS input plus 4.7K pullup resistor). Output lines can drive a minimum of 50 LSTTL loads. Pins which are unspecified in Figures 6 and 7 are electrically open.

Exceptions to the general loading rules are:

a. WAITRQ* input, which is 15 LSTTL loads.

b. PBRESET* input, which is 1 uF typical in parallel with 2 LSTTL loads.

c. CLOCK* output, which can drive 10 LSTTL loads.

d. PCI and PCO, which are connected to each other but to nothing else on the 7801.

FIGURE 6 : 7801 STD BUS EDGE CONNECTOR PINOUT AND LOADING

STD/7801 EDGE CONNECTOR PIN LIST							
PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
2	IN		+5 VOLTS	1		IN	+5 VOLTS
4	IN		GROUND	3		IN	GROUND
6			-5V	5			-5V
8	5	50	D7	7	50	5	D3
10	5	50	D6	9	50	5	D2
12	5	50	D5	11	50	5	D1
14	5	50	D4	13	50	5	D0
16	5	50	A15	15	50	5	A7
18	5	50	A14	17	50	5	A6
20	5	50	A13	19	50	5	A5
22	5	50	A12	21	50	5	A4
24	5	50	A11	23	50	5	A3
26	5	50	A10	25	50	5	A2
28	5	50	A9	27	50	5	A1
30	5	50	A8	29	50	5	A0
32	5	50	RD*	31	50	5	WR*
34	5	50	MEMRQ*	33	50	5	IORQ*
36		OUT	MEMEX* (GROUND)	35	OUT		IOEXP* (GROUND)
38	5	50	MCSYNC* (ALE*)	37			REFRESH*
40	5	50	STATUS 0* (S0*)	39	50	5	STATUS 1* (S1*)
42	5		BUSRQ* (HOLD*)	41	50	5	BUSAK* (HLDA*)
44	5		INTRQ* (INTR*)	43	50	5	INTAK* (INTA*)
46	5		NMIRQ* (TRAP*)	45		15	WAITRQ* (READY)
48	1 μF		PBRESET* (R*)	47	50	5	SYSRESET* (RST*)
50			CNTRL* - EXT CLK IN	49	10		CLOCK*
52	IN		PC1	51	OUT		PC0
54			AUX GND	53			AUX GND
56			AUX -V	55			AUX +V

***Designates Active Low Level Logic**

() Designates equivalent 8085A pin names

J1 SERIAL I/O AND INTERRUPT PIN OUT AND LOADING							
PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL)				OUTPUT (LSTTL)			
INPUT (LSTTL)						INPUT (LSTTL)	
INTERRUPT 7.5 *	5		1	16	OUT		GROUND
INTERRUPT 6.5 *	5		2	15	OUT		GROUND
INTERRUPT 5.5 *	5		3	14	OUT		GROUND
SOD*		50	4	13	OUT		GROUND
SID*	5		5	12	OUT		GROUND
(SPARE)			6	11	OUT		GROUND
(SPARE)			7	10	OUT		GROUND
(SPARE)			8	9	OUT		GROUND

*Low Level Active

FIGURE 7 : SERIAL I/O & INTERRUPT CONNECTOR PINOUT AND LOADING

NOTE: Pads are provided at spare pins for user-connected signals

Clock Generator

The 7801's 8085A microprocessor has an internal clock oscillator that serves as the primary timing element in a 7801-based system. The oscillator's output is divided by two to produce the time state clock. The time state clock's period is the shortest program-related period of interest in the system. Instruction execution times are computed as whole multiples of the time state clock period (see Section 5).

The 7801 is shipped with a crystal installed which sets the system's time state period. The only difference between the 7801 and 7801-1 is the resonant frequency of this crystal.

If desired, the user can substitute a different crystal or replace the crystal with a TTL-compatible clock signal generated externally. Details of this option are given in Appendix A. The frequency/period characteristics of the crystal or external clock signal are shown in Figure 8 .

CRYSTAL OR EXTERNAL CLOCK FREQUENCY	RESULTING TIME STATE PERIOD	COMMENT
6.250 MHz	320.00 ns	7801 operating rate; fastest allowable rate for 8085A with onboard crystal
6.144 MHz	325.52 ns	7801-1 operating rate; compatible with SBC-type systems and divisible to standard Baud rates
6.000 MHz	333.33 ns	Fastest recommended external user-provided clock signal with crystal removed
1.000 MHz	2000.00 ns	Slowest allowable crystal or external clock signal for 8085A

FIGURE 8 : 7801 Clock Oscillator Frequency Summary

Timing Specifications (Based on 320ns ± 0.05% time states)

An understanding of the 7801's signal timing characteristics is necessary for the selection of speed-compatible memory devices, I/O functions, and other peripheral STD BUS cards, and for real-time logic analysis of 7801-based STD BUS card systems.

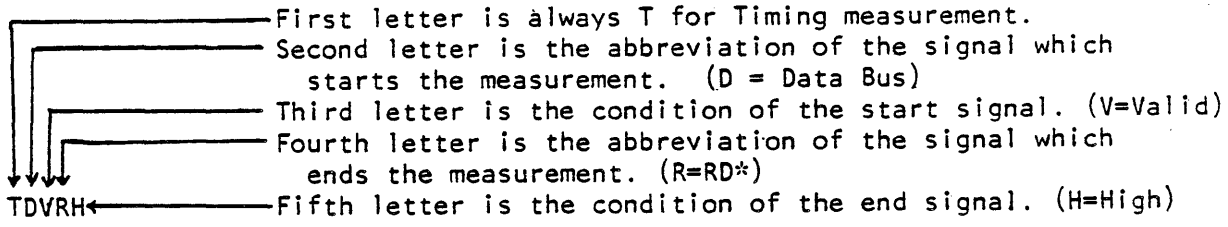
The 7801's timing characteristics are established by its 8085A microprocessor, with additional delays added by LSTTL buffers. The basic operations performed by the 7801 and the signals controlling these operations are shown in Figure 9.

SIGNALS	OPERATION	WAVEFORM
MEMRQ*, RD* A0-A15 ⚠1	Read from memory	Figure 10
MEMRQ*, WR* A0-A15 ⚠1	Write to memory	Figure 11
IORQ*, RD* A0-A7 ⚠1	Read from an input port	Figure 10
IORQ*, WR* A0-A7 ⚠1	Write to an output port	Figure 11
INTAK*	Read an interrupt instruction (in response to INTRQ* only)	Figure 10

FIGURE 9 : BASIC 7801 OPERATIONS

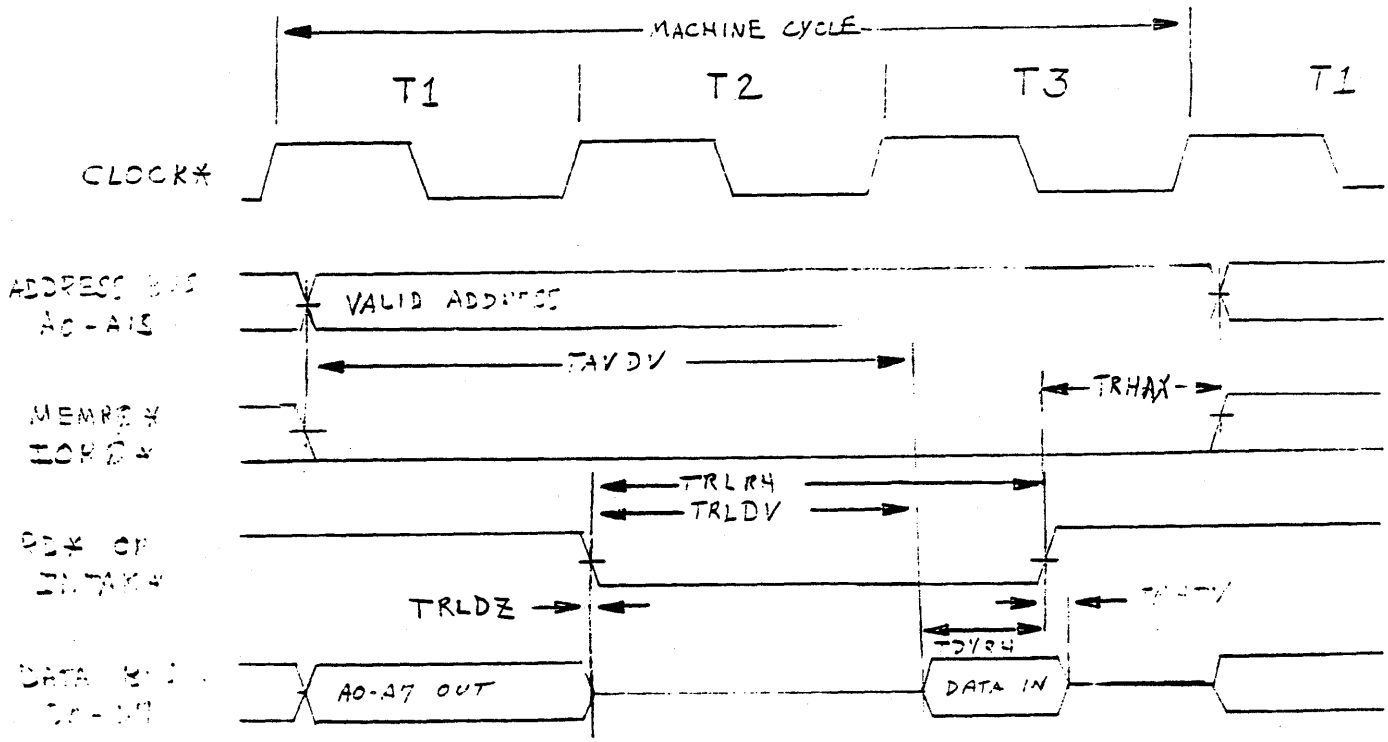
⚠1 Note that the following signals all have identical timing characteristics: ADDRESS BUS A8-A15 MEMRQ*, IORQ*, STATUS 0*, STATUS 1*.

The waveforms on the following pages show timing measurements as a 5-letter code as follows:



For example, TDVRH stands for Time from Data Valid until RD*(READ) High inactive. Specific abbreviations are given in the Legend on each page of the specification.

* Denotes low level active signal

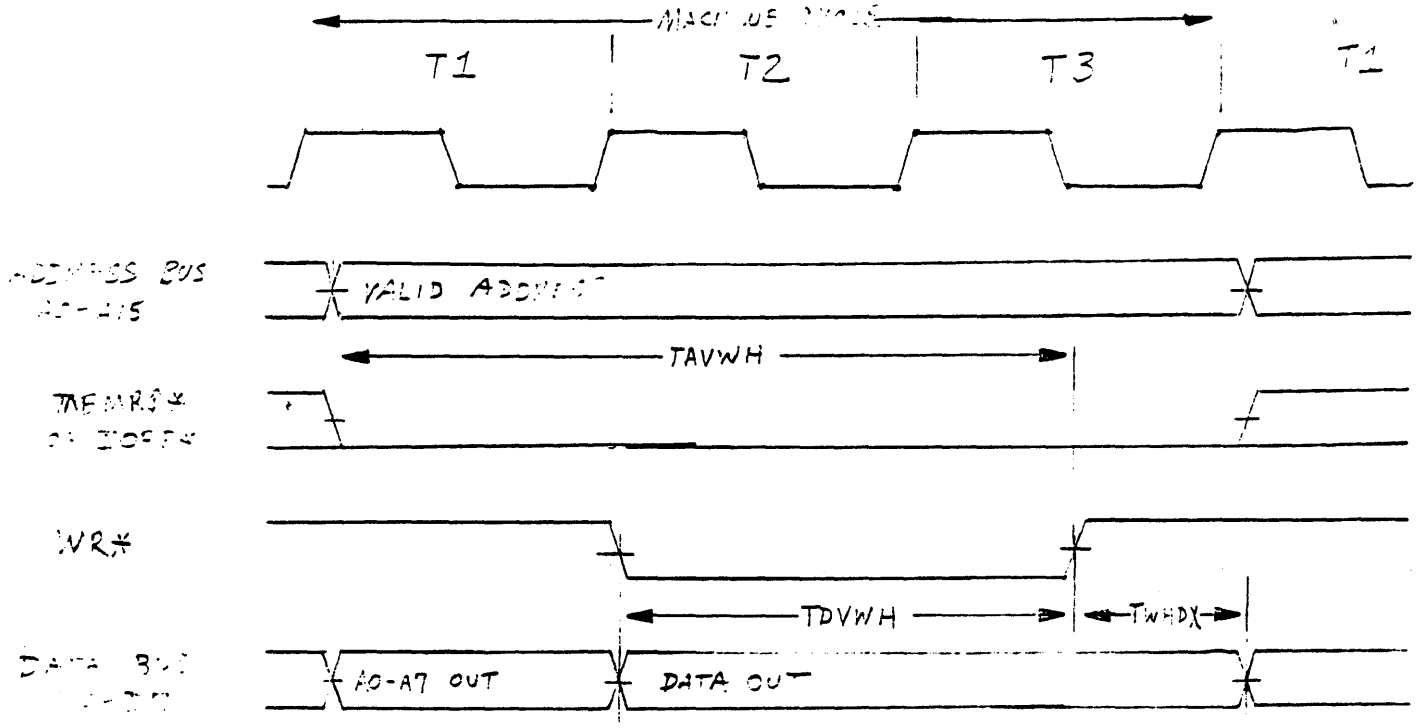


LEGEND	
A	Any Address Line A0-A15 MEMRQ*, IORQ*
D	Any Data line D0-D7
R	RD* line
L	Low state
H	High state
V	Valid
Z	High impedance

SYMBOL	PARAMETER	MIN	MAX	UNITS
TAVDV	Address valid before bus data must be valid		525	ns
TRLDV	RD* active before bus data must be valid		250	ns
TRLRH	RD* pulse width	385		ns
TDVRH	Data setup time	100		ns
TRHDV	Data hold time	0		ns
TRLDZ	Data bus drivers OFF (high impedance read mode) after RD* active		0	ns
TRHAX	Address hold time after RD* inactive	135		ns

FIGURE 10: READ TIMING - MEMORY FETCH, INPUT PORT, INTERRUPT INSTRUCTION

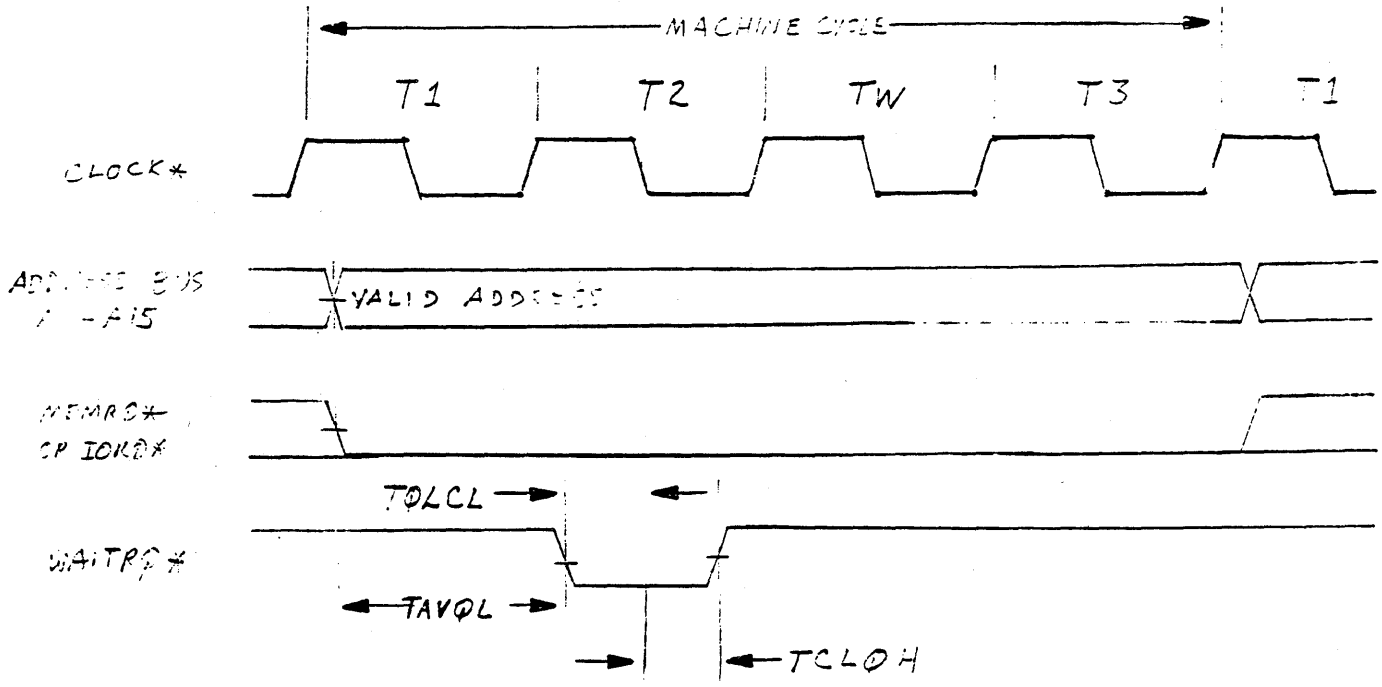
NOTE: In onboard memory read operations (Section 6) the Data Bus does not enter the high impedence read mode; instead the 7801 drives data fetched from the onboard memory sockets onto the Data Bus to facilitate logic state analysis. The access time for onboard memory devices may not exceed the values shown for TAVDV and TRLDV shown above.



LEGEND	
A	Any address Line A0-A15 MEMRQ*, IORQ*
D	Any data line D0-D7
W	WR* line
H	High state
V	Valid
X	Don't care

SYMBOL	PARAMETER	MIN	MAX	UNITS
TAVWH	Address valid before write strobe (WR* rising edge)	625		ns
TDVWH	Data setup time and WR* pulsewidth	400		ns
TWHDX	Data (and address) hold time	85		ns

FIGURE 11 : WRITE TIMING - MEMORY AND OUTPUT PORT



LEGEND	
A	Any address line A0-A15, MEMRQ*, IORQ*
Q	WAITRQ*
C	CLOCK*
L	Low state
H	High state
V	Valid

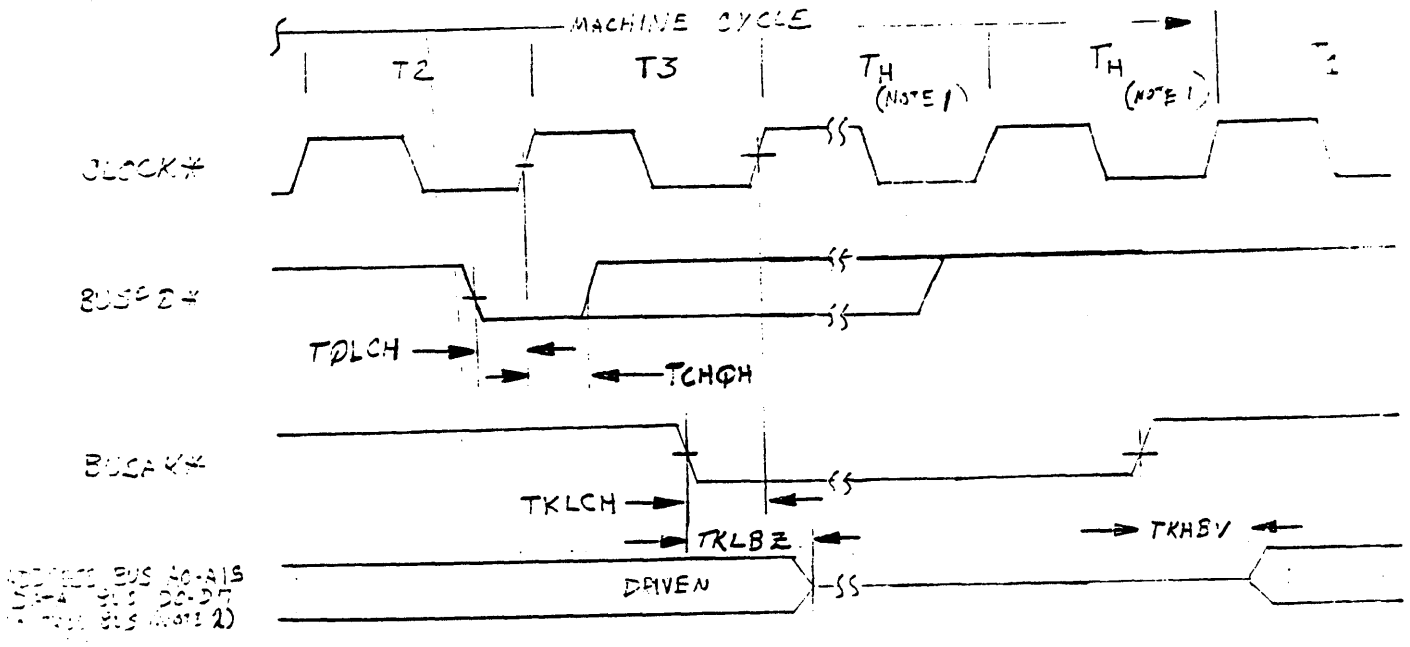
SYMBOL	PARAMETER	MIN	MAX	UNITS
TAVQL	Address valid before WAITRQ* must be active to insert WAIT state in this cycle	185		ns
TQLCL	WAITRQ* setup time prior to clock transition in T2 (for first WAIT state) or in TW.	110		ns
TCLQH	WAITRQ* hold time after clock transition in T2 (for first WAIT state) or in TW.	0		ns

NOTE: MEMRQ* and IORQ* timing is identical to Address Bus timing.

FIGURE 12: WAITRQ* TIMING (One WAIT state shown)

WAIT REQUEST

The WAITRQ* input allows the 7801 to enter the WAIT state in any memory, I/O or interrupt acknowledge cycle while a slow memory device responds, or until a control function such as an analog-to-digital converter finishes. WAITRQ* can also be used to single-step the 7801.



LEGEND	
Q	BUSRQ*
K	BUSAK*
C	CLOCK*
B	Address Bus Data Bus Control Bus
L	Low state
H	High state
Z	High impedance
V	Valid

SYMBOL	PARAMETER	MIN	MAX	UNITS
TQLCH	BUSRQ* active prior to T3 (BUSRQ* setup time)	200		ns
TCHQH	BUSRQ* active after start of T3 (BUSRQ* hold time)	0		ns
TKLCH	BUSAK* asserted prior to TH (Note 1)	125		ns
TKLBZ	Address Bus, Data Bus, and most Control Bus (Note 2) outputs float after BUSAK* is asserted, allowing DMA operations		50	ns
TKHBV	7801 resumes drive on the Address, Data, and Control Busses after BUSAK* goes inactive		50	ns

NOTES:
1. TH time states are clock periods during which the 7801 has relinquished the STD BUS, allowing DMA operations to proceed with an alternate controller card. Equivalent to 8085A Hold mode.
2. The following Control Bus lines are floated when BUSAK* is active: WR*, RD*, IORQ*, MEMRQ*, MCSYNC*, STATUS 1*, STATUS 0*, INTAK*, SYSRESET*, DATA BUS D0-D7, ADDRESS BUS A0-A15.

FIGURE 13 : 7801/STD BUS TIMING FOR DIRECT MEMORY ACCESS (DMA) OPERATIONS

Mechanical

The 7801 meets all STD BUS mechanical specifications. Refer to the Series 7000 Technical Manual for outline dimensions.

If the Interrupt and Serial I/O access socket J1 is used, one additional open card slot on the component side of the 7801 may be needed for ribbon cable access, depending on the connector and cable type used.

Environmental

PARAMETER	MIN	TYP	MAX	UNITS
Free Air Ambient Operating Temperature	0	25	55	°Celsius
Absolute Nonoperating Free Air Ambient Temperature	-40		75	°Celsius
Relative Humidity, Noncondensing	5		95	%
Absolute Nonoperating Relative Humidity, Noncondensing	0		100	%

FIGURE 14: ENVIRONMENTAL SPECIFICATIONS

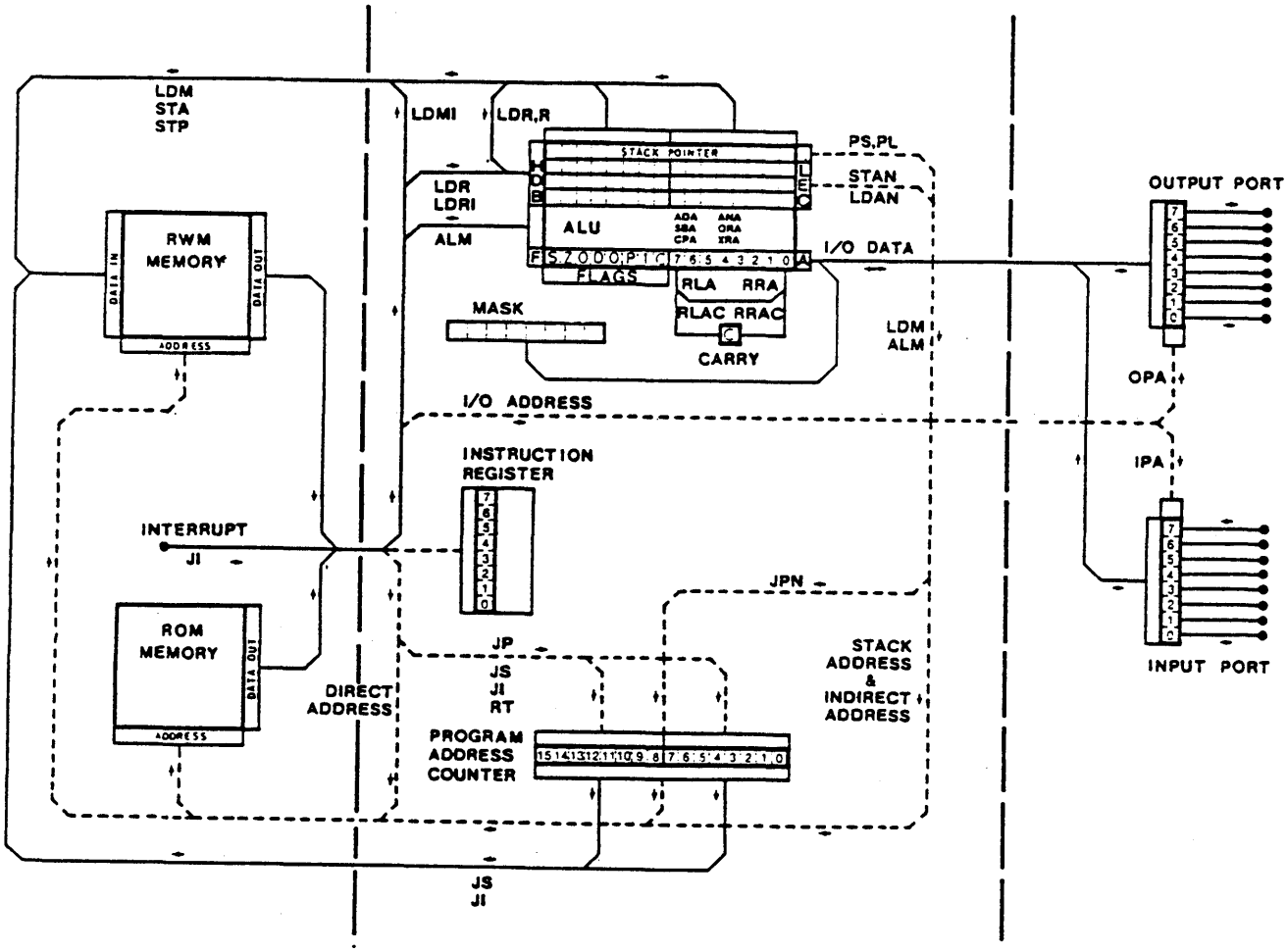


FIGURE 15 : 8085A PROGRAMMING MODEL

Data flow

Memory or Port Address

8085A Architecture

The 8085A processor (figure 15) consists of an 8-bit instruction register, a 16-bit Program Address Counter, a 16-bit Stack Pointer, six 8-bit General Purpose Registers that can be paired to form three 16-bit Register Pairs, and an 8-bit Arithmetic/Logical Unit (ALU) containing an 8-bit Accumulator Register and a 5-bit Flag Register. An 8-bit interrupt register provides serial I/O capability and additional interrupt control.

Instruction Register: The 8-bit Instruction Register provides storage and decoding for instruction operation codes (opcodes) as they are read from program memory.

The second and third words of multiple word instructions bypass the Instruction Register. These provide either data or addressing information and are routed directly to the General Purpose Registers, the Accumulator, or the Program Address Counter as required.

Program Address Counter: The 16-bit Program Address Counter (PC) keeps track of the location of the next instruction to be executed from the program memory. The PC increments automatically for each instruction word; the JUMP and RETURN instructions modify the PC's address content by loading a new address.

Stack Pointer: A 16-bit auto-counting Stack Pointer (SP) provides the address of the subroutine return address stack location in RAM memory. The SP is used for controlling subroutines and interrupts, and can also be used to "push" and "pull" data in memory at high speed.

Subroutine return addresses are automatically stored on the stack when a jump-to-subroutine (JS) instruction is executed, and are retrieved when return (RT) instruction is executed. Interrupts in 8085A systems are generally treated as subroutine jumps.

All of the General Purpose Register Pairs and the Accumulator/Flag Register pair can be stored and fetched from memory using the SP as an indirect address register. 16-bit data movement and address autocounting in the SP result in fast data manipulation.
The address stored in the SP can be brought into the HL Register Pair for arithmetic manipulation with the ADP HL,SP instruction and restored with the LDP HL,SP instruction.

General Purpose Registers: Consists of six 8-bit registers (B,C,D,E,H,L) which can be treated as three 16-bit Register Pairs (BC, DE, HL). Specific instructions regard them as individual registers, while other instructions treat them as pairs. These registers are useful for the temporary storage of 8-bit or 16-bit data, and as pairs can be used as indirect address registers.

Data can be transferred from register to register, register to memory, memory to register, or from the second word of the instruction (8-bit) or second and third words of the instruction (16-bit pair). Individual registers and register pairs can be incremented, decremented, and added. In 16-bit arithmetic, a carry propagates automatically from the lower register to the higher.

The HL register pair forms the indirect memory address for register, arithmetic, and logical operations with any memory location. HL can also be exchanged with pair DE or the top of the stack and loaded to the Stack Pointer and Program Counter (indirect jump). The BC and DE pairs can also be used for indirect addressing with the Accumulator (A) register only.

Arithmetic/Logical Unit (ALU): The Accumulator (Register A) and five status flags (Register F) with associated control logic form the ALU. The ALU provides add and subtract (with or without carry/borrow), and the logical operations AND, OR, Exclusive OR, complement, and shift. Arithmetic/logical operations are performed on the A register using data from the other registers, or from memory, or from the second byte of the instruction (immediate data).

The A register can be decimally adjusted and rotated right or left, with or without the carry bit.

All I/O operations involve the data contained in Register A (unless the system uses memory-mapped I/O).

The Flag Register contains five status flags (see figure 20):

1. Carry/Borrow (C)
2. Zero Result (Z)
3. Sign (S)
4. Parity (P)
5. Decimal half-carry (D)

The C,Z,S,P flags can all be tested by the conditional jump and return instructions for decision-making. The D flag affects the decimal-adjust operation. The C flag is affected by arithmetic, logical, and rotate instructions and has its own set, clear, and complement instructions.

Memory: The 16-bit register pairs, the Stack Pointer, and the Program Counter allow addressing of 64K bytes of memory which can be any combination of ROM and RAM (See Section 6). RAM is required for stack operations to allow the use of subroutines and interrupt. The instruction set allows long direct addressing (16-bit memory address is part of the instruction); immediate (8-bit or 16-bit data is part of the instruction); and indirect (16-bit memory address is contained in one of the register pairs or the Stack Pointer). I/O port addressing is always direct unless I/O is memory-mapped. Figure 21 shows automatic memory allocation for certain instructions.

Interrupt: The 8085A has a single maskable, vectorable interrupt (STD BUS line INTRQ*) and a single nonmaskable, implied vector interrupt (NMIRQ*). Three additional maskable, implied vector interrupts are provided at the 7801's J1 socket. Figure 23 shows the addresses implied by these interrupts, and figure 22 shows how the interrupt mask is programmed for these inputs.

The vectorable INTRQ* input, when acknowledged, causes INTAK* to be asserted. INTAK* is used to read an instruction (supplied by the interrupting device) into the processor via the Data Bus. This may be any 1, 2, or 3-byte instruction; if a multibyte instruction, INTAK* will be asserted one or two more times after the opcode to read in the entire instruction. (The instruction's execution time is unchanged when supplied during interrupt.) The J1 (jump-to-interrupt, or RESTART) instructions are an efficient means of handling up to eight interrupts without polling; see Figure 19B

Inputs and Outputs (I/O): Separate I/O instructions and control signals allow I/O to be mapped separately from memory. The OPA instruction writes data from the Accumulator to the specified output port, and the IPA instruction reads data from the specified input port to the Accumulator. Ports are specified by the second byte of the IPA or OPA instruction, allowing up to 256 each input and output ports. In the 7801, all ports are provided on external cards.

One serial input line and one serial output line are provided at the 7801's J1 interface connector. These lines are operated by the LDA I and LDI A instructions as shown in Figure 22.

8080/8085/Z80 Compatibility

Both the 8085 and the Z80 instruction sets include the 8080's instructions as a subset. Programs written exclusively in 8080 assembly codes will execute normally in the 8085 and the Z80. Note, however, that all three processors require a different number of time states in some instances to execute otherwise identical instructions, and in most systems the processors use different time state clock frequencies. Accordingly, programmed timing (such as count-and-test time delays) will require modification when running an 8080 or Z80 program on an 8085, and vice versa.

Note that only the 8085 instructions which are not part of the 8080 set are the LDA I and LDI A (RIM and SIM) serial I/O and interrupt mask instructions.

8085A vs 8085 Characteristics

The 8085A differs from the 8085 in the following characteristics:

a. ALE (Address Latch Enable; ALE* = MCSYNC* on the 7801)

In the 8085A, ALE is not generated during machine cycles 2 and 3 for the ADP (Add Pair) instruction only (equivalent to Intel mnemonic DAD). This applies only to the ADP instruction.

In addition, ALE does not float during reset, DMA operations, and in WAIT states. Note, however, that MCSYNC* is floated on the STD BUS during DMA operations.

b. INTERRUPTS

The 8085A asserts IORQ* during any interrupt acknowledge machine cycle, while the 8085 asserts MEMRQ*.

In the 8085A, NMIRQ* (nonmaskable interrupt, or Trap) does not destroy the previous interrupt enable status. The LDA I instruction (load accumulator with interrupt mask register, or RIM) must be executed after response to NMIRQ* in order to restore the previous interrupt status.

STD INSTRUCTION MNEMONICS

The STD Instruction Mnemonics are a standard set of processor instruction abbreviations suitable for use as an assembly language for writing programs.

These mnemonics are standard in that they do not change but keep the same meaning regardless of the processor they are applied to. They are also standard in that they are derived from a set of easily understood rules.

The instruction mnemonic is an abbreviated action statement containing an operator, a locator and a qualifier plus a supplemental and separate modifier.

1. The operator is a unique two letter abbreviation that suggests the action.
2. The locator follows the operator and designates the operand or data to be operated on. Instructions without operands ignore the locator.
3. The qualifier states the addressing mode or provides further qualifying information for compound instructions.
4. The modifier carries detailed support information; labels, conditions, addressing and data.

The operator, locator and qualifier letters are strung together to form the instruction mnemonic. The modifier, when needed, stands alone either in its own separate column or separated by spaces or additional lines in written text.

	OPERATOR	LOCATOR	QUALIFIER	MODIFIER	INSTRUCTION DESCRIPTION
RTS	RT	S			Return from Subroutine
CLA	CL	A			Clear A
LDAD	LD	A	D		Load A Direct
LDA B	LD	A		B	Load A with B
LDAN (BC)	LD	A	N	(BC)	Load A indirect using BC as an Address Pointer
JS (LABEL)	JS			(LABEL)	Jump to Subroutine Located at (LABEL)

Figure 1-6 Examples of Instruction Mnemonic Structure

The following table defines all STD mnemonics and contains specific 8085 notation used in the instruction tables, figures 19A and 19B.

STANDARD MNEMONICS DEFINITIONS

OPERATIONS		LOCATORS, MODIFIERS		QUALIFIERS	
LD	LOAD	A	ACCUMULATOR REGISTER	C	WITH CARRY
ST	STORE	B,C,D, E,H,L	GENERAL 8-BIT REGISTERS	D	DIRECT ADDRESSING, DECIMAL
IC	INCREMENT			I	IMMEDIATE ADDRESSING
DC	DECREMENT	F	FLAG REGISTER	N	INDIRECT ADDRESSING
AD (AC)	ADD (WITH CARRY)			T	TOP OF STACK
SU (SC)	SUBTRACT (WITH CARRY)	c	CARRY FLAG		
AN	AND	d	DECIMAL FLAG		
OR	INCLUSIVE OR	z	ZERO FLAG		
XR	EXCLUSIVE OR	s	SIGN FLAG (MSB)		
CP	COMPARE	p	PARITY FLAG		
CL	CLEAR	1.0	STATE OF INDICATED FLAG		
SE	SET				
CM	COMPLEMENT	AF	ACCUMULATOR, FLAGS PAIRED		
AJ	ADJUST (DECIMAL)	BC, DE, HL	GENERAL REGISTER PAIRS (16-BIT DATA, POINTERS)		
RR	ROTATE RIGHT				
RL	ROTATE LEFT	P	ANY REGISTER PAIR		
PS	PUSH VIA STACK	R	ANY SINGLE REGISTER		
PL	PULL VIA STACK	M	MEMORY, ADDRESSED INDIRECTLY		
XC	EXCHANGE	I	INTERRUPTS		
IP	INPUT FROM PORT			**MISCELLANEOUS**	
OP	OUTPUT TO PORT	PC	PROGRAM COUNTER		
EN	ENABLE	SP	STACK POINTER		
DS	DISABLE			UN	UNCONDITIONAL
JP	JUMP	x	REGISTER, IMMEDIATE DATA MODIFIER	NMI	NONMASKABLE INTERRUPT
JS	SUBROUTINE JUMP	xx	REGISTER PAIR MODIFIER	MSB	MOST SIGNIFICANT BIT
JI	JUMP TO INTERRUPT	Cx	JUMP CONDITION		
RTS	RETURN (FROM SUBROUTINE)	Px	I/O PORT ADDRESS (1 byte)		
HLT	HALT	LABEL	MEMORY ADDRESS (2 bytes)		
NOP	NO OPERATION				

Figure 17: STD MNEMONICS

INSTRUCTION CATEGORY		STANDARD MNEMONIC	INTEL MNEMONIC
REGISTER	LRR	LDA,x LDB,x LDC,x LDD,x LDE,x LDH,x LDL,x	MOV,r1,r2
	LRI	LDA,x LDB,x LDC,x LDD,x LDE,x LDH,x LDL,x	MVI,r
	CTR	DC R, ICR	INR,r DCR,r
	STAD LDAD	STAD/LDAD	STA/LDA
MEMORY	LMR	LDM,R LDAN	MOV,M,r STAX,B STAX,D
	LRM	LDA,m LDB,m LDC,m LDD,m LDE,m LDH,m LDL,m STAN	MOV,r,M LDAX,B LDAX,D
	LMI	LDM,x	MVI,M
	CTM	DCM, ICM	INR,M DCR,M
ALU	ALR	ADA,x ACA,x SCA,x ANA,x XRA,x ORA,x CPA,x	ADD,r ADC,r SUB,r SBB,r ANA,r XRA,r ORA,r CMP,r
	ALM		ADD,M ADC,M SUB,M SBB,M ANA,M XRA,M ORA,M CMP,M
	ALI		ADI ACI SUI SBI ANI XRI ORI CPI
	ROT	RLA RRA RLAC RRAC	RLC RRC RAL RAR
	ACC	CLAC CLC CMC CMA SEC AJA	CMC CMA STC DAA
ADDRESS	JP	JP,CX	JMP JC JNC JZ JNZ JP JM JPE JPO
	JS	JS,CX	CALL CC CNC CZ CNZ CP CM CPE CPO
	RTS	RTS,CX	RET RC RNC RC RNZ RP RM RPE RPO
	JI	JI,xx	RST
REGISTER PAIR	LPI	LDPI	LXI,B LXI,D LXI,H LXI,SP JMP
	PSP	PSP	PUSH,B PUSH,D POP,H PUSH, PSW
	PLP	PLP	POP,B POP,D POP,H POP,PSW
	XDH	XCP DE,HL	XCHG
	XTH	XCPT HL	XTHL
	CTP	INCP,xx ICP DECP,xx DCP	INX,B INX,D INX,H INX,SP DEX,B DEX,D DEX,H DEX,SP
	SHD/LHD	SHLD/LHLD STPD HL LDPD HL	SHLD/LHLD
	JPN	LDP SPIHL JPN	SPHL PCHL
	ADP	ADP HL	DAD,B DAD,D DAD,H DAD,SP
I/O	IPA	IPA	INP
	OPA	OPA	OUT
MACHINE	INT	ENI, DSI	EI DI
	NOP	NOP	NOP
	HLT	HLT	HLT
	LDA I	LDA I	RIM
	LDI A	LDI A	SIM

Figure 18 Instruction Mnemonic and Category Cross-Reference

THE 8085A INSTRUCTION SET

Figures 19A and 19B present the 8085/8085A instruction set with STD mnemonics and functionally grouped by: Register, Memory, Program Address Control, Machine, Register Pair, Input/Output and Restart instructions.

The flag status nomenclature is as follows: Lower case letters are variable, upper case followed by 0 or 1 indicate absolute condition. Only the affected flags are tabulated.

The information presented in figures 19-22 is available from Pro-Log as a shirt pocket programming aid card, document #102967.

REGISTER AND MEMORY INSTRUCTIONS

INSTRUCTION MNEMONIC										IMMEDIATE 2 BYTES	FLAG STATUS	DESCRIPTION OF OPERATION
							MEMORY					
		REGISTER							(H,L)			
INSTR	MOD	A	B	C	D	E	H	L	M			
LDA	x	7F	78	79	7A	7B	7C	7D	7E	3E		Load with register x
LDB	x	47	40	41	42	43	44	45	46	06		
LDC	x	4F	48	49	4A	4B	4C	4D	4E	0E		
LDD	x	57	50	51	52	53	54	55	56	16		
LDE	x	5F	58	59	5A	5B	5C	5D	5E	1E		
LDH	x	67	60	61	62	63	64	65	66	26		
LDL	x	6F	68	69	6A	6B	6C	6D	6E	2E		
LDMI	(HL)									36		Load memory immediate
STxN	(HL)	77	70	71	72	73	74	75				Store register x indirect
ICx		3C	04	0C	14	1C	24	2C	34		d,z,s,p	Increment register x
DCx		3D	05	0D	15	1D	25	2D	35		d,z,s,p	Decrement register x
ADA	x	87	80	81	82	83	84	85	86	C6	c,d,z,s,p	Add to A
ACA	x	8F	88	89	8A	8B	8C	8D	8E	CE	c,d,z,s,p	Add to A W/C
SUA	x	97	90	91	92	93	94	95	96	D6	c,d,z,s,p	Sub from A
SCA	x	9F	98	99	9A	9B	9C	9D	9E	DE	c,d,z,s,p	Sub from A W/C
ANA	x	A7	A0	A1	A2	A3	A4	A5	A6	E6	C0,D1,z,s,p	And with A
XRA	x	AF	A8	A9	AA	AB	AC	AD	AE	EE	C0,D0,z,s,p	Exclusive or with A
ORA	x	B7	B0	B1	B2	B3	B4	B5	B6	F6	C0,D0,z,s,p	Or with A
CPA	x	BF	B8	B9	BA	BB	BC	BD	BE	FE	c,d,z,s,p	Compare with A
CLAC		AF	0→C 0→A								C0,D0,Z1,S0,P1	Clear A and carry
CLC		B7	0→C								C0,D0,z,s,p	Clear carry
CMC		3F	C→C								c	Complement carry
CMA		2F	A→A									Complement A
SEC		37	1→C								C1	Set carry
AJAD		27	C ?, D = ?								c,d,z,s,p	Adjust A Decimally
RRA		0F	A0→C A0→A7								c	Rotate A right
RLA		07	A7→C A7→A0								c	Rotate A left
RRAC		1F	A0→C→A7								c	Rotate A right W/C
RLAC		17	A7→C→A0								c	Rotate A left W/C
STAD		32	A→M									Store A direct
LDAD		3A	M→A				3 Bytes					Load A direct

3 Byte Instructions: Byte 2 = Lower Order Address (Line) or data bits 0-7
Byte 3 = Higher Order Address (Page) or data bits 8-15

Figure 19A: 8085A INSTRUCTIONS

REGISTER PAIR OPERATIONS

		AF	BC	DE	HL	SP	FLAG STATUS	
ICP	xx		03	13	23	33		Increment Pair
DCP	xx		0B	1B	2B	3B		Decrement Pair
STAN	xx		02	12	77			Store A Indirect
LDAN	xx		0A	1A	7E			Load A Indirect
ADP	HL,xx		09	19	29	39	c	Add to Pair HL
PSP	xx	F5	C5	D5	E5			Push Pair ⟶(SP)
PLP	xx	F1	C1	D1	E1		(AF: c,d,z,s,p)	Pull Pair ⟵(SP)
STPD	HL				22			Store HL Direct } 3 BYTE INSTR.
LDPD	HL				2A			Load HL Direct } 3 BYTE INSTR.
LDPI	xx		01	11	21	31		Load Pair Immediate } 3 BYTE INSTR.
XCPT	HL				E3			Exchange Top & HL
XCP	HL,DE,			EB				Exchange Pair DE⟷HL
LDP	SP,HL				F9			Load SP with HL

PROGRAM ADDRESS CONTROL INSTRUCTIONS

INSTRUCTION MNEMONIC		FLAG CONDITIONS, Cx									DESCRIPTION OF OPERATION
			≥	≠	+	ODD	<	=	—	EVEN	ARITHMETIC
INSTR	MODIFIER	UN	C0	Z0	S0	P0	C1	Z1	S1	P1	LOGICAL
	Cx	C3	D2	C2	F2	E2	DA	CA	FA	EA	Jump on Condition
	Cx	CD	D4	C4	F4	E4	DC	CC	FC	EC	Jump to Subroutine
RTS	Cx	C9	D0	C0	F0	E0	D8	C8	F8	E8	Return from Subroutine
JPN	(HL)	E9									Jump Indirect

3 bite instruction

JUMP TO INTERRUPT

		NMI	5.5	6.5	7.5	INTERRUPT
		24	2C	34	3C	RESTART AT SPECIFIED ADDRESS IN PAGE 00

INSTR	MODIFIER	00	08	10	18	20	28	30	38	RESTART ADDRESS IN PAGE 00
JI	XX	C7	CF	D7	DF	E7	EF	F7	FF	RESTART AT SPECIFIED ADDRESS

INTERRUPT AND SERIAL I/O INSTRUCTIONS

ENI		FB	Enable Interrupt
DSI		F3	Disable Interrupt (Reset Condition)
LDA	I	20	Load A with Interrupt Mask and Serial Input
LDI	A	30	Load Interrupt Mask, Write Serial Output from Accumulator

INPUT OUTPUT INSTRUCTIONS

IPA	Px	DB	The Second Byte Px is a 2 digit hex port address	Input from Px to ACC	2 BYTE INSTR.
OPA	Px	D3		Output from ACC to Px	2 BYTE INSTR.

MACHINE INSTRUCTIONS

NOP		00	7F 40 49 52 5B 64 6D	No operation
HLT		76		Halt

Figure 19B: 8085 INSTRUCTIONS

S - SIGN
Z - ZERO
D - DECIMAL (half carry)
P - PARITY
C - CARRY

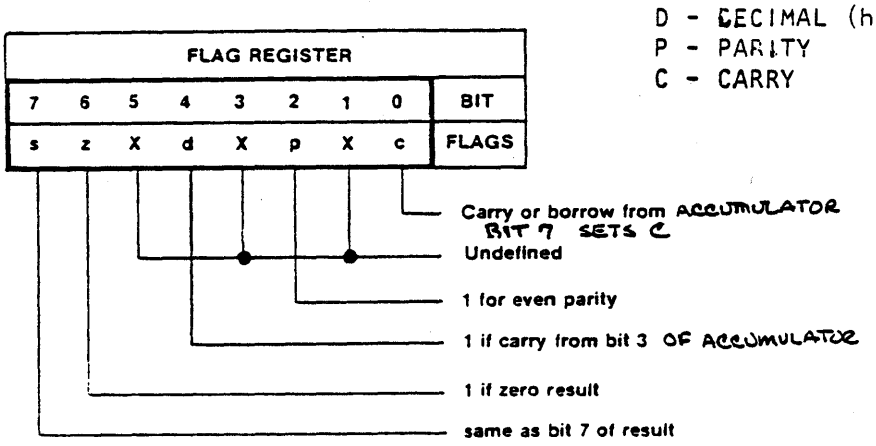


FIGURE 20 : FLAG BIT ALLOCATION IN REGISTER F

AUTOMATIC MEMORY OPERATIONS	
PSP,JS,JI:	Page at (SP-1) Line at (SP-2)
PLP,RTS:	Line from (SP) Page from (SP + 1)
XCPT HL:	(L) ⟷ (SP) (H) ⟷ (SP + 1)
LDPD HL STPD HL	(L) ⟷ (ADR) (H) ⟷ (ADR + 1)

FIGURE 21 : AUTOMATIC MEMORY ALLOCATION BY INSTRUCTION

NOTE: This table shows how memory is allocated automatically by the processor when certain instructions are executed. For example, the PLP instruction pulls a line address or low-order register (C, E, F, or L); increments the SP, then pulls a page address or high-order register (A, B, D, or H); and increments the SP again, leaving the SP two counts higher than its initial value.

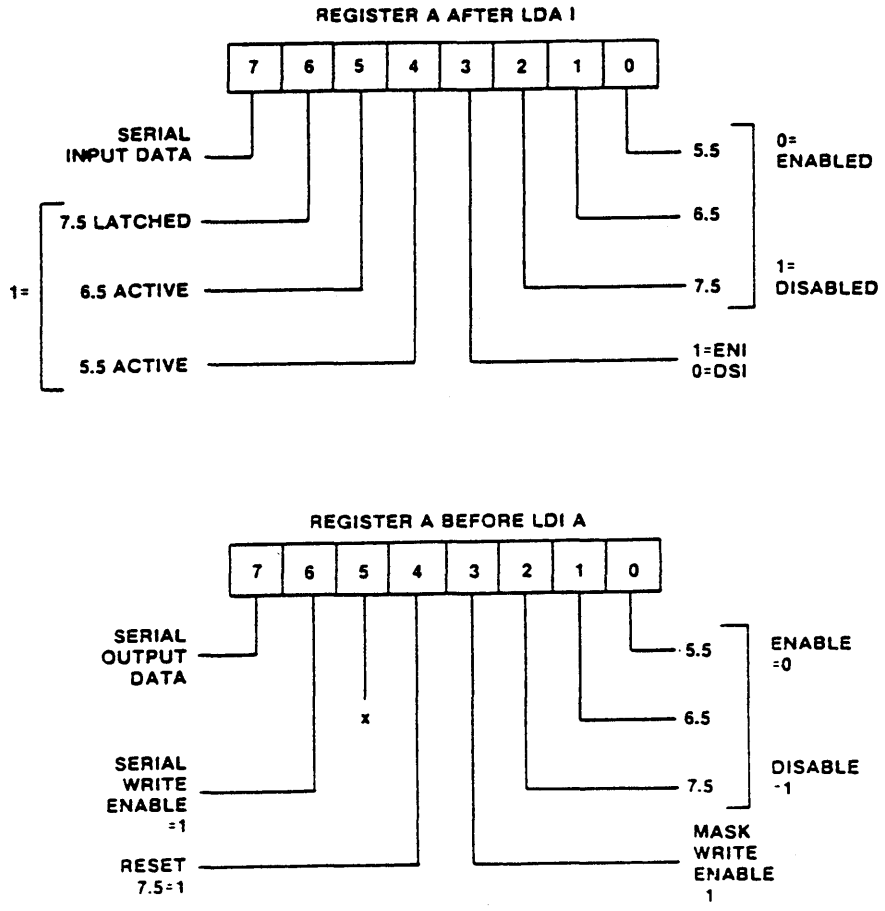


FIGURE 22 : BIT FUNCTIONS OF THE LDA I AND LDI A INSTRUCTIONS

Interrupts

The 7801 has five interrupt request inputs, with two (NMIRQ* and INTRQ*) available at the STD BUS backplane, and three (INTR 5.5*, INTR 6.5*, and INTR 7.5*) at Serial I/O and Interrupt Connector J1 located near the card ejector.

The various interrupt inputs have different characteristics as summarized in Figure 23.

INTERRUPT NAME	INPUT SENSITIVITY	PRIORITY	PROCESSOR ACTION UPON RESPONSE	GENERATES INTAK*?	8080/Z80 COMPATIBLE?	MASKABLE?
NMIRQ*	Falling edge and low level	Highest	Restart at hex address 0024	no	no	no
INTR 7.5*	Falling edge	Second	Restart at hex address 003C	no	no	yes
INTR 6.5*	Low level	Third	Restart at hex address 0034	no	no	yes
INTR 5.5*	Low level	Fourth	Restart at hex address 002C	no	no	yes
INTRQ*	Low level	Lowest	Read 1 to 3-byte instruction from Data Bus	yes - 1 to 3 pulses	yes	yes

Figure 23: Interrupt Summary

NMIRQ* (STD BUS pin 46) is nonmaskable and cannot be disabled by the program. Its input characteristics require that it fall low, then remain low, to be recognized. It cannot be recognized a second time until after the first response, and then being returned high, and then again dropped and held low. NMIRQ* is often used for catastrophic system events, such as impending power failure, but may be used for any interrupt function.

INTR 7.5* (J1 pin 1) drives an edge-sensitive latch in the 8085A. Register I bit 4 resets this latch with the LDI A instruction (Figure 22).

INTR 7.5*, INTR 6.5* (J1 pin 2), and INTR 5.5* (J1 pin 3) are monitored and masked by the I Register. Bits 4,5,6 allow the program to monitor activity at the request pins, regardless of whether the interrupts are enabled (Figure 22); and bits bits 0,1,2 allow the program to read the mask using LDA I to see which interrupts are enabled. Bits 0,1,2 are also used to set or clear the three mask bits using the LDI A instruction to disable/enable these three interrupts (Note that bit 3 must be high in order to write into the interrupt mask).

INTRQ* (STD BUS pin 44) is identical to the 8080's interrupt system. INTRQ* is a maskable interrupt and is enabled/disabled with the ENI and DSI instructions. I Register bit 3, when read with the LDA I instruction, shows whether the interrupt system is currently enabled or disabled (Figure 22).

When the 7801 responds to INTRQ*, it asserts INTAK* (interrupt acknowledge). This signal is used by the interrupting device as a read-memory strobe; the interrupting device responds by placing an instruction opcode onto the STD Data Bus during INTAK*

* low level active.

If it is desired to vector the program to an interrupt service routine (as is usually the case), the instruction inserted during INTAK* is generally either one of the JI (Jump-to-Interrupt, or RESTART) instructions, or one of the JS (Jump-to-Subroutine) instructions shown in Figure 19B. These instructions store the return-from-interrupt address on the Stack via the Stack Pointer, and allow the interrupt routine to exit back to the interrupted program using the RTS instructions. Alternately, any instruction in the instruction set can be executed out of sequence in the interrupt ackowledge cycle identified by INTAK*.

Note that any 1, 2, or 3-byte instruction can be executed at interrupt. The 8085A determines, after decoding the opcode read in by the first INTAK*, whether a multibyte instruction requiring one or two more INTAK* cucles is being executed.

The 8085A automatically disables the interrupt system when acknowledging INTRQ*, thereby eliminating any critical timing for the INTRQ* signal. Simply wait until INTRQ* is inactive before executing the ENI instruction, and multiple responses to the same INTRQ* signal cannot occur (an input port bit or the Serial Input -JI pin 5 can be used to monitor INTRQ*).

INTAK* (STD BUS pin 43) is active only in response to INTRQ* as noted above. However, the coincidence of status signals shown in Figure 4 can be detected outside the 7801 when needed to note the processor's response to any of the other interrupts. This function is seldom necessary since NMIRQ* and the INTR 7.5,6.5, and 5.5 are all implied vector interrupts, while INTRQ* is a supplied vector interrupt requiring INTAK* to control the information exchange between the 7801 and the interrupting device.

Pro Log's 7320 Priority Interrupt Controller may be used to expand any of the 7801's five interrupt inputs regardless of edge or level sensitivity. Each 7320 card expands the interrupt line by a factor of eight and provides additional program control over the interrupt system while handling expansion signal protocol.

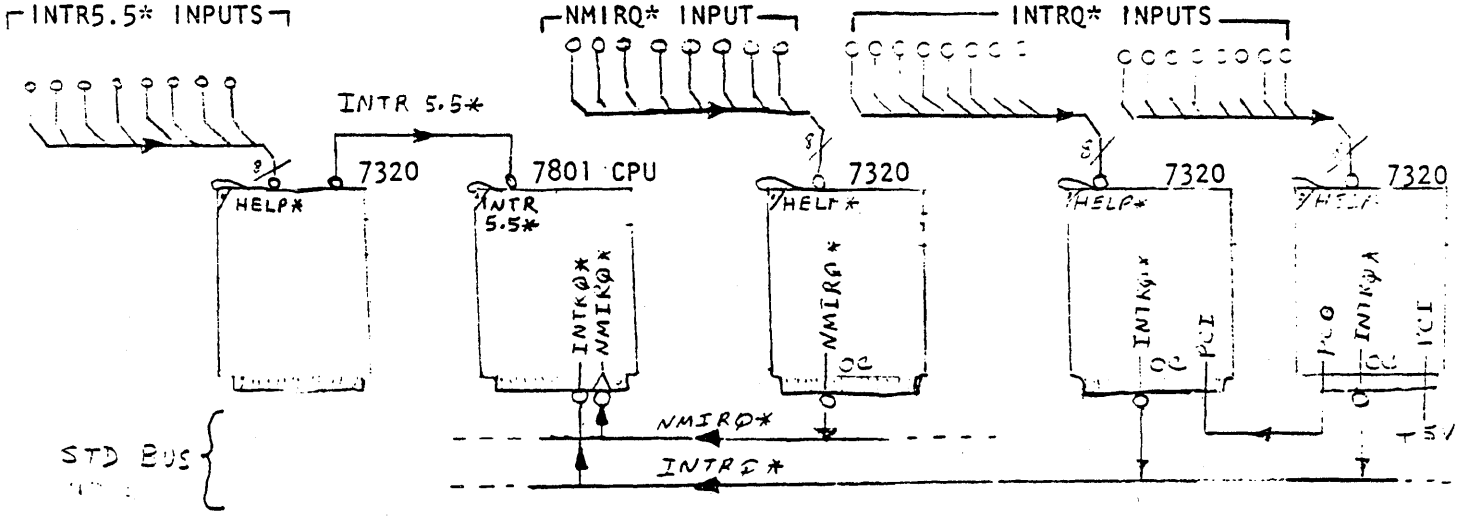


FIGURE 24: EXAMPLE OF 7801 INTERRUPT INPUTS EXPANDED WITH FOUR 7320 CARDS

Note: Address and data busses omitted. OC - open collector * low level active

SECTION 5 - PROGRAM INSTRUCTION TIMING

Introduction

The execution of a program instruction is a sequential process. The time state clock (Section 3) is used to step the 8085A through a specific sequence for each instruction type. The execution time for each instruction is the total of the time states needed by the instruction, with the time state period set by the processor's clock oscillator.

An understanding of the 8085A's instruction execution timing is important in real time programming, where the program's execution rate is precisely matched to the speed requirements of the application. When using a signal or logic state analyzer, a knowledge of the time state sequence makes it possible to predict the data and control states present on the STD BUS backplane and at the 8085A chip pins at any given instant in the execution of a program (Figure 34).

Machine Cycles

Each transaction between the 8085A and its memory and I/O ports requires a distinct time period called a machine cycle. In the 8085A, machine cycles are composed of 3 to 6 time states, with specific activity occurring in each time state. Although the number of time states and machine cycles vary among different types of instructions, they are precisely predictable for any given instruction. (Figure 27)

Figure 25 is a timing diagram for the STAD (STore Accumulator Direct) instruction. This instruction requires four machine cycles (M1 through M4) with a total of 13 time states. Four machine cycles are necessary because the instruction accesses memory four times.

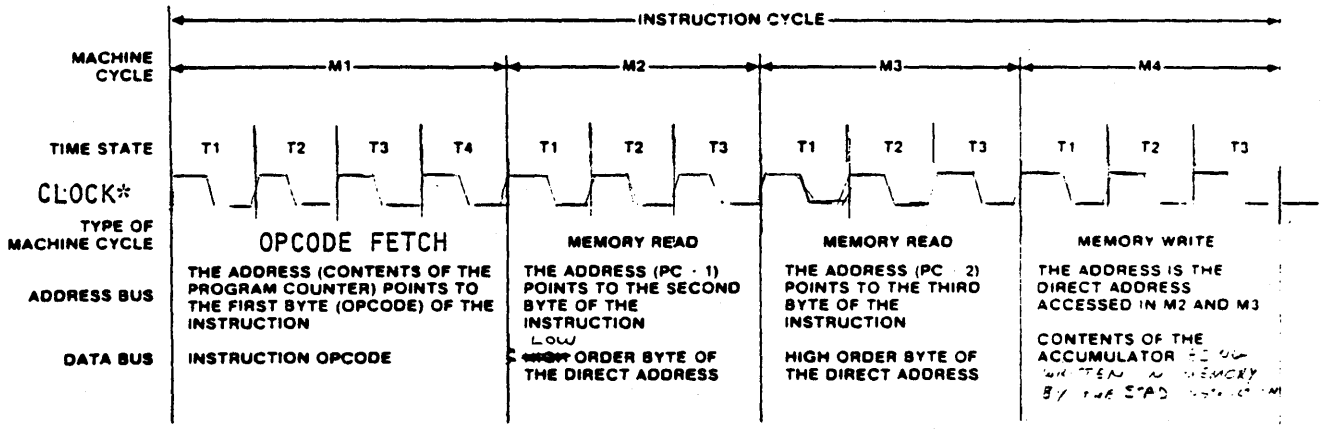


FIGURE 25: TIMING FOR STAD INSTRUCTION (STORE ACCUMULATOR DIRECT)

The first machine cycle in the instruction (M1 in Figure 25) is always used to read the instruction's operation code (opcode) from the program area of memory. M1 is called the opcode fetch cycle and is used by the 8085A to decode the instruction and prepare itself for the operation specified. The opcode fetch cycle always requires a minimum of four time states (T1, T2, T3, T4), although some instructions stretch M1 by adding T5 and T6 to gain additional time.

Certain instructions execute fully during the opcode fetch cycle. Other instructions require additional machine cycles (up to M5) to execute. When the 8085A decodes the opcode during M1, it will add additional machine cycles if it finds that:

a. The instruction is composed of more than one byte, with 1 or 2 bytes of data, memory address, or I/O port address appended to the opcode; or

b. The instruction requires the processor to access memory or an I/O port as part of the function performed by the instruction.

Either condition results in additional machine cycles, with each subsequent machine cycle following M1 composed of only three time states.

For example, the STAD instruction in Figure 25 is a 3-byte instruction (opcode plus 16-bit address contained in the next two bytes following the opcode), and the instruction is one which stores one byte in memory. Therefore STAD requires 4 machine cycles with M1, M2, M3 used to read the 3-byte instruction and M4 used to perform the operation.

WAIT States

Although the number of time states in any given machine cycle is fixed, the user can insert one or more WAIT states in the cycle. WAIT states are added by driving the 7801's WAITRQ* line active during the T2 time state in the machine cycle (see Section 3 for precise timing requirements for WAITRQ*). The WAIT state is a do-nothing time period that can be used to interface slow memories to the 7801, or to cause the processor to pause while a slow system function (such as an analog-to-digital converter or arithmetic processor) completes its task. The effect of holding WAITRQ* active indefinitely is to halt the processor; when WAITRQ* is released, the processor resumes operation with no change in its internal data or control states.

DMA Mode (8085A HOLD Mode)

Direct Memory Access (DMA) operations are controlled by driving the 7801's BUSRQ* line active when sampled at the end of the T2 time state. This causes the 7801 to relinquish the STD Data and Address Busses, and many of the Control Bus lines (see Section 2 for signal functionality and Section 3 for precise BUSRQ*/BUSAK* signal timing). The BUSAK* signal is used to signify that the 7801's 3-state bus drivers are in the OFF condition, allowing an alternate system controller to operate the memory, I/O, and other peripheral cards external to the 7801 on the same mother-board. Once in DMA mode, the 8085A itself halts in a manner similar to the WAIT state with its internal data and control states protected for restoration when BUSRQ* is removed. Like WAITRQ*, BUSRQ* can be held active indefinitely.

Sequential Time State Operations

The table in Figure 26 shows function of the time state within a machine cycle. This table is a summary only, with the precise timing needed to interface memory device, ports, WAIT state circuitry, and DMA circuitry given in Section 3.

TIME STATE	MACHINE CYCLE EVENTS
T1	a. Upper address lines (A8-A15, or memory page address) stable shortly after the start of T1. b. MEMRQ* or IORQ* and STATUS 0*, STATUS 1* stable shortly after the start of T1; SAME TIMING AS A8-A15. c. Lower address lines (A0-A7, memory line or I/O port address) stable prior to the end of T1. d. MCSYNC* (ALE*) issued during the first half of T1
T2	a. RD* or WR* signal active shortly after the start of T2. b. In memory or output port write operations, output data is stable on the Data Bus shortly after the start of T2. c. WAITRQ* line is sampled at the midpoint of T2. d. BUSRQ* line is sampled at the end of T2.
TW	If the WAITRQ* line was active when sampled in T2, processor enters the WAIT state instead of T3. If WAITRQ* was inactive, TW does not exist and the processor goes directly to T3.
T3	a. In memory or input port read operations, the processor reads the Data Bus at the lagging (rising) edge of the RD* line during the second half of T3. b. In memory or output port write operations, the memory or port device latches the data on the Data Bus at the lagging (rising) edge of WR* in the second half of T3. c. If BUSRQ* was active when sampled during T2, the processor issues BUSAK* and allows DMA operations at the end of T3.
T4, T5, T6	These time states only occur in the opcode fetch cycle M1. The processor uses them for internal operations and no new data or control states appear externally to the 8085A for logic analysis. Not all M1 cycles use time states T5 and T6. Note that if present, T4, T5, and T6 continue to execute internally in the 8085A even when the processor issues BUSAK* and enters DMA mode at the end of T3.

FIGURE 26: SUMMARY OF 8085A TIME STATE OPERATIONS

Instruction Timing Table

The table in Figure 27 shows the actual number of memory bytes, machine cycles and time states required for all of the 8085A instruction set. Three time state periods are included for convenience with the full execution time of the instructions shown for the three different time state periods. The time state periods shown are:

a. 320 ns: 7801 state time, the fastest allowed for the 8085A

b. 325.5 ns: 7801-1 and SBC-type state time

c. 488 ns: Included for comparison with Pro Log's older 8080-based systems (note: some 8085A instructions execute with fewer time states, others with more time states than 8080-identical instruction functions).

Figure 27 uses the concept of Instruction Categories, where similar instruction types are grouped without regard to specific instruction mnemonics. For example, the 49 load-register-with-register instructions (LDA A, LDA B, LDA C...) all have identical timing and are grouped together as the LRR group.

Figure 28 is included to support Figure 27. It shows how the Instruction Categories are formed using both Pro Log's STD instruction mnemonics and the equivalent Intel mnemonics for the 8085A.

INSTRUCTION TIMING

FUNCTION	N=NUMBER OF TIME STATES PER INSTRUCTION	NUMBER OF MACHINE CYCLES	NUMBER OF INSTRUCTION WORDS	INSTRUCTION CATEGORY		N	T=EXECUTION TIMES STATE TIME 0.488μs	STATE TIME 0.320μs	STATE TIME 0.3255us
REGISTER	1	1	LRR	Load Register with Register		4	1.95	1.28	1.30
	2	2	LRI	Load Register Immediate		7	3.42	2.24	2.29
	1	1	CTR	Count Register (Increment or Decrement)		4	1.95	1.28	1.30
	4	3	STAD LDAD	Register A (Accumulator) Store/Load Direct		13	6.34	4.16	4.23
MEMORY	2	1	LMR	Load Memory with Register		7	3.42	2.24	2.28
	2	1	SRM	Store Register in Memory		7	3.42	2.24	2.28
	3	2	LMI	Load Memory Immediate		10	4.88	3.20	3.26
	3	1	CTM	Count Memory		10	4.88	3.20	3.36
ALU	1	1	ALR	Arithmetic or Logical from Register		4	1.95	1.28	1.30
	2	1	ALM	Arithmetic or Logical from Memory		7	3.42	2.24	2.28
	2	2	ALI	Arithmetic or Logical Immediate		7	3.42	2.24	2.28
	1	1	ROT	Rotate Register A		4	1.95	1.28	1.30
	1	1	ACC	Accumulator/Carry Control		4	1.95	1.28	1.30
ADDRESS	3	3	JP	Unconditional Jump		10	4.88	3.20	3.26
	2			Jump On Flag Condition	No Jump	7	3.42	2.24	2.28
	3				Jumps	10	4.88	3.20	3.26
	5	3	JS	Unconditional Subroutine Jump		18	8.78	5.76	5.86
	2			Jump to Subroutine On Flag Condition	No Jump	9	4.39	2.88	2.93
	5				Jumps	18	8.78	5.76	5.86
	3	1	RTS	Unconditional Subroutine Return		10	4.88	3.20	3.26
	1			Subroutine Return On Flag Condition	No Return	6	2.92	1.92	1.95
	3				Returns	12	5.85	3.84	3.91
	3	1	JI	Jump to Interrupt		12	5.85	3.84	3.91
REGISTER PAIR	3	3	LPI	Load Pair Immediate		10	4.88	3.20	3.26
	3	1	PSP	Push Pair on Stack		12	5.85	3.84	3.91
	3	1	PLP	Pull Pair from Stack		10	4.88	3.20	3.26
	1	1	XCP	Exchange D&E with H&L		4	1.95	1.28	1.30
	5	1	XCPT	Exchange Top of Stack with H&L		16	7.81	5.12	5.21
	1	1	CTP	Increment, Decrement Pair (Count)		6	2.92	1.92	1.95
	5	3	HLD	Store/Load H&L Direct		16	7.81	5.12	5.21
	1	1	JPN/ LDP	Jump Indirect/Load SP with HL		6	2.92	1.92	1.95
	3	1	ADP	Add Pair to H&L		10	4.88	3.20	3.26
I/O	3	2	IPA	Read Input Port		10	4.88	3.20	3.26
	3	2	OPA	Write Output Port		10	4.88	3.20	3.26
MACHINE	1	1	INT	Interrupt Enable/Disable		4	1.95	1.28	1.30
	1	1		Read Interrupt Masks and Serial In		4	1.95	1.28	1.30
	1	1		Set Interrupt Masks and Serial Out		4	1.95	1.28	1.30
	1	1	HLT	Halt		5	2.440	1.60	1.63
	1	1	NOP	No Operation (00 only)		4	1.95	1.28	1.30

INSTRUCTION TIMING CALCULATIONS

T = Nt, Where
T = Execution Time
N = Number of time states
t = Time State Time

FIGURE 27: 7801/8085A INSTRUCTION TIMING TABLE

INSTRUCTION CATEGORY		PRO-LOG MNEMONIC	INTEL MNEMONIC
REGISTER	LRR	LDA,x LDB,x LDC,x LDD,x LDE,x LDH,x LDL,x	MOV,r1,r2
	LRI	LDA,x LDB,x LDC,x LDD,x LDE,x LDH,x LDL,x	MVI,r
	CTR	DC R, ICR	INR,r DCR,r
	STAD LDAD	STAD/LDAD	STA/LDA
MEMORY	LMR	LDM,R LDAN	MOV,M,r STAX,B STAX,D
	LRM	LDA,m LDB,m LDC,m LDD,m LDE,m LDH,m LDL,m STAN	MOV,r,M LDAX,B LDAX,D
	LMI	LDM,x	MVI,M
	CTM	DCM, ICM	INR,M DCR,M
ALU	ALR	ADA,x ACA,x SCA,x ANA,x XRA,x ORA,x CPA,x	ADD,r ADC,r SUB,r SBB,r ANA,r XRA,r ORA,r CMP,r
	ALM		ADD,M ADC,M SUB,M SBB,M ANA,M XRA,M ORA,M CMP,M
	ALI		ADI ACI SUI SBI ANI XRI ORI CPI
	ROT	RLA RRA RLAC RRAC	RLC RRC RAL RAR
	ACC	CLAC CLC CMC CMA SEC AJA	CMC CMA STC DAA
ADDRESS	JP	JP,CX	JMP JC JNC JZ JNZ . JP JM JPE JPO
	JS	JS,CX	CALL CC CNC CZ CNZ CP CM CPE CPO
	RTS	RTS,CX	RET RC RNC RC RNZ RP RM RPE RPO
	JI	JI,xx	RST
REGISTER PAIR	LPI	LDPI	LXI,B LXI,D LXI,H LXI,SP JMP
	PSP	PSP	PUSH,B PUSH,D POP,H PUSH, PSW
	PLP	PLP	POP,B POP,D POP,H POP,PSW
	XDH	XCP DE,HL	XCHG
	XTH	XCPT HL	XTHL
	CTP	INCP,xx ICP DECP,xx DCP	INX,B INX,D INX,H INX,SP DEX,B DEX,D DEX,H DEX,SP
	SHD/LHD	SHLD/LHLD STPD HL LDPD HL	SHLD/LHLD
	JPN	LDP SPIHL JPN	SPHL PCHL
	ADP	ADP HL	DAD,B DAD,D DAD,H DAD,SP
I/O	IPA	IPA	INP
	OPA	OPA	OUT
MACHINE	INT	ENI, DSI	EI DI
	NOP	NOP	NOP
	HLT	HLT	HLT
	LDAI	LDA I	RIM
	LDI A	LDI A	SIM

FIGURE 28 : INSTRUCTION CATEGORY AND MNEMONIC CROSS-REFERENCE TABLE

Instruction Timing Example

The execution time for any routine or program segment is found by totalling all of the time states in all of the instructions executed. The factors affecting the execution time of a program segment are:

a. The clock frequency, which determines the time state period (Section 3).

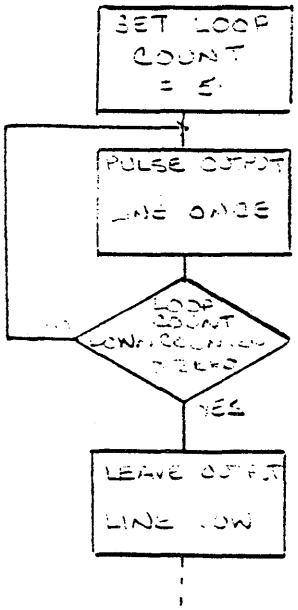
b. The specific instructions used, which determines the number of time states in the segment (Figure 27).

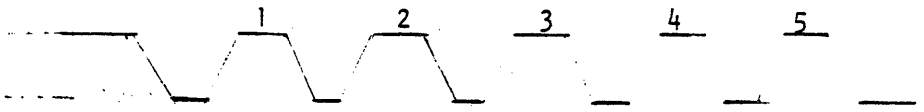
c. The instantaneous Flag (Register F) bit states which summarize processor conditions when the conditional instructions (jump, jump-to-subroutine, return-from-subroutine) are executed (Figure 20).

d. The number of instruction loops within the instruction sequence, and the number of times each loop is executed (loop iterations).

e. If the program segment has more than one entrance or exit, every combination of routes through the segment that are used by the program should be considered.

The following example shows how to compute execution times in a program segment. The 8085A is programmed to generate a series of five short pulses at an output port bit line. Determine the overall execution time of the program segment and the period of the pulses generated





WAVEFORM GENERATED

	0			LDA	I	SET LOOP COUNT = 5
	1				05	
	2		LOOP	CLAC		SET OUTPUT PORT 00 BITS = LOW
	3			OPA		
	4				PORT 00	
	5			LDAI		SET OUTPUT PORT 00 BIT 7 = HIGH
	6				80	
	7			OPA		
	8				PORT 00	
	9			DCI		TEST FOR END
	A			JP	20	
	B				LOOP	
	C				—	
	D			CLAC		FINISHED - LEAVE OUTPUT PORT BITS LOW
	E			OPA		
	F			—	PORT 00	

FIGURE 29 : INSTRUCTION SEGMENT TIMING EXAMPLE

In the example in Figure 30, 6 of the program segment's 9 instructions are within the loop and are executed 5 times each. The last instruction in the loop, JP Z0, executes in one of two numbers of time states (7 or 10, Figure 27) according to whether or not the condition is met that the Z (Zero) flag is not set (Z=0). Fewer time states are needed if the jump does not occur, which is the case on the fifth iteration of the loop.

FLOW DIAGRAM FUNCTION	TIMES PERFORMED	INSTRUCTIONS	TIME STATES	CATEGORY AND EXECUTION TIME IN 320 NS 7801 SYSTEM
Set Loop Count = 5	Once	LDBI 05	7	LRI 2.24 µs
LOOP: Pulse output line once	Five Times	CLAC	4	ACC 1.28 µs
		OPA PORT 00	10	OPA 3.20 µs
		LDAI 80	7	LRI 2.24 µs
		OPA PORT 00	10	OPA 3.20 µs
Test for End	Five Times	DCB	4	CTR 1.28 µs
		JP Z0 LOOP	10/7	JP 3.20 µs (4 times); 2.24 µs (once)
Leave Output Line Low	Once	CLAC	4	ACC 1.28 µs
		OPA PORT 00	10	OPA 3.20 µs

FIGURE 30: SAMPLE TIMING CALCULATION

The total execution time for the functions performed once, outside the loop, is

$$2.24 + 1.28 + 3.20 = 6.72\ \mu s$$

One pass through the loop requires

$$1.28 + 3.20 + 2.24 + 3.20 + 1.28 + 3.20 = 14.40\ \mu s$$

Five loop iterations requires (5) (14.40) = 72.00 µs; however, the JP Z0 instruction requires only 2.24 us the fifth time instead of 3.20 us, so the total time is corrected to

$$72.00 - 0.96 = 71.04\ \mu s.$$

The total time for the program segment (instructions inside and outside the loop) is

$$71.04 + 6.72 = \underline{77.76\ \mu s}$$

The period of the pulses is found by adding the time the pulse is low to the time the pulse is high. The pulse is low from the end of the first OPA instruction to the end of the second (2.24 + 3.20 = 5.44 µs). The pulse is high from the end of the second OPA instruction to the end of the first (or third) OPA instruction as the program flows around (or exits) the loop (1.28 + 3.20 + 1.28 + 3.20 = 8.96 µs). The period of the pulses is therefore 5.44 + 8.96 = 14.40 µs, except the last pulse which is 13.44 µs due to the action of the JP Z0 instruction.

SECTION 6 - MEMORY AND I/O MAPPING AND CONTROL

Memory Addressing

The 7801's 16-bit Address Bus can directly address a 65,536-byte (64K) memory. A specific memory location is addressed when these conditions are met:

a. The Address Bus contains the specific address of the memory location (0000 through FFFF hexadecimal);

b. MEMRQ* (memory request) and RD* (read) or WR* (write) control signals are active.

c. MEMEX* (memory expansion) is active.

Other factors affecting the 7801's control of its memory are:

a. In the Interrupt Acknowledge Cycle the 7801 issues INTAK* in place of the memory enable signals, when responding to INTRQ*. This causes the interrupting device to provide an instruction to the 7801 over the STD Data Bus.

b. The 7801 can pause to wait for a slow memory-mapped device,or be single-stepped,by inserting WAIT states in memory access machine cycles.

c. The 7801 can disconnect from the STD BUS and enter the WAIT state while Direct Memory Access (DMA) operations are conducted by an alternate system controller card. DMA is controlled by the BUSRQ*/BUSAK* (Bus Request/ Bus Acknowledge) signals.

A typical memory implementation is shown in Figure 32.

12K-Byte Onboard Memory

The 7801 card has a combined EPROM/ROM and RAM memory on the card which is large enough to store the program and variable data required in many applications, without the need for additional external memory cards. The card is shipped with 1K of RAM and sockets which allow the user to add up to 8K of EPROM or masked ROM devices and to expand the RAM to 4K. The onboard memory sockets have addressing restrictions (Figure 31) and are not accessable in DMA operations

The onboard memory is organized as follows:

a. EPROM/ROM sockets: provide capacity for four 2716 or equivalent single +5V supply EPROM devices which can be mixed in any combination with 2316E or equivalent masked ROMs. Each device is a 2048-byte (2K) read-only memory for a total capacity of 8192 (8K) bytes. All of these devices are supplied by the user.

b. RAM and RAM Sockets: provides two 2114L or equivalent RAM devices organized as a 1024-byte (1K) memory, and sockets for six additional user-supplied 2114 RAMs. The 2114 is a 1024x4 device and two chips are required for each 1K of RAM added to the card. The total RAM capacity of the 7801 with all sockets loaded is 4096 (4K) bytes.

MEMORY DEVICE DESIGNATION	FULL HEXADECIMAL ADDRESS FIELD (1)			
	AS- SHIPPED	OPTION A	OPTION B	OPTION C
ROM 0 (2K)	0000 - 07FF	0000 - 07FF	C000 - C7FF	C000 - C7FF
ROM 1 (2K)	0800 - 0FFF	0800 - 0FFF	C800 - CFFF	C800 - CFFF
ROM 2 (2K)	1000 - 17FF	1000 - 17FF	D000 - D7FF	D000 - D7FF
ROM 3 (2K)	1800 - 1FFF	1800 - 1FFF	D800 - DFFF	D800 - DFFF
(2) RAM U15,U19 (1K)	2000 - 23FF	3000 - 33FF	E000 - E3FF	F000 - F3FF
RAM U16,U20 (1K)	2400 - 27FF	3400 - 37FF	E400 - E7FF	F400 - F7FF
RAM U17,U21 (1K)	2800 - 2BFF	3800 - 3BFF	E800 - EBFF	F800 - FBFF
RAM U18,U22 (1K)	2C00 - 2FFF	3C00 - 3FFF	EC00 - EFFF	FC00 - FFFF
(3) UNUSABLE ADDRESSES	3000 - 3FFF	2000 - 2FFF	F000 - FFFF	E000 - EFFF
INTENDED APPLICATION	ROM memory at 0000 allows onboard memory to take control immediately after system reset; recommended for most control applications.		ROM mapped into upper quadrant of memory allows user-supplied RAM memory with post-reset bootstrap at address 0000; required in many data processing and development system applications.	
	RAM addressing options allow for compatibility with various existing firmware packages, and 8085A-based systems from other manufacturers.			

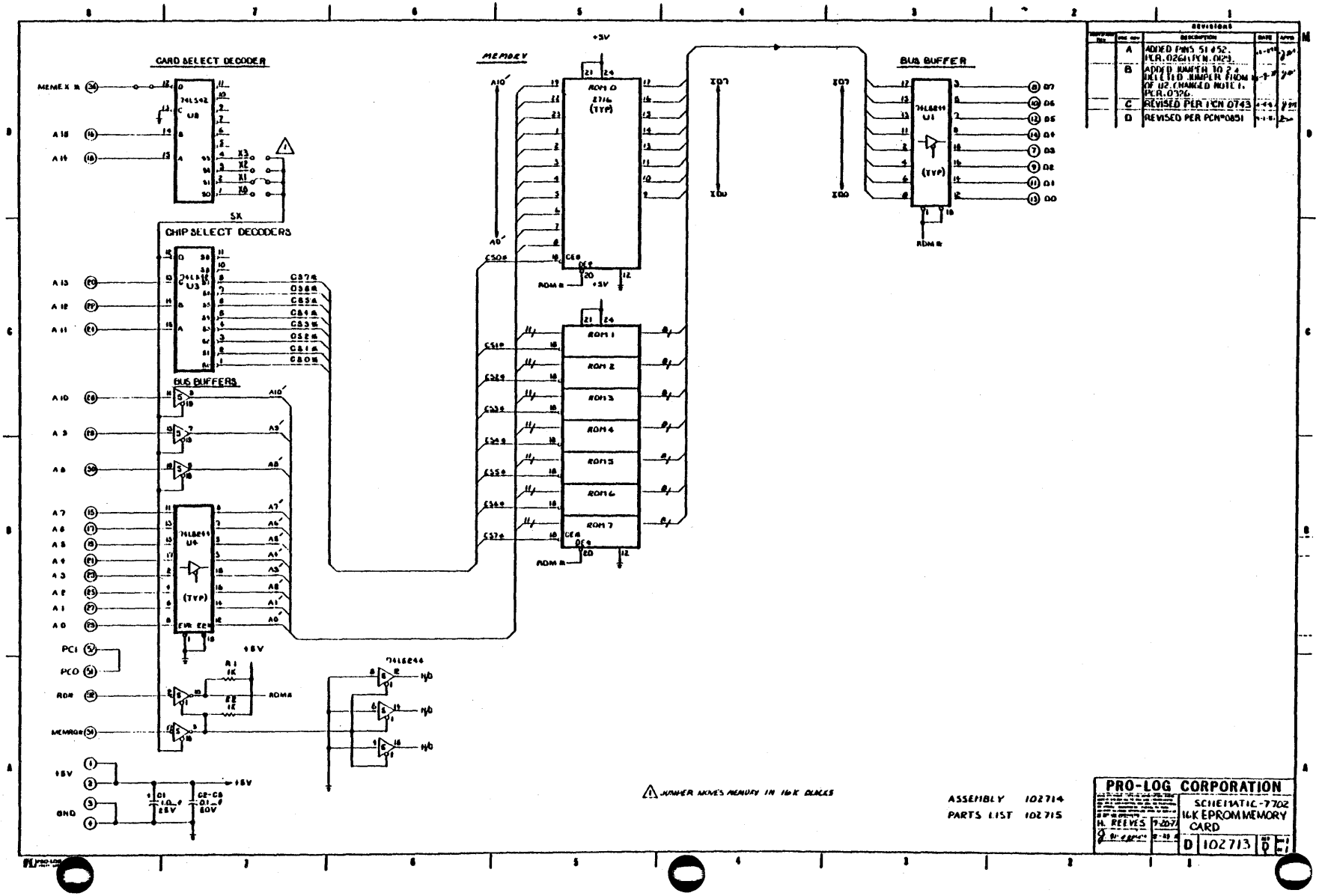
NOTES: (1) To implement wire-jumper options A, B, and C, refer to Appendix A

(2) RAM devices U15 and U19 are supplied with the 7801. All other memory devices are supplied by the user.

(3) Maximum 7801 system addressing range is 60K (12K onboard plus 48K on external cards) when using the 7801's onboard memory. If the onboard memory is disabled (Appendix A), maximum system memory size is 64K and no mapping restrictions are imposed by the 7801.

FIGURE 31 : 7801 ONBOARD MEMORY SOCKETS ADDRESS MAPPING

FIGURE 32: TYPICAL EXTERNAL MEMORY IMPLEMENTATION (7702 EPROM CARD)



Input/Output (I/O) Port Addressing

The 7801 can address up to 256 each input ports and output ports. The port address appears on the low-order half of the Address Bus (A0-A7) and is repeated on the high-order half of the Address Bus (A8-A15). A specific I/O port is addressed when the following conditions are met:

a. The Address Bus (A0-A7) contains the specific address of the I/O port (00 through FF hexadecimal);

b. IORQ* (I/O Request) is active

c. IOEXP* (I/O Expansion) is active

d. RD* (read) is active to select an input port, or WR* (write) is active to select an output port.

The 8-bit input ports provide a means for reading data or status lines into the processor to take part in programmed operations. The 8-bit output ports provide a means for outputting program-generated data or control states. Typical input and output port circuits are shown in Figure 33

Onboard Serial I/O Lines

The 7801 provides one serial output line (SOD*) and one serial input line (SID*) which are accessed at pins 4 and 5, respectively, of the User Interface Connector J1.

The serial I/O lines are TTL compatible and suitable for serial communications between 7801 Processor cards in a local distributed processing system, or as general purpose programmable TTL I/O control lines. These lines allow direct serial communication over short runs of dual twisted pair (signal/ground) lines up to 3 feet (1 meter) or less unterminated. For longer distances or for communication with a UART, isolation or signal conditioning may be necessary.

SOD* and SID* are programmed by the LDA 1 and LDI A (RIM and SIM) instructions as shown in Figure 22.

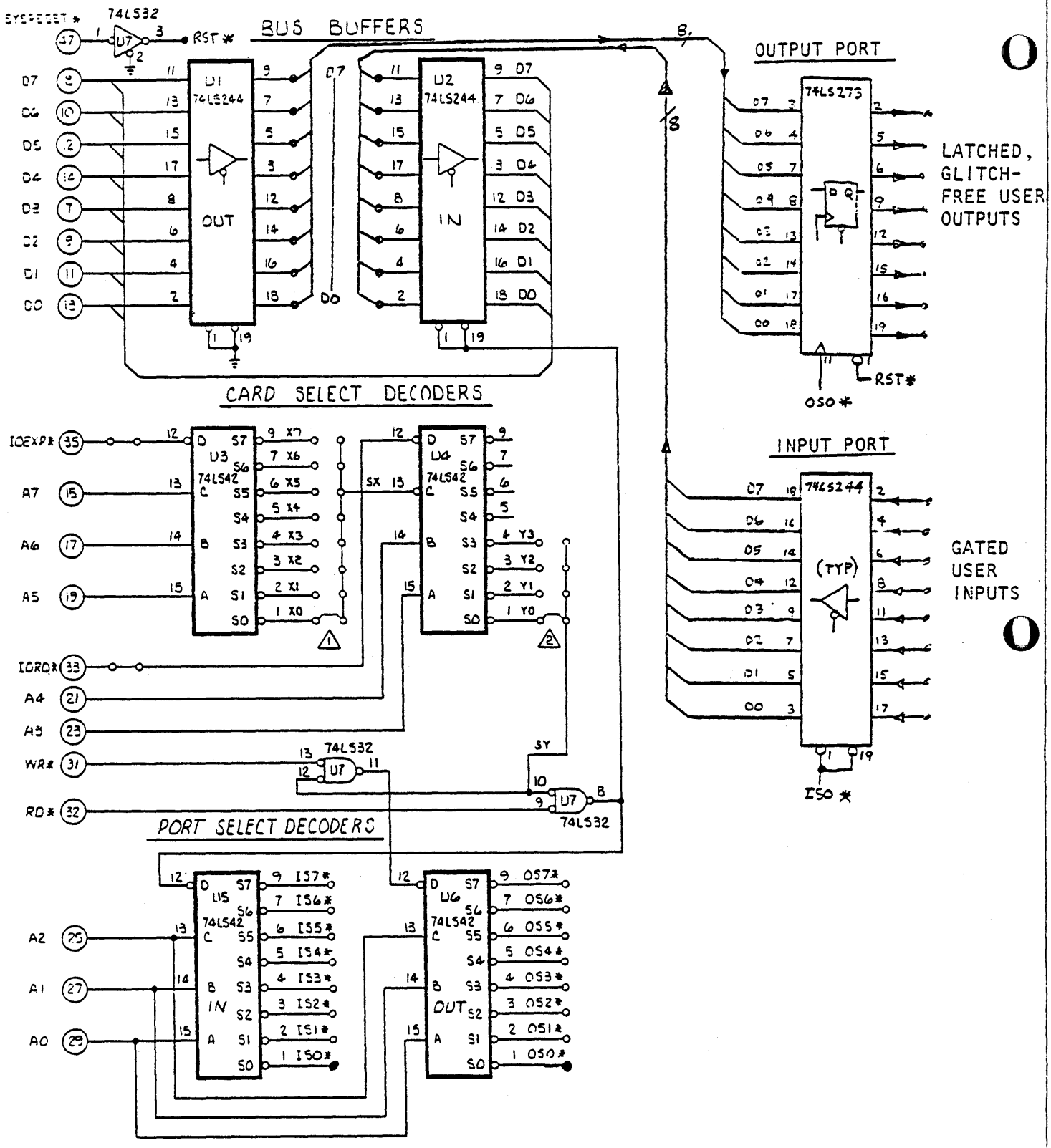


FIGURE 33: TYPICAL INPUT & OUTPUT PORT IMPLEMENTATION

This figure illustrates the Bus interface and I/O port address decoding circuitry and device types typically used to implement I/O ports. Pro Log's 7500, 7600, and 7900 Series I/O modules are similar to this example.

SECTION 7 - PROGRAM AND HARDWARE DEBUGGING

Microprocessor Logic State Analysis

An attempt at monitoring the execution of a microprocessor program in real time using a conventional multitrace oscilloscope will be found to be impossible for practical purposes. The capacity of the scope and the operator will be quickly exhausted by the magnitude of the problem because of the following characteristics:

a. Parallel data and addresses. Data is transferred as byte-parallel information (the address bus is 2 bytes wide). Individual bits on these busses have little meaning in program debugging. It is necessary to see the full content of both busses at once, and a hexadecimal display of numeric values is much more meaningful than binary waveforms.

b. Display Trigger Qualification. As many as 20 signals (combined address and control signals) may be used simultaneously to qualify the enabling of a peripheral memory card, for example. In order to capture this event, the test instrumentation must also be trigger-qualified by the same group of signals. Conventional oscilloscopes lack the number of trigger channels and operating modes needed to interface with a processor system such as the 7801.

c. Data Bus Voltage Levels and Timing. The 7801 and all of its peripheral cards in a given system will drive the Data Bus at different times, and will do so with a variety of logic high and logic low levels, all of which are different but within specification. This presents two problems: the operator will find it difficult to identify the source of any given waveform on the scope display; and in order to see a specific data segment on the Data Bus, the operator will find it necessary to synchronize the display with the processor's software program rather than with the voltage output of any one element of system hardware. The logic state analyzer solves these problems by displaying formatted high/low logic states rather than analog waveforms, and by offering enough trigger channels and coincidence logic to allow literal program/display synchronization.

A logic state analyzer is considered an essential troubleshooting aid for both program development and system maintenance in any 7801-based system where the needs of the Manufacturing Test and Field Service organizations are important considerations.

The logic state analyzer performs these basic functions:

a. Tracks the actual instruction sequence as the program executes, facilitating program debugging.

b. Monitors control states and data passing between the processor and the system it contols, allowing the system external to the processor card to be observed at the same time as the program flow, using the same display.

c. Provides a multi-qualified trigger to a conventional oscilloscope when analog measurements are unavoidable (e.g. propagation delay through a suspected memory device).

Figure 34 below shows the Data Bus content during the various time states for all of the 8085A's instructions, listed by Instruction Category (see also Figure 28). This is the information the user would expect to see presented on a logic state analyzer with the 7801's Data Bus displayed.

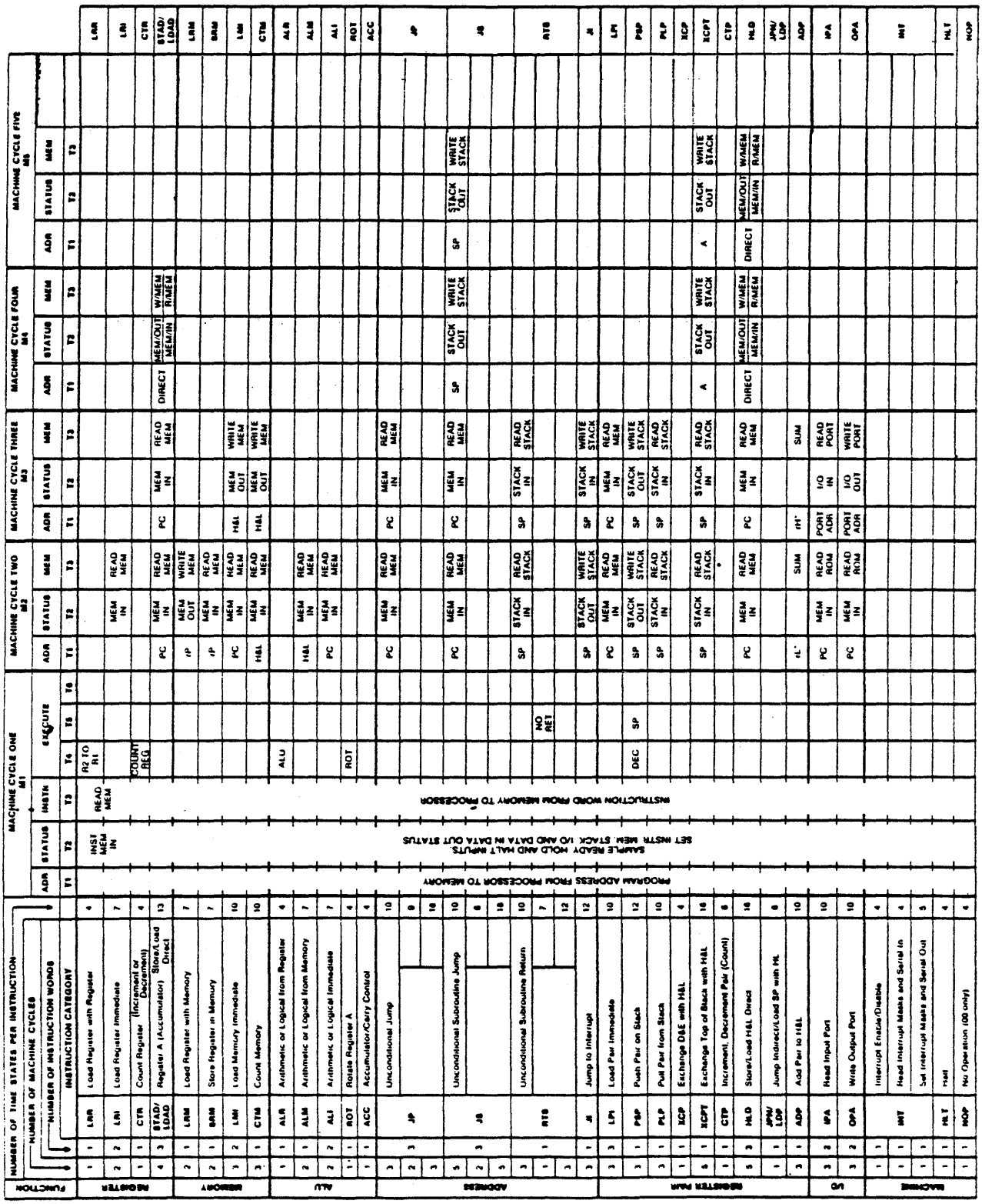


FIGURE 34 : 7801 DATA BUS CONTENT BY INSTRUCTION AND TIME STATE

Pro Log M825 System Analyzer

Figure 35 below summarizes the ability of the M825 to capture, format, and display the information available from all the time states in any user-specified machine cycle at any instruction in the operating program. The M825 can debug the program and system in dynamic, single-step, and breakpoint modes; track interrupts and DMA operations, pick instructions out of nested loops; and trigger other test equipment. The M825 is portable and clips onto the 8085A device on the 7801, eliminating the need for test probes and a lengthy test setup procedure.

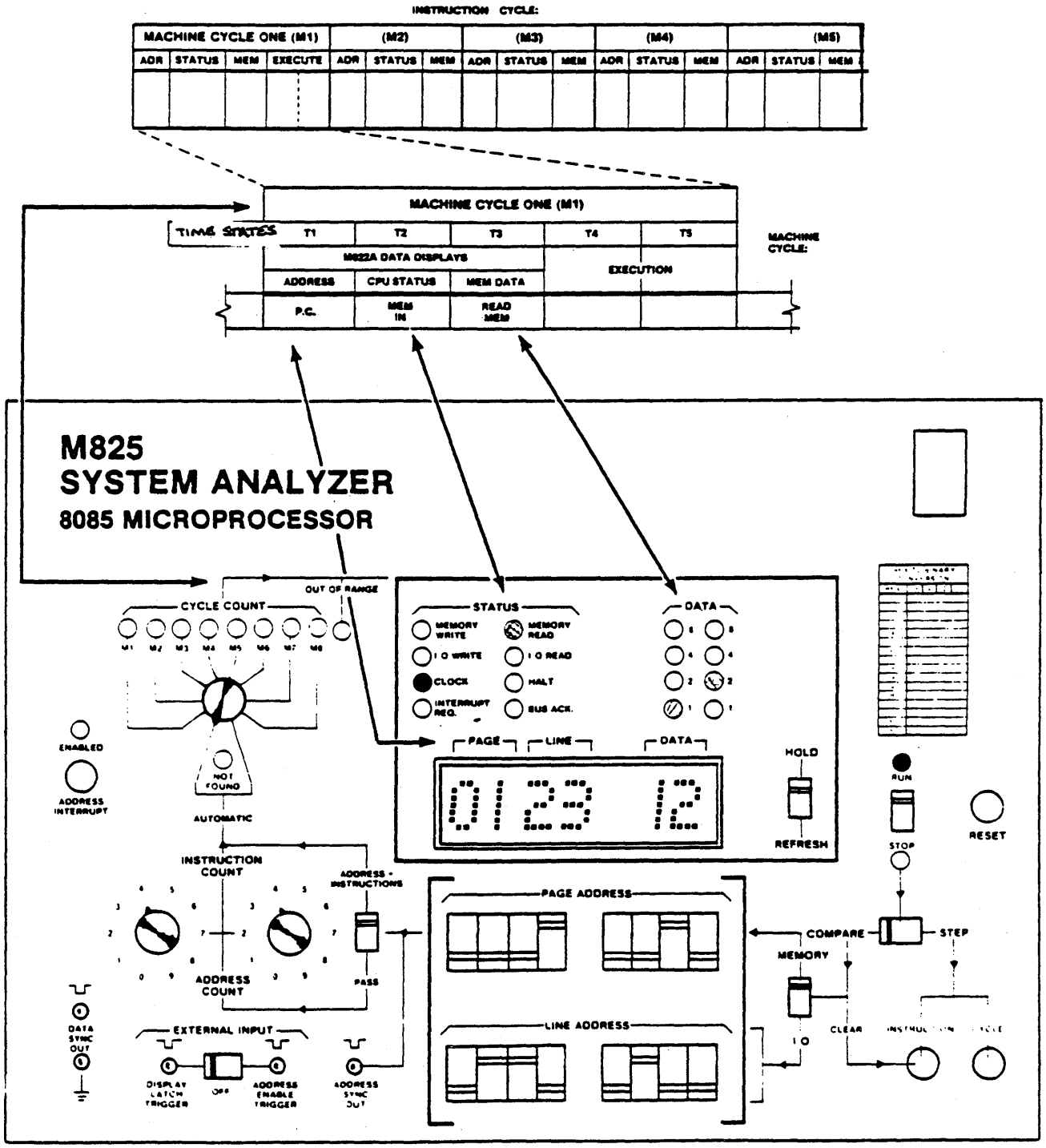


FIGURE 35 : M825 SYSTEM ANALYZER FOR 8085A-BASED SYSTEMS

APPENDIX A - 7801 USER STRAPPING OPTIONS

In new 7801 applications, system characteristics such as memory mapping and clock frequency are generally arbitrary. The as-shipped configuration of the 7801 is recommended to minimize system assembly costs, and field service and repair documentation efforts.

Jumper-wire strapping options are provided on the 7801 to allow processor upgrading in existing applications, compatibility with similar cards from other manufacturers, and compatibility with existing program firmware.

The strapping options for the 7801 are identified by the letters A through M on the Schematic (Pro Log document #102745), Assembly Diagram (102746), and by silkscreened letters on the 7801 circuit card. The options include:

a. Clock (jumpers A-D): output clock to STD BUS, or input external clock in place of crystal

b. Mapping and Bank Control (jumpers E-M): remap or disable the onboard RAM and EPROM memory sockets, and allow external control of bank selection (MEMEX* and IOEXP* lines).

Clock

Output: Certain 8085A peripheral devices, I/O functions, and BUS or logic signal analyzers require access to the system clock. Connecting jumper A places the 3.125 MHz clock (7801) on STD BUS trace pin 49. (CLOCK*). Note that the output driver for this signal is not floated during DMA operations.

Input: an external clock can be used to drive the 8085A's Ø1 input. This should be a TTL-compatible signal in the range of 1 to 6 MHz with 50% duty cycle. The 8085A will divide the external clock by 2, producing time states in the range 2000 ns to 333 ns (Figure 8).

The external clock is assigned STD BUS pin 50 (CNTRL*). Remove the 7801's crystal Y1 and connect jumper B (connect CNTRL* to 8085A pin 1). 8085A pin 2 should remain open.

NOTE: the driver supplying the clock to the 8085A should have VOH >+4V. A 470.56 to 1K pullup to +5V is recommended for standard TTL and LSTTL drivers.

Mapping

The 7801's onboard memory can occupy the lower quadrant of memory (0000-3FFF, as shipped), or the upper quadrant (C000-FFFF) or be disabled. Within the enabled selections, RAM can be contiguous with EPROM or separated for program compatibility with SBC-type cards.

Figure 36 summarizes these selections and shows the jumpers required to obtain them.

MEMORY ADDRESS ASSIGNMENT		JUMPER WIRES			
EPROMS	RAMS	E	F	J&K	L&M
0000 - 1FFF	2000 - 2FFF	OPEN	JUMPER	JUMPERS	OPENS
0000 - 1FFF	3000 - 3FFF	OPEN	JUMPER	OPENS	JUMPERS
C000 - DFFF	E000 - EFFF	JUMPER	OPEN	JUMPERS	OPENS
C000 - DFFF	F000 - FFFF	JUMPER	OPEN	OPENS	JUMPERS
DISABLED	DISABLED	OPEN	OPEN	DON'T CARE	

FIGURE 36 : ONBOARD MEMORY MAPPING JUMPERS

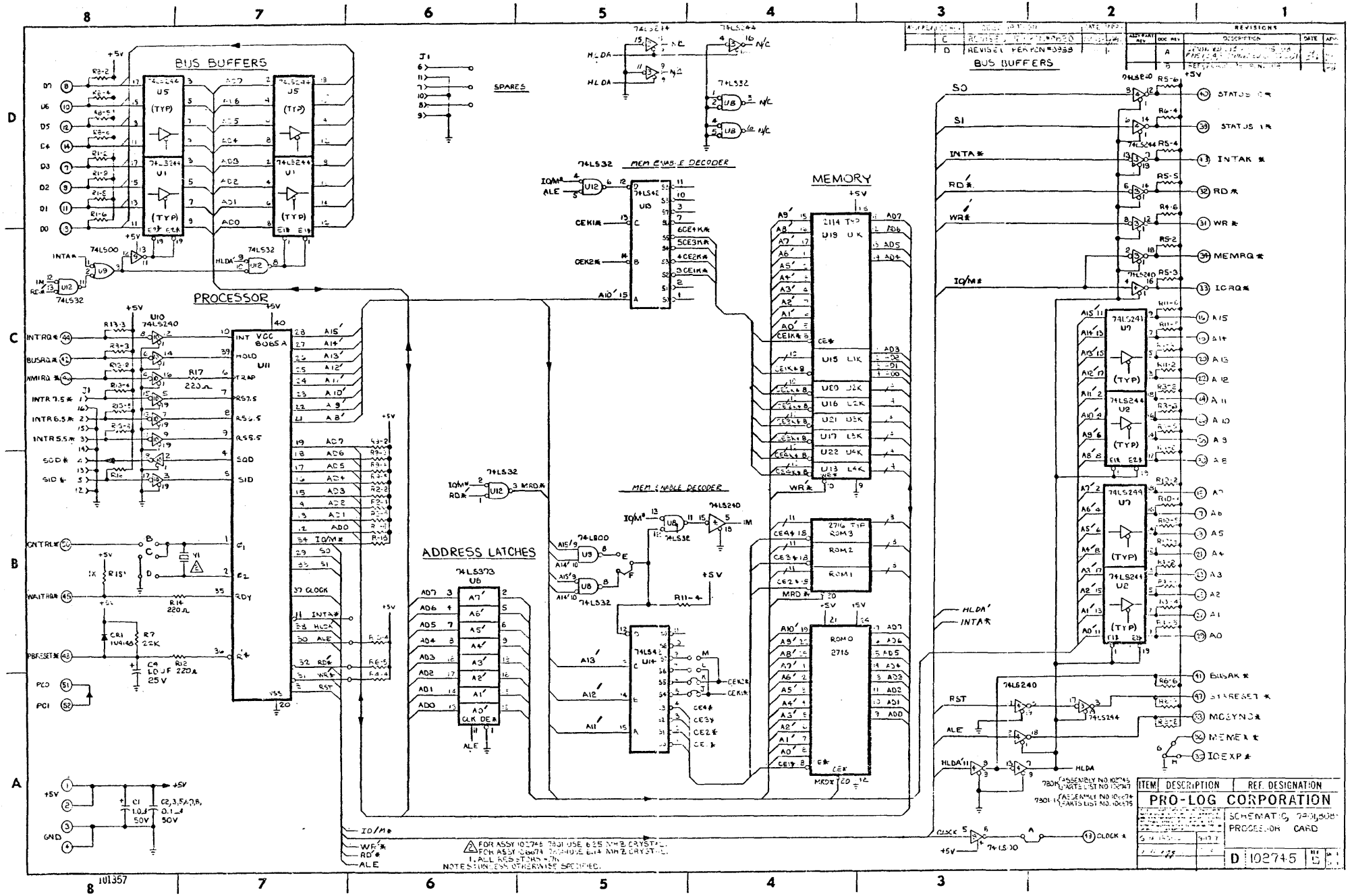
Bank Selection

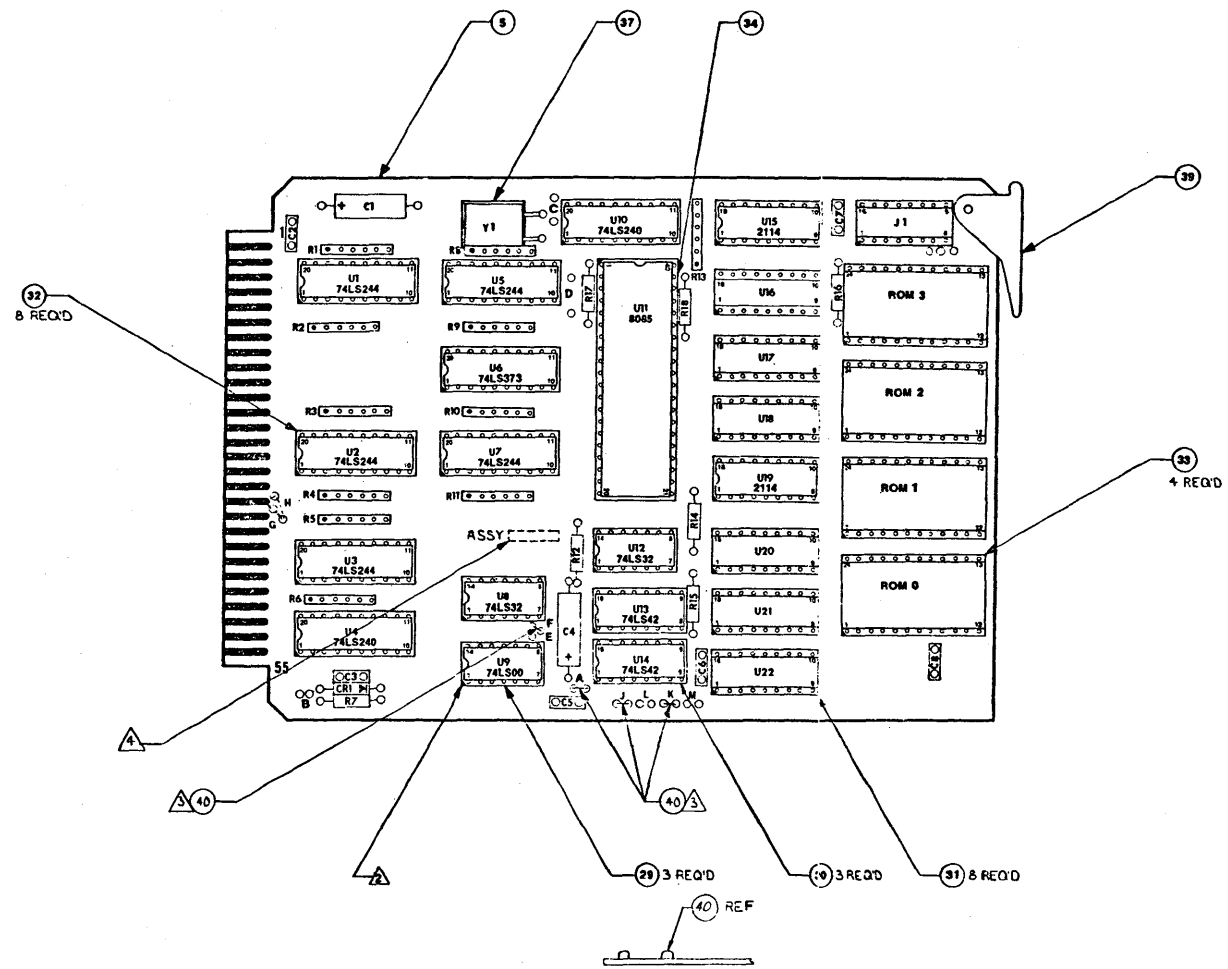
Jumpers G and H hold MEMEX* and IOEXP*, respectively, active by connecting the traces to ground on the 7801 card. At least one additional 64K memory bank and 256 I/O port bank could be enabled on the same motherboard by employing memory and I/O cards which regard MEMEX* and IOEXP* as high level active signals. Thus a high level on these traces would select the alternate memory or I/O bank while a low level selects the primary banks.

If the user wishes to implement alternate memory or I/O banks, open jumper trace G (MEMEX*) or H (IOEXP*) on the 7801. This allows a peripheral card to drive the bank expansion traces as required.

Note that the 7801's onboard memory sockets are not qualified by MEMEX* and thus remain available regardless of the state of MEMEX*, providing a convenient location for the instructions which control the memory bank selection.

DOCUMENTATION


BUS BUFFERS
PROCESSOR
SPARES
MEMORY
ADDRESS LATCHES
MEM ENABLE DECODER
MEM ENABLE DECODER
BUS BUFFERS
PRO-LOG CORPORATION
SCHEMATIC, 7801,7808
PROCESSOR CARD
D 102745
ITEM DESCRIPTION REF. DESIGNATION
FOR ASSY 102745 7801 USE 6.35 MHZ CRYSTAL
FOR ASSY 102674 7808 USE 8.64 MHZ CRYSTAL
ALL RESISTORS 1/4W
UNLESS OTHERWISE SPECIFIED
101357



REVISIONS				
ASSY/PART REV	DOC REV	DESCRIPTION	DATE	APP'D
	A	ALLEG [illegible]	[illegible]	[illegible]
	B	[illegible]	[illegible]	[illegible]
	C	REF [illegible]	[illegible]	[illegible]
	D	UPDATE [illegible] 45	[illegible]	[illegible]
	E	REVISED PER P.N. [illegible]	[illegible]	[illegible]
	F	REVISED PER PCN [illegible]	[illegible]	[illegible]
	G	REVISED PER PCN 0086	[illegible]	[illegible]

ITEM	DESCRIPTION	REF. DESIGNATION
36	6.25 MHZ	Y1
17	IN5148	CR1
16		
15	1K 1/4W 5%	R15
14	22K 1/4W 5%	R7
13	4.7K NETWORK	R1-R6, R8-R11, R13
12	4.7K 1/4W 5%	R16, R5
11		
10	220 Ω 1/4W 5%	R14, R12, R17
9		
8	1.0 μF 50V	C1, C4
7	0.1 μF 50V	[illegible]

SCHEMATIC NO. 102745
PARTS LIST NO. 102747

1. IDENTIFY WITH ASSEMBLY NO. AND REV. LETTER USING RUBBER STAMP.
2. INSTALL JUMPERS AS SHOWN ON COMP SIDE OF BOARD.
3. INDICATES PIN NO. 1 OF SOCKETS (TYP.)
4. FOR ASSY PROCEDURES SEE AS1004.

NOTES: UNLESS OTHERWISE SPECIFIED.

PRO-LOG CORPORATION

[illegible]	ASSEMBLY, PROL 8085 PROCESSOR CARD
C.A.CLARK	
[illegible]	D 102746

FOR BUS APPLICATIONS ONLY

TEST EQUIPMENT
M825, 8085(A) SYSTEM ANALYZER

The M825 System Analyzer is a portable, cost-effective instrument which supports the design, development, production, and field service of 8085 and 8085A Microprocessor-based systems. The unit functions as a program monitor, program-to-hardware integrator and provides many of the display functions of a computer control panel.

FEATURES:

- **Tests Systems using the 8085 or 8085A Microprocessor**
- **Displays Address, Data, Machine Cycle, and Status**
- **Static and Dynamic Display Modes**
- **System Run/Step Control**
- **System Reset Push Button**
- **Connects to Processor Chip Via Clip-On or Low-Profile Connector**
- **Oscilloscope Trigger at Address Compare or Data Display Time**
- **Delayed Data Capture**
- **Memory or I/O Address Select**
- **Non-Maskable Interrupt Capability at Address Compare**
- **External Control of Data Display**
- **Address Stop**
- **Interrupt Trap and Display**
- **Interface Buffer to Minimize Microprocessor Loading**
- **High-Impact Attache Case**

M825, System Analyzer in Case

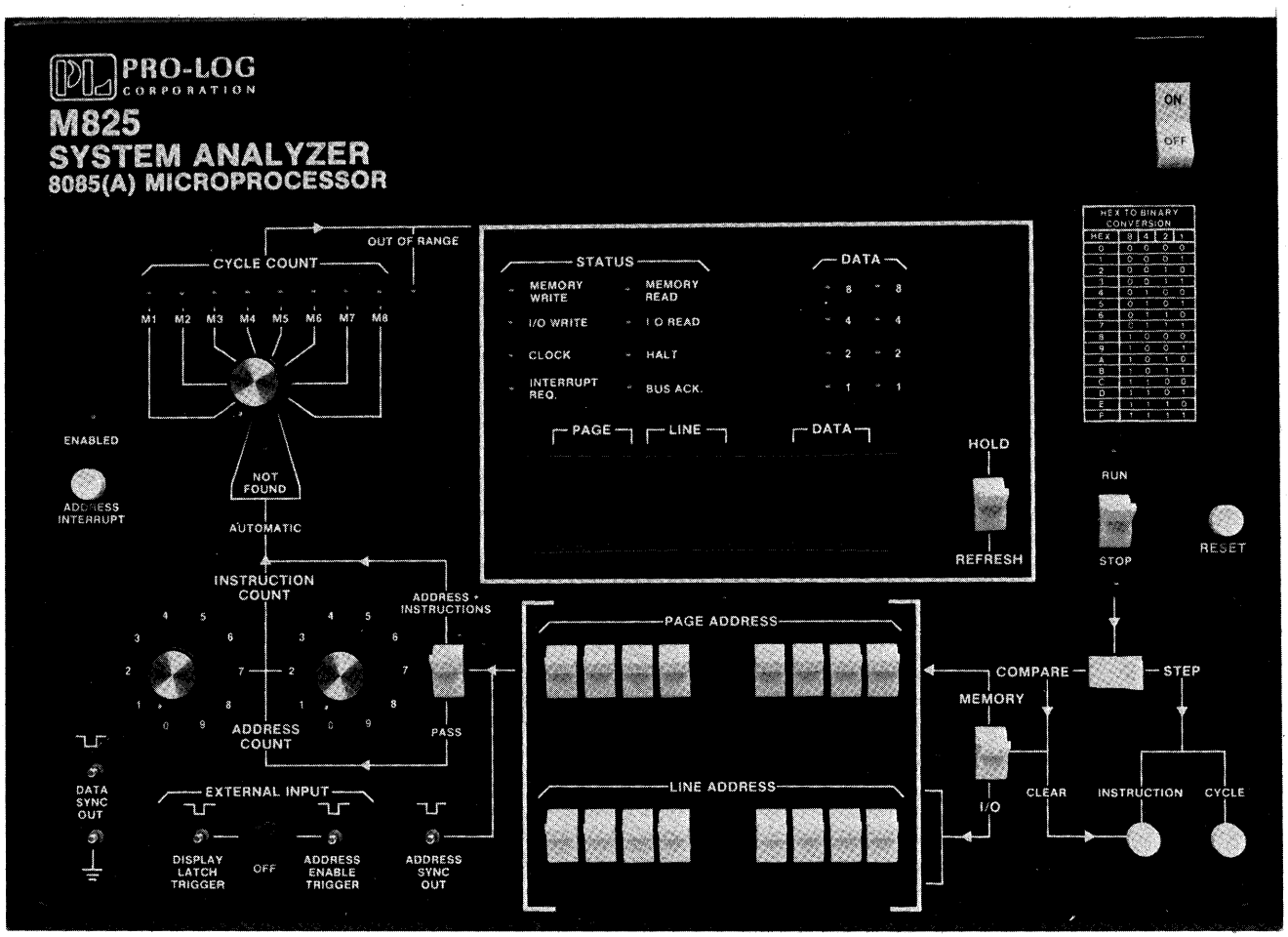
The M825 is self-contained and easily connected to your system microprocessor by means of a single DIP clip or low-profile connector. It is useful as an alternative or complement to software techniques for program development or debugging of 8085-based microprocessor systems. Since it is easily attached, the M825 System Analyzer, together with adequate program documentation, is an ideal tool for field service or production.

The Analyzer allows examination of the system (address, data, and status) during a user-specified machine cycle at the desired Compare Address. Observation of the system is possible at full system speed or by single-step by instruction or machine cycle. The possible display modes are dynamic mode, in which the processor continues to run without analyzer interference, and static mode, in which the analyzer controls the processor WAIT line.

Delayed Data Capture affords the capability of observing a particular machine cycle up to 99 instructions past a chosen reference address. The feature also allows observing the reference address after a user-defined number of passes over that address. A two-decade address counter, coupled with a single machine cycle counter, provides the operator with the capability of simply "dialing" his way through the program under investigation. This delay capability may be extended to any number by utilizing Stop/Compare mode.

The M825 provides Memory or I/O Address selection and Interrupt Trap and/or Stop on Interrupt, along with Hex address, Hex and Binary Data, and Status Displays. The analyzer also features an oscilloscope synchronization output pulse during Address Compare and Data Display Latch time. DATA SYNC OUT can be utilized to trigger an oscilloscope at any selectable instruction cycle.

Operator-initiated functions include microprocessor push button Reset, Latch Display or Latch Display and Stop at the next T2 state after trigger, Stop on Next Address Compare after trigger, and generation of non-maskable interrupt at Address Compare time.



M825, Front Panel

ADDRESS CONTROLS

ADDRESS Switches: Sixteen address (bit) select toggle switches, broken into two groups: Page Address (high order address - A8 thru A15) and Line Address (low order address or I/O - A0 thru A7); used to establish the trigger reference address.

RUN/STOP Switch: Selects dynamic mode (microprocessor continues to run) or static mode (microprocessor is stopped at Data Latch time and may be stepped through the program).

COMPARE/STEP Switch: Is only functional in stop mode and selects Stop on Address Compare and single Step on cycle or instruction.

MEMORY I/O Switch: Selects examination of data flow to/from memory location defined by Page and Line Address switches, or I/O device defined by the low-order (Line) address switches.

HOLD/REFRESH Switch: Controls latching of the data display. In HOLD, the display is frozen the first time the selected compare condition is met. In REFRESH, the display is refreshed each time the selected compare condition is met.

DELAYED DATA CAPTURE CONTROLS

ADDRESS + INSTRUCTION/PASS Toggle Switch: Address + Instruction mode allows data selection and display at an address up to 99 instructions beyond Compare Address. Pass mode allows up to 99 passes through a selected address before data is displayed.

ADDRESS COUNT/INSTRUCTION COUNT Rotary Switch: Controls the number of address passes in Pass mode, the number of additional instruction in Address + Instruction mode.

CYCLE COUNT Rotary Switch: Selects machine cycle of interest.

ADDRESS INTERRUPT PUSH BUTTON

ADDRESS INTERRUPT: Activation of this push button will set an Address Compare latch and the next occurrence of Address Compare will generate a Non-Maskable Interrupt. Appropriate interrupt service routines must be supplied by the user and located at the required memory location. If the Analyzer is stopped by Address Compare, the interrupt will be generated immediately.

DISPLAYS

ADDRESS: Displays 16-bit address as 4 Hex digits within a range of 0000-FFFF.

DATA: a 2-digit Hex display and two groups of 8 (bit) indicators, providing binary and hex data representation.

STATUS: Eight individual indicators showing Data and Machine Status.

MEMORY READ/WRITE AND I/O READ/WRITE: Indicate the function associated with the data being displayed.

CLOCK: Indicates the processor clock is operational.

INTERRUPT REQ: Indicates a System Interrupt has occurred.

HALT: Indicates the processor is in the HALT state.

BUS ACK: Indicates the processor has acknowledged and responded to a Bus Request.

RUN/STOP: Indicates status of the Machine READY line; RUN for program execution, STOP for processor idle (WAIT state).

CYCLE COUNT: Machine cycle indicator showing the cycle of the instruction with which the displayed data is associated.

NOT FOUND: Indicates that the selected machine cycle was not found.

ENABLED: Indicates the Address Interrupt feature is enabled.

OUT OF RANGE: Indicates a Machine Cycle greater than 8 is being displayed.

SYNC POINTS

ADDRESS SYNC OUT: Provides a negative pulse out for oscilloscope triggering each time the selected address compares with the system address lines.

DATA SYNC OUT: Provides a delayed negative pulse out for oscilloscope triggering each time the Analyzer data display is latched. The delay is a function of the setting of Address/Instruction + Machine Cycle Count selectors.

DISPLAY LATCH TRIGGER IN: Each negative input edge causes the Analyzer to latch data at the next T2 time. If the display selector is in the Hold mode, Address and Data are latched for each negative edge and all Address Compare Data is locked out. If the Analyzer is in the Stop mode, the system can thus be halted by the external event.

ADDRESS ENABLE TRIGGER IN: For each negative input edge an Address Compare latch will be set and the next Address Compare occurring will stop the system via the WAIT line whether or not the Analyzer is in the Run mode. Depressing CLEAR will release the system and reset the latch.

GROUND Pin: Ground provided for all outputs and triggers.

USER SYSTEM REQUIREMENTS

The READY, RESET IN and TRAP lines must be capable of being wire-ORed. All interrupt lines must be strapped inactive if not used. A minimum gate isolation resistance of 220Ω is recommended.

MAXIMUM μP CLOCK FREQUENCY: 3.2 MHz

LOADING SPECIFICATIONS

Inputs:

Address, Data, Clock and System Control Lines	0.125 TTL Loads @ 50 pf
INTR, RST 7.5, RST 6.5, and RST 5.5	0.25 TTL Loads @ 50 pf
READY, RESET IN	1.6 TTL Loads @ 100 pf
TRAP	0.125 TTL Loads @ 100 pf
Display Latch and Address Enable Trigger	1.6 TTL Loads @ 50 pf

Outputs:

READY, RESET IN	8 TTL Loads
TRAP	ON: Source 40 mA (min) to +5V OFF: Open Circuit
Address and Data Sync Out	1 TTL Load

POWER REQUIREMENTS

50/60 Hz 115 VAC @ 0.75 amp or
50/60 Hz 230 VAC @ 0.300 amp

PHYSICAL CHARACTERISTICS

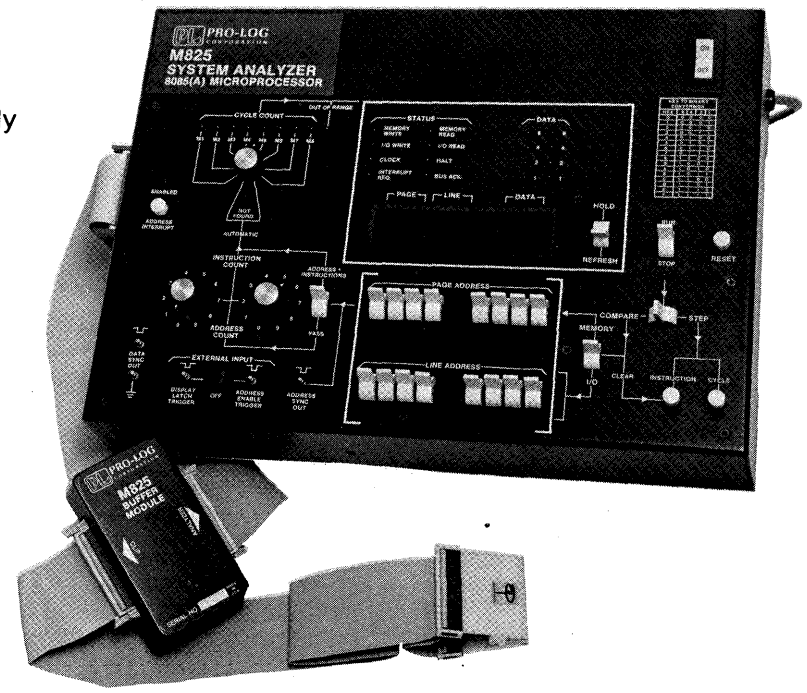
Analyzer Control Unit	Buffer Module and Cables	Attache Case
Height - 4.5"	Height - 1.125"	Height - 6.5"
Width - 21"	Width - 2.5"	Width - 12.5"
Length - 12"	Length - 4.5"	Length - 23"

Total product weight is less than 15 pounds.

OPERATING TEMPERATURE: 0°C to +45°C

M825 INCLUDES:

- Analyzer Control Unit
- Plug-in Buffer Module and Cable
- 40 Pin DIP Clip Connector Assembly
- 40 Pin Low-Profile Connector Assembly
- Attache Case
- Two Copies of Operating Manual



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USER'S MANUAL

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