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SantaFe

CPU : DOTHAN-ULV
Chip Set : INTEL 915GMS
Remarks : CPT LCD

Model Name : SantaFe
PBA Name :

Dev. Step : SR
Revision : 0.9
T.R. Date : 2005.xx.xx

DRAW	CHECK	APPROVAL
YM An	HJ Kim	JS Euh

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DRAW	Youngno An	DATE	3/7/2006	TITLE	SantaFe	SAMSUNG ELECTRONICS
CHECK	HJ Kim	DEV. STEP	SR	COVER	PART NO.	
APPROVAL	JS Euh	REV	0.9	March 7, 2006 12:22:03 PM		PAGE 1 OF 41
MODULE CODE	LAST EDIT					

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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
CARDBUS	AD25	0	A
USB Hub to PCI	AD29(internal)	Programmable	
LPC Bridge/IDE/AC97/SMBUS	AD30(internal)		
Internal MAC	AD31(internal)		
Internal MAC	AD24(internal)		

I²C / SMB Address

Devices	Address	Hex	Bus
ICH6M	Master	-	SMBUS Master
CK-410M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 001X	A2h	
MICOM	Master		
BATTERY	0001 011h	16h	-
THERMAL MORNITOR	x100 1100	4Ch	-

USB PORT Assign

PORT 0	RIGHT SIDE USB PORT
PORT 1	LEFT SIDE USB PORT
PORT 2	TSP CONTROLLER
PORT 3	DMB
PORT 4	BLUETOOTH
PORT 6	MINI CARD
PORT 5,7	EMPTY

System Power States

Power Rail	Devices (Page Number)
P5V	FAN(9) ICH6M(15) 80PORT(19) MICOM(25) DMB(27) USB(27) CARDBUS POWER(28) LDQ(31) AUDIO AMP(32)
P3.3V	CLOCK(6) Thermal sensor(9) SODIMM(14) ICH6-M(17) FWH(19) 80PORT(19) HDD(24) MICOM(25) DMB(27) CARDBUS Controller(28) MiniCARD(29) SUB Left(30) CPU VRM(37)
P1.5V	CPU(8) 915GMS(12) ICH6-M(17) MiniCARD(29)
P2.5V	915GMS(11) ICH6-M(17) LCD(22) CRT(23) LAN(26)
P1.8V	CARDBUS Controller(28)
P5V_AUX	ICH6M(17) ISL6227(35) DDR2 POWER(36)
P3.3V_AUX	LM26CIM5X-TPA(9) ICH6-M(17) MICOM(25) LAN(26) LB LED(25) MiniCARD(29) MAX1999(34)
P1.8V_AUX	915GMS(11) SODIMM(17) DDR2 POWER(36)
VCCP	CLOCK(6) CPU(8) 915GMS(10) ICH6-M(17) MICOM(25)
VCC_CORE	CPU (8)

Voltage Rails

Power Rail	Descriptions
PRTC_BAT VDC	3.3V (can drop to 2.0V min. in G3 state) supply for the RTC well. Primary DC system power supply (9 to 19V)
P5V_AUX	5.0V power rail (off in S4-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P1.8V_AUX	GMCH/DDR II Power Source(off in S4-S5)
MEMT_VREF	0.9V DDR2 Reference(off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
VCCP	1.05V power rail. GMCH core, CPU/GMCH FSB Termination.
VCC_CORE	Core voltage for DOTHAN CPU (0.74~1.30V)
MICOM_P3V	3.3V always on power rail for MICOM
P1.5V_DMI	1.5V (Direct Media Interface Compensation)
INV_VDC	DC power (Inverter)
LCD_VDD3V	3.3V (LCD)
VCC_CRT	5V (CRT)
CB3_A_VCC	3.3V (CF card)
AVDD	4.75V (AD1986)
AMP_VDD	5V (Audio AMP)
BLT_P3.3V	3.3V(BLUETOOTH)

CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V
0	0	0	0	1	0	1.676 V	1	0	0	0	1	0	1.164 V
0	0	0	0	1	1	1.660 V	1	0	0	0	1	1	1.148 V
0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1	1.116 V
0	0	1	0	0	0	1.612 V	1	0	0	1	1	0	1.100 V
0	0	1	0	1	1	1.596 V	1	0	0	1	1	1	1.084 V
0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V
0	0	1	0	0	1	1.564 V	1	0	1	0	0	1	1.052 V
0	0	1	0	1	0	1.548 V	1	0	1	0	1	0	1.036 V
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V
0	0	1	1	0	0	1.516 V	1	0	1	1	0	0	1.004 V
0	0	1	1	0	1	1.500 V	1	0	1	1	0	1	0.988 V
0	0	1	1	1	0	1.484 V	1	0	1	1	1	0	0.972 V
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.930 V
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V
0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V
0	1	0	1	1	0	1.356 V	1	1	0	1	1	0	0.844 V
0	1	0	1	1	1	1.340 V	1	1	0	1	1	1	0.828 V
0	1	1	0	0	0	1.324 V	1	1	1	0	0	0	0.812 V
0	1	1	0	0	1	1.308 V	1	1	1	0	0	1	0.796 V
0	1	1	0	1	0	1.292 V	1	1	1	0	1	0	0.780 V
0	1	1	0	1	1	1.276 V	1	1	1	0	1	1	0.764 V
0	1	1	1	0	0	1.260 V	1	1	1	1	0	0	0.748 V
0	1	1	1	0	1	1.244 V	1	1	1	1	0	1	0.732 V
0	1	1	1	1	0	1.228 V	1	1	1	1	1	0	0.716 V
0	1	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V

DOTHAN-ULV
HIGH FREQUENCY MODE

DOTHAN-ULV
LOW FREQUENCY MODE

DOTHAN-ULV
DEEPER SLEEP MODE
Refer to page43

DRAW	Youngno An	DATE	3/7/2006	TITLE	SantaFe	SAMSUNG ELECTRONICS
CHECK	HJ Kim	DEV. STEP	SR	MAIN		
APPROVAL	JS Euh	REV	0.9	BOARD INFORMATION		PART NO.
MODULE CODE		LAST EDIT	March 7, 2006 12:22:03 PM	PAGE	5	OF 41

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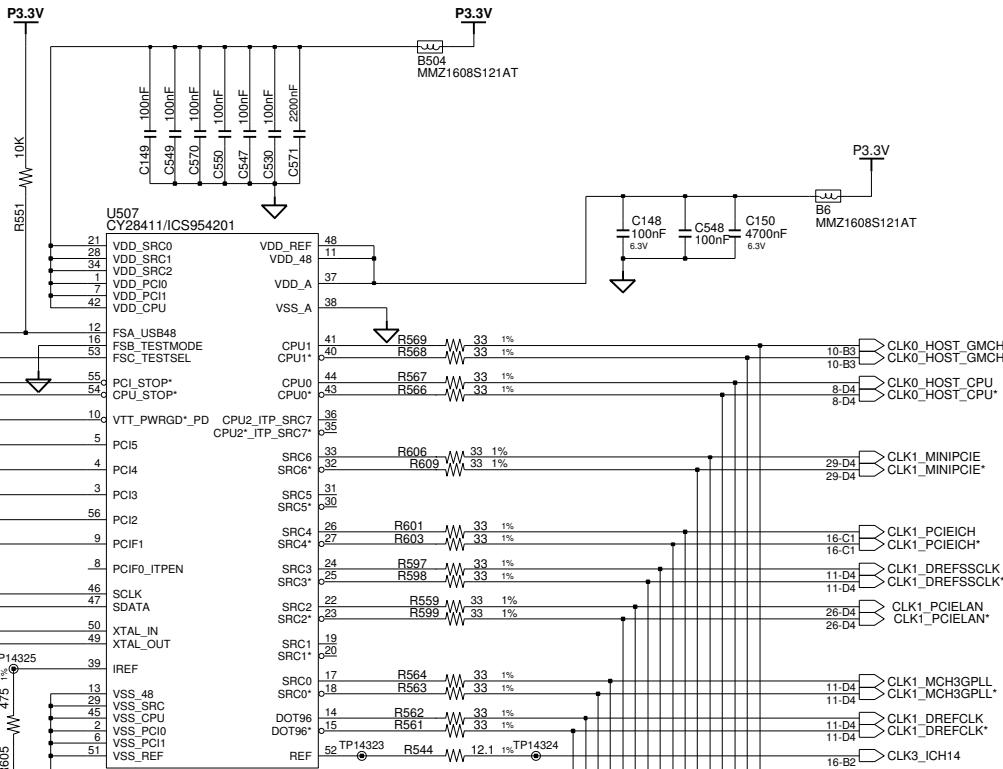
CK-410M

ICS954201
CY28411ZC

Bus Selection for CK-410M (100MHz)

F5B/F5C : by CPU/MCH BSEL(Page 6)
F5A : P3.3V PU

CK-410M CPU	F5A BSEL2	F5B BSEL1	F5C BSEL0	HOST CLK
	0	0	0	266 MHz
	0	0	1	333 MHz
	0	1	0	200 MHz
	0	1	1	400 MHz
	1	0	0	133 MHz
	1	0	1	100 MHz
	1	1	0	166 MHz
	1	1	1	RSVD

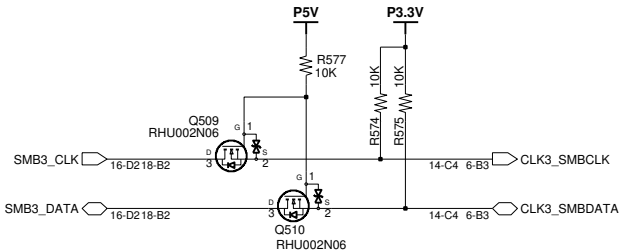


Place 14.318MHz within 500mils of CK-410M

Trace Width *2

SMBUS Address "D2h"
ICS: 1205-002705
Cypress: 1205-002574

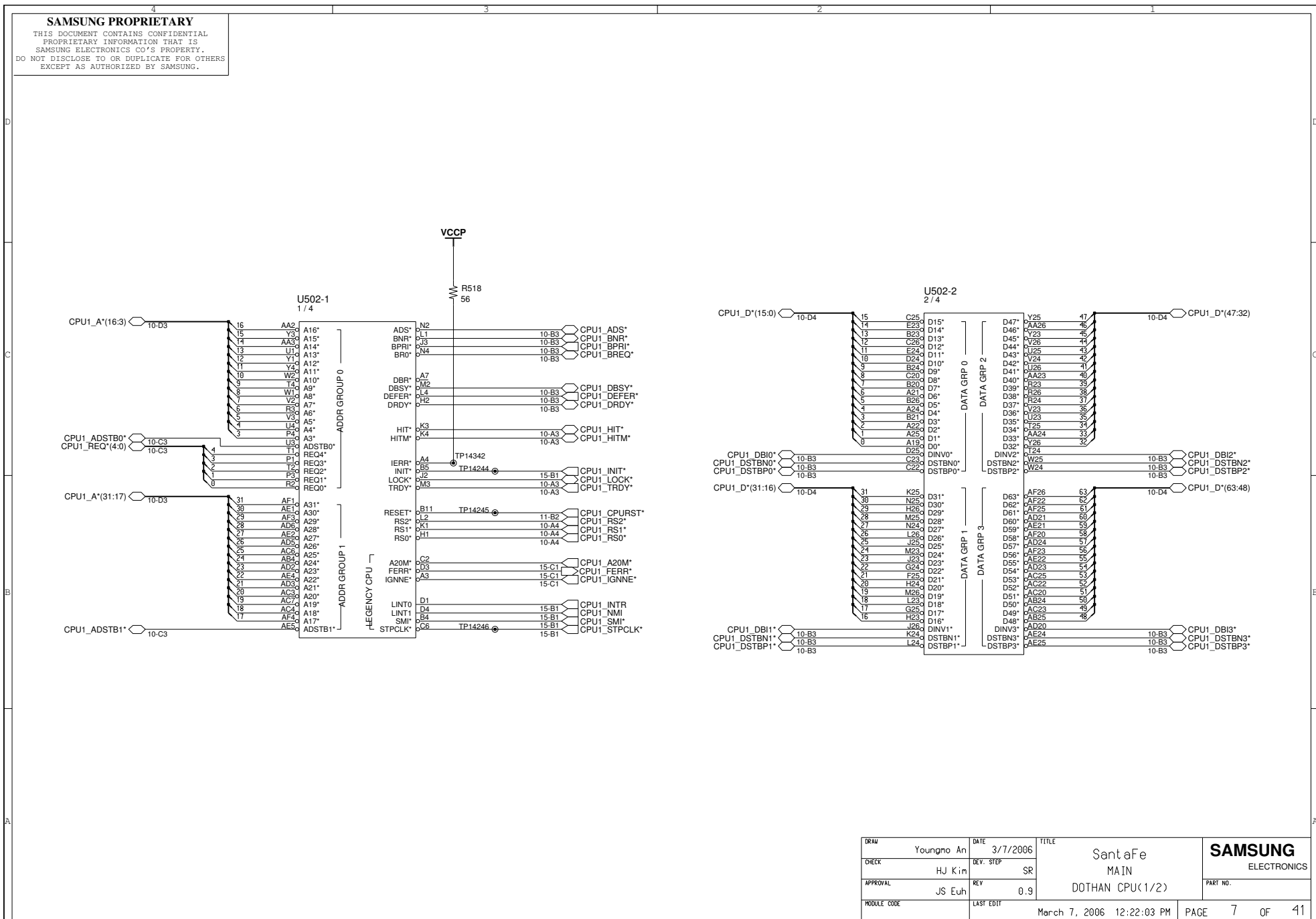
Place Termination close to CK-410M



DRAW	Youngno An	DATE	3/7/2006	TITLE	SantaFe MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS
CHECK	HJ Kim	DEV. STEP	SR	REV	0.9	
APPROVAL	JS Euh	LAST EDIT	March 7, 2006 12:22:03 PM	PAGE	6 OF 41	PART NO.

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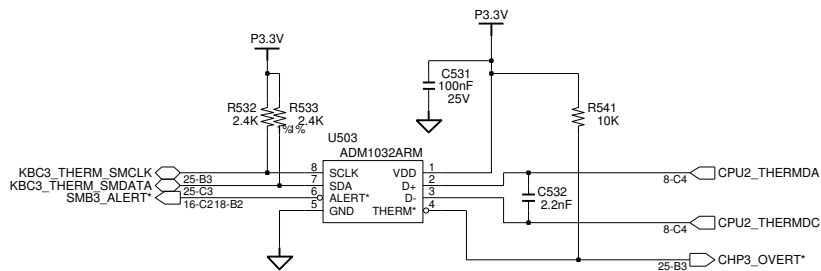
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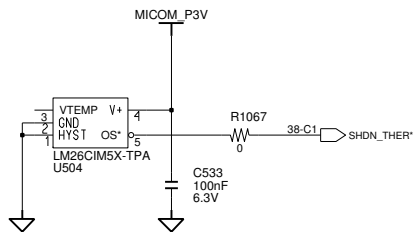
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CHECK	HJ Kim	DEV. STEP	SR			
APPROVAL	JS Euh	REV	0.9			
MODULE CODE		LAST EDIT				
March 7, 2006 12:22:03 PM					PAGE	7 OF 41

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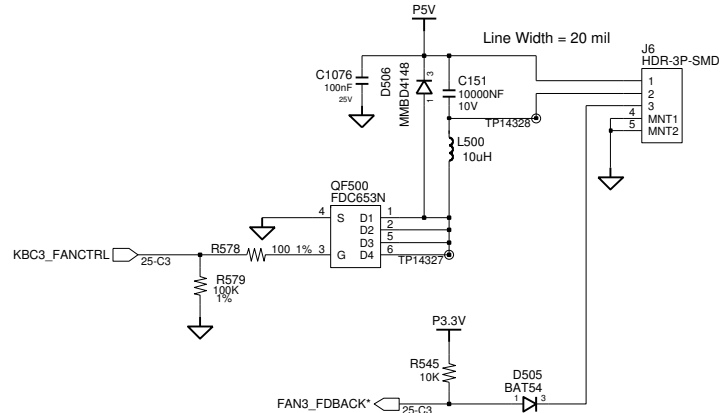
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CPU Thermal Sensor
 SMBUS Addr"4Ch"(x100 1100)
 Put this sensor between CPU and MCH



FAN Control Logic

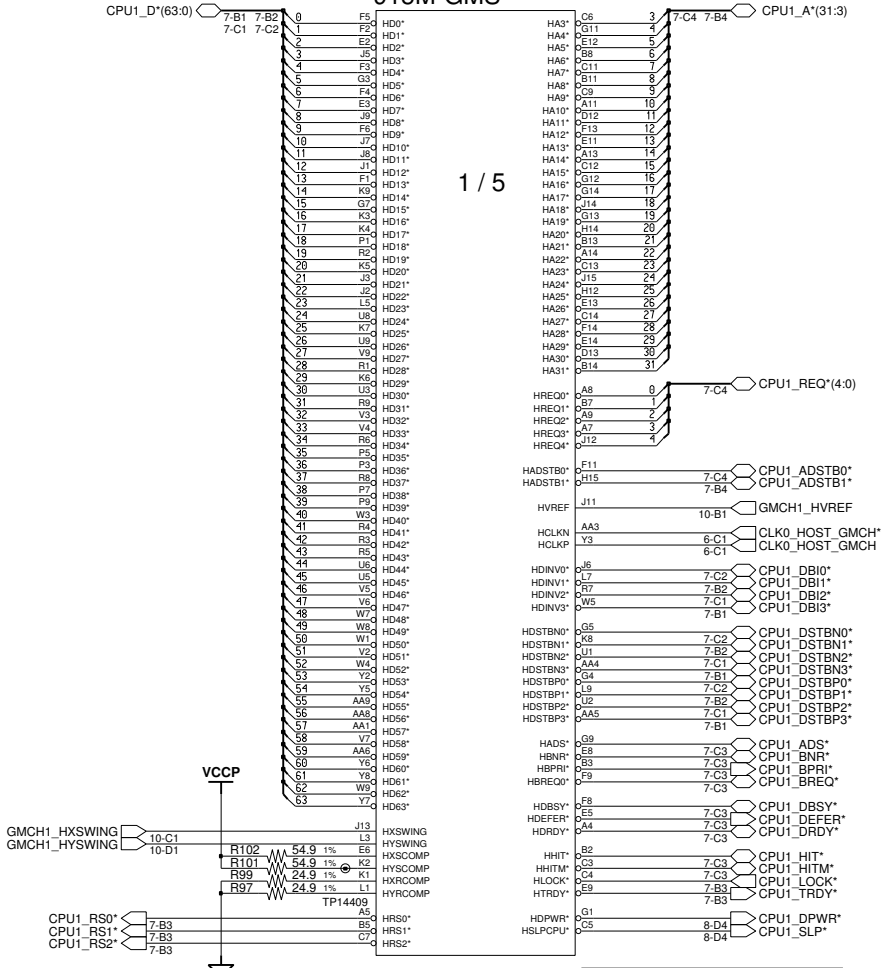


DRAW	Youngno An	DATE	3/7/2006	TITLE	SantaFe MAIN	SAMSUNG ELECTRONICS
CHECK	HJ Kim	DEV. STEP	SR	THERMAL SENSOR/FAN CONTRL		
APPROVAL	JS Euh	REV	0.9	PART NO.		
MODULE CODE		LAST EDIT	March 7, 2006 12:22:03 PM	PAGE	9	OF 41

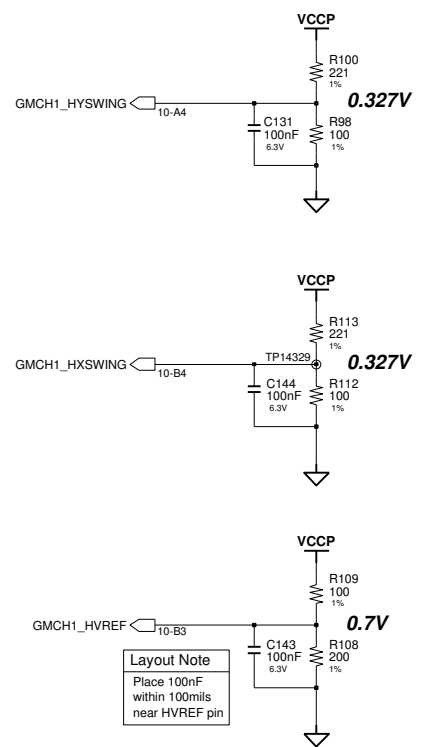
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**U506-1
915M-GMS**



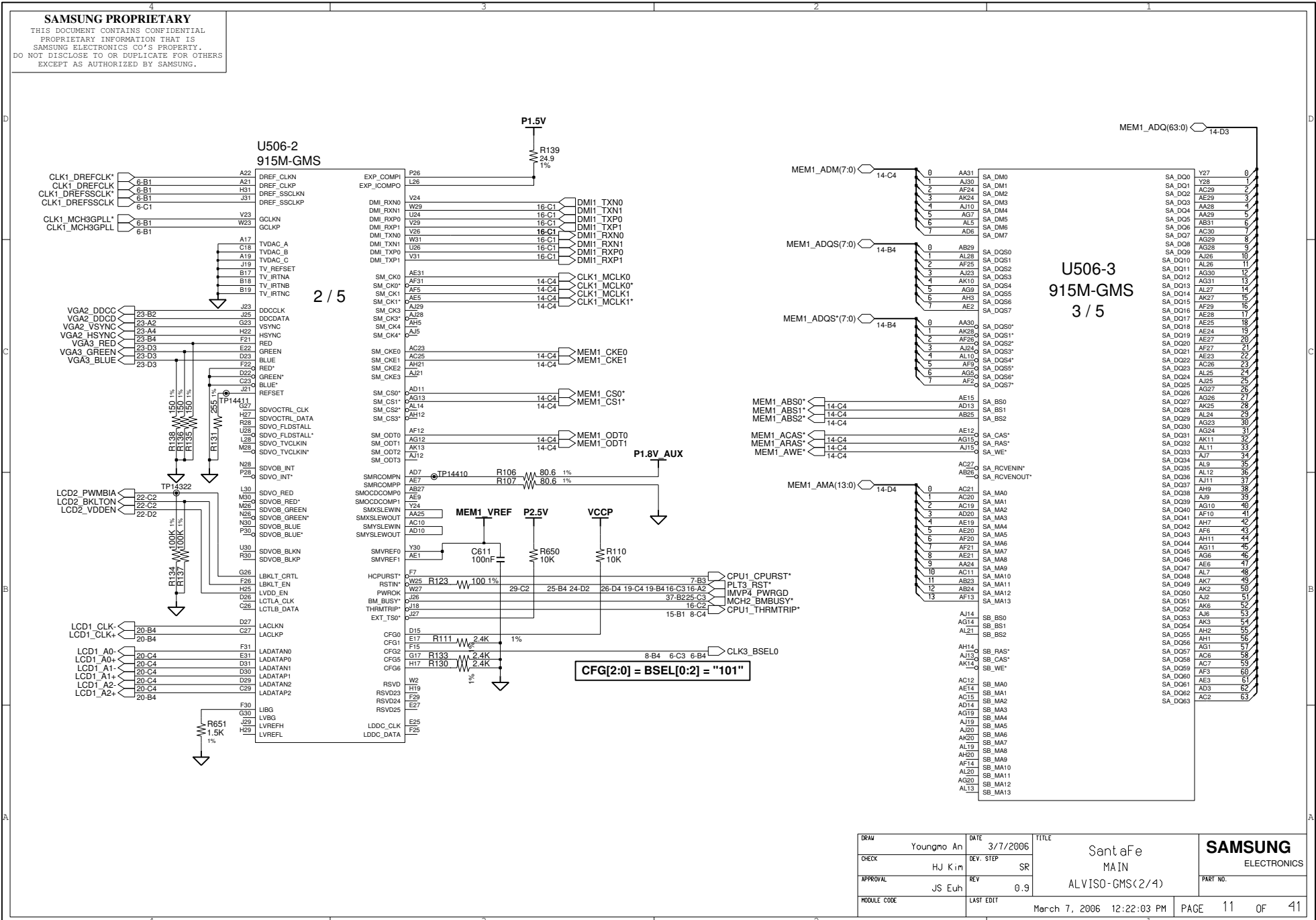
HSLPCPU* - GMCH : Enhanced mode (def.)
HSLPCPU* - ICH : Legacy mode



DRAW	Youngmo An	DATE	3/7/2006	TITLE	SantaFe MAIN ALVISO-GMS(1/4)	SAMSUNG ELECTRONICS
CHECK	HJ Kim	DEV. STEP	SR	PART NO.		
APPROVAL	JS Euh	REV	0.9	March 7, 2006 12:22:03 PM	PAGE	10 OF 41
MODULE CODE		LAST EDIT				

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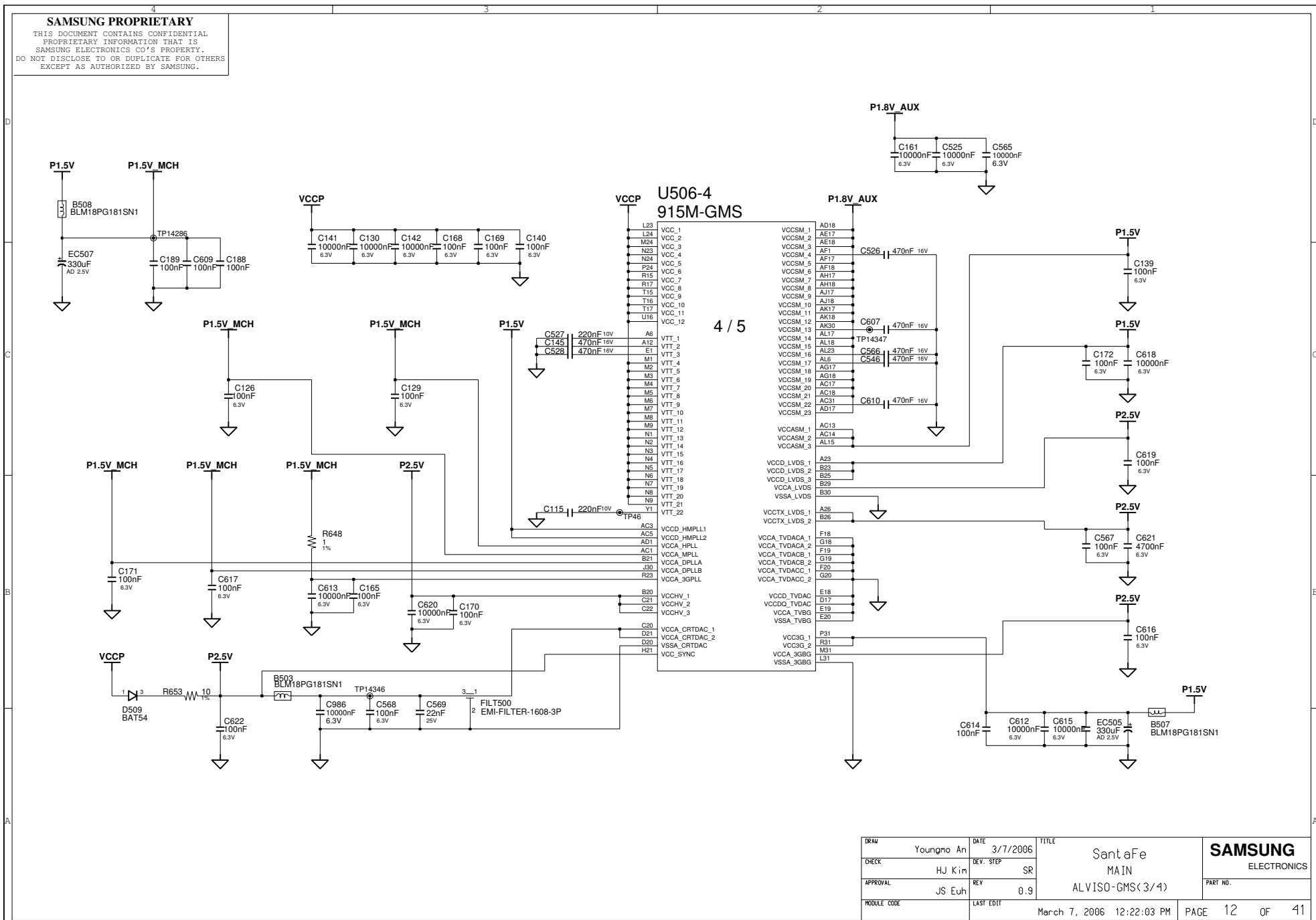
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CHECK	HJ Kim	DEV. STEP	SR	MAIN		
APPROVAL	JS Euh	REV	0.9	ALVISO-GMS(2/4)		PART NO.
MODULE CODE		LAST EDIT	March 7, 2006 12:22:03 PM	PAGE	11	OF 41

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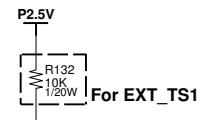
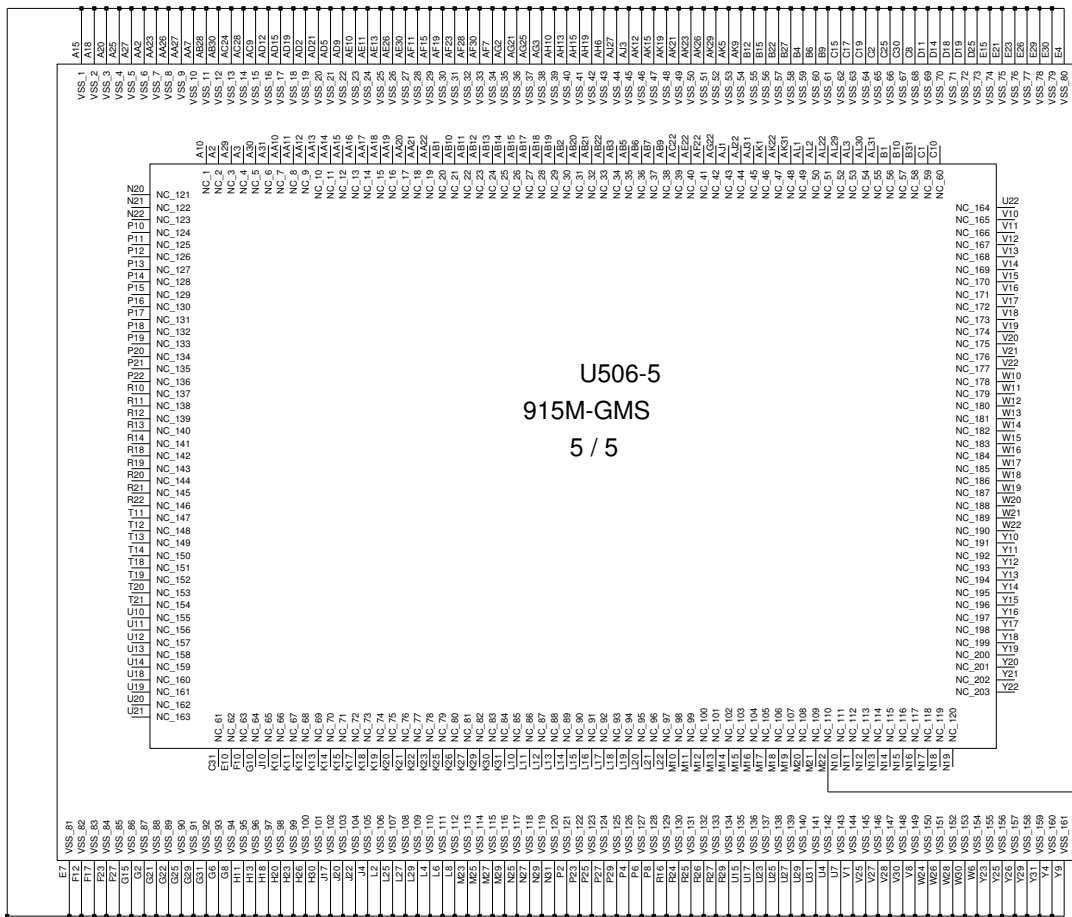
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CHECK	HJ Kim	DEV. STEP	SR			
APPROVAL	JS Euh	REV	0.9			
MODULE CODE		LAST EDIT	March 7, 2006 12:22:03 PM	PAGE 12 OF 41		

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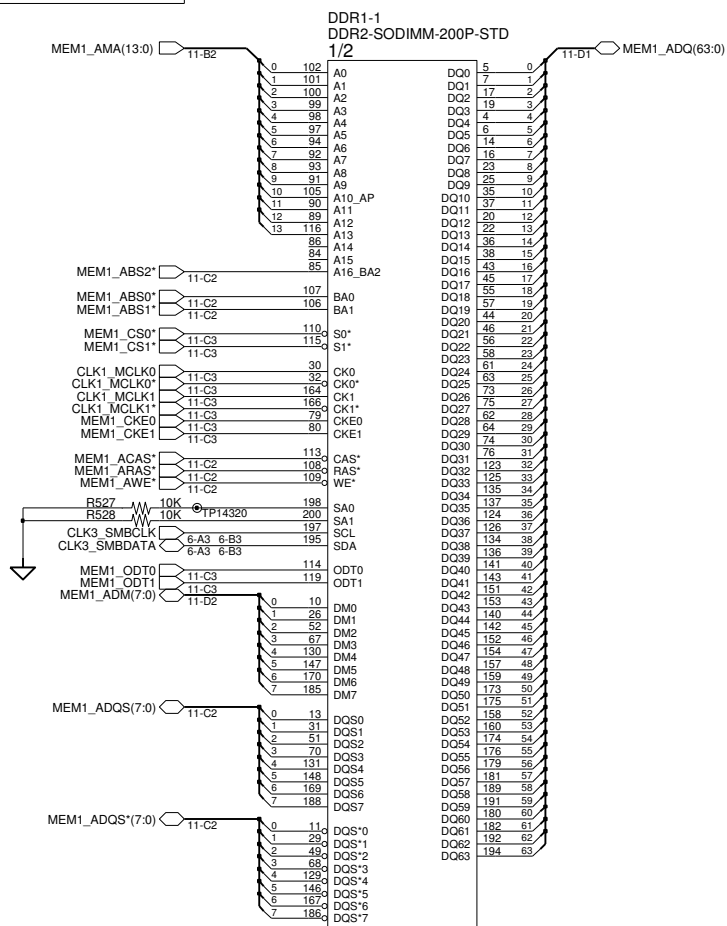
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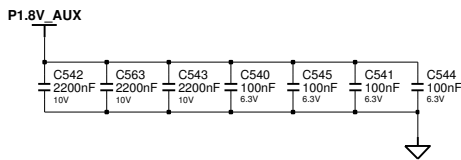
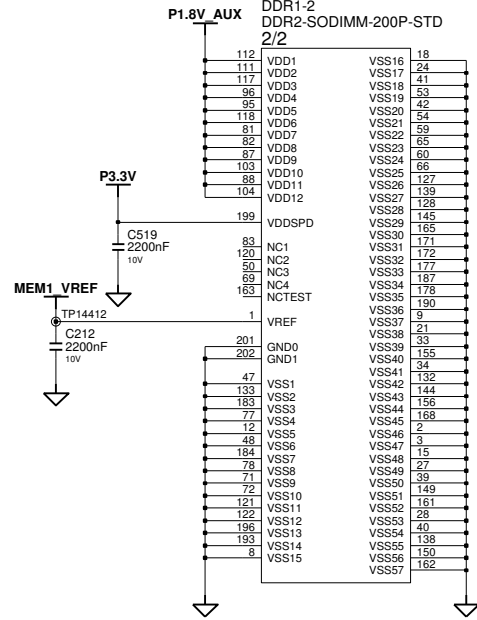
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CHECK	HJ Kim	DEV. STEP	SR	PART NO.		
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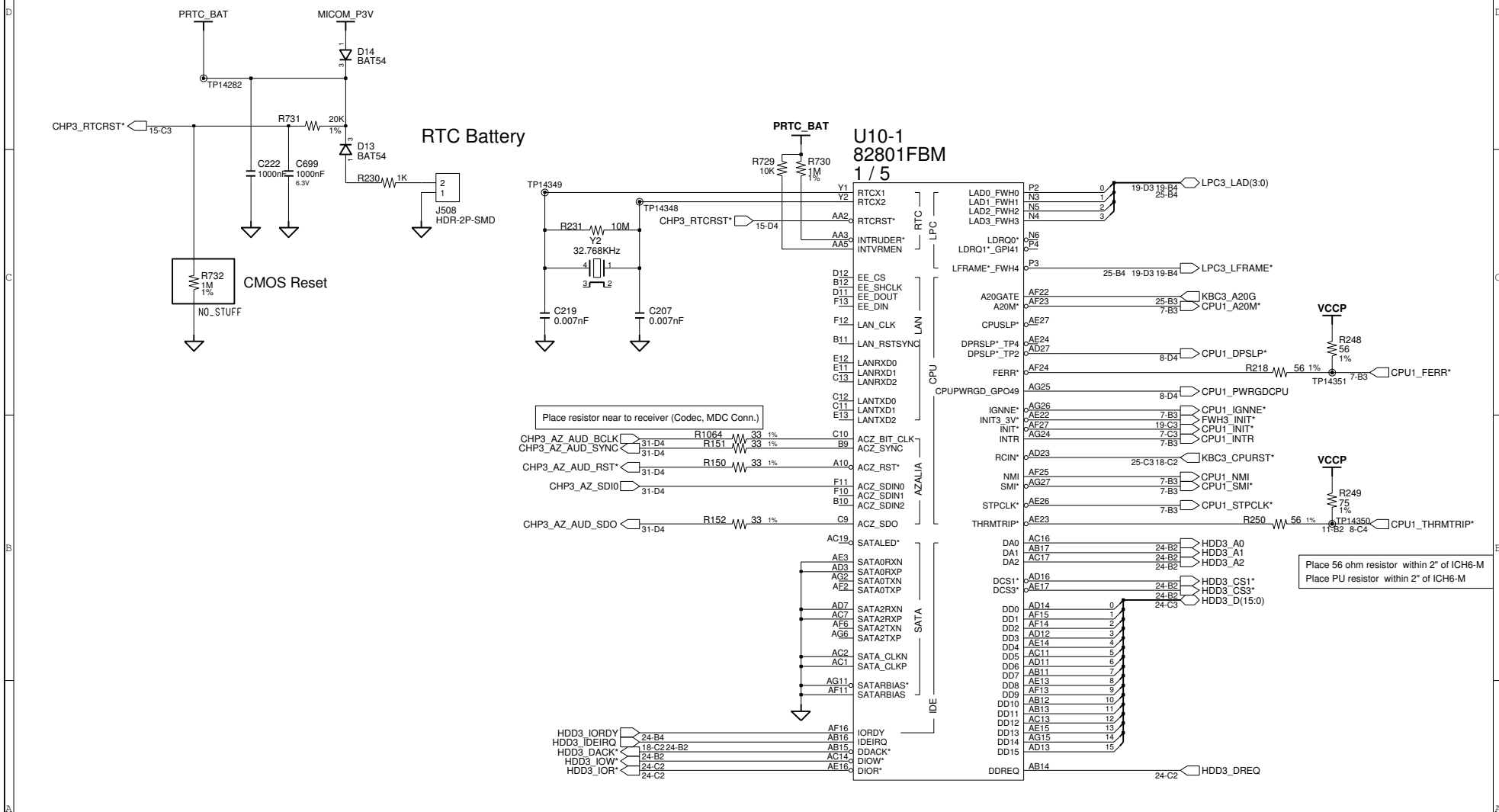
SMBUS ADDR "A2h"



DRAW	Youngno An	DATE	3/7/2006	TITLE	SantaFe MAIN DDR2 Memory	SAMSUNG ELECTRONICS
CHECK	HJ Kim	DEV. STEP	SR	PART NO.		
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Place resistor near to receiver (Codec, MDC Conn.)

Place 56 ohm resistor within 2" of ICH6-M
Place PU resistor within 2" of ICH6-M

DRAW	Youngmo An	DATE	3/7/2006	TITLE	SantaFe MAIN	SAMSUNG ELECTRONICS PART NO.
CHECK	HJ Kim	DEV. STEP	SR	ICH6-M (1/4)		
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MODULE CODE		LAST EDIT	March 7, 2006 12:22:03 PM	PAGE	15 OF 41	

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U10-2 82801FBM 2 / 5

U10-3 82801FBM 3 / 5

AC caps : PCIe need to be within 250mils of the driver Resistor for Test : Place Stuffing Option to minimize stubs

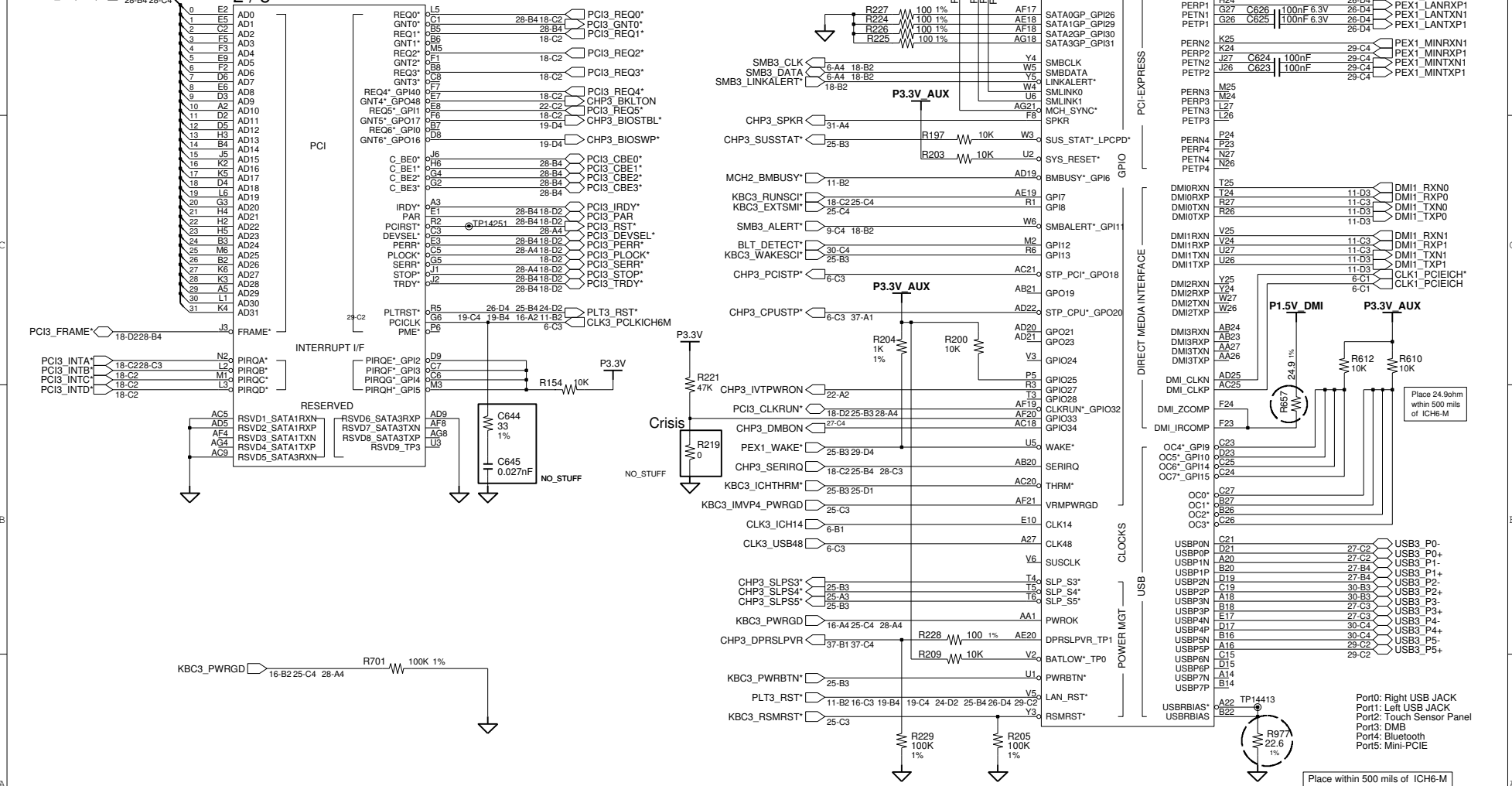


Table listing PCI Express pins and their connections to external components like capacitors and resistors.

Table listing Direct Media Interface pins and their connections to external components like capacitors and resistors.

Table listing USB pins and their connections to external components like capacitors and resistors.

Table listing Power Mgt pins and their connections to external components like capacitors and resistors.

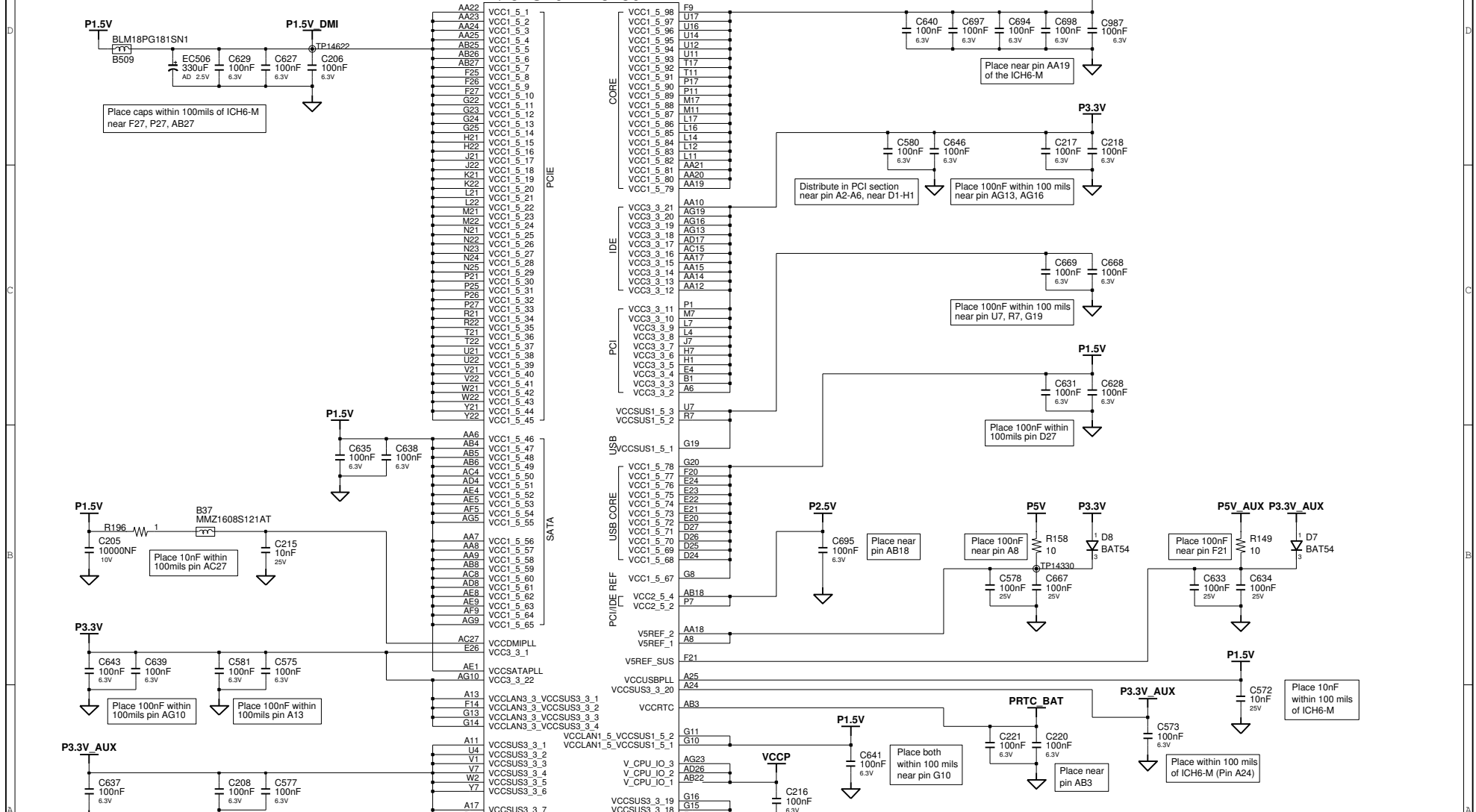
Table listing Clocks pins and their connections to external components like capacitors and resistors.

Table listing USB pins and their connections to external components like capacitors and resistors.

Revision control table with columns for DRAW, CHECK, APPROVAL, MODULE CODE, DATE, DEV. STEP, REV, LAST EDIT, TITLE, and PAGE.

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4 / 5 U10-4 82801FBM

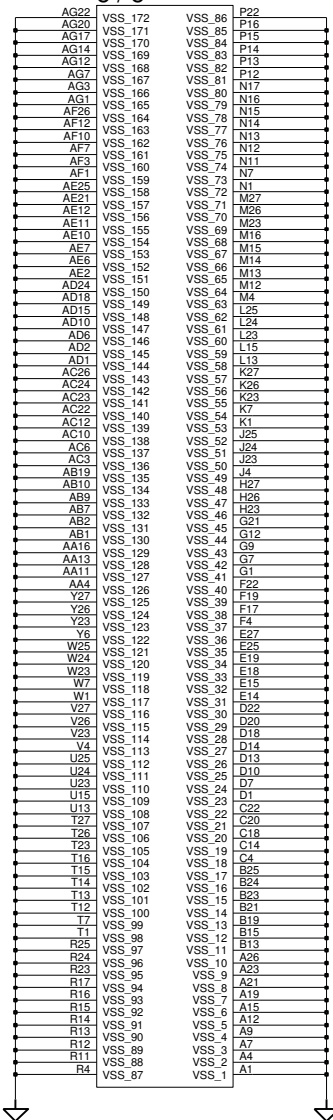


DRAW	Youngmo An	DATE	3/7/2006	TITLE	SantaFe	SAMSUNG ELECTRONICS
CHECK	HJ Kim	DEV. STEP	SR	MAIN		
APPROVAL	JS Euh	REV	0.9	ICH6 - M(3/4)	PART NO.	
MODULE CODE		LAST EDIT	March 7, 2006 12:22:03 PM	PAGE	17	OF 41

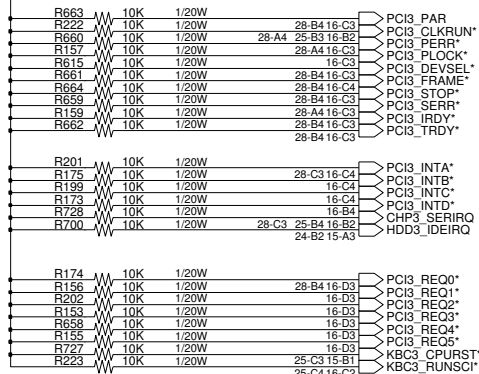
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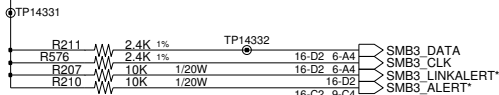
**U10-5
 82801FBM
 5 / 5**



P3.3V



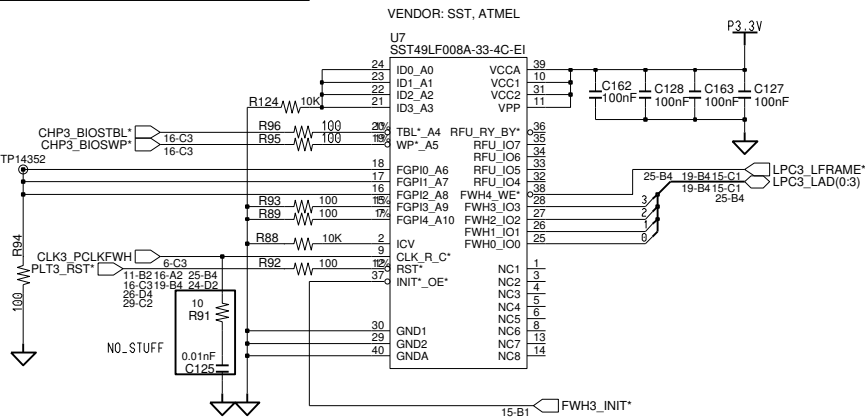
P3.3V_AUX



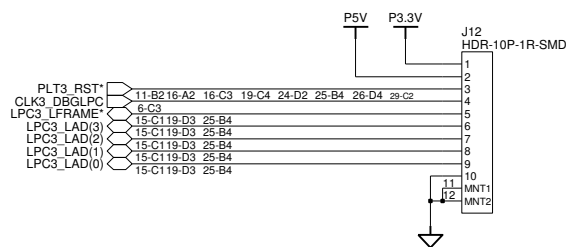
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APPROVAL	JS Euh	REV	0.9	ICH6 - M(4/4)		PART NO.
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80 Port



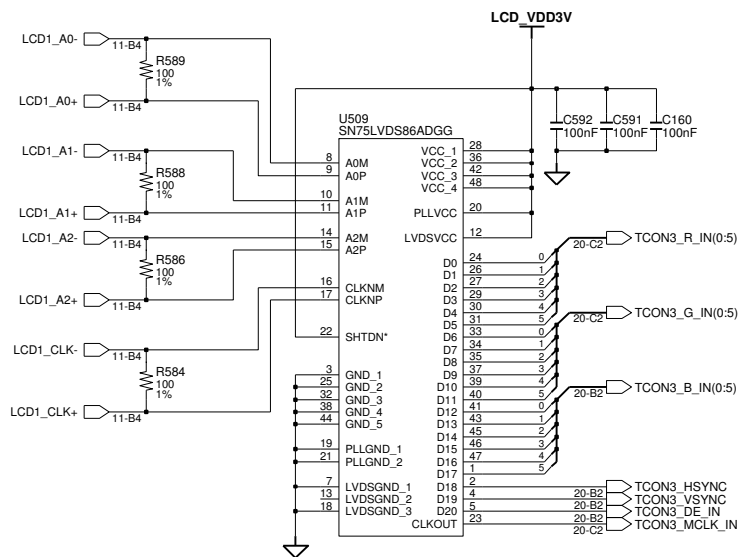
- 02 VERIFY REAL MODE
- 03 DISABLE NMI
- 04 GET CPU TYPE
- 06 INIT. SYSTEM H/W
- 08 INIT. CHIPSET REG.
- 09 SET IN POST FLAG
- 0A INIT CPU.REG
- 0B CPU CACHE ON
- 0C INIT.CACHE TO POST
- 0E INIT. I/O VALUE
- 0F ENABLE THE L-BUS IDE
- 10 INIT. POWER MANAGER
- 11 LOAD ALTERNATE REG.
- 13 PCI BUS MASTER RESET WITH INITIAL POST VALUE
- 14 INIT. KEYBOARD CONTROLLER
- 16 CHECK CHECKSUM
- 18 8254 TIMER INIT.
- 1A 8237 DMA CONTROLLER INIT.
- 1C RESET INTERRUPT CONTROLLER
- 20 TEST DRAM REFRESH
- 22 TEST 8742 KEYBOARD CONTROLLER
- 24 SET ES SEGMENT REG. TO 4GB
- 26 ENABLE A20
- 28 AUTO SIZING DRAM
- 32 COMPUTE THE CPU SPEED
- 34 TESET CMOS RAM
- 38 SHADOW SYSTEM BIOS ROM
- 3A AUTO SIZING CACHE
- 3C CONFIGURE ADVANCED CHIPSET REG.
- 3D LOAD ALTER REG. WITH CMOS VALUE
- 42 INIT. INTERRUPT VECTOR
- 44 INIT. BIOS INTERRUPT
- 46 CHECK ROM COPYRIGHT NOTICE
- 47 INIT. I20 SUPPORT IF INSTALLED
- 48 CHECK VIDEO CONFIGURE AGAINST CMOS
- 49 INIT. PCI BUS AND DEVICE
- 4A INIT. ALL VIDEO BIOS ROM
- 4C SHADOW VIDEO BIOS ROM
- 50 DISPLAY CPU TYPE AND SPEED
- 52 TEST KEYBOARD
- 54 SET KEYCLICK IF ENABLED
- 56 ENABLE KEYBOARD
- 58 TEST FOR UNEXPECTED INTERRUPTS
- 5A DISPLAY " PRESS SETUP"
- 5C TEST RAM BETWEEN 512K AND 640K
- 60 TEST EXTENDED MEMORY
- 62 TEST EXTENDED MEMORY ADDRESS LINE
- 64 JUMP TO USER PATCH 1
- 66 CONFIGURE ADVANCE CACHE REG.
- 6A DISPLAY EXTERNAL CACHE SIZE
- 6C DISPLAY SHADOW MESSAGE
- 6E DISPLAY NON-DISPOSABLE SEGMENT
- 70 DISPLAY ERROR MESSAGE
- 72 CHECK FOR CONFIGURATION ERROR
- 74 TEST REAL-TIME CLOCK
- 76 CHECK FOR KEYBOARD ERROR
- 7C SETUP HARDWARE INTERRUPT VECTOR
- 7E TEST COPROCESSER IF PRESENT
- 80 DISABLE ON-BOARD I/O PORT
- 82 DETECT AND INSTALL EXT.RS232C
- 84 DETECT AND INSTALL EXT.PARALLEL
- 86 RE-INIT. ON-BOARD I/O PORT
- 88 INIT. BIOS DATA ROM
- 8A INIT.EXTENDED BIOS DATA AREA
- 8C INIT. FDD CONTROLLER
- 9A SHADOW OPTION ROMS
- 9C SETUP POWER MANAGEMENT
- 9E ENABLE H/W INTERRUPT
- A0 SET TIME OF DAY
- A4 INIT. TYPOMATIC RATE
- A8 ERASE F2 PROMPT
- AA SCAN FOR F2 KEY STROKE
- AC ENTER SETUP
- AE CLEAR IN POST FLAG
- B0 CHECK FOR ERRORS
- B2 POST DONE-PREPARE TO BOOT 0/S
- B4 ONE BEEP
- B6 CHECK PASSWORD (OPTION)
- B7 ACPI INIT
- BA DMI INIT
- BE CLEAR SCREEN
- C0 TRY BOOT WITH INT19
- D0 INTERRUPT HANDLER ERROR
- D2 UNKNOWN INTERRUPT ERROR
- D4 PENDING INTERRUPT ERROR
- D6 SHUTDOWN 5
- D8 SHUTDOWN ERROR
- DA EXTENDED BLOCK MOVE
- DC SHUTDOWN 10
- 89 ENABLE NMI
- 90 INIT. HDD CONTROLLER
- 91 INIT. LOCAL BUS HDD CONTROLLER
- 92 JUMP TO USER PATCH 2
- 94 DISABLE A20 ADDRESS LINE
- 96 CLEAR HUGE ES SEGMENT REG.
- 98 SEARCH FOR OPTION ROMS

DRAW	Youngno An	DATE	3/7/2006	TITLE	SantaFe	SAMSUNG ELECTRONICS
CHECK	HJ Kim	DEV. STEP	SR		MAIN	
APPROVAL	JS Euh	REV	0.9		FWH & 80Port	PART NO.
MODULE CODE		LAST EDIT		March 7, 2006 12:22:03 PM	PAGE	19 OF 41

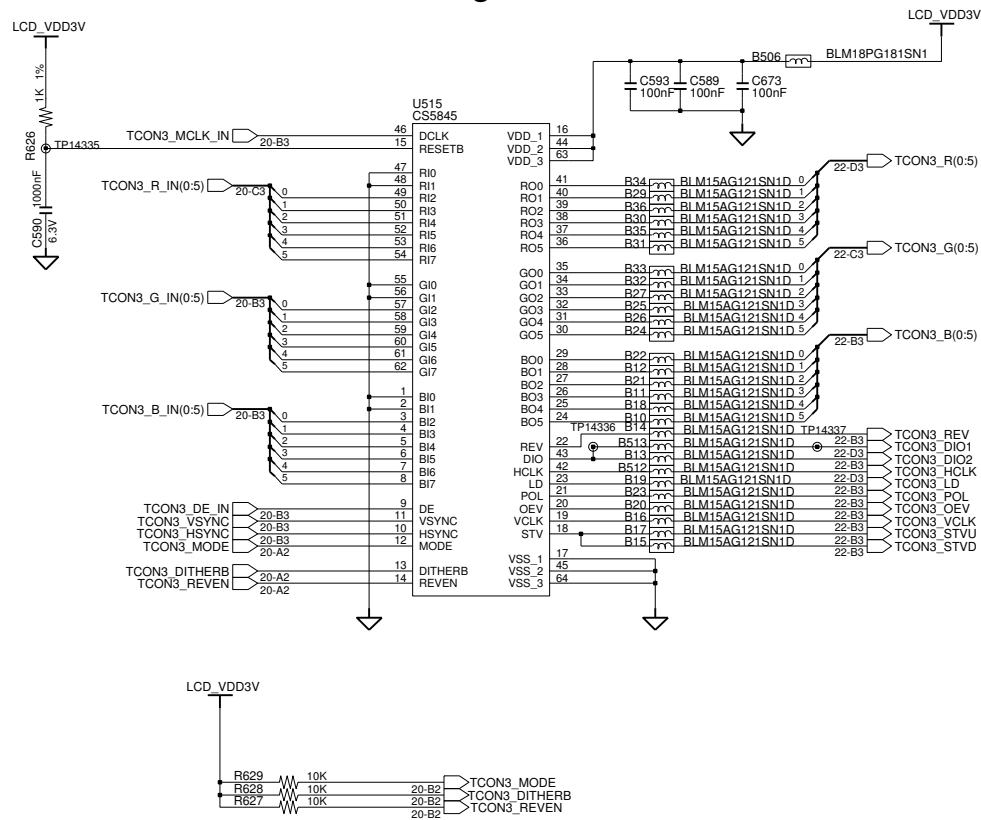
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LVDS to LVTTTL



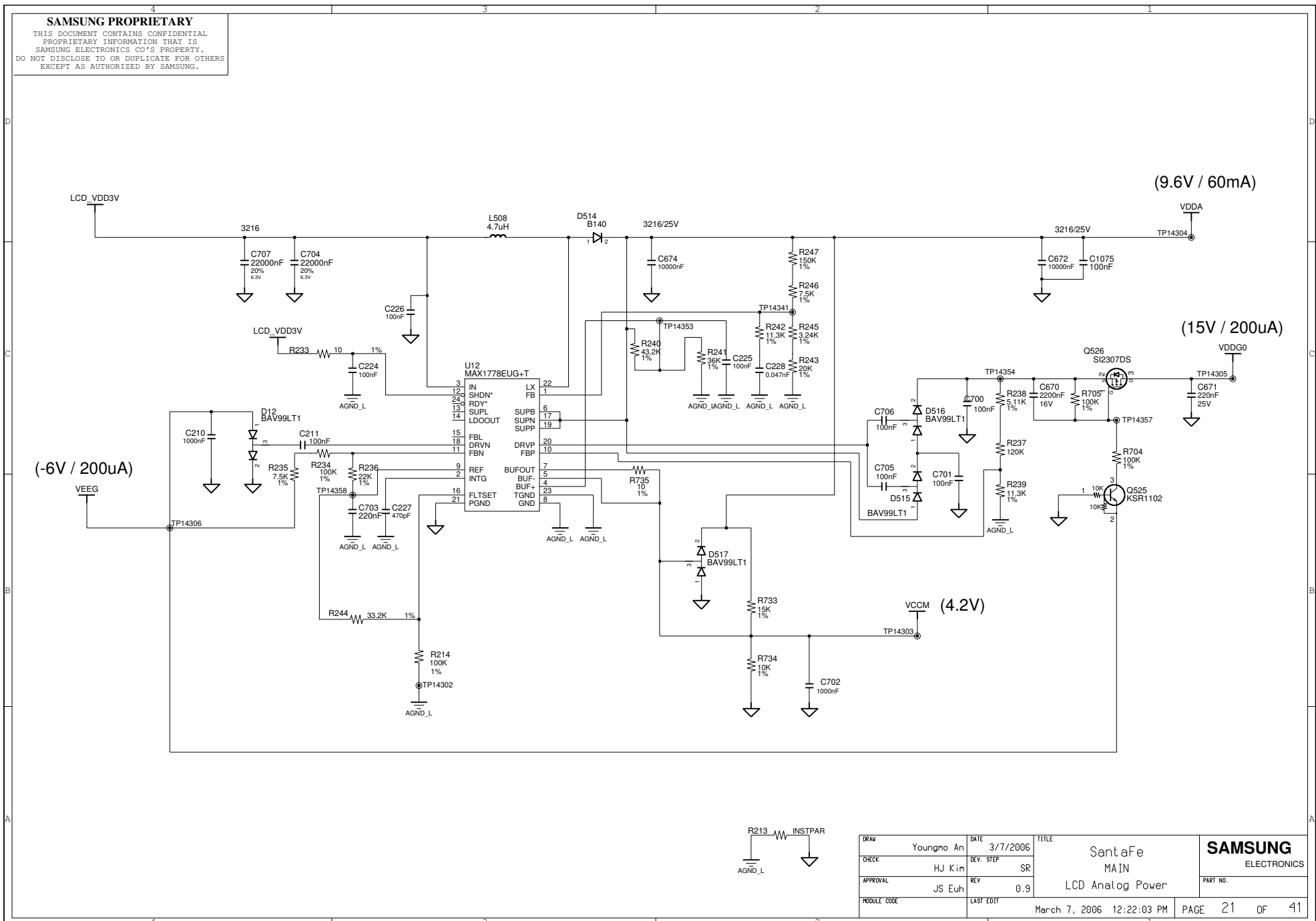
LCD Timing Controller



DRAW	Youngmo An	DATE	3/7/2006	TITLE	SantaFe MAIN LVDS TO LVTTTL & Tcon	SAMSUNG ELECTRONICS PART NO.
CHECK	HJ Kim	DEV. STEP	SR			
APPROVAL	JS Euh	REV	0.9			
MODULE CODE		LAST EDIT				

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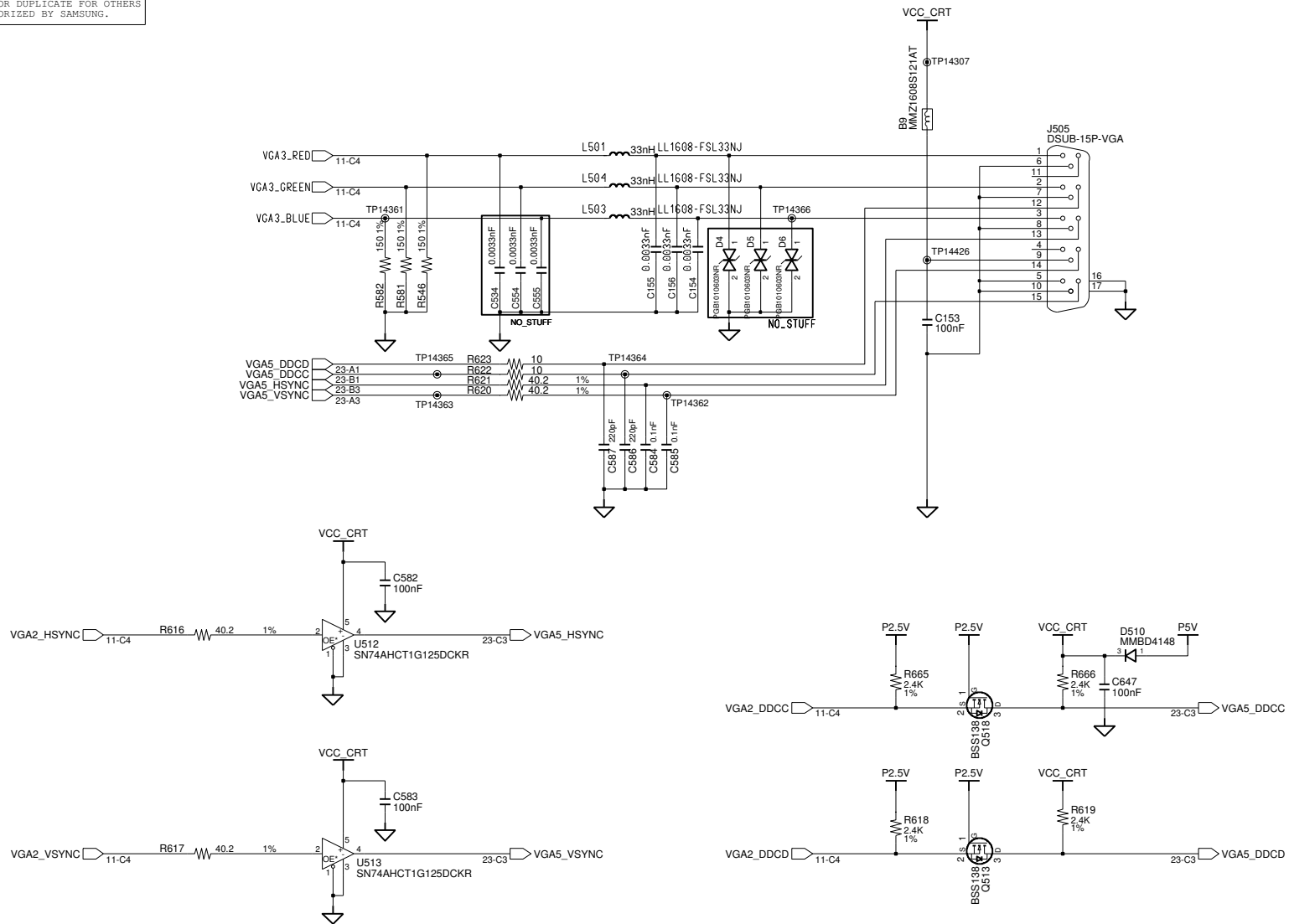
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DRAW	Youngmo An	DATE	3/7/2006	TITLE	SantaFe MAIN LCD Analog Power	SAMSUNG ELECTRONICS
CHECK	HJ Kim	DEV. STEP	SR	PART NO.		
APPROVAL	JS Euh	REV	0.9	March 7, 2006 12:22:03 PM		PAGE 21 OF 41
MODULE CODE		LAST EDIT				

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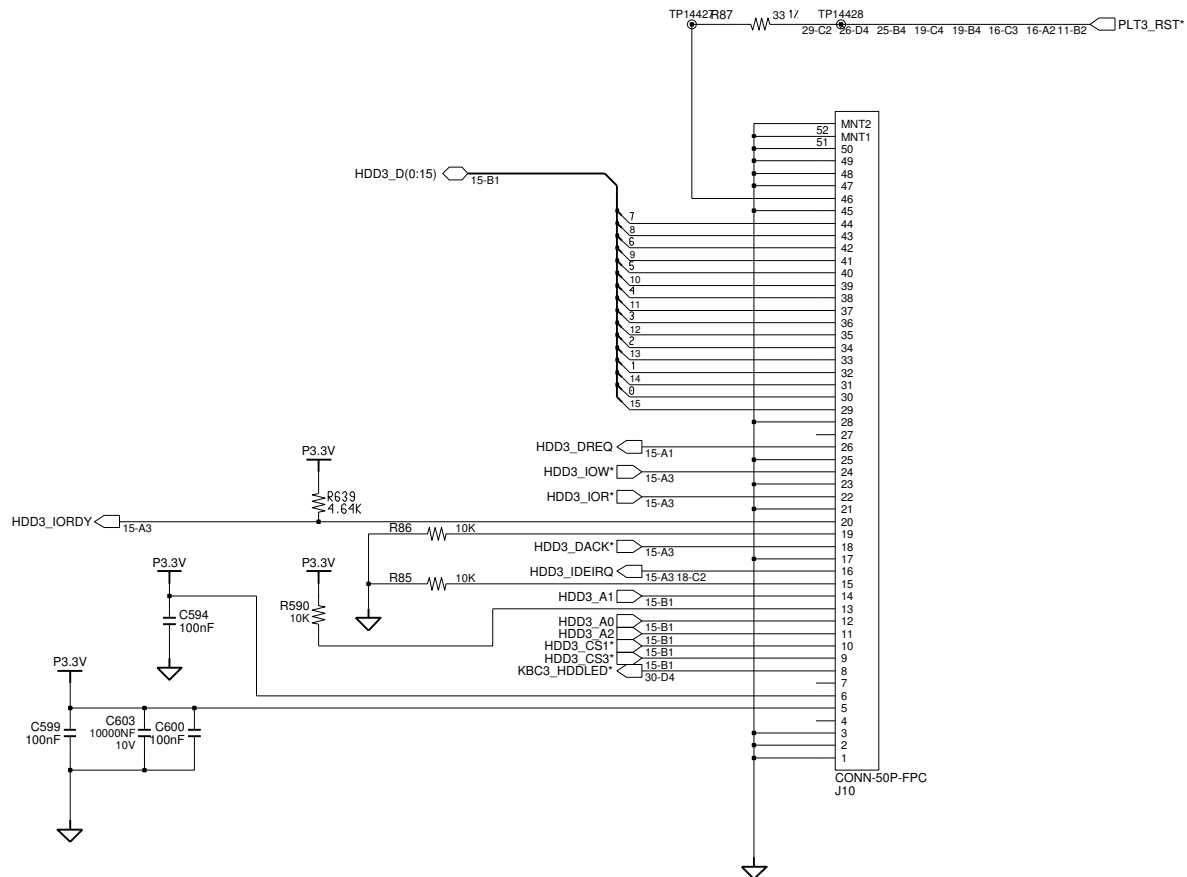
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DRAW	Youngmo An	DATE	3/7/2006	TITLE	SantaFe MAIN VGA Level Shift	SAMSUNG ELECTRONICS
CHECK	HJ Kim	DEV. STEP	SR	PART NO.		
APPROVAL	JS Euh	REV	0.9	March 7, 2006 12:22:03 PM		PAGE 23 OF 41
MODULE CODE		LAST EDIT				

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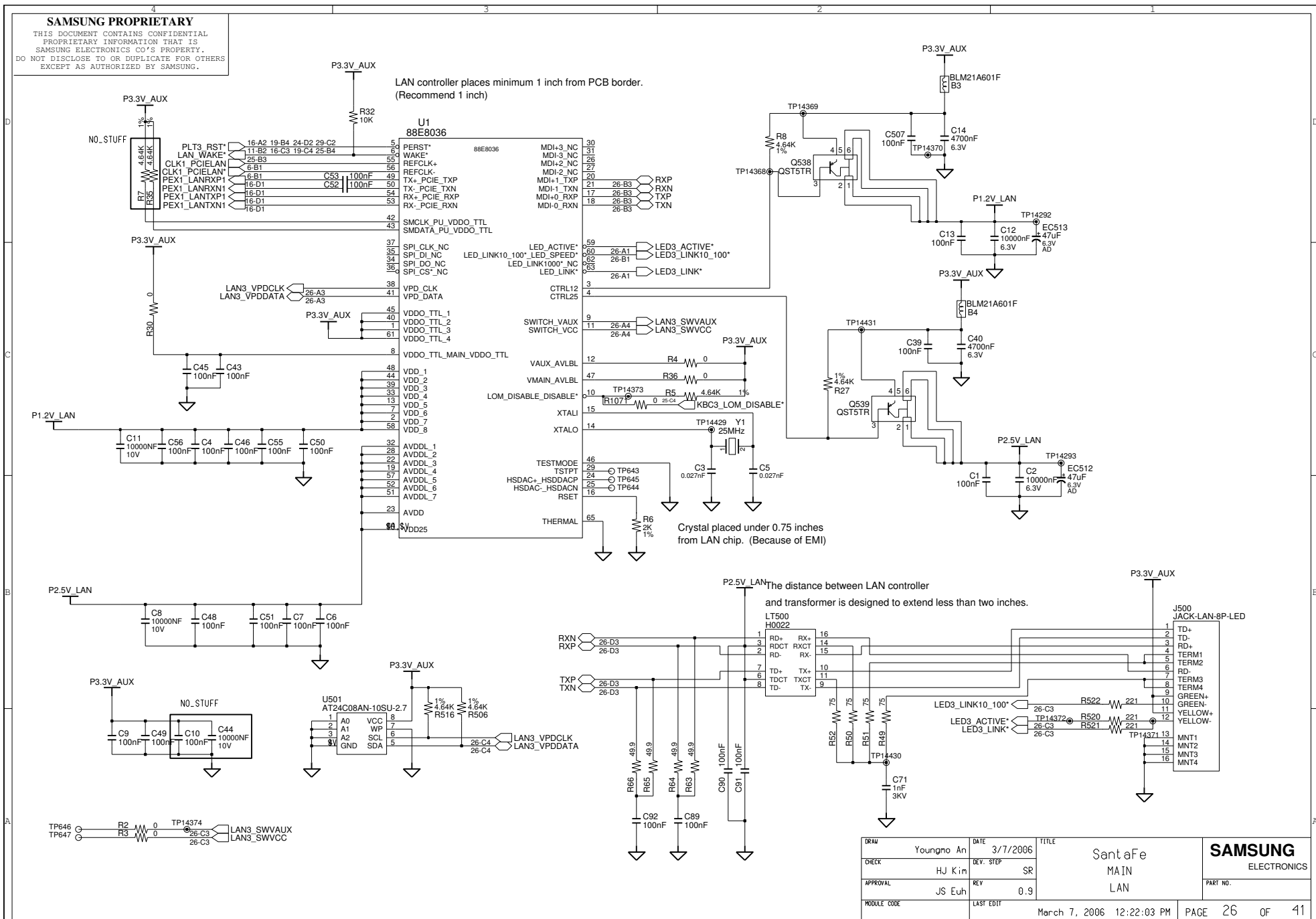
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DRAW	Youngmo An	DATE	3/7/2006	TITLE	SantaFe MAIN HDD CONNECTOR	SAMSUNG ELECTRONICS
CHECK	HJ Kim	DEV. STEP	SR	PART NO.		
APPROVAL	JS Euh	REV	0.9			
MODULE CODE		LAST EDIT	March 7, 2006 12:22:03 PM	PAGE 24 OF 41		

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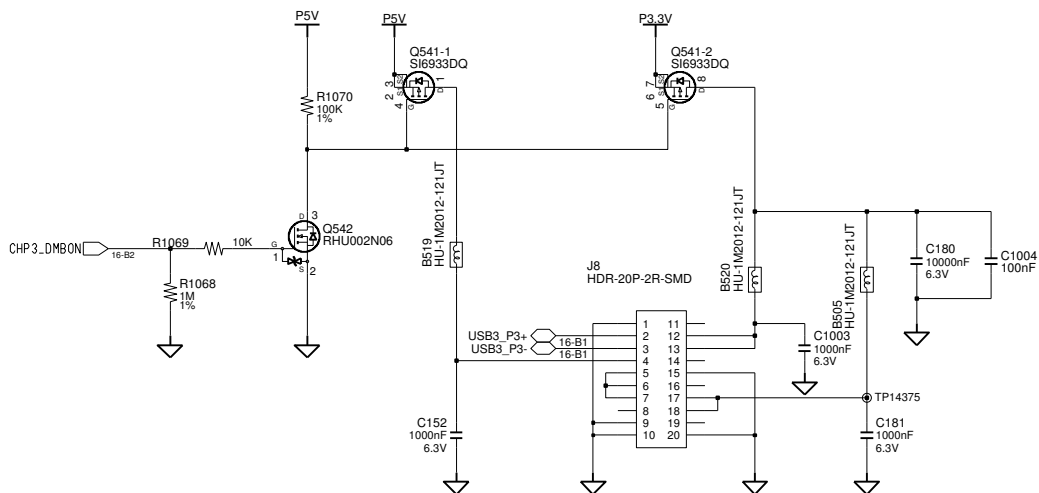


DRAW	Youngmo An	DATE	3/7/2006	TITLE	SantaFe MAIN LAN	SAMSUNG ELECTRONICS PART NO.
CHECK	HJ Kim	DEV. STEP	SR			
APPROVAL	JS Euh	REV	0.9			
MODULE CODE		LAST EDIT				
March 7, 2006 12:22:03 PM						PAGE 26 OF 41

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DMB Connector & Pem(5mm Height)

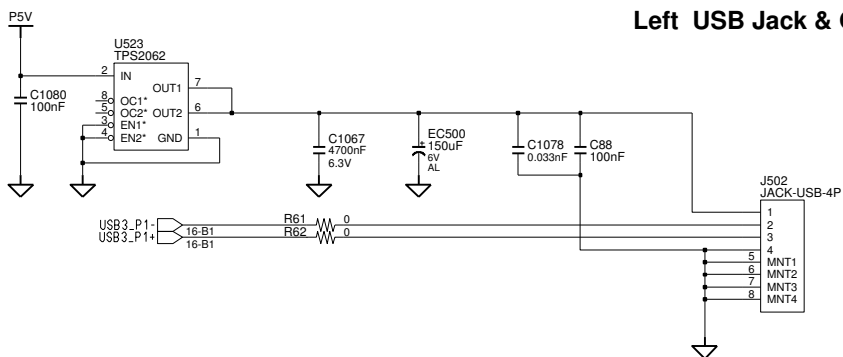


3711-005979

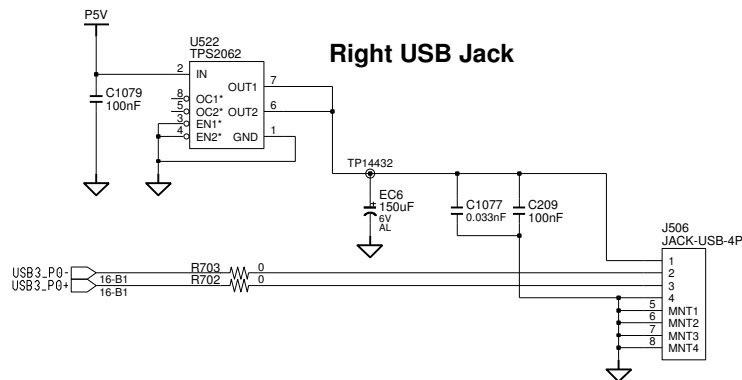


BA81-00730A

Left USB Jack & ODD Power Jack



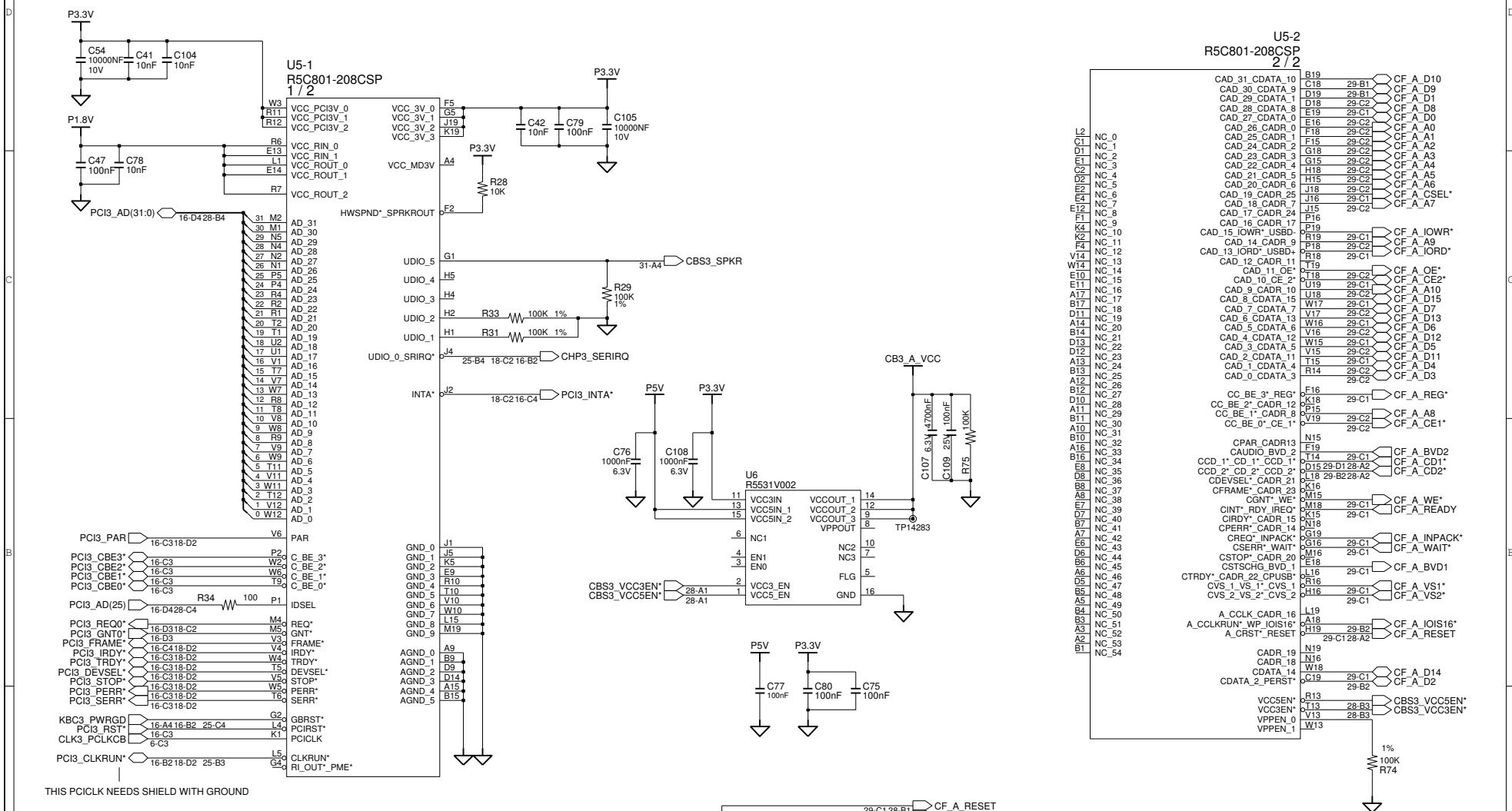
Right USB Jack



DRAW	Youngmo An	DATE	3/7/2006	TITLE	SantaFe MAIN DMB & USB	SAMSUNG ELECTRONICS
CHECK	HJ Kim	DEV. STEP	SR	PART NO.		
APPROVAL	JS Euh	REV	0.9			
MODULE CODE		LAST EDIT	March 7, 2006 12:22:03 PM	PAGE 27 OF 41		

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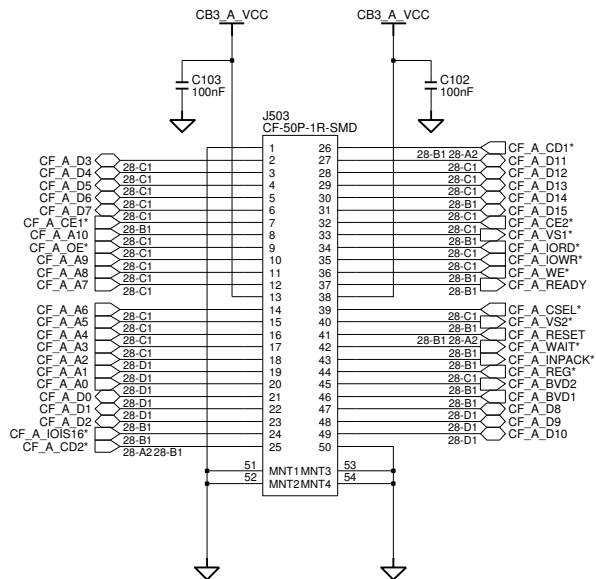
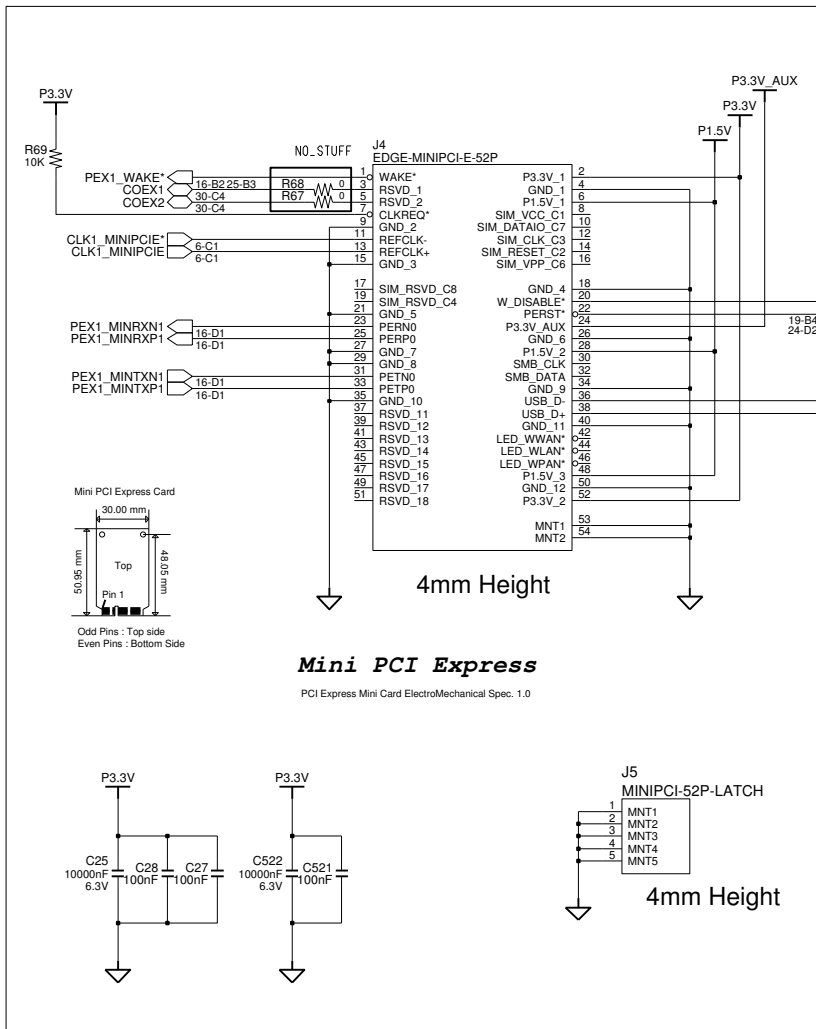
THIS PCI3_CLKRUN* NEEDS SHIELD WITH GROUND

DRAW	Youngmo An	DATE	3/7/2006	TITLE	SantaFe MAIN Cardbus controller	SAMSUNG ELECTRONICS PART NO.
CHECK	HJ Kim	DEV. STEP	SR			
APPROVAL	JS Euh	REV	0.9			
MODULE CODE		LAST EDIT				
				March 7, 2006 12:22:03 PM	PAGE 28 OF 41	

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CF SLOT

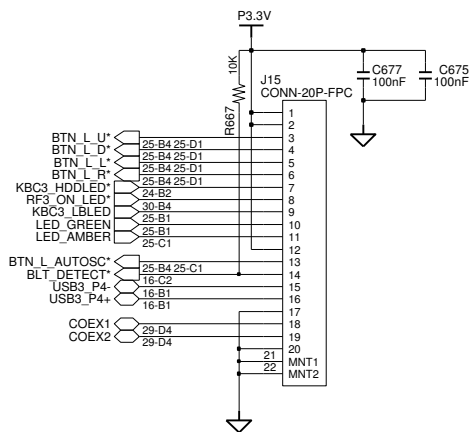


DRAW	Youngno An	DATE	3/7/2006	TITLE	SantaFe MAIN Mini Card & CF Slot	SAMSUNG ELECTRONICS PART NO.
CHECK	HJ Kim	DEV. STEP	SR			
APPROVAL	JS Euh	REV	0.9			
MODULE CODE		LAST EDIT				
				March 7, 2006 12:22:03 PM	PAGE	29 OF 41

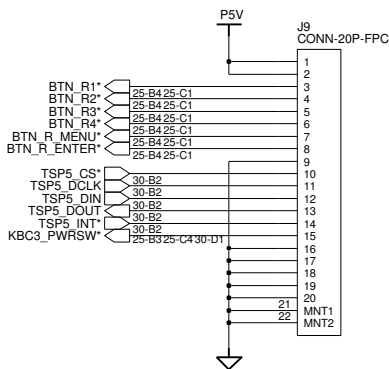
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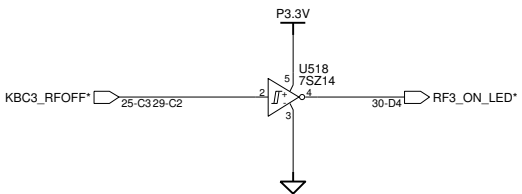
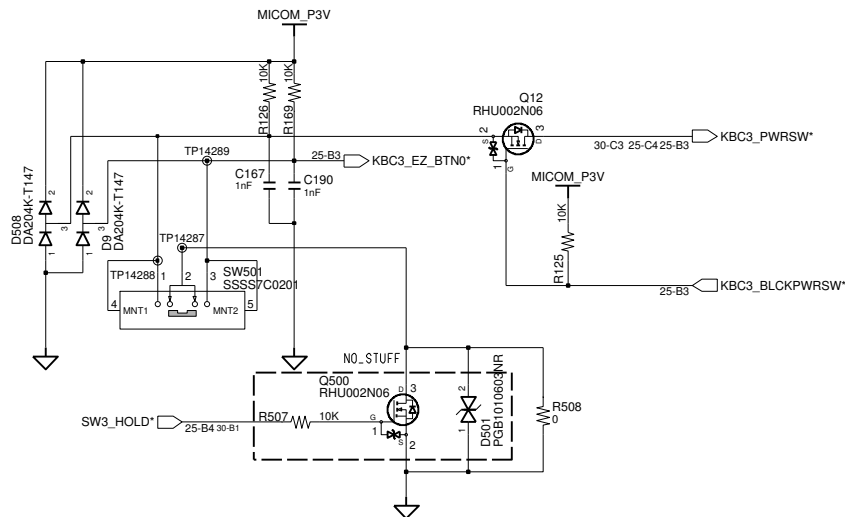
Main to Subboard(Left)



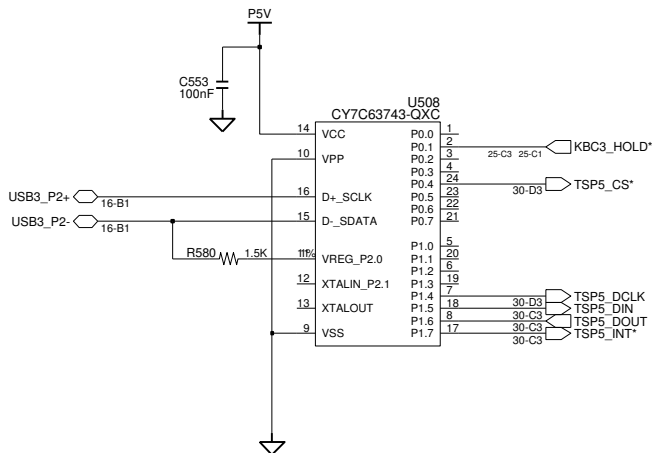
Main to Subboard(Right)



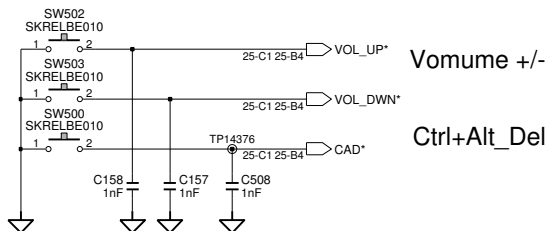
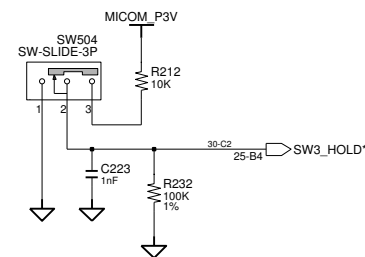
POWER & MIO S/W



TSP



HOLD S/W

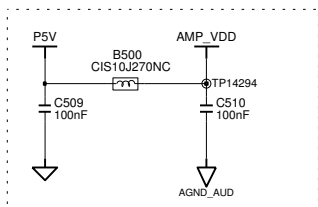


DRAW	Youngmo An	DATE	3/7/2006	TITLE	SantaFe	SAMSUNG ELECTRONICS
CHECK	HJ Kim	DEV. STEP	SR	MAIN		
APPROVAL	JS Euh	REV	0.9	TSP & SUB B'D Conn. & S/W		PART NO.
MODULE CODE		LAST EDIT	March 7, 2006 12:22:03 PM	PAGE	30	OF 41

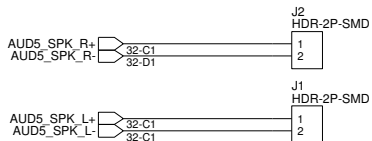
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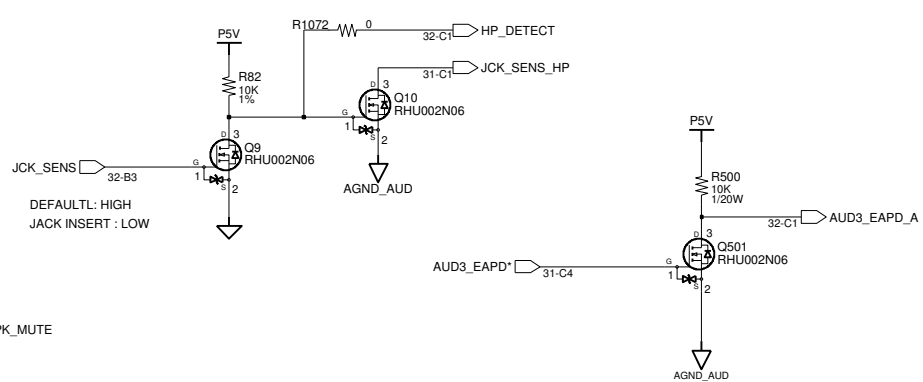
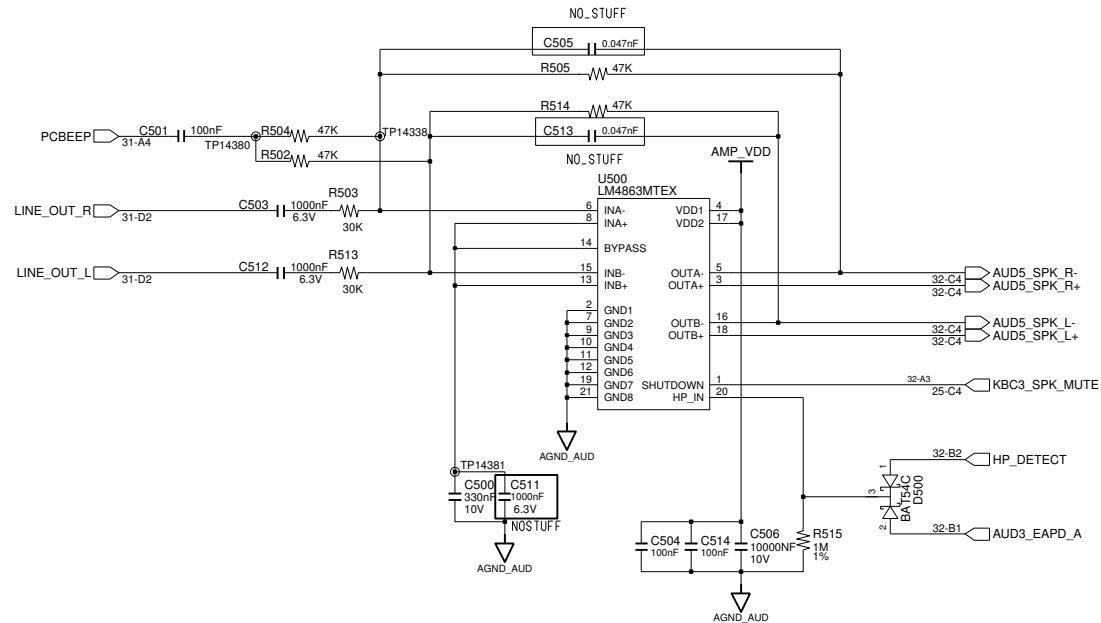
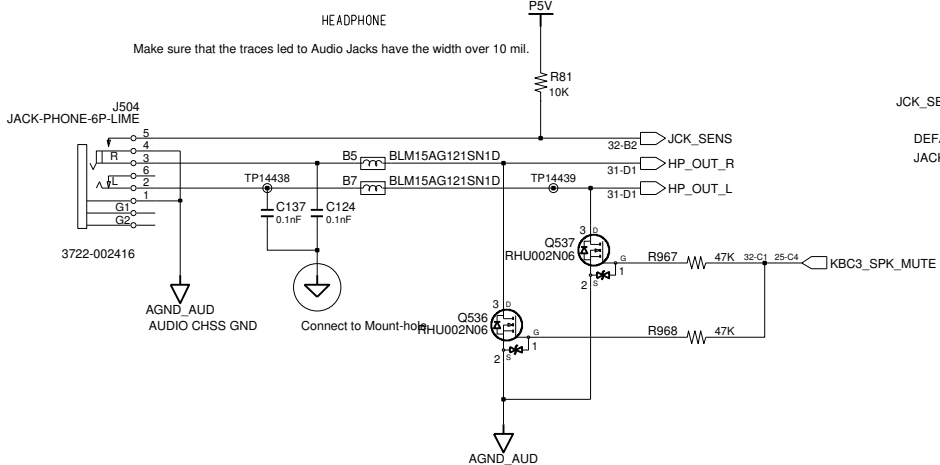
AMP_VDD



INTERNAL STEREO SPEAKERS



3711-005752

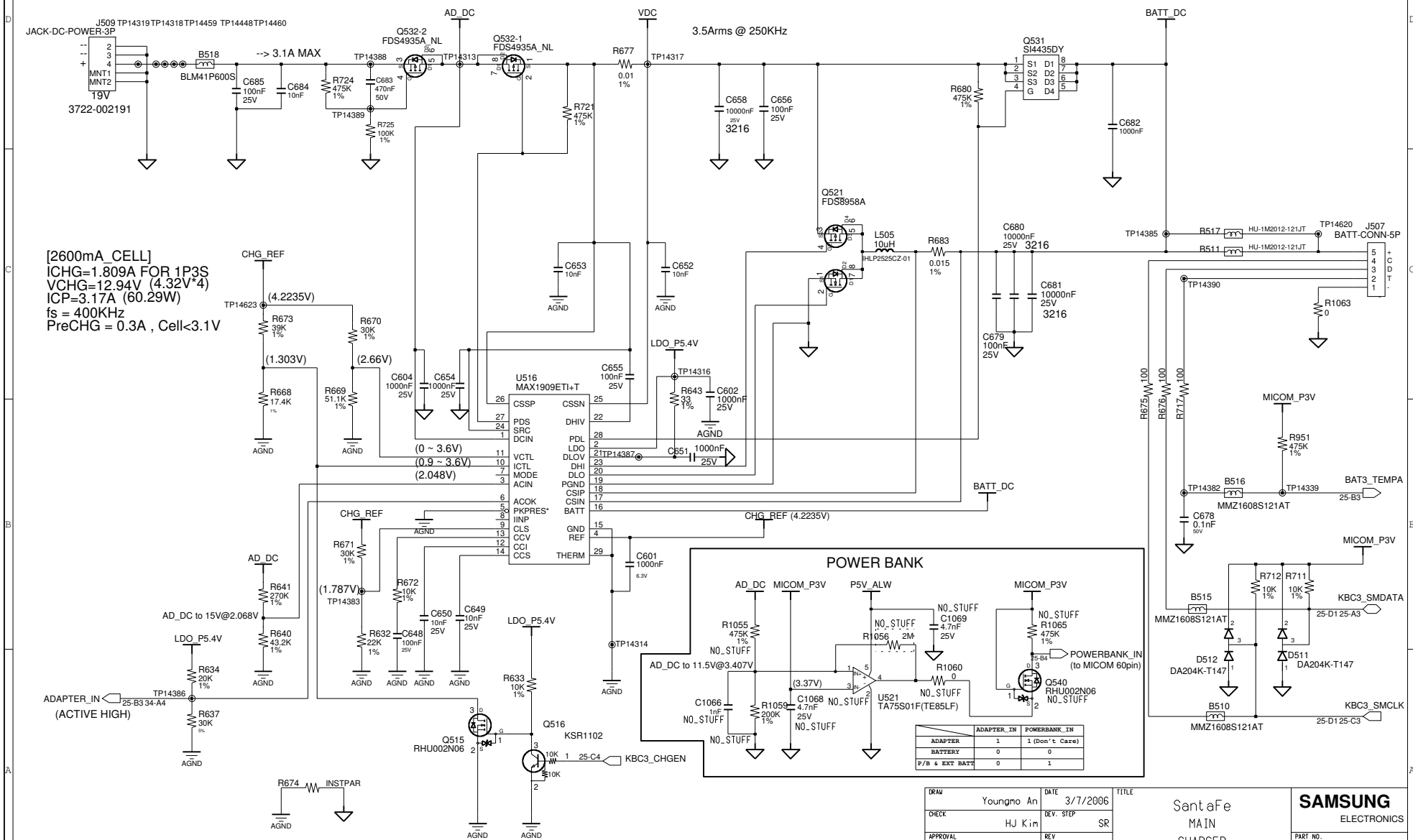


DRAW	Youngmo An	DATE	3/7/2006	TITLE	SantaFe MAIN	SAMSUNG ELECTRONICS
CHECK	HJ Kim	DEV. STEP	SR	AMP & Spkr Conn & HP Jack		
APPROVAL	JS Euh	REV	0.9	PART NO.		
MODULE CODE		LAST EDIT	March 7, 2006 12:22:03 PM	PAGE	32	OF 41

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CHARGER & POWER MANAGEMENT



[2600mA_CELL]
 ICHG=1.809A FOR 1P3S
 VCHG=12.94V (4.32V*4)
 ICP=3.17A (60.29W)
 fs = 400KHz
 PreCHG = 0.3A , Cell<3.1V

POWER BANK

ADAPTER_IN	POWERBANK_IN
ADAPTER	1 (Don't Care)
BATTERY	0
P/B & EXT BATT	0 1

DRAW	Youngmo An	DATE	3/7/2006	TITLE
CHECK	HJ Kim	DEV. STEP	SR	
APPROVAL	JS Euh	REV	0.9	
MODULE CODE		LAST EDIT		

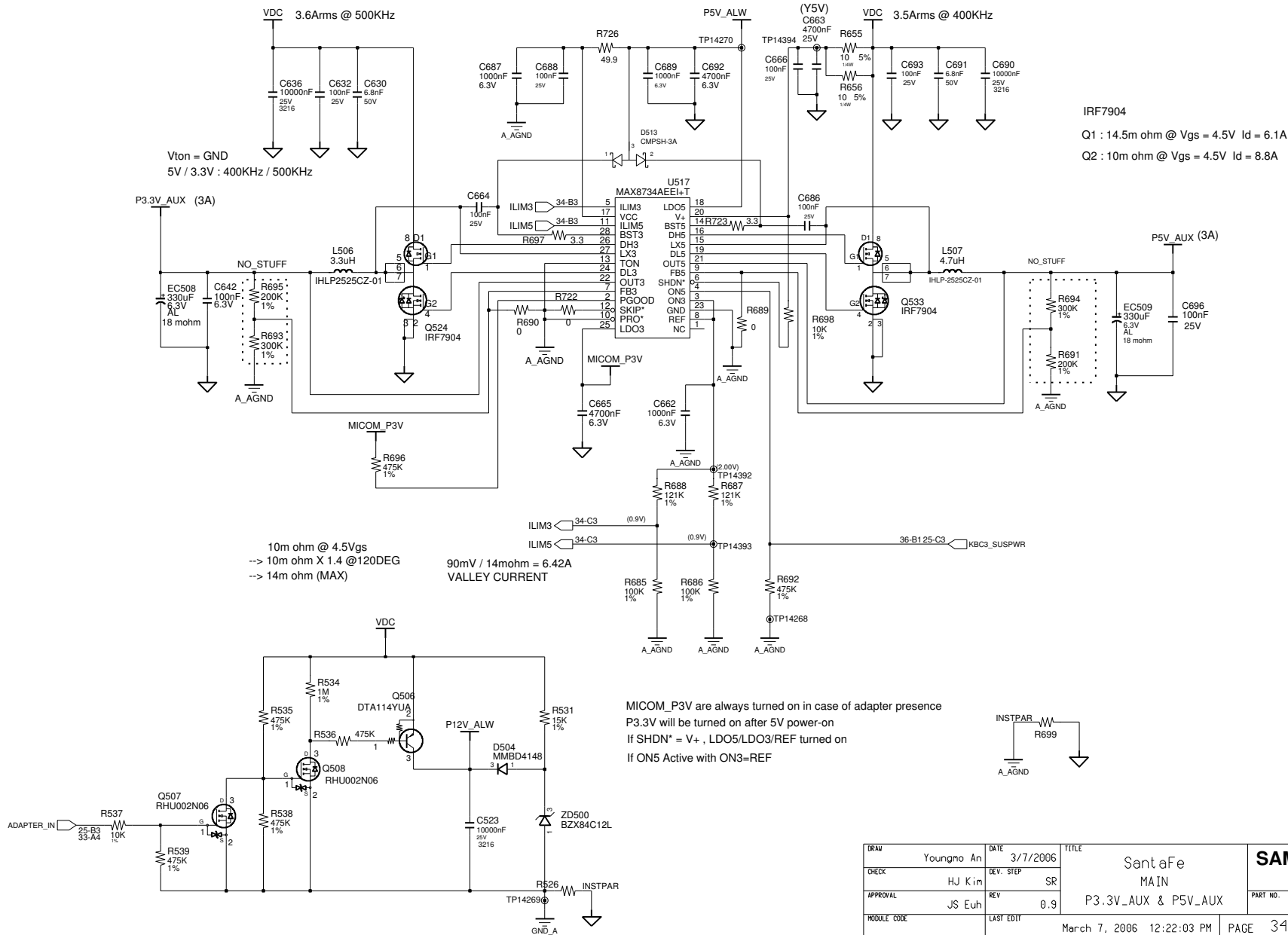
SantaFe
 MAIN
 CHARGER

SAMSUNG
 ELECTRONICS
 PART NO.

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P3.3V_AUX & P5V_AUX & MICOM_P3V

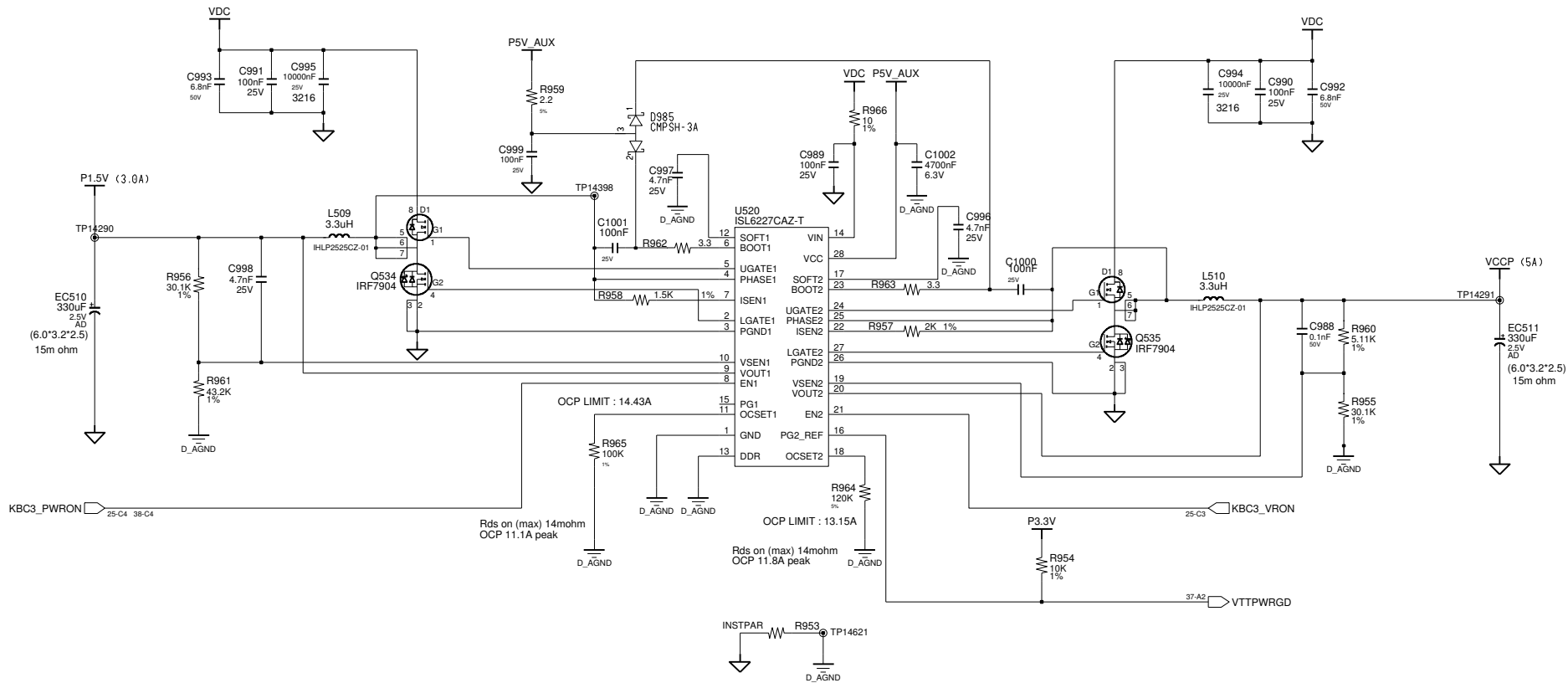


DRAW	Youngmo An	DATE	3/7/2006	TITLE	SantaFe MAIN P3.3V_AUX & P5V_AUX	SAMSUNG ELECTRONICS
CHECK	HJ Kim	DEV. STEP	SR	PART NO.		
APPROVAL	JS Euh	REV	0.9			
MODULE CODE		LAST EDIT	March 7, 2006 12:22:03 PM	PAGE	34	OF 41

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P1.5V & VCCP (1.05V)

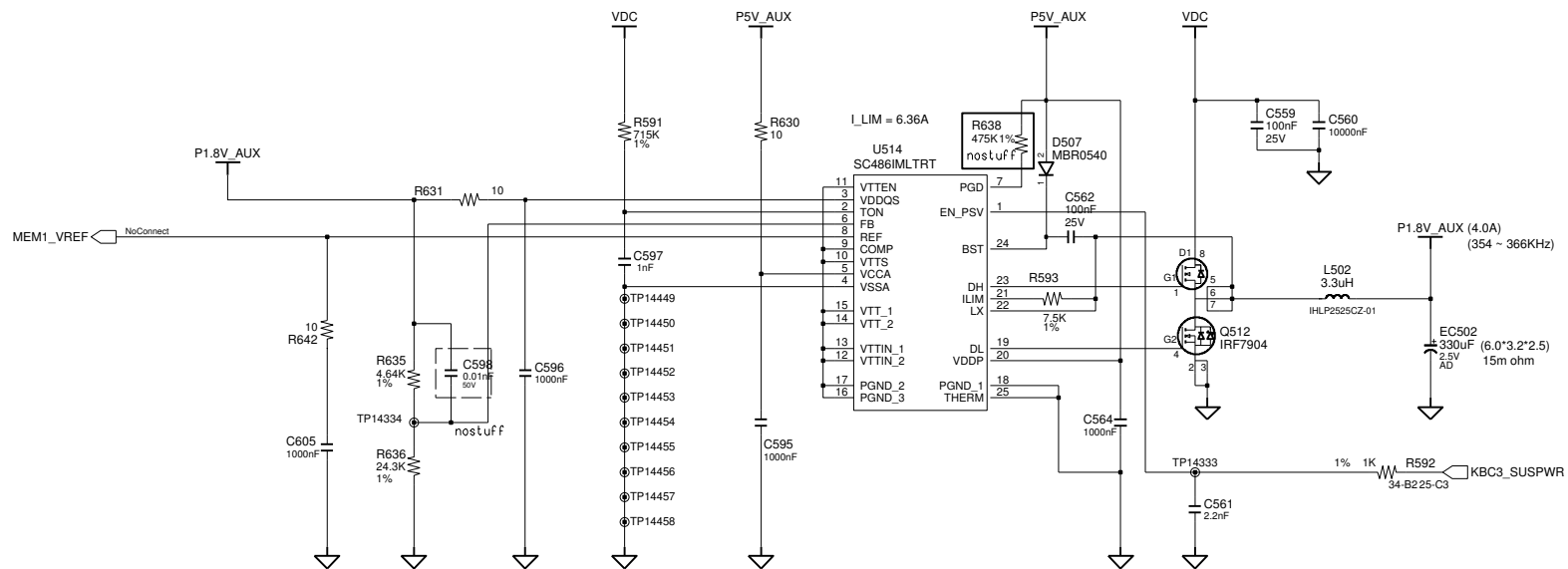


DRAW	Youngmo An	DATE	3/7/2006	TITLE	SantaFe MAIN P1.5V & VCCP	SAMSUNG ELECTRONICS
CHECK	HJ Kim	DEV. STEP	SR	PART NO.		
APPROVAL	JS Euh	REV	0.9			
MODULE CODE		LAST EDIT	March 7, 2006 12:22:03 PM	PAGE 35 OF 41		

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DDR2 Power

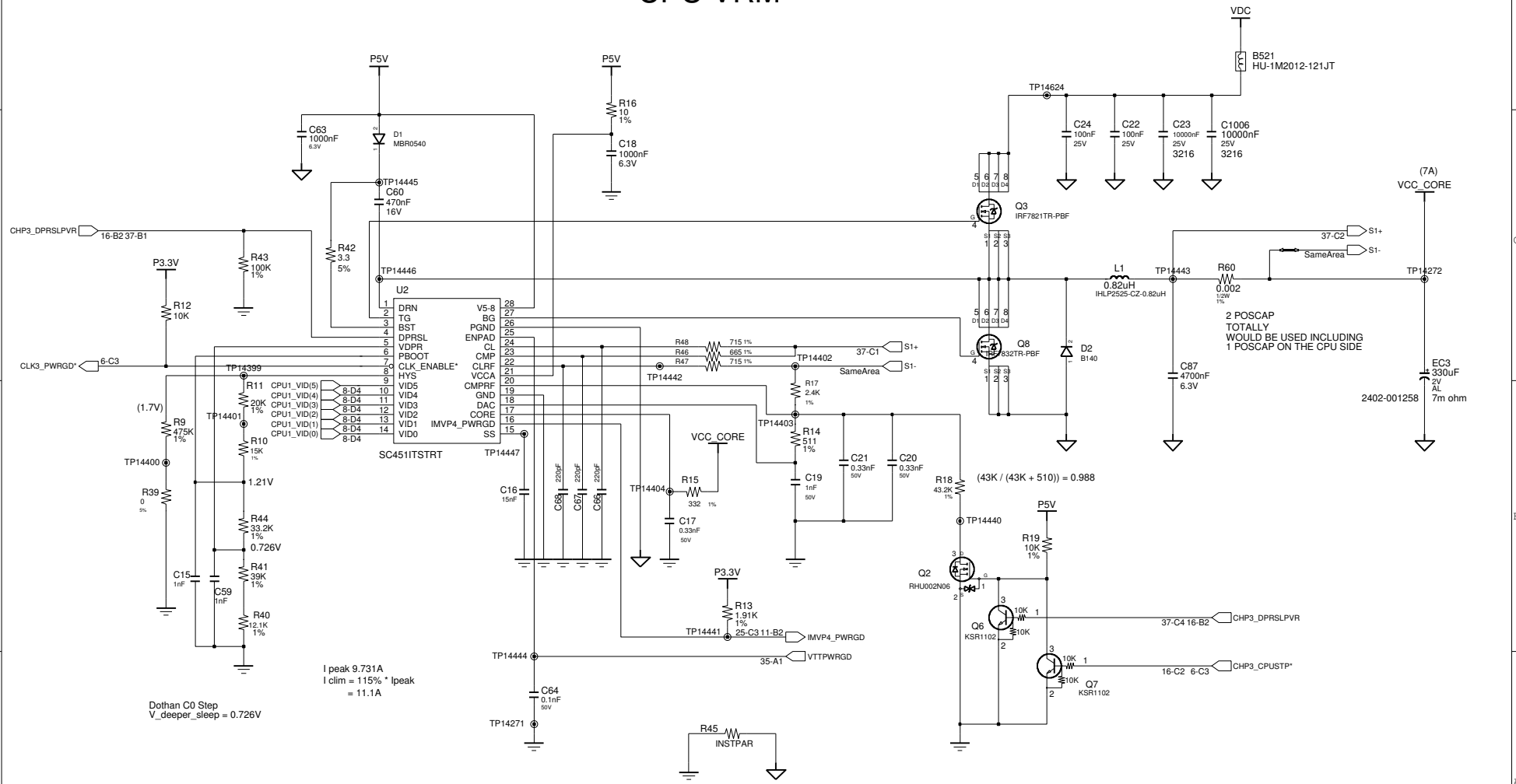


DRAW	Youngmo An	DATE	3/7/2006	TITLE	SantaFe MAIN DDR2 POWER	SAMSUNG ELECTRONICS PART NO.
CHECK	HJ Kim	DEV. STEP	SR			
APPROVAL	JS Euh	REV	0.9			
MODULE CODE		LAST EDIT	March 7, 2006 12:22:03 PM			
				PAGE	36	OF 41

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CPU VRM



Dothan C0 Step
V_deeper_sleep = 0.726V

I_peak 9.731A
I_clim = 115% * I_peak
= 11.1A

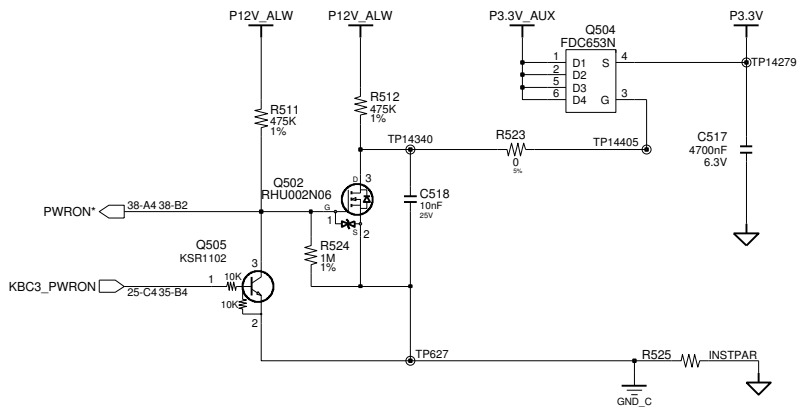
2 POSCAP
TOTALLY
WOULD BE USED INCLUDING
1 POSCAP ON THE CPU SIDE

DRAW	Youngmo An	DATE	3/7/2006	TITLE	SantaFe MAIN CPU VRM	SAMSUNG ELECTRONICS
CHECK	HJ Kim	DEV. STEP	SR			
APPROVAL	JS Euh	REV	0.9			PART NO.
MODULE CODE		LAST EDIT	March 7, 2006 12:22:03 PM	PAGE	37	OF 41

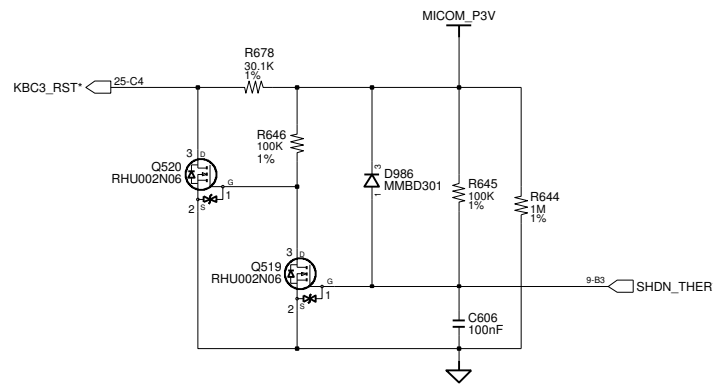
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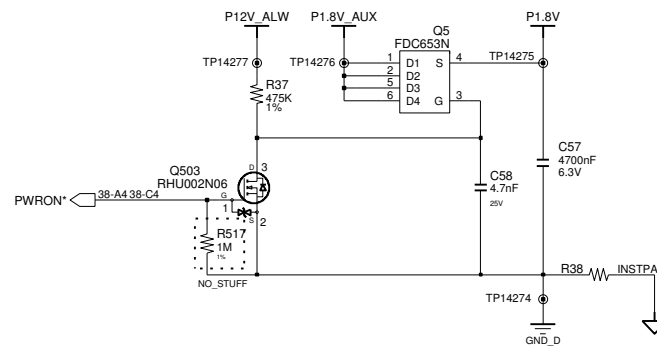
Switched Power On (P3.3V)



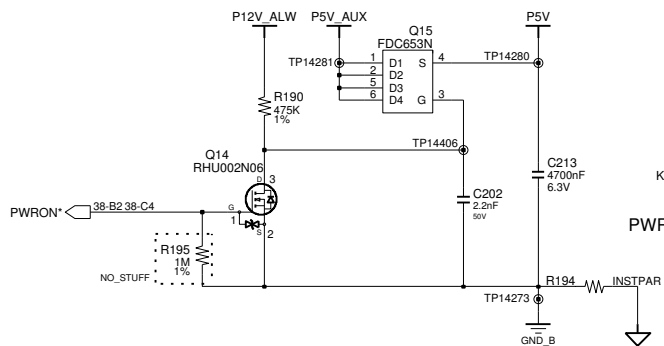
MICOM RESET



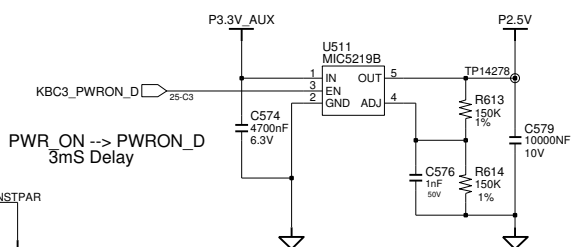
Switched Power On (P1.8V)



Switched Power On (P5V)



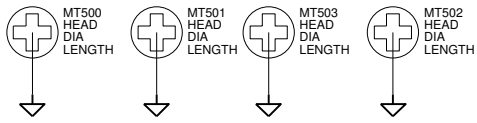
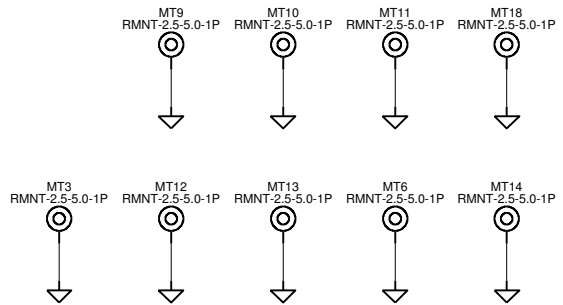
Switched Power On (P2.5V)



DRAW	Youngmo An	DATE	3/7/2006	TITLE	SantaFe MAIN Switched Power	SAMSUNG ELECTRONICS
CHECK	HJ Kim	DEV. STEP	SR			
APPROVAL	JS Euh	REV	0.9			PART NO.
MODULE CODE		LAST EDIT	March 7, 2006 12:22:03 PM	PAGE	38	OF 41

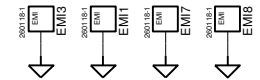
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RHE PEM(2mm): BA61-00955A

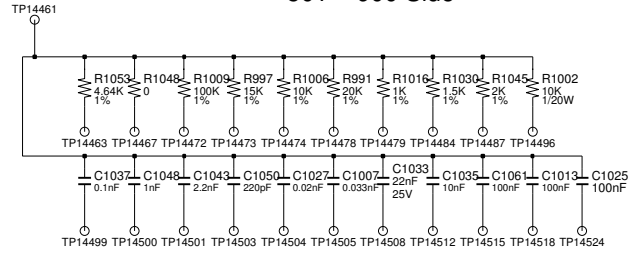
EMI FINGER : 005299021



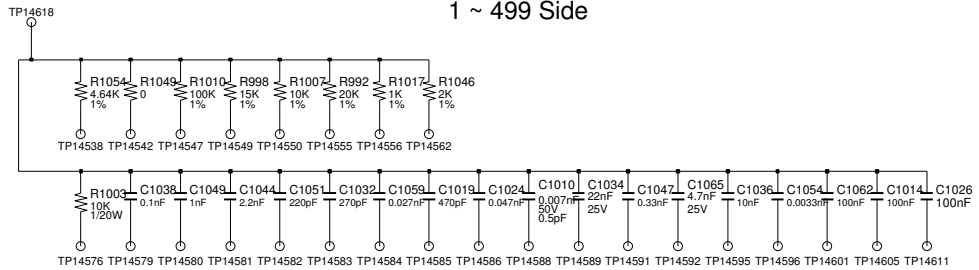
PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/D)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

REV500
1 O
2 O O3

501 ~ 900 Side



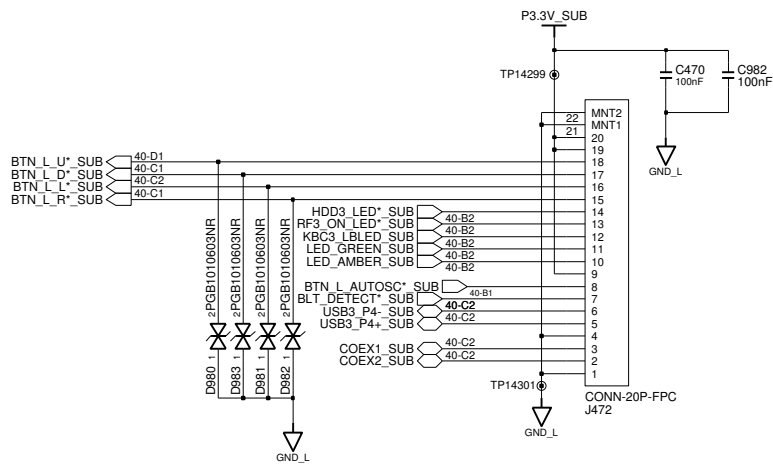
1 ~ 499 Side



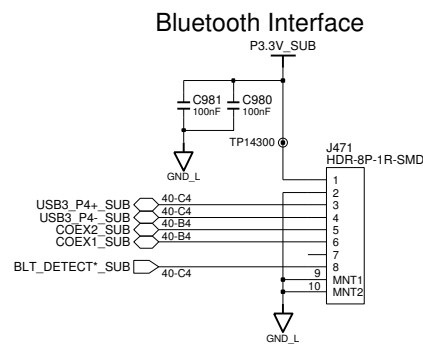
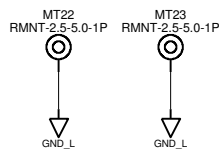
DRAW	Youngmo An	DATE	3/7/2006	TITLE	Sant aFe MAIN Mount Hole	SAMSUNG ELECTRONICS
CHECK	HJ Kim	DEV. STEP	SR	PART NO.		
APPROVAL	JS Euh	REV	0.9			
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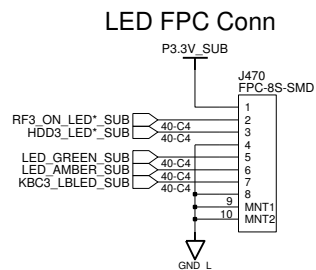
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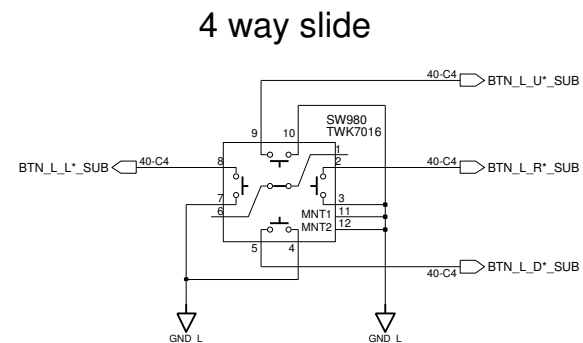
Main to Subboard(Left)



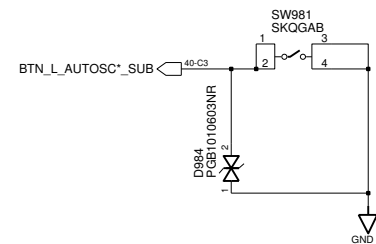
Bluetooth Interface



LED FPC Conn



4 way slide

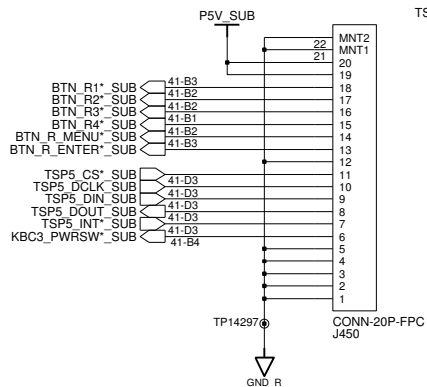


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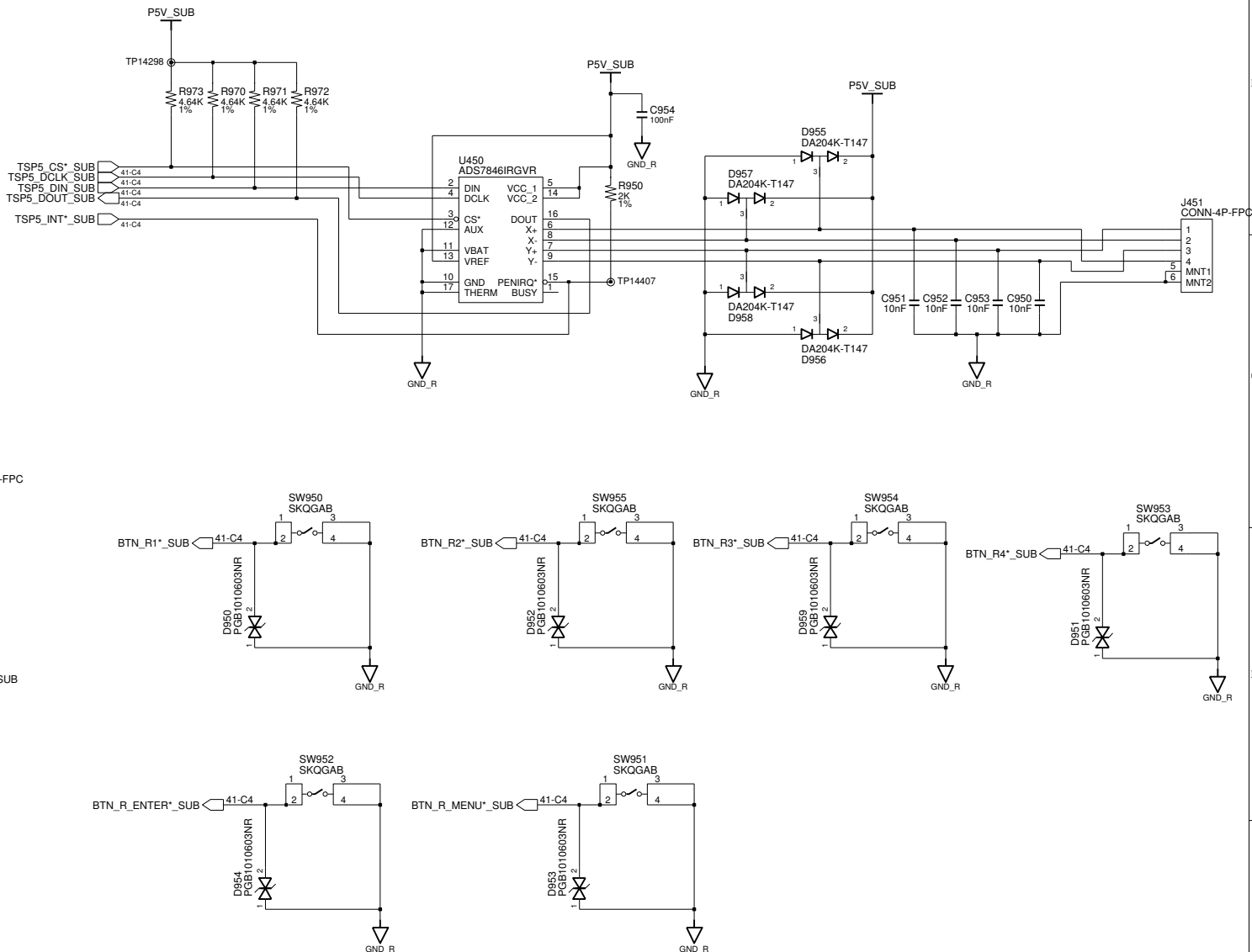
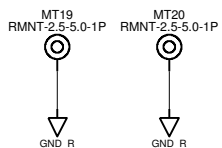
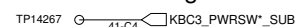
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**Top contact
Main to Subboard(Right)**



For FCT Jig



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