sun microsystems

Sun-2/50
Field Service Manual

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Contents

Preface

The Sun-2/50 is a microprocessor-based workstation, capable of operating stand-alone or as part of a local area network. Offering 1Mbyte of dynamic memory in its standard configuration, the Sun-2/50 may be expanded to a maximum of 4Mbytes with the addition of one of several memory expansion boards. Memory architecture, based on the concepts of virtual memory, provides access to significantly greater amounts of data storage than is resident on the workstation itself; while integral Ethernet, RS-423 and VME bus interfaces supply data links to a number of systems environments.

The information presented in this manual is designed to give the reader some insight into the workings of Sun-2/50 logic, provide assistance in troubleshooting problems and, finally, offer step-by-step procedures for the removal and replacement of system components. Figure 1-1 provides an overview of the Sun-2/50 in a typical system environment.

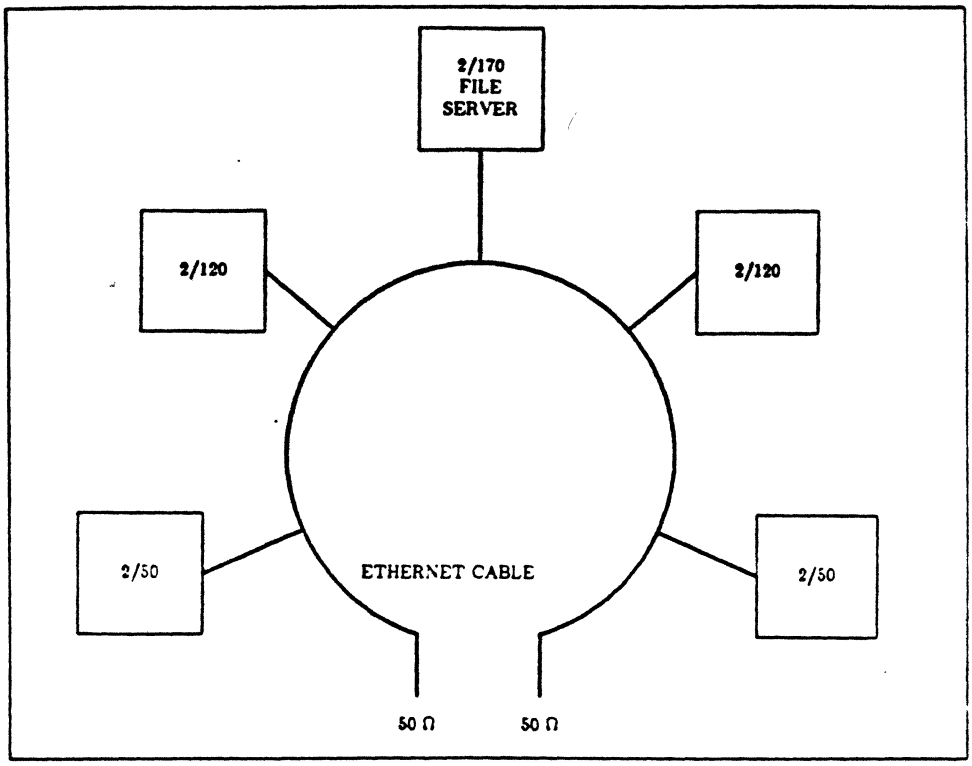


Figure 0-1 *Sun-2/50 System Overview*

Assumptions About Reader Knowledge

In presenting the information contained in this manual, it is assumed that the reader is familiar with TTL and ECL logic, and with the Motorola MC68010 Microprocessor. The reader should also have a working knowledge of Local Area Networks, Sun-2 virtual memory management architecture and the VME bus specification.

List of Applicable Documents

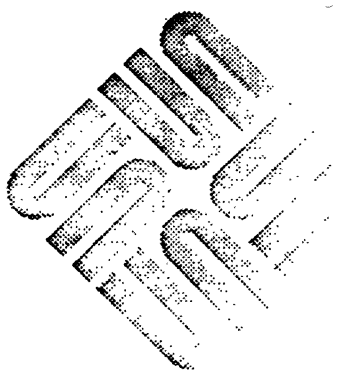
This list provides additional sources of information to be used in conjunction with the Sun-2/50 Service Manual.

- Motorola MC68010 Databook (Motorola P/N ADI 942)
- Hardware Installation Manual for the Sun-2/50 Desktop SunStation (Sun P/N 800-1143-01)
- VMEbus Specification Manual (VME Manufacturers Group, Rev. B,Aug. 1982)
- Moniterm Monitor Service Manual for the Sun-2 Family of Workstations (Sun P/N 800-1147-01)
- Philips Electronics Ltd. Video Display Products Service/Operator Manual 19" Video Display Unit Model: M19P114A/5102
- System Managers Manual for the Sun Workstation-Models 120/170 (Sun P/N 800-1110-01)
- RS 423 Interface Specification
- System Release 1.1, Rev. C, release date 3-12-84
- 1.3 Manual for the Sun Workstation (Sun P/N 800-1159-01)

Figures

1

Theory of Operations



1

Theory of Operations

This section offers a brief operational overview of the Sun-2/50 SunStation. For the purpose of this overview, all Sun-2/50 components will be separated into three functional groupings: printed circuit boards (CPU board and optional Memory Expansion board), the monitor and the power supply.

1.1. Printed Circuit Boards

A single CPU board contains all of the logic necessary to operate the Sun-2/50 in its standard configuration. Memory capabilities may be enhanced with the addition of the optional Memory Expansion board.

The following logic description applies primarily to the CPU board. Information pertaining to the Memory Expansion board is contained in the section titled "Main Memory". The logic resident on both circuit boards is represented by the functional block diagram in Figure 1-2.

CPU board logic may be separated into the following functional blocks: CPU logic, Video Control circuitry, Memory and Interface logic. Each of these blocks, as well as the interconnecting bus architecture, will be described in the following paragraphs.

CPU Logic

The CPU logic block consists of the microprocessor and the following associated circuitry (refer to Figure 1-3 for a functional block diagram supporting this logic):

- Power-On/Reset Logic
- Clock Circuitry
- Interrupt Logic
- Boot PROMs
- ID PROM
- Function Code PAL
- Bus and Address Error Logic

Microprocessor

The CPU logic is designed around the Motorola 68010 microprocessor. The 68010 is a 16-bit, virtual memory microprocessor with an asynchronous bus structure supporting 24-bit addresses and 16-bit data words. Refer to Appendix E for pinouts and signal definitions for the 68010.

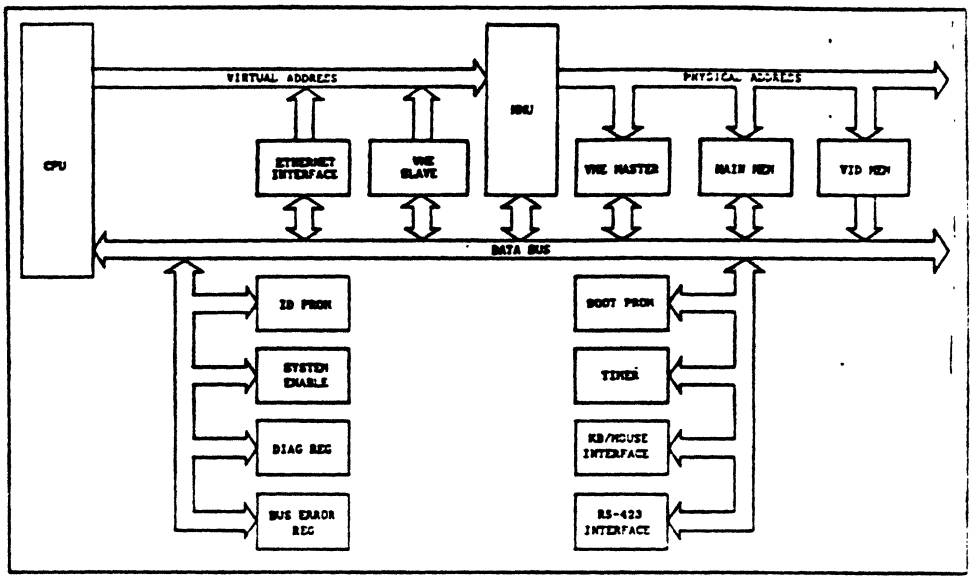


Figure 1-1 *Sun-2/50 Circuit Overview*

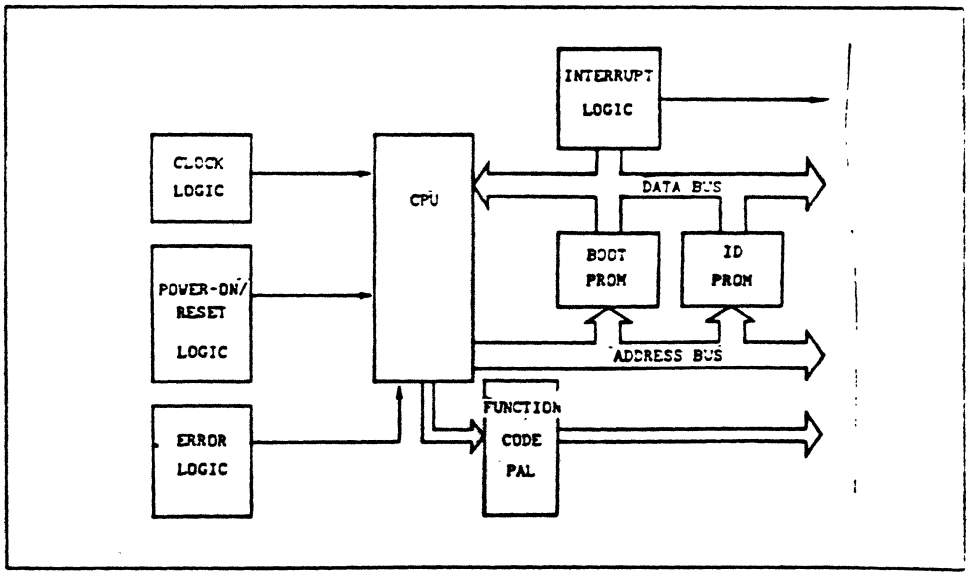


Figure 1-2 *CPU Logic*

Power-On/Reset Logic

The power-on/reset logic provide a means of starting a processor and/or system initialization sequence. This sequence is initiated in response to fluctuations in the supply voltage, a reset signal from an external bus, or a halt in a CPU processing cycle.

Microprocessor reset signals are generated by the PAL at U102 as the result of a power-on reset, an external reset, or a watchdog reset (refer to Appendix A). Inputs to the PAL are provided by the power-on reset generator (POR), the VME

bus (SYSR) and the 68010 (HALT).

Initialization and power-on-reset pulses are supplied by a power-on/power-off reset generator. This generator is composed of a dual comparator (U133), reference voltage diode (D101), charge capacitor (K100) and resistor network (R100-107).

The comparator acting as the power-on reset generator compares the voltage from the charge capacitor with the +1.2V reference voltage provided by the diode. The comparator will assert its output until the capacitor voltage reaches +4.5V.

The comparator acting as the power-off reset generator compares the +5.0V supply voltage with the +1.2V reference. The comparator output will be asserted when the +5.0V supply voltage drops below a threshold value of +4.5V.

The comparator outputs are combined to produce a power-on-reset (POR) signal when either comparator output is asserted.

An external reset will be generated when the Sun-2/50 is configured as a "reset slave" and a VME system reset (SYSR) is received. Both POR and SYSR are ORed at U108 and input to the PAL as POR1.

A watchdog reset is generated when the microprocessor stops during a normal cycle and asserts the HALT signal. The PAL will respond by asserting RESET to continue the processing cycle.

Refer to Figure 1-4 for a functional block diagram supporting the Power-On/ Reset logic.

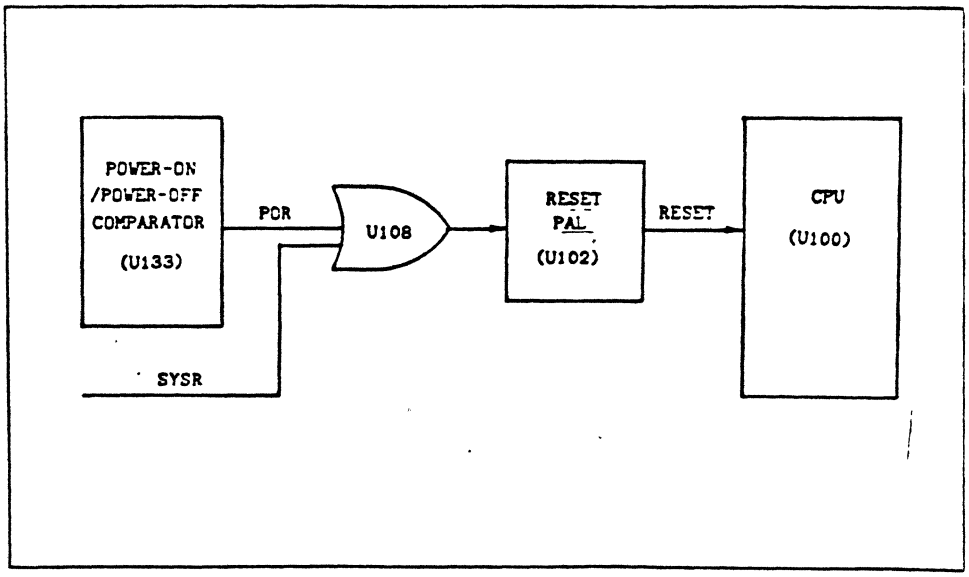


Figure 1-3 *Power-on/Reset Logic*

Boot PROMs

The boot code used by the CPU during reset, "boot state" and normal code- fetch cycles is stored in two 16,384 word by 8-bit PROMs. These PROMs (U500,U501) are addressed directly with the low-order address bits from the CPU (A01-14). Both PROMs are constantly chip-enabled and their outputs are controlled by an output enable signal (OE.PROM) from the PAL at U101.

Function Code PAL

The PAL at U101 controls a number of processes which are designated as "special cycles" (refer to Appendix A). Special cycles are operations in which the 68010 function code is neither program nor data. Examples of special cycles are CPU and MMU space cycles and boot PROM read cycles. The PAL receives function code data (P.FC0-2) from the 68010 which indicates the state (user or supervisor) and the cycle type currently being executed.

Clock Circuits

The clock logic provides the timing necessary for internal data processing and for communication with external devices; such as the Ethernet, keyboard, mouse and monitor.

All system clocks are derived from four independent oscillators, located on the CPU board. The output of the 19.6608MHz oscillator (U200) is divided by two, producing a 10MHz clock for the CPU (U100) and for the DVMA Request/ Arbitration machine (U213-15). These clocks are further divided to supply 4.9152MHz timing pulses to the Interrupt Request Timer (U504) and to the Serial Communications Controllers (U600/U601).

The 16.0000MHz oscillator (U202) is used to produce 8MHz timing pulses for the Ethernet Controller (U700), as well as providing a system clock to the VME bus.

The 100.0000MHz oscillator at U1800 supplies clock pulses to the video shift circuit (U1807-8).

The output of the 24.0000MHz oscillator (U201) is divided by two to produce a 12MHz clock designed for special applications.

Refer to Figure 1-5 for a functional block diagram representing the Clock logic.

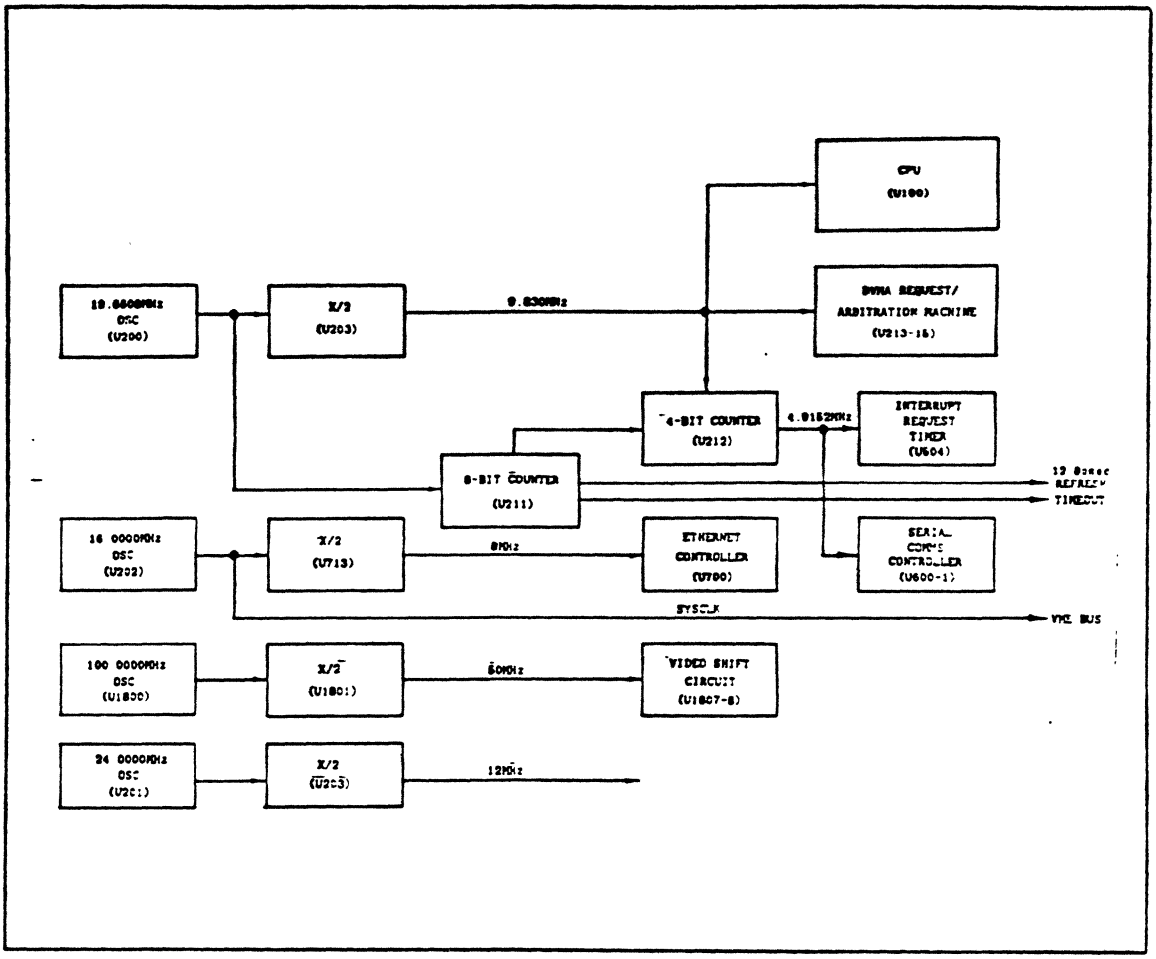


Figure 1-4 *Clock Circuits*

nterrupt Logic

The Sun-2/50 interrupt logic provides a means of prioritizing requests for processor attention from both internal and external logic groups.

The interrupt logic consists of a timer at U504 and an interrupt PROM at U105. The timer provides five 16-bit counters for the main logic board and is driven by a 4.9152MHz clock pulse derived from the 19.6608MHz oscillator at U200. Processor address bit A01 selects the count source and the read and write strobes are supplied by the read/write decoders at U401 and U402 respectively. The timer outputs a level 7 interrupt request (IRQ7) and four level 5 interrupt requests (IRQ5).

The interrupt PROM receives inputs from the timer (IRQ5, IRQ7), from the bus error logic (EN.INT1-3), from the video controller logic (V.IRQ-), from the ethernet controller (E.IRQ) and from the Serial Communications Controllers (IRQ6-).

The interrupt PROM outputs three interrupt control signals to the microprocessor (IPL0-2-), which contain the encoded priority level of the device requesting the interrupt. Level 7 is the highest priority interrupt and cannot be masked. Interrupt levels are defined as follows:

Level	*Meaning*
7	NMI (Non Maskable Interrupt)
6	Serial Communications Controllers
5	Interrupt Timer
4	Video
3	Ethernet
1, 2, 3	INT

ID PROM

The ID PROM (U510) contains basic information on the type and configuration of the Sun-2/50 in which it is installed. This information includes the serial number of the CPU board, the machine Ethernet address and the specific implementation of Sun-2 architecture used. Refer to Appendix A for a listing of the ID PROM contents.

If the original CPU board is removed and a replacement board installed, the ID PROM from the original board must be reinstalled on the new board.

Processor Bus Errors

A bus error (BERR) signal to the microprocessor indicates that a problem exists with the data transfer currently being executed. A bus error may be caused by page or protection errors in the Memory Management Unit (refer to Appendix A), parity errors, VMEbus errors, or a timeout.

The eight signals used to generate a bus error are ANDed together at U130. The output of this register (ERROR), when asserted, provides disable lines for the read/write strobe decoder (U400) and for the I/O decoder (U403). ERROR is also presented to the PAL at U103, which then generates the signals BERR, BERRCLK and PARCLK.

BERR is the processor bus error signal. BERRCLK latches the error condition into the bus error register at U511. PARCLR clears the parity error registers at U424, in the event that they were set. Refer to Figure 1-6 for a functional block diagram illustrating the bus error logic.

Data Transfers

The CPU uses a number of handshake signals to generate the timing required by the devices it is accessing. Upon completion of any data transfer cycle, a data transfer acknowledge signal (DTACK) is presented to the CPU by an eight-to-one multiplexer at U118. Inputs to the multiplexer are provided by PALs at U101 and U106.

When the CPU receives DTACK during a read cycle, the data is latched one clock cycle later and the bus cycle is terminated. When DTACK is received during a write cycle, the write strobes are deasserted and the bus cycle is terminated.

Devices requesting the bus from the CPU assert the signal Bus Request (BG). The CPU relinguishes the bus with the signal Bus Grant (BG). Refer to Figure 1-6 for a functional block diagram of the data transfer logic and to Appendix E for CPU signal definitions.

Address Error Cycle

An address error cycle is handled by the CPU much like an internally generated bus error. The address strobe (AS) is asserted and a normal cycle is executed, but no data is transferred because neither of the data strobes (UDS,LDS) are asserted. Note that the statistic bits in the Memory Management Unit (MMU) are still updated during this cycle (see the section describing the MMU).

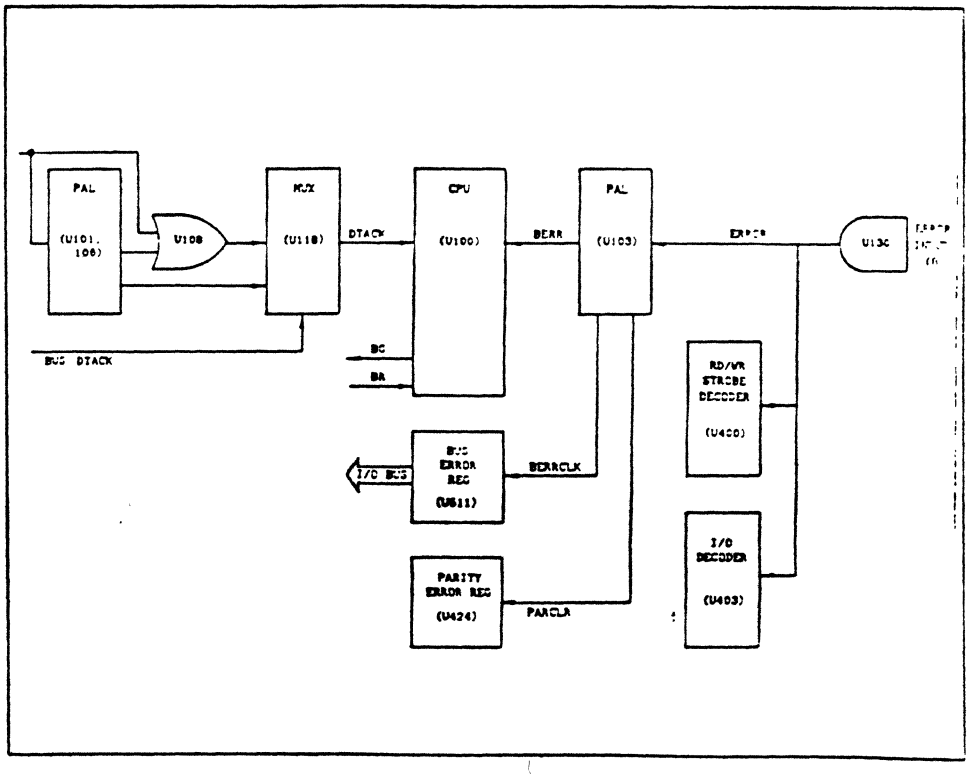


Figure 1-5 *Data Transfer and Bus Error Logic*

Bus Architecture

Sun-2/50 bus architecture supports a number of serial interfaces, as well as direct virtual memory access (DVMA) of the VMEbus by either the CPU or the Ethernet controller. The internal buses include the processor data and address buses, the memory data and address buses, and the I/O data bus. The VME bus is described in the Interface Logic section. Refer to Figure 1-7 for an overview of the Sun-2/50 bus architecture.

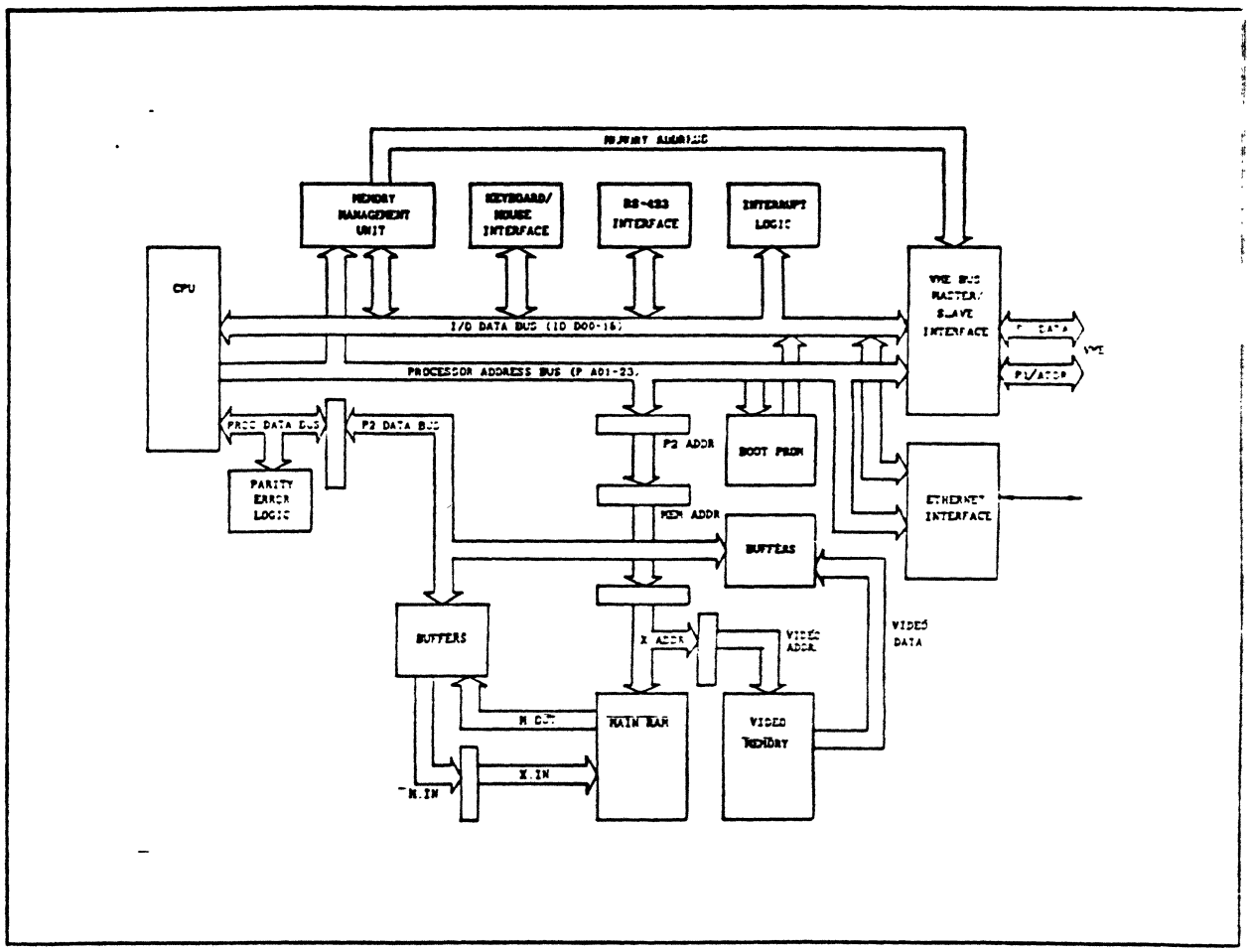


Figure 1-6 *Sun-2/50 Bus Architecture*

Processor Data and Address Buses

The 68010 utilizes a 23-bit address bus (P.A01-23) to provide addresses to the Memory Management Unit (MMU), the boot PROMs, the VME bus interface and to the Ethernet interface. Addresses transmitted to main, video and expansion memory are sent via the P2 bus.

The processor data bus (P.D00-15) is connected to the I/O data bus (IO.D00-15) through a pair of bidirectional transceivers at U110 and U111. All on-board data transfers, with the exception of information sent to the parity error logic, are carried out on the I/O data bus.

Data transmitted between the CPU board and the optional memory expansion board is seen as P.D00-15 by the CPU and as P2.D00-15 by the memory.

I/O Data Bus

The I/O data bus (IO.D00-15) provides a data path between the CPU and the MMU, the VME bus data port and all input/output devices. The I/O devices serviced by this bus include the boot PROMs (U500,U501), the Ethernet control logic (U700,U716,U717), the interrupt timer (U504) as well as the keyboard/mouse and RS-423 interfaces (U600 and U601 respectively). Refer to Figure 1-8 for a functional block diagram of the I/O data bus.

Individual I/O devices are selected by a comparator at U403. The comparator, in conjunction with the AND gate at U433, produces the chip enable signal "CE.IO-". This signal is presented to the bus decoder (U400) and to the read/write decoders (U401,U402) which then decode mapped address lines to select one of eight possible devices.

Processor data is placed on the I/O data bus via the transceivers at U110 and U111. These transceivers receive read/write strobes from the PAL at U102.

The I/O data bus is driven by the processor data bus on all processor-write and DVMA read-cycles. The processor data bus is driven by the I/O data bus during all DVMA-write and processor-read cycles generated by the I/O devices, the MMU and the VME bus.

Memory (P2) Bus

The P2 bus allows addresses and data to be transferred between the CPU and the main memory, video memory and the optional expansion memory. The P2 bus consists of address lines (P2.A00-23), bidirectional data lines (P2.D00-15) and miscellaneous control signals. The memory control signals include the row address strobes (RAS, RAS0, RAS1), the column address strobe (CAS), the read strobe (RD) and the write strobes (WEL,WEU).

RAS is asserted when the processor address strobe and clock are both active. This is the case when the processor has reached a specified state. Once RAS has been asserted, it is latched until a later specified state or until the address strobe is deasserted.

CAS is asserted at a specified processor state on non-special cycles only. During a special cycle (refer to Appendix A), CAS is inhibited by the signal SPECIAL. The column address is inhibited because, during memory management updates, it is not guarenteed to be stable and could result in invalid memory decoding.

The write strobes (WEL,WEU) are the product of the memory write signal (P2.WR-) from the decoder at U400, and the upper and lower data strobes (LDS,UDS). The write strobes are asserted with a specified processor state and while the data strobe (DS-) is active. The write strobes are turned off when LDS and UDS are deasserted.

P2 bus access is controlled by the decoder at U400. A read or write reference to the P2 bus is generated when the following conditions are met: the page type field is 0 or 1 (refer to the description of the MMU logic), the data strobe is asserted, the specified processor state is asserted and no bus error conditions exist.

During a memory bus read-modify-write cycle, the processor address strobe, as well as the row and column address strobes, are asserted for the entire cycle.

Both RAS and CAS are asserted before the page map type field is decoded by U400 and before the protection field is evaluated. As a result, CAS will indicate a valid address, but not necessarily a valid reference. The read/ write strobes (RD,WEL,WEU) qualify the reference.

Parity Error Logic

The parity error logic generates and checks parity during read/write cycles to main or expansion memory. This logic is not used during any other bus cycle and is not used during read/write cycles to the video memory.

Odd parity is generated, during memory write cycles, by the parity generators at U420 and U421. Inputs to these generators are supplied by the processor data bus (P.D00-15) and by the system enable register at U512 (EN PARGEN).

Parity is monitored during read operations by the parity checkers at U422 and U423. A parity error (even parity) results in the assertion of the EVEN output from one or both of the checkers. These signals are clocked into a pair of parity error flipflops (U424) during the memory read cycle, which in turn generate the parity error signals PARERRU- and PARERRL-.

The parity error signals are ORed at U130 with other error conditions to produce ERROR, which is used by the PAL at U103 to assert a bus error state (BERR) to the processor.

Parity errors, unlike other bus errors, cannot abort the current CPU cycle. Because a parity error can only be detected at the end of the read cycle, its existence is not recognized by the processor in time to abort the cycle. The parity error logic provides a means of retaining the error state until it can be recognized by the processor.

In order to ackowledge a bus error (caused by a pending parity error), the CPU must execute a non-special cycle. During this cycle, the PAL at U103 will assert the signal BERRCLK, which clocks the parity error state into the parity error register at U511. PARCLR is also asserted by the PAL to clear the parity error flipflops at U424.

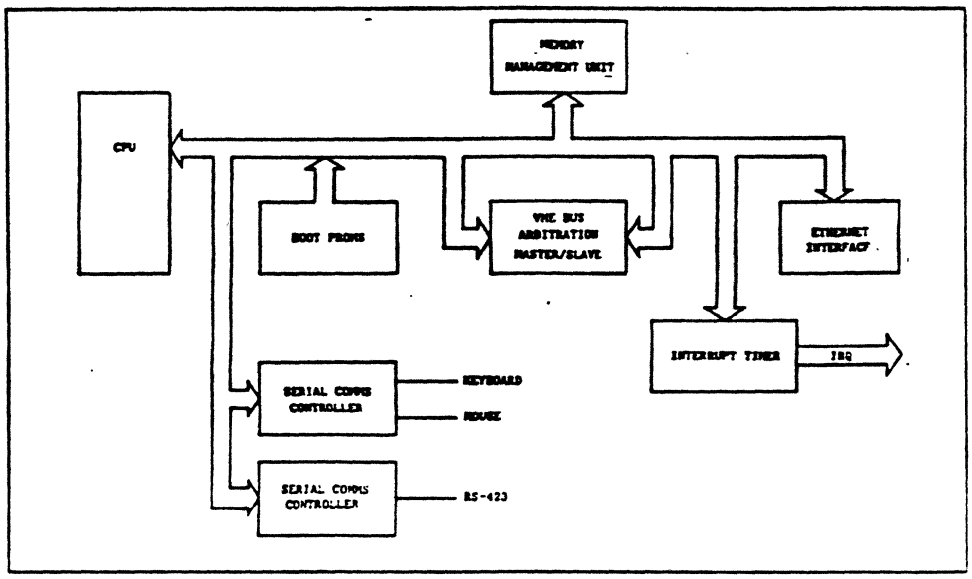


Figure 1-7 *I/O Data Bus*

Video Logic

The video logic consists of 128K bytes of memory, the memory controller, the video sync control circuitry, address decode logic, memory (P2) bus interface logic and the video shifter. Figure 1-9 provides a functional block diagram illustrating the video logic.

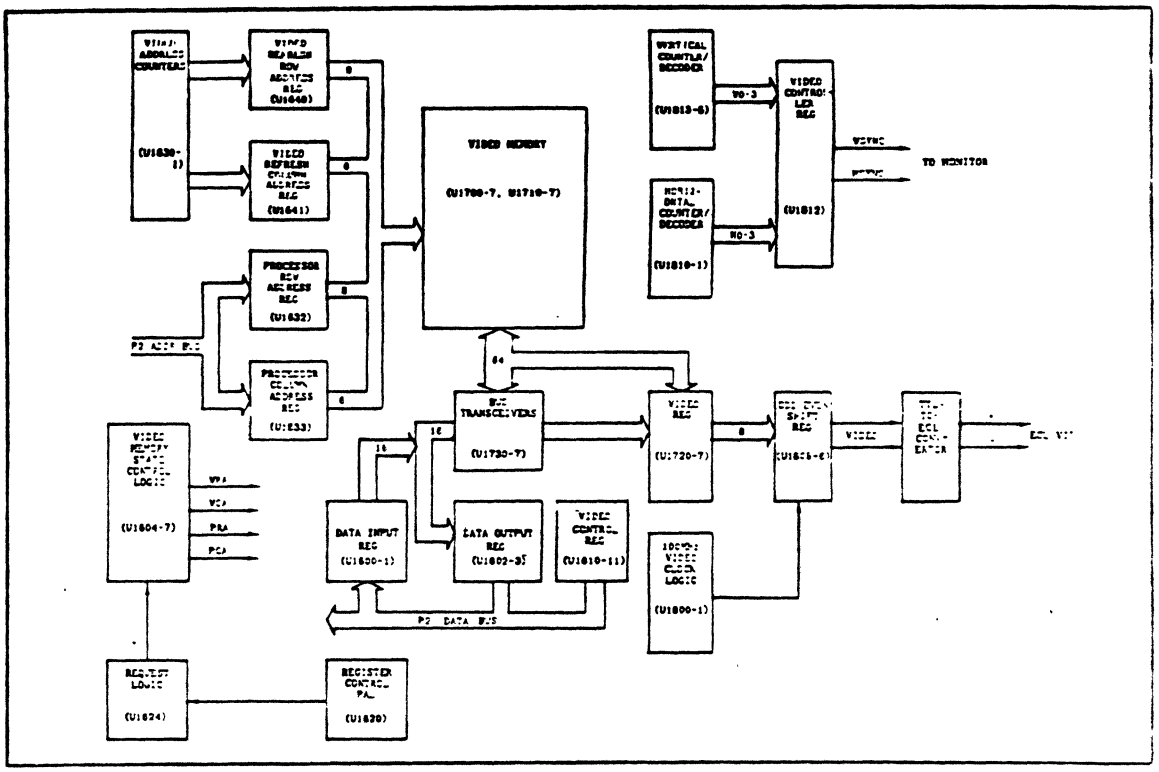


Figure 1-8 *Video Logic*

Video Memory and Address Decoding

Video memory (U1700-1707, U1710-1717) is located on the CPU board and is configured as 16K words of 64 bits each. The memory is dual ported to allow access by both the processor and the video refresh logic. Processor update cycles read 16 bits at a time, and write either 8 or 16 bits. Video refresh cycles read 64 bits at a time.

Processor cycle addresses are transmitted via the P2 bus, with the incoming row and column addresses stored in registers at U1632 and U1633 respectively. The video cycle addresses are generated by address counters at U1630 and U1631, and input to a pair of registers at U1640 and U1641. During video refresh, the address counters are incremented every 640nsec with an output enable signal from the decoder at U1728. The refresh counters are reset with the signal V RESET, generated by the video controller register at U1812.

Data is transmitted between the video memory and the P2 bus by the bidirectional bus transceivers at U1730-1737. Outgoing data, to the video shift logic, is latched by registers U1720-1727.

Video Memory Controller

The video memory controller supplies timing pulses to the memory and its associated logic. The memory controller is a state machine consisting of two PROMs (U1604, U1605) and a pair of registers (U1606, U1607). The state machine has a total of 16 states (STATE 0-15), which are continuously executed in sequence. Each state has a duration of 40nsec, making the entire 16-state sequence 640nsec long. Timing for this control logic is provided by clock pulses derived from the 100MHz oscillator at U1800.

The memory controller is capable of executing three types of cycles: idle, processor update and video refresh (refer to Appendix A). Idle and processor update cycles are executed in the first eight states; the refresh cycle is executed in the last eight. If no memory requests are pending, the memory controller will execute idle cycles. During these cycles no memory control signals are asserted.

A synchronous request (V SREQ), output from the request flipflops at U1624, causes the memory controller to execute a processor update cycle. During this cycle, the controller outputs the enable signals PRA and PCA to the row and column address registers (U1632, U1633). These signals ensure that both address registers are enabled in time for the video row and column address strobes (V.RAS, V.CAS).

Video Sync Control Circuitry

The video sync control circuitry is composed of the horizontal and vertical state machines (U1810-1811 and U1813-1815 respectively) and the video controller latch (U1812). This logic generates horizontal and vertical sync signals for use by the video monitor.

The horizontal counter at U1810 is incremented every 640nsec, on the falling edge of the memory controller signal V.HCLK. Counter outputs are presented to the horizontal decode PROM at U1811, along with VBLANK from the vertical state machine. The decode PROM generates the control signals horizontal clear (V.HCLR), horizontal sync (V.HSYNC) and display enable (V.DISPEN). V.HCLR provides a reset signal to the counter at U1810. V.HSYNC is used to clock the vertical state machine. V.DISPEN is sent to the video shift logic.

The vertical counter (U1813, U1814) is incremented on the falling edge of horizontal sync (V.HSYNC). Counter outputs are presented to the vertical decode PROM at U1815, which decodes the counter states to produce the signals V.V0-3. These signals are latched by the video controller latch (U1812) and output as vertical sync (V.SYNC), video clear (V.CLR), vertical blank (V.VBLANK) and video reset (V.RESET).

Video Shift Logic

The video shift logic is composed of a pair of 50MHz shift registers (U1805, U1806), a TTL-to-ECL converter (U1807) and a 100Mhz shift register (U1809).

Video data (V.D00-07) is output from the video memory, via registers at U1720-1727, and loaded into the shift registers at U1805 and U1806. These registers shift out the even (U1805) and odd (U1806) bits, outputting them as V.VID0 and V.VID1 respectively. Each pair of even and odd bits, together with 10nsec and 20nsec clock pulses (derived from the 100MHz oscillator at U1800), is loaded into the TTL-to-ECL converter at U1807. This converter outputs both true and inverted ECL data to the shift register at U1809. The shifted differential outputs

(VIDEO+, VIDEO-) are terminated with 390ohm resistors at R1800 and R1801.

Video Interface to the Memory (P2) Bus

The video interface to the memory bus consists of data input/output registers, the video control registers and associated logic. Data transmitted over the P2 bus to the video logic is latched by the data input registers at U1600 and U1601. Video data sent to the P2 bus is latched by data output registers U1602 and U1603. The data input strobe (V.REQ) and the data output register enable line (V.RD-) are generated by the Control PAL at U1620. The output register clock (V.ACK) and the input register enable signal (V.WU-) are produced by the video memory controller and the RAS decoder PAL (U1616), respectively.

The video logic responds to three types of memory accesses: direct reads, direct writes and copy writes. Direct reads and writes are selected via the bus select decoder at U1621. The decoder uses the four most significant P2 bus address bits (P2.A20-23) to generate the video bus select signal V.BSEL. V.BSEL is input to the control PAL at U1620, which then generates a video request signal (V.REQ).

A copy write is executed when two conditions are satisfied: the copy comparator at U1623 successfully matches P2 address bits A.17-22 with video base address bits V.BASE1-6, and the control PAL (U1620) is in copy mode.

Following a successful address match, the copy comparator asserts the select signal V.CSEL-. This signal is input to the control PAL, along with P2 address bit A17, to generate read/write strobes (V.WLC,V.WUC) for the control registers at U1610 and U1611.

Video Write Cycles

Data is written to the video memory when the external write strobes (LDS,UDS) are asserted by the request latch at U1615. These signals are input to the RAS decoder PAL at U1616. The decoder PAL generates enable signals (V.WU, V.WL) for the bus transceivers (U1730-1737) and data input registers (U1600-1601), as well as row address strobes (RAS0-3) for the memory. Refer to Figure 1-9 for a block diagram supporting this logic.

P2 bus data (P2.D00-15) is received by the data input registers and is driven, via the bus transceivers, to the video memory.

Video Read Cycles

A read cycle is executed if no write strobes (LDS,UDS) are asserted. The request latch (U1615) outputs bank select signals 1 and 2 (V.BS1,2), which are decoded by the PAL at U1616 to address a word in memory.

The video data is transmitted from memory to the bus transceivers at U1730-1737. The transceiver output (V.B00-15) is strobed into the data output registers (U1602,1603), and onto the P2 bus, by V.ACK from the memory controller (refer to Figure 1-9).

Video Refresh Cycle

A video refresh cycle is performed during the last eight states of every memory controller execution sequence in order to refresh the data stored in the dynamic RAM. During this cycle, the signals video row address (VRA-) and video column address (VCA-), from the memory controller, provide output enables for the video address registers at U1640 and U1641 respectively. With the assertion of these signals, the address registers latch values from the address counters

(U1630,1631) and transmit them to memory.

Video to Memory (P2) Bus Data Transfers

All write data is stored in a set of registers, allowing the processor to write to memory without waiting for a port to become available. The write cycle is automatically completed when the register data is strobed into memory.

A second write cycle can only be initiated after the first write operation has been completed. The signal P2.WAIT, output by the latch at U1816, inhibits subsequent writes until the current write operation is completed.

P2.WAIT is also used during the unbuffered read cycle to inhibit the processor read-data request until the data is available. This is also the case when a read request is pending while a write cycle is still in progress.

The video read/write handshake is implemented by the register control PAL at U1620. The PAL receives bus select signals V.BSEL and V.CSEL, from the bus access decoder (U1621) and copy comparator (U1623) respectively. These signals are used to assert the video request line V.REQ, which clocks addresses and control information into the processor address registers (U1632, U1633), and into the request latch (U1615). V.REQ is also input to the sync request registers at U1624 to produce the video state request signal V.SREQ. The state request signal is, in turn, presented to the memory controller logic, where it determines what cycle (processor or idle) will be performed.

Video Interrupts

Video interrupts are generated by the flipflop at U1803. The flipflop is clocked on the leading edge of V.VBLANK, from the vertical state machine. The outputs are asserted whenever the interrupt enable signal (V.INTEN), from the video control register, is active. The interrupt signals V.INTREQ and V.IRQ are output to the video control register and the processor respectively.

Memory

Sun-2/50 memory is composed of the following logic:

- Memory Management Unit
- Direct Virtual Memory Access Logic
- Physical Memory (Main and Expansion)
- Address Decoding

Overview of Sun-2 Memory Architecture

Sun-2/50 memory architecture is based on the concept of virtual memory, in which the physical memory resident on the PCBs (1-4MB) represents only a small amount of the memory space addressable by the CPU. The balance of the maximum virtual memory space is located on a secondary storage device (e.g. a large capacity disk drive) located elsewhere on the network.

When the CPU attempts to access a virtual memory address location that is not currently residing in physical memory, the access is temporarily suspended until the data is fetched from the secondary storage device. When the physical memory is updated, the suspended access is completed.

Addressable memory is arranged in 2K byte pages, with 16 pages comprising a 32K byte segment. Eight contexts may be mapped concurrently, each context having a maximum virtual address space of 16M bytes.

Memory Management Unit (MMU)

The MMU consists of a user context register (U300), a system context register (U301), a user/system context multiplexor (U302), the segment map RAMs (U303, U304), the page map RAMs (U305-310) and associated logic. Refer to Figure 1-10 for a functional block diagram supporting this logic and to Appendix A for definitions of MMU terms.

The MMU is accessed by the lower and upper byte decoders (U322 and U323 respectively) and by the read decoder (U324). All three decoders use the processor address bits P.A01-3 to generate read and write decode signals for the MMU logic.

During an address translation cycle, the function code from the CPU is used to select either the user or the supervisor context. The context value, output from either the user or supervisor context registers (U300 and U301 respectively), is presented to the multiplexor at U302. The multiplexor outputs, together with processor address lines P.A15-23, are input to the segment map RAMs at U303 and U304. The segment map RAMs use these inputs to produce a page map entry group, which in conjunction with address lines P.A11-14, is used to index the page map RAMs (U305-310). The page map RAMs generate an output composed of mapped address lines and a number of status bits (refer to Figure 1-10) which provides addresses to the CPU and to memory.

The validity of the protection field (PROT 0-5) is checked by the multiplexor at U315. If the protection bits are not set in accordance with the state of read/write line and the processor function codes, the output PROTERR (protection error) is asserted. This signal is presented to the bus error register at U130.

The accessed and modified bits (refer to Figure 1-11) are updated on all nonspecial cycles. The update is initiated when the current type field is input to the update register at U316. The update PAL at U103 asserts WR.UPDATE, which supplies a write enable signal to the page map RAM at U307, as well as

WR.STAT, which output enables the update register. The update register then writes the new data (TYPE0, TYPE1) to the page map RAM.

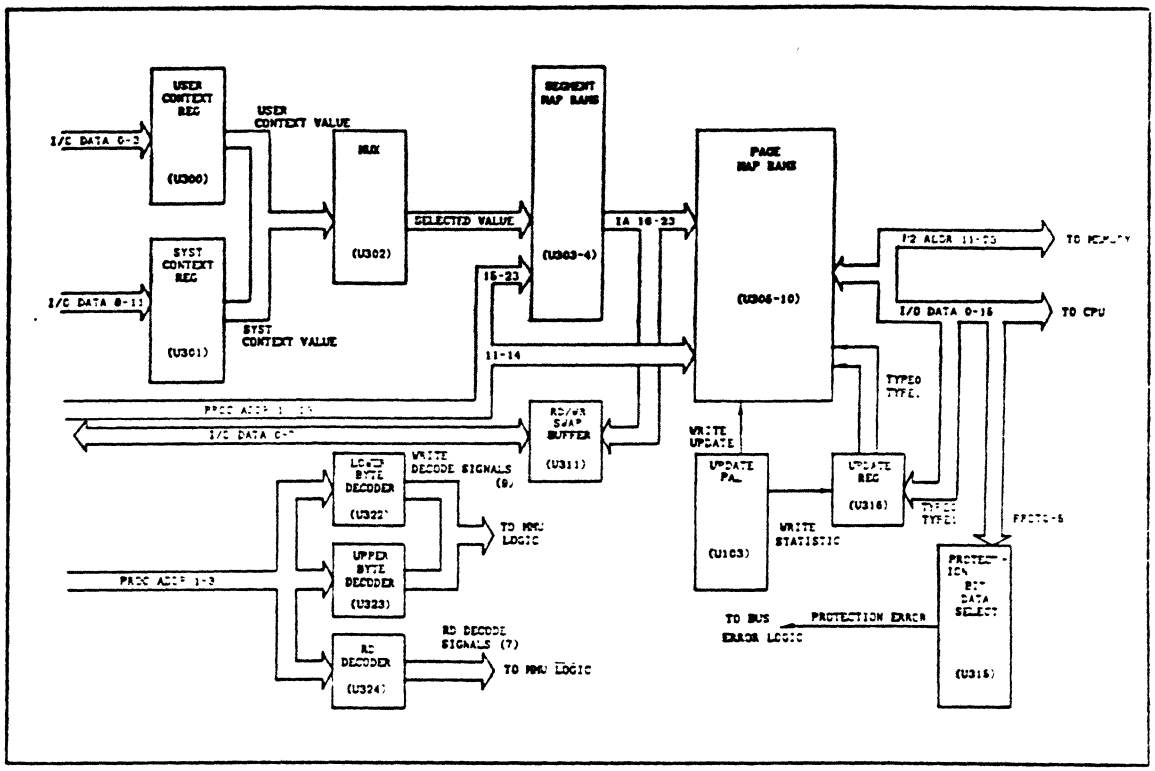


Figure 1-9 *MMU Logic*

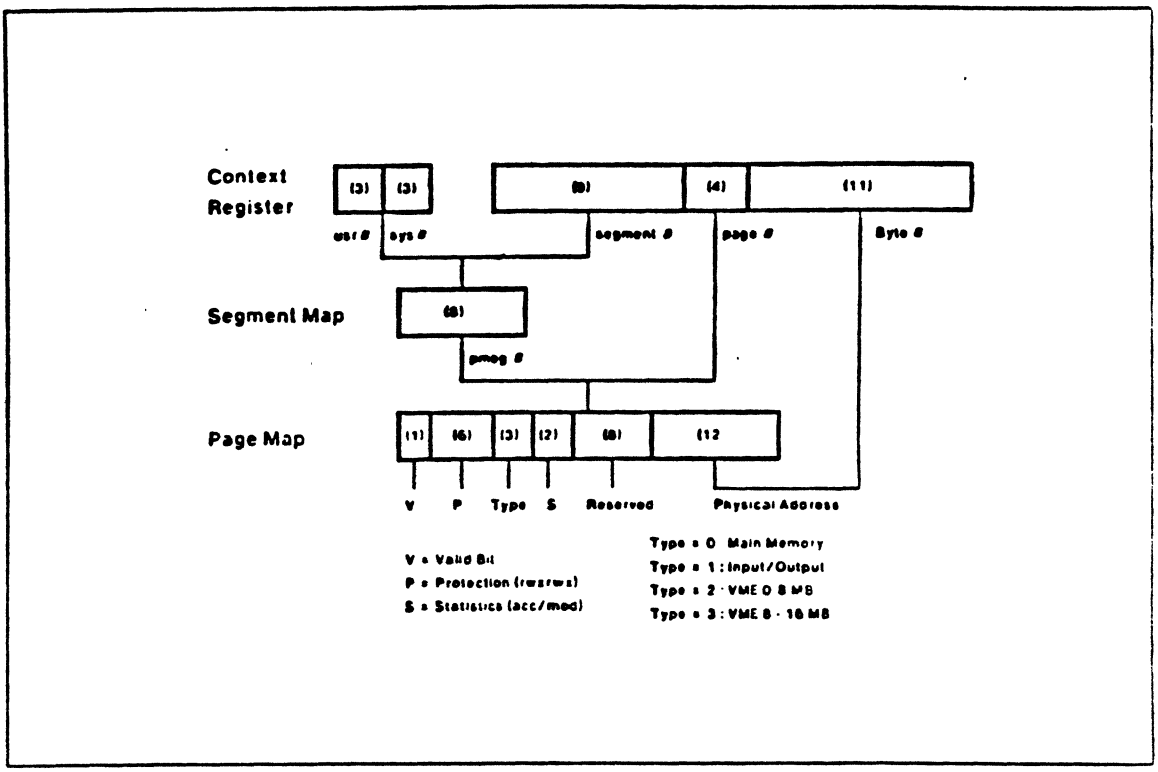


Figure 1-10 *Sun-2 Memory Management*

Main Memory

This circuit description is applicable to both the main memory and to the optional expansion memory. Main memory is located on the CPU board and provides the system with 1Mbyte of dynamic RAM. The expansion memory is located on the Memory Expansion board and supplies up to 4Mbytes of additional dynamic RAM storage.

Both main and expansion memory are organized as eight banks of eighteen chips each, for a total of 144 chips. Each bank is capable of storing a 16-bit data word along with two parity bits. The dynamic RAM may be either 64K or 256K bits per chip, providing memory capacity ranging from 1 to 4Mbytes.

The memory is arbitrarily divided into 1Mbyte sections: The first megabyte is always enabled, the second megabyte is enabled when pins 1 and 2, on select jumper J1201, are shunted. The third and fourth megabytes are selected as a pair, when pins 3 and 4 of select jumper J1201 are shunted. Refer to Appendix B for the location of the select jumper.

Address decoding for main and expansion memory is virtually identical: The memory select decoder at U1200 uses the three most significant bits from the P2 bus (P2.A20-22), as well as the configuration of select jumper J1201, to determine if the section being addressed is enabled. If the selected section is enabled, the decoder will output a memory select signal (M.SEL) to the CAS decoder at U1201, and to the read/write decoder at U1202. The read/write decoder will then enable the read/write buffers (U1210-1214) via either M.RD or M.WR, allowing

data to be transferred to and from memory over the P2 bus.

Note that the row address strobe (RAS) is not enabled during the bank select operation. Because of the pipelined RAS-CAS access, the address bits used to select which bank of memory is accessed are only available in time for the column address strobe (CAS).

Each bank of RAM receives an eight-bit address (A0-7) and the control signals RAS, CAS, WEL and WEU. The address is output from the read/write buffers (U1210-1214) and driven to the RAM inputs by line drivers (U1319,1339,1359 and 1379) through 33ohm series terminators (U1318, 1338,1358 and 1378).

CAS signals for each bank (M.CAS0-7) are driven directly to the RAM by the CAS decoder at U1201. RAS signals (P2.RAS,0,1) from the RAS generation logic, and the upper and lower byte write strobes (WEL,WEU) from the read/write decoderat U400, are driven to the RAM via a bank of line drivers (U1220,1222,1224 and 1226). Refer to Figure 1-12 for a functional block diagram supporting this logic.

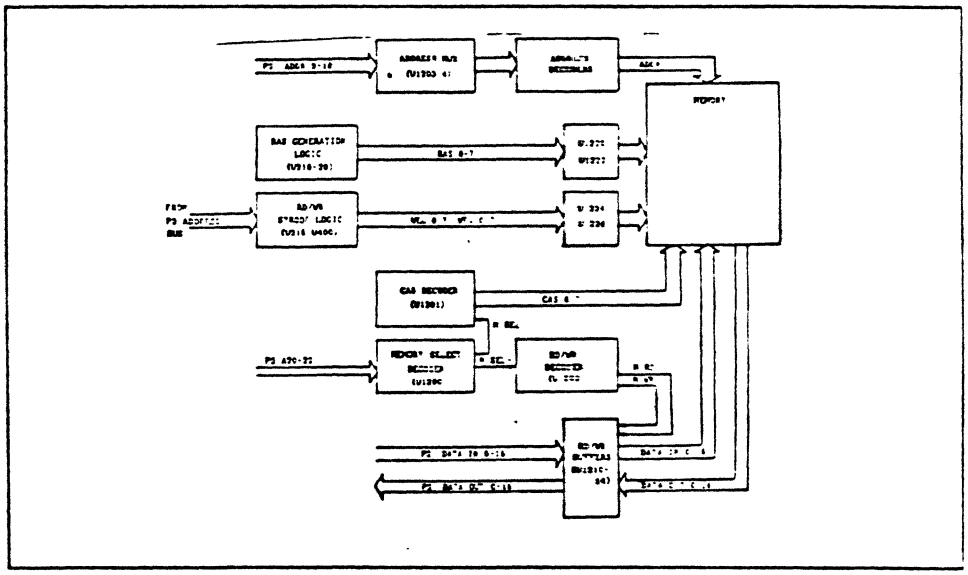


Figure 1-11 *Memory Address Decode Logic*

Direct Virtual Memory Access (DVMA)

Direct virtual memory access allows other devices to read from and write to the Sun-2/50 memory without interrupting the current CPU process. The DVMA controller logic obtains the processor bus from the CPU and performs the read/write cycle for the requesting device. The DVMA logic accepts requests from the memory refresh logic, the Ethernet controller and the VME bus.

The DVMA control logic is composed of the request flipflops (U207, 203), the request arbitrator latch (U213), the controller PAL (U214) and the strobe PAL (U215).

The request flipflops receive clock pulses from the memory refresh logic (R.REQ), the Ethernet control circuitry (E.DS) and the VME bus slave interface

(X.DMA). When one of the clock pulses is asserted, the flipflops generate the appropriate DMA request and present it to the DVMA request arbitrator latch at U213. The latched request signal is input to the DVMA controller PAL (U214), which prioritizes the request and issues a bus request signal (BR) to the CPU. The CPU responds with a bus grant signal (BG) and the deassertion of the processor address strobe (P.AS). The controller PAL then sends DMA enable signals to the requesting device and to the strobe PAL at U215. The strobe PAL provides the function code for the processor, as well as address and data strobes for the requesting device. Refer to Figure 1-13 for a functional block diagram of the DVMA control logic.

Memory refresh cycles are generated every 12.8usec by the 8-bit counter at U211. The counter output provides a clock for the request flipflop at U207, which issues a refresh DMA request signal (R.DMAREQ) to the associated DVMA control logic. The control logic outputs a DMA enable signal (R.DMAEN) to the refresh counter at U210, causing a "row address" refresh address to be presented to the dynamic RAMs. The PAL at U106 insures that both banks of memory are enabled during the refresh cycle by asserting the signals BANK0 and BANK1 to the RAS generation logic (U218-20). The RAS logic transmits the signals RAS, RAS0 and RAS1 to the RAM. Refer to Figure 1-14 for a functional block diagram illustrating the refresh logic.

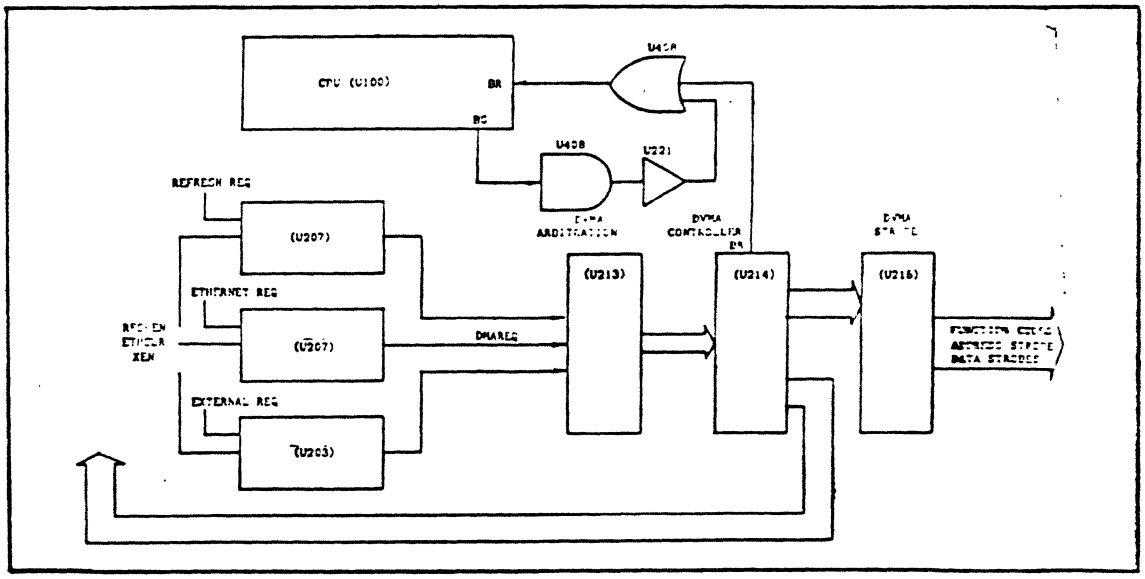


Figure 1-12 *DVMA Control Logic*

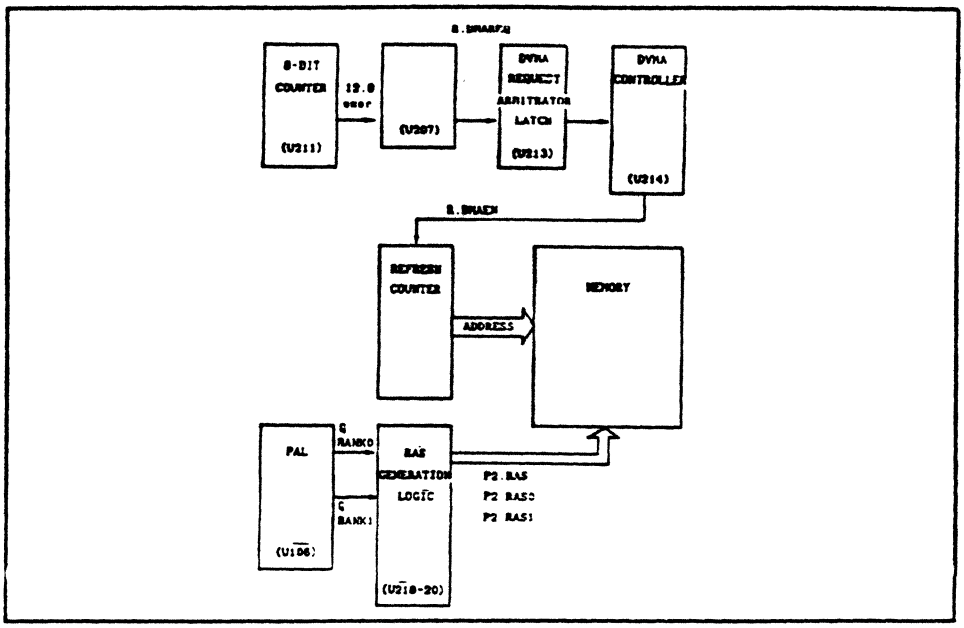


Figure 1-13 *DVMA Memory Refresh Logic*

Interface Logic

The interface logic consists of the serial ports for keyboard, mouse and RS-423 communication, as well as the Ethernet and VME bus interfaces.

Serial Communications

Serial communications between the Sun-2/50 and the keyboard, mouse and RS-423 interface is provided by a pair of Z8530 Serial Communication Controllers (SCCs). The SCC at U600 controls the keyboard and mouse, while the SCC at U601 supports the RS-423 interface.

Timing for both SCCs is provided by a 4.9152MHz clock, derived from the 19.6608MHz oscillator at U200. Chip select lines for the SCCs are supplied by processor address lines P.A01 and P.A02. Read/write control signals are provided by the read/write decoders at U401 and U402. Channels A and B, of the SCC at U600, are assigned to the keyboard and mouse respectively. Channels A and B, of the SCC at U601, correspond to ports A and B of the RS-423 interface.

Data being sent off-board is received by the SCCs over the I/O data bus as IO.D08-15. This data is converted from parallel to serial and transmitted to the selected device via dedicated RXD and TXD lines. For incoming serial data, the process is reversed.

Incoming RS-423 data is driven onto the board by the line receivers at U606 and U607. Outgoing data is driven onto the RS-423 interface by line drivers at U609 and U611. The line receiver at U615 is shared between channels A and B in order to support synchronous SCC applications.

Refer to Figure 1-15 for a functional block diagram supporting the serial communications logic.

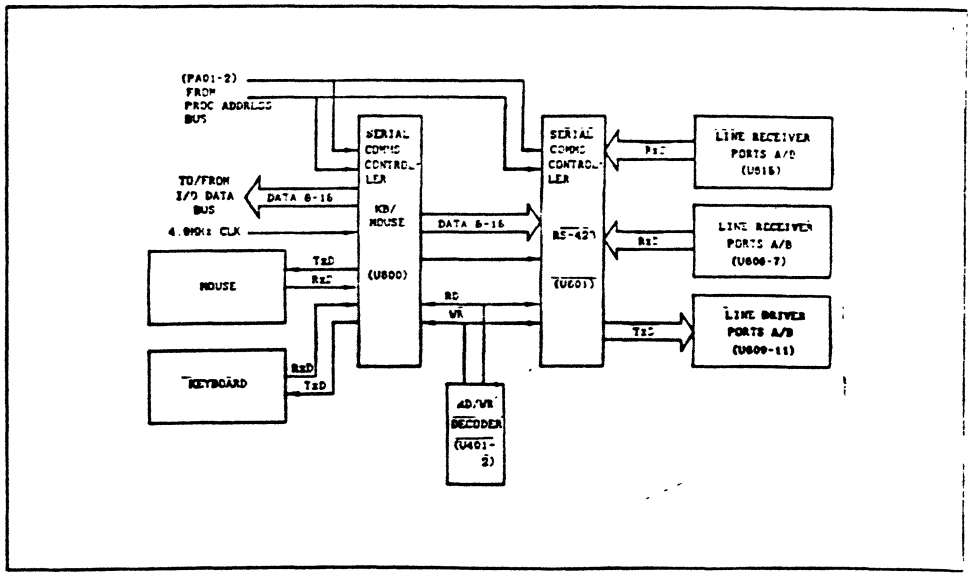


Figure 1-14 *Serial Communications Logic*

Ethernet Interface

The Ethernet interface consists of the Ethernet controller (U700), a phase lock loop decoder (U701), the control registers (U716-7) and associated logic. Refer to Figure 1-16 for a functional block diagram supporting the Ethernet interface logic.

Ethernet control is provided by an Intel 82586 Local Area Network Coprocessor. This device implements the Carrier-Sense-Multiple-Access-with-Collision-Detection method of link management (refer to Appendix A), which allows multiple workstations to access the local area network (LAN) at will.

The phase lock loop decoder at U701 acts as an Ethernet encoder/decoder circuit. This decoder connects the Sun-2/50 directly to an external Ethernet transceiver. Outgoing TTL-level data is encoded as transceiver-level code and placed on the Ethernet. Incoming Ethernet data is decoded into TTL-level data and clock signals. The decoding method employs a phase-locked loop approach with 10 samples per bit cell. Sample rate timing is provided by an external crystal (X700) and its associated tank circuit, which provide a 100MHz clock to the decoder's internal oscillator. Either Ethernet level 1 or level 2 interface characteristics may be supported via the select jumper at J704. Refer to Appendix B for the select jumper location.

The Ethernet control registers (U716, U717) manage the overall operation of the Ethernet interface. Inputs to these registers include an error signal from the bus error register (U719) and four bits from the I/O data Bus. The control registers generate interrupt, DVMA request, loopback and reset signals for the Ethernet interface logic.

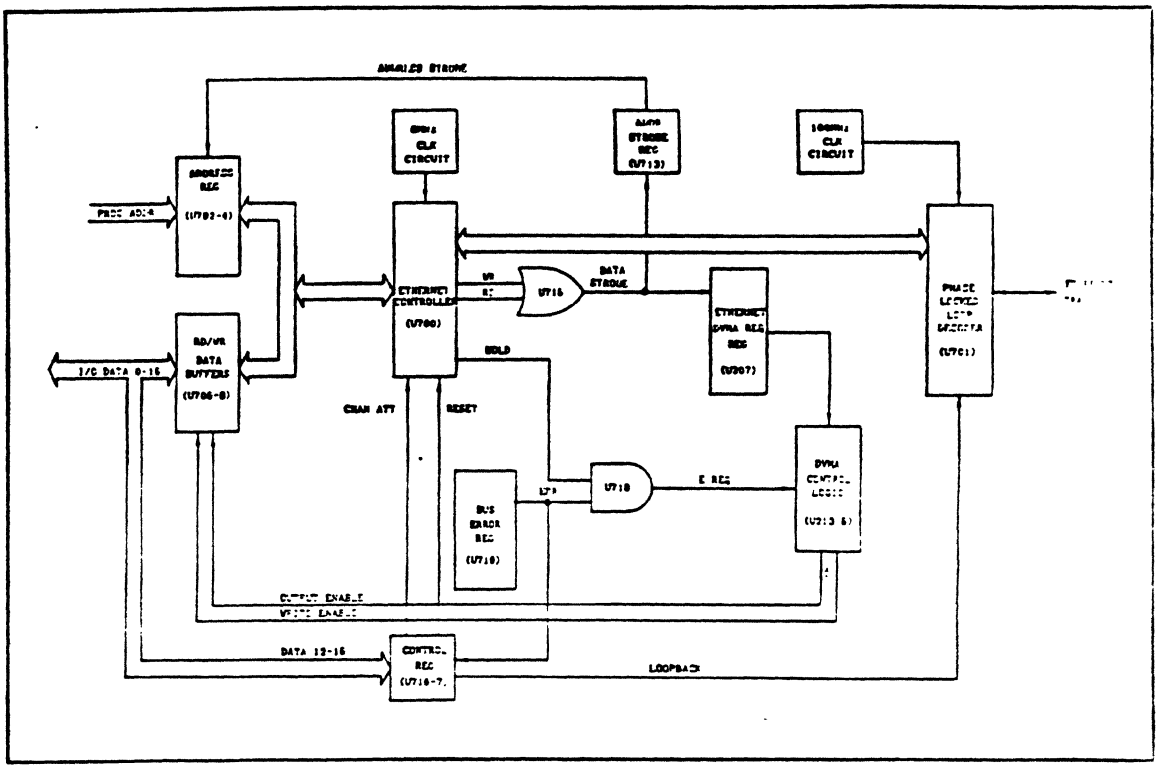


Figure 1-15 *Ethernet Interface logic*

Ethernet DVMA Cycle

An Ethernet memory access is initiated by the assertion of a read (RD) or write (WR) signal by the Ethernet controller (U700). These signals are ORed at U718 to produce an Ethernet data strobe (DS), which is used to clock the DVMA request flipflop at U207. The flipflop outputs the request signal E.DMAREQ to the DVMA control logic. The control logic also receives the Ethernet request signal E.REQ. This signal is the result of ANDing HOLD, from the Ethernet controller and E.ERR, from the bus error register. With these signals asserted, the DVMA arbitrator (U213) will continuously request the bus from the CPU until the Ethernet controller deasserts HOLD.

The Ethernet data strobe (DS) is also used, via the register at U713, to produce an address strobe. The address strobe (AS) latches the 24-bit Ethernet address (P.A01-23) into the address registers at U702-4 when the enable signal E.DMAEN is asserted by the DVMA control logic.

During an Ethernet write to memory, the DVMA control logic will provide an output enable signal (E.OE) to the write data buffers at U707 and U708. Data, from the Ethernet controller (U700) is input to the buffers and driven onto the I/O data bus as IO.D00-15.

During an Ethernet read from memory, data is latched into the read buffers at U705 and U706 by the write enable signal E.WE. The buffers are output enabled, driving I/O bus data to the Ethernet controller inputs, by the Ethernet read line (E.RD) issued from the DVMA control logic.

The Ethernet read and write buffers are byte swapped between the I/O data bus and the Ethernet data bus: I/O bus data bits 0-7 correspond to Ethernet bus data bits 8-15 and vice versa.

Ethernet bus errors are flagged by the bus error register at U719. In the event of a bus error, this register transmits the error signal E.ERR to the Ethernet control registers (U716-7) and to the DVMA request register (U207). The E.ERR signal inhibits any future DVMA requests from being sent to the DVMA control logic. DVMA requests are inhibited until the bus error register is cleared by a reset signal (RESET) from the Ethernet control registers.

VME (P1) Bus Interface

The VME bus interface provides the Sun-2/50 with bidirectional data access to any device attached to the VME bus. As the bus master, the CPU may access any of the slaves on the bus. As a bus slave, the Sun-2/50 may be accessed by other VME bus masters. Refer to Figure 1-17 for an illustration of the VME bus data transfer sequence.

The VME bus interface logic is composed of the arbitration and request circuitry, the VME master interface and the VME slave interface.

VME bus utilities are implemented using four control lines: system clock (SYSCLK), AC fail (ACFAIL), system reset (SYSR) and system fail (SYSF).

SYSCLK is derived from the 16MHz oscillator at U202. This signal is driven onto the VME bus by a high-current driver at U817. This clock signal has no phase relationship to other VME bus signals and may be disconnected by removing the shunt from pins 15 and 16 of select jumper J900. Refer to Appendix B for the location of the select jumper.

ACFAIL is derived from the power-on/reset signal POR and is driven onto the VME bus by the driver at U818.

System reset (SYSR) is driven onto the bus by the driver at U818 and is asserted whenever processor reset (P.RESET) is active. When configured as a bus master, the Sun-2/50 issues a reset signal to the VME bus with RESOUT. RESOUT is asserted as the result of a power-on reset, a processor reset or a watchdog reset. As a bus slave, the Sun-2/50 receives a reset signal (RESIN) from the VME bus.

VME Bus Arbitration and Request Logic

The arbitration and request logic consists of two PALs (U811, U814) and a pair of registers (U812, U813). Bus request levels are monitored and requests arbitrated using a level daisy chain (refer to Appendix A). A CPU bus request (in order to perform a read/write cycle, or to ackowledge an interrupt) is initiated with the assertion of a bus select signal (BSEL) to the PAL at U811. If the arbitor does not have control of the bus, it will request mastership by asserting the VME bus request signal BREQ and implement a normal bus arbitration sequence. If the arbitor currently controls the bus, it will keep control until another bus master requests it.

VME Master Interface

Once the arbitration logic has obtained bus mastership, the VME master interface allows the CPU board to access any slaves on the VME bus. The master interface is composed of address/address modifier latches (U940-03), a bank of address drivers (U900-03), write data registers (U910-11), write data drivers (U912-13), read data buffers (U908-09) and a control line driver (U817).

The VME slave device being addressed will respond to the data transfer with either an acknowledge signal (DTACK) or a bus error flag (BERR). These signals are latched at U815 and input to the PAL at U816, where they are transmitted to the CPU.

The VME master interface utilizes its backoff/rerun capability in response to VME bus deadlocks and VME accesses that take longer than 2-3usec. A VME bus deadlock results when the CPU attempts to access the VME bus while another bus master is concurrently trying to access the CPU as a slave device. Because the VME bus has no rerun capability, it requests that the CPU resolve the deadlock.

When a VME access is not completed within the specified time limit, or the bus is deadlocked, the state of the VME interface is frozen and a CPU rerun cycle is initiated. During the rerun cycle, the processor may relinguish the bus to the Ethernet interface or to the refresh logic, allowing those devices to execute their functions. The rerun cycle is then ended and the processor continues with the VME access. Rerun cycles are transparent to the VME bus and may also be performed while the CPU is waiting for bus mastership.

Conditions requiring a rerun cycle are recognized by the PAL at U810, which issues a bus rerun signal (B RERUN). This signal is input to the PAL at U102, which generates bus error (BERR) and halt (P.HALT) signals for the processor.

Rerun operations are monitored by a counter at U809. When the count reaches 128, a TIMEOUT signal is asserted to the bus error register (U130).

VME Slave Interface

The VME slave interface allows the CPU board to be accessed by other VME bus masters. A number of conditions must be met before the slave interface is enabled: The address comparator at U930 must successfully match the 4-bit VME bus address (P1.A20-23) to four bits from the switch-selectable base address (X.A0-3) The VME address modifiers must be specified and set. The VME interrupt acknowledge signal (P1.IACK) must be deasserted. The CPU board cannot currently be the bus master, and both the VME address (X.AS) and data (X.UDS,X.LDS) must be asserted. When all of the preceding conditions are met, the signal X.DMA is asserted by the comparator, indicating that a VME slave interface is pending.

When another bus master requests access to the CPU board, the DVMA control logic treats the access as an external DVMA request. When the DVMA control logic receives X.DMA, it initiates an on-board fetch cycle using the external DVMA address held in the registers at U904-06.

During a VME bus write cycle, VME data is placed onto the I/O data bus via the data buffers at U908 and U909. During a VME bus read cycle, data from memory is latched in registers at U910 and U911 and driven onto the VME bus

by data buffers at U912 and U913. The data transfer handshake is completed on the trailing edge of the enable signal (X.DMAEN) from the DVMA control logic. The handshake register at U931 will then assert either an acknowledge signal (X.DTACK) or, in the event of a bus error, the error signal X.BERR. The transfer signal X.DMA, from the comparator at U930, remains asserted until the VME bus master deasserts the data strobes. The handshake register (U931) is cleared on the falling edge of X.DMA.

VME Interrupt Control

There are seven VME bus interrupt lines, designated P1.IRQ1-7. All seven lines pass through a select jumper at J800 (refer to Appendix B), allowing any combination of interrupt levels to be selected. The selected interrupt lines are input to the priority decoder at U800, which prioritizes the interrupt requests and outputs the encoded interrupt lines B.IPL0-2. These lines are combined with on-board interrupt requests at the inputs of PROM U105, which produces the processor interrupt signals IPL0-2.

Upon receiving an interrupt request, the CPU generates the appropriate function code for the PAL at U101 and transmits the interrupt level being acknowledged on address lines A01-3. The multiplexor at U802 monitors A01-3 and the interrupt lines IRQ1-7, to determine if the pending interrupt is from an external source.

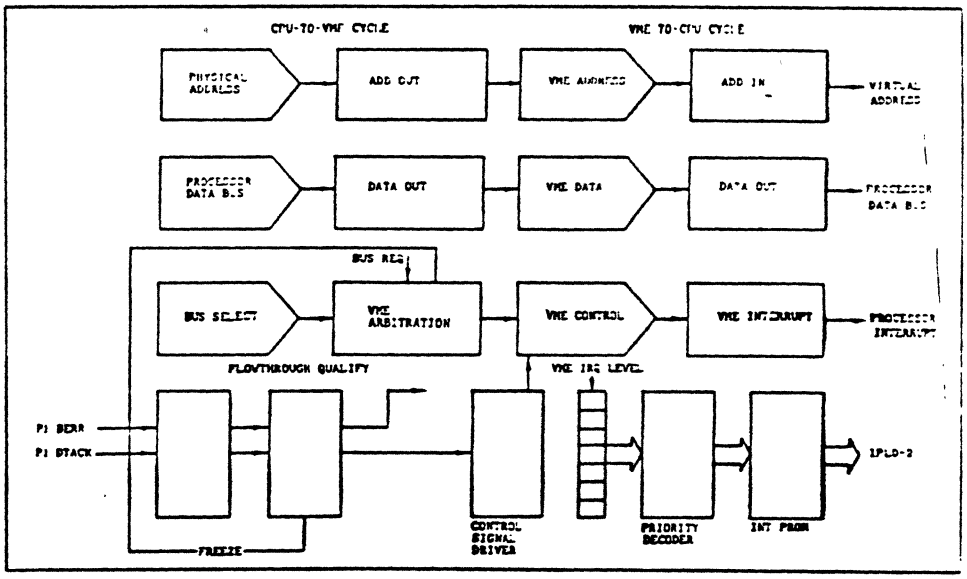


Figure 1-16 *VME Bus Data Transfer Sequence*

1.2. Monitor

The Sun-2/50 is configured with either a Phillips or a Moniterm monitor. While there are minor differences between the two, both monitors receive the following inputs:

- Horizontal Sync (HSYNC)
- Vertical Sync (VSYNC)
- ECL Video (VIDEO+,-)
- 120/240 AC

The video monitors share the following operational characteristics:

Visual Display-	900 horizontal lines with 1152 pixels per line (Version A) 1024 horizontal lines with 1024 pixels per line (Version B)
Video Clock-	10nsec from 100MHz oscillator
Horizontal Cycle-	16.00usec 62.5KHz
Vertical Cycle-	15000usec 66.67Hz
Horizontal Retrace-	4.48usec
Vertical Retrace-	600usec

Monitor adjustment procedures are provided in Chapter 2, Diagnostics and Troubleshooting. Comprehensive hardware descriptions and maintenance procedures are to be found in the monitors' respective service manuals (refer to the list of applicable documents).

1.3. Power Supply

Power for the Sun-2/50 is provided by a single-board power supply, located in the workstation chassis. The supply generates three regulated voltages, +5VDC, +12VDC and -12VDC, which are available at the system backplane. Refer to the power supply removal procedure in chapter 3 for a wiring diagram showing the supply outputs and their respective voltages.

The power supply operating specifications are as follows:

AC Inputs-	115/230VAC, 47-70Hz field selectable (Nominal) 90-132/180-264VAC (Operating Range)
DC Outputs-	Output 1, +5VDC +/-1% steady state at 22 amps Output 2, +12VDC +/-1% steady state at 1.5 amps Output 3, -12VDC +/-1% steady state at 0.5 amps

2

Diagnostics and Troubleshooting

2

Diagnostics and Troubleshooting

2.1. Overview

This chapter describes how to diagnose and repair problems on your Sun 2/50 workstation. It provides help for many levels of problems, ranging from simple items like checking power cords and switches, through complicated procedures like running standalone programs and PROM-based diagnostic programs.

This chapter is divided into five sections, each of which provides a different method of solving the problem. The choice of which to use depends on the nature of the problem, your experience, and the resources available.

The sections are:

- A symptom/action table — this provides a list of possible problems followed by instructions describing what to do about them.
- Observing the unit during startup — this section describes what the workstation goes through when it starts, what it needs to complete the process, and how to determine what's wrong by interpreting the messages displayed during this process.
- PROM diagnostics (pdiags) — a set of PROM chips, available from Sun, perform an extensive series of tests on the system hardware. These tests usually pinpoint the source of a hardware problem.
- Standalone programs — these are programs designed to be booted from the system monitor when UNIX is not present. They are designed to get at and test resources that are unaccessible when UNIX is present. For standalone programs to run, the system must be able to communicate with its file server.
- A quick reference troubleshooting guide — this is a flowchart which provides two kinds of help. In some cases, it acts as a pointer, leading the user to the other troubleshooting and repair sections in this manual; in other cases it actually guides the user through the troubleshooting and repair routine itself.

The chapter "Theory of Operations" includes a procedure for checking the power supply levels. This is sometimes included as part of the above procedures. Chapter 3, Maintenance, describes how to replace defective or damage field replacable units (FRUs).

2.2. Symptom Analysis

This section contains a list of the more common problem indications, followed by actions to correct them.

Sometimes, the solutions here refer the user to the other troubleshooting sections in this chapter, or to other manuals. This procedure assumes the user will take the corrective measures indicated there.

Local Problems

Problem	*Action*
System is inert; nothing happens when attempting to start it.	Check, in this order: Power switch ON Power cord plugged in Wall power ON System fuse OK (see procedure) Power supply OK (see procedure)
System won't complete autoboot procedure properly.	Check it as per "Startup Problems" section in this chapter.
Video display shows spurrious blips, or doesn't redraw correctly.	Check video cable and connections Run pdiags Check power supply levels
Video display wavy, dim or uneven.	Check and adjust video monitor and power supply as per procedure in the flowchart in this chapter.
Memory parity error reports.	If report includes address, check to see if address is within CPU's memory range (usually but not always 1 Megabyte). If address is greater, swap memory expansion board and run pdiag. If no address is present, or if address is within CPU's memory address range, run pdiag

Bus error reports. EXAMPLE:
 	
`Panic bus error`
`syncing disk ...`
`444444 ... done`
`dumping to dev NNN,`
`offset XXX`
`dump succeeded`
`rebooting`
	Allow system to reboot and proceed with normal use. If bus errors persist, run pdiag

Ethernet Problems

Problem	*Action*
Error reports prefaced by "ie0", or cursor displays a question mark '?' during boot procedure and booting won't continue. NOTE: When the cursor alternates between an equal sign and question mark during startup, it is searching for a bootable copy of UNIX. Give it some time before assuming problems; the Ethernet may be slow due to heavier than normal use.	Check connectors and cables including Ethernet connector on back panel of workstation. A picture of the connector appears in Appendix G. Check other stations, if accessable, to see if they're experiencing Ethernet problems. Correct Ethernet as per Ethernet instruction manual.

File Server Problems

Problem	*Action*
File server doesn't respond, or during startup procedure, cursor on workstation screen continues to display a question mark then an equal sign (? =) while staying in same location.	Verify that file server system is running correctly as per "System Administration for the Sun Workstation".
File system damage for more than one client	Verify that file server system is running correctly as per "System Administration for the Sun Workstation.
Messages containing prefix "nd", such as "nd output error 55"	Check file /etc/nd.local as described in "System Administration for the Sun Workstation".
File system damage for ONLY ONE client (who has Sun workstation!)	Suspect client's CPU — run pdiags

2.3. Observing the Startup Procedure

After power-on or reset, the Sun 2/50 workstation goes through a series of steps designed to bring it up piece by piece, testing and taking inventory as it goes. The boot PROM contains a program called the monitor, which performs some routine hardware tests, attempts to boot the UNIX kernel, then passes control to it.

The user can interrupt the monitor after it finishes its startup tests but before it passes control to UNIX. This causes the monitor to enter an interactive mode,

enabling the user to load and execute (boot) programs other than UNIX.

If the user does not interrupt the monitor, and the Ethernet and file server are working correctly, the monitor boots the UNIX kernel and passes control to it.

The messages generated during this procedure provide clues as to how the system is working and what (if anything) is wrong.

Startup Tests

If the startup tests pass, the monitor displays the following message on the screen, or on a terminal if one is attached (dashes "-" indicate variables):

```
Self Test completed successfully

Sun Workstation, Model Sun-2/50 or Sun-2/160, Sun-2 Keyboard
ROM Rev -, -MB memory installed
Serial # --, Ethernet address -:-:--:-:-:--

Probing I/O bus: ie
Auto boot in progress
```

If this message does not appear, the selftest failed. To confirm this, check the CPU LEDs and note the pattern displayed. They should either display one pattern constantly, or cycle through a series of patterns starting with the beginning-of-test (all clear).

In either case, the LEDs provide information about the failed test. If the pattern remains constant, the monitor is cycling on one test; that should be the one that failed. If the LEDs are cycling through a number of patterns then returning to all-clear, the last pattern visible before the all-clear should be the test that failed. In either case, identify the failed test by matching the pattern to the tests, as shown below.

Table 2-1 *LED Displays During Startup Selftest*

LEDs ★=*on*, o=*off*	*Hex*	*Test in progress*	*Suspect if LEDs stuck or cycling to here*
★★★★ ★★★★	FF	Reset - no tests running	CPU or monitor PROMs
oooo oooo	00	Startup tests complete	All tests passed
oooo ★ooo	04	Blinks if NMI OK	System seems OK
oooo oo★o	02	Entering user watchdog routine	Software bug
ooo★ ooo★	11	Context registers	CPU
oo★o ooo★	21	Data lines in segment map	CPU
oo★o oo★o	22	Address dependencies in segment map	CPU

Table 2-1 *LED Displays During Startup Selftest— Continued*

LEDs ⋆=*on*, o=*off*	*Hex*	*Test in progress*	*Suspect if LEDs stuck or cycling to here*
oo⋆⋆ ooo⋆	31	Constant data in page map	CPU
oo⋆⋆ oo⋆⋆	33	Data lines in page map	CPU
oo⋆⋆ oo⋆o	32	Address dependency in page map	CPU
o⋆oo oooo	40	PROM contents	CPU or monitor PROMs
o⋆o⋆ oooo	50	SCC chips	CPU
o⋆⋆⋆ oooo	70	Sizing memory	CPU or memory expansion
o⋆⋆⋆ ooo⋆	71	Memory constant data	CPU or memory expansion
o⋆⋆⋆ oo⋆o	72	Memory address dependency	CPU or memory expansion
o⋆⋆⋆ ⋆⋆⋆⋆	7F	Parity circuit	CPU or memory expansion
⋆ooo ooo⋆	81	Timer chip	CPU
oooo ooo⋆	01	Selftest done; perparing to boot	CPU or memory expansion
oooo oo⋆⋆	03	After local memory verified	CPU
oooo o⋆⋆⋆	07	Setting up-diagnostics complete	CPU
⋆⋆⋆⋆ ooo⋆	F1	Setting up memory-diagnostics complete	CPU
⋆⋆⋆⋆ oo⋆o	F2	Setting up maps-diagnostics complete	CPU
⋆⋆⋆⋆ oo⋆⋆	F3	Setting up frame buffer	CPU or video/video frame buffer
⋆⋆⋆⋆ o⋆oo	F4	Setting up NMI or keyboard	CPU

Boot Device

If the selftests complete successfully, the monitor attempts to boot UNIX over the Ethernet. It displays the following message:

```
Probing I/O bus: ie0
Auto-boot in progress
Boot: ie(0,0,0)VMUNIX
Load: ie(0,0,0)boot
Boot: ie(0,0,0)VMUNIX
Size: NNNNNN, NNNNN, NNNNN bytes
Sun UNIX 4.2...
```

Before the "Auto-boot in progress" is displayed, the system checks to ensure that it has a keyboard connected. If it does not, it doesn't panic, it simply informs the user with the message:

```
    Using RS232-A Input
```

```
right before
```

```
    Auto-boot in progress
```

If you think you have a keyboard attached, this message indicates a defective connection or keyboard. It will cause the startup procedure to abort later if no terminal is connected to RS232 port A.

The monitor looks for a bootable copy of UNIX on local disk, local tape, and then on the server over the Ethernet. While it is looking, it displays an alternating question mark, then an equal sign inside the cursor on the workstation screen. Since the 2/50 does not normally have a local disk or tape, the Ethernet copy gets booted.

If the Ethernet is not working correctly, this message or one like it appears:

```
Probing I/O bus: ie0
Auto-boot in progress
Boot:  ie(0,0,0)VMUNIX
ie xmit failed: NNNN
ie Ethernet jammed
ie xmit failed: NNNN
ie Ethernet jammed ...
```

If this happens, check the Ethernet connector on the back of the system, or the Ethernet itself, as per it's instruction manual. The Ethernet connector appears in Appendix G.

If the Ethernet is working but the monitor cannot find something to boot, it continues to display the alternating question mark and equal sign. Check to ensure the file server is working correctly and a bootable copy of UNIX lives in /vmunix. See "System Administration for the Sun Workstation".

UNIX Kernel

Assuming the Ethernet is working, and the monitor was not interrupted, the system searches out the file /vmunix on the server and downloads it over the Ethernet into local memory. This file should be a bootable UNIX kernel; the monitor passes control to it when it is loaded.

The kernel takes over the task of bringing the workstation on line. It conducts a search of available resources and displays the results on the screen with a display similar to the following (where Xs and Ns are variables):

```
Boot: ie(0,0,0)vmunix
Load: ie(0,0,0)boot
Boot: ie(0,0,0)vmunix
Load: ie(0,0,0)boot
Boot: ie(0,0,0)vmunix
Size: NNNNNN+NNNNN+NNNNN
Sun UNIX 4.2 Release Kn (XXXXXX-CLIENT) #X: Tue Oct 23 18:30:3
Copyright (c) 1984 by Sun Microsystems, Inc.
mem = NNNNK (0x0n0000)
avail mem = nnnnnnn
Ethernet Address = N:N:NN:N:N:NN
zs0 at virtual nnnNNN pri 3
zs1 at virtual nnnNNN pri 3
is0 at virtual nnNNNN pri 3
bwtwo0 at obio N pri N
using NN buffers containing NNNNNN bytes of main memory
Automatic reboot in progress
DDD MMM DD HH:MM:SS TTT YYYY
/dev/nd0: NNN files, NNNN used, NNNN free (NN flags, NNNN blo
DDD MMM DD HH:MM:SS TTT YYYY
System went down at DDD MMM DD HH:MM:SS TTT YYYY
Dump time is DDD MMM DD HH:MM:SS TTT YYYY
local daemons: local sendmail portwrap
preserving editor files
clearing /tmp
standard daemons: update cron printer accounting
Starting network at: inet
DDD MMM DD HH:MM:SS TTT YYYY

NNNNNN login:
```

After the "Automatic reboot in progress" line, a program checks to ensure file system integrity, and attempts to repair any inconsistancies. If this program does any repairs, it reports its activities, then resets the system, causing the entire reset sequence to repeat. This condition is most likely if the system was shut down or reset without using /etc/halt to do it correctly.

The later half of the above message may vary according to the conditions and system configuration. Certain trivial system problems may generate error reports that do not substantially effect the procedure.

The following line in the above message represents a data and time report:

```
DDD MMM DD HH:MM:SS:TTT YYYY
```

for example:

```
Fri Dec 21 13:35:22 PST 1984
```

Now, the UNIX controls the workstation. This presents a whole new spectrum of possible problems that are beyond the scope of this manual. For instructions, see the Sun UNIX documentation and consult your local UNIX expert.

2.4. PROM Diagnostics (PDIAG)

A set of two PROM chips, labeled 0 and 8, contain the most comprehensive diagnostic program available for the Sun-2/50. These PROMs are normally not present; they must be installed in place of the normal boot PROMs (U500 and U501) for the diagnostic effort. Then, when the workstation is powered-on, they take over operation, allowing no other program to run.

Using these diagnostics requires

a) powering down the workstation,

b) opening the case and installing the PROMs,

c) powering it on, and

d) interpreting the results.

The following procedures provide instructions.

Installing PROMs

1)

- A phillips screwdriver
- An ASCII terminal, set up as follows:
  - Full Duplex
  - 9600 baud
  - XON and XOFF
- An RS232 cable connected as follows:
  - Cross-connect 2 and 3
  - Loop back 5 and 6 at both ends
  - Connect 7 straight through

A set of diagnostic PROMs labeled 0 and 8

2) Power-down the workstation. If UNIX is running, use /etc/halt.

3) Unplug the power cord.

4) Remove the PC board as described in Chapter 3, Maintenance, in this manual.

5) Locate the boot PROMs, U500 and U501, on the main PC board.

6) Replace these with the two diagnostic PROMs.

   a) Install the diagnostic PROMs in the correct pads. Both the pads and the PROMs are labeled "0" and "8"; make sure they match. 0 goes in PROM0 and 8 goes in PROM8.

   b) Install the diagnostic PROMs in the right direction. Line the U-shaped depression in the PROM chip with the V-shaped indentation silk-screened around the PROM holder.

   c) Handle PROM chips carefully! Avoid bending or damaging pins, and place the PROMs in an anti-static pad when not using them.

7) Replace the main PC board and close up the workstation. Again, refer to the Chapter 3 for details.

8) Connect the terminal's RS232 cable to the connector labelled SIO-A on the rear panel of the workstation.

9) Plug in and power up the terminal.

10) Plug in and power up the workstation.

11) The diagnostics should start automatically. Refer to the procedure "Using the Diagnostics" in this section for details.

12) When the diagnostic is completed, repeat steps 3 through 7, replacing the diagnostic PROMs with the boot PROMs. OBSERVE ALL CAUTIONS!

Using the Diagnostics

The diagnostic program (pdiag) starts automatically when the workstation is powered-on with the PROMs installed. It runs through the first series of tests (11 through 41), then enters menu mode. In menu mode, the user can allow it to run a default series of tests, or can interrupt it and then control it via the menu.

Because the video monitor may not be working, the diagnostics send all output messages to the terminal. However, the video monitor should be connected, so it can be tested, and because some of the tests display patterns on it.

Automatic Tests

The diagnostic program displays the following message on the terminal as it completes the automatic tests:

```
Model 50 Prom Diagnostic REV 1.7 10/23/84 Sun Micro

T21(segcons) T22(seg uniq) T23(seg check)
T24(pagecons) T25(page uniq) T26(page check)
0x0N0000 bytes of memory found
T31(cons mem) T32(mem uniq) T33(mem rand) T34(mem check)
T37(page a/m bits) T38(pageon) T39(pageoff) T40(valid) T41(ints)
Starting Menu
Press key to stop default tests
Model 50 diagnostic Menu REV 1.3 10/16/84
Video menu REV 1.2 9/25/84
enable: video 1/1 copy 0/0 int 0/0
base 0x2/0x2
jumper: b/0 a 0 color 0 1K 0
Pass1
Pass2
Pass3
Pass4
Pass5
Pass6
Pass7
Pass8
Pass9
Pass10
Pass1 ...
```

The tests generate the above message as they pass. If they fail, the sequence is interrupted; the resulting indications are listed in "Test Descriptions" later in this section.

The words "Starting Menu" in the above message signal the transition from the automatic portion of the tests to the menu portion. Pressing any key after this message causes the program to interrupt its sequence; it can then be controlled as described in the "Menu Mode" description a bit later.

The menu portion runs through the following automatic sequence if allowed to continue uninterrupted (no key is pressed and no test fails):

```
Start

Tests 11 through 41 (crawlout tests)

Menu Mode Automatic Defaults as follows:

   Video tests:

     Register test

     Memory test, 10 passes - prints "Pass1, Pass2, etc" on t
     and displays different patterns on the workstation scree

     Copy test, 10 passes - prints "Pass1, Pass2," etc on the
     displays different patterns on the workstation screen.

   Ethernet:

     Diagnose

     Local Loopback

     Encoder loopback

  Returns to beginning of diagnostic program and starts over w
```

Menu Mode

After the diagnostic program displays the words "Starting Menu", pressing any key interrupts the automatic test sequence and causes it to enter menu mode.

The menus allow the user to select individual tests from the groups Video, Ethernet, and Memory, and to select some parameters. To display the current menu enter "?"; to display the current test and parameters, enter a <return>. To run a single test, enter the test letter from the list below; to run a series of tests, enter a series of letters from the list, separated by commas.

The following list shows the menus and tests. For details of each test, see "Test Descriptions" later in this section.

Table 2-2 *Menu List*

Menu Type	*Items in Menu*	
Top Menu	v	Video
	e	Ethernet
	m	Memory
Video Menu	r	Register
	m	Memory
	c	Copy
	u	Up to main menu
	?	Display menu
Ethernet Menu	d	Diagnose
	l	Local loop
	e	Encoder loop
	E	External loop
	D	Dump
	U	Up to main menu
	?	Display Menu
Memory Menu	m	Map
	p	Pattern
	a	Address unique
	r	Random
	m	Change Modes
	b	Bang
	u	Up to main menu
	?	Display menu

Test Descriptions

The following list describes each individual test, and the messages and indications generated if it fails. The tests start at Test 11.

Context Tests

Test 11: Supervisor Context Register — Tests ability to read and write the supervisor context register by writing, then reading the values 0 to 7. Non-matching values cause a fatal write/read loop. Uses byte access in fc3.

Failure Mode — Tests 11 through 15 repeat indefinitely upon failure. Test 16 repeats for (about) 5 minutes, then allows the test suite to continue. As each test runs (and repeats!) it displays its test number in binary on the CPU LEDs; these numbers can be converted to hexadecimal to yield the test number.

Test 12: User Context Register — Tests ability to read and write the user context register by writing, then reading the values 0 to 7. Non-matching values cause a fatal write/read loop. Uses byte access in fc3.

Test 13: User/Supervisor Context Register — Writes the value 7 in the user context register while the writing the values 7 to 0 in the supervisor context register, then decrements the value in the user context register to 6 and again writes 7 to 0 in the supervisor context register. It continues until both registers contain 0. Uses word access in fc3.

Test 14: Supervisor/User Context Register — Same test as above, only the user and supervisor context registers are reversed. Uses word access in fc3

Startup Tests

Test 15: Check Function 6 and PROM — Checks to see that the data fetched in function code 5 (supervisor instruction - fc5) space matches the data fetched in fc6 (supervisor data space). Failure causes a fatal read/write loop from fc5 followed by a read from fc6 at the failing address. Uses byte access in fc5 and fc6 spaces.

Test 16: Initiate UART — This test initializes the UARTs and attempts to print the PROM revision level. If it fails, the test loops for about 5 minutes, then the program continues to the next test. It attempts to write to the UART; however, it may not succeed.

Segment Tests

Test 21: Segment Constants — This writes the values 0xaa, 0x00, 0xff and 0x23 to the segment map starting at context 7 and working down to 0.

Failure Mode — Tests 21 through 23 perform three actions upon failure: a) they repeat the failed action indefinitely, b) they display the test number in binary on the CPU LEDs, and c) they attempt to write a failure message to the terminal. The message identifies the test, and what was expected and obtained. (EXAMPLE - Segment NNN Exp NNN Obs YYY)

Test 22: Segment Address Unique — This test writes the values 0x00 through 0xff in each context to the segment maps, then reads back the result. This test may miss MSB (256 values over 512 entries) or context decoding problems, but the checkertest should catch those. Uses byte access in fc3.

Test 23: Segment Checkertest — This test writes a pattern of 0x55 then 0xaa on the area under test, then doubles the size of the pattern and repeats the test until the pattern = 1/2 times the area. It reads back the area to ensure it returns the right pattern.

Page Tests

Test 24: Page Constants — This test writes the values 0xaaxxaaa, 0x000xx000, 0xfffxxfff, 0x555xx555 and 0x213xx731 to the page maps, then reads them, verifying that it receives what it wrote. Note that in page maps, the middle two numbers (xx) are undefined. Uses long access in fc3 space.

Failure Mode: When page tests (tests 24, 25, and 26) find an error, they continue to test the offending address while displaying the test number in binary on the CPU LEDs. They attempt

to write a message to the terminal; this identifies the test, what was expected, and what was observed.

Test 25: Page Unique — Writes the values 0x000xxfff through 0x000xx000 to the page maps to determine that page decoding is unique. Uses access in fc3 space.

Test 26: Page Checkertest — This runs the same as Test 23, except uses 0xaaaxxaaa pattern on page maps. Uses long access in fc3.

Memory Tests

Test 30: Memory Sizing — This test determines the amount of memory installed by mapping the first 4 Mbytes, then doing a byte write to the last location of each 1 Mbyte chunk, starting at 4 Mbytes and working backwards. The first Mbyte found is the memory size, which is reported on the terminal and used for subsequent memory tests. If it finds no memory, it prints the address of the last read, the page map involved, and the virtual address of the attempt.

Failure Mode: Memory errors in tests 30 through 34 cause the program to enter a loop which repeats 64K times, prints the last value it received out to the terminal, then continues. While the program is repeating, the user can a) type a "b" to cause the diagnostics to start over, b) type an "s" to skip memory tests (skips to Test 35), or c) type any other key to continue to the next memory test. If left alone, the tests loop indefinitely when they find failures.

Test 31: Memory Constants — This test writes, then reads a series of constants to or from memory. It uses long accesses in fc6 space.

Test 32: Memory Unique — This test writes the virtual address of every location to that location, then reads back that address. it uses long accesses in fc6 space.

Test 33: Random Addressing — This test writes random numbers to memory then reads them back. It uses long accesses in fc6 space.

Test 34: to main memory. It uses a pattern 0xaaaaaaaa, and takes a long time to complete, especially in machines with large memories. It uses a long access in fc6 space.

Parity Tests

Test 35: Parity Function — This test writes the values 0x0000, 0x0001, 0x1000 and 0x1001 to memory, then checks for parity errors. Then it sets the parity generator bit in the system enable register to cause a parity error, and re-writes the same four values to memory. Now it checks to ensure that the right parity error is generated for each value. Uses word accesses in fc6.

Failure Mode: If test 35 passes, it indicates that the parity circuit is working; if this test fails, finding the cause requires skilled investigation; as many different conditions can cause it to fail.

On the positive side, except for the menu tests and the memory tests, virtually any failures indicate problems on the CPU board. In the case of parity problems, determining exactly where the failure is on the CPU board is NOT easy or straightforward.

When it encounters a failure, the parity function test returns a message:

```
Unexpected bus error - XXXXXX
```

Test 36: Parity validity — This test writes odd and even parity combinations to all of memory and checks to ensure parity protection works.

Failure Mode: The parity validity test reads then decodes the buss error register; it reports one of the following:

```
lower parity
upper parity
timeout
protection error
P1 master
page invalid.
```

Test 37: Page map access/modify bits — This test maps in a page of memory and performs both read and write access to it. The test checks to ensure that the proper accessed and modified bits are set.

Failure Mode: If it finds errors, test 37 prints either:

```
access test exp NNN obs YYY, or
modify test exp NNN obs YYY
```

Test 38: Page permissions on — This test turns on permission bits, then tries a number of accesses to ensure permission bits allow accesses.

Failure Mode: When test 38 finds an error, it prints:

```
buserror berrNN spaceNN writeNN page0xAA
```

Test 39: Page permissions off — This test turns off permission bits, then tries a number of accesses to ensure permission bits disallow accesses.

Failure Mode: When test 39 finds an error, it prints:

```
mismatch berrNN expNN fcNN wNN page0xAA
no buserror!! fcNN wNN page0xAA
```

Test 40: Page invalid — This test attempts an access to an invalid page, then verifies the bus error.

Failure Mode: When test 40 finds an error, it prints:

```
mismatch berr NN expNN page0xAA
no buserror!! page0xAA
```

Test 41: Interrupts — This test checks interrupt levels 1 thorugh 3 and 5 through 7 to ensure they occur. Level 7 uses the 9513 timer (OUT5), level 6 uses the SCC, level 5 uses the 9513 again (OUT4), and levels 1 through 3 use the system enable register to generate their interrupts.

Failure Mode: When test 40 finds an error, it prints:

```
Got level X instead of Y, or
No interrupt on level X
```

Video Menu Tests

Register test
sets the video, copy, and interrupt enables, and the copy base. It reads these and the other known bits in the video control register back, then checks to ensure that the settable bits read the way they were written.

(Video) memory test
runs a series of general memory tests on the video frame buffer. THIS TEST CAUSES PATTERNS TO APPEAR ON THE VIDEO MONITOR.

(Video) copy test
runs a series of general memory tests on the video frame buffer using copy mode. It then checks both the frame buffer and the memory written. THIS TEST CAUSES PATTERNS TO APPEAR ON THE VIDEO MONITOR.

Ethernet Menu Tests

Diagnose
The diagnose test sets the 82586 chip initialization then tries to do it. If the reset fails, the test loops on the reset.

Loop tests (local, encoder, external) — These tests do local loopbacks.

local
does internal loopbacks in the 82586

encoder
does loopback through the 8502 (sends headers only)

external
does loopback through the Ethernet cable (sends headers only and requires cable and functioning Ethernet).

Failure Mode: Loop tests note any deviation from expected results and dump relevant data structures. External loop test fails if Ethernet is not connected right.

Dump test
dumps the data and command structures used ty the 82586 in memory. The results of this test are beyond the scope of this document.

Memory Menu Tests

map — Detail to be provided

pattern — details to be provided

address/unique — details to be provided

Failure Mode: Memory tests loop when they detect failures.

2.5. Standalone Programs

Standalone programs get their name from the fact that they run in a standalone environment, without UNIX. They are booted manually while the workstation is under control on the monitor, after its autoboot procedure is interrupted.

As troubleshooting tools, standalone programs have two major advantages over programs that run under UNIX:

a) UNIX restricts access to facilities that these programs need, and

b) often when standalone programs are required, the system isn't running well enough for UNIX to run properly.

Environment

Standalone programs require a fairly high level of system functionality to run effectively. The monitor program must run, and the path to the standalone programs over the Ethernet must be functioning. If these conditions cannot be met, use other troubleshooting tools described in this chapter.

To activate the monitor's command interpreter, power-on or reset the system. When the message:

```
Auto-boot in progress
```

appears, press either:

L1-a
(while holding down "L1", press "a") from the keyboard,

k1 (press "k", "1", then <return>) from the keyboard, or

BREAK
(press the "break" key) from a terminal. The monitor should respond by interrupting the current process and displaying a "greater than" symbol (>), which is its prompt.

To exit the monitor and resume the normal boot procedure, type:

k2 (type "k", "2", then <return>) from the keyboard or terminal.

When the prompt is displayed, you can execute programs by entering the path name, just like in UNIX. The names and paths to the relevant standalone programs are:

Name/Location Function

THE STANDALONE PROGRAMS AND HOW TO USE THEM TO BE PROVIDED

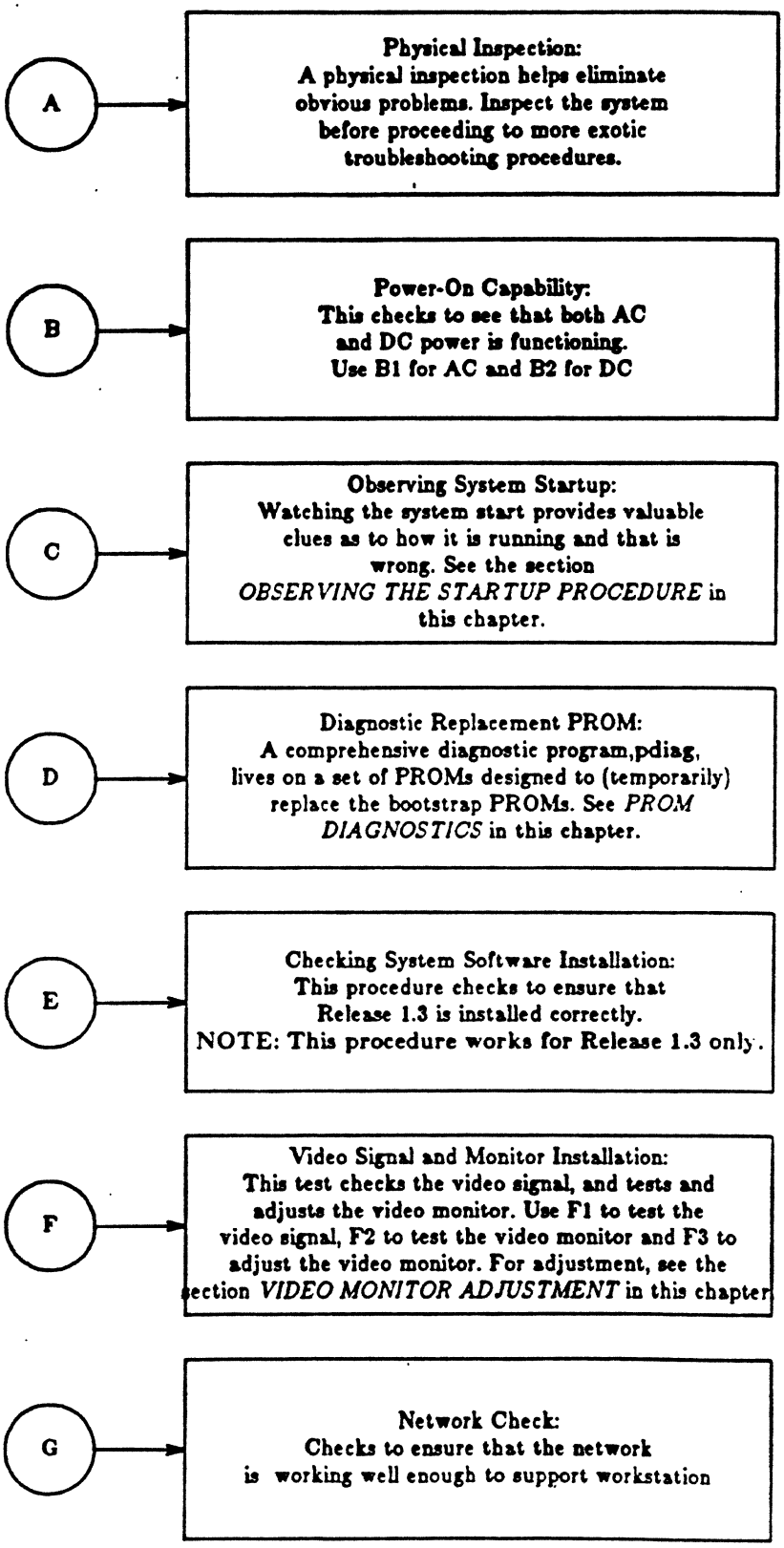
2.6. Quick Reference Troubleshooting Guide

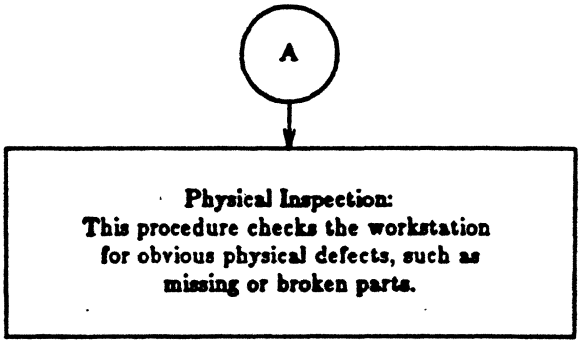
This section contains the Quick Reference Troubleshooting Guide. It is a flowchart designed to help you in two different ways:

a) it can guide you to one of the other procedures in this chapter.

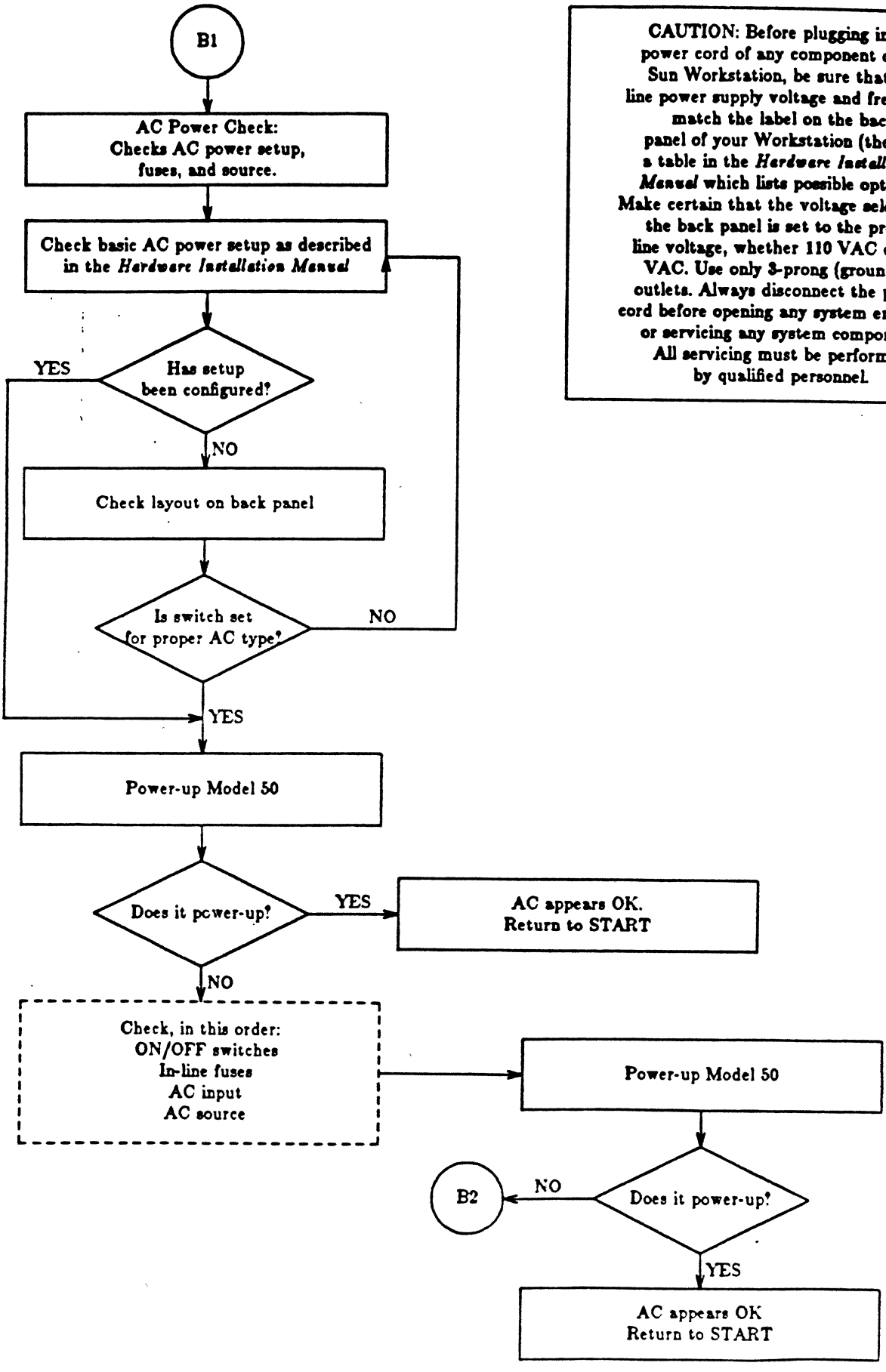
b) it contains two useful procedures; one to ensure that the network file server has the the correct version of the operating system installed and that it is complete, and another to adjust the video monitor.

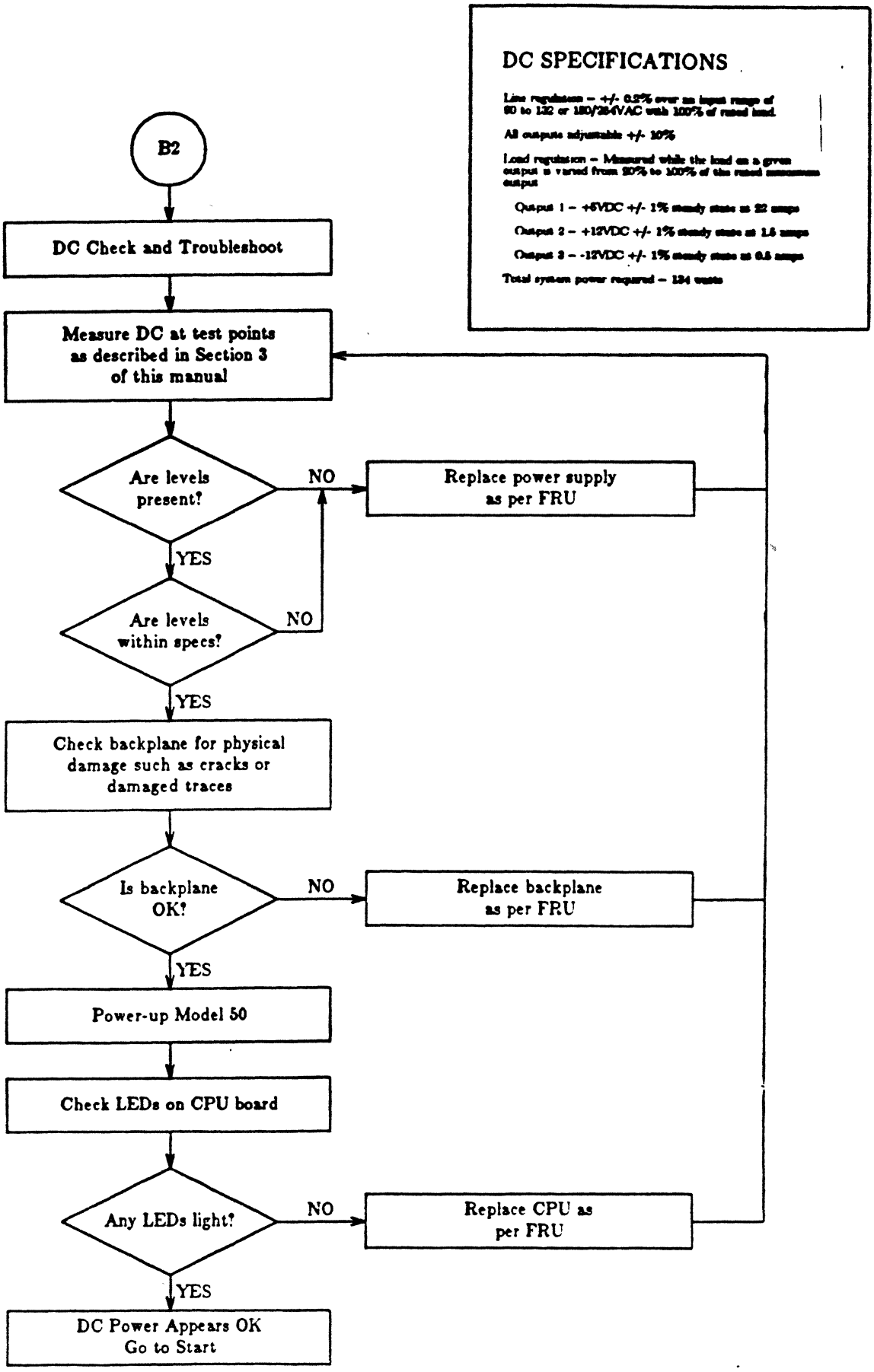
FLOWCHART

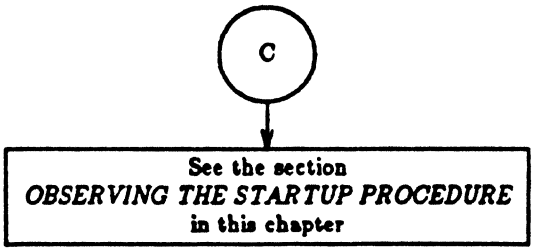

A
Physical Inspection:
A physical inspection helps eliminate obvious problems. Inspect the system before proceeding to more exotic troubleshooting procedures.
B
Power-On Capability:
This checks to see that both AC and DC power is functioning.
Use B1 for AC and B2 for DC
C
Observing System Startup:
Watching the system start provides valuable clues as to how it is running and that is wrong. See the section
OBSERVING THE STARTUP PROCEDURE in this chapter.
D
Diagnostic Replacement PROM:
A comprehensive diagnostic program,pdiag, lives on a set of PROMs designed to (temporarily) replace the bootstrap PROMs. See PROM DIAGNOSTICS in this chapter.
E
Checking System Software Installation:
This procedure checks to ensure that Release 1.3 is installed correctly.
NOTE: This procedure works for Release 1.3 only.
F
Video Signal and Monitor Installation:
This test checks the video signal, and tests and adjusts the video monitor. Use F1 to test the video signal, F2 to test the video monitor and F3 to adjust the video monitor. For adjustment, see the section VIDEO MONITOR ADJUSTMENT in this chapter.
G
Network Check:
Checks to ensure that the network is working well enough to support workstation

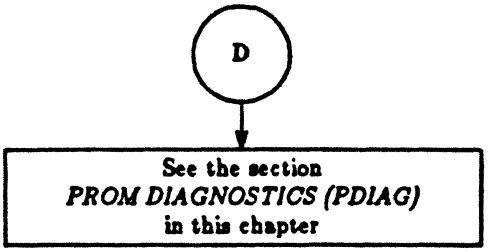


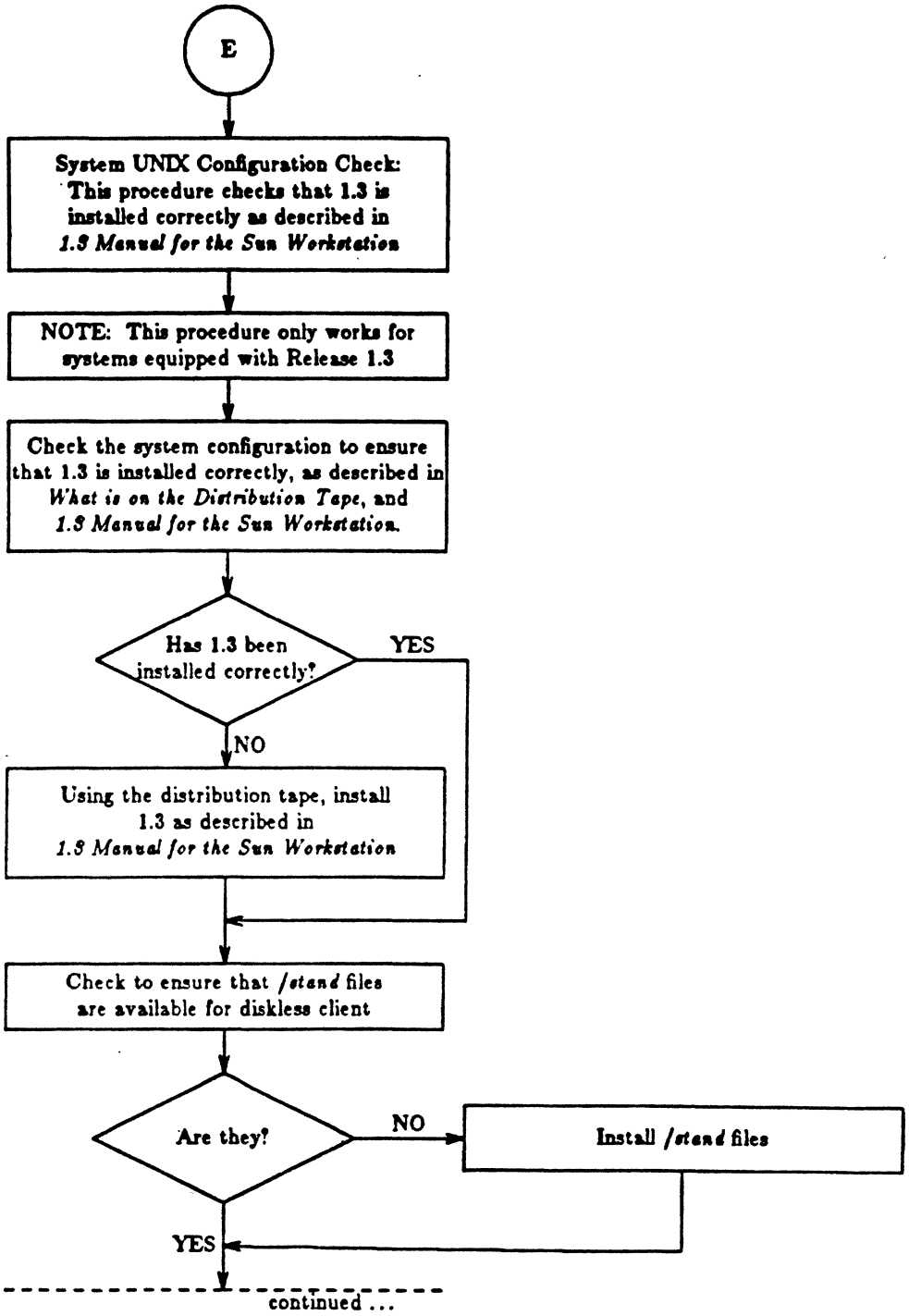
The physical inspection procedure is in the *Hardware Installation Manual*.

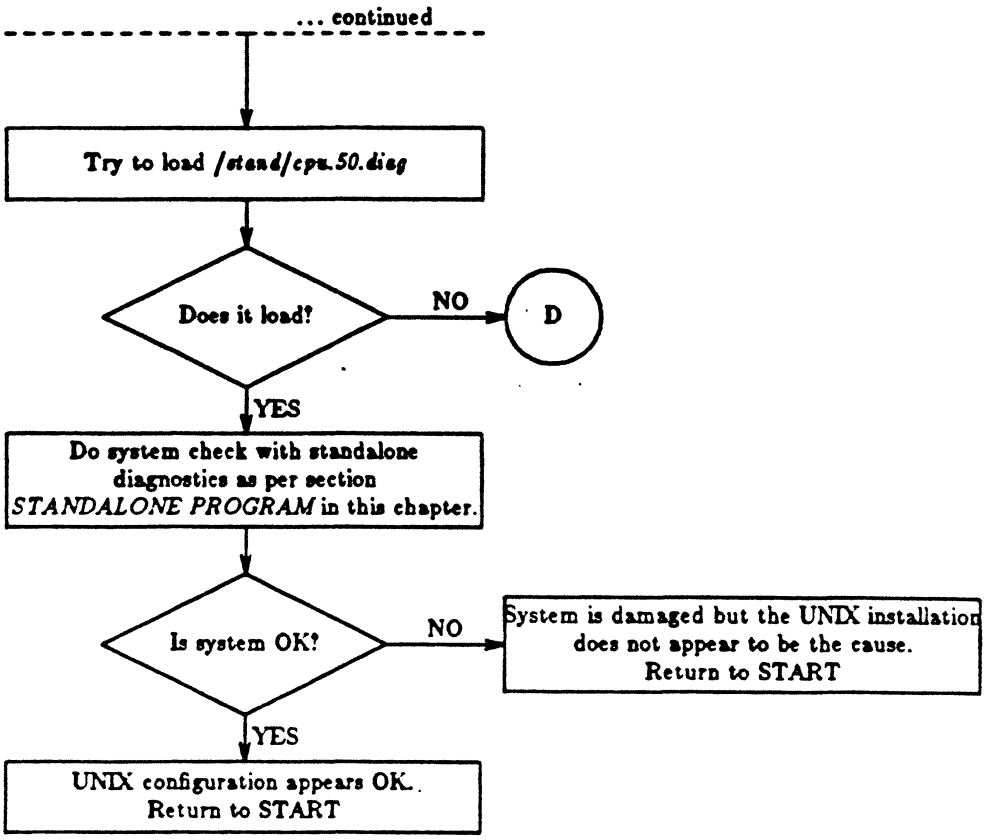

B1
AC Power Check:
Checks AC power setup,
fuses, and source.
Check basic AC power setup as described
in the Hardware Installation Manual
YES
Has setup
been configured?
NO
Check layout on back panel
Is switch set
for proper AC type?
NO
YES
Power-up Model 50
Does it power-up?
YES
AC appears OK.
Return to START
NO
Check, in this order:
ON/OFF switches
In-line fuses
AC input
AC source
Power-up Model 50
B2
NO
Does it power-up?
YES
AC appears OK
Return to START
CAUTION: Before plugging in the
power cord of any component of the
Sun Workstation, be sure that the
line power supply voltage and frequency
match the label on the back
panel of your Workstation (there is
a table in the Hardware Installation
Manual which lists possible options).
Make certain that the voltage selector on
the back panel is set to the proper
line voltage, whether 110 VAC or 220
VAC. Use only 3-prong (grounded)
outlets. Always disconnect the power
cord before opening any system enclosure
or servicing any system component.
All servicing must be performed
by qualified personnel.


DC SPECIFICATIONS
Line regulation – +/- 0.2% over an input range of 90 to 132 or 180/264VAC with 100% of rated load.
All outputs adjustable +/- 10%
Load regulation – Measured while the load on a given output is varied from 20% to 100% of the rated maximum output
Output 1 – +5VDC +/- 1% steady state at 22 amps
Output 2 – +12VDC +/- 1% steady state at 1.5 amps
Output 3 – -12VDC +/- 1% steady state at 0.5 amps
Total system power required – 134 watts
B2
DC Check and Troubleshoot
Measure DC at test points as described in Section 3 of this manual
Are levels present?
NO
Replace power supply as per FRU
YES
Are levels within specs?
NO
YES
Check backplane for physical damage such as cracks or damaged traces
Is backplane OK?
NO
Replace backplane as per FRU
YES
Power-up Model 50
Check LEDs on CPU board
Any LEDs light?
NO
Replace CPU as per FRU
YES
DC Power Appears OK Go to Start


C
See the section
OBSERVING THE STARTUP PROCEDURE
in this chapter


D
See the section
PROM DIAGNOSTICS (PDIAG)
in this chapter


E
System UNIX Configuration Check: This procedure checks that 1.3 is installed correctly as described in 1.3 Manual for the Sun Workstation
NOTE: This procedure only works for systems equipped with Release 1.3
Check the system configuration to ensure that 1.3 is installed correctly, as described in What is on the Distribution Tape, and 1.3 Manual for the Sun Workstation.
Has 1.3 been installed correctly?
YES
NO
Using the distribution tape, install 1.3 as described in 1.3 Manual for the Sun Workstation
Check to ensure that /stand files are available for diskless client
Are they?
NO
Install /stand files
YES
continued ...


... continued
Try to load /stand/cpu.50.diag
Does it load?
NO
D
YES
Do system check with standalone diagnostics as per section STANDALONE PROGRAM in this chapter.
Is system OK?
NO
System is damaged but the UNIX installation does not appear to be the cause. Return to START
YES
UNIX configuration appears OK. Return to START

What is on the Distribution Tape?

Distribution of the 1.3 Release binaries is either on a 1/4" magnetic tape cartridge or a 1/2" nine-track tape. The tapes contain eight files, as follows:

File 1: Boot block.
A general-purpose boot program which knows how to boot from the various devices that can be attached to the Sun Workstation. The PROM monitor boots this general-purpose boot program.

File 2: Bootable *diag* program.
This is a new version of *diag*, the disk formatting and labelling program; this version has enhanced diagnostic capabilities. For more information on changes in this version, see Chapter 3 of the *1.3 Manual for the Sun Workstation*, *Supplemental diag Release Documentation*.

File 3: Copyright file.

File 4: *tar* file of the installation utility.
A script which handles both installation and (if necessary) 'un-installation' of any incremental release.

File 5: *tar* file of replacement 1.3 binaries.
A *tar* format file of the replacement 1.3 object files, executable files, and libraries.

File 6: *tar* file of 1.1 binaries.
A backup version of the binaries replaced by File 5 of the tape, in case you need to back out the 1.3 changes.

File 7: *tar* file of new/revised manual pages.
These are the online versions of the material contained in Chapter 6 of this manual.

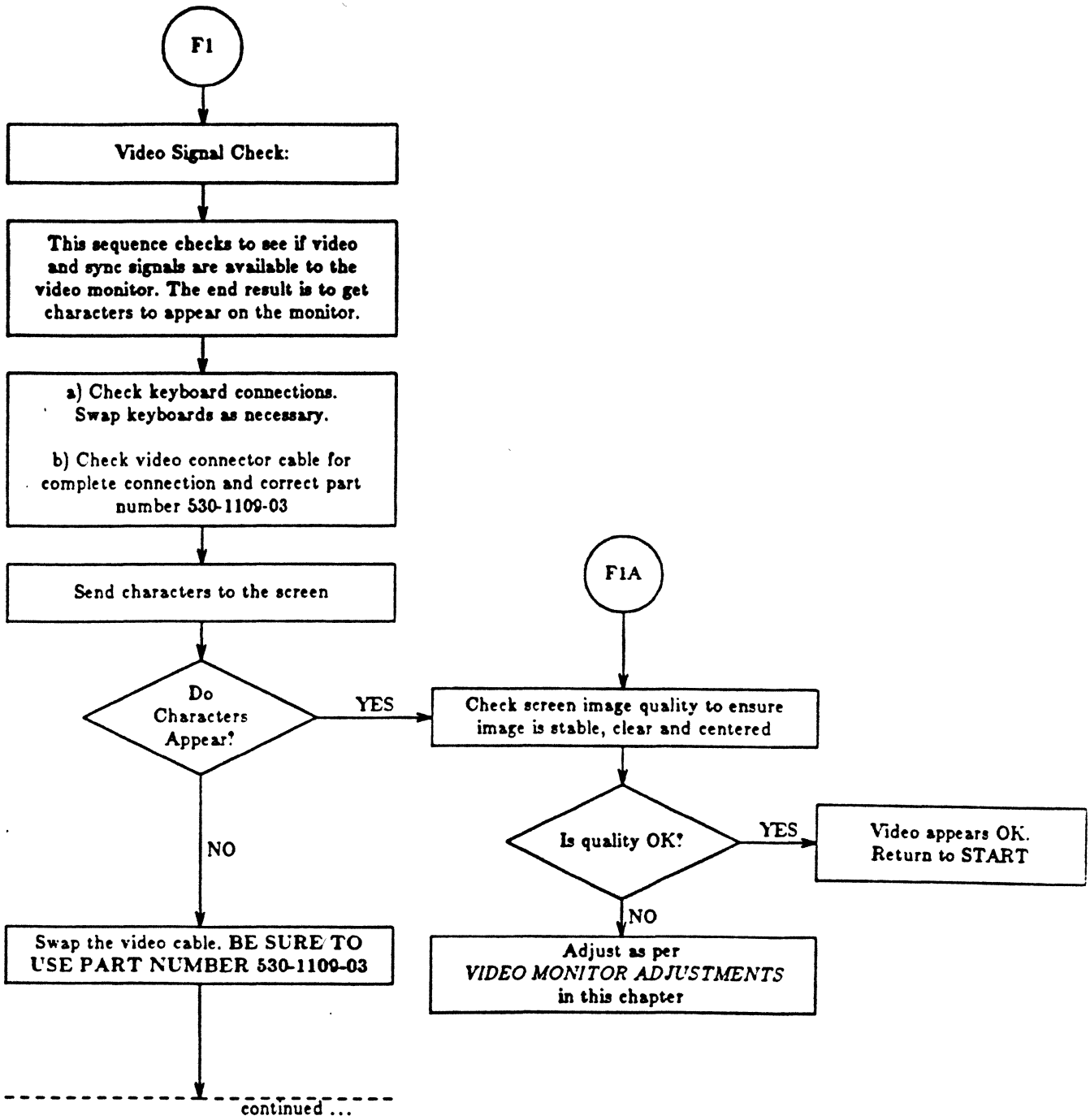
File 8: Copyright file.

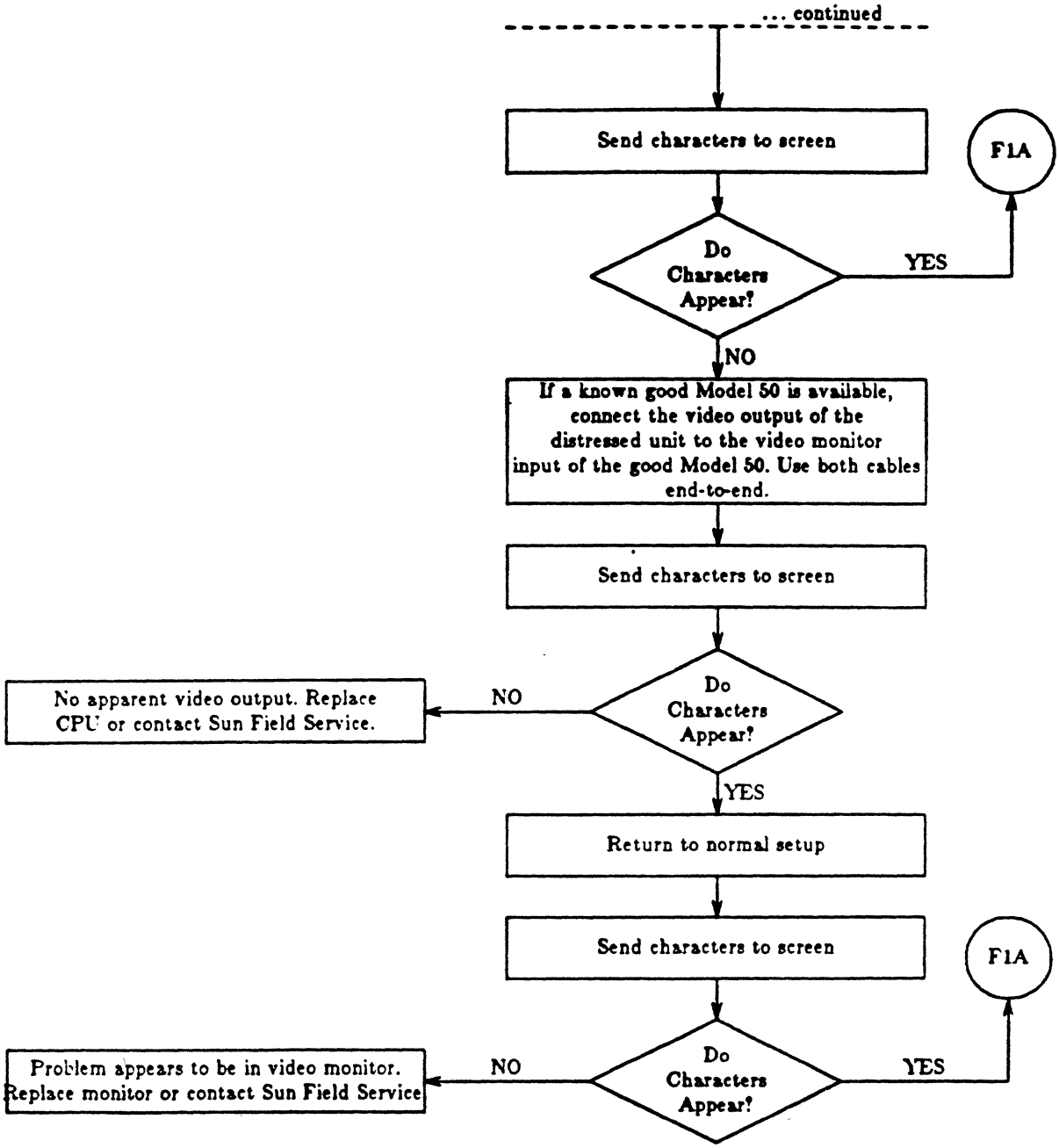
Overview of the Installation Procedure

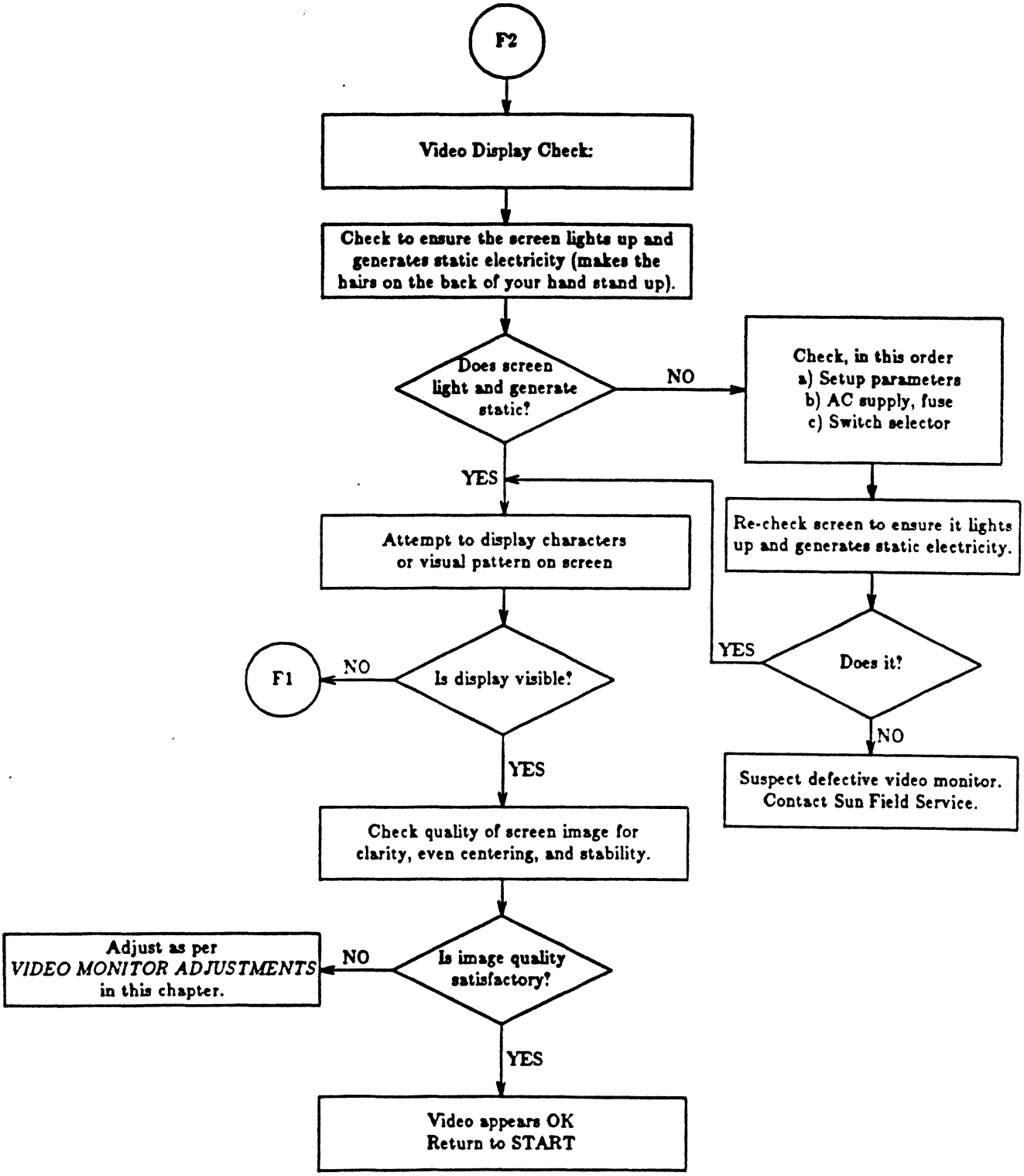
The object of this exercise is to load the Release 1.3 binaries from the magnetic tape onto your local or network disk subsystem.

The basic steps in installation are:

1. Load the tape.
2. Load the 1.3 installation utility.
3. If you are installing a server, halt any diskless clients.
4. Run the installation utility.
5. Optionally, use the *tar*(1) command to extract the new or revised manual pages for your online documentation.
6. Reconfigure your system kernel.


F1
Video Signal Check:
This sequence checks to see if video and sync signals are available to the video monitor. The end result is to get characters to appear on the monitor.
a) Check keyboard connections. Swap keyboards as necessary.
b) Check video connector cable for complete connection and correct part number 530-1109-03
Send characters to the screen
Do Characters Appear?
YES
NO
Swap the video cable. BE SURE TO USE PART NUMBER 530-1109-03
continued ...
F1A
Check screen image quality to ensure image is stable, clear and centered
Is quality OK?
YES
Video appears OK. Return to START
NO
Adjust as per VIDEO MONITOR ADJUSTMENTS in this chapter


... continued
Send characters to screen
F1A
Do Characters Appear?
YES
NO
If a known good Model 50 is available, connect the video output of the distressed unit to the video monitor input of the good Model 50. Use both cables end-to-end.
Send characters to screen
Do Characters Appear?
NO
No apparent video output. Replace CPU or contact Sun Field Service.
YES
Return to normal setup
Send characters to screen
F1A
Do Characters Appear?
NO
YES
Problem appears to be in video monitor. Replace monitor or contact Sun Field Service

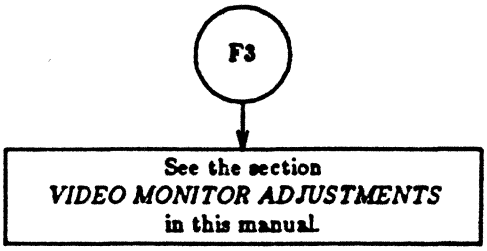

F2
Video Display Check:
Check to ensure the screen lights up and generates static electricity (makes the hairs on the back of your hand stand up).
Does screen light and generate static?
NO
Check, in this order
a) Setup parameters
b) AC supply, fuse
c) Switch selector
YES
Attempt to display characters or visual pattern on screen
Re-check screen to ensure it lights up and generates static electricity.
F1
NO
Is display visible?
YES
Does it?
NO
YES
Suspect defective video monitor. Contact Sun Field Service.
YES
Check quality of screen image for clarity, even centering, and stability.
Adjust as per
VIDEO MONITOR ADJUSTMENTS
in this chapter.
NO
Is image quality satisfactory?
YES
Video appears OK
Return to START

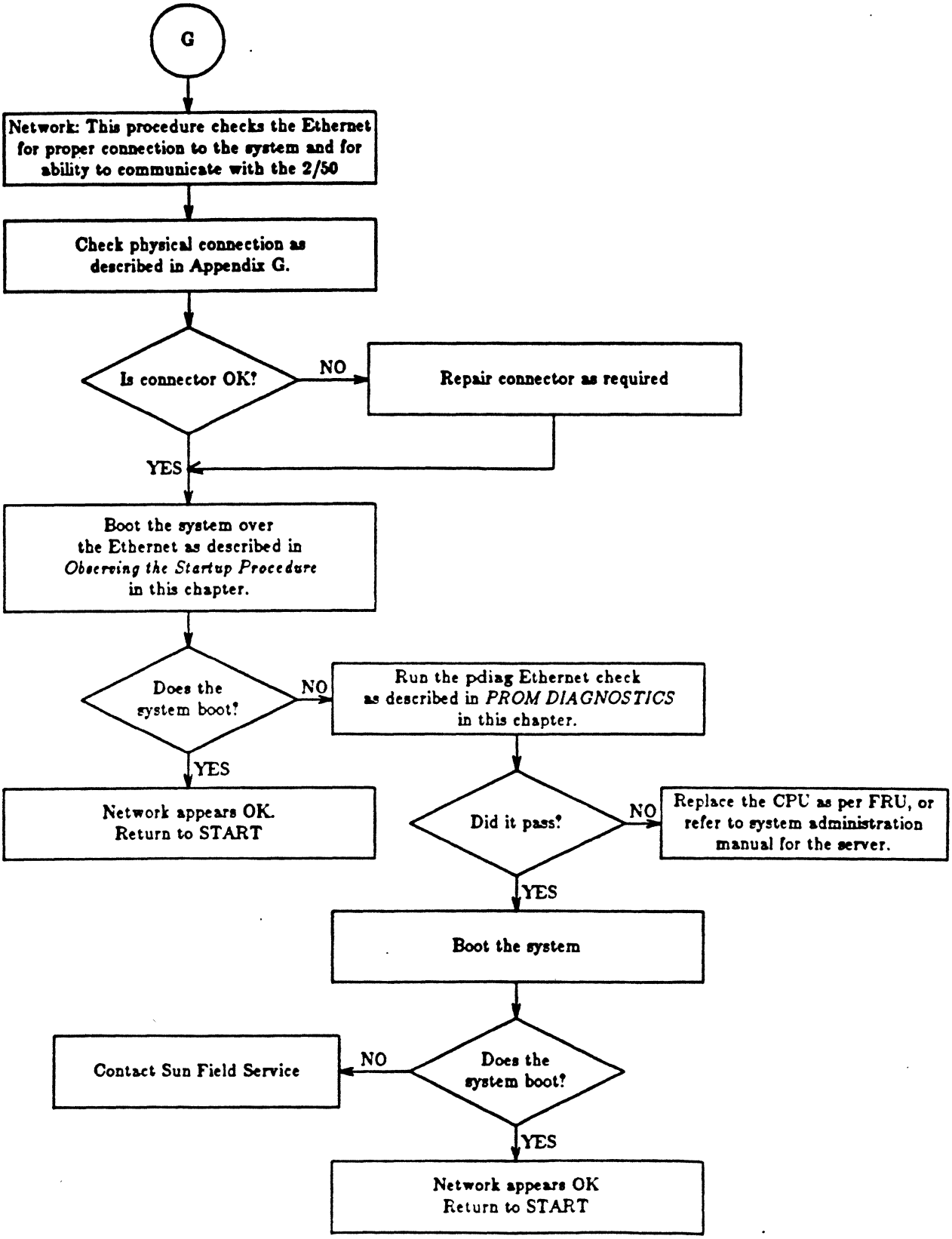
VIDEO MONITOR ADJUST AND REPAIR

NOTE: The Sun Model 50 comes with two types of video monitor; one by Phillips and the other by Moniterm. In this procedure, both are treated the same; however, for further information, each has its own manual. The part numbers appear in the List of Applicable Documents in this manual.

Both video monitors meet the following specifications:

- Video Input — Balanced ECL
- Video Display — 1152 X 900 pixel display (1024 X 1024 optional)
- Video Clock — 10 nsec, 100 MHz
- Horizontal Sync — 16000 usec, 62.5KHz
- Vertical Sync — 15000 usec, 66.66kHz
- Horizontal Retrace — 4.48 usec
- Vertical Retrace — 600 usec


F3
See the section
VIDEO MONITOR ADJUSTMENTS
in this manual.


G
Network: This procedure checks the Ethernet for proper connection to the system and for ability to communicate with the 2/50
Check physical connection as described in Appendix G.
Is connector OK?
NO
Repair connector as required
YES
Boot the system over the Ethernet as described in Observing the Startup Procedure in this chapter.
Does the system boot?
NO
Run the pdiag Ethernet check as described in PROM DIAGNOSTICS in this chapter.
YES
Network appears OK. Return to START
Did it pass?
NO
Replace the CPU as per FRU, or refer to system administration manual for the server.
YES
Boot the system
Contact Sun Field Service
NO
Does the system boot?
YES
Network appears OK Return to START

3

Maintenance

3

Maintenance

This section contains the information necessary to remove and replace all components of the Sun-2/50 SunStation designated as field replacable units (FRUs).

3.1. Printed Circuit Board Removal

The CPU board (Sun P/N 501-1005-050) and optional Memory Expansion Board (3MB- Sun P/N 501-1067-01, 4MB- Sun P/N 501-1047-03) are located in a card-cage in the Sun-2/50 chassis. Both boards are attached to the rear panel assembly (Sun P/N 340-1171-01). Remove the rear panel and the two circuit boards as follows:

a. If the system is configured with the optional Memory Expansion board, remove the four screws securing it to the rear panel (see Figure 3-1). If the system is configured with a single board, proceed to step b.

b. Unfasten the ten screws securing the rear panel to the chassis (see Figure 3-1).

c. Insert a screwdriver through the bottom extraction bracket on the rear panel and into the fulcrum bracket on the chassis (see Figure 3-2).

d. Pry outward with the screwdriver to release the CPU board from the back-plane connectors.

e. Withdraw the CPU and rear panel assembly from the chassis (see Figure 3-3).

f. Withdraw the Memory Expansion board (if installed) from the chassis.

g. Installation is the reverse of this procedure. Note that if the CPU board is replaced, the ID PROM must be removed from the original board and reinstalled on the replacement board. Refer to Appendix B for the location of the ID PROM. *The ID PROM is fragile and should be handled with care to avoid damage.*

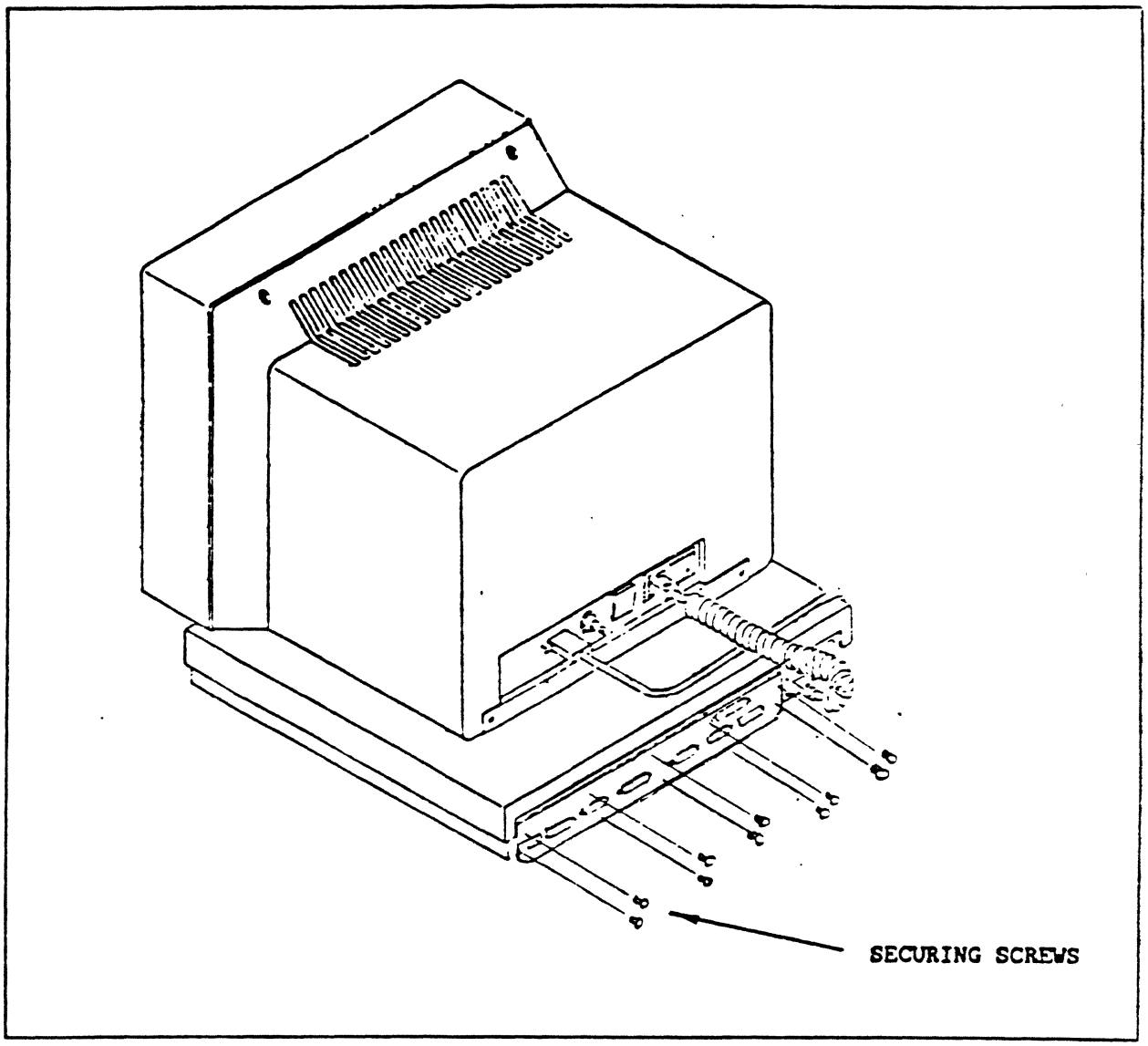


Figure 3-1 *Rear Panel Securing Screws*

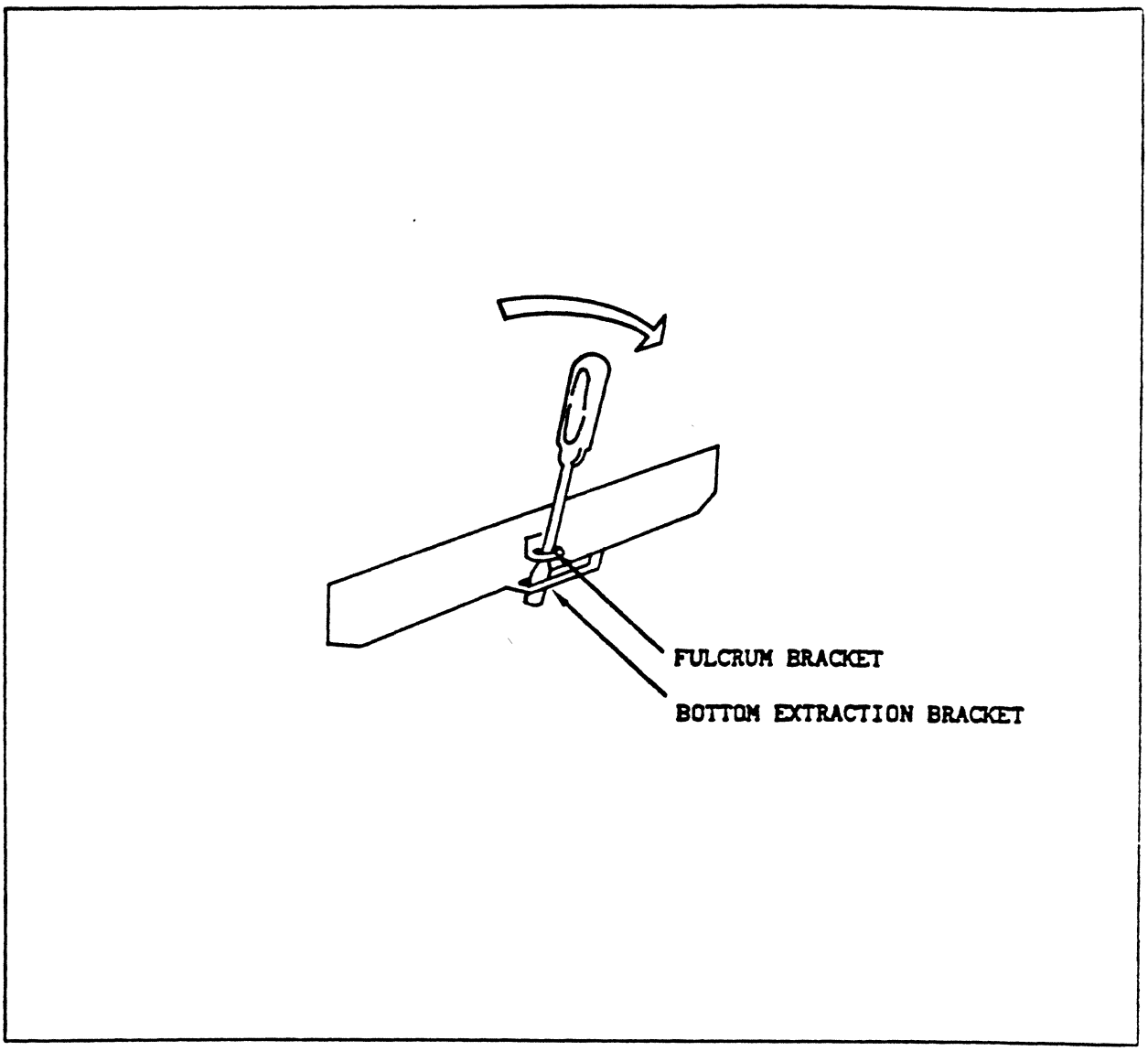


Figure 3-2 *Releasing Backplane Connectors*

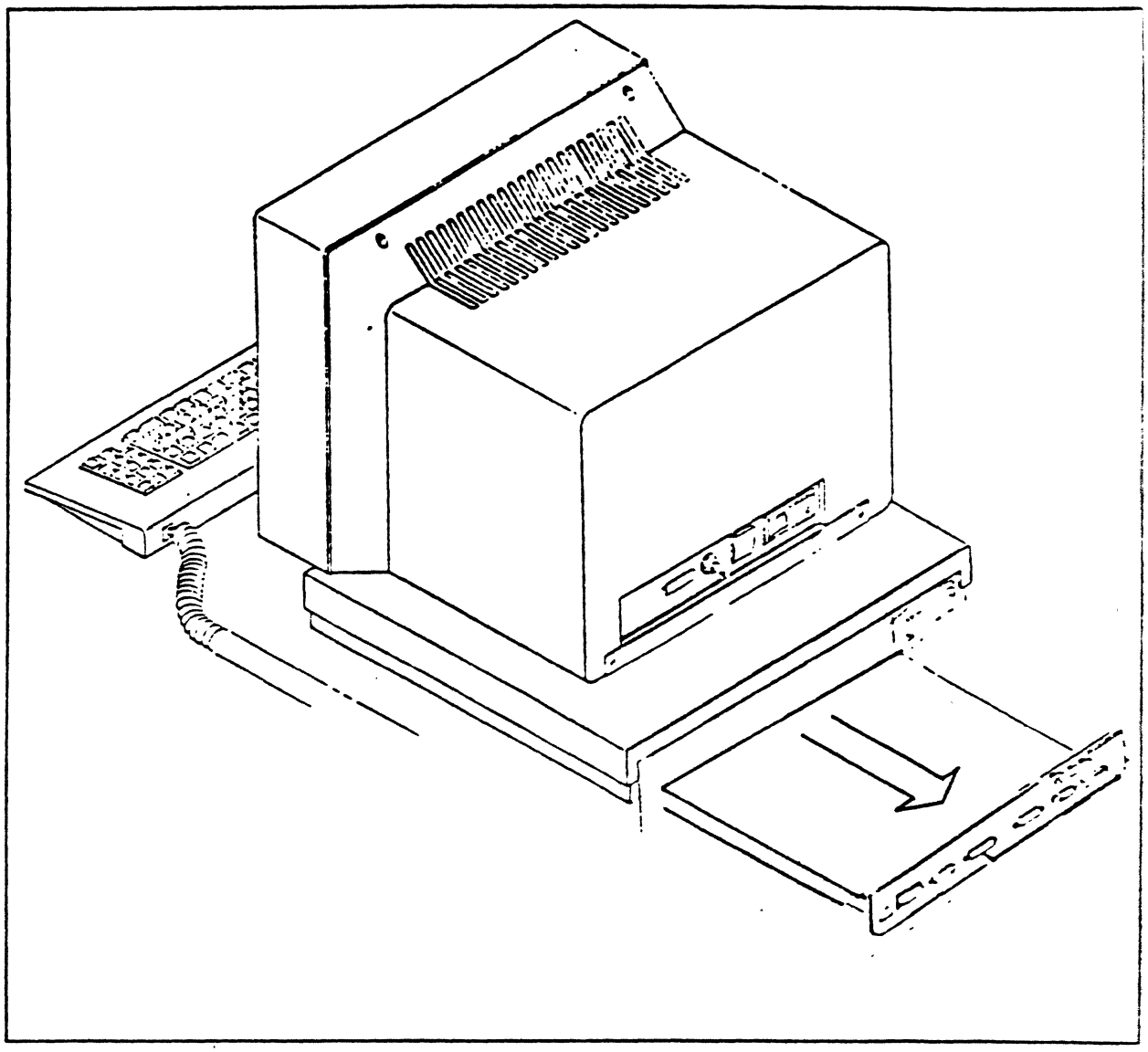


Figure 3-3 *Removing Rear Panel Assembly from Chassis*

3.2. Monitor Removal from Chassis

The monitor (Sun P/N 540-1062-01) rests on top of the Sun-2/50 chassis inside a large, dish-shaped bearing. The monitor attaches to the chassis via a keyway in the monitor cabinet. This keyway fits over a corresponding tee bar mounted in the bearing located in the chassis cover (see Figure 3-4). Remove the monitor from the chassis as follows:

a. Power-down the unit and remove the power and video cables from the rear panel of the monitor.

b. Position the monitor so that the screen is perpendicular to the chassis and rotated ninety degrees to either side of the straight forward position (see Figure 3-5). The keyway on the monitor is now aligned with the tee bar on the

chassis cover.

c. Lift the monitor straight up from the chassis to remove.

d. Installation is the reverse of this procedure.

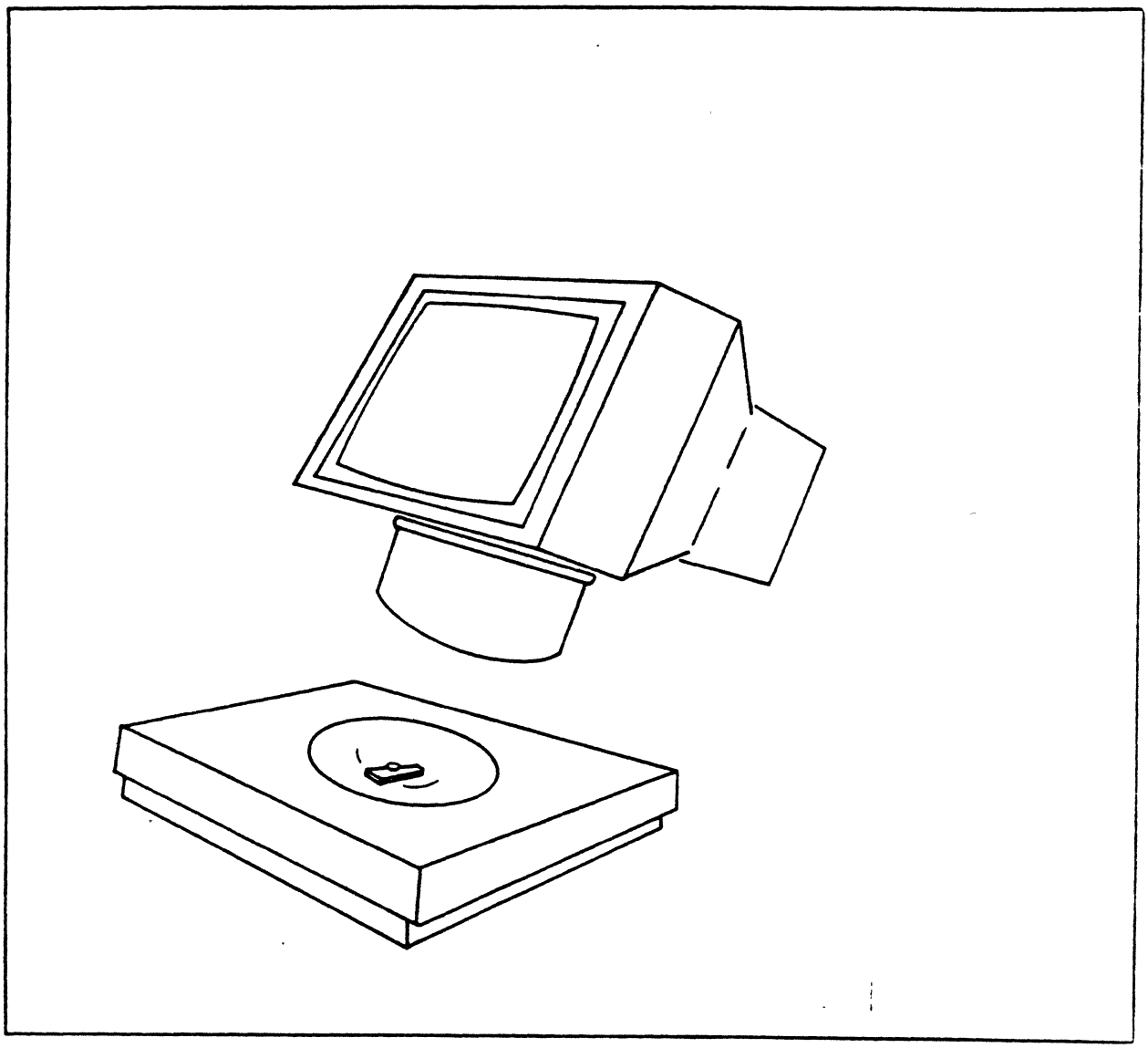


Figure 3-4 *Monitor Mounting*

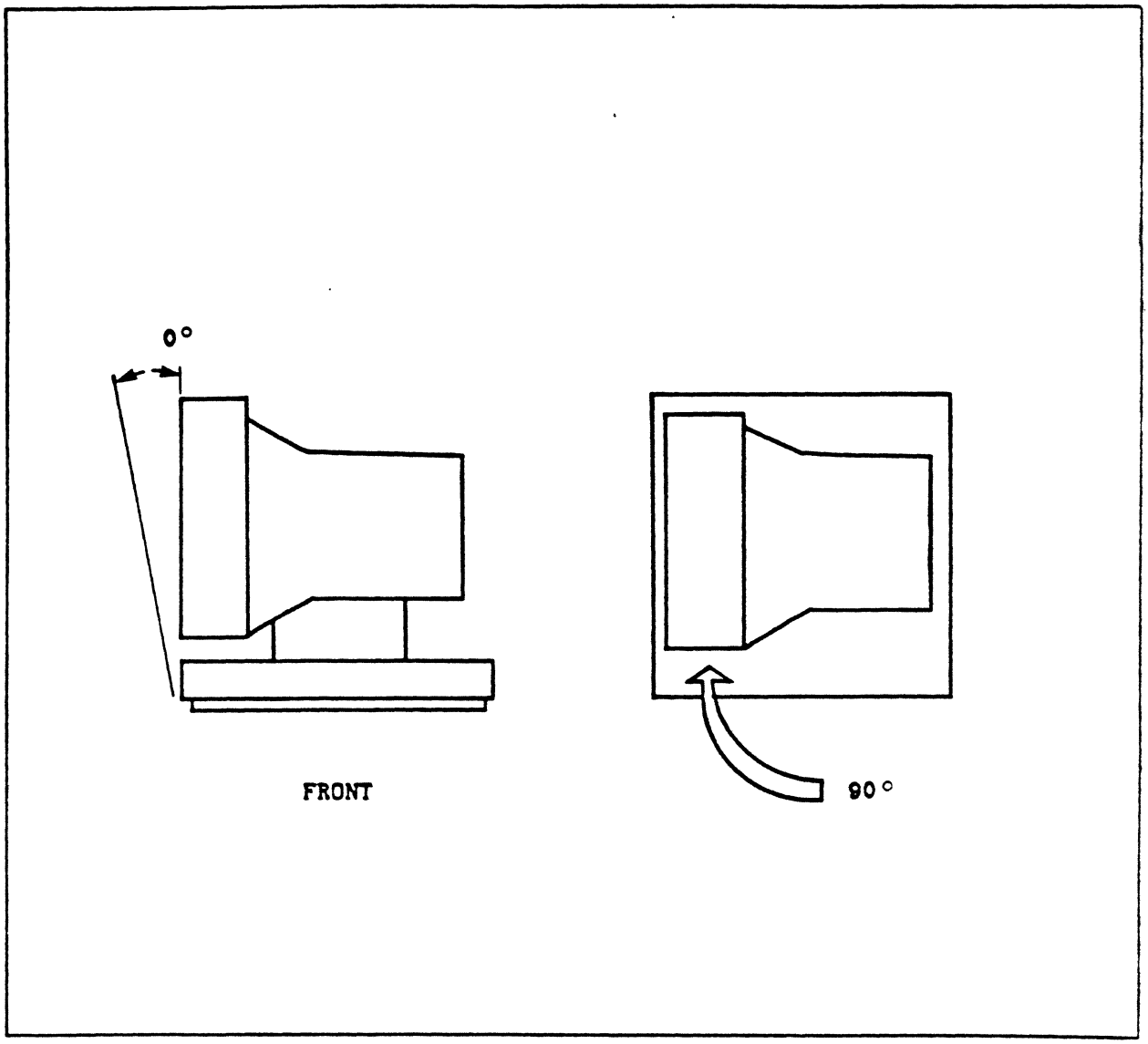


Figure 3-5 *Positioning Monitor for Removal*

3.3. Chassis Cover Removal

a. Power-down the system and remove the monitor as described in in the monitor removal procedure.

b. Disconnect all power and interface cables from the rear panel of the chassis.

c. Place the system chassis on its side.

d. Loosen the four captive studs securing the chassis cover (Sun P/N 540-1100-01). See Figure 3-6.

e. Set the chassis back in the upright position and remove the cover.

f. Installation is the reverse of this procedure.

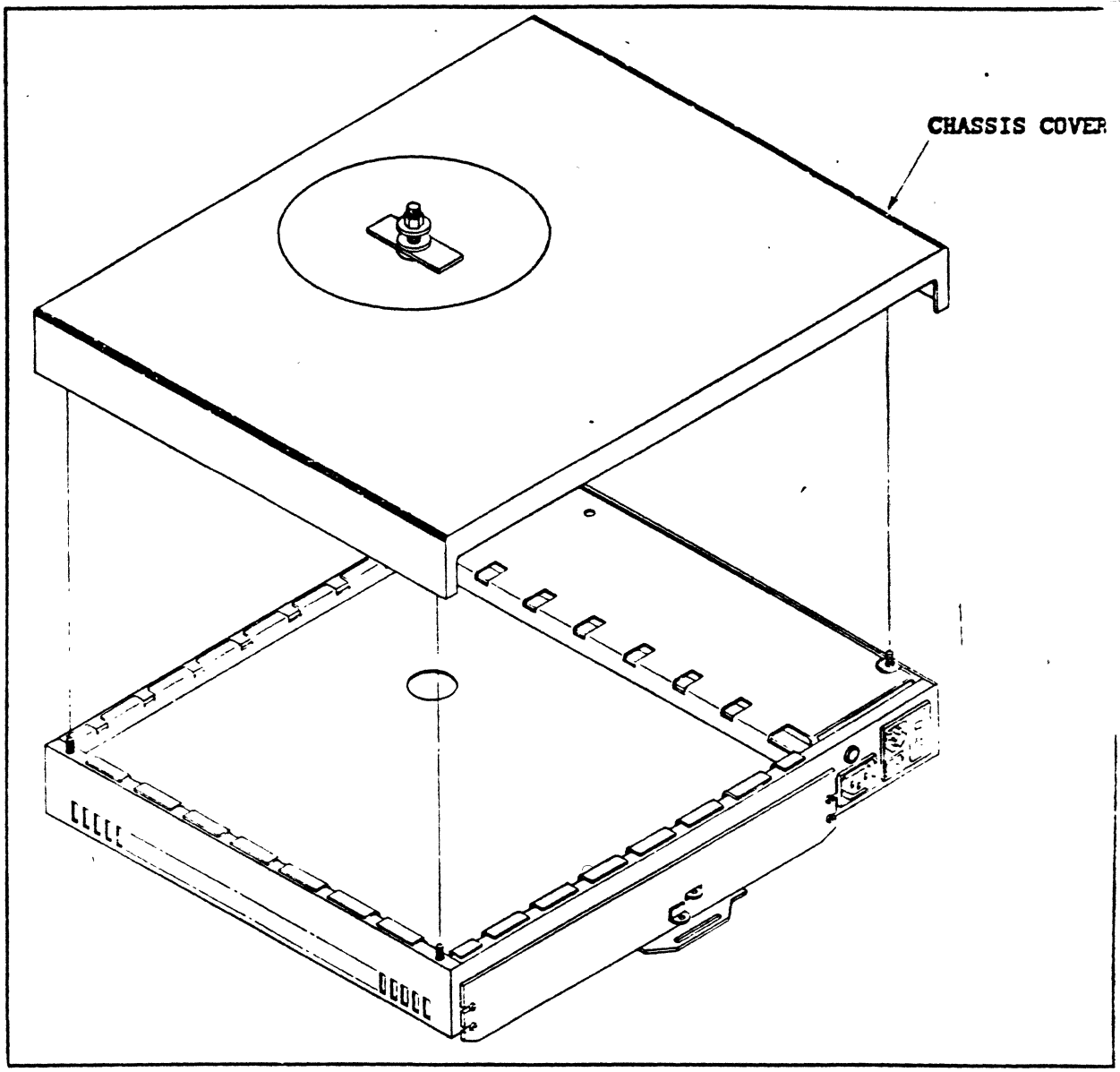


Figure 3-6 *Chassis Cover Removal*

3.4. RFI Shield Removal

a. Remove the monitor and chassis cover as described in previous procedures.

b. Using a screwdriver as a lever, gently pry the RFI shield (Sun P/N 540-1105-01) from the top of the chassis. Do not pry against the metal gasket when removing the cover (see Figure 3-7).

c. The RFI shield is reinstalled by simply snapping it into place.

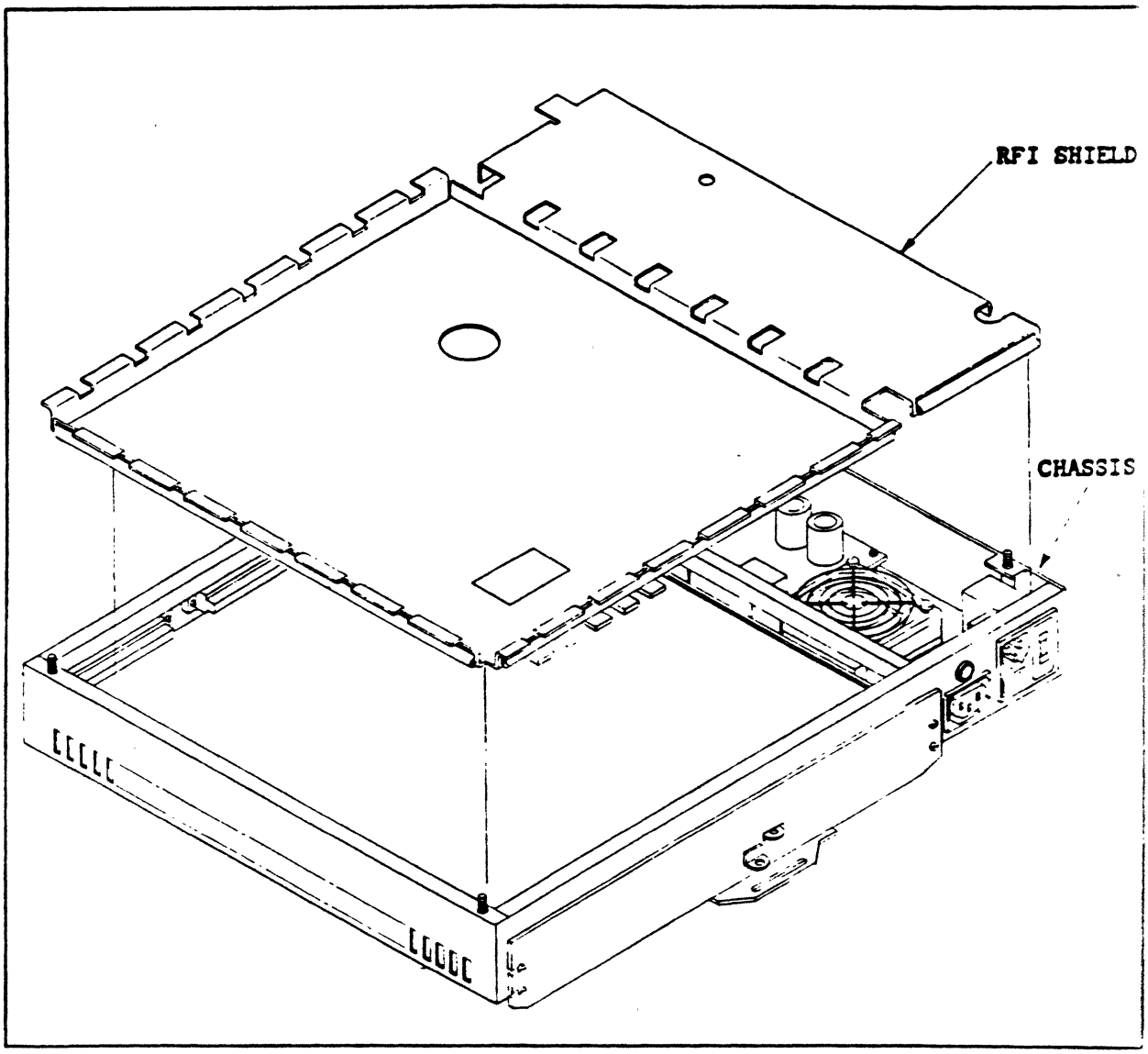


Figure 3-7 *RFI Shield Removal*

3.5. Power Supply Removal

The power supply (Sun P/N 300-1002-01) is contained on a single PCB, located in the system chassis. Remove the power supply as follows:

a. Remove the monitor, chassis cover and RFI shield as described in the previous procedures.

b. Remove the wires from the bayonet connectors on the power supply labelled 115V and 230V (see Figure 3-8, detail A).

c. Unfasten the connectors at J1 and J6. Do not pull on the wires when removing these connectors, as this may damage the pins.

d. Unfasten the four screws securing the power supply board to the chassis. Partially withdraw the power supply from the chassis to expose the six backplane connections (see Figure 3-8, detail B).

e. Disconnect the six backplane connections and remove the power supply from the chassis.

f. When reinstalling the power supply, ensure that the backplane connectors are located as shown in the wiring diagram in Figure 3-8, detail B.

g. Installation is the reverse of this procedure.

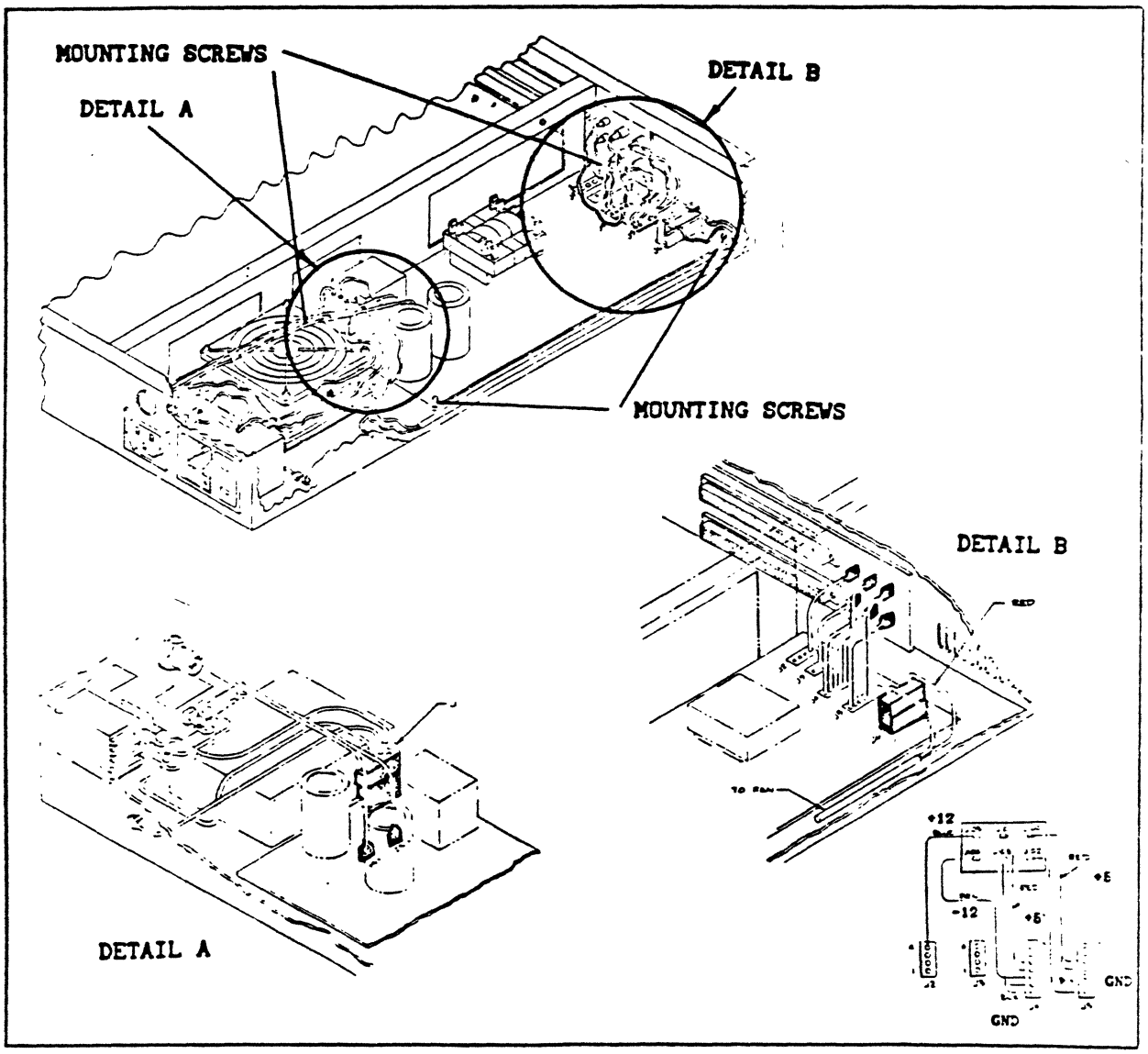


Figure 3-8 *Power Supply Removal*

3.6. Cooling Fan Removal

a. Remove the monitor, chassis cover and RFI shield as described in previous procedures.

b. Unfasten the connector at J6 on the power supply board (see Figure 3-8, detail B).

c. Place the chassis on its side and unscrew the four nuts and bolts securing the fan (Sun P/N 540-1068-02) and fingerguard (Sun P/N 340-1178-01) to the chassis.

d. Remove the fan and fingerguard.

e. Installation is the reverse of this procedure.

3.7. Backplane Removal

a. Remove the PCB, rear panel and power supply as previously described.

b. Unfasten the 12 securing screws and remove the backplane (Sun P/N 501-1042-01). See Figure 3-9.

c. Installation is the reverse of this procedure.

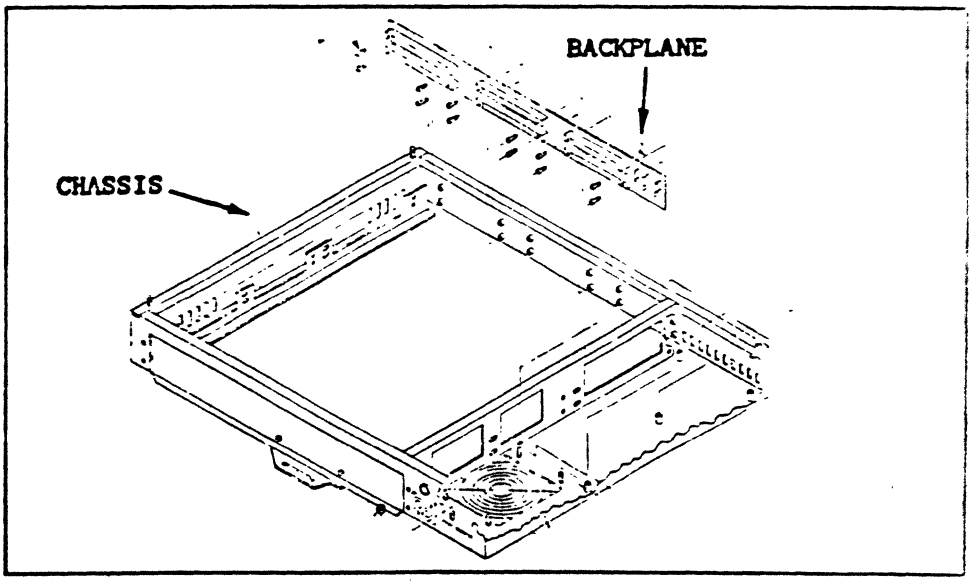
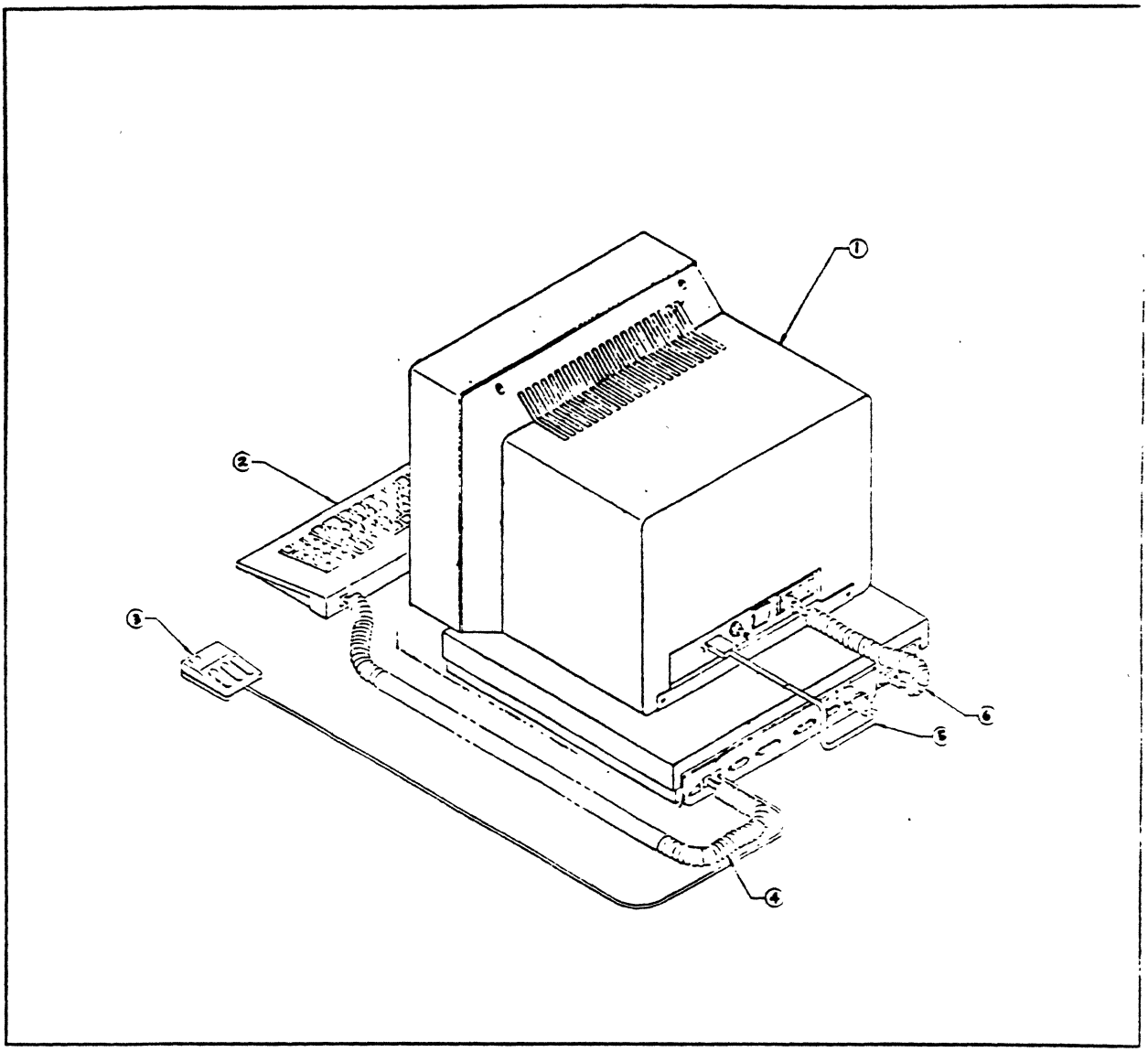


Figure 3-9 *Backplane Removal*

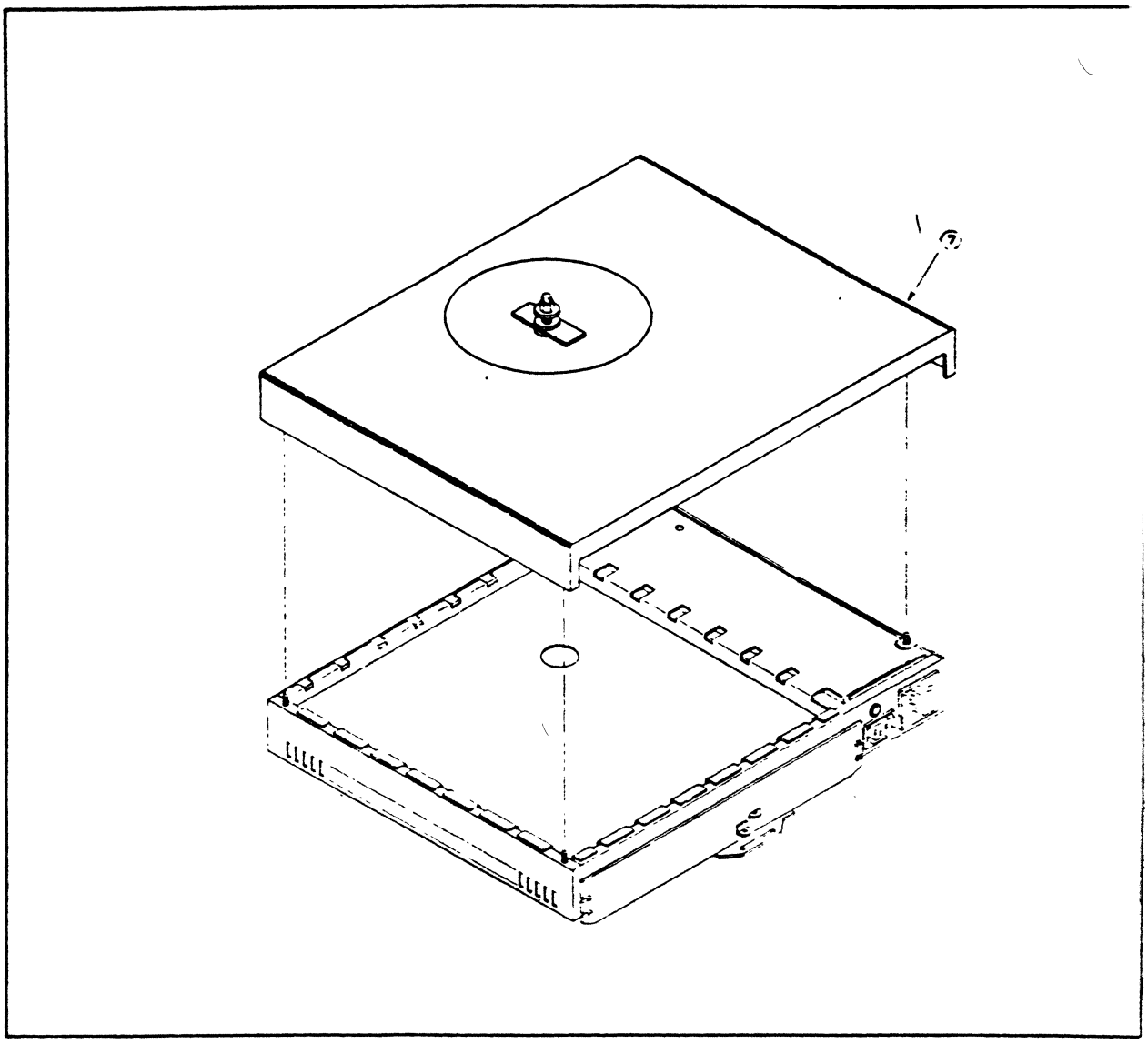
3.8. Miscellaneous Parts Removal

In addition to the assemblies described in the preceding paragraphs, there are a number of other field replaceable components in the Sun-2/50 SunStation. The removal of these components is straight- forward and will become apparent when viewing the illustrated parts breakdown in Figure 3-10a through 3-10i.



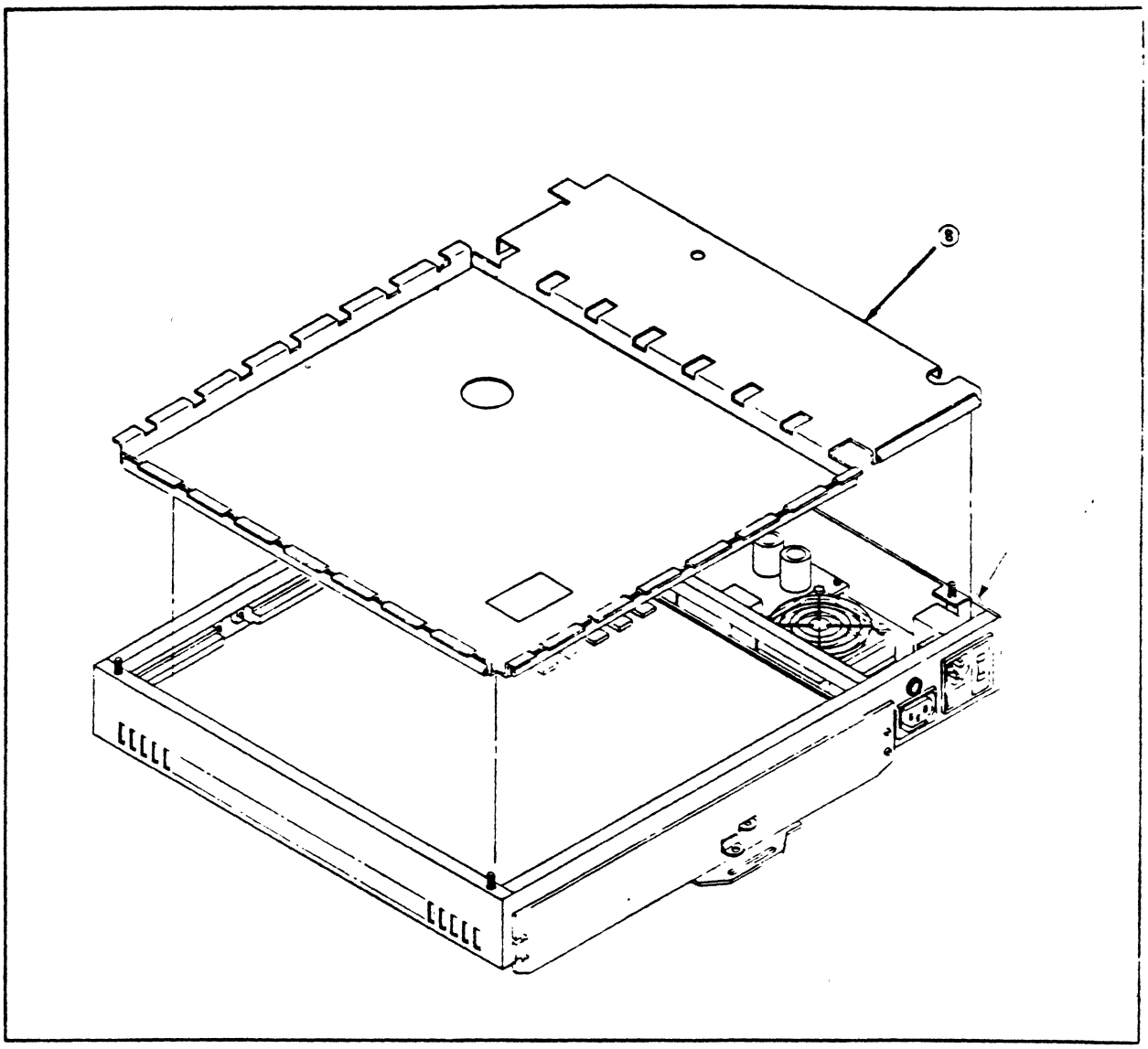
Reference	Description	Part Number
1	Monitor	540-1062-01
2	Keyboard	540-1006-01
3	Mouse	370-1025-01
4	Keyboard Cable	530-1068-01
5	Monitor Cable	530-1109-02
6	AC Power Cord	180-1010-01

Figure 3-10 *Sun-2/50 Illustrated Parts Breakdown*



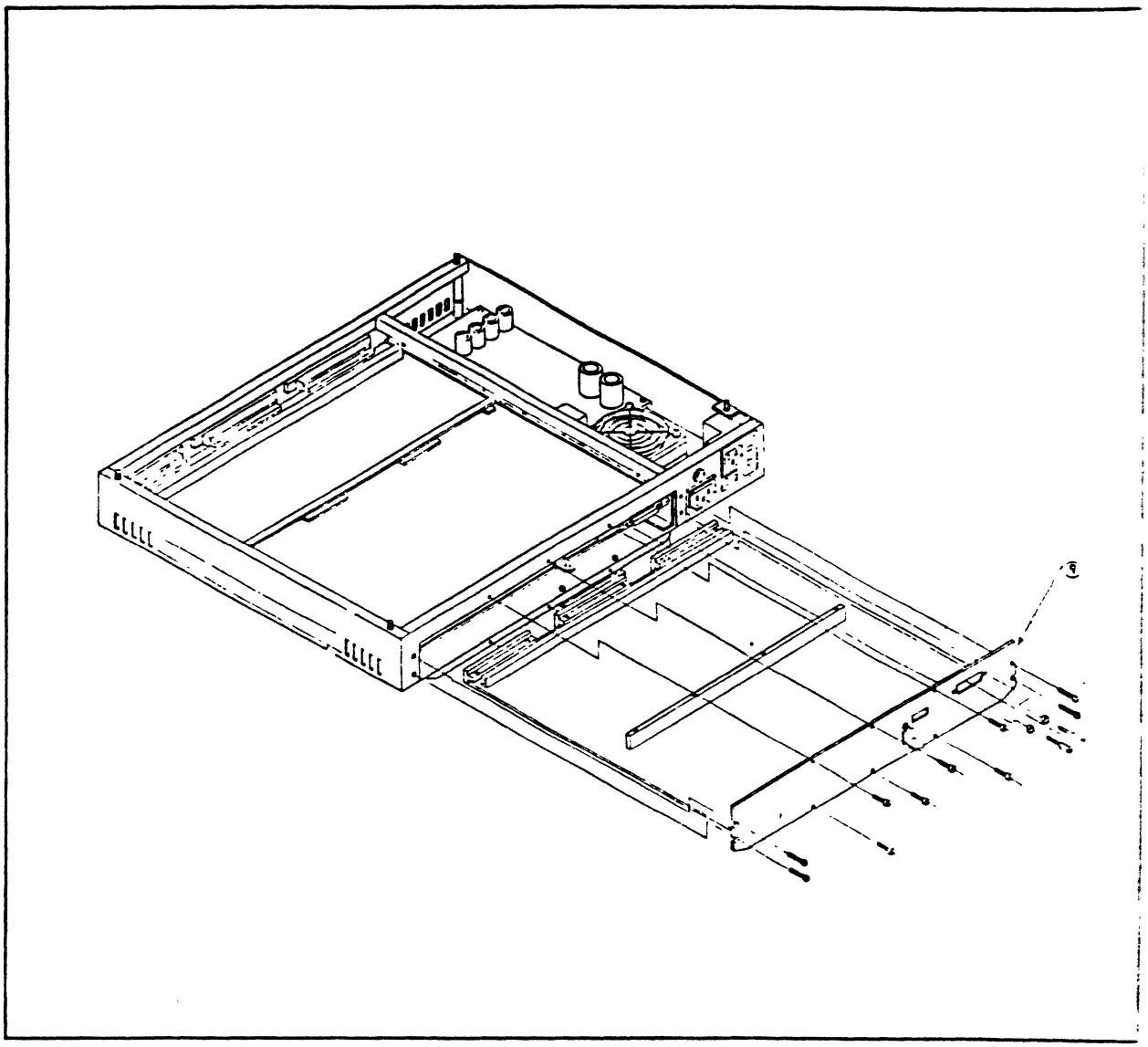
Reference	Description	Part Number
7	Chassis Cover	540-1100-01

Figure 3-11 *Sun-2/50 Illustrated Parts Breakdown*



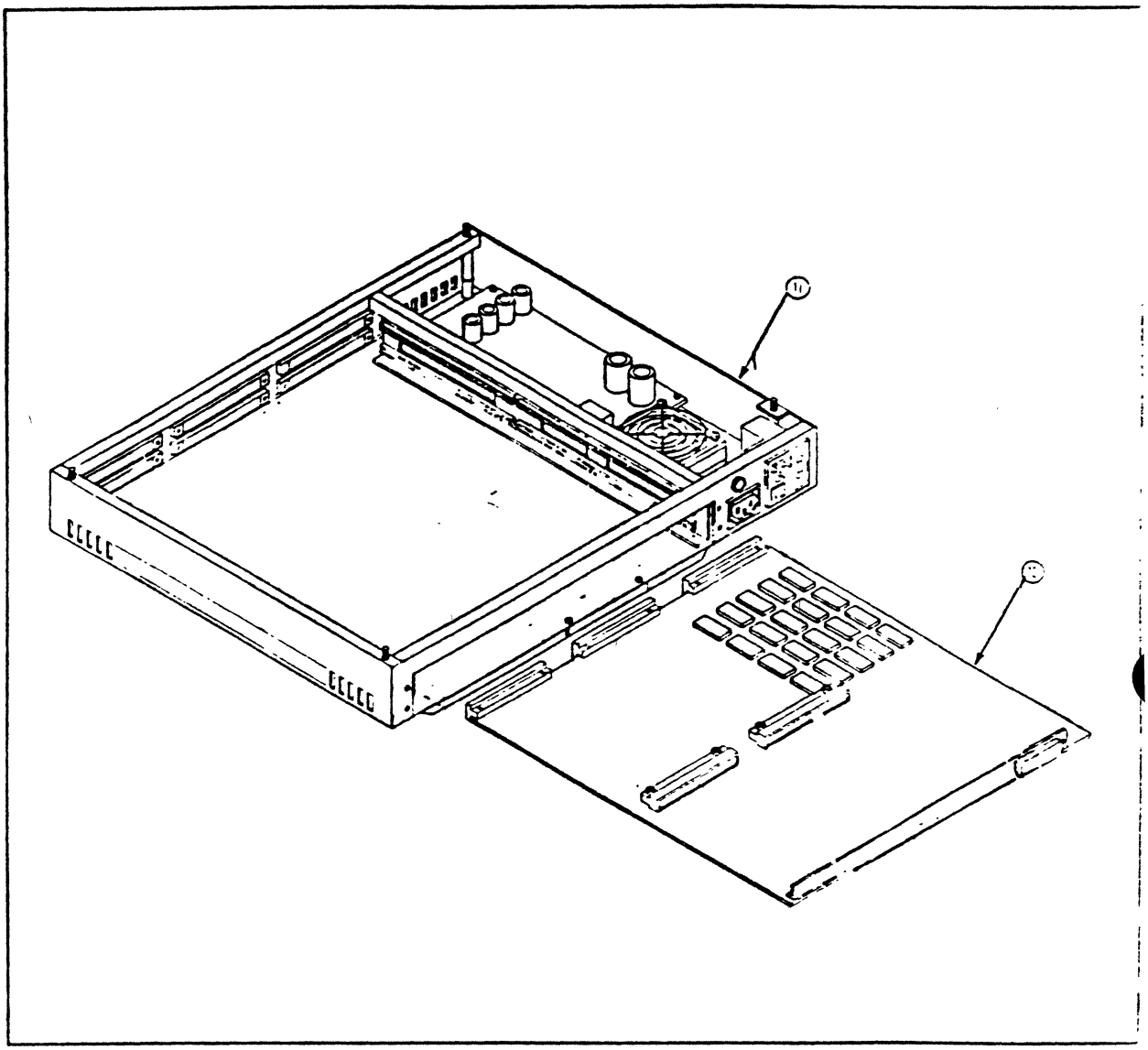
Reference	Description	Part Number
8	RFI Shield	540-1105-01

Figure 3-12 *Sun-2/50 Illustrated Parts Breakdown*



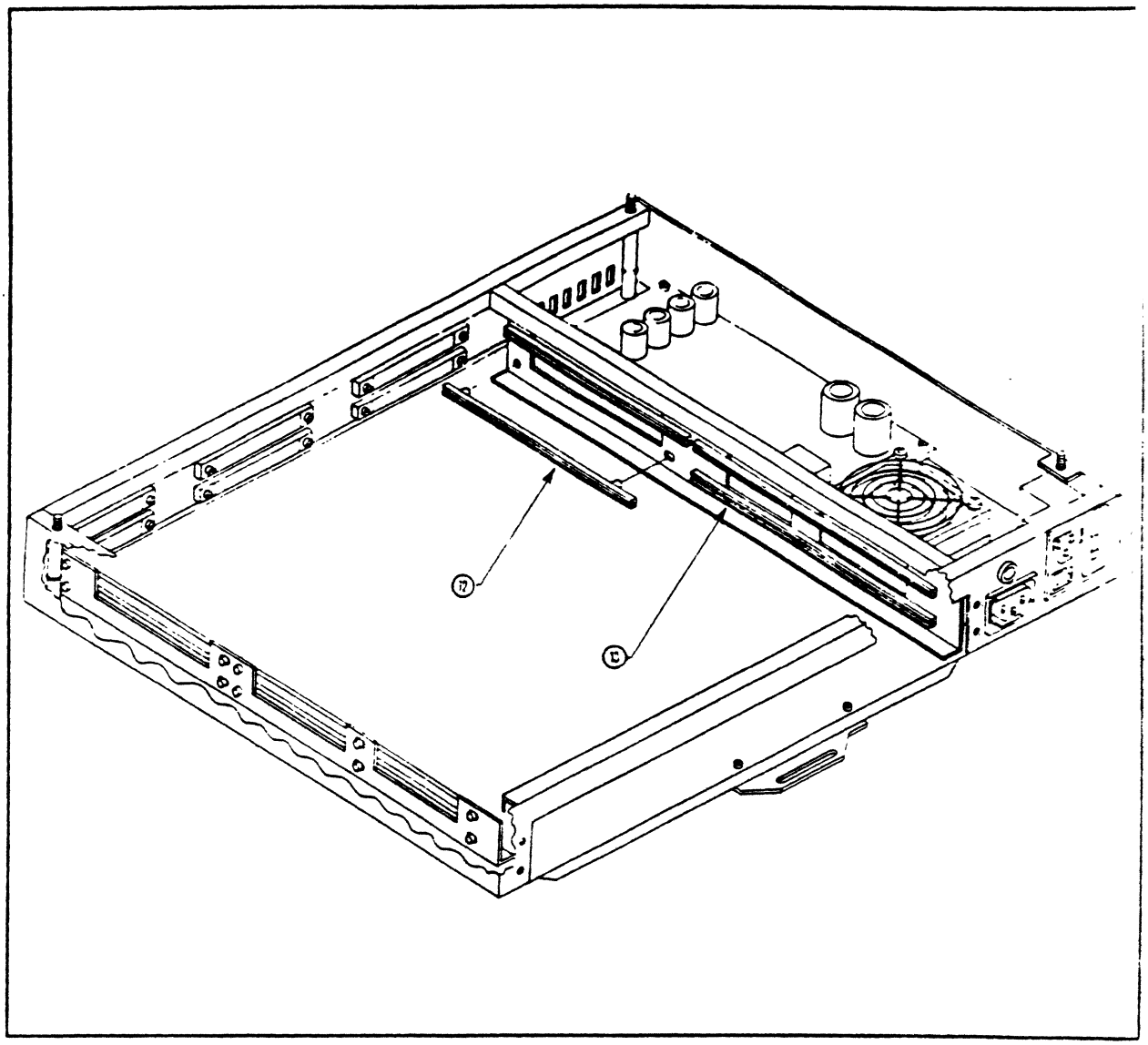
Reference	Description	Part Number
9	CPU Board-Rear Panel Assy.	540-1101-01

Figure 3-13 *Sun-2/50 Illustrated Parts Breakdown*



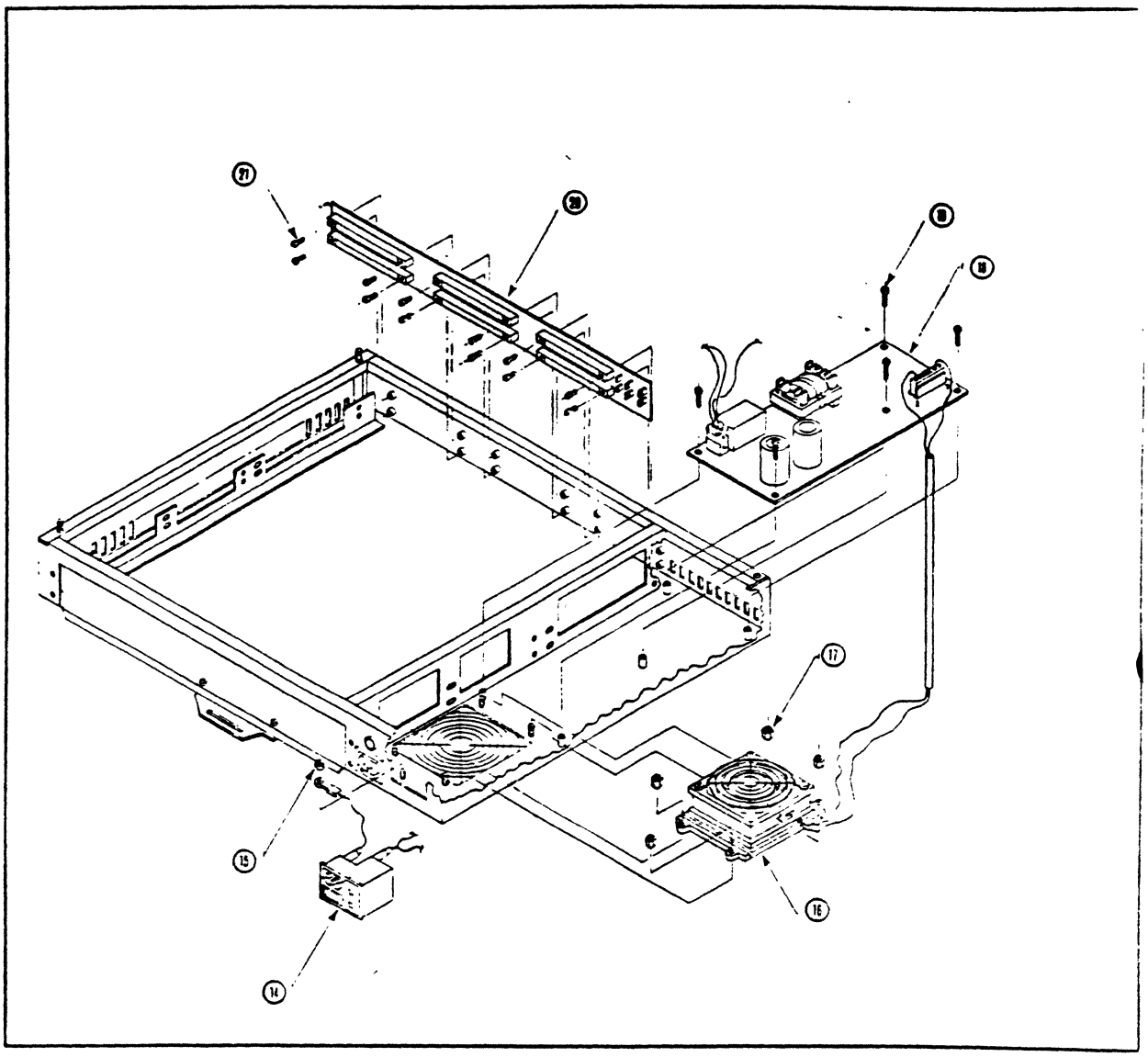
Reference	Description	Part Number
10	Memory Board (2MB)	501-1046-03
	Memory Board (3MB)	501-1067-01
	Memory Board (4MB)	501-1047-03
11	Chassis Assy.	540-1102-01

Figure 3-14 *Sun-2/50 Illustrated Parts Breakdown*



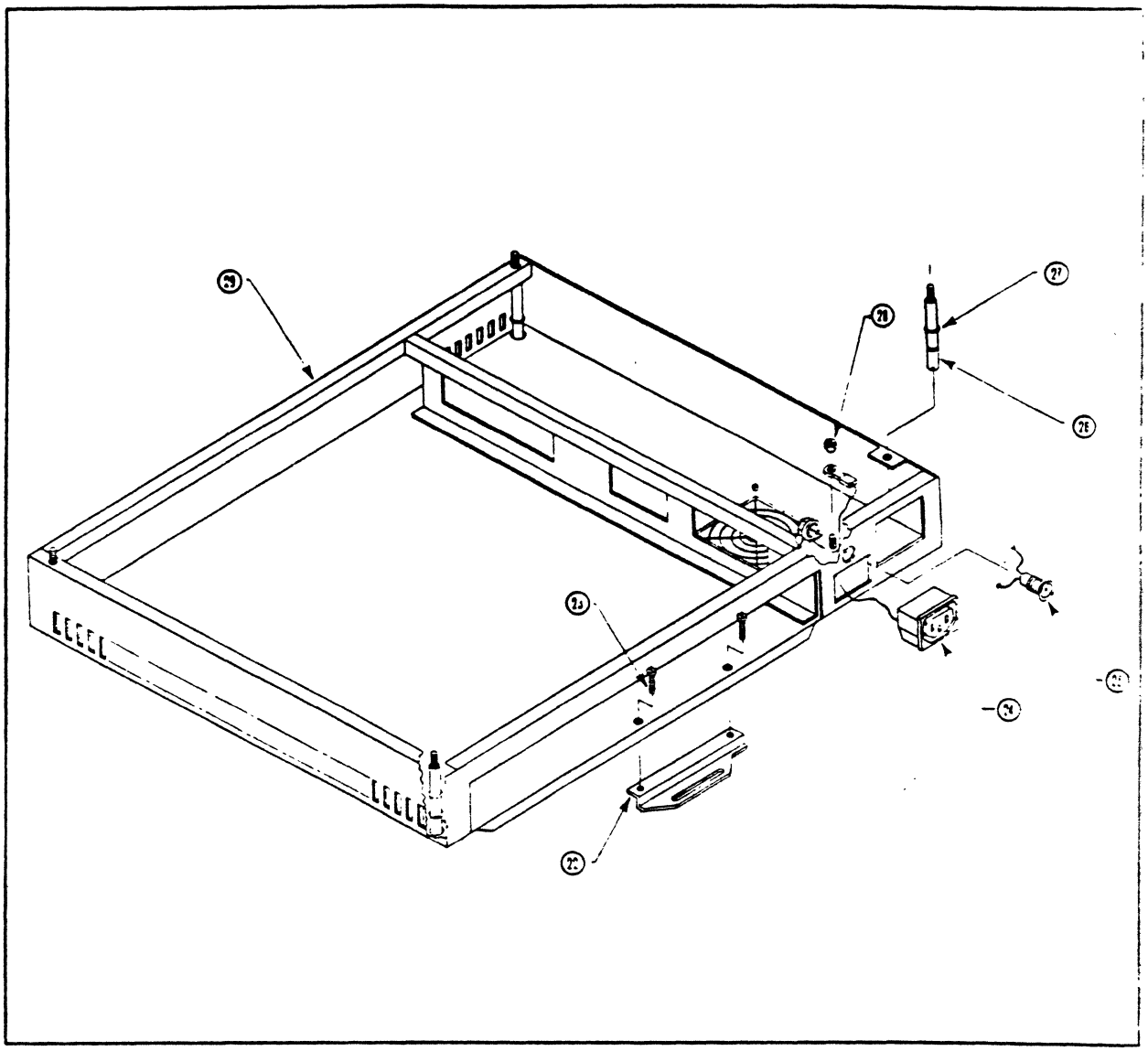
Reference	Description	Part Number
12	Card Guide (6")	230-1028-01
13	Card Guide (8.5")	230-1029-01

Figure 3-15 *Sun-2/50 Illustrated Parts Breakdown*



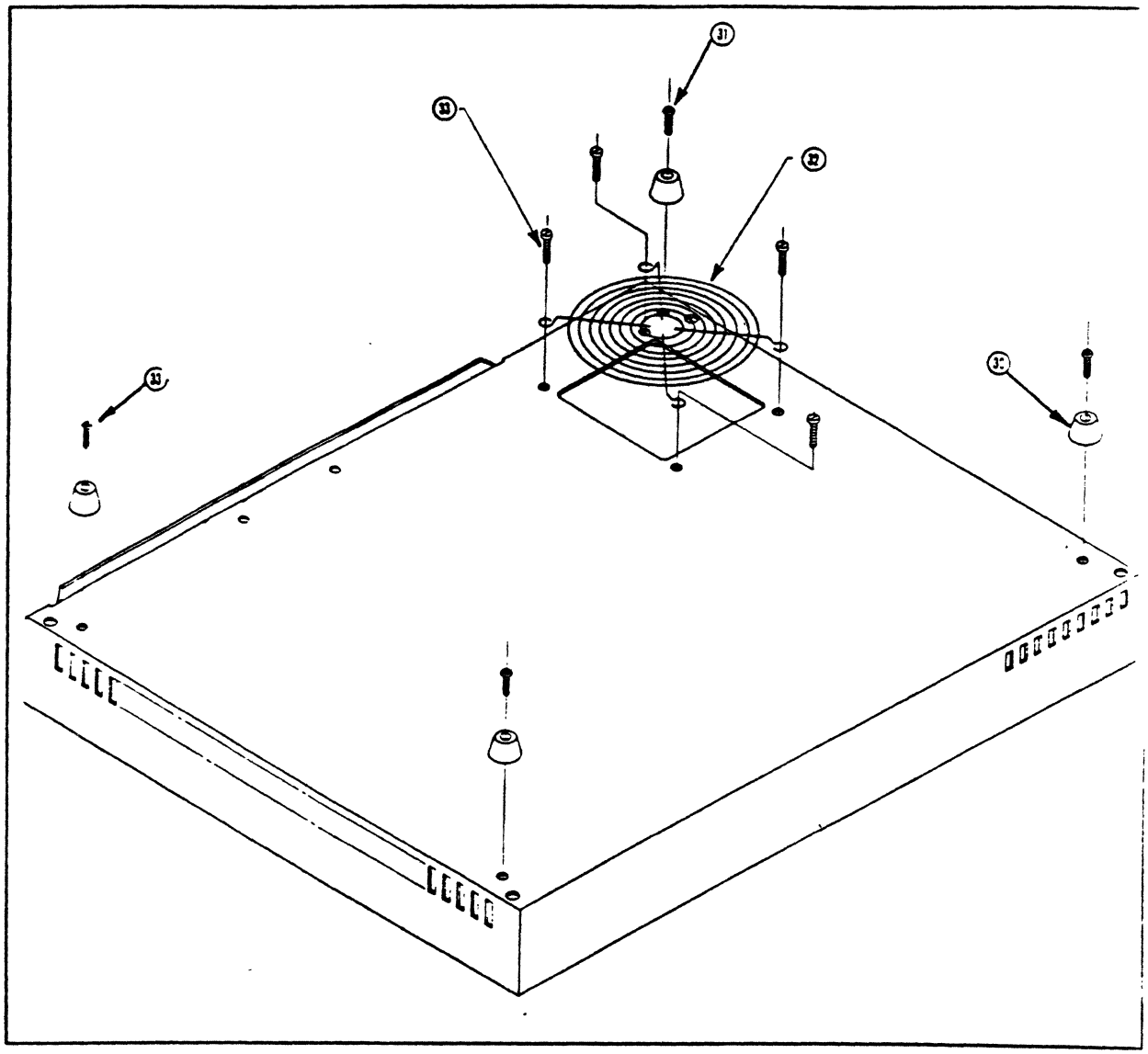
Reference	Description	Part Number
14	AC Switch-Fuse Assy.	530-1020-01
15	6-32 Kepnut (2)	240-0254
16	Fan Assy.	540-1068-02
17	Hex Standoff (4)	240-1219-01
18	Power Supply	300-1002-01
19	6-32" Crosshead Screw (5)	540-1158-01
20	Backplane	501-1042-01
21	Securing Screws (12)	240-1159-01

Figure 3-16 *Sun-2/50 Illustrated Parts Breakdown*



Reference	Description	Part Number
22	Fulcrum Bracket	340-1175-01
23	6-32 Screw (2)	240-1214-01
24	AC Cable Receptacle	540-1069-01
25	115V-230V Select Switch	540-1078-01
26	Chassis Cover Retaining Screw (4)	240-1024-02
27	O-Ring (4)	230-1033-01
28	6-32 Kepnut	240-0254
29	Chassis	340-1031-02

Figure 3-17 *Sun-2/50 Illustrated Parts Breakdown*

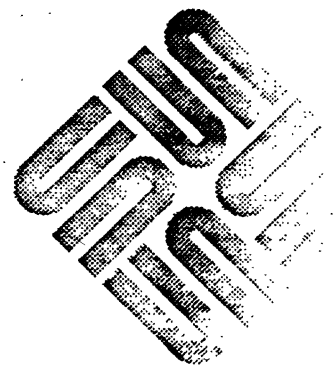


Reference	Description	Part Number
30	Rubber Bumper (4)	230-1025-01
31	6-32 Screw (4)	240-1158-01
32	Fingerguard	340-1178-01
33	6-32 Screw (4)	240-1202-01

Figure 3-18 *Sun-2/50 Illustrated Parts Breakdown*

A

Glossary of Sun Terms



A

Glossary of Sun Terms

The following definitions provide additional information about technical terms used elsewhere in this manual, and how those terms are defined in the context of Sun-2 architecture.

Accessed/Modified Bits -
statistical bits that are set whenever a page in memory is accessed or written to (modified). These bits will not be updated if the page number being accessed is invalid, if the protection code does not allow the attempted operation, or if a parity error in the previous cycle causes the current cycle to abort. The statistical bits are updated on all other cycles, including cycles which generate parity errors or terminate due to a timeout.

Carrier Sense Multiple Access with Collision Detection -
term for the link management procedure used by the Ethernet. This procedure allows the broadcast channel to be accessed by multiple stations, avoids contention via carrier sense and deference, and resolves contention by collision detection and retransmission.

Contexts -
arbitrary divisions in the MMU, corresponding to eight distinct address spaces. Separate context values are assigned to the supervisor and user, allowing each to address all eight contexts. The current context is selected via one of two 3-bit context registers. When the CPU issues a supervisor function code, the system context register provides the context value. When a user function code is issued, the user context register supplies the value. Refer to the definitions of supervisor and user states.

Copy Write -
an operation in which the contents of main memory are transferred to the video memory for transmission to the video monitor.

Direct Virtual Memory Access (DVMA) -
capability allowing any device designated as a VME bus master to directly access on-board memory using a virtual address. Data may be transferred between the Sun-2/50 and other devices on the VME bus without interrupting the current CPU cycle.

Function Code -
three bits (FC0-2), output from the 68010, which indicate the state (user or supervisor) and cycle type currently being executed. Function code outputs are defined as follows:

ID PROM -

provides basic information about the machine type and configuration via a unique serial number. The contents of the ID PROM are listed as follows:

Field	*Description*	*Size*
Format	the format of the ID PROM	1 byte
Machine type	specifies the implementation of the architecture.	1 byte
Ethernet address	unique 48-bit address assigned by Sun to this machine.	6 bytes
Date	the date the ID PROM was generated.	4 bytes
Serial number	a three byte serial number	3 bytes
Checksum	definition of checksum yield	1 byte
	Reserved for future expansion	16 bytes

Level Daisy Chain -

method of allowing any number of devices to receive signals (e.g. interrupts) of the same priority level and at the same time.

Memory Controller Cycles -

idle, processor update and video refresh. These cycles are performed during the sixteen state memory controller execution sequence. The idle cycle is executed between states 0 and 7 if no request is pending. Processor update cycles (read and write) are also executed between states 0 and 7 if the signal synchronous request (V.SREQ) is asserted and if the register select bit (V.BS19) is clear. Video refresh cycles are performed during the last eight states (8-15) of every memory controller execution sequence.

Page Map -

translates intermediate addresses, from the segment map, into physical addresses for memory. The page map contains 4096 page entries, with each entry mapping a 2K byte page. Page map entries are separated into 256 sections of 16 entries each. Pointers to individual sections are provided by the Page Map Entry Groups.

Page Map Entry Group (PMEG) -
a 32-bit word, generated by the MMU, which contains a physical address in memory as well as data defining that address. Refer to Figure 1-11.

Protection Field/Bits -
a 6-bit field used to control page access. The field may be configured to represent all 64 possible combinations of supervisor and user read-write-execute privilages.

Resets -
power-on, watchdog and 68010. Power-on reset (POR) is active for 100msec after the power supply reaches 4.5VDC. POR resets the 68010 and clears the system enable register, forcing a boot state.

Watchdog reset is generated as the result of a double bus fault (i.e. two bus errors in a row) and causes the 68010 to be reset.

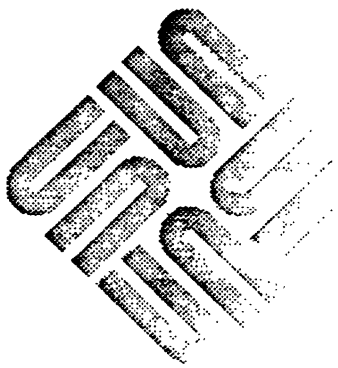
A 68010 reset, generated when the processor executes a reset instruction, resets all on- and off-board devices equipped with an external reset capability. This reset does not affect the 68010 or related logic, such as the system enable or diagnostic registers.

Segment Map -
translates virtual addresses, from the processor, into intermediate addresses for the page map. The segment map contains 4096 entries divided into eight equal sections, with one section per context. The 8-bit segment map entry is used to point to a page map entry group (PMEG).

Supervisor/User States -
are two states of privilage used by the MMU to control and translate memory accesses. The two privilage states are a system security mechanism which allow most programs to execute in the user state, but limits their access to their own code and data areas. The operating system executes in the supervisor state and so has access to all memory resources.

B

Printed Circuit Board Layouts

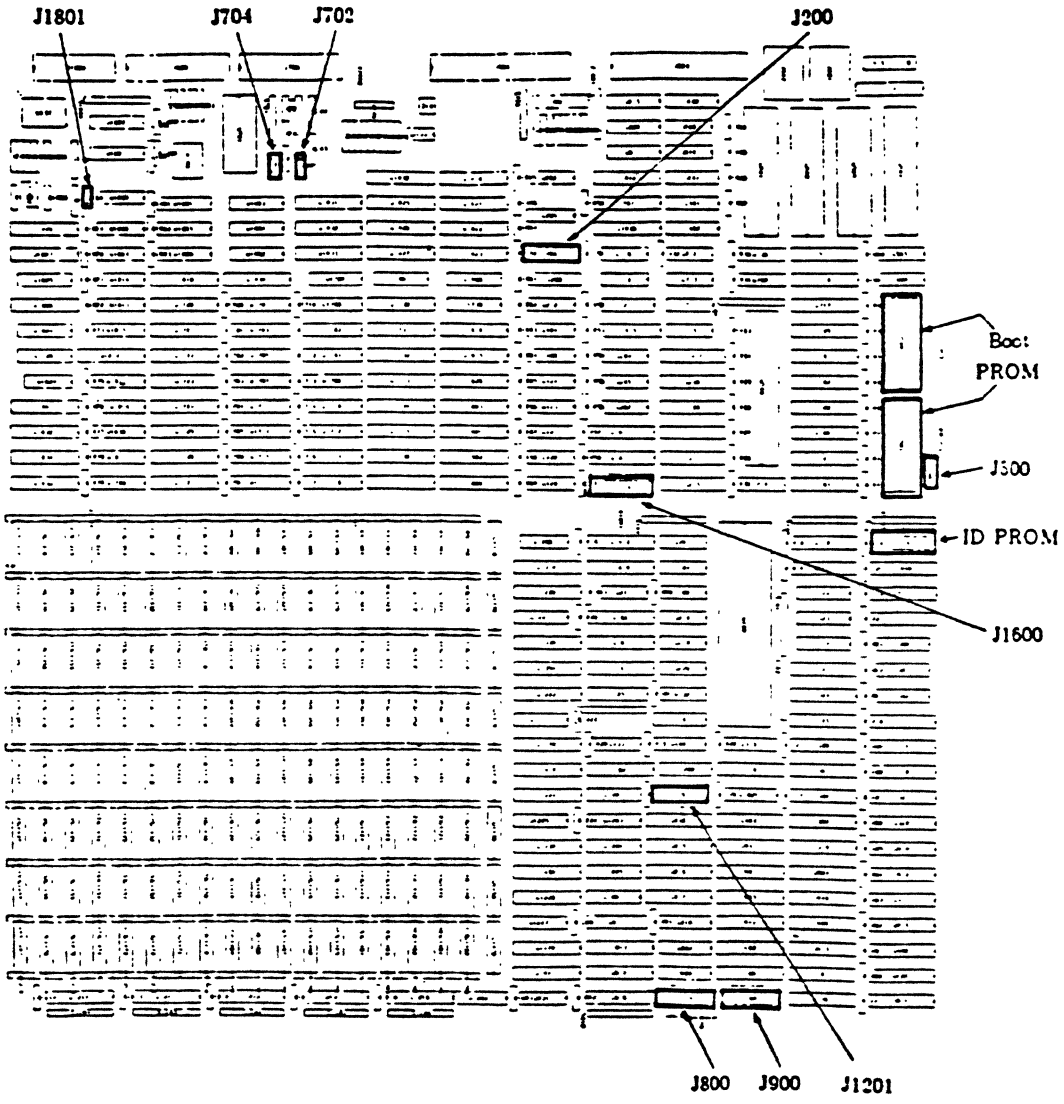


B

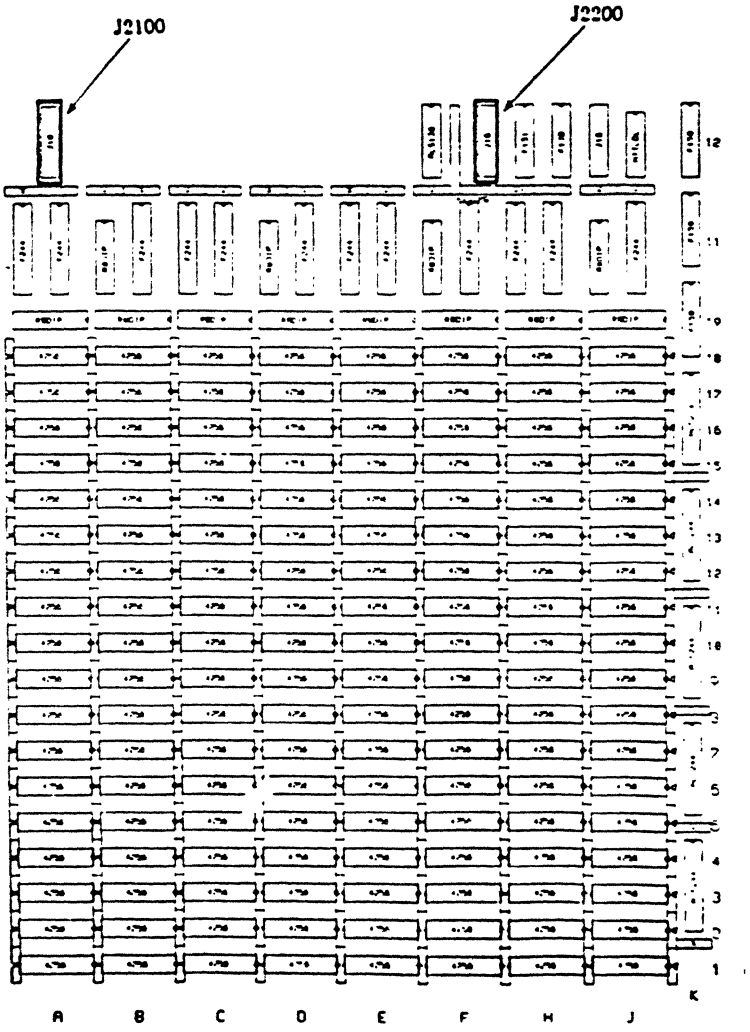
Printed Circuit Board Layouts

This appendix provides the board locations of select jumpers and devices referenced in the text.

CPU Board


J1801
J704
J702
J200
Boot PROM
J300
ID PROM
J1600
J800
J900
J1201

Memory Expansion Boards (2MB,3MB,4MB)



C

Printed Circuit Board Connector Pinouts

C

Printed Circuit Board Connector Pinouts

This appendix provides pinouts for all connectors on the CPU board.

J603: Serial Port A

PIN	SIGNAL	PIN	SIGNAL
1	----	14	----
2	TXDA[]	15	DBA[]
3	RXDA[]	16	----
4	RTSA[]	17	DDA[]
5	CTSA[]	18	----
6	DSRA[]	19	----
7	GND	20	DTRA[]
8	DCDA[]	21	----
9	----	22	----
10	----	23	----
11	----	24	DAA[]
12	----	25	VEE
13	----	--	----

J604: Serial Port B

PIN	SIGNAL	PIN	SIGNAL
1	----	14	----
2	TXDB[]	15	DBB[]
3	RXDB[]	16	----
4	RTSB[]	17	DDB[]
5	CTSB[]	18	----
6	DSRB[]	19	----
7	GND	20	DTRB[]
8	DCDB[]	21	----
9	----	22	----
10	----	23	----
11	----	24	DAB[]
12	----	25	VEE
13	----	--	----

J605: Keyboard/Mouse

PIN	SIGNAL	PIN	SIGNAL
1	RXD0[]	9	GND
2	GND	10	VCC
3	TXD0[]	11	VCC
4	GND	12	VCC
5	RXD1[]	13	----
6	GND	14	VCC
7	TXD1[]	15	VCC
8	GND	--	----

J700: Ethernet

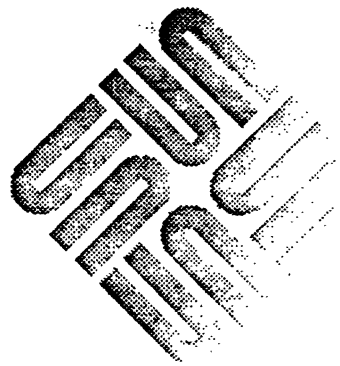
PIN	SIGNAL	PIN	SIGNAL
1	----	9	E.COL-
2	E.COL+	10	E.TXD-
3	E.TXD+	11	----
4	----	12	E.RXD-
5	E.RXD+	13	+12V
6	GND	14	----
7	VCC	15	----
8	----	--	----

J1800: Video

PIN	SIGNAL	PIN	SIGNAL
1	VIDEO+	6	VIDEO-
2	----	7	GND
3	HSYNC	8	GND
4	VSYNC	9	GND
5	----	-	----

D

Select Jumper Options



D

Select Jumper Options

This appendix provides information supporting all possible jumper options on both the CPU and Expansion Memory boards.

CPU Board Permanent Jumpers

The following jumpers are factory installed and are normally not modified. The factory configuration is indicated by an asterisk (*).

LABEL	PINS	DESCRIPTION IN/OUT
*J200	1-2	Enable/Disable UART Clock
*J200	3-4	10/12 MHZ CPU operation
J200	5-6	12/10 MHZ CPU operation
J200	7-8	Reserved
J200	9-10	Reserved
*J200	11-12	Enable/Disable Ethernet Clock
*J200	13-14	Enable/Disable Memory Refresh
*J200	15-16	Enable/Disable Timeouts
J500	1-2	PROM TYPE = 27128
*J500	3-4	PROM TYPE = 27256 or 27512
*J500	5-6	PROM TYPE = 27128 or 27128
J500	7-8	PROM TYPE = 27512
J1201	1-2	Enable/Disable 2nd megabyte (256K RAM)
J1201	3-4	Enable/Disable 3/4 megabyte (256K RAM)
*J1201	5-6	64K/256K RAMs
J1201	7-8	256K/64K RAMs
*J1201	9-10	64K/256K RAMs
J1201	11-12	256K/64K RAMs
*J1201	13-14	64K/256K RAMs
J1201	15-16	256K/64K RAMs
J1600	9-10	Reserved
J1600	11-12	Reserved
*J1600	13-14	10/12 MHZ CPU operation
J1600	15-16	12/10 MHZ CPU operation
*J1801	1-2	Enable/Disable 100 MHZ Video Clock

The jumper positions for different PROM sizes are summarized in the table below.

PROM	JUMPER	JUMPERED PINS
27128	J600	1-2 and 5-6
27256	J600	3-4 and 5-6
27512	J600	3-4 and 7-8

CPU Board Configuration Jumpers

The asterisk (*) indicates the factory-installed configuration.

LABEL	PINS	DESCRIPTION IN/OUT
*J702	1-2	Enable/Disable 5 Volt to Ethernet
*J704	1-2	Level 2/Level 1 Ethernet Transceiver
*J800	1-2	Enable/Disable VME Interrupt Level 1
*J800	3-4	Enable/Disable VME Interrupt Level 2
*J800	5-6	Enable/Disable VME Interrupt Level 3
*J800	7-8	Enable/Disable VME Interrupt Level 4
*J800	9-10	Enable/Disable VME Interrupt Level 5
*J800	11-12	Enable/Disable VME Interrupt Level 6
*J800	13-14	Enable/Disable VME Interrupt Level 7
*J900	1-2	DVMA Address Comparator A20=0/1
*J900	3-4	DVMA Address Comparator A21=0/1
*J900	5-6	DVMA Address Comparator A22=0/1
*J900	7-8	DVMA Address Comparator A23=0/1
*J900	9-10	Enable/Disable VME Arbiter
*J900	11-12	Enable/Disable VME Reset Master
J900	13-14	Enable/Disable VME Reset Slave
*J900	15-16	Enable/Disable VME System Clock
*J1600	1-2	Video Register Sense Bit 0
*J1600	3-4	Video Register Sense Bit 1
*J1600	5-6	Video Register Sense Bit 2
*J1600	7-8	Video Register Sense Bit 3

Memory Board Permanent Jumpers (2MB, 3MB, 4MB)

The memory expansion board(s) has select jumpers which correspond to various amounts of memory (2MB, 3MB, 4MB). For a 1MB base board, the jumpers are configured as follows:

SIZE	JUMPER	JUMPERED PINS
1 MB	J2200	3-4
1 MB	J2201	5-6, 9-10, 13-14
2 MB	J2200	3-4, 5-6
2 MB	J2201	3-4, 7-8, 11-12
3 MB	J2200	3-4, 5-6, 7-8
3 MB	J2201	7-8, 11-12, 15-16
4 MB	J2200	3-4, 5-6, 7-8, 9-10
4 MB	J2201	7-8, 11-12, 15-16

The select jumper at J2100 allows VME bus grant lines to be daisy-chained, as well as the VME bus interrupt acknowledge lines. This jumper is configured as follows:

JUMPER	PINS	FUNCTION
J2100	1-2	BUS GRANT 0
J2100	3-4	BUS GRANT 1
J2100	5-6	BUS GRANT 2
J2100	7-8	BUS GRANT 3
J2100	15-16	IACK CHAIN

E

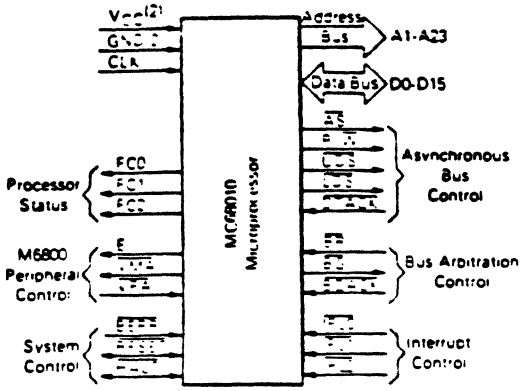
Manufacturer's Component Data

E

Manufacturer's Component Data

This appendix supplies information about selected chips used in Sun-2 architecture.

Motorola 68010 Microprocessor



Signal Name	Mnemonic	Input/Output	Active State	H-Z	
				On HALT	On BGACK
Address Bus	A1-A23	Output	High	Yes	Yes
Data Bus	D0-D15	Input/Output	High	Yes	Yes
Address Strobe	AS	Output	Low	No	Yes
Read/Write	R/W	Output	Read=High Write=Low	No	Yes
Upper and Lower Data Strobes	UDS, LDS	Output	Low	No	Yes
Data Transfer Acknowledge	DTACK	Input	Low	–	–
Bus Request	BR	Input	Low	–	–
Bus Grant	BG	Output	Low	No	No
Bus Grant Acknowledge	BGACK	Input	Low	–	–
Interrupt Priority Level	IPL0, IPL1, IPL2	Input	Low	–	–
Bus Error	BERR	Input	Low	–	–
Reset	RESET	Input/Output	Low	No*	No*
Halt	HALT	Input/Output	Low	No*	No*
Enable	E	Output	High	No	No
Valid Memory Address	VMA	Output	Low	No	Yes
Valid Peripheral Address	VPA	Input	Low	–	–
Function Code Output	FC0, FC1, FC2	Output	High	No	Yes
Clock	CLK	Input	High	–	–
Power Input	VCC	Input	–	–	–
Ground	GND	Input	–	–	–

*Open Drain

Z8530 Serial Communications Controller

Features

- Two independent, 0 to 1M bit/second, full-duplex channels, each with a separate crystal oscillator, baud rate generator, and Digital Phase-Locked Loop for clock recovery.
- Multi-protocol operation under program control: programmable for NRZ, NRZI, or FM data encoding.
- Asynchronous mode with five to eight bits and one, one and one-half, or two stop bits per character; programmable clock factor; break detection and generation; parity, overrun, and framing error detection.
- Synchronous mode with internal or external character synchronization on one or two synchronous characters and CRC generation and checking with CRC-16 or CRC-CCITT preset to either 1s or 0s.
- SDLC/HDLC mode with comprehensive frame-level control, automatic zero insertion and deletion, I-field residue handling, abort generation and detection, CRC generation and checking, and SDLC Loop mode operation.
- Local Loopback and Auto Echo modes.

General Description

The Z8530 SCC Serial Communications Controller is a dual-channel, multi protocol data communications peripheral designed for use with conventional non-multiplexed buses. The SCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The SCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, Digital Phase-Locked Loops, and crystal oscillators that dramatically reduce the need for external logic.

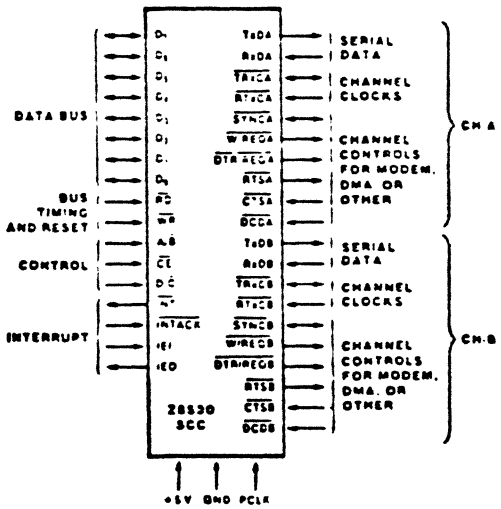


Figure 1. Pin Functions

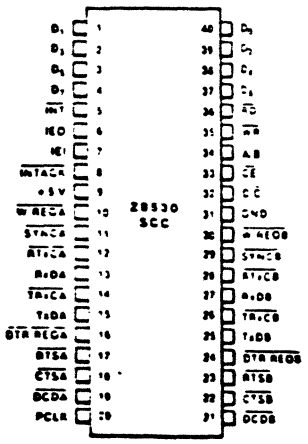


Figure 2. Pin Assignments

AM78073 System Timing Controller

DISTINCTIVE CHARACTERISTICS

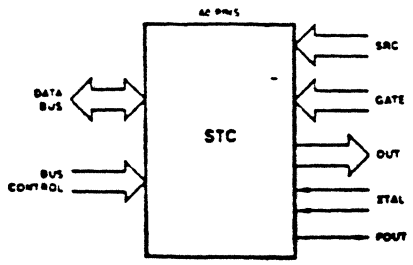
- Five independent 16-bit counters
- High speed counting rates
- Up/down and binary/BCD counting
- Internal oscillator frequency source
- Tapped frequency scaler
- Programmable frequency output
- 8-bit or 16-bit bus interface
- Time-of-day option
- Alarm comparators on counters 1 and 2
- Complex duty cycle outputs
- One-shot or continuous outputs
- Programmable count/gate source selection
- Programmable input and output polarities
- Programmable gating functions
- Retriggering capability
- +5 volt power supply
- Standard 40-pin package
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

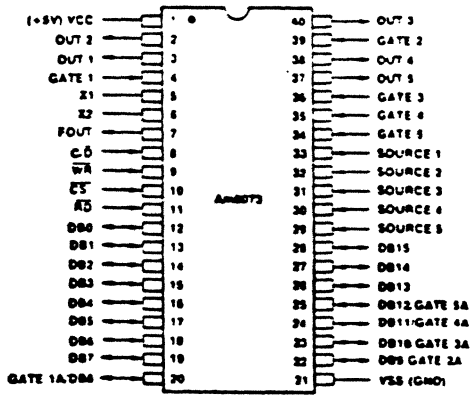
The AmZ8073 System Timing Controller is an LSI circuit designed to service many types of counting, sequencing and timing applications. It provides the capability for programmable frequency synthesis, high resolution programmable duty cycle waveforms, retriggerable digital one-shots, time-of-day clocking, coincidence alarms, complex pulse generation, high resolution baud rate generation, frequency shift keying, stop-watching, timing event count accumulation, waveform analysis and many more. A variety of programmable operating modes and control features allow the AmZ8073 to be personalized for particular applications as well as dynamically reconfigured under program control.

The STC includes five general-purpose 16-bit counters. A variety of internal frequency sources and external pins may be selected as inputs for individual counters with software selectable active high or active-low input polarity. Both hardware and software gating of each counter is available. Three-state outputs for each counter provide pulses or levels and can be active-high or active-low. The counters can be programmed to count up or down in either binary or BCD. The host processor may read an accumulated count at any time without disturbing the counting process. Any of the counters may be internally concatenated to form any effective counter length up to 80 bits.

INTERFACE FLOW

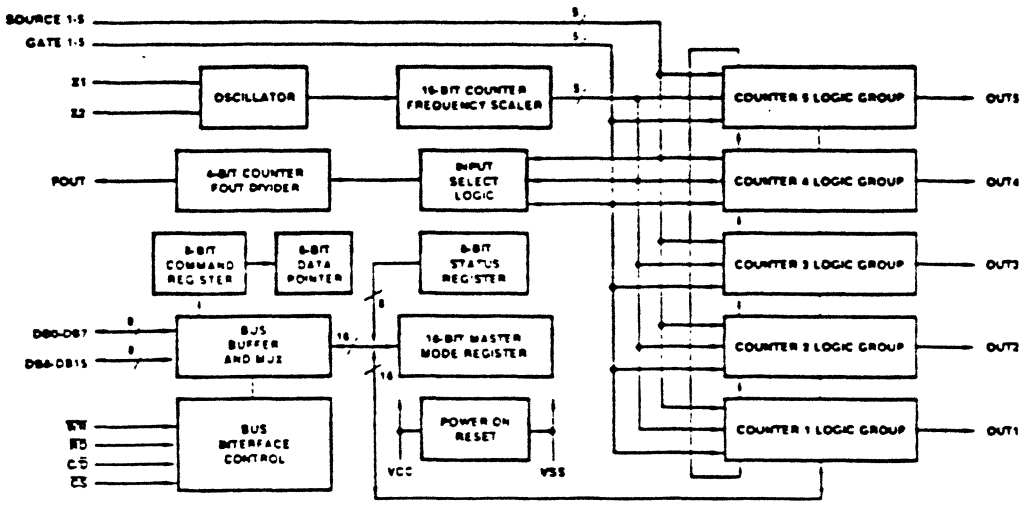


CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

FUNCTIONAL BLOCK DIAGRAM



82586 Local Area Network Coprocessor

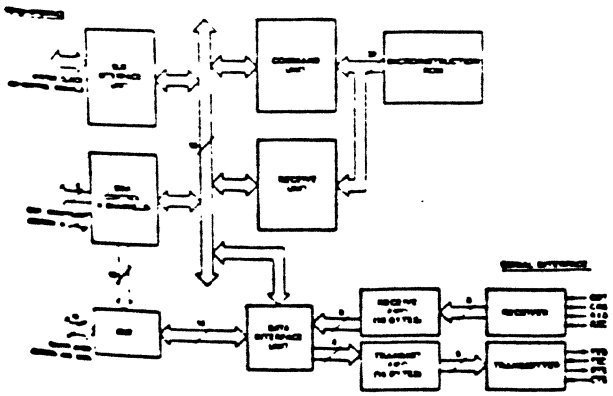
Fully implements the IEEE 802.3/Ethernet Data Link specifications without CPU overhead.

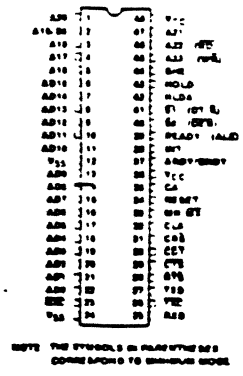
Bus interface optimized to iAPX 186 and 188 microprocessors.

On-chip DMA channels provide automatic memory management.

Independent parallel bus and serial line clocks.

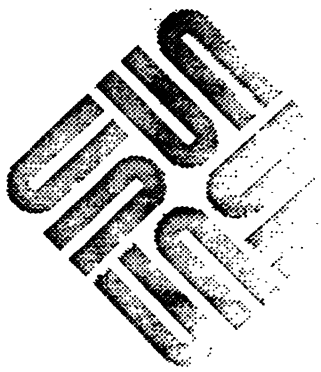
- Network diagnostics:
  - Frame CRC errors
  - Frame alignment errors
  - Location of cable opens/shorts
  - Collision tallies
- Self test diagnostics
  - Loop back
  - Register Dump
  - Backoff timer check
- Efficient use of memory via buffer chaining.
- User configurable to realize broadband, short topology and 1 Mbps networks.





F

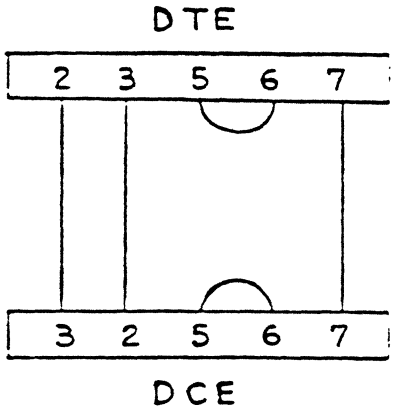
RS-423 P-Diag Jumper Pinout



F

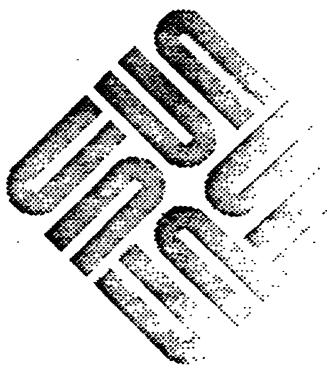
RS-423 P-Diag Jumper Pinout

Below is a pinout of the RS-232 compatible PROM-diagnostics jumper.



G

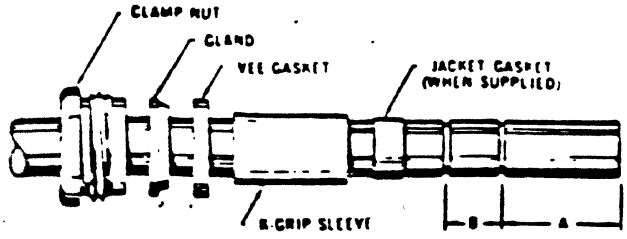
Ethernet Cable Connections



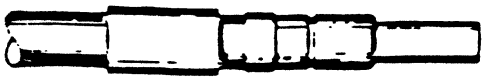
G

Ethernet Cable Connections

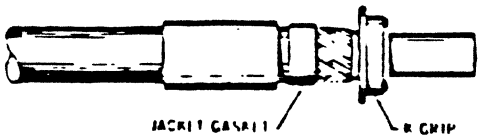
This appendix provides the information necessary to make Ethernet cable connections.



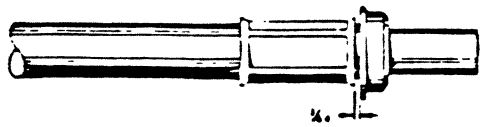
1. Cut cable end square slide K-GRIP sleeve and back end parts over jacket Using jacket trim jig make cuts A and B in jacket



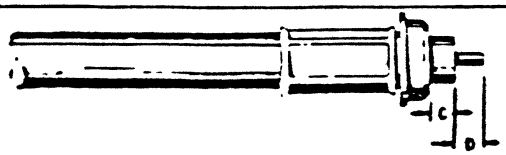
2. Remove jacket to dimension "A" Flare or bulge back braid Trim with scissors at edge of jacket



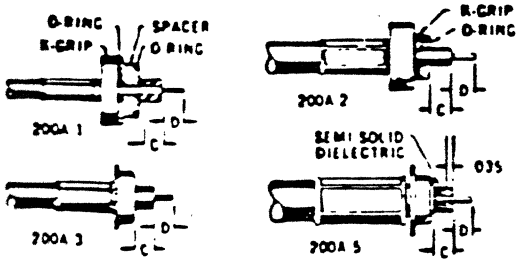
3. Remove jacket to dimension "B" Push K-GRIP over dielectric and under braid Slide jacket gasket when provided forward to position flush with jacket edge (When the "B" dimension in the trim code is 0 push the K-GRIP under both braid and jacket butting braid against flange of K-GRIP Teflon jackets may be slit axially ¼" in the two places to facilitate entry of the K-GRIP)



4. Slide K-GRIP sleeve against flange on K-GRIP. Form hex.

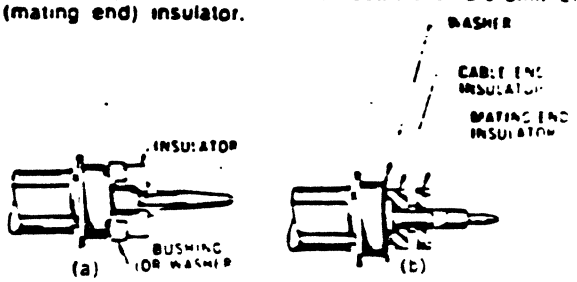


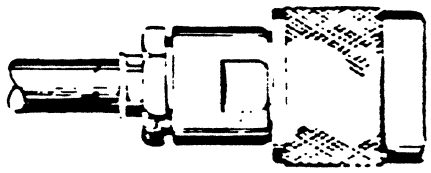
5. With dielectric trim jig trim dielectric to dimension "C." Cut center conductor to dimension "D." Assemble internal O-ring seals and spacer, when provided, as shown below When cable positioning insulators are used adjust trim code dimensions as shown below, and assemble as indicated



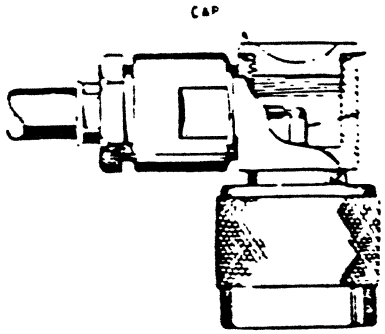
6. Solder or crimp contact to center conductor For access type angle connectors, omit this step and proceed to step 7.

For captive contacts: (a) assemble bushing and insulator Attach contact or (b) assemble washer and larger (cable end) insulator Attach contact. Assemble smaller (mating end) insulator.





7. Thread assembly into connector and [illegible] Vee gasket must be split by braid clamp



8. For access type angle connectors, solder center conductor in contact groove Close access opening

TRIM CODE CHART

CODE	A	B	C	D
201A	½	3/32	.110	7/64
202A	9/16	3/32	.130	9/64
205A	39/64	3/32	.212	7/64
207A	9/16	3/32	.118	9/64
211A	35/64	3/32	.045	7/64
213A	21/32	3/32	.041	7/64
220A	61/64	3/32	.470	1/8
221A	33/64	3/32	.371	5/64
223A	17/32	3/32	.096	5/64
230A	33/32	3/32	.043	1/16
233A	49/64	3/16	.233	13/64
234A	19/32	3/16	.187	1/8

H

MUX Box Specification

H

MUX Box Specification

This appendix supplies information on the installation and operation of the 2110 Multiport Transceiver (MUX box). The MUX box is used to expand the number of stations per transceiver in an Ethernet local area network. A single 2110 MUX box can operate an independent network of up to eight stations. Nine MUX boxes may be cascaded to create a 64-station network, which can operate either independently or connected to the Ethernet (via a TCL Model 2010E series transceiver, see Appendix I)

H.1. Installation Requirements

- 115V, 60Hz power supply
- Appropriate transceiver cables (refer to MUX box specifications).
- TCL Model 2110E series transceiver (if MUX box is to be connected to an Ethernet cable).
- TCL Model 2110-A1 mininet adapter (if MUX box is to be operated as an independent network).
- Sufficient airspace surrounding the MUX box to allow for adequate ventilation.

H.2. MUX Box (2110) Installation

1. Refer to Figure H-1 for acceptable network configurations. Note that MUX boxes whose 2110-A0 modules are connected to a 2110-B0 module of another MUX box can only have stations connected to their 2110-B0 modules. Multiport transceivers whose 2110-A0 module is connected to either a 2110-A1 mininet adapter or to a 2010E series transceiver may have either stations or a MUX box connected to its 2110-B0 module.

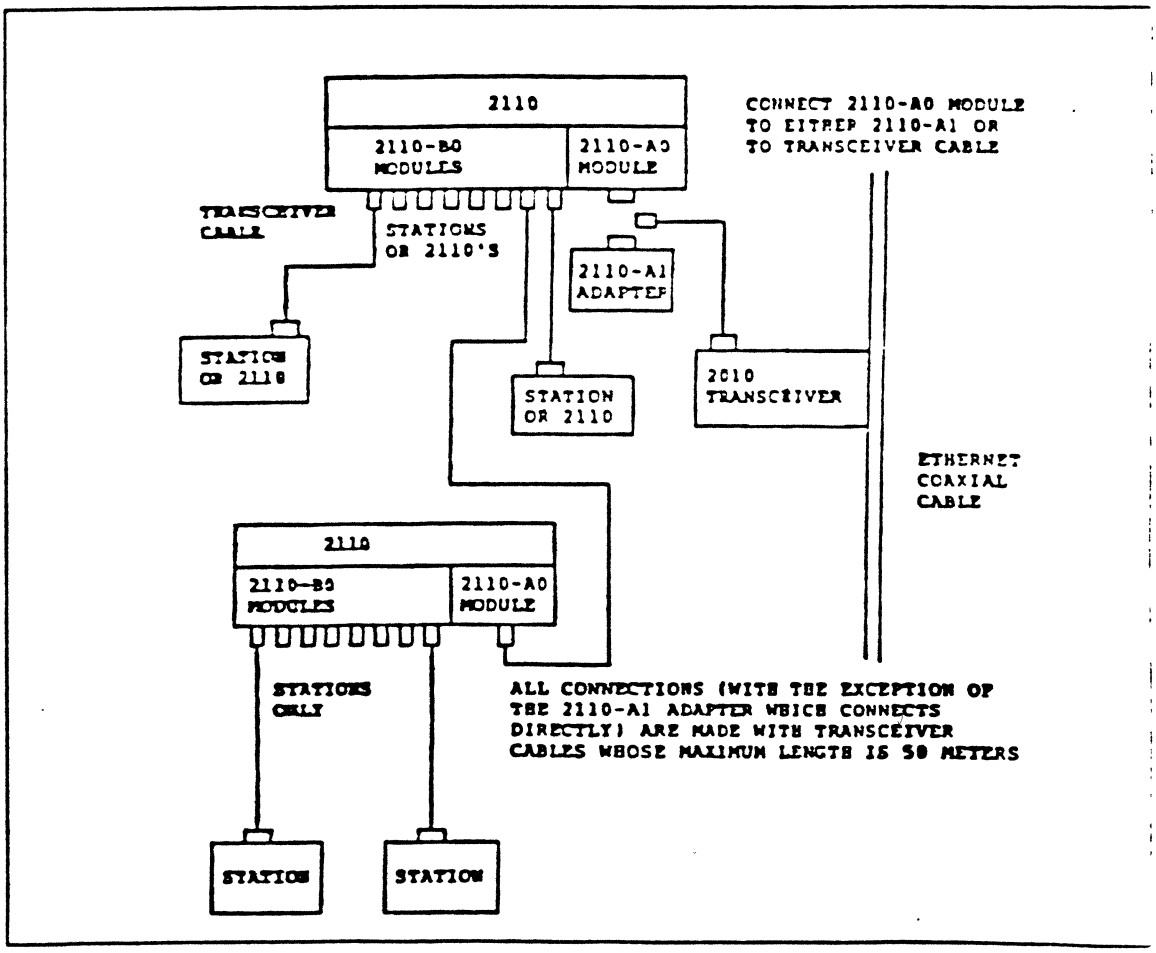


Figure H-1 *Network Configurations*

2. Use transceiver cables to connect the stations, multiport transceivers and series transceivers as required. Transceiver cable length must not exceed 50 meters. If the installation is an independent network, connect the mininet

adapter directly to the 2110-A0 module.

3. Apply power. Note that the transceiver cables may be installed and removed with power applied to the MUX box.

H.3. 2110-B0 Module Installation

1. Remove the blank face plate (2110-D0) by unfastening the screws at the top and bottom of the panel.

2. Insert the 2110-B0 module in the multiport transceiver chassis with the screws removed in step 1.

3. Blank face plates (2110-D0) should be installed over all unused module slots to ensure compliance with the FCC regulations governing radio frequency interference.

H.4. 2110-A0/2110-B0 Module Operation

When power is applied, the LED in the 2110-A0 module will light, indicating that the unit is operating correctly. If the LED fails to light, first check the fuse and then verify that the correct voltage is present. If these checks fail to uncover the problem, the module is faulty.

An unlit LED on the 2110-B0 module indicates one of the following conditions

- the module is not connected to a station
- the station the module is connected to is in continuous transmission mode
- station power is turned off

H.5. Specifications

Function	2110/ 2110-A0	Nominal DC Offset	Signal Range	Load Resistance
Output	Transmit+	+4V	+/-0.6 to +/-0.9V	78ohm
	Transmit-	+4V	+/-0.6 to +/-0.9V	78ohm
Input	Receive+	+/-10V*	+/-0.5 to +/-1.0V	78ohm
	Receive-	+/-10V*	+/-0.5 to +/-1.0V	78ohm
Input	Collision+	+/-10V*	+/-0.5 to +/-1.0V	78ohm
	Collision-	+/-10V*	+/-0.5 to +/-1.0V	78ohm

Connector: 15-pin D-subminiture female with slide lock Power: 100-130V, 60Hz, 27VA Size: 15.5"W x 8.5"H x 8.0"D Weight: 13.5lbs LED: No light indicates no power.

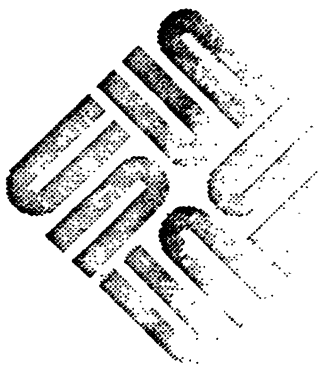
Function	2110-B0/ DC Offset	Nominal Range	Signal Resistance	Load
Input	Transmit+	+10V*	+/-0.5 to +/-1.0V	78ohm
	Transmit-	+10V*	+/-0.5 to +/-1.0V	78ohm
Output	Receive+	+/-4V	+/-0.6 to +/-0.9V	78ohm
	Receive-	+/-4V	+/-0.6 to +/-0.9V	78ohm
Output	Collision+	+/-4V	+/-0.6 to +/-0.9V	78ohm
	Collision-	+/-4V	+/-0.6 to +/-0.9V	78ohm

Connector: 15-pin D-subminiture male with locking posts Power: 9.8 to 15.5VDC, 450ma MAX. Size: 1.5"W x 6.75"H x 3/8"D Watchdog Timer: 40 to 80msec LED: No light means no power/transmission from station exceeds 50msec nominal/internal fault detected Collision Presence Test: 0.3 to 3.0usec following end of reception, three cycles minimum

* Input circuits will track the common mode voltage or the received signals.

I

Vampire Transceiver Box Installation



I

Vampire Transceiver Box Installation

This procedure provides the information necessary to install additional Ethernet (Vampire) transceivers in the field.

I.1. Tools and Equipment Required

- 9/16" open-end or adjustable wrench
- TCL Coring Tool Kit (TCL A0003-DS-0)
- Vampire Transceiver Box (TCL 2010ECS)

I.2. Transceiver Installation

1. Clamp the tap block (TCL A0003-CO-1) to the Ethernet cable with the threaded hole in the block facing upwards. Refer to Figure I-1.
2. Place the clear plastic shim (TCL A0003-HO-0) on the Ethernet cable with the gap in the shim facing upwards. Center the tap block on the shim (refer to Figure I-2). *Locate the tap block in an area where it will not contact grounded objects, such as conduit or piping.*

Figure I-1 *Tap Block*

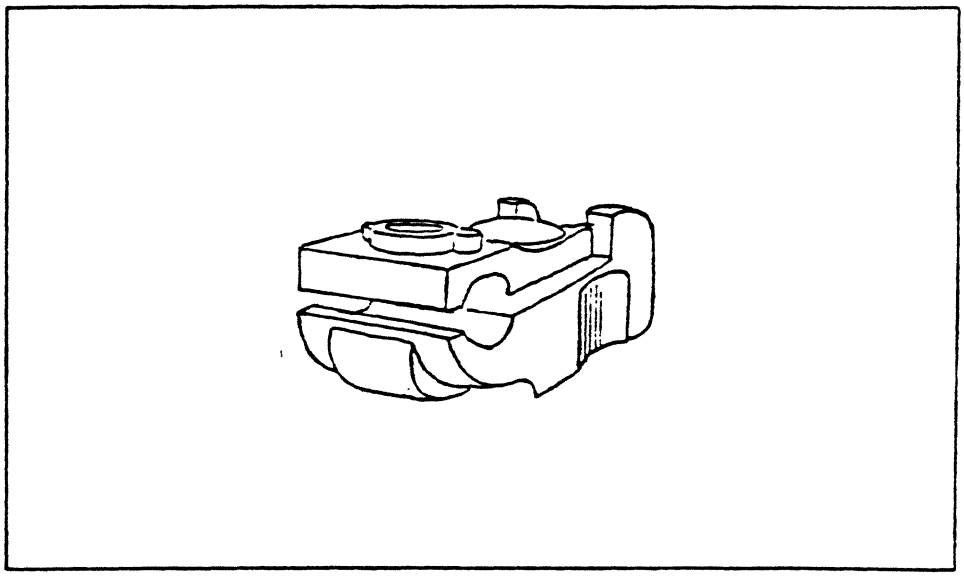
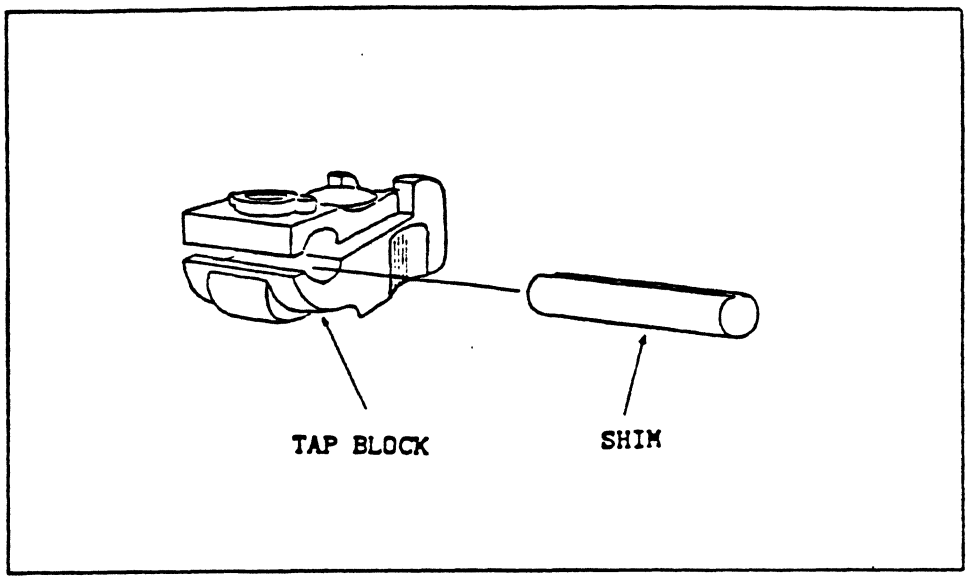
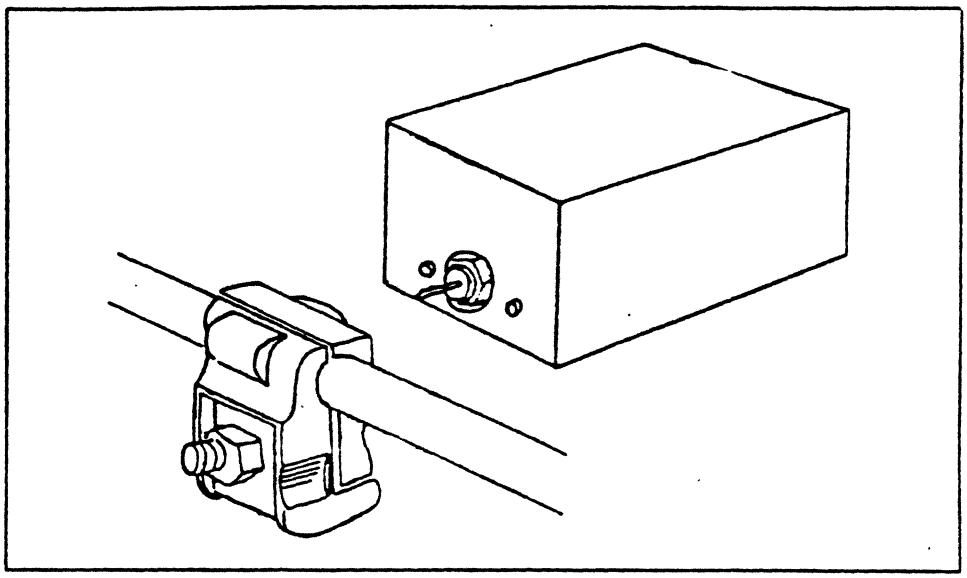


Figure I-2 *Shim Placement*



3. Tighten the 9/16" tap block nut.
4. Screw the cable coring tool (TCL A0003-DO-1) into the threaded hole in the tap block until the tool bottoms out, then remove the tool from the tap block. Repeat this process several times.
5. Insert the shield removal tool (TCL A0003-D1-0) into the hole in the tap block. Rotate the tool to cut through the cable shielding. Use a scribe to remove any shielding material or ground braid remaining in the hole. Failure to remove loose ground braid from the hole may cause a short in the Ethernet cable when the transceiver is installed. This condition will bring down the entire network.
6. Screw the piercing tool (TCL A0003-02-0) into the threaded hole in the tap block until it bottoms out. Contact with the conductor should be felt. Remove the tool and verify that a pinpoint of metal is visible through a small hole in the insulation.
7. Remove the protective cover from the stinger on the vampire transceiver box and install the O-ring on the threaded stinger housing (refer to Figure I-3).

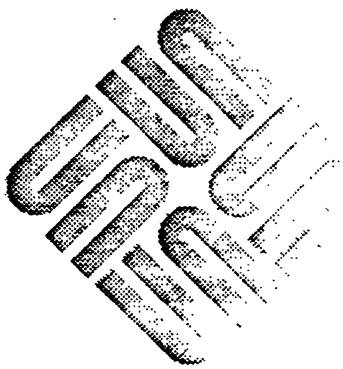
Figure I-3 *Transceiver Installation*



8. Carefully insert the stinger housing, on the transceiver box, into the hole in the tap block. Screw the tranceiver into the tap block until the O-ring is seated. Do not overtighten the transceiver.
9. Verify that there is +12VDC at pin 13 of the interface connector, on the transceiver box.
10. Insert the male interface cable connector into the corresponding female connector on the transceiver box (refer to Figure I-3). Use the slide lock, on the interface cable connector, to secure the cable to the box.
11. When power is applied to the transceiver box, the LED located on the rear panel of the box should light. If the LED fails to light, there is a problem with the transceiver and it should be replaced.

J

System Block Diagram



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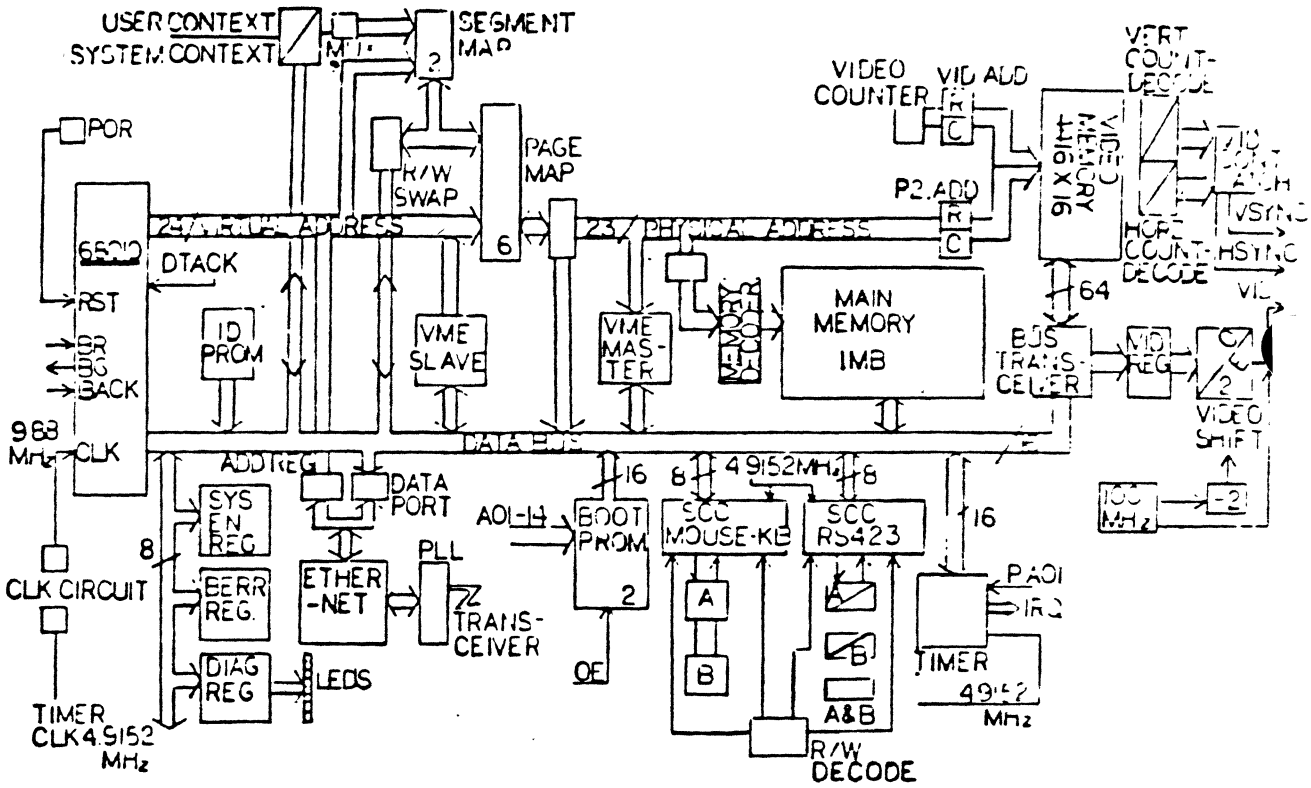
System Block Diagram



K

K

Specifications

This appendix provides a summary of Sun-2/50 specifications and features.

K.1. CPU

- M68010 16-bit, virtual memory microprocessor

K.2. Memory

- 1MB (64K) or 1/2/3/4MB (256K) of main memory
- 1MB (64K) or 1/2/3/4MB (256K) of expansion memory
- high-speed, no-wait state operation
- transparent hardware memory refresh
- byte parity error detection
- up to 128KB of EPROM
- software-readable ID PROM

K.3. Memory Management Unit

- Sun-2 memory architecture
- two-level, multiprocess, virtual memory management
- full support for demand paging
- 16MBs of virtual address space per process
- separate address space for supervisor and user
- valid, accessed and modified tags to assist paging algorithms
- separate read, write and execute tags for user and supervisor
- direct virtual memory access (DVMA) from VME bus

K.4. Display Subsystem

- dedicated, dual-ported video memory
- 1152 pixel x 900 line display format
- 100MHz video clock
- 67Hz non-interlaced video refresh

K.5. Ethernet Interface

- VLSI Ethernet controller
- digital phase-locked decoder
- packets transferred directly in and out of main memory
- extensive diagnostic capabilities

K.6. Serial I/O Ports

- two programmable serial I/O ports
- based on synchronous communications controllers
- software-programmable baud rates (75 baud to 19.2 Kbaud)
- synchronous, asynchronous and bit-stuffing protocols
- two serial ports for keyboard and mouse

K.7. Diagnostic Features

- diagnostic LED display
- bus error register
- watchdog reset timer
- bus timeout timer

K.8. VME Bus Specification

Master Capabilities

- 8-bit/16-bit data bus
- 16-bit/24-bit address bus
- 100usec timeout option
- 7-level, jumper-selectable interrupt handler
- level 3 release-on-request option

Slave Capabilities

- 8-bit/16-bit data bus
- 24-bit address bus
- no interrupter options

.H 3 "System Controller Capabilities"

- 16MHz jumper-selectable clock option
- level 3 bus request level

K.9. Power Monitor Capabilities

- ASFAIL signal asserted when voltage is below 4.5VDC
- system reset (SYSR) asserted during CPU reset
- system fail (SYSFAIL) may be inhibited

K.10. Environmental Characteristics

- operating temperature 10-55 degrees C
- humidity 0-90% non-condensing

K.11. Power Characteristics

- 12.0 amp max at +5.0VDC +/-5%
- 0.5 amp max at +12VDC +/-5%
- 0.5 amp max at -12VDC +/-5%

Physical Characteristics	- height 55.1cm (21.7") - width 53.3cm (21.0") - depth 43.7cm (17.2") - weight 20.4kg (45lb)

2.7. VIDEO MONITOR ADJUSTMENTS

This chapter describes how to perform video monitor adjustments. These adjustments may be used to correct video problems, such as vertical scrolling or an incorrect image size, or they may be used to simply improve the quality of the video image.

NOTE: This section is referred to as "F3" in the Quick Reference Troubleshooting Guide" in this chapter.

These adjustments do NOT correct problems in the video controller circuits on the CPU board.

The Sun 50 comes with two types of video monitor; one by Phillips and the other by Moniterm. In this procedure, both are treated the same; however, for further information, each has its own manual. For manual part numbers, see the introductory material at the beginning of this procedure.

Both video monitors meet the following specifications:

Video Input -- Balanced ECL
Video Display -- 1152 X 900 pixel display (1024 X 1024 optional)
Video Clk -- 10 nsec, 100 MHz
Horizontal Sync -- 16000 usec, 62.5KHz
Vertical Sync -- 15000 usec, 66.66kHz
Horizontal Retrace -- 4.48 usec
Vertical Retrace -- 600 usec

WARNING: The video circuitry generates extremely high voltages, particularly the output of the PKT high voltage supply and the anode connection to the CRT. To avoid injury, be sure all power to the monitor is OFF before attempting repairs.

CAUTION: To avoid damaging the video circuits, DO NOT use a standard screwdriver to turn adjustment pots. Instead, use a non-metallic adjustment tool, also called a pot adjuster or a tweeking tool.

NOTE: This manual only covers basic adjustments which do not require removing the mesh screen inside the monitor rear housing. For more information, read the appropriate video screen manual.

The adjustments are on the deflection board mounted vertically to the right of the video screen looking in from the back of the system with the rear panel removed.

1) Remove the set screws holding the rear cover on the workstation.

2) Read the description following this procedure, and perform any adjustments indicated.

3) When the adjustments are complete, replace the workstation rear cover.

4) If the adjustment fails to correct the problem, refer to the monitor's manual or return the system to Sun.

DESCRIPTION OF VIDEO MONITOR ADJUSTMENTS

NOTE: See Figure 2-1 for adjustment pot locations.

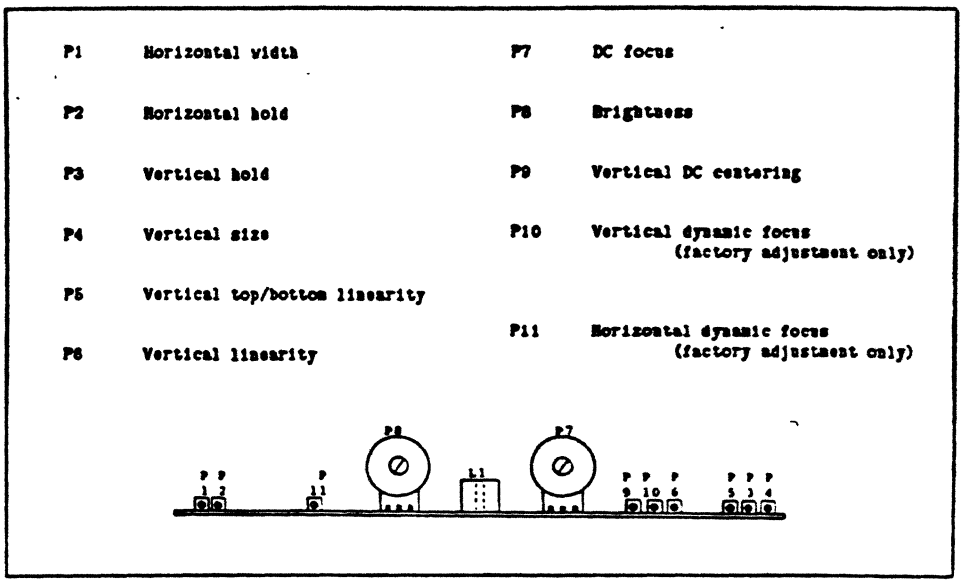


Figure 2-1: Adjustment Pots

P1 – Horizontal width. This controls the horizontal left/right width of the visible display on the screen. Turning the adjustment screw clockwise expands the frame; counter-clockwise reduces the size of the video frame.

P2 – Horizontal hold. This controls the horizontal left/right movement of the video frame on the CRT screen. Clockwise adjustment moves the image to the left; counter-clockwise adjustment moves it to the right.

P3 – Vertical hold. This controls the top-to-bottom movement of the video frame as follows:

a) Turn P3 adjustment pot in one direction until the picture goes out-of-sync (rolls up or down the screen).

b) Counting the number of turns you make, adjust P3 in the opposite direction until the screen goes into sync, then out-of-sync in the opposite direction.

c) Turn P3 back in the original direction by half this number of turns.

NOTE: This procedure provides an average position between the two extremes of vertical sync. The return adjustment usually requires around 5 or 6 turns.

P4 – Vertical size. Controls the top-to-bottom size of the video frame. Clockwise motion expands the video frame; counter-clockwise motion contracts it.

P5 – Vertical top-to-bottom linearity. Controls the relative size of the image at the top and bottom of the screen compared to the image in the middle of the screen. Clockwise adjustments make the top and bottom images relatively larger; counter-clockwise adjustments

make them relatively smaller.

P6 – Vertical linearity. Controls the size of the image ofer the entire screen area. Clockwise adjustment moves the top and bottom edges away from the center; counter-clockwise adjustment moves them closer.

P7 – DC focus. Controls the sharpness of the overall image. Fill the screen with an image, then turn the pot until the image is sharpest (generally around the center of the adjustment).

P8 – Brightness. Controls the contrast between the light and dark areas of the screen. **This adjustment should not normally be performed in the field, as incorrect adjustment can damage the picture tube.** The remote brightness adjustment pot, located on the exterior of the Model 50, is normally used for adjusting brightness.

P9 – Vertical DC centering. Controls the up-down position of the video frame on the screen, Turning the pot clockwise moves the image down, and turning it counter-clockwise moves the image up.

P10 – Vertical dynamic focus. NOT FIELD ADJUSTABLE

P11 – Horizontal dynamic focus. NOT FIELD ADJUSTABLE.

NOTE: Bleeding characters indicate possible dynamic focus problems. Adjusting P7 sometimes corrects this problem.