OMRON

MODEL 8025G
CRT TERMINAL

OMRON

8025 CRT TERMINAL

MAINTENANCE MANUAL

OMRON CORPORATION OF AMERICA

INFORMATION PRODUCTS DIVISION

432 TOYAMA DRIVE, SUNNYVALE, CA. 94086

(408) 734-8400 TWX 910-339-9341

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OMRON P/N 88-036-XXX

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FOREWORD

This manual gives accurate, usable information to help you get the best service from your 8025 CRT Terminal.

It supplies you with the details needed to:

- become thoroughly familiar with the 8025
- operate the 8025
- understand how the 8025 operates
- service the 8025

We have taken care to make this manual as complete, accurate, and understandable as possible. Your comments and suggestions for increasing its quality and effectiveness will be most welcome. A convenient, pre-addressed "Publication Change Request" form for this purpose is provided on the next page.

To receive updated materials, your manual must be registered with Omron. A pre-addressed form is also supplied for this purpose.

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1.1 GENERAL DESCRIPTION

The 8025 CRT Terminal is a versatile, simple-to-operate, self-contained cathode ray tube (CRT) display with keyboard entry that is capable of performing data processing functions. Capabilities of the 8025 cover a broad spectrum...from simple teletype (TTY) replacement to stand-alone operations.

Primary application for the 8025 is as a remote intelligent interactive terminal. In this role, it provides direct input of source data via keyboard entry, in addition to editing, information retrieval, and visual display of both transmitted and received data.

1.1.1 Functional Description

The 8025 CRT Terminal is a computer system designed around an internal microprocesor (CPU) interfaced to memory. The CPU allows the terminal to be easily adapted to many applications and functional routines without hardware changes. In addition, data bus organization permits the 8025 to be interfaced to a wide selection of peripherals such as communications modems, auxiliary storage devices, and printers.

The 8025 Terminal has an ASCII (American Standard Code for Information Interchange)96- or 64-character keyboard. Keyboard arrangement, shown in Figure 1-1, conforms with the QWERTY format. In addition, there are 14 special function keys and 6 basic cursor control keys. The terminal also has a 12-key numeric pad.

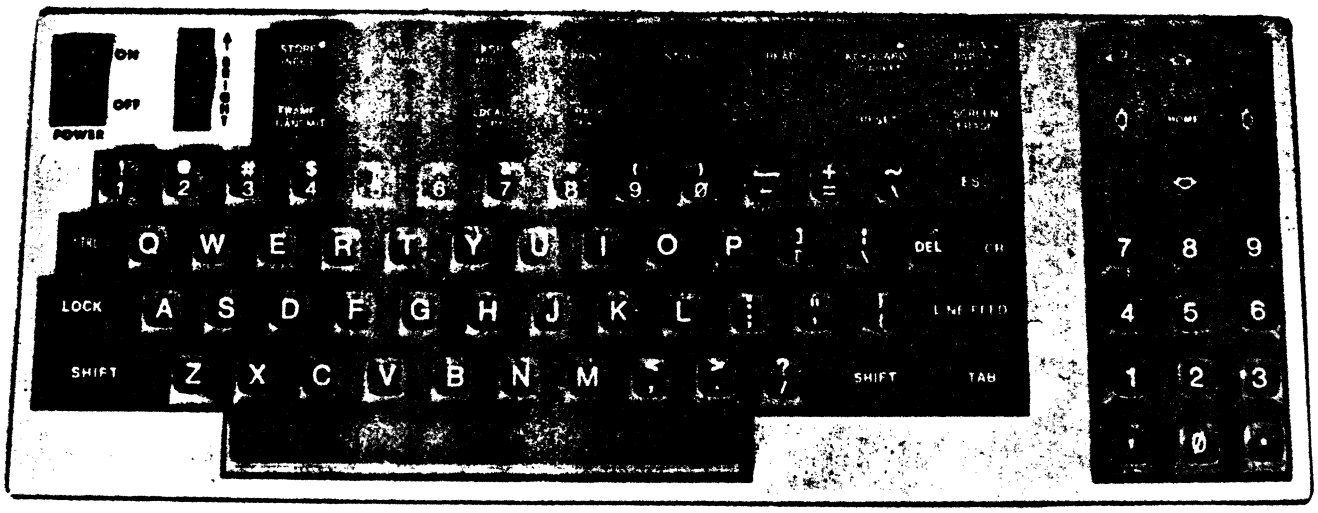


Figure 1-1. Keyboard arrangement

On 24-line-per-page terminals, up to 1,920 characters (80 characters per line) can be displayed on a 15-inch CRT display. Up to 960 characters can be displayed on 12-line-per-page terminals. The basic memory consists of a 1,024 byte RAM (random access memory) refresh memory and a 2,048 byte PROM (programmed read only memory) or ROM (read only memory) program memory. Communications I/O (input/output) interfacing conforms with Electronic Industries Association (EIA) Standard RS-232C. Additional RS-232 interfaces are included to interface the terminal with a printer and an auxiliary memory.

Paragraph 1.2 gives complete specifications for the terminal.

1.1.2 Mechanical Description

External. Figure 1-2 shows the outside of the 8025. The terminal is contained within a two-piece, free-standing plastic housing. Its size, weight, and design make the unit ideal for table or desk-top installation. Interfacing with external equipment and primary power is done at the rear panel. Only five screws need to be removed to take off the top section of the housing. With this section removed, the internal assemblies are easy to reach.

Internal. Figure 1-3 shows the inside of the 8025. Most of its circuitry is contained in a card cage that accommodates up to 18 plug-in circuit cards. Immediately above the cage is the CRT electronic circuitry. CRT electronics are mounted on the chassis and circuit cards. A removable power supply assembly is located behind the card cage, below the CRT. The keyboard assembly is also removable.

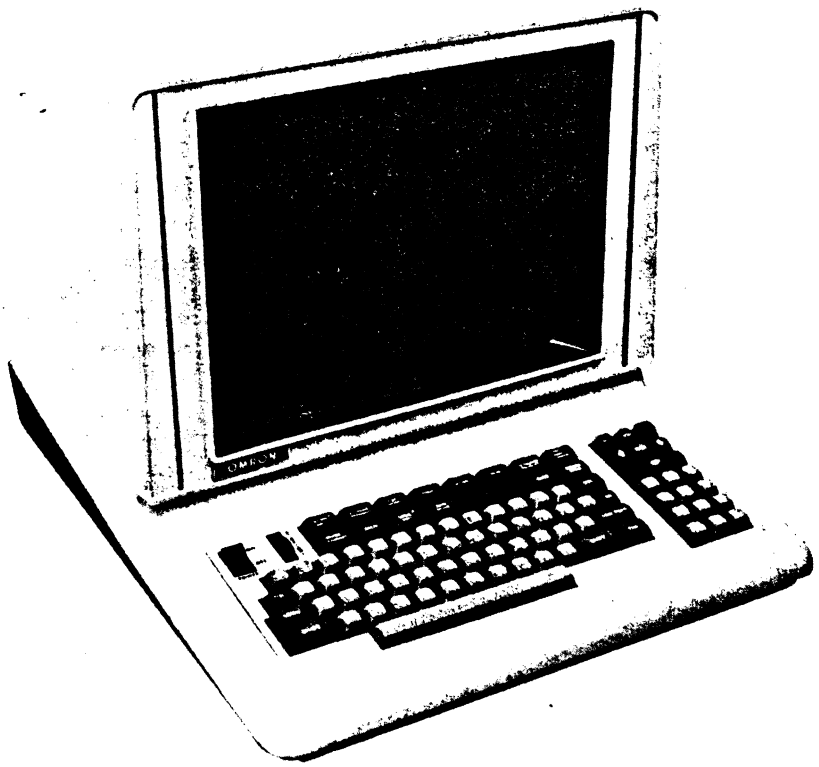


Figure 1-2. Exterior of 8025 CRT terminal.

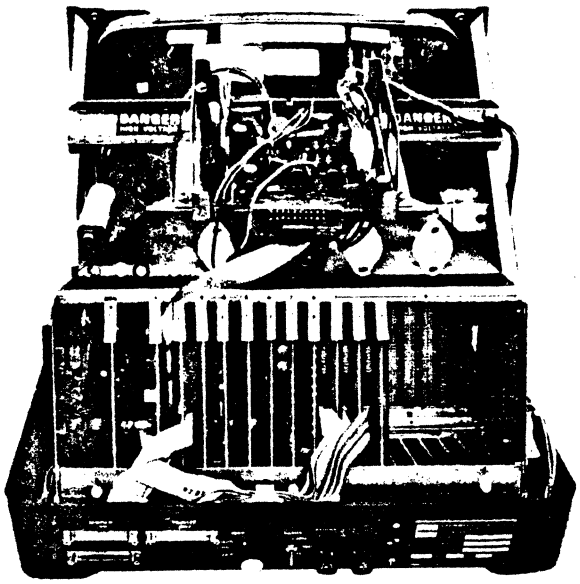


Figure 1-3. Interior of 8025 CRT terminal.

1.1.3 Basic Operation

A simplified block diagram of the basic 8025 terminal is shown in Figure 1-4. For simplicity, the diagram shows internal communications taking place over only one data-address bus.

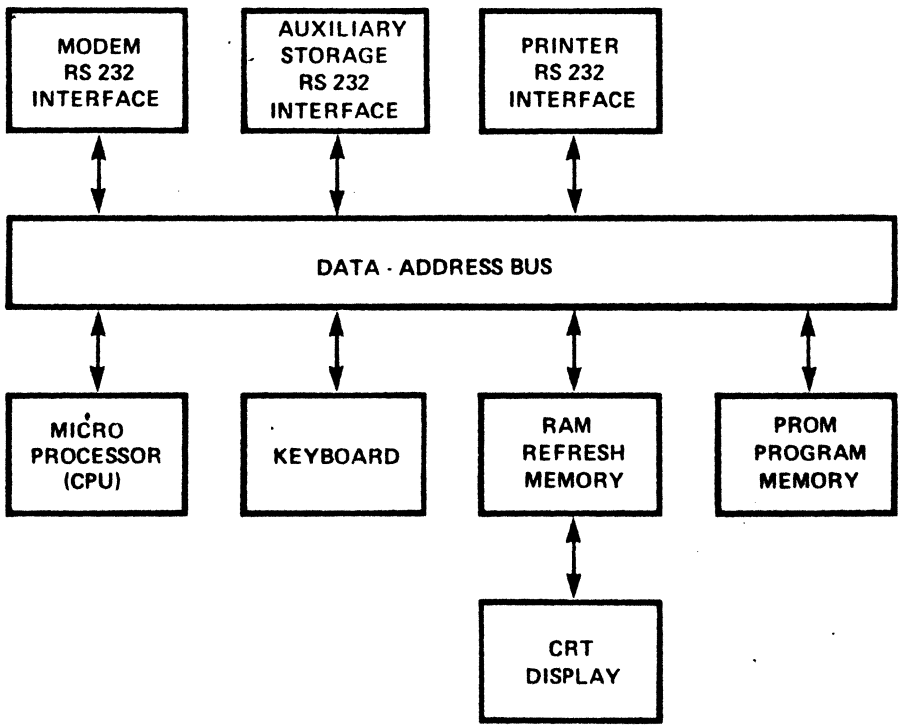


Figure 1-4. 8025 CRT terminal, simplified block diagram.

Nearly all operations in the terminal are controlled by the CPU according to instructions stored in the program memory. Typical operation is briefly described in the following paragraphs.

The CPU periodically polls the I/O cards and other functional modules on the bus to find whether any are ready to send or receive data. Assume the keyboard has data for the CPU. The keyboard intercepts a poll and identifies itself to the CPU. The CPU then enters the keyboard routine in program memory and enables the keyboard to transfer the data.

Following program instructions, the CPU processes the data. If the data is a character for display, the CPU determines where the next character is to be displayed and stores it at that location in the refresh memory. The refresh memory can then supply the data to the CRT display. If the data is a function code (e.g., carriage return), the CPU executes the instructions to move the cursor to the start of the line in refresh memory.

A data transfer from an I/O interface is performed in the same manner. In this case, the interface intercepts the poll and identifies itself to the CPU. The CPU enables the transfer and processes the data as if it came from the keyboard.

Assume the CPU has data for the interface. The CPU addresses, enables, and sets up the interface for the transfer. When the interface responds to the next poll, the CPU places the data on the bus for the interface.

1.2 SPECIFICATIONS

1.2.1 Standard Terminal Specifications

Specifications for the 8025 CRT Terminal are given in Table 1-1.

Table 1-1. 8025 CRT terminal specifications

PARAMETER	SPECIFICATION
8025 CRT Display	
Screen Size	Nominal 8" x 10", 15" diagonal.
Safety Glass	Integral part of CRT face.
Phosphor	P4 (white, medium persistence).
Deflection Angle	110°.
Refresh Rate	60 Hz.
Resolution	1,000 TV lines at 40 fL, center. 800 TV lines at 40 fL, corner. 0.010" diameter spot at center.

Table 1-1. 8025 CRT terminal specifications (continued)

PARAMETER	SPECIFICATION
Radiation	Complies with DHEW Rules 42-CFR-Part 78.
Mechanical	Integral part of 8025 Terminal.
Display Format	
Scanning	Modified raster, 60 frames/sec.
Symbol Formation	Upper case and numerics, 7 x 7 dot matrix; 14 x 7 effective dot matrix with 1/2 dot shift provides more natural-looking characters; lower case, 7 x 9 dot matrix (7 x 7 displayable).
Character Size	0.125" x .0875" (H x W).
Page Format	80 characters/line, 24 lines/frame (1,920 characters/frame max. displayable) or 80 characters/line, 12 lines/frame (960 characters/frame max. displayable).
Character Set	ASCII, 64 or 96 characters.
Memory System	
Display Refresh	RAM, 1,024 bytes.
Program	PROM or ROM, 2,048 bytes.
Keyboard	
I/O Code	ASCII, 64 or 96 alphanumeric character.
Arrangement	QWERTY.
Numeric Pad	12-key including decimal point and comma.
Cursor Type	Nondestructive blinking underline.
Cursor Control	6-way--up, down, left, right, home, and return left to next line on "Next Line" (↵) command.

Table 1-1. 8025 CRT terminal specifications (continued)

PARAMETER	SPECIFICATION
Control Keys	14--carriage return, line feed, tab, delete, shift lock, cursor controls, escape, and control.
Special Function Keys	12--store input, storage transmit, KSR mode, frame transmit, print, store, break, backspace, local copy, read, reset, and screen erase.
Indicator Lights	6--receive parity error, keyboard disabled, KSR mode, local copy, storage transmit, and store.
Input/Output	
Modem Interface	RS-232 asynchronous - 110, 300, 1,200, 1,800 and 2,000, switch selectable. ASR/KSR half/full duplex. 11-bit character, 110 baud. 10-bit character, all other rates. Parity - odd, even, or none, switch selectable.
Printer Interface	RS-232 asynchronous - 1,200 baud standard; 110, 300, 1,200, 1,800, 2,000 selectable by internal jumper option.
Auxiliary Storage Interface	RS-232 asynchronous - 1,200 baud standard; 110, 300, 1,200, 1,800, 2,000 selectable by internal jumper option.
Operating Features	
N-Key Rollover	No data loss when two or more keys are simultaneously depressed.
Acoustic Feedback	Programmable beep indicates that an event has taken place, or is taking place, in the terminal (e.g., end of line).
Automatic Repeat	Character repeats 15 times/sec if key is depressed for 0.5 sec or longer.
Tab	Transmits TAB code in KSR mode.
Editing	Automatic character insertion at position indicated by cursor replaces previously recorded character.

Table 1-1. 8025 CRT terminal specifications (continued)

PARAMETER	SPECIFICATION
Electrical	
Input Power	115 V ± 11.5 V ac, 59-61 Hz, 300 watts.
Mechanical	
Size	16" height, 17.5" width, 23" depth.
Weight	50 lb.
Mounting	Free standing.
Cabinet	Plastic, beige finish.
Environmental	
Temperature	Operating, +5° C to 40° C ambient. Storage, -40° C to +65° C.
Humidity	5 to 80%, noncondensing.
Altitude	10,000 feet maximum.

1.3 WARRANTY INFORMATION

This section contains OMRON's warranty and explains the warranty policy as it pertains to your 8025 CRT Terminal. Your 8025 Terminal was fully inspected and tested for workmanship and proper operation prior to shipment.

1.3.1 Claim for Transit Damage

It is important that the instrument be inspected for physical damage an tested for proper operation (see Section 3) upon arrival at its destination. If i does not operate properly, or is damaged in any way, a claim should be filed immediately with the carrier. A complete report of the damage should be furnished the claim agent and a copy forwarded to OMRON. Do not proceed with repair; OMRON wil advise you of the disposition to be made of the terminal and arrange for repair or replacement. Please include name of equipment, model number, serial number and your purchase order number in any correspondence regarding the terminal.

1.3.2 Statement of OMRON Warranty

OMRON warrants to the original purchaser, for a period of three (3) mon from the date of shipment, that the 8025 CRT Terminal shall be free from defects i material and workmanship, but does not cover shipping damage, physical abuse, fire theft, damage incurred during field repair, or damage as a result of not following proper preventive maintenance procedures.

All parts and labor will be provided free of charge for three (3) months at the OMRON-designated facility (see Paragraph 1.3.4) with shipping being paid in both directions by the customer.

The customer has the option of returning either the complete terminal, individual assemblies, or components. All items will be system tested before return to the customer. A Merchandise Return Authorization should be used for this purpose. (See the sample on page 1-11).

This warranty does not apply to fuses, lamps and other such parts for which normal periodic replacement is required.

Vendor-supplied subassemblies and sealed units are subject to their individual warranties and cannot be opened or repaired by the customer during the warranty period without voiding their warranties. Paragraph 1.3.5 provides information on such items used in the 8025 Terminal.

This warranty is in lieu of all other warranties, expressed or implied, statutory or otherwise, including any implied warranty of merchantability. OMRON shall not otherwise be liable to any inquiries, loss or damage direct or consequential arising out of the use or inability to use the equipment.

1.3.3 Warranty Claims Against OMRON

When making a warranty claim on your 8025 CRT Terminal, follow the repair and return policies outlined in Paragraph 1.4 of this manual.

If damage to the 8025 Terminal has been caused by improper use, abnormal operating conditions, improper maintenance or other factors excluded by the warranty, repairs will be billed at cost. In such cases an estimate will be submitted before the work starts.

1.3.4 OMRON Designated Facility

The following facility is authorized to repair the 8025 CRT Terminal:

OMRON Corporation of America
Information Products Division
Field Service Department
432 Toyama Drive
Sunnyvale, Ca. 94086

1.3.5 Suppliers Warranties

Vendor-supplied subassemblies and units used in the 8025 CRT Terminal which are covered by supplier warranties are as follows:

Item	Supplier	Warranty Period
CRT Display	Miratel	12 months

1.4 REPAIR AND RETURN OF EQUIPMENT

1.4.1 Policy

OMRON shall provide maintenance (labor and parts) and shall keep the equipment in good operating condition. Maintenance shall not include repair of damage resulting from accident, transportation between sites, neglect, misuse, failure of electrical power or air conditioning or humidity control, or cause other than ordinary use.

1.4.2 Equipment Failure

When equipment failure occurs, regardless of cause, and the equipment is determined to be non-repairable on-site, it shall be returned to OMRON.

1.4.3 Non-repairable Determination

Normally, the determination of non-repairable equipment will be made with an OMRON representative present. If a representative is not available, authorization to return non-repairable equipment must be received from this repair facility:

OMRON Corporation of America
Information Products Division
Field Service Department
432 Toyama Drive
Sunnyvale, Ca. 94086
(408) 734-8400 TWX 910-339-9341

1.4.4 Equipment Return Procedure

The OMRON representative, whether present on-site or using communication media, will prepare the appropriate Merchandise Return Authorization (Form No. MRA-83-001).. This authorization must be individually numbered. It must properly identify the non-repairable equipment by description, part number, and serial number. The reason or reasons for return must also be stated in adequate detail. A sample Merchandise Return Authorization appears on page 1-11. A copy of the Authorization shall be filed at the returnee's site. The remaining copies will be attached to the shipping crate as shown on the form.

1.4.5 Packing and Packaging Procedure

After proper completion of MRA form, return the equipment as follows:

1. Pack the unit in a container appropriate for the method of shipment. Ideally, use a package similiar to the one in which the unit was delivered. Attach the MRA to the container.
2. Ship the unit, transportation prepaid, to the address mentioned in paragraph 1.4.3. All sub-assemblies and parts described in the warranty will be replaced if OMRON's examination discloses that the defects are within the limits of the warranty. If damage or defect(s) are not covered by the warranty, the returnee will be told what repairs are required and how much they will cost. The unit will be repaired and returned upon agreement.

OMRON CORPORATION OF AMERICA

Information Products Division
432 TOYAMA DRIVE
SUNNYVALE, CALIF. 94086
(408) 734-8400 TWX 910-339-9341

№ 009

MERCHANDISE RETURN AUTHORIZATION

CUSTOMER: Mr. Ron J. Fejeran
OCA
9401 Indian Head Highway
Oxon Hill, MD 20022

Date: 9-8-75

1 PLEASE COMPLETE THIS FORM AND RETURN IT TO OMRON CORPORATION OF AMERICA, INFORMATION PRODUCTS DIVISION, ATTACHED TO THE SHIPPING CRATE.

2 SHIP PREPAID TO:

U.S. SHIPMENTS

OMRON CORPORATION OF AMERICA
INFORMATION PRODUCTS DIVISION
432 TOYAMA DRIVE
SUNNYVALE, CALIFORNIA 94086

EX—U.S. SHIPMENTS

3 MRA Authorized by: E. L. Mleczko, Asst. Division Manager

ITEM	QTY	PART NO.	SERIAL NO.	DESCRIPTION
1	1	99-399-001	501	RS232

SAMPLE

REASON FOR RETURN: Does not transmit.

AUTHORIZED BY: Ron J. Fejeran — Government Marketing Mgr. — 9-8-75
Ron J. Fejeran (Name) / Title / Date

RECEIVED BY: Name / Title / Date

ROUTE TO: Quality Assurance for evaluation.

CUSTOMER FILE COPY

1.5 LIST OF OMRON MNEMONICS

The following list defines the various mnemonics developed for the 8025 CRT Terminal.

ADB0-7:	A Data Bus bits.
BA:	RS 232 signal used by modem.
BDB0-7:	B Data Bus bits.
BEEP:	Decode of CPU $\overline{I/O}$ command; triggers beep circuit which produces audible output whenever a Keyboard key is depressed.
BLANK:	Blanks screen under program control.
BLINK:	Signal from Refresh Buffer to enable blink function on Video Control Card.
CA:	RS 232 signal used by modem.
CD:	RS 232 signal used by modem.
CG0-7:	Character generator input bits; 8-bit ASCII code.
CLK RDY:	Clock ready; synchronous 8008 Ready with IC clock.
CLRF:	Clear 'F'; clears video attribute register on Video Control card at end of each scan line.
CNT 80:	Indicates next line shift register is loaded.
COMP BLNK:	Composite blanking signal.
CPU BUSY:	Indicates CPU is using memory busses.
CP:	Clock pulse; Keyboard encoder clock at H40 rate.
CPU R/$\overline{W}$:	CPU read/write; signal controlling writing of data into memories by CPU.
CS0-3:	Video status bits; CS0, CS1, CS2 and CS3 control video on/off, block/off, cursor underline, control/character display and half line mode.
CURS LINE:	Cursor line; defines the scan line in each character row on which cursor is displayed.
DSO:	Data strobe out; indicates Keyboard wants to send a character.

EOP: End of page; timing signal used to control the update of hardware parameters from 6 fixed locations in memory.

EOR: End of row; timing signal used to control loading of character display shift register.

EXT ADRS: External address; allows an external device to address memory.

H1: Timing signal; 7.488 MHz, one-half HF CLK.

H2: Timing signal; 3.744 MHz, one-fourth HF CLK.

H4: Timing signal; 1.872 MHz, one-eighth HF CLK.

H8: Timing signal; character clock, 670 nsec period.

H10: Timing signal; two character clock periods (1.34 usec).

H20: Timing signal; four character clock periods (2.68 usec).

H40: Timing signal; eight character clock periods (5.36 usec).

H80: Timing signal; 16 character clock periods (10.72 usec), equals horizontal blanking time.

H160: Timing signal; period equals 1/3 of horizontal scan line (21.44 usec).

H320: Timing signal; period equals 1/2 of horizontal scan line (32.16 usec).

HF CLK: Basic timing signal; provides reference for all terminal timing signals.

H LINE: Horizontal line; 15,000 Hz (63.32 usec), horizontal frequency.

H SYNC: Timing signal at scan line rate used to drive scan circuits in monitor (same as H DRIVE).

IC CLK: Timing signal in sync with alternate Ø2 clocks; indicates 2nd half of CPU cycle.

INH LD: Inhibit load; inhibits loading of video parallel-to-serial converter when Refresh Memory is accessed by anything other than the video generator.

IOB: Decode of CPU I/O command INP3; initiates data transfer to or from peripheral without resetting the interface.

IOD: Decode of CPU I/O command INP1; initiates data transfer to or from peripheral with reset of the interface.

KDB0-7: Keyboard data bus bits; data out of Keyboard.

LCLSB: Load count least significant bits; loads row position stored in Refresh Memory into cursor row register on Cursor Control Card.

LCMSB: Load count most significant bits; loads column position stored in Refresh Memory into cursor column register on Cursor Control Card.

LDCNT: Load count; clocks two-character delay, clocks write command to Refresh Memory.

LITE1-12: Interconnect circuits for Keyboard LED indicators.

LOAD F: Decode of video attribute character on CG0-7;controls loading of video attribute register.

MA0-15: Memory address bits.

MATCH: Signal generated whenever outputs from video counter and cursor position register are equal; used to generate cursor.

NULL: Detection of blank "character" in row (i.e., blank memory).

OE: Output enable; resets DS0 and enables Keyboard output register for next key depression.

PC6: D6 output of CPU during T2 state; one of two bits that define CPU cycle type.

PC7: D7 output of CPU during T2 state; second of two bits that define CPU cycle type.

POC: Power on clear; initializes Terminal when power is applied.

POLL: Decode of CPU I/O command (INP0); poll signal initiates selection of peripheral device for data transfer.

POS TIME: Position time; occurs at scan line rate (see timing diagrams in Section 4).

RATE: 5 pps clock; controls video blink rate.

RC: Row carry; blanks CRT during vertical retrace.

RD0-7: Data bits into Refresh Memory.

READ CLK: Read clock; used as a reference to generate timing signals for ROM memories.

REF ADRS: Refresh address; indicates refresh memory is being accessed.

REF R/$\overline{W}$: Refresh read/write; controls writing of data into Refresh Memory.

RESYNC: CPU SYNC output reclocked with Ø2.

RMO-7: Output data bits from Refresh Memory.

RPT: Repeat; signal to Keyboard telling it to repeat last character transferred as long as the key is depressed.

RS CLK: Clock used to generate timing reference for I/O data transfer RS 232 cards.

RSTO-2: Restart command bits; inserts program address into CPU.

SET LDFF: Set load flip-flop; output of load flip-flop loads video parallel-to-serial converter.

SPKR: Speaker; produces audible energy generated by BEEP oscillator circuit.

SR COUNT: Indicates refresh logic has control of memory bus.

SRINH: Shift register inhibit; controls loading of display shift register in half line mode.

STAT: Status; decode of CPU I/O command (INP2).

SYNC: Output of CPU; indicates CPU is on second half of a timing state.

T2 SYNC: Second half of CPU T2 timing state.

T3': Early T3 timing state; synced with IC CLK.

T3 SYNC: Second half of CPU T3 timing state.

UA CLK: Universal asynchronous clock; clocks transmitter-receiver on RS 232 Interface card.

UND BLNK: Undelayed blanking signal.

UPDATE: Pulse occuring at frame rate controlling updating of hardware parameter from 6 fixed locations in memory.

V1, V2, V4: Timing signal; defines scanning lines one through eight (character row lines are numbered 0 through 9).

V8: Timing signal; defines scan line nine (8) by itself, defines scan line ten (9) in conjunction with V1.

V10: Differentiates between even and odd vertical rows.

VIDEO: Signal which drives the monitor to produce the white areas on screen which form characters, video attributes, etc.

V DRIVE: Vertical drive.

V SYNC: Timing signal at frame rate used to drive scan circuits in monitor (same as V DRIVE).

WAIT: CPU timing state; indicates READY was low prior to end of T2 state.

WAIT SYNC: Second half of CPU WAIT state.

Ø1, Ø2: Timing signal that provides timing reference for all data transfer on memory busses.

Every 8025 CRT terminal is fully inspected and tested before shipment to ensure that it meets specifications. It is packaged for safe transit under normal freight-handling conditions. The terminal should normally arrive ready for use.

Claims with the carrier should be filed within 15 days from delivery. OMRON therefore recommends that you unpack and test the terminal upon receipt.

Terminal installation should be made as outlined in this section.

2.1 UNPACKING PROCEDURE

2.1.1 Inspection

Before unpacking the terminal, inspect the shipping container for signs of possible damage to the unit during transit.

2.1.2 Unpacking

Set the crate "Right End Up" and use a knife blade, 1/4" or less long, to open the top of the crate. Save the shipping container and packing materials in case the terminal must someday be returned to OMRON or shipped to a repair facility.

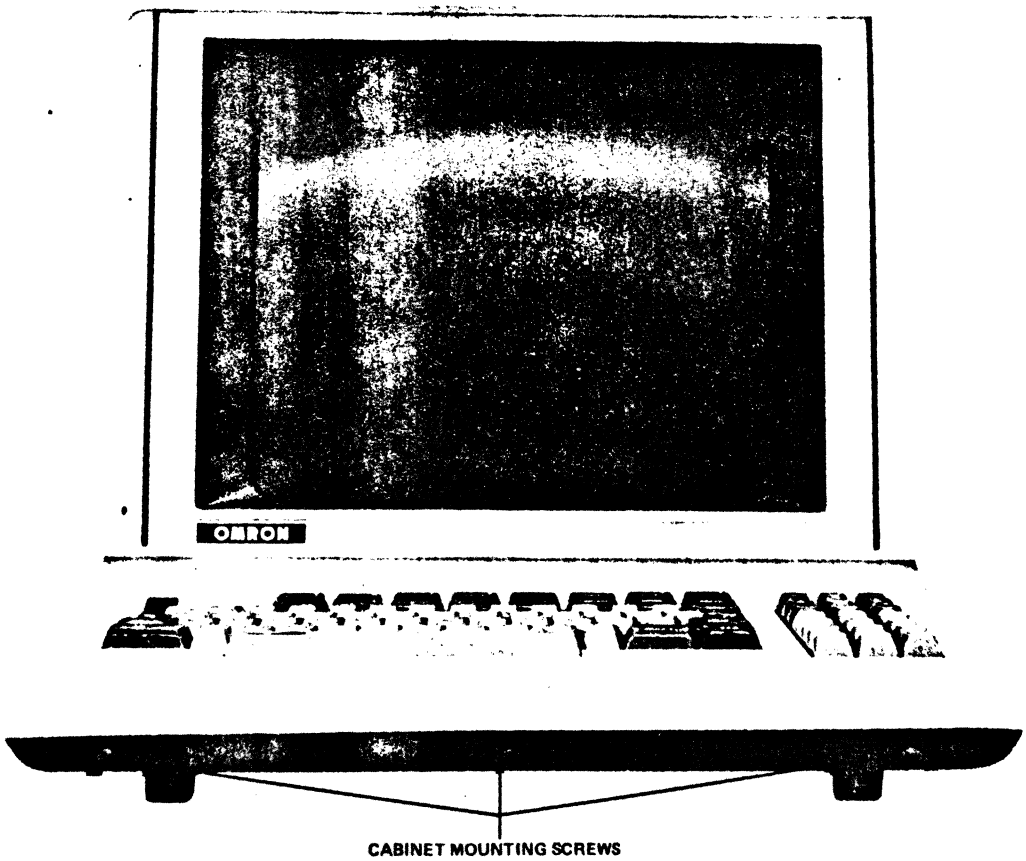


Figure 2-1. Cabinet mounting screws (front).

2.2 OFF-LINE CHECKOUT

2.2.1 Mechanical Inspection

External Inspection. Inspect the terminal for external damage such as broken keys or cracked cabinet. Should there be any damage, refer to paragraph 1.3.1 in Section 1.

If there is no damage, perform the operational check described in paragraph 2.2.2. Proceed with installation if the terminal is operating correctly. Should the terminal not operate correctly, first check that line voltage is present and the fuses are intact. Then remove the cabinet and make an internal inspection.

Cabinet Removal. To take off the top of the cabinet, remove the five screws (three on the front, two on the back) as shown in Figure 2-1 and Figure 2-2. Lift the cabinet top straight up. With the top portion of the cabinet removed, the internal assembly is easily reached.

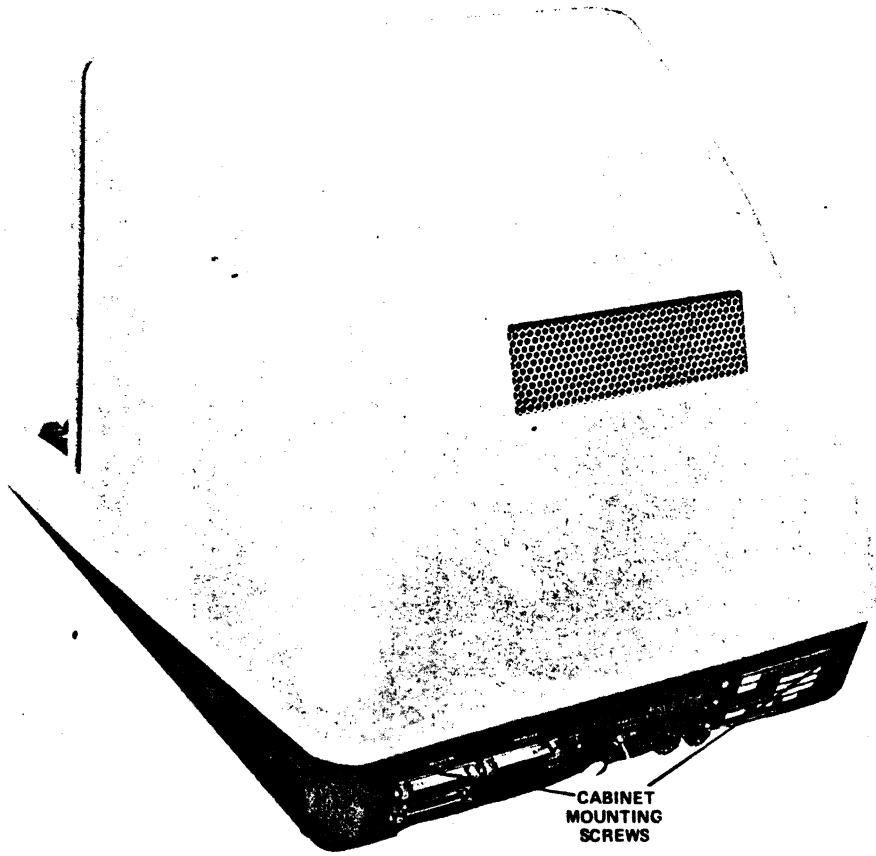


Figure 2-2. Cabinet mounting screws (rear).

Internal Inspection. Inspect the entire terminal for physical damage. Especially check around the neck of the cathode ray tube (CRT) and the Monitor Deflection Card (see Figures 2-3 and 2-5). If there is damage, refer to paragraph 1.3.1 in Section 1.

Make sure all circuit boards are properly seated and that the terminal has a full complement of cards, as shown in Figure 2-4. From left to right these are: Regulator Card, Cursor Control Card, Video Control Card, Refresh Buffer Card, Timing Control Card, Refresh Memory Card, Refresh Control Card, Processor Card, PROM Card, RS-232 Interface Card, Auxiliary Storage RS-232 Interface Card, Printer RS-232 Interface Card, and Terminator Card.

CAUTION: MOS ELEMENTS USED ON CIRCUIT CARDS ARE EASILY DAMAGED BY STATIC DISCHARGE. ALWAYS HANDLE CARDS SO THAT ANY DISCHARGE WILL NOT FLOW THROUGH THE CARD. BEFORE TOUCHING A CARD, PLACE ONE HAND ON THE TERMINAL CHASSIS AND USE THE OTHER HAND FOR THE CARD.

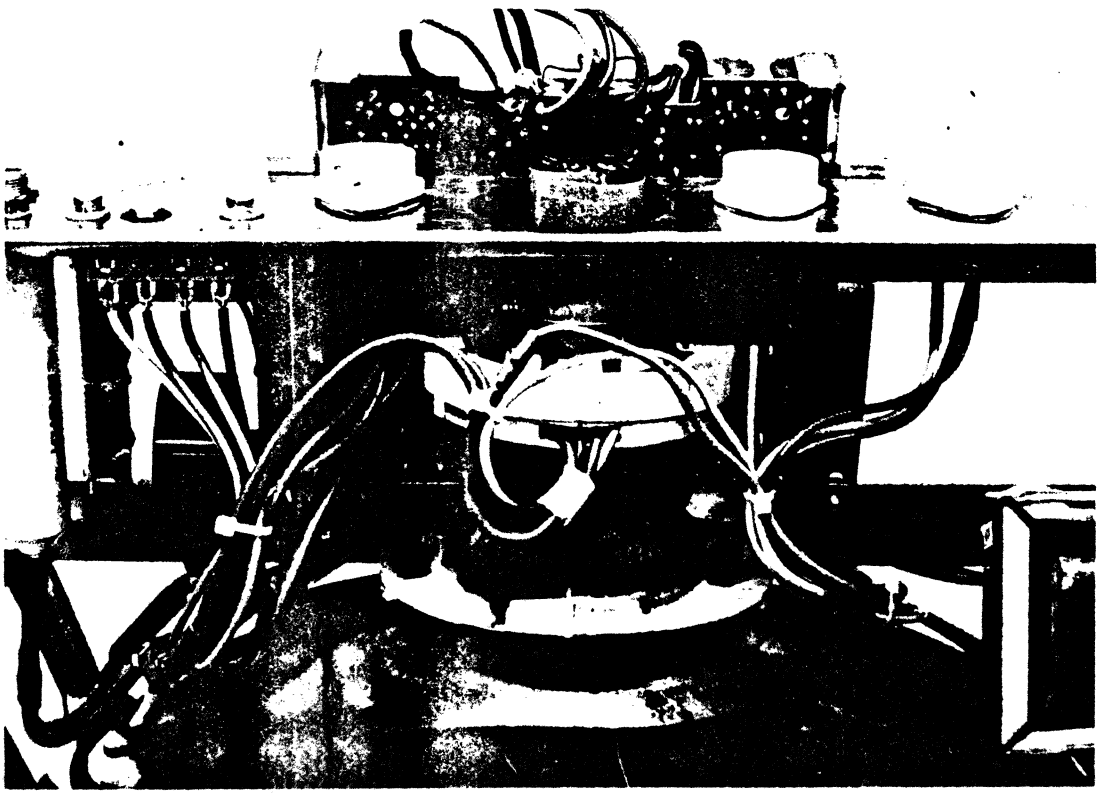


Figure 2-3. CRT display high voltage circuits (mounted below Monitor Deflection Board.)

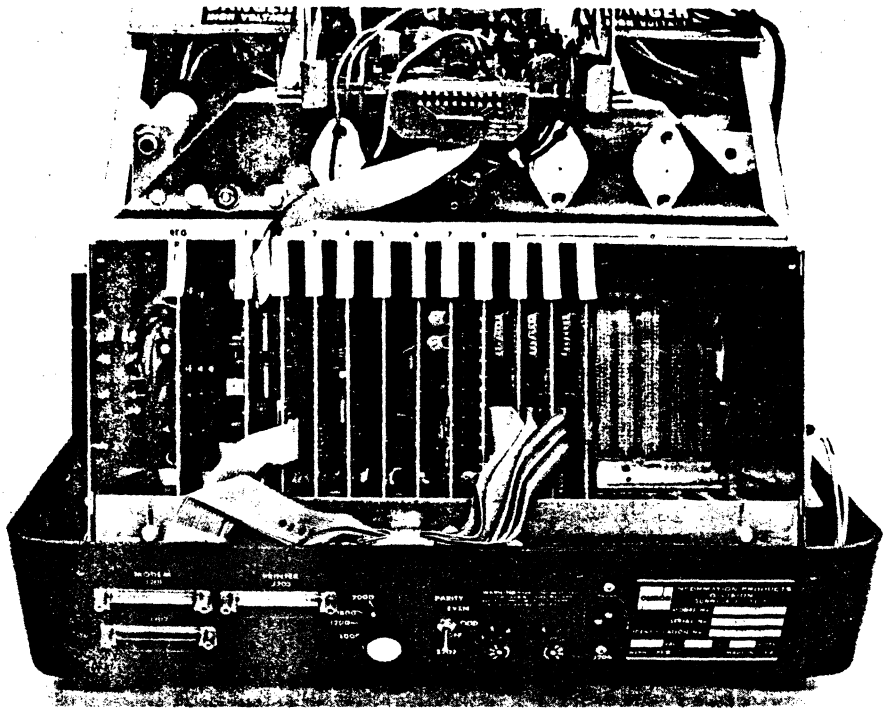


Figure 2-4. Printed circuit card locations.

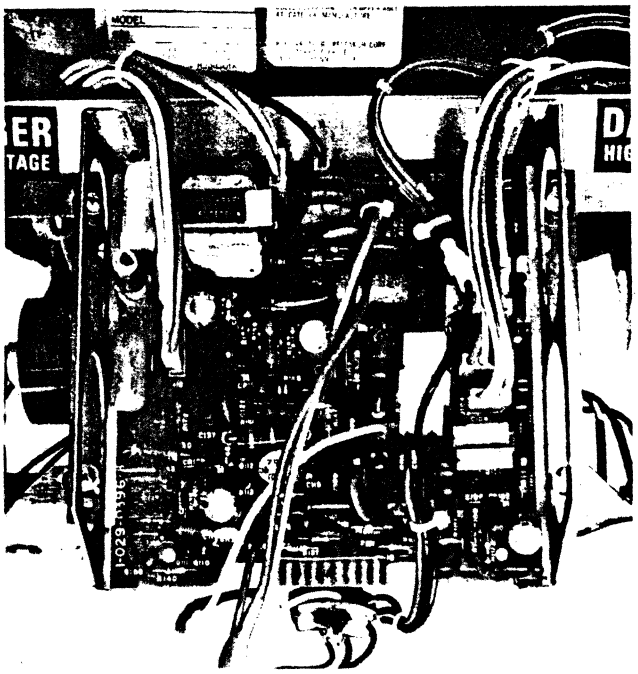


Figure 2-5. Monitor Deflection Board connections (viewed from top of terminal).

Figure 2-6 shows the correct routing of all flat-line interconnect cables in the terminal. Cable routing is as follows:

1) The cable on the far right (a 16-conductor flat-line) connects the Printer RS-232 Interface Card to J203, mounted on the rear panel of the terminal.

2) The second cable from the right (a 16-conductor flat-line) connects the Auxiliary Storage RS-232 Interface Card to J202, mounted on the rear panel of the terminal.

3) The next card, the Communications (Modem) RS-232 Interface Card, has two cables. A 14-conductor flat-line (top-connector) connects it to the Baud Rate Switch mounted on the rear panel of the terminal. A 16-conductor flat-line (just below the Baud Rate cable) connects the card to J201 mounted on the rear panel of the terminal.

4) The cable on the far left (a 16-conductor flat-line) connects the Cursor Control Card to the keyboard. This cable is routed along the right side of the terminal (viewed from front).

5) The cable running to the top of the photo (a 16-conductor flat-line) connects the Video Control Card to the Monitor Deflection Board.

6) The remaining cable (a 14-conductor flat-line) connects the Refresh Buffer Card to the keyboard indicator lights. This cable is routed along the right side of the terminal (viewed from front).

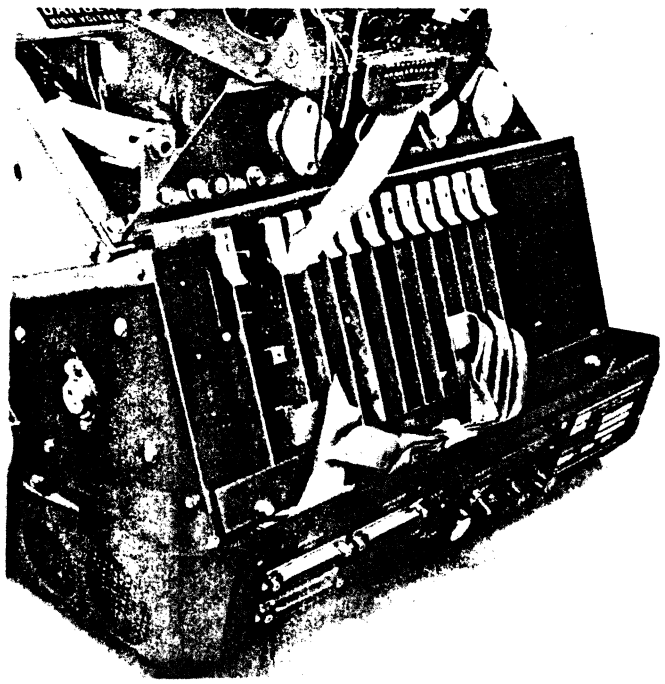


Figure 2-6. Flat cable connections.

Figure 2-7 illustrates flat-line connector configurations. Each flat line connector is labeled with pin numbers on the back. Pin 1 should be inserted into pin 1 on the socket.

If all cards are properly installed, interconnect cabling is correct, and there is no visible damage, replace the cabinet top and the screws.

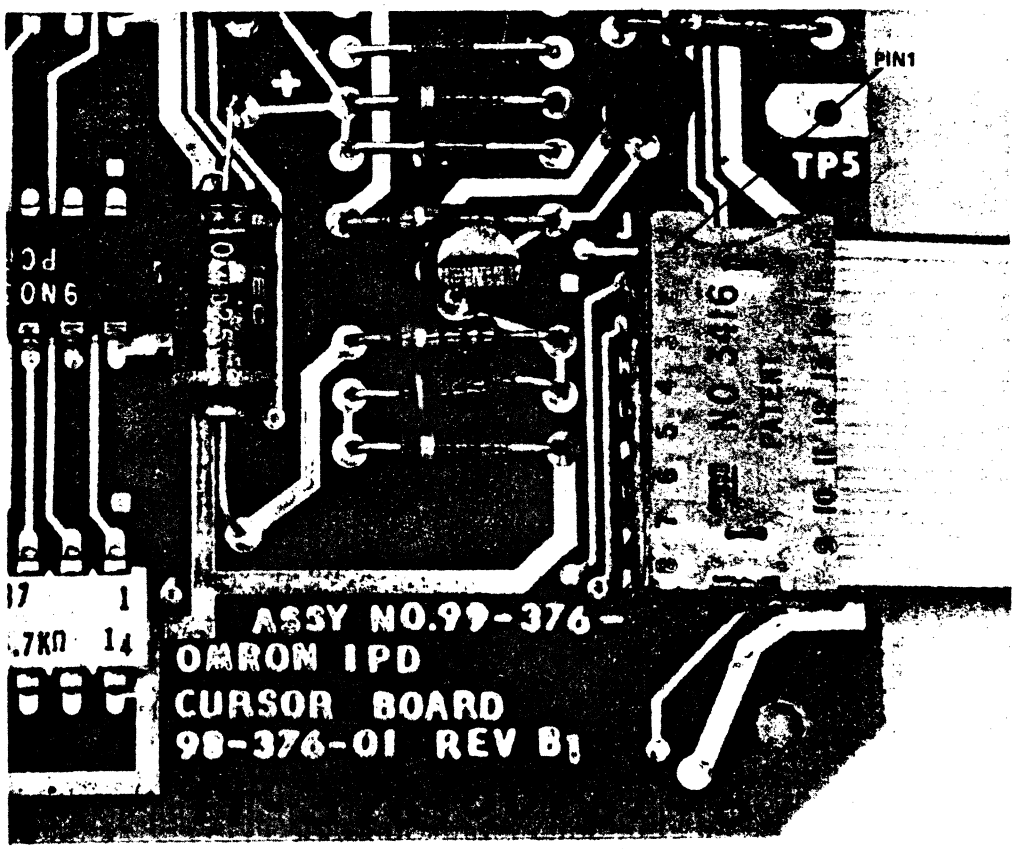


Figure 2-7. Flat-line connector configurations.

2.2.2 Operational Check

The purpose of the operational check is to determine that the terminal is operational as a stand-alone unit. To perform this check, proceed as follows:

1) Make certain that the Baud Rate Switch on the rear of the terminal is in the correct position for your application.

2) Connect the power cord to the NEMA-approved three-contact grounding outlet that supplies 117 V ac ±10%, 60 Hz, 1 Ø or the voltage specified on the identification label located on the bottom of the terminal. The outlet must provide at least 400 Watts of noise-free power. (If only a two-contact outlet is available, use a properly grounded two-wire-to-three-wire adapter or some other appropriate means to ensure chassis grounding).

3) Turn the terminal on with the On-Off Switch at the extreme upper left of the keyboard.

4) Listen for the sound of the cooling fans. If you cannot hear them, turn the terminal off and refer to paragraph 1.3.1. in Section 1.

5) Advance the Brightness Control (located to the immediate right of the On-Off Switch) all the way up. When the raster appears, reduce brightness until the raster disappears but characters are visible.

6) Allow the terminal to operate for a few minutes. Until the raster appears on the CRT, be alert to any abnormal sounds or odors. If you detect any, turn the terminal off and refer to paragraph 1.3.1 in Section 1.

7) Check out all keyboard functions (e.g., cursor and screen movements, edit functions, escape sequences, and alpha-numeric-symbol keys) for proper operation. Refer to Section 3.

2.3 INSTALLATION

2.3.1 Physical Requirements

Place the terminal on a stable platform at a height suitable for operator comfort in a place that falls within the environmental specifications for the terminal. (Refer to Table 1-1 in Section 1.)

2.3.2 Electrical Requirements

The terminal must be connected to a noise-free power line with the characteristics specified in Table 1-1 in Section 1.

Connect power cord to a NEMA-approved three-contact grounding outlet to ensure that the terminal chassis is grounded.

NOTE 1: If only a two-contact outlet is available, use a properly grounded two-wire-to-three-wire adapter or some other appropriate means to ensure chassis grounding.

NOTE 2: The use of extension cords is not recommended.

2.3.3 External Connections

All external connections are made at the rear of the terminal. Figure 2-8 identifies the external connectors. Table 2-1 defines the terminal-data system interconnects.

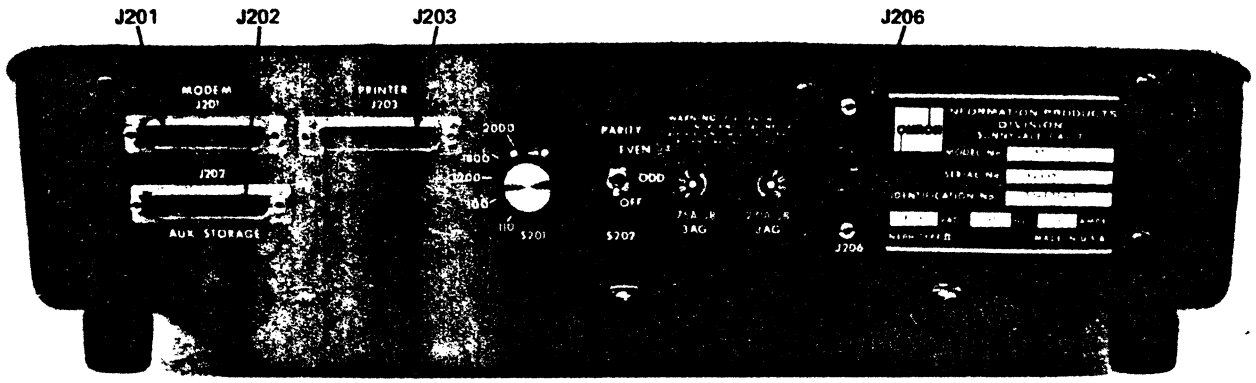


Figure 2-8. 8025 CRT Terminal: rear panel connectors.

Table 2-1. Terminal-system interconnection.

8025 CRT TERMINAL REAR PANEL CONNECTOR	CONNECTS TO
J201	Communications modem
J202	Auxiliary storage
J203	Printer
J206	117 V ac line

2.3.4 RS-232 Speed Adjustment

The Auxiliary Storage and Printer RS-232 interface cards are set for 1,200 baud, parity off. The speed for these cards can also be set for 110, 300, 1,800 and 2,000 baud. If a speed change is required, refer to Section 7.

2.4 ON-LINE CHECKOUT

Connect the 8025 CRT Terminal into the system. Use the system terminal operating procedure to determine that the 8025 terminal operates correctly in the system.

3.1 OPERATING CONTROLS

All day-to-day operating controls are located on the keyboard of the terminal. (See Figure 3-1.) Completely familiarize yourself with these controls. Read this section and use the controls while observing their effect on the display.

3.1.1 On-Off Switch

As shown in Figure 3-1, the ON-OFF switch is located in the extreme upper left corner of the keyboard panel. Press down on the upper end of the switch to turn the terminal on. Press down on the lower end to turn the terminal off.

3.1.2 Brightness Control

The BRIGHTNESS control is located next to the ON-OFF switch. Like the brightness control on a TV set, it controls the overall brightness of the white areas on the display screen.

For maximum brightness, move the control up until the stop is reached. For minimum brightness, move the control down until the stop is reached (dark screen).

There is no specific set-point for the brightness control. Continuous operation at a very high setting, however, can shorten CRT life. A recommended setting is one that makes the screen easy to read and comfortable for the eyes. Be sure to eliminate the raster.

3.1.3 Baud Rate Switch

The Baud Rate switch is located on the rear panel of the terminal. This switch sets the transmission rate for the modem interface (primary RS-232 Interface Card). Rates of 110, 300, 1,200, 1,800, and 2,000 baud are selectable with this control.

NOTE: Terminals with 2,400 baud option will have 2,400 baud in place of 2,000.

3.1.4 Parity Switch

The Parity switch is also on the rear panel of the terminal. The setting of this switch establishes the parity mode for the modem interface of the terminal. Odd parity, even parity and parity off are selectable with this control. The Parity Switch controls both transmitted and received data.

When the Switch is in the OFF position, all characters are transmitted with bit 8 low. (NOTE: Transmission with bit 8 high can be elected with a jumper option on the RS-232 Interface Card.) Parity in received characters is ignored.

In the ODD position, all characters are transmitted with odd parity; that is, bit 8 is set high when there is an even number of highs in bits 1 through 7. Received characters are checked for odd parity; that is, the number of highs in

bits 1 through 8 is odd.

In the EVEN position, all characters are transmitted with even parity; that is, bit 8 is set high when there is an odd number of highs in bits 1 through 7. Received characters are checked for even parity; that is, the number of highs in bits 1 through 8 is even.

3.2 THE DISPLAY SCREEN

The display screen is the primary means through which the terminal communicates with you. Data entries into the terminal, regardless of source, will normally be displayed on the screen. Thus, you can proof information entered from the keyboard, read information supplied from an external device, fill in forms, and in general readily converse with other equipment in a data communications system.

3.3 AUDIO INDICATORS

Audio indicators provide a secondary means through which the terminal communicates specific information to you. Two such indicators are built into your 8025 terminal: a "click" sound and a "beep" sound.

3.3.1 The Click Sound

A click tells you that the terminal accepted a key stroke.

3.3.2 The Beep Sound

A beep indicates one of two events: 1) the ASCII code "BEL" was received or 2) the terminal was unable to accept a key stroke. The second event occurs when the terminal is busy or when an unacceptable operation is requested.

3.4 VISUAL INDICATORS

Indicator lights are built into six of the special function keys located in the two top rows of the left-hand key pad. Table 3-1 defines the on-off states for each indicator.

Table 3-1. Visual Indicator On-Off States

INDICATOR	STATE	INDICATION
STORE INPUT	ON OFF	Store input function active Store input function inactive
STORAGE TRANSMIT	ON OFF	Transmit from auxiliary storage function active Transmit from auxiliary storage function inactive
KSR MODE	ON OFF	Terminal in KSR transmission mode Terminal in ASR transmission mode
KEYBOARD DISABLED	ON OFF	Terminal is busy; keyboard entries ignored except certain function keys (see text) Terminal available to keyboard
RECEIVED PARITY ERROR	ON OFF	Parity error detected in received characters No parity error detected
LOCAL COPY	ON OFF	Keyboard entries displayed (half duplex operation) Received data only displayed (full duplex operation)

3.5 BASIC OPERATING MODES

The 8025 CRT terminal has two basic operating modes: KSR and ASR.

3.5.1 KSR Mode

In KSR (keyed send and receive) mode, the terminal operates as a basic character-by-character key entry device. Each character entered on the keyboard is transmitted immediately to the communications line. If the character is displayable, it is also entered onto the screen.

Displayable data received from the communications line is also displayed on the screen and may be intermixed with keyboard-originated data.

Note that data received from the line is checked for parity according to the setting of the parity switch. A (?) parity error character is substituted for any character received with incorrect parity.

3.5.2 ASR Mode

In ASR (automatic send and receive) mode, the terminal operates as a block transmit device. Characters entered on the keyboard are not transmitted to the communications line as entered. Displayable characters are "saved" on the screen and transmitted under control of the FRAME TRANSMIT key (see 3.7.10). Received data is ignored unless STORE INPUT is selected (see 3.7.2).

3.6 KEYBOARD KEYS

Figure 3-1 shows the keyboard arrangement.

3.6.1 Operating Features

Automatic Repeat. This feature causes a character to repeat itself about 15 times per second if the key is held down for more than one-half second. Repetition continues until the key is released.

N-Key Rollover. This feature allows several keys to be struck at the same time without loss of characters or commands. Data entry, however, is in the order of actual key switch closures. (NOTE: It is virtually impossible to strike more than one key so that switch closures will be simultaneous.)

3.6.2 "Typewriter" Keys

This group of keys includes the alphabetical, numerical, punctuation, and symbol keys plus SHIFT/LOCK, Space Bar, TAB, CR (Carriage Return), and LINE FEED. They are arranged as shown in Figure 3-1. Individually they perform many of the same functions as on a typewriter or a teletype machine.

3.6.3 Numeric Pad Keys

Some terminals have a numeric pad, shown in Figure 3-1. These keys duplicate the numerical, comma, and period (decimal point) keys in the "typewriter" grouping. That is, striking a key in the numeric pad has the same effect as striking the corresponding key in the "typewriter" group.

3.6.4 Escape (ESC) and Control (CTRL) Keys

The escape (ESC) and control (CTRL) keys are each used with one or more other keys to initiate functions or characters for which special function keys are not provided.

3.6.5 Cursor Control Keys

The five cursor control keys, labeled with heavy arrows and HOME, control cursor movement. The cursor moves in the direction of the arrows or to its home position (top left corner of screen).

3.6.6 Next Line (↵) Key

This key moves the cursor to the start of the next line, or to the start of the first line if the cursor is in the last line when the key is depressed.

3.6.7 Function Keys and Indicators

The remaining keys are special function keys. They initiate commonly used operations. Some include indicator lights to show terminal status. These keys are identified in Figure 3-1.

3.7 INDIVIDUAL KEY DESCRIPTIONS

3.7.1 Alphanumeric-Punctuation-Symbol Keys

These keys enter the applicable character into the terminal.

3.7.2 STORE INPUT Key/Indicator

Pressing STORE INPUT (shifted or unshifted) to turn the indicator light on activates the store input function and disables the keyboard (KEYBOARD DISABLED indicator on). RESET and STORE INPUT remain enabled. All data received from the host system is placed in the auxiliary storage.

NOTE: It may also be necessary to actuate a control on the storage device being used. For example, a TECHTRAN 4100 series tape cassette drive requires that the WRITE control be pressed to space the tape over the leader when the tape is on clear leader.

If the terminal is in KSR, this data is also displayed on the CRT screen. In ASR mode, the screen is not disturbed.

Pressing STORE INPUT (shifted or unshifted) to turn the indicator off switches the store input function off and enables the keyboard again.

3.7.3 STORAGE TRANSMIT Key/Indicator

Pressing this key (shifted or unshifted) to turn the indicator light on activates the storage transmit function and disables the keyboard (KEYBOARD DISABLED indicator on). RESET and STORAGE TRANSMIT remain enabled. A record in the auxiliary storage is displayed on the screen and also transmitted to the host.

Pressing STORAGE TRANSMIT (shifted or unshifted) to turn the indicator off switches the storage transmit function off and reenables the keyboard. The keyboard is enabled after the last character in the record is transmitted.

3.7.4 KSR MODE Key/Indicator

Pressing KSR MODE (shifted or unshifted) to turn the indicator light on sets the terminal for KSR operation. Data entered from the keyboard is displayed on the screen and transmitted character-by-character to the host. Received data is also displayed. With parity on, a received parity error turns the RECEIVED PARITY ERROR indicator light on. Also, a backward question mark (؟) is displayed on the screen in place of the character.

Pressing KSR MODE (shifted or unshifted) to turn the indicator off sets the terminal to ASR mode.

NOTE: The terminal will enter KSR mode only if a carrier indication is being received from the communications line.

3.7.5 PRINT Key

Pressing PRINT (shifted or unshifted) transfers data on the CRT screen to the printer and disables the keyboard. Data from the cursor home position (upper left corner of screen) to the cursor is printed. If the cursor is in its home position, the entire screen is printed. When the transfer is completed, the keyboard is re-enabled.

3.7.6 STORE Key

Pressing STORE (shifted or unshifted) transfers data on the CRT screen to the auxiliary storage and disables the keyboard. Data from the cursor home position (upper left corner of screen) to the cursor is transferred. If the cursor is in its home position, the entire screen of data is transferred.

NOTE: It may also be necessary to actuate controls on the storage device being used. For example, a TECHTRAN 4100 series tape cassette drive requires that, 1) the WRITE control be pressed to space the tape over the leader when the tape is on clear leader and, 2) the END MODE control be pressed if the drive just completed a read command.

3.7.7 READ Key

Pressing READ (shifted or unshifted) transfers data from the auxiliary storage to the CRT screen and disables the keyboard. Data in storage will be read until a stop read command is transferred or the end of file is encountered on the medium. (The exact sequence depends on the characteristics of the storage device).

NOTE: The host must supply the start and stop commands when data was entered into the auxiliary storage with the STORE INPUT function. Data entry with the STORE key includes terminal-supplied start and stop command.

The keyboard is automatically enabled after the record is transferred.

3.7.8 KEYBOARD DISABLED Indicator

This key position functions only as an indicator. When the light is on, keyboard input is not allowed. Exceptions (explained earlier): RESET, STORE INPUT, and STORAGE TRANSMIT. That is, the terminal will not accept key strokes. The keyboard is enabled when the indicator is off.

3.7.9 RECEIVED PARITY ERROR Indicator

This key position serves only as an indicator, and it operates only if parity is enabled (see paragraph 3.1.4). When the indicator is on, it signifies that a parity error was detected in a received character.

NOTE: A "?" is displayed on the CRT screen in place of the character. The indicator stays on until it is cleared by a reset function as described in paragraph 3.8.2

3.7.10 FRAME TRANSMIT Key

Pressing FRAME TRANSMIT (shifted or unshifted) ASR transmits data on the CRT screen to the host and disables the keyboard. Data from the cursor home position (upper left corner of screen) to the cursor is transmitted. If the cursor is in its home position, the entire screen is transmitted. The keyboard is automatically enabled at the end of transmission.

3.7.11 LOCAL COPY Key/Indicator

This key is used only in KSR mode. The key directs data entries to both the communications system and the display screen when pressed to turn the indicator light on (LOCAL COPY on for half-duplex operation). If the light is off (LOCAL COPY off for full-duplex operation) after pressing the key, data entries are sent only to the communications line.

3.7.12 BREAK Key

Pressing this key places a 200-250 millisecond space on the communications line. This key functions the same as the "interrupt" or "attention" key on other terminals.

3.7.13 RESET Key

This key is used to perform the input-out and master reset operations described in paragraph 3.8.3.

3.7.14 SCREEN ERASE Key

Pressing SCREEN ERASE (shifted or unshifted) clears the entire display screen to nulls and places the cursor at its home position (upper left corner of screen).

3.7.15 Control (CTRL) Key

The CTRL key, when used with an alphanumeric, punctuation or symbol key (shifted or unshifted) initiates function or enters a character, as defined in Table 3-2. The control key must be depressed first and held down while the other key, or keys, are operated.

3.7.16 SHIFT Key

This key shifts from lower case to upper case as on a typewriter. On dual character keys, it shifts from one character to another. Press the key to produce upper case characters.

3.7.17 LOCK Key

This key locks the SHIFT key in the upper case position, as on a typewriter.

3.7.18 Space Bar

The space bar (at the bottom of the keyboard) functions as a typewriter space bar. Striking this key enters a space character into the terminal memory.

3.7.19 TAB Key

Striking TAB transmits an HT character in KSR mode. The display is not changed.

3.7.20 LINE FEED Key

Striking LINE FEED moves the cursor down one line. This is equivalent to a teletype line-feed action. No character is entered into the screen.

3.7.21 Carriage Return (CR) Key

Striking CR moves the cursor to the start of the line in which it resides. This is equivalent to a teletype carriage return action. A carriage return symbol (←) is entered into the screen.

If a CR is followed by a line feed, the line on which the CR was entered is cleared from the character position following the CR to the end of the line. When multiple CRs are entered and followed by a line feed, the line is cleared from the character position following the first CR entered to the end of the line.

3.7.22 Delete (DEL) Key

Striking DEL generates the ASCII seven-bit delete (DEL) character.

3.7.23 Backspace (BS) Key

Striking BS moves the cursor one position to the left and transmits an ASCII backspace to the communications line.

3.7.24 Cursor Control (HOME and Arrow) Keys

Six keys control cursor movement. They are HOME and the 5 keys with arrows.

Striking the HOME key moves the cursor to its home position--the first character space in the upper left corner of the CRT screen.

To move the cursor up, down, left, or right, stroke the applicable "arrow" key. Each time you press the key, the cursor moves one space in the direction you wish--one space horizontally or one line vertically. Should the cursor be at the start of a line, cursor left normally moves the cursor to the end of the preceding line. Striking cursor right when the cursor is at the end of a line normally moves the cursor to the start of the following line.

When the cursor is in its home position, cursor left moves the cursor to the end of the last line. The reverse is true if the cursor is at the end of the last line and you strike cursor right.

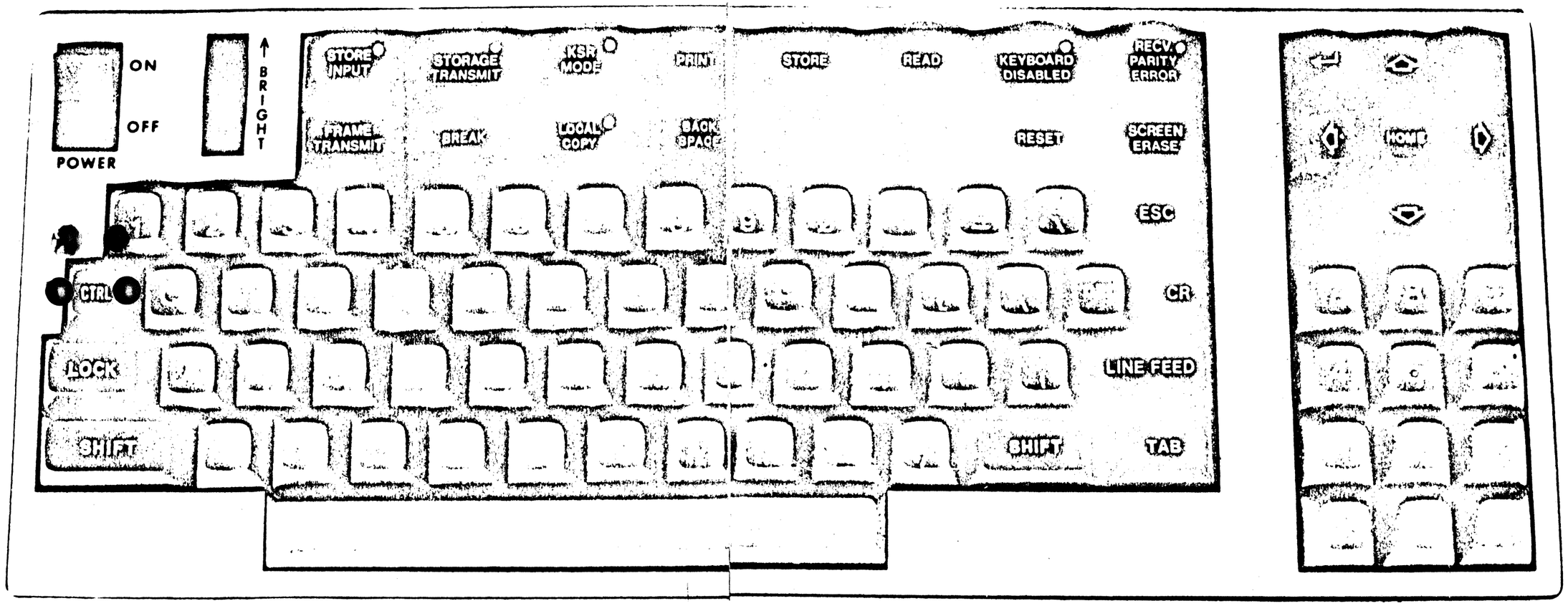


Figure 3-1. CRT terminal keyboard.

If the cursor is on the first line, cursor up moves the cursor to the same position in the last line. Cursor down performs the reverse action if the cursor is in the last line.

Striking the next line key (↵) moves the cursor to the start of the following line. If the cursor is already on the last line, it moves to the HOME position.

3.8 OPERATING PROCEDURES

3.8.1 Turning the Terminal On and Off

Turn the terminal on as follows: 1) Apply power by pressing down on the upper end of the ON-OFF switch, 2) Allow the terminal to warm up for two or three minutes, 3) Hold any character key down, and 4) Adjust the BRIGHTNESS control as desired (raster should not be visible). Table 3-2 tells how to initiate operating functions.

When the terminal is turned on, it automatically sets to ASR mode.

To turn the terminal off, press down on the lower end of the ON-OFF switch. It is not necessary to reduce the brightness. You can leave the terminal on if you wish, but turn the BRIGHTNESS control down (dark screen) to extend CRT life.

3.8.2 Clear/Reset Functions

I/O Reset. Press CTRL and RESET at the same time to stop all input/output (I/O) operations. This action resets all I/O interfaces to off, sets the terminal to ASR mode, and resets the parity error indicator. It does not clear memory.

Master Clear (or Reset). Press CTRL, SHIFT, and RESET at the same time to clear memory, position the cursor at its home position, reset all I/O interfaces, set the terminal to ASR mode, and clear parity error indicator. A master clear is performed automatically whenever the terminal is turned on.

Clear Screen. Strike SCREEN ERASE to clear the memory and place the cursor at its home position.

Table 3-2. Control code generation in the 8025 terminal

ACTION	CODE	SPECIAL FUNCTION KEY	CONTROL SEQUENCE (CTRL plus)
Start of heading	SOH		a
Start of text	STX		b
End of text	ETX		c
End of transmission	EOT		d
Enquiry	ENQ		e
Acknowledge	ACK		f
Bell	BEL		g
Backspace	BS	BS	h
Horizontal tab	HT	TAB	i
Line feed	LF	LINE FEED	j
Vertical tab	VT		k
Form Feed	FF		l
Carriage return	CR	CR	m
Shift out	SO		n
Shift in	SI		o
Data link escape	DLE		p
Device control 1	DC1		q
Device control 2	DC2		r
Device control 3	DC3		s
Device control 4	DC4		t

Table 3-2. Control code generation in the 8025 terminal (contd)

ACTION	CODE	SPECIAL FUNCTION KEY	CONTROL SEQUENCE (CTRL plus)
Negative Acknowledge	NAK		u
Synchronous idle	SYN		v
End of transmission block	ETB		w
Cancel	CAN		x
End of medium	EM		y
Substitute	SUB		z
Delete	DEL		
Escape	ESC	ESC	\
File separator	FS		'
Group separator	GS		{
Record separator	RS		=
Unit separator	US		DEL
Clear screen		SCREEN ERASE	
Master clear[1]			SHIFT+RESET
I/O reset			RESET
Frame transmit		FRAME TRANSMIT	
Next line		↵	
Store Input on		STORE INPUT (light on)	
Storage transmit on		STORAGE TRANSMIT (light on)	

Table 3-2. Control code generation in the 8025 terminal (contd)

ACTION	CODE	SPECIAL FUNCTION KEY	CONTROL SEQUENCE (CTRL plus)
KSR mode on		KSR MODE (light on)	
Print on		PRINT	
Store on		STORE	
Read on		READ	
Local copy on		LOCAL COPY (light on)	
Local copy off		LOCAL COPY (light off)	
Break		BREAK	

4.1 TERMINAL BLOCK DIAGRAM ANALYSIS

A simplified block diagram of the 8025 CRT Terminal is shown in Figure 4-1. Table 4-1 outlines signal sources and their distribution. These signals are defined or described in Section I, as well as at first mention in the text.

The 8025 CRT terminal is built around a central processing unit (CPU) located on the processor card. Data travels between the CPU and the rest of the terminal via three buses: an address bus (MA Data Bus), an input data bus (A Data Bus), and an output data bus (B Data Bus). Timing and control signals are generated and distributed as shown on the block diagram.

4.1.1 Timing, Control, and Data Signals

The basic clock and timing signals for the 8025 CRT Terminal are produced by circuits on the Timing Control Card.

The timing generator produces the clock signals and (T) and also drives another timing circuit which generates the horizontal (H) and vertical (V) timing signals used throughout the terminal as indicated.

V and H signals are also used to produce vertical and horizontal sync (V and H respectively), composite sync (C), and composite blanking (C_B) signals. Both V_S and H_S drive the CRT Display, and V_S is used to reset part of the video counter on the Cursor Control Card. C_S is combined on the Video Control Card with a composite video signal for use by an external display. C_B is used by the Video Control Card to blank out sweep retraces on the CRT display as well as to reset part of the video counter on the Cursor Control Card.

Circuits on the Timing Control Card also decode CPU-generated I/O command signals for distribution to the Cursor Control and RS-232 Interface Cards.

The timing control card also contains the power-on clear (POC) generator. Whenever power is applied to the terminal, this circuit produces a pulse that clears and resets clocks and registers on the processor, refresh buffer, and RS-232 interface cards.

Most operations on the terminal are controlled by the CPU on the Processor Card. Data to and from the CPU travels over the three data buses shown. Outputs from the CPU are decoded in the control logic to provide a number of control signals (PC_L). Another CPU output is combined with a T signal to generate a clock signal (IC CLK) for use by the RS-232 Interface and Refresh Buffer cards.

Programmed read-only memory (PROM) circuits on the PROM Card or marked Read Only Memory (ROM) on the ROM card contain the basic control program for the 8025 CRT terminal. Data is read our of memory to the A Data Bus and the memory is addressed via the MA Data Bus. The address sector circuit allows the card to respond only to a certain range of addresses, while memory circuit selections, as defined by MA inputs, is done by the chip selector.

The Refresh Memory Card contains a number of random access memory (RAM) circuits which temporarily store data from either the CPU or a direct memory access (DMA) device such as a cassette tape deck. The stored data can subsequently be read

out for use by the CRT display or a DMA device. One section of the memory is reserved for specifying special terminal related functions such as cursor position and page base. As shown, data is written into memory via the B Data Bus, and read out through an output gated to the RM Data Channel. A control signal (RC_L) from the Refresh Control Card determines if data is to be read into or out of memory.

The RAM circuits on the Refresh Memory card are addressed via the MA Data Bus. With an address on the MA Data Bus, the address sector circuit puts out a refresh address signal (R_A) which controls the RM gate on the Refresh Buffer Card. The address sector circuit also applies a signal to the chip selector which selects the addressed RAM circuit and enables the data readout gate.

The Refresh Buffer Card has two primary functions: temporary data storage and video refresh. Working with the Refresh Control Card, the Refresh Buffer Card reads data from the Refresh Memory Card one line at a time. It temporarily stores each line of data while transmitting it repeatedly (10 times) to the Video Control Card for display.

The data from the refresh memory, coming in on the RM Data Channel, includes characters to be displayed as well as video modification characters (e.g., turn video on or off). When the latter are detected, a strobe signal to the video status latch causes them to be stored until the end of the current display line.

On/Off data for the keyboard indicator lights are stored in the LED latch and made available to the Keyboard on the LED Data Channel.

Two 80-character shift registers provide refresh data over the CG Data Channel. Data from the refresh memory may be used either by the processor or by the Refresh Memory for screen refresh. In either case control signal RA enables the RM gate to allow passage of data on the RM Data Channel. The half-line gate remains enabled unless the terminal uses a 40-character-per-line display format.

The beep decode circuit on the Refresh Buffer Card decodes MA Data Bus, IC, and I/O inputs to produce a signal that activates the beep portion of the click-beep circuit on the Cursor Control Card.

The Refresh Control Card controls addressing and reading of the refresh memory by the refresh buffer. It contains two counters, one of which controls the addressing while the other counts characters. For each line of characters displayed (10 repetitions), the memory is read 80 times. In addition, the eight fixed positions at the end of memory (addresses 37770_8 - 37777_8) are read during vertical retrace.

The Cursor Control Card includes cursor control, acoustic feedback (click-beep), and keyboard interface circuits.

Cursor control circuitry produces the $\overline{\text{MATCH}}$ signal used by the Video Control Card to create the cursor display. A Video counter, counting in sync with the sweep, defines the current position of the electron beam on the CRT. The cursor position specified by the refresh memory. When the outputs of the two are equal, the comparator sends a $\overline{\text{MATCH}}$ signal to the video modification logic on the Video Control Card, which intensifies the video. The resulting cursor display shows the position of the next character to be displayed.

The keyboard interface controls data transfer from the keyboard to the CPU. To transfer data, the keyboard encoder sends a strobe signal to the keyboard interface, which leads to the following sequence of events. Upon receipt of a POLL I/O command from the CPU, the interface responds with its address over the A Data Bus. When the CPU in turn responds with an I/O command, the interface gates KB Data to the A Data Bus, and signals the encoder that the data was transferred. If a key is depressed for more than one-half second, the interface also signals the encoder to repeat the last character transferred until the key is released.

Each time the keyboard interface transfers KB Data to the A Data Bus, it causes the click/beep circuit to produce an output pulse heard on the keyboard speaker as a click. When the click-beep circuit receives a signal from the beep decode circuit on the Refresh Buffer Card, it produces an output heard on the speaker as a beep.

Circuits on the Video Control Card generate the signals that produce and control the display on both the terminal CRT Display and an optional external display.

Characters stored in the character generator ROM are addressed for display by data from the shift register on the Refresh Buffer Card. The line to be displayed in the character row is specified by the V inputs to the ROM. Parallel data out of the ROM is converted into serial form and gated, under video modification control, to two mixer drivers. In one of these, the video is mixed with the blanking signal (C_B) for use by the CRT display. In the second, the video is mixed with the comp-sync signal (C_S) for use by an external display.

Video modification data from the shift register on the Refresh Buffer Card is stored in the video modification register. The video modification logic decodes the register outputs, video status data on the CS Data channel, and the other input signals shown to produce modification commands. These commands are applied to the video gate to modify the video display as required (e.g., reverse video, underline, etc.).

The Keyboard Card contains an X-Y switch matrix, a shift and control circuit, and an encoder. An X output from the encoder is connected to a Y input to the encoder when a key is depressed. The encoder converts the X-Y coordinates into an ASCII code, which it places on the KB Data Channel. At the same time, the encoder sends a strobe signal to the keyboard interface on the Cursor Control Card to indicate that the keyboard has data for the CPU. After the data is transferred, the interface sends a signal to the encoder to reset the strobe selector and enable the encoder for the next key stroke. Shift and control inputs to the encoder initiate keyboard shift action and control character code generation.

The RS-232 Interface Card provides for compatability between the 8025 Terminal and a data communications system. Parallel data supplied by the CPU via the MA Data Bus is converted into serial form in the receiver-transmitter, and then transmitted, under control of the control logic, to the data communications system (output BA). Incoming serial data (BB) goes through the control logic to the receiver-transmitter where it is converted into parallel form. The control logic enables the received data gate to transfer the data to the A Data Bus for entry into the CPU.

As shown in the block diagram, the control logic also controls: 1) gating of the interface card's address to the A Data Bus; 2) gating of error status, such as parity and overrun, to the A Data Bus; and 3) gating of card and modem status, such as data set ready and transmitter-received status, to the A Data Bus. In addition, the logic control provides the necessary interface for data communications signals such as request to send (CA) and clear to send (CB).

The rate, or speed, of data transmission is set by the clock, which is driven by the T input. Any of five clock frequencies may be selected at the rear panel of the terminal.

The Terminator Card performs two functions: (1) it provides resistive loading and terminations for the data bus and control lines driven by open-collector-drivers, and (2) it selects one of eight addresses at which the processor program restarts after an interrupt.

4.1.2 Typical Operating Sequences

Keyboard Entry. Assume the "A" key on the keyboard is struck. The corresponding X-Y coordinates from the X-Y switch matrix, are decoded by the encoder and converted into the 8-bit ASCII code for an "A". (See Section 10, Reference Information.) After conversion, the character is stored in the encoder's output buffer, while the encoder sends a data strobe output ($\overline{DSO}$) signal to the keyboard interface.

The CPU on the Processor Card periodically sends out an I/O command (POLL) to determine if any peripheral devices require data transfer. When the POLL command arrives at the keyboard interface and the $\overline{DSO}$ signal is present, the interface does three things: (1) prevents further propagation of the POLL, (2) selects itself for the next data transfer to the CPU, and (3) identifies itself by putting the keyboard address on the A Data Bus.

Upon receiving the keyboard address, the CPU responds with another I/O command (IOD), which allows the interface to transfer the keyboard data (character "A") to the A Data Bus and to deselect itself. At the time it transfers the keyboard data, the interface also activates the click-beep circuit to produce an audible click from the keyboard speaker. The IOD command also causes the interface to send an output enable ($\overline{OE}$) signal to the encoder to reset $\overline{DSO}$ and enable the encoder for the next key stroke. At this point all keyboard operations related to the character "A" are finished.

During these keyboard operations, the CPU addresses (over the MA Data Bus) the cursor location in the refresh memory to determine where the next character should appear.

After receiving the cursor position, the CPU processes the information and stores the ASCII-coded "A" at the appropriate address in refresh memory. At the same time, the CPU adds one to the cursor position in the Refresh Memory in readiness for the next character. (Addressing is done via the MA Data Bus; cursor position and the ASCII code for the "A" are entered into memory over the B Data Bus.) The cursor change will automatically update the cursor position register on the Cursor Control Card via the RM Data Channel.

The CPU is now finised with the "A" transfer, and, after performing various

housekeeping tasks, will send out another POLL command.

During display time, the address counter on the Refresh Control Card sequentially scans the refresh memory over the MA Data Bus. When the address for the "A" is reached, the stored ASCII code is read out of memory through the output gate to the Refresh Memory Card. Here the "A" goes through the RM and half-line gates to the shift register for transmission over the CG Data Channel.

Full addressing of the character generator ROM on the Video Control Card includes CG data plus vertical timing signals (V). The former defines the "A"; the latter specifies the scanning line in the character row to be displayed. The character generator ROM decodes the line and character information for the "A" and puts out the data in parallel form.

After conversion in the parallel-to-serial converter, a video signal containing horizontal line segments of an "A" is gated to the video mixer/driver. This circuit combines the video with the composite blanking signal (C_B) for application to the CRT display.

Let's assume now, that instead of an "A" the keyboard character entered is a video modification character specifying reverse video (black characters on a white background).

For a video modification character the operating sequence is the same as that for the "A" with these exceptions: (1) the character leaving the refresh shift register contains information identifying it as a video modification character; (2) the character contains reverse video commands that go to the video modification register on the video control card; (3) outputs from the register are decoded by the video modification logic; and (4) the logic output alters the video signal to display black on white until either the next video modification character arrives or the end of the line is reached.

Finally, let's assume the NEW LINE key is struck. After determining that the character is nondisplayable, the CPU addresses the ROM program via the MA Data Bus and receives program instructions over the A Data Bus. In this case the CPU is instructed to move the cursor position down to the next character row and to the left side of the display. The CPU then updates, via the B Data Bus, the cursor location in the refresh memory's fixed-position address block. The new cursor position will subsequently update the cursor position register on the Cursor Control Card so as to change the cursor position on the CRT screen.

RS-232 Interface Transfers. Data transfer from the RS-232 Interface Card is basically the same as a keyboard entry. In this case, however, data can be transferred in either direction.

Assume the RS-232 Interface Card wants to transfer an "A" from a modem to the CPU for display on the CRT. The "A" received in serial form from the modem on the BB line, is fed to the receiver-transmitter. On the RS-232 Card, the receiver converts the serial data into parallel form and puts the "A" in a local register. When it intercepts a POLL command from the CPU, the interface stops further propagation of the POLL, places its address on the A Data Bus, and selects itself for the next data transfer. An IOD signal from the CPU in response causes the interface to deselect itself and gates the "A" to the A Data Bus for transfer to the CPU. The re

mainder of the operation to display the "A" is identical to a keyboard entry, and the same is true for a non displayable character, received by the RS-232 Interface Card.

Assume now that the CPU wants to send an "A" to the RS-232 Interface Card for transmission. The CPU, under program instruction, puts the card's address on the MA Data Bus and sends a STAT I/O command to enable and set up the card and modem for the transfer. In turn, the card responds to the CPU over the A Data Bus with its status (e.g., receiver ON or OFF; ready for data transfer, etc.). When the transmitter is turned on and its buffer register is empty, it can respond to the next POLL command in the same way as the receiver. Data from the MA Bus enters the buffer register in the transmitter and is shifted out serially. When the serial data transfer is complete, the transmitter will again answer a POLL command. The card can be turned off with a STAT signal if no more data is available for transfer.

4.2 8025 CRT TERMINAL INPUT/OUT STRUCTURE

The 8025 CRT Terminal input/output structure is built around a data bus consisting of 14 memory address lines (MA Data Bus), eight data input lines (A Data Bus), eight data output lines (B data Bus), a priority signal, and a number of timing and control signals.

The terminal card cage has numbered slots for up to 17 cards. The first 7 slots are occupied by basic function cards, with slot 7 being used for the basic processor (CPU). Slot 8 is generally used for the program card, which may be a PROM, ROM, ROM/PROM, or PROM/RAM. For some configurations, the DMA processor must be located next to the CPU, in which case the program card is moved over to slot 9 (the wiring of slots 8 and 9 is the same).

After the program card, the cage accepts either memory or input-output cards in any order or combination. The position of a card relative to the basic processor, however, determines the card's priority for responding to a POLL I/O command. The Terminator Card appears in the last (leftmost) occupied slot of the card cage.

4.2.1 Memory Cards

Memory cards can be of either the ROM (storing programs or data) or RAM read/write variety.

Up to 16,384 bytes of memory can be addressed. Memory can consist of PROM, ROM, or RAM, and includes 1-15 kilobytes of RAM used for video refresh. The display RAM must occupy the highest part of memory and, because of the restart instructions, the program must occupy the lowest part. Since memory is normally packaged with 4,096 bytes per card, a maximum of four memory cards may be installed. The PROM/ROM card can hold up to 4K of ROM and 2K of PROM for a total of 6K.

Each memory card has the most significant two bits of its address wired to the memory-desired sector, and in most cases the ROM card is wired to sector 0 (address 0 - 4096) with additional ROMs

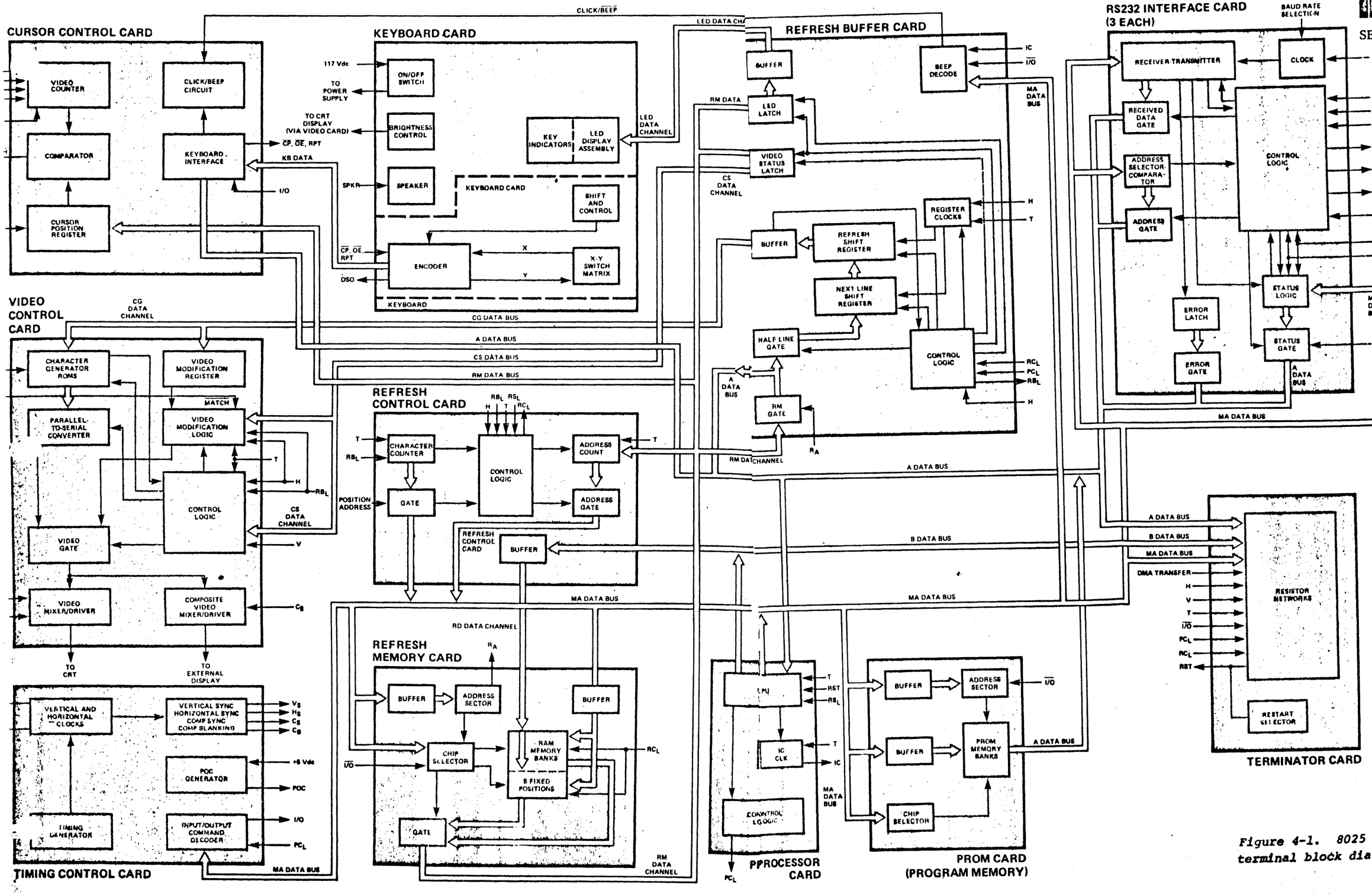


Figure 4-1. 8025 CRT terminal block diagram.

Table 4-1. Sources and distribution of signals in the 8025 CRT Terminal.

SIGNAL SOURCE	SIGNAL USED BY / SIGNAL MNEMONIC	Timing Control	Processor	PROM	Refresh Memory	Refresh Buffer	Refresh Control	Video Control	Cursor Control	Keyboard	RS 232 Interface	Input/Output Bus	Terminator	CRT Display
Timing Control	$\overline{\text{COMP BLNK}}$							X	X					
	CURS LINE							X	X					
	EOP						X							
	EOR					X	X							
	H4					X								
	$\overline{\text{H8}}$					X		X	X					
	$\overline{\text{H10}}$							X						
	$\overline{\text{H20}}$						X							
	$\overline{\text{H40}}$					X	X		X					
	$\overline{\text{H80}}$						X							
	HF CLK							X						
	H SYNC													X
	IOB											X		
	IOD								X		X			
	POC	X				X					X			
	POLL								X		X			
	$\overline{\text{POS TIME}}$					X	X							
	RATE	X				X		X						
	READ CLK		X											
	RS CLK										X			
	$\overline{\text{SET LDFF}}$							X						
	STAT										X			
	$\overline{\text{V1}}$							X						
	$\overline{\text{V2}}$							X						
	$\overline{\text{V4}}$							X						
	$\overline{\text{V8}}$							X	X					

Table 4-1. Sources and distribution of signals in the 8025 CRT Terminal.

SIGNAL SOURCE	SIGNAL USED BY / SIGNAL MNEMONIC	Timing Control	Processor	PROM	Refresh Memory	Refresh Buffer	Refresh Control	Video Control	Cursor Control	Keyboard	RS 232 Interface	Input/Output Bus	Terminator	CRT Display
Timing Control ↓	$\overline{\text{V SYNC}}$								X					X
	Ø1		X				X							
	Ø2		X			X	X							
Processor ↓	BDB0				X		X							
	BDB1				X		X							
	BDB2				X		X							
	BDB3				X		X							
	BDB4				X		X							
	BDB5				X		X							
	BDB6				X		X							
	BDB7				X		X							
	CPU BUSY					X								
	CPU R/$\overline{\text{W}}$						X							
	IC CLK					X					X			
	$\overline{\text{I/O}}$	X		X	X	X								
	MA0			X	X						X			
	MA1			X	X						X			
	MA2			X	X						X			
	MA3			X	X						X			
	MA4			X	X						X			
	MA5			X	X						X			
	MA6			X	X						X			
	MA7			X	X						X			
	MA8	X		X	X									
	MA9	X		X	X	X								
	MA10	X		X	X	X								
	MA11	X		X	X	X								

Table 4-1. Sources and distribution of signals in the 8025 CRT Terminal.

SIGNAL SOURCE	SIGNAL USED BY / SIGNAL MNEMONIC	Timing Control	Processor	PROM	Refresh Memory	Refresh Buffer	Refresh Control	Video Control	Cursor Control	Keyboard	RS 232 Interface	Input/Output Bus	Terminator	CRT Display
Processor	MA12	X		X	X	X								
	MA13	X		X	X	X								
	MA14			X	X									
	MA15			X	X									
	PC6											X		
	PC7											X		
	WAIT	X												
PROM	$\overline{ADB0}$		X											
	$\overline{ADB1}$		X											
	$\overline{ADB2}$		X											
	$\overline{ADB3}$		X											
	$\overline{ADB4}$		X											
	$\overline{ADB5}$		X											
	$\overline{ADB6}$		X											
	$\overline{ADB7}$		X											
Refresh Memory	$\overline{RM0}$					X	X		X					
	$\overline{RM1}$					X	X		X					
	$\overline{RM2}$					X	X		X					
	$\overline{RM3}$					X	X		X					
	$\overline{RM4}$					X	X		X					
	$\overline{RM5}$					X	X		X					
	$\overline{RM6}$					X	X		X					
	$\overline{RM7}$					X	X							
	$\overline{REF\ ADRS}$					X								
Refresh Buffer	$\overline{ADB0}$		X											
	$\overline{ADB1}$		X											
	$\overline{ADB2}$		X											

Table 4-1. Sources and distribution of signals in the 8025 CRT Terminal.

SIGNAL SOURCE	SIGNAL USED BY / SIGNAL MNEMONIC	Timing Control	Processor	PROM	Refresh Memory	Refresh Buffer	Refresh Control	Video Control	Cursor Control	Keyboard	RS 232 Interface	Input/Output Bus	Terminator	CRT Display
Refresh Buffer	$\overline{\text{ADB3}}$		X											
	$\overline{\text{ADB4}}$		X											
	$\overline{\text{ADB5}}$		X											
	$\overline{\text{ADB6}}$		X											
	$\overline{\text{ADB7}}$		X											
	$\overline{\text{BEEP}}$								X					
	$\overline{\text{BLANK}}$							X						
	BLINK							X						
	CG0							X						
	CG1							X						
	CG2							X						
	CG3							X						
	CG4							X						
	CG5							X						
	CG6							X						
	CG7							X						
	$\overline{\text{CLRF}}$							X						
	$\overline{\text{CS0}}$							X						
	$\overline{\text{CS1}}$							X						
	$\overline{\text{CS2}}$							X						
	$\overline{\text{CS3}}$						X							
	$\overline{\text{EXT ADRS}}$		X											
	$\overline{\text{INHLD}}$							X						
	$\overline{\text{LCLSB}}$								X					
	$\overline{\text{LCMSB}}$								X					
	LITE 1									X				
	LITE 2									X				
	LITE 5									X				

Table 4-1. Sources and distribution of signals in the 8025 CRT Terminal.

SIGNAL SOURCE	SIGNAL USED BY / SIGNAL MNEMONIC	Timing Control	Processor	PROM	Refresh Memory	Refresh Buffer	Refresh Control	Video Control	Cursor Control	Keyboard	RS 232 Interface	Input/Output Bus	Terminator	CRT Display
Refresh Buffer	LITE 10									X				
	LITE 11									X				
	LITE 12									X				
	LOAD "F"							X						
	SR COUNT						X							
Refresh Control	CNT 80					X								
	MA0				X									
	MA1				X									
	MA2				X									
	MA3				X									
	MA4				X									
	MA5				X									
	MA6				X									
	MA7				X									
	MA8				X									
	MA9				X									
	MA10				X									
	MA11				X									
	MA12				X									
	MA13				X									
	REF R/$\overline{W}$				X									
	$\overline{RD0}$				X									
	$\overline{RD1}$				X									
	$\overline{RD2}$				X									
	$\overline{RD3}$				X									
	$\overline{RD4}$				X									
	$\overline{RD5}$				X									
	$\overline{RD6}$				X									

Table 4-1. Sources and distribution of signals in the 8025 CRT Terminal.

SIGNAL SOURCE	SIGNAL USED BY / SIGNAL MNEMONIC	Timing Control	Processor	PROM	Refresh Memory	Refresh Buffer	Refresh Control	Video Control	Cursor Control	Keyboard	RS 232 Interface	Input/Output Bus	Terminator	CRT Display
Refresh Control ↓	$\overline{RD7}$				X									
	SRINH					X								
	$\overline{UPDATE}$					X								
Video Control	VIDEO													X
Cursor Control ↓	$\overline{ADB0}$		X											
	$\overline{ADB1}$		X											
	$\overline{ADB2}$		X											
	$\overline{ADB3}$		X											
	$\overline{ADB4}$		X											
	$\overline{ADB5}$		X											
	$\overline{ADB6}$		X											
	$\overline{ADB7}$		X											
	$\overline{CP}$									X				
	MATCH							X						
	$\overline{OE}$									X				
	POLL										X			
	RPT									X				
	SPKR									X				
Keyboard ↓	$\overline{DSO}$								X					
	KDB0								X					
	KDB1								X					
	KDB2								X					
	KDB3								X					
	KDB4								X					
	KDB5								X					
	KDB6								X					
	KDB7								X					

Table 4-1. Sources and distribution of signals in the 8025 CRT Terminal.

SIGNAL SOURCE	SIGNAL MNEMONIC / SIGNAL USED BY	Timing Control	Processor	PROM	Refresh Memory	Refresh Buffer	Refresh Control	Video Control	Cursor Control	Keyboard	RS 232 Interface	Input/Output Bus	Terminator	CRT Display
Regulator	+5 V (Reg.)	X	X	X	X	X	X	X	X	X	X			
	+12 V (Reg.)					X		X	X					
	-12 V (Reg.)		X					X	X	X	X			
Power Supply	+80 V (Unreg.)													X
	6.3 VAC													X
RS-232 Interface	$\overline{ADB0}$		X											
	$\overline{ADB1}$		X											
	$\overline{ADB2}$		X											
	$\overline{ADB3}$		X											
	$\overline{ADB4}$		X											
	$\overline{ADB5}$		X											
	$\overline{ADB6}$		X											
	$\overline{ADB7}$		X											
	BA, CA, CD	Used By Modem												
	POLL	Propagated On To Following I/O Interfaces												
Terminator	$\overline{RST0}$		X											
	$\overline{RST1}$		X											
	$\overline{RST2}$		X											

4.2.2 Program-Processor Controlled I/O Cards

The RS-232 Interface Card is an example of a program-processor controlled I/O card. This type of I/O card transfers data to and from the CPU one character at a time. The transfer is performed under program control of the CPU.

Four types of I/O commands are used in the transfer: POLL, IOD, IOB, and STAT (status). POLL, IOD, and IOB are general commands; STAT is a specific command. These commands are summarized as follows:

POLL (Produced by INP 0 within CPU). The POLL command is used to determine if any device on the data bus has data to be transferred in either direction. As the command travels down the bus from the CPU, it passes through each of the interface cards in turn. The first device along the way which is ready for data transfer in effect selects itself by inhibiting further travel of the command. The selected device returns its address (in the lower-order five bits of eight bit bytes) to the CPU's register. The higher-order three bits sent to the CPU contains device status information which varies with the device. If no device requires service, the CPU receives an address of zero.

When a non-zero address appears, the processor determines what kind of I/O device requires service and responds with an appropriate set of commands. For the actual data transfer, in either direction, the processor sends an IOB or IOD command to the interface. Output data is placed in the CPU's A register prior to IOD or IOB, while input data appears in the register upon completion of IOD or IOB.

IOD (Produced by INP 1 within CPU). With the IOD command the contents of the CPU's A register becomes available to the device and the device may specify the new contents of the register. IOD also causes the device to deselect itself. Every POLL is followed in succession by an IOD to prevent system lock up; that is, only one device at a time can be selected.

IOB (Produced by INP 3 within CPU). The IOB command is essentially the same as the IOD except that IOB does not cause the card to deselect itself. Deselection is accomplished with an IOD or STATUS command.

STATUS (Produced by INP within CPU). With the STATUS command the five lower-order bits of the CPU's A register are interpreted as a device address. The three higher-order bits of the register are interpreted as status bits to be written into the device's status register. Typically these bits are: on/off device, on/off POLL response, and disable writing of the first two bits. The CPU's A register is respecified as the current contents of the addressed device's status register. At least three of the eight status register bits will be: on/off device, on/off POLL response, and device ready regardless of on/off status.

In general, the three bits of status included in a device's response to a POLL will also be included in its response to a STATUS.

4.2.3 DMA Transfer I/O Cards

DMA (direct memory access) transfer I/O cards work with a DMA Processor Card to transfer data between the Refresh Memory and high-speed, block-oriented devices. Examples of such devices include tape cassette drives and line printers. DMA transfers can move data from or to memory at rates up to 600,000 bytes per second

without Processor Card Control.

The CPU sets up a DMA transfer by sending the I/O card a status command and control information. Once the operation is set up, the DMA Processor and I/O cards assume full control of addressing and other data transfer functions, including the control of bus priority. The data bus is available for DMA transfers whenever the Processor Card does not need it (approximately 80% of the time during normal operation).

In general, DMA operations transfer memory data in blocks. The starting address and number of words in the block are sent to the DMA processor via a normal program-processor data transfer. Once this information is in the DMA Processor, the transfer can begin and is then transferred sequentially, beginning with the starting address. The address is incremented (or decremented) for each transfer until the number of transfers defined by the block length is completed. When the transfer is complete the I/O card becomes ready. That is, it will answer a POLL command and either be turned off to wait for more data or reset to transfer a new block of data.

4.3 CHARACTER GENERATION

An understanding of how characters are formed on the 8025 CRT screen will help in following the card descriptions presented later in this section.

The CRT screen can be thought of as a large matrix of small light elements, or dots, that can be turned on and off. In this context the overall video presentation is made up of light and dark dots.

The basic display format for the 8025 Terminal is 80 characters per line with a maximum of 24 lines per frame (page). Thus, up to 1920 characters can be displayed per page. Some terminals are configured for a 12 line page format with a maximum of 960 displayed characters per page.

A 10 x 10 dot area on the screen is allotted for each character displayed. Consequently, each row of characters consisting of eighty 10 x 10 dot areas, requires ten horizontal scan lines.

To provide for both character and row spacing, only nine dot lines (L) and seven dot columns (C) are allotted for character generation. Only seven of the dot lines, however, are displayable.

In addition, a half-dot horizontal shift feature creates an effective 7 x 14 (L x C) dot area for character generation. The function of this shift feature is explained in Section 4.3.1.

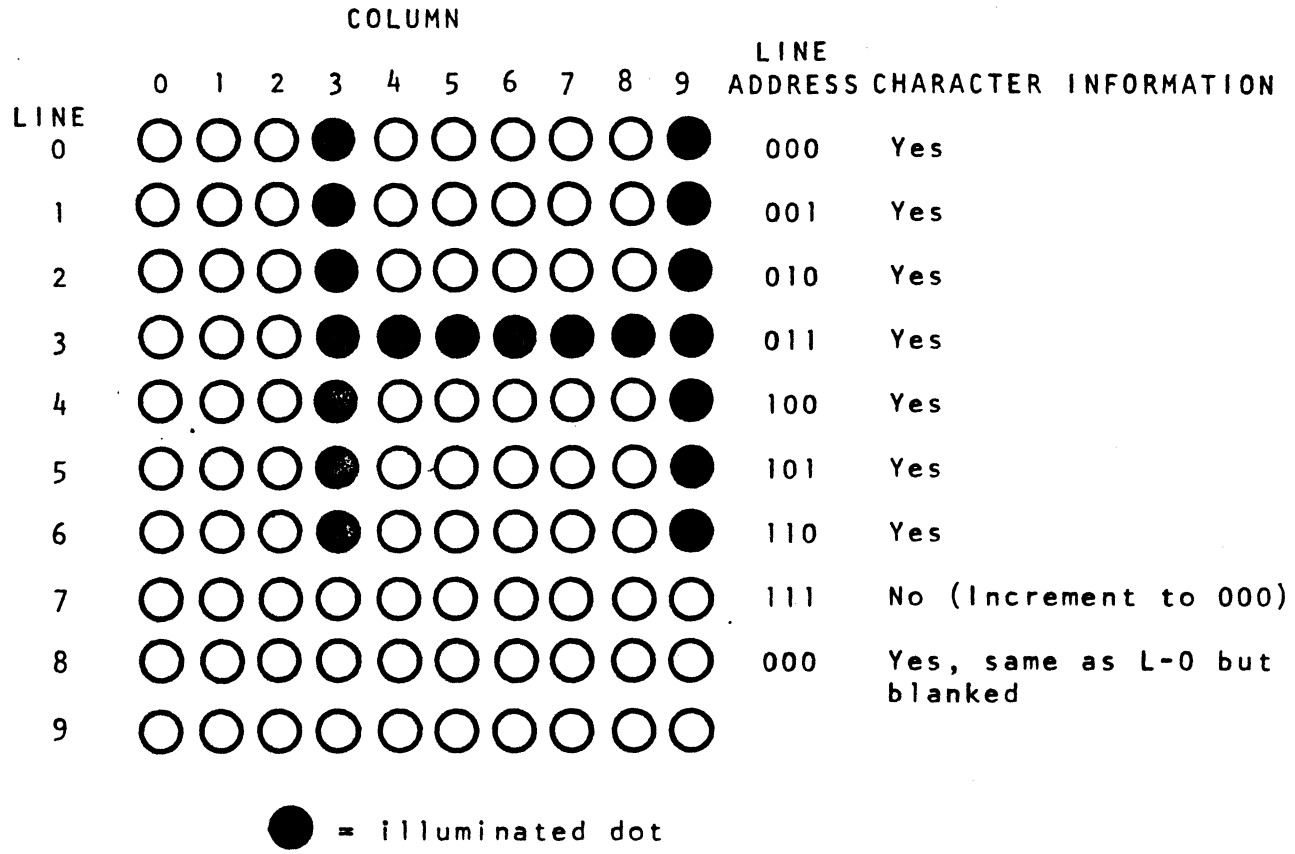
The eighth dot in each scan line is not displayed. It is used as a control dot, as explained in Section 4.3.2.

4.3.1 Upper Case Characters

B, D, E, F, H, I, K, L, M, N, P, R, T, W, X, and Z. In Figure 4-2, "H" is used as an example of how characters in this group are formed. As stated earlier, nine lines are allotted for each character, with only seven lines being displayable.

Hence, the character generator must be addressed nine times to complete a character. A three-bit octal code is used for line addressing (000 through 111), which provides eight lines. The ninth line is obtained by incrementing the eighth-line address back to the first line (000).

As shown in Figure 4-2, dot formation (C-3 through C-9) for producing the "H" is contained in the character generator for the first seven lines (L-0 through L-6, address 000 through 110). No dot information is contained in the eighth line (L-7, address 111), and no dots ever exist in C-0 through C-2. Incrementing L-7 back to L-0 makes the ninth line (L-8) dot information identical to L-0. For this group of characters, however, L-8 dot information is blanked out and does not appear on the CRT screen.



LINE ADDRESS	CHARACTER INFORMATION
000	Yes
001	Yes
010	Yes
011	Yes
100	Yes
101	Yes
110	Yes
111	No (Increment to 000)
000	Yes, same as L-0 but blanked

Figure 4-2. Example of upper case character (H).

A, C, G, J, O, Q, S, U, V, and Y. In Figure 4-3 "V" is used as an example of how characters in this group are formed. The basic operations for creating the other upper case characters also apply to this group. But in this group a non-displayable control dot can exist in C-2, L-1 through L-6.

As shown in Figure 4-3, whenever a control dot is present in a line, (L-1, L-2, and L-5), that line is shifted one-half dot position to the right. (Note that a control dot is never used in L-0 for this group of characters.) This feature makes the characters displayed in this group more natural looking by creating an effective 7 x 14 dot area in an actual 7 x 7 dot area.

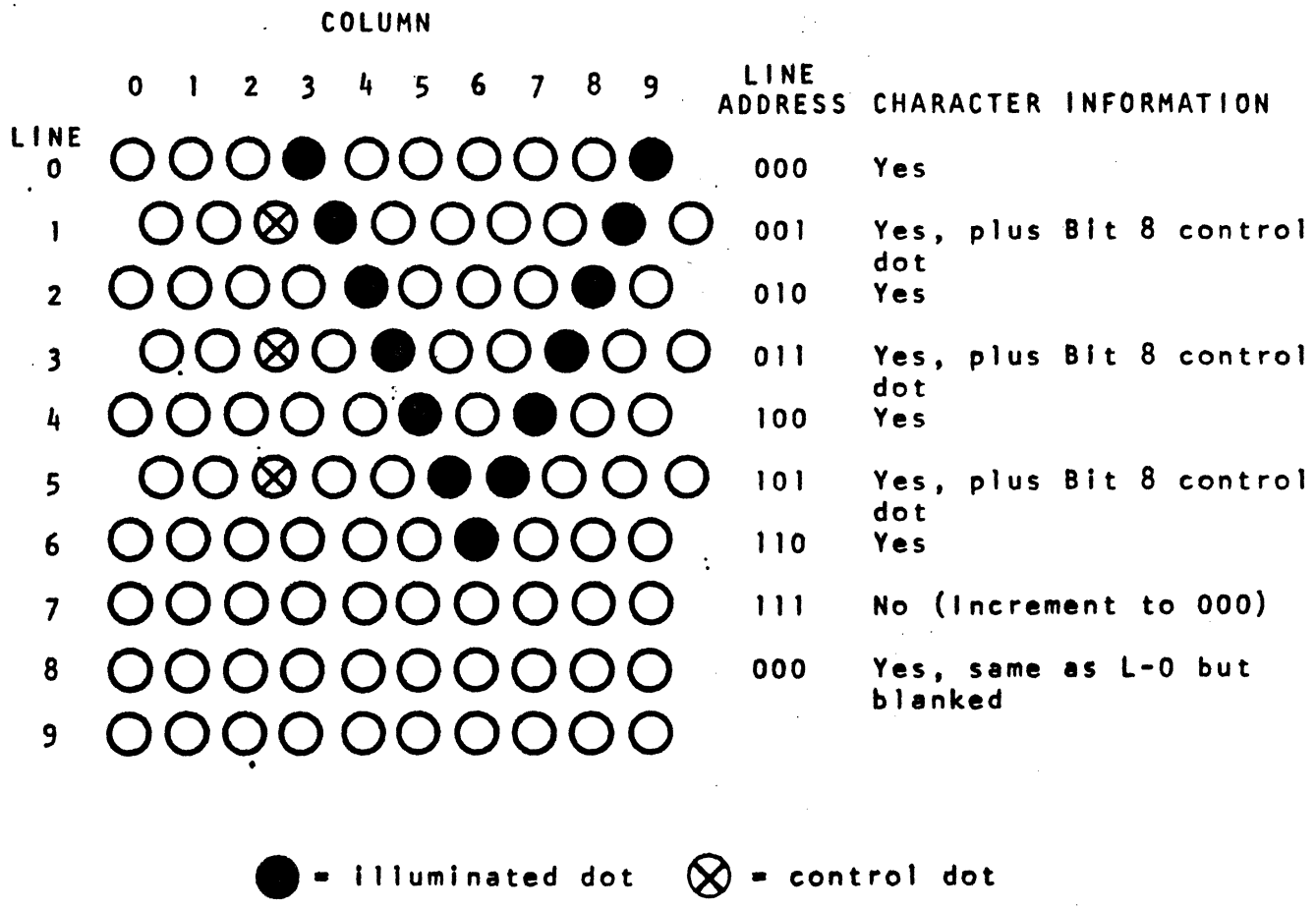


Figure 4-3. Example of upper case character (V).

4.3.2 Lower Case Characters

Characters Without Descenders. As shown in Figure 4-4, lower case characters without descenders (e.g., "h") are formed in the same way as the first group of upper case characters (B, D, E, etc.) discussed in Section 4.3.1.

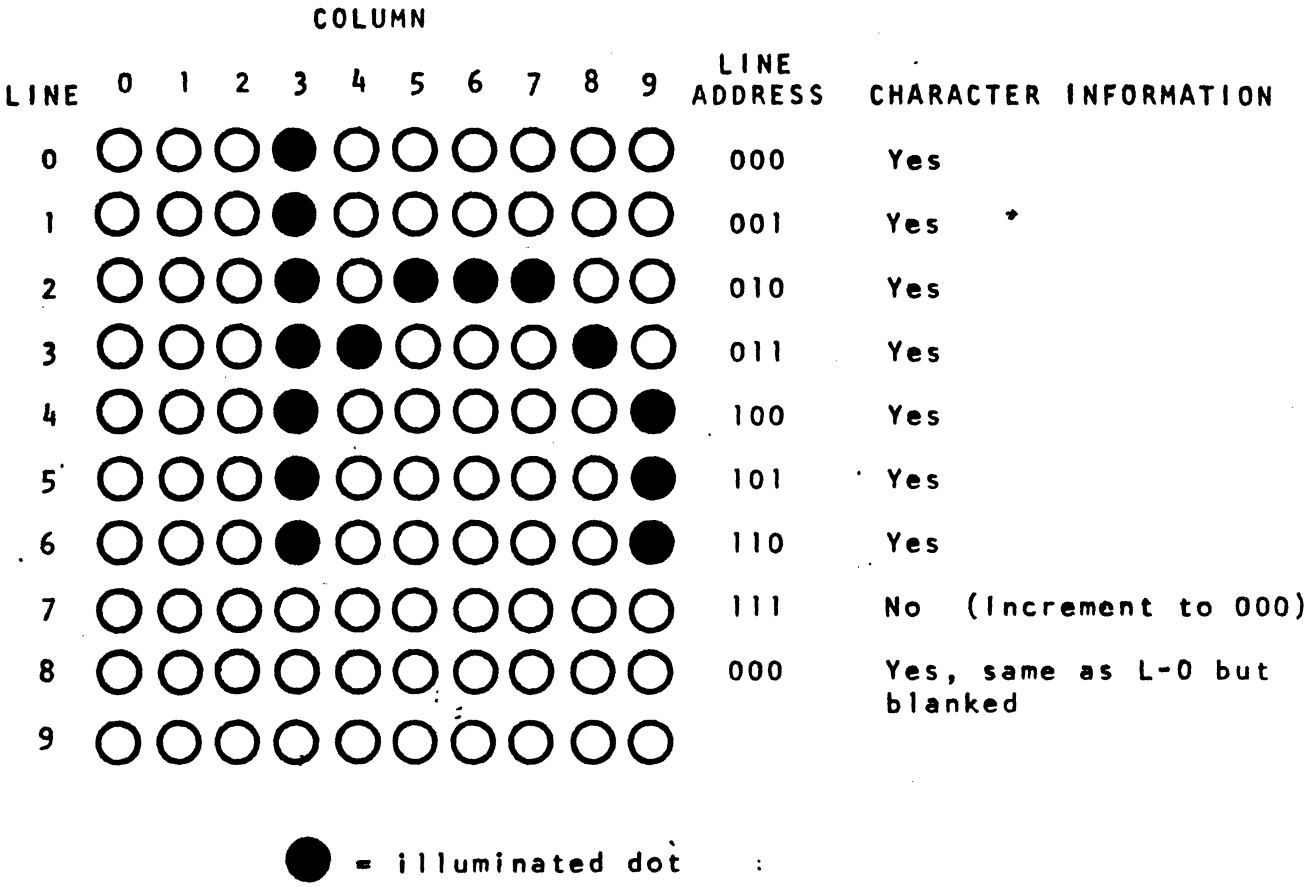


Figure 4-4. Example of lower case character (h).

Characters With Descenders (g, j, p, q, and y). Using "p" as an example, Figure 4-5 shows how lower-case characters with descenders are formed. Again, the same basic operations as for the other lower-case characters apply. For this group, however, a control dot in C-2, L-0, in addition to producing the half-dot shift, indicates that dot formation in L-0 will be used in the ninth line (L-8) of the display. That is, when L-7 (111) is incremented to L-8 (000), the dot information in L-0 will not be blanked out as it would for lower-case characters without descenders. Note that, since the control dot in C-2, L-0 produces the half-dot shift, all other scan lines in the character must also be shifted if the character has a vertical straight line.

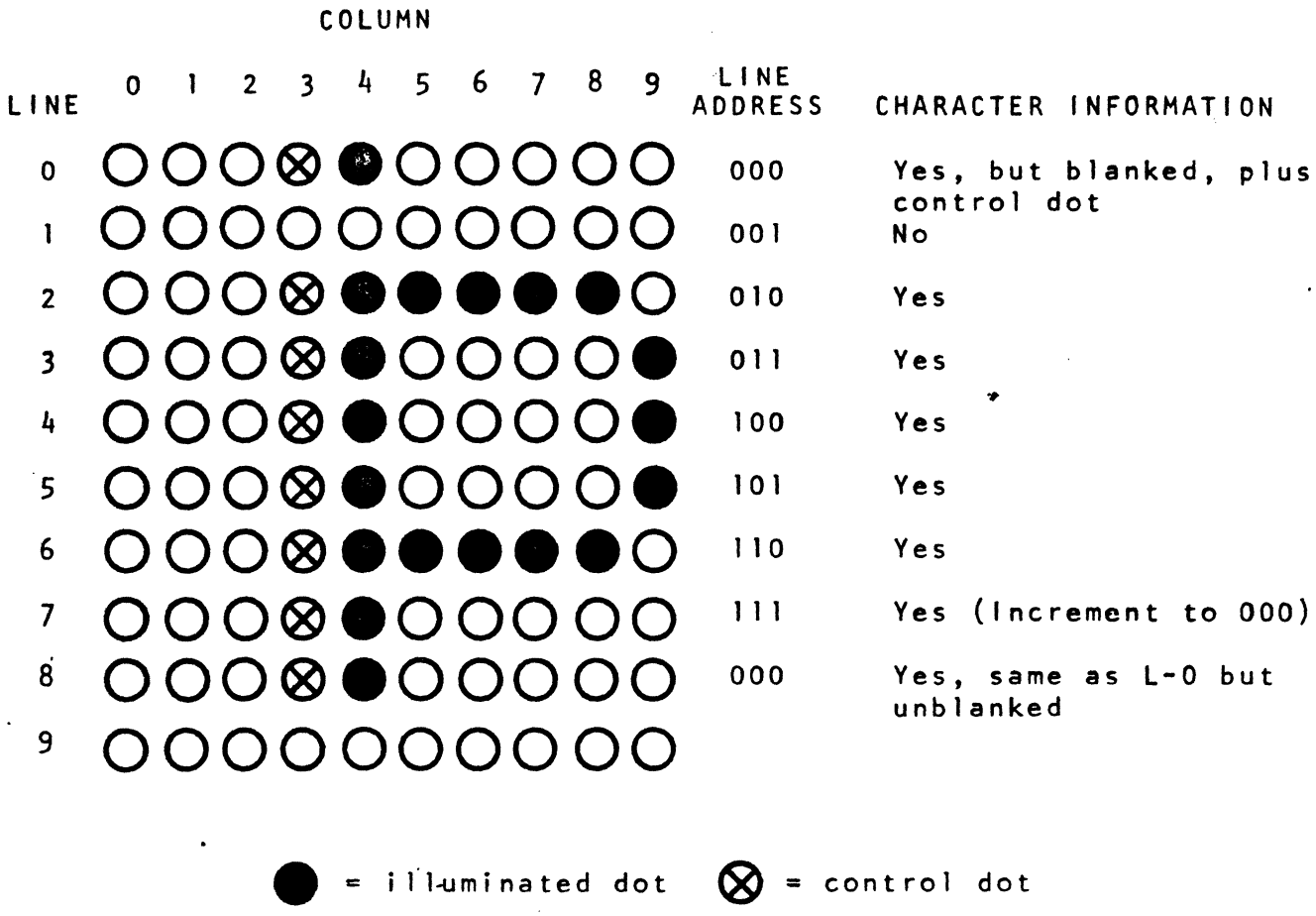


Figure 4-5. Example of lower case character (p).

4.4 CARD/SECTION DESCRIPTIONS

4.4.1 Power Supply

Except for the dc voltages used in the CRT Display, the Power Supply provides all voltages required by the 8025 CRT Terminal.

Block Diagram Analysis. As shown by the simplified block diagram in Figure 4-6, the Power Supply consists of a power supply assembly and a regulator card.

The rectified output voltage of T1 is applied to the 5-volt regulator, which

maintains a constant 5 V dc output with the aid of the current shunt transistor.

Regulated ±12 V dc outputs are produced by T2, a bridge rectifier, and two voltage regulators. Another section of T2 supplies a 6.3 V ac output as well as the input voltage to another bridge rectfier that provides an unregulated 80 V dc.

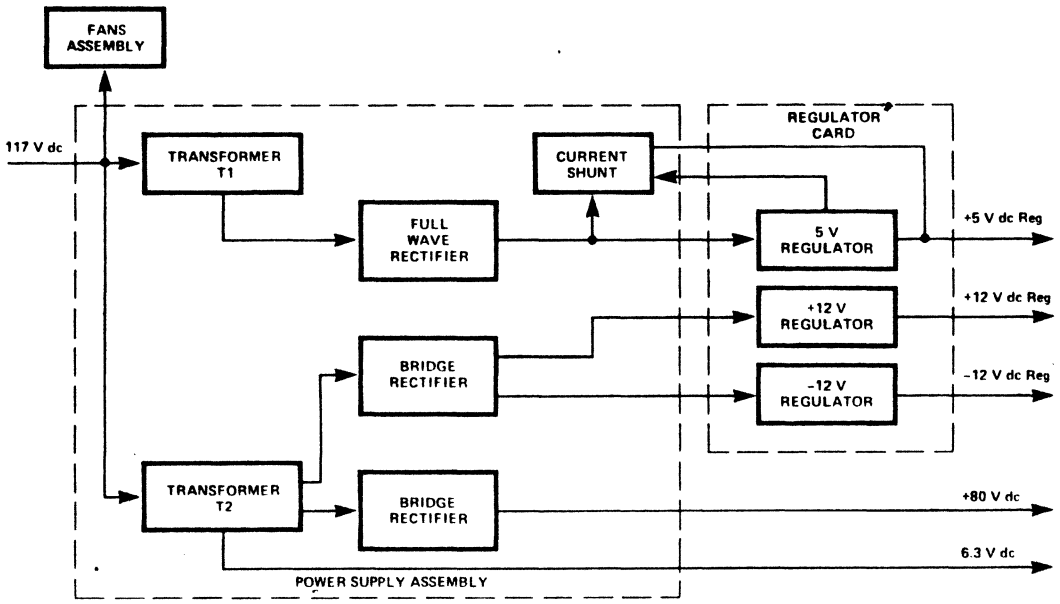


Figure 4-6. Power supply block diagram.

Circuit Description. Refer to schematic diagrams in Section 8.

With the terminal on/off switch closed, primary power is applied through fuse F201 to the fans assembly and to the primary windings of step-down transformer T2. Power is also applied via fuse F202 to the primary of step-down transformer T1.

One secondary winding (10, 11) of T2 supplies 6.3 V ac for the display CRT filament via J61-3,4. The 80 V dc output for the 8025 CRT Display is derived from the voltage across another secondary winding (8, 9) of T2. This voltage is rectified by bridge rectifier (CR4) and filtered by C4.

Bridge rectifier CR3, connected across the third secondary winding (12, 14) of T2, is the source for the +12 and -12 V dc supplies.

The positive output of CR3, filtered by C3, is fed to the regulator assembly via J6-5 and motherboard lines 53-56. The negative output is filtered by C2 and applied to J62-4 and motherboard lines 17-20. Two IC voltage regulators, Z2 and Z3, provide regulated -12 V dc and +12 V dc, respectively. Capacitors C7 and C8 provide additional filtering. Output bypass capacitors, C10 and C11, improve response time by attenuating transients.

The voltage across the secondary of T1 is rectified by full-wave rectifier CR1 and CR2, filtered by C1, and applied to J63-1,2,3, and motherboard lines 59-62.

The voltage on lines 59-62 is applied to IC voltage regulator Z1, which maintains a constant voltage on motherboard lines 71-80, and 65-66 at currents below 700 milliamps. The level of this output is set by R4 while C6 provides additional filtering of the input to Z1 and C9 improves transient response. The voltage drop across R1 controls the current through Q1.

4.4.2 CRT Display

The CRT Display in the terminal is basically a 15 - inch television monitor. It provides visual readout of input data from the keyboard or from external devices.

Block Diagram Analysis. As shown by the simplified block diagram in Figure 4-7; the CRT Display is made up of four major sections: video, vertical sweep, horizontal sweep, and low-voltage regulator.

An adjustable closed-loop voltage regulator provides a constant output to all stages in the CRT Display. The X-ray protection circuit prevents any X-radiation due to line voltage surges or regulator failure. Under those conditions, the circuit disables the horizontal drive multi-vibrator.

Video inputs are amplified and inverted by the video amplifier driver. The video amplifier output is coupled directly to the video output stage, which provides a low-impedance source for driving the cathode of the CRT.

The vertical oscillator is a relaxation oscillator synchronized to the vertical interval which is set by the vertical drive input. A sawtooth output from the oscillator is directly coupled to a driver amplifier, the output of which is applied to the vertical output. The vertical output in turn is transformer coupled to the yoke.

Horizontal drive pulses, after being delayed by an adjustable delay circuit, are applied to the horizontal drive one-shot. This delay compensates for inherent deflection-circuit delays. The output of the one-shot is coupled to the horizontal output stage, which supplies the correct horizontal scanning currents and the high-voltage pulses for the high-voltage supply.

Circuit Description. Refer to schematic diagram 95-146-02 in Section 8 and to the voltage waveforms shown in Figure 4-8.

The video section consists of Q103 and Q104 with their associated circuitry.

The video amplifier consists of Q102 and its associated circuitry. The incoming video signal (typically 4 V P-P) is applied to the base of Q103. The gain of this stage can be varied from 12 to 25 with R119, the video gain adjustment. Q103 operates as a class B amplifier and remains cut off until a dc-coupled, positive-going signal arrives at its base and turns the transistor on. R118 and R119 add series feedback to make the voltage gain relatively independent of transistor variations. This feedback also stabilizes against voltage and current changes caused by ambient temperature variations.

The negative-going signal at the collector of Q103 is dc coupled to the base of Q104, the video output. Q104 is an emitter follower that supplies a low source impedance for driving the cathode of the CRT. Class-B biasing of the video output allows a maximum available contrast ratio by providing a large video output signal to modulate the CRT cathode. Typically a video output of about 25 V P-P is required for optimum contrast.

Overall brightness of the display is determined by the negative potential at the grid of V1. The normal adjustment range of CRT grid voltage is from +10 to -100 V dc. This voltage is set with the brightness control located on the terminal keyboard.

The vertical sweep section is made up of Q101, Q102, and Q122.

Q101, a programmable unijunction transistor, with its associated circuitry forms a relaxation oscillator operating at the vertical sweep rate. Timing is determined by RC network R106-108, C103, and C104. When power is applied, C103 and C104 charge toward +55 V dc through R106 and R107. The charging rate is set by the time constant of the network. Capacitors C103 and C104 continue charging until the anode voltage of Q101 is within 0.6 V of the gate voltage. When this occurs, Q101 fires, and C103 and C104 rapidly discharge through Q101 and L101 to near ground. Q101 then turns off and allows C103 and C104 to recharge to the firing potential.

The gate threshold voltage for Q101 is developed across R105, the level being established by the network R103, CR101, CR102, and R105. This voltage, variable with the vertical hold control (R103), is typically 4.6 V. Thus C103 and C104 must charge to approximately 4 V before Q101 fires.

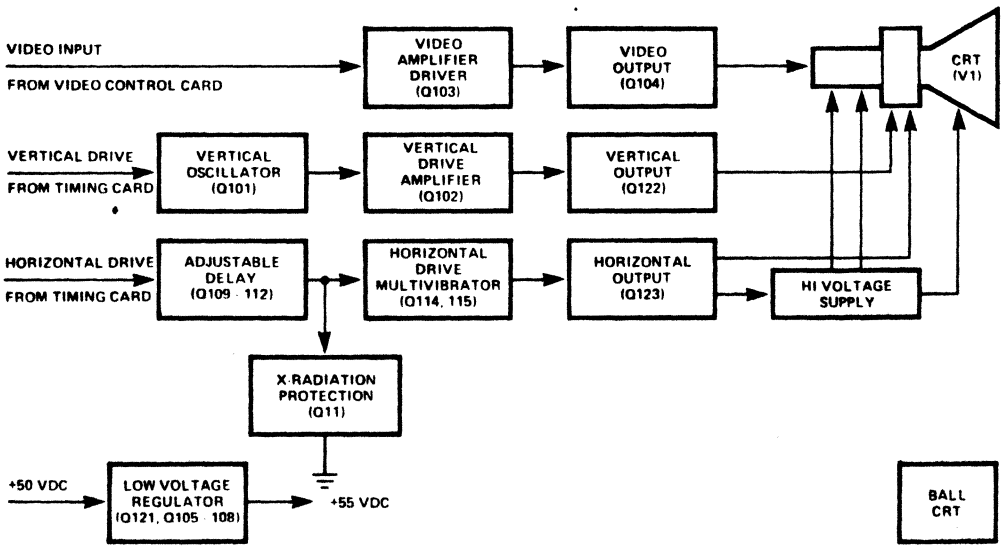


Figure 4-7. CRT display block diagram.

Q101 can also be fired by rapidly lowering the gate voltage to within 0.6 V of the anode voltage. This is done by applying a negative synchronization pulse through R101, C101, CR101, and CR102 to reduce or stop current flow through R105. When a synchronization pulse is applied, the voltage across R105 instantly drops one or two volts below the gate threshold potential. Such a drop at the gate of Q101 causes it to fire, providing the timing network has charged to about 4 volts.

In summary, Q101 can be fired by (1) allowing the anode voltage to rise within 0.6 V of the gate potential, or (2) rapidly lowering the gate potential to within 0.6 V of the anode voltage. Without vertical synchronization pulses, Q101 oscillates by anode voltage changes. With vertical synchronization it is operated by gate voltage changes.

The amplitude of the sawtooth waveform developed at the anode of Q101 is determined by C102, R106, and R107. R107, the height adjustment, varies the RC time constant and, in consequence, the voltage applied to the oscillator circuit. This voltage, developed across C102, is typically 14 V. The sawtooth output at the anode of Q101 is directly coupled to the base of vertical drive amplifier Q102.

Because the slope and linearity of the sawtooth input to Q102 would produce a distorted vertical sweep, wave-shaping is needed. Capacitors C103 and C104 improve linearity, and the slope is modified as follows: The sawtooth output of Q102 is fed back to C104, through R110 and R109. Capacitor C104 shapes this feedback into a parabola and adds it to the input of Q102 to change the slope. Potentiometer R109, the vertical linearity adjustment, determines the slope change rate. Consequently, emitter follower Q102 supplies a suitable sawtooth waveform of about 5 V amplitude to the base of Q122.

The vertical output stage, Q122, operates as a class-B amplifier with output transformer-coupled to provide a proper impedance match with the yoke (L124). During retrace time, a large positive pulse (typically 300 V) is developed across T102. This pulse reverses the current through the yoke and moves the beam from the bottom of the screen to the top. Resistor R121 prevents oscillations by providing damping across the vertical deflection coils. Network CR103, C107, and R113 keeps the collector voltage of Q122 at safe levels during retrace.

The horizontal sweep section consists of Q109 through Q115 and Q123.

The horizontal output transistor, Q123, has a storage period of several microseconds. To compensate for this period, a drive pulse that occurs a few microseconds before flyback is needed. Such a pulse is obtained by delaying the synchronization input nearly one full horizontal sweep. This delay effectively provides a few microseconds lead time for the drive pulse. The circuits that provide the delay are one-shot Q109, Q111 and amplifier, Q112.

The positive horizontal sync input signal is differentiated by R140, C115, and R137 so that the positive-going edge of the signal triggers Q110 on. The resulting negative pulse at the collector of Q110 triggers the one-shot (Q109, Q111), and the collectors of Q111 and Q109 go low and high, respectively. After one-half horizontal line, the one-shot returns to its stable state (collectors of Q111 and Q109 high and low respectively). This change generates a negative gate, which is applied through C117 to the base of Q112. Transistor Q112 in turn generates a 15 V positive gate at its collector. After one-third line, C117 discharges through R144

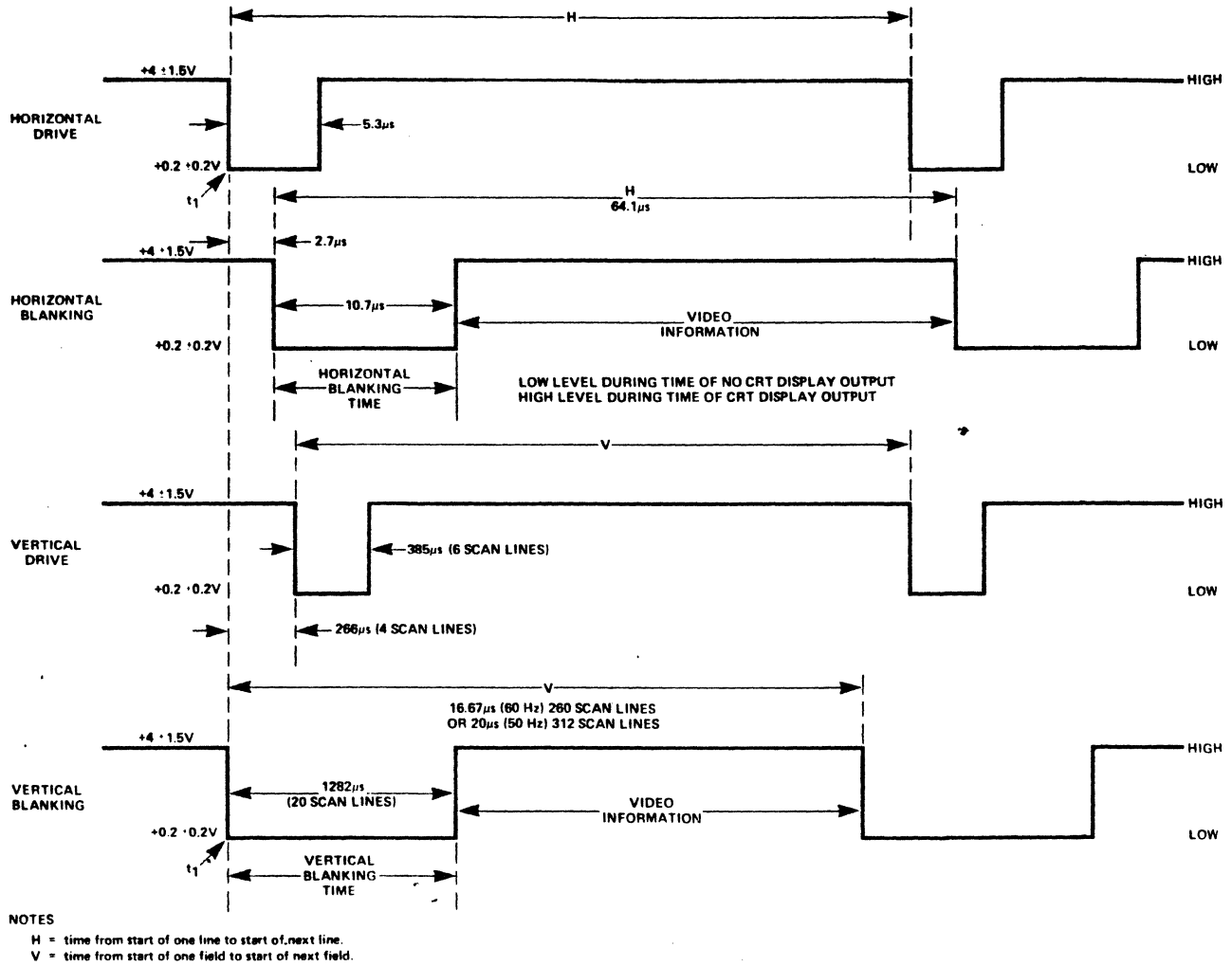


Figure 4-8. CRT waveforms.

and R143 to terminate the positive gate at the collector of Q112. Horizontal centering adjustment R143 varies the one-third line delay by changing the time constant of the C117 discharge path. The trailing edge of the positive gate is differentiated by C121 and R153 to trigger the horizontal drive one-shot (Q114, Q115).

In the stable state of the horizontal drive one-shot, Q114 is held at saturation (low state) by virtue of the base current flowing through R152 and CR109. Consequently Q115 is at cutoff (high state). When the negative-going differentiated pulse from Q112 is applied to the base of Q114, Q114 is driven to cutoff to produce a positive pulse at the base of Q115. Q115 then becomes saturated (low state). The resulting negative feedback through R157, R156, C122, and CR109 to the base of Q114 holds that transistor at cutoff. After approximately one-half line, C122 discharges through R152, causing Q114 to conduct (low state). Transistor Q115, consequently, is cut off to produce a 100-volt gate at its collector with an additional 100-volt transient at the leading edge. This positive gate is clipped and limited to approximately 55 V by R157 and CR110 and reduced to approximately 25 V by divider network R156 and R155. Feedback through C122 initiates regeneration and holds Q114 in conduction until the next trigger pulse arrives.

The phasing and turns ratio of transformer T101 are such that a negative 100-volt gate at the collector of Q115 creates a negative gate of several volts at the base of the horizontal output transistor (Q123).

When Q115 conducts, energy is stored in T101 and the voltage at the secondary is negative, so that Q123 is cut off. When the primary current of T101 is interrupted by collector cutoff of Q115, the secondary voltage of T101 reverses polarity, causing Q123 to start conducting. The collector current of Q123 slowly increases a sawtooth pattern during the remaining period of the horizontal line scan. Although Q123 will be at collector saturation, current flow is determined by the collector load (yoke inductance and flyback transformer). Typically the peak sawtooth current through Q123 is 2 to 3 amperes, depending upon line rate and length of the horizontal sweep.

The horizontal output stage has three main functions: (1) supply the yoke (L101) with the correct horizontal scanning currents, (2) develop 17 kV dc for the CRT anode, and (3) develop +800 V dc and -100 V dc for the CRT bias.

Transistor Q123 acts as a switch that is turned on or off by the rectangular waveform on its base. When Q123 is turned on, the supply voltage plus the charge on C135 causes L124 current to increase in a linear manner to move the beam from near center screen to the right side. At this time, Q123 is turned off by a negative voltage on its base, which causes the output circuit to complete one-half cycle of sine-wave oscillation. A positive flyback voltage pulse--several microseconds in duration, several hundred volts in amplitude, and in the form of a half-cycle sine wave--is developed by the combined inductance of L124 and T103 plus C127. The peak inductive energy stored in L124 during the sweep time is then transferred to C127 and the distributed capacity in L124. During this cycle the beam is returned to the center of the screen.

Capacitor C127 and the distributed capacity in L124 now discharge into L124, which induces a current in a direction opposite to the current in the previous part of the cycle. The magnetic field thus created around L124 moves the scanning beam to the left of the screen.

After one half cycle, the voltage across C127 drops below ground potential, which causes damper diode CR116 to conduct and thus keeps the flyback pulse from oscillating. The inductive energy stored in the yoke by the discharge of its distributed capacity and C127 is now released to provide sweep for the first half of the scanning line. The released energy also charges C135 through CR116. The cycle repeats itself when the base voltage of Q123 is driven positive again.

Capacitor C135, in series with L124, also serves to block dc through L124 and provide "S" shaping of the current waveform. "S" shaping compensates for the stretching that would occur at the left and right sides of the CRT because the curvature of its face and the deflected beam do not describe the same arc.

The width control, L104, is placed in series with L124. The setting of L104 determines the amount of deflection current flowing through L124 and thus controls the width of the horizontal sweep.

The positive flyback pulse developed during the horizontal retrace time is rectified by CR114 and filtered by C125. This produces approximately 600 V dc,

which is coupled through the focus control, R167, to the focusing grid (C4) of the CRT (V1). Network CR112, CR113, C123, and C124 forms a voltage doubler that delivers approximately 1000 V dc to divider R163, R170. This divider provides approximately 800 V dc for the first anode (G2) of the CRT. The flyback pulse is also transformer-coupled to the secondary of T103, and the stepped-up pulse is rectified by CR100 and CR115 to produce approximately 17 kV dc and -100 V dc, respectively. The 17 kV dc is the anode voltage for the CRT; the -100 V dc serves as the source voltage for the brightness control.

Returning to the delay circuit (Q109-Q111), note that a separate and lower supply voltage is used. A series dropping resistor, R151, reduces the +55 V dc supply voltage to approximately 25 V dc. This arrangement serves two purposes: (1) it guards against the production of X-rays during an over-voltage condition, and (2) it prevents triggering of Q123 by random drive pulses when the terminal is turned on or off.

The circuitry that guards against X-ray production consists of SCR Q123, zener diode VR102, and associated components. Assume that the +55 V dc regulator circuit fails and the output voltage exceeds approximately 60 V dc. The voltage drop across divider network R147, R148, and R149 will also increase, causing current to flow through VR102 and R150. The voltage developed across R150 then causes SCR Q113 to fire and to discharge C118. This effect drops the entire supply voltage across R151 and disables Q109-Q111. Without drive, the horizontal output stage and high-voltage supply are disabled also.

A separate, lower supply line also protects against triggering of the horizontal output transistor (Q123) by random drive pulses during turn-on or turn-off. Normally, several ac cycles are required after turn-on to bring the +55 V dc bus up to level. By virtue of the component values selected for Q109, Q111, and R151, the delay one-shot will not trigger until the regulator voltage exceeds approximately +30 V dc. This dc voltage is adequate to provide stable operation of the horizontal drive one-shot and to supply adequate base drive to Q123. In this way, random drive pulses and poor collector saturation of Q123 are avoided.

During turn-off this separate supply line also offers some degree of protection against CRT spot burn. After power is turned off, C113 is rapidly discharged by the load current. The +55 V dc regulator output consequently decays rapidly to 30 V dc and Q109, Q111 will fail to trigger below this level. As a result, Q123 and the high-voltage circuit are disabled, reducing the discharge current from C113 to approximately one-third its former rate. The energy thus retained by C113 is used mainly by the vertical deflection circuit for a significantly longer discharge period. CRT beam energy is consequently distributed along the vertical axis to prevent spot burn while the high voltage stored in the CRT aquadag is discharged.

The low voltage regulator circuit consists of Q105-Q108, Q121, and related circuitry.

The +80 V dc at P102-1 is dropped to +55 V dc by series regulator Q121, whose output is sampled by voltage divider R133, R134, and R135. Approximately +7 V dc, tapped from R134, is applied to the base of Q108, while a reference voltage developed across VR101 is applied to the emitter of Q108. This transistor develops an error current that flows through R130 to the base of Q106 and the collector of Q108 by Q105, used as a dc current generator. The bias current tends to shift the

base of Q106 in a positive direction while the current from Q108 tends to shift the base in the negative direction. Thus, the error current from the collector of Q108 controls Q106, which in turn controls Q121. As a result, the output voltage is maintained at +55 V dc despite variation in load or input voltage.

Foldback current limiting is provided by Q107, R127, R128, and R129. Bias current flowing through R127 and R129 to ground provides a drop of approximately 2.4 V dc across R127. Load current through R128 provides a voltage drop that is proportional to the load current. If the load current exceeds 2.4 amperes, the emitter of Q107 is biased approximately 3 volts below the emitter of Q121, assuming a drop of 2.4 volts across R128 and 0.6 volt across CR106. Since the base of Q107 is biased below the emitter of Q121, Q107 will conduct. The drop across Q105 consequently increases so as to reduce the output voltage of the power supply, and thereby limit the peak current to approximately 2.4 amperes.

Should a short-circuit occur on the +55 V dc line, the output voltage will drop to near zero, and the short-circuit current will be limited to approximately 100 mA. Removing the short-circuit allows the regulator to resume normal operation. The average current through Q121 is approximately 0.5 amp. Combined peak currents of the horizontal and vertical deflection circuits, however, may be much greater than the average current, even though electrolytic capacitors are used across the +55 V dc line.

4.4.3 Timing Control Card

The timing control card supplies the basic clock and timing signals for the 8025 CRT terminal. This card is also the source of a power-on clear signal and the four input/output signals used in the terminal.

Block Diagram Analysis. As shown by the simplified block diagram in Figure 4-9, the Timing Control Card consists of three basic circuits: the I/O (input/output) command decoder, the power on clear (POC) circuit, and the basic timing generator for the terminal.

The decoder decodes I/O commands generated by circuits on the processor card. Decoded outputs are used on the cursor control card and the I/O interface cards.

When power is applied to the terminal, the power-on clear circuit generates a POC signal to clear the terminal. As indicated, POC is used by the processor, refresh buffer, and I/O interface cards.

A basic HF (high frequency) clock signal of 14.976 MHz is produced by dividing the master oscillator output of 29.952 MHz with a divide-by-two counter. The HF clock frequency is then counted down to provide the following clock signals: H1 - H LINE, RS CLK, Ø1 and Ø2, and READ CLK (derived from Ø2).

Horizontal clock signals H1-H LINE are used to generate the timing signals - horizontal sync (H SYNC), a composite sync (COMP SYNC), composite blanking (COMP BLNK), and horizontal blanking - needed for the video presentation. The H BLNK (horizontal blanking) output from the horizontal blanking generator is also inverted to produce POS TIME.

A vertical clock output, synchronized by $\overline{\text{H BLNK}}$, produces basic vertical timing signals (V1, V2, V4, V8, and V10). V10 is counted down in a divide-by-26 counter to generate $\overline{\text{RC}}$, which becomes a component of COMP BLNK. It is also divided by 12 to supply RATE CLK.

Other timing logic on the card uses horizontal and vertical clock inputs to supply additional timing signals. Three of these signals define the end of a character row (EOR), the end of 24 character rows (EOP), and the line in the character row used for the cursor display (CURS LINE). The fourth signal (SET LDFF) controls loading of a parallel-to-serial converter on the video control card.

NOTE: Gates are described by package reference and output pin number. Thus, XF5-4 means that gate in package XF5 which has its output on pin 4.

Circuit Description. Refer to schematic diagram 96-452-01 in Section 8, and Figures 4-10 and 4-11 for signal timing.

Gates XF5-4 and -10 and XE5-6 plus a BCD-to-decimal decoder (XE4) make up the I/O command decoder. To get an output from the decoder, all inputs to XE5-6 must be high and $\overline{\text{I/O}}$ must be low. Thus MA9 and MA10 levels determine which I/O command is generated. The truth table for the decoder is shown as Table 4-2.

The POC circuit consists of a one-shot (XA6) with its associated circuitry. When power is turned on, C14 charges through R11 to +5 V dc to fire the one-shot. The Q output of XA6 is then inverted to provide the POC pulse on pin 72.

The balance of the schematic is devoted to the generation of timing signals for the terminal. Q1, Q2 and their related components form a crystal-controlled master clock at 29.952 MHz. Its output is coupled through XB1-8 to XA1-11, which divides the clock frequency by two to supply HF CLK (high-frequency clock). HF CLK (14.976 MHz) is applied to the character clock divider (XD5), RS clock divider (XB3, XB2), and the first horizontal frequency clock (XE6).

HF CLK is divided by 10 in XD5, the character clock divider, to produce H8 (1.497 MHz). H8 has a period of 670 nsec, the time allowed for a character scan line. H1, H2, H4, and H8 outputs from XD5 are used as indicated on the schematic.

A 1.497 MHz carry output (XD5-15) enables the first counter (XE6) in the horizontal clock to count on every tenth HF clock pulse. Thus, the character clock frequency is divided by 16 in XE6 and 6 in XC2 to supply H LINE, the horizontal frequency (15.6 kHz).

HF CLK is divided by 4 and 13 in XB3 and XB2, respectively, to provide an RS CLK of 288 kHz. XB3, a decade counter, is preset to a count of six so that it operates as a divide-by-four counter. XB2 is a basic divide-by-16 counter. By presenting it to a count of 3, it operates as a divide-by-13 counter. These two counters in combination, divide HF CLK by 52 to provide a 288 kHz output at XC5-2.

The Ø1 clock signals are derived from H4, H10, and $\overline{\text{H10}}$ with a J-K master-slave flip-flop (XC4) and its associated gates. The Ø2 clock signals are derived from H1, H2, H8, and H10 with another J-K flip-flop (XC4). In both circuits the J and K inputs and the trailing edge of HF CLK determine the positive-going and

Table 4-2. I/O command decoder truth table.

CPU COMMAND	INPUTS				ACTIVE OUTPUTS			
CODE	MA8	MA11 - 13, WAIT, I/O	MA9	MA10	POLL	IOD	STAT	IOB
INP0	H	L	L	L	L	H	H	H
INP1	H	L	H	L	H	L	H	H
INP2	H	L	L	H	H	H	L	H
INP3	H	L	H	H	H	H	H	L

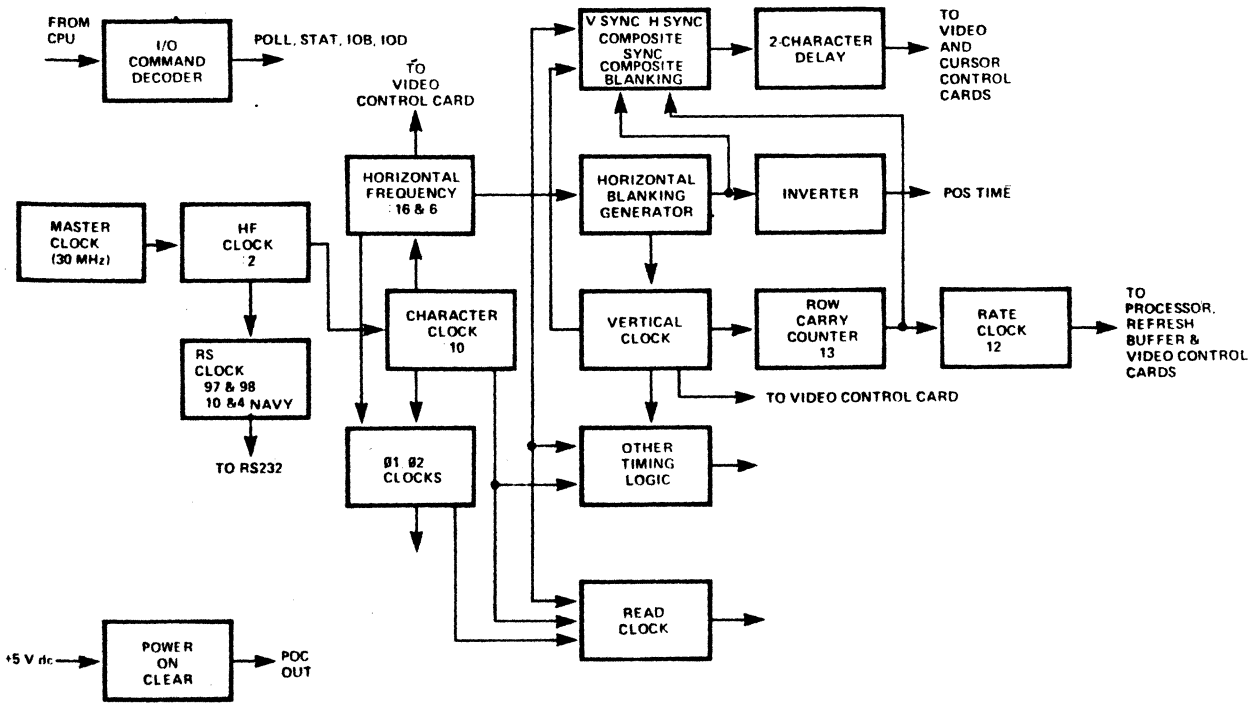


Figure 4-9. Timing control card block diagram.

negative-going transitions of the clock pulses, respectively. Each clock circuit operates to provide an output pulse for every 20 HF clock pulses. Thus, Ø1 and Ø2 pulses occur at the rate of 748.8 kHz. They do not overlap, however, since different horizontal timing signals are used for each circuit. For the same reason, Ø1 and Ø2 have different pulse widths--402 nsec and 335 nsec, respectively.

READ CLK (read clock) is produced by an edge-triggered D-type flip-flop (XC3-6). Signal $\overline{Ø2}$ at XC3-3 determines the positive-going transition of READ CLK. H1, H8, and $\overline{H10}$ are NAND-gated by XE5-8 to preset XC3-6 low. Thus, the preset input to XC3 determines the negative-going transition of READ CLK. The timing of H1, H8, $\overline{H10}$, and $\overline{Ø2}$ produces a square-wave clock signal at the Ø2 rate, 748.8 kHz.

Horizontal timing signals for the video presentation are generated in XB5-5 (J-K flip-flop) and XC3-8 (edge triggered D-type flip-flop).

H BLNK (horizontal blanking) is produced at XB5-5. On the negative edge of H LINE, XB5-5 is set high and remains high until XB5 is cleared by the output on XF2-12. The timing of the clear operation depends upon the jumper arrangement (E3 through E7) at the input to XF2. Normally, E3 and E4 are connected; other jumper arrangements are used for special terminal configurations.

With only E3 and E4 connected, XB5 is cleared when H160 goes high. This event produces a 10.72 usec, 15.6 Hz H BLNK pulse used with the standard 80-character-per-line display and the optional 40-character-per-line display.

H BLNK is inverted by XC5-12 to become $\overline{\text{POS TIME}}$. H BLNK is also used for the J-K inputs to the XB5-2 flip-flop, which produces the horizontal component of composite sync ($\overline{\text{COMP SYNC}}$). The negative edge of H40 sets XB5. Eight character periods later it is reset by $\overline{H160}$ at XB5-13 to produce a 5.36 usec pulse. The output on XB5-2 is OR-gated by XE2-11 to the 2D input of XE3, a two-character-period delay register. This delay compensates for the time between character addressing and the character display on the CRT. Note that XE3 is clocked by the output on pin 8 of XE2. This clock pulse is developed from H2, H4, and H10 to clock XE3 every other character period.

Horizontal sync (H SYNC) is generated at pin 8 of XC3. XC3 is set by the gated output of H40, H80, H320, and H LINE on XD3-8. It is reset by XB5-2 8.04 usec later to supply the H SYNC input to XE3 at the line rate of 15.6 kHz.

The vertical timing signals for the video presentation are generated by XC1, XC2, and XD2 which, count-down H BLNK pulses.

XC1 divides by 10 or 12, depending on the power-line frequency, to provide V1, V2, V4 and V8. For 60 Hz operation, XC1 is loaded by V1 and V8 through XF2-8. It is loaded by V1, V2 (jumper E8-E9 connected), and V8 for 50 Hz operation. (Note that at 50 Hz there are 2 extra lines between character rows and 52 extra lines per frame). The output of XF2-8 also becomes the $\overline{\text{EOR (end of row)}}$ signal at XF1-10. EOR is a 63.6 usec pulse occurring at a 1.56 kHz rate.

The V8 output of XC1 is divided by 2 and 13 in XC2 and XD2, respectively, with XC2 supplying V10 and XD2 providing RC (row carry). RC is a 1.28 millisecond pulse occurring at a 60 Hz rate.

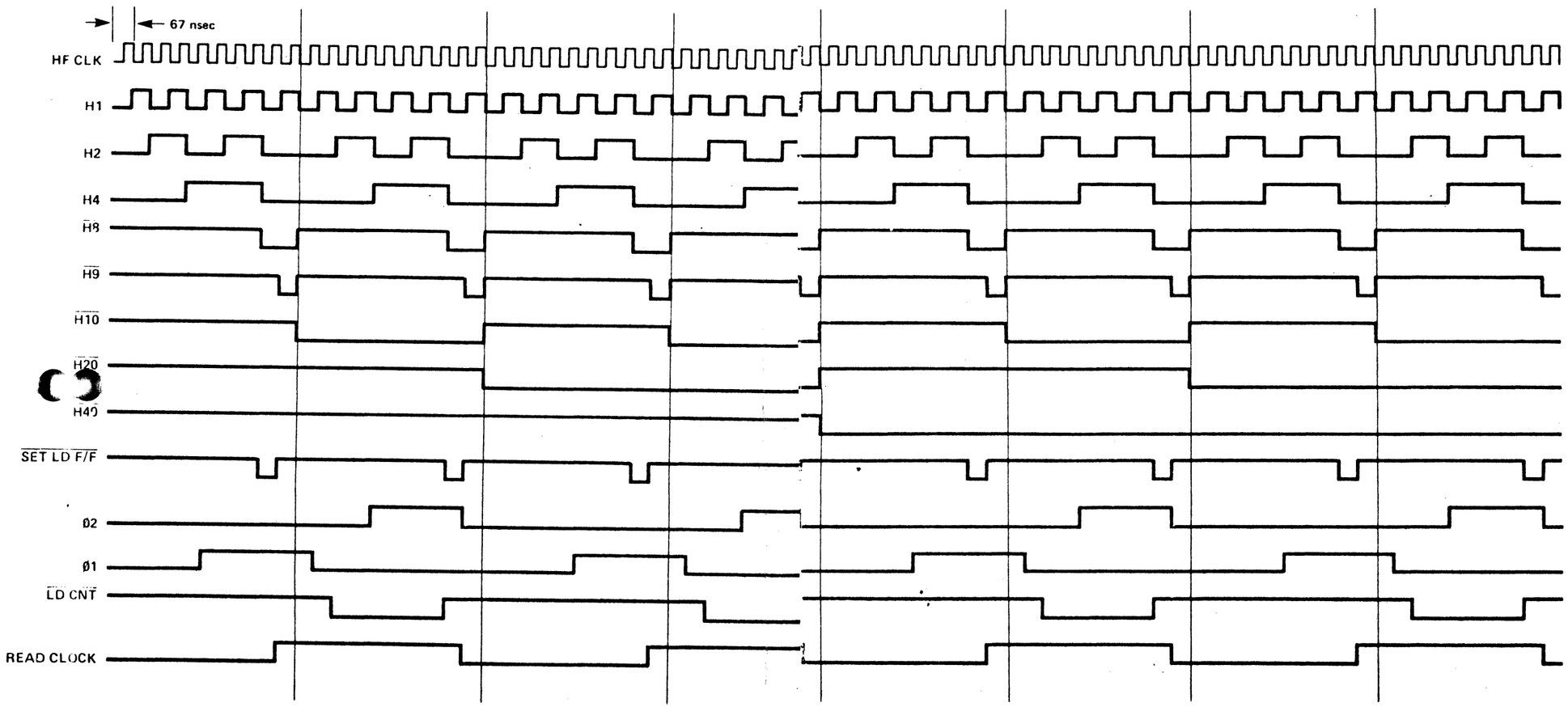


Figure 4-10. Timing control card timing diagram.

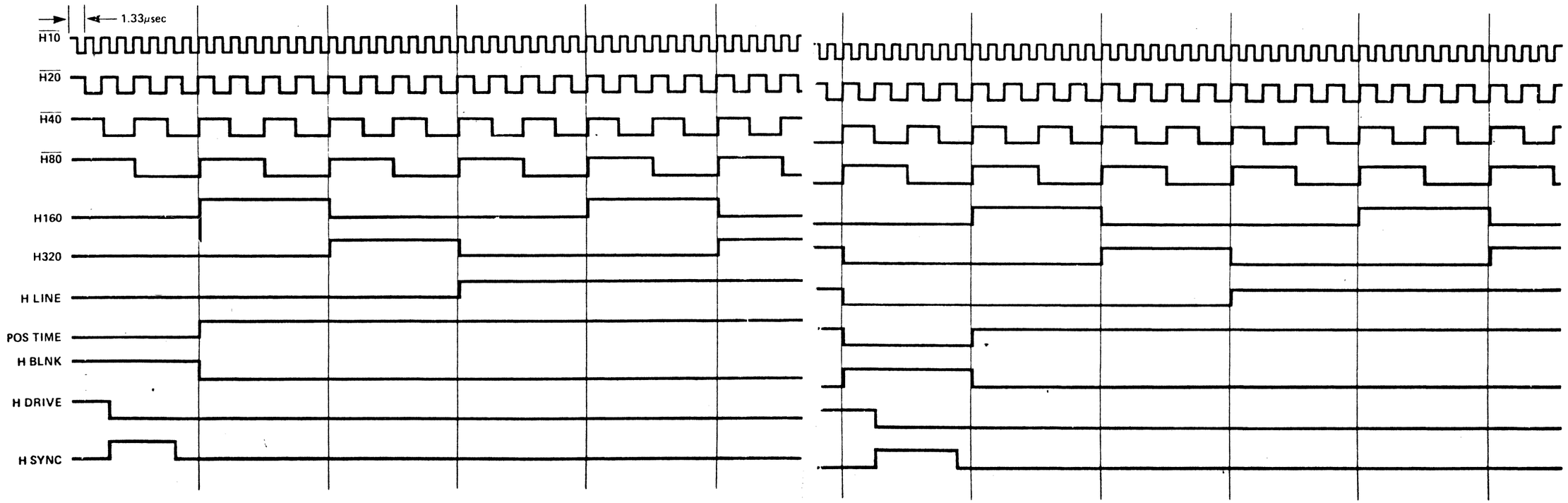


Figure 4-11a. Timing control card timing diagram.

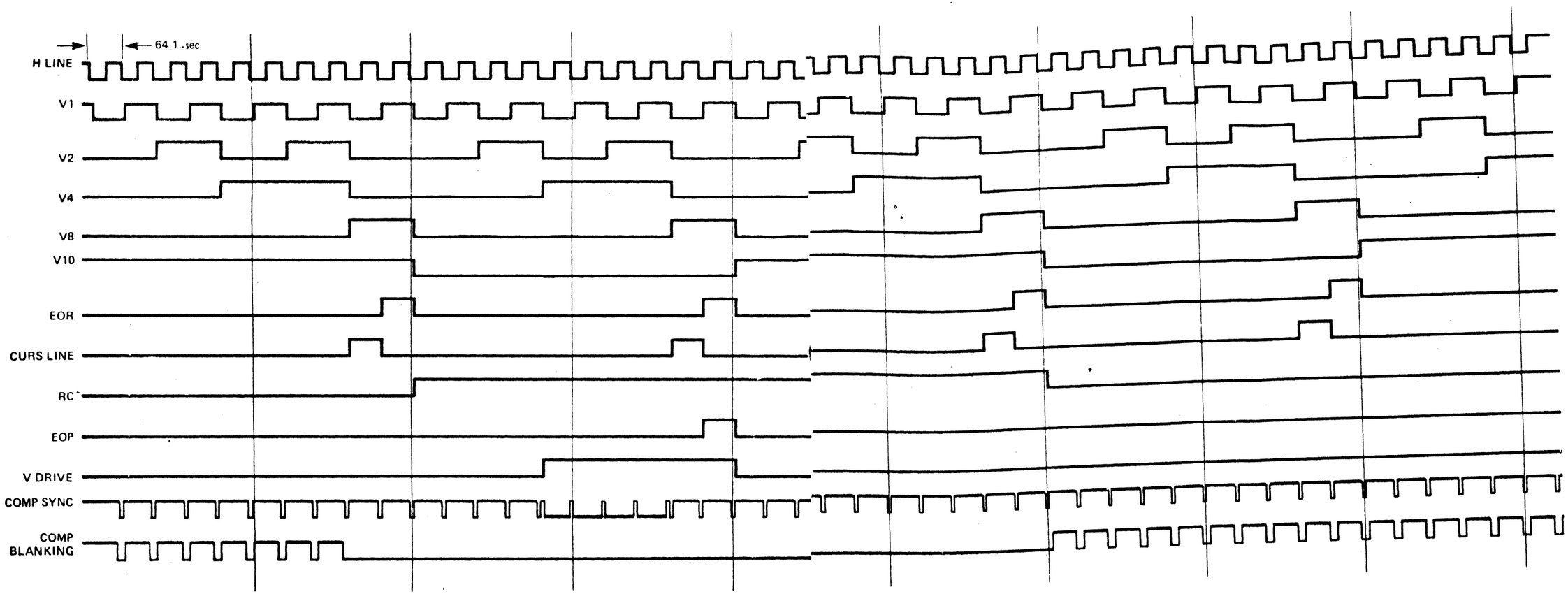


Figure 4-11b. Timing control card timing diagram.

RC is inverted by XD6-14 to $\overline{RC}$. $\overline{RC}$ blanks the CRT during vertical retrace, which occurs during the last two character rows in a frame. It is also divided by 12 in XD6 to produce the RATE (rate clock) at 5 Hz.

Vertical sync (V SYNC) signals are derived by gating V4, V8, RC and V10 through XE1-10 and -13 and XE2 to the two-character delay, XE3. V SYNC, with a 350 usec pulse width, occurs at a 60 Hz rate.

Composite sync ($\overline{COMP\ SYNC}$) is obtained by OR-gating the horizontal sync and vertical equalization pulses in XE2-11 to the 2D input of XE3. Vertical components are gated through to XD1-8 during V DRIVE when V4 and H SYNC at XC3-8 are high. Thus, during the display position of the field of COMP SYNC pulses are 8.04 usec long, occuring once every horizontal line. During the vertical sync period there are four 54 usec pulses at the horizontal frequency. $\overline{COMP\ SYNC}$ is also applied to XE3.

Composite blanking ($\overline{COMP\ BLNK}$) is the OR-gated combination of $\overline{H\ BLNK}$, vertical blanking ($\overline{RC}$), and 10th through 12th lines of each character row (50 Hz version only). The 10th through 12th line input to OR gate XD3 (pin 4) is low when V1 and V2 are high at XE1-5 and -6. Composite blanking is applied to the two-character delay (XE3) and also to an inverter (XF3-12) to supply an undelayed blanking (UND BLNK) signal.

The remaining signals generated on the Timing Control Card are cursor line (CURS LINE), end of page (EOP), and set load flip-flop ($\overline{SET\ LDFF}$).

Cursor line is produced by XD1 (pin 6) whenever V1 and V2 are low at pins 5 and 6 of XE1 and V8 is high. EOP is generated by decoding RC, $\overline{V10}$, and EOR in XF2-6. A 63.6 usec output pulse, with a 60 Hz rate, appears at XF3-8 at the end of every 24 character rows. SET LDFF is the NAND combination of $\overline{H1}$ and H8 at XC6-6. This signal has a pulse width of 67 nsec and an H8 repetition rate (1.497 MHz).

4.4.4 Processor Card

The processor card controls nearly all terminal operations. It polls cards on the A Data Bus to determine whether a card is ready to transfer data in either direction. When a card is ready, the processor--working with the terminal memory--interprets and processes the data and enables the transfer.

Block Diagram Analysis. A simplified block diagram of the processor card is provided in Figure 4-12. The processor card centers around an IC central processor unit (CPU) designed to work with an external memory. Data enters and leaves the CPU on an internal time-multiplexed data bus. The CPU has eight timing states, labeled and defined as follows:

T1: Time used to load least significant eight bits of address into external memory and increment CPU program counter.

T2: Time used to load most significant six bits of address and two control bits into external memory; also to increment CPU program counter with a carry from T1.

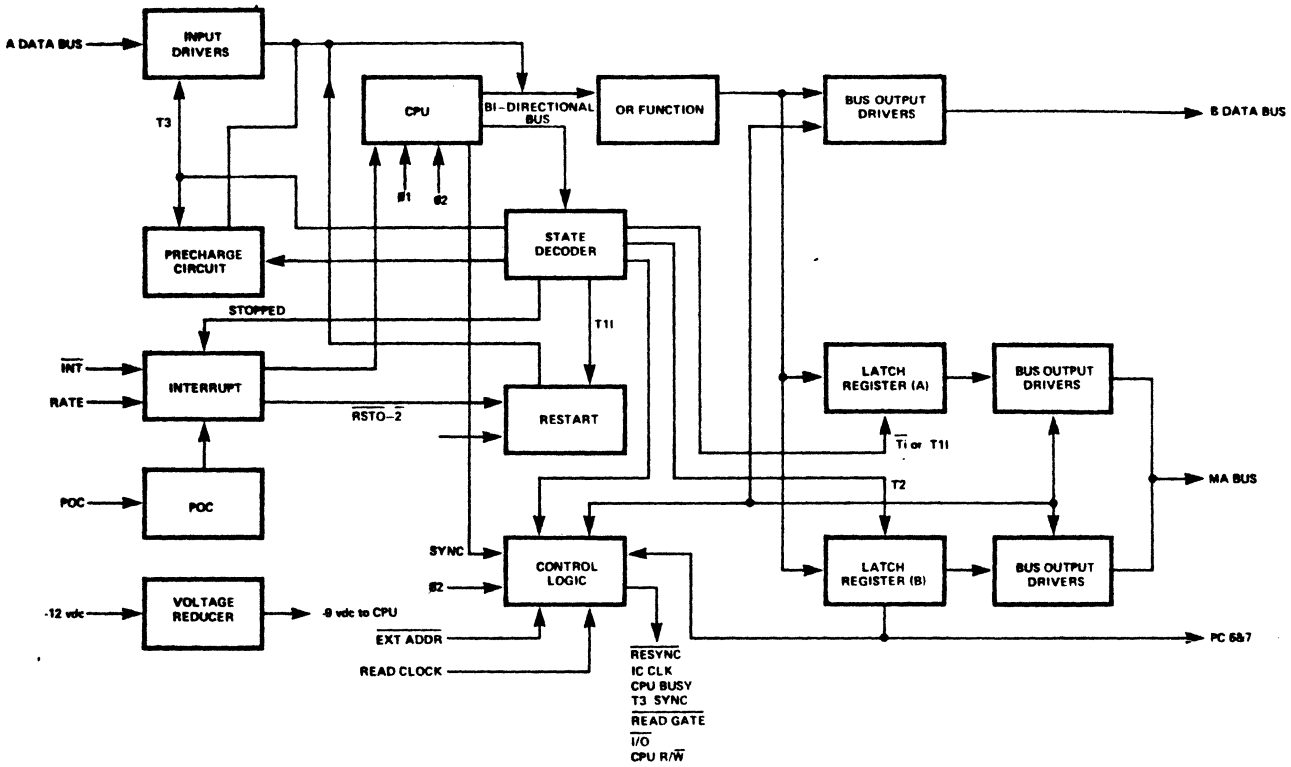


Figure 4-12. Processor card block diagram.

T3: Time used to transfer data into or out of the CPU, obtain and decode instruction, or acknowledge READY: refresh CPU internal memories.

T4,T5: Time used by CPU to execute instruction.

T1I: CPU acknowledgement of interrupt signal; replaces T1 when CPU is interrupted.

STOPPED: Indicates CPU received a HALT instruction.

WAIT: Indicates CPU READY line was low prior to end of T2 cycle.

Data on the A Data Bus comes in to the CPU through the input drivers during T3. A precharge circuit decreases the input rise time. Output data from the CPU is placed on the B Data Bus during T3 and on the MA Data Bus during T2 and T1 or T1I. In addition, data from other sources can be applied to the buses when the CPU is not transferring data.

Output-state signals from the CPU are decoded to provide the previously described timing states.

Interrupt is used to restart the CPU program at a memory address specified by $\overline{RST0}$-$\overline{RST2}$. The interrupt sequence can be initiated by a POC, an interrupt signal ($\overline{INT}$), or a decoded STOPPED signal. During an interrupt, the restart circuit enters a restart address into the CPU to define the start location of the program.

A voltage reducer lowers the -12 V dc supply to -9 V dc for the CPU.

Circuit Description. Refer to schematic diagram 96-369-01 in Section 8, and to Figure 4-13 for signal timing.

The control inputs to the CPU (XC2) are Ø1 and Ø2 clock signals, READY, interrupt ($\overline{INT}$), and $\overline{RST0}$-$\overline{2}$ (restart). The Ø1 and the Ø2 inputs provide a 748.8 kHz two-phase, non-overlapping clock signal for the CPU.

READY inhibits the CPU when the external memory is not available for data transfer. This input is not used in the 8025 CRT Terminal, since the memory is always available.

The CPU can recognize interrupt only at certain times. Control logic is thus required to meet the timing requirements.

When $\overline{INT}$ goes low, the negative-going edge--inverted by XB5--sets flip-flop XA6 at pin 3. The leading edge of IC CLK (IC Clock) from XB6-11 sets the other XA6 flip-flop at pin 11. The output on XA6-9 enters an INTERRUPT signal into the CPU. When the CPU replies with a T1I (decoded from SO, S1, and S2), T1I sets flip-flop XA4 at pin 1. This flip-flop enables the six interrupt NAND gates (XC3, XC4) to restart the CPU during T3. Flip-flops XA6 and XA4 are reset at the end and start of T3 at pins 1 and 4, respectively.

A POC-initiated interrupt is accomplished in the following manner. When power is applied to the terminal POC goes high and is inverted by XB5-10 to reset flip-flop XA3 at pin 10. The next low RATE pulse at pin 9 of XB5 sets the XA3 flip-flop at pin 9. Since RATE occurs at 5 pps, it produces an interrupt 0.2 sec after power is applied. This delay allows the CPU to clear all its registers and preset all its flip-flops before interrupt restarts the program. Note that POC also resets XA4 at pin 10, XA5 at pin 1, and XA6 at pin 13.

An interrupt can also be generated when the CPU enters the stopped ($\overline{STOP}$) state; $\overline{STOP}$ sets flip-flop XA6 at pin 4. On the leading edge of IC CLK, the other XA6 flip-flop is set at pin 11 to produce an interrupt signal at XA6-9.

The states of $\overline{RST0}$-$\overline{2}$ specify the program restart address supplied to the CPU when the interrupt gates are open during T3. For $\overline{INT}$ and $\overline{STOP}$ interrupts, one of eight addresses can be specified (0_8, 10_8, 20_8, 30_8, 40_8, 50_8, 60_8, and 70_8). One of only four restart addresses (10_8, 30_8, 50_8, and 70_8) can be specified for a POC interrupt. This is true because $\overline{RST0}$ is held high by the output on pin 6 of XC4. Thus, the least significant bit of the restart command is always low for a POC interrupt.

The SYNC output from the CPU indicates that it is on the second half of the timing state represented by SO, S1, and S2. SO, S1, and S2 are decoded in XB2, a BCD-to-decimal decoder, to indicate the state of the CPU at any time in the instruction cycle.

Data on the A Data Bus is transferred to the CPU through eight open-collector TTL input drivers (XE3, XF3), which are enabled during T3 to gate data into the CPU. A precharge circuit (Q1, R7 through R16, and CR1 through CR8) is used to decrease the input rise time. This circuit switches in R7-14 during the time (T3) data is entering the CPU. During the rest of the time, these resistors are disconnected by CR1-8. Thus, the CPU does not have to drive the load presented by R7-14. The precharge circuit is switched in when T3 sets XA4 at pin 11 to make XA4-6 high. Disconnect is performed when XA4 is reset at pin 8 by T2 SYNC and T1I or T2 SYNC when XC5-8 is high (CPU in read mode).

Data out of the CPU is OR-gated through XE1 and XE2 to bus output drivers XF1 and XF2, and latch registers XD2 through XD5.

CPU data is placed on the B Data Bus when the bus output drivers are enabled by a high output from XF6-8. XF6-8 is high whenever the CPU can transfer data in either direction (CPU BUSY and $\overline{\text{EXT ADDR}}$ are high).

The data transfer occurs during a READ instruction, the second half of T2 or WAIT, or T3. The drivers are disconnected from the bus when the CPU cannot transfer data (CPU BUSY or EXT ADDR are low). This frees the bus for DMA-type data transfers.

During T1 or T1I, output data is loaded into the XD2 and XD4 registers to provide the least significant eight bits of an address. The most significant six bits are loaded into XD3 and XD5 during T2. Data out of the registers is placed on the MA Data Bus via drivers XE4, XE5, and XF5. These drivers are also enabled when the CPU can transfer data in either direction. Note that the two most significant bits located into XD5 contain CPU cycle-type information.

Other control signals generated on the processor card are $\overline{\text{RESYNC}}$, $\overline{\text{READ GATE}}$, $\overline{\text{I/O}}$, CPU R/$\overline{\text{W}}$ and IC CLK.

$\overline{\text{RESYNC}}$, at XO6-12, is the SYNC pulse reclocked with Ø2 in flip-flop XA3 (pin 3). It is required because SYNC is delayed up to 700 nsec in the CPU after Ø2.

$\overline{\text{READ GATE}}$, at XE5-8, is the second half of T2 or WAIT AND-gated with READ CLOCK.

$\overline{\text{I/O}}$ (input/output) results from a decoding in XF6 of the CPU cycle-type information contained on the D6 and D7 outputs of the CPU during T2. CPU R/$\overline{\text{W}}$ (CPU read, not write) is the AND-gated combination of T3 SYNC and a decoding of $\overline{\text{PC6}}$ and $\overline{\text{PC7}}$ at XC5-9. XC5-9 is low when the CPU writes data into memory. Thus, the CPU writes data into or reads data out of memory when CPU R/$\overline{\text{W}}$ is low and high, respectively.

IC CLK is derived by NAND-gating the SYNC output from the CPU with Ø2. This supplies a 335 nsec pulse at 374.4 kHz.

Q2 and its associated circuitry reduces the -12 V dc supply to -9 V dc, the voltage needed for the CPU. A reference voltage of 9 V for regulator Q2 is developed across R22 and CR9; thus Q2, operating as an emitter follower, maintains the output level at 9 volts.

THEORY OF OPERATION

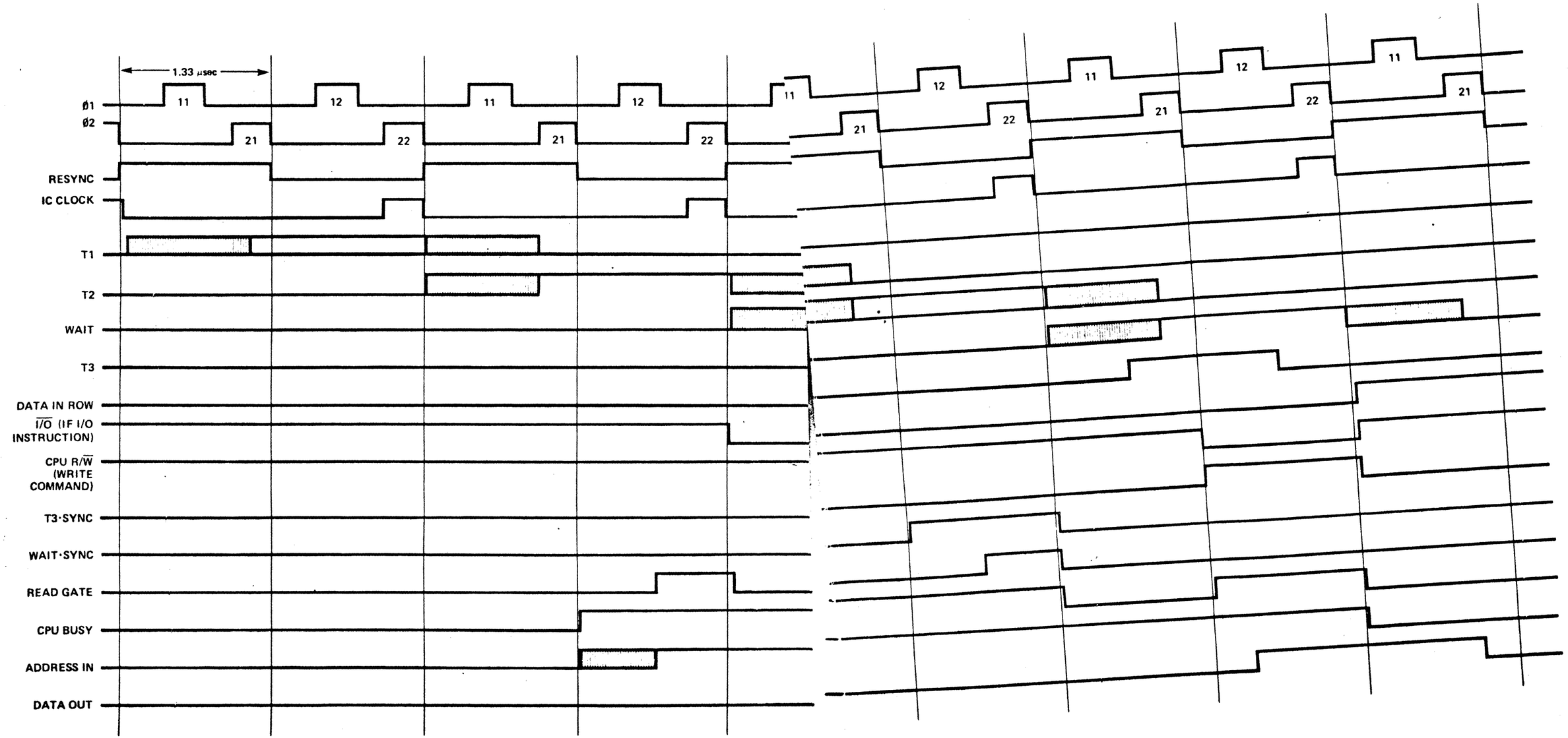


Figure 4-13. Processor card (CPU) timing diagram.

4.4.5 PROM Card

The PROM card serves as the program memory for the 8025 CRT Terminal. Memory chips on this card contain all instructions needed by the CPU to control terminal operations.

Block Diagram Analysis. As shown by the simplified block diagram in Figure 4-14, the PROM card has three major sections: an address sector gate, a chip selector, and a memory that consists of sixteen 256-byte PROM chips. Full addressing of the card is done on MA0-15, with the state of MA14 and 15 always held constant.

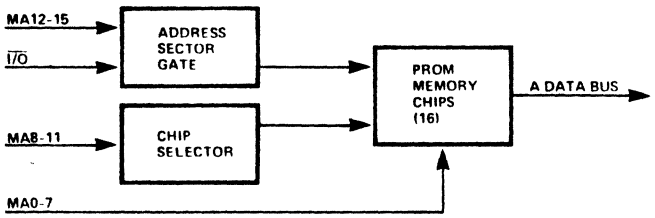


Figure 4-14. Buffered PROM card block diagram.

The address sector gate defines the range of addresses to which the card can respond. For addresses outside the range, the sector gate disables all the PROM chips by inhibiting one of two enable inputs required by each chip. For addresses within the defined range, MA12-15 will satisfy the gate, and it partially enables all of the chips.

Assuming the sector gate is satisfied, the chip selector supplies the second enable input to the PROM chips specified on MA8-11. This second enable input, plus addressing on MA0-7, defines the memory location of the data to be read out on the A Data Bus.

Circuit Description. Refer to Schematic diagram 96-434-XX in Section 8.

The maximum capacity of the PROM card is 4,096 bytes (32 chips) of memory. If fewer than 4,096 bytes are needed for a particular version of the terminal, the unused chips are eliminated. For example, if only 2,048 bytes are used, rows A and C of chips are eliminated.

Four inverters (XF5 pins 2, 8, 10 and 12), header XF6 and NAND gate XE6-8 form the address sector gate circuit. The four most significant address bits (MA12-15) are wired on the header to define the address sector for the card. For the card shown, jumpers E2-E15, E4-E13, E5-E12 and E7-E10 are in place to define address sector 0 (addresses 0_8 to 3777_8).

The six highest bits of address are transferred during CPU state T2. Addresses are changing during T1 and T2, but are stable throughout T3. MA14 and 15 are hard-wired at a high level for this system.

For any address between 0_8 and 3777_8, MA12 and 13 are low. Inversion through XF6 places high inputs on pins 11 and 12 of gate XE6. MA14 and 15 are also high at the input to XE6-8 with $\overline{I/O}$ also high, XE6-8 applies a low partial enable input to CS_2 (pin 14) of each PROM chip. Any change in the inputs to the address sector gate will cause the output of XE6-8 to go high to inhibit all chips.

Inputs MA8-11 select the PROM chips to be addressed. These inputs are converted in two BCD-to-decimal decoders (XE4 and XE5), and each output of the decoder is applied to the $\overline{CS}$ inputs (pin 13) of two PROM chips (e.g., the output at XE5-1 is applied to PROM chips XB1 and XD1). A low input at $\overline{CS}$ selects the two chips for reading. The lower four and higher four data bits are stored in the XB and XD series PROM chips, respectively.

Eight bits of address (MA0-7) plus a low input at both $\overline{CS}$ and $\overline{CS_2}$ allow the data stored in the two chips to be read onto the A Data Bus.

Table 4-3 gives PROM chip location as a function of memory address.

Table 4-3. PROM chip location vs. memory address.

PROM CHIP COORDINATES		MEMORY ADDRESS (in octal)
MOST SIGNIFICANT BITS	LEAST SIGNIFICANT BITS	
XD1	XB1	00000 - 00377
XD2	XB2	00400 - 00777
XD3	XB3	01000 - 01377
XD4	XB4	01400 - 01777
XD5	XB5	02000 - 02377
XD6	XB6	02400 - 02777
XD7	XB7	03000 - 03377
XD8	XB8	03400 - 03777
XC1	XE1	04000 - 04377
XC2	XE2	04400 - 04777

4.4.6 Buffered RAM (Refresh) Memory Card

Block Diagram Analysis. A simplified block diagram of the RAM (refresh) memory card is shown in Figure 4-15.

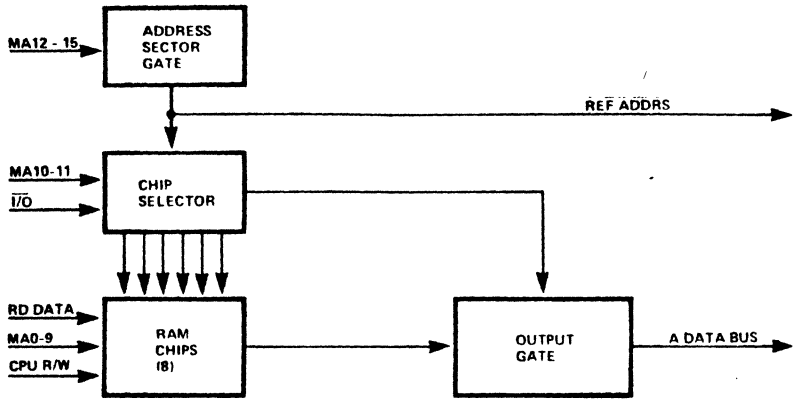


Figure 4-15. Buffered RAM memory card block diagram.

As with the program memory, the address sector gate defines the range of addresses to which the card responds. Data can be read into the memory from the RD Data lines when a CPU read signal is applied to the RAM chips. Data is read out of the memory through the output gate on the A Data Bus. The chip selector controls the output gate and selects the memory chips to be addressed.

Circuit Description. Refer to Schematic diagram 96-433-XX in Section 8, and to Figure 4-17 for signal timing.

Maximum capacity of the RAM card is 4,096 bytes (32 chips) of memory. Since only 2,048 bytes (16 chips) are used in the standard 8025 CRT terminal, the XA and XB chips are eliminated.

Four inverters (XF5 pins 2, 8, 10 and 12) header XF6, and NAND gate XE6-8 form the address sector gate. The four most significant address bits (MA12-15) are wired on the header to define the address sector for the card. For the card shown, jumpers E1-E16, E3-E14, E5-E12, and E7-E10 are in place to define address sector 3 (addresses 34000_8 to 37777_8).

For any address between 34000_8 and 37777_8, MA12 and MA13 are high. MA14 and MA15 are hard-wired at a high level for this system. Thus, NAND gate XE6-8 is enabled when $\overline{I/O}$ is high and applies a low input to XE5-12. Because this card is used as the refresh memory, the A-B jumper is in place, and consequently, the input to XE5-12 also serves as $\overline{REF\ ADDR}$.

The inputs to XE5 (MA10, MA11, $\overline{I/O}$, and $\overline{REF\ ADDR}$) define the memory chips to be addressed. MA10 and MA11 in the combinations high-low and high-high enable the XC and XD chips, respectively, assuming that $\overline{I/O}$ is high and XE5-12 is low.

Nine bits of address, plus a low level at pin 13 of each RAM chip in a given row, allow data from the RD Data Channel to be entered into the memory when CPU R/$\overline{W}$ at pin 65 is low. If CPU R/$\overline{W}$ is high, data is read out of the memory through the output gate to the A Data Bus. The output gates are enabled by the output of the XE6-6 NOR gate when the memory chips are enabled.

Table 4-4. RAM chip location vs. memory address.

RAM CHIP COORDINATES								MEMORY ADDRESS (in octal)
BIT POSITIONS								
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	
C8	C7	C6	C5	C4	C3	C2	C1	34000 - 35777
D8	D7	D6	D5	D4	D3	D2	D1	36000 - 37777

4.4.7 Refresh Buffer Card

The refresh buffer card provides refresh data for the video display, temporarily stores video status and keyboard indicator light (LED) data, and decodes a beep signal.

Block Diagram Analysis. A simplified block diagram of the card is shown in Figure 4-16.

Video status data is stored at address 37771_8 in the refresh memory. When called from memory, at the end of each page, the data is placed on RM0-3 in order to update the video status latch. The $\overline{BLANK}$ and $\overline{CS0-3}$ outputs control block and underline cursor, video on-off, and control character blanking.

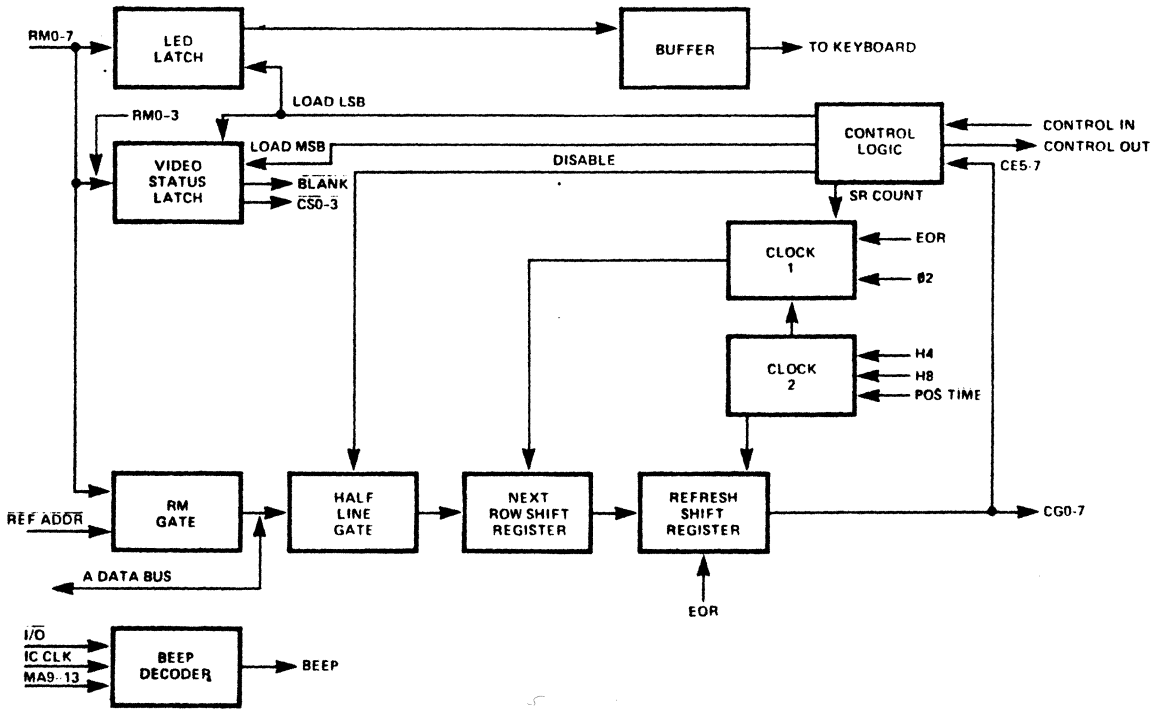


Figure 4-16. Refresh buffer card block diagram.

The XD RAM chips contain six special bytes, as follows:

- Keyboard indicators (illuninated keys); see Section 4.4.7
- Video status (video, cursor type); see Section 4.4.10
- Cursor position (row); see Section 4.4.9
- Cursor position (column); see Section 4.4.9
- Page base (least significant bits); see Section 4.4.8
- Page base (most significant bits); see Section 4.4.8

Table 4-4 gives RAM chip location as a function of memory address.

The video status address in memory also stores four bits of LED (light emitting diode) data. Eight other LED bits are stored at memory address 37770_8. All 12 of these bits are loaded into the LED latches during vertical retrace. The LEDs themselves are located in the terminal keyboard, and each lights up whenever a "1" is stored in the corresponding latch. (Note that only those LEDs that are used for a particular configuration are installed in the keyboard).

Any time the refresh memory is addressed, a $\overline{\text{REF ADDR}}$ signal enables the RM gate. As a result, RM data is placed on the A Data Bus for use by either the CPU, shift registers or DMA devices. With an 80-character-per-row display, the half-line gate is always open.

Data for an entire character row (80 characters) is loaded into the refresh shift register from the next row shift register at the end of every character row. The refresh register functions as a 10-cycle recirculating memory to supply refresh data for the video display on CGO-7. When data has been transferred to the refresh register, data for the following character row is read out of memory and loaded into the next row register.

The beep decoder decodes $\overline{\text{I/O}}$, IC CLK, and MA9-13 to provide a beep signal for use on the cursor control card.

Circuit Description. Refer to schematic diagram 96-415-01 in Section 8, and to the timing diagram in Figure 4-17.

Whenever the refresh memory is addressed, $\overline{\text{REF ADDR}}$ is low at XD6-2 and -13. If the CPU has not issued an $\overline{\text{I/O}}$, XD6-1 will also be low. The resulting high output at XD6-12 enables the XC4, XB4 gates to couple RMC-7 to the A Data Bus.

The refresh shift register (XE2, XD2) is loaded from the next row shift register (XE3, XD3) by signal EOR, which occurs during the 10th line scan for each row of characters. During this line scan the data from the previous line of characters appears at the output of the refresh shift register while data for the next row is moved in from the next row shift register. During the subsequent 9 line scans, the next row shift register is reloaded from refresh memory with data for the next

row of the display.

XE3 and XD3 are clocked by SR COUNT while being loaded and by REG 2 cl while transferring data into the refresh shift register. SR Count, which causes the refresh control card to address refresh memory at sequential locations is an OR function of:

1. The output on XA5-12 when the terminal operates in the standard 80-character-per-row mode.
2. The output on XA5-6 or XA5-12 when the terminal operates in the 40-character-per-row mode.

In the first case, SRINH (shift register inhibit) is always high, and the XA5-6 output is held high. SRINH goes low once 40 characters have been loade from memory into the next row shift register. This allows the remaining space in the register to be filled with nulls.

In the 80-character-per-row mode (and during the first half of a charac ter row in the 40-character mode), SR COUNT is produced by the output on XA6-3. When the CPU is not busy (CPU BUSY is low), the refresh buffer takes every other available bus cycle. XA6-3 is low for one Ø2 period, and is then set high for th next Ø2 period to generate SR COUNT.

As stated above, data in XE3 and XD3 is loaded at the end of each charac- ter row into the refresh shift register, XE2 and XD2 with loading controlled by the EOR (end of row) signal. XE2 and XD2 act as a 10-cycle recirculating shift register to provide the refresh function for the video display. The clock signal for this register, supplied at XC6-3, is derived from H4 or $\overline{H8}$ during display time

The video status latch, XC3, temporarily stores video status information arriving on RMO-3 to provide the outputs indicated. Table 4-5 defines the functic of these outputs.

Table 4-5. Video status functions.

FUNCTION	BIT STATE			
	$\overline{CS3}$	CS2	$\overline{CS1}$	$\overline{CS0}$
Underline cursor, video on	X	X	H	H
Block cursor, video on	X	X	H	L
Cursor off	X	X	L	H
Video off ($\overline{BLANK}$)	X	X	L	L
Blank control characters	X	H	X	X
40 characters-per-row	H	X	X	X
X = don't care (may be either state)				

THEORY OF OPERATION

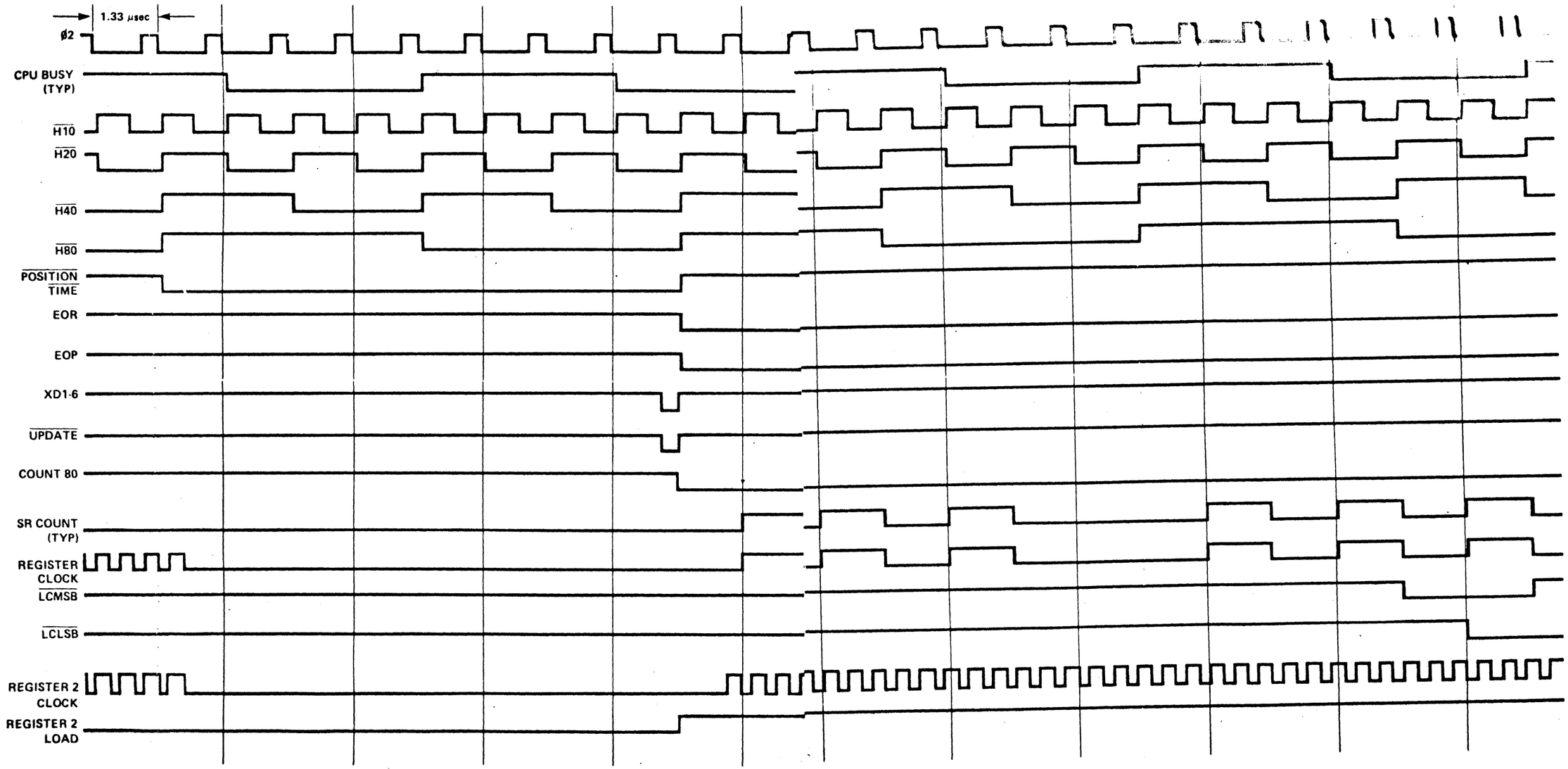


Figure 4-17a. Refresh buffer/control card timing diagram.

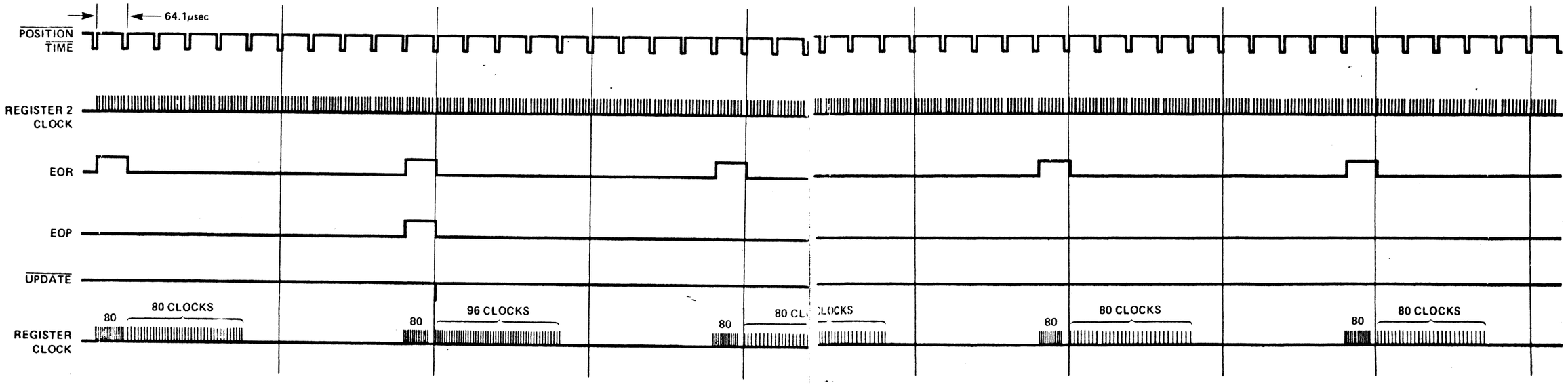


Figure 4-17b. Refresh buffer/control card timing diagram.

XB3, XC2, and XB2 make up the 12-bit LED latch. The first byte of LED data on RM4-7 is stored in XB3; the second byte on RM0-7 is stored in XC2 and XE3. Data in all latches is applied to the B1 and C1 drivers to operate light emitting diode indicators located on the keyboard. The LED current is limited to a maximum of 40 MA by resistors R1-R12.

Both the video status and LED latches are cleared by POC and H4 (XD5-2 and -1, respectively) whenever the terminal is turned on. Since both video status data and the first byte of LED data are located at the same memory address (37771), XC3 and XB3 are loaded by the same load pulse, generated at XA2-9. The output on XA2-1 loads XC2 and XB2.

Both the video status and LED latches are loaded at the end of each display page when $\overline{\text{UPDATE}}$ goes low. This low level sets the XA3 counter to zero. XA3 then counts to 15 and stops since its carry output (pin 15) is fed back to inhibit XA3 at pin 7. XA2, a BCD-to-decimal decoder, decodes the other XA3 outputs. The load pulse for XC2 and XB2 is produced on Count 0, and XC3 and XB3 are loaded on count 7. $\overline{\text{LCMSB}}$ and $\overline{\text{LCLSB}}$ are generated on counts 5 and 6, respectively. These two signals load update data from memory into the cursor position register on the cursor control card.

Other control signals generated on the refresh buffer card are: LOAD F, BLINK, $\overline{\text{CLRF}}$, $\overline{\text{EXT ADDR}}$, PRIORITY OUT, and $\overline{\text{DMA REQ}}$.

LOAD F is produced if an HLL is decoded in the most significant bits out of the refresh shift register. If an HLL is decoded in XC5 and XD6, the character on CGO-7 is a video modification character rather than a displayable character. The three least significant bits of the character define the modification (e.g., dim, blink) to be made to the video presentation. LOAD F is gated at the character rate ($\overline{\text{H8}}$) on XE5-5 as long as an HLL exists. LOAD F is used to load the video modification register on the video control card.

BLINK is used to make characters on the CRT blink by inhibiting the video 25% of the time. The blink rate is 2.5 pps as derived by dividing RATE CLK (5pps) by two in XC5 and AND-gating the output with RATE CLK in XC6.

$\overline{\text{CLR F}}$ is used to clear the video modification register at the end of every scan line. It is generated at XD6-6 during POS TIME in sync with $\overline{\text{H40}}$. This terminates the video modification at the end of each row of characters.

$\overline{\text{EXT ADDR}}$ is produced whenever the refresh buffer takes a bus cycle. As previously described, CPU BUSY is low and pin 3 of XA6 is high when this occurs. The resulting low output at XA4-6 allows external devices to address the refresh memory by inhibiting the B Data Bus drivers on the processor card.

PRIORITY OUT at XC6-11 is also used by external devices. XC6-11 can only be high when the CPU doesn't need the bus (CPU BUSY is low) and the refresh buffer has not taken the bus (XA6-2 is high).

$\overline{\text{DMA REQ}}$ (direct memory access request) is generated at XA4-11 by $\overline{\text{CNT 80}}$ when SRINH is high. ($\overline{\text{DMA REQ}}$ is not used in this terminal).

The BEEP circuit (XE5, XE6), though not related to refresh functions, is included on the refresh buffer card. A $\overline{\text{BEEP}}$ pulse is generated in sync with IC CLK when a beep command is decoded. The $\overline{\text{BEEP}}$ signal triggers an audio oscillator on the cursor control card.

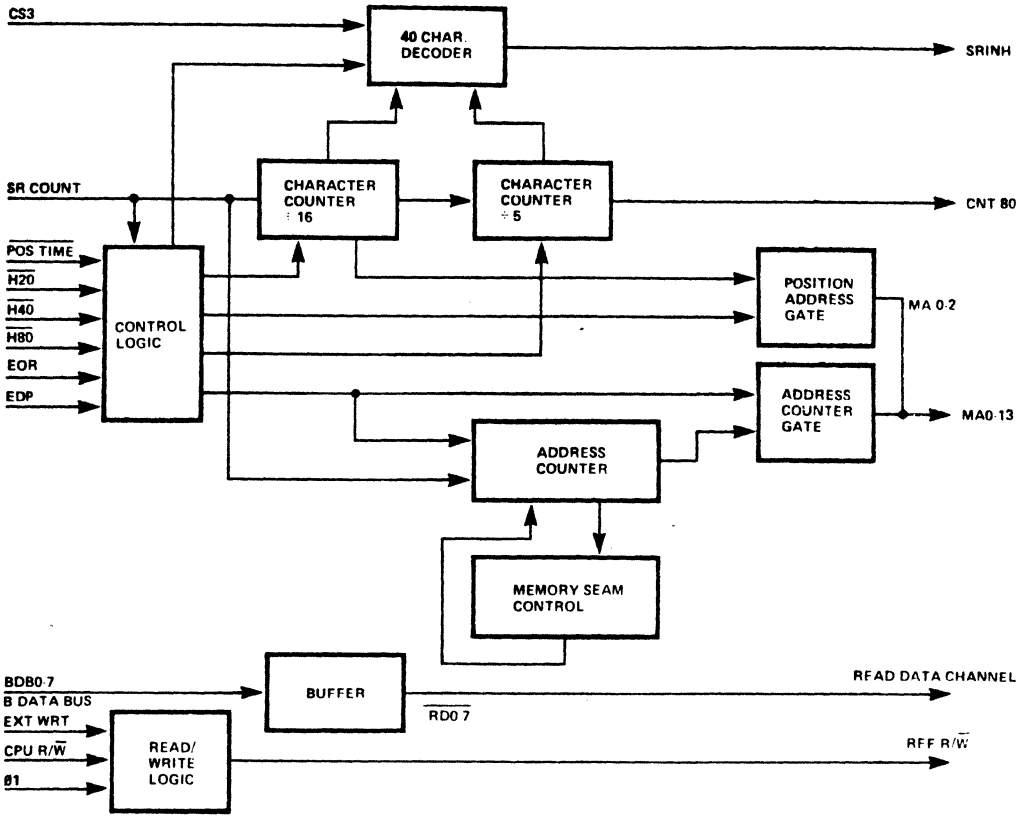


Figure 4-18. Refresh control card block diagram.

4.4.8 Refresh Control Card

Block Diagram Analysis. As shown by the block diagram, in Figure 4-18, the refresh control card consists of an address counter, a character counter and the logic needed to control their operation. Also included are buffers to drive the write inputs of the refresh buffer card from the B Data Bus, and logic to generate the MEMORY R/$\overline{W}$ control signal.

Whenever the refresh buffer takes a bus cycle, SR COUNT enables the two-stage character counter for 1 count. The first stage counts from 0 to 15 and supplies a carry output to the second stage. The second stage, preset to a count of ten at the end of every character row, counts 5 of the first stage carry outputs to generate CNT 80. The character counter thus counts the number of character positions in a row.

Outputs from the character counter are decoded in the 40 character decoder to generate an output at the 40th character position. This output is used only if the 40-character-per-row mode is enabled by $\overline{CS3}$. In this mode the shift register inhibit generator produces SRINH to disable the address gate during the last half of the character row. SRINH has no active part in the refresh control card operation in the standard 80-character-per-row mode.

At the end of each display page, the eight fixed positions in memory are updated. They are addressed by the first stage of the character counter. $\overline{UPDATE}$ presets this stage to a count of seven so that it can sequentially address the eight fixed positions via MA0-2. Outputs from the counter are gated to the MA Data Bus by SR COUNT and the Q output of the control flip-flop.

While loading the next line shift register on the refresh buffer card, the address counter gate is enabled, and the counter is incremented, by SR COUNT and the $\overline{Q}$ output of the control flip-flop. The address counter sequentially counts in blocks of 80 (e.g., 0-79, 80-159). In so doing, it supplies the address for the character to be loaded into the next line shift register on the refresh buffer card. If the top of memory (address $37{,}577_8$) is reached before the end of the display page, the memory seam decoder resets the address counter to the bottom of display memory (address $30{,}000_8$ for two pages of refresh or $34{,}000_8$ for one page). At the end of the page, the counter is initialized with page base data stored in locations $37{,}774_8$ and $37{,}775_8$. Page base defines the address of the first character in the display page.

Circuit Description. Refer to schematic diagram 96-457-01 , in Section 8, and to the timing diagram in Figure 4-17.

The character counter XB2 and XB1, counts a character position each time SR COUNT is high (refresh buffer has taken a bus cycle). While addressing memory to load the next line shift register, XB2 repeatedly counts from 0 to 15. On each 15th count, XB2 puts out a carry pulse to XB1-10. XB1 is present to a count of 10 at the end of each display row by a load pulse generated at XD1-6. XB1 consequently counts five XB2 carry outputs to provide the CNT 80 (5 x 16) signal at XB1-15. This signal is used by the refresh buffer card to inhibit SR COUNT.

XA2 decodes outputs from the character counter to set the SRINH generator (XA4-6) in the 40-character-per-row mode ($\overline{CS3}$ low). On the 40th character count, a low output at XA2-8 sets XA4-6 low. XA4-8 is high except when the last 8 locations in memory are being addressed during vertical retrace. XA4-6 remains low until cleared at the end of the character row (input on XC1-2) or the end of the page (input on XC1-13). Thus, SRINH is high during the loading of the characters for the first half of the character row, and low during the last half. When SRINH is low, XB4-3 and -6 are low to inhibit the address gates (XE3-XE6) and memory address counter XC3-6. If CS3 is high (80-character-per-row mode), XA4-6 remains high constantly, due to a continuous low input at XA4-10.

$\overline{\text{UPDATE}}$ at XC2-3 is a signal decoded from EOP (end of page) and the inputs to XC1. $\overline{\text{POS TIME}}$ is high during display time and low for 16 character periods at the end of each horizontal scanning in the character row. EOR (end of row) is high during position time at the end of every character row; EOP (end of page) is high during position time at the end of the last character row on the display. Thus, $\overline{\text{UPDATE}}$ is a pulse that starts 2.68 usec before the end of position time, and occurs once per frame during vertical retrace.

When $\overline{\text{UPDATE}}$ goes low, it presets the first stage (XB2) of the character counter to a count of 7 since XB2-3, -4 and -5 are high and XB2-6 is low. $\overline{\text{UPDATE}}$ also sets XA4-3 high.

XB2 then counts to 15 to address the eight fixed positions in memory along MAO-2 via position address gates XD2-3, -6 and -1, respectively. These gates are enabled by the high output at XB4-8, produced by SR COUNT and the high level on XA4-3. At the count of 15, the carry output from XB2 causes XA4 to change state. As a result, XB4-8 goes low to inhibit the position address gates.

Since SR COUNT is in sync with the trailing edge of Ø2, and is high for only one Ø2 pulse at a time, the address counter (XC3-XC6) counts one memory location at a time. The counter is loaded from the page base location in refresh memory during vertical retrace. XC3 and XC4 are loaded from location 37774_8, while XC5

and XC6 are loaded from 37775_8. Load pulses are supplied via XA3-11 and -8, respectively, by a decoding of the correct counts of the character counter (XB2) an< XA4 pin 3 being high.

If the end of memory address (memory seam) is reached before the end of the page, the seam is decoded in XB5-8 and XB6-8. When the seam is decoded XB6-8 gets low, which resets XC3 and 4 to zero. If jumper E1-E2 is not installed, XC5 is set to zero and the resulting address is $30,000_8$. If E1-E2 is in place, XC5 i: set to binary 1000 and the resulting address is $34,000_8$. Note that XC6 had to be set to binary 0011 (LLHH) to enable XB6.

When the end of memory address (37677_8) is reached it is decoded in XB5-8 and XB6-8, making XB6 pin 8 low, resetting XC3 and XC4 to address $30,000_8$. Note that, in a 12-line-per-page terminal, this causes the second half of the screen to be loaded from nonexistent memory. That is, all nulls are loaded and the bottom half of the screen is blank.

Note that page base data (addresses $37,774_8$ and $37,775_8$) does not have to be located at $30,000_8$ but can be stored at any location in refresh memory. During update at the end of the display page, the counter is loaded with page base data via RMO-7. At the count of 10 in the character counter's (XB2) update cycle, the level at pin 8 of XD1 goes low and is OR-gated as a high input to XA3-10. Since bit A in the XB2 output is low at the count of 10, XA3-8 goes low to load one byte of page base into XC5 and XC6. At the count of 11, bit A goes high. Consequently, XA3-8 goes high and XA3-11 goes low to load the second byte of page base into XC3 and XC4.

The remaining circuit on the refresh control card generates REF R/$\overline{W}$. This signal is CPU R/$\overline{W}$ or EXT WRT clocked with Ø1. EXT WRT is used by an external device to write data into memory.

4.4.9 Cursor Control Card

The cursor control card defines the position on the CRT display at which the next character is to appear. It also generates the audio indicator signals (click and beep) used in the 8025 CRT Terminal and provides the interface between the keyboard and the A Data Bus.

Block Diagram Analysis. A simplified block diagram of the cursor control card is shown in Figure 4-19.

In addition to the cursor control circuitry, the cursor control card contains the keyboard interface and repeat circuit, as well as the circuit used for audio indications (click-beep).

A $\overline{DSO}$ (data strobe out) signals the keyboard interface that the keyboard wants to send a character. When a POLL IN is received the interface selects itself for the next data transfer to the CPU and gates the interface address onto the A Data Bus. The CPU responds with an IOD signal that enables the gate to transfer the keyboard data to the A Data Bus. $\overline{IOD}$ also generates $\overline{OE}$ (output enable). $\overline{OE}$ signals the keyboard that the data was transferred, and the keyboard removes the $\overline{DSO}$ to reset the interface control logic.

Removal of DSO also triggers a one-shot that produces a 0.5-second pulse. If another data transfer has not occurred, the enable flip-flop is set to enable a 15 Hz multivibrator that, in turn, triggers a three-stage shift register.

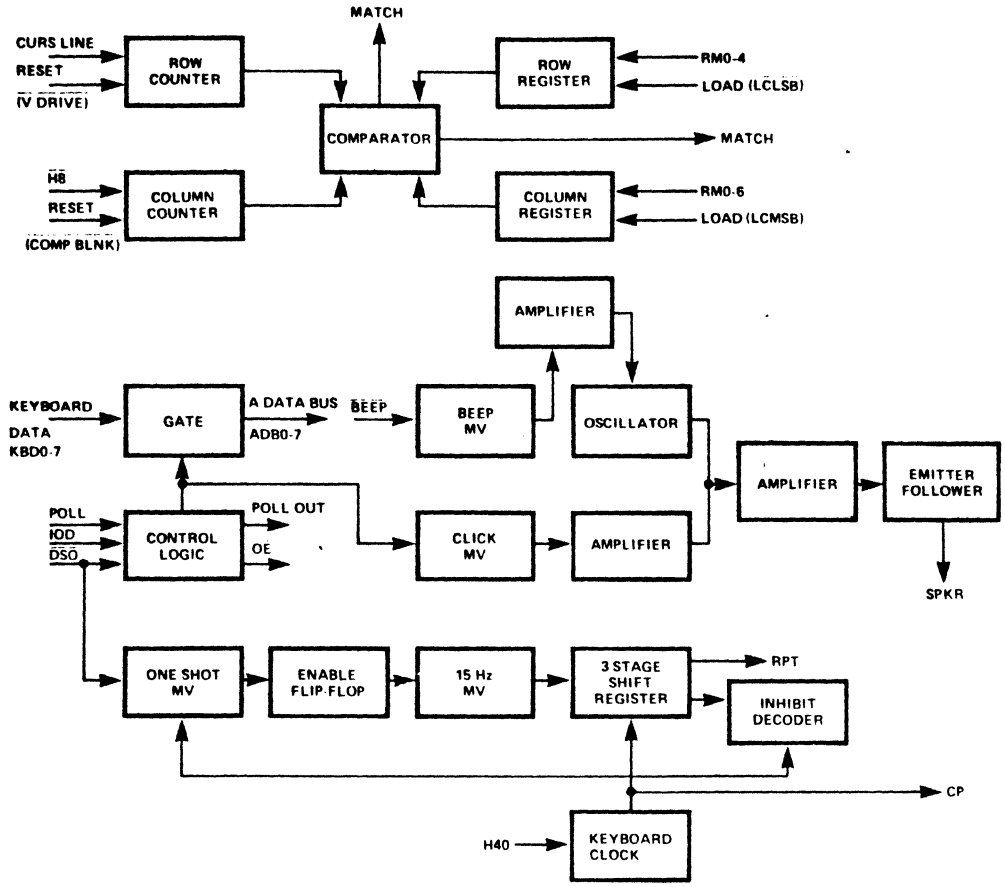


Figure 4-19. Cursor control card block diagram.

One output of the register is the RPT (repeat) rate signal. Triggering of the one-shot is inhibited by another output from the register. If the key for the last character transferred is still depressed after two $\overline{CP}$ periods, the keyboard responds with a new $\overline{DSO}$ and the character will be repeated approximately 15 times per second until the key is released. The enable flip-flop is reset to disable the RPT signal when a key is not depressed for more than two $\overline{CP}$ periods.

The click-beep circuit provides acoustic feedback to the terminal operator. The control logic output that enables the KDB-to-ADB gate also triggers the click multivibrator. The pulse output from this one-shot is amplified to drive a speaker mounted on the keyboard. The click one-shot is triggered every time a key on the keyboard is depressed.

A programmable beep feedback is controlled by the $\overline{BEEP}$ input to another one-shot multivibrator. The output pulse from this one-shot is amplified to turn an oscillator on for the duration of the pulse. The oscillator output is amplified so that it can drive the keyboard-mounted speaker.

Cursor control circuitry defines, for the video control card, where the character will be displayed. The row and column counters count in synchronization with the CRT sweep to specify the current position of the CRT beam. The row and column registers contain the cursor position as specified by the refresh memory on RM0-6. Outputs from the counters and corresponding registers are compared. When these are equal, the comparator sends a MATCH signal to the video control card.

Circuit Description. Refer to schematic diagram 96-376-01 in Sectio

The cursor control circuit consists of a row counter (XE6 and XC3), a column counter (XD6 and XC6), a row register (XE4 and XC3), a column register (X and XC4), and a comparator (XC5, XD5, and XE5). The counter is synchronized tc the video sweep; the register contains the desired cursor position on the CRT as defined by the refresh memory. Cursor position specifies where the cursor is tc be displayed on the CRT.

The row counter (XE6, XC3) counts CURS LINE signals generated on the Timing Control Card and starting at the beginning of every tenth scan line in a character row. $\overline{\text{V DRIVE}}$ resets XE6 and XC3 at the end of each frame. The column counter (XD6, XC6) counts $\overline{\text{H8}}$ clock pulses that occur at the character rate, and $\overline{\text{COMP BLNK}}$ resets XD6 and XC6 at the end of each scan line. Since these two coun ters are synchronized with the video sweep, their outputs define the current pos tion of the beam on the CRT.

The cursor position registers store the row and column coordinates spe fied by the refresh memory and thus specify the desired position for the cursor. Cursor row and column coordinates, loaded into the refresh memory are in two of the eight fixed positions. XE4 and XC3 store the row data. XD4 and XC4 store the column data. Data is loaded into these two registers at the end of each page by $\overline{\text{LCLSB}}$ and $\overline{\text{LCMSB}}$, respectively, during update time.

Twelve exclusive NOR gates (XC5, XD5, and XE5) function as the comparat The top five gates compare row information while the bottom seven compare column information. When all counter outputs are equal, the comparator produces a high output (MATCH).

The keyboard interface circuitry consists of the KBD-to-ADB gates with their related control logic, a POLL gate, and a repeat signal generator. The sequence by which data is transferred from the keyboard to the A Data Bus is initiated by $\overline{\text{DSO}}$.

The control logic includes three R-S flip-flops made up of the followin components: XC1-3 and XC1-6; XB2-3 and XC2-8; and XB2-8 and XB2-11. With $\overline{\text{DSO}}$ and POLL IN high, XC1-1, -2, XC2-9, -10, and XB2-12, -13 are low; XC1-4, -5, XB2-1, - and XB2-9, -10 are high. These conditions also exist after reset.

Assuming that $\overline{\text{DSO}}$ is high, the output of the first flip-flop (XC1-3) is high, partially enabling the POLL OUT gate (XB1-6). When POLL IN goes high, the level change at XC1-11 does not alter the state of the first flip-flop. Since the POLL IN is high at XB1-4, the POLL OUT gate is enabled and the POLL signal is propagated down the bus.

If $\overline{\text{DSO}}$ goes low in the absence of a POLL IN, XC1-1 and XC1-9 go high to set the first flip-flop, and the output of XC1-6 goes high, partially enabling the XB1-3 AND gate. Arrival of a POLL IN is AND-gated by XB1-3 to: (1) set the second flip-flop, partially enabling the XB2-6 NAND gate at pin 4 (the keyboard interface is now selected for the next data transfer); and (2) place the address 001 (LLH) on $\overline{\text{ADBO}}$ by causing XB3-11 to go low. POLL IN is also inhibited from further propagation down the bus, since the POLL OUT gate was disabled when the first flip-flop was set.

After the CPU receives the address, it responds with an IOD that enables the XB2 NAND gate at pin 5. The resulting low output at XB2-6 is inverted by XD3-6 to gate the keyboard character to the A Data Bus.

IOD, via XB2-6, also sets the third flip-flop to produce $\overline{OE}$ which indicates to the keyboard card that the data was transferred. The keyboard card responds by removing $\overline{DSO}$, which, in turn, resets the three flip-flops.

Should $\overline{DSO}$ arrive while POLL IN is present, the former cannot initiate selection of the interface because the low at XC1-10 will not allow the first flip-flop to be set. The POLL IN will thus be propagated down the bus. Since $\overline{DSO}$ cannot be removed without an $\overline{OE}$, it will be available to start the selection process once POLL IN goes high.

A $\overline{DSO}$ on arrival is also differentiated by C18 and R6 to trigger an 0.5 second retriggerable one-shot (XD1). Should another $\overline{DSO}$ arrive before the 0.5 second period elapses, the output pulse of XD1 is extended. If another $\overline{DSO}$ has not occurred, the output at XD1-4 sets flip-flop XD2 0.5 second after $\overline{DSO}$. The resulting output at pin 6 of XD2 enables multivibrator XE1, which oscillates at 15 Hz as determined by R31, C26 and R32, C27. XE1 triggers a three-stage shift register (XD2, XE2), which is clocked by H40 (5.36 usec). The output on XD2-9 is the RPT signal for the keyboard card. If a key on the keyboard is still depressed, the keyboard card responds with another $\overline{DSO}$ two clock pulses later.

The outputs of the second and third stages of the register (XE2-9 and -6) are decoded by NAND gate XC2-3 to inhibit triggering of XD1 during the two-clock-pulse period. If $\overline{DSO}$ occurs at the end of two clock pulses it indicates that the key is still depressed, and the last character transferred is repeated approximately 15 times per second until the key is released. Should more than one key be depressed at the same time, a 0.5-second delay occurs after each key depression, and the repeat function operates on the last key depressed. Absence of $\overline{DSO}$ after the two-clock-pulse period indicates that the key has been released. The resulting low output at XB1-11 clears XD2 at pin 1. Consequently XD2-5 goes low to preset the Q outputs of the shift register and drive XE2-6 low. XD2 is also reset at pin 1 with every $\overline{DSO}$.

A dual one-shot (XA1), a dual operational amplifier (XA4)--with one section operating as an oscillator and the other as an amplifier--and Q1 through Q5 make up the click-beep circuit.

The click portion of the circuit is activated whenever the KDB-to-ADB gates are enabled. In addition to enabling the gates, the high output at XD3-6 is applied at XA1-10 to trigger the corresponding one-shot.

The triggered one-shot generates a single 450-usec pulse (as determined by R4 and C17) at XA1-5. This pulse, coupled to the base of Q2, turns Q2 on for 450 usec and the resulting negative-going pulse at the collector goes to pin 1 of XA4. This section of XA4 amplifies the pulse and applies it to Q5, an emitter-follower, which provides a low source-impedance for driving the keyboard-mounted speaker.

The beep section of the circuit is enabled with a $\overline{\text{BEEP}}$ input at XA1-1, to the other one-shot. $\overline{\text{BEEP}}$ is programmable to provide an audio indication of a given event within the terminal. The beep one-shot generates a single pulse approximately 45 msec in duration (as determined by R3 and C16) at XA1-13. The pulse, coupled to the base of Q1, turns Q1 on for 45 msec. With Q1 on, the oscillator section of XA4 is enabled, and a 1,500 Hz output at XA4-10 is applied to XA4-1. The amplified output at XA4-12 is then applied to emitter-follower Q5.

R25 in the XA4 amplifier circuit varies the volume of the audio output while Q3 and Q4 squelch the audio.

4.4.10 Video Control Card

The video control card interprets ASCII characters from the refresh buffer card and converts the data into a usable video signal for the CRT display. It also includes circuitry to control and modify the video display.

Block Diagram Analysis. As shown by the simplified block diagram in Figure 4-20, display characters are stored in the character generator ROMs, and each character to be displayed is selected by the corresponding 8-bit ASCII code on CG0 through CG7. The line to be displayed is specified by V1, V2 and V4. A parallel-to-serial converter serializes seven bits out of the character generator at the video rate (HF CLK) and applies the output to two video mixer-amplifier channels. One channel feeds the CRT display; the other combines video and composi sync signals to supply a composite video signal for an external display.

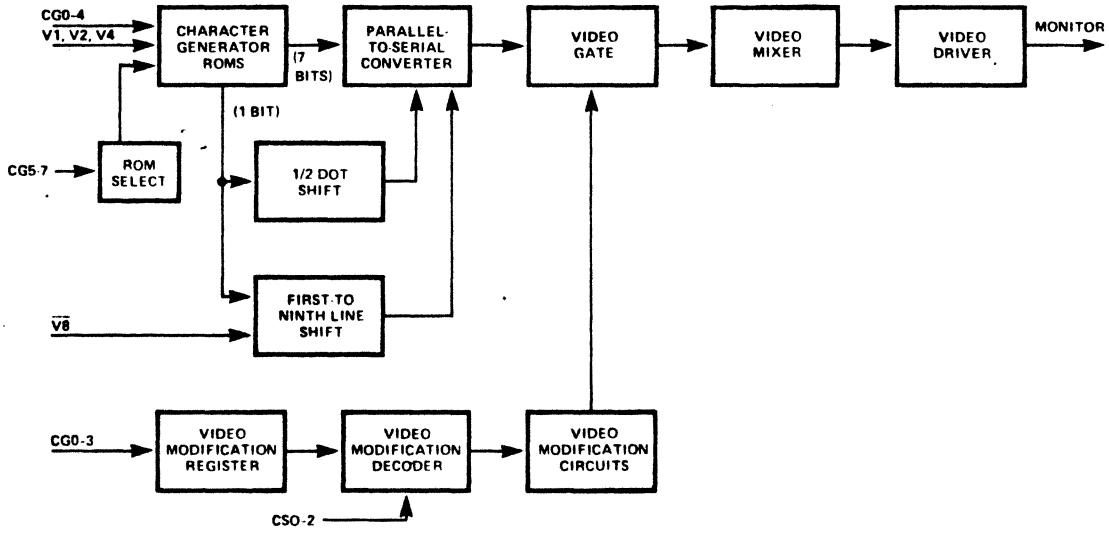


Figure 4-20. Video control card block diagram.

The eighth bit (or control dot) from the character generator controls the half-dot shift circuit and the first-to-ninth line shift circuit. The former provides for more natural looking characters and the latter produces decenders on lower-case characters.

Video modification codes on CG0 through CG3 are stored in the video modification register, the output of which is decoded along with the video status bits (CS0-2) in the video modification decoder. The output of the decoder drives video modification (e.g., blink) circuits to modify the video as required.

Circuit Description. Refer to schematic diagram 96-454-01 in Section 8.

Up to four character-generator ROM chips (XA2, XA4, XA5, and XA6) may be installed on the video control card. Two (XA2 and XA4) are installed in this terminal. XA2 contains the ASCII 64-character set (upper-case letters, numerals, and punctuation) and XA4 contains lower-case and control characters.

The ROMs are addressed by CG0-7, $\overline{V1}$, $\overline{V2}$, and $\overline{V4}$. The character to be displayed, as defined by the 8-bit ASCII code (see Section 10), comes in from the refresh buffer card on CG0 through CG7. The line in the character row to be displayed is defined by $\overline{V1}$, $\overline{V2}$ and $\overline{V4}$ from the timing control card.

CG5, 6 and 7 select the character-generator ROM by enabling it for a readout. A ROM is enabled under conditions (see Table 4-6) that drive E1 low and E2 high.

A review of the ASCII Standard chart in Section 10 will show that the CG5, 6, and 7 bits for columns 2 through 5 meet the selection criteria for XA2, and the bits for columns 0, 1, 6, and 7 meet the criteria for XA4.

Table 4-6. Character generator ROM selection.

ROM ENABLED	ROM INPUT	
	E1	E2
XA4	CG5 & CG6 = both L or both H and CG7 = L	XD5 - 6 = H
XA2	CG7 = L	CG5 = H or CG6 = H (but not both)

When line and character information are applied to a ROM that is enabled, it puts out character data in parallel form. The outputs of both ROMs (O_1 through O_8) are wired in parallel. XB2, a parallel-to-serial converter, serializes the first seven bits of the character-generator output at the video rate (14.976 MHz). XB2 is clocked (or shifted) by HF CLK through exclusive OR gate XE2-8 and data is loaded into XB2 by the output of XE4 (pin 6).

Pin 6 of XE4 goes low with the negative-going edge of the $\overline{\text{SET LDFF}}$ signal, which coincides with the positive-going edge of H8 (the end of the eighth dot in the dot matrix). Pin 6 goes high on the next positive-going edge of HF CLK. The clear function on XE4-1 is an overriding clear.

The eighth dot (O_8) from the ROM is used to control shifting and the inhibiting of XB2. A shifting delay changes the position of character dots within

the display matrix. Inhibiting XB2 prevents loading of data. Bit O_8 is applied t both pin 13 on flip-flop XD6 and pin 4 of XE6 (an exclusive OR gate). XD6-15 controls the phase of HF Clock applied to XB2 and hence the position of the character dots. The output of XE6-6 controls whether the contents of the ROM for the first line of data is displayed during the first or the ninth line of the character row.

If O_8 is low, it sets the fourth flip-flop in XD6 to place a high input on XE2-10. Since the output at XE2-8 is low when both gate inputs are high, HF CL is shifted 180°. This means that HF CLK, whose period corresponds to one dot in t character matrix, is shifted one-half dot. Thus, video data out of XB2 is shifted one-half dot position. The fourth flip-flop in XD6 changes state on the next negative-going edge of H8, providing O_8 of the next character in the row is not low.

Should O_8 be low in the first scan line, the video information in that line will be displayed in the ninth scan line. This is accomplished by inhibiting XB2 during the first line and allowing first-line data to be displayed during the ninth line.

Inhibiting of XB2 is done by the logic associated with the clear input to XE4 (pin 1). As shown, XE4 can be inhibited by the combination of O_8-V8 (XE2-4, -5) and V1-V2-V4 (XC6-9, -10, -11), the latter signals being inverted by XB6 from $\overline{V1}$, $\overline{V2}$, and $\overline{V4}$ respectively.

V1, V2 and V4 are low for the first (L_0) and ninth (L_8) lines in the character display matrix. Thus, XC6-9, -10, and -11 are low during L_0 and L_8 to produce a high input to XE6-13 that partially enables XE6 during these two lines. V8 is high for matrix lines L_0 through L_7, so that XE6-6 is high during these lines when XE6-4 is low. Thus, NAND gate XE6-11 is enabled only when O_8 is low in L_0 and L_8 (with respect to data, L_0 and L_8 are identical).

During L_0 the low output of XE6-11--670 nsec in duration--is NOR-gated through XC3-12 and inverted by XE5 so as to apply a low clear input to XE4-1. This sets XE4-6 high to inhibit loading L_0 data into XB1. At the beginning of L_8, however, $\overline{V8}$ goes low and, coupled with a low O_8, provides a low output at XE2-6 to permit loading L_0 data into XB2. The sequence just described occurs only for lower-case characters with descenders.

For upper-case characters and for lower-case characters without descenders, L_8 must be inhibited since in both types of characters O_8 is never low in the first matrix line. Thus, the high input at XE2-4 is gated to XE6-12 to enable the latter gate.

The $\overline{\text{INH LD}}$ input to XC3-13 is not used and is therefore held at a constant high level.

(NOTE: Jumper E3-E4 is omitted only for certain custom options.)

The output of XB2 goes to XC2-10, and the video signal is gated on HF CLK to pins 12 and 13 of XC2. Assuming BLINK is not present, XE3-11 stays low and the video signal is gated to XE2-13. If a reverse video signal is not present, the video signal is gated through XE2 and XD1 to the video mixer.

Video at the mixer (R13, R17, R18) can be blanked and changed in intensity. Output signals from the mixer are direct-coupled to emitter follower Q3 which drives the CRT video amplifier section via J1-6.

In some terminals, composite video signals are provided by Q1, Q2, and Q4. The composite sync signal from the timing control card is amplified by Q4, coupled through CR5, and added to the video in a second mixer consisting of R8, R9, and R12. The resulting composite video signal is amplified by Q1, Q2, and is made available at J2-1 and a BNC connector on the rear of the terminal.

If the most significant three bits of the character code are 100 (i.e., HLLXXXXX), the character is a nondisplayable video modification character. This kind of character specifies some modification to be made to the video presentation until either the next video modification character or the end of the line occurs.

The modification character format is HLLXXYYY, with YYY defining the modification (e.g., reverse video, blink, etc.). The XX portion is available for defining software functions (e.g., define protected fields). Modification codes and their functions are given in Table 4-7.

Video modification codes on CG0 through CG2 are stored in XC4, a type 74175 flip-flop. XC4 is loaded by LOAD F, which is generated on the refresh buffer card when a 100 (HLL) is decoded in the most significant three bits out of the refresh shift register. $\overline{\text{CLR F}}$, also generated on the refresh buffer card, clears XC4. Table 4-7 shows the XC4 input and output levels for the various video modification functions.

Table 4-7. Video modification register (XC4) input-output parameters

XC4 INPUTS			VIDEO MODIFICATION	XC4 OUTPUTS				
CG2	CG1	CG0		$\overline{1Q}$	2Q	$\overline{2Q}$	3Q	$\overline{3Q}$
L	L	L	Normal Display	H	L	H	L	H
L	L	H	Video Off	L	L	H	L	H
L	H	L	Underline	H	H	L	L	H
L	H	H	Reverse Video	L	H	L	L	H
H	L	L	Dim Normal	H	L	H	H	L
H	L	H	Dim Reverse	L	L	H	H	L
H	H	L	Blink Normal	H	H	L	H	L
H	H	H	Blink Reverse	L	H	L	H	L

The blink function is generated by decoding 2Q, 3Q, and the BLINK signal at XC3-8. With 2Q and 3Q (XC3-10 and -9, respectively) high, XC3 is enabled when XC3-11 is high. BLINK occurs 2.5 times per second. The resulting high output at XE3-10 inhibits XE3-13 25% of the time to produce a blinking video display. Reverse blink occurs in the same manner if the reverse video function enables XE2-

Reverse video is produced with $\overline{1Q}$ low. With XE2-12 low, the exclusive OR gate does not invert the output (pin 13) of XE3. Thus, the output at XD1-6 is inverted with respect to the output of XB2 and the video display shows up as black on a white field.

The dim function results from decoding $\overline{2Q}$ (XD3-12) and 3Q (XD3-13). When both of these are high, the low level at XD3-11 is NOR-gated to XD1-9 (an open-collector gate) to turn it on. Turning XD1 on places R19 in the video mixer network and R19 thus reduces the video voltage to produce a dim character. Dim reverse is accomplished in the same way when the reverse video function is present

Underline is generated by decoding $\overline{1Q}$ (XD4-2), 2Q (XD4-1), and $\overline{3Q}$ (XD4- in XD4. With all three signals high, XD4-6 is partially enabled and then fully en abled when CURS LINE is high, during the ninth scan line (L_8) of the character. T resulting low-level at XD4-6 is NOR-gated to XD3-3, whose output is inverted by XD to apply a low level on XD1-4. This low level holds XD1-6 high (video on) for the duration of CURS LINE.

Video off is controlled by $\overline{1Q}$ (XC5-11), 2Q (XC5-10), and 3Q (XC5-9). With all of these low, the resulting high at XC5-8 is NAND-gated to a low level at XE1-8. This level clamps the video signal at the mixer network to ground and caus the CRT screen to go blank.

Blanking is also performed by the output at XE1-3, which is controlled by the $\overline{\text{COMP BLNK}}$ and $\overline{\text{BLANK}}$ inputs. The video is blanked when either or both of these inputs are low.

The cursor function involves the logic whose inputs are $\overline{\text{CS1}}$, $\overline{\text{CS0}}$, MATCH and RATE. XD4-8 is low when MATCH (from the cursor control card) is high, video status bit $\overline{\text{CS1}}$ is high (underline cursor on), and $\overline{\text{H10}}$ is high during L_8 (CURS LINE) of the character. This low level is inverted by XD2-12, partially enabling XD5 at pin 1 and XD1 at pin 12. XD5 and XD1 are thus turned on and off at a 5 pps rate by the RATE signal on XD5-2 and XD1-13, respectively. With XD2-12 high, XD5-3 is high (off), XD1-11 is on, and XD1-8 is off during the low half of RATE. The result ing low level at XD1-11 puts R19 in the video mixer network to dim the display. Du ing the opposite phase of RATE, XD5-3 is low while XD1-8 and XD1-11 are high. The low level at XD5-3 also causes XE1-6 to go high. With XD1-8 and XE1-6 high, the video voltage can rise to a full 5 volts to produce an intensified video. Even wit reverse video the cursor will not be lost, since it blinks from dim to bright.

A blinking block cursor can also be generated by gating a low $\overline{\text{CS0}}$ (block cursor on) at XD3-9 to XD4-9. $\overline{\text{H10}}$ is high for each scan line in the character matrix. Hence, the cursor gates function as described in the preceding paragraph during the entire character matrix period to produce a blinking (dim to bright) block.

The remaining logic on the video control card blanks control characters and nulls.

Control characters (e.g., ACK, BEL and CR) are blanked by not reading them out of the character generator ROM (XA4). CG5, 6, and 7 are low bits in the ASCII control-character codes (see Section 10), and they are applied to pins 4, 3, and 5, respectively, of XC5. With these three bits low, XC5-6 is high, partially enabling XD5 at pin 5. If the video status bit (CS2) is high, the low level at XD5-6 disables XA4 at pin 19 and XA2 at pin 20.

Nulls are blanked when the output at XD6-3 is high. This occurs when XC6-6 and XC5-6 and -12 decode a null (all levels low) on CG0-7. Note that XE4-8 and XC6-5 are low during the display time ($\overline{\text{CLR F}}$ is high). A high level at XD6-3 is NAND-gated to a low level at XE1-11 that clamps the video signal to ground.

4.4.11 The Keyboard

The keyboard is the interface between the terminal and the operator. It converts key depressions into terminal "language" and provides visual indications of terminal status. In addition, the on/off and brightness controls are located on the keyboard, as is the speaker that produces the audio indications.

Block Diagram Analysis. As shown by the block diagram in Figure 4-21, the encoder acts as an interface between the keyboard and keyboard data bus (KDB0-8). It translates X-Y coordinates of the keyboard matrix into ASCII characters and control codes. Within the encoder, an integrated circuit, are found the logic and storage capability needed to perform the translations.

The encoder supplies a pulse train to the X lines in the matrix. When a key is depressed to connect the X output to the Y input of the encoder, the X-Y coordinates in the matrix are defined. The encoder decodes the coordinates, converts them into 8-bit ASCII encoded on KDB0-7, and supplies a $\overline{\text{DSO}}$ (data strobe out) signal to the keyboard interface on the cursor control card. When the data is transferred, the keyboard interface on the cursor control card sends a $\overline{\text{OE}}$ (output enable) signal to the encoder, which resets the strobe and enables the encoder for the next key depression. The RPT input causes the encoder to repeat the last character transferred if the key is depressed for more than 0.5 second.

Shift and control inputs to the encoder determine to which of four different codes the X-Y coordinates will be converted. The shift input by itself performs the same function as the shift key on a typewriter.

Inputs from the LED (light emitting diode) latch on the refresh buffer card drive LED indicators on the keyboard to indicate terminal operating modes and status.

Circuit Description. Refer to schematic diagrams 96-453-XX and 96-393-XX in Section 8.

The keyboard card consists of a 9 x 10 X-Y key switch matrix, shift and control key switches and a keyboard encoder.

The X-Y matrix consists of 90 SPST switches that are actuated by keys on the keyboard. A diode is connected in series with each switch to prevent sneak paths in the matrix when three or more keys are depressed simultaneously. When a key is depressed, one of nine X lines is connected to one of the ten Y lines to define the X-Y coordinates for the encoder.

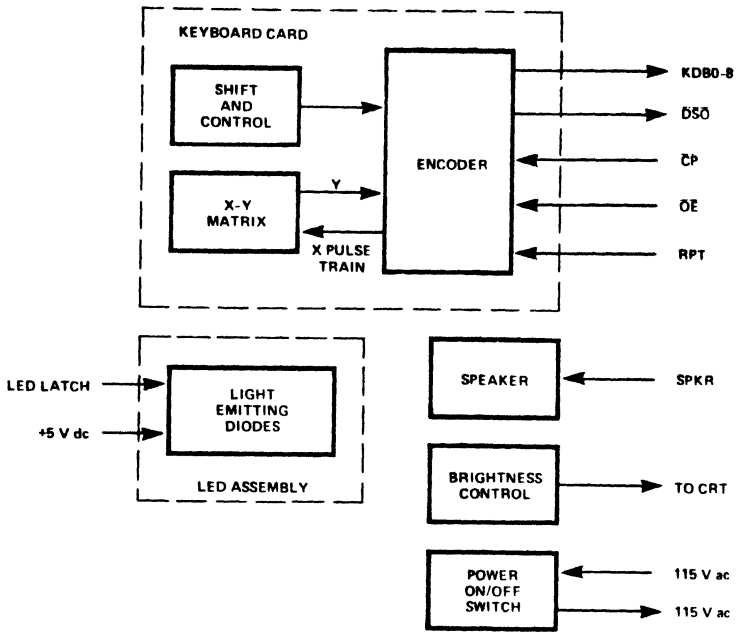


Figure 4-21. Keyboard block diagram.

In the 12 line display terminal, X-Y matrix switches 58 through 69 are omitted. Table 4-8 defines the active keys and their functions.

NOTE: Unused keys are still active, but are inhibited by software.

A series of pulses, generated by the encoder chip, is sequentially applied to the X lines, and the Y inputs to the encoder are serially gated. Thus, each line can be detected individually. When a key is depressed (switch closure), an X driver in the encoder is connected to a Y decoder, and the corresponding X-Y coordinates are determined.

The X-Y coordinates are decoded in the encoder and converted to an ASCII 8-bit code by a ROM in the encoder. Each X-Y coordinate can be converted into four different codes through the use of the shift and control keys. Mode logic within the encoder serves as an interface between these keys and the ROM.

Shift and lock (switches 2 or 13 and 15, respectively) perform the same function as the shift and lock keys on a typewriter, (i.e., shift from lower-case to upper-case characters). The ASCII control code is generated when the control key (switch 29) is depressed. Depressing both shift and control keys generates additional codes.

After the ASCII code is generated, the character is stored on KDBØ-8 via an output buffer in the encoder and the encoder sends a $\overline{DSO}$ signal (pin 9 of J71 goes low) to the keyboard interface on the cursor control card. When data on KDBØ- is transferred to the A Data Bus by the keyboard interface, it sends an $\overline{OE}$ signal to the encoder via J71, pin 13. $\overline{OE}$ resets the strobe circuitry and enables the output buffer circuitry for the next key stroke.

Table 4-8. X-Y matrix switches and their functions.

(24 line display terminal)

SWITCH NUMBER	FUNCTION
2, 13	Shift
14	Tab
15	Lock
28	Line feed
29	Control
42	Delete
43	Carriage return
57	Escape
58 - 69	Numeric pad
70	Not used
71, 73-75, 77	Cursor control
72	Not used
76	Cursor control
78	Not used
79-82, 85, 86	Special functions
53, 84	Not used
87 - 94	Special functions
Remainder	Alphabetic typewriter keys

(12 line display terminal)

SWITCH NUMBER	FUNCTION
2, 13	Shift
14	Tab
15	Lock
28	Line feed
29	Control
42	Delete
43	Carriage return
57	Escape
58 - 69	Omitted
70	Not used
71, 73-75, 77	Cursor control
72	Not used
76	Cursor control
78	Not used
79-82, 85, 86	Special functions
53, 84	Not used
87 - 94	Special functions
Remainder	Alphabetic typewriter keys

NOTE: Unused keys are still active, but are inhibited by software.

Any number of keys can be struck almost simultaneously and the encoder will "remember" the order in which they were depressed. This means that the operator can depress a second, third, or more keys before releasing the first, and all characters will still be displayed in the order in which the keys were struck. This feature is called "N key rollover".

If a key is held down for more than 0.5 second, RPT (repeat) signal on pin 12 of J71 causes the encoder to repeat the last character transferred at the rate of about 15 times per second until the key is released. If more than one key remains depressed at the same time, the 0.5-second period begins after each keystroke. RPT, however, operates on the last keystroke.

The LED assembly can accommodate up to 16 light-emitting diodes (CR1-16) These are used to provide visual keyboard indications of terminal status and/or operating modes. A LED is activated whenever a LED latch buffer on the refresh buffer card applies a low level to the LED cathode. The diodes installed and their corresponding indications are listed in Table 4-9.

Table 4-9. LED keyboard indicators.

DIODE	ON/OFF STATE INDICATION	KEY ILLUMINATED
CR1	On: parity error in received data Off: no parity errors	RECV PARITY ERROR
CR2	On: terminal busy Off: terminal available	KEYBOARD DISABLED
CR3-5	Not used	---
CR6	On: KSR transmission mode Off: terminal not in KSR mode	KSR MODE
CR7	On: data from auxiliary storage is arriving at terminal Off: auxiliary storage not connected	STORAGE TRANSMIT
CR8	On: terminal is receiving data and transmitting it to aux. storage Off: store input function inactive	STORE INPUT
CR9-13,15,16	Not used	---
CR14	On: local copy on (half-duplex) Off: local copy off (full-duplex)	LOCAL COPY

4.4.12 RS-232 Interface Card

The RS-232 Interface Card provides the input/output interface between the 8025 terminal and external devices. It (1) converts parallel data from the CPU to serial form for transmission, (2) converts received serial data to parallel form for the CPU, and (3) controls data flow in and out of the terminal.

Block Diagram Analysis. As shown by the block diagram in Figure 4-22, the interface card consists basically of a receiver-transmitter that is controlled by RS-232 control, clock, interface control, word length selector, and parity control circuits. Gating logic, a command decoder, a status register, and a master reset circuit complete the card.

The master reset circuit clears the card to begin operation by clearing the receiver-transmitter logic and resetting the status register. Reset is initiated by a CPU read status command, (MA1-4 and STAT), a decoded CPU set status command (MA0, 5-7) or a power-on clear (POC) signal when terminal power is turned on.

The IC receiver-transmitter performs data conversions. Parallel data from the CPU on MA0-7 is converted into serial form by the transmitter and then applied to the RS-232 transmit control. From there, the data output (BA) goes to an RS-232 connector on the rear of the terminal. A break circuit, activated by the CPU, places a space level on the BA line to interrupt the external device. Serial data (BB) from the modem is applied to the RS-232 receive control. From there, the data goes to the receiver, where it is converted into parallel form, and is then placed on the A Data Bus through the data gate. Word length (5, 6, 7, or 8 bits) is established by the word length selector.

The receiver-transmitter also generates overrun, framing, and parity error signals. Latched error signals are gated by the error gate to the A Data Bus. Even, odd, or no parity is selected by a switch located on the rear panel of the terminal.

Clock signals (UA CLK) for the receiver-transmitter are derived by counting down the RS CLK input from the Timing Control Card, UA CLK provides a clock frequency that is determined by the rate selector.

The interface control circuit accepts inputs from the receiver-transmitter, CPU, and modem to produce enable signals for the data, error, and address gates. One output controls transmitter loading.

The data gate, enabled by the interface control circuit, gates received data to the A Data Bus ($\overline{ADB0\text{-}7}$).

Parity, framing, and overrun error signals are gated to the A Data Bus ($\overline{ADB5}$, $\overline{6}$, and $\overline{7}$) by the error gate. These three signals are included in both status and poll address bits. That is, error signals are gated to the A Data Bus in response to a read status command and a POLL. The error gate is enabled by the AND-gated combination of STAT and the address comparator output for a read status command. For a POLL, the gate is enabled by the interface control circuitry.

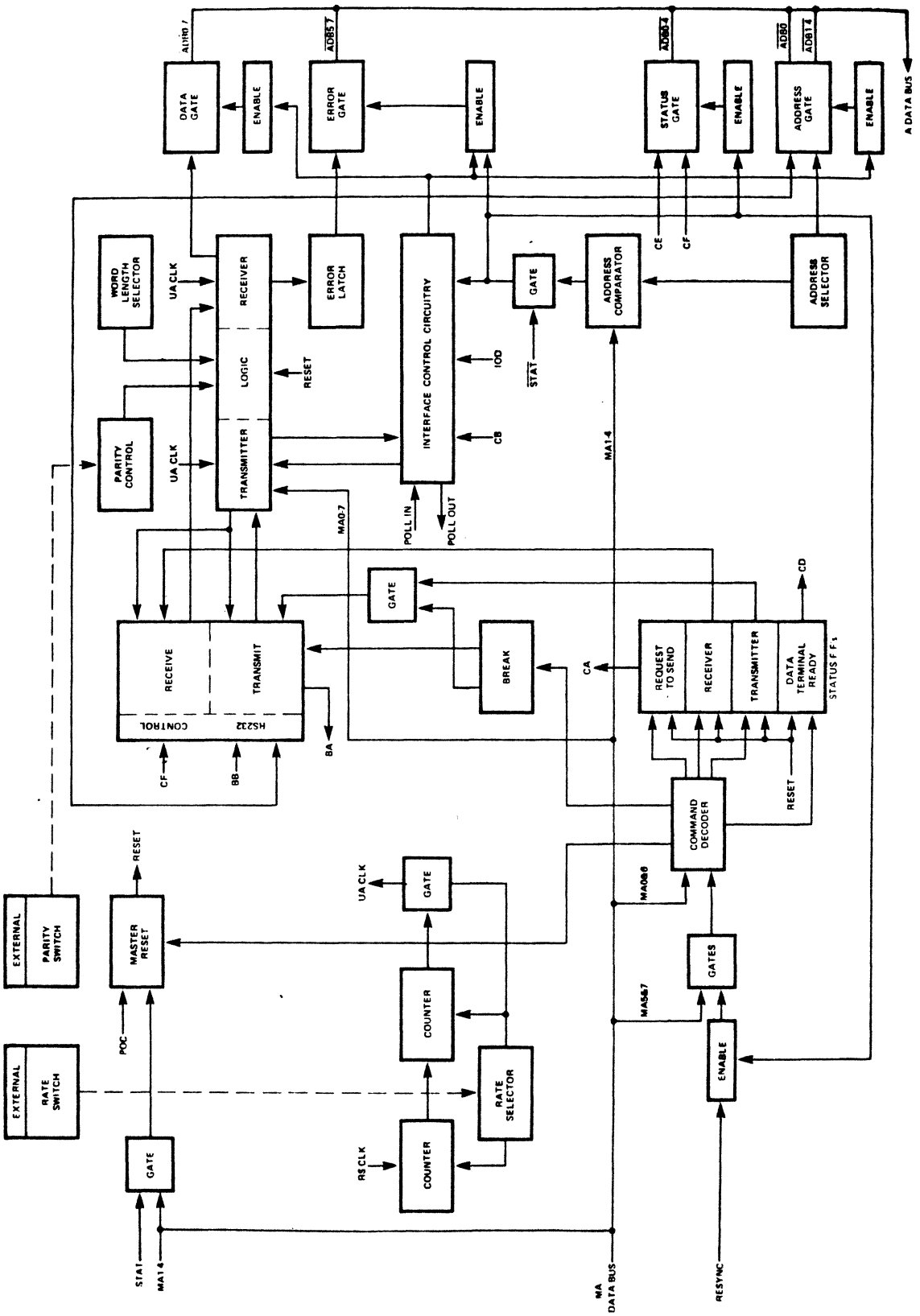


Figure 4-22. RS-232 Interface card block diagram.

Device status information is placed on the A Data Bus ($\overline{ADB0-4}$) by the status gate. Status bits, in addition to the error signals are: CF (received line signal detector) on $\overline{ADB0}$, transmitter status on $\overline{ADB3}$,and ring indicator (CE) on $\overline{ADB4}$. The status gate is enabled by the AND-gated combination of STAT and the address comparator output.

Finally, the address gate places the device address, as determined by the address selector, on the A Data Bus ($\overline{ADB0-4}$). The address gate is enabled by a POLL command from the CPU if the receiver or transmitter are in the ready condition. Poll address bits are: receive/transmit selection on $\overline{ADB0}$, device address on $\overline{ADB1-4}$, and the error signals on $\overline{ADB5}$, $\overline{6}$, and $\overline{7}$.

Circuit Description. Refer to schematic diagram 96-451-01 in Section 8.

When terminal power is turned on, a POC at XD4-5 is inverted and NOR-gated by XC6-8 to trigger XD6, a monostable multivibrator. XD6 produces a positive and negative approximately 1 usec pulse (as determined by R1 and CA) at pins 5 and 12, respectively. The output at XD6-5 resets the receiver-transmitter (XG3) at pin 21 to clear all receiver-transmitter logic. That is, it resets the transmitter and receiver registers, resets the receiver holding register, FE, OE, PE and DRR, and sets TRO high.

The negative pulse at XD6-12 resets the outputs of the status flip-flops (XE5) to a low level. The reset states for the four flip-flops in XE5 are as follows:

1. Request-to-send (CA) flip-flop (Q_0) off; CA is thus low at XB6-6.
2. Receiver flip-flop (Q_1) off.
3. Transmitter flip-flop (Q_3) off.
4. Data terminal ready (CD) flip-flop (Q_4) off; CD is thus low at XB6-8.

Reset is also initiated by a read status command from the CPU. This event occurs if STAT (status) plus IC CLK are high at XC6-4, and MA1-4 at XC3-8, -9, -6, and -5 respectively, are low.

A set status command from the CPU can reset the interface card also. In this case, MA0, 6, and 7 are low and MA5 is high. STAT must also be high at XF5-4, and the address on MA1-4 must match the card address set by the strapping on XA2. When the addresses match, the address comparator (XD3-3, -4, -10, and -11) applies a high level to XE6-1. This event enables STAT to be gated to XF5-4. STAT, clocked with IC CLK (integrated circuit clock) at XE6-11, is applied to XF5-5. XF4-12 and -4 are, consequently, enabled during IC CLK to enter the command on MA0 and 5-7 into XB4, the command decoder. For a reset command, XE4 puts out a low level on pin 10 to XC6-11 to reset the card.

Three types of commands are used to transfer data between the CPU and the interface card. STAT, at XG4-9, turns the card and peripheral device on and off and transfers status information to the CPU. POLL, at XG6-4, interrogates the card to determine if it is ready to transfer data. IOD, at XF5-13 and -1, causes data to be transferred.

Receipt of a POLL at XG6-4 and -10 enables the two gates. If the receiver is not ready, XG5-5 is low to inhibit XG6 at pin 5, and XG5-6 is high. As a result, the POLL is gated to XG6-13 and -1. If the transmitter is not ready, XG5-3 is low to inhibit XG6 at pin 12, and XG5-2 is high. Thus, the POLL output at XG6-3 is transferred to the next card installed. XG6-6 and -11 are low when the card is not ready to transfer data. With these two low levels at XC5-4, and -5, XC5-6 is low to inhibit the $\overline{\text{ADB1}}$ through $\overline{\text{ADB4}}$ gates (XD2-11, -6, -3 and -8) and, consequently, the card address is not placed on the A Data Bus. That is, $\overline{\text{ADB1-4}}$ is high. The low level at XG6-11 is also inverted by XD4-12 to make $\overline{\text{ADB0}}$ high.

Assume the receiver is ready. In this case the DR output (pin 19) of XG3 is high to indicate that received data is available. This high level at XG5-8 causes CG5-5 to change state (go high) on the next IC CLK pulse (XE6-8). With XG5-8 high, gate XG6-6 is enabled and gate XG6-8 is inhibited by the low level at XG5-6. The latter prevents POLL propagation while the former applies a high level when POLL arrives, to XC5-10, XC5-5, and XF6-1.

The high level at XC5-10 is gated to pins 4, 2, and 12 of the error gates (XG1) to enable them. The address gates (XD2) are enabled at pins 12, 5, 2, and 10 by the high XC5-5 and 6. Thus, the card address (as determined by the strapping on XA2) is gated to $\overline{\text{ADB1-4}}$. (NOTE: SW1-4 are not installed in this terminal.) When XC5-5 is high, XG6-11 is low, since the transmitter flip-flop is low at XG5-3. The low level at XG6-11, inverted at XD4-12, makes $\overline{\text{ADB0}}$ high to indicate that the card is in the receive mode.

The high level at XF6-1 causes XF6-3 to go high on the next IC CLK pulse at XF6-12, enabling the XF5-3 gate. Without an IOD, the low level at XF5-3 inhibits the received data gates (XF1, XE2) at pins 2, 4, 12, and 10.

When the CPU sends an IOD, XF5-3 goes high to enable the received data gates and, consequently, the character in XG3 is placed on the A Data Bus. The high level at XF5-3 is also clocked with IC CLK, and the resulting low level at XF4-3 is applied to the DRR input (pin 18) of XG3 to reset its DR output to a low level. When DR goes low it deselects the card on the next IC CLK by resetting the XG5 and XF6 receiver ready flip-flops (XG5-5 and XF6-3 low). The change in state of XG5 and XF6 performs three functions: (1) it permits transfer of the next POLL to XG6-13 and -1; (2) it disables the received data gates; and (3) it causes XF5-3 to go low, XF4-3 to go high, and XC1-8 to go low to load the error latch (XG2). Note that a $\overline{\text{RCVR OFF}}$ signal (XE5-13 low) will also set XG5 and XF6 to the not ready state (XG5-6 high).

The other section of the XG5-XF6 logic controls transmitter loading. Operation is essentially the same as that described for the receiver control flip-flops. In this case, however, the transmitter ready state is defined by: (1) a signal from the transmitter indicating that the transmitter register is available for loading (THRE, pin 22, of XG3 is high); (2) the presence of a clear to send (CB) signal (XB5-10 high); (3) a high level at XE5-12 (transmitter on); and (4) the absence of $\overline{\text{BREAK}}$.

If CB and THRE are high at XC3-12 and -11, respectively, XG5-3 will set low (transmitter off). If either XE5-12 or $\overline{\text{BREAK}}$ is low at XF5-9 and -10 respectively, XG5-3 will be cleared, at pin 10, to a low level. If XE5-12 and $\overline{\text{BREAK}}$ are high, along with a low CB and THRL at XC3-10 and -11, XG5-3 is set high on the next IC CLK to enable the XG6-11 gate. The next POLL at XG6-13 produces a high level at XF6-8.

The high level at XF6-8 does three things. It (1) enables the address gates (XD2-12, -5, -2, -10) via the XC5-6 gate; (2) places a low level on $\overline{ADB0}$ via XD4-12, -13 and XG4-10, -11 to indicate transmit mode; and (3) causes XF6-5 to be set high on the next IC CLK, which enables the XF4-8 gate when IOD occurs.

The resulting low level at XF4-8 applied to the THRL input (pin 23) of XG3, loads the character on MA0-7 into the transmitter holding register. When XF4-8 subsequently makes the transition from low to high, it transfers the character to the transmitter register if the latter is not in the process of transmitting a character. If transmission is still in process, the transfer from the holding register is delayed until transmission has been completed.

The status signal reads the state of the interface card, sets the state of the receiver-transmitter, and sets output control signals.

When the CPU is ready for a read status transfer, it sends a STAT command to the interface card. STAT is sent only after the CPU is prepared to send the card address.

Four address bits on MA1-4 are applied to XD3-13, -8, -2 and -5, respectively. The card address, determined by the strapping on XA2, is applied to four exclusive NOR gates (XD3-12, -9, -1 and -6) that function as a comparator. If the address sent by the CPU matches the card address, the comparator puts out a high level to enable gate XE6 at pin 1. With XE6 enabled, the card can accept STAT at XE6-2.

STAT enables four of the status gates (XE1) at pins 10, 13, 2, and 5, and the fifth status gate (XG1) at pin 10. This places five status bits on the A Data Bus. Received line signal detector (CF) is gated to $\overline{ADB0}$ at XE1-8; $\overline{ADB1}$ and $\overline{2}$ are not used. The input on XE1-4, derived from CB (clear to send), THRE, and TRE, is gated to $\overline{ADB3}$ to report transmission status. THRE indicates if XG3 can be loaded, and TRE indicates if XG3 is transmitting a character. If XE1-4 is low, the transmitter is not available. Ring indicator (CE) is gated to $\overline{ADB0}$ at XG1-8.

STAT is also OR-gated through XC5-8, and the resulting high level at XC5-8 enables the three error gates (XG1-11, -3 and -6): PE (parity error), gated to $\overline{ADB5}$, indicates that the last character received by XG3 contained a parity error. FE (framing error) is gated to $\overline{ADB6}$ to indicate a missing stop bit in a received character. (This event will occur if there is noise on the line or a BREAK command is received.) OE (overrun error), gated to $\overline{ADB7}$, occurs when the CPU did not transfer a received character before a new character was received.

The output on XE6-3 (STAT AND-gated with the address comparator output) enables XF5 at pin 4. STAT is also clocked by IC CLK to produce a high output at XE6-11. This output is gated to XF5-6 to enable XF4 at pins 12 and 4. Thus, MA5 and 7 are gated to XE4-14 and -12, respectively. MA0 and MA6 are applied to pins 15 and 13, respectively, of XE4. XE4, the command decoder, decodes the states of MA0, 5, 6, and 7 to set the RS-232 interface status. The inputs and corresponding output states for XE4 are given in Table 4-10.

In summary, the RS-232 Interface Card responds to a POLL with its address, error status, and operating mode. The card responds to a read status command (STAT plus MA0 high or low and MA5-7 low) with error, transmitter availability, ring indicator, and received line signal detector status. For a set status command (STAT

Table 4-10. Input and output states of command decoder (XD2).

XE4 INPUT				XE4 OUTPUT		FUNCTION
D MA7	C MA6	B MA5	A MA0	Pin	State	
0	0	0	0		-	Used to read status without
0	0	0	1		-	altering condition of interface
0	0	1	0	10	8	Master reset
0	0	1	1	11	9	Trigger BREAK one-shot (XD6)
0	1	0	0		-	
0	1	0	1		-	Not used
0	1	1	0		-	
0	1	1	1		-	
1	0	0	0	3	2	Set data terminal ready flip-flop (XE5-10) to on
1	0	0	1	4	3	Set request to send flip-flop (XE5-15) to on
1	0	1	0	1	0	Set receiver flip-flop (XE5-13 to on
1	0	1	1	2	1	Set transmitter flip-flop (XE5-12) to on
1	1	0	0	7	6	Reset data terminal ready flip-flop to off
1	1	0	1	9	7	Reset request to send flip-flop to off
1	1	1	0	5	4	Reset receiver flip-flop to off
1	1	1	1	6	5	Reset transmitter flip-flop to off

plus a decoded command from XE4), the CPU sets the status of the card and external device. The status bits are defined in Table 4-11.

The remainder of the RS-232 card controls Baud Rate, data flow between the external device and interface card, parity and word length, and the number of stop bits to be transmitted.

The UA CLK circuit consists of two counter stages, XB3 and XB4. RS CLK (288 kHz) is divided in these counters to produce a UA CLK signal for XG3. UA CLK, at 16 times the shift rate, is applied to the RCC and TRC (pins 17 and 40) inputs of XG3.

Table 4-11. Status bits

STATUS BITS	
ADB0	Receive line signal detector (CF)
ADB1	Not used
ADB2	Not used
ADB3	Transmitter available if H; not available if L
ADB4	Ring indicator (CE)
ADB5	Parity error
ADB6	Framing error
ADB7	Overrun error
POLL Address Bits	
ADB0	H for receive mode; L for transmit mode
ADB1-4	Device address
ADB5	Parity error
ADB6	Framing error
ADB7	Overrun error

Any of five shift rates can be selected with the Baud Rate switch mounte on the rear panel of the terminal and connected to J20. This switch, through XA6, configures the preset states of XB3 and XB4 to supply the UA CLK rate needed for the selected baud rate. Table 4-12 gives the UA CLK configurations corresponding to the Baud Rate switch settings.

Table 4-12. UA CLK Configurations for various Baud Rates.

BAUD RATE	XB3 PRESET TO	XB4 PRESET TO	UA CLOCK (kHz)
110	÷15	÷11	1.745
300	÷15	÷ 4	4.8
1200	÷15	÷ 1	19.2
1800	÷10	÷ 1	28.8
2000	÷ 9	÷ 1	32.0

Data flow control between the modem and interface card is performed by the logic associated with: (1) received data (BB) at J21-15; (2) received line signal detector (CF) at J21-10; (3) transmitted data (BA) at J21-16; and (4) $\overline{\text{BREAK}}$ at XC1-4.

Received data (BB) on J21-15 is inverted by XB5-11. If CF (received line signal detector) is high at XB5-1, the data is applied to the RI input (pin 20) of XG3.

Data for transmission appears on the TRO output (pin 25) of XG3 and goes to XB6-13. This data is gated by XB6-11, the RS-232 driver, to J21-16 (BA) by $\overline{\text{BREAK}}$ at XB6-12. A "stop" state (high level from TRO) produces a "mark", or low level at the BA output. A "start" (low level from TRO) or a $\overline{\text{BREAK}}$ pulse from XD6-4 produces a "space", or high, level at BA.

$\overline{\text{BREAK}}$ is produced by XD6, a one-shot triggered by a status set command from the command decoder, XE4 (see Table 4-10). A $\overline{\text{BREAK}}$ pulse of about 200 ms (as determined by R6 and C15) produces a space on the BA line that is longer than the normal character time. The receiving end of the line interprets the space as an interrupt signal.

A parity switch, located on the rear panel of the terminal, and connected to XA6, selects parity and word length. (NOTE: Switches SW5-8 are not installed.)

With the parity switch in the off position, R5 and R4 are connected to +5 V dc. The resulting drop across R5 places a high level on pins 35 and 38 of XG3. The high level pin 35 inhibits the parity generation and verification circuits in XG3; the high level at pin 38 selects a character length of eight bits.

Setting the parity switch in the odd parity position (the position shown on the schematic) disconnects R5 and R4 from +5 V dc. As a result, pin 35 is low to enable the parity circuits in XG3. The low level at pin 38 selects a character length (excluding parity) of seven bits. Pin 39 of XG3 is also low since R3 is not connected to +5 V dc. A low level at pin 39 selects odd parity.

With the parity switch in the even parity position, R3 and R4 are connected to +5 V dc, which drives pin 39 of XG3 high to select even parity. The levels at pins 35 and 38 do not change from the odd parity levels.

4.4.13 Terminator Card

The terminator card provides resistive pull-ups and terminations for the data bus and control lines in the terminal. A strapping block is also included to program restart commands.

Block Diagram Analysis. As indicated by the block diagram in Figure 4-23, all data bus, control, clock, and restart lines are terminated to prevent signal deterioration. The location selector, a strapping block, provides for grounding one or more of the restart lines to specify restart commands. A restart command specifies the program memory location at which the program starts after an interrupt.

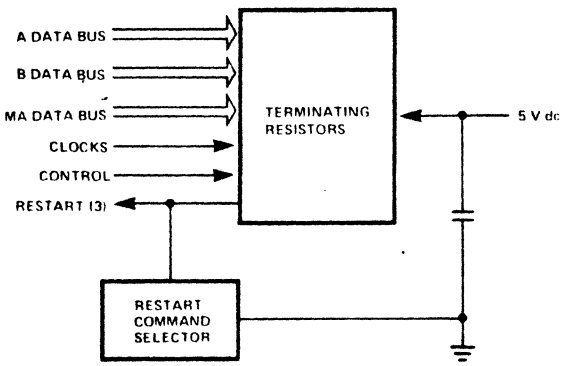


Figure 4-23. Terminator card block diagram.

Circuit Description. Refer to schematic diagram 96-394-01 in Section 8.

X1 through X5 are resistance networks that provide resistance pull-ups and terminations for the data bus and control lines driven with open-collector drivers.

The program restart address is determined by the E1 through E6 jumper arrangement. With no jumpers in place (standard configuration), the program starts at address 0_8 after an interrupt, and 10_8 after a POC (power on clear).

In the case of a POC, circuitry on the processor card (see Section 4.4.4) holds $\overline{\text{RSTO}}$ high. Thus, one of only four POC restart addresses can be specified. One of eight addresses, however, can be specified for other types of interrupts.

Table 4-13 shows restart addresses provided by various E1-E6 jumper connections.

Table 4-13. Program restart addresses provided by E1-E6 jumper options.

JUMPERS IN	RESTART ADDRESS AFTER	
	AN INTERRUPT	A POC
None (standard)	0_8	10_8
E1 to E2	10_8	10_8
E3 to E4	20_8	30_8
E1 to E2 and E3 to E4	30_8	30_8
E5 to E6	40_8	50_8
E1 to E2 and E5 to E6	50_8	50_8
E3 to E4 and E5 to E6	60_8	70_8
E1 to E2, E3 to E4, and E5 to E6	70_8	70_8

This section is not applicable to the 8025G CRT terminal.

6.1 PREVENTIVE MAINTENANCE

Preventive maintenance of the 8025 CRT Terminal is based on routine performance of the steps in paragraphs 6.1.3 and 6.1.4. Sight, smell, hearing, and touch are used, rather than test measurements.

Follow the steps every time the terminal is serviced, regardless of the reason. However, do not make internal inspections unless the cabinet is removed for another purpose.

6.1.1 Objective

Preventive maintenance helps to minimize terminal down time caused by malfunctions. It can find and correct abnormal conditions before they develop into failures.

6.1.2 Required Equipment and Materials

The following equipment and materials are used in preventive maintenance:

- Triplett 310 Multimeter or equivalent
- Clean, soft cloth
- Glass cleaner (nonabrasive)
- Contact cleaner (e.g., "No Noise" Contact Restorer)
- Anti-corona lacquer or dope
- Hand tools

6.1.3 General Procedure

Whenever the terminal is serviced, be sure to check its physical condition:

- Visually inspect the terminal, inside and out, for dust, dirt, etc.

  NOTE: Check inside the terminal only if the cabinet must be removed for servicing.

- Look for poorly seated printed-circuit cards and connectors, signs of overheating, damaged connectors and cables, or other faults.

  CAUTION: MOS ELEMENTS USED ON CIRCUIT CARDS ARE EASILY DAMAGED BY STATIC DISCHARGE. ALWAYS HANDLE CARDS SO THAT NO DISCHARGE FLOWS THROUGH THE CARD. BEFORE TOUCHING A CARD, PLACE ONE HAND ON THE TERMINAL CHASSIS. KEEPING THAT HAND ON THE CHASSIS, USE YOUR OTHER HAND FOR THE CARD.

- Check to make sure that both the fans are working. Listen also for unusual click and beep sounds, high voltage arcing, etc.
- Be alert to abnormal odors such as charring and ozone.
- Make any corrections needed.
- Check all keyboard keys and controls for correct terminal response (refer to Section 3).
- Keep a log of inspections, faults, and repairs for each terminal. You will find it a valuable aid to proper maintenance.

6.1.4 Specific Procedures

Before starting these maintenance procedures, correct any irregular conditions; then proceed as follows:

WARNING: DANGEROUSLY HIGH VOLTAGE IS EXPOSED IN THE CRT AREA WHEN THE TERMINAL IS OPERATED WITH THE TOP SECTION OF THE CABINET REMOVED.

WARNING: BEFORE WORKING IN OR NEAR THE POWER SUPPLY AREA, DISCHARGE ALL FILTER CAPACITORS.

Rear Panel. Verify that the fuse holders are tight and all connectors are secure and undamaged.

Keyboard. 1) Check keys for loose caps and switches, sluggish movement, intermittent operation, and double-stroke action (two characters produced per stroke) 2) Inspect the keyboard area for foreign material if service required cabinet removal.

Cooling Fan. 1) See whether the cooling vents are blocked with paper, lint, etc. 2) Listen for normal fan operation (speed, bearings, etc.) 3) Check fan blades for accumulated dirt and grease if cabinet removal is required.

Regulated Output Voltages. Measure +5 V dc regulated output on the Regulator Card (see paragraph 7.2 in Section 7). Also measure +55 V dc regulated output on the Monitor Deflection Board (see paragraph 7.4.2 in Section 7). If they are out of specification, check that the line voltage is 117 V ac $\pm$ 10%. Adjust the +5 V dc and +55 V dc outputs, as required, if the line voltage is correct.

Card Cage. If cabinet removal is required, 1) visually inspect the card cage area. 2) See whether all cards and flat-line connectors are properly seated.

NOTE: DO NOT remove any circuit card unless removal is required by other maintenance requirements.

CAUTION: MOS ELEMENTS USED ON CIRCUIT CARDS ARE EASILY DAMAGED BY STATIC DISCHARGE. ALWAYS HANDLE CARDS SO THAT NO DISCHARGE FLOWS THROUGH THE CARD.

BEFORE TOUCHING A CARD, PLACE ONE HAND ON THE TERMINAL CHASSIS. KEEPING THAT HAND ON THE CHASSIS, USE YOUR OTHER HAND FOR THE CARD.

If a card must be removed, check the gold-plated edge contacts for tarnish. Clean with a soft cloth and some contact cleaner. NEVER CLEAN WITH AN ABRASIVE.

Check the mating connector on the mother board for distorted contacts, especially if the card does not seat smoothly and fully. DO NOT attempt to clean the contacts except with a spray contact cleaner.

8025 CRT Display. If cabinet removal is required, make certain that the circuit card edge connector and the CRT connectors are properly seated. Check for corona discharge (high voltage arcing). If present, remove dust from all high voltage leads and apply anti-corona lacquer/dope.

Confirm that all display parameters (e.g., centering, linearity, and width) are set for a normal presentation. (See Figure 7-3 in Section 7.) Make the required adjustments for normal presentation (refer to paragraph 7.4 in Section 7).

Clean the CRT face with a nonabrasive glass cleaner.

6.2 FIELD MAINTENANCE

This paragraph tells how to isolate malfunctions in the 8025 CRT Terminal to field-replaceable parts. Included are a troubleshooting procedure and a guide. Information also includes removal and replacement procedures normally used in field maintenance.

6.2.1 Objective

Field maintenance is intended to make the terminal operational in the least time, with minimum equipment. This objective is best met by isolating the problem to one of the recommended field replaceable parts and installing an operational part. Field replaceable parts are listed in paragraph 6.2.4.

6.2.2 Required Equipment

The following equipment is used in field maintenance.

- Triplett 310 Multimeter or equivalent
- One set of circuit cards (see paragraph 6.2.4)

- Hand tools
- Clean, soft cloth
- Glass cleaner (nonabrasive)
- Contact cleaner (e.g., "No Noise" Contact Restorer)
- Anti-corona lacquer or dope
- Integrated-circuit puller
- Keyboard key removal tool

6.2.3 Rules of Good Maintenance

Observing the following general rules of good maintenance will help minimize down time, reduce chances of personal injury, and prolong terminal life.

CAUTION: DANGEROUSLY HIGH VOLTAGE IS EXPOSED IN THE CRT AREA WHEN THE TERMINAL IS OPERATED WITH THE TOP SECTION OF THE CABINET REMOVED. TAKE ADEQUATE PRECAUTIONS.

- Do not remove or replace fuses when the power cord is connected.
- FIND THE CAUSE OF A BLOWN FUSE BEFORE REPLACING IT.
- DO NOT REMOVE OR REPLACE CIRCUIT CARDS WHEN TERMINAL POWER IS ON.
- MOS elements are used in the terminal. They are easily damaged by discharges of static electricity. Never handle circuit cards unnecessarily. Correct handling procedures are outlined in paragraph 6.2.5.
- Keep the terminal clean, inside and out.
- Perform routine maintenance procedures (refer to paragraph 6.1) every time the terminal is serviced.
- Use the advice in this manual to locate and repair malfunctions.

6.2.4 Field Troubleshooting Procedure

We recommend that field maintenance should not go beyond isolating a malfunction to a field-replaceable part. We also recommend that you restrict field replacements to these parts. Field replaceable parts are as follows (refer to Section 9 for part numbers):

- Regulator Card*
- Cursor Control Card*
- Video Control Card*
- Refresh Buffer Card*
- Timing Control Card*
- Refresh Memory Card*
- Refresh Control Card*
- Processor Card*
- ROM (Program Memory) Card*
- RS-232 Interface Card*
- Terminator Card*
- Monitor Deflection Board
- Keyboard Assembly
- Keyboard Encoder
- Key switches and caps
- Fuses
- LEDs

* One operable set of these cards is recommended for field maintenance.

Visual Inspection. Visually inspect the terminal for loose or broken connections, damaged printed circuit cards, scorched wires or components, etc. Visible troubles usually have an obvious remedy. Set the Baud Rate switch at the correct position before you begin troubleshooting.

Isolating Malfunctions. When troubleshooting, consider all complaints and symptoms together, rather than individually. Also be aware of possible temperature effects when isolating an intermittent problem.

Table 6-1 will help you to isolate malfunctions. It lists the components in which malfunctions are most likely to produce the indicated symptom. Note that symptoms can result from faults in more than one section or card in the terminal.

In such cases, you can often narrow a problem down to one or two possibilities by thoroughly analyzing the symptom.

For example, assume there is no beep response. Table 6-1 indicates that the Cursor Control, Refresh Buffer, Keyboard or Speaker could be at fault. Your aim should be to eliminate as many choices as possible by determining which cards are probably not at fault. Here is a typical elimination procedure:

1. Two audio indicators--beep and click--are used in the terminal. Is the click response operating?

2. (Assume click is operative) The "Click response inoperative" entry in Table 6-1 potentially eliminates the Timing Control, Refresh Memory, and Processor Cards and brackets the problem to the Cursor Control and Refresh Buffer cards. (Note that the Refresh Buffer is not related to the click response.)

3. Before replacing either the Cursor Control or Refresh Buffer, however, determine the probable operating status of the other three cards. Review the Theory of Operation and schematics in this manual to establish which signals on the three cards are directly or indirectly related to both the click and the beep circuits. Such a review will reveal that both audio indicators are related in some manner to $\overline{I/O}$, $\overline{WAIT}$ and MA8-13.

4. In the absence of other symptoms that might relate to $\overline{I/O}$, $\overline{WAIT}$, and MA8-13 (e.g., input/output problems), Step 3 established a high probability that the Timing Control, Refresh Memory, and Processor Cards are not at fault.

5. The choice is now narrowed to two: Cursor Control and Refresh Buffer. Since the Refresh Buffer is the easier card to replace (no interconnect cable to disconnect), it is the logical first choice for replacement.

If you need to take fault isolation beyond a field replaceable part, bench maintenance is recommended (see paragraph 6.3).

Table 6-1. Symptoms vs. probable malfunctions in 8025 Terminal

SYMPTOM	MALFUNCTION PROBABLY IN																								
	Cursor Control	Video Control	Refresh Buffer	Timing Control	Refresh Memory	Refresh Control	Processor	ROM (Program)	RS-232 (Modem)	Keyboard	Key Switch	Encoder	Speaker	CRT Display	Power Supply	5 V Regulator	12 V Regulator	Fuse	ON/OFF Switch	Terminator	Cursor Cable	Video Cable	Modem Cable	RS-232 (Aux. Sto.)	RS-232 (Printer)
A U D I B L E S Y M P T O M S																									
Beep response inoperative	X		X							X			X												
Continuous beep	X		X							X															
Beep response, all keys	X		X					X		X		X													
Beep and click responses inoperative	X												X												
Click response inoperative	X						X			X		X	X												
Continuous click after terminal power is applied*											X														
Rapid click response	X									X															
Varying click/repeat rate	X											X													
Continuous click with character repeat after terminal power is applied											X														
Cooling fans inaudible															X										

* To locate bad key switch, individually depress each key for more than one-half second. Bad key will be inactive after this period.

Table 6-1 (continued)

SYMPTOM	MALFUNCTION PROBABLY IN																								
	Cursor Control	Video Control	Refresh Buffer	Timing Control	Refresh Memory	Refresh Control	Processor	ROM (Program)	RS-232 (Modem)	Keyboard	Key Switch	Encoder	Speaker	CRT Display	Power Supply	5 V Regulator	12 V Regulator	Fuse	ON/OFF Switch	Terminator	Cursor Cable	Video Cable	Modem Cable	RS-232 (Aux. Sto.)	RS-232 (Printer)
C U R S O R S Y M P T O M S																									
No cursor, characters displayed	X		X	X	X																				
No block cursor in protect mode		X	X																						
Non-blinking cursor	X	X		X																					
Cursor at home; no keyboard response	X																X				X				
Cursor/displayed character out of sync	X		X		X																				
Cursor movement abnormally limited	X		X			X		X																	
Cursor moves down two or more lines when CR key is struck										X	X														
C H A R A C T E R S Y M P T O M S																									
Constant character jitter		X	X	X	X																				
Character jitter, every key stroke		X				X								X											
Character flicker		X	X																						
Deformed character(s)		X												X											

Table 6-1 (continued)

SYMPTOM	MALFUNCTION PROBABLY IN																								
	Cursor Control	Video Control	Refresh Buffer	Timing Control	Refresh Memory	Refresh Control	Processor	ROM (Program)	RS-232 (Modem)	Keyboard	Key Switch	Encoder	Speaker	CRT Display	Power Supply	5 V Regulator	12 V Regulator	Fuse	ON/OFF Switch	Terminator	Cursor Cable	Video Cable	Modem Cable	RS-232 (Aux. Sto.)	RS-232 (Printer)
C H A R A C T E R S Y M P T O M S (continued)																									
No upper or lower case characters		X	X			X																			
Missing character set		X																							
Displayed character alternates between correct and incorrect character			X		X																				
Character is displayed simultaneously on two or more lines	X					X																			
Display filled with one character					X				X															X	X
O T H E R D I S P L A Y S Y M P T O M S																									
No raster		X		X										X	X	X						X			
Intermittent raster		X		X										X	X	X						X			
Raster flicker		X		X										X	X	X						X			
Raster wiggle/drift				X										X	X										
Small raster/blooming/dim/video loss of sync														X	X										
Radical blooming	Open Brightness Control																								
Lightning-like flashes on display screen				X										X											

Table 6-1 (continued)

SYMPTOM	MALFUNCTION PROBABLY IN																								
	Cursor Control	Video Control	Refresh Buffer	Timing Control	Refresh Memory	Refresh Control	Processor	ROM (Program)	RS-232 (Modem)	Keyboard	Key Switch	Encoder	Speaker	CRT Display	Power Supply	5 V Regulator	12 V Regulator	Fuse	ON/OFF Switch	Terminator	Cursor Cable	Video Cable	Modem Cable	RS-232 (Aux. Sto.)	RS-232 (Printer)
OTHER DISPLAY SYMPTOMS (continued)																									
Blank display; raster present	X	X	X	X	X		X										X			X					
Brightness control ineffective	Defective Brightness Control																								
Garbled data display		X	X	X				X																	
Repetitive garbled data displayed					X			X																	
Only one line (usually short) displayed			X		X															X				
All field modification functions inoperative		X								X															
Blink functions inoperative				X																					
Field modification functions occur without command		X	X																						
Display pages flip once or repeatedly						X																			
KEYBOARD SYMPTOMS																									
No keyboard response			X	X	X		X	X		X		X					X			X					
Incorrect keyboard response					X	X	X	X		X		X								X					
Keyboard locked out				X	X		X	X	X	X														X	X

Table 6-1 (continued)

SYMPTOM	MALFUNCTION PROBABLY IN																								
	Cursor Control	Video Control	Refresh Buffer	Timing Control	Refresh Memory	Refresh Control	Processor	ROM (Program)	RS-232 (Modem)	Keyboard	Key Switch	Encoder	Speaker	CRT Display	Power Supply	5 V Regulator	12 V Regulator	Fuse	ON/OFF Switch	Terminator	Cursor Cable	Video Cable	Modem Cable	RS-232 (Aux. Sto.)	RS-232 (Printer)
K E Y B O A R D S Y M P T O M S (continued)																									
Keyboard mode (case/control) incorrect		X								X											X				
Repeat function inoperative	X									X		X									X				
Single key inoperative											X														
Multiple character display per stroke	X										X														
Multiple character display, all or group of keys												X													
Two different characters displayed per stroke										X															
Wrong character consistently displayed per stroke					X							X													
C L E A R F U N C T I O N S Y M P T O M S																									
Incomplete clear			X		X			X																	
Power on clear (POC) function inoperative		X		X			X	X																	
Display filled with one character after terminal clears					X				X															X	X

Table 6-1 (continued)

SYMPTOM	MALFUNCTION PROBABLY IN																								
	Cursor Control	Video Control	Refresh Buffer	Timing Control	Refresh Memory	Refresh Control	Processor	ROM (Program)	RS-232 (Modem)	Keyboard	Key Switch	Encoder	Speaker	CRT Display	Power Supply	5 V Regulator	12 V Regulator	Fuse	ON/OFF Switch	Terminator	Cursor Cable	Video Cable	Modem Cable	RS-232 (Aux. Sto.)	RS-232 (Printer)
C O M M U N I C A T I O N S S Y M P T O M S																									
Transmits garbled data									X														X	X	X
Receives garbled data									X														X	X	X
Receives garbled data when terminal should not be receiving									X															X	X
No I/O with communications system				X					X														X	X	X
M I S C E L L A N E O U S S Y M T O M S																									
Intermittent, correct operation															X	X									
Intermittent, incorrect operation	X	X	X	X	X	X	X	X	X	X		X			X	X								X	X
Intermittent communications				X					X						X		X						X	X	X
Smoke/arcing/burning odor														X	X										
Cannot turn terminal on															X			X	X						
Cannot turn terminal off																			X						
Terminal locked up							X	X	X															X	X
No I/O function				X					X														X	X	X
Escape functions inoperative	X	X		X																					

Table 6-1 (continued)

SYMPTOM	MALFUNCTION PROBABLY IN																								
	Cursor Control	Video Control	Refresh Buffer	Timing Control	Refresh Memory	Refresh Control	Processor	ROM (Program)	RS-232 (Modem)	Keyboard	Key Switch	Encoder	Speaker	CRT Display	Power Supply	5 V Regulator	12 V Regulator	Fuse	ON/Off Switch	Terminator	Cursor Cable	Video Cable	Modem Cable	RS-232 (Aux. Sto.)	RS-232 (Printer)
M I S C E L L A N E O U S S Y M P T O M S (continued)																									
Escape functions operate incorrectly	X	X	X	X																					
Program malfunction							X	X																	
No composite video at video jack (J15)		X																							
Terminal inoperative; raster present							X	X							X		X								

6.2.5 Removal and Replacement Procedures

Cabinet Removal and Replacement. To take the top section of the cabinet off, remove the five screws (three on the front, two on the back) shown in Figure 6-1 and 6-2. Lift the cabinet straight up.

To replace the top section of the cabinet, lower it straight down over the internal assembly. Replace the five screws shown in Figure 6-1 and 6-2.

Circuit Card Removal and Replacement. The 8025 CRT Terminal contains removable circuit cards housed in a card cage with a capacity of 18 cards. The card slots are numbered REG, 1, 2, 3, 4, 5, 6, 7, 8, 9-------9, from left to right. Each card is equipped with an ejector tab to help removal. The tabs are marked with the slot location. The card cage, with no cards installed, is shown in Figure 6-3.

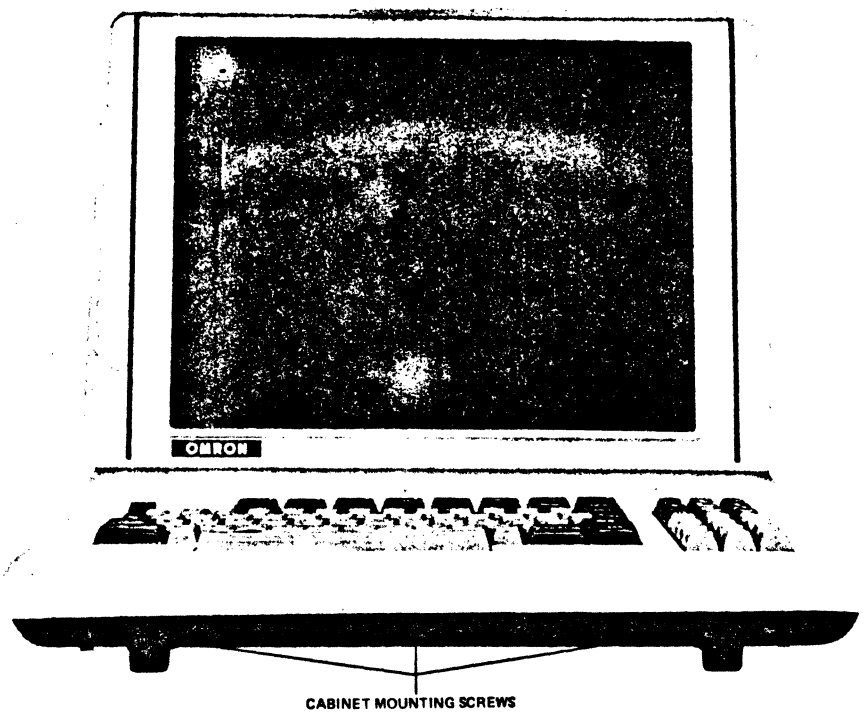


Figure 6-1. Cabinet mounting screws (front).

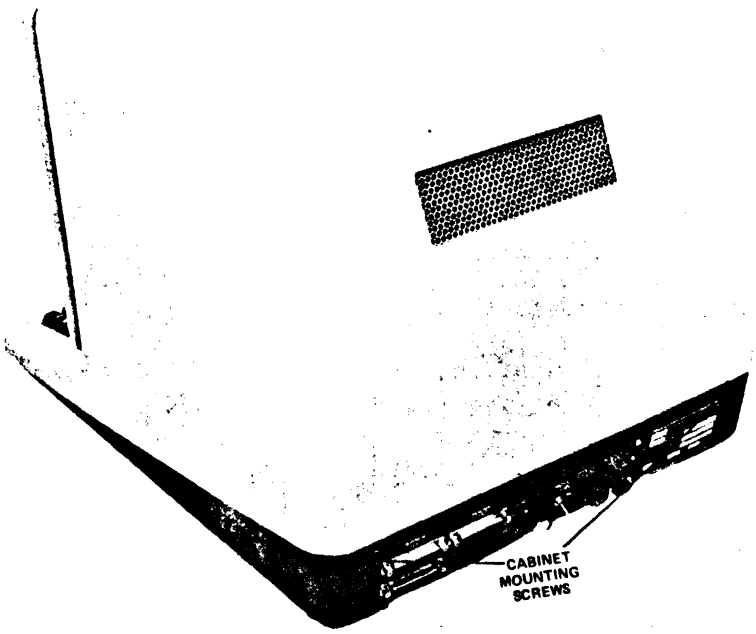


Figure 6-2. Cabinet mounting screws (rear).

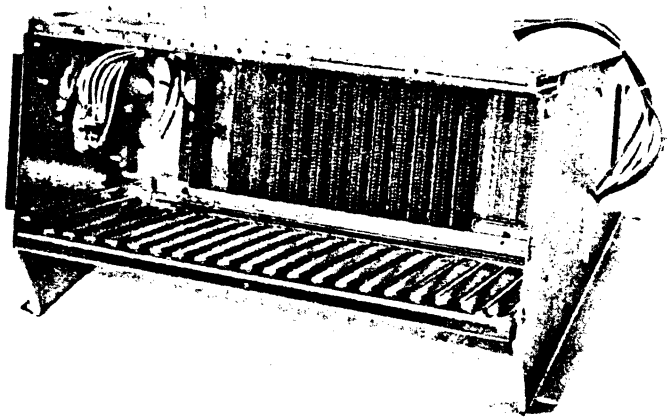


Figure 6-3. Card cage.

CAUTION #1: NEVER REMOVE OR REPLACE A CIRCUIT CARD WHEN THE TERMINAL IS TURNED ON.

CAUTION #2: MOS ELEMENTS ARE EASILY DAMAGED BY STATIC DISCHARGE. ALWAYS HANDLE CARDS SO THAT NO DISCHARGE FLOWS THROUGH THE CARD.

BEFORE TOUCHING A CARD, PLACE ONE HAND ON THE SURFACE CONTACTING THE CARD. USE THE OTHER HAND FOR THE CARD.

NOTE: To unplug ribbon cables, use only an IC puller, or use a small screwdriver to lever the plug out from both ends. NEVER PULL ON THE CABLE OR THE LID OF THE PLUG.

When picking up a card, first place one hand against the surface on which the card rests. Then pick the card up with your other hand.

To put a card down, first place the hand not holding the card against the surface on which you want to place the card. This precaution discharges body static, so that you can safely lay the card down.

To remove a card from the card cage, proceed as follows:

1. Place one hand on the CRT face and the mounting band or the terminal chassis.
2. Grasp the pull tab on the card with the other hand.
3. Pull the card partially out of the slot.
4. Disconnect the card connector(s).

5. After the card is completely clear of the terminal, remove your other hand from the equipment.

To replace a card in the card cage, proceed as follows:

1. Hold the card in one hand.

2. Place your other hand on the CRT face and the mounting band or the terminal chassis.

3. Insert the card partially into the correct slot.

4. Plug in the connector(s).

5. Push the card in until it is properly seated.

NOTE: The DIP plug is numbered on the lid. Make sure it is oriented the same way as the socket into which it is being inserted.

6. After the card is seated and the connector(s) plugged in, remove the hand holding the CRT face or the terminal chassis.

Keyboard Removal and Replacement. Removal of the keyboard from the terminal is done this way:

1. Remove the top section of the cabinet as described earlier.

2. From underneath, remove the four keyboard mounting screws shown in Figure 6-4.

NOTE: Do not remove the angle brackets attached to the keyboard.

3. Undo the cable clamps.

4. Remove the two connectors on the left-hand side of the machine and unplug the ribbon cable from the Refresh Buffer Card in slot #3.

5. Lift the keyboard straight up.

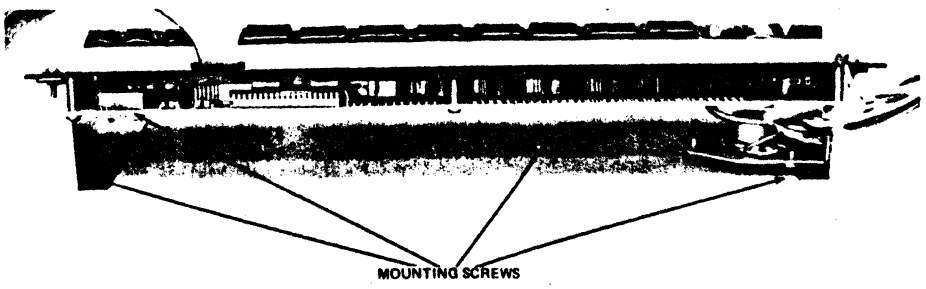


Figure 6-4. Keyboard mounting screw locations.

To replace the keyboard, proceed as follows:

1. Place the keyboard in position and plug in the connectors.
2. Replace the four keyboard-mounting screws shown in Figure 6-3. Drive the screws only far enough to hold the keyboard loosely in place.
3. Lower the top section of the cabinet into place and align the keyboard within the opening in the cabinet.
4. Carefully remove the top section of the cabinet so that you do not move the keyboard.
5. Tighten the four keyboard-mounting screws, again taking care not to move the keyboard.
6. Replace the top section of the cabinet as described earlier.

Key Cap/Switch Removal and Replacement. To remove a key switch, proceed as follows:

1. Remove the key cap by pulling straight up with a key cap removal tool.
2. Remove the keyboard as described earlier.
3. Locate the two leads of the defective switch on the back of the circuit card.
4. Unsolder both switch leads, sucking all solder from the mounting holes.
5. Lift the switch straight up, if possible.
6. If the lead solder connection is too strong, try wiggling each of the leads with needle-nose pliers to break the connection. Then lift the switch straight up.
7. If the switch still is not free after Step 6, reheat each lead alternately while wiggling the switch until it is free.

Replace a key switch as follows:

1. Clear excess solder from the mounting holes in the circuit board.
2. Insert new switch leads to the appropriate depth and solder them into place.

NOTE: Switch leads are mechanically configured to prevent incorrect installation.

3. Replace the keyboard as described earlier.

4. Push the key cap down onto the key switch.

Keyboard Encoder Removal and Replacement. The keyboard encoder (an integrated circuit) is located on the keyboard printed circuit card (see Figure 6-3). It is installed in an integrated circuit socket. The caution concerning static discharg given for circuit cards applies to removing or replacing the encoder.

Fuse Removal and Replacement. The terminal is protected by two fuses housed on the back panel, a 3/4 amp (F201) and a 2 amp (F202). To remove them, disconnect the power cord, turn the post cap counterclockwise, and pull straight out. Remove the old fuse from the cap. To install a fuse, insert it in the post cap, push it into the post, and turn it clockwise to lock it in place.

Monitor Deflection Board Removal and Replacement. The Monitor Deflection Board is located above the neck of the CRT. To remove the board, disconnect E101 through E104 and P102 through P112, excluding P109, (see Figure 6-5). Then remove four screws indicated in Figure 6-5 and lift the board off the chassis.

To install the board, position it on the chassis to align the mounting holes. Replace the four mounting screws and reconnect all interconnects. Refer to the terminal wiring diagram in Section 8 if in doubt about correct interconnection.

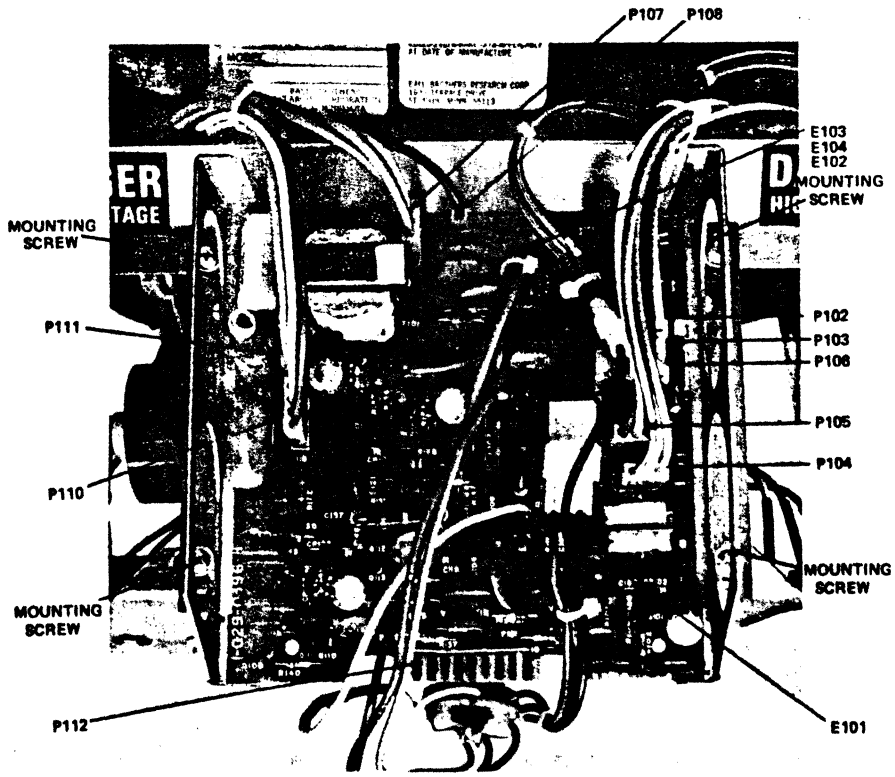


Figure 6-5. Monitor Deflection Board interconnections and mounting screws.

6.3 BENCH MAINTENANCE

This paragraph tells how to isolate malfunctions in the 8025 CRT Terminal to component level. Included are general and specific troubleshooting procedures. Information also includes removal and replacement procedures normally used in bench maintenance.

NOTE: Only qualified electronics technicians should perform bench maintenance of the terminal.

6.3.1 Objective

Bench maintenance is intended to make the terminal operational by correcting malfunctions that cannot be fixed in the field with the procedures in Paragraph 6.2 This objective is best met by isolating the problem to a component on a circuit card or assembly and replacing it with a good component. A secondary objective is safety. Thus, CRT removal and replacement are recommended bench service procedures.

6.3.2 Required Equipment and Materials

NOTE: Equivalent substitutes may be used.

- Oscilloscope, Tektronix 465
- Multimeter, Triplett 310
- Digital voltmeter, Fluke 8000A
- Logic probe, Hewlett-Packard 10525T
- EIA interface monitor, International Data Model 60
- Extender cards, 2 ea., OMRON 99-381-01
- "Dip Clip", Pomona Electronics 3916
- Illuminated magnifier
- Handtools
- Miniature soldering iron, controlled heat, 47 watts maximum
- Solder removal kit, "Wickit"
- Industrial alcohol
- 8025 CRT Terminal service manual

6.3.3 Rules of Good Maintenance

Observing the following general rules of good maintenance will help minimize down time, prolong terminal life, and reduce the chances of personal injury.

- Use procedures, aids, and technical information in this manual to locate and repair malfunctions
- Check the "obvious" (e.g., disconnected power cord) before investigating more difficult-to-locate causes of malfunction.
- When a trial-and-error replacement approach must be used, start with the easiest-to-verify alternative.
- Do not remove or replace fuses with power cord connected.
- Do not remove or replace circuit cards when terminal power is on.
- Consider temperature possibilities when investigating an intermittent problem.
- Transistor failure is often caused by failure of another component. Investigate this possibility before replacing a transistor.
- Keep terminal clean, inside and out.
- Solder quickly and use heat shunts to prevent heat damage.
- Avoid excessive card extraction and insertion.

6.3.4 Replaceable Parts

Replaceable parts are listed in Section 9.

NOTE: Use OMRON or OMRON-approved parts only. The use of other parts can void the manufacturer's warranty.

6.3.5 Workmanship

Bench maintenance recommendations and procedures presume high workmanship standards. Any damage caused by the use of improper tools, carelessness, mistreatment, or substandard workmanship voids the manufacturer's warranty, as will using component leads for studs and making unauthorized modifications.

6.3.6 General Troubleshooting Procedure

A general procedure for locating a faulty component follows:

1. Evaluate all complaints and symptoms together, rather than individually.

2. Determine the section, or sections, in the terminal that are operating incorrectly. The terminal contains the following sections:

- Cursor Control Card (Slot 1)
- Video Control Card (Slot 2)
- Refresh Buffer Card (Slot 3)
- Timing Control Card (Slot 4)
- Refresh Memory Card (Slot 5)
- Refresh Control Card (Slot 6)
- Processor Card (Slot 7)
- Program Memory Card (Slot 8)
- RS232 Interface Card Modem (Slot 9)
- RS232 Interface Card, Storage (Slot 10)
- RS232 Interface Card, Printer (Slot 11)
- Terminator Card (Slot 12)
- Regulator Card (Slot REG)
- LED Assembly
- Keyboard Assembly
- Power Supply Assembly
- CRT Monitor Assembly

Such determinations can usually be made by visual inspection, observing the display, and listening to the sounds of the terminal. Also use Table 6-1 to assist you in isolating a faulty section.

3. Determine the defective circuit or subsection of the faulty section. (NOTE: all sections in the terminal can be broken down into subsections and circuits. Refer to block diagrams in Section 4.) Visually inspect the section and check operating events, voltages, logic levels, waveforms, and resistances. Look for discrepancies between measurements and the data supplied in this section and Sections 4 and 8. Troubleshooting procedures for each section in the terminal are detailed later in Paragraph 6.3.7.

4. After narrowing the problem down to a circuit or subsection, determine the defective component or components. The defect can be found through visual inspection; measurement of voltage, logic level, and resistance; waveform analysis; or replacement of the suspected component or components. Also, many of the section troubleshooting procedures detailed later in Paragraph 6.3.7 relate malfunctions to possible component failures.

Visual Inspection. Visually inspect the terminal and suspect sections before starting a dynamic procedure to isolate a problem. Look for loose or broken connections, damaged cards or components, and so forth. Examine printed circuit boards under an illuminated magnifier and check for imperfections, excessive heating, cracked conductive paths, solder bridges, broken leads, and other abnormal conditions. Visible troubles usually have an obvious remedy.

Dynamic Testing. Procedures for isolating problems to the component level in each section of the terminal are given in Paragraph 6.3.7. In many cases, malfunctions are related to possible component failure. These procedures should always be used with the information supplied in Sections 4 and 8. If the problem still exists after you exhaust the applicable procedure, contact OMRON Field Service for assistance.

6.3.7 Specific Troubleshooting Procedures

Most circuit cards and subassemblies in the 8025 CRT Terminal are repairable on a component level. Such maintenance, however, is recommended only for "emergency" repairs. OMRON does not consider this type of service to be equal to maintenance performed in its own service facility.

OMRON service includes complete automatic diagnostic testing that cannot easily be duplicated in the field. Repairs are made with preconditioned components, and the workmanship is subject to stringent quality control monitoring. Also, repaired cards and subassemblies are environmentally seasoned and undergo full system testing.

CAUTION 1: WHEN HIGH CURRENT DRAIN IS INDICATED (BLOWN FUSE, CIRCUIT BOARD DISCOLORATION, HEAT DAMAGED HARNESS WIRES, BURNT OR DISCOLORED COMPONENTS, UNUSUAL ODORS, OR A DRASTIC DROP IN POWER SUPPLY VOLTAGE), DO NOT TROUBLESHOOT WITH THE POWER ON. FIND AND CORRECT THE CAUSE BEFORE DYNAMIC TESTING.

CAUTION 2: BEFORE INSERTING A CARD IN THE CARD CAGE, CHECK FOR ZERO (0) OHMS BETWEEN PINS 79 and 80 OF EDGE CONNECTOR, ZERO (0) OHMS BETWEEN PINS 1 AND 2, AND 50 OHMS (LOWEST METER RANGE) BETWEEN PINS 1 AND 80. TO AVOID DAMAGING OTHER CARDS IN THE TERMINAL, DO NOT INSERT ANY CARD NOT MEETING THESE REQUIREMENTS.

NOTE 1: Waveforms supplied in this paragraph are consecutively numbered. These numbers appear on the waveform photos and in the photo captions. Correspondingly numbered call outs on the applicable schematic indicate where the waveform can be observed. Waveforms are referenced to chassis ground.

NOTE 2: Should the insertion of any circuit card lock out the keyboard, return the card to OMRON for repair.

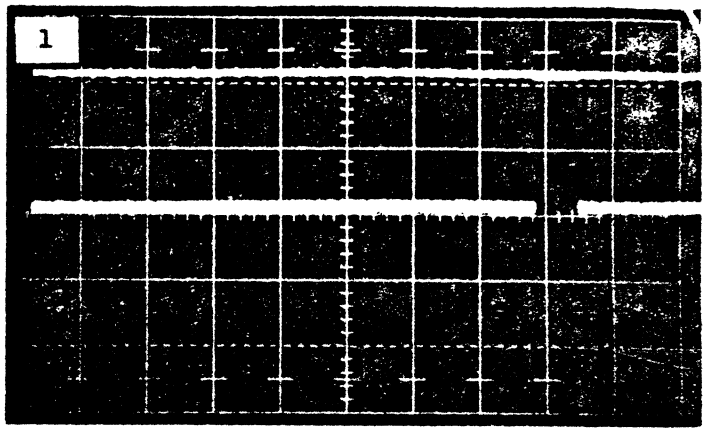
Video Control Card. Plug the card onto the extender card and insert in the terminal. Connect the ribbon connector. Check for the following signals in the order given.

WAVEFORM 1: BLANK

Oscilloscope Settings:
Vertical, 2 V/cm
Horizontal, 2 msec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XE6-6, Timing Control Card, Refresh Buffer Card

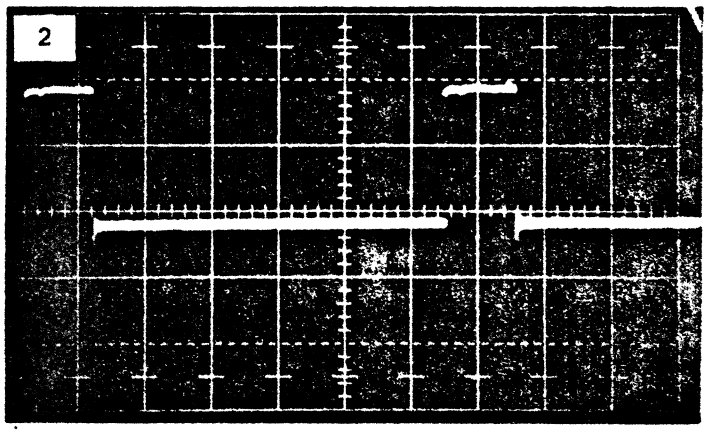


WAVEFORM 2: BLANK

Oscilloscope Settings:
Vertical, 2 V/cm
Horizontal, 10 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK;

XE6-6, Timing Control Card, Refresh Buffer Card

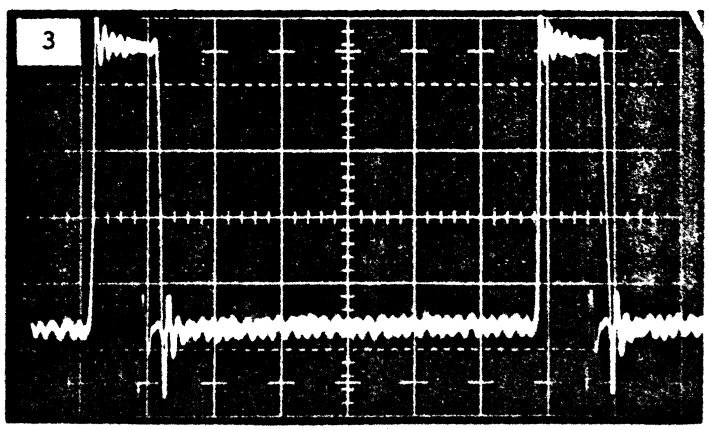


WAVEFORM 3: Clock Timing

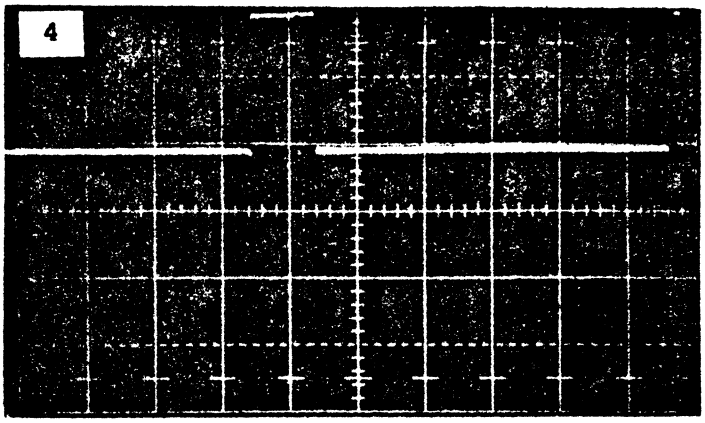
Oscilloscope Settings;
Vertical, 1 V/cm
Horizontal, 0.1 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XE4, XE2-8, Timing Control Card



WAVEFORM 4: MATCH

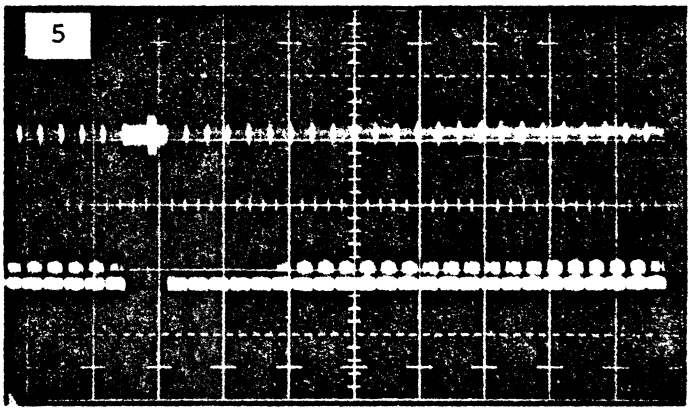


Oscilloscope Settings:
Vertical, 2 V/cm
Horizontal, 0.5 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XD4-8, XD5-11, XE5-4, XD3-8, XD2-10, Timing Control Card, Cursor Control Card, Refresh Buffer Card.

WAVEFORM 5: Video

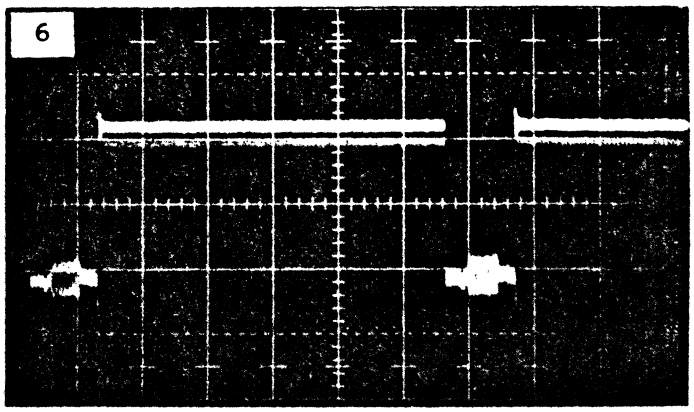


Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 2 msec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

CR3, XD1-6, XE1-6, XE1-8, XE1-11, XE1-3 and circuitry related to these components.

WAVEFORM 6: Video



Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 10 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

CR3, XD1-6, XE1-6, XE1-8, XE1-11, XE1-3 and circuitry related to these components.

WAVEFORM 7

(Not applicable to 8025G Terminal)

WAVEFORM 8

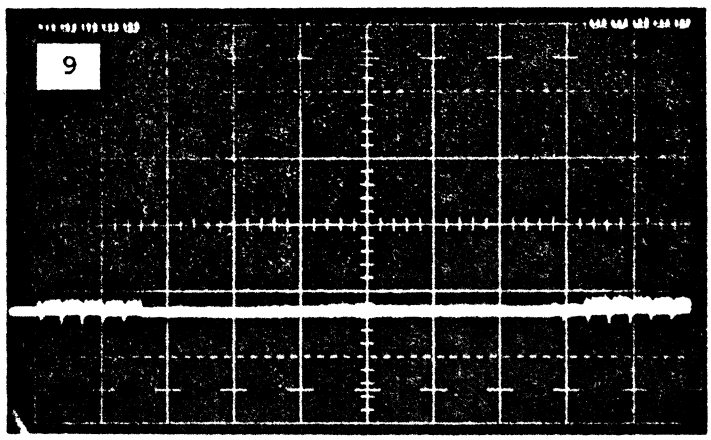
(Not applicable to 8025G Terminal)

WAVEFORM 9: Parallel-to-serial converter output

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 2 msec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XA2, XA4, Refresh Buffer Card

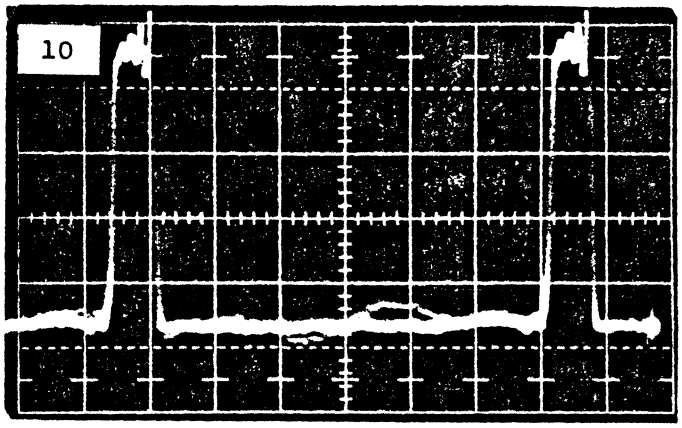


WAVEFORM 10: Parallel-to-serial converter output

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 0.1 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XA2, XA4, Refresh Buffer Card

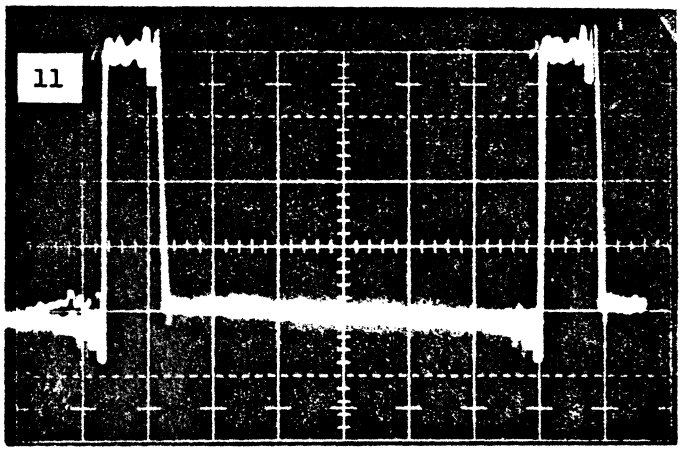


WAVEFORM 11: Clock Timing

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 0.1 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

Timing Control Card

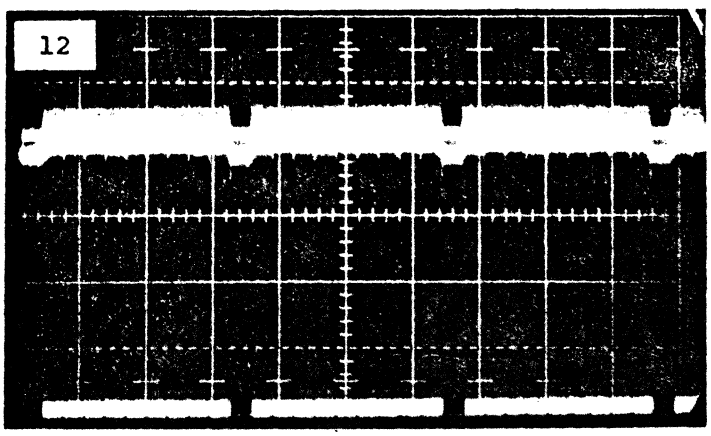


WAVEFORM 12: Clock Timing

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 0.2 msec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

Timing Control Card

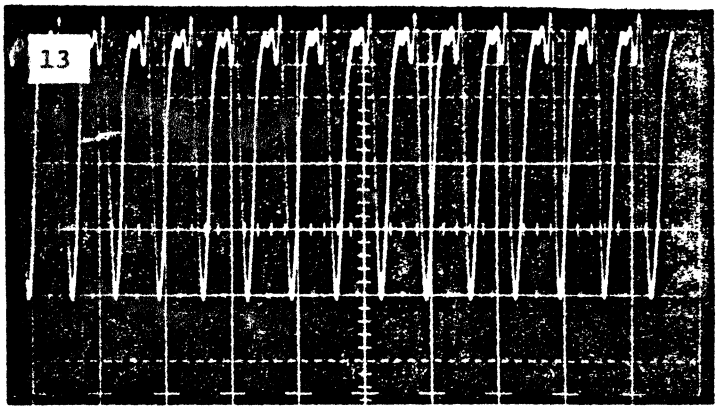


WAVEFORM 13: HF CLK

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 0.1 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

Timing Control Card

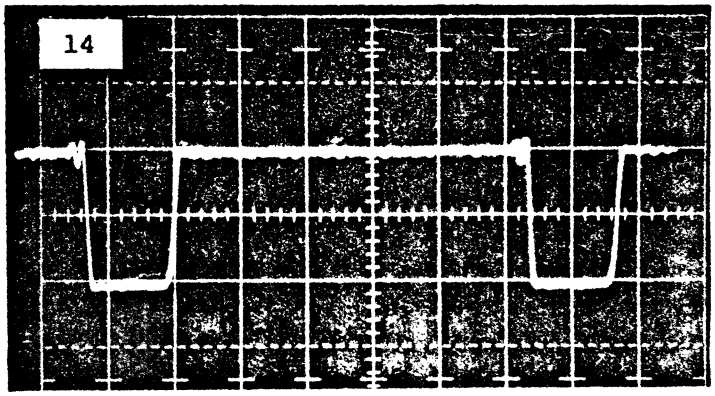


WAVEFORM 14: H8 Clocks

Oscilloscope Settings:
Vertical, 0.2 V/cm
Horizontal, 0.1 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XE5-6, Timing Control Card

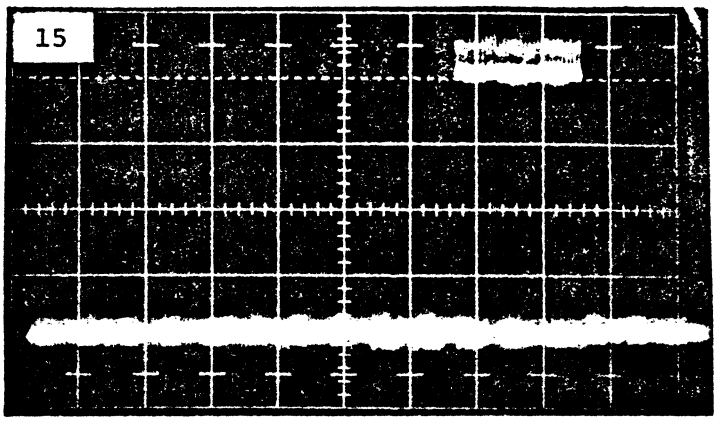


Refresh Buffer Card. Plug the card onto the extender card and insert in the terminal. Connect the ribbon connector. Check for the following signals in the order given:

WAVEFORM 15: Each CG bus line, one-half page data

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 2 msec/cm
Synchronization, internal

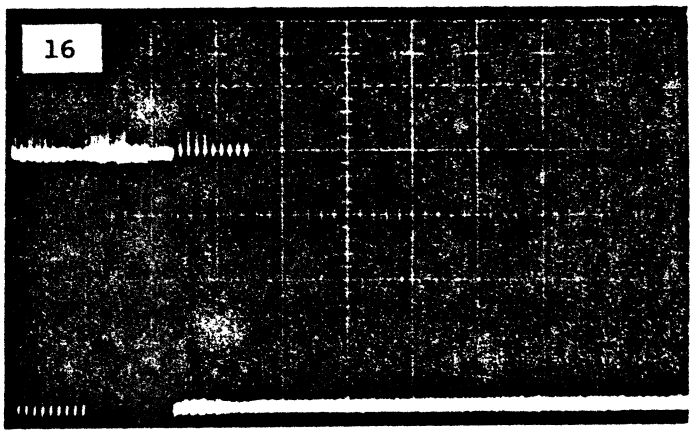
IF SIGNAL IS INCORRECT OR ABSENT, CHECK:
XE1-3, 6, 8, and 11; XD1-3, 6, 8 and 11.



WAVEFORM 16: Each CG bus line, one-half page data

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 0.5 msec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:
XE1-3, 6, 8, and 11; XD1-3, 6, 8 and 11.

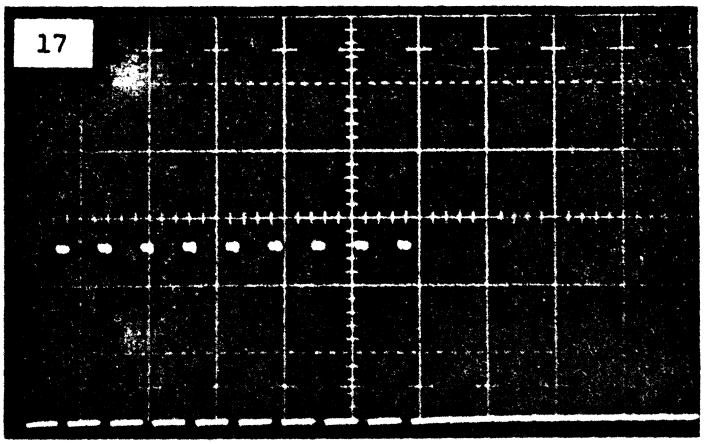


WAVEFORM 17: Refresh shift register outputs, one-half page data

Oscilloscope Settings:
Vertical, 2 V/cm
Horizontal, 0.1 msec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

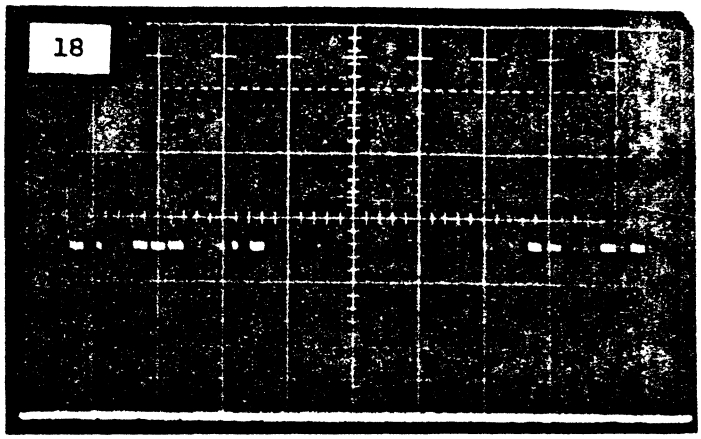
XE2, XD2, REG 2 Clock and load circuitry.



WAVEFORM 18: Next-line shift register outputs, one-half page data

Oscilloscope Settings:
Vertical, 2 V/cm
Horizontal, 0.1 msec/cm
Synchronization, internal

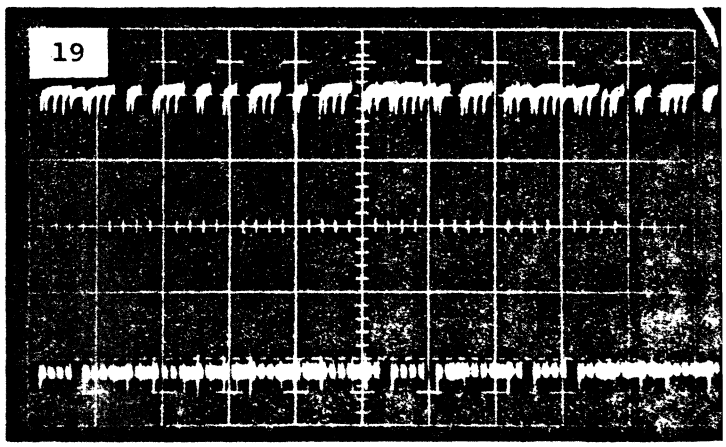
IF SIGNAL IS INCORRECT OR ABSENT, CHECK:
XE3, XD3, REG 1 clock circuitry



WAVEFORM 19: Next-line shift register inputs, one-half page data

Oscilloscope Settings:
Vertical 1 V/cm
Horizontal, 2 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:
XE4-1, 4, 10, 13; XD4-1, 4, 10, 13; XB6-2; XC4-3, 6, 8, 11; XB4-3, 6, 8, 11; XD6-12, Refresh Memory Card

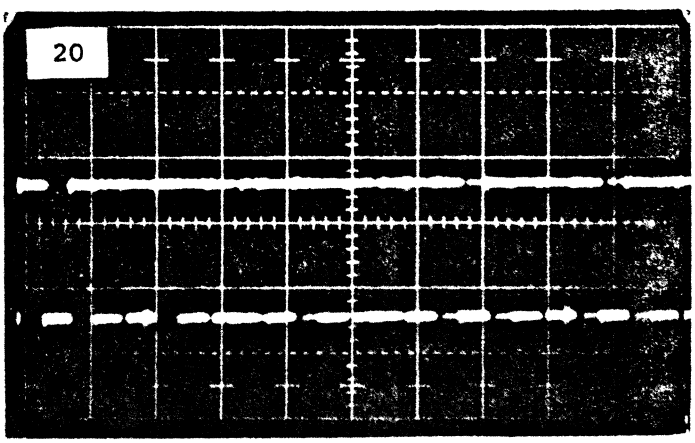


WAVEFORM 20: CPU BUSY

Oscilloscope Settings:
Vertical, 2 V/cm
Horizontal, 10 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XB6-8, Processor Card

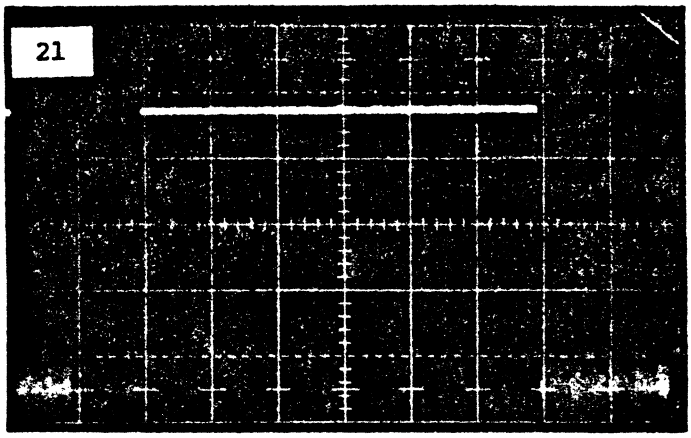


WAVEFORM 21: BLINK

Oscilloscope Settings:
Vertical, 2 V/cm
Horizontal, 50 msec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XC6-6, XC5, XD5-11, XD5-3, Timing Control Card

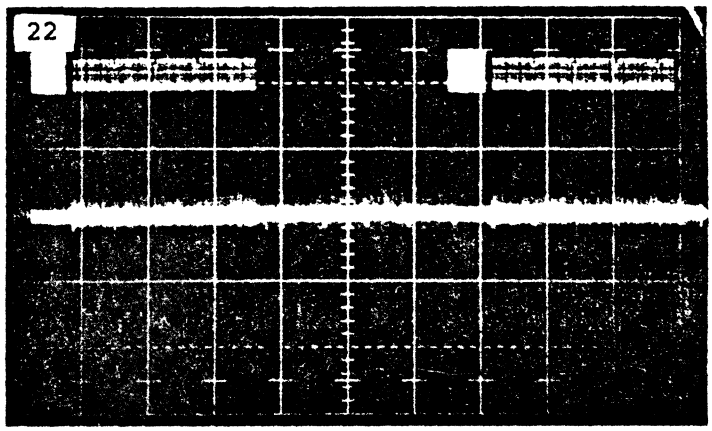


WAVEFORM 22: REG 1 CLK

Oscilloscope Settings:
Vertical, 2 V/cm
Horizontal, 0.1 msec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XB5-8 and related input circuitry



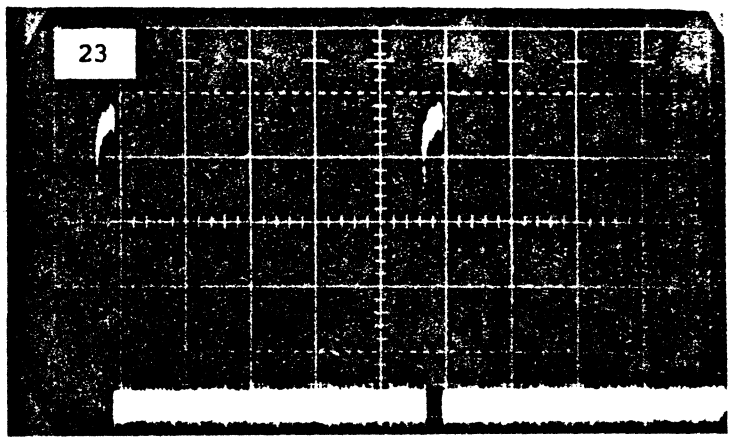
Timing Control Card. Plug the card onto the extender card and insert in the terminal. Check for the following signals in the order given:

WAVEFORM 23: I/O Command

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 10 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XE5-6, XF5-4, XF5-10, Processor Card

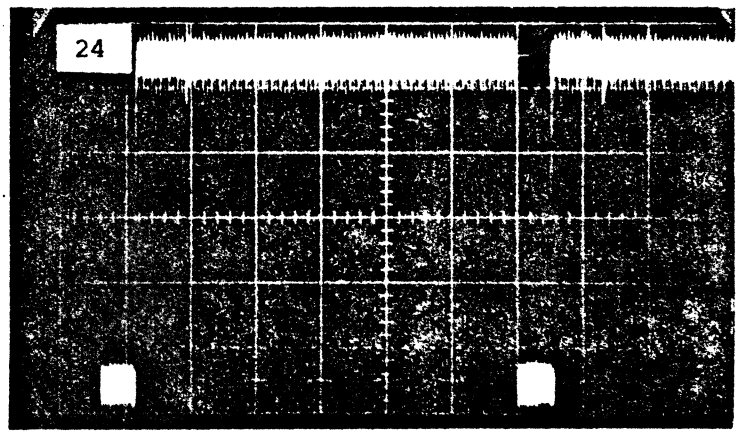


WAVEFORM 24: V SYNC

Oscilloscope Settings:
Verticle, 1V/cm
Horizontal, 10 usec/cm
Synchonization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XF4-12, XE3, circuitry related to pin 4 of XE3

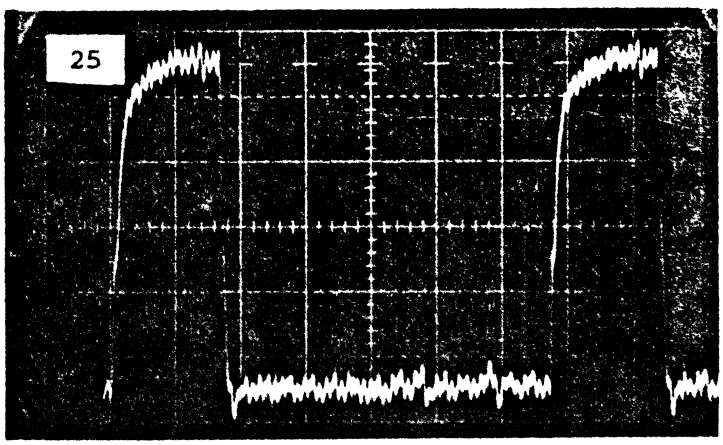


WAVEFORM 25: H SYNC

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 0.2 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

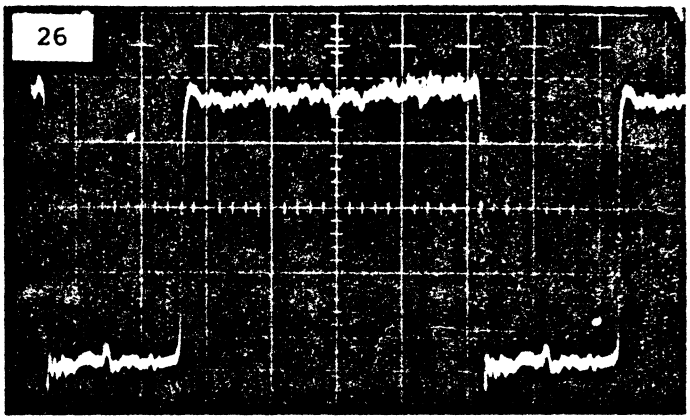
XF4-10, XE3, circuitry related to pin 13 of XE3



WAVEFORM 26: Vertical Timing (V1, V2, V4, V8)

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 0.2 usec/cm
Synchronization, internal

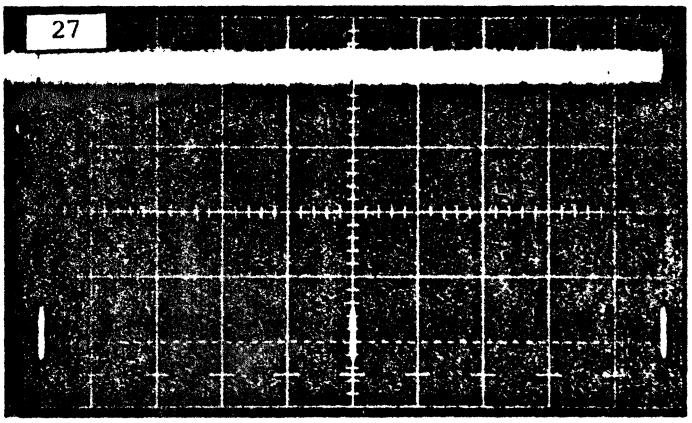
IF SIGNAL IS INCORRECT OR ABSENT, CHECK:
XF1-2, 4, 6, 8; XC1; $\overline{\text{H BLNK}}$ circuitry



WAVEFORM 27: POLL

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 50 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:
XD4-6, XE4

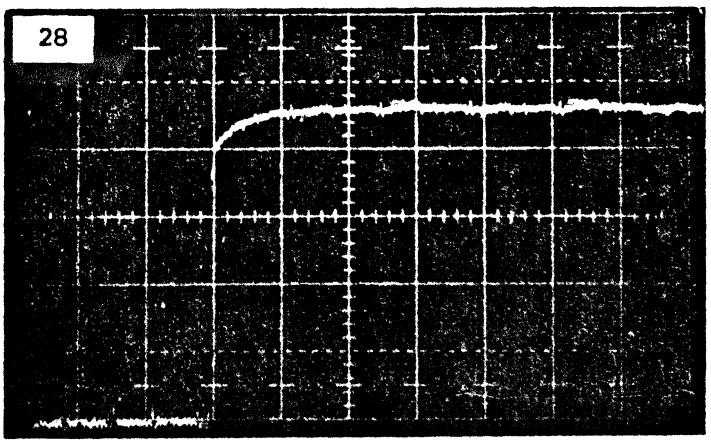


WAVEFORM 28: POLL

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 1 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XD4-6, XE4

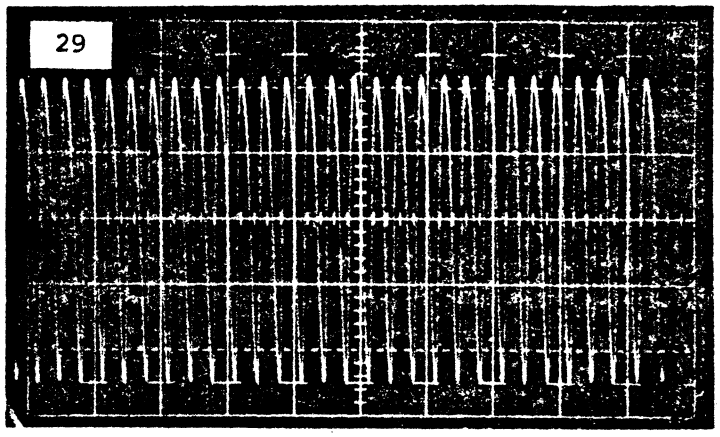


WAVEFORM 29: Master Clock, 29.952 MHz

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 0.1 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XB1-8, Q2, Q1, Y1 and related components.

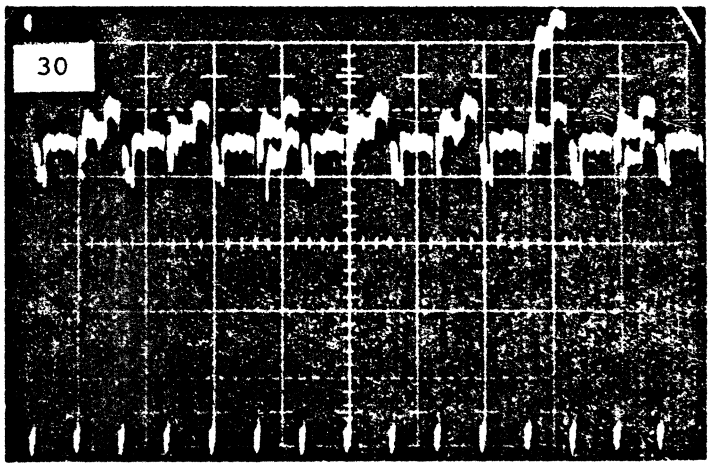


WAVEFORM 30: $\overline{\text{LDCNT}}$

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 10 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XE2-8, XE6, XF6-4, XF5-13, XD5

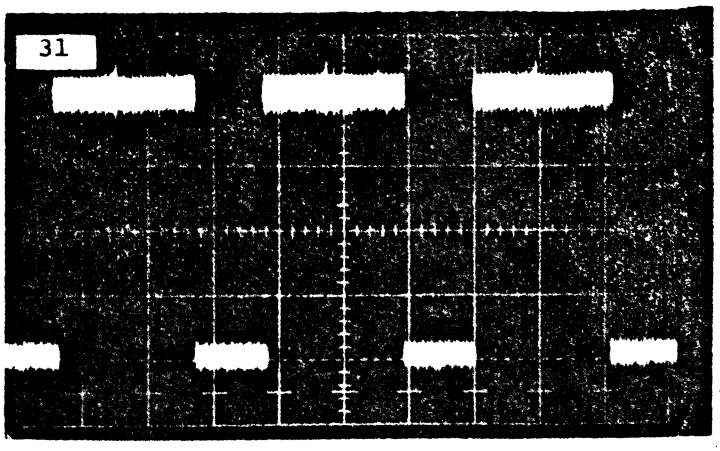


WAVEFORM 31: H320

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 10 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XC2

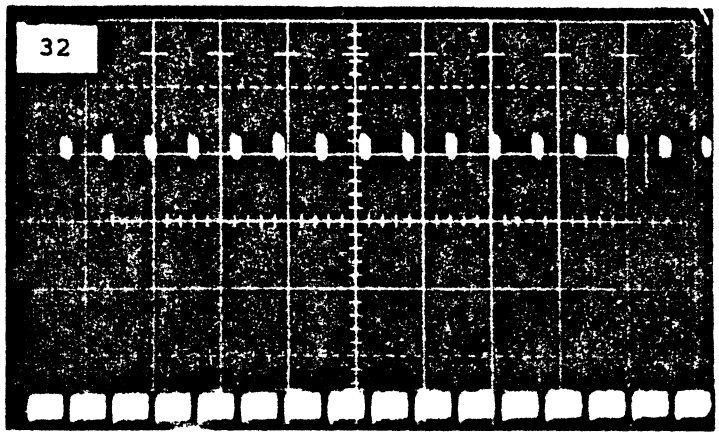


WAVEFORM 32: HF CLK

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 0.1 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XB1-3, XB1-11, XA1



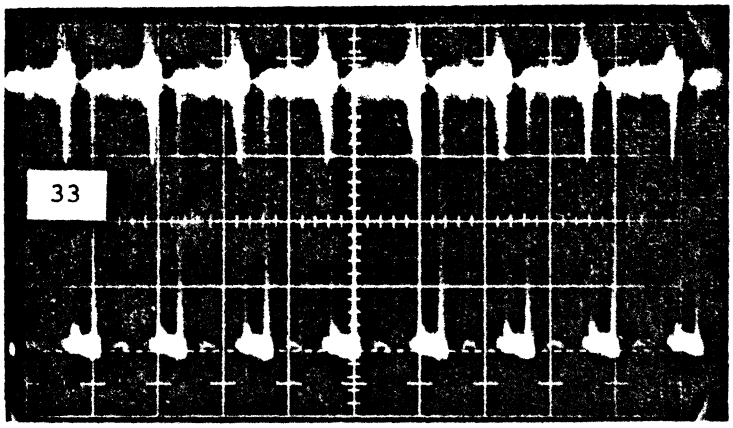
Refresh Control Card. Plug the card onto the extender card and insert in the terminal. Check for the following signals in the order given:

WAVEFORM 33: Each RD bus line

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 1 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

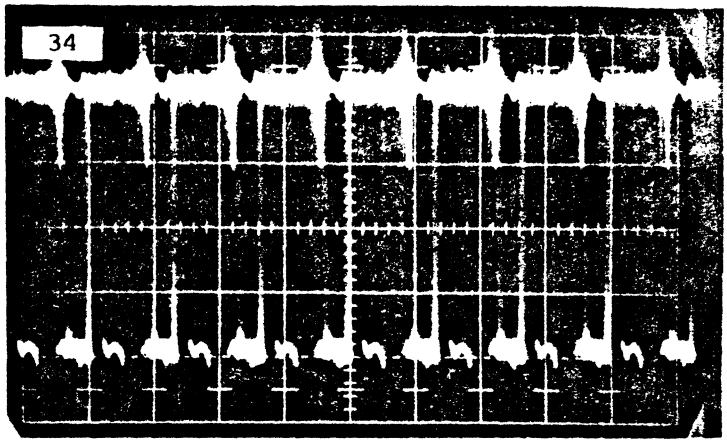
XE1-4, 6, 8, 10; XE2-4, 6, 8, 10



WAVEFORM 34: Each MA bus line

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 1 usec/cm
Synchronization, internal

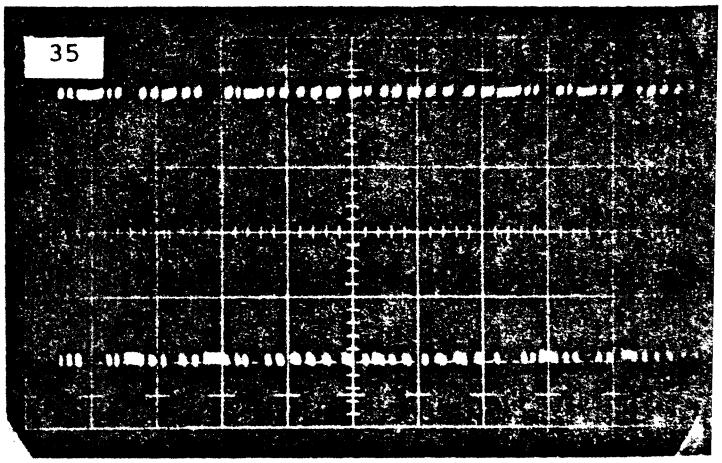
IF SIGNAL IS INCORRECT OR ABSENT, CHECK:
XE3-3, 6, 8, 11; XE4-3, 6, 8, 11;
XE5-3, 6, 8, 11; XE6-3, 6, 8, 11;
related input circuitry



WAVEFORM 35: Address counter (XC4) outputs

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 1 msec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:
XC4, XC3, XA3-11, XB4-3, XB4-6, XB6-8, XD4-2, XD3-2, XE2-12, Timing Control Card

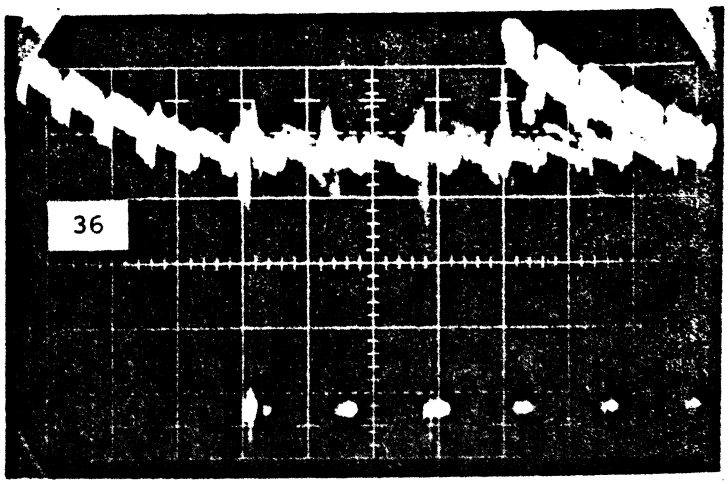


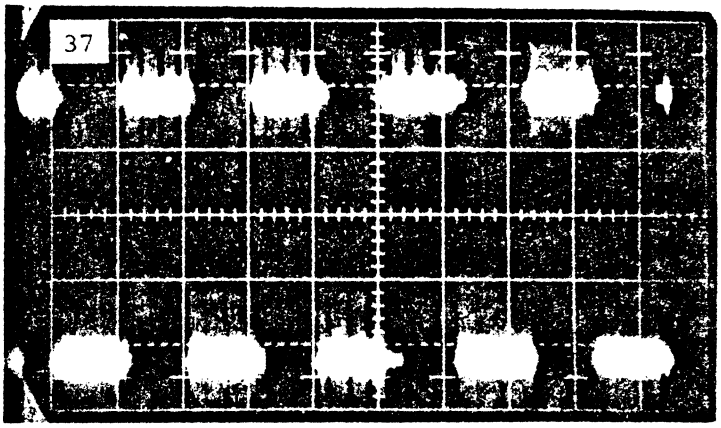
WAVEFORM 36: RM-4,5,6,7

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 1 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

Refresh Memory Card



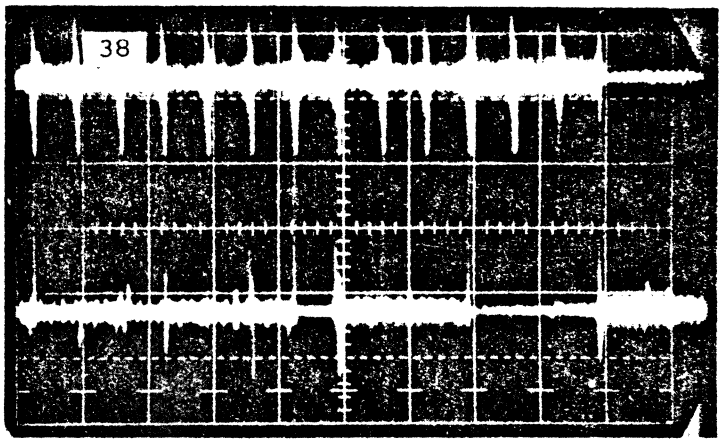


WAVEFORM 37: Address counter (XC5) outputs

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 2 msec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XC5

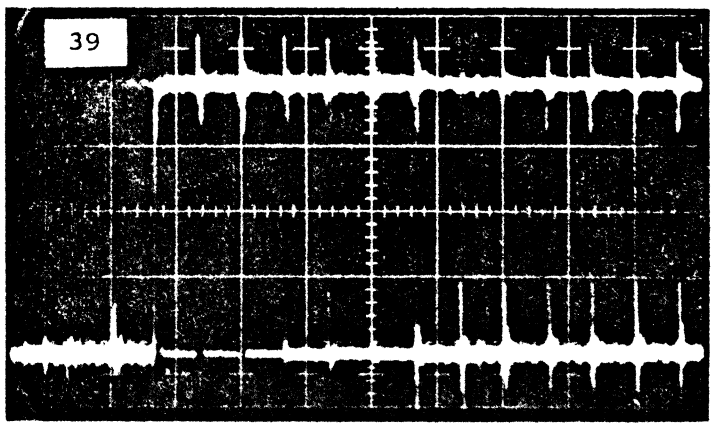


WAVEFORM 38: RM0,1,2,3

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 2 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

Input circuitry to XC5, Refresh Memory Card



WAVEFORM 39: Address counter (XC3) outputs

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 2 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

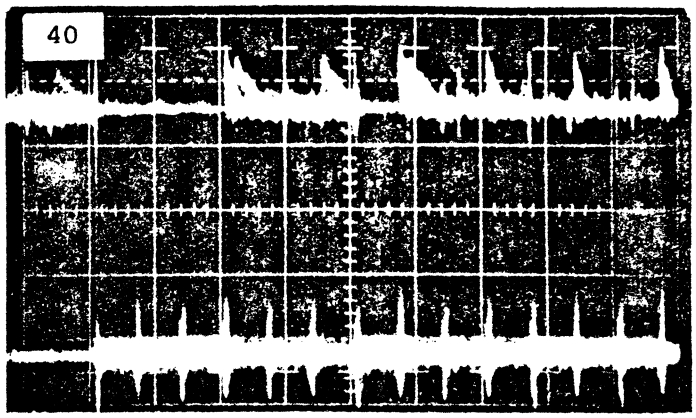
XC3

WAVEFORM 40: RM0,1,2,3

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 2 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

Refresh Memory Card

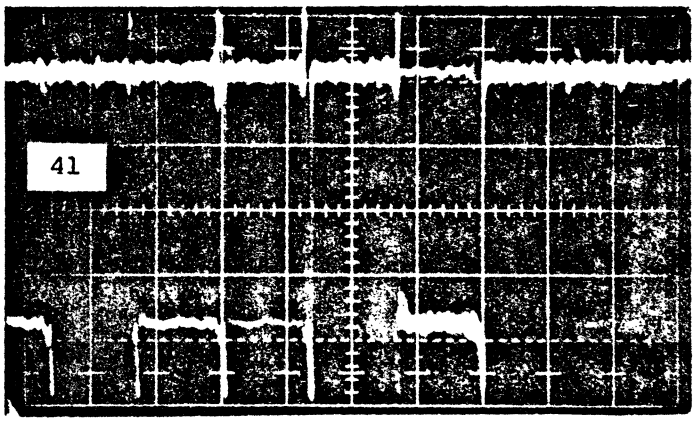


WAVEFORM 41: MA bus enable

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 1 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XB4-3, XB4-6, related input circuitry

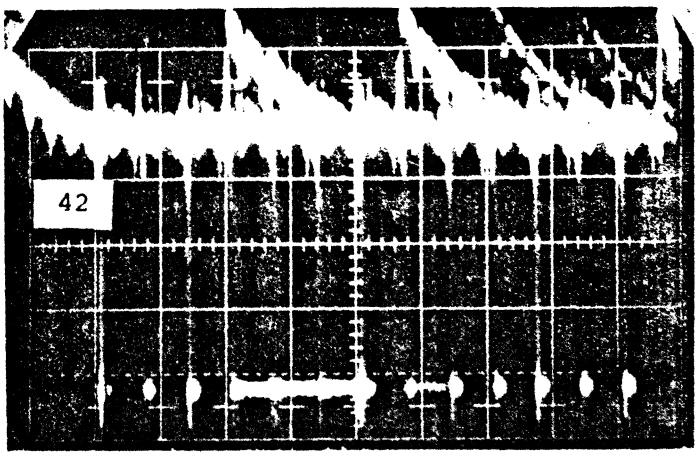


WAVEFORM 42: RM-4, 5, 6, 7

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 2 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

Refresh Memory Card



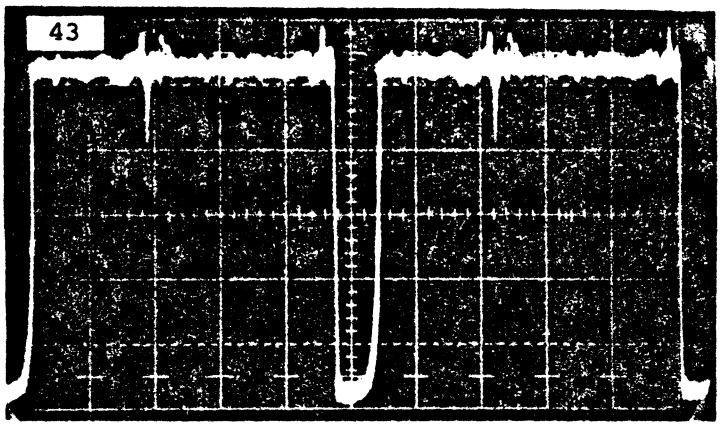
Processor Card. Plug the card onto the extender card and insert in the terminal. Check for the following signals in the order given:

WAVEFORM 43: IC CLK

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 0.5 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XC6-2, XC2, Timing Control Card

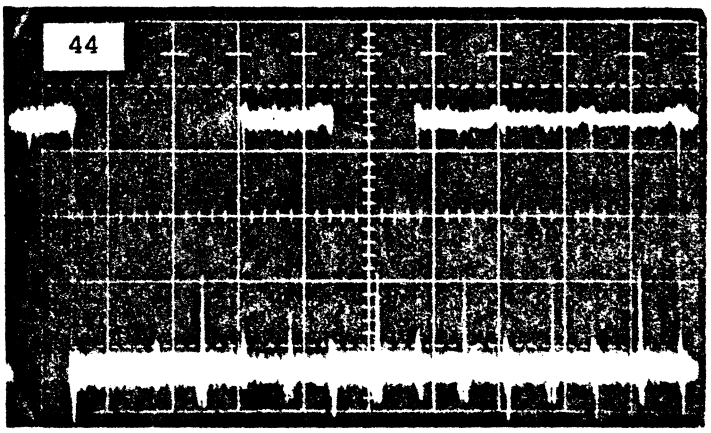


WAVEFORM 44: CPU Timing

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 2 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

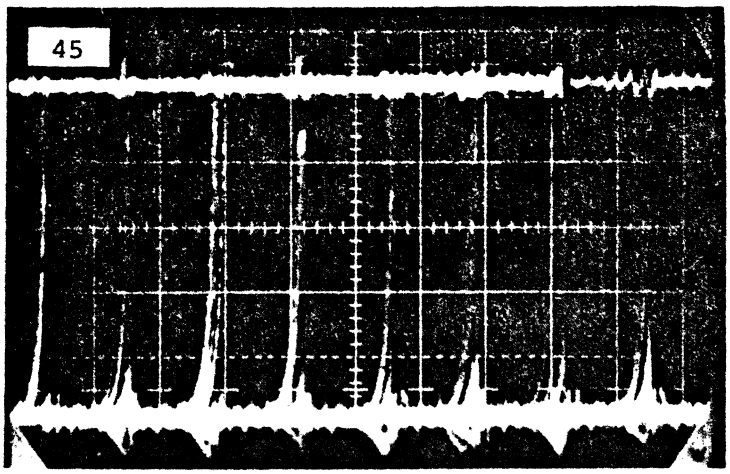
XA4, XB2, circuitry related to inputs to XA4



WAVEFORM 45: Each MA bus line

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 1 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:
XF6-8; XE4-3,6,8,11; XF4-3,6,8,11; XE5-3,6; XF5-3,6,8,11; XD2; XD4; XD3; XD5; input circuitry related to XD2, XD4, XD3 and XD5

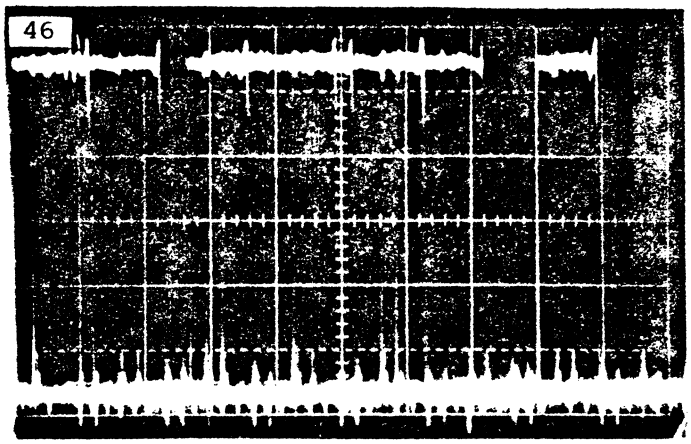


WAVEFORM 46: Each B Data Bus line

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 2 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XF1-3, 6, 8, 11; XF2-3, 6, 8, 11; related input circuitry

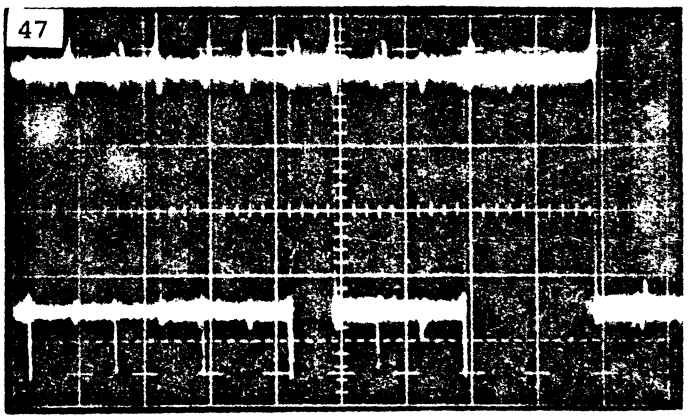


WAVEFORM 47: CPU BUSY

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 2 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XE6-8 and related input circuits

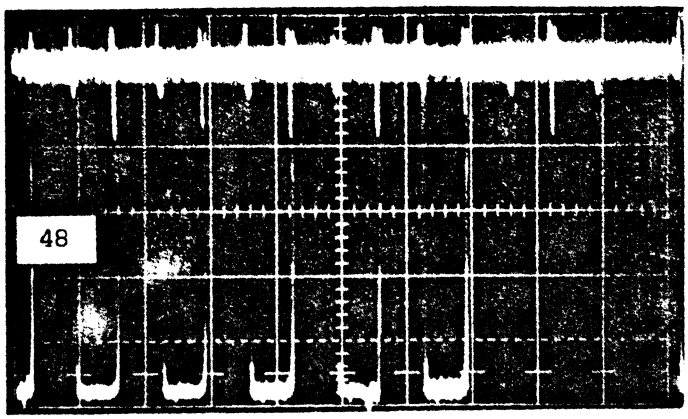


WAVEFORM 48: $\overline{T2}$

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 2 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XB4-6, XA2-3, input circuitry related to XA2-3

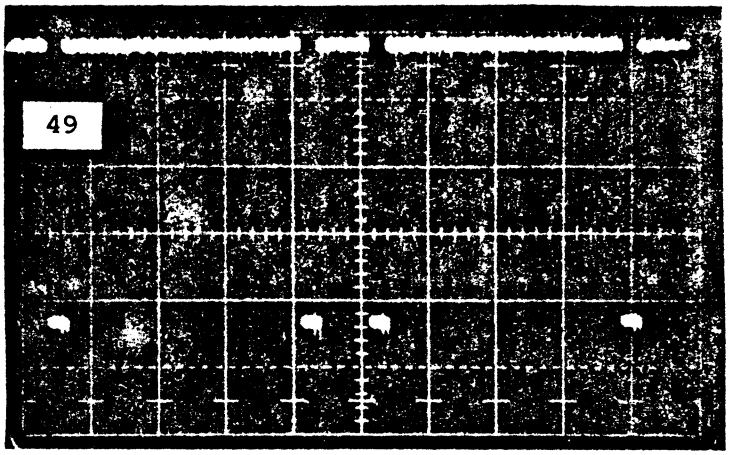


WAVEFORM 49: WAIT

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 2 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XE5-11, XA5

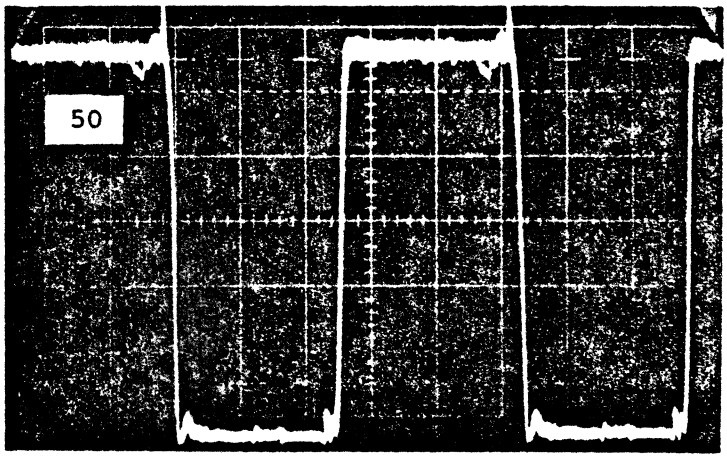


WAVEFORM 50: SYNC

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 0.5 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XC2

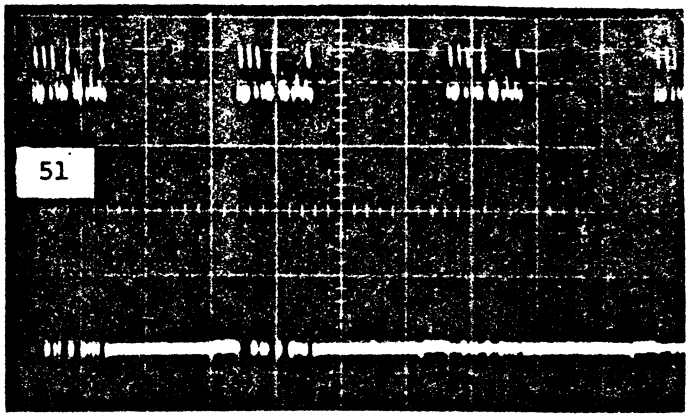


RS-232 Interface. Plug the card onto the extender card and insert in the terminal. Connect the ribbon cables. Check for the following waveforms in the order given:

WAVEFORM 51: Each A Data Bus line

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 1 msec/cm
Synch ronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:
XE1-3, 6, 8, 11; XG1-3, 6, 11; related input circuitry to XE1 and XG1; Timing Control Card

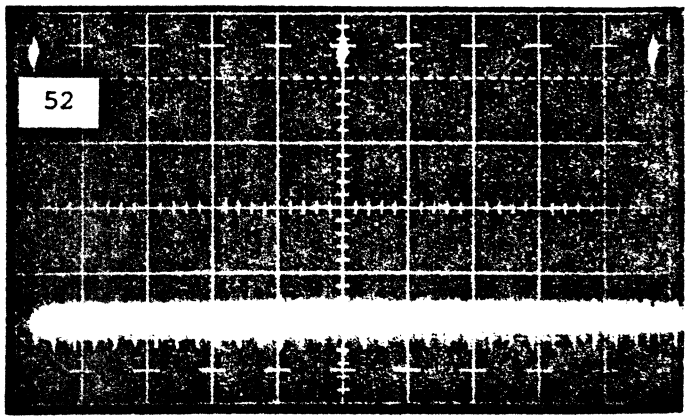


WAVEFORM 52: POLL OUT

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 50 msec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XG6-3 and related input circuitry, Timing Control Card

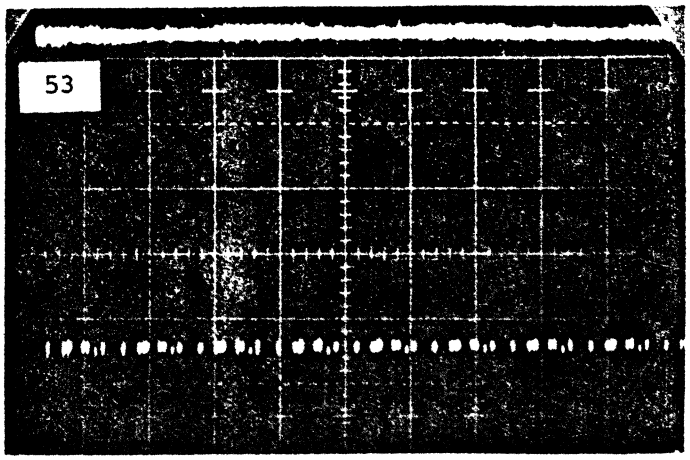


WAVEFORM 53: Reset Command (MA1,2,3,4)

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 2 msec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

Processor Card

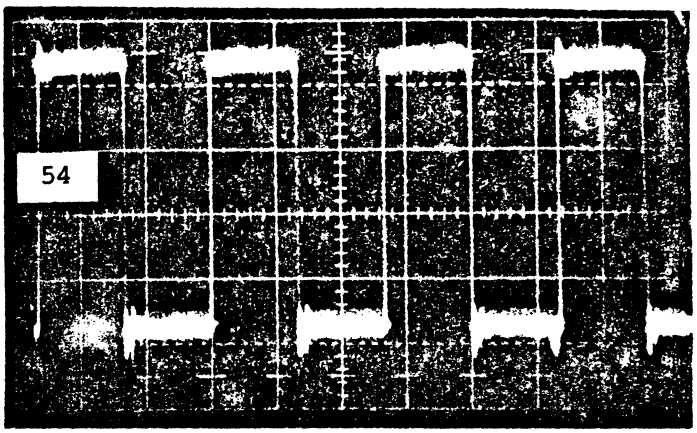


WAVEFORM 54: STAT

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 1 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XG4-8, Timing Control Card

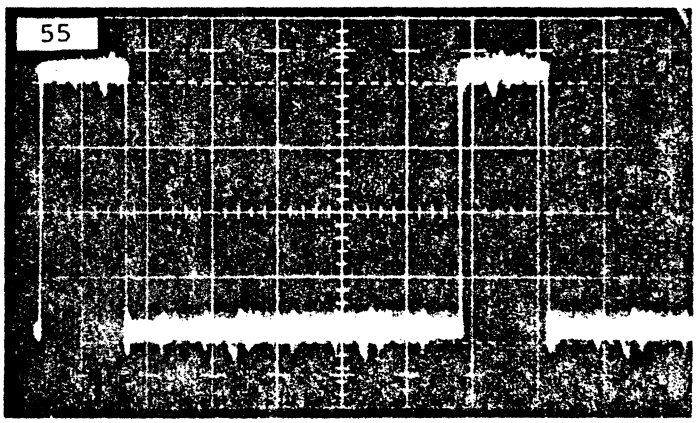


WAVEFORM 55: RS CLK

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 1 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XB1-2, Timing Control Card

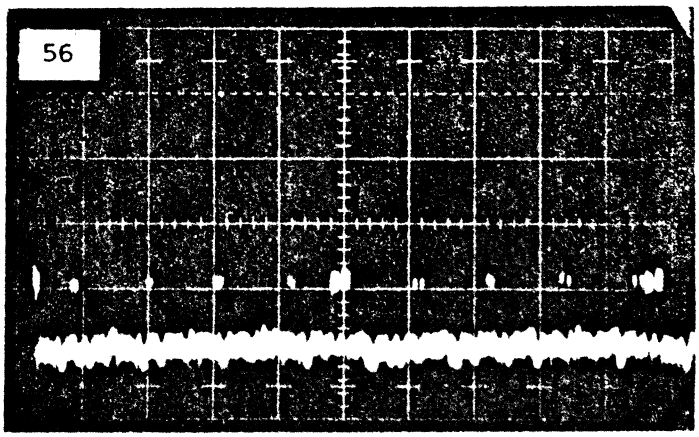


WAVEFORM 56: Address comparator output

Oscilloscope Settings:
Vertical, 0.2 V/cm
Horizontal, 50 msec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XD3-3, 4, 10, 11



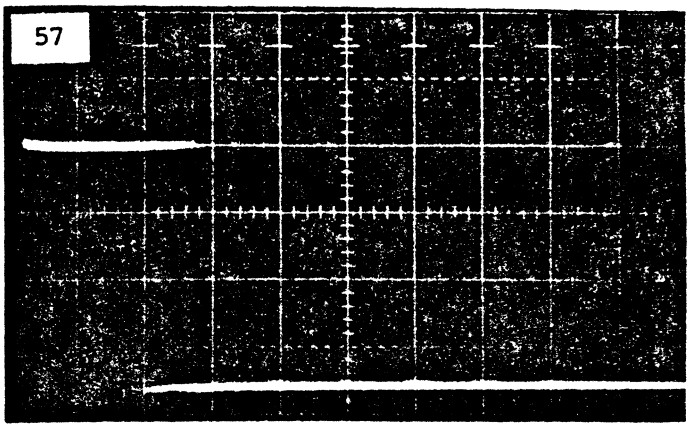
Cursor Control Card. Plug the card onto the extender card and insert in the terminal. Connect the ribbon cable. Check for the following waveforms in the order given:

WAVEFORM 57: DSO

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 1 usec/cm
Synchonization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XD3-2, Keyboard Card (encoder)

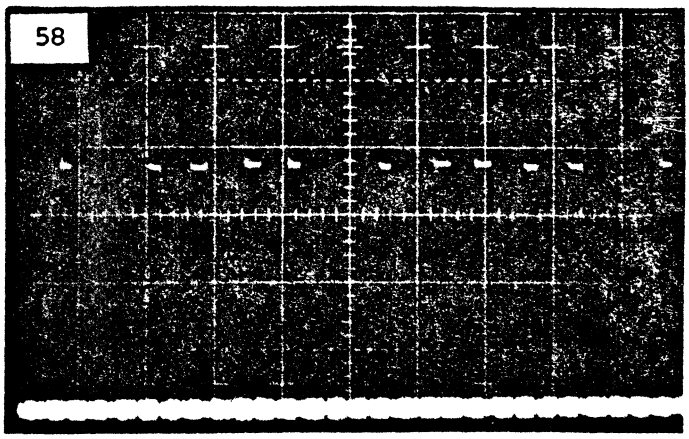


WAVEFORM 58: DSO

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 2 msec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

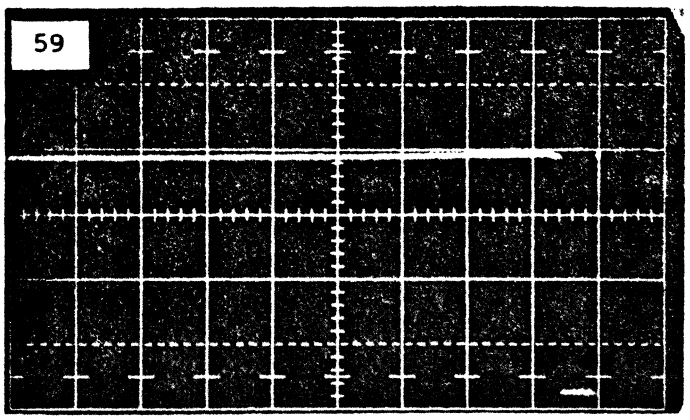
XD3-2, Keyboard Card (encoder)



WAVEFORM 59: KYBD STROBE

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal 0.1 usec/cm
Synchronization, internal

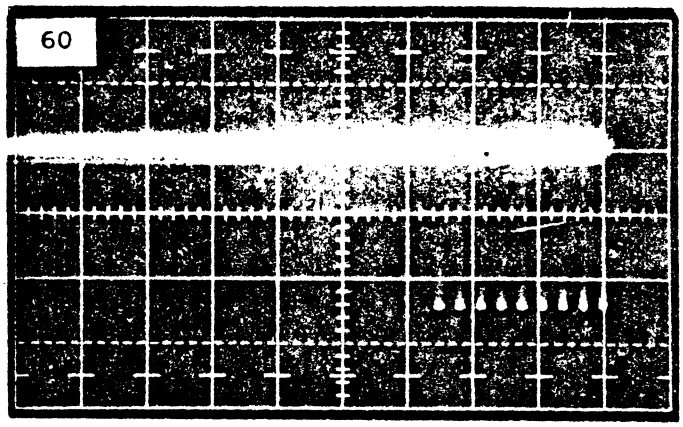
IF SIGNAL IS INCORRECT OR ABSENT, CHECK:
XD3-6, XB2-6, circuitry related to pin 4 of XB2, Timing Control Card



WAVEFORM 60; MATCH

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 20 msec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:
XC5-3,4,10,11; XD5-3,4,10,11; XE5-3,4,10,11; input circuitry to XC5, XD5 and XE5

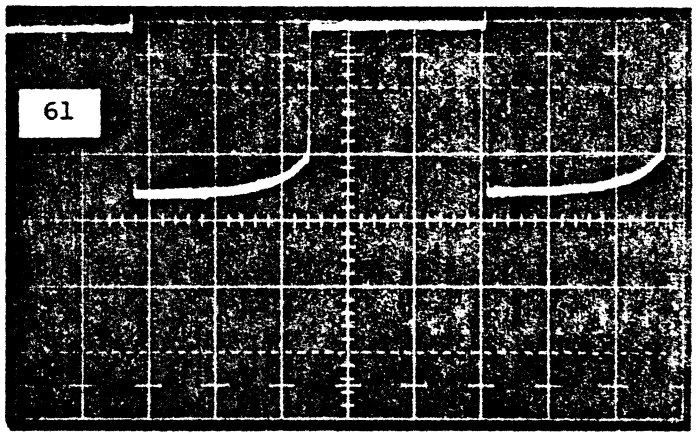


WAVEFORM 61: H40 ($\overline{CP}$) Clock

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 20 usec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XD3-4, Timing Control Card

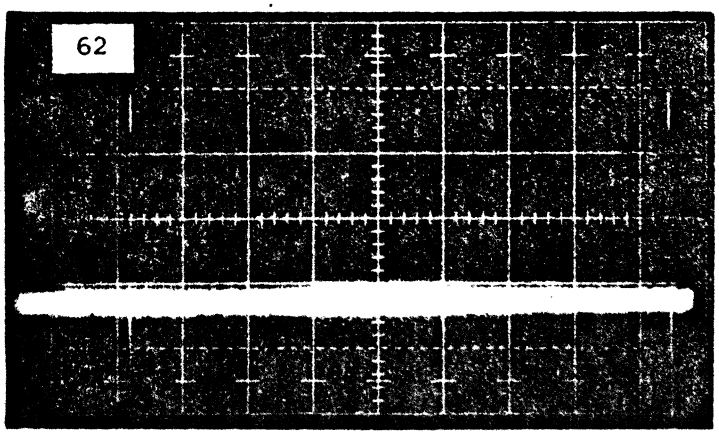


WAVEFORM 62: Click

Oscilloscope Settings:
Vertical, 2 V/cm
Horizontal, 10 msec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XA1

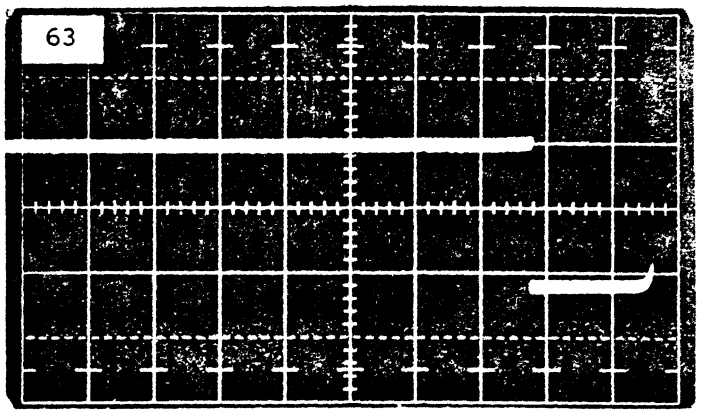


WAVEFORM 63: Click

Oscilloscope Settings:
Vertical, 2 V/cm
Horizontal, 0.2 msec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XA1

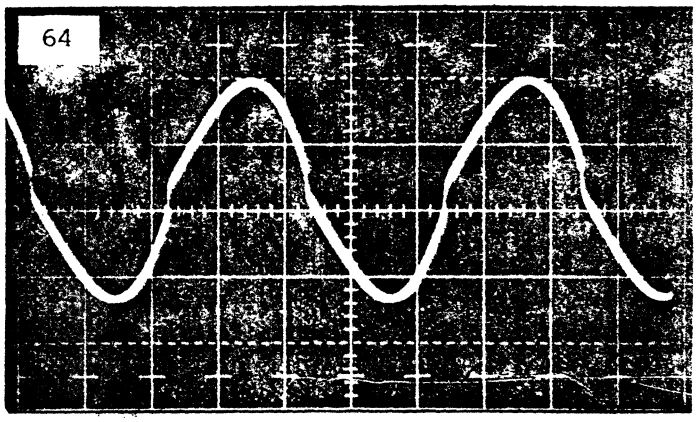


WAVEFORM 64: Beep

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, 0.1 msec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XA4-10, Q1, XA1, Refresh Buffer Card

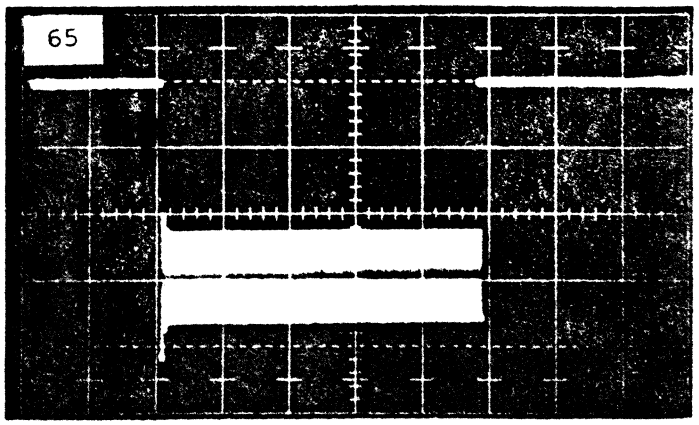


WAVEFORM 65: Beep

Oscilloscope Settings:
Vertical, 5 V/cm
Horizontal, 10 msec/cm
Synchronization, internal

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

XA4-10, Q1, XA1, Refresh Buffer Card



Refresh Memory Card. Do not perform bench maintenance on this card. Replace with an operational card and return the faulty card to OMRON for repair.

Program (PROM) Memory Card. Do not perform bench maintenance on this card. Replace with an operational card and return the faulty card to OMRON for repair.

Keyboard Card. Except for key switch and encoder replacement (refer to Paragraph 6.2), do not perform bench service on this card. Replace with an operational card and return the faulty card to OMRON for repair.

Motherboard. Do not perform bench service on this board. Replace with an operational board and return the faulty board to OMRON for repair.

LED Assembly. Except for damage to the printed circuit card, a non-operational LED (light emitting diode) is the only malfunction that can exist in this assembly.

To test LEDs, apply 5 V dc to pin 8 or 9 of P24. Then individually ground the cathode of each LED. Replace any LED that does not turn on. If an operational LED does not turn on under normal terminal operation, the problem is probably on the Refresh Buffer Card.

Power Supply Assembly and Regulator Card. Basic power supply and regulator circuitry is used in the terminal. Use standard voltage and resistance measurement techniques to isolate problems in these two sections.

Terminator Card. The Terminator Card consists of five integrated-circuit resistive networks (X1 through X5). A malfunction in a network is detected by measuring the resistance between pin 16 and each of the other pins (1 through 15). The readings should be 330 ohms on X1 through X4 and 470 ohms on X5.

CRT Display. Once a malfunction is narrowed to the CRT Display section, the fault can be further isolated to a circuit and component as follows:

NOTE: Before troubleshooting the CRT display, be sure the problem is not caused by incorrect adjustment settings (refer to Section 7) or absence of terminal inputs to the display.

1. Many malfunctions can be narrowed to a section or circuit by analyzing the display presentation. When you are able to locate the problem area with this technique, proceed to Step 3.

2. Measure +55 V dc. Connect the positive lead to the cathode of CR106 and the negative lead to ground.

NOTE: If +55 V dc is correct, go immediately to Step 3.

a. If the voltage is too high, Q113 may fire erratically and cause raster "tearing".

b. A short circuit causes the regulator to "foldback" to limit the current. This condition is indicated by a low or zero voltage at the cathode of CR106.

c. If the voltage cycles from low to high at high rate (about 1,000 times per second), the horizontal output stage (Q123) is probably faulty. A low, audible buzz is often associated with this problem.

d. If the voltage cycles from low to high at or near the vertical rate, excessive pulse current is probably being drawn by the vertical output amplifier (Q122).

e. Disconnect P104 to isolate Q122 and P110 to isolate Q123 and the flyback transformer (T103). Use a short alligator-clip lead between the chassis and anode of VR101 to re-establish ground connection.

f. If the regulator continues to perform abnormally, the problem is probably a shorted electrolytic capacitor or defective components in the regulator circuit.

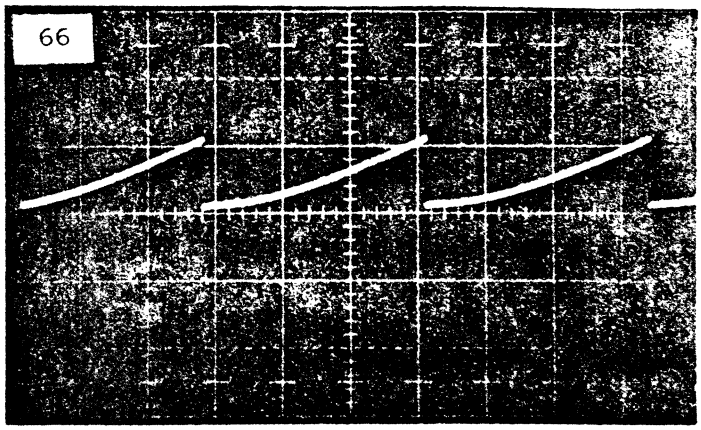
g. If the regulator performs normally, isolate the problem to individual stages as outlined in Step 3.

3. Check for the following waveforms in the order given.

WAVEFORM 66: Q101 Anode

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, field rate
Synchronization; external
with leading edge of V SYNC

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:
R106-108, C103 and C104, R102-104, CR101 and 102, Q101

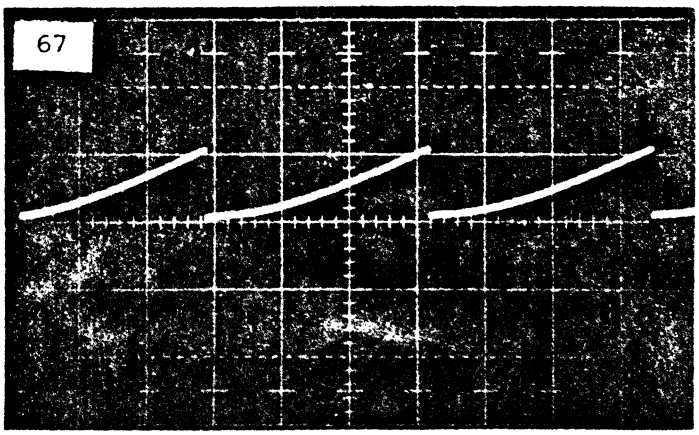


WAVEFORM 67: Q122 Base

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, field rate
Synchronization; external
with leading edge of V SYNC

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

R109 and 110, Q102

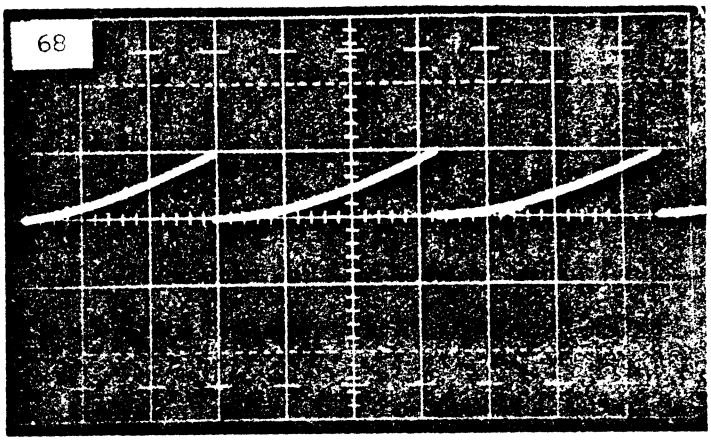


WAVEFORM 68: Q122 Emitter

Oscilloscope Settings:
Vertical, 1 V/cm
Horizontal, field rate
Synchronization; external
with leading edge of V SYNC

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

R114

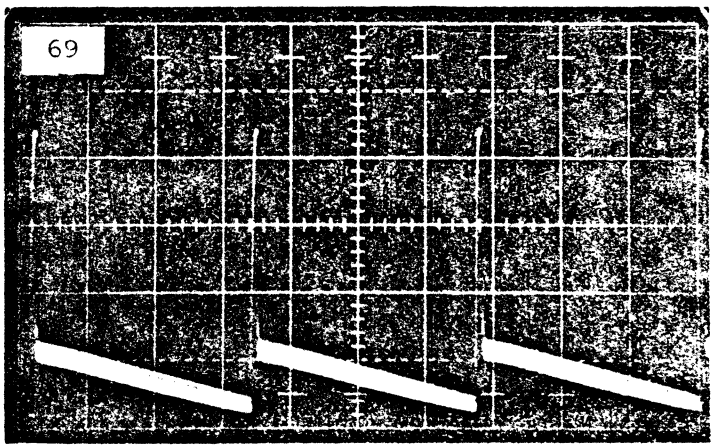


WAVEFORM 69: Q122 Collector

Oscilloscope Settings:
Vertical, 50 V/cm
Horizontal, field rate
Synchronization; external
with leading edge of V SYNC

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

CR103, R113 and C107, R121

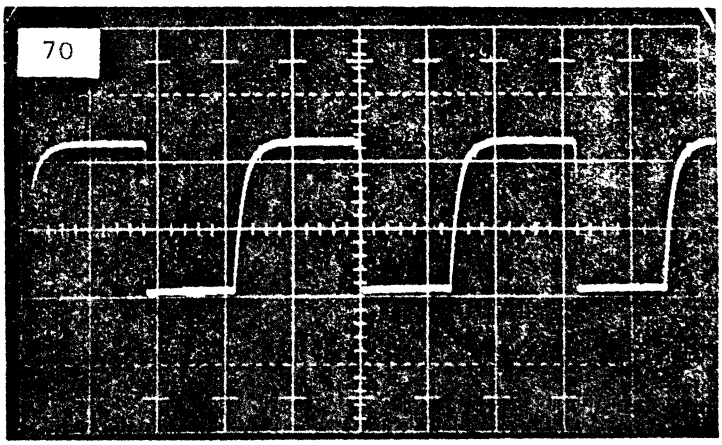


WAVEFORM 70: Q109 Collector

Oscilloscope Settings:
Vertical, 5 V/cm
Horizontal, line rate
Synchronization; external
with leading edge of H SYNC

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

R142 and C116, C114, Q110, Q109 and Q111

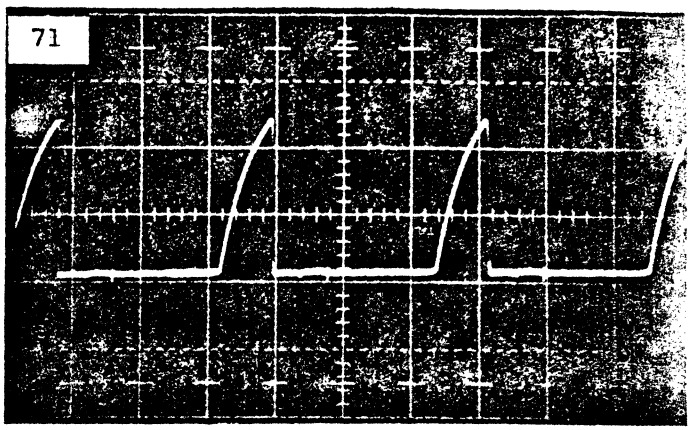


WAVEFORM 71: Q112 Collector

Oscilloscope Settings:
Vertical, 5 V/cm
Horizontal, line rate
Synchronization; external with leading edge of H SYNC

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

C117, CR108, R143 and R144, Q112

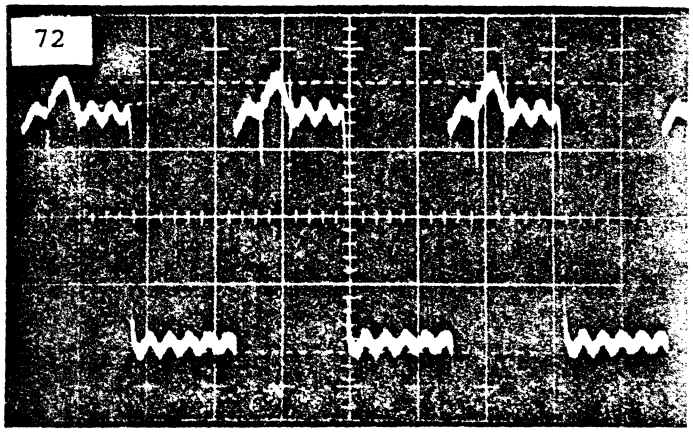


WAVEFORM 72: Q114 Collector

Oscilloscope Settings:
Vertical, 0.5 V/cm
Horizontal, line rate
Synchronization; external with leading edge of H SYNC

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

C121, R153, R156 and R157, C122, CR109, R152, C122, Q114 and Q115

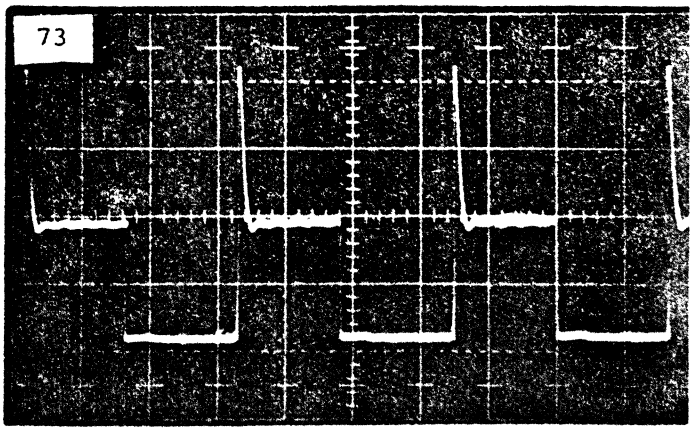


WAVEFORM 73: Q115 Collector

Oscilloscope Settings:
Vertical, 50 V/cm
Horizontal, line rate
Synchronization; external with leading edge of H SYNC

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

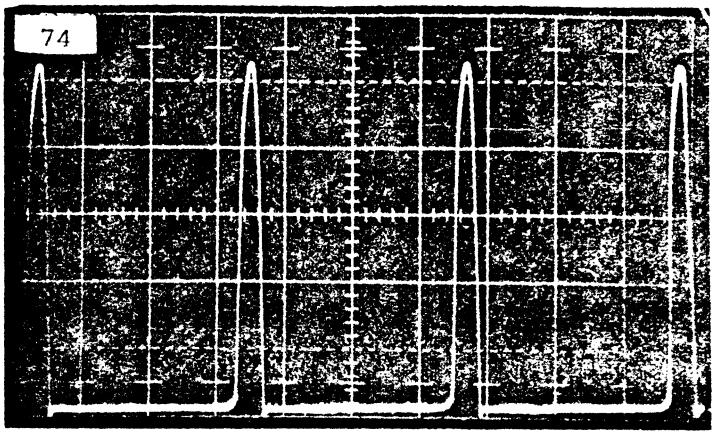
CR110, Q115



WAVEFORM 74: Q123 Collector (horizontal flyback pulse)

Oscilloscope Settings:
Vertical, 100 V/cm
Horizontal, line rate
Synchronization; external with leading edge of H SYNC

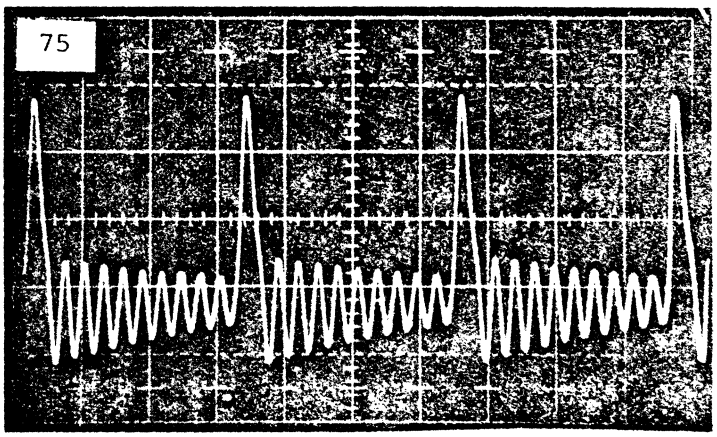
IF SIGNAL IS INCORRECT OR ABSENT, CHECK:
T101, Q123



WAVEFORM 75: Radiated Pulse from T103, 10:1, probe held 2" away, AC coupled

Oscilloscope Settings:
Vertical, 50 V/cm
Horizontal, line rate
Synchronization; external with leading edge of H SYNC

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:
CR116 and C127, L124, T103

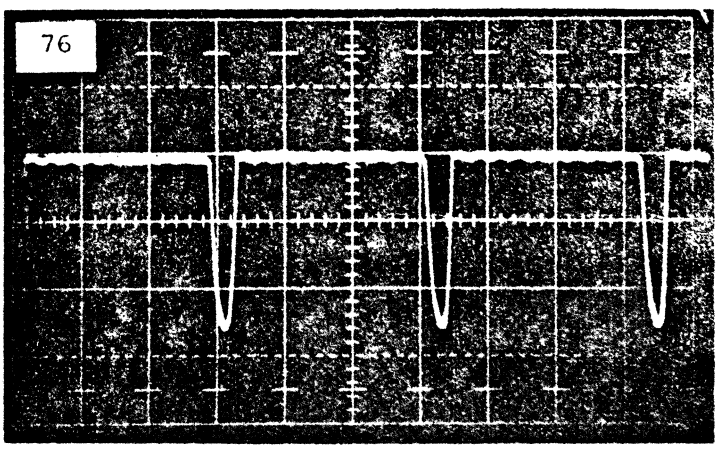


WAVEFORM 76: CR115 Cathode

Oscilloscope Settings:
Vertical, 50 V/cm
Horizontal, line rate
Synchronization; external with leading edge of H SYNC

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

C130, CR115

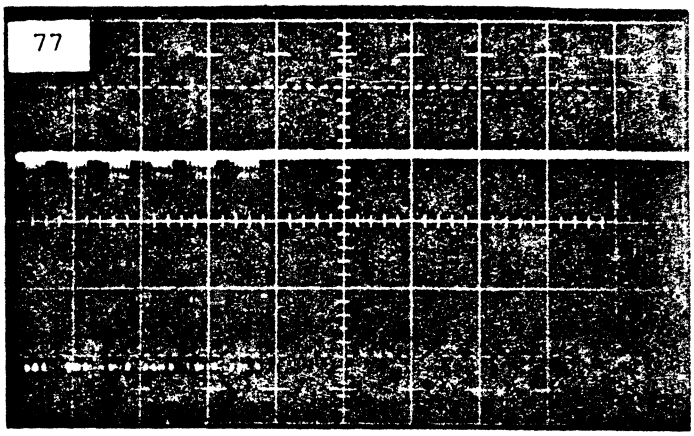


WAVEFORM 77: CRT (V1) Cathode

Oscilloscope Settings:
Vertical, 10 V/cm
Horizontal, line rate
Synchronization; external with leading edge of H SYNC

IF SIGNAL IS INCORRECT OR ABSENT, CHECK:

Q103, Q104 and related components



6.3.8 Removal and Replacement Procedures

Circuit Card Removal and Replacement. The procedure for removing and replacing circuit cards is given in Paragraph 6.2.5.

CAUTION: IMPROPER HANDLING CAN DAMAGE CIRCUIT CARDS. REFER TO PARAGRAPH 6.2.5.

Printed Circuit Card Components. To remove or install components, other than semiconductor components, proceed as follows:

1. Scrape away any coating from the card pads with a sharp-edged instrument.
2. Use a heat sink (shunt) to protect adjacent components.
3. With a controlled-heat soldering iron, remove component and clear excess solder from mounting holes as quickly as possible.
4. Bend replacement component leads to fit the distance between mounting holes and insert leads.
5. Use a heat sink to protect the replacement component and adjacent components.
6. Solder and clip leads 1/8" minimum above the pad. Solder quickly and cleanly, using as little solder as possible.

Semiconductor Components. To remove or install semiconductor components, proceed as follows:

1. Note the pin arrangement when removing the component.
2. Isolate the component from the soldering iron with a heat sink (shunt).

3. With a controlled-heat soldering iron (47 watts maximum), remove the component and clear excess solder from the mounting holes as quickly as possible.

4. Insert the new component pins to match the arrangement of the old component.

5. Solder quickly and cleanly, using as little solder as possible.

Integrated Circuit Removal and Replacement. Integrated circuit (IC) components are installed in IC sockets. To remove, use an IC puller. When installing these components, make sure the IC is oriented the same way as the socket into which it is being installed.

CAUTION: TO PREVENT DAMAGE BY STATIC DISCHARGE, HANDLE IC COMPONENTS IN THE SAME WAY AS CIRCUIT CARDS. REFER TO PARAGRAPH 6.2.5.

Cathode Ray Tube (CRT) Removal and Replacement. To remove and install the CRT, proceed as follows:

1. Turn the terminal off and remove the ac plug.

2. Wait 2 to 3 minutes for the high voltage (H.V.) supply to drain.

3. Remove the top section of the cabinet (refer to Paragraph 6.2.5).

4. Peel the H.V. cap on the red lead back from the CRT (see Figure 6-6).

5. Discharge H.V. by shorting the H.V. lead and CRT anode button to ground. Also short the anode button to the aquadag coating on the CRT.

6. Remove the H.V. lead from the CRT by pinching the two spring wires together.

7. Disconnect P106 (yellow and green wires) and P111 (red and blue wires) from the Monitor Deflection Board (see Figure 6-5). Make sure the wires are free of any cabling or clamps.

8. Remove the CRT socket.

9. Remove the upper two bolts and loosen the lower two bolts shown in Figure 6-6.

10. Support the CRT face and remove the lower two bolts in Figure 6-6.

WARNING: WEAR SAFETY GOGGLES AND HEAVY GLOVES WHEN REMOVING OR INSTALLING THE CRT.

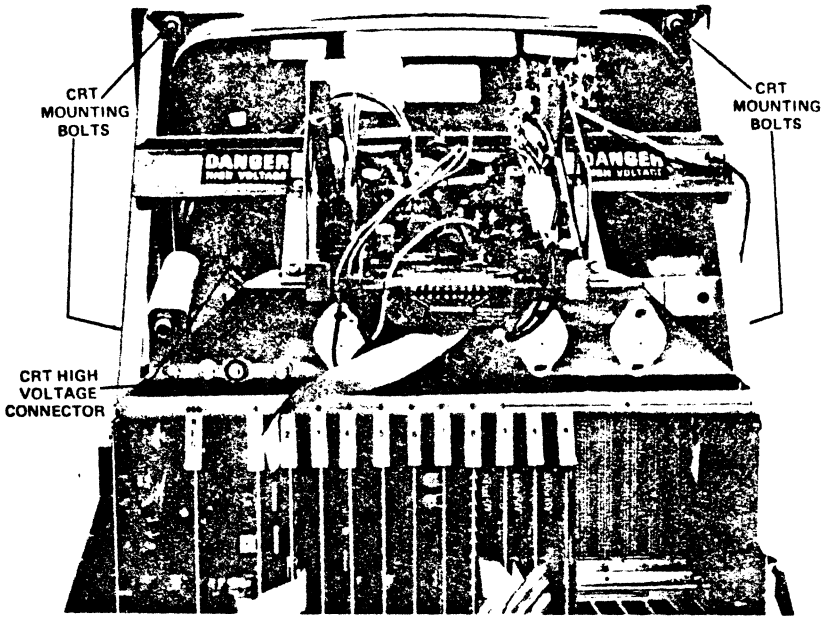


Figure 6-6. CRT mounting bolts and high voltage connector.

11. Face the screen and carefully pull the CRT with the yoke assembly toward you.

WARNING 1: DO NOT STRIKE OR SCRATCH OR USE MORE THAN MODERATE PRESSURE WHEN HANDLING THE CRT.

WARNING 2: STRESS IN THE CRT NECK CAN BREAK THE CRT AND CAUSE SERIOUS PERSONAL INJURY. HOLD THE CRT BY THE RIM OF THE FACE, NEVER BY THE NECK. YOU MAY GENTLY SUPPORT THE NECK, BUT ONLY TO STEADY AND GUIDE THE CRT.

12. Place the CRT face down on a soft grit-free surface.

13. Loosen the yoke-mounting screw (refer to Figure 7-14 in Section 7) and pull the yoke straight up and off the CRT neck.

WARNING: NEVER PRY THE YOKE OFF THE CRT NECK. TO DO SO MAY SCRATCH OR BREAK THE CRT.

14. To replace the CRT, install the deflection yoke and repeat steps 1 through 11 in reverse.

NOTE 1: Replace the CRT so that the anode button is on the right side as viewed from the front of the terminal.

NOTE 2: Make sure the CRT adjustments are correctly set (refer to Section 7).

7.1 REQUIRED EQUIPMENT

The following test equipment is needed to make adjustments in the 8025 CRT Terminal:

Triplett 310 Multimeter or equivalent

Tektronix 422 Oscilloscope or equivalent.

7.2 +5 V dc REGULATED OUTPUT

NOTE: Check that the line voltage is 117 V ac ± 10% before you make this adjustment.

The +5 V dc regulated output adjustment is located on the Regulator Card (see Figure 7-1). This card is installed in the first card cage slot (left side as viewed from the rear of the terminal).

Connect the positive and negative leads of the multimeter to test points TP +5 REG and TP GND respectively. Set R4 to provide 5.00 ± 0.10 V dc if required.

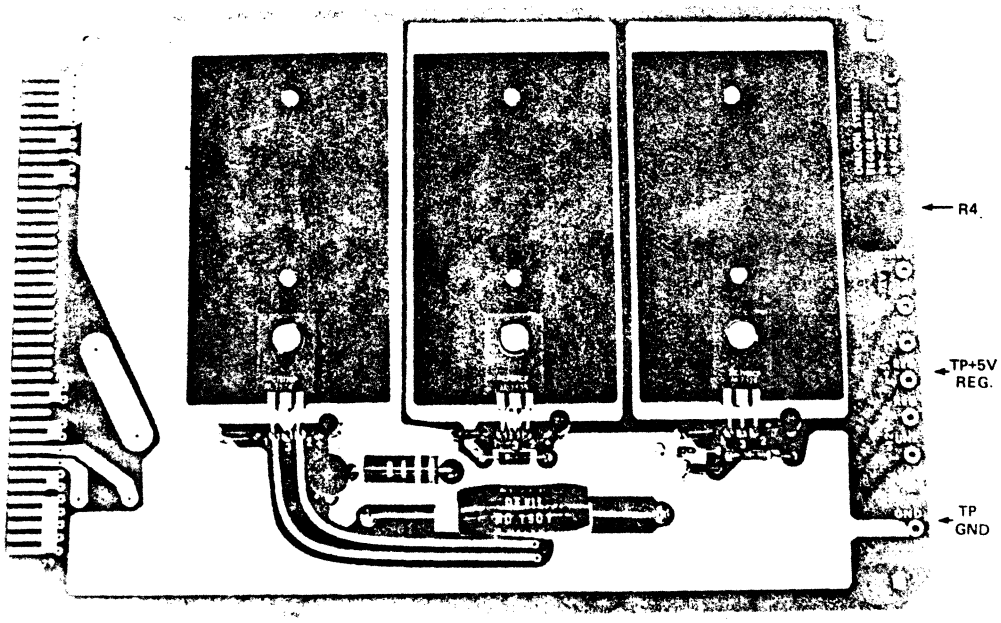


Figure 7-1. Regulator Card: +5 V dc adjustment and test point locations.

7.3 CLICK/BEEP VOLUME

The click/beep volume adjustment is located on the Cursor Control Card (see Figure 7-2). This card is installed in the second slot from the left end (as viewed from the rear of the terminal) of the card cage.

Set R25 for the desired click/beep volume. This adjustment sets the volume for both click and beep.

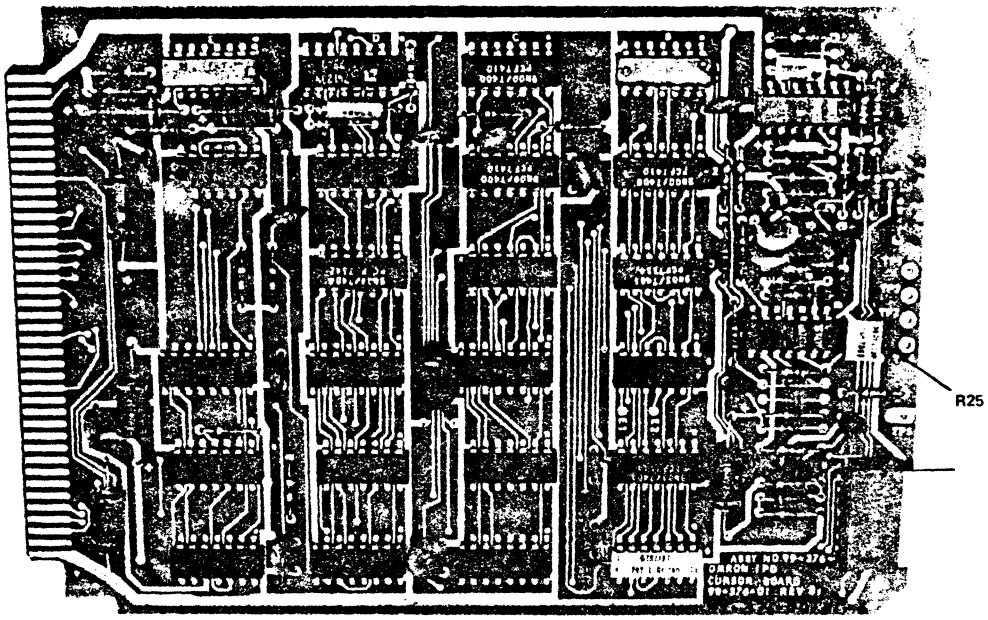


Figure 7-2. Cursor Control Card click/beep volume adjustment location.

7.4 CRT DISPLAY ADJUSTMENTS

NOTE: All display adjustments are made with the terminal operating, the screen filled with data, and the cabinet removed.

WARNING: DANGEROUSLY HIGH VOLTAGES ARE PRESENT IN THE CRT AREA.

7.4.1 Preliminary Procedure

Turn the terminal on and enter characters from the keyboard to fill the screen completely. The pattern shown in Figure 7-3 gives a good picture for making CRT display adjustments.

With an oscilloscope, check that horizontal and vertical sync signals are a nominal +4 volts peak-to-peak. Horizontal sync is available at pin 6, and vertical sync at pin 9, of P112 (the plug connected to the edge connector of the Monitor Deflection Board). Pins 1 and 10 of P112 are at ground.

NOTE: A significantly lower amplitude indicates a possible problem in the Timing Control Card or the Video Card.

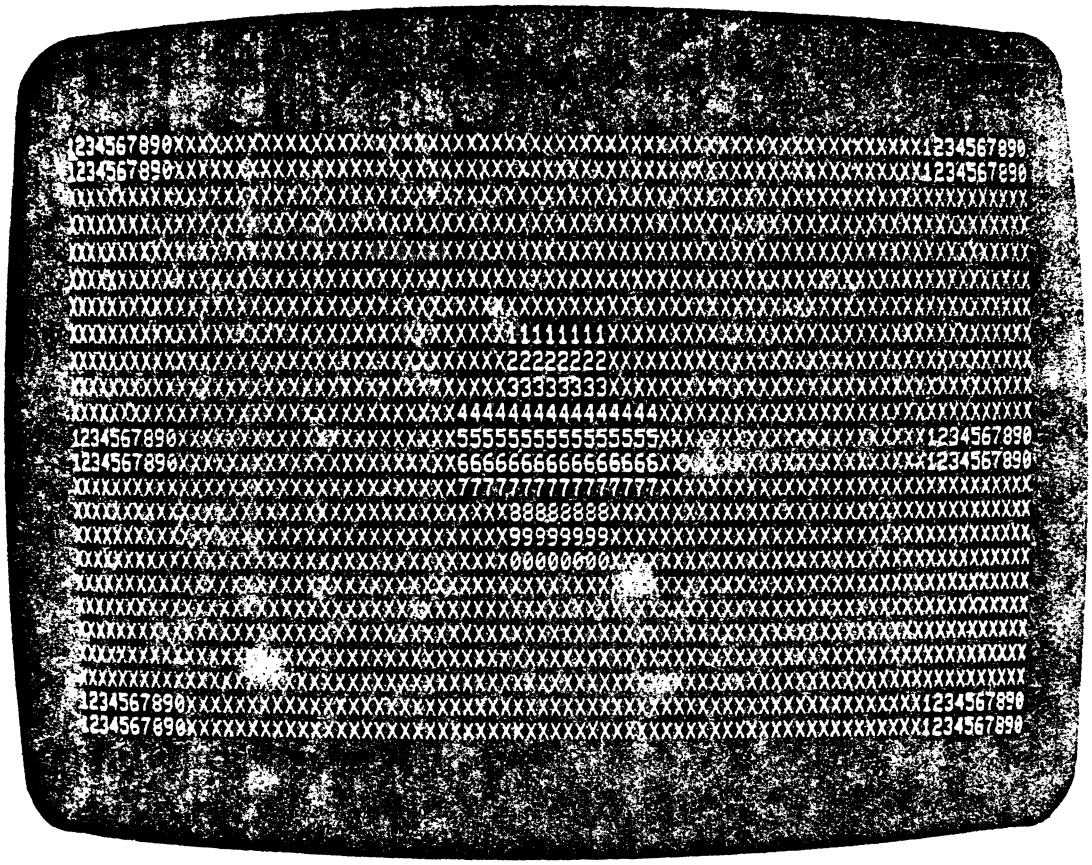


Figure 7-3. Normal 8025 CRT presentation. (24 line display shown)

If required, adjust the BRIGHTNESS control on the keyboard to just "extinguish" the raster. Figure 7-3 illustrates the correct setting. Figures 7-9 and 7-13 show displays for which the BRIGHTNESS control is set too high.

7.4.2 +55 V dc (B+) Adjust

The B+ adjustment (R134) is located on the Monitor Deflection Board (see Figure 7-4).

Connect the positive lead of the multimeter to the cathode of CR106, and the negative lead to the anode of VR101 (see Figure 7-4). Set R134 to provide +55 volts dc.

7.4.3 Video Gain

The video gain adjustment (R119) is located on the Monitor Deflection Board (see Figure 7-4).

Adjust R119 (see Figure 7-4) just enough for maximum contrast between the characters and the black background.

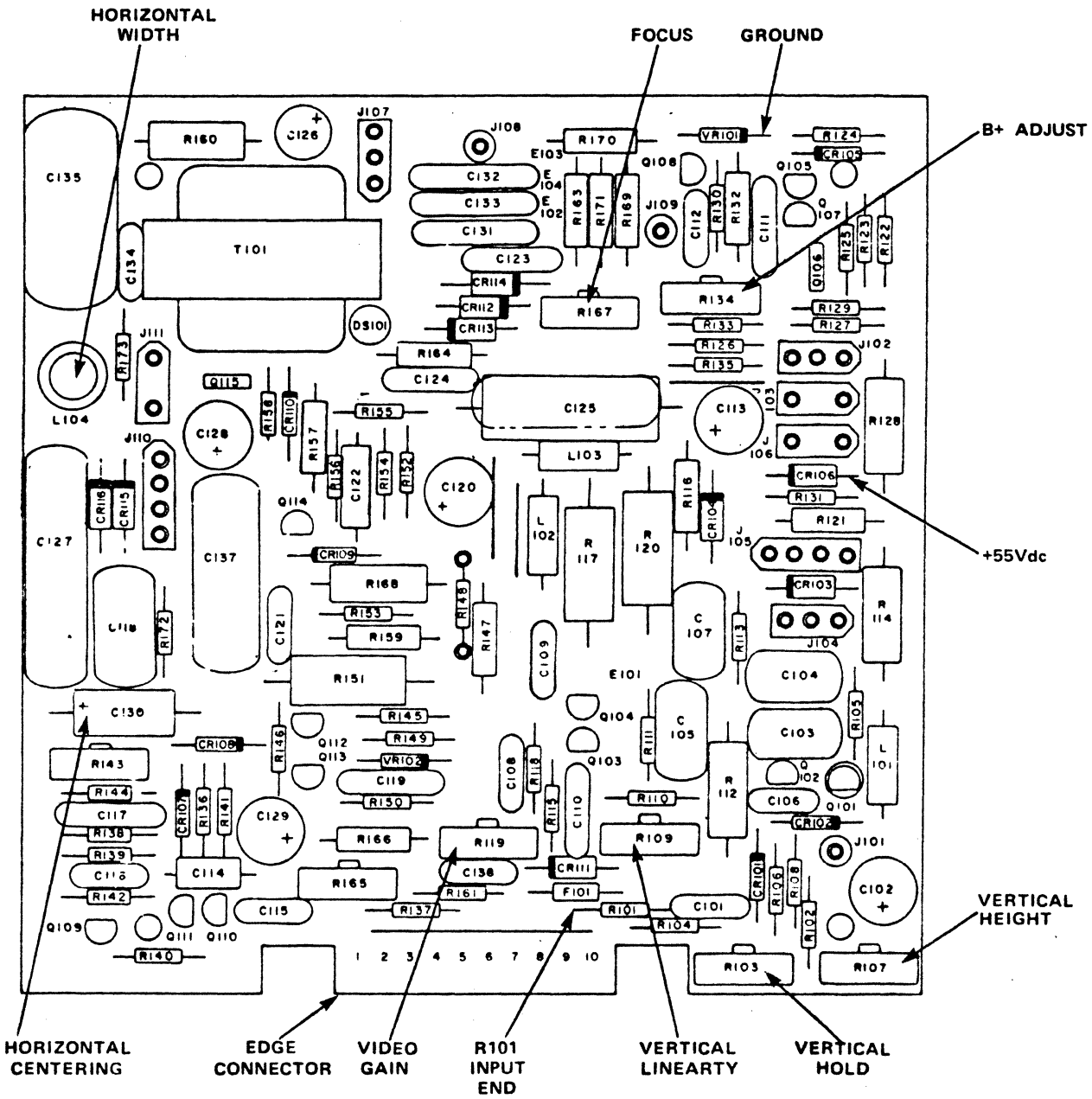


Figure 7-4. Monitor Deflection Card: CRT adjustment and "test point" locations.

7.4.4 Vertical Adjustments

All vertical adjustments are located on the Monitor Deflection Board (see Figure 7-4).

NOTE: The height, vertical hold, and vertical linearity adjustments tend to interact. Changing one may affect the others.

Figures 7-5 through 7-8 show CRT presentations with incorrect settings of the vertical adjustment. Figure 7-3 illustrates a normal display.

1. If the presentation is not centered vertically, refer to paragraph 7.4.6.
2. Set R103 (vertical hold) near the center of its rotation range.
3. Adjust R107 (height) for vertical size indicated in Figure 7-3.
4. Adjust R109 (vertical linearity) for best overall linearity from top to bottom. Use the spaces between character rows as a guide.
5. Short the input end of R101 to ground and set R103 (vertical hold) until the video presentation rolls down slowly.
6. Remove the short used in Step 4.
7. Recheck height and vertical linearity.

7.4.5 Horizontal Adjustments

Except for the horizontal linearity adjustment, all horizontal adjustments are located on the Monitor Deflection Board (see Figure 7-4). You will find the horizontal linearity adjustment sleeve on the neck of the CRT, beneath the deflection yoke.

NOTE #1: No horizontal hold adjustment is used.

NOTE #2: Raster width is a function of both the horizontal width and the linearity adjustments.

NOTE #3: Horizontal centering is a function of both the horizontal (video) centering adjustment described in this paragraph and the raster centering adjustments described in paragraph 7.4.6.

Figures 7-9 and 7-10 show CRT presentations with incorrect horizontal adjustment settings. Figure 7-3 shows a normal display.

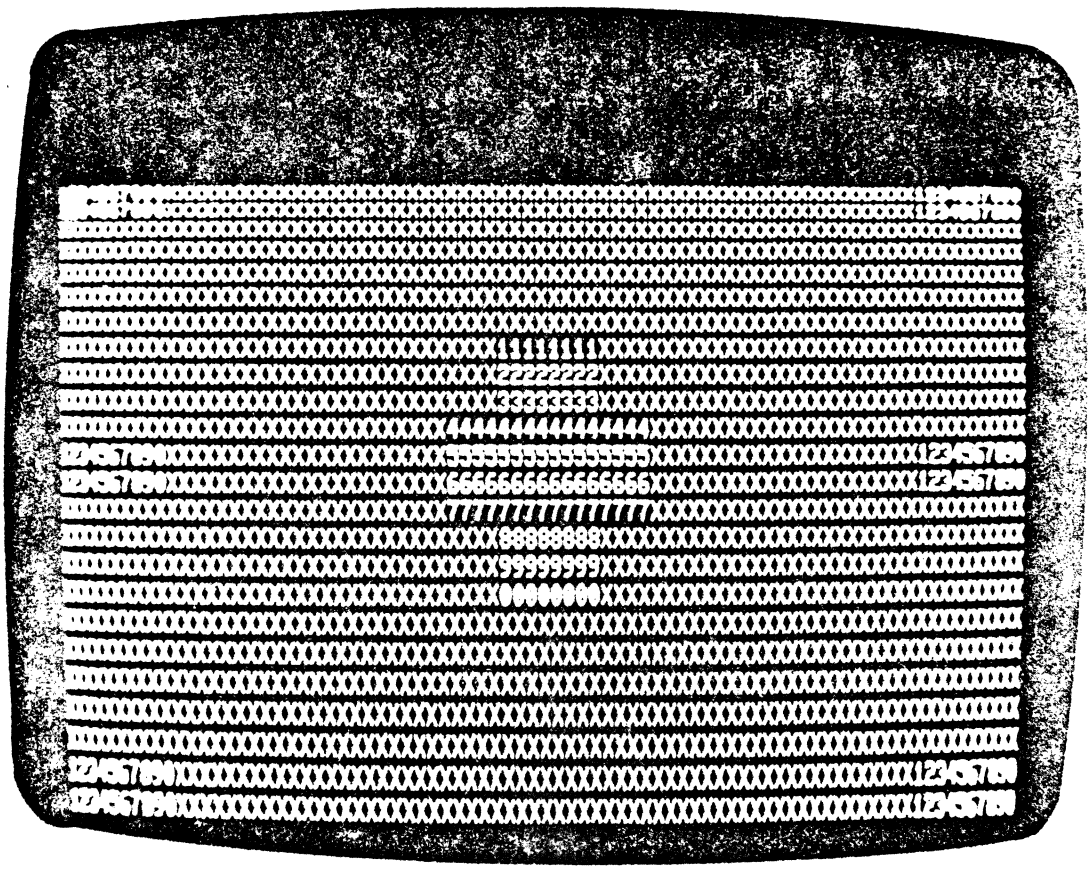


Figure 7-5. Vertical linearity adjustment (R109) incorrectly set.(24 line display shown)

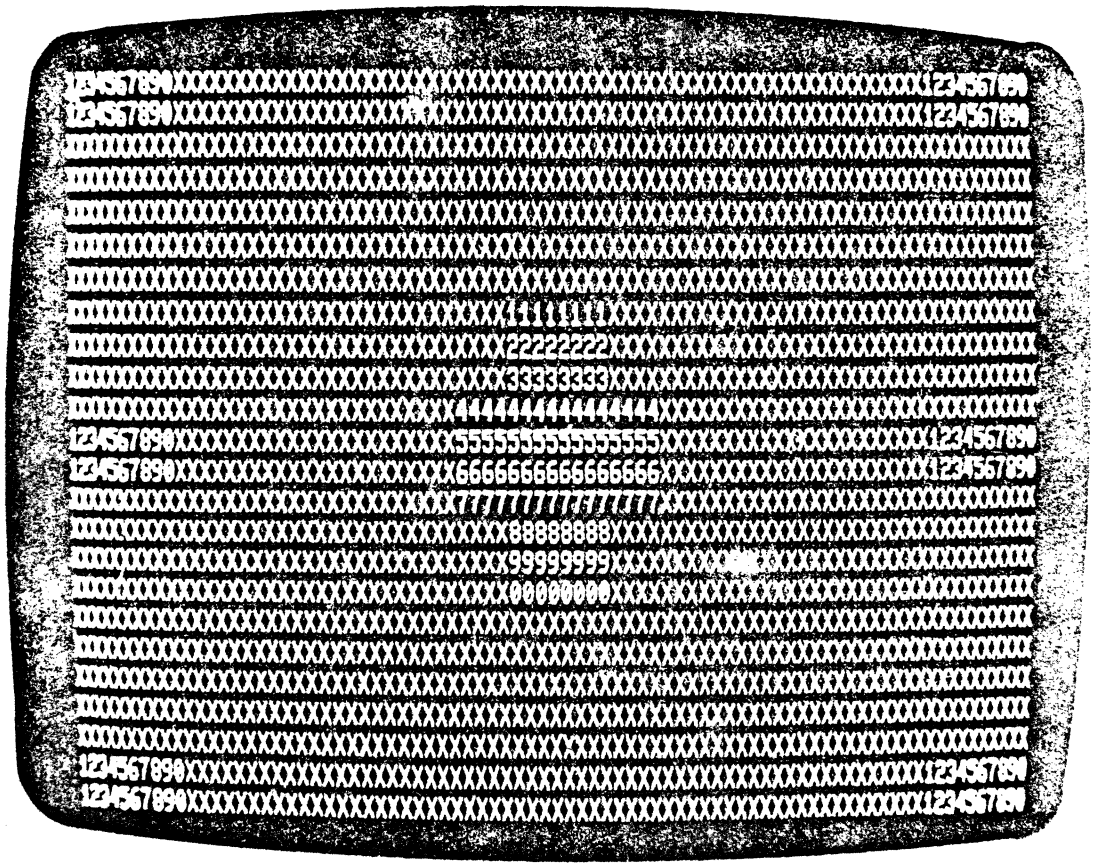


Figure 7-6. Height adjustment (R107) incorrectly set.(24 line display shown)

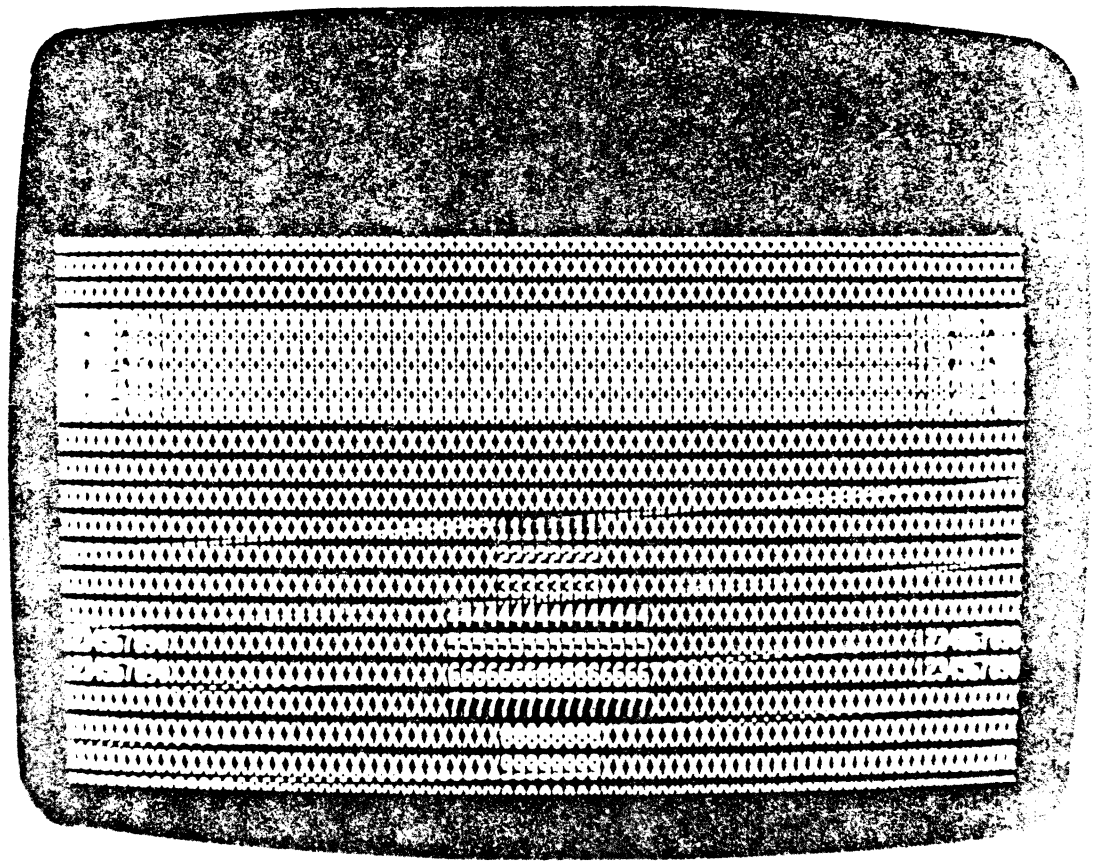


Figure 7-7. Vertical hold adjustment (R103) incorrectly set. (24 line display shown)

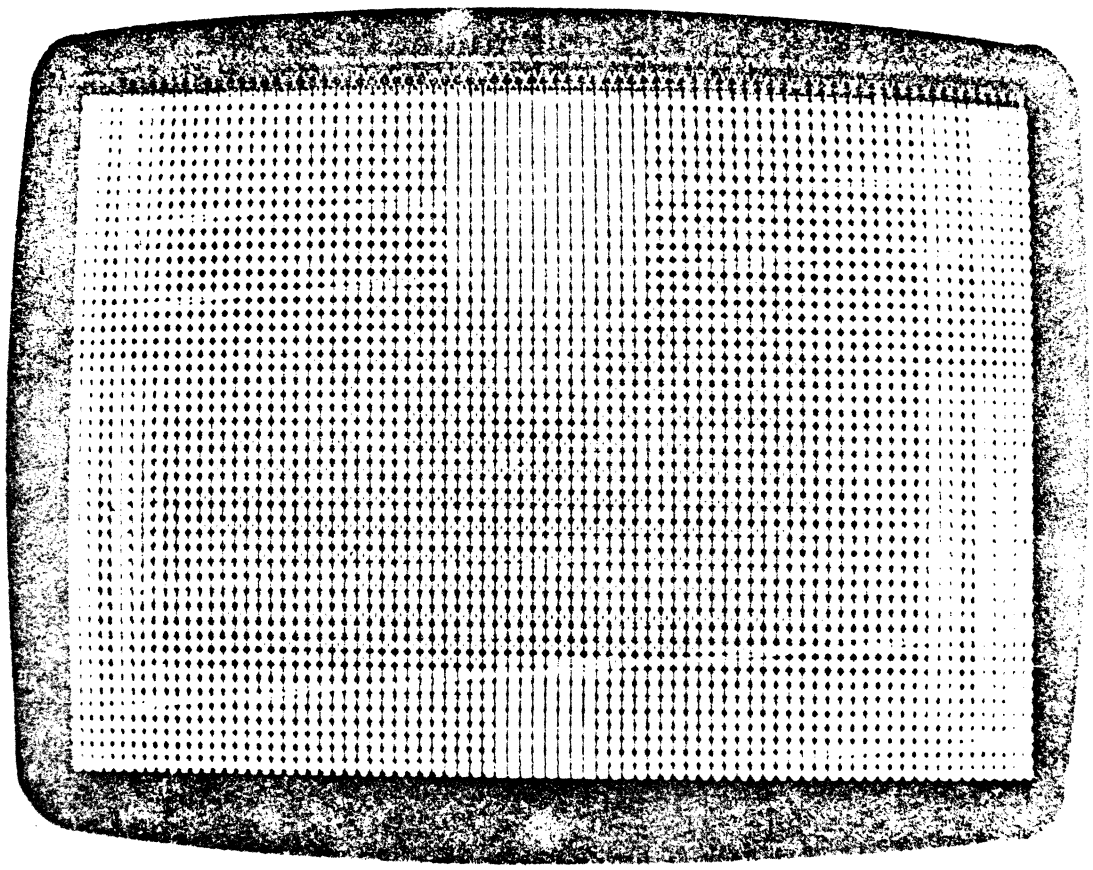


Figure 7-8. Vertical hold adjustment (R103) incorrectly set. (24 line display shown)

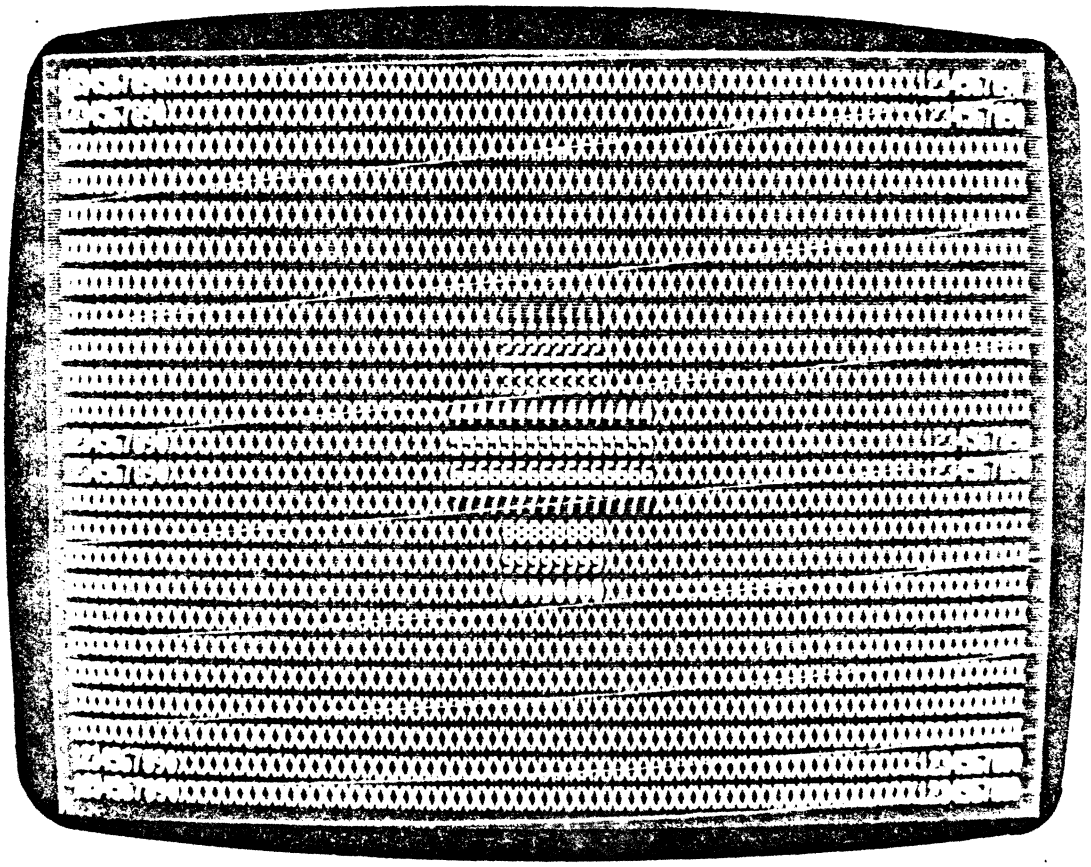


Figure 7-9. Horizontal width adjustment (L104) incorrectly set. Brightness control too high. (24 line display shown)

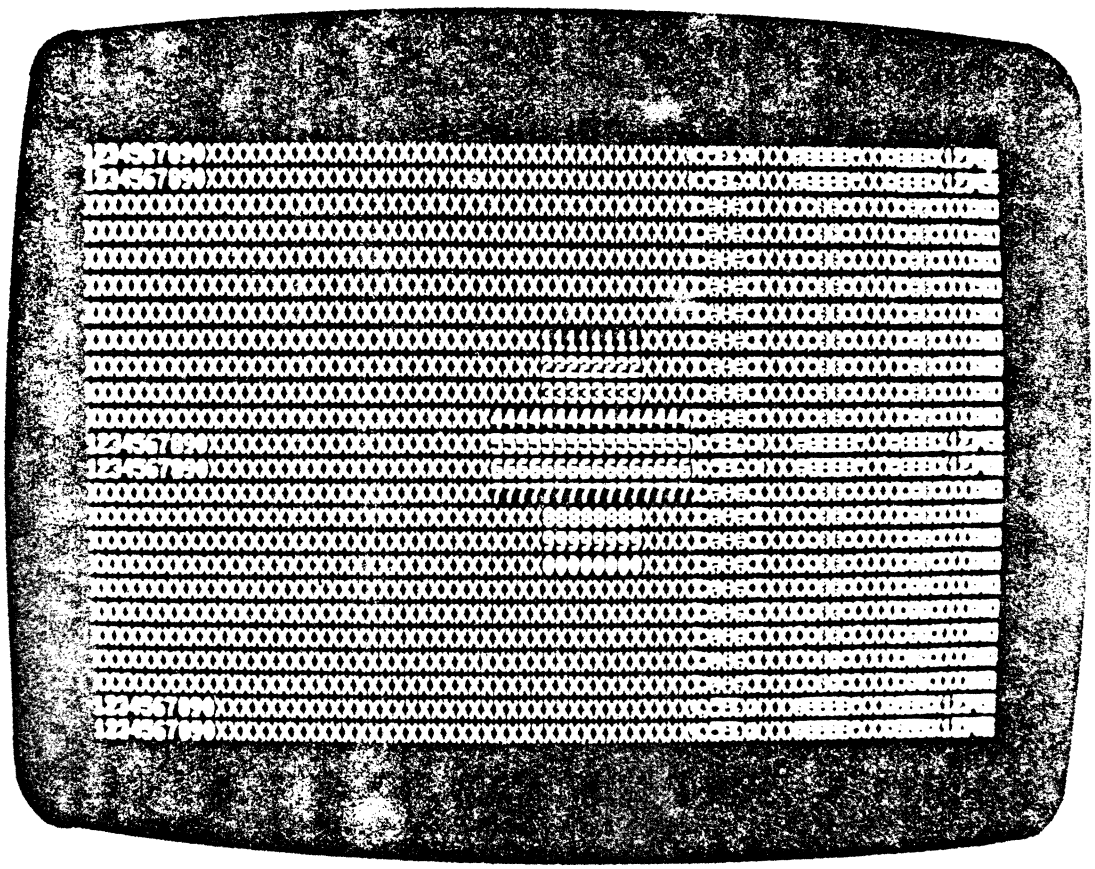


Figure 7-10. Severe misadjustment of horizontal centering adjustment (R143). Note foldover on right side. (24 line display shown)

1. Insert the horizontal linearity sleeve (see Figure 7-11) about one-third of its length under the deflection yoke.

2. Adjust L104 (width) for the horizontal size indicated in Figure 7-3.

3. Slide the linearity sleeve further under the yoke to get the best overall linearity from left to right. Use character widths as a guide. Do not use this adjustment to set horizontal width. It is to be used only to optimize linearity.

CAUTION: INSERTING THE LINEARITY SLEEVE FURTHER THAN NECESSARY CAN DAMAGE THE HORIZONTAL OUTPUT CIRCUIT.

4. Readjust L104 for correct horizontal size.

5. Make fine adjustments of the linearity sleeve and L104, if required, for optimum linearity and width (refer to Figure 7-3).

6. If the presentation is not centered horizontally as shown in Figure 7-12, turn the BRIGHTNESS control up until the raster is visible (see Figure 7-13).

7. If the video is not centered horizontally within the raster, center the video with R143 (horizontal centering).

8. If the raster is not centered horizontally, refer to paragraph 7.4.6.

7.4.6 Centering Adjustments

Two ring magnets mounted on the neck of the CRT (see Figure 7-14) position the raster on the CRT face. Rotate the centering magnets to center the raster vertically and horizontally. Correct raster placement positions the video as shown in Figure 7-3.

7.4.7 Yoke Adjustments

If the presentation is tilted (see Figure 7-15), the deflection yoke is not positioned correctly on the neck of the CRT. Loosen the yoke-mounting screw (see Figure 7-14) and rotate the yoke so that the presentation appears as shown in Figure 7-3.

7.4.8 Focus

Adjust R167 (focus) to obtain the sharpest overall presentation possible. Use characters in the corners and center of the display as a guide. Figure 7-3 shows a presentation with correct focus.

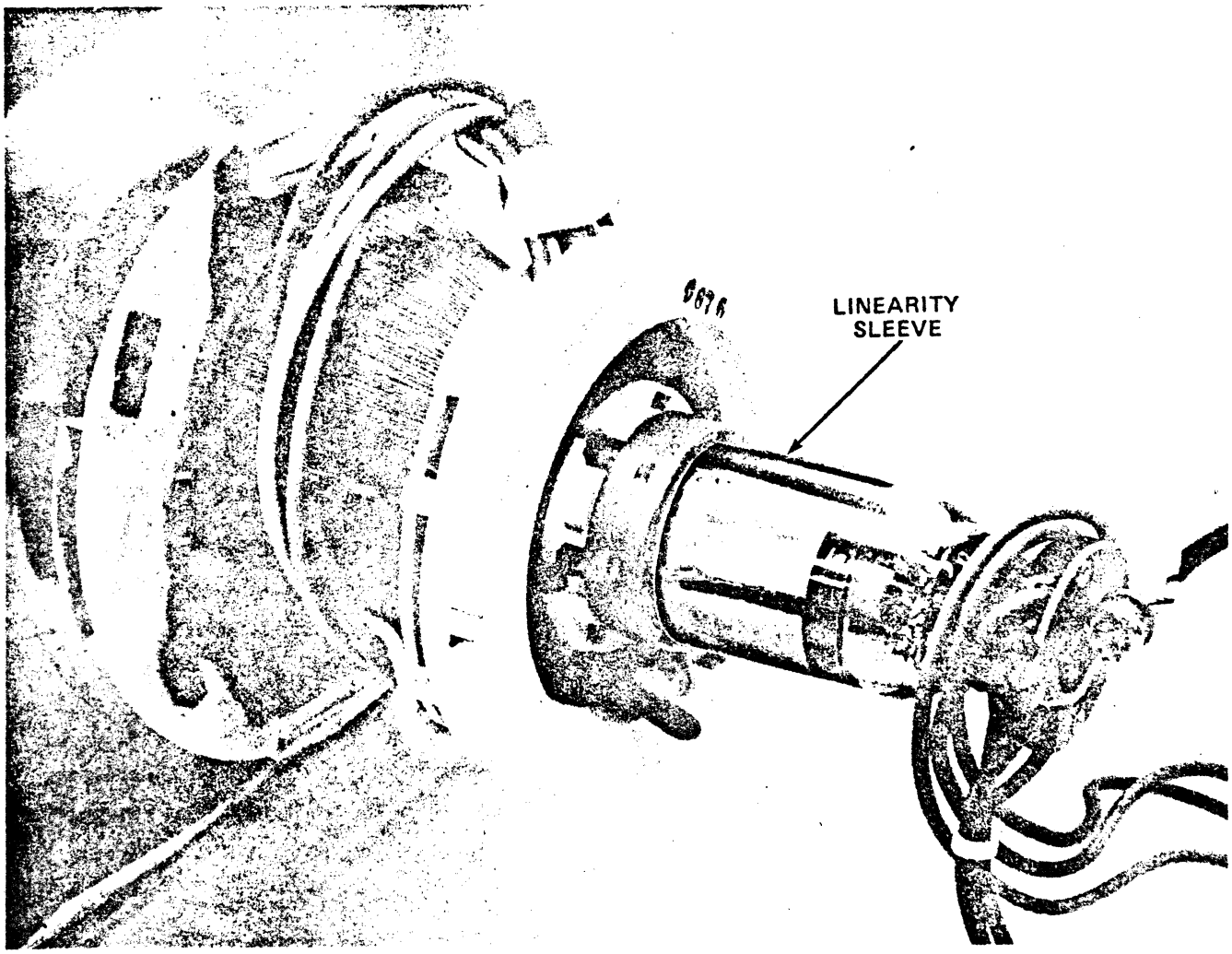


Figure 7-11. Horizontal linearity is positioned on neck of CRT for best overall linearity from left to right.

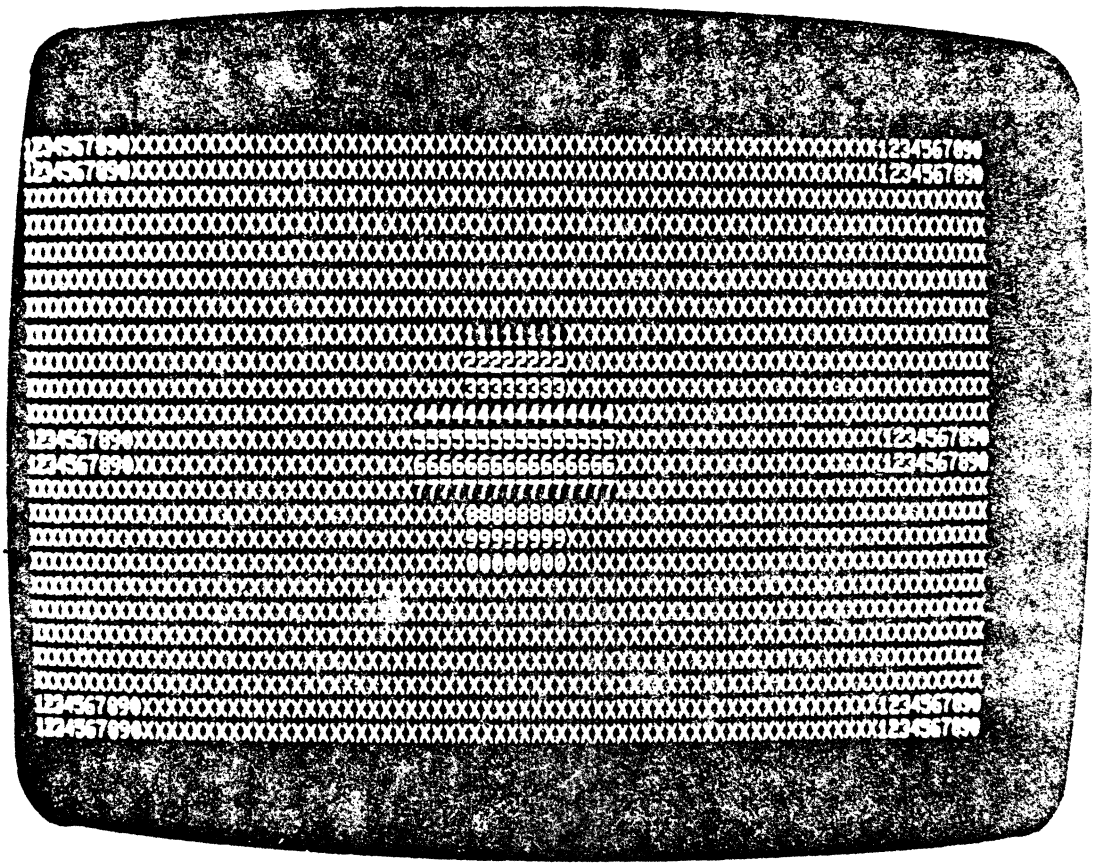


Figure 7-12. Example of a horizontal centering problem caused by incorrect setting of the horizontal centering adjustment (R143) or of the raster centering magnet discussed in paragraph 7.4.6. (24 line display shown)

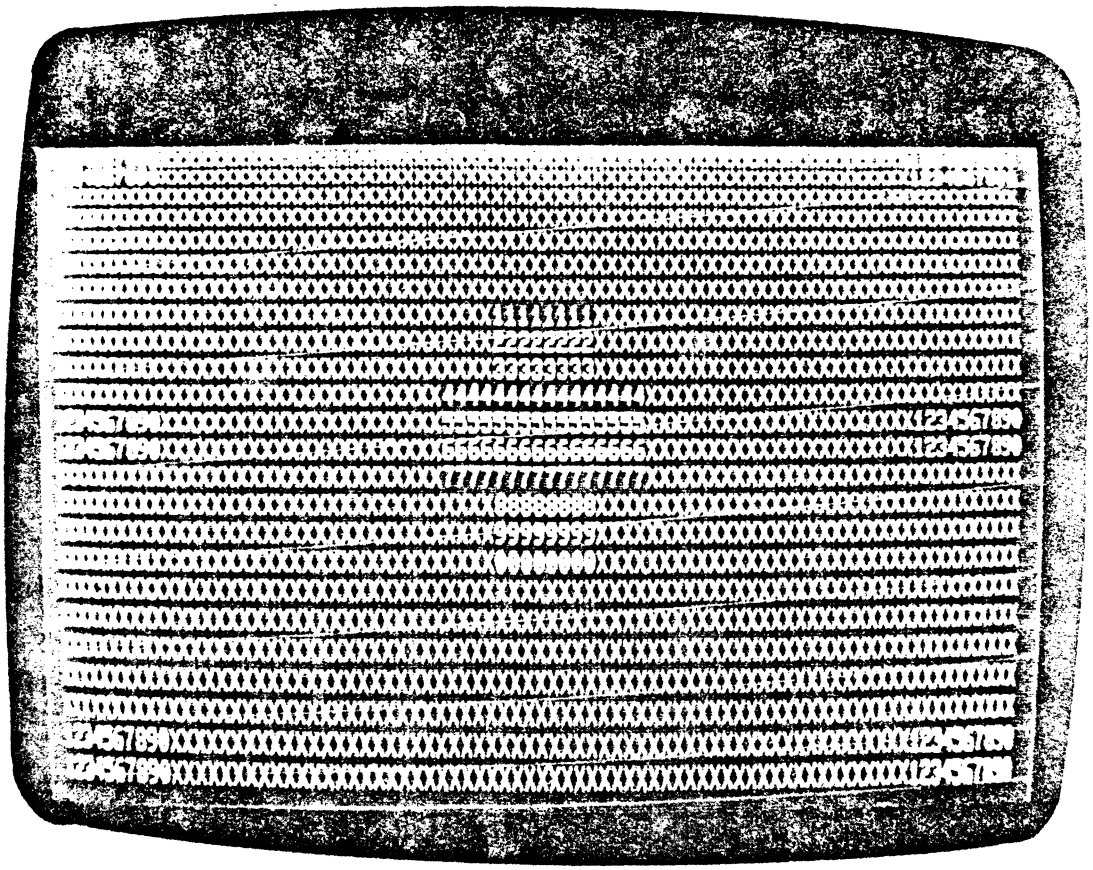


Figure 7-13. To determine which centering adjustment is incorrectly set, turn the control up until the raster is visible. The photo illustrates the correct setting of the horizontal (video) centering adjustment (R143) and the raster centering magnets. Note that the vertical linearity adjustment (R109) is incorrectly set. (24 line display shown)

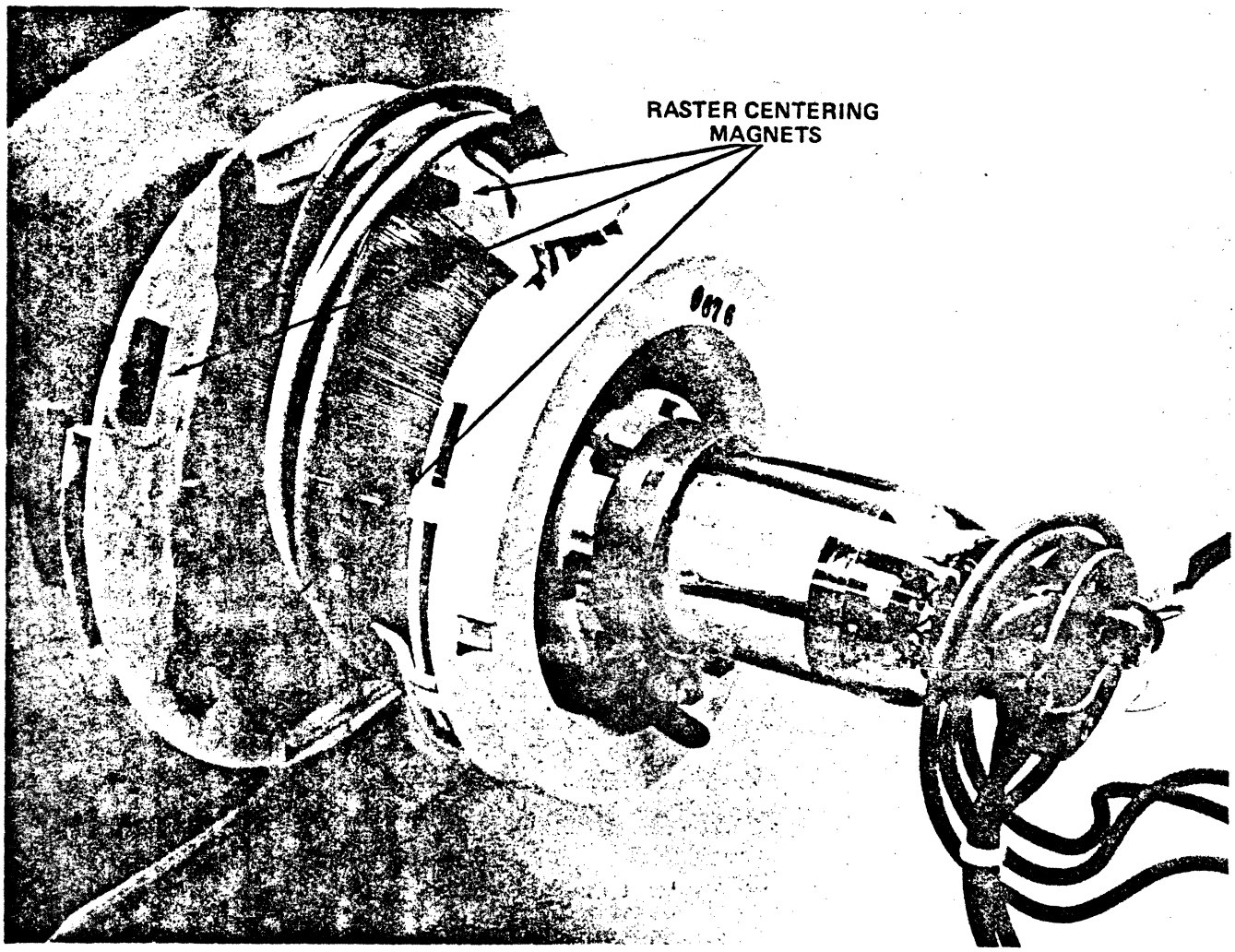


Figure 7-14. Raster centering magnets are used to center the raster vertically and horizontally on the CRT screen. The deflection yoke is used to correct raster tilt.

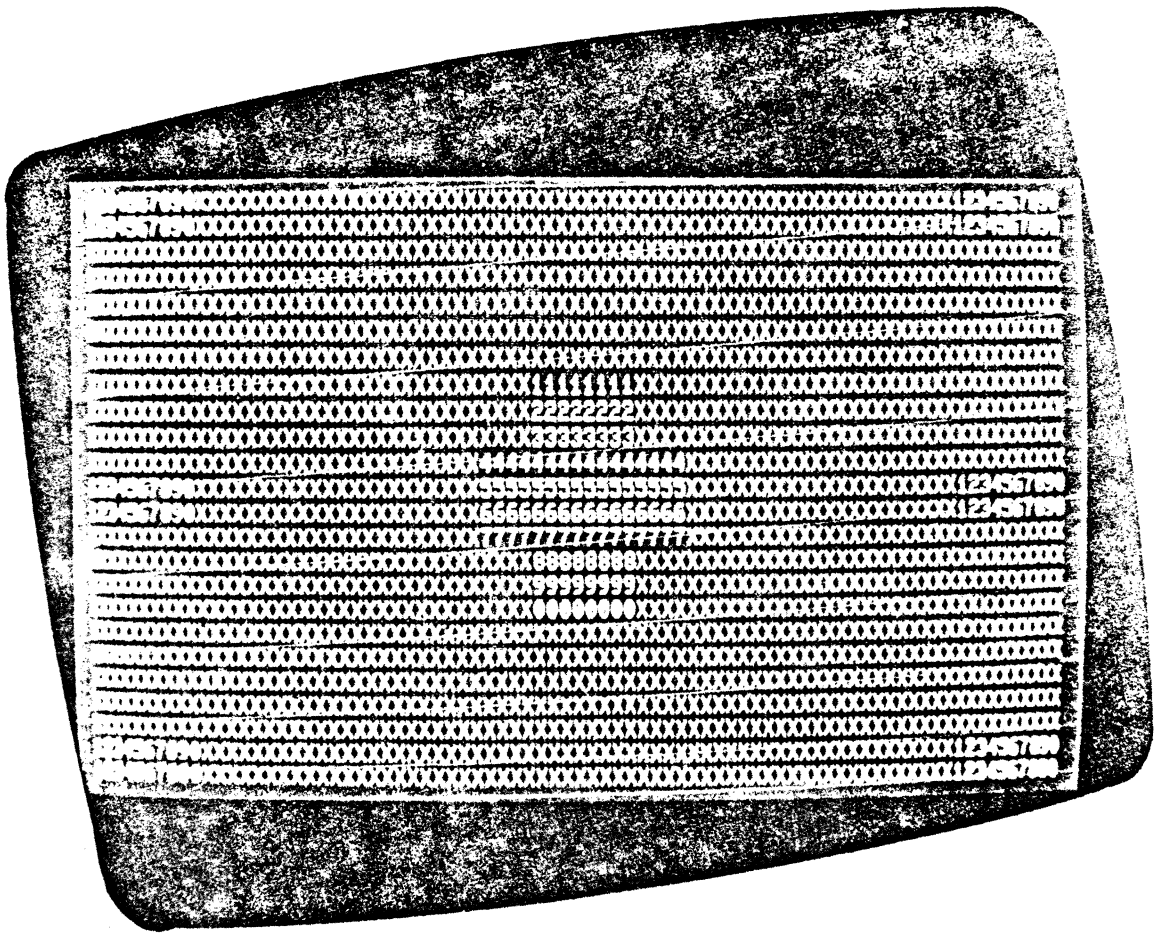
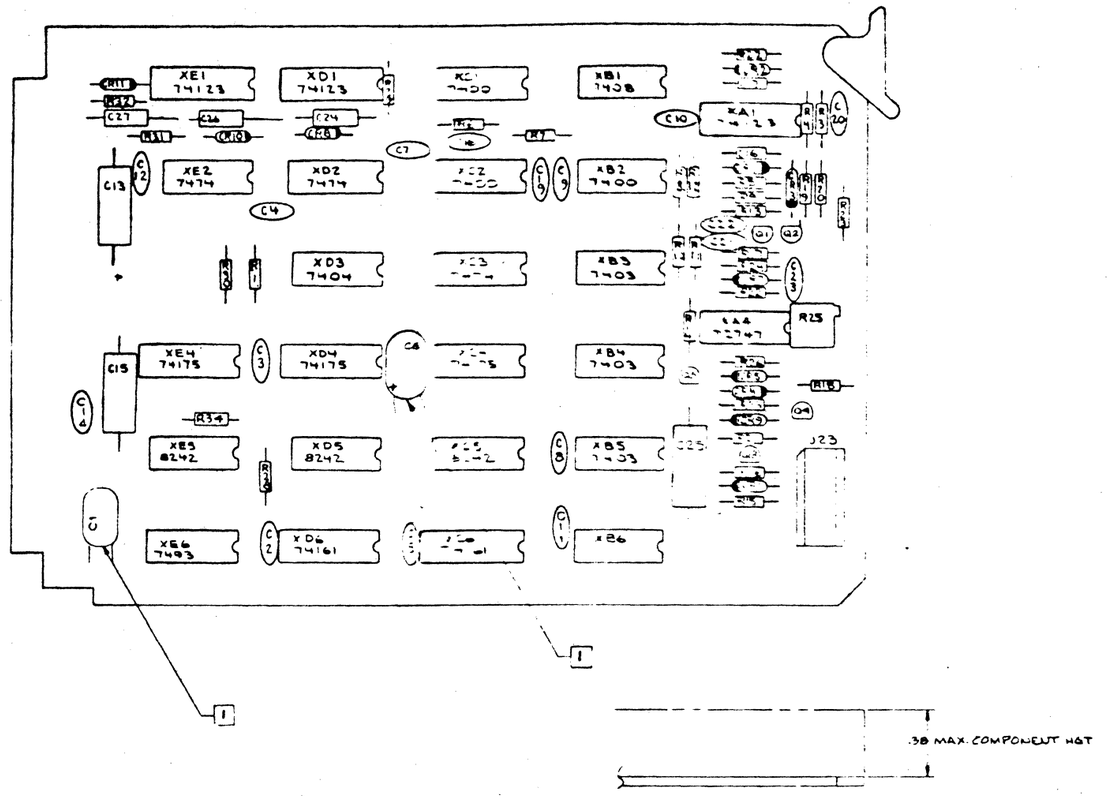


Figure 7-15. Deflection yoke incorrectly set.
(24 line display shown)

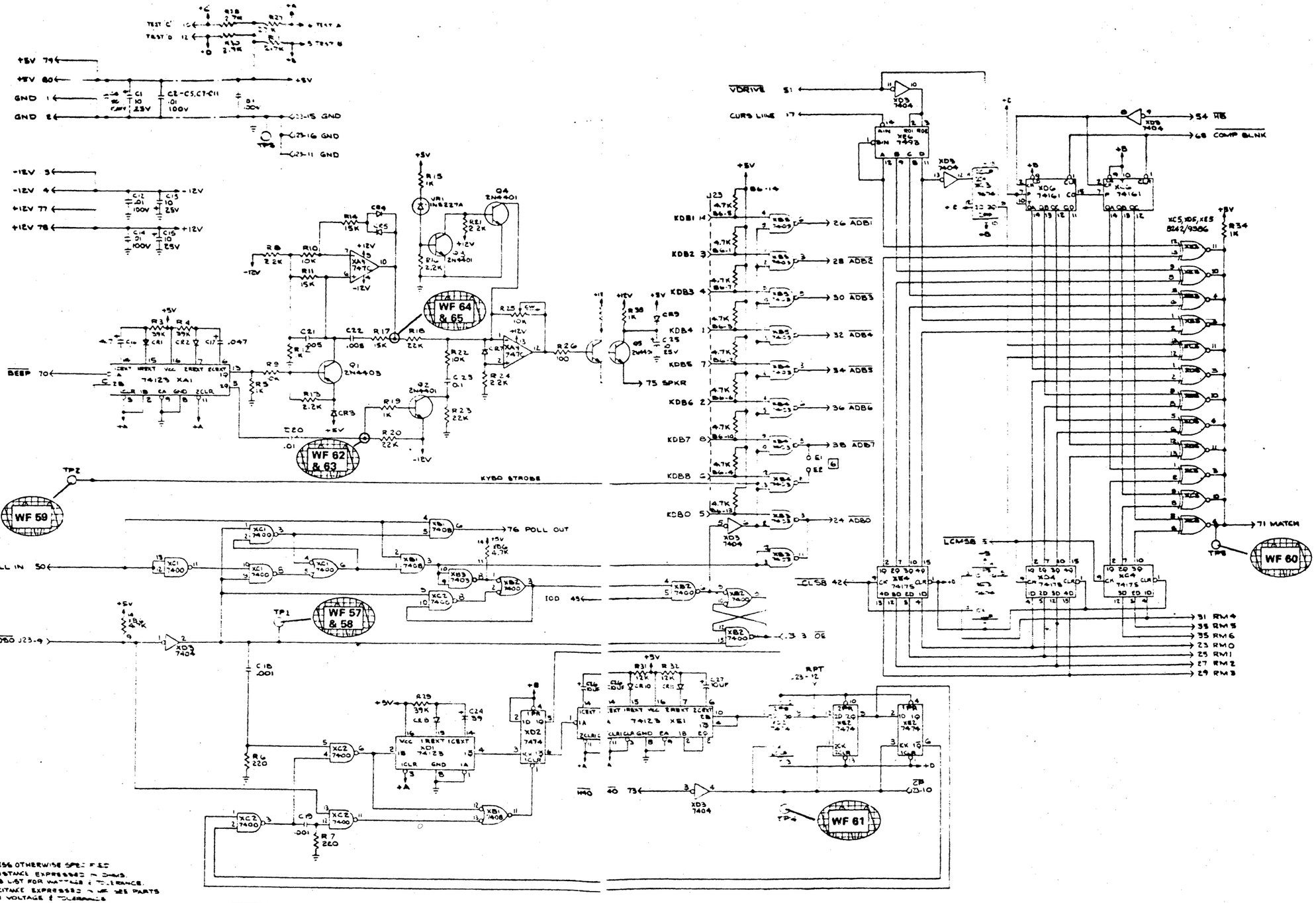
DRAWINGS



NOTES: UNLESS OTHERWISE SPECIFIED.

[1] C1 & C6 ARE ALLOWED TO BE .410 MAX. HEIGHT.

TITLE	PWB ASSY, CURSOR CONTROL	
DWG NO	99-376-01	REV C



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE EXPRESSED IN OHMS. SEE PARTS LIST FOR WATTAGE & TOLERANCE.
2. ALL CAPACITANCE EXPRESSED IN MFD. SEE PARTS LIST FOR VOLTAGE & TOLERANCE.
3. ALL DIODES ARE 1N914
4. SPARE GATES: 7408 XB1-9,10,13 7403 XB3,1-4,5,6
5. ABBREVIATIONS: NON STD
   CO - CARRY OUTPUT
   LO - LOAD
6. OPTION PCB - ADD JUMPER E TO E2. THIS OPTION ADDS BIT 5 (+5V) TO THE IC KEY AND KEYBOARD SWITCHES S8 THRU S11 WHEN DEPRESSED. THIS NOTE APPLIES FOR KEYBOARD ENCODER MM5740OD ONLY.

(WF) IS USED TO IDENTIFY THE PROPER WAVEFORM FOR SPECIFIC, CRITICAL CIRCUIT POINTS. ALL WAVEFORMS WITH CORRESPONDING IDENTIFICATION NUMBERS ARE LISTED IN SECTION 6, TROUBLESHOOTING, OF THIS MANUAL.
--* INDICATES OTHER CIRCUIT POINTS WHERE THE SAME WAVEFORM SHOULD APPEAR.

REF DESIG NO	DEV NO	GND	Vcc
XB7 XC1 XC2	7400	7	14
XD3	7404	7	14
XB1	7408	7	14
XD2 XE2 XC3	7474	7	14
XE6	7493	10	5
XC6 XD6	74161/3716	8	16
XC4 XD4 XE4	74175	8	16
XA1 XD1 XE1	74123	8	16
XB3 XB4 XB5	7403	7	14
XC5 XD5 XE5	8242/9306	7	14
XA4	7477C		
XB6	MES PACK	—	14

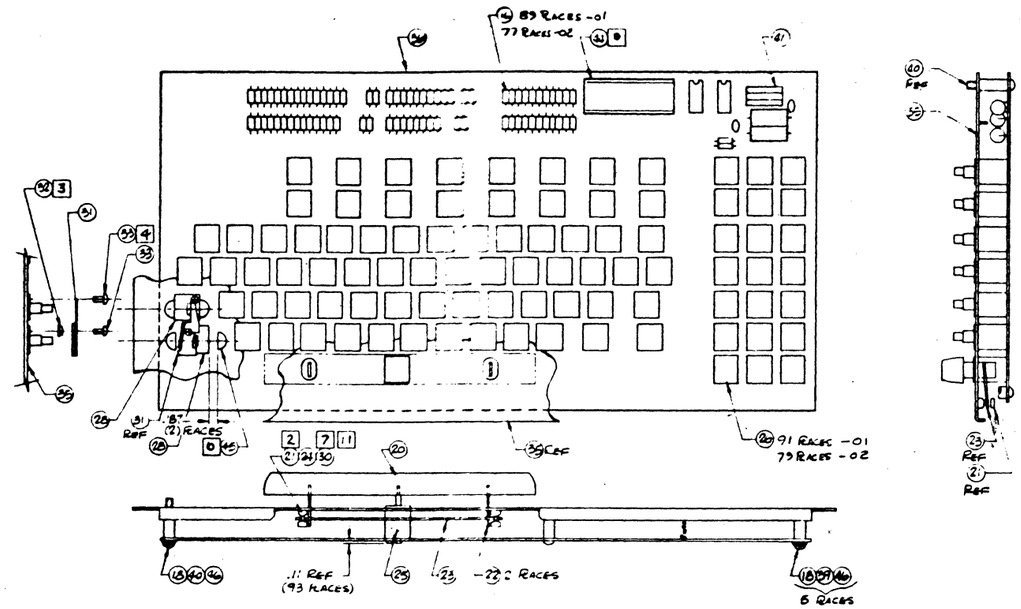
REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C27	
CR11	CR6
R34	R2
TP5	
XA4	XA2, XA3, XA5, XA6
XB6	
XC6	
XD6	
XE6	XE3
VR1	

TEST POINTS:
TP1 - CSO
TP2 - +5V SD STROBE
TP3 - MATCH
TP4 - HMS
TP5 - GND

8-1

TITLE	
SCHEMATIC DIAG. CURSOR CONTROL	
DWG NO 96-376-01	REV B

DRAWINGS



NOTES: UNLESS OTHERWISE SPECIFIED

1) ITEM No. 32 (KEYBOARD PANEL) MUST BE ATTACHED TO THE BOARD BEFORE THE SWITCHES, ITEM 25, ARE INSTALLED.

3 INSTALL ITEM 21 PRIOR TO INSTALLATION OF ITEM 35

4 APPLY LUBRICANT (ITEM 14) ON BEARING.

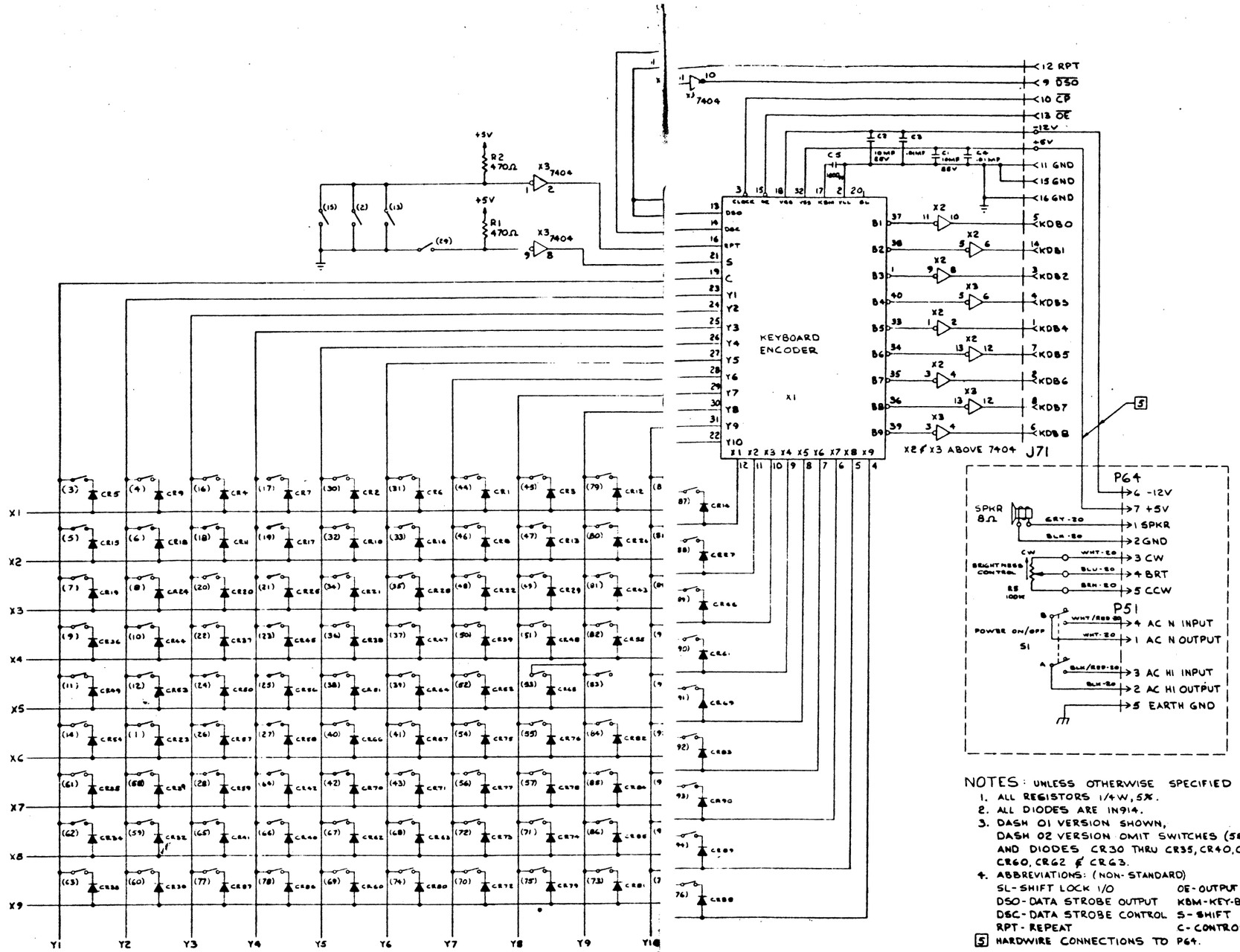
5 AFTER INSTALLATION OF SHIFT LOCK LEVER, INSTALL ADJUSTING SCREW TO LIMIT THE VERTICAL MOVEMENT OF THE LEVER.

6 CUT ITEM 45 IN HALF AND LOCTITE AS SHOWN

7 APPLY LOCTITE TO THREAD

8 INSTALL ITEM 1 (CK ITEM 2) AS REQUIRED ADJUST PIVOT (ITEM 8.) IN PARALLEL FASHION AGAINST RUNNERS (ITEM 22) AND EACH OFF PIVOT .010 TO .015 THE SPACE BALANCE SHALL OPERATE WITH SLIGHT LOOSENESS WITH JAMMING

TITLE	PWB KEYBOARD ASSEMBLY	
DWG NO	99-453-XX	REV A

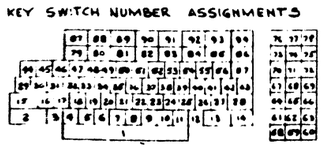


REF. DESIG. NO.	DEV. NO.	GND	VCC	VGG
X2,X3	7404	7	14	
X1	MM5740	8	32	18

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
CR90	CR68
C9	
R2	
(94)	

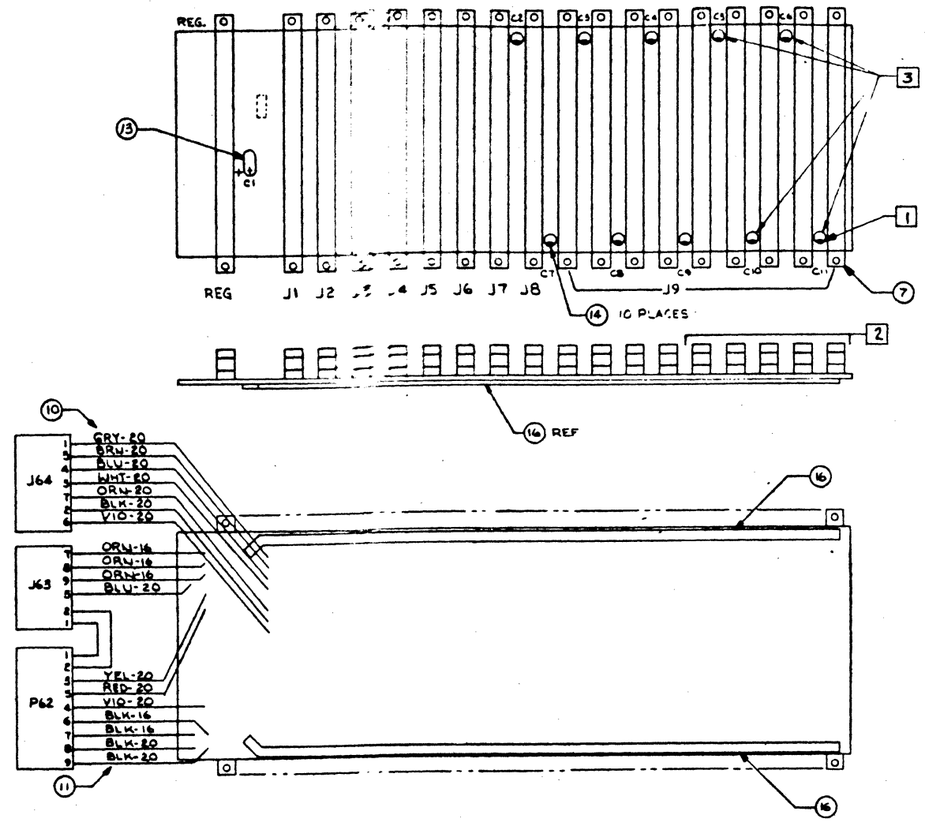
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL REGISTORS 1/4W, 5%.
2. ALL DIODES ARE IN914.
3. DASH 01 VERSION SHOWN, DASH 02 VERSION OMIT SWITCHES (58) THRU(69) AND DIODES CR30 THRU CR35, CR40, CR41, CR42, CR60, CR62 & CR63.
4. ABBREVIATIONS: (NON-STANDARD)
   SL-SHIFT LOCK I/O — OE-OUTPUT ENABLE
   DSO-DATA STROBE OUTPUT — KBM-KEY-BOUNCE MASK
   DSC-DATA STROBE CONTROL — S-SHIFT
   RPT-REPEAT — C-CONTROL
5. HARDWIRE CONNECTIONS TO P64.

KEY SWITCH NUMBER ASSIGNMENTS



TITLE	SCHEMATIC DIAGRAM KEYBOARD
DWG NO	96-453-XX
REV	A

DRAWINGS



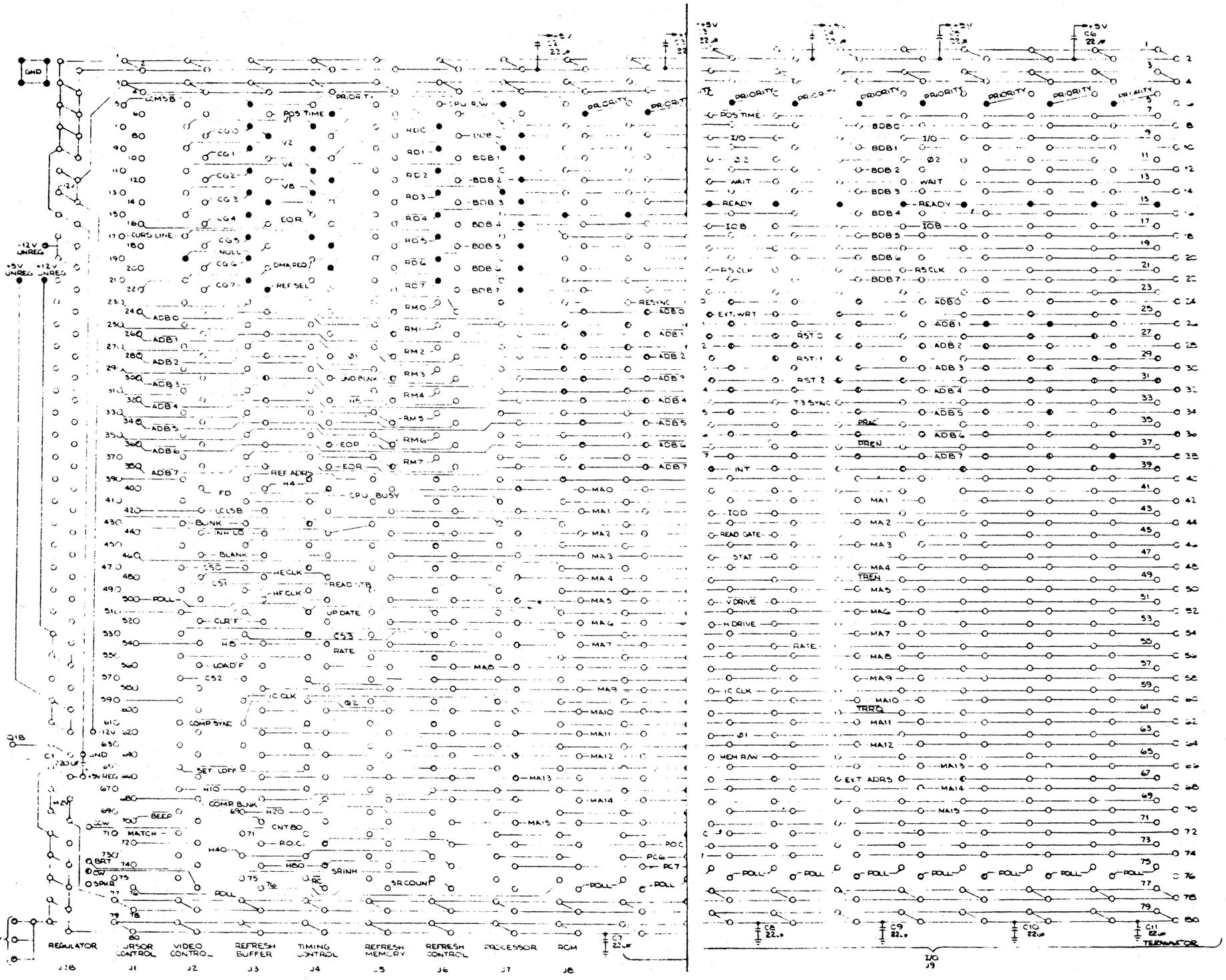
NOTES: UNLESS OTHERWISE SPECIFIED

[1] ⊕ DENOTES + (PLUS) SIDE OF CAPACITOR

[2] DASH 01 AS SHOWN OMIT CONN. INDICATED ON DASH 02 VERSION ONLY

[3] DASH 01 AS SHOWN, OMIT C5,C6,C10,C11 ON DASH 02 VERSION ONLY

TITLE	PWB ASSY, MOTHER BOARD
DWG NO 99-414-XX	REV B

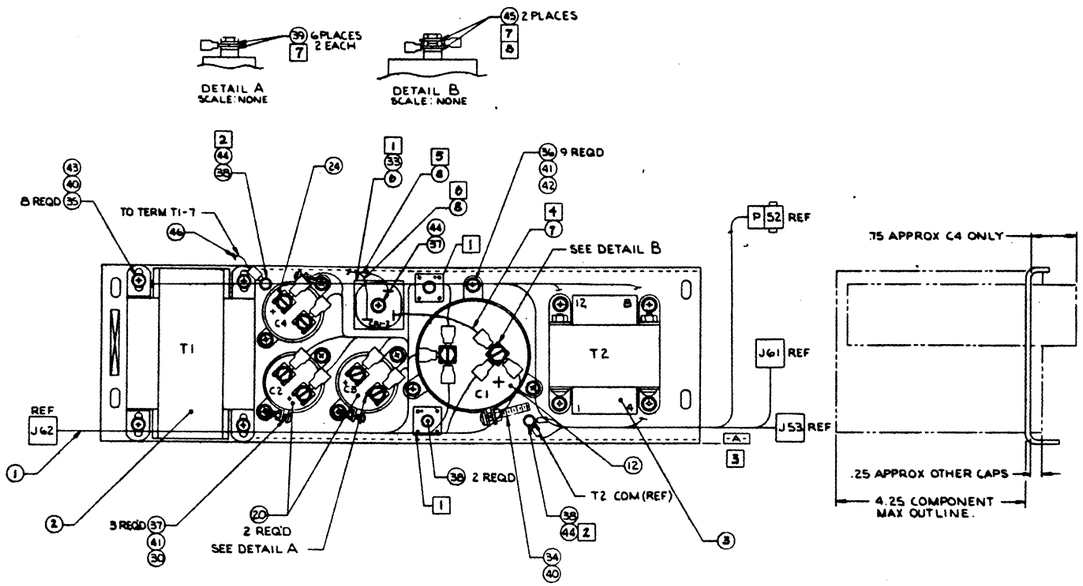


NOTES: UNLES OTHERWISE SPECIFIED.
1. ● SOURCES

TITLE	MOTHER BOARD CRT TERMINAL SCHEMATIC DIAGRAM
DWG NO	96-914-01
REV	B

CONFIGURATION A

(CONFIGURATION B ON FOLLOWING PAGE)



NOTES: UNLESS OTHERWISE SPECIFIED

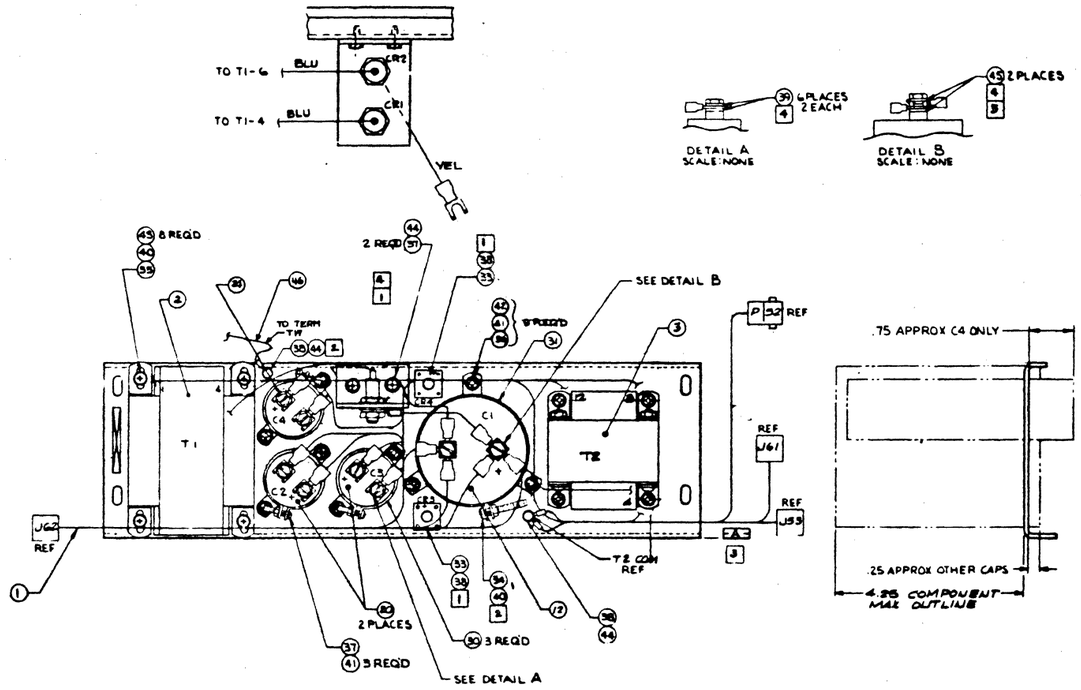
1. APPLY THERMAL COMPOUND (ITEM 33) BETWEEN RECTIFIED AND CHASSIS (ITEM 1)
2. ASSEMBLE WITH LOCKWASHER (ITEM 44) AGAINST THE CHASSIS.
3. COMPONENTS AND/OR WIRES NOT TO EXCEED SURFACE A.
4. WIRE AS SHOWN FROM POS TERMINAL OF CR1-2 TO POS TERMINAL OF C1.
5. WIRE FROM BRIDGE AS SHOWN TO T1 TERM 4.
6. WIRE FROM BRIDGE AS SHOWN TO T1 TERM 6.
7. ASSEMBLY WITH TERMINAL(S) BETWEEN THE TWO LOCK-WASHERS WITH TOES UP.
8. USE ITEM 45, INT. TOOTH LOCK-WASHERS WHEN NOT SUPPLIED WITH ITEM 12 (C1).

(INTERCHANGEABLE WITH 07-041-01)

TITLE	
POWER SUPPLY ASSEMBLY	
DWG NO 07-041-02	REV A

DRAWINGS

CONFIGURATION B

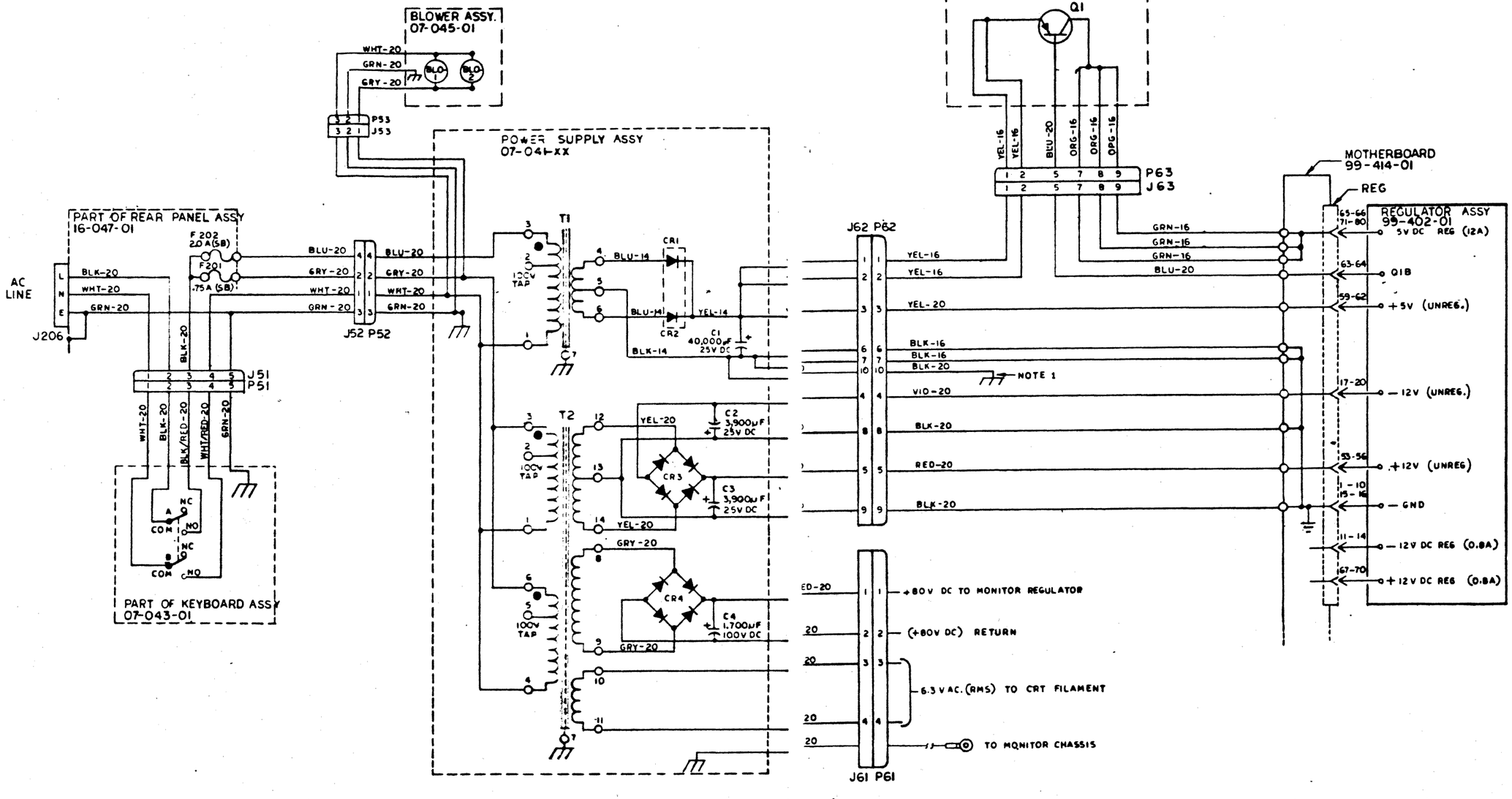


NOTES : UNLESS OTHERWISE SPECIFIED

1. APPLY THERMAL COMPOUND (ITEM 33) TO CR3, CR4, (ITEM 2) AND CHASSIS (ITEM 1)
2. ASSEMBLE WITH LOCKWASHER (ITEM 44) AGAINST THE CHASSIS.
3. COMPONENTS AND/OR WIRES NOT TO EXCEED SURFACE A.
4. ASSEMBLE WITH THE TERMINAL (8) BETWEEN THE LOCKWASHERS WITH TOES UP.
5. USE ITEM 45, WHEN NOT SUPPLIED WITH C1 (ITEM 12).

(INTERCHANGEABLE WITH 07-041-02, SAME SCHEMATIC)

TITLE	POWER SUPPLY ASSEMBLY •
DWG NO	REV

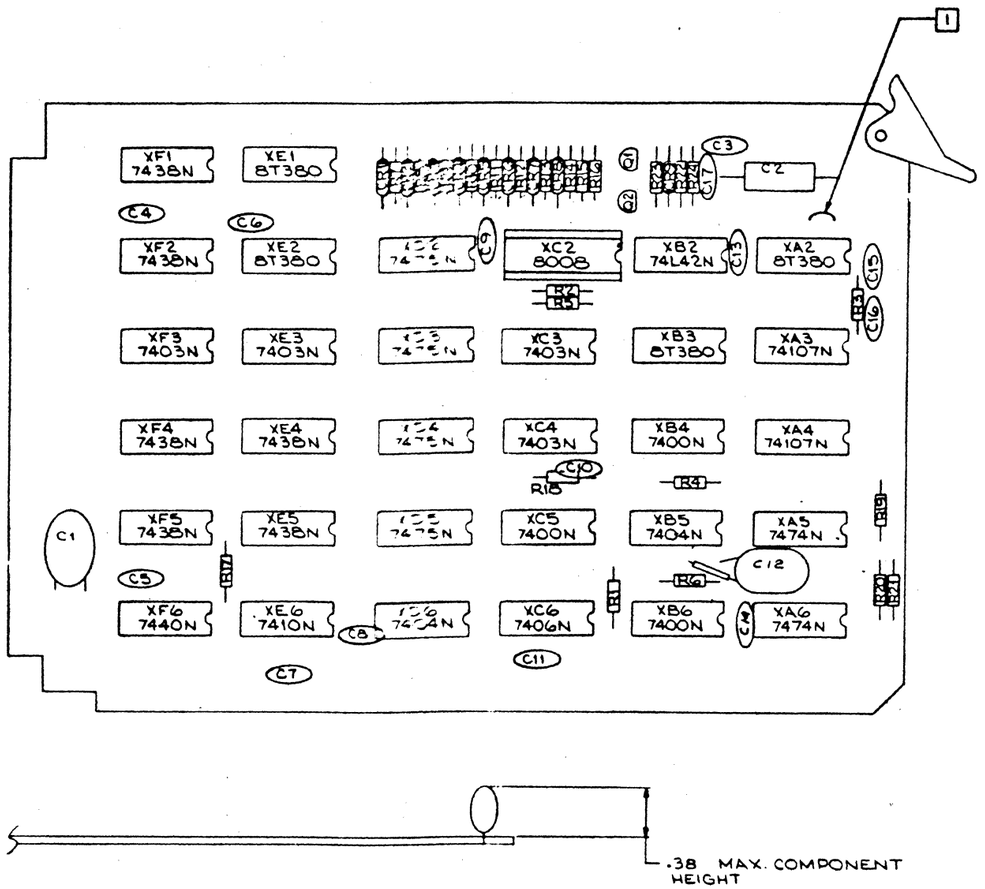


NOTES:

1. WHEN ISOLATION BETWEEN SIGNAL GROUND AND CHASSIS IS REQUIRED, GROUND LEAD IS TO BE CUT AT THIS LOCATION.

TITLE	SCHEMATIC DIAGRAM POWER SUPPLY
DWG NO 95-145-01	REV B

DRAWINGS

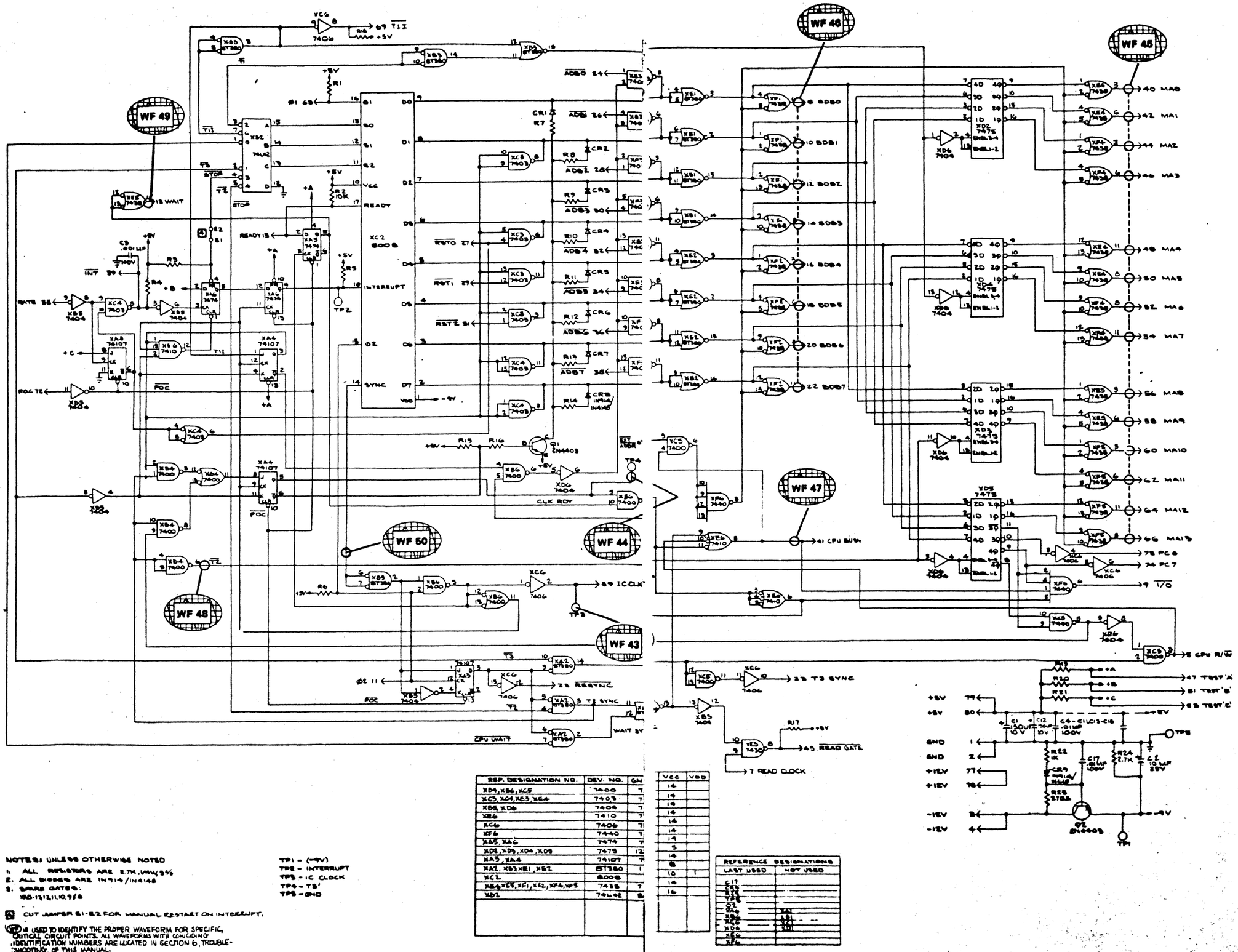


NOTES: UNLESS OTHERWISE SPECIFIED

1. ADD 26 AWG BUSSWIRE (ITEM 42) BETWEEN E1 & E2.
2. C1 IS ALLOWED TO BE .400 MAX HEIGHT.

TITLE PWB ASSEMBLY PROCESSOR

DWG NO | REV



RSP. DESIGNATION NO.	DEV. NO.	QN
XD4, XD6, XC5	7400	7
XC3, XC4, XC5, XC4	7403	7
XD5, XD6	7404	7
XE6	7410	7
XC6	7406	7
XF6	7440	7
XA5, XA6	7474	7
XD2, XD3, XD4, XD5	7475	12
XA3, XA4	74107	7
XA2, XB3 XE1, XE2	8T380	1
XC2	8008	1
XE4, XE5, XF1, XE2, XF4, XF5	7438	7
XB2	74L42	8

VCC	VDD
14	
14	
14	
14	
14	
14	
14	
5	
14	
8	
10	1
14	
16	

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C17	
CR9	
R25	
Q2	
XA4	XA1
XB2	XB1 ---
XC6	XC1
XD6	XD1
XE6	XE1
XF6	XF1

NOTES: UNLESS OTHERWISE NOTED

1. ALL RESISTORS ARE 2.7K, 1/4W, 5%
2. ALL DIODES ARE IN914/IN4148
3. SAME GATES:
   XB5-13,12,11,10,9,8

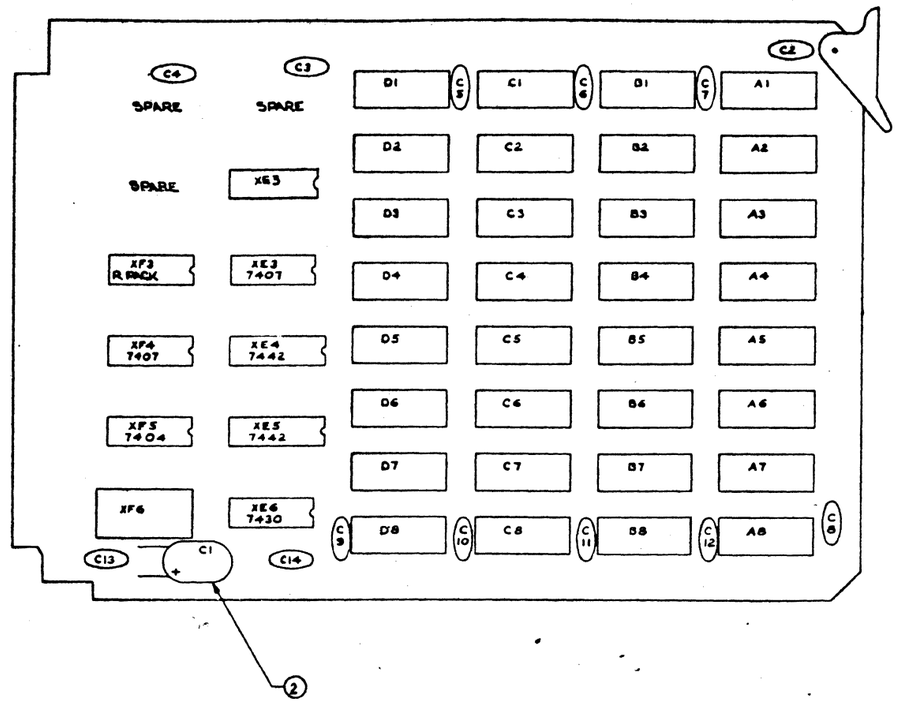
A CUT JUMPER E1-E2 FOR MANUAL RESTART ON INTERRUPT.

WF# IS USED TO IDENTIFY THE PROPER WAVEFORM FOR SPECIFIC CRITICAL CIRCUIT POINTS. ALL WAVEFORMS WITH COINCIDING IDENTIFICATION NUMBERS ARE LOCATED IN SECTION 6, TROUBLESHOOTING, OF THIS MANUAL.
#—O INDICATES OTHER CIRCUIT POINTS WHERE THE SAME WAVEFORM SHOULD APPEAR.

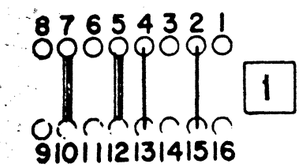
TP1 - (-9V)
TP2 - INTERRUPT
TP3 - IC CLOCK
TP4 - T3'
TP5 - GND

TITLE: SCHEMATIC DIAGRAM PROCESSOR
DWG NO. 96-369-01 REV C

DRAWINGS



ADDRESS JUMPER TABLE					
THIS OPTION	1–16	2–15	3–14	4–13	OCTAL ADDRESS LOCATION
✓	OPEN	JMPR	OPEN	JMPR	0000–7777
	JMPR	OPEN	OPEN	JMPR	10000–17777
	OPEN	JMPR	JMPR	OPEN	20000–27777



ADDRESS JUMPER DETAIL
SEE ADDRESS TABLE

2 PAGE PROM CONFIGURATION

D	C	B	A	
1617	1633	1885	1632	1
1619	1635	1618	1634	2
1621	1826	1714	1825	3
1623	1887	1622	1886	4
1625	1889	1624	1888	5
1627	1643	1626	1642	6
1629	1648	1628	1644	7
1631	1828	1630	1827	8

NOTES: UNLESS OTHERWISE SPECIFIED
1. JUMPERS 7-10 & 5-12 ARE ALWAYS USED, REGARDLESS OF THE OPTION.
2. C1 IS ALLOWED TO BE .900 MAX HEIGHT.

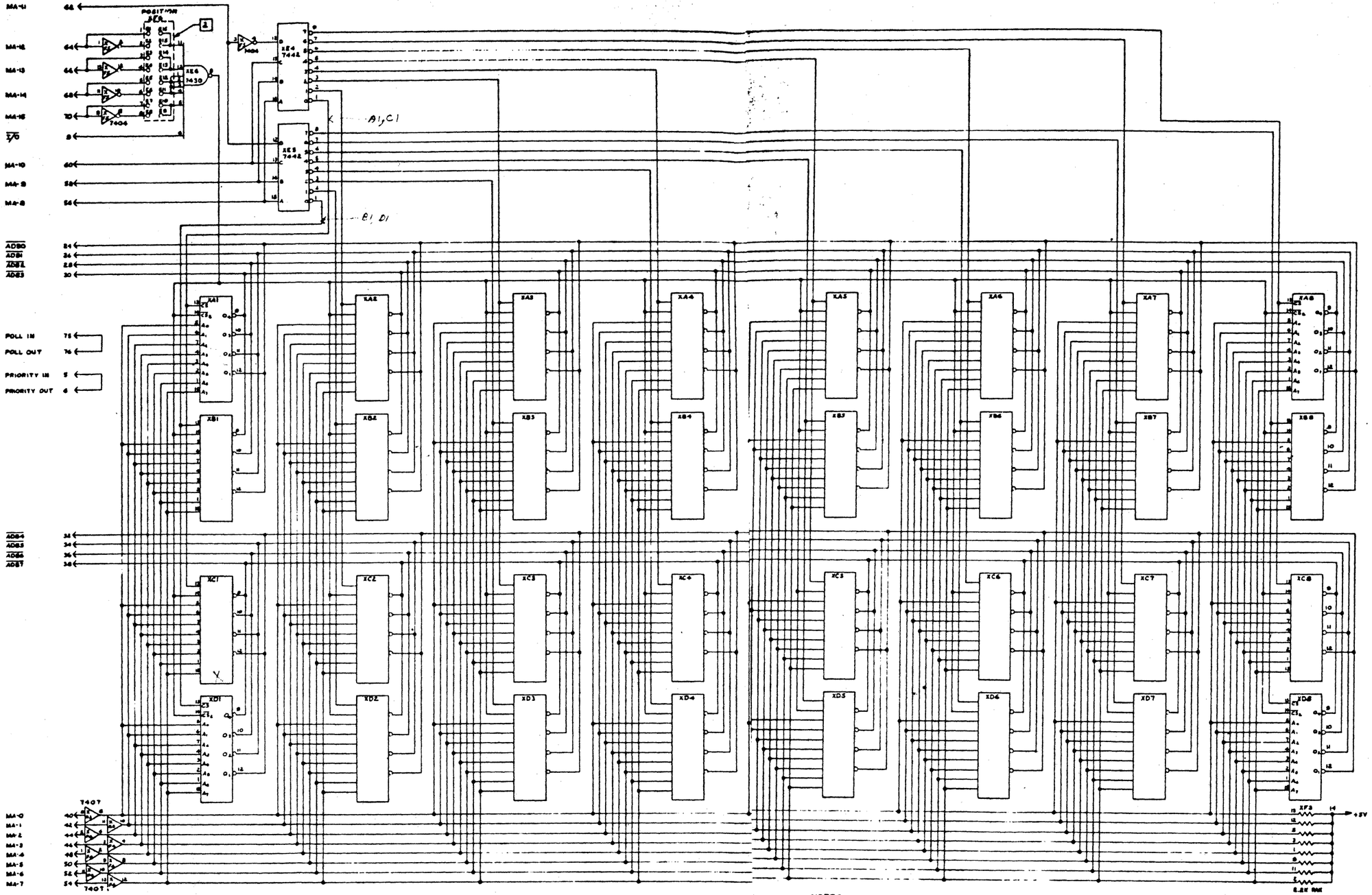
TITLE	
PWB ASSEMBLY BUFFERED PROM	
DWG NO 99-436-36	REV A

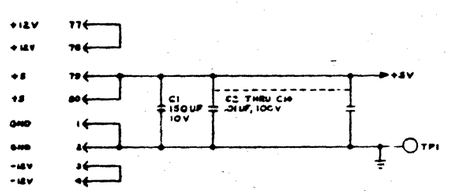
PROMS { MMI 6300-1

256 x 4
14 BITS WIDE

60 NS
SINGLE +5V
TRI-STATE OUTPUT

6300-1 SAME AS SIGNETICS 825126
FIELD PROGRAMMABLE
NI-CR FUSIBLE LINK





REF DESIG. NO.	DEV NO.	GND	VCC
XA1-XA8, XB1-XB8, XC1-XC8, XD1-XD8	[1]	8	16
XE2, XE3, XF4	7407	7	14
XE4, XE5	7442	8	16
XE1	7404	7	14
XE6	74S30	7	14
XF5	RES. PACK	—	14

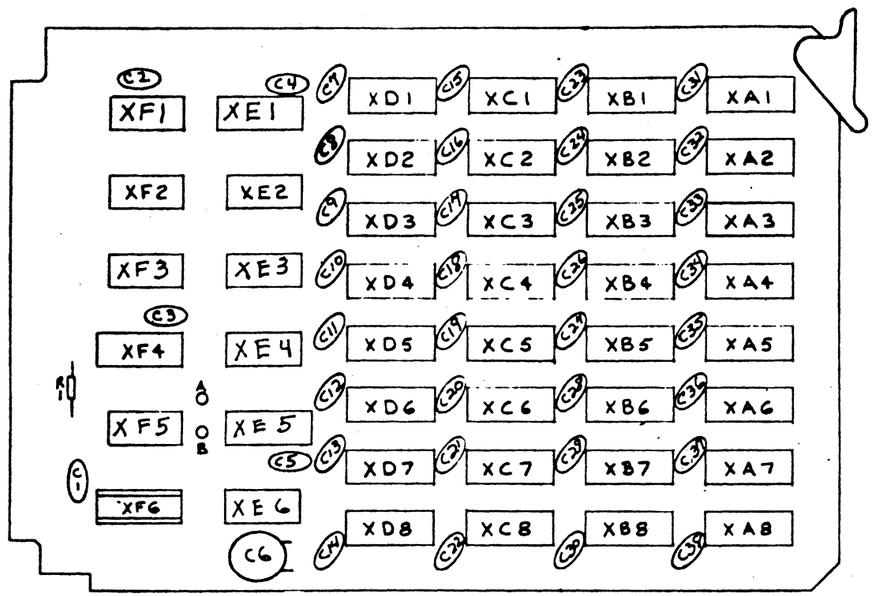
REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C10, XA8, XB8, XC8, XD8, XE6, XF5	XE1, XF1, XF2

NOTES: UNLESS OTHERWISE SPECIFIED:
[1] REFERENCE APPROPRIATE OPTION DRAWING [illegible] XA-
[2] JUMPER E5 TO E12 AND E7 TO E10 ON HEADER XF5.

8-17

TITLE: SCHEMATIC DIAGRAM BUFFERED PROM
DWG NO 96-434-XX | REV A

DRAWINGS

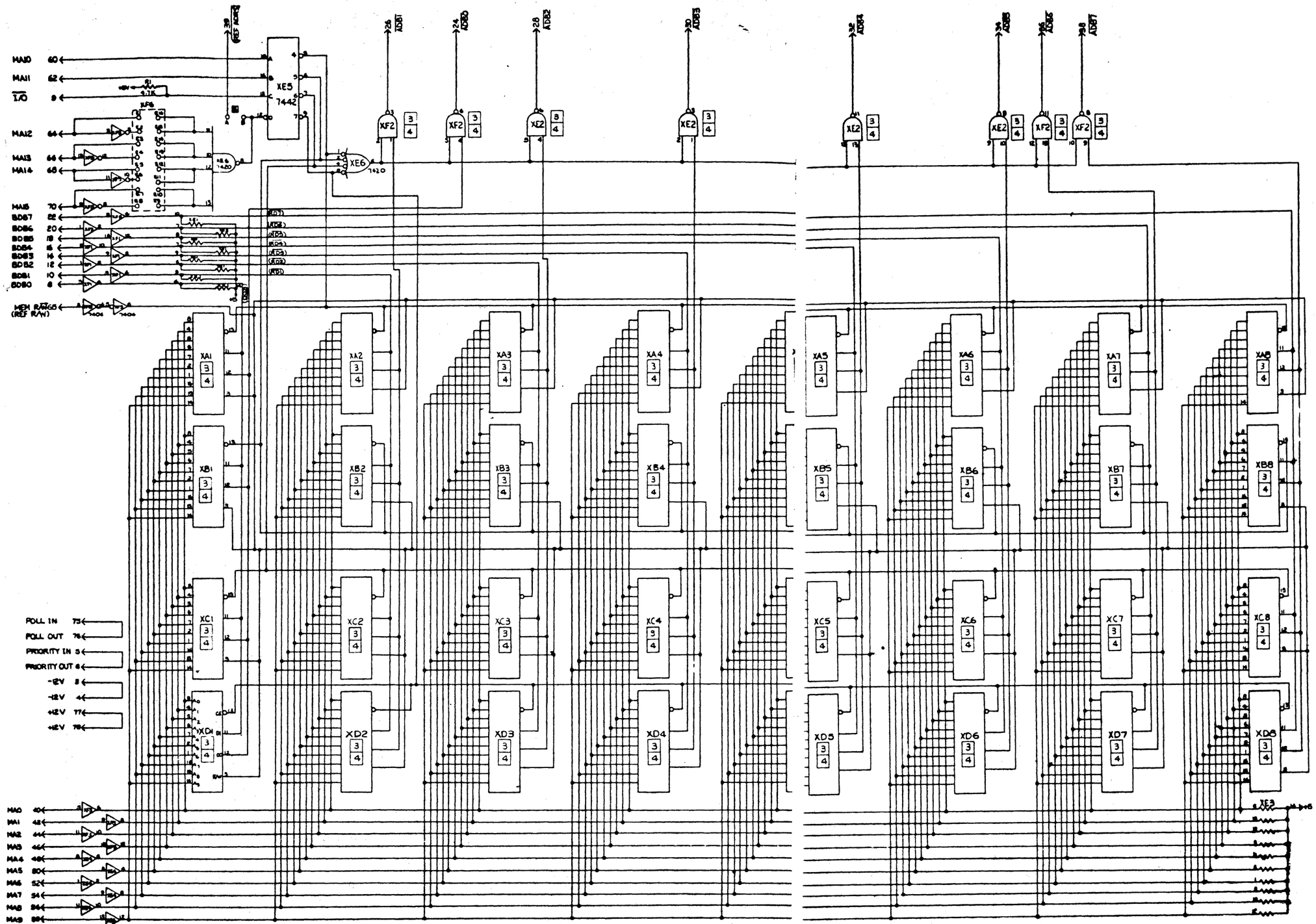


OPTION	BYTES OF RAM		LOAD 2102-2	LOAD 74H00	LOAD 7438	JUMPERS ON XFG	JUMPERS ON PWB		NOTES
							OPEN	JUMPER	
-08	1024		XD1-XD8	XE2, XF2	—	1-16, 3-14 5-12, 7-10	—	A-B	[1]
-09	2048		XC1-XC8 XD1-XD8	XE2, XF2	—	1-16, 3-14 5-12, 7-10	—	A-B	[1]

NOTES: UNLESS OTHERWISE SPECIFIED

[1] REFRESH RAM (BUFFERED)

TITLE	
PWB ASSEMBLY BUFFERED RAM	
DWG NO 99-445-XX	REV B



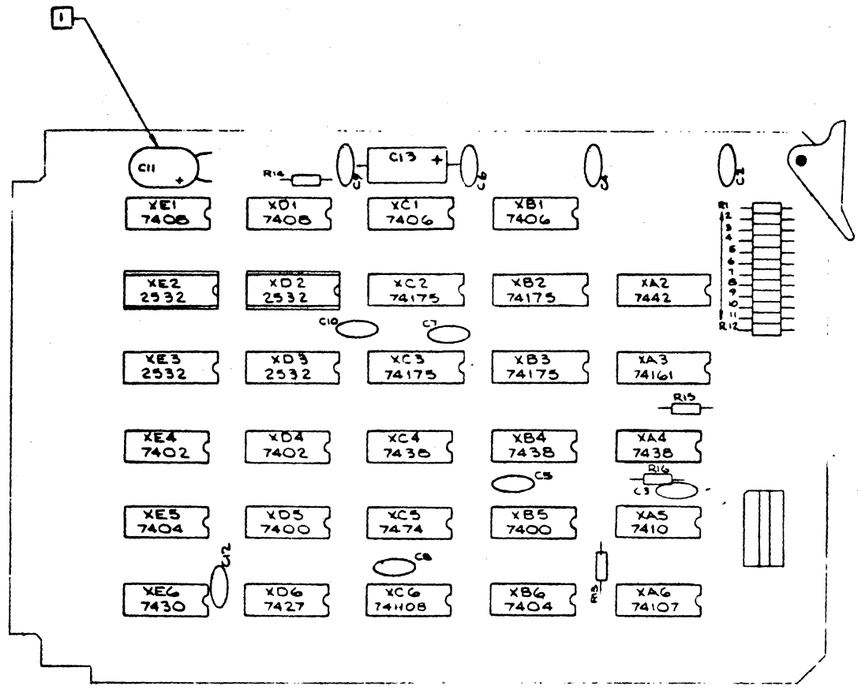
NOTES: UNLESS OTHERWISE SPECIFIED:
1. NUMBERS USED IN REFRESH RAM POSITION MNEMONICS IN PARENTHESES APPLY.
2. SEE ASSEMBLY DRAWING FOR FULL CONFIGURATION. (DWG NO. 99-445-XX)
3. USE 2108-2 AND 74H00 FOR REFRESH RAM OPTIONS -01 AND -06, -08 AND -09.
4. USE 2102-2 AND 7488 FOR MANIFOLD RAM OPTIONS -05, -04, -06, -07.
5. ADD JUMPER A-B FOR OPTIONS -01 AND -02. REMOVE JUMPER FOR OPTIONS -05, -04, -06 AND -07.

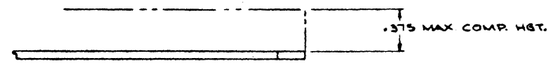
REF. DESIG. NO.	DEV. NO.	GND	VCC	
XA1-XA8, XB1-XB8 XC1-XC8, XD1-XD8	2102-2	9	10	3/4
XE5	7442	8	16	
XE1, XF8	74H00/74S8	7	14	2/4
XF8	7404	7	14	
XE6	7420	7	14	
XF1, XF5, XE4	7407	7	14	
XE1, XE3	RESISTOR N		2.2K	

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C38	
XA8	
XB8	
XC8	
XD8	
XE8	
XF8	
R1	XE4

TITLE: SCHEMATIC DIAGRAM BUFFERED RAM
DWG NO: 96-433-XX REV: B

DRAWINGS

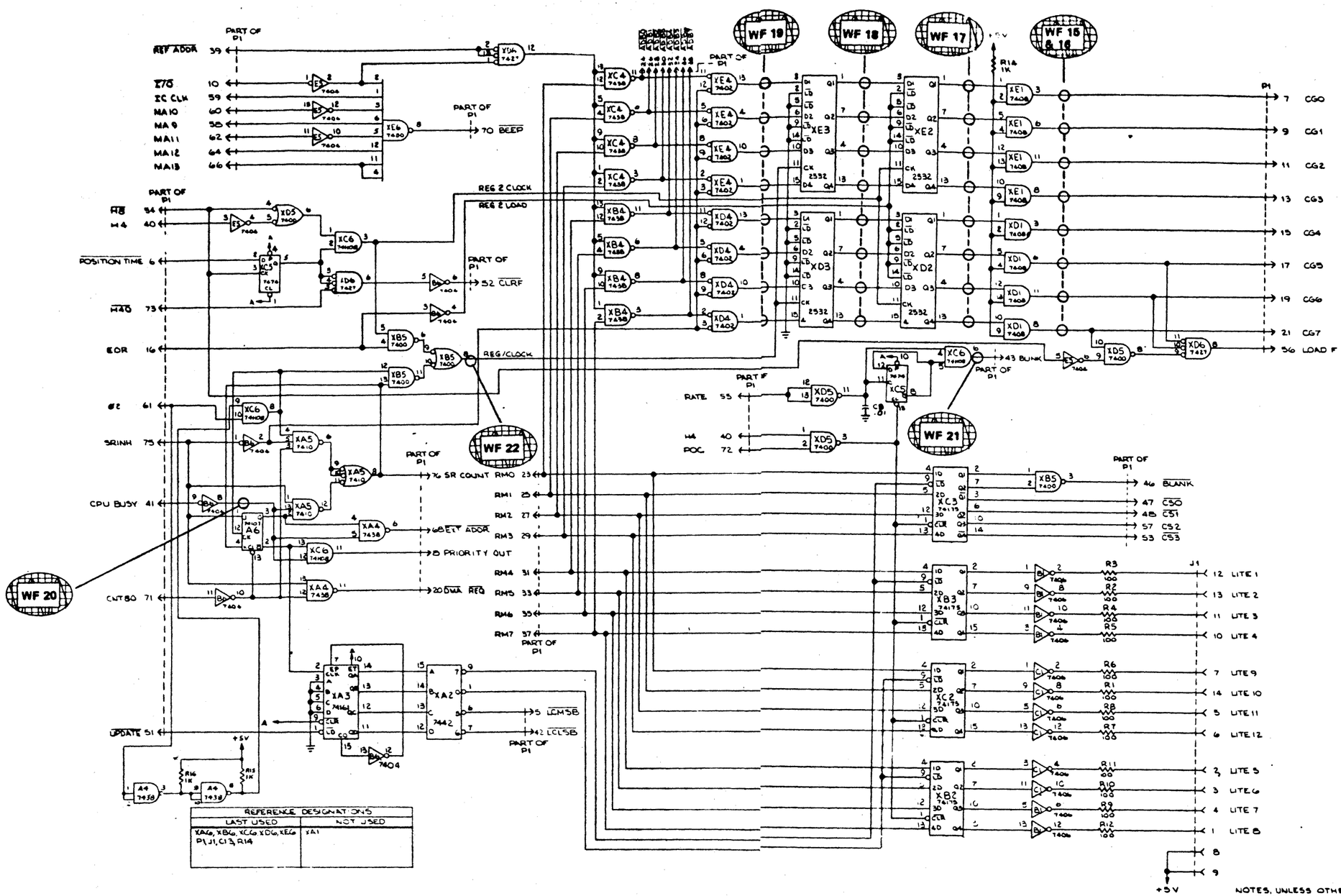




NOTES: UNLESS OTHERWISE SPECIFIED.

[1] C11 IS ALLOWED TO BE .410 MAX HEIGHT.

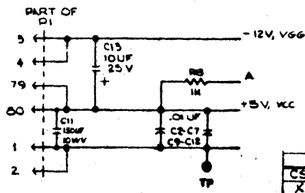
TITLE	PWB ASSEMBLY REFRESH BUFFER
DWG NO. 99-415-01	REV C

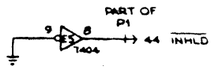


REFERENCE DESIGNATIONS

LAST USED	NOT USED
XA6, XB6, XC6 XD6, XE6 P1, J1, C13, R14	XA1

REF. DESIG. Nº	DEVICE Nº	VCC	GND	VGG
XA2,	7442	16	8	
XA3	74161	16	8	
XA4, XB4, XC4,	7438	14	7	
XA5,	7410	14	7	
XA6	74107	14	7	
XB1, XC1	7406	14	7	
XB2, XB3, XC2, XC3	74175	16	8	
XB5, XD5	7400	14	7	
XB6, XE5	7404	14	7	
XC5	7474	14	7	
XD1, XE1	74C8	16	7	
XD2, XD3, XE2, XE3	2532	16	5	12
XD4, XE4	7402	14	7	
XD6	7427	14	7	
XE6	7430	14	7	
XC6	74HC08	14	7	





CURSOR SPECIFICATIONS

CS3	CS2	CS1	CS0	FUNCTION
X	X	0	0	UNDERLINE CURSOR, VIDEO ON
X	X	0	1	BLOCK CURSOR, VIDEO ON
X	X	1	0	CURSOR OFF
X	X	1	1	VIDEO OFF (BLANK)
X	1	X	X	BLANK CONTROL CHARACTERS
1	X	X	X	COMPACTED MODE

NOTES, UNLESS OTHERWISE SPECIFIED:

1. SPARES:

   74107- XA6- PINS 5,6,8,9,10, AND 11

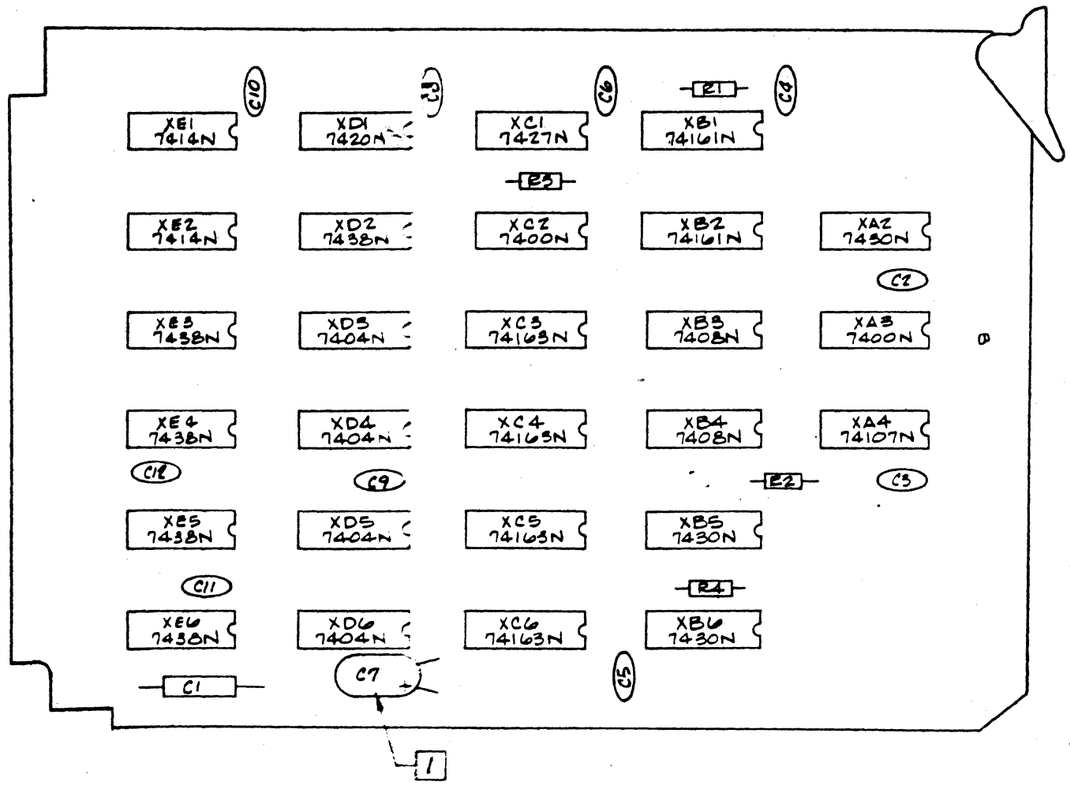
2. ALL RESISTORS ARE 1/4 WATT, 5%
3. ALL CAPACITOR VALUES ARE IN UF

WF IS USED TO IDENTIFY THE PROPER WAVEFORM FOR SPECIFIC, CRITICAL CIRCUIT POINTS. ALL WAVEFORMS WITH COINCIDING IDENTIFICATION NUMBERS ARE LOCATED IN SECTION 6, TROUBLE-SHOOTING, OF THIS MANUAL.
⊕—⊖ INDICATES OTHER CIRCUIT POINTS WHERE THE SAME WAVEFORM SHOULD APPEAR.

TITLE: SCHEMATIC DIAGRAM REFRESH BUFFER

DWG NO 96-416-01 REV C

DRAWINGS



1 NOTES: UNLESS OTHERWISE SPECIFIED
MAX. COMPONENT SHALL BE .375, EXCEPT
C7 SHALL BE ALLOWED A MAX HEIGHT
OF .410

TITLE	PWB ASSEMBLY REFRESH CONTROL
DWG NO 99-457-01	REV B

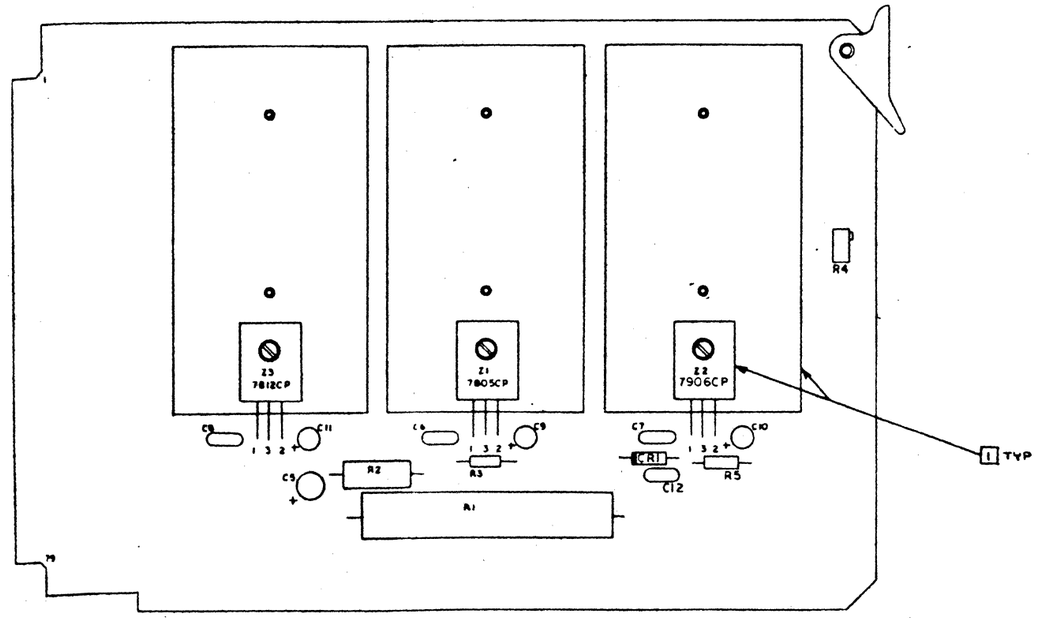
REFERENCE DESIGNATIONS	
LAST USED	NOT USED
XA4, XB6, XC6, XD6, XE6	XA1
E4, C12, P1	

REF DESIGNATE	DEVICE NR	VCC	GND
XA2, XB5, XB6	7430	14	7
XA5, XC2	7400	14	7
XA3	74107	14	7
XB1, XB2	74161	16	8
XB3, XB4	7408	14	7
XA1	7427	14	7
XC3, XC4, XC5, XC6	74163	16	8
XD1	7420	14	7
XD2, XE3, XE4, XE5, XE6	7438	14	7
XD3, XD4, XDE, XD6	7404	14	7
XE1, XE2	7414	14	7

NOTES: UNLESS OTHERWISE SPECIFIED
1) SPARES: 7404. XD4 - PINS 12 & 13.
7404. XD5 - PINS 1 & 2.
7404. XD6 - PINS 1 & 13.
2) ALL RESISTORS ARE 1/4 WATT, ±5%.
3) ALL CAPACITOR VALUES ARE IN µF

WF) IS USED TO IDENTIFY THE PROPER WAVEFORM FOR SPECIFIC CRITICAL CIRCUIT POINTS. ALL WAVEFORMS WITH CORRESPONDING IDENTIFICATION NUMBERS ARE LOCATED IN SECTION 6, TROUBLESHOOTING, OF THIS MANUAL.
→ INDICATES OTHER CIRCUIT POINTS WHERE THE SAME WAVEFORM SHOULD APPEAR.

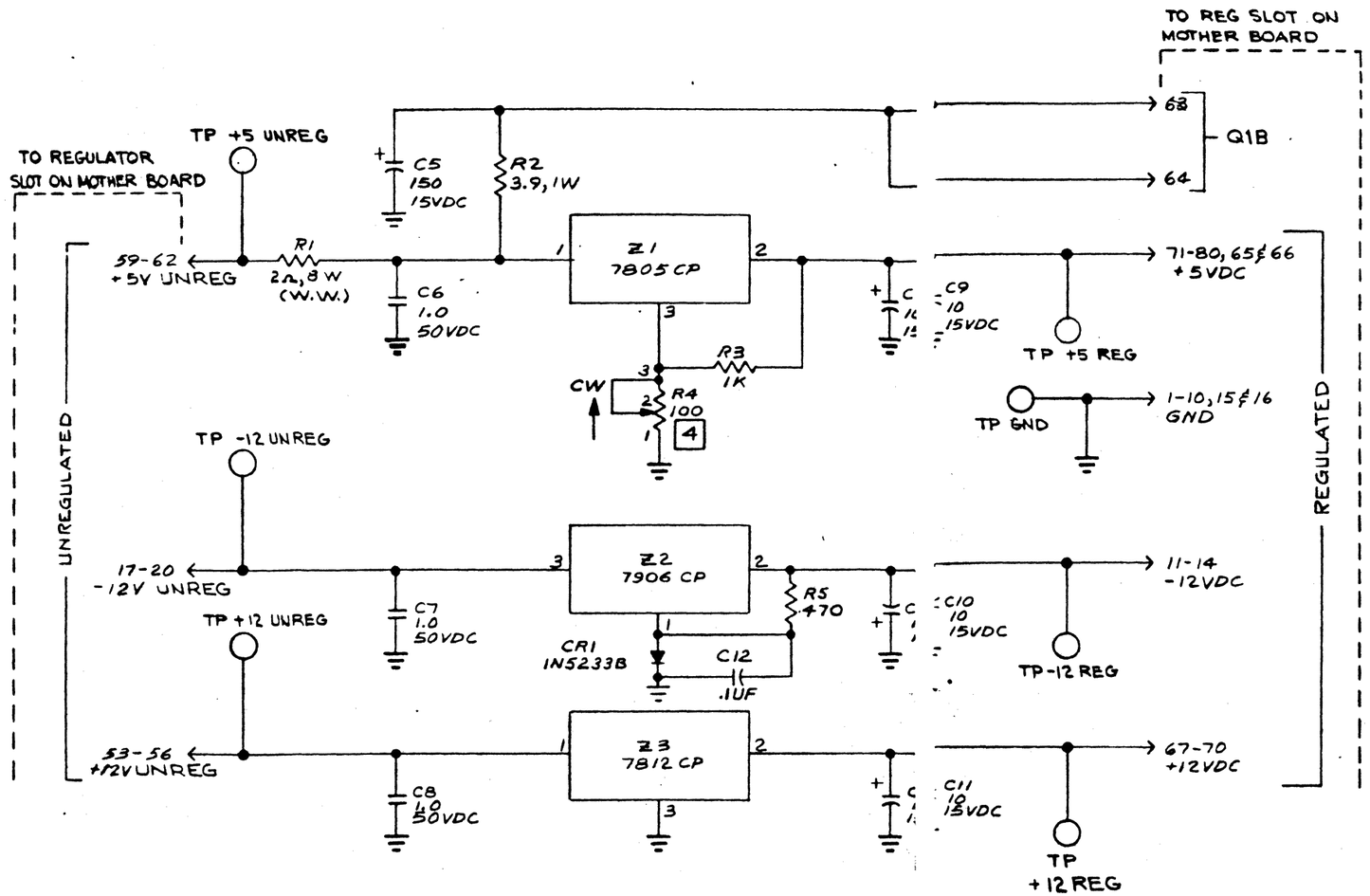
DRAWINGS



NOTES: UNLESS OTHERWISE SPECIFIED

[1] USE HEATSINK COMPOUND BETWEEN P.W. BOARD AND ITEM 7 AND BETWEEN ITEM 7 AND Z1, Z2 & Z3.

TITLE	PWB ASSEMBLY REGULATOR
DWG NO	99-402-01
REV	B



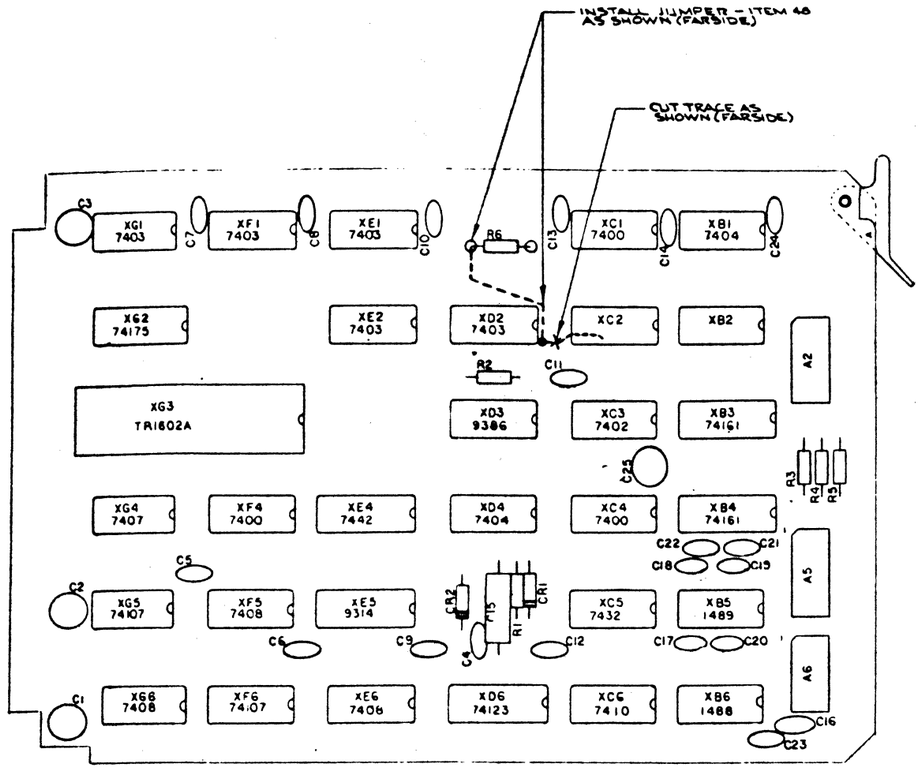
NOTES: UNLESS OTHERWISE SPECIFIED -

1. ALL RESISTORS ARE 1/4 W, 5%, CARBON.
2. ALL RESISTORS VALUES ARE IN OHMS
3. ALL CAPACITORS VALUES ARE IN MICROFARADS.
4. R4 TO BE ADJUSTED TO PROVIDE 5.15 ± 0.10 VDC AT THE REG +5V TEST POINT. LOCK R4 WITH GLYP. AFTER ADJUST.

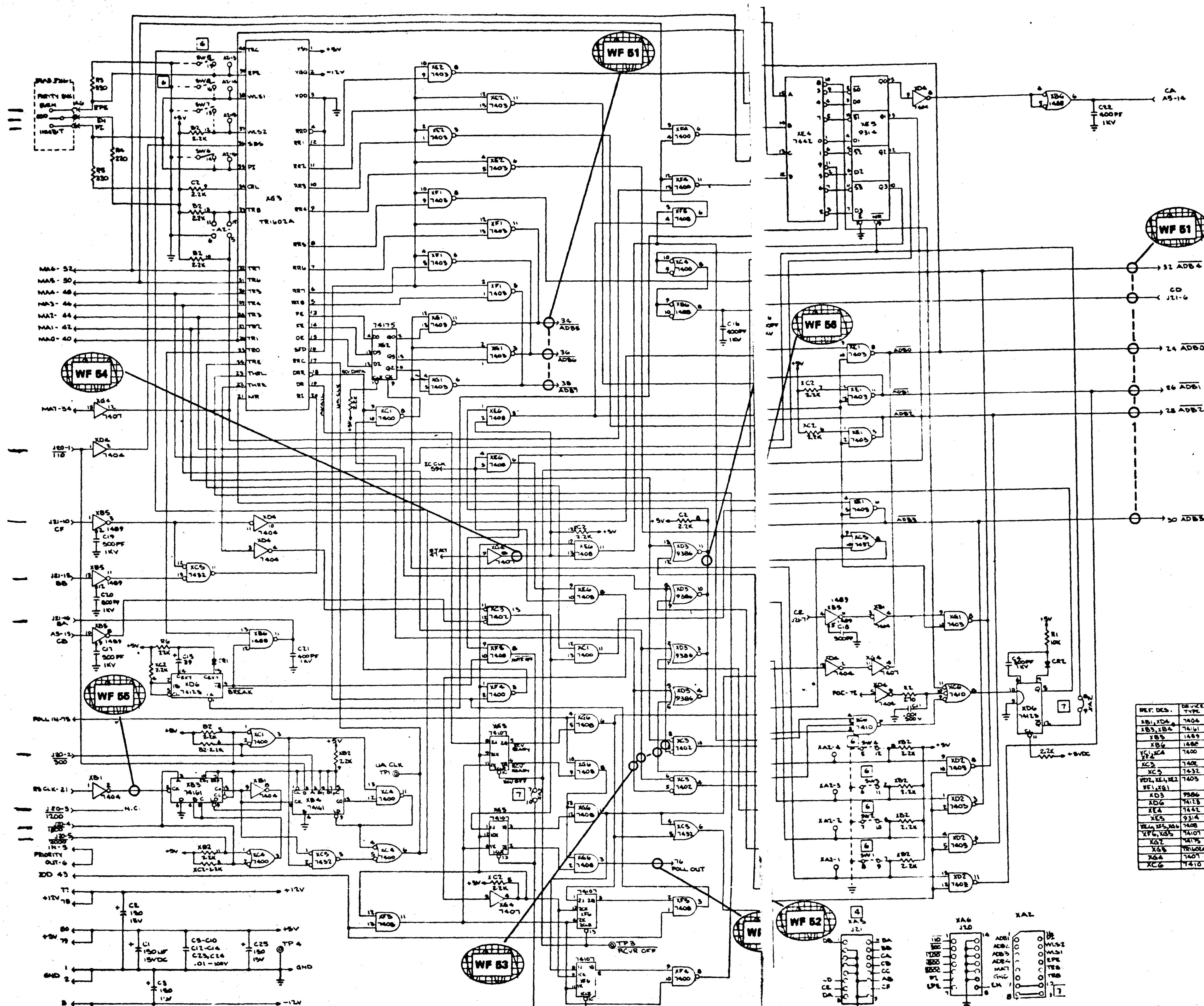
TITLE: SCHEMATIC DIAGRAM REGULATOR

DWG NO 96-402-01 REV B

DRAWINGS



TITLE	
ASSY. OF RS232 ASYNC. INTERFACE	
DWG NO 99-451-01	REV A



XA2 JUMPERS

DEVICE ADR.	JUMPER
32	2-6
34	1-6
36	—
POLARITY OF STD BIT WHEN PARITY OFF SELECTED.	
ZERO	6-11
ONE	—
MA7	5-12

XA6 JUMPERS

BAUD RATE	JUMPER
110	1-14
300	2-13
1200	3-12
1800	4-11
2000	5-10
PARITY SELECT	JUMPER
EVEN	7-8
ODD	—
OFF	6-8

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE 1/4W, ±5%.
2. ALL CAPACITANCE IS IN MICROFARADS
3. ALL RESISTANCE IS IN OHMS.
4. RS232 CONNECTIONS:

DES	FUNCTION
AB	SIGNAL GROUND
BA	TRANSMITTED DATA
BB	RECIEVED DATA
CA	REQUEST TO SEND
CB	CLEAR TO SEND
CC	DATA SET READY
CD	DATA TERMINAL READY
CE	RING INDICATOR
CF	RECIEVED LINE SIG. DETECTOR
DA	SIGNAL TIMING TO DCE*
DB	SIGNAL TIMING FROM DCE*
*	DCE = DATA COMMUNICATION EQUIPMENT

5. ALL DIODES ARE IN914/IN4148
6. SWITCH PACK (XA1) IS NOT USED ON THIS CONFIGURATION AT THIS TIME.
7. NORMALLY JUMPERED. PROVIDED FOR TEST PURPOSES ONLY.

WF IS USED TO IDENTIFY THE PROPER WAVEFORM FOR SPECIFIC, CRITICAL CIRCUIT POINTS. ALL WAVEFORMS WITH COINCIDING IDENTIFICATION NUMBERS ARE LOCATED IN SECTION 6, TROUBLE-SHOOTING, OF THIS MANUAL.
⊕—O INDICATES OTHER CIRCUIT POINTS WHERE THE SAME WAVEFORM SHOULD APPEAR.

REF. DES.	DEVICE TYPE	+5	GND	+12	-12
XB1, XD4	7404	14	7	—	—
XB3, XB4	74161	16	8	—	—
XB5	1489	14	7	•	—
XB6	1488	—	7	14	1
XC1, XC4 XF4	7400	14	7	—	—
XC3	7402	14	7	—	—
XC5	7432	14	7		
XD2, XE4, XE2 XF1, XG1	7403	14	7	—	—
XD3	9386	14	7	—	—
XD6	74123	16	8	—	—
XE4	7442	16	8	—	—
XE5	9314	14	7		
XE6, XF5, XA6	7408	14	7	—	—
XF6, XG5	74107	14	7	—	—
XG2	74175	16	8	—	—
XG3	TR1602A	1	3	—	2
XG4	7407	14	7	—	—
XC6	7410	14	7	—	—

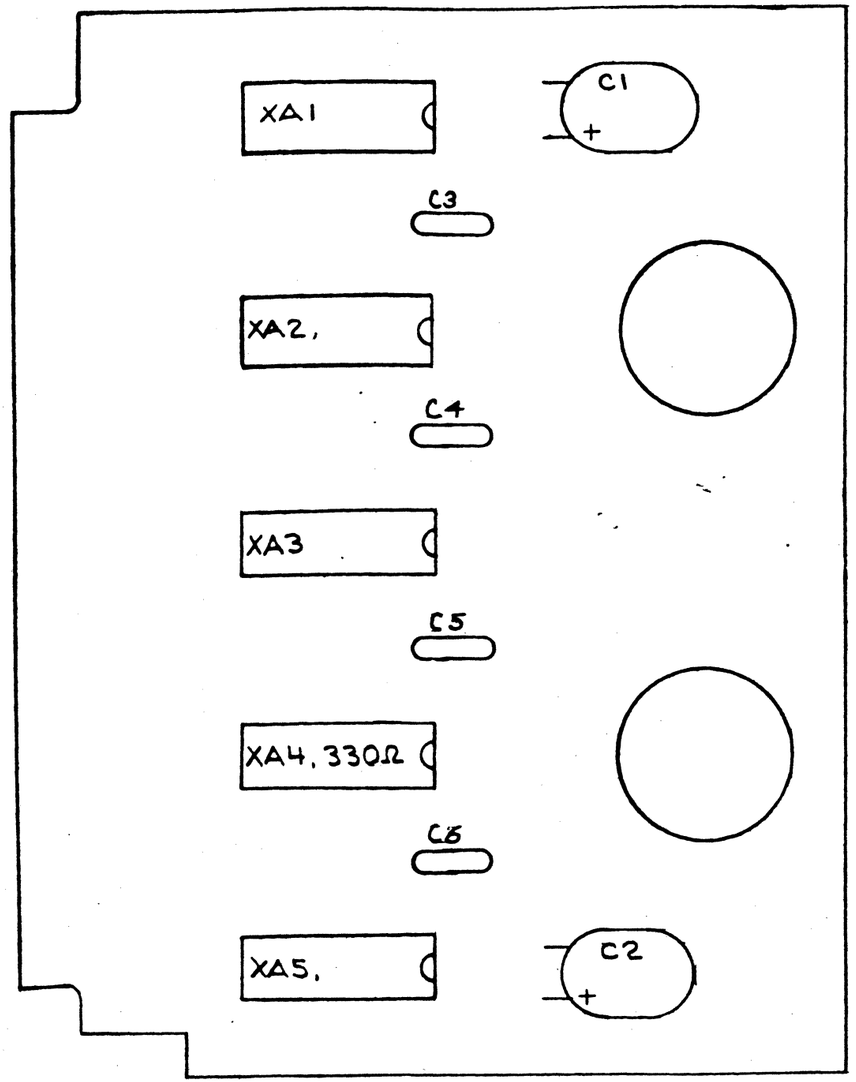
SPARE GATES	
XB6	PINS 2 & 3 - 1488
XC1	PINS 4, 5 & 6 - 7400
XC3	PINS 1, 2 & 3 - 7402
XC6	PINS 1, 2, 12 & 13 - 7410
XG4	PINS 1, 2, 5 & 6 - 7407
XB1	PINS 5, 6 10, 11, 12 & 13

PARITY + BAUD RATE

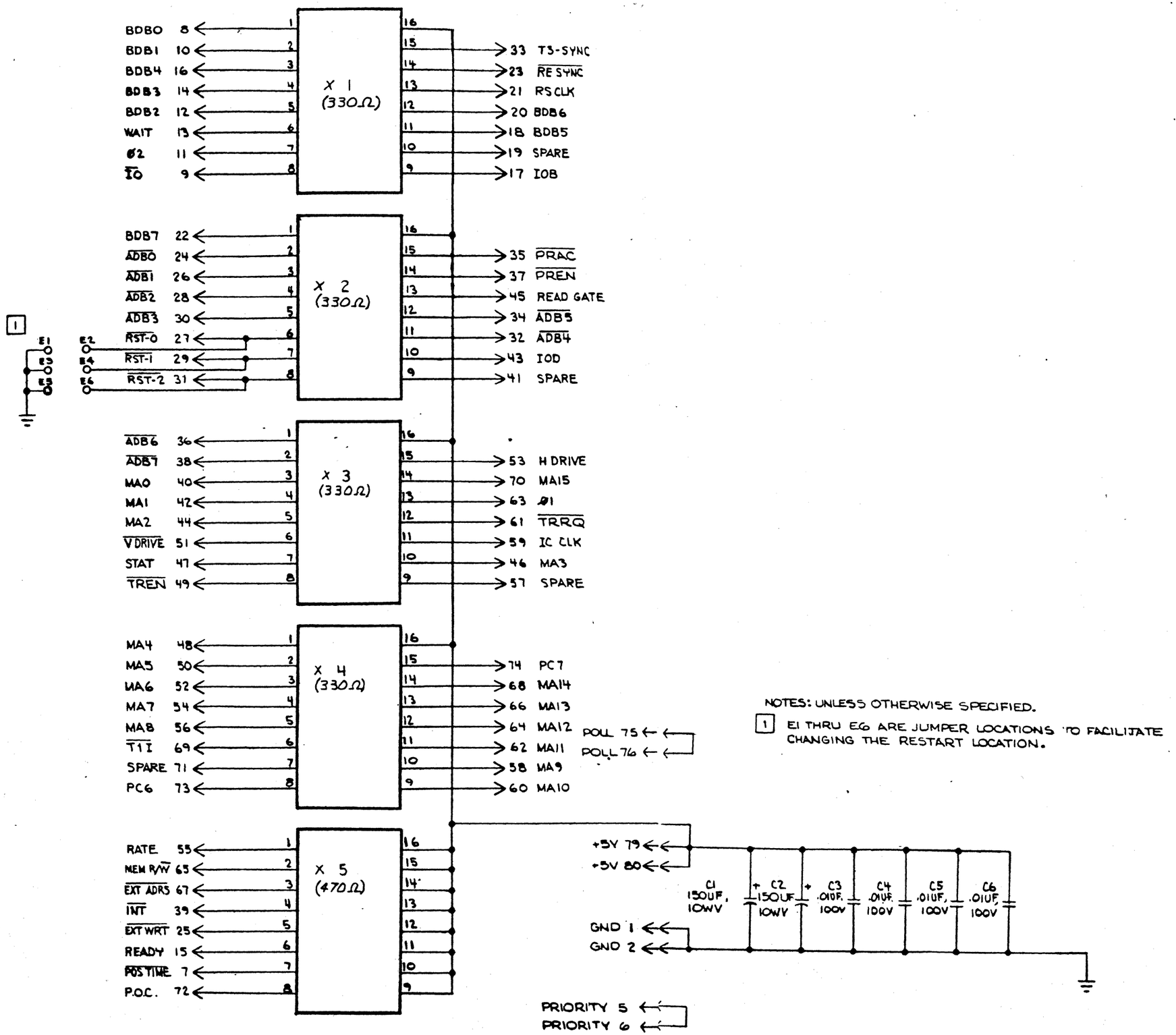
EN TO PI = NO PARITY
EPE TO EN = EVEN PARITY
NC = ODD PARITY

TITLE SCHEMATIC RS232 ASYNC. INTERFACE

DWG NO 96-451-01 REV A



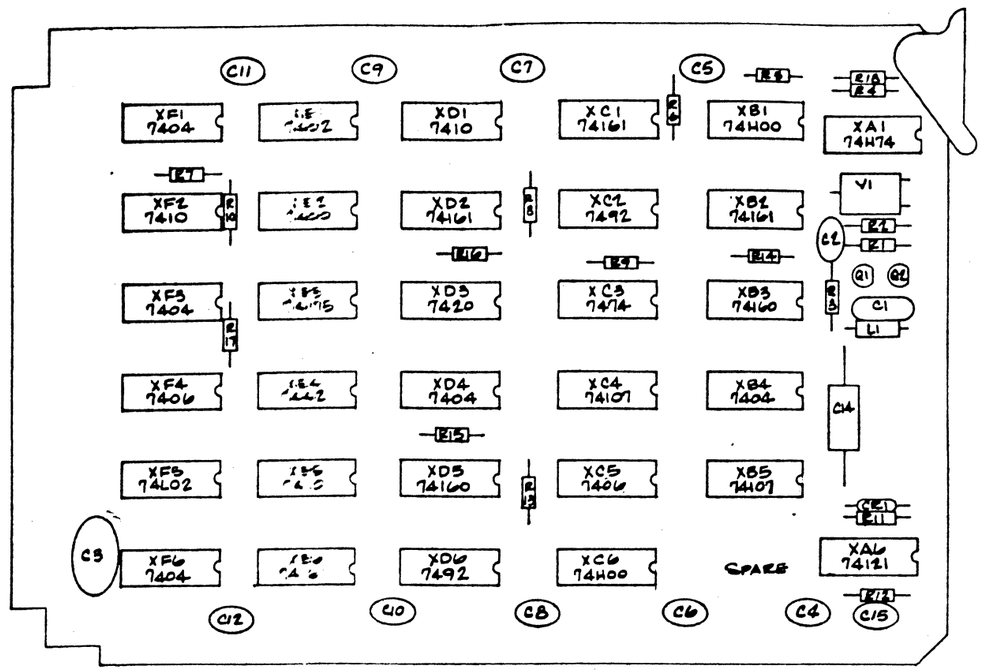
TITLE	
PWB ASSEMBLY TERMINATOR	
DWG NO 99-394-01	REV B



NOTES: UNLESS OTHERWISE SPECIFIED.

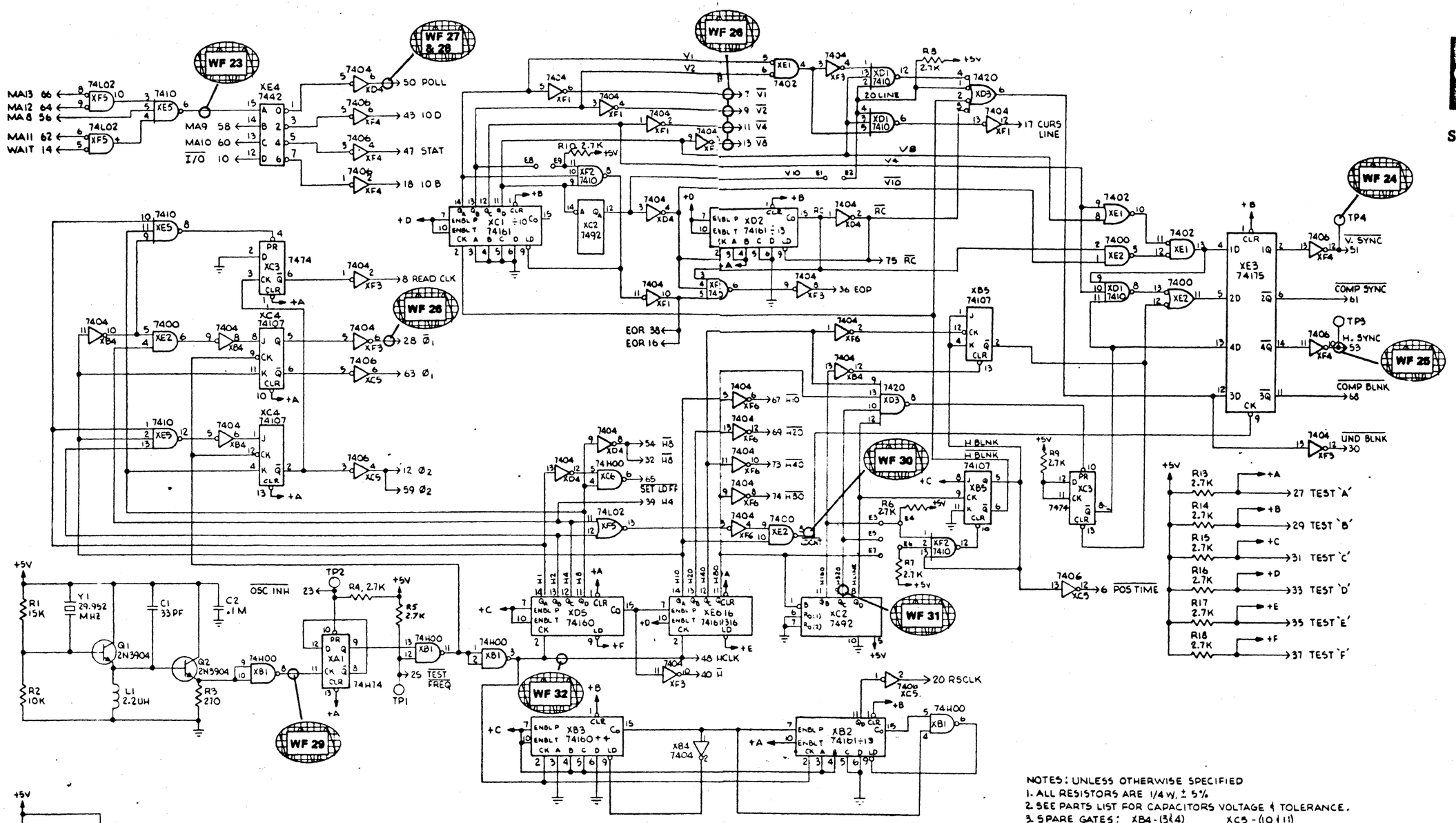
[1] E1 THRU E6 ARE JUMPER LOCATIONS TO FACILITATE CHANGING THE RESTART LOCATION.

DRAWINGS



NOTES: UNLESS OTHERWISE SPECIFIED
1) MAX. COMPONENT HEIGHT .375.
2) C3 IS ALLOWED TO BE .400 MAX HEIGHT.

TITLE	PWB. ASSEMBLY TIMING CONTROL	
DWG NO	99-452-01	REV C



TP1 TEST FREQ
TP2 OSC INH
TP3 I/O COMMAND
TP4 Ø2
TP5 V DRIVE
TP6 H DRIVE
TP7 GND

OPTION TABLE			
OPTION	JUMPER	CUT	FUNCTION
	E1-E2		12 ROWS
STANDARD		E1-E2	24 ROWS
STANDARD	E3-E4		80 CHARS/LINE
	E5-E4 E6-E7		72 CHARS/LINE
	E5-E6	E3-E4	64 CHARS/LINE
	E3-E4		40 CHARS/LINE
STANDARD		E8-E9	60 HZ
	E8-E9		50 HZ

REFERENCE DESIGNATOR	
LAST USED	NEXT USED
XA6 XB5, XC6	XA7 XA8
XD6, XE6, XF6	XB6, XC7
C15, CR1, L1, R18	
Y1, Q2	

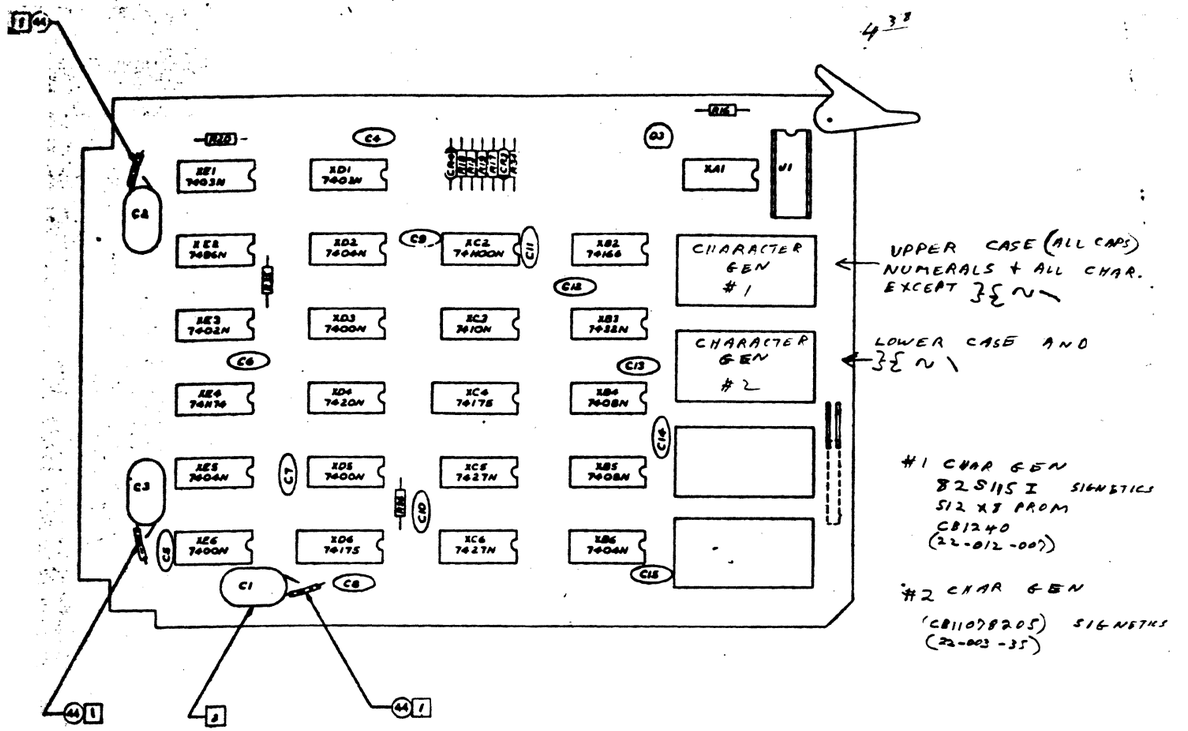
REF DESIG NO.	DEVICE NO.	GND	VCC
XE2	7400	7	14
XE1	7402	7	14
XB4, XD4, XF1, XF3, XF6	7404	7	14
XD1, XE5, XF2	7410	7	14
XD5	7420	7	14
XC2, XD6	7492	10	5
XB5, XC4	74107	7	14
XA6	74121	7	14
XB3, XD5	74160	8	16
XC1, XD2, XE6, XB2	74161	8	16
XE3	74175	8	16
XB1, XC6	74H00	7	14
XA1	74H74	7	14
XC3	7474	7	14
XF4, XC5	7406	7	14
XF5	74L02	7	14
XE4	7442	8	16

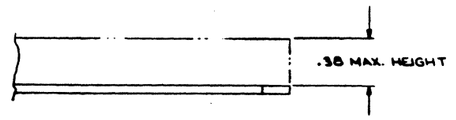
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4 W, ± 5%
2. SEE PARTS LIST FOR CAPACITORS VOLTAGE & TOLERANCE.
3. SPARE GATES: XB4 - (3 & 4) XC5 - (10 & 11)
XC6 - (1, 2 & 3), (8, 9 & 10), (11, 12 & 13)
XD4 - (10 & 11), XE1 - (4, 5 & 6)
XF5 - (1, 2 & 5), XA1 - (1, 2, 3, 4, 5 & 6)
4. ABBREVIATIONS (NOT STANDARD)
LD - LOAD
CLR - CLEAR
CO - CARRY OUTPUT

WF IS USED TO IDENTIFY THE PROPER WAVEFORM FOR SPECIFIC, CRITICAL CIRCUIT POINTS. ALL WAVEFORMS WITH CONCIDING IDENTIFICATION NUMBERS ARE LOCATED IN SECTION 6, TROUBLE-SHOOTING, OF THIS MANUAL.
o---o INDICATES OTHER CIRCUIT POINTS WHERE THE SAME WAVEFORM SHOULD APPEAR.

TITLE SCHEMATIC DIAGRAM TIMING CONTROL
DWG NO 96-152-01 REV A

DRAWINGS



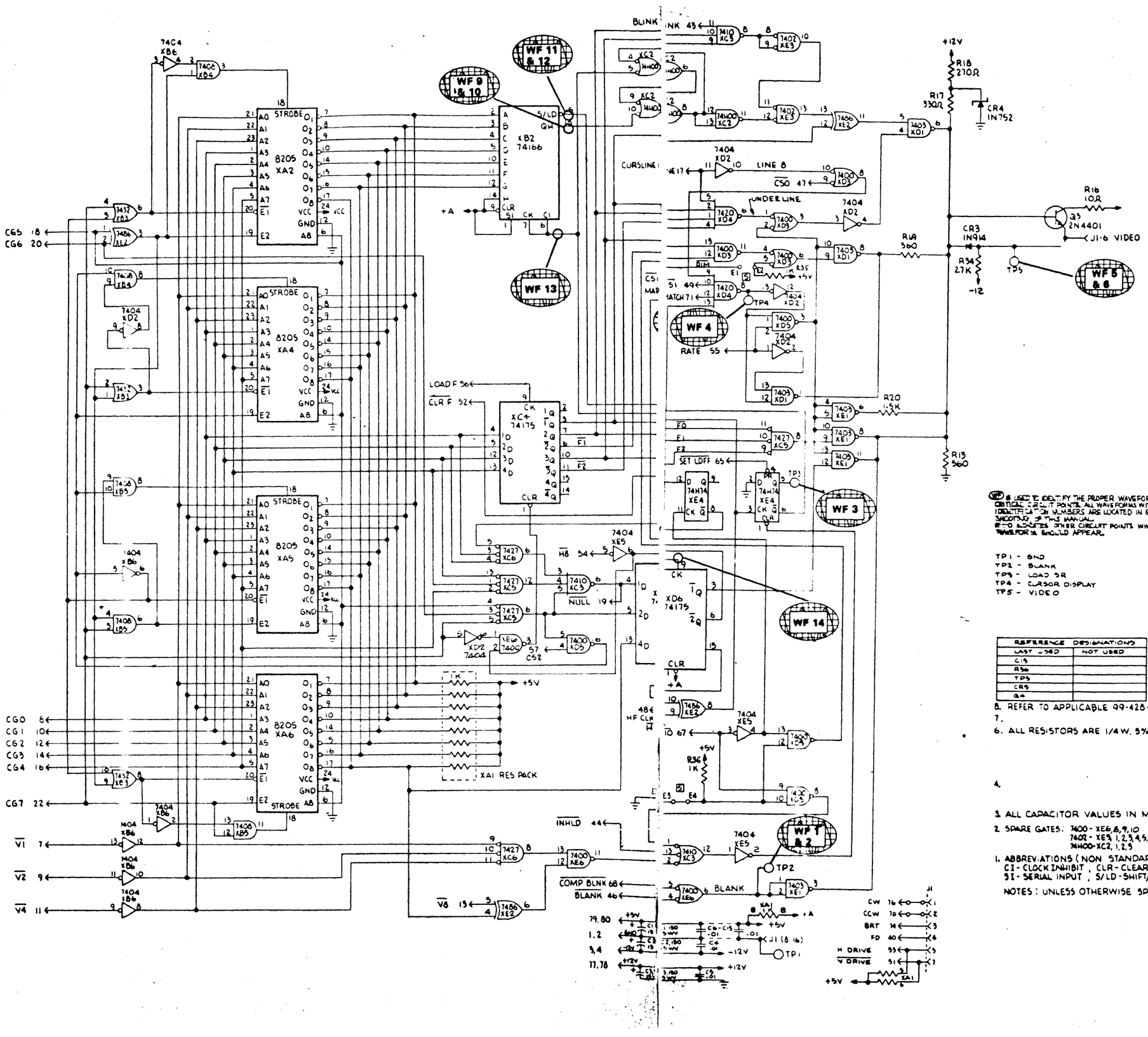


NOTES: UNLESS OTHERWISE SPECIFIED

[1] ADD SLEEVING (ITEM 44) AS REQUIRED.

[4] C1,C2 & C3 ARE ALLOWED TO BE 0.41 MAX. HEIGHT.

TITLE	PWB. ASSY VIDEO CONTROL	
DWG NO.	99-151-01	REV B



WF IS USED TO IDENTIFY THE PROPER WAVEFORM FOR SPECIFIC CRITICAL CIRCUIT POINTS. ALL WAVEFORMS WITH CORRESPONDING IDENTIFICATION NUMBERS ARE LOCATED IN SECTION 6, TROUBLE-SHOOTING, OF THIS MANUAL.
E-O ADDRESSES OTHER CIRCUIT POINTS WHERE THE SAME WAVEFORM SHOULD APPEAR.

TP1 - GND
TP2 - BLANK
TP3 - LOAD SR
TP4 - CURSOR DISPLAY
TP5 - VIDEO

REF DESIG LOCATION	DRV NO	GND	VCC
XA1	RES PACK	—	4
XB5, XB4	7400N	7	14
XB3	7432N	7	14
XD3, XE6, XD5	7400N	7	14
XE3	7402N	7	14
XB1, XD1	7403N	7	14
XE5, XD2, XB6	7404N	7	14
XC3	7410N	7	14
XD4	7420N	7	14
XC5 XC6	7427N	7	14
XE4	74H74N	7	14
XE2	7486N	7	14
XB2	74166N	8	16
XD6, XC4	74175N	8	16
XA3	8205N	12	24
XC2	74-00CN	7	14

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C15	
R36	
TP5	
CR3	
Q4	

8. REFER TO APPLICABLE 99-426-XX FOR CHARACTER GENERATOR SET
7.
6. ALL RESISTORS ARE 1/4 W, 5%

4.

3. ALL CAPACITOR VALUES IN MF

2. SPARE GATES: 7400 - XE6,8,9,10 7427 - XC6 1,2,12,13
7402 - XE3 1,2,3,4,5,6 XE5,8,9,10,11,12,13
74H00 - XC2, 1,2,3 7408 - XB4, 4,5,6,11,12,13 XB5, 1,2,3
7432 - XB3, 11,12,13

1. ABBREVIATIONS (NON STANDARD)
CI - CLOCK INHIBIT, CLR - CLEAR ; FD - FAST DOWN,
SI - SERIAL INPUT, S/LD - SHIFT/LOAD, HDRIVE - HORIZONTAL DRIVE, VDRIVE - VERTICAL DRIVE.

NOTES: UNLESS OTHERWISE SPECIFIED

TITLE: SCHEMATIC DIAGRAM VIDEO CONTROL
DWG NO 96-154-01 REV B

CURSOR CONTROL CARD		ASSEMBLY 99-376-01C
REF. DES.	DESCRIPTION	OMRON P/N
	CAPACITORS	
C18, C19	.001UF, 100V, 10%, Disc	80-320-90
C21, C22	.005UF, 100V Disc	80-320-92
C2,3,4,5,7,8,9, 10,11,12,14,20	.01UF, 100V Disc	80-320-93
C17	.047UF, 100V Mylar	80-312-58
C23	.1UF,50V Disc	80-319-01
C16	4.7UF,10V Tant	80-310-41
C26,27	10UF, 25V Elect	80-305-29
C24	39UF,10V Tant	80-302-08
C13,15,25	10UF,25V 10% Elect	80-305-21
C6,C1	150UF,15V, Tant	80-311-58
	DIODES	
CR1-5,7-11	IN914/IN4148	80-404-03
VRI	Zener IN5227A	80-404-11
	INTEGRATED CIRCUITS	
XC1,XC2, XB2	7400N	80-460-22
XB3,XB4,XB5	7403N	80-460-59
XD3	7404N	80-460-18
XB1	7408N	80-460-50
XE2,XD2,XC3	7474N	80-460-34
XE6	7493N	80-460-39
XE1,XD1,XA1	74123N	80-460-52
XD6,XC6	74161N/9316	80-460-58
XE4,XD4,XC4	74175N	80-460-64
XE5,XD5,XC5	8242/9386	80-460-88
XA4	72747N	80-460-86

CURSOR CONTROL CARD		ASSEMBLY 99-376-01C
REF. DES.	DESCRIPTION	OMRON P/N
	RESISTORS	
R26	100Ω,1/4W,5%	80-211-01
R6,R7	220Ω,1/4W, 5%	80-212-21
R5,15,19,34,33,12	1KΩ,1/4W,5%	80-211-02
R8,13,16,21,24	2.2KΩ,1/4W,5%	80-212-22
R1,27,28,30	2.7KΩ,1/4W,5%	80-212-72
R31,32	12KΩ, 1/4W,5%	80-211-23
R9,10,22	10KΩ, 1/4W,5%	80-211-03
R11,14,17	15KΩ, 1/4W,5%	80-211-53
R18,20,23	22KΩ, 1/4W,5%	80-212-23
R3,4,29	39KΩ, 1/4W,5%	80-213-93
R25	ADJ,10K, Cermet Trimpot	80-270-52
XB6	Pack 4.7K, 1/4W,5%	80-290-50
J23	Socket, 16 Pin Dip	80-676-04
	TRANSISTORS	
Q2, 3,4,5	2N4401	80-419-01
Q1	2N4403	80-423-02
	Ejector	40-109-01

KEYBOARD ASSEMBLY		Assembly 99-453-XXA
REF. DES.	DESCRIPTION	OMRON P/N
	CAPACITORS	
C1,C2	10&F, 25V, Electrolytic	80-305-21
C3,C4	.01UF, 100V, Disc	80-320-93
C5	1000PF, 1KV, Disc	80-319-05
CR1 thru CR67 CR69 thru CR90 CR30 thru 35,40, 41,42,60,62,63 Removed -02	Diode, IN914/IN4148	80-404-03
	INTEGRATED CIRCUITS	
X1	MM5740 BEE/N	80-460-95
X2,X3	SN7404N	80-460-18
	INTEGRATED CIRCUIT SOCKETS	
J71	16 Pin Dip	80-676-04
X1	40 Pin Dip	80-675-10
R1,R2	Resistor, 470Ω, 1/4W, 5% Carb. Comp.	80-214-71
	SWITCHES	
S1	Space, Form A	80-932-10
S3-S14, S16-S94 S58-S69 Remove-02	Single, Form A	80-932-02
S2-S15	Shift & Lock	80-932-03

L.E.D. DISPLAY		ASSEMBLY 99-393-XXC
REF. DES.	DESCRIPTION	OMRON P/N
CR1, CR2,CR5-CR8	L.E.D. (Fairchild FLV 104)	80-400-01

MOTHER BOARD		ASSEMBLY 99-414-XXB
REF. DES.	DESCRIPTION	OMRON P/N
	CAPACITORS	
C1	220UF, 10WV,Tant	80-310-51
C2-C11	22UF, 15WV, Tant	80-311-53
REG J1-J4	PWB, Connector, 80 Pin	80-612-12

POWER SUPPLY ASSEMBLY		ASSEMBLY 07-041-01C
REF.DES.	DESCRIPTION	OMRON P/N
	CAPACITORS	
C1	40,000MFD, 20WVDC	80-305-23
C2,C3	3,900MFD, 35WVDC	80-300-67
C4	1,700MFD, 100WVDC	80-307-13
CR1,CR2	RECTIFIER ASSEMBLY	07-046-01
	TRANSFORMERS	
T1	Transformer	85-023-01
T2	Transformer	85-021-01

POWER SUPPLY ASSEMBLY		ASSEMBLY 07-041-02A
REF. DES.	DESCRIPTION	OMRON P/N
	CAPACITORS	
C1	40,000 µF, 20WVDC	80-305-23
C2,C3	3,900 µF, 35WVDC	80-300-67
C4	1,700 µF, 100WVDC	80-307-13
	TRANSFORMERS	
T1	Transformer	85-023-01
T2	Transformer	85-021-01
CR1,CR2	Rectifier, Center Tapped Bridge	80-412-11

PROCESSOR CARD		ASSEMBLY 99-369-01C
REF. DES.	DESCRIPTION	OMRON P/N
	CAPACITORS	
C2	10UF, 25V, 10%, Elect	80-305-21
C3	.001UF, 100V, Cer Disc	80-320-90
C4-C11,C13-C17	.01UF, 100V, Cer Disc	80-320-93
C12, C1	150MF, 10V, Tant	80-311-58
CR1-CR9	Diodes, IN914/IN4148	80-404-03
	INTEGRATED CIRCUITS	
XB4, XB6, XC5	7400N	80-460-22
XC3,XC4,XE3, XF3	7403N	80-460-59
XB5,XD6	7404N	80-460-18
XC6	7406N	80-460-73
XE6	7410N	80-460-19
XE4,XE5,XF1, XF2,XF4,XF5	7438N	80-461-22
XF6	7440N	80-460-42
XB2	74L42N	80-460-70
XA5,XA6	7474N	80-460-34
XD2,XD3,XD4,XD5	7475N	80-460-38
XA3,XA4	74107N	80-460-46
XC2	8008	80-460-90
XA2,XB3,XE1,XE2	8T380	80-461-07
	RESISTORS	
R23	270Ω ,5%,1/4W	80-212-71
R22	1K, 5%,1/4W	80-211-02
R1,R3-R21,R24	2.7K, 5%,1/4W	80-212-03
R2	10K, 5%, 1/4W	80-211-03
Q1,Q2	Transistor, 2N4403	80-423-02
XC2	I.C. Socket, 18 Pin Dip	80-675-09
	Ejector	40-109-07

PROM CARD		ASSEMBLY 99-434-01A
REF. DES.	DESCRIPTION	OMRON P/N
	CAPACITORS	
C1	150UF, 10V, Tant	80-311-058
C2 thru C14	.01U, 100V Cer. Disc	80-320-093
	INTEGRATED CIRCUITS	
XF5	7404	80-460-018
XE3,XF4	7407	80-461-036
XE6	7430	80-460-045
XE4,XE5	7442	80-460-031
XF3	Resistor Pak 2.2K	80-290-051
XA1 thru XA8 XB1 thru XB8 XC1 thru XC8 XD1 thru XD8 XF6	Socket (16 Pin Dip)	80-676-04

PROM CARD		ASSEMBLY 99-436-36A
REF. DES.	DESCRIPTION	OMRON P/N
	CAPACITORS	
C1	150UF, 10V Tant	80-311-058
C2 thru C14	.01U, 100V Cer. Disc	80-320-093
	INTEGRATED CIRCUITS	
XB1 L0000-0377	825126	22-011-59
XD1 H0000-0377	825126	22-011-60
XB2 L0400-0777	825126	22-011-61
XD2 H0400-0777	825126	22-011-62
XB3 L1000-1377	825126	22-011-63
XD3 H1000-1377	825126	22-011-64
XB4 L1400-1777	825126	22-011-65
XD4 H1400-1777	825126	22-011-66
XB5 L2000-2377	825126	22-011-67
XD5 H2000-2377	825126	22-011-68
XB6 L2400-2777	825126	22-011-69
XD6 H2400-2777	825126	22-011-70
XB7 L3000-3377	825126	22-011-71
XD7 H3000-3377	825126	22-011-72
XB8 L3400-3777	825126	22-011-73
XD8 H3400-3777	825126	22-011-74
XF5	7404	80-460-018
XE3,XF4	7407	80-461-036
XE6	7430	80-460-045
XE4,XE5	7442	80-460-031
	Buffered Prom Sub-Assy.	99-434-02
	Ejector	40-109-08
XF3	Resistor Pak 2.2K	80-290-051
XF6	Socket Adapter	80-625-03
XA1 thru XA8 XB1 thru XB8 XC1 thru XC8 XD1 thru XD8 XF6	Socket (16 Pin Dip)	80-676-04

RAM CARD		ASSEMBLY 99-445-XXB
REF. DES.	DESCRIPTION	OMRON P/N
	CAPACITORS	
C6	150UF, 10V Tant	80-311-058
C1-C5, C7-C38 C1-C5, C7-C22	.01UF,100V Cer. Disc	80-320-093
	INTEGRATED CIRCUITS	
XA1-XA8 XB1-XB8 XC1-XC8 XD1-XD8	2102-2	80-460-91
XE2, XF2	74H00	80-460-35
XE2, XF2	7438	80-461-22
XE5	7442	80-460-031
XF5	7404	80-460-018
XE6	7420	80-460-017
XF1, XF3, XE4	7407	80-461-036
	EJECTORS	
	Ejector	40-109-05
	Ejector	40-109-09
	Buffered Ram Sub-Assembly	99-433-01
XE3,XE1	Resistor Pak 2.2K	80-290-051
R1	Resistor 4.7K, 1/4W, 5%	80-214-72
A1 thru A8 B1 thru B8 C1 thru C8 D1 thru D8, F6	Socket (16 Pin Dip)	80-675-008
E2,F2	I.C. Socket, 14 Pin Dip	80-675-007
XF6	Socket Adapter	80-625-03

RAM CARD		ASSEMBLY 99-433-XXC
REF. DES.	DESCRIPTION	OMRON P/N
	CAPACITORS	
C6	150UF 10V TANT	80-311-058
C1-C5, C7-C38 C1-C5, C7-C22	.01UF 100V Cer. Disc.	80-320-093
	INTEGRATED CIRCUITS	
XE5	7442	80-460-031
XF5	7404	80-460-018
XE6	7420	80-460-017
XF1,XF3,XE4	7407	80-461-036
E2,F2	I.C. Socket, 14 Pin Dip	80-675-007
R1	Resistor, 4.7K, 1/4W, 5%	80-214-72
XE3, XE1	Resistor Pak 2.2K	80-290-051
A1 thru A8 B1 thru B8 C1 thru C8 D1 thru D8 F6	Socket (16 Pin Dip)	80-675-008
XF6	Socket Adaptor	80-625-03

REFRESH BUFFER CARD		ASSEMBLY 99-415-01D
REF. DES.	DESCRIPTION	OMRON P/N
	CAPACITORS	
C2-C8, C9, C10, C12	Cer., 0.01UF, 100V	80-320-93
C13	Elec., 10UF, 25V	80-305-21
C11	150UF, 10WV, Tant	80-311-58
	INTEGRATED CIRCUITS	
XB6, XE5	7404N	80-460-18
XA4,XB4,XC4	7438N	80-461-22
XD6	7427N	80-460-61
XD2,XD3,XE2,XE3	2532B	80-461-34
XE6	7430N	80-460-45
XB5,XD5	7400N	80-460-22
XD4,XE4	7402N	80-460-62
XA5	7410N	80-460-19
XC5	7474N	80-460-34
XA6	74107N	80-460-46
XB2,XB3,XC2,XC3	74175N	80-460-64
XA2	7442N	80-460-31
XA3	74161N	80-460-58
XB1,XC1	7406N	80-460-73
XC6,XD1,XE1	7408N	80-460-50
XC6	74H08	80-461-49
	RESISTORS	
R1-R12	100Ω, 1/4W, 5%	80-211-01
R13,14,15,16	1K, 1/4W,5%	80-211-02
	SOCKETS	
J1	14 Pin Dip	80-676-03
XE2,XD2	16 Pin Dip	80-676-01

REFRESH CONTROL CARD		ASSEMBLY 99-457-01B
REF. DES.	DESCRIPTION	OMRON P/N
	CAPACITORS	
C2-C6, C8-C12	.01UF, 100V., Cer. Disc.	80-320-93
C1	.10UF, 25V., 10% Elec.	80-305-21
C7	150MF, 15V, Tant	80-311-55
	INTEGRATED CIRCUITS	
XA3,XC2	7400N	80-460-22
XD3-XD6	7404N	80-460-18
XB3,XB4	7408N	80-460-50
XD1	7420N	80-460-17
XC1	7427N	80-460-61
XA2,XB5,XB6	7430N	80-460-45
XD2,XE3-XE6	7438N	80-461-22
XA4	74107N	80-460-46
XB1,XB2	74161N	80-460-58
XC3-XC6	74163N	80-460-79
XE1,XE2	7414N	80-461-45
	Card Ejector	40-109-06
R1,R4	Resistor, 1K,5%, 1/4W	80-211-02

REGULATOR CARD		ASSEMBLY 99-402-01B
REF.DES.	DESCRIPTION	OMRON P/N
	CAPACITORS	
C5	150MF, 15 VDC Tant	80-311-55
C6,C7,C8	1.0MF, 50 VDC, Cer.	80-319-06
C9,C10,C11	10MF, 15 VDC, Tant	80-311-56
C12	0.1UF,20%, Cer. Disc.	80-319-01
	RESISTORS	
R1	Fixed, WW, 2Ω,8W,±5%	80-258-03
R2	Fixed, WW, 3.9Ω,1W,5%	80-251-18
R3	Fixed, 1K, 1/4W, 5%	80-211,02
R5	470Ω,5%, 1/4W	80-214-71
	REGULATORS	
Z1	7805CP	80-464-02
Z3	7812CP	80-464-03
Z2	7906CP	80-464-05
CR1	Diode Zener	80-403-08
R4	Pot, Trim, 100Ω	80-270-15
	Card Ejector	40-109-10

RS232 INTERFACE CARD		ASSEMBLY 99-451-001A
REF. DES.	DESCRIPTION	OMRON P/N
	CAPACITORS	
C5-C10,C12-C14 C23,C24	.01UF,100V, Cer. Disc.	80-320-093
C11	.001UF,500V, Cer. Disc.	80-320-090
C4	300PF,1KV, Cer. Disc.	80-319-016
C21,C22,C16	400PF,1KV, Cer. Disc.	80-319-003
C17-C20	500PF,1KV, Cer. Disc.	80-319-002
C1-C3,C25	150UF,15V, Tant, Dip	80-311-055
C15	39UF,10V, Tant	80-302-008
	INTEGRATED CIRCUITS	
XB1,XD4	7404	80-460-018
XB3,XB4	74161	80-460-058
XB5	1489	80-460-084
XB6	1488	80-460-083
XC1,XC4,XF4	7400	80-460-022
XC3	7402	80-460-062
XC5	7432	80-461-054
XD2,XE1,XE2 XF1,XG1	7403	80-460-059
XD3	9386	80-460-088
XD6	74123	80-460-052
XE4	7442	80-460-031
XE5	9314	80-461-029
XE6,XF5,XG6	7408	80-460-050
XF6,XG5	74107	80-460-046
XG2	74175	80-460-064
XG3	TRI602A	80-460-098
XG4	7407	80-461-036
XC6	7410	80-460-019

RS232 INTERFACE CARD		ASSEMBLY 99-451-001A
REF. DES.	DESCRIPTION	OMRON P/N
	RESISTORS	
R1	Fixed, 10K, 1/4W, ±5%	80-211-003
R2	Fixed, 270Ω,1/4W, ±5%	80-212-071
R3,R5	Fixed, 330Ω,1/4W, ±5%	80-213-031
R4	Fixed,220Ω, 1/4W, ±5%	80-212-021
R6	Fixed,22K, 1/4W,±5%	80-212-023
	SOCKETS	
(REF G3)	40 Pin Dip	80-675-010
(REF J20(A6))	14 Pin Dip	80-676-003
(REF J21(A5))	16 Pin Dip	80-676-004
(REF A2)	16 Pin Dip	80-676-001
	Card Ejector	40-109-009
CR1,CR2	Diode, IN914/IN4148	80-404-003
XB2,XC2	Resistor Pack, 2.2K (760-1)	80-290-051

TERMINATOR CARD		ASSEMBLY 99-394-01B
REF. DES.	DESCRIPTION	OMRON P/N
	CAPACITORS	
C1,C2	150UF,10WV, Tant	80-311-58
C3-C6	.01UF,100V, 10%, Cer. Disc	80-320-93
	RESISTOR PACK	
X1-X4	(898-1-R330) 330Ω	80-290-53
X5	(893-3-R470) 470Ω	80-290-54

TIMING CONTROL CARD		ASSEMBLY 99-452-01C
REF. DES.	DESCRIPTION	OMRON P/N
	CAPACITORS	
C3	150MF, 15V, Tant	80-311-55
C1	33PF, 100V, Silver Mica	80-320-87
C14	39UF, 10V, Tant	80-302-08
C2	1UF, 50V, Disc. Cer.	80-319-01
C4-C12,C15	.01UF, 100V, Disc. Cer.	80-320-93
	INTEGRATED CIRCUITS	
XE2	7400	80-460-22
XB1,XC6	74H00	80-460-35
XE1	7402	80-460-62
XB4,XF1, XF3, XF6, XD4	7404	80-460-18
XC5, XF4	7406	80-460-73
XD1, XE5, XF2	7410	80-460-19
XD3	7420	80-460-17
XE4	7442	80-460-31
XC3	7474	80-460-34
XA1	74H74	80-460-77
XC2,XD6	7492	80-461-15
XF5	74L02	80-460-67
XB5, XC4	74107	80-460-46
XA6	74121	80-460-94
XB3,XD5	74160	80-460-76
XC1,XD1,XE6, XB2	74161	80-460-58
XE3	74175	80-460-64
	RESISTORS	
R3	270Ω,5% 1/4W	80-212-71
R4-R10,R12-R18	2.7K,5% 1/4W	80-212-72
R11	4.7K,5% 1/4W	80-214-72
R2	10K,5% 1/4W	80-211-03
R1	15K,5% 1/4W	80-211-53

TIMING CONTROL CARD		ASSEMBLY 99-452-01C
REF. DES.	DESCRIPTION	OMRON P/N
Y1	Crystal, 29.952 MHZ	80-967-93
CR1	Diode, IN914	80-404-03
	Ejector	40-109-04
L1	Inductor, 2.2UH	80-501-40
Q1,Q2	Transistor, 2N3904	80-422-11

VIDEO CONTROL CARD		ASSEMBLY 99-454-01A
REF. DES.	DESCRIPTION	OMRON P/N
	CAPACITORS	
C4-C15	.01MF,100V,10%, Cer. Disc.	80-320-93
C1-C3	150MF, 15V, Tant	80-311-55
	CHARACTER GENERAL	
A2,A4	ROM Lower Case	22-003-035
A2	Upper Case (PROM)	22-012-07
	DIODES	
CR4	IN752A	80-404-12
CR3	IN914/IN4148	80-404-03
	INTEGRATED CIRCUITS	
XD3,XD5,XE6	7400N	80-460-22
XE3	7402N	80-460-62
XD1,XE1	7403N	80-460-59
XB6,XD2,XE5	7404N	80-460-18
XC3	7410N	80-460-19
XD4	7420N	80-460-17
XC5,XC6	7427N	80-460-61
XE4	74H74N	80-460-77
XE2	7486N	80-460-54
XB2	74166N	80-460-63
XC4,XD6	74175N	80-460-64
XC2	74H00N	80-460-35
XB4,XB5	7408N	80-460-50
XB3	7432N	80-461-54

VIDEO CONTROL CARD		ASSEMBLY 99-454-01A
REF. DES.	DESCRIPTION	OMRON P/N
	RESISTORS	
R16	10Ω,1/4W,5%	80-211-00
R18	270Ω,1/4W, 5%	80-212-71
R17	330Ω,1/4W, 5%	80-213-02
R35,R36	1KΩ,1/4W, 5%	80-211-02
R13,R19	560Ω,1/4W, 5%	80-215-61
R34	2.7K,1/4W, 5%	80-212-72
R20	1.5K,1/4W, 5%	80-211-52
	Ejector	40-103-02
XA1	Resistor Pack, 1K,760-1-1K-13	80-290-60
J22	Socket, (16 Pin Dip)	80-676-04
	Socket, 24 Pin Dip	80-675-11
Q3	Transistor 2N4401	80-419-01

10.1 EIA STANDARD RS-232C

The EIA standard RS-232C* ensures equipment compatability and interchangeability between vendors by defining the electrical and mechanical interface between the modem and the data terminal. Specifically, the standard sets the minimum voltage (5 volts) and the maximum (15 volts) that can be present at the interface. It also establishes the "handshaking" routine and timing.

Table 10-1 shows the relationship between pin numbers, direction of signal flow, RS-232C nomenclature, and Bell Telephone nomenclature.

Circuit descriptions for the RS-232C nomenclature in Table 10-1 follow.

10.1.1 Transmit Data (BA), Pin 2

Data from the terminal is transmitted to the remote end. Line is held at a "mark" (negative voltage) between characters.

10.1.2 Receive Data (BB), Pin 3

Data from the remote end comes through the modem to the terminal. Line is held at a mark between characters.

10.1.3 Request to Send (CA), Pin 4

A signal from the terminal tells the modem that it wants to transmit data. This signal allows the modem to prepare for data transmission by turning on the carrier, if necessary, allowing the carrier to stabilize, and permitting the remote carrier to synchronize.

10.1.4 Clear to Send (CB), Pin 5

A signal from the modem in response to CA indicates that it is ready to receive data. Various CB delays and options are available to permit the modem to perform different functions.

10.1.5 Data Set Ready (CC), Pin 6

Interlock to terminal indicates that the modem is in an operational state. The terminal should never try to pass data if this signal is absent.

10.1.6 Received Line Signal Detector (CF), Pin 8

This signal indicates that the local modem is receiving a carrier from the remote modem. The terminal should not read Receive Data line unless CF is present.

10.1.7 Data Terminal Ready (CD), Pin 20

A signal from the terminal activates the modem. It is generally impossible to pass data in either direction without this signal.

* "Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange"

10.1.8 Ring Indicator (CE), Pin 22

This signal is used in conjunction with auto-answer options. The local modem uses it to indicate that a ringing signal was received from the remote modem. This line may be used with special purpose peripherals for other purposes.

Table 10-1. RS-232C pin number-signal flow-nomenclature relationship

SIGNAL FLOW	PIN NO.	RS-232C NOMENCLATURE	BELL TELEPHONE NOMENCLATURE
MODEM or DAA* ← TERMINAL	1	(AA) Protective Ground	(FG) Frame Ground
MODEM or DAA* ← TERMINAL	2	(BA) Transmit Data	(SD) Send Data
MODEM or DAA* → TERMINAL	3	(BB) Receive Data	(RD) Receive Data
MODEM or DAA* ← TERMINAL	4	(CA) Request to Send	(SR) Send Request
MODEM or DAA* → TERMINAL	5	(CB) Clear to Send	(CS) Clear to Send
MODEM or DAA* → TERMINAL	6	(CC) Data Set Ready	(IT) Interlock
	7	(AB) Signal Ground	(SG) Signal Ground
MODEM or DAA* → TERMINAL	8	(CF) Received Line Signal Detector	(CO) Carrier On
MODEM or DAA* → TERMINAL	9	Reserved--Modem Testing	(+12V) Positive Battery
MODEM or DAA* → TERMINAL	10	Reserved--Modem Testing	(-12V) Negative Battery
	11	Unassigned	Not Used
MODEM or DAA* → TERMINAL	12	(SCF) Secondary Receive Line Signal Detect	Not Used
MODEM or DAA* → TERMINAL	13	(SCB) Secondary Clear to Send	Not Used
MODEM or DAA* ← TERMINAL	14	(SBA) Secondary Transmit Data	(NS) New Sync
MODEM or DAA* → TERMINAL	15	(DB) Transmitter Signal Element Timing	(SCT) Serial Clock Transmitter
MODEM or DAA* → TERMINAL	16	(SBB) *Secondary Receive Data	(DCT) Debit Clock Transmitter
MODEM or DAA* → TERMINAL	17	(DD) Receiver Signal Element Timing	(SCR) Serial Clock Receiver
	18	Unassigned	(DCR) Debit Clock Receiver
MODEM or DAA* ← TERMINAL	19	(SCA) Secondary Request to Send	(RR) Remote Release
MODEM or DAA* ← TERMINAL	20	(CD) Data Terminal Ready	(RC) Remote Control
MODEM or DAA* → TERMINAL	21	(CG) Signal Quality Detector	(RDY) Ready
MODEM or DAA* → TERMINAL	22	(CE) Ring Indicator	(RG1) Ring Indicator
MODEM or DAA* → TERMINAL	23	(CH/CI) Data Signal Rate Selector	(RG2) Ring Indicator
MODEM or DAA* ← TERMINAL	24	(DA) Transmitter Signal Element Timing	(SCTE) Serial Clock Transmitter External
	25	Unassigned	Not Used

*Data Access Arrangement (Bell Telephone)

10.2 ISO CHARACTER ASSIGNMENTS

This paragraph provides ISO (International Standard Organization) code and character assignments for information interchange. Contained within the ISO code are the ASCII (American Standard Code for Information Interchange) character assignments.

10.2.1 Mnemonics and Their Definitions

Table 10-2 defines the mnemonics used in conjunction with the ISO and ASCII codes.

Table 10-2. ISO/ASCII mnemonics and their definitions

3-CHARACTER CONTROL 7-BIT CODE	ALTERNATE 2-CHARACTER MNEMONIC	ANSI MNEMONIC 8-BIT CODE	ECMA MNEMONIC-IF DIFFERENT	DEFINITION
ACK	(AK)			Acknowledge
BEL	(BL)			Bell
BS				Backspace
CAN	(CN)			Cancel
		CD	DCL	Character Delete
		CI	ICL	Character Insert
		CIF		Character Insert Off
		CIN		Character Insert On
		CLC	EEL	Clear Line from Cursor
CR				Carriage Return
		CSC	EED	Clear Screen from Cursor
DC1	(D1)			Device Control 1
DC2	(D2)			Device Control 2
DC3	(D3)			Device Control 3
DC4	(D4)			Device Control 4
DEL	(DT)			Delete
DLE	(DL)			Data Link Escape
EM				End of Medium
ENQ	(EQ)			Enquiry
		EO		Eight Ones
EOT	(ET)			End of Transmission
ESC	(EC)			Escape
		ESI		Extended Shift In
		ESO		Extended Shift Out
ETB	(EB)			End of Transmission Block
ETX	(EX)			End of Text
FF				Form Feed
FS				File Separator
GS				Group Separator
		HF	RPM	Highlight Off
		HLF	FHL	Half Line Feed
		HLR	RHL	Half Line Reverse Feed
		HN	APM	Highlight On
HT				Horizontal Tab
		HTC		Horizontal Tab Clear
		HTS		Horizontal Tab Set
		LCF		Local Copy Off-full duplex
		LCN		Local Copy On-half duplex

Table 10-2. ISO/ASCII mnemonics and their definitions (cont'd)

3-CHARACTER CONTROL 7-BIT CODE	ALTERNATE 2-CHARACTER MNEMONIC	ANSI MNEMONIC 8-BIT CODE	ECMA MNEMONIC-IF DIFFERENT	DEFINITION
		LD	DL	Line Delete
LF				Line Feed
		LI	IL	Line Insert
NAK	(NK)			Negative Acknowledge
		NP		Next Page
NUL	(NU)			Null
		PD	CUD	Cursor (Pointer) Down
		PFF		Protect Format Off
		PFN		Protect Format On
		PH	CUH	Cursor (Pointer) Home
		PL	CUB	Cursor (Pointer) Left
		PM		Cursor (Pointer) Return
		PP		Previous Page
		PR	CUF	Cursor (Pointer) Right
		PT		Cursor (Pointer) Tab
		PU	CUU	Cursor (Pointer) Up
		RLF		Reverse Line Feed
RS				Record Separator
		SD		Scroll Down
SI				Shift In
SO				Shift Out
SOH	(SH)			Start of Heading
SP				Space (a blank)
STX	(SX)			Start of Text
		SU		Scroll Up
SUB	(SB)			Substitute
SYN	(SY)			Synchronous Idle
US				Unit Separator
VT				Vertical Tab
		VTC		Vertical Tab Clear
		VTS		Vertical Tab Set

10.2.2 The ASCII Code

Table 10-3 defines the ISO code that incorporates the ASCII code. Columns 2 through 5 define the ASCII 64-character set, 2 through 7 the ASCII 96-character set, and 2 through 9 the ASCII 128-character set.

10.2.3 Tape Track Assignments

Track Assignments for 25.40 mm (1 inch) punched paper tape and 12.70 mm (0.5 inch magnetic tape as related to serial transmission of the ISO and ASCII codes as shown in Figure 10-1.

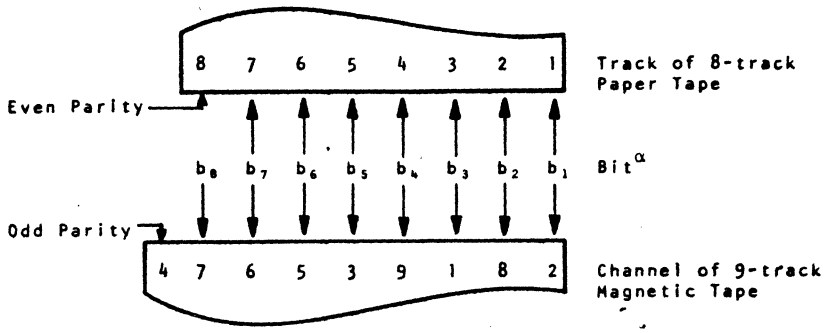


Figure 10-1. Tape track assignments for ISO/ASCII codes.

Notes for Table 10-3.

1. Columns 2 through 7 - These 12 positions are variable--2 for currency, 7 for primary national usage, and 3 for secondary usage which are diacritical marks used for alphabetical extension when preceded by BS. Positions 2/7 and 2/12 are invariant but also serve as diacritical marks. Presently known assignments are given in Table E-3, Page E-7.

2. Columns 2 through 5 - Define the ASCII 64-Character set.

3. Columns 2 through 7 - Define the ASCII 96-character set.

4. Columns 2 through 9 - Define the ASCII 128-character set.

5. Columns 4 and 5 - (ESC.) (CHAR.)

6. Columns 4 through 9 - Soft Copy Controls.

7. Columns 8 and 9 - (SINGLE CHAR.)

8. Columns 8 through 15 - JSCII (Japanese Industrial Standard Code for Information Interchange) is an 8-bit code consisting of the ISO characters plus the Kata Kana characters shown in upper row positions of Columns 10-13. (Columns 8 and 9 are reserved for additional controls, and 14 and 15 for additional graphics.)

   GOST 13052.67 defines the USSR set shown in lower row entry positions of Columns 12-15. The standard defines these characters for Columns 4-7 of a 7-bit set

(SO = Russian register, SI = Latin register). Columns 8-11 are identical to 0-3.

9. Columns 3 through 7 - Alternate controls in these 5 columns are achieved by preceding a regular character with an ESCape.

10. Hollerith card code for 256 characters [8 x 32 (2^5) = 256] is constructed

12		1 or 2 or 3 ... or 7 or blank (no punch).
11	8	and any combination of 12, 11, 0, 8 and 9 (from none to all).
0	9	

For historical reasons, assignments present little in the way of a regular pattern, but they are the key for translation to and from IBM EBCDIC.

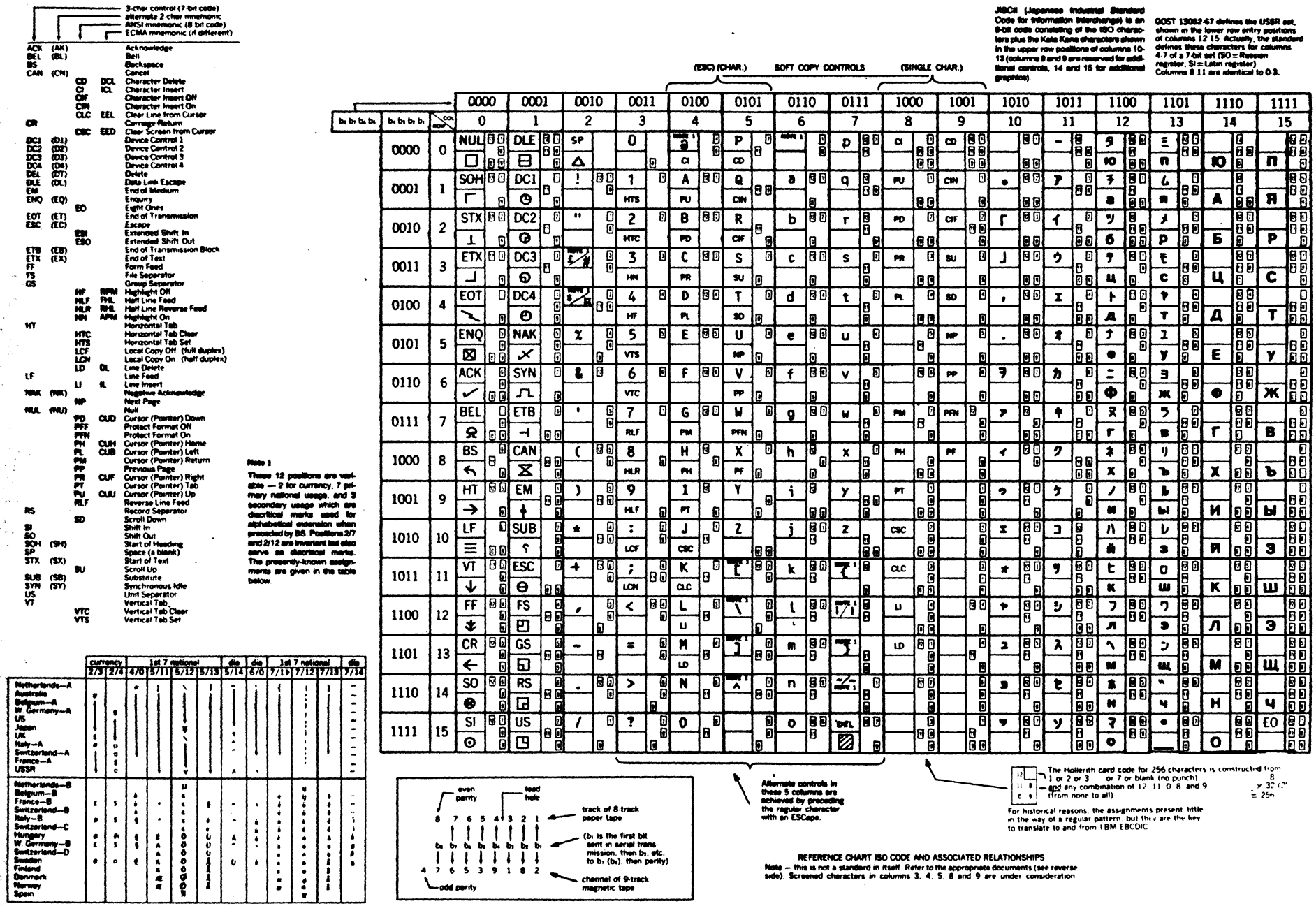


Table 10-3. ISO Code

LIST OF ABBREVIATIONS

ABBREVIATION	DEFINITION
ac	alternating current
ASCII	American Standard Code for Information Interchange
ASR	automatic send and receive
BA	transmitted data
BB	received data
°C	degrees Centigrade or Celsius
CA	request to send
CB	clear to send
CD	data terminal ready
CE	ring indicator
CF	received line signal detector
cm	centimeter
CPU	central processing unit
CRT	cathode ray tube
dc	direct current
DHEW	Department of Health, Education and Welfare
e.g.	for example
EIA	Electronic Industries Association
FL	foot-lamberts
GND	ground
H (dimensions)	height
H (logic level)	logic 1
H.V.	high voltage
Hz	Hertz
IC	integrated circuit

LIST OF ABBREVIATIONS

ABBREVIATION	DEFINITION
I/O	input/output
ISO	International Standards Organization
KB	keyboard
k or kilo	10^3
KSR	keyed send and receive, character-by-character
L (logic level)	logic 0
lb	pound
LED	light emitting diode
M or mega	10^6
m or milli	10^{-3}
micro or μ	10^{-6}
MOS	metal-oxide semiconductor
NEMA	National Electrical Manufacturers Association
n or nano	10^{-9}
ϕ	phase
pps	pulses per second
PROM	programmed read only memory
QWERTY	standard typewriter keyboard arrangement
RAM	random access memory
REG	regulated
ROM	read only memory
sec	second
sync	synchronization
TTY	teletypewriter
u or μ (micro)	10^{-6}

LIST OF ABBREVIATIONS

ABBREVIATION	DEFINITION
V	volts
W (dimensions)	width

GLOSSARY

A data bus: Bus lines over which data is entered into the terminal CPU.

Address: Binary number on the MA Data Bus that specifies a card or location in memory.

AND gate: Gate that has a high output when all inputs are high.

Auxiliary storage: External memory device that stores data.

B data bus: Bus lines over which data from the terminal CPU is transmitted.

Baud: Unit of signaling speed indicating the number of signal elements that can be transmitted per second.

Bench maintenance: Maintenance performed to correct malfunctions by replacing circuit components in modules or on circuit cards.

Bit: Smallest unit of information in binary notation.

Byte: Measurable portion of consecutive binary digits, usually operated on as a unit.

Cathode ray tube: Electron tube, like a T.V. picture tube, used for visual display.

CG data channel: Channel for supplying refresh data to the video control card.

Character generator: Memory device that stores the video dot pattern for character generation on the CRT display.

Character period: Time (670 nsec) needed for one dot line in a character.

Clear memory: Instruction to erase data in RAM memory.

CRT display: Device that visually displays data.

CS data channel: Channel over which video status data is supplied to the video control card.

Cursor: Visual indicator on the display that indicates where the next character is to appear.

Dot: One element in the matrix used to display a character.

Dot line: One horizontal line of 10 dots in the character matrix.

Display page: 12 or 24 consecutive lines of displayed data.

Exclusive OR gate: Gate that has a high output when either input, but not both, is high.

Exclusive NOR gate: Gate that has a low output when either input, but not both, is high.

GLOSSARY

Field maintenance: Maintenance performed to correct malfunctions by replacing readily changed parts, modules, or circuit cards.

Full-duplex: Two-way simultaneous communications.

Half-duplex: Alternate, one-way-at-a-time, independent transmission.

Header: IC socket plug to which jumper wires can be added to change circuitry on a circuit card.

High: Logic 1.

KB data channel: Channel on which data leaves the keyboard.

LED data channel: Channel for supplying on/off instructions to the keyboard LED indicators.

Line: Horizontal line of characters on the display screen.

Low: Logic 0.

MA data bus: Bus lines over which addressing is done in the terminal.

Memory: Device that temporarily or permanently stores information.

Memory seam: Highest available address in memory.

Modem: Device that modulates and demodulates signals transmitted over communications facilities.

Monitor: Same as CRT display.

NAND gate: Gate that has a low output when all inputs are high.

NOR gate: Gate that has a low output when at least one input is high.

OR gate: Gate that has a high output when at least one input is high.

Page base: Defines the memory location of the character displayed in the uppermost left character position on the CRT display.

Preventive maintenance: Maintenance performed to correct abnormal conditions before they develop into malfunctions.

Printer: External device that supplies hard copy of data.

Program memory: Memory that stores the instructions needed by a CPU to perform its functions.

Programmed read only memory (PROM): Read only memory that can be programmed by the equipment manufacturer rather than by the memory manufacturer.

GLOSSARY

Random access memory (RAM): Temporary memory that data can be written into and read out of.

Raster: Illuminated area on a CRT.

RD data channel: Channel on which data enters the refresh memory.

Read only memory (ROM): Permanent memory in which stored data can only be read.

Refresh memory: Memory that stores information for use by a CRT display or other read devices.

RM data channel: Channel on which data leaves the refresh memory.

Screen: Face of the CRT used in a CRT display.

Video modification: Change to the "normal" presentation on the CRT display.