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TECHNICAL MANUAL

MAGNETIC TAPE SYSTEM

MODEL 7371/7372/7374

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LIST OF RELATED PUBLICATIONS

The following publications contain information not included in this manual, but necessary for a complete understanding of the Magnetic Tape System Model 7371/7372/7374.

Publication Title	Publication No.
Power Supply Model PT16 Technical Manual	901080
Power Supply Model PT18 Technical Manual	900866
Power Supply Model PT19 Technical Manual	900867
Peripheral Equipment Tester Model 7901 Technical Manual	901004
Sigma Computer Systems Interface Design Manual	900973
SDS Sigma 2 Computer Reference Manual	900964
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SDS Sigma 7 Computer Technical Manual	901060
Sigma 5 and 7 Magnetic Tape Test (7-Channel) Diagnostic Program Manual	901165
Sigma 2 Magnetic Tape Test (7-Channel) Diagnostic Program Manual	901536
7-Track Magnetic Tape Systems Models 7361/7362/7371/7372 Reference Manual for SDS Sigma Computers	900978
Diagnostic Control Program for Sigma 5 and Sigma 7 Computer Peripheral Devices Reference Manual	900712

SECTION I
GENERAL DESCRIPTION

1-1 INTRODUCTION

1-2 SCOPE OF MANUAL

This publication describes the Magnetic Tape System Model 7371/7372/7374 (figures 1-1 and 1-2), designed and manufactured by Scientific Data Systems for use with Sigma-series computers.

1-3 RELATED PUBLICATIONS

The publications listed in the front matter contain information necessary for a complete understanding of the magnetic tape system.

1-4 PURPOSE AND BRIEF DESCRIPTION

The magnetic tape system provides medium-speed (75 ips) input/output facilities for SDS Sigma-series computers. It may be used for program storage, as inputs to sorts and merges, for large data processing files, or as scratch or working tapes. Data is written and read in IBM-compatible tape format. The magnetic tape system records data on and reads data from standard 1/2-inch, seven-channel magnetic tape having a recording density of 200, 556, or 800 bits per inch. Binary and decimal (BCD) are the two standard read and write modes of operation for the model 7371/7372; packed binary reading and writing is an optional feature (model 7374).

The basic magnetic tape system is made up of the Magnetic Tape Controller Model 7371 and the Magnetic Tape Station Model 7372. A more extensive system may be formed by interconnecting up to eight magnetic tape stations, with complete control of the system originating from the magnetic tape station that contains the magnetic tape controller. In this manual, the 7371 magnetic tape controller will be referred to as "the magnetic tape controller" or "the controller"; the 7372 magnetic tape station will be identified as "the magnetic tape station" or "the station."

1-5 PHYSICAL DESCRIPTION

1-6 GENERAL

The basic magnetic tape system is contained in a standard Sigma cabinet 63-1/2 inches high, 29-1/4 inches wide, and 35 inches deep, having front and rear access. The tape transport mechanism is mounted at the front of the cabinet. Access to the tape handling portion is provided through a sliding glass door. A swing frame at the rear of the cabinet holds the two chassis of station electronics (S and U) and the four additional chassis (V, W, Y, and Z) that comprise the magnetic tape controller. (See figures 1-1 and 1-2.)

When more than one station is used in the system, they are bolted together, side by side, and side panels are provided for the two outside ends only. The station containing the controller is located nearest the center of the system. The weight of a magnetic station alone is approximately 850 pounds; the weight of the basic system (magnetic tape station with controller) is approximately 950 pounds.

1-7 MAGNETIC TAPE STATION (See figures 1-1, 1-2, and 3-6)

The station consists of the main components described in paragraphs 1-8 through 1-17.

1-8 Transport Assembly

The transport assembly is mounted on the top front portion of the station. It includes the following:

a. Main transport casting on which the transport components are mounted (figure 1-2)

b. Reel hub assemblies, reel motors, and reel tachometers (figure 3-6)

c. Tape drive capstan, capstan motor, and tachometer (figure 1-1)

d. Read/write head assembly (includes tape cleaner) (figure 1-1)

e. Tape guides (figure 4-11)

f. Photosense assembly (figure 4-11)

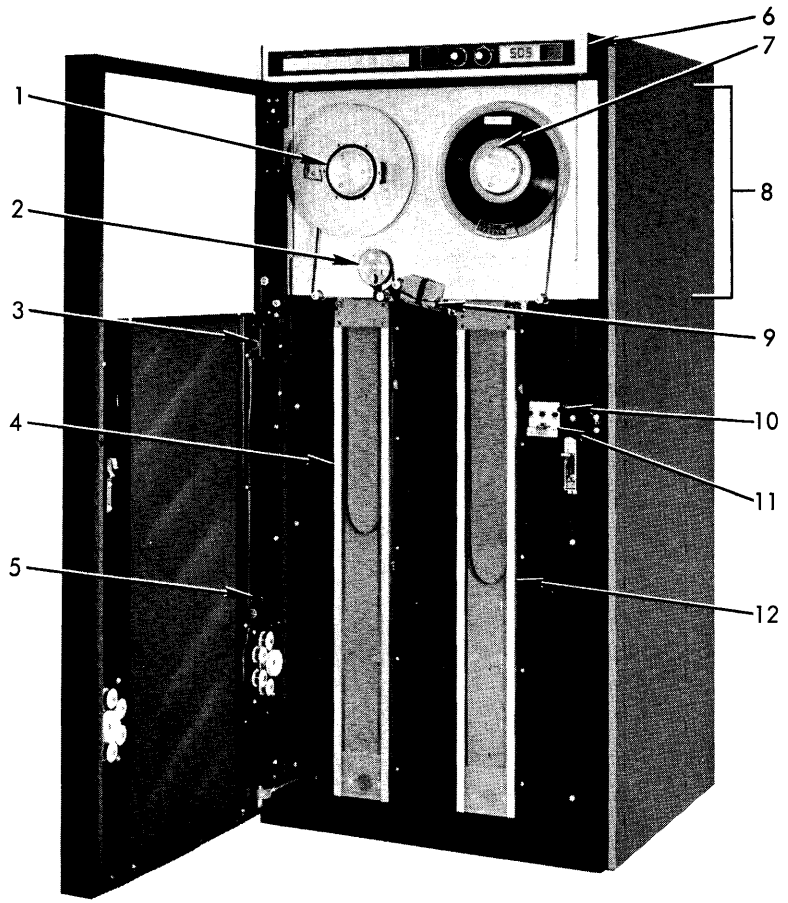
g. Write enable switch (figure 1-2)

h. Magnetic head cover actuator (figure 1-2)

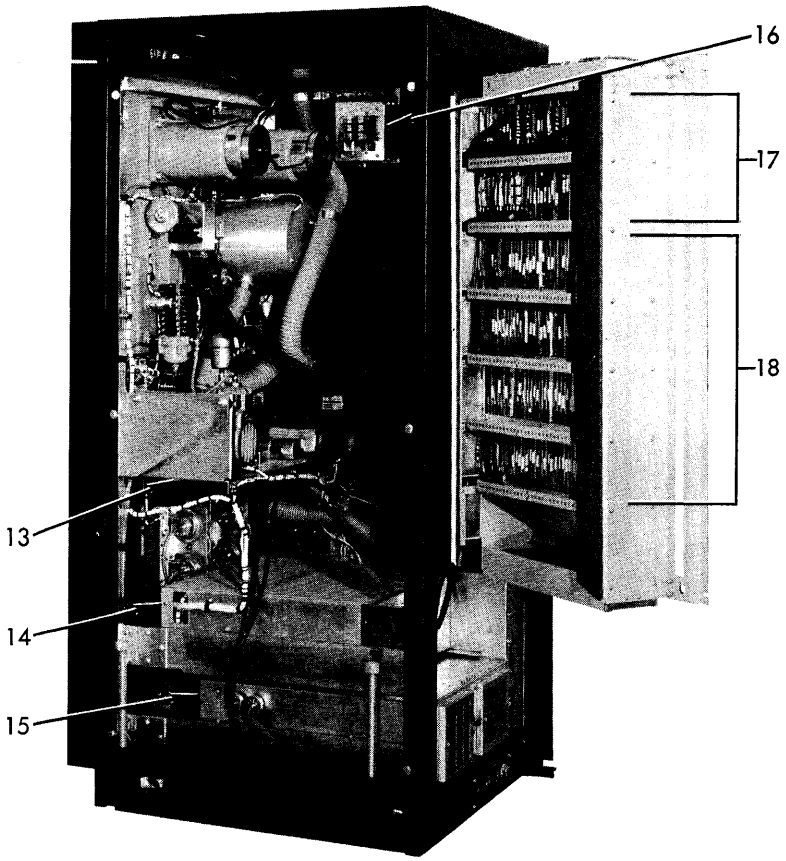
i. Positive pressure switch (figure 3-10)

j. Swinging door interlock switch (figure 1-1)

k. Auxiliary control panel (figure 1-1)



FRONT VIEW



SIDE VIEW

1. FIXED REEL HUB
2. CAPSTAN AND TACHOMETER
3. TOP DOOR SWITCH
4. FIXED TAPE STORAGE VACUUM CHAMBER
5. BOTTOM DOOR SWITCH
6. OPERATOR CONTROL PANEL
7. FILE REEL HUB
8. STATION TRANSPORT
9. READ/WRITE HEAD ASSEMBLY
10. SWINGING DOOR INTERLOCK
11. AUXILLARY CONTROL PANEL
12. FILE TAPE STORAGE VACUUM CHAMBER
13. BLOWER SHELF
14. TRANSPORT DRIVE ELECTRONICS
15. POWER SUPPLY PT19
16. RELAY CHASSIS
17. STATION ELECTRONICS
18. CONTROLLER MODEL 7371

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Figure 1-1. Magnetic Tape System Model 7371/7372/7374, Front and Side Views

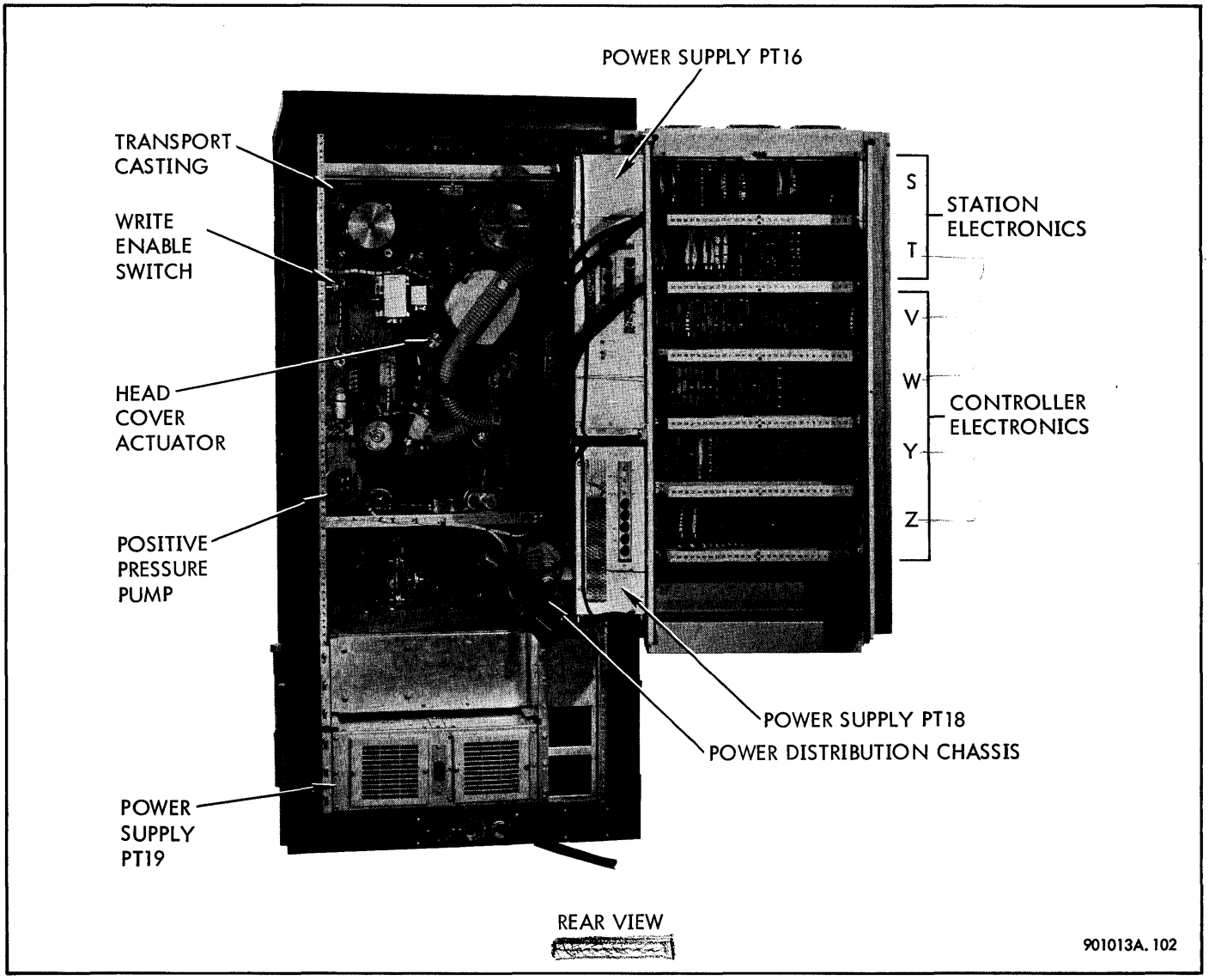


Figure 1-2. Magnetic Tape System Model 7371/7372/7374, Rear View

1-9 Operator Control Panel (Figure 1-1)

The operator control panel is mounted on the front of the station above the station transport main casting. The panel consists of switches for operating the station and lamp indicators for displaying the current status and condition of the station. It provides the necessary control signals for address selection, loading, unloading, and rewinding, as well as the signals needed for switching the station on-line or off-line.

1-10 Vacuum System

The vacuum system includes the following:

a. Vacuum blower (figure 3-6)

b. Tape storage chambers (figure 1-1)

c. Vacuum switches (Figure 3-6)

d. Vacuum plenum (located at bottom front of station)

1-11 Positive Pressure System (Figure 1-2)

Positive air pressure is generated by the positive pressure pump and is fed to the air plenum in the main casting. The plenum supplies air to the tape guides and operating pressure for the head door actuator and positive pressure interlock.

1-12 Blower Shelf Assembly (Figure 1-1)

The blower shelf assembly is mounted at the front center portion of the station behind the tape vacuum chambers. Mounted on the blower shelf assembly are the positive pressure pump and the vacuum blower.

1-13 Relay Chassis Assembly (Figures 1-1 and 4-25)

The relay chassis assembly is mounted at the top left center side of the main frame. It contains the ac interlock, ready, speed, rewind, dc interlock, and file protect relays.

1-14 Power Supplies (Figure 1-1)

There are three power supplies: PT19, PT18, and PT16. Power supply PT19 is located at the bottom rear of the station. It generates the 2000 Hz power that is used as input for both the PT16 and PT18 supplies. The PT18 supply is mounted on the bottom left-hand side of the swinging frame assembly. This supply generates +25 Vdc and -25 Vdc voltages. The PT16 supply is mounted at the top left-hand side of the swinging frame assembly. This supply generates +4 Vdc, +8 Vdc, and -8 Vdc voltages.

1-15 Power Distribution Chassis (Figure 1-2)

The power distribution chassis is mounted near the bottom front left-hand corner of the station. It provides necessary ac power controls to properly operate the station and devices connected in the system.

1-16 Transport Drive Electronics (Figure 1-2)

The transport drive electronics contains power supplies and power amplifiers for driving the capstan motor and the reel motor. It is contained in one assembly mounted near the bottom rear of the station cabinet, behind the tape vacuum chamber and below the motors.

1-17 Station Electronics (Figure 1-2)

The station electronics are mounted in module chassis S and U on the swinging frame assembly. Chassis S includes the modules that contain circuitry to handle the station data operations. Chassis U includes the modules that contain circuitry for control of the station motion operations.

1-18 MAGNETIC TAPE CONTROLLER (Figure 1-2)

The controller is comprised of module chassis V, W, Y, and Z. Chassis V and W enclose the modules which contain circuitry for handling the system data operations. The modules which contain circuitry for control of the system motion operations are included in chassis Y and Z.

1-19 FUNCTIONAL DESCRIPTION

The magnetic tape system communicates with the computer through the input/output processor (IOP), which controls tape system operation. It may store data on the magnetic tape (write operation) or retrieve it (read operation). The information is recorded on seven parallel tracks along the length of the tape at a selectable density of 200, 556, or 800 bytes per inch. Each byte consists of seven bits (six data bits plus one parity bit), which form a row across the width of the tape. (See figure 1-4.) The bits are formed by the nonreturn to zero, change on ones recording method (NRZ1). In this method, the write head current causes the state of flux in the tape to be switched from one level of saturation to the opposite level each time a binary one is recorded. The absence of such a change represents a binary zero.

1-20 MAGNETIC TAPE STATION

The tape transport moves the tape across a read/write head in response to commands from the computer or signals generated from the operator control panel. In a write operation, the data electronics translates the information from the tape controller and drives the write head to record the data on the tape. In a read operation, the information detected by the read head is amplified and then transferred to the controller.

1-21 MAGNETIC TAPE CONTROLLER

In automatic operation, all operating commands and read/write data transfers for the tape station are handled by the magnetic tape controller. Data to be recorded is received from the computer through the IOP and is routed to the magnetic tape controller and then to the selected tape station. The data flow follows a reverse sequence during a read operation. Refer to figure 1-3 for an overall functional block diagram of the magnetic tape system.

1-22 TAPE FORMAT

The tape data format conforms to IBM 729, seven-track format (see figure 1-4). Information on tape is arranged in records. Each record may contain any number of bytes, limited only by the length of the usable portion of tape.

Records are separated on tape by an interrecord gap of approximately 0.750 inches. When a write operation is initiated from the load point, a gap of approximately 0.94 inches in length is automatically inserted between the beginning of tape (BOT) marker and the first record. At the end of each record three blank characters are written, followed by a longitudinal redundancy check character mark (LRC). A group of one or more consecutive records forms a file of information. Adjacent files are separated by a tape mark record, which consists of a single byte. An LRC character occurs three spaces after the tape mark.

1-23 SPECIFICATIONS AND LEADING PARTICULARS

1-24 GENERAL REQUIREMENTS

Tables 1-1 and 1-2 list the general requirements and specifications for the magnetic tape system.

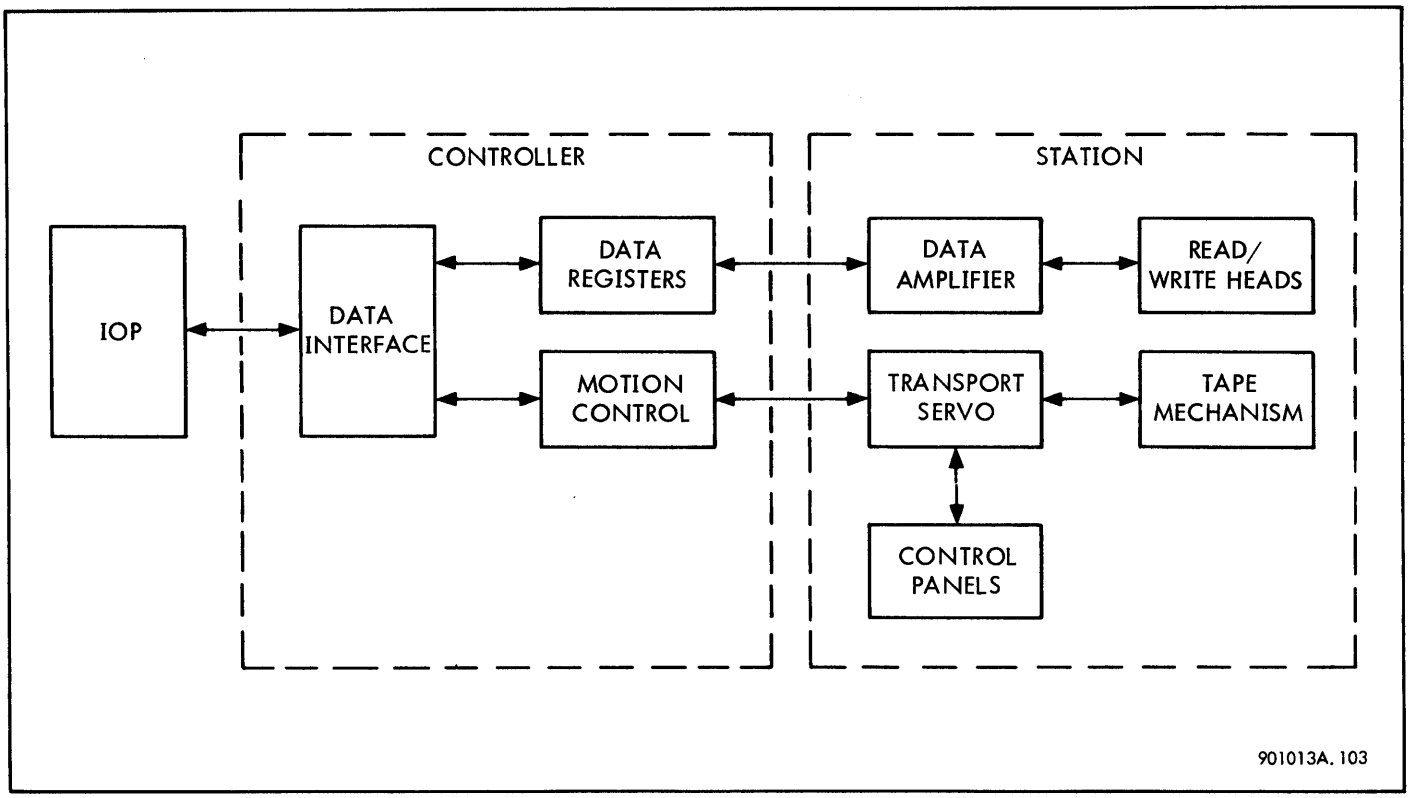


Figure 1-3. Magnetic Tape System Block Diagram

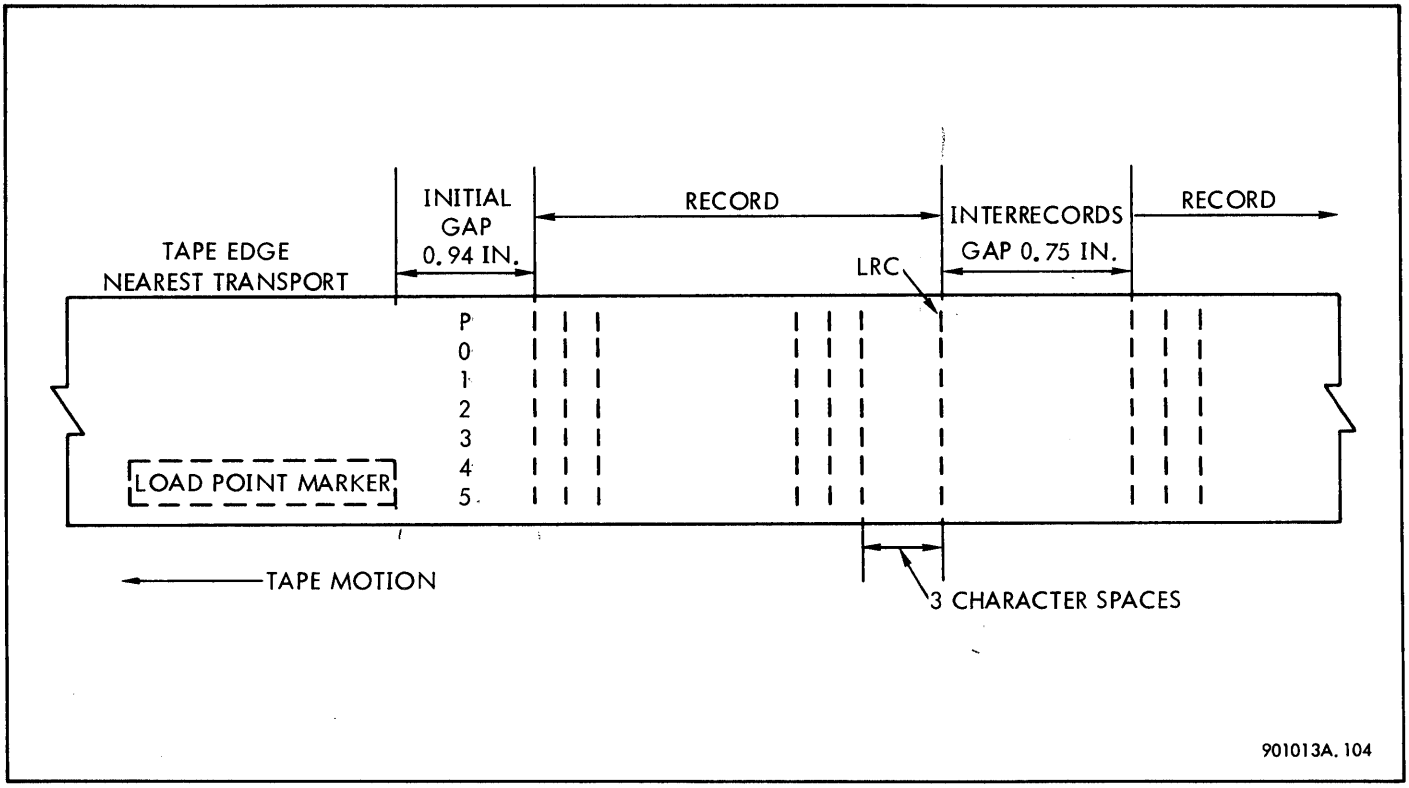


Figure 1-4. Physical Spacing on Tape

Table 1-1. General Requirements

Characteristics	Specifications
Power requirements	
Primary	108-127 Vac, 30A 45-66 Hz, 1Ø *
Secondary	±25 Vdc (±10%) ±8 Vdc (±10%) +4 Vdc (±10%)
Environmental requirements	
Temperature range	50°F-140°F
Humidity range	5% - 80%
Logic levels	
True	+4.0 ±0.4 Vdc
False	+0.25 ±0.25 Vdc
Tape characteristics	
Recording density	200, 556, or 800 bpi
Width	1/2 in.
Type	1.5 mil base, Mylar
Reel size	10.5 in. diameter 3.688 in. hub (IBM)

* 50 Hz operation requires the 50 Hz modification kit part No. 137746

Table 1-2. Parameter Definitions and Specifications

Parameter	Definition	Specification
Start time	The time interval between the receipt of a start command and the attainment of a tape speed that is within 8% of nominal speed	5.0 ms max
Start distance	The distance traversed by a point on the tape during the start time	0.190 ±0.01 in.

Table 1-2. Parameter Definitions and Specifications (Cont.)

Parameter	Definition	Specification
Nominal tape speed	The speed at which the tape moves across the read/write heads for purposes of reading and writing	75 ips
Total speed variation	The maximum deviation from the nominal tape speed at any time after start time and previous to a stop command	±8%
Fast tape speed	The speed at which the tape moves for purposes other than reading and writing	250 ips ±5%
Stop time	The time interval between the receipt of a stop command and the cessation of tape motion	5.0 ms max
Stop distance	The distance traversed by a point on the tape during the stop time	0.190 ±0.01 in.
Skew	The displacement of a bit from a line across the tape drawn perpendicular to the direction of ideal tape motion at the head assembly	
Static skew	The nonvarying portion of skew contributed by the mechanical tolerances of the tape, transport, and head assembly	225 µin max
Dynamic skew	The portion of skew contributed by time-variant tape motion not parallel to the ideal tape path	225 µin (p-p)

1-25 FUSE AND LAMP COMPLEMENT

The fuses and lamps used in the magnetic tape system are listed and described in table 2-1. Refer to table 4-28 for lamp location and identification.

SECTION II
OPERATION AND PROGRAMMING

2-1 CONTROLS AND INDICATORS

The following information defines the operation and function of all the controls and indicators in the station.

Manual control of the tape station is provided by switches located in one of the following:

a. Operator control panel

b. Auxiliary control panel

c. Interlock system

d. Power distribution chassis

e. Power supply PT19 and PT16 chassis

All indicators are contained on the operator control panel. They display the current status and conditions of the tape system.

2-2 OPERATOR CONTROL PANEL SWITCHES (See figure 2-1)

During normal operation, the only controls accessible to the operator are those on the control panel. This panel is mounted on the front of the tape station, above the transport main casting. The names, reference designators, types, and functions of the control switches are listed in table 2-1.

2-3 AUXILIARY (MAINTENANCE) CONTROL PANEL SWITCHES (See figure 1-1)

The auxiliary control panel is inset directly below the lower right-hand corner of the station transport main casting. It is accessible from the front of the station when the swinging front door is open. The panel is equipped with three switches, labeled FORWARD, REVERSE, and FAST. The switches are used for motion control of the station transport when the station is being operated in the manual mode.

The FORWARD and REVERSE switches are used to control tape directional motion at a speed of 75 ips. For fast tape motion, the direction switch selected is used in conjunction with the FAST switch, which causes the fast tape speed circuitry to be energized, producing a 250 ips tape movement.

2-4 SWINGING FRONT DOOR INTERLOCK SWITCH

The swinging door interlock switch is a part of the auxiliary control panel. Since this switch is in the door interlock system, the door must be closed for the station to become ready. The switch may be actuated with the door open for maintenance purposes by pulling outward on the pushrod. Under normal operating conditions, the switch opens when the swinging door is swung outward and closes when the swinging door is shut. Table 2-2 lists the auxiliary panel switches and their functions.

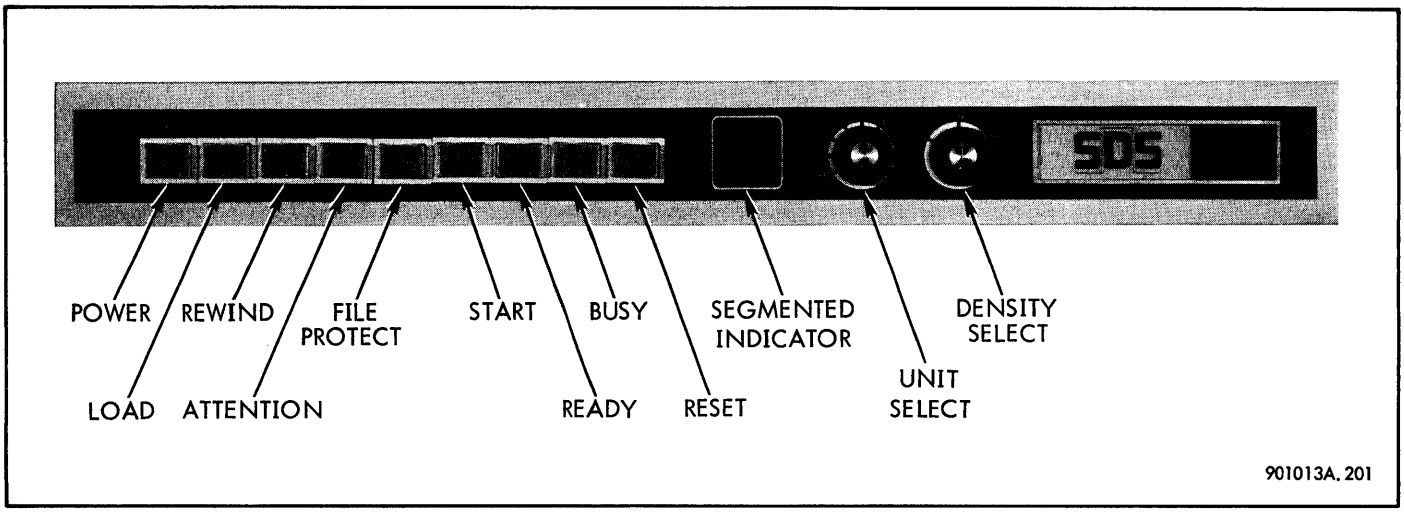


Figure 2-1. Operator Control Panel, Front View

Table 2-1. Operator Control Panel Switches and Indicators

Name	Reference Designator	Type	Function
POWER			
Switch	S1	Dpdt, alternate action pushbutton switch	Controls the primary power to the drive electronics and to the motors and blowers in the positive pressure and vacuum systems. It is effective only if the circuit breaker (CB1) is closed on the power distribution chassis
Indicator	DS1	Incandescent 28-Vdc midget lamp	Lights when the circuit breaker on the power distribution chassis is set to ON and the POWER switch is pressed on the operator control panel
LOAD			
Switch	S2	Dpdt, momentary contact pushbutton switch	Causes the transport to load tape automatically into the vacuum chambers. Actuation of this switch feeds tape from the file reel into both the file and fixed vacuum chambers. The tape is then driven to the load point (BOT marker), at which time the tape motion ceases and the unit becomes ready. The switch is pressed after loading a new tape onto the file reel. When the BOT marker is detected, the LOAD indicator lights on the operator control panel
Indicator	DS2	Incandescent 28-Vdc midget lamp	Lights whenever the tape reaches the load point position. This position is reached with tape motion stopped and the beginning of tape reflective marker (BOT) positioned directly under the photosense head
REWIND			
Switch	S3	Dpdt, momentary contact pushbutton switch	Initiates an off-line rewind operation, provided the station is not in the automatic mode. When this switch is activated, fast reverse tape motion takes place and the tape rewinds until the BOT marker is detected, at which point tape motion ceases, and the LOAD indicator lights on the operator control panel. When this switch is pressed, with the tape in the load point position, an unload operation is initiated. The unload operation is performed to unwind the portion of tape ahead of the BOT marker from the fixed reel
Indicator	DS3	Incandescent 28-Vdc midget lamp	Lights throughout the duration of a rewind operation. It goes out when the beginning of the tape marker is detected by the photosense head. It also lights when fast tape motion is initiated from the auxiliary (maintenance) panel
ATTENTION			
Switch	S4	Dpdt, momentary contact pushbutton switch	Pressing this switch when the station is not in automatic sets a latch that provides a device interrupt to the processor when the station is switched into automatic. Pressing this switch when the station is in automatic has no effect
Indicator	DS4	Incandescent 28-Vdc midget lamp	Lights when the ATTENTION switch is pressed while the station is not in the automatic mode. It remains on until the interrupt call signal comes true from the controller

(Continued)

Table 2-1. Operator Control Panel Switches and Indicators (Cont.)

Name	Reference Designator	Type	Function
FILE PROTECT			
Indicator	DS5	Incandescent 28-Vdc midget lamp	Lights when the write enable ring is not installed in the file reel. This constitutes a file protect condition. No writing can take place under these circumstances
START			
Switch	S6	Dpdt, momentary contact pushbutton switch	Places the station in the automatic mode, provided the station is ready (all interlocks closed)
Indicator	DS6	Incandescent 28-Vdc midget lamp	Lights when the station is in automatic. In this mode, the station may respond to tape motion commands from the controller
READY			
Switch	S7	Dpdt, momentary contact pushbutton switch	Tests all panel indicator bulbs with the exception of the POWER light. Pressing this switch should cause all the indicators except POWER and RESET to light
Indicator	DS7	Incandescent 28-Vdc midget lamp	Lights when the station is operational, but not busy. The station is operational if all the voltages are present, the interlocks are closed, and no reset, load, or tape backup operation is taking place. The station is busy if it has been selected for any operation
BUSY			
Indicator	DS8	Incandescent 28-Vdc midget lamp	Lights when the station is operational and busy. The station is operational if all the voltages are present, the interlocks are closed, and no reset, load, or tape backup operation is in progress. The station is busy only if it is performing an operation in response to a command from the controller
RESET			
Switch	S9	Dpdt, momentary contact pushbutton switch	Resets the station to the manual mode. In this condition tape motion is stopped and the station no longer responds to tape motion commands from the processor
UNIT SELECT			
Switch	S11	Rotary, 9-position, 3-deck	The positioning of this switch determines the station number (0-7). There may be 8 stations connected to a controller. It is the station number that determines which station responds to a given command from the processor. The command includes a station address number, which is compared with the number specified by the UNIT SELECT switch. No two stations connected to a controller can have the same switch setting. The UNIT SELECT switch also has an OFF position. With the switch set to OFF, the particular station does not respond to the station address line from the controller. Status checks may be made on a station in manual or automatic mode by addressing the station. Because of this, the only way a station may be taken off-line is to set the UNIT SELECT switch to OFF

(Continued)

Table 2-1. Operator Control Panel Switches and Indicators (Cont.)

Name	Reference Designator	Type	Function
SEGMENTED Indicator	DS10	Incandescent 28-Vdc midget lamps (7 bulbs)	Shows the number (0-7) selected for a particular unit or indicates the off-line position
DENSITY SELECT Switch	S12	Rotary, 3-position	This switch permits the selection of one of three operating densities: 200, 556, or 800 bpi

Table 2-2. Auxiliary Control Panel Switches

Name	Type	Function
FORWARD	Spdt momentary contact pushbutton switch	Moves tape forward at 75 ips
REVERSE	Spdt momentary contact pushbutton switch	Moves tape in reverse at 75 ips
FAST	Spdt momentary contact pushbutton switch	Used in combination with FORWARD or REVERSE switch to move tape at 250 ips
Swinging front door interlock		In normal operation, the switch opens when the swinging door is swung outward. This opens the interlock network and prevents the station from being ready

2-5 POWER DISTRIBUTION CHASSIS SWITCHES (See figure 1-2)

The power distribution chassis is mounted near the bottom front left-hand corner of the tape station. See paragraph 3-9 for detailed theory of operation.

There are two manual controls mounted on the power distribution chassis. These controls are a circuit breaker switch (CB1) and a toggle switch (S1) with LOCAL, REMOTE, and OFF positions. The two switches are accessible from the rear of the station. Table 2-3 describes these switches and their functions.

2-6 POWER SUPPLY SWITCHES AND FUSES

Three power supplies are used in the tape station: the PT19, PT16, and PT18 power supplies. The PT19 power supply is located at the bottom rear of the station (figure 1-1); the PT16 power supply is mounted on the top left-hand side of the swinging frame assembly; the PT18 power supply is mounted on the bottom left-hand side of the swinging frame assembly (figure 1-2). There is an ON-OFF circuit breaker on both the PT19 and PT16 power supplies. The H-L-L switches on the PT18 and PT16 supplies are used by maintenance personnel only. The fuses on the supplies are listed in the power supply manual listed in the front matter. The fuse in the PT19 supply is accessible only after removing the top cover of the supply. Refer to the list of related publications for manuals that give a detailed description of these supplies.

2-7 MANUALLY OPERATED INTERLOCK SWITCHES (See figure 1-1)

The tape station interlock system consists of manually operated switches: the top door switch, the swinging door switch, and the bottom door switch. Table 2-4 lists the switches, how they are actuated, and their functions; figure 2-2 shows the functions of the switches.

Table 2-3. Power Distribution Chassis Switches

Name	Reference Designator	Type	Function
ON-OFF	CB1	Circuit breaker, 15A, 1 pole	When placed in the ON position connects 115 Vac power to the positive pressure system pump, the vacuum system blowers, and the servo power supplies in the transport drive electronics, if ac power is connected to the power distribution chassis at P1, and the LOCAL-OFF-REMOTE switch is not in the OFF position
LOCAL-OFF-REMOTE	S1	Toggle, dpdt, 9V	Determines whether the 115 Vac power to the power distribution chassis is controlled by the processor control panel or is applied locally when 115 Vac is connected at P1. Can also be set to OFF to remove all ac power into the power distribution chassis. When set to LOCAL, the power is connected to the station as soon as 115 Vac is connected to P1 on the power distribution chassis. When set to REMOTE, ac power is connected to the station only after the POWER switch is set on the central processor control panel, if 115 Vac is connected to P1 on the power distribution chassis

Table 2-4. Manually Operated Interlock Switches

Switch	How Actuated	Function
Top door switch	This switch is closed only when the sliding glass door is completely shut	Prevents the station from being ready if the sliding glass door is open
Swinging door switch	This switch is closed when the swinging door is completely shut. For maintenance purposes it may be closed by pulling outwards on the switch pushrod	Prevents the station from becoming ready when open
Bottom door Switch	This switch closes when the sliding glass door is lowered to the fully open position	When this switch is closed, it connects brake power to the reel motors to release the brakes and shut off the vacuum and positive pressure systems

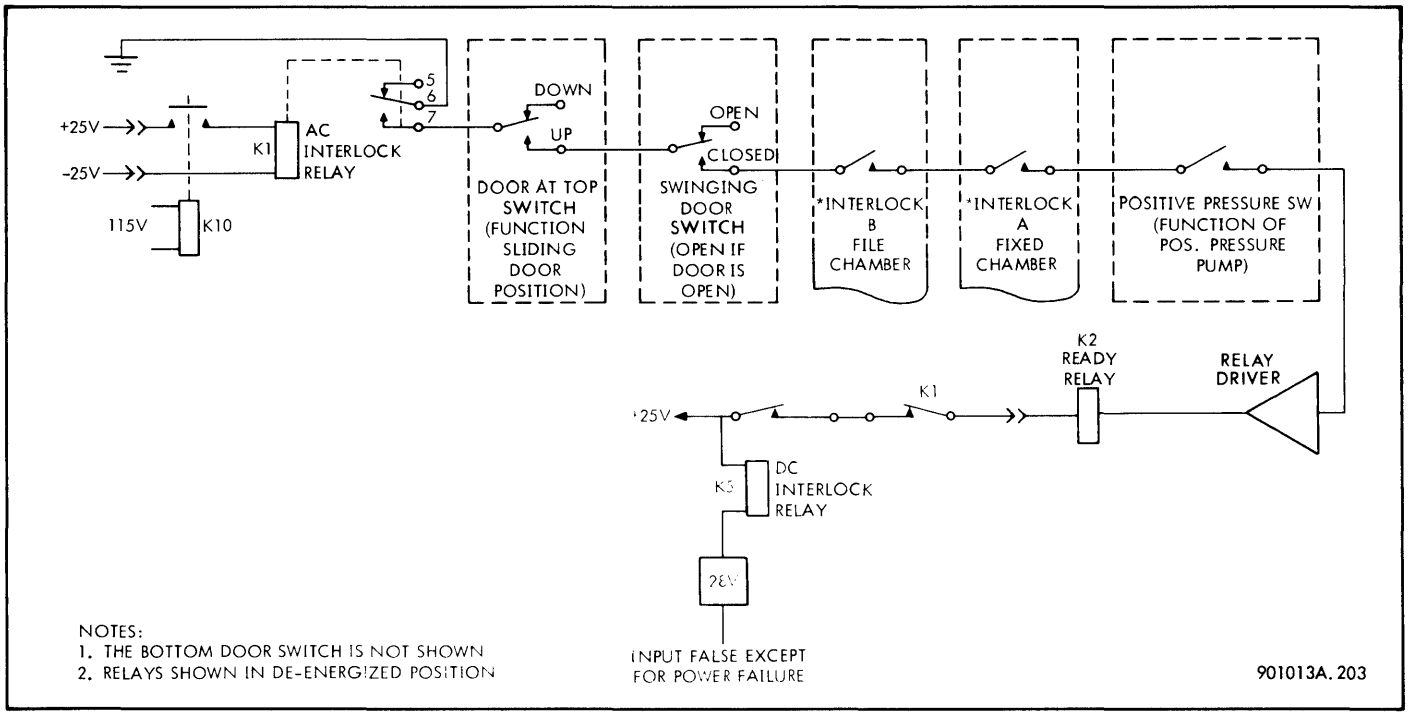


Figure 2-2. Interlock Network

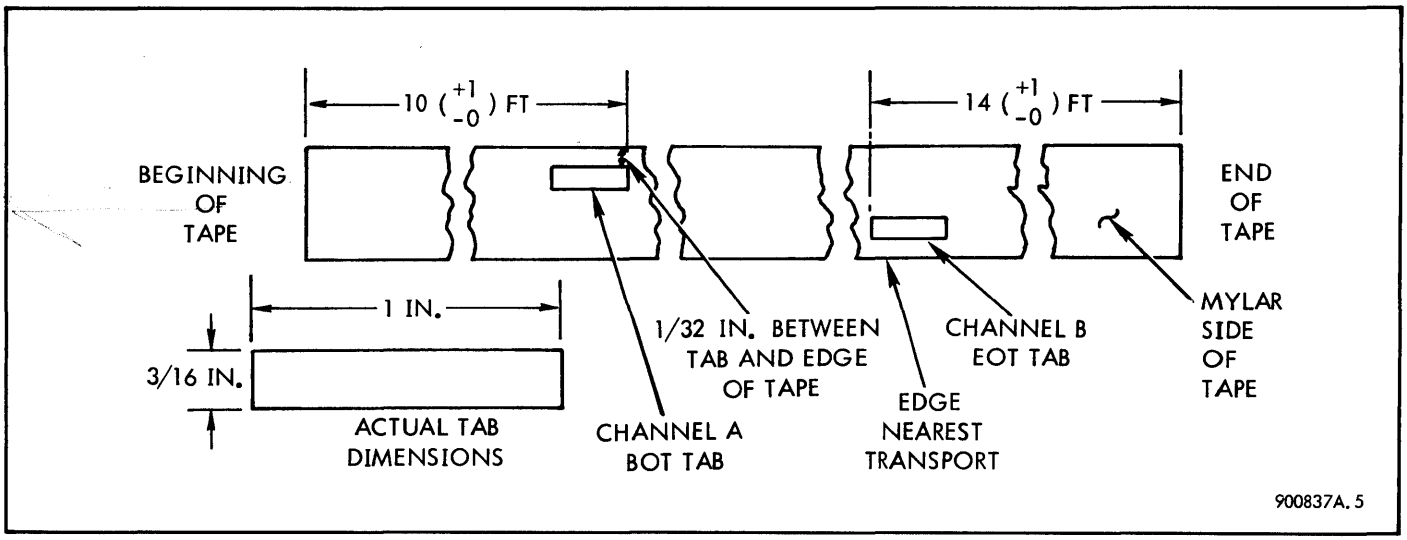


Figure 2-3. Location of Reflective Tape Markers

2-8 OPERATING INSTRUCTIONS

2-9 INITIAL TURN-ON PROCEDURE

To completely energize the magnetic tape system, execute the following steps:

a. Place the circuit breakers on the PT16 and PT19 power supplies to the ON position.

b. Place circuit breaker CB1 (ON-OFF) and switch S1 (LOCAL-OFF-REMOTE), in the power distribution chassis, to the ON and REMOTE positions, respectively.

c. Press the POWER switch on the operator control panel.

2-10 TAPE PREPARATION

2-11 Reflective Markers (Figure 2-3)

Reflective markers are placed on the tape to enable sensing the beginning and end of the usable portion of the tape. The reflective markers are plastic strips coated on one side with adhesive and on the other with vaporized aluminum. They are placed on the base or uncoated side of the tape for detection by the photosensing circuits.

2-12 File Protect Ring

A circular slot around the hub opening on the back of each tape reel is designed to accept a plastic file protect ring (figure 2-4). A write operation is permissible only when a file protect ring is present on the supply reel. The FILE PROTECT indicator on the operator control panel is lit when a file protect ring is not present on the supply reel.

2-13 Push-On, Pull-Off (POPO) Hub Assembly (Figure 2-5)

The station is equipped with a POPO hub assembly, which is attached to the shaft of the file reel motor, and upon which is mounted the file reel. The POPO hub simplifies the procedure for mounting or removing the file reel from the station transport. To install a file reel, hold the reel with both hands, slip the reel over the hub assembly, and then push the reel inward on the hub as far as possible. To prevent tape damage while installing the reel, apply the pressure only on the reel flange nearest the tape transport. To remove the reel, pull it outward with both hands on the outer flange.

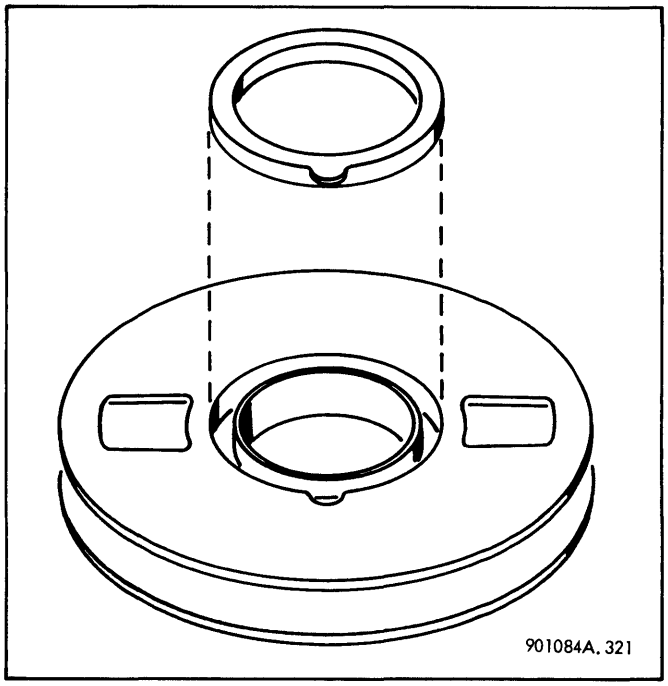


Figure 2-4. File Reel and File Protect Ring

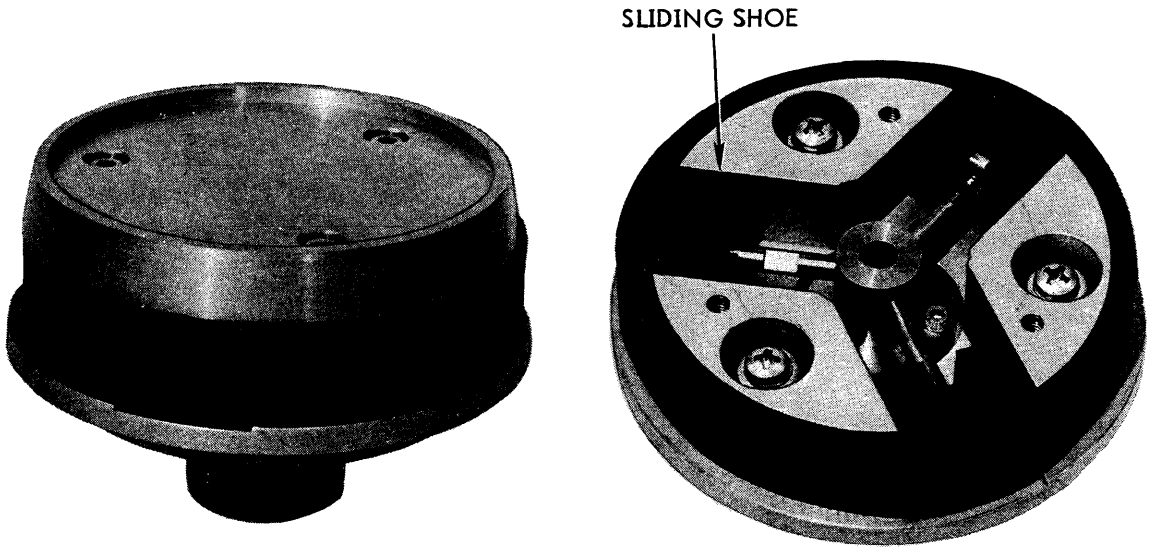


Figure 2-5. POPO Hub Assembly

2-14 LOADING THE TRANSPORT

The procedure for loading the tape from the file reel to the fixed reel after the file reel has been mounted is as follows:

a. Close the swinging front door and lower the sliding glass door to the fully open position.

b. After determining that the write enable ring is in place if file protect is not required, push the supply reel onto the file reel hub.

c. Unwind five to six feet of tape leader from the file reel.

d. Thread the tape along the path shown in figure 2-6. Wind two to four turns of tape onto the fixed reel. Because the transport provides an automatic tape loading feature, it is not necessary to feed tape manually into the vacuum chambers.

e. Raise the sliding glass door to the fully closed position, then press the LOAD switch on the operator control panel. This initiates the following load sequence:

1. The capstan and the reels move forward, serving tape into the vacuum chamber.

2. The moving tape arrives at load point, forward motion ceases, and the LOAD indicator on the control panel lights.

3. The tape loops settle to their standby positions in the vacuum chambers. This completes the transport loading operation.

Note

If forward motion does not stop when the load point is reached, press the RESET switch to stop the transport and check the position of the BOT marker (see figure 2-3).

2-15 ON-LINE OPERATION

After loading the transport and closing all interlock switches (see table 2-4 and figure 2-2), the system becomes fully operational. To put the station on-line, set the UNIT SELECT switch to the proper station number, as displayed by the segmented indicator (DS10), then press the START switch. If an interrupt is desired, to let the CPU know that the station is available, the ATTENTION switch should be pressed before the START switch is activated. These switches are all located on the operator control panel (see figure 2-1).

2-16 TURNOFF PROCEDURE

If the removal of all power from the magnetic tape system is desired, the opposite directions of the turn-on procedure should be executed and the steps followed in reverse sequence.

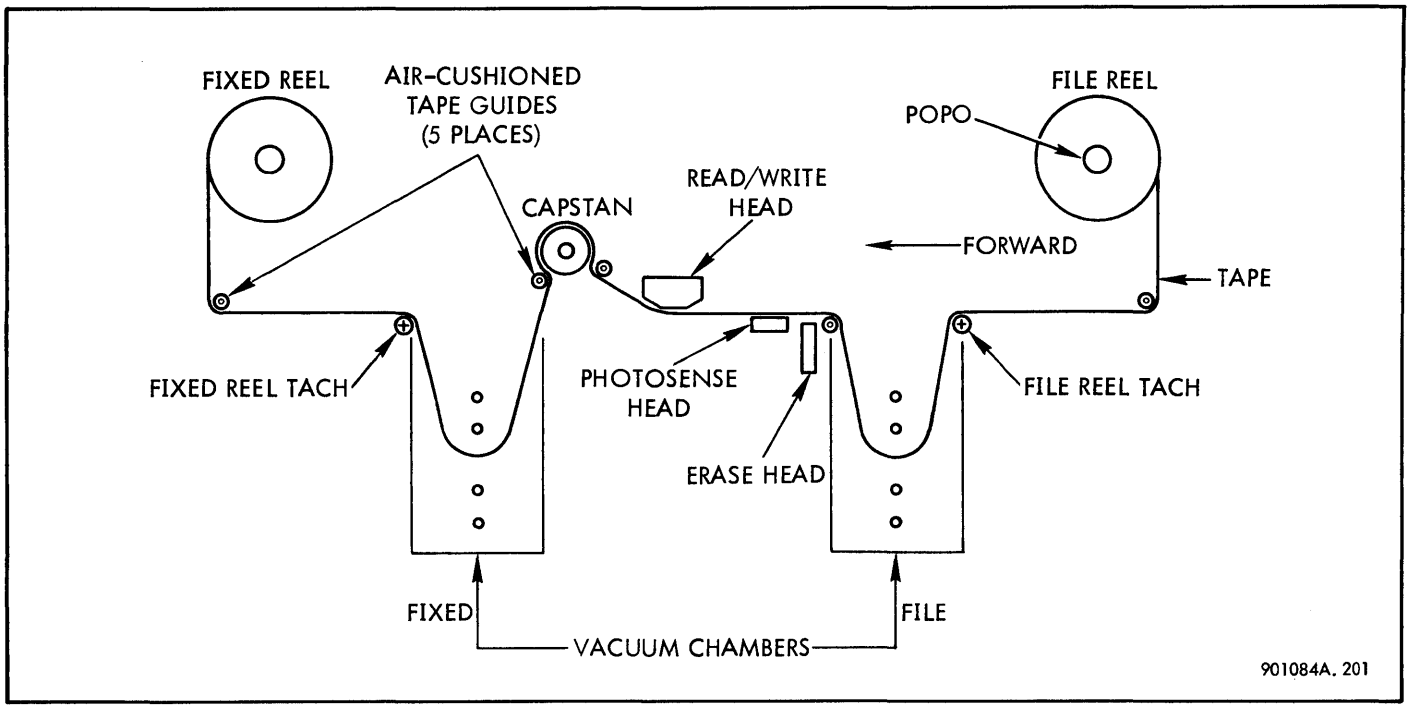


Figure 2-6. Tape Path

2-17 PROGRAMMING

This portion of the manual describes the magnetic tape system orders, error indications, and input/output (I/O) instructions and responses. Specific procedures for programming on-line test routines are available in the magnetic tape test diagnostic program manuals, SDS publications 901536 and 901165. Further information is found in the diagnostic control program reference manual, SDS 900712. For off-line operation and trouble analysis, the peripheral equipment tester (PET) is recommended. Instructions for PET operation are provided in SDS publication 901004.

2-18 MAGNETIC TAPE SYSTEM I/O INSTRUCTIONS AND RESPONSES

The CPU communicates with the magnetic tape system through the following five instructions:

Instruction Name	Mnemonic
Start input/output	SIO
Halt input/output	HIO
Test input/output	TIO
Test device	TDV
Acknowledge I/O	AIO

An eight-bit I/O address must be provided by the I/O processor (IOP) to select a device for the SIO, HIO, TIO, and TDV instructions. For the AIO instruction, the device selected by the priority chain to process its interrupt presents its eight-bit address to the IOP. The assignment of an address for the magnetic tape controller is performed by setting up switches on the LT26 module in the subcontroller portion of the controller (chassis Y). The magnetic tape controller and the station respond to each I/O instruction with a set of condition codes and with status information for the CPU to examine. This information is contained in bit positions zero through seven of the status response byte (see tables 2-5, 2-6, and 2-7). The symbols CC1 and CC2 refer to condition code bits when the interface is with Sigma 5 and 7 computers. The symbols O (overflow) and C (carry) correspond to CC1 and CC2, respectively, when the interface refers to Sigma 2 computers.

2-19 Start Input/Output (SIO)

The CPU executes an SIO to initiate an input/output operation with the device specified by the I/O address. The addressed controller sets up the condition codes (CC1 and CC2) in the IOP for the CPU to examine, as follows:

CC1	CC2	Interpretation
0	0	I/O address recognized and SIO accepted (tape station has advanced to busy condition)
0	1	I/O address recognized but SIO not accepted (tape station already busy or device interrupt pending)
1	0	Tape system attached to a busy selector IOP (not applicable to Sigma 2)
1	1	I/O address not recognized

I/O address recognition indicates that the addressed station is on-line. The magnetic tape controller accepts the SIO and indicates a successful SIO only if the controller is not busy with a previous operation, if the station addressed is operational and ready, and if neither the controller nor the addressed station has an interrupt pending.

2-20 Halt Input/Output (HIO)

Upon execution of an HIO, the addressed station immediately halts all current operations. The magnetic tape controller itself, if busy, returns to the ready state. If the HIO is addressed to the active station that has a transmission interrupt pending in the controller, this interrupt is reset. An HIO instruction is used only in special cases, and the tape position of a busy station so halted is undefinable. The condition codes for an HIO are as follows:

CC1	CC2	Interpretation
0	0	I/O address recognized and tape station not busy when halt occurred
0	1	I/O address recognized and tape station busy when halt occurred
1	1	I/O address not recognized

2-21 Test Input/Output (TIO)

The CPU uses a TIO instruction to gain access to the status information of the selected IOP, magnetic tape controller, and station, without affecting their operations. The condition codes for a TIO are as follows:

CC1	CC2	Interpretation
0	0	I/O address recognized and SIO can be accepted (station ready with no interrupt pending)
0	1	I/O address recognized but SIO cannot be accepted
1	0	Tape system attached to a busy selector IOP (not applicable to Sigma 2)
1	1	I/O address not recognized

Status response information for the SIO, HIO, and TIO instructions is given in table 2-5.

Table 2-5. Status Responses, SIO, HIO, and TIO Instructions

Bit Position	Bit State	Description
0	1	Interrupt pending. Either the addressed station has requested an interrupt or the magnetic tape controller has set an interrupt after having received a request from the IOP that was associated with previous data transmission to the addressed station. An SIO is not possible while a controller interrupt is pending, but command chaining may occur
1, 2	0, 0	Device ready. The selected station is operational and is not connected to the magnetic tape controller for an operation
	0, 1	Device not operational. The addressed station has developed some condition that does not allow it to proceed
	1, 0	Not used
	1, 1	Device busy. The addressed station is operational and either is connected to the magnetic tape controller for an operation, or is rewinding
3	1	Automatic mode. A successful SIO is possible. The station is under program control
	0	Manual mode. A successful SIO is possible. The station will delay any order requiring tape movement until the operator sets it in the automatic mode
4	1	Unusual end. The magnetic tape controller has encountered an unusual condition after having accepted the last order
5, 6	0, 0	Device controller ready. The addressed magnetic tape controller, if on-line, is in standby but may have an interrupt pending
	0, 1	Not used
	1, 0	Not used
	1, 1	Device controller busy. The addressed magnetic tape controller is on-line and is engaged in performing an operation
7		Not used

2-22 Test Device (TDV)

The CPU uses a TDV instruction to obtain a more detailed status report from the magnetic tape system. The execution of a TDV does not alter the operation of the addressed IOP, magnetic tape controller, or station. The condition codes for the TDV instruction are as follows:

CC1	CC2	Interpretation
0	0	I/O address recognized
1	0	Tape station is attached to a busy selector IOP (not applicable to Sigma 2)
1	1	I/O address not recognized

Status response information for the TDV instruction is given in table 2-6.

Table 2-6. Status Responses, TDV Instruction

Bit Position	Bit State	Description
0	1	Rate error. The addressed magnetic tape controller has detected a data transfer rate error during the last read or write operation. This condition is caused by equipment malfunction or by the I/O data rate exceeding the system limits. When a rate error occurs during writing, dummy characters are written until further bytes are available, at which time normal writing resumes
1	1	Write permitted. Writing may be performed
	0	Write protected. The addressed station is write protected; only reading may be performed
2	1	Write protect violation error. The addressed station receives a write order while write protected
3	1	End of file. Either the BOT marker has been detected or the last record read or spaced was a tape mark record
4		Not applicable
5	1	Load point. The addressed station is positioned at the BOT marker
6	1	End of tape. The addressed station has passed the EOT marker
7	1	Rewind on-line. The addressed station is rewinding in the automatic mode

2-23 Acknowledge Input/Output Interrupt (AIO)

The CPU executes an AIO to acknowledge an I/O interrupt and to identify the source of the interrupt condition. The condition codes for AIO are as follows:

CC1	CC2	Interpretation
0	0	Normal interrupt condition present. Channel end or zero byte count
0	1	Unusual interrupt condition present
1	1	No interrupt condition present

Status response information for the AIO instruction is given in table 2-7.

Table 2-7. Status Responses, AIO Instruction

Bit Position	Bit State	Description
0	1	Rate error. The magnetic tape controller has detected a data transfer rate error during the last read or write operation. This condition exists when the total I/O data transfer rate exceeds the system limits. If a rate error occurs during writing, dummy characters are written until further bytes are available, at which time normal writing resumes
1	0	Controller interrupt. In response to an IOP request, an interrupt is generated through a terminal order
	1	Device end interrupt. An interrupt is generated when either a station has just completed a rewind and interrupt order or it has been manually placed in the automatic mode
2	1	Write protect violation error. The addressed station receives a write order while write protected
3	1	End of file. Either the BOT marker has been detected or the last record read or spaced was a tape mark record

2-24 MAGNETIC TAPE SYSTEM CONDITIONS

Some of the status levels and conditions referred to in tables 2-5, 2-6, and 2-7 comprise a priority chain that must be satisfied before the system can operate in conjunction with

the IOP. Paragraphs 2-25 through 2-29 briefly explain these conditions and modes of operation.

2-25 Input/Output Address Recognition

This condition exists unless the system does not have its power on or unless the UNIT SELECT switch on the operator panel is in the OFF position.

2-26 Station Operational

The station is operational if all vacuum and interlock requirements are satisfied. A not-operational condition exists when the vacuum or positive pressure falls too low, the tape goes off its path, or either the door or window is not closed.

2-27 Station Ready

The station is considered ready when it can accept and execute an SIO instruction. The station must be operational and not busy. It may be in either the manual or the automatic mode and still be considered ready.

2-28 Controller Ready

The controller has only two states, ready and busy. It is busy if it has accepted an SIO but has not processed the instruction because of a prevailing condition in the addressed station. The controller becomes ready when the addressed station starts and conditions allow another SIO to be accepted.

2-29 Station Automatic

The station is in the automatic mode when the START switch is pressed, after all previous conditions have been met. The station changes to the manual mode when either the RESET switch is pressed, a not-operational condition arises, or a rewind off-line order occurs.

2-30 MAGNETIC TAPE SYSTEM ORDERS

An input/output operation is begun when the magnetic tape system accepts an SIO instruction. The controller then proceeds to request an order from the IOP. The orders, coded in the byte presented by the IOP, are interpreted by the controller as definite functions to be performed.

2-31 Order Codes

There are 15 orders that specify the magnetic tape system operations. The order bytes and their respective names are listed in table 2-8. Orders other than those listed result in either an unusual end or an undefined operation.

Table 2-8. Input/Output Order Bytes

BIT POSITIONS 0	1	2	3	4	5	6	7	HEXADECIMAL EQUIVALENT	ORDER
0	0	0	0	0	0	1	0	02	Read packed mode
0	0	0	0	0	1	1	0	06	Read binary mode
0	0	0	0	1	1	1	0	0E	Read BCD mode
0	0	0	0	0	0	0	1	01	Write packed mode
0	0	0	0	0	1	0	1	05	Write binary mode
0	0	0	0	1	1	0	1	0D	Write BCD mode
0	1	1	1	0	0	1	1	73	Write tape mark
0	0	0	0	1	1	0	0		Not used. Applicable to nine-track tape systems only
0	0	0	0	0	1	0	0		
0	0	0	0	0	0	1	1		
0	0	0	1	0	0	1	1	13	Rewind and interrupt
0	0	1	0	0	0	1	1	23	Rewind off-line
0	0	1	1	0	0	1	1	33	Rewind on-line
0	1	0	0	0	0	1	1	43	Space record forward
0	1	0	0	1	0	1	1	4B	Space record reverse
0	1	0	1	0	0	1	1	53	Space file forward
0	1	0	1	1	0	1	1	5B	Space file reverse
0	1	1	0	0	0	1	1	63	Set erase

2-32 Order Descriptions

The operations associated with the order codes used with the magnetic tape system are described below. A more detailed functional description is presented in section III of this manual.

WRITE. When a write order is received, the tape station starts forward tape motion. After a 7 ms delay, information is recorded on the tape in one of three program-selected modes: binary, packed binary, or BCD (see paragraph 3-3). When the desired number of characters has been recorded, data transfer terminates, the LRC character is recorded, and tape motion stops. If another write order arrives before the tape comes to a complete stop, motion resumes immediately but writing begins only after the 7 ms delay has elapsed.

If the order is a write tape mark, the same process outlined above takes place. The only difference is that the record written consists of a single character (the BCD character √), generated locally, with a preceding 3.5 in. erased gap, instead of normally transferred data.

READ. When a read order is received, the tape station starts forward tape motion. As soon as the portion of tape containing information reaches the read head, the detected

characters are transmitted sequentially to the IOP. The tape is read in binary, packed binary, or BCD. The controller checks vertical parity as each character passes the read head. Reading continues until the interrecord gap is detected. If no further order is pending, tape motion stops with the write head located in the middle of the interrecord gap. If another read order arrives before the tape comes to a complete stop, motion and reading resume without delay.

When an LRC character is read, longitudinal parity is checked in the controller. If an error is detected, a transmission data error indicator is set. If no error is detected, a channel end indication occurs.

The same reading operation applies to tape mark records, except that an unusual end indication is generated as soon as the LRC character has been read.

SPACE. The effect of a space order is to move the tape, with respect to the heads, in a forward or reverse direction. The length of tape that passes the heads depends on the length of the record or file that is to be spaced. Four orders determine the type of spacing to be performed: space record forward, space record reverse, space file forward, and space file reverse.

When a space record order is received, the tape is spaced over one record in the forward or reverse direction, as specified by the order. If no further order is received, the tape stops with the write head located in the center of the gap following or preceding the record spaced. A channel end indication is then generated.

When a space file order is received, the tape is spaced over one file in the forward or reverse direction, as specified by the order. The tape stops when a tape mark is detected, with the write head located in the center of the gap following the tape mark. A channel end indication is then generated. If no tape mark is detected while the tape is being spaced in the reverse direction, the tape stops at the load point.

REWIND. The effect of a rewind order is to move the tape in the reverse direction and to stop it when the BOT marker is detected. Several tape stations in the system may perform a rewind operation simultaneously. There are three kinds of rewind orders: rewind on-line, rewind and interrupt, and rewind off-line.

When a rewind on-line order is received, if the selected station is not busy, channel end is indicated. The station then proceeds to rewind and enters into a busy condition, until tape motion stops.

A rewind and interrupt order produces the same events as a rewind on-line order, except that an I/O device interrupt is requested after the operation is completed.

A rewind off-line order is similar to a rewind on-line order, except that it switches the station to the manual mode. Operator intervention is then required to place the station back on-line.

ERASE. The only function of this order is to set an indicator that enables the station to erase 3-1/2 inches of tape preceding a record upon receipt of a write order. If the next order received is not a write order, this indicator is immediately reset.

2-33 Termination of Order and Error Indications

After executing an order, the magnetic tape controller signals the IOP by sending a channel end indication, an unusual end indication, or both, and the error indications accumulated during the order execution. Error indicators are cumulative if there is command chaining.

CHANNEL END. A channel end indication is reported after each order execution, except when any of the following conditions is present:

a. An order out service cycle terminates with an IOP error halt indication.

b. A space record reverse or space file reverse order is received by a station in which the tape is at the load point.

c. A write order is received by a station that is write protected.

UNUSUAL END. An unusual end indication is reported when any of the conditions noted in the previous paragraph is present, and also when the following conditions exist:

a. The IOP signals an IOP error halt, except when a terminal order follows the order in.

b. An attempt is made to read over a tape mark record.

c. A space record order is executed over a tape mark record.

SECTION III
PRINCIPLES OF OPERATION

3-1 INTRODUCTION

This section presents the principles of operation for the magnetic tape system. The overall functional concepts are described in respect to the basic components of the system: the station and the controller. The primary functions of the system are then explained in detail, by tracing the signals and associated circuitry that determine the system operations. A glossary of terms is provided at the end of the section.

3-2 GENERAL INFORMATION

3-3 DATA TRANSFER MODES

The standard magnetic tape system (model 7371/7372) writes and reads data in either of two program-selected modes: binary or binary coded decimal (BCD). When the binary packing option (model 7374) is added, a packed binary mode is also available to the program. The mode of operation selected is determined by the order codes.

3-4 Binary Mode

When a write operation is executed in the binary mode, data is transferred from the IOP to the controller in the same order as it is arranged in memory (see figure 3-1). The two most significant bits of each byte (bit positions 0 and 1) are discarded at the controller. During a read operation, the 6-bit byte read from the tape is reconstructed as it originally appeared in memory, with the two most significant bits substituted by zeros, before it is transferred to the IOP. Parity is always odd in binary mode.

3-5 Binary Coded Decimal Mode

When a write operation is executed in the BCD mode, data is recorded in standard 6-bit binary coded decimal interchange code (BCDIC). The 8-bit byte from the CPU, as presented by the IOP to the controller, is interpreted as being in the standard 62 character set of the 8-bit extended binary coded decimal interchange code (EBCDIC). The EBCDIC information is translated in the controller to an equivalent 6-bit character in the BCDIC format and then recorded on tape (see figure 3-2). During a read operation, the 6-bit character read from the tape is translated from BCDIC to the 8-bit EBCDIC format before it is transferred to the IOP. Parity on tape is always even in the BCD mode.

Table 3-1 shows the conversion of BCDIC to EBCDIC. Control codes are read and recorded as undefined characters. Some of the special characters in EBCDIC format are changed to fit the BCDIC character set.

3-6 Packed Binary Mode

During a write operation in the packed binary mode, each group of three 8-bit bytes from memory results in the recording of four 6-bit characters on tape (see figure 3-3). While being transferred, each bit is preserved in its relative location. The last tape character recorded consists of zeros if the CPU does not send a number of bytes which is a multiple of three. Parity in the packed mode is always odd.

The write packed end conditions are these:

a. If the record contains 3N bytes, 4N characters are recorded on tape.

b. If the record contains 3N+1 bytes, 4N+2 characters are recorded, the last character containing zeros in the four least significant bit positions.

c. If the record contains 3N+2 bytes, 4N+3 characters are recorded, the last character containing zeros in the two least significant bit positions.

During a read operation, 6-bit binary characters read from tape are packed sequentially in descending order (left to right). Four tape characters are packed into exactly three bytes and transmitted to the IOP, each bit kept in its relative location. If a multiple of four tape characters is not read, the additional characters after 4N are left adjusted within the proper three byte group in memory. The last byte transmitted is completed with an even number of zeros. The last memory byte transmitted contains eight zeros if 4N characters are not read from tape.

The read packed end conditions are these:

a. If 4N characters are read from tape, 3N bytes are sent to the IOP.

b. If 4N+1 characters are read from tape, 3N+1 bytes are sent to the IOP, the last byte containing zeros in the two least significant bit positions.

c. If 4N+2 characters are read from tape, 3N+2 bytes are sent to the IOP, the last byte containing zeros in the four least significant bit positions.

d. If 4N+3 characters are read from tape, 3N+3 bytes are sent to the IOP, the last byte containing zeros in the four least significant bit positions.

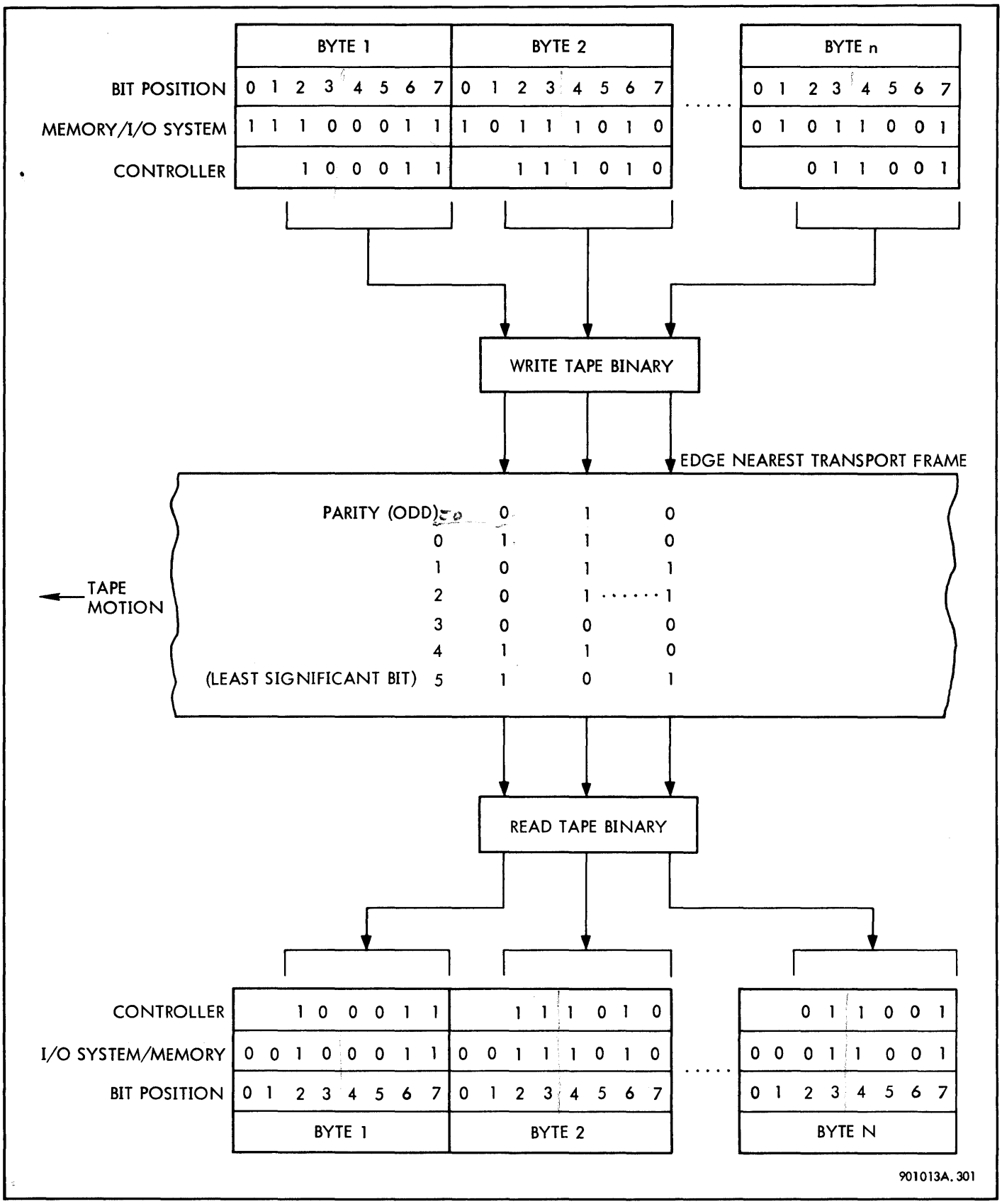


Figure 3-1. Data Representation on Tape, Binary Mode

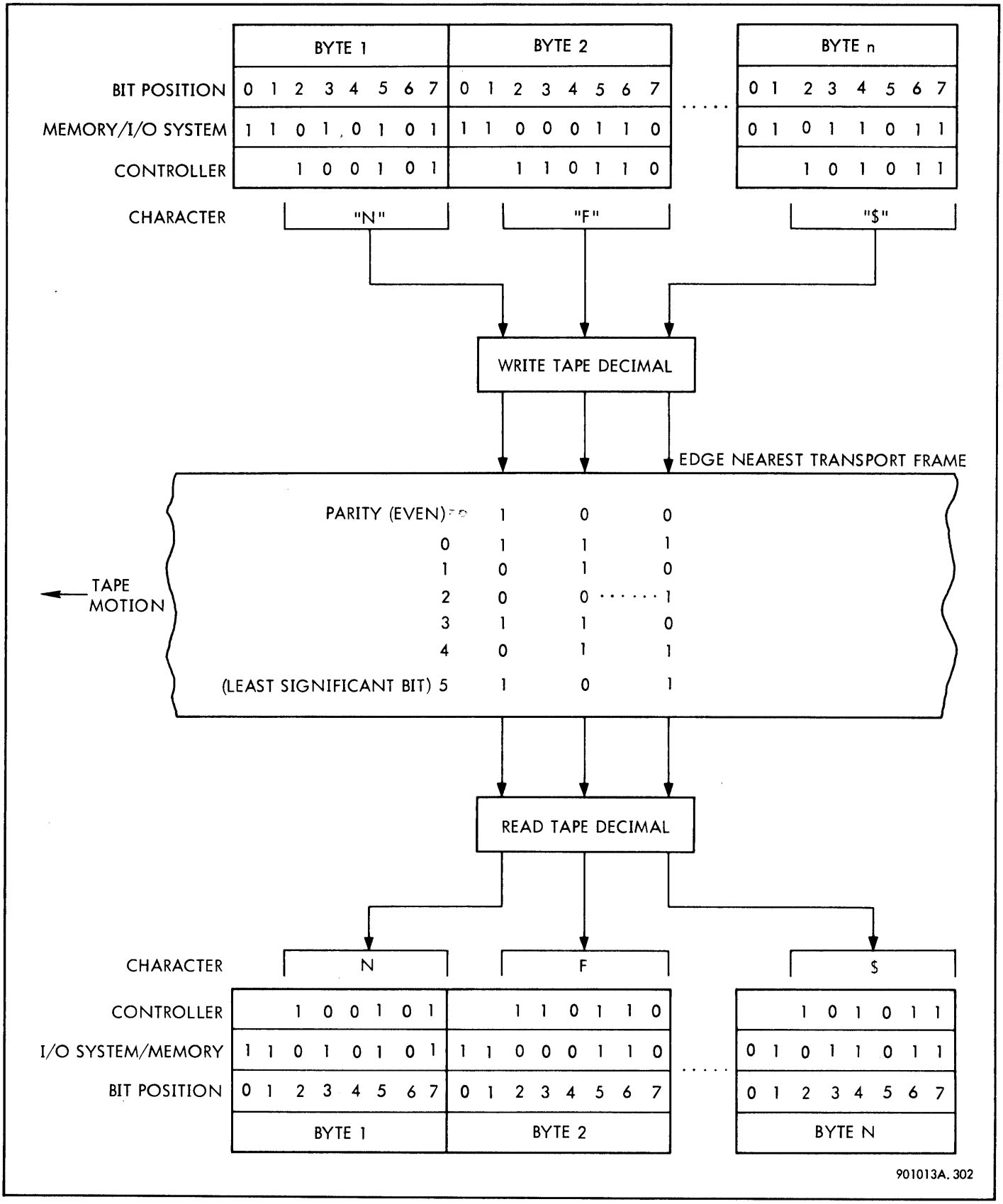


Figure 3-2. Data Representation on Tape, Decimal Mode

Table 3-1. BCDIC to EBCDIC Conversion

EBCDIC Character	EBCDIC Code Hexadecimal	BCD Code Octal	BCD Character	EBCDIC Character	EBCDIC Code Hexadecimal	BCD Code Octal	BCD Character
A	C1	61	A	6	F6	06	6
B	C2	62	B	7	F7	07	7
C	C3	63	C	8	F8	10	8
D	C4	64	D	9	F9	11	9
E	C5	65	E				
F	C6	66	F	Blank	40	20	Blank
G	C7	67	G	¢	4A	72	? or backspace
H	C8	70	H	.	4B	73	.
I	C9	71	I	<	4C	74	) or ¤
J	D1	41	J	(	4D	75	[
K	D2	42	K	+	4E	76	<
L	D3	43	L	|	4F	77	≠
M	D4	44	M	&	50	60	+ or &
N	D5	45	N	!	5A	52	! or carriage return
O	D6	46	O	$	5B	53	$
P	D7	47	P	*	5C	54	*
Q	D8	50	Q	)	5D	55	]
R	D9	51	R	;	5E	56	;
S	E2	22	S	¬	5F	57	△
T	E3	23	T	-	60	40	- (dash or minus)
U	E4	24	U	/	61	21	/
V	E5	25	V	None assigned	6A	32	‡ or tab
W	E6	26	W	,	6B	33	,
X	E7	27	X	%	6C	34	(or %
Y	E8	30	Y	-	6D	35	~
Z	E9	31	Z	>	6E	36	\
				?	6F	37	##
0	F0	12	0*	:	7A	12	0*
1	F1	01	1	#	7B	13	# or =
2	F2	02	2	@	7C	14	@ or '
3	F3	03	3	'	7D	15	:
4	F4	04	4	=	7E	16	>
5	F5	05	5	"	7F	17	√†

*During writing, both X 'F0' and '7A' are recorded as 12_8 on tape. During reading, 12_8 is always read and translated as X 'F0'

†A tape record consisting of only √ characters is defined as a tape mark

The following byte count conditions exist in the IOP after the same record has been written and immediately read in the packed mode:

Bytes Sent	Bytes Received
3N	3N
3N + 1	3N + 2
3N + 2	3N + 3

3-7 POWER CIRCUITS

3-8 Primary Power (See figure 3-4)

Primary power is derived from an external 117 Vac, 60 Hz, 30A source. The 117 Vac are connected to TB1 on the power distribution chassis. When power is applied to TB1, the muffin fan assembly, at top and bottom of the module cage, and the PT19 converter power supply are energized. The 2000 Hz output from the PT19 power supply is used as the input power source for the PT16 and PT18 power supplies, which generates the necessary dc voltages for the system.

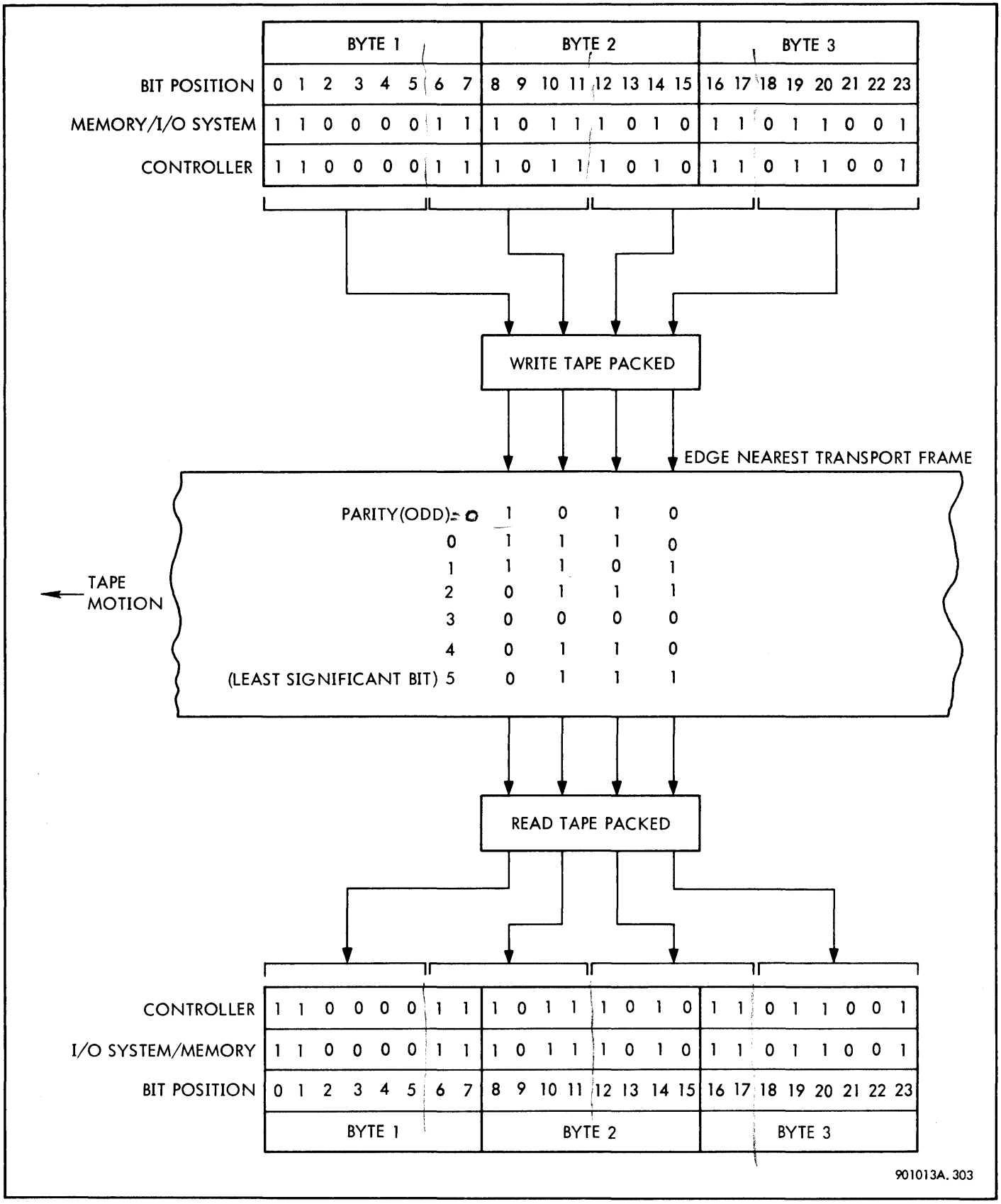


Figure 3-3. Data Representation, Packed Binary Mode

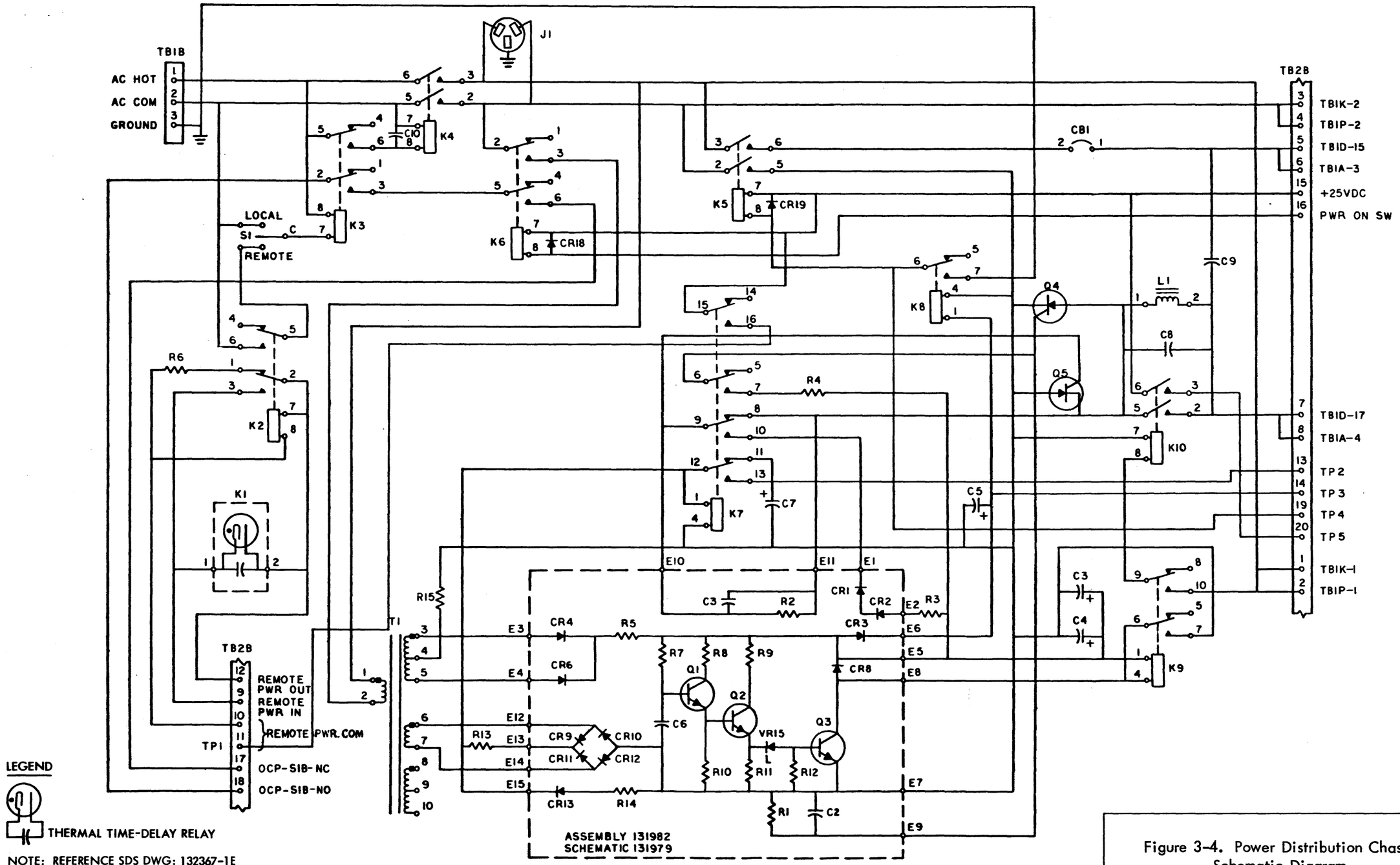


Figure 3-4. Power Distribution Chassis, Schematic Diagram

901084A.711

One side of the primary power line is routed from the power distribution chassis to the POWER switch on the operator control panel. Pressing the POWER switch to the ON position energizes relay K6 and thereby connects 117 Vac to the following parts of the system:

a. The vacuum motor. When power is applied, the motor starts rotating.

b. The transport drive electronics assembly (if the circuit breaker on the power distribution chassis is closed) and the servo amplifier power supplies.

c. The positive pressure pump. It starts functioning if the sliding door is closed.

3-9 Power Distribution (See figures 3-4 and 4-24)

The power distribution chassis has the following purposes:

a. To provide a means of controlling ac power into the station.

b. To apply power in the station by stages. This action diminishes current surges and minimizes noise transients.

c. To provide a delay before ac power is applied to the next station in the system. This ensures that the stations are energized in sequence rather than simultaneously, which would produce an undesirable current surge.

3-10 Turn-On Sequence

After the ac cord is plugged in, relay K3 turns on the power for the blower and the PT19 power supply. Relay K3 is controlled by the LOCAL-OFF-REMOTE switch S1 on the power distribution panel. If this switch is in the OFF position, power cannot be turned on. If the switch is in the LOCAL position, relay K3 energizes immediately after the power cord is plugged in. If the switch is in the REMOTE position, relay K3 energizes after approximately one second. Time delay relay K1 with R6 provides a one second delay (see figure 3-4). This delay prevents the simultaneous energizing of all the stations in the system.

Power to the vacuum blower, positive pressure pump, and servo power supply is switched on by relay K5 and SCR's Q4 and Q5, which are operated by the control circuits and relays. When the POWER switch on the operator control panel is actuated, the following events take place:

a. Relay K6 energizes, which applies primary power to the transformer.

b. Relay K8 energizes after a small delay, which in turn energizes relay K5.

c. Relay K5 connects the ac hot line to the vacuum blower positive pressure pump and servo power supply. K5 also connects the ac return line to the SCR's, which are not yet conducting.

d. Relay K7 pulls in after a 100 to 200 ms delay and turns on the SCR's. This delay is determined by capacitor C7.

e. The servo power supply capacitors are charged while the current is limited by choke L1. Relay K9 energizes after a 0.8 to 2.8 second delay, causing relay K10 to energize and short out the choke coil L1. This delay is determined by capacitor C6 in series with resistor R7 in the Q1 base bias circuit and the 5.6V zener diode in the Q3 base bias circuit. After relay K9 energizes, Q3 is shunted by contacts K9-6 and K9-7.

3-11 Turnoff Sequence

When the POWER switch is pressed to the OFF position, the following events take place:

a. Relay K6 opens and removes power from the primary of the transformer.

b. Relay K7 drops out shortly after step a occurs, removing the forward bias from the SCR's.

c. The SCR's stop conducting after the current reaches zero.

d. Relay K9 opens after the power supply capacitors are discharged through the K9 coil, which in turn opens relay K10.

e. Relay K8 opens after the voltage across capacitor C5 reaches approximately 15V. Relay K5 is then deenergized and opens both ac lines to the vacuum blower, positive pressure pump, and servo power supply. The timing diagram shown in figure 3-5 indicates the power turn-on and turnoff sequence.

3-12 STATION

The station consists basically of pneumatic and mechanical devices, with associated sensing and control electronics, which allow proper handling of the magnetic tape. Figure 3-6 shows the main components of the tape transport. The station also contains the necessary transducers and motion and data electronics to store and detect information on tape. The data electronics is described under the heading Magnetic Tape System Functions, paragraph 3-57.

3-13 PNEUMATICS

There are two separate but related pneumatic networks in the station: the positive pressure system and the vacuum system.

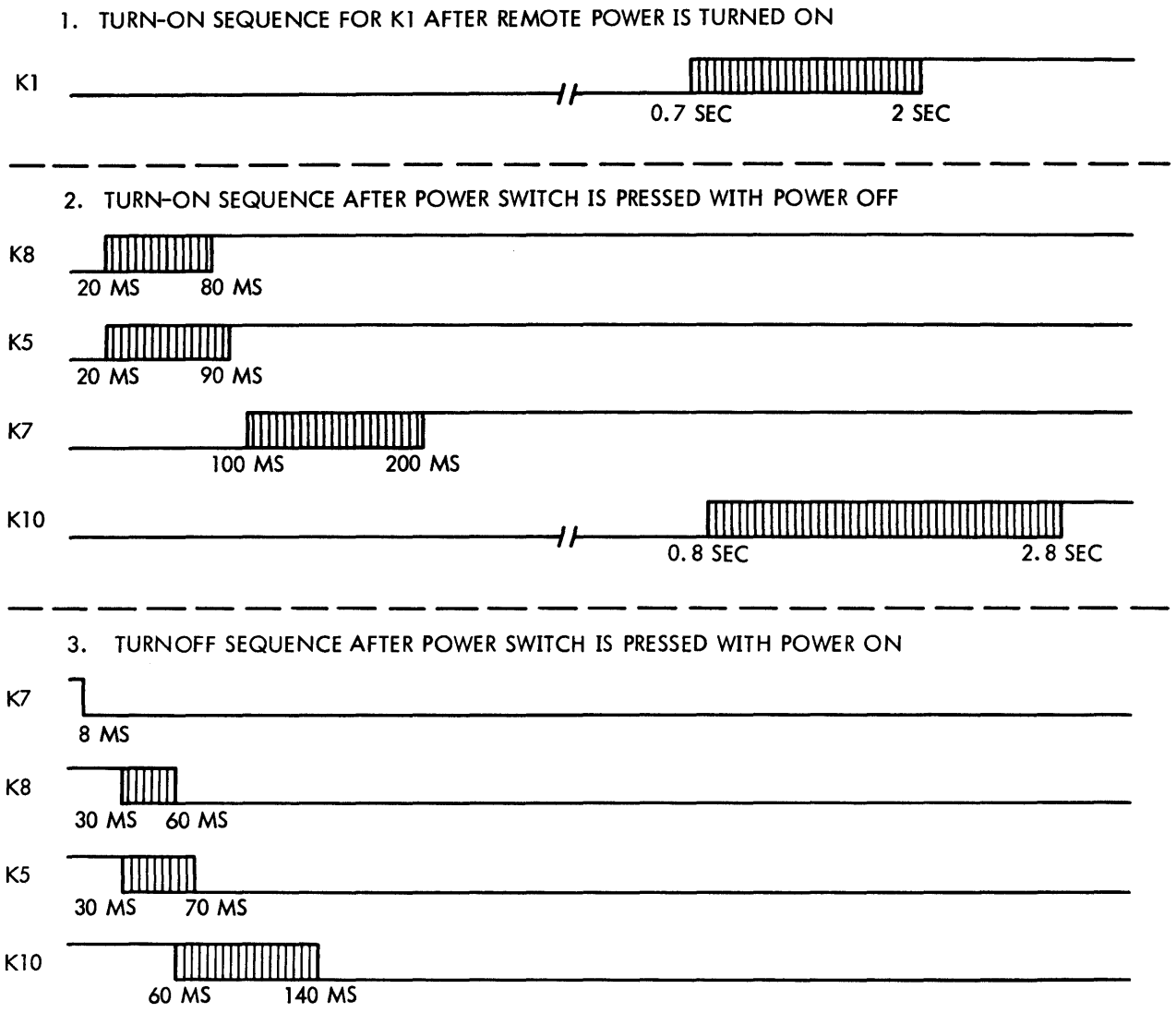


Figure 3-5. Power Sequence, Timing Diagram

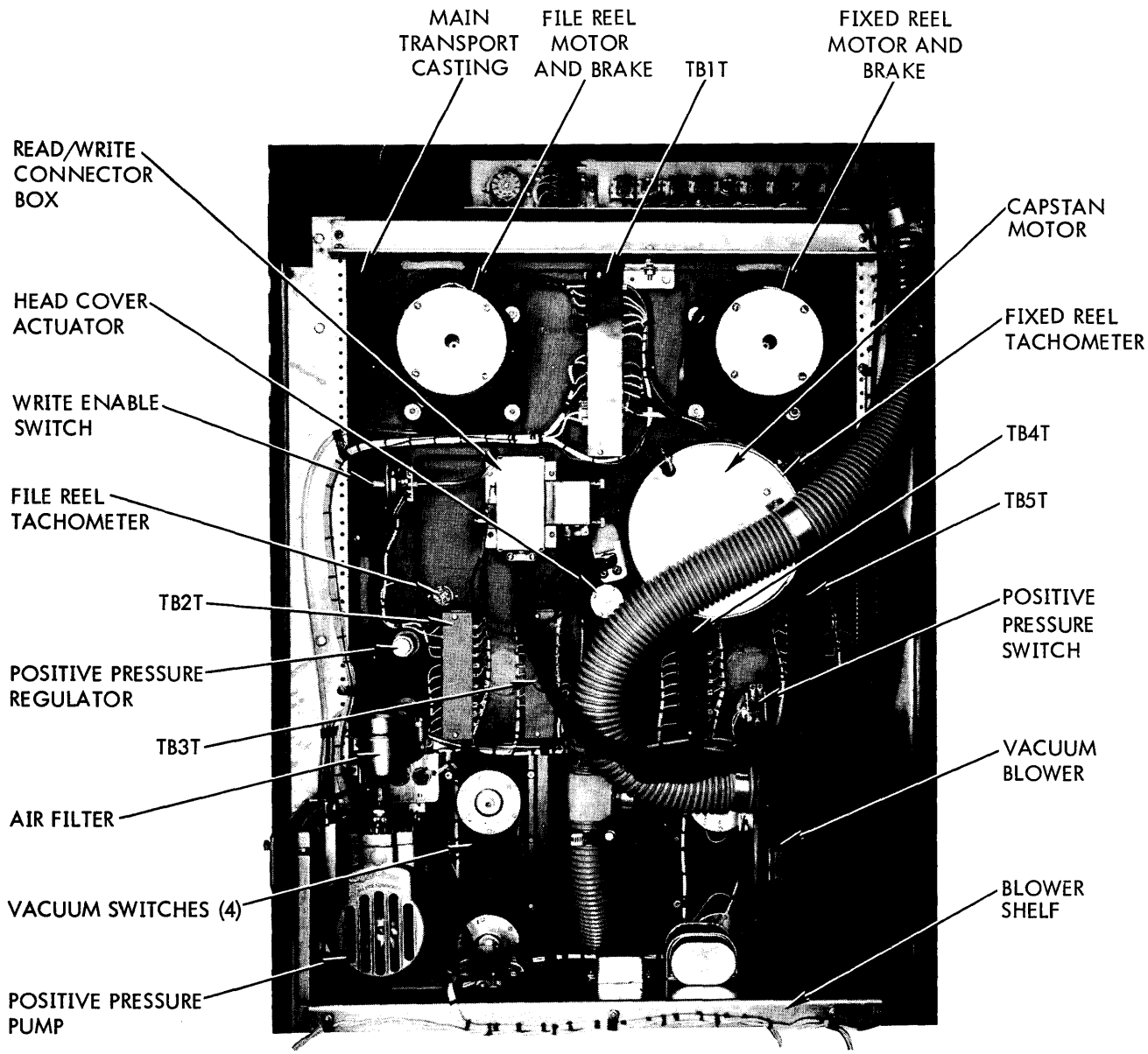


Figure 3-6. Magnetic Tape Transport, Back View

3-14 Positive Pressure System

Air pressure is generated by the positive pressure pump and fed to the air plenum, which forms part of the transport casting. The air plenum supplies air to the tape guides, the head cover actuator, and the positive pressure switch. The amount of pressure is controlled by a regulator connected to the air plenum (see figure 3-7).

TAPE GUIDES. (See figures 2-6 and 3-8.) The tape guides provide a continuous flow of air from their hollow cores (connected to the air plenum) to the surface facing the tape. The air flow is regulated to provide a cushion of air between tape and tape guide. This air layer ensures that only the read/write heads touch the recording surface of the tape.

HEAD COVER ACTUATOR. (See figures 3-6 and 3-9.) The head cover actuator consists of a piston and plunger assembly mounted in an airtight cylinder. When positive pressure is applied to the cylinder, the piston presses a return spring, which closes the head cover with the plunger. When no pressure is applied to the cylinder, the head cover remains open.

POSITIVE PRESSURE SWITCH. (See figures 3-6 and 3-10.) The positive pressure switch is connected to the air plenum and located above the vacuum blower. This switch provides a means of sensing a minimum of pressure in the air plenum, as determined by the adjustment of the positive pressure regulator. The switch is in series with interlocks A and B in the vacuum chambers (see figure 2-2). When the positive pressure reaches a specified value of 5 lb/in^2 the switch closes. The station becomes ready if interlocks A and B are closed.

3-15 Vacuum System

A vacuum is created by the vacuum blower that is located to the right of the blower shelf (see figure 3-6). The vacuum blower is connected to the vacuum plenum at the bottom front of the station through a solenoid-operated valve. The vacuum plenum provides a vacuum to the vacuum storage chambers, the write enable switch, and the tape cleaner. The vacuum blower is also connected to the capstan motor housing for cooling purposes.

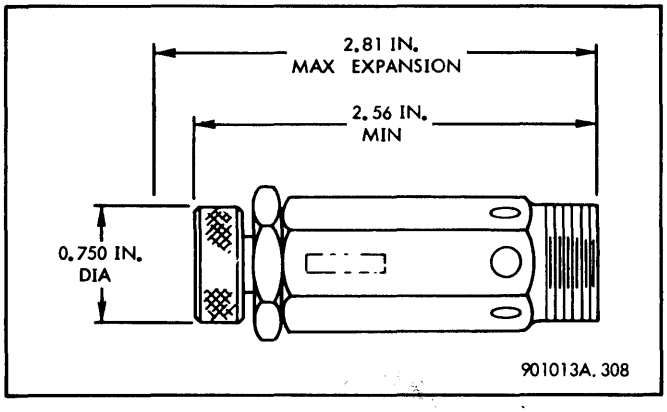


Figure 3-7. Pressure Regulator

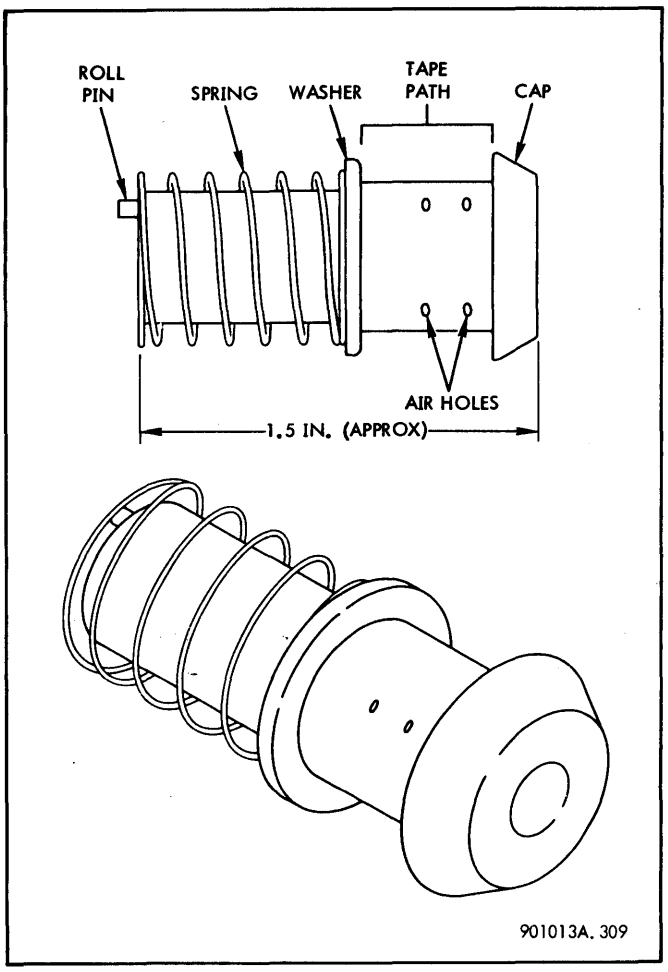


Figure 3-8. Tape Guide

VACUUM VALVE. The vacuum valve is connected between the vacuum blower and the vacuum plenum. The valve is open or closed depending on whether the station is in a ready or not-ready condition. The vacuum valve is controlled by a solenoid, which is connected in series with the bottom door switch (SN1). The solenoid is closed only when the sliding door is fully closed. When SN1 is closed, and the station is in a ready condition, the solenoid is energized and the valve opens.

VACUUM STORAGE CHAMBERS. (See figures 1-1 and 3-18.) The tape transport uses tape loops to reduce to a minimum the tape mass handled by the capstan during start and stop times. The loops, located at both sides of the capstan, are stored in two chambers associated with the fixed reel and the file reel (see figure 2-6).

When tape movement is required, the capstan pulls the tape from the loop in one chamber and places it in the other chamber, to form the other loop. As tape is drawn from the file chamber, it is replaced by the file reel. As tape is fed into the fixed chamber, the fixed reel takes up the slack. The net effect is, first, that inertia is minimized in the capstan system, so that the system only has to accelerate the

mass of a few feet of tape. Second, the tape loops in the vacuum storage chambers effectively separate the capstan movements from the reel movements. This allows the capstan to accelerate at high rates without requiring the reels to rotate at exactly the same rate.

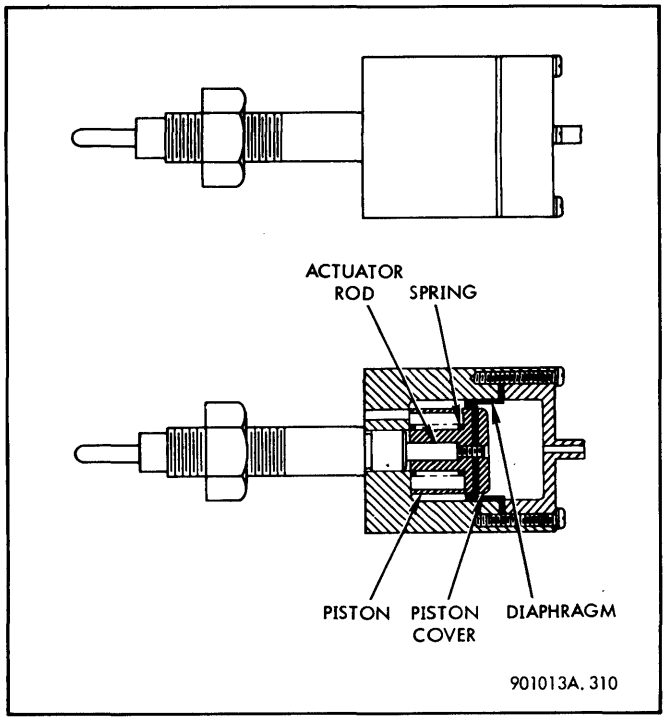


Figure 3-9. Head Cover Actuator

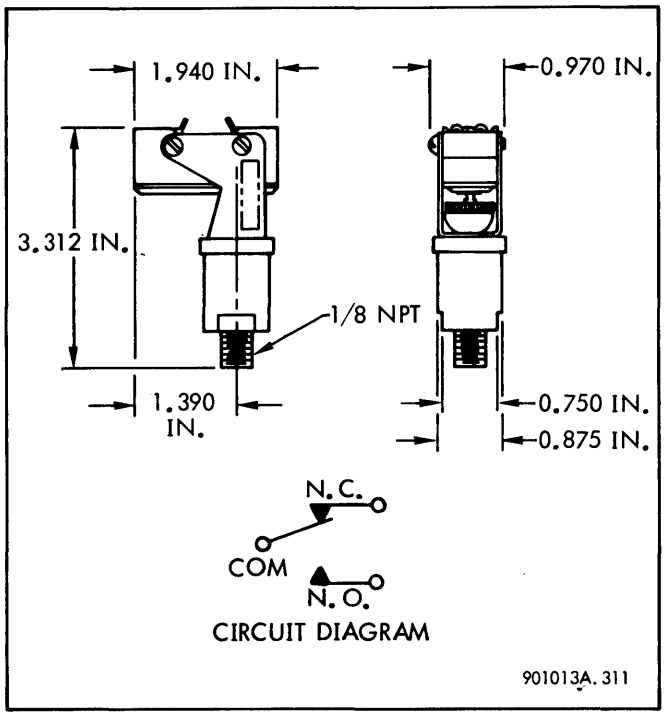


Figure 3-10. Positive Pressure Switch

The vacuum storage chambers also produce and maintain proper tape tension along the tape path. Each loop fits snugly into the chamber, effectively dividing it into two sections. The bottom portion of the chamber is connected to the vacuum plenum and is therefore under reduced pressure. The upper part is at atmospheric pressure, which pushes the tape down and provides the necessary pressure on the loop.

The sensing holes placed across the length of the chamber actuate the vacuum interlock switches and the tape loop position switches. These vacuum switches function as protection and control devices, respectively. The vacuum interlock switches interrupt the reel drive circuits, which in turn stop the reel motors when either the vacuum fails or the tape is in an abnormal position. Figures 3-6 and 3-18 show the location of these switches, while figures 3-13 and 4-13 show their function in the control circuits. A detailed operation of these switches, in association with the servo electronics, is given in paragraph 3-18.

WRITE ENABLE SWITCH. The function of the write enable switch is to permit or prevent recording on tape. This function is called file protection and depends on the presence or absence of a file protect ring in the file reel (see paragraph 2-12). The file protection function is performed by the write enable switch actuator (see figures 3-11 and 4-2) and the write enable vacuum switch (see figure 3-6).

The write enable switch actuator assembly is mounted immediately below the file reel hub. This assembly contains a piston with a pushrod connected to one end. The pushrod extends through the front of the transport casting. The file reel contains an inner groove into which a file protect ring can be inserted. When the file reel is mounted, the file protect ring, if installed, makes contact with the pushrod on the actuator, and the piston is pressed. This causes holes to close around the circumference of the actuator cylinder housing. When this occurs, pressure in the cylinder approaches a vacuum, which is produced by a hose connecting the write enable switch actuator to the vacuum plenum. Another hose connects the write enable switch actuator to the write enable vacuum switch mounted at the back of the transport casting. This switch is of a diaphragm type and closes when the pressure in the actuator cylinder approaches a vacuum.

When the file protect ring is not installed in the file reel, the holes around the actuator's cylinder housing are exposed to the atmosphere. Under these conditions, pressure on both sides of the write enable switch diaphragm is the same, and therefore the contacts are open.

When the write enable switch is closed, a ground is provided to one side of the coil in file protect relay K6. This relay is mounted on the relay chassis assembly (see figure 3-12). The other side of the relay K6 coil is connected to

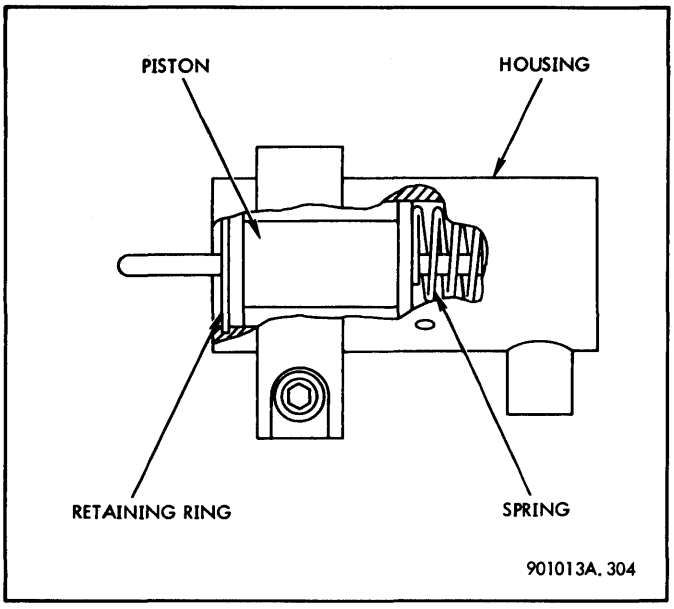


Figure 3-11. Write Enable Switch Actuator

+25 Vdc. Relay K6 is therefore energized, which causes the following to occur:

a. The +25 Vdc write current source is connected to the write heads. This enables the heads to write on tape.

b. A ground is placed on the write permit line to the controller. This line is designated file protect in the controller.

c. A ground is removed from the FILE PROTECT indicator on the operator control panel. This turns the indicator off.

With the file protect ring removed from the file reel, the write enable switch cannot close, and relay K6 is not energized. Therefore, the following conditions exist:

a. No write current is available to the write heads.

b. The write permit line is floating.

c. A ground is provided to the FILE PROTECT indicator. This turns the indicator on.

TAPE CLEANER. The tape cleaner, contained in the head assembly, consists of a slightly curved surface over which the oxide side of the tape passes. The curved surface has a sharp-edged hole pattern that removes dirt and foreign particles from the tape. Vacuum is connected to the rear of the hole pattern to dispose of the dirt and foreign particles.

3-16 MECHANICS

Three fundamental tape motions are necessary during normal station operation: forward, reverse, and rewind. Forward and reverse motions are performed during read or write operations. The tape is moved from one reel, past the read/write heads, to the other reel. Motion during a space operation is the same as for a read operation.

Tape motion is determined by a single capstan. The tape is continuously in contact with the capstan and moves only when the capstan rotates. The reel and capstan movements are isolated from each other by the loops in the vacuum storage chambers. Therefore, the capstan and the reels, with their respective tachometers, form separate but related mechanical systems. Figure 3-13 shows a block diagram of both the reel and capstan control electronics.

3-17 Capstan Motion (See figures 3-13 and 4-10)

The capstan system consists of a reference generator, ramp generator, tachometer, preamplifier, amplifier, and capstan motor. Capstan motions are controlled, through a feedback loop, by the capstan servo electronics. When a motion order is received from the controller, the reference generator triggers a ramp in the ramp generator. This ramp closely matches the output voltage of the capstan tachometer. The voltage difference between the ramp and the tachometer output is amplified by the preamplifier and the power amplifier. The amplified difference signal slows or accelerates the capstan motor. This change in motor speed affects the output voltage of the tachometer, which is mechanically coupled to the capstan motor. The increment in tachometer output is compared with the ramp, closing the feedback loop, and the process is repeated.

Capstan motion may be initiated in manual or automatic mode. When in manual, the CAPSTAN FWDS or REVS signal comes true, depending on the switch pressed on the operator or auxiliary control panel. Figure 3-14 shows the logic involved in this operation.

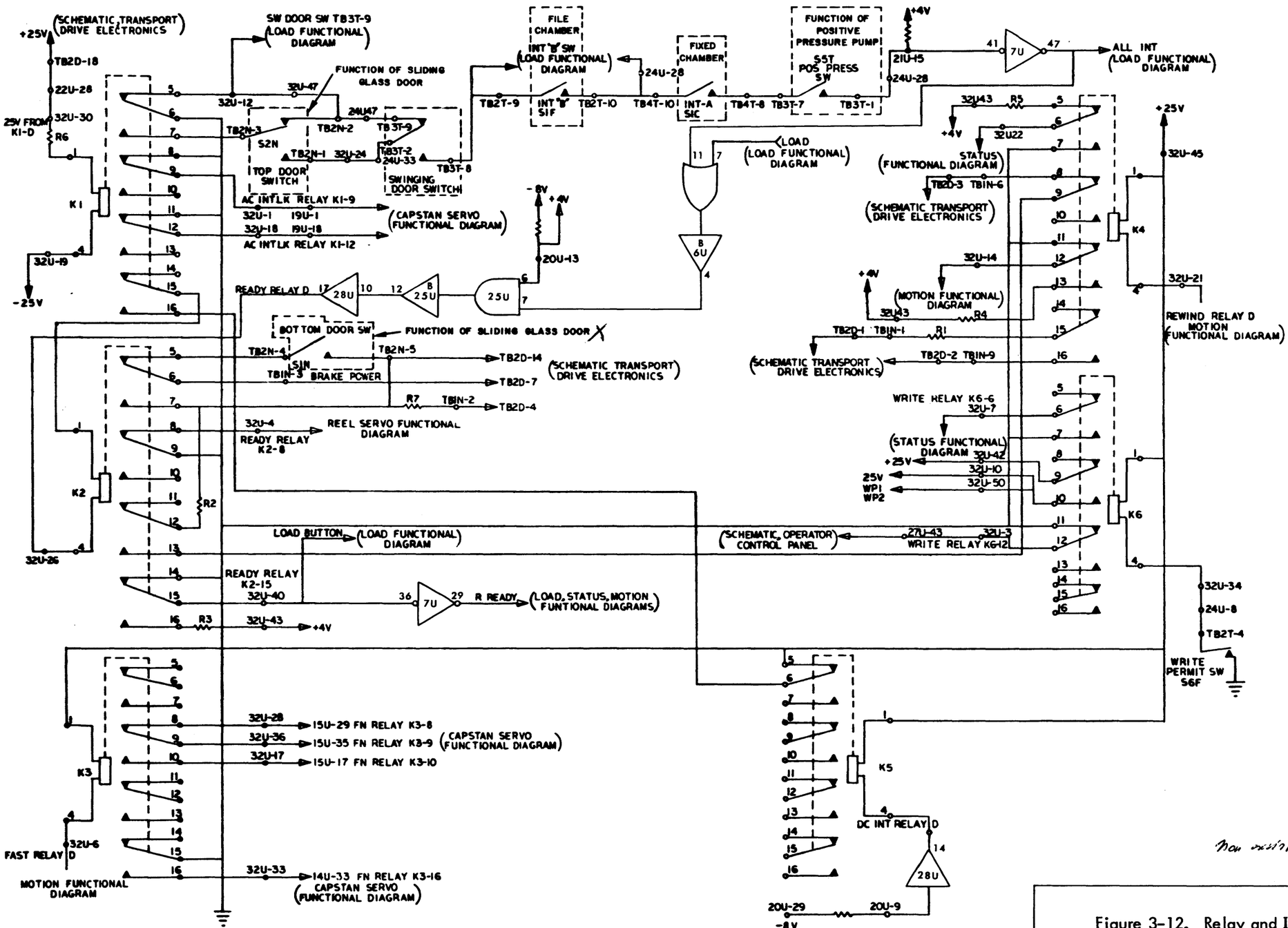
When motion is initiated in the automatic mode, the RVRC line, from the controller, comes true for reverse motion, or false for forward motion. This causes RVRS or NRVRS to be true, respectively. These two terms are AND-gated with term OSCTS on separate gates on the station logic (see figure 3-15). Term OSCTS comes true when the station enters state 0 after being selected. The outputs of these two gates cause the RVSS term to be true for reverse or false for forward motion. RVSS is AND-gated with START CONTR to produce term REVS. START CONTR is true if the station is in the automatic mode.

When reverse motion is specified by RVRS coming true, the RVSS term is latched true by NRVRS. This latch allows the controller to drop the RVRC direction control line to a particular station and still have motion maintained in that station. This action is required during motion delays.

Term REVS is true when reverse motion is required or false when forward tape motion is required. Terms REVS and NRVSS are AND-gated with the activate motor signal ACMS:

ACMS = START CONTR FS1S

Terms CAPSTAN FWDS and CAPSTAN REVS are originated from two separate branches of this circuit, as is shown in figure 3-14.



NOTE: REFERENCE SDS DWG: 135531-1A

Figure 3-12. Relay and Interlock Functional Diagram

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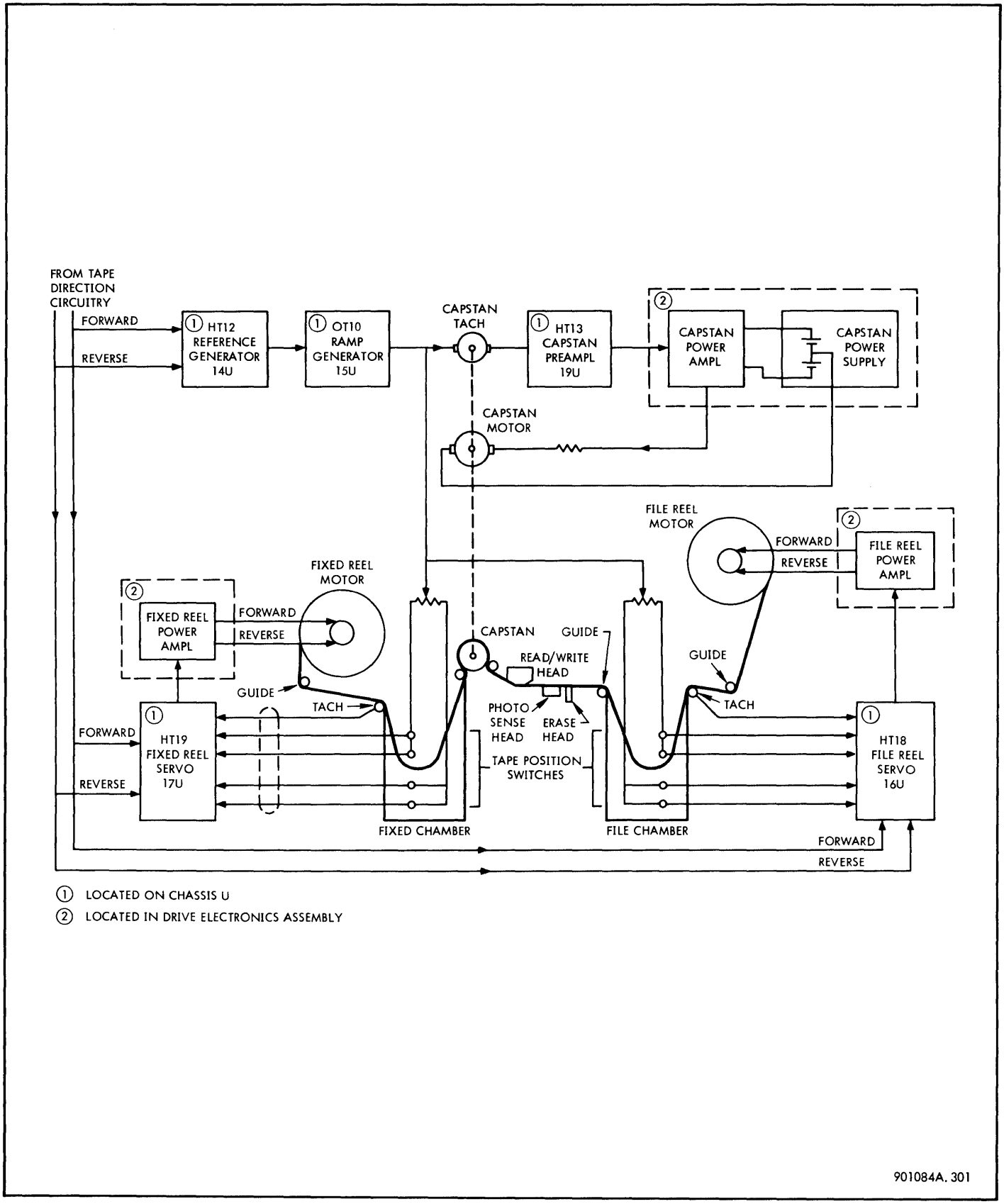
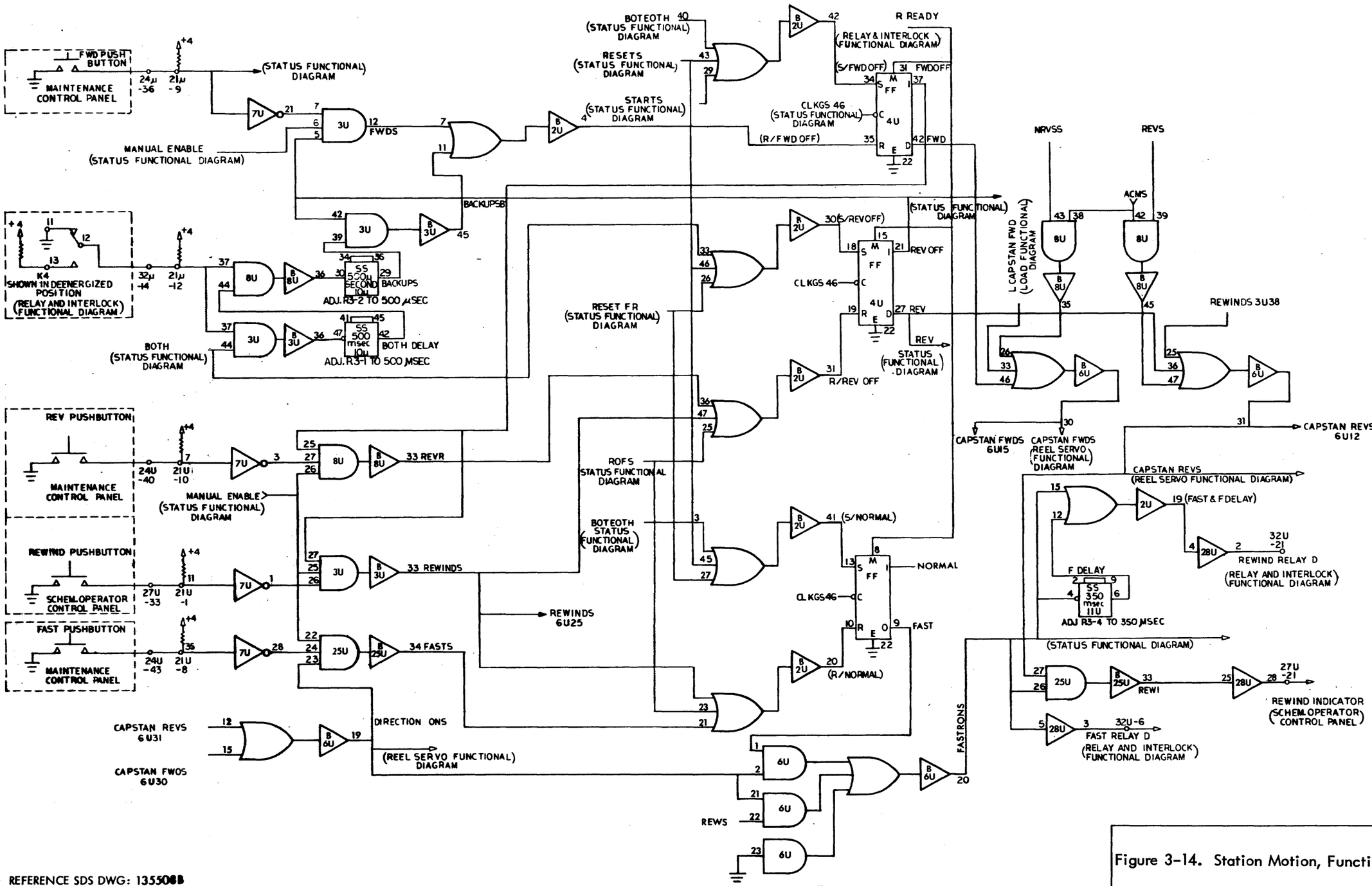


Figure 3-13. Station Transport Motion Control, Block Diagram



NOTE: REFERENCE SDS DWG: 1355088

Figure 3-14. Station Motion, Functional Diagram

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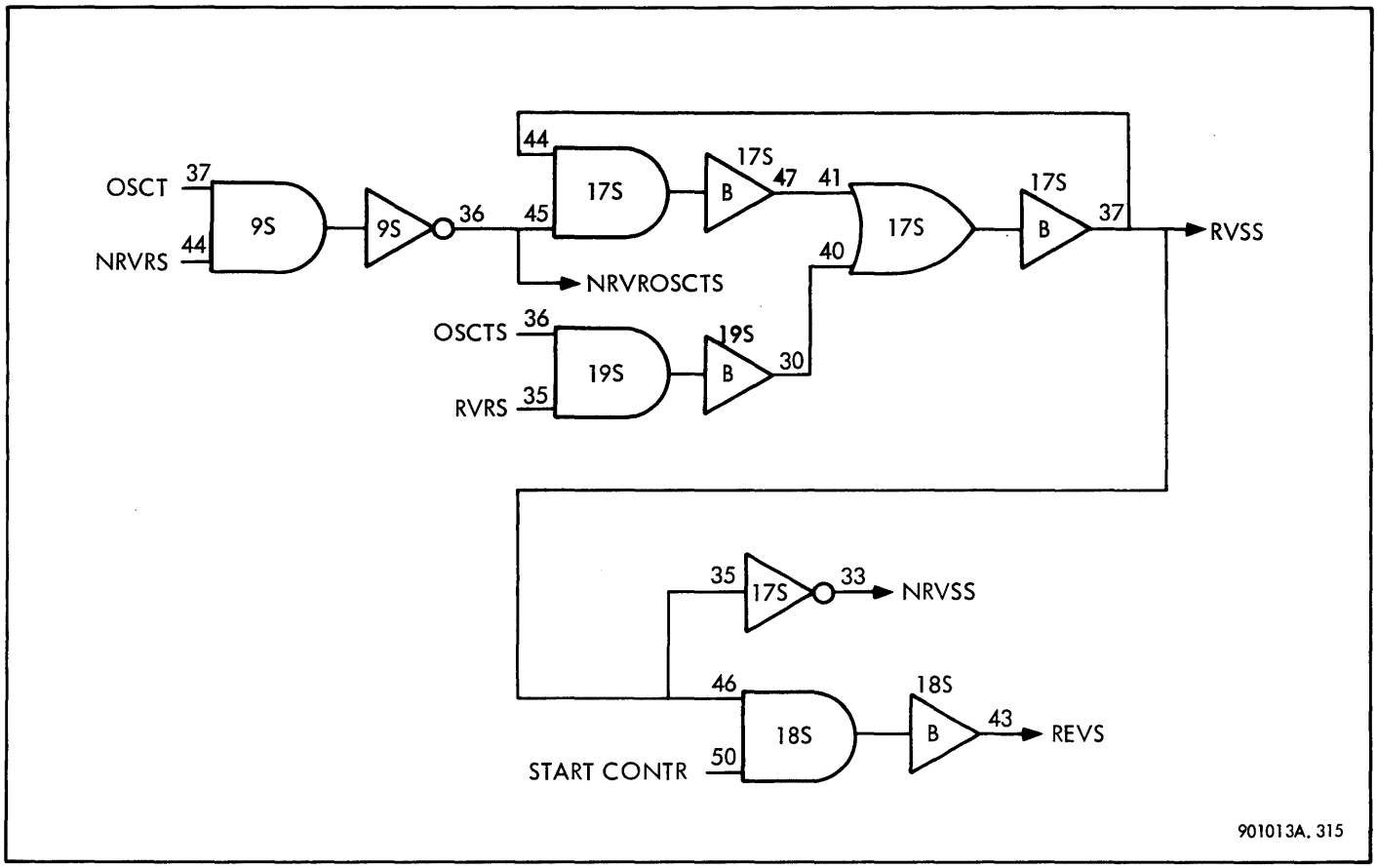


Figure 3-15. Direction Latch

START CONTR enable is true if the station is in the automatic mode. FS1S in the state counter is set on any operation that moves tape except off-line rewind. Therefore, NRVSS is true when REVS is false; and so either CAPSTAN FWDS or CAPSTAN REVS is true when tape movement is to take place. These signals are applied as inputs to the reference generator.

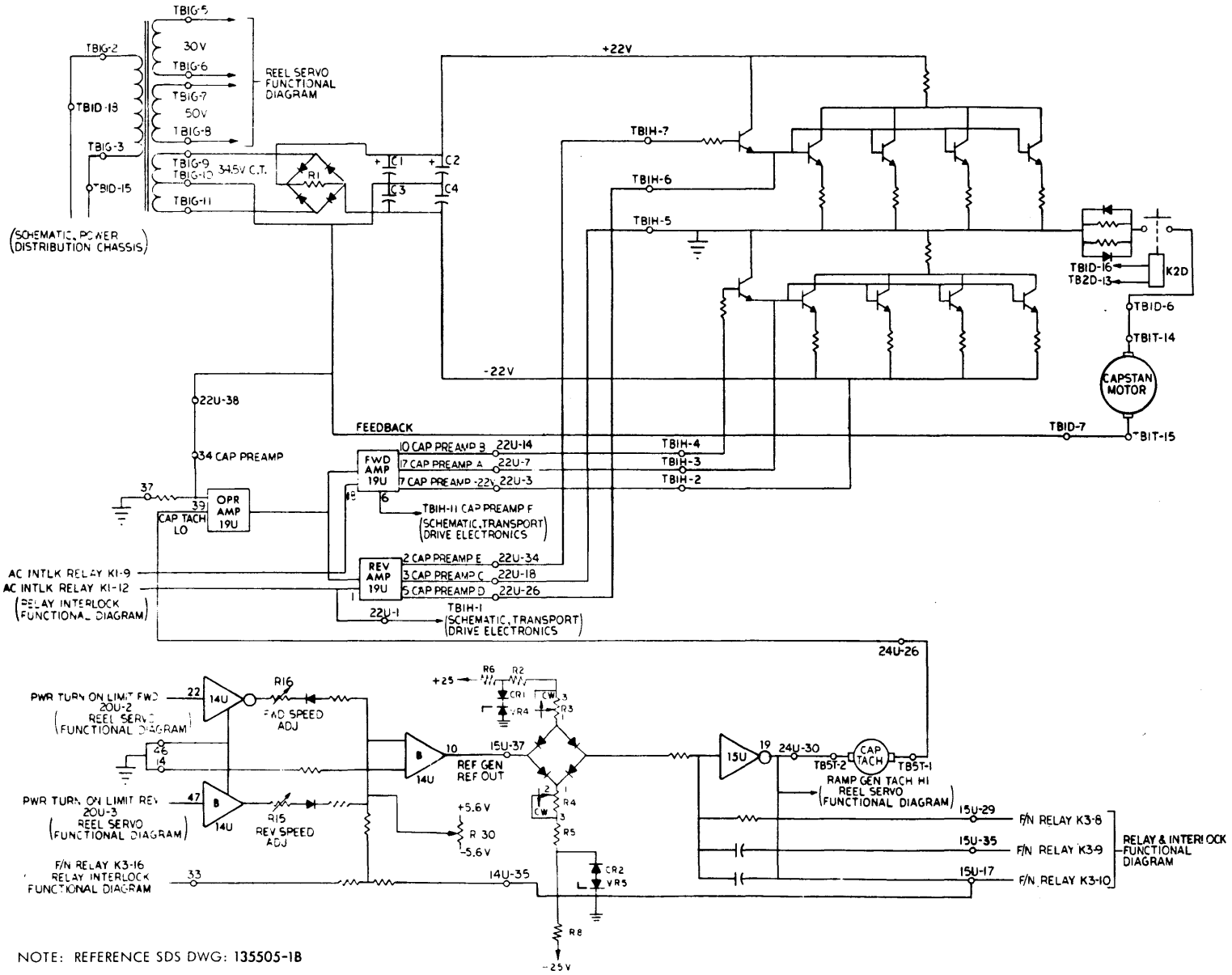
REFERENCE GENERATOR. The reference generator is contained in module HT12, chassis U. It is shown in figure 3-16 as part of the capstan circuitry. A buffer is connected to the reverse input line and an inverter to the forward input line. The output stage consists of a noninverting operational amplifier.

When a capstan direction signal is received in pin 22 for forward or pin 47 for reverse, either the buffer or inverter causes a reference current to appear at the summing point of the operational amplifier. Potentiometers R15 and R16 provide tape velocity adjustment. The voltage at the output of the operational amplifier is negative for forward motion and positive for reverse motion. This output, at pin 10 of 14U, is connected to the input of the ramp generator, pin 37 of 15U.

RAMP GENERATOR. (See figure 3-16.) Capstan acceleration and deceleration is determined by the slope of the output signal from the ramp generator. When accelerating to nominal speed, the ramp goes from zero to maximum amplitude in about 4 ms. During high-speed operation, the ramp goes from zero to maximum in approximately 1.7 seconds, in order to decrease the acceleration and allow the reel servo to maintain the loops in the vacuum chambers.

The ramp generator is contained in module OT10, chassis U. It consists of a diode bridge and an inverting high gain operational amplifier. If the input to the bridge is positive, a certain amount of current exists from the +25V supply into the amplifier. This produces a reverse tape motion condition. If the input is negative, a current path is established from the -25V supply into the amplifier. This produces a forward tape motion condition.

The amplitude and slope of the ramp are determined by a combination of resistors and capacitors in a feedback loop that is switched by relay K3 (see figure 3-12). For 75 ips operation, K3 is deenergized. This decreases the amplitude of the ramp and increases its slope. For 250 ips, high-speed operation, K3 is energized. This increases the amplitude and decreases the slope of the ramp. The output of the ramp generator is connected to the capstan preamplifier through the capstan tachometer.



NOTE: REFERENCE SDS DWG: 135505-1B

901013A.316

Figure 3-16. Capstan Servo, Functional Diagram

CAPSTAN TACHOMETER. (See figure 3-16.) The capstan tachometer is mechanically coupled to the capstan motor shaft, as shown in figure 4-10. The tachometer generates a voltage proportional to the capstan velocity. When the capstan is running, the tachometer senses capstan speed, and any variation causes correction signals to be applied to the capstan preamplifier. The capstan tachometer is connected between the ramp generator output and the input to the capstan preamplifier, module HT13. The voltage generated by the tachometer opposes the ramp voltage. The ramp voltage is also compared with the feedback signal from the capstan motor, and this differential signal is amplified by the capstan preamplifier.

CAPSTAN PREAMPLIFIER. (See figure 3-16.) The capstan preamplifier is contained in an HT13 module located in 19U. The input signal from the capstan tachometer is applied at pin 39. The feedback from the capstan motor appears at pin 34. The first stage is a differential amplifier which feeds its output into a complementary symmetry amplifier. One branch of the complementary symmetry amplifier drives the reverse power amplifier when the input is positive. The other branch drives the forward amplifier when the input is negative.

CAPSTAN AMPLIFIER. (See figures 3-16 and 4-28.) The capstan power amplifiers and respective power supplies are contained in the servo drive electronics chassis. The output of the reverse preamplifier is fed to the reverse power amplifier at TB1H-7, which consists of transistors Q1 through Q5. The forward preamplifier output goes to the forward power amplifier at TB1H-4, which consists of Q6 through Q10. Each of the power amplifiers has an associated power supply also contained in the drive electronics. There is a -22V power supply for the forward amplifier and a +22V supply for the reverse amplifier. Both supplies use the same bridge rectifier network consisting of CR9 through CR12.

The power amplifier amplifies the voltage difference originated between the ramp and the tachometer output. The output of both amplifiers is connected to the capstan motor, which responds by accelerating in the designated direction. The capstan tachometer, which is coupled to the capstan motor shaft, begins to generate a voltage that tends to equal that of the ramp reference voltage as speed increases. When the two voltages are equal, there is no input to the capstan preamplifier, so there is no output from the power amplifiers. The capstan motor then tends to decelerate, which causes the tachometer output voltage to decrease. This produces a voltage difference between the tachometer and the ramp generator outputs, and the process is repeated. By this method, short bursts of current are applied to the motor to maintain a constant velocity.

CAPSTAN MOTOR. (See figure 4-10.) The capstan is fixed to the shaft of a high torque, fast response, permanent magnet dc motor capable of rapid acceleration at a low level of power consumption. The vacuum in the chambers exerts tension to hold the tape in firm contact with the surface of the capstan during station operations.

3-18 Reel Motion (See figure 3-13)

The reel system consists of sensing switches, tachometers, servo electronics, power control, and reel motors. The reel system continuously controls the position of the tape loops and maintains the proper length of tape in the vacuum chambers. Refer to paragraph 3-15 for a description of vacuum chamber functions.

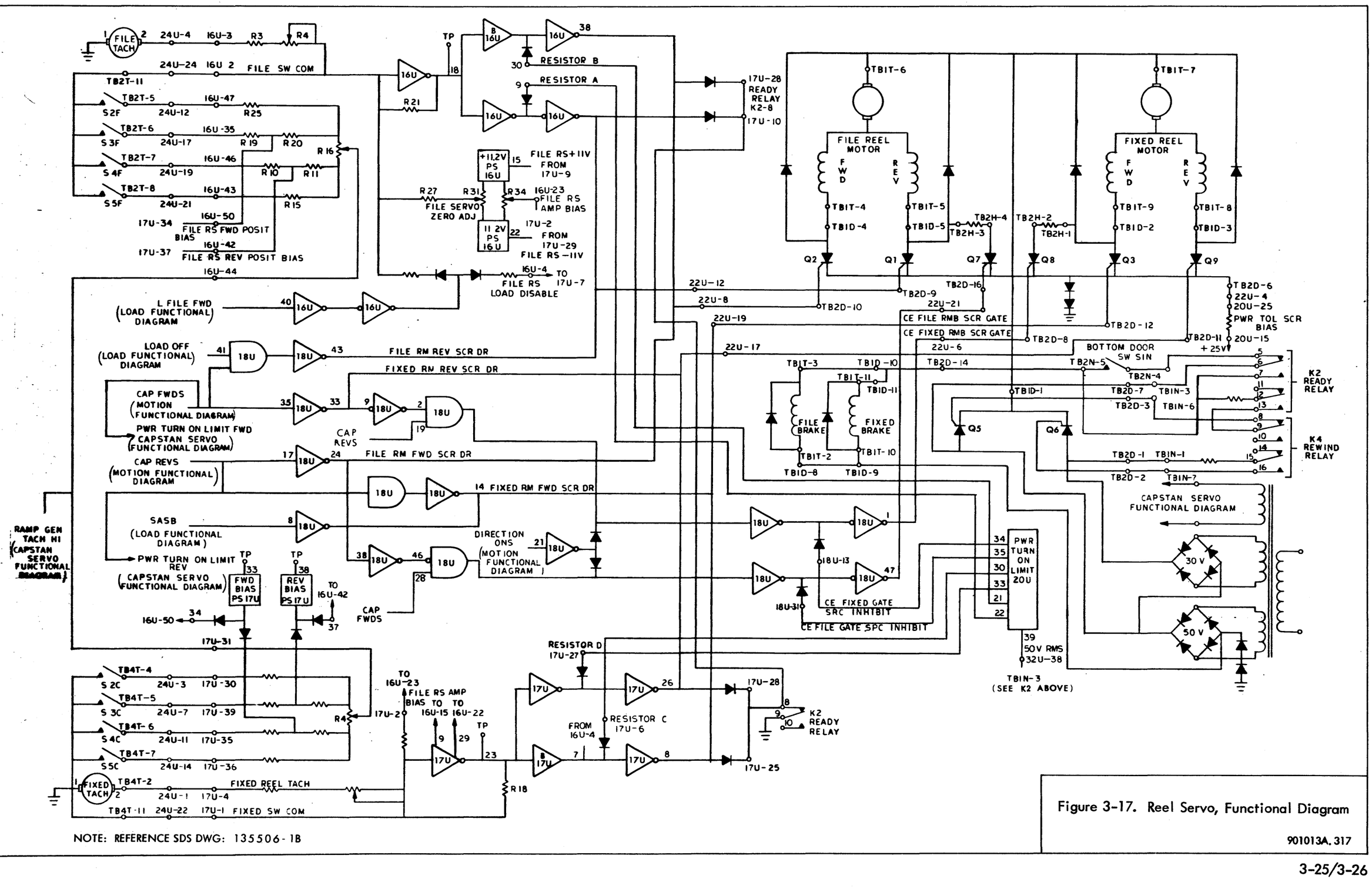
Reel motions are controlled by two separate servo electronics networks: the fixed reel servo and the file reel servo. The ramp generator output is connected to the input of both servo circuits, through the sensing vacuum switches in the vacuum chambers. The file and fixed reel tachometers produce an output voltage proportional to the tape velocity and opposite in polarity to that of the ramp generator output. Both voltages are applied to the same point at the input of the respective servo electronics circuit. Any difference between the tachometer and the ramp voltages, positive or negative, is amplified by the servo electronics.

The motor power control circuits are activated whenever a signal appears at the servo electronics outputs. When a certain tape velocity is reached, a minimum preset difference voltage is produced and accelerating voltage is then removed from the respective reel motor. As the tape speed is reduced, the tachometer output voltage changes, a voltage difference is produced, and power is again applied to the reel motor. The ramp voltage polarity determines forward or reverse reel motor rotation. During a rewind operation, high speed is achieved by increasing the power supply voltage to the reel motors. Figure 3-17 shows a functional diagram of the reel servo electronics.

SENSING SWITCHES. (See figure 3-17.) The operation of the servo electronics is a function of eight vacuum switches, designated S2F through S5F and S2C through S5C, identified as tape loop position switches. These switches, located in the vacuum chambers, sense the tape loop positions (see figure 3-18).

A vacuum switch operates by means of a diaphragm that closes or opens a pair of contacts when a pressure difference exists between its sides (see figure 3-19). Switches S1C, S2C, S3C, S1F, S2F, and S3F close when reduced pressure is applied at the vacuum orifice while the hole on the other side is at atmospheric pressure. Switches S4C, S5C, S4F, and S5F open under the same conditions. All switches are mounted with the vacuum orifice toward the vacuum chamber.

The tape loop in the vacuum chamber divides it into two compartments, the upper at atmospheric pressure and the lower at reduced pressure. When the station is in ready condition, the tape loops rest between S3C and S4C or S3F and S4F. All position switches are then open. A switch closes when the tape loop, in moving up or down the chamber, passes its respective sensing hole position. The closed switch provides a path for the ramp signal to appear at the summing junction of the servo electronics circuit input (see figure 3-17).



NOTE: REFERENCE SDS DWG: 135506-1B

Figure 3-17. Reel Servo, Functional Diagram

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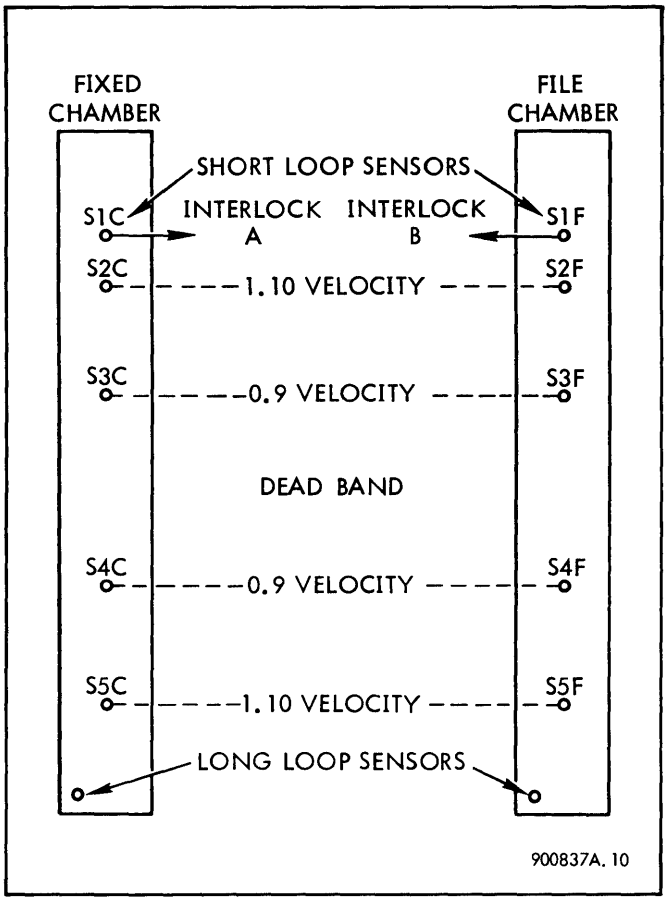


Figure 3-18. Vacuum Chamber, Tape Position Switches

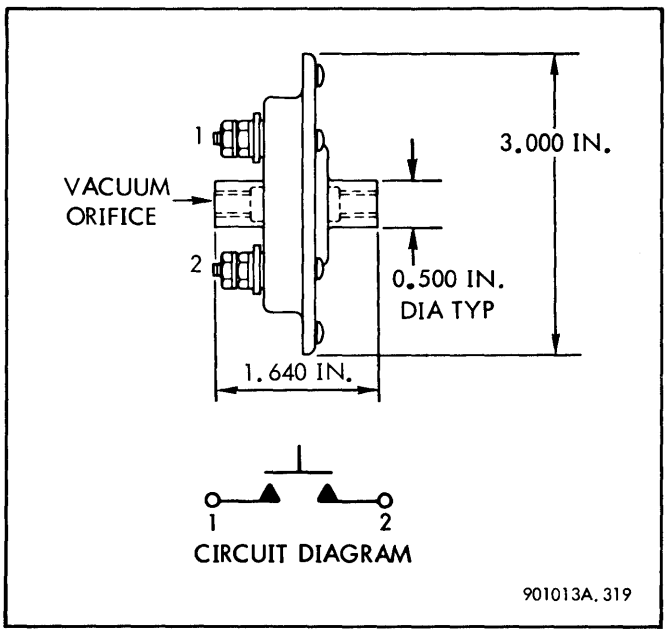


Figure 3-19. Vacuum Switch

Switches S2F, S3F, S4C, and S5C are active during forward tape motion; S2C, S3C, S4F, and S5F are active during reverse motion. When the transport is in standby condition, the tape loop in the file chamber is positioned between S3F and S4F, and the loop in the fixed chamber is between S3C and S4C. This area is called the tape motion dead band. A holding bias is applied to the summing junctions to prevent amplifier drift and tape creepage.

TACHOMETER. (See figure 3-17.) There are two tachometers in the reel system, the fixed reel tachometer and the file reel tachometer. The reel tachometers are mounted between the reel and vacuum chamber (see figure 3-13).

Both tachometers function in a similar manner. When the tape reel is mounted on the transport, the Mylar (back) side of the tape is threaded around the tachometer pulley. When the reel is in motion, tape movement causes the tachometer to rotate and generate a voltage proportional to the tape speed. The tachometer output is applied to the summing junction of the respective reel servo amplifier through a velocity adjustment potentiometer.

REEL SERVO ELECTRONICS. (See figure 3-17.) The fixed reel servo is an HT19 module located in 17U. The file reel servo is an HT18 module located in 16U. The reel servo modules receive the following input signals:

a. L FILE FWD on pin 40 of the HT18 module. This signal is received from the load logic when the loading sequence is in progress.

b. A reference input (RAMP GEN H1) on pin 44 of the HT18 module and pin 31 of the HT19 module. This is the signal from the ramp generator that is fed to the summing amplifier input junction through the tape position switches.

c. The tachometer inputs on pin 3 of the HT18 module and pin 4 of the HT19 module.

When a forward motion operation takes place, the ramp generator produces a positive ramp that is applied simultaneously to the capstan preamplifier and the reel servo electronics input. This initiates the following sequence of events:

a. The capstan begins to rotate forward, taking tape from the file chamber and depositing it into the fixed chamber at a rate determined by the slope of the ramp.

b. When the file chamber loop is drawn up past S3F, the switch closes and the ramp signal appears at the summing junction input of the file amplifier, where it is inverted and fed into a buffer amplifier. (The output of the first amplifier is actually sent to a buffer and an inverter, but the inverter is biased to reject the negative going signal.) The ramp is inverted again and fed to the gate of Q2, enabling it to drive the file reel forward.

c. The file reel tachometer is set into motion by the moving tape and a voltage is generated opposite in polarity to the reference input. When the velocity of the tape going into the chamber is 90% of the velocity of the tape leaving the chamber, the tachometer output is enough to cancel out the ramp voltage at the summing junction and remove the accelerating drive from the file reel motor.

d. The tape is still leaving the file chamber faster than it is being replaced by the file reel; consequently, the loop moves up to S2F, and S2F is closed. When S3F and S2F are both closed, the ramp voltage at the summing junction is raised to the point that the file reel velocity has to be increased until the tachometer output is great enough to cancel out the ramp. The velocity of the tape going into the chamber is then 110% of the velocity of the tape leaving the chamber.

e. With tape now being fed into the file chamber faster than it is being taken out, the tape loop descends below S2F and allows S2F to open. The file reel then slows the tape to its 90% velocity, the loop is drawn up by the capstan again, and the cycle keeps repeating as long as the capstan is moving forward.

The same sequence applies also to the fixed reel and chamber. The tachometer and reel functions are the same for both forward and reverse operations. In reverse operation, the polarity of the input signal changes and certain assignments in the servo electronics are transferred to different components, as follows:

a. Fixed reel motion is begun when the tape loop in the fixed chamber is pulled up across S3C, which allows the ramp signal to proceed to the input of the fixed servo electronics. Switches S3C and S2C then operate alternately, keeping the tape loop between them during the tape motion.

b. File reel motion is initiated when the loop in the file reel chamber drops below S4F, allowing the ramp signal to proceed to the input of the file servo electronics. Switches S4F and S5F then operate alternately, keeping the tape loop between them during tape motion.

c. The summing amplifier output is inverted and fed to the gate of the reverse SCR, enabling it to drive the reel in the reverse direction.

POWER CONTROL. (See figure 3-17.) All reel motor power control is achieved through the use of SCR's. Q1 and Q2 control file reel motor reverse and forward motions. Q3 and Q4 control fixed reel forward and reverse motions. Q5 connects the 50 Vdc power supply to the reel motor circuits during normal speed operation; Q5 is off during high-speed operations. Q6 connects the 30 Vdc power supply in series with the 50 Vdc power supply during high-speed operation; Q6 is off during normal speed operations. Q7 and Q8 permit the reels to decelerate gradually after a motion takes place. During standby, Q7 and Q8 provide a small steady current to the reel motors so that they pull the tape in opposite directions with enough force to compensate for the pull in the vacuum chambers.

The outputs from the reel servo electronics in modules HT18 and HT19 are applied to the motion control SCR's from the following points:

a. File reel reverse amplifier output, on HT18 pin 1.

b. Fixed reel reverse amplifier output, on HT19 pin 26.

c. File reel forward amplifier output, on HT18 pin 38.

d. Fixed reel forward amplifier output, on HT19 pin 8.

To prevent undesired reel motion when the transport is not ready for operation, the reel servo outputs are clamped to ground by diodes through the normally closed contacts 8 and 9 of ready relay K2. When K2 is energized, the servo electronics outputs are ungrounded.

Power Turn-On Limit. The function of the power turn-on limit circuit is to prevent the reel motion control SCR's from being turned on at the peaks of the power supply voltage. This avoids excessive turn-on current surges and resulting transients. The circuit is contained in module WT18, located at U20.

The pulsating dc voltage of the 50V power supply is sensed and input at pin 39. Whenever the pulsating voltage reaches a 30V level, the power turn-on limit outputs (pins 34, 35, 30, 33, 21, and 22) are raised from a ground potential to +8 Vdc. This voltage is applied to the drivers of Q1, Q2, Q3, Q4, Q7, and Q8, preventing them from turning on the SCR's. As soon as the pulsating voltage cycles to a level lower than 30V, the drivers are again enabled to trigger the SCR's. Once an SCR is turned on, it remains on regardless of gate drive.

Coast Enable. The function of the coast enable circuit is to switch Q7 and Q8 on or off at the times when a change of tape motion is required. Q7 and Q8, in turn, partially energize the reel motor reverse and forward windings, to provide adequate deceleration. During standby, Q7 and Q8 provide a current of 1A to their respective motor windings in order to keep the tape motionless.

When the capstan is being driven forward, the tape position switches cause the file reel to rotate in the same direction until the reel velocity exceeds the capstan velocity. At this time the file reel forward SCR driver signal goes to zero, and the following events take place in the logic circuit:

a. The low input signal from the file reel forward SCR drivers fed to the inverter on pin 38, slot 18U, results in a high output, which feeds to the input of an AND gate.

b. The high capstan forward signal on pin 30, slot 6U, feeds to the other gate input, pin 28, slot 18U, enabling the gate to feed a high input to the buffer.

c. The buffer output enables SCR Q7, allowing current to flow through the reverse winding of the file reel motor. This current is limited by the series resistor to a value that permits the reverse winding to decelerate the motor gradually.

When the capstan is driven in the reverse direction, the inputs are on pins 9 and 19, and Q8 is enabled to allow limited current flow through the forward winding of the fixed reel motor, which causes the motor to decelerate gradually. When there is no capstan drive command present, the direction ONS signal from pin 19, slot 6U, is low. This causes pin 21, slot 18U, in the WT16 coast enable module to be low. The output of the inverter connected to pin 21, slot 18U, goes true. This causes Q7 and Q8 to be forward biased, thereby producing approximately 1 amp of current through the file reel motor reverse and the fixed reel motor forward windings. The torque developed by the 1 amp of current plus the brake drag is enough to counteract the tape tension due to the vacuum. This keeps the tape motionless in the tape motion dead-band portion of the chamber.

MOTOR AND BRAKE. (See figures 4-7 and 4-12.) The reel is driven by a dc series motor with separate field windings to control forward and reverse motion. A friction brake is attached to the rear of the motor. Reel motion is prevented when no power is applied to the brake. This situation exists when ready relay K2 is deenergized and the sliding front door is closed or when transport power is lost.

Reel motion is permitted when power is applied to the brake. This situation exists when K2 is energized, or when K2 is deenergized and the sliding front door is pushed down to the fully open position, thereby closing the bottom door switch.

REEL SERVO POWER SUPPLY. (See figures 3-17 and 4-28.) The reel servo power supply is located in the tape transport drive electronics chassis. It furnishes driving power for the reel motors and brakes. Circuit protection is provided by dc interlock relay K1. Dc power comes from two full-wave rectifier circuits, providing 50 volts and 30 volts, respectively. The 50 Vdc supply is used to drive the motors at nominal speed and to supply brake power. For high-speed operation, the two supplies are cascaded to provide greater driving power.

3-19 Fast Motion

When an on-line rewind operation is to be initiated or when fast tape motion is started from the auxiliary control panel, the term FASTRONS comes true (see figure 3-14). This enables the fast motion circuitry by making the K4 relay driver go false. The coil of K4 is then provided with a return path and K4 is energized (see figure 3-12). Under this condition, the following events take place:

a. Contacts 8 and 9 open. This leaves the gate of Q5 open (see figure 3-17).

b. Contacts 15 and 16 close. This turns on Q6, which turns off Q5 and places the 30V and the 50V supplies in series.

c. Contacts 12 and 13 close. This provides a dc enable signal to the backup circuitry in the station motion control logic (see figure 3-14).

d. Contacts 6 and 7 close. This disables the load point AND gate that turns on the LOAD indicator driver (see figure 3-22).

During a normal speed operation, K4 remains energized until the tape stops with the BOT marker located at the sensing head. At the end of a rewind operation, the BOT marker is detected, but due to the high speed of the tape, the BOT marker overshoots the photosense head before it stops. Therefore, the tape has to be moved back until the BOT marker is located at the sensing head. To prevent a false load point indication, K4 is kept energized until the BOT marker is backed up.

REWIND CIRCUIT. (See figure 3-14.) During an on-line rewind, the term REWS is AND-gated with signal DIRECTION ON, which causes the term FASTRONS to go true. When the BOT marker is first detected while rewinding, term REWS goes false, making FASTRONS go false.

During an on-line rewind operation, when the BOT marker is detected, the FAST signal from 4U-9 goes low, causing FASTRONS to go false. Enable 45SS is true. When FASTRONS goes low, K4 is deenergized and the backup circuit is disabled after a 500 ms delay produced by a single shot-designated F delay. This action provides enough time for the tape to decelerate.

BACKUP CIRCUIT. (See figure 3-14.) The function of the backup circuit is to produce a forward movement that places the BOT marker over the photosense head after a rewind operation. The backup circuitry is utilized only during fast reverse tape motion. When the leading edge of the BOT marker is detected after a fast reverse tape motion operation, the term BOTH comes true. This enables the BOTH delay single shot:

BOTH DELAY = BOTH REWIND RELAY OFFS

The term REWIND RELAY OFFS is true when K4 is energized.

The trailing edge of the BOT marker triggers the BOTH delay. This takes place approximately 4 μs after the leading edge of the BOT marker is detected. The BOTH DELAY single shot goes true for 500 ms. The purpose of this delay is to allow the tape to decelerate before the backup motion begins. The output of the BOTH delay single shot is AND-gated with an enable signal that is true when

K4 is energized. This output is fed to a 500 μs single shot delay that produces term BACKUPS:

BACKUPS = BOTH DELAY REWIND RELAY ONS

The REWIND RELAY ONS enable is true as long as the fast relay is energized. The fast relay remains energized until the fast relay delay times out.

The equation for BACKUPS denotes that terms BOTH DELAY and REWIND RELAY ONS must come true to provide a trigger to the one-shot. However, the one-shot is triggered only when one of the two input terms goes false. Neither term goes false until approximately 350 ms have elapsed after the detection of the BOT marker. This is enough time to allow the tape to decelerate. The 10 μs BACKUPS single shot is then triggered.

When the BACKUPS term comes true, it is AND-gated with term REV OFF to produce the BACKUPS B input to the FWD flip-flop reset terminal. The REV OFF term comes true whenever the BOT marker is detected. Therefore, the FWD flip-flop is reset to apply capstan forward motion when the term BOTH DELAY times out, since the rewind relay stays energized. The capstan moves the tape forward until the BOT marker is again detected. At this time, the BOTEOTH enable comes true and sets the FWD flip-flop. Capstan power is then removed and the tape stops.

3-20 Load Operation

Loading the transport with a tape reel initiates the functional operation of the magnetic tape system. The loading procedure is described in paragraph 2-14. The main features of the load operation are the push-on, pull-off (POPO) reel hub and the automatic loading function.

POPO HUB. (See figure 3-20.) The baseplate of the hub assembly is attached to the reel turntable by shoulder screws that permit limited movement between the hub and turntable. Within the assembly three equally spaced radial arms form knuckle joints with a center post connected to the turntable. The outer ends of the arms are pivoted to sliding blocks, or shoes, that are guided in radial channels and retained by a circumferential rubber ring. In an unloaded condition, the assembly is held away from the turntable by pivot arm movements resulting from ring pressure on the shoes. When a tape reel is slipped over the assembly and pressed against the baseplate flange, axial movement pivots the arm to force the shoes outward and compresses the ring between the shoes and the reel hub. Continued axial movement causes toggle action of the arms to lock the assembly against the turntable.

LOAD FUNCTION. (See figure 3-21.) When the LOAD switch is pressed, an input is applied to reset the load flip-flop to the load state, provided that the swinging front door is shut and the ready relay is deenergized. The station should not be ready when a load operation is begun because in a ready condition the vacuum chambers are empty, which causes interlocks A and B to open. The clock input to the load flip-flop comes from the controller during normal operation. When the LOAD switch is pressed, an input is also provided to trigger the SAS one-shot, which goes true for 500 ms. This provides a signal to the fixed reel servo preamplifier in slot 17U that prevents the fixed reel from turning. This one-shot is also input to an inverter on the set input to the load flip-flop. As long as the one-shot is timing out, it will not provide a true input to the set side of the load flip-flop. With the load flip-flop reset, the following occurs:

a. The reset output of the load flip-flop provides an enable to the relay driver in slot 28U that drives the ready relay regardless of the interlock system. The ready relay is energized, which causes power to be applied to the reel servo brakes. This action releases the brakes.

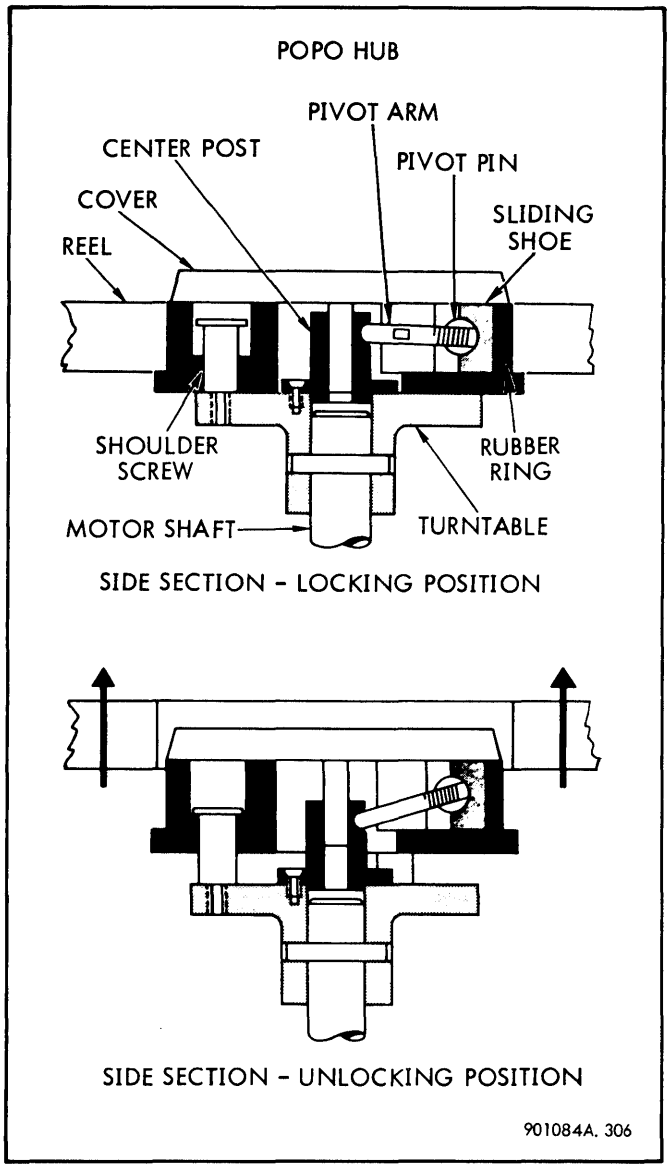
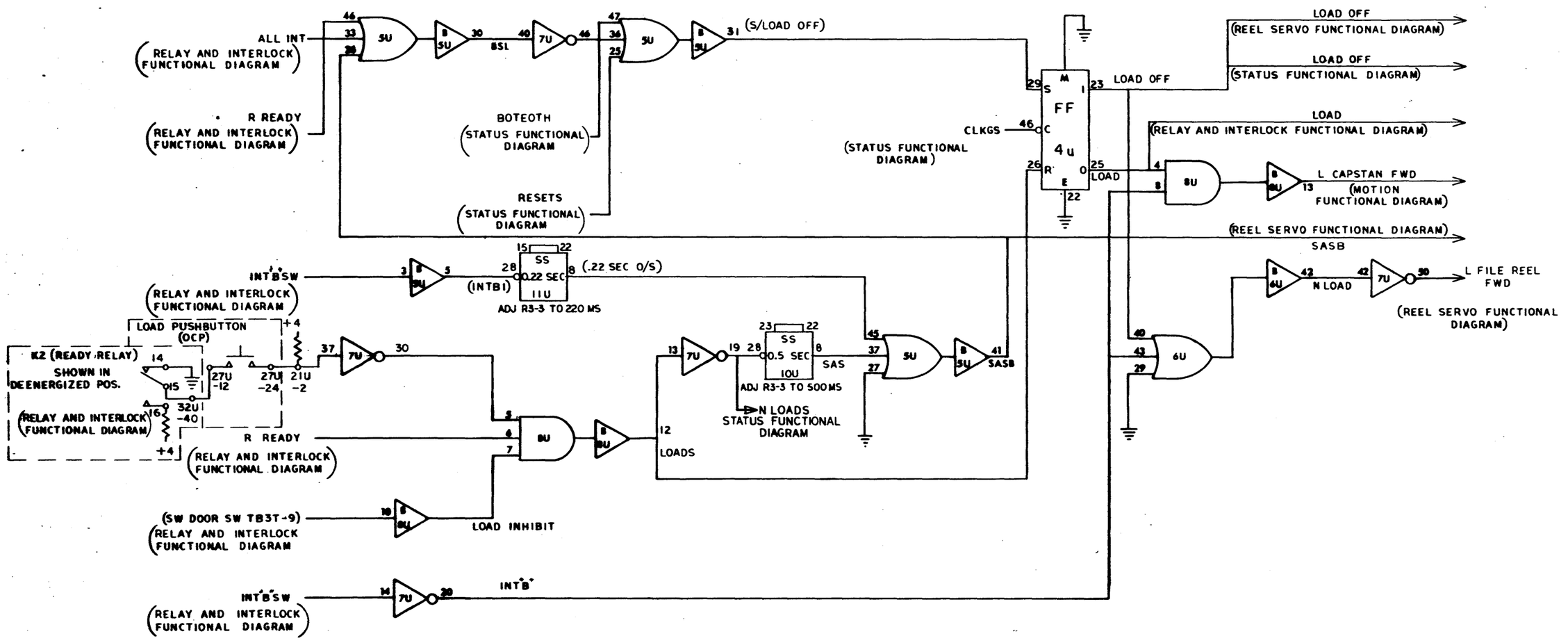


Figure 3-20. POPO Hub Assembly



NOTE: REFERENCE SDS DWG: 135907-18

Figure 3-21. Load, Functional Diagram

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b. The set output of the load flip-flop causes the output of an inverter in slot 7U to go true. This provides a forward file reel signal to be applied to the file reel servo in slot 16U. The file reel starts turning in the forward (clockwise) direction, thereby feeding tape into the file reel vacuum chamber.

c. The set output of the load flip-flop disables the gate in slot 3U that produces term OPERATIONAL CONTR. This prevents the station from performing any operation until the load operation is completed.

d. The set output of the load flip-flop disables the input to an inverter in the coast enable circuitry in slot 18U. The output of this inverter goes true and enables the reverse servo circuitry in the file reel servo. This allows the file reel to decelerate under full power. Deceleration under full power is necessary because the file reel motor is accelerated up to approximately 100 ips before the tape reaches interlock B. When interlock B closes, the capstan forward signal controls both the capstan speed and reel motor speed. Because the reel motor speed is much higher than the 75 ips, the low decelerating torque applied by the count system is not great enough to bring the reel motor speed down to 75 ips within the available chamber length.

e. When the tape enters the file vacuum chamber, the INTB (interlock B) vacuum interlock switch closes and initiates the following:

1. A true INTB1 input is provided, which triggers a 220 ms one-shot located in slot 11U. The one-shot goes true for 220 ms. This provides a signal to the fixed reel servo in slot 17U that prevents the fixed reel from turning. Tape is thereby safeguarded from being pulled out from the fixed chamber while it is being loaded. This 11U one-shot is also input to an inverter on the set input to the load flip-flop. As long as this one-shot is timing out, it does not provide a true input to the set side of the load flip-flop.

2. An INTB enable is AND-gated with the reset output of the load flip-flop to provide a capstan forward signal to the capstan direction and velocity circuitry. The capstan starts accelerating in the forward (counterclockwise) direction, which feeds tape into the fixed reel vacuum chamber.

3. An INTB enable is provided to an inverter in slot 7U, the output of which is the file reel forward signal. The inverter output goes false, which removes the file reel forward signal from the servo and allows the ramp generator tachometer high signal to take over control of the reel servo.

f. When the tape enters the fixed vacuum chamber, the interlock A (INTA) vacuum interlock switch closes. This completes the interlock network, which causes a ground to be connected through the ac interlock relay, top door switch, swinging door switch, INTB = INTA, and positive pressure switch to the input of an inverter in slot 7U. The output of this inverter, all interlocks closed (ALL INT), goes true. Term ALL INT is applied as an input to an inverter on the set input to the load flip-flop to prevent it from setting before the BOT tab is reached.

g. The tape settles into the fixed and file vacuum chambers and continues to move in a forward direction under capstan control until the BOT marker is detected. When the BOT marker is detected, the load operation has been functionally completed and must be terminated by the setting of the load flip-flop to the load off condition. BOT detection causes term BOTEOTH to come true, which sets the load flip-flop. When the load flip-flop is set, the following occurs:

1. The capstan forward signal goes false, which stops tape motion.

2. The disable is removed from the operational control gate.

3. The load enable is removed on the input to the ready relay driver. The ready relay should not deenergize, however, because of the ALL INT signal being true at this time.

4. The LOAD indicator on the control panel should light. At this point, the complete load operation is finished.

Protective logic circuitry is provided to terminate the load operation if one of the following malfunctions exists:

a. Interlock B is not closed because tape was not fed properly into the file vacuum chamber. The 500 ms SAS single shot times out and resets the load flip-flop.

b. Interlock B is closed properly, but interlock A is not closed because tape was not fed properly into the fixed chamber. The 220 ms single shot times out and resets the load flip-flop.

c. At the time that both single shots time out, the ready relay remains energized and the interlock network is open. Terms R READY and ALL INT are false and the load flip-flop is set.

d. The BOT marker is not detected. The tape moves in the forward direction until the EOT marker is detected or the RESET switch is pressed on the operator control panel.

3-21 HEADS

There are three heads in the magnetic tape station: the read/write head, the erase head, and the photosense head. The read/write head handles data detection and recording. The erase head permits the erasing of previously recorded data. The photosense head detects the beginning and end of the useable portion of tape. The heads are located along the tape path on the tape transport, as shown in figure 2-6.

3-22 Read/Write Head (See figure 4-17)

The read and write heads comprise a single assembly that includes a tape cleaner. Each head consists of a stack of seven coils with laminated cores. The core gaps are aligned perpendicularly to the transport casting, within a maximum deviation of 150 μin. Both heads are placed side by side with the gap lines separated by approximately 0.30 in. The read head is placed after the write head, relative to forward tape motion, so that information can be detected by the read head 4 ms after it is written on the tape, at a tape speed of 75 ips.

3-23 Erase Head (See figure 4-16)

The erase head, energized during write operations only, removes all information previously recorded on the tape. The erasure takes place from the Mylar (uncoated) side of the tape and across the full width of the tape. Erasing is accomplished when the tape comes into contact with the head gap while the head coil is energized with a specified current of 60 mA. The resultant erasure leaves a trace of the previously recorded data. The ratio of the residual signal voltage to the originally recorded level is greater than -40 dB.

3-24 Photosense Head (See figures 3-22 and 4-14)

The photosense head consists of a light source and two photoelectric transducers. These transducers are photosensitive transistors which detect the light reflected by the markers placed at the beginning and end of tape. The BOT marker actuates one of the photoelectric elements and the EOT marker actuates the other (see figure 2-3).

BOT DETECTION. When the BOT marker passes over the lamp, light is reflected from the marker to one of the two photoelectric transistors. The transistor detects this light and provides an input to the BOT sense amplifier module, AT28, located at 13U. The sense amplifier then produces the following signals: BOTH, LOAD POINT CONTR, LOAD POINT INDICATOR, and BOT EOT H. These signals are used to initiate a backup operation (after rewind), light the LOAD indicator, and stop tape motion.

EOT DETECTION. When the EOT passes over the lamp, light is reflected from the marker to the other phototransistor. The transistor detects this light and provides an input to the EOT sense amplifier located at 13U. The sense amplifier then produces the signals EOT CONTR and BOT EOT H, which are used to stop tape motion. Figure 3-22 shows the functional generation of these terms.

3-25 MOTION ELECTRONICS

The electronic circuits and their operations described in paragraphs 3-26 through 3-32, are located in the modules contained in chassis S of the station electronics (see figure 1-2). The operation and description of the station data electronics, located in the modules contained in chassis U, is given under the heading Magnetic Tape System Functions, paragraphs 3-57 through 3-60.

3-26 Delay Count Register (See figure 3-23)

The purpose of the delay count register is to provide various delay times necessary for the correct operation of the magnetic tape station. The delay counter consists of 12 gated flip-flops and their associated input logic. The flip-flops are designated FC01S through FC12S.

The initialize count register term, ICRS, comes true when the delay count register is to be used:

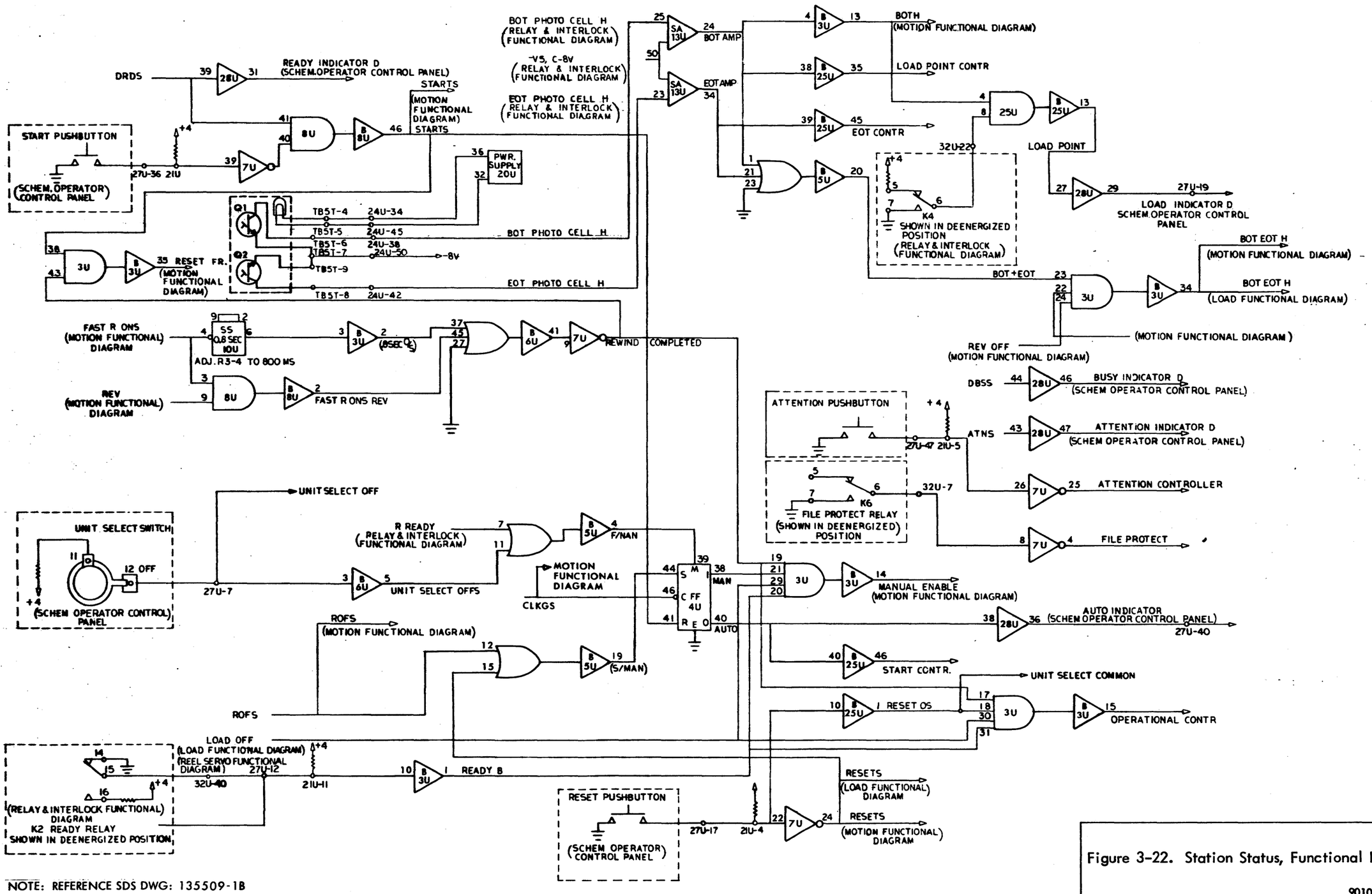
$$ICRS = 0SCTS + 07SS$$

Enable 0SCTS is true in state 0. Enable 07SS is true in state 7. Therefore, the count register is initialized whenever the station enters state 0 or 7. When ICRS comes true, flip-flops FC05S through FC12S are reset, and flip-flops FC01S through FC04S are set. This configuration constitutes the initialized condition.

FC01S through FC12S are connected as a binary counter, with FC12S producing the least significant count. The maximum delay obtainable is approximately 70 ms. However, the maximum delay used in the station is approximately 51 ms. This is the delay required for an erase operation. The delay counter is clocked by the master clock signal input to FC12S. This signal originates in the controller and produces a count approximately every 16 μs. The delays are generated by using different configurations of the counter. The delay times and associated states and instructions are listed in table 3-2.

Table 3-2. Delay Count Register Data

State	Delay Time	Instruction
0	16.7 μs	Rewind off-line/on-line, with interrupt
0	16.7 μs	Read, write, space forward
0	16.7 μs	Write, space reverse
6	51.3 ms	Erase, BOT read
6	6.5 ms	Write
6	29.9 ms	BOT read/space
6	5.5 ms	Read/space
3	5.3 ms	Forward ending delay
6	2.9 ms	Reverse delay
2	5.3 ms	Reverse ending delay



NOTE: REFERENCE SDS DWG: 135509-1B

Figure 3-22. Station Status, Functional Diagram

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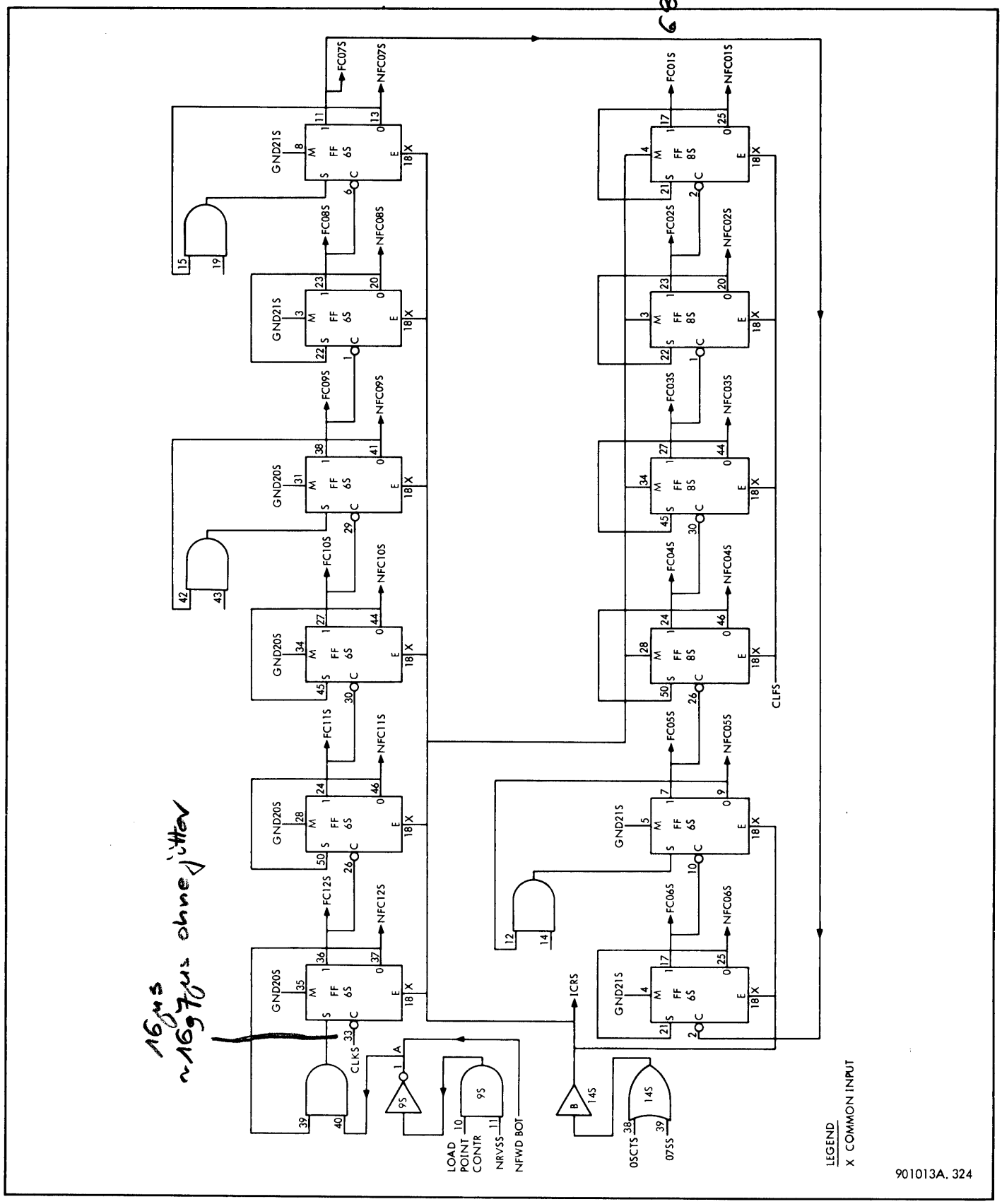

Figure 3-23. Delay Counter, Logic Diagram

3-27 State Counter

The state counter consists of four gated flip-flops designated as FCTS, FS1S, FS2S, and FS3S with associated logic circuitry. Flip-flop FCTS is referred to as the select or connect flip-flop. Whenever an operation is to be performed on a station, it must first be selected from the controller. A station is selected when flip-flop FCTS is set. Figure 3-24 shows a logic diagram of the state counter.

Flip-flops FS1S through FS3S determine which of the eight possible states the station is in at a given time. The state number designation (0 through 7) is directly related to the binary configuration of FS1S, FS2S, and FS3S, with FS3S being the least significant bit of the binary configuration. Table 3-3 lists the flip-flop configuration and functions for each station state.

STATE COUNTER FUNCTION DURING WRITE OPERATION. When a write operation is to be performed, neither the WN1C nor WN2C line comes true from the controller. This causes both terms WN1S and WN2S to be false in the station and inverted NWN1S and NWN2S terms to be true.

Term NWN2S is AND-gated with OSCTS on the set input to the FS1S flip-flop. Term OSCTS, which is true in the selected station, is AND-gated with the clock input to FS1S, and flip-flop FS1S is therefore set. At the same time, flip-flop FS2S is set because of the NWN1S NWN2S OSCTS gate on the set input.

Table 3-3. State Counter Data

State	Configuration	Function
0	NFS3S, NFS2S, NFS1S, FSCT	Station selection
1	FS3S, NFS2S, NFS1S, NFSCT	Backup delay
2	NFS3S, FS2S, NFS1S, NFSCT	Reverse stop delay
3	FS3S, FS2S, NFS1S, NFSCT	Forward stop delay
4	NFS3S, NFS2S, FS1S, NFSCT	Rewind without interrupt
5	FS3S, NFS2S, FS1S, NFSCT	Rewind with interrupt
6	NFS3S, FS2S, FS1S, FSCT	Prerecord delay
7	FS3S, FS2S, FS1S, FSCT	Space, read, or write

With FS1S and FS2S set, the station is in state 6. State 6 is known as the forward prerecord, read or write delay, or reverse postrecord delay state. The purpose of state 6 is to ensure the attainment of proper tape speed so that proper gap exists between records. The state counter remains in state 6 for approximately 6.5 ms. This period is the amount of time it takes for the delay counter to reach an FC05S set, FC09S set, and FC04S reset configuration. When this configuration is reached, term SFS3S comes true on the set input to the FS3S flip-flop:

S/FS3S = SFS3S FCTS
FCTS = True in selected station
SFS3S = 06SS NERSS TWRS
06SS = True in state 6
NERSS = True if the erase signal is false from the controller and no BOT is detected
TWRS = WRTS, FC05S, FC09S, NFC04S

Flip-flop SFS3 is set, which causes the station to enter state 7.

STATE COUNTER FUNCTION DURING READ OPERATION. When a read operation is to be performed, neither line WN1C nor WN2C comes true from the controller. This causes terms WN1S and WN2S to be false in the station. Term NWN2S is AND-gated with OSCTS on the set input to the FS1S flip-flop. Term OSCTS, which is true in the selected station, is also applied as the clock input to the FS1S flip-flop. The FS1S flip-flop is therefore set. At the same time, flip-flop FS2S is set because of the NWN1S NWN2S OSCTS gate on the set input.

With FS1S and FS2S set, the station is in state 6. In this state, the device proceed signal, DPRS, is prevented from being sent to the controller after a read operation is initiated for a period of approximately 5.5 ms. This prevents noise generated during gap time from being read by the controller. The 5.5 ms period is the amount of time it takes for the delay counter to count to an FC06S set, FC09S set, and FC04S reset configuration. When this configuration is reached, term SFS3S comes true on the set input to the FS3S flip-flop:

S/FS3S = SFS3S FCTS
FCTS = True in selected station
SFS3S = 06SS TRDDS
06SS = True in state 6
TRDDS = NWRTS TRDS
NWRTS = True in a read operation
TRDS = NFC04S FC09S FC06S NERSS
NERSS = True on a read except when the beginning of tape marker is detected

The FS3S flip-flop is set, causing the station to enter state 7.

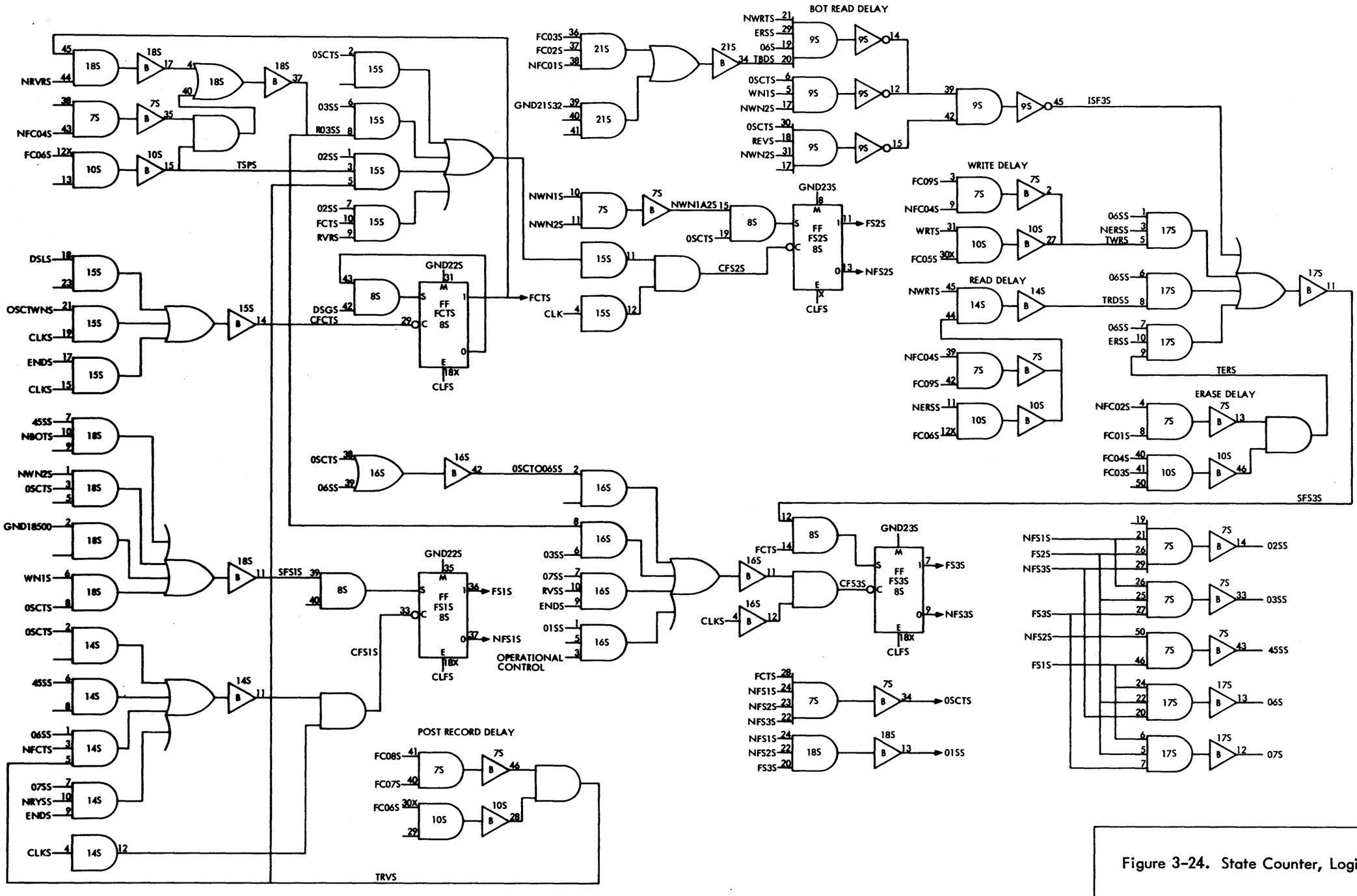

Figure 3-24. State Counter, Logic Diagram

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STATE COUNTER FUNCTION DURING REWIND OPERATION. When an on-line rewind without interrupt is desired, lines WN1C and WN2C come true from the controller to the station. This causes the WN1S and WN2S line receiver output terms to be true and the inverted NWN1S and NWN2S terms to be false. Term WN1S is AND-gated with OSCTS on the set input to the FS1S flip-flop in the state counter. OSCTS is also applied as a clock enable to the FS1S flip-flop. OSTS comes true in the selected station. Therefore, the FS1S flip-flop is set to on-line without interrupt operation. The FS2S and FS3S flip-flops remain reset. This state counter configuration places the station in state 4. The station will remain in state 4 until the completion of the rewind because the 45SS NBOTS latch gate on FS1S holds FS1S set until the BOT marker is detected, at which time the set input is disabled and the 45SS CLKS input clocks FS1S to the reset state. The 45SS enable is true in state 4 or state 5.

When an on-line rewind with interrupt is to be initiated, the WN1C line is true and the WN2C line is false from the controller to the station. This causes term WN1S and inverted term NWN2S to be true and the WN2S and inverted NWN1S terms to be false in the station logic. Term NWN2S is AND-gated with OSCTS on the set input to the FS1S flip-flop in the state counter. OSCTS is also applied as a clock enable to the FS1S flip-flop. OSCTS comes true in the selected station. Therefore, the FS1S flip-flop is set to on-line rewind with interrupt operation.

Terms WN1S and NWN2S are AND-gated with OSCTS to produce, through a network of gates, an SFS3S input to the set side of flip-flop FS3S in the state counter:

S/FS3S = SFS3S FCTS

The FCTS enable is true because the FCTS flip-flop is set in the station selected for the rewind operation. The state 0 OSCTS enable, which is true in the selected station, is AND-gated with the master clock from the controller, CLKS, to provide a clock input that sets flip-flop FS3S. The FS2S flip-flop remains reset. Therefore, an on-line rewind with interrupt operation causes the state counter to be set to an FS1S set, FS2S reset, and FS3S set configuration. This state counter configuration places the station in state 5, where the rewind operation is initiated. When the BOT marker is detected, the 45SS NBOTS latch gate on FS1S is disabled, and the 45SS clock input causes FS1S to reset. At this time, FS3S is still set and the station enters state 1.

3-28 Station Selection

Station selection is performed during on-line operations. To select a station for a particular operation, the FCTS connect flip-flop must be set:

S/FCTS = DSGS NFCTS

The DSGS enable is the output of the device selection gate (see figure 3-25):

DSGS = DSCS DSSS DRDS

The DSCS enable is the output of the device select call circuitry. This circuitry compares the station number (0 through 7) determined by the unit select switch on the control panel with the DVXR, unit number, and line from the controller. No two units on a given controller will have the same unit select switch setting; therefore, only one unit responds to the particular DVXR line. The true DVXR line is determined from a command issued by the CPU. The DSSS enable is true from the controller to all connected stations. It indicates than an operation is to be performed, e.g., read, or write. The DRDS enable is the output of the device ready circuitry in the station logic (see figure 3-25):

DRDS = Operational control NFCTS NFS1S

The operational control enable originates in the transport logic station. It is true if the station is not involved in a rewind, tape load, or reset operation and if the ready relay in the transport control circuitry is energized. The ready relay is energized if proper voltages are present and all the interlocks are closed. Enable NFCTS is true if the connect flip-flop is reset. This enable essentially indicates that the station is not already selected for a previous operation. Enable NFS1S is true except when the FS1S flip-flop is set during a forward prerecord delay, reverse postrecord delay, space, rewind, read, or write operation.

There are latch gates on both DSGS and DRDS terms. The latch gate in both cases is enabled by a signal from the controller. With all the above conditions true, the DSGS station selected term comes true, enabling the set input to FCTS, and the term is transmitted to the controller:

C/FCTS = DSLS

The device select line, DSLS, comes true from the controller after the controller responds to the selected signal, DSGS, from the tape station. Therefore, if all the above conditions are met, the FCT select flip-flop will set. The FCTS flip-flop remains set until the completion of the operation, except in the case of a rewind. The resetting of FCTS is known as station deselection.

3-29 Station Deselection

A station remains selected until the completion of the operation being performed, except in the case of a rewind operation. To deselect a station at the termination of an operation, the FCTS connect flip-flop must be reset:

C/FCTS = ENDS CLKS

The ENDS enable comes true from the controller after the completion of the operation being performed. This is true for either successful or unsuccessful terminations. Enable CLKS is the output of the free-running master clock circuitry in the controller:

S/FCTS = DSGS NFCTS

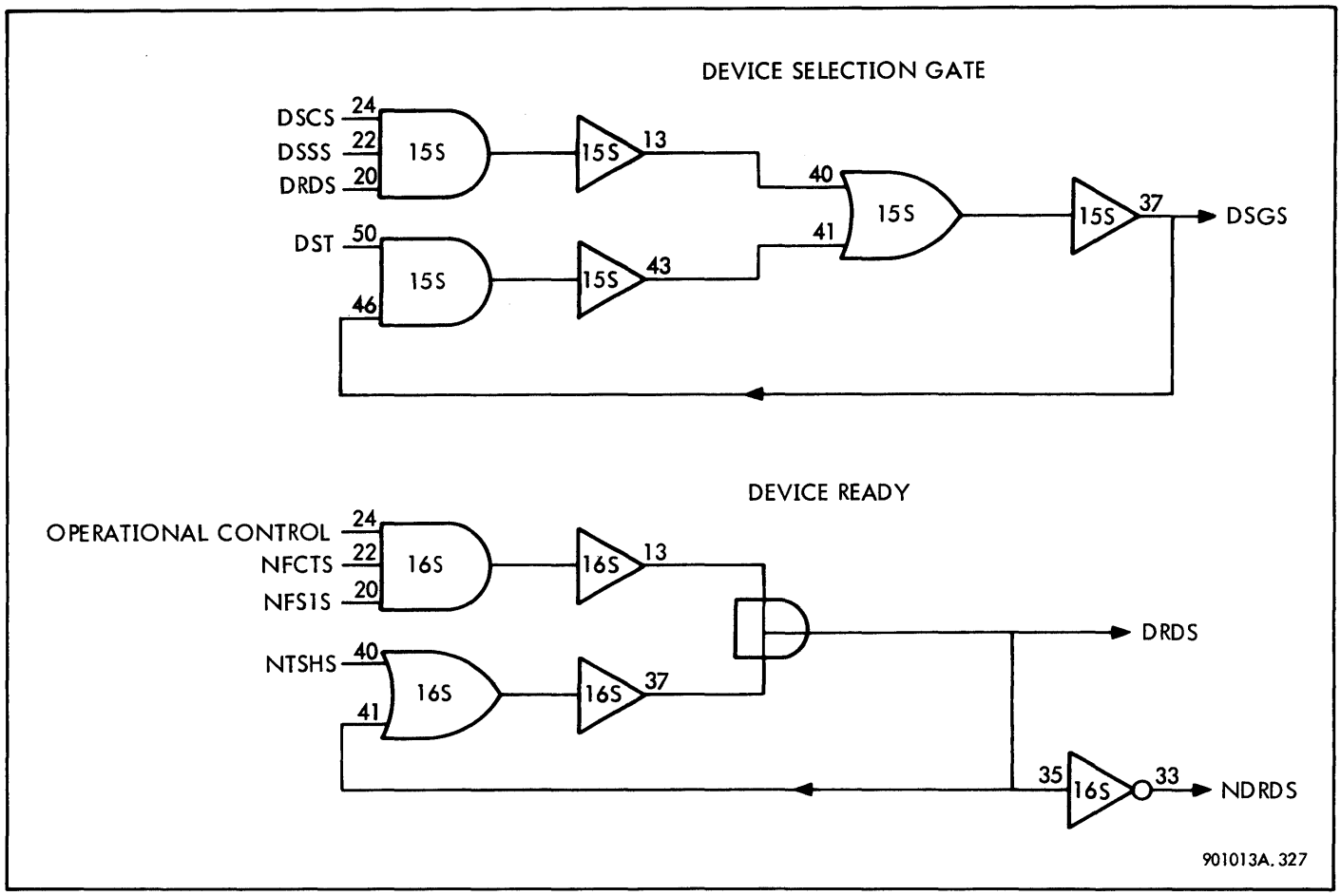


Figure 3-25. Device Selection and Device Ready, Logic Diagram

Enable NFCTS, on the set input, is false because the FCTS flip-flop was set at the start of the operation. Therefore, the FCTS flip-flop is reset when ENDS comes true from the controller, thereby causing the station to be deselected.

A station remains selected until the termination of any operation other than a rewind. In the case of a rewind operation, this is not necessary, so the FCTS connect flip-flop is reset at the start of the rewind operation:

C/FCTS = OSCT WNS CLKS

OSCT WNS = OSCTS WNIO2S

The CLKS enable is produced by the free-running master clock in the controller. Term NWN1S, NWN2S, or both are false from the controller, making the WNIO2S enable true when a rewind operation is to take place. The OSCTS enable is true in the selected station. Therefore, term OSCTWNS comes true, producing a clock input to the FCTS flip-flop. When the FCTS flip-flop was set during station selection, the NFCTS enable to the FCTS set input went false. At OSCTWNS clock time, therefore, the set input is disabled and FCTS is reset. This ensures that the FCTS enable to the read amp cable drivers is removed. This prevents any data line interference from the rewinding station with another station that may be selected by the controller during rewind time. Therefore, in a rewind operation, the station is selected for only the short period of time that the FCTS flip-flop is set. During this time, the rewind logic is triggered, and the controller assumes that fast reverse tape motion has been initiated. The controller can therefore service other units during rewind time.

3-30 Rewind Operation

The three types of rewind operation that may be performed on the tape station are these:

a. Rewind on-line without interrupt

b. Rewind on-line with interrupt

c. Rewind off-line

REWIND ON-LINE WITHOUT INTERRUPT. The state counter is set to an FS1S set, FS2S reset, and FS3S reset, state 4 configuration for an on-line rewind without interrupt operation. FS1S is AND-gated with NFS2S to produce term

45SS, which, in turn, is applied as an input to the gate that produces rewind signal REWS. The FS1S flip-flop is set (FS1S) and the FS2S flip-flop is reset (NFS2S) only when the station is to perform a rewind:

REWS = NBOTS 45SS

Enable NBOTS is true if the BOT marker is not being detected by the photosense head. This enable ensures that a rewind cannot be initiated if there is no more tape to wind.

When the REWS signal comes true, it is applied as an enable to the fast tape motion circuitry.

Term REWS is input to a two-term AND gate that produces term FASTRONS:

FASTRONS = REWS DIRECTION ONS

The DIRECTION ONS enable is true as a result of the capstan REVS (reverse) line being true. Term REVS comes true in state 4 when the active motor signal ACMS is AND-gated with the true reverse line from the controller. When the FASTRONS term comes true, the fast tape speed circuitry is enabled. When REVS comes true in state 4 along with the activate motor signal (ACMS), reverse power is applied to the capstan motor to produce reverse motion.

REWIND ON-LINE WITH INTERRUPT. The FS1S flip-flop is set, FS2S is reset, and FS3S is set immediately after station selection during a rewind on-line with interrupt. This places the station in state 5. In state 5 the activate motor signal, ACMS is AND-gated with the reverse signal from the controller to initiate reverse tape motion. The fast circuitry is also energized so that the tape moves at 250 ips. This action is initiated in the same manner as for the rewind without interrupt operation. Figure 3-26 shows a block diagram of the rewind on-line with interrupt operations.

The difference between the two on-line rewinds is that with interrupt, the IOP wants to know when the rewind has been completed so that it may service the station. In this case, the station must transmit an interrupt signal to the controller at the completion of the rewind operation. This is accomplished as follows: the FS1S flip-flop in the state counter has been set while tape is rewinding in state 5:

S/FS1S = SFS1S

SFS1S = 45SS NBOTS

The 45SS enable is true in state 5. The NBOTS enable is true until the BOT marker is detected, at which time NBOTS goes false, disabling the set input on FS1S. Term 45SS provides a clock input to FS1S, and it resets, dropping motor power (NACMS). This action leaves only FS3S set, which causes the station to enter state 1.

The purpose of entering state 1 is to prevent an interrupt signal from being transmitted to the controller during backup time. To leave state 1, the FS3S flip-flop must be reset:

C/FS3S = CFS3S

CFS3S = 01SS OPERATIONAL CONTROL CLKS

The 01SS enable is true in state 1. The operational control enable, however, is inhibited for approximately 800 ms after the detection of the BOT marker:

OPERATIONAL CONTROL = LOAD OFF
RESET OS
READY B
REWIND
COMPLETED

REWIND COMPLETED = BRC

BRC = 0.8 sec O/S (timed out) + FAST ON REV

The above equation indicates that if the 0.8 sec one-shot is triggered, the operational control is false. The 0.8 sec one-shot is triggered by the trailing edge of the term FAST R ONS, which occurs when BOT is detected. Therefore, the FS3S flip-flop cannot be reset and the station cannot leave state 1 for 800 ms. This is enough time for tape backup to take place.

Interrupt to Controller. When the FS3S flip-flop resets, an NFS3S enable is provided to an AND gate in the INTDS interrupt latch circuitry:

INTDS = INTS

INTS = (Inverter) NINTS

NINTS = (Inverter) NFS3S INGS B
+ (NGNTS NTSHS START CONTR)

The interrupt gating enable, INGS, comes true in state 1 every 16 μs because of the 01SS CLK input gate. Enable NTSHS is true from the processor if the controller is not currently responding to an SIO, TIO, or HIO instruction. NGNTS is true if the controller is not currently requesting device addresses from interrupting stations. The START CONTR enable is true if the station is on-line.

The same clock that resets the FS3S flip-flop to exit state 1 provides an INGS input to the interrupt circuitry. Term INGS is latched as long as LINGS is true. When OPERATIONAL CONTR or NRSTS goes false or the DSCS AIOCDS gate is enabled, the INGS interrupt gate goes false. If the NGNTS, NTSHS, and START CONTR terms are true at this time, an INTDS interrupt signal is transmitted to the controller. This interrupt signal is latched by an INTS INGS gate. The interrupt signal is transferred through the controller to the processor.

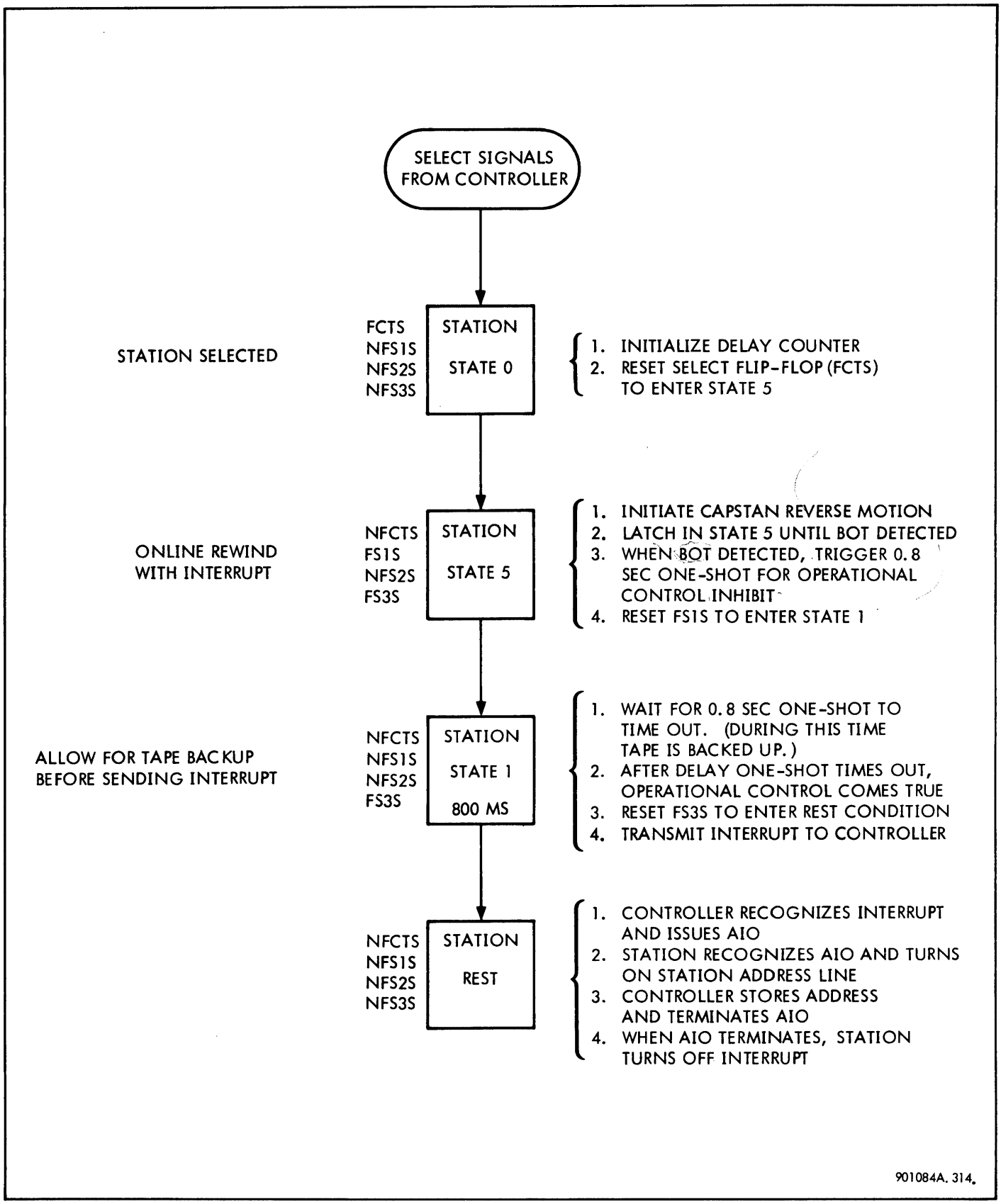


Figure 3-26. Rewind On-Line With Interrupt, Block Diagram

Interrupting Unit Number to Controller. After interrupt line acknowledgement, the processor issues an acknowledge interrupt instruction (AIO), causing the GNTS line to come true from the controller to the station. Term GNTS is applied as an enable to device-number-to-address-line gating circuitry in all the stations connected to the particular controller. The station address lines to the controller are designated DV0DS through DV7DS. For the purpose of explanation, it is assumed that station 0 is the interrupting station:

DV0DS = GNTS UNIT SELECT SWOC INTS

GNTS is true from the controller. The UNIT SELECT SWOC enable is true from the unit select switch on the operator control panel in the unit that has been allotted number 0. Enable INTS is true if the rewind on-line with interrupt operation has been completed. The DV0DS address line, therefore, comes high to the controller. This line informs the controller that station 0 is interrupting. During the acknowledge interrupt instruction, the AI0CDS line comes true from the controller. This causes the AI0CDS DSCS gate to be enabled, which removes the interrupt latch, thereby dropping the interrupt line from the station. It should be noted that more than one station may have the interrupt line high at any given moment. In this case, more than one of the address lines comes high when the AIO instruction is generated. The station interrupt from the lowest station address is recognized by the controller. The controller recognizes the highest priority address line, with station 0 having the highest priority and station 7 the lowest priority.

REWIND OFF-LINE. The rewind off-line order from the IOP causes the following to occur:

a. Term ROFS comes true, to store the rewind order in the station transport reverse and rewind flip-flops.

b. The station remains in state 0.

c. The station is placed in the manual mode.

This order gives the programmer the ability to rewind a unit and place it in the manual mode. It could be used to protect a tape upon which information had just been written.

3-31 Erase Operation

A programmed erase operation takes place when a portion of tape must be erased before new data can be written onto tape. An erase operation also takes place automatically when tape is in the load point (BOT) position and a write operation is initiated. In this case, approximately 3-1/2 inches is erased.

PROGRAMMED ERASE BEFORE WRITE. If an erase order is issued by the processor, the erase flip-flop is set in the controller. If this order is immediately followed by a write or write tape mark order, the station is selected, tape motion is initiated, and the following occurs: with the erase flip-flop set in the controller, the erase term, RASC, is true from the controller, which causes RASS to be true in the station. Term RASS is applied as an input to the tape erase, ERSS, circuitry:

ERSS $\stackrel{I}{=}$ NERSS

NERSS $\stackrel{I}{=}$ RASOBOTS 0SCTS + ERSS FCTS

Enable RASOBTS is true if the erase flip-flop is set in the controller. Enable 0SCTS comes true when the station enters state 0 after being selected by the write order following the erase order. When ERSS comes true, it is latched by a gate with input enables FCTS and ERSS. The FCTS connect flip-flop is set throughout the write operation.

The following describes the difference between the erase before write and the normal write operation. The essential difference is in the starting delay time (state 6). The station exit from state 6 to state 7 in a write operation takes place in 6.5 ms. In the erase before write operation, the exit from state 6 to state 7 does not take place for 51.3 ms. To exit from state 6 to state 7, the FS3S flip-flop must be set:

FS3S = SFS3S FCTS

FCTS = True in selected station

SFS3S = 06SS (state 6) ERSS (erase) TERS

TERS = FC04S FC03S NFC02S FC01S

The delay counter that began counting when the station entered state 6 does not reach a FC04S, FC03S, NFC02S, and FC01S configuration for 51.3 ms. Therefore, the FS3S flip-flop is not set, and the station does not exit state 6 until 51.3 ms have elapsed. Throughout this 51.3 ms period, the write enable term, WENS, is true, which causes erase head current to flow, and results in 3.5 inches of tape being erased. Write head current also flows at this time, which erases the portion of tape between the write and erase heads.

LOAD POINT (BOT), AUTOMATIC ERASE. The ERSS tape erase circuitry is also enabled by LOAD POINT CONTR, which is true with the tape positioned at load point:

ERSS $\stackrel{I}{=}$ NERSS

NERSS $\stackrel{I}{=}$ RASOBOTS 0SCTS

Enable RASOBOTS is true if the tape is positioned at load point. Enable 0SCTS comes true when a station enters state 0 after being selected. When ERSS comes true, it is latched by the ERSS and FCTS gate. When the station enters state 6 on a write operation with the tape at load point, it does not exit to state 7 for 51.3 ms, 3-1/2 inches of tape is erased, and a gap of 0.94 inches of erased tape is left between the BOT marker and the first data character.

3-32 Spacing Operation

The space record and space file operations are identical in all respects to a read operation at the station. In either case, the data read from tape to the controller is not transferred to the IOP. This transfer inhibit is a function of the space order.

3-33 CONTROLLER

The controller portion of the magnetic tape system consists entirely of the modules contained in chassis V, W, Y, and Z (see figure 1-2). Chassis V and W enclose the modules which contain circuitry for handling the system's data transfer operations. Chassis Y and Z enclose the modules which contain circuitry for controlling the system's interface and motion operations. Figure 3-27 shows a block diagram of the magnetic tape controller.

The main functions of the controller are to send and receive data from the CPU through the IOP, and to control the tape motions by directing appropriate orders to the stations. These functions are carried out in eight conceptual states as determined by the state counter. Figure 3-28 shows a block diagram of the controller states.

The magnetic tape controller can be functionally divided into three main circuit units: interface, motion, and data. The interface operation, communication and service cycles, and controller states are described in paragraphs 3-34 through 3-56. The data handling circuits are described under the heading Magnetic Tape System Functions (paragraphs 3-57 through 3-70).

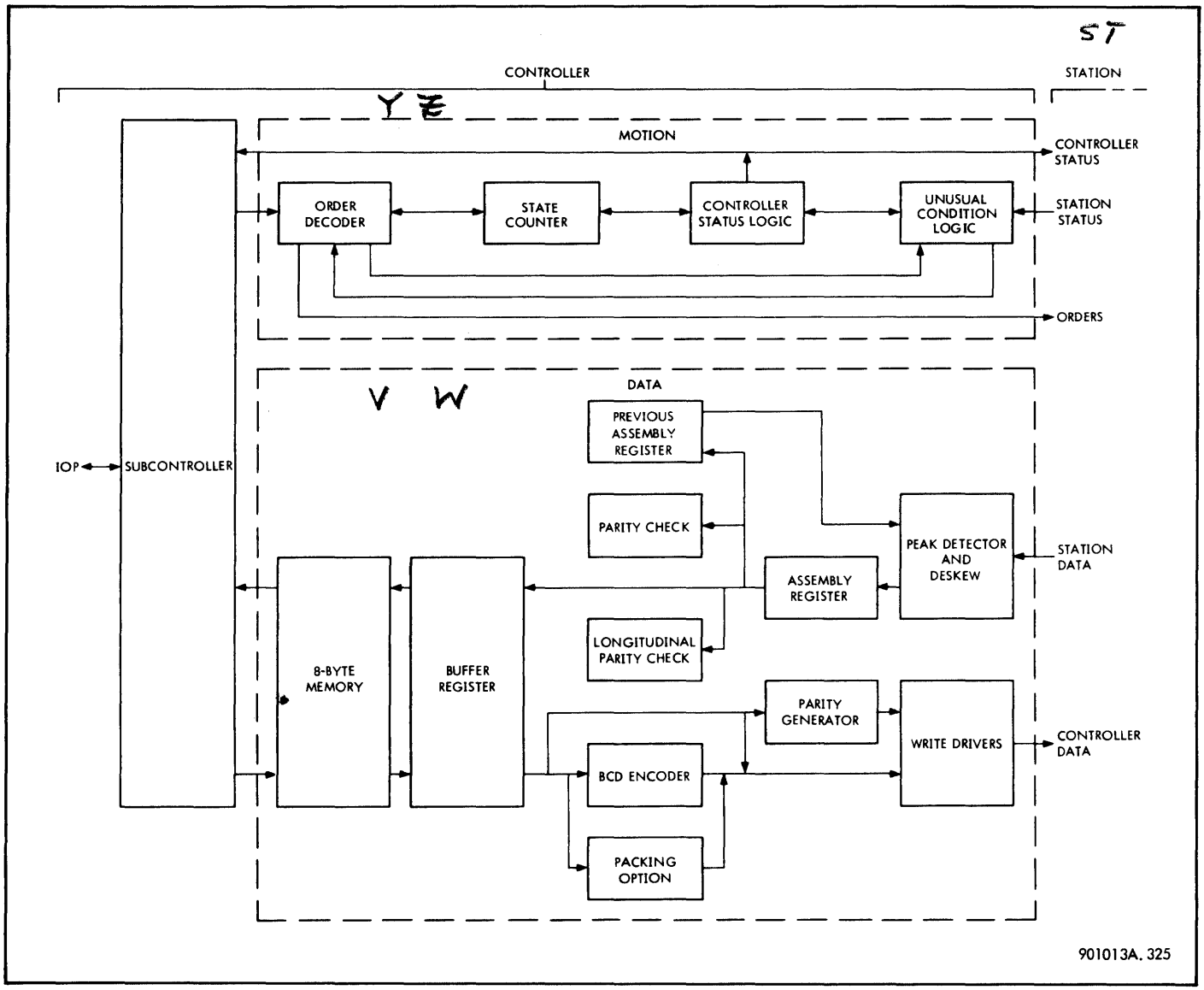


Figure 3-27. Magnetic Tape Controller, Block Diagram

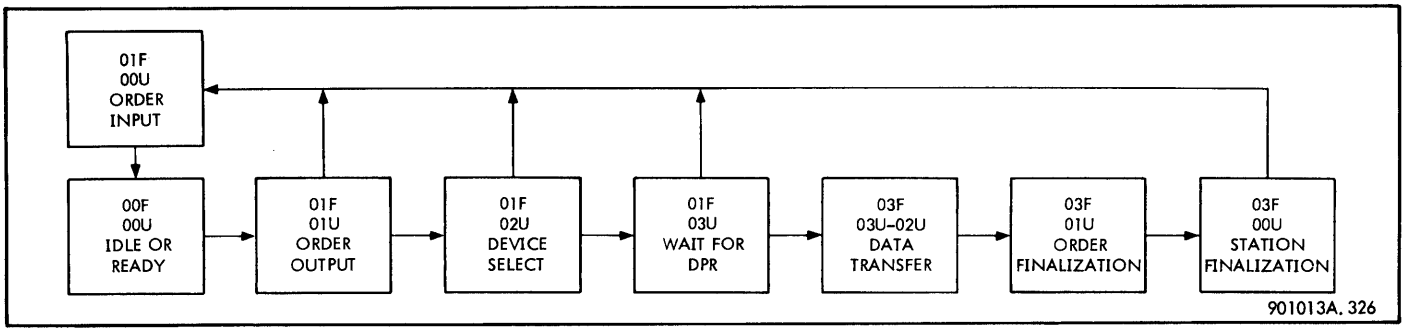


Figure 3-28. Magnetic Tape Controller States, Simplified Block Diagram

3-34 INTERFACE

The IOP-controller interface permits all device controllers to operate simultaneously by time-sharing interface signals with the IOP. The interface function for the magnetic tape controller is handled by a group of modules located in chassis Y. These modules constitute an assembly which is part of each Sigma peripheral controller and is called a device subcontroller (DS). Figure 3-29 shows a block diagram of the subcontroller with the main signals identified.

To carry out its interface function, the subcontroller contains the following logic circuits and components:

a. Cable drivers and receivers that link the eight-bit data path interface from the IOP

b. Logic circuitry to determine priority during ASC and AIO operations

c. Eight address determining switches and logic circuits, which determine and compare the controller number for IOP detection during SIO, HIO, TIO, and TDV operations

d. Service connect flip-flop (SCF) and associated logic circuitry, to indicate that the controller is connected for service

e. Relay logic, under remote control, for connection or removal of the subcontroller during system on/off operations

The subcontroller modules, their associated cables and connector locations, as well as module descriptions are given in table 3-4.

Table 3-4. Subcontroller Connector/Cable/Module Identification

Connector Location	Module Type	Cable Designation	Module Description
23	LT25		Special logic module. Contains service call latch circuits, data line (received) inverters, a toggle switch (to indicate on-line or off-line), and other subcontroller functions
24	LT26		Special logic module. Contains 8 toggle switches for device controller address selection and two 4-bit comparators to compare selected address with IOP output address during SIO, HIO, and TDV instructions
25	Reserved: AT17 takes two slots		
26	AT17	J4	Cable driver-receiver and power on-off relay to which the input and output priority determination cable connects (occupies two module positions)
27	LT24		Special logic module. Contains function response line buffers with 3-way OR gates and other subcontroller circuits
28	AT10	J3	Cable receiver to which one cable from the IOP connects
29	AT41		Special logic module. Contains some priority determination logic, service-connect flip-flop (FSC), TSH, and TTSH
30	AT11	J2	Cable driver-receiver to which one cable from the IOP connects
31	LT43		Special logic module. Contains some priority determination logic and various subcontroller circuits
32	AT12	J1	Cable driver to which one cable from the IOP connects

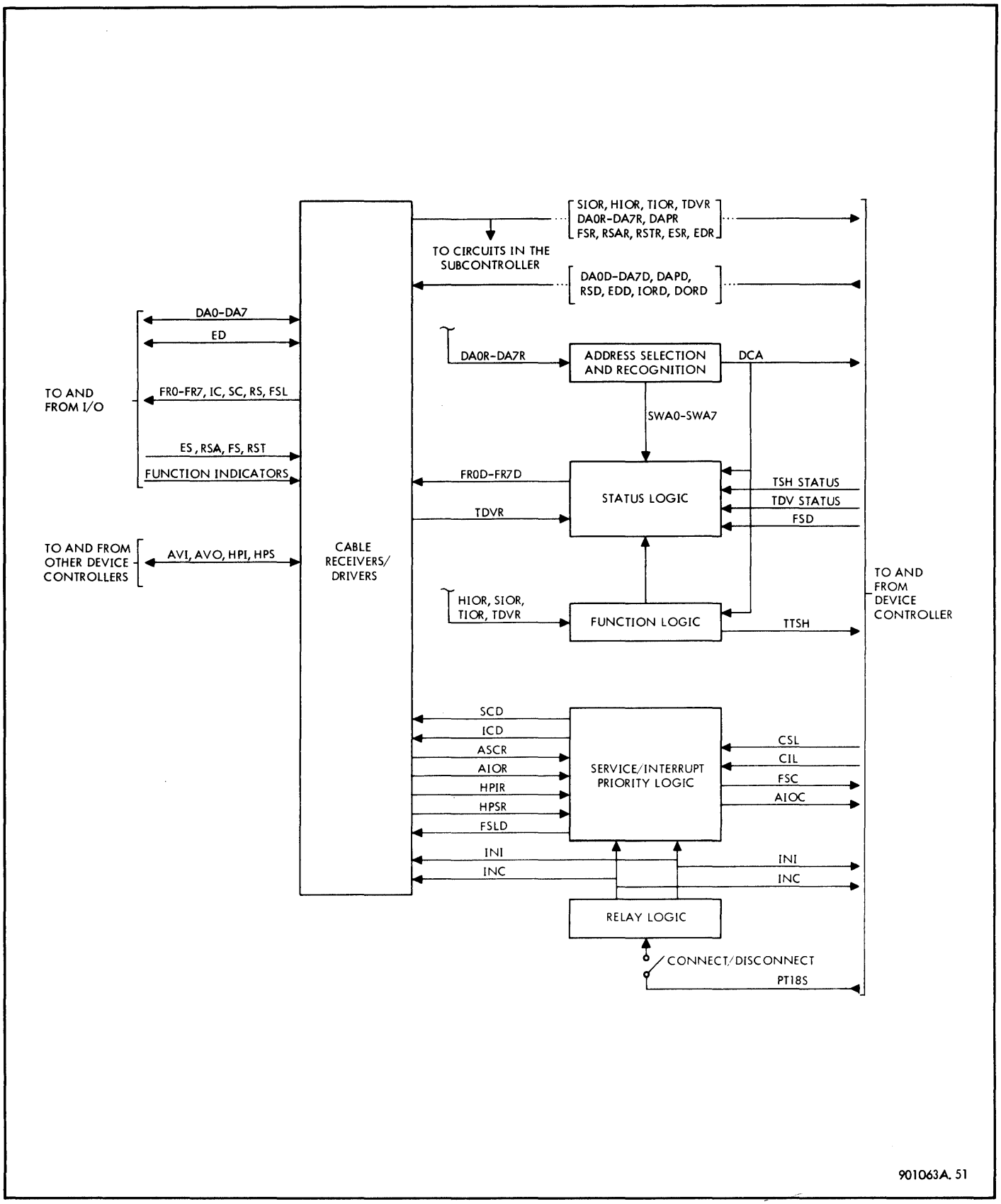


Figure 3-29. Subcontroller, Simplified Functional Block Diagram

3-35 Data Path

The IOP provides three connectors and cables for transmission of all signals to and from the controller. These cables are routed to each peripheral device, in a bus fashion, by means of the shortest path. An additional priority cable interconnects the controllers to the IOP in a trunktail fashion, with the first controller in the chain having priority during service and interrupt calls. Figure 3-30 shows a typical data path interconnection diagram.

The cables consist of 14 shielded wires with a characteristic impedance of 33 ohms. There are cable driver and cable receiver circuits connected to each cable. The cable drivers consist of emitter followers presenting 16.5 ohms output impedance for a logic one and high impedance for a logic zero. The cable receivers are amplifiers with an input discrimination level of approximately +1 volt. The signal levels are +2 volts for a logic one and zero volts for a logic zero.

3-36 IOP-Controller Signals

The signal exchange between the IOP and the controller is carried via cable receiver module AT10 (Y28), cable driver and receiver module AT11 (Y30), and cable driver module AT12 (Y32). The interface signal lines interconnecting the IOP and controller are shown and identified in figure 3-31. The status for the response and data lines is given in table 3-5, where the corresponding system functions are described and identified.

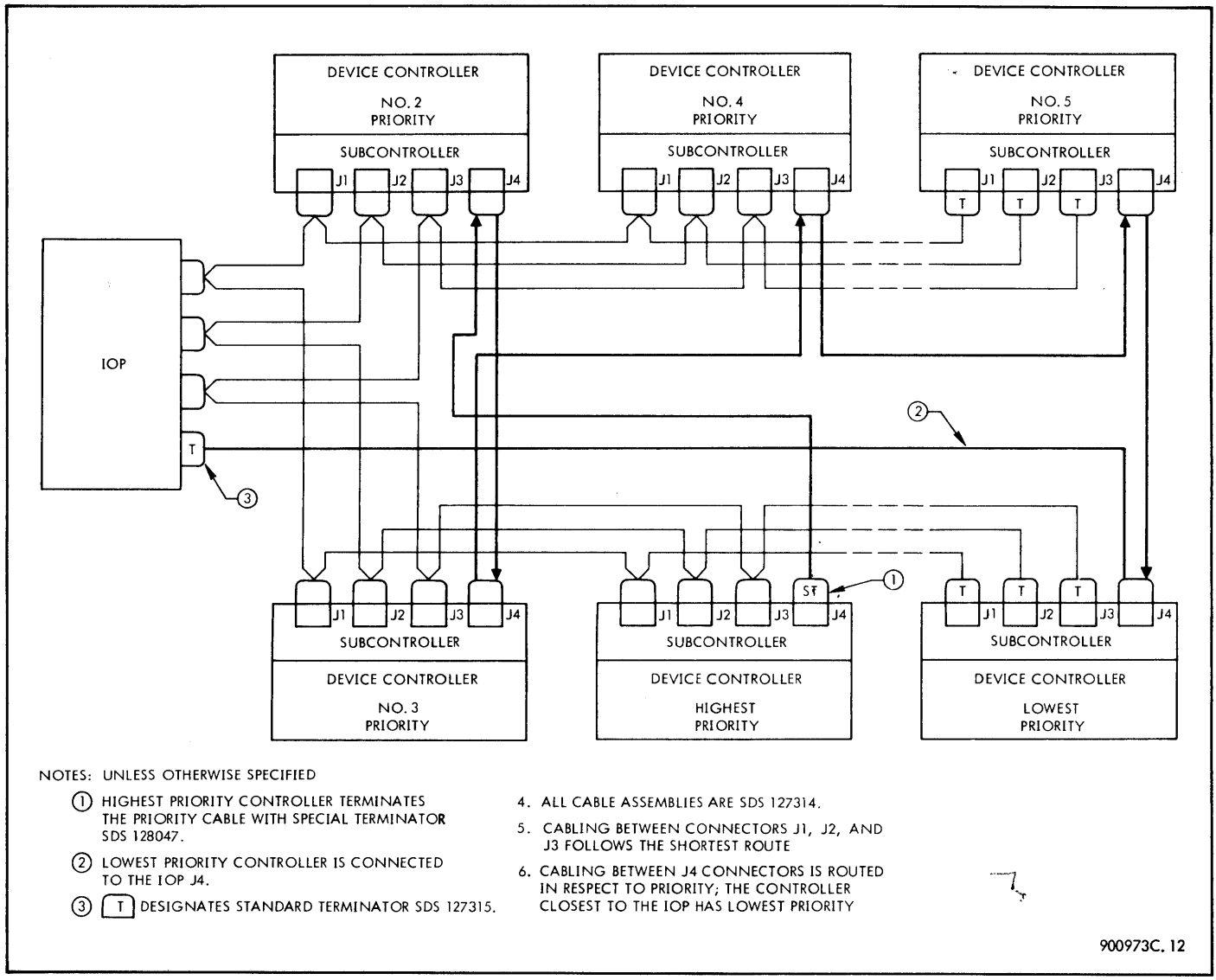


Figure 3-30. Typical I/O Interconnections

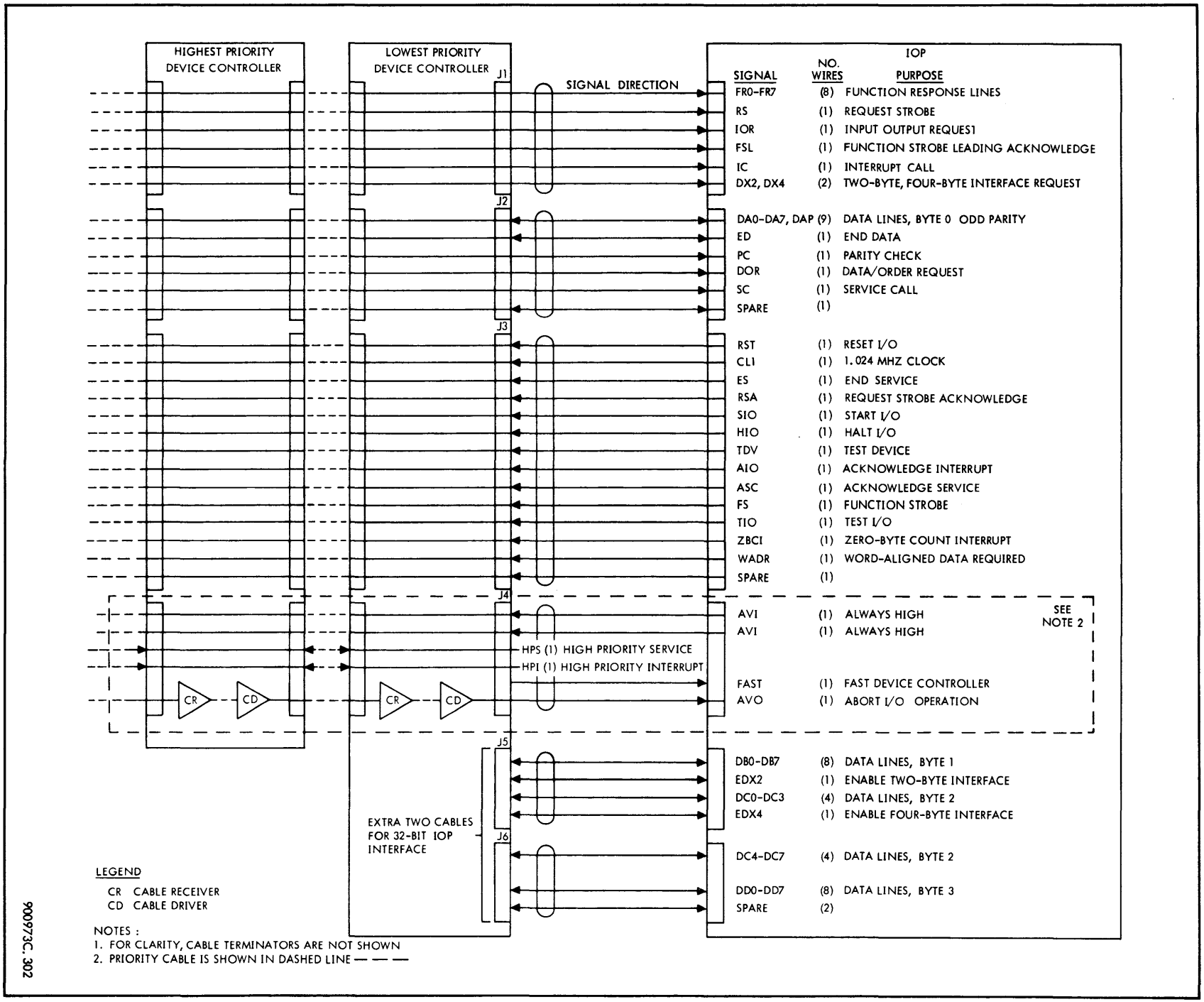
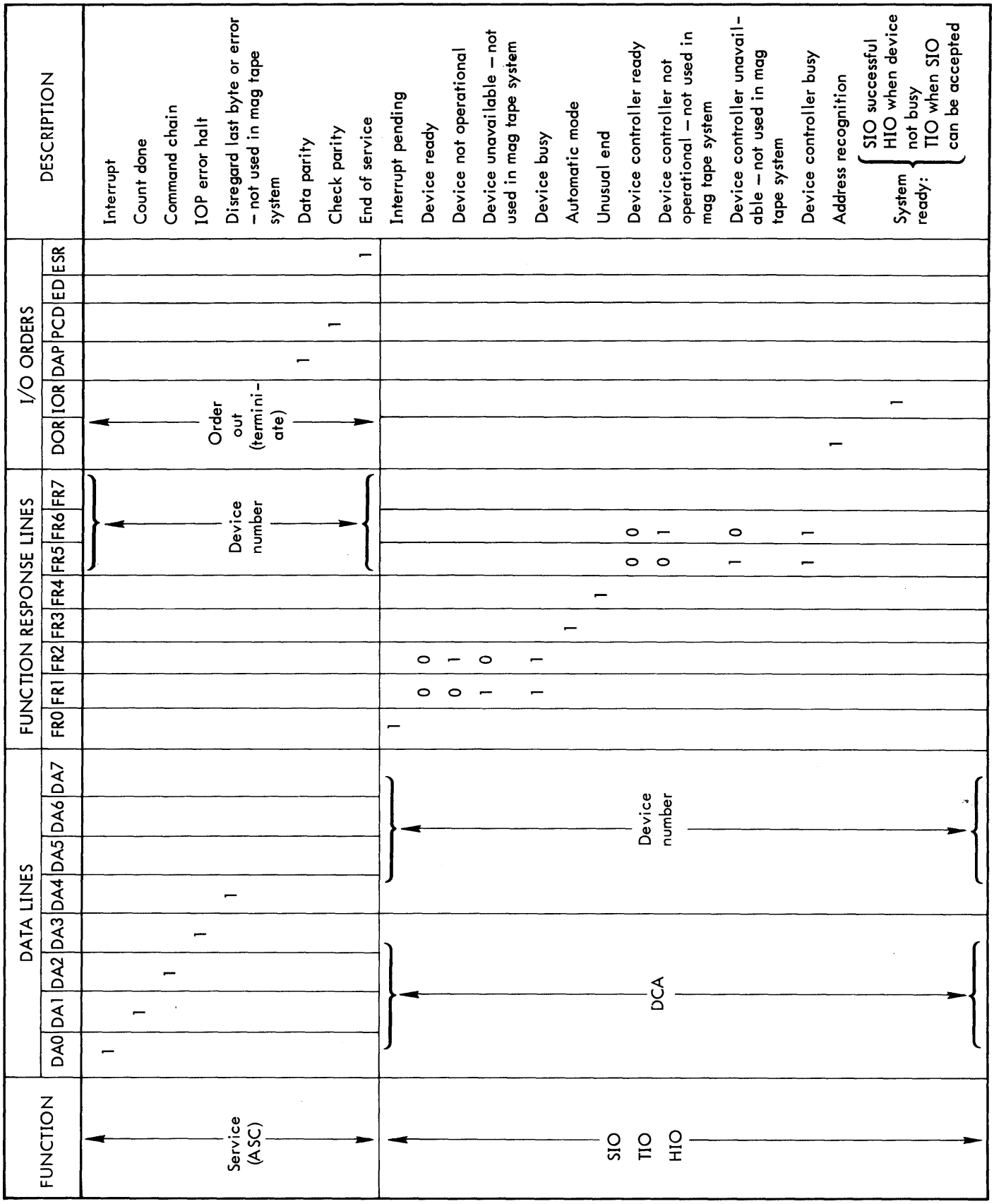


Figure 3-31. IOP-Interface Signal Lines Diagram

Table 3-5. Subcontroller Interface (Continued)

FUNCTION	DATA LINES								FUNCTION RESPONSE LINES								I/O ORDERS						DESCRIPTION
	DA0	DA1	DA2	DA3	DA4	DA5	DA6	DA7	FR0	FR1	FR2	FR3	FR4	FR5	FR6	FR7	DOR	IOR	DAP	PCD	ED	ESR	
Service (ASC)													Device number				1						Order (0 ⟹ data)
																		1					Output (0 ⟹ input)
																					1		End data
					0	0	0	1									Order out						Write packed
					0	1	0	1															Write binary
					1	1	0	1															Write BCD
					0	0	1	0															Read packed
					0	1	1	0															Read binary
					1	1	1	0															Read BCD
		0	0	1	0		1	1															Rewind and interrupt (on-line)
		0	1	0	0		1	1															Rewind off-line (manual mode)
		0	1	1	0		1	1															Rewind (rewinds to load point on automatic)
		1	0	0	D		1	1															Space record (D = 0 ⟹ forward; D = 1 ⟹ backward)
		1	0	1	D		1	1															Space file (D = 0 ⟹ forward; D = 1 ⟹ backward)
		1	1	0			1	1															Set erase (to be used with next write)
		1	1	1	0		1	1															Write tape mark
	1																Order in						Transmission error
		1																					Incorrect length
			1																				Chaining modifier - not used in mag tape system
				1																			Channel end
					1																		Unusual end

Table 3-5. Subcontroller Interface (Cont.)



(Continued)

Table 3-5. Subcontroller Interface (Cont.)

FUNCTION	DATA LINES								FUNCTION RESPONSE LINES								I/O ORDERS						DESCRIPTION
	DA0	DA1	DA2	DA3	DA4	DA5	DA6	DA7	FR0	FR1	FR2	FR3	FR4	FR5	FR6	FR7	DOR	IOR	DAP	PCD	ED	ESR	
TDV		DCA				Device number			1														Rate error
																	1						Address recognition
										1								1					Abnormal condition does not exist (device operational)
											1												Write permitted /
												1											Write protect violation
														1									End of file
															1								Load point
																1							End of tape
																							Rewind on-line
AIO																							Device end
		1															1						AIO recognition
			1															1					No unusual end condition detected
				1																			Write protect violation
	1																						End of file
																							Rate error

3-37 Controller-Station Signals

The controller has two sets of connectors for attachment to the stations. One of these connects the controller to the station electronics located in the controller cabinet. The other set of connectors is used to connect the adjacent stations, each of the stations being the beginning of a trunk-tail connection that extends to the last station of the system.

The signals between the controller and the station are carried by cables connected to modules contained in chassis Z. These modules are cable driver and receiver module AT11 (32Z), cable driver module AT12 (26Z), and cable receiver module AT10 (28Z).

Control and status lines are connected between the station and the transport. The status lines indicate the current condition of the transport. The control lines determine the transport mode of operation (see table 3-6).

Table 3-7 shows the interface signals between the controller and the station, and between the station and the transport. Refer to the glossary, at the end of the section, for a description of terms.

Table 3-6. Transport Modes

CONTROL TERM	MODE OF OPERATION			
	Forward	Reverse	Rewind	Rewind Off-Line
REVS	0	1	1	0
ACMS	1	1	1	0
REWS	0	0	1	0
ROFS	0	0	0	1

Table 3-7. Magnetic Tape System Interface Signals

Transport	Station	Station	Controller
Device ready indicator	← DRDS	RVRS	← REV
Device busy indicator	← DBSS	WN1	← WN1
Attention indicator	← ATNS	WN2	← WN2
Reverse/forward	← REVS	WRT	← WRT
Actuate Motor	← ACMS	RASS	← FRS
Rewind/off-line	← ROFS	DSS	← DSS
Fast/normal	← REWS	DST	← DST
Unit select switch 0C →	UNIT SELECT SW 0C	DSL	← DSL
1C →	1C	END	← END
2C →	2C	DV0D →	DV0R
3C →	3C	⋮	⋮
4C →	4C	DV7D →	DV7R
5C →	5C	INPS →	INPS
6C →	6C	DRDS →	DRDS
Unit select switch 7C →	UNIT SELECT SW 7C	DBSS →	DBSS
ATTENTION CONTR →	ATTENTION CONTR	AUTS →	AUTS
START CONTR →	START CONTR	ARGS →	ARGS
OPERATIONAL CONTR →	OPERATIONAL CONTR	WPMS →	WPMS

(Continued)

Table 3-7. Magnetic Tape System Interface Signals (Cont.)

Transport	Station	Station	Controller
		BTSS →	BTSS
FILE PROTECT →	FILE PROTECT	ENTS →	ENTS
EOT CONTR →	EOT CONTR	WNDS →	WNDS
LOAD POINT CONTR →	LOAD POINT CONTR	LSPS →	LSPS
LSPS →	LSPS	HSPS →	HSPS
HSPS →	HSPS	BOTS →	BOTS
25VWP1 →	25VWP1	INTS →	INTS
25VWP2 →	25VWP2	DSGS →	DSGS
POWER FAILURE IN* →	POWER FAILURE IN*	DPRS →	DPRS
POWER FAILURE OUT* →	POWER FAILURE OUT*	DV0R	← DV0D
		⋮	⋮
		DV7R	← DV7D
		GNT	← GNT
		RST	← RST
		ATO, HLTD	← ATO, HLTD
		AIOCD	← AIOCD
		NTSH	← NTSH
		CLK	← CLK

*Utilized only if the station and the controller occupy a common cabinet

3-38 Interface Disconnect

The device subcontroller contains circuits for connecting and disconnecting the device controller from the IOP interface in a transient-free manner when power is applied or removed from the device controller. Although the subcontroller provides the proper connect and disconnect sequencing, the controller actually provides the signal to initiate the operation. Figure 3-32 shows a timing diagram for the connect/disconnect operation.

DISCONNECT OPERATION. The DS is disconnected from the IOP interface whenever the ON-OFF switch located on the LT25 module is positioned to OFF, or the controller removes the ground source from the connect/disconnect circuits. The ON-OFF switch on the DS is connected in series with the ground source to the connect/disconnect circuits. When the ground source to these circuits is removed, the following sequence occurs:

a. Approximately 1.6 milliseconds after the ground source is removed, all service and interrupt calls to the IOP are inhibited. (Refer to figure 3-30.) This is accomplished by grounding the INC term and letting NINC go true through relay and transistor logic.

b. Approximately 4.2 milliseconds after INC is grounded, the term INI is grounded through a set of relay contacts. AVI also becomes shorted to AVO through a second set of relay contacts at this time. The timing of the two sets of contacts can vary by as much as 250 microseconds.

c. Approximately 0.5 milliseconds after INI is grounded, NINI is allowed to go true. When INI is grounded, the subcontroller is considered disconnected from the IOP interface, since INI grounds all input to the subcontroller cable drivers. AVI is short circuited to AVO, so that the DS is still physically connected to the priority cable of the IOP interface without interfering in the operation of the priority cable.

CONNECT OPERATION. When the device subcontroller is to be connected to the IOP interface, the ON/OFF switch on the DS must be positioned to ON and a ground source must be applied to the connect/disconnect circuits. The ground source to the circuits should be applied after all voltages have reached the specified operating level. When the ground source is applied to the connect/disconnect circuits, the following sequence occurs:

a. Approximately 4.5 milliseconds after the ground source is applied, a set of relay contacts is closed and term NINI is grounded. (Refer to figure 3-30.)

b. Approximately 0.5 milliseconds later, term INI is allowed to go true. The short circuit between AVI and AVO is removed at this time.

c. Approximately 120 microseconds after INI goes true, term INC goes true and term NINC is grounded. When INI and INC have reached the true state, the controller is connected to the IOP interface, and the service call, interrupt call, and cable driver lines become active.

3-39 COMMUNICATION CYCLES

The IOP-controller interface involves signals going from the IOP to the controller and from the controller to the IOP. The controller-to-IOP direction defines a communication cycle. The IOP-to-controller direction defines a service cycle.

During a communication cycle, the IOP raises different function lines as a result of the instructions executed by the CPU. These are the functions:

a. The start or halt of each station under program control (SIO and HIO)

b. Status testing of the controller, the station, or both (TIO and TDV)

c. Service or interrupt acknowledgement (AIO)

d. The transfer of orders or data from the IOP (ASC)

The sequence of controller operations for SIO, HIO, TIO, and TDV functions is similar, as far as the IOP-controller interface is concerned. Therefore, a description of the SIO function is given as an illustration (see figure 3-33). The controller internal operations during these communication cycles are described in the Controller States portion of this section, paragraphs 3-48 through 3-56.

3-40 Start Input/Output (SIO)

To initiate data transfer with the magnetic tape system, the CPU executes an SIO instruction. The IOP then receives a command word that contains a controller address, a device address, and a memory location that defines the starting point for the list of commands to be carried out. The IOP then raises the SIO function line that goes to the controllers. After priority determination and selection, the magnetic tape controller responds according to the current conditions in the magnetic tape system (see paragraph 2-19). This response is associated to the previous operation performed by the controller, and it is undefined if the SIO is the first instruction after initial turn-on. Figure 3-34 shows a flow diagram of the SIO, HIO, TIO, and TDV operations.

The controller receives the function strobe and function indicator (SIO), along with the device address. There are two strobe signals generated by the IOP: request strobe and function strobe. The strobe signals are acknowledged in a closed-loop manner. That is, the strobe signal is applied until an acknowledge signal is received. Then the acknowledge signal remains applied until the strobe signal is removed, at which time the acknowledge signal is removed.

The controller acknowledges the FS signal with a maximum delay of 100 ns. If it is in the 00F00U state (idle or ready) the controller raises FSL and supplies status information on the function response lines (see table 3-5).

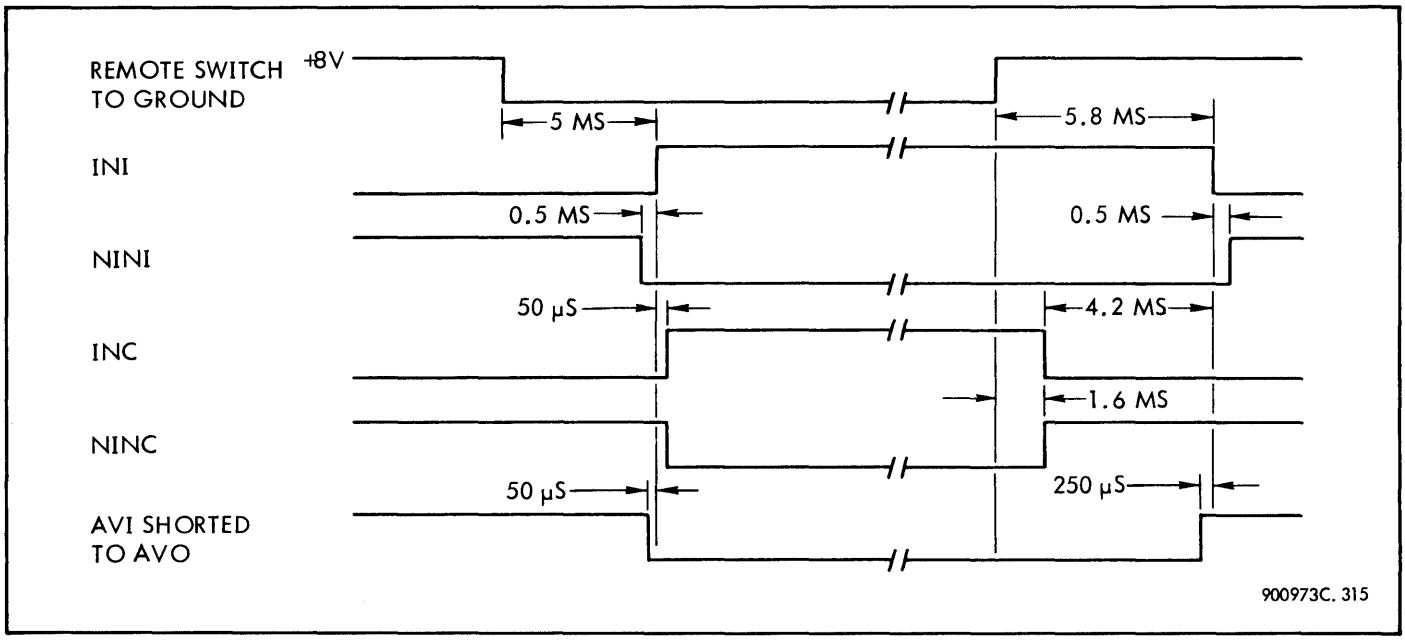


Figure 3-32. Connect/Disconnect Timing

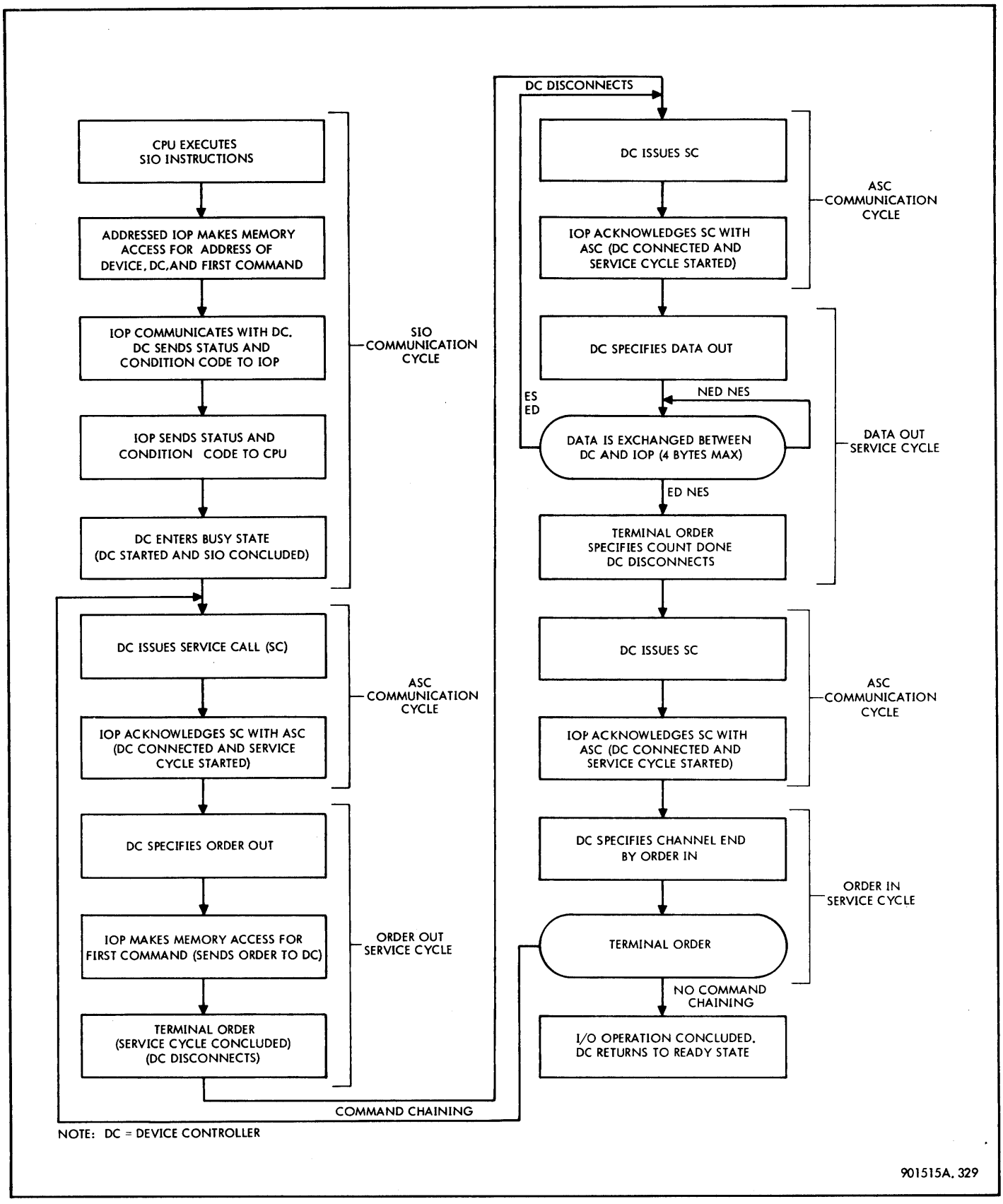
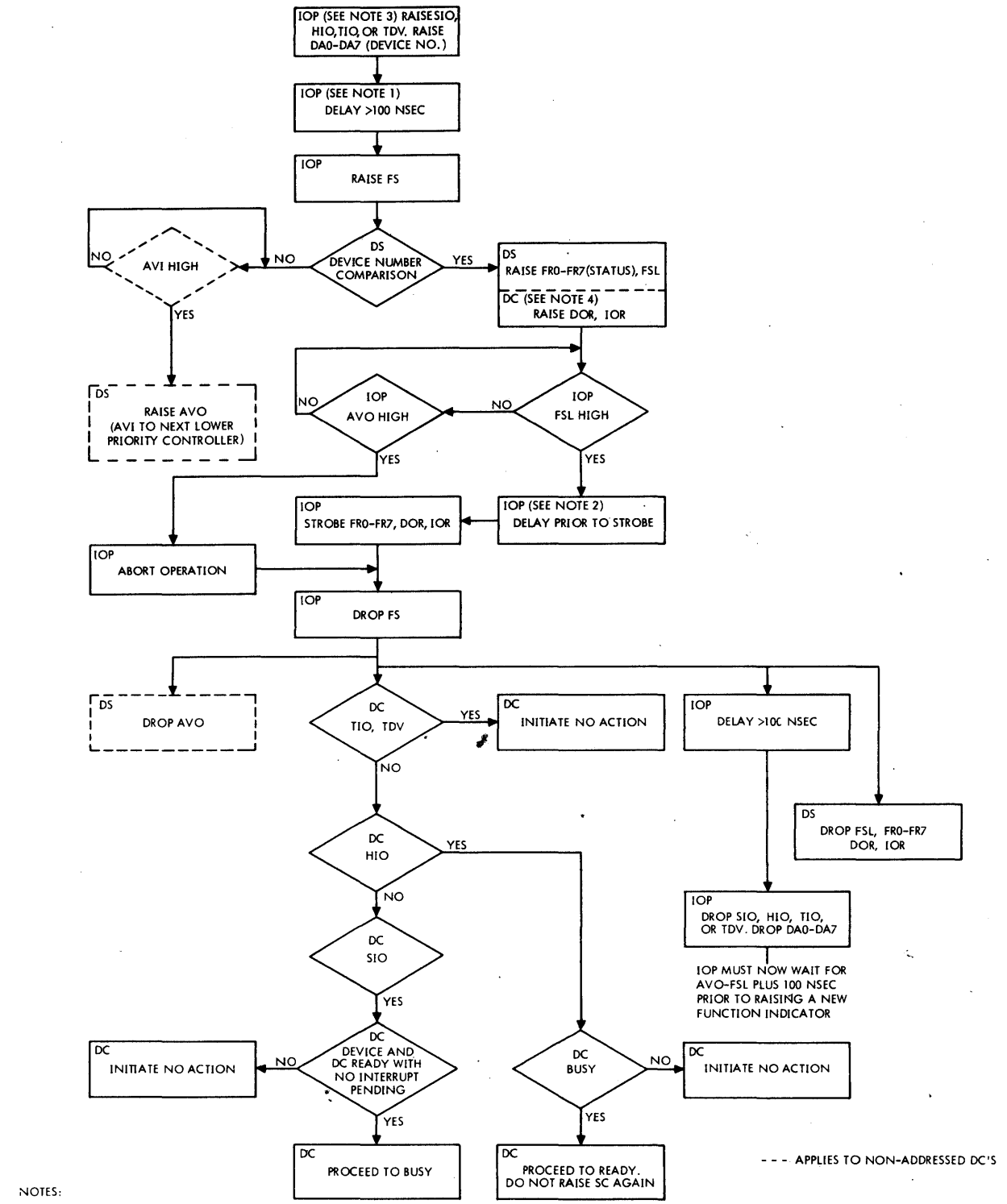


Figure 3-33. Communication and Service Cycle Sequence



NOTES:

1. FOR SIGNALS ARRIVING FROM IOP, ALL TIMING IS MEASURED AT OUTPUT OF DEVICE CONTROLLER CABLE RECEIVER.
2. BEFORE STROBING INPUT SIGNAL LINES AFTER RECEIVING FSL OR RS SIGNAL, IOP MUST COMPENSATE FOR WORST-CASE SIGNAL DISPERSION CAUSED BY CABLES, IOP RECEIVERS, IOP LOGIC, PLUS 60 NSEC.
3. ONLY ONE FUNCTION INDICATOR (SIO, HIO, TIO, TDV, AIO, OR ASC) CAN BE HIGH AT ANY TIME.
4. DOR AND IOR REPRESENT CONDITION CODES NCC1 AND NCC2, RESPECTIVELY, AT THIS TIME. RAISE IOR (NCC2) ONLY IF APPLICABLE.
5. AVI TO THE HIGHEST PRIORITY DEVICE CONTROLLER IS ALWAYS HIGH.

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Figure 3-34. SIO, HIO, TIO, and TDV, Flow Diagram

DEVICE PRIORITY. When a device controller has been activated by an SIO instruction, it may make service calls to the IOP until it halts itself or is halted by an HIO instruction. Since many controllers may be connected to one IOP, a priority chain is established to enable the IOP to determine which controller wants service.

A priority cable is connected between each controller in the chain and between the lowest priority controller and the IOP. Four signals are carried on the cable:

a. HPI – High priority interrupt

b. HPS – High priority service

c. AVO – Available output

d. AVI – Available input

The first two signals (HPI and HPS) constitute a signal bus that is tapped and driven by each controller. Signal AVO is an output from each controller that is sent to the next lower priority controller in the chain; it is a logical function of AVI (the input priority signal). Signal AVI is always true for the first (highest priority) controller in the chain. Signal AVI for each subsequent controller in the chain is equal to AVO from the preceding controller.

When more than one controller has made a service request at the same time, only one may be connected for service. When the IOP acknowledges the service call, the requesting controller with the highest priority responds to the IOP acknowledgement.

If a controller has no service request pending, it passes on signal AVO when it detects signal AVI. If a controller has a service request pending, the controller passes on signal AVO only if signal HPS is true, or if the controller service request is of a low priority (that is, the controller has not generated the HPS itself).

If a controller has a service request pending, the controller does not pass on signal AVO when it detects signal AVI if it has generated the HPS itself, or if the HPS is not true.

If, during the execution of an SIO, TIO, TDV, or HIO, a controller does not sense its own address, it will pass on signal AVO when it detects signal AVI.

DEVICE SELECTION. When the IOP raises the SIO, HIO, TIO, or TDV function indicators, the device number is supplied as a byte on the DAxR lines. The address number in the case of multiple devices is in the following form:

DAxR lines	Data line	0	1 2 3	4 5 6 7
Contents	Data byte	1	Device controller number	Device number

DAxR lines 1, 2, and 3 specify the device controller number, and lines 4, 5, 6, and 7 specify the device number.

For controllers, with only one device, the following form is used:

DAxR lines	Data line	0	1 2 3 4 5 6 7
Contents	Data byte	0	Device number

The subcontroller compares the contents of the data lines (DA0R through DA7R) against the outputs of the eight address switches. Terms DCA and DCA47 come true during a successful comparison:

$$\begin{aligned} DCA = {} & N(NDA0R\ SWA0 + DA0R\ NSWA0 \\ & + NDA1R\ SWA1 + DA1R\ NSWA1 \\ & + NDA2R\ SWA2 + DA2R\ NSWA2 \\ & + NDA3R\ SWA3 + DA3R\ NSWA3)\ NFSC \end{aligned}$$

$$\begin{aligned} DCA47 = {} & N(NDA4R\ SWA4 + DA4R\ NSWA4 \\ & + NDA5R\ SWA5 + DA5R\ NSWA5 \\ & + NDA6R\ SWA6 + DA6R\ NSWA6 \\ & + NDA7R\ SWA7 + DA7R\ NSWA7) \end{aligned}$$

When the controller is used with a signal tape station, the outputs of signals DCA and DCA47 must be interconnected to achieve the full eight-bit device number comparison. DCA is held false when FSC is true.

After the IOP raises the function strobe, FS, the subcontroller supplies terms FSL or AVO, depending on the state of DCA:

$$FSLD = DCA\ FSD\ TTSH + BSYC$$

$$FSD = \text{Function strobe delayed}$$

$$BSYC = ASCM\ FSR\ AVIR\ ASCR + AIOM\ FSD\ AVIR\ AIOR$$

$$AVOD = TTSH\ NDCA\ FSR\ AVIR + \ldots$$

The subcontroller also supplies two control terms, TSH and TTSH:

$$TSH = DCA\ (SIOR + HIOR + TIOR)$$

$$TTSH = TIOR + TDVR + SIOR + HIOR$$

When status is applied to the function response lines (FR0 through FR7), the controller supplies term FSD. After FS goes low, FSD drops, and the controller status information is gated into the function response lines:

$$\begin{aligned} FR0D = {} & TSH\ FSD\ STSH00 + TDVR\ DCA\ FSD\ STDV00 \\ & + \ldots \\ & \vdots \\ FR7D = {} & TSH\ FSD\ STSH07 + TDVR\ DCA\ FSD\ STDV00 \\ & + \ldots \end{aligned}$$

Terms STSH00 through STSH07 represent status information supplied by the controller during SIO, HIO, or TIO operations. Terms STDV00 through STDV07 are supplied during TDV.

If the controller address does not agree with the address on the DAxR lines, signal DCA remains false, and AVO is sent to the next lower priority controller in the priority chain. If the controller address does agree with the address on the DAxR lines, the status report is put on the function response lines. When the status report is detected, the controller is connected to the IOP for service.

If, when addressed, the controller is not connected to the interface cables, or it has its power removed, the AVO signal is eventually received by the IOP. The IOP then aborts the operation. Figure 3-35 illustrates the signal sequencing for SIO, HIO, TIO, and TDV functions.

3-41 Acknowledge Input/Output (AIO)

The CPU sends an AIO instruction to acknowledge an I/O interrupt, and to identify the source and the cause of the interrupt. Figure 3-36 shows a flow diagram of an AIO interface operation.

The controller raises the term CIL when an interrupt call is required. CIL is kept raised during the AIO function by latching circuit LIL:

LIL = INC NAIOR CIL + LIL AIOR INI NRSTR

The controller provides the term CIH for high priority interrupt calls. CIH is latched by circuit LIH:

LIH = INC NAIOR CIL CIH + LIH AIOR INI NRSTR

LIL is followed by the high priority interrupt line ICD, while LIH is followed by HPID.

When the CPU acknowledges the interrupt call, the IOP raises the AIO function indicator. At this time, the terms LIL, LIH, and HPIL are latched. HPIL continuously monitors the state of the high priority interrupt line:

NHPIL = NAIOR HPIR + HPIL AIOR

When the IOP raises FS, the highest priority controller examines LIL, LIH, and HPIL to determine whether the AIO instruction may be accepted. If the AIO cannot be accepted, AVO is sent to the next lower priority controller:

AVOD = NAIOM AIOR FSR AVIR + ...

NAIOM = LIH + LIL NHPIL

AVIR is true at all times if the controller has the highest priority. If it does not, AVIR comes true only after all higher priority controllers have applied AVO.

The action of sequentially sending AVO from higher priority controllers to lower priority controllers continues until AIOM is found true. AVOD is then inhibited and FSL is raised:

FSLD = BSYC + ...

BSYC = AVIR AIOR FSD AIOM + ...

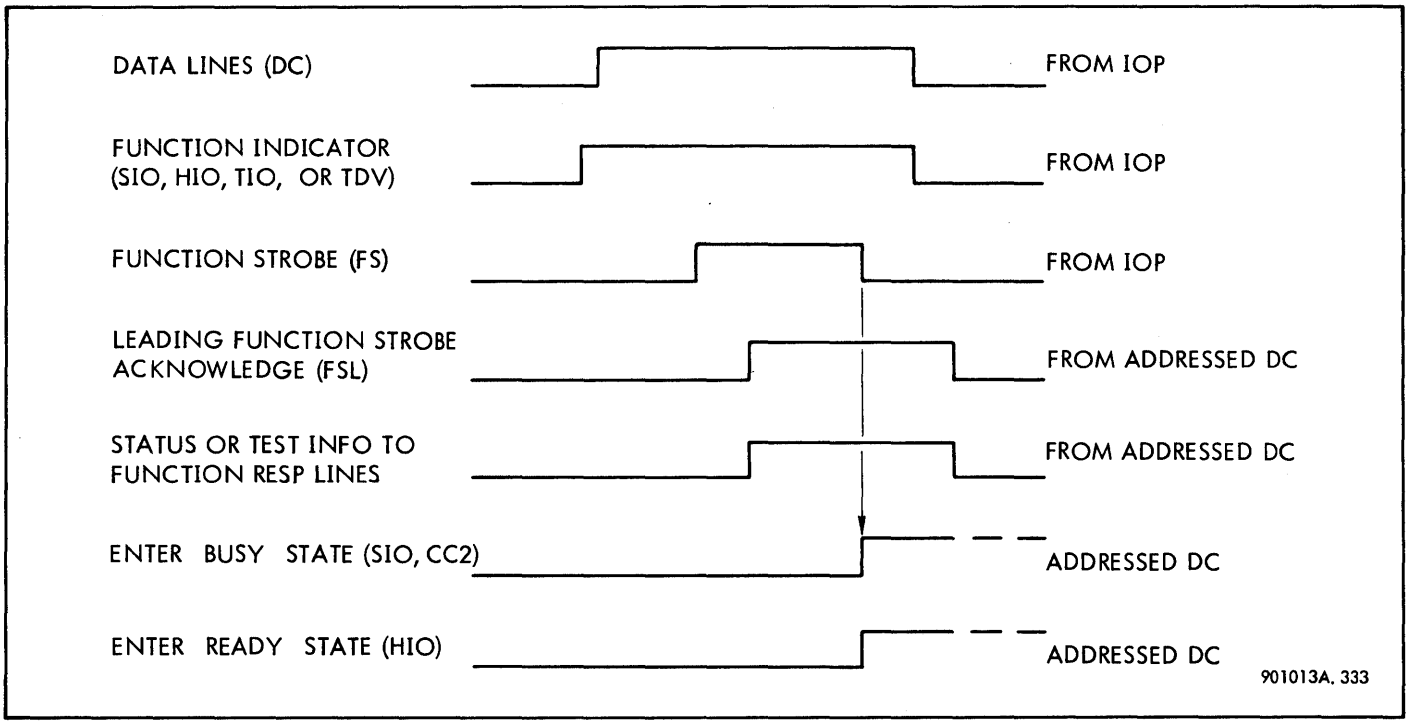


Figure 3-35. SIO, HIO, TIO, and TDV Interface Signal Sequencing

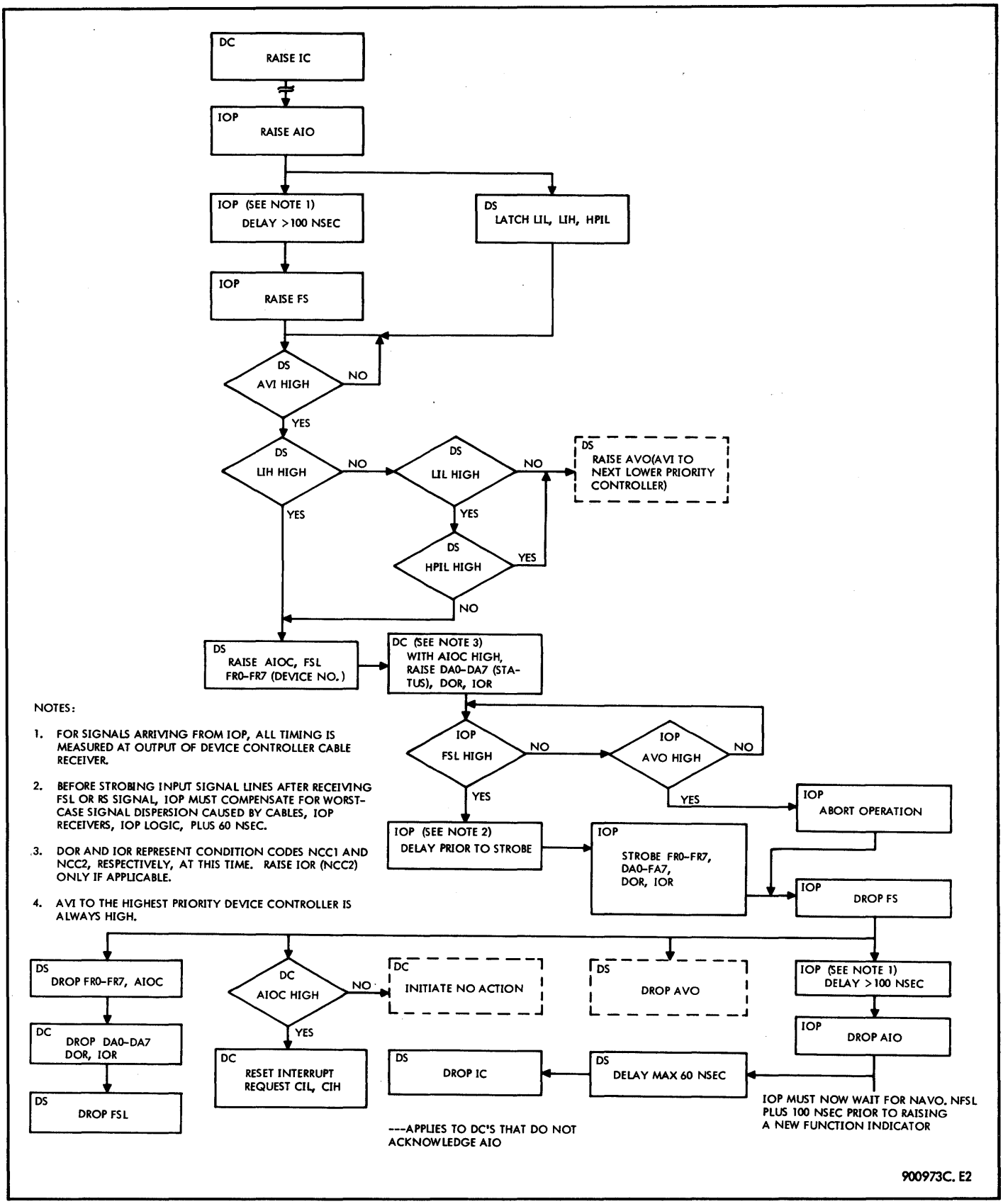


Figure 3-36. AIO Operation, Flow Diagram

At this time, the subcontroller presents the controller and station address numbers on the response lines (FR0D through FR7D). Term AIOC is also supplied, which indicates that the interrupt call is being acknowledged:

AIOC = AVIR AIOR AIOM + AIOC FSD INI NRSTR

The controller continues to hold CIL and CIH high until AIOC is raised. It then uses AIOC and FSR to reset CIL, CIH, and any interrupt indicators that may be set. While AIOC is high, the controller provides status and condition codes on the DOR and IOR lines.

When FSL is high, the IOP drops FS and 100 ns later drops AIO. This completes the AIO function. Figure 3-37 shows the interface signal sequence for AIO.

3-42 Acknowledge Service Call (ASC)

During the ASC function, the controller with the highest priority sets its service connect and resets its service call logic. After the ASC operation is completed, the controller whose service connect flip-flop is set gets connected to the IOP until the connection is terminated by service acknowledgement. Figure 3-38 illustrates the flow of an ASC interface operation.

The controller raises the term CSL when a service call is required. The subcontroller latches CSL by latching circuit LSL:

LSL = CSL INC NFSC NASCR
+ LSL NFSC NRSTR ASCR INI

ASCR = ASC

For high priority service calls, the controller provides the term CSH, which is then latched by LSH:

LSH = CSH CSL NFSC INC NASCR
+ LSH NFSC NRSTR ASCR INI

The service call line follows LSL, and the high priority line follows LSH:

SCD = LSL

HPSD = LSH

The IOP, detecting SC raised, acknowledges this by raising ASC. At this time, the subcontroller latches the condition of LSL, LSH, and HPSL:

NHPSL = HPSR NASCR + HPSL ASCR

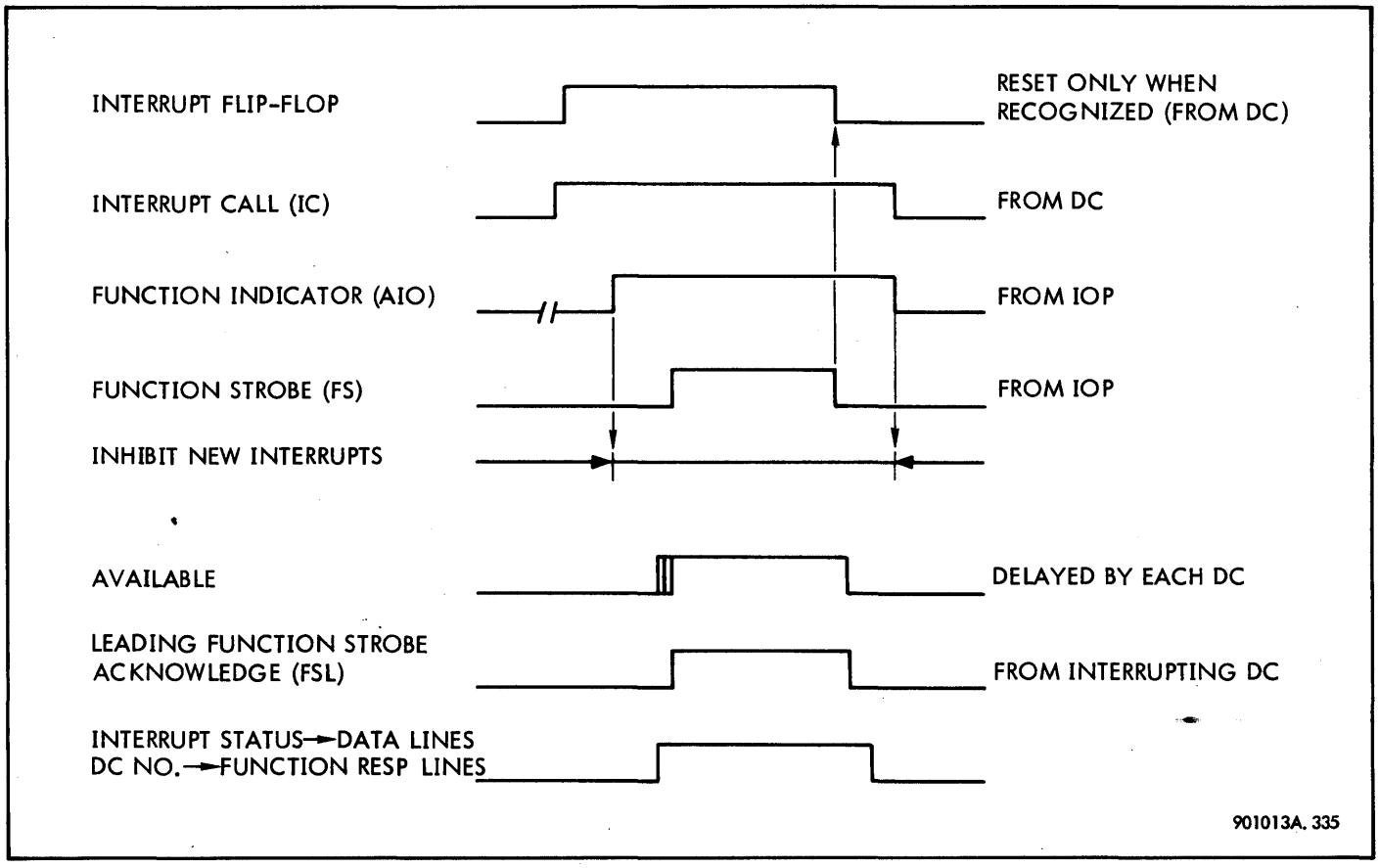


Figure 3-37. AIO Interface Signal Sequencing

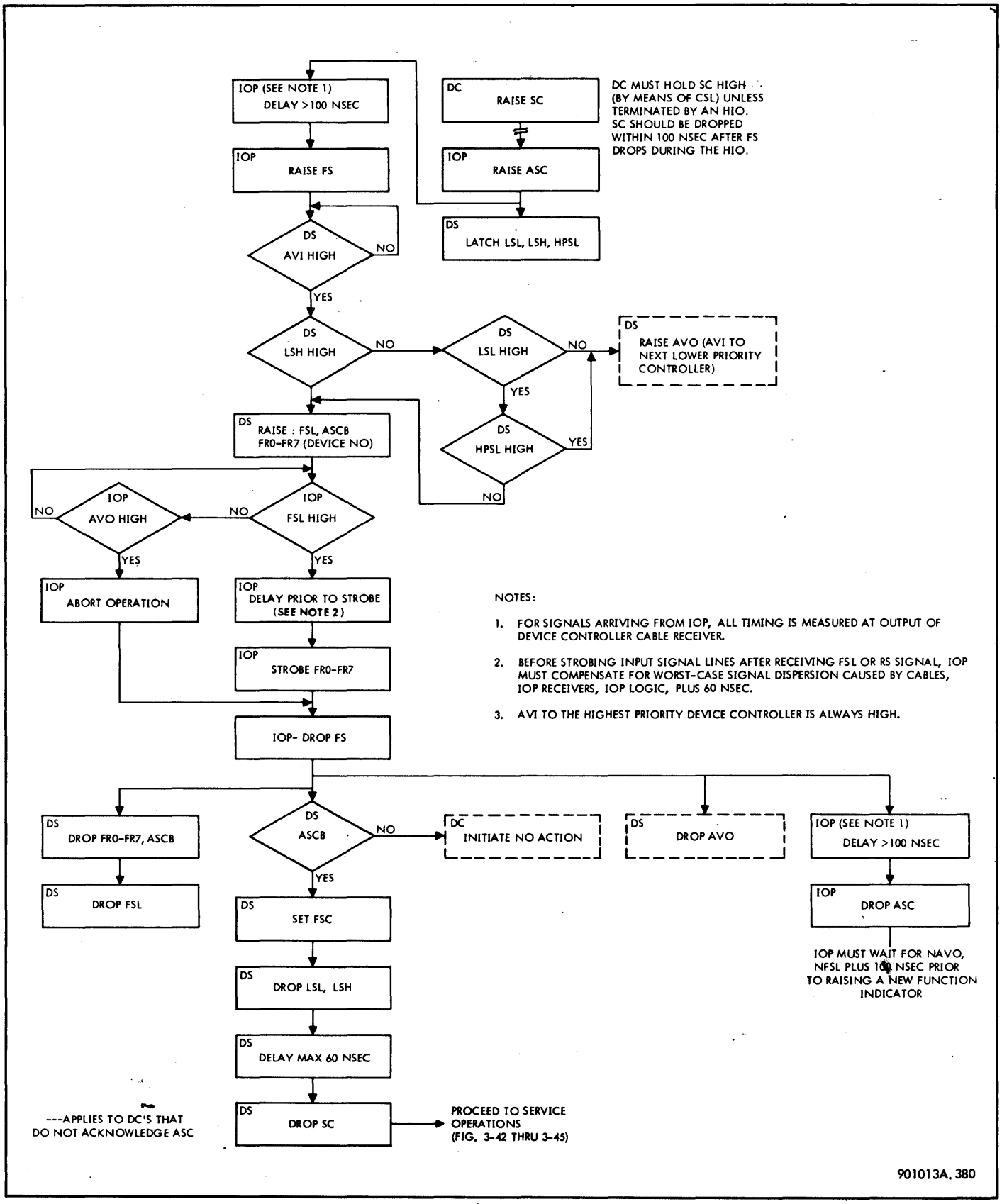


Figure 3-38. ASC Operation, Flow Diagram (Prior to Service Connection)

When the IOP raises FS, the controller examines LSL, LSH, and HPSL to determine whether any ASC may be accepted. If the ASC cannot be accepted, AVO is sent to the next lower priority controller:

AVOD = NASCM ASCR FSR AVIR

NASCM = LSM + LSL NHPSL

Priority determination and device selection then take place in the same manner as for the AIO function.

After FSL is raised, the IOP drops FS. The subcontroller, having ASCM high, sets FSC with the trailing edge of FS:

S/FSC = ASCB

C/FSC = FSR NFSC + ...

ASCB = AVIR ASCR FSR ASCM
+ ASCB NFSC INI NRSTR

When FSC is high, the controller proceeds with the service operation by raising RS and its associated signal lines:

RSD = FSC NRSARC

RSARC = RSAR + FSCL

FSCL = FSC ESR RSAR + FSCL FSC

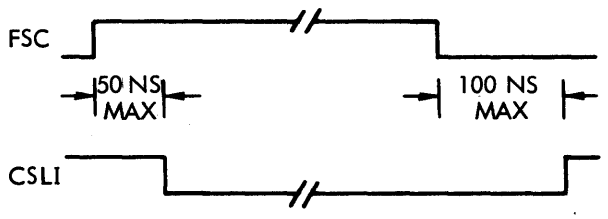
The term NRSARC prevents switching transients on the request strobe line, RS, if FSC is slow in resetting.

FSC remains set until ES is raised. This occurs at the trailing edge of RS:

R/FSC = ESR FSC

C/FSC = RSD FSC

The controller continues to hold CSL and CSH until FSC is set, unless halted by an HIO. Before FSC is set, the controller removes CSL and CSH. A typical equation for CSL or CSH is CSL = CSLI. CSLI is a delay circuit with the following characteristics:



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The purpose of CSLI is to prevent controller logic switching transients from appearing on the service call line.

After FSC is set, the ASC function is completed and communication between the controller and the IOP is established.

Figure 3-39 shows the interface signal sequence for the FSC function.

3-43 SERVICE CYCLES

When the magnetic tape controller has been connected to the IOP, and after FSC is set, a service cycle is initiated. There are four types of service cycles: order in, order out, data in, and data out. The signals present in lines DOR and IOR of the interface (CC1 and CC2 at the IOP) determine the type of service cycle for any instruction. Figure 3-40 shows a signal sequence after an SIO in which the service cycles are identified.

An order input cycle occurs when the controller reports either channel end or unusual conditions to the IOP. An order output cycle occurs when the controller requests an order from the IOP. The data in and data out service cycles refer to the transfer of data to and from the IOP. After a service cycle is completed, a terminal order is initiated by the controller. Figure 3-41 illustrates the timing sequence for a service cycle after FSC is set.

3-44 Order Input

The order in cycle takes place when the controller must report errors, unusual end, channel end, etc. to the IOP. This information is presented to the IOP on the data lines (DA0 through DA7).

The controller first generates a service call and waits for FSC to be set. At this time, the request strobe, order request, and data lines are driven. After detecting the service cycle information, the IOP responds by presenting the ASC signal. If the IOP does not generate ES during the order input cycle, the controller requests a terminal order by raising a request strobe. Figure 3-42 shows a flow diagram for the order input cycle.

3-45 Order Output

The order output cycle takes place when the controller requests a new order to the IOP. The controller sends a service call to the IOP and then waits for FSC to be set. At this time, the request strobe, order request, output request, and end data lines are driven. The IOP responds by raising RSA and presenting the requested order information on the data lines. If a terminal order is required by the IOP, the controller sends one more request strobe signal to the IOP. Figure 3-43 shows a flow diagram for an order output.

3-46 Data Input and Data Output

The data input/output cycle takes place when the controller is ready to send or receive data, and also when the controller is ready to accept control information for a space operation. After FSC is set, the request strobe, input/output, and data lines are driven. The IOP responds by accepting or presenting the data on the data lines. The controller continues sending request strobe signals until the IOP sends ES. If a terminal order is necessary at this time, the IOP sends not ES, but a count done indication. Figures 3-44 and 3-45 show flow diagrams for the data input and data output cycles, respectively.

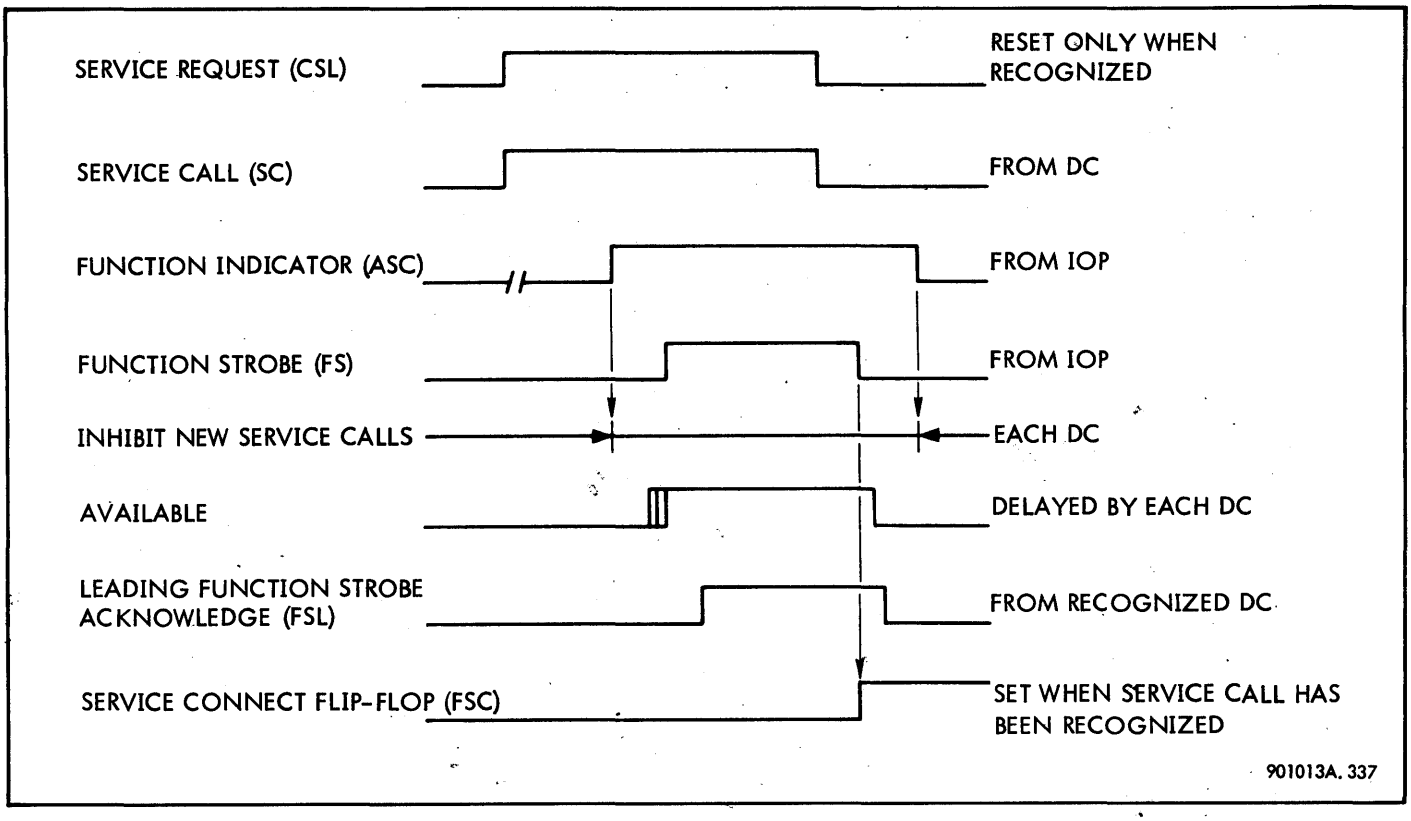


Figure 3-39. FSC Interface Signal Sequencing

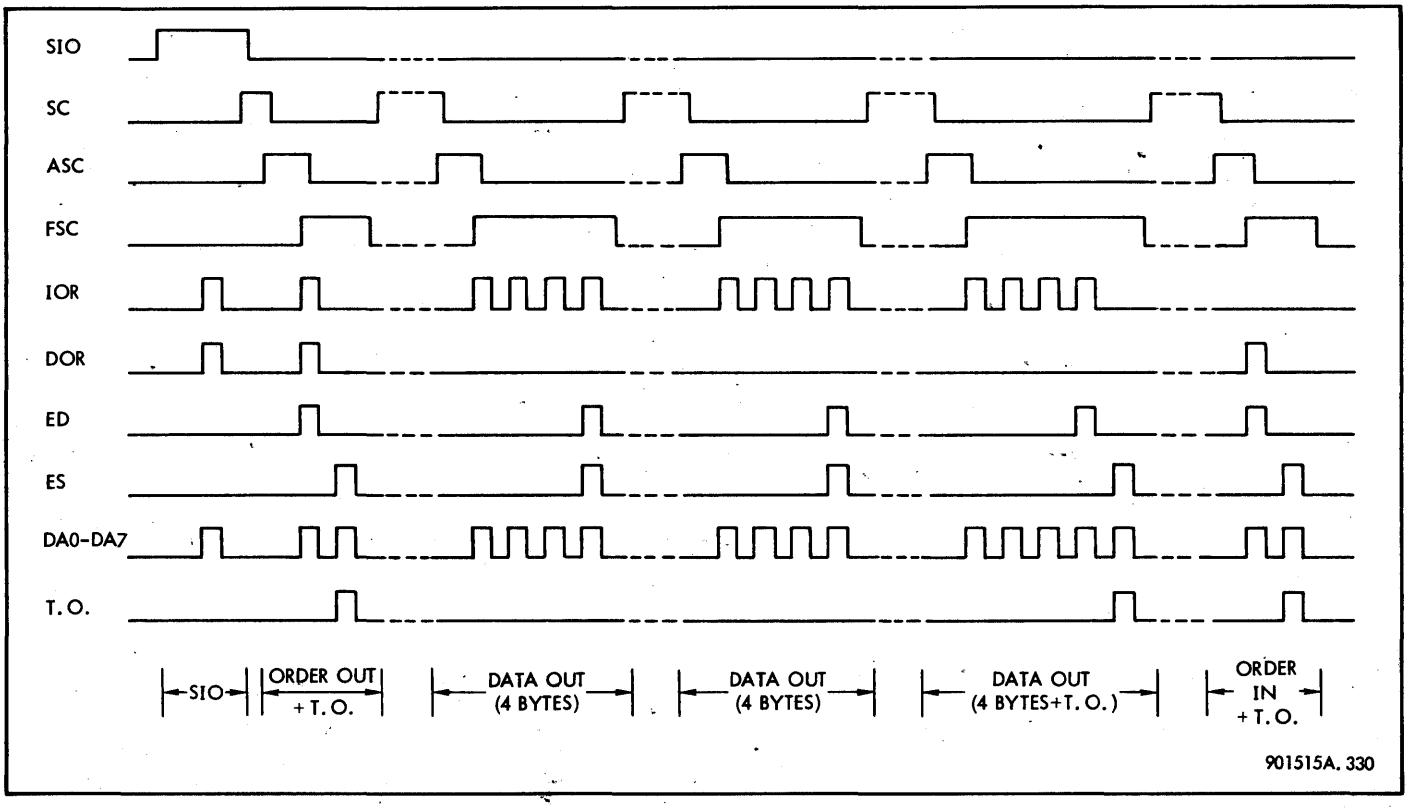


Figure 3-40. Service Cycles, Timing Diagram

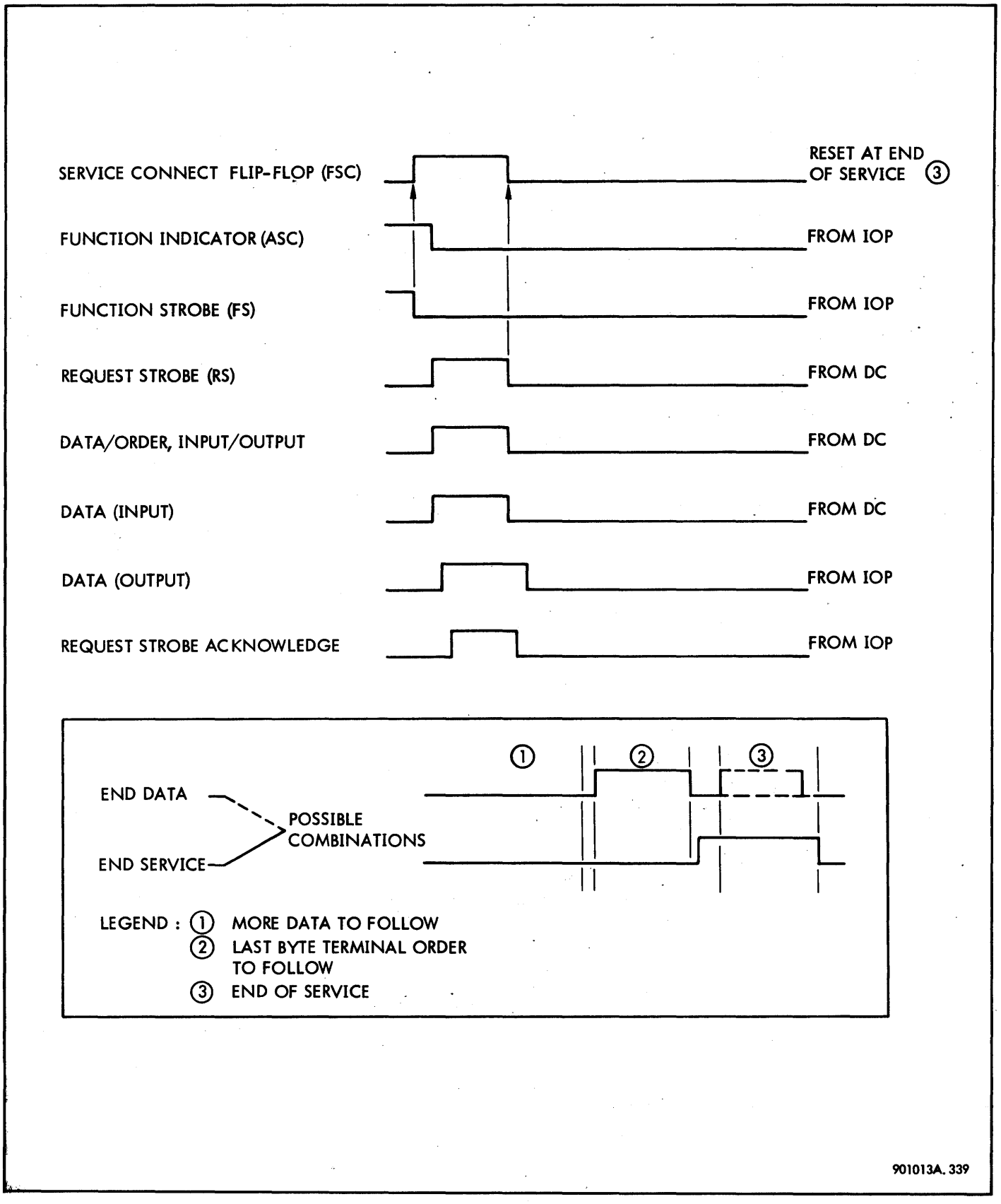


Figure 3-41. Service Cycle, Timing Sequence (One Byte)

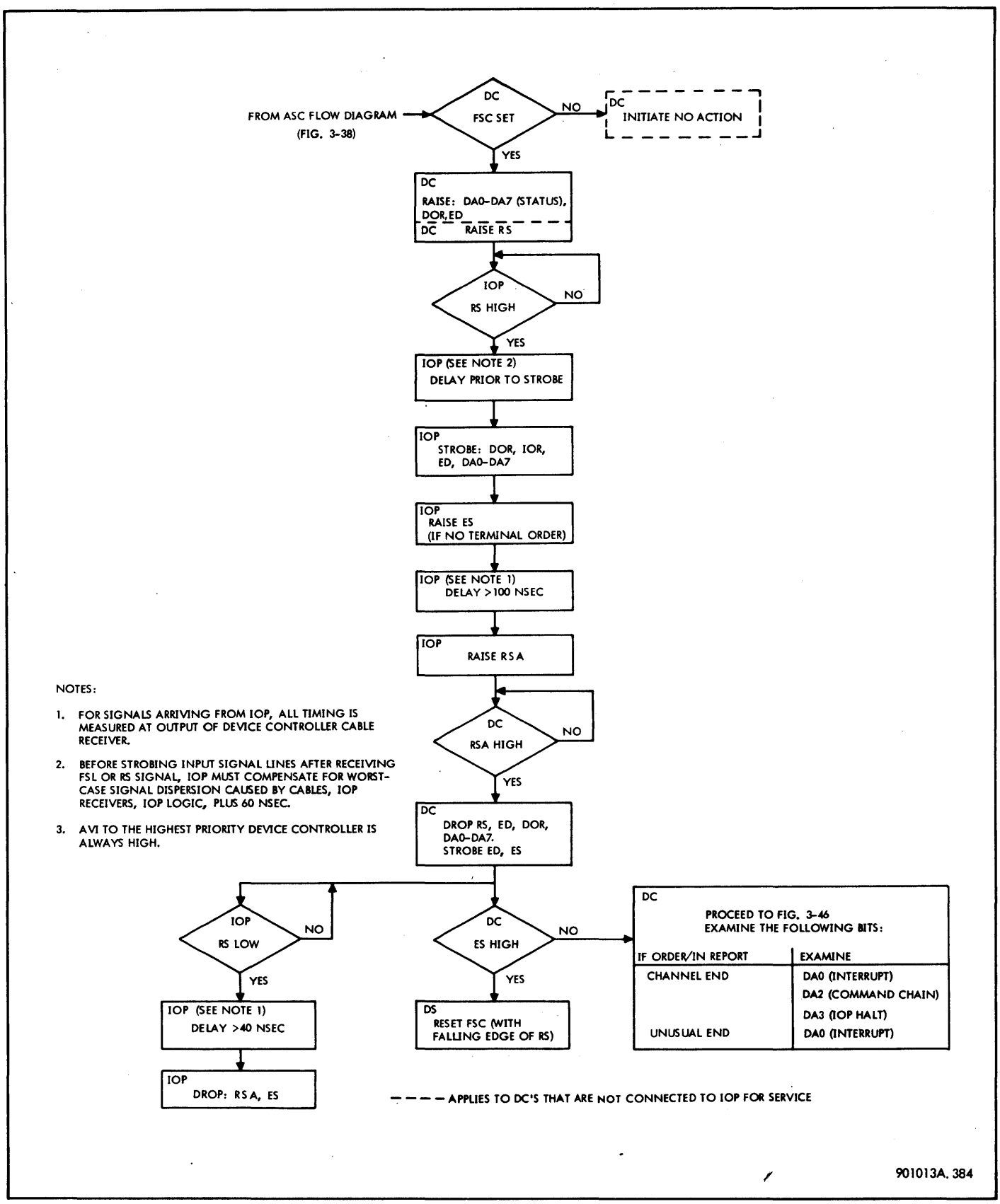


Figure 3-42. Order Input Operation, Flow Diagram

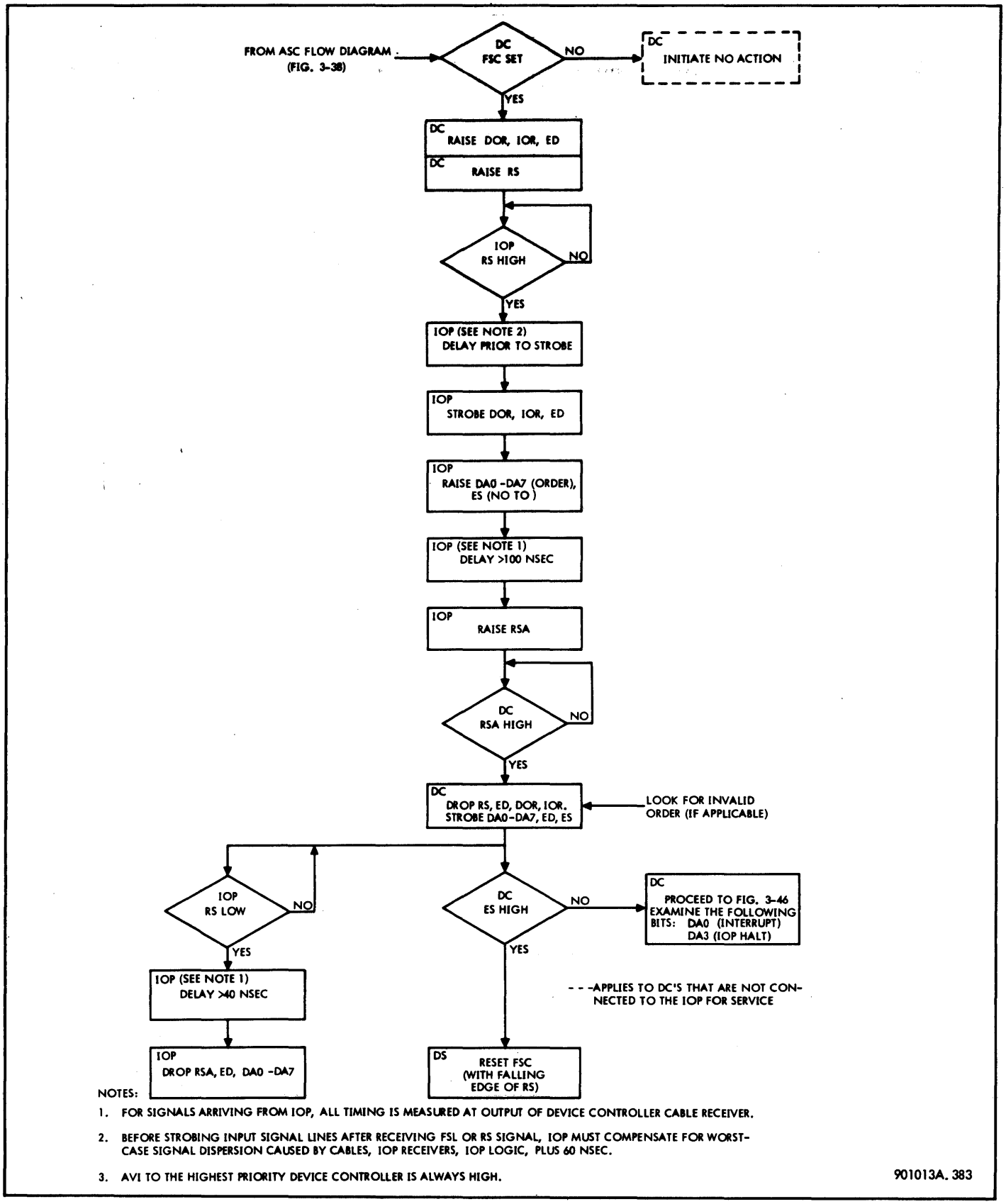


Figure 3-43. Order Output Operation, Flow Diagram

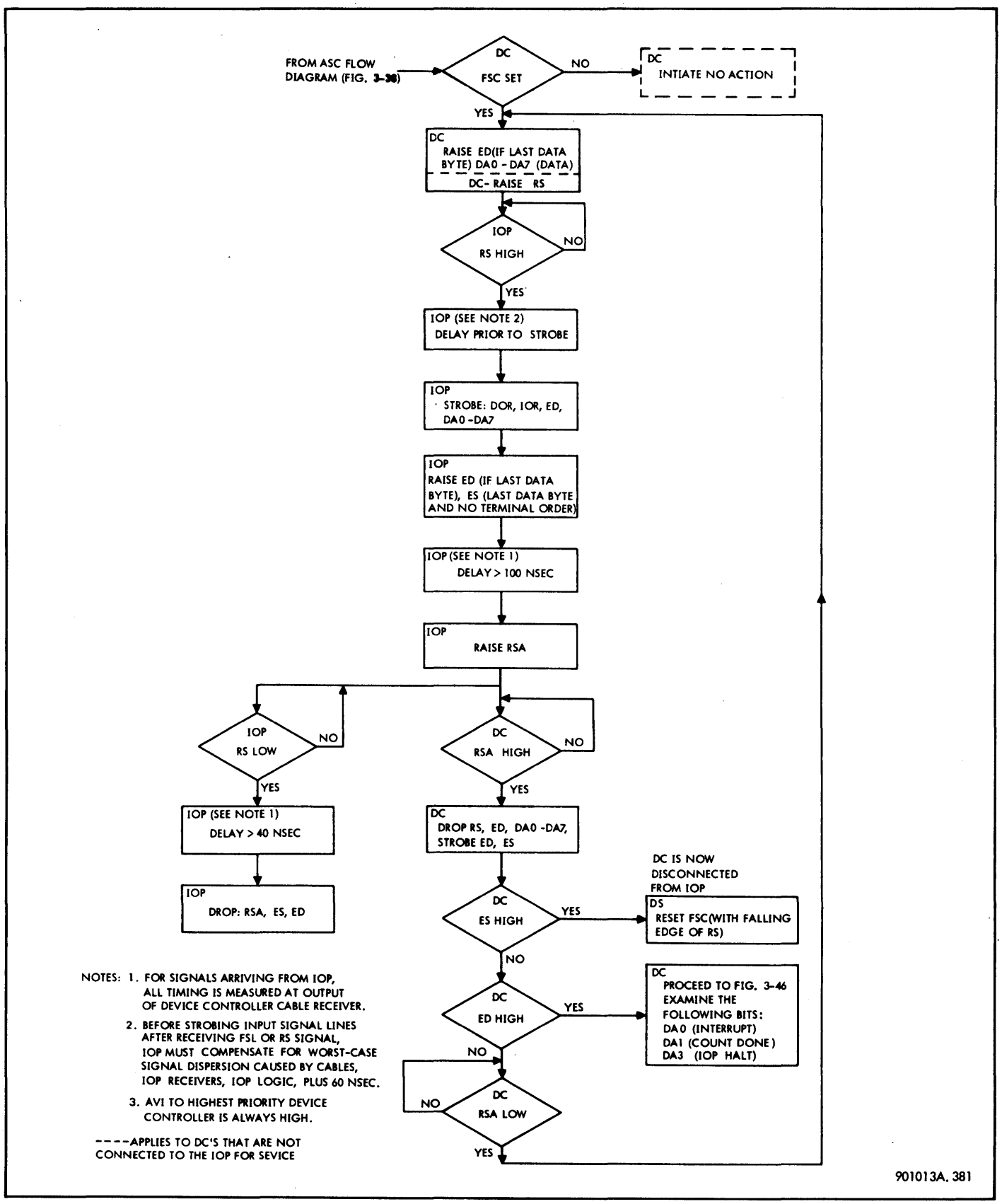


Figure 3-44. Data Input Operation, Flow Diagram

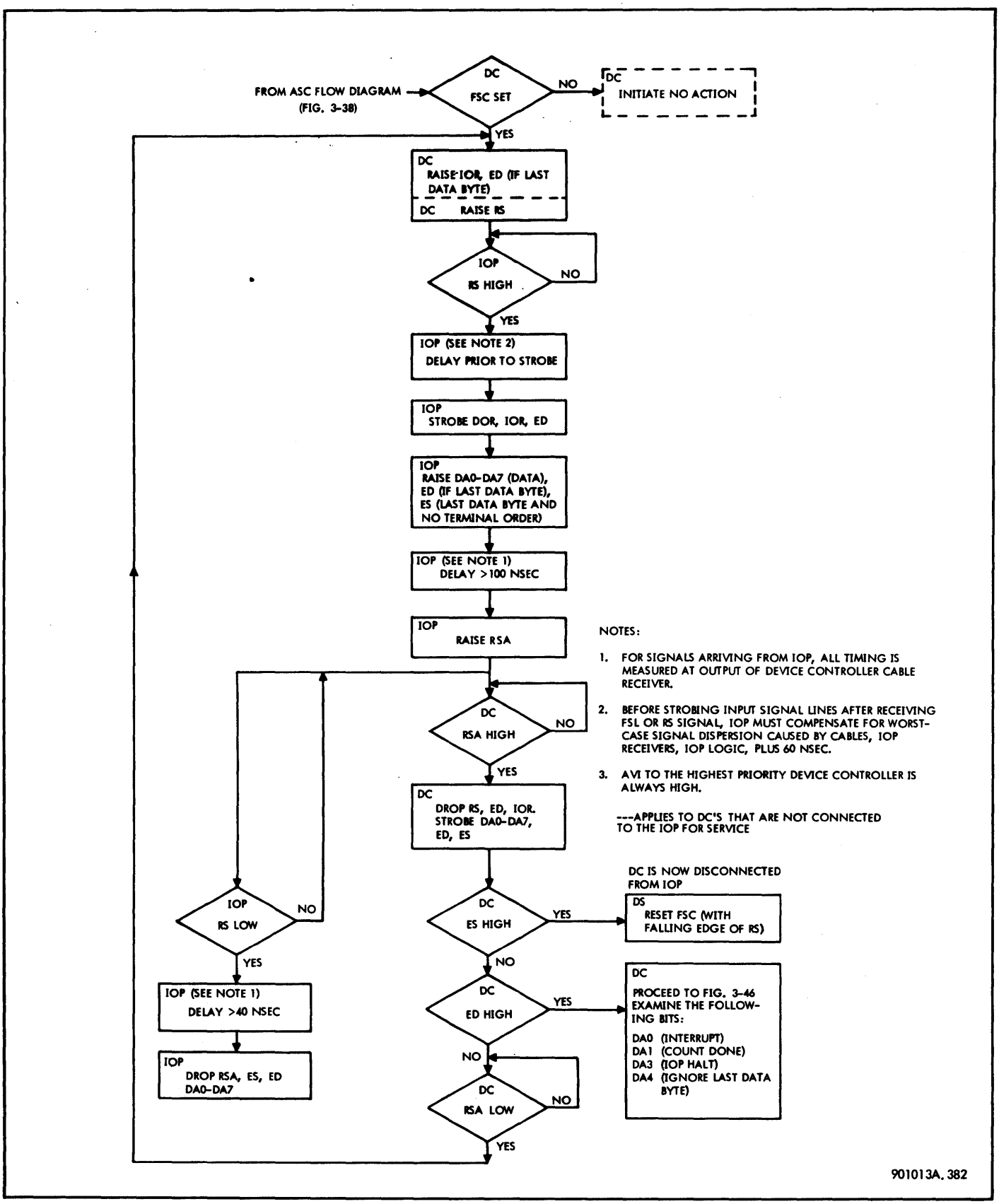


Figure 3-45. Data Output Operation, Flow Diagram

3-47 Terminal Order

A terminal order may be carried out by the controller after any service cycle. The controller initiates the order if ED is high and ES is low. Under these conditions, the controller sends a request strobe signal. The IOP then presents the terminal order information on the data lines.

The next operation of the controller is determined by the data lines that are currently raised, as follows:

Data Line	Operation	Controller Action
0	IOP halt	Data transfer stops and unusual end or channel end is reported
1	Command chain	An order output cycle is initiated after device end
2	Count done	An order input cycle is initiated after channel end and device end
3	Interrupt	An interrupt call is initiated

The end data and end service lines control the termination of a service cycle in the following manner:

End Data	End Service	Definition
0	0	More data to follow
1	0	Last byte. Terminal order requested
x	1	End of service

The end data line can be raised by either the controller or the IOP to indicate a last byte condition. The end service line is controlled by the IOP only. The controller resets FSC when ES is raised. Figure 3-46 shows a flow diagram for a terminal order.

3-48 STATES

The controller goes through eight different states in the performance of its functions. The controller states are determined by the condition of four flip-flops: FF1, FF2, FU1, and FU2. FF1 and FF2 are located in 16Y; FU1 and FU2 are located in 17Y. FF1 and FF2 determine the F phase, while FU1 and FU2 determine the U phase. The four flip-flops and their associated logic circuits constitute the state counter. Figure 3-47 shows a block diagram of the state counter conditions and state transitions.

3-49 00F00U, Idle or Ready

The controller enters the 00F00U state for any of the following reasons:

a. Power is initially applied.

b. The I/O reset is generated by the CPU.

c. The CPU executes a halt instruction.

d. The IOP indicates a halt by a terminal order (unusual end).

e. Channel end takes place without command chaining.

f. The RESET switch on the station has been activated (unusual end, if busy).

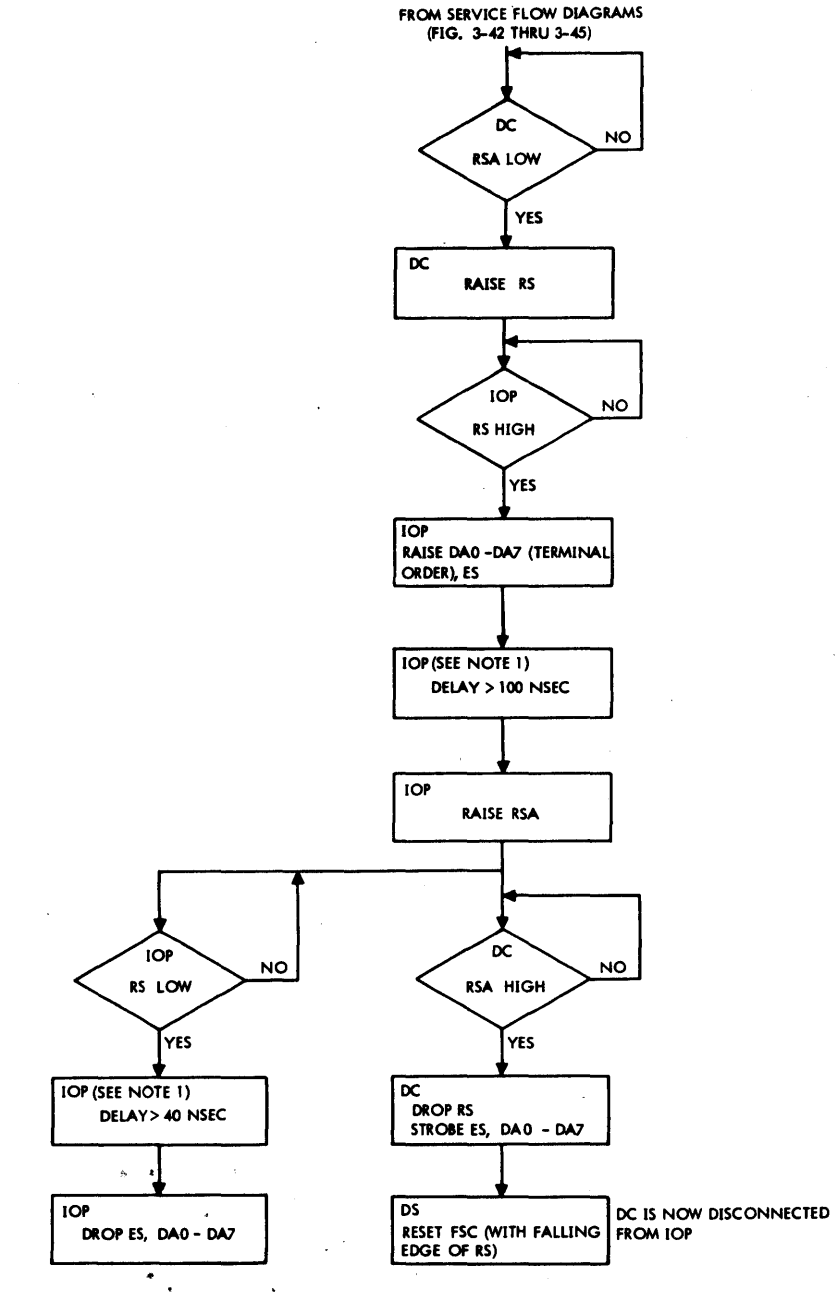
g. An unusual end condition arises.

h. Channel end and device end do not occur at the same time.

During this state, the controller is in an idle or ready condition. It can generate new interrupts or accept an SIO if no interrupts are pending. Upon acceptance of an SIO, the controller advances to the next state. See figure 3-48 for a flow diagram of the SIO operation.

The controller enters state 00F00U when FF1, FF2, FU1, and FU2 are false:

00F	=	NFF1 NFF2
00U	=	NFU1 NFU2
E/FF1	=	RSTA
E/FF2	=	RSTA
RSTA	=	DACFDD HLTD + RSTS
DACFDD	=	DACFD FSR + ATO DACFDD
DACFD	=	(FD1 DA5R) + (NFD1 NDA5R)
		(FD2 DA6R) + (NFD2 NDA6R)
		(FD3 DA7R) + (NFD3 NDA7R)
FSR	=	Function strobe receiver. Receiver output from IOP signal FS
ATO	=	(BAND0 FSD) + (ATO HIOR)
HLTD	=	NFSR ATO
NFSR	=	Inverted output of FSR receiver
RSTS	=	(RSTR + NINI) NMAN
RSTR	=	Receiver output from IOP signal RST (I/O reset signal)
NINI	=	Inverted output of switch contact signal source INI. (Diode clamp gate for power failure or initialize)
NMAN	=	NMANC
NMANC	=	Selector toggle switch output for PET panel
E/FU1	=	RSTS
E/FU2	=	RSTS



NOTES: 1. FOR SIGNALS ARRIVING FROM IOP, ALL TIMING IS MEASURED AT OUTPUT OF DEVICE CONTOLLER CABLE RECEIVER.

2. AVI TO THE HIGHEST PRIORITY DEVICE CONTROLLER IS ALWAYS HIGH.

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Figure 3-46. Terminal Order Operation, Flow Diagram

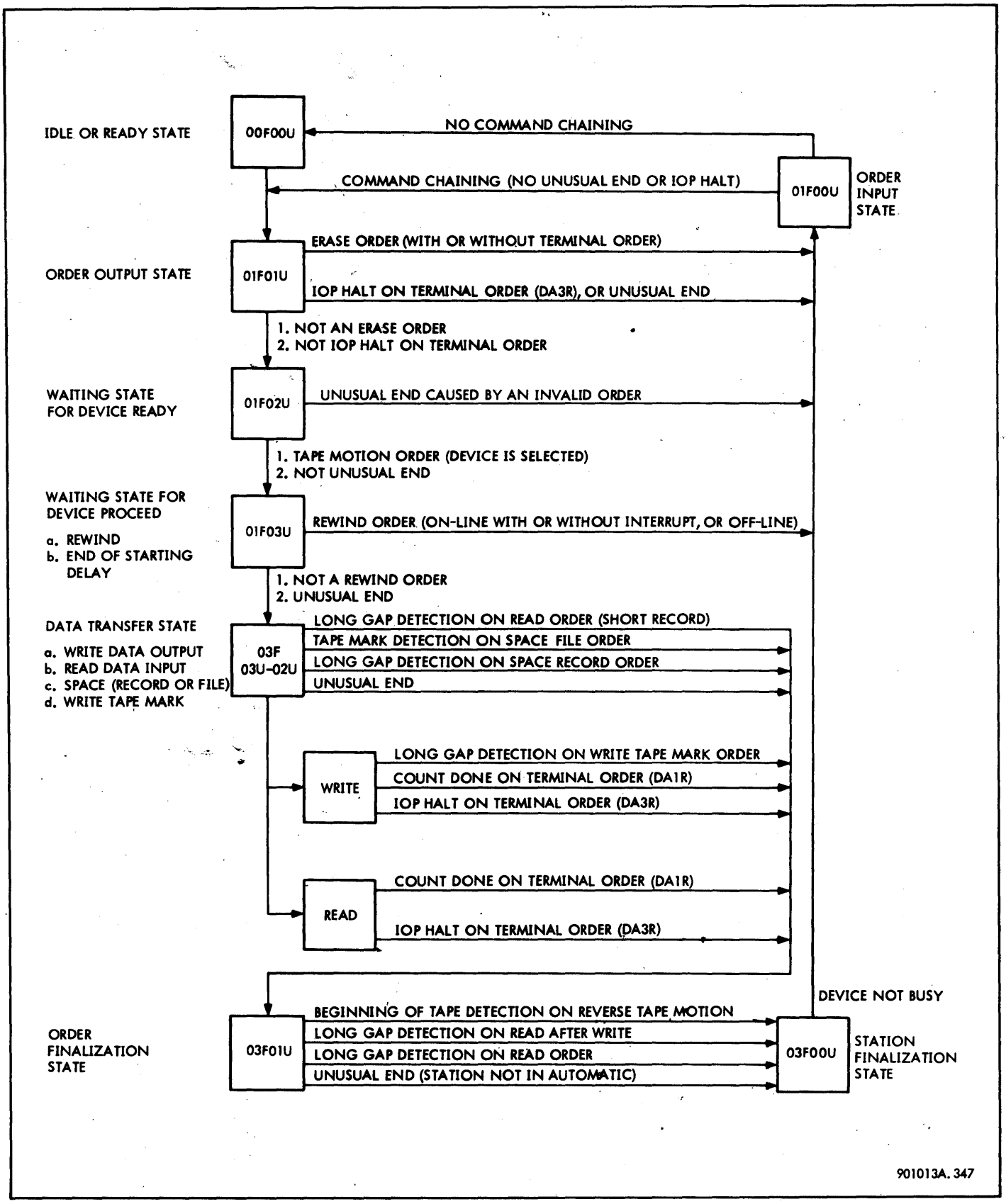

Figure 3-47. Magnetic Tape Controller States, Flow Diagram

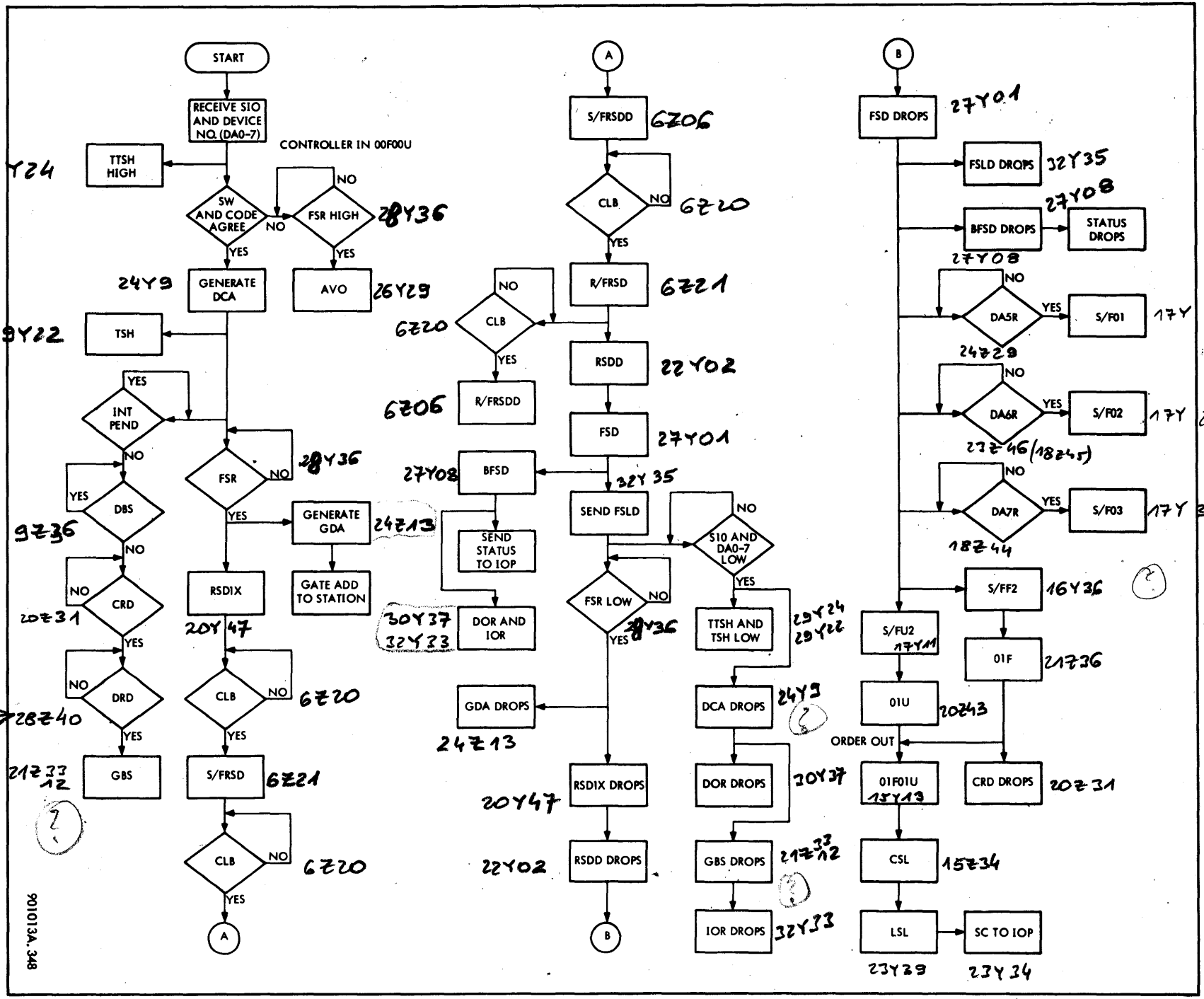

Figure 3-48. SIO Operation, Flow Diagram

When flip-flops FF1, FF2, FU1, and FU2 are reset, the controller raises CRD (controller ready) if there are no pending interrupts:

CRD = NTSH NMAN 00F + 00F NMAN CRD

NTSH = NSIOR NHIOR NTIOR NDCA

The controller is now ready to accept an SIO from the IOP. When the SIO arrives, SIOR (receiver output from IOP signal SIO) is made true. See figure 3-49 for a timing diagram of the 00F00U state.

The IOP raises the device designation on the DA5R, DA6R, and DA7R lines. These lines are connected to the set inputs of flip-flops FD1, FD2, and FD3, respectively:

S/FD1 = DA5R

C/FD1 = GBS FSD

M/FD1 = PETDA1 MAN

PETDA1 = PETDA1C

E/FD1 = RSTA

S/FD2 = DA6R

C/FD2 = GBS FSD

M/FD2 = PETDA2 MAN

PETDA2 = PETDA2C

E/FD2 = RSTA

S/FD3 = DA7R

C/FD3 = GBS FSD

M/FD3 = PETDA3 MAN

PETDA3 = PETDA3C

E/FD3 = RSTA

PETDA1C, PETDA2C, and PETDA3C are used for the PET panel.

The set inputs of the flip-flops selected by the DA lines (FD1, FD2, or FD3) are also made true by the DA lines. The IOP raises FS, and FSR (receiver output from IOP signal FS) is made true. The controller now raises FSD, which makes the clock inputs of FD1, FD2, and FD3 true. When the controller drops FSD, the three flip-flops are clocked, and the ones that have their set inputs true are set. The output from these flip-flops is connected to a decoder. The output of the decoder (DFD0 through DFD7) is routed through other gating circuitry and sent to the IOP as DV0D through DV7D. These lines indicate to the IOP that the correct device has been selected and is now waiting for the next command.

After device selection takes place, term DCA comes true and in turn causes GBS to come true. GBS and FSD cause RESIN to come true. They are also connected to the set and clock inputs of flip-flops FF2 and FU2.

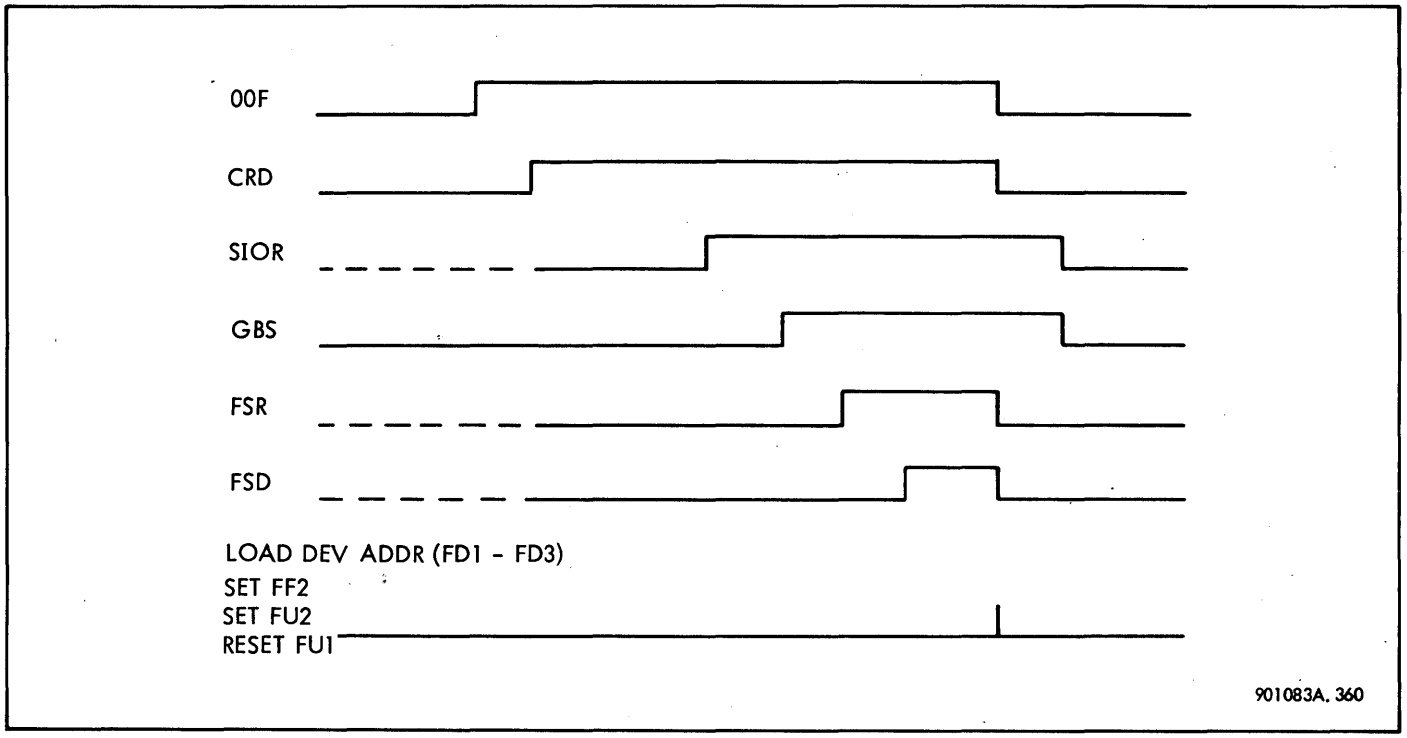

Figure 3-49. 00F00U State, Timing Diagram

RESIN = RSTB + BAND05
S/FF2 = (GBS NFF2) + ...
RSTB = RSTA
BAND05 = GBS FSD
C/FF2 = (GBS FSD) + ...
S/FU2 = (ESR 01F00U) + (NESR 01F01U) + GBSODST
ESR = ESRC NMAN + BOR05 MANA RSD1
ESRC = Receiver output of IOP's ES
BOR05 = BAND28 + FU3
MANA = MANC (selector toggle switch output)
RSD1 = RSD
01F01U = Controller state
GBSODST = GBS + DST
C/FU2 = CFU2
CFU2 = BAND05 + BAND22 SRIPA + CFU2X RSD + CFU2Y CLK
BAND22 = WRITE NWTM FU1
SRIPA = MD3 DLCP
CFU2X = 01F00U + 01F01U + BAND24 NFU3
CFU2Y = BAND20 FU3 + BAND19 + 03F END

RESIN then resets direct-connected (dc) data logic circuits NCRE, RATE, and DATE. When FSD goes false, it clocks both FF2 and FU2 and they set, which advances the controller to the next state.

3-50 01F01U, Order Output

The controller advances to state 01F01U for either of the following reasons:

a. An SIO has been accepted from the IOP.

b. The controller has reported channel end with command chaining.

In this state, the controller requests service from the IOP by raising signal CSL. After the controller is connected to the IOP for service, the order for the function to be performed is sent from the IOP. After the order is received, the controller advances to state 01F02U. Refer to figure 3-50 for a flow diagram of the 01F01U state.

When 01F01U comes true and if term ESR is false, flip-flops FUN, FCN, FPE, FLE, and FIO are reset:

E/FUN = BOR03
BOR03 = RSTB + BAND06
RSTB = RSTA
BAND06 = 01F01U NESR
E/FCN = BOR03
E/FPE = BOR03
E/FLE = RSTB
E/FIO = RSTA

The controller also raises CSL:

CSL = CSLX CSLI
CSLX = (01F01U + 01F00U) + (BAND22 BAND30 + BAND24 BAND30)
BAND24 = FU1 READ
BAND30 = BMT NFUN
CSLI = Service request inhibit signal

The IOP then raises ASC (acknowledge service call), FS (function strobe), and AVI (available input). These signals are used to generate the set input for service connect flip-flop FSC:

S/FSC = ASCB
ASCB = ASCR FSR AVIR ASCM
ASCR = Acknowledge service call receiver output signal from IOP's ASC
FSR = Function strobe receiver output signal from IOP's FS
AVIR = Available signal receiver output
ASCM = LSH + LSL NHPSL
LSH = CSH CSL NFSC INC NASCR + LSH NRSTR ASCR INI NFSC
LSL = CSL INC NFSC NASCR + LSL NRSTR NFSC ASCR INI
NHPSL = NHPSR NASCR + NASCR NHPSL

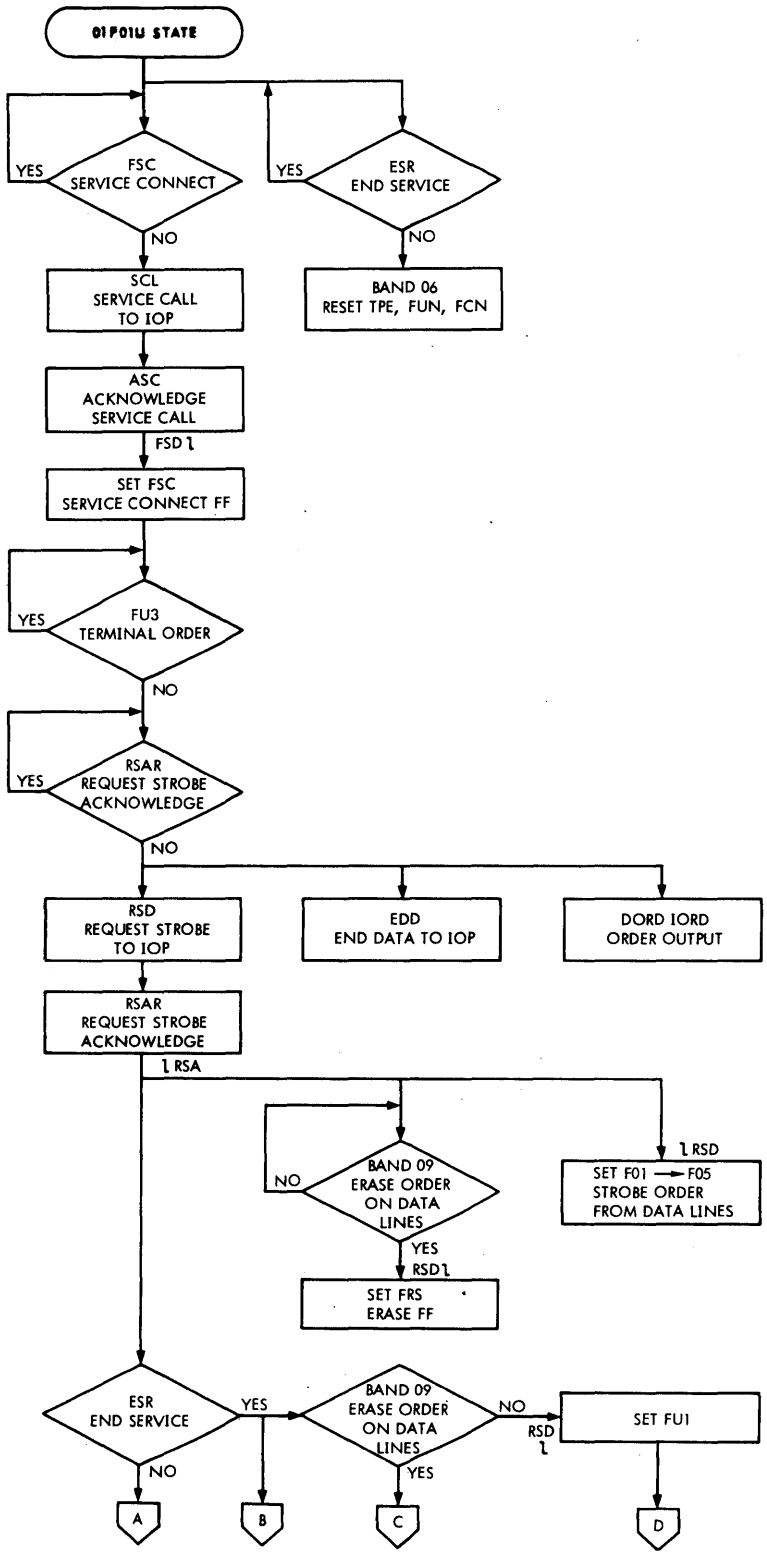

Figure 3-50. 01F01U State, Flow Diagram (Sheet 1 of 2)

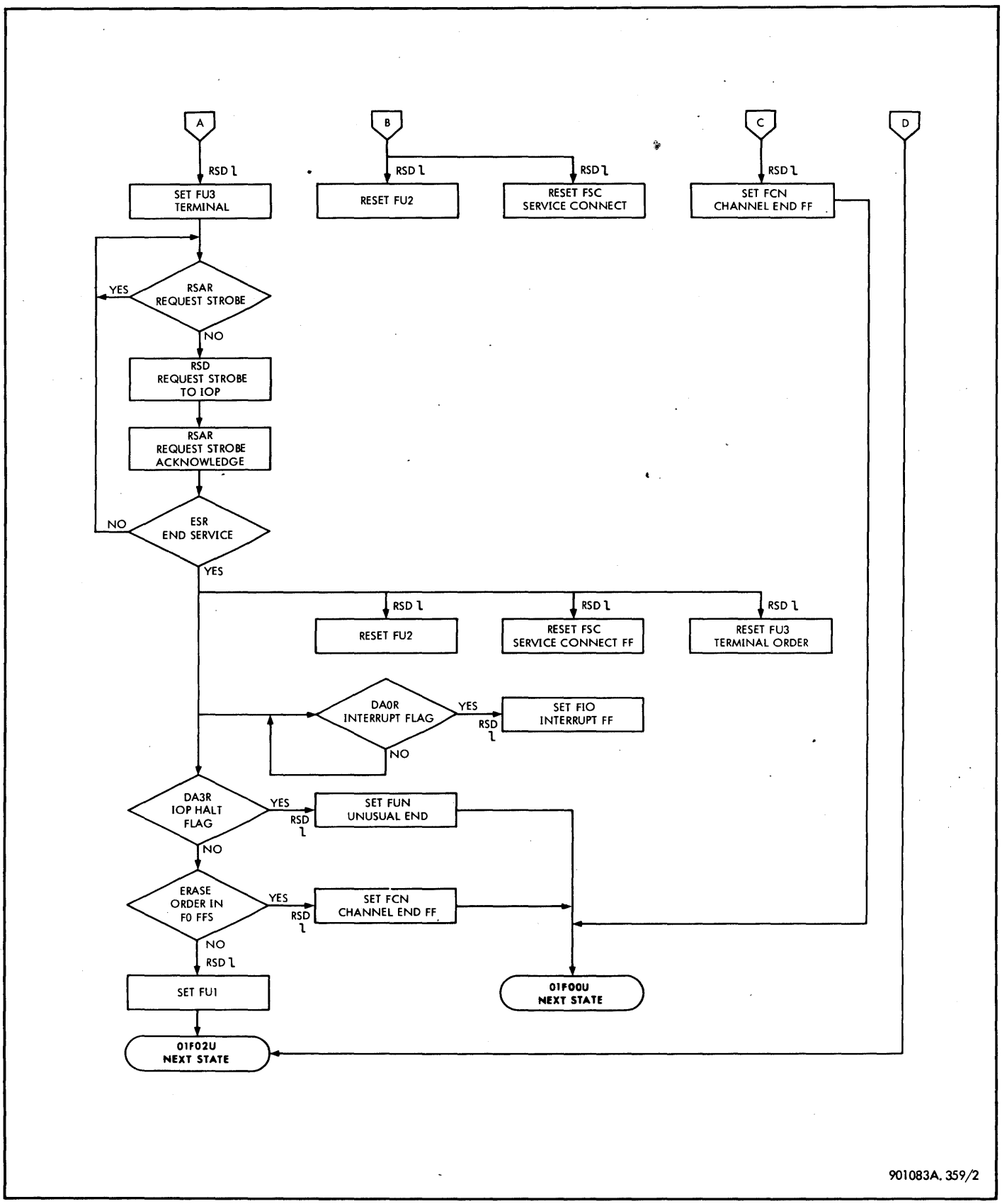

Figure 3-50. 01F01U State, Flow Diagram (Sheet 2 of 2)

The set and clock inputs for FSC are made true. When FSR goes false, FSC is clocked and sets. At this time, the RSD (request strobe driven), DORD (order request), IORD (output request), and EDD (end data) lines are made true:

DORD = BAND08 + BAND13 + BAND01 + DCA TTSH ARG

BAND08 = 01F01U NFU3 RSD

BAND13 = 01F00U NFU3 RSD

TTSH = SIOR + HIOR + TIOR + TDVR

ARG = Address recognized by station

IORD = (DRD TDVR DCA) + (DCA TDVR DBS) + IORDY + BAND08 + (NFUN BAND01) + (BAND22 BAND16) + GBS + [BAND04 (CRD + NDACFD)]

TDVR = Test device line receiver output

DBS = Device busy signal (from station)

IORDY = (DCA TIOR DRD) (NDBS NINTPEND CRD)

BAND16 = NFU3 RSD

BAND04 = DCA HIOR

EDD = EDDX + BAND08 + FSCC EDB BAND31

EDDX = BAND13

EDB = BMTC MCO1

BAND31 = FU1 NFU3 READ

The DORD and IORD lines are used by the controller to specify to the IOP the type of communication which is to take place. The DORD and IORD line designations are as follows:

	DORD	IORD
Order out	1	1
Order in	1	0
Data out	0	1
Data in	0	0

DORD and IORD are both true in this phase, which is an order out cycle.

The order that the IOP places on the DA0 through DA7 lines is impressed on the set inputs of flip-flops FO1 through FO5:

S/FO1 = DA6R DA7R

S/FO2 = DA4R

S/FO3 = (DA6R DA7R) DA1R + (NDA6R + NDA7R) DA5R

S/FO4 = (DA6R DA7R) DA2R + (NDA6R + NDA7R) DA6R

S/FO5 = (DA6R DA7R) DA3R + (NDA6R + NDA7R) DA7R

C/FO1-C/FO5 = 01F01U NFU3 RSD

When 01F01U, NFU3, and RSD are true, the IOP raises RSA (request strobe acknowledge); at that time, RSD goes false and clocks the flip-flops:

RSD = NRSAR RSDX + ...

The flip-flops set to the order on their set inputs. The controller now performs its logic functions and advances to one of two possible states, either 01F00U (order input) or 01F02U (device selection), depending upon the order that is in flip-flops FO1 through FO5.

If the order in the controller is an erase order, the IOP raises ESR (end service). Flip-flops FCN (channel end) and FRS (erase) are set, and FU2 and FSC (service connect) are reset.

S/FCN = NFCN + SFCN

SFCN = [(NFU3 BAND09 BAND11) + (BAND11 BAND12 FRS)] + BAND19 + 03F00U

BAND09 = DA1R DA2R NDA3R DA6R DA7R

BAND11 = 01F01U ESR

S/FRS = SFRS

SFRS = SFCROFRS + BAND09 BAND10

SFCROFRS = (NBORO6 + NESR) 01F00U

BAND10 = 01F01U NFU3

C/FRS = CFRS

CFRS = CFRSX RSD

CFRSX = NFRS BAND10 + FRS 01F00U

M/FRS = (M/FRS)

(M/FRS) = DST FO1345

FO1345 = FO1 FO3 FO4 FO5

E/FRS = RSTA

C/FU2 = CFUX RSD + ...

C/FSC = RSD FSC + ...

R/FSC = ESRC FSC

When RSD goes false, FCN and FRS are clocked and set, and FU2 and FSC are clocked and reset. The controller then advances to the next state, 01F00U (order input).

If a terminal order had been required, the IOP would not have raised ESR immediately. Then, FU3 (terminal order) would have set, and FU2 and FSC would have remained set when RSD went false:

S/FU2 = BAND20 DSG NFU3
+ EDR NESR FSCC

BAND20 = DST NFUN

DST = 01F02U

DSG = Device selected signal (from station)

The controller raises RSD again, and the IOP raises RSA and ESR. When RSA goes true, RSD goes false and clocks and resets flip-flops FU2, FU3, and FSC; the controller again advances to state 01F00U. If the IOP gives an interrupt to the controller in the terminal order (DA0 true), flip-flop FIO (interrupt) sets when RSD goes false.

S/FIO = DAOR SFIO

SFIO = FU3 NDST

If the IOP gives a halt command to the controller in the terminal order (DA3R true), flip-flop FUN (unusual end) sets when RSD goes false:

S/FUN = SFUN

SFUN = SFUNX + CFUNX

SFUNX = FU3 NDST ESR DA3R

If there is an erase order in the controller, FCN sets when RSD goes false. Flip-flops FU2 and FSC reset when RSD goes false and the controller has advanced to the next state, 01F00U.

If there is not an erase order in the controller, flip-flop FU1 sets, and FU2 and FSC reset when RSD goes false:

S/FU1 = SFU1

SFU1 = SFU1X + 03F00U

SFU1X = (BAND22 NBAND23 FSCC)
+ (NBAND23 BAND24 FSCC)
+ (NFU3 NBAND09 BAND11)
+ (BAND11 BAND12 FO134NFO51)

The controller then advances to 01F02U (waiting for device ready). Figure 3-51 shows a timing diagram for the 01F01U state.

3-51 01F02U, Waiting for Device Ready

In this state, the controller separates valid and invalid orders and connects the device for operation. The controller then advances to state 01F03U (waiting for device proceed). See figure 3-52 for a flow diagram of the 01F02U state.

The controller enters the 01F02U state, and DST (device select time) comes true:

DST = 01F02U

If the controller contains a write order when entering the 01F02U state, WRT comes true:

WRT = (FO1345 + FO5NFO14) NFPET1

FO1345 = FO1 FO3 FO4 FO5

FO5NFO14 = FO5 NFO1 NFO4

NFPET1 = Flip-flop output for PET panel

If the controller does not contain a write order, FRS (erase flip-flop) remains reset. IVO (invalid order) comes true for the following reasons:

a. BTSC (load point control) in the station FO1, and FO2 are true:

IVO = BTS FO1 FO2 (Reverse function at BOT)

b. Arriving orders are not used in the 7371 mode:

IVO = NFO4 NFO5 (FO1 NFO3 + NFO1)

c. WRT and NWPM are true:

IVO = WRT NWPM (Write when file protected)

If WRT and NWPM are true, FPE (write protect violation) is set when CLK goes false:

S/FPE = NWPM WRT

NWPM = Not file protected

WRT = Write operation

C/FPE = CLK BAND17

BAND17 = DST NOR01 AUT

DST = 01F02U

NOR01 = (NDCA + NTTSH) NAIOR

If IVO is true, FUN (unusual end) sets when CLK goes false:

S/FUN = IVO BAND17 + ...

C/FUN = CLK CFUNX + ...

FU1 resets the next time that CLK goes false, and the controller now advances to state 01F00U (order input) on an invalid order.

Assume that the order in the controller is correct. DSS (device select) is then true:

DSS = NIVO BAND17

DSG (device select gate) from the station comes true, and FU3 sets when CLK goes false:

S/FU3 = DSG BAND20 NFU3 + ...

C/FU3 = CLK DST + ...

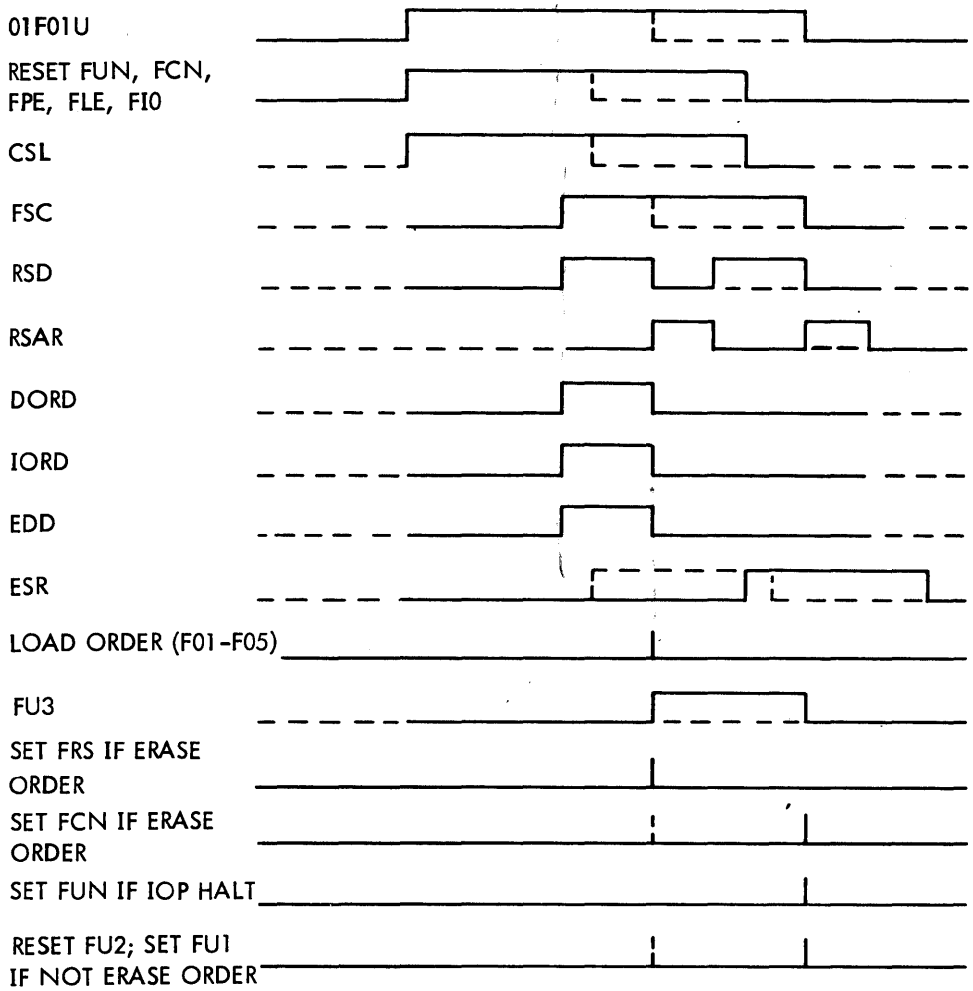

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Figure 3-51. 01F01U State, Timing Diagram

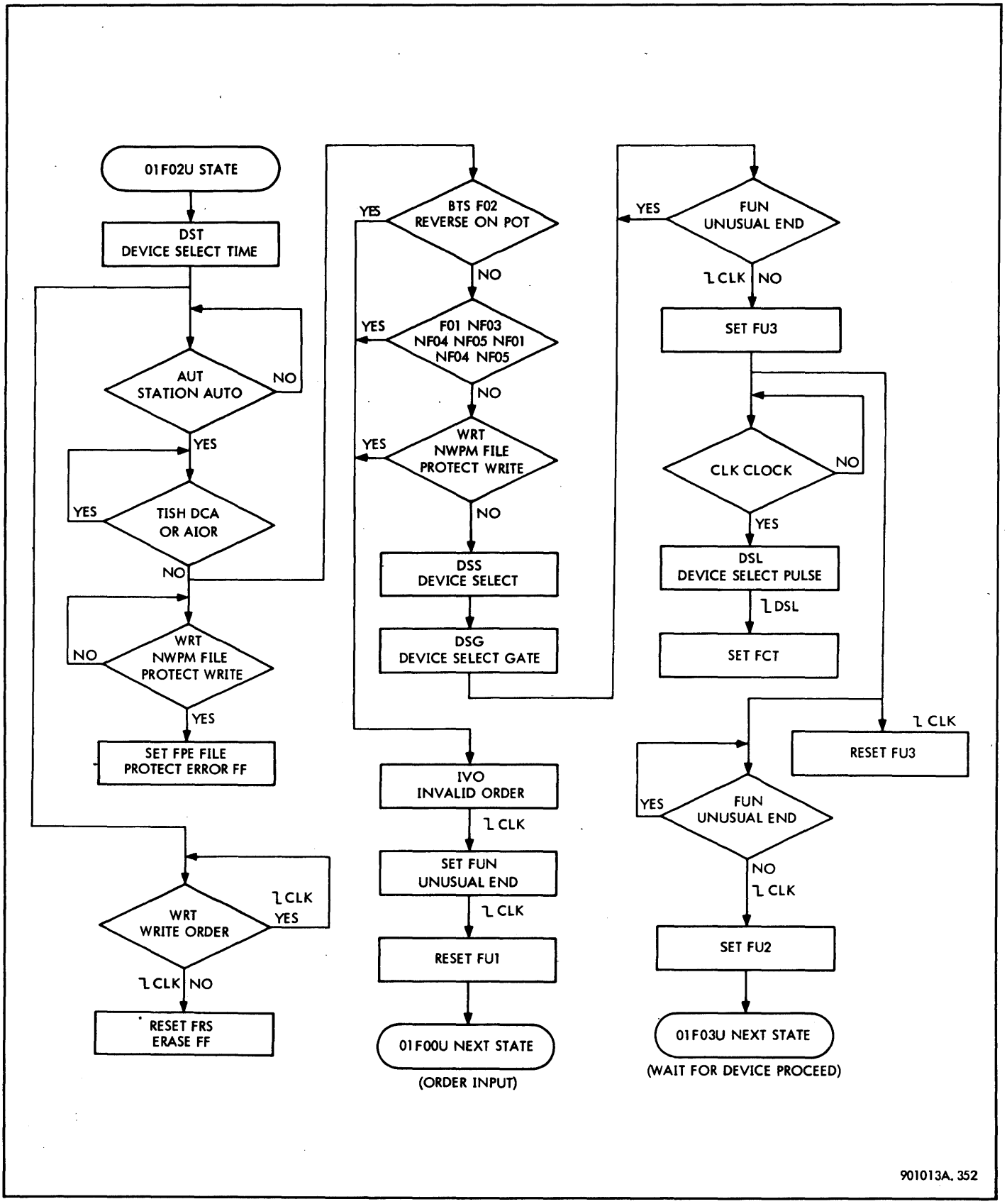

Figure 3-52. 01F02U State, Flow Diagram

DSL comes true the next time that CLK comes true:

DSL = CLK FU3 DST

When CLK goes false, FU3 resets, DSL goes false, and FU2 sets. When DSL goes false, it sets FCT (device connect flip-flop) in the station. When FU2 is set, the controller advances to the next state, 01F03U (wait for device proceed), on a device select order. Figure 3-53 shows a timing diagram for the 01F02U state.

3-52 01F03U, Waiting for Device Proceed

The controller advances to the 01F03U state and enters a waiting phase for a device proceed order. This phase ends with either a rewind order or an end of starting delay. See figure 3-54 for a flow diagram representation of the 01F03U state.

REWIND. When the controller enters state 01F03U, RES is made true:

RES = 01F03U NDPR + ...

RES is used as one of the reset signals for the data logic circuits.

When DPR (device proceed) in the station comes true, it is AND-connected with the rewind order (WN1O2) at the clock inputs of FCN, FU1, and FU2:

WN1O2 = WN1 + WN2
WN1 = FO1 NFO3 FO5
WN2 = FO1 NFO3 FO4
C/FCN = CLK CFCNX + ...
CFCNX = BAND19 + ...
BAND19 = 01F03U DPR WN1O2
C/FU1 = CLK CFU1Z + ...
CFU1Z = BAND19 + ...
C/FU2 = CLK CFU2Y
CFU2Y = BAND19 + ...

When CLK goes false, it clocks and sets FCN, and resets FU1 and FU2. The controller now advances to the 01F00U state (order input), on a rewind order.

END OF STARTING DELAY (NOT A REWIND). When the controller enters state 01F03U, RES is made true. When DPR in the station comes true, it makes the set input of FF1 true (when the operation is not a rewind):

S/FF1 = DPRNWN + ...
C/FF1 = CLK 01F03U
DPRNWN = DPR NWN1O2

When CLK comes true, it makes the clock input of FF1 come true; when CLK goes false, FF1 is clocked and sets. The controller now advances to state 03F03U (data transfer).

When the 01F03U state is entered, if DCA or TTSH is false, AIOR is false, and AUTO is not true, FUN (unusual end) is clocked and set.

C/FUN = BAND29 01F03U + ...
BAND29 = NOR01 NAUT
NOR01 = (NDCA + NTTSH) NAIOR

When FUN comes true, it makes the set input of FF1 true:

S/FF1 = FUN + ...

When CLK comes true, it makes the clock input of FF1 true; and when CLK goes false, FF1 is clocked and sets. The controller now advances to state 03F03U (data transfer) on an unusual end order. Figure 3-55 shows a timing diagram for the 01F03U state.

3-53 03F03U-02U, Data Transfer

The controller advances to state 03F03U-02U and may enter one of the following phases: write, read, space file, or space record. The write and read functions are described in the last part of this section under the heading Magnetic Tape System Functions (paragraphs 3-57 through 3-70). The space file and space record phase description is given below. Figure 3-56 shows a flow diagram for the 03F03U-02U state.

SPACE FILE ORDER. When the controller advances to state 03F03U-02U and it contains a space file order, WRT is false and FO1 and SPF are true:

S/FO1 = DA6R DA7R
SPF = BAND21 FO5
BAND21 = 03F FO1 FO3 NFO4

When the tape mark record is detected, TM comes true. When CLK comes true, it makes the clock input of FU1 true; when it goes false, it clocks and resets FU1. See figure 3-57 for a timing diagram of the space file operation.

C/FU1 = CLK SPF TM + ...

The controller now advances to state 03F01U on a space file order.

If TM does not come true on a space file order, LG comes true and causes RES to come true:

RES = NTM LG SPF + ...

RES is used as a reset signal in the data logic circuits.

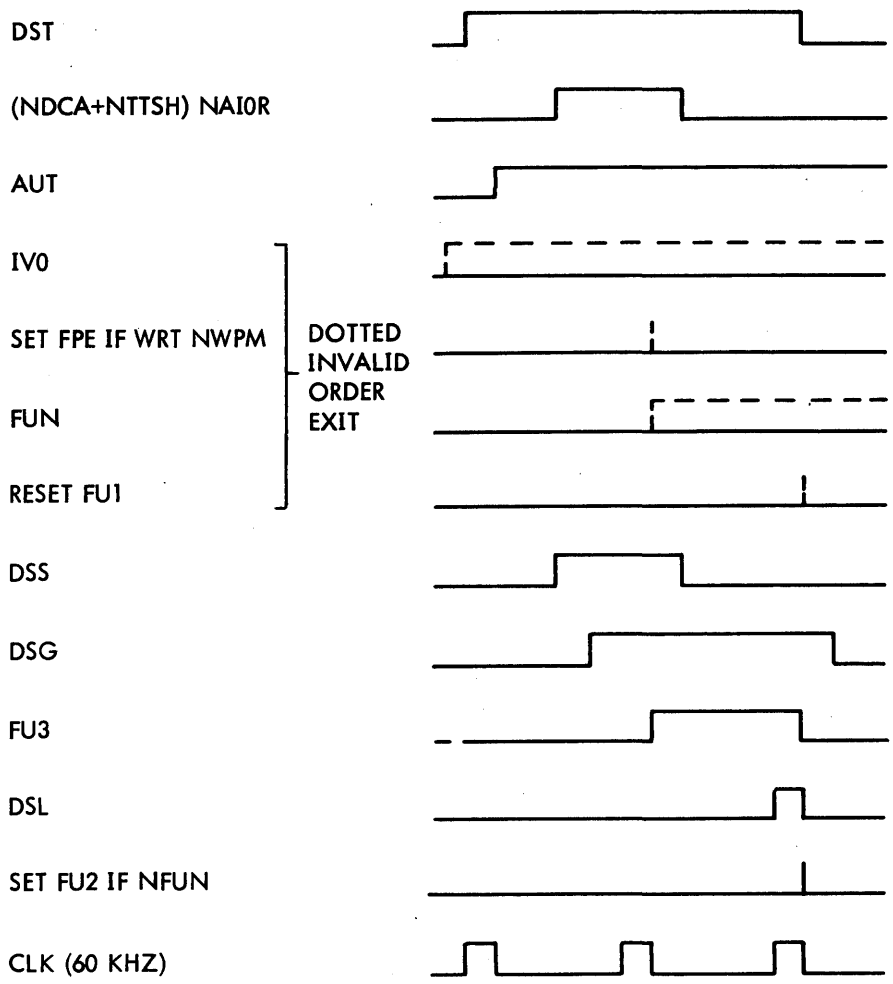

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Figure 3-53. 01F02U State, Timing Diagram

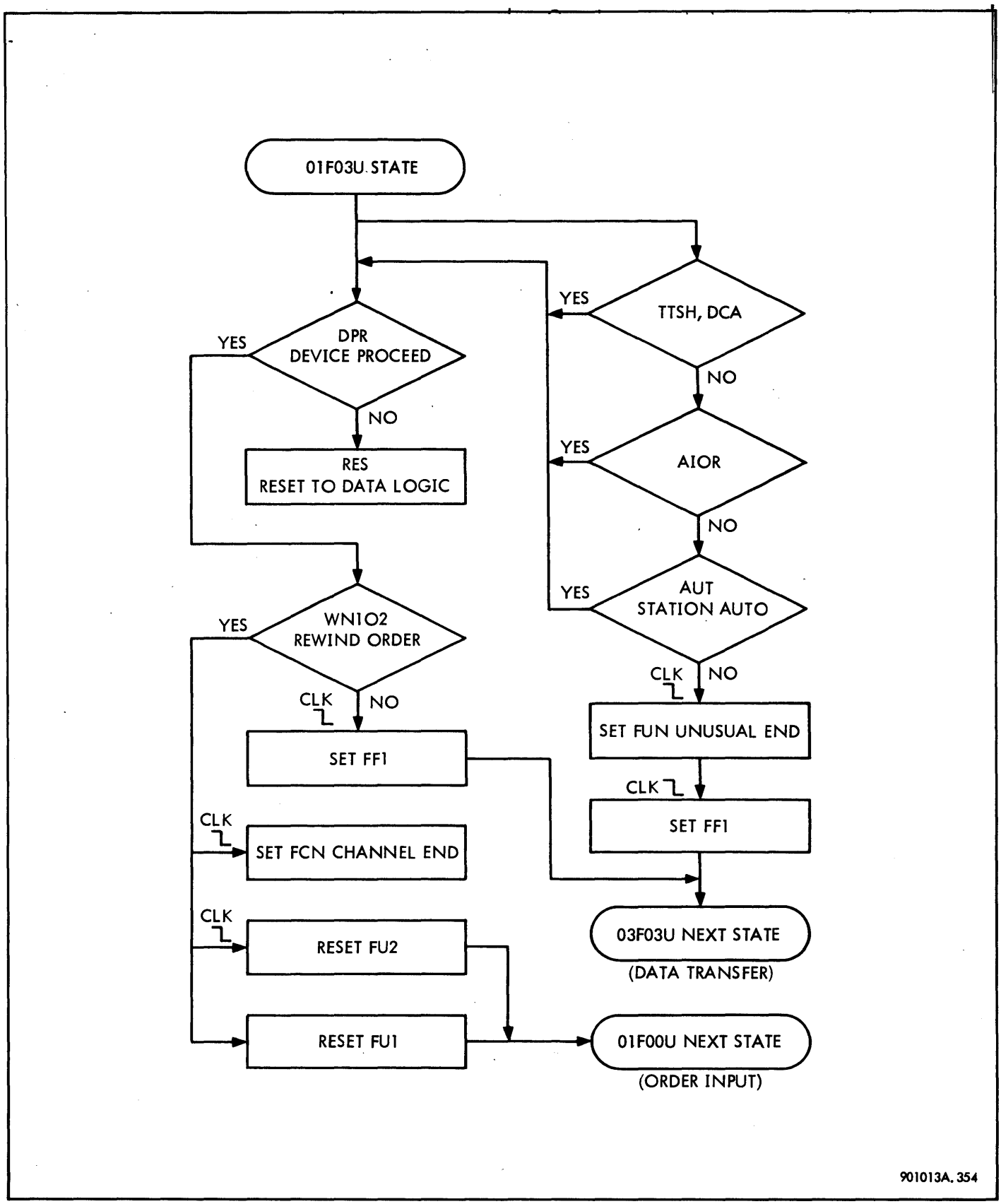

Figure 3-54. 01F03U State, Flow Diagram

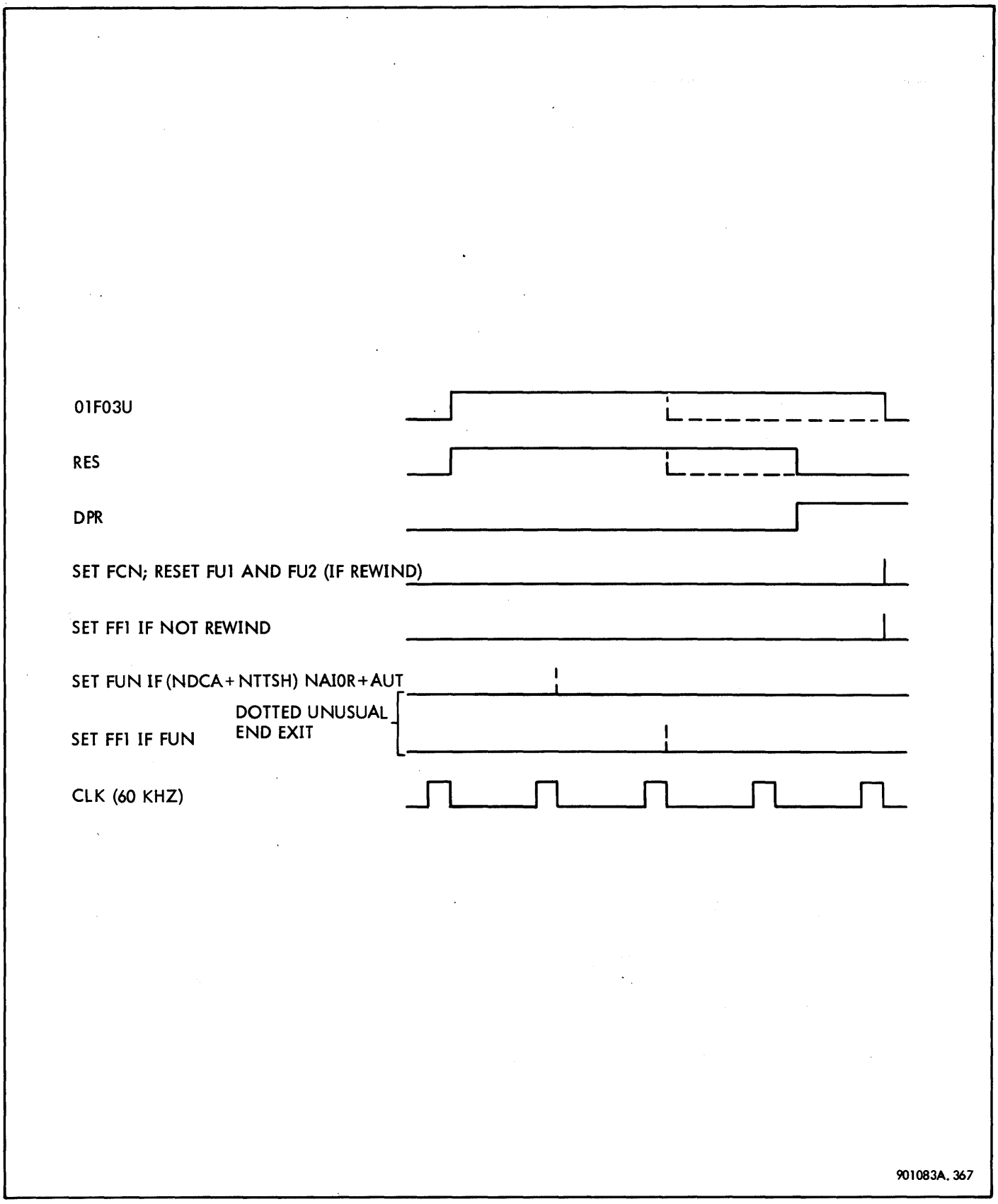

Figure 3-55. 01F03U State, Timing Diagram

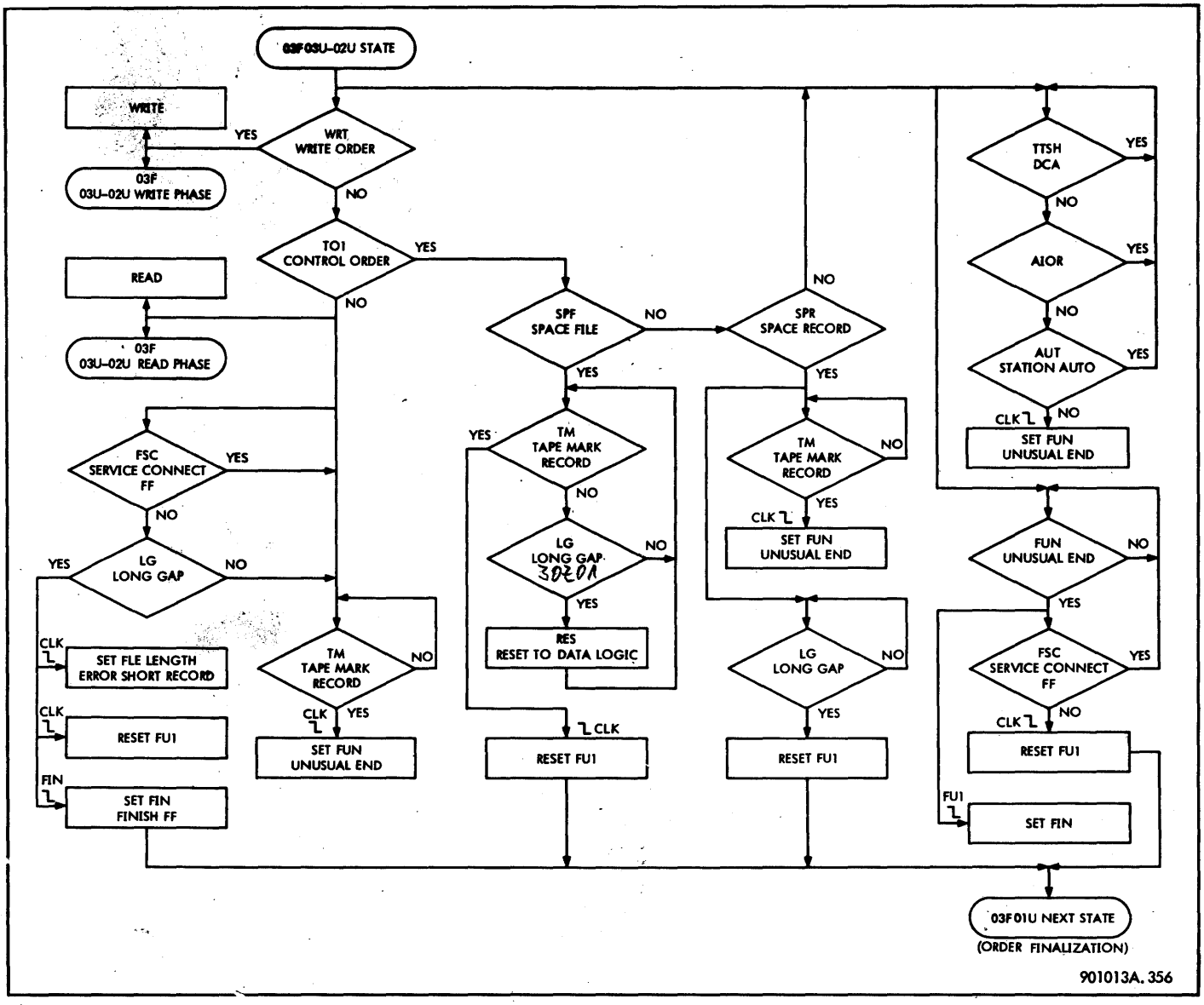

Figure 3-56. 03F03U-02U State, Flow Diagram

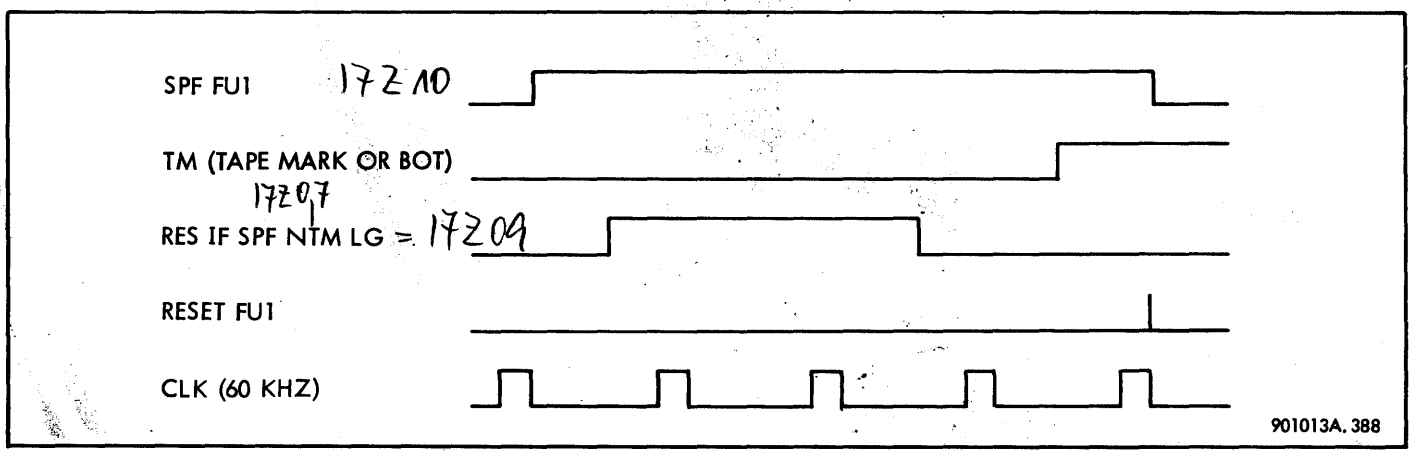

Figure 3-57. 03F03U State (Space File), Timing Diagram

SPACE RECORD ORDER. When the controller advances to state 03F03U-02U and it contains a space record order, WRT and SPF are false and SPR is true:

SPR = BAND21 NFO5
BAND21 = 03F FO1 FO3 NFO4

LG is connected to the clock input of FU1. When LG and CLK come true, the clock input of FU1 is made true; when CLK goes false, FU1 is clocked and resets:

C/FU1 = SPR LG CLK + ...

The controller now advances to state 03F01U on a space record order. See figure 3-58 for a timing diagram of the space record operation.

If TM comes true (before LG), unusual end flip-flop FUN sets:

S/FUN = TM READ FU1 + ...
C/FUN = TM READ FU1 CLK + ...

TM is connected to the set and clock inputs of FUN. When TM comes true, it makes the set input of FUN true. When CLK comes true, it makes the clock input of FUN true; when it goes false, it clocks and sets FUN.

FUN is connected to the clock input of FU1. When CLK comes true, it makes the clock input of FU1 true. When CLK goes false, FU1 is clocked and resets. The controller has now advanced to state 03F01U on a space record error:

C/FU1 = FUN CLK NFSCC 03F + ...

UNUSUAL END. If FUN (unusual end) is true and FSC (service connect) is false when the controller enters state 03F03U-02U, it immediately advances to state 03F01U. FUN is connected to the clock inputs of FU1 and FIN:

C/FU1 = FUN CLK NFSCC 03F + ...
C/FIN = FU1 FUN 03F + ...

When CLK comes true, the clock input of FU1 is made true, and when it goes false, it clocks and resets FU1. When FU1 goes false, it clocks and sets FIN. The controller now advances to state 03F01U on an unusual end condition.

When the controller advances to state 03F03U-02U, DCA, TTSH, AIOR, and AUTO are false and FUN sets:

C/FUN = 03F BAND29 CLK
BAND29 = NDCA NTTSH NAIOR NAUT

When CLK comes true, it makes the set input of FUN true; when it goes false, it clocks and sets FUN. FUN is connected to the clock input of FU1; when it goes false, it resets FU1, which advances the controller to state 03F01U.

3-54 03F01U, Order Finalization

The 03F01U state is the order finalization (or terminate process) state. In this state, the read, write, space record, and space file orders from the preceding state (03F03U-02U) are terminated. Figure 3-59 shows a flow diagram for the 03F01U state.

When the controller enters the 03F01U state on a read or write order, that order remains true.

If FUN is true on a read order, however, it will dc-set FLE (length error flip-flop), indicating a long record:

M/FLE = READ 01U FUN + ...

If FUN is false and BMT is true on a read order, FLE is dc-set by BMT:

M/FLE = READ 01U BMT + ...

LG DETECTION ON READ OR READ-AFTER-WRITE ORDERS. When the controller enters this phase, if LG comes true, END comes true:

END = 03F NFU1 ENDX
ENDX = ENDY + BAND29
ENDY = LG + (FO2 FO1 BOT)
BAND29 = NDCA NTTSH NAIOR NAUT

END is connected to the clock input of FU2:

C/FU2 = CLK END 03F + ...

See figure 3-60 for a timing diagram of the terminate process operation.

When CLK comes true, it makes the clock input of FU2 true; when it goes false, it clocks and resets FU2, advancing the controller to state 03F00U (station finalization).

BEGINNING OF TAPE DETECTION ON REVERSE TAPE MOTION. If FO2 FO1 (reverse order) is true when the controller enters this state and BOT (beginning of tape) comes true, END comes true:

END = 03F NFU1 (FO2 FO1 BOT + ...)

END is connected to the clock input of FU2:

C/FU2 = CLK END 03F + ...

When CLK comes true, it makes the clock input of FU2 true; when it goes false, it clocks and resets FU2, which advances the controller to state 03F00U.

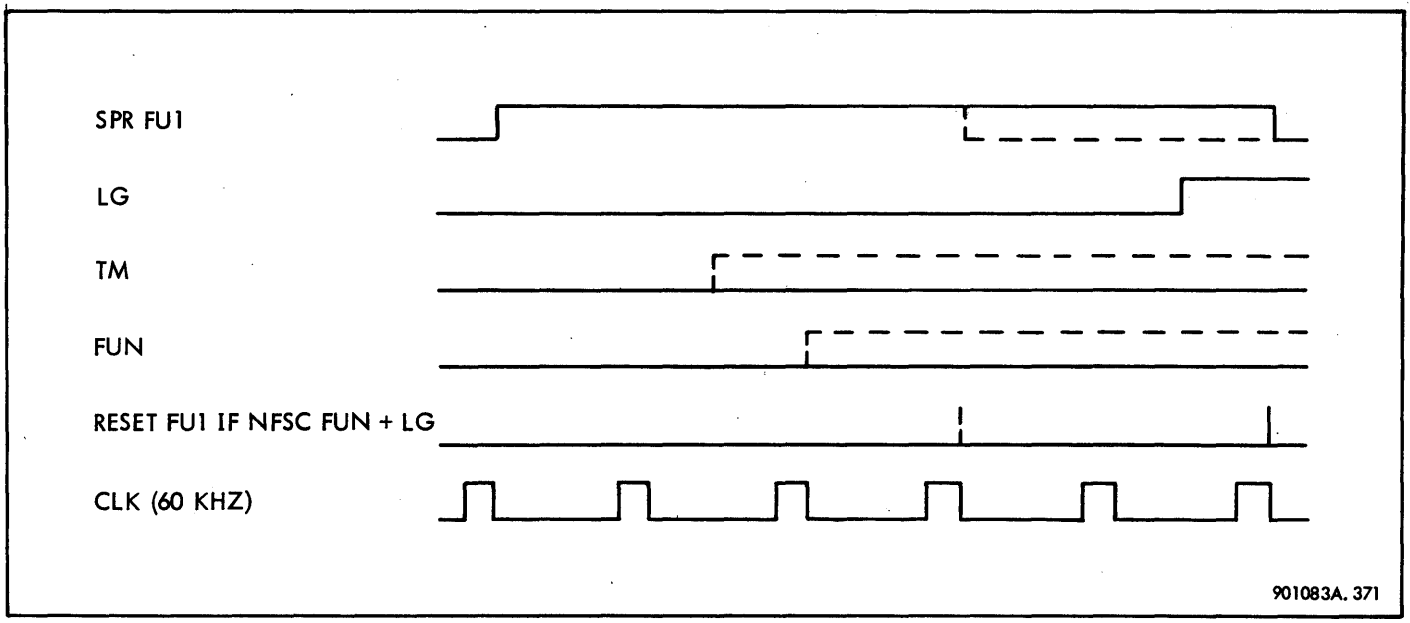

Figure 3-58. 03F03U State (Space Record), Timing Diagram

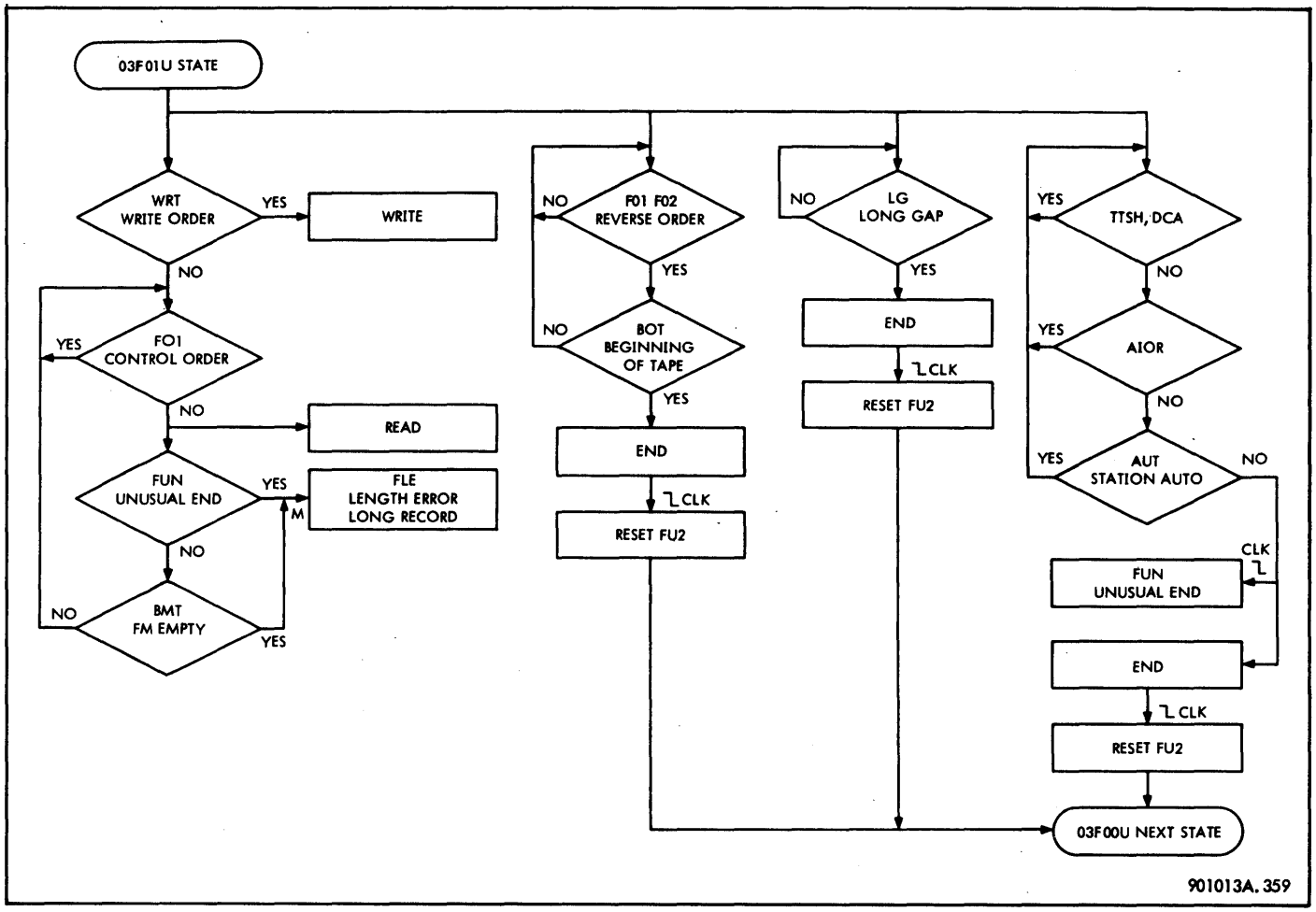

Figure 3-59. 03F01U State, Flow Diagram

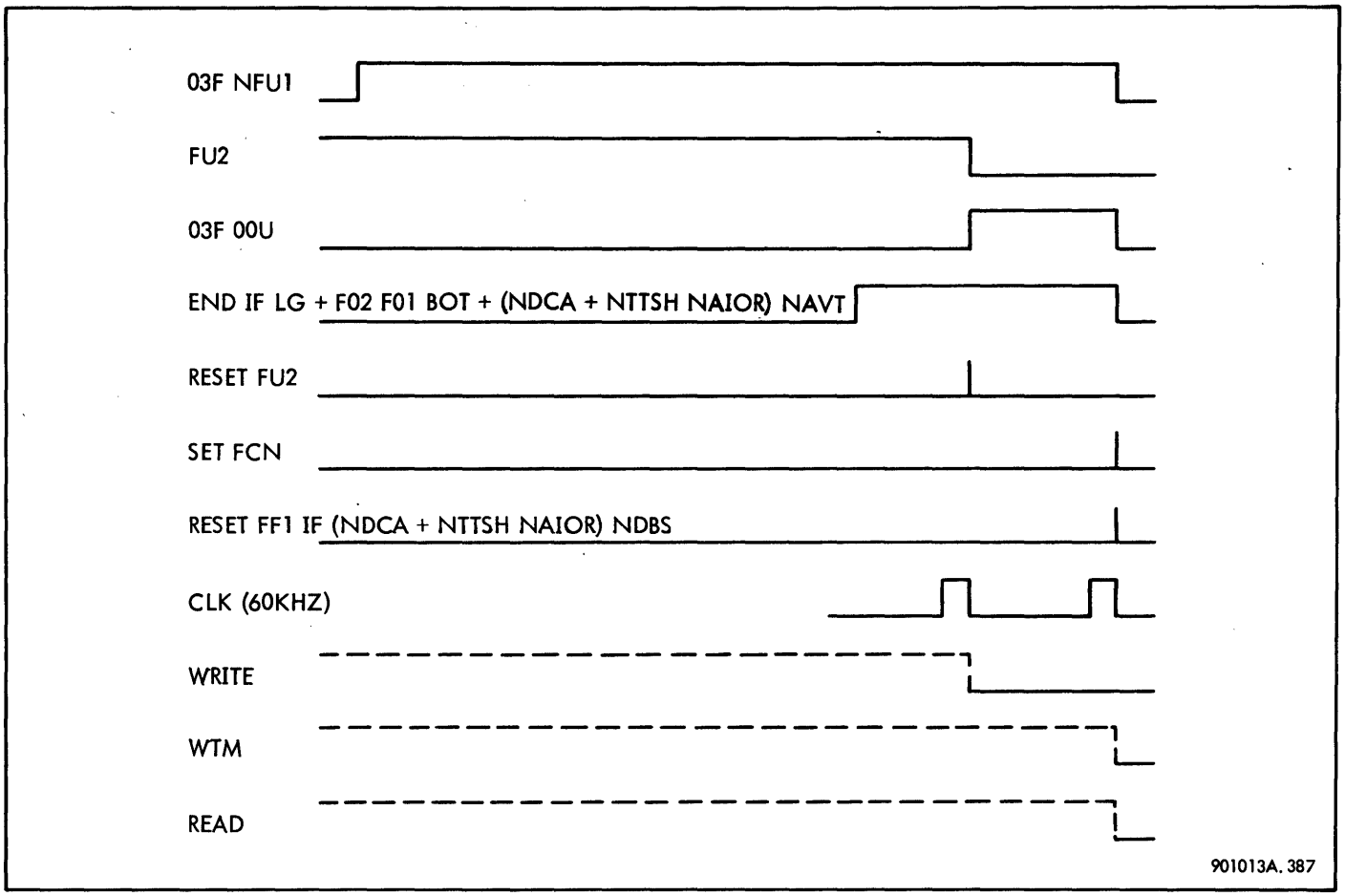

Figure 3-60. 03F01U State, Timing Diagram

UNUSUAL END (STATION NOT IN AUTO). If, when the controller advances to state 03F01U, DCA, TTSH, AIOR and AUTO are false, FUN sets and END comes true:

C/FUN = 03F BAND29 CLK + ...
BAND29 = NDCA NTTSH NAIOR NAUT
END = 03F NFU1 BAND29

When CLK comes true, it makes the clock input of FUN true, and when it goes false, it clocks and sets FUN. END is connected to the clock input of FU2:

C/FU2 = CLK END 03F

When CLK comes true, it makes the clock input of FU2 true, and when it goes false, it clocks and resets FU2,which advances the controller to state 03F00U.

3-55 03F00U, Station Finalization

The 03F00U state is the station finalization state. In this state, the read and write orders are either carried through to the next state (order input) in a command chaining operation, or the operation is terminated on an unusual end condition. See figure 3-61 for a flow diagram of the 03F00U state.

When the controller enters this state, if DCA, TTSH, AIOR, and DBS (device busy) are false and AUTO is true, the following events occur: FF1 is reset, FCN (channel end) is set, and the controller advances to the 01F00U state (order input):

C/FF1 = 03F00U NOR01 NDBS CLK
NOR01 = NDCA NTSTH NAIOR
C/FCN = CLK 03F00U + ...

When CLK comes true, it makes the clock inputs of FF1 and FCN true; when it goes false, it clocks and resets FF1 and sets FCN. The controller then advances to state 01F00U (order input).

If, however, AUTO is false, FUN (unusual end) is set:

C/FUN = BAND29 CLK 03F
BAND29 = NDCA NTTSH NAIOR NAUT

When CLK comes ture, it makes the clock input of FUN true; when it goes false, it clocks and sets FUN.

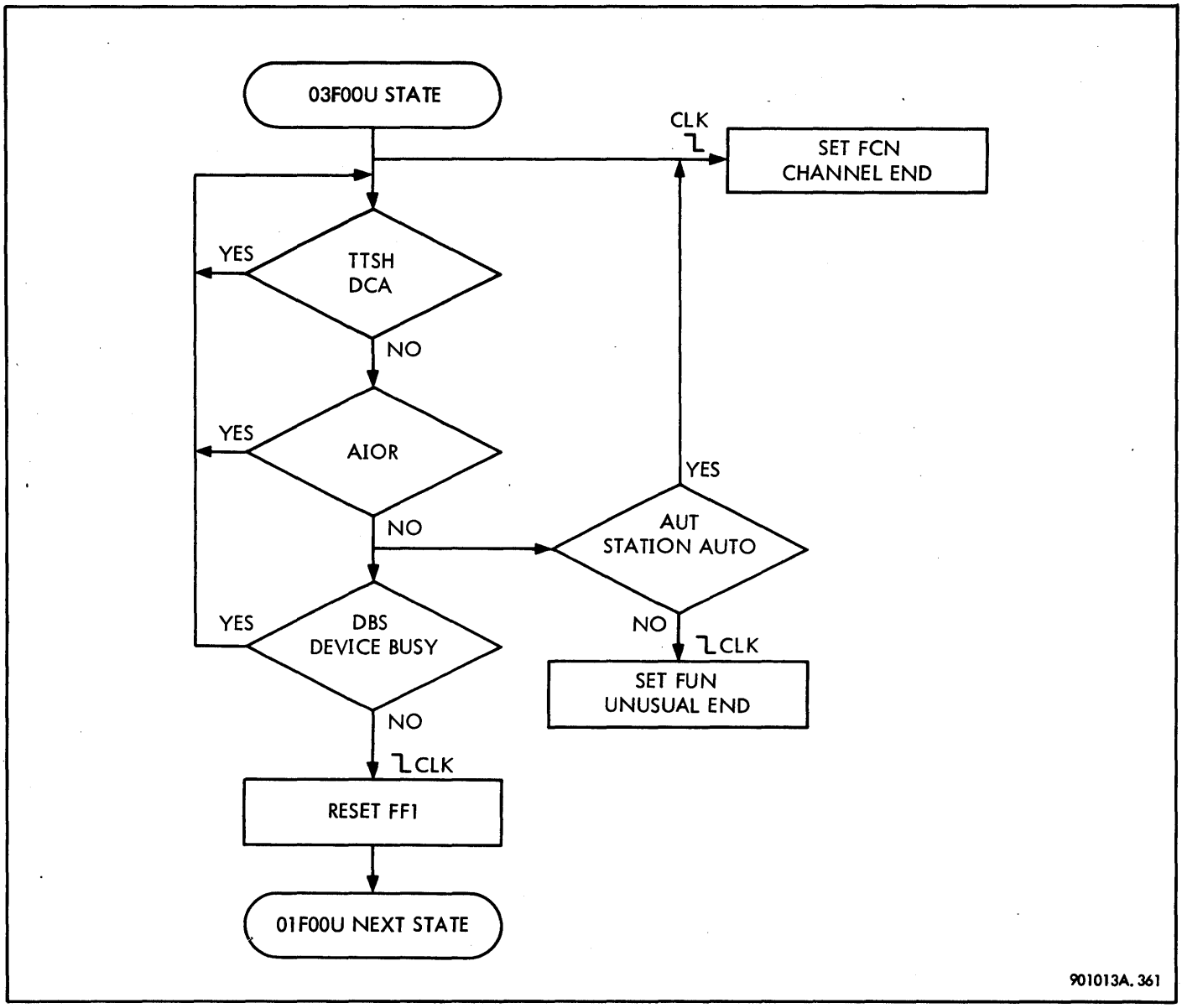

Figure 3-61. 03F00U State, Flow Diagram

3-56 01F00U, Order Input

The 01F00U state is the order input state. The controller enters this state when it must report errors, unusual end, and channel end to the IOP, or when the command chaining order must be sent to the state 01F01U. Figure 3-62 shows a flow diagram for the 01F00U state.

The IOP receives its input orders during this state on the following DA lines:

Input Order	DA Line
Unusual end	DA4
Channel end	DA3
Chaining modifier	DA2
Incorrect length	DA1
Transmission error	DA0

Figure 3-63 shows a timing diagram for the 01F00U state.

UNUSUAL END. When the controller enters this state, it generates a service call by raising CSL:

CSL = 01F00U + ...

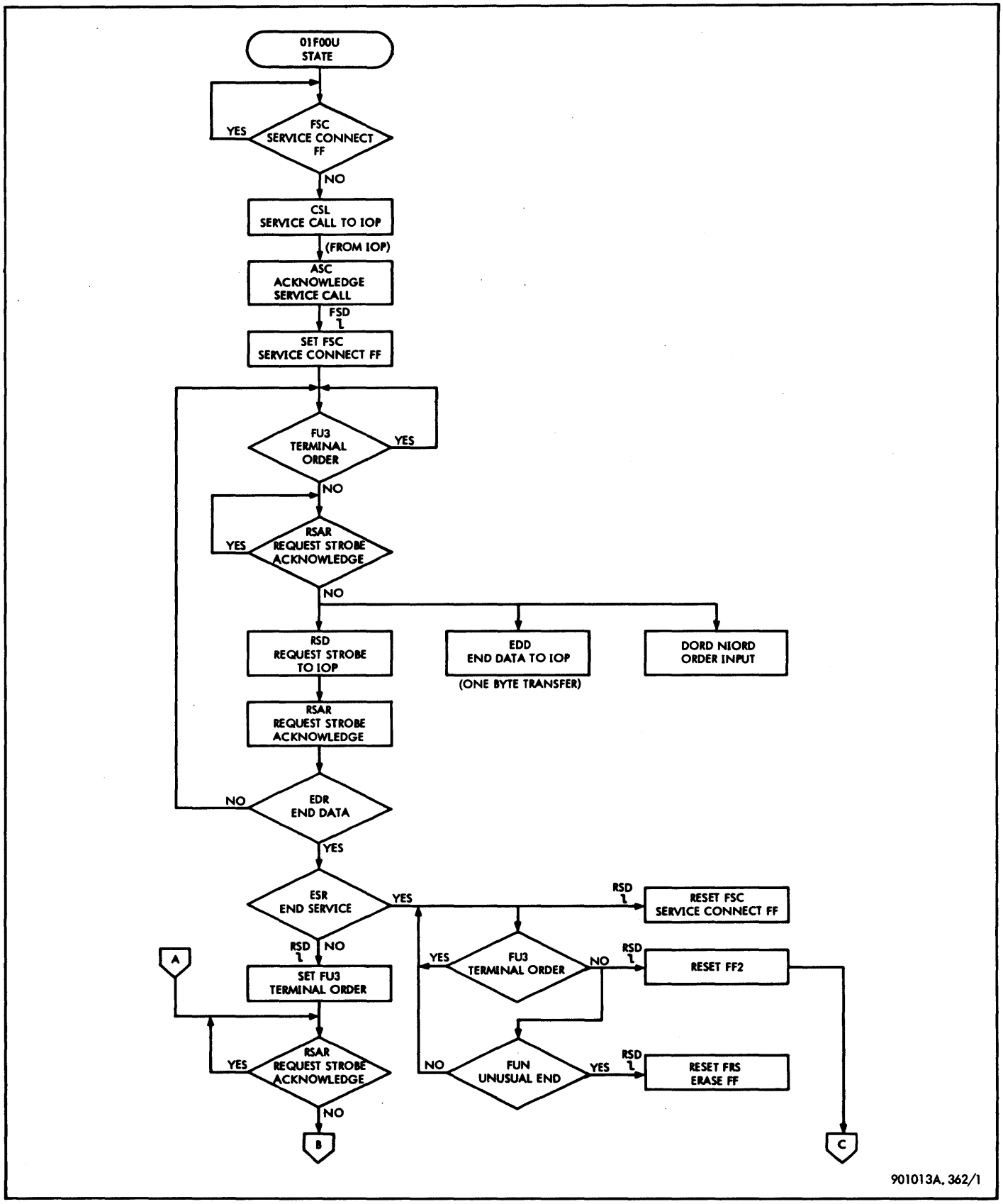

Figure 3-62. 01F00U State, Flow Diagram (Sheet 1 of 2)

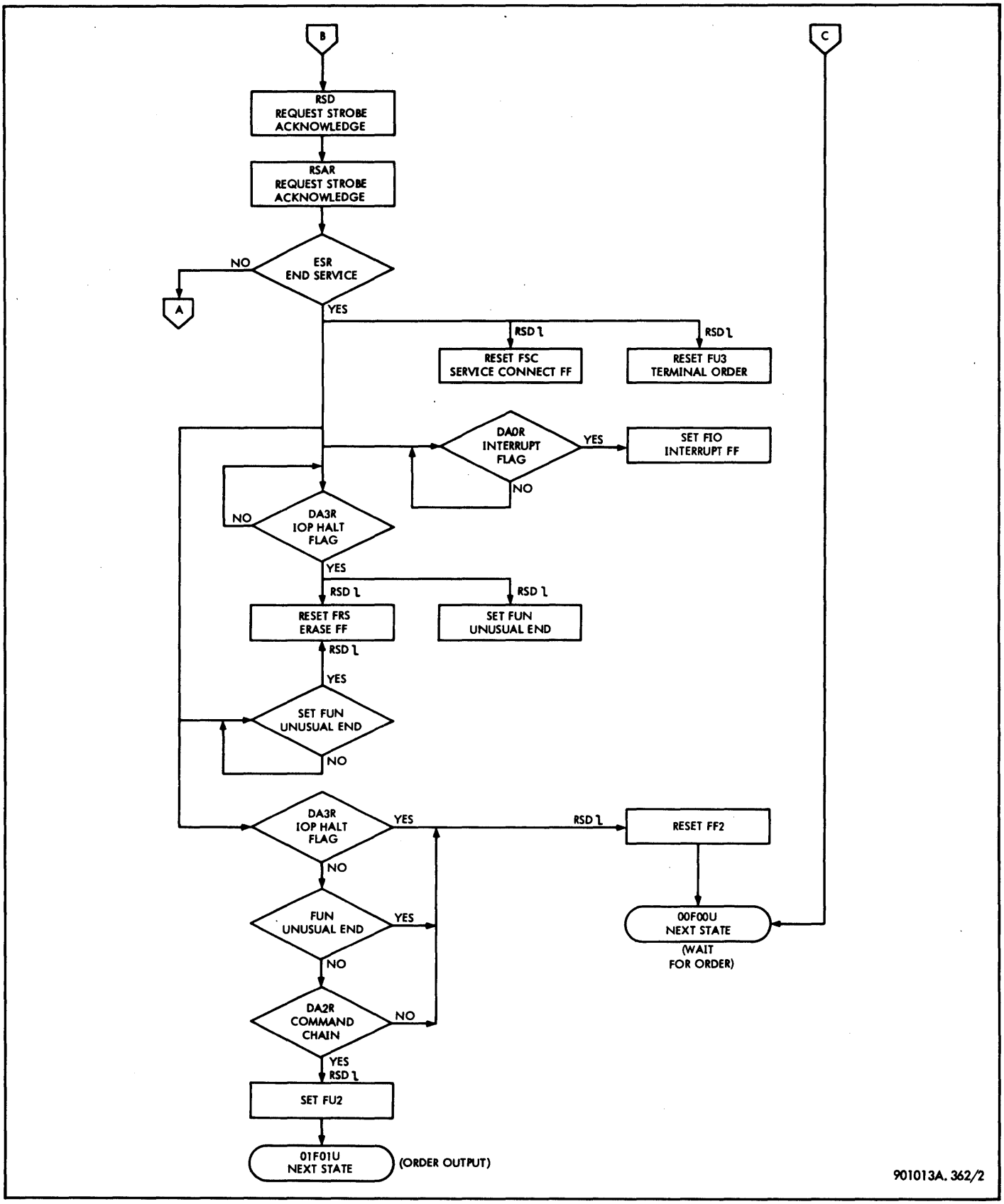

Figure 3-62. 01F00U State, Flow Diagram (Sheet 2 of 2)

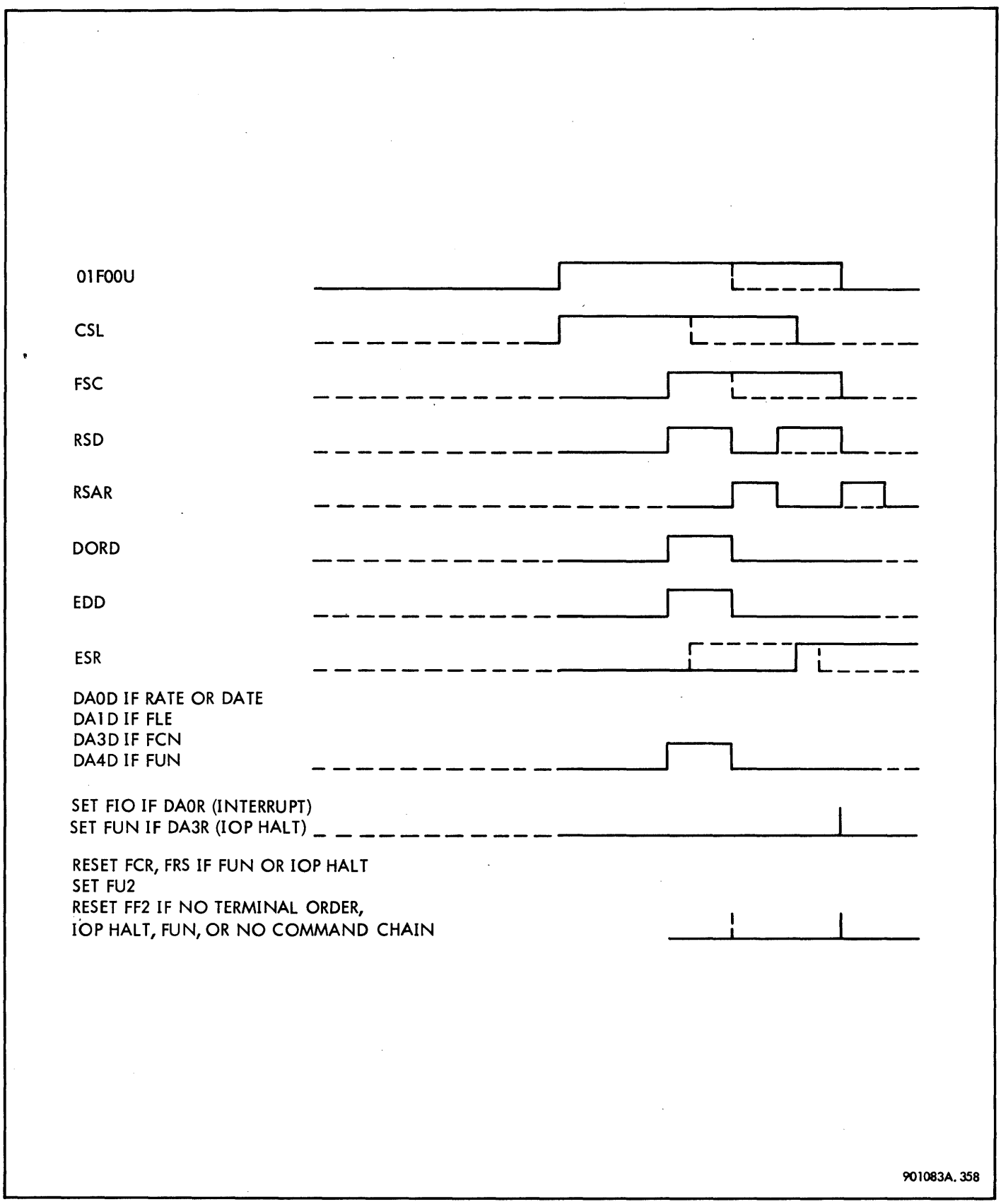

Figure 3-63. 01F00U State, Timing Diagram

The IOP acknowledges the service call request by raising ASC, FS, and AVI. The set and clock inputs of service connect flip-flop FSC are made true, and when FSR (from the IOP) goes false, FSC is clocked and sets. At the same time, RSD, DORD, EDD, and DA4 are made true.

The IOP accepts the data and raises ESR and RSA (request strobe acknowledge). RSAR (receiver output from RSA) then comes true. When RSAR comes true, RSD goes false. When RSD goes false, it clocks and resets FSC. If there is no terminal order, RSD also resets FF2, and if there is an unusual end condition, it resets FRS (erase flip-flop):

C/FRS = RSD 01F00U FRS + ...

C/FF2 = RSD 01F00U + ...

The controller now advances to state 00F00U (ready state), where it waits for the next order.

CHANNEL END AND INTERRUPT. The controller raises CSL, and the IOP acknowledges the service call request by raising ASC, FS, and AVI. FSC is clocked and set by FSR (from the IOP), and RSD, DORD, EDD, and DA3 are made true. The IOP accepts the data and raises RSA, and RSAR comes true. When RSAR comes true, RSD goes false. When RSD goes false, it clocks and sets FU3:

C/FU3 = RSD FSCC

The IOP drops RSA, and RSD comes true again. The IOP raises ESR and RSA, and RSD goes false. When RSD goes false, it clocks and resets FSC and FU3.

If DA0 (interrupt) is true, FIO is set when RSD goes false:

C/FIO = (FU3 NDST) ESR RSD1 NFIO + ...

If DA3 is true, FUN is set, and FCR, FRS, and FF2 are reset when RSD goes false.

The controller then advances to state 00F00U (ready) on a channel end or interrupt.

COMMAND CHAINING. The controller raises CSL, and the IOP acknowledges the service call request by raising ASC, FS, and AVI. FSC is clocked and set by FSR (from the IOP), and RSD, DORD, EDD, and DA2 are made true. The IOP accepts the data and raises RSA, and RSAR comes true. When RSAR comes true, RSD goes false. When RSD goes false, it clocks and sets FU3. The IOP drops RSA, and RSD comes true again. The IOP raises ESR and RSA, and RSD goes false. When RSD goes false, it clocks and resets FSC and FU3.

If IOP halt (DA3) and FUN are false and command chain (DA2) is true, FU2 sets when RSD goes false, and the controller advances to state 01F01U (order output) on a command chain order:

C/FU2 = 01F00U RSD

The controller now continues with the order that it contains (read or write) until the particular operation is completed.

3-57 MAGNETIC TAPE SYSTEM FUNCTIONS

The main functions of the magnetic tape system are to write and read data on tape. The logic circuits that perform these functions are the station data electronics and the controller data electronics. The station data electronics is comprised of the modules contained in chassis S. The controller data electronics is comprised of the modules contained in chassis V and W. The description that follows covers the write and read functions in two parts: station data electronics and controller data electronics.

3-58 STATION DATA ELECTRONICS

The station data electronics performs all the data processing required to enable the station to write and read information on tape. This data is provided by the controller as determined by the program. Figure 3-64 shows a flow diagram of the station states and different operations for read and write functions.

3-59 Writing Operation

Before the actual recording of information on tape can take place, one of the eight stations must be selected. After selection, the station is in state 0 with FCTS set and FS1S through FS3S reset. The station remains in state 0 for 16.7 μs (one clock time) and then enters the forward prerecord delay, state 6. (State 6 is referred to as the prewrite delay when a write operation is specified in the text.) The activate motor signal, ACMS, comes true and forward tape motion is initiated. Figure 3-65 shows a flow diagram of the write operation.

One of the signals received from the controller during a write operation is WRT, which is applied to a gate that produces write enable term WENS:

WENS = OSCTS WRT START CONTR

Enable OCTS is true in the selected station. Enable START CONTR is true if the station is in the on-line mode. WENS is applied along with the set and reset outputs of the write flip-flops to write drivers that connect to the write head. Prior to WENS coming true, the write flip-flops were all set. This occurs because NWENS, on the dc-set input, is true prior to the write operation or because NWLRSC inhibited the reset gates at write time. All that is required at this time to record on tape is for data to be transferred from the controller to the station on the WRXS data lines. Before the controller can begin sending data to the station, it must first receive the device proceed signal, DPRSD, from the station:

DPRSD = DPRS FCTD

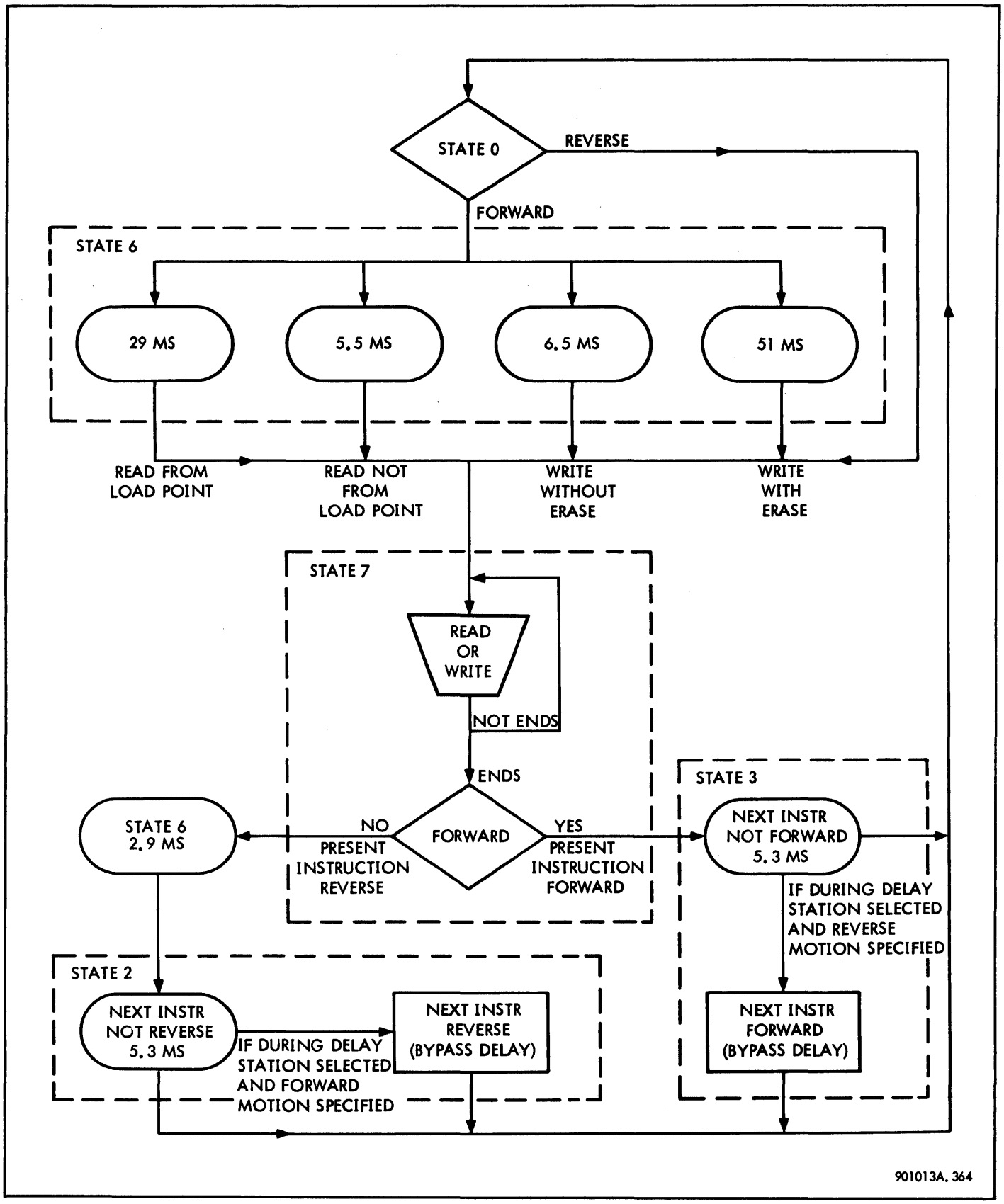

Figure 3-64. Read/Write Operation, Flow Diagram

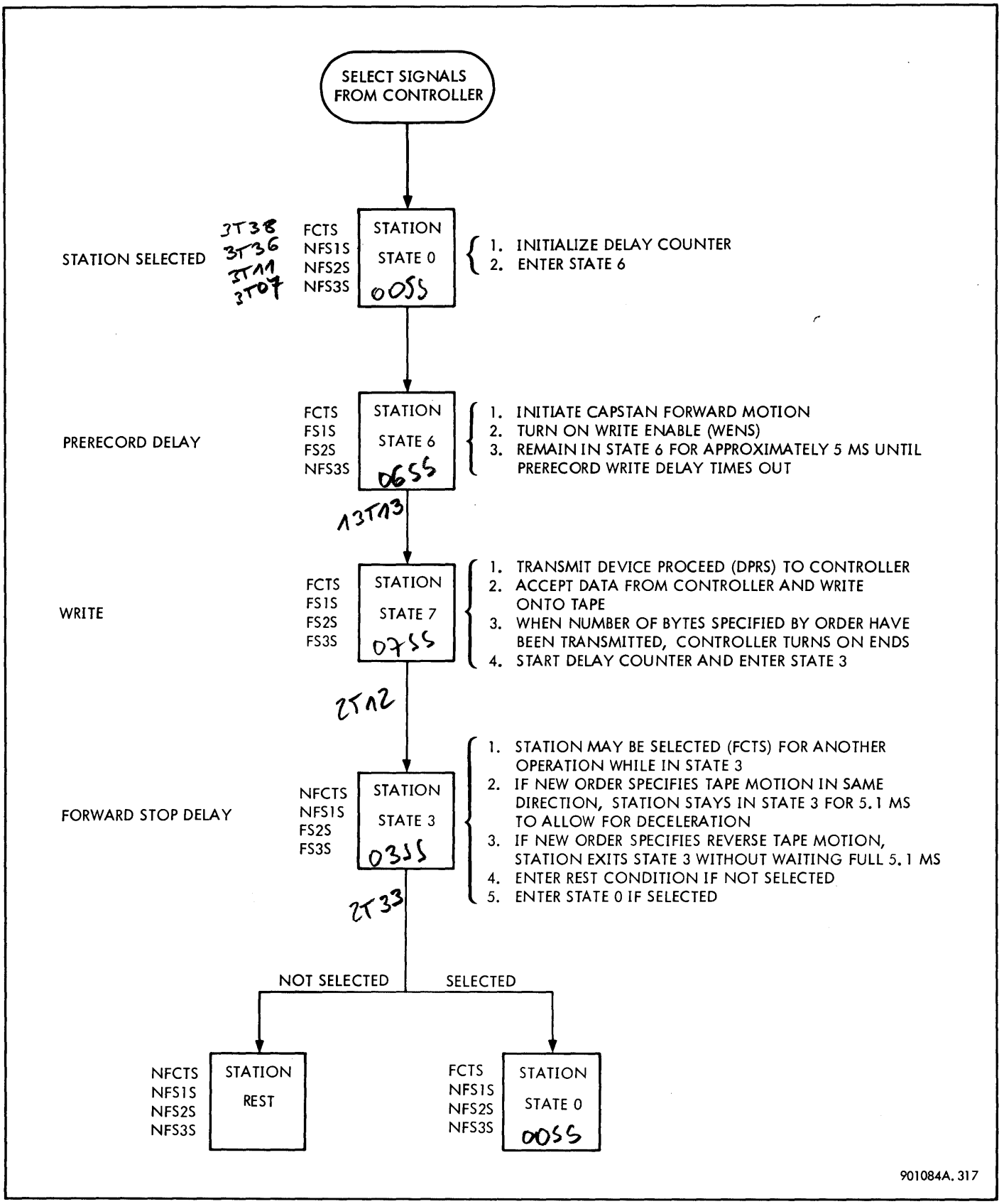

Figure 3-65. Write Operation, Flow Diagram

Enable FCTD is true because the FCT flip-flop is set in the selected station. Enable DPRS comes true if the state counter enters state 7; this causes term 07SS to come true. The state counter will not set the FS3S flip-flop and enter state 7 until after the forward prerecord delay time has elapsed:

S/FS3S	=	SFS3S FCTS
FCTS	=	True in selected station
SFS3S	=	06SS NERSS TWRS
06SS	=	True in state 6
NERSS	=	True if the erase signal is false from the controller
TWRS	=	WRTS FC05S FC09S NFC04S

Enable WRTS is true from the controller during a write operation.

START PRERECORD DELAY. For the delay counter to reach a FC05S, FC09S, NFC04S configuration it takes approximately 6.5 ms after the initiation of a write operation. Therefore, the FS3S flip-flop cannot be set, and it takes approximately 6.5 ms to exit state 6 and enter state 7 on a write operation. This delay is known as the start prerecord delay, which is necessary to ensure the attainment of proper tape speed and to have a proper gap between records.

When the FS3S flip-flop sets, the station enters state 7, term 07SS comes true, and the device proceed signal, DPRSD, goes to the controller. When the controller receives DPRSD, the data is transferred from controller to station.

CONTROLLER TO STATION WRITE DATA FLOW. Information to be written on tape is transferred by characters via cables from write register output cable drivers in the controller to cable receivers in the tape station. The outputs of these cable receivers are designated WR0S through WR7S and WRPS. The receiver inputs from the controller are designated WR0CD through WR7CD and WRPCD. The The WRxS data signals are AND-gated with the SWOAx, -Bx, and -Cx outputs of the associated write deskew switches and clocks.

WRITE DESKEW CIRCUITS. (See figure 3-66) The write deskew switches decode one of eight binary write deskew counts from the output of a counter located in the controller. These counter terms are designated WDC1CD through WDC3CD. The WDCxCD term is transferred via cables from write deskew counter cable drivers in the controller to the input of one of the line receivers in the tape station, designated WDC1S through WDC3S. The outputs of WDC1S through WDC3S are parallel input to three write deskew switches on the barred and unbarred inputs to each of the C/WDRx buffered AND gates (a total of 27 switches). These switches are positioned during the deskewing adjustment. They are set for individual channels so that one of eight binary counts is selected for input to the associated C/WDR buffered data cable receiver. The clock term on the inputs to the C/WDR buffered AND gates also originates in the controller. Its function is to strobe all the data inputs from the controller at the same time. This action suppresses the effect of any parasitic variations on the data or write skew count lines. Therefore, the output of a particular C/WDR buffered AND gate goes true at clock time if a one bit is present on the WRXS data line and the appropriate write skew count has been reached.

WRITE FLIP-FLOPS. The outputs of the C/WDR0 through C/WDR7 and C/WDRP write deskew buffered AND gates are applied to the clock input of the WDR0 through WDR7 and WDRP write driver flip-flops. These flip-flops are also referred to as write toggles. The clock input to these write toggles is true only if a one bit is to be written on tape. A clock pulse is necessary to change the state of a write flip-flop. Therefore, the write flip-flops toggle on a one bit from the controller and do not change state with a zero bit from the controller.

To set or reset the write flip-flops, the WRDE toggle enable term must be true. This term originates in the controller and is a function of the two most significant flip-flops in the write deskew counter. The toggle enable comes true during the last quandrant of the bit time while writing. The set output of each write flip-flop is connected to the reset input of the same flip-flop and the reset output is connected to the set input. Therefore, at toggle enable time (WRDE) and at the trailing edge of the clock input (a one bit to be written), any write flip-flop will set if it is in the reset state or reset if it is in the set state.

WRITE DRIVERS. The set and reset outputs of the write flip-flops are connected to separate two-term NAND gates on the input to write-drivers located on the same module as the write flip-flops. The other enable on these gates is term WENS, which came true at the start of the write operation when the station entered state 0 (0SCTS true). It should be noted that before the write operation, all the write flip-flops were set because term NWENS was true or because term NWLRCS was false.

WRITE DRIVERS TO WRITE HEAD. The outputs of the write driver NAND gates, designated WDRX, are connected through a resistor module and cable to opposite ends of one of the seven write head coils. The center tap of each write head coil is connected through a resistor module to a write current source. The +25V write current source is connected through the write enable relay.

With term WENS true, one of the two NAND gates on the inputs to the write drivers is enabled. The state of the write flip-flop, set or reset, determines which gate is enabled. The output of the enabled gate is at a ground potential. Therefore, current flows from the write current source through one side of the write head coil to ground, provided by the enabled NAND gate. As long as term WENS remains

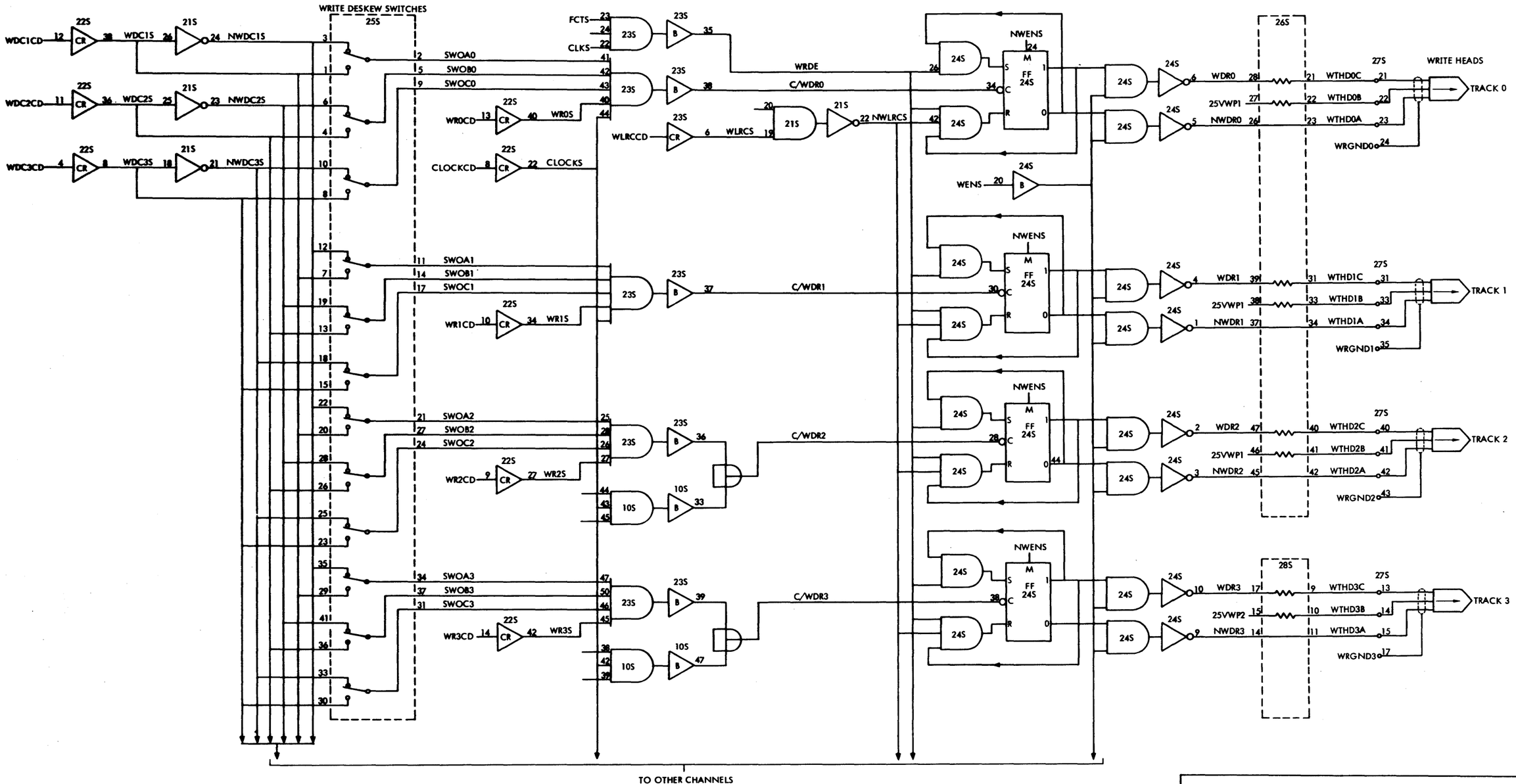

Figure 3-66. Write Deskew and Write Head Interconnect, Logic Diagram

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true and the write flip-flop does not change state, the write current continues to flow in the same direction through the associated write head coil. These conditions cause the magnetic flux for the associated track on the magnetic tape to be aligned in one direction.

WRITING ON TAPE. When a one bit is received from the controller, the state of the write flip-flop changes. This causes the write current ground to switch from one end of the write coil to the other. Therefore, a current path is provided through the opposite side of the write coil, which causes the direction of the write current to reverse. This in turn causes the flux on the magnetic tape to change direction by 180°. In the nonreturn-to-zero (NRZ) method of magnetic recording, this change in flux direction is recognized as a one bit. Thus, each one bit of data from the controller causes the write toggles to change state, which causes a one bit to be recorded on tape. The write toggles do not change state with a zero data bit from the controller (no clock). Therefore, the direction of current through the write coil does not change, causing a zero bit to be written on tape.

END OF WRITE DETECTION. In this manner, seven-bit data characters are recorded on tape. After writing the last character, the controller waits three byte times and then transmits an all-ones character to the station. This all-ones character is used in the generation of the LRC (longitudinal redundancy character).

LRC CHARACTER GENERATION. When the LRC character is to be written, the WLRC term (write longitudinal redundancy character) comes true from the controller. With WLRC true, the inverted NWLRC term goes false. This inhibits the reset side of all the write flip-flops. When the all-ones byte is received from the controller, a C/WDR clock term is produced to all the write flip-flops. The particular write flip-flop may be set or reset before writing the LRC character. The NWLRC reset inhibit and the clock produced by the all-ones byte cause all the write flip-flops that are reset to set at the time LRC is to be written. This change to the set state causes the configuration in the write flip-flops to be written on tape as the LRC character.

CONTROLLER WRITE TERMINATION. After the LRC character has been written and transferred back to the controller by the read after write operation, the controller transmits the ENDC signal to the station. When the ENDC signal is received from the controller, term ENDS comes true and is AND-gated with CLKS to clock the FCTS connected flip-flop to the reset (not connected) state. This disconnects the station from the controller, thereby terminating the write operation as far as the controller is concerned. Term ENDS is also applied to a three-term gate on the clock input to the FS1S flip-flop in the state counter:

C/FS1S = 01SS NRVSS ENDS

Upon being disconnected from the controller, the station is in state 7; therefore, 07SS is true. Enable NRVSS is true because forward motion is always specified in a write operation. Therefore, when ENDS comes true, an input is produced that clocks the FS1S flip-flop to the reset state. The FS2S and FS3S flip-flops are still set, which cause the station to enter state 3. As the station leaves state 7, capstan motor power is removed (NACMS) and the delay counter begins to count. (The delay counter was reset on entering state 7.)

FORWARD STOP DELAY. State 3 is known as the forward stop delay. Its purpose is to provide a delay for the capstan to decelerate after the forward operation is completed. In order to leave state 3 and enter state 0, or the idle state (NFCTS, NFS1S, NFS2S, NFS3S), it is necessary for the FS2S and FS3S flip-flops to be clocked to the reset state:

C/FS2S = CFS2S
CFS2S = 03SS R03SS
C/FS3S = CFS3S
CFS3S = 03SS R03SS
R03SS = TSPS
TSPS = FC08S FC07S NFC04S

The delay counter, which was initialized on entering state 3, reaches an FC07S, NFC04S configuration in approximately 5.3 ms. Enable 03SS is true in state 3. Therefore, the station remains in state 3 for 5.3 ms and then enters state 0 or idle except in the following circumstances:

a. When the FCTS connect flip-flop was reset at the time the station received the ENDS signal, which was before entering state 3. Therefore, the station can be selected by another order from the IOP while in state 3. If this new order specifies tape motion in the same direction, it is not necessary to stay in state 3 for the entire 5.3 ms because the tape can be accelerated to nominal speed without first coming to a stop. There is a clock gate on both the FS2S and FS3S flip-flops with input enables 03SS and R03SS:

R03SS = FCTS RNVRS

b. When enable FCTS comes true after the station is selected.

c. When enable NRVRS is true after the new order specifies tape motion in the forward direction. This is the direction in which the tape is already moving. Therefore, the station exits from state 3 to state 0 after a forward read as soon as it is selected if the tape motion specified by the new order is in the forward direction.

3-60 Reading Operation

Before information can be read from tape, one of the eight possible stations must be selected. The station after selection is in state 0 with FCTS set and FS1S through FS3S reset. The station remains in state 0 for 16.7 μs (one clock time) and then enters the forward prerecord delay, state 6, by FS1S and FS2S being set. Figure 3-67 shows a flow diagram for the read operation.

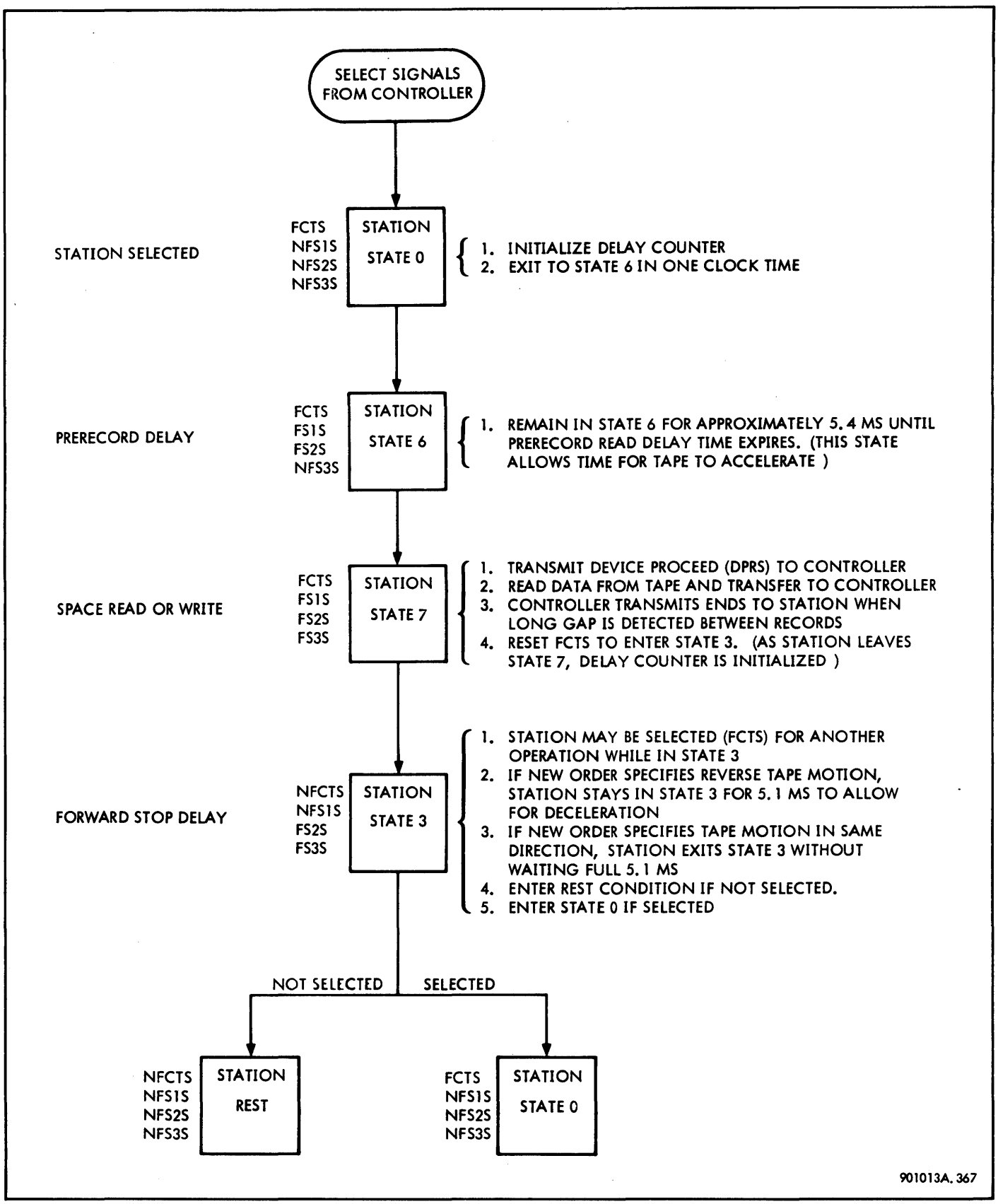


Figure 3-67. Read Operation, Flow Diagram

State 6 is referred to as the preread delay when a read operation is specified in the text. The activator motor signal, ACMS, comes true and forward tape motion is initiated. The purpose of state 6 on a forward read is to prevent noise generated during gap time from being interpreted as data in the controller. This is accomplished by delaying the generation of the device proceed signal, DPRS, to the controller for a period of 5.5 ms. This delay prevents the controller from entering the read state for 5.5 ms.

For the controller to read information, it is first necessary that it receive the device proceed signal, DPRS, from the station:

DPRSD = DPRS FCTD

Enable FCTD is true because the FCT flip-flop is set in the selected station. Enable DPRS comes true if the state counter enters state 7, causing term 07SS to come true. The FS3S flip-flop does not set to place the station in state 7 until after the forward prerecord delay time has expired:

S/FS3S = SFS3S FCTS
FCTS = True in selected station
SFS3S = 06SS TRDDS + ...
06SS = True in state 6
TRDDS = NWRTS TRDS
NWRTS = True in a read operation
TRDS = NFC04S FC09S FC06S NERSS
NERSS = True in a read operation except when the beginning of the tape marker is detected

For the delay counter to reach an FC06S, FC09S, NFC04S configuration, it takes approximately 5.5 ms after the initiation of a read operation. Therefore, the FS3S flip-flop cannot be set, and it takes 5.5 ms to exit state 6 and enter state 7 on a read operation. This delay is known as the start prerecord delay.

When the station enters state 6 on a read operation with the tape at load point, it does not exit to state 7 for 29.9 ms. This is because of the following set input to the FS3S flip-flop. It is necessary to set FS3S to enter state 7:

S/FS3S = SFS3S FCTS
FCTS = True in selected station
SFS3S = ISFS3S
ISFS3S = NWRTS (true in a read) ERSS (true because tape at BOT) 06SS (state 6) TBDS
TBDS = NFC01S FC02S FC03S

Note

The delay counter is inhibited until the tape is moved off BOT sensor.

The delay counter which began counting when the station entered state 6 does not reach an NFC01S, FC02S, and FC03S configuration for 29.9 ms. Therefore, the FS3S flip-flop is not set, and the station does not exit state 6 until 29.9 ms have elapsed. During this 29.9 ms period, reading is prevented for approximately 2.1 inches after the BOT marker, where noise and bad tape may exist.

When the FS3S flip-flop sets, the station enters state 7 (FS1S, FS2S and FS3S), term 07SS comes true, thereby enabling the device proceed signal, DPRSD, to the controller. When the controller receives DPRSD, it enters a state where it can receive data from the station and transmit data to the IOP.

The preread delay is always less than the write delay. The station, therefore, leaves state 6 before reading the first byte of a record on tape. This ensures that the controller has received DPRSD and is ready to receive data before the read head sensing the first byte of a record on tape. At this time, tape has attained a speed of 75 ips and the controller is in a state in which it may receive data.

READ DATA FLOW. (See figure 3-68) As the magnetic tape passes over the read head, signals are induced in the coils of the read head. These signals are designated RDHD0-5 (A, B, and C) for read heads 0 through 5 and RDHDP (A, B, and C) for read head parity. The letters A, B, and C pertain to the two ends and center tap of an individual read head coil. The RDHD0-5 and RDHDP signals are transferred through a cable and cable connecting module joining the read head coil to one of the associated read amplifiers, designated RD AMP 0S through RD AMP 5S and RD AMP PS.

Read Amplifiers. The read amplifier responds only to signals that exceed the threshold voltage level. Each read amplifier has a threshold adjustment that determines the minimum amplitude necessary for signal recognition.

The 20 to 30 μV read signals from the read head are amplified, rectified, and then clipped in the read amplifiers. The resultant signal at the test point in the read amplifier is approximately 1.6V for an all ones pattern on tape and 1.9V for a single one bit.

Read Amplifiers to Controller. The RD AMP 0S through RD AMP 5S and RD AMP PS outputs of the read amplifiers are applied as inputs to two-term input AND gates on buffered cable driver circuits designated RD AMP 0 SD through RD AMP 5 SD and RD AMP P SD, respectively. The other enabling term on these gates is common enable term FCTS.

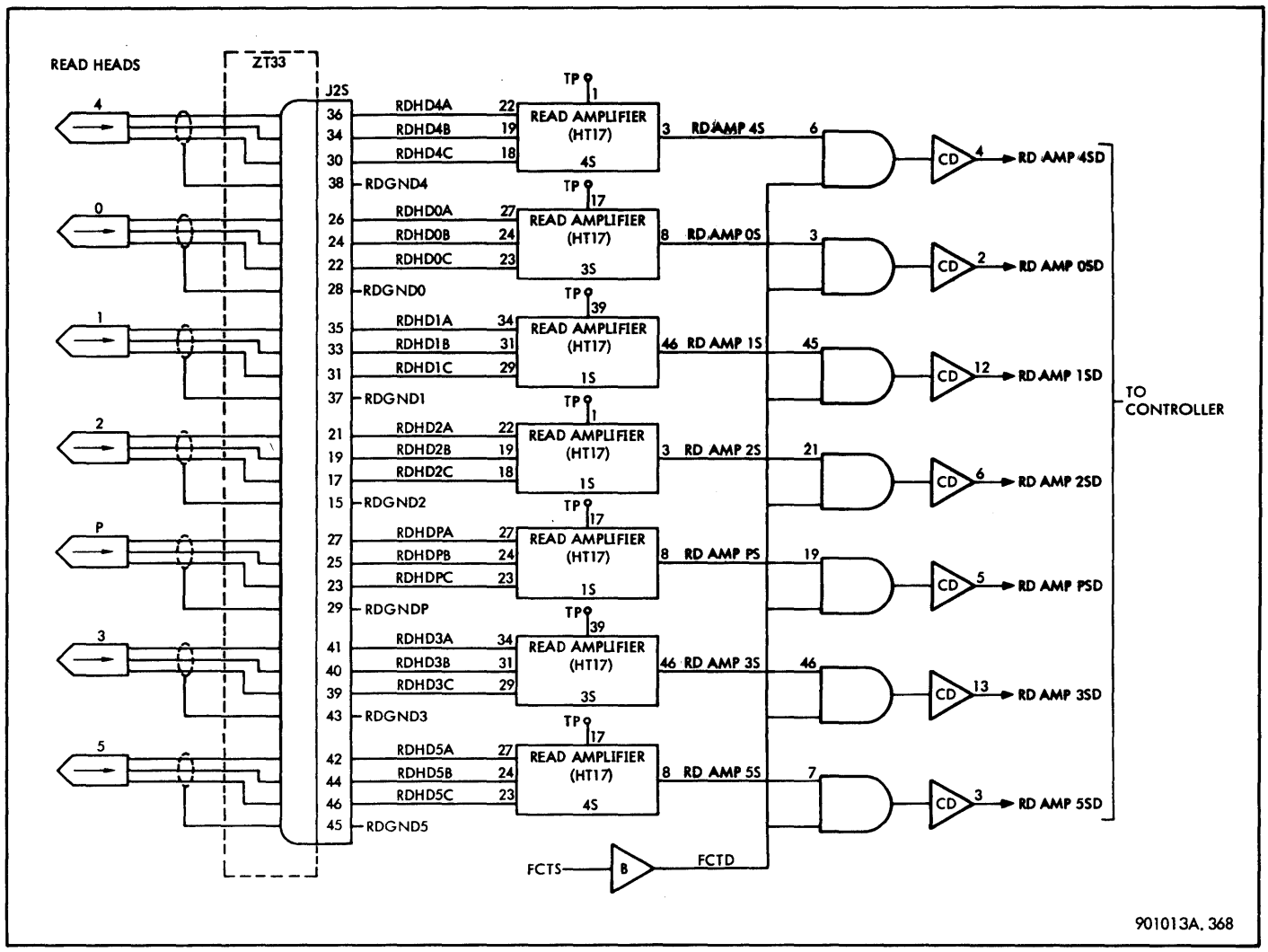


Figure 3-68. Read Head Interconnect, Logic Diagram

The outputs of these AND gates are input to the driver portion of the particular RD AMP X SD buffered cable driver. The outputs of the buffered cable drivers feed cables that transfer data from the tape station to the associated peak detect counter in the magnetic tape controller. There are seven peak counters, one for each of the cable driver outputs.

END OF READ DETECTION. For tape deceleration to be initiated, the ENDC signal must come true from the controller. It would not be desirable for ENDC to be transmitted to the station as soon as the read termination signals are received by the controller from the IOP because the read/write head may be positioned somewhere between the start and end of a record of information on tape. Therefore, the ENDC signal is not transmitted from the controller until the controller detects a long gap on tape. When the ENDC signal is received from the controller, term ENDS comes true and is AND-gated with CLKS to clock the FCTS connect flip-flop to the reset (not connected) state. This disconnects the station from the controller, thereby terminating the forward read operation as far as the controller is concerned.

Term ENDS is also applied to a gate on the clock input to the FSIS flip-flop in the state counter:

C/FSIS = 07SS NRVSS ENDS

The station is in state 7, so 07SS is true. Enable NRVSS is true because forward motion is specified. Therefore, ENDS produces an input to clock FSIS to the reset state. This makes ACMS go false, removing capstan motor power. The FS2S and FS3S flip-flops are still set, which causes the station to enter state 3. As the station leaves state 7, the delay counter is initialized.

FORWARD STOP DELAY. State 3 is known as the forward stop delay. Its purpose is to provide a delay for the capstan to decelerate after the read operation is completed.

In order to leave state 3 and enter state 0 or the idle state (NFCTS, NFS1S, NFS2S, NFS3S), it is necessary for the FS2S and FS3S flip-flops to be clocked to the reset state:

C/FS2S = CFS2S
CFS2S = 03SS R03SS
C/FS3S = CFS3S
CFS3S = 03SS R03SS
R03SS = TSPS
TSPS = FC06S NFC04S

The delay counter, which started counting, on entering state 3 reaches an FC06S, NFC04S configuration in approximately 5.3 ms. Enable 03SS is true in state 3. Therefore, the station remains in state 3 for 5.3 ms and then enters state 0 or idle, except in the following circumstance.

EXIT FROM STATE 3 BEFORE 5.3 MS. The FCTS connect flip-flop was reset at the time the station received the ENDS signal before entering state 3. Therefore, the station can be selected by another order, from the IOP, while in state 3. If this new order specifies tape motion in the same direction, it is not necessary to stay in state 3 for the entire 5.3 ms because the tape can be accelerated to nominal speed without first coming to a stop. There is a clock gate on both the FS2S and FS3S flip-flops with input enables 03SS and R03SS:

R03SS = FCTS NRVRS

Enable FCTS comes true when the station is selected. Enable NRVRS is true if the new order specifies tape motion in the forward direction. This is the direction in which the tape is already moving. Therefore, the station exits from state 3 to state 0 after a forward read as soon as it is selected if the tape motion specified by the new order is in the forward direction.

REVERSE POSTRECORD DELAY. The 2.9 ms delay in state 6 is provided to allow the last bit read to move close to the write head before any tape deceleration takes place. As soon as the FS1S flip-flop is reset, the station exits state 6 and enters state 2. The ACMS signal goes false, removing motor power. State 2 is known as the reverse stop delay. The purpose of state 2 is to provide a delay for the capstan to decelerate after the reverse read operation is completed. To leave state 2, the FS2S flip-flop must be clocked to the reset state:

C/FS2S = CFS2S
CFS2S = 02SS TSPS TRVS
TSPS = FC06S NFC04S
TRVS = FC05S FC08S FC07S

Enable 02SS is true in state 2. The binary combination of the TSPS and TRVS delays equals 5.3 ms. Therefore, the station remains in state 2 for 5.3 ms. It then enters state 0 if the station has been selected, or the idle state except in the following circumstance.

The FCTS connect flip-flop was reset at the time the station received the ENDS signal, which was before entering state 6. However, the station can be selected by another order from the IOP while in state 2. If this new order specifies tape motion in the same (reverse) direction, it is not necessary to stay in state 2 for the entire 5.3 ms period because the tape can be accelerated to nominal speed without coming to a complete stop. There is a clock gate on the FS2S flip-flop with input enables 02SS, FCTS and RVRS:

C/FS2S = CFS2S
CFS2S = 02SS FCTS RVRS

The FCTS enable is true if the station is selected. The 02SS enable is true in state 2. The RVRS enable is true if reverse motion is specified. Therefore, the station exits from state 2 in one clock time if it is selected, and the tape motion specified by the new order is in the reverse direction.

3-61 CONTROLLER DATA ELECTRONICS

The seven-track controller data chassis is available in two configurations: one with and one without the packing option. The model 7371 controller contains the controller chassis (Y and Z) and the data chassis (V and W). The packing option (model 7374) consists of four modules and an interchassis cable which interconnects the Y, Z, and W chassis. The model 7371 is always wired for the packing option. However, only if the model 7374 modules are inserted will the packing function be effected.

3-62 General Description

A description of the controller data logic follows. A block diagram of the controller is shown in figure 3-69.

Previous to any operation, a reset signal is sent by the controller to initialize all registers and counters. In write operations, bytes are requested from the IOP and stored in the eight-byte memory, to be transferred to the buffer register as directed by the data logic. The buffer register provides the intermediate storage interval during which the byte to be recorded is modified as required by the mode logic.

During the write interval, the character to be recorded is transferred from the buffer register via the write cable to the write drivers in the selected station, and is then recorded on tape. The accuracy of the written material is checked by the read logic, which monitors the read amplifiers, deskews the data output, and checks for lateral parity, longitudinal parity, and skew errors.

During read operations, the data appearing at the read amplifier is deskewed and assembled at the assembly register.

At the end of the skew interval, the character is checked for parity, transferred to the longitudinal check register and is transferred to the buffer register. In the buffer register, the character is modified according to the mode of operation (BCD, binary or packed) and transferred to the memory for subsequent transfer to the IOP.

Error checking is done in the longitudinal check register for longitudinal parity errors, and in the assembly register for lateral parity errors.

3-63 Mode Control

In conjunction with the write and read signals, the controller must transmit information to define the mode of operation of the data electronics. The controller flip-flops FO2 and FO3 determine the mode as follows:

FO2	FO3	Mode
0	0	Pack
0	1	Binary
1	0	Pack
1	1	BCD

The pack mode signal is formed in the packing option logic:

DPAK = NFO3 OPER

OPER = WNTME + READ

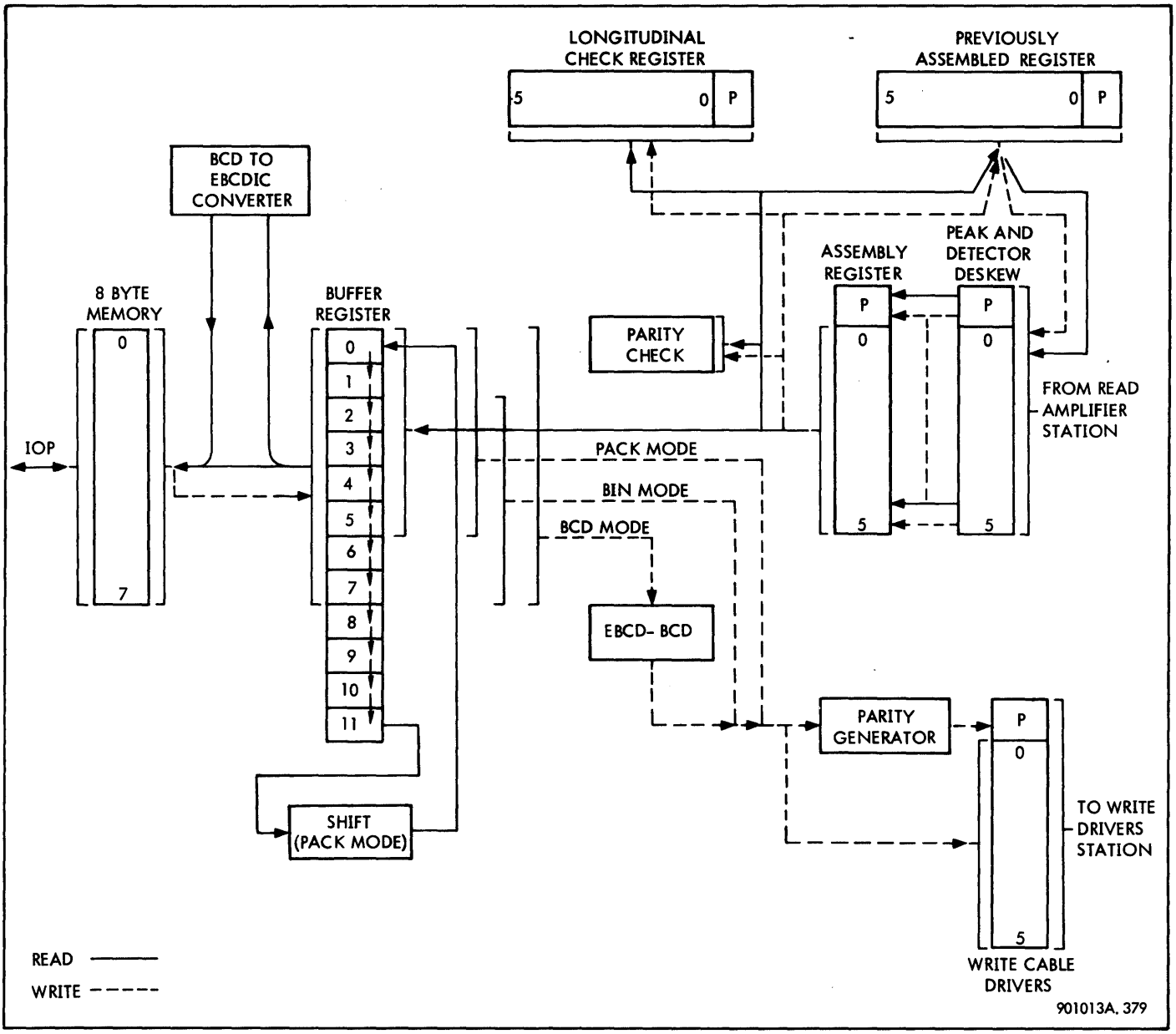


Figure 3-69. Controller, Block Diagram

The binary and BCD modes are formed from the pack signal:

DBIN = NDPAK NFO2 OPER

DBCD = NDPAK FO2 OPER

In the event that the program calls for the pack mode and the packing option is not installed, the binary mode is selected automatically. This occurs because the term NDPAK is formed within the packing option logic, and if the option is not installed, NDPAK remains true.

3-64 Memory Access

An eight-byte memory provides intermediate buffering between the IOP and the data electronics. Access to memory, from either the station electronics or the controller, is controlled by a priority flip-flop, MSTA, and a memory clock cycle control, MCLK.

STATION ACCESS. The station access request signal, MARS, is driven by either WMAR, the write memory access request, or RCHP, the read access request. Assuming that the controller is not making a request, MARS sets MSTA true. MCLK is also set, which starts the memory clock cycle:

MARS = WMAR MCCA + RCHP NRCPA NMFUL

During write operations, MARS in inhibited if there are no bytes in memory. During read operations, MARS is inhibited if memory is full:

M/MSTA = MARS NMARC NDLAC

M/MCLK = MARS NDLAC + MARC NDLAC

S/MCLK = NMCLK

C/MCLK = DLDP

MCLK drives a series of 50 ns delay lines which provide the memory timing:

DLA2 = MCLK delayed by 50 ns

DLA1 = DLA2 delayed by 50 ns

DLA2 = DLA3 delayed by 50 ns
+ MARC MCON DLA1
+ MARS MSTA DLA1

DLAC = DLA1

DLAP = MCLK NDLA1

DLBP = DLAP delayed by 50 ns

DLCP = DLBP delayed by 50 ns

DLDP = DLCP delayed by 50 ns

DLA1 is held true until the request currently being processed is removed; this provides a time lapse for the memory cycle to prevent timing conflicts.

The address of the memory location is controlled by the mode signals: memory to controller, MMTC; memory to buffer register, MMTB; controller to memory, MCTM; or buffer register to memory, MBTM:

MMTB = MSTA WRITE

MBTM = MSTA READ

MCTM = MCON WRITE

MMTC = MCON READ

The memory address comes from either the write memory register, when loading bytes into memory from the buffer register or the controller data lines, or from the read memory register, when loading either the buffer register or the controller data lines.

The read and write address registers are each three-bit binary counters that are incremented each time a read or write memory access cycle is completed:

MAD0 = + MW03 (MBTM + MCTM)
+ MR03 (MMTB + MMTC)

MAD1 = + MW02 (MBTM + MCTM)
+ MR02 (MMTB + MMTC)

MAD2 = + MW01 (MBTM + MCTM)
+ MR01 (MMTB + MMTC)

S/MR03 = NMR03

C/MR03 = MRCL

S/MR02 = NMR02

C/MR02 = MR03

S/MR01 = NMR01

C/MR01 = MR02

MRCL = DLA1 (MMTB + MMTC)

S/MW03 = NMW03

C/MW03 = MWCL

S/MW02 = NMW02

C/MW02 = MW03

S/MW01 = NMW01

C/MW01 = MW02

MWCL = DLA1 (MBTM + MCTM)

When the time interval DLDP is true, the data is written into the memory if the cycle is a write cycle. If it is a read cycle, the memory outputs are loaded into the buffer register:

WRITE MEMORY = DLDP (MBTM + MCTM)

LOAD BUFFER REGISTER = XMEM

XMEM = WRITE MMTB DLDP NWLCC

DLDP resets WMAR, if the cycle is a write access request during write operations, or sets RCPA, if the cycle is a read access request during read operations:

C/WMAR = + MMTB DLDP + ... (Reset clock)
S/RCPA = NRCPA
C/RCPA = + NRCPA DLDP MBTM + ...

Either WMAR being reset or RCPA being set allows MARS to go false, after which DLA1 and DLAC are dropped:

DLA1 = MARS MSTA DLA1 + ...
DLAC = DLA1

DLA1 goes false and resets MSTA, which enables the controller to access memory:

R/MSTA = MSTA
C/MSTA = MSTA DLA1

The fall of DLA1 also increments the address registers:

MRCL = DLA1 (...)
MWCL = DLA1 (...)

After DLA1 goes false, NDLAC goes true to allow a new access cycle to begin. NDLAC provides a time lapse in the priority cycle to permit completion of the previous cycle.

CONTROLLER ACCESS. The controller access request signal, MARC, is driven by the service request signal from the controller:

MARC = SRIP NSRPD
SRPD = + WRITE MFUL + READ MC01 NBMTC

The SRIP delay signal, SRPD, is normally used only in operations involving a selector IOP. During write operations, SRIP is delayed if the memory has eight bytes in it; during read, SRIP is delayed until there is more than one character in the memory. Once MARC is allowed to go true, the access process is identical with that of a station access.

At the time of DLCP, the acknowledge signal is sent to the controller. During read operations, the signal is RDOL, read data on-line. During write operations, the signal is SRPA, SRIP acknowledge:

RDOL = + DLCP MCON
+ SRIP RDOL
SRPA = NRDOL

The fall of SRPA indicates to the controller that the memory has taken the data. RDOL is held true until the controller acknowledges the data by releasing SRIP.

A four-stage counter is used to monitor the number of bytes in the memory and to signal the controller or station when service is required to load or unload the memory. The counter MCCA, -B, -C, -D is a modified binary counter operating as follows:

Stage (MCCX)				
A	B	C	D	Bytes in Memory
0	0	0	0	None
1	0	0	0	1
1	0	0	1	2
1	0	1	0	3
1	0	1	1	4
1	1	0	0	5
1	1	0	1	6
1	1	1	0	7
1	1	1	1	8

The counter is incremented by MWCL each time a byte is loaded into the memory from either the controller or the station. The counter is decremented by MRCL each time a byte is read from the memory:

S/MCCA = NMCCA
C/MCCA = + NMCCA MWCL
+ MCCA MC01 MRCL
S/MCCB = NMCCB MCCC
C/MCCB = + MCCC MCCD MWCL
+ NMCCC NMCCD MRCL
S/MCC = NMCCC
C/MCCC = + MCCD MWCL
+ NMCCD NMC01 MRCL
S/MCCD = NMCCD
C/MCCD = + MCCA MWCL
+ NMC01 MRCL

MC01 = MCCA NMCCB NMCCC NMCCD

If a write operation is in progress and the memory contains less than five bytes, a service request signal is sent to the controller. If a read operation is in progress and the memory contains more than four bytes, a service request is sent to the controller:

BMTC = + WRITE NMCCB
+ READ MCCB
+ ...

Figure 3-70 shows a timing diagram for the memory access operation.

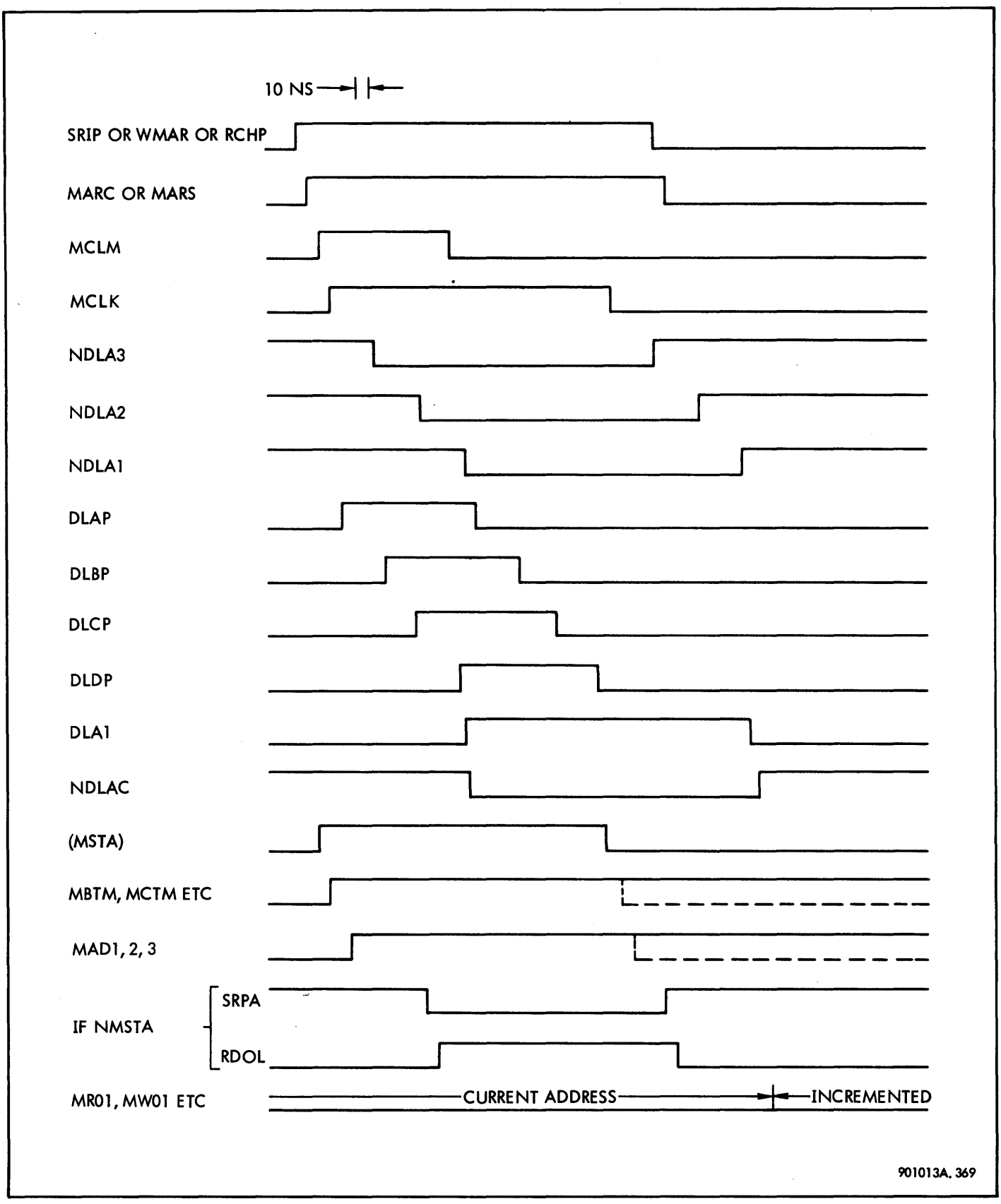


Figure 3-70. Memory Access (Controller and Station), Timing Diagram.

3-65 Clock Signal

The master clock signal is derived from a 3.84 mc crystal oscillator. The frequency is chosen so that the character interval at 800 bpi may be divided evenly into 32 parts. With this method, one clock cycle equals 39.0625 μin. of tape.

Since the controller is capable of operating with any one of three different speed transports, 150 ips, 75 ips, or 37.5 ips, the clock signal is available in three frequencies, produced by a counter: 3.84 mc, 1.92 mc, and 0.96 mc. These frequencies are for the 150 ips, 75 ips, or 37.5 ips transports, respectively. These frequencies are chosen so that 32 clock cycles are equal to the specified distance between characters at 800 bpi. Thus, in every case, one clock cycle is equal to 39.0625 μin. of tape.

The clock equations are these:

F384 = 3.84 mc oscillator output

S/F192 = NF192 1.92 mc

R/F192 = F192

C/F192 = F384

S/F096 = NF096 0.96 mc

R/F096 = F096

C/F096 = F192

CLOK = + V150 F384
+ V075 F192
+ V037 F096

3-66 Write Operations

WRITE DESKEW COUNTER. The write deskew counter is an eight-stage binary counter with a variable reset state. The counter provides the timing for the write logic, the write deskew comparators in the station, and the clock signal for the controller and station.

The counter is always running, the least significant stage, WDC7, being clocked by the CLOK signal. The seven least significant stages, WDC1 through WDC7, are used to provide the write timing signals.

The most significant stage, WDC8, is used in deriving the controller clock signal, CLKS.

The variable reset feature enables the counter to provide the correct timing intervals for the three recording densities. As can be seen from the table below, the state from which the counter is reset is always 177. The initial state is 000 when recording at 200 bpi, is 122 at 556 bpi, and is 140 at 800 bpi.

Position 1	2	3	4	5	6	7	Description
1	1	1	1	1	1	1	Last count
0	0	1	0	0	1	0	No station selected
0	0	0	0	0	0	0	200 bpi initial state
1	0	1	0	0	1	0	556 bpi initial state
1	1	0	0	0	0	0	800 bpi initial state
1	1	1	1	0	0	0	Write deskew interval
1	1	1	1	1	1	1	Reset state

The WDC counter reset terms are controlled by the density switch setting of the station selected. If no station is selected, the WDC counter resets on a combination of 200 bpi and 556 bpi settings. Since each clock period is equivalent to 39.1 microinches of tape, the period of the WDC counter is as follows:

Nominal Density (bpi)	Actual Density (bpi)	Clock Cycles	Distance
200	200	128	5000 μin.
556	556.5	46	1796 μin.
800	800	32	1250 μin.

The eighth stage, WDC8, toggles each time the WDC counter resets during operations at 556 bpi, and remains set at 200 or 800 bpi.

The state of WDC8 is used to determine the station and controller clock frequency, CLKS:

CLKS = + WDC8 WDC4 WDC3
+ NWDC8 WDC4 NWDC3

The interval WDC3 WDC4 has a period of 32 clock cycles. During 200 bpi operations, there are 128 clock cycles each WDC period; therefore, there are exactly four intervals of CLKS per period. At 800 bpi there are 32 clock cycles each WDC period, resulting in one CLKS interval per period.

At 556 bpi, the WDC period is 46 clock cycles. By using WDC8 to alternately select the normal or complement side of WDC3, the effective period of CLKS is 30.6 clock cycles.

With no station selected, the period of the WDC is 110 clock cycles, and hence the period of CLKS averages 27.5 clock cycles.

The density settings and the respective frequencies of CLKS are given below:

Density	CLKS Period (Clock Cycles)	CLKS Frequency
200	32	60 kHz
556	30.6	62.6 kHz
800	32	60 kHz
No station selected	27.5	51.5 kHz

These are the WDC equations:

S/WDC7 = NWDC7
C/WDC7 = CLOK

S/WDC6 = NWDC6 + DEN5 WDFL
C/WDC6 = CLOK WDC7

S/WDC5 = NWDC5
C/WDC5 = CLOK WDC7 WDC6

S/WDC4 = NWDC4
C/WDC4 = CLOK WDC7 WDC6 WDC5

S/WDC3 = NWDC3 + DEN5 WDFL
C/WDC3 = CLOK WDC4 WDHF

S/WDC2 = NWDC2 + DEN8 WDFL
C/WDC2 = CLOK WDC4 WEC3 WDHF

S/WDC1 = NWDC1 + NDEN2 WDFL
C/WDC1 = CLOK WDC4 WDC3 WDC2 WDHF

S/WDC8 = NWDC8 + NDEN5
C/WDC8 = CLOK WDFL

WDC COUNT OUTPUT TERMS:

WDMR = WDC1 WDC2 NWDC3 NWDC4 NWDC5 WDC6 WDC7
(Count 143) .

WDFL = WDC1 WDC2 WDC3 WDC4 WDC5 WDC6 WDC7
(Count 177)

WDWI = WDC1 WDC2 WDC3 WDC4
(Count 17X)

WDHF = WDC5 WDC6 WDC7 (Count XX7)

WD16 = WDC1 WDC2 WDC3 NWDC4 NWDC5 WDC6 WDC7
(Count 163)

WD14 = WDC1 WDC2 NWDC3 NWDC4
(Count 14X)

WRITE START. A write operation begins when the controller sets the write, not tape mark signal true, which indicates that the start gap has been generated and writing may commence. The data electronics responds by setting the write signal true:

WRIT = WNTME

The controller is then signaled that the memory has less than five bytes:

BMTC = WRIT NMCCB + ...

The memory signal remains true until five bytes are stored in memory, at which time MCCB goes true to remove BMTC.

With the loading of the first byte into memory, MCCA is set. MCCA indicates that at least one byte is in memory. One clock time after MCCA is set, WENA, the write enable flip-flop is set:

S/WENA = NFINC NWLCC WRIT MCCA + ...
C/WENA = CLOK

When WDMR (write deskew counter count 143) is true, a memory access request is made and WENB is set:

S/WMAR = NWMAR
C/WMAR = + WDMR WENA NPCH2 WNTME (MCCA + NFINC) + ...

S/WENB = NWENB WRIT
C/WENB = WDMR WENA

The signal WENB enables the data transfer to the write amplifiers and enables the pack mode counters if the pack mode is in operation.

The write process is now started and continues until the last character is written on tape.

Figure 3-71 shows a timing diagram for the write start operation.

WRITE PROCESS. Data may be recorded on tape in any of three modes: binary, BCD, or pack mode. In the binary mode, the two high order bits of the eight-bit byte from the IOP are discarded and the remaining six are recorded on tape. Parity of the character is created by a parity generator which monitors the six bits and provides a seventh bit to produce odd character parity.

In the BCD mode, the byte is assumed to be coded in the EBCDIC code and is translated into the equivalent BCD code for recording on tape. The seventh bit is again generated by a parity generator to produce even character parity.

The pack mode is used when it is desired to record all of the information sent from the IOP without conversion and without discarding any bits. This mode causes four six-bit characters to be recorded on tape for each three eight-bit bytes received from the IOP. Parity is generated and recorded on tape as odd character parity.

Write Binary or BCD. Binary and BCD recording operate in the same manner as far as the buffer register is concerned.

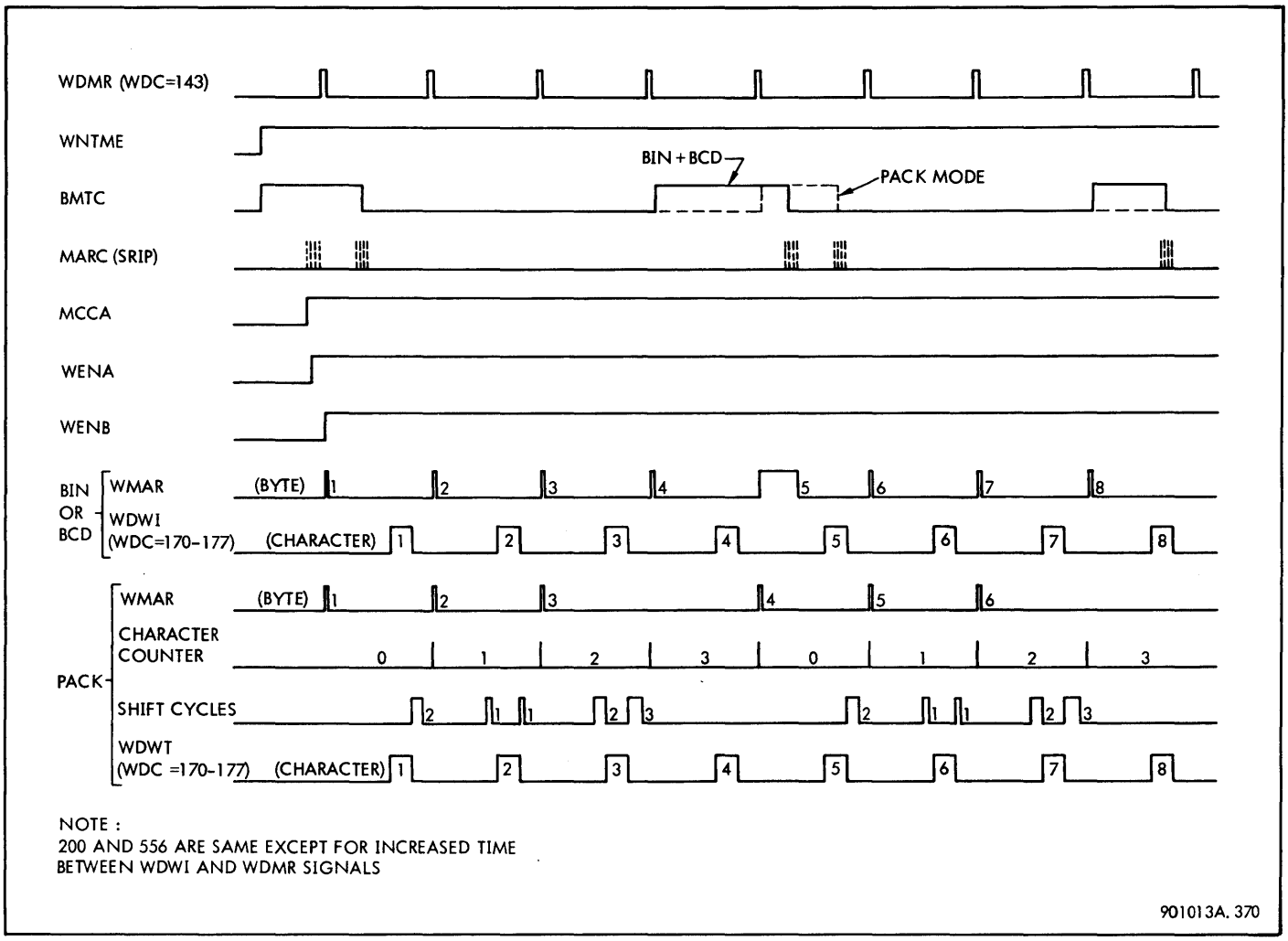


Figure 3-71. Write Start (800 bpi), Timing Diagram

The only difference is in the code presented to the write transfer logic. In the process of writing, the arrival of WDMR (WDC count of 143), clears the buffer register and sets WMAR if there are bytes in memory or the controller has not finished:

E/BR00-07 = WDMR WENA NPCH2 + ...

S/WMAR = NWMAR

C/WMAR = WDMR WENA NPCH2 WNTME (MCCA + NFINC) + ...

The character counter is enabled only during pack mode. During binary and BCD modes, PCH0 is true and PCH1, -2, and -3 are false.

When the station acquires control of the memory request signal, the access cycle begins and DLDP transfers the contents of the memory location to the buffer register:

M/BR00 = XMEM FM00

M/BR01 = XMEM FM01

⋮

M/BR07 = XMEM FM07

XMEM = WRITE DLDP MMTB NWLCC

The buffer register parity generator produces an output which represents the parity of the six low order bits, BR02 through BR07:

PODD = True if BR02-BR07 are odd

PEVN = True if BR02-BR07 are even

If the binary mode is in operation, WBIN transfers the buffer register to the write drivers, discarding the two high order buffer register bits:

WCD0 = WBIN BR02 + ...

WCD1 = WBIN BR03 + ...

WCD5 = WBIN BR07 + ...

WCDP = WBIN PEVN + ...

WBIN = WENB DBIN

If the BCD mode is in operation, WBCD transfers the BCDIC equivalent of the code in BR00 through BR07 to the write drivers:

WCD0 = WBCD (NBR02 NEBLN + EDSH) + ...

WCD1 = WBCD (NBR03 NEDSH + EAMP) + ...

WCD2 = WBCE (BR04 + EZER) + ...

WCD3 = WBCD (BR05) + ...

WCD4 = WBCD (BR06 + EZER) + ...

WCD5 = WBCD (BR07) + ...

WCDP = WBCD (PODD + EBLN) + ...

WBCD = WENB DBCD

EDSH = EBCDIC dash code

= BR02 NBR03 NBR04 NBR05 NBR06 NBR07

EAMP = EBCDIC ampersand code

= NBR02 BR03 NBR04 NBR05 NBR06 NBR07

EZER = EBCDIC zero code

= BR02 BR03 NBR04 NBR05 NBR06 NBR07

The write drivers provide the inputs to the write deskew logic in conjunction with WDWI and WDC5, WDC6, and WDC7.

WDWI is true during the WDC counts of 170 through 177. In this interval, the outputs of the three lowest stages of the WDC counter, WDC5, WDC6, and WDC7, are compared with the write deskew switches. When coincidence occurs, each write toggle flip-flop is triggered if a one is to be written in its respective channel and a one is recorded on tape.

The write toggle flip-flops, WDRn, are set by the station write enable signal, initially in the false state:

M/WDRn = NWENS

S/WDRn = NWDRn WRDE

R/WDRn = WDRn WRDE NWLRCS

C/WDRn = CLOCKS WRnS
(SWnA WDC7 + NSWnA NWDC7)
(SWnB WDC6 + NSWnA NWDC6)
(SWnC WDC5 + NSWnA NWDC5)

WENS = (Station write enable signal)

WRDE = WDWI (FCTS)

WLRCS = WLCC

WRnS = WCDn

n = 0, 1, 2, 3, 4, 5, P

The write toggle flip-flop outputs combined with the write enable signal drive the write head amplifiers:

WTHDn = WDRn WENS

NWTHDn = NWDRn WENS

The write longitudinal check character signal, WLCC, disables the reset input to the write toggle flip-flops during the write finish cycle so that the LCC character inputs cause all flip-flops to be set, thus recording the LCC character.

Write Pack Mode. Pack mode writing takes place differently than in the binary or BCD mode. The buffer register undergoes shifting sequences in order to present all of the data to the write drivers for recording on the tape. The write operation begins when WENB is set by WDMR WENA. The same term sets the memory access request:

S/WENB = NWENB WRITE

C/WENB = WDMR WENA

S/WMAR = NWMAR

C/WMAR = WDMR WENA NPCH2
(MCCA + NFINC) + ...

The character counter remains at PCH0 as WENB is set after WDMR passes.

The first byte is loaded into the buffer register by DLDP and WMAR is reset. The parity generator produces an output corresponding to the bit configuration of BR00 through BR05.

ZBAP = True, if BR00 through BR05 are odd

= False, if BR00 through BR05 are even

During WDWI time, the outputs of BR00 through BR05 are sent to the write drivers. Bits 1, 2, 3, 4, 5, and 6 of a three byte group are recorded on tape in the same manner as for nonpack mode:

WCD0 = WPAK BR00

WCD1 = WPAK BR01

WCD5 = WPAK BR05

WCDP = WPAK NZBAP

WPAK = WENB DPAK

When WDFL is true (WDC time 177), the shift counter is set in order to shift BR06 and BR07 to positions BR10 and BR11.

This requires a shift count of 2, as each bit position receives the input from the second stage removed:

S/SHF1 = WDFL WENB PCH0 + ...

S/BR02 = BR00

S/BR03 = BR01

⋮

S/BR11 = BR09

S/BR00 = BR10

S/BR01 = BR11

C/BR00-11 = CLOK (SHF1 + SHF2)

The next two clock cycles cause the buffer register to precess. At WDMR time (WDC count 143), the second memory access request is made, stages BR00 through BR07 are cleared, and the character counter is advanced to state 1:

E/BR00-07 = WDMR WENA NPCH2 + ...

C/CHR1 CHR2 = WENB DPAK WDMR + ...

At WD16 (WDC count 163), the buffer register is set to precess two places, to put the seventh and eighth bits of the first byte, held in BR10 and BR11, into BR00 and BR01:

S/SHF2 = WD16 WENB PCH1 + ...

During WDWI time, BR00 through BR05 are transferred to the write drivers, and bits 7, 8, 9, 10, 11, and 12 of the three byte group are recorded on tape.

At WDFL, the buffer register is set to precess two places, to place bits 13, 14, 15, and 16 into BR08, BR09, BR10, and BR11, respectively:

S/SHF2 = WDFL WENB PCH1 + ...

At WDMR, the third memory access request is made, BR00 through BR07 are cleared, and the character counter is advanced to state 2.

At WD16, the buffer register is set to precess four places, to place bits 13, 14, 15, 16, 17, and 18 into BR00 through BR05:

S/SHF2 = WD16 WENB PCH2

During WDWI time, BR00 through BR05 are sent to the write drivers, and bits 13, 14, 15, 16, 17, and 18 are recorded on tape.

At WDFL, the buffer register is set to precess six places, to place bits 19, 20, 21, 22, 23, and 24 into BR00 through BR05:

S/SHF1 = WDFL WENB PCH2

S/SHF2 = WDFL WENB PCH2

At WDMR, the character counter is advanced to state 3; however, a memory access request is not made and the buffer register is not cleared:

C/WMAR = WENA WDMR NPCH2 (MCCA + NFINC)

C/BR00-07 = WENA WDMR NPCH2

During WDWI time, bits 19, 20, 21, 22, 23, and 24 of the three byte group are transferred to the write drivers.

At WDMR, the first byte of the next group of three is requested, BR00 through BR07 are cleared, and the character counter is advanced to state 0.

This completes a cycle of the write pack operation. All cycles follow an identical sequence until the end sequence starts, which is indicated by WDMR occurring when FINC is set and MCCA is false. Figure 3-72 shows a timing diagram for the BCD and pack writing modes. Table 3-8 gives the status and contents of the buffer register during the write pack mode.

WRITE FINISH. The write process is terminated in a different manner for each mode of operation, pack or nonpack.

Write Binary or BCD. In the nonpack (BIN or BCD) mode, the flip-flop FINC is set when the last byte has been loaded into the memory by the controller:

S/FINC = RWFIN

C/FINC = FICL

The data electronics continues the process of requesting bytes from the memory until MC01 is true, which signifies that only one byte is in memory. When the request for memory access occurs and MC01 is true, the write finish flip-flop, WFIN, is set.

MC01 = MCCA NMCCB NMCCC NMCCD

S/WFIN = NWFIN FINC MC01 DPAK + ...

C/WFIN = WENA WDMR

R/WFIN = WFIN

When the last byte is taken from memory, MCCA is reset. The next time WDMR is true, WFIN is reset, WLCC (the write longitudinal check character flip-flop) is set, and WENB is reset:

S/WLCC = WFIN NWLCC

C/WLCC = WDMR

R/WENB = WFIN

C/WENB = WDMR WENA

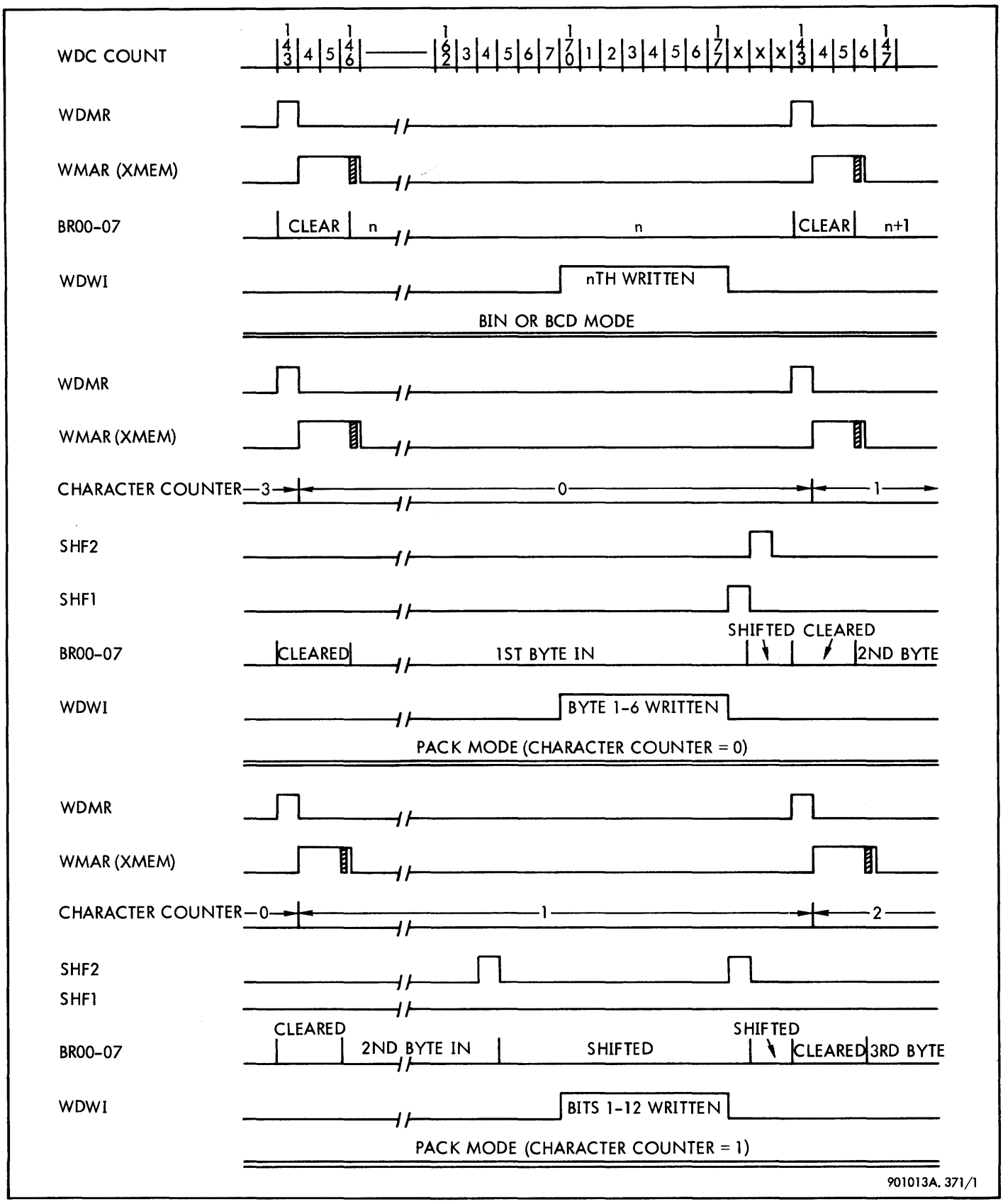
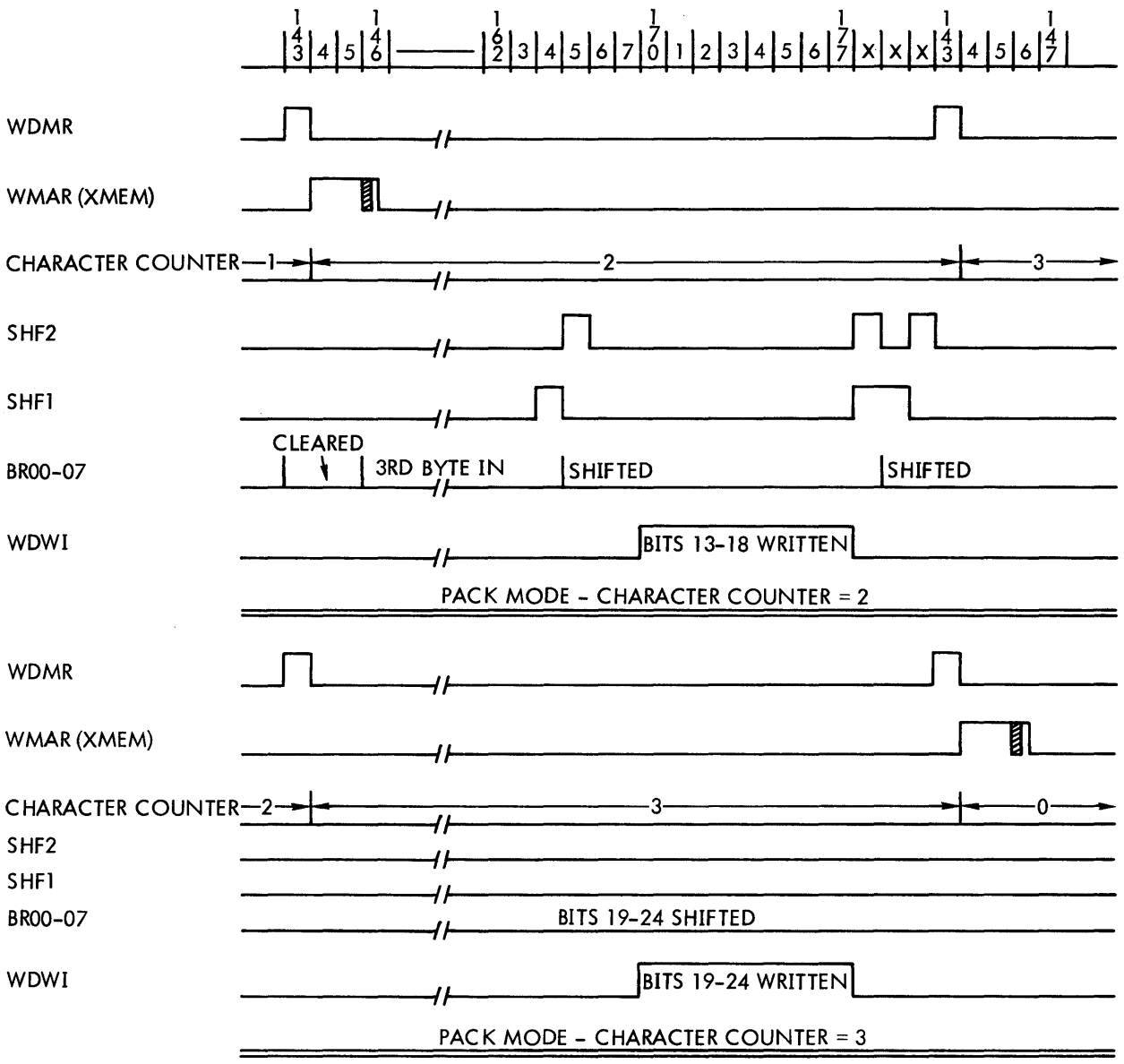


Figure 3-72. Write Operation (800 bpi), Timing Diagram (Sheet 1 of 2)



NOTE : 200 AND 556 bpi ARE SAME EXCEPT THAT CLOCK TIMES 'X'
REPRESENT WDC COUNTING BETWEEN 177_8 AND 143_8

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Figure 3-72. Write Operation (800 bpi), Timing Diagram (Sheet 2 of 2)

Table 3-8. Buffer Register Status During Write Pack Mode

WDC CLOCK TIME	CLOCK SIGNAL NAME	CHARACTER COUNTER STATE	BUFFER REGISTER CONTENTS*												REMARKS
			0	1	2	3	4	5	6	7	8	9	10	11	
143	WDMR	3									X	X	X	X	BR00-07 were erased by WDMR. WMAR will be set
163	WD16	0	1	2	3	4	5	6	7	8	X	X	X	X	First byte loaded into BR00-07 by XMEM
177	WDFL	0	1	2	3	4	5	6	7	8	X	X	X	X	Bits 1-6 sent to write drivers by WDW1. Two shifts will now be done
142		0	X	X	X	X	1	2	3	4	5	6	7	8	Two shift cycles done
143	WDMR	0									5	6	7	8	BR00-07 were erased by WDMR. WMAR will be set
163	WD16	1	9	10	11	12	13	14	15	16	5	6	7	8	Second byte loaded into BR00-07 by XMEM. One shift cycle will be done
177	WDFL	1	7	8	9	10	11	12	13	14	15	16	5	6	One shift was done. Bits 7-12 sent to write drivers. One shift will be done
142		1	5	6	7	8	9	10	11	12	13	14	15	16	One shift done
143	WDMR	1									13	14	15	16	BR00-07 were erased by WDMR. WMAR will be set
163	WD16	2	17	18	19	20	21	22	23	24	13	14	15	16	Third byte loaded into BR00-07 by XMEM. Two shift cycles will be done
177	WDFL	2	13	14	15	16	17	18	19	20	21	22	23	24	Two shifts were done. Bits 13-18 sent to the write drivers. Three shifts will be done
142		2	19	20	21	22	23	24	13	14	15	16	17	18	Three shifts done
143	WDMR	2	19	20	21	22	23	24	13	14	15	16	17	18	No action occurs. WMAR is not set
163	WD16	3	19	20	21	22	23	24	13	14	15	16	17	18	No action occurs
177	WDFL	3	19	20	21	22	23	24	13	14	15	16	17	18	Bits 19-25 sent to the write drivers
142		3	19	20	21	22	23	24	13	14	15	16	17	18	No action occurs
143	WDMR	3									15	16	17	18	BR00-07 were erased by WDMR. WMAR will be set
163	WD16	0	1	2	3	4	5	6	7	8	15	16	17	18	First byte of next group of three is loaded in
177	WDFL	0	1	2	3	4	5	6	7	8	15	16	17	18	Bits 1-6 of next group are sent to write driver. Two shifts will be done

*Contents given are those at clock time

Three clock cycles later, at time 147, the memory character counter is set to indicate three bytes in memory, WENA is reset, and the buffer register is cleared:

E/BR00-BR07 = WLCC WENA WD14 WDHF

M/MCCA = M/MCCC

M/MCCC = WLCC WENA WD14 WDHF

R/WENA = WLCC WENA WD14 WDHF

C/WENA = CLOK

Data requests are now made to the memory each time WDMR is true until MCCA is reset. Since WLCC is set, however, data is not loaded into the buffer register and it remains clear:

C/WMAR = WDMR WLCC MCCA + ...

XMEM = WRIT NWLCC MMTB DLDP

The longitudinal check gap is now generated as WENB is reset, which prevents data from reaching the write toggle flip-flops. The LCC gap is generated for three character times.

When the last dummy byte has been removed from the memory, MCCA goes false. When the write deskew counter reaches time 163, the buffer register is loaded with all ones. During the write interval, WDWI, the write toggle flip-flops are enabled by WPAK, and the reset inputs of the flip-flops are held false by WLCC. The longitudinal check character is then recorded by returning all flip-flops to their original state:

M/BR00-BR07 = WRIT NMCCA WLCC WD16

WPAK = WLCC NMCCA + ...

WLCC is then reset to complete the write cycle:

R/WLCC = NMCCA

C/WLCC = WDMR

Figure 3-73 shows a timing diagram for the write finish operation in the BIN and BCD modes.

Write Pack Mode. In the pack mode, the IOP normally transmits a multiple of three bytes, which results in a multiple of four characters on tape. It is also possible that the byte count from the IOP is either 3n + 1 or 3n + 2 bytes, in which case the record has 4n + 2 or 4n + 3 characters, respectively. The end sequence for all three conditions is the same; only the composition of the last character on tape is different.

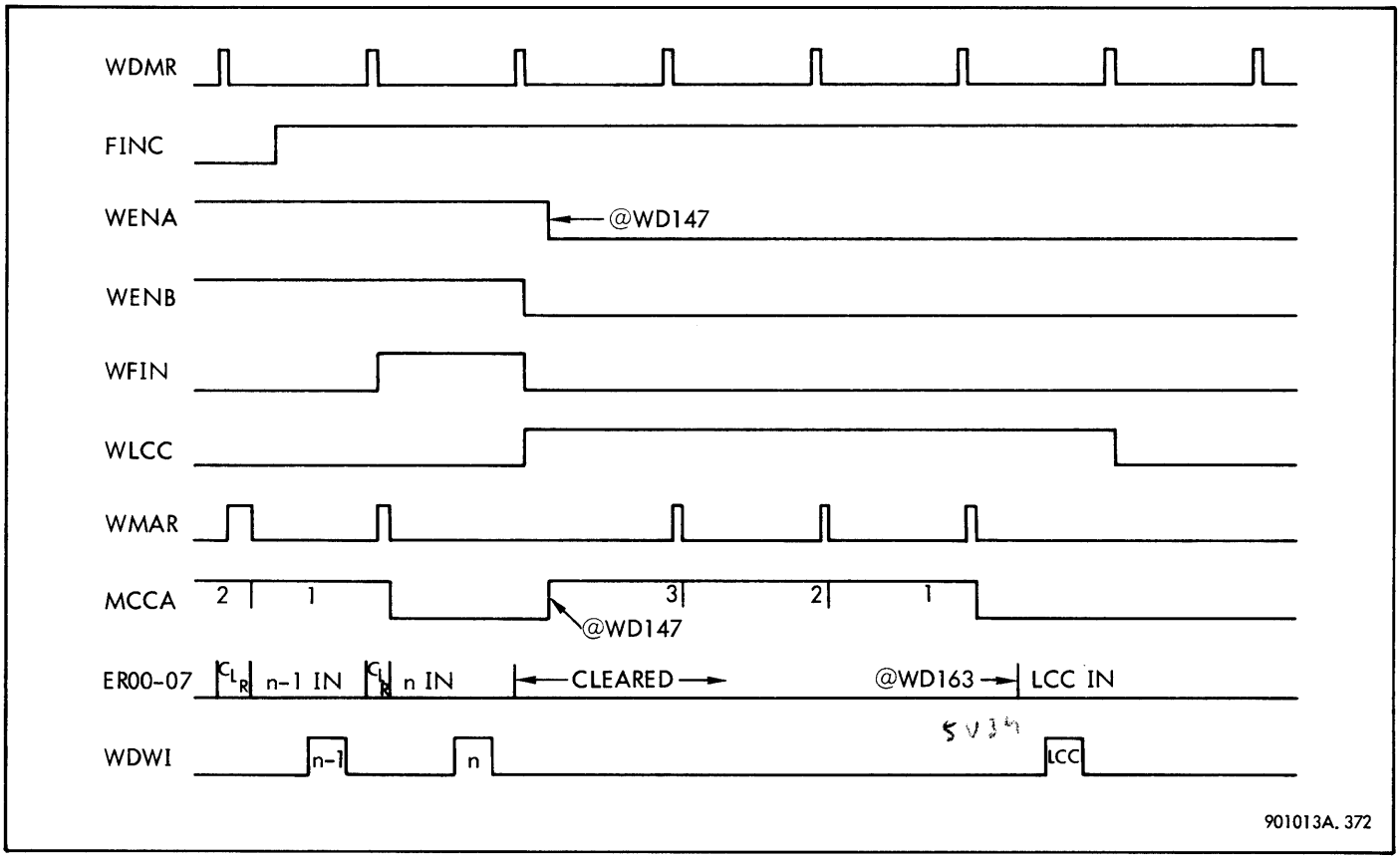


Figure 3-73. Write Finish BIN or BCD Mode (800 bpi), Timing Diagram

In the case of 3n bytes, the last character contains bits 18 through 24 of the three byte set. In the case of 3n + 1 bytes, the last byte contains bits 7 and 8 and four zeros. In the case of 3n + 2 bytes, the last byte contains bits 13, 14, 15, 16, and two zeros.

The end sequence begins when the signal WDMR occurs and FINC, the controller finished signal, is true and MCCA is false, which indicates that the memory is empty. At this time, WFIN is set:

S/WFIN = NWFIN FINC NMCCA DPAK + ...
C/WFIN = WDMR WENA

If either PCH0, PCH1, or PCH3 is true, the buffer register is cleared, as if a byte were to be received from memory:

E/BR00-07 = WENA WDMR NPCH2 + ...

No data request is made from the memory when FINC is true and MCCA is false:

C/WMAR = WDMR NPCH2 WENA
(NFINC + MCCA) + ...

The shift and write sequence is followed in the same manner as though the end sequence were not being performed. In the case of 3n bytes, the shift sequence placed the last six bits in position in the buffer register for writing, and at WDMI time they are transferred to the write toggle flip-flops.

In the case of 3n + 1 bytes, the shift sequence brought bits 7 and 8 to the most significant bit positions of the buffer register. The four least significant bit positions are zero, since the buffer register, which was cleared in anticipation of the next character, was never loaded. Thus at WDWI time, bits 7 and 8 and four zeros are written.

In the case of 3n + 2 bytes, the action is similar except that the remaining four bits are written along with two zeros.

At the WDMR time, following the writing of the last character, WFIN and WENB are reset and WLCC is set. The longitudinal check character is then recorded in the identical manner as for nonpack operations. Figure 3-74 gives a timing diagram for the write finish operation in the pack mode.

WRITE TAPE MARK. A tape mark is defined as a record consisting of only BCD code 17_8 characters. There are two ways to create this record. The standard method is for the CPU to send a write tape mark order. The tape system then automatically writes a single 17_8 character, even parity, and its accompanying longitudinal check character.

An optional procedure is to send a write BCD, one byte (or more) code X'7F' order. The system then creates a tape mark, using the standard write operation. This method is not recommended, as it involves needless programming and, in the case of multiple byte tape marks, may introduce interpretation problems in other than Sigma-series equipment.

A tape mark operation begins when the controller sets WTM true. This is directly converted to DWTM. The first clock after DWTM is true sets WENA:

S/WENA = NFINC DWTM + ...
C/WENA = CLOCK

The next WDMR signal (WDC time 143) sets WFIN:

S/WFIN = NWFIN DWTM + ...
C/WFIN = WENA WDMR

At the next WD16 (WDC time 163), the hexadecimal code X'7F' is inserted into the buffer register. This code is the EBCDIC code which, when converted to BCDIC, is a √ or tape mark. FINC is also set to inhibit the write logic:

M/BR01-07 = DWTM WD16 WFIN + ...
M/FINC = DWTM WD16 WFIN

The write data transfer logic is enabled to transfer the BCD equivalent of the buffer register contents to the write toggle flip-flops during the WDWI interval:

WBCD = WFIN DWTM

The next WDMR time resets WFIN and sets WLCC, and the standard longitudinal check character write procedure then completes the record. Figure 3-75 shows a timing diagram for the write tape mark operation.

3-67 Read Operations

READ START. At the beginning of the write, read, or space operations, the assembly period counter is reset and the deskew logic is primed. Any signal that appears on the read amplifier lines to the peak detectors starts the data assembly logic.

At the end of the assembly period, EAP1, the assembled character is ready for transfer. In space or read after write operations, the assembly register is transferred into the longitudinal check register and the bit crowding register. In read operations, the data is transferred as above, and in addition, RCPD is set to signal the buffer register that a character is ready. The read process then follows the normal pattern.

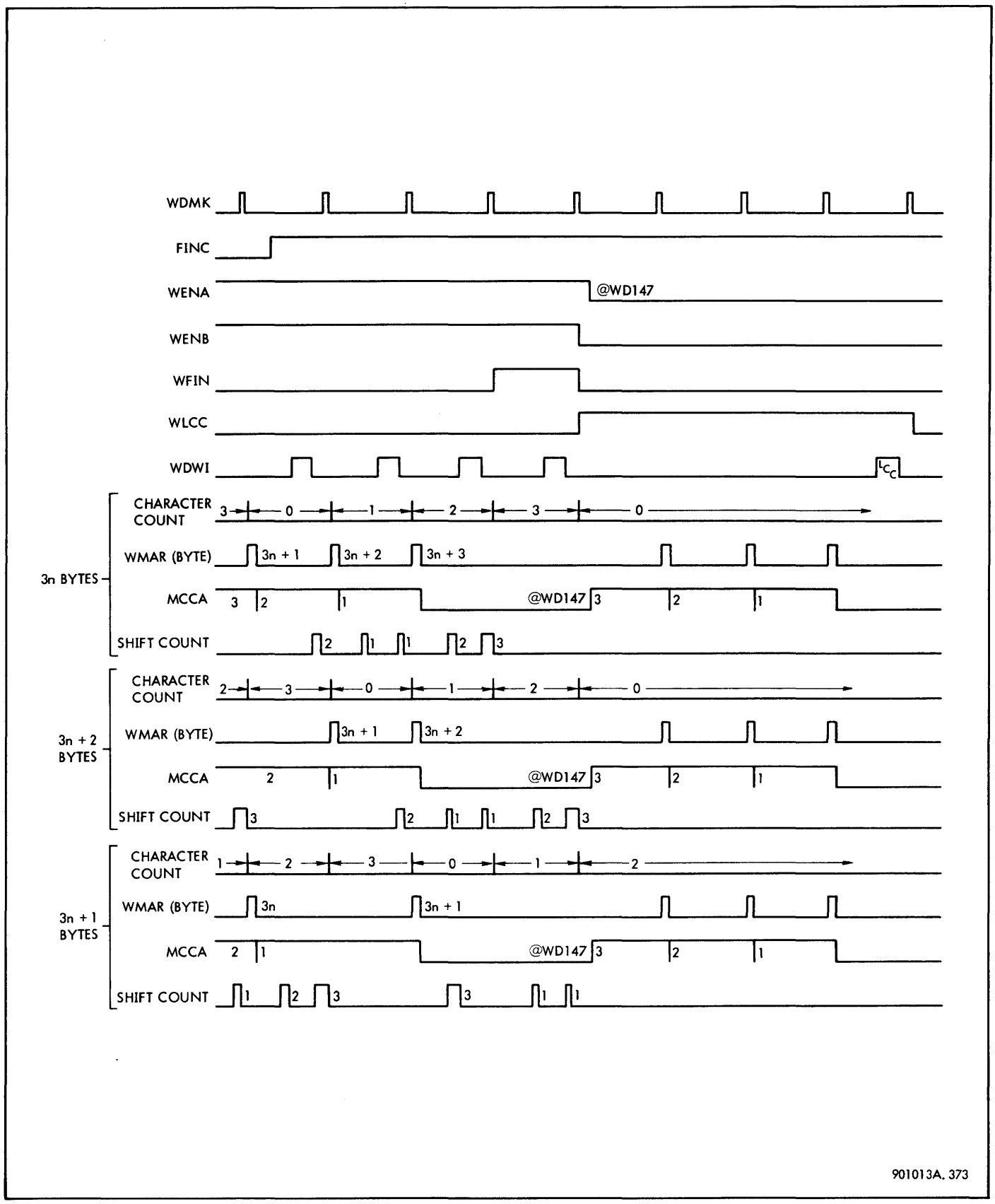


Figure 3-74. Write Finish Pack Mode (800 bpi), Timing Diagram

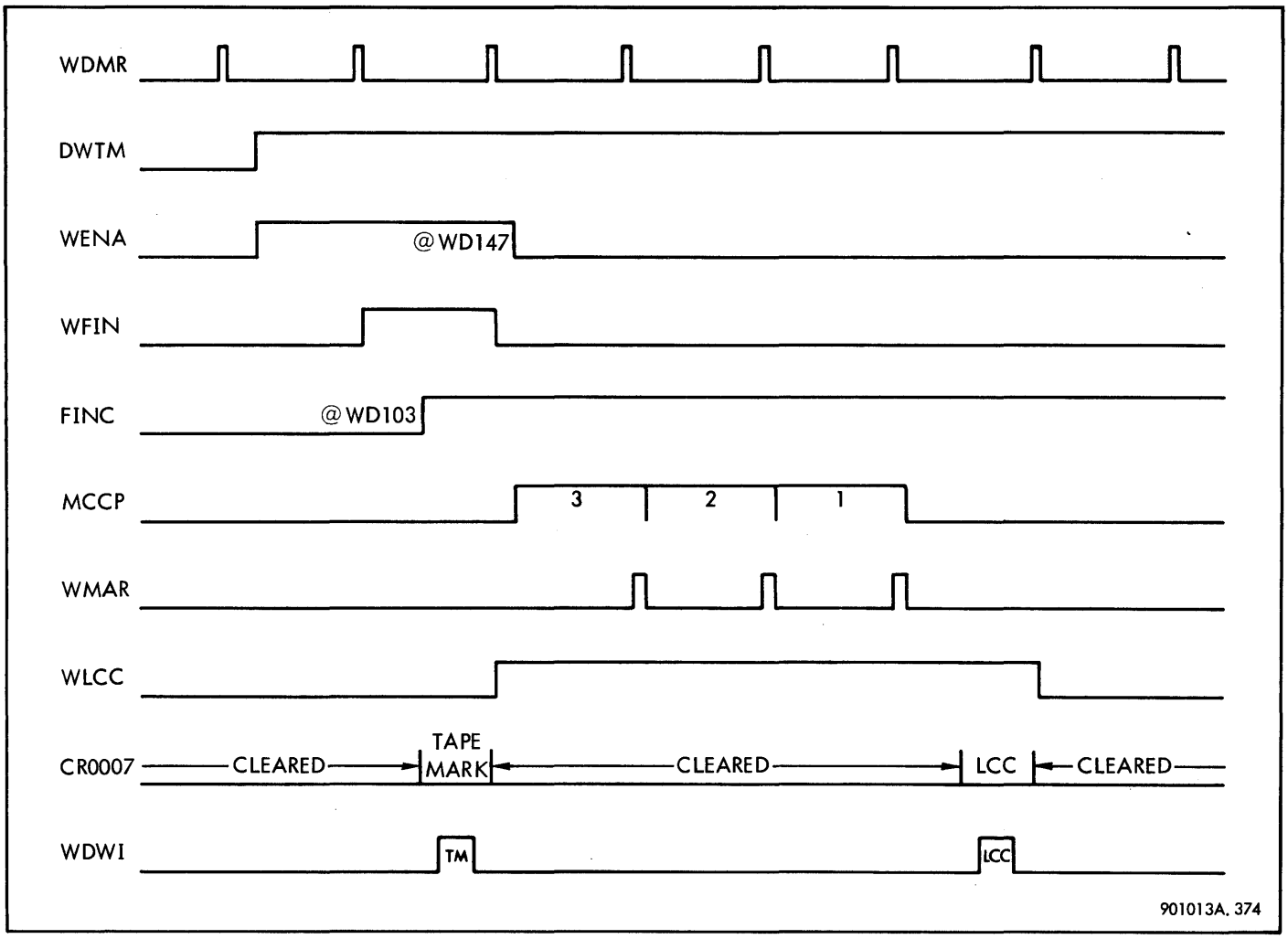


Figure 3-75. Write Tape Mark (800 bpi), Timing Diagram

The first character assembled sets RXF1. The second character resets RXF1 and sets RXF2. These flip-flops are used to prevent stopping the tape, during space reverse operations, until at least two characters have been assembled and transferred:

S/RXF1 = NRXF1 NRXF2
C/RXF1 = EAP2

S/RXF2 = Always true
C/RXF2 = RXF1

Figure 3-76 shows a timing diagram for the read start operation.

READ PROCESS. The read assembly logic, consisting of the digital deskew network, assembly time register, longitudinal check register, and bit crowding register, is always enabled. During writing, the read logic is used to verify the data being written as a read after write check. During spacing operations, the logic checks for errors, gap, and tape marks. During read, the logic performs as in a spacing operation, but it also transfers the assembled character to the buffer register and then to the memory.

The operations of digital peak detection, digital deskew, and character assembly are the same for all three densities and for all three data modes. The only differences are that bit crowding correction is applied at 800 bpi and 556 bpi and that the assembly interval and gap detection times are different for each density setting.

Peak Detection and Deskew. The digital peak detector is a six-stage binary counter which converts the output of the read amplifier into a binary count. The read amplifier output is a square wave derived from the amplified and clipped read head signal.

The appearance of the read amplifier output signal at the peak detector enables the peak detector counter:

S/CnP1 = CHNn NCnP1

C/CnP1 = CLOK

S/CnP2 = NCnP2

C/CnP2 = CnP1 CLOK

⋮

S/CnP6 = NCnP6

C/CnP6 = CnP1 CnP2 CnP3 CnP4 CnP5 CLOK

n = 0, 1, 2, 3, 4, 5, P

When the counter has reached a value which indicates that the read amplifier output is of sufficient duration to constitute a legitimate signal, the qualify signal is set:

S/CnPQ = + WRITE NCnP1 NCnP2 CnP3 CnP4 NCnPT

+ NWRITE NCnP1 CnP2 CnP3 NCnP4 NCnPT

C/CnPQ = CLOK

The different counts required by write and not-write are due to the fact that, during write, the signal must be longer to ensure subsequent readability.

When the read amplifier signal goes false, the transfer signal is set:

S/CnPT = CnPQ NCHNn CnDZ

C/CnPT = CLOK

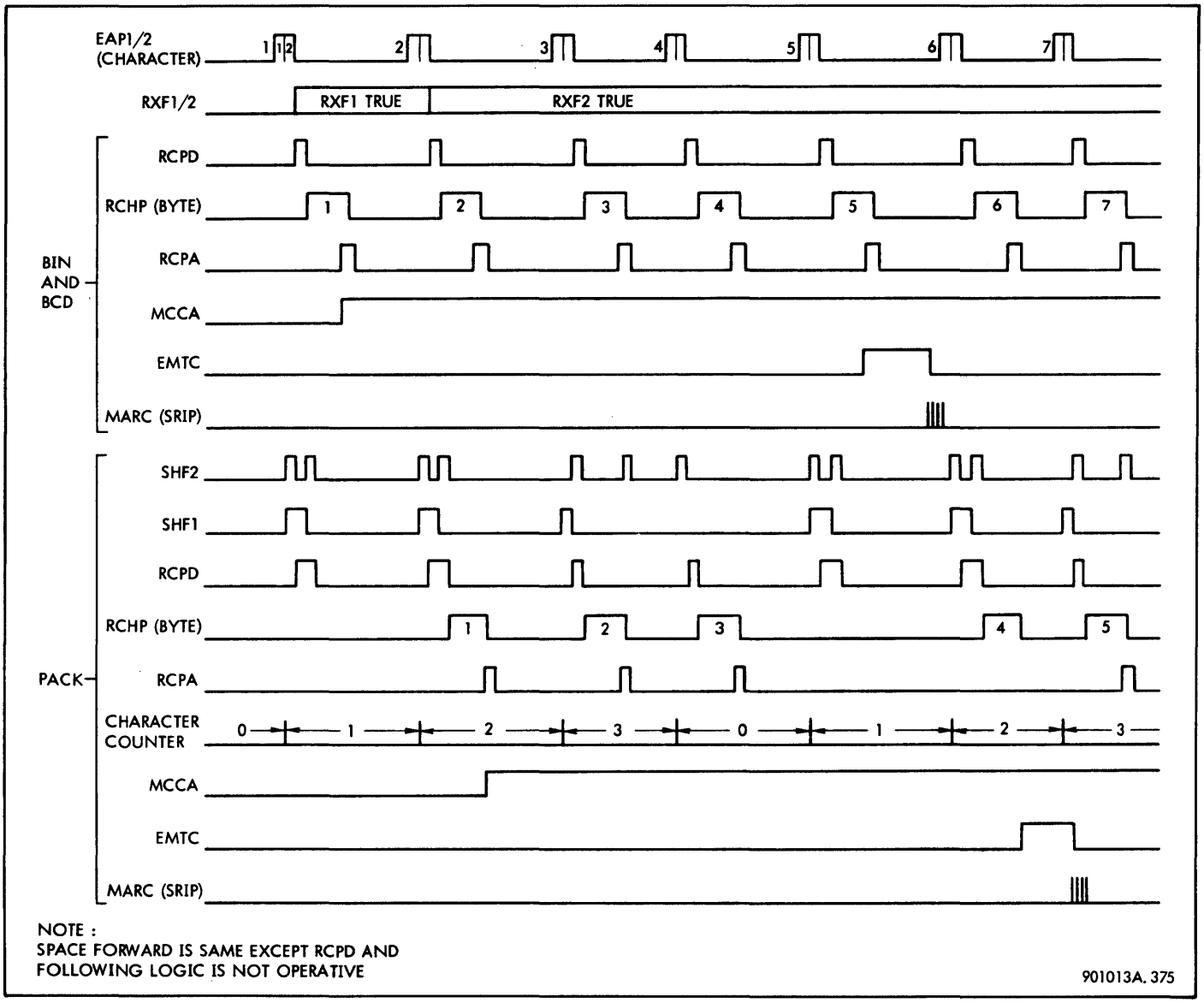


Figure 3-76. Read Start, Timing Diagram

The signal CnDZ indicates that the deskew counter is reset. One clock time later, CnPQ and CnPT are reset, and the peak detector counter contents are transferred to the deskew counter. The peak detector counter is then reset:

```
R/CnPQ   =  CnPT
R/CnPT   =  CnPT

M/CnD1   =  CnP2 CnPT
M/CnD2   =  CnP3 CnPT
   :           :
M/CnD5   =  CnP6 CnPT

E/CnP1-CnP6 = NCHNn NCnPQ
```

The transfer of the peak detector counter contents into the deskew counter effectively divides the peak detector value in half. The deskew counter at transfer time is set at a value which it would have reached had it begun counting at the peak of the read amplifier signal.

The deskew counter then counts up to a value determined by the bit crowding correction network. At that time it starts the bit crowding counter:

```
S/CnD1   =  NCnD1 NCnDZ
C/CnD1   =  CLOK NCnPT

S/CnD2   =  NCnD2
C/CnD2   =  CLOK NCnPT CnD1
   :
S/CnD5   =  NCnD5
C/CnD5   =  CLOK NCnPT CnD1 CnD2 CnD3
            CnD4
CnDZ     =  NCnD1 NCnD2 NCnD3 NCnD4
            NCnD5
```

The bit crowding network monitors the previous bit in the particular channel. If the previous bit is a zero, the bit crowding counter is started when the deskew counter reaches 37_8. If the previous bit is a one, the counter is started when the count reaches 35_8:

```
CnBC     =  + CnD5 CnD4 CnD3 CnD2 CnD1
            (DEN2 + NPARn)
            + CnD5 CnD4 CnD3 NCnD2 CnD1
            (NDEN2 PARn)
```

By starting the bit crowding counter earlier, if the previous bit is a one, the effective location of the peak is moved ahead in time to compensate for the backward shift in time of the peak due to bit crowding. Bit crowding correction is not performed at 200 bpi.

The bit crowding counter now advances until the output of the counter is equal to the settings of the deskew jumpers:

```
S/CnB1   =  + CnBC NCnB1
            + NCnB1 CnB2
            + NCnB1 CnB3
C/CnB1   =  CLOK
S/CnB2   =  NCnB2
C/CnB2   =  CnB1 CLOK
S/CnB3   =  NCnB3
C/CnB3   =  CnB1 CnB2 CLOK
```

The deskew jumpers are located in the station logic. They represent a three-bit binary equivalent of the skew correction required to bring the static skew of the particular channel into alignment with that of the other channels.

When equality is reached between the deskew jumper value and the bit crowding counter, the data bit is ready and a one is set into the appropriate bit position in the assembly register:

```
RBDn     =  [CnJ1 CnB1 + NCnJ1 NCnB1]
            [CnJ2 CnB2 + NCnJ2 NCnB2]
            [CnJ3 CnB3 + NCnJ3 NCnB3]
S/ASRn   =  RBDn
R/ASRn   =  EAP2
C/ASRn   =  CLOK
```

The assembly register resets after the previous character is transferred. It then accepts the outputs of each of the seven-bit crowding counters until the end of the assembly period, at which time the character is transferred out.

Assembly. The assembly period is controlled by a 10-stage binary counter, AP01 through AP10. This counter serves to define the end of the assembly period short gap, between data and LCC character, and the long gap (to signal the controller that the record is completed).

The first data bit to arrive in time resets the assembly period counter, count signal APOB, and sets the APC start control APOA:

```
RBDC     =  RBD0 + RBD1 + ... + RBDP
S/APOB   =  + APOA NRES
            + APOB NRES NAPCZ NFINS
            NRBDC
R/APOB   =  APOB
C/APOB   =  CLOK
C/AP01-AP10 = NAPOB
S/APOA   =  NAPOA RBDC
R/APOA   =  EAP1
C/APOA   =  CLOK
```

APOB is set on the next clock and the assembly period counter increments with each succeeding clock pulse:

S/AP10 = NAP10 APOB
C/AP10 = CLOK
S/AP09 = NAP09
C/AP09 = AP10 CLOK
S/AP08 = NAP08
C/AP08 = AP10 AP09 CLOK
⋮
S/AP05 = NAP05
C/AP05 = AP10 AP09 AP08 AP07 AP06 CLOK

The four highest stages count in a ripple fashion:

S/AP04 = NAP04
C/AP04 = AP05
⋮
S/AP01 = NAP01
C/AP01 = AP02

The end assembly period signal, EAP1, is different for each density and for write or not write. EAP1 represents the closing of the allowable skew interval:

S/EAPA = DEN8 [AC02 + AC04 + ...]
C/EAPA = CLOK
S/EAPB = DEN5 [AC02 + AC05 + ...]
C/EAPB = CLOK
S/EAPC = DEN2 [AC03 + AC06 + ...]
C/EAPC = CLOK
AC02 = Write (APC count of 10_8)
AC04 = Notwrite (APC count of 15_8), etc.
EAP1 = EAPA + EAPB + EAPC

The end of assembly period, EAP1 transfers the contents of the assembly register into the longitudinal check register, LCR, the previous bit register, PAR, and also sets EAP2.

S/LCRn = NLCRn
R/LCRn = LCRn
C/LCRn = EAP1 ASRn

S/PARn = ASRn
C/PARn = EAP1

S/EAP2 = EAP1
C/EAP2 = CLOK

EAP2 is used to reset the assembly register and set the read character present signal if a read operation is in progress:

R/ASR0-ASRP = EAP2
S/RCPD = EAP2 NRLCC
C/RCPD = CLOCK READ

The assembly period counter continues counting beyond EAP1 until either the next RBDC appears (at which it resets to begin another assembly period) or the short gap time is reached, indicating the end of the record.

Transfer to Memory. During read operations, the arrival of EAP2 indicates that a character has been assembled and is ready for transfer into the memory. The memory access request is made immediately in binary or BCD operations. In pack mode, the buffer register must undergo precess operations before the request can be made.

In binary or BCD mode, the end of assembly period signal, EAP1, transfers the contents of the assembly register into the buffer register:

M/BR00 = XASR ASR0
M/BR01 = XASR ASR1
⋮
M/BR05 = XASR ASR5
XASR = READ EAP1 NRLCC

One clock later, EAP2 sets RCPD to signal the buffer register that the character is ready:

S/RCPD = EAP2 NRLCC
R/RCPD = NSHF1
C/RCPD = READ CLOK

In the nonpack modes, SHF1 is never set, as no shifting is necessary. One clock later, RCPD is reset and RCHP, the read character present signal, is set:

S/RCHP = RCPD NSHF1
C/RCHP = NPCH1 CLOK

RCHP then sets the memory access request true:

MARS = RCHP NRCPA NMFUL + ...

When DLDP goes true, signifying that the memory is ready, the buffer register contents are transferred to memory. In binary mode, the transfer is as follows:

MIN0 = XBIN GND + ...
MIN1 = XBIN GND + ...
MIN2 = XBIN BR00 + ...
⋮
MIN7 = XBIN BR05 + ...
XBIN = DLDP MBTM DBIN READ

In BCD mode, the EBCDIC equivalent of BR00 through BR05 is transferred:

MIN0 = XBCD (BR02 NBR03 NBR04 + BZER + NBR02 NBAMP NBLN NBSLS NBDSH) + ...
MIN1 = XBCD "TRUE" + ...
MIN2 = XBCD (BDSH + NBR00 NBLN) + ...
MIN3 = XBCD (BAMP + NBR01 NBDSH) + ...
MIN4 = XBCD (BR02 NBZER) + ...
MIN5 = XBCD (BR03) + ...
MIN6 = XBCD (BR04 NBZER) + ...
MIN7 = XBCD (BR05) + ...
XBCD = DLDP MBTM DBCD READ
BBLN = Buffer register BCDIC code of blank
BDSH = Buffer register BCDIC code of dash
BSLS = Buffer register BCDIC code of slash
BAMP = Buffer register BCDIC code of ampersand
BZER = Buffer register BCDIC code of zero

DLDP sets the acknowledge signal RCPA:

S/RCPA = NRCPA
C/RCPA = MBTM NRCPA DLDP + ...

RCPA resets RCHP and the station access request is dropped; RCPA is reset one clock later:

R/RCHP = RCPA
C/RCHP = NPCH1 CLOK
R/RCPA = RCPA
C/RCPA = RCPA NRCHP CLOK + ...

During the interval NRCHP through RCPA, the buffer register is cleared in preparation for the next character to be received from the assembly register:

E/BR00-BR07 = RCPA NRCHP

READ PACK. The pack mode operates in the same manner except that the buffer register is precessed so that four six-bit characters from the tape are assembled and transferred to the memory in the form of three eight-bit bytes.

At the start of the read cycle, PCH0 is true. The end of assembly period signal, EAP1, advances the character to state 1, loads the character into the buffer register, sets SHF1 and SHF2, and sets EAP2:

C/CHR1-CHR2 = READ EAP1 DPAK + ...
XASR = EAP1 READ NRLCC
S/SHF1 = READ EAP1 PCH0 + ...
S/SHF2 = READ EAP1 PCH0 + ...
C/SHF1-SHF2 = CLOK
S/EAP2 = EAP1
C/EAP2 = CLOK

The buffer register precesses two positions for each clock pulse, during which either SHF1 or SHF2 is true. Since both SHF1 and SHF2 are set, the buffer register precesses six places. The first six data bits go into BR06 through BR11:

S/BR00 = BR10
S/BR01 = BR11
S/BR02 = BR00
⋮
S/BR11 = BR09
C/BR00-BR11 = (SHF1 + SHF2) CLOK

RCPD is set by EAP2 and reset at the completion of the precess. RCHP is not set, because the character is now in state 1:

S/RCPD = EAP2 NRLCC
R/RCPD = NSHF1
C/RCPD = READ CLOK
S/RCHP = NSHF1 RCPD
C/RCHP = NPCH1 CLOK

The data logic now waits for the second six bits to be assembled in the assembly register.

The arrival of EAP1 for the second group of six bits transfers the contents of the assembly register into the buffer register, advances the character counter to state 2, sets SHF1 and SHF2, and sets EAP2:

S/SHF1 = READ EAP1 PCH1
S/SHF2 = READ EAP1 PCH1

The buffer register now precesses six places, placing data bits 1 through 12 into BR00 through BR11.

RCPD is set by EAP2 and reset at the completion of the shift. RCHP is then set to signal the memory that the first byte is ready:

S/RCHP = NSHF1 RCPD
C/RCHP = NPCH1 CLOK

Buffer register stages 00 through 07 are transferred to the memory by DLDP:

MIN0 = XPAK BR00 + ...
⋮
MIN7 = XPAK BR07 + ...

XPAK = DLDP MBTM READ DPAK

RCPA is set by DLDP, and RCPA in turn clears the buffer register and resets RCHP. The data logic waits for the EAP1 signal from the third character.

When EAP1 occurs, the assembly register is transferred to the buffer register, EAP2 is set, the character counter is advanced to state 3, and SHF1 is set to precess the register:

S/SHF1 = EAP1 READ PCH2 + ...

The buffer register precesses four positions to place bits 8 through 18 in BR00 through BR09, respectively. EAP2 sets RCPD, which in turn sets RCHP when the precess is completed. RCHP drives the memory access request.

RCPA is set by DLDP to indicate that the second byte has been taken by memory. The buffer register stages BR00 through BR07 are cleared by RCPA after RCHP is reset. SHF2 is set to precess the register two places:

S/SHF2 = READ RCPA NRCHP PCH3 + ...

Data bits 17 and 18 are in BR10 and BR11, respectively, after the shift is completed. The buffer register now awaits the fourth character.

When the EAP1 corresponding to the fourth character occurs, the assembly register is transferred to the buffer register, EAP2 is set, the character counter is advanced to state 0, and SHF2 is set to precess the register:

S/SHF2 = PCH3 EAP1 READ

The register shifts two places to place data bits 17 to 24 in BR00 through BR07. RCPD and RCHP are set when the shift is completed. RCHP drives the memory access request.

After the byte has been accepted by the memory, RCPA is set. RCPA resets RCHP and clears the buffer register. The read logic now waits for the first character of the next four-character group.

Figure 3-77 shows a timing diagram of the read data transfer operation. Table 3-9 presents the status of the buffer register during a read pack operation.

READ FINISH. The termination of the read data process consists of two operations: the detection of the longitudinal check gap, and the processing of the last characters in the case of a read pack cycle. In read after write checking and in spacing operations, the logic checks the longitudinal check character validity and then signals an end to the controller. In reading, checking is done and the last data characters are transferred to memory. A gap is defined as the absence of characters for an interval of approximately 2.2 character periods. When this situation occurs, the end of the data portion is assumed to have occurred and the termination process begins.

After each character is transferred out of the assembly register by EAP1, the assembly period counter continues counting upwards. The first bit to occur in the next frame, RBDC, resets the counter and restarts the process. In the event that the counter is not reset by an RBDC signal before it reaches the gap time, RLCC, the read longitudinal check character control, is set. The gap time is different for each of the recording densities:

S/RLCC = RXF2 (AC13 + AC14 + AC15)

C/RLCC = NRLCC CLOK

AC13 = DEN8 (APC count = 107_8)

AC14 = DEN5 (APC count = 147_8)

AC15 = DEN2 (APC count = 427_8)

RXF2 indicates that at least two characters have been transferred out of the assembly register.

Once RLCC is set, it can only be reset by the general controller reset signal. RLCC inhibits transferring the LCC character into the memory by blocking RCPD:

SCPD = EAP2 NRLCC

RLCC also signals the controller if there are any bytes remaining in memory:

BMTC = RLCC MCCA NTMKD + ...

The data electronics now waits for the LCC character to arrive. When the RBDC signal for the LCC character appears, the APC counter is reset and the normal assembly period begins.

When EAP1 occurs, the assembly register contents are transferred into the LCR register. One clock time later, EAP2 is set, which clears the assembly register and sets FINS, the station finished control. FINS signals the controller that all reading and checking is finished:

S/FINS = RLCC

C/FINS = EAP2 CLOK

APOB is reset by FINS, which then resets the APC counter:

S/APOB = APOB NRES NRBDC NAPCZ NFINS + ...

C/APOB = CLOK

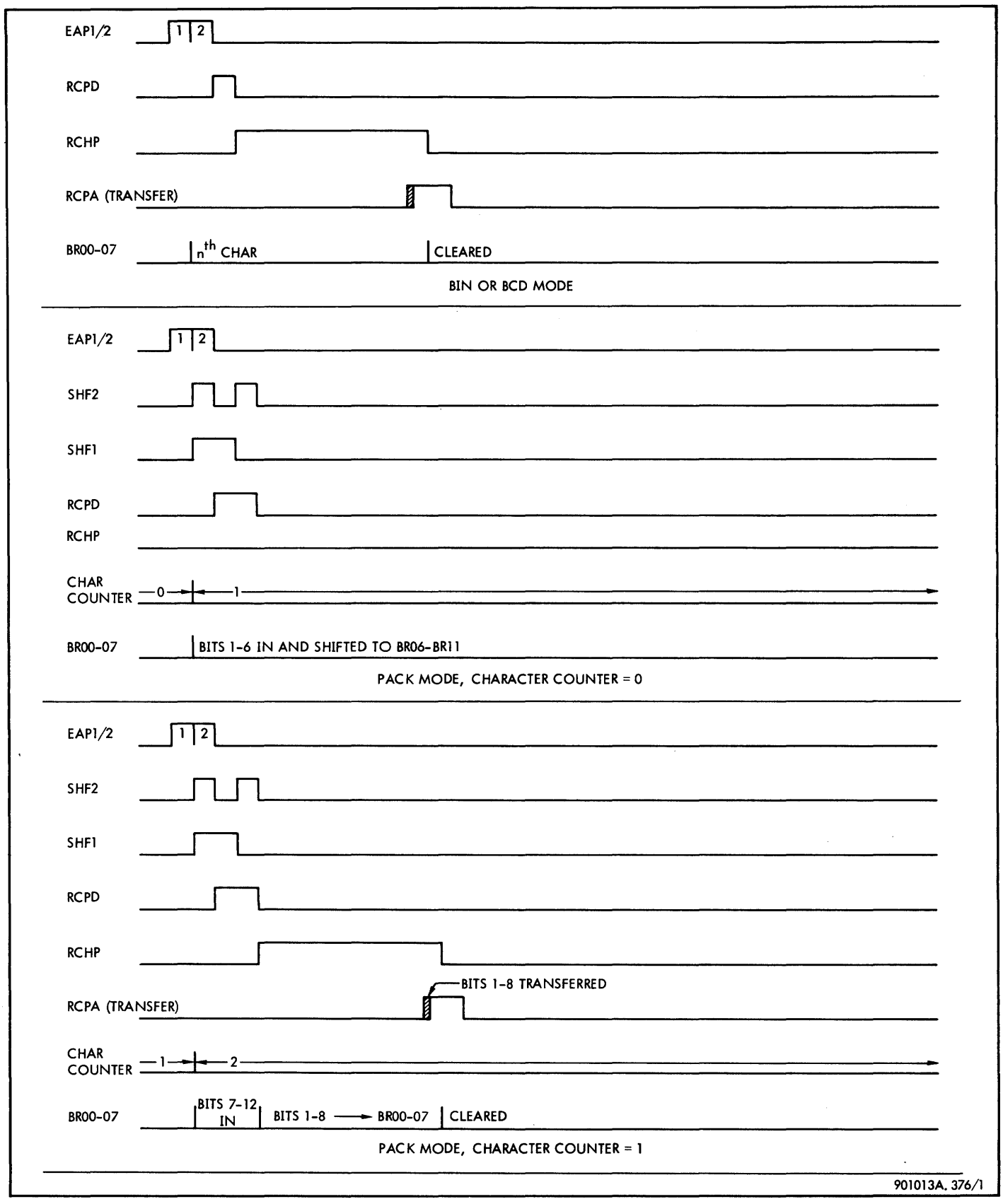


Figure 3-77. Read Operation, Timing Diagram (Sheet 1 of 2)

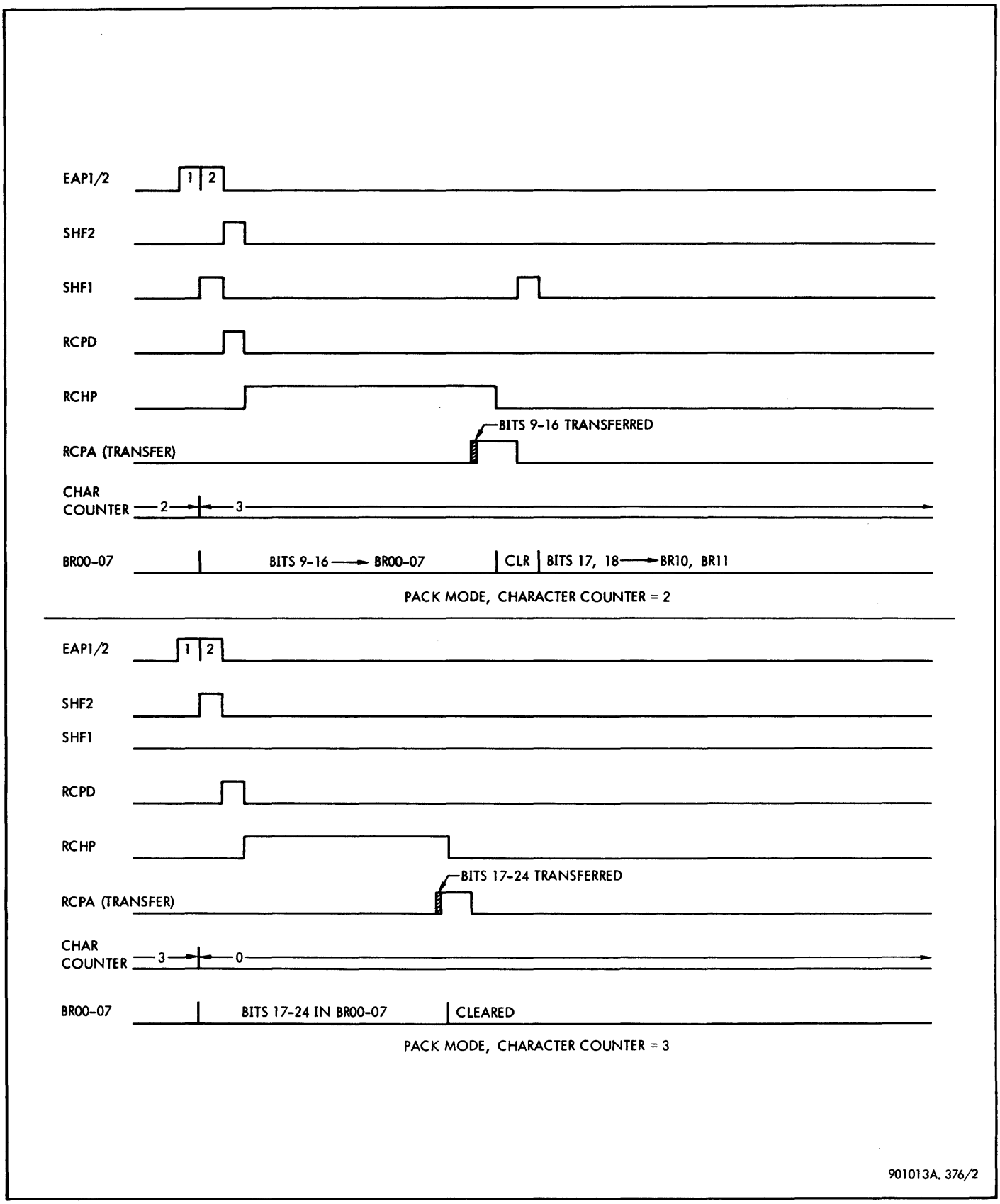


Figure 3-77. Read Operation, Timing Diagram (Sheet 2 of 2)

Table 3-9. Buffer Register Status During Read Pack

SIGNAL NAME	CHARACTER COUNTER STATE	BUFFER REGISTER CONTENTS*												REMARKS
		0	1	2	3	4	5	6	7	8	9	10	11	
EAP1	0									X	X	X	X	BR00-07 erased. EAP1 will load first character
EAP2	1	1	2	3	4	5	6			X	X	X	X	First character in from assembly register. Three shifts will now be done
EAP1	1							1	2	3	4	5	6	Three shifts done. EAP1 will load second character
EAP2	2	7	8	9	10	11	12	1	2	3	4	5	6	Second character in from assembly register. Three shifts will be done and RCHP will be set
RCPA	2	1	2	3	4	5	6	7	8	9	10	11	12	Bits 1-8 sent to memory. BR00-07 will be cleared
EAP1	2									9	10	11	12	BR00-07 erased. EAP1 will load third character
EAP2	3	13	14	15	16	17	18			9	10	11	12	Third character in from assembly register. Two shifts will be done and RCHP will be set
RCPA	3	9	10	11	12	13	14	15	16	17	18			Bits 9-16 sent to memory. BR00-07 will be erased and one shift will be done
EAP1	3											17	18	BR00-07 erased and one shift done. EAP1 will load fourth character
EAP2	0	19	20	21	22	23	24					17	18	Fourth character in from assembly register. One shift will be done and RCHP will be set
RCPA	0	17	18	19	20	21	22	23	24					Bits 17-24 sent to memory. BR00-07 will be erased
EAP1	0													BR00-07 erased. EAP1 will load first character of next group
EAP2	1	1	2	3	4	5	6							First character in from assembly register. Three shifts will be done
EAP1	1							1	2	3	4	5	6	Three shifts done. EAP1 will load second character

*Contents given are those at clock time

In the event that the LCC character is not present on tape (i.e., it is all zeros), the end process is different. Once RLCC is set, the counter continues upward, waiting for the RBDC signal of the LCC character. If the RBDC signal does not appear at the long gap time (AC10, 11, 12), the data assembly transfers a dummy character (all zeros) into the LCR register and then sets FINS:

S/EAPA = + AC10 DEN8 + ...
C/EAPA = CLOK
S/EAPS = + AC11 DEN5 + ...
C/EAPC = CLOK
S/EAPC = + AC12 DEN2 + ...
C/EAPC = CLOK

AC10 = RLCC (APC count = 425_8)

AC11 = RLCC (APC count = 605_8)

AC12 = RLCC (APC count = $1{,}765_8$)

Read operations in pack mode are terminated in a different manner than in nonpack mode because a record may not contain a multiple of four characters. When this happens, the data assembly must fill in the last character with zeros.

If the record contains a multiple of four characters, the assembling and transferring to the buffer register of the last character leaves the character counter at PCH0. In this case, the arrival of the gap signal sets RLCC and the logic then operates in identical manner as for nonpack mode endings.

If the record does not contain a multiple of four characters, the assembling and transferring of the last character to the buffer register leaves NPCH0 true and a partial eight-bit byte in the buffer register.

Two clock times before the gap time, a dummy (all zeros) character is transferred to the buffer register and the normal shift for that particular character counter state occurs:

S/EAPA = AC07 DEN8 + ...
C/EAPA = CLOK

S/EAPB = AC08 DEN5 + ...
C/EAPB = CLOK

S/EAPC = AC09 DEN2 + ...
C/EAPC = CLOK

AC07 = NPCH0 (APC count = 105_8)

AC08 = NPCH0 (APC count = 145_8)

AC09 = NPCH0 (APC count = 425_8)

EAP1 transfers the dummy character to the buffer register and EAP2 clears the assembly register. RLCC is set in the same manner as for all other operations and the LCC character is handled in the same manner. Figures 3-78 and 3-79 show timing diagrams for the read finish operations, in the case of 4n and not 4n characters, respectively.

READ TAPE MARK. A tape mark is defined as any record containing only BCD √ characters (17_8, even parity). The tape mark is used to identify and separate series of records on tape and may appear at any time on any (binary, BCD, or pack) data configuration.

At the start of every tape operation, TMKD, the tape mark detect flip-flop is set. If any character read from the tape and transferred out of the assembly register is not a 17_8 even parity character, TMKD is reset, indicating that the record is not a tape mark:

M/TMKD = RES
R/TMKD = TMKD NTMCH
C/TMKD = TMKD NRLCC APOA EAP1
TMCH = NASR0 NASR1 ASR2 ASR3 ASR4 ASR5 NASRP

Once TMKD is reset, it remains reset until the next operation begins. In the event that TMKD is still set after the longitudinal check is finished, TMRK, the tape mark signal, is set when FINS is set:

S/FINS = RLCC
C/FINS = EAP2 CLOK
S/TMRK = TMKD RLCC
C/TMRK = EAP2 CLOK

If the tape mark is encountered during a read operation, read data characters are not sent to the controller, even though the memory has the character, because TMKD is still true:

BMTC = RLCC NTMKD MCCA + ...

If a reverse tape operation, other than rewind, encounters the load point, TMRK is set:

M/TMRK = REV BOTS

3-68 Pack Mode

CHARACTER COUNTER. The packed mode character counter is a two-stage binary counter, CHR1 and CHR2, which defines the four shift and transfer states occurring during pack operation. The outputs of the counter are the four character signals:

PCH0 = NCHR1 NCHR2

PCH1 = NCHR1 CHR2

PCH2 = CHR1 NCHR2
PCH3 = CHR1 CHR2

During a write operation, the character counter is advanced each time a data request is sent to the memory. During a read operation, the counter is advanced each time a character is assembled, as signaled by EAP1:

S/CHR2 = NCHR2
C/CHR2 = CHCL
S/CHR1 = NCHR1
C/CHR1 = CHCL CHR2
CHCL = + WENB DPAK WDMR
+ READ DPAK EAP1

SHIFT COUNTER. The packed mode shift counter is a two-stage binary counter, SHF1 and SHF2, which controls the number of shifts the buffer register makes in each of the four states of the character counter.

The counter is set to the desired count by the set logic and then counts down. As long as either SHF1 or SHF2 is true, the buffer register shifts two places for each clock cycle. Although the maximum shift required is six places, each of the intermediate shifts is either two or four; thus, a shift count of three maximum, with each shift being two places, is sufficient to cover all of the possible conditions.

S/SHF2 = (WD16 WENB PCH1
+ WDFL WENB PCH1
+ WDFL WENB PCH2
+ READ EAP1 PCH0
+ READ EAP1 PCH1
+ READ EAP1 PCH3
+ READ NRCHP RCPA PCH3
+ SHF1 NSHF2) DPAK
S/SHF1 = (WDFL WENB PCH0
+ WDFL WENB PCH2
+ WD16 WENB PCH2
+ READ EAP1 PCH0
+ READ EAP1 PCH1
+ READ EAP1 PCH2
+ SHF1 SHF2) DPAK
C/SHF1 = CLOK
C/SHF2 = CLOK

3-69 Error Detection

There are four types of data errors that can occur in the data electronics. These are rate errors, data parity errors, longitudinal check errors, and tape mark errors.

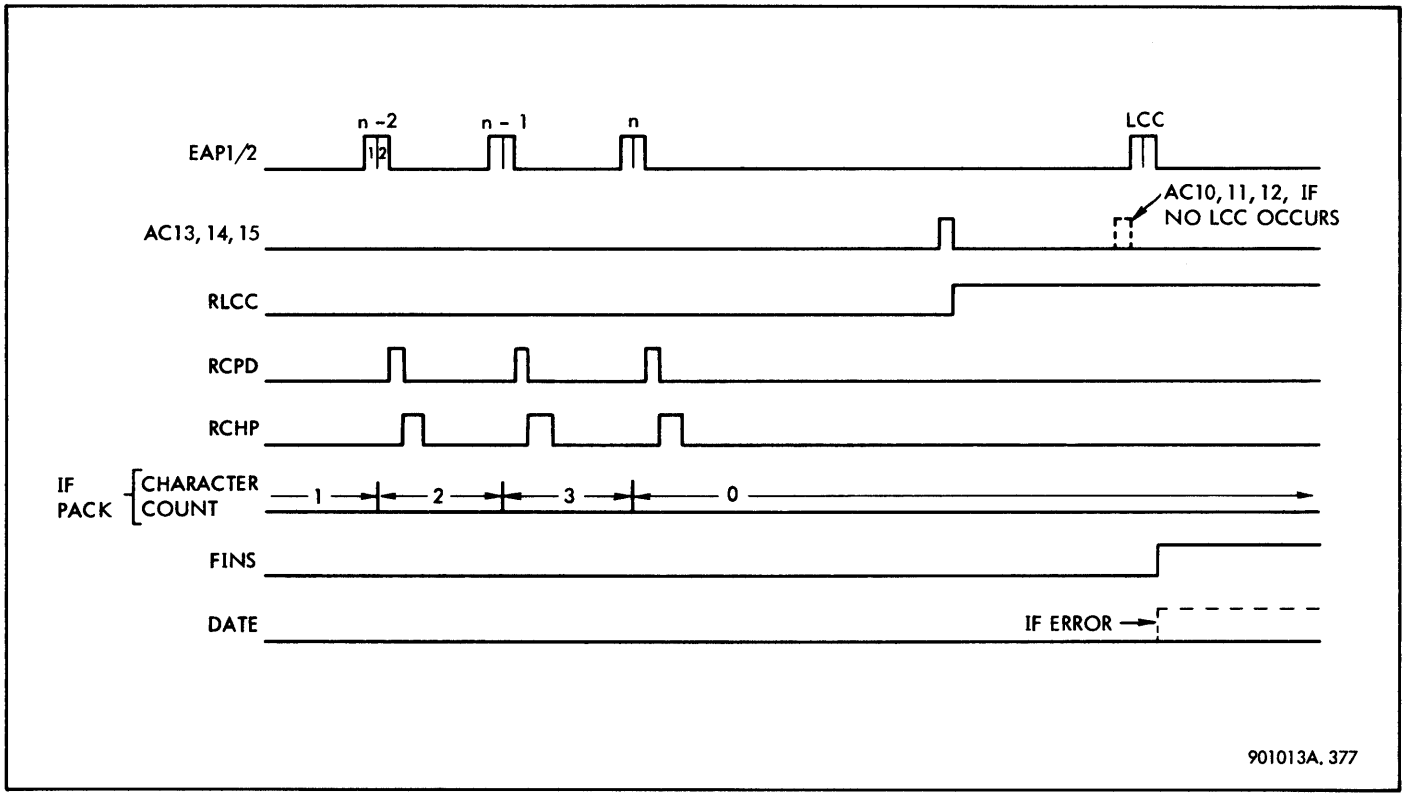


Figure 3-78. Read End (BIN, BCD, or Pack, 4n Characters Read), Timing Diagram

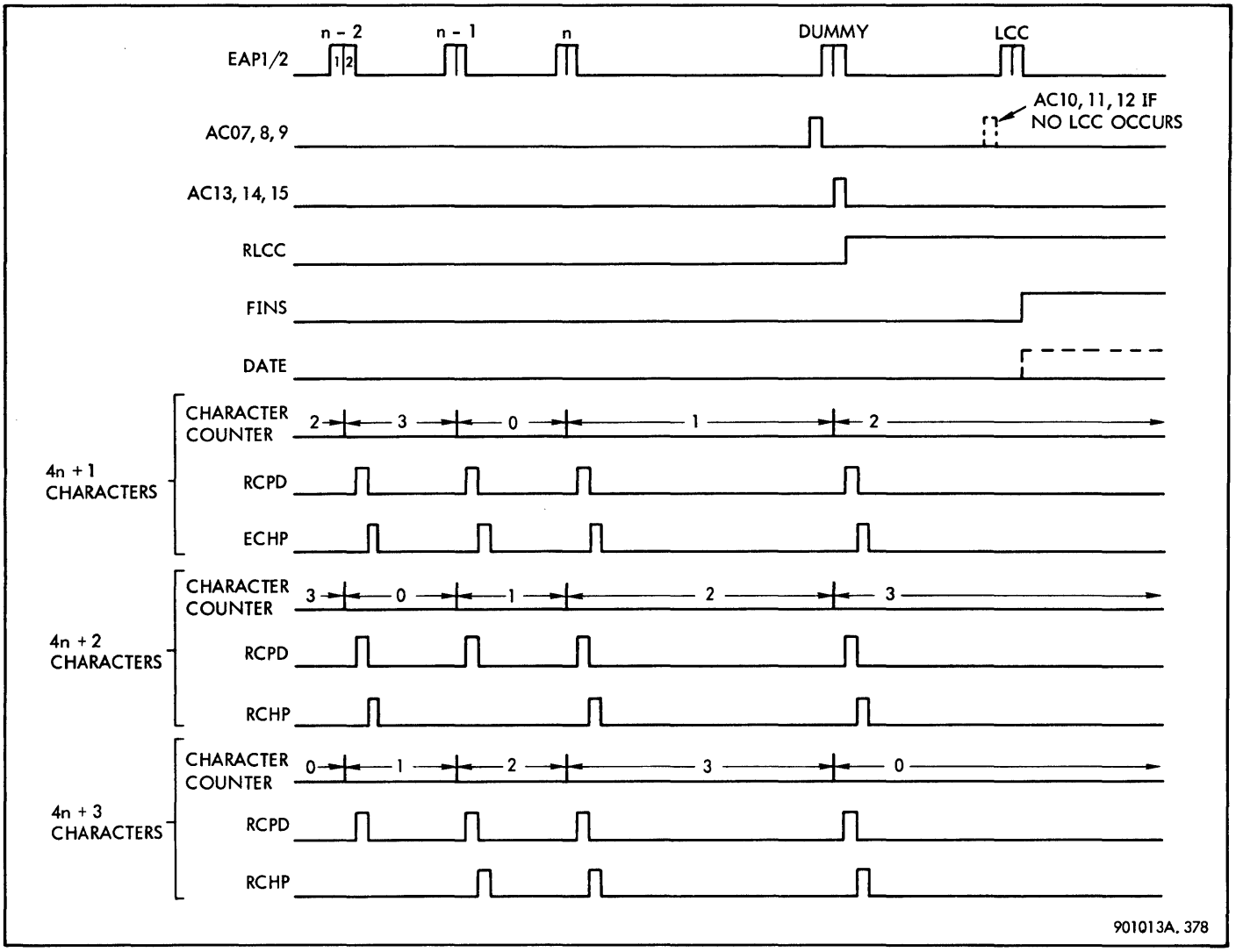


Figure 3-79. Read End (Pack, Not 4n Characters Read), Timing Diagram

RATE ERRORS. The tape system is a real-time device requiring characters to be transferred to or from the tape at specific intervals. If for any reason the transfer is delayed longer than the buffer capacity of the tape system, a rate error is signaled.

During writing, a rate error occurs if the byte requested from memory at WDMR time (WDC count = 143_8) is not available by WD16 time (WDC = 163_8):

RATE = WD16 WMAR + ...

During reading, a rate error occurs if the EAP1 signal (character ready to be transferred from assembly register) goes true and the buffer register is still either requesting memory access or shifting the previous character:

RATE = EAP1 READ CLOK
(RCHP RCPA SHF2)

Once set, rate will remain true until reset by RESN, the SIO/HIO reset signal from the controller:

RATE = RATE NRESN + ...

Data errors can result from failure of the data electronics to maintain character or longitudinal parity or to write a tape mark if so ordered.

PARITY ERRORS. A character parity error occurs if the character read from tape and assembled in the assembly register does not have an odd number of ones, in the case of binary or pack operating modes, or does not have an even number of ones, in BCD or tape mark operations:

S/PARE = ZARP (DBCD + DWTM)
= + NZARP (DBIN + DPAK)

C/PARE = NPARE NRLCC APOA EAP1

Once PARE is set, only the general station reset signal can reset it. APOA is included to inhibit checking parity on the dummy characters inserted into the assembly register during end conditions. NRLCC inhibits checking parity on the LCC character, since it then has indeterminate parity.

At the finish of the record, when FINS is set, DATE is set if a parity error occurred in this record:

DATE = PARE NTMKD RLCC EAP2 + ...

NTMKD prevents data errors when a tape mark is read. This is required because a tape mark can occur in a binary recorded tape. The tape mark, which has even parity, would give a parity error.

Once DATE is set, it remains set until reset by the controller SIO/HIO reset signal:

DATE = DATE NRESN + ...

LONGITUDINAL CHECK ERRORS. Each data channel on the tape must contain an even number of ones. The LCC character produces this result. After data is recorded, any channel which has an odd number of ones receives an additional one in its position in the LCC character.

The longitudinal check register is used to verify the longitudinal parity of each channel. Each of the seven stages of the LCR register monitors its particular channel and toggles, or half-adds, each time a one bit is present. At the end of the record, including the LCC character, each stage should be in the reset state:

S/LCRn = NLCRn

R/LCRn = LCRn

C/LCRn = EAP1 ASRn

n = 0, 1, 2, 3, 4, 5, P

LCRZ = NLCR0 NLCR1 ... NLCRP

If the LCR register is not completely reset, a data error is signaled:

DATE = NLCRZ EAP2 RLCC OPER CLOK + ...

TAPE MARK ERRORS. Verification of a tape mark during writing is done automatically by the character parity logic. PARE is set if the TM character itself does not have an even number of ones:

S/PARE = ZARP DWTM + ...

Since each character of a tape mark record must be a tape mark character, TMKD is reset if a character does not have the proper code. DATE is then set:

DATE = PARE NTMKD EAP2 NRLCC + ...

3-70 BCD-EBCDIC Conversion Charts

Tables 3-10 and 3-11 show BCD-EBCDIC conversion during read and write operations.

Table 3-10. EBCDIC-BCDIC Conversion (62 Set)

EBCDIC								WRITE → READ ←	BCDIC							CHARACTER
0	1	2	3	4	5	6	7		0	1	2	3	4	5	P	
1	1	1	1	0	0	0	0		0	0	1	0	1	0	0	0
1	1	1	1	0	0	0	1		0	0	0	0	0	1	1	1
1	1	1	1	0	0	1	0		0	0	0	0	1	0	1	2
1	1	1	1	0	0	1	1		0	0	0	0	1	1	0	3
1	1	1	1	0	1	0	0		0	0	0	1	0	0	1	4
1	1	1	1	0	1	0	1		0	0	0	1	0	1	0	5
1	1	1	1	0	1	1	0		0	0	0	1	1	0	0	6
1	1	1	1	0	1	1	1		0	0	0	1	1	1	1	7
1	1	1	1	1	0	0	0		0	0	1	0	0	0	1	8
1	1	1	1	1	0	0	1		0	0	1	0	0	1	0	9
1	1	0	0	0	0	0	1		1	1	0	0	0	1	1	A
1	1	0	0	0	0	1	0		1	1	0	0	1	0	1	B
1	1	0	0	0	0	1	1		1	1	0	0	1	1	0	C
1	1	0	0	0	1	0	0		1	1	0	1	0	0	1	D
1	1	0	0	0	1	0	1		1	1	0	1	0	1	0	E
1	1	0	0	0	1	1	0		1	1	0	1	1	0	0	F
1	1	0	0	0	1	1	1		1	1	0	1	1	1	1	G
1	1	0	0	1	0	0	0		1	1	1	0	0	0	1	H
1	1	0	0	1	0	0	1		1	1	1	0	0	1	0	I
1	1	0	1	0	0	0	1		1	0	0	0	0	1	0	J
1	1	0	1	0	0	1	0		1	0	0	0	1	0	0	K
1	1	0	1	0	0	1	1		1	0	0	0	1	1	1	L
1	1	0	1	0	1	0	0		1	0	0	1	0	0	0	M
1	1	0	1	0	1	0	1		1	0	0	1	0	1	1	N
1	1	0	1	0	1	1	0		1	0	0	1	1	0	1	O
1	1	0	1	0	1	1	1		1	0	0	1	1	1	0	P
1	1	0	1	1	0	0	0		1	0	1	0	0	0	0	Q
1	1	0	1	1	0	0	1		1	0	1	0	0	1	1	R
1	1	1	0	0	0	1	0		0	1	0	0	1	0	0	S
1	1	1	0	0	0	1	1		0	1	0	0	1	1	1	T
1	1	1	0	0	1	0	0		0	1	0	1	0	0	0	U

(Continued)

Table 3-10. EBCDIC-BCDIC Conversion (62 Set) (Cont.)

EBCDIC 0 1 2 3 4 5 6 7	WRITE → READ ←	BCDIC 0 1 2 3 4 5 P	CHARACTER
1 1 1 0 0 1 0 1		0 1 0 1 0 1 1	V
1 1 1 0 0 1 1 0		0 1 0 1 1 0 1	W
1 1 1 0 0 1 1 1		0 1 0 1 1 1 0	X
1 1 1 0 1 0 0 0		0 1 1 0 0 0 0	Y
1 1 1 0 1 0 0 1		0 1 1 0 0 1 1	Z
			E / B
0 1 0 0 0 0 0 0		0 1 0 0 0 0 1	Blank / Blank
0 1 0 0 1 0 1 0		1 1 1 0 1 0 0	¢ / ?*
0 1 0 0 1 0 1 1		1 1 1 0 1 1 1	. / .
0 1 0 0 1 1 0 0		1 1 1 1 0 0 0	< /)
0 1 0 0 1 1 0 1		1 1 1 1 0 1 1	(/ [
0 1 0 0 1 1 1 0		1 1 1 1 1 0 1	+ / <
0 1 0 0 1 1 1 1		1 1 1 1 1 1 0	| / ≠
0 1 0 1 0 0 0 0		1 1 0 0 0 0 0	& / &
0 1 0 1 1 0 1 0		1 0 1 0 1 0 1	! / !*
0 1 0 1 1 0 1 1		1 0 1 0 1 1 0	$ / $
0 1 0 1 1 1 0 0		1 0 1 1 0 0 1	* / *

*These characters are only included in the 88 graphic set; however, if they are sent, they will be converted as shown

†On write only. 12_8 during read gives zero

Table 3-10. EBCDIC-BCDIC Conversion (62 Set) (Cont.)

EBCDIC 0 1 2 3 4 5 6 7	WRITE → READ ←	BCDIC 0 1 2 3 4 5 P	CHARACTER E	B
0 1 0 1 1 1 0 1		1 0 1 1 0 1 0	)	]
0 1 0 1 1 1 1 0		1 0 1 1 1 0 0	;	;
0 1 0 1 1 1 1 1		1 0 1 1 1 1 1	¬	△*
0 1 1 0 0 0 0 0		1 0 0 0 0 0 1	-	-
0 1 1 0 0 0 0 1		0 1 0 0 0 1 0	/	/
0 1 1 0 1 0 1 0		0 1 1 0 1 0 1	None	F
0 1 1 0 1 0 1 1		0 1 1 0 1 1 0	,	,
0 1 1 0 1 1 0 0		0 1 1 1 0 0 1	%	%
0 1 1 0 1 1 0 1		0 1 1 1 0 1 0	—	m*
0 1 1 0 1 1 1 0		0 1 1 1 1 0 0	>	\
0 1 1 0 1 1 1 1		0 1 1 1 1 1 1	?	≠*
0 1 1 1 1 0 1 0	Only →	0 0 1 0 1 0 0	:	0†
0 1 1 1 1 0 1 1		0 0 1 0 1 1 1	#	#
0 1 1 1 1 1 0 0		0 0 1 1 0 0 0	@	@
0 1 1 1 1 1 0 1		0 0 1 1 0 1 1	'	:
0 1 1 1 1 1 1 0		0 0 1 1 1 0 1	=	>
0 1 1 1 1 1 1 1		0 0 1 1 1 1 0	"	✓*

*These characters are only included in the 88 graphic set; however, if they are sent, they will be converted as shown

†On write only. 12_8 during read gives zero

Table 3-11. Sigma BCD-EBCDIC Conversion Chart

MOST SIGNIFICANT DIGIT	HEXA-DECIMAL	LEAST SIGNIFICANT DIGIT 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	0	ↄ Null	A	B	C	D	E HT	F	G	H EOM	I	?	.	)	[	<	≠
	1	&	J	K	L	M	N NL	O	P	Q	R	!	$	*	]	;	△
	2	- ds	/ ss	S fs	T si	U	V	W	X	Y	Z	≠	,	%	m	\	≠
	3	0	1	2	3	4	5	6	7	8	9	0†	#	@	:	>	✓
	4	ↄ blank	A	B	C	D	E	F	G	H	I	? ¢	. .	) <	[(	< +	≠ |

(Continued)

Table 3-11. Sigma BCD-EBCDIC Conversion Chart (Cont.)

MOST SIGNIFICANT DIGIT	HEXA-DECIMAL	LEAST SIGNIFICANT DIGIT 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	5	& &	J	K	L	M	N	O	P	Q	R	! !	$ $	* *	])	; ;	△ ¬
	6	- -	/ /	S	T	U	V	W	X	Y	Z	‡	, ,	% %	m _	\ >	++ ?
	7	0	1	2	3	4	5	6	7	8	9	0* :	# #	@ @	: '	> =	"
	8	b	A a	B b	C c	D d	E e	F f	G g	H h	I i	?	.	)	[	<	≠
	9	&	J j	K k	L l	M m	N n	O o	P p	Q q	R r	!	$	*	]	;	△
	A	-	/	S s	T t	U u	V v	W w	X x	Y y	Z z	‡	,	%	m	\	++
	B	0	1	2	3	4	5	6	7	8	9	0*	#	@	:	>	✓
	C	b	A A	B B	C C	D D	E E	F F	G G	H H	I I	?	.	)	[	<	‡
	D	&	J J	K K	L L	M M	N N	O O	P P	Q Q	R R	!	$	*	]	;	△
	E	-	/	S S	T T	U U	V V	W W	X X	Y Y	Z Z	‡	,	%	m	\	++
	F	0 0	1 1	2 2	3 3	4 4	5 5	6 6	7 7	8 8	9 9	0*	#	@	:	>	✓ CD

*Codes X'3A', '7A', 'BA', and 'FA' are recorded and read back as BCD '0'

NOTES:

1. The chart shows the BCD character that is recorded on tape for the EBCDIC code sent. If an EBCDIC character is assigned, it is shown below the BCD character

2. The characters enclosed within the heavy lines are the standard SDS 62-graphic set

3. During read, only those codes and their appropriate characters that are enclosed in the heavy lines are sent to the I/O system, regardless of the code that was sent by the computer

4. See appendix A in the Sigma computer reference manuals for the functions of the control codes included in this chart

3-71 GLOSSARY OF TERMS

3-72 S and U Chassis Terms

Table 3-12 is a glossary of terms for chassis S and U.

Table 3-12. S and U Chassis Glossary of Terms

Term	Description
.22 sec O/S	Load interlock time delay
.8 sec O/S	Rewind completed delay
01SS	Station state counter in state 1
02SS	Station state counter in state 2
03SS	Station state counter in state 3
06SS	Station state counter in state 6
07SS	Station state counter in state 7
0SCTS	Station state counter in state 0
45SS	Station state counter in state 4 or 5
ACMS	Actuate motor signal
AIOCDS	Acknowledge interrupt signal (from controller)
ALLINT	All transport interlocks closed
ARGC	Address recognized by station (to controller)
ATNS	Attention signal latch
ATOC	HIO operation starting
ATTENTION CONTR	Attention pushbutton pressed
AUTC	Station in automatic mode (to controller)
AUTO	Station in automatic mode
BACKUPS	Return to loadpoint after rewind
BOTH	Beginning of tape signal
BOTH DELAY	Delay prior to setting backups
BOTSD	Addressed station at beginning of tape
BRC	Rewind operation completed
BRR	Ready relay enable signal
BSL	Load cycle – tape now in chambers
BTSC	Beginning of tape signal for TDV (to controller)
CLFS	Interrupt latch clear signal
CLKGS	Transport clock

Table 3-12. S and U Chassis Glossary of Terms (Cont.)

Term	Description
CLKS	Station clock (from controller)
CLOCKS	Write toggle register clock (from data)
DBSC	Device busy signal (to controller)
DBSS	Device busy signal
In the following, n = 0-7, P	
DJAnSD	Deskew jumper A to channel n (to data)
DJAnS	Deskew jumper A to channel n (to data)
DJBnSD	Deskew jumper B to channel n (to data)
DJBnS	Deskew jumper B to channel n (to data)
DJCnSD	Deskew jumper C to channel n (to data)
DJCnS	Deskew jumper C to channel n (to data)
DPRSD	Device proceed signal (to controller)
DPRS	Device proceed signal
DRDC	Device ready signal (to controller)
DRDS	Device ready signal
DSOTH2S	Device select lines 0, 1, and 2 and unit select switch positions 0, 1, and 2 match
DSOTH5S	Device select lines 0-5 and unit select switch positions 0-5 match
DS3TH5S	Device select lines 3-5 and unit select switch positions 3-5 match
DSCS	Device select lines 0-7 and unit select switch positions 0-7 match
DSCDS	Buffered DSCS
DSGC	Device selected signal (to controller)
DSGS	Device selected signal
DSLS	Device selected clock (from controller)

(Continued)

Table 3-12. S and T Chassis Glossary of Terms (Cont.)

Term	Description
DSSS	Device selection gate enable (from controller)
DSTS	Device selection time (from controller)
DVxC	Device select line x (from controller) x = 0-7
DVxDS	Device select line x driver
DVxRS	Device select line x receiver
EDR	Erase head power
ENDC	End operation signal (from controller)
ENDS	End operation signal
ENTC	End of tape signal (to controller)
ENTS	End of tape signal
ERSS	Erase operation in process
FAST	Move capstan at high speed in manual
FAST RONS	Capstan moving at high speed
FASTS	FAST pushbutton pressed when capstan in motion
FSnnS	Station read/write delay counter (nn = 01-12)
FCTS	Station connected to controller
FCTD	Buffered FCTS
F DELAY	Delay interval to allow capstan to stop from high speed
FS1S	Station state counter is in stage 1
FS2S	Station state counter is in stage 2
FS3S	Station state counter is in stage 3
FWD	Move capstan forward in manual
FWDS	Forward button pressed
GNTS	Gate unit address to device address lines if interrupt set
HLTDC	Halt signal being received (from controller)
HLTDS	Halt signal being received
HSPS	Transport is a 150 ips unit
ICRS	Initialize delay counter
INGS	Interval during which interrupt may be set

Table 3-12. S and T Chassis Glossary of Terms (Cont.)

Term	Description
INPC	Interrupt pending during TDV (to controller)
INTB	Interlock B closed (file chamber)
INTC	Interrupt signal set (to controller)
INTS	Interrupt signal set
INTDS	Interrupt signal set, buffered
LATOS	Halt signal being processed
LINGS	Latch interrupt signal
LOAD	Load tape cycle in progress
LOAD INHIBIT	Prevent loading if door not raised
LOAD OFF	Load cycle not in progress
LOADS	Load button pressed
LSPS	Transport is 37.5 ips unit
MAN	Station in manual mode
MANUAL ENABLE	Station in manual and interlocks mode
NORMAL	Move capstan at normal speed in manual
OPERATIONAL CONTR	Station is operational (from transport)
OPRS	Station is operational
OSCLKA	Station clock (in manual mode)
OSCLKB	Station clock (in manual mode)
RASOBOTS	Erase order or at BOT
RASS	Erase order being received
RDAMPxS	Read amplifier output – channel x
RDAMPxSD	Read amplifier output (to data chassis)
READY B	Ready relay energized
RESETFR	Reset FWD and REV manual when START pushed
RESETOS	RESET button pressed
RESETS	RESET button pressed
REV	Move capstan reverse in manual

(Continued)

Table 3-12. S and T Chassis Glossary of Terms (Cont.)

Term	Description
REVS	Move capstan in reverse in automatic
REWI	Rewind indicator signal
REWS	Rewind signal in automatic
ROFS	Rewind off-line order
RSTS	Station reset signal (from controller)
RVRS	Reverse signal (from controller)
RVSS	Reverse operation in progress
SAS	Load cycle, primary safety interval
SASB	Load cycle, secondary safety interval
SELI	Buffered FCTS signal
SELZ	Buffered FCTS signal
STARTS	START button pushed
SWOAx	Write deskew switch A, channel x
SWOBx	Write deskew switch B, channel x
SWOCx	Write deskew switch C, channel x
TBDS	Delay counter has reached BOT delay count
TERS	Delay counter has reached erase delay count
TRDS	Delay counter has reached read delay count
TRVS	Delay counter has reached reverse delay count
TSPS	Delay counter has reached stop delay count
TWRS	Delay counter has reached write delay count
TSHS	TIO, SIO, or HIO operation in progress
WDC1S	Write deskew counter output stage 1 (from data)
WDC2S	Write deskew counter output stage 2 (from data)
WEC3S	Write deskew counter output stage 3 (from data)
WDRx	Write head driver, channel x
WENS	Write enable signal

Table 3-12. S and T Chassis Glossary of Terms (Cont.)

Term	Description
WLRCS	Write longitudinal check character interval
WN1S	Rewind and interrupt order (from controller)
WN2S	Rewind off-line order (from controller)
WNDC	Addressed device is rewinding
WPMC	Addressed device is file protected
WRxS	Write data, channel x (from controller)
WRDE	Write driver toggle register enable
WRTS	Write operation in progress

3-73 Y and Z Chassis Terms

Table 3-13 is a glossary of terms for chassis Y and Z.

Table 3-13. Y and Z Chassis Glossary of Terms

Term	Description
00F	Controller state counter, phase 0
01F	Controller state counter, phase 1
03F	Controller state counter, phase 2
00U	Controller state counter, subphase 0
01U	Controller state counter, subphase 1
02U	Controller state counter, subphase 2
03U	Controller state counter, subphase 3
01F00U	Order input state
01F01U	Order output state
01F02U	Receive and decode order
01F03U	Wait for device proceed (DPR) signal
03F00U	Terminate read/write operation

(Continued)

Table 3-13. Y and Z Chassis Glossary of Terms (Cont.)

Term	Description
ABD	Data enable, read mode, controller to IOP
AIOR	Acknowledge interrupt signal from IOP
AIOC	Acknowledge interrupt signal, miscellaneous logic
AIOM	Acknowledge interrupt signal, miscellaneous logic
AIOCD	Acknowledge interrupt signal, miscellaneous logic
ARG	Address recognized by station
ASCR	Acknowledge service call signal from IOP
ASCM	Acknowledge service call logic, miscellaneous
ASCB	Acknowledge service call logic, miscellaneous
AIO	Initiates HIO operation in controller
AUT	Station in automatic mode (from station)
AVI	Available signal input (from preceding controller)
AVO	Available signal output (to succeeding controller)
AVIR	Available signal receiver (for controller use)
AVOD	Available signal driver (from controller logic)
BAND XX	Miscellaneous logic terms (XX = 01-32)
BOR XX	Miscellaneous logic terms (XX = 02-07)
BFSD	Buffered FSD signal (for status transfer logic)
BMT	Data electronics memory needs service (from data)
BOT	Addressed station at beginning of tape (from station)
BSYC	Controller busy processing an order
BTS	Beginning of tape response signal for TDV (from station)
CFCNX	Clock signal for FCN

Table 3-13. Y and Z Chassis Glossary of Terms (Cont.)

Term	Description
CFCNY	Clock signal for FCN
CFCR	Clock signal for FCR
CFCRX	Clock signal for FCR
CFCRY	Clock signal for FCR
CFF1	Clock signal for FF1
CFF1X	Clock signal for FF1
CFF2	Clock signal for FF2
CFIO	Clock signal for FIO
CFLE	Clock signal for FLE
CFPET5	Clock signal for FPET5
CFRS	Clock signal for FRS
CFRSX	Clock signal for FRS
CFSCM	Clock signal for FSC
CFU1	Clock signal for FU1
CFU1X	Clock signal for FU1
CFU1Y	Clock signal for FU1
CFU1Z	Clock signal for FU1
CFU1ZA	Clock signal for FU1
CFUZ	Clock signal for FUZ
CFUZX	Clock signal for FUZ
CFUZY	Clock signal for FUZ
CFU3	Clock signal for FU3
CFUNX	Clock signal for FUN
CIH	High priority interrupt signal
CIL	Low priority interrupt signal
CLB	Clock signal for FRSD and FRSDD
CLK	General clock signal (from data electronics)
CORE	Correctable read error
CRD	Controller ready for order
CSH	High priority service request
CSL	Low priority service request
CSLI	Service request inhibit (100 nsec delay of NFSC)
CTL	Control order being interpreted

(Continued)

Table 3-13. Y and Z Chassis Glossary of Terms (Cont.)

Term	Description
In the following, n = 0-7, P	
DAn	Data line n to/from IOP and controller
DAnD	Data line n to driver
DAnR	Data line n to receiver
DAnC	Data line n to/from station and controller
DACFD	Device address compares with device in operation
DACFDD	Addressed device to be given halt signal
DAI5	Device number transferring to FR lines
DAI6	Device number transferring to FR lines
DAI7	Device number transferring to FR lines
DATE	Data error signal (from data)
DBS	Device busy signal (from station)
DCA	Controller address recognized
DCA47	Station address recognized
In the following, x = 0-7	
DDAx	Data lines have octal code of x
DFDx	Device in operation is octal x
DOR	Data/order line to/from IOP
DORD	Data/order line driver
DORR	Data/order line receiver
DPR	Device proceed signal (from station)
DPRNWN	Device proceed, not rewind order
DRD	Device ready signal (from station)
DSG	Device selected signal (from station)
DSL	Device selected clock signal (to station)
DSS	Device selection gate enable (to station)
DST	Device selection time (to station)

Table 3-13. Y and Z Chassis Glossary of Terms (Cont.)

Term	Description
DVxC	Device address line (to/from station)
DVxD	Device address line driver input
DVxR	Device address line receiver output
ED	End data line (to/from IOP and controller)
EDB	Less than 4 bytes in data memory at long gap
EDD	End data line driver
EDR	End data line receiver
END	End operation signal to station
ENT	End of tape signal from station
ES	End service line (to/from IOP and controller)
ESR	End service signal
EXTCLK	Clock signal (to PET panel)
EXTRES	Reset signal (to PET panel)
FCD	AIO being processed
FCN	Channel end signal storage
FCR	Set correction signal storage
FD1	Device in operation address – bit 1
FD2	Device in operation address – bit 2
FD3	Device in operation address – bit 3
FF1	Phase counter stage 1
FF2	Phase counter stage 2
FIO	Interrupt signal storage
FLE	Incorrect length error storage
F01	Order code register stage 1 (MSB)
F02	Order code register stage 2
F03	Order code register stage 3
F04	Order code register stage 4
F05	Order code register stage 5 (LSB)

(Continued)

Table 3-13. Y and Z Chassis Glossary of Terms (Cont.)

Term	Description
FPE	Write protect violation occurred
FPET1	PET panel record counter, stage 1 (MSB)
FPET2	PET panel record counter, stage 2
FPET3	PET panel record counter, stage 3
FPET4	PET panel record counter, stage 4
FPET5	PET panel record counter, stage 5 (LSB)
FPET6	PET panel byte counter, stage 6 (MSB)
FPET7	PET panel byte counter, stage 7
FPET8	PET panel byte counter, stage 8 (LSB)
FPETIE	Error insertion signal in PET operations
FRx	Function response line (to IOP)
FRxD	Function response line driver
FRS	Erase order storage
FRSD	Request strobe delay 1
FRSDD	Request strobe delay 2
FS	Function strobe (from IOP)
FSC	Controller connected to IOP for service
FSCC	Controller connected for service
FSCL	Extend RSAR until FSC is reset
FSCM	Controller connected to PET for service
FSD	Function strobe drive
FSL	Function strobe leading signal (to IOP)
FSLD	Function strobe leading signal driver
FSA	Function strobe receiver
FU1	Subphase counter, stage 1
FU2	Subphase counter, stage 2
FU3	Subphase counter, terminal order next
FUN	Unusual end storage

Table 3-13. Y and Z Chassis Glossary of Terms (Cont.)

Term	Description
GBS	Controller now busy
GDA	Gate data lines to device lines during FS
GFD	Gate active device number to device lines except during an FS response
GFI	Gate interrupt latch to highest priority device during AIO
GNT	Gate all interrupting devices to interrupt latch in AIO
GNDXXX	Ground signal
GRDXXX	Ground signal
HIO	HIO signal line (from IOP)
HLTD	Halt signal to be sent to station
HPI	High priority interrupt level
HPS	High priority service level
IC	Interrupt line (to IOP)
ICD	Interrupt line driver
INx	Interrupt latch, station x
INC	Initialize controller signal
INI	Initialize controller signal
INP	Addressed device has interrupt pending
INT	Device interrupt is occurring
IOR	Input/output signal line (to/from IOP)
IORD	Input/output signal line driver
IVO	Invalid order received in controller
LG	Long gap detected by data electronics
LIH	High priority interrupt latch
LIL	Low priority interrupt latch
LIRS	Inhibit new request strobe until disconnected
LSH	High priority service request latch
LSL	Low priority service request latch
MAN	Controller operating from PET

(Continued)

Table 3-13. Y and Z Chassis Glossary of Terms (Cont.)

Term	Description
PC	Check parity on transmitted byte
PETCx	PET counter, stage 0-7
PETCD	PET counter reset
PETCMPA	Strobe pulse to compare data in PET
PETCTR	PET data control signal
PETDA1	PET data control signal
PETDA2	PET data control signal
PETDA3	PET data control signal
PETFB	Write/read a fixed number of records
PETPATA	PET data control signal
PETPATB	PET data control signal
PETPATC	PET data control signal
PETPATD	PET data control signal
PETPATX	PET data control signal
PETRP	Repeat cycle signal from PET
PETST	Start signal from PET
PETWDx	Data signal for comparison in PET
PETWDP	Parity signal from PET
PETWDPA	Parity signal for comparison in PET
RxB	Data line x from data electronics (x = 0-7, P)
RxBA	Data line x to PET (x = 0-7, P)
RASC	Erase signal (to station)
RATE	Rate error signal (from data chassis)
RDP	Read data on line (from data chassis)
READ	Read operation in progress
RES	General reset signal (to data chassis)
RESIN	SIO reset signal to data chassis
REV	Reverse operation in progress
RS	Request strobe line (to IOP)
RSDA	Request strobe line driver
RSA	Request strobe acknowledge line (from IOP)

Table 3-13. Y and Z Chassis Glossary of Terms (Cont.)

Term	Description
RSARC	Request strobe acknowledge line receiver
RSAR	Request strobe acknowledge signal
RSD	Request strobe signal
RSDD	Request strobe signal delayed
RST	Controller reset signal
RVRC	Reverse operation in progress (to station)
RWFIN	Read/write data transmission completed
SC	Service call line (to IOP)
SCD	Service call line driver
SIO	Start input/output line (from IOP)
SIOR	Start input/output line receiver
SPF	Space record forward operation in progress
SPR	Space record reverse operation in progress
SRIP	Memory access request (to data)
SRIPA	Memory access request acknowledge (from data)
SWAx	Address code switch x
TDV	Test device line (from IOP)
TDVR	Test device line receiver
TIO	Test controller line (from IOP)
TIOR	Test controller line receiver
TM	Tape mark has been detected (from data)
TSH	TIO, SIO, or HIO operation in progress
TTSH	TDV, TIO, SIO, or HIO operation in progress
WDC45C	Clock signal from data chassis
WN1	Rewind and interrupt code in order register
WN1C	Rewind and interrupt code to station

(Continued)

Table 3-13. Y and Z Chassis Glossary of Terms (Cont.)

Term	Description
WN2	Rewind off-line code in order register
WN2C	Rewind and interrupt code to station
WN102	Rewind code in order register
WND	Station in rewind
WPM	Station in write protect mode
WRITE	Write operation in progress (to data)
WRT	Write operation in progress
WRTC	Write operation signal (to station)
WTM	Write tape mark operation in progress

3-74 V and W Chassis Terms

Table 3-14 is a glossary of terms for chassis V and W.

Table 3-14. V and W Chassis Glossary of Terms

Term	Description
AC02	Assembly period counter count
AC03	Assembly period counter count
AC04	Assembly period counter count
AC05	Assembly period counter count
AC06	Assembly period counter count
AC07	Assembly period counter count
AC08	Assembly period counter count
AC09	Assembly period counter count
AC10	Assembly period counter count
AC11	Assembly period counter count
AC12	Assembly period counter count
AC13	Assembly period counter count
AC14	Assembly period counter count
AC15	Assembly period counter count
ACVA	Assembly period counter state
ACVB	Assembly period counter state

Table 3-14. V and W Chassis Glossary of Terms (Cont.)

Term	Description
ACVC	Assembly period counter state
ACVD	Assembly period counter state
ACVE	Assembly period counter state
ACVF	Assembly period counter state
ACVG	Assembly period counter state
ACVH	Assembly period counter state
ACVI	Assembly period counter state
ACVJ	Assembly period counter state
ACVK	Assembly period counter state
ACVL	Assembly period counter state
ACVM	Assembly period counter state
ACVN	Assembly period counter state
ACVP	Assembly period counter state
AP01	Assembly period counter, stage 1 (MSB)
AP02	Assembly period counter, stage 2
AP03	Assembly period counter, stage 3
AP04	Assembly period counter, stage 4
AP05	Assembly period counter, stage 5
AP06	Assembly period counter, stage 6
AP07	Assembly period counter, stage 7
AP08	Assembly period counter, stage 8
AP09	Assembly period counter, stage 9
AP10	Assembly period counter, stage 10 (LSB)
APOA	First bit detector for assembly period counter
APOB	Assembly period counter clock enable
APCZ	Assembly period counter reset
ASRO	Assembly register, bit position 0 (MSB)
ASR1	Assembly register, bit position 1

(Continued)

Table 3-14. V and W Chassis Glossary of Terms (Cont.)

Term	Description
ASR2	Assembly register, bit position 2
ASR3	Assembly register, bit position 3
ASR4	Assembly register, bit position 4
ASR5	Assembly register, bit position 5
ASR6	Assembly register, bit position 6 (LSB)
ASRP	Assembly register, bit position parity
BAMP	BCDIC code for ampersand
BBLN	BCDIC code for blank
BDSH	BCDIC code for dash
BMTC	Memory empty signal (to controller)
BOTS	Beginning of tape signal (to controller)
BR00	Buffer register stage 0
BR01	Buffer register stage 1
BR02	Buffer register stage 2
BR03	Buffer register stage 3
BR04	Buffer register stage 4
BR05	Buffer register stage 5
BR06	Buffer register stage 6
BR07	Buffer register stage 7
BR08	Buffer register stage 8
BR09	Buffer register stage 9
BR10	Buffer register stage 10
BR11	Buffer register stage 11
BRAE	Buffer register stages 0-7 erase signal
BRCL	Buffer register shift clock
BRI0	Buffer register stage 0 mark input
BRI1	Buffer register stage 1 mark input
BRI2	Buffer register stage 2 mark input
BRI3	Buffer register stage 3 mark input
BRI4	Buffer register stage 4 mark input
BRI5	Buffer register stage 5 mark input
BRI6	Buffer register stage 6 mark input
BRI7	Buffer register stage 7 mark input
BSLS	BCDIC code for slash

Table 3-14. V and W Chassis Glossary of Terms (Cont.)

Term	Description
BZER	BCDIC code for zero
In following terms, n = 0, 1, 2, 3, 4, 5, P	
CnB1	Channel n bit crowding counter, stage 1
CnB2	Channel n bit crowding counter, stage 2
CnB3	Channel n bit crowding counter, stage 3
CnBC	Channel n bit crowding counter, output
CnCL	Channel n clock signal
CnD1	Channel n deskew counter, stage 1
CnD2	Channel n deskew counter, stage 2
CnD3	Channel n deskew counter, stage 3
CnD4	Channel n deskew counter, stage 4
CnD5	Channel n deskew counter, stage 5
CnDZ	Channel n deskew counter reset
CnJ1	Channel n deskew jumper, stage 1
CnJ2	Channel n deskew jumper, stage 2
CnJ3	Channel n deskew jumper, stage 3
CnP1	Channel n peak detector stage 1
CnP2	Channel n peak detector, stage 2
CnP3	Channel n peak detector, stage 3
CnP4	Channel n peak detector, stage 4
CnP5	Channel n peak detector, stage 5
CnP6	Channel n peak detector, stage 6
CnPQ	Channel n peak qualified signal
CnPT	Channel n peak transfer signal
CHNn	Channel n read amplifier signal
CLKS	Clock signal (to station)
CLOK1	Clock signal
CLOK2	Clock signal
CLOK3	Clock signal
DA0R	Data line bit 0 (from controller)
DA1R	Data line bit 1 (from controller)
DA2R	Data line bit 2 (from controller)
DA3R	Data line bit 3 (from controller)
DA4R	Data line bit 4 (from controller)

(Continued)

Table 3-14. V and W Chassis Glossary of Terms (Cont.)

Term	Description
DA5R	Data line bit 5 (from controller)
DA6R	Data line bit 6 (from controller)
DA7R	Data line bit 7 (from controller)
DATE	Data error (to controller)
DBCD	BCDIC mode of operation
DBIN	Binary mode of operation
DEN2	200 bpi density selected
DEN5	556 bpi density selected
DEN8	800 bpi density selected
DLA1	Delay signal in memory access logic
DAL2	Delay signal in memory access logic
DLAC	Delay signal in memory access logic
DLAP	Delay pulse for memory access
DLBP	Delay pulse for memory access
DLCP	Delay pulse for memory access
DLDP	Delay pulse for memory access
DPAK	Packed mode of operation
DPRS	Device proceed signal (from station to controller)
DWTM	Write tape mark mode of operation
EAMP	EBCDIC code for ampersand
EAP1A	End of assembly period, first clock
EAP1B	End of assembly period, first clock
EAP2	End of assembly period, second clock
EAPA	End of assembly period, first clock - 200 bpi
EAPB	End of assembly period, first clock - 556 bpi
EAPC	End of assembly period, first clock - 800 bpi
EBLN	EBCDIC code for blank
EDBC	End data signal (to controller)
EDSH	EBCDIC code for dash
EZER	EBCDIC code for zero
F096	960 kHz frequency clock signal
F192	1920 kHz frequency clock signal
F384	3840 kHz frequency clock signal

Table 3-14. V and W Chassis Glossary of Terms (Cont.)

Term	Description
F02C	Command register bit 2 (from controller)
FICL	Data finished signal clock (from controller)
FINC	Data finished signal - controller
FINS	Data finished signal (to controller)
H001-H038	Miscellaneous jumpers in data logic
LCR0	Longitudinal check character register, bit 0
LCR1	Longitudinal check character register, bit 1
LCR2	Longitudinal check character register, bit 2
LCR3	Longitudinal check character register, bit 3
LCR4	Longitudinal check character register, bit 4
LCR5	Longitudinal check character register, bit 5
LCRP	Longitudinal check character register, bit P
LCRZ	Longitudinal check register reset
MACL	Memory character counter, stage A clock
MAD0	Memory character address, bit 0
MAD1	Memory character address, bit 1
MAD2	Memory character address, bit 2
MARC	Memory access request - controller
MARS	Memory access request - data
MBCL	Memory character counter, stage B clock
MBTM	Transfer control, buffer register to memory
MC01	One character in memory
MCCA	Memory character counter, stage A
MCCB	Memory character counter, stage B
MCCC	Memory character counter, stage C

(Continued)

Table 3-14. V and W Chassis Glossary of Terms (Cont.)

Term	Description
MCCD	Memory character counter, stage D
MCCL	Memory character counter, stage C clock
MCLK	Memory access cycle enable
MCLM	Mark input to MCLK
MCON	Memory being accessed by controller
MCTM	Transfer control, controller to memory
MDCL	Memory character counter, stage D clock
MFUL	Eight characters in memory
MIN0	Memory input signal, bit 0
MIN1	Memory input signal, bit 1
MIN2	Memory input signal, bit 2
MIN3	Memory input signal, bit 3
MIN4	Memory input signal, bit 4
MIN5	Memory input signal, bit 5
MIN6	Memory input signal, bit 6
MIN7	Memory input signal, bit 7
MMTB	Transfer control, memory to buffer register
MMTC	Transfer control, memory to controller
MOU0	Memory output signal, bit 0
MOU1	Memory output signal, bit 1
MOU2	Memory output signal, bit 2
MOU3	Memory output signal, bit 3
MOU4	Memory output signal, bit 4
MOU5	Memory output signal, bit 5
MOU6	Memory output signal, bit 6
MOU7	Memory output signal, bit 7
MR01	Read memory character address, bit 1
MR02	Read memory character address, bit 2
MR03	Read memory character address, bit 3
MRCL	Read memory character address - clock

Table 3-14. V and W Chassis Glossary of Terms (Cont.)

Term	Description
MSTA	Memory being accessed by data electronics
MW01	Write memory character address, bit 1
MW02	Write memory character address, bit 2
MW03	Write memory character address, bit 3
MWCL	Write memory character address - clock
OPER	Operate mode, read or write, not tape mark
PACL	Parity error register clock
PAR0	Previously assembled character register, bit 0
PAR1	Previously assembled character register, bit 1
PAR2	Previously assembled character register, bit 2
PAR3	Previously assembled character register, bit 3
PAR4	Previously assembled character register, bit 4
PAR5	Previously assembled character register, bit 5
PARP	Previously assembled character register, parity
PARE	Parity error storage register
PCH0	Pack mode character counter, state 0
PCH1	Pack mode character counter, state 1
PCH2	Pack mode character counter, state 2
PEVN	Parity of buffer register bits 2-7 is even
PODD	Parity of buffer register bits 2-7 is odd
RATE	Rate error occurred
RBD0	Deskewed read data output, bit 0
RBD1	Deskewed read data output, bit 1
RBD2	Deskewed read data output, bit 2

(Continued)

Table 3-14. V and W Chassis Glossary of Terms (Cont.)

Term	Description
RBD3	Deskewed read data output, bit 3
RBD4	Deskewed read data output, bit 4
RBD5	Deskewed read data output, bit 5
RBDP	Deskewed read data output, parity
RBDC	First deskewed bit in character has arrived
RCCL	Read character present acknowledge clock
RCHP	Buffer register ready for transfer to memory
RCPA	Buffer register ready signal acknowledge
RCPD	Buffer register ready signal delay
RDOL	Read data on-line (to controller)
READ	Read mode in operation
READE	Read mode signal (from controller)
RES1	General reset signal
RES2	General reset signal
RES4	General reset signal
RESC	General reset signal (from controller)
RESN	SIO reset signal (from controller)
RETM	Reset signal composed of general and SIO reset
RLCC	Longitudinal check character is to be read
RWFIN	Data finished signal (from controller)
RXF1	First character transferred from assembly register
RXF2	Second character transferred from assembly register
SHF1	Pack mode shift counter, stage 1
SHF2	Pack mode shift counter, stage 2
SHGP	Short gap reached
SRIP	Controller wants access to memory
SRPA	Controller access request acknowledge
SRPD	Controller access request delay
TMCH	Assembly register contains tape mark character

Table 3-14. V and W Chassis Glossary of Terms (Cont.)

Term	Description
TMCL	Tape mark detect clock
TMKD	Tape mark has been detected
TMRK	Tape mark signal to controller
V037	Transport in operation is 37.5 ips
V075	Transport in operation is 75 ips
V150	Transport in operation is 150 ips
WBCD	Write BCDIC code characters
WBIN	Write binary code characters
WCCL	Write control logic clock
WCD0	Write data cable driver (to station), bit 0
WCD1	Write data cable driver (to station), bit 1
WCD2	Write data cable driver (to station), bit 2
WCD3	Write data cable driver (to station), bit 3
WCD4	Write data cable driver (to station), bit 4
WCD5	Write data cable driver (to station), bit 5
WCDP	Write data cable driver (to station), parity
WD14	Write deskew counter states 140-147
WD16	Write deskew counter state 163
WDC1	Write deskew counter, stage 1 (MSB)
WDC2	Write deskew counter, stage 2
WDC3	Write deskew counter, stage 3
WDC4	Write deskew counter, stage 4
WDC5	Write deskew counter, stage 5
WDC6	Write deskew counter, stage 6
WDC7	Write deskew counter, stage 7 (LSB)
WDC8	Write deskew counter, stage 8 (556 only)
WDFL	Write deskew counter state 177
WDHF	Write deskew counter state XX7
WDMR	Write deskew counter state 143

(Continued)

Table 3-14. V and W Chassis Glossary of Terms (Cont.)

Term	Description
WDWI	Write deskew counter states 170-177
WENA	Write control logic enable signal
WENB	Write control logic enable follower
WFIN	Last data character to be written
WLCC	Longitudinal check character to be written
WMAR	Memory access request, write mode
WMCL	Memory access request clock
WNTME	Write, not tape mark mode (from controller)
WPAK	Write packed code characters
WRT1	Write mode
WRT2	Write mode
WRITE	Write mode (from controller)
XASR	Transfer assembly register to buffer register
XBCD	Transfer data in BCDIC code to write drivers
XBIN	Transfer data in binary code to write drivers
XLCC	Transfer longitudinal check code to buffer register
XMEM	Transfer memory output character to buffer register
XMI0	Miscellaneous jumper in memory input transfer

Table 3-14. V and W Chassis Glossary of Terms (Cont.)

Term	Description
XMI2	Miscellaneous jumper in memory input transfer
XMI4	Miscellaneous jumper in memory input transfer
XMI6	Miscellaneous jumper in memory input transfer
XPAK	Transfer data in packed code to write driver
XTMC	Transfer tape mark code to buffer register
XWI0	Miscellaneous jumper in write data transfer
XWI1	Miscellaneous jumper in write data transfer
ZARP	Parity of assembly register is odd
ZARW	Parity of assembly register (bits 0, 1, and 2) is odd
ZARY	Parity of assembly register (bits 3, 4, and 5) is odd
ZBAP	Parity of buffer register (bits 0-5) is odd
ZBBP	Parity of buffer register (bits 2-7) is odd
ZBRW	Parity of buffer register (bits 0, 1, and 2) is odd
ZBRX	Parity of buffer register (bits 3, 4, and 5) is odd
ZBRY	Parity of buffer register (bits 2, 6, and 7) is odd

SECTION IV
MAINTENANCE AND PARTS LIST

4-1 INTRODUCTION

This section contains information necessary to check out, maintain, and repair the magnetic tape station and procedures necessary to remove and replace tape station components. Replaceable parts for the assemblies and components used in the tape station are shown in assembly drawings and parts list tables. They are identified by name on the drawings and by part number and circuit designators in the parts list tables.

Power and environmental requirements are given beginning with paragraph 1-23. Table 4-1 lists the special tools and test equipment required to check out, maintain, and repair the station. (Common tools such as pliers, screw drivers, and soldering irons, however, are not listed.) Table 4-2 lists the cleaning agents and lubricants required to maintain and repair the station.

Table 4-1. Tools and Test Equipment

Name	Type
Controller, test	SDS model 7371
Gauge, pressure	0-15 lb/in.^{2} (±2% at 8 lb/in.^{2})
Gauge, thickness	Starrett No. 66
Gauge, vacuum	0-30 in. of water (±2% at 16 in.)
Kit, special tool	SDS model 9298
Fixture, POPO alignment	SDS No. 131157
Tape, master speed	SDS No. 131956
Wrench, POPO adjustment	SDS No. 117569
Module extenders (2)	SDS No. 117037
Module, switch ST28	SDS No. 128254
Multimeter	Triplett No. 630
Oscilloscope	Tektronix model 545 with model CA dual trace preamplifier or equivalent

Table 4-1. Tools and Test Equipment (Cont.)

Name	Type
Overlay, PET	SDS No. 136975
Pliers, C-ring internal (Circlip)	
Power supply	0-40V, 300 mA
Spring scale, 500 grams	Chatillion 16 Eg
Tape, speed test and alignment test	SDS No. 131956-001
Tachometer alignment fixture	SDS No. T802896
Peripheral equipment tester	SDS model 7901

Table 4-2. Cleaning Equipment

Item	Type
Alcohol	Denatured
Head cleaner brush	SDS approved
Tissues	Lint-free

4-2 CABLING

The controller has two sets of cables for attachment to the stations. The cables from the controller to the stations have been kept as short as possible to increase response speed. Table 4-3 lists the station interconnecting cables. Figures 4-1 and 4-2 show the cable interconnections.

4-3 MODULE LOCATION

Figure 4-3 shows the module location for the magnetic tape system.

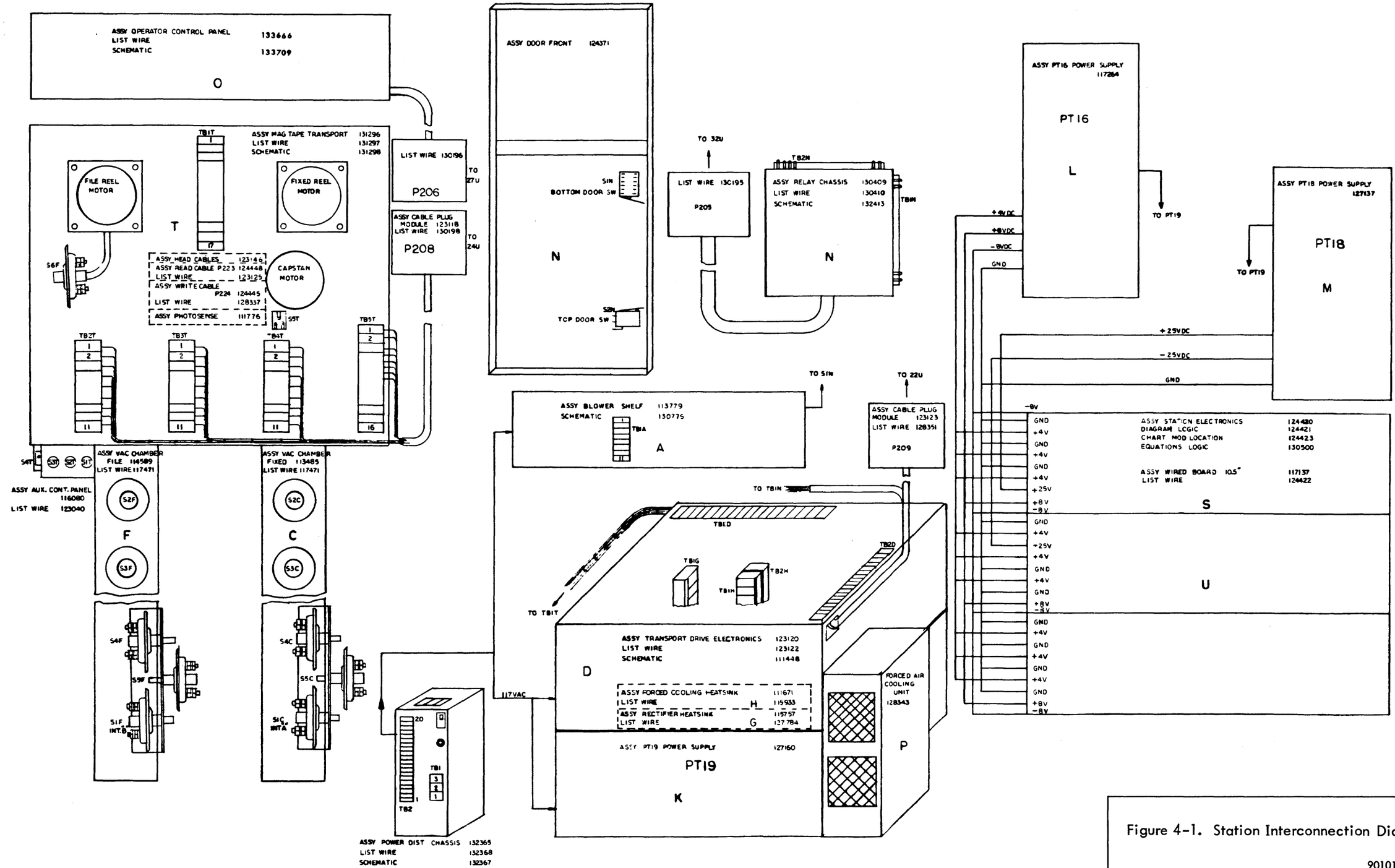
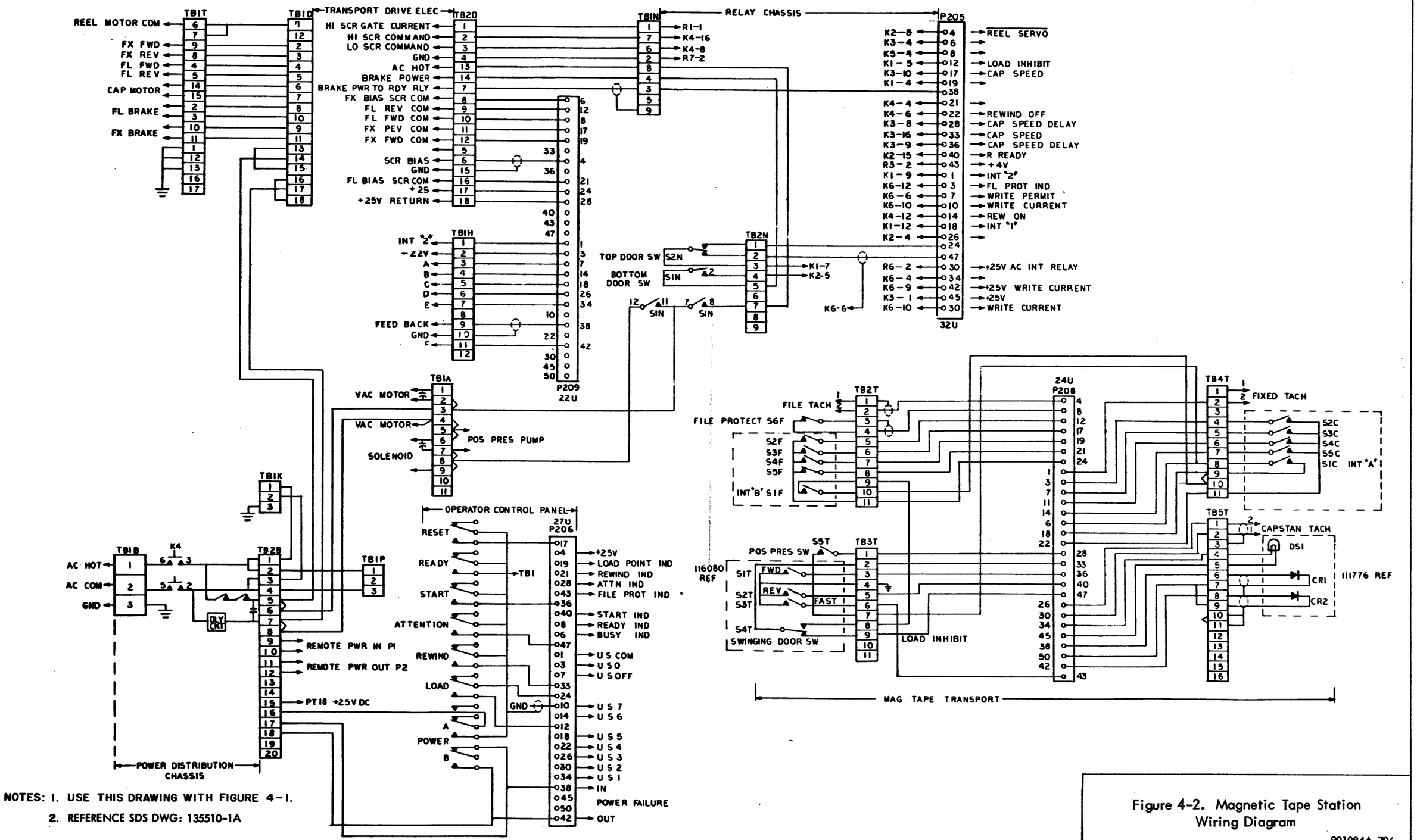


Figure 4-1. Station Interconnection Diagram

901013A. 408



NOTES: 1. USE THIS DRAWING WITH FIGURE 4-1.

2. REFERENCE SDS DWG: 135510-1A

Figure 4-2. Magnetic Tape Station Wiring Diagram

901084A. 706

Table 4-3. Station Interconnecting Cables

Cable	From	To	Function
P205	U32	TBIN in relay chassis	Connects relay chassis to the station electronics
P206	U27	Operator control panel	Provides signal paths between the operator control panel and the station electronics
P208	U24	Station transport casting	Provides signal paths between the station transport casting (TB2-TB5) and the station electronics
P209	U22	Station transport drive electronics	Provides signal paths between the capstan and reel power amplifiers and the station electronics
P223	S2	Read/write head	Provides signal paths between the read head and the station electronics
P224	S27	Read/write head	Provides signal paths between the write head and the station electronics

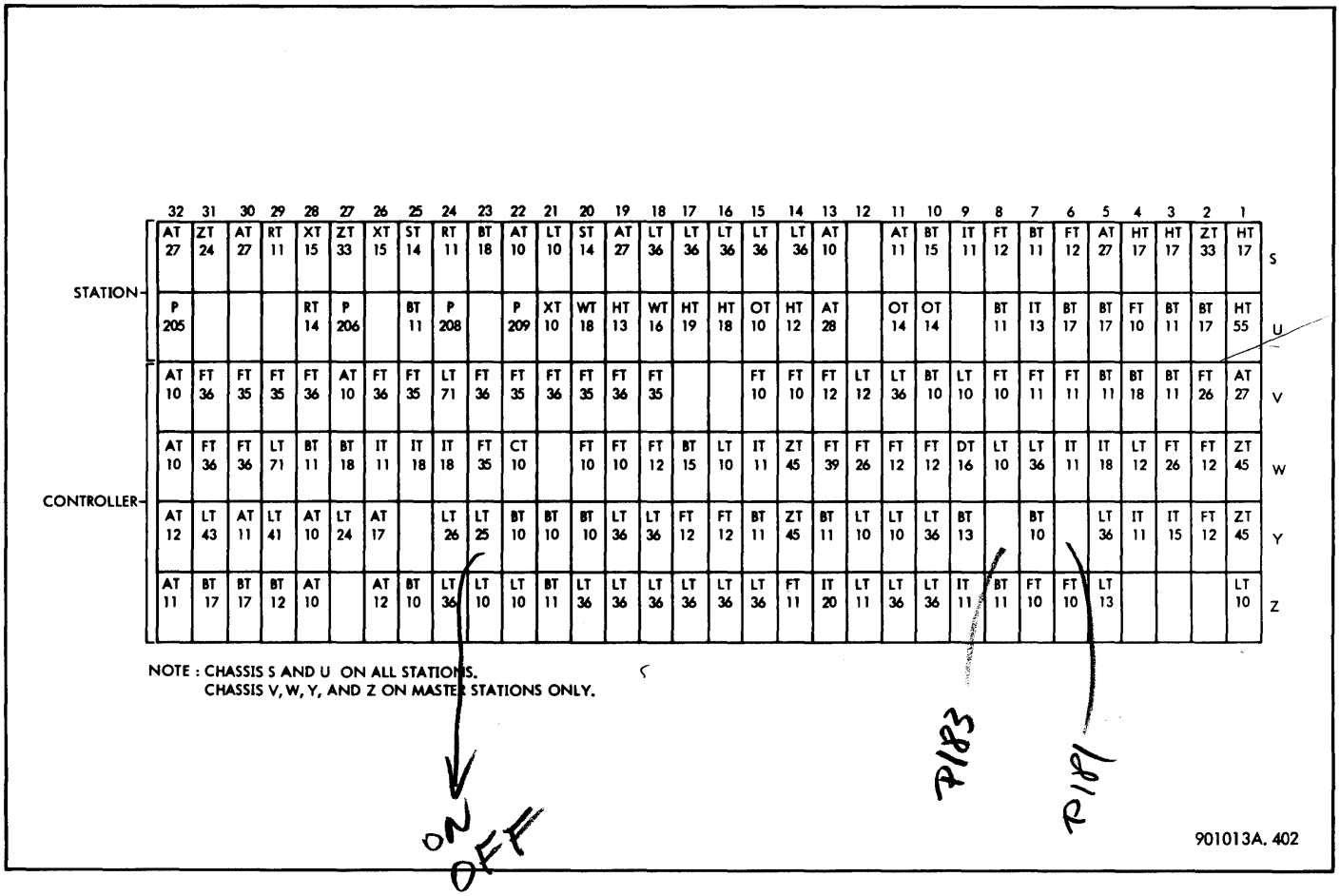


Figure 4-3. Module Location Chart

4-4 PREVENTIVE MAINTENANCE

A program of preventive maintenance is the most effective method of ensuring efficient station operation and reliability. Table 4-4 provides information necessary for visual inspection of the station. Since the need for this inspection is determined by environmental conditions, no absolute checking intervals are specified.

A prescribed maintenance schedule is presented in table 4-5. Since all bearings in the station are prepacked and sealed, no periodic lubrication is necessary.

4-5 CLEANING PROCEDURES

The following cleaning procedures should be performed at the intervals specified in table 4-5 with the cleaning equipment listed in table 4-2.

a. Capstan. Dampen a tissue with alcohol and gently wipe around the rubber surface until all foreign particles and tape oxide are removed. Allow capstan to dry for at least one minute.

b. Tape guides. (See figure 3-8.) Dampen a tissue with alcohol and wipe the body of the guide, making sure that the corner between the guide body and the ceramic cap is completely free of dirt or oxide. Clean the spring loaded washer and make sure that it rests flush on the shoulder of the guide body. Do not remove the ceramic cap on the guide when cleaning.

c. Read/write head. Dampen a tissue with alcohol and clean both heads.

d. Tape cleaner. Dampen a tissue with alcohol and gently wipe the tape cleaner face. Make sure that the tissue is not torn by the cleaning holes, as any lint or tissue fragments may clog the cleaning holes.

e. Vacuum chambers. Open the vacuum chamber doors and clean the corners of the chamber with a brush soaked in alcohol. Soak a tissue in alcohol and clean the chamber bases and the door glass.

f. Reel tachometer pulleys. Dampen a tissue with alcohol and clean the faces and corners of the pulleys.

g. Erase head. Dampen a tissue with alcohol and clean the head.

h. Cabinet. When dusty, the cabinet and transport surface should be wiped with a clean, alcohol-moistened cloth.

Table 4-4. Visual Inspection Information

Item to be Inspected	Inspect For	Corrective Procedure
Power cable	Defective plug pins	Replace plug
	Frayed or damaged cable	Replace cable
Capacitors	Damaged container	Replace capacitor
	Loose terminal connections	Tighten
Resistors	Cracks, charred surface	Replace resistor
	Poor solder connections	Resolder
Transformers	Burned insulation or evidence of overheating	Replace transformer Note Before applying power to new transformer, check the rectifier(s), filter capacitors and choke(s), or resistors. Replace the defective components
	Loose mounting hardware	Tighten
Semiconductors	Loose terminal connections	Resolder connections
Switches	Defective contact; loose toggle	Replace switch

(Continued)

Table 4-4. Visual Inspection Information (Cont.)

Item to be Inspected	Inspect For	Corrective Procedure
Terminal blocks	Loose or broken terminals or wires	Replace terminal block
Terminals (on terminal boards, terminal blocks, transformers, etc.)	Accumulated dirt	Clean with an approved cleaning agent such as trichlorethylene or isopropyl alcohol
	Loose terminals	Tighten
Power supply chassis wiring	Poor soldering	Resolder
	Shorted wiring or potential sources of shorted wiring such as loose screws and bare wire in close proximity to metal chassis	Insulate bare wire where necessary, and tighten loose hardware
Connectors	Bent pins	Straighten
Printed circuit modules	Oxidation film on board terminals	Clean with approved cleaning agent such as trichlorethylene or alcohol
Tape tracking	Tape entry into the chambers from the reel tachometers should be unimpeded	See paragraph 4-38
	Tape guide spring washers, except on the 2 outer guides, should be resting against the inner tape edge. If the washers are pressed and tilted, they may hang up on the guide body, resulting in a loss of tape tracking	
	Note Except on the 2 outer guides, the outer edge of the tape will always be spring loaded against the ceramic tape guide caps. The tape should enter the tape reels without excessive rubbing of the tape edges against the reel flanges. The position of the reels is set during manufacture of the transport, so adjustment should not be required	
Erase head	Erase head should be mounted perpendicular to the tape. Tape should be as close as possible to erase head but should not touch head	See paragraph titled Tape Heads under paragraph 4-8
Relay chassis	All relays should be properly mounted and the ground strap should be properly connected between TB1-9 and chassis	See figure 4-25
Tape creepage or vibration in vacuum chambers	Movement of tape in vacuum chambers	Fixed reel: adjust R34 on U16 for zero volts. Place scope probe on test point U17-23 File reel: adjust R31 on U16 for zero volts. Place scope probe on test point U16-18

(Continued)

Table 4-4. Visual Inspection Information (Cont.)

Item to be Inspected	Inspect For	Corrective Procedure
Tape creepage at capstan motor	Movement of tape at capstan drive	Adjust R30 on U14 for zero volts. Place voltmeter leads on contacts 14 and 15 on TB1T. (Use low range on voltmeter; 10-volt range or lower)
Read/write head	Check for proper slack in the head cable at the connector and head stack. Check the head surface for scratches, imperfections, and dirt	See paragraph titled Tape Heads under paragraph 4-8

Table 4-5. Preventive Maintenance Schedule

ITEM	CLEAN	ADJUST	REPLACE	PARAGRAPH REFERENCE
	Hours of Operation			
Capstan	8			4-5
Tape guides	8			4-5
Read/write head	8			4-5
Erase head	8			4-5
Tape cleaner	8			4-5
Vacuum chambers	8			4-5
Reel tachometer pulleys	8			4-5
Tape tracking		8		4-38
Vacuum system		500		4-11 thru 4-13
Positive pressure system		500		4-15
Holddown knob		500		4-67
Holddown knob rubber ring	500		8,000	4-67
Capstan velocity ramp generator		500*		4-40
Reel servo		2,000		4-26 thru 4-28
Head cover actuator		2,000		4-16
Reel brake friction discs			8,000	4-65
Reel motor brushes			8,000	4-73
Capstan motor		8,000		4-70
Positive pressure pump		8,000		4-72
Reel motor		8,000		4-73
Cabinet	As required			

*Check

4-6 CORRECTIVE MAINTENANCE

4-7 PRELIMINARY CHECKS

In the event of station failure, or if a complete checkout is desired, the following power distribution resistance and voltage checks should be made.

4-8 Resistance Checks

POWER DISTRIBUTION. Resistance checks are made as follows:

a. Turn off all ac and dc power in station.

b. Set the circuit breaker on the power distribution chassis to the ON position and the LOCAL/AUTO switch to the LOCAL position.

c. Use a multimeter (RX1 scale) to check for short circuits between all power bus bars and ground. If shorts exist, the most probable cause is contact pins touching. Visual inspection will usually determine the location of trouble.

d. Measure the resistance between pins 1 and 2 on TB1. The resistance should be infinite. If it is not, check relays K3 and K4 and replace defective parts. (See figures 3-4 and 4-24.)

e. Measure the resistance between terminals 6 and 7 on TB2. The resistance should be approximately 1 ohm. If it is infinite, check the input transformer, and replace it if defective.

f. Measure the resistance between terminals 9 and 10 on TB2. It should be infinite. If it is 470 ohms, relay K2 is defective.

Note

In the following test, CR18 will be in parallel with the meter. Therefore, polarity of the multitester leads is critical.

Measure resistance between terminals 15 and 16 on TB2. The resistance should be 70 ohms. If resistance is more than 77 ohms or less than 63 ohms, replace relays K6 and CR18.

TAPE HEADS. The tape head resistance checks should be made only if tape head difficulties are suspected. Resistance checks of tape heads are made as follows:

CAUTION

The voltage presented to the test leads by the internal multitester battery may be enough to damage the tape head windings. Therefore, use a low voltage ohmmeter, if available.

Erase head resistance is measured at TB1 on the magnetic head cable assembly (figure 4-12), and should be 25 (±1.25) ohms. If out of tolerance, it must be replaced. (See figure 4-16.) For removal and replacement procedure, see paragraph 4-76.

Note

The read and write heads are actually stacks of seven heads, and measurements must be performed on each section of each head. Therefore, if any section of the head is defective, the entire head must be replaced. Pin connections for the head connectors are shown in figure 4-17.

Resistance of the read head coils should be 25 (±1.25) ohms. For removal and replacement procedure, see paragraph 4-74.

4-9 Voltage Check

Station voltages are checked as follows:

a. Connect the ac power to the station.

b. Set the ac distribution chassis circuit breaker to ON, and the LOCAL/AUTO switch to LOCAL.

c. Press the POWER switch on the operator control panel.

d. Measure the voltages at the pins indicated:

Pin	Module Shelf	Voltage
0, 16, 32, 48	S, U	0
50	S, U	-8
51	S, U	+8
49	S, U	+4
45	U	+25
41	U	-25

e. If voltages are more than 10% out of tolerance, readjust the affected power supply.

The contents of this section include step-by-step procedures for adjustment, removal, replacement, and repair of the tape station.

Note

Some of the adjustments in this section require the use of an oscilloscope. The instructions given are intended for use with a Tektronix oscilloscope model 545 with a model CA plug-in preamplifier and X10 probes. When other oscilloscopes are used,

Note (Cont.)

their controls must be set to the same values as those called out for the Tektronix 545. The Tektronix control designations may be different than those of some other makes of equipment; therefore, table 4-6 shows the Tektronix designation followed by the generic term for the function.

Table 4-6. Tektronix Oscilloscope Control Designations

Designation	Generic Term
VOLTS/CM	Vertical sensitivity
TIME/CM	Sweep rate
TRIGGERING MODE	Sync mode
TRIGGER INPUT	Sync input

4-10 MECHANICAL ADJUSTMENTS

4-11 Vacuum Chamber Door Adjustment

The vacuum chamber door is adjusted as follows:

a. Place short tape loops in each vacuum chamber.

b. Connect the vacuum side of the blower directly to the vacuum chamber plenum.

c. Slacken hinge mounting screws on both chamber doors.

d. Apply vacuum to the chambers.

e. Press the chamber doors at various points along their length to ensure that they are seated against the chamber side rails.

f. Tighten the chamber door hinge screws and measure the vacuum in the plenum. The vacuum should measure a minimum of 25 inches of water.

g. Reconnect the vacuum side of the blower to the tee junction and the vacuum line from the junction to the plenum.

4-12 Vacuum Level Adjustment

The vacuum level is adjusted as follows:

a. Disconnect the plastic tube at the nipple mounted on the vacuum chamber plenum closest to the blower side of the cabinet.

b. Connect vacuum gauge to this nipple.

c. Start the station and manually move the tape loops halfway between the four loop sensing switches in each vacuum chamber.

d. Adjust the variable impedance valve mounted at the exhaust outlet of the capstan motor housing. This is done by loosening the locking screw located at one side of the exhaust outlet and by turning the butterfly spindle located on the opposite side. Rotation of the butterfly spindle will result in a vacuum change. Set the vacuum to 16 (±1/2) inches of water.

e. After setting the vacuum, tighten the butterfly spindle locking screw, remove the vacuum gauge, and replace the plastic tubing.

4-13 Vacuum Valve Adjustment

Adjust the vacuum valve as follows:

a. Remove the vacuum valve return spring.

b. Make sure that the solenoid plunger moves freely during several valve operations. If the plunger sticks, adjust the coil position.

c. Replace the return spring.

4-14 Write Enable (File Protect) Switch Adjustment

Adjust the write enable switch as follows:

a. Using a tape reel with a segment removed, check the location of the write enable switch sensing pin. This pin should protrude into the annular cutout in the reel without touching the reel.

b. Using a tape reel with a write enable ring in place, check for correct action of the write enable piston and electrical contact in the vacuum switch.

c. If the write enable switch is incorrectly positioned, adjust it by means of a collet clamp. See paragraph 4-64 for the removal and replacement procedure.

4-15 Positive Pressure Adjustment

Adjust the positive pressure system as follows:

a. Disconnect the plastic tubing to the head cover actuator.

b. Connect the pressure gauge to the plastic tubing just removed.

c. Loosen the locknut on the pressure regulator located on the main casting above the positive pressure pump. See figures 4-12 and 3-7.

d. Start the station, making sure that the tape loops are halfway between four loop sensing switches in each vacuum chamber.

e. Adjust the regulator adjusting screw until the gauge reads 5 (±1/2) lb/in^2.

f. Set the positive pressure interlock switch (located below the capstan motor on the main casting) so that contact is made at 5 lb/in^2. This may be done by connecting continuity tester leads to the switch arm and the unused, normally closed contact. At 5 lb/in^2, the switch should actuate. (Actuation pressure is adjusted by a knurled screw on the switch assembly.)

g. Disconnect the pressure gauge and replace the plastic tube on the head cover actuator.

See paragraph 4-72 for the positive pump removal and replacement procedure. Drain the condensation trap every 500 hours.

4-16 Head Cover Actuator Adjustment

Adjust the head cover actuator as follows:

CAUTION

Turn off the tape station power before making this adjustment.

a. Loosen the locknut on actuator housing assembly at the back of the transport casting.

b. Remove the plastic tube connecting the actuator to the pressure source.

c. Turn the actuator until the head cover is approximately 60° open.

d. Tighten locknut on actuator housing assembly.

e. Reconnect plastic tube connection.

4-17 File Reel Hub Holddown Adjustment

Adjust as follows:

a. Remove reel and cover from hub.

b. With hub in unlocked position (pulled out), place the push-on/pull-off (POPO) alignment fixture on the hub and lock hub.

c. Using the POPO adjustment wrench, adjust each shoe arm one-half turn at a time until the outside of the rubber ring touches the inside of the fixture. Shoe positions should be uniform in relation to the contact point with the rubber ring. Rotate the fixture by hand to determine whether the shoe fit is snug.

d. Remove the fixture and replace the cover.

e. Unlock the hub. Verify uniform positioning of shoes against rubber ring. Place the reel on the hub and lock the hub. Rotate the reel by hand. The hub should rotate with the reel.

f. For removal and replacement procedure, see paragraph 4-67.

4-18 Fixed Reel Check

Check reel wobble and tape entry. If irregularities exist, replace defective parts. See paragraph 4-68 for removal and replacement procedures.

4-19 Reel Motor Drag Torque

Adjust reel motor torque as follows:

a. With reel motor brakes energized, rotate the shaft of each reel motor shaft to check for smooth operation. Drag torque should be uniform with no perceptible irregularities.

b. If tight spots exist, check and readjust the reel motor brake armature gap to 0.010 in. (paragraph 4-66).

See paragraph 4-65 for removal and replacement procedures.

4-20 ELECTRICAL ADJUSTMENTS, TRANSPORT

4-21 Transport Clock Adjustment

The transport clock is adjusted as follows:

a. Ground the following points:

Pin 41 on U8 (DRDS)	Pin 12 on U5 (ROFS)
Pin 38 on U7 (REVS)	Pin 12 on U6 (REWS)
Pin 38 on U8 (ACMS)	

b. With the transport in ready and local modes, use an oscilloscope to observe the waveforms at pin 42 on U11 (OSCLKA). The waveform should be a symmetrical square wave with a 100 μs period. Adjust R3-1 on U11 to obtain 50 μs positive, and R3-2 on U11 to obtain 50 μs off.

4-22 Photosense Lamp Current, BOT and EOT Adjustments

Adjust the BOT and EOT as follows:

a. Remove the wire from TB5T-5 on the transport casting (figure 4-1).

b. Connect a multimeter on the 100 mA range between TB5T-5 and the disconnected wire.

c. Adjust R27 on U20 for 100 (±2) mA reading.

d. Turn off station power. This is imperative.

e. Replace the wire on TB5T-5.

f. Turn on the station power.

g. Adjust R21 on U13 to obtain equal voltage on pins 22 and 23 on U13. The voltage should not be less than 15V or more than 18V.

h. Adjust R20 on U13 to obtain 13V on pin 21 on U13.

i. See paragraph 4-75 for photosense head removal and replacement.

4-23 Capstan Dead Band Adjustment

The following adjustment is to prevent capstan motion when the station is in idle. This adjustment should be made whenever a new HT12 reference generator is installed in U14 or if capstan motion is observed when station is in idle.

a. Remove the tape from the capstan.

b. Place service loops in both vacuum chambers so that the bottom of each loop is positioned between loop sensing switches S3 and S4.

c. Connect a vacuum tube voltmeter between TB1T-14 and TB1T-15 on the transport casting. The voltmeter is now directly across capstan motor.

d. Adjust R30 on U14 so that the voltmeter reads 0 (±0.01) Vdc. The capstan should be motionless.

4-24 Preliminary Capstan Speed Adjustment

Preliminary capstan speed adjustments are made as follows:

a. Connect VTVM to 19 on U15.

b. Press FORWARD on auxiliary control panel and adjust R15 on 14T to read +1.6 (+0.1) V.

c. Press RESET on the operator control panel.

d. Press REVERSE on the auxiliary control panel and adjust R16 on 14T to read -1.6 (±0.1) V.

e. Press RESET on the operator control panel.

For accurate speed and ramp adjustments, see paragraphs 4-39 and 4-40.

4-25 Oscillation Check

Perform the oscillation check as follows:

a. Set the oscilloscope controls as follows:

1. VOLTS/CM to 1.5
2. TIME/CM to 1 MILLI SEC
3. TRIGGERING MODE to INT +
4. AC/DC switch to DC
5. Vertical MODE switch to A ONLY

b. Connect oscilloscope channel A probe to pin 19 on U15, the ramp generator.

c. Press the FORWARD button on the auxiliary control panel to start tape forward motion. Observe the oscilloscope for oscillations. Press the RESET button on the operator control panel to stop tape motion. Press the REVERSE button on the auxiliary control panel to start tape reverse motion. Observe oscilloscope for oscillations. Press RESET on operation control panel to stop tape motion.

d. Repeat step c with the oscilloscope connected to the following pins:

1. Pin 18 on T16 (file reel servo)
2. Pin 23 on T17 (fixed reel servo)

e. Oscillations should not be present in any of the above tests. (Oscillations could be caused by a faulty tachometer, a high resistance ground, or a defective transistor in the transport drive electronics [see figure 4-27]).

4-26 Reel Servo Amplifiers Zero Adjustment

Adjust the reel servo amplifiers as follows:

a. Set the oscilloscope controls as shown below:

1. VOLTS/CM to 0.5
2. TIME/CM to 1 MILLI SEC
3. TRIGGERING MODE to AUTO
4. AC/DC switch to DC
5. Vertical MODE switch to A ONLY

b. Connect the oscilloscope channel A probe to pin 18 on U16.

c. Adjust R31 on U16 for an oscilloscope reading of 0 (±0.2) Vdc.

d. Connect the oscilloscope channel A probe to pin 23 on U17.

e. Adjust R34 on U16 for an oscilloscope reading of 0 (±0.2) Vdc.

4-27 Fixed Reel Servo Amplifier Tape Loop Positioning Adjustment

With the transport in manual mode (press RESET), adjust the tape loop position as follows.

a. Press FAST and FORWARD on the auxiliary control panel to obtain tape fast forward motion.

b. Adjust R15 on U17 so that the tape loop stays between switches S4C and S5C on the fixed reel vacuum chamber. Turning R15 clockwise corrects upward drift, and counterclockwise corrects downward drift.

c. Press RESET on the operator control panel to stop tape motion.

d. Press FAST and REVERSE on the auxiliary control panel or REWIND on the operator control panel to obtain tape fast reverse motion.

e. Adjust R4 on U17 so that the tape loop stays between switches S2C and S3C. Turning R4 clockwise corrects upward drift, and counterclockwise corrects downward drift.

f. If adjustment e disturbs adjustment b, repeat these steps and adjust R4 until drift is about equal but opposite for each direction. Adjust R15 so that tape loop stays steadily between S2C and S4C in reverse direction and between S4C and S5C in forward direction. Repeat the above operations until steady tape loop travel is obtained.

g. Turn R15 on U17 three full turns clockwise.

4-28 File Reel Servo Amplifier Tape Loop Positioning Adjustment

With the transport in manual mode, adjust the tape loop positioning of the file reel servo amplifier as follows:

a. Press FAST and REVERSE on the auxiliary control panel or REWIND on the operator control panel to obtain fast reverse tape motion.

b. Adjust R4 on U16 so that the tape loop stays between switches S4F and S5F on the file reel vacuum chamber. Turning R4 clockwise corrects upward drift, and counterclockwise corrects downward drift.

c. Press RESET on the operator control panel to stop tape motion.

d. Press FAST and FORWARD on the auxiliary control panel to obtain fast forward tape motion.

e. Adjust R16 on U16 so that the tape loop stays between switches S2F and S3F. Turning R16 clockwise corrects upward drift, and counterclockwise corrects downward drift.

f. If adjustment e disturbs adjustment b, repeat these steps and adjust R16 until drift is about equal but opposite in each direction. Repeat the above operations until a steady tape loop is obtained.

g. Turn R4 three full turns clockwise.

4-29 Load One-Shot Adjustment (SAS and 0.22 Sec One-Shots)

SAS. Adjust SAS as follows:

a. Set oscilloscope controls as shown below:

1. VOLTS/CM to 2
2. TIME/CM to 0.5 MILLI SEC
3. TRIGGERING MODE to INT +
4. AC/DC switch to DC
5. Vertical MODE switch to A ONLY

b. Install an empty reel on the file reel hub.

c. Connect oscilloscope channel A probe to pin 8 on U10.

d. Continually press and release the LOAD switch while observing waveforms on the oscilloscope.

e. Adjust R3-3 on U10 for 500 (±10) ms pulse width.

0.22 Sec One-Shot. Adjust the one-shot as follows:

a. Connect the oscilloscope channel A probe to pin 8 on U11.

b. Continually press and release the LOAD switch while observing waveforms on the oscilloscope.

c. Adjust R3-3 on U11 for 200 (±10) ms pulse width.

4-30 Load Function Test

Test the load function as follows:

a. Unload all tape from the machine.

b. Lower the sliding glass window to fully release the reel motor brakes.

c. Load the tape by threading it on the normal path and wind two to four turns on the fixed reel. Make sure that the tape does not get caught on the vacuum chamber edge.

d. Raise the sliding glass window to the fully closed position.

e. Press the LOAD switch and observe the tape movement. The tape should first go into the file vacuum chamber. When the loop reaches the interlock switch, the capstan should start to turn forward, allowing tape to go into the fixed chamber. The tape will continue to move until the BOT mark reaches the photosense heads. At that time the tape will stop.

Note

In case of tape breakage or marker loss, information required for replacement is found in figure 2-3.

4-31 Rewind One-Shot Adjustment (0.8 Sec O-S, Both Delay, Backups, and F Delay)

Adjust the one-shots as follows:

a. Set the oscilloscope controls as follows:

1. VOLTS/CM to 2
2. TIME/CM to 2 MILLI SEC
3. TRIGGERING MODE to EXT +
4. AC/DC switch to DC
5. Vertical MODE to A ONLY

b. Put the station into manual mode by pressing the RESET switch.

c. Connect the oscilloscope channel A probe as shown in table 4-7. Adjust one-shots as shown in the table. The one-shots are triggered each time the station goes from stop to rewind. Proper tape motion for the adjustments may be obtained by using the RESET switch for stop action, and the REWIND switch.

d. The outputs of the one-shots should not have extra spikes at leading or trailing edges.

Table 4-7. Rewind One-Shot Adjustments

One-Shot	Oscilloscope Probe Connection	Adjust	Adjust For
0.8 sec one-shot	Pin 6 on U10	R3-4	800 (±10) ms
BOTH delay	Pin 42 on U10	R3-1	500 (±10) ms
Backups	Pin 29 on U10	R3-2	500 (±50) ms
F delay	Pin 6 on U11	R3-4	350 (±10) ms

4-32 Write Enable (File Protect) Check

Check the write enable system as follows:

a. Load the file reel with the file protect ring installed.

b. Using a multimeter, check for +25V at pins 10 and 50 of U32.

c. Remove the file protect ring from the file reel, reload, and put the station in the ready mode (all interlocks closed).

d. The voltage at pins 10 and 50 on U32 should now be zero.

e. The write enable relay is K6 on relay chassis (figure 4-26).

Turn off the power and remove the jumpers installed in paragraph 4-21, step a.

4-33 ELECTRICAL ADJUSTMENTS, CONTROLLER

This section pertains to units equipped with the model 7371 controller, which consists of module chassis V through Z.

The associated Magnetic Tape Station Model 7372 should be completely checked out and adjusted as delineated in paragraphs 4-7 through 4-32 and 4-37 through 4-54.

Visually inspect the controller as called out in the applicable portions of table 4-3.

4-34 Module Location

Figure 4-3 shows the module location for the controller.

4-35 Clock Oscillator Check

Check out clock oscillator CT10 in slot W22 as follows:

a. Set the controls on the oscilloscope as follows:

1. VOLTS/CM to 1V
2. TIME/CM to .1 μSEC. (After step h, change to 2 μSEC.)
3. TRIGGERING MODE to INT +
4. AC/DC switch to DC
5. Vertical MODE switch to A ONLY

b. Turn station power off.

c. Remove module CT10, insert module ZT10 into slot W22, insert CT10 into ZT10.

d. Turn station power on.

e. Put the oscilloscope channel A probe on test point A on CT10.

f. Adjust L1 for maximum amplitude.

g. Put oscilloscope channel A probe on pin 34.

h. Adjust R16 for a positive pulse duration time of 130 ns. The period of the cycle should be 261 ns.

i. Check signal CLKS at pin 45 of W14. It should have a period of 16.0 μs, the positive portion being 4.0 μs, with a small amount of jitter.

j. Connect a jumper from pin 44 to 48 on W25.

k. The CLKS period should be 16.7 μs with no jitter.

l. Turn station power off.

m. Remove module ZT10 and replace CT10 in W22.

n. Remove jumper on W25.

o. Turn station power on.

4-36 Controller Checkout With IOP

The following test requires that the controller be connected to a Sigma series computer.

Check as follows:

a. Set the toggle switch on LT25 at Y23 to the ON-LINE position.

b. Set up the desired controller address with SWA0 through SWA3 toggle switches on LT26 at Y24. SWA0 in the ON position, and SWA1 through SWA3 in the OFF position correspond to a controller address of X8. The X is the station address, which can be set to 0 through 7 by the UNIT SELECT switch.

c. Test the controller by running the appropriate program shown below.

Computer	Program
Sigma 5 or 7	704026-83* or 704026-84†
Sigma 2	704057-83* or 704051-84†

*On punched paper tape

†On punched cards

4-37 STATION LOGIC ADJUSTMENTS

The following adjustments require that the station be connected to a model 7371 controller, and a Peripheral Equipment Tester (PET) Model 7901 with a front panel overlay No. 135781. Instructions for the connection of these devices are found in paragraph 4-56 and in the instruction manual for this equipment.

4-38 Tape Tracking

Note

Although this test is mechanical in nature, it is important that tracking and alignment be as accurate as possible before the tests that follow this one are performed.

Adjust tape tracking and alignment as follows:

a. Make sure that all tape path elements are clean and free of tape oxide deposits. See paragraph 4-5.

b. Make sure that on all tape guides the spring loaded washer is flush with the shoulder of the guide body.

c. Operate the station in forward and reverse directions. Except for the two outer guides, the edge of the tape should contact the ceramic guide cap at all times.

d. Tape should enter both vacuum chambers without tape edges touching the chamber base or the inside face of the chamber cover.

e. If adjustment is necessary, adjust the position of the reel servo tachometers. See paragraph 4-69.

4-39 Capstan Speed Check and Adjustment

Adjust the capstan speed as follows:

a. An accurate oscilloscope time base setting is mandatory for this procedure. Set oscilloscope controls as follows:

1. VOLTS/CM to 1V
2. TIME/CM to 10 μSEC
3. TRIGGERING MODE to INT -
4. AC/DC switch to DC
5. Vertical MODE to ALTERNATE

b. Connect channel A probe to pin 13 on S13 (CLKS output of CLKS line receiver). Term CLKS is from 60 kHz master clock in the controller.

c. Connect a jumper between pins 44 and 48, slot W25 on the controller. Channel A waveform should go false approximately every 16.7 μs.

d. Adjust TIME/CM VARIABLE so that a negative transition occurs at each centimeter marker.

Note

Do not disturb the TIME/CM VARIABLE setting during the following tests.

e. Load master speed checking tape on station.

f. Connect channel B oscilloscope probe to pin 46 on S1.

g. Press FORWARD switch on auxiliary control panel. A negative-going transition should appear at each centimeter marker. (Instantaneous speed variations cause some jitter. This is normal.) The display on the oscilloscope should be as shown in figure 4-4.

h. If the negative-going transitions do not coincide with the centimeter markers, adjust R16 on U14 until the waveform resembles the one shown in figure 4-4.

k. Press the RESET switch to stop tape motion.

l. Press the REVERSE switch on the auxiliary control panel.

m. Repeat steps i and j, adjusting R15 on U14 for proper waveform placement.

n. Stop tape motion by pressing the RESET button.

Note

Ramp adjustment (paragraph 4-40) must always be performed after capstan speed adjustment.

4-40 Ramp Adjustment for Acceleration and Deceleration

Adjust ramp acceleration and deceleration as follows:

a. Set the oscilloscope controls as follows:

1. VOLTS/CM to .5
2. TIME/CM to 1 MILLI SEC
3. TRIGGERING MODE to EXT +
4. AC/DC switch to DC
5. Vertical MODE to ALTERNATE

b. Connect the oscilloscope probes as follows:

1. Channel A to pin 19 on U15
2. Channel B to pin 46 on S1
3. Trigger input to pin 17 on S8

c. Load the test tape with all ones recorded.

d. Move the tape past the BOT marker.

e. Open the door interlock.

f. Install the jumpers as follows:

1. Pin 17 on S8 (FC01S) to pin 15 on U7 (FWD PB)
2. Pin 25 on S8 (NFC01S) to pin 22 on U7 (RESET PB)
3. Pin 32 on S5 (Ground) to pin 30 on S5 (NOPRNAUTS)

g. Close all interlocks.

h. The tape should move forward for 34 ms and stop for 34 ms. After cycling has started, adjust R4 on U15 to make the channel A waveform reach maximum amplitude 4 ms after the start of the forward ramp. This should cause the channel B waveform to reach maximum amplitude in approximately 5 ms. Ramp adjustment waveforms are illustrated in figure 4-5.

i. Open the door interlock, stopping tape motion.

j. Repeat steps f, g, h, and i, changing jumpers and adjustment potentiometers as follows.

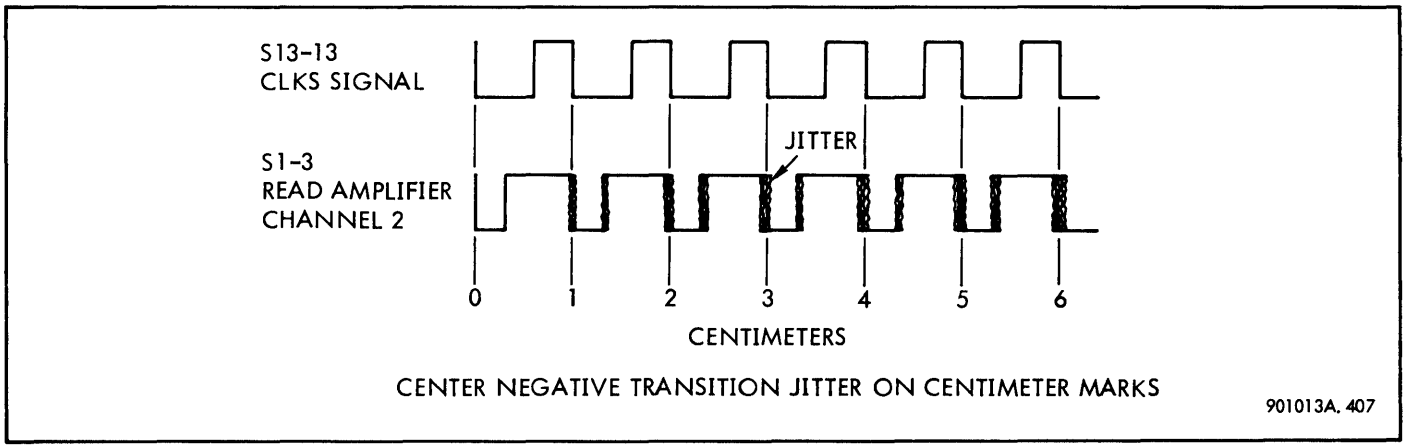


Figure 4-4. Waveforms, Capstan Speed Adjustments

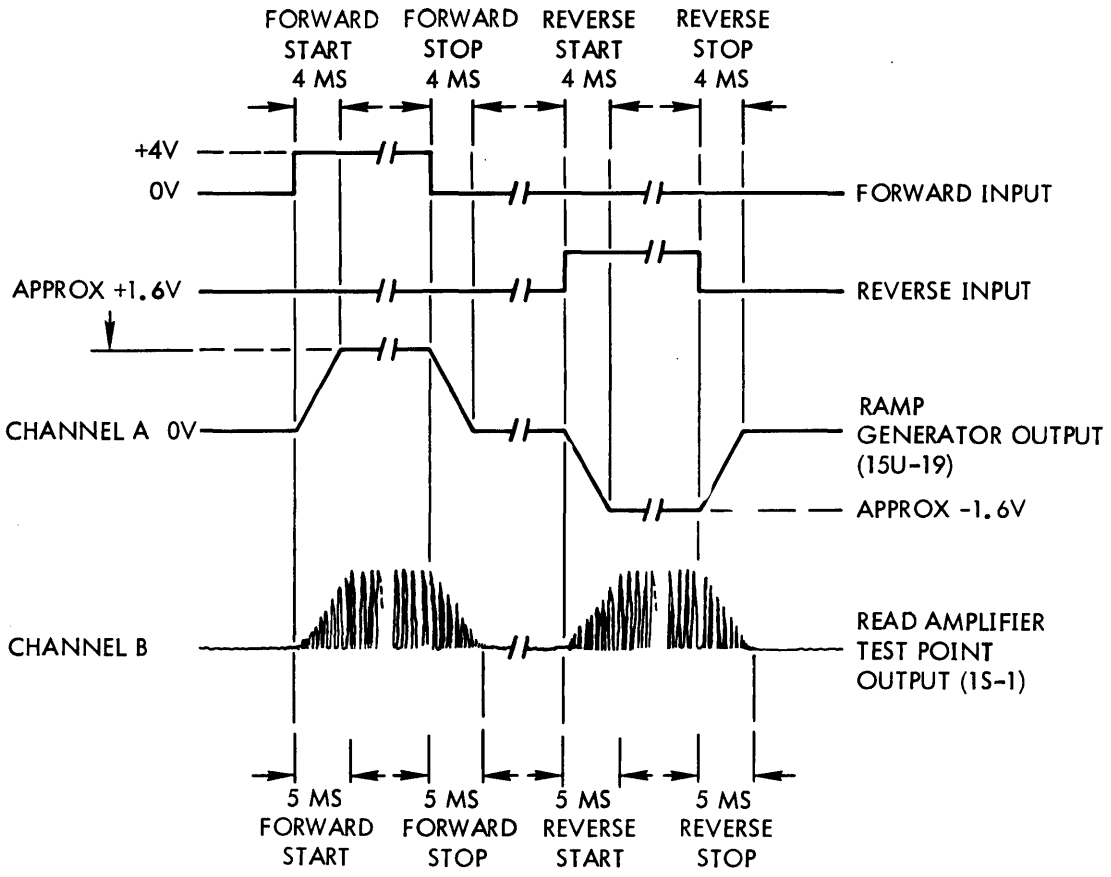


Figure 4-5. Waveforms, Ramp Adjustment

1. Move the jumper end on pin 15 on U7 to pin 7 on U7. Adjust R3 on U15. The tape will move in reverse.

k. Press the RESET switch to stop tape motion.

4-41 Master Clock

The master clock is checked as follows:

a. Set the oscilloscope controls as follows:

1. VOLTS/CM to .2
2. TIME/CM to 5 μSEC
3. TRIGGERING MODE to INT +
4. AC/DC switch to DC
5. Vertical MODE to A ONLY

b. Put the station in manual mode by pressing the RESET switch.

c. Connect the oscilloscope channel A probe to pin 13 on S13.

d. The waveform should be an unsymmetrical square-wave with a period of 16 μs; 4 μs true (+4V) and 12 μs false (0V), with a small amount of jitter.

e. Connect a jumper from pin 44 to pin 48 on W25.

f. The jitter should disappear and the period should increase to 16.7 μs; 4.1 μs true and 12.6 μs false.

g. Remove the jumper on W25.

4-42 Delay Counter

Adjust the delay counter as follows:

a. Put the station in the manual mode by pressing the RESET switch.

b. Set the oscilloscope controls as follows:

1. VOLTS/CM switch to .2
2. TIME/CM switch as required
3. TRIGGERING MODE to INT +
4. AC/DC switch to DC
5. Vertical MODE to A ONLY

c. Connect the oscilloscope to the outputs of each stage and determine that the counter is working correctly. Each stage should have twice the period of the preceding stage. The waveform at pin 17 of S8 should be 68.4 ms. The stages are listed in the order shown in table 4-8.

Table 4-8. Delay Counter Access

STAGE	LOCATION	
	Pin	Module
FC12S	36	S6
FC11S	24	S6
FC10S	27	S6
FC09S	38	S6
FC08S	23	S6
FC07S	11	S6
FC06S	17	S6
FC05S	7	S6
FC04S	24	S8
FC03S	27	S8
FC02S	23	S8
FC01S	17	S8

d. Move the tape to the BOT marker. The delay counter should stop counting.

4-43 Device Ready Latch

Check the device ready latch as follows:

a. Set the oscilloscope controls as in paragraph 4-42, item b.

b. Connect oscilloscope channel A probe to pin 37 on S16 (DRDS).

c. Waveform should indicate true (+4V) condition.

d. Press RESET switch. The waveform should indicate a false (0V) condition as long as the RESET switch is held down.

4-44 Station Address Selection

This test requires the use of the peripheral equipment tester (PET) described in table 4-1, and the oscilloscope controls set as in paragraph 4-42, step b.

Check station address selection as follows:

a. Set the PET controls to write all zeros (paragraph 4-59, step e1).

b. Set the UNIT SELECT switch on the operator control panel to position 0.

c. Set all three DEV ADDR switches on the PET to the down position.

d. Press the START button on the PET. If the address selection logic is operating properly, the station will start writing.

e. Repeat steps b, c, and d, using the switch positions shown in table 4-9.

Table 4-9. Address Selection

Unit Desired	DEV ADDR*
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111
*0 = Down position; 1 = Up position	

4-45 Station Connect

This test requires the use of the peripheral equipment tester described in table 4-1, and the oscilloscope controls set as in paragraph 4-31, item a. Check the station connect as follows:

a. Connect a jumper from pin 37 of S14 to ground.

b. Remove the tape from the capstan.

c. Press the RESET and the START switches.

d. Set the PET controls for the write operation (paragraph 4-59).

e. Connect the oscilloscope TRIGGERING INPUT to pin 37 on S15.

f. Connect the oscilloscope channel A probe to the pins designated in table 4-10, which gives the term to be observed and the expected waveform for each depression of the START button on the PET.

g. Move the tape so that the BOT marker is at the photosense.

h. ERSS at pin 31 on S18 goes true when OSCTS (pin 34 on S7) goes true.

i. Move the tape so that the BOT marker is away from the photosense.

j. Set the PET controls as follows:

1. Read forward (paragraph 4-60)
2. Push START button on PET

WENS at pin 31 on S15 will go true after OSCTS goes true.

k. Set PET control for space reverse (paragraph 4-61).

l. Push START button on PET. RVSS at pin 37 on S17 will go true after OSCTS goes true.

Table 4-10. Station Connect Test

Term	Pin Location	Waveform
DSGS (device select gate)	Pin 37 on slot S15	True for 16.7 to 33.4 μs
DSTS	Pin 40 on slot S13	True for 16.7 to 33.4 μs
DSLS	Pin 42 on slot S13	True for 4.1 μs when DSTS is true
FCTS (connect flip-flop)	Pin 38 on slot S08	True at trailing edge of DSLS
DRDS (device ready)	Pin 37 on slot S16	False when the FCTS flip-flop gets set
OSCTS (state 0)	Pin 34 on slot S07	True for 16.7 μs after the FCTS flip-flop gets set
WRTS	Pin 34 on slot S13	True
WENS (write enable)	Pin 31 on slot S15	Goes true after term OSCTS goes true if the previous order was a read
NRVSS (not reverse)	Pin 33 on slot S17	Goes true after OSCTS goes true if the previous order was a reverse

4-46 Starting Delay Check

This test requires the use of the peripheral equipment tester described in table 4-1, and the oscilloscope controls set as described in paragraph 4-31, item a. Check starting delay as follows:

a. Connect the oscilloscope TRIGGER INPUT probe to pin 34 on S7 (OSCTS).

b. Set the DENSITY switch to 800 bpi.

c. Remove the tape from the capstan.

d. Press the RESET and START switches.

e. Move the tape away from the BOT marker.

f. Set PET controls for write operation (paragraph 4-59).

g. Using the oscilloscope channel A probe, check for the following:

1. The state 6 term, 06SS, at pin 13 on S17 should go true for 6.5 ms.

2. The state 7 term, 07SS, at pin 12 on S7 should go true after term 06SS goes false.

3. If 06SS does not go true, the enables for the tape write delay signal, TWRS, should come true. These enables appear on pin 2 on S7 and pin 27 on S10.

h. Set the PET controls for the read forward operation (paragraph 4-60).

i. Using the oscilloscope channel A probe, check for the following:

1. The state 6 term, 06SS at pin 13 on S17 should go true for 5.5 ms.

2. The state 7 term, 07SS, at pin 12 on S7 should go true after term 06SS goes false.

3. If 06SS does not go true, the enables for the tape read delay signal, TRDS, should come true. These enables appear on pin 45 on S7 and pin 14 on S10.

j. Set the PET controls as for the space reverse operation (paragraph 4-61).

k. Using the oscilloscope channel A probe, check that the state 7 term, 07SS, on pin 12 of S7 goes true after OSCTS, pin 34 on S7, goes false.

l. Connect jumper pin 30 on S18 (NERSS) to ground.

m. Set the PET controls for the write operation (paragraph 4-59).

n. Using the oscilloscope channel A probe, check for the following:

1. The state 6 term, 06SS, on pin 13 on S17 should go true for 51 ms.

2. If 06SS does not go true, the enables (TERS) at pin 13 on S7 and pin 46 on S10 should come true.

o. Set the PET controls for read forward operation (paragraph 4-60).

p. Using the oscilloscope channel A probe, check that the state 6 term 06SS at pin 13 on S17 goes true for 29.3 ms. If 06SS does not go true, check that the enable (TBDS) at pin 34 on S14 goes true.

q. Remove the ground jumpers at pin 37 on S14 and pin 30 on S18.

4-47 Read/Write Amplifiers

Using the PET and the oscilloscope, the read/write amplifiers are checked as follows:

a. Connect jumper pin 15 on Y8 (PET CD) to ground. This writes a continuous record without gaps.

b. Set the DENSITY switch to 800 bpi.

c. Put the tape on the capstan.

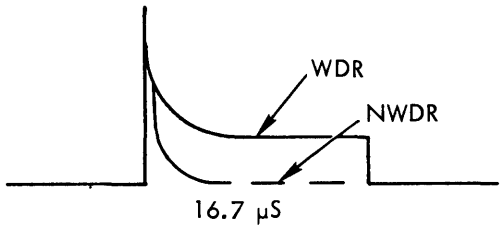
d. Close all interlocks and press the RESET and START switches.

e. Set the PET controls for write operation with ones in all channels (paragraph 4-59, step e-2).

f. Using the oscilloscope, check for the output at each channel. Refer to table 4-11.

g. While observing the oscilloscope pattern for each channel, switch the PATTERN CTR switch for that channel from ONE to ZERO and back repeatedly. The read amplifier output should change from one to zero with the switch action.

h. If there is no output at the read amplifier, check the write driver output signals (WDR and NWDR). Pin locations for these terms are shown in table 4-11. The desired waveforms for WDR and NWDR are shown below:



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i. Remove the jumper from pin 15 of Y8 to ground.

Table 4-11. Read and Write Amplifier Access Pins

CHANNEL	READ AMPLIFIER			WRITE DRIVER			THRESHOLD OUTPUT SLOT U1 PIN
	Module	Out Pin	TP Pin	Module	WRD Pin	NWRD Pin	
0	S3	3	1	S24	6	5	8
1	S3	8	17	S24	4	1	11
2	S1	46	39	S24	2	3	15
3	S1	3	1	S24	10	9	18
4	S1	8	17	S29	6	5	20
5	S3	46	39	S29	4	1	23
P	S4	46	39	S29	10	9	4

4-48 Threshold Adjustment For Read Amplifiers

Using the PET and the oscilloscope, the threshold level of the read amplifiers should be adjusted while writing a long record pattern of 100010001000... on a new tape. The threshold level is adjusted as follows:

a. Set the following PET switches to the ON position: PATA, PATB, all RECORD LENGTH, and PET ON.

b. Adjust each of the threshold potentiometers for an output voltage of -5.5V. The potentiometers are located in slot U1, and are arranged vertically with the parity channel on top, followed by channels 0, 1, 2, 3, 4, and 5. (See table 4-11.)

c. Set the oscilloscope controls as follows:

1. Change the vertical input probes to X1
2. VOLTS/CM to .5
3. TIME/CM to 5 μ SEC
4. TRIGGERING INPUT to EXT +
5. AC/DC switch to DC
6. Dual trace MODE to A ONLY
7. Connect TRIGGER INPUT probe to channel A input

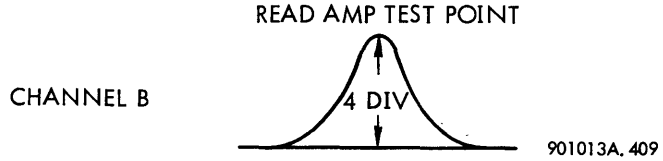
d. Connect the oscilloscope channel A probe to the read amplifier output (table 4-11) for the channel under observation.

e. Press the START switch on the PET.

f. The duration of the output signal should be 25 to 28 μs.

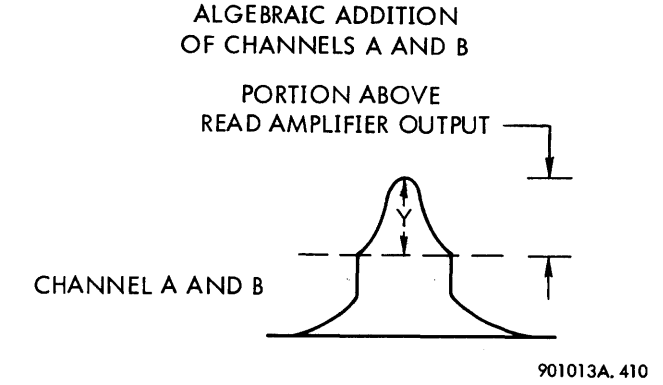
g. Set the oscilloscope dual trace mode to B ONLY.

h. Connect the oscilloscope channel B probe to the read amplifier test point (table 4-11) for the channel under adjustment. Signal amplitude should be approximately 1.9V. Adjust the VOLTS/CM VARIABLE control so that the waveform is four divisions high, as shown below.



i. Set the oscilloscope dual trace MODE to ADDED ALGEBRAICALLY.

j. Adjust the threshold potentiometer (table 4-11) until the pattern shown below is attained. Then set the threshold for 25%.



k. Repeat steps d through j for all channels except parity.

l. Set PET switches CTR and any one of the PATTERN CTR's to the up position to record the same pattern in the parity channel.

m. Adjust the parity channel using steps d through j.

4-49 Deskew Adjustment

The deskew adjustments are made in three consecutive steps:

a. Forward read deskew, using the speed test alignment tape (paragraph 4-50).

b. Reverse read deskew, using the speed test alignment tape (paragraph 4-51).

c. Write deskew, while writing on blank tape (paragraph 4-52).

4-50 Forward Read Deskew

Make the forward read deskew adjustment as follows:

a. Make sure that the read/write head and all tape guides are clean.

b. Remove the jumper module ZT24 from slot S31.

c. On a ST28 switch module, set all switches marked SW0A through SWPA, and SW0B through SW8B to 0 (open). Set all switches marked SW0C through SW8C to S (short). Insert module ST28 into slot S31.

Note

The above setting for each channel corresponds to a deskew count of 4. The 4 is expressed in binary. The deskew count of 4 is the center of the adjustment range. For channels that are late, an early deskew count is required (from 1 to 3). For channels that are early, a late deskew is required (from 5 to 7). A deskew setting of 0 (zero) must not be used. If the channels cannot be deskewed within the range of 1 to 7 (1.8 μs), the read/write head is not mounted properly.

d. Mount the master speed alignment tape.

CAUTION

The FILE PROTECT indicator on the operator control panel must light when the station becomes ready (all interlocks closed).

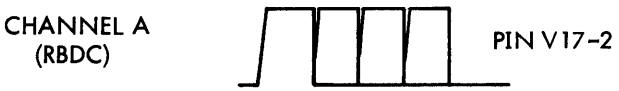
e. Set the PET controls for a read forward operation (paragraph 4-60).

f. Set the oscilloscope controls as follows:

1. VOLTS/CM to .5
2. TIME/CM to .5 μSEC
3. TRIGGERING MODE to EXT +
4. AC/DC switch to DC
5. Vertical MODE to CHOPPED

g. Connect the oscilloscope channel A probe and the TRIGGER INPUT probe to pin 2 on W19 (read bit deskew common).

h. Adjust the oscilloscope triggering controls so that the first pulse does not have a trace at the ground line as shown below. If more than five pulses appear, check head alignment and the tape guide position.



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i. Connect the oscilloscope channel B probe to pin 15 on V15 (read bit deskew 0). Observe the waveform, and compare the timing with channel A. Increase or decrease the deskew count (using the ST28 switches) until it is as close to the time of the channel A waveform as possible.

j. Repeat step i for channels 1 through p, using table 4-12.

Table 4-12. Deskew Access Pins

Read Bit Deskew Channel Out	Slot V16 Pin
RBD 0	01
RBD 1	03
RBD 2	05
RBD 3	07
RBD 4	09
RBD 5	11
RBD P	13

k. After all channels have been adjusted, look at the switch settings on ST28. If the settings are all to one side of 4, add or subtract an equal count from each channel to move them closer to 4.

l. Repeat steps i, j, and k until the total skew cannot be further reduced.

m. Transfer the switch settings established on the ST28 switch module to the ZT24 jumper module. This is done by cutting out the forward jumper (identified by an F) that corresponds with each switch in the 0 position.

n. Insert ZT24 module into slot S31. Read the skew (steps i and j) to ensure that the switch settings have been properly transferred to the jumper module. If the skew does not agree with the previous reading, recheck the switches and jumpers.

4-51 Reverse Read Deskew

Make reverse read deskew adjustments as follows:

a. Repeat paragraph 4-50 steps a through d.

b. Set the PET controls for the space reverse operation (paragraph 4-61).

c. Repeat paragraph 4-50 steps f through l. The total skew must not exceed five pulses or 2.6 μs.

d. Transfer the switch settings established on the ST28 switch module to the ZT24 jumper module. This is done by cutting out the reverse jumper (identified by an R) that corresponds with each switch in the 0 position.

e. Repeat paragraph 4-50 step n.

4-52 Write Deskew

Make write deskew adjustments as follows:

a. Put ST14 modules at slots S20 and S25 on extender cards and reinsert them into slots.

b. Set a binary count of 4 on each set switch. This is done by setting all SW0A and SW0B switches to 0 and all SW0C switches to 1. Switch locations are determined from table 4-13.

Table 4-13. Write Deskew Switches

WRITE CHANNEL	MODULE LOCATION	SWITCH NUMBERS		
		S1-SW0A (lsb)	S1-SW0B	S1-SW0C (msb)
0	S25	5	10	15
1	S25	4	9	14
2	S25	3	8	13
3	S25	2	7	12
4	S20	5	10	15
5	S20	4	9	14
P	S20	1	6	11

c. Load a new blank tape on the station.

d. Set the PET controls to write binary, all ones in all channels. Make sure the REV switch is off. (See paragraph 4-59, step e2.)

e. While writing on tape, repeat paragraph 4-50 steps f through l (forward read deskew) adjusting the ST14 modules instead of the ST28. The total skew must not exceed five pulses, or 2.6 μs.

f. Remove extender cards from the ST14 modules and reinsert them in slots S20 and S25. It is very important that the modules not be reversed, and that the switch settings not be disturbed.

g. Set the PET controls to write 16 long records with ones in all channels and to reverse space the record just written. With switch RP on, the tape will move forward and reverse. Check reverse read skew (paragraph 4-51) against read after write skew (paragraph 4-52) for each channel. The difference should be no more than one pulse (0.52 μs).

4-53 Ending Delay Check

The ending delay check is made as follows:

a. Close all interlocks, and press the START switch.

b. Set the oscilloscope controls as in paragraph 4-48, step c.

c. Set the PET controls for the write operation (paragraph 4-59).

Switches FB and RP should be OFF.

Note

Table 4-14 lists logic terms and their locations. These terms are referred to in this check procedure.

Table 4-14. Ending Delay Logic Terms

Term	Pin	Module
ENDS	13	S11
OSCTS	34	S7
TSPS	35	S7
	15	S10
TRVS	46	S7
	28	S10
02SS	14	S7
03SS	33	S7
06SS	13	S17

d. Connect the TRIGGER INPUT of the oscilloscope to ENDS.

e. Using the channel A probe of the oscilloscope, do the following:

1. Check that ENDS goes true for 16.7 to 33.4 μs after the write operation starts.

2. Connect a jumper from pin 47 on S18 to ground.

3. Check that 03SS goes true not later than 16.7 μs after ENDS and that it remains true for 5.3 ms. If 03SS does not go true, check TSPS.

4. After 03SS goes false, OSCTS goes true for 16.7 μs.

5. Remove the jumper from pin 47 of S18.

6. Check that 03SS goes true for 67 μs.

7. After 03SS goes false, check that OSCTS goes true for 16.7 μs.

Note

The TSPS delay will be short if a new order is issued by the controller and the new order is for tape motion in the same direction. If reversal of direction is ordered, 03SS will remain true for 5.3 ms.

f. Set the PET controls for space reverse operation. Using the oscilloscope, do the following:

1. Check that 06SS goes true not later than 16.7 μs after ENDS and remains true for 1.9 ms. If 06SS does not go true, check TRVS.

2. Connect a jumper from pin 13 on S8 to pin 23 on S15. Read reverse will not run continuously. Press the START button for a new order.

3. After 06SS goes false, check that 02SS goes true for 5.3 ms.

4. Remove the jumper in step 2.

5. Check that 02SS goes true for 50 μs.

6. After 02SS goes false, check that OSCTS goes true for 16.7 μs.

4-54 Operator Control Panel Indicator Check

The following operator control panel indicators should light under the conditions indicated (see figures 4-22 and 4-23):

a. POWER. When primary power is applied to station.

b. LOAD. When the BOT tab is over the photosense head.

c. REWIND. When the transport is rewinding.

d. ATTENTION. When the indicator is pressed and the machine is in the manual mode and operating.

e. FILE PROTECT. When the file protect ring is absent.

f. AUTO. When the station is in the automatic mode. (The AUTO indicator illuminates the START button.)

g. BUSY. When the station is in the automatic mode, and the controller is using the machine.

h. READY. When all power is on, all power supplies are functioning, vacuum and pressure pumps are operating, tape is properly loaded, and all interlocks are closed. Pressing the READY indicator activates a lamp test switch, which lights the lamps in all of the indicators except RESET and POWER. (The RESET switch has no lamp.)

4-55 PERIPHERAL EQUIPMENT TESTER OPERATION

The Peripheral Equipment Tester (PET) Model 7901 is used with the tape system, as described in paragraphs 4-56 through 4-61.

4-56 Preparation and Connection

To perform the tests described in this section, connect the PET to the controller as follows:

a. Connect the power plug to 115 Vac single phase. Make sure that the POWER switch is OFF.

b. Connect the P180-P181 cable from the PET to controller slot Y6.

c. Connect the P182-P183 cable from the PET to controller slot Y8.

Note

If the PET is a portable unit, P180 and P182 plug in wiring side up. If the PET is a rack mounted unit, P180 and P182 plug in wiring side down.

Check PET connection and voltages as follows:

a. Turn on power to the PET and tape system.

b. Check the logic supply voltages in the PET and the tape system. Settings in the shaded area monitor the voltages generated in the PET, while the rest of the settings monitor the voltages in the controller. Be sure all voltages are normal at this time. There should be no indication in positions TV01 and TV02.

CAUTION

Do not use the PET voltmeter to adjust any power supplies.

4-57 Overlay

Figure 4-6 is a full-size drawing of the magnetic tape No. 12 overlay. This overlay should be used for the tests in this manual. In the event that the overlay is unavailable, figure 4-6 may be removed from this book and used for the overlay.

4-58 On-Line/Off-Line Switch

The on-line/off-line switch on the LT25 module located in slot Y23 must be placed in the OFF-LINE position for the PET to operate. 4-58a) US in AUT

4-59 Write Operation

The write operation is set up on the PET as follows:

a. Set the PET ON-OFF/RESET switch to the OFF/RESET position.

b. Select the desired station with the DEV ADDR switches.

c. Set the command switches to 00101. (X 05)

d. Select the number of bytes per record using the RECORD LENGTH switches. All switches in the off (down) position will cause eight bytes per record to be written, switch 2^0 will cause 16 bytes to be written, and so forth.

e. Select the data pattern as follows:

1. All zero pattern. Place all PATTERN CTR switches in the ZERO position. Place CTR and all DATA PATTERN switches in off (down) position.

2. All one pattern. Place all PATTERN CTR switches in the ONE position. Place CTR and all DATA PATTERN switches in the off position.

3. Binary pattern. Data for each channel will correspond to the counter output. Place all PATTERN CTR switches in the COUNT position. Place CTR switch and RECORD LENGTH 2^7 switches in the on (up) position. Set all DATA PATTERN switches to the off position.

4. Patterns A through D. The combination of DATA PATTERN switches will determine the data pattern for each channel, with parity generated automatically. The switch positions for the available pattern are shown in table 4-15. Place CTR in off position, and all PATTERN CTR switches to ZERO.

f. Select the mode of operation from table 4-16.

g. If monitoring of data channels is desired, patch from the desired monitor jack (BFR0 to BFR7) to either AUX 1 or AUX 2. Place LATCH/ONE-SHOT in the up position. (See table 4-17.)

h. To stop the operation, momentarily move PET ON-OFF/RESET to the OFF/RESET position.

4-60 Read Forward Operation

The read forward operation is set up on the PET as follows:

a. Set the PET ON-OFF/RESET switch to OFF/RESET.

b. Set the COMMAND switches to the ~~01100 (X 0C)~~ position. 00110 (X 06)

c. Select the mode of operation from table 4-16.

d. Move the PET ON-OFF/RESET switch to the ON position.

e. Press and release the START pushbutton to initiate an operation.

f. To stop the operation, momentarily move the PET ON-OFF/RESET switch to OFF/RESET.

4-61 Space Reverse Operation

The space reverse operation is set up on the PET as follows:

a. Set the PET ON-OFF/RESET switch to OFF/RESET.

b. Set the COMMAND switches to the 11100 (X 1C) position.

c. Select the mode of operation from table 4-16.

d. Move the PET ON-OFF/RESET switch to ON.

e. Press and release the START pushbutton to begin operation.

f. To stop the operation, momentarily move the PET ON-OFF/RESET switch to the PET ON position.

4-62 REMOVAL AND REPLACEMENT PROCEDURES

Paragraphs 4-63 through 4-76 give step-by-step instructions for removing and replacing the major components of the magnetic tape transport.

4-63 Tape Guide Removal and Replacement (See figure 3-8

The following should be done for removing and replacing the tape guides:

a. Remove the screw securing the ceramic cap.

b. Remove the O-ring inside the ceramic cap and examine for damage. If damaged, replace.

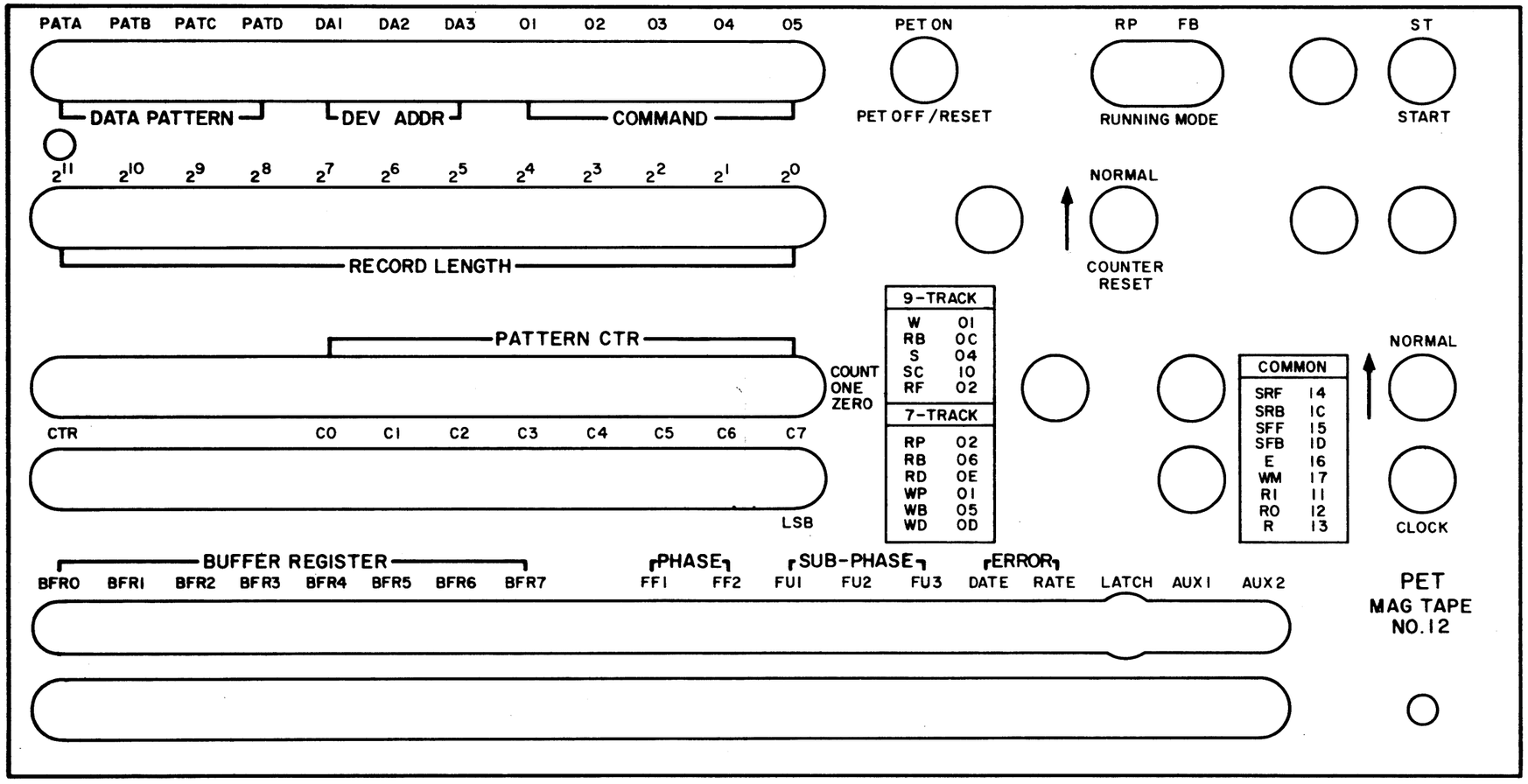


Figure 4-6. PET Magnetic Tape Overlay No. 12

901013A.401

c. Remove the special screw inside the air guide housing.

d. Remove the housing, spring, and washer.

e. Carefully examine the washer for wear. If there are signs of the tape edge having cut into the washer, replace the washer.

f. Clean all parts thoroughly with alcohol.

g. When reassembling the tape guide, ensure that the radiused edge of the washer is adjacent to the guide housing shoulder.

Table 4-15. PET Data Patterns

SWITCH UP	BYTE NUMBER															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
PATA	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
PATB	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
PATA & PATB	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
PATC	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
PATD	0	1	0	1	1	0	1	0	0	1	0	1	1	0	1	0

Table 4-16. PET Functions

Overlay Designation	Panel Designation	Function
COMMAND 01 02 03 04 05	DATA CONTROL 7 8 9 10 11	Functions indicated on PET overlay and the chart below Abbreviation — Command — Hexidecimal Representation — Switch Position* RP — Read packed — 02 — 00010 RB — Read binary — 06 — ~~0C~~ — ~~01100~~ 00110 RD — Read BCD — 0E — 01110 WP — Write packed — 01 — 00001 WB — Write binary — 05 — 00101 WD — Write BCD — 0D — 01101 SRF — Space record forward — 14 — 10100 SRB — Space record backward — 1C — 11100 SFF — Space file forward — 15 — 10101 SFB — Space file backward — 1D — 11101 E — Set erase — 16 — 10110 WM — Write tape mark — 17 — 10111 RI — Rewind and interrupt — 11 — 10001 RO — Rewind off-line — 12 — 10010 R — Rewind on-line — 13 — 10011 *1 = up; 0 = down
CTR	COUNTER OUTPUT 0	Must be in up position for PATTERN CTR switches to be effective. If CTR is in down position, data pattern is controlled by DATA PATTERN switches
DEV ADDR DA1 DA2 DA3	DATA CONTROL 4 5 6	Selects station address. DA1 is most significant switch, and DA3 is least significant switch. Station address is selected by the binary setting of the DEV ADDR switches and the UNIT SELECT switch on the station operator control panel
DATA PATTERN PATA PATB PATC PATD	DATA CONTROL 0 1 2 3	Determines data patterns for all station channels. See table 4-15 for switch combinations

(Continued)

Table 4-16. PET Functions (Cont.)

Overlay Designation	Panel Designation	Function
PATTERN CTR C0 C1 C2 C3 C4 C5 C6 C7	COUNTER OUTPUT 4 5 6 7 8 9 10 11	Determines data for channels 0-7. If switch setting is ONE or ZERO, sets up data. If switch setting is COUNT, data to channel corresponds to counter output
RECORD LENGTH 2^{11} 2^{0}	COUNTER RESET 0 11	Determines record length for a write operation. Switch 2^0 is the most significant, and switch 2^{11} the least significant switch. With all switches UP, 8 bytes are written on tape. Write count can be incremented in multiples of 8 bytes. In the packed mode, 4 characters on tape are equivalent to 3 bytes from the PET/IOP
PET ON-PET OFF/ RESET	SELECTOR	In OFF position, resets controller. In ON position, enables PET operations
RUNNING MODE RP FB	DEBOUNCED 1 2	Controls tape motion as follows: RP ON, FB OFF. Continuous mode. Selected operation is repeated until RP is turned OFF or tape runs out. Tape will not stop at EOT marker RP OFF, FB ON. Single cycle mode. Selected operation is repeated 16 times, tape spaces backward 16 times, and unit returns to idle state RP ON, FB ON. Continuous cycle mode. Same as single cycle mode except unit repeats operation continuously rather than going into idle state RP OFF, FB OFF. Single order mode. One operation is executed and unit returns to idle state
ST/START	3	Initiates selected operation. Operation is started when switch is released
NORMAL/COUNTER RESET	RESET DEV/INT	Connects device reset signal to 12-stage binary counter. Must always be in UP position
NORMAL CLOCK	COUNTER CLOCK DEV/INT	Allows device clock to increment counter in PET. Must always be in UP position

Table 4-17. Overlay Indicators

Overlay	PET	Description
DATE	14	Data error. A data parity error may consist of a lateral or longitudinal parity error in both read and read after write, or of a cyclic redundancy check mismatch error during reading
FF1	9	Major phase determinate. It is used in conjunction with FF2 to determine major phase of controller

(Continued)

Table 4-17. Overlay Indicators (Cont.)

Overlay	PET	Description
FF2	10	Major phase determinate. It is used in conjunction with FF1 to determine major phase of controller. The indications show the major phase the controller is in FF1 FF2 Major Phase 0 0 00F 0 1 01F 1 1 03F
FU1, FU2, FU3	11, 12, 13	Subphase or minor phase determinate of controller. The various combinations below are possible: FU1 FU2 Minor Phase 0 0 00U 0 1 01U 1 0 02U 1 1 03U
RATE	15	Rate error. A rate error can occur during a read or write operation
BFR0-BFR7	0-8	Read data. Used to indicate data pattern being read in each of 9 channels. Due to frequency and pulse width, indicators do not turn on. It is necessary to patch into one-shot circuit (AUX1 or AUX2) to get an indication of the data pattern

Note

To keep the tape path aligned and to prevent loss of air pressure, the casting and guide base must be absolutely clean before replacement.

h. After applying a thin coat of silicone grease to the base of the guide to ensure an airtight seal, replace the spring and secure the guide housing to the main casting.

CAUTION

To assure an unimpeded flow of cushioning air and to prevent tape contamination, the ceramic cap and guide upper surface must be absolutely clean before replacement.

i. Replace the ceramic cap and tighten the guide mounting screw until the O-ring is compressed.

Note

Guide housings are not interchangeable due to the different tape wrap positions, so the correct guide must be specified during replacement. All other parts are identical for each assembly.

4-64 Write Enable Switch Removal and Replacement (See figure 3-11)

To completely remove the write enable switch assembly, the reel motor-reel brake assembly must first be removed. (See paragraph 4-73.) Proceed as follows:

a. Disconnect the two plastic tubes connected to the write enable switch housing at the rear of the main casting.

b. Loosen one of the collet mounting screws.

c. Loosen the collet clamping screw.

d. Remove write enable switch assembly.

e. Using internal circlip pliers, remove the circlip from write enable switch housing.

f. Remove piston rod assembly and spring.

g. Assemble with replacement parts by reversing this procedure.

h. The front face of the write enable switch assembly should be set by means of the collet approximately 0.03 in. from the rear face of the holddown knob housing, with the holddown knob assembly in its pressed position.

Note

The position of the write enable switch assembly may be adjusted without removing any parts by means of the collet clamping screw and collet mounting screw.

4-65 Reel Motor Brake Removal and Replacement
(See figures 4-7, 4-8, and 4-12)

The following test equipment is required for this procedure:

a. Dc power supply, 40 volts at 0.3 amp (the +25 and -25 internal station supply may be used).

b. 0.010-in. thickness gauge.

c. 0- to 16-oz spring scale.

The procedure for removal and replacement is as follows:

a. Open the sliding front door.

b. Disconnect the reel motor brake electrical connections. (See figure 4-13.)

c. Connect the brake electrical connections to an external power supply or across the +25 Vdc and -25 Vdc internal station supply.

d. With power applied, remove the four screws from the rear of the brake housing. Remove the brake assembly from the reel motor.

CAUTION

The drag brake spring will release the outer friction disc from the spline hub once the magnet and sleeve assembly are removed.

e. Remove the drag brake spring, fixed spacer, and inner friction disc.

f. Remove the four mounting screws from the end plate. Secure the end plate to the brake housing, using the four long screws.

g. Power may now be safely removed.

h. Apply power to the replacement brake assembly.

i. Remove the four long screws from the rear of brake assembly.

j. Remove the end plate from the brake assembly and install the plate on the reel motor.

k. Install the replacement inner friction disc.

l. Replace the fixed spacer.

m. Replace the drag brake spring.

n. Install the replacement outer friction disc, holding the disc against the spring by means of a piece of string (see figure 4-8).

Note

Only one face of the inner and outer friction disc will wear, due to the drag brake. The life of the friction discs may be extended by reversing the discs during replacement.

o. With power applied to the brake, a second person should mount the magnet and adjusting sleeve assembly while the outer friction disc is held in place.

p. The string should pass through the slots in the adjusting sleeve, so that it can easily be withdrawn once the magnet and sleeve assembly are mounted.

q. Remove the string.

r. Adjust the air gap between the armature and magnet pole piece, as described in paragraph 4-66.

s. Reconnect electrical connections.

4-66 Reel Motor Brake Adjustment

Adjust the reel motor brake as follows:

a. With no power applied to the brake, measure the air gap between the magnet pole piece and the armature, using a feeler gauge inserted through one of the four cutouts around the brake adjustment sleeve. The gap should be .010 in.

b. Using internal or external power, energize the brake (dc power supply 40V at 0.3 amp if external power is used).

c. Slacken the four screws at the rear of the brake housing approximately three turns each.

d. To increase the air gap between the magnet pole piece and armature, rotate the adjustment sleeve clockwise as viewed from the rear (counterclockwise will decrease the gap). A quarter turn of the adjustment sleeve approximates a change of .015 in. in the gap between the magnet pole piece and the armature.

e. Tighten the four brake housing screws and remove power to the brake.

CAUTION

Never remove power to the brake unless the four brake housing screws are secure.

f. Check the armature air gap and repeat the procedure if necessary until the gap is .010 in.

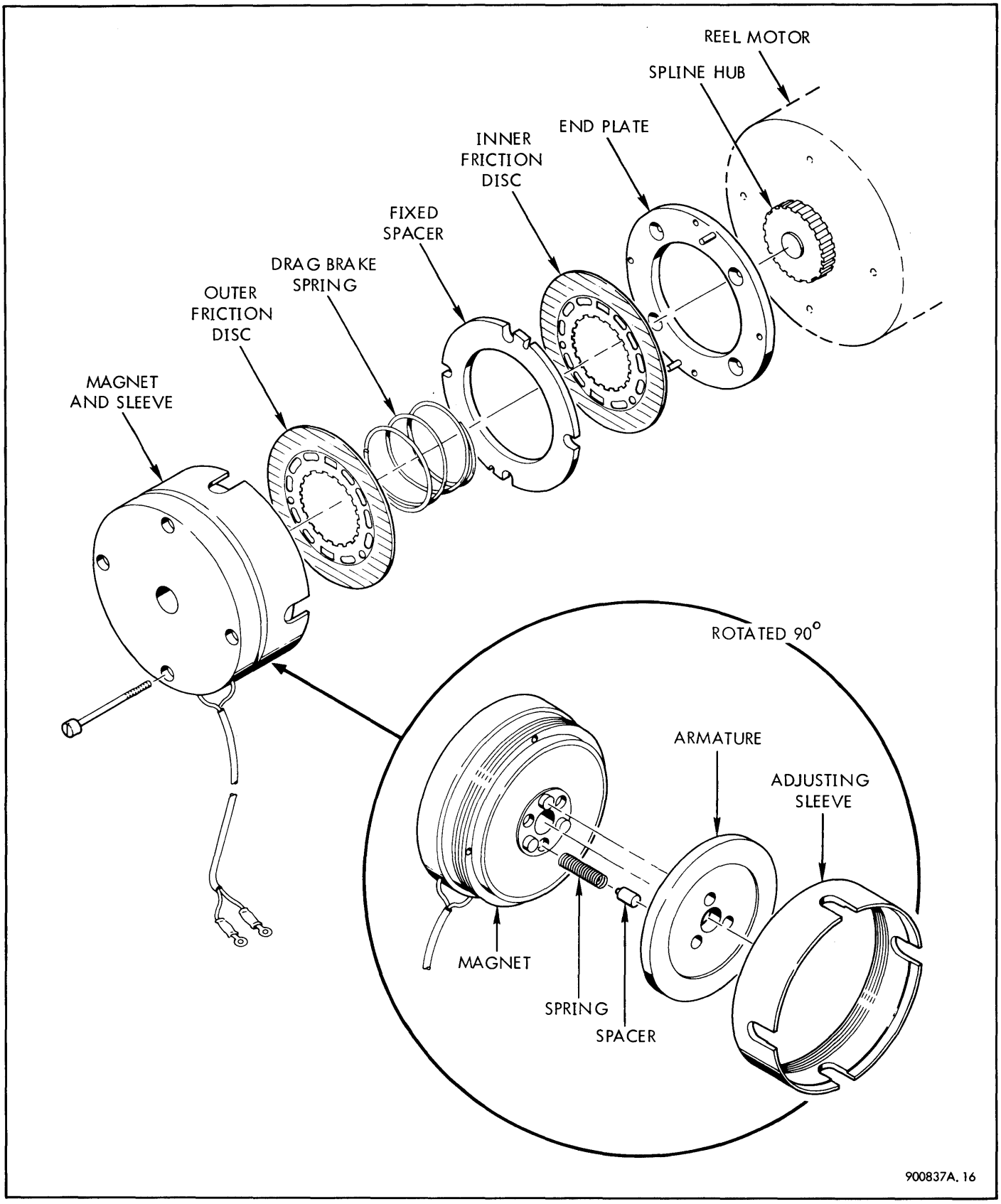


Figure 4-7. Reel Motor Brake, Exploded View

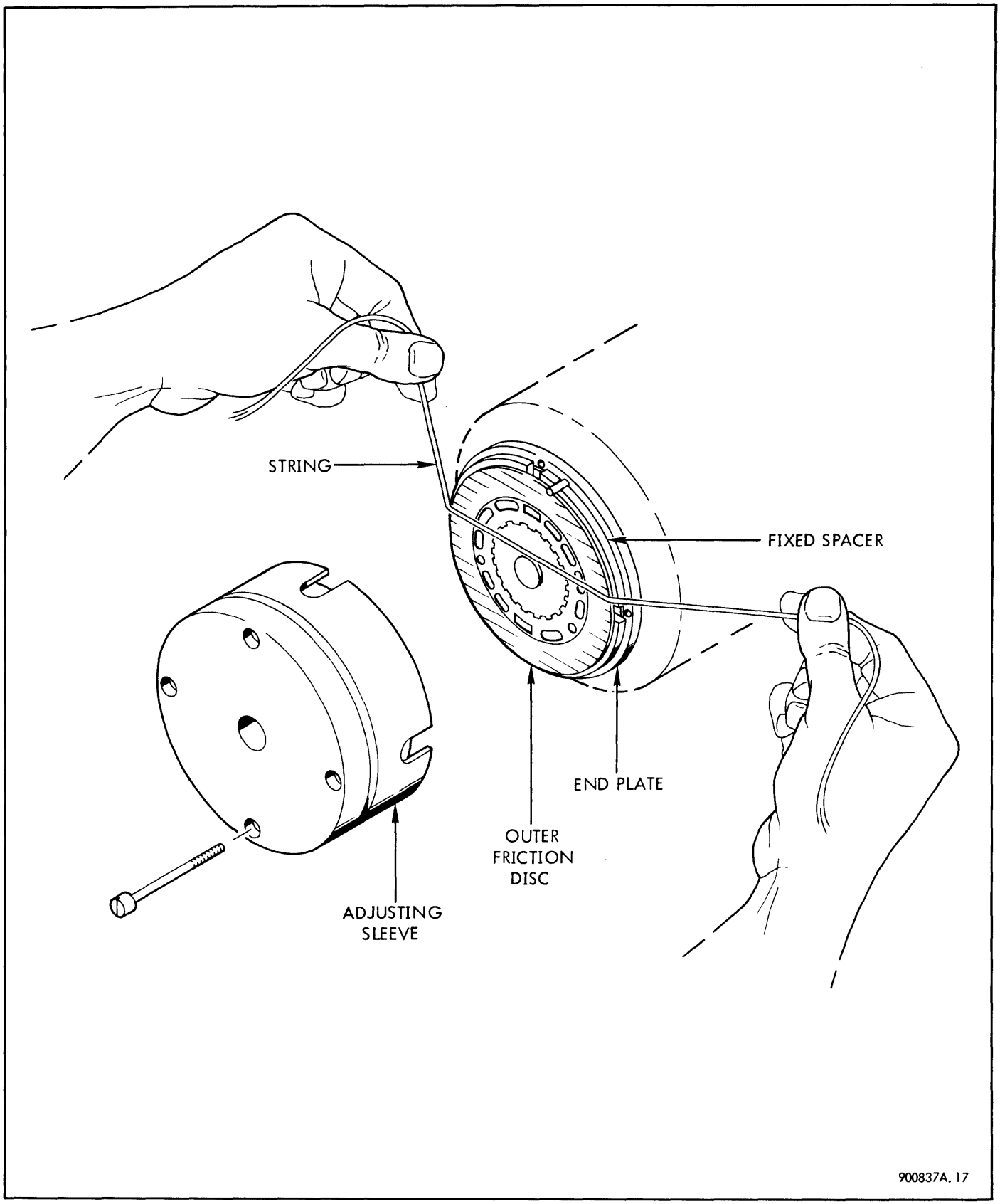


Figure 4-8. Reel Motor Brake, Reassembly

4-67 File Reel Holddown Knob Removal and Replacement
(See figures 4-9 and 2-5)

Perform the following steps:

a. Remove the three screws holding the cover.

b. Withdraw the cover locating pin assembly and shim located behind the cover.

c. Remove the locating pin from the cover only if replacement is required.

d. Remove the three-shoe pivot, pin pivot arm assemblies.

Note

Do not turn pivot arm unless necessary; if the arm is turned, the unit will have to be readjusted on assembly.

e. Dismantle the shoe pivot, pin pivot arm assembly only if replacement is required.

Note

The slider pins have a slight taper with a 1/8-in. long parallel portion at one end. This end is nearest the turntable and care should be taken to reassemble in the same position.

f. Remove the three screws holding the slider pins and withdraw the slider pins from the housing. The housing is now loose.

g. Remove the rubber ring from the housing only if replacement is required.

h. It is not necessary to remove the pivot arm post to remove the reel brake assembly from the transport. If removal of the pivot arm post is required, remove the three screws, then remove the post.

i. All parts should be thoroughly cleaned before replacement.

j. Replace parts by reversing this procedure.

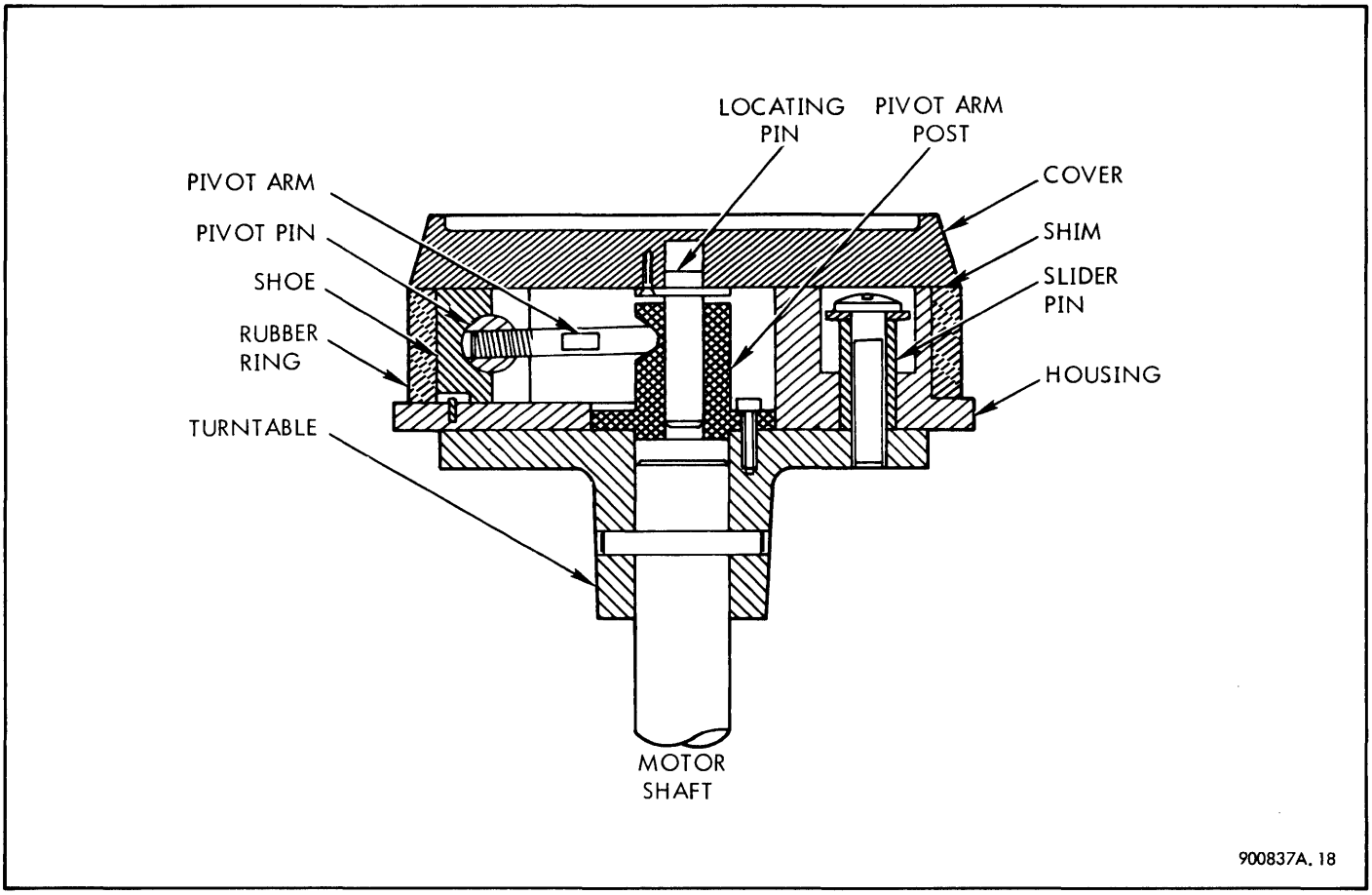


Figure 4-9. File Reel Hub

k. Apply a thin coat of silicone grease to the slider pins, pivot arm knuckle joints, and locating pin before replacement.

l. If the rubber ring shows signs of wear at the point where the shoes react, rotate the rubber ring 60 degrees with respect to the housing.

m. Before tightening the slider pin screws, locate the adjustment fixture reference pin in the pivot arm post to maintain concentricity between the housing and the pivot arm post.

n. Insert shoe pivot, pin pivot arm assemblies.

Note

If no replacements have been made on the shoe pivot, pin pivot arm assembly, no adjustment will be required during assembly. However, if any part of the assembly has been replaced, the adjustment fixture must be used to reset the correct length of the pivot arm.

o. The correct length of the pivot arm is set by rotating the pivot arm, which is threaded into the pivot pin. Flats are provided on the pivot arm for this purpose.

p. After assembly, the holddown knob should be tested for holding torque greater than the reel brake torque, and for concentricity of the reel during rotation.

q. Individual adjustment of the pivot arms determines the concentricity of the reel, and equal adjustment of all the pivot arms determines the reel holding torque. Both conditions are satisfied if the adjustment fixture is used.

Note

Only the cover-locating pin assembly and shim need be removed to adjust the holddown knob using the adjustment fixture.

4-68 Fixed Reel Removal and Replacement

Proceed as follows:

a. Remove the three screws holding the cover.

b. Withdraw the cover and the backup washer.

c. Remove the fixed reel.

d. Remove the adapter assembly.

e. Replace parts by reversing this procedure.

Note

For reel replacement only, the adapter assembly need not be removed.

4-69 Reel Tachometer Removal and Replacement (See figure 4-19)

The following test equipment is required for this procedure:

a. Special alignment fixture

b. 0.015-in. thickness gauge

Perform the following procedure for removal and replacement:

a. Loosen one of the reel tachometer collet mounting screws.

Note

Only one of the two reel tachometer collet mounting screws will be readily accessible; loosening either will suffice.

b. Loosen the collet clamping screw.

CAUTION

Note the polarity of the electrical connections. The tachometer terminals are marked 1 and 2; be careful during replacement not to switch the lead connections.

c. Remove the electrical connections to the tachometer at the rear of the main casting. (See figure 4-13.)

d. Remove the tachometer pulley assembly.

e. Loosen the tachometer pulley screw and remove the pulley.

f. Attach the pulley to the replacement tachometer using a 0.015-in. feeler gauge to set the gap between the pulley flange and the front flange of the tachometer.

g. Place the tachometer pulley assembly in the collet and tighten the collet clamping screw so that the tachometer pulley assembly can just slide within the collet with a small force applied.

h. Remove the four screws holding the top outer cover of the chamber.

i. Set the position of the tachometer pulley assembly, using the special alignment fixture.

Note

Never adjust the position of the tachometer pulley by adjusting the position of the pulley on the tachometer shaft. Always adjust the pulley position by means of the collet.

j. The special alignment fixture sets the position of the lower inside tachometer pulley flange with respect to the chamber base.

k. Tighten the collet clamping screw.

l. Tighten the collet mounting screw.

m. Replace the tachometer electrical connections (note polarity).

n. Replace the top outer cover of the chamber.

o. Using a length of tape pulled tightly across the tachometer pulley and the adjacent guide, check to determine that the tape edge does not interfere with the chamber base or cover.

4-70 Capstan Motor Removal and Replacement
(See figure 4-10)

Proceed as follows to remove and replace the capstan motor:

a. Remove the fixed reel, following the procedure listed in paragraph 4-68.

b. Remove the overlay panel directly behind the capstan by removing the three screws at the rear of the transport casting.

c. Remove the capstan securing screw.

CAUTION

Two flats on the capstan motor shaft immediately behind the capstan enable the shaft to be held by an adjustable wrench. In making adjustments, never hold the capstan, as it can easily be damaged.

d. Remove the capstan and two rubber washers, one on either side of the capstan.

e. Disconnect the two flexible tubes from the capstan motor cooling shroud nipples.

CAUTION

Note the polarity of connections.

f. Disconnect the motor and tachometer electrical connections at the terminal boards.

g. Remove the four screws holding the capstan motor while a second person holds the motor assembly at the rear of the transport; then place the motor on a workbench.

h. Remove the two screws holding the capstan motor housing cover and remove the cover.

i. Remove the two cover spacers.

j. Remove the seven screws holding the capstan motor cooling shroud and remove the shroud.

k. Loosen the tachometer coupling screw and remove the tachometer and coupling.

l. Remove the capstan tachometer mount.

m. Remove the rubber gasket from the capstan motor.

n. Use new rubber gasket on the replacement capstan motor, making sure that the windows in the gasket correspond to the cooling hole segments in the motor.

o. Replace the tachometer coupling and the tachometer. (See capstan tachometer removal and replacement procedure in paragraph 4-71.)

p. Replace the tachometer mount.

q. Replace the cover spacers and cover.

r. Replace the cooling shroud.

s. Mount the motor.

t. Replace the capstan, using two new rubber washers.

u. Replace the overlay panel.

v. Reconnect the vacuum tubing.

w. Reconnect the motor and tachometer electrical connections.

4-71 Capstan Tachometer Removal and Replacement
(See figure 4-10)

Proceed as follows to remove and replace the capstan tachometer:

a. Remove the two screws holding the capstan motor housing cover.

CAUTION

Note the polarity of the electrical connections. The tachometer terminals are marked 1 and 2; be careful during replacement not to switch the lead connections.

b. Remove the electrical connections to the tachometer.

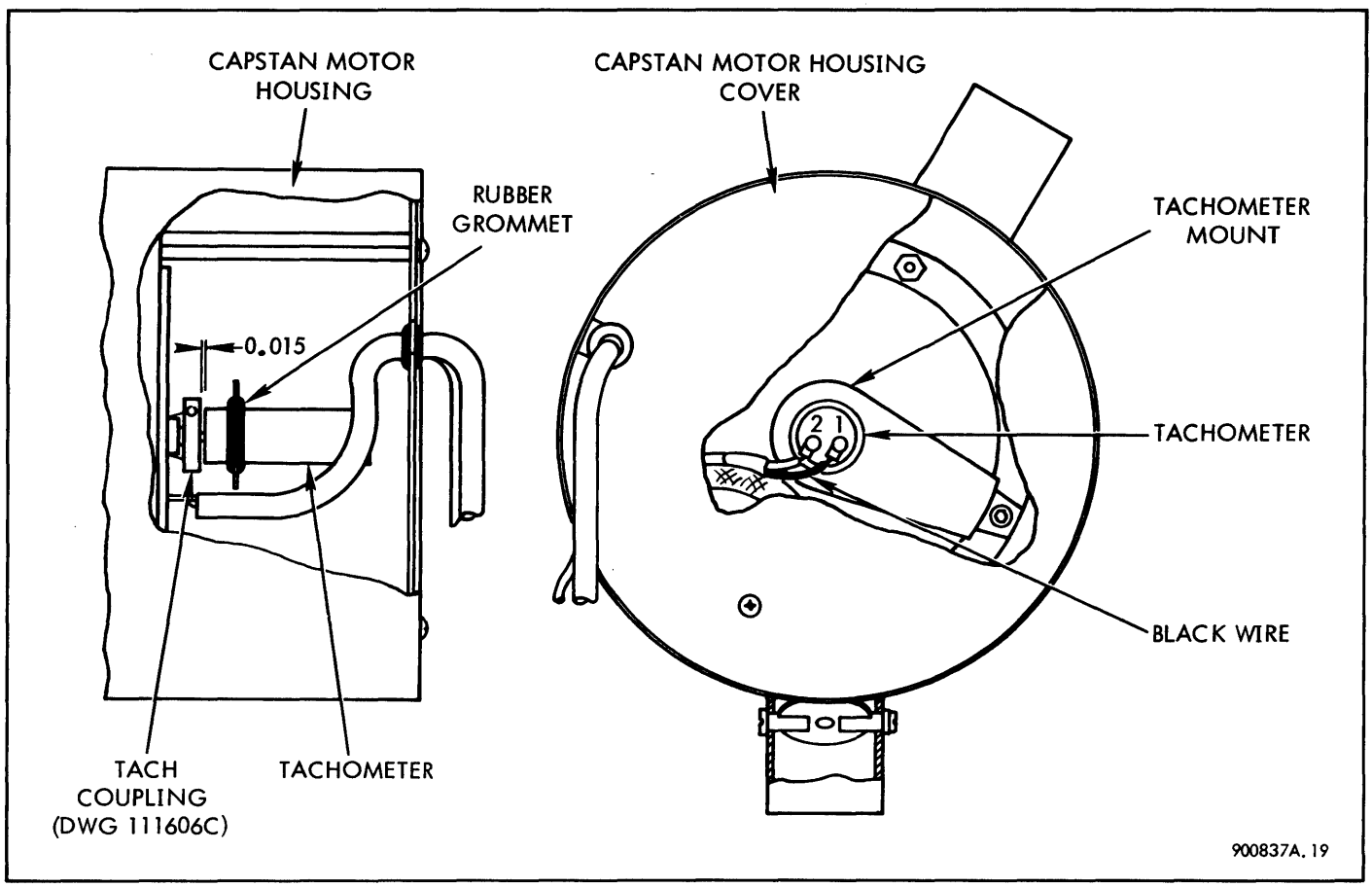


Figure 4-10. Capstan Tachometer Mounting Position

c. Loosen the tachometer coupling screw.

d. Remove the tachometer, sliding the mount grommet across the tachometer housing.

e. Install the replacement tachometer by reversing this procedure.

CAUTION

The position of the capstan tachometer and tachometer coupling is important. (See figure 4-10.)

4-72 Positive Pressure Pump Removal and Replacement
(See figure 4-20)

Proceed as follows:

a. Disconnect the plastic tube fitting at the pump outlet.

b. Disconnect the electrical connections to the pump at terminal board A, pins 5 and 7. (See figure 4-21.)

c. Remove the four screws holding the pump.

d. Remove the air filter from the pump inlet.

e. Replace the air filter on the replacement pump.

f. Reverse this procedure for pump replacement.

CAUTION

Examine the nylon olive at the pump output fitting for damage. If it is damaged, replace it.

4-73 Reel Motor Removal and Replacement
(See figure 4-12)

Proceed as follows to remove and replace the reel motor:

a. Remove the electrical connections from the reel motor and brake.

b. Before removing the file reel motor, remove the file reel (paragraph 4-67).

c. Before removing the fixed reel motor, remove the fixed reel (paragraph 4-68).

d. Remove the motor brake by following the procedure listed in paragraph 4-65 steps a through d.

e. Remove the four corner screws that secure the motor mounting bracket to the main casting, and lift the motor away from the casting.

f. Install the replacement motor by reversing the removal procedure.

4-74 Read/Write Head Removal and Replacement
(See figure 4-17)

CAUTION

Care must be taken at all times to avoid damage to faces of the read/write heads.

Proceed as follows:

a. Disconnect the two read/write head connectors at rear of transport casting.

b. Remove the overlay panel directly behind the capstan (three screws at the rear of the transport casting).

c. Remove the three screws holding the read/write head assembly.

d. Remove the read/write head assembly by passing the connectors through the opening in the transport casting.

e. Remove the four screws holding the head cover to the baseplate.

f. Remove the head cover.

g. Remove the tape cleaner assembly (one screw).

h. Mount tape cleaner assembly on the replacement head assembly.

i. Replace the head cover assembly.

j. Pass the connectors through the opening in the transport casting.

k. Secure the read/write baseplate to casting.

l. Connect the read/write head connectors.

m. Replace the overlay panel.

Note

No mechanical shimming is required after replacement of the read/write assembly.

4-75 Photosense Removal and Replacement
(See figure 4-14)

Proceed as follows for photosense removal and replacement:

a. Disconnect the electrical connections to the photosense at terminal board TB5T, pins 4 to 11, inclusive.

b. Remove the photosense mounting screw from the rear of the main casting.

c. Remove the photosense assembly, passing the electrical leads and connectors through the clearance hole in the main casting.

d. Install the replacement photosense assembly by reversing this procedure.

e. Adjust the lamp intensity as described in paragraph 4-22.

Note

Damaged photosense assemblies should be returned to SDS for repair.

4-76 Erase Head Removal and Replacement
(See figure 4-16)

Proceed as follows to remove and replace the erase head:

a. Disconnect the erase head wires from TB1 on the head cable assembly. (Observe polarity.)

b. Remove the erase head mounting screw from the front of the transport.

c. Remove the erase head, passing the wires and terminals through the clearance hole in the main casting.

d. Install the replacement head by reversing this procedure.

e. Adjust the erase head position as described in table 4-4.

4-77 PARTS LIST

The tables and figures in this section list and illustrate the replaceable parts in the magnetic tape system.

4-78 TABULAR LISTINGS (Tables 4-18 through 4-44)

The replaceable parts are arranged in parts list tables. Table 4-18 lists the main assemblies of the equipment. Each main assembly is then broken down into subassemblies or component parts. Breakdown by table continues until all replaceable parts down to a field replaceable level

have been listed and illustrated. Each parts list table is arranged in six columns, as follows:

a. The figure number of the listed part

b. A brief description of the part

c. The reference designator of the part as shown on the schematic diagram for that part

d. The manufacturer's code for the part

e. The manufacturer's part number for the part

f. The quantity of the part used per assembly

4-79 ILLUSTRATIONS (Figures 4-11 through 4-28)

Each parts list is accompanied by a figure showing parts placement for that list. Also shown in some cases are schematic diagrams for assemblies.

4-80 MANUFACTURER CODE INDEX (Table 4-45)

The manufacturers of parts listed in this section are indicated by code numbers. Their names and addresses are shown in the manufacturer code index (table 4-45).

Table 4-18. Magnetic Tape System

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
	Magnetic Tape System 7371/7372/ 7374 *		SDS	133665	1
4-11, 4-12	. Tape Transport Assembly (See table 4-19 for replaceable parts)		SDS	131296	1
4-20	. Blower Shelf Assembly (See table 4-27 for replaceable parts)		SDS	113779	1
4-22	. Operator Control Panel Assembly (See table 4-28 for replaceable parts)		SDS	123145	1
1-1, 1-2	. 28" Cabinet Assembly (See table 4-29 for replaceable parts)		SDS	124361	1
1-1	. Front Door Assembly (See table 4-44 replaceable parts)		SDS	124371	1

*See figure 4-2 for wiring diagram

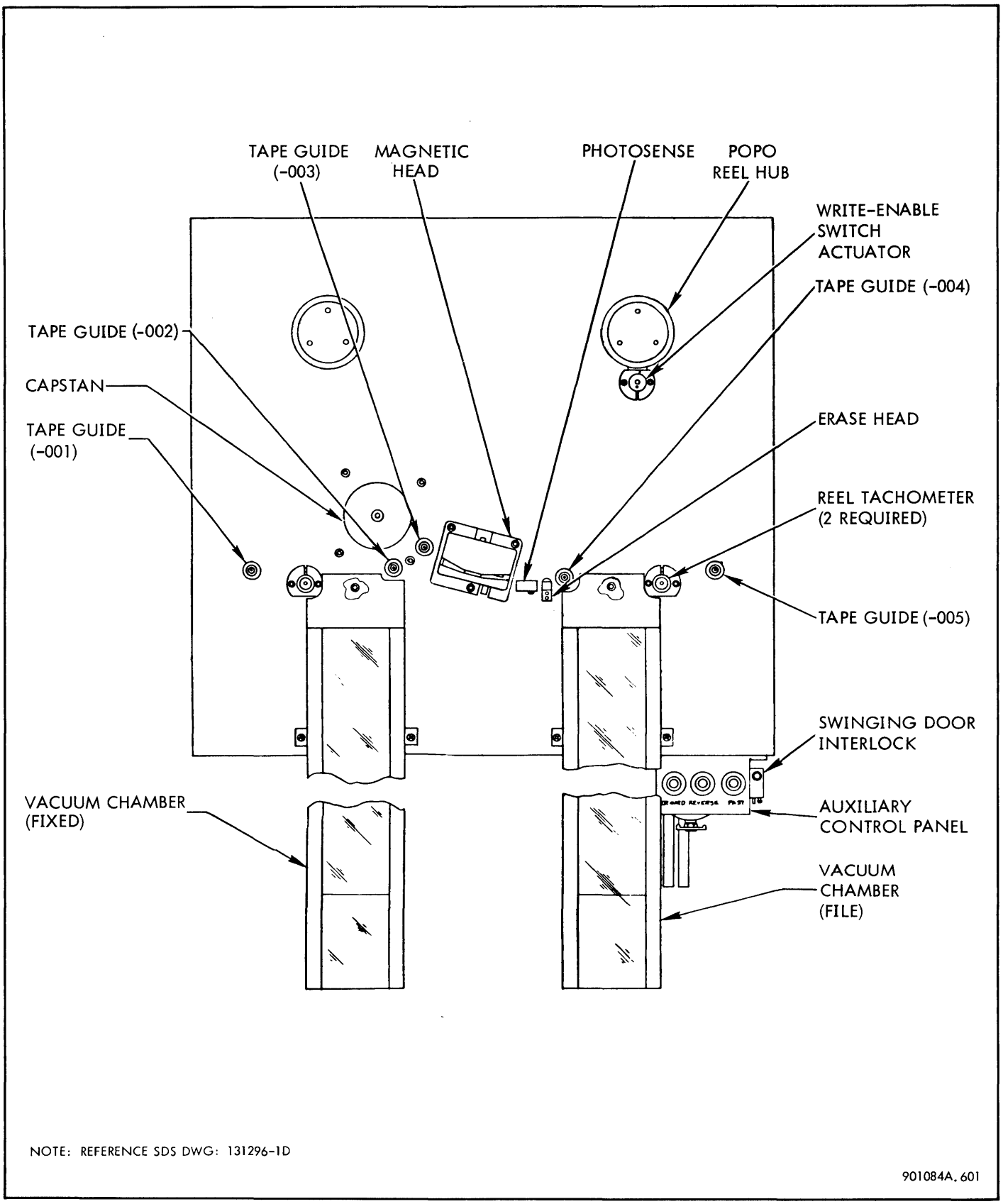


Figure 4-11. Transport Front View

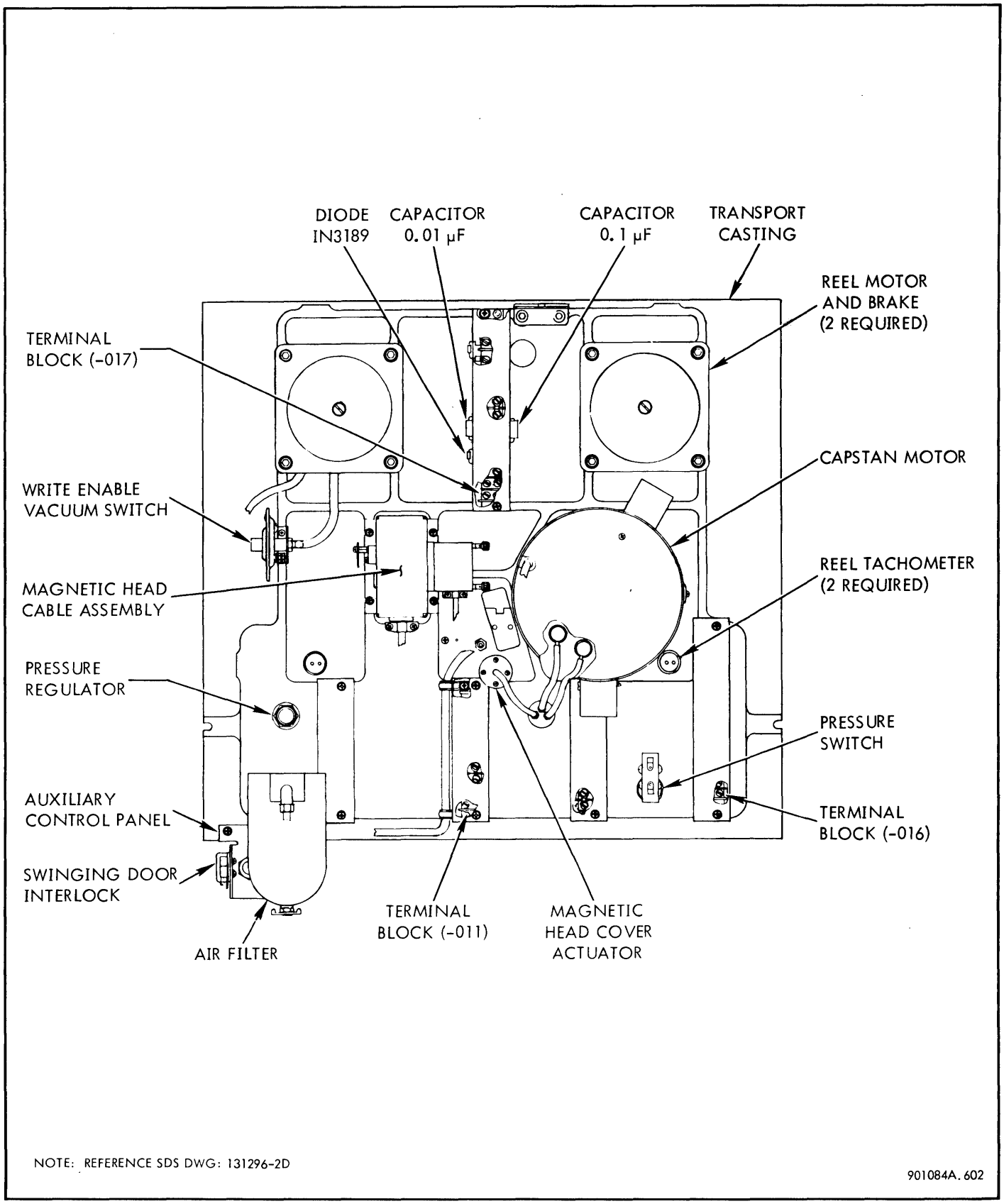


Figure 4-12. Transport Rear View

Table 4-19. Magnetic Tape Transport Assembly, Replaceable Parts

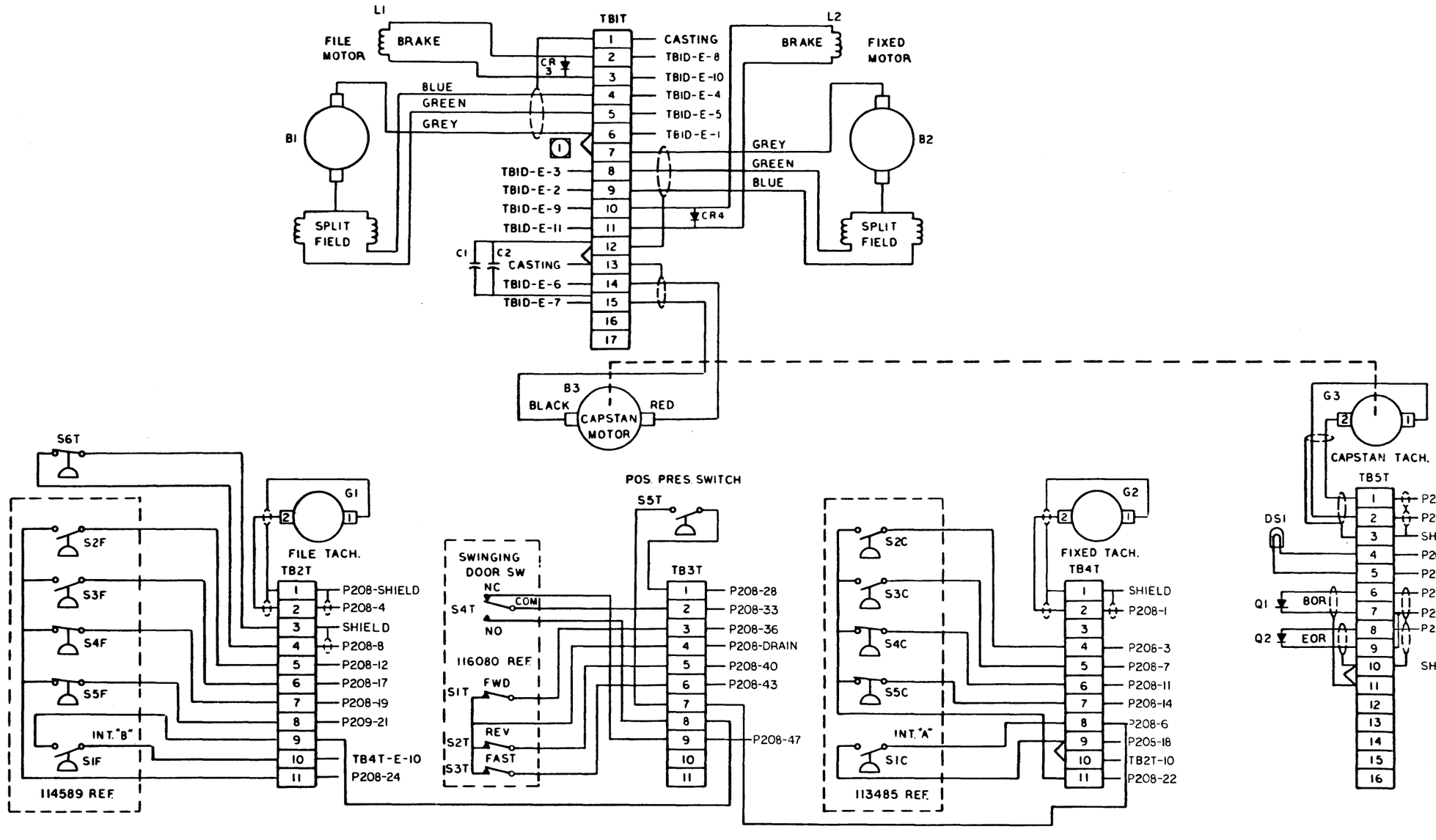
Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
4-11, 4-12	Magnetic Tape Transport (See table 4-18 for next higher assembly)*		SDS	131296	Ref
4-14	. Photosense Assembly (See table 4-20 for replaceable parts)		SDS	111776	1
4-15	. Capstan Motor Assembly (See table 4-21 for replaceable parts)		SDS	111599	1
4-12	. Reel Motor Brake Assembly (See table 4-22 for replaceable parts)		SDS	111469	2
4-18	. Auxiliary Control Panel Assembly (See table 4-23 for replaceable parts)		SDS	116080	1
4-19	. Reel Tachometer Assembly (See table 4-24 for replaceable parts)		SDS	116220	2
4-11	. Fixed Vacuum Chamber Assembly (See table 4-25 for replaceable parts)		SDS	113485	1
4-11	. File Vacuum Chamber Assembly (See table 4-26 for replaceable parts)		SDS	114589	1
3-9	. Actuator, head cover		SDS	116111	1
	. Assembly, head cable		SDS	123146	1
	. Block, terminal, 2-screw (SDS 100094-011)		51	141	3
	. Block, terminal, 2-screw (SDS 100094-016)		51	141	1
	. Block, terminal, 2-screw (SDS 100094-017)		51	141	1
	. Capacitor, Mylar, 0.01 µF 10%, 80V (SDS 100308-103)		25	64F	1
	. Capacitor, Mylar, 0.01 µF 10%, 80V (SDS 100308-104)		25	64F	1
	. Capstan, 2.8 in. dia		SDS	107827	1
	. Diode, silicon (SDS 101164)		5	IN3189	2
3-8	. Guide, tape		SDS	111342-001	1
3-8	. Guide, tape		SDS	111342-002	1
3-8	. Guide, tape		SDS	111342-003	1

* See figure 4-13 for wiring diagram

(Continued)

Table 4-19. Magnetic Tape Transport Assembly, Replaceable Parts (Cont.)

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
3-8	. Guide, tape		SDS	111342-004	1
3-8	. Guide, tape		SDS	111342-005	1
4-16	. Head, erase		SDS	123381	1
4-17	. Head, magnetic, 7-channel		SDS	134019	1
3-7	. Regulator, pressure (SDS 111765)		360	AA325	1
3-10	. Switch, pressure (SDS 113707-001)		361	222-240-9591	1
	. Switch, snap action		SDS	109372	1
	. Switch, snap action		SDS	114285	1
3-19	. Switch, vacuum		SDS	113691-100	1
3-11	. Switch, write enable		SDS	111767	1



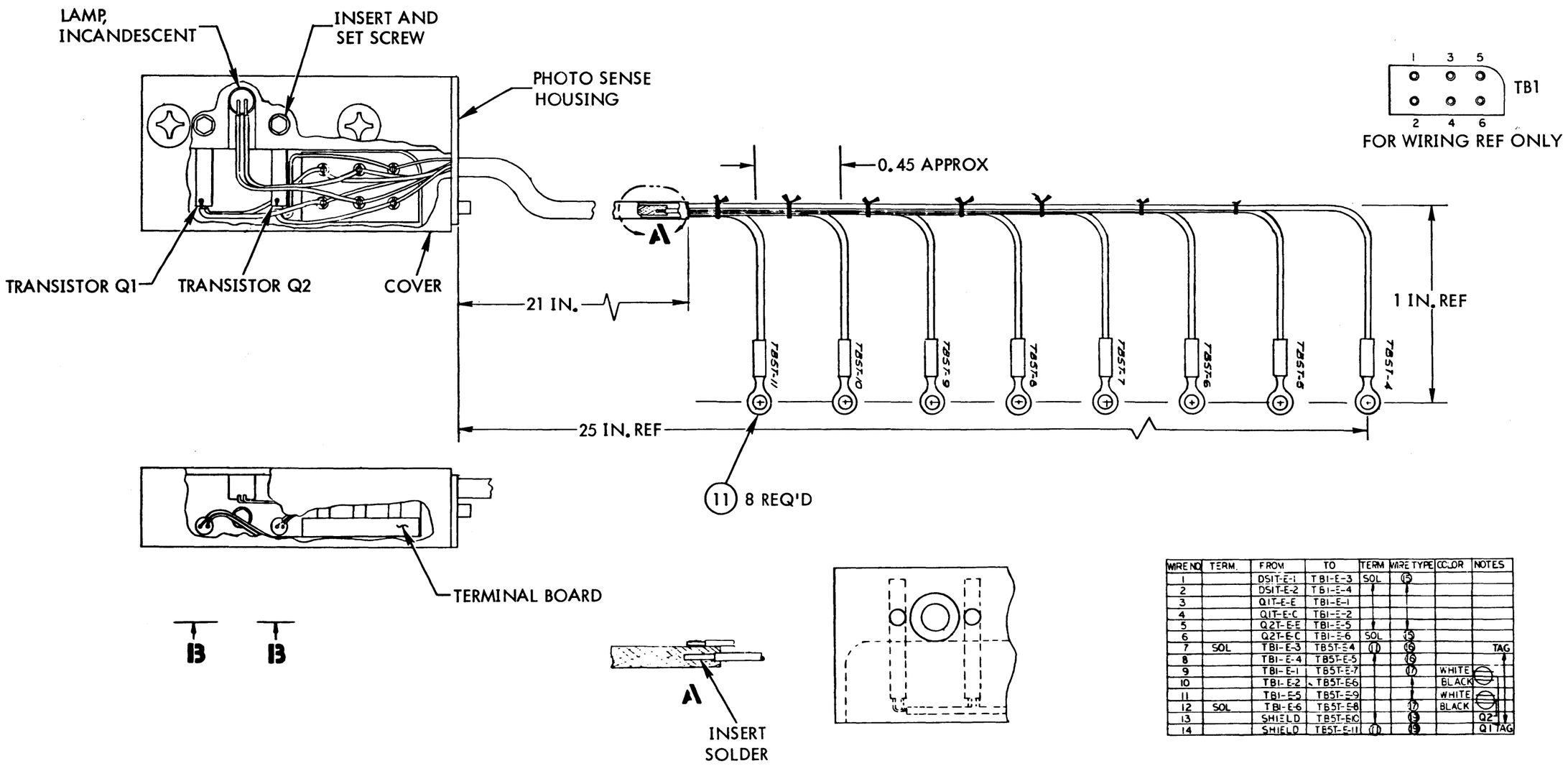
NOTE: REFERENCE SDS DWG: 131298-1C

Figure 4-13. Transport Wiring Diagram

901084A. 705

Table 4-20. Photosense Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
4-14	Photosense Assembly (See table 4-19 for next higher assembly)		SDS	111776	Ref
	. Board, terminal		SDS	113170	1
	. Cover, photosense		SDS	111780	1
	. Lamp, incandescent, 5V unbased (SDS 111778)	DS1	363	D39	1
	. Transistor, npn, photoconditioned (SDS 224)	Q1, Q2	5	21DF2 (1)	2



WIRE NO	TERM.	FROM	TO	TERM	WIRE TYPE	COLOR	NOTES
1		DS1T-E-1	TB1-E-3	SOL	15		
2		DS1T-E-2	TB1-E-4				
3		Q1T-E-E	TB1-E-1				
4		Q1T-E-C	TB1-E-2				
5		Q2T-E-E	TB1-E-5				
6		Q2T-E-C	TB1-E-6	SOL	15		
7	SOL	TB1-E-3	TB5T-E-4	10	16		TAG
8		TB1-E-4	TB5T-E-5		16		
9		TB1-E-1	TB5T-E-7		17	WHITE	
10		TB1-E-2	TB5T-E-6			BLACK	
11		TB1-E-5	TB5T-E-9			WHITE	
12	SOL	TB1-E-6	TB5T-E-8		17	BLACK	
13		SHIELD	TB5T-E-10		18		Q2
14		SHIELD	TB5T-E-11	11	18		Q1 TAG

NOTES : 1. RED DOT INDICATES COLLECTOR LEAD.
USE CLEAR TEFLON TUBING OVER RED DOT

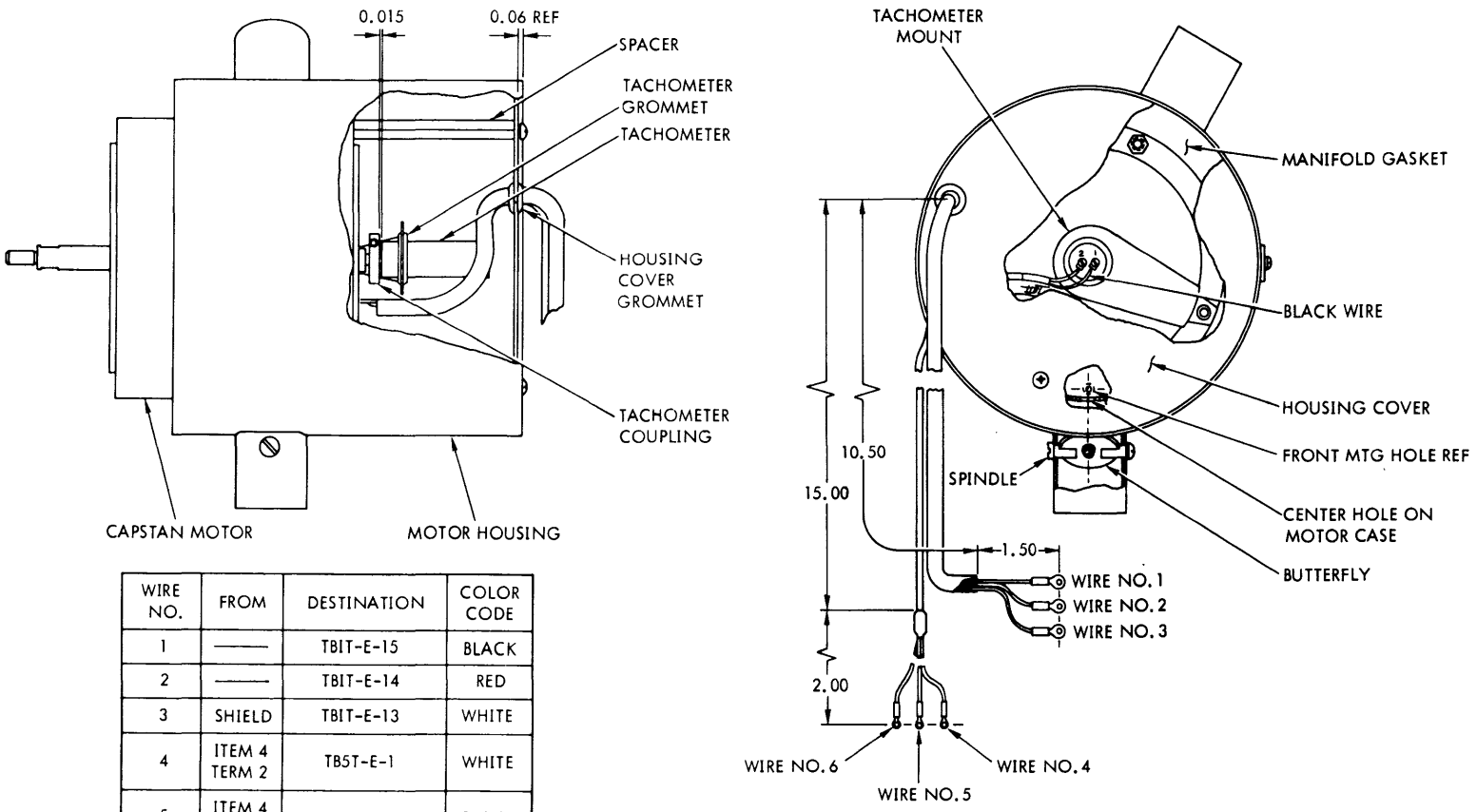
2. REFERENCE SDS DWG: 111776-1E

Figure 4-14. Photosense Assembly

901084A.606

Table 4-21. Capstan Motor Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
4-15	Capstan Motor Assembly (See table 4-19 for next higher assembly)		SDS	111599	Ref
	. Butterfly, motor housing		SDS	116713	1
	. Coupling, tachometer		SDS	111606	1
	. Gasket, manifold		SDS	111601	1
	. Grommet, rubber, housing cover		SDS	100720-005	1
	. Grommet, rubber, tachometer		SDS	100720-010	1
	. Motor, capstan		SDS	108057	1
	. Mount, tachometer		SDS	111605	1
	. Spacer, capstan housing		SDS	116143	2
	. Spindle, motor housing		SDS	116714	1
	. Tachometer, capstan		SDS	111829	1

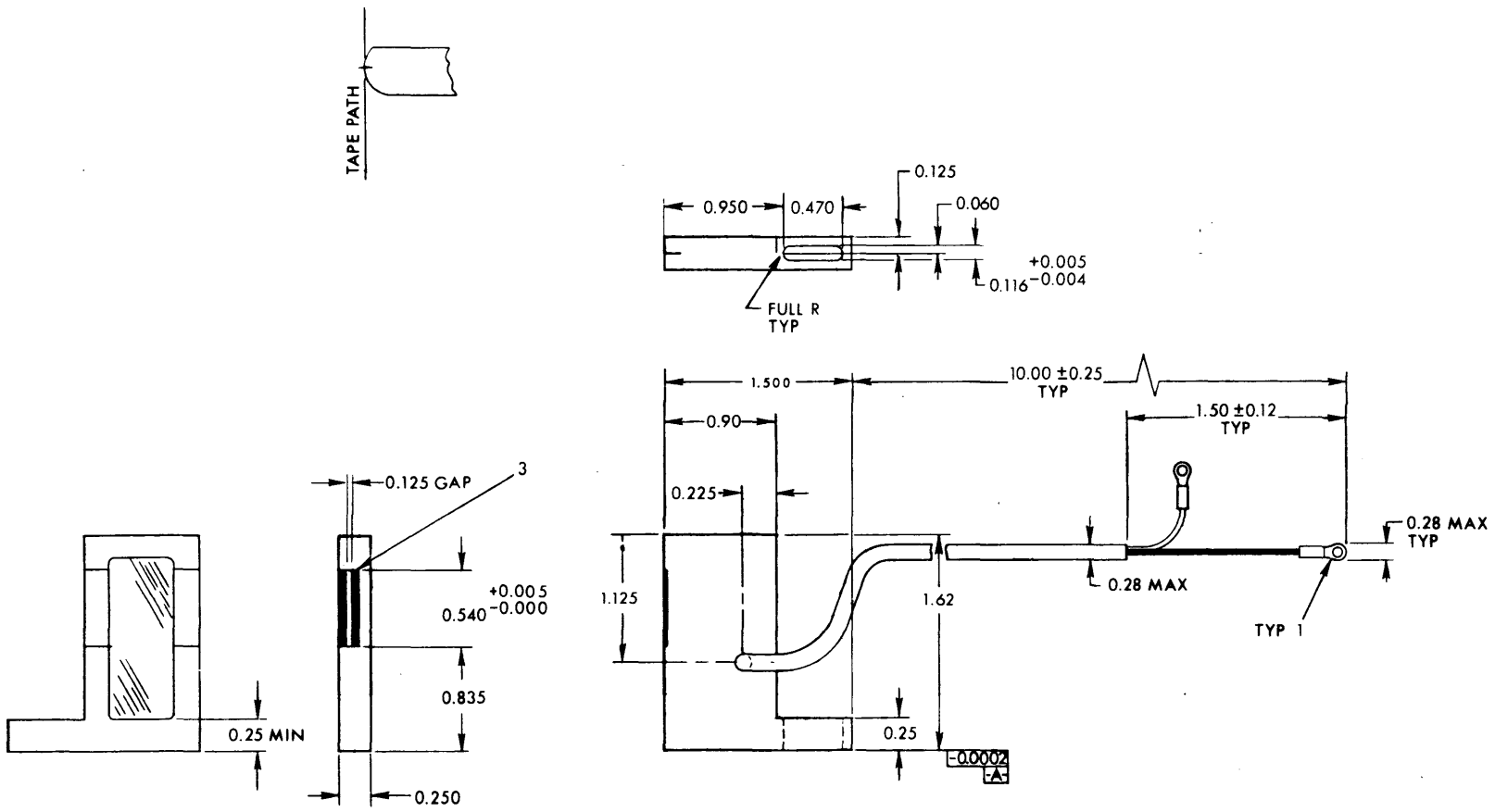


WIRE NO.	FROM	DESTINATION	COLOR CODE
1	———	TB1T-E-15	BLACK
2	———	TB1T-E-14	RED
3	SHIELD	TB1T-E-13	WHITE
4	ITEM 4 TERM 2	TB5T-E-1	WHITE
5	ITEM 4 TERM 1	TB5T-E-2	BLACK
6	SHIELD	TB5T-E-3	WHITE

NOTE: REFERENCE SDS DWG: 111599-1C

901084A.614

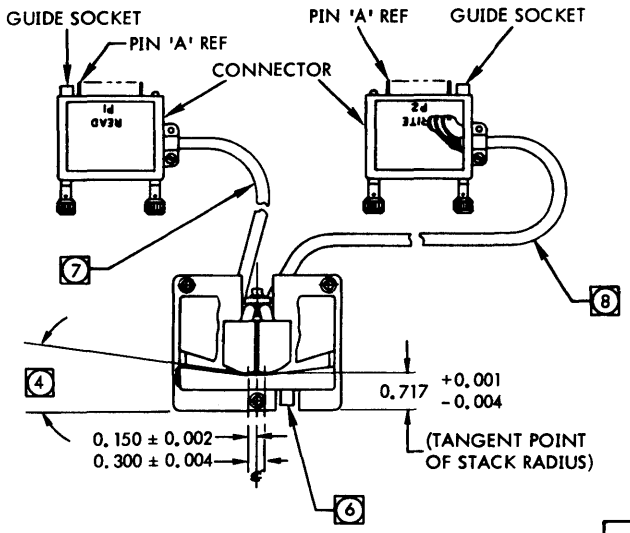
Figure 4-15. Capstan Motor Assembly

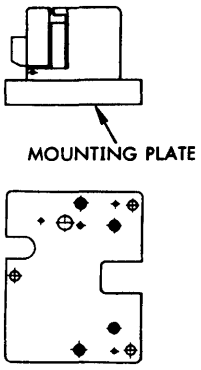


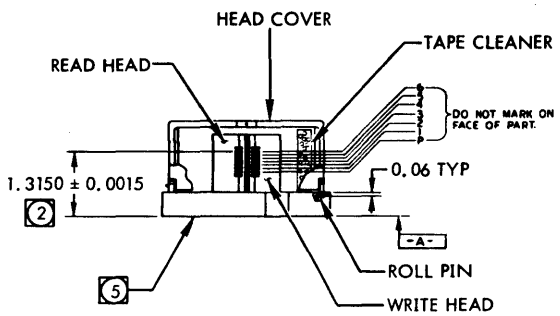
NOTES: 1. INSULATED RING TONGUE TERMINAL FOR #6-32NC
2. TOLERANCES TO BE XX 0.010, XXX 0.005
3. NORTH SEEKING END OF COMPASS WILL SEEK THIS CORE HALF WHEN CURRENT IS APPLIED
4. REFERENCE SDS DWG. 123381F

901013A.404

Figure 4-16. Erase Head Assembly







HEAD GATE REMOVED FROM THIS VIEW FOR CLARITY

CHANNEL	COLOR	READ HEAD TO P1	WRITE HEAD TO P2
P	WHT BLK B/W	B A D	B D A
1		F E J	F J E
2		L K N	L N K
3		R P T	R T P
4		V U X	V X U
5		Z Y BB	Z BB Y
6	WHT BLK B/W	DD CC FF	DD FF CC
GRD	-	C	C

B/W IS CENTERTAP

NOTES : UNLESS OTHERWISE SPECIFIED

1. FOR MAG HEAD SPEC SEE DWG 134022

[2] DIMENSION TO CENTERLINE OF ACTIVE CHANNEL NO. 6

[3] CHANNEL NO. 6 IS THE ACTIVE CHANNEL FARTHEST FROM THE BASE PLATE

[4] TAPE WRAP ANGLE TO BE $8^{\circ}\ ^{+1^{\circ}}_{-1/2^{\circ}}$ FOR ALL TESTS

[5] NO HARDWARE OR OTHER OBJECTS SHALL PROTRUDE BELOW SURFACE -A-

[6] COVER GATE SHALL BE HELD CLOSED BY EXTERNAL ACTUATOR. GATE TRAVEL SHALL BE 60° WITH POSITIVE STOP IN OPEN POSITION

[7] READ CABLE LENGTH IS 9.00 ± 0.50 MEASURED FROM SURFACE "A" TO THE END OF THE CONNECTOR CABLE CLAMP

[8] WRITE CABLE LENGTH IS 8.00 ± 0.50 MEASURED FROM SURFACE "A" TO THE END OF THE CONNECTOR CABLE CLAMP

[9] WHEN THE HEAD GATE IS IN THE CLOSED POSITION, THE MYLAR SIDE OF THE MAGNETIC TAPE (INCLUDING SPLICES, REFLECTIVE TAPE ETC) SHALL NOT TOUCH THE SURFACE OF THE HEAD GATE OR SHIELD. MAINTAIN A MINIMUM CLEARANCE OF 0.010 INCH

[10] EACH TRACK AND TOLERANCE SHALL REFERENCE TO THE BOTTOM OF THE BASEPLATE

TRACK NO.	AND TO BASEPLATE	
P	0.8950	± 0.0015
1	0.9650	± 0.0015
2	1.035	± 0.0015
3	1.105	±.0.0015
4	1.175	± 0.0015
5	1.245	± 0.0015
6	1.315	±.0.0015

11. REFERENCE SDS DWG : 134019-1C

901013A. 403

Figure 4-17. Read/Write Head Assembly

Table 4-22. Reel Motor Brake Assembly

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
4-12	Reel Motor Brake Assembly (See table 4-19 for next higher assembly)		SDS	111469	Ref
	. Disc, friction		SDS	132779	2

Table 4-23. Auxiliary Control Panel Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
4-18	Auxiliary Control Panel (See table 4-19 for next higher assembly)		SDS	116080	Ref
	. Bumper, rubber		SDS	116083-005	1
	. Pushrod, door interlock		SDS	116082	1
	. Switch, interlock		SDS	111757	1
	. Switch, pushbutton, spdt		113	101076-001	3

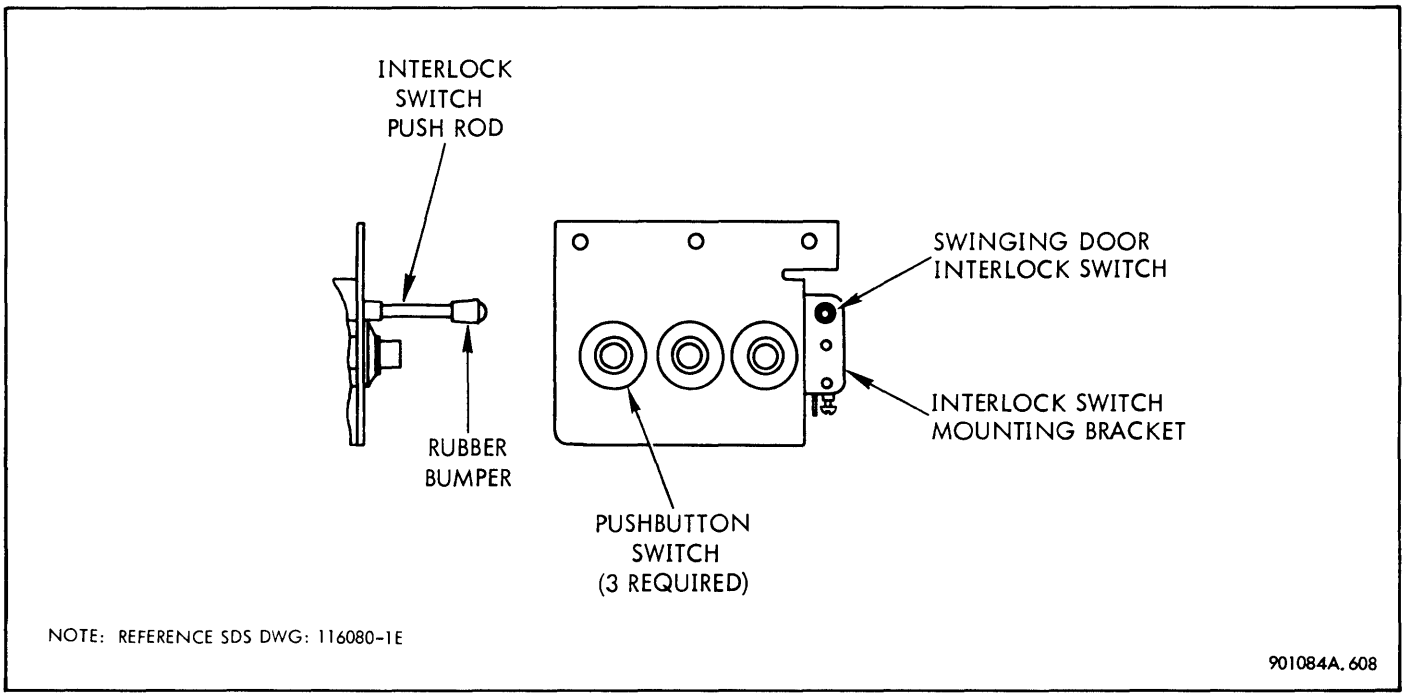


Figure 4-18. Auxiliary Control Panel Assembly

Table 4-24. Tachometer Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
4-19	Reel Tachometer Assembly (See table 4-19 for next higher assembly)		SDS	116220	Ref
	. Collar, mounting		SDS	111608	1
	. Pulley, reel tachometer		SDS	111598	1

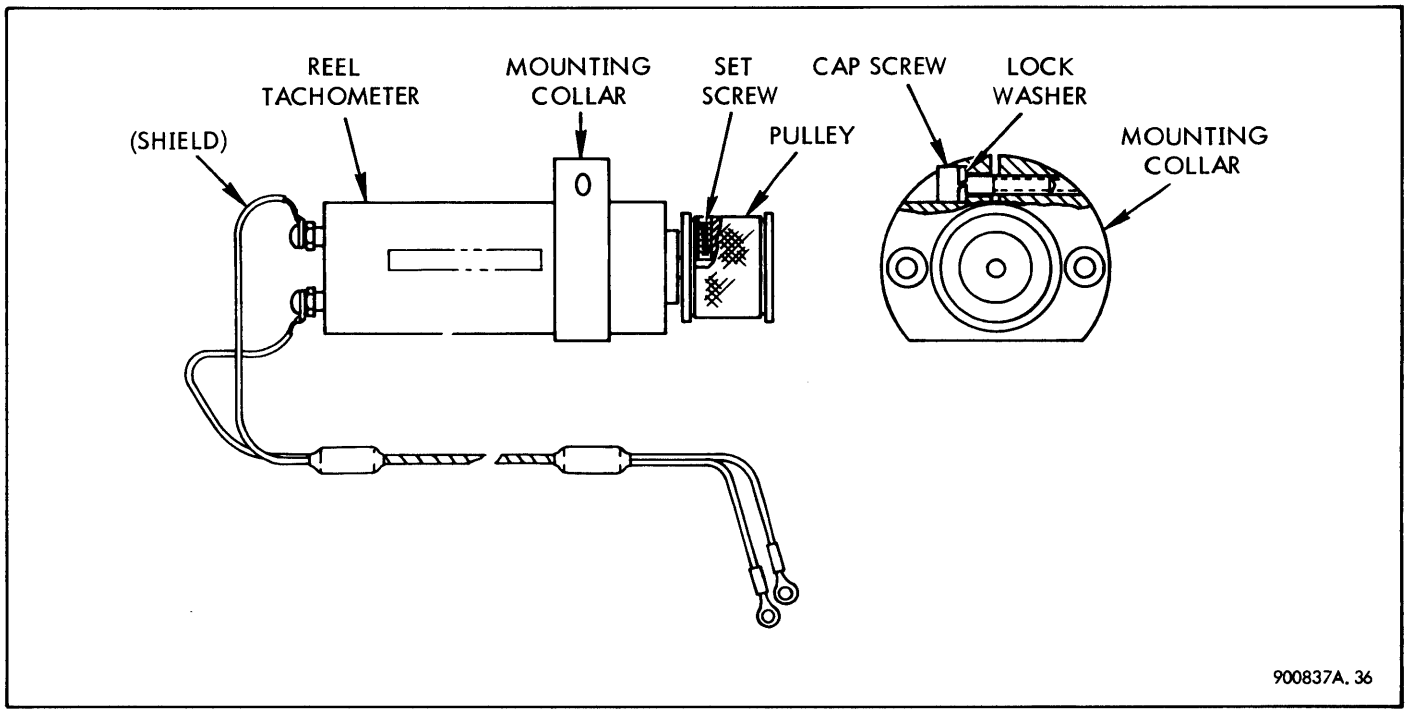


Figure 4-19. Reel Tachometer Assembly

Table 4-25. Fixed Vacuum Chamber Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
4-11	Fixed Vacuum Chamber (See table 4-19 for next higher assembly)		SDS	113485	Ref
	. Switch, vacuum	S1	SDS	113691-400	1
	. Switch, vacuum	S2, S3	SDS	113691-100	2
	. Switch, vacuum	S4, S5	SDS	113691-200	2

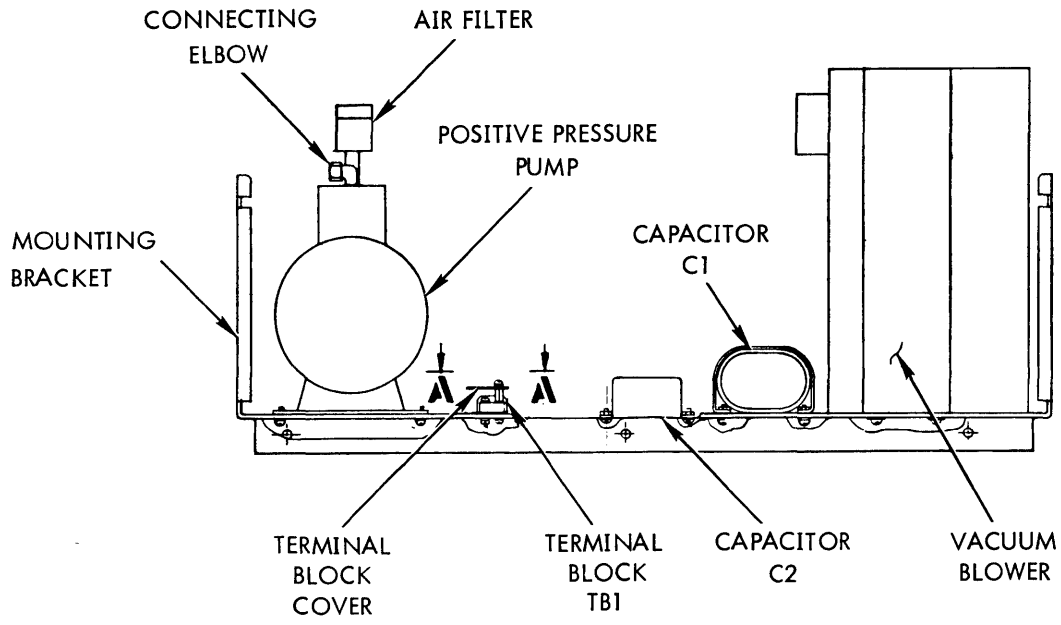
Table 4-26. File Vacuum Chamber Assembly, Replaceable Parts

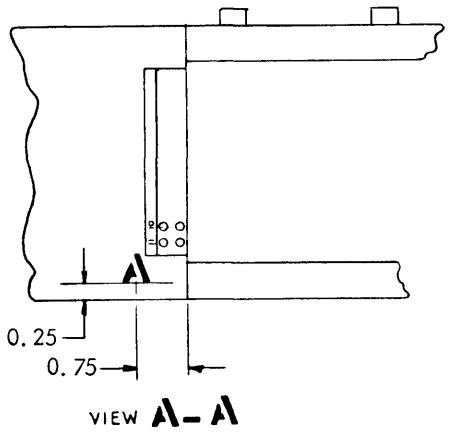
Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
4-11	File Vacuum Chamber (See table 4-19 for next higher assembly)		SDS	114589	Ref
	. Switch, vacuum	S1	SDS	113691-300	1
	. Switch, vacuum	S2, S3	SDS	113691-100	2
	. Switch, vacuum	S4, S5	SDS	113691-200	2

Table 4-27. Blower Shelf Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
4-20	Blower Shelf Assembly (See table 4-18 for next higher assembly) *		SDS	113779	1
	. Block, terminal, molded barrier (SDS 100094-011)	TB1	51	141	1
	. Blower, vacuum		SDS	111843	1
	. Capacitor, ac, 25 μF, 165V, 60 Hz	C1	SDS	135116	1
	. Capacitor, oil impregnated, 1000 Vdc, 120 Vac, 60 Hz, bathtub (SDS 100992-005)	C2	189	CP53	1
	. Elbow, connection (SDS 116702-001)		255	269-P	1
	. Filter, air		362	SYC1Z-1338	1
	. Pump, positive pressure		SDS	111842	1

* See figure 4-21 for schematic



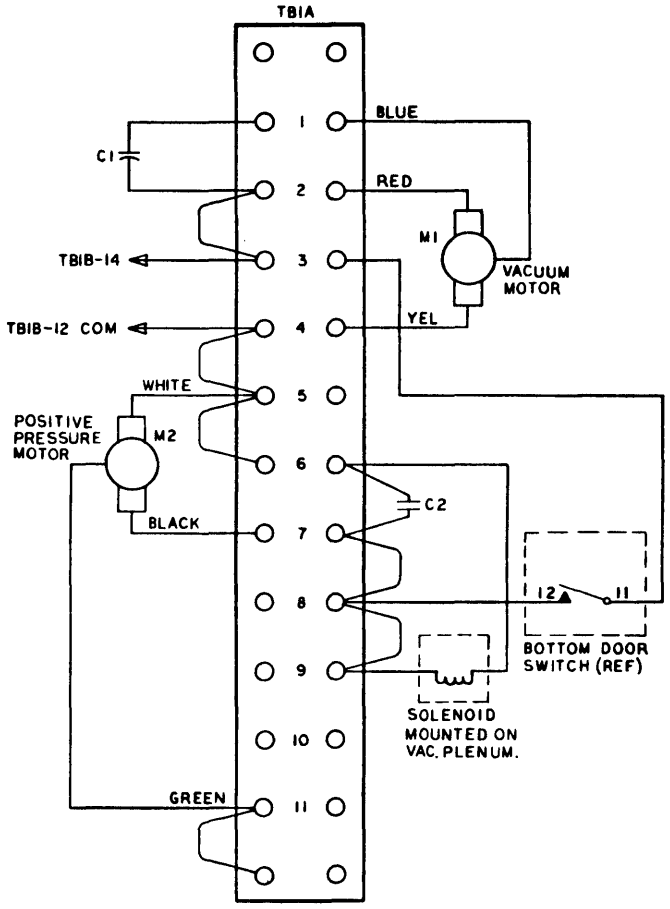


WIRE NO.	TERM	FROM	TO	TERM	WIRE TYPE	
1	(9)	TB1A-E-1	C1A-E-1	SOL	(22)	
2	(9)	TB1A-E-2	C1A-E-2	SOL	(22)	
3	MECH	TB1A-E-2	TB1A-E-3	MECH	(24)	
4	↑	TB1A-E-4	TB1A-E-5	↑	↑	
5	↑	TB1A-E-5	TB1A-E-6	↑	↑	
6	↑	TB1A-E-7	TB1A-E-8	↑	↑	
7	↑	TB1A-E-8	TB1A-E-9	MECH	(24)	
8	↑	B1A-E-BLUE	TB1A-E-1	(7)	—	
9	↑	B1A-E-RED	TB1A-E-2	(9)	—	
10	↑	B1AE-YEL.	TB1A-E-4	(7)	—	
11	↓	B2A-E-WHT	TB1A-E-5	(8)	—	
12	MECH	B2AE-BLK	TB1A-E-7	(8)	—	
13	TAG	KIN-E-1	TB1A-E-6	—	—	} REF
14	TAG	KIN-E-2	TB1A-E-9	—	—	} REF
15	MECH	B2A-E-GRN	TB1A-E-11	8	—	
16	MECH	TB1A-E-11	TB1A-E-GND	MECH	(24)	
17	SOL	C2A-E-1	TB1A-E-6	(9)	(22)	
18	SOL	C2A-E-2	TB1A-E-7	(9)	(22)	

NOTE: REFERENCE SDS DWG: 113779-1G

901084A.604

Figure 4-20. Blower Shelf Assembly



NOTE: REFERENCE SDS DWG: 130776-1B

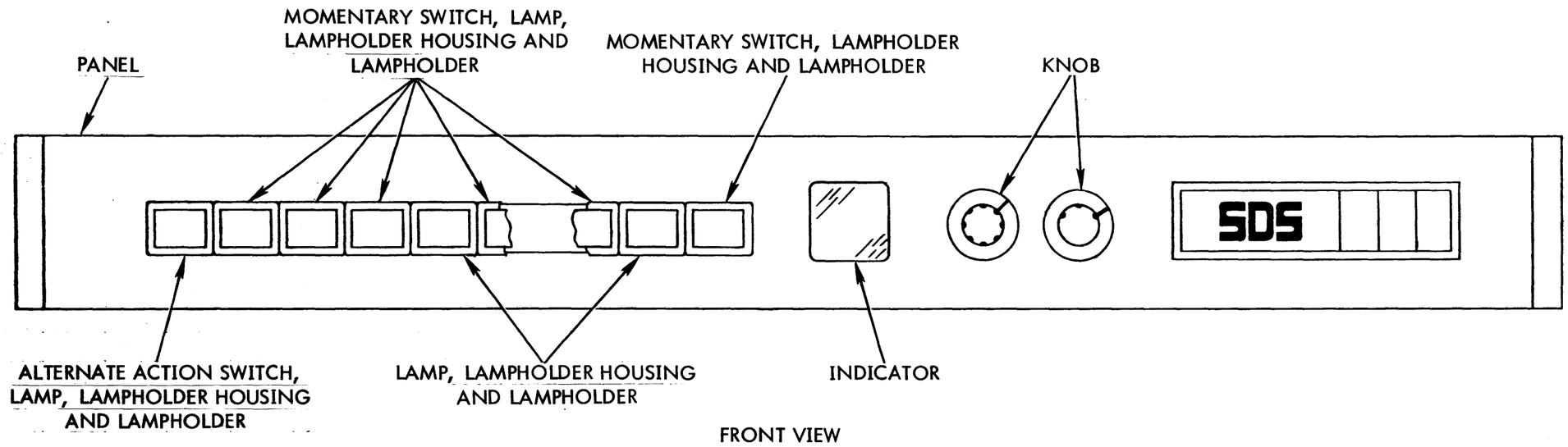
901084A. 703

Figure 4-21. Blower Shelf Schematic

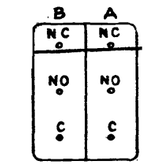
Table 4-28. Operator Control Panel Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
4-22	Operator Control Panel (See table 4-18 for next highest assembly) *		SDS	133666	Ref
	Cable Plug Module Assembly	P206	SDS	133028-023	1
	Board, diode mounting	TB1	SDS	124802	1
	Connector, 14-pin, coax-to-pw board		232	SDS 115833	2
	Diode, silicon, 200V, 750mA (SDS 101154)	CR1-CR7	5	1N3189	7
	Housing, lampholder (SDS 116283-001)		203	10E series	9
	Indicator, segmented, red window (SDS 126619)	DS10	104	700-0135-004	1
	Knob, skirted, black (SDS 126876)		364	PS-70SL-2 Blk	2
	Lampholder, midget, flanged base (SDS 116284-001)		203	10E series	9
	Lamp, incandescent, 28V, midget flanged base (SDS 101922)		83	CM387	16
	Panel, control, mag tape		SDS	133667	1
	Switch, alternate action, dpdt, (SDS 111455)	S1	203	10EF3	1
	Switch, momentary, dpdt, (SDS 111459)	S2, S3, S4, S6, S7, S9	203	10EF1	6
	Switch, rotary, 9-position, 3-deck	S11	55	SDS 129857	1
	Switch, rotary, 3-position	S12	55	SDS 111456-003	1

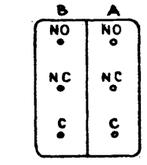
* See figure 4-23 for schematic



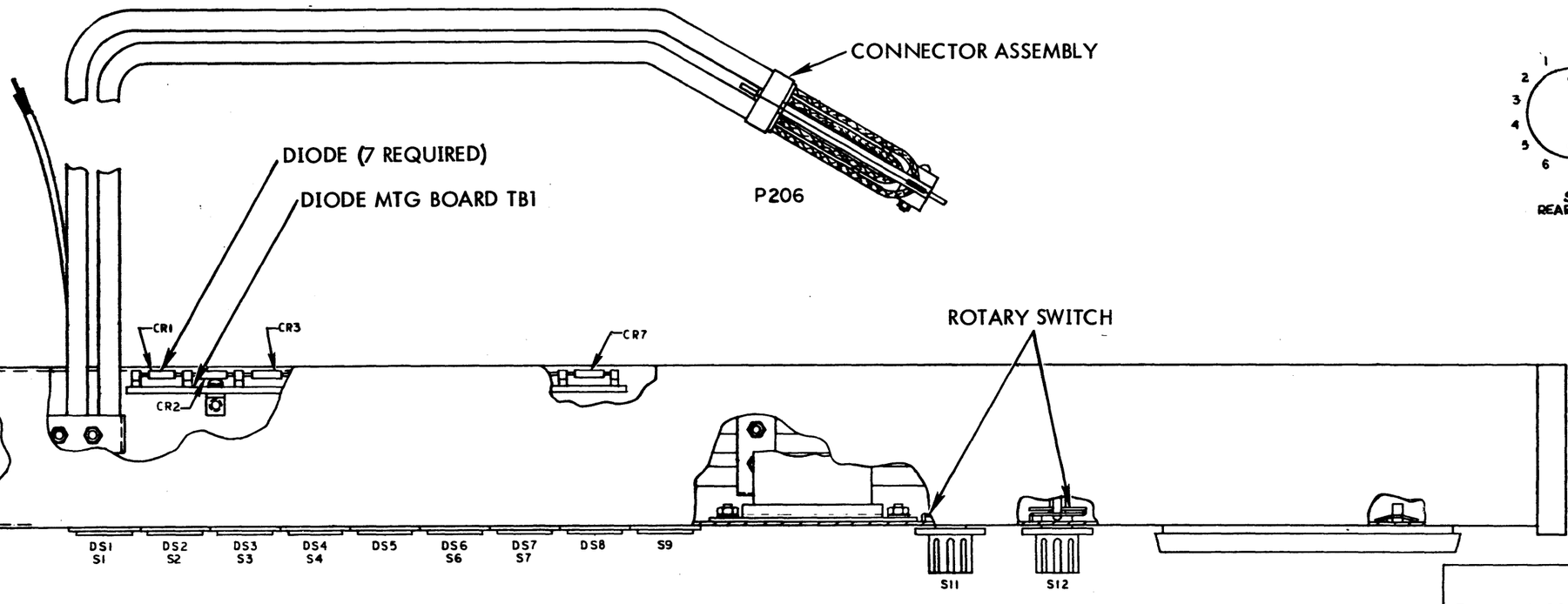
FRONT VIEW



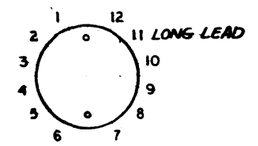
ORIENTATION OF S1
REAR VIEW



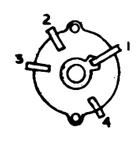
TYP ORIENTATION OF S2, S3, S4, S6, S7 & S9
REAR VIEW



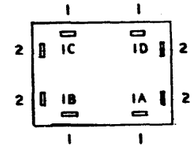
TOP VIEW



S11
REAR VIEW



S-12
REAR VIEW

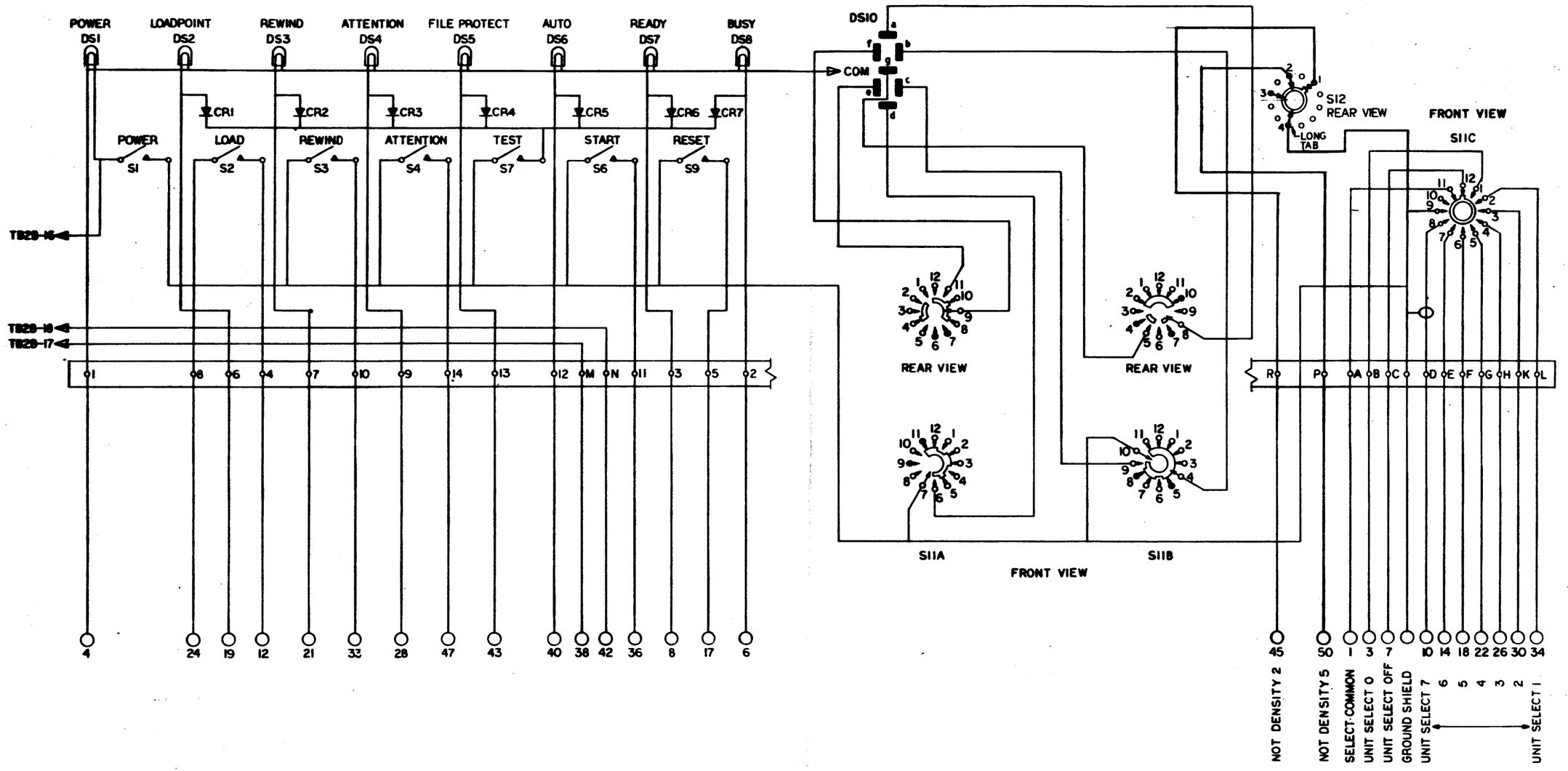


TYPICAL PIN LOCATION OF DS1 THRU DS8

NOTE: REFERENCE SDS DWG: 133666-1G,2E

Figure 4-22. Operator Control Panel Assembly

901013A.406



NOTE: REFERENCE SDS DWG: 1337098

Figure 4-23. Operator Control Panel Schematic

901013A.405

Table 4-29. 28" Cabinet Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
1-1, 1-2	28" Cabinet Assembly (See table 4-18 for next higher assembly)		SDS	124361	Ref
4-24	. Power Distribution Chassis Assembly (See table 4-30 for replaceable parts)		SDS	132365	1
4-25	. Relay Chassis Assembly (See table 4-31 for replaceable parts)		SDS	130409	1
	. Power Supply, PT19		SDS	127160	1
4-27	. Transport Drive Electronics Assembly (See table 4-32 for replaceable parts)		SDS	123120	1
1-2	. Swing Frame Assembly (See table 4-35 for replaceable parts)		SDS	127598	1
	. Filter		SDS	128344	1

Table 4-30. Power Distribution Chassis Assembly, Replaceable Parts

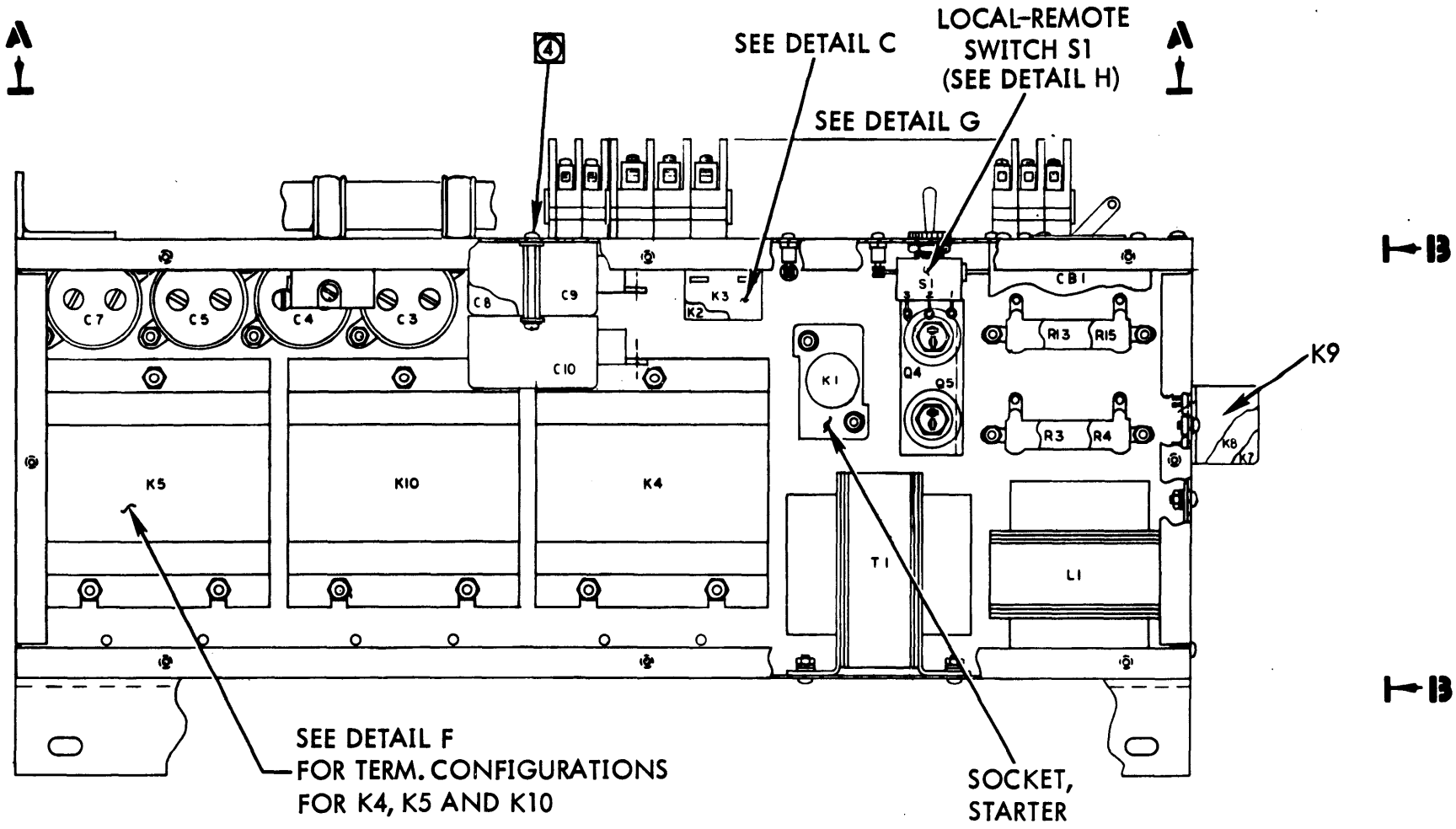
Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
4-24	Power Distribution Chassis Assembly (See table 4-29 for next higher assembly)*		SDS	132365	Ref
	. Assembly, module, board, power control unit		SDS	131982	1
	. Block, terminal, stack (SDS 109432-001)	TB2B	107	1492 series	20
	. Block, terminal, stack (SDS 109432-007)	TB1B	107	1492 series	3
	. Capacitor, electrolytic, 630 μF, large can-type (SDS 108474-018)	C3, C4 C5, C7	25	43F/86F	4
	. Capacitor, all paper, 1μF, 120 Vac bathtub (SDS 100992-005)	C8, C9, C10	189	CP53	3
	. Choke	L1	SDS	132370	1
	. Circuit breaker, 15A, 1-pole (SDS 105016)	CB1	105	AM-12-15 Curve 4	1
	. Clip, retaining (SDS 109432-005)		107	1492 Series	4

* See figure 3-4 for schematic

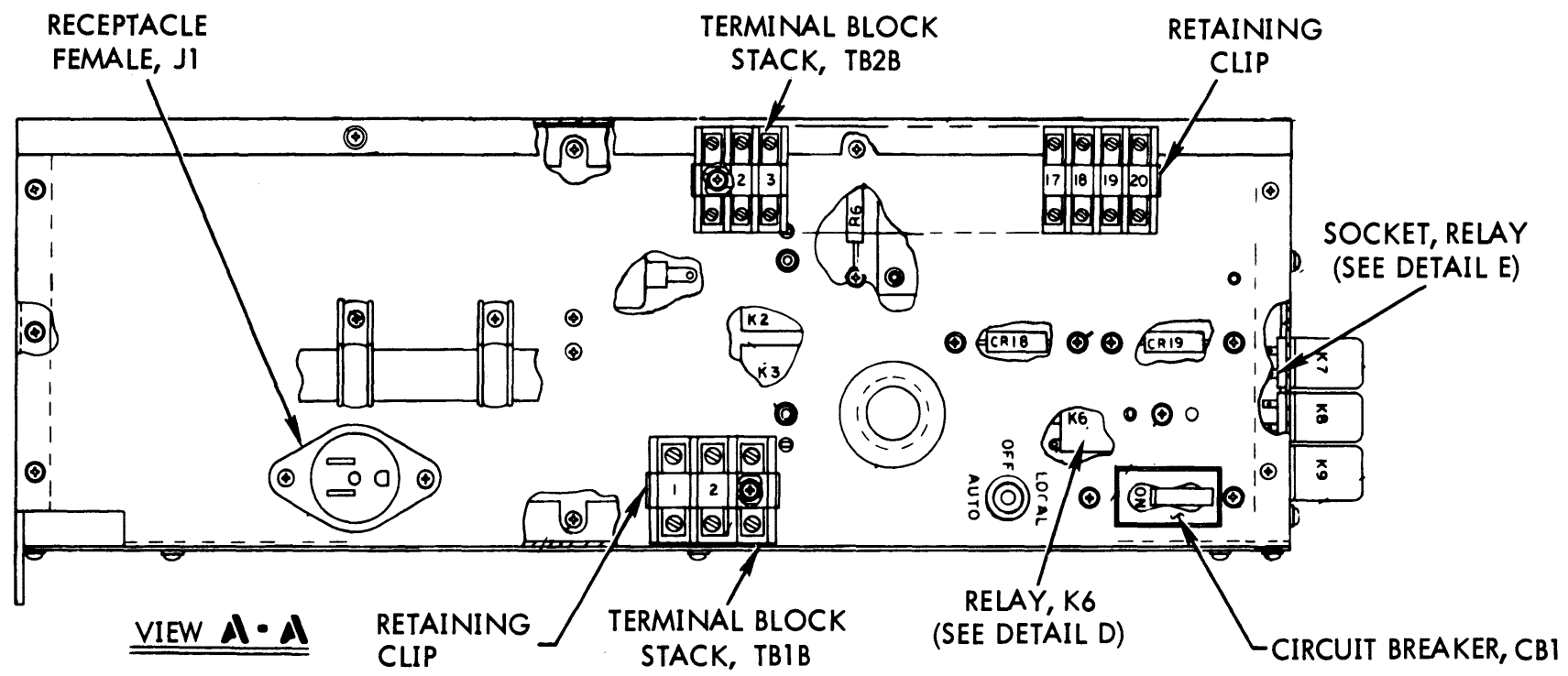
(Continued)

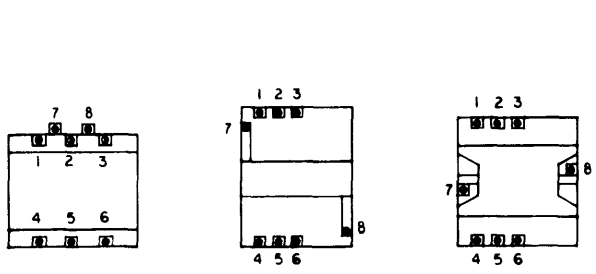
Table 4-30. Power Distribution Chassis Assembly, Replaceable Parts (Cont.)

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
4-24 (Cont.)	. Contacter, 3-pole, 30A, 600 Vac with 120 Vac coil (SDS 130422-001)	K4, K10	106	CRA-130-U 120 Vac XB2001	2
	. Contacter, 3-pole, 30A, 600 Vac with 25 Vac coil (SDS 130422-002)	K5	106	CRA-130-U 24 Vdc XB2000	1
	. Diode, silicon, rectifier, SDS 113, 200V, 750 mA (SDS 101154)	CR18, CR19	5	IN4003	2
	. Receptacle, female, 3-contact, 15A, 125V, grounding type (SDS 101430)	J1	365	5256	1
	. Rectifier, thyristor, SCR, 200V, 16A, SDS 229 (SDS 113977)	Q4, Q5	5	C30BX35	2
	. Relay, dpdt, 10A, 115 Vac coil (SDS 130132)	K2, K3	164	KA3310	2
	. Relay, 24 Vdc coil, dpdt, 5A (SDS 130540)	K6	164	GA11D-24 Vdc	1
	. Relay (SDS 106994)	K7, K8, K9			3
	. Resistor, fixed, 200 ohm 5%, ww, power, 20W, (SDS 101155-201)	R3, R4	244	F203	2
	. Resistor, 470 ohm 2%, fixed film, 1W, (SDS 110996-471)	R6	73	MF7C	1
	. Resistor, 2.5k 5%, ww, power, 20W, (SDS 101155-252)	R13	244	F203	1
	. Resistor, 15 ohm 5%, ww, power, 20W, (SDS 101155-150)	R15	244	F203	1
	. Socket, relay		SDS	106843-001	3
	. Socket, relay, time delay for 129681 (SDS 129682)		366	4309	1
	. Relay, start, thermionic time delay, spst, 115 Vac (SDS 129681)	K1	366	FS2	1
	. Switch, 9V, toggle, dpdt (SDS 130462)	S1	106	83028	1
	. Transformer	T1	SDS	132369	1



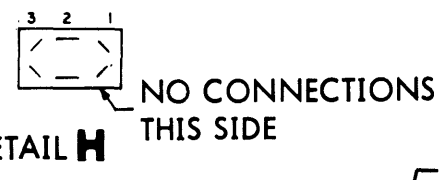
COVER REMOVED FOR CLARITY



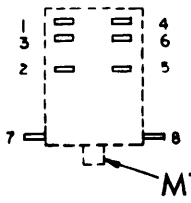


PIN LOCATION ON K4, K5, K10

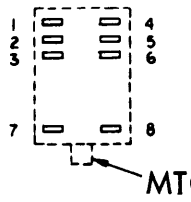
DETAIL F



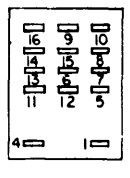
DETAIL H



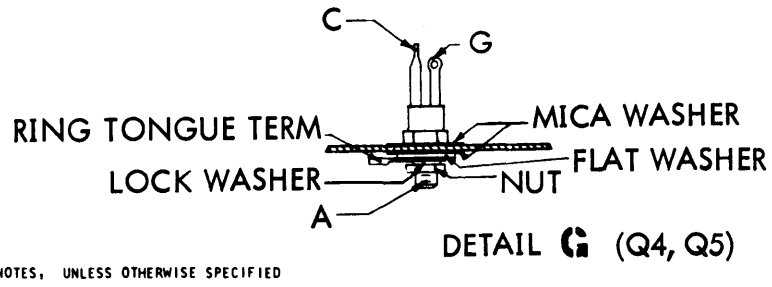
DETAIL C
PIN LOCATION
TYP ON K2, K3



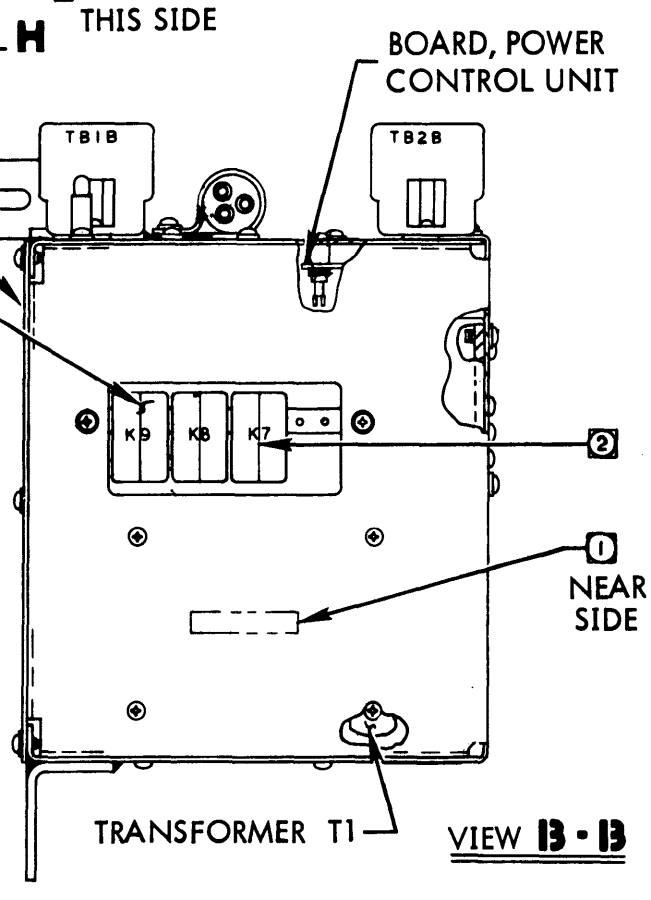
DETAIL D
PIN LOCATION
ON K6



DETAIL E
PIN LOCATION
ON K7, K8, K9



DETAIL G (Q4, Q5)



NOTES, UNLESS OTHERWISE SPECIFIED

1. IDENTIFY PART PER SDS SPEC 100198.
2. INSTALL RELAYS USING SPRING CLIPS SUPPLIED PRIOR TO SUBMITTING TO TEST.
3. MOUNT C10 ON TOP OF C9.
4. REFERENCE SDS DWG: 132365-1D, 2D, 3D
5. FOR SCHEMATIC SEE FIGURE 3-4

ALL CONFIGURATIONS ARE SHOWN
SELECT THE ONE THAT IS APPLICABLE

Figure 4-24. Power Distribution Chassis Assembly

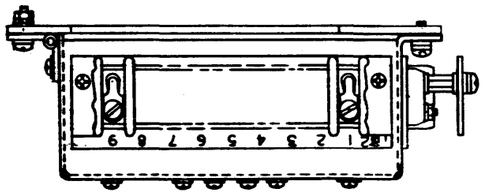
901013A.412

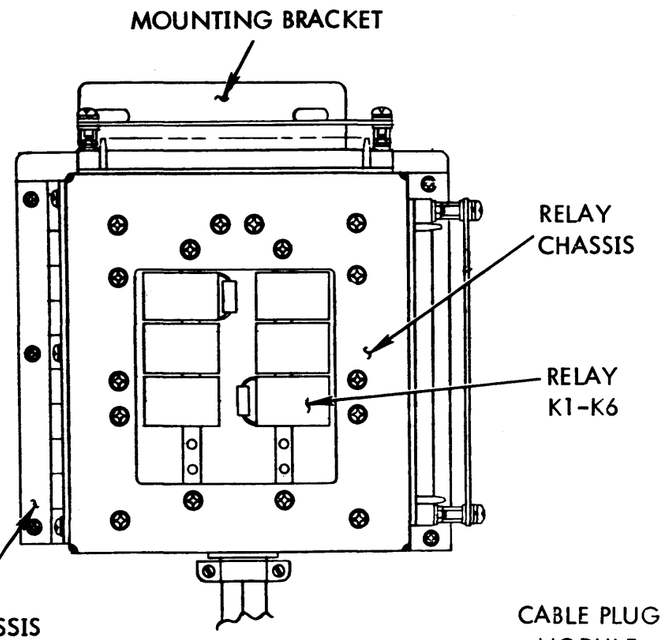
SDS 901013

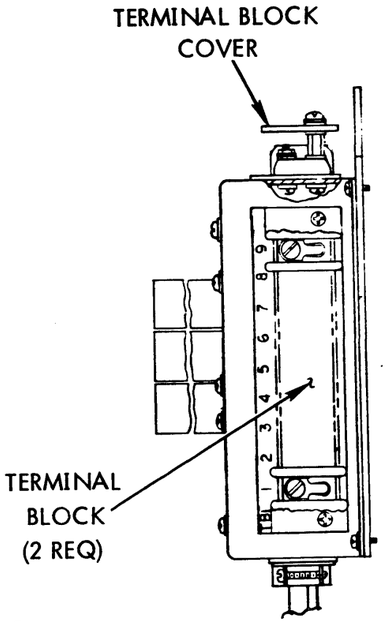
Table 4-31. Relay Chassis Assembly, Replaceable Parts

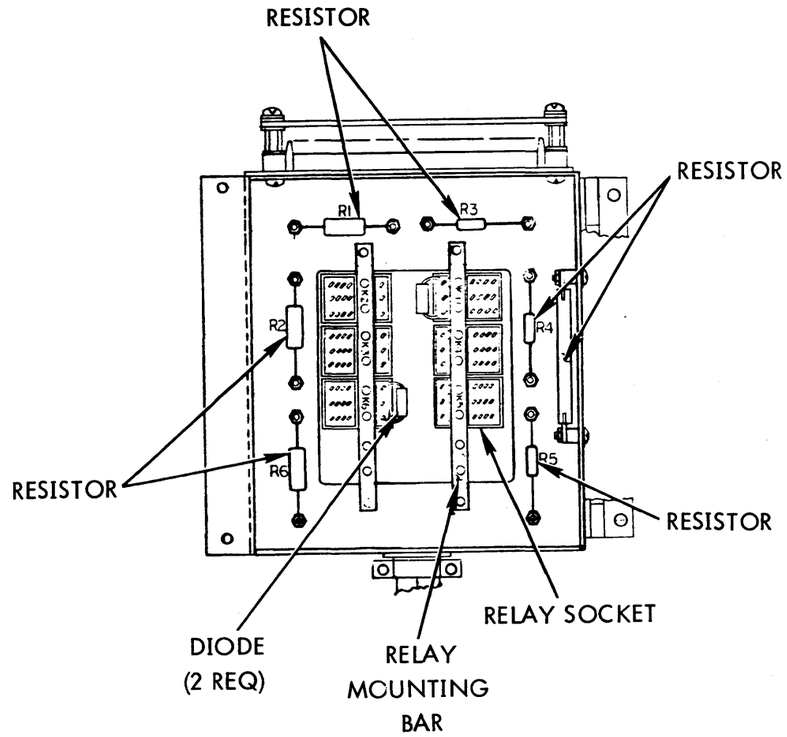
Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
4-25	Relay Chassis Assembly (See table 4-29 for next higher assembly) *		SDS	130409	Ref
	. Cable Plug Module Assembly	P208	SDS	133028-022	1
	. Bar, relay mounting		SDS	130193	2
	. Block, terminal, molded (SDS 100513-009)		51	141-Y	2
	. Bracket, mounting		SDS	130199	1
	. Chassis, relay		SDS	130408	1
	. Diode, silicon, rectifier, SDS 113, 200V, 750 mA (SDS 101154)		5	1N3189	2
	. Hinge, chassis mounting		SDS	130194	1
	. Relay, dc (SDS 106994)	K1-K6		TF-154-4C	6
	. Resistor, fixed film, 1W, 120 ohm (SDS 110996-121)	R1, R2	36	CES-L-32	2
	. Resistor, fixed film, 1/4W 5%, 4.7K (SDS 116447-472)	R3, R4, R5	36	L07, CCM, DM	3
	. Resistor, fixed film, 1W, 1K (SDS 110996-102)	R6	36	CES-L-32	1
	. Resistor, fixed, ww, 20W 5% (SDS 101155-401)	R7	53	8450	1
	. Socket, relay (SDS 106843)		79	30055-4	6

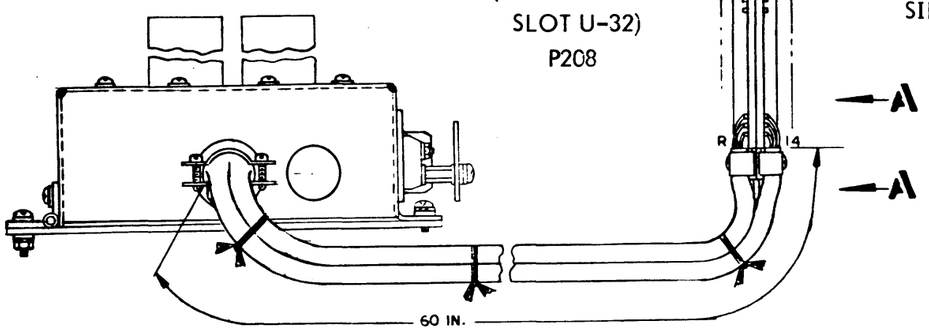
* See figure 4-26 for schematic

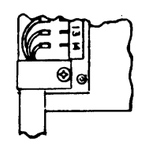








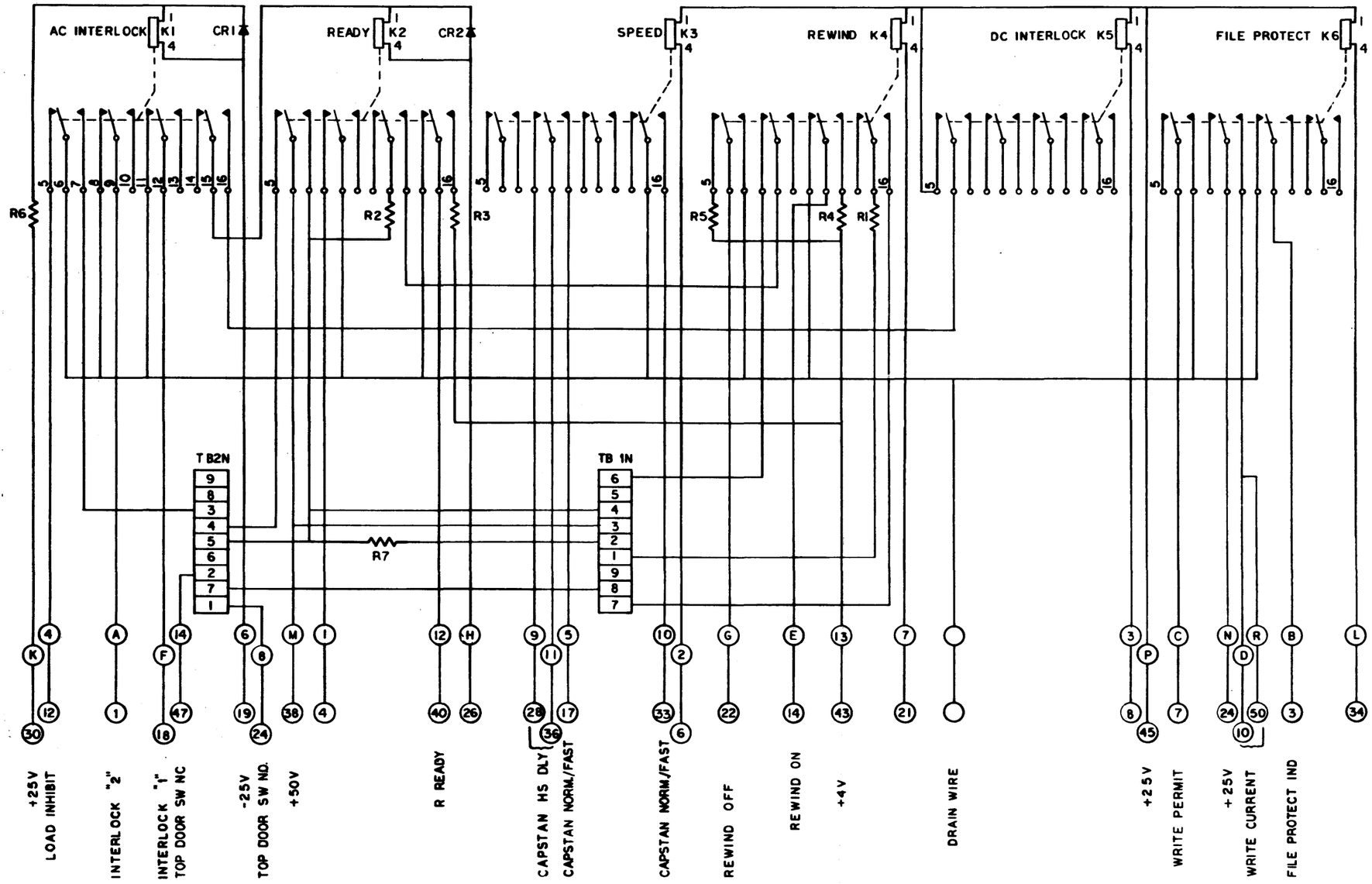




NOTE: REFERENCE SDS DWG: 130409-1C

Figure 4-25. Relay Chassis Assembly

901084A.605



TBIN

1	+80V
2	GROUND
3	
4	READY BRAKE POWER
5	
6	LO SPEED SCR GATE
7	HI SPEED SCR GATE
8	117VAC
9	

TB2N

1	
2	
3	INTLK GROUND
4	$\overline{\text{READY BRAKE POWER}}$
5	
6	
7	
8	
9	

NOTE: REFERENCE SDS DWG: 132413-1A

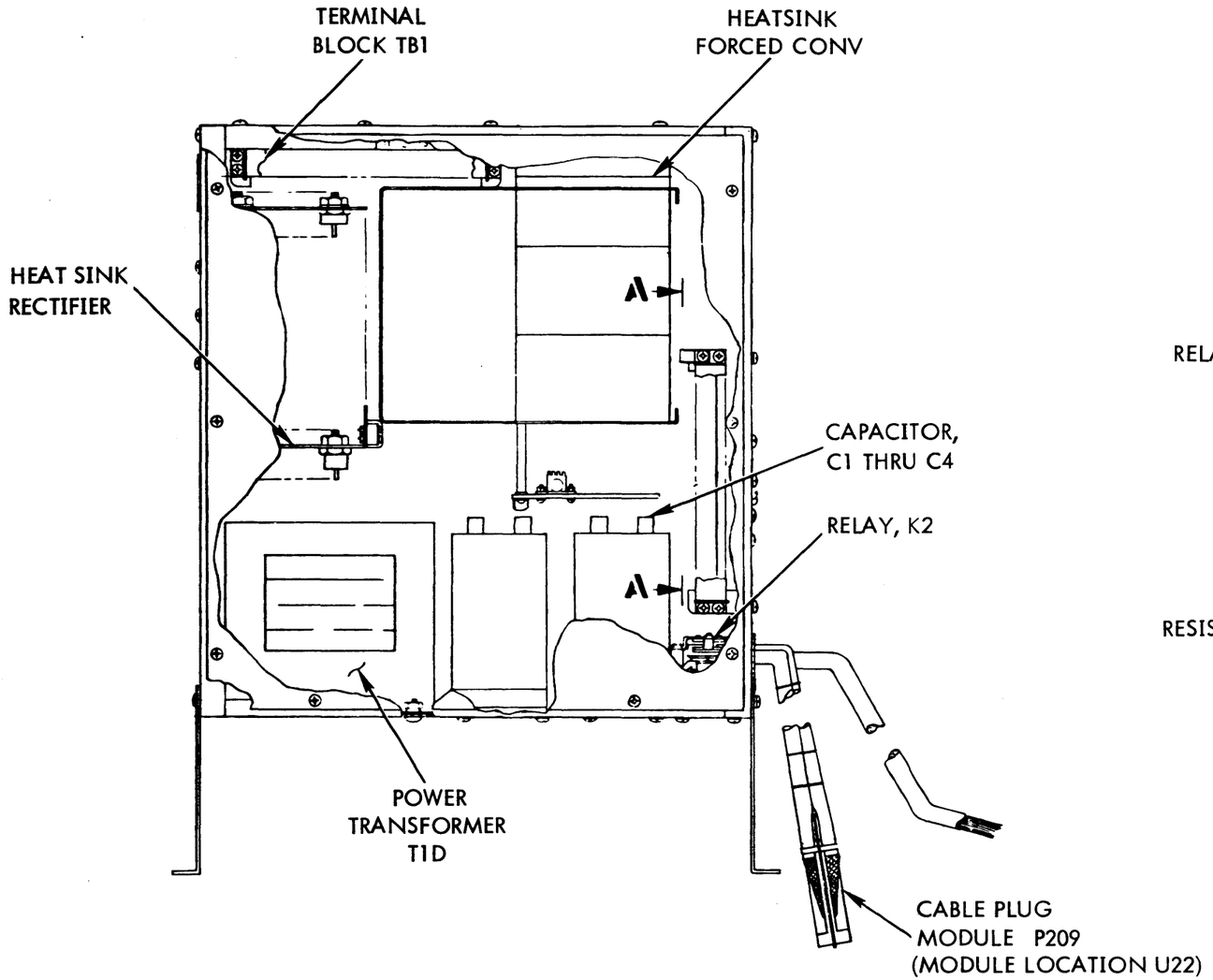
Figure 4-26. Relay Chassis Schematic

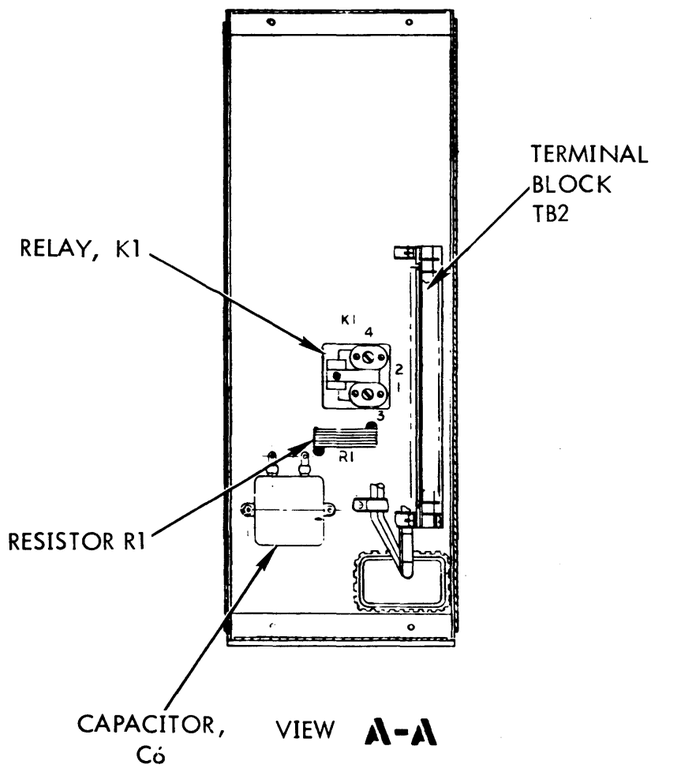
901084A.710

Table 4-32. Transport Drive Electronics Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
4-27	Transport Drive Electronics Assembly (See table 4-29 for next higher assembly) *		SDS	123120	Ref
	. Forced Convection Heatsink Assembly (See table 4-33 for breakdown)		SDS	111671	1
	. Rectifier Heatsink Assembly (See table 4-34 for breakdown)		SDS	115757	1
	. Assembly, cable plug module	P209	SDS	123123	1
	. Block, terminal, molded barrier (SDS 100513-018)	TB1, TB2	51	141-Y	2
	. Capacitor, JC, electrolytic, 65°C, large can-type, 27,000 mfd (SDS 100594-002)	C1D-C4D	25	43F	4
	. Capacitor, oil impregnated, 1000 Vdc, 120 Vac, bathtub (SDS 100992-005)	C6	189	CP53	1
	. Relay, spst, 50A, 115 Vac (SDS 101664)	K1, K2	79	CNAS	2
	. Resistor, fp, fixed, ww (SDS 101517-053)	R1	182	MC-500	1
	. Transformer, power, special	T1D	SDS	113770	1

* See figure 4-28 for schematic diagram

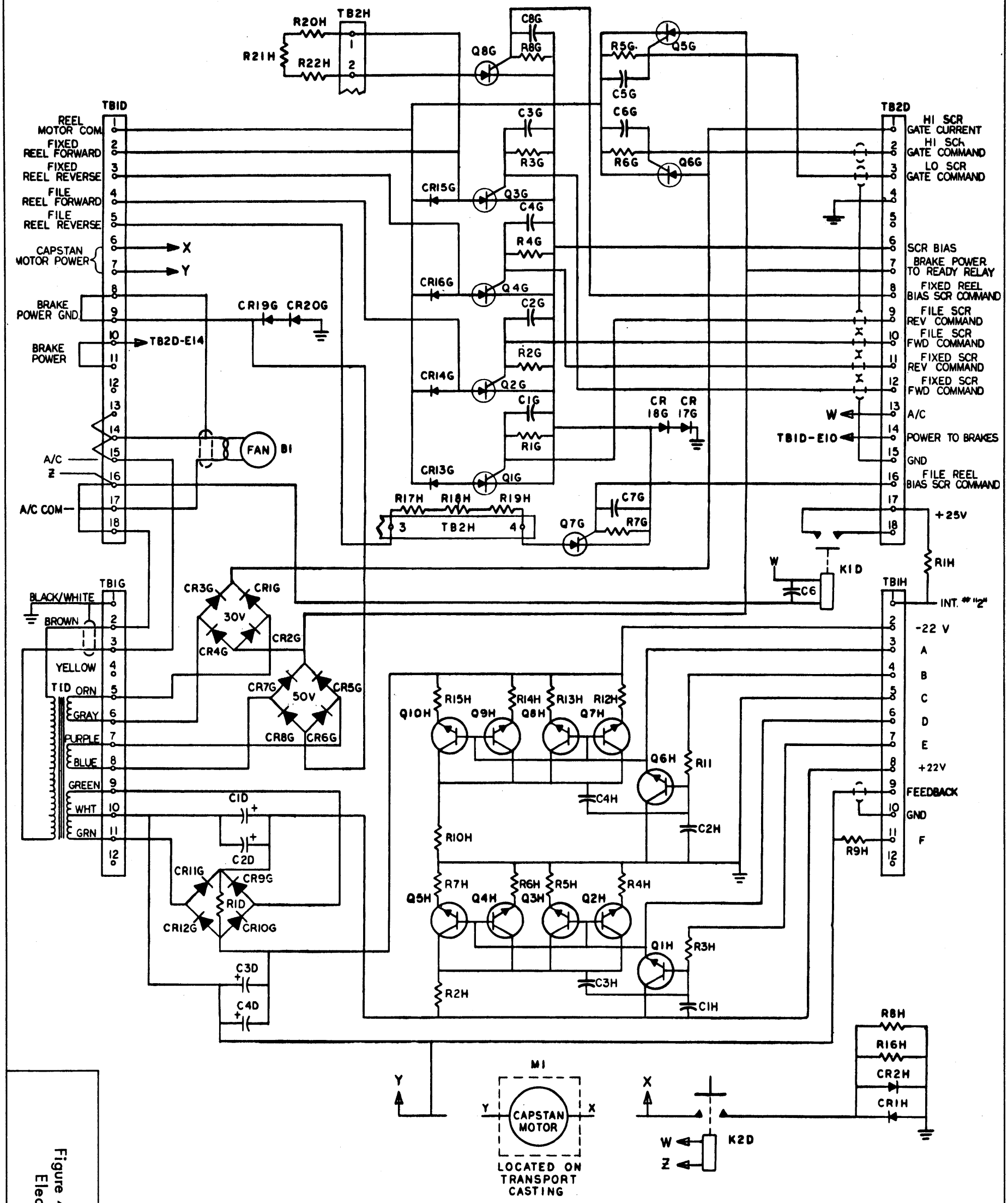




NOTE: REFERENCE SDS DWG: 123120-1D

Figure 4-27. Transport Drive Electronics Assembly

901084A.603



NOTE: REFERENCE SDS DWG: 111448-1C

Figure 4-28. Transport Drive Electronics Schematic

901084A.701

Table 4-33. Forced Convection Heatsink Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
4-27	Forced Convection Heatsink Assembly (See table 4-32 for next higher assembly)	-H	SDS	111671	Ref
	. Capacitor, Mylar, 0.22 µF 10%, 80V (SDS 100308-224)	C1-C2	191	CTM	2
	. Capacitor, Mylar, 0.33 µF 10%, 80V (SDS 100308-224)	C3-C4	191	CTM	2
	. Diode, SDS 121 (SDS 111660)	CR1-CR2	5	A40B	2
	. Fan, cooling, 100CFM (SDS 107742)	B1	144	BS2107F	1
	. Transistor, SDS 225 (SDS 107820)	Q1-Q10	1	2N3055	10
	. Resistor, ww, 110 ohms 1%, 50W	R1, R9	182	MC500	2
	. Resistor, ww, 0.2 ohms 1%, 50W	R2, R4-R7, R10, R12-R15	182	MC500	10
	. Resistor, film 4.7 ohms 5%, 1/2W	R3, R11	36	BW 20	2
	. Resistor, ww, 3.3 ohms 5%, 1W	R16	36	KNR	1
	. Resistor, ww, 10 ohms 1%, 50W	R17-R22	182	MC500	6
	. Resistor, ww, 4.7 ohms 5%, 1W	R8	36	KNR	1

Table 4-34. Rectifier Heatsink Assembly

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
4-27	Rectifier Heatsink Assembly (See table 4-32 for next higher assembly)	-G	SDS	115757	Ref
	Capacitor, Mylar (SDS 100308-334) 0.33 µF 10%, 80V	C1-C8	191	CTM	8
	. Diode, SDS 121 (SDS 111660)	CR1-CR20	5	A40B	20
	. Rectifier, silicon control SDS 236 (SDS 132495)	Q1-Q4	1	2N689	4
	. Rectifier, silicon control SDS 229 (SDS 113977)	Q5-Q8	1	2N685	4
	. Resistor, film, 1k 2%, 1/2W (SDS 100111-102)	R1-R8	96	E009	8

Table 4-35. Swing Frame Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
1-2	Swing Frame Assembly (See table 4-29 for next higher assembly)		SDS	135721	Ref
	. Station Electronics Assembly (See table 4-36 for replaceable parts)		SDS		1
	. Controller Electronics Assembly (See table 4-39 for replaceable parts)		SDS	134049	1
	. Top Fan Assembly		SDS	123943	1
	. Bottom Fan Assembly		SDS	117320	1
	. Power Supply PT18		SDS	127137	1
	. Power Supply PT16		SDS	117264	1

Table 4-36. Station Electronics Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
4-3, 1-2	Station Electronics Assembly (See table 4-35 for next higher assembly)		SDS		Ref
	. Station Electronics Chassis S Assembly (See table 4-37 for replaceable parts)		SDS	116231	1
	. Station Electronics Chassis U Assembly (See table 4-38 for replaceable parts)		SDS	116231	1

Table 4-37. Station Electronics Chassis S Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
	Station Electronics Chassis S Assembly (See table 4-36 for next higher assembly)		SDS	116231	Ref
	. Read Amplifier HT17	S1, S3, S4	SDS	128170	3
	. Cable Plug Module ZT33	S2, S27	SDS	130908	2
	. Buffered Cable Driver AT27	S5, S19, S30, S32	SDS	129862	4
	. Gated Flip-Flop FT12	S6, S8	SDS	117028	2
	. Band Gate BT11	S7	SDS	116029	1
	. Nand/Nor Gate IT11	S9	SDS	116994	1
	. Gated Buffer BT15	S10	SDS	117389	1
	. Cable Driver AT11	S11	SDS	123019	1
	. Line Receiver AT10	S13, S22	SDS	123018	2
	. Logic Element LT36	S14, S15, S16, S17, S18	SDS	131328	5
	. Buffered Cable Driver AT27	S19, S30, S32	SDS	129862	3
	. Switch Module ST14	S20, S25	SDS	123008	2
	. Logic Element LT10	S21	SDS	116017	1
	. Band Gate BT18	S23	SDS	126613	1
	. Write Driver RT11	S24, S29	SDS	128126	2
	. Resistor Module XT15	S26, S28	SDS	128116	2
	. Cable Plug Module ZT33	S27	SDS	130908	1
	. Jumper Module ZT24	S31	SDS	128252	1

Table 4-38. Station Electronics Chassis U Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
	Station Electronics Chassis U Assembly (See table 4-36 for next higher assembly)		SDS	116231	Ref
	Assy, PW, Read Threshold Adjust HT55	U1	SDS	145928	1
	. Gated Buffer BT17	U2, U5, U6	SDS	126330	3
	. Band Gate BT11	U3, U8, U25	SDS	116029	3
	. Basic Flip-Flop FT10	U4	SDS	116380	1
	. Inverter Matrix IT13	U7	SDS	117000	1
	. One-Shot OT14	U10, U11	SDS	129920	2
	. Photosense Amplifier AT28	U13	SDS	130080	1
	. Reference Generator HT12	U14	SDS	123186	1
	. Ramp Generator OT10	U15	SDS	123193	1
	. File Reel Servo HT18	U16	SDS	129849	1
	. Fixed Reel Servo HT19	U17	SDS	129851	1
	. Coast Enable WT16	U18	SDS	129854	1
	. Capstan Preamplifier HT13	U19	SDS	123200	1
	. Power Turn-On Limit WT18	U20	SDS	130474	1
	. Logic Terminator XT10	U21	SDS	116257	1
	. Cable Plug Module P209	U22	SDS	123123	1
	. Cable Plug Module P208	U24	SDS	123118	1
	. Cable Plug Module P206	U27	SDS	115833	1
	. Relay Driver RT14	U28	SDS	132061	1
	. Cable Plug Module P205	U32	SDS	115833	1

Table 4-39. Controller Electronics Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
1-2, 4-3	Controller Electronics Assembly (See table 4-35 for the next higher assembly)		SDS	134049	Ref
	. Controller Chassis V Assembly (See table 4-40 for replaceable parts)		SDS	116231	1
	. Controller Chassis W Assembly (See table 4-41 for replaceable parts)		SDS	116231	1
	. Controller Chassis Y Assembly (See table 4-42 for replaceable parts)		SDS	116231	1
	. Controller Chassis Z Assembly (See table 4-43 for replaceable parts)		SDS	116231	1

Table 4-40. Controller Chassis V Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
	Controller Chassis V Assembly (See table 4-39 for next higher assembly)		SDS	116231	Ref
	. Buffered Cable Driver AT27	V1	SDS	129862	1
	. Buffered Latch FT26	V2	SDS	126856	1
	. Band Gate BT11	V3, V5	SDS	116029	2
	. Band Gate BT18	V4	SDS	126613	1
	. High Speed Count FT11	V6, V7	SDS	117021	2
	. Basic Flip-Flop FT10	V8, V14	SDS	116380	3
	. Logic Element LT10	V9	SDS	116017	1
	. Buffered And/Or Gate BT10	V10	SDS	116056	1
	. Logic Element LT36	V11	SDS	131617	1
	. Parity Generator LT12	V12	SDS	117382	1
	. Gated Flip-Flop FT12	V13	SDS	117028	1
	. Peak Detector FT35	V18, V20, V22, V25, V29, V30	SDS	130178	6
	. Deskew Register FT36	V19, V21, V23, V26, V28, V31	SDS	130187	6
	. Logic Element LT71	V24	SDS	136547	1
	. Cable Receiver AT10	V27, V32	SDS	123018	2

Table 4-41. Controller Chassis W Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
	Controller Chassis W Assembly (See table 4-39 for next higher assembly)		SDS	116231	Ref
	. Ribbon Cable ZT45	W1, W14	SDS	133218	2
	. Gated Flip-Flop FT12	W2, W10 W11, W18	SDS	117028	4
	. Buffered Latch FT26	W3, W12	SDS	126856	2
	. Parity Generator LT12	W4	SDS	117382	1
	. Nand Gate IT18	W5, W24, W25	SDS	126372	3
	. Nand Gate IT11	W6, W15, W26	SDS	116994	3
	. Logic Element LT36	W7	SDS	131617	1
	. Logic Element LT10	W8, W16	SDS	116017	2
	. Delay Element DT16	W9	SDS	128172	1
	. Fast Access Memory FT39	W13	SDS	131072	1
	. Gated Buffer BT15	W17	SDS	117389	1
	. Basic Flip-Flop FT10	W19	SDS	116380	2
	. Clock Oscillator CT10	W22	SDS	123491	1
	. Peak Detector FT35	W23	SDS	130178	1
	. Band Gate BT18	W27	SDS	126613	1
	. Band Gate BT11	W28	SDS	116029	1
	. Logic Element LT71	W29	SDS	136547	1
	. Deskew Register FT36	W30, W31	SDS	130187	2
	. Cable Receiver AT10	W32	SDS	123018	1

Table 4-42. Controller Chassis Y Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
	Controller Chassis Y Assembly (See table 4-39 for next higher assembly)		SDS	116231	Ref
	Ribbon Cable ZT45	Y1	SDS	133218	2
	. Gated Flip-Flop FT12	Y2, Y16, Y17	SDS	117028	3
	. Gated Inverter IT15	Y3	SDS	117375	1
	. Nand Gate IT11	Y4	SDS	116994	1
	. Logic Element LT36	Y5, Y10, Y18, Y19	SDS	131617	4
	. Buffered And/Or Gate BT10	Y7, Y20, Y21, Y22	SDS	116056	4
	. Buffered Matrix BT13	Y9	SDS	116407	1
	. Logic Element LT10	Y11, Y12	SDS	116017	2
	. Band Gate BT11	Y13, Y15	SDS	126613	2
	. Gated Flip-Flop FT12	Y16, Y17	SDS	117028	2
	. Logic Element LT25	Y23	SDS	126712	1
	. Switch Comparator LT26	Y24	SDS	126982	1
	. Cable Driver/Receiver AT17	Y25, Y26	SDS	126714	2
	. Logic Element LT24	Y27	SDS	126710	1
	. Cable Receiver AT10	Y28	SDS	123018	1
	. Logic Element LT41	Y29	SDS	133392	1
	. Cable Driver/Receiver AT11	Y30	SDS	123019	1
	. Logic Element LT43	Y31	SDS	133657	1
	. Cable Driver AT12	Y32	SDS	124629	1

Table 4-43. Controller Chassis Z Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
	Controller Chassis Z Assembly (See table 4-39 for next higher assembly)		SDS	116231	Ref
	. Logic Element LT10	Z1, Z22	SDS	116017	2
	. Buffer Inverter 1, LT13	Z5	SDS	123016	1
	. Basic Flip-Flop FT10	Z6, Z7	SDS	116380	2
	. Band Gate BT11	Z8, Z21	SDS	116029	2
	. Nand Gate IT11	Z9	SDS	116994	1
	. Logic Element LT36	Z10, Z11, Z15, Z16, Z17, Z18, Z19, Z20, Z24	SDS	131617	9
	. Logic Element LT11	Z12	SDS	116324	1
	. Gated Inverter IT20	Z13	SDS	126747	1
	. High Speed Count FT11	Z14	SDS	117021	1
	. Buffered And/Or Gate BT10	Z25	SDS	116056	1
	. Cable Driver AT12	Z26	SDS	124629	1
	. Cable Receiver AT10	Z28	SDS	123018	1
	. Decoder BT12	Z29	SDS	115965	1
	. Gated Buffer BT17	Z30, Z31	SDS	126330	2
	. Cable Driver/Receiver AT11	Z32	SDS	123019	1

Table 4-44. Front Door Assembly, Replaceable Parts

Fig. No.	Description	Reference Designator	Manufacturer	Part No.	Qty
1-1	Front Door Assembly (See table 4-18 for next higher assembly)		SDS	124371	Ref
	. Switch (SDS 114285)		113	K3-4	1
	. Switch (SDS 109372)		162	V3-15	1

Table 4-45. Manufacturer Code Index

Code No.	Name	Address
1	Motorola Semiconductor Products, Inc.	P. O. Box 2953, Phoenix, Ariz. 85002
5	General Electric Co., Semiconductor Product Div.	Electronics Park, Syracuse, N. Y. 13201
25	General Electric Co., Capacitor Dept.	P. O. Box 158, Irmo, S. C. 29063
36	International Resistance Co.	401 N. Board St., Philadelphia, Pa. 19108
51	Cinch Manufacturing Co.	1026 S. Homan Ave., Chicago, Ill. 60624
53	Ohmite Manufacturing Co.	3635 Howard St., Skokie, Ill. 60076
55	Centralab Electronics	900 E. Keefe Ave., Milwaukee, Wisc. 53201
73	Electra Manufacturing Co.	800 North 21, Independence, Kans. 67301
79	Allied Control Co., Inc.	2 East End Ave., New York, N. Y. 10021
83	Chicago Miniature Lamp Works	Dept. E, 4433 Ravenswood Ave., Chicago, Ill. 60640
96	Amperex Electronic Corp.	230 Duffy Ave., Hicksville, N. Y. 11802
104	Dialight Corp.	60 Stewart Ave., Brooklyn, N. Y. 11237
105	Heinemann Electric Co.	2636 Brunswick Pike, Trenton, N. J. 08602
106	Arrow-Hart & Hegeman Electric Co.	103 Hawthorne St., Hartford, Conn. 06106
107	Allen-Bradley Co.	1201 Second St., Milwaukee, Wisc. 53204
113	Controls Co. of America	9655 Spreng Ave., Schiller Park, Ill. 60176
144	IMC Magnetics Corp.	570 Main St., Westburn, N. Y. 11590
162	Honeywell, Micro Switch Div.	11 W. Spring St., Freeport, Ill. 61033
164	Potter & Brumfield, Div. AMF	1200 E. Broadway, Box 322, Princeton, Ind. 47570
182	California Resistor	1631 Colorado Ave., Santa Monica, Calif. 90404
189	Cornell-Dubilier Electronics	50 Ave. "L", Newark, N. J. 07101
191	Dearborn Electronics, Inc.	Box 350, Orlando, Fla. 32802
203	Master Specialties Co.	15020 Figueroa, Gardena, Calif. 90247
244	Hardwick, Hindle Products	Huntington, Ind. 46750
255	Ducommun	4890 S. Alameda, Los Angeles, Calif. 90000
360	Gost Manufacturing, C/O Brenner Fieldler & Assoc.	7563 Melrose Ave., L. A., Calif. 90046
361	United Electrical Controls	423 S. Brookhurst, Anaheim, Calif. 92800
362	Bell and Gossett	8200 N. Austin, Morton Grove, Ill. 60053
363	Precision Lamp Engineers, "Goldlamp" Div.	809 San Antonio Rd., Palo Alto, Calif. 94300
364	Buckeye Stamping Co.	555 Marion Road, Columbus, Ohio 43207
365	Harvey Hubbell, Inc.	Harvey St. & Bostwick, Bridgeport, Conn. 06600
366	Bryant Computer Products	850 Ladd Rd., Walled Lake, Mich. 48088