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Advanced Measurement and Diagnosis Methods

Exercise 3
Signature analysis

Gdansk, 2012

1. Introduction

The aim of the exercise is to become familiar with the method of diagnosis digital circuits using Signature Analysis. The exercise is realized using Signature Analyzer HP 5004A and Signature Analyzer HP 5006A. The programme of the exercise contains measurements of simple and composite signatures in digital circuits (binary counters) and comparison obtained results with theoretical.

2. Signature Analysis

Signature analysis was developed by Hewlett-Packard as a method for both testing and fault finding in complex digital instruments, being suitable for use both within a factory environment and on site. It consists basically of a 16-bit autonomous linear feedback shift register (LFSR), a probe connected to the input exclusive-OR of the LFSR, a hexadecimal numerical display and an appropriate test vector generator, see Fig. 1. In use the following procedure is followed:

- the network under test is first reset to a known initial state, and the LFSR also reset usually to 0 0 0 0,
- the probe is manually applied to a chosen point in the network under test (a primary output or an internal node), and a start signal given which causes a given number of input test vectors to be generated and applied to the circuit, the same number of clock pulses also being applied to the LFSR,
- after the given number of test vectors has been applied a stop signal is generated, and the resulting residual count in the 16-bit LFSR read out as four hexadecimal numbers.

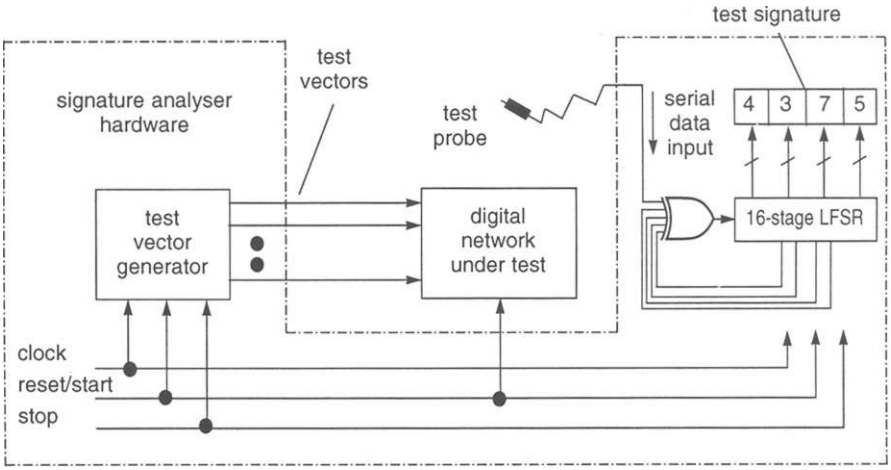
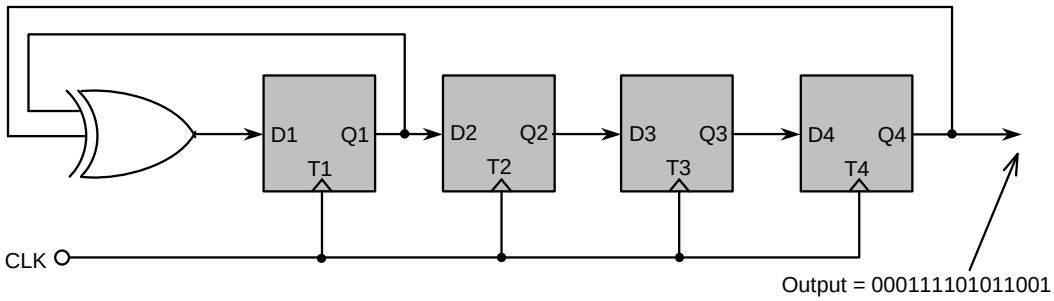


Fig. 1. The signature analysis circuit, where the test probe may be manually applied to any accessible node of the network under test

The final hexadecimal output count of the LFSR is the test signature for the particular node under test. Note that this test gives a compressed signature, since only the residual bits in the LFSR are read at the end of a test and not the full LFSR output sequence. Fault finding is made possible by producing a comprehensive list of fault-free signatures for the nodes in the circuit and comparing them with obtained signatures.

Linear feedback shift register produce a pseudorandom binary sequence (PRBS) of ones and zeroes. However, after some sequence length the pattern repeats. The random-like selection of bits provides nearly ideal statistical characteristics, yet the sequences are usable because of their predictability. A PRBS based upon an n-bit generator may have any length

up to 2^n-1 bits before repeating. A generator that repeats after exactly 2^n-1 bits is termed maximal length. Such a generator will produce all possible n-bit sequences, excluding a string of n zeros. As an example in Fig. 2, let us take the sequence: 000111101011001. This is a fifteen-bit pattern produced by a four-bit maximal-length generator (15 = 2^4-1). If we were to wrap this sequence around on itself, we would notice that all possible non-zero four-bit patterns occur once and only once, and then the sequence repeats.



	Cycle	Q1	Q2	Q3	Q4	D1=Q1⊕Q4
Initial state	0	1	0	0	0	1
	1	1	1	0	0	1
	2	1	1	1	0	1
	3	1	1	1	1	0
	4	0	1	1	1	1
	5	1	0	1	1	0
	6	0	1	0	1	1
	7	1	0	1	0	1
	8	1	1	0	1	0
	9	0	1	1	0	0
	10	0	0	1	1	1
	11	1	0	0	1	0
	12	0	1	0	0	0
	13	0	0	1	0	0
	14	0	0	0	1	1
Begins to repeat	15	1	0	0	0	1

Fig. 2. Four bits LFSR that generates a 15-bit pseudorandom binary sequence

To construct a PRBS generator we look to the realm of linear sequential circuits, which is where the simplest generators reside mathematically. Here there exist only two types of operating elements. The first is a modulo-2 adder, also known as an exclusive-OR gate. The other element is a simple D-type flip-flop, which being a memory element behaves merely as a time delay of one clock period. By connecting flip-flops in series we construct a shift-register as in Fig. 2, and by taking the outputs of various flip-flops, exclusive-ORing them, and feeding the result back to the register input, we make it a feedback shift register that will produce a pseudorandom sequence. With properly chosen feedback taps, the sequence will be maximal length. The fifteen-bit sequence above was produced by the generator in Fig. 2, with the flip-flops initially in the 0001 (Q4, Q3, Q2, Q1) state since the all-zero state is disallowed. The table in Fig. 2 shows the sequence in detail. The list contains each of the fifteen ways of arranging four bits, except four zeros.

If we take the same feedback shift register and provide it with an external input, as in Fig. 3, we can overlay data onto the pseudorandom sequence. The overlaid data disturbs the internal sequence of the generator. If we begin with an initial state of all zeros, and supply a data impulse of 1000..., the result is the same sequence as in Fig. 2 delayed by one clock period.

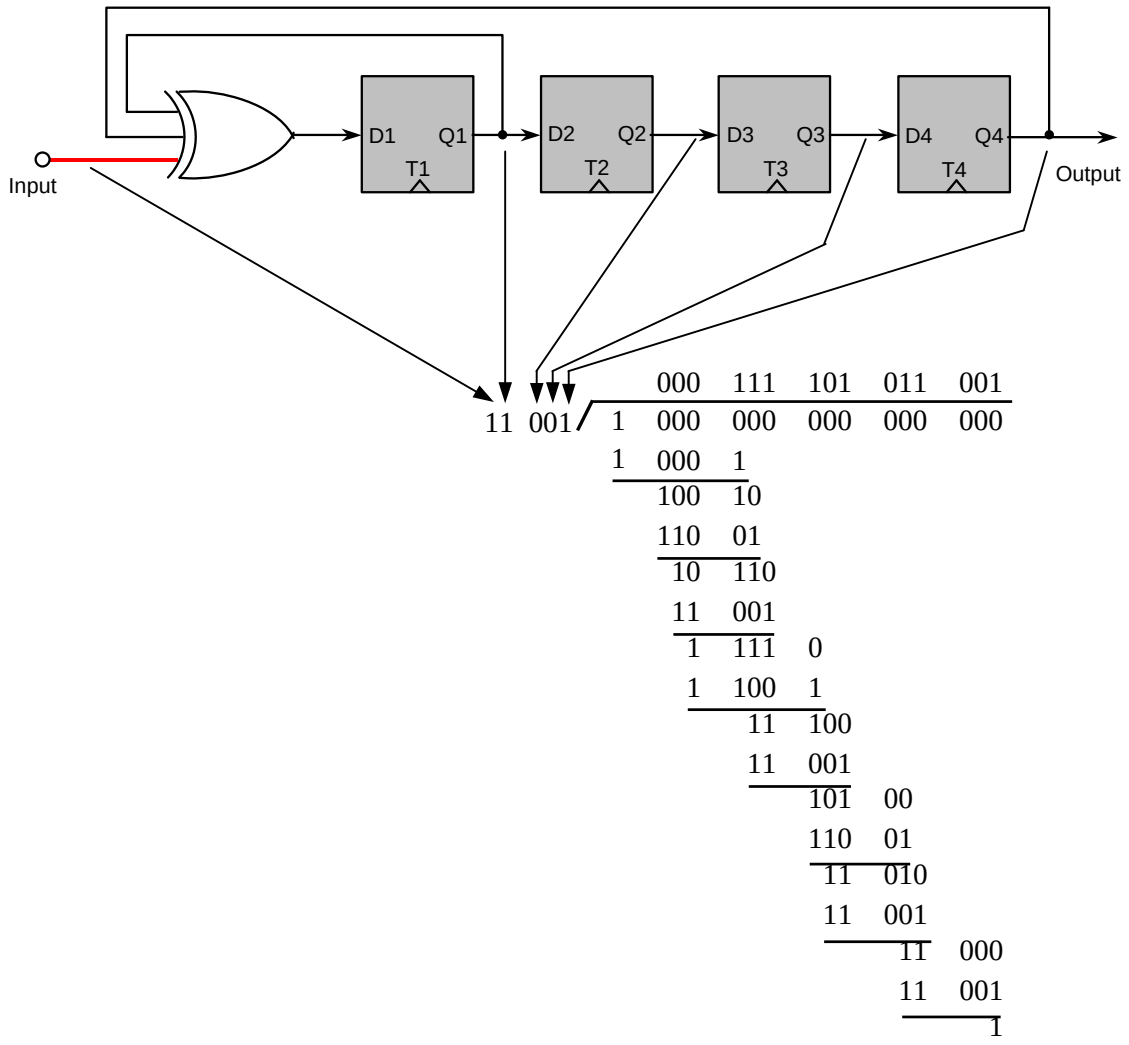


Fig. 3. LFSR with external input which overlay pseudorandom sequence

A shift register may be described using a transform operator D defined such that X(t) = DX(t-l). Multiplying by D is equivalent to delaying data by one unit of time. (Recall that we are concerned only about synchronous logic circuits). In Fig. 3 the data entering the register is the sum of samples taken after one clock period and four clock periods along with the input data itself. Thus, the feedback equation may be written as $F(X)=D^4X(t)+DX(t)+X(t)$ or simply $F(X)=X^4 + X + l$.

It happens that feeding a data stream into a LFSR is equivalent to dividing the data stream by the characteristic polynomial of the generator. For the particular implementation of the feedback shift register considered here the characteristic polynomial is $W(X)=X^4 + X^3 + l$, which is the reverse of the feedback equation. Fig. 3 shows the register along with longhand division of the impulse data stream (100...). Keep in mind that in modulo-2 arithmetic, addition and subtraction are the same and there is no carry. It can be seen that the quotient is

identical to the pattern in Fig, 2 and repeats after fifteen bits (the "1" in the remainder starts the sequence again).

Because the shift register with exclusive-OR feedback is a linear sequential circuit it gives the same weight to each input bit. A nonlinear circuit, on the other hand, would contain such combinatorial devices as AND gates, which are not modulo-2 operators and which would cancel some inputs based upon prior bits. In other words a linear polynomial is one for which P(X+Y) = P(X) + P(Y). Take the example of Fig. 4, where the three different bit streams X, Y, and X + Y are fed to the same LFSR. Notice that the output sequences follow the above relationship, that is, Q(X+Y) = Q(X) + Q(Y). Also, notice that Y is a single impulse bit delayed in time with respect to the other sequences and the only difference between X and X + Y is that single bit. Yet, Q(X + Y) looks nothing like Q(X). Indeed, if we stop after entering only twenty bits of the sequences and compare the remainders, or the residues in the shift register, they would be: R(X + Y) = 0100, R(X) = 0111.

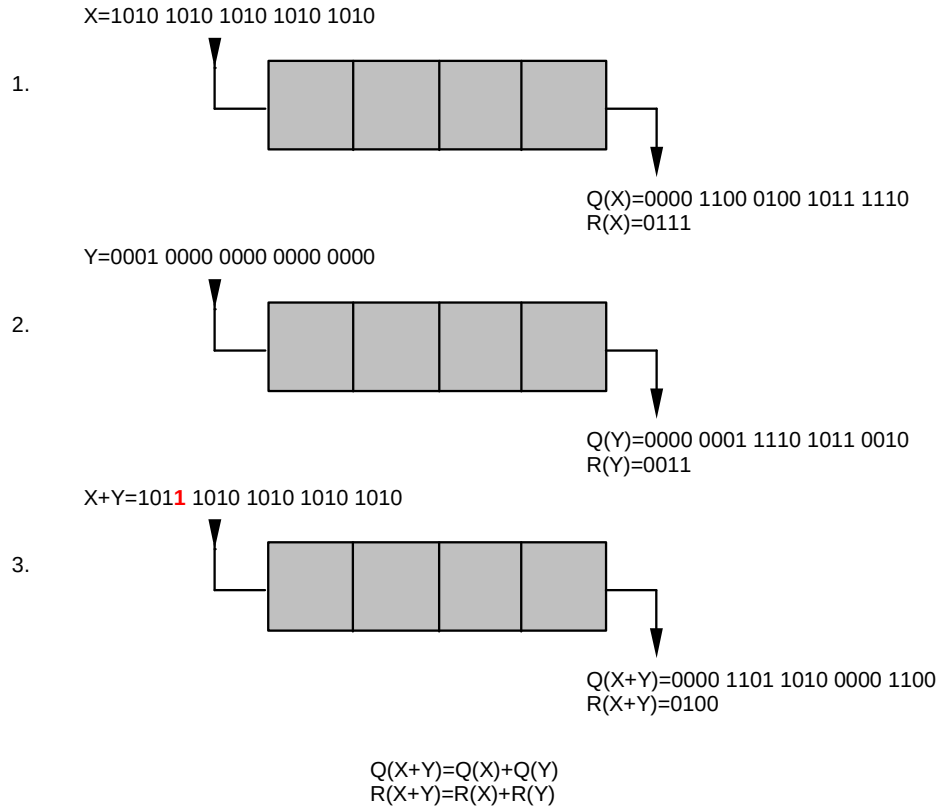


Fig. 4. Three different input data sequence fed to the same LFSR produce very different output sequences

Looking at this example in another manner, we can think of X as a valid input data stream and X + Y as an erroneous input with Y being the error sequence. Any single-bit error, regardless of when it occurs, will always be detected by stopping the register at any time and comparing the remainder bits (four in this case) with what they should be. This error detection capability is independent of the length of the input sequence. In the example of Fig. 4, R(X + Y) differs from the correct R(X), and the effect of the error remains even though the error has disappeared many clock periods ago.

In the case of multiple errors not all errors are detected. Suppose the number of bits in the serial input stream to the LFSR is *m* (which in practice may be the result of some exhaustive input test sequence), and the number of stages in the LFSR is *n*, where $n < m$, then the total number of possible serial input sequences is 2^m, but the number of possible different residual

signatures in the LFSR is only 2^n. Therefore, if all possible faults in the input bit stream are considered to be equally possible, we have one fault-free bit stream and the correct LFSR signature, with 2^m - 1 faulty bit streams of which 2^{m-n}- 1 give the same signature as the fault-free input. The probability of fault masking is therefore given by:

$$P_{al} = \frac{2^{m-n}}{2^m - 1} \cdot 100\%$$

which, if 2^m and 2^{m-n} are both »1, gives:

$$P_{al} = \frac{2^{m-n}}{2^m} \approx \frac{1}{2^n} \cdot 100\%$$

In summary, a LFSR of length *n* will detect all errors in data streams of *n* or fewer bits, because the entire sequence will remain in the register, R(X) = P(X).

For data streams of greater than n bits in length, the probability of detecting, an error using a LFSR is very near certainty even for generators of modest length.

Furthermore, such error detection methods will always detect a single-bit error regardless of the length of the data stream.

It can also be proved that the only undetectable error sequence containing two errors such that the second cancels the effect of the first is produced by separating the two errors by exactly 2^n - 1 zeros.

2.1. Description of HP 5004A Signature Analyzer

The HP 5004A Signature Analyzer is a test instrument for troubleshooting complex electronic logic circuits. It uses the signature analysis technique of troubleshooting.

To use signature analysis with the HP 5004A, the unit to be tested must have certain characteristics included with the original design. Typically a logic product intended for signature analysis troubleshooting will have a programmed controller and a stored short test program that can exercise most of the unit. Usually the test program is started by a "self-test" mode of the instrument. With the test program running, the HP 5004A (connected to the unit being tested) will display a unique hexadecimal signature for each signature analysis test point in the unit being tested.

The HP 5004A requires four signals from the unit being tested: CLOCK, START, DATA, and STOP. The CLOCK signal synchronizes the two instruments. The exactly repetitive START and STOP signals define a window during which the DATA signal is being received by the 5004A. After the STOP signal the 5004A displays the unique hexadecimal signature of the data received.

The HP 5004A Signature Analyzer presents digital signatures with a four-character (symbol) display on its front panel. Each character, which can be any one of 16 symbols, is shown on a 7- segment light-emitting-diode display. The 16 possible characters are shown in Fig.5.:

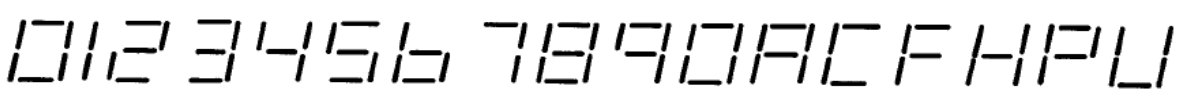
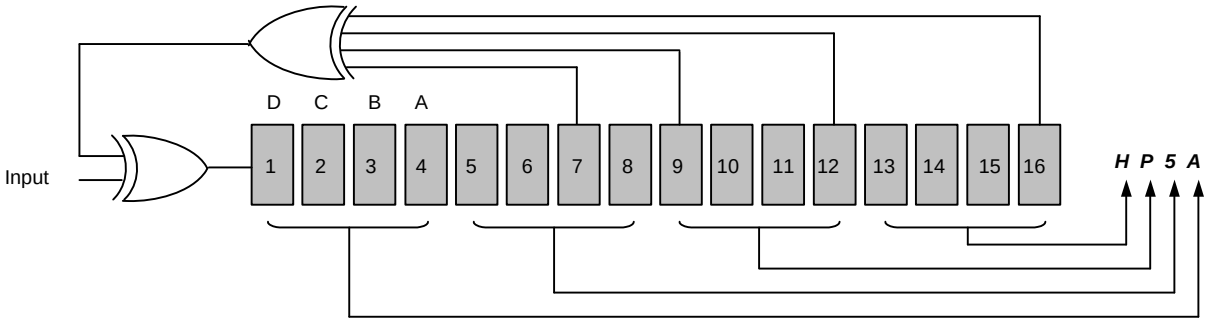


Fig. 5. Characters of HP 5004A display

The characters presented on the display are a hexadecimal number which is the residue of a count in the HP 004A after a START and a STOP signal have been received with some data bits in between. No signature appearing on the HP 5004A display has any particular significance beyond being a correct (expected) signature or an incorrect signature. The number is, however, a count residue in the HP 5004A converted to and displayed in hexadecimal. The four-digit front panel display presents numbers in a special set of hexadecimal symbols as it seen on Fig. 6.



D C B A	display
0 0 0 0	*0*
0 0 0 1	1
0 0 1 0	*2*
0 0 1 1	*3*
0 1 0 0	*4*
0 1 0 1	*5*
0 1 1 0	*6*
0 1 1 1	*7*
1 0 0 0	*8*
1 0 0 1	*9*
1 0 1 0	*A*
1 0 1 1	*C*
1 1 0 0	*F*
1 1 0 1	*H*
1 1 1 0	*P*
1 1 1 1	*U*

Fig. 6. Set of hexadecimal symbols of HP 5004A

Note that the final six symbols are not the common hexadecimal symbols ABCDEF because the seven-segment display of the HP 5004A can not show a B or D that would be different from an 8 or 0 respectively (and several other symbols could be ambiguous).

Front panel of HP 5004A is shown on Fig. 7. Below are described elements of the front panel.

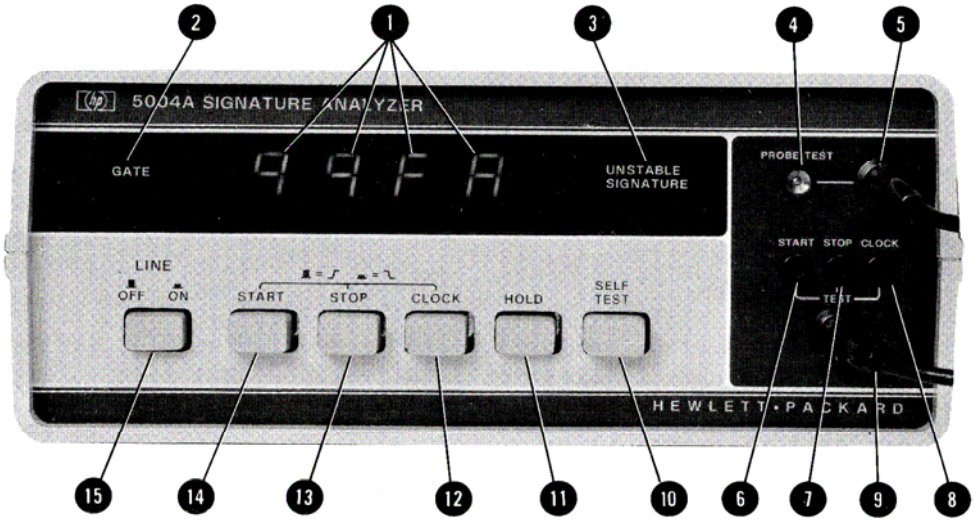


Fig. 7. Front panel of HP 5004A

1. **FOUR-DIGIT DISPLAY** - Shows the unique signature stimulated by the input signals.
2. **GATE** Lamp - Regular blinking of GATE lamp indicates proper START/STOP gating signals.
3. **UNSTABLE SIGNATURE** Lamp - Intermittent or occasional blinking of this lamp indicates a difference between successive signatures inputted to the 5004A.
4. **PROBE TEST** Connector - Test point for 5004A data probe in SELF-TEST mode.
5. **DATA PROBE** - Point of entry for data from unit being tested by 5004A. Lamp near probe tip indicates logic level at tip - On Bright = High. On Dim - Bad-level, Off = Low, 10 ns or greater pulses are stretched to 100 ms. Note side ground connector for fast circuits and RESET switch.
6. **START** Test Point - Test point for the **START** test connector on the active pod in the SELF- TEST mode.
7. **STOP** Test Point - Test point for the **STOP** test connector on the active pod in the SELF-TEST mode.
8. **CLOCK** Test Point - test point for the **CLOCK** test connector on the active pod in the SELF - TEST mode.
9. **Active Test Pod** - Four test inputs **START**, **STOP**, **CLOCK** and a common **GND** (ground) are extended with this active pod for fast rise time signals and low circuit loading.

(10). **SELF-TEST** Switch - When pushed and locked in, this test puts the HP 5004A in the SELF- TEST mode.

(11). **HOLD** Signature Switch - When pushed and locked in, this switch will hold a single, one-time signature for comparison or recording.

12, 13, 14 **CLOCK**, **STOP**, and **START** Switches - These three switches are set to select either the positive-going (▁▕▔) transition or the negative-going (▔▏▁) transition of the respective signals as the active control for that signal. The **CLOCK**, **STOP**, and **START** switches are respectively the active control switches for the **CLOCK**, **STOP**, and **START** test inputs on the active pod.

15 **LINE OFF ON** Switch - This switch controls application of mains line power to the HP 5004A. Line power is applied when the switch is pushed and locked in.

2.1.1. Self-Test mode

The HP 5004A Signature Analyzer has a SELF-TEST (front panel switch) mode which can be used to check the condition of the unit thoroughly. To perform SELF-TEST use the following procedure:

- Remove the grabber connectors from the pod test leads, and connect the pod (START, STOP, and CLOCK) leads to the matching START, STOP, and CLOCK receptacles on the HP 5004A front panel,
- Connect the HP 5004A data probe to the PROBE TEST receptacle on the HP 5004A front panel. Push the probe tip point gently and firmly into the PROBE TEST receptacle until the point is held securely.
- Switch on power source and set the HP 5004A front panel as follows for the displays shown in Table 1.

Table 1. Self Test mode.

Switch Settings			Displays			
START	STOP	CLOCK	Four Seven-Segment (See Note)	GATE	UNSTABLE SIGNATURE	PROBE TIP LIGHT
▁⎺	▁⎺	(▀ ⎍) or (▁⎺)	*UP73* then *ACA2*	flickers	Flickers except when good signature is on	Flickers when "*ACA2*" is on
▀ ⎍	▀ ⎍	(▀ ⎍) or (▁⎺)	3951 then 2P61	flickers	Flickers except when good signature is on	Flickers when "*2P61*" is on

NOTE
In SELF-TEST mode, the four 7-segment displays first have all seven segments lit dimly, 8 for about 1-second (tests all segments) and then have one of the signature sets listed above for about 1-second. If the probe RESET switch is pressed during the SELF-TEST mode, the four 7-segment-digit displays will show 0000 (all zeroes) except when all segments are dimly lit 8888.

2.1.2. Operating Instruction

To perform signature analysis use the following procedure:

- Connect the 5004A START, STOP, CLOCK, and GND test inputs (**9**) on the test pod to the specified test points of the DUT,
- Set the 5004A front panel START (**14**), STOP (**13**), and CLOCK (**12**) (▀ ⎍) (▁⎺) (edge select) switches in proper position. The edge select switches allow flexibility in selection of START and STOP signals. For example, one long pulse can be used for both START and STOP if the rising edge is START and the falling edge is STOP,
- The HOLD (**11**) and SELF-TEST (**10**) switch buttons should normally be in the out position,
- Use the 5004A Data Probe (**5**) to check the signature nodes of the DUT, and compare the signatures found with the nominal signatures of good DUT,

- Especially when slow clock signals are used, the first one or two signatures displayed may be wrong. Two successive identical signatures indicate the signature of that point,
- If most or all signatures are incorrect, check the preliminary settings for given DUT,
- Using the HOLD function (HOLD switch **11**) allows observation of a signature occurring once. (The, DATA PROBE (**5**) RESET switch will erase a HOLD signature).

2.2. Description of HP 5006A Composite Signature Analyzer

The 5006A Signature Analyzer is a test instrument capable of both normal and qualified (QUAL) signature measurements. The 5006A has a maximum clock frequency of 25 MHz. Polarities for the Timing Pod Clock, Start, Stop and Qual inputs are selectable. Input trigger thresholds are preset to standard TTL logic levels (0.8 volts low, 2.0 volts high for Data Probe, and 1.4 volts for the Timing Pod inputs). The thresholds may be modified to CMOS logic levels via a CMOS sense input located on the front panel. In addition to the standard Signature Analysis capabilities, the 5006A features the following unique enhancements to signature measurements:

- Automatic generation of a unique "composite" signature, representative of the set of all signatures intentionally probed since CLEAR or Power-up. This provides a method of verifying the proper operation of an entire IC, bus, or circuit, through a single signature.
- An on-board memory stack which stores up to thirty-two sequential signatures. The signatures in memory can be reviewed, edited, or added-to.
- A selectable Signature Latch function for the display. If enabled, the displayed signature will be held or "latched" in the display until replaced by another triggered measurement or cleared.
- A selectable Unstable Signature Latch function for the UNSTABLE LED. If enabled, a momentary unstable signature will cause the UNSTABLE LED to light and remain lighted until cleared or the function is disabled.
- Input connectors on the front panel to configure the 5006A for a complete operation verification.
- The 5006A is fully programmable, through either the HP-IB or HP-IL optional interfaces. Interface access is provided not only to the current signature, but also the keyboard, the signature memory, and the logic probe light. For example, the user can even use the 5006A as an interfaceable logic probe.

2.2.1. Power-Up Self-Check and Self Test

Power-Up Self-Check

When the 5006A is turned-on, a Power-Up Self-Check cycle is automatically started. **With no inputs** applied to the Data Probe or Timing Pod, the sequence is as follows:

1. After pressing the POWER switch in to switch the instrument from off to on, all the display segments and LED indicators on the front panel and display should light momentarily.
2. After approximately two seconds, the interface address (if installed) will be displayed momentarily, formatted as follows: "Ad.10" for interface address ten.

Successful completion of the power-up self-check is indicated when the front panel assumes its power-up default state; all FUNCTIONS off, the CLOCK, START, and STOP POLARITIES to "rising edge" (indicated by the lighted LEDs above the keys), QUAL polarity to off, and the four dashes (center segments) of the display are lighted. All other front panel LEDs are off.

During this cycle, the microprocessor performs a checksum of the internal program in ROM, and a bit pattern is written into and read from RAM. Problems during the power-up self-check will usually result in a visibly improper state of the front panel display and indicators or the display of a numbered error or failure message. Error messages, which are preceded by "Erxx", can be cleared by pressing the CLEAR key, and the operation reattempted. Failure messages, which are preceded by "F-xx" or an improper power-up display state may also be cleared by pressing the CLEAR key, but typically indicate service is required.

Self-Test

More detailed the operation of the HP5006A may be verified by performing the two-part Self-Test. The first part of the test automatically verifies a majority of the instrument circuitry, **including all cables**, then displays the results as either a "PASS" or "F-xx" (Fail) message. The second part of the test initiates a front panel LED verification cycle, which is activated by the operator by pressing the Data Probe Switch. This test allows each individual front panel LED and display segment to be visually verified. The Self-Test requires no additional equipment.

The procedure of Self-Test is as follows:

1. Turn the 5006A ON, by pressing in the POWER switch.
2. Insert the Data Probe tip into the PROBE test connector on the front panel.
3. Connect the START, STOP, CLOCK, and GND Timing Pod inputs to corresponding POD test connectors on the front panel.

Verify that all front panel LEDs flash (some very briefly) and the display flashes "PASS". The Self-Test cycle is activated when the GND Timing Pod lead is connected. A flashing failure display will appear whenever the GND lead is connected and any of the other leads or the probe tip is not connected. The Self-Test displays should respond as follows:

Table 2. Self-Test response

		Probe Tip	
		Unconnected	Connected
Start, Stop Clock Leads	Unconnected	F-30	F-33
	Connected	F-30	Pass

4. Press the probe Switch and observe the front panel LED test. Verify that each front panel LED and each display segment lights, in sequence.

Problems during the Power-Up Self-Check and Self-Test result in an error or failure condition, detected by the 5006A and identified by a specific numbered message. The 5006A separates problems into two classes; Errors and Failures.

Errors are defined as problems which occur because of the manner in which the instrument is operated, but where no hardware failure is present. These conditions usually indicate an attempted incorrect operation such as an illegal numeric parameter, or an incorrect key operation.

Failures indicate a hardware type problem, and generally require the instrument to be serviced.

2.2.2. Data Probe

The Data Probe has LED lamp and switch (pushbutton) which acts as a trigger signal to the instrument.

The Data Probe tip LED normally operates as a logic indicator, reflecting the electrical activity at the probe tip. The logic state at the tip is sampled over ≈ 100ms intervals. If neither a high nor a low is seen during the interval, the probe LED will be set to DIM (indicating high-impedance). If both a high and a low are seen, the LED will blink on and off to indicate activity. A steady high will cause the LED to turn on BRIGHT, a steady low will cause the LED to turn OFF.

The only time (other than Self-Test) that the probe LED does not operate as a logic indicator is during a triggered signature measurement. After a trigger (probe switch press) is received, the probe LED will turn on BRIGHT (during the measurement). When the measurement is complete, the probe LED will turn off, then resume normal logic activity.

The Data Probe switch (pushbutton) acts as a trigger signal to the instrument. The Data Probe switch is the only instrument key which cannot be locked out by the interface, and is one of only two keys (along with LOCAL) still active while in REMOTE. The Data Probe Switch, as shown in Table 3, is utilized for several functions, depending on the instrument mode of operation.

Table 3. Probe Switch Functions

Mode	Data Probe Switch Function
NORMAL	Initiates a "Triggered" signature measurement which is stored in memory and represented in the Composite Signature
SIG LATCH	Initiates a "Triggered" signature measurement which updates the display. The signature is stored in memory and represented in the Composite Signature.
RECALL	Increments or "rolls" the memory stack through the display. Each keypress decrements the memory one measurement.
EDIT	Initiates; a "Triggered" signature measurement which replaces the last signature stored in memory and recalculates the Composite Signature accordingly. When used with RECALL, initiates a "Triggered" signature measurement which replaces the currently displayed signature in memory and recalculates the Composite Signature accordingly.
SELF-TEST	Shifts the Self-Test Operation Verification sequence from the general PASS/FAIL test to a single segment display verification routine. Each LED and display segment on the front panel is lighted momentarily. When finished, returns to the standard Self-Test routine.

In Normal mode the Data Probe switch is used to select the signatures to be entered into the memory. When the Data Probe switch is pressed during normal operation, the next single measurement to start is known as a "triggered" signature measurement. Triggered signatures are (always) stored into the signature memory, and are the only signatures stored there. Triggered signatures are the only signatures represented in the Composite Signature.

With the SIG LATCH function enabled, the Data Probe switch must be pressed to initiate a "triggered" signature measurement in order to update or change the displayed signature. Only triggered signatures will be displayed with the SIG LATCH function. The Data Probe switch allows the user to make measurements in a "sample and hold" fashion.

While in the RECALL function, the Data Probe switch is used to increment or roll the memory stack through the display. While in the EDIT function, the Data Probe switch is used to trigger a new signature to replace the signature displayed. The new signature acquired after pressing the Data Probe switch assumes the position and reference number of the previously "recalled" signature.

During the Self-Test Operation Verification, the Data Probe switch is used to shift the test sequence to a single segment display verification routine. The Data Probe switch can also be utilized interactively during remote operation.

2.2.3. The 5006A Signature Memory

The 5006A contains a dedicated memory, to accumulate up to thirty-two triggered signatures. In operation, the signature memory acts as a push-down stack. That is, entries are pushed onto the top of the stack. After the stack is full, signatures are lost off the bottom.

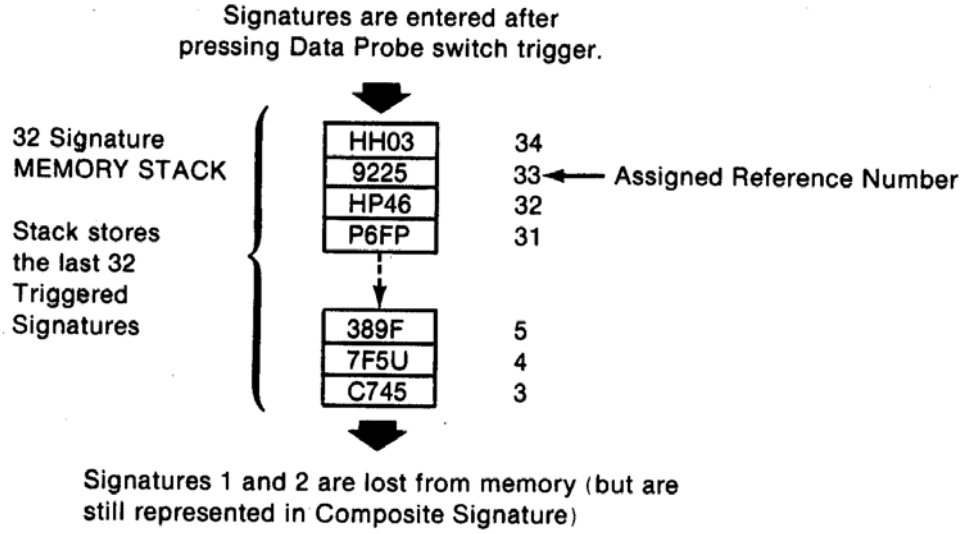


Fig. 8. Signature memory

The 5006A automatically assigns each stored signature a reference number. This number is used to locate the signature during the RECALL or EDIT functions. The signatures are numbered in the order in which they are entered. The first signature is "1", the second is "2", and so on. Numbering continues incrementally even after the memory is full. For example, if thirty-four signatures were entered into the memory (refer to Fig. 8), the most recent entry would be number "34" and the oldest retrievable entry would be "3" (1 and 2 would be lost). Numbering continues until either the memory is CLEARED or the instrument is turned off then on. Only two digits are used for numbering. When the number of stored signatures exceeds 99, only the last two significant digits are displayed on recall.

2.2.4. The 5006A Composite Signature

The 5006A automatically generates a unique Composite Signature after each triggered signature measurement. The Composite Signature is a computed signature, representative of the binary sum of all the triggered signatures accumulated since the last CLEAR or power-up. Only triggered signatures (those preceded by pressing the Data Probe Switch) can affect the Composite Signature. In operation, the Composite Signature is automatically recalculated and updated with each new measurement, based on two factors; the previous Composite Signature and the new triggered signature. In this manner, the Composite Signature remains representative of all signatures taken, even after signatures have dropped off the bottom of the memory stack.

The Composite Signature can be reviewed at any time by pressing the front panel RECALL key. In the RECALL function, the Composite Signature is identified in two ways: the front panel COMPOSITE SIGNATURE LED annunciator lights and all four decimal points in the display light. To return to normal operation press RECALL a second time to turn the function off.

2.2.5. Signature Analysis measurements

Signature Analysis (SA) employs a unique data compression technique that reduces any long, complex data stream pattern on a logic node to a four- digit "signature". The operator supplies the Start and Stop signals to identify the data stream, and a Clock signal to control the sample rate of the probe input.

Signature Analysis Measurements (Normal)

The 5006A makes SA measurements on TTL and CMOS logic families. The trigger thresholds for the inputs are selectable from the standard preset values for TTL logic families, or determined from an external dc input for CMOS. The edge for the Clock, Start, and Stop inputs is selectable using the POLARITY keys. The Start signal is applied to the START/ST/SP (green) Timing Pod lead. The Stop signal is applied to the STOP/QUAL (red) Timing Pod lead. The Clock signal is applied to the CLOCK (yellow) Timing Pod lead, and the measurement is made through the Data Probe.

During SA measurements the front panel GATE LED indicator will flash if there are valid Start and Stop inputs and an active Clock input. The Data Probe tip LED acts as a logic state indicator, lighting "brightly" for a logic high state, "dimly" for a high-impedance state, and "off" for a logic low state. The Data Probe tip LED will "flash" to indicate activity at the node, however the flash duration is controlled by a pulse-stretching circuit and does not reflect the frequency of the input. The UNSTABLE LED will flash if there is a difference between two or more successive signatures.

Signature Analysis Measurements (Qualified)

The Qualified SA mode is selected by pressing the QUAL function key. The Qualified Signature Analysis mode is similar to the normal mode, but with the following enhancement.

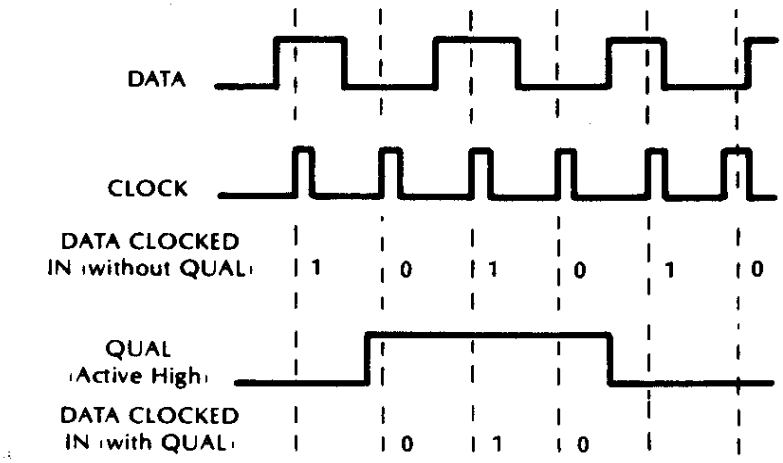


Fig. 9. Signature analysis measurement timing

In this mode, the STOP/ QUAL input on the Timing Pod is sensed as a "data qualifier". Conceptually, the qualifier can be thought of as "enable" signal. By controlling the logic state

of this input, the operator can effectively window the signature measurement within a specific stream of data (Fig. 9).

The trigger thresholds for the inputs are selectable from the standard preset values for TTL, or determined from an external dc input for CMOS. The active edge or level for CLOCK, START, STOP and QUAL, is selectable using the POLARITY keys. When in the QUAL Signature mode, the red Timing Pod lead is the QUAL (qualifier) input, and the green Timing Pod lead is both the START and STOP input. The measurement is made through the Data Probe.

The operation of the GATE, UNSTABLE, and Data Probe tip LEDs during the SA QUAL mode is the same as in SA normal mode.

Signature Analysis Measurements Procedure

The recommended sequence for setting-up and making a measurement with the 5006A is given below.

1. Set the 5006A POWER switch to ON. The 5006A should perform a power-up self-check, then preset to the power-up default settings.
2. Select the desired POLARITY edges for the CLOCK, START, and STOP Timing Pod inputs.
3. Activate the QUAL Timing Pod input, if desired, by pressing the QUAL function key. Select the desired active enable level for the QUAL input with the QUAL POLARITY key; when the QUAL POLARITY LED is lighted, the active enable state is "HI", when the QUAL POLARITY LED is off, the active enable state is "LO".
4. If the circuit logic under test is CMQS, input the CMOS power supply (+3V to +20V) into the front panel CMOS connector.
5. Select the SIG LATCH function, if desired, by pressing the labeled function key. The SIG LATCH function displays only triggered signatures. The function indicator LED above the key should light whenever the function is activated. Select the SIG LATCH function, if desired, by pressing the labeled function key. The SIG LATCH function displays only triggered signatures. The function indicator LED above the key should light whenever the function is activated.
6. If desired, select the UNSTABLE LATCH function by pressing the labeled function key. The UNSTABLE LATCH function monitors the Data Probe input for an unstable signature, latching the front panel UNSTABLE LED on if one is desired.
7. Connect the Timing Pod leads to the appropriate input signals. The GATE LED should be flashing.
8. Touch the Data Probe tip to the desired node. The node signature should be displayed, unless the Signature Latch function is on. To enter the displayed signature into the 5006A memory, press the Data Probe switch.

2.2.6. Front panel indicators and controls of HP 5006A

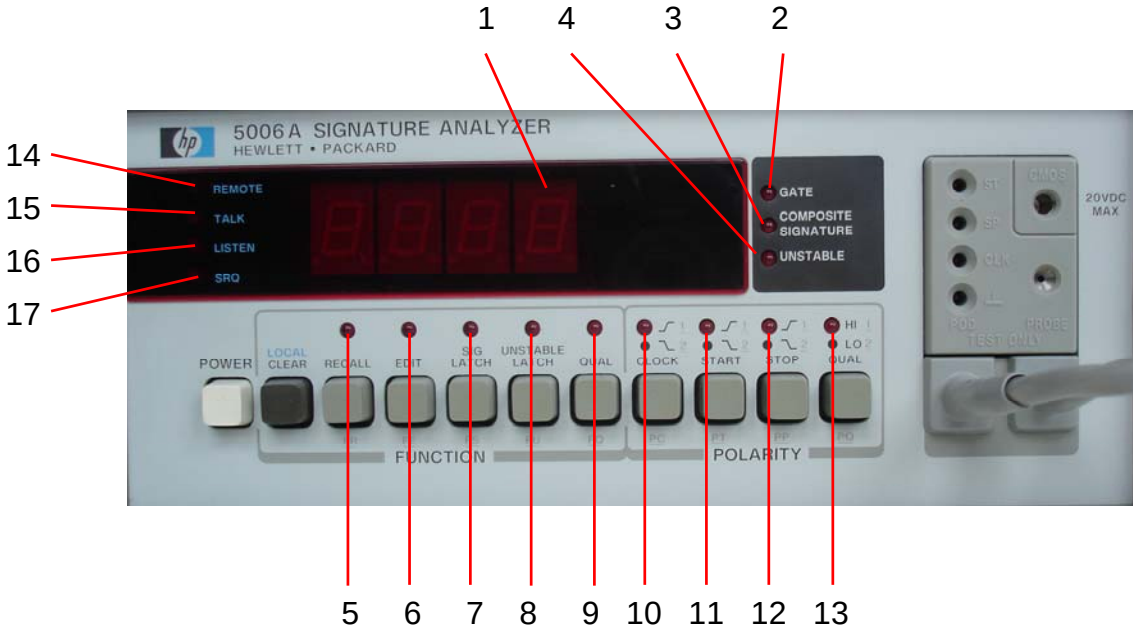


Fig. 10. Front panel indicators of HP 5006A

1**. DISPLAY** - Contains the four seven-segment LED displays.
2. **GATE** LED - Flashing of **GATE LED** indicates the 5006A is being gated. It does not indicate the frequency of the gate cycle.
3. **COMPOSITE SIGNATURE** LED - If lighted, indicates that the signature displayed is the computed Composite Signature derived from all the signatures taken since the last **CLEAR** or **POWER-UP** condition.
4. **UNSTABLE** LED - If lighted, indicates the current signature measurement is different from the previous signature measurement.
5. **RECALL** LED - If lighted, indicates the **RECAL**L function is activated.
6. **EDIT** LED - If lighted, indicates the **EDI**T function is activated.
7. **SIG LATCH** LED - If lighted, indicates the **SIGNATURE LATCH** function is activated.
8. **UNSTABLE LATCH** LED - If lighted, indicates the **UNSTABLE SIGNATURE LATCH** function is activated.
9. **QUAL** LED - If lighted, indicates the **QUAL** function mode of SA is activated.
10. **CLOCK** LED - indicator for the status of the **CLOCK** Polarity. lf lighted indicates rising edge selected, off indicates falling edge.
11. **START** LED - indicator for the status of the **START** Polarity. lf lighted indicates rising edge selected, off indicates falling edge.
12. **STOP** LED - indicator for the status of the **STOP** Polarity. If lighted indicates rising edge selected, off indicates falling edge.
13. **QUAL** LED - indicator for the status of the **QUAL** Polarity. If lighted indicates **HI** level selected, off indicates **LO** level selected. The **QUAL FUNCTION** must be selected for **QUAL POLARITY** to be activated.

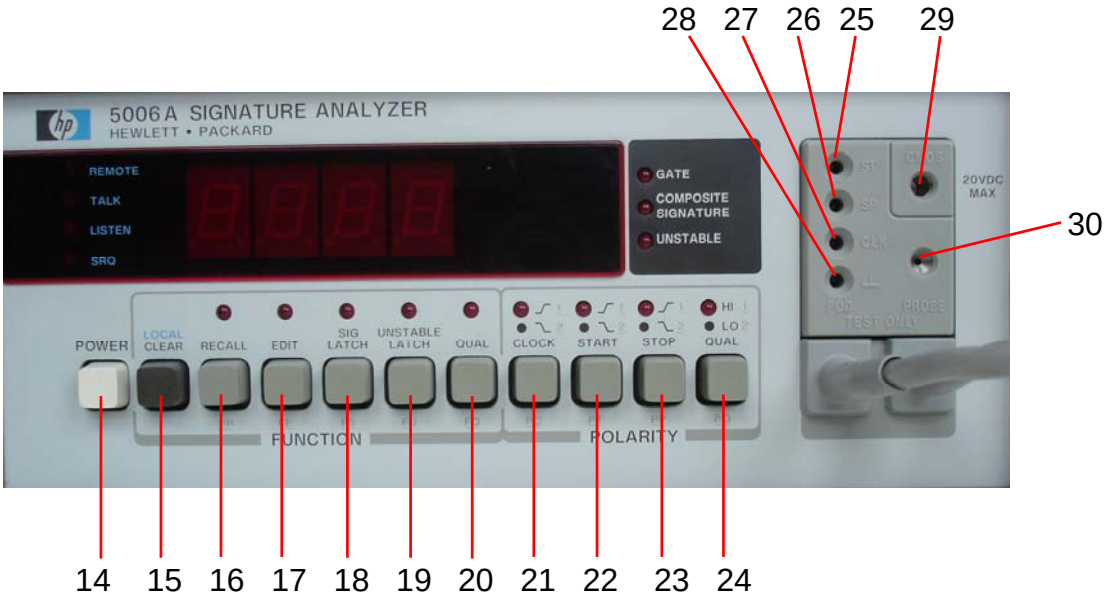


Fig. 11. Front panel controls of HP 5006A

14. **POWER** key - Main power switch for the 5006A.
15. **CLEAR/LOCAL** key - With no Error or Failure displayed, this key will clear the memory of triggered signatures and the **Unstable Signature LED**. In remote operation, with no Error or Failure displayed, this key will return the instrument to "Local" operation and clear the memory of triggered signatures (unless the Local Lockout command has been issued). If an Error or Failure is displayed, this key will clear only the Error or Failure display. Pressing the key a second time will complete the CLEAR and LOCAL function.
16. **RECALL** key - Selects the **RECALL** function. **RECALL** first displays the **Composite Signature**. Pressing the **Data Probe** switch accesses the triggered signatures stored in memory for review or edit, beginning with the most recent entry. Repeated presses of the **Data Probe** switch recall each of the stored signatures in reverse order.
17. **EDIT** key - Selects the **EDIT** function. **EDIT** allows replacement of the last triggered signature in memory, or in conjunction with **RECALL** allows replacement of any stored signature. Replacing a stored signature in memory causes the **Composite Signature** to change.
18. **SIG LATCH** key - Selects the **SIGNATURE LATCH** function, which latches the last signature into the display. The **Data Probe** switch must be pressed to update the display.
19. **UNSTABLE LATCH** key - Selects the **UNSTABLE SIGNATURE LATCH** function, which sets up the **UNSTABLE LED** to light and remain lighted whenever an unstable signature is detected.
20. **QUAL** key - Selects the **QUAL** function mode of SA. In this mode, signature measurement is enabled by either the high (HI) or low (LO) level of the qualifying input signal.
21. **CLOCK** key - Selects the **CLOCK** Polarity. Pressing the **CLOCK** key toggles the current setting of the Clock polarity, indicated by the LED above the key. A lighted LED indicates the rising edge, an unlighted LED indicates the falling edge.
22. **START** key - Selects the **START** Polarity. Pressing the **START** key toggles the current setting of the Start polarity, indicated by the LED above the key. A lighted LED indicates the rising edge, an unlighted LED indicates the falling edge.

23. **STOP** key - Selects the **STOP** Polarity. Pressing the **STOP** key toggles the current setting of the Stop polarity, indicated by the LED above the key. A lighted LED indicates the rising edge, an unlighted LED indicates the falling edge.
24. **QUAL** key - Selects the **QUAL** Polarity. Pressing the **QUAL** key toggles the current setting of the Qual polarity, indicated by the LED above the key. A lighted LED indicates a HI level selected, an unlighted LED indicates a LO level selected.
25. **ST Connector -** Test connector for **START** Timing Pod lead during Operation Verification test procedure.
26. **SP Connector -** Test connector for **STOP** Timing Pod lead during Operation Verification test procedure.
27. **CLK Connector -** Test connector for **CLOCK** Timing Pod lead during Operation Verification test procedure.
28. **GND Connector -** Test connector for ⊥ (**GND**) Timing Pod lead during Operation Verification test procedure. CAUTION: This connector is not connected to chassis ground (⊥) and is not at zero volts.
29. **CMOS Connector -** Input connector for CMOS sense voltage. When using CMOS circuitry, input the corresponding CMOS power supply through this connector to modify the 5006A trigger levels.
30. **PROBE Connector -** Test connector for the Data Probe during Operation Verification test procedure.

3. Prepare for exercise

Check presence of equipment:

1. Signature analyzer HP 5004A
2. Signature analyzer HP 5006A
3. Function generator Agilent 33210A
4. Board with Device Under Test

4. Laboratory tasks

4.1. Signature Analyzer HP 5004A

4.1.1. Self-Test of HP 5004A Signature Analyzer

Remove the banana connectors from the pod test leads, and connect the pod (START, STOP, and CLOCK) leads to the matching START, STOP, and CLOCK receptacles on the HP 5004A front panel,

Connect the HP 5004A Data Probe to the PROBE TEST receptacle on the HP 5004A front panel. Push the probe tip point gently and firmly into the PROBE TEST receptacle until the point is held securely.

Switch ON the power source

Set the HP 5004A front panel switches in the following manner:
START - ■ ⎍
STOP - ■ ⎍
CLOCK - ■ ⎍
Switch on the **TEST-SELF** switch and note signatures from display.

Repeat Self-Test sequence for
START - ▁◹
STOP - ▁◹
CLOCK - ■◹

and note signatures from display.
Compare obtained results with Table 1. Does the analyzer work properly?

4.1.2. Signature Analysis measurements with HP 5004A

Connect the HP 5004A START, STOP, CLOCK, and GND test inputs on the Test Pod to the specified test points of the DUT according to Fig. 12.

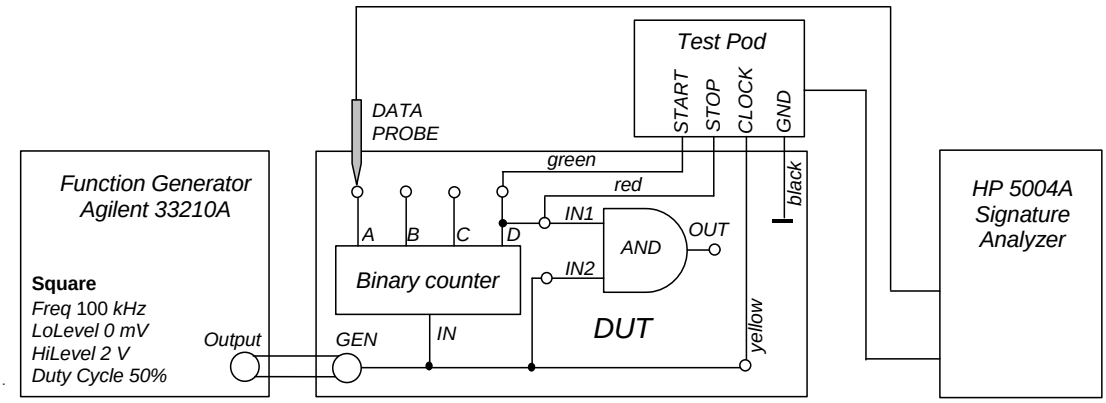


Fig. 12. Signature Analysis measurements with HP 5004A

According to Table 4 and Fig. 7 set the 5004A front panel START (**14**), STOP (**13**), and CLOCK (**12**) (■◹) (▁◹) (edge select) switches in proper position. Using Data Probe measure signatures on outputs of binary counter and note results in Table 4.

Table 4. Signature analysis measurements with HP 5004A

Switch Settings			Signatures			
START	STOP	CLOCK	A	B	C	D
■◹	■◹	■◹				
▁◹	▁◹	■◹				
▁◹	■◹	■◹				
■◹	▁◹	■◹				

Unstable signatures

Set START, STOP and CLOCK edge select switches in position ■◹. Connect Data Probe to OUT of AND gate and measure signature observing Unstable Signature LED. Is this signature stable?

Hold mode

Leave START, STOP and CLOCK edge select switches in position ⊓⌐. Connect Data Probe to output **C** of binary counter.

Switch off function generator Agilent 33210A using **Output** key (do not use the Power switch). Switch on HOLD key in HP 5004A and reset old signature using Data Probe RESET switch.

Switch on function generator Agilent 33210A using **Output** key and note obtained signatures. Repeat 3 times the above sequence. Are all signatures the same?

Switch on function generator Agilent 33210A. Observe signatures on output C of binary counter in mode HOLD disconnecting and then connecting DUT to 230 V line. Are signatures the same in this case?

4.2. Signature Analyzer HP 5006A

4.2.1. Self-Test of HP 5006A Signature Analyzer

Power-Up Self-Check

Disconnect all signals from Data Probe and Timing Pod. Press the POWER switch ON to start a Power-Up Self-Check cycle. Observe Power-Up Self-Check sequence and compare it with the correct one (page 10).

Self-Test

1. Turn the 5006A ON, by pressing the POWER switch. Insert the Data Probe tip into the PROBE test connector on the front panel. Connect the Timing Pod inputs to corresponding POD test connectors on the front panel:

   START (green) to ST,

   STOP (red) to SP,

   CLOCK (yellow) to CLK,

   GND (black) to ⊥.

   Switch on the **TEST-SELF** switch and verify that all front panel LEDs flash and the display flashes "PASS".

2. Disconnect Data Probe tip from the PROBE test connector and then disconnect the Timing Pod inputs START, STOP, CLOCK from Pod test connectors. Compare Self-Test displays response on the front panel with Table 2 on page 11.

3. Press 2 seconds the Probe Switch and observe the front panel LED test. Verify that each front panel LED and each display segment lights in sequence.

4.2.2. Signature Analysis measurements with HP 5006A

Connect the HP 5006A START, STOP, CLOCK, and GND test inputs on the Test Pod to the specified test points of the DUT according to Fig. 13.

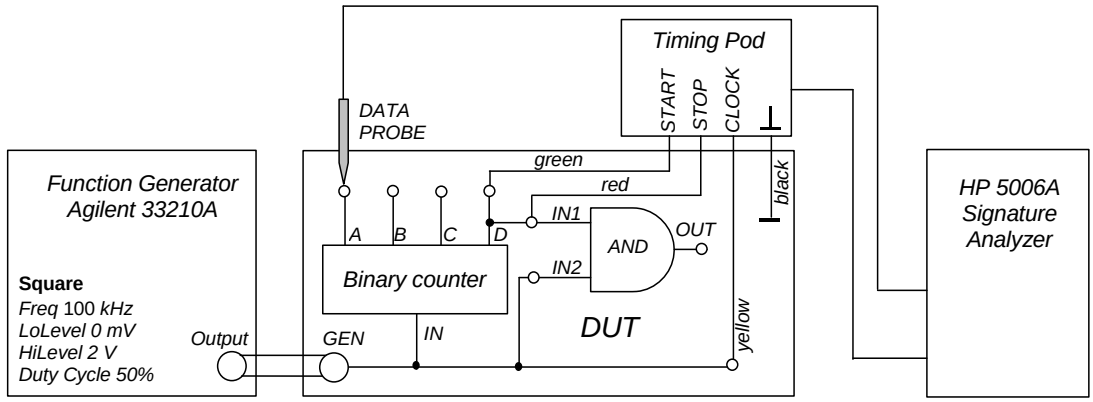


Fig. 13. Signature Analysis measurements with HP 5006A

According to Table 5 set on the 5006A the active edge for CLOCK, START and STOP signals (a lighted LED indicates the rising edge, an unlighted LED indicates the falling edge). Using Data Probe measure signatures on outputs of binary counter and note results in Table 5.

Table 5. Signature analysis measurements with HP 5006A

Edge select			Signatures			
CLOCK	START	STOP	A	B	C	D
⎍	⎍	⎍				

Compare obtained results with HP 5004A measurement in Table 4.

Signature Memory and Composite Signature

Set active edge for CLOCK - ⎍ START - ⎏ and STOP - ⎍ on the 5006A.

1. Select the SIG LATCH function, by pressing the SIG LATCH (key indicator LED above the key should light).
2. Clear Memory by pressing CLEAR key.
3. Connect Data Probe to output A of DUT.
4. Press Probe Switch on Data Probe and in this way write the actual signature to the memory.
5. Repeat the above sequence for output B and C of DUT.
6. Press RECALL key (key indicator LED above the key should light). Write down the obtained Composite Signature (with dots) in Table 6.
7. Pressing Probe Switch on Data Probe read signatures from memory and note in Table 6.

Table 6. Composite Signature measurements with HP 5006A

Output	A	B	C	Composite Signature
Memory location	01	02	03	x.x.x.x.
Signature				

According to Fig. 6 write down binary representation of signatures obtained in Table 6. Calculate the theoretical value of Composite Signature (the binary sum of all the signatures accumulated).

Table 7. Composite Signature measurements with HP 5006A

Output	A	B	C	Composite Signature
Memory location	01	02	03	x.x.x.x.
Binary representation of signature				
Binary representation of theoretical value of Composite Signature				

Compare theoretical value of Composite Signature with obtained from measurements.