# Service Guide

## HP 85644A/85645A Tracking Source


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# The HP 85644A and HP 85645A Tracking Sources

The HP 85644A and HP 85645A tracking sources complement and expand the measurement capability and versatility of your HP spectrum analyzer. They are designed primarily as general purpose accessories for spectrum analyzers (referred to as the host instrument).

**What the HP 85644A and HP 85645A tracking sources offer** A tracking source combined with a host spectrum analyzer allows you to measure the swept amplitude response of a device, such as an amplifier or a filter. These measurements have the advantage of high dynamic range and speed. In addition, since the spectrum analyzer is a tuned receiver, measurements are not affected by spurious signals or harmonics.

## Performance options

The HP 85644A tracking source is ac coupled. The frequency range is from 300 kHz to 6.5 GHz with selectable RF output power.

The HP 85645A tracking source allows you to choose ac or dc coupling. The frequency range is from 300 kHz to 26.5 GHz with selectable RF output power.

## Versatility and compatibility

The tracking sources can easily be configured to track the input frequency of a variety of spectrum analyzers or the output frequency of a microwave sweep oscillator. A configuration menu, accessible at the press of a front-panel key or via HP-IB, allows you to choose from among the following compatible host instruments:

- HP 8560 Series portable spectrum analyzers
- HP 8566A/B spectrum analyzers
- HP 8590 Series portable spectrum analyzers
- HP 8340A/B synthesized sweepers
- HP 8350 Series sweep oscillators

## The HP 85644A and HP 85645A tracking sources extend measurement capability

**Offset tracking**

The tracking sources have offset tracking capability. Offset tracking makes possible the amplitude response measurements of many frequency translation devices (such as mixers), and of systems with delays (such as satellite links). The advantage of the host spectrum analyzer (a tuned receiver) minimizes the effects of other mixing products.

**Swept TOI** With two tracking sources set to appropriate offset frequencies, swept TOI (third-order-intercept) measurements are possible over a continuous range of frequencies. The time required for the swept TOI measurement is minimal

**Power sweep** The tracking source also offers power sweep capability. Power sweep is useful for characterizing saturation effects of devices under test.

**Rugged CW source**

The tracking sources can generate stand-alone, CW signals at fixed, non-synthesized, frequencies of your choosing. No connections to a host instrument are required. The CW signal from the tracking source can be used, along with a host spectrum analyzer, for measuring harmonics generated by a device such as an amplifier.

**EMC measurements**

The tracking source combined with a transducer can make swept measurements of circuit immunity to electromagnetic interference.

## In This Book

This book is your service guide for the HP 85644A and HP 85645A tracking sources.

Chapter 1, "Making Adjustments," provides instructions for adjusting the tracking source.

Chapter 2, "Self-Test Diagnostics," provides information about the self-test diagnostics for the tracking source.

Chapter 3, "General Troubleshooting," provides information for troubleshooting the tracking source.

Chapter 4, "Test Key Menu Functions," provides information about the tracking source test key user menu and service menu functions.

Chapter 5, "Adjust Key Menu Functions," provides information about the tracking source adjust key user menu and service menu functions.

Chapter 6, "If You Have a Problem,' provides information to help you when you have a problem with the tracking source.

Chapter 7, "Assembly Replacement," provides information for identifying, ordering, and replacing assemblies, parts, and accessories for the tracking source.

Chapter 8, "Major Assembly and Cable Locations," illustrates the various assembly and cable locations in the tracking source.

## Warranty

This Hewlett-Packard instrument product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by Hewlett-Packard. Buyer shall prepay shipping charges to Hewlett-Packard and Hewlett-Packard shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to Hewlett-Packard from another country.

Hewlett-Packard warrants that its software and firmware designated by Hewlett-Packard for use with an instrument will execute its programming instructions when properly installed on that instrument. Hewlett-Packard does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error-free.

**LIMITATION OF WARRANTY**

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

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## Assistance

***Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.***

***For any assistance, contact your nearest Hewlett-Packard Sales and Service Office.***

## Safety Symbols

The following safety symbols are used throughout this manual. Familiarize yourself with each of the symbols and its meaning before operating this instrument.

**Caution**

The ***caution*** sign denotes a hazard. It calls attention to a procedure which, if not correctly performed or adhered to, could result in damage to or destruction of the instrument. Do not proceed beyond a ***caution*** sign until the indicated conditions are fully understood and met.

**Warning**

***The warning*** **sign denotes a hazard. It calls attention to a procedure which, if not correctly performed or adhered to, could result in injury or loss of life. Do not proceed beyond a `warning` sign until the indicated conditions are fully understood and met.**

## General Safety Considerations

**Warning**

***Before this instrument is switched on,*** **make sure it has been properly grounded through the protective conductor of the ac power cable to a socket outlet provided with protective earth contact.**

**Any interruption of the protective (grounding) conductor, inside or outside the instrument, or disconnection of the protective earth terminal can result in personal injury.**

**Warning**

**There are many points in the instrument which can, if contacted, cause personal injury. Be extremely careful.**

**Any adjustments or service procedures that require operation of the instrument with protective covers removed should be performed only by trained service personnel.**

**Caution**

***Before this instrument is switched on,*** make sure its primary power circuitry has been adapted to the voltage of the ac power source.

Failure to set the ac power input to the correct voltage could cause damage to the instrument when the ac power cable is plugged in.

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# Making Adjustments

The procedures in this chapter adjust the tracking source to the specifications listed in the HP *85644A/85645A Trucking Source User's Guide.*

If one or more tracking source assemblies has been replaced or repaired, adjustment procedures should be done before verifying operation. Refer to Table l-l to determine which adjustment to perform after repairing or replacing an assembly. Find the assembly that has been repaired or replaced in the left-hand column. Then perform the adjustments marked across the adjustment columns for that assembly.

This chapter contains the following adjustments:

**Adjusting the Leveling Amplifier.**
This procedure adjusts the output levels of the first and second leveling amplifiers.

**Adjusting the Switched YIG-Tuned Multiplier (HP 85645A only).**
This procedure adjusts the YTM Filter for bands 1 through 4, and the SRD Bias for bands 2 through 4. This procedure applies only to the HP 85645A tracking source.

**Adjusting the Low-Band Slope and ALC.**
This procedure adjusts and checks the low-band slope and adjusts the ALC low-band circuitry.

**Adjusting the High-Band Slope and ALC.**
This procedure adjusts and checks the high-band slope and adjusts the ALC high-band circuitry.

**Adjusting the Frequency Accuracy.**
This procedure adjusts the frequency accuracy of the tracking source.

**Adjusting the Internal 10 MHz Reference.**
This procedure adjusts the internal 10 MHz reference of the tracking source.

The tracking source must be turned on and allowed to warm up for at least 1/2 hour before making any adjustments. It is acceptable to turn the power off briefly while making connections.

**Table 1-1. Adjustments Performed After Assembly Repair or Replacement**

| Assembly Repaired or Replaced | Adjustment | | | | | |
|---|---|---|---|---|---|---|
| | Leveling Amplifier | SYTM *(HP 85645A only)* | Low-Band Slope and ALC | High-Band Slope and ALC | Frequency Accuracy | Internal 10 MHz Reference |
| A2 Controller Board | • | • | • | • | • | • |
| A3 RF Board | | • | • | • | • | • |
| A4 YTO | | | | | • | • |
| A5 Attenuator | | | • | • | | |
| A6 SYTM *(HP 85645A only)* | | • | • | • | | |
| A7 Coupler *(HP 85645A only)* | | • | • | • | | |
| A8 Detector *(HP 85645A only)* | | • | | • | | |
| A9 Modulator Switch *(HP 85644A only)* | | | • | • | | |
| A9 Modulator/Amplifier *(HP 85645A only)* | | • | | • | | |
| A10 Isolator *(HP 85645A only)* | | • | | • | | |
| A11 Detector | • | | | | | |
| A12 Amplifier | • | | | | | |
| A13 Amplifier | • | | | | | |
| A15 Low Band | | | • | | | |
| A18 5 GHz Low Pass Filter | • | | | | | |
| AT1 6 dB Attenuator | • | | | | | |
| AT2 6 dB Attenuator | • | | | | | |

## Adjusting the Leveling Amplifier

The spectrum analyzer LO input signal goes through two leveling amplifiers before entering the band discriminator and offset mixer. The leveling amplifiers compensate for the LO input signal power variation and for the gain versus temperature and frequency errors of the leveling amplifiers. The leveling amplifiers also provide the required reverse isolation to the LO host.

The output levels of the leveling amplifiers are adjusted by two digital to analog converters (DACs) on the controller board. These DACs provide reference voltages that the leveling detector voltages are compared to in the two leveling loops.

This adjustment procedure adjusts both the first and second leveling amplifiers. The band discriminator adjustment, which is part of the second amplifier adjustment, is the most critical.

The following equipment is required for the leveling amplifier adjustment:

Spectrum analyzer ..... HP 8562A
Synthesized sweeper ..... HP 8340B
Powermeter ..... HP 436A
Power sensor ..... HP 8485A
Cable, BNC, 1.22 m (three ***required)*** . . . . HP part number 81205529
Cable, SMA, 1 m ***(two required)*** . . . . . HP part number 5061-5458

The tracking source must be turned on and allowed to warm up for at least 1/2 hour before making any adjustments. It is acceptable to turn the power off briefly while making the following connections.

1. Connect the tracking source to a spectrum analyzer host.

   - Connect the BNC cables between the HP 85644A/85645A tracking source and the HP 8562A spectrum analyzer as described in the table below.

| From Tracking Source Connector | To HP 8562A Connector |
|---|---|
| 10 MHz IN | 10 MHz REF IN/OUT |
| SWP + TUNE IN | 0.5V/GHz OUTPUT |
| BLANK IN | BLANKING OUTPUT |

- Connect the SMA cables between the HP 85644A/85645A tracking source and the HP 8562A spectrum analyzer as described in the table below.

| From Tracking Source Connector | To HP 8562A Connector |
|---|---|
| RF OUT | RF INPUT |
| LO INPUT | LO OUTPUT |

2. Configure the tracking source and HP 8562A spectrum analyzer by pressing the following tracking source keys:
   - Press (PRESET).
   - Press (CONFIG).
   - Press (MENU DOWN) until CNFG #1 HOST SELECT is displayed.
   - Press (ENTER) to select the host instrument.
   - Press (↑) or (↓) until CNFG #1 HP 8562 is displayed.
   - Press (ENTER); CNFG #1 HP 8562 ← is displayed.

   The HP 8562A spectrum analyzer is now selected as host instrument to the tracking source.
3. Set up the equipment by using the following steps:
   - Set the HP 8562A spectrum analyzer to the following:

     Frequency span ..... 0 Hz
     Center frequency ..... 3.5 GHz
   - Connect the HP 8485A power sensor to the HP 436A power meter.
   - Zero and calibrate the power meter and power sensor, as described in the power meter operation manual.
   - Connect the power meter to the tracking source LO OUTPUT connector.
4. Select the first leveling amplifier adjustment from the extended adjust menu of the tracking source. Select the adjustment by pressing the following tracking source keys:
   - Press (ADJUST).
   - Press the (7) and (GHz) keys at the same time until EXTENDED MENU is momentarily displayed.
   - Press (MENU UP) or (MENU DOWN) until #5 LEVEL AMP 1 is displayed.
   - Press (ENTER).

   The first leveling amplifier adjustment is now selected.

5. Adjust the first leveling amplifier.

   Press the ⇧ or ⇩ keys on the tracking source to adjust the first leveling amplifier until the LO OUTPUT power level of the tracking source displayed on the power meter is **+7.5 dBm ±0.5 dBm.**

6. Adjust the second leveling amplifier by using the following steps:

   - **Press** (MENU UP) or (MENU DOWN) until **#6** LEVEL AMP 2 is displayed.
   - Press (ENTER) The tracking source displays the following messages:

     SET SA TO 0 SPAN (displayed for 2 seconds)
     PRESSENTER
   - Set the HP **8562A** spectrum analyzer frequency span to 0.
   - **Press** (ENTER) on the tracking source. The tracking source displays the following messages:

     SET SA TO 3.5 **GHz** (displayed for 2 seconds)
     PRESS ENTER
   - Set the HP 85628 spectrum analyzer center frequency to 3.5 **GHz.**
   - Press (ENTER) on the tracking source. The tracking source displays the following messages:

     SET SA TO 4.896 **GHz** (displayed for 3 seconds)
     PRESS ENTER
   - Set the HP 85628 spectrum analyzer center frequency to 4.896 **GHz.**
   - Press (ENTER) on the tracking source. The tracking source displays the following messages:

     SET SA TO 5.155 **GHz** (displayed for 3 seconds)
     PRESSENTER
   - Set the HP **8562A** spectrum analyzer center frequency to 5.155 **GHz.**
   - Press (ENTER) on the tracking source. This starts the routine that sets the operating point of the second leveling amplifier.
   - Press (ENTER) after ENTER TO STORE is displayed on the tracking source. This stores the values into EEPROM.

## Adjusting the Switched YIG-Tuned Multiplier (HP 85645A only)

This adjustment applies only to the HP 85645A tracking source. Figure l-l illustrates how you determine which procedures to perform.

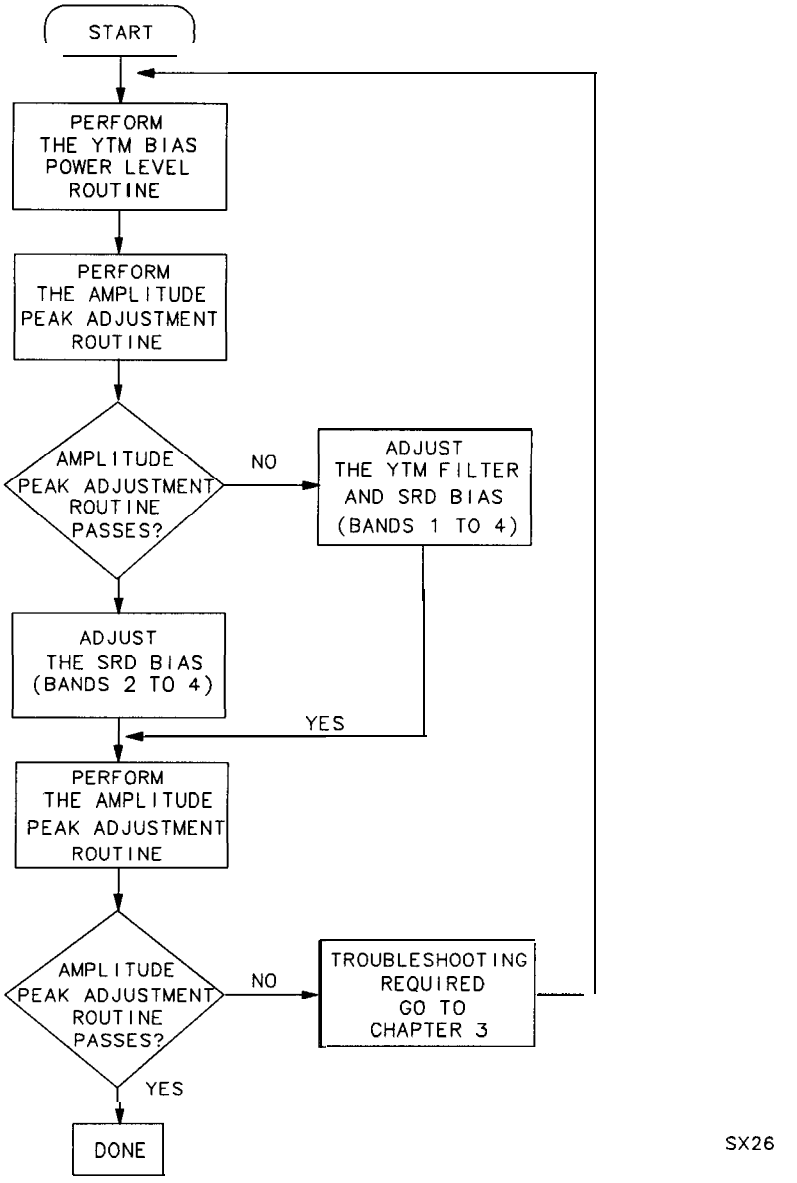



**Figure l-l. SYTM Adjustment Procedure at a Glance**

The Switched YIG-Tuned Multiplier (SYTM) adjustment procedure is divided into the following:

- Perform the YTM Bias Power Level Routine
- Perform the Amplitude Peak Adjustment Routine
- Adjust the SRD Bias (performed if the amplitude peak adjustment routine passes.)
- Adjust the YTM Filter and SRD Bias (performed only if the amplitude peak adjustment routine fails.)

Both the YTM (YIG-tuned multiplier) Bias Power Level and the Amplitude Peak Adjustment routines must be performed before any SRD (step recovery diode) or YTM filter adjustments are performed. The results of the Amplitude Peak Adjustment routine determine which procedure, "Adjust the SRD Bias" or "Adjust the YTM Filter and SRD Bias", completes the adjustment. Figure l-l illustrates the procedure process flow.

The routines and adjustments included in the SYTM adjustment procedure are described below.

**YTM Bias Power Level Routine.** An internal adjustment routine that will set up default conditions within the tracking source and internally adjust some of the bias parameters. Perform this routine before performing the Amplitude Peak Adjustment routine and before performing any YTM adjustments.

**Amplitude Peak Adjustment Routine.** An internal YTM amplitude peaking routine that will perform all of the adjustments, except the SRD bias adjustments. Perform this routine after performing the YTM Bias Power Level routine and before performing any YTM adjustments.

**SRD Bias Adjustment Procedure.** This adjustment procedure is performed only if the Amplitude Peak Adjustment routine has passed. This procedure adjusts the SRD bias for bands 2 through 4. Each band adjustment consists of the following:

YTM bias offset
YTM bias gain

**YTM Filter and SRD Bias Adjustment Procedure.** This adjustment procedure is performed *only* if the Amplitude Peak Adjustment routine has failed. This procedure adjusts the YTM filter for bands 1 through 4 and the SRD bias for bands 2 through 4. Each band adjustment consists of the following:

YTM offset
YTM gain
YTM breakpoints
YTM bias offset (bands 2 through 4 only)
YTM bias gain (bands 2 through 4 only)

## Perform the YTM Bias Power Level Routine

The YTM Bias Power Level routine installs default values for the SRD bias and internally adjusts some of the bias parameters. Perform this routine before performing the Amplitude Peak Adjustment routine and the YTM filter or SRD bias adjustments.

Select the YTM bias power level adjustment from the extended adjust menu of the tracking source. Select the adjustment and set the YTM bias power level by pressing the following tracking source keys:

1. Press (ADJUST).
2. Press the (7) and (GHz) keys at the same time until EXTENDED MENU is momentarily displayed.
3. Press [MENU DOWN) until #21 YTM BIAS PWR LVL is displayed.
4. Press (ENTER). The YTM bias power level adjustment is now selected and will be performed.
5. Press (ENTER) after ENTER TO STORE is displayed on the tracking source to install default values into EEPROM.

The YTM Bias Power Level routine is finished, now continue with the Amplitude Peak Adjustment routine.

## Perform the Amplitude Peak Adjustment Routine

Perform the Amplitude Peak Adjustment routine after executing the YTM Bias Power Level routine and before performing the YTM filter or SRD bias adjustments. This routine ensures maximum power at various operating temperatures and reduces the problems associated with the drift and temperature variation of the YTM filter.

If the Amplitude Peak Adjustment routine performs successfully, the YTM filter has been properly adjusted and only the "Adjust the SRD Bias" procedure must be performed.

Use the following to select the amplitude peak routine from the adjust menu of the tracking source. Select the adjustment by pressing the following tracking source keys:

1. Press (ADJUST).
2. Press (MENU DOWN] until #1 AMPLITUDE PEAK is displayed.
3. Press (ENTER). The amplitude peak routine is now selected; the tracking source will now perform the routine.
   - If the routine passes, YTM PEAK DONE is displayed on the tracking source. The Amplitude Peak Adjustment routine is finished, now continue with "Adjust the SRD Bias" in the following pages.
   - If the routine fails, YTM PEAK FAIL is displayed on the tracking source. The Amplitude Peak Adjustment routine is finished, now continue with "Adjust the YTM filter and SRD Bias" in the following pages.

## Adjust the SRD Bias

The Amplitude Peak Adjustment routine must pass before this SRD bias adjustment is performed (See Figure l-l). This procedure allows you to perform the SRD bias adjustments needed for bands 2 through 4. (Band 1 is not adjusted.)

### Set up the equipment

The following equipment is required for the SRD bias adjustment:

Spectrum analyzer . . . . . HP 8562A
Cable, BNC, 1.22 m ***(three required)*** . . . . HP part number 8120-5529
Cable, SMA, 1 m ***(two required)*** . . . . . HP part number 5061-5458

The tracking source must be turned on and allowed to warm up for at least 1/2 hour before making any adjustments. It is acceptable to turn the power off briefly while making the following connections.

1. Connect the tracking source to a spectrum analyzer host.
   - Connect the BNC cables between the HP 84645A tracking source and the HP 8562A spectrum analyzer as described in the table below.

| From HP 85645A Connector | To HP 8562A Connector |
|---|---|
| 10 MHz IN | 10 MHz REF IN/OUT |
| SWP+TUNE IN | 0.5V/GHz OUTPUT |
| BLANK IN | BLANKING OUTPUT |

   - Connect the SMA cables between the HP 85645A tracking source and the HP 8562A spectrum analyzer as described in the table below.

| From HP 85645A Connector | To HP 8562A Connector |
|---|---|
| RF OUT | RF INPUT |
| LO INPUT | LO OUTPUT |

2. Configure the tracking source and HP 8562A spectrum analyzer by pressing the following tracking source keys:
   - Press (PRESET).
   - Press (CONFIG).
   - Press [MENU DOWN] until CNFG Xl HOST SELECT is displayed.
   - Press (ENTER) to select the host instrument.
   - Press (↑) or (↓) until CNFG #1 HP 8562 is displayed.
   - Press (ENTER); CNFG #1 HP 8562 ← is displayed.

   The HP 8562A spectrum analyzer is now selected as host instrument to the tracking source.

3. Set the HP 8562A spectrum analyzer to the following:

| | |
|---|---|
| Reference level | +25 dBm |
| Frequency start | 5.7 GHz |
| Frequency stop | 13.0 GHz |
| Scale | 5 dB/div |

4. Set the tracking source power level by pressing (POWER LEVEL), then 30 (dBm).

### Adjust the SBD bias for band 2

Steps 5 through 12 allow you to perform the SRD bias adjustments for band 2. You must constantly monitor the entire band displayed on the spectrum analyzer while you are performing these steps. Be sure the SRD is not being overdriven, watch for the signal dropping out or showing unstable responses

5. Select the band lock mode from the extended adjust menu of the tracking source and lock it to band 2 by pressing the following tracking source keys:
   - Press (ADJUST).
   - Press [MENU DOWN) until #4 BAND LOCK is displayed.
   - Press (ENTER).
   - Press 2, then (ENTER). The tracking source is now locked to band 2.
6. Select the YTM bias offset adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
   - Press [MENU DOWN) until #22 YTM BIAS OFS is displayed.
   - Press (ENTER). The YTM bias offset adjustment is now selected.
7. Adjust the YTM bias offset by using the following steps:
   - Set the marker of the spectrum analyzer to 5.7 GHz.
   - Press the (↑) or (↓) keys to change the YTM bias offset value until the signal on the spectrum analyzer is peaked at 5.7 GHz. Be sure the SRD is not being overdriven.
8. Select the YTM bias gain adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
   - Press [MENU DOWN) until #23 YTM BIAS GN is displayed.
   - Press (ENTER). The YTM bias gain adjustment is now selected.

9. **Adjust** the YTM bias gain by using the following steps:
   - Set the marker of the spectrum analyzer to 13.0 **GHz.**
   - Press the ↑ or ↓ keys to change the YTM bias gain value until the signal on the spectrum analyzer is peaked at 13.0 **GHz.**
10. Select the YTM bias offset adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (MENU UP) until **#22** YTM BIAS OFS is displayed.
    - Press (ENTER). The YTM bias offset adjustment is now selected.
11. Adjust the final YTM bias offset by pressing the ↓ key 15 times. This is to ensure that the SRD is not being overdriven. The final YTM bias offset is now set for band 2.

**Caution**

Do not use the UNDO option when performing the next step. Using the UNDO option will store invalid data that will be loaded the next time the instrument is powered on.

12. Select the store cal data test routine from the extended test menu of the tracking source by pressing the following tracking source keys:
    - Press (TEST).
    - Press the (4) and (GHz) keys at the same time until EXTENDED MENU is momentarily displayed.
    - Press (MENU DOWN) until **#28** STORE CAL DATA is displayed.
    - Press (ENTER). All values for band 2 are now stored into EEPROM.

    The SRD bias adjustment for band 2 is finished, now continue with the SRD bias adjustment for band 3.

### Adjust the SRD bias for band 3

Steps 13 through 21 allow you to perform the SRD bias adjustments for band 3. You must constantly monitor the entire band displayed on the spectrum analyzer while you are performing these steps. Be sure the SRD is not being overdriven, watch for the signal dropping out or showing unstable responses.

13. Set the HP **8562A** spectrum analyzer to the following:

| | |
|---|---|
| Frequency start ..... | 12.36 **GHz** |
| Frequency stop ..... | 19.7 **GHz** |

14. Select the band lock mode from the extended adjust menu of the tracking source and lock it to band 3 by pressing the following tracking source keys:
    - Press (ADJUST).
    - Press (MENU DOWN) until #4 BAND LOCK is displayed.
    - Press (ENTER).
    - Press 3, then (ENTER). The tracking source is now locked to band 3.
15. Select the YTM bias offset adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (ADJUST)
    - Press (MENU DOWN) until #22 YTM BIAS OFS is displayed.
    - Press (ENTER). The YTM bias offset adjustment is now selected.
16. Adjust the YTM bias offset by using the following steps:
    - Set the marker of the spectrum analyzer to 12.4 GHz.
    - Press the ↑ or ↓ keys to change the YTM bias offset value until the signal on the spectrum analyzer is peaked at 12.4 GHz. Be sure the SRD is not being overdriven.
17. Select the YTM bias gain adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (MENU DOWN) until #23 YTM BIAS GN is displayed.
    - Press (ENTER). The YTM bias gain adjustment is now selected.
18. Adjust the YTM bias gain by using the following steps:
    - Set the marker of the spectrum analyzer to 19.7 GHz.
    - Press the ↑ or ↓ keys to change the YTM bias gain value until the signal on the spectrum analyzer is peaked at 19.7 GHz.
19. Select the YTM bias offset adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (MENU UP) until #22 YTM BIAS OFS is displayed.
    - Press (ENTER). The YTM bias offset adjustment is now selected.
20. Adjust the final YTM bias offset by pressing the ↓ key 15 times. This is to ensure that the SRD is not being overdriven. The final YTM bias offset is now set for band 3.

**Caution** Do not use the UNDO option when performing the next step. Using the UNDO option will store invalid data that will be loaded the next time the instrument is powered on.

21. Select the store cal data test routine from the extended test menu of the tracking source by pressing the following tracking source keys:
    - Press (TEST).
    - Press (MENU DOWN) until #28 STORE CAL DATA is displayed.
    - Press (ENTER). All values for band 3 are now stored into EEPROM.

    The SRD bias adjustment for band 3 is finished, now continue with the SRD bias adjustment for band 4.

### Adjust the SRD bias for band 4

Steps 22 through 30 allow you to perform the SRD bias adjustments for band 4. You must constantly monitor the entire band displayed on the spectrum analyzer while you are performing these steps Be sure the SRD is not being overdriven, watch for the signal dropping out or showing unstable responses.

22. Set the HP 8562A spectrum analyzer to the following:

    Frequency start .....*... 19.031 GHz
    Frequency stop ..... 26.5 GHz

23. Select the band lock mode from the extended adjust menu of the tracking source and lock it to band 4 by pressing the following tracking source keys:
    - Press (ADJUST).
    - Press (MENU DOWN) until #4 BAND LOCK is displayed.
    - Press (ENTER)
    - Press 4, then (ENTER). The tracking source is now locked to band 4.

24. Select the YTM bias offset adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (ADJUST)
    - Press (MENU DOWN) until #22 YTM BIAS OFS is displayed.
    - Press (ENTER). The YTM bias offset adjustment is now selected.

25. Adjust the **YTM** bias offset by using the following steps:
    - Set the marker of the spectrum analyzer to 20.0 **GHz.**
    - Press the ↑ or ↓ keys to change the **YTM** bias offset value until the signal on the spectrum analyzer is peaked at 20.0 **GHz.** Be sure the SRD is not being overdriven.
26. Select the **YTM** bias gain adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press [MENU DOWN] until **#23** YTM BIAS GN is displayed.
    - Press [ENTER]. The **YTM** bias gain adjustment is now selected.
27. Adjust the **YTM** bias gain by using the following steps:
    - Set the marker of the spectrum analyzer to 26.5 **GHz.**
    - Press the ↑ or ↓ keys to change the **YTM** bias gain value until the signal on the spectrum analyzer is peaked at 26.5 **GHz.**
28. Select the **YTM** bias offset adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press [MENU UP] until **#22** YTM BIAS OFS is displayed.
    - Press (ENTER). The **YTM** bias offset adjustment is now selected.
29. Adjust the final **YTM** bias offset by pressing the ↓ key 15 times. This is to ensure that the SRD is not being overdriven. The final **YTM** bias offset is now set for band 4.

**Caution**

Do not use the UNDO option when performing the next step. Using the UNDO option will store invalid data that will be loaded the next time the instrument is powered on.

30. Select the store cal data test routine from the extended test menu of the tracking source by pressing the following tracking source keys:
    - Press [TEST].
    - Press [MENU DOWN] until **#28** STORE CAL DATA is displayed.
    - Press [ENTER]. All values for band 4 are now stored into EEPROM.

### Store the values into EEPROM

Steps 31 and 32 allow you to perform the Amplitude Peak Adjustment routine, then store the values into EEPROM.

31. Select the Amplitude Peak Adjustment routine from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (ADJUST).
    - Press (MENU DOWN) or (MENU UP) until #1 AMPLITUDE PEAK is displayed.
    - Press (ENTER). The amplitude peak routine is now selected; the tracking source will now perform the routine.

      If the routine passes, YTM PEAK DONE is displayed on the tracking source. Continue with step 32.

      If the routine fails, YTM PEAK FAIL is displayed on the tracking source. There is probably a hardware problem, refer to Chapter 3 for further troubleshooting. After repairing the instrument, repeat the entire SYTM adjustment procedure beginning with YTM Bias Power Level routine.

**Caution**

Do not use the UNDO option when performing the next step. Using the UNDO option will store invalid data that will be loaded the next time the instrument is powered on.

32. Select the store cal data test routine from the extended test menu of the tracking source by pressing the following tracking source keys:
    - Press (TEST).
    - Press (MENU DOWN) until #28 STORE CAL DATA is displayed.
    - Press (ENTER). All values for the Amplitude Peak Adjustment routine are now stored into EEPROM.

    The SRD Bias adjustment is finished. This step completes the SYTM adjustments for the HP 85645A tracking source.

## Adjust the YTM Filter and SRD Bias

This procedure is to be performed only if the Amplitude Peak Adjustment routine failed (See Figure 1-1). This procedure allows you to perform the YTM filter adjustments for each band (1 through 4). The SRD bias adjustment follows each STYM filter adjustment. (Band 1 does not have an SRD bias adjustment.)

### Set up the equipment

The following equipment is required for the YTM filter and SRD bias adjustments:

Spectrum analyzer ..... HP 8562A
Cable, BNC, 1.22 m ***(three required)*** . . . . HP part number 8120-5529
Cable, SMA, 1 m ***(two required)*** . . . . . HP part number 5061-5458

The tracking source must be turned on and allowed to warm up for at least 1/2 hour before making any adjustments. It is acceptable to turn the power off briefly while making the following connections.

1. Connect the tracking source to a spectrum analyzer host.
   - Connect the BNC cables between the HP 85645A tracking source and the HP 8562A spectrum analyzer as described in the table below.

| From HP 85645A Connector | To HP 8562A Connector |
|---|---|
| 10 MHz IN | 10 MHz REF IN/OUT |
| SWP+ TUNE IN | 0.5V/GHz OUTPUT |
| BLANK IN | BLANKING OUTPUT |

   - Connect the SMA cables between the HP 85645A tracking source and the HP 8562A spectrum analyzer as described in the table below.

| From HP 85645A Connector | To HP 8562A Connector |
|---|---|
| RF OUT | RF INPUT |
| LO INPUT | LO OUTPUT |

2. Configure the tracking source and HP **8562A** spectrum analyzer by pressing the following tracking source keys:
   - Press (PRESET).
   - ⊳□ℳ•• (CONFIG).
   - Press (MENU DOWN) until `CNFG #1 HOST SELECT` is displayed.
   - Press (ENTER) to select the host instrument.
   - Press (⇧) or (⇩) until CNFG **#1** HP 8562 is displayed.
   - Press (ENTER); CNFG **#1** `HP 8562` ← is displayed.

   The HP **8562A** spectrum analyzer is now selected as host instrument to the tracking source.

### Adjust the YTM filter for band 1

Steps 3 through 12 allow you to perform the **YTM** filter adjustments for band 1.

3. Set the HP **8562A** spectrum analyzer to the following:

| | |
|---|---|
| Reference level | **+25 dBm** |
| Frequency start | 2.75 **GHz** |
| **Frequency** stop | 6.46 **GHz** |
| Marker | 3 **GHz** |
| Scale | 5 **dB/div** |

4. Set the tracking source power level by pressing (POWER LEVEL), then 30 (dBm).
5. Select the band lock mode from the extended adjust menu of the tracking source. Lock the tracking source to band 1 by pressing the following tracking source keys:
   - Press (MENU DOWN) until **#4** `BAND LOCK` is displayed.
   - Press (ENTER).
   - Press 1, then (ENTER). The tracking source is now locked to band 1.
6. Select the **YTM** offset DAC from the extended adjust menu of the tracking source and set the **YTM** offset DAC by pressing the following tracking source keys:
   - Press (MENU DOWN) until **#14** `YTM OFFSET` is displayed.
   - Press (ENTER) to select.
   - Press 255, then (ENTER) on the tracking source to set the **YTM** offset DAC to its maximum value.
7. Select the **YTM** gain adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
   - Press (MENU UP) until **#13** YTM `GAIN` is displayed.
   - Press (ENTER). The **YTM** gain adjustment is now selected.

8. Calculate and adjust the YTM gain DAC value at 3 GHz by using the following steps:

   - While viewing the spectrum analyzer display (marker level), peak the signal at 3 GHz by pressing the ⇧ key on the tracking source. Pressing the ⇧ key increases the YTM gain DAC value.

     The first peak may not always be the correct peak. Occasionally, traveling modes in the YTF' will appear as a narrow peak. Keep tuning until the main filter peak (wider than a traveling mode) is identified.

   - After the signal is peaked, press [MARKER DELTA] on the spectrum analyzer. The marker delta should read 0 dB.

   - Press the ⇧ key on the tracking source to increase the YTM gain DAC value until the marker delta reads -1 dB.

     Record this DAC value below.

     UPPER VAL = _____

   - Press the ⇩ key on the tracking source to decrease the YTM gain DAC value until the marker delta goes back through 0 dB, then again reads -1 dB.

     Record this DAC value below.

     LOWER VAL = _____

   - Calculate the average DAC (DAC LOW) value using the following equation:

     DAC LOW = (UPPER VAL + LOWER VAL)/ 2

     DAC LOW = _____

9. Calculate and adjust the YTM gain DAC value at 6 GHz using the following steps:

   - Set the marker to NORMAL at 6 GHz on the spectrum analyzer.

   - While viewing the spectrum analyzer display (marker level), peak the signal at 6 GHz by pressing the ⇧ key on the tracking source. Pressing the ⇧ key increases the YTM gain DAC value.

     The first peak may not always be the correct peak. Occasionally, traveling modes in the YTF' will appear as a narrow peak, keep tuning until the main filter peak (wider than a traveling mode) is identified.

   - After the signal is peaked, press [MARKER DELTA] on the spectrum analyzer. The marker delta should read 0 dB.

   - Press the ⇧ key on the tracking source to increase the YTM gain DAC value until the marker delta reads -1 dB.

     Record this DAC value below.

     UPPER VAL = _____

- Press the ⇩ key on the tracking source to decrease the YTM gain DAC value until the marker delta goes back through 0 dB, then again reads -1 dB.

  Record this DAC value below.

  LOWER VAL = _____

- Calculate the average DAC (DAC HIGH) value using the following equation:

  DAC HIGH = (UPPER VAL + LOWER VAL)/ 2

  DAC HIGH = _____

10. Calculate and set the YTM gain value using the following steps:
    - Calculate the YTM gain value using the following equation:

      YTM GAIN = [(DAC HIGH x 6) – (DAC LOW x 3)]/3

    - Enter the YTM GAIN value into the tracking source and record it below. (This value will be used for the YTM gain for all of the bands.)

      YTM GAIN = _____

    - Press (ENTER) on the tracking source to install this value.
11. Select the YTM offset adjustment from the extended adjust menu of the tracking source and set the YTM offset DAC by pressing the following tracking source keys:
    - Press (MENU DOWN) until #14 YTM OFFSET is displayed.
    - Press (ENTER) to select.
    - Press ⇧ or ⇩ to peak the spectrum analyzer trace for the greatest power level across the entire band of the spectrum analyzer.

**Caution**

Do not use the UNDO option when performing the next step. Using the UNDO option will store invalid data that will be loaded the next time the instrument is powered on.

12. Select the store cal data routine from the extended test menu of the tracking source by pressing the following tracking source keys:
    - Press (TEST).
    - Press the (4) and (GHz) keys at the same time until EXTENDED MENU is momentarily displayed.
    - Press (MENU DOWN) until #28 STORE CAL DATA is displayed.
    - Press (ENTER). All values are now stored into EEPROM.

    The YTM filter adjustment for band 1 is finished, now continue with the YTM filter adjustment for band 2.

### Adjust the YTM filter for band 2

The YTM filter adjustment for band 1 must be done before band 2 can be adjusted. Steps 13 through 19 allow you to perform the YTM filter adjustments for band 2.

13. Set the HP 85628 spectrum analyzer to the following:

    Frequency start ..... 5.7 GHz
    Frequency stop ..... 13.0 GHz

14. Select the band lock mode from the extended adjust menu of the tracking source and lock it to band 2 by pressing the following tracking source keys:
    - Press (ADJUST).
    - Press (MENU DOWN) until #4 BAND LOCK is displayed.
    - Press (ENTER).
    - Press 2, then (ENTER). The tracking source is now locked to band 2.

15. Select the YTM gain adjustment from the extended adjust menu of the tracking source and enter the YTM gain value by pressing the following tracking source keys:
    - Press (MENU DOWN) until #13 YTM GAIN is displayed.
    - Press (ENTER).
    - Enter the YTM GAIN value, calculated and recorded in step 10, into the tracking source.
    - Press (ENTER) to install this value. The YTM gain is now set for band 2.

16. Select the YTM offset adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (MENU DOWN) until #14 YTM OFFSET is displayed.
    - Press (ENTER). The YTM offset adjustment is now selected.

17. Adjust the YTM offset using the following steps:
    - Set the marker of the spectrum analyzer to 5.7 GHz.
    - Press the (↑) or (↓) keys to change the YTM offset value until the signal on the spectrum analyzer is peaked at 5.7 GHz.
    - Press (ENTER) on the tracking source to store the YTM offset value into EEPROM.

18. Select the YTM breakpoint 1 adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (MENU DOWN) until #15 YTM BP1 is displayed.
    - Press (ENTER). The YTM breakpoint number 1 adjustment is now selected.

19. Adjust the YTM breakpoint number 1 using the following steps:
    - Set the marker of the spectrum analyzer to 13.0 GHz.
    - Press the ↑ or ↓ keys to change the YTM breakpoint number 1 value until the signal on the spectrum analyzer is peaked at 13.0 GHz.
    - Record the YTM breakpoint number 1 value. (This value will be used for the first breakpoint in all of the bands.)

      YTM BP1 = _____

    The YTM Alter adjustment for band 2 is finished, now continue with the SRD bias adjustment for band 2.

### Adjust the SRD bias for band 2

The YTM filter adjustment for band 2 must be done before the SRD bias for band 2 can be adjusted. Steps 20 through 26 allow you to perform the SRD bias adjustments for band 2. You must constantly monitor the entire band displayed on the spectrum analyzer while you are performing these steps. Be sure the SRD is not being overdriven, watch for the signal dropping out or showing unstable responses.

20. Select the YTM bias offset adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (MENU DOWN) until #22 YTM BIAS OFS is displayed.
    - Press (ENTER). The YTM bias offset adjustment is now selected.
21. Adjust the YTM bias offset by using the following steps:
    - Set the marker of the spectrum analyzer to 13.0 GHz.
    - Press the ↑ or ↓ keys to change the YTM bias offset value until the signal on the spectrum analyzer is peaked at 13.0 GHz. Be sure the SRD is not being overdriven.
22. Select the YTM bias gain adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (MENU DOWN) until #23 YTM BIAS GN is displayed.
    - Press (ENTER). The YTM bias gain adjustment is now selected.
23. Adjust the YTM bias gain by using the following steps:
    - Set the marker of the spectrum analyzer to 13.0 GHz.
    - Press the ↑ or ↓ keys to change the YTM bias gain value until the signal on the spectrum analyzer is peaked at 13.0 GHz.

24. Select the YTM bias offset adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (MENU UP) until #22 YTM BIAS OFS is displayed.
    - Press (ENTER). The YTM bias offset adjustment is now selected.
25. Adjust the final YTM bias offset by pressing the (⇩) key 15 times. This is to ensure that the SRD is not being overdriven. The final YTM bias offset is now set for band 2.

**Caution**

Do not use the UNDO option when performing the next step. Using the UNDO option will store invalid data that will be loaded the next time the instrument is powered on.

26. Select the store cal data test routine from the extended test menu of the tracking source by pressing the following tracking source keys:
    - Press (TEST).
    - Press the (4) and (GHz) keys at the same time until EXTENDED MENU is momentarily displayed.
    - Press (MENU DOWN) until #28 STORE CAL DATA is displayed.
    - Press (ENTER). All values for band 2 are now stored into EEPROM.

    The SRD bias adjustment for band 2 is finished, now continue with the YTM filter adjustment for band 3.

### Adjust the YTM filter for band 3

The YTM filter and SRD bias adjustments for band 2 must be done before the YTM filter for band 3 can be adjusted. Steps 27 through 34 allow you to perform the YTM filter adjustments for band 3.

27. Set the HP 8562A spectrum analyzer to the following:

    Frequency start ..... 12.36 GHz
    Frequency stop . . . . . ..*.....*..... 19.7 GHz

28. Select the band lock mode from the extended adjust menu of the tracking source and lock it to band 3 by pressing the following tracking source keys:
    - Press (ADJUST).
    - Press (MENU DOWN) until #4 BAND LOCK is displayed.
    - Press (ENTER).
    - Press 3, then (ENTER). The tracking source is now locked to band 3.

29. Select the YTM gain adjustment from the extended adjust menu of the tracking source and enter the YTM gain value by pressing the following tracking source keys:
    - Press (MENU DOWN) until #13 YTM GAIN is displayed.
    - ▷□ℳ•• (ENTER).
    - Enter the YTM GAIN value, calculated in step 10, into the tracking source.
    - Press (ENTER) to install this value. The YTM gain is now set for band 3.
30. Select the YTM breakpoint number 1 adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (MENU DOWN) until #15 YTM BP1 is displayed.
    - Press (ENTER).
    - Enter the YTM BP1 value, recorded in step 19, into the tracking source.
    - Press (ENTER) to install this value. The YTM breakpoint number 1 is now set for band 3.
31. Select the YTM offset adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (MENU UP) until #14 YTM OFFSET is displayed.
    - Press (ENTER). The YTM offset adjustment is now selected.
32. Adjust the YTM offset using the following steps:
    - Set the marker of the spectrum analyzer to 12.4 GHz.
    - Press the (⇧) or (⇩) keys to change the YTM offset value until the signal on the spectrum analyzer is peaked at 12.4 GHz.
33. Select the YTM breakpoint 2 adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (MENU DOWN) until #16 YTM BP2 is displayed.
    - Press (ENTER]. The YTM breakpoint number 2 adjustment is now selected.

34. Adjust the YTM breakpoint number 2 using the following steps:
    - Set the marker of the spectrum analyzer to 19.7 GHz.
    - Press the ↑ or ↓ keys to change the YTM breakpoint number 2 value until the signal on the spectrum analyzer is peaked at 19.7 GHz.
    - Record the YTM breakpoint number 2 value. (This value will be used for the YTM BP2 value for band 4.)

      YTM BP2 = _____

    The YTM filter adjustment for band 3 is finished, now continue with the SRD bias adjustment for band 3.

### Adjust the SRD bias for band 3

The YTM filter adjustment for band 3 must be done before the SRD bias for band 3 can be adjusted. Steps 35 through 41 allow you to perform the SRD bias adjustments for band 3. You must constantly monitor the entire band displayed on the spectrum analyzer while you are performing these steps. Be sure the SRD is not being overdriven, watch for the signal dropping out or showing unstable responses.

35. Select the YTM bias offset adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (MENU DOWN) until #22 YTM BIAS OFS is displayed.
    - Press (ENTER). The YTM bias offset adjustment is now selected.
36. Adjust the YTM bias offset by using the following steps:
    - Set the marker of the spectrum analyzer to 12.4 GHz.
    - Press the ↑ or ↓ keys to change the YTM bias offset value until the signal on the spectrum analyzer is peaked at 12.4 GHz. Be sure the SRD is not being overdriven.
37. Select the YTM bias gain adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (MENU DOWN) until #23 YTM BIAS GN is displayed.
    - Press (ENTER). The YTM bias gain adjustment is now selected.
38. Adjust the YTM bias gain by using the following steps:
    - Set the marker of the spectrum analyzer to 19.7 GHz.
    - Press the ↑ or ↓ keys to change the YTM bias gain value until the signal on the spectrum analyzer is peaked at 19.7 GHz.

39. Select the YTM bias offset adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (MENU UP) until **#22** YTM BIAS **OFS** is displayed.
    - Press [ENTER). The **YTM** bias offset adjustment is now selected.

40. Adjust the final **YTM** bias offset by pressing the (↓) key 15 times. This is to ensure that the SRD is not being overdriven. The final YTM bias offset is now set for band 3.

**Caution**

Do not use the UNDO option when performing the next step. Using the UNDO option will store invalid data that will be loaded the next time the instrument is powered on.

41. Select the store cal data test routine from the extended test menu of the tracking source by pressing the following tracking source keys:
    - Press (TEST).
    - Press (MENU DOWN) until **#28** STORE CAL DATA is displayed.
    - Press (ENTER). All values for band 3 are now stored into EEPROM.

    The SRD bias adjustment for band 3 is finished, now continue with the **YTM** filter adjustment for band 4.

### Adjust the YTM filter for band 4

The **YTM** filter and SRD bias adjustments for band 3 must be done before the **YTM** filter for band 4 can be adjusted. Steps 42 through 52 allow you to perform the **YTM** filter adjustments for band 4.

42. Set the HP **8562A** spectrum analyzer to the following:

    Frequency start ..... 19.031 **GHz**
    Frequency stop ..... **26.5 GHz**

43. Select the band lock mode from the extended adjust menu of the tracking source and lock it to band 4 by pressing the following tracking source keys:
    - Press (ADJUST).
    - Press [MENU DOWN] until **#4** BAND LOCK is displayed.
    - Press [ENTER).
    - Press 4, then (ENTER). The tracking source is now locked to band 4.

44. Select the YTM gain adjustment from the extended adjust menu of the tracking source and enter the YTM gain value by pressing the following tracking source keys:
    - Press (MENU DOWN) until #13 YTM GAIN is displayed.
    - Press (ENTER).
    - Enter the YTM GAIN value, calculated in step 10, into the tracking source.
    - Press (ENTER) to install this value. The YTM gain is now set for band 4.
45. Select the YTM breakpoint number 1 adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (MENU DOWN) until #15 YTM BP1 is displayed.
    - Press (ENTER).
    - Enter the YTM BP1 value, recorded in step 19, into the tracking source.
    - Press (ENTER) to install this value. The YTM breakpoint number 1 is now set for band 4.
46. Select the YTM breakpoint number 2 adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (MENU DOWN) until #16 YTM BP2 is displayed.
    - Press (ENTER).
    - Enter the YTM BP2 value, recorded in step 34, into the tracking source.
    - Press (ENTER) to install this value. The YTM breakpoint number 2 is now set for band 4.
47. Select the YTM offset adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (MENU UP) until #14 YTM OFFSET is displayed.
    - Press (ENTER).

    The YTM offset adjustment is now selected.
48. Adjust the YTM offset using the following steps:
    - Set the marker of the spectrum analyzer to 19.031 GHz.
    - Press the (↑) or (↓) keys to change the YTM offset value until the signal on the spectrum analyzer is peaked at 19.031 GHz.
49. Select the YTM breakpoint 3 adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (MENU DOWN) until #17 YTM BP3 is displayed.
    - Press (ENTER). The YTM breakpoint number 3 adjustment is now selected.

50. Adjust the YTM breakpoint number 3 using the following steps:
    - Set the marker of the spectrum analyzer to 22.75 GHz.
    - Press the ↑ or ↓ keys to change the YTM breakpoint number 3 value until the signal on the spectrum analyzer is peaked at 22.75 GHz.
51. Select the YTM breakpoint 4 adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press [MENU DOWN] until #18 YTM BP4 is displayed.
    - Press [ENTER]. The YTM breakpoint number 4 adjustment is now selected.
52. Adjust the YTM breakpoint number 4 using the following steps:
    - Set the marker of the spectrum analyzer to 26.5 GHz.
    - Press the ↑ or ↓ keys to change the YTM breakpoint number 4 value until the signal on the spectrum analyzer is peaked at 26.5 GHz.

    The YTM filter adjustment for band 4 is finished, now continue with the SRD bias adjustment for band 4.

### Adjust the SBD bias for band 4

The YTM filter adjustment for band 4 must be done before the SRD bias for band 4 can be adjusted. Steps 53 through 59 complete the YTM filter and SRD bias adjustment, and allow you to perform the SRD bias adjustments for band 4. You must constantly monitor the entire band displayed on the spectrum analyzer while you are performing these steps. Be sure the SRD is not being overdriven, watch for the signal dropping out or showing unstable responses.

53. Select the YTM bias offset adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press [MENU DOWN] until #22 YTM BIAS OFS is displayed.
    - Press [ENTER]. The YTM bias offset adjustment is now selected.
54. Adjust the YTM bias offset by using the following steps:
    - Set the marker of the spectrum analyzer to 20.0 GHz.
    - Press the ↑ or ↓ keys to change the YTM bias offset value until the signal on the spectrum analyzer is peaked at 20.0 GHz. Be sure the SRD is not being overdriven.
55. Select the YTM bias gain adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press [MENU DOWN] until #23 YTM BIAS GN is displayed.
    - Press [ENTER]. The YTM bias gain adjustment is now selected.

56. Adjust the **YTM** bias gain by using the following steps:
    - Set the marker of the spectrum analyzer to 26.5 **GHz.**
    - Press the ↑ or ↓ keys to change the **YTM** bias gain value until the signal on the spectrum analyzer is peaked at 26.5 **GHz.**
57. Select the **YTM** bias offset adjustment from the extended **adjust** menu of the tracking source by pressing the following tracking source keys:
    - Press (MENU UP) until **#22** YTM BIAS OFS is displayed.
    - Press (ENTER). The **YTM** bias offset adjustment is now selected.
58. **Adjust** the final YTM bias offset by pressing the ↓ key 15 times. This is to ensure that the SRD is not being overdriven. The final YTM bias offset is now set for band 4.

**Caution**

Do not use the UNDO option when performing the next step. Using the UNDO option will store invalid data that will be loaded the next time the instrument is powered on.

59. Select the store cal data test routine from the extended test menu of the tracking source by pressing the following tracking source keys:
    - Press (TEST).
    - Press (MENU DOWN) until **#28** STORE CAL DATA is displayed.
    - Press (ENTER). All values for band 4 are now stored into EEPROM.

### Store the values into EEPBOM

Steps 60 and 61 allow you to perform the Amplitude Peak Adjustment routine, then store the values into EEPROM.

60. Select the amplitude peak adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
    - Press (ADJUST).
    - Press (MENU DOWN) or (MENU UP) until **#1** AMPLITUDE PEAK is displayed.
    - Press (ENTER). The amplitude peak routine is now selected; the tracking source will now perform the routine.

      If the routine passes, YTM PEAK DONE is displayed on the tracking source. Continue with step 61.

      If the routine fails, YTM PEAK FAIL is displayed on the tracking source. There is probably a hardware problem, refer to Chapter 3 for further troubleshooting. After repairing the instrument, repeat the entire **SYTM** adjustment procedure beginning with **YTM** Bias Power Level routine.

**Caution**

Do not use the UNDO option when performing the next step. Using the UNDO option will store invalid data that will be loaded the next time the instrument is powered on.

61. Select the store cal data test routine from the extended test menu of the tracking source by pressing the following tracking source keys:
    - Press (TEST).
    - Press (MENU DOWN) until #28 STORE CAL DATA is displayed.
    - Press (ENTER). All values for the Amplitude Peak Adjustment routine are now stored into EEPROM.

    The YTM Filter and SRD bias adjustment is finished. This step completes the SYTM adjustments for the HP 85645A tracking source.

## Adjusting Low-Band Slope and ALC

The slope adjustment is necessary to correct for insertion losses that may occur in the tracking source. The slope correction is implemented by adding a voltage to the ALC circuitry. This compensates for RF insertion loss between the leveling coupler and front panel by increasing the output from the amplifier at the leveling coupler. The correction voltage is calculated from a straight line equation, using data obtained during this procedure.

This adjustment has three sections: adjust the low-band slope, adjust the ALC, and check the slope.

The ALC adjustment is done after the slope adjustment. The slope and ALC adjustments are dependent on each other; therefore, these adjustments may need to be repeated several times.

The following equipment is required for the Low-Band Slope and ALC adjustment:

Spectrum analyzer . . . . . HP 85628
Power meter . . . . . HP 4368
Power sensor . . . . . HP 8485A
Cable, BNC, 1.22 m ***(three*** required) . . . . HP part number 8120-5529
Cable, SMA, 1 m ***(two required)*** . . . . . HP part number 5061-5458

### Step 1. Adjust the low-band slope

This section establishes the initial slope correction value. During later iterations the correction value may differ from this established value. This difference is due to the ALC algorithm recalculating the slope value to account for changes made during the ALC adjustment. The ALC algorithm does this to maintain the correct slope.

The tracking source must be turned on and allowed to warm up for at least 1/2 hour before making any adjustments. It is acceptable to turn the power off briefly while making the following connections.

1. Connect the tracking source to a spectrum analyzer host.

   - Connect the BNC cables between the HP 85644A/85645A tracking source and the HP 85628 spectrum analyzer as described in the table below.

| From Tracking Source Connector | To HP 8562A Connector |
|---|---|
| 10 MHz IN | 10 MHz REF IN/OUT |
| SWP+TUNE IN | 0.5V/GHz OUTPUT |
| BLANK IN | BLANKING OUTPUT |

   - Connect an SMA cable from the HP 85644A/85645A tracking source LO INPUT connector to the LO OUTPUT connector of the HP 8562A spectrum analyzer.

2. Conllgure the tracking source and HP 8562A spectrum analyzer by pressing the following tracking source keys:
   - Press (PRESET).
   - ▷□ℳ•• (CONFIG).
   - Press (MENU DOWN) until CNFG #1 HOST SELECT is displayed.
   - Press (ENTER) to select the host instrument.
   - Press (↑) or (↓) until CNFG #1 HP 8562 is displayed.
   - Press (ENTER); CNFG #1 HP 8562 ← is displayed.

   The HP 8562A spectrum analyzer is now selected as host instrument to the tracking source.

3. Set up the equipment to adjust the low-band slope using the following steps:

   a Set the HP 8562A spectrum analyzer to the following:

   Frequency span . . . . . 0 Hz
   Center frequency . . . . . 300 MHz

   - Connect the HP 84858 power sensor to the HP 436A power meter.
   - Zero and calibrate the power meter and power sensor, as described in the power meter operation manual.

4. Set the low frequency corrected power (PWR_LOW) value by using the following steps:
   - Adjust the power meter for the calibration factor of the power sensor at 300 MHz.
   - Connect the power meter to the tracking source RF OUTPUT connector.
   - Press [POWER LEVEL] on the tracking source to adjust the power level.
   - Press (↑) or (↓) on the tracking source until 0 ±.01 dBm is displayed on the power meter.
   - Record the PWR_LOW value displayed on the power meter.

     PWR-LOW = _____dBm

5. Measure the high frequency corrected power (PWR-HI) value, using the following steps to measure the PWR-HI value:
   - Set the HP 8562A center frequency to 2.45 GHz.
   - Adjust the power meter for the calibration factor of the power sensor at 2.45 GHz.
   - Record the measured power (PWR-HI) displayed on the power meter.

     PWR-HI = _____dBm

6. Select the low-band slope adjustment from the extended adjust menu of the tracking source. Select the adjustment by pressing the following tracking source keys:
   - Press (ADJUST).
   - Press the (7) and (GHz) keys at the same time until EXTENDED MENU is momentarily displayed.
   - Press (MENU DOWN) until **#7** SLOPE LO BAND is displayed.
   - Press [ENTER). The low-band slope adjustment is now selected and the initial slope correction value is displayed on the tracking source.
7. Calculate the slope correction value, using the following steps:
   - Record the initial slope correction factor ( from the tracking source display).

     initial slope correction = _____dB/GHz
   - Calculate the slope correction value using the values recorded above and in steps 4 and 5. The slope correction value is calculated using the equation below. The slope correction must always be greater than or equal to 0 **dB/GHz.** Record this value below.

     [(PWR-LOW – PWR-HI **dBm)/2.15 GHz]** + initial slope correction = slope correction

     calculated slope correction = _____**dB/GHz**
8. Adjust the low-band slope of the tracking source.

   Press the (⇧) or (⇩) keys to adjust the slope correction value until it matches the value calculated in step 7.
9. Verify that the difference between the new slope correction value and the old value is less than **±0.5 dB.** If the difference is greater than this, repeat steps 4 through 8 until the change in the slope correction is within the **±0.5 dB** limit.
10. Press (ENTER) on the tracking source. The tracking source displays the following:

    ENTER TO STORE
11. Press (ENTER) to store the correction values into EEPROM.

## Step 2. Adjust the ALC

This section of the adjustment procedure aligns the vernier power output. This adjustment is interactive with the slope correction adjustment.

1. Set up the tracking source so that you can adjust the ALC by pressing the following tracking source keys:
   - Press (CW).
   - Press 300 (MHz).

2. Adjust the power meter for the calibration factor of the power sensor at 300 MHz.

3. Select the low-band ALC adjustment from the extended adjust menu of the tracking source. Select the adjustment by pressing the following tracking source keys:

   - Press (ADJUST).
   - Press the (7) and (GHz) keys at the same time until EXTENDED MENU is momentarily displayed.
   - Press (MENU DOWN) until #8 ALC LO BAND is displayed.
   - Press (ENTER). The low-band ALC adjustment is now selected.

4. Adjust the ALC low band by performing the following steps for each DAC setting. The tracking source will display a power level that corresponds to the power it believes is being output. The corrected output power is entered into EEPROM for each DAC setting. The tracking source will then recalculate its ALC correction so that the displayed (programmed) output power is accurate.

   - Read the power level displayed on the power meter.
   - Enter the power into the tracking source.

     After each entry the tracking source will step to the next DAC setting and change the displayed power out for the entire vernier range.

     If the entry is correct and does not need to be changed, press (ENTER) to bypass this entry.

     If you make a mistake while entering the corrected power, press the (↑) or (↓) keys to retrieve and correct a previous entry.

   - Repeat these steps until the message ENTER TO STORE appears on the tracking source.

5. Press (ENTER) to store the cal values in EEPROM.

6. Check the front-panel ERR indicator.

   - If the ERR indicator is not lit proceed with "Step 3. Check the slope".
   - If the ERR indicator is lit repeat this section ("Step 2. Adjust the ALC").

## Step 3. Check the slope

The slope correction and the ALC adjustments are interactive. The most accurate slope correction value may be different than the value that was established in "Step 1. Adjust the low-band slope.' Therefore, it is necessary to check the slope correction.

1. Check the slope by performing steps 2 through 11 of "Step 1. Adjust the low-band slope. "
2. Record the new slope correction value.

   new slope correction = _____dB/GHz

3. Compare this new slope correction value to the slope correction value established in step 7 of the low-band slope adjustment.
   - If the new slope correction value is changed more than ±0.5 dB it is necessary to repeat "Step 1. Adjust the low-band slope" and "Step 2. Adjust the ALC" until the slope correction value is within the ±0.5 dB limit.
   - If the new slope correction value is changed less than ±0.5 dB the adjustment is finished.

## Adjusting High-Band Slope and ALC

The slope adjustment is necessary to correct for insertion losses that may occur in the tracking source. The slope correction is implemented by adding a voltage to the ALC circuitry. This compensates for RF insertion loss between the leveling coupler and front panel by increasing the output from the amplifier at the leveling coupler. The correction voltage is calculated from a straight line equation, using data obtained during this procedure.

This adjustment has three sections: adjust the high-band slope, adjust the ALC, and check the slope.

The ALC adjustment is done after the slope adjustment. The slope and ALC adjustments are dependent on each other; therefore, these adjustments may need to be repeated several times.

The following equipment is required for the High-Band Slope and ALC adjustment:

Spectrum analyzer ..... HP 8562A
Power meter ..... HP 4368
Power sensor ..... HP 8485A
Cable, BNC, 1.22 m *(three* required) . . . . HP part number 8120-5529
Cable, SMA, 1 m *(two required)* . . . . . HP part number 5061-5458

### Step 1. Adjust the high-band slope

This section establishes the initial slope correction value. During later iterations the correction value may differ from this established value. This difference is due to the ALC algorithm recalculating the slope value to account for changes made during the ALC adjustment. The ALC algorithm does this to maintain the correct slope.

The tracking source must be turned on and allowed to warm up for at least 1/2 hour before making any adjustments. It is acceptable to turn the power off briefly while making the following connections.

1. Connect the tracking source to a spectrum analyzer host.
   - Connect the BNC cables between the HP 85644A/85645A tracking source and the HP 8562A spectrum analyzer as described in the table below.

| From Tracking Source Connector | To HP 8562A Connector |
|---|---|
| 10 MHz IN | 10 MHz REF IN/OUT |
| SWP+TUNE IN | 0.5V/GHz OUTPUT |
| BLANK IN | BLANKING OUTPUT |

   - Connect an SMA cable from the HP 85644A/85645A tracking source LO INPUT connector to the LO OUTPUT connector of the HP 8562A spectrum analyzer.

2. Configure the tracking source and HP 8562A spectrum analyzer by pressing the following tracking source keys:
   - Press (PRESET).
   - Press (CONFIG).
   - Press (MENU DOWN) until CNFG #1 HOST SELECT is displayed.
   - Press (ENTER) to select the host instrument.
   - Press (↑) or (↓) until CNFG #1 HP 8562 is displayed.
   - Press (ENTER); CNFG #1 HP 8562 ← is displayed.

   The HP 8562A spectrum analyzer is now selected as host instrument to the tracking source.
3. Set up the equipment to adjust the high-band slope using the following steps:
   - Set the HP 8562A spectrum analyzer to the following:

     Frequency span ..... 0 Hz
     Center frequency ..... 3 GHz
   - Connect the HP 8485A power sensor to the HP 436A power meter.
   - Zero and calibrate the power meter and power sensor, as described in the power meter operation manual.
4. Set the high frequency corrected power (PWR-LOW) value by using the following steps:
   - ' Adjust the power meter for the calibration factor of the power sensor at 3 GHz.
   - Connect the power meter to the tracking source RF OUTPUT connector.
   - Press (POWER LEVEL) on the tracking source to adjust the power level.
   - Press (↑) or (↓) on the tracking source until 0 ±.01 dBm is displayed on the power meter.
   - Record the PWR-LOW value displayed on the power meter.

     PWR-LOW = _____dBm

5. Measure the high frequency corrected power (PWR-HI) value.

   The following steps are necessary to measure the PWR-HI value:

   - Set the HP **8562A** center frequency:

     If you have an HP **85644A** tracking source set the center frequency to 6.0 **GHz.** Then adjust the power meter for the calibration factor of the power sensor at 6.0 **GHz.**

     If you have an HP **85645A** tracking source set the center frequency to 23.0 **GHz.** Then adjust the power meter for the calibration factor of the power sensor at 23.0 **GHz.**

   - Record the measured power (PWR-HI) displayed on the power meter.

     PWR-HI = measured power x calibration factor

     PWR-HI = _____ **dBm**

6. Select the high-band slope adjustment from the extended adjust menu of the tracking source. Select the adjustment by pressing the following tracking source keys:

   - ▷□ℳ•• (ADJUST).
   - Press the (7) and (GHz) keys at the same time until EXTENDED MENU is momentarily displayed.
   - Press (MENU DOWN) until **#9** SLOPE HI BAND is displayed.
   - Press (ENTER). The high-band slope adjustment is now selected and the initial slope correction value is displayed on the tracking source.

7. Calculate the slope correction value, using the following steps:

   - Record the initial slope correction factor (from the tracking source display).

     initial slope correction = _____ dB/GHz

   - Calculate the slope correction value using the values recorded above and in steps 4 and 5. The slope correction value is calculated using the equation below. The slope correction must always be greater than or equal to 0 **dB/GHz.** Record this value below

     The frequency band value used in this equation is 3 **GHz** for an HP **85644A** tracking source or 20 **GHz** for an HP **85645A** tracking source.

     [(**PWR_LOW** – PWR-HI dBm)/frequency band] + initial slope correction = slope correction

     calculated slope correction = _____ dB/GHz

8. Adjust the high-band slope of the tracking source.

   Press the ⇧ or ⇩ keys to adjust the slope correction value until it matches the value calculated in step 7.

9. Verify that the difference between the new slope correction value and the old value is less than ±0.5 dB. If the difference is greater than this, repeat steps 4 through 8 until the slope correction is within the ±0.5 dB limit.

10. Press (‘ENTER) on the tracking source. The tracking source displays the following:

    **ENTER TO** STORE

11. Press (ENTER) to store the correction values into EEPROM.

## Step 2. Adjust the ALC

This section of the adjustment procedure aligns the vernier power output. This adjustment is interactive with the slope correction adjustment.

1. Set up the tracking source so that you can adjust the ALC. Perform the setup by pressing the following tracking source keys:
   - Press (CW).
   - Press 3 (GHz).
2. Adjust the power meter for the calibration factor of the power sensor at 3 GHz.
3. Select the high-band ALC adjustment from the extended adjust menu of the tracking source. Select the adjustment by pressing the following tracking source keys:
   - Press (ADJUST).
   - Press the (7) and (GHz) keys at the same time until EXTENDED MENU is momentarily displayed.
   - Press (MENU DOWN) until #10 ALC HI BAND is displayed.
   - Press (ENTER). The high-band ALC adjustment is now selected.

4. Adjust the ALC high band by performing the following steps for each DAC setting. The tracking source will display a power level that corresponds to the power it believes is being output. The corrected output power is entered into EEPROM for each DAC setting. The tracking source will then recalculate its ALC correction so that the displayed (programmed) output power is accurate.

   - Read the power level displayed on the power meter.
   - Enter the power into the tracking source.

     After each entry the tracking source will step to the next DAC setting and change the displayed power out for the entire vernier range.

     If the entry is correct and does not need to be changed, press (ENTER) to bypass this entry.

     If you make a mistake while entering the corrected power, press the ↑ or ↓ keys to retrieve and correct a previous entry.

   - Repeat these steps until the message ENTER TO STORE appears on the tracking source.

5. Press (ENTER) to store the cal values in EEPROM.
6. Check the front-panel ERR indicator.
   - If the ERR indicator is not lit proceed with the "Step 3. Check the Slope" section.
   - If the ERR indicator is lit repeat this section ("Step 2. Adjust the ALC").

## Step 3. Check the Slope

The slope correction and the ALC adjustments are interactive. The most accurate slope correction value may be different than the value that was established in "Step 1. Adjust the high-band slope.' Therefore, it is necessary to check the slope correction.

1. Check the slope by performing steps 2 through 11 of "Step 1. Adjust the high-band slope."
2. Record the new slope correction value.

   new slope correction = _____ dB/GHz

3. Compare this new slope correction value to the slope correction value established in step 7 of the high-band slope adjustment.
   - If the new slope correction value is changed more than ±0.5 dB it is necessary to repeat "Step 1. Adjust the high-band slope" and "Step 2. Adjust the ALC" until the change in the slope correction value is within the ±0.5 dB limit.
   - If the new slope correction value is not changed the adjustment is flnished.

## Adjusting the Frequency Accuracy

The frequency accuracy of the tracking source must be adjusted for operation when the instrument is not locked to the LO of a host. The adjustment requires that the tracking source step through various output frequencies while the operator enters in the actual measured frequency values. After the last measured frequency is entered, an internal routine calculates the tuning points that produce the correct output frequencies.

The following equipment is required for the frequency accuracy adjustment:

Spectrum analyzer ..... HP 8562A
Cable, BNC, 1.22 m ..... HP part number 81205529

The tracking source must be turned on and allowed to warm up for at least 1/2 hour before making any adjustments. It is acceptable to turn the power off briefly while making the following connections.

1. Connect the tracking source to the spectrum analyzer.

   Connect a BNC cable between the RF OUTPUT of the HP 85644A/85645A tracking source and the RF INPUT of the HP 8562A spectrum analyzer. ***Do not connect any other signals between the two instruments.***

2. Set the equipment to adjust the frequency accuracy by using the following steps:

   - Set the HP 8562A spectrum analyzer to the following:

     Frequency span ..... 500 MHz
     Reference level ..... 10 dBm
     Scale ..... 10 dB/div
     Frequency count ..... on

   - Press (CW) on the tracking source to enter CW mode.

3. Select the CW accuracy adjustment from the extended adjust menu of the tracking source. Select the adjustment by pressing the following tracking source keys:

   - Press (ADJUST).
   - Press the (7) and (GHz) keys at the same time until `EXTENDED MENU` is momentarily displayed.
   - Press (MENU DOWN) until `# 11 CW ACCURACY` is displayed.
   - Press (ENTER). The frequency accuracy adjustment is now selected.

4. Adjust the frequency accuracy by using the following steps:
   - Set the spectrum analyzer center frequency to the frequency that is displayed on the tracking source.
   - Press (PEAK SEARCH) on the spectrum analyzer then let the spectrum analyzer take at least Ave sweeps to allow the CW output to settle.
   - On the tracking source, enter the measured frequency, which is displayed on the spectrum analyzer as the frequency count (CNT). The tracking source will then step to a new frequency.
   - Repeat these steps until the message ENTER TO STORE appears on the tracking source.
5. Press (ENTER) on the tracking source to store the values in EEPROM.
6. Check the frequency accuracy by using the following steps:
   - Press (CW) on the tracking source to enter CW mode.
   - Set the tracking source and the spectrum analyzer to the first frequency below.

| Frequency for an HP 85644A | Frequency for an HP 85645A |
|---|---|
| 10.0 MHz | 10.0 MHz |
| 1.25 GHz | 1.24 GHz |
| 2.5 GHz | 2.5 GHz |
| 2.501 GHz | 5.0 GHz |
| 6.5 GHz | 7.0 GHz |
| | 10.0 GHz |
| | 15.0 GHz |
| | 20.0 GHz |
| | 26.5 GHz |

   - Verify the measured frequency is within 5 MHz of the desired frequency.
   - Change to the next frequency setting; repeat the steps until all the frequency points have been checked.

## Adjusting the Internal 10 MHz Reference

The internal 10 MHz reference can have an error of several **kHz.** This could develop into an error of several MHz in low band, creating a large tracking error. The following procedure removes a large part of this error. Make this adjustment at a frequency of 1 **GHz.**

The procedure is similar to adjusting for tracking or preselector error. The tune frequency of the internal 10 MHz reference will be changed, and the response will be watched on the spectrum analyzer display. As the response moves, the user will attempt to maximize it. Narrowing the resolution bandwidth in the middle of the process makes the response of the spectrum analyzer more sensitive.

The following equipment is required for the internal 10 MHz reference adjustment:

Spectrum analyzer . . . . . HP **8562A**
Cable, BNC, 1.22 m ***(two required)*** . . . . . HP part number 8120-5529
Cable, SMA, 1 m ***(two required)*** . . . . . HP part number 5061-5458

The tracking source must be turned on and allowed to warm up for at least **1/2** hour before making any adjustments. It is acceptable to turn the power off briefly while making the following connections.

1. Connect the tracking source to a spectrum analyzer host.

   - Connect the BNC cables between the HP **84645A** tracking source and the HP **8562A** spectrum analyzer as described in the table below.

| From HP 85645A Connector | To HP 8562A Connector |
|---|---|
| SWP+TUNE IN | 0.5V/GHz OUTPUT |
| BLANK IN | BLANKING OUTPUT |

   - Connect the SMA cables between the HP **85645A** tracking source and the HP **8562A** spectrum analyzer as described in the table below.

| From HP 85645A Connector | To HP 8562A Connector |
|---|---|
| RF OUT | RF INPUT |
| LO INPUT | LO OUTPUT |

2. Configure the tracking source and HP 8562A spectrum analyzer by pressing the following tracking source keys:
   - Press (PRESET).
   - Press (CONFIG).
   - Press (MENU DOWN) until CNFG Xl HOST SELECT is displayed.
   - Press (ENTER) to select the host instrument.
   - Press (↑) or (↓) until CNFG #1 HP 8562 is displayed.
   - Press (ENTER); CNFG #1 HP 8562 ← is displayed.

   The HP 8562A spectrum analyzer is now selected as host instrument to the tracking source.

3. Set the equipment to adjust the internal 10 MHz reference by setting the HP 8562A spectrum analyzer to the following:

   Frequency span ..... 0 Hz
   Center frequency ..... 1 GHz
   Resolution bandwidth ..... 1 MHz

4. Select the internal 10 MHz reference adjustment from the extended adjust menu of the tracking source by pressing the following tracking source keys:
   - Press (ADJUST).
   - Press the (7) and (GHz) keys at the same time until EXTENDED MENU is momentarily displayed.
   - Press (MENU DOWN) until #12 INT REFERENCE is displayed.
   - Press (ENTER). The 10 MHz reference adjustment is now selected.

   The tracking source will display the following messages:

   REMOVE EXT REF (displayed for 2 seconds)

   PRESSENTER

5. Adjust the internal 10 MHz reference by using the following steps:
   - Make sure the 10 MHz IN connector is not connected to the tracking source.
   - Press (ENTER) on the tracking source. The tracking source displays the following:

     OFS 0Hz
   - While observing the trace on the spectrum analyzer, use the (↑) or (↓) keys on the tracking source to peak the trace. Narrow the spectrum analyzer resolution bandwidth as the peak is approached to improve the sensitivity. This will insure that the signal is peaked.
   - After the trace is peaked, press (ENTER) on the tracking source. The tracking source displays the following:

     ENTER TOSTONE
   - Press (ENTER) to store the correction value in EEPROM.

# 2

# Self-Test Diagnostics

In addition to the power-on diagnostics routine that is run every time the instrument is turned on, the tracking source has an internal self-test diagnostics routine. The self-test diagnostics routine consists of several diagnostic tests. This chapter is organized into the following sections:

**Self-Test Diagnostics Procedure.**
A procedure for selecting and performing the self-test diagnostics procedure.

**Self-Test Diagnostic Routine Failures.**
Information about identifying which diagnostic test has failed and monitoring diagnostic signals.

**Diagnostic-Test Descriptions.**
A description of each diagnostic test, including related error messages, tests, and adjustments.

## Self-Test Diagnostics Procedure

The power-on diagnostics routine must pass before the user can successfully run the self-test diagnostic routine. To select the self-test diagnostic routine press the following tracking source keys:

- Press [TEST.
- Press (MENU DOWN] until TEST #1 SELF TEST appears on the tracking source display.
- Press (ENTER).

The self-test routine has been selected and will now be performed.

The tracking source will set itself to several known states, then check various points in the circuitry for the proper levels of operation. If a point does not meet defined limits, the self-test routine stops and an error message about the failure is displayed. If the self-test passes, TEST #1 SELF TEST PASSED is displayed.

## Self-Test Diagnostic Routine Failures

It is easy to identify which diagnostic test has failed. Refer to Table 2-1 and find the error message that was displayed on the tracking source when the self-test routine failed. The related diagnostic test is listed after the error message. To isolate the problem further go to the description for the related diagnostic test in this chapter.

**Table 2-1. Self Test Diagnostic Error Messages**

| Error Message | Related Diagnostic Test |
|---|---|
| ERR 801 MOTHER BUS | 1. Bus Test |
| ERR 802 FNT PANEL BUS | 1. Bus Test |
| ERR 803 INT BUS FAILURE | 1. Bus Test |
| ERR 804 ADC GND INPUT | 2. MUX and ADC |
| ERR 805 ADC VERF INPUT | 2. MUX and ADC |
| ERR 806 CONTRL REVISION | 3. Controller Board Revision Check |
| ERR 807 ADC 24V INPUT | 4. + 24 V Supply |
| ERR 808 ADC/MOD 7V INPUT | 5. Modulator Amplifier +7 V Supply |
| ERR 809 ADC/MOD -3V INPT | 6. Modulator Amplifier – 3 V Supply |
| ERR 810 HIGH BAND SWITCH | 7. High- and Low-Band Switch |
| ERR 811 LOW BAND SWITCH | 7. High- and Low-Band Switch |
| ERR 812 LOW BAND PWR OFF | 8. Low-Band Power |
| ERR 813 LOW BAND PWR ON | 8. Low-Band Power |
| ERR 814 RF ASSY REV | 9. RF Board Revision Check |
| ERR 815 ADC/RF GND INPUT | 10. Diagnostics Ground |
| ERR 816 ADC/RF VERF INPT | 11. + 10 V Reference |
| ERR 817 SWPTUNE OFF FINE | 12. Sweep + Tune Offset (fine) |
| ERR 818 SWPTUNE OFF COAR | 13. Sweep + Tune Offset (coarse) |
| ERR 819 SWPTUNE GAIN CW | 14. Sweep + Tune Gain CW Switch |
| ERR 820 UNLOCK SRCH NEG | 15. Unlock Detector and Search Up/Down |
| ERR 821 UNLOCK SRCH POS | 15. Unlock Detector and Search Up/Down |
| ERR 822 CW UNLOCK SRCH | 16. Unlock Detector and Search CW |
| ERR 823 MAIN COIL SUMAMP | 17. Main Coil Summing Amplifier |
| ERR 824 MAIN COIL BND SW | 18. Main Coil Band Switch |
| ERR 825 MAIN COIL DVR | 19. Main Coil Driver |
| ERR 826 FM DVR | 20. FM Coil Driver |
| ERR 827 PLL1 INTEGRATOR | 21. PLL1 Loop Integrator |

**Table 2-1. Self Test Diagnostic Error Messages (continued)**

| Error Message | Related Diagnostic Test |
|---|---|
| ERR 828 PLL2 INTEGRATOR | 22. PLL2 Loop Integrator |
| ERR 829 PLL3 INTEGRATOR | 23. PLL3 Loop Integrator |
| ERR 830 YTO INTEGRATOR | 24. YTO Loop Integrator |
| ERR 831 ALC PREAMP | 25. ALC Preamplifier |
| ERR 832 ALC COARSE DAC | 26. ALC Level DACs (coarse) |
| ERR 833 ALC FINE DAC | 27. ALC Level DACs (fine) |
| ERR 834 ALC SLOPE DAC | 28. ALC Slope DACs |
| ERR 835 YTO LEVELING | 29. YTO Leveling |
| ERR 836 ALC LOOP LO BAND | 30. ALC Loop Integrator |
| ERR 837 ALC LOOP HI BAND | 30. ALC Loop Integrator |
| ERR 838 SWP T BUFFER | 31. Sweep + Tune Buffers |
| ERR 839 YTM GAIN DAC | 32. YTM Gain |
| ERR 840 YTM BP3 DAC | 33. YTM Breakpoint 3 |
| ERR 841 YTM BP4 FREQ DAC | 34. YTM Breakpoint 4 Frequency |
| ERR 842 YTM BP4 DAC | 35. YTM Breakpoint 4 DAC |
| ERR 843 YTM OFFSET | 36. YTM Offset |
| ERR 844 YTM BP1 DAC | 37. YTM Breakpoint 1 |
| ERR 845 YTM BP2 DAC | 38. YTM Breakpoint 2 |
| ERR 846 YTM DRIVER | 39. YTM Drive |
| ERR 847 BIAS BAND OFFSET | 40. Bias Band Offset |
| ERR 848 BIAS OFFSET DAC | 41. Bias Offset |
| ERR 849 BIAS GAIN DAC | 42. Bias Gain |
| ERR 850 PWR LEVEL DAC | 43. Power Level Adjustment |
| ERR 851 SYTM BIAS DAC | 44. SYTM Bias |
| ERR 852 LEVEL AMP DAC | 45. Leveling Amplifier Driver Sense 1 |
| ERR 852 LEVEL AMP DAC | 46. Leveling Amplifier Driver Sense 2 |
| ERR 853 260 MHz OSC | 47. 260 MHz Low-Band 'lest |
| ERR 854 4.2 GHz OSC | 48. 4.2 GHz Low-Band Test |

## Diagnostic Signals

There are many different diagnostic and control signals throughout the instrument that are monitored and controlled by the self-test routine. Individual diagnostic signals can be monitored on a real time basis by accessing the #25 ADC VALUE and #26 SYTM VALUE functions under the extended test menu. Observing these signals under different instrument states can be helpful in troubleshooting a problem. Refer to chapters 4 and 5 for more information.

## Diagnostic-Test Descriptions

Each diagnostic test is described with a brief description of the test, a listing of error messages that are related to the diagnostic test, a troubleshooting checklist to help isolate the failure, and a list of related tests and adjustments. The diagnostic test descriptions are organized in the order they occur within the self-test routine.

## 1. Bus Test

This diagnostic test exercises the mother bus, the front-panel bus, and some buffers and **MUXes** on the **A2** Controller board assembly. The mother bus connects the **A3** RF assembly with the **A2** Controller assembly. The front-panel bus connects the Al Front Panel assembly with the **A2** Controller board assembly.

### If the test fails

The following error messages may be displayed on the tracking source:

| | |
|---|---|
| `ERR 801 MOTHER BUS` | A motherboard bus interface problem. |
| `ERR 802 FNT PANEL BUS` | A front-panel interface problem. |
| `ERR 803 INT BUS FAILURE` | An internal bus failure problem. |

The following checklist is provided to help isolate a bus test failure.

- Check the Mother-Bus Buffer block of the controller board assembly.
- Check the YTO Loop Digital Interface block of the RF board assembly.
- Check the Digital Control block of the RF board assembly
- Check the Timing block on the controller board assembly.
- Check the **MUXes** block on the controller board assembly.
- I Check the Front-Panel Buffers block on the controller board assembly.
- I Check that **W1** (the digital address and data bus cable) is connected and not defective.
- Check that the **W2** and **W3** cables between the controller and front-panel board assemblies are connected and not defective.
- Check the front-panel board assembly circuits.

## 2. MUX and ADC

This is a basic functional test of the MUX and ADC block of circuitry on the controller board assembly. The ADC attempts to make two measurements, the +5 V and ground. The +5 V that is measured is derived from the ADC's internal 10 V reference. The ADC's internal reference is divided through two 10 KΩ resistors to produce the +5 V. This +5 V is then sent through the ADC MUX to the ADC circuitry. If the ADC circuitry is not working properly, the diagnostic test routine cannot continue.

The following assumptions are made for the MUX and ADC diagnostic test to run:

- The + 5 V supply is operational.
- The power-on diagnostics passed.

### If the test fails

The following error messages may be displayed on the tracking source:

| | |
|---|---|
| ERR 804 ADC GND INPUT | An ADC ground input problem. |
| ERR 805 ADC VERF INPUT | An ADC voltage reference input problem. |

The following checklist is provided to help isolate a MUX and ADC failure.

•I Check the MUX and ADC block on the controller board assembly.

- ❑ Check the MUX and ADC block control signals.
- ❑ Check the ±15 V supplies
- ❑ Check the + 10 V reference on the controller board assembly.
- ❑ Check individual signals from the MUX through the ADC circuitry; perform the #25 ADC VALUE test.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST #25 ADC VALUE | This function monitors individual signals from the MUX through the ADC. |
| TEST #26 SYTM VALUE | This function monitors SYTM signals through the ADC. |

# 3. Controller Board Revision Check

This diagnostic test checks the controller board revision. The revision signal is a dc voltage that is produced through a resistor divider. The ends of the divider are tied to the ±15 V supplies The voltage will be different for each board revision. The voltage is routed through the diagnostic **MUXes** to the MUX and ADC block on the controller board assembly.

The firmware must know the revision of the board in order to perform the applicable tests using the correct test limits.

## If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 806 CNTRL REVISION | The **A2** controller assembly revision is unknown. |

The firmware does not recognize the revision of the controller board being tested. There may be some tests and test limits in the firmware that are not correct for this board revision.

If the revision is not recognized by the firmware:

- Update the firmware in the ROMs to a current revision. Contact your nearest service center (refer to Chapter 6).
- Troubleshoot the board assembly manually if there is still a problem with the revision code on the controller board assembly.

## Related tests and adjustments

'lest and adjustment functions are found under the extended [TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST **#26** SYTM VALUE | This function monitors **SYTM** signals through the ADC. (MUX signal **#26,** CNTL,BD,REV.) |

## 4. + 24 V Supply

This diagnostic test checks the ADC circuitry over an additional part of its range and increases confidence in the ADC operation. This is the first time that the diagnostic **MUXes** are selected.

The input for the **+24** V regulator is **+32.5** V. The tested signal comes from the **+24** V regulator through a resistor divider in the **+24** V supply block. It is then routed through the diagnostic **MUXes,** to the MUX and ADC block on the controller board assembly.

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| `ERR 807 ADC 24V INPUT` | An analog to digital 24 V input problem. |

The following checklist is provided to help isolate a failure with the **+24** V supply.

- Check the **+24** V block circuits on the controller board assembly.
- Check the **+32** V supply.
- Check the circuits and control signals that affect the **+24_DIAG** signal path from the controller board **+24** V block to the ADC circuitry.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| `TEST #26 SYTM VALUE` | This function monitors SYTM signals through the ADC. (MUX signal **#21, 24V_DIAG.**) |

# 5. Modulator Amplifier + 7 V Supply (HP 85645A only)

This diagnostic test checks the ADC circuitry over an additional part of its range and increases confidence in the ADC operation.

The input for the +7 V supply is + 15 V. The tested signal comes from an adjustable regulator that is set to +7.5 V. It is on the Mod Amp supplies block. The output is routed through the diagnostic MUXes, to the MUX and ADC block on the controller board assembly.

## If the test fails

The following error message may be displayed on the tracking source:

ERR 808 ADC/MOD 7V INPUT — An ADC +7 V input problem.

The following checklist is provided to help isolate a failure with the +7 v supply.

- Check the +7 V supply in the controller board assembly MOD AMP SUPPLIES block.
- Check the circuits in the controller board assembly DIAGNOSTICS MUXES block.
- Check the + 15 V supply on the controller board assembly.
- Check the circuits and control signals that affect the +7V_DIAG signal path from the controller board assembly MOD AMP SUPPLIES block to the ADC circuitry.

## Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

TEST #26 SYTM VALUE — This function monitors SYTM signals through the ADC. (MUX signal #15, 7V_DIAG.)

## 6. Modulator Amplifier -3 V Supply

This verifies the presence and operation of the -3 V supply to the A9 Modulator/Amplifier assembly. The -3 V supply is generated by connecting a 12 V zener diode to the -15 V supply.

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 809 **ADC/MOD –3V** INPT | An ADC Mod Amp -3 V input problem. |

The following checklist is provided to help isolate a failure with the -3 v supply.

- Check the MOD AMP SUPPLIES block in the controller board assembly.
- Check the -15 V supply on the controller board assembly.
- Check the modulator amplifier and modulator switch microcircuits.
- Check the circuits and control signals that affect the **–3V_DIAG** signal path from the controller board assembly MOD AMP SUPPLIES block to the ADC circuitry.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST **#26** SYTM VALUE | This function monitors **SYTM** signals through the ADC. (MUX signal **#27, –3V_DIAG.**) |

# 7. High-Band and Low-Band Switch (HP 85645A only)

The control for the high-band and low-band switch in the SYTM is set to the high-band position and the SW-DIAG signal from the diagnostic MUXes is checked to verify that the voltage is approximately -10 V. Then, the switch is set to the low-band position and the SW-DIAG signal is checked for a voltage of approximately + 10 V.

## If the test fails

The following error messages may be displayed on the tracking source:

| | |
|---|---|
| `ERR 810 HIGH BAND SWITCH` | The high-band switch operation does not meet test limits. |
| `ERR 811 LOU BAND SWITCH` | The low-band switch operation does not meet test limits. |

The following checklist is provided to help isolate a failure with the high-band and low-band switches of the HP 856458.

- ❑ Check the HI/LOW BAND SWITCH block of the controller board assembly.
- ❑ Check the control signals to the HI/LOW BAND SWITCH block of the controller board assembly.
- ❑ Check the ATTENUATOR LATCH block of the controller board assembly.
- •I Check the control signals to the ATTENUATOR LATCH block of the controller board assembly.
- ❑ Check the + 10 V reference on the controller board assembly.
- ❑ Check the circuits and control signals that affect the SW-DIAG signal path from the controller board assembly HI/LOW BAND SWITCH block to the ADC block.

## Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| `ADJ #4 BAND LOCK` | This function can be used to lock the tracking source to band 0 or band 1, while observing the display. |
| `TEST #25 ADC VALUE` | This function monitors individual signals from the MUX through the ADC. |
| `TEST #26 SYTM VALUE` | This function monitors SYTM signals through the ADC. |

## 8. Low-Band Power

The +20 V power to the low-band microcircuit is turned on and off. The diagnostic voltage is checked to verify that it changes to the expected values. When the low-band microcircuit is turned off the +20V status signal will be approximately 1.25 V.

### If the test fails

The following error messages may be displayed on the tracking source:

| | |
|---|---|
| ERR 812 LOU BAND PWR OFF | Unable to reduce low-band power to specified level. |
| ERR 813 LOW BAND PWR ON | Unable to increase low-band power to specified level. |

The following checklist is provided to help isolate a failure with the low-band power.

- Check the LOW BAND POWER block of the controller board assembly.
- Check the control signals to the LOW BAND POWER block of the controller board assembly.
- Check the +32.5 V supply on the controller board assembly.
- Check the ATTENUATOR LATCH block on the controller board assembly.
- Check the control signals to the ATTENUATOR LATCH block of the controller board assembly.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST #25 ADC VALUE | This function monitors individual signals from the MUX through the ADC. |
| TEST #26 SYTM VALUE | This function monitors SYTM signals through the ADC. |

# 9. RF Board Revision Check

This diagnostic test checks the RF board assembly revision. The revision signal is a dc voltage that is produced through a resistor divider. The ends of the divider are tied to the ±15 V supplies. The voltage will be different for each board revision. The voltage is routed through the diagnostic **MUXes** to the MUX and ADC block on the controller board assembly.

The **firmware** must know the revision of the board in order to perform the applicable tests using the correct test limits.

## If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 814 RF ASSY **REV** | The **A3** RF board assembly revision is unknown. |

The firmware does not recognize the revision of the RF board assembly being tested. There may be some tests and test limits in the firmware that are not correct for this board revision.

If the revision is not recognized by the firmware:

- Update the firmware in the ROMs to a current revision. Contact your nearest service center (refer to Chapter 6).
- Troubleshoot the board assembly manually if there is still a problem with the revision code on the RF board assembly.

## Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST **#25** ADC VALUE | This function monitors individual signals from the MUX through the ADC. (MUX signal **#27, RF_BD_REV.**) |

## 10. Diagnostics Ground

This diagnostic test selects and measures the ground on the input of one of the RF board assembly diagnostic **MUXes**. This is a simple test that involves few circuits and requires minimum control. It checks that the ADC is able to select and read the RF board assembly diagnostic voltages.

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 815 **ADC/RF** GND INPUT | The ADC RF board ground input value does not meet the test limit. |

The following checklist is provided to help isolate a failure with the low-band power.

- ☐ Check the ±15 V supplies.
- ☐ Check the circuits and control signals that affect the ground signal path from the RF board assembly DIAGNOSTICS MUX block to the ADC circuitry.
- ☐ Check that **W1** (the digital address and data bus cable) is not defective.
- ☐ Check individual signals from the MUX through the ADC circuitry; perform the **#25** ADC VALUE test.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST **#25** ADC VALUE | This function monitors individual signals from the MUX through the ADC. (MUX signal **#46**, GND.) |

# 11. + 10 V Reference

The + 10 V reference is used throughout the RF board assembly for proper operation. The + 10 V signal comes from the POWER SUPPLY FILTERING block. The + 10 V reference is divided through two 10 **KΩ** resistors, therefore, the measured voltage is + 5 V. One of the diagnostic **MUXes** selects the signal **and** sends it to the MUX and ADC block on the controller board assembly. The 10 V is divided to **+5** V because of the ADC input measurement limit.

## If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 816 **ADC/RF** VERF INPT | The ADC voltage reference input does not meet the test limit. |

The following checklist is provided to help isolate a failure with the + 10 V reference.

- Check the circuits in the POWER SUPPLY FILTERING block on the RF board assembly that include the + 10 V reference.
- Check the circuits and control signals that affect the **D_RF_10V_REF** signal path from POWER SUPPLY FILTERING block of the RF board assembly to the ADC circuitry.
- Check that **W1** (the digital address and data bus cable) is not defective.

## Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and [ADJUST) key menus They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST **#25** ADC VALUE | This function monitors individual signals from the MUX through the ADC. (MUX signal **#24, D_RF_10V_REF.**) |

## 12. Sweep + Tune Offset (fine)

This is a range and monotonicity test of the sweep + tune offset (fine) DAC. This is an **8-bit** dac

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| `ERR 817 SWPTUNE OFF FINE` | The sweep + tune offset (fine) DAC does not meet the test limit. |

The following checklist is provided to help isolate a failure with the sweep + tune offset **(fine)** DAC.

- Check the sweep + tune offset (fine) DAC on the RF board assembly. Use the `TEST #8 S+T OFFSET F` function to access the DAC. Refer to Chapter 4.
- Check that the power supplies to the RF board assembly are functional.
- Check the circuits and control signals that affect the **D_YTO_OFFS_F** signal path from the SWEEP + TUNE OFFSET block to the ADC circuitry.
- Check that **W1** (the digital address and data bus cable) is not defective.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| `TEST #8 S+T OFFSET F` | This function monitors and can set the sweep + tune offset fine DAC. |
| `TEST #25 ADC VALUE` | This function monitors individual signals from the MUX through the ADC. (MUX signal `#22, D,YTO,OFFS,F.`) |

# 13. Sweep + Tune Offset (coarse)

This is a range **and** monotonicity test of the sweep + tune offset (coarse) DAC. This is a **12-bit** dac

## If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 818 SWPTUNE OFF COAR | The sweep + tune offset (coarse) DAC does not meet the test limit. |

The following checklist is provided to help isolate a failure with the sweep + tune offset (coarse) DAC.

- Check the sweep + tune offset (coarse) DAC on the RF board assembly. Use the TEST **#7** S+T OFFSET C function to access the DAC. Refer to Chapter 4.
- Check the power supplies to the RF board assembly
- Check the circuits and control signals that affect the D-YTO-OFFS-C signal path from the SWEEP + TUNE OFFSET block on the RF board assembly to the ADC circuitry.
- Check that **W1** (the digital address and data bus cable) is not defective.

## Related tests and adjustments

**Test** and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST **#7** S+T OFFST C | This function monitors and can set the sweep + tune offset coarse DAC. |
| TEST **#25** ADC VALUE | This function monitors individual signals from the MUX through the ADC. (MUX signal **#21,** D,YTO,OFFS,C.) |
| TEST **#26** SYTM VALUE | This function monitors SYTM signals through the ADC. |

## 14. Sweep + Tune Gain CW Switch

The instrument is set to the CW mode. This diagnostic test sets the CW switch, then measures the voltage.

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| `ERR 819 SWPTUNE GAIN CW` | The sweep + tune gain CW switch does not meet the test limit. |

The following checklist is provided to help isolate a failure with the sweep + tune gain CW switch block.

- Check the SWEEP + TUNE GAIN block on the RF board assembly.
- Check the circuits and control signals in and to the YTO LOOP DIGITAL INTERFACE block on the RF board assembly.
- Check the power supplies to the RF board assembly.
- Check the circuits and control signals that affect the **UN_S+T** signal path from the SWEEP + TUNE GAIN block on the RF board assembly to the ADC circuitry.
- Check that **W1** (the digital address and data bus cable) is not defective.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| `TEST #6 S+T GAIN` | This function monitors and can set the sweep + tune gain DAC. |
| `TEST #25 ADC VALUE` | This function monitors individual signals from the MUX through the ADC. (MUX signal `#0, SWEEP+TUNE.`) |

# 16. Unlock Detector and Search Up/Down

This diagnostic test momentarily sets the output of the UNLOCK DETECTOR AND SEARCH circuitry to its limits and measures the values.

## If the test fails

The following error messages may be displayed on the tracking source:

| | |
|---|---|
| `ERR 820 UNLOCK SRCH NEG` | The unlock detector and search down circuits do not meet the test limits. |
| `ERR 821 UNLOCK SRCH POS` | The unlock detector and search up circuits do not meet the test limits. |

The following checklist is provided to help isolate a failure with the unlock detector and search up/down.

- Check the UNLOCK DETECTOR AND SEARCH block of the RF board assembly.
- Check the circuits and control signals that affect the D-YTO-UNLK signal path from the UNLOCK DETECTOR SEARCH block on the RF board assembly to the ADC circuitry.

## Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| `TEST #9 YTO LATCH 1` | This monitors the current YTO state. |
| `TEST #25 ADC VALUE` | This function monitors individual signals from the MUX through the ADC. (MUX signal **#17, D_YTO_UNLK**.) |

## 16. Unlock Detector and Search CW

This diagnostic test sets the tracking source to the CW mode. In this mode the input to the UNLOCK DETECTOR AND SEARCH circuitry should be set to 0 V. That value is measured.

### If the test fails

The following error messages may be displayed on the tracking source:

| | |
|---|---|
| ERR 822 CW UNLOCK SRCH | The unlock detector and CW search circuitry operations do not meet the test limits. |

The following checklist is provided to help isolate a failure with the unlock detector and search CW.

- Check the UNLOCK DETECTOR AND SEARCH block of the RF board assembly.
- Check the YTO LOOP DIGITAL INTEGRATOR block of the RF board assembly.
- Check the circuits and control signals that affect the **D_YTO_UNLK** signal path from the UNLOCK DETECTOR SEARCH block on the RF board assembly to the ADC circuitry.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST **#9** YTO LATCH 1 | This monitors the current YTO state. |
| TEST **#25** ADC VALUE | This function monitors individual signals from the MUX through the ADC. (MUX signal **#17,** D,YTO,UNLK.) |

# 17. Main Coil Summing Amplifier

This diagnostic test checks the output voltage of the main coil summing amplifier. This output voltage is the sum of voltages from several circuits By setting the tracking source to CW mode and to a frequency in band 1, all of the summing voltages can be canceled out except the voltage for the sweep + tune offset DACs. The sweep + tune offset (coarse) DAC is used to set the output of the main coil summing amplifier, then the output is measured.

## If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 823 MAIN COIL SUMAMP | The main coil summing amplifier does not meet the test limit. |

The following checklist is provided to help isolate a failure with the main coil summing amplifier.

- Check the MAIN COIL SUMMING AMPLIFIER block on the RF board assembly.
- Check the BAND LOCK RANGE SWITCH block on the RF board assembly.
- Check the circuits and control signals that affect the D-YTO-SUM signal from the MAIN COIL SUMMING AMPLIFIER block on the RF board assembly to the ADC circuitry.
- Check the power supplies to the RF board assembly.
- Check that W1 (the digital address and data bus cable) is not defective.

## Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST #25 ADC VALUE | This function monitors individual signals from the MUX through the ADC. (MUX signal #12, D_YTO_SUM.) |

## 18. Main Coil Band Switch

This diagnostic test sets the tracking source to CW and to each of the upper bands using the YTO latch 1. A voltage is read through the RF diagnostic **MUXes** and band to band comparisons are made.

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 824 MAIN COIL BND SW | The main coil band switch operation does not meet the test limits. |

The following checklist is provided to help isolate a failure with the main coil band switch.

- ❑ Check the MAIN COIL BAND SWITCH block on the RF board assembly.
- ❑ Check the BAND LOCK RANGE SWITCH block on the RF board assembly.
- ❑ Check the MAIN COIL LOW PASS FILTER block on the RF board assembly.
- ❑ Check the circuits and control signals that affect the **D_YTO_BAND** signal from the MAIN COIL BAND SWITCH block on the RF board assembly to the ADC circuitry. Use the TEST **#9** YTO LATCH 1 or TEST **#10** YTO LATCH 2 functions to manually set the YTO latch controls. Refer to Chapter 4.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST **#9** YTO LATCH 1 | This monitors the current YTO state. |
| TEST **#25** ADC VALUE | This function monitors individual signals from the MUX through the ADC. (MUX signal **#13, D_YTO_BAND.**) |

# 19. Main Coil Driver

This test examines the MAIN COIL DRIVER block on the RF board assembly. The instrument is set to CW mode in band 4. The sweep + tune offset DAC is set to 0 and 4095, and readings are taken and compared to the expected values.

## If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 825 MAIN COIL DVR | The main coil driver operation does not meet the test limits. |

The following checklist is provided to help isolate a failure with the main coil driver.

- Check the MAIN COIL DRIVER block of the RF board assembly.
- Check the **A4** YTO microcircuit.
- Check the **W7** cable assembly.
- Check the circuits and control signals that affect the **D_YTO_SENSE** signal from the MAIN COIL DRIVER block on the RF board assembly to the ADC circuitry.

## Related tests and adjustments

**Test** and **adjustment** functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST **#25** ADC VALUE | This function monitors individual signals from the MUX through the ADC. (MUX signal **#14,** D,YTO,SENSE.) |

## 20. FM Coil Driver

This diagnostic test measures the YTO FM coil driver voltage and verifies the value.

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 826 FM DVR | The FM coil driver operation does not meet specification. |

The following checklist is provided to help isolate a failure with the FM coil driver.

- Check the FM COIL DRIVER block on the RF board assembly.
- Check the **A4** YTO microcircuit.
- Check the **W7** cable assembly.
- Check the circuits and control signals that affect the **D_YTO_FM_DVR** signal from the FM COIL DRIVER block on the RF board assembly to the ADC circuitry.

### Related tests and adjustments

Test and adjustment functions are found under the extended [TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST **#25** ADC VALUE | This function monitors individual signals from the MUX through the ADC. (MUX signal **#23, D_YTO_FM_DVR.**) |

# 21. PLL1 Loop Integrator

The phase locked loop 1 (PLL1) oscillator is set to 120 MHz for the low setting and 200 MHz for the high settings. The integrator voltage is measured at these two frequencies to check that it is working within known test limits. The measured signal comes from the PLL1 LOOP INTEGRATOR block on the RF board assembly. It is routed through the diagnostic MUXes, to the MUX and ADC block on the controller board assembly.

## If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 827 PLL1 INTEGRATOR | The phase locked loop 1 integrator operation does not meet the test limits. |

The following checklist is provided to help isolate a failure with PLL1.

- ❑ Check the PLL1 PHASE/FREQUENCY DETECTOR block on the RF board assembly.
- ❑ Check the PLL1 LOOP INTEGRATOR block on the RF board assembly.
- ❑ Check the PLL1 LOOP FILTER (500 Hz) block on the RF board assembly.
- ❑ Check the PLL1 OSCILLATOR (120 – 200 MHz) block on the RF board assembly.
- ❑ Check the PLL1 LOOP DIVIDER block on the RF board assembly. Use the TEST #17 PLL1 DIV function to determine the internal value for the divider number in PLL1. Refer to Chapter 4.
- ❑ Check the DIGITAL CONTROL block on the RF board assembly.
- ❑ Check the PLL1 & PLL3 FREQUENCY REFERENCES block on the RF board assembly. Use the TEST #18 PLL1 FRQ function to determine the internal value for the frequency of PLL1. Refer to Chapter 4.
- ❑ Check the 10 MHz INPUT AMPLIFIER block on the RF board assembly.
- ❑ Check the SWITCHED 10 MHz OSCILLATOR block on the RF board assembly.
- ❑ Check the circuits and control signals that affect the D_PLL1_INTGR signal path from the PLL1 LOOP INTEGRATOR block on the RF board assembly to the ADC circuitry.

## Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST #17 PLL1 DIV | This function monitors the internal divider number in phase locked loop 1. |
| TEST #18 PLL1 FRQ | This function displays the expected value of the frequency of phase locked loop 1. |

# 22. PLL2 Loop Integrator

The phase locked loop 2 (PLL2) diagnostic test is very similar to the phase locked loop 1 (PLL1) diagnostic test. The PLL2 oscillator range is 200 kHz, from 240.3 MHz to 240.5 MHz. The frequency of PLL2 is dependent on the frequency of PLL1. PLL1 will be used to adjust the PLL2 frequency. As the PLL1 frequency is adjusted, the voltage of the PLL2 LOOP INTEGRATOR is measured. The measured signal comes from the PLL2 LOOP INTEGRATOR block on the RF board assembly, it is routed through the diagnostic MUXes, to the MUX and ADC block on the controller board assembly.

## If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 828 PLL2 INTEGRATOR | The phase locked loop 2 integrator operation does not meet the test limits. |

The following checklist is provided to help isolate a failure with PLL2.

- Check the PLL2 PHASE/FREQUENCY DETECTOR block on the RF board assembly. Use the TEST #19 PLL2 FRQ function to determine the internal value for the frequency of PLL2. Refer to Chapter 4.
- Check the PLL2 LOOP INTEGRATOR block on the RF board assembly.
- Check the PLL2 OSCILLATOR (120 – 200 MHz) block on the RF board assembly.
- Check the PLL2 IF (0.3 – 0.5 MHz) block on the RF board assembly.
- Check the PLL1 OUTPUT TO DIVIDER (divide by 400) block on the RF board assembly.
- Check the 60 MHz GENERATOR block on the RF board assembly.
- Check the PLL2 FREQUENCY REFERENCE block on the RF board assembly.
- Check the circuits and control signals that affect the D_PLL2_INTGR signal path from the PLL2 LOOP INTEGRATOR block on the RF board assembly to the ADC circuitry.

## Related tests and adjustments

Test and adjustment functions are found under the extended [TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST #19 PLL2 FRQ | This function displays the expected value of the frequency of phase locked loop 2. |

## 23. PLL3 Loop Integrator

The phase locked loop 3 (PLL3) diagnostic test is similar to the phase locked loop 1 (PLL1) diagnostic test. The frequency of the PLL3 oscillator can be adjusted two different ways:

- Adjust the PLL1 frequency.
- Use the dividers in PLL3.

For this test the PLL1 frequency is set to the center of its range at 160 MHz, then the PLL3 divider is used to change the PLL3 frequency.

The measured signal comes from the PLL3 LOOP FILTER block on the RF board assembly (it is routed through the diagnostic MUXes) to the MUX and ADC block on the controller board assembly.

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 829 PLL3 INTEGRATOR | The phase locked loop 3 integrator operation does not meet the test limits. |

The following checklist is provided to help isolate a failure with PLL3.

- ❑ Check the PLL3 MIXER block on the RF board assembly.
- ❑ Check the PLL3 IF (30 – 100 MHz) block on the RF board assembly.
- ❑ Check the PLL3 LOOP DIVIDER block on the RF board assembly. Use the TEST #20 PLL3 DIV or TEST #22 PLL3 OUTDIV functions to determine the internal value for the divider or the divider output of PLL3. Refer to Chapter 4.
- ❑ Check the PLL3 PHASE/FREQUENCY DETECTOR block on the RF board assembly.
- ❑ Check the PLL3 LOOP INTEGRATOR block on the RF board assembly.
- ❑ Check the PLL3 LOOP FILTER (100 kHz) block on the RF board assembly.
- ❑ Check the PLL3 OSCILLATOR (270 – 340 MHz) block on the RF board assembly.
- ❑ Check the PLL1 & PLL3 FREQUENCY REFERENCE block on the RF board assembly. Use the TEST #21 PLL3 FRQ function to determine the internal value for the frequency of PLL3. Refer to Chapter 4.
- ❑ Check the circuits and control signals that affect the D_PLL3_INTGR signal path from the PLL3 LOOP INTEGRATOR block on the RF board assembly to the ADC circuitry.

## Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST_) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions

| | |
|---|---|
| TEST **#20 PLL3** DIV | This function monitors the internal value of the divider number for phase locked loop 3. |
| TEST **#21 PLL3 FRQ** | This function displays the expected value of the frequency of phase locked loop 3. |
| TEST **#22 PLL3** OUT DIV | This function monitors the internal value of the divider number of the output of phase locked loop 3. |

## 24. YTO Loop Integrator

The range of the YTO loop integrator is measured by switching the YTO IF polarity bit of the YTO latch 2, while controlling the stimulus.

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| `ERR 830 YTO INTEGRATOR` | The YTO loop integrator operation does not meet the test limits. |

The following checklist is provided to help isolate a failure with the YTO integrator.

- ❑ Check the YTO LOOP INTEGRATOR block of the RF board assembly.
- ❑ Check the YTO PHASE/FREQUENCY DETECTOR block of the RF board assembly.
- ❑ Check the IF POLARITY SWITCH block of the RF board assembly.
- ❑ Check the YTO DIVIDE SELECTOR block of the RF board assembly.
- ❑ Check the YTO LOOP DIGITAL INTERFACE block of the RF board assembly.
- ❑ Check the **PLL3 OUTPUT** DIVIDER block of the RF board assembly.
- ❑ Check the circuits or control signals that affect the **D_YTO_ERR** signal path from the RF board assembly **YTO** LOOP INTEGRATOR block to the controller board assembly ADC.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| `TEST #23 YTO DIV` | This function monitors the internal value of the divider number of the YTO. |
| `TEST #24 YTO IF` | This function monitors the internal value of the IF frequency of the YTO. |

# 26. ALC Preamplifier

The ALC input selector switch is set to the calibrate mode. This setting selects and applies ground through the **MUXes** to the ALC preamplifier. The offset voltage is measured and compared to the expected value.

## If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| `ERR 831 ALC PREAMP` | The ALC preamplifier circuit operation does not meet the test limits |

The following checklist is provided to help isolate a failure with the ALC preamplifier.

- ❑ Check the ALC PREAMPLIFIER block on the RF board assembly.
- ❑ Check the ALC INPUT SELECTOR SWITCH block on the RF board assembly.
- ❑ Check the YTO LOOP DIGITAL INTERFACE block on the RF board assembly.
- ❑ Check the ALC DIGITAL INTERFACE block on the RF board assembly.

## Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| `TEST #25 ADC VALUE` | This function monitors individual signals from the MUX through the ADC. (MUX signal `#30, D,ALC,PREAMP.`) |

## 26.ALC Level DACS (coarse)

This is a monotonicity and range test of the ALC level DACs used for coarse tuning. It tests one half of the dual 8-bit DAC, the A half.

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 832 ALC COARSE DAC | The ALC coarse level DAC operation does not meet the test limits. |

The following checklist is provided to help isolate a failure with the ALC coarse level DAC.

- Check the ALC LEVEL DACS block on the RF board assembly.
- Check the YTO LOOP DIGITAL INTERFACE block on the RF board assembly.
- Check the ALC DIGITAL INTERFACE block on the RF board assembly.
- Check the power supplies to the RF board assembly.
- Check the circuits or control signals that affect the D_ALC_LVL_C signal path from the ALC LEVEL DACS block to the ADC.
- Check that W1 (the digital address and data bus cable) is not defective.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST #12 ALC COARSE | This function monitors and can set the value of the ALC coarse DAC. |
| TEST #25 ADC VALUE | This function monitors individual signals from the MUX through the ADC. (MUX signal #34, D_ALC_LVL_C.) |

# 27. ALC Level DACS (fine)

This is a monotonicity and range test of the ALC level DACs used for fine tuning. It tests one half of the dual S-bit DAC, the B half.

## If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 833 ALC FINE DAC | The ALC fme level DAC operation does not meet the test limits |

The following checklist is provided to help isolate a failure with the ALC fine level DAC.

- Check the ALC LEVEL DACS block on the RF board assembly.
- Check the power supplies to the RF board assembly.
- Check the circuits or control signals that affect the D_ALC_LVL_F signal path from the ALC LEVEL DACS block to the ADC.
- Check that W1 (the digital address and data bus cable) is not defective.

## Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and [ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST #13 ALC FINE | This function monitors and can set the value of the ALC fine DAC. |
| TEST #25 ADC VALUE | This function monitors individual signals from the MUX through the ADC. (MUX signal #35, D_ALC_LVL_F.) |

## 28. ALC Slope DACS

Only the B half of a dual DAC is tested by this routine. Testing the A half requires external stimulus **To** test the B half of the DAC, the A half is set to 0, the ALC-DVR-SEL switch is opened, and the SWEEP+TUNE OFFSET coarse DAC is set to its maximum setting. This eliminates offsets that might be put on the DAC's output and sets the DAC's (Vref in) voltage reference input to + 10 **V.** A monotonicity and range test are performed on the B half of the DAC.

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| `ERR 834 ALC SLOPE DAC` | The ALC slope DAC operation does not meet the test limits |

The following checklist is provided to help isolate a failure with the ALC slope DAC.

- Check the ALC RAMP DACS block on the RF board assembly.
- Check the ALC DIGITAL INTERFACE block on the RF board assembly.
- Check the power supplies to the RF board assembly.
- Check the circuits or control signals that affect the **D_ALC_RAMP** signal path from the ALC RAMP DACS block to the ADC.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| `ADJ #7 SLOPE LO BAND` | This function monitors and can set the low-band slope correction. |
| `ADJ #9 SLOPE HI BAND` | This function monitors and can set the high-band slope correction. |

## 29. YTO Leveling

The tracking source is put in the CW mode and the YTO leveling voltage is measured. The CW frequency will be set to two different points: 2.501 GHz, then 6.46 GHZ. A steady dc voltage is expected at each frequency.

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 835 YTO LEVELING | The YTO level voltage does not meet the test limit. |

The following checklist is provided to help isolate a failure with YTO leveling.

- ❑ Check the YTO LEVELING block on the RF board assembly
- ❑ Check the A4 YTO microcircuit assembly.
- ❑ Check the A9 Modulation Amplifier microcircuit assembly (HP 85645A only).
- ❑ Check the A9 Modulation Switch microcircuit assembly (HP 85644A only).
- •I Check the circuits or control signals that affect the D_YTO_LVL signal path from the RF board assembly YTO LEVELING block to the ADC.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions

| | |
|---|---|
| TEST #25 ADC VALUE | This function monitors individual signals from the MUX through the ADC. (MUX signal #37, D_YTO_LVL.) |

## 30. ALC Loop Integrator

The tracking source's ALC is closed and a measurement is made to check for a leveled condition. Two tests will be performed, one in low band and one in high band. The error message indicates one of three possible failures, either low band failed, high band failed, or both failed.

### If the test fails

The following error messages may be displayed on the tracking source:

| | |
|---|---|
| `ERR 836 ALC LOOP LO BAND` | The ALC loop integrator operation in low band does not meet the test limits. |
| `ERR 837 ALC LOOP HI BAND` | The ALC loop integrator operation in high band does not meet the test limits. |

The following checklist is provided to help isolate a failure with the ALC loop integrator.

**If the low-band operation has failed:**

- ❑ Check the ALC LOOP INTEGRATOR block on the RF board assembly.
- ❑ Check the ALC LOG AMPLIFIER block on the RF board assembly.
- ❑ Check the ALC ABSOLUTE VALUE AMPLIFIER block on the RF board assembly.
- ❑ Check the ALC PREAMPLIFIER block on the RF board assembly.
- ❑ Check the ALC INPUT SELECTOR SWITCH block on the RF board assembly.
- ❑ Check the LOW BAND MODULATOR DRIVER block on the RF board assembly.
- ❑ Check the BAND SWITCH DRIVER block on the RF board assembly.
- ❑ Check the ALC DIGITAL INTERFACE block on the RF board assembly.
- ❑ Check the LOW BAND microcircuit A15 block on the RF board assembly.
- ❑ Check the A9 Modulation Amplifier microcircuit assembly. (HP 85645A only.)
- ❑ Check the A9 Modulation Switch microcircuit assembly. (HP 85644A only.)

**If the high-band operation has failed:**

- Check the ALC LOOP INTEGRATOR block on the RF board assembly.
- Check the ALC LOG AMPLIFIER block on the RF board assembly.
- Check the ALC ABSOLUTE VALUE AMPLIFIER block on the RF board assembly.
- Check the ALC PREAMPLIFIER block on the RF board assembly.
- Check the ALC INPUT SELECTOR SWITCH block on the RF board assembly.
- Check the HIGH BAND MODULATOR DRIVER block on the RF board assembly.
- Check the BAND SWITCH DRIVER block on the RF board assembly.
- Check the ALC DIGITAL INTERFACE block on the RF board assembly.
- Check the **A9** Modulation Amplifier microcircuit assembly. (HP **85645A** only.)
- Check the **A9** Modulation Switch microcircuit assembly. (HP 856448 only.)

**If both low-band and high-band operations have failed:**

- Check all of the function blocks on the RF board that are indicated above for both the low- and high-band operations.
- Check the **A9** microcircuit assembly.
- Check the **A4** YTO microcircuit assembly.

## Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST **#25** ADC VALUE | This function monitors individual signals from the MUX through the ADC. |
| TEST **#26** SYTM VALUE | This function monitors SYTM signals through the ADC. |

## 31. Sweep + Tune Buffers (HP 85645A only)

The test sets the sweep + tune coarse DAC to its lower and upper limits and measures the voltage from the sweep + tune buffers.

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 838 SUP T BUFFER | The sweep + tune buffer operation does not meet the test limits. |

The following checklist is provided to help isolate a failure with the sweep + tune buffer.

- Check the SWP & T **BUFFERS** block on the controller board assembly.
- Check the circuits or control signals that affect the RAMP-DIAG signal from the controller board SWP & T BUFFERS block to the ADC.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST **#7 S+T** OFFST C | This function monitors and can set the sweep + tune offset coarse DAC. |
| TEST **#26** SYTM VALUE | This function monitors SYTM signals through the ADC. (MUX signal **#7,** RAMP,DIAG.) |

# 32. YTM Gain (HP 85645A only)

This is a range check of the 12 bit **YTM** gain DAC. The MAIN RAMP is used as the reference to the DAC. The ramp is set close to + 10 **V.**

## If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 839 YTM GAIN DAC | The **YTM** gain DAC operation does not meet the test limits. |

The following checklist is provided to help isolate a failure with the **YTM** gain DAC.

- Check the **YTF** GAIN block on the controller board assembly.
- Check the CONTROL BUS BUFFERS block on the controller board assembly.
- Check the circuits or control signals that affect the **YTF_DIAG1** signal from the controller board **YTF** GAIN block up to the ADC.

## Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| ADJ **#13** YTM GAIN | This function provides access to the **YTM** gain DAC. |
| TEST **#26** SYTM VALUE | This function monitors **SYTM** signals through the ADC. (MUX signal Xl, YTF,DIAGI.) |

## 33. YTM Breakpoint 3 (HP 85645A only)

This is a range and monotonicity check of the YTM breakpoint 3 DAC. This is an B-bit DAC. The reference to the DAC is set to -4 V by setting the MAIN RAMP to + 10 V.

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 840 YTM **BP3** DAC | The YTM breakpoint 3 DAC operation does not meet the test limit. |

The following checklist is provided to help isolate a failure with the YTM breakpoint 3 DAC.

- Check the YTF GAIN block on the controller board assembly
- I Check the circuits or control signals that affect the **YTF_DIAG4** signal from the controller board YTF GAIN block to the ADC.

### Related tests and adjustments

Test and adjustment functions are found under the extended [TEST] and [ADJUST] key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| ADJ **#17** YTM **BP3** | This function provides access to the YTM breakpoint 3 DAC. |
| TEST **#26** SYTM VALUE | This function monitors SYTM signals through the ADC. (MUX signal **#4, YTF_DIAG4.**) |

# 34. YTM Breakpoint 4 Frequency (HP 85645A only)

This is a range and monotonicity check of the YTM breakpoint 4 frequency DAC. This is an 8-bit DAC. The reference to the DAC is set to -5 V by setting the MAIN RAMP to + 10 V and the breakpoint 4 DAC to its maximum value.

## If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 841 YTM BP4 FREQ DAC | The YTM breakpoint 4 frequency DAC operation does not meet the test limit. |

The following checklist is provided to help isolate a failure with the YTM breakpoint 4, frequency DAC.

- Check the YTF BREAKPOINT 4 block on the controller board assembly.
- Check the circuits or control signals that affect the YTF_DIAG signal being tested, from the controller board YTF BREAKPOINT 4 block to the ADC.

## Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| ADJ #19 YTM BP4 FRQ | This function provides access to the YTM breakpoint 4 frequency DAC. |
| TEST #26 SYTM VALUE | This function monitors SYTM signals through the ADC. (MUX signal #5, YTF_DIAG5.) |

## 36. YTM Breakpoint 4 DAC (HP 85645A only)

This is a range and monotonicity check of the YTM breakpoint 4 frequency DAC. This is an **8-bit** DAC. The reference to the DAC is set to -5 V by setting the MAIN RAMP to + 10 V and the breakpoint 4 frequency DAC to its maximum value.

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 842 YTM **BP4** DAC | The YTM breakpoint 4 DAC operation does not meet the test limit. |

The following checklist is provided to help isolate a failure with the YTM breakpoint 4 DAC.

- Check the YTF' BREAKPOINT 4 block on the controller board assembly.
- Check the circuits or control signals that affect the **YTF_DIAG5** signal from the controller board YTF' BREAKPOINT 4 block to the ADC.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| ADJ **#18** YTM **BP4** | This function provides access to the YTM breakpoint 4 DAC. |
| TEST **#26** SYTM VALUE | This function monitors SYTM signals through the ADC. (MUX signal **#5, YTF_DIAG5.**) |

# 36. YTM Offset (HP 85645A only)

This is a range and monotonicity check of the YTM offset DAC. This is an 8-bit DAC.

## If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 843 YTM OFFSET DAC | The YTM offset DAC operation does not meet the test limit. |

The following checklist is provided to help isolate a failure with the YTM offset DAC.

- Check the YTF OFFSET block on the controller board assembly.
- Check the TTL TO CMOS block on the controller board assembly.
- Check the circuits or control signals that affect the YTF_DIAG6 signal from the controller board YTF OFFSET block up to the ADC.

## Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| ADJ #14 YTM OFFSET | This function provides access to the YTM offset DAC. |
| TEST #26 SYTM VALUE | This function monitors SYTM signals through the ADC. (MUX signal #6, YTF_DIAG6.) |

## 37. YTM Breakpoint 1

This is a range and monotonicity check of the YTM breakpoint 1 DAC. The sweep + tune offset (coarse) DAC is set to its maximum value, which sets **NEG_RAMP** to -10 V. The YTM breakpoint 1 DAC is then tested.

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 844 YTM **BP1** DAC | The YTM breakpoint 1 DAC does not meet the test limit. |

The following checklist is provided to help isolate a failure with the YTM breakpoint 1 DAC.

- Check the YTF' BREAKPOINT 1 block on the controller board assembly.
- Check the **TTL** TO CMOS block on the controller board assembly.
- Check the circuits or control signals that affect the **YTF_DIAG2** signal from the controller board YTF' BREAKPOINT 1 block up to the ADC.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions

| | |
|---|---|
| ADJ **#15** YTM **BP1** | This function provides access to the YTM breakpoint 1 DAC. |
| TEST **#26** SYTM VALUE | This function monitors SYTM signals through the ADC. (MUX signal **#2, YTF_DIAG2.**) |

# 38. YTM Breakpoint 2 (HP 85645A only)

This is a range and monotonicity check of the YTM breakpoint 2 DAC. The sweep + tune offset DAC is set to its maximum value, which sets NEG-RAMP to -10 V. The YTM breakpoint 2 DAC is then tested.

## If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 845 YTM **BP2** DAC | The YTM breakpoint 2 DAC operation does not meet the test limit. |

The following checklist is provided to help isolate a failure with the YTM breakpoint 2 DAC.

- Check the YTF BREAKPOINT 2 block on the controller board assembly.
- Check the **TTL** TO CMOS block on the controller board assembly.
- Check the circuits or control signals that affect the **YTF_DIAG3** signal from the controller board YTF BREAKPOINT 2 block to the ADC.

## Related tests and adjustments

Test and adjustment functions are found under the extended (TEST_) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| ADJ **#16** YTM **BP2** | This function provides access to the **YTM** breakpoint 2 DAC. |
| TEST **#26** SYTM VALUE | This function monitors SYTM signals through the ADC. (MUX signal **#3, YTF_DIAG3.**) |

## 39. YTM Drive (HP 85645A only)

The YTM drive block is tested by setting the tracking source to 15 GHz in CW mode. Then the sweep + tune offset (coarse) DAC, the YTM gain DAC, and the YTM breakpoint 1 DAC are set to their maximum values. The ADC is read after each setting.

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 846 YTM DRIVE | The YTM drive circuit operation does not meet the test limits. |

The following checklist is provided to help isolate a failure with the YTM drive.

- Check the YTF' DRIVE block of the controller board assembly.
- Check the YTF ADJUST block of the controller board assembly.
- Check the circuits or control signals that affect the YTF_DIAG7 signal from the YTF' DRIVE block to the ADC.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST] and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST #26 SYTM VALUE | This function monitors SYTM signals through the ADC. (MUX signal #0, YTF_DIAG7.) |

# 40. Bias Band Offset (HP 85645A only)

**Two DACs** are controlled in this test to insure that the voltage stays within the ADC range. These are **8-bit DACs.**

## If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 847 BIAS BAND OFFSET | The bias band offset DAC operation does not meet the test limits. |

The following checklist is provided to help isolate a failure with the bias band offset DAC.

- Check the BIAS BAND **OFFSET** block of the controller board assembly.
- Check the circuits or control signals that affect the signal being tested, from the BIAS BAND **OFFSET** block up to the ADC.

## Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions

| | |
|---|---|
| ADJ **#25** YTM BIAS BN | This function provides access to the **YTM** bias band offset DAC. |
| TEST **#26** SYTM VALUE | This function monitors **SYTM** signals through the ADC. (MUX signal **#10, BIAS_DIAG1.**) |

## 41. Bias Offset (HP 85645A only)

A range and monotonicity check are performed on the 8-bit bias offset DAC.

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 848 BIAS OFFSET DAC | The bias offset DAC operation does not meet the test limit. |

The following checklist is provided to help isolate a failure with the bias offset DAC.

- Check the BIAS OFFSET block of the controller board assembly.
- Check the circuits or control signals that affect the signal being tested, from the BIAS OFFSET block up to the ADC.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| ADJ #22 YTM BIAS OFS | This function provides access to the YTM bias offset DAC. |
| TEST #26 SYTM VALUE | This function monitors SYTM signals through the ADC. (MUX signal #20, BIAS_DIAG6.) |

# 42. Bias Gain (HP 85645A only)

A range and monotonicity check are performed on the 8-bit bias gain DAC.

## If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 849 BIAS GAIN DAC | The bias gain DAC operation does not meet the test limit. |

The following checklist is provided to help isolate a failure with the bias gain DAC.

- Check the BIAS GAIN block of the controller board assembly.
- Check the circuits or control signals that affect the signal being tested, from the BIAS GAIN block up to the ADC.

## Related tests and adjustments

Test and adjustment functions are found under the extended [TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| ADJ #23 YTM BIAS GAIN | This function provides access to the YTM bias gain DAC. |
| TEST #26 SYTM VALUE | This function monitors SYTM signals through the ADC. (MUX signal #10, BIAS_DIAG1.) |

## 43. Power Level Adjustment (HP 85645A only)

The tracking source is set to a 0 dBm output power at 19 GHz. An ADC reading is taken and compared to the expected value. Then a range and monotonicity check is performed on the 8-bit power level DAC.

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| `ERR 850 PWR LEVEL DAC` | The power level DAC operation does not meet the test limit. |

The following checklist is provided to help isolate a failure with the power level DAC.

- Check the POWER LEVEL ADJ block of the controller board assembly.
- Check the circuits or control signals that affect the signal being tested, from the POWER LEVEL ADJ block up to the ADC.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST_) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| `ADJ #21 YTM BIAS PWR LVL` | This function provides access to the YTM bias power level DAC. |
| `TEST #26 SYTM VALUE` | This function monitors SYTM signals through the ADC. (MUX signal #14, BIAS_DIAG5.) |

# 44. SYTM Bias (HP 85645A only)

A range and monotonicity check is performed on the 8-bit SYTM bias DAC.

## If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 851 *SYTM* BIAS DAC | The SYTM bias DAC operation does not meet the test limit. |

The following checklist is provided to help isolate a failure with the SYTM bias DAC.

- Check the DAC or the associated circuits in the SYTM BIAS block on the controller board assembly.
- Check the circuits or control signals that affect BIAS_DIAG3 signal being tested, from the SYTM BIAS block up to the ADC.

## Related tests and adjustments

Test and adjustment functions are found under the extended [TEST) and [ADJUST] key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| ADJ #24 YTM BIAS | This function provides access to the YTM bias DAC. |
| TEST #26 SYTM VALUE | This function monitors SYTM signals through the ADC. (MUX signal #12, BIAS_DIAG3.) |

## 46. Leveling Amplifier Driver Sense 1

A range check is performed on the A half of the 8-bit leveling amplifier DAC.

### If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 852 LEVEL AMP DAC | The leveling amplifier driver DAC operation does not meet the test limits. |

The following checklist is provided to help isolate a failure with the first half of the leveling amplifier DAC.

- Check the dual DAC or associated circuits in the LEVELING AMPLIFIER DRIVERS block on the controller board assembly
- Check the circuits or control signals that affect LVL-AMP-DACS signal being tested, from the controller board LEVELING AMPLIFIER DRIVERS block to the ADC.

### Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| ADJ #5 LEVEL AMP 1 | This function provides access to the DAC for the first leveling amplifier. |
| TEST #26 SYTM VALUE | This function monitors SYTM signals through the ADC. (MUX signal #25, LVL,AMP,DACS.) |

# 46. Leveling Amplifier Driver Sense 2

A range check is performed on the B half of the leveling amplifier driver DAC.

## If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 852 LEVEL AMP DAC | The leveling amplifier driver DAC operation does not meet the test limits |

The following checklist is provided to help isolate a failure with second half of the leveling amplifier DAC.

- Check the dual DAC or associated circuits in the LEVELING AMPLIFIER DRIVERS block on the controller board assembly.
- Check the circuits or control signals that affect **LVL_AMP_DACS** signal being tested, from the controller board LEVELING AMPLIFIER DRIVERS block to the ADC.

## Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and [ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| ADJ #6 LEVEL AMP 2 | This function provides access to the DAC for the second leveling amplifier. |
| TEST #26 SYTM VALUE | This function monitors SYTM signals through the ADC. (MUX signal #25 LVL,AMP,DACS.) |

## 47. 260 MHz Oscillator Low-Band Test

The tracking source is set to CW mode with a CW frequency of 300 MHz, and a power level of 0 **dBm.** The 260 MHz lock input to the ADC is measured and compared to the expected value.

### If the test fails

The following error message may be displayed on the tracking source:

`ERR 853 260 MHz OSC` — The 260 MHz oscillator in the low-band microcircuit does not meet the test limit.

The following checklist is provided to help isolate a failure with the 260 MHz oscillator from the low-band assembly.

- Check the **A3** Low-Band microcircuit assembly.
- Check the **W5** cable harness.
- Check the circuits or control signals that affect 260 MHz LOCK signal being tested, from the **A3** Low-Band microcircuit to the ADC.

### Related tests and adjustments

Test and adjustment functions are found under the extended I-TEST) and (ADJUST) key menus, They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

`TEST #26 SYTM VALUE` — This function monitors SYTM signals through the ADC. (MUX signal **#16, 260MHZ_LOCK.**)

# 48. 4.2 GHz Oscillator Low-Band Test

The tracking source is set to CW mode with a CW frequency of 300 MHz and a power level of 0 dBm. The 4.2 GHz lock signal is measured by the ADC and compared to the expected value.

## If the test fails

The following error message may be displayed on the tracking source:

| | |
|---|---|
| ERR 854 4.2 GHz OSC | The 4.2 GHz oscillator in the low-band microcircuit does not meet the test limit. |

The following checklist is provided to help isolate a failure with the 4.2 GHz oscillator from the low-band assembly.

- Check the A3 Low-Band microcircuit assembly.
- Check the W5 cable harness.
- Check the circuits or control signals that affect 4.2GHz LOCK signal being tested, from the Low-Band microcircuit to the ADC.

## Related tests and adjustments

Test and adjustment functions are found under the extended (TEST) and (ADJUST) key menus. They can be used to correct or help troubleshoot a failure. Refer to chapters 4 and 5 for more information about these functions.

| | |
|---|---|
| TEST #26 SYTM VALUE | This function monitors SYTM signals through the ADC. (MUX signal #17, 4.2GHZ_LOCK.) |

# 3

# General Troubleshooting

This chapter contains the following sections of information:

- Troubleshooting process summary.
- Troubleshooting procedures that help you use the instrument's features to troubleshoot the tracking source.
- Tracking source operation and theory information that can assist in troubleshooting the instrument.
- **Major** Assembly troubleshooting information and explanations of how different parts of the instrument operate.

If a problem occurs, there are several techniques available to help you determine the general location of the problem:

- Use the block diagram to help you isolate the problem. Refer to the information on the block diagram and observe instrument operation.
- Follow the troubleshooting procedures to exercise the main internal functions. These include verifying the operation of the following:
  - ❑ The low band and high band signal path operation.
  - ❑ The main locking loop.
  - ❑ The discriminator.
  - 0 The leveling loop.
  - ❑ The digital control circuitry.
- Refer to the circuit descriptions for the major assemblies at the end of this chapter.

## Troubleshooting Process Summary

The information below is a summary of the detailed troubleshooting that follows:

1. Check the front-panel status indicator LEDs.
2. Check the power supply operation.
3. Perform the instrument's self-diagnostics test (if available).
4. Set the instrument to CW mode. Check the RF output frequency and amplitude.
   a. Set the CW frequency to a value that will verify low-band operation, and check the ALC by switching through the attenuator and vernier ranges.
   b. Set the CW frequency to a value that will verify high-band operation, and check for proper signal levels.
5. Place the instrument in tracking mode with zero offset. Check the RF output frequency and amplitude.
   a. Set the frequency to zero span and to a value within low-band operation to check the lock loop and discriminator.
   b. Set the frequency to zero span and to a value within high-band operation to check the lock loop and discriminator.
   c. Set the tracking source to a frequency value within low-band range. Check the signal tracking operation.
   d. Set the tracking source to a frequency value within high-band range. Check the signal tracking operation.
   e. For the HP 85645A tracking source, check multiband and A6 SYTM operations.

## Troubleshooting the Tracking Source

The items listed below may be used to help you determine whether the basic functions of the tracking source are working.

### Check Basic Operation

lb check the status indicators and power supply settings, refer to the following list:

- ❑ Check that the LINE power status indicator is lit.
- ❑ Check other front-panel status indicator LED's.
- ❑ Check the condition of the instrument's fuse. The fuse is located on the rear panel.
- ❑ Check the position of the line-voltage selector switch. The switch is located on the rear panel.
- •I Check that the instrument fan is operating.
- ❑ Check the ac-source line power.
- ❑ Check for error messages displayed in the 32-character display windows. For error message information, refer to the ***HP 85644A and HP 85645A Tracking Source User's Guide.***

■ If none of the status indicator LEDs are working, there is a power problem. Remove the instrument cover and refer to the following list:

- ❑ Check for a power supply problem or for a short in the instrument.
- ❑ Check whether the power supply has shut down due to excessive current or temperature levels.
- ❑ Refer to "A16 Power Supply Circuitry" in this chapter for specific information.

■ If *some* of the status indicator LEDs are functioning, but not all of them, refer to the following list:

- ❑ Check the status indicator LEDs. There may be a problem with the LEDs themselves
- ❑ Check for proper voltage levels to the LEDs of the power supplies. Refer to "A16 Power Supply Circuitry" for specific information.
- ❑ Check the operation of A3 Controller board. Refer to the A3 Controller board troubleshooting information in this chapter.
- ❑ Check the operation of Al Front Panel assembly and W1 cable assembly. Refer to "A3 Controller Board Troubleshooting Detail" for information about the 16 error LEDs.

■ If all of the status indicator LEDs are functioning correctly, refer to the following procedure:

- ❑ Execute the built-in self-test routine as explained in "Run the Tracking Source Self-Test Routine".

- Execute the procedure in "Checking Instrument Operation" that follows this section.

### Run the Tracking Source Self-Test Routine

You can troubleshoot the HP 85644A or HP 85645A tracking source with or without the built-in self-test routine.

The self-test routine is available on tracking sources with the firmware revision dated 910801 or later. The self-test routine provides a quick conildence check that can provide diagnostic error messages. A detailed description of the self-test routine, its error messages, and diagnostic information is provided in Chapter 2, "Self-Test Diagnostics." Run the self-test routine using the procedure below.

lb run the self-test routine, press the following tracking source keys:

1. Press [TEST).
2. Press (MENU DOWN).
3. Press (ENTER) to select and execute the self-test.

The self-test routine requires that the processor, the display, and some power supplies be operational before it can run. Once initiated, the routine runs until the first error is detected, then it stops. Use the "Checking Instrument Operation" procedure to obtain more diagnostic information without removing the instrument covers.

## Checking Instrument Operation

This troubleshooting process can be used to further diagnose a problem using normal instrument operation.

The process starts with operating modes that use the minimum amount of circuitry. Functionality can then be added gradually to verify the operation of additional parts of the instrument until the most complex operations are checked.

### Check instrument operation in CW mode

CW mode uses the least amount of circuitry in the instrument and can be used to check the signal path and the leveling loop. Refer to the following procedure:

1. Press (PRESET_) on the tracking source.
2. Press (CW). In this mode the signal path and ALC operation can be verified. Neither the lock loop nor the discriminator circuitry are being used in CW mode.
3. Check the RF output signal frequency and amplitude while you select and exercise different operating modes.

4. Set the CW frequency to a value less than 2.5 GHz to verify low band operation. This check verifies whether parts of the following assemblies are functioning properly:
   - A15 Low Band microcircuit
   - A4 YTO
   - A9 Mod Ampl
   - A5 Step Atten
   - A2 RF board
   - The low- and high-band switch

   The internal 10 MHz reference circuit (on the A2 RF board) is used unless an external reference is connected to rear panel J4.
5. While in low band, you can also check the 4.2 GHz signal and A4 YTO signal leakage. Check for signal leakage through the RF OUTPUT connector.
6. Check ALC operation by changing the step attenuator settings through its entire range. On the HP 85645A only, switch the attenuator between ac- and dc-coupled operation. Make sure the amplitude vernier can be varied through its entire range.
7. Check the external detector functionality.
8. Set the CW frequency to a value greater than 2.5 GHz but less than 6.0 GHz. This frequency setting can help verify both high-band operation and low- and high-band switch operation.

   A check of operation at high-band frequencies can verify portions of the following:
   - A4 YTO
   - A2 RF board
   - A7 Coupler (on the HP 85645A)
   - A8 Detector (on the HP 85644A)

## Check instrument operation in tracking mode

If the CW mode circuitry is functioning properly, the next level of operation complexity is tracking mode. Refer to the steps below:

1. Change from CW mode to tracking mode.
2. Set the offset frequency to zero offset.
3. Set the frequency span to zero span.
4. Verify that the host instrument has been selected.
5. Check the RF output with another spectrum analyzer while the tracking source signal is locked to the host spectrum analyzer signal. Verify that the output is present. Then verify that it is at the correct frequency and in the correct band.
6. Check the sweep ramp input.

7. Set the frequency to a value less than 2.0 GHz for low-band operation. This frequency setting verifies whether portions of the LO INPUT signal conditioning circuitry (AT1, A12, AT2, A13 and AT3) are functioning properly. Proper operation at this frequency setting verifies mixer operation in the A15 Low Band microcircuit. It also verifies the operation of the discriminator circuitry, which includes the A13 Leveling Ampl, A18 5 GHz LPF, and All Detector assemblies
8. Set the frequency to a value greater than 2.75 GHz, but less than 5.8 GHz and the span set to zero to check high band operation. These settings verify A14 Mixer and A19 1 GHz LPF operation.
9. Set the tracking source to tracking mode with zero offset frequency.
10. Set the frequency range for 3.0 GHz start frequency to the maximum frequency for the model being tested. These settings check the sweep capabilities of the A2 RF board. For the HP 85645A, these settings check the A6 SYTM and multi-band operation. Notice that the HP 85644A output power will appear to drop when the host instrument switches to band 2.

## Tracking Source Circuit Theory Summary

The HP 85644A and 85645A tracking sources provide an RF output signal. This output can be set either to CW mode, to track the frequency of a host instrument, or to offset track the host signal. The amplitude of the output can be set with either internal or external leveling, and it can be modulated by an external sweep ramp.

These frequency and amplitude functions can help you understand the various parts of the block diagram. Use this information to help isolate a failure to the correct assembly.

### Control and Communication Circuitry

The Al Front-Panel board, A3 Controller board, and A17 HPIB Interface board provide the means for controlling the remainder of the circuitry in the tracking source.

Al, A3, and A17 must be functional before normal instrument operation or the self-test routine can work.

### Power Supply Circuitry

The tracking source models each have a switching power supply (A16) that provides several output voltages. The power supply needs to have a proper load for stability. The power supply safety features are designed to shut it down if the temperature or current levels become excessive.

For additional information, refer to the section titled "A16 Power Supply Circuitry".

## Tracking Source Signal Path Descriptions

The signal paths of the HP 85644A and the HP 85645A are similar Both instruments have the same low band microcircuit assembly and 2.0 GHz to 7 GHz YIG-tuned oscillator. They both have a distribution amplifier (part of the A9 assembly). However, the HP 85644A tracking source has more features integrated into its A9 assembly than does the HP 85645A. In addition, the HP 85645A has an additional switched YIG-tuned multiplier (A6 SYTM) that provides frequencies up to 26.5 GHz.

### HP 85644A Tracking Source Signal Path

The HP 85644A tracking source signal path starts with an internal 2.0 GHz to 7 GHz oscillator (A4 YTO). This signal is sent to a distribution amplifier (part of the A9 MOD Switch assembly). The signal path then splits One path is the low-frequency band path, the other is the high-frequency band path.

The high frequency output signals are generated by the YTO. Output frequencies that are lower than the YTO frequency are obtained by down conversion in the A15 Low Band microcircuit assembly.

The low-band signal path uses a leveled output signal of 4.2 GHz to 7.1 GHz from the YTO through the A9 Mod Switch assembly. This signal is mixed in the A15 Low Band microcircuit with a CW 4.2 GHz signal. The resulting 0 to 2.9 GHz signal is low-pass filtered, amplified, and routed through a low-band detector in the A15 Low Band microcircuit assembly. The signal then goes to the band switch in A9.

After the switch assembly, the signal path are recombined. The high-band path is routed to the A5 Step Attenuator assembly.

The HP 85644A high-band signal path has an output amplifier in A9. The high- and low-band switch is also part of A9. The high-band coupler and detector follow the switch assembly and are also part of A9.

The output of the high-band coupler and detector is used by the ALC to measure and control high-band output power. The RF signal is routed from A9 to A5, a 70 dB step attenuator, then to the front-panel RF output.

### HP 85645A Tracking Source Signal Path

The HP 85645A signal path starts with an internal 2.0 GHz to 7 GHz oscillator (A4 YTO). This signal is sent to a distribution amplifier (part of the A9 MOD Switch assembly). The signal path then splits into a low-frequency band path and a high-frequency band path. The high frequency output signals are generated by the YTO and the multiplier.

Output frequencies below the YTO frequency are obtained by down conversion in the A15 Low Band microcircuit assembly.

The low-band signal path uses a leveled output signal of 4.2 GHz to 7.1 GHz from the YTO through A9. In the A15 Low Band microcircuit assembly, this signal is mixed with a 4.2 GHz signal to obtain 0 to 2.9 GHz. The 0 to 2.9 GHz signal then passes through a low-pass filter, an amplifier, and the low-band detector in A15. The signal then goes

to the band switch in the A6 SYTM assembly. After A6, the high- and low-band signal paths are recombined. The signal path continues to the A5 Step Attenuator assembly.

The HP 85645A high-band signal path has a high power output amplifier integrated in the A9 Mod Ampl assembly. An isolator (A10) provides a good match between A9 and the multiplier diode in A6.

The A6 SYTM assembly can multiply the 2.0 GHz to 7 GHz input by 1, 2, 3, or 4. The signal is also filtered to reduce the amplitude of unwanted harmonics

The high- and low-band switch is integrated into the A6 SYTM assembly. The A7 coupler follows the A6 SYTM. The coupled signal out of A7 provides a low level output to the high-band detector (A8). The output from the high-band detector is used by the ALC to measure and control high-band output power. The signal output of the A7 high-band coupler is routed through the ac or dc coupled A5 Step Atten assembly to the front-panel RF output.

## ALC (Amplitude Level Control) Circuitry

Amplitude control is accomplished by modulators, detectors, and parts of the A2 RF Board circuitry. These components comprise the "ALC system."

There are separate detectors for high- and low-band operation. The low-band detector is in the A15 Low Band microcircuit assembly. For the HP 85644A, the high-band detector is in the A9 Mod Switch assembly. For the HP 85645A, the high-band detector is in the A8 Detector assembly. Alternatively, an external detector can be selected rather than these detectors.

There are separate modulators for low band (in the A15 Low Band microcircuit assembly), and high band (in the A9 Mod Ampl assembly). Most of the ALC amplifier and drive circuits are on the A2 RF Board assembly and are shared by both low and high bands.

## Main Lock Loop Circuitry

Tracking and offset tracking operations use the main lock loop. CW mode signals do not use the main lock loop functionality. In tracking mode, the loop locks A4 YTO to the LO input signal from the tracking source's front panel LO INPUT connector. lb function properly, this lock loop requires that the YTO frequency be offset from the LO frequency by at least 30 MHz.

The 30 MHz minimum offset requirement is true for both tracking and offset tracking operations. The desired offset is computed from several pieces of information. The information includes the host instrument's first IF frequency and band settings as well as the tracking source's tracking-adjust and frequency-offset settings.

To track, or offset track, an LO input signal is required at front panel connector J2 (LO INPUT). The LO input signal is adjusted to the correct amplitude by AT1, A12, AT2, A13, and AT3. The signal is then mixed with the signal from the A4 YTO assembly. The resulting difference-frequency is routed through the A19 1 GHz

LPF assembly to the **A2** RF Board assembly lock-loop circuitry. On **A2,** the resulting difference-frequency is compared to a calculated, desired difference-frequency that is generated by the offset frequency synthesizer on **A2.**

An error voltage is obtained and used to adjust or lock the **A4** YTO with the desired offset frequency.

## Discriminator and Frequency Band Determination Circuitry

The discriminator circuitry includes the **A13** Leveling Ampl, **A18** 5 **GHz** LPF, and All Detector assemblies. The discriminator circuits are used for signal locking in tracking and offset tracking modes.

For tracking operation, the tracking source must determine the host instrument's current frequency band. The frequency band information is used to calculate the correct offset for the main lock loop and to select between low- and high-band paths The band information is also used to select the harmonic number for **A6** SYTM.

The current host instrument frequency band is determined by these factors:

- The microprocessor on the **A3** Controller board
- The output sweep + tune input signal (rear-panel **J5** connector)
- The output of the All Discriminator assembly

The discriminator determines whether the frequency of the LO input signal is in the lower or upper half of its range.

The discriminator detector provides a large output voltage if the LO input is below 5 **GHz,** and a small output voltage if the LO input is above 5 **GHz.** The discriminator output voltage along with the sweep + tune input frequency information (at rear-panel **J5)** are used to determine the current band of the host instrument.

The host instrument's sensitivity factor is a known value. As a result, when the sweep + tune input signal is measured by the ADC (on **A3),** the approximate host instrument frequency can be calculated.

The additional information obtained from the discriminator allows the microprocessor to correctly determine the currently selected host instrument frequency band. This is especially important when the frequency is near a band boundary. The microprocessor can differentiate whether the frequency is at the upper end of a band or the lower end of the next higher band.

# Major Assembly Troubleshooting and Circuit Theory Detail

The following detailed information is provided to aid in troubleshooting the tracking source. The section is divided into the following topics:

- A2 RF Board, Phase-Lock-Loop, YTO, and ALC Detail
- A3 Controller Board and Communication Detail, and Miscellaneous Circuit Detail
- Power Supply Detail

## A2 RF Board Troubleshooting Detail

The A2 RF board assembly troubleshooting information is divided into the following main functional groups. Refer to the schematic diagram as indicated in Figure 3-1:

- Signature analysis troubleshooting
- Frequency reference troubleshooting
- PLL1 troubleshooting
- PLL2 troubleshooting
- PLL3 troubleshooting
- YTO loop troubleshooting
- ALC troubleshooting

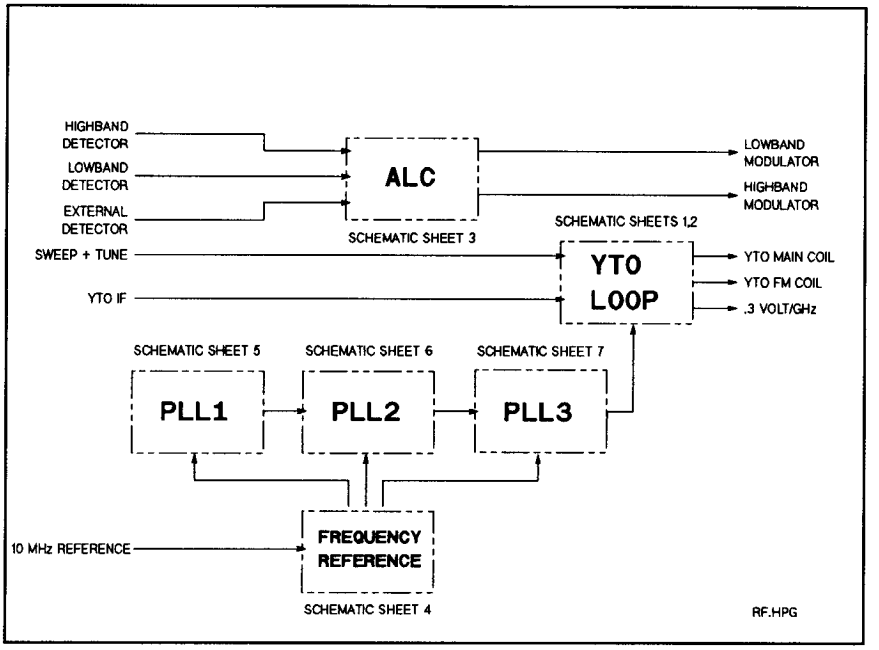



**Figure 3-1.**
**Tracking Source A2 RF Board Assembly and Related Circuits**

## Frequency Reference Operation

The frequency reference circuitry in the tracking source is diagramed in Figure 3-2.

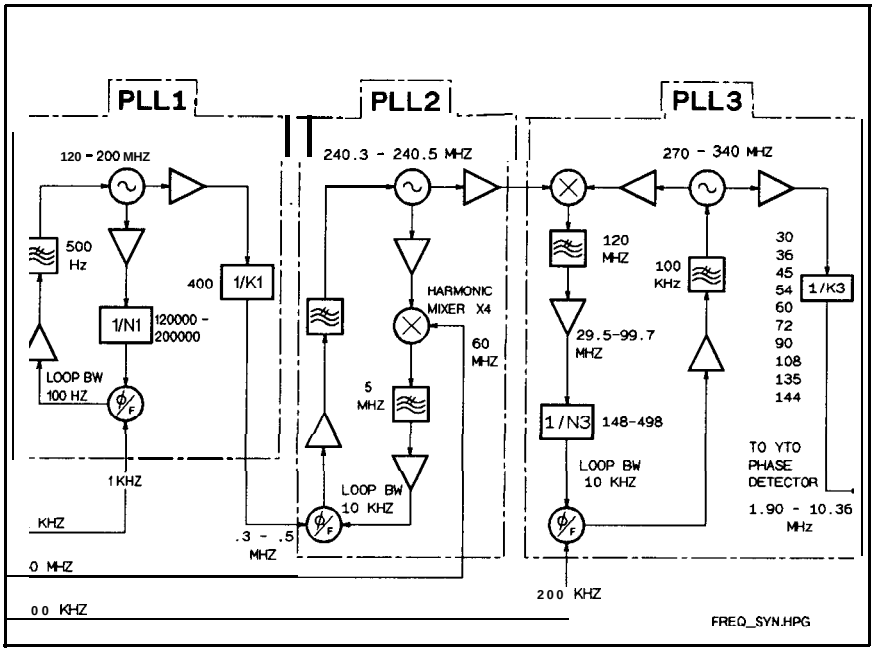



**Figure 3-2. Tracking Source Frequency Reference Circuitry**

The following plots indicate typical signals that are present at the major nodes in the frequency reference circuitry.

All measurements were made with an active probe with a 20 dB (10:1) attenuator attached. A spanner tip is recommended so that ground is always connected to a nearby shield trace.

The location of the major nodes is indicated in Figure 3-10.

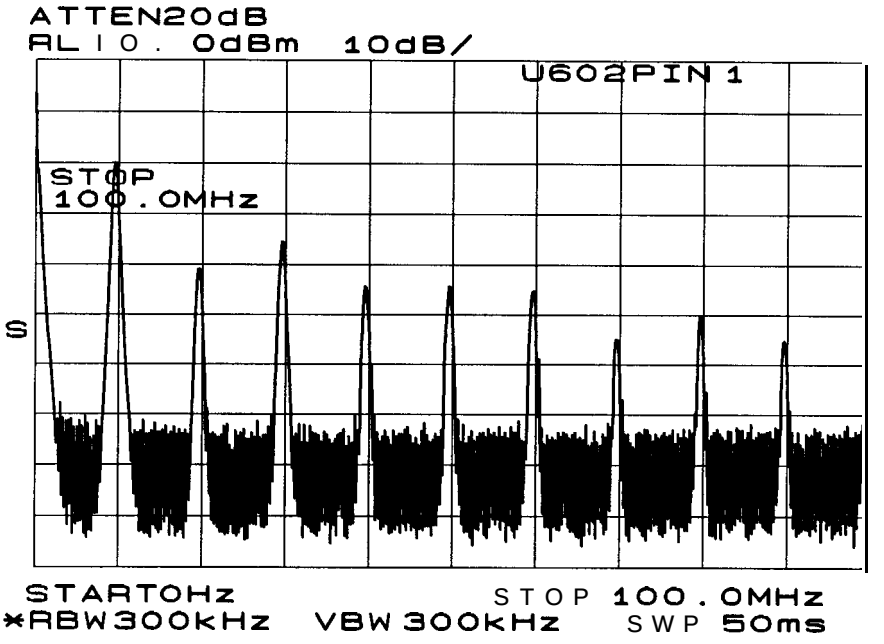



**Figure 3-3. Display of Signal at U602 Pin 1**

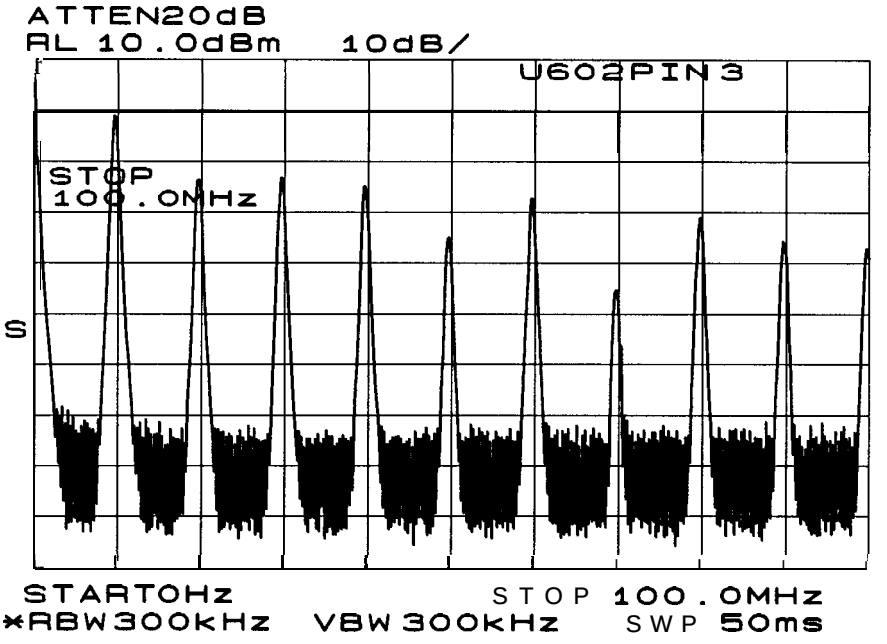



**Figure 3-4. Display of Signal at U602 Pin 3**

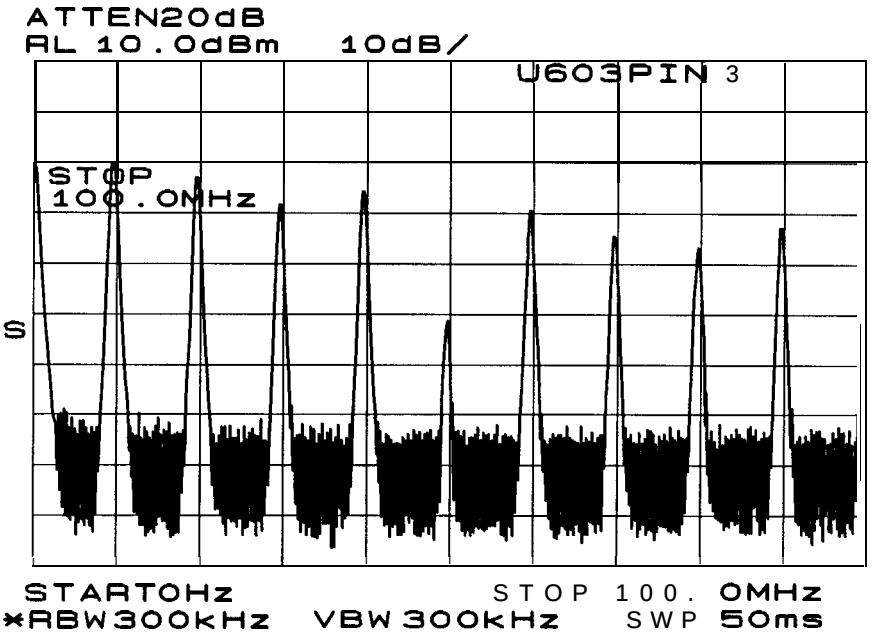



**Figure 3-5. Display of Signal at U603 Pin 3**

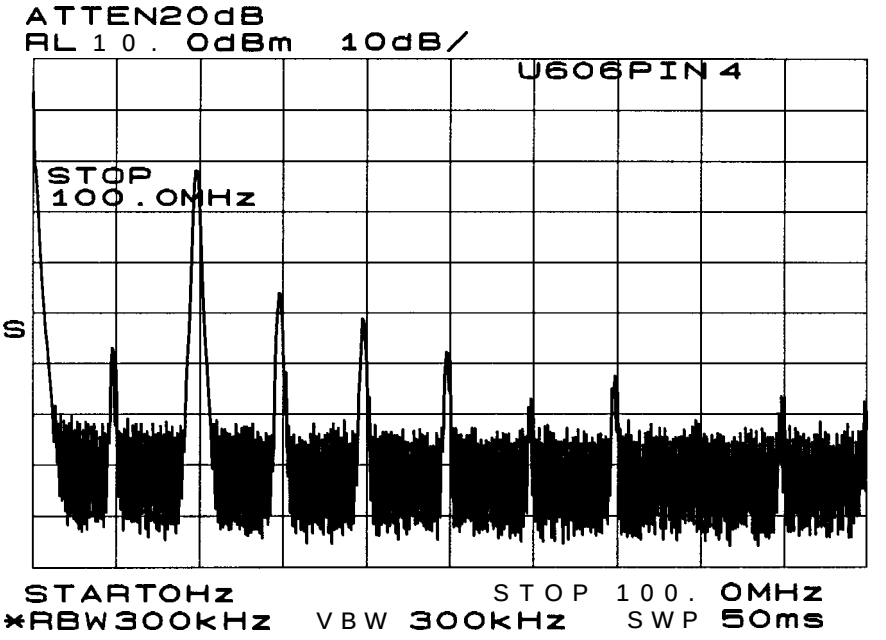



**Figure 3-6. Display of Signal at U606 Pin 4**

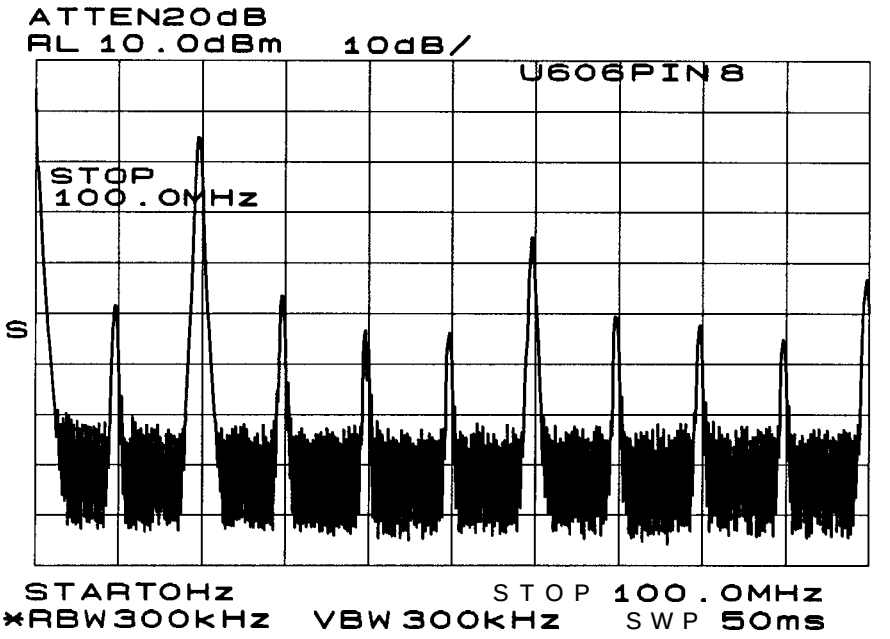



**Figure 3-7. Display of Signal at U606 Pin 8**

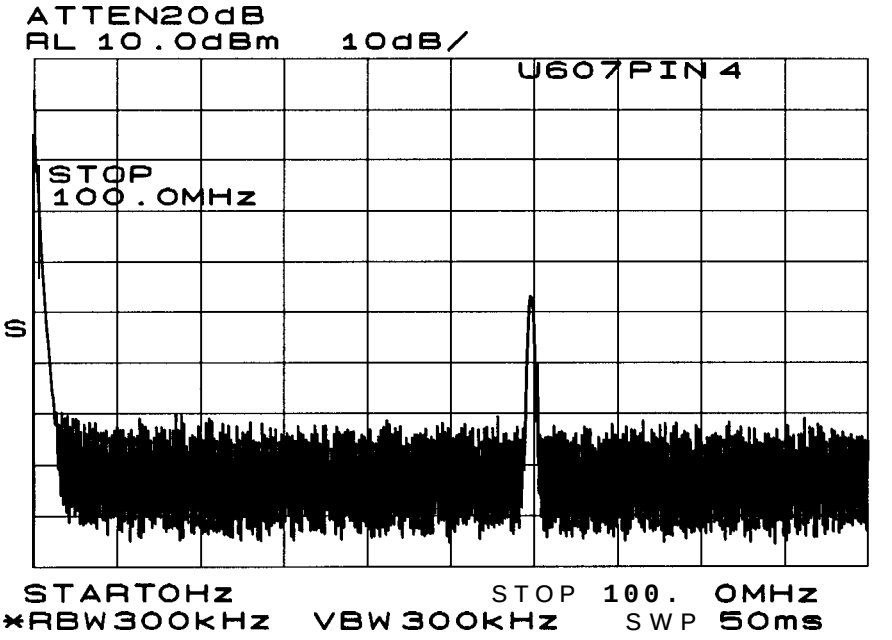



**Figure 3-8. Display of Signal at U607 Pin 4**

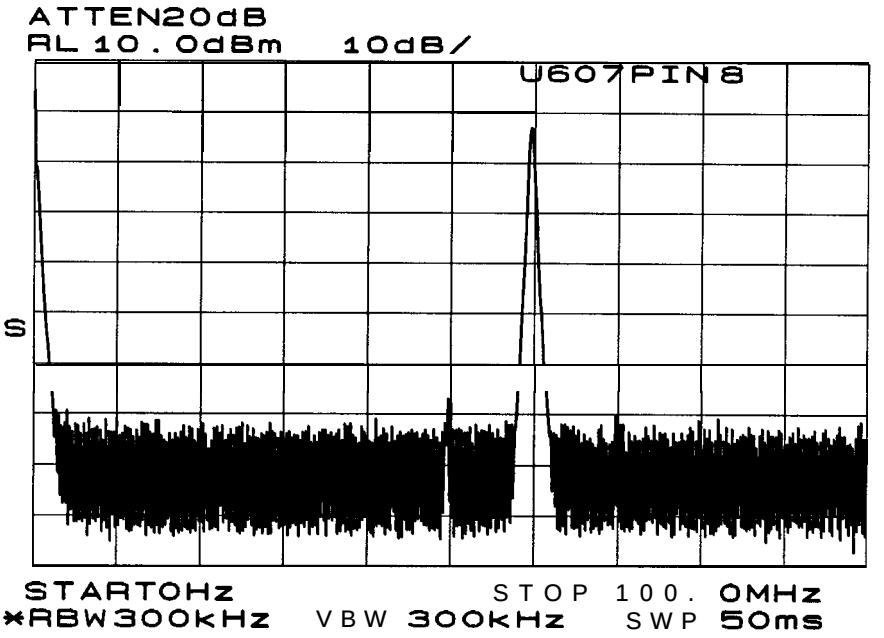



**Figure 3-9. Display of Signal at U607 Pin 8**

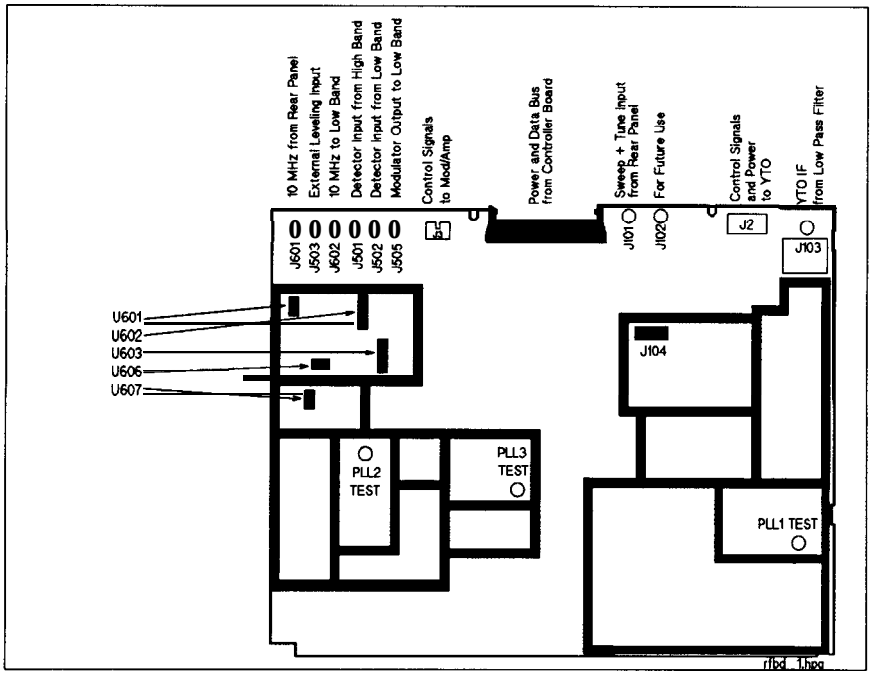



**Figure 3-10. A2 RF Board Assembly Node Location Detail**

## Frequency Synthesizer Operation

The frequency synthesizer is comprised of the tracking sources three phase-lock loops. Refer to Figure 3-11 for the block diagram of the three loops. Refer to Figure 3-10, Figure 3-12, and Figure 3-15 for the location of the phase-lock loop circuitry on the A2 RF board.

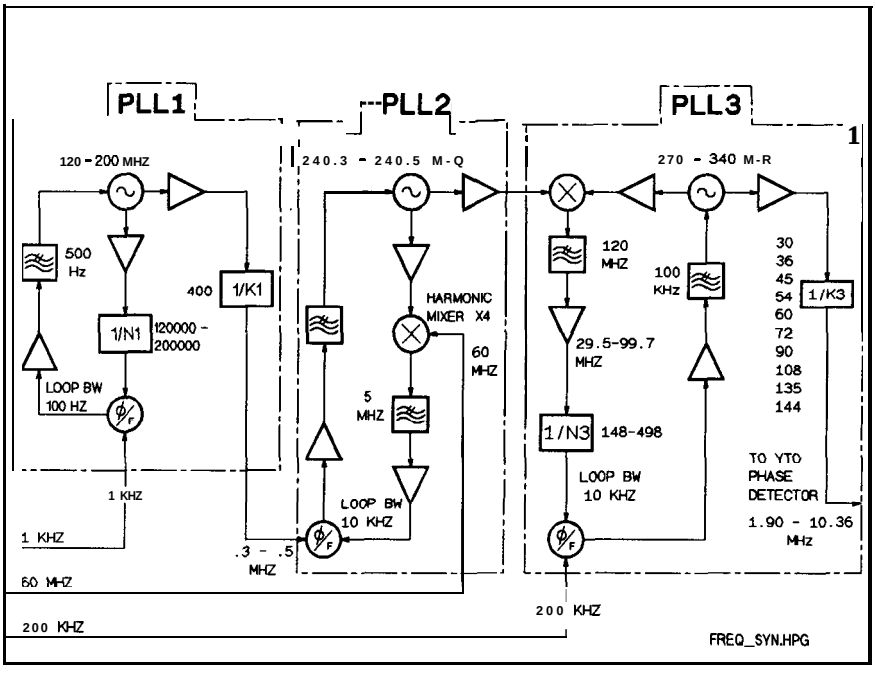



**Figure 3-1 1. Frequency Synthesizer Circuitry**

**PLL1 Troubleshooting.** The following values were derived by using an HP 8562A spectrum analyzer as the selected host instrument. The center frequency is set to 1 GHz with zero span. The tracking source is set to the tracking mode.

Move YTO test jumper 5103 to TEST position until you have finished making measurements. Return the jumper to normal operating position when finished.

**Table 3-1. PLL1 Troubleshooting Information**

| PLL1 Schematic Sheet 5 | Block | Test Point | Tracking Offset | |
|---|---|---|---|---|
| | | | 190.878 MHz | 190.697 MHz |
| PLL1 Frequency | RR | PLL1 TEST | 120.0 MHz<br>0 dBm | 199.7 MHz<br>0 dBm |
| PLL1 Oscillator | RR | U707 Pin 7 | 0 dBm | -3 dBm |
| PLL1 Oscillator | RR | U708 Pin 7 | +4 dBm | 0 dBm |
| PLL1 Oscillator | RR | U709 Pin 7 | +4 dBm | 0 dBm |
| PLL1 Loop Divider | TT | U715 Pins 3, 4, 5, 6 | TTL state<br>L-Low<br>L H L L | TTL State<br>H=High<br>L L H L |
| PLL1 Loop Divider | TT | U716 Pins 3, 4, 5, 6 | H L L L | L H L L |
| PLL1 Loop Divider | TT | U717 Pin 3, 4, 6, 6 | H L H H | H H L H |
| PLL1 Loop Divider | 'IT | U718 Pin 3, 4, 5, 6 | H L H H | H H L H |
| PLL1 Loop Divider | TT | U719 Pin 3, 4, 5, 6 | L L H H | L L L H |
| PLL1 Integrator | PP | U704 Pin 1 | -10 v | +5 V |
| PLL1 Loop Filter | QQ | U705 Pin 1<br>U705 Pin 7 | o v<br>+8.7 V | o v<br>-4.3 v |
| PLL1 Loop Filter | QQ | U706 Pin 1<br>U706 Pin 7 | o v<br>-9 V | o v<br>+4.4 v |
| Varactor Tune | RR | CR701 Anode | +1 v | +11 v |
| PLL1 Loop Divider<br>Pulses<br>Width<br>Spacing | TT | U713 Pin 9 | <br>Negative<br>80 ns<br>1.3$\mu$s | <br>Negative<br>50 ns<br>800 ns |
| PLL1 output Divider | u u | U710 Pin 7 | 12 MHz | 19.97 MHz |
| PLL1 output Divider | u u | U711 Pin 8 | 3 MHz | 4.99 MHz |
| PLL1 output Divider | u u | U712 Pin 3 | 300 kHz | 499 kHz |

The components identified in Table 3-1 are located as shown in Figure 3-12 below.

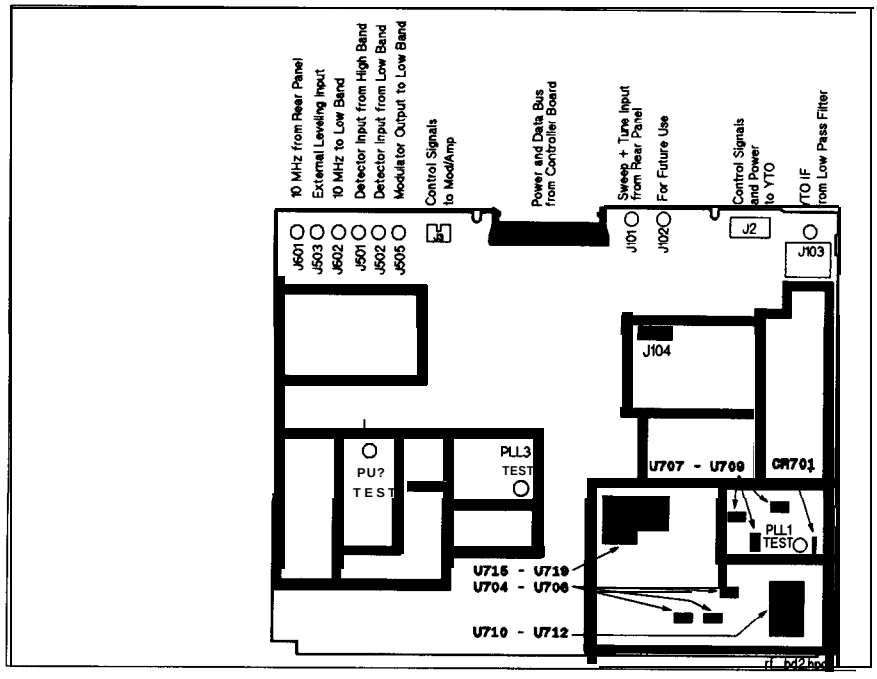



**Figure 3-12. Phase-Lock-Loop 2 Test Point Locations**

**PLL2 Troubleshooting.** The following values were derived by using an HP 8562A spectrum analyzer as the selected host instrument. The center frequency is set to 1 GHz with zero span. The tracking source is set to the tracking mode with a tracking offset of 190.878 MHz.

Move YTO test jumper 5103 to TEST position until you have finished making measurements. Return the jumper to normal operating position when finished.

**Table 3-2. PLL2 Troubleshooting Information**

| PLL2 Schematic Sheet 6 | Block | Test Point | Probe | Measured Value |
|---|---|---|---|---|
| PLL2 Frequency | XX | PLL2 TEST | 50Ω cable | 240.3 MHz<br>-16 dBm |
| PLL2 Oscillator | XX | U804 Pin 7 | Active probe | 0 dBm |
| PLL2 Oscillator | XX | U805 Pin 7 | Active probe | +4 dBm |
| PLL2 Oscillator | XX | U806 Pin 7 | Active probe | 0 dBm |
| PLL2 IF | YY | CR806 Anode | Active probe | Refer to Figure 3-13 |
| PLL2 IF | YY | U807 Pin 6 | Active probe | 300 kHz<br>-38 dBm |
| PLL2 IF | YY | U807 Pin 1 | Active probe | 300 kHz<br>+10 dBm |
| PLL2 IF | YY | U802 Pin 11 | Scope probe | 300 kHz TTL square wave |
| PLL2 Loop Integrator | WW | U803 Pin 1 | DVM | +1 V to +QV<br>+6 V typical |
| PLL2 Loop Integrator | WW | U803 Pin 7 | DVM | +13 V |

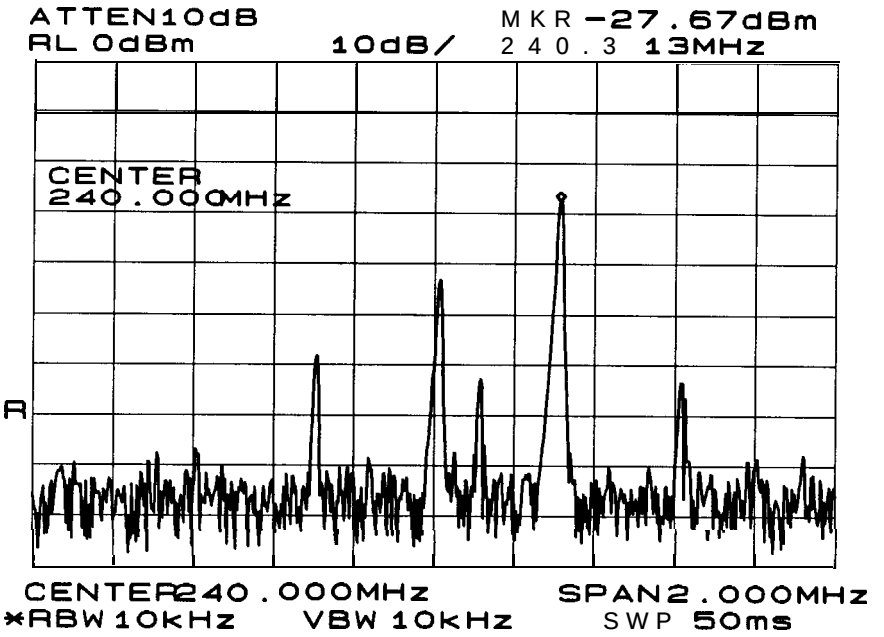



**Figure 3-13. Phase-Lock-Loop 2, First IF Signal Example**

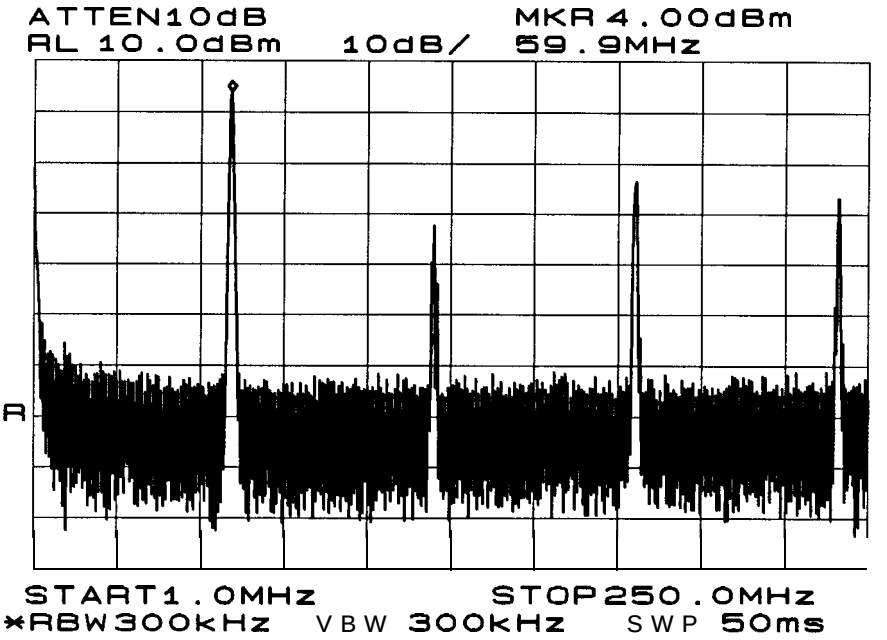



**Figure 3-14. Phase-Lock-Loop 2, Second IF Signal Example**

The loop can be forced open by connecting a positive power supply across C809. The voltage supply directly tunes the oscillator, the response of the different areas of the phase-locked loop can be examined in this mode. However, integrator U803A, does not operate properly in this mode. U803A output rails either high or low, depending upon whether the VCO frequency is too high or too low. If the VCO frequency is too low, the voltage should be high at about +13 V.

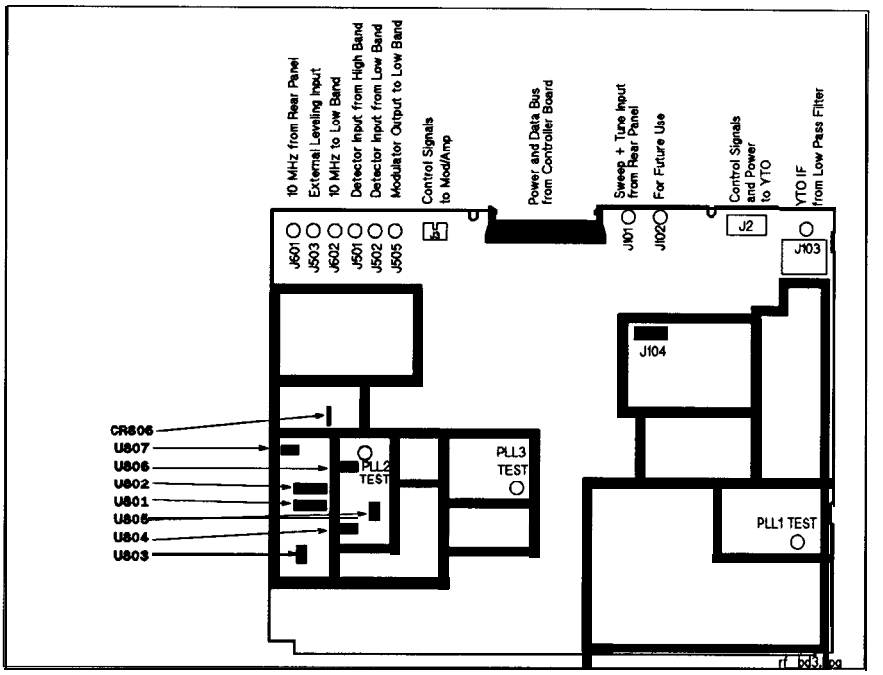



**Figure 3-15. Phase-Lock-Loop 3 Test Point Locations**

**PLL3 Troubleshooting.** The following values were derived by using an HP 8562A spectrum analyzer. The center frequency is set to 1 GHz in zero span. The tracking source is set to tracking mode with the spectrum analyzer selected as the host instrument.

Move YTO test jumper 5103 to TEST position until you have finished making measurements. Return the jumper to normal operating position when finished.

**Table 3-3. PLL3 Troubleshooting Information**

| PLL3 Schematic Sheet 7 | Block | Test Point | Tracking Offset | |
|---|---|---|---|---|
| | | | 190.878 MHz | 190.697 MHZ |
| PLL3 Test | BBB | PLL3 TEST | 270 MHz<br>-8 dBm | 337.5 MHz<br>-7 dBm |
| PLL3 Oscillator | BBB | U919 Pin 7 | +5 dBm | +2 dBm |
| PLL3 Oscillator | BBB | U918 Pin 7 | +3 dBm | +5 dBm |
| PLL3 Oscillator | B B B | U920 Pin 7 | +8 dBm | +6 dBm |
| PLL3 Mixer (RF port) | ZZ | U921 Pin 4 | 240.3 MHz<br>-20 dBm | 240.5 MHz<br>-20 dBm |
| PLL3 Mixer (IF port) | ZZ | U921 Pin 5 | 29.7 MHz<br>-33 dBm | 97 MHz<br>-38 dBm |
| PLL3 IF | AAA | U901 Pin 6 | -34 dBm | -35 dBm |
| PLL3 IF | A A A | U901 Pin 1 | – 13 dBm | – 14 dBm |
| PLL3 IF | A A A | U902 Pin 6 | – 13 dBm | – 15 dBm |
| PLL3 IF | A A A | U902 Pin 1 | +2 dBm | +6 dBm |
| PLL3 Loop Divider | DDD | U903 Pin 7 | Refer to Figure 3-16 | Figure 3-17 |
| PLL3 Loop Divider | DDD | U905 Pins 3, 4, 5, 6 | TTL State<br>L-LOW Low<br>H L L L | TTL State<br>H=High<br>H L L L |
| PLL3 Loop Divider | D D D | U906 Pins 3, 4, 5, 6 | L L L H | L L L L |
| PLL3 Loop Divider | DDD | U907 Pin 3, 4, 5, 6 | H L L L | H L H H |
| PLL3Loop htegrator | FFF | U910 Pin 1 | o v | o v |
| PLL3 Loop htegrator | F F F | U910 Pin 7 | 3.7 v | 10 v |
| PLL3 Loop htegrator | FFF | U911 Pin 1 | -14 v | -14 v |
| PLL3Loop Integrator | FFF | U913 Pins 1, 8, 9, 16 | H H L H | H H H H |
| PLL3 output Divider | CCC | U914 Pin 2 | 45 MHz | 67.5 MHz |
| PLL3 output Divider | c c c | U914 Pin 7 | 15 MHz | 22.5 MHz |
| PLL3 output Divider | CCC | U916 Pin 15 | 7.5 MHz | 7.5 MHz |

The loop can be forced open by connecting a 0 to + 10 V power supply across CR903. Vary the voltage to tune the oscillator throughout its range. The dividers should function correctly. The integrator output (U910 Pin 7) limits high if the frequency is too low, or limits low if the frequency is too high.

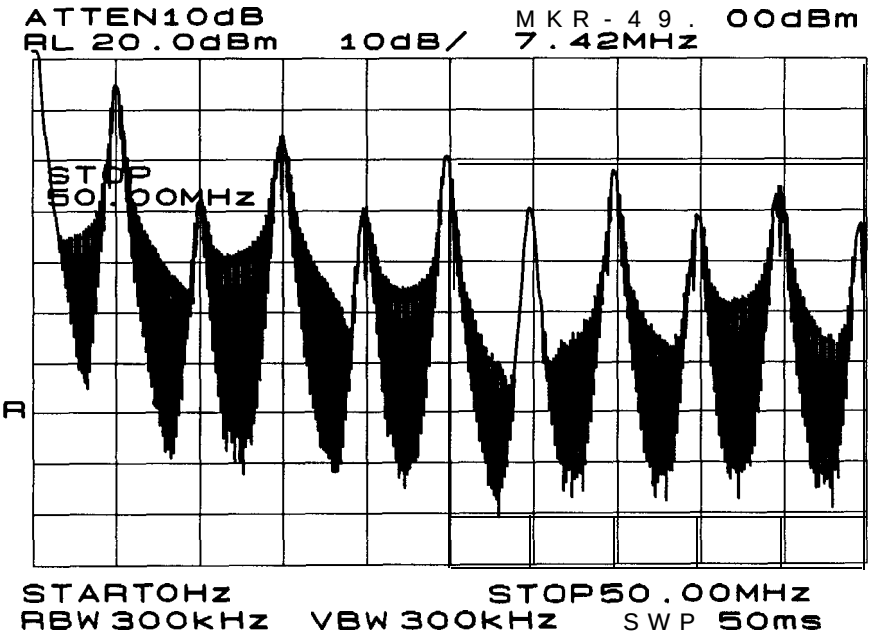



**Figure 3-16. Phase-Lock-Loop 2 First IF Signal Example**

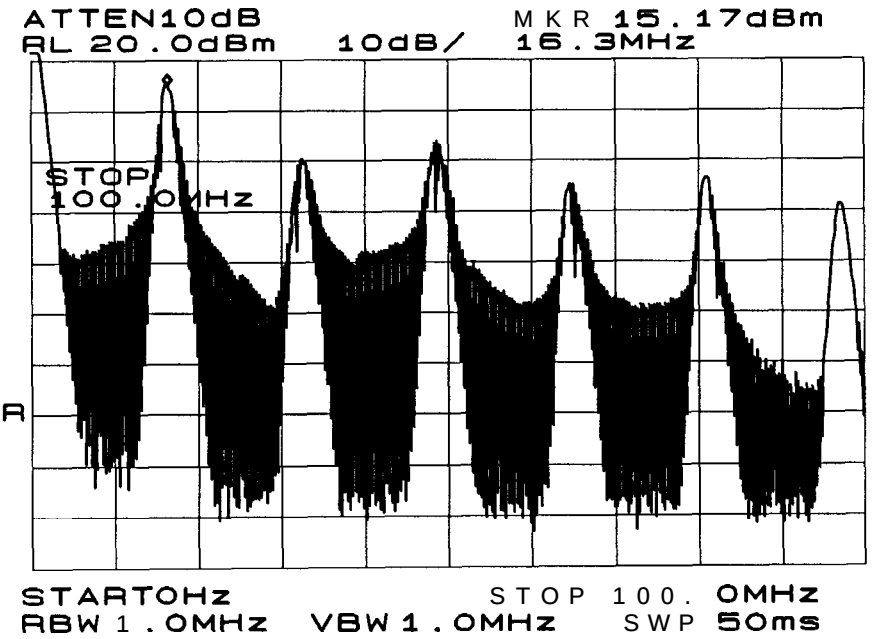



**Figure 3-17. Phase-Lock-Loop 3 High Frequency**

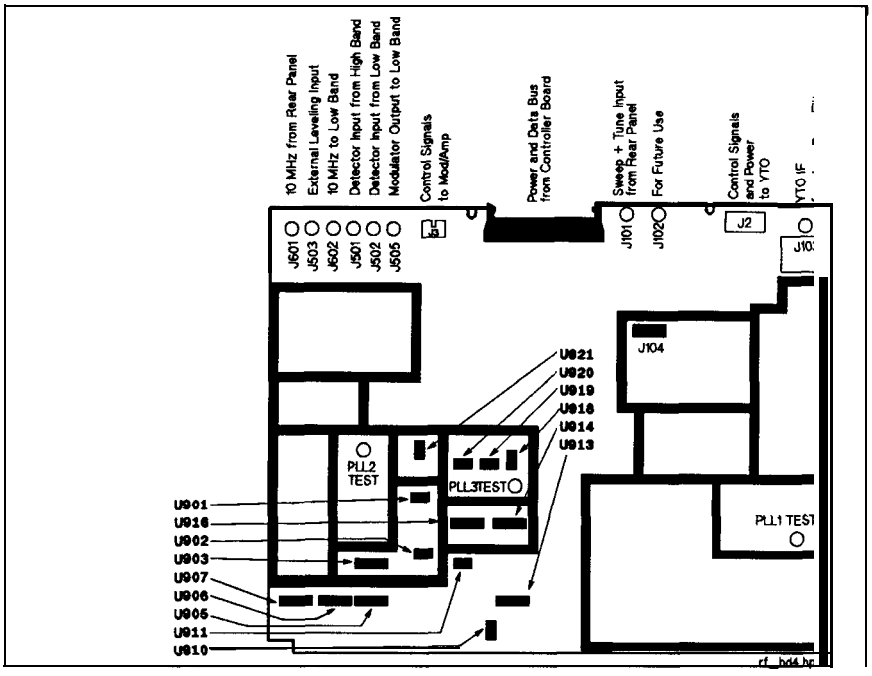



**Figure 3-18. Phase-Lock-Loop 3 Test Point Locations**

## YTO Loop Troubleshooting

Figure 3-19 is a detailed block diagram of the YTO phase-lock loop. The portion within the dotted line represents the A2 RF board assembly circuitry. lb troubleshoot a YTO locking problem, the simplest configuration in which the problem can be observed is used. The following list begins with the simplest configuration, then progresses toward the most complex configuration. Begin troubleshooting by using the simplest configuration to identify the problem. Use the more complex setups as necessary.

Tracking source in CW mode

In CW mode, the output frequency relies only on the sweep + tune offset DACs voltages. These voltages are applied to the YTO main coil. The frequency, before CW calibration is added, should be within a few hundred MHz (or better) of the desired value.

Jumper J104 moved to test position

With J104 in the test position, the instrument's function is similar to CW mode. The difference being that the sweep + tune voltage from the analyzer is added to the voltage from the offset DACs. The jumper shorts the YTO loop error voltage and disables the hardware searching. The remaining voltage is the YTO pretune voltage which should place the frequency within the locking range (within a few hundred MHz) in closed loop operation.

Zero span tracking

In zero span tracking mode, the phase lock loop is activated, but does not have any changes in frequency to track. Also, there is no sweep retrace to cause unlocking.

Single band tracking

In single band tracking mode with narrow spans (less than a few hundred MHz), the instrument operation is similarly to zero span mode. In wider spans the YTO loop would have to relock due to the sweep retracing and, under certain conditions, because of YTF hysteresis. It may be necessary to bandlock the tracking source to insure that it does not change bands near band edges. The PLL1, PLL2, and PLL3 test signals should all be steady. They should not shift in frequency if the tracking source is band locked.

Multiband tracking

In multiband tracking mode, the most complex operation of the tracking source occurs. The YTO loop not only has to unlock between bands due to the host instrument's LO retrace, but also has to follow any YTF hysteresis pulses. Hysteresis pulses cause rapid band changes.

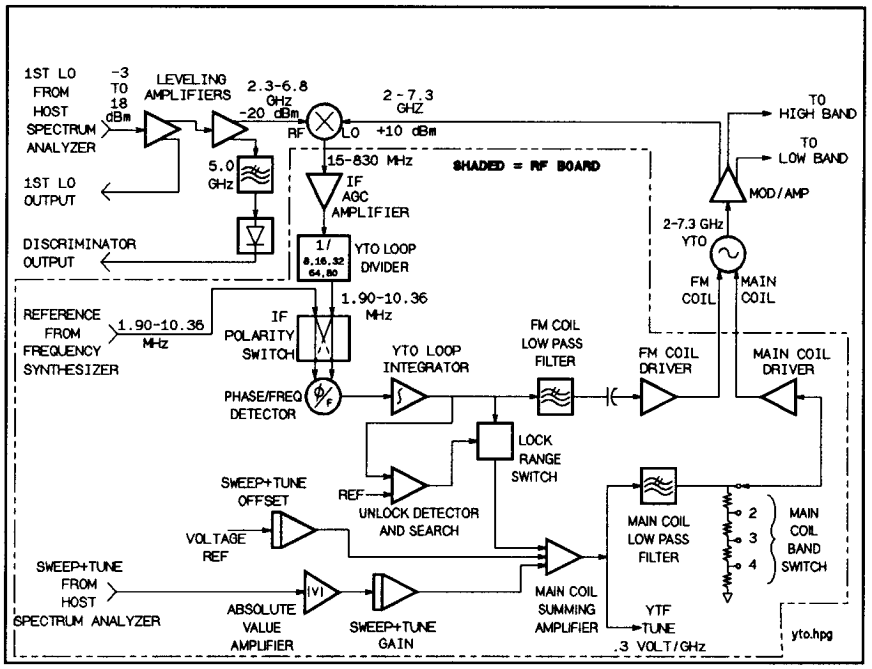



**Figure 3-19. Tracking Source YTO Loop Circuitry**

In general, YTO loop problems can be separated into pretune problems and loop problems. Pretune problems, which are associated with sweep + tune circuits and offset DACs, are easier to diagnose since there is no feedback. Loop problems are easier to solve if they can be analyzed with the loop open (using J104).

When the jumper 5104 is in the normal operation position, the exposed pin of **J104** is the YTO error voltage. The error voltage is also known as the YTO integrator output. It should be about 0 V (within a few volts) when the tracking source is locked and the sweep rate is not too fast (less than 100 **GHz** per second). If something causes the error voltage to be around **+9** V or -9 V, the hardware search activates and causes an unlocked condition.

Slowing the sweep rate of the host analyzer can sometimes decrease unlocking. This is especially true of the YTO error voltage is large. The increase in time helps compensate for the charging of a capacitor in the loop, such as in the main coil low pass filter.

If the tracking source unlocks only near band edges, then the cause is most likely the discriminator or the sweep + tune voltage. Refer to the procedures at then end of this section.

**YTO Loop Troubleshooting in CW Mode,** In low band, 4.2 **GHz** must be added to the CW frequency for all calculations in the last column of **Table** 3-4. N is the harmonic number for the frequency.

If the voltages above all appear correct, check the output voltage coming directly from the **YTO.** Also check the power supply voltages to the YTO.

**Table 3-4. CW Mode Voltages**

| Schematic Sheet 1 | Block | Signal | Location | CW = 3 GHz | CW = F GHz |
|---|---|---|---|---|---|
| Sweep + Tune Gain | B | UN-S+T | **U2 Pin 7** | -5 v | -5 v |
| Sweep + Tune Offset | H | **D_YTO_OFFS_F** | **U19** Pin 5 | -0.9 v | -0.3 ***F** V |
| **Sweep** + Tune Offset | H | **D_YTO_OFFS_C** | **U19** Pin 6 | **N/A** | **N/A** |
| Main Coil Summing Amplifier | C | **D_YTO_SUM** | **U18** Pin **6** | **+0.9** V | **+0.3*** FV |
| Main Coil Low Pass Filter | D | SWP+T | **U7 Pin 1** | **+0.9** V | **+0.3*** FV |
| Main Coil Band Switch | E | **D_YTO_BAND** | **U18** Pin 7 | **+0.9** V | **+0.3 *F/N** V |
| Main Coil Driver | F | **D_YTO_SENSE** | **U18** Pin 12 | **+2.06** V | **+0.69** *F/N V |
| Main Coil Driver | F | YTO Main **Coil** | **C58 Negative** Side | **+25** V | **+32** V to **2.2*F/N** V |
| FM **Coil** Driver | K | **D_YTO_FM_DVR** | **U19** Pin 7 | ov | ov |

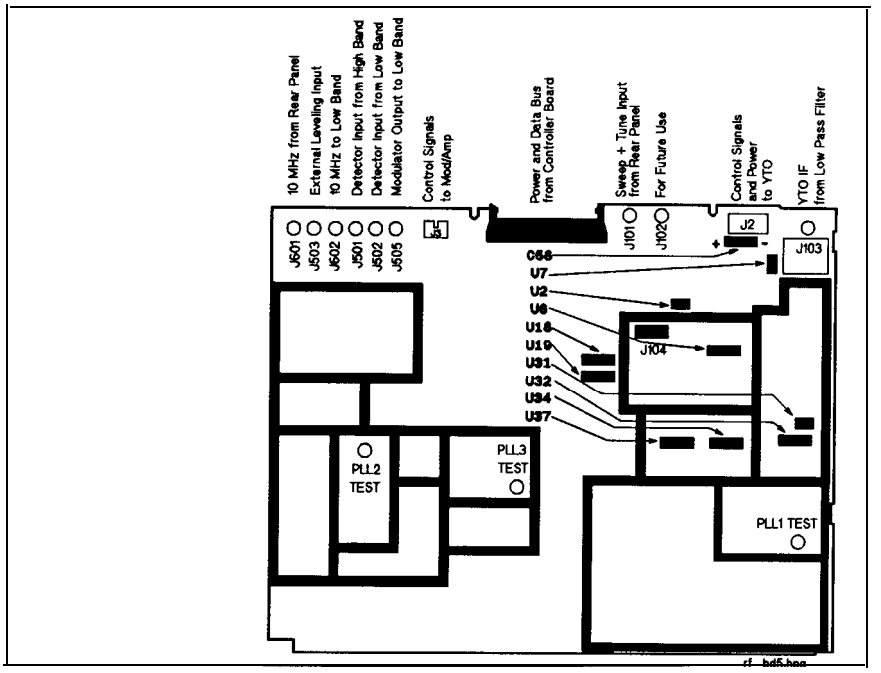



**Figure 3-20. YTO Loop Test Points**

**YTO Loop Troubleshooting in Tracking Mode.** Use the procedure below to identify a problem in the tracking mode.

1. Check that CW mode works at the problem frequency.
2. Put the tracking source in tracking mode with the host instrument selected.
3. Set the host instrument span to zero span at a frequency where the problem still occurs.
4. Move jumper 5104 (the RF board jumper) to the test position to disable the loop searching circuitry and ground the loop error voltage. The test position is the position nearest the edge of the board.
5. Perform the following checks using the procedure below:
   a. Find the frequency of the output. The frequency should be within a few hundred MHz of the desired frequency. If not, measure the following signals to check the pretune voltages from the sweep + tune circuitry.

**Table 3-5.**
**Tracking Mode Voltages (F indicates frequency in GHz)**

| Schematic **Sheet 1** | **Block** | **Signal** | Location | **HP 8562B Host Instrument** | **HP 8566B Host Instrument** |
|---|---|---|---|---|---|
| Sweep + Tune Input Voltage | A | | Cable to **J101** | + **0.5*F** V | **−1.0*F** V |
| Absolute Value **Amplifier** | A | D-S-T-ABS | **U18** Pin **5** | + **0.125*F** V | + **0.25*F** V |
| Sweep + Tune Gain | B | UN-S+T | **U2 Pin 7** | **−0.3*F** V | **−0.3*F** V |
| Main Coil Summing **Amplifier** | C | D-YTO-SUM | **U18** Pin 6 | + **0.3*FV** | **+0.3●** FV |

b. Measure the signal level and frequency at the cable coming to 5103. This should be between -16 and -26 dBm. If it is not, check that the output of the last leveling amplifier is about + 10 dBm. A much lower level would indicate any of the following:

- A bad leveling amplifier.
- No LO input from the host instrument.
- A bad cable.
- Bad leveling amplifier calibration data.

The frequency should be near 300 MHz divided by the harmonic number, for all high bands. For example, a host frequency of 8 GHz would be in band 2 and should give a YTO IF frequency of about 300/2 = 150 MHz. This resulting frequency is inaccurate by the inaccuracy of the sweep + tune circuitry, which can be up to a few hundred MHz.

c. Remove the shield over the YTO circuitry and use an active probe with a spectrum analyzer to follow the YTO IF signal along its path to the phase/frequency detector. For the non-offset tracking mode, the dividers in the YTO loop divider section should divide the frequency according to the values in Table 3-6.

**Table 3-6.**
**YTO Divider Frequencies (F = YTO IF frequency at 5103)**

| | Level | HP 8566B Band 0 | HP 8562B Band 0 | Band 1 | Bands 2 through 4 |
|---|---|---|---|---|---|
| U31 Pin 2 | 0 dBm | F MHz | F MHz | F MHz | F MHz |
| U31 Pin 5 | 0 dBm (ECL) | F/4 MHz | F/4 MHz | F/4 MHz | F/4 MHz |
| U32 Pin 3 | 0 dBm (ECL) | F/8 MHz | F/8 MHz | F/8 MHz | F/8 MHz |
| U32 Pin 14 | 0 dBm (ECL) | F/16 MHz | F/16 MHz | F/16 MHz | F/16 MHz |
| U34 Pin 13 | 0 dBm (ECL) | F/64 MHz | F/32 MHz | F/32 MHz | N/A |
| U34 Pin 15 | 0 dBm (ECL) | F/64 MHz | F/32 MHz | F/32 MHz | F/16 MHz |
| U37 Pin 6 | 0 dBm (ECL) | F/64 MHz | F/32 MHz | | HP 8566B F/16 MHz HP 8562B F/16 MHz |
| U37 Pin 11 | | | F/32 MHz | | |

The frequency from 5103 is divided and applied to the phase/frequency detector U37 pin 11 or pin 6. Which pin is determined by the IF polarity switch and depends on the polarity of the mixing in the YTO mixer. In Table 3-6, the pin that receives the YTO IF frequency in the different bands is indicated.

Check the phase/frequency detector in combination with U22 difference amplifier. Refer to the steps below:

a. Insure that jumper **J104** is in the TEST position.

b. Connect an oscilloscope to the output of **U22,** pin 6.

c. Check that the input frequencies to the phase/frequency detector on pins 6 and 11 of **U37** with an active probe and a spectrum analyzer. One of these signals is the reference frequency for the YTO loop and remains Axed. (For convenience, store this signal in trace B of the spectrum analyzer to use for comparisons later.)

d. Select the extended Test Menu **Test #7** S + T OFFSET C function. Access the extended menu by pressing the number (4) and (GHz) at the same time until EXTENDED MEND is displayed. Scroll to test **#7.** Refer to Chapter 4, **"Test** Key Menu Functions" for additional information.

e. Adjust the YTO IF frequency until the frequency at pin 6 of **U37** is about half of the value at pin 11 of **U37.** The output at **U22** should always be positive, even though there is ripple and perhaps saw-tooth waveforms riding on the dc level.

f. Use the **S+T** OFFSET C function and adjust it until the frequency at pin 6 is about two times the frequency at pin 11.

g. Verify that the output of **U22** is negative. The output should be negative including the signal variations.

## Unlock Detector and Search Circuitry Troubleshooting

**To** check the unlock detector and search circuitry, remove the shield and set **J104** in the TEST position. Refer to the procedure below:

1. Connect an oscilloscope probe to **U18** pin 9 **(D_YTO_UNLK).**
2. Connect a jumper between **U6** pin 7 and the -15 V supply. The oscilloscope should show a series of pulses about 2.5 ms wide with an amplitude of about + 12 V. Refer to Figure 3-21 for an example of the signal.
3. Repeat the above step, but connect the jumper to the + 15 V supply. The oscilloscope should indicate the same signal as before, but the amplitude of the pulses is -12 V.

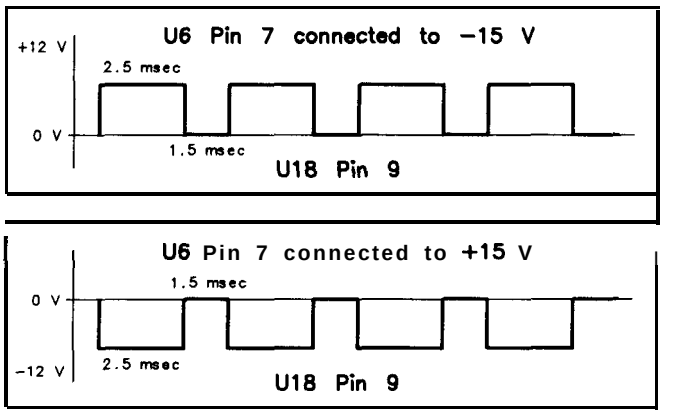



**Figure 3-21. U18 Pin 9 and U6 Pin 7 Pulse Examples**

**Unlocking at Band Edges and Discriminator Problems.**

If the tracking source unlocks only near band edges, the cause is most likely the discriminator or the sweep + tune voltage.

lb check for unlocking at band edges and for discriminator problems, refer to the procedure below:

1. Use the BAND LOCK function under the extended Adjust Menu to band lock the tracking source.
   - Access the extended menu by pressing the number (7) and (GHz) at the same time until EXTENDED MENU is displayed.
   - Scroll to ADJ. #4 and select the BAND LOCK function. Refer to Chapter 5, "Adjust Key Menu Functions" for additional information.
   - If band locking the instrument solves the problem, the trouble is probably with the discriminator.
2. Set the host spectrum analyzer to zero span and tune it to a center frequency where the unlocking occurs. If necessary, band lock the spectrum analyzer to insure that it remains in the desired frequency band.
3. Read the discriminator threshold voltage under Test #11 in the extended Test Menu.
   - Access the extended menu by pressing the number (4) and (GHz) at the same time until EXTENDED MENU is displayed.
   - Scroll to ADJ. #11 and select the DSC THRSH function. Refer to Chapter 4, "Test Key Menu Functions" for additional information.
   - The number displayed is the threshold voltage in millivolts. Typically, it is a value between 100 and 200 mV. The value is set during the calibration of the second leveling amplifier. Adjust the threshold up and down. If the locking problem disappears, the cause is probably in the leveling amplifiers or their adjustment.

4. Measure the voltage at the discriminator output. The discriminator output is located at the output of the detector on the top of the deck and behind the instrument's line switch. (Also, you can measure this voltage at the coaxial connector near the top-center of the **A3** Controller **Board** assembly.

   - If this voltage measures above the threshold voltage, the controller selects the higher of the two possible bands
   - If this voltage measures below the threshold voltage, the controller selects the lower of the of the two possible bands.
   - If the voltage and band selection does not correlate, suspect any of the following:
     - The leveling amplifiers
     - The calibration of the leveling amplifiers.
     - A bad detector.
     - A bad cable.

5. Check the discriminator functionability by measuring the discriminator output voltage.

   - Set the host spectrum analyzer to 3 **GHz.**
   - Measure the discriminator output at the location described above.
   - Check that the output is above 200 **mV** (it is typically above **400mV).**
   - Check the polarity. The polarity is probably negative, but either polarity is acceptable.

6. If the discriminator voltage appears to be correct, check the sweep + tune voltage at **U2** pin 7.

   - Check the voltage at **U2** pin 7. The value should be equal to -0.3 V times the spectrum analyzer's center frequency in **GHz, ±3%.**
   - If the voltage is correct, continue checking the voltage by following it to the ADC.
   - Verify that the voltage is correct along the path to the ADC checking that the connections, the **MUXs** and the buffer amplifiers are functioning properly.

### Leveling Loop Troubleshooting

There are three additional leveling loops beyond the ALC. These are as follows:

- Leveling amplifier 1.
- Leveling amplifier 2.
- YTO input leveling.

Refer to **Table** 3-7 below to determine quickly whether these loops are working correctly. Refer to **Figure** 3-22 for the approximate locations of the test points.

**Table 3-7. Leveling Loop Voltage Verifications**

| | Measurement Point | Normal Operation | No Input Signal |
|---|---|---|---|
| Leveling Amplifier 1 | PIN ATTEN | Approximately −2 V | Approximately +14 V |
| Leveling Amplifier 2 | PIN ATTEN | Approximately −2 V | Approximately +14 V |
| YTO Input Leveling | MOD AMP IN1 | Approximately−1.2 V | +0.7V |
| | MOD AMP IN2 | Approximately − 1.2 V | −5 v |

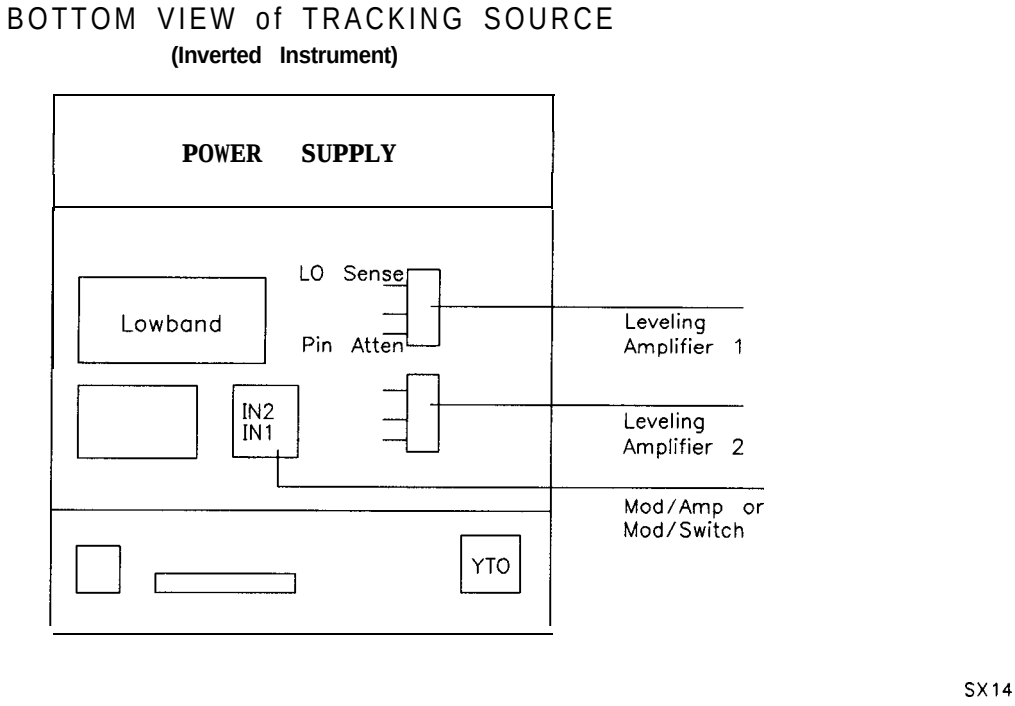



**Figure 3-22. Tracking Source Power Supply (Inverted Instrument View)**

The voltages in the column labeled No Input Signal occur if there is no LO input signal from the host instrument, or if there is no input to the Mod Amp (or Mod Switch) from the YTO.

These voltages can also occur if the detectors or detector cables are open. The cables to check are labeled LO SENSE on the leveling amplifiers and DET or REF on the Mod Amp microcircuit.

Be aware that the leveling amplifiers have LO sense voltages that are different from the value printed on the microcircuit label. The actual voltage depends upon the appropriate leveling amplifier adjustment.

The YTO input leveling loop divider circuits are on the RF board assembly and are illustrated in RF board schematic sheet 3, block DD.

Refer to Table 3-8 for the acceptable input and output voltages for the YTO and leveling amplifiers. Refer to Figure 3-23 for the approximate locations of the test points.

Refer to **Table** 3-8 for the acceptable input and output voltages for the YTO and leveling amplifiers. Refer to Figure 3-23 for the approximate locations of the test points

**Table 3-8.**
**Leveling Loop Input and Output Voltages Verification**

| | Input Voltage | Output Voltage |
|---|---|---|
| Leveling Amplifier 1 | -2 **dBm** to + 18 **dBm** | +9 **dBm** to + 12 **dBm** |
| Leveling Amplifier 2 | + 1 **dBm** | + 10 **dBm** |
| YTO | | +9 **dBm** to +18 **dBm** |

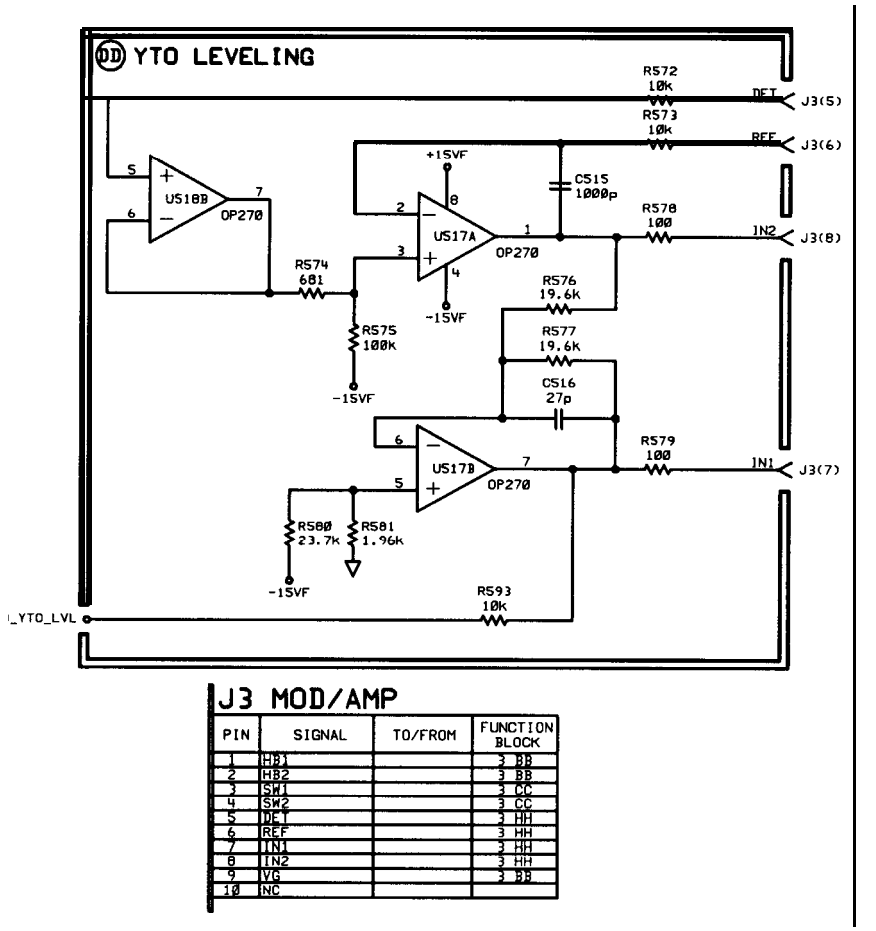



**Figure 3-23. Tracking Source YTO Leveling Loop Circuitry**

The reference voltage of 50 **mV,** which equals the desired detector voltage, is set by the **value** of **R574** times the current through it. The current is essentially constant and equal to -15 V divided by the **value** of **R575.**

The first leveling amplifier may go unleveled if the input signal is near + 18 **dBm.** This is normal operation.

The leveling amplifier drive circuits are on the controller board. The reference voltages for them are set by DACs.

## ALC Troubleshooting

Refer to Figure 3-24 for an illustration of the ALC loop. Table 3-9 lists the typical voltage values for low band or high band operation.

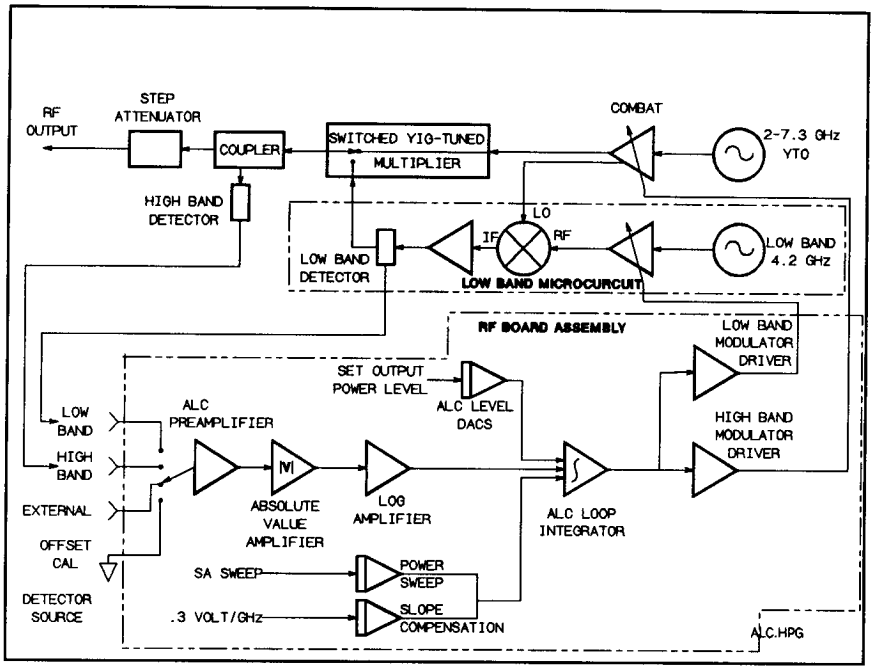



**Figure 3-24. Tracking Source ALC Loop Circuitry**

### ALC Troubleshooting Aids

Under the extended Test Menu, select the function test #5 UNLVL PWR. Test #5 is especially useful for setting the output power level without having tghe ALC loop function.

When the UNLVL PWR function is selected, U516B switch closes around the integrator and turns it into an amplifier. The input selector MUX is set to the calibrate input. As a result, no signals are applied to the ALC circuitry from the detectors.

In the above mode, the step keys adjust the output power by changing the ALC coarse level DAC. The coarse level DAC is no longer calibrated, so trial and error must be used to determine the proper setting for the desired output power level. Usually, the steps are very coarse, and it is easier to make the adjustments using the test #13 ALC FINE function after test #5 UNLVL PWR is activated.

Another troubleshooting aid is to use the test #12 ALC COARSE function under the extended Test Menu. In normal operation, the output attenuator steps, or changes, as the output power is lowered below −10.99 dBm. Using test #12 ALC COARSE lowers the output power to the minimum power level that can be managed by the ALC system without switching the attenuator.

### Distinguishing Between Unlocking and ALC Problems

When the tracking source is in normal tracking mode, locking problems generally show as drop-outs in the output signal. The drop-outs can be viewed on a spectrum analyzer. These drop-outs are especially evident at the beginning of the spectrum analyzer frequency bands where locking requirements are the most stringent.

ALC problems, however, generally appear as changes in amplitude that do not extend all the way down to the noise floor. Some of the low band ALC circuitry is common to the high band, some of it is specific to the band selected. The circuitry is identical for all high bands. This suggests that if there are flatness problems that appear different in the different high bands, the problem may not be with the tracking source, but with the spectrum analyzer.

Check for the following conditions to help determine the source of the problem:

- Compare the low band problem with the high band problem.
- Compare the problem in each of the high bands.
- Compare the problem in CW mode with the problem in tracking mode.

For noisy signals that are tracking, the following procedure can help identify whether the problem is related to frequency locking or to the ALC.

- Change the resolution bandwidth of the host spectrum analyzer.
  - If the amplitude of the noise stays constant, the problem is probably related to the ALC.
  - If the noise increases as the bandwidth decreases, the problem is probably related to frequency locking.
- Set the tracking generator to offset tracking mode.
  - Adjust the tracking offset until the trace drops about 10 dB.
  - Notice the appearance of the noise.
  - Now adjust the tracking offset to the same magnitude, but in the opposite polarity, and compare the signal with the previous signal.
  - If the noise appears unchanged in either state, suspect the ALC.
  - If the noise changes (such as it appears above the trace for one offset and below the trace for another offset), suspect a frequency locking problem.
  - Set the power level to +30 dBm which causes an unleveled ALC at all frequencies. The noise should disappear if the cause is the ALC.

**Table 3-9. ALC Voltages with Spectrum Analyzer in Zero Span**

| Frequency Band | Schematic & Measurement Point | Pin Measured | −10 dBm | 0 dBm | +10 dBm |
|---|---|---|---|---|---|
| Low Band 1 GHz | ALC Input Selector | U501 Pin 5 | 10 mV | 44 mV | 180 ml |
| | ALC Input Selector | U521 Pin 6 | < 10 mV | < 10 mV | < 10 mV |
| | ALC Preamplifier | U502 Pin 6 | 0.11 v | 0.48 v | 1.9 V |
| | Absolute Value Amplifier | U505 Pin 1 | 0.11 v | 0.48 v | 1.9 7 |
| | ALC Log Amplifier | U514 Pin 6 | -0.45 v | -0.11 v | + 0.21 7 |
| | ALC Level DACs | U514 Pin 12 | -3.6 v | -4.5 v | -5.5 V |
| | ALC Loop Integrator | U514 Pin 7 | -0.10 v | -0.14 v | +0.34 V |
| | High Band Mod Driver | | | | |
| | HB2 | U507 Pin 7 | 2.2 v | 2.2 v | 2.2 V |
| | Vgg | U518 Pin 1 | −6 V | -6 V | - 6 7 |
| | Low Band | U508 Pin 7 | 1.4 v | 1.2 v | 1.0 V |
| | Band Switch Driver | | | | |
| | | U519 Pin 1 | o v | o v | 0 V |
| | | U519 Pin 7 | -10 v | - l o v | -10 V |
| High Band 5 GHz | ALC Input Selector | U501 Pin 4 | -1.5 v | -13 mV | -87 mV |
| | ALC Input Selector | U521 Pin 6 | < 5 mV | < 5 mV | < 5 mV |
| | ALC Preamplifier | U502 Pin 6 | -16 mV | -150 mV | -0.95 V |
| | Absolute Value Amplifier | U505 Pin 1 | +16 mV | +150 mV | + 0.95 V |
| | ALC Log Amplifier | U514 Pin 6 | -0.9 V | -0.4 | +1 V |
| | ALC Level DACs | U514 Pin 7 | -2.3 V | -3.8 V | -5.1 v |
| | ALC Loop Integrator | U514 Pin 7 | 0.85 V | 0.88 v | 0.91 V |
| | High Band Mod Driver | | | | |
| | HB2 | U507 Pin 7 | -2.1 v | -1.95 V | -1.8 V |
| | Vgg | U518 Pin 1 | -1.4 v | -1.7 v | -2.0 v |
| | Band Switch Driver | | | | |
| | SW1 | U519 Pin 1 | -10 v | -10 v | - l o v |
| | SW2 | U519 Pin 7 | o v | o v | o v |

The values in Table 3-9 are typical and the actual values may differ somewhat.

Log amplifier output — The log amplifier output value depends on the characteristics of the diodes in the log amplifier. Under all input and diode conditions, the output voltage should be between -3 V and + 1 V.

Coarse level DAC — The coarse level DAC setting depends on the ALC calibration which in turn depends on the log amplifier

characteristics and the detector characteristics.

Integrator output

When the ALC loop is closed, the integrator output voltage must match the drive needed by the modulator for the desired output power. Therefore, this voltage is directly determined by the modulator characteristics and by the gain and loss in the RF path. This level should always be below + 1.5 V whenever the ALC loop is closed.

Modulator driver

Like the integrator output, the modulator driver outputs are also directly determined by the modulator characteristics and the RF path.

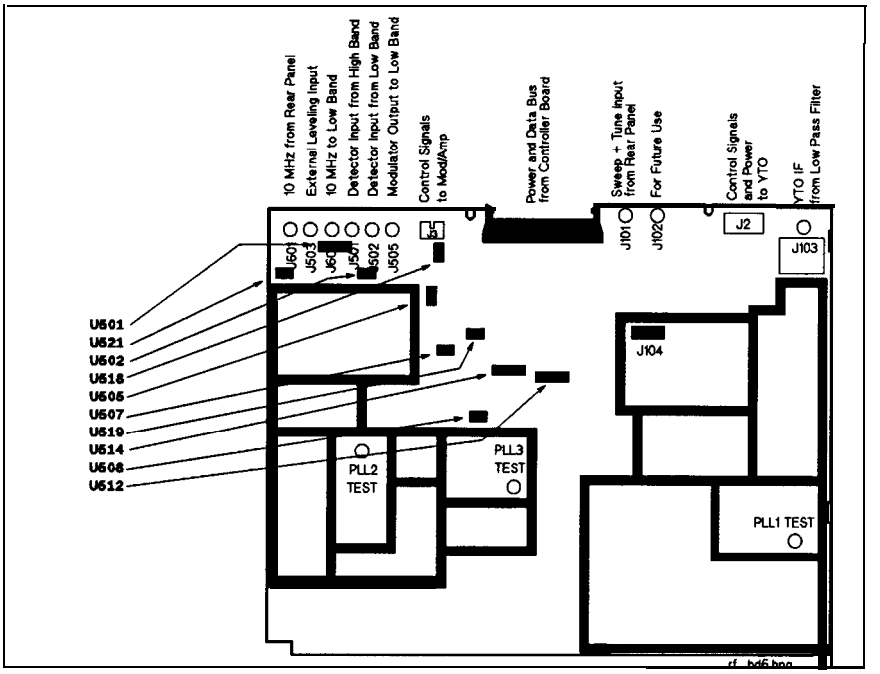



**Figure 3-25. Tracking Source ALC Loop Test Points**

### ALC Input Offset Compensation

Offset compensation at room temperature should be a value very near the center of the offset range. The output of latch U512 is considered to be a 4-bit number, and is usually 7 or 8. If the output is 0 or 15 (at one or the other limit), there is probably a voltage present in the signal path before the log amplifier, even if there is no input signal. Refer to Table 3-10 for the values.

**Table 3-10.**
**ALC Voltages with Spectrum Analyzer in Zero Span**

| Offset Compensation | Latch Bit | output '7" | output "8" |
|---|---|---|---|
| MSB | U512 Pin 16 | 0 V | +5 V |
| | U512 Pin 17 | +5 V | 0 V |
| | U512 Pin 18 | +5 V | 0 V |
| LSB | U512 Pin 19 | +5 V | 0 V |

## A2 RF Board Frequency Reference Theory Detail

The frequency reference section on the A2 RF board assembly supplies the following fixed frequencies:

| | |
|---|---|
| Low Band | 10 MHz |
| PLL1 | 1 kHz |
| PLL2 | 60 MHz |
| PLL3 | 200 kHz |

In addition, the frequency reference section contains a 10 MHz reference oscillator that operates automatically when an external 10 MHz reference is not supplied.

### 10 MHz Input Amplifier

The 10 MHz input amplifier gets the signal from the rear panel, amplifies it, then converts it to TTL levels. The amplification is accomplished with a video amplifier (integrated circuit U601) that supplies about 24 dB of gain.

### Switched 10 MHz Oscillator

The 10 MHz oscillator is used only if an external 10 MHz signal is not connected to the tracking source. When the external reference signal is supplied, the oscillator appears as a TTL level on the line to CR603.

### Low Band Frequency Reference Circuit

The low band frequency reference circuit buffers the 10 MHz reference with U602D. It ac couples the reference signal and provides a 50 Ω load which reduces low band distortions on the cable to the low band microcircuit.

### 60 MHz Generator

The 60 MHz signal is generated in two stages. The first stage is the 10 MHz signal multiplied by 2 in a doubler. The second stage is multiplying the resulting signal by 3. Refer to "PLL2 Frequency Reference" information.

The doubler is essentially a full-wave rectifier. The input signal is split into two paths One path is inverted with an extra gate (U603D). The outputs of the buffer gates are filtered to produce sine waves that are 180° out of phase with each other.

The positive portion of the waveforms alternately turn on diodes CR604 and CR605. This produces the full-wave rectified signal at R615. The signal at R615 contains many even harmonics and the fundamental is suppressed. The bandpass filter Alters the waveform into a 20 MHz sine wave.

### PLL2 Frequency Reference

The 60 MHz filter's output drives amplifier U606 into limiting. Amplifier U606 limits symmetrically so that the output current resembles a square wave, full of odd harmonics The 3rd harmonic (60 MHz) is selected by a subsequent bandpass filter. The filter output is amplified by U607 to provide a large signal for PLL2.

### PLL1 and PLL3 Frequency References

This frequency reference circuit continually divides the 10 MHz reference by 5 and 2 until a 1 kHz signal is obtained. Each divider divides by 2 and then by 5. The divider can be connected to perform either division first.

## Phase Lock Loop Circuit Theory

The circuit theory of PLL1, PLL2, and PLL3 is provided below:

**PLL1**

PLL1 is a phase-locked loop that generates fine frequency steps. These fine steps are especially important for tracking offset adjustments when the host instrument resolution bandwidth is narrow.

The output of PLL1 can be incremented in 2.5 Hz steps (following the PLL1 output divider) from 120 MHz to 200 MHz. The loop bandwidth is 50 Hz to 100 Hz.

**PLL2**

PLL2 is a phase-locked loop that takes the 0.3 MHz to 0.5 MHz output of PLL1 and translates it into a 240.3 MHz to 240.5 MHz range. The translation is accomplished by mixing the PLL2 oscillator output with 240 MHz, then locking the result to the PLL1 output (0.3 MHz to 0.5 MHz).

**PLL3**

PLL3 is a phase-locked loop that combines its frequency steps of 200 kHz with the 2.5 Hz fine steps from PLL2 to generate a range of 270 MHz to 340 MHz. The oscillator output is divided by various numbers to supply the proper reference frequency for the YTO phase-locked loop.

The actual oscillator frequency and output divide number are determined by the microprocessor. These numbers depend upon the host instrument band number, the offset tracking amount, and any tracking adjust frequency.

## YTO Loop Circuit Theory

Figure 3-26 illustrates a detailed block diagram of the YTO phase-locked loop. The portion within the dotted line represents the **A2** RF board assembly circuitry.

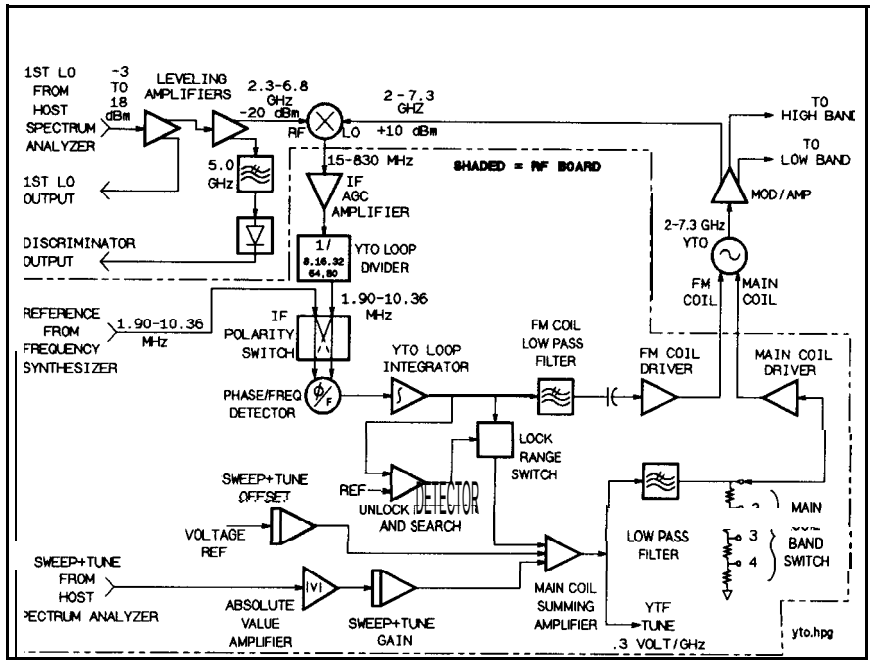



**Figure 3-26. Tracking Source YTO Loop Block Diagram**

The Yig-Tuned Oscillator (YTO) output is routed to the Mod/Amp (or Mod/Switch on the HP **85644A).** The Mod/Amp or Mod/Switch levels the amplitude and distributes the LO signal to low band, high band, and to the mixer in the YTO phase-locked loop.

In the YTO phase-lock loop mixer, the LO signal is combined with the host instrument LO signal. The difference in frequency between these two LO signals is filtered, then passed to the RF board circuitry. On the **A2** RF board, the signal is amplified and leveled to about 0 **dBm** with the YTO IF AGC amplifier.

The amplified signal is then divided with digital dividers and compared to a reference frequency in the phase detector. There is a double-pole, double-throw switch within the two phase detector inputs The switch determines whether the host's LO frequency is above or below the YTO frequency.

The phase detector output is amplified, integrated, and routed to both the main coil and the FM coil of the YTO. The portion of the signal that is passed to the main coil is the dc and low-frequency part. The FM coil is **ac** coupled and only receives the high frequency part of the signal.

The tuning voltage (also called the error voltage), supplied by the phase-locked loop can only tune the **YTO** by a few hundred MHz. A pretune voltage is generated by additional circuitry to set the unlocked YTO frequency within this range. The major component of

the pretune voltage is the host instrument's sweep + tune voltage (also called FAV or frequency-analog voltage). This is made unipolar in the absolute value amplifier and is scaled to a constant sensitivity (V per GHz) by a DAC. The result is summed with other tuning voltages, Altered to reduce phase noise, divided for harmonic bands, and applied to the YTO main coil by the main coil driver.

Another component of the pretune voltage comes from the sweep + tune offset DACs. This voltage compensates for offset tracking mode and low band offset (in low band, the sweep + tune voltage is proportional to the YTO frequency, but with a large offset). In CW mode, these DACs provide the open loop tuning voltage for the YTO. Three components of the pretune tuning voltage have been discussed. There is one other voltage included. This final voltage is the search voltage. When the YTO phase-locked loop in unlocked, the loop can have positive feedback. This generates an error voltage that drives the YTO frequency away from the desired frequency. This occurs because of the mixer in the loop. When this occurs, the unlock detector trips (because the integrator output voltage rails for about 1 ms) and the search circuitry adds a voltage to the main coil to counteract the effects of the error voltage. This search lasts only a few milliseconds. If the loop still does not lock, the search repeats If something prevents locking, the search repeats continuously with a period of about 5 ms.

## ALC Circuit Theory

The ALC circuitry is used to accomplish the following functions in the tracking source:

- lb set the desired output power level.
- lb level the output power.
- To generate power sweeps.
- lb provide slope compensation.

The ALC serves as a feedback system. It senses the tracking source's output power by tapping a portion (-16 dB in high band) of the power to a broadband detector.

The detector output goes through a multiplexer switch that selects the detector to use. The signal is amplified by a gain of 11, then sent to an absolute value amplifier. This absolute value amplifier enables the ALC to operate with detectors of either positive or negative polarity without switching. This is especially important for the external detector mode.

A small dc voltage is summed into the absolute value amplifier to first-order cancel system offsets The cancelation helps the ALC to operate at low detector levels. Normally, the voltage is very close to 0 V, but at high temperatures, it can increase to the limits to the -16 dBm mentioned above. The voltage is set by firmware whenever an ALC calibration is performed, and also whenever a YTF PEAK is performed.

After the signal is processed through the absolute value amplifier, the log of the signal is calculated. Using the log value compensates for the exponential nature of the detector and keeps the loop bandwidth constant. The log value also allows power sweeps to be "linear" in dB.

The log amplifier output is summed with dc voltages from the ALC Level DACs and with ramp voltages (if enabled) from the ALC Ramp DACs. The feedback operation of the ALC loop causes the conditioned detector voltage (at the log amplifier output) to be equal and opposite in polarity to the other signals being summed.

The integrator changes its output voltage until its input voltage equals 0 V. At this point, the output remains fixed, and the loop is closed. The integrator output voltage is conditioned and routed to the correct modulator by the modulator drivers. When the loop is closed, the integrator output voltage, modified by the driver, is exactly what the modulator requires to deliver the desired output power.

There are two other circuits included in the ALC loop. These are the band-switch driver and the YTO-leveling circuit.

The band-switch driver switches a switch located within the Mod/Amp or Mod/Switch for either low band or high band operation.

The YTO-leveling circuit operates in conjunction with a detector and modulator located within the Mod/Amp and Mod/Switch to level the YTO output. This maintains a reasonably constant power level over temperature and instrument-to-instrument variations for the low band mixer and the YTO phase-locked-loop mixer.

## ALC Detector Theory of Operation

The low band ALC has its own detector and it is part of the low-band microcircuit. The detector is temperature compensated with a voltage from a reference diode. The two voltages are subtracted in a differential amplifier. The output of the differential amplifier is the input to the A2 RF board.

The high band ALC contains a coupler and a packaged detector. The output is routed directly to the A2 RF board assembly.

## A3 Controller Board Circuit Theory

The controller board contains most of the tracking source circuitry that is not related to RF or ALC operations. The two main functions (and the majority of the physical components) are for digital and analog control.

The digital control portion contains the processor and interface circuitry. The analog control portion contains the following functions:

- The SYTM driver, comprised of the YTF drive and the SRD bias.
- Power supply filtering and distribution.
- Miscellaneous analog circuitry.

## YTF Drive Circuitry

The A6 SYTM microcircuit multiplies the output signal of the A9 modulation amplifier microcircuit to generate the desired signal for harmonic bands 2, 3, and 4. A6 also contains a YIG-tuned Alter (YTF) that is tuned to track the desired output signal and eliminate unwanted harmonic signals.

The YTF filter is very narrow, having a specified minimum bandwidth of 24 MHz. The YTF driver provides a slope and offset function to tune the filter over the frequency range.

### YTF Drive Operation

The YTF Drive sums the various drive voltages and supplies a drive current to the YTF. The majority of the drive voltage comes from the MAIN-RAMP input, which is a tuning voltage of 0.3 V/GHz.

The remainder of the drive current comes from the other two inputs to the U55 summer. The input from the YTF ADJUST block, contains the slope or gain portions of the drive and has a sensitivity of 20 mA/V of YTF drive. The input from the YTF OFFSET block, which just supplies an offset voltage, has a sensitivity of 10 mA/V.

### YTF Offset Operation

DAC U52 generates the YTF OFFSET signal. The YTF offset range is -133 MHz to 533 MHz at a YTF tuning sensitivity of 15 mA/MHz, and a DAC sensitivity of 2.6 MHz/step.

### YTF Adjust Operation

YTF Gain DAC U53 sums and scales the YTF GAIN and breakpoint voltages.

### YTF Gain Operation

YTF Gain DAC U53 is a 12-bit DAC used to correct overall gain. The gain DAC is adjusted in band 1 from 2 to 7 GHz, and is carried forward to all the other bands The gain variations in bands 2, 3, and 4 are corrected by the breakpoint DACs.

### YTF Breakpoints

The YTF breakpoints add additional gain to the YTF drive. The additional gain accounts for the non-linearities in tuning the YTF. All four breakpoints follow the same basic design. Breakpoint 4 is an exception because it has a DAC that adjusts the breakpoint frequency.

## SRD Bias Circuitry

The SYTM uses an SRD (step recovery diode) to generate the harmonics of the input signal. The YTF then selects the desired harmonic The bias voltage applied to the SRD optimizes the power for the desired harmonic and maximizes the output power from the tracking source. Over a frequency band, the optimum bias generally is an increasing voltage.

Use the Power Level Adjustment to scale the A9 modulation amplifier detector voltage to a nominal +5 V. The +5 V is used by the multiplier circuitry. The multiplier circuitry scaling provides the

SRD bias voltage that changes the power of the signal from the A9 modulation amplifier to the SYTM.

## Analog Control Circuitry

The unleveled detector generates an interrupt when the ALC goes unleveled. The ALC_IRQ unleveled interrupt line goes to the MFP. The MFP searches for the rising or falling edge, generates the interrupt signal, and turns on or off the unleveled detector indicator. The comparator has a 2.5 V threshold.

## Miscellaneous Analog Circuitry

The remaining analog circuitry is described in this section.

### SYTM Heater

The SYTM heater maintains a constant 85°C temperature in the SYTM heater. FET Q3 controls the current flow to the SYTM heater. When the output of U5 is + 10 V, the FET gets turned off. When the FET is turned off, there is no current flow to the SYTM heaters. When the output of U5 is -10 V, the FET is turned on and maximum current to the SYTM heaters is available.

Resistors R89 and R90 set the operating point of the heater control loop, thus controlling the temperature.

### Attenuator Latch

The attenuator latch provides digital control lines to various analog devices. The four LSB of the latch drive the attenuator.

The following digital lines control the devices described:

- D4 controls the LOW BAND POWER circuity
- D5 controls the PIN SWITCH DRIVER for the SYTM (SYTM-HB)
- D6 is a digital signal that is sent to the A15 Low Band microcircuit
- D7 is a dual DAC select line (LVL-AB)

### HI/LOW Band Switch

This circuitry (on the HP 85645A only) controls a pin switch in the SYTM. This pin switch combines the separate high- and low-band paths into a single output and selects which one is active.

When SYTM-HB is 1, the high-band path is selected.

When SYTM-HB is 0, the low band path is selected.

## Analog Circuitry Troubleshooting Hints

Due to the large number of DACs in the analog circuitry, it is best to rely on the internal diagnostic test routines. The routines can help you quickly locate a problem.

For the limitations to the internal diagnostics tests, most of the diagnostic tests can be manually performed.

- lb measure a fixed voltage (such as a power supply), you can measure that voltage with a voltmeter.
- To verify DACs, perform the adjustment procedure that uses the DAC in question and change the DAC value and observe the instrument performance. As an example, if you adjust the YTM offset DAC, observe whether the unleveled output power go up and down.
- If none of the DACs work, the problem may be related to the control-bus buffers or the hardware strobes rather than to the specific DACs.
- If the diagnostic test results indicate several problems, there may be trouble beyond the scope of the routines. The problem may be related to the diagnostic lines or the ADC rather than with the hardware tested.

### A3 Controller Board Troubleshooting Detail

The A3 Controller board has several, built-in troubleshooting aids. Diagnostic lines from most of the analog blocks return to the ADC for automatic testing.

Feedback registers and turn-on tests are incorporated into the digital design. Therefore, if the processor is able to run, and the problem is on the processor, then it can identify the probable cause. If the processor cannot run, it cannot identify the problem.

The first part of this troubleshooting information is about repairing the digital system. Then the digital diagnostic tests are explained.

The final section provides some information about locating problems in the analog circuitry.

**Digital Core Components: CPU, ROMS, Error LEDs.** The digital core is made up the following:

- CPU (U12)
- UVPROMs (U18 & U78)
- Error LEDs (U23 & U24)
- Discrete logic components for digital processing:

  0 Timing (U107)

  - MUXs (U17)
  - RAM (U9 and U22)
  - Clock (U1 and U2)

Notice that the ROMs (U19 and U20) are not included.

The above components make up the core and is the smallest subset of integrated circuits needed to generate the LED "light show". By displaying a unique pattern sequence with the error LEDs, the processor indicates that it is functioning properly. If the "light show" does not appear as indicated in Figure 3-27, some part of the digital core is not functioning.

**Error LEDs Power-On Light Show.** When the processor powers up, the "light show" occurs immediately. The "light show" is accomplished by reading ROM instruction data, then writing the data to the error LEDs. The "light show" should occur as follows:

1. All of the LEDs are turned on, then off in a single flash.
2. The LEDs are turned back on two at a time, beginning with the two outside edge LEDs, then moving toward the center until all LEDs are lighted.
3. At the completion of the "light show", all of the LEDs are turned off and remain off.

Figure 3-27 illustrates is an example of the "light show" pattern.

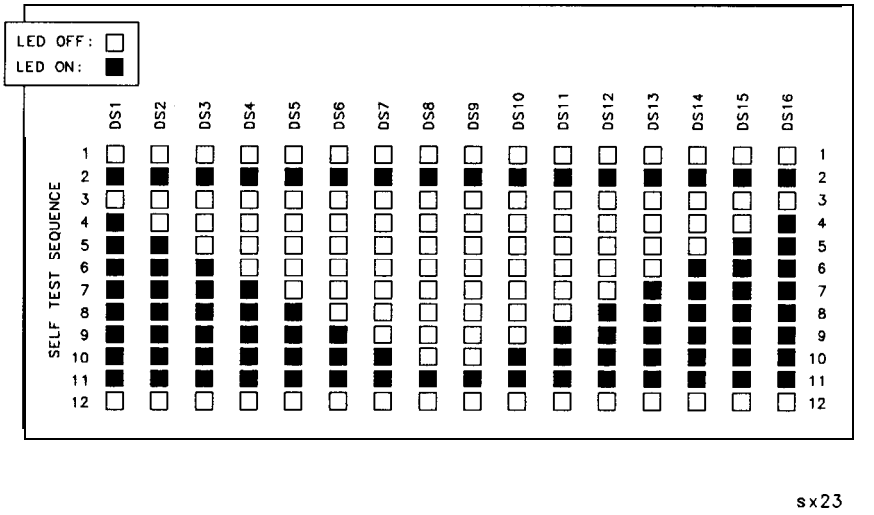



**Figure 3-27. A3 Controller Board Error LEDs "Light Show"**

Since the error LEDs are usually on when the power is turned on, the initial flash may appear to occur twice. The following functions occur before the actual "light show" flash and sequence begins.

- The front panel is turned on just before the error LEDs flash.
- On the front panel, status LEDs turn on and the DEL (an alternating pattern of on and off squares) character appears in each of the 16-character display windows.
- There is a 500 ms delay preceding the initial flash. If, for some reason, the processor continues to repeat the "light show," this delay allows us to read the error LEDs before they are turned off.

**If the 'Light Show" Does Not Occur.** If the "light show" does not occur, try to determine whether the processor is functioning at all. The areas to check first are listed below:

- Check that the ROMs are in their correct sockets and well seated. Check that none of the ROM pins are bent.
- If the error LEDs change state (on to off, or off to on) or you hear the attenuator clicking every few seconds, then the processor is running, but not correctly. If you see these symptoms, the ROMs probably need to be replaced.
- Check the processor's +5V supply, Vcc.
- Check for high signals on the reset (RST) and halt (HLT) lines. If either or both of these lines are low, there is probably a problem with either A3U10 or the power valid (PWR-VLD) signal.
- Touch reset (RST) to Ground *briefly* to reset the processor. This can also be done by shorting U10 pin 6 to U10 pin 7. If the processor begins running, there is probably a problem with the power valid (PWR-VLD) signal's power supply. The reset line and the PWR-VLD line need to remain low 100 ms after the +5V has powered up. The 100 ms allows the processor to turn on correctly and begin running.
- Check for an 8 MHz CLK (clock) square wave signal with an oscilloscope.

If each of the above items indicate no problem, then there is probably problems with discrete logic circuitry. Signature analysis is recommended.

### Mother Bus and Front-Panel Bus Diagnostics

These diagnostic routines are non-fatal. They test the front panel bus and the RF board bus (the mother bus). The controller can start even if there is a problem with one of the busses. As a result, the instrument can be operated over HP-IB while the front panel is disconnected.

For the above two busses, the address and data lines can be read on the output side of their buffers The information from the address and data line can help determine whether there is a short on these lines. In addition, some of the RF and front-panel board address and data lines can be verified for continuity.

### Digital Controller Operation

The digital controller consists of U12, a 68000 processor. The processor operates at 8 MHz, contains 256 kbytes of UVPROM, and 64 kbytes of battery-backed RAM. The controller also contains a multi-function peripheral (MFP) for timers and interrupts, 8 Kbytes of EEPROM for storing calibration data, and error LEDs for controller diagnostics.

**CPU Operation.** The U12 68000 processor is shown in block B of the schematic diagram. In addition to power and a clock, the processor is dependent upon three additional signals to run. These are RESET (pin 20), HALT (pin 19), and DTACK (pin 10).

RESET and HALT are derived from the PWR_VLD signal coming from the power supply. During normal operation, these signals should always be high, not asserted.

Jumper El is used for digital signature analysis (DSA). When jumper El is removed, DTACK and key data lines are forced high or low. This causes the processor to run and cycle though memory even if the ROM, MUXs, timing PAL, or other digital components are broken.

**Timing PAL Operation.** The chief function of timing PAL U107 (in function block K of the block diagram) is to generate the LDTACK signal. Since the MFP generates its own LDTACK signal, the LDTACK from PAL U107 is disabled during access to the MFP. The 1 kΩ resistor, R1, pulls LDTACK high when it is not asserted.

The PAL also generates the LOE (low output enable) signal. This signal enables the outputs from the RAM and EEPROM during a memory read cycle. Finally, the PAL generates the BUS_EN1 and BUS_EN2 signals to control analog hardware timing.

**MFP Operation.** The MFP (multi-function peripheral) handles most of the hardware interrupts in the tracking source. The MFP also handles interrupts from four internal timers. These operate from the 4 MHz clock.

Six of the eight I/O lines are dedicated to interrupts. These inputs are edge sensitive. An interrupt is triggered by either a rising or falling edge, or on any edge, depending upon how the input is configured.

**ROM Operation.** The ROM (read-only memory) is composed of two 1 Mbit UVPROMs. These provide 256 kbytes of ROM.

The RAM memory is composed of the 256 kbyte integrated circuits. These circuits provide 64 kbytes of random access memory. RAM memory is battery backed, which prevents data loss when power is turned off. U21 supplies power to RAM and switches the +5 V power to the battery supply when power is turned off.

**EEPROM Operation.** The EEPROM (electrically erasable/programmable read-only memory) consists of a single integrated circuit that provides 8 Kbytes of memory. The EEPROM contains the tracking source's calibration data.

**Error LEDs.** The Error LEDs indicate digital hardware problems and status. When power is turned on, the "light show" indicates that the processor is running. Any failures of the digital diagnostic test are indicated by the error LEDs. If no errors are detected, DS16 is turned on. After this, DS1—5 indicate what harmonic frequency band the instrument is locked to.

### Digital Interface Circuitry

The digital interface circuity is the interface from the controller board to the other boards in the instrument and to the rear panel. The interface consists of the following:

- The instrument's front panel and mother bus buffers
- The HP-IB and AUX connector circuitry
- A 12-bit ADC and MUX for reading internal voltages

**Mother Bus Buffer Operation. The** mother bus is the 50-pin cable that connects the controller board to the tracking source's RF board and option boards The mother bus buffer circuitry buffers the data and control lines, and provides diagnostic features for the mother bus

**Front-Panel Buffer Operation. The** front-panel bus is the 14-pin cable and the 16-pin cable that connects the controller board to the front panel. Front-panel buffers buffer the data and control lines, and provide diagnostic features for this bus.

**HP-IB Operation. The** HP-IB control integrated circuit, U4, implements all the HP-IB hardware functions. Line drivers U92 and U97 provide the interface to the rear-panel HP-IB connector.

**MUX Inputs. The** analog MUX, U42, receives many inputs that can be directed to the 12-bit ADC, U44. Some of these inputs are for diagnostic purposes Others are for band-locking. The following paragraphs describe these analog inputs:

Diagnostic MUXs

These MUXs route the analog diagnostic lines to the ADC. Latch U88 selects which line and which MUX is routed to the ADC. Only one MUX can be enabled at a time.

Components R205 and R120 create a revision voltage. If a hardware change affects any of the diagnostic lines, the value of these resistors is changed and creates a different revision voltage. By reading the revision voltage, the processor can determine the version of the board assembly and which diagnostic routines to use.

Retrace Input Request Signals (IRQ)

These are rear-panel signals BLANK IN and HI SWEEP These input signals indicate when the host spectrum analyzer is retracing.

The BLANK IN signal is used by the HP 8560 Series spectrum analyzers. BLANK IN is high when the host spectrum analyzer is retracing and it prevents the unleveled LED from turning on during retrace.

The HI SWEEP input signal is used by the HP 8590 Series spectrum analyzers and is bi-directional. The host spectrum analyzer pulls this line low at the end of a sweep. Then the tracking source keeps HI SWEEP low, preventing the spectrum analyzer from sweeping, until the tracking source is re-locked. HI SWEEP also prevents the unleveled LED from turning on during retrace.

## Signature Analysis Troubleshooting

Use signature analysis to check the digital logic while the instrument is running. Signature analysis is accomplished by setting the processor to a known state, connecting the start, stop, and clock lines from the signature analyzer, then touching the data probe to one of the pins on the integrated circuit of interest.

The signature analyzer uses the start, stop, and clock lines to generate a "signature" or number.

Compare the results of this signature with that of a known good board (preferably of the same vintage) to determine whether the digital logic is working correctly.

'Ib perform digital signature analysis on an HP 85644A or HP 85645A, remove jumper El from its socket. Removing the jumper causes the processor to cycle through memory independent of the ROMs, the timing PAL, and other digital logic circuitry. The memory cycle takes approximately 8 seconds.

Signature analysis can not locate problems involving interrupts, nor is a test of the RAM valid. Fortunately, these two areas are checked by the processor when it is functioning.

Signature analysis can be used on the ROMs and data lines, but requires a different setup. In addition, the signatures of the ROMs are dependent upon their date code.

Although you can read the digital signatures of address lines, viewing the signals with an oscilloscope is more informative. By viewing the signals, you can verify whether the processor is running correctly. Since the processor is cycling sequentially through memory, Al is a square wave with a period of 1 $\mu$s, A2 has a period of 2 $\mu$s, and so on until finally A23 which has a period of 4,194,304 $\mu$s (or about 4 s).

To perform signature analysis on the tracking source, follow the steps below:

1. Remove jumper El from its socket. Refer to the A3 Controller assembly schematic diagram.
2. Connect the signature analyzer's lines as follows:

**Table 3-11. Signature Analysis Connections**

| Signature Analyzer | Tracking Source |
|---|---|
| Ground | to GND |
| Clock | to 8 MHz clock |
| Start and Stop | to A23 |

3. Configure the signature analyzer as follows:

**Table 3-12. Signature Analyzer Configuration**

| Function | Setting |
|---|---|
| Signature | Norm |
| Clock | Rising |
| start | Rising |
| stop | Rising |

4. Compare the measured signatures with those of a functioning instrument.
5. To perform signature analysis on the ROMs or data lines, the signature analyzer configuration must be altered to the following:

**Table 3-13.**
**Configuration for ROM Signature Analysis**

| Function | Setting |
|---|---|
| Signature | **Norm** |
| Clock | Rising |
| start | Falling |
| stop | Rising |

Check the address lines. If the processor is running, Al has a square wave with a period of 1 $\mu$s, A2 has a period of 2 $\mu$s, and so on until finally A23 with a square wave of about 4s.

If the square waves are not present on the address lines, or are not what is expected, reset the processor by briefly grounding the RESET line. If the processor still fails to run, recheck the power supply, the RESET and HALT lines, and the clock signal.

### Digital Diagnostics: RAM, MFP, Busses

Once the digital core is working, the light show operates properly, and the processor can perform diagnostic tests on the remaining digital components. The processor can report the results with the error LEDs. Some of the tests identify fatal errors such as a malfunctioning RAM. When one of the fatal errors is encountered, the processor begins a special routine that repeatedly flashes the appropriate error LED. Although digital errors prevent proper instrument operation, they are not fatal to the digital controller. The digital controller continues to operate normally.

Refer to Table 3-14 for the meaning of each error LED. Only the first eight LEDs indicate fatal (catastrophic) errors.

Other tests check the RF board and front-panel board interface busses.

**Fatal Errors.** When one of the diagnostic tests reveal a fatal error, the processor begins a special routine that cycles though valid memory address and flashes the error LEDs. The routine alternates turning on all the LEDs, and only turning on the LED that indicates the located error. During this routine, only the flashing LEDs and the digital core are working.

**Table 3-14. Error LED Descriptions**

| LED Number | Error Meaning | Possible Cause | Fatal |
|---|---|---|---|
| DS1 | RAM bad | | Yes |
| DS2 | MFP data bad<br>The data read from the MFP does not match the data written to it. | Some of the data lines or control lines to the MFP may be broken. Check the 4 MHz clock and perform signature analysis on the data and control lines | Yes |
| DS3 | MFP timer not counting<br>After the 1 ms delay, the timer value did not change. | The timer is not counting. Check the 4 MHz clock line. | Yes |
| DS4 | MFP timer interrupt<br>After 11 ms, the timer time-out and interrupt did not occur. | The MFP integrated circuit probably needs replacing. | Yes |
| DS5 | MFP interrupt<br>The interrupt either did not occur or occurred, but was incorrect. The error flag is set prior to the interrupt so that the error condition is retained if the processor does not function correctly. | The MFP may be faulty. Check the address lines to determine whether the processor is still running. If not, check the LIACK and DTACK lines to the MFP. Also, A3U33 may need to be replaced. | Yes |
| DS6 | MFP interrupt vector<br>The MFP returned an incorrect interrupt vector number during the interrupt-acknowledge cycle. | The MFP probably needs to be replaced. | Yes |
| DS7 | LIACK fail<br>The processor obtained the interrupt vector from RAM, rather than the MFP. | The LIACK signal generated by A3U107 failed. | Yes |
| DS8 | interrupt number<br>The processor obtained the interrupt vector "0FFh" which is neither from the RAM nor the MFP. | The MFP may be faulty, or the LIACK signal from A3U107 may be failing. | Yes |
| DS9 | mother bus data<br>The data read from mother-bus latch U31 differs from the data written to it. | The mother bus data lines may be shorted together or shorted to ground. | No |

**Table 3-14. Error LED Descriptions (continued)**

| LED Number | Error Meaning | Possible Cause | Fatal |
|---|---|---|---|
| DS10 | mother bus address<br>The address lines through U29 to the data bus did not match the address written to. | Either the mother bus address lines or the data lines may be shorted. | No |
| DS11 | mother bus feedback data<br>The data from the four LSB data lines returned from the RF board does not match the data written. | Either there is an open circuit on the A2 RF board assembly or the board assembly is not connected. | No |
| DS12 | mother bus feedback address<br>The data from the four address lines returned from the RF board does not match the data written. | Either there is an open circuit on the A2 RF board assembly or the board assembly is not connected. | No |
| DS13 | front panel data<br>The data read from latch U37 did not match the data written to it. | Either the front-panel address lines or the data lines may be shorted. | No |
| DS14 | front panel address<br>The address lines going through U38 to the data bus did not match the address to which it was written. | Either the front-panel address lines or the data lines are shorted. | No |
| DS15 | front panel feedback address<br>The three LSB address lines from the front panel board assembly do not match the address to which it was written. | There is either an open circuit on the front panel board assembly or the board is not connected. | No |
| DS16 | digital system okay<br>The hardware has successfully passed all the digital diagnostic tests. | | |

**RAM Diagnostic.** The RAM diagnostic test is the first test performed. The test writes to RAM and reads the patterns to ensure that all memory locations are working properly. Any failure lights DS1, the RAM bad LED, and initiates the special processor routine.

Before the processor starts cycling though memory, the RAM is filled with a known pattern. This allows for digital signature analysis.

Refer to the procedure below to perform RAM signature analysis.

1. Connect the following signature analyzer's lines as listed:

**Table 3-15. Configuration for RAM Signature Analysis**

| Signature Analyzer | Tracking Source Connection |
|---|---|
| Ground | to U17 Pin 8 GND |
| Clock | to U2 Pin 5 8 MHz clock |
| Start and stop | to U17 Pin 12 ERR_LED2_CS |
| QUAL | to U17 Pin 7 RAM_CS |

2. Configure the signature analyzer as listed below:

**Table 3-16. Signature Analyzer Configuration**

| Signature Analysis or Function | Setting |
|---|---|
| Signature | Qual |
| Clock | Rising |
| start | Rising |
| stop | Rising |
| Qual | Low |

**MFP and Interrupt Diagnostics.** The multi-function peripheral, MFP, is an integral part of the interrupt system. As a result, when the MFP functionality is tested, so is the interrupt logic

The primary function of the diagnostic routine is to program an MFP timer with a 10 ms wait. At the end of the wait time, the timer generates an interrupt that sets a flag. During this time, the diagnostic routine checks whether the MFP is functioning correctly. It checks for proper programming, for proper counting in the timer operation, and performs other checks.

## A16 Power Supply Circuitry

The five main sections of the power supply board assembly are listed below:

Line Rectifier
: The line rectifier creates a high level dc voltage (nominally 325 V) from the ac power line.

Buck Regulator
: The buck regulator is a switching regulator that steps down the high level dc (nominally 110 V) that was created by the line rectifier. The output voltage is adjusted to obtain the desired accuracy on the 5 V power supply.

dc-to-dc Convertor
: The dc-to-dc convertor converts the output of the buck regulator into an ac voltage that is transformer coupled, rectified, and filtered into the desired dc voltage supplies of 5.2 V, ±18 V, and + 36 V.

Linear Post Regulators
: The linear regulators are used to drop the dc to dc converter output to the final desired value. Since the buck regulator regulates only the 5 V output, the other voltage supplies need some post regulation to achieve the required accuracy and any required current limiting.

Control
: The control circuit's primary function is to provide the signal to the buck regulator which maintains the 5 V output. The control circuit also performs maintenance functions that ultimately turn off or on the power supply and a power-valid signal. The power-valid signal alerts the micro processor when the power supply is functioning properly. The maintenance functions are listed below:

  - Under-voltage lock out.
  - Over-current protection.
  - Over-temperature protection.

### Safety Considerations

Components T103, U206, C105 and C106 provide safety isolation. There is a minimum spacing of 3mm between primary (dangerous) and secondary (safe) circuits. This spacing includes any circuit from a primary circuit to any part of the instrument chassis.

**Warning**

**Circuits illustrated to the left of T103 and U206 on the A16 Power Supply schematic diagram are not isolated and are extremely dangerous.**

**Under normal operating conditions, the primary-common can have several hundred volts, with respect to ground, present.**

**Always use an isolation transformer when you make any measurements to dangerous circuits. The isolation transformer breaks the ac power line ground reference and grounds the primary-common.**

### Input EMI Filter Operation

The input EMI filter reduces the amount of power supply switching noise conducted back onto the ac power line. The components that are responsible for the filtering are as follows:

- Components C103, C104, and L101 form a filter that attenuates the differential-mode noise.
- Components C105, C106, and L101 make up the common-mode filter.
- Components C113 and R112 de-Q the differential filter resonance. (Q is the measure of R/C filter selectivity.)
- Components R119 and R120 discharge all filter caps (for safety purposes) when the ac power line cord is removed.
- Additional high frequency filtering is achieved by a line module connected to 5101.

### ac Line Rectifier Operation

In the 115 V mode (when S102 is closed), CR102 acts as a half-wave doubler. The voltage at TP108 equals two times the square root of twice the RMS value of the ac input voltage (nominal: 2 x 1.414 V x 115 V = 325 V).

In the 230 V mode, CR102 acts as a full-wave bridge rectifier. The voltage at TP108 equals the square root of two times the ac input voltage
(nominal: 1.414 V x 230 V = 325 V).

Components C101, C102, C107, and C108 store the charge that provides the nearly constant voltage to the input of the buck regulator. Inductors L102 and L103, in conjunction with capacitors C107 and C108, provide 40 kHz and 80 kHz of filtering that reduces conducted emissions.

Components RT101 and RT102 are negative temperature coefficient thermistors that limit the in-rush capacitor charging current. Their resistance is approximately 5Ω when cold, then very small when hot.

Component E101 provides surge protection in the 115 V mode. Component E101 also opens the line fuse if the supply is connected to a 230 V ac power line while the instrument is in the 115 V mode. If the power supply gets 230 V while it is in the 115 V mode, the

remainder of the supply can be severely damaged. Both components E101 and E102 provide surge protection in the 230 V mode.

Components R106, R107, and VR201 discharge the main filter capacitors after an under-voltage lockout has occurred. These components also provide the minimal power that supplies the kick-start oscillator.

### Buck Regulator Operation

This is the main switching regulator for the power supply. Transistor Q102 is pulse-width modulated at an 80 kHz rate. The transistor's drive is transformer coupled with clamp-bias C111 and CR106.

Resistor R108 reduces transformer ringing. Resistor R109 discharges the gate capacitance of Q102, that turns the transistor off. Inductor L104 is a turn-off-snubber that also reduces the transient generated by CR108's recovery time.

Inductor L105 is the main-energy storage inductor. The capacitance normally found in a buck regulator is the output-rectifier capacitance that is reflected through T103. The equivalent impedance present at the output of L105 is about 5Ω in series with 150μF.

### dc-to-dc Converter Operation

Component T103 makes up the dc-to-dc converter. T103 is driven by a current source at the primary center tap. The current commutation is accomplished by Q103 and Q104, which switch at a 40 kHz rate, synchronous with the buck regulator. Resistor R116 is used to sense the transformer current. Components R114 and C112 make up a snubber that limits the voltage stress on Q103 and Q104.

Components R101 and CR201 provide take-over power. The take-over power allows the power supply to continue operating after a kick-start interval is completed.

### Output Rectifier Operation

The output at T103 is a square wave with a 50% duty cycle. The output becomes a dc voltage when it is full-wave rectified (no filtering). The voltage waveforms on pin 5 and pin 12 of T103 have a peak amplitude of 5.7 V (11.4 V peak-to-peak) while pin 8 and pin 11 have 18 V (36 V peak-to-peak).

A full-wave doubler formed with components C301, C312, CR301, CR302, CR31 1, and CR312 create the 36 Vdc supply.

### Linear Post Voltage Regulators Operation

The 5 V supply does not use post regulation. Regulation for the 5 V supply is provided by the main buck regulator. All the other supplies use variations of a simple three-terminal regulator. The + 15A, + 15B and the -15 supplies are all fixed regulators, while the +32.5 V and the instrument fan voltages are variable supplies.

The instrument fan relies on thermistor RT301 to sense the air temperature and adjust the output voltage to vary the fan speed. Component CR313 clamps the output to a minimum of 5.75 V to prevent fan stalls at low temperatures. Component CR315 clamps the

maximum output to about 16 V to prevent over-voltage damage to the fan.

### Kick-Start and Bias Power Supply Operation

The kick-starter starts the supply when ac power is first applied to the instrument. There is no other power source for the control circuitry at that time. The kick-starter is powered by a minimal current drawn through R106 and R107.

The kick-starter output is a square wave that is high (about 15 V) for 200 ms of its 2-second period. This output turns Q201 on. Q201 then supplies the current to the control circuitry from TP108. Once the supply has turned on, the take-over supply (refer to "dc-to-dc Converter Operation" above) pulls the source of Q201 high enough to prevent it from being turned on.

Switching thermistor RT202 provides short-circuit protection for the + 12 V power supply. The current flowing through RT202 heats it up. This heating causes rapid resistance increase once the temperature exceeds the switching temperature.

### Buck Regulator Control Operation

The primary function of the buck regulator control is to adjust the duty cycle of Q102 to minimize the error voltage at pin 3 of U203. This function corresponds to regulating the +5_DIGITAL supply to 5.2 V. One feed-forward loop and two feedback loops are required for optimum performance. The inner feedback loop regulates T103 pin 4 voltage to approximately 110 V. The outer loop provides the fine adjustment for accurately setting the +5_DIGITAL. The feed-forward loop reduces the sensitivity of the loop gain to variations in TP108 voltage, which effectively reduces the 120 Hz output ripple by 10 dB.

In addition to providing buck regulation control, this circuitry also provides the following protection features:

Soft Start Circuit Operation

This circuit causes the duty cycle to increase slowly from zero to its regulated level at initial turn on. Without this circuit's operation at power-on, the pulse-width modulator would sense low-power and would increase the duty cycle to its maximum value. Maximizing the duty cycle could cause the +5_DIGITAL to overshoot its operating voltage and start oscillating. This circuit also limits the maximum duty cycle to about 95 % .

Under Voltage Lockout Operation

The power supply turns on when the following condition is satisfied:

$$V_{tp108} =$$

$$5(R201 + R202 + R209a + (R209b||R209c))/(R209b||R209c) = 197\ V$$

The power supply turns off when the following condition is satisfied:

$$V_{tp108} = 5(R201 + R202 + R209a + R209b)/R209b = 154\ V$$

Slow-Start Circuit Operation

The slow-start circuit corrects for a potential power-on problem that can occur when both the line power and temperature are low. When the power supply is cold, the resistances of RT101 and RT102 are high (approximately 59). When the voltage at TP108 reaches 197 V, the supply starts to turn on. The buck regulator starts drawing current from node TP108. When this current flows in the thermistors, TP108 voltage begins to drop. Without the slow- start circuit, the power supply will experience an under-voltage lockout condition.

The voltage at TP108 rises to 197 V again, then the supply tries to start again. The rise and start cycle continues until the thermistors can sufficiently warm up. Occasionally the power supply does not start at all. The slow-start comparator begins to get charged by soft-start capacitor C206 when the following condition is true for the slow-start circuitry:

$$V_{tp108} = 5.31$$
$$(R201 + R202 + R209a + R209b)/R209b = 164\ V$$

Since there is no hysteresis in the slow-start circuitry, the output will oscillate at a rate that causes the duty cycle to regulate TP108 to 164 V. This condition causes a small current to flow through the thermistors, which warms them up. Within a short time they are warm enough and the supply can start.

Over-Current Protection Operation

The current into the center tap of T103 is sensed by measuring the voltage across R116. This circuit limits the total power delivered to the secondaries. It provides the only form of short-circuit protection for the 5 V supply. When the 5 V supply exceeds 0.582 V (about 2.6 amps), the output from U204B is latched high. The pulse-width modulator turns off when U204B is latched high, and the soft-start capacitor is discharged.

As a result, the supply must wait for the next kick-start. At the next kick-start, the supply can try to start again, but it must go through a soft start. If the cause of the over-current

condition is removed (the short is removed), the supply can start at the next kick-start. The supply continues to kick-start indefinitely if the over-current condition remains. Components R212 and C204 provide some of the 80 kHz noise filtering.

Over-Temperature Protection Operation

Switching thermistor RT201 is attached to the same heat sink as Q102. The thermistor's function is to limit power dissipation in the buck transistor. The circuit's function becomes apparent when the power supply is operating without the fan. The thermistor resistance is low until the 100°C switching temperature is reached. At 100°C, the resistance increases rapidly. The pulse-width modulator shuts down when the voltage across the thermistor reaches 0.6 V.

dc to dc Converter Control Operation

The saw-tooth signal used by the pulse-width modulator is compared to a dc level that creates an 80 kHz square wave. The phase of the 80 kHz square wave can be adjusted by changing the dc level. The 80 kHz square-wave pulses toggle the outputs of U204A. U204A outputs drive commutation FETs Q103 and Q104 at a 40 kHz rate. The toggle flip-flop is designed to guarantee that the two FETs both turn on for a brief time. Their duty cycle is just slightly over 50%.

### Feedback Circuit Operation

Components R304 and VR304 form the shunt regulator that provides + 15 V to the secondary circuits. Components R305 and VR305 form the shunt regulator for the -15 V.

Component U305 is a precision +5 V reference. Components U306A, R329, and R330 scale the reference to -9.26 V. Component U306B forces U306 pin 6 to be a virtual ground and causes the following condition to be satisfied:

$$(V_{tp307}/R333) + (-9.26\ V/R331) = 0$$

As a result, Vtp307 is forced to equal 5.2 V. Components C314 and R343 shape the open-loop frequency response. They have a pole at the origin, a zero at 450 Hz, and a higher frequency pole due to the operational amplifier.

Component R315 gets used when network analysis is performed on the control loop.

Components R316 and C321 generate a triangle wave from the 36 V peak-to-peak, 40 kHz signal at T103 pin 12. The RC-time constant is chosen large compared to 1/(40 kHz) such that the waveform looks like a triangle wave rather than an exponential rise and fall wave.

Component U302 compares the triangle wave to the error voltage from U306B. The pulse-width modulator signal that results has a pulse width proportional to the error voltage.

Component U206 is an opto-isolator that passes the pulse-width modulator signal from the secondary to the primary. Components R221 and C210 convert the primary referenced pulse-width modulator signal back to an error signal.

### Power Valid Signal Operation

Power valid sends a signal to the microprocessor about 40 ms after the 5 V digital supply achieves its normal operating voltage, allowing the processor to start. It immediately warns the processor if the power level becomes unacceptable.

Components R318 and R342 form a voltage divider that reduces the 5 V reference to 4.89 V. Combined with C304, they provide some noise filtering.

Components R317 and C319 filter noise and introduce a little delay. Components R317 and R320 add hysteresis. Resistor R321 is a pull-up resistor.

The power-valid circuitry senses that the power level is appropriate when the +5_DIGITAL exceeds 4.98 V. Due to the delay caused by R319 and C320, PWR-VLD goes to TTL high after a 40 ms lapse of time.

PWR-VLD goes low almost immediately after + 5_DIGITAL drops below 4.89 V.

## Power Distribution

Power distribution in the tracking source is managed by the following circuitry:

- Power supplies.
- A9 Modulation Amplifier supplies.
- +24 V supply.
- Low-band power supply.

### Power Supplies

The power supply is the voltage supplier via connector J2. The supplies are filtered and distributed by the controller board circuitry. Table 3-17 identifies the power supplies and their uses.

**Table 3-17. Power Supply Identifications**

| Signals | Uses |
|---|---|
| +5A | Unfiltered + 5 V |
| +15_VA | Unfiltered + 15 V for protection diodes |
| +15_VB | Unfiltered + 15 V to other boards |
| –15V | Unfiltered -15 V for protection diodes and to the other boards |
| +5VA | +5 V to the analog circuitry of the controller board |
| +5LVL | + 5 V to the leveling amplifiers |
| +5FP | +5 V to the front panel |
| +5VL | + 5 V to the digital logic circuitry |
| +32.5VF | +32.5 V to the YTF drive |
| +15VF | + 15 V for the A3 Controller board |
| –15VF | -15 V for the A3 Controller board |

### A9 Modulation Amplifier Supplies

These power supplies are filtered and used to generate the power supplies for the A9 modulation amplifier microcircuit. The +7CB supply is generated by the Ulll regulator and is actually 7.5 V. The 0.5 V difference allows for voltage drop across traces and connectors to the A9 modulation amplifier microcircuit. Diode VR4 is a 12 V zener diode that generates -3 V from the -15 V supply.

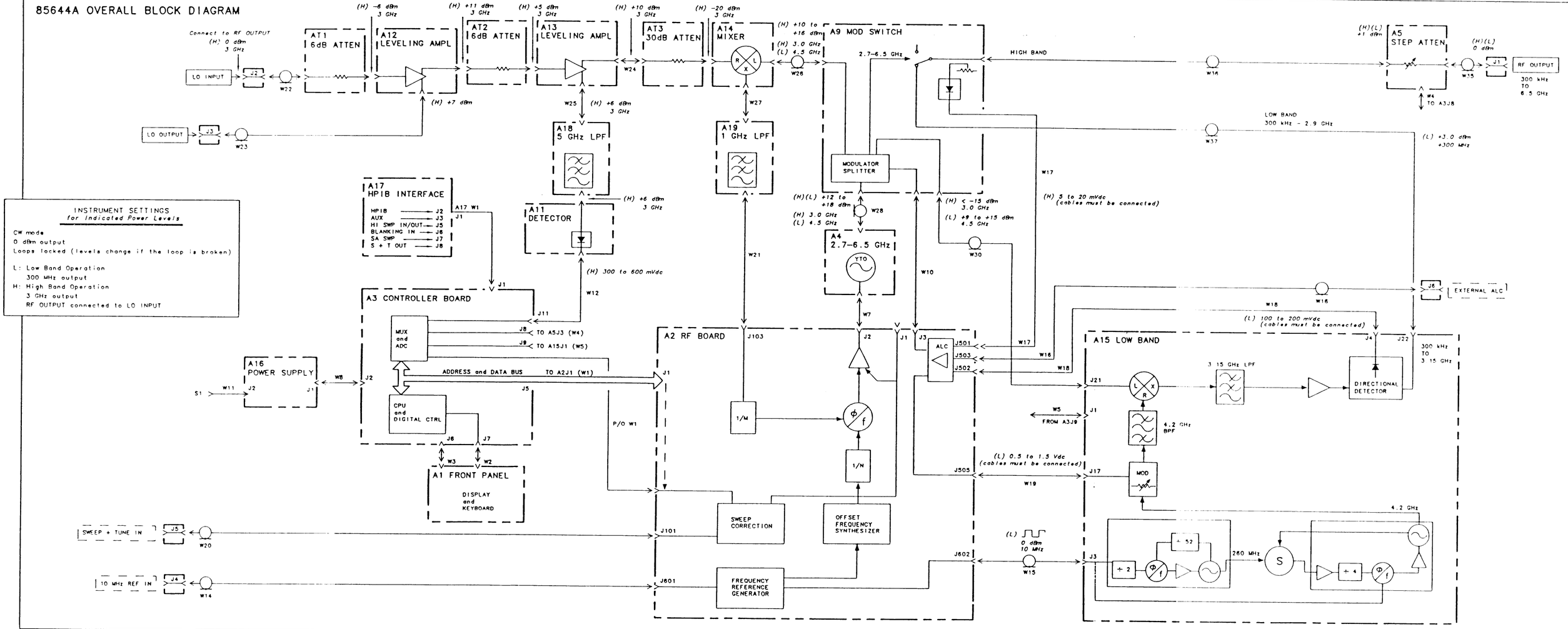
### + 24 V Supply

Regulator U83 generates the +24 V from the +32.5 VF power supply. This voltage is used by the attenuator and the SYTM heater.

### Low Band Power

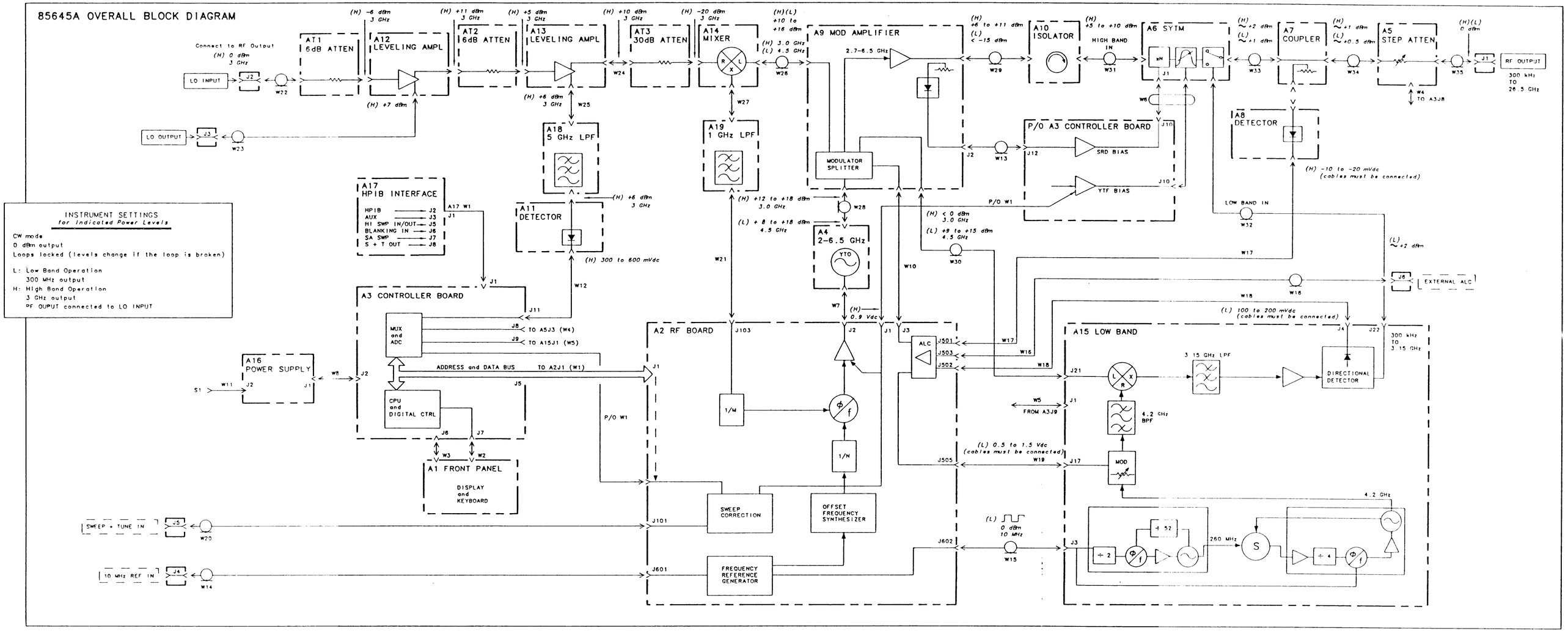
Regulator U95 uses the + 32.5 VF power supply to provide +20 V to the A15 Low Band microcircuit. Switch U46D turns the +20 V supply off, and shuts down low band when it is not in use.

# 85644A OVERALL BLOCK DIAGRAM




SX22

# 85645A OVERALL BLOCK DIAGRAM



# 4

# Test Key Menu Functions

This chapter contains information about the tracking source (TEST) key user menu and service menu functions. The remote command for each function is included in the description, if a remote command is available. The chapter is organized into the following sections:

- (TEST) Key Menu Functions and Related Commands Summary

  This section contains a procedure for accessing either the user menu functions or the service menu functions. A summary table of menu choices includes brief descriptions of the functions and lists the syntax of any related commands

- (TEST) Key Menu Functions and Related Commands Descriptions

  This section is organized numerically. The information describes each user menu and the service menu function. If there is a related remote command for the menu function, its syntax, parameter range and description is provided.

## Summary of (TEST) Key Menu Functions and Related Commands

This section is a reference for the (TEST) key menu functions. The procedure tells you how to enter the menus. Refer to **Table 4-1** or **Table** 4-2 to learn which function to use. The functions are listed numerically.

Whether you choose the menu function or the equivalent command, the resulting function is the same

Refer to Chapter 1, "Making Adjustments" in this manual for related adjustment procedures. Refer to Chapter 8, "Programming Reference," in the ***HP 85644A/HP 85645A Tracking Source Users' Guide*** **for** more information about using the SCPI command language.

## To access the (TEST) key menu functions

There are a total of 29 (TEST) key menu functions available. Use the following procedure to access either the user menu or the service menu. Test menu functions #0 through #3 are user keys. Menu functions #4 through #28 are service menu keys.

- lb access the user menu functions #0 through #3.

  Access the user menu functions by following the procedure below:

  - Press (TEST). User menu functions #0 through #3 are displayed in the display windows
  - •I Press the (MENU UP) and (MENU DOWN) keys to scroll choices #0 through #3.
  - Press (ENTER) to select the item. Refer to each function's description listed numerically in this chapter for information about its operation.

- lb access service menu functions #4 through #28.

  Access the service menu functions by following the steps below:

  - Press the tracking source (TEST) key.
  - Press the (4) key and (GHz) key at the same time. Hold both keys down for a few seconds until the message EXTENDED MENU flashes across the display window.
  - Press the (MENU UP) or (MENU DOWN) keys to scroll through the menu functions.
  - Press the (ENTER) key to select a function. Refer to each item's description listed numerically in this chapter for information about the operation.

## Summary Tables of Menu Choices

Refer to the following tables to learn which function you want to use.

**Table 4-1. User Menu Functions**

| Function Number and Name | Remote Command |
|---|---|
| TEST #0 RECALL ERRORS | SYSTem:ERRor? |
| TEST #1 SELF TEST | DIAGnostic:TEST? |
| TEST #2 TESTPATTERN | DIAGnostic:PATTern TEST |
| TEST #3 TEST HOST MODE | DIAGnostic:THMode\|? |
| | DIAGnostic:THFReq<integer (band number)> <real number (frequency)>\|? |

**Table 4-2. Service Menu Functions**

| Function Number and Name | Remote Command |
|---|---|
| TEST #4 ALC | SOURce:POWer:ALC:STATe ON\|OFF\|1\|0\|? |
| TEST #5 UNLVL PWR | DIAGnostic:ALCCourse <integer> \|?<br>(integer range 0 to 4095) |
| TEST #6 S + T GAIN | DIAGnostic:SWEeptune:GAIN <integer>\|?<br>(integer range 0 to 4095) |
| TEST #7 S + TOFFSTC | DIAGnostic:SWEeptune:COARse <integer>\|?<br>(integer range 0 to 255) |
| TEST #8 S + T OFFSET F | DIAGnostic:SWEeptune:FINe <integer>\|?<br>(integer range 0 to 255) |
| TEST #Q YTO LATCH 1 | DIAGnostic:YTO:LATCh:ONE <integer> \|?<br>(integer range 0 to 255) |
| TEST #10 YTO LATCH 2 | DIAGnostic:YTO:LATCh:TWO <integer>\|?<br>(integer range 0 to 255) |
| TEST #11 DSC THRSH | DIAGnostic:DSCThresh <integer>\|?<br>(integer range 100 to 300) |
| TEST #12 ALC COARSE | DIAGnostic:ALC:COARse <integer> \|?<br>(integer range 0 to 4095) |

**Table 4-2. Service Menu Functions (continued)**

| Function Number and Name | Remote Command |
|---|---|
| **TEST #13** ALC FINE | **DIAGnostic:ALC:FINE** <integer>)?<br>(integer range 0 to 255) |
| TEST **#14** ALC **LATCH1** | **DIAGnostic:ALC:LATCh:ONE** <integer> **\|?**<br>(integer range 0 to 255) |
| **TEST #15** ALC **LATCH2** | **DIAGnostic:ALC:LATCh:TWO <integer>\|?**<br>(integer range 0 **to** 255) |
| **TEST #16** ALC RAMP GN | **DIAGnostic:ALC:RAMPgain** <integer> **\|?**<br>(integer range 0 to 255) |
| **TEST #17 PLL1** DIV | **DIAGnostics:PLL1:DIV** <to be **determined>\|?**<br>**(integer range to )** |
| TEST **#18 PLL1** FRQ | **DIAGnostics:PLL1:FREQ?**<br>(returns a real number) |
| TEST **#19 PLL2** FRQ | **DIAGnostic:PLL2:FREQ?**<br>(returns a real number) |
| TEST **#20 PLL3** DIV | **DIAGnostic:PLL3:DIV?**<br>(returns a real number) |
| **TEST #21 PLL3 FRQ** | **DIAGnostic:PLL3:FREQ?**<br>(returns a real number) |
| **TEST #22 PLL3** OUT DIV | **DIAGnostic:PLL3:OUTDiv?**<br>(returns a integer range to ) |
| **TEST #23** YTO DIV | DIAGnostic:YTO:DIV?<br>**(returns** a real number) |
| **TEST #24** YTO IF | DIAGnostic:YTO:IF?<br>(returns a real number) |
| **TEST #25** ADC VALUE | - - |
| **TEST #26** SYTM VALUE | - - |
| **TEST #27** LOAD ROM DEFAULT | - - |
| **TEST #28 STORE** CAL DATA | **DIAGnostic:STOReе** |

## Description of (TEST) Key Menu Functions

This section describes the menu functions. The functions are listed numerically from #0 to #28. Any remote commands for the function are defined here as well. The remote command's operation is virtually the same as the manual operation.

As indicated with "– –" in Table 4-2, some of the functions do not have remote commands

# TEST #0 RECALL ERRORS

## Function Description

Select this function to identify errors that have occurred. The ERR status indicator lights when there are errors. Press (TEST), then TEST #0, RECALL ERRORS appears in the display windows Press (ENTER) to display the first error number and message. Use the (↑) and (↓) keys to scroll through the list of errors. The message LAST ERROR appears momentarily when you reach the end of the list; FIRST ERROR when you reach the top of the list. Exit this operation by pressing any front-panel key, other than data keys or the (↑) and (↓) keys. Press (PRESET) to clear all errors except the Adjustment function errors.

## Related Command Syntax

SYSTem:ERRor?

Use this query to identify what tracking source errors have occurred. Repeat the command to review each error.

## Command Example

lb retrieve each error message, repeat the following command lines until there are no more errors in the error-queue.

```
OUTPUT703;"SYSTem:ERRor?"      What is the first error in the error queue?
ENTER 703;Error$               Get the first error stored in the error queue.
PRINT "The error is ",Error$"  Print or display the error number and message Delete the error from memory if it is due to remote programming, retain the error in memory if it is hardware related.
```

# TEST #1 SELF TEST

## Function Description

This feature is not implemented for **firmware** revision 910508. (The firmware revision can be read in the tracking source windows when the power is turned on.) When this test is implemented, select it to have the tracking source perform a self-test routine. Press [TEST), then press [MENU DOWN) until TEST #1 , SELF TEST appears in the display windows Press (ENTER) and the self-test process begins. The instrument sets itself to several known states, then checks various points in the circuitry for proper levels of operation. If a point does not meet defined limits, the self-test stops and a message about the failure is displayed. If the self-test passes, the message TEST #1 SELF TEST PASSED is displayed.

## Related Command Syntax

DIAGnostic:TEST?

Use this query to determine the tracking source self-test results. If the query returns the number 0, the self-test passed. If the number 1 is returned, the self-test failed.

## Command Example

```
OUTPUT703;"DIAGnostic:TEST?"     Did the test pass or fail?
ENTER 703;Fail                   Find the test status.
PRINT "If Test fail print 1"     Return 1 if the test has failed.
PRINT Fail                       Print or display the result.
```

# TEST #2 TESTPATTERN

## Function Description

Select this test to verify the operation of most of the front-panel status indicators and the display windows Press (TEST), then press [MENU DOWN] until TEST #2, TESTPATTERN appears in the display windows. Press (ENTER) and the test pattern is displayed. The status indicators labeled RMT, ERR, AC COUPLING, DC COUPLING, and RF OUTPUT ON should all light. If an external 10 MHz reference signal is attached, the EXT reference status indicator should light, otherwise the INT reference status indicator should light.

The UNLVLD and REF INT or **EXT** status-indicator states are not changed during this test.

Exit the test-pattern operation by pressing a key in the AMPLITUDE, FREQUENCY, or INSTRUMENT **STATE** block of the front panel. Pressing the (↑) and (↓) keys, data keys, or any of the keys corresponding with one of the status indicators will not exit the test-pattern.

## Related Command Syntax

DISPlay:TESTpattem TEST

Use this command to initiate the display test-pattern. There are no parameters for this command.

## Command Example

```
OUTPUT 703;"DISPlay:TESTpattern TEST"
```
*Invoke the front-panel test pattern.*

# TEST #3 TEST HOST MODE

## Function Description

Select this function to use an external signal source (such as the HP 8340A synthesized sweeper) as the test host instrument. The HP 8340A synthesized sweeper can be used to exercise the full frequency range of the tracking source.

Press [TEST], then press (MENU DOWN) until TEST #3, TEST HOST MODE appears in the display windows. Press (ENTER). The left-hand display window indicates the number of the band (for example, BAND #0), and the right-hand display window indicates the CW frequency of the band activated.

Use the (↑) and (↓) keys to change the band and display the corresponding tracking source CW frequency. Change the CW frequency setting with the data entry keys, then terminate data entry with the (ENTER) key.

An LO input signal is required as a reference frequency in test-host mode. This frequency must be set 300 MHz below the CW frequency in bands 1 through 4. In band 0, the external reference frequency must be set 3900 MHz above the tracking source CW frequency.

The actual output frequency of the tracking source is phase locked to the external reference frequency with either the 300 MHz or 3900 MHz offset (depending on the band setting). The CW frequency of the tracking source must be set close enough (within about 200 MHz) to the LO input signal frequency. When the CW frequency is within the 200 MHz "window," the tracking source can phase lock to the LO input signal.

'lb set the output frequency (external reference frequency) of the synthesized sweeper, refer to the following formula:

For band 0:

[desired tracking source frequency + 3900 MHz] = synthesized sweeper frequency setting

For bands 1 through 4:

[desired tracking source frequency/band number]
– 300 MHz = synthesized sweeper frequency setting

**Table 4-3.**
**Frequency Ranges and Band Numbers for Test #3, Test Host Mode**

| Band Number | Frequency Range | Synthesized Sweeper Frequency |
|---|---|---|
| 0 | 0.00 to 3100 GHz | 3900 to 7000 MHz |
| 1 | 2000 to 7500 GHz | 1700 to 7200 MHz |
| For HP 85645A Tracking Source Only | | |
| 2 | 4000 to 15000 GHz | 1700 to 7200 MHz |
| 3 | 6000 to 22500 GHz | 1700 to 7200 MHz |
| 4 | 8000 to 26500 GHz | 1700 to 6325 MHz |

## Related Command Syntax

DIAGnostic:THMode 1|0

DIAGnostic:THMode?

DIAGnostic:THFReq (refer to Table 4-3 for frequency information)

DIAGnostic:THFReq?

Use the THMode command to initiate the test-host mode. Follow with the THFReq command to set the frequency of interest. The frequency setting depends upon the tracking source band number.

Use the THMode query to retrieve the current test-host mode state. Use the THFReq query to determine the band number and frequency setting of the test host instrument (LO signal source frequency).

## Command Example

```
OUTPUT703;"DIAGnostic:THMode"
```
*Place the tracking source in test host mode.*

```
OUTPUT 703;"DIAGnostic:THFReq 0 1.25 GHZ;"
```
*Select tracking source band 0, and set the frequency to 1.25 GHz.*

```
OUTPUT703;"DIAGnostic:THMode?"
```
*What is the current test-host mode setting?*

```
ENTER 703;Thost
```
*Find the current test-host mode setting.*

```
PRINT  "The Test Host mode is ",
       Thost;BOOLEAN
```
*Print or display a 1 if test host mode is on; a 0 if it is off.*

```
OUTPUT703;"DIAGnostic:THFReq?;"
```
*What are the current test-host mode band number and frequency settings?*

```
ENTER 703;Band,Freq
```
*Get the band number and frequency setting.*

```
PRINT  "The test host band is ",Band,
       "and frequency is ",Freq
```
*Print or display the band number and frequency settings.*

# TEST #4 ALC

**Function Description** Select this function to enable or disable the ALC-loop state in the tracking source. During normal operation, the ALC loop is locked. In the disabled state, the ALC loop is actually opened. As a result, the path for the feedback voltage that corrects the output power level is interrupted.

## Related Command Syntax

SOURce:POWer:ALC:STATe ON|OFF|1|0

SOURce:POWer:ALC:STATe?

Use this command to enable (1 or ON) or disable (0 or OFF) the ALC loop state. In the enabled mode, the ALC loop is closed and functioning. In the disabled mode, the ALC loop is opened and the feedback voltage path is interrupted.

Use the query to determine whether the ALC loop is enabled or disabled.

## Command Syntax

```
OUTPUT 703;"SOURce:POWer:ALC:STATe OFF"
```
*Turn the ALC loop function off. The optional command [:STATe] is included.*

```
OUTPUT 703;"SOURce:POWer:ALC:STATe?"
```
*what is the current ALC loop state, on or off?*

```
ENTER 703;Alcstate
```
*Get the current ALC loop function state*

```
PRINT "The ALC state is set to ",Alcstate
```
*A Boolean 1 is returned if the ALC loop state is activated and a 0 if it is deactivated.*

# TEST #5 UNLVL PWR

## Function Description

Select this function to set the ALC coarse DAC with the ALC loop open. When you select this function, the band is locked to the current band number. The current band number is the point on the trace where the sweep is when the key is pressed. If a different band is desired, select it with adjust function ADJ . #4 BAND LOCK under the (ADJUST) key. The ALC loop is disabled (open) and the ALC DAC number is displayed. The output power can then be changed manually. Using this function is equivalent to combining test function #4 ALC with test function #12 ALC COARSE. For power control with finer resolution, use test function TEST #13 ALC FINE under the (TEST) key, after activating TEST #5 UNLVL PWR.

## Related Command Syntax

DIAGnostic:ALC:COURse <integer>
(integer range 0 to 4095)

DIAGnostic:ALC:COURse?

Use this command to access and set the ALC coarse DAC when the ALC loop is open. The ALC loop must first be opened, or disabled, with the SOURce:POWer:ALC:STATe command, defined in test function #4 ALC.

Use the query to retrieve the current ALC coarse DAC setting.

## Command Example

```
OUTPUT 703;"SOURce:POWer:ALC:STATe OFF"
```
*Turn the ALC loop function off. The optional command [:STATe] is included.*

```
OUTPUT 703;"DIAGnostic:ALC:COURse 1024"
```
*Set the ALC coarse DAC to 1024.*

```
OUTPUT 703;"SOURce:POWer:ALC:STATe?"
```
*Return the current ALC on or off state.*

```
ENTER 703;Alcstate
```
*Get the ALC state.*

```
PRINT "The ALC state is set to ",Alcstate
```
*The value returned is Boolean 1 for on, or 0 for off.*

```
OUTPUT 703;"DIAGnostic:ALC:COURse?"
```
*What is the ALC warse DAC setting?*

```
ENTER 703;Alcc
```
*Get the DAC setting.*

```
PRINT "The ALC coarse DAC setting is ",Alcc
```
*Print or display the current ALC warse DAC setting.*

# TEST #6 S+T GAIN

**Function Description** Select this function to either monitor or change the sweep + tune gain DAC. When you select this function, the band is locked to the current band number. The current band number is the point on the trace where the sweep is when the key is pressed.

## Related Command Syntax

DIAGnostic:SWEeptune:GAIN <integer>
(integer range 0 to 255)

DIAGnostic:SWEeptune:GAIN?

Use this command to monitor the current sweep + tune gain DAC setting.

Use the query to retrieve the gain DAC setting.

## Command Example

```
OUTPUT703;"DIAGnostic:SWEeptune:GAIN126;"
```
*Set the sweep + tune gain DAC to 126.*

```
OUTPUT703;"DIAGnostic:SWEeptune:GAIN?"
```
*What is the current setting of the sweep + tune gain DAC?*

```
ENTER 703;Stg
```
*Get the current sweep + tune gain DAC setting.*

```
PRINT "The sweep + tune gain DAC setting is ",Stg
```
Print or *display the current DAC setting.*

# TEST #7 S+T OFFST C

## Function Description

Select this function to either monitor or set the current sweep + tune coarse offset DAC. When you select this function, the band is locked to the current band number. The current band number is the point on the trace where the sweep is when the key is pressed. After the band-lock function is complete, the ALC loop is opened. When the current DAC value is displayed you can either monitor or change the DAC value.

## Related Command Syntax

DIAGnostic:SWEeptune:COARse <integer>
(integer range 0 to 255)

DIAGnostic:SWEeptune:COARse?

Use this command to set the current sweep + tune coarse adjust DAC value.

Use the query to monitor the current DAC setting.

## Command Example

```
OUTPUT703;"DIAGnostic:SWEeptune:COARse126;"
```
*Set the sweep + tune warse-adjust DAC to 126.*

```
OUTPUT703;"DIAGnostic:SWEeptune:COARse?"
```
*What is the current setting of the sweep + tune coarse-adjust DAC?*

```
ENTER 703;Stoc
```
*Get the current sweep + tune warse DAC setting.*

```
PRINT "The sweep + tune coarse-adjust
       DAC setting is ",Stoc
```
*Print or display the current DAC setting.*

## TEST #8 S+T OFFSET F

**Function Description** Select this function to either monitor or set the sweep + tune fine offset DAC. When you select this function, the band is locked to the current band number. The current band number is the point on the trace where the sweep is when the key is pressed. When the current DAC value is displayed you can either monitor or change the DAC value.

### Related Command Syntax

**DIAGnostic:SWEeptune:FINe** <integer>
(integer range 0 to 255)

**DIAGnostic:SWEeptune:FINe?**

Use this command to set the sweep + tune fine-adjust DAC value.

Use the query to monitor the current DAC setting.

### Command Example

```
OUTPUT 703;"DIAGnostic:SWEeptune:FINe 126;"
```
*Set the sweep + tune fine-adjust DAC to 126.*

```
OUTPUT703;"DIAGnostic:SWEeptune:FINe?"
```
*What is the current setting of the sweep + tune fine-adjust DAC?*

```
ENTER 703;Stof
```
*Get the current sweep + tune fine-adjust DAC setting.*

```
PRINT "The sweep + tune fine-adjust
       DAC setting is ",Stof
```
*Print or display the current DAC setting.*

# TEST #9 YTO LATCH 1

## Function Description

Select this function to either monitor or set YTO latch 1. When you select this function, the band is locked to the current band number.

The current band number is the point on the trace where the sweep is when the key is pressed. YTO latch 1 is an 8-bit latch containing several YTO-state settings Refer to Table 4-4 for the states

By selecting #9 YTO LATCH 1, you can measure latch output values and compare them with its function. Refer to the schematic diagram for output values.

**Table 4-4. Bit States**

| State of DO and D1 | Band Number | Harmonic Number |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 2 | 2 |
| 2 | 3 | 3 |
| 3 | 4 | 4 |

Bits DO and D1 indicate YTO harmonics numbers

Bits D2 and D3 equal 0 during a no-search state

Bit D2 should equal 1 when searching up

Bit D3 should equal 1 when searching down

Bit D4 equals 1 for CW mode

Bit D7 equals 1 for CW mode

## Warning

**Do not set bits D2 and D3 at the same time. Setting bits D2 and D3 at the same time may result in instrument damage.**

## Related Command Syntax

DIAGnostic:YTO:LATCh:ONE <integer>
(integer range 0 to 255)

DIAGnostic:YTO:LATCh:ONE?

Use this command to set the values of YTO latch 1.

Use the query to monitor the current DAC setting of YTO latch 1.

## Command Example

```
OUTPUT 703;"DIAGnostic:YTO:LATCH:ONE 126;"
OUTPUT 703;"DIAGnostic:YTO:LATCh:ONE?"

ENTER 703;Yto1

PRINT "The current YTO latch 1
       setting is ",Yto1
```

*Set YTO latch 1 to 126.*

*what is the current setting of YTO latch 1?*

*Get the current YTO latch 1 setting.*

*Print or display the current YTO latch 1 setting.*

# TEST #10 YTO LATCH 2

## Function Description

Select this function to either monitor or set YTO latch 2. When you select this function, the band is locked to the current band number. The current band number is the point on the trace where the sweep is when the key is pressed. YTO latch 2 is an 8-bit latch containing several YTO-state settings By selecting #10 YTO LATCH 2, you can measure latch output values and compare them with its function. Refer to the schematic diagram for output values,

## Related Command Syntax

DIAGnostic:YTO:LATCh:TWO <integer>
(integer range 0 to 255)

DIAGnostic:YTO:LATCh:TWO?

Use this command to set the values of YTO latch 2.

Use the query to monitor the current DAC setting of YTO latch 2.

## Command Example

```
OUTPUT 703;"DIAGnostic:YTO:LATCH:TWO 126;"
OUTPUT 703;"DIAGnostic:YTO:LATCh:TWO?"

ENTER 703;Yto2

PRINT "The current YTO latch 2
       setting is ",Yto2
```

*Set YTO latch 2 to 126.*

*What is the current setting of YTCJ latch 2'*

*Get the current YTO latch 2 setting.*

*Print or display the current YTO latch 2 setting.*

## TEST #11 DSC THRSH

### Function Description

Select this function to either monitor or set the discriminator threshold value This value is initially set at the factory and used to determine the frequency band of the host instrument. The factory setting is determined by the adjust function ADJ . **#6** LEVEL AMP 2 routine.

If you change the default setting, then save it, the new setting is the default value. The new default value is not changed by any adjustment procedures or calibration routine.

The threshold value is used to differentiate between the lower and upper part of a frequency band. Once the band position is determined, the information is combined with the sweep + tune voltage to determine which host instrument frequency band the tracking source is to track.

### Related Command Syntax

DIAGnostic:DSCThresh <integer>
(integer number range is 100 to 300)

DIAGnostic:DSCThresh?

Use this command to set the discriminator threshold value. The factory default setting is 200.

Use the query to monitor the current discriminator threshold setting.

### Command Example

```
OUTPUT 703;"DIAGnostic:DSCThresh 220;"
```
*Set the discriminator threshotd to 220.*

```
OUTPUT703;"DIAGnostic:DSCThresh?"
```
*What is the current setting of the discriminator threshold?*

```
ENTER 703;Dsc
```
*Get the current discriminator threshold setting.*

```
PRINT "The current discriminator
       threshold setting is ",Dsc
```
*Print or display the current discriminator threshold setting.*

# TEST #12 ALC COARSE

## Function Description

Select this function to either monitor or set the ALC coarse DAC value. When you select this function, the band is locked to the current value. The current band number is the point on the trace where the sweep is when the key is pressed.

The ALC loop remains closed while this function is activated. The values you enter control the ALC DACs and change the output power in coarse steps.

## Related Command Syntax

DIAGnostic:ALC:COARse <integer>
(integer range is 0 to 4095)

DIAGnostic:ALC:COARse?

Use this command to access the ALC DAC and enter values to change the DAC setting. The values provide large-change control of the tracking source's output power.

Use the query to determine the current ALC coarse DAC setting.

## Command Example

```
OUTPUT 703;"DIAGnostic:ALC:COARse 1024;"
OUTPUT703;"DIAGnostic:ALC:COARse?"

ENTER 703;Alcc

PRINT "The current ALC coarse DAC
       setting is ",Alcc
```

*Set the ALC coarse DAC to 1024.*
*What is the current setting of the ALC warse DAC?*
*Get the current ALC warse DAC setting.*
*Print or display the current setting of the ALC warse DAC.*

# TEST #13 ALC FINE

## Function Description

Select this function to monitor or change the ALC fine DAC values. When you select this function, the band is locked to the current band number. The current band number is the point on the trace where the sweep is when the key is pressed.

The ALC loop remains locked while this function is activated. The values you enter control the ALC **DACs** and change the output power in fine steps.

## Related Command Syntax

**DIAGnostic:ALC:FINe** <integer>
(integer range is 0 to 255)

**DIAGnostic:ALC:FINe?**

Use this command to access the ALC DAC and enter values to change the DAC setting. The values provide small-change control of the tracking source's output power.

Use the query to retrieve the current ALC fine DAC setting.

## Command Example

```
OUTPUT 703;"DIAGnostic:ALC:FINe 126;"
OUTPUT703;"DIAGnostic:ALC:FINe?"

ENTER 703;Alcf

PRINT "The current ALC fine DAC setting is ",Alcf
```

***Set the ALC fine DAC to 126.***

***What is the current setting** of **the ALC fine DAC?***

***Get the current ALC fine DAC setting.***

***Print or display the current setting** of the **ALC fine DAC.***

# TEST #14 ALC LATCH1

## Function Description

Select this function to either monitor or set ALC latch 1. When you select this function, the band is locked to the current band number. The current band number is the point on the trace where the sweep is when the key is pressed. ALC latch 1 is an 8-bit latch containing several ALC-state settings. By selecting #14 ALC LATCH1, you can measure latch output values and compare them with its function. Refer to the schematic diagrams for output values.

## Related Command Syntax

DIAGnostic:ALC:LATCh:ONE <integer>
(integer range 0 to 255)

DIAGnostic:ALC:LATCh:ONE?

Use this command to set the values of ALC latch 1.

Use the query to monitor the current ALC latch 1 setting.

## Command Example

```
OUTPUT 703;"DIAGnostic:ALC:LATCh:ONE 104;"      Set ALC latch 1 to 104.
OUTPUT703;"DIAGnostic:ALC:LATCh:ONE?"           What is the current setting of
                                                ALC latch l?
ENTER 703;Alcl1                                 Get the current setting of ALC
                                                latch 1.
PRINT "The current ALC latch 1 setting is ",Alcl1   Print or display the current
                                                setting of ALC latch 1.
```

## TEST #15 ALC LATCH2

**Function Description**

Select this function to either monitor or set ALC latch 2. When you select this function, the band is locked to the current band number. The current band number is the point on the trace where the sweep is when the key is pressed. ALC latch 2 is an 8-bit latch containing several ALC-state settings By selecting #15 ALC LATCH2, you can measure latch output values and compare them with its function. Refer to the schematic diagram for the output values.

### Related Command Syntax

DIAGnostic:ALC:LATCh:TWO <integer>
(integer range 0 to 255)

DIAGnostic:ALC:LATCh:TWO?

Use this command to set the values of ALC latch 2.

Use the query to monitor the current ALC latch 2 setting.

### Command Example

```
OUTPUT 703;"DIAGnostic:ALC:LATCh:TWO 124;"
OUTPUT 703;"DIAGnostic:ALC:LATCh:TWO?"

ENTER 703;Alc12

PRINT "The current ALC latch
       2 setting is ",Alc12
```

*Set ALC latch 2 to 124.*

*What is the current setting of ALC latch 2?*

*Get the current setting of ALC latch 1.*

*Print or display the current setting of ALC latch 2.*

# TEST #16 ALC RAMP GN

## Function Description

Select this function to either monitor or set the ALC ramp-gain DAC. When you select this function, the band is locked to the current value **The** current band number is the point on the trace where the sweep is when the key is pressed.

The values stored in this DAC control the power-sweep operation. The settings alter the ramp input to the ALC loop that generates the power-sweep output. These DAC values do not alter the power-slope settings. Adjust the power-slope values via the front-panel AUX menu.

## Related Command Syntax

DIAGnostic:ALC:RAMPgain <integer>
(integer range is 0 to 255)

DIAGnostic:ALC:RAMPgain?

Use this command to set the ALC ramp-gain DAC. The values entered control the tracking source's power-sweep operation.

Use the query to monitor the current ALC ramp-gain DAC setting.

## Command Example

```
OUTPUT 703;"DIAGnostic:ALC:RAMPgain 104;"
```
***Set the ALC ramp-gain latch 104.***

```
OUTPUT703;"DIAGnostic:ALC:RAMPgain?"
```
***What is the current setting of the ALC ramp-gain latch?***

```
ENTER 703;Alcrg
```
***Get the current setting of the ALC ramp-gain latch.***

```
PRINT "The current ALC ramp-gain
      latch setting is ",Alcrg
```
***Print or display the current setting of ALC ramp-gain latch.***

# TEST #17 PLL1 DIV

**Function Description** Select this function to monitor the divide value of phase lock loop 1.

## Related Command Syntax

**DIAGnostic:PLL1:DIV?**

Use this query to monitor the divide value used in phase lock loop 1.

## Command Example

```
OUTPUT703;"DIAGnostic:PLL1:DIV?"      What is the current phase-lock
                                      loop 1 divide number?
ENTER 703;Pll1div                     Get the current phase-lock loop
                                      1 divide number.
PRINT "The current phase-lock loop 1  Print or display the current
      divide number is ",Pll1div      phase-lock loop 1 divide number.
```

# TEST #18 PLL1 FRQ

**Function Description** Select this function to monitor the frequency value of phase lock loop 1.

## Related Command Syntax

**DIAGnostic:PLL1:FREQuency?**

Use this query to monitor the frequency value of phase lock loop 1.

## Command Example

```
OUTPUT703;"DIAGnostic:PLL1:FREQuency?"      What is the current phase-lock
                                            loop 1 frequency value?
ENTER 703;Pll1f                             Get the current phase-lock loop
                                            1 frequency value.
PRINT "The current phase-lock loop 1        Print or display the current
       frequency value is ",Pll1f           phase-lock loop 1 frequency value.
```

## TEST #19 PLL2 FRQ

**Function Description** Select this function to monitor the frequency value of phase lock loop 2. The frequency you monitor here should match the frequency at the connector labeled **PLL2** TEST on **A3** RF board assembly.

### Related Command Syntax

DIAGnostic:PLL2:FREQuency?

Use this query to monitor the frequency value of phase lock loop 2.

### Command Example

```
OUTPUT703;"DIAGnostic:PLL2:FREQuency?"
ENTER 703;P112f
PRINT "The current phase-lock loop 2
      frequency value is ",P112f
```

*What is the current phase-lock loop 2 frequency value?*

*Get the current phase-lock loop 2 frequency value.*

*Print or display the current phase-lock loop 2 frequency value*

# TEST #20 PLL3 DIV

**Function Description** Select this function to monitor the divide value of phase lock loop 3.

## Related Command Syntax

DIAGnostic:PLL3:DIV?

Use this query to monitor the divide value of phase lock loop 3.

## Command Example

```
OUTPUT 703;"DIAGnostic:PLL2:DIV?"      What is the current phase-lock
                                       loop 2 divide number?
ENTER 703;Pll2div                      Get the current phase-lock loop
                                       2 divide number.
PRINT "The current phase-lock loop 2   Print or display the current
      divide number is ",Pll2div       phase-lock loop 2 divide number.
```

# TEST #21 PLL3 FRQ

**Function Description** Select this function to monitor the frequency value of phase lock loop *3.*

## Related Command Syntax

**DIAGnostic:PLL3:FREQuency?**

Use this query to monitor the frequency value of phase lock loop 3. The frequency you monitor here should match the frequency at the connector labeled **PLL3** TEST on **A3** RF board assembly.

## Command Example

```
OUTPUT703;"DIAGnostic:PLL3:FREQuency?"
ENTER 703;Pll3f
PRINT "The current phase-lock loop 3
      frequency value is ",Pll3f
```

*What is the current phase-lock loop 3 frequency value?*

*Get the current phase-lock loop 3 frequency value.*

*Print or display the current phase-lock loop 3 frequency value*

# TEST #22 PLL3 OUT DIV

**Function Description** Select this function to monitor phase lock loop 3 output divider value.

## Related Command Syntax

**DIAGnostic:PLL3:OUTDiv?**

Use this query to monitor the output divider value of phase lock loop 3.

## Command Example

```
OUTPUT 703;"DIAGnostic:PLL3:OUTDiv?"
What is the current phase-lock loop 3 output divide value?
ENTER 703;Pll3od
Get the current phase-lock loop 3 output divide value.
PRINT "The current phase-lock loop 3 output divide value is
",Pll3od
Print or display the current phase-lock loop 3 output divide value.
```

# TEST #23 YTO DIV

**Function Description** Select this function to monitor the YTO divide value.

## Related Command Syntax

DIAGnostic:YTO:DIV?

Use this query to monitor the YTO divide value.

## Command Example

```
OUTPUT 703;"DIAGnostic:YTO:DIV?"      What is the current YTO divide value?
ENTER 703;Ytodiv                      Get the current YTO divide value.
PRINT "The current YTO divide value   Print or display the current YTO divide value.
      is ",Ytodiv
```

# TEST #24 YTO IF

**Function Description** Select this function to monitor the YTO IF frequency.

## Related Command Syntax

DIAGnostic:YTO:IF?

Use this query to monitor the **YTO** IF frequency value.

## Command Example

```
OUTPUT 703;"DIAGnostic:YTO:IF?"          What is the current setting of the YTO IF?
ENTER 703;Ytoif                          Get the current YTO IF setting.
PRINT "The current YTO IF setting is ",Ytoif   Print or display the current YTO IF value.
```

## TEST #25 ADC VALUE

### Function Description

Select this function to monitor, in real time, the voltage on any line of any main diagnostic MUX. The tracking source uses six different **8-bit MUXes** for general instrument operation. Through the ADC, any one of the 48 different diagnostic signals can be monitored in real time. These signals are identified in Table 4-5.

Select which MUX line to monitor with the ⇧ and ⇩ keys. The first digit of the MUX number represents the MUX that is selected. The second digit indicates which diagnostic signal line on the MUX is selected. Single digit MUX number corresponds to the main ADC MUX. Once you have selected the MUX line, the real-time voltage appears in the tracking source's display windows

### Related Command Syntax

There is no remote command for this function.

**Table 4-5. Definitions of ADC Line Values**

| MUX Reference Designator | MUX Line Number | Line Definition | Pin Number |
|---|---|---|---|
| A2U42 | #0 | UNCOR SWP + T | 4 |
| | 1 | RF DIAG | 5 |
| | 2 | OPT DIAG (not connected) | 6 |
| | 3 | SYTM DIAG | 7 |
| | 4 | GND | 12 |
| | 6 | DISCRIMINATOR | 11 |
| | 6 | SW-DIAG | 10 |
| | 7 | REF_VOLTAGE | 9 |
| A3U18 | #10 | D-S-T-SIGN | 4 |
| | 11 | D-S-TABS | 5 |
| | 12 | D_YTO_SUM | 6 |
| | 13 | D-YTO-BAND | 7 |
| | 14 | D_YTO_SENSE | 12 |
| | 15 | D_YTO_ERR | 11 |
| | 16 | (not connected) | 10 |
| | 17 | D_YTO_UNLOCK | 9 |
| A3U19 | #20 | D_SA_SWP | 4 |
| | 21 | D_YTO_OFFS_C | 6 |
| | 22 | D_YTO_OFFS_F | 6 |
| | 23 | D_YTO_FM_DVR | 7 |
| | 24 | D_YTO_RF_10V_REF | 12 |
| | 25 | D_YTO_IF_INT | 11 |
| | 26 | D-YTO-IF SRC | 10 |
| | 27 | RF-BD-REV | 9 |
| A3U514 | #30 | D_ALC_PREAMP | 4 |
| | 31 | D_ALC_ABS | 5 |
| | 32 | D_ALC_LOGAMP | 6 |
| | 33 | D_ALC_INTGR | 7 |
| | 34 | D_ALC_LVL_C | 12 |
| | 35 | D_ALC_LVL_F | 11 |
| | 36 | D-LACRAMP | 10 |
| | 37 | D_YTO_LVL | 9 |

**Table 4-5.**
**Definitions of ADC Line Values (continued)**

| MUX Reference Designator | MUX Line Number | Line Definition | Pin Number |
|---|---|---|---|
| A3U922 | #40 | D_PLL1_INTGR | 4 |
| | 41 | D_PLL1_LPF | 5 |
| | 42 | D_PLL2_INTGR | 6 |
| | 43 | D_PLL2_SRCH | 7 |
| | 44 | D_PLL3_INTGR | 12 |
| | 46 | D_PLL3_SRCH | 11 |
| | 46 | GND | 10 |
| | 47 | D_10MHZ_INT | 9 |

# TEST #26 SYTM VALUE

## Function Description

Select this function to monitor, in real time, the voltage on any line of any SYTM diagnostic MUX. The tracking source uses three different **8-bit MUXes** for SYTM operation. Through the ADC, any one of the 24 different SYTM signals can be monitored in real time. These signals are identified in Table 4-6.

Select which MUX line to monitor with the ⇧ and ⇩ keys. The first digit of the number represents the number of the MUX that is selected. The second digit indicates which diagnostic signal line on the MUX is selected. With single digit MUX numbers, the first number is assumed to be 0 (MUX **#01,** 02, 03, and so on). Once you have selected the MUX line, the real time voltage appears in the tracking source's display windows

## Related Command Syntax

There is no remote command for this function.

**Table 4-6. Definitions of SYTM Line Values**

| MUX Reference Designator | SYTM MUX Number | Line Definition | Pin Number |
|---|---|---|---|
| A2U86 | #0 | YTF_DIAG7 | 4 |
| | 1 | YTF_DIAG1 | 5 |
| | 2 | YTF_DIAG2 | 6 |
| | 3 | YTF_DIAG3 | 7 |
| | 4 | YTF_DIAG4 | 12 |
| | 5 | YTF_DIAG5 | 11 |
| | 6 | YTF_DIAG6 | 10 |
| | 7 | RAMP-DIAG | 9 |
| A2U87 | #10 | BIAS_DIAG1 | 4 |
| | 11 | BIAS-DIAGS | 5 |
| | 12 | BIAS-DIAGS | 6 |
| | 13 | BIAS_DIAG4 | 7 |
| | 14 | BIAS-DIAGS | 12 |
| | 15 | +7V_DIAG | 11 |
| | 16 | 260MHZ LOCK | 10 |
| | 17 | 4.2MHZ LOCK | 9 |
| A2U93 | #20 | BIAS_DIAG6 | 4 |
| | 21 | 24V_DIAG | 5 |
| | 22 | LB_PWR_SPLY | 6 |
| | 23 | LVL_AMP_1 | 7 |
| | 24 | LVL_AMP_2 | 12 |
| | 25 | XL-AMP-DACS | 11 |
| | 26 | CNTL_BD_REV | 10 |
| | 27 | -3V_DIAG | 9 |

# TEST #27 LOAD ROM DEFAULT

**Function Description** Select this function to load the factory default calibration values from ROM into the active RAM memory. The active RAM values are lost when the instrument's power is turned off.

## Related Command Syntax

There is no remote command for this function.

# TEST #28 STORE CAL DATA

**Function Description** Select this function to store the calibration values which are currently stored in RAM to EEPROM memory. Storing these values in EEPROM changes the checksum values The new checksum values are checked when the instrument's power is turned on.

## Related Command Syntax

DIAGnostic:STOReе

Use this command to store calibration data to the instrument EEPROM.

## Command Example

```
OUTPUT 703;"DIAGnostic:STOReе"
```

***Save the calibration values in the instrument EEROM.***

# 5

# Adjust Key Menu Functions

This chapter contains information about the tracking source (ADJUST) key user menu and service menu functions. The remote command for each function is included in the description, if a remote command is available. The chapter is organized into the following sections:

- (ADJUST) Key Menu Functions and Related Commands Summary

  This section contains a procedure for accessing either the user menu functions or the service menu functions. A summary table of menu choices includes brief descriptions of the functions and lists the syntax of any related remote command.

- (ADJUST) Key Menu Functions and Related Commands Descriptions

  This section is organized numerically. The information describes each of the menu functions. If there is a remote command for the menu function, its syntax, parameter range, and description is provided.

## Summary of (ADJUST) Key Menu Functions and Related Commands

This section is a reference for the (ADJUST) key menu functions. The procedure tells you how to enter the menus. Refer to Table 5-1 or Table 5-2 to learn which function you need. The functions are listed numerically.

Whether you choose the menu function or the equivalent remote command, the resulting function is the same.

Refer to Chapter 1, "Making Adjustments," in this manual for related adjustment procedures, and to Chapter 8, "Programming Reference," in the ***HP 85644A/HP 85645A Tracking Source Users Guide*** for information about using the SCPI command language.

## To access the adjustment menu functions

There are a total of 27 (ADJUST) key menu functions available. Use the following procedure to access either the user menu or the service menu. Menu items #0 through #3 are user keys. Menu items #4 through #26 are service menu functions.

- To access the user menu functions #0 through #3.

  Access the user menu functions by following the steps below:

  - Press (ADJUST). User menu functions #0 through #3 are displayed in the display windows
  - Press the (MENU UP) and (MENU DOWN) keys to scroll choices #0 through #3.
  - Press (ENTER) to select the item. Refer to each function's description listed numerically in this chapter for information about its operation.

- lb access the (ADJUST) key menu functions #4 through #26.

  Access service menu functions #4 through #26 by following the steps below:

  - Press the (ADJUST) key.
  - Press the (7) key and the (GHz) key at the same time. Hold both keys down for a few seconds until the message EXTENDED MENU flashes across the display window.
  - Press (MENU UP) or (MENU DOWN) to scroll through the adjustment menu functions.
  - Press the (ENTER) key to select a function.

## Summary Tables of Menu Choices

Refer to the following tables to learn which function you want to use.

**Table 5-1. User Menu Functions**

| Function Number and Name | Remote Command | Related Procedure |
|---|---|---|
| #0 DISP INTENSITY | DISPlay:BRIGhtness <real> \| ? (real number range 0.0 to 1.0) | |
| #1 AMPLITUDE PEAK | CALIbration:PEAKing | -- |
| #2 ALC EXT DETECTOR | not implemented yet | |
| #3 SWP + TUNE ADJ | CALibration:SWEeptune:ADJust, followed with CALibration:SWEeptune:EXECute | CALibration:SWEep:SETTing |

**Table 5-2. Service Menu Functions**

| Function Number and Name | Remote Command | Related Procedure |
|---|---|---|
| #4 BAND LOCK | DIAGnostic:BNDLock <integer>\| UP\|DOWN\|? [integer range 0 to 4) | -- |
| #5 LEVEL AMP 1 | DIAGnostic:LEVelamp:FIRSt<integer> \|? [integer range 0 to 255) | |
| #6 LEVEL AMP 2 | DIAGnostic:LEVelamp:SECond | -- |
| #7 SLOPE LO BAND | CALibration:POWer:SLOPe:LOWBand <real number>\|UP\|DOWN\|? | CALibration:ALC:LOWBand |
| #8 ALC LO BAND | CALibration:ALC:LOWBand, followed with CALibration:ALC:POWer <real number>dBm | -- |
| #Q SLOPE HI BAND | CALibration:POWer:SLOPe:HIGHband UP\|DOWN\|? | CALibration:ALC:HIGHband |
| #10 ALC HI BAND | CALibration:ALC:HIGHband or CALibration:ALC:EXTernal, followed with CALibration:ALC:POWer <real number>dBm | - - |
| #11 CW ACCURACY | CALibration:FREQuency:ADJ, followed with CALibration:FREQuency[:CW] <real number> <frequency unit> \|? [real number range for HP 85644A is 0 Hz to 6.5 GHz, for HP 85645A it is 0 Hz to 26.5 GHz) | -- |
| #12 INT REFERENCE | CALibration:REFerence:ADJ, followed with CALibration:REFerence[:OFFSet] <real number><frequency unit> (real number range for HP 85644A is 0 Hz to 6.5 GHz, for HP 85645A it is 0 Hz to 26.5 GHz) | -- |
| #13 YTM GAIN | DIAGnostic:YTM:GAIN<integer>\|? [integer range 0 to 255) | -- |
| #14 YTM OFFSET | DIAGnostic:YTM:OFFSet <integer>\|? [integer range 0 to 255) | -- |
| #15 YTM BP1 | DIAGnostic:YTM:BREakpoint:ONE <integer>\| ? [integer range 0 to 255) | -- |

**Table 5-2. Service Menu Functions (continued)**

| Function Number and Name | Remote Command | Related Procedure |
|---|---|---|
| #16 YTM BP2 | DIAGnostic:YTM:BREakpoint:TWO <integer>\|? (integer range 0 to 255) | - - |
| ;617 YTM BP3 | DIAGnostic:YTM:BREakpoint:THRee <integer>\|? (integer range 0 to 255) | - - |
| #18 YTM BP4 | DIAGnostic:YTM:BREakpoint:FOUR <integer>\|? (integer range 0 to 255) | - - |
| #19 YTM BP4 FRQ | DIAGnostic:YTM:BP4Freq <integer> \|? (integer range 0 to 255) | - - |
| #20 YTM DELAY | DIAGnostic:YTF:DELay <integer> \|? (integer range 0 to 255) | - - |
| #21 YTM BIAS PWR LVL | DIAGnostic:BIAS:PWRLvl | - - |
| #22 YTM BIAS OFS | DIAGnostic:BIAS:OFFSet <integer> \|? (integer range 0 to 255) | - - |
| #23 YTM BIAS GAIN | DIAGnostic:BIAS:GAIN <integer> \|? (integer range 0 to 255) | - - |
| #24 YTM BIAS | DIAGnostic:BIAS:SYTM <integer>\|? (integer range 0 to 255) | - - |
| #25 YTM BIAS BN | DIAGnostic:BIAS:BOFFset <integer> \|? (integer range 0 to 255) | - - |
| #26 YTM BIAS ALC | DIAGnostic:BIAS:ALCGain <integer> \|? (integer range 0 to 255) | - - |

## Description of (ADJUST) Key Menu Functions

This section describes the (ADJUST) key menu functions. The functions are listed numerically from #0 to #26. Any remote command for a function is also defined in this section. The function of the remote command is virtually the same as for the manual operation.

# ADJ. #0 DISP INTENSITY

## Function Description

Select this adjustment to change the intensity level of the display windows. Press (ADJUST). When ADJ #0, DISP INTENSITY appears in the display windows, press (ENTER) to display the current intensity setting. Change the value with the (⇧) and (⇩) keys or enter a value between 0.0 and 1.0 with the data keys. A value of 0.0 reduces the display intensity to its minimum level. A value of 1.0 increases the display intensity to its maximum level.

## Related Command Syntax

**DISPlay:BRIGhtness** <real number>
(real number range is 0.0 to 1.0)

**DISPlay:BRIGhtness?**

Use this command to access and change the tracking source display window brightness.

Use the query to determine the current display brightness setting.

## Command Example

```
OUTPUT 703;"DISPlay:BRIGhtness 0.8"
```
***Set the display windows to the*** 0.8 ***intensity*** level.

```
OUTPUT 703;"DISPlay: BRIGhtness?"
```
***What is the current display window intensity setting?***

```
ENTER 703;Value
```
***Get the*** intensity ***setting.***

```
PRINT "The display intensity setting is ",Value
```
***Print or display the current setting value.***

# ADJ. #1 AMPLITUDE PEAK

## Function Description

Select this adjustment *(available on the HP 85645A only)* to run the automatic amplitude peaking routine. This adjustment optimizes the peak output power in bands 1 through 4 of the HP 85645A tracking source. The amplitude peak adjustment routine is especially valuable when you are using the tracking source in environments with temperature extremes, or when peak power is critical to a measurement.

Press (PRESET) before selecting this adjustment. During the adjustment, avoid pressing any front-panel keys.

Make sure the RF output power is turned on. The RF OUTPUT ON/OFF status indicator should be lit.

Press (ADJUST), then press (MENU DOWN) until ADJ . #1 , AMPLITUDE PEAK appears in the display windows. Press (ENTER) and the automatic amplitude peaking routine begins. After a moment, the message YTM PEAK DONE is displayed. During the amplitude peaking routine, the following errors may occur. Regardless of the error, however, previous YTM calibration data is restored.

- If error message 604 ALC LOOP BROKEN is displayed, the routine was unable to properly adjust the signal amplitude. There may be a problem with the ALC loop in the instrument.
- If error message 605 MOD AMP PWR LOW is displayed, the output power from the modulation amplifier is low. The cause may be related to the modulation amplifier, the power detector (which is part of the modulation amplifier), or the gain circuitry on the controller board assembly. Service the instrument to determine the cause.
- If error message 610 YTM CAL FAIL is displayed, the amplitude peak routine could not finish. This error message appears, usually along with those listed above, if there is a problem with the YTM driver on the controller board assembly, or with the YTM itself. Service the instrument to determine the cause.

## Related Command Syntax

CALibration:PEAKing[:EXEcute]

Use this command to start the tracking source's amplitude peaking routine.

## Command Example

```
OUTPUT703;"CALibration:PEAKing;*OPC"
```

***Start the instrument peaking routine. At the end of the routine, send an operation complete (OPC) indication to the display windows.***

```
J=0
  REPEAT
      J=J+l
```

***Start the loop sequence. This is a timeout sequence***

```
      IF J>TIME LIMIT THEN
      OUTPUT 703;"*RST;
      DISP  "ABORTED"

      STOP
  END IF

UNTIL BIT(SPOLL(703),6)=1
END
```

***If the time limit exceeds defined limits, reset the instrument. Print to the display that the procedure was aborted.***

# ADJ. #2 ALC EXT DETECTOR

## Function Description

Select this adjustment to access the external-detector calibration routine. Press (ADJUST), then press (MENU DOWN_) until ADJ #2, ALC EXT DETECTOR appears in the display windows. Press (ENTER) to display ENTER DET FREQ.

Enter the frequency value (within the range of the tracking source) at which you want to calibrate the external detector. Press a frequency-units key to terminate data entry.

The numbers that appear in the right-hand display window represent a DAC number and a previously existing power level. The power level displayed may or may not be accurate for your detector.

The adjustment routine prompts you for actual output power values at each DAC setting. Actual output power values can be accurately determined by using a power meter with a power sensor. The power sensor is placed at the point where leveling is desired. Enter the measured power value and terminate the entry with an appropriate power-units key. Notice that the DAC number changes after each entry.

Continue entering power meter readings associated with the DAC numbers until the message ENTER TO STORE appears. Press (ENTER). The message PROGRAMMING appears in the display window as the instrument stores the power values in memory. When the message ENTER TO UNDO appears, either press (ENTER) to start over or press any other front-panel key to exit the adjustment. During the calibration routine, press (↑) and (↓) to check or edit data entries.

Because the tracking source has no way of knowing where the minimum and maximum detector voltages are, the adjustment begins at the center of the tracking source's DAC numbers, which is at number 128, then decrements. The count of the DAC number decreases until the external detector voltage is as small as possible for the tracking source's hardware to operate. At that point, the count returns to the next DAC number just above the mid-point and begins incrementing until the detector voltage stops changing (reaches a peak output capability).

The detector is now calibrated and the power values you entered are stored until you need to calibrate another detector. Anytime the calibrated detector is used in external leveling mode, the output power selected with the tracking source's (POWER LEVEL) key is accurately calibrated for your measurement.

## Related Command Syntax

**CALibration:ALC:EXTernal**

**CALibration:ALC:EXT:FREQuency** <real number>

CALibration:ALC:POWer <real number>

Use the above commands to calibrate the external detector.

# ADJ. #3 SWP+TUNE ADJ

## Function Description

Select this adjustment to run the interactive routine that corrects for variations in the host SWP + TUNE OUTPUT signal. Use this adjustment only if the tracking source has difficulty remaining locked to the host (generally this is only the case with HP 8590 Series spectrum analyzers). The results of this adjustment are invoked by selecting (CONFIG), then SWP+TUNE SETTING and selecting the CUSTOM option, The results are not automatically activated at the end of the adjustment.

For host instruments other than the HP 8590 Series spectrum analyzers, the factory defined default values are acceptable. Press (ADJUST), then press (MENU DOWN) until ADJ **#3, SWP+TUNE** ADJ appears in the display windows Make sure the SWP + TUNE OUTPUT signal from the host is connected to the tracking source, then press (ENTER) to display `Set SA` to 0 SPAN. Set the host to 0 span. Set the host to the various frequency settings as prompted by the tracking source, pressing (ENTER) on the tracking source after each entry.

Refer to **Table** 5-3 for the frequency settings required by the tracking source for the different host instruments. The tracking source stores the sweep + tune voltages detected at the various frequencies, then uses these voltages for self-adjustment to improve its tracking operation.

## Related Command Syntax

CALibration:SWEep:ADJust

CALibration:SWEep:EXECute

Use these commands to adjust the sweep + tune voltages at different frequencies.

## Command Example

```
OUTPUT703;"CALibration:SWEeptune:
          ADJust;*OPC;

REPEAT

   OUTPUT 703;"CALibration:SWEeptune EXECute"

   WAIT .250

UNTIL BIT( SPOLL(703) ,6)=1

OUTPUT703;"DIAG:STORee"
```

*Access the sweep + tune adjustment mode. Display a message indicating the end of the process when it is completed. The *OPC command sends a completion sequence to the display at the completion of the process.*

*Set the host frequency value specified on the tracking source. Do this either manually or from a stored table of values. If you enter the value manually, be sure to allow an amount of wait time to allow the instrument to accept the command.*

*Continue adjusting the sweep + tune voltage for maximum performance.*

*Wait this amount of time for the instrument to accept the command.*

*The repeat loop continues until OPC=1. When OPC=l, bit 6 of the Status Byte register is set to 1.*

*Store the new sweep + tune settings in the instrument EEPROM.*

**Table 5-3. Host Instrument Sweep + Tune Adjustment Frequency Settings**

| Host Instrument | Band | Adjustment Start Frequency | Adjustment End Frequency |
|---|---|---|---|
| **HP 8560A spectrum analyzer** | 0 | 150 MHz | 2900 MHz |
| **HP 8561A spectrum analyzer** | 0 | 150 MHz | 2400 MHz |
| | 1 | 3600 MHz | 6460 MHz |
| **HP 8562A spectrum analyzer,**<br>**HP 8562A spectrum analyzer (including old S/N preceding 2350A),**<br>**and HP 8563A/B spectrum analyzer** | 0<br>1<br>2<br>3<br>4 | 150 MHz<br>3600 MHz<br>6700 MHz<br>13600 MHz<br>19810 MHz | 2400 MHz<br>5500 MHz<br>1190 MHz<br>18400 MHz<br>26500 MHz |
| **HP 8566A/B spectrum analyzer** | 0 | 0 MHz | 1900 MHz |
| | 1 | 2700 MHz | 5500 MHz |
| | 2 | 6100 MHz | 12100 MHz |
| | 3 | 12700 MHz | 18100 MHz |
| | 4 | 18900 MHz | 24000 MHz |
| **HP 8593A spectrum analyzer** | 0 | 300 MHz | 2550 MHz |
| | 1 | 3400 MHz | 5900 MHz |
| | 2 | 6600 MHz | 12100 MHz |
| | 3 | 13100 MHz | 18800 MHz |
| | 4 | 19600 MHz | 26500 MHz |
| **HP 8594A spectrum analyzer** | 0 | 300 MHz | 2900 MHz |
| **HP 8595A spectrum analyzer** | 0 | 300 MHz | 2550 MHz |
| | 1 | 3400 MHz | 6400 MHz |
| **HP 8340A synthesized sweeper** | 0 | 10 MHz | 2200 MHz |
| | 1 | 2500 MHz | 6800 MHz |
| | 2 | 7100 MHz | 13250 MHz |
| | 3 | 13600 MHz | 19700 MHz |
| | 4 | 20100 MHz | 26500 MHz |

**Table 5-3.**
**Host Instrument Sweep + Tune Adjustment Frequency Settings (continued)**

| Host Instrument | Band | Adjustment Start Frequency | Adjustment En Frequency |
|---|---|---|---|
| **HP 83590A RF plug-in** | 0 | 2000 MHz | 6800 MHz |
| | 1 | 7100 MHz | 13300 MHz |
| | 2 | 13600 MHz | 20000 MHz |
| **HP 83592A/B/C RF plug-in** | 0 | 25 MHz | 2200 MHz |
| | 1 | 2500 MHz | 6800 MHz |
| | 2 | 7100 MHz | 13300 MHz |
| | 3 | 13600 MHz | 20000 MHz |
| **HP 83594A RF plug-in** | 0 | 2000 MHz | 6800 MHz |
| | 1 | 7100 MHz | 13300 MHz |
| | 2 | 13600 MHz | 19900 MHz |
| | 3 | 20100 MHz | 26500 MHz |
| **HP 83595A RF plug-in** | 0 | 25 MHz | 2200 MHz |
| | 1 | 2500 MHz | 6800 MHz |
| | 2 | 7100 MHz | 13300 MHz |
| | 3 | 13600 MHz | 20100 MHz |
| | 4 | 20100 MHz | 26500 MHz |

# ADJ. #4 BAND LOCK

## Function Description

Select this function to lock onto a frequency band. Selecting a band with this function limits instrument operation and output frequency to the specified band. If the frequency and span setting of a host instrument configured with the tracking source exceeds the frequency limits of the specified band, signal tracking does not continue beyond the frequency limits of the specified band.

lb restore the instrument to normal operation, either press [PRESET] or enter a number larger than the largest band number of the tracking source you are using. The message MULTIBAND will appear in the display windows.

## Related Command Syntax

DIAGnostic:BNDLock <integer>
(integer range is 0 to 1 on the HP 85644A, and 0 to 4 on the HP 85645A)

DIAGnostic:BNDLock?

Use this command to select a tracking source harmonic band for the tracking source. When you select a band number, you limit the output frequency range to the range of the band chosen.

Use the query to determine the current harmonic band chosen. The response may be a real number from 0 to 4 or the multiband state.

## Command Example

```
OUTPUT 703;"DIAGnostic:BANDlock 3;"          Set the tracking source to band 3.
OUTPUT703;"DIAGnostic:BANDlock:STATeOFF"     Put the tracking source in multiband-
                                             sweep mode.
OUTPUT703;"DIAGnostic:BANDlock?;"            What is the current tracking
                                             source band setting?
ENTER 703;Value                              Get the current band setting.
PRINT "The tracking source band lock         Print or display the current
       setting is ",Value                    setting of band lock.
```

## ADJ. #5 LEVEL AMP 1

**Function Description**

Select this adjustment to display or change the first leveling amplifier DAC. The adjustment affects instrument calibration and should be performed in conjunction with the adjustment procedure in Chapter 1 of this manual.

You must provide an acceptable LO input signal to the tracking source. Refer to the tracking source specifications in the ***HP 85644A/HP 85645A Tracking Source*** Users ***Guide*** for acceptable LO input signal requirements.

Measure the LO output power from the tracking source. Enter this value into the tracking source EEROM. Once the value is entered, you can choose to save the measured value in the tracking source EEROM.

### Related Command Syntax

DIAGnostic:LEVelamp:FIRst <integer>
(integer range is 0 to 255)

DIAGnostic:LEVelamp:FIRst?

Use this command to access the first leveling amplifier DAC. The DAC should be adjusted only in conjunction with the manual adjustment procedure. Refer to Chapter 1, "Making Adjustments. "

Use the query to determine the current leveling amplifier DAC setting.

### Command Example

```
OUTPUT703;"DIAGnostic:LEVelamp:FIRSt126;"
```
*Set the first leveling amplifier DAC to 126.*

```
OUTPUT703;"DIAGnostic:LEVelamp:FIRSt?
```
*What is the current setting of the first Leveling amplifier DAC?*

```
ENTER 703;Level
```
*Get the current setting of the first leveling amplifier DAC.*

```
PRINT "The current first leveling
      amplifier setting is ",Alcrg
```
*Print or display the current setting* of *the first leveling am-&/i&r DAC.*

# ADJ. #6 LEVEL AMP 2

## Function Description

Select this adjustment to calibrate the internal LO amplifier. The adjustment affects instrument calibration and should be performed in conjunction with the adjustment procedure in Chapter 1 of this manual.

Once the values are entered, you can choose to save the calibration values in the tracking source EEPROM.

## Related Command Syntax

DIAGnostic:LEVelamp:SECond

Use this command to automatically adjust the second leveling amplifier DAC. The adjustment sets the DAC for an optimum discriminator output voltage.

When the frequency value is displayed on the tracking source, set the host instrument to that frequency. Wait for a moment as the host instrument frequency adjusts to the setting. Now enter the following commands:

DIAGnostic:LEVelamp:SECond:EXECute

DIAGnostic:STOReе

The command DIAG:LEV:SEC:EXEC activates a termination sequence. Store the calibration factors in the EEPROM by entering the command DIAGnostic:STOReе.

## Command Example

```
OUTPUT703;"DIAGnostic:LEVelamp:SECond;*OPC;"
```

*Adjust the second leveling amplifier for optimum output. The *OPC command can be included to alert you when the process is completed.*

```
OUTPUT703;"DIAGnostic:LEVelamp:SECond:EXECute
```

*After setting the host instrument frequency to the value displayed in the tracking source display windows, enter this command to terminate data entry. Wait for the frequency to be set.*

```
OUTPUT703;"DIAGnostic:STOReе"
```

*Store the new calibration factors in the instrument's EEPROM.*

# ADJ. #7 SLOPE LO BAND

**Function Description** Select this function to adjust the amplitude response as a function of frequency for low band operation. The adjustment affects instrument calibration and should be performed in conjunction with the adjustment procedure in Chapter 1 of this manual.

## Related Command Syntax

CALibration:POWer:SLOPe:LOWBand <integer> |UP|DOWN
(integer range is 0 to 3)

CALibration:POWer:SLOPe:LOWBand?

Use the CAL:POW:SLOP:LOWB command to activate the low-band slope adjustment mode. The UP and DOWN parameters adjust the slope in increments equal to the power-level step increment. Follow immediately with the CAL:POWer:SLOPe:EXEC command to activate the value.

## Command Example

```
OUTPUT 703;"CALibration:POWer:SLOPe:LOWBand UP"
```
*Access low-band mode, then adjust the slope up one power-level step unit from its current position.*

```
OUTPUT 703;"CALibration:POWer:SLOPe:EXEC
```
*After the slope adjustment is completed with the* above *command, enter this command to activate the new level.*

```
OUTPUT 703;"CALibration:POWer:SLOPe:LOWBand?"
```
*What is the current low-band slope setting?*

```
ENTER 703;Lslope
```
*Get the current low-band slope setting.*

```
PRINT "The low-band slope setting
       is ",Lslope, "dB."
```
*Print or display the current setting.*

# ADJ. #8 ALC LO BAND

## Function Description

Select this function to adjust the amplitude response as a function of frequency for low band operation. The adjustment affects instrument calibration and should be performed in conjunction with the adjustment procedure in Chapter 1 of this manual.

## Related Command Syntax

CALibration:ALC:LOBand; *OPC

Use this command to place the tracking source in calibration mode for ALC low-band operation. Follow the command with the *OPC command so that the instrument displays a completion notification at the end of the process.

## Command Example

```
OUTPUT 703;"CALibration:ALC:LOWBand;*OPC;"
REPEAT
    OUTPUT 703;"CALibration:ALC:POWer -10dBm"
    WAIT .250
UNTIL BIT( SPOLL(703),6)=1
OUTPUT 703;"DIAG:STOReE"
```

*Access the low-band adjustment mode. Display a message indicating the end of the process when it is completed. The *OPC command sends a completion sequence to the display at the completion of the process.*

*Continue adjusting the ALC. When the power meter measurement is settled, read the power meter or spectrum analyzer for the measured amplitude value,*

*Enter the power meter value.*

*Wait this amount* of time for *the instrument to accept the command.*

*The repeat loop continues until OPC=1. When OPC=1, bit 6 of the Status Byte register is set to 1.*

*Store the amplitude value in the instrument EEPROM.*

## ADJ. #9 SLOPE HI BAND

**Function Description** Select this function to adjust the amplitude response as a function of frequency for high band operation. The adjustment affects instrument calibration and should be performed in conjunction with the adjustment procedure in Chapter 1 of this manual.

### Related Command Syntax

CALibration:POWer:HIGHband **<integer>|UP|DOWN|?**
(integer range is 0 to 1 **dB** for high band)

CALibration:SLOPe:EXECute

Use the **CAL:POW:SLOP:HIGH** command to adjust the high-band power slope. Follow immediately with the CAL:POWer:SLOPe:EXEC command to activate the value.

### Command Example

```
OUTPUT 703;"CALibration:POWer:SLOPe:HIGHband UP"
```
*Access high-band mode, then adjust the slope up one power-level step unit from its current position.*

```
OUTPUT 703;"CALibration:POWer:SLOPe:EXEC
```
*After the slope adjustment is completed with the above command, enter this command to activate the new level.*

```
OUTPUT 703;"CALibration:POWer:SLOPe:HIGHband?"
```
*What is the current high-band slope setting?*

```
ENTER 703;Hslope
```
*Get the current high band slope setting.*

```
PRINT "The high-band slope setting
       is ",Hslope, "dB."
```
*Print or display the current setting.*

# ADJ. #10 ALC HI BAND

**Function Description** Select this function to calibrate the output power level of the ALC.

## Related Command Syntax

CALibration:ALC:HIGHband; *OPC

Use this command to place the tracking source in calibration mode for ALC high-band operation. Optionally, follow the command with the *OPC command so that the instrument displays a completion notification at the end of the process.

## Command Example

```
OUTPUT703;"CALibration:ALC:HIGHband;*OPC;"
REPEAT
   OUTPUT 703;"CALibration:ALC:POWer 10dBm"
   WAIT .250
UNTIL BIT( SPOLL(703) ,6)=1
OUTPUT703;"DIAG:STOReе"
```

*Access the* high-band *adjustment mode. Display a message indicating the end of the process when it is completed. The *OPC command sends a completion sequence to the display at the completion of the proms.*

*Continue adjusting the ALC. When the power meter measurement is settled, read the power meter or spectrum analyzer for the measured amplitude value,*

*Enter the power meter value.*

*Wait this amount of time for the instrument to accept the command.*

*The repeat loop continues until OPC=1. When OPC=1, bit 6 of the Status Byte register is set to 1.*

*Store the amplitude value in the instrument EEPROM.*

## ADJ. #11 CW ACCURACY

**Function Description** Select this function to calibrate the CW frequency accuracy of the instrument.

### Related Command Syntax

CALibration:FREQuency:ADJ

CALibration:FREQuency[:CW] <real **number><frequency** unit> (real number range for the HP **85644A** is 0 Hz to 6.5 **GHz;** for the HP **85645A** it is 0 Hz to 26.5 **GHz)**

The CAL:REF:ADJ command must be executed first to access the CW accuracy adjustment. After executing the command, measure the CW frequency with a frequency counter. Now enter the CAL:FREQ[:CW] command and include the measured CW frequency value.

### Command Example

```
OUTPUT703;"CALibration:FREQuency:ADJust;*OPC;
REPEAT
   OUTPUT 703;"CALibration:FREQuency 2.51GHz"
   WAIT .250
   UNTIL BIT( SPOLL(703) , 6)=1
OUTPUT703;"DIAG:STORee"
```

*Access the CW accuracy adjustment mode. Display a message indicating the end of the process once it is completed. The *OPC command sends a completion sequence to the display at the completion of the process.*

*Continue ad&sting the ALC. Whim the frequency measurement is settled, read the frequency counter or spectrum analyzer for the measured frequency value.*

*Enter the measured frequency value.*

*Wait this amount of time for the instrument to accept the command.*

*The repeat loop continues until OPC=1. When OPC=1, bit 6 of the Status Byte register is set to 1.*

*Store the frequency value in the instrument EEPROM.*

# ADJ. #12 INT REFERENCE

Select this function to initiate the internal reference frequency adjustment procedure. This adjustment improves the frequency tracking response of the HP 856458 tracking source.

## Function Description

## Related Command Syntax

CALibration:REFerence:ADJ

CALibration:REFerence[:OFFSet] <real number><frequency unit> | UP|DOWN
(real number range for the HP 85644A is 0 Hz to 6.5 GHz; for the HP 85645A it is 0 Hz to 26.5 GHz)

DIAGnostic:STOReе

The CAL:REF:ADJ command must be executed first to access the internal-reference amplitude-accuracy adjustment mode. Follow with the CAL:REF[:OFFS] command. Observe the trace on the display. Peak the trace by sending the UP and DOWN commands as appropriate. Complete the adjustment by sending the DIAG:STOR command to store the new values in instrument memory.

## Command Example

```
OUTPUT703;"CALibration:REFerence:
          ADJust;*OPC;
```
*Access the internal-reference amplitud accuracy adjustment mode. Display a* message *indicating the end of the process when it is completed. The *OPC command sends a completion sequence to the display at the completion of the process.*

```
REPEAT
```
*2Continue adjusting the ALC. After the amplitude measurement is settled, read the power meter or spectrum analyzer for the measured amplitude value.*

```
   OUTPUT703;"CALibration:REFerence UP"
```
*Continue adjusting the frequency up or down until the amplitude is peaked.*

```
   WAIT .250
```
*Wait this number of seconds for the instrument to accept the command.*

```
UNTIL BIT( SPOLL(703) , 6)=1
```
*The repeat loop continues until OPC=1. When OPC=1, bit 6 of the Status Byte register is set to 1.*

```
   OUTPUT703;"SOURce:FREQuency;OFFset?"
```
*What is the current frequency offset value?*

```
   ENTER 703;R
```
*Read the final frequency value*

```
OUTPUT 703;"CALibration:REFerence:;R; ";"
```
*Enter the final value of R to terminate the adjustment procedure.*

```
OUTPUT703;"DIAG:STOREe"
```
*Store the amplitude value* in *the instrument EEPROM.*

# ADJ. #13 YTM GAIN

**Function Description** Select this function (only on an HP 85645A) to adjust the YTM gain DAC. The gain DAC adjustment affects the amplitude accuracy of the instrument. The DAC should be adjusted only in conjunction with the manual adjustment procedure. Refer to Chapter 1, "Making Adjustments "

## Related Command Syntax

DIAGnostics:YTM:GAIN <integer>
(integer range is 0 to 255)

DIAGnostics:YTM:GAIN?

Use this command to access and set the YTM GAIN DAC.

Use the query to determine the current YTM gain DAC setting.

## Command example

```
OUTPUT 703;"DIAGnostic:YTM:GAIN 126"      Set the YTM gain DAC to 126.
OUTPUT703;"DIAGnostic:YTM:GAIN?"          What is the current YTM gain
                                          DAC setting?
ENTER 703;Gvalue                          Get the DAC setting.
PRINT "The current YTM gain DAC setting   Print or display the current
      is ",Gvalue                         YTM gain DAC setting.
```

# ADJ. #14 YTM OFFSET

**Function Description** Select this function (only on an HP 85645A) to adjust the YTM offset DAC. The DAC should be adjusted only in conjunction with the manual adjustment procedure. Refer to Chapter 1, "Making Adjustments.'

## Related Command Syntax

DIAGnostic:YTM:OFFSet <integer>
(integer range is 0 to 255)

DIAGnostic:YTM:OFFSet?

Use this command to access and set the YTM offset DAC.

Use the query to determine the current YTM offset DAC setting.

## Command Example

```
OUTPUT 703;"DIAGnostic:YTM:OFFSet 126"      Set the YTM offset DAC to 126.
OUTPUT 703;"DIAGnostic:YTM:OFFSet?"         What is the current YTM offset
                                            DAC setting?
ENTER 703;Value                             Get the DAC setting.
PRINT "The current YTM offset DAC           Print or display the current
       setting is ",Value                   YTM offset DAC setting.
```

# ADJ. #15 YTM BP1

**Function Description** Select this function (only on an HP 85645A) to adjust the YTM breakpoint one DAC. The DAC should be adjusted only in conjunction with the manual adjustment procedure. Refer to Chapter 1, "Making Adjustments. "

## Related Command Syntax

DIAGnostic:YTM:BREakpoint:ONE <integer>
(integer range is 0 to 255)

DIAGnostic:YTM:BREakpoint:ONE?

Use this command to access and set the YTM breakpoint one DAC.

Use the query to determine the current DAC setting of YTM breakpoint one.

## Command Example

```
OUTPUT 703;"DIAGnostic:YTM:BREakpoint:ONE 126"      Set the YTM breakpoint one
                                                    DAC to 126.
OUTPUT 703;"DIAGnostic:YTM:BREakpoint?"             What is the current YTM break-
                                                    point one DAC setting?
ENTER 703;Break                                     Get the DAC setting.
PRINT "The current YTM breakpoint one DAC           Print or display the current
       setting is ",Break                           YTM breakpoint one DAC setting.
```

# ADJ. #16 YTM BP2

**Function Description** Select this function (only on an HP 85645A) to adjust the YTM breakpoint two DAC. The DAC should be adjusted only in conjunction with the manual adjustment procedure. Refer to Chapter 1, "Making Adjustments."

## Related Command Syntax

DIAGnostic:YTM:BREakpoint:TWO <integer>
(integer range is 0 to 255)

DIAGnostic:YTM:BREakpoint:TWO?

Use this command to access and set the YTM breakpoint two DAC. The DAC should be adjusted only in conjunction with the manual adjustment procedure. Refer to Chapter 1, "Making Adjustments."

Use the query to determine the current DAC setting of YTM breakpoint two.

## Command Example

```
OUTPUT 703;"DIAGnostic:YTM:BREakpoint:TWO 126"
```
*Set the YTM breakpoint two DAC to 126.*

```
OUTPUT 703;"DIAGnostic:YTM:BREakpoint?"
```
*What is the current YTM breakpoint two DAC setting?*

```
ENTER 703;Break
```
*Get the DAC setting.*

```
PRINT "The current YTM breakpoint two DAC
      setting is ",Break
```
*Print or display the current YTM breakpoint two DAC setting.*

# ADJ. #17 YTM BP3

## Function Description

Select this function (only on an HP 85645A) to adjust the YTM breakpoint three DAC. The DAC should be adjusted only in conjunction with the manual adjustment procedure. Refer to Chapter 1, "Making Adjustments."

## Related Command Syntax

**DIAGnostic:YTM:BREakpoint:THRee** <integer>
(integer range is 0 to 255)

DIAGnostic:YTM:BREakpoint:THRee?

Use this command to access and set the YTM breakpoint three DAC.

Use the query to determine the current DAC setting of YTM breakpoint three.

## Command Example

```
OUTPUT 703;"DIAGnostic:YTM:BREakpoint:THRee 126"
```
*Set the YTM breakpoint three DAC to 126.*

```
OUTPUT 703;"DIAGnostic:YTM:BREakpoint?"
```
*What is the current YTM breakpoint three DAC setting?*

```
ENTER 703;Break
```
*Get the DAC setting.*

```
PRINT "The current YTM breakpoint three DAC
      setting is ",Break
```
*Print or display the current YTM breakpoint three DAC setting.*

# ADJ. #18 YTM BP4

**Function Description** Select this function (only on an HP 85645A) to adjust the YTM breakpoint four DAC. The DAC should be adjusted only in conjunction with the manual adjustment procedure. Refer to Chapter 1, "Making Adjustments. "

## Related Command Syntax

**DIAGnostic:YTF:BREakpoint:FOUR** <integer>
(integer range is 0 to 255)

DIAGnostic:YTF:BREakpoint:FOUR?

Use this command to access and set the breakpoint four DAC.

Use the query to determine the current DAC setting of YTM breakpoint four.

## Command Example

```
OUTPUT 703;"DIAGnostic:YTM:BREakpoint:FOUR 126"

OUTPUT 703;"DIAGnostic:YTM:BREakpoint?"

ENTER 703;Break
PRINT "The current YTM breakpoint four DAC
       setting is ",Break
```

*Set the YTM breakpoint four DAC to 126.*

*What is the current YTM breakpoint four DAC setting?*

*Get the DAC setting.*

*Print or display the current YTM breakpoint four DAC setting.*

# ADJ. #19 YTM BP4 FRQ

## Function Description

Select this function (only on an HP 85645A) to adjust the YTM breakpoint four frequency DAC. The DAC should be adjusted only in conjunction with the manual adjustment procedure. Refer to Chapter 1, "Making Adjustments."

## Related Command Syntax

**DIAGnostic:YTM:BPF4Freq** <integer>
(integer range is 0 to 255)

**DIAGnostic:YTM:BP4Freq?**

Use this command to access and set the YTM breakpoint four frequency DAC. The DAC should be adjusted only in conjunction with the manual adjustment procedure. Refer to Chapter 1, "Making Adjustments."

Use the query to determine the current DAC setting for YTM breakpoint four frequency.

## Command Example

```
OUTPUT703;"DIAGnostic:YTM:BP4Freq126"      Set the YTM breakpoint four
                                           frequency DAC to 126.
OUTPUT703;"DIAGnostic:YTM:BP4Freq?"        What is thecurrent YTMbreak-
                                           point four frequency DACsetting?
ENTER703;Breakfr                           Get the DAC setting.
PRINT "The current YTM breakpoint four     Print or display the current
      frequency DAC setting is ",Breakfr   YTMbreakpoint four frequency
                                           DAC setting.
```

# ADJ. #20 YTM DELAY

**Function Description** Select this function (only on an HP 856458) to adjust the YTM delay DAC. The DAC should be adjusted only in conjunction with the manual adjustment procedure. Refer to Chapter 1, "Making Adjustments. "

## Related Command Syntax

DIAGnostic:YTM:DELay <integer>
(integer range is 0 to 255)

DIAGnostic:YTM:DELay?

Use this command to access and set the YTM delay DAC.

Use the query to determine the current YTM delay DAC setting.

## Command Example

```
OUTPUT 703;"DIAGnostic:YTM:DELay 126"
OUTPUT 703;"DIAGnostic:YTM:DELay?"

ENTER 703;Break
PRINT "The current YTM delay DAC
       setting is ",Break
```

*Set the YTM delay DAC to 126.*
*What is the current YTM delay DAC setting?*
*Get the DAC setting.*
*Print or display the current YTM delay DAC setting.*

# ADJ. #21 YTM BIAS PWR LVL

## Function Description

Select this function (only on an HP 85645A) to adjust the YTM bias and power-level adjust DAC. The DAC should be adjusted only in conjunction with the manual adjustment procedure. Refer to Chapter 1, "Making Adjustments, "

## Related Command Syntax

DIAGnostic:BIAS:PWRLvl

Use this command to automatically adjust the power-level adjust DAC and the SYTM bias DAC.

## Command Example

```
OUTPUT703;"DIAGnostic:BIAS:PWRLvl"
```

*Adjust the power-level adjust DAC and the SYTM bias DAC.*

# ADJ. #22 YTM BIAS OFS

**Function Description** Select this function (only on an HP 85645A) to adjust the YTM bias offset DAC. The DAC should be adjusted only in conjunction with the manual adjustment procedure. Refer to Chapter 1, "Making Adjustments. "

## Related Command Syntax

DIAGnostic:BIAS:OFFSet <integer>
(integer range is 0 to 255)

DIAGnostic:BIAS:OFFSet?

Use this command to access and set the YTM bias offset DAC. The DAC should be adjusted only in conjunction with the manual adjustment procedure. Refer to Chapter 1, "Making Adjustments."

Use the query to determine the current bias offset DAC setting.

## Command Example

```
OUTPUT 703;"DIAGnostic:BIAS:OFFSet 126"     Set the bias offset DAC to 126.
OUTPUT 703;"DIAGnostic:BIAS:OFFSet?"        What is the current bias offset
                                            DAC setting?
ENTER 703;Biaso                             Get the DAC setting.
PRINT "The current bias offset DAC          Print or display the current
       setting is ",Biaso                   bias offset DAC setting.
```

# ADJ. #23 YTM BIAS GAIN

## Function Description

Select this function (only on an HP 85645A) to adjust the YTM bias gain DAC. The DAC should be adjusted only in conjunction with the manual adjustment procedure. Refer to Chapter 1, "Making Adjustments. "

## Related Command Syntax

DIAGnostic:BIAS:GAIN <integer>
(integer range is 0 to 255)

DIAGnostic:BIAS:GAIN?

Use this command to access and set the YTM bias gain DAC. The DAC should be adjusted only in conjunction with the manual adjustment procedure. Refer to Chapter 1, "Making Adjustments"

Use the query to determine the current bias gain DAC setting.

## Command Example

```
OUTPUT 703;"DIAGnostic:BIAS:GAIN 126"
OUTPUT 703;"DIAGnostic:BIAS:GAIN?"

ENTER 703;Biasg
PRINT "The current bias gain DAC
       setting is ",Biasg
```

*Set the bias gain DAC to 126.*
*What is the current bias gain DAC setting?*
*Get the DAC setting.*
*Print or display the current bias gain DAC setting.*

# ADJ. #24 YTM BIAS

**Function Description** Select this function (only on an HP 85645A) to adjust the SYTM bias DAC. The DAC should be adjusted only in conjunction with the manual adjustment procedure. Refer to Chapter 1, "Making Adjustments. "

## Related Command Syntax

DIAGnostic:BIAS:SYTM <integer>
(integer range is 0 to 255)

DIAGnostic:BIAS:SYTM?

Use this command to access and set the SYTM bias DAC.

Use the query to determine the current SYTM bias DAC setting.

## Command Example

```
OUTPUT 703;"DIAGnostic:BIAS:SYTM 126"      Set the SYTM bias DAC to 126.
OUTPUT 703;"DIAGnostic:BIAS:SYTM?"         What is the current SYTM bias
                                           DAC setting?
ENTER 703;Sytmb                            Get the DAC setting.
PRINT "The current SYTM bias DAC setting   Print or display the current
      is ",Sytmb                           SYTM bias DAC setting.
```

# ADJ. #25 YTM BIAS BN

## Function Description

Select this function to adjust the YTM bias band offset DAC. The DAC should be adjusted only in conjunction with the manual adjustment procedure. Refer to Chapter 1, "Making Adjustments."

## Related Command Syntax

**DIAGnostic:BIAS:BOFFset** <integer>
(integer range is 0 to 255)

**DIAGnostic:BIAS:BOFFset?**

Use this command to access and set the bias band offset DAC.

Use the query to determine the current bias band offset DAC setting.

## Command Example

```
OUTPUT 703;"DIAGnostic:BIAS:BOFFset 126"
```
*Set the bias band offset DAC to 126.*

```
OUTPUT703;"DIAGnostic:BIAS:BOFFset?"
```
*What is the current bias band offset DAC setting?*

```
ENTER 703;Bboffs
```
*Get the DAC setting.*

```
PRINT "The current bias band offset DAC
      setting is ",Bdoffs
```
*Print or display the current bias band offset DAC setting.*

# ADJ. #26 YTM BIAS ALC

**Function Description** Select this function (only on an HP 85645A) to adjust the bias ALC gain DAC. The DAC should be adjusted only in conjunction with the manual adjustment procedure. Refer to Chapter 1, "Making Adjustments. "

## Related Command Syntax

DIAGnostic:BIAS:ALCGain <integer>
(integer range is 0 to 255)

DIAGnostic:BIAS:ALCGain?

Use this command to access and set the bias ALC gain DAC.

Use the query to determine the current YTM bias ALC DAC setting.

## Command Example

```
OUTPUT 703;"DIAGnostic:ALCGain 126"
```
*Set the current ALC gain DAC to 126.*

```
OUTPUT703;"DIAGnostic:ALCGain?"
```
*What is the current ALC gain DAC setting?*

```
ENTER 703;Sytmb
```
*Get the DAC setting.*

```
PRINT "The current SYTM bias DAC
       setting is ",Sytmb
```
*Print or display the current SYTM bias DAC setting.*

# 6

# If You Have a Problem

If you have a problem with the HP 85644A/85645A tracking source, first, check the basics This chapter contains a checklist that will help identify some of the most common problems. If further troubleshooting is necessary, refer to Chapter 3, "General Troubleshooting," in this book or return the tracking source to Hewlett-Packard. This chapter is organized into the following sections:

**Check the Basics.**
A quick checklist to help identify some of the most common problems.

**Calling HP Sales and Service Offices.**
Refer to this section for information about contacting an HP sales and service office.

**Returning Your Tracking Source for Service.**
Refer to this section for information about returning your tracking source for service.

## Check the Basics

Often problems may be solved by repeating what was being done when the problem occurred. A few minutes spent in performing these simple checks may eliminate time spent waiting for instrument repair.

- Check that the tracking source is plugged into the proper ac power source.
- Check that the line socket has power.
- Check that the rear-panel voltage selector switch is set correctly.
- Check that the line fuse is good.
- Check that the tracking source is turned on.
- Check that the other equipment, cables, and connectors are connected properly and operating correctly.
- Check the equipment settings in the procedure that was being used when the problem occurred.
- Check that the test being performed and the expected results are within the specifications and capabilities of the tracking source. Refer to Chapter 4 of the ***HP 85644A/85645A Tracking Source User's Guide.***
- Check the tracking source display for error messages. Refer to Chapter 7 of the ***HP 85644A/85645A Tracking Source*** User's ***Guide.***
- Check operation by performing the verification procedures in Chapter 2 of the ***HP 85644A/85645A Tracking Source User's Guide.*** Record all results in the Performance Test record.
- Check for problems similar to those described in Chapter 3 of the ***HP 85644A/85645A Tracking Source User's Guide.***

If there is still a problem, refer to Chapter 3, "General Troubleshooting, " in this book.

## Calling HP Sales and Service Offices

Use the information in this section to obtain Hewlett-Packard sales and service offices information. Sales and service offices are located around the world to provide complete support for your tracking source. To obtain servicing information or to order replacement parts, contact the nearest Hewlett-Packard Sales and Service office listed in Table 6-1. In any correspondence or telephone conversations, refer to the tracking source by its model number and full serial number. With this information, the HP representative can quickly determine whether your unit is still within its warranty period.

## Instrument serial numbers

Hewlett-Packard makes frequent improvements to its products to enhance their performance and reliability. Hewlett-Packard service personnel have access to the records of design changes for each instrument, based on the instrument's serial number and option designation.

Whenever you contact Hewlett-Packard about your tracking source, have a complete serial number. This will ensure that you obtain accurate service information.

A serial-number label is attached to the rear of the tracking source. This label has two instrument identification entries: the Arst provides the instrument's serial number and the second provides the identification number for each option built into the instrument.

The serial number is divided into three parts The **first** four digits are the serial-number prefix; the letter indicates the country of origin; the last five digits are the suffix. See Figure **6-1.**

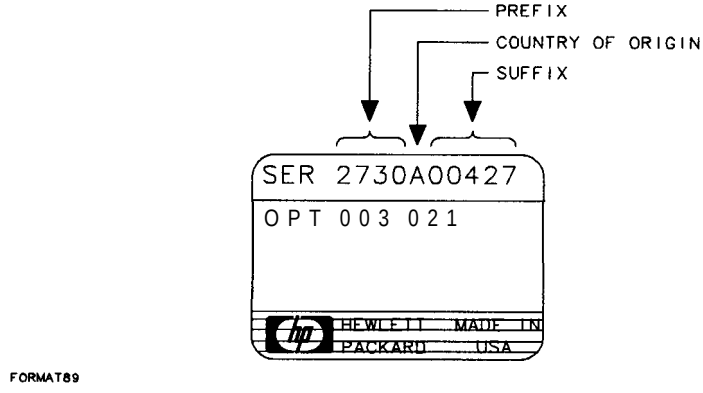



**Figure 6-1. Typical Serial-Number Label**

The serial-number prefix is a code that identifies the date of the last major design change that is built into the tracking source. The letter identifies the country where the instrument was manufactured. The five-digit suffix is a sequential number and is different for each instrument.

## Before calling Hewlett-Packard

Before calling Hewlett-Packard or returning the tracking source for service, please make the checks listed in "Check the Basics". If you still have a problem please read the warranty printed at the front of this guide. **If** your tracking source is covered by a separate maintenance agreement, please be familiar with its terms,

Hewlett-Packard offers several maintenance plans to service your tracking source after warranty expiration. Call your HP Sales and Service Office for full details.

If you want to service the tracking source yourself after warranty expiration, refer to Chapter 3, “General Troubleshooting,” in this book.

## HP sales and service offices

Refer to the following table for HP sales and service office telephone and address information.

## Table 6-1. Hewlett-Packard Sales and Service Offices

### US FIELD OPERATIONS

**Customer Information**
Hewlett-Packard Company
19320 Pruneridge Avenue
Cupertino, CA 95014, USA
(800) 752-0900

**California, Northern**
Hewlett-Packard Co.
301 E. Evelyn
Mountain View, CA 94041
(415) 694-2000

**California, Southern**
Hewlett-Packard Co.
1421 South Manhattan Ave.
Fullerton, CA 92631
(714) 999-6700

**Colorado**
Hewlett-Packard Co.
24 Inverness Place, East
Englewood, CC 80112
(303) 649-5000

**Georgia**
Hewlett-Packard Co.
2000 South Park Place
Atlanta, GA 30339
(404) 955-1500

**Illinois**
Hewlett-Packard Co.
5201 lbllview Drive
Rolling Meadows, IL 60008
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## Returning Your Tracking Source for Service

Use the information in this section if you need to return the tracking source to Hewlett-Packard.

### Package the tracking source for shipment

Use the following steps to package the tracking source for shipment to Hewlett-Packard for service:

1. Pill in a service tag (available at the end of this chapter) and attach it to the instrument. Please be as specific as possible about the nature of the problem. Send a copy of any or all of the following information:
   - Any error messages that appeared on the tracking source display.
   - A completed Performance Test record. (Located in Chapter 2 of the ***HP 85644A/85645A Tracking Source User's Guide***
   - Any other specific data on the performance of the tracking source.

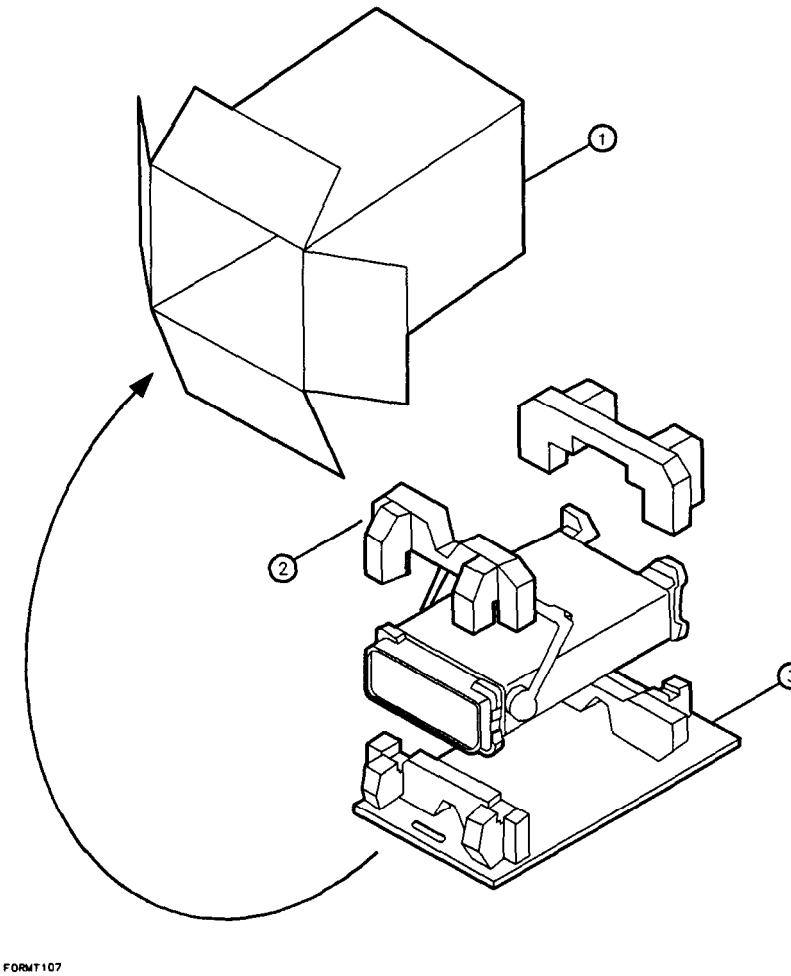
**Caution**

Tracking source damage can result from using packaging materials other than those specified. Never use styrene pellets in any shape as packaging materials They do not adequately cushion the instrument or prevent it from shifting in the carton. Styrene pellets cause equipment damage by generating static electricity and by lodging in the tracking source fan.

2. Use the original packaging materials (see Figure 6-2) or a strong shipping container that is made of double-walled, corrugated cardboard with 159 kg (350 lb) bursting strength. The carton must be both large enough and strong enough to accommodate the tracking source and allow at least 3 to 4 inches on all sides of the tracking source for packing material.
3. Surround the instrument with at least 3 to 4 inches of packing material, or enough to prevent the instrument from moving in the carton. If packing foam is not available, the best alternative is SD-240 Air Cap™ from Sealed Air Corporation (Commerce, CA 90001). Air Cap looks like a plastic sheet covered with 1-1/4 inch air-filled bubbles Use the pink Air Cap to reduce static electricity. Wrap the instrument several times in the material to both protect the instrument and prevent it from moving in the carton.
4. Seal the shipping container securely with strong nylon adhesive tape.
5. Mark the shipping container "FRAGILE, HANDLE WITH CARE" to ensure careful handling.
6. Retain copies of all shipping papers.

## Packaging materials to use

Use the following illustration and table to help you package a tracking source for shipment.




| Item | Description | HP part number |
|---|---|---|
| 1 | Outer Carton | 9211-6348 |
| 2 | Inner Foam Pad Set | 9220-4734 |
| 3 | Bottom Skid Tray | 9220-4733 |

**Figure 6-2.**
**HP 85644A/85645A Tracking Source Packaging Materials**

# 7

# Assembly Replacement

This chapter provides information for identifying, ordering, and replacing assemblies, parts and accessories for the HP 85644A/85645A tracking source:

**Ordering Information.**
Information about ordering replaceable assemblies and parts used in the HP 85644A/85645A tracking source by using Hewlett-Packard's direct mail-order or phone-order systems.

**Static-Safe Accessories.**
Information about electrostatic discharge (ESD) and HP part numbers of static-safe accessories.

**Assembly Removal Diagrams.**
Information about the removal of some tracking source assemblies.

**Replaceable Parts.**
Information for identifying and ordering replaceable assemblies and parts used in the HP 85644A/85645A tracking source. This section also contains a table containing definitions of the reference designations, abbreviations, and multipliers used in the parts tables

**Component-Level Information Packets.**
Information about component-level information packets (CLIPS).

## Ordering Information

lb order an assembly or part listed in this chapter, quote the Hewlett-Packard part number and the check digit, and indicate the quantity required. The check digit is used to verify the correct part number. The check digit will ensure accurate processing of your order.

lb order a part that is ***not*** listed, include the following information with the order:

- Tracking source model number.
- Tracking source serial number (located on the rear panel of the instrument).
- Description of where the part is located, what it looks like, and its function (if known).
- Quantity needed.

Parts can be ordered by addressing the order to the nearest Hewlett-Packard office. Customers within the USA can also use either the direct mail-order system, or the direct phone-order system described below. The direct phone-order system has a toll-free phone number available.

### Direct Mail-Order System

Within the USA, Hewlett-Packard can supply parts through a direct mail-order system. Advantages of using the system are as follows:

- Direct ordering and shipment from Hewlett-Packard.
- No maximum or minimum on any mail order. (There is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing.)
- Prepaid transportation. (There is a small handling charge for each order.)
- No invoices.

lb provide these advantages, a check or money order must accompany each order. Mail-order forms and specific ordering information are available through your local HP office.

## Direct Phone-Order System

Within the USA, a phone order system is available for regular and hotline replacement parts service. A toll-free phone number is available, and Mastercard and Visa are accepted.

### Regular Orders

The toll-free phone number, (800) 227-8164, is available Monday through Friday, 6 AM to 5 PM (Pacific time). Regular orders have a 4-day delivery time.

### Hotline Orders

Hotline service is available 24 hours a day, 365 days a year, for emergency parts ordering. The toll-free phone number, (800) 227-8164, is available Monday through Friday, 6 AM to 5 PM (Pacific time). After-hours and on holidays, call (415) 968-2347.

lb cover the cost of freight and special handing, there is an additional hotline charge on each order (three line items maximum per order). Hotline orders are normally delivered the next business day after they are ordered.

## Static-Safe Accessories

Electrostatic discharge (ESD) can damage or destroy electronic components. All work performed on assemblies containing electronic components should be done ***only*** at a static-safe work station.

**Table 7-1** provides information on ordering static-safe accessories and shows an example of a static-safe work station using two types of ESD protection:

- Conductive table-mat and wrist-strap combination.
- Conductive floor-mat and heel-strap combination.

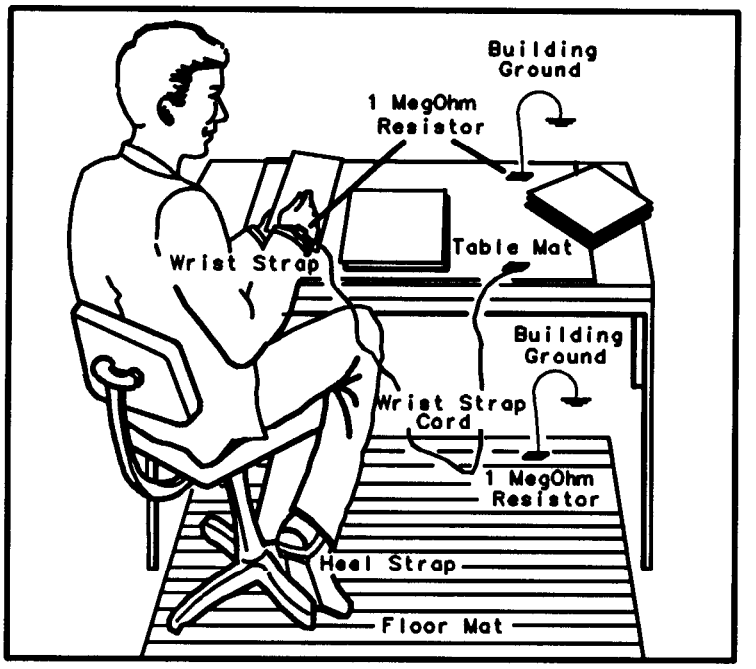
The two types must be used together to ensure adequate ESD protection.

**Warning** 

**These techniques for a static-safe work station should not be used when working on circuitry that has a voltage potential greater than 500 volts.**

For more information about preventing ESD damage, contact the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Association, Inc. The ESD standards developed by this agency are sanctioned by the American National Standards Institute (ANSI).

**Table 7-1. Static-Safe Accessories**




FORMAT46

**Figure 7- 1.**

| HP Part Number | Description |
|---|---|
| 9300-0797 | Set includes: 3M static control mat 0.6 m x 1.2 m (2 ft x 4 ft) and 4.6 cm (16 ft) ground wire. (The wrist-strap and wrist-strap cord are not included. They must be ordered separately.) |
| 9300-0980 | Wrist-strap cord 1.5 m (5 ft) |
| 9300-1383 | Wrist-strap, color black, stainless steel, without cord, has four adjustable links and a 7 mm post-type connection. |
| 9300-1169 | ESD heel-strap (reusable 6 to 12 months). |

## Assembly Removal Diagrams

The following diagrams illustrate the steps required to remove the **A16** Power Supply Board assembly, and the correct **S1** Line Switch assembly cable connections.

### A16 Power Supply Board Removal Diagram

The following diagram and procedure illustrate how to remove the **A16** Power Supply Board assembly from the tracking source:

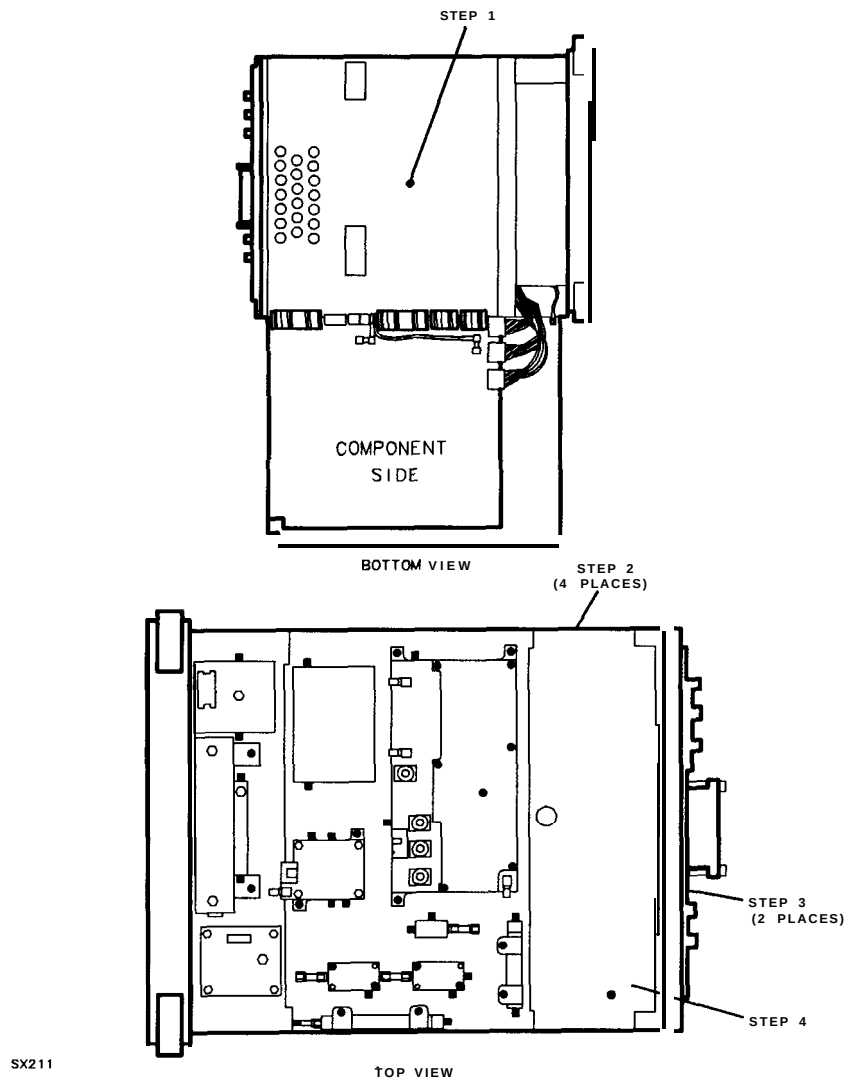



**Figure 7-2. A16 Power Supply Board Assembly Removal**

1. Remove the screw that secures the power supply board assembly to the center deck.
2. Remove the four screws (two each side) that secure the board assembly to the sides of the tracking source.

3. Remove the two screws that secure the board assembly to the rear frame.
4. Remove the power supply cover.

## Line-Switch Cable Connection Diagram

It is necessary to disconnect the line switch cable **(W11)** from the front-panel switch **(S1)** when removing the instrument front panel or replacing **S1** or **W11.** The following diagram illustrates the correct line-switch cable connection when replacing these assemblies.

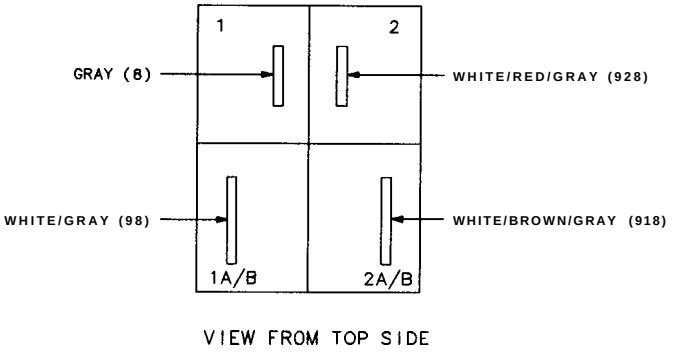



**Figure 7-3. Line-Switch Cable Connection**

## Replaceable Parts

This section contains information for identifying and ordering replacement assemblies for the HP 85644A/85645A tracking source. Major assembly and cable location information is given in Chapter 8.

Table 7-1 defines the reference designations, abbreviations, and multipliers used in the parts tables

Tables 7-2 and 7-3 list the following information for each major assembly and for each electrical part that is not part of a major assembly:

1. Assembly reference designation.
2. Hewlett-Packard part number.
3. Part number check digit (CD).
4. Description of the assembly.

Tables 7-4 through 7-6 list the following information for each replaceable mechanical and hardware part that is not part of a major assembly:

1. Hewlett-Packard part number.
2. Part number check digit (CD).
3. Description of the assembly.

## Table 7-2. Reference Designations, Abbreviations, and Multipliers (1 of 4)

### REFERENCE DESIGNATIONS

| | | |
|---|---|---|
| A Assembly | F Fuse | RT Thermistor |
| AT Attenuator, Isolator, Limiter, lbrmination | FL Filter | S Switch |
| B Fan, Motor | HY Circulator | T Transformer |
| BT Battery | J Electrical Connector (Stationary Portion), Jack | TB Terminal Board |
| C Capacitor | K Relay | TC Thermocouple |
| CP Coupler | L Coil, Inductor | TP Test Point |
| CR Diode, Diode Thyristor, Step Recovery Diode, Varactor | M Meter | U Integrated Circuit, Microcircuit |
| DC Directional Coupler | MP Miscellaneous Mechanical Part | V Electron Tube |
| DL Delay Line | P Electrical Connector (Movable Portion), Plug | VR Breakdown Diode (Zener), Voltage Regulator |
| DS Annunciator, Lamp, Light Emitting Diode (LED), Signaling Device (Visible) | Q Silicon Controlled Rectifier (SCR), Transistor, Triode Thyristor | W Cable, Wire, Jumper |
| E Miscellaneous Electrical Par | R Resistor | X Socket |
| | | Y crystalunit (Piezoelectric, Quartz) |
| | | Z Tuned Cavity, Tuned Circuit |

### ABBREVIATIONS

| A | | |
|---|---|---|
| 4 Across Flats, Acrylic, Air (Dry Method), Ampere | BSC Basic | CNDCT Conducting, Conductive, Conductivity, Conductor |
| ADJ Adjust, Adjustment | BTN Button | CONT Contact, Continuous, Control, Controller |
| ANSI American National Standards Institute (formerly USASI-ASA) | c | CGNV Converter |
| ASSY Assembly | C Capacitance, Capacitor, Center Tapped, Cermet, Cold, Compression | CPRSN Compression |
| AWG American Wire Gage | CCP Carbon Composition Plastic | CUP-PT Cup Point |
| | CD Cadmium, Card, Cord | c w Clockwise, Continuous Wave |
| B | CER Ceramic | |
| BCD Binary Coded Decimal | CHAM Chamfer | |
| BD Board, Bundle | CHAR Character, Characteristic, Charcoal | D |
| BE-CU Beryllium Copper | CMOS Complementary Metal Oxide Semiconductor | D Deep, Depletion, Depth, Diameter Direct Current |
| BNC Type of Connector | | DA Darlington |
| BRG Bearing Boring | | |
| BRS Brass | | |

## Table 7-2. Reference Designations, Abbreviations, and Multipliers (2 of 4)

**ABBREVIATIONS**

| | | | | | |
|---|---|---|---|---|---|
| DAP-GL | Diallyl Phthalate Glass | FT | Current Gain Bandwidth Product (Transition Frequency), Feet, Foot | JFET | Junction Field Effect Transistor |
| DBL | Double | | | | |
| DCDR | Decoder | | | | **K** |
| DEG | Degree | | | | |
| D-HOLE | D-Shaped Hole | FXD | Fixed | K | Kelvin, Key, Kilo, Potassium |
| DIA | Diameter | | | | |
| DIP | Dual In-Line Package | | G | KNRLD | Knurled |
| DIP-SLDR | Dip Solder | | | KVDC | Kilovolts |
| D-MODE | Depletion Mode | GEN | General, Generator | | Direct Current |
| DO | Package Type Desiguation | GND | Ground | | |
| | | GP | General Purpose, Group | | **L** |
| DP | Deep, Depth, Diametric Pitch, Dip | | | LED | Light Emitting Diode |
| DP3T | Double Pole Three Throw | | **H** | LG | Length, Long |
| | | | | LIN | Linear, Linearity |
| DPDT | Double Pole Double Throw | H | Henry, High | LK | Link, Lock |
| | | HDW | Hardware | LKG | Leakage, Locking |
| DWL | Dowell | HEX | Hexadecimal, Hexagon, Hexagonal | LUM | Luminous |
| | **E** | | | | |
| | | HLCL | Helical | | |
| E-R | E-Ring | HP | Hewlett-Packard Company, High Pass | | **M** |
| EXT | Extended, Extension External, Extinguish | | | M | Male, Maximum, Mega, Mil, Milli, Mode |
| | | | **I** | | |
| | **F** | | | | |
| | | IC | Collector Current, Integrated Circuit | MA | Milliampere |
| F | Fahrenheit, Farad, Female, Fihu (Resistor), Fixed, Flange, Frequency | | | MACH | Machined |
| | | ID | Identification, Inside Diameter | MAX | Maximum |
| | | | | MC | Molded Carbon Composition |
| FC | Carbon Film/ Composition, Edge of Cutoff Frequency, Face | IF | Forward Current, Intermediate Frequency | MET | Metal, Metallized |
| | | | | MHZ | Megahertz |
| | | IN | Inch | MINTR | Miniature |
| FDTHRU | Feedthrough | INCL | Including | MIT | Miter |
| FEM | Female | INT | Integral, Intensity, Internal | MLD | Mold, Molded |
| FIL-HD | Fillister Head | | | MM | Magnetized Material, Millimeter |
| FL | Flash, Fiat, Fluid | | **J** | MOM | Momentary |
| FLAT-PT | Flat Point | | | MTG | Mounting |
| FR | Front | J-FET | Junction Field Effect Transiior | MTLC | Metallic |
| FREQ | Frequency | | | MW | Miiwatt |

**Table 7-2. Reference Designations, Abbreviations, and Multipliers (3 of 4)**

**ABBREVIATIONS**

| | |
|---|---|
| | **N** |
| **N** | Nano, None |
| **N-CHAN** | N-Channel |
| NH | Nanohenry |
| NM | Nanometer, Nonmetallic |
| NO | Normally Open, Number |
| **NOM** | Nominal |
| NPN | Negative Positive Negative **(Transistor** |
| NS | Nanosecond, Non-Shorting, Nose |
| NUM | Numeric |
| NYL | Nylon (Polyamide) |
| | 0 |
| OA | Over-All |
| OD | Outside Diameter |
| OP AMP | Operational Amplifier |
| OPT | Optical, Option, Optional |
| | **P** |
| PA | **Picoampere,** Power Amplifier |
| PAN-HD | Pan Head |
| PAR | Parallel, **Parity** |
| PB | Lead (Metal), Pushbutton |
| PC | Printed Circuit |
| PCB | Printed Circuit Board |
| **P-CHAN** | P-Channel |
| PD | Pad, Power Dissipation |
| PF | Picofarad, Power Factor |
| PKG | Package |
| **PLSTC** | Plastic |
| PNL | Panel |
| PNP | Positive **Negative** Positive (Transistor: |
| **POLYC** | Polycarbonate |
| **POLYE** | Polyester |
| POT | Potentiometer |
| POZI | Pozidriv Recess |
| PREC | Precision |
| PRP | **Purple, Purpose** |
| **PSTN** | Piston |
| PT | Part, Point, Pulse Time |
| **PW** | Pulse Width |
| | **Q** |
| Q | Figure of **Merit** |
| | **R** |
| **R** | **Range, Red,** Resistance, Resistor |
| | **Right,** Ring |
| REF | Reference |
| RES | Resistance, Resistor |
| RF | Radio Frequency |
| RGD | Rigid |
| **RND** | Round |
| RR | Rear |
| **RVT** | Rivet, Riveted |
| | **S** |
| **SAWR** | Surface Acoustic Wave Resonator |
| **SEG** | Segment |
| **SGL** | Single |
| **SI** | Silicon, Square Inch |
| **SL** | Slide, Slow |
| **SLT** | Slot, Slotted |
| **SMA** | Subminiature, **A Type (Threade Connector)** |
| SMB | Subminiature, **B Type (Slip-on** Connector) |
| **SMC** | **Subminiature,** C-Type **(Threade** Connector) |
| **SPCG** | **Spacing** |
| SPDT | Single Pole Double Throw |
| **SPST** | Single Pole Single Throw |
| **SQ** | **Square** |
| ssl! | Stainless Steel |
| **STL** | Steel |
| SUBMIN | Subminiature |
| **SZ** | **Size** |
| | **T** |
| **T** | Teeth, Temperature, Thickness, Time, Timed, lboth, **Typical** |
| **TA** | Ambient Temperature, **Tantalum** |
| **TC** | **Temperature Coefficient** |
| THD | Thread, Threaded |
| **THK** | Thick |
| **TO** | **Package Type** Designation |
| **TPG** | **Tapping** |
| **TR-HD** | Truss Head |
| **TRMR** | Trimmer |
| **TRN** | Turn, Turns |
| **TRSN** | **Torsion** |

**Table 7-2. Reference Designations, Abbreviations, and Multipliers (4 of 4)**

**ABBREVIATIONS**

**U**

UCD Microcandela
UF Microfarad
UH Microhenry
UL Microliter, Underwriters' Laboratories, Inc.
UNHDND Unhardened

**V**

V Variable, Violet, Volt, Voltage
VAC vacuum, Volts—Alternating Current
VAR Variable
VDC Volts-Direct Current

**W**

W Watt, Wattage, White, Wide, Width
W/SW With Switch
WW Wire Wound

**X**

X By (Used with Dimensions), Reactance

Y

YIG Yttrium-Iron-Garnet

**Z**

ZNR Zener

**MULTIPLIERS**

| Abbreviation | Prefix | Multiple | Abbreviation | Prefix | Multiple |
|---|---|---|---|---|---|
| T | tera | $10^{12}$ | m | milli | $10^{-3}$ |
| G | giga | $10^{9}$ | $\mu$ | micro | $10^{-6}$ |
| M | mega | $10^{6}$ | n | nano | $10^{-9}$ |
| k | kilo | $10^{3}$ | p | pico | $10^{-12}$ |
| da | deka | 10 | f | femto | $10^{-15}$ |
| d | deci | $10^{-1}$ | a | atto | $10^{-18}$ |
| c | centi | $10^{-2}$ | | | |

## Table 7-3. HP 85644A Assembly-Level Replaceable Parts (1 of 2)

| Reference Designator | HP Part Number | CD | Description |
|---|---|---|---|
| A1 | * | | BOARD ASSEMBLY, FRONT-PANEL |
| A2 | * | | BOARD ASSEMBLY, CONTROLLER |
| A3 | * | | BOARD ASSEMBLY, RF |
| A4 | 60867541 | 5 | YIG-TUNED OSCILLATOR |
| A5 | 60867878 | 0 | ATTENUATOR, 0.6 GHZ |
| | 60866876 | 7 | REBUILT ATTENUATOR, 6.6 GHZ |
| A6 | | | NOT ASSIGNED |
| A7 | | | NOT ASSIGNED |
| A8 | | | NOT ASSIGNED |
| A9 | 5086-7862 | 3 | MODULATOR/AMPLIFIER |
| | 5086-6862 | 1 | REBUILT MODULATOR/AMPLIFIER |
| A10 | | | NOT ASSIGNED |
| A11 | 5086-7886 | 1 | DETECTOR |
| A12 | 0955-0332 | 6 | AMPLIFIER, 13 DBM, 3-6 GHZ |
| A13 | 0955-0332 | 6 | AMPLIFIER, 13 DBM, 3-6 GHZ |
| A14 | 0955-0547 | 5 | MIXER, 13 DB, 2-7 GHZ |
| A15 | 5086-7861 | 2 | LOWBAND ASSEMBLY |
| | 5086-6861 | 0 | REBUILT LOWBAND ASSEMBLY |
| A16 | * | | BOARD ASSEMBLY, POWER SUPPLY |
| A17 | * | | BOARD ASSEMBLY, HP-IB INTERFACE |
| A18 | 0955-0545 | 3 | FILTER, LOW PASS 6 GHZ |
| A19 | 0955-0487 | 2 | FILTER, LOW PASS 1 GHZ |
| A20 | 5062-8243 | 6 | FILTER ASSEMBLY, LINE |
| AT1 | 0955-0209 | 6 | ATTENUATOR, 6 DB, 8 GHZ |
| AT2 | 0955-0536 | 2 | ATTENUATOR, 6 DB, 8 GHZ |
| AT3 | 0955-0537 | 3 | ATTENUATOR, 30 DB, 8 GHZ |
| F1 | 2110-0756 | 3 | FUSE, 6.0 AMP 250V |
| | 2110-0709 | 3 | FUSE, 6.0 AMP 250V (ALTERNATE) |
| B1 | 5062-8244 | 6 | FANASSEMBLY |
| BT1 | 1420-0341 | 5 | BATTERY, 3.0 V, 1.2 AMP HOURS |
| J1 | 1250-2191 | 6 | CONNECTOR, RF OUTPUT, FRONT PANEL |
| J2 | 1250-1666 | 8 | CONNECTOR, LO INPUT, FRONT PANEL |
| J3 | 1250-1666 | 8 | CONNECTOR, LO OUTPUT, FRONT PANEL |
| J4 | P/O W14 | | CONNECTOR, 10 MHZ REF IN, REAR PANEL |
| J5 | P/O W20 | | CONNECTOR, SWEEP + TUNE IN, REAR PANEL |
| J6 | P/O W16 | | CONNECTOR, EXTERNAL ALC, REAR PANEL |
| S1 | 3101-3108 | 4 | SWITCH, ROCKER DPST |

Refer to Table 7-8 for current HP pert number.

**Table 7-3. HP 85644A Assembly-Level Replaceable Parts (2 of 2)**

| Reference Designator | HP Part Number | CD | Description |
|---|---|---|---|
| W1 | 5062-7066 | 0 | CABLE ASSY, CONTROL, A2J1 TO A3J1 |
| W2 | 60624877 | 4 | CABLE ASSY, DISPLAY VIDEO, A3J7 TO Al FRONT PANEL |
| W3 | 5062-7067 | 0 | CABLE ASSY, A3J6 TO Al FRONT PANEL |
| W4 | 5062-4879 | 6 | CABLE ASSY, A3J8 TO A5J3 |
| W5 | 60624884 | 3 | CABLE ASSY, LOW BAND, A3J9 TO A15J1 |
| W6 | | | NOT ASSIGNED |
| W7 | 60624881 | 0 | CABLE ASSY, OSCILLATOR, A2J2 TO A4 |
| W8 | 5062-4876 | 3 | CABLE ASSY, POWER SUPPLY OUTPUT, A16J1 TO A3J2 |
| w o | 60624886 | 4 | CABLE ASSY, LEVELING AMPLIFIER CONTROL, A3 TO A12 AND A13 |
| W10 | 60624880 | 9 | CABLE ASSY, A3J3/A2J3 TO A9 |
| W11 | 5062-7756 | 4 | CABLE ASSY, S1 TO A16J2 |
| W12 | 85645-60013 | 4 | CABLE ASSY, A3J11 TO All |
| W13 | | | NOT ASSIGNED |
| W14 | 60624897 | 8 | CABLE ASSY, 10 MHZ IN, A2J601 TO REAR-PANEL J4 |
| W15 | 85645-60015 | 6 | CABLE ASSY, A15J3 TO A2J602 |
| W16 | 85645-60012 | 3 | CABLE ASSY, EXTERNAL ALC, A2J503 TO REAR- PANEL J6 |
| W17 | 85644-60004 | 2 | CABLE ASSY, A9J4 TO A2J501 |
| W18 | 85645-60017 | 8 | CABLE ASSY, A15J4 TO A2J502 |
| W19 | 85645-60018 | 0 | CABLE ASSY, A15J17 TO A2J505 |
| W20 | 8120-5506 | 6 | CABLE ASSY, SWEEP + TUNE OUTPUT, A2J101 TO REAR-PANEL J5 |
| W21 | 85645-60010 | 1 | CABLE ASSY, 6 GHZ LPF, A2J103 TO A19 |
| W22 | 602 1-9333 | 1 | CABLE ASSY, LO IN/LVL, FRONT-PANEL J2 TO AT1 |
| W23 | 5021-9334 | 2 | CABLE ASSY, LO OUT/LVL, FRONT-PANEL J3 TO A12 |
| W24 | 5021-9336 | 4 | CABLE ASSY, LEVELING AMP OUTPUT, A13 TO AT3 |
| W25 | 5021-9335 | 3 | CABLE ASSY, LPF OUTPUT, A18 TO A13 |
| W26 | 5021-9338 | 6 | CABLE ASSY, MIXER, A14 TO A9 |
| W27 | 502 1-9337 | 1 | CABLE ASSY, 1 GHZ LPF OUTPUT, A19 TO A14 |
| W28 | 5021-9339 | 7 | CABLE ASSY, YTO OUTPUT, A4 TO A9 |
| W29 | | | NOT ASSIGNED |
| W30 | 5021-9341 | 1 | CABLE ASSY, LOW BAND INPUT, A9 TO A15J21 |
| W31-W34 | | | NOT ASSIGNED |
| W35 | 5021-9927 | 9 | CABLE ASSY, RF OUTPUT, A5 TO FRONT-PANEL J1 |
| W36 | 5022-0094 | 5 | CABLE ASSY, MOD AMP OUTPUT, A9 TO A5 |
| W37 | 5022-0095 | 6 | CABLE ASSY, LO BAND OUTPUT, A9 TO A15J22 |

## Table 7-4. HP 85645A Assembly-Level Replaceable Parts (1 of 2)

| Reference Designator | HP Part Number | CD | Description |
|---|---|---|---|
| A l | · | | BOARD ASSEMBLY, FRONT-PANEL |
| A2 | • | | BOARD ASSEMBLY, CONTROLLER |
| A3 | * | | BOARD ASSEMBLY, RF |
| A4 | 5086-7541 | 5 | YIG-TUNED OSCILLATOR |
| AS | 50867874 | 7 | ATTENUATOR |
| | 5086-6874 | 5 | REBUILT ATTENUATOR, 26.5 GHZ |
| A6 | 5086-7556 | 2 | SWITCHED YIG-TUNED MULTIPLIER (SYTM) |
| | 5086-6556 | 0 | REBUILT SWITCHED YIG-TUNED MULTIPLIER (SYTM) |
| A7 | 0955-0125 | 5 | COUPLER, 16 DB, 2-26.5 GHZ |
| A8 | 5086-7887 | 2 | DETECTOR, 26.5 GHZ |
| A9 | 5086-7862 | 3 | MODULATOR/AMPLIFIER |
| | 5086-6862 | 1 | REBUILT MODULATOR/AMPLIFIER |
| A10 | 0955-0475 | 8 | ISOLATOR, 20 DB, 2-7 GHZ |
| A l l | 5086-7886 | 1 | DETECTOR |
| A12 | 0955-0332 | 6 | AMPLIFIER, 13 DBM, 3-6 GHZ |
| A13 | 0955-0332 | 6 | AMPLIFIER, 13 DBM, 3-6 GHZ |
| A14 | 0955-0547 | 5 | MIXER, 13 DB, 2-7 GHZ |
| A15 | 5086-7861 | 2 | MWBAND ASSEMBLY |
| | 5086-6861 | 0 | REBUILT LOWBAND ASSEMBLY |
| A16 | * | | BOARD ASSEMBLY, POWER SUPPLY |
| A17 | • | | BOARD ASSEMBLY, HP-IB INTERFACE |
| A18 | 0955-0545 | 3 | FILTER, LOW PASS 5 GHZ |
| A19 | 0955-0487 | 2 | FILTER, LOW PASS 1 GHZ |
| A20 | 5062-8243 | 6 | FILTER ASSEMBLY, LINE |
| AT1 | 09559209 | 6 | ATTENUATOR, 6 DB, 8 GHZ |
| AT2 | 0955-0536 | 2 | ATTENUATOR, 6 DB, 8 GHZ |
| AT3 | 0955-0537 | 3 | ATTENUATOR, 30 DB, 8 GHZ |
| F1 | 2110-0756 | 3 | FUSE, 5.0 AMP 250V |
| | 2110-0709 | 3 | FUSE, 5.0 AMP 250V (ALTERNATE) |
| B1 | 5062-8244 | 7 | FAN ASSEMBLY |
| BT1 | 1420-0341 | 5 | BATTERY, 3.0 V, 1.2 AMP HOURS |
| J1 | 08673-60040 | 9 | CONNECTOR, RF OUTPUT, FRONT PANEL |
| J2 | 1250-1666 | 8 | CONNECTOR, LO INPUT, FRONT PANEL |
| J3 | 1250-1666 | 8 | CONNECTOR, LO OUTPUT, FRONT PANEL |
| J4 | P/O W14 | | CONNECTOR, 10 MHZ REF IN, REAR PANEL |
| J5 | P/O W20 | | CONNECTOR, SWEEP + TUNE IN, REAR PANEL |
| J6 | P/O W16 | | CONNECTOR, EXTERNAL ALC, REAR PANEL |
| S1 | 3101-3108 | 4 | SWITCH, ROCKER DPST |

' Refer to Table 7-8 for current HP pert number.

**Table 7-4. HP 85645A Assembly-Level Replaceable Parts (2 of 2)**

| Reference Designator | HP Part Number | CD | Description |
|---|---|---|---|
| W1 | 5062-7066 | 9 | CABLE ASSY, CONTROL, A2J1 TO A3J5 |
| W2 | 50624877 | 4 | CABLE ASSY, DISPLAY VIDEO, A3J7 TO Al FRONT PANEL |
| W3 | 5062-7067 | 0 | CABLE ASSY, A3J6 TO Al FRONT PANEL |
| W4 | 50624879 | 6 | CABLE ASS-Y, A3J8 TO A5J3 |
| W5 | 50624884 | 3 | CABLE ASSY, LOW BAND, A3J9 TO A15J1 |
| W6 | 60624882 | 1 | CABLE ASSY, SYTM, A6J1 TO A3J10 |
| W7 | 50624881 | 0 | CABLE ASSY, OSCILLATOR, A2J2 TO A4 |
| W8 | 50624876 | 3 | CABLE ASSY, POWER SUPPLY OUTPUT, A16J1 TO A3J2 |
| W9 | 50624885 | 4 | CABLE ASSY, LEVELING AMPLIFIER CONTROL, A3 TO A12 AND A13 |
| W10 | 50624880 | 9 | CABLE ASSY, A3J3/A2J3 TO A9 |
| W11 | 5062-7756 | 4 | CABLE ASSY, S1 TO A16J2 |
| W12 | 85645-60013 | 4 | CABLE ASSY, A3J11 TO All |
| W13 | 85645-60014 | 6 | CABLE ASSY, A9J2 TO A3J12 |
| W14 | 5062-4897 | 8 | CABLE ASSY, 10 MHZ IN, A2J601 TO REAR-PANEL J4 |
| W15 | 85645-60015 | 6 | CABLE ASSY, A15J3 TO A2J602 |
| W16 | 85645-60012 | 3 | CABLE ASSY, EXTERNAL ALC, A2J503 TO REAR- PANEL J6 |
| W17 | 85645-60016 | 7 | CABLE ASSY, A8 TO A2J501 |
| W18 | 85645-60017 | 8 | CABLE ASSY, A15J4 TO A2J502 |
| W19 | 85645-60018 | 9 | CABLE ASSY, A15J17 TO A2J505 |
| W20 | 86645-60011 | 2 | CABLE ASSY, SWEEP + TUNE OUTPUT, A2J101 TO REAR-PANEL J5 |
| W21 | 85645-60010 | 1 | CABLE ASSY, 6 GHZ LPF, A2J103 TO A19 |
| W22 | 5021-9333 | 1 | CABLE ASSY, LO IN/LVL, FRONT-PANEL J2 TO AT1 |
| W23 | 5021-9334 | 2 | CABLE ASSY, LO OUT/LVL, FRONT-PANEL J3 TO A12 |
| W24 | 5021-9336 | 4 | CABLE ASSY, LEVELING AMP OUTPUT, A13 TO AT3 |
| W25 | 5021-9335 | 3 | CABLE ASSY, LPF OUTPUT, A18 TO A13 |
| W26 | 5021-9338 | 6 | CABLE ASSY, MIXER, A14 TO A9 |
| W27 | 5021-9337 | 5 | CABLE ASSY, 1 GHZ LPF OUTPUT, A19 TO A14 |
| W28 | 5021-9339 | 7 | CABLE ASSY, YTO OUTPUT, A4 TO A9 |
| W29 | 5021-9340 | 0 | CABLE ASSY, MOD AMP OUTPUT, A9 TO A10 |
| W30 | 5021-9341 | 1 | CABLE ASSY, LOW BAND INPUT, A9 TO A15J21 |
| W31 | 5021-9342 | 2 | CABLE ASSY, HI BAND IN, A10 TO A6 |
| W32 | 5021-9926 | 8 | CABLE ASSY, LOW BAND IN, A6 TO A15J22 |
| W33 | 5021-9332 | 0 | CABLE ASSY, SYTM OUTPUT, A6 TO A7 |
| W34 | 5021-9331 | 9 | CABLE ASSY, COUPLER OUTPUT, A7 TO A5 |
| W35 | 5021-9927 | 9 | CABLE ASSY, RF OUTPUT, A5 TO FRONT-PANEL J1 |

**Table 7-5.**
**HP 85645A/85644A Cover Assembly Replaceable Parts**

| Description | HP Part Number | CD |
|---|---|---|
| COVER, INSTRUMENT | 5001-8771 | 7 |
| SIDE-TRIM | 5041-8901 | 9 |
| HANDLE | 5041-8911 | 1 |
| BACK-UP PLATE (FOR HANDLE) | 6001-8728 | 4 |
| GEAR SOCKET (FOR HANDLE) | 5021-6344 | 8 |
| GEAR RING (FOR HANDLE) | 5021-6343 | 7 |
| PLATE (FOR HANDLE) | 5021-8667 | 2 |
| SPRING, CPR (FOR HANDLE) | 1460-2164 | 8 |
| TRIM CAP (FOR HANDLE) | 5041-8912 | 2 |

**Table 7-6.**
**HP 85645A/85644A Miscellaneous Chassis Replaceable Parts**

| Decription | HP Part Number | CD |
|---|---|---|
| BRACKET, ATTENUATOR | 5002-0606 | 3 |
| FRONTBUMPER | 5041-8928 | 0 |
| COVER,POWERSUPPLY | 5002-0615 | 4 |
| DECK,CENTER | 5001-8775 | 1 |
| DECK, AUXILIARY | 5002-0605 | 2 |
| FRONTFRAME | 5021-8615 | 0 |
| FRONTPANEL | 85645-00002 | 5 |
| GASKET, EMI 3.97MDIA (3 FT) | 8160-0520 | 7 |
| GRILL,FAN | 3160-0309 | 6 |
| HINGE ASSEMBLY, TWO BOARD | 50623203 | 8 |
| KEYPAD | 5041-8960 | 0 |
| REARFRAME | 5021-8616 | 1 |
| REARPANEL,RIGHT | 5002-0658 | 5 |
| REAR PANEL, LEFT | 5002-0657 | 4 |
| FOOT, REAR | 5041-8929 | 1 |

**Table 7-7.**
**HP 85644A/85645A Miscellaneous Hardware Replaceable Parts**

| Qty | HP Part Number | CD | Description |
|---|---|---|---|
| 2 | 1400-1404 | 1 | CABLE CLIP, .5D .375W |
| 2 | 1400-1616 | 7 | CABLE CLIP, .38D .38W |
| 3 | 1400-0249 | 1 | CABLE TIE, .062E.09W |
| 7 | 2950-0035 | 8 | NUT, HEX 15/32-32 |
| 4 | 0535-0082 | 3 | NUT, LKWR M4 |
| 2 | 2950-0007 | 4 | NUT, HEX 5/16-32 |
| 2 | 0515-0314 | 2 | SCREW, SM 2-56 .188FLTX |
| 2 | 0515-0661 | 2 | SCREW, SMM2.0 CWPNTX |
| 4 | 0515-1992 | 4 | SCREW, SMM2.5 20 CWPNTX |
| 2 | 0515-1934 | 4 | SCREW, SMM2.5 6 CWPNTX |
| 2 | 0515-2001 | 8 | SCREW, SMM2.5 10 FLTRX |
| 4 | 0515-2194 | 0 | SCREW, SMM3.0 50 CWPNTX |
| 21 | 0515-0372 | 2 | SCREW, SMM3.0 8 CWPNTX |
| 13 | 0515-1035 | 6 | SCREW, SMM3.0 8 FLTRX |
| 6 | 0515-1349 | 5 | SCREW, SMM3.0 30 CWPNTX |
| 12 | 0515-0374 | 4 | SCREW, SMM3.0 10 CWPNTX |
| 2 | 0515-0375 | 6 | SCREW, SMM3.0 16 CWPNTX |
| 9 | 0616-0430 | 3 | SCREW, SMM3.0 6 CWPNTX |
| 3 | 0616-0468 | 6 | SCREW, SMM3.5 8 FLTRX |
| 8 | 0515-1101 | 7 | SCREW, SMM4.0 FLTRX |
| 6 | 0616-0433 | 6 | SCREW, SMM4.0 8 CWPNTX |
| 4 | 0515-2195 | 1 | SCREW, SMM4.0 40 CWPNTX |
| 4 | 0380-0012 | 0 | SPACER, .875L.181ID |
| 2 | 0380-1591 | 2 | STANDOFF, .188L 4-40 |
| 2 | 0380-0644 | 4 | STANDOFF, .327L 6-32 |
| 2 | 3050-1017 | 1 | WASHER, FL .324ID |
| 1 | 2190-0401 | 0 | WASHER,FL .120ID 4 |
| 1 | 3050-0890 | 6 | WASHER, FL M2.5ID |
| 2 | 2190-0024 | 3 | WASHER,LK .320ID |
| 2 | 00310-48801 | 0 | WASHER,SHOULDERED |

# Component-Level Information Packets

Component-level information is available for selected instrument assemblies The information for each repairable assembly is provided in the form of Component-Level Information packets (CLIPS).

A CLIP consists of a parts list, component-location diagram, and schematic diagram relating to a unique instrument assembly. An HP part number is assigned to each CLIP When an instrument assembly part number changes, a new CLIP is generated.

## Ordering CLIPs

For ordering convenience, current CLIPS for a specific instrument are combined into Component-Level Information binders. The current set of CLIPS contains information supporting the instrument assemblies manufactured at the time this manual was printed, plus a packet containing general CLIP information.

A complete set of CLIPs can be obtained by ordering the ***HP 85644A/85645A Tracking Source Component-Level Information*** binder, HP part number 85645-90007. Some CLIPS may not be available for recently introduced assemblies.

Updated or replacement CLIPs may be ordered through your local Hewlett-Packard Sales or Service office using the CLIP part number provided in Table 7-8. lb order ***General CLIP Information***, use HP part number 5958-7060.

CLIPS are packaged in protective plastic envelopes Accessories are available to use and store your CLIPs effectively (Refer to Table 7-9).

**Table 7-8.**
**HP 85644A/85645A Tracking Source Board Assembly, Serial Number, and CLIP Fart Number Cross-Reference**

| Assembly | Instrument Serial Prefix | Board Assembly Part Number | CLIP Part Number |
|---|---|---|---|
| Al Front-Panel | au | 85645-60001 | 85645-90013 |
| A2 RF | au | 8664560003 | 85645-90015 |
| A3 Controller *(HP 85644A only)* | au | 85644-60002 | 85644-90003 |
| A3 Controller *(HP 85645A only)* | au | 85645-60002 | 85645-90014 |
| A16 Power Supply | all | 85645-60006 | 8664590017 |
| A17 HP-IB I/O | au | 85645-60004 | 85645-90016 |

**Table 7-9.**
**Component-Level Information Packet Accessories**

| HP Part Number | Description |
|---|---|
| 9282-1134 | 2-1/2 inch CLIP binder (for 26 to 30 packets) |
| 9282-1133 | 2 inch CLIP binder (for 16 to 26 packets) |
| 9282-1132 | 1-1/2 inch CLIP binder (for fewer than 16 packets) |
| 9222-1636 | Replacement plastic CLIP envelope |

# 8

# Major Assembly and Cable Locations

## Introduction

The various assemblies and cables of the HP 85644A/85645A tracking source are illustrated in this chapter. Refer to Chapter 7, "Assembly Replacement," for part numbers, assembly descriptions, and ordering information.

## Contents

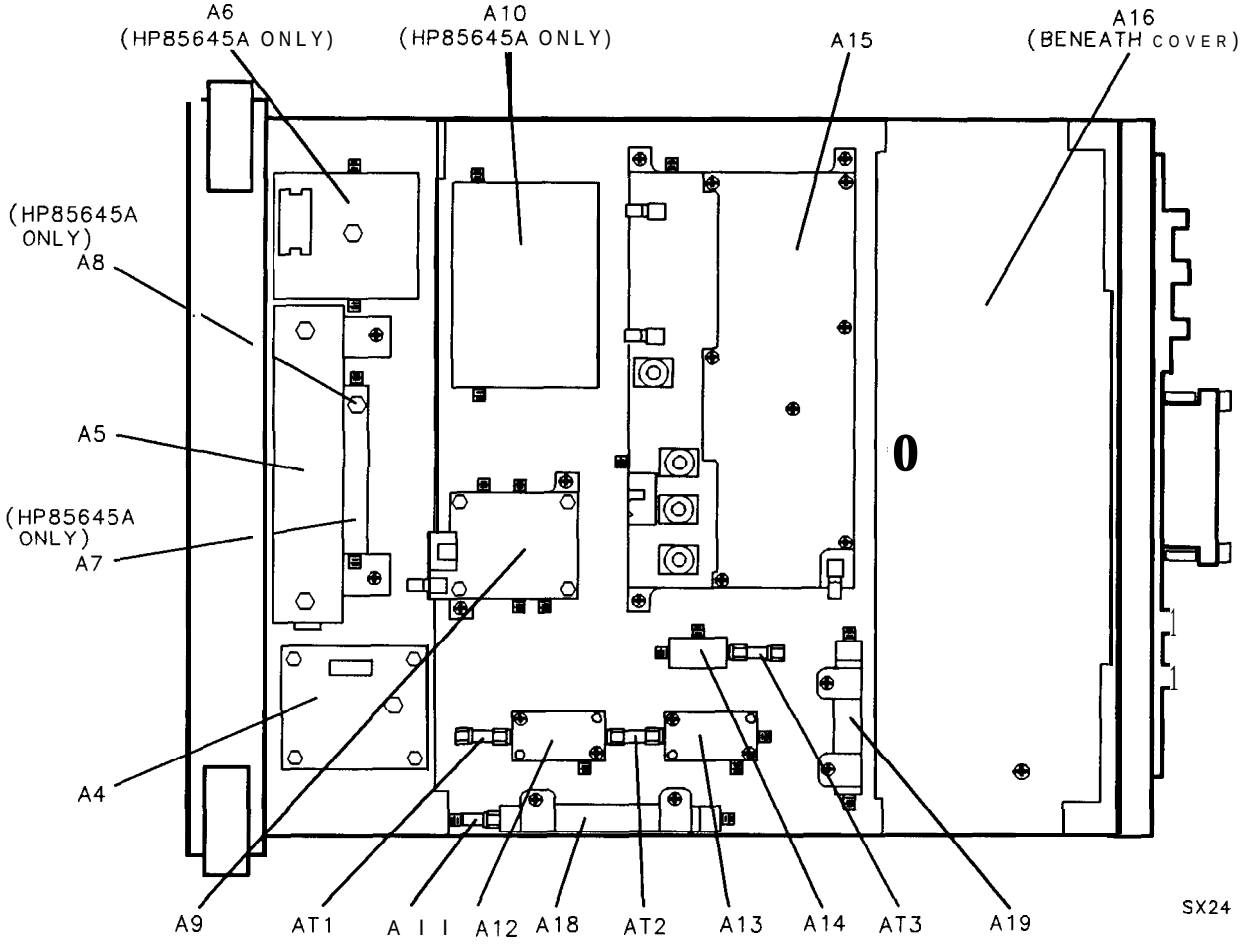
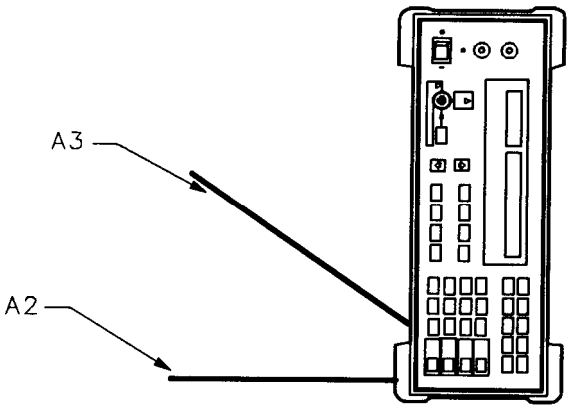



**Figure 8-1. HP 85644A/85645A Top View Assembly Locations**




SX27

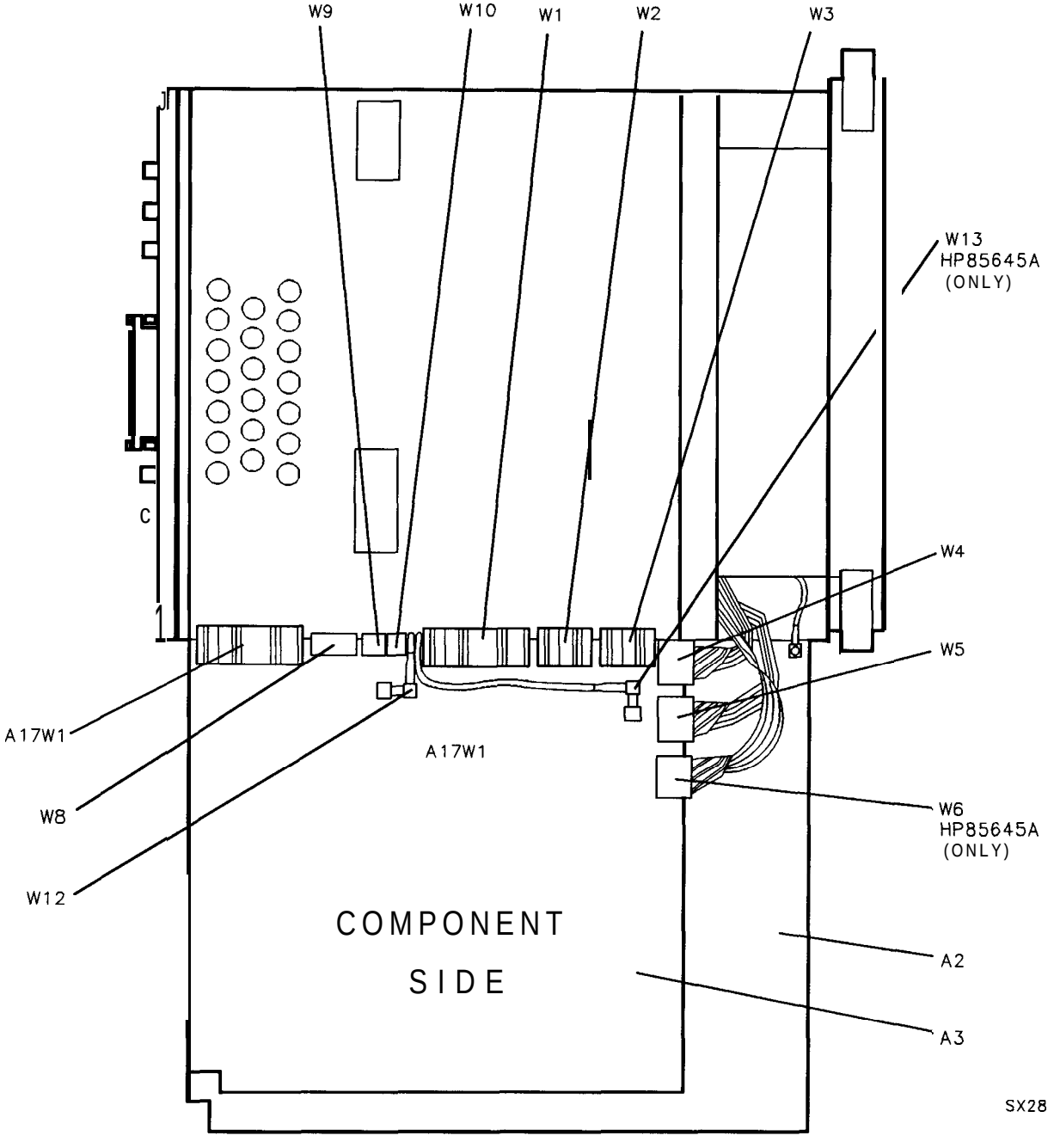



**Figure 8-2. HP 85644A/85645A Bottom View Assembly and Cable Locations (1 of 2)**

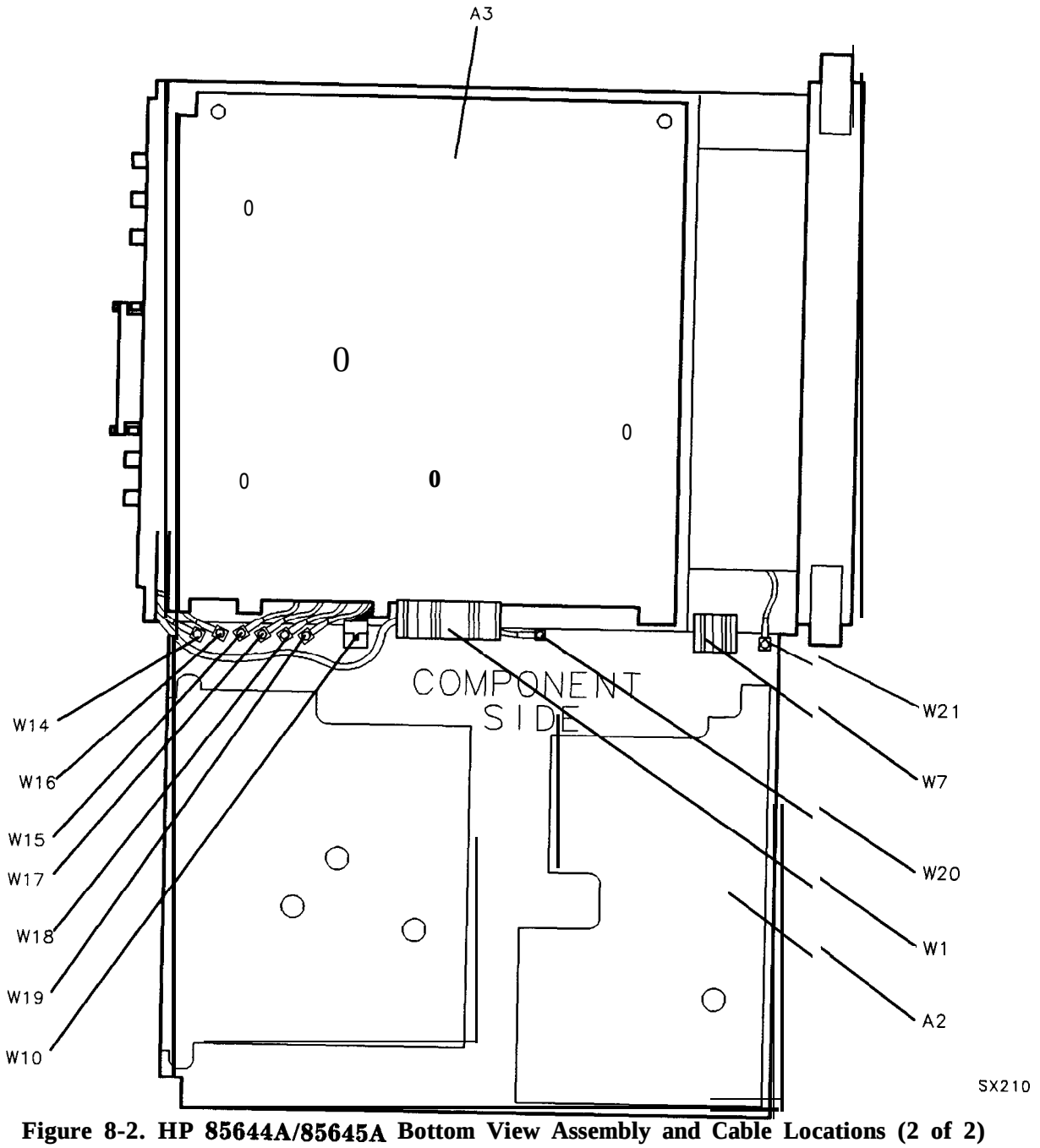



**Figure 8-2. HP 85644A/85645A Bottom View Assembly and Cable Locations (2 of 2)**

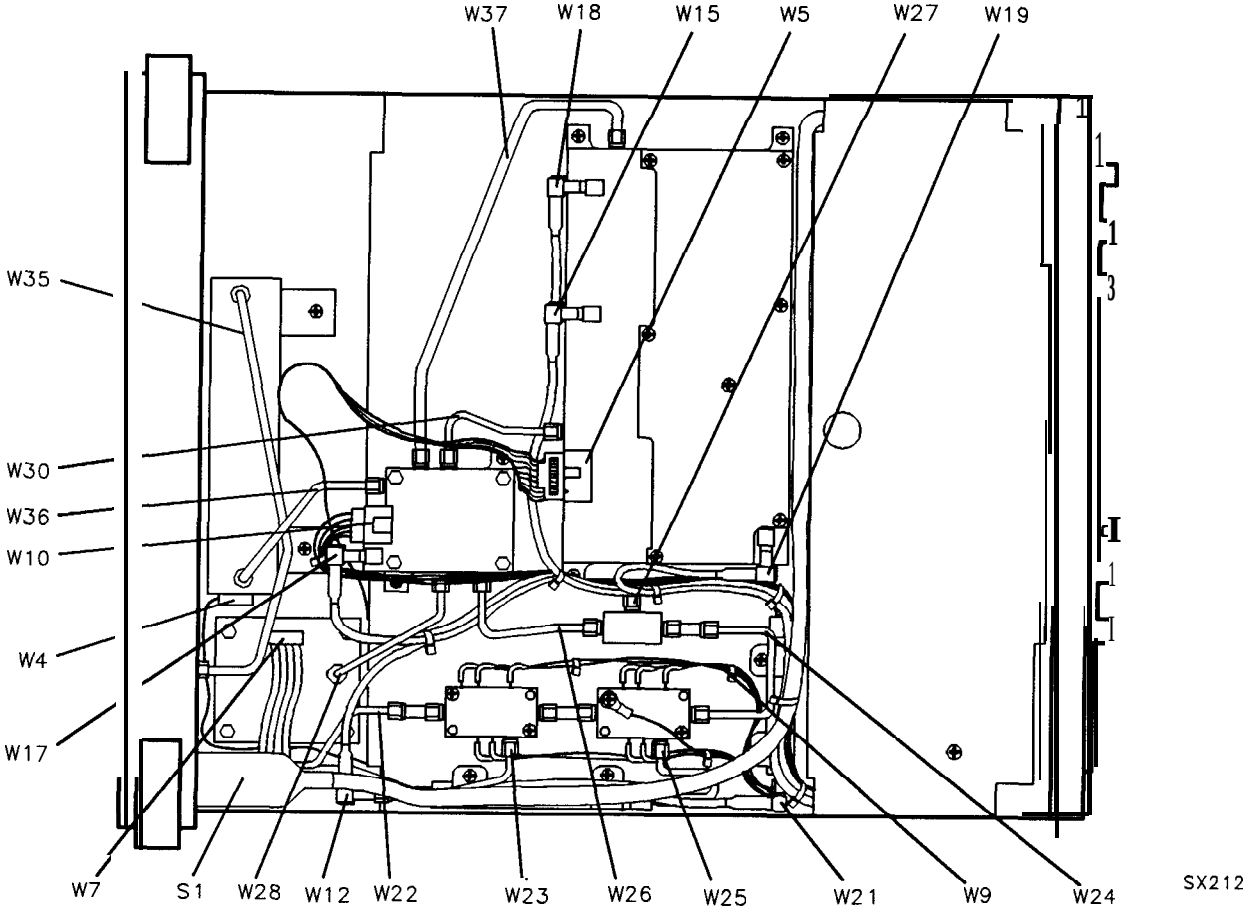



**Figure 8-3. HP 85644A Top View Cable Locations**

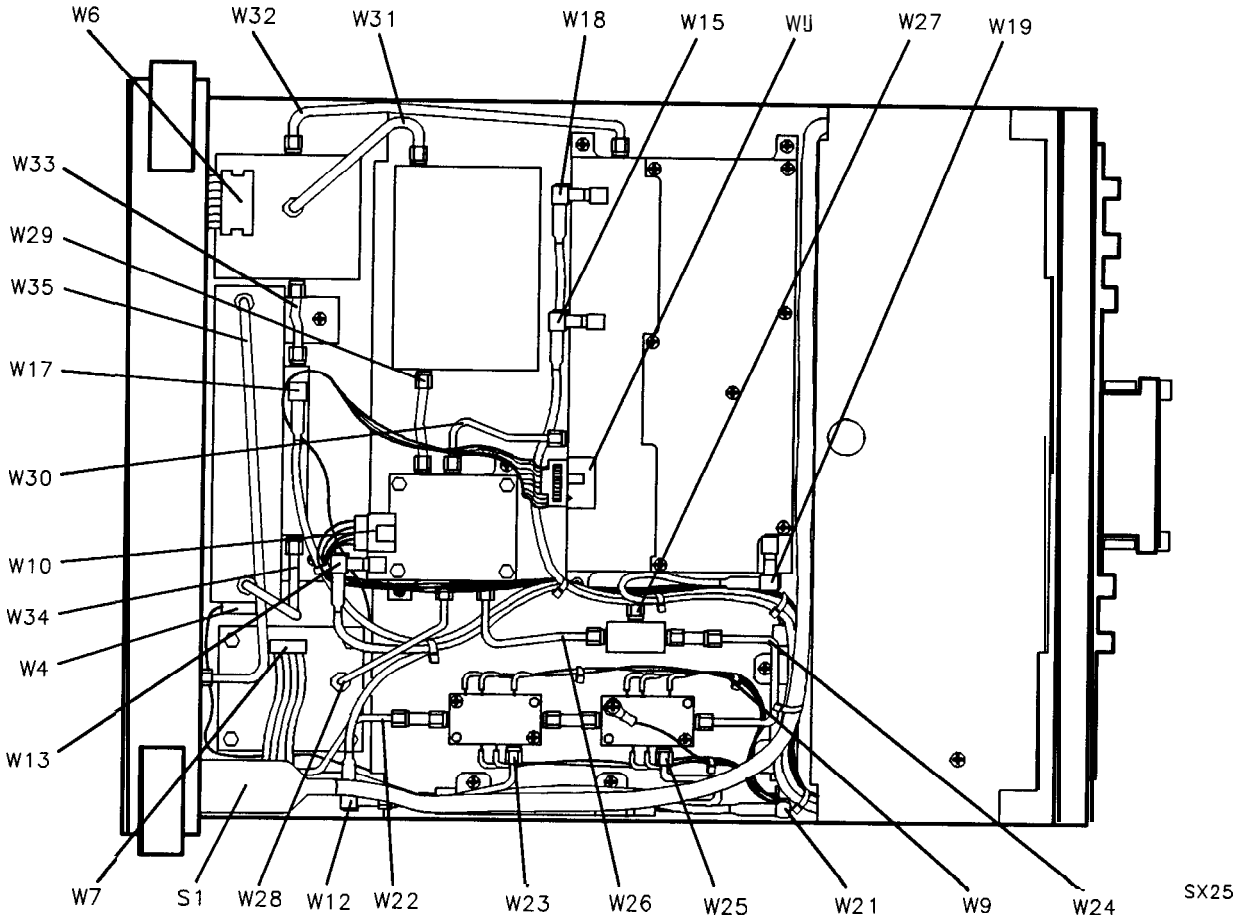



**Figure 8-4. HP 85645A Top View Cable Locations**