

FEATURES

- 125 MHz Clock Rate
- On-Chip High Performance DAC & High Speed Comparator
- DAC SFDR > 50 dB @ 40 MHz AOUT
- 32-Bit Frequency Tuning Word
- Simplified Control Interface: Parallel Byte or Serial Loading Format
- Phase Modulation Capability
- +3.3 V or +5 V Single Supply Operation
- Low Power: 380 mW @ 125 MHz (+5 V)
155 mW @ 110 MHz (+3.3 V)
- Power-Down Function
- Ultrasmall 28-Lead SSOP Packaging

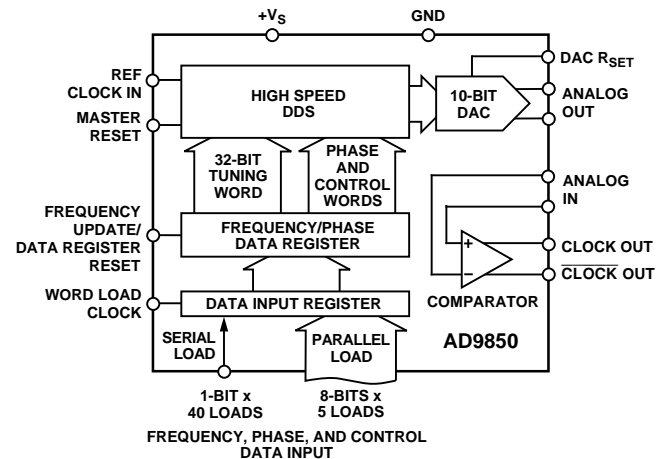
APPLICATIONS

- Frequency/Phase-Agile Sine-Wave Synthesis
- Clock Recovery and Locking Circuitry for Digital Communications
- Digitally Controlled ADC Encode Generator
- Agile Local Oscillator Applications

GENERAL DESCRIPTION

The AD9850 is a highly integrated device that uses advanced DDS technology, coupled with an internal high speed, high performance, D/A converter, and comparator, to form a complete digitally programmable frequency synthesizer and clock generator function. When referenced to an accurate clock source, the AD9850 generates a spectrally-pure, frequency/phase-programmable, analog output sine wave. This sine wave can be used directly as a frequency source, or converted to a square wave for agile-clock generator applications. The AD9850's innovative high speed DDS core provides a 32-bit frequency tuning word, which results in an output tuning resolution of 0.0291 Hz, for a 125 MHz reference clock input. The AD9850's circuit architecture allows the generation of output frequencies of up to one-half the reference clock frequency, or 62.5 MHz, and the output frequency can be digitally changed (asynchronously) at a rate of up to 23 million new frequencies per second. The device also provides 5 bits of digitally controlled

FUNCTIONAL BLOCK DIAGRAM



phase modulation which enables phase shifting of its output in increments of 180°, 90°, 45°, 22.5°, 11.25°, and any combination thereof. The AD9850 also contains a high speed comparator which can be configured to accept the (externally) filtered output of the DAC to generate a low jitter square wave output. This facilitates the device's use as an agile clock generator function.

The frequency tuning, control, and phase modulation words are loaded into the AD9850 via a parallel byte or serial loading format. The parallel load format consists of five iterative loads of an 8-bit control word (byte). The first byte controls phase modulation, power-down enable, and loading format; bytes 2-5 comprise the 32-bit frequency tuning word. Serial loading is accomplished via a 40-bit serial data stream on a single pin. The AD9850 Complete-DDS uses advanced CMOS technology to provide this breakthrough level of functionality and performance on just 155 mW of power dissipation (+3.3 V supply).

The AD9850 is available in a space saving 28-lead SSOP, surface mount package. It is specified to operate over the extended industrial temperature range of -40°C to +85°C.

REV. 0

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AD9850–SPECIFICATIONS ($V_S = +5\text{ V} \pm 5\%$ except as noted, $R_{SET} = 3.9\text{ k}\Omega$)

Parameter	Temp	Test Level	AD9850BRS			Units
			Min	Typ	Max	
CLOCK INPUT CHARACTERISTICS						
Frequency Range						
+5 V Supply	FULL	IV	1		125	MHz
+3.3 V Supply	FULL	IV	1		110	MHz
Pulse Width High/Low						
+5 V Supply	+25°C	IV	3.2			ns
+3.3 V Supply	+25°C	IV	4.1			ns
DAC OUTPUT CHARACTERISTICS						
Full-Scale Output Current						
$R_{SET} = 3.9\text{ k}\Omega$	+25°C	V		10.24		mA
$R_{SET} = 1.95\text{ k}\Omega$	+25°C	V		20.48		mA
Gain Error	+25°C	I	-10		+10	% FS
Gain Temperature Coefficient	FULL	V		150		ppm/°C
Output Offset	+25°C	I			10	μA
Output Offset Temperature Coefficient	FULL	V		50		nA/°C
Differential Nonlinearity	+25°C	I		0.5	0.75	LSB
Integral Nonlinearity	+25°C	I		0.5	1	LSB
Output Slew Rate (50 Ω , 2 pF Load)	+25°C	V		400		V/ μs
Output Impedance	+25°C	IV	50	120		k Ω
Output Capacitance	+25°C	IV			8	pF
Voltage Compliance	+25°C	I			1.5	V
Spurious-Free Dynamic Range (SFDR):						
Wideband (Nyquist Bandwidth)						
1 MHz Analog Out	+25°C	IV	63	72		dBc
20 MHz Analog Out	+25°C	IV	50	58		dBc
40 MHz Analog Out	+25°C	IV	46	54		dBc
Narrowband						
40.13579 MHz \pm 50 kHz	+25°C	IV		80		dBc
40.13579 MHz \pm 200 kHz	+25°C	IV		77		dBc
4.513579 MHz \pm 50 kHz/20.5 MHz CLK	+25°C	IV		84		dBc
4.513579 MHz \pm 200 kHz/20.5 MHz CLK	+25°C	IV		84		dBc
COMPARATOR INPUT CHARACTERISTICS						
Input Capacitance	+25°C	V		3		pF
Input Resistance	+25°C	IV	500			k Ω
Input Current	+25°C	I	-12		+12	μA
Input Voltage Range	+25°C	IV	0		V_{DD}	V
Comparator Offset*	FULL	VI	30		30	mV
COMPARATOR OUTPUT CHARACTERISTICS						
Logic "1" Voltage +5 V Supply	FULL	VI	+4.8			V
Logic "1" Voltage +3.3 V Supply	FULL	VI	+3.1			V
Logic "0" Voltage	FULL	VI			+0.4	V
Propagation Delay, +5 V Supply (15 pF Load)	+25°C	V		5.5		ns
Propagation Delay, +3.3 V Supply (15 pF Load)	+25°C	V		7		ns
Rise/Fall Time, +5 V Supply (15 pF Load)	+25°C	V		3		ns
Rise/Fall Time, +3.3 V Supply (15 pF Load)	+25°C	V		3.5		ns
Output Jitter (p-p)	+25°C	V		80		ps
CLOCK OUTPUT CHARACTERISTICS						
Clock Output Duty Cycle (Clk Gen. Config.)	+25°C	IV		50 \pm 10		%

Parameter	Temp	Test Level	AD9850BRS			Units
			Min	Typ	Max	
CMOS LOGIC INPUTS (Including CLKIN)						
Logic "1" Voltage, +5 V Supply	+25°C	I	3.5			V
Logic "1" Voltage, +3.3 V Supply	+25°C	I	3.0			V
Logic "0" Voltage	+25°C	I			0.4	V
Logic "1" Current	+25°C	I			12	μA
Logic "0" Current	+25°C	I			12	μA
Input Capacitance	+25°C	V		3		pF
POWER SUPPLY (AOUT = 1/3 CLKIN)						
+V _S Current @:						
62.5 MHz Clock, +3.3 V Supply	FULL	VI		30	48	mA
110 MHz Clock, +3.3 V Supply	FULL	VI		47	60	mA
62.5 MHz Clock, +5 V Supply	FULL	VI		44	64	mA
125 MHz Clock, +5 V Supply	FULL	VI		76	96	mA
P _{DISS} @:						
62.5 MHz Clock, +3.3 V Supply	FULL	VI		100	160	mW
110 MHz Clock, +3.3 V Supply	FULL	VI		155	200	mW
62.5 MHz Clock, +5 V Supply	FULL	VI		220	320	mW
125 MHz Clock, +5 V Supply	FULL	VI		380	480	mW
P _{DISS} Power-Down Mode						
+5 V Supply	FULL	V		30		mW
+3.3 V Supply	FULL	V		10		mW

NOTES

*Tested by measuring output duty cycle variation.

Specifications subject to change without notice.

TIMING CHARACTERISTICS* (V_S = +5 V ± 5% except as noted, R_{SET} = 3.9 kΩ)

Parameter	Temp	Test Level	AD9850BRS			Units
			Min	Typ	Max	
t _{DS} (Data Setup Time)	FULL	IV	3.5			ns
t _{DH} (Data Hold Time)	FULL	IV	3.5			ns
t _{WH} (W_CLK min. Pulse Width High)	FULL	IV	3.5			ns
t _{WL} (W_CLK min. Pulse Width Low)	FULL	IV	3.5			ns
t _{WD} (W_CLK Delay After FQ_UD)	FULL	IV	7.0			ns
t _{CD} (CLKIN Delay After FQ_UD)	FULL	IV	3.5			ns
t _{FH} (FQ_UD High)	FULL	IV	7.0			ns
t _{FL} (FQ_UD Low)	FULL	IV	7.0			ns
t _{CF} (Output Latency from FQ_UD)						
Frequency Change	FULL	IV	18			CLKIN Cycles
Phase Change	FULL	IV	13			CLKIN Cycles
t _{FD} (FQ_UD Min. Delay After W_CLK)	FULL	IV	7.0			ns
t _{RH} (CLKIN Delay After RESET Rising Edge)	FULL	IV	3.5			ns
t _{RL} (RESET Falling Edge After CLKIN)	FULL	IV	3.5			ns
t _{RS} (Minimum RESET Width)	FULL	IV	5			CLKIN Cycles
t _{OL} (RESET Output Latency)	FULL	IV	13			CLKIN Cycles
t _{RR} (Recovery from RESET)	FULL	IV	2			CLKIN Cycles
Wake-Up Time from Power-Down Mode	+25°C	V		5		μs

NOTES

*Control functions are asynchronous with CLKIN.

Specifications subject to change without notice.

AD9850

ABSOLUTE MAXIMUM RATINGS*

Maximum Junction Temperature	+165°C
VDD	+6 V
Digital Inputs	-0.7 V to +V _S
Digital Output Continuous Current	5 mA
DAC Output Current	30 mA
Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C
Lead Temperature (Soldering 10 sec)	+300°C
SSOP θ_{JA} Thermal Impedance	82°C/W

*Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

EXPLANATION OF TEST LEVELS

Test Level

- I - 100% Production Tested.
- III - Sample Tested Only.
- IV - Parameter is guaranteed by design and characterization testing.
- V - Parameter is a typical value only.
- VI - All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for military temperature devices; guaranteed by design and characterization testing for industrial devices.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9850 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ORDERING GUIDE

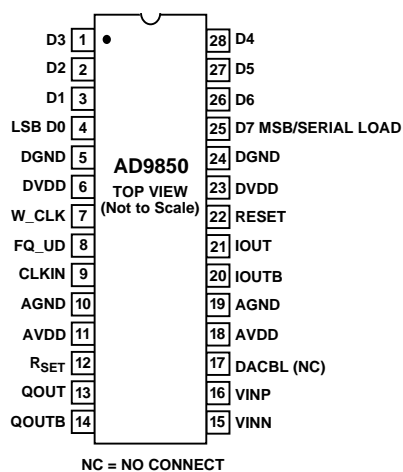
Model	Temperature Range	Package Option*
AD9850BRS	-40°C to +85°C	RS-28

*RS = Shrink Small Outline (SSOP).

Table I. Lead Function Descriptions

Mnemonic	Lead No.	Function
CLKIN	9	Reference Clock Input. This may be a continuous CMOS-level pulse train or sine input biased at 1/2 V supply. The rising edge of this clock initiates operation.
R _{SET}	12	This is the DAC's external R _{SET} connection. This resistor value sets the DAC full-scale output current. For normal applications ($F_S I_{OUT} = 10 \text{ mA}$), the value for R _{SET} is 3.9 k Ω connected to ground. The R _{SET} /I _{OUT} relationship is: $I_{OUT} = 32 (1.248 \text{ V}/R_{SET})$.
AGND	10, 19	Analog Ground. These leads are the ground return for the analog circuitry (DAC and comparator).
DGND	5, 24	Digital Ground. These are the ground return leads for the digital circuitry.
DVDD	6, 23	Supply Voltage Leads for digital circuitry.
AVDD	11, 18	Supply Voltage for the analog circuitry (DAC and comparator).
W_CLK	7	Word Load Clock. This clock is used to load the parallel or serial frequency/phase/control words.
FQ_UD	8	Frequency Update. On the rising edge of this clock, the DDS will update to the frequency (or phase) loaded in the data input register, it then resets the pointer to Word 0.
D0–D7	1–4, 25–28	8-Bit Data Input. This is the 8-bit data port for iteratively loading the 32-bit frequency and 8-bit phase/control word. D7 = MSB; D0 = LSB. D7 (Pin 25) also serves as the input pin for the 40-bit serial data word.
RESET	22	Reset. This is the master reset function; when set high it clears all registers (except the input register) and the DAC output will go to Cosine 0 after additional clock cycles—see Figure 19.
IOUT	21	Analog Current Output of the DAC.
IOUTB	20	The Complementary Analog Output of the DAC.
DACBL	17	DAC Baseline. This is the DAC baseline voltage reference; this lead is internally bypassed and should normally be considered a “no connect” for optimum performance.
VIN	16	Noninverting voltage input. This is the comparator's positive input.
VINN	15	Inverting Voltage Input. This is the comparator's negative input.
QOUT	14	Output True. This is the comparator's true output.
QOUTB	13	Output Complement. This is the comparator's complement output.

PIN CONFIGURATIONS



AD9850–Typical Performance Characteristics

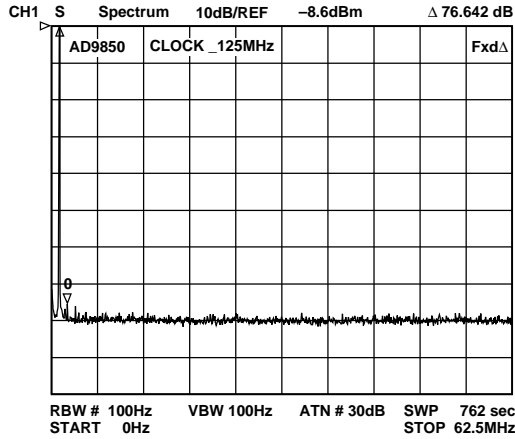


Figure 1. SFDR, CLKIN = 125 MHz/FOUT = 1 MHz

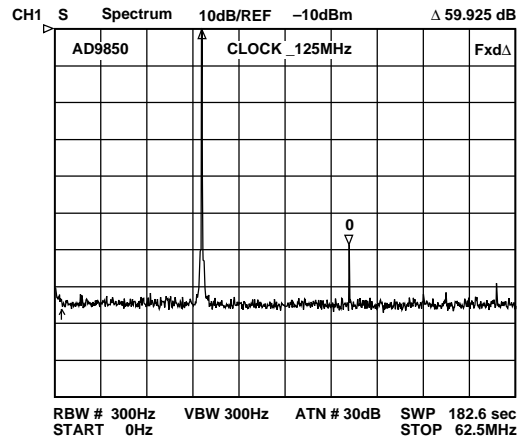


Figure 4. SFDR, CLKIN = 125 MHz/FOUT = 20 MHz

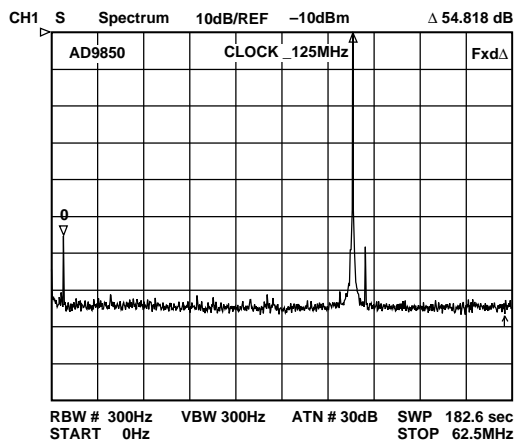


Figure 2. SFDR, CLKIN = 125 MHz/FOUT = 41 MHz

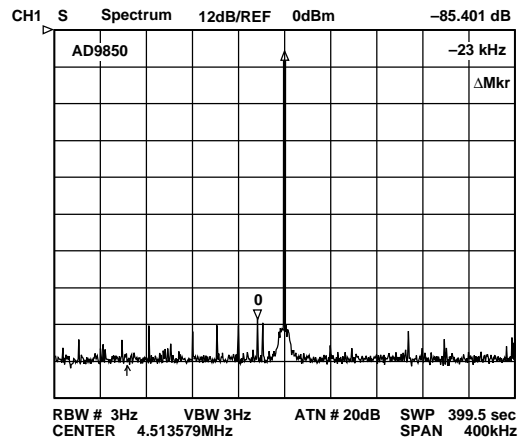


Figure 5. SFDR, CLKIN = 20.5 MHz/FOUT = 4.5 MHz

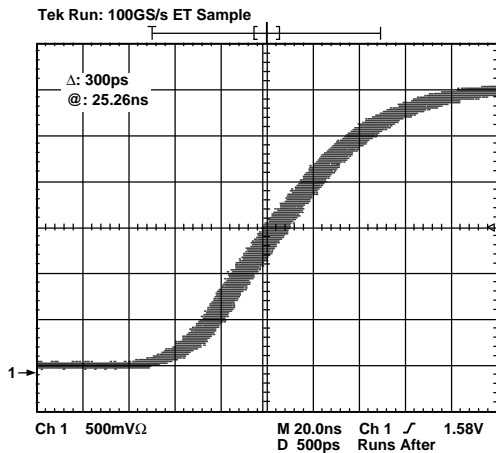


Figure 3. Typical Comparator Output Jitter, AD9850 Configured as Clock Generator w/42 MHz LP Filter (40 MHz AOUT/125 MHz CLKIN)

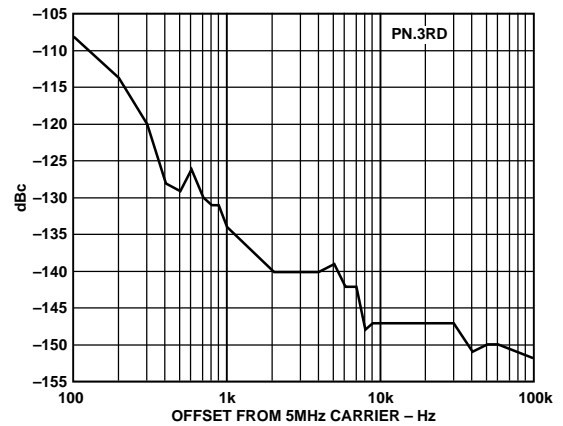


Figure 6. Output Phase Noise (5 MHz AOUT/125 MHz CLKIN)

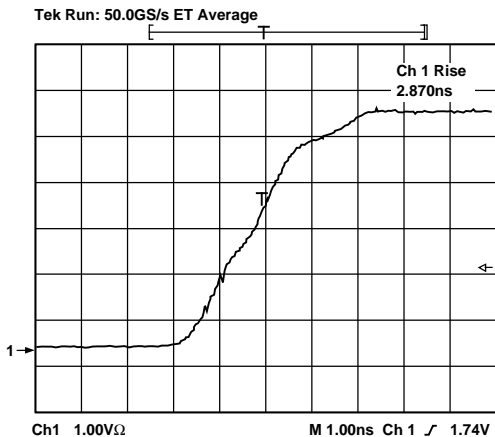


Figure 7. Comparator Output Rise Time (5 V Supply/15 pF Load)

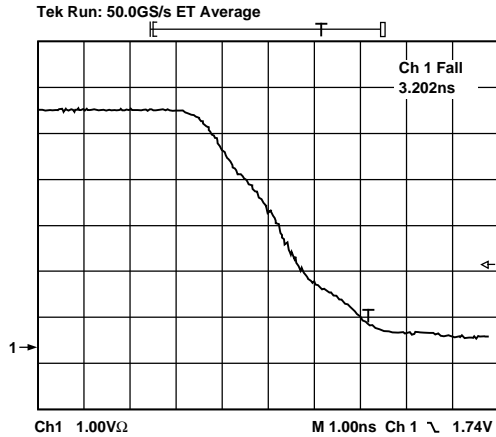


Figure 10. Comparator Output Fall Time (5 V Supply/15 pF Load)

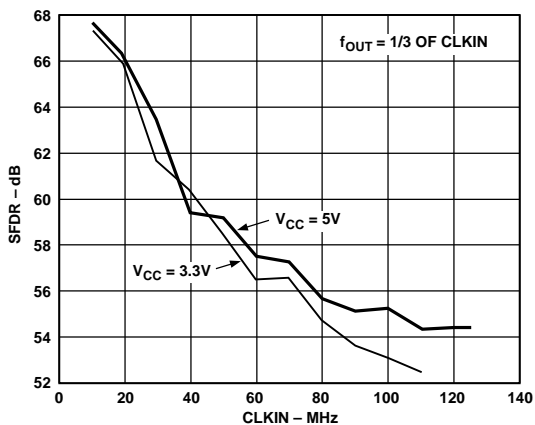


Figure 8. SFDR vs. CLKIN Frequency (AOUT = 1/3 of CLKIN)

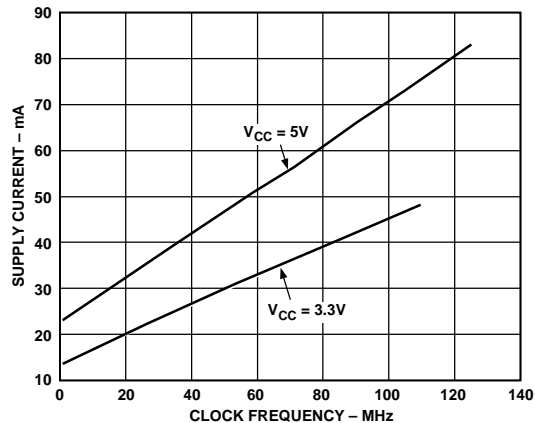


Figure 11. Supply Current vs. CLKIN Frequency (AOUT = 1/3 of CLKIN)

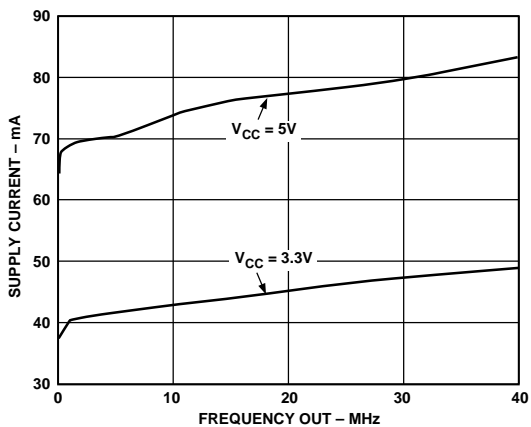


Figure 9. Supply Current vs. AOUT Frequency (CLKIN = 125/110 MHz for 5 V/3.3 V Plot)

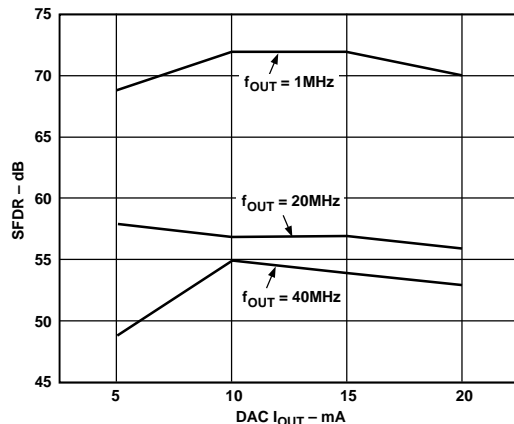


Figure 12. SFDR vs. DAC IOUT (AOUT = 1/3 of CLKIN)

AD9850

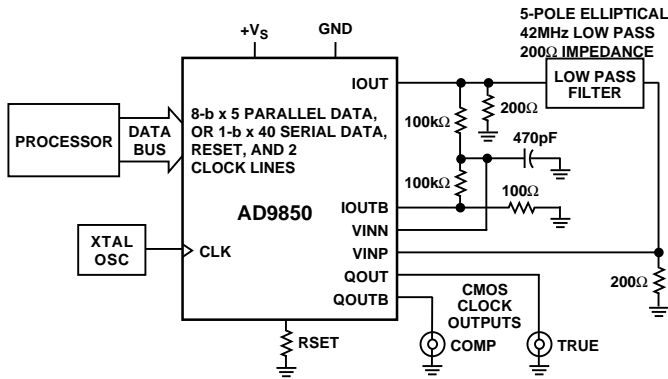


Figure 13. Basic AD9850 Clock Generator Application with Low-Pass Filter

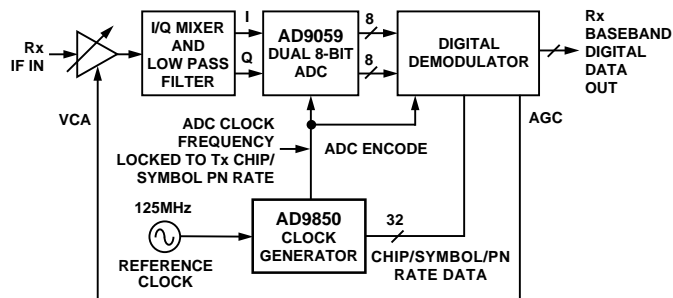
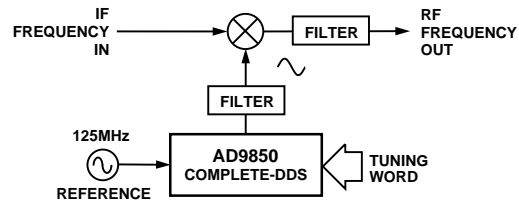
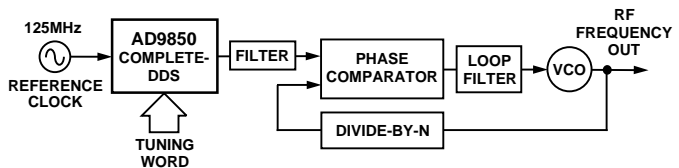


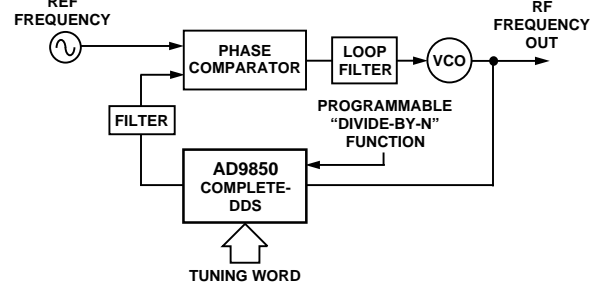
Figure 14. AD9850 Clock Generator Application in a Spread-Spectrum Receiver



a. Frequency/Phase-Agile Local Oscillator



b. Frequency/Phase-Agile Reference for PLL



c. Digitally-Programmable "Divide-by-N" Function in PLL

Figure 15. AD9850 Complete-DDS Synthesizer in Frequency Up-Conversion Applications

THEORY OF OPERATION AND APPLICATION

The AD9850 utilizes direct digital synthesis (DDS) technology, in the form of a numerically controlled oscillator, to generate a frequency/phase-agile sine wave. The digital sine wave is converted to analog form via an internal 10-bit high speed D/A converter and an onboard high speed comparator is provided to translate the analog sine wave into a low-jitter TTL/CMOS-compatible output square wave. DDS technology is an innovative circuit architecture that allows fast and precise manipulation of its output frequency, under full digital control. DDS also enables very high resolution in the incremental selection of output frequency; the AD9850 allows an output frequency resolution of 0.0291 Hz, with a 125 MHz reference clock applied. The AD9850's output waveform is phase-continuous when changed.

The basic functional block diagram and signal flow of the AD9850 configured as a clock generator is shown in Figure 16.

The DDS circuitry is basically a digital frequency divider function whose incremental resolution is determined by the frequency of the reference clock, divided by the 2^N number of bits in the tuning word. The phase accumulator is a variable-modulus counter that increments the number stored in it each time it

receives a clock pulse. When the counter overflows it wraps around which makes the phase accumulator's output contiguous. The frequency tuning word sets the modulus of the counter which effectively determines the size of the increment (Δ Phase) that gets added to the value in the phase accumulator on the next clock pulse. The larger the added increment, the faster the accumulator overflows, which results in a higher output frequency. The AD9850 utilizes an innovative and proprietary algorithm that mathematically converts the 14-bit truncated value of the phase accumulator to the appropriate COS value. This unique algorithm uses a much reduced ROM look-up table and DSP techniques to perform this function, which contributes to the small size and low power dissipation of the AD9850. The relationship of the output frequency, reference clock, and tuning word of the AD9850 is determined by the formula:

$$F_{OUT} = (\Delta \text{ Phase} \times CLKIN) / 2^{32}$$

where: Δ Phase = value of 32-bit tuning word

CLKIN = input reference clock frequency in MHz

F_{OUT} = frequency of the output signal in MHz

The digital sine wave output of the DDS block drives the internal high speed 10-bit D/A converter which reconstructs the sine

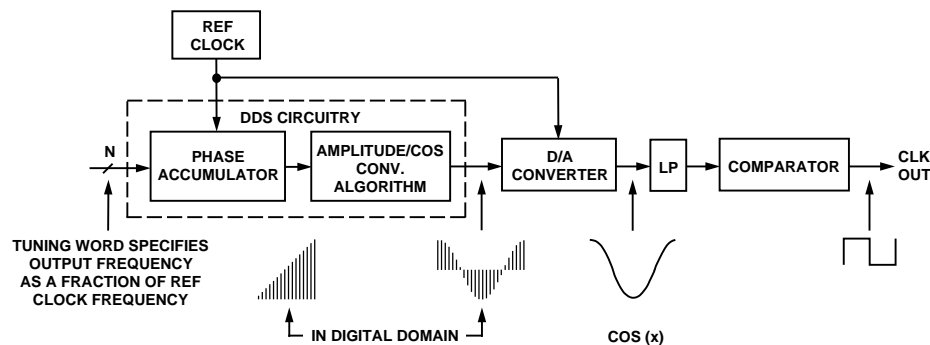


Figure 16. Basic DDS Block Diagram and Signal Flow of AD9850

wave in analog form. This DAC has been optimized for dynamic performance and low glitch energy as manifested in the low jitter performance of the AD9850. Since the output of the AD9850 is a sampled signal, its output spectrum follows the Nyquist sampling theorem. Specifically, its output spectrum contains the fundamental plus aliased signals (images) that occur at multiples of the Reference Clock Frequency \pm the selected output frequency. A graphical representation of the sampled spectrum, with aliased images, is shown in Figure 17.

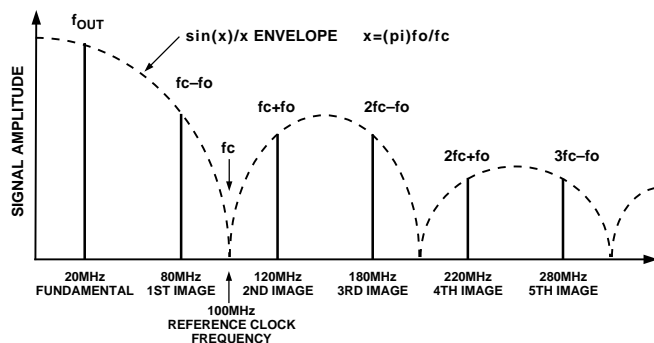


Figure 17. Output Spectrum of a Sampled Signal

In this example, the reference clock is 100 MHz and the output frequency is set to 20 MHz. As can be seen, the aliased images are very prominent and of a relatively high energy level as determined by the $\sin(x)/x$ roll-off of the quantized D/A converter output. In fact, depending on the $f_o/\text{Ref Clk}$ relationship, the first aliased image can be on the order of -3 dB below the fundamental. A low-pass filter is generally placed between the output of the D/A converter and the input of the comparator to further suppress the effects of aliased images. Obviously, consideration must be given to the relationship of the selected output frequency and the Reference Clock frequency to avoid unwanted (and unexpected) output anomalies.

A good rule-of-thumb for applying the AD9850 as a clock generator is to limit the selected output frequency to $<33\%$ of Reference Clock frequency to avoid generating aliased signals that fall within, or close to, the output band of interest (generally dc-selected output frequency). This practice will ease the complexity (and cost) of the external filter requirement for the clock generator application.

The reference clock frequency of the AD9850 has a minimum limitation of 1 MHz. The device has internal circuitry that senses when the minimum clock rate threshold has been exceeded and automatically places itself in the power-down mode. When in this state, if the clock frequency again exceeds the threshold, the device resumes normal operation. This shutdown mode prevents excessive current leakage in the dynamic registers of the device.

The D/A converter output and comparator inputs are available as differential signals which can be flexibly configured in any manner desired to achieve the objectives of the end-system. The typical application of the AD9850 is with single-ended output/input analog signals, a single low-pass filter, and generating the comparator reference midpoint from the differential DAC output, as shown in Figure 13.

Programming the AD9850

The AD9850 contains a 40-bit register which is used to program the 32-bit frequency control word, the 5-bit phase modulation word, and the power-down function. This register can be loaded in a parallel or serial mode.

In the parallel load mode, the register is loaded via an 8-bit bus; the full 40-bit word requires five iterations of the 8-bit word. The W_CLK and FQ_UD signals are used to address and load the registers. The rising edge of FQ_UD loads the (up to) 40-bit control data word into the device and resets the address pointer to the first register. Subsequent W_CLK rising edges load the 8-bit data on words [7:0] and move the pointer to the next register. After *five* loads, W_CLK edges are ignored until either a reset or an FQ_UD rising edge resets the address pointer to the first register.

In serial load mode, subsequent rising edges of W_CLK shift the 1-bit data on Lead 25 (D7) through the 40 bits of programming information. After 40 bits are shifted through, an FQ_UD pulse is required to update the output frequency (or phase).

The function assignments of the data and control words are shown in Table III; the detailed timing sequence for updating the output frequency and/or phase, resetting the device, and powering-up/down, are shown in the timing diagrams of Figures 18–24.

Note: There are specific control codes, used for factory test purposes, which render the AD9850 temporarily inoperable. The user must take deliberate precaution to avoid inputting the codes listed in Table II.

Table II. Factory-Reserved Internal Test Control Codes

Loading Format	Factory-Reserved Codes
Parallel	1) W0 = XXXXXX10 2) W0 = XXXXXX01
Serial	1) W32 = 1; W33 = 0 2) W32 = 0; W33 = 1 3) W32 = 1, W33 = 1

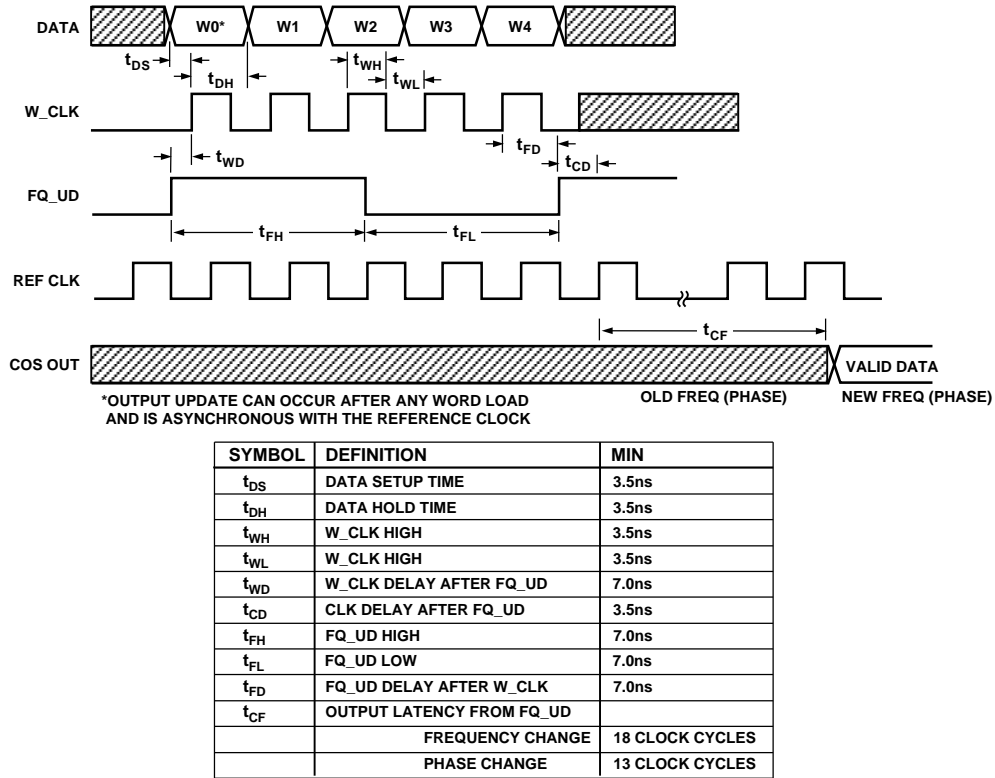
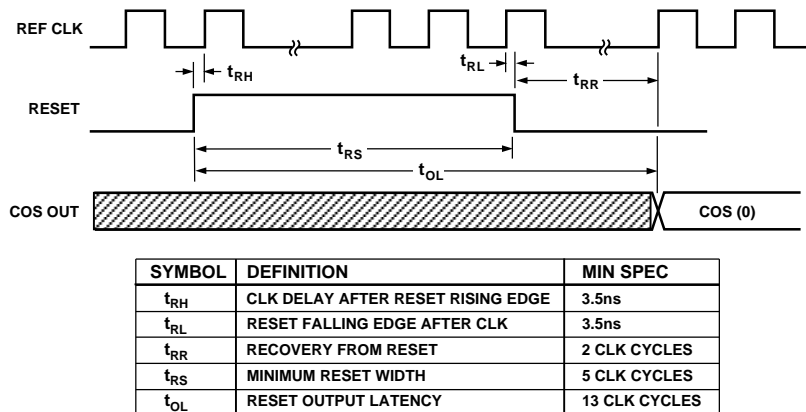


Figure 18. Parallel-Load Frequency/Phase Update Timing Sequence

Table III. 8-Bit Parallel-Load Data/Control Word Functional Assignment

Word	data[7]	data[6]	data[5]	data[4]	data[3]	data[2]	data[1]	data[0]
W0	Phase-b4 (MSB)	Phase-b3	Phase-b2	Phase-b1	Phase-b0 (LSB)	Power-Down	Control	Control
W1	Freq-b31 (MSB)	Freq-b30	Freq-b29	Freq-b28	Freq-b27	Freq-b26	Freq-b25	Freq-b24
W2	Freq-b23	Freq-b22	Freq-b21	Freq-b20	Freq-b19	Freq-b18	Freq-b17	Freq-b16
W3	Freq-b15	Freq-b14	Freq-b13	Freq-b12	Freq-b11	Freq-b10	Freq-b9	Freq-b8
W4	Freq-b7	Freq-b6	Freq-b5	Freq-b4	Freq-b3	Freq-b2	Freq-b1	Freq-b0 (LSB)



RESULTS OF RESET:
 - FREQUENCY/PHASE REGISTER SET TO 0
 - ADDRESS POINTER RESET TO W0
 - POWER-DOWN BIT RESET TO "0"
 - DATA INPUT REGISTER UNEFFECTED

Figure 19. Master Reset Timing Sequence

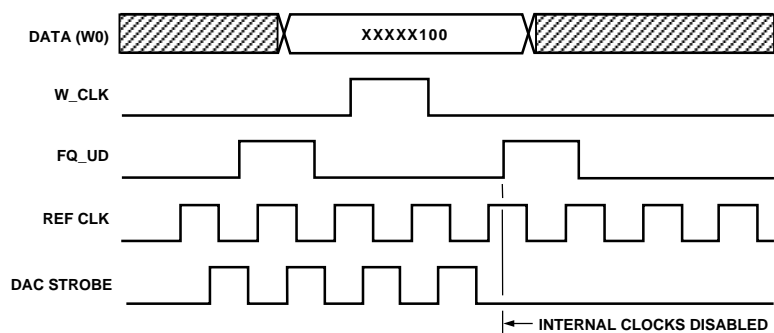


Figure 20. Parallel-Load Power-Down Sequence/Internal Operation

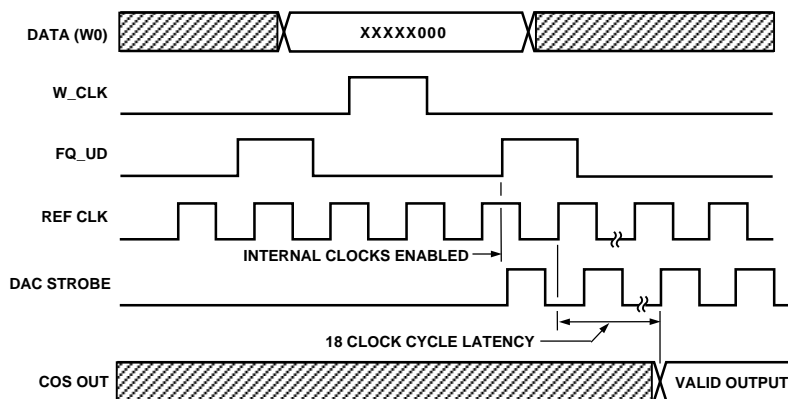


Figure 21. Parallel-Load Power-Up Sequence/Internal Operation

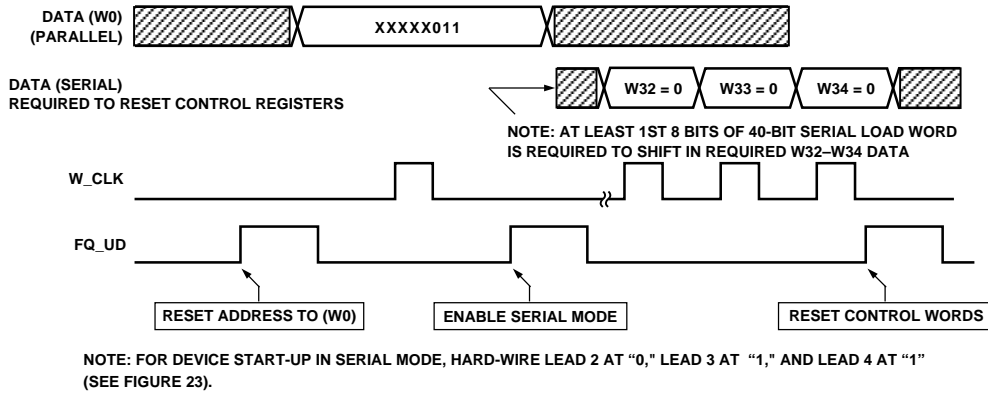


Figure 22. Serial-Load Enable Sequence

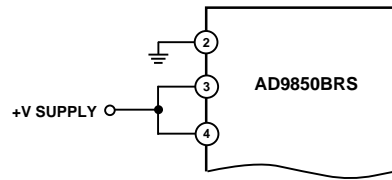


Figure 23. Leads 2-4 Connection for Default Serial-Mode Operation

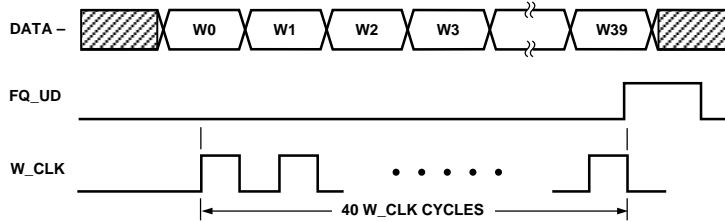


Figure 24. Serial-Load Frequency/Phase Update Sequence

Table IV. 40-Bit Serial-Load Word Function Assignment

W0	Freq-b0 (LSB)	W14	Freq-b14	W28	Freq-b28
W1	Freq-b1	W15	Freq-b15	W29	Freq-b29
W2	Freq-b2	W16	Freq-b16	W30	Freq-b30
W3	Freq-b3	W17	Freq-b17	W31	Freq-b31 (MSB)
W4	Freq-b4	W18	Freq-b18	W32	Control
W5	Freq-b5	W19	Freq-b19	W33	Control
W6	Freq-b6	W20	Freq-b20	W34	Power-Down
W7	Freq-b7	W21	Freq-b21	W35	Phase-b0 (LSB)
W8	Freq-b8	W22	Freq-b22	W36	Phase-b1
W9	Freq-b9	W23	Freq-b23	W37	Phase-b2
W10	Freq-b10	W24	Freq-b24	W38	Phase-b3
W11	Freq-b11	W25	Freq-b25	W39	Phase-b4 (MSB)
W12	Freq-b12	W26	Freq-b26		
W13	Freq-b13	W27	Freq-b27		

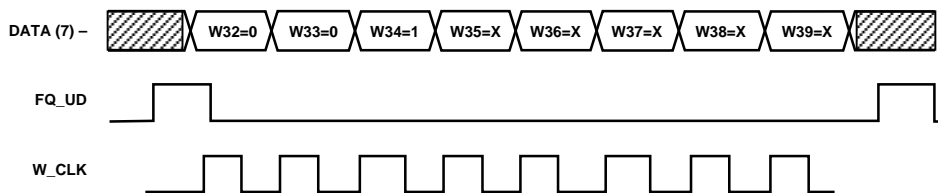


Figure 25. Serial-Load Power-Down Sequence

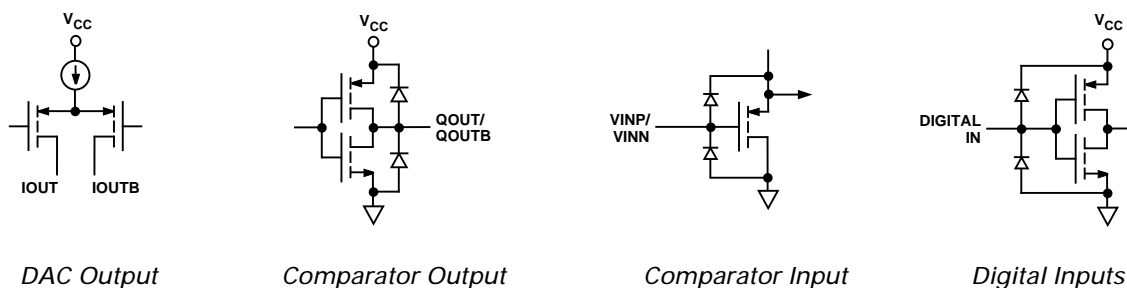


Figure 26. AD9850 I/O Equivalent Circuits

PCB LAYOUT INFORMATION

The AD9850/CGPCB and AD9850/FSPCB evaluation boards (Figures 27–30) represent typical implementations of the AD9850 and exemplify the use of high frequency/high resolution design and layout practices. The printed circuit board that contains the AD9850 should be a multilayer board that allows dedicated power and ground planes. The power and ground planes should be free of etched traces that cause discontinuities in the planes. It is recommended that the top layer of the multilayer board also contain interspatial ground plane which makes ground available for surface-mount devices. If separate analog and digital system ground planes exist, they should be connected together at the AD9850 for optimum results.

Avoid running digital lines under the device as these will couple noise onto the die. The power supply lines to the AD9850 should use as large of a track as possible to provide a low-impedance path and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with ground to avoid radiating noise to other sections of the board. Avoid crossover of digital and analog signal paths. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the circuit board. Use microstrip techniques where possible.

Good decoupling is also an important consideration. The analog (AVDD) and digital (DVDD) supplies to the AD9850 are independent and separately pinned out to minimize coupling between analog and digital sections of the device. All analog and digital supplies should be decoupled to AGND and DGND respectively with high quality ceramic capacitors. To achieve best performance from the decoupling capacitors, they should be placed as close as possible to the device, ideally right up against the device. In systems where a common supply is used to drive both the AVDD and DVDD supplies of the AD9850, it is recommended that the system's AVDD supply be used.

Analog Devices, Inc., applications engineering support is available to answer additional questions on grounding and PCB layout. Call 1-800-ANALOGD.

Evaluation Boards

Two versions of evaluation boards are available for the AD9850 that facilitate the implementation of the device for benchtop analysis, and serve as a reference for PCB layout. The *AD9850/FSPCB* is intended for applications where the device will primarily be used as frequency synthesizer. This version facilitates connection of the AD9850's internal D/A converter output to a 50 Ω spectrum analyzer input; the internal comparator on the AD9850 DUT is not enabled (see Figure 28 for electrical schematic of AD9850/FSPCB). The *AD9850/CGPCB* is intended for applications using the device in the clock generator mode. It connects the AD9850's DAC output to the internal comparator input via a single-ended, 42 MHz low-pass, 5-pole Elliptical filter. This model facilitates the access of the AD9850's comparator output for evaluation of the device as a frequency- and phase-agile clock source (see Figure 29 for electrical schematic of AD9850/CGPCB).

Both versions of the AD9850 evaluation boards are designed to interface to the parallel printer port of a PC. The operating software runs under Microsoft Windows and provides a user-friendly and intuitive format for controlling the functionality and observing the performance of the device. The 3.5" floppy provided with the evaluation board contains an executable file which loads and displays the AD9850 function-selection screen. The evaluation board may be operated with +3.3 V or +5 V supplies. The evaluation boards are configured at the factory for an external reference clock input; if the onboard crystal clock source is utilized, remove R2.

AD9850

AD9850/XXPCB Evaluation Board Instructions

Required hardware/software:

IBM compatible computer operating in a Windows™ environment
Printer port and Centronics compatible printer cable
3.5" disk drive
Mouse
AD9850 evaluation board software disk
AD9850/XXPCB evaluation board
XTAL clock or signal generator—if using a signal generator, dc offset the clock signal to 1/2 the supply voltage and apply at least 3 V p-p signal across the 50 Ω (R2) input resistor. Remove R2 for a high Z clock input impedance.
+3.3 V or +5 V supply

Setup:

Copy the contents of the AD9850 disk onto host computer's hard drive.
Connect printer cable from computer's printer port to the AD9850/XXPCB evaluation board.
Apply power to AD9850/XXPCB evaluation board.
Apply external TTL-compatible reference clock to the AD9850/XXPCB evaluation board or install crystal clock source in socket (remember to remove R2).
Locate the WIN9850.EXE file and execute that program.
Your monitor should display a "control panel" to allow operation of the AD9850/XXPCB evaluation board.

Operation:

On the control panel, locate the box called "COMPUTER I/O." With the mouse (or by tabbing over) click on the selection marked "LPT1" and then click on the "TEST" box. A message will appear indicating whether or not this choice of output ports is valid. Choose alternate ports as necessary to achieve a correct setting.

On the control panel, click on "MASTER RESET" button. This will reset the AD9850 to 0 Hz, 0° COS phase; the DAC output should be a dc voltage equal to the full-scale output of the AD9850.

Place the cursor in the "CLOCK" box and type in the exact clock frequency in MHz that will be applied to the evaluation board. Click on the "LOAD" button (or press enter on the keyboard).

Place the cursor in the "OUTPUT FREQUENCY" box and type in the desired output frequency in MHz. Click on the "LOAD" button (or press enter on the keyboard). The BUS MONITOR display on the control panel will display the hexadecimal value of the input 32-bit tuning word. Upon completion of this step, the AD9850/XXPCB evaluation board should be generating the desired sine wave. (Note: VER 1.1 of the AD9850/XXPCB operating software is resolution limited to the nearest Hz.)

Changing the phase of the AD9850/XXPCB's output sine wave is accomplished by clicking on the down arrow in the "OUTPUT PHASE DELAY" box, selecting the desired delay increment, and clicking on the "LOAD" button.

Other operational modes available on the control panel are activated by pointing and clicking.

The AD9850/FSPCB provides access into and out of the on-chip comparator via test point pairs (each pair has an active input and a ground connection). The two active inputs are labeled TP1 and TP2. The unmarked hole next to each labeled test point is a ground connection. The two active outputs are labeled TP5 and TP6. Adjacent to each of those test points are unmarked ground connections.

The AD9850/CGPCB provides BNC inputs and outputs associated with the on-chip comparator and the on-board, 5th order, 200 Ω input/output Z, elliptic 45 MHz low-pass filter. Jumpering (soldering a wire between) E1 to E2, E3 to E4, and E5 to E6 will connect the on-board filter and the midpoint switching voltage to the comparator. Users may elect to insert their own filter and threshold voltage by removing the jumpers and inserting a filter between J7 and J6 and providing a threshold voltage at E1.

If you choose to utilize the XTAL socket to supply the clock to the AD9850 DUT, you must remove R2 (50 Ω chip resistor). The XTAL oscillator must be either TTL or (preferably) CMOS compatible.

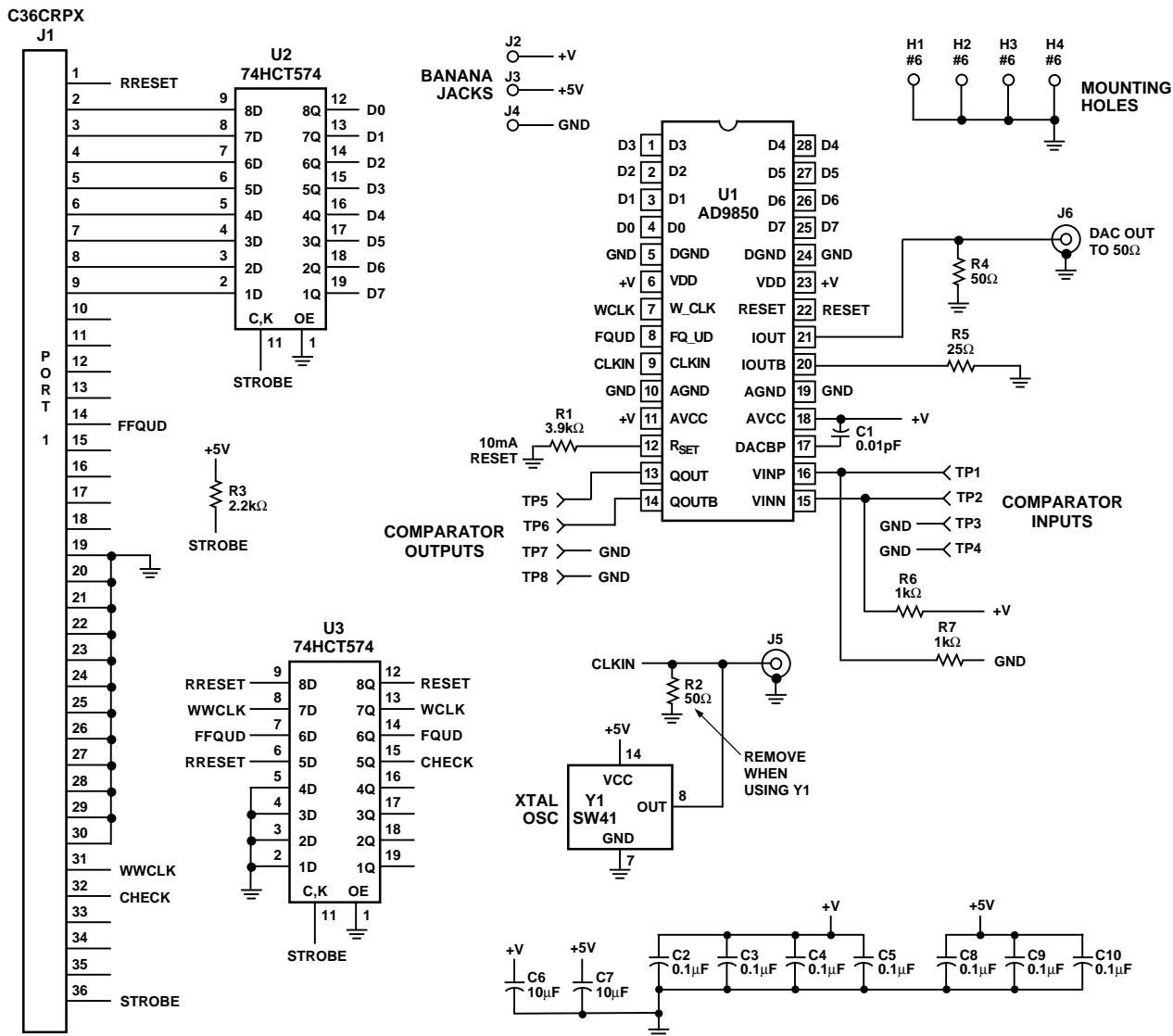


Figure 27. AD9850/FSPCB Electrical Schematic

COMPONENT LIST

Integrated Circuits

- U1 AD9850BRS (28-Pin SSOP)
- U2, U3 74HCT574 H-CMOS Octal Flip-Flop

Capacitors

- C2-C5, C8-C10 0.1 μF Ceramic Chip Capacitor
- C6, C7 10 μF Ceramic Chip Capacitor

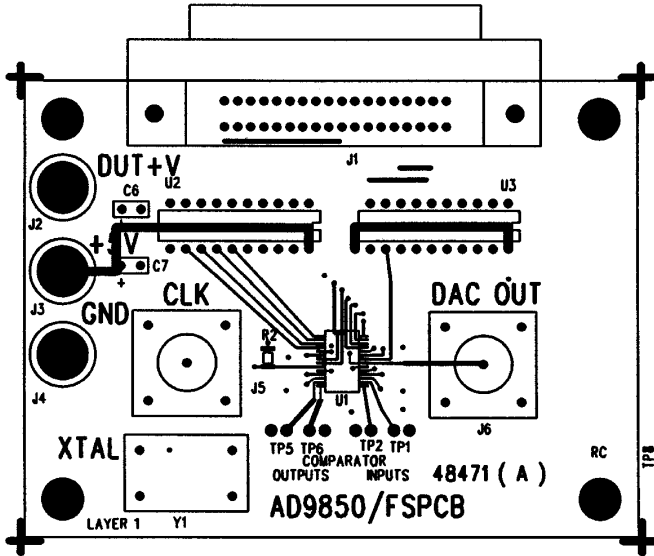
Resistors

- R1 3.9 kΩ Resistor
- R2, R4 50 Ω Resistor
- R3 2.2 kΩ Resistor
- R5 25 Ω Resistor
- R6, R7 1 kΩ Resistor

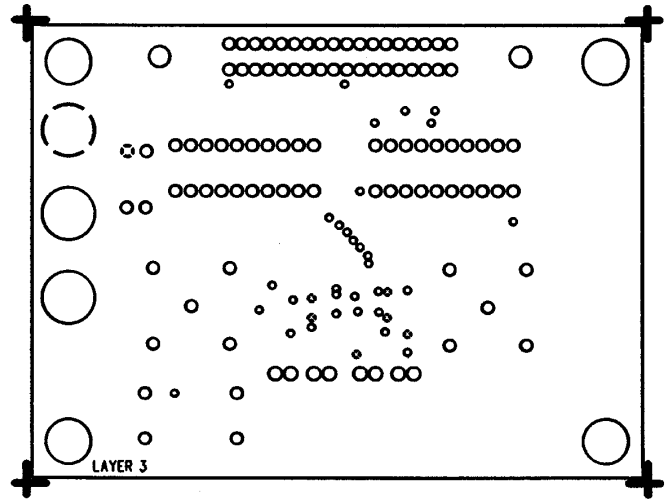
Connectors

- J1 36-Pin D Connector
- J2, J3 Banana Jack
- J5, J6 BNC Connector

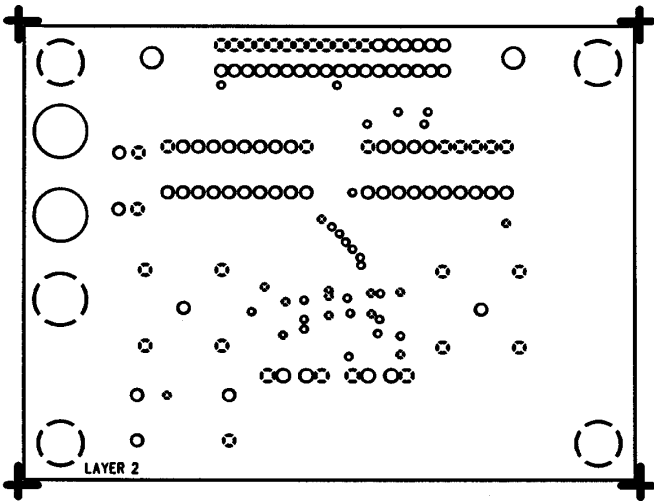
AD9850



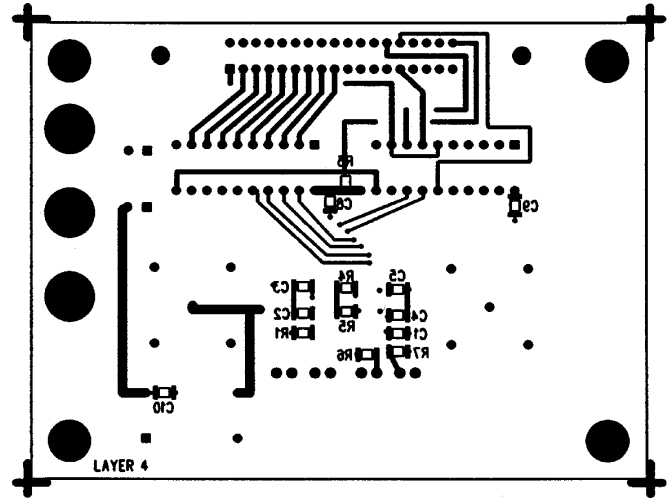
a. AD9850/FSPCB Top Layer



c. AD9850/FSPCB Power Plane



b. AD9850/FSPCB Ground Plane



d. AD9850/FSPCB Bottom Layer

Figure 28. AD9850/FSPCB Evaluation Board Layout

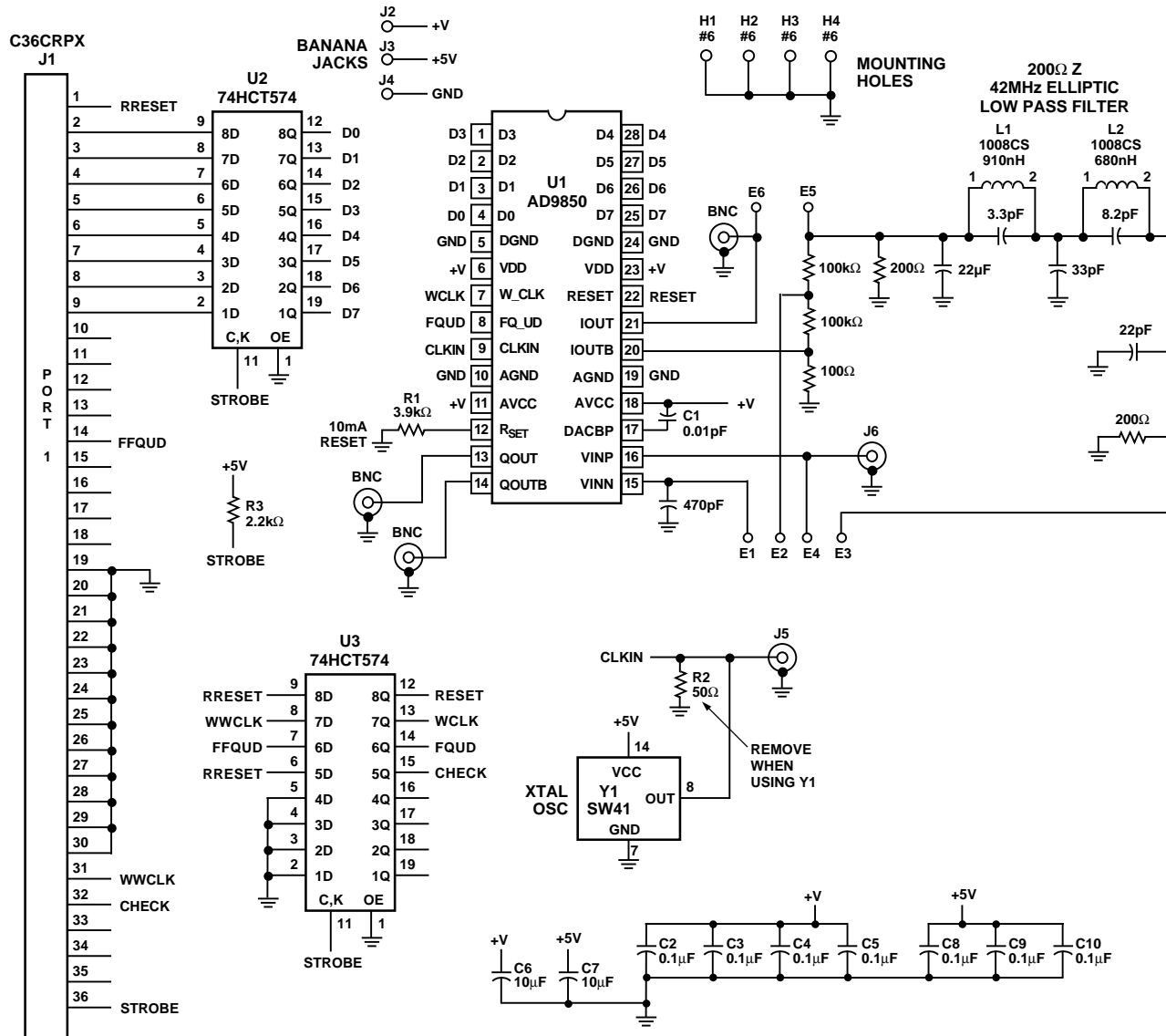


Figure 29. AD9850/CGPCB Electrical Schematic

COMPONENT LIST

Integrated Circuits

U1	AD9850BRS (28-Pin SSOP)
U2, U3	74HCT574 H-CMOS Octal Flip-Flop

Capacitors

C1	470 pF Ceramic Chip Capacitor
C2-C5, C8-C10	0.1 μF Ceramic Chip Capacitor
C6, C7	10 μF Ceramic Chip Capacitor
C11	22 μF Ceramic Chip Capacitor
C12	3.3 pF Ceramic Chip Capacitor
C13	33 pF Ceramic Chip Capacitor
C14	8.2 pF Ceramic Chip Capacitor
C15	22 pF Ceramic Chip Capacitor

Resistors

R1	3.9 kΩ Resistor
R2	50 Ω Resistor
R3	2.2 kΩ Resistor
R4, R5	100 kΩ Resistor
R6, R7	200 Ω Resistor
R8	100 Ω Resistor

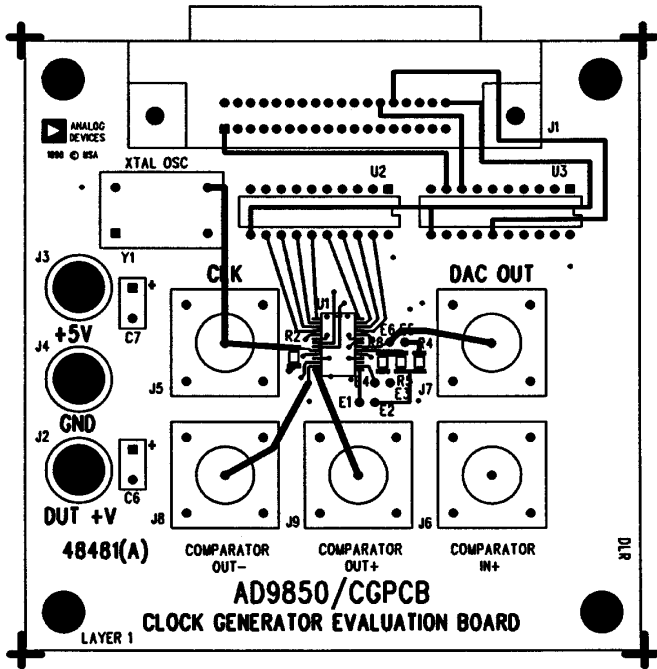
Connectors

J2, J3, J4	Banana Jack
J5-J9	BNC Connector

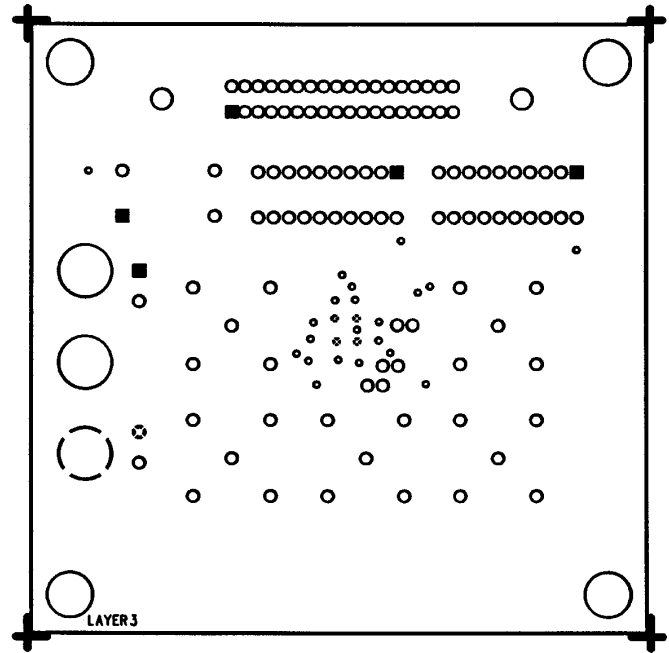
Inductors

L1	910 nH Surface Mount
L2	680 nH Surface Mount

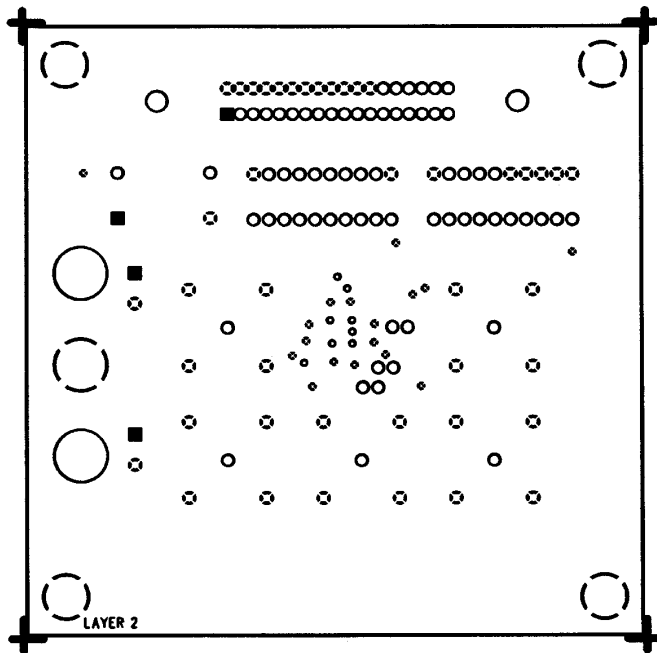
AD9850



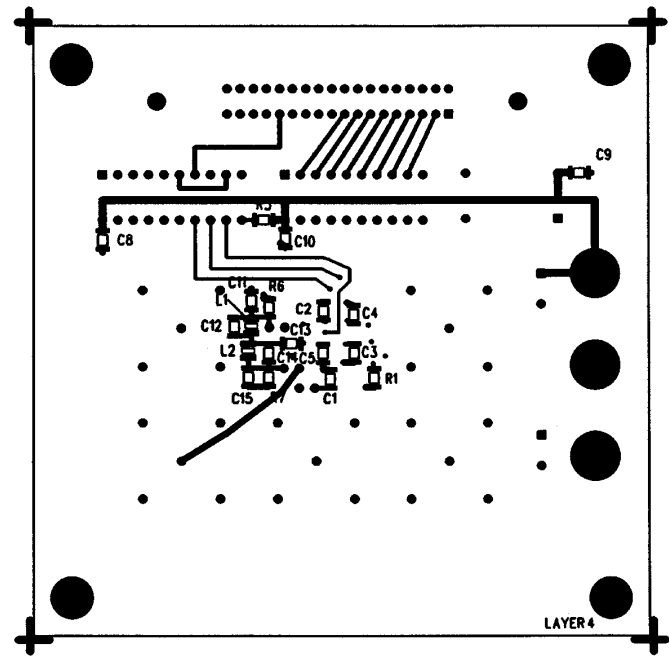
a. AD9850/FSPCB Top Layer



c. AD9850/FSPCB Power Plane



b. AD9850/FSPCB Ground Plane



d. AD9850/FSPCB Bottom Layer

Figure 30. AD9850/FSPCB Evaluation Board Layout

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

**28-Lead Shrink Small Outline Package
(RS-28)**

