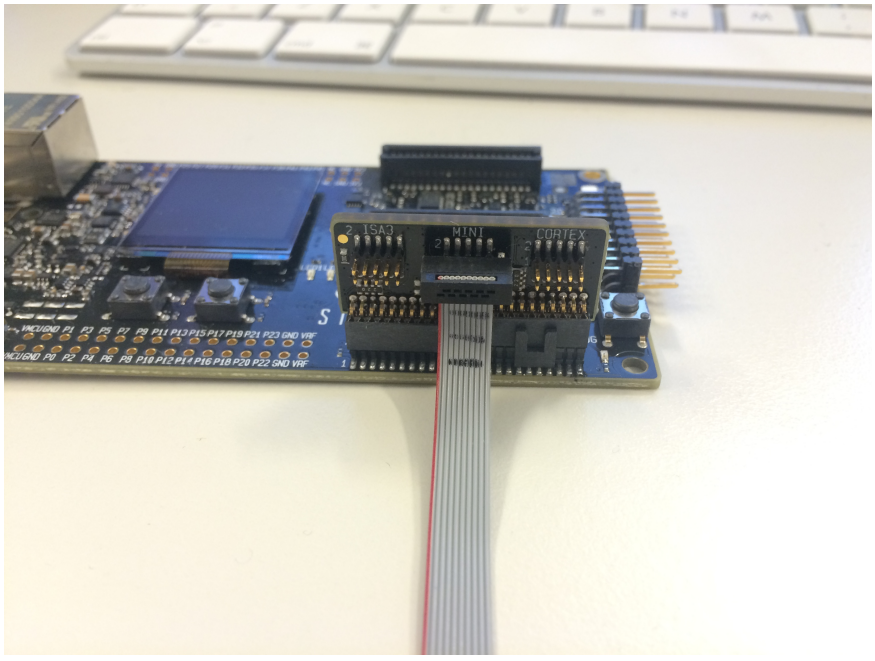
AN958: Debugging and Programming Interfaces for Custom Designs

The Silicon Labs MCU and Wireless Starter Kits and Simplicity Studio provide a powerful development and debug environment.

In order to take advantage of these capabilities and features on custom hardware, Silicon Labs recommends including debugging and programming interface connector(s) in custom hardware designs. Possible options include full support of all debugging and programming capabilities of the STK, to serial wire programming only. This application note describes the benefits of including these connector interfaces in custom hardware designs and provides the details regarding these interfaces.

KEY POINTS

- Wireless starter kits along with Simplicity Studio provide a powerful development and debug environment
- Use the debugging and programming interface connector(s) to take advantage of these capabilities



Mini Simplicity Adapter Board

1. Background

The Silicon Labs MCU Starter Kit (STK) and Wireless Starter Kit (WSTK) provide a powerful development and debug environment when used with Simplicity Studio. The STK and WSTK provide several debug capabilities and features, including the following:

- SWD (serial wire debug)
  - 2-pin serial wire debug interface for programming and debugging, using the pins SWCLK and SWDIO.
- JTAG
  - 4-wire interface for programming and debugging, using the pins TCK, TMS, TDI, and TDO.
- C2 interface (for 8-bit devices)
  - 2-wire programming interface used by most Silicon Labs 8-bit MCUs.
  - See "AN124: Pin Sharing Techniques for the C2 Interface", which discusses pin sharing for C2 devices.
- ETM* (embedded trace macrocell)
  - Debug component which enables reconstruction of program execution, and is designed as a high-speed, low-power debug tool that only supports instruction trace.
- AEM (advanced energy monitoring)
  - Accurate high-speed current measurements and energy debugging/profiling when the STK/WSTK power selection switch is in the AEM position. Use with Simplicity Studio Energy Profiler perspective.
- PTI (packet trace interface [WSTK only])
  - Physical layer (PHY) level PTI for effective network-level debugging. Monitors all the PHY transmit and receive packets between the MAC and baseband modules within the radio without affecting normal operation.
- VCOM (virtual COM port)
  - UART COM port interface to the target from the debugger (pass-through UART).
- Virtual UART
  - SWD-based virtual UART interface to the target from the debugger, available through the SWD interface (SWDIO, SWCLK, and SWO).

These features are available via several different interface means, depending on the features required by the custom target hardware design and the board space available for these interface connectors or test points. These details are discussed in the following sections.

***Note:** The STK and WSTK support ETM only when using an external debugger which supports ETM Capture. The STK and WSTK do not include an ETM capture unit. Only devices that have an ETM macrocell will support ETM capture, regardless of the debugger capabilities. Consult the corresponding MCU or Wireless device data sheet for details regarding whether ETM is supported on the device. Silicon Labs MCU and Wireless Development Kits may include support for ETM. Consult the kit documentation for further details.

2. Interface Feature Mapping

The table below summarizes the capabilities and features of the various interfaces described in the following sections. Click on the column header hyperlinks to go directly to the section describing each specific interface.

Table 2.1. Interface Capabilities and Features

Feature	20-pin Standard ARM Cortex Debug+ETM Connector	20-pin Simplicity Connector	Mini Simplicity Adapter Interface (Standard or Tag-Connect 10-pin cable)			Tag-Connect 6-pin Interface
			Mini Simplicity Connector	Cortex Debug Connector	ISA3 Packet Trace Port Connector[1]	
SWD (serial wire debug)	X		X	X	X	X
JTAG	X			X	X	
C2	X			X		
ETM (embedded trace module)	X					
AEM (advanced energy monitoring)		X	X			
PTI (packet trace interface)		X	X		X	
VCOM (virtual COM port)		X	X			
Virtual UART	X		X	X	X	X

Note:
1. ISA3 Packet Trace Port Connector interface is not yet supported by the WSTK.

3. Connector Interfaces

This section presents the standard debug connector interfaces provided by the STK and WSTK, as well as recommendations for including connector interfaces on custom target hardware designs in order to utilize these debug capabilities and features.

3.1 Standard ARM Cortex Debug+ETM Connector

In cases where ETM and/or JTAG debug capabilities and features are required on custom target hardware, a 20-pin (2x10, 1.27 mm pitch) standard ARM Cortex Debug+ETM Connector (similar to Sullins™ part number GRPB102VWQS) should be included in the design. A 20-pin 2x10 1.27 mm pitch ribbon cable (similar to Samtec™ part number FFSD-10-D-6.00-01-N) is required for the connection between the WSTK debug connector and the custom target hardware board connector.

Note: Silicon Labs deviates slightly from the ARM standard, as this version of the connector includes the key pin.

3.1.1 Connector Pin-Out

A pin-out for this debug connector interface is provided in the figure and table below. If ETM and/or JTAG are not required, see 4. Alternative Interfaces for other debug interface options to include on target hardware designs.

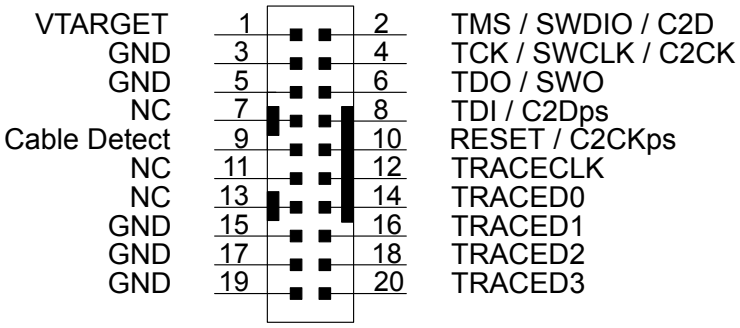


Figure 3.1. Debug Connector

Table 3.1. Debug Connector Pin Descriptions

Pin Number(s)	Function	Note
1	VTARGET	Target voltage on the debugged application
2	TMS / SDWIO / C2D	JTAG test mode select, Serial Wire data or C2 data
4	TCK / SWCLK / C2CK	JTAG test clock, Serial Wire clock or C2 clock
6	TDO/SWO	JTAG test data out or Serial Wire Output
8	TDI / C2Dps	JTAG test data in, or C2D "pin sharing" function[1]
10	RESET / C2CKps	Target device reset, or C2CK "pin sharing" function
12	TRACECLK	Not connected
14	TRACED0	Not connected
16	TRACED1	Not connected
18	TRACED2	Not connected
20	TRACED3	Not connected
9	Cable detect	Connect to ground
11, 13	NC	Not connected
3, 5, 15, 17, 19	GND	

Note:
1. See "AN124: Pin Sharing Techniques for the C2 Interface", which discusses pin sharing for C2 devices.

3.1.2 Connector Footprint

An example component footprint is from Sullins for part number GRPB102VWQS. Refer to http://www.sullinscorp.com/catalogs/82_PAGE90-91_.050_MALE_HDR_ST_RA_SMT.pdf for details on this connector footprint for the custom target hardware PCB.

3.2 20-pin Simplicity Connector

If AEM, PTI, and VCOM functionality are desired, include the 20-pin (2x10, 1.27 mm pitch) Simplicity Connector (similar to Sullins part number GRPB102VWQS) on the target hardware design. A 20-pin 2 x 10 1.27 mm pitch ribbon cable (similar to Samtec part number FFSD-10-D-6.00-01-N) is required for this connection between WSTK Simplicity connector and the custom target hardware board connector. If space constraints do not allow inclusion of this connector on the target hardware design, see 4. Alternative Interfaces for smaller interfaces which provide similar debug features.

3.2.1 Connector Pin-Out

A pin-out for this Simplicity Connector interface is provided in the figure and table below.

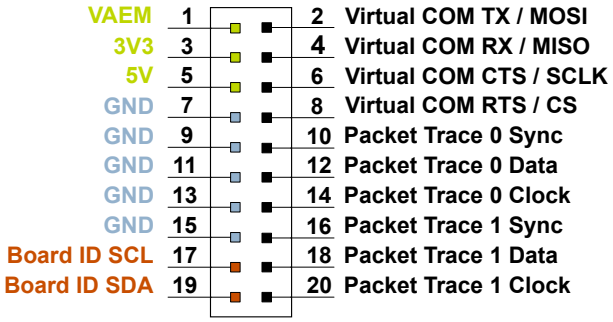


Figure 3.2. Simplicity Connector

Table 3.2. Simplicity Connector Pin Descriptions

Pin Number(s)	Function	Note
1	VAEM	3.3 V power rail, monitored by the AEM
3	3V3	3.3 V power rail
5	5V	5 V power rail
2	VCOM_TX_MOSI	Virtual COM Tx/MOSI
4	VCOM_RX_MISO	Virtual COM Rx/MISO
6	VCOM_CTS_#SCLK	Virtual COM CTS/SCLK
8	VCOM_#RTS_#CS	Virtual COM RTS/CS
10	PTI0_SYNC	Packet Trace 0 Sync
12	PTI0_DATA	Packet Trace 0 Data
14	PTI0_CLK	Packet Trace 0 Clock
16	PTI1_SYNC	Packet Trace 1 Sync
18	PTI1_DATA	Packet Trace 1 Data
20	PTI1_CLK	Packet Trace 1 Clock
17	EXT_ID_SCL	Board ID SCL
19	EXT_ID_SDA	Board ID SDA
7, 9, 11, 13, 15	GND	

Note: Packet Trace 0 should be the default packet trace port selection. Packet Trace 1 is reserved for implementations which include more than one radio on the same IC.

3.2.2 Connector Footprint

An example component footprint is from Sullins for part number GRPB102VWQS. Refer to http://www.sullinscorp.com/catalogs/82_PAGE90-91_.050_MALE_HDR_ST_RA_SMT.pdf for details on this connector footprint for the custom target hardware PCB.

4. Alternative Interfaces

In addition to the standard connector interfaces provided with the STK and WSTK, there are some alternative interfaces that are available, depending on debug needs and available space. The following sections outline these alternative interfaces.

4.1 STK/WSTK Debug Adapter/Connector Interface

A debug adapter board is included in some WSTKs which, when plugged into the two 20-pin connectors of the STK or WSTK, remaps these interfaces to provide a sub-set of debug capabilities and features through a smaller form-factor connector interface.The debug adapter is available standalone with a 15 cm (6 inch) cable as orderable part number SLSDA001A.

For space constrained designs, Silicon Labs recommends the Mini-Simplicity Connector, a 10-pin (2x5) small form-factor (1.27 mm pitch, 3.05 mm pin length) header connector (similar to Samtec part number FTSH-105-01-L-DV-K), on the custom hardware design. This will mate with a standard 10-pin ribbon cable (similar to Samtec part number FFSD-05-D-6.00-01-N) back to the Mini Simplicity Interface Connector on the adapter board, or in the future directly to the STK or WSTK main board.

Note: ETM and JTAG functionality are not supported with this interface and are therefore only available via the 20-pin Debug Connector. Alternatively, JTAG is available via the Cortex port of the adapter board, which follows the standard 10-pin ARM Cortex pin-out, as stated in Section 4.1.2 Connector Pin-Out (Cortex).

With the use of the STK/WSTK Debug Adapter Board plugged into these two 20-pin connectors, a 10-pin connector interface is exposed (see mini connector in the right-hand image in the figure below), which provides a subset of debug capabilities and features in a standardized small form-factor connector. These capabilities include the following:

- SWD (Serial Wire Debug, including SWO)
- AEM (advanced energy monitoring)
- PTI (packet trace interface [WSTK only])
- VCOM (virtual COM port)

The figure below shows the Mini Simplicity Adapter Board.

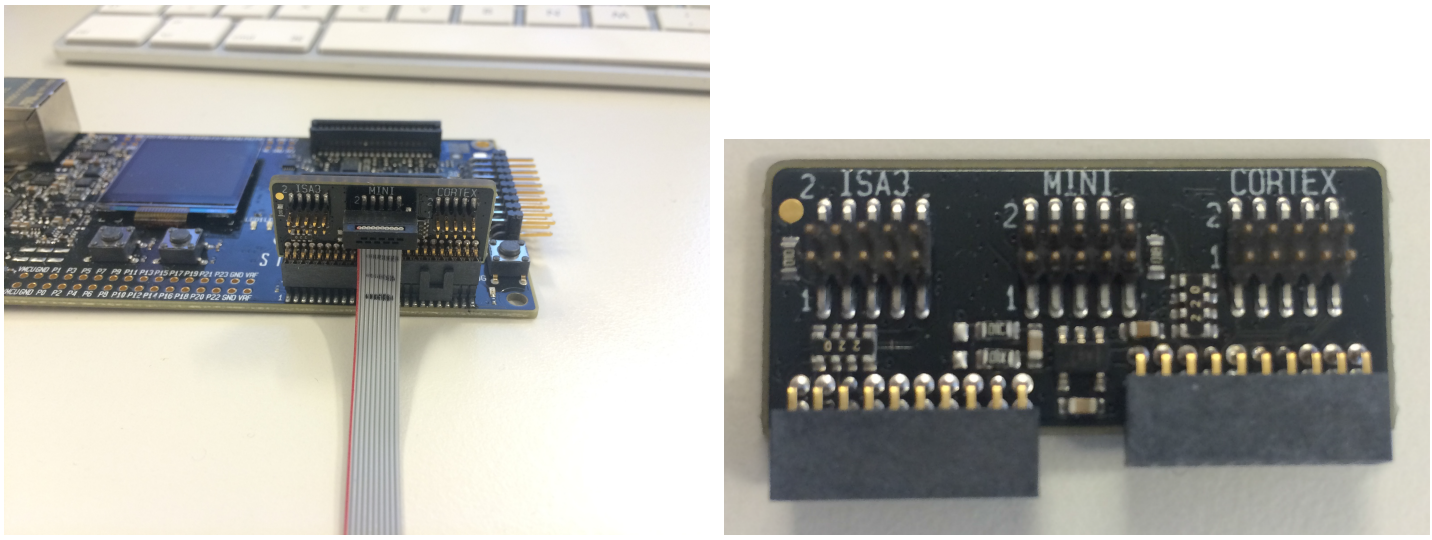


Figure 4.1. STK/WSTK Debug Adapter Board

In order to take advantage of these capabilities and features, Silicon Labs recommends including the Mini Simplicity Connector in the custom hardware design. Alternatively, if only serial wire / JTAG programming and debug capabilities are desired, a standard 10-pin ARM Cortex programming interface is available through the Cortex port of the adapter board.

4.1.1 Connector Pin-Out (MINI)

The figure below shows the pin-out for this 10-pin Mini Simplicity connector, while table below lists the pin functions associated with this pin-out.

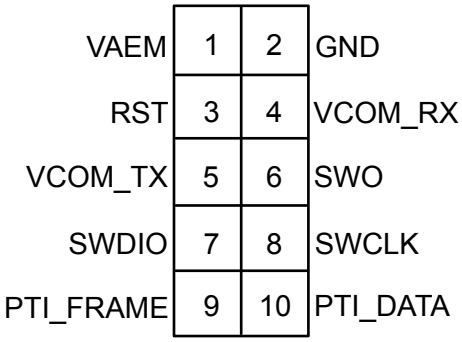


Figure 4.2. Mini Simplicity Connector Pin-Out

Table 4.1. Mini Simplicity Connector Pin Function

Pin #	Pin Name	Pin Function	EFR32 Functionality
1	VAEM	Target Advanced Energy Monitor Voltage Net	VDD
2	GND	Target Ground	VSS
3	RST	Target Reset (Active Low)	RESETn
4	VCOM_RX	Target Pass-through UART/Virtual COM Port Receive	US0_RX
5	VCOM_TX	Target Pass-through UART/Virtual COM Port Transmit	US0_TX
6	SWO	Target Serial Wire Output	SWO
7	SWDIO	Target Serial Wire Data Input/Output	SWDIO
8	SWCLK	Target Serial Wire Clock	SWCLK
9	PTI_FRAME	Target Packet Trace Interface Frame Signal	FRC_DFRAME
10	PTI_DATA	Target Packet Trace Interface Data Signal	FRC_DOUT

Note: Mini Simplicity Connector pin-out is referenced from the device target side.

Note: The power switch on the WSTK main board determines whether the WSTK VAEM pin sources current to the target. When this power switch is set to the “AEM” position, the WSTK is connecting VAEM to the target and monitoring current of the external target using AEM. If the target board requires external power supply, the power switch of the WSTK should be set to the “BAT” position, disconnecting the on-board regulator and AEM circuits.

4.1.2 Connector Pin-Out (Cortex)

The figure below shows the pin-out for this 10-pin standard ARM Cortex Debug Connector from the adapter board, while the table below lists the pin functions associated with this pin-out.

Note: Silicon Labs deviates from the ARM standard for this connector by not including the key pin.

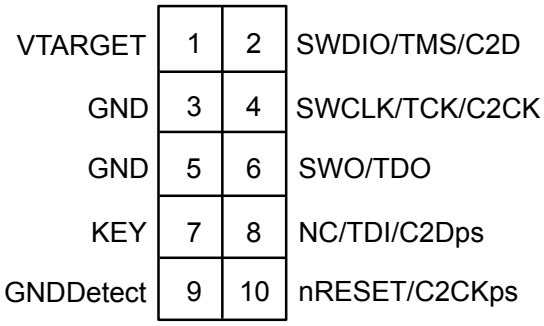


Figure 4.3. 10-pin Standard ARM Cortex Connector Pin-Out

Table 4.2. 10-pin Standard ARM Cortex Connector Pin Descriptions

Pin Number	Pin Name
1	VTARGET
2	SWDIO/TMS/C2D
3	GND
4	SWCLK/TCK/C2CK
5	GND
6	SWO/TDO
7	KEY
8	NC/TDI/C2Dps
9	GNDDetect
10	nRESET/C2CKps

4.1.3 Connector Pin-Out (ISA3)

This interface is not yet formally supported, but is intended to allow a WSTK interface to existing EM3x wireless products which include the 10-pin Packet Trace connector footprint.

4.1.4 Connector Part Numbers

The table below lists examples of connectors that can be placed on the customer design for this connector.

Table 4.3. Example Connector Part Numbers

Manufacturer	Manufacturer PN	Notes
Samtec	FTSH-105-01-L	—
Samtec	FTSH-105-01-L-DV	Add –K for keying shroud
Samtec	FTSH-105-01-L-DH	Right-angle
Samtec	FTSH-105-01-L-D-K	Through hole, add –K for keying shroud
Samtec	FTSH-105-01-L-D-R	Through hole, right-angle

4.1.5 Connector Footprint

For the recommended connector footprint, refer to the manufacturer specifications and recommendations in the applicable connector part data sheet.

4.2 Tag-Connect™ 10-pin Interface

If the same capabilities of the of the STK/WSTK Debug Adapter Interface (either through MINI or CORTEX port of the adapter board) are desired but the design is space constrained, a Tag-Connect™ 10-pin interface is a possible alternative. This interface maintains the 10-pin feature set and uses the same Mini Simplicity Adapter board, as noted in 4.1 STK/WSTK Debug Adapter/Connector Interface. This interface also uses a different cable (either TC2050-IDC-NL-050-ALL or TC2050-ICD-050-ALL) and utilizes a smaller footprint area on the custom target hardware board, given the lack of a connector required on the target hardware design. The NL version has no legs, while the standard version includes legs for locking the cable into place on the PCB. For additional details on the interface cable required for interfacing to the target hardware design for this option, see http://www.tag-connect.com/TC2050-IDC-050-ALL or http://www.tag-connect.com/TC2050-IDC-NL-050-ALL.

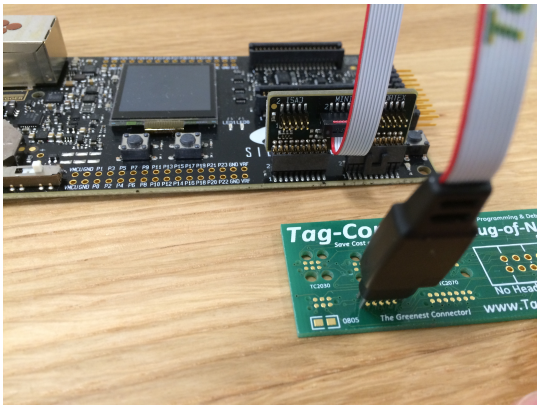


Figure 4.4. TC2050-IDC-NL-050-ALL Cable

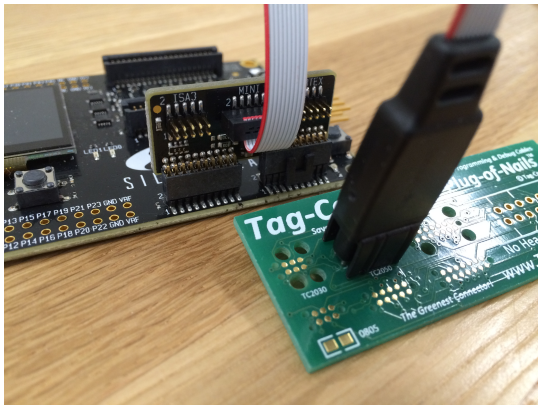


Figure 4.5. TC2050-IDC-050-ALL Cable

4.2.1 Interface Pin-Out

The pin-out for this interface is identical to the ones listed in Table 4.1 Mini Simplicity Connector Pin Function on page 7 or Table 4.2 10-pin Standard ARM Cortex Connector Pin Descriptions on page 8.

4.2.2 Interface Footprint

The footprint details for this interface on the custom target hardware board side can be found at http://www.tag-connect.com/Materials/TC2050-IDC%20Datasheet.pdf or http://www.tag-connect.com/Materials/TC2050-IDC-NL%20Datasheet.pdf.

4.3 Tag-Connect 6-pin Interface

If only a serial wire programming and debug interface is desired on the target hardware design, or space constraints prevent adding larger interfaces, a Tag-Connect 6-pin interface is a possible solution. This interface is similar to the Tag-Connect 10-pin interface but connects to the 20-pin Standard ARM Cortex Debug Connector directly and provides only 6-pins for serial wire debug capabilities only. The cable part numbers are TC2030-CTX-20-NL and TC2030-CTX-20. The NL version has no legs, while the standard version include legs for locking the cable into place on the PCB. For additional details on these cables, see http://www.tag-connect.com/TC2030-CTX-20 and http://www.tag-connect.com/TC2030-CTX-20-NL.

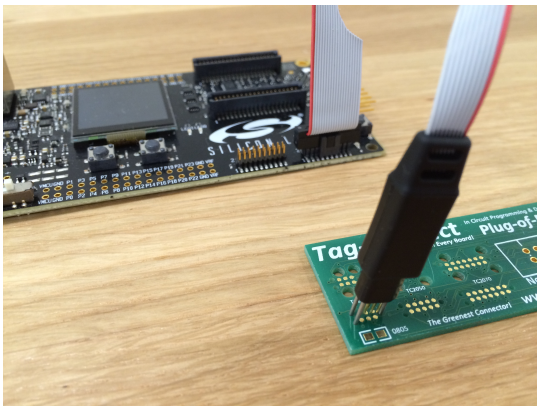


Figure 4.6. TC2030-CTX-20-NL Cable

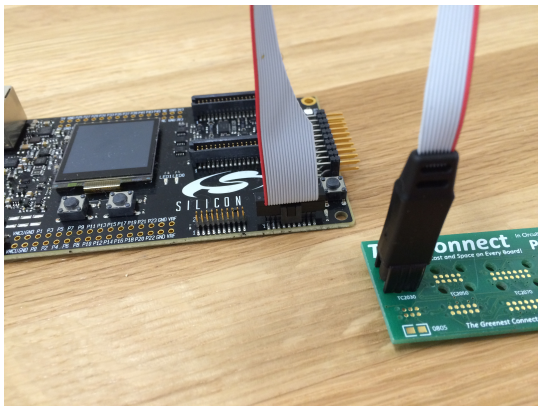


Figure 4.7. TC2030-CTX-20 Cable

4.3.1 Interface Pin-Out

The figure and table below show the pin-out and descriptions for this interface.

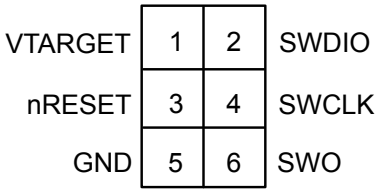


Figure 4.8. 6-pin Interface Pin-Out

Table 4.4. Pin Descriptions

Pin	Function
1	VTARGET
2	SWDIO
3	nRESET
4	SWCLK
5	GND
6	SWO

4.3.2 Interface Footprint

The footprint details for this interface to be placed on the custom target hardware board can be found at http://www.tag-connect.com/Materials/TC2030-IDC.pdf and http://www.tag-connect.com/Materials/TC2030-IDC-NL.pdf.

5. Special Considerations

5.1 IOVDD < Main Supply Voltage

In cases where IOVDD is less than the main supply voltage on the target hardware (for example, IOVDD at 1.8 V and main supply at 3.3 V), care needs to be taken when interfacing to the STK or WSTK main board. In the case where both the Simplicity Connector and ARM Cortex Debug+ETM Connector are connected to the target hardware, IOVDD should be connected to the VTARGET net of the debug connector, while the target main supply voltage net should be connected to the VAEM net of the Simplicity Connector. This ensures that the reference voltage for the target debug interface signals is correct. In this scenario, current measurements will be roughly 50–100 µA higher than normal due to powering of main board level shifters. When using the STK/WSTK Debug Adapter for some of the alternative interfaces detailed in 4. Alternative Interfaces, only the VAEM net is available and VTARGET is buffered from VAEM. In this case, the target IOVDD net needs to be connected to the debug adapter VAEM net in order for the main board level shifters to work properly, and there will be no target main supply connection to the Debug Adapter. Also, in this mode, the target power select switch needs to be set to BAT.

5.2 Network Co-Processor (NCP)

When the target hardware is a wireless network co-processor (NCP), care should be taken to ensure that the VCOM interface to the debugger does not utilize the same pins selected for the NCP interface (either SPI or UART), as this may cause contention of either the NCP operation or the VCOM serial port operation. If the VCOM interface is desired for test purposes and the same pins are selected for the NCP interface, such as for a QFN32 package or otherwise GPIO-constrained devices, series 0 Ω resistors are recommended in-line with the VCOM connection to the debugger (to be depopulated when the NCP application is running). This ensures no contention of NCP operation when the debugger is connected to the target device. In these situations, the best method may be to route (in layout) the resistor footprints to allow a connection between the EFR32 and the NCP, or between the EFR32 and the VCOM port, depending on placement of the 0 Ω resistor.

6. Related Documentation

AN124: Pin Sharing Techniques for the C2 Interface:

http://www.silabs.com/Support%20Documents/TechnicalDocs/AN124.pdf

AN0043: EFM32 Debug and Trace:

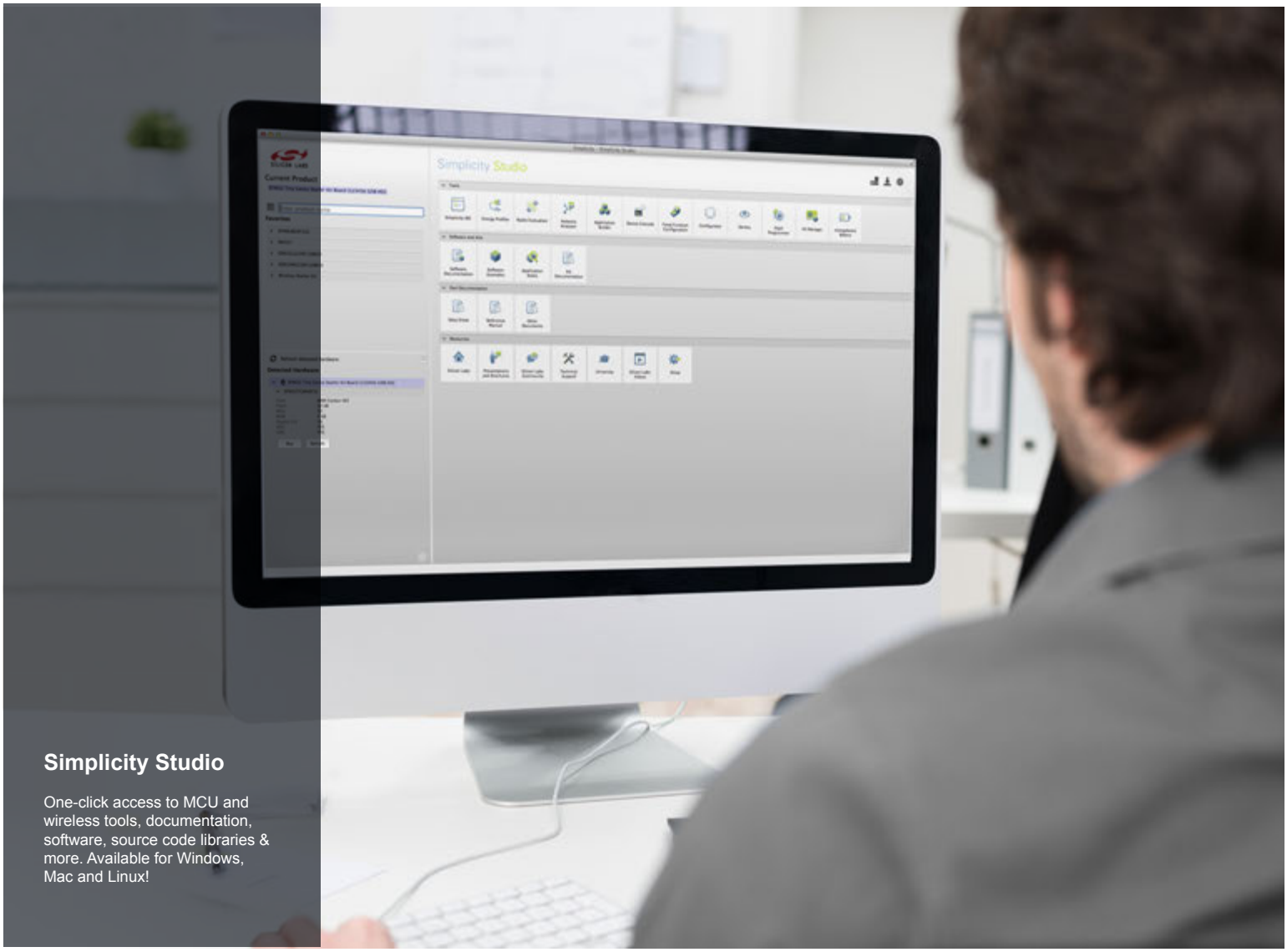
http://www.silabs.com/Support%20Documents/TechnicalDocs/AN0043.pdf

AN961: Bringing Up Customer Nodes for the Mighty Gecko and Flex Gecko Families:

http://www.silabs.com/Support%20Documents/TechnicalDocs/AN961-CustomNodesEFR32.pdf

UG162: Simplicity Commander Reference Guide:

http://www.silabs.com/Support%20Documents/TechnicalDocs/UG162-SimplicityCommanderReferenceGuide.pdf



Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!

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