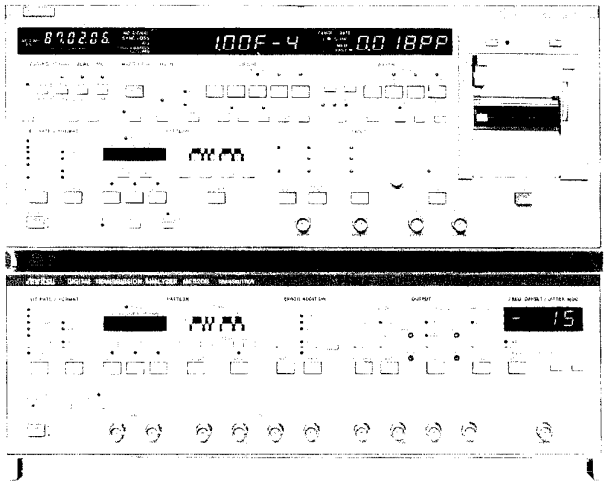
DIGITAL TRANSMISSION ANALYZER
ME520B

1 kHz to 150 MHz, 1 kHz to 170 MHz (with Option 02)



《GP-IB》

The ME520B is used to measure error rate and jitter of PCM signals with clock frequencies ranging from 1 kHz to 150 MHz (in which 1st to 4th order PCM hierarchy and 10 CH system are included).
It is possible to measure error rate and jitter simultaneously. Measured data are indicated on a digital display and analyzed at the same time. The analysis results, in combination with time/date, are printed out by an internal printer, thus, continuous measurement for long periods is possible.
The ME520B is best suited for development and maintenance of radio PCM, wired PCM, optical fiber systems or other digital communication systems.
Its transmitter and receiver are housed in separate cabinets, making end-to-end measurement possible. The transmitter generates M-sequence pseudorandom pattern signals and jitter modulated signals that are close to actual transmitted signals. The receiver receives signals from the system under measurement and detects error and the amount of jitter.
Furthermore, the ME520B can perform error analysis in accordance with the CCITT Rec. G.821, so the ME520B is indispensable for evaluation of international communication circuits.

Features

- Conforms to CCITT Recommendations
- Simultaneous measurement of error and jitter
- End-to-end measurement
- A variety of test patterns enable testing digital systems including PCM transmission over cables, radio and optical fiber links
  CMI pattern : 4 outputs
  Bipolar pattern : 4 outputs
  AMI, HDB3 code
  Unipolar pattern : 4 outputs
  Clock : 2 outputs
- Measuring pattern
  Pseudorandom : 2^{10}-1, 2^{15}-1, 2^{23}-1 bits
  Word pattern : Programmable 16 bits or 2 × 8 bits word
- Error addition
  Bit or code errors with 10^{-3}, 10^{-4}, 10^{-5} or 10^{-6} error rate or single error can be added to the sending pattern.
- Zero substitution
  The sequence can be disabled for 8 to 120 clock periods.
- Code error measurement is possible for actual line in service.

Specifications

• Transmitter

Bit rate	Internal clock	Bit rate	704, 2048, 8448, 34368, 68736, 139264 kbit/s
		Accuracy	±2 ppm, ±5 ppm/0° to 50°C
	External clock	Frequency	1 kHz to 150 MHz, (Option 02: up to 170 MHz)
		Amplitude	0.3 to 3 Vp-p, 1 kHz to 1 MHz (rectangular), >1 MHz (Sine or rectangular)
		Impedance	Nominal 75 Ω, unbalanced
		Duty cycle	50%
Clock output	Numbers		2 separate buffered outputs, common phase
	Polarity		CLOCK or CLOCK, selectable
	Level	TTL	High state ≙2.5 V, low state ≙0.5 V
		ECL	ECL level
		SET	Amplitude 1 to 2 V, offset 0 to ±2 V
	Format		Square wave, 50% ±10% duty cycle on internal clock
	Impedance		75 Ω, unbalanced

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■ PCM MEASURING INSTRUMENTS

Pattern	PRBS (Pseudorandom binary sequence)		$2^{15}-1$, $2^{20}-1$, $2^{23}-1$
	Word		Freely programmable digital word, adjustable length 1 to 16 bits Two 8-bit words, any possible setting (Can be changed over by an external control signal)
	Zero substitution		Sequence can be disabled for 8 to 120 of clock periods, in multiples of 8 clock periods.
Error pulse	Error addition	Error rate	10^{-3}, 10^{-4}, 10^{-5} and 10^{-6}, selectable
		Single error	1 error is produced for each depression of key.
	External error input	Impedance	Nominal 680 Ω, unbalanced to −5.2 V
		Frequency	DC to one fourth of the clock frequency
Output data	CMI	Bit rate	1 kbit/s to 150 Mbit/s
		Amplitude	1 ±0.1 Vp-p
		Numbers	4 separate buffered outputs, common phase
	Unipolar (RZ, NRZ)	Bit rate	1 kbit/s to 150 Mbit/s, (Option 02: up to 170 MHz)
		Level	TTL, ECL, SET, selectable [TTL: high state ≙2.5 V, low state ≙0.5 V] [SET: amplitude 1 to 2 V, offset 0 to ±2 V]
		RZ duty cycle	50% ±10% on internal clock
		NRZ width*	100% ±5%
		Numbers	4 separate buffered outputs, each delayed 4 bits
	Bipolar (RZ)	Bit rate	1 kbit/s to 50 Mbit/s
		Format	AMI, HDB3
		Amplitude	2.37 ±0.237 V/0 ±0.237 V or 1.0 ±0.1 V/0 ±0.1 V, selectable
		Numbers	4 separate buffered outputs, each delayed 4 bits
Jitter modulation	Function		Timing jitter can be added to the clock and data output signals by applying an external modulation source.
	Input	Frequency	DC to 5% or 2.5% of bit rate (see Fig. 1 and Table 1)
		Sensitivity	10 UIp-p/V (5 Hz)
		Impedance	Nominal 75 Ω, unbalanced to ground
	Output	Display	10.10 UIp-p, max.
	Jitter reference clock output	Level	ECL
		Impedance	Nominal low, unbalanced to ground
Pattern sync output	Pattern	PRBS	1 pulse/sequence
		2 to 16 bits word length	1 pulse/2 sequences
		1 bit word length	1 pulse/4 bits
		2 × 8 bit word length	1 pulse/sequence
GP-IB interface			Meets IEEE Standard 488.1
Ambient temperature, rated range of use			0° to 50°C
Power			AC 90 to 138 V or AC 180 to 250 V, 50/60 Hz, approx. 200 VA
Dimensions and weight			132.5H × 426W × 351D mm; approx. 11 kg

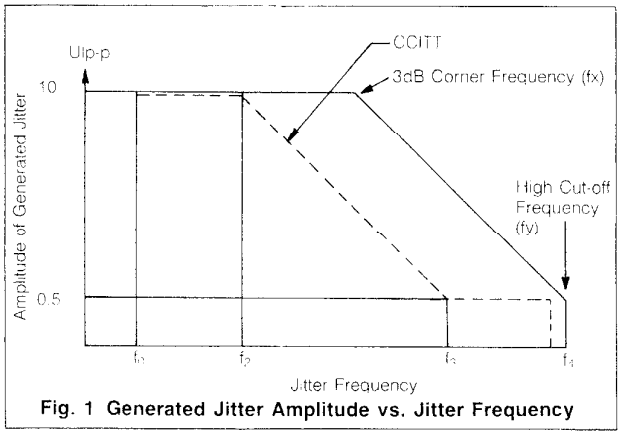

Fig. 1 Generated Jitter Amplitude vs. Jitter Frequency

Table 1 Jitter Frequency

	CCITT Rec. O.171				ME520B	
Bit rate (kb/s)	f_0 (Hz)	f_2 (kHz)	f_3 (kHz)	f_4 (kHz)	fx* (kHz)	fy* (kHz)
704	—	—	—	—	4.5	35
2 048	2	2.4	45	100	13	102
8 448	2	10.7	200	400	50	422
34 368	2	1.0	20	800	210	1 000
68 736	—	—	—	—	300	2 000
139 264	2	0.5	10	3 500	600	4 000
EXT	Can be modulated at internal rates ±10%					

*Typical figures

Note: When used in conjunction with the MH370A Jitter Modulation Oscillator, the ME520B can perform the maximum input jitter tolerance test according to the CCITT Rec. G.703. For details, please refer to the MH370A data sheet.

• Receiver

Bit rate	Clock recovery	Receiving rate	704, 2048, 8448, 34368, 68736, 139264 kbit/s
		Pulling range	±50 ppm (Jitter measurement), ±100 ppm (AMI), ±3% (HDB3), ±1% (68736 kbit/s CMI), ±3% (139264 kbit/s CMI)
		Format	AMI, HDB3 (704, 2048, 8448, 34368 kbit/s), CMI (68736, 139264 kbit/s)
	Clock input	Polarity	CLOCK or $\overline{\text{CLOCK}}$, selectable
		Frequency	1 kHz to 150 MHz (Option 02: up to 170 MHz)
		Amplitude	0.3 to 3 Vp-p
		Impedance	75 Ω, unbalanced
		Termination	Ground or nominal −2 V (via switch)
Pattern	PRBS (Pseudorandom binary sequence)		$2^{10}-1$, $2^{15}-1$, $2^{23}-1$
	Word		Freely programmable digital word, adjustable length 1 to 16 bits
	Zero substitution		Sequence can be disabled for 8 to 120 of clock periods, in multiples of 8 clock periods
Input data	RZ, NRZ input	Bit rate	1 kbit/s to 150 Mbit/s, (Option 02: up to 170 MHz)
		Threshold	−3 V to +3 V, ground or ECL, selectable
		Impedance	75 Ω, unbalanced
		Amplitude	0.3 to 3 Vp-p
		Polarity	DATA or $\overline{\text{DATA}}$, internally switched at the binary level
	CMI input	Threshold	Ground
		Impedance	75 Ω, unbalanced
		Amplitude	1 Vp-p automatic vf equalization
		Monitor mode	Additional gain 26 to 30 dB
		Polarity	DATA or $\overline{\text{DATA}}$, internally switched at the binary level
	AMI, HDB3 input	Impedance	75 Ω, unbalanced
		Amplitude	2.37 V/0 V (704, 2048, 8448 kb/s), 1 V/0 V (34368 kbit/s), Automatic vf equalization
		Monitor mode	Additional gain at 30 dB: 704, 2048, 8448 kbit/s Additional gain at 26 dB: 34368 kbit/s
		Polarity	DATA or $\overline{\text{DATA}}$, internally switched at the binary level
Error measurement	Bit error		Closed loop bit-by-bit detection at the binary level
	Code error	AMI	Bipolar violations are code errors
		HDB3	"Violation of violations" rule, i.e., two consecutive bipolar violations with same polarity
		CMI	"Violation of CMI coding rules," i.e., two consecutive bits, whose intervals are one full unit time, with same polarity.
	Block error		For PRBS only, the block length coincides with the length of the PRBS. Error is detected if a block contains one or more bit errors
	Pattern synchronization	Mode	Automatic or manual
		Sync gain	PRBS: No errors in 32 clock periods WORD: No errors in 32 to 512 clock periods
		Sync loss	PRBS: Approx. 10,000 errors in 30,000 clock periods WORD: Approx. 1,000 errors in 30,000 clock periods
Error display	Error rate	Display	0.00F MN ($0.00 \times 10^{(MN)}$), MN = 1 to 15 with automatic scaling
		Accuracy	Indication given if measurement result is based on < 100 errors
	Error count	Method	Totalizes errors over selected gating period
		Display	6-digit LED display with leading zero blanking When count exceeds 999999, display automatically changes to 0.00E00, with automatic round-up to a maximum count of 9.99E15 (9.99×10^{15})
	Error intervals	Method	Totalizes the number of intervals (1, 0.1, 0.01 s) which contain one or more errors (Intervals can be selected by the switch on rear panel.)
		Display	Same as error count
	Error-free intervals %	Method	Totalizes the number of intervals (1, 0.1, 0.01 s) during which no errors occur over selected gating period
		Display	6-digit LED display with leading zero blanking up to 100.000%

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Error performance display	%US (% unavailable second)			Displays % values including 4 digits of decimal part Error rate threshold: 1×10^{-2} to 1×10^{-4} Error count threshold: 1 to 999999, 1.00×10^{6} to 1.99×10^{7}
	%SES (% severely errored second)			Error rate averaged per 1 second or the total number of 1 second intervals exceeding threshold. Displays % values including 4 digits of decimal part Error rate threshold: 1×10^{-2} to 1×10^{-4} Error count threshold: 1 to 999999, 1.00×10^{6} to 1.99×10^{7}
	%DM (% degraded minutes)			Error rate averaged per 1 second or rate of time in which 1 minute error count exceeded threshold. Displays % values including 4 digits of decimal part Error rate threshold: 1×10^{-3} to 1×10^{-7} Error count threshold: 1 to 999999, 1.00×10^{6} to 1.99×10^{8}
	%ES (% errored second)			The total number of 1 second intervals containing at least one count error Displays % values including 4 digits of decimal part
Status display	Display			Live and last record of no signal, sync loss, AIS, < 100 errors
Jitter measurement	Range, accuracy	1 UI		0.000 to 1.010 UIp-p
		10 UI		0.00 to 10.10 UIp-p, ±4% ± additional error as shown in Table 3 (with HP1, LP)
	Jitter amplitude versus jitter frequency			Refer to Fig. 2 and Table 2
	Hit count	Display		When count exceeds 999999, display automatically changes to 0.00E00, with automatic round-up to a maximum count of 9.99E15 (9.99×10^{15}).
		Sensitivity		Typically ≧100 ns pulse width counted
		Hit threshold		Range 1: 0.05 to 0.5 UIp-p Range 10: 0.5 to 5.0 UIp-p
		Accuracy		Typically ±5%
	Hit intervals	Method		Totalizes the number of hit intervals (1, 0.1, 0.01 s). Intervals can be selected by the switch
				Other specifications are same as hit count.
	Hit-free intervals %	Method		Totalizes the number of intervals (1, 0.1, 0.01 s) during which no hits occur
		Display		6-digit LED display with leading zero blanking up to 100.000%
Gating period and real-time clock	Gating period	Setting		Manual, clock, time
		Display	Last data	Displayed data and status record is data in last gating period
			Current data	Displayed data and status record is data in current gating period.
	Real-time clock			Year, month, day, hour, minute, second
GP-IB interface				Meets IEEE Standard 488.1
Ambient temperature, rated range of use				0° to 50°C
Power				AC 90 to 138/180 to 250 V, 50/60 Hz, approx. 230 VA
Dimensions and weight				177H × 426W × 351D mm, approx. 15 kg

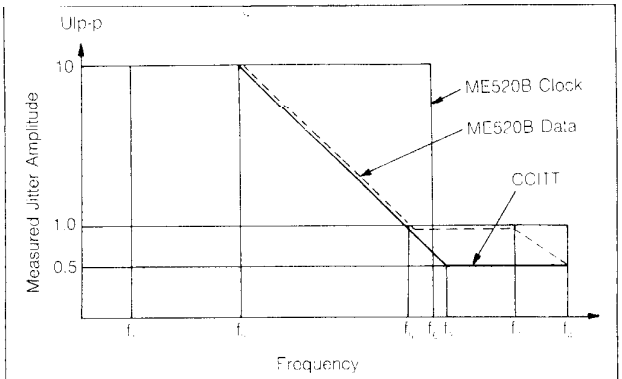

Fig. 2 Measured Jitter Amplitude vs. Frequency

Table 2 Jitter Frequency

Bit rate (kbit/s)	CCITT Rec. O.171				ME520B (typical)		
	f_4 (Hz)	f_2 (Hz)	f_3 (Hz)	f_1 (Hz)	f_5 (Hz)	f_6 (Hz)	f_7 (Hz)
704	(20)	(1 k)		(35 k)	7 k	8 k	10 k
2,048	20	2.4 k	45 k	100 k	24 k	27 k	30 k
8,448	20	10.7 k	200k	400 k	107 k	110 k	120 k
34,368	100	1 k	20 k	800 k	10 k	344 k	320 k
68,736	(100)	(40 k)	—	(1 M)	400 k	400 k	500 k
139,264	200	500	10 k	3.5 M	100 k	500 k	1.4 M

Table 3 Additional Error

Range	Additional error in UIp-p				
	Data		Clock		
	HDB3	CMI*	f ≦ 50 M	50 M < f ≦ 150 M	f > 150 M (OPT 02)
1 UIp-p	≦0.035	≦0.08*	≦0.01	≦0.02	≦0.03
10 UIp-p	≦0.12	≦0.24	≦0.1	≦0.2	≦0.3

* The residual jitter of 139264 kbit/s CMI signals can be improved by using the MI1547A Clock Recovery.

Ordering information

Please specify model/order number, name and quantity when ordering.

Model/Order No.	Name		Remarks
	Main frame		
ME520B	Digital Transmission Analyzer		
	Standard accessories		
J0126B	Coaxial Cord, 2 m:	4 pcs	BNC-P•3C-2V•BNC-P
J0017	Power Cord, 2.5 m:	2 pcs	
F0049	Fuse for ME520B Transmitter, 8 A:	2 pcs	MF51NN250V8ADC01
F0046	Fuse for ME520B Transmitter, 3.15 A:	1 pc	MF51NN250V3.15ADC01
F0042	Fuse for ME520B Transmitter, 0.8 A:	1 pc	MF51NN250V0.8ADC01
F0012 (F0011)	Fuse for ME520B Transmitter, 3.15 A or 2 A:	2 pcs	T3.15A250V/T2A250V (3.15 A is for AC 90 to 138 V, 2 A is for AC 180 to 250 V)
F0049	Fuse for ME520B Receiver, 8 A:	3 pcs	MF51NN250V8ADC01
F0043	Fuse for ME520B Receiver, 1 A:	2 pcs	MF51NN250V1ADC01
F0013 (F0012)	Fuse for ME520B Receiver, 5 A or 3.15 A:	2 pcs	MF51NN250V5AAC05/3.15AAC05 (5 A is for AC 90 to 138 V, 3.15 A is for AC 180 to 250 V)
Z0031A	Printer Paper:	3 sets	2 rolls/set
W0168AE	ME520B Operation Manual:	1 copy	
W0168BE	ME520B Service Manual:	1 copy	
	Options (factory assembly required)*		
ME520B-02	170 MHz Operation		Format: NRZ, RZ
ME520B-04	External Data for Transmitter		Error addition, jitter modulation and code conversion into external pattern data are available.
ME520B-21	35.008 MHz Internal Clock for Transmitter		Format: NRZ, RZ
ME520B-22	41.2416 MHz Internal Clock for Transmitter		Format: NRZ, RZ
ME520B-23	104.448 MHz Internal Clock for Transmitter		Format: NRZ, RZ
ME520B-24	141.040 MHz Internal Clock for Transmitter		Format: NRZ, RZ
ME520B-25	141.248 MHz Internal Clock for Transmitter		Format: NRZ, RZ
ME520B-26	141.475 MHz Internal Clock for Transmitter		Format: NRZ, RZ
ME520B-27	167.1168 MHz Internal Clock for Transmitter		Format: NRZ, RZ (Option 02 is also necessary)
ME520B-29	32.064 MHz Internal Clock for Transmitter		Format: NRZ, RZ
ME520B-30	110.592 MHz Internal Clock for Transmitter		Format: NRZ, RZ
ME520B-32	143.360 MHz Internal Clock for Transmitter		Format: NRZ, RZ
ME520B-33	30.720 MHz Internal Clock for Transmitter		Format: NRZ, RZ
ME520B-35	25.776 MHz Internal Clock for Transmitter		Format: NRZ, RZ
ME520B-36	8.192 MHz Internal Clock for Transmitter		Format: NRZ, RZ
ME520B-37	70.848 MHz Internal Clock for Transmitter		Format: NRZ, RZ
ME520B-38	34.724 MHz Internal Clock for Transmitter		Format: NRZ, RZ
ME520B-40	168.443 MHz Internal Clock for Transmitter		Format: NRZ, RZ (Option 02 is also necessary)
ME520B-42	35.840 MHz Internal Clock for Transmitter		Format: NRZ, RZ
ME520B-43	35.9391 MHz Internal Clock for Transmitter		Format: NRZ, RZ
ME520B-44	155.520 MHz Internal Clock for Transmitter		Format: NRZ, RZ (Option 02 is also necessary)
ME520B-45	125.000 MHz Internal Clock for Transmitter		Format: NRZ, RZ
	Optional accessories		
MB23A	Portable Test Rack		Tilt angle type
MB24A	Portable Test Rack		Fixed table type
MP35A	Matching Transformer, 75 Ω unbal/120 Ω bal		Fits to Siemens C42334 A282
MP547A	Clock Recovery Unit (139264 kbit/s, CMI)		Residual jitter: <0.025 UIp-p, HP1 – LP, 25° ± 10°C
J0081	Coaxial Cord, 2 m		3CV-P2•3C-2V•3CV-P2
J0008	GP-IB Cable, 2 m		
B0064	Soft Case		B0019 also required for transmitter.
B0065	Soft Case		B0020 also required for receiver.
B0066	Transport Case		B0019 and B0064 required for transmitter.
B0067	Transport Case		B0020 and B0065 required for receiver.
B0019	Protective Cover (for transmitter)		2 pcs are necessary for front/rear panel
B0020	Protective Cover (for receiver)		2 pcs are necessary for front/rear panel
B0042	Rack Mount Kit		
B0043	Rack Mount Kit		

*Options for equipment are set at the time of shipment, and cannot be sold separately. With the exception of ME520B-02, only one option may be ordered per main frame.