

**ADVANCED SYSTEM  
CONTROLLER  
ASC/2S  
MAINTENANCE MANUAL**

P/N 37539-05

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### **ASC/2S FAMILY**

The ASC/2S family of actuated controllers consists of three models. Each provides the same control functions but uses a different type of input/output (I/O) structure to interface with other components of the traffic control cabinet.

The first model, the ASC/2S-1000, provides an I/O interface conforming to NEMA TS2 standard requirements for Type 1 controllers. This interface controls all cabinet I/O over a serial communications channel (Port 1). This serial communications channel is used for data exchange with a Malfunction Management Unit (MMU), to retrieve vehicle detector data from detector racks and interface to Terminals and Facilities within the traffic control cabinet. All I/O functions are handled by one or more Bus Interface Units (BIUs). Each BIU controls up to 15 outputs, 24 input/outputs, 8 inputs and four optically coupled inputs. Type 1 I/O also includes EIA-232 compatible terminal (Port 2) and telemetry (Port 3) interfaces.

The second model of the ASC/2S family, the ASC/2S-2000, has an I/O interface that conforms to both NEMA TS1 and TS2 Type 2 controller requirements. This interface controls I/O functions through industry standard circular connectors (A, B, & C) and includes the serial communications, terminal, and telemetry interfaces of the Type 1 interface. TS1 operation allows the ASC/2-2000 to be used in existing traffic control cabinets without any cabinet changes. The Type 2 I/O operates in one of eight I/O modes. Each mode assigns specific functions to 24 input and output connections. The first I/O mode (Mode 0) provides compatibility with the I/O requirements of the NEMA TS1 standard. This TS1 operational mode is selected by setting the Type 2 I/O mode to Mode 0 (default) and disabling the serial communications channel.

The serial communications channel of the Type 2 interface is used to communicate with a Malfunction Management Unit and detector racks as with the Type 1 interface. However, a minimum of 20 vehicle detectors can optionally be connected directly to the controller using one of the Type 2 I/O modes. The ASC/2S-2000 can also be programmed to operate as a Type 1 controller. In this mode external I/O interface is disabled and all I/O functions are handled over the serial communications channel. This allows the ASC/2S-2000 to duplicate the operation of the ASC/2S-1000.

The ASC/2S-2100 is the third model of the ASC/2S actuated controller family. The ASC/2S-2100 Processor-I/O module includes components that add additional I/O to the ASC/2S-2000 capabilities described above. The expansion I/O components include the "D" connector, 25-pin telemetry connector, and optionally, the NEMA overlap card connector interfaces matching those of the ASC-8000. This allows the ASC/2S-2100 to be used as a replacement for an ASC-8000 or ASC/2-2100 in existing traffic control cabinets without any cabinet changes.

## INTRODUCTION

### ASC/2 FAMILY

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The ASC/2S family of actuated controllers are made of a formed aluminum enclosure. Controller fronts consist of the User Interface panel and the Connector Interface panel. The User Interface panel consists of a custom, weather and dust-proof conductive rubber keyboard with numeric, function and cursor keys, and a high-contrast 16 line by 40 character liquid crystal display with LED back lighting. The Connector Interface panel contains two fuses (115 VAC/1 Amp and +24 VDC/ 0.75 Amp) and various interface connectors. The type of connectors depends on the controller model.

The ASC/2S controller unit contains two main electronic modules and a power supply. The first main module is the Processor-I/O module which is installed directly in the enclosure. This module contains the MC68302 microprocessor which controls all ASC/2S operations and circuitry that transfers input and output signals between the I/O connectors and the processor. Also located on the Processor-I/O module is a connector for installing a telemetry module. The second main module is the User Interface assembly mounted to the hinged front panel. All versions of the ASC/2S controller use the same modules. The model type is defined by the components installed on the Processor-I/O module. The Processor-I/O and User Interface modules are interconnected by a ribbon cable located across the front panel hinge. The Processor-I/O module together with the connector interface panel, is held in place by two quarter turn fasteners and a card guide. The User Interface panel is held in place by 3 nuts. Both modules may be easily removed.

The ASC/2S power supply furnishes +24VDC for controller unit operation. It is mounted internally on the back panel of the enclosure. The power supply is held in place four screws and is connected to the processor-I/O module by two wire harnesses.

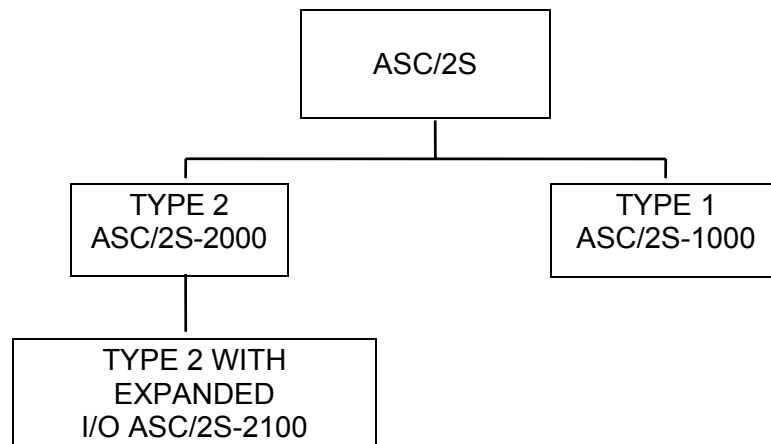


Figure 1-1. ASC/2S Family



**MANUALS****Programming Manuals**

Programming of the ASC/2S controller unit is covered in the ASC/2S programming manual. However, maintenance information is provided for all ASC/2S family members in this manual.

**Maintenance Manual**

This manual contains the information needed to understand the hardware functions of the ASC/2S controller family. Information about the circuitry, general maintenance requirements, installation and disassembly is included. Fault isolation charts are provided to help the technician isolate problems or to at least provide a good starting point for troubleshooting. Schematics and comprehensive parts lists are included as well as several appendices to supplement the hardware descriptions.

Section II contains the ASC/2S theory of operation beginning with a functional description of each module followed by a detailed description of circuit operation.

Section III is a collection of procedures and check lists that should be used as part of regular maintenance. Included are procedures for installation, disassembly, visual inspection, cleaning, battery check, and various adjustments. Test equipment and connector-cable assignment lists are included. ASC/2S diagnostic tests, the primary method for hardware verification and fault isolation, are explained.

Section IV is a troubleshooting chart. The chart outlines a series of possible hardware, software, and programming problems with associated possible causes and suggested solutions.

Section V contains controller assembly parts lists. It lists components, cables and assemblies with both Econolite and manufacturer's part numbers.

Section VI contains schematics and assembly drawings.

Appendix A contains cable diagrams to be used when interfacing the ASC/2S to a printer or personal computer or for data transfer.

Appendix B contains pin lists for all connectors A-D, SDLC, Terminal and Telemetry.

Appendix C describes standard system interconnection using Econolite telemetry interface boards and transient suppressors.

Appendix D is a guide to lease-line installation used in Econolite system communication.

Appendix E lists and identifies loopback diagnostic error codes.



**FUNCTIONAL DESCRIPTION**

This section begins with a functional description of the ASC/2S modules. Each module is then described in detail. The circuit and signal descriptions are best understood when studied together with the block diagrams and system schematics. The block diagrams are included in this section and schematics are located in Section VI.

As an aid to finding circuitry described in the detail text, schematic zone references, which contain the schematic coordinates of the circuitry, are included in the text where pertinent. A schematic zone reference has the format [(D),N,X,Y] where (D) is the optional document number, N is the schematic page, X is the horizontal coordinate and Y is the vertical coordinate of the page. The document number is normally referenced at the beginning of each new section. Also, all part numbers, pin, and signal names are printed in **bold type**.

Figure 2-1. ASC/2S System Block Diagram

## **Processor Module**

### **Processor Module**

The Processor-I/O module contains the microprocessor chip, memory chips and support circuitry required to operate and control all ASC/2S functions. This module also includes all I/O circuitry and controls the User Interface module keyboard and display operations. Ribbon connector **J3** connects this module to the User Interface module.

The system busses include the address bus that identifies the device or memory location targeted for information exchange, the data bus, which carries the information, and the control bus which synchronizes the data transfers. The communications busses include the Telemetry bus, SDLC bus and Terminal bus which transfer serial data between the microprocessor and the dual asynchronous receiver transmitter (DUART) chips and their associated interface chips.

The Processor-I/O module is connected to the power supply module via connectors **J18** and **J19**. The power supply provides +24VDC.

Auxiliary processor functions include a watchdog timer which checks for proper program operation, the voltage monitor which checks for power fail conditions, and the battery-backed clock circuit which keeps accurate time when power is removed from the unit. System RAM is powered by the rechargeable, backup battery circuit so that data integrity is maintained during power fail conditions.

Also included on the module are the AC line transient protection circuit and line referenced, 120Hz interrupt generator.

The I/O interface section connects external inputs and outputs, with the microprocessor system address, data and serial communications busses. This allows the microprocessor to perform all input and output functions.

## THEORY OF OPERATION FUNCTIONAL DESCRIPTION

## I/O Interface Module/Power Supply Module

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### I/O Interface Modules

The I/O section of the Processor-I/O module consists of input multiplexers, logic level translators, output latches, output drivers, serial communications interface circuits, the telemetry module interface connector **J4** and expansion I/O connector **J1** (unused).

External parallel inputs are applied through front panel connectors **A**, **B** and **C**. The input voltage levels are translated to logic levels to be used by the system. The TRUE/FALSE (LOW/HIGH) states are then applied to input multiplexers. The processor reads the input status by addressing the input and enabling the multiplexer, thus transferring the input status onto the system data bus.

The processor uses output latches to control the external parallel signals. It addresses a specific output and latches that output status from the data bus by enabling the latch. The signal is then sent to external connectors **A**, **B** or **C**. In the event of a long power failure, the latches are cleared to prepare for an orderly controller re-start.

The Terminal bus signals interface with external equipment through Terminal connector **J13** (PORT 2). It is used to communicate with printers, computer terminals or other controllers in the ASC family.

The SDLC bus signals interface with optional Bus Interface Units and/or a Malfunction Management Unit via SDLC connector **J15**(PORT 1).

The Telemetry bus signals attach to connector **J4** and supply the signals required for FSK and EIA-232/fiber optic telemetry interconnects. Once translated by the Modem module, the signals interface with external signals via connectors **J17**(PORT 3) and **J14** on the model ASC/2S-2100.

VOLTAGE MONITOR CONTROL is generated by monitoring the power supply and battery voltages and Processor signals. It is output to external equipment as VOLTAGE MONITOR.

When the processor-I/O module is configured as an ASC/2S-2100 it includes type D and 25-pin Telemetry connectors and associated input multiplexers, logic level translators, output latches and output drivers. External parallel inputs and outputs are processed as mentioned above. A plug-in NEMA overlap programming card (optional) is connected to the input multiplexers by connector **J6**. When programmed, the overlap inputs are read by the processor in the same way as external inputs.

### Power Supply Module

The Power Supply module is a 40 watt, 24 volt off-line switching supply set for 120VAC operation. When configured as an ASC/2S-2000 or ASC/2S-2100 controller, input power is applied through the A-connector on the controller front panel and then routed, via the AC line transient protection circuit, to **J19** on the I/O module. A wire harness connects between **J19** and the power supply module. When used in the ASC/2S-1000 controller, input power is applied through MS connector **J16** on the front panel and then routed to the power supply module as mentioned above. The +24VDC output from the supply is routed back to the Processor-I/O module via a wire harness connected to **J18**.

### Telemetry Module

The Telemetry module operates as a transceiver providing communication between the ASC/2S-1000, ASC/2S-2000 or ASC/2S-2100 and an ASC/2M-1000 or KMC-10000 master controller. The module is controlled by the Processor module and interfaces with to the Telemetry bus via connector **J4**. Transmit, and receive signals are interfaced through the Telemetry connector(s) on the front panel.

### Transceiver Operation

Communication between the local and master controllers is achieved over voice grade four-wire (two data channels) type 3002 leased telephone lines, or customer owned cable. The telemetry data channel is made up of command (master to local) and readback (local to master) lines. Additional lease-line information is found in Appendix D. Each local transceiver is assigned a unique telemetry address used by the master to identify the transceiver. The address is assigned by either direct keyboard entry (refer to the ASC/2S Programming Manual) or by activating External Address Enable (**J14-15**) and assigning the desired bit pattern to the appropriate D-connector system inputs (refer to Appendix E). Devices connected to the local transceiver are identified by subaddresses assigned and used by the master.

The master generates command messages containing local telemetry address, message type, subaddress, data, and a horizontal parity word. Command messages are transmitted to the local transceiver in a predefined sequence. The sequence begins with a zero address command which simultaneously transmits, to all local controllers, the system traffic program and four special functions. Local controllers do not respond to the zero address command. Subsequent messages request the status of the devices (listed above) connected to the local transceiver. The addressed local controller sends an appropriate response to the master on the readback line. Transmission of commands and readbacks occurs simultaneously. An error status is generated if a readback is not received by the master within a predefined period. For more information on master controller operation using telemetry, refer to the ASC/2M-1000 or KMC 10,000 Master Programming and Maintenance Manuals.

At the local transceiver, modulated command message signals are transformer coupled to the receiver where they are filtered and demodulated to a serial-bit pattern. The serial-bit pattern is converted by an SCC receive channel on the microprocessor into a parallel pattern, four-word command message which is read by the microprocessor. If the message address corresponds to that of the local transceiver and if the message is valid, the microprocessor performs the operation specified by the message type. Where readbacks are required, the local transceiver generates a three-word readback message containing the requested data and horizontal parity word. The three data words from the microprocessor are converted to a serial bit pattern by a transmit channel on the DUART. The serial bit pattern is then sent to the MODEM which provides frequency shift key (FSK) modulation for transmission. Valid data, transmit, and received carrier LEDs are ON or flash during normal data transmission.

## THEORY OF OPERATION DETAILED DESCRIPTION

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This section contains detailed descriptions of the various ASC/2S modules. Each module is described in detail with references to schematics in the format [(D),N,X,Y] where (D) is the document number, N is the schematic page, X is the horizontal coordinate and Y is the vertical coordinate of the page. The document number (D) is not always provided in this format but it is normally referenced at the beginning of each new section. Part numbers are identified in parenthesis (###) immediately before references to schematic coordinates. Example: **U24** (74HCT244) [4,2,C]. Pin and signal names are also printed in **bold type**.

The schematics are found in Section VI of this manual. Also, a module block diagram is shown before the discussion of each module. These block diagrams illustrate general functional operation.



Figure 2-2. Processor Section Block Diagram

Figure 2-3. I/O Section Block Diagram

Figure 2-4. Processor-I/O Module Component Placement

**Processor Module (Schematic document number 34251, pages 1-20)**

Microprocessor

The ASC/2S family of controllers uses the Motorola MC68302 integrated multiprotocol processor. This is a Very Large Scale Integration (VLSI), CMOS device which includes a 16-bit, 68000 core processor, a system integration block and a (RISC) communications processor.

Features of the system integration block that are used by the ASC/2 include: the independent DMA controller, a 19-level interrupt controller, the dual port RAM area, three programmable timers, the four programmable chip select lines, sixteen parallel I/O lines, the on-chip clock generator and several other "glue logic" functions.

The communications processor provides the following functions: the main controller (RISC Processor), three independent full-duplex serial communications controllers (SCC), six serial DMA channels for the three SCCs and an SCP channel for synchronous peripheral communications.

The following is the microprocessor signal description. All relevant information about the microprocessor signals and their associated control circuits is discussed.

Clocks

The system clock synchronizes the internal operations of the microprocessor and all external devices on the system busses. Microprocessor timing is controlled by a 14.7456 MHz crystal attached to the on chip clock generator circuit through pins **EXTAL** and **XTAL** [2,2,B]. The system clock rate is 14.7456 MHz. This system clock is output by the processor on the **CLKO** pin [2,2,B]. The **CLKO** signal is divided by four by **U21** (GAL16V8) [4,4,D], to provide a 3.6864 Mhz clock to DUART **U20** (SCN2681)[4,5,A]. **U20** divides the 3.6864 MHz clock by 96 and outputs a 19,200 Hz clock (16 X 1200 baud) on **OP3** [4,5,A] for the external transmit clock inputs of SCC1 (**TCLK1**) and SCC2 (**TCLK2**) on processor chip **U12** [2,5,C]. This signal is also used to trigger the processors data request line **/DREQ** [2,5,B] of the independent DMA controller which transfers data to the LCD module.

System Control Pins

**/RESET** is a bi-directional pin, acting as an input and when asserted along with the **/HALT** pin [2,3,B], it causes a total system reset. The **/RESET** and **/HALT** signals are generated by a combination of **U11** (74LS09), **U5** (14538b) [8,2-4,B-C] and **U4** (LM2598-5.0) [3,5,B]. **U4** holds the **PWRGOOD** signal low anytime VCC is out of tolerance. If the program running in the processor fails to toggle the **/WDOG** signal [8,5,B], the **U5** watchdog timer circuit will time out and generate a reset pulse. The **/RESET** pin can also act as an output which allows the program to output a **/RESET** signal to peripheral devices.

**/BERR**, **BUSW**, **DISCPU** and **/FRZ** pins are not used.

### System Busses

#### Data Bus (D0-D16)

This 16-bit, bi-directional, three-state bus is the general-purpose path for exchanging data with memory and other system devices. It can transmit and accept data in either byte or word widths. For all 16-bit accesses, byte 0, the high-order byte of a word, is available on **D8-D15** and the low-order byte is available on **D0-D7** [2,3,C]. The low order data lines are buffered by the system data buffers before being routed to the various I/O circuits. Buffering to the parallel I/O section is performed by **U25** (74HCT245) [4,4,D]. Unbuffered data signals are labeled **D(n)** and buffered signals are labeled **BD(n)**. Buffering to the User Interface panel is performed by **U38** (74HCT245) [10,5,C]. Unbuffered data signals are labeled **D(n)** and buffered signals are labeled **FPD(n)**.

#### Address Bus (A1-A23)

Pins **A1-A23** [2,3,D] form a 24-bit address bus when combined with the **/LDS** and **/UDS** pins [2,3,B]. The address bus is a bi-directional, three-state bus capable of addressing 16M bytes of data. On the ASC/2S, address lines **A21-A23** are not used. All address lines are buffered before being routed to the various I/O circuits. Buffering to the parallel I/O section is performed by **U24** (74HCT244) [4,2,C]. Unbuffered address signals are labeled **A(n)** and buffered signals are labeled **BA(n)**. Buffering for the User Interface panel is performed by **U39** (74HCT244) [10,5,B]. Buffered address signals are labeled **FPA(n)**.

#### Control Bus

This is a multipurpose bus that includes all the Processor-I/O modules chip select, write enable and output enable signals. These signals are used to control communications with the various RAM and EPROM devices, parallel I/O devices, the data module and the User Interface module. The control bus signals are generated by the decode and control section. These signals will be explained when their associated circuitry is discussed.

#### Telemetry Bus

This bus contains the serial data and hand shaking signals which are routed to the Telemetry module connector. Signals included in this bus are: the receive data line **RXD1** [2,5,D] which inputs serial data into SCC1 on the processor, the transmit data line **TXDA** [4,5,B] which transmits data out of **U20** and **/CTSA**, **/RTSA**, **/CDA**, **MDCTL1** and **MDCTL2**, generated by **U20** [4,5,B], which control communications handshaking and provide modem control.

#### Terminal Bus

This bus contains the serial data and hand shaking signals which are routed to the Terminal Port (PORT2) RS-232 interface chip **U80** (MAX214) [7,2,C]. Signals included in this bus are: the receive data line **RXD2** which inputs serial data into SCC2 on the processor, the transmit data line **TXD2** which transmits data out of SCC2, **/CTS2**, **/RTS2**, and **/CD2** generated by SCC2 [4,6,C] and **/DTRT** generated by **U20** [4,5,A] which control communications handshaking and provide modem control.

#### SDLC Bus

This bus contains the serial data and clock signals which are routed to the SDLC Port (PORT1) RS-485 interface chips **U81** and **U82** (LT490) [7,D,6]. Signals included in this bus are: the receive data line **RXD3**, which inputs serial data into SCC3 on the processor, **TXD3** which outputs serial data from SCC3 and transmit and receive clocks **TCLK3** and **RCLK3** [2,5,C] which are required to synchronize communications over the SDLC channel.

### SPI Bus

This bus contains the serial data, clock and handshake signals which are used for communications with **U3** (68HC68T) [8,4,D], the battery-backed clock. Signals included in this bus are: serial transmit data line **SPTXD**, serial receive data line **SPRXD**, synchronizing clock line **SPCLK** and slave select line **SS** [2,5,C].

### Decode And Control

This section takes the microprocessors address, data strobe, address strobe, read/write, chip select and clock signals and combines them in various ways to generate the control bus signals required for proper interaction between devices on the Processor-I/O module and the User Interface panel. These signals will be discussed below. All signals starting with a slash character i.e. /xxx are low only when active otherwise they are normally high.

**CLKO** [2,2,D] outputs the 14.7456 MHz system clock.

**/AS** [2,3,B] indicates when there is a valid address on the address bus (/AS is not used outside the processor chip in this design.).

**R/W** [2,3,B] defines the data bus transfer as a read or write cycle. It is HIGH during a read and LOW only during a write cycle.

**/UDS** [2,3,B] is the upper data strobe signal. It controls the flow of data on data bus lines **D8-D15** by specifying when valid data should be on the bus.

**/LDS** [2,3,B] is the lower data strobe signal. It controls the flow of data on data bus lines **D0-D7** by specifying when valid data should be on the bus.

**/CS0-/CS3** [2,3,A] are the four system chip select signals. **/CS0** is the primary chip select for all EPROM accesses. **/CS1** selects the RAM bank. **/CS2** is the chip select signal for the data module **/CS3** is the primary chip select for all I/O accesses. Address decoding and **DTACK** and Wait-State generation for these signals is performed onboard the processor chip.

**RESETB** [2,5,B] is an active high reset signal for the DUART (SCN2681) **U20** [4,5,A].

**/WEO** [4,5,D] is the write enable signal for the odd addressed RAM chip. This signal is generated by **U14B** (74ALS32) [4,6,D] by ORing the lower data strobe **/LDS** from the processor and the gated read/write signal **GR/W** from **U21** (GAL16V8) [4,4,D]. **GR/W** is held inactive when **VCC** fails which write protects the RAM when power is removed.

**/OEO** [4,5,D] is the output enable signal for the odd addressed RAM and EPROM chips and the data module. This signal gates the data from the device onto the data bus allowing the processor to read the data. This signal is generated by **U14A** (74ALS32) [4,6,D] by ORing the lower data strobe **/LDS** with the inverted read/write line **/RW**. **/RW** is generated by **U15A** (74ACT04) [4,5,C] by inverting the **R/W** signal from the processor.

**/WEE** [4,5,D] is the write enable signal for the even addressed RAM chip. This signal allows the processor to write data from the data bus into the device if the devices chip select line is active. This signal is generated by **U14D** (74ALS32) [4,6,C] by ORing the upper data strobe **/UDS** from the processor and the gated read/write signal **GR/W** from **U21** (GAL16V8) [4,4,D]. **GR/W** is held inactive when **VCC** fails which write protects the RAM when power is removed.

**/OEE** [4,5,D] is the output enable signal for the even addressed RAM and EPROM chips. This signal gates the data from the device onto the data bus allowing the processor to read the data. This signal is generated by **U14C** (74ALS32) [4,6,D] by ORing the upper data strobe **/UDS** with the inverted read/write line **/RW**. **/RW** is generated by **U15A** by inverting the **R/W** signal from the processor.

**/CS0L** [4,3,C] is the chip select signal for the onboard flash EPROM chip. This signal is generated by **U13** (GAL16V8) [4,4,C] by combining the main EPROM chip select line **/CS0** from the processor with **A20**. **/CS0L** is active for the address range \$000000-\$0FFFFFF

**/CS0H** [4,3,C] is the chip select signal for the off board flash EPROM memory space. This signal is generated by **U13** (GAL16V8) [4,4,C] by combining the main EPROM chip select line **/CS0** from the processor with **A20**. **/CS0H** is active for the address range \$100000-\$1FFFFFF

**/CS1L** [4,3,C] is the chip select signal for the onboard RAM chips. This signal is generated by **U13** (GAL16V8) [4,4,C] by combining the RAM chip select signal from the processor **/CS1** and **A16**. This signal utilizes the fact that GAL16V8 outputs float when power is removed. This eliminates a current path out of the RAM chips during battery backup operation thus extending battery life.

**/CS1H** [4,3,C] is the chip select signal for the off board RAM memory space. This signal is generated by **U13** (GAL16V8) [4,4,C] by combining the RAM chip select signal from the processor **/CS1** and **A16**. This signal utilizes the fact that GAL16V8 outputs float when power is removed. This eliminates a current path out of the RAM chips during battery backup operation thus extending battery life.

**/CSWE** [4,3,C] is the write enable signal for the data module. This signal allows the processor to write data from the data bus into the device if the devices chip select line is active. This signal is generated by **U13** (GAL16V8) [4,4,C] by combining input signals **GR/W**, **A9-A13** and the input from the EEPROM write protect jumper **JP3** [4,4,B]. **A9-A13** are used to differentiate between the write-protected and non write-protected areas of the module.

**/SWAPCS0** [4,4,C] is used during flash EPROM download module.

**3.6864** [4,3,D] provides a 3.6864 Mhz clock signal to the DUART **U20** (SCN2681) [4,6,A]. This signal is generated by **U21** (GAL16V8) [4,4,D] by dividing the system clock **CLKO** by four.  
STOP HERE

**/DWEO** [4,3,D] is the write enable signal for DUART **U20** (SCN2681) [4,6,A]. This signal allows the processor to write data from the data bus into the device if the devices chip select line is active. This signal is buffered version of **/WEO** and is generated by **U21** (GAL16V8) [4,4,D].

**/DOEO** [4,3,D] is the output enable signal for DUART **U20** (SCN2681) [4,6,A]. This signal gates the data from the device onto the data bus allowing the processor to read the data. This signal is buffered version of **/OEO** and is generated by **U21** (GAL16V8) [4,4,D].

**/DUART** [4,3,D] is the DUART chip enable line. This signal is generated by **U21** (GAL16V8) [4,4,D] by combining the system I/O enable signal **/CS3** from the processor and address lines **A17-A19**. It is routed to **U20** (SCN2681) [4,5,A]. **/DUART** is active for the address range \$E00000-\$E1FFFF.

**/PIOSL** [4,3,D] is the parallel I/O device enable line. It is generated by **U21** (GAL16V8) [4,4,D] by combining the system I/O enable signal **/CS3** from the processor and address lines **A17-A19**. This signal enables the I/O data buffer **U25** (74HCT245) [4,2,D] and bank selector **U23** [13,6,D]. **/PIOSL** is active for the address range \$E20000-\$E3FFFF.

**GR/W** [4,3,C] is the **R/W** line from the processor combined with the **PWRGOOD** signal. A write to a memory device can not be accomplished until **PWRGOOD** is asserted high.

**/FPSEL** [10,5,D] is the User Interface buffer **U38** (74HCT245) [10,5,C] enable line. This signal is generated by **U22** (GAL16V8) [10,5,D] by combining the system I/O enable signal **/CS3** from the processor and address lines **A17-A19**.

**/KEYSEL** [10,5,D] is the keyboard input buffer enable line that is routed to the User Interface module connector **J3** [10,5,A]. This signal is generated by **U22** (GAL16V8) [10,5,D] by combining the system I/O enable signal **/CS3** from the processor and address lines **A17-A19**. **/KEYSEL** is active for the address range \$EC0000-\$EDFFFF.

**/LCDSEL** [10,5,D] is the LCD module select line. This signal is generated by **U22** (GAL16V8) [10,5,D] by combining the system I/O enable signal **/CS3** from the processor and address lines **A17-A19**. **/LCDSEL** is routed to the User Interface module connector **J3** [10,5,A]. **/LCDSEL** is active for the address range \$E80000-\$E9FFFF.

**LCDEN** is the LCD module enable line. This signal is generated by **U22** (GAL16V8) [10,5,D] by stretching **/LCDSEL** by one system clock period and then ANDing this signal with **/LDS**. **LCDEN** is routed to the User Interface module connector **J3** [10,5,A].



### External Interrupt Sources

An interrupt signal causes the processor to stop normal program execution and go to an address that is the beginning of an interrupt service routine. Executing the routine provides whatever action is necessary to service the device generating the interrupt.

**/IRQ41** [2,5,B] is a signal which requests service by the real-time clock interrupt routine. This AC line referenced, 120Hz square wave signal is generated by **U1B** (14538) [8,5,A] in conjunction with optoisolator **U91** [20,2,C]. This routine controls timing of all controller software activity and provides real-time clock updates.

**/IRQ6** [2,3,A] is an active LOW open drain signal generated by **U20** (SCN2681) [4,5,B] during telemetry transmissions.

**/IRQ4F** [2,5,B] interrupt is used to shut down the controller in the event of a power failure. **/IRQ4F** is one of the highest priority interrupts thus causing the processor to take immediate action for an orderly controller shut-down. **/IRQ4F** is generated by the missing pulse detector circuit **U1A** (14538) [8,4,A]. The missing pulse detector is used to detect a loss of 120 Hz pulses. It is a re-triggerable one shot with a period of approximately 22 milliseconds. Positive transitions of **OPTO1**, from **U91** [20,2,C], are cleaned up by **U1B** then fed to **U1A**. This signal re-triggers the one shot every 8.33 milliseconds and also produces the **/IRQ41** signal. During a power failure the one shot will not be retriggered and will time out, causing an **/IRQ4F** interrupt. Also, if the power supply output voltage is out of tolerance, **VM24** will go LOW, thus forcing an **/IRQ4F** interrupt.

### Internal Interrupt Sources

The 68302 processor contains 16 on-board sources which can generate interrupts. The ASC/2 controller family uses the following interrupts: SCC1-SCC3 and Timers 1-2. The receive channel of SCC1 which is used for the telemetry channel, is set up to generate an interrupt when: 1. The controllers' address is recognized on the telemetry line, 2. After the block of data has been received and 3. When the checksum has been received.

The receive channel of SCC2 which is used for the terminal interface, generates an interrupt when: 1. An XON or XOFF character is recognized while the port is used for printing, 2. Blocks of data of various predefined lengths are received from another device during the direct connect process.

The receive channel of SCC3 which is used for the SDLC interface, generates an interrupt after a complete frame is received from a BIU or MMU.

Timer 1 is used for the telemetry channel and generates an interrupt when: 1. It is time to turn on the carrier signal, 2. It is time to transmit the data packet and 3. It is time to turn off the carrier.

Timer 2 is used for the SDLC channel and generates interrupts that set the proper timing of the transmission of SDLC frames to the BIUs and MMU.

Memory

Flash EPROM Program Memory

The software program that controls processor operation is written into **U2** (29F800AB-90) [5,4,D]. This is a 90-nanosecond rewritable flash EPROM that provides 1 Megabyte of program address space configured as 512K x 16 words. The EPROM is accessed using zero wait states. The number of wait states are set using the processors internal wait state generator associated with the master EPROM chip select signal **/CS0**. **U2** is enabled by chip enable line **/CS0L**. **U2** puts its data on the data bus (**D0-D15**) when the chip enable line is low and either or both output enable lines **/OEE** or **/OEO** [5,6,C] are low. A write operation to **U2** requires that **/CS0L** is low and **/WEO** is low.

RAM

All variable data is stored in Random Access Memory (RAM) pair **U6** and **U7** (628128-) [5,3,D]. The standard ASC/2S configuration uses 128K x 8, 70 nanosecond devices. This provides 256K bytes of data memory. The RAM is accessed using zero wait states. This is set using the processors internal wait state generator associated with the master RAM chip select signal **/CS1**. RAM is powered by voltage **BAT** [5,4,B] so that data is not lost during power outages. The RAM read/write operations function as follows:

When the RAM chip select signal **/CS1L** and the odd write enable signal **/WEO** are LOW, and the odd output enable signal **/OEO** is HIGH, the RAM stores the data on the odd data bus (**D0-D7**) in the location specified by the address bus (**A1-A15**).

When the RAM chip select signal **/CS1L** and the even write enable signal **/WEE** are LOW, and the even output enable signal **/OEE** is HIGH, the RAM stores the data on the even data bus (**D8-D15**) in the location specified by the address bus (**A1-A15**).

When the RAM chip select signal **/CS1L** is low and the odd write enable signal **/WEO** are high, and the odd output enable signal **/OEO** is low, the RAM supplies the odd data bus (**D0-D7**) with the data stored in the location specified by the address bus (**A1-A15**).

When the RAM chip select signal **/CS1L** is low and the even write enable signal **/WEE** are high, and the even output enable signal **/OEE** is low, the RAM supplies the even data bus (**D8-D15**) with the data stored in the location specified by the address bus (**A1-A15**).

When the processor does a word read or write access, both odd and even chips within the bank are enabled simultaneously

Data Module

The Data module is mounted on the Processor-I/O module. The module is connected by **J5** [6,5,C].

**\*\*CAUTION\*\***

Do not remove or insert  
data module with power  
applied to controller.

### EEPROM Memory

All user entered data is stored on the data module. The ASC/2S comes standard with a 32K x 8, 250 nanosecond Electrically Erasable Programmable Read Only Memory (EEPROM) installed on its data module. During a write cycle, the address and data are latched internally and the cycle is automatically completed by the EEPROM. The write cycle takes a maximum of 10 milliseconds during which the chip cannot be accessed. The EEPROM is accessed using three wait states. This is set using the processors internal wait state generator associated with the master EEPROM chip select signal **/CS2**.

The processor writes to EEPROM when the EEPROM chip enable signal **/CS2** is low, the odd output enable signal **/OEO** is HIGH, and the write enable signal **/CSWE** is LOW. When the EEPROM chip enable signal **/CS2** and the odd output enable signal **/OEO** are LOW, and the write enable signal **/CSWE** is HIGH, the EEPROM supplies the data bus (**D0-D7**) with the data stored in the location specified by address bus (**A1-A14**). The processor then reads the data from the data bus. EEPROM retains all user data when power is not applied to the controller.

### Memory Expansion Connector

Connector **J2** [9,2-6,A-D] allows for several functions including memory system expansion, Flash EPROM programming and system debugging. The Flash EPROM download module can be inserted into this connector for rapid programming of the on board Flash EPROM. All 68000 bus signals used by the ASC/2S are present on this connector.

### Voltage Monitor Control

The voltage monitor control circuit is used to force the Voltage Monitor output FALSE, thus setting the intersection to flash and turning on **LED1** [8,2,C]. The circuit consists of **U11C** and **U11D** (74LS09) [8,1,C]. These two gates AND the **VM24** and **/CPUVM** signals. **VM24** is an open collector output from comparator **U10A** (LM393) [3,4,B] that uses as its pull up voltage, the output of the watchdog timer **/DOG**. If **VM24**, **/CPUVM** or **/DOG** goes low, **VMC** will go low (FALSE). **VM24** is the output from the power supply voltage monitor circuit. This signal is set low if the +24VDC supply voltage goes out of tolerance. **/CPUVM** is an output from the processor chip. This line is set low when a flash condition is detected by the processor. **/DOG** is the output from the system watchdog timer circuit **U5** (14538) [8,4,B]. The watchdog input is toggled by the processor approximately once every 100 milliseconds. **/DOG** is set low if, due to erratic program behavior, the processor fails to toggle the watchdog input. Under normal conditions all three inputs are high thus maintaining Voltage Monitor Control **VMC** HIGH. A flash condition is indicated by a **VMC** LOW. The LOW **VMC** signal is inverted again at the I/O Interface and output as **Voltage Monitor**. This signal can be used in conjunction with a conflict monitor to set the intersection in flash.

Down Time Accumulator

The Down Time Accumulator (DTA) is used to detect missing 120 Hz interrupts and to time the length of power outages. The DTA consists of battery-backed real time clock chip **U3** (68HC68T) [8,4,D] and the processor chips' internal **Timer 3**.

**\*\*CAUTION\*\***

Do not attempt to adjust the crystal oscillator **C19** in the field. This is a precision adjustment. See maintenance section for proper adjustment procedure.

**Timer 3** is used to determine whether the length of a power failure is less than or greater than 0.75 seconds. This time was selected as the limit, within NEMA range, in determining the action to take after a short (< 0.75) or long (> 0.75) power failure. If the power failure is less than 0.75 seconds the controller continues to operate. If the power failure is greater than 0.75 seconds the controller reverts to its start-up sequence. If power fails altogether, the processor writes its internal RTC time out to **U3** to keep accurate time until power is reapplied. **U3** uses a combination of **VCC** and battery **B1** [8,5,C] voltage to operate. The processor communicates with **U3** over the **SPI** bus. When power is reapplied, the processor reads the time from **U3** and updates its internal RTC time.

Local Voltage Regulators

Switching regulator **U4** (LM2598-5.0) [3,5,B] converts the incoming +24VDC into the +5VDC **VCC** signal used throughout the module. **U4** also generates the **PWRGOOD** signal used by the reset circuit and **GR/W** generation. Diode **CR11** protects other circuits in the event of a short between U4-2 (+24VDC) and U4-3. Transient voltage suppressor **CR1** (P6KE27A) [3,6,B] protects the input from any transients greater than about +30VDC.

Linear regulator **U79** (LM7812) [7,3,D] provides a high current, short circuit protected +12VDC source for use by the telemetry module and external fiber optic modems.

### Back-Up Power Supply

The back-up power supply provides power to the RAM and the battery-backed clock during a power failure. With power applied, the **VCC** power supply provides power to the battery-backed real time clock **U3** (68HC68T) [8,5,D] and the RAM chips via transistor **Q1** (MMBT3904ALT1) [8,5,B]. As long as **VCC** is greater than 4.74VDC, **PWRGOOD** will be high and **Q1** will turn on.

When power is removed, **Q1** turns off and diode **CR3** conducts, thus supplying power from the lithium battery **B1** [8,5,C]. Jumper **JP2** disconnects the battery during troubling shooting or periods of extended storage. **B1** is a rechargeable lithium battery and uses resistors **R36**, **R38** and diode **CR13** as the charging circuit.

Battery voltage is monitored by comparator circuit **U10B** (LM393) [3,4,A]. When battery voltage drops below 2.2 VDC, the comparator triggers causing output signal **/LOBAT** to go low thus signaling the processor that the battery is not recharging properly and replacement is required.

### Display

The User Interface module contains a Liquid Crystal Display (LCD) formatted as 16 lines of 40 characters, the display contrast control, the display backlight circuit, the display heater circuit, the keyboard matrix and the system buzzer. The display contains its own control and drive electronics and appears as two registers to the processor. The display is connected to the processor module via User Interface connector **J3**. Please note: The User interface panel should be sent to Econolite for repair.

### Display Interface

The processor uses its Independent Direct Memory Access (**IDMA**) channel to write to the display. When a screen update is required, the program fills a RAM buffer with screen data. The program then initializes and activates the **IDMA** channel. The **IDMA** transfers one byte at a time from the buffer to transceiver **U38** (74HCT245) [10,5,C] via **D00-D07**. When **/FPSEL** [10,6,C] is low and **R/W** is low, the data is transferred to the User Interface module data bus and routed to the LCD module's data lines. The LCD module uses a combination of signals **LCDEN**, **/LCDSEL**, **A01** buffered by **U39A** (74HCT244) [106,B] and **R/W** buffered by **U39B** on its inputs to transfer the data to its internal circuitry. The **IDMA** uses the signal **TCLK1** [4,3,A] to generate its data request signal **/DREQ** [2,5,B]. Thus one byte is transferred for each cycle of **TCLK1**. The LCD module has a cycle time of 1 microsecond. The processor has a cycle time of 271 nanoseconds. The master I/O chip select signal **/CS3** is generated using 6 wait states and signal **LCDEN** is stretched by **U22** (GAL16V8) [10,5,D] to accommodate this discrepancy.

### Display LED Backlight

The LCD module contains a matrix of yellow/green LEDs used to backlight the display. The backlight is enabled from the front panel.

The processor uses its **PB2** output signal **LCD-B** [2,5,B] to activate the backlight. The processor turns the backlight ON by setting **PB2** HIGH. **LCD-B** is buffered before going to the User Interface module by **U39B** (74HCT244) [10,5,B].

Keyboard

The User Interface module keyboard consists of a matrix of conductive rubber switches. The processor scans the matrix via **J3** by reading specific addresses. The lower nibble of the address bus (**A01-A04**), which generates the row strobes, is buffered by **U39A** (74HCT244) [10,5,B]. The column data is input by buffer **U38** (74HCT245) [10,5,C]. Scan circuitry on the User Interface module is enabled by signal **/KEYSEL**. The processor then decodes the four column status bytes to determine which key is pressed.

Buzzer

The processor uses its **PB1** output signal **BUZ** [2,5,B] to activate the User Interface module buzzer. The processor turns the buzzer ON by setting **PB1** HIGH. **BUZ** is buffered before going to the User Interface module by **U39B** (74HCT244) [10,5,B].

## **Parallel I/O Interface**

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### **Parallel I/O Section**

The three members of the ASC/2S family use the same Processor-I/O module. The model type is differentiated by which components are installed in the parallel I/O section. The following discussion will address the board generically. Any circuits associated with a particular model type will be addressed separately.

All processor access to the parallel I/O section is done through buffers **U25** (74HCT245) [4,2,D] and **U24** (74HCT244) [4,2,C]. These chips buffer the **D00-D07** data lines, **A01-A06** address lines, **/LDS** and **/RESET**.

The I/O DECODER **U23** (74HCT138) [12,6,D] divides the I/O block defined by parallel I/O chip select signal **/PIOSL** into 8 sections, **/LE0**, **/LE1**, **//O0**, **I/O1**, **/Y4**, **/Y5**, **/Y6** and **/Y7**. These signals are generated by combining the block select signal **/PIOSL** with the buffered lower data strobe **/BLDS** and the addresses appearing on **BA4-BA6** and **BA17**. The following signals are generated:

**/LE0** is the latch enable for the bank of outputs containing the following phase 1-8 functions: PHASE ON, PHASE NEXT, PHASE CHECK, GREEN, YELLOW and RED DRIVERS, WALK DRIVER and PED CLEAR DRIVER. It is selected by address \$E20001.

**/LE1** is the latch enable for the bank of outputs containing the following functions: Phase 1-8 DON'T WALK DRIVERS, RING 1 AND 2 STATUS BIT DRIVERS and OVERLAP DRIVERS. **/LE1** is also routed to the expansion I/O connector **I/O2P1**. It is selected by address (\$E20011)

**//O0** selects the input multiplexer bank containing the following functions: Phase 1-8 HOLD, PHASE OMIT, PED OMIT, VEH CALL DET, PED CALL DET, RING 1 and 2 INH MAX TERM, MAX II SELECT, OMIT ALL RED CLEAR, RED REST MODE, PED RECYCLE, FORCE OFF and STOP TIME along with CALL TO NON-ACT, WALK REST MODIFIER, MIN RECALL, INTERVAL ADVANCE, MANUAL CONTROL ENABLE, INDICATOR LAMP CONTROL AND EXTERNAL START. It is selected by address \$E20021.

**//O1** selects the input multiplexer bank for the expanded I/O function of the ASC/2S-2100. It is selected by address \$E20031.

**/Y4** selects the input buffer containing the following functions: MODE BIT A-C, PREEMPT DET 2,4,5,6 and the COORD FREE INPUT. It is selected by address \$E20041.

**/Y5** selects the input buffer containing the following functions: TEST C, SPARES 1-6 and the signal that tells the controller that an expansion I/O module is present **ASCIO**. It is selected by address \$E20051.

**/Y6** and **/Y7** select the expanded I/O input buffers. They are selected by addresses \$E20061 and \$E20071, respectively.

Address Bus

This bus carries the address information used by the input multiplexers and output latches to select a particular I/O line. It is a buffered subset of the processors address bus and includes **BA1-BA3**.

Data Bus

This bus carries the data that is sent to the output latches or received from the input multiplexers. It contains the buffered lower (ODD) data bus which includes BD0-BD7.

Logic Level Translators

Each logic level translator consists of a three resistor network (10K, 75K, and 18K) which converts the 24 V (FALSE), 0 V (TRUE) logic levels of control signals from external equipment to the HCMOS logic levels required by the input multiplexers.

A 10K pull-up resistor biases the input to the FALSE state when the external control input is not connected. The voltage divider (75K and 18K) establishes the input level to the input multiplexer. An external input of 0 V to 8 V is detected as TRUE and an input of 16 V to 24 V is detected as FALSE (inputs are inverted internal to the processor). The combination of the 75K resistor, acting as a current limiter, and the internal protection circuit of the input multiplexer protects against transient input voltages exceeding 24 V.



### Input Multiplexers

Input multiplexers interface external control inputs (from connectors A, B, C and D) with the system data bus. The processor controls the multiplexer functions by enabling the multiplexer, addressing the inputs, and reading the input status. In this way, it controls the 16 HCMOS tri-state, 8-bit multiplexers **U51, U52, U53, U54, U55, U56, U58** and **U60** (74HC251) [14-15,1-6,A-D] on the ASC/2S-2000 plus **U40, U41, U42, U43, U47, U48, U49, U50** on the ASC/2S-2100. Each multiplexer receives eight external control inputs from a corresponding logic level translator. Each control input has a unique address associated with it. When the input is addressed and the multiplexer is enabled, the input status (ON/OFF) is routed to a single data bit at the multiplexer output pin (W) connected to the data bus.

The processor reads the input data by addressing it through the I/O Interface address bus **BA1-BA3**. The selected input is gated onto the I/O data bus by the LOW state of signal **I/O0** or **I/O1**. The processor simultaneously reads eight I/O data bits from 8 different multiplexors onto **BD0-BD7**.

Typical input operation is described below.

The signal from input pin **A1-/h** (PHASE 1 HOLD) [15,4,D] is applied, via logic level translator **RP22** [15,4,D] to input **DO** (pin 4), of input multiplexer **U58**. Coded address bits **BA1-BA3** from the address bus are applied to address select inputs **S0, S1**, and **S2** (pins 11, 10, and 9) of input multiplexer **U29**. When address lines **BA1-BA3** are all LOW, input **DO**, pin 4 of input multiplexer **U29** is selected. The LOW state of signal **I/O0** enables the multiplexer and causes the selected input to be inverted and output from **IY** (pin 6) as I/O module data bit **BD0**.

### Input Buffers

Input buffers **U19A** and **U59** (74HCT244) [12,6,B-C] transfer local and external data to the data bus. **U59** receives its inputs from logic level translator **RP23**. **U19A** inputs a combination of external and local status inputs. On an ASC/2S-2100, input buffer **U30B** (74HCT244) [12,3,B-C] and **U57** get their inputs from the 25-pin telemetry connector via logic level translators **RP36** and **RP35** respectively. The buffers output their data onto the data bus when the proper chip select line **IY4-IY8** goes low. Among other signals, **U19A** inputs the signal that tells the processor, when low, that the board is configured as an ASC/2S-2100.

### Overlap Program Inputs

On the ASC/2S-2100, a NEMA overlap program card is optionally available for programming overlaps A-D. This plug-in card is connected to optional connector **J6** [11,1,D]. Phase combinations of the four programmable overlap phases A, B, C and D are programmed by installing jumpers on the card. When the overlap card is installed, the jumpers ground the 10K pull-up resistors, **RP5-RP8** [17-18,3,B-D] at the (74HC251) multiplexer inputs. A ground at these inputs indicates that the associated phase is assigned to the overlap while an open circuit indicates that it is not. Program data for each overlap phase (A-D) is output by the multiplexers as eight bits representing the eight controller phases N1-N8. The overlap inputs are read by the processor at the multiplexer output pins as described above.

Output Latches

Output latches are used to interface data from the system data bus with external control output lines. The processor controls the data transfer by enabling the latches and addressing the output, thus latching the data from the data bus to be sent to external equipment. In this way, it controls twelve addressable 8-bit output latches, U31, U32, U33, U34, U35, U36, U37, U44, U45, U46, U61 and U62 (74HC259) [13-14,1-6,A-D] with associated output drivers, U67, U68, U69, U70, U71, U72, U73, U74, U75, U76, U77 and U78 (ULN2803A) on an ASC/2S-2000. In addition the ASC/2S-2100 also includes latches **U26-U29** [19,1-6, A-D] and associated output drivers **U63-U66**. All output drivers are biased to the 24 V (FALSE) state, when not asserted, through a 10K pull-up resistor.

Latches are addressed by bits A1-A3 and enabled by the /LE0 and /LE1 signals from the I/O device selector **U23** [12,6,D]. At the same time, data bits DB0-DB7 are input to the addressed latches.

Data is latched on the rising edges of the enable signals and remains latched until changed during a data update from the processor, which occurs every 100 ms. The buffered /RESET signal, /IORESET [4,2,B], clears all data from the latches at power on.

The Q outputs of each latch are applied to a high-current, high-voltage, Darlington transistor output driver (ULN2803A). Logic level transition to +24V (FALSE) and 0 V (TRUE) occurs at the driver outputs. Output lines are connected to interface connectors A, B C and D.

The ULN2803 output drivers are protected from transients on their output pins by Transient Voltage Suppressors **CR16** and **CR19** (P6KE33A) [13,3,C] [19,3,C]. These provide the output devices with a low impedance path to ground for voltages greater than 33VDC. This prevents damage to a driver by the reverse voltage generated when a relay coil connected to the output is de-energized or other transient occurs.

The FLASH LOGIC OUT output on A1-X [14,3,A] is derived from the **Q4** output of latch **U62** (74HC259) [14,6,B]. When this output is active, output driver **U78** (ULN2803A), sinks current from A1-X through diode **CR15**. When **U78** is off, **Q2** (MMBT2222ALT1) [14,4,A], is turned on and current is sourced to A1-X through the current sourcing circuit consisting of transistor **Q2** diodes **CR17-CR20** and current limit resistors **R57-R58**. This output can source 50mA maximum and can sink 200mA maximum. Diode **CR20** shunts any negative voltages on the output to ground. **CR17** shunts any voltage greater than 33VDC to ground.

On the ASC/2S-2100 the PREEMPT CMU INTERLOCK output associated with **U27** (pin 5) [19,5,B] is active only if there is a preemption requirement. The circuit consists of **Q3** (MMBT2222ALT) [19,3,C] **R62**, **CR16** and **CR21**. If a preemption sequence is not programmed, this output is forced LOW. This output can be connected to the conflict monitor 24 V monitor input to set the intersection to flash if a required preempt sequence is not programmed.

The voltage monitor **VMC** and fault monitor /**FLTMN** signals, generated by **U11** [8,1,C], detect out of tolerance voltage levels and processor failures and send control signals to the I/O section to be output as VOLTAGE MONITOR and FAULT MONITOR. The **VMC** signal is inverted and buffered by **U78** (ULN2803A) [14,5,B] and routed to **A1-C**. The /**FLTMN** signal is inverted and buffered by **U74A** (ULN2803A) [14,3,C] and routed to **J16-F**.

SDLC (EIA-485) Interface

The SDLC interface circuit sends and receives its signals on the SDLC bus. All TTL to EIA-485 signal level translation is provided by **U81** and **U82** (LT690) [7,6,C]. These contain one EIA-485 driver and one EIA-485 receiver each. After the signals are translated to EIA-485, they are routed to the outside world via connector **J15** (DA15S) [7,4,D]. The interface includes the following signals:

**TXD+** and **TXD-** are the differential transmit data pair. The processor transmits this serial data signal as **TXD3** from **SCC3** [2,5,C]. This signal is converted to a differential pair by **U81**. It is then output on connector **J15** pins 1 and 9.

**TXC+** and **TXC-** are the differential transmit clock pair. The processor transmits this serial data signal as **TCLK3** from **SCC3** [2,5,C]. The signal is converted to a differential pair by **U82**. It is then output on connector **J15** pins 3 and 11.

**RXD+** and **RXD-** are the differential receive data pair. These signals appear on pins 5 and 13 of connector **I/O2P5**. After conversion by **U81**, the single ended TTL signal is routed to **SCC3** on the processor as **RXD3** [2,5,C].

**RXC+** and **RXC-** are the differential receive clock pair. These signals appear on pins 7 and 15 of connector **I/O2P5**. After translation by **U82**, the single ended TTL signal is routed to **SCC3** on the processor as **RCLK3** [2,5,C].

Terminal (EIA-232) Interface

The terminal interface circuit sends and receives its signals on the terminal bus. All TTL to EIA-232 signal level translation is provided by **U80** (MAX214) [7,2,C] which contains three EIA-232 drivers and three EIA-232 receivers. **U80** uses capacitors **C66**, **C67**, **C71** and **C72** for its onboard positive and negative voltage generation circuits. **U80** also has an internal DCE/DTE switch that is controlled by **TERMCTRL1** [7,3,B]. Terminal signals are routed to the outside world via connector **J13** (DB25) [7,1,C]. The EIA-232 level signals are protected against over voltage transients by transient voltage suppressors (MMBZ15VDLT1) [7,1,B]. The interface contains the following signals:

**TXD** is the transmit data signal. The processor outputs this serial signal from **SCC2** as **TXD2** [2,5,C]. After translation, it appears on pin 2 of **J13**.

**RXD** is the receive data signal. This serial input signal appears on pin 3 of **J13**. It is translated and routed to **SCC2** of the processor as **RXD2** [2,5,C]. This signal is also routed to the DUART **U20** [4,5,B] as **RXDB**.

**CD** is the Data Carrier Detect handshaking signal. This input signal appears on pin 8 of **J13**. It is translated and routed to **SCC2** of the processor as **/CD2** [2,5,C].

**CTS** is the Clear To Send handshaking signal. This input signal appears on pin 5 of **J13**. It is translated and routed to **SCC2** of the processor as **/CTS2** [2,5,C].

**RTS** is the Request To Send handshaking signal. The processor outputs this serial signal from **SCC2** as **/RTS2** [2,5,C]. After translation, it appears on pin 4 of **J13**.

**DTR** is the Data Terminal Ready handshaking signal. DUART **U2** [4,5,A] outputs this serial signal from **OP2** as **/DTRT**. After translation, it appears on pin 20 of **J13**.

Signals **RTS**, **CTS**, **CD** and **DTR** are handled under program control and are implemented only as required. Communications with a printer utilize the XON / XOFF software handshake protocol.

#### Telemetry Interface

The Telemetry interface sends and receives its signals on the Telemetry bus. The signals are routed to the telemetry module connector **J4** [7,5,B], translated by the telemetry module and then routed to the outside world via connectors **J17** (DE9P) [7,3,B] and **J14** (DB25P) [7,4,A]. All TTL to FSK, EIA-232 or EIA-485 signal level translation is provided by the telemetry module attached to connector **J4**. The interface contains the following signals:

**TXD** is the transmit data signal. The DUART **U20** [4,5,B] outputs this serial signal to the telemetry module as **TXDA**. After translation, it is routed to **J17**, pins 1 and 2, and expansion I/O connector **J14** as signal pair **XMIT+** and **XMIT-**.

**RXD** is the receive data signal. This serial input signal appears on pins 4 and 5 of **J17** and expansion I/O connector **J14** as **RECV+** and **RECV-** then routed to **J4**. It is translated by the Telemetry module and routed to **SCC1** of the processor as **RXD1** [2,5,D].

**CD** is the Data Carrier Detect handshaking signal. This signal is generated by the FSK telemetry module and appears on pin 9 of **J4**. It is routed to the DUART as **/CDA** [4,5,B]. EIA-232 telemetry modules input this signal from **J17** pin 1.

**CTS** is the Clear To Send handshaking signal. This input signal, generated by the telemetry module, appears on pin 7 of **J4**. It is routed to the DUART as **/CTSA** [32806,5,3,A]. This signal also serves as the MODEM PRESENT signal used by the processor to determine if a Telemetry module is present. The Telemetry module will pull this signal low if present. EIA-232 telemetry module input this signal from **J17** pin 1.

**RTS** is the Request To Send handshaking signal. The DUART outputs this signal as **/RTSA** [4,5,B]. It is routed to pin 8 of **J4**. EIA-232 telemetry modules output this signal on **J17** pin 7.

**MDCTL1** and **MDCTL2** are used to control various functions on the Telemetry module. They are generated under program control by using two of the DUARTs parallel I/O lines [4,5,A]. **MDCTL2** is also routed to inverter/driver **U64** (ULN2803A) [19,5,B] It is used on **J14** as the **KEY** signal required by the radio interconnect.

**/IORESET** is used to reset the telemetry module circuitry. It is a buffered version of system **/RESET**.

Signals **RTS**, **CTS** and **CD** are handled under program control and are implemented only as required.

### **AC Power Input**

The AC line transient protection circuit consists of resistors **R65** and **R67**, and varistors **RV1**, **RV2** and **RV3**. The circuit receives a three-wire, 120 VAC, 60 Hz input from the A connector **J12** or **J16** on the ASC/2S-1000. The three inputs are AC line, AC neutral, and earth ground. AC line is over current protected by fuse **F2**. AC line and AC neutral are then routed to current-limiting resistors **R67** and **R65** respectively. Varistor **RV1**, **RV2**, and **RV3** provide both common and differential mode transient protection. This is accomplished by clamping transients occurring between AC line and AC neutral with varistor **RV2**. Transients occurring between AC line or AC neutral and earth ground are clamped by **RV1** and **RV3**, respectively. The output of the transient protection circuit is then applied to the power supply via connector **J19** [20,2,D]. Additional transient protection and noise filtering circuits are present on the power supply module.

#### Line Reference Circuits

Signal **OPTO1** is the 120 Hz line frequency reference used by the controller program as the input to the real time clock. It is generated by full wave rectifier **CR25** (VM88) [20,3,C] which rectifies the 120 VAC 60 Hz line voltage, to produce a 120 Hz signal which is presented to dual opto-isolator **U91** (MCT6). Zener diode **CR24** (1N4763A) prevents output of the **OPTO1** signal when the line voltage is below 82 VAC. The **OPTO1** signal is routed to **U1B** (14538) [8,6,A]

Signal **OPTO2** is the 60 Hz line frequency reference used by the controller program during dimming operations. It is generated by opto-isolator **U91** which only turns on during the positive half cycle of the waveform thus, producing a 60 Hz signal. The **OPTO2** signal is routed to an input on DUART **U20** (SCN2681) [4,5,A]

#### Processor-I/O DC input circuit

+24VDC enters the Processor-I/O module on connector **J18**. Diode **CR4** (MBRS340T3) [20,4,B] provides reverse polarity protection. **CR7**, **CR8** and **CR10** provide current steering for the proper charging and discharging of the hold-up capacitor **C76**. **R31** limits inrush current while charging **C76**. **+24VE** is the primary onboard +24VDC voltage source for I/O devices. **+24VI** supplies +24VDC to the +5VDC voltage regulator in the processor section. The **+24VEXT** external output is applied to connector pin A-B. This output is rated at 500 mA and provides sufficient current for most traffic applications. The 24 VDC has been fused with a 3/4 Amp SLO-BLO fuse, **F1**, to allow the controller to supply sufficient current for a controller test fixture using LED displays (20 mA per LED). This higher current capability should only be used during testing. Note that the 24 VDC load in the traffic control cabinet should never exceed 500 mA. Inductor L2 [20,4,A] filters out noise induced on the logic ground (**FGND**) when it is run outside the controller.

### **FSK Telemetry Module**

The MODEM provides Frequency Shift Keying (FSK) modulation of data from **TXDA** to make the data compatible for transmission over telephone lines or twisted pair cable. It also receives FSK signals and demodulates them to provide the **RXD1** signal.

All signals going to or from the telemetry module are routed through connector **J1** [2,6,A-D and others]. This connector interfaces with connector **J4** on the Processor-I/O module.

#### Transmit Data (TXDA)

The **TXDA** [3,6,B] line carries TTL level serial data from the DUART on the processor module [34251,4,5,B] to the analog multiplexer **U2** (74HC4051) [3,3,C] which is then routed to the FSK modulator. The data rate is 1200 bits per second.

#### Receive Data (RXD1)

The **RXD1** [4,1,D] line sends TTL level serial data, that originates at the FSK demodulator, from output buffer **U10** [4,5,D] to the SCC1 receive channel on the processor chip [34251,2,5,D]. The data rate is 1200 baud.

#### Data Carrier Detect (/CDA)

This signal originates at the FSK demodulator and is routed via **U10** [4,5,D] to the DUART. It indicates the status of the MODEM carrier signal. The line is HIGH if the carrier is lost, usually because of an abnormal condition. Under normal conditions the line is LOW, indicating that the carrier is present.

#### Modem Control 1 (**MDCTL1**)

This signal which originates on the DUART is used by the program to turn on the VALID DATA LED **DS2** [2,5,C].

#### Modem Control 2 (**MDCTL2**)

This signal which originates on the DUART is used by the program to turn on the transmit interface circuit. When **MDCTL2** is LOW the LEDs inside opto-isolators **U4** and **U5** (MCT6) turn on thus, turning on the transmitter output.

#### Modulator-Transmitter Circuit

**U7C** [3,4,A] in conjunction with **U2** [3,3,C] set the voltages used by **U3** [3,1,D], the FSK modulator. **U3** is a voltage to frequency converter. One of three voltages are generated by **U2** to select 1200 Hz (Mark), 2200Hz (Space) or 900Hz (Soft Carrier Turn Off) generation by **U3**. During standard four-wire operation, the **TXDA** signal selects between Mark and Space generation. When Soft Carrier Turn Off operation is selected during two wire operation, it operates as follows: **/RTSA** [3,6,A] goes low at the start of a message. During this time, the pull up resistor **R14** [3,4,A], at the output of **U7C** has no pull up voltage thus, the output of **U7C** is low. Because of this, the level of the **TXDA** line is used by **U2** to select between Mark and Space voltages. At the end of the message, **/RTSA** goes high turning on the soft carrier voltage. During this time, **C20** charges through **R26** (an 8mS time constant). After 8mS, the threshold voltage of the comparator is exceeded and its output goes low thus, turning off the softcarrier voltage. **R24** [3,2,C] sets the 1200Hz voltage, **R23** [3,2,B] sets the 2200 Hz voltage and **R6** sets the 900Hz SCTO voltage. When the input voltage to **U3** pin 8 changes, the frequency output by **U3** pin 2 varies. **R25** [3,2,D] is the transmitter output level adjust.

Opto couplers **U4A** and **U4B** gate the analog signal from the FSK modulator according to the level on **MDCTL2**. **U6** acts as a temperature compensated output buffer with gain. Opto couplers **U5A** and **U5B** allow the output stage to be permanently enabled with a 600 ohm load or gated by **MDCTL2**. **U7**, **Q1**, **DS3** and associated components are the output level comparator circuit that is used for measurement of the output level and transmit level indication. When **U5** is ON, the FSK output signal is coupled through transformer **T1** (T2104) [4,5,A] to transmitter terminations **XMIT+** and **XMIT-**. Transformer **T1**, **R28**, **R29** **RV2** **CR3** and **CR4** provide a balanced, isolated, transient protected output.

Receive Filter And Demodulator Circuit

Transformer **T2**, **R1**, **R3**, **RV1**, **CR1** and **CR2** [2,5,B] provide a balanced, isolated input with transient protection. **C24** and **R43** are the initial high pass filter. This filter provides -6dB/octave attenuation of frequencies below 480Hz. **U9A** (LM324) [2,4,C] is the input preamplifier with adjustable gain. **U9B-U9D** are the band pass filter that remove out-of-band high and low frequency noise signals. Jumper **JP3** [2,5,C] allows routing of the signal from the secondary of the output transformer to the input circuit (in two wire mode, the output transformer **T1** is also the input transformer.). **JP7** [2,1,B] provides a way to bypass the input filter. The output from **JP7** is then sent to the FSK demodulator as **RC** [3,6,D]. **U8** (XR-2211) [3,5,D] is the FSK demodulator. It outputs the received data **RD** signal, carrier detect **/CD** and drives the carrier detect LED **DS4** via **Q2** [2,6,C]. **R22** [2,4,D] sets the receiver center frequency (1700Hz).





## **SECTION 3 MAINTENANCE**

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Several procedures, guides and lists are provided for general maintenance of the ASC/2S family. This section contains unpacking and installation procedures, useful for the first ASC/2S installation and for later reference. A disassembly procedure instructs on removing each module and major components. Basic procedures include printed circuit board cleaning, voltage checking and down time accumulator crystal adjustment. A list of test equipment recommended for maintenance is also included. The circuit components used in the ASC/2S require care in handling, installing, storing, and operating both unmounted and mounted on printed circuit boards. Modules and their components should only be handled at a static-free workstation. Personnel and equipment **MUST** be properly grounded. Please refer to the Motorola CMOS LOGIC data book or any other MOS manufacturer's procedures for more information.

## MAINTENANCE

### UNPACKING AND INSTALLATION

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#### UNPACKING

The ASC/2S controller is packed in a specially designed protective shipping carton. All necessary precautions have been taken to ensure that the equipment is received intact and in proper working order. However, the following steps should be taken when unpacking the controller to verify that there is no shipping damage.

1. Carefully inspect the shipping container for damage before opening. If the container is damaged, unpack the controller in the presence of the carrier.
2. Do not discard the packing materials (foam endcaps and box) as they have been specially made for the ASC/2S and must be used should it be necessary to ship the controller again.
3. Once unpacked, carefully inspect the controller for damage. Check for broken wires, connectors, loose components, bent panels, and dents or scratches on the enclosure.
4. If any physical damage is discovered, notify the carrier immediately.

#### INSTALLATION PROCEDURE

The ASC/2S should be installed in a location where the front panel is easily accessible. Adequate room should be left around the controller to allow easy removal if necessary. Care should be taken to install the controller so that vents on the back side are not blocked. **Before applying AC power**, perform the following pre-installation checks:

1. Open the front panel door, remove the plug-in data module and verify that the number on the EEPROM label matches the program number on the controller label located on the top surface of the unit. Reseat the data module.
2. Verify that all modules are properly secured and that all connector ribbon cables are in place.

Once these preliminary steps have been taken the controller is ready for operation. Required cable connector part numbers are listed below. Refer to Appendix B for the connector pin lists.

**MAINTENANCE  
CONNECTOR CABLE ASSIGNMENT**

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**CONNECTOR CABLE ASSIGNMENT**

<u>CONNECTOR</u>	<u>CABLE</u>	<u>CONNECTOR</u>	<u>ECONOLITE PART NUMBER</u>
A		MS-3116-22-55S	44143P1
B		MS-3116-22-55P	44143P2
C		MS-3116-24-61P	44143P3
D		AMP #205842-1	31163P2
	CRIMP SOCKET		31163P4
	SDLC (PORT1)	DAU-15P	54665P4
	TERMINAL (PORT2)	CANNON #DBC25P	54665P7
	TELEMETRY (PORT3)	DEU-9S	54647P9
	TELEMETRY (EXPIO)	CANNON #DBC25S	54647P6

# MAINTENANCE ENVIRONMENTAL REQUIREMENTS AND STORAGE

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## ENVIRONMENTAL REQUIREMENTS

The ASC/2S meets or exceeds the NEMA environmental standards for traffic control equipment summarized below:

### ENVIRONMENTAL OPERATION SPECIFICATIONS (NEMA TS 2 SECTION 2)

CATEGORY	REQUIREMENT
Input Power	Line Voltage: 89 to 135 VAC
Power Consumption	ASC/2S-1000 20 Watts ASC/2S-2100 25 Watts
Ambient Temperature	Operating Range: -34EC to +74EC Storage Range: -45EC to +85EC
Humidity	Relative humidity is not to exceed 95% over the temperature range of +4.4EC to +43.4EC
Vibration	The major units of the controller assembly maintain their programmed functions and physical integrity when subjected to a vibration of up to 0.5g at 5 to 30 cycles per second, applied in each of the three mutually perpendicular planes.
Shock	The major units of the controller assembly do not suffer either permanent mechanical deformation or any damage that renders the unit inoperable, when subjected to a shock of 10G applied in each of the three mutually perpendicular planes.

## MAINTENANCE TEST EQUIPMENT

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### TEST EQUIPMENT

The following is a list of suggested test equipment to be used for fault isolation, basic check-out, and general maintenance.

1. 100Mhz, digital, dual-trace oscilloscope. Used for observing signals and checking of time relationships of two waveforms where necessary.
2. Digital Multimeter (DMM). Used for continuity testing, diode and transistor checks, and general voltage measurements.

The DMM should meet the following specifications:

<u>PARAMETER</u>	<u>RANGE</u>	<u>ACCURACY</u>	<u>INPUT IMPEDANCE</u>
DC VOLTS	200mV-1000V	" 0.25% of Input	10 MS
AC VOLTS	200mV-750V		10 MS, Capacitance < 100 pF
RESISTANCE (OHMS)	200S-20MS	-	-

3. Frequency counter. Used for Down Time Accumulator crystal adjustment. Note that the DTA crystal adjustment is a high precision adjustment, therefore an accurate frequency counter is required.

**DISASSEMBLY**

When disassembling the controller always disconnect input power before attempting to disassemble any part of the controller. Below is a disassembly description for each module.

<p><b>** CAUTION **</b> Disconnect Input Power before attempting to disassemble the controller</p>
--

**Processor Module**

The Processor-I/O module is attached to the enclosure by two 1/4 turn fasteners. To remove the module:

1. Disconnect the interface cable to the front panel.
2. Turn the fasteners 1/4 turn to the left.
3. Hold onto the assembly by the connector plate and pull the module out from the bottom until it slides out of the card guide on the inside top of the enclosure.
4. Pull the module out far enough to disconnect the two power supply harnesses attached to the rear of the module.

**Power Supply**

The power supply is mounted on the inside rear panel of the enclosure on standoffs. The supply is held in place by four screws and washers. To remove the Power Supply module:

1. Remove the Processor-I/O module.
2. Remove the two wire harnesses from the power supply module.
3. Remove the four screws and washers.
4. Remove the supply from the enclosure.

## **CLEANING AND INSPECTION**

General controller maintenance includes regular cleaning and inspection of the controller printed circuit boards (PCB's), electronic components, connectors, cables, and plastic and metal parts of the enclosure.

Use the following cleaning and inspection procedure to prolong equipment life and to minimize the risk of failure.

### **Cleaning**

1. The power source must be disconnected before attempting to clean any of the controller components.
2. When boards are repaired, clean flux residue from solder connections with or an environmentally safe flux remover. Free air dry.
3. Clean keys and front panels with a soft, lint free, damp cloth. Free air dry. Do not allow excessive amounts of water to collect around or enter keyboard and display areas.

**\*\* CAUTION \*\***

Do not apply any cleaning solvents to keyboards, front panel, display, or any other plastic parts.

4. Clean PCBs with a non-abrasive, moisture and residue free aerosol duster.

## MAINTENANCE CLEANING AND INSPECTION

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### Inspection

The following inspection guide is provided as a quick reference when inspecting the controller and its components.

Table 3-1. Visual Inspection Guide

Item	Defect
Capacitors, general	Burned spots, damaged leads.
Capacitors, ceramic or tantalum	Broken or cracked bodies.
Capacitors, electrolytic	Ruptured bodies, leaking electrolyte.
Connectors	Broken, loose, bent, corroded, or missing pins; cracked insulation; incorrect polarization.
Equipment, general	Dented or bent. Dust, dirt, lint, grease, oil; excess resin, spattered solder, metal chips, filings, or other foreign matter in equipment. Worn spots or deep scratches on surfaces, marred protective finish exposing bare metal, evidence of arcing, loosening screw thread assemblies.
Hardware	Incorrect screw length. Missing screws, nuts, bolts, rivets, lockwashers, and nutplates; screws, nuts, or bolts with stripped threads.
Integrated circuits	Broken or cracked bodies, corrosion, shorted contacts.
Markings, decals, and reference designators	Missing, incorrect, illegible, or obliterated.
Printed circuit boards	Broken, cracked, or burned parts; broken or missing rivets; broken circuitry; chipped contacts; copper showing on contacts; copper showing on circuitry; cracks, holes, or burns in cards; defective soldering joints; cracks; flat surfaces; bubbles or holes; lifted pads; broken or missing eyelets.
Resistors	Discolored body, loose connections.
Solder connections	No solder, insufficient solder, excess solder, cold or crystallized joints.
Transformers	Melted insulation compound, frayed insulation
Terminal strips and boards	Cracked, burned, or damaged terminal pins
Wiring	Cut, burned, or abraded insulation exposing bare conductor, abrupt V bends which weaken conductor; points of abrasion not insulated; pinched or damaged wires; broken or loose lacing; loose clamps.



### Lithium Battery

The lithium-cell battery, mounted in the upper left side of the Processor-I/O module, supplies power to the CMOS RAM and the Battery Backed Clock during a power failure. This battery is rechargeable and should not require replacement during the life of the controller. However, if a battery requires replacement, please observe the following precautions:

### IMPORTANT SAFETY INFORMATION

Lithium cells or batteries are very high energy power sources and therefore must be handled with care. **Please observe the following precautions.**

**Do not short battery terminals.** Cells and batteries contain high energy. If they are short circuited or heat up, immediately disconnect from load using JP2 [8,5,C].

**Do not open, puncture, or crush batteries.** Cells and batteries contain sulphur dioxide and flammable material.

**Dispose of properly. Do not incinerate.** Cells and batteries can be disposed of in sanitary land fills. Discharged lithium cells and batteries may contain significant amounts of unused energy and should be handled carefully. They should be packed for disposal and electrically isolated. **Do not compact for disposal.**

**ADJUSTMENTS AND TESTS**

**MODEM Check Out Procedure**

Required Test Equipment:  
Test Loopback Cable 33279G6  
Oscilloscope

1. Install jumpers as follows:

A. JP1	4W
B. JP2	4W
C. JP3	4W
D. JP6	4W
E. JP4	2W/O
F. JP5	ESC
G. JP7	FE
H. JP8	INSTALLED
I. JP9	OPEN
2. Turn off controller power. Install module in controller. Reapply power.
3. Attach 600 ohm load loop back cable (33279G6) to telemetry connector.
4. Set oscilloscope to 5 Volts/Division and .1mSec/Division.
5. Adjust R22 to produce a 1,700 ( $\pm 15$ ) Hz square wave on JP9 pin 2. This corresponds to approximately 5.8 horizontal divisions on the oscilloscope screen (.58mS).
6. Remove jumper on JP8 and install it on JP9.
7. Attach scope or frequency counter probe across R28 and R29.
8. Go to the controllers telemetry diagnostic display (Main Menu, 9, 6). Select #1, Mark.
9. Turn R25 all the way counter clockwise (35 turns max.). Then, turn R25 clockwise until DS3 (TD/TLEV) just turns fully on.
10. Set oscilloscope to 5 Volts/Division and .2mSec/Division.
11. Adjust R24 to produce a 1200 ( $\pm 15$ ) Hz sine wave. This corresponds to approximately 4.2 horizontal divisions on the oscilloscope screen (.83mS).
12. Go to the controllers telemetry diagnostic display (Main Menu, 9, 6). Select #2, Space.
13. Set oscilloscope 5 Volts/Division and .1mSec/Division.
14. Adjust R23 to produce a 2200 ( $\pm 15$ ) Hz sine wave. This corresponds to approximately 4.5 horizontal divisions on the oscilloscope screen (.454mS).
15. Verify that the output is 2.2 (+.6 -.2) volts peak-to-peak when DS3 is on. Adjust R25 as necessary.
16. Turn R20 all the way counter-clockwise (35 turns max.). Then turn R20 8 turns clockwise. (This sets receiver gain to unity. For field adjustment, turn R20 clockwise to increase the receiver gain.)
17. Verify that DS4 (CD) and DS1 (RDATA) turn on when mark or space are selected on the controller menu.
18. Go to the controllers telemetry diagnostic display (Main Menu, 9, 6). Select #3, Modem.
19. Verify that DS2 (VDATA) blinks briefly at start of test. Verify that "Telemetry Data Test Passed" message is displayed at end of test.

**Modem Check**

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1. Install module in test controller. Attach telemetry Master cable to Port 3.
2. Set proper telemetry channel.
3. If controller is attached to an ASC/2M, set telemetry response delay on controller to 8800. (Set ASC/2M "TELEMETRY WINDOW to 80.) If controller is attached to a KMC 10,000, set telemetry response delay to 10,000.
4. Verify that controller communicates with master.
5. Set jumper JP5 to the DSC position.
6. Verify that controller communicates with master.

Page 1 of 2

7. Verify that jumpers are set according to the following table before shipment:

- A. JP1 = 4W
- B. JP2 = 4W
- C. JP3 = 4W
- D. JP4 = 2W/O
- E. JP5 = DSC
- F. JP6 = 4W
- G. JP7 = FE
- H. JP8 = NOT INSTALLED
- I. JP9 = INSTALLED

27. Remove test equipment.
28. If the controller is to be stored, set the battery jumper to the OFF position.

**Crystal Adjustment Procedure**

Replacement of any Battery Backed Clock oscillator circuit components (**U3, R12, C5, C12, Y1**) [8,4,D] requires a crystal adjustment. Before the controller is put back in service, the following adjustment procedure should be completed.

**\*\* CAUTION \*\***

Setting the Battery Backed Clock oscillator requires careful adjustment. This **MUST** be done in the lab **NOT** in the field

Required Test Equipment:

Frequency counter, oscilloscope

1. Verify that the battery jumper is in the ON (top) position.
2. Allow controller and test equipment to warm up for approximately 10 minutes. This is an important step in achieving an accurate adjustment.
3. Connect the oscilloscope/frequency counter to the top terminal of **Y1**.
4. Monitor the oscilloscope and set waveform for maximum amplitude by adjusting capacitor **C5**. Adjust the clock using a non-metallic adjustment tool.
5. Verify frequency is set to 32.768 kHz  $\pm$  2 Hz and remove test equipment.

**Diagnostics Menu - Inputs**

**Diagnostics Menu**

Several diagnostic functions are included in the standard release controller software. These functions are accessed by selecting the DIAGNOSTICS (9) menu item from the MAIN MENU. The DIAGNOSTICS menu includes functions for testing INPUTS (1), OUTPUTS (2), DISPLAY (3), KEYBOARD (4), OVERLAP PROGRAM (5), TELEMETRY (6) and LOOPBACK (7). Following is a description of each test function and how to perform the test.

ASC/2 MAIN MENU	
1. CONFIGURATION	6. DETECTORS
2. CONTROLLER	7. STATUS DISPLAY
3. COORDINATOR	8. UTILITIES
4. PREEMPTOR	9. DIAGNOSTICS
5. NIC/TOD	
PRESS KEYS 1..9 TO SELECT	

DIAGNOSTICS SUBMENU	
1. INPUTS	5. OVERLAP PROGRAM
2. OUTPUTS	6. TELEMETRY
3. DISPLAY	7. LOOPBACK
4. KEYBOARD	
PRESS KEYS 1..7 TO SELECT	

**Inputs (1)**

This test displays the state of each input from connectors A, B and C when the controller is connected to a suitcase tester. Perform the following steps:

1. Attach controller to a suitcase tester.
2. Select INPUTS (1) from the DIAGNOSTICS SUBMENU. When this is selected, the controller beeps and displays a message saying that it will go into flash when this test is started.
3. When the INPUT DIAGNOSTIC screen is displayed, push VEH DETECTOR #1 input on the suitcase tester. An X will be displayed on the screen in the VEH DETECTOR #1 position. Activate the other switches on the suitcase tester to verify proper operation of all inputs.
4. Press the NEXT PAGE (F6) key to view and activate inputs on the remaining screens. Push SUB MENU (F3) to exit this test.

If this test uncovers an input failure, use the detailed description of the I/O section of the Processor-I/O and the schematic included in the document to pinpoint the problem.

# MAINTENANCE ADJUSTMENTS AND TEST

## Diagnostics Menu - Inputs

```

*****
*                                     *
*               WARNING               *
*                                     *
* THIS DIAGNOSTIC RESULTS IN         *
* INTERSECTION FLASH! PRESS ENTER TO *
* PROCEED OR SUBMENU TO EXIT.        *
*                                     *
*****

```

```

INPUT DIAGNOSTIC CONNECTORS A, B & C

PHASE          1 2 3 4 5 6 7 8

VEH DETECTOR..

PED DETECTOR

HOLD

PHASE OMIT.

PED OMIT

```

```

INPUT DIAGNOSTIC CONNECTORS A, B & C

RING 1          RING 2

MAX RED STP FRC    MAX RED STP FRC
INH RST TIM OFF   INH RST TIM OFF

PED MAX OMT       PED MAX OMT
REC 2 AR          REC 2 AR

```

```

INPUT DIAGNOSTIC CONNECTORS A, B & C

MIN WRST CNA CNA TEST TEST TEST
REC MOD  1  2  A  B  C

INT NCON LAMP EXT      I/O MODE
ADV EN  OFF  STRT     A  B  C

PMT PMT PMT PMT CORD
 2  4  5  6  FREE

```

```

INPUT DIAGNOSTIC CONNECTOR D

CYC  CYC  CYC  CORD  OFT  OFT  OFT  REM
 1   2   3   FREE  1   2   3   FLSH
 X   X                   X   X

SPLT SPLT DUAL SPLT PMT PMT TIME
 1   2   CORD DMD  1   2   RESET

PMT PMT PMT PMT
 3   4   5   6

```

```

INPUT DIAGNOSTIC TELEMETRY CONNECTOR

LOC  MAIN ALRM ALRM CMU  EXT  TLM  TLM
FLSH REQD  1  2  FLSH ADDR SP1 SP2

SYSTEM DETECTORS

1   2   3   4   5   6   7   8

```

**Diagnostics Menu - Outputs**

Outputs (2)

This test allows for manual activation of each output to connectors A, B and C when the controller is connected to a suitcase tester. Perform the following steps:

1. Attach controller to a suitcase tester.
2. Select OUTPUTS (2) from the DIAGNOSTICS SUBMENU. When this is selected, the controller beeps and displays a message saying that it will go into flash when this test is started.
3. When the OUTPUT DIAGNOSTIC screen is displayed, the cursor will be in the PHASE #1 RED position. Push the TOGGLE (0) key several times. Notice that the PHASE #1 RED LED on the suitcase tester is turned on and off. Use the cursor keys to position the cursor over the other output locations. Verify proper operation of all the outputs.
4. Press the NEXT PAGE (F6) key to view and activate outputs on the remaining screens. Push SUB MENU (F3) to exit this test.

If this test uncovers an output failure, use the detailed description of the I/O section of the Processor-I/O and the schematic included in the document to pinpoint the problem.

OUTPUT DIAGNOSTIC CONNECTORS A, B & C

PHASE	1	2	3	4	5	6	7	8
RED								
YELLOW								
GREEN								
WALK								
DON'T WALK								
PED CLEAR								
CHECK								
PHASE ON								
PHASE NEXT								

PRESS TOGGLE TO CHANGE

OUTPUT DIAGNOSTIC CONNECTOR D

CYC	CYC	CYC	SYNC	OFT	OFT	OFT	XSTR
1	2	3	OUT	1	2	3	SYNC
SPLT	SPLT	NIC	NIC	PMT	PMT	CMU	CORD
1	2	SF1	SF2	1	2	INLK	STAT

PRESS TOGGLE TO CHANGE

OUTPUT DIAGNOSTIC CONNECTORS A, B & C

	RING 1 STATUS	RING 2 STATUS				
	A	B	C	A	B	C
OVERLAP	A	B	C	D		
RED						
YELLOW						
GREEN						
FLASHING LOGIC						

PRESS TOGGLE TO CHANGE

OUTPUT DIAGNOSTIC CONNECTOR D

PMT	PMT	PMT	PMT				
3	4	5	6				
			SPARE OUTPUTS				
1	2	3	4	5	6	7	8
OUTPUT DIAGNOSTIC TELEMETRY CONNECTOR							
TLM	TLM	TLM	TLM				
SF1	SF2	SF3	SF4				

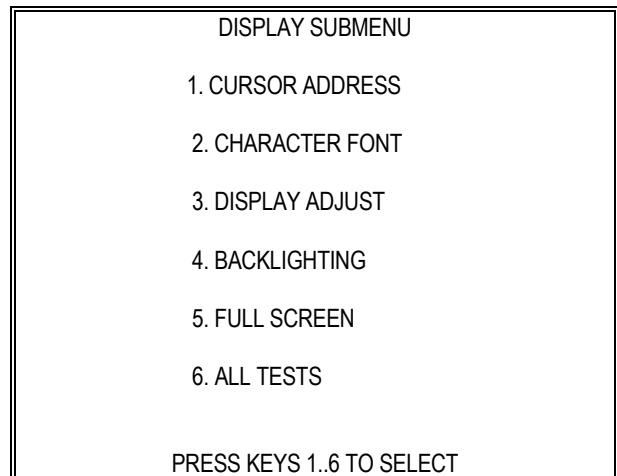
PRESS TOGGLE TO CHANGE

Display (3)

This menu provides a comprehensive set of functions for testing all aspects of the LCD module. Perform the following steps:

1. Select DISPLAY (3) from the DIAGNOSTICS SUBMENU. When this is selected, the controller beeps and displays a message saying that it will go into flash when this test is started.
2. When the DISPLAY SUBMENU is displayed, select CURSOR ADDRESS (1). This will perform a test which causes the cursor to address every character location on the display. Verify all positions are addressed. Push SUB MENU (F3) to exit this test.
3. Select CHARACTER FONT (2). This test will display complete ASCII character set supported by the module. Verify all characters are properly formed. Push SUB MENU (F3) to exit this test.
4. DISPLAY ADJUST (3). The display adjust test does not work on the ASC/2S controller.
5. Select BACKLIGHTING (4). This test will continuously turn the display backlight on and the off. Verify this operation. Push SUB MENU (F3) to exit this test.
6. Select FULL SCREEN (5). This test fills the display with dark characters. This should give the appearance of forty black columns each separated by a one white pixel. Verify this operation. Push SUB MENU (F3) to exit this test. If this test produces a screen with missing pixels, LCD module replacement may be required.
7. ALL TESTS (6) automatically performs tests 1-5 above. Push SUB MENU (F3) to exit this test.

Please note: There are no user serviceable parts on the User Interface module. If it has been determined that a display problem is caused by the module, please return it to Econolite.





Diagnostics Menu - Keyboard/Overlap

Keyboard (4)

This function tests all front panel keys. Perform the following steps:

Select KEYBOARD (4) from the DIAGNOSTICS SUBMENU. When this is selected, the controller beeps and displays a message saying that it will go into flash when this test is started.

1. When the KEYBOARD DIAGNOSTICS screen is first displayed, the user is prompted to push the "0" key. Push this key and verify that the number "0" is displayed in the proper position on the keyboard diagram shown on the LCD. The user is then prompted to push the next key. Continue for all twenty five keys. If a key is not pressed within twenty seconds or a key is pressed out of sequence, the test will fail. Push SUB MENU (F3) to exit this test

Please note: There are no user serviceable parts on the User Interface module. If it has been determined that a display problem is caused by the module, please return it to Econolite.

Overlap (5)

This test is used to verify proper reading of the optional overlap card which can be installed on the optional Expansion I/O module. Perform the following steps.

1. Select OVERLAP (5) from the DIAGNOSTICS SUBMENU.
2. Verify that the displayed X's correspond to the jumpers inserted on the overlap card. Push SUB MENU (F3) to exit this test.

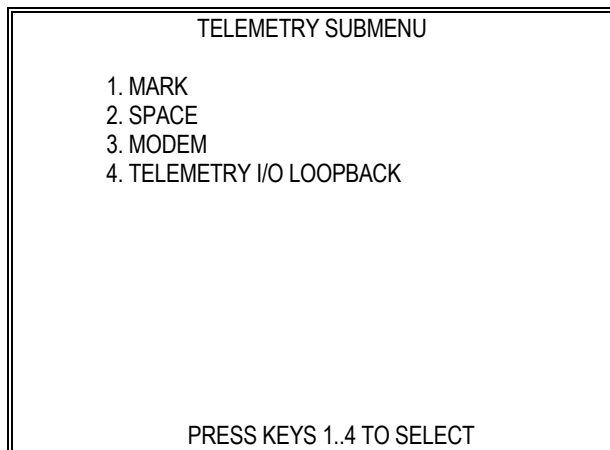
If this test uncovers an Overlap card failure, use the detailed description of the I/O section of the Processor-I/O and the schematic included in the document to pinpoint the problem.

OVERLAP PROGRAM CARD DATA								
PHASE	1	2	3	4	5	6	7	8
OVERLAP A								
OVERLAP B								
OVERLAP C								
OVERLAP D								

Telemetry (6)

This menu provides a set of functions for testing all aspects of the Telemetry module and the PORT3 and 25-pin Telemetry ports. Test loop back cable 33279G6 is required for testing the PORT3 Telemetry port. Loop back cable 33279G5 is required for testing the 25-pin Telemetry port. Perform the following steps:

1. Select MARK (1) or SPACE (2). This generates a Mark frequency of 1200 Hz or SPACE frequency of 2200 Hz. This signal can be viewed with an oscilloscope across resistors R28 and R29 on the telemetry module [34091, 4,6,A]. This signal should also be present across pins 1 and 2 of J17 [34251,7,3,B] the PORT3 telemetry connector and across pins 12 and 13 of connector J14 [34251,7,4,A] the 25-pin Telemetry connector, if installed. These signals can be used for line attenuation testing in the field. Push SUB MENU (F3) to exit either test.
2. Attach the appropriate loop back cable for the port to be tested. Select MODEM (3). This starts a test that transmits ASCII characters modulated by the modem transmitter. The modulated signal is routed back to the modem chips receiver via the loop back cable. The display will reflect the pass or fail condition. If test fails, replace Telemetry module. Check receiver/transmitter circuits. Refer to the detailed description of the Telemetry module and document 34091.
3. Attach the 33279G5 loop back cable to 25-pin Telemetry connector J14 [34251,7,4,B]. Select TELEMETRY I/O LOOP BACK (4). This tests the parallel I/O lines on the 25-pin Telemetry connector. Input and output circuitry including input multiplexers, logic level translators, output latches, and output drivers are exercised. The display will output a hexadecimal code corresponding to any I/O loop failure. Use this code in conjunction with Appendix F, document 34251, and the detailed description of the I/O section of the Processor-I/O module to determine the cause of failure.



### Loopback (7)

This menu provides a set of functions for performing loop back tests on the A, B, C, D, TERMINAL (PORT2) and SDLC (PORT1) connectors. Proceed as follows:

1. Attach the 33279G1, 33279G2 and 33279G3 loop back cables to the A, B and C connectors. Select STANDARD I/O (1). This tests the parallel I/O lines on the Type-2 I/O module connectors. Input and output circuitry including input multiplexers, logic level translators, output latches, and output drivers are exercised. The display will output a hexadecimal code corresponding to any I/O loop failure. Use this code in conjunction with APPENDIX F, document 34251 and the detailed description of the I/O section to determine the cause of failure.
2. Attach the 33279G4 loop back cable to the D connector. Select EXPANDED I/O (2). This tests the parallel I/O lines on the Expansion I/O module D connector. Input and output circuitry including input multiplexers, logic level translators, output latches, and output drivers are exercised. The display will output a hexadecimal code corresponding to any I/O loop failure. Use this code in conjunction with Appendix F, document 34251 and the detailed description of the I/O section to determine the cause of failure.
3. Attach the 33279G8 loop back cable to the Terminal port (PORT 2). Select TERMINAL (3). This starts a test that transmits ASCII characters through the RS-232 level translator chip and exercises the RS-232 hand shake lines. The signal is routed back to the translator chips receiver via the loop back cable. The display will reflect the pass or fail condition. If test fails, check signals at RS-232 transceiver chip U80 in the I/O section and DUART U20 in the processor section. Refer to the detailed descriptions of the Processor-I/O module, and document 34251.
4. Attach the 33279G7 loop back cable to the SDLC port (PORT 2). Select SDLC (3). This starts a test that transmits SDLC frames of ASCII characters through the RS-485 level translator chips. The signal is routed back to the translator receivers via the loop back cable. The display will reflect the pass or fail condition. If test fails, check signals at RS-485 transceiver chips U81 and 82 in the I/O section. Refer to detailed descriptions of Processor-I/O module and document 34251.

**Memory Tests**

The ASC/2S does not require keyboard entered memory testing. All memory tests are performed automatically as follows:

During power on, the controller does a preliminary check of all memory components. All system RAM chips are completely checked for read/write integrity. A check sum test is performed on each EPROM pair and program compatibility checks are performed. A cyclic redundancy check (CRC) is performed on the data module EEPROM. If any of these tests fail, an appropriate message is displayed and the program goes into a continuous loop with the voltage monitor ON which forces the intersection into flash.

After start up checks are performed, the controller enters the main program. While the main program is running, a CRC is continuously run, in background, on both the EPROMS and EEPROM. If either of these tests fail, an appropriate message is displayed and the program goes into a continuous loop with the voltage monitor ON which forces the intersection into flash.

The fault isolation tables in this section list malfunctions and their possible causes. The list is by no means complete but careful study of the symptoms may provide a starting point for troubleshooting.

Because of the modular design of the ASC/2S, repair at the cabinet level should be limited to removal and replacement of bad modules and fuses. Any in-depth fault isolation should be done in a shop with the proper test equipment. **Personnel and equipment should be properly grounded to prevent damage due to static electricity.** Exercise caution so that the programming integrity within the controller is maintained, as intended for the particular intersection, during removal and replacement of modules. Therefore, modules containing unique programming for a specific intersection (Processor module, overlap program board, Data module) must not be used operationally anywhere other than at that intersection.

If a problem is found, on the Processor-I/O module, the customer has the option to either repair the equipment or return it to Econolite for service. The User Interface and Power Supply modules should always be returned to Econolite for service. In any case, all information, relevant to the failure, must be recorded. If a defective module or the complete controller is returned for service, please send as much information as possible about the failure. Note the nature of the malfunction and details about the conditions affecting the controller at the time of failure. Try to reproduce the failure in a lab to determine the pattern, if any. Use these guidelines when documenting a failure.

Record:

- a) All controller settings. Print all data if possible.
- b) Mode of operation (coordination, preemption, NIC,).
- c) All external conditions (temperature, humidity, lightning,).
- d) Time of failure.
- e) Interconnect type.

Record details of a failure condition:

- f) Controller hangs-up.
- g) Record: The interval, how often hang-up occurs (every cycle, during a certain function,...).
- h) Controller skips intervals.
- i) Record: The interval, under what conditions (every cycle, only when external command is applied,...).

Use descriptive statements:

- j) Local not responding.
- k) Incorrect data in a readback.

## TROUBLESHOOTING PRECAUTIONS

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- i) Incorrect output at a local.
- j) Abnormal LCD indications.
- k) Improper signal indications on the same phase (conflicting conditions).

**The fault isolation tables are preceded by some precautions. It is imperative that these be read and understood before attempting to work on the ASC/2S controller.**

### PRECAUTIONS

#### CAUTION:

**Before doing any troubleshooting please note** that much of the ASC/2S operation is determined by the program contained in the configuration EEPROM.

1. Make sure that the program number on top of the controller matches the label number on EEPROM U1 located on the Data module.
2. If necessary, and if PROM programming equipment is available, use Appendix G to check EEPROM against required intersection configuration.
3. DO NOT unplug Data module while power is applied to the controller.

**Before working on any module ALWAYS** take the following precautionary steps:

4. Disconnect primary power from the controller before removing or installing modules.
5. Allow at least 15 seconds for the filter capacitors to discharge before working on any module in the controller.
6. Do not use low resistance VOM or continuity tester for continuity checks. These may damage CMOS circuits.
7. Remember to handle the Processor module with care to ensure that the on-card battery is not inadvertently shorted (such as by laying the module on a metal surface) or bent.
8. Be careful not to flex the Processor-I/O module excessively. When bench testing, the module should be supported by a fixture so that it lays flat and does not rest on the capacitor mounted on the read of the module.

#### **WARNING**

Line voltages are present on the Processor-I/O and Power Supply modules. Extreme care should be taken when working in these areas.

# TROUBLESHOOTING HARDWARE FAULT ISOLATION

## HARDWARE FAULT ISOLATION

A = Cabinet-level fault isolation.      B = Bench-level fault isolation.

PROBLEM	POSSIBLE CAUSE	ACTION
Controller is inoperative. Processor Monitor LED LED1 is OFF.	<ol style="list-style-type: none"> <li>1. 115 VAC fuse blown.</li> <li>2. Controller not supplied with 115 VAC.</li> <li>2. Loose power supply harnesses</li> <li>4. Power supply module failure</li> </ol>	<ol style="list-style-type: none"> <li>A) Check fuse F2 replace if necessary.</li> <li>2. A) Verify that power is applied.</li> <li>3. B) Check construction and seating of harnesses.</li> <li>4. B) Verify +24VDC output. Return supply to Econolite for repair.</li> </ol>
Time is lost when power removed. Timing incorrect or inconsistent or controller hangs up.	<ol style="list-style-type: none"> <li>1. Battery jumper JP2 not on.</li> <li>1. 120 Hz reference circuit.</li>   <li>2. OPTO1 circuit.</li> </ol>	<ol style="list-style-type: none"> <li>1. A) Remove/replace Processor-I/O module.</li> <li>B) Check AC power monitor circuit interrupt operation (U1)[8,4-6,A].</li> <li>2. A) Remove/replace Processor-I/O module.</li> <li>B) Check OPTO1 circuit [20,2-3,C]. <b>(CAUTION: LETHAL VOLTAGES PRESENT IN THIS CIRCUIT).</b></li> </ol>
Voltage monitor/ Fault monitor output FALSE	<ol style="list-style-type: none"> <li>1. Power supply out of tolerance, voltage or voltage monitor control circuit failed.</li>   <li>2. a) Preemptor phases programmed not IN USE when preemptor becomes active. b) Preemption active during power outage.</li> </ol>	<ol style="list-style-type: none"> <li>1. A) Remove/replace power supply.</li> <li>B) Check +24VDC and voltage monitor circuits [3,4,B].</li>   <li>2. a) Program preemptor phases IN USE (Recall data page PREEMPTOR Submenu).</li> </ol>
One phase has no outputs.	<ol style="list-style-type: none"> <li>1. I/O section failure. Output circuitry for phase in I/O Interface section failed.</li>   <li>2. Phase omitted in configuration PROM programming.</li> </ol>	<ol style="list-style-type: none"> <li>1. A) Remove/replace Processor-I/O Interface module.</li> <li>B) Check output circuit operation for the particular output.</li>   <li>2. A) Replace EEPROM with correct program.</li> <li>B) Reprogram EEPROM in order to correct phase omitted.</li> </ol>
Controller appears to be operating but all outputs are OFF.	<ol style="list-style-type: none"> <li>1. 24 V EXT fuse (F1) is blown.</li>   <li>2. Processor section failure. /PIOSL decode circuits failed.</li>   <li>3. I/O Interface module failure.</li> </ol>	<ol style="list-style-type: none"> <li>1. Check fuse F1.</li>   <li>2. A) Remove/replace Processor-I/O module.</li> <li>B) Check /PIOSL decode circuit operation U21 [4,4,C]. Check I/O module buffers U24 and U25 [4,2,B-D]</li>   <li>3.. Check output latch chip select decoder operation U22 [10,6,D].</li> </ol>
All outputs from one phase or one output does not turn ON.	<ol style="list-style-type: none"> <li>1. I/O section failure. Output driver failed.</li> </ol>	<ol style="list-style-type: none"> <li>1. A) Remove/replace Processor-I/O module.</li> <li>B) Check output latch and output driver for that phase.</li> </ol>
All inputs inoperative.	<ol style="list-style-type: none"> <li>1. I/O Interface section failure.</li>   <li>2. Processor section failed.</li> </ol>	<ol style="list-style-type: none"> <li>1. A) Remove/replace Processor-I/O module.</li> <li>B) Check I/O decoder U23 [12,6,D].</li>   <li>2. A) Remove/replace Processor-I/O module.</li> <li>B) Check /PIOSL decode circuit operation U21 [4,4,B]. Check I/O buffers U24 and U25 [4,3,B-D].</li> </ol>

# TROUBLESHOOTING HARDWARE FAULT ISOLATION

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PROBLEM	POSSIBLE CAUSE	ACTION
All inputs to one phase or one input inoperative.	1. I/O Interface section failure. Input multiplexer failed.  2. Phase not IN USE.	1.A) Remove/replace Processor-I/O module. B) Check input multiplexer operation for that particular phase.  2. Program phase IN USE on Recall data page Controller Submenu.
No inputs or outputs from a phase	1. Phase not IN USE.	1. Check Recall data page Controller Submenu.
Controller beeps repetitively. Does not accept any keyboard inputs.	1. A key is stuck ON or the keyboard control circuit failed.	1. A) Check User Interface control circuits [10,4-6,A-D]].
A key is inoperative or intermittently inoperative.	1. Keyboard failed.	1. Remove User Interface panel and return to Econolite for repair.
Phase sequencing problem.	1. Incorrect configuration EEPROM installed.	1. A) Remove/replace Data Module. B) Check configuration EEPROM programming if programming equipment available otherwise contact Econolite for another configuration EEPROM.
Controller hangs up after a certain condition occurs.	1. Program memory failed. Watch dog timer timed out.	1. A) Remove/replace Processor module. B) Use displayed message to localize problem. Check program memory and program memory circuit operation.
Controller hangs up and PROCESSOR MONITOR LED LED1 is ON.	1. Processor failed. 2. Power supply failed.	1. A) Remove/replace Processor module. B) Check processor operation. 1. A) Remove/replace power supply. B) Check power supply for low voltage output.
Characters are lost while printing.	1. XON / XOFF handshake protocol not recognized.	1. Program printer to recognize XON / XOFF protocol.



## SECTION 5 PARTS LISTS

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The parts list is divided into tables as shown. Parts are listed with both Econolite and manufacturer's part numbers and primary and secondary descriptions. All components of the ASC/2S controller are listed including software. Only one supplier part number is given; however, qualified equivalent parts, as determined by Econolite, may be used.

When ordering controller software always specify the latest software version and part number.

**\*\* CAUTION \*\***

HC and HCT CMOS parts are NOT interchangeable. When changing parts, be careful to replace with the same type of part.

<u>Table</u>	<u>Title</u>
5-1	Controller Assembly ASC/2S-1000 (34240G1) [E]
5-2	Controller Assembly ASC/2S-2000 (34240G2)[E]
5-3	Controller Assembly ASC/2S-2100 (34240G3)[F]
5-4	Controller Assembly ASC/2S-2100 with OLAP (32420G4)[F]
5-5	Processor-I/O PCB Subassembly ASC/2S-1000 (34250G1)[J]
5-6	Processor I/O PCB Subassembly ASC/2S-2000 (34250G2)[J]
5-7	Processor I/O PCB Subassembly ASC/2S-2100 (34250G3)[K]
5-8	Processor I/O PCB Subassembly ASC/2S-2100 Exp W/Olap (34250G4)[A]
5-9	Telemetry PCB Assembly (34090G1)[G]
5-10	RS-232 Telemetry PCB Assembly (33525G1)[F]
5-11	Data Module PCB Assembly (32845G2)[A]

# PARTS LISTS

Table 5-1. Controller Assembly ASC/2S-1000 (34240G1) (Page 1 of 1)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
34240	ASSY DWG ASC/2S		
34285G2	C/C ASSY P/S DC OUTPUT	INTERNAL CABLE ASC/2S	
34250G1	PCA PROCESSOR I/O INTF	CONTROLLER TYPE 1	
32845G2	PCA DATA MODULE ASC/2	W/EPROM 32K X 8	
34280P1	POWER SUPPLY	110VAC 50/60HZ	POWER ONE MAP42-S204
N695P9008C	SCRW SEMS #4 X 1/2	PH PHIL	
N695P9006C	SCRW SEMS #4 X 3/8	PH PHIL	
N44P9005C	SCRW #4 X 5/16 FIL SLT	STL CD MACH	
N695P13004C	SCRW SEMS #6 X 1/4	PH PHIL	
31348P51	BLOCK LATCHING 2 PC PKG		AMP 745286-2
34269P1	RESTRAINT, CABLE	ASC/2S A/MD	
32542P1	STUD SNAP IN .345L	SLOTTED HD 1/4 TURN	SOUTHCO 82-11-200-16-1 SEE ENG DWG
31144P1	IDENT PLATE CNTLR	ECONOLITE	
34255G1	CHASSIS SUB ASSY		
34259P1	PLATE CONN, TYPE 1		
34260G1	DISPLAY PANEL ASC/2S		DENSITRON HC4129BGHNGO345
34285G1	C/C ASSY PS AC INPUT		
N138P9008C	SCRW SEMS #4 X 1/2 PH SLT		
N238P9B	HEX NUT/LK WSHR #4 STL/CAD		
32542P20	FSTNR BAIL RING		SOUTHCO 82-15-200-16
32542P103	WSHR WEAR CUP	NYLON BLACK	SOUTHCO 82-46-101-41
32542P106	SPRING RETAINER	1/4 TURN	SOUTHCO 43-13-1-24
32542P100	RETAINER LOCK RING	S/STL NO. 82	SOUTHCO 82-32-201-20
53048P15	TIE CABLE 4" DIA ST	BLACK	DENNISON 10-408
55399P1	GROMMET STRIP	.062-.099 THK	PANDUIT GES99F-A-C
53048P12	TIE CABLE .75" DIA ST	BLACK	DENNISON 08-404

Table 5-2. Controller Assembly ASC/2S-2000 (34240G2) (Page 1 of 1)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
34240	ASSY DWG ASC/2S		
34255G1	CHASSIS SUB ASSY	ASC/2S	
34259P2	ASSY, PLATE CONN	TYPE 2 ASC/2S	
		D/AD	
34260G1	DISPLAY PANEL ASC/2S		DENSITRON HC4129BGHNG0345
		ASC/2S 34251S 34253AW	
		256K RAM	
34250G2	PCA PROCESSOR I/O INTERFACE	TYPE 2	
32845G2	PCA DATA MODULE ASC/2	W/EPROM 32K X 8	
34280P1	POWER SUPPLY	110VAC 50/60HZ	POWER ONE MAP42-S204
N695P9006C	SCRW SEMS #4 X 3/8	PH PHIL	
N44P9005C	SCRW #4 X 5/16 FIL SLT	STL CD MACH	
N695P13004C	SCRW SEMS #6 X 1/4	PH PHIL	
31348P51	BLOCK LATCHING 2 PC PKG		AMP 745286-2
34269P1	RESTRAINT, CABLE	ASC/2S A/MD	
32542P1	STUD SNAP IN .345L	SLOTTED HD 1/4 TURN	SOUTHCO 82-11-200-16-1
31144P1	IDENT PLATE CNTLR	ECONOLITE	SEE ENG DWG
34285G1	C/C ASSY PS AC INPUT		
N138P9008C	SCRW SEMS #4 X 1/2 PH SLT		
N238P9B	HEX NUT/LK WSHR #4 STL/CAD		
32542P20	FSTNR BAIL RING		SOUTHCO 82-15-200-16
32542P103	WSHR WEAR CUP	NYLON BLACK	SOUTHCO 82-46-101-41
32542P106	SPRING RETAINER	1/4 TURN	SOUTHCO 43-13-1-24
32542P100	RETAINER LOCK RING	S/STL NO. 82	SOUTHCO 82-32-201-20
53048P15	TIE CABLE 4" DIA ST	BLACK	DENNISON 10-408
55399P1	GROMMET STRIP	.062-.099 THK	PANDUIT GES99F-A-C
53048P12	TIE CABLE .75" DIA ST	BLACK	DENNISON 08-404

# PARTS LISTS

Table 5-3. Controller Assembly ASC/2S-2100 (34240G3) (Page 1 of 1)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY D ESCRIPTION	MFGR/PART#
34240	ASSY DWG ASC/2S		
34255G1	CHASSIS SUB ASSY	ASC/2S	
34259P3	ASSY, PLATE CONN	TYPE 2 EXP ASC/2S D/AD	
34260G1	DISPLAY PANEL ASC/2S		DENSITRON HC4129BGHNG0345
34285G1	C/C ASSY PS AC INPUT	INTERNAL CABLE ASC/2S	
34285G2	C/C ASSY P/S DC OUTPUT	INTERNAL CABLE ASC/2S	
34250G3	PCA PROCESSOR I/O INTF	CONTROLLER TYPE 2 EXP ASC/2S	
32845G2	PCA DATA MODULE ASC/2	W/EPROM 32K X 8	
34280P1	POWER SUPPLY	110VAC 50/60HZ	POWER ONE MAP42-S204
N695P9006C	SCRW SEMS #4 X 3/8	PH PHIL	
N695P13008C	SCRW SEMS #6 X 1/2	PH PHIL	
N44P9005C	SCRW #4 X 5/16 FIL SLT	STL CD MACH	
N695P13004C	SCRW SEMS #6 X 1/4	PH PHIL	
31348P51	BLOCK LATCHING 2 PC PKG		AMP 745286-2
31348P12	LATCH SPRING	1 SET PER PKG	CANNON D110277
34269P1	RESTRAINT, CABLE	ASC/2S A/MD	
32542P1	STUD SNAP IN .345L	SLOTTED HD 1/4 TURN	SOUTHCO 82-11-200-16-1
31144P1	IDENT PLATE CNTLR	ECONOLITE	SEE ENG DWG
N138P9008C	SCRW SEMS #4 X 1/2 PH SLT		
N238P9B	HEX NUT/LK WSHR #4 STL/CAD		
32542P20	FSTNR BAIL RING		SOUTHCO 82-15-200-16
32542P103	WSHR WEAR CUP	NYLON BLACK	SOUTHCO 82-46-101-41
32542P106	SPRING RETAINER	1/4 TURN	SOUTHCO 43-13-1-24
32542P100	RETAINER LOCK RING	S/STL NO. 82	SOUTHCO 82-32-201-20
53048P15	TIE CABLE 4" DIA ST	BLACK	DENNISON 10-408
55399P1	GROMMET STRIP	.062-.099 THK	PANDUIT GES99F-A-C
53048P12	TIE CABLE .75" DIA ST	BLACK	DENNISON 08-404

Table 5-4. Controller Assembly ASC/2S-2100 with OLAP (34240G4) (Page 1 of 1)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
34240	ASSY DWG ASC/2S		
34255G1	CHASSIS SUB ASSY	ASC/2S	
34259P3	ASSY, PLATE CONN	TYPE 2 EXP ASC/2S D/AD	
34260G1	DISPLAY PANEL ASC/2S		DENSITRON HC4129BGHNG0345
34285G1	C/C ASSY PS AC INPUT	INTERNAL CABLE ASC/2S	
34285G2	C/C ASSY P/S DC OUTPUT	INTERNAL CABLE ASC/2S	
34250G4	PCA PROCESSOR I/O INTF	CNTRL TYPE 2 EXP W/OLAP	
32845G2	PCA DATA MODULE ASC/2	W/EPROM 32K X 8	
34280P1	POWER SUPPLY	110VAC 50/60HZ	POWER ONE MAP42-S204
N695P9006C	SCRW SEMS #4 X 3/8	PH PHIL	
N695P13008C	SCRW SEMS #6 X 1/2	PH PHIL	
N44P9005C	SCRW #4 X 5/16 FIL SLT	STL CD MACH	
N695P13004C	SCRW SEMS #6 X 1/4	PH PHIL	
31348P51	BLOCK LATCHING 2 PC PKG		AMP 745286-2
31348P12	LATCH SPRING	1 SET PER PKG	CANNON D110277
34269P1	RESTRAINT, CABLE	ASC/2S A/MD	
32542P1	STUD SNAP IN .345L	SLOTTED HD 1/4 TURN	SOUTHCO 82-11-200-16-1
31144P1	IDENT PLATE CNTLR	ECONOLITE	SEE ENG DWG
31775G1	PCB ASSY O/LAP STD NEMA	B/AD 31777AW	
N138P9008C	SCRW SEMS #4 X 1/2 PH SLT		
N238P9B	HEX NUT/LK WSHR #4 STL/CAD		
32542P20	FSTNR BAIL RING		SOUTHCO 82-15-200-16
32542P103	WSHR WEAR CUP	NYLON BLACK	SOUTHCO 82-46-101-41
32542P106	SPRING RETAINER	1/4 TURN	SOUTHCO 43-13-1-24
32542P100	RETAINER LOCK RING	S/STL NO. 82	SOUTHCO 82-32-201-20
53048P15	TIE CABLE 4" DIA ST	BLACK	DENNISON 10-408
55399P1	GROMMET STRIP	.062-.099 THK	PANDUIT GES99F-A-C
53048P12	TIE CABLE .75" DIA ST	BLACK	DENNISON 08-404

# PARTS LISTS

Table 5-5. Processor-I/O PCB Subassembly ASC/2S-1000 (34250G1)\* (Page 1 of 5)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
34250	ASSEMBLY DRAWING	PROCESSOR I/O	
34251	SCHEMATIC PROCESSOR I/O		
34253	MASTER ARTWORK	PROCESSOR I/O	
34254	TEST SPEC	PROCESSOR I/O	
34252P1	PCB PROCESSOR I/O INTF	ASC/2S	
32911P21	BTRY 3V PC MTG B1	LITHIUM	PANASONIC VL2330-1VC
33748P5103	CAPAC .01MF 50V C1 C3 C4 C8 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C26 C27 C28 C32 C33 C34 C35 C36 C37 C38 C45 C46 C47 C48 C75	SMT 0603 10% X7R CERM	AVX 06035C103KAT2A
33740P5220	CAPAC 22PF 50V C12	SMT 0805 COG CERAM	MURATA GRM40COG220J050BD
33741P5104	CAPAC .1MF 50V C2 C11 C68	SMT 1206 10% X7R CERM	KEMET C1206C104K5RAC
33877P105	CAPAC 1MF 35V TANT C29	SMT 3528	SPRAGUE 293D105X9035B2T
33878P10	CAPAC 10MF 35V ELECT C31	SMT NEMCO CASE B	NICHICON UWX1V100MCR1GB
33740P5270	CAPAC 27PF 50V C43	SMT 0805 COG CERAM	MURATA GRM40COG270J050BD
33740P5330	CAPAC 33PF 50V C44	SMT 0805 COG CERAM	MURATA GRM40COG330J050BD
31884P4	CAP VARIABLE 7-50PF C5	SMT A-TYPE	MURATA TZBX4R500BA110
32895P7	CAPAC 120MF 50V ELECT C6 C7		NICHICON UPL1H121MPH
33878P047	CAPAC 4.7MF 25V ELECT C66 C67 C71 C72 C73	SMT NEMCO CASE B	NICHICON UWX1E4R7MCR1GB
32169P19	CAPAC ELECT 18000MF 35V C76	AL SNAP MTG	NICHICON LLK1V183MHSC
31769P61	TRANSORB P6KE27A CR1	25.7-28.4V	GEN INST P6KE27A
33870P1	DIODE FDLL4148 CR2 CR12 CR13	SMT D035	NATIONAL FDLL4148

\*For Parts lists 34250G1, 34250G2, and 34250G3 the following note applies.

One 8 MB of flash PROM (U2) can be replaced by installing two 4 MB flash PROMs in locations U2 and U92. The following parts must also be installed: C78, C79, C80, R82, R83 and U93.

33748P5103	CAPAC .01MF 50V C78*C79		AVX* 06035C103KAT2A
33748P5471	CAPAC 470PF 50V C80		MURATA ERIE GRM39X7R47K050B
33872P122	RES 1.2K 5% 1/16W R82*R83		DALE CRCW0603122J
33901P1	IC 29F400BB FLASH 4 MB U2*U92		AMD AM29F400BB-90EC
33902P32	IC 74VHC32 SMT S014 U93		FAIRCHILD 74VHC32MTC

Table 5-5. Processor-I/O PCB Subassembly ASC/2S-1000 (34250G1) (Page 2 of 5)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
58064P12	DIODE 1N4763A CR24	1W ZENER	MOTOROLA 1N4763A
32416P6	DIODE BRIDGE 1A 800V CR25	4 PIN DIP	DIODES INC DB106 OR DF08
33831P4	DIODE MBR0520 20V 1/2A CR3 CR5 CR11	SCHOTTKY SMT CASE 403	MOTOROLA MBR0520LT1
33831P3	DIODE MRB34 34V CR4 CR6 CR7 CR8 CR10	SCHOTTKY SMT CASE 403	MOTOROLA MBRS340TS
58873P29	DIODE 1N5232B 5.6V 5% CR9	500MW ZENER REPLACES 58052P6	MOTOROLA 1N5232B
55205P17	FUSE 3/4A 250V 3AG S/B F1	1.25 X .25	LITTELFUSE 313.750
55205P19	FUSE 1A 250V 3AG S/B 3 F2	1.25X.25	LITTELFUSE 313001
32183P4	FUSE HLDR W/CARRIER XF1 XF2	SOLDER TERM	SCHURTER FEU031.1659
31912P1	SPCR NYL .50ID X.76OD XF1 XF2	.18 THK 3 AG F/HLDR	SEASTROM 5606-44-177
57255P700	WIRE 22AWG BLK 19 STRD XF1 XF2	TYPE B/N 600V	SEE ENG SPEC TDK
32758P1	INDUCTOR FERRITE BEAD FB1 FB2 FB3 FB4		BF45-4002
33857P10	CONN 10P PCMT J16	CIRCULAR	ITT CANNON CA24252-2599
31369P27	CONN D SUB 25S W/W J13	METAL SHELL	CINCH DBKL-25SUT
31369P26	CONN D SUB 15S W/W J15	METAL SHELL	CINCH DAKL-15SUT
31369P25	CONN D SUB 9P J17	METAL SHELL	CINCH DEKL-09PUTI
58751P32	HDR 3 CKT LKG STRGHT J18	.156 CTRS W/LOCK GOLD	MOLEX 26-61-4030
58751P14	WAFER POLARIZING 5 CKT J19	.156 CTRS W/LOCK	AMP 640388-5
33852P68	CONN 68 PIN STRAIGHT J2	.050 PITCH	MOLEX 15-92-1468
32158P113	HDR 13/26 CTR POL STR J3	.100 CTRS W/SHORT LATCH	HIROSE HIF3BAG-26PA-2.54DSA
32219P1	CONN DIN 32P R/A J4	W/W .512L	PANDUIT 100-632-051
32219P8	CONN DIN 32S STR J5	A/SD	PANDUIT 100-632-432
31535P1	WAFER 2 CKT J7 J8 TP1 TP2 TP3	.100 CTRS	MOLEX 22-03-2021
31535P2	WAFER 3 CKT JP2 JP3 JP4 JP5	.100 CTRS	MOLEX 22-03-2031
33879P1	INDUCTOR POWER SMT L1	DO3316	COILCRAFT DO3316P-104
56668P3	CHOKE HASH 250MH L2		JW MILLER 5254
37129P2	DIODE LED BRIGHT RED LED1		GEN INST MV5752
33730P2	XSTR 2N3904 NPN Q1	SMT SOT23 GENERAL PURPOSE	ZETEX FMMT3904-NDA
33872P103	RES 10K 5% 1/16W SMT R1 R6 R8 R26 R27 R32 R40 R44 R55	0603	DALE CRCW0603103J

# PARTS LISTS

Table 5-5. Processor-I/O PCB Subassembly ASC/2S-1000 (34250G1) (Page 3 of 5)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
33872P681	RES 680 5% 1/16W SMT R10	0603	DALE CRCW0603681J
33872P000	RES00HM 5% 1/6W R81	SMT0603	DALE CRCW0603000J
33872P331	RES 330 5% 1/16W SMT R11 R16 R20 R45 R46 R48 R51 R52	0603	DALE CRCW0603331J
54719P153	RES 22 MEG 1/4W 5% R12	MIL-R-11F FIXED COMP	RC07GF226J
33873P5491	RES 5.49K 1% 1/16W SMT R14	0603	DALE CRCW06035491F
33873P1302	RES 13K 1% 1/16W SMT R17	0603	DALE CRCW06031302F
33872P472	RES 4.7K 1/16W SMT R19 R30	0603	DALE CRCW0603472J
33873P2212	RES 22.1K 1% 1/16W SMT R2	0603	DALE CRCW0602212F
33873P1002	RES 10K 1% 1/16W SMT R22, R76, R77, R78, R79	0603	DALE CRCW06031002F
33872P105	RES 1M 5% 1/16W SMT R23 R25	0603	DALE CRCW0603105J
33872P102	RES 1K 5% 1/16W SMT R24	0603	DALE CRCW0603102J
33872P221	RES 220 5% 1/16W SMT R28	0603	DALE CRCW0603221J
33872P473	RES 47K 5% 1/16W SMT R29 R34	0603	DALE CRCW0603473J
33873P9092	RES 90.9K 1% 1/16W SMT R3	0603	DALE CRCW06039092F
54582P5	RES 15 OHMS 1/2W 5% R31	FIXED COMP	A/BRADLEY EB1505
33825P000	RES ZERO OHM JUMPER R35	THICK FILM 0805	DALE CRCW080500J
33872P271	RES 270 5% 1/16W SMT R36	0603	DALE CRCW063271J
33872P101	RES 100 5% 1/16W SMT R37 R42 R47	0603	DALE CRCW0603101J
33872P112	RES 1.1K 5% 1/16W SMT R38	0603	DALE CRCW0603112J
33872P122	RES 1.2K 5% 1/16W SMT R39 R41 R82 R83	0603	DALE CRCW0603122J
33873P5112	RES 51.1K 1% 1/16W SMT R4 R5	0603	DALE CRCW06035112F
33711P000	RES ZERO OHM JUMPER SMT R43 R50 R60	THICK FILM 1206	KOA SPEER RM73Z2BT
33873P6813	RES 681K 1% 1/16W SMT R49	0603	DALE CRCW06036813F
33713P222	RES 2.2K 5% 1/2W SMT R56	THICK FILM 2010	DALE CRCW2010222J
33872P183	RES 18K 5% 1/16W SMT R64	0603	DALE CRCW0603183J
43654P2	RES 2.2 OHMS 5W R65 R67	WIRE WOUND	OHMITE 95J2R2
33872P152	RES 1.5K 5% 1/16W SMT R68 R70 R71 R73	0603	DALE CRCW0603152J
33872P121	RES 120 5% 1/16W SMT R69 R72	0603	DALE CRCW0603121J
33873P4493	RES 449K 1% 1/16W SMT R7	0603	DALE CRCW06034493F



Table 5-5. Processor-I/O PCB Subassembly ASC/2S-1000 (34250G1) (Page 4 of 5)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
31263P97	RES 10K 3W 5% W/W R74 R75	REPLACES 0500-0039	DALE CW2C-14-10K 5%
33873P1003	RES 100K 1% 1/16W SMT R9 R15 R18	0603	DALE CRCW06031003F
43577P3	RES NTWK 10K COM PIN RP1 RP2 RP10 RP34	10 PIN SIP 9 RES 1W 2% REPLACES 0500-0213	BOURNS 4610X-101-103
43577P26	RES NTWK 10K COM PIN RP3 RP4	10 PIN 9 RES MOLDED	BOURNS 4310R-101-103
31770P1	VARISTOR 55 JOULES RV1 RV2 RV3	212V-255V METAL OXIDE UL/CSA RECOGNIZED	HARRIS V150LA20B
33859P1	IC 14538B DUAL MONOSTBL U1 U5	PRECISION SMT SO16-.150	MOTOROLA MC14538BDW
33772P2	IC LM393 U10	DUAL COMPARATOR SMT S08-.150	NATIONAL LM393M
33864P09	IC TTL LPS 74LS09 U11	QUAD 2 INPUT POS ANGATE SMT SO14-.150	MOTOROLA SN74LS09D
32878P1	IC 68302 U12	SMT PQFP-132	MOTOROLA MC68302FC16C
34245P13	IC PRGMD PER 34245 U13	GAL16V8B M/F 34290P1	SEE ENG DWG
33854P32	IC ALSMOS 74ALS32 U14	QUAD 2-INPUT POS-ORGATE SMT SO14-.150	NATIONAL DM74ALS32M
33703P04	IC ACTMOS 74ACT04 U15	HEX INVERTER SMT SO14-.150	NATIONAL 74ACT04SC
33854P08	IC ALSMOS 74ALS08 U16	QUAD 2-INPUT AND-GATE SMT SO14-.150	NATIONAL DM74ALS08M
33863P244	IC HCTMOS 74HCT244 U17 U18 U19 U24 U39	OCTAL BUFFER/LINE DRVR SMT SO20-.300	MOTOROLA MC74HCT244AD
33860P1*	IC 29F800BB U2	SMT TSOP48	AMD AM29F800BB-90EC
33865P1	IC 88C681 U20	SMT PLCC44	PHILLIPS SCN2681TC1A44
34247P21	IC PRGMD PER 34247 U21	GAL16V8D M/F 33866P1	SEE ENG DWG
34248P22	IC PRGMD PER 34248 U22	GAL16V8D M/F 33866P1	SEE ENG DWG
33863P138	IC HCTMOS 74HCT138 U23	3 TO 8 LINE DECODE/DMUX SMT SO16-.150	MOTOROLA MC74HCT138AD
33863P245	IC HCTMOS 74HCT245 U25 U38	OCTAL BUS TRANSCVR SMT SO20-.300	MOTOROLA MC74HCT245AD
33861P1	IC 68HC68T U3	SMT SOIC16-.300	MOTOROLA MC68HC68T1DW
33868P1	IC 2598 VOLTAGE REG U4	SMT	NATIONAL LM2598-5.0
33858P1	IC 128K X 8 STATIC RAM U6 U7	100 NS SMT SOL32-.500	HITACHI HM628128BLFP-10
31414P3	XSTR NTWK ULN-2803A U64 U69 U74	18P DIP DARLINGTON TESTED REPLD 0900-0132	SPRAGUE ULN2803A
40029P4	VOLT REG +12V U79	TO-220 1 AMP	MOTOROLA MC7812CP
33764P4	IC MAX214 U80	QUAD RS-232 XMTR/RCVR SMT SO28-.300	MAXIM MAX214CWI

# PARTS LISTS

Table 5-5. Processor-I/O PCB Subassembly ASC/2S-1000 (34250G1) (Page 5 of 5)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
33853P1	IC 490 RS-485 XMTR U81 U82	SMT SO8-.150	LINEAR TECH LTC490CS8
33851P1	IC MMBZ15VDLT1 U83 U84 U85 U86 U87 U88 U89 U90	SMT SOT23	MOTOROLA MMBZ15VDLT1
43730P2	IC MCT6 DUAL OPTO ISOL U91	8P DIP	MONSANTO MCT6
33737P3	XTAL 32.768KHZ Y1	SMT MC-405	EPSON MC-405-32.768K-A2
33737P4	XTAL 14.7456MHZ Y2	SMT MA-505	EPSON MA-505-14.745M-C2
33245P8	HEATSINK PLUG-IN TO-220 XU79		AAVID 576802B03100
32289P1	JUMPER SHORTING XJP2 XJP3 XJP4 XJP5 XJ7 XJ8		AMP 531220-2
56671P41	STNDF SWAGE #4 X .125 M2 M3	.25 DIA BRS/NI	UNICORP SS240-1-D-7
56671P4	STNDF SWAGE #4 X.469L XJ16	.25 DIA BRS/NI	UNICORP SS251-1-D-7
56671P42	STNDF SWAGE #4 X .250 XJ13 XJ15 XJ17	.25 DIA BRS/NI	UNICORP SS244-1-D-7
56671P25	STNDF SWAGE #2 X .38L XJ4	.16 DIA BRS/NIC	UNICORP SS130-1-D-7
N57P5006C	SCRW #2 X 3/8 PH SLT XJ4	STL CD MACH	
N404P8C	WSHR LK INT #2 STL XJ4	CAD PLATED	
33395P3	SPCR PCB LKING .38L	1/4 TURN PLASTIC	HARTWELL HNST4-375-1
53048P12	TIE CABLE .75" DIA ST	BLACK	DENNISON 08-404

Table 5.6. Processor I/O PCB Subassembly ASC/2S-2000 (34250G2)\* (Page 1 of 6)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
34250	ASSEMBLY DRAWING	PROCESSOR I/O	
34251	SCHEMATIC PROCESSOR I/O		
34253	MASTER ARTWORK	PROCESSOR I/O	
34254	TEST SPEC	PROCESSOR I/O	
34252P1	PCB PROCESSOR I/O INTF	ASC/2S	
32911P21	BTRY 3V PC MTG B1	LITHIUM	PANASONIC VL2330-1VC
33748P5103	CAPAC .01MF 50V C1 C3 C4 C8 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C26 C27 C28 C32 C33 C34 C35 C36 C37 C38 C45 C46 C47 C48 C49 C50 C51 C52 C53 C54 C55 C61 C62 C63 C64 C65 C70 C75	SMT 0603 10% X7R CERM	AVX 06035C103KAT2A
33740P5220	CAPAC 22PF 50V C12	SMT 0805 COG CERAM	MURATA GRM40COG220J050BD
33741P5104	CAPAC .1MF 50V C2 C11 C68	SMT 1206 10% X7R CERM	KEMET C1206C104K5RAC
33877P105	CAPAC 1MF 35V TANT C29	SMT 3528	SPRAGUE 293D105X9035B2T
33878P10	CAPAC 10MF 35V ELECT C31 C69	SMT NEMCO CASE B	NICHICON UWX1V100MCR1GB
33740P5270	CAPAC 27PF 50V C43	SMT 0805 COG CERAM	MURATA GRM40COG270J050BD
33740P5330	CAPAC 33PF 50V C44	SMT 0805 COG CERAM	MURATA GRM40COG330J050BD
31884P4	CAP VARIABLE 7-50PF C5	SMT A-TYPE	MURATA TZBX4R500BA110
32895P7	CAPAC 120MF 50V ELECT C6 C7		NICHICON UPL1H121MPH
33878P047	CAPAC 4.7MF 25V ELECT C66 C67 C71 C72 C73	SMT NEMCO CASE B	NICHICON UWX1E4R7MCR1GB
32169P19	CAPAC ELECT 18000MF 35V C76	AL SNAP MTG	NICHICON LLK1V183MHSC
33745P2105	CAPAC 1MF 16V C9 C10 C25	SMT 3216 20% TANT	KEMET T491A105M016AS

\*For Parts lists 34250G1, 34250G2, and 34250G3 the following note applies.

One 8 MB of flash PROM (U2) can be replaced by installing two 4 MB flash PROMs in locations U2 and U92. The following parts must also be installed: C78, C79, C80, R82, R83 and U93.

33748P5103	CAPAC .01MF 50V C78*C79		AVX* 06035C103KAT2A
33748P5471	CAPAC 470PF 50V C80		MURATA ERIE GRM39X7R47K050B
33872P122	RES 1.2K 5% 1/16W R82*R83		DALE CRCW0603122J
33901P1	IC 29F400BB FLASH 4 MB U2*U92		AMD AM29F400BB-90EC
33902P32	IC 74VHC32 SMT S014 U93		FAIRCHILD 74VHC32MTC

# PARTS LISTS

Table 5.6. Processor I/O PCB Subassembly ASC/2S-2000 (34250G2) (Page 2 of 6)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
31769P61	TRANSORB P6KE27A CR1 CR22 CR23	25.7-28.4V	GEN INST P6KE27A
31769P59	TRANSORB P6KE6.8A CR14	600W UNIDIRECTIONAL 6.45-7.14V	MOTOROLA P6KE6.8A
31769P60	TRANSORB P6KE33A CR18 CR19	600W UNIDIRECTIONAL 31.4-34.7V	MOTOROLA P6KE33A
33870P1	DIODE FDLL4148 CR2 CR12 CR13 CR15 CR17 CR20	SMT D035	NATIONAL FDLL4148
58064P12	DIODE 1N4763A CR24	1W ZENER	MOTOROLA 1N4763A
32416P6	DIODE BRIDGE 1A 800V CR25	4 PIN DIP	DIODES INC DB106 OR DF08
33831P4	DIODE MBR0520 20V 1/2A CR3 CR5 CR11	SCHOTTKY SMT CASE 403	MOTOROLA MBR0520LT1
33831P3	DIODE MRB340 34V CR4 CR6 CR7 CR8 CR10	SCHOTTKY SMT CASE 403	MOTOROLA MBRS340TS
58873P29	DIODE 1N5232B 5.6V 5% CR9	500MW ZENER REPLACES 58052P6	MOTOROLA 1N5232B
55205P17	FUSE 3/4A 250V 3AG S/B F1	1.25 X .25	LITTELFUSE 313.750
55205P19	FUSE 1A 250V 3AG S/B 3 F2	1.25X.25	LITTELFUSE 313001
32183P4	FUSE HLDR W/CARRIER XF1 XF2	SOLDER TERM	SCHURTER FEU031.1659
31912P1	SPCR NYL .50ID X.76OD XF1 XF2	.18 THK 3 AG F/HLDR	SEASTROM 5606-44-177
57255P700	WIRE 22AWG BLK 19 STRD XF1 XF2	TYPE B/N 600V	SEE ENG SPEC
32758P1	INDUCTOR FERRITE BEAD FB1 FB2 FB3 FB4		TDK BF45-4002
31058P4	CONN CIRC 61S BOX MTG J10	D/SLDR CONT MIL-C-26482	CANNON KPT02E24-61S SPCL
31058P3	CONN CIRC 55S BOX MTG J11	D/SLDR CONT MIL-C-26482	CANNON KPT02E2255S SPCL
31058P2	CONN CIRC 55P BOX MTG J12	D/SLDR CONT MIL-C-26482	CANNON KPT02E22-55PDV
31369P27	CONN D SUB 25S W/W J13	METAL SHELL	CINCH DBKL-25SUT
31369P26	CONN D SUB 15S W/W J15	METAL SHELL	CINCH DAKL-15SUT
31369P25	CONN D SUB 9P J17	METAL SHELL	CINCH DEKL-09PUTI
58751P32	HDR 3 CKT LKG STRGHT J18	.156 CTRS W/LOCK GOLD	MOLEX 26-61-4030
58751P14	WAFER POLARIZING 5 CKT J19	.156 CTRS W/LOCK	AMP 640388-5
33852P68	CONN 68 PIN STRAIGHT J2	.050 PITCH	MOLEX 15-92-1468
32158P113	HDR 13/26 CTR POL STR J3	.100 CTRS W/SHORT LATCH	HIROSE HIF3BAG-26PA-2.54DSA
32219P1	CONN DIN 32P R/A J4	W/W .512L	PANDUIT 100-632-051
32219P8	CONN DIN 32S STR J5	A/SD	PANDUIT 100-632-432
31535P1	WAFER 2 CKT J7 J8 TP1 TP2 TP3	.100 CTRS	MOLEX 22-03-2021

Table 5.6. Processor I/O PCB Subassembly ASC/2S-2000 (34250G2) (Page 3 of 6)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
31535P2	WAFER 3 CKT JP2 JP3 JP4 JP5	.100 CTRS	MOLEX 22-03-2031
33879P1	INDUCTOR POWER SMT L1	DO3316	COILCRAFT DO3316P-104
56668P3	CHOKER HASH 250MH L2		JW MILLER 5254
37129P2	DIODE LED BRIGHT RED LED1		GEN INST MV5752
33730P2	XSTR 2N3904 NPN Q1	SMT SOT23 GENERAL PURPOSE	ZETEX FMMT3904-NDA
33730P1	XSTR NPN 2222A Q2	SMT SOT23	MOTOROLA MMBT2222A
33872P103	RES 10K 5% 1/16W SMT R1 R6 R8 R26 R27 R32 R40 R44 R54 R55	0603	DALE CRCW0603103J
33872P681	RES 680 5% 1/16W SMT R10	0603	DALE CRCW0603681J
33872P331	RES 330 5% 1/16W SMT R11 R16 R20 R45 R46 R48 R51 R52	0603	DALE CRCW0603331J
54719P153	RES 22 MEG 1/4W 5% R12	MIL-R-11F FIXED COMP	
33873P5491	RES 5.49K 1% 1/16W SMT R14	0603	RC07GF226J DALE CRCW06035491F
33873P1302	RES 13K 1% 1/16W SMT R17	0603	DALE CRCW06031302F
33872P472	RES 4.7K 1/16W SMT R19 R30	0603	DALE CRCW0603472J
33873P2212	RES 22.1K 1% 1/16W SMT R2	0603	DALE CRCW06032212F
33873P1002	RES 10K 1% 1/16W SMT R22 R76 R77 R78 R79	0603	DALE CRCW06031002F
33872P105	RES 1M 5% 1/16W SMT R23 R25	0603	DALE CRCW0603105J
33872P102	RES 1K 5% 1/16W SMT R24	0603	DALE CRCW0603102J
33872P221	RES 220 5% 1/16W SMT R28	0603	DALE CRCW0603221J
33872P473	RES 47K 5% 1/16W SMT R29 R34	0603	DALE CRCW0603473J
33873P9092	RES 90.9K 1% 1/16W SMT R3	0603	DALE CRCW06039092F
54582P5	RES 15 OHMS 1/2W 5% R31	FIXED COMP	A/BRADLEY EB1505
33825P000	RES ZERO OHM JUMPER R35	THICK FILM 0805	DALE CRCW080500J
33872P271	RES 270 5% 1/16W SMT R36	0603	DALE CRCW063271J
33872P101	RES 100 5% 1/16W SMT R37 R42 R47	0603	DALE CRCW0603101J
33872P112	RES 1.1K 5% 1/16W SMT R38	0603	DALE CRCW0603112J
33872P122	RES 1.2K 5% 1/16W SMT R39 R41	0603	DALE CRCW0603122J
33873P5112	RES 51.1K 1% 1/16W SMT R4 R5	0603	DALE CRCW06035112F
33872P000	RES 0 OHM 5% 1/16 W R81	SMT 0603	DALE CRCW0603000J

## PARTS LISTS

Table 5.6. Processor I/O PCB Subassembly ASC/2S-2000 (34250G2) (Page 4 of 6)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
33711P000	RES ZERO OHM JUMPER SMT R43 R60	THICK FILM 1206	KOA SPEER RM73Z2BT
33873P6813	RES 681K 1% 1/16W SMT R49	0603	DALE CRCW06036813F
33713P222	RES 2.2K 5% 1/2W SMT R56	THICK FILM 2010	DALE CRCW2010222J
33875P241	RES 240 5% 1W SMT R57 R58	2512	DALE CRCW2512241J
33872P753	RES 75K 5% 1/16W SMT R63	0603	DALE CRCW0603753J
33872P183	RES 18K 5% 1/16W SMT R64	0603	DALE CRCW0603183J
43654P2	RES 2.2 OHMS 5W R65 R67	WIRE WOUND	OHMITE 95J2R2
33872P152	RES 1.5K 5% 1/16W SMT R68 R70 R71 R73	0603	DALE CRCW0603152J
33872P121	RES 120 5% 1/16W SMT R69 R72	0603	DALE CRCW0603121J
33873P4493	RES 499K 1% 1/16W SMT R7	0603	DALE CRCW0604993F
31263P97	RES 10K 3W 5% W/W R74 R75	REPLACES 0500-0039	DALE CW2C-14-10K 5%
33873P1003	RES 100K 1% 1/16W SMT R9 R15 R18	0603	DALE CRCW06031003F
43577P3	RES NTWK 10K COM PIN RP1 RP2 RP25 RP26 RP27 RP29 RP30 RP31 RP32 RP33 RP34	10 PIN SIP 9 RES 1W 2% REPLACES 0500-0213	BOURNS 4610X-101-103
32876P1	LOGIC LEVEL TRANS RP12 RP13 RP14 RP15 RP16 RP17 RP18 RP19 RP20 RP21 RP22 RP23 RP24	SURFACE MTG CUSTOM SO20-.300	SPRAGUE 820C110N187
43577P26	RES NTWK 10K COM PIN RP3 RP4 RP37 RP38 RP39	10 PIN 9 RES MOLDED	BOURNS 4310R-101-103
31770P1	VARISTOR 55 JOULES RV1 RV2 RV3	212V-255V METAL OXIDE UL/CSA RECOGNIZED	HARRIS V150LA20B
33859P1	IC 14538B DUAL MONOSTBL U1 U5	PRECISION SMT SO16-.150	MOTOROLA MC14538BDW
33772P2	IC LM393 U10	DUAL COMPARATOR SMT S08-.150	NATIONAL LM393M
33864P09	IC TTL LPS 74LS09 U11	QUAD 2 INPUT POS ANGATE SMT SO14-.150	MOTOROLA SN74LS09D
32878P1	IC 68302 U12	SMT PQFP-132	MOTOROLA MC68302FC16C
34245P13	IC PRGMD PER 34245 U13	GAL16V8B M/F 34290P1	SEE ENG DWG
33854P32	IC ALSMOS 74ALS32 U14	QUAD 2-INPUT POS-ORGATE SMT SO14-.150	NATIONAL DM74ALS32M
33703P04	IC ACTMOS 74ACT04 U15	HEX INVERTER SMT SO14-.150	NATIONAL 74ACT04SC
33854P08	IC ALSMOS 74ALS08 U16	QUAD 2-INPUT AND-GATE SMT SO14-.150	NATIONAL DM74ALS08M

Table 5.6. Processor I/O PCB Subassembly ASC/2S-2000 (34250G2) (Page 5 of 6)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
33863P244	IC HCTMOS 74HCT244 U17 U18 U19 U24 U39 U59	OCTAL BUFFER/LINE DRVR SMT SO20-.300	MOTOROLA MC74HCT244AD
33860P1*	IC 29F800BB FLASH 8 MB U2	SMT TSOP48	AMD AM29F800BB-90EC
33865P1	IC 88C681 U20	SMT PLCC44	PHILLIPS SCN2681TC1A44
34247P21	IC PRGMD PER 34247 U21	GAL16V8D M/F 33866P1	SEE ENG DWG
34248P22	IC PRGMD PER 34248 U22	GAL16V8D M/F 33866P1	SEE ENG DWG
33863P138	IC HCTMOS 74HCT138 U23	3 TO 8 LINE DECODE/DMUX SMT SO16-.150	MOTOROLA MC74HCT138AD
33863P245	IC HCTMOS 74HCT245 U25 U38	OCTAL BUS TRANSCVR SMT SO20-.300	MOTOROLA MC74HCT245AD
33862P259	IC HCMOS 74HC259 U31 U32 U33 U34 U35 U36 U37 U44 U45 U46 U61 U62	8 BIT ADDRESSABLE LATCH SMT SO16-.150	MOTOROLA MC74HC259D
33861P1	IC 68HC68T U3	SMT SOIC16-.300	MOTOROLA MC68HC68T1DW
33868P1	IC 2598 VOLTAGE REG U4	SMT	NATIONAL LM2598-5.0
33862P251	IC HCMOS 74HC251 U51 U52 U53 U54 U55 U56 U58 U60	1 OF 8 DATA SEL/MPLEX SMT SO16-.150	MOTOROLA MC74HC251D
33858P1	IC 128K X 8 STATIC RAM U6 U7	100 NS SMT SOL32-.500	HITACHI HM628128BLFP-10
31414P3	XSTR NTWK ULN-2803A U64 U67 U68 U69 U70 U71 U72 U73 U74 U75 U76 U77 U78	18P DIP DARLINGTON TESTED REPLD 0900-0132	SPRAGUE ULN2803A
40029P4	VOLT REG +12V U79	TO-220 1 AMP	MOTOROLA MC7812CP
33764P4	IC MAX214 U80	QUAD RS-232 XMTR/RCVR SMT SO28-.300	MAXIM MAX214CWI
33853P1	IC 490 RS-485 XMTR U81 U82	SMT SO8-.150	LINEAR TECH LTC490CS8
33851P1	IC MMBZ15VDLT1 U83 U84 U85 U86 U87 U88 U89 U90	SMT SOT23	MOTOROLA MMBZ15VDLT1
43730P2	IC MCT6 DUAL OPTO ISOL U91	8P DIP	MONSANTO MCT6
33737P3	XTAL 32.768KHZ Y1	SMT MC-405	EPSON MC-405-32.768K-A2
33737P4	XTAL 14.7456MHZ Y2	SMT MA-505	EPSON MA-505-14.745M-C2
33245P8	HEATSINK PLUG-IN TO-220 XU79		AAVID 576802B03100
32289P1	JUMPER SHORTING XJP2 XJP3 XJP4 XJP5 XJ7 XJ8		AMP 531220-2

# PARTS LISTS

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Table 5.6. Processor I/O PCB Subassembly ASC/2S-2000 (34250G2) (Page 6 of 6)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
56671P41	STNDF SWAGE #4 X .125 M2 M3	.25 DIA BRS/NI	UNICORP SS240-1-D-7
56671P4	STNDF SWAGE #4 X.469L XJ10 XJ11 XJ12	.25 DIA BRS/NI	UNICORP SS251-1-D-7
56671P42	STNDF SWAGE #4 X .250 XJ13 XJ15 XJ17	.25 DIA BRS/NI	UNICORP SS244-1-D-7
56671P25	STNDF SWAGE #2 X .38L XJ4	.16 DIA BRS/NIC	UNICORP SS130-1-D-7
N57P5006C	SCRW #2 X 3/8 PH SLT XJ4	STL CD MACH	
N404P8C	WSHR LK INT #2 STL XJ4	CAD PLATED	
33395P3	SPCR PCB LKING .38L	1/4 TURN PLASTIC	HARTWELL HNST4-375-1
53048P12	TIE CABLE .75" DIA STD	BLACK	DENNISON 08-404



**Table 5-7. Processor I/O PCB Subassembly ASC/2S-2100 (34250G3)\* (Page 1 of 6)**

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
34250	ASSEMBLY DRAWING	PROCESSOR I/O	
34251	SCHEMATIC PROCESSOR I/O		
34253	MASTER ARTWORK	PROCESSOR I/O	
34254	TEST SPEC	PROCESSOR I/O	
34252P1	PCB PROCESSOR I/O INTF	ASC/2S	
32911P21	BTRY 3V PC MTG B1	LITHIUM	PANASONIC VL2330-1VC
33748P5103	CAPAC .01MF 50V C1 C3 C4 C8 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C26 C27 C28 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C45 C46 C47 C48 C49 C50 C51 C52 C53 C54 C55 C56 C57 C58 C59 C60 C61 C62 C63 C64 C65 C70 C75	SMT 0603 10% X7R CERM	AVX 06035C103KAT2A
33740P5220	CAPAC 22PF 50V C12	SMT 0805 COG CERAM	MURATA GRM40COG220J050BD
33741P5104	CAPAC .1MF 50V C2 C11 C68	SMT 1206 10% X7R CERM	KEMET C1206C104K5RAC
33877P105	CAPAC 1MF 35V TANT C29	SMT 3528	SPRAGUE 293D105X9035B2T
33878P10	CAPAC 10MF 35V ELECT C31 C69	SMT NEMCO CASE B	NICHICON UWX1V100MCR1GB
33740P5270	CAPAC 27PF 50V C43	SMT 0805 COG CERAM	MURATA GRM40COG270J050BD
33740P5330	CAPAC 33PF 50V C44	SMT 0805 COG CERAM	MURATA GRM40COG330J050BD
31884P4	CAP VARIABLE 7-50PF C5	SMT A-TYPE	MURATA TZBX4R500BA110
32895P7	CAPAC 120MF 50V ELECT C6 C7		NICHICON UPL1H121MPH
33878P047	CAPAC 4.7MF 25V ELECT C66 C67 C71 C72 C73	SMT NEMCO CASE B	NICHICON UWX1E4R7MCR1GB
32169P19	CAPAC ELECT 18000MF 35V C76	AL SNAP MTG	NICHICON LLK1V183MHSC

\*For Parts lists 34250G1, 34250G2, and 34250G3 the following note applies.

One 8 MB of flash PROM (U2) can be replaced by installing two 4 MB flash PROMs in locations U2 and U92. The following parts must also be installed: C78, C79, C80, R82, R83 and U93.

33748P5103	CAPAC .01MF 50V C78*C79		AVX* 06035C103KAT2A
33748P5471	CAPAC 470PF 50V C80		MURATA ERIE GRM39X7R47K050B
33872P122	RES 1.2K 5% 1/16W R82*R83		DALE CRCW0603122J
33901P1	IC 29F400BB FLASH 4 MB U2*U92		AMD AM29F400BB-90EC
33902P32	IC 74VHC32 SMT S014 U93		FAIRCHILD 74VHC32MTC

# PARTS LISTS

Table 5-7. Processor I/O PCB Subassembly ASC/2S-2100 (34250G3) (Page 2 of 6)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
58064P12	DIODE 1N4763A CR24	1W ZENER	MOTOROLA 1N4763A
32416P6	DIODE BRIDGE 1A 800V CR25	4 PIN DIP	DIODES INC DB106 OR DF08
33831P4	DIODE MBR0520 20V 1/2A CR3 CR5 CR11	SCHOTTKY SMT CASE 403	MOTOROLA MBR0520LT1
33831P3	DIODE MRB340 34V CR4 CR6 CR7 CR8 CR10	SCHOTTKY SMT CASE 403	MOTOROLA MBRS340TS
58873P29	DIODE 1N5232B 5.6V 5% CR9	500MW ZENER REPLACES 58052P6	MOTOROLA 1N5232B
55205P17	FUSE 3/4A 250V 3AG S/B F1	1.25 X .25	LITTELFUSE 313.750
55205P19	FUSE 1A 250V 3AG S/B 3 F2	1.25X.25	LITTELFUSE 313001
32183P4	FUSE HLDR W/CARRIER XF1 XF2	SOLDER TERM	SCHURTER FEU031.1659
31912P1	SPCR NYL .50ID X.76OD XF1 XF2	.18 THK 3 AG F/HLDR	SEASTROM 5606-44-177
57255P700	WIRE 22AWG BLK 19 STRD XF1 XF2	TYPE B/N 600V	SEE ENG SPEC
32758P1	INDUCTOR FERRITE BEAD FB1 FB2 FB3 FB4		TDK BF45-4002
31058P4	CONN CIRC 61S BOX MTG J10	D/SLDR CONT MIL-C-26482	CANNON KPT02E24-61S SPCL
31058P3	CONN CIRC 55S BOX MTG J11	D/SLDR CONT MIL-C-26482	CANNON KPT02E2255S SPCL
31058P2	CONN CIRC 55P BOX MTG J12	D/SLDR CONT MIL-C-26482	CANNON KPT02E22-55PDV
31369P27	CONN D SUB 25S W/W J13	METAL SHELL	CINCH DBKL-25SUT
31369P28	CONN D SUB 25P W/W J14	METAL SHELL	CINCH DBKL-25PUTI
31369P26	CONN D SUB 15S W/W J15	METAL SHELL	CINCH DAKL-15SUT
31369P25	CONN D SUB 9P J17	METAL SHELL	CINCH DEKL-09PUTI
58751P32	HDR 3 CKT LKG STRGHT J18	.156 CTRS W/LOCK GOLD	MOLEX 26-61-4030
58751P14	WAFER POLARIZING 5 CKT J19	.156 CTRS W/LOCK	AMP 640388-5
33852P68	CONN 68 PIN STRAIGHT J2	.050 PITCH	MOLEX 15-92-1468
32158P113	HDR 13/26 CTR POL STR J3	.100 CTRS W/SHORT LATCH	HIROSE HIF3BAG-26PA-2.54DSA
32219P1	CONN DIN 32P R/A J4	W/W .512L	PANDUIT 100-632-051
32219P8	CONN DIN 32S STR J5	A/SD	PANDUIT 100-632-432
33745P2105	CAPAC 1MF 16V C9 C10 C25	SMT 3216 20% TANT	KEMET T491A105M016AS
31769P61	TRANSORB P6KE27A CR1 CR22 CR23	25.7-28.4V	GEN INST P6KE27A
31769P59	TRANSORB P6KE6.8A CR14	600W UNIDIRECTIONAL 6.45-7.14V	MOTOROLA P6KE6.8A
31769P60	TRANSORB P6KE33A CR18 CR19	600W UNIDIRECTIONAL 31.4-34.7V	MOTOROLA P6KE33A

Table 5-7. Processor I/O PCB Subassembly ASC/2S-2100 (34250G3) (Page 3 of 6)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
31535P1	WAFER 2 CKT J7 J8 TP1 TP2 TP3	.100 CTRS	MOLEX 22-03-2021
31163P31	CONN CIRC 63P BOX MTG J9	D/SLDR CONT PLASTIC	AMP 206455-2
31535P2	WAFER 3 CKT JP2 JP3 JP4 JP5	.100 CTRS	MOLEX 22-03-2031
33879P1	INDUCTOR POWER SMT L1	DO3316	COILCRAFT DO3316P-104
56668P3	CHOKE HASH 250MH L2		JW MILLER 5254
37129P2	DIODE LED BRIGHT RED LED1		GEN INST MV5752
33730P2	XSTR 2N3904 NPN Q1	SMT SOT23 GENERAL PURPOSE	ZETEX FMMT3904-NDA
33730P1	XSTR NPN 2222A Q2 Q3	SMT SOT23	MOTOROLA MMBT2222A
33872P103	RES 10K 5% 1/16W SMT R1 R6 R8 R26 R27 R32 R40 R44 R54 R55	0603	DALE CRCW0603103J
33872P681	RES 680 5% 1/16W SMT R10	0603	DALE CRCW0603681J
33872P331	RES 330 5% 1/16W SMT R11 R16 R20 R45 R46 R48 R51 R52	0603	DALE CRCW0603331J
54719P153	RES 22 MEG 1/4W 5% R12	MIL-R-11F FIXED COMP	RC07GF226J
33872P000	RES 0 5% 1/16W SMT R13 R21 R81	0603	DALE CRCW0603000J
33873P5491	RES 5.49K 1% 1/16W SMT R14	0603	DALE CRCW06035491F
33873P1302	RES 13K 1% 1/16W SMT R17	0603	DALE CRCW06031302F
33872P472	RES 4.7K 1/16W SMT R19 R30	0603	DALE CRCW0603472J
33873P2212	RES 22.1K 1% 1/16W SMT R2	0603	DALE CRCW06032212F
33873P1002	RES 10K 1% 1/16W SMT R22 R76 R77 R78	0603	DALE CRCW06031002F
33872P105	RES 1M 5% 1/16W SMT R23 R25	0603	DALE CRCW0603105J
33872P102	RES 1K 5% 1/16W SMT R24	0603	DALE CRCW0603102J
33872P221	RES 220 5% 1/16W SMT R28	0603	DALE CRCW0603221J
33872P473	RES 47K 5% 1/16W SMT R29 R34	0603	DALE CRCW0603473J
33873P9092	RES 90.9K 1% 1/16W SMT R3	0603	DALE CRCW06039092F
54582P5	RES 15 OHMS 1/2W 5% R31	FIXED COMP	A/BRADLEY EB1505
33825P000	RES ZERO OHM JUMPER R35	THICK FILM 0805	DALE CRCW080500J
33870P1	DIODE FDLL4148 CR2 CR12 CR13 CR15 CR16 CR17 CR20 CR21	SMT D035	NATIONAL FDLL4148

# PARTS LISTS

Table 5-7. Processor I/O PCB Subassembly ASC/2S-2100 (34250G3) (Page 4 of 6)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
33872P271	RES 270 5% 1/16W SMT R36	0603	DALE CRCW063271J
33872P101	RES 100 5% 1/16W SMT R37 R42 R47	0603	DALE CRCW0603101J
33872P112	RES 1.1K 5% 1/16W SMT R38	0603	DALE CRCW0603112J
33872P122	RES 1.2K 5% 1/16W SMT R39 R41	0603	DALE CRCW0603122J
33873P5112	RES 51.1K 1% 1/16W SMT R4 R5	0603	DALE CRCW06035112F
33711P000	RES ZERO OHM JUMPER SMT R43 R60	THICK FILM 1206	KOA SPEER RM73Z2BT
33873P6813	RES 681K 1% 1/16W SMT R49	0603	DALE CRCW06036813F
33713P222	RES 2.2K 5% 1/2W SMT R56	THICK FILM 2010	DALE CRCW2010222J
33875P241	RES 240 5% 1W SMT R57 R58	2512	DALE CRCW2512241J
33872P222	RES 2.2K 5% 1/16W SMT R61	0603	DALE CRCW0603222J
33875P102	RES 1K 5% 1W SMT R62	2512	DALE CRCW2512102J
33872P753	RES 75K 5% 1/16W SMT R63	0603	DALE CRCW0603753J
33872P183	RES 18K 5% 1/16W SMT R64	0603	DALE CRCW0603183J
43654P2	RES 2.2 OHMS 5W R65 R67	WIRE WOUND	OHMITE 95J2R2
33872P152	RES 1.5K 5% 1/16W SMT R68 R70 R71 R73	0603	DALE CRCW0603152J
33872P121	RES 120 5% 1/16W SMT R69 R72	0603	DALE CRCW0603121J
33873P4993	RES 499K 1% 1/16W SMT R7	0603	DALE CRCW06034993F
31263P97	RES 10K 3W 5% W/W R74 R75	REPLACES 0500-0039	DALE CW2C-14-10K 5%
33873P1003	RES 100K 1% 1/16W SMT R9 R15 R18	0603	DALE CRCW06031003F
43577P3	RES NTWK 10K COM PIN RP1 RP2 RP5 RP6 RP7 RP8 RP9 RP10 RP11 RP25 RP26 RP27 RP28 RP29 RP30 RP31 RP32 RP33 RP34	10 PIN SIP 9 RES 1W 2% REPLACES 0500-0213	BOURNS 4610X-101-103
32876P1	LOGIC LEVEL TRANS RP12 RP13 RP14 RP15 RP16 RP17 RP18 RP19 RP20 RP21 RP22 RP23 RP24 RP35 RP36	SURFACE MTG CUSTOM SO20-.300	SPRAGUE 820C110N187
43577P26	RES NTWK 10K COM PIN RP3 RP4 RP37 RP38 RP39	10 PIN 9 RES MOLDED	BOURNS 4310R-101-103
31770P1	VARISTOR 55 JOULES RV1 RV2 RV3	212V-255V METAL OXIDE UL/CSA RECOGNIZED	HARRIS V150LA20B

Table 5-7. Processor I/O PCB Subassembly ASC/2S-2100 (34250G3) (Page 5 of 6)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
33859P1	IC 14538B DUAL MONOSTBL U1 U5	PRECISION SMT SO16-.150	MOTOROLA MC14538BDW
33772P2	IC LM393 U10	DUAL COMPARATOR SMT S08-.150	NATIONAL LM393M
33864P09	IC TTL LPS 74LS09 U11	QUAD 2 INPUT POS ANGATE SMT SO14-.150	MOTOROLA SN74LS09D
32878P1	IC 68302 U12	SMT PQFP-132	MOTOROLA MC68302FC16C
34245P13	IC PRGMD PER 34245 U13	GAL16V8B M/F 34290P1	SEE ENG DWG
33854P32	IC ALSMOS 74ALS32 U14	QUAD 2-INPUT POS-ORGATE SMT SO14-.150	NATIONAL DM74ALS32M
33703P04	IC ACTMOS 74ACT04 U15	HEX INVERTER SMT SO14-.150	NATIONAL 74ACT04SC
33854P08	IC ALSMOS 74ALS08 U16	QUAD 2-INPUT AND-GATE SMT SO14-.150	NATIONAL DM74ALS08M
33863P244	IC HCTMOS 74HCT244 U17 U18 U19 U24 U30 U39 U57 U59	OCTAL BUFFER/LINE DRVR SMT SO20-.300	MOTOROLA MC74HCT244AD
33860P1*	IC 29F800BB FLASH 8 MB U2	SMT TSOP48	AMD AM29F800BB-90EC
33865P1	IC 88C681 U20	SMT PLCC44	PHILLIPS SCN2681TC1A44
34247P21	IC PRGMD PER 34247 U21	GAL16V8D M/F 33866P1	SEE ENG DWG
34248P22	IC PRGMD PER 34248 U22	GAL16V8D M/F 33866P1	SEE ENG DWG
33863P138	IC HCTMOS 74HCT138 U23	3 TO 8 LINE DECODE/DMUX SMT SO16-.150	MOTOROLA MC74HCT138AD
33863P245	IC HCTMOS 74HCT245 U25 U38	OCTAL BUS TRANSCVR SMT SO20-.300	MOTOROLA MC74HCT245AD
33862P259	IC HCMOS 74HC259 U26 U27 U28 U29 U31 U32 U33 U34 U35 U36 U37 U44 U45 U46 U61 U62	8 BIT ADDRESSABLE LATCH SMT SO16-.150	MOTOROLA MC74HC259D
33861P1	IC 68HC68T U3	SMT SOIC16-.300	MOTOROLA MC68HC68T1DW
33868P1	IC 2598 VOLTAGE REG U4	SMT	NATIONAL LM2598-5.0
33862P251	IC HCMOS 74HC251 U40 U41 U42 U43 U47 U48 U49 U50 U51 U52 U53 U54 U55 U56 U58 U60	1 OF 8 DATA SEL/MPLEX SMT SO16-.150	MOTOROLA MC74HC251D
33858P1	IC 128K X 8 STATIC RAM U6 U7	100 NS SMT SOL32-.500	HITACHI HM628128BLFP-10
31414P3	XSTR NTWK ULN-2803A U63 U64 U65 U66 U67 U68 U69 U70 U71 U72 U73 U74 U75 U76 U77 U78	18P DIP DARLINGTON TESTED REPLD 0900-0132	SPRAGUE ULN2803A
40029P4	VOLT REG +12V U79	TO-220 1 AMP	MOTOROLA MC7812CP

# PARTS LISTS

Table 5-7. Processor I/O PCB Subassembly ASC/2S-2100 (34250G3) (Page 6 of 6)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
33764P4	IC MAX214 U80	QUAD RS-232 XMTR/RCVR SMT SO28-.300	MAXIM MAX214CWI
33853P1	IC 490 RS-485 XMTR U81 U82	SMT SO8-.150	LINEAR TECH LTC490CS8
33851P1	IC MMBZ15VDLT1 U83 U84 U85 U86 U87 U88 U89 U90	SMT SOT23	MOTOROLA MMBZ15VDLT1
43730P2	IC MCT6 DUAL OPTO ISOL U91	8P DIP	MONSANTO MCT6
33737P3	XTAL 32.768KHZ Y1	SMT MC-405	EPSON MC-405-32.768K-A2
33737P4	XTAL 14.7456MHZ Y2	SMT MA-505	EPSON MA-505-14.745M-C2
33245P8	HEATSINK PLUG-IN TO-220 XU79		AAVID 576802B03100
32289P1	JUMPER SHORTING XJP2 XJP3 XJP4 XJP5 XJ7 XJ8		AMP 531220-2
56671P41	STNDF SWAGE #4 X .125 M2 M3	.25 DIA BRS/NI	UNICORP SS240-1-D-7
56671P4	STNDF SWAGE #4 X.469L XJ10 XJ11 XJ12	.25 DIA BRS/NI	UNICORP SS251-1-D-7
56671P42	STNDF SWAGE #4 X .250 XJ13 XJ14 XJ15 XJ17	.25 DIA BRS/NI	UNICORP SS244-1-D-7
56671P25	STNDF SWAGE #2 X .38L XJ4	.16 DIA BRS/NIC	UNICORP SS130-1-D-7
56671P37	STNDF SWAGE #6 X .406 XJ9	.25 DIA BRS/NI	UNICORP SS359-1-D-7
N57P5006C	SCRW #2 X 3/8 PH SLT XJ4	STL CD MACH	
N404P8C	WSHR LK INT #2 STL XJ4	CAD PLATED	
33395P3	SPCR PCB LKING .38L	1/4 TURN PLASTIC	HARTWELL HNST4-375-1
53048P12	TIE CABLE .75" DIA STD	BLACK	DENNISON 08-404

Table 5-8. Processor I/O PCB Subassembly ASC/2S-2100 Exp W/Olap (34250G4)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
34250G3 56157P6	PCA PROCESSOR I/O CONN E/CARD 22/44 J6	CONTROLLER TYPE 2 EXP .156 CTR R/ANGLE	MICROPLASTICS MP0156-22-DW8R(.375)
56157P101	KEY XJ6	USE W/56157P5, P6	MICROPLASTICS 04-0004-000
N57P9012C	SCREW #4 X 3/4 PH S XJ6	STL CD MACH	
58229P3	SPCR .25D X .25L XJ6	.140 DIA THRU AL	AMATOM 9224-A140-10
N238P9B	HEX NUT/LK WSHR #4 XJ6		

Table 5-9. Telemetry PCB Assembly (34090G1) (page 1 of 4)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
34092P1	PCB TELEM 2 & 4 WIRE	ASC/2	
56829P4	HNDLE PCB 1.25L HDW MTG		BIVAR CP-3
54552P5	RIVET 3/32 X .34L O/HD	AL POP	CHEERRY AAP-34
N402P3C	WSHR FL #2 NAR STL	CAD PLATED	
56182P25	RES 10 OHM 2W 5% W/W		IRC SPH-10-5%
	R1 R3 R28 R29		
54719P37	RES 330 OHM 1/4W 5%	MIL-R-11F FIXED COMP	
	R9 R31		RC07GF331J
54719P41	RES 470 OHM 1/4W 5%	MIL-R-11F FIXED COMP	
	R60 R61 R62 R63		RC07GF471J
54719P49	RES 1K 1/4W 5%	MIL-R-11F FIXED COMP	
	R10		RC07GF102J
54719P59	RES 2.7K 1/4W 5%	MIL-R-11F FIXED COMP	
	R32 R33		RC07GF272J
54719P65	RES 4.7K 1/4W 5%	MIL-R-11F FIXED COMP	
	R27		RC07GF472J
54719P73	RES 10K 1/4W 5%	MIL-R-11F FIXED COMP	
	R8 R12 R14 R15		RC07GF103J
	R37 R45 R46		
54719P82	RES 24K 1/4W 5%	MIL-R-11F FIXED COMP	
	R59		RC07GF243J
31489P126	RES 200 OHM 1/8W 1%		
	R7		MF55C2000F
31489P163	RES 487 OHM 1/8W 1%		
	R18		MF55C4870F
57250P16	WIRE 22AWG SOLID	BUS TINNED MIL-W-3861/1	
	XR58	TYPE S, QQ-W-343, ASTM-B3	SEE ENG SPEC
31489P209	RES 1.47K 1/8W 1%		
	R48		MF55C1471F
31489P213	RES 1.62KOHM 1/8W 1%		
	R36		MF55C1621F
31489P222	RES 2K OHM 1/8W 1%		
	R47		MF55C2001F
31489P234	RES 2.67KOHM 1/8W 1%		
	R39		MF55C2671F
31489P261	RES 5.11K OHM 1/8W 1%		
	R19 R30		MF55C5111F
31489P265	RES 5.62K OHM 1/8W 1%		
	R67		MF55C5621F
31489P274	RES 6.98K OHM 1/8W 1%		
	R65		MF55C6981F
31489P331	RES 27.4K OHM 1/8W 1%		
	R21		MF55C2742F
31489P307	RES 15.4K OHM 1/8W 1%		
	R68		MF55C1542F
31489P289	RES 10K OHM 1/8W 1%		
	R38		MF55C1002F
31489P296	RES 11.8K OHM 1/8W 1%		
	R64		MF55C1182F
31489P302	RES 13.7K OHM 1/8W 1%		
	R55		MF55C1372F



# PARTS LISTS

Table 5-9. Telemetry PCB Assembly (34090G1) (page 2 of 4)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
31489P306	RES 15K OHM 1/8W 1% R2 R5 R11 R43		MF55C1502F
31489P311	RES 16.9K OHM 1/8W 1% R56		MF55C1692F
31489P316	RES 19.1K OHM 1/8W 1% R50		MF55C1912F
31489P321	RES 21.5K OHM 1/8W 1% R41		MF55C2152F
31489P336	RES 30.9K 1/8W 1% R49		MF55C3092F
31489P337	RES 31.6K 1/8W 1% R4 R17		MF55C3162F
31489P361	RES 56.2K OHM 1/8W 1% R16		MF55C5622F
31489P364	RES 60.4K OHM 1/8W 1% R34		MF55C6042F
31489P373	RES 75K OHM 1/8W 1% R42		MF55C7502F
31489P385	RES 100K OHM 1/8W 1% R51		MF55C1003F
31489P389	RES 110K 1/8W 1% R13		MF55C1103F
31489P400	RES 143K OHM 1/8W 1% R66		MF55C1433F
31489P405	RES 162K 1/8W 1% R6		MF55C1623F
31489P434	RES 475K OHM 1/8W 1% R44		MF55C4753F
31489P435	RES 511K 1/8W 1% R57		MF55C5113F
31489P454	RES 806K OHMS 1/8W 1% R26		MF55C8063F
31489P353	RES 46.4K 1/8W 1% R40		MF55C4642F
31489P258	RES 4.75K OHM 1/8W 1% R52 R53		MF55C4751F
31489P275	RES 7.15K OHM 1/8W 1% R54		MF55C7151F
58454P34	CAPAC CERM .015MF 50V C27	5% COG	MURATA RPE113COG153J50V
58454P35	CAPAC CERM .0022MF 50V C31	5% COG	MURATA RPE121COG222J50V
58454P36	CAPAC CERM .022MF 50V C21 C24	5% COG	MURATA RPE114COG223J50V
58454P37	CAPAC CERM .0068MF 50V C11	5% COG	MURATA RPE113COG68250V
58454P38	CAPAC CERM .1MF 50V C23	10% X7R	MURATA RPE122X7R104K50V
58454P39	CAPAC CERM .22MF 50V C16 C30	10% XR7	MURATA RPE113X7R224K50V
58454P40	CAPAC CERM .047MF 50V C13	10% X7R	MURATA RPE122X7R473K50V
58454P1	CAPAC CERM .1MF 50V C10 C15 C25 C26	20%	MURATA ERIE RPE122Z54104M50V

Table 5-9 Telemetry PCB Assembly (34090G1) (page 3 of 4)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
32082P2	CAPAC TANT 2.2MF 20V C1 C2 C3 C4 C12	10% REPLACES 0400-0097	SPRAGUE 199D225X9025AE3
58873P1	DIODE 1N5233B 6V 5% CR1 CR2 CR3 CR4	500MW ZENER	MOTOROLA 1N5233B
33214P1	DIODE LED RED DS1 DS2 DS3 DS4	DIFFUSED T-1 3/4 HIGH EFFICIENCY	HP HLMP-3301
58053P2	DIODE 1N4148 CR6 CR7		NATL 1N4148
31626P2	DIODE 1N5817 20V CR5	RECT SCHOTTKY PWR	MOTOROLA 1N5817
32219P16	CONN DIN 32S RA J1	W/BOARD LOCKS	PANDUIT 130-632-533B
31535P1	WAFER 2 CKT JP8 JP9 TP1	.100 CTRS	MOLEX 22-03-2021
31535P2	WAFER 3 CKT JP1 JP2 JP3 JP4 JP5 JP6 JP7	.100 CTRS	MOLEX 22-03-2031
32099P1	XSTR NPN 2N2222 Q1 Q2		MOTOROLA 2N2222
31872P1	THERMISTOR NTC 10K RT1		KETEMA 1DC103H-EC-24
40057P10	VARISTOR 3 JOULES RV1 RV2	14CV-18V METAL OXIDE	PANASONIC ERZ-C14DK180
58874P9	POTEN 50K .5W 10% CRMT R20 R22 R23 R24	25 TRN PC MTG	BOURNS 3299W-1-503
58874P16	POTEN 10K .5W 10% CRMT R25	25 TRN PC MTG	BOURNS 3299W-1-103
58583P2	XFMR TELE COUPLING T1		PREMIER MAGNETICS TSD-544
58583P3	XFMR ISOLATION T2		PREMIER MAG TSD-545
31397P1	IC LM339 VOLT COMP QUAD U7		MOTOROLA LM339P
31495P1	IC XR2206 MONO FUNC GEN U3		EXAR XR2206CP
31495P2	IC XR2211 FSK DEMOD U8		EXAR XR2211P
31938P3	IC OP-AMP-QUAD 324 U9	LOW POWER	MOTOROLA LM324N
31938P1	IC OP AMP 741 U6	8P DIP	MOTOROLA MC1741CP1
32529P125	IC HCMOS 74HC125 U1	QUAD BUS BUFFER W/ 3 STATE OUTPUTS	TEXAS INST SN74HC125N
32529P4051	IC HCMOS 74HC4051 U2	8-CHANNEL ANALOG MULTI- PLEXER/DEMUTIPLEXER	MOTOROLA MC74HC4051AN
43730P2	IC MCT6 DUAL OPTO ISOL U4 U5	8P DIP	MONSANTO MCT6
58454P33	CAPAC CERM .01MF 50V C18 C19 C20 C22 C28 C29 C32 C33	5% COG	MURATA RPE113COG103J50V
58454P3	CAPAC CERM .01MF 50V C5 C6 C7 C8 C9 C14 C17	20%	SPRAGUE 1C10ZU103M050B

## PARTS LISTS

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Table 5-9 Telemetry PCB Assembly (34090G1) (page 4 of 4)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
31913P2	VOLT REG +9V U11	T0-92	NATIONAL LM78L09ACZ
32289P1	JUMPER SHORTING		AMP 390088-2

Table 5-10. RS-232 Telemetry PCB Assembly (33525G1) (Page 1 of 1)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
33527P1	PWB CAB RS232 TEL INTF	ASC/2	
32082P18	CAPAC TANT 10MF 35V C1 C2 C3	10% DIPPED RADIAL	SEE ENG SPEC SPRAGUE 199D106X9035BE2
58454P3	CAPAC CERM .01MF 50V C4 C5 C6	20%	SPRAGUE 1C10ZU103M050B
44076P12	CAPAC CERM 47PF 200V C7 C9 C10 C11 C12 C13	10%	CK05BX470K
58053P2	DIODE 1N4148 CR1 CR2 CR3 CR5	REPLACES 0600-0026	NATL 1N4148
33214P1	DIODE LED RED DS1 DS2 DS3	DIFFUSED T-1 3/4 HIGH EFFICIENCY	HP HLMP-3301
32099P1	XSTR NPN 2N2222 Q1		MOTOROLA 2N2222
54719P41	RES 470 OHM 1/4W 5% R2 R3 R4 R5	MIL-R-11F FIXED COMP	RC07GF471J
31283P105	IC TTL 1488 U1	QUAD LINE DRVR	NATIONAL DS1488N
31283P106	IC TTL 1489 U2	QUAD LINE RCVR	NATIONAL DS1489N
32219P16	CONN DIN 32S R/A J1	W/BD LK 2 PER	PANDUIT 100-632-533B
32740P1	SWITCH 6PDT SW1	PC DIP	ALCO ASF62
31535P2	WAFER 3 CKT JP1 JP2 JP3 JP4	.100 CTRS	MOLEX 22-03-2031
56829P4	HNDLE PCB 1.25L HDW MTG		BIVAR CP-3
54552P5	RIVET 3/32 X .34L O/HD	AL POP REPLACES 40418P100	CHERRY AAP-34
N402P3C 32289P1	WSHR FL #2 NAR STL JUMPER SHORTING	CAD PLATED	AMP 390088-2
54719P90	RES 51K 1/4W 5% R1 R7 R8	MIL-R-11F FIXED COMP	RC07GF513J
54719P57	RES 2.2K 1/4W 5% R6	MIL-R-11F FIXED COMP	RC07GF222J

# PARTS LISTS

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Table 5-11. Data Module PCB Assembly (32845G2) (Page 1 of 1)

ECONOLITE P/N	PRIMARY DESC/REF DESGN	SECONDARY DESCRIPTION	MFGR/PART#
32847P1	PCB DATA MOD ASC/2	C/SD C32846S 32848AW	SEE ENG SPEC
32082P1	CAPAC TANT 1MF 35V C1	10% DIPPED RADIAL	SPRAGUE 199D105X9035AE3
58454P3	CAPAC CERM .01MF 50V C2	20%	SPRAGUE 1C10ZU103M050B
32219P7	CONN DIN 32P STR DMP6	A/SD	PANDUIT 100-632-133
32849P1	IC EEPROM 28C256 U1	256K X 8 BIT ELECTRIC ERASABLE PROM 90-200NS	ATMEL AT28C256-20PC
31260P5	SOCKET 28P IC MACH CONT XU1	AUTO INSERT	ROB NUGENT ICE-286-SD2-TG

## SCHEMATICS AND ASSEMBLY DRAWINGS

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Schematics and assembly drawings for the controller are listed below in the order that they appear in this section. These are subject to revision due to design changes made after the revision date of this manual. Contact Econolite if revised drawings are required.

### Schematic Number

34251  
34091  
33526  
32846

### Description

Processor I/O Module  
Telemetry Module  
RS-232 Telemetry  
Data Module

### Drawing Number

34240  
34250  
34280  
34090  
33525  
32845

### Description

ASC/2S Controller  
Processor I/O Interface  
Power Supply  
Telemetry Module  
RS-232 Telemetry Interface  
Data Module

## APPENDIX A TERMINAL CABLE DIAGRAMS

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The ASC/2S has the capability to switch between Data Communication Equipment (DCE) and Data Terminal Equipment (DTE) operation. To talk directly to a Personal Computer with a standard cable, the controller should be set into the DCE mode. This makes the controller appear to the PC as a modem. When attaching a serial printer or modem to the controller, set the controller to the DTE mode. When connecting two controllers together for data transfer, set one controller to DTE and the other to DCE.

The controller is switched between mode via either jumper **JP4** [34251,7,2,B] or through the user interface on the PORT 2 configuration screen. Set JP4 to the left hand position for DCE mode and the right hand position for DTE mode.

The Terminal port uses the XON / XOFF protocol for device to device handshaking. In addition to correct cable and jumper connections, the TERMINAL PORT page of the CONFIGURATION submenu must be correctly programmed before data transfer occurs.

The following NULL MODEM cable diagrams are provided for reference only. The cables are constructed to mate with the terminal interface on the I/O Interface modules.

Figures A-1 and A-2 represent configurations for ASC/2 to ASC/2 communication. Figure A-2 illustrates the minimum cable for both controller to controller and controller to printer communication. Figure A-3 illustrates the minimum cable to attach an ASC/2 to a laptop with a DB-9 connector.

### CONTROLLER TO CONTROLLER CABLE DIAGRAM

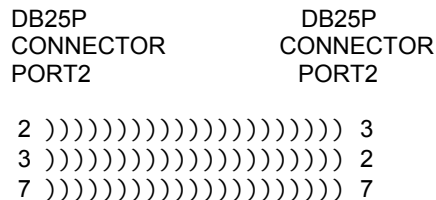


FIGURE A-1

### CONTROLLER TO CONTROLLER CABLE DIAGRAM (MINIMUM CABLE)

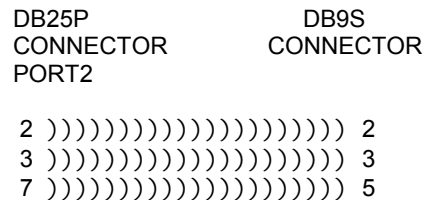


FIGURE A-2





## APPENDIX B

### PIN LISTS/INTERFACE CONNECTORS

#### CONNECTOR A

55 Pin (Plug) Type #22-55P

PIN	FUNCTION	I/O
A	Fault Monitor	[O]
B	+24 VDC External	[O]
C	Voltage Monitor	[O]
D	N1 Red	[O]
E	N1 Don't Walk	[O]
F	N2 Red	[O]
G	N2 Don't Walk	[O]
H	N2 Ped Clear	[O]
J	N2 Walk	[O]
K	Vehicle Detector 2	[I]
L	Ped Detector 2	[I]
M	N2 Hold	[I]
N	Stop Time (Ring 1)	[I]
P	Inhibit Max Term (Ring 1)	[I]
R	External Start	[I]
S	Interval Advance	[I]
T	Indicator Lamp Control	[I]
U	AC-Common	[I]
V	Chassis Ground	[I]
W	Logic Ground	[O]
X	Flashing Logic Out	[O]
Y	Status Bit C (Ring1)	[O]
Z	N1 Yellow	[O]
a	N1 Ped Clear	[O]
b	N2 Yellow	[O]
c	N2 Green	[O]
d	N2 Check	[O]
e	N2 Phase On	[O]
f	Vehicle Detector 1	[I]
g	Ped Detector 1	[I]
h	N1 Hold	[I]
i	Force-Off (Ring 1)	[I]
j	Ext Min Recall	[I]
k	Manual Control Enable	[I]
m	Call To Non Actuated I	[I]
n	Test A	[I]
p	AC+ (Control)	[I]
q	I/O Mode Bit A	[I]
r	Status Bit B (Ring 1)	[O]
s	N1 Green	[O]
t	N1 Walk	[O]
u	N1 Check	[O]
v	N2 Ped Omit	[I]
w	Omit All Red Clear (Ring1)	[I]
x	Red Rest (Ring 1)	[I]
y	I/O Mode Bit B	[I]
z	Call To Non Actuated II	[I]
AA	Test B	[I]
BB	Walk Rest Modifier	[I]
CC	Status Bit A (Ring 1)	[O]
DD	N1 Phase On	[O]
EE	N1 Ped Omit	[I]
FF	Ped Recycle (Ring 1)	[I]
GG	Max II Selection (Ring 1)	[I]
HH	I/O Mode Bit C	[I]

#### CONNECTOR B

55 Pin (Socket) Type #22-55S

PIN	FUNCTION	I/O
A	N1 Phase Next	[O]
B	Preempt 2 Detector	[I]
C	N2 Phase Next	[O]
D	N3 Green	[O]
E	N3 Yellow	[O]
F	N3 Red	[O]
G	N4 Red	[O]
H	N4 Ped Clear	[O]
J	N4 Don't Walk	[O]
K	N4 Check	[O]
L	Vehicle Detector 4	[I]
M	Ped Detector 4	[I]
N	Vehicle Detector 3	[I]
P	Ped Detector 3	[I]
R	N3 Phase Omit	[I]
S	N2 Phase Omit	[I]
T	N5 Ped Omit	[I]
U	N1 Phase Omit	[I]
V	Ped Recycle (Ring 2)	[I]
W	Preempt 4 Detector	[I]
X	Preempt 5 Detector	[I]
Y	N3 Walk	[O]
Z	N3 Ped Clear	[O]
a	N3 Don't Walk	[O]
b	N4 Green	[O]
c	N4 Yellow	[O]
d	N4 Walk	[O]
e	N4 Phase On	[O]
f	N4 Phase Next	[O]
g	N4 Phase Omit	[I]
h	N4 Hold	[I]
i	N3 Hold	[I]
j	N3 Ped Omit	[I]
k	N6 Ped Omit	[I]
m	N7 Ped Omit	[I]
n	N8 Ped Omit	[I]
p	Overlap A Yellow	[O]
q	Overlap A Red	[O]
r	N3 Check	[O]
s	N3 Phase On	[O]
t	N3 Phase Next	[O]
u	Overlap D Red	[O]
v	Preempt 6 Detector	[I]
w	Overlap D Green	[O]
x	N4 Ped Omit	[I]
y	Free (No Coord)	[I]
z	Max II Selection (Ring 2)	[I]
AA	Overlap A Green	[O]
BB	Overlap B Yellow	[O]
CC	Overlap B Red	[O]
DD	Overlap C Red	[O]
EE	Overlap D Yellow	[O]
FF	Overlap C Green	[O]
GG	Overlap B Green	[O]
HH	Overlap C Yellow	[O]

#### CONNECTOR C

61 Pin (Socket) Type #24-61S

PIN	FUNCTION
A	Status Bit A (Ring 2)
B	Status Bit B (Ring 2)
C	N8 Don't Walk
D	N8 Red
E	N7 Yellow
F	N7 Red
G	N6 Red
H	N5 Red
J	N5 Yellow
K	N5 Ped Clear
L	N5 Don't Walk
M	N5 Phase Next
N	N5 Phase On
P	Vehicle Detector 5
R	Ped Detector 5
S	Vehicle Detector 6
T	Ped Detector 6
U	Ped Detector 7
V	Vehicle Detector 7
W	Ped Detector 8
X	N8 Hold Off
Y	Force-Off (Ring 2)
Z	Stop Time (Ring 2)
a	Inhibit Max Term (Ring 2)
b	Test C
c	Status Bit C (Ring 2)
d	N8 Walk
e	N8 Yellow
f	N7 Green
g	N6 Green
h	N6 Yellow
i	N5 Green
j	N5 Walk
k	N5 Check
m	N5 Hold
n	N5 Phase Omit
p	N6 Hold
q	N6 Phase Omit
r	N7 Phase Omit
s	N8 Phase Omit
t	Vehicle Detector 8
u	Red Rest Mode (Ring 2)
v	Omit Red Clear (Ring 2)
w	N8 Ped Clear
x	N8 Green
y	N7 Don't Walk
z	N6 Don't Walk
AA	N6 Ped Clear
BB	N6 Check
CC	N6 Phase On
DD	N6 Phase Next
EE	N7 Hold
FF	N8 Check
GG	N8 Phase On
HH	N8 Phase Next
JJ	N7 Walk
KK	N7 Ped Clear
LL	N6 Walk
MM	N7 Check
NN	N7 Phase On
PP	N7 Phase Next

# APPENDIX B

## PIN LISTS/INTERFACE CONNECTORS

---

### CONNECTOR D

PIN	FUNCTION
25	SYSTEM COMMAND CYCLE BIT 1 INPUT
35	SYSTEM COMMAND CYCLE BIT 2 INPUT
6	SYSTEM COMMAND CYCLE BIT 3 INPUT
12	SYSTEM COMMAND OFFSET BIT 1 INPUT/ EXTERNAL ADDRESS BIT 0
10	SYSTEM COMMAND OFFSET BIT 2 INPUT/ EXTERNAL ADDRESS BIT 1
36	SYSTEM COMMAND OFFSET BIT 3 INPUT/ EXTERNAL ADDRESS BIT 2
16	SYSTEM COMMAND SPLIT BIT 1 INPUT/ EXTERNAL ADDRESS BIT 3
9	SYSTEM COMMAND SPLIT BIT 2 INPUT/ EXTERNAL ADDRESS BIT 4
4	SYSTEM COMMAND COORD SYNC INPUT
26	COORD FREE
60	REMOTE FLASH
3	SPLIT DEMAND
38	DUAL COORD
14	TIME RESET
20	TEST INPUT C
37	TEST INPUT D
19	TEST INPUT E
57	PREEMPTOR CALL #1
49	PREEMPTOR CALL #2
50	PREEMPTOR CALL #3/BUS PREEMPTOR #1
55	PREEMPTOR CALL #4/BUS PREEMPTOR #2
56	PREEMPTOR CALL #5/BUS PREEMPTOR #3
61	PREEMPTOR CALL #6/BUS PREEMPTOR #4
58	CMU STOP TIME (CONFLICT FLASH)
17	EXPANDED DETECTOR #1
47	EXPANDED DETECTOR #2
31	EXPANDED DETECTOR #3
18	EXPANDED DETECTOR #4
30	EXPANDED DETECTOR #5
39	EXPANDED DETECTOR #6
40	EXPANDED DETECTOR #7
13	EXPANDED DETECTOR #8

### PIN FUNCTION

43	SYSTEM COMMAND CYCLE BIT 1 OUTPUT
44	SYSTEM COMMAND CYCLE BIT 2 OUTPUT
29	SYSTEM COMMAND CYCLE BIT 3 OUTPUT
33	SYSTEM COMMAND OFFSET BIT 1 OUTPUT
42	SYSTEM COMMAND OFFSET BIT 2 OUTPUT
2	SYSTEM COMMAND OFFSET BIT 3 OUTPUT
21	SYSTEM COMMAND SPLIT BIT 1 OUTPUT
46	SYSTEM COMMAND SPLIT BIT 2 OUTPUT
53	SYSTEM COMMAND SYNC OUT
23	PREEMPTOR #1 ACTIVE
32	PREEMPTOR #2 ACTIVE
22	PREEMPTOR #3 ACTIVE
34	PREEMPTOR #4 ACTIVE
1	PREEMPTOR #5 ACTIVE
48	PREEMPTOR #6 ACTIVE
59	PREEMPT CMU INTERLOCK (1K PULL UP)
27	COORD STATUS
5	CROSS STREET SYNC
28	NIC SPECIAL FUNCTION 1
8	NIC SPECIAL FUNCTION 2
24	NIC SPECIAL FUNCTION 3/ SPARE OUTPUT 1
11	NIC SPECIAL FUNCTION 4/ SPARE OUTPUT 2
15	PREEMPTOR FLASH CONTROL
41	SPARE OUTPUT 4
45	SPARE OUTPUT 5
51	SPARE OUTPUT 6
52	SPARE OUTPUT 7
54	SPARE OUTPUT 8

### NOTE

Priority preemptors 1 & 2 will respond to any NEMA defined input that is applied to Preemptor Call input 1 & 2, respectively.

Priority preemptors 3-6 will respond to any NEMA defined input that is applied for at least 0.8 seconds to Preemptor Call inputs 3-6, respectively.

Bus Preemptors 1-4 will respond to a pulsing (1 pps at 50% duty cycle) NEMA defined input that is applied to Preemptor Call input 3-6, respectively.

# APPENDIX B PIN LISTS

## PORTS 1, 2, 3 / TYPE 1 POWER

### PORT 1 SDLC

PIN	FUNCTION
1	Tx Data +
2	Logic Ground
3	Tx Clock +
4	Logic Ground
5	Rx Data +
6	Logic Ground
7	Rx Clock +
8	Logic Ground
9	Tx Data -
10	Port 1 Disable (0VDC=disable)
11	Tx Clock -
12	Chassis Ground
13	Rx Data -
14	Reserved
15	Rx Clock -

### PORT 2 TERMINAL

PIN	FUNCTION	I/O
1	Chassis Ground	[-]
2	Transmit Data	[O]
3	Receive Data	[I]
4	Request To Send	[O]
5	Clear To Send	[I]
6	Not Used	
7	Logic Ground	[-]
8	Data Carrier Detect	[I]
9-19	Not Used	
20	Data Terminal Ready	[O]
21-25	Not Used	

### PORT 3 FSK TELEMETRY

PIN	FUNCTION	I/O
1	Transmit 1	[O]
2	Transmit 2	[O]
3	Reserved	
4	Receive 1	[I]
5	Receive 2	[I]
6	Chassis Ground	[-]
7	Reserved	
8	Reserved	
9	Chassis Ground	[-]

### PORT 3 EIA-232 TELEMETRY

PIN	FUNCTION	I/O
1	DCD	
2	RXD	
3	TXD	
4	DTR	
5	GND	
6	DSR	
7	RTS	
8	NC	
9	NC	

### 25-pin TELEMETRY CONNECTOR

PIN	FUNCTION
3	SYSTEM DETECTOR A1
2	SYSTEM DETECTOR A2
5	SYSTEM DETECTOR B1
19	SYSTEM DETECTOR B2
4	SYSTEM DETECTOR C1
1	SYSTEM DETECTOR C2
7	SYSTEM DETECTOR D1
8	SYSTEM DETECTOR D2
18	LOCAL FLASH
16	DOOR OPEN (MAINTENANCE REQUIRED)
14	TLM SPARE 1
17	ALARM 1
21	ALARM 2
6	TLM SPARE 2
15	EXTERNAL ADDRESS ENABLE
20	CONFLICT FLASH
24	RECEIVE 1
25	RECEIVE 2
9	TLM SPECIAL FUNCTION 1
22	TLM SPECIAL FUNCTION 2
10	TLM SPECIAL FUNCTION 3
23	TLM SPECIAL FUNCTION 4
12	TRANSMIT 1
13	TRANSMIT 2

### TYPE 1 POWER

PIN	FUNCTION	I/O
A	AC Neutral	[I]
B	Not Used	
C	AC Line	[I]
D	Not Used	
E	Not Used	
F	Fault Monitor	[O]
G	Logic Ground	[O]
H	Chassis Ground	[I]
I	Not Used	
J	Not Used	

## APPENDIX B

### PIN LISTS

### Type-2 I/O Modes

#### CONNECTOR A

55 Pin (Plug) Type #22-55P

PIN	FUNCTION	I/O
A	Fault Monitor	[O]
B	+24 VDC External	[O]
C	Voltage Monitor	[O]
D	N1 Red	[O]
E	N1 Don't Walk	[O]
F	N2 Red	[O]
G	N2 Don't Walk	[O]
H	N2 Ped Clear	[O]
J	N2 Walk	[O]
K	Vehicle Detector 2	[I]
L	Ped Detector 2	[I]
M	Mode Input 2	[I]
N	Stop Time (Ring 1)	[I]
P	Inhibit Max Term (Ring 1)	[I]
R	External Start	[I]
S	Interval Advance	[I]
T	Indicator Lamp Control	[I]
U	AC-Common	[I]
V	Chassis Ground	[I]
W	Logic Ground	[O]
X	Flashing Logic Out	[O]
Y	Status Bit C (Ring1)	[O]
Z	N1 Yellow	[O]
a	N1 Ped Clear	[O]
b	N2 Yellow	[O]
c	N2 Green	[O]
d	Mode Output 18	[O]
e	Mode Output 2	[O]
f	Vehicle Detector 1	[I]
g	Ped Detector 1	[I]
h	Mode Input 1	[I]
i	Force-Off (Ring 1)	[I]
j	Ext Min Recall	[I]
k	Manual Control Enable	[I]
m	Call To Non Actuated I	[I]
n	Test A	[I]
p	AC+ (Control)	[I]
q	I/O Mode Bit A	[I]
r	Status Bit B (Ring 1)	[O]
s	N1 Green	[O]
t	N1 Walk	[O]
u	Mode Output 17	[O]
v	Mode Input 18	[I]
w	Omit All Red Clear (Ring1)	[I]
x	Red Rest (Ring 1)	[I]
y	I/O Mode Bit B	[I]
z	Call To Non Actuated II	[I]
AA	Test B	[I]
BB	Walk Rest Modifier	[I]
CC	Status Bit A (Ring 1)	[O]
DD	Mode Output 1	[O]
EE	Mode Input 17	[I]
FF	Ped Recycle (Ring 1)	[I]
GG	Max II Selection (Ring 1)	[I]
HH	I/O Mode Bit C	[I]

#### CONNECTOR B

55 Pin (Socket) Type #22-55S

PIN	FUNCTION	I/O
A	Mode Output 9	[O]
B	Preempt 2 Detector	[I]
C	Mode Output 10	[O]
D	N3 Green	[O]
E	N3 Yellow	[O]
F	N3 Red	[O]
G	N4 Red	[O]
H	N4 Ped Clear	[O]
J	N4 Don't Walk	[O]
K	Mode Output 20	[O]
L	Vehicle Detector 4	[I]
M	Ped Detector 4	[I]
N	Vehicle Detector 3	[I]
P	Ped Detector 3	[I]
R	Mode Input 11	[I]
S	Mode Input 10	[I]
T	Mode Input 21	[I]
U	Mode Input 9	[I]
V	Ped Recycle (Ring 2)	[I]
W	Preempt 4 Detector	[I]
X	Preempt 5 Detector	[I]
Y	N3 Walk	[O]
a	N3 Don't Walk	[O]
b	N4 Green	[O]
c	N4 Yellow	[O]
d	N4 Walk	[O]
e	Mode Output 4	[O]
f	Mode Output 12	[O]
g	Mode Input 12	[I]
h	Mode Input 4	[I]
i	Mode Input 3	[I]
j	Mode Input 19	[I]
k	Mode Input 22	[I]
m	Mode Input 23	[I]
n	Mode Input 24	[I]
p	Overlap A Yellow	[O]
q	Overlap A Red	[O]
r	Mode Output 19	[O]
s	Mode Output 3	[O]
t	Mode Output 11	[O]
u	Overlap D Red	[O]
v	Preempt 6 Detector	[I]
w	Overlap D Green	[O]
x	Mode Input 20	[I]
y	Free (No Coord)	[I]
z	Max II Selection (Ring 2)	[I]
AA	Overlap A Green	[O]
BB	Overlap B Yellow	[O]
CC	Overlap B Red	[O]
DD	Overlap C Red	[O]
EE	Overlap D Yellow	[O]
FF	Overlap C Green	[O]
GG	Overlap B Green	[O]
HH	Overlap C Yellow	[O]

#### CONNECTOR C

61 Pin (Socket) Type #24-61S

PIN	FUNCTION
A	Status Bit A (Ring 2)
B	Status Bit B (Ring 2)
C	N8 Don't Walk
D	N8 Red
E	N7 Yellow
F	N7 Red
G	N6 Red
H	N5 Red
J	N5 Yellow
K	N5 Ped Clear
L	N5 Don't Walk
M	Mode Output 13
N	Mode Output 5
P	Vehicle Detector 5
R	Ped Detector 5
S	Vehicle Detector 6
T	Ped Detector 6
U	Ped Detector 7
V	Vehicle Detector 7
W	Ped Detector 8
X	Mode Input 8
Y	Force-Off (Ring 2)
Z	Stop Time (Ring 2)
a	Inhibit Max Term (Ring 2)
b	Test C
c	Status Bit C (Ring 2)
d	N8 Walk
e	N8 Yellow
f	N7 Green
g	N6 Green
h	N6 Yellow
i	N5 Green
j	N5 Walk
k	Mode Output 21
m	Mode Input 5
n	Mode Input 13
p	Mode Input 6
q	Mode Input 14
r	Mode Input 15
s	Mode Input 16
t	Vehicle Detector 8
u	Red Rest Mode (Ring 2)
v	Omit Red Clear (Ring 2)
w	N8 Ped Clear
x	N8 Green
y	N7 Don't Walk
z	N6 Don't Walk
AA	N6 Ped Clear
BB	Mode Output 22
CC	Mode Output 6
DD	Mode Output 14
EE	Mode Input 7
FF	Mode Output 24
GG	Mode Output 8
HH	Mode Output 16
JJ	N7 Walk
KK	N7 Ped Clear
LL	N6 Walk
MM	Mode Output 23
NN	Mode Output 7
PP	Mode Output 15

Type-2 I/O Modes

I/O MODE BITS (3 PER UNIT)

Mode	Bit	State	State	Names
#	A	B	C	
0	OFF	OFF	OFF	TS 1 Compatible
1	ON	OFF	OFF	Hardwire Interconnect
2	OFF	ON	OFF	System Interface
3	ON	ON	OFF	Reserved
4	OFF	OFF	ON	Reserved
5	ON	OFF	ON	Reserved
6	OFF	ON	ON	Manufacturer Specific
7	ON	ON	ON	Manufacturer Specific

Voltage Levels: OFF = +24; ON = 0

MODE 0 INPUT/OUTPUT FUNCTIONS

Inputs:

Pin	Function
A-h	Phase 1 Hold
A-M	Phase 2 Hold
B-i	Phase 3 Hold
B-h	Phase 4 Hold
C-m	Phase 5 Hold
C-p	Phase 6 Hold
C-EE	Phase 7 Hold
C-X	Phase 8 Hold
B-U	Phase 1 Phase Omit
B-S	Phase 2 Phase Omit
B-R	Phase 3 Phase Omit
B-g	Phase 4 Phase Omit
C-n	Phase 5 Phase Omit
C-q	Phase 6 Phase Omit
C-r	Phase 7 Phase Omit
C-s	Phase 8 Phase Omit
A-EE	Phase 1 Ped Omit
A-v	Phase 2 Ped Omit
B-j	Phase 3 Ped Omit
B-x	Phase 4 Ped Omit
B-T	Phase 5 Ped Omit
B-k	Phase 6 Ped Omit
B-m	Phase 7 Ped Omit
B-n	Phase 8 Ped Omit

Outputs:

Pin	Function
A-DD	Phase 1 Phase On
A-e	Phase 2 Phase On
B-s	Phase 3 Phase On
B-e	Phase 4 Phase On
C-N	Phase 5 Phase On
C-CC	Phase 6 Phase On
C-NN	Phase 7 Phase On
C-GG	Phase 8 Phase On
B-A	Phase 1 Phase Next
B-C	Phase 2 Phase Next
B-t	Phase 3 Phase Next
B-f	Phase 4 Phase Next
C-M	Phase 5 Phase Next
C-DD	Phase 6 Phase Next
C-PP	Phase 7 Phase Next
C-HH	Phase 8 Phase Next
A-u	Phase 1 Check
A-d	Phase 2 Check
B-r	Phase 3 Check
B-K	Phase 4 Check
C-k	Phase 5 Check
C-BB	Phase 6 Check
C-MM	Phase 7 Check
C-FF	Phase 8 Check

MODE 1 INPUT/OUTPUT FUNCTIONS

Inputs:

Pin	Function
A-h	Preempt 1
A-M	Preempt 3
B-i	Vehicle Detector 9
B-h	Vehicle Detector 10
C-m	Vehicle Detector 13
C-p	Vehicle Detector 14
C-EE	Vehicle Detector 15
C-X	Vehicle Detector 16
B-U	Vehicle Detector 11
B-S	Vehicle Detector 12
B-R	Timing Plan C
B-g	Timing Plan D
C-n	Alternate Sequence A
C-q	Alternate Sequence B
C-r	Alternate Sequence C
C-s	Alternate Sequence D
A-EE	Dimming Enable
A-v	Automatic Flash
B-j	Timing Plan A
B-x	Timing Plan B
B-T	Offset 1
B-k	Offset 2
B-m	Offset 3
B-n	TBC On Line

Outputs:

Pin	Function
A-DD	Preempt 1 Status
A-e	Preempt 3 Status
B-s	TBC Auxiliary 1
B-e	TBC Auxiliary 2
C-N	Timing Plan A
C-CC	Timing Plan B
C-NN	Offset 1
C-GG	Offset 2
B-A	Preempt 2 Status
B-C	Preempt 4 Status
B-t	Preempt 5 Status
B-f	Preempt 6 Status
C-M	Offset 3
C-DD	Timing Plan C
C-PP	Timing Plan D
C-HH	Reserved
A-u	Free/Coord Status
A-d	Automatic Flash
B-r	TBC Auxiliary 3
B-K	Reserved
C-k	Reserved
C-BB	Reserved
C-MM	Reserved
C-FF	Reserved

MODE 2 INPUT/OUTPUT FUNCTIONS

Inputs:

Pin	Function
A-h	Preempt 1
A-M	Preempt 3
B-i	Vehicle Detector 9
B-h	Vehicle Detector 10
C-m	Vehicle Detector 13
C-p	Vehicle Detector 14
C-EE	Vehicle Detector 15
C-X	Vehicle Detector 16
B-U	Vehicle Detector 11
B-S	Vehicle Detector 12
B-R	Vehicle Detector 17
B-g	Vehicle Detector 18
C-n	Vehicle Detector 19
C-q	Vehicle Detector 20
C-r	Alarm 1
C-s	Alarm 2
A-EE	Dimming Enable
A-v	Local Flash Status
B-j	Address Bit 0
B-x	Address Bit 1
B-T	Address Bit 2
B-k	Address Bit 3
B-m	Address Bit 4
B-n	MMU Flash Status

Outputs:

Pin	Function
A-DD	Preempt 1 Status
A-e	Preempt 3 Status
B-s	TBC Auxiliary 1
B-e	TBC Auxiliary 2
C-N	Timing Plan A
C-CC	Timing Plan B
C-NN	Offset 1
C-GG	Offset 2
B-A	Preempt 2 Status
B-C	Preempt 4 Status
B-t	Preempt 5 Status
B-f	Preempt 6 Status
C-M	Offset 3
C-DD	Timing Plan C
C-PP	Timing Plan D
C-HH	Reserved
A-u	Free/Coord Status
A-d	Automatic Flash
B-r	TBC Auxiliary 3
B-K	Reserved
C-k	System Special Function 1
C-BB	System Special Function 2
C-MM	System Special Function 3
C-FF	System Special Function 4

# APPENDIX B PIN LISTS

## MODE 2 ADDRESS BIT ASSIGNMENT

<u>ADDRESS BITS</u>					<u>EXTERNAL ADDRESS</u>
<u>4</u>	<u>3</u>	<u>2</u>	<u>1</u>	<u>0</u>	
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14
0	1	1	1	1	15
1	0	0	0	0	16
1	0	0	0	1	17
1	0	0	1	0	18
1	0	0	1	1	19
1	0	1	0	0	20
1	0	1	0	1	21
1	0	1	1	0	22
1	0	1	1	1	23
1	1	0	0	0	24

0 = FALSE (24 V OR OPEN)  
1 = TRUE (0 V OR GROUND)

## **APPENDIX C**

### **SYSTEM INTERCONNECTION**

---

A master transceiver can be interconnected with a number of local transceivers to make up a system. If a leased line is used for interconnection, up to 19 local transceivers can be connected. If customer-owned twisted pair lines are used, up to 24 local transceivers can be connected. Each transmitter output is essentially an open circuit unless it is ON. Each receiver input impedance is 15 kilohms.

The system is interconnected by one or two data channels implying either one or two Telemetry modules at the master. For each channel, the master transmitter outputs are connected to a wire pair designated as the command line which is connected to all local receiver inputs. The master receiver inputs and all local transmitter outputs are connected to another wire pair designated as the readback line. Transient protection on these lines is achieved with a Telemetry Interface Board (TIB) or a Communications Transient Suppressor (CTS) installed in the cabinets between each transceiver and the communication lines.





## APPENDIX D

### GUIDE TO LEASE-LINE INSTALLATION

---

Telephone Companies offer several types of networks designed for lease-line service. This guide is intended to assist Econolite system users and their local telephone company with installation of the proper data transmission lines required for Econolite systems.

Econolite recommends the **Broadcast Polling Multipoint Method** as a cost-effective and reliable means of networking traffic control equipment. "Polling" refers to the method in which a Master station addresses a particular local station, anticipating a data response. Upon completion of the data transaction, the next local station is polled. Econolite utilizes this method but employs full duplex communications; whereby the Master station addresses the next local station while simultaneously receiving data from a previously addressed station.

The system consists of a single Master station, ASC/2M-1000 Zone Master or KMCE-10,000 Arterial Master and one to 24 local stations with any combination of the following controllers: ASC/2(S) family, the CBD, ASC-8000, ASC-8000RM, KMCE-8000, KFT-18/2400. All transmissions from the master station are simultaneously received by all local stations while all transmissions from local stations are received only by the master. Thus, the master station controls the network and no interaction between the local stations occurs.

The following specifications define telephone company lease-line requirements for Econolite Master/Local station networking. Econolite telemetry module modem design specifications are also enclosed to assist in telephone company circuit design. Further assistance from Econolite is available upon request.

## APPENDIX D

### GUIDE TO LEASE LINE INSTALLATION

---

#### LEASE-LINE SPECIFICATIONS

Line Type:	Voice Grade
Interconnect Method:	Broadcast Polling Multipoint
Drops:	20 Points or 4,000 Facility Miles
Battery Voltage:	DC Voltage shall not be present on the line between tip and ring or tip, ring, and ground
Data Signal Power:	Maximum Transmitted: 0 dBm (3 second average) +13 dBm (instantaneous) Received: -16 dBm " 1 dB
Loss Variation:	No more than " 4 dB long term (12 dB to 20 dB) No more than " 3 dB short term
Terminal Equipment Impedance:	600 S " 10% resistive over the voiceband and balanced
Isolation To Ground:	At least 50 kS AC (300-3000 Hz)
Breakdown Voltage:	At least 1500 VRMS at 60 Hz
Channel Requirements:	Two channels minimum: (1) transmit, (1) receive. This is equivalent to one Econolite telemetry channel. For systems larger than 10 intersection controllers, Econolite recommends the use of two telemetry channels (four leased-lines) to ensure full data communications within 1 second.

**ECONOLITE TELEMETRY MODULE MODEM SPECIFICATIONS**

TRANSMITTER CHARACTERISTICS

Transmitter:	Digital-to-FSK modulator
Output Level:	0 dBm " 15% into a 600 S load adjustable to +6 dBm
Transmit Frequencies:	2200 Hz represents a digital LOW 1200 Hz represents a digital HIGH
Frequency Stability:	±1 Hz over the operating temperature range

RECEIVER CHARACTERISTICS

Receiver:	FSK-to-digital demodulator
Signal-To-Noise: (In-band)	+10 dB or greater
Signal-To-60 Hz Noise:	Greater than -50 dB at an input signal level of 50 mV
Receiver Sensitivity:	-34 dBm
Receiver Frequency:	2200 Hz represents a digital LOW 1200 Hz represents a digital HIGH
Common Mode Rejection: (Input)	Greater than 40 dB

DATA CHANNEL CHARACTERISTICS

Communication Line:	Unconditioned type 3002 voice grade, four-wire private line channel, or equivalent
Line Impedance:	600 S
Type of Transmission:	Time division multiplex/frequency shift keying
Baud Rate:	1200 bps
Word Length:	Eight bits plus odd vertical parity
Command Message:	Three words plus odd horizontal parity
Readback Message:	Two words plus odd horizontal parity with phantom address
Channel Capacity:	Twenty-five messages per second
Channel Operation:	One command message containing cycle, offset, split, master zero, and four special function commands is simultaneously transmitted to all local transceivers. Up to twenty-four command messages per second are then transmitted requesting status readbacks, data and special command and information.



## APPENDIX E

### ASC/2S LOOPBACK DIAGNOSTIC INPUT/OUTPUT TABLES

Loopback diagnostic failures are identified by error codes. The tables in this appendix list these error codes and the input and output connections required for loopback diagnostics. For connectors A, B, C, D, and Telemetry, the connector pins and their corresponding input or output buffer circuits are listed with the associated error code. The tables show groups of circuits that can be connected for loopback diagnostics. Some groups contain one input (or output) circuit which can be paired with more than one output (or input) circuit to generate a different error code with each connection.

#### CONNECTOR A

PIN	ERROR CODE	INPUT BUFFER	OUTPUT CIRCUITS	DESCRIPTION	PIN	ERROR CODE	BUFFER INPUT	OUTPUT CIRCUITS	DESCRIPTION
f	00	RP22-16	U58-1 (IN)	Ø1 VEH DET	z	10	RP24-12	U60-12 (IN)	NON-ACTUATED 2
s		U76-15	U46-7 (OUT)	Ø1 GRN	K	11	RP24-16	U60-1 (IN)	Ø2 VEH DET
g	01	RP22-15	U58-15 (IN)	Ø1 PED DET	c		U77-15	U61-7 (OUT)	Ø2 GRN
Z		U76-14	U46-9 (OUT)	Ø1 YEL	L	12	RP24-15	U60-15 (IN)	Ø2 PED DET
h	02	RP22-19	U58-4 (IN)	Ø1 HOLD	b		U77-14	U61-9 (OUT)	Ø2 YEL
D		U76-13	U46-10 (OUT)	Ø1 RED	M	13	RP24-19	U60-4 (IN)	Ø2 HOLD
N	03	RP17-14	U52-14 (IN)	RING 1 STOP TIME	F		U77-13	U61-10 (OUT)	Ø2 RED
t		U76-12	U46-11 (OUT)	Ø1 WALK	n	14	RP21-14	U56-14 (IN)	TEST "A"
EE	04	RP22-17	U58-2 (IN)	Ø1 PED OMIT	J		U77-12	U61-11	Ø2 WALK
a		U76-11	U46-12 (OUT)	Ø1 PED CLR	v	15	RP24-17	U60-2 (IN)	Ø2 PED OMIT
FF	05	RP18-14	U53-14 (IN)	RING 1 PED REC	H		U77-11	U61-12 (OUT)	Ø2 PED CLR
E		U78-18	U62-4 (OUT)	Ø1 DON'T WALK	i	16	RP16-14	U51-14 (IN)	RING 1 FORCE OFF
w	06	RP20-14	U55-14 (IN)	RING 1 OMIT ALL RED	G		U78-17	U62-5 (OUT)	Ø2 DON'T WALK
DD		U76-18	U46-4 (OUT)	Ø1 PHASE ON	x	17	RP19-14	U54-14 (IN)	RING 1 RED REST
P	07	RP22-14	U58-14 (IN)	RING 1 INH MAX	e		U77-18	U61-4 (OUT)	Ø2 PHASE ON
u		U76-16	U46-6 (OUT)	Ø1 CHECK	GG	18	RP24-14	U60-14 (IN)	RING 1 MAX 2
T	08	RP16-12	U51-12 (IN)	LAMP CONTROL	d		U77-16	U61-6 (OUT)	Ø2 CHECK
R	09	RP17-12	U52-12 (IN)	EXTERNAL START	q	19	RP23-19	U59-2 (IN)	I/O MODE "A"
AA	0A	RP21-13	U56-13 (IN)	TEST "B"	A		U74-18	U73-4 (OUT)	FAULT MONITOR
CC		U78-13	U62-10 (OUT)	RING 1 STATUS BIT "A"	HH	1A	RP23-17	U59-6 (IN)	I/O MODE "C"
S	0B	RP19-12	U54-12 (IN)	INTERNAL ADVANCE	y	1B	RP23-18	U59-4 (IN)	I/O MODE "B"
r		U78-12	U62-11 (OUT)	RING 1 STATUS BIT "B"	C		U78-16	U62-6 (OUT)	VOLTAGE MONITOR
k	0C	RP18-12	U53-12 (IN)	MANUAL CONTROL ENABLE					
BB	0D	RP21-12	U56-12 (IN)	WALK REST MODIFIER					
Y		U78-11	U62-12 (OUT)	RING 1 STATUS BIT "C"		1C			RESERVED
j	0E	RP20-12	U55-12 (IN)	MINIMUM RECALL					
m	0F	RP22-12	U58-12 (IN)	NON-ACTUATED 1	p				AC+
X		CR20	CR17 (OUT)	FLASHING LOGIC	U				AC-
		Q2	R58	FLASHING LOGIC	V				CHASSIS GROUND
		CR15	U78-14	FLASHING LOGIC					
		U62-9		FLASHING LOGIC					

## APPENDIX E

### ASC/2S LOOPBACK DIAGNOSTIC INPUT/OUTPUT TABLES

#### CONNECTOR B

PIN	ERROR CODE	INPUT BUFFER	CIRCUITS OUTPUT	DESCRIPTION	PIN	ERROR CODE	INPUT BUFFER	CIRCUITS OUTPUT	DESCRIPTION
N		RP21-16	U56-1 (IN)	Ø3 VEH DET	M		RP20-15	U55-15 (IN)	Ø4 PED DET
D	1D	U72-15	U36-7 (OUT)	Ø3 GRN	c	2F	U75-14	U45-9 (OUT)	Ø4 YEL
AA	1E	U73-16	U37-6 (OUT)	OVERLAP "A" GRN	BB	30	U73-12	U37-11 (OUT)	OVERLAP "B" YEL
P		RP21-15	U56-15 (IN)	Ø3 PED DET	h		RP20-19	U55-4 (IN)	Ø4 HOLD
E	1F	U72-14	U36-9 (OUT)	Ø3 YEL	G	31	U75-13	U45-10 (OUT)	Ø4 RED
p	20	U73-15	U37-7 (OUT)	OVERLAP "A"	CC	32	U73-11	U37-12 (OUT)	OVERLAP "B" RED
i		RP21-19	U56-4 (IN)	Ø3 HOLD	g		RP20-18	U55-3 (IN)	Ø4 PHASE OMIT
F	21	U72-13	U36-10 (OUT)	Ø3 RED	d	33	U75-12	U45-11 (OUT)	Ø4 WALK
q	22	U73-14	U37-9 (OUT)	OVERLAP "A" RED	w	34	U74-13	U44-10 (OUT)	OVERLAP "D" GRN
R		RP21-18	U56-3 (IN)	Ø3 PHASE OMIT	n		RP17-17	U52-2 (IN)	Ø8 PED OMIT
Y	23	U72-12	U36-11 (OUT)	Ø3 WALK	H	35	U75-11	U45-12 (OUT)	Ø4 PED CLEAR
FF	24	U74-16	U44-6 (OUT)	OVERLAP "C" GRN	EE	36	U74-12	U44-11 (OUT)	OVERLAP "D" YEL
m		RP16-17	U51-2 (IN)	Ø7 PED OMIT	k		RP18-17	U53-2 (IN)	Ø6 PED OMIT
Z	25	U72-11	U36-12 (OUT)	Ø3 PED CLEAR	J	37	U73-17	U37-5 (OUT)	Ø4 DON'T WALK
HH	26	U74-15	U44-7 (OUT)	OVERLAP "C" YEL	u	38	U74-11	U44-12 (OUT)	OVERLAP "D" RED
T		RP19-17	U54-2 (IN)	Ø5 PED OMIT	x		RP20-17	U55-2 (IN)	Ø4 PED OMIT
a	27	U73-18	U37-4 (OUT)	Ø3 DON'T WALK	e	39	U75-18	U45-4 (OUT)	Ø4 PHASE ON
DD	28	U74-14	U44-9 (OUT)	OVERLAP "C" RED	C	3A	U77-17	U61-5 (OUT)	Ø2 PHASE NEXT
j		RP21-17	U56-2 (IN)	Ø3 PED OMIT	S	3B	RP24-18	U60-3 (IN)	Ø2 PHASE OMIT
s	29	U72-18	U36-4 (OUT)	Ø3 PHASE ON	K		U75-16	U45-6 (OUT)	Ø4 CHECK
A	2A	U76-17	U46-5 (OUT)	Ø1 PHASE NEXT	z	3C	RP24-13	U60-13 (IN)	RING 2 MAX 2
U	2B	RP22-18	U58-3 (IN)	Ø1 PHASE OMIT	B	3D	RP23-16	U59-8 (IN)	PREEMPT 2 CALL
r		U72-16	U36-6 (OUT)	Ø3 CHECK	W	3E	RP23-15	U59-11 (IN)	PREEMPT 4 CALL
V	2C	RP18-13	U53-13 (IN)	RING 2 PED RECYCLE	X	3F	RP23-14	U59-13 (IN)	PREEMPT 5 CALL
t		U72-17	U36-5 (OUT)	Ø3 PHASE NEXT	v	40	RP23-13	U59-15 (IN)	PREEMPT 6 CALL
L		RP20-16	U55-1 (IN)	Ø4 VEH DET	y	41	RP23-12	U59-17 (IN)	COORD FREE
b	2D	U75-15	U45-7 (OUT)	Ø4 GRN	f		U75-17	U45-5 (OUT)	Ø4 PHASE NEXT
GG	2E	U73-13	U37-10 (OUT)	OVERLAP "B" GRN					

**APPENDIX E**

**ASC/2S LOOPBACK DIAGNOSTIC INPUT/OUTPUT TABLES**

**CONNECTOR C**

PIN	ERROR CODE	INPUT BUFFER	CIRCUITS OUTPUT	DESCRIPTION	PIN	ERROR CODE	INPUT BUFFER	CIRCUITS OUTPUT	DESCRIPTION
P		RP19-16	U54-1 (IN)	Ø5 VEH DET	G	55	U70-13	U34-10 (OUT)	Ø6 RED
i	42	U68-15	U32-7 (OUT)	Ø5 GRN	CC	56	U70-18	U34-4 (OUT)	Ø6 PHASE ON
K	43	U68-11	U32-12 (OUT)	Ø5 PED CLEAR	q		RP18-18	U53-3 (IN)	Ø6 PHASE OMIT
M	44	U68-17	U32-5 (OUT)	Ø5 PHASE NEXT	LL	57	U70-12	U34-11 (OUT)	Ø6 WALK
R		RP19-15	U54-15 (IN)	Ø5 PED DET	BB	58	U70-16	U34-6 (OUT)	Ø6 CHECK
J	45	U68-14	U32-9 (OUT)	Ø5 YEL	V		RP16-16	U51-1 (IN)	Ø7 VEH DET
L	46	U69-18	U33-4 (OUT)	Ø5 DON'T WALK	f	59	U71-15	U35-7 (OUT)	Ø7 GRN
DD	47	U70-17	U34-5 (OUT)	Ø6 PHASE NEXT	KK	5A	U71-11	U35-12 (OUT)	Ø7 PED CLEAR
m		RP19-19	U54-4 (IN)	Ø5 HOLD	U		RP16-15	U51-15 (IN)	Ø7 PED DET
H	48	U68-13	U32-10 (OUT)	Ø5 RED	E	5B	U71-14	U35-9 (OUT)	Ø7 YEL
N	49	U68-18	U32-4 (OUT)	Ø5 PHASE ON	y	5C	U69-16	U33-6 (OUT)	Ø7 DON'T WALK
n		RP19-18	U54-3 (IN)	Ø5 PHASE OMIT	EE		RP16-19	U51-4 (IN)	Ø7 HOLD
j	4A	U68-12	U32-11 (OUT)	Ø5 WALK	F	5D	U71-13	U35-10 (OUT)	Ø7 RED
k	4B	U68-16	U32-6 (OUT)	Ø5 CHECK	NN	5E	U71-18	U35-4 (OUT)	Ø7 PHASE ON
a	4C	RP22-13	U58-13 (IN)	RING 2 INH MAX	r		RP16-18	U51-3 (IN)	Ø7 PHASE OMIT
PP		U71-17	U35-5 (OUT)	Ø7 PHASE NEXT	JJ	5F	U71-12	U35-11 (OUT)	Ø7 WALK
u	4D	RP19-13	U54-13 (IN)	RING 2 RED REST	MM	60	U71-16	U35-6 (OUT)	Ø7 CHECK
HH		U67-17	U31-5 (OUT)	Ø8 PHASE NEXT	t		RP17-16	U52-1 (IN)	Ø8 VEH DET
v	4E	RP20-13	U55-13 (IN)	RING 2 OMIT ALL RED	x	61	U67-15	U31-7 (OUT)	Ø8 GRN
A		U69-13	U33-10 (OUT)	RING 2 STATUS BIT "A"	w	62	U67-11	U31-12 (OUT)	Ø8 PED CLEAR
Z	4F	RP17-13	U52-13 (IN)	RING 2 STOP TIME	W		RP17-15	U52-15 (IN)	Ø8 PED DET
B		U69-12	U33-11 (OUT)	RING 2 STATUS BIT "B"	e	63	U67-14	U31-9 (OUT)	Ø8 YEL
Y	50	RP16-13	U51-13 (IN)	RING 2 FORCE OFF	C	64	U69-15	U33-7 (OUT)	Ø8 DON'T WALK
c		U69-11	U33-12 (OUT)	RING 2 STATUS BIT "C"	X		RP17-19	U52-4 (IN)	Ø8 HOLD
S		RP18-16	U53-1 (IN)	Ø6 VEH DET	D	65	U67-13	U31-10 (OUT)	Ø8 RED
g	51	U70-15	U34-7 (OUT)	Ø6 GRN	GG	66	U67-18	U31-4 (OUT)	Ø8 PHASE ON
AA	52	U70-11	U34-12 (OUT)	Ø6 PED CLEAR	s	67	RP17-18	U52-3 (IN)	Ø8 PHASE OMIT
T		RP18-15	U53-15 (IN)	Ø6 PED DET	d		U67-12	U31-11 (OUT)	Ø8 WALK
h	53	U70-14	U34-9 (OUT)	Ø6 YEL	FF	68	U67-16	U31-6 (OUT)	Ø8 CHECK
z	54	U69-17	U33-5 (OUT)	Ø6 DON'T WALK	b		R54,R63,R64	U19-2 (IN)	TEST C
p		RP18-19	U53-4 (IN)	Ø6 HOLD		69			SEE TELEMETRY PORT 1

## APPENDIX E

### ASC/2S LOOPBACK DIAGNOSTIC INPUT/OUTPUT TABLES

#### CONNECTOR D

PIN	ERROR CODE	INPUT BUFFER	CIRCUITS OUTPUT	DESCRIPTION	PIN	ERROR CODE	INPUT BUFFER	CIRCUITS OUTPUT	DESCRIPTION
1		U65-12	U28-11 (OUT)	PREEMPT 5 ACTIVE	47	7A	RP14-12	U42-1 (IN)	EXP DET 2
57	6A	RP14-17	U49-2 (IN)	PREEMPT 1 CALL	41		U65-18	U28-4 (OUT)	SPARE 4
2		U64-14	U27-9 (OUT)	OFFSET BIT 3	20	7B	RP12-18	U47-3 (IN)	TEST C
50	6B	PR15-17	U50-2 (IN)	PREEMPT 3 CALL	42		U65-14	U28-9 (OUT)	OFFSET BIT 2
5		U63-17	U26-5 (OUT)	CROSS STREET SYNC	13	7C	RP12-12	U40-1 (IN)	EXP DET 8
60	6C	RP15-18	U50-3 (IN)	REMOTE FLASH	43		U66-15	U29-7 (OUT)	CYCLE BIT 1
49	6D	RP14-13	U42-2 (IN)	PREEMPT 2 CALL	16	7D	RP14-19	U49-4 (IN)	SPLIT BIT 1
8		U65-16	U28-6 (OUT)	NIC SPECIAL FUNTN 2	44		U65-15	U28-7 (OUT)	CYCLE BIT 2
61	6E	RP13-13	U41-2 (IN)	PREEMPT 6 CALL	14	7E	RP13-14	U41-3 (IN)	TIME RESET
11		U63-16	U26-6 (OUT)	SPARE 2	45		U64-18	U27-4 (OUT)	SPARE 5
55	6F	RP15-13	U43-2 (IN)	PREEMPT 4 CALL	19	7F	RP12-13	U40-2 (IN)	SPARE 3
15		U66-18	U29-4 (OUT)	SPARE 3	46		U63-14	U26-9 (OUT)	SPLIT BIT 2
56	70	RP13-17	U48-2 (IN)	PREEMPT 5 CALL	18	80	RP15-12	U43-1 (IN)	EXP DET 4
21		U63-15	U26-7 (OUT)	SPLIT BIT 1	48		U64-12	U27-11 (OUT)	PREEMPT 6 ACTIVE
58	71	RP12-17	U47-2 (IN)	CMV STOP TIME	17	81	RP14-16	U49-1 (IN)	EXP DET 1
22		U64-13	U27-10 (OUT)	PREEMPT 3 ACTIVE	51		U63-18	U26-4 (OUT)	SPARE 6
9	72	RP14-15	U42-4 (IN)	SPLIT BIT 2	25	82	RP15-19	U50-4 (IN)	CYCLE BIT 1
23		U66-13	U29-10 (OUT)	PREEMPT 1 ACTIVE	52		U66-17	U29-5 (OUT)	SPARE 7
38	73	RP13-18	U48-3 (IN)	DUAL COORD	30	83	RP13-16	U48-1 (IN)	EXP DET 5
24		U64-16	U27-6 (OUT)	NIC SPECIAL FUNTION 3	53		U63-13	U26-10 (OUT)	SYNC
3	74	RP15-14	U43-3 (IN)	SPLIT DEMAND	26	84	RP14-14	U42-3 (IN)	COORD FREE
27		U63-12	U26-11 (OUT)	COORD STATUS	40	85	RP12-16	U47-1 (IN)	EXP DET 7
12	75	RP13-15	U41-4 (IN)	OFFSET BIT 1	54		U65-17	U28-5 (OUT)	SPARE 8
28		U66-16	U29-6 (OUT)	NIC SPECIAL FUNCTN 1	31	86	RP15-16	U50-1 (IN)	EXP DET 3
36	76	RP12-15	U40-4 (IN)	OFFSET BIT 3	35	87	RP15-15	U43-4 (IN)	CYCLE BIT 2
29		U64-15	U27-7 (OUT)	CYCLE BIT 3	59		CR16	CR21 (OUT)	PREEMPT CMU INTERLOCK
10	77	RP12-19	U47-4	OFFSET BIT 2			Q3	R62	PREEMPT CMU INTERLOCK
32		U65-13	U28-10 (OUT)	PREEMPT 2 ACTIVE			R61	U27-5	PREEMPT CMU INTERLOCK
6	78	RP13-19	U48-4 (IN)	CYCLE BIT 3					PREEMPT CMU INTERLOCK
33		U66-14	U29-9 (OUT)	OFFSET BIT 1	37	88	RP12-14	U40-3 (IN)	TEST D
4	79	RP14-18	U49-3 (IN)	COORD SYNC	39	89	RP13-12	U41-1 (IN)	EXP DET 6
34		U66-12	U29-11 (OUT)	PREEMPT 4 ACTIVE					



## APPENDIX E

### ASC/2S LOOPBACK DIAGNOSTIC INPUT/OUTPUT TABLES

#### 25-PIN TELEMETRY CONNECTOR AND PORT 1

PIN	ERROR CODE	INPUT BUFFER	CIRCUITS OUTPUT	DESCRIPTION	PIN	ERROR CODE	INPUT BUFFER	CIRCUITS OUTPUT	DESCRIPTION
9		U66-11	U29-12 (OUT)	TLM SPF 1	10		U64-11	U27-12 (OUT)	TLM SPF 3
3	8A	RP36-19	U30-2 (IN)	SYS DET A1	5	92	RP36-17	U30-6 (IN)	SYS DET B1
4	8B	RP36-15	U30-11 (IN)	SYS DET C1	7	93	RP36-13	U30-15 (IN)	SYS DET D1
14	8C	RP35-19	U57-2 (IN)	TLM SPARE 1	21	94	RP35-17	U57-6 (IN)	ALARM 2
15	8D	RP35-15	U57-11 (IN)	EXT ADDRESS ENABLE	18	95	RP35-13	U57-15 (IN)	LOCAL FLASH
22		U65-11	U28-12 (OUT)	TLM SPF 2	23		U63-11	U26-12 (OUT)	TLM SPF 4
2	8E	RP36-18	U30-4 (IN)	SYS DET A2	19	96	RP36-16	U30-8 (IN)	SYS DET B2
1	8F	RP36-14	U30-13 (IN)	SYS DET C2	8	97	RP36-12	U30-17 (IN)	SYS DET D2
17	90	RP35-18	U57-4 (IN)	ALARM 1	6	98	RP35-16	U57-8 (IN)	TLM SPARE 2
20	91	RP35-14	U57-13 (IN)	CONFLICT FLASH	16	99	RP35-12	U57-17 (IN)	DOOR OPEN
						69			TELEMETRY FAIL

#### PORT 1 FSK LOOP BACK CONNECTOR

OUTPUT PIN	INPUT PIN
1	4
2	5

(Attach a 600 ohm resistor between pins 1 and 5.)

#### TERMINAL (PORT 2)

PIN	ERROR CODE	INPUT BUFFER	CIRCUITS OUTPUT	DESCRIPTION	PIN	ERROR CODE	INPUT BUFFER	CIRCUITS OUTPUT	DESCRIPTION
9A				TERMINAL FAIL					

#### PORT 2 TERMINAL LOOP BACK CONNECTOR

OUTPUT PIN	INPUT PIN
2	3
5	4
20	6
8	6

#### SDLC (PORT 3)

PIN	ERROR CODE	INPUT BUFFER	CIRCUITS OUTPUT	DESCRIPTION	PIN	ERROR CODE	INPUT BUFFER	CIRCUITS OUTPUT	DESCRIPTION
9B				SDLC FAIL					



**APPENDIX E**  
**ASC/2S LOOPBACK DIAGNOSTIC INPUT/OUTPUT TABLES**

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**PORT 3 SDLC LOOP BACK CONNECTOR**

OUTPUT PIN	INPUT PIN
1	5
3	7
9	13
11	15



Figure 2-1. ASC/2S System Block Diagram

Figure 2-2. Processor Section Block Diagram

Figure 2-3. I/O Section Block Diagram

Figure 2-4. Processor-I/O Module Component Placement