


A8T/M SCHEMATIC R2.1

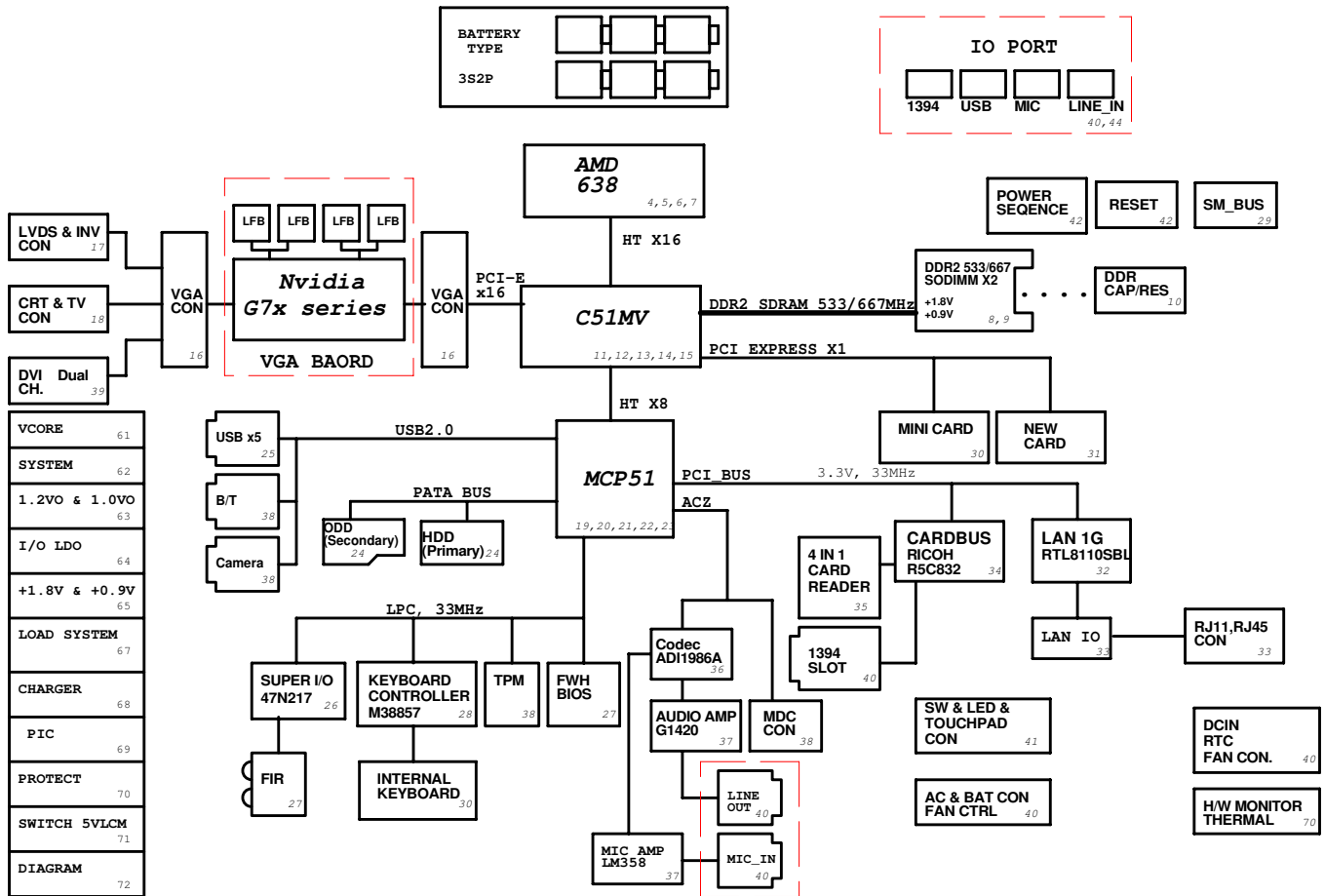
PAGE	Content	PAGE	Content
SYSTEM PAGE REF.		POWER PAGE REF.	
4	AMD S1 CPU--HT	61	POWER_VCORE
5	AMD S1 CPU--CNIL	62	POWER_SYSTEM
6	AMD S1 CPU--DDR2	63	POWER_I/O_1.2VO & 1.0VO
7	AMD S1 CPU--PWR/GND	64	POWER_I/O_LDO
8	DDR2 SO-DIMM_0	65	POWER_I/O_DDR2
9	DDR2 SO-DIMM_1	66	POWER_VGA_CORE (Empty)
10	DDR2 ADDRESS TERMINATION	67	POWER_LOAD_SYSTEM
11	C51M--HT TO CPU	68	POWER_CHARGER
12	C51M--HT TO MCP	69	POWER_PIC
13	C51M--PCI-E	70	POWER_PROTECT
14	C51M--CRT & LVDS	71	POWER_SWITCH_+5VLCM
15	C51M--PWR/GND	72	POWER_DIAGRAM
16	VGA CONN		
17	LVDS & INVERTER CONN		
18	CRT & TV_OUT		
19	MCP51--HT		
20	MCP51--PCI		
21	MCP51--IDE		
22	MCP51--USB & HDA & GPIO		
23	MCP51--PWR/GND		
24	HDD & CD-ROM CONN		
25	USB PORTS		
26	SUPER I/O LPC47N217		
27	BIOS & FIR		
28	KBC 38857		
29	SM BUS & POWER PORT		
30	PCI-E--MINI CARD		
31	PCI-E--NEW CARD		
32	PCI--LAN RTL8110CL		
33	RJ45 & RJ11		
34	PCI--1394, CardReader R5C832		
35	PCI--4 IN1 CON		
36	AUDIO CODEC ALC660		
37	AUDIO AMP G1420		
38	MDC,B/T,TPM & DISCHG,HOLE		
39	DVI CONN		
40	ACIN, BAT, FAN, I/O PORT		
41	SW & LED & TP		
42	POWER-ON SEQUENCE		
43	HISTORY		
44	I/O PORT		

Core Design

	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: PAGE REF.	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		2.1	SHEET 1 OF 55		RELEASE DATE:	

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A8T/M AMD S1/C51MV BLOCK DIAGRAM



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 PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: BLOCK DAIGRAM	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
	2.1	SHEET 2 OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>

PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
LAN -- Realtek	AD17	1	C	
1394	AD16	0	A	
4 IN 1		0	B	

SM_BUS ADDRESS : Thermal MAX6657 = 1001100x (98h)
DDR_SODIMM0 = 1010000x (A0h)
DDR_SODIMM1 = 1010001x (A2h)

MCP51_GPIO	Use As	Signal Name	Power
GPIO_1	GPI	PCB_ID2	+3VS
GPIO_2	GPI	KB_SCI#	+3VSUS
GPIO_3	GPI	PWRLMT#	+3VSUS
GPIO_4		SUS_STAT#	+3VSUS
GPIO_5	GPO	802_LED_EN#	+3VSUS
GPIO_6	GPO	MCP_TV_EN	+3VSUS
GPIO_7	GPO	CB_SD#	+3VSUS
GPIO_8		CR_VID0	+3VSUS
GPIO_9		CR_VID1	+3VSUS
GPIO_10		(CR_VID2)	+3VSUS
GPIO_11:16]		(CPD_VID[0:5])	+3VSUS
GPIO_17		(LID#)	+3VSUS
GPIO_18		BATT_TALARM#	+3VSUS
GPIO_19		USB_OC#1	+3VSUS
GPIO_20	GPO	1 Hz	+3VSUS
GPIO_21	GPO	IGP_DDC_SELECT	+3VSUS
GPIO_22		ACZ_SDINO_AUD	+3VSUS
GPIO_23		ACZ_SDINI_MDC	+3VSUS
GPIO_24	GPI	CHG_FULL_OC	+3VSUS
GPIO_25		SMB_MEM_SCL	+3VSUS
GPIO_26		SMB_MEM_SDA	+3VSUS
GPIO_27		SMB_CLK_SB	+3VSUS
GPIO_28		SMB_DAT_SB	+3VSUS
GPIO_29		(SMB_ALERT#)	+3VSUS
GPIO_30		PCI_PME#	+3VSUS
GPIO_31	GPI	STO_SMI#	+3VSUS
GPIO_32		EXTSMI#_3A	+3VSUS
GPIO_33	GPI	(R3#)	+3VSUS
GPIO_34		SUS_CLK	+3VSUS
GPIO_35	GPO	WLAN_ON#	+3VSUS
GPIO_36			+3VSUS
GPIO_37	GPO	OP_SD#	+3VSUS
GPIO_38	GPO	MXM_PWR_ON	+3VS
GPIO_39	GPI	VGA_DETECT#	+3VS
GPIO_40	GPO	BACK_OFF#	+3VS
GPIO_41	GPI	VGA_PWRGD	+3VS
GPIO_42		PM_CLKRUN#	+3VS
GPIO_43		PCI_PERR#	+3VS
GPIO_44		ACZ_SYNC	+3VS
GPIO_45		ACZ_SDOUT	+3VS
GPIO_46	GPO	BT_ON/OFF#	+3VS

MCP51_GPIO	Use As	Signal Name	Power
GPIO_47	GPI	LOAD_TEST	+3VS
GPIO_48			
GPIO_49	GPO	FWH_WP#	+3VS
GPIO_50	GPO	LCD_VDD_EN_GM	+3VS
GPIO_51	GPO	LCD_BACKEN_GM	+3VS
GPIO_52		EDID_CLK_C51M	+3VS
GPIO_53		EDID_DATA_C51M	+3VS
GPIO_54	GPO	GPU_ON	+3VS
GPIO_55		HA20GATE	+3VS
GPIO_56		KBDCPURST	+3VS
GPIO_57		SATA_LED#	+3VS
GPIO_58		CPU_THERMTRIP#	+3VS
GPIO_59		PM_THERM#	+3VS
GPIO_60	GPI	PCB_ID0	+3VS
GPIO_61	GPI	PCB_ID1	+3VS
GPIO_62	GPO	IGP_SELECT	+3VS
GPIO_63		(CABLE_DET_F)	+3VS
GPIO_64		(CABLE_DET_S)	+3VS

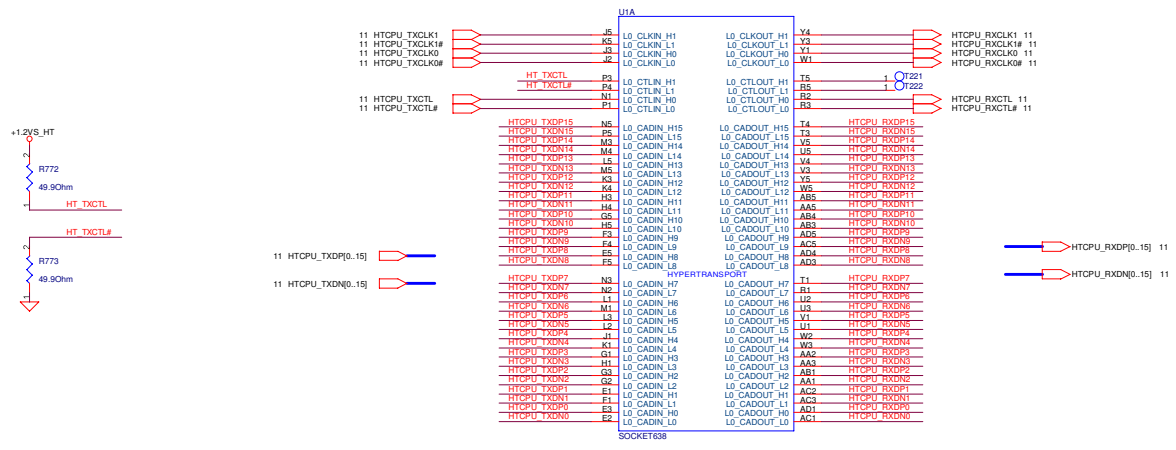
47N217_GPIO	USE_AS	SIGNAL_NAME	Power
GPIO10	GPI		+3VS
GPIO[11:12]	GPO		+3VS
GPIO[13:14]	GPI		+3VS
GPIO23	GPO		+3VS
GPIO[40:45]	GPI		+3VS
GPIO46	GPI		+3VS
GPIO47	GPI		+3VS

M38857_GPIO	USE_AS	SIGNAL_NAME	Power
P23	GPO	MSK_INSTKEY#	+3V
P22	GPO	BAT_LEARN	+3V
P21	GPO		+3V
P20	GPO	KBCRSM	+3V
P42	GPO	WATCHDOG	+3V
P43	GPI	SWDJ_EN	+3V
P44	GPO	KBCPURST_3Q	+3V
P45	GPO	KBC_GA20	+3V
P46	GPO	KBSCI_3Q	+3V
P47	GPI	PM_CLKRUN#	+3V
P50	GPI	BAT_LLOW#_OC	+3V
P51	GPI	FAN1_TACH	+3V
P52	GPO	KBDDT0	+3V
P53	GPO	KBDDT1	+3V
P54	GPI	LID_KBC#	+3V
P55	GPI	BAT_IN_OC#	+3V
P56	GPO	FAN1_DC	+3V
P57	GPO	ADJ_BL	+3V
P67	GPI	NEWCARD_OFF#	+3V
P66	GPI	PANLOCK_#	+3V
P65	GPI	MARATHON_#	+3V
P64	GPI	ACIN_OC#	+3V
P63	GPI	NEWCARD_DET#	+3V
P62	GPI	WIRELESS_#	+3V
P61	GPI	INTERNET_#	+3V
P60	GPI	BLUETOOTH_#	+3V
P76	GPI	SMD_BAT	+3V
P77	GPI	SMC_BAT	+3V
P27	GPO	SCR_LED#	+3V
P26	GPO	NUM_LED#	+3V
P25	GPO	CAP_LED#	+3V
P24	GPO	SET_PCIRSTNS#	+3V
P40	GPO	KBC_EXTSMI	+3V
P41	GPO	PANLOCK_LED	+3V

Core Design:

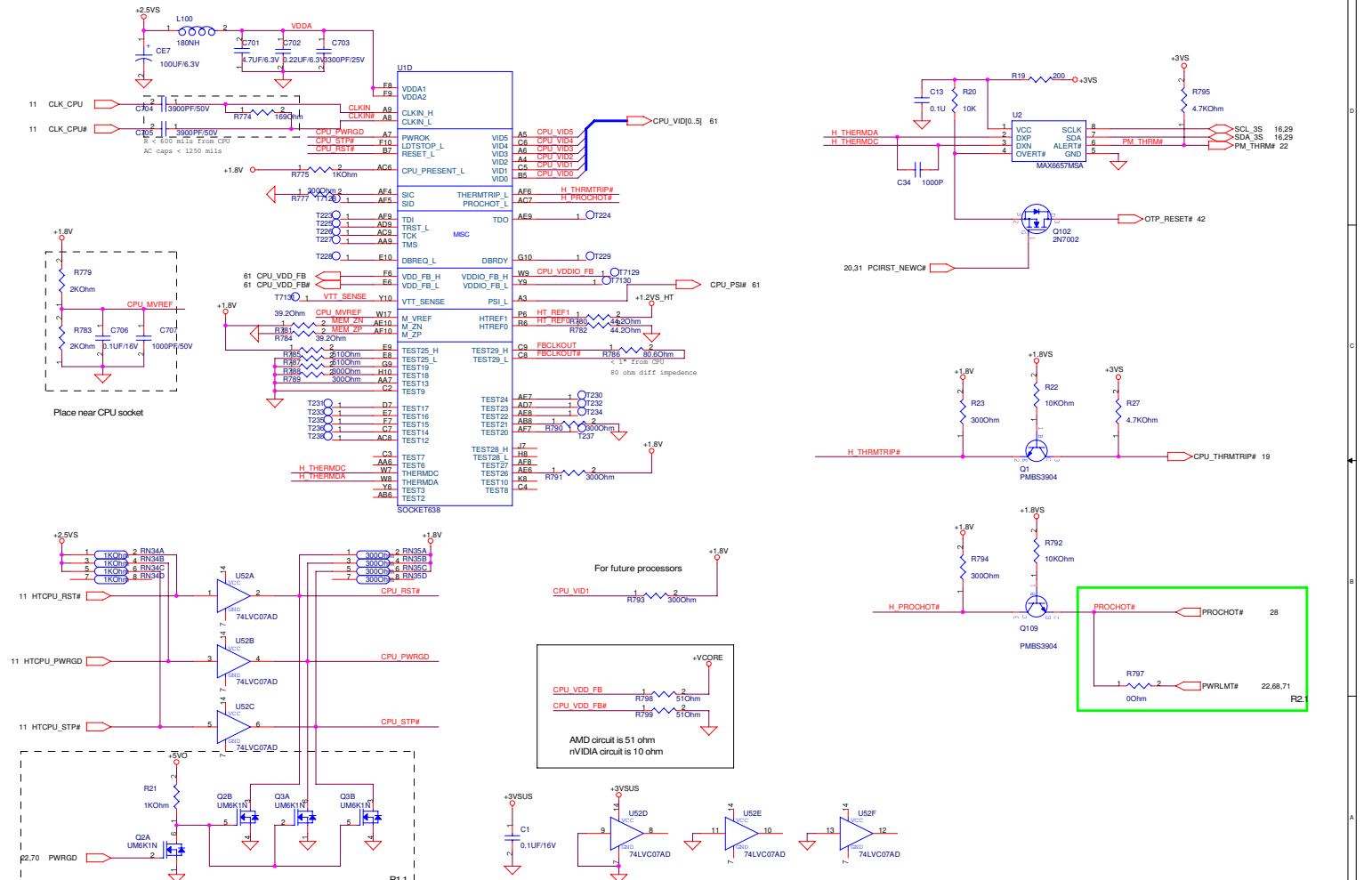
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		2.1	SHEET 3 OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>



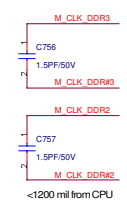
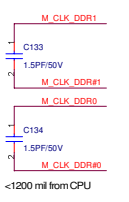
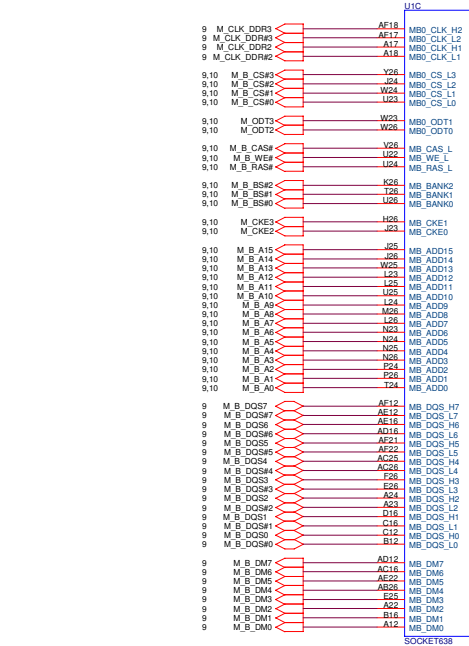
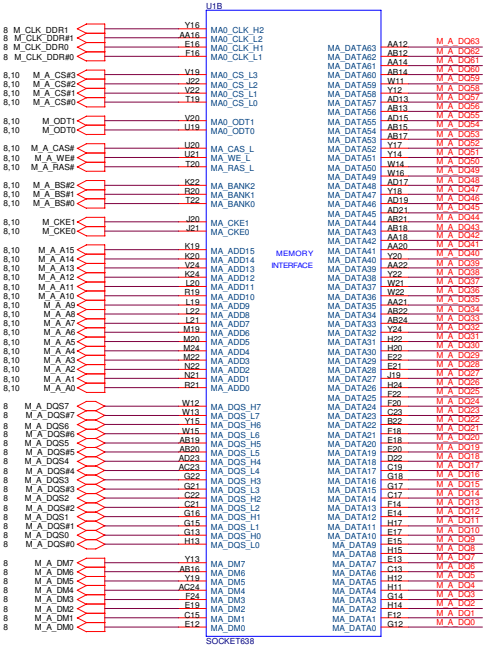
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	2.1	SHEET 4 OF 55		RELEASE DATE :	

<< Kennedy_Zhang >>



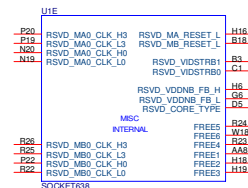
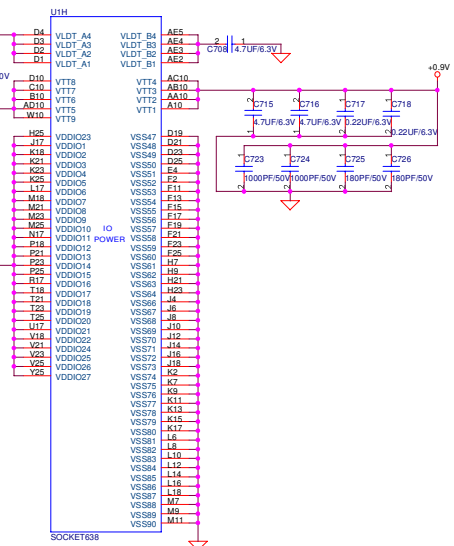
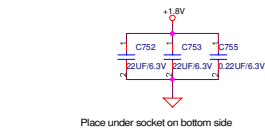
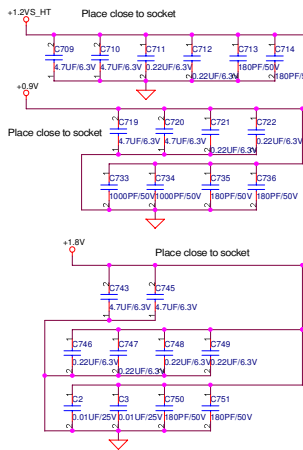
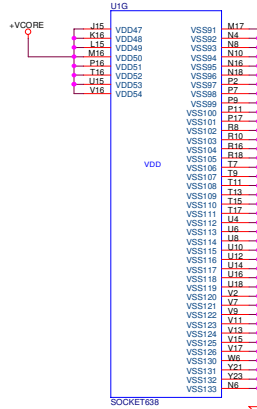
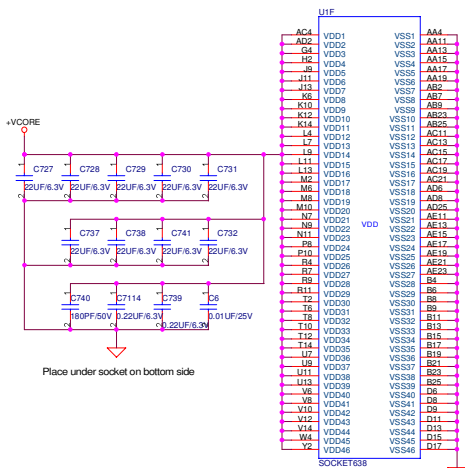
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			SHEET: 5 OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>



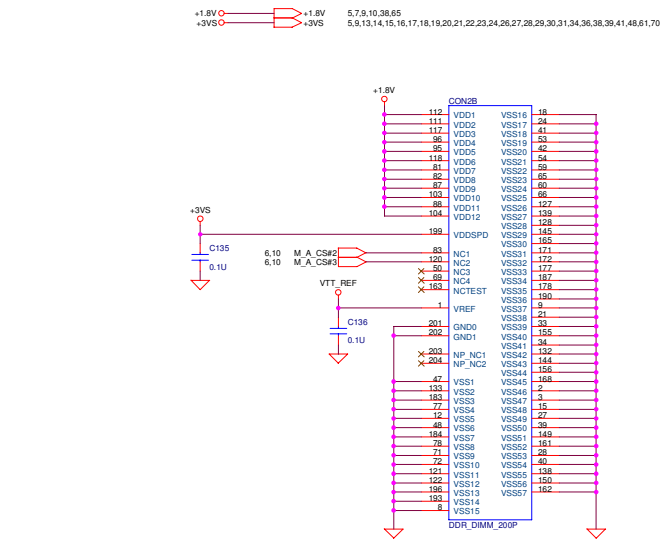
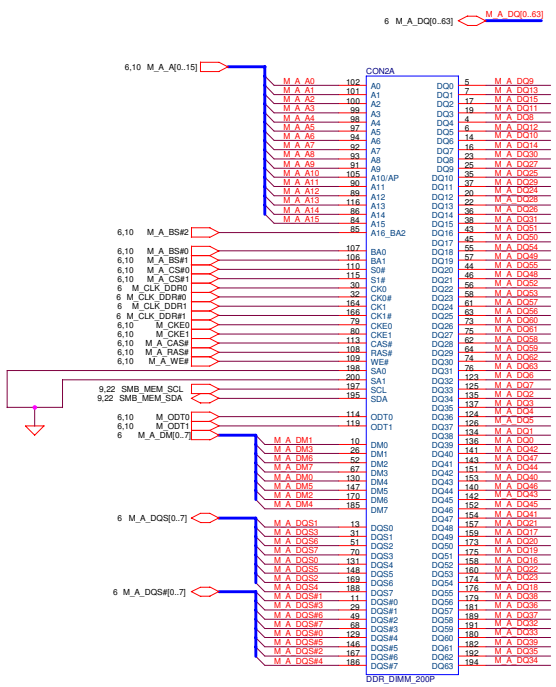
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			SHEET: 6 OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>

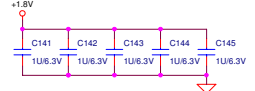
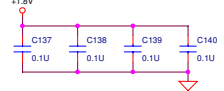


ASUS PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	SHEET: 7 OF 55	DESCRIPTION: S1 CPU PWR/GND	SCHEMATIC FILE NAME: _____	RELEASE DATE: _____	DESIGN ENGINEER: Albert Su
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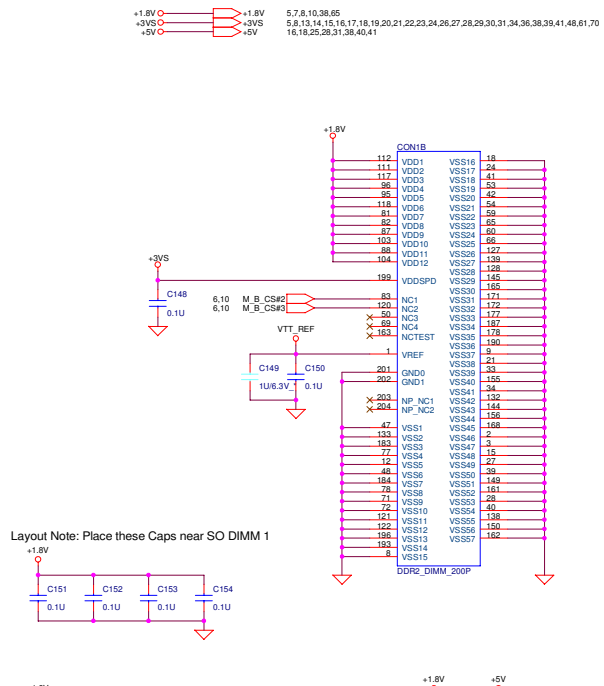
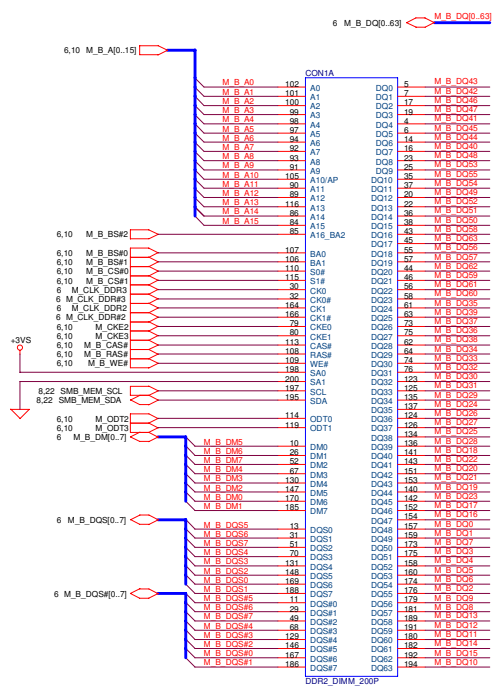


Layout Note: Place these Caps near SO DIMM 0

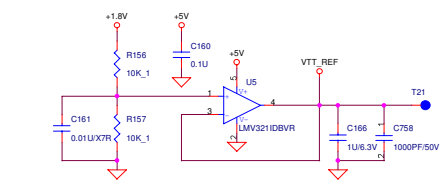
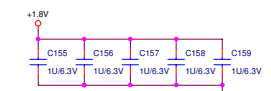
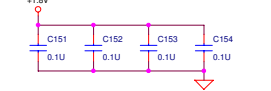


ASUS PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: DDR2 SO-DIMM0	SCHMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
	2.1	SHEET 8 OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>

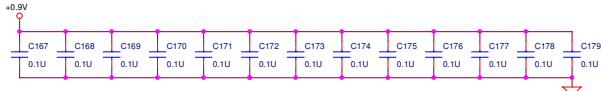


Layout Note: Place these Caps near SO DIMM 1

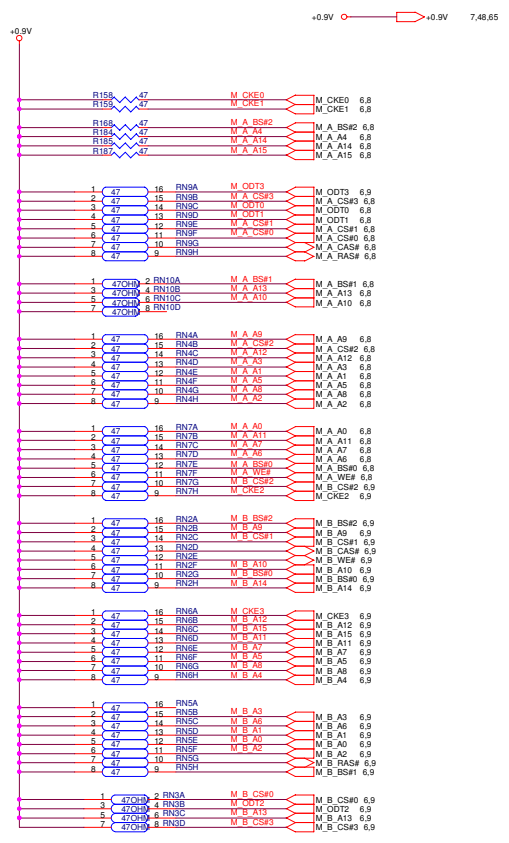
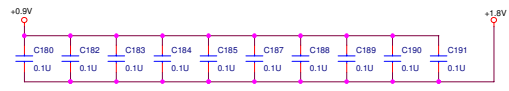


ASUS	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: DDR2 SO-DIMM1	SCHMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		SHEET: 9	OF: 55	RELEASE DATE:		

<< Kennedy_Zhang >>

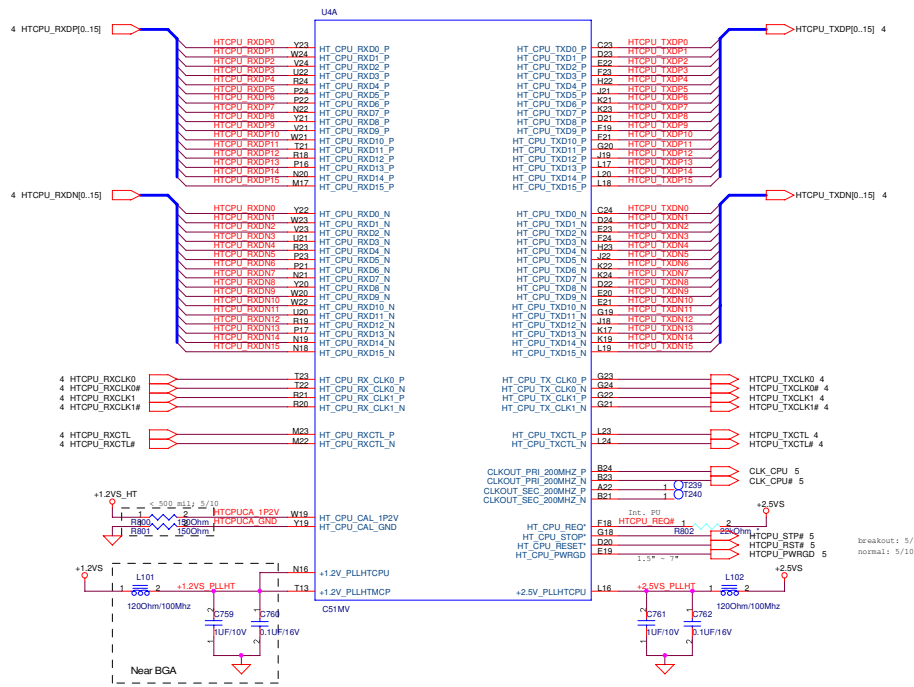


Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V



ASUS	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: DDR2 ADDRESS TERMINATION	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		2.1	SHEET 10 OF 55			

<< Kennedy_Zhang >>

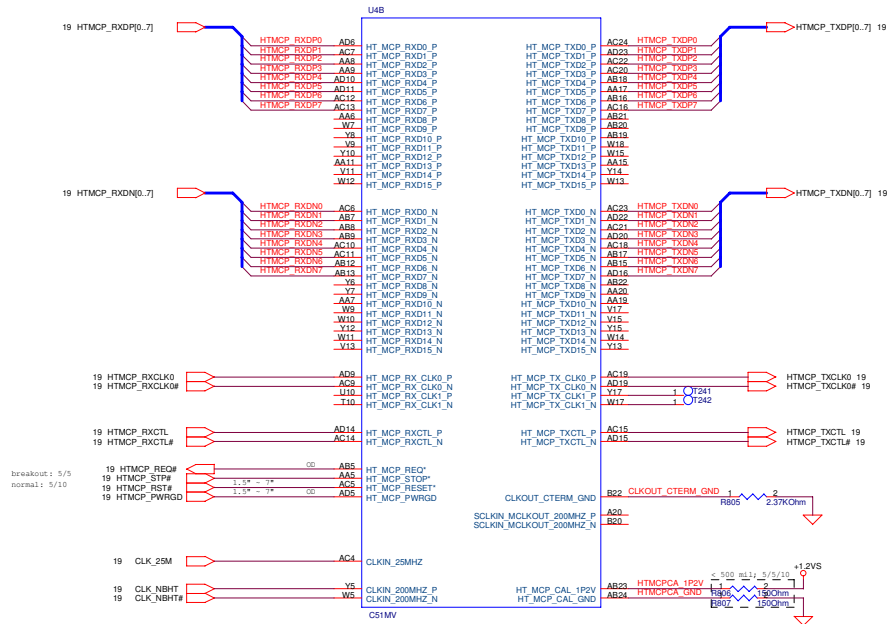


breakout: 5/5
normal: 5/10

Core Designs

ASUS PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION:	SCHMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 11 OF 55	C51M HT	RELEASE DATE :	Albert Su

<< Kennedy_Zhang >>

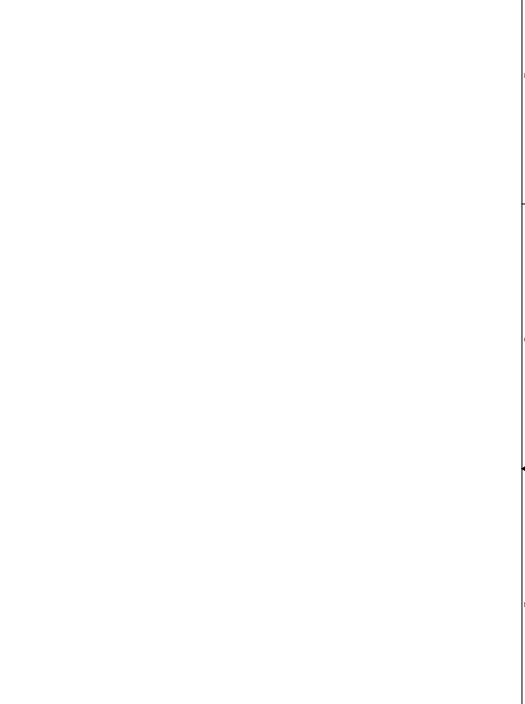
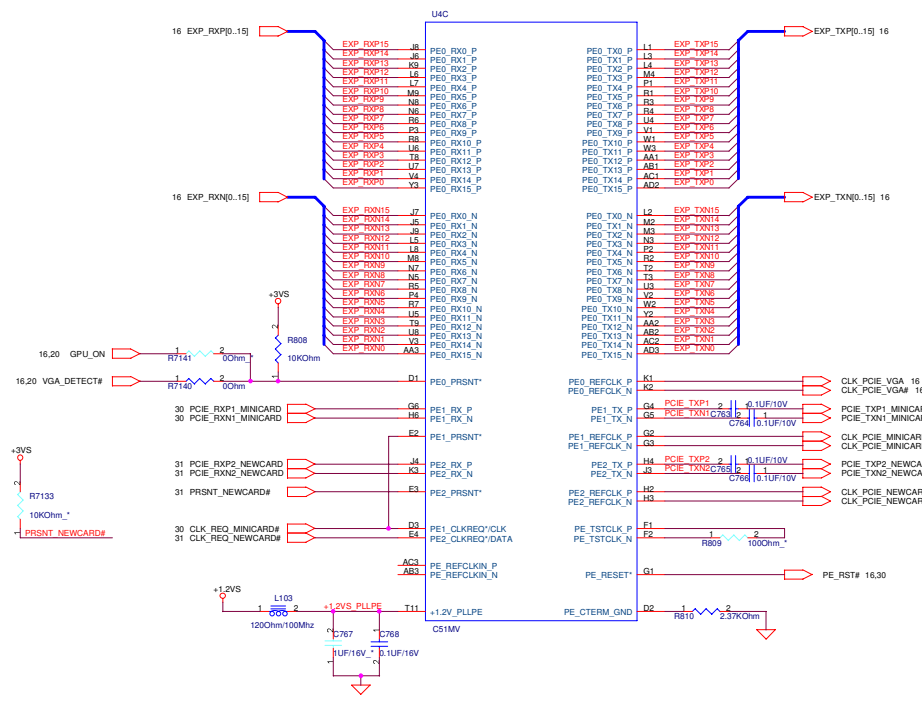


breakout: 5/5
normal: 5/10

Core Designs

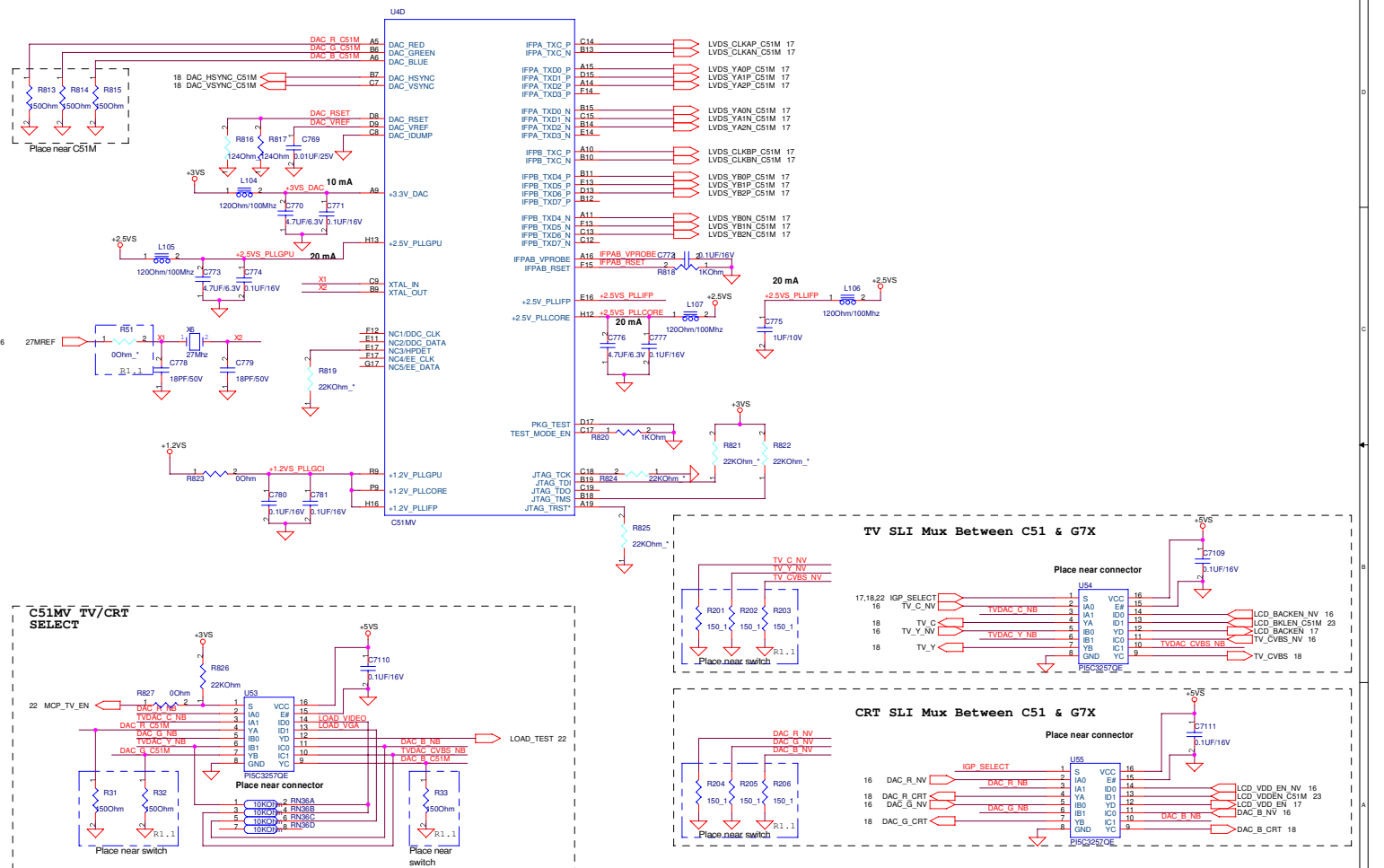
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			SHEET: 12			RELEASE DATE:	

<< Kennedy_Zhang >>



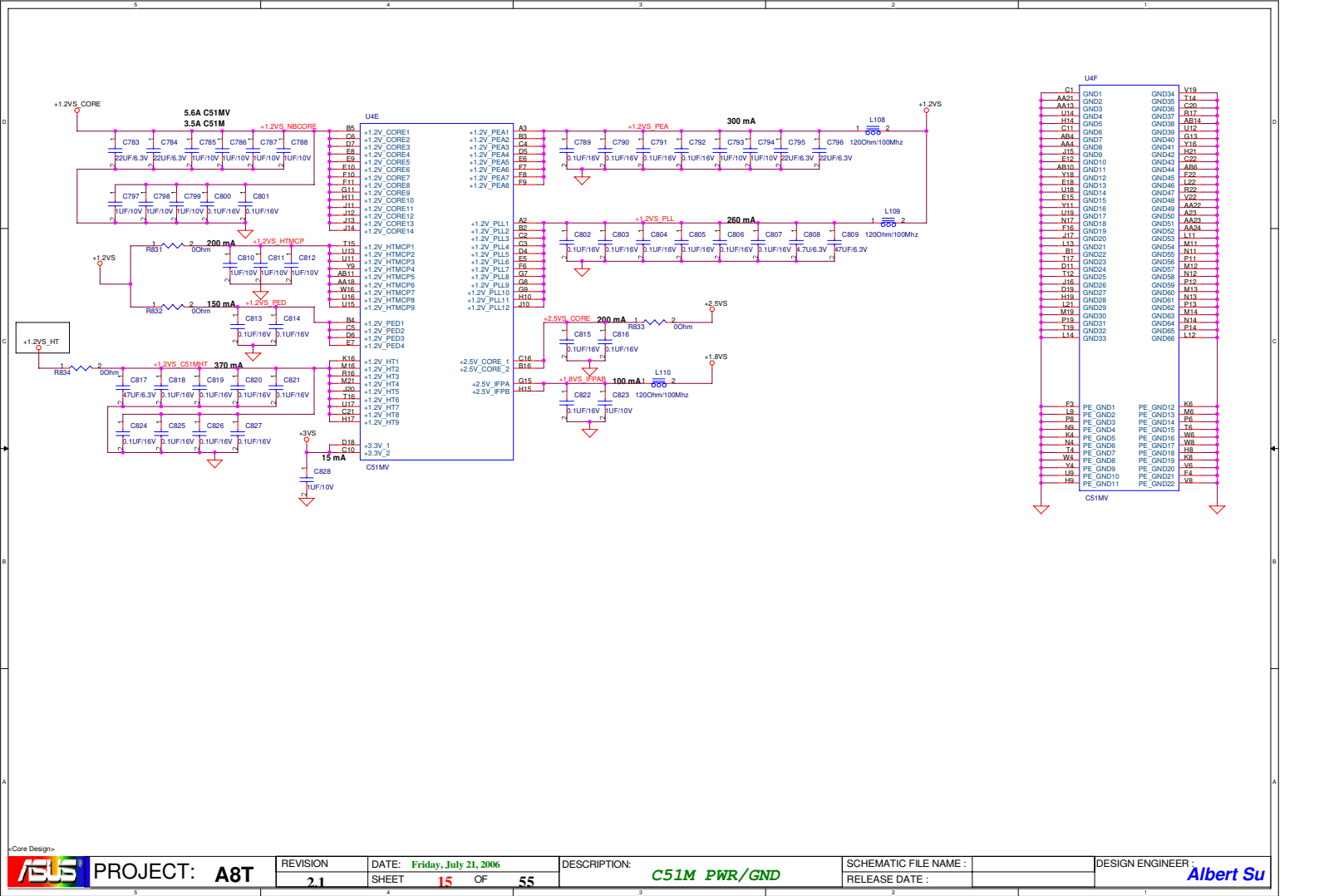
PROJECT: A8T		REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: C51M PCI-E	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		SHEET: 13 OF 55			RELEASE DATE:	

<< Kennedy_Zhang >>



ASUS	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: C51M CRT&LVDS	SCHMATIC FILE NAME: _____	DESIGN ENGINEER: Albert Su
		SHEET: 14 OF 55			RELEASE DATE: _____	

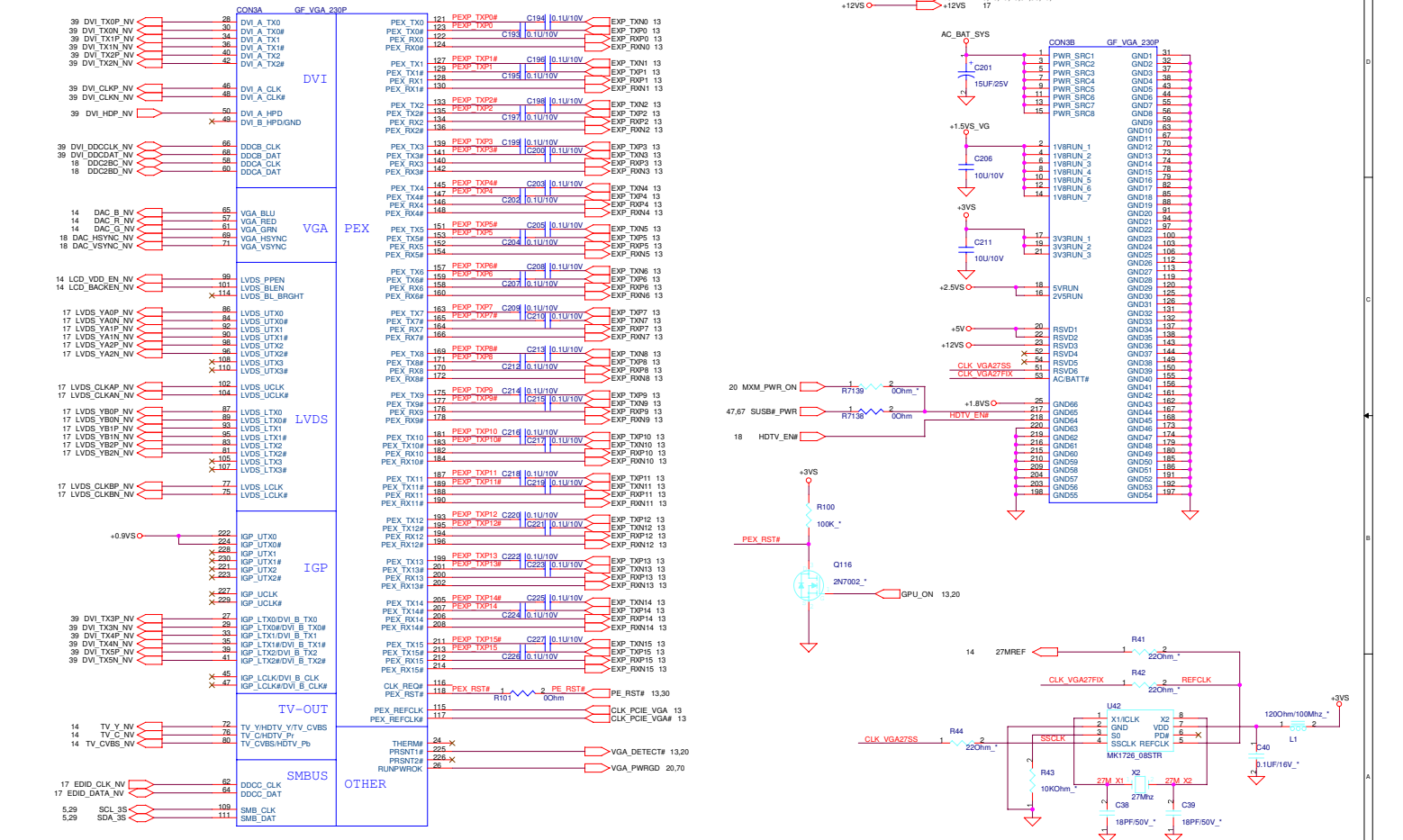
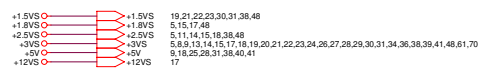
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ASUS PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: C51M PWR/GND	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
	SHEET: 15 OF 55			RELEASE DATE:	

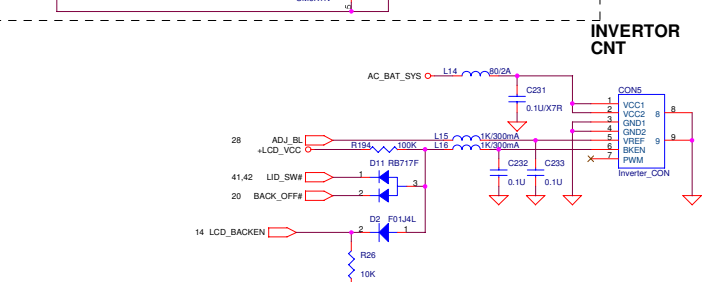
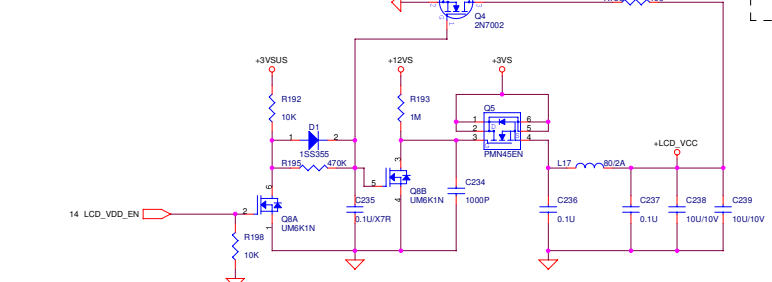
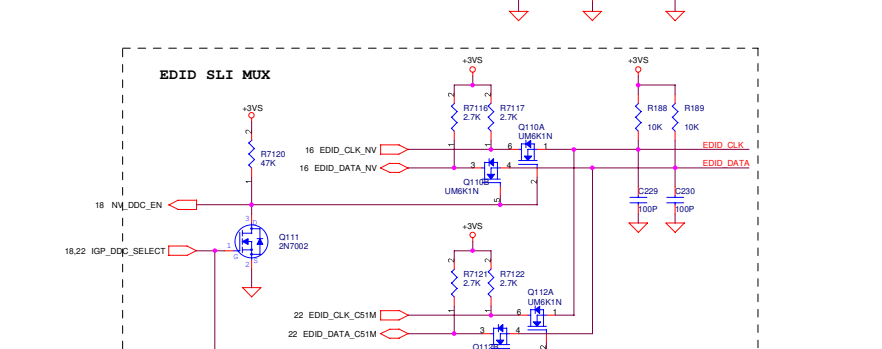
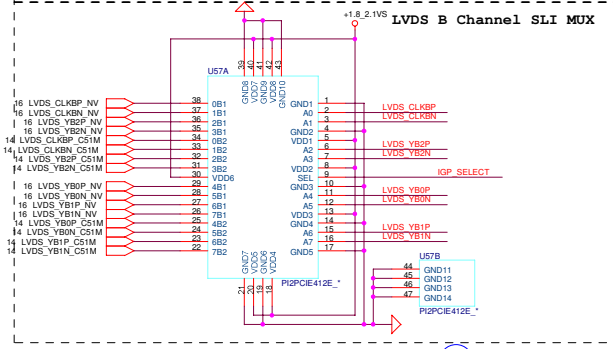
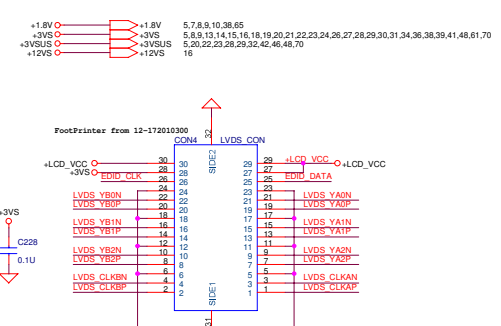
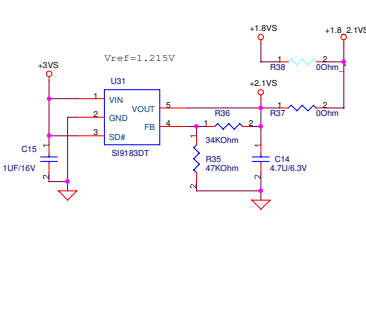
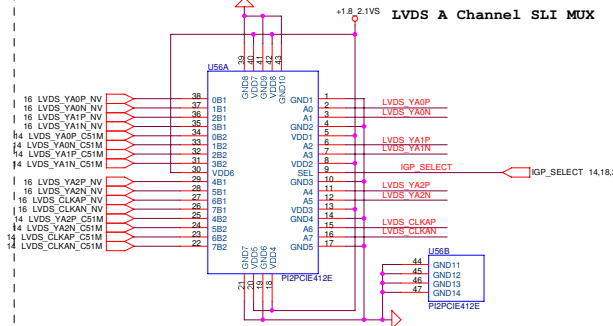
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Parity Inversion:
PEXP_TXP0, 1, 2, 4, 5,
6, 8, 14



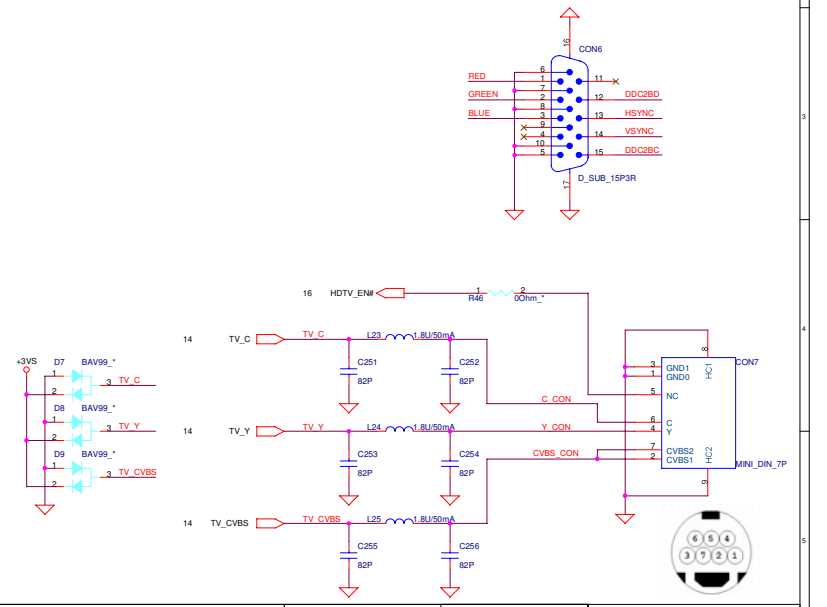
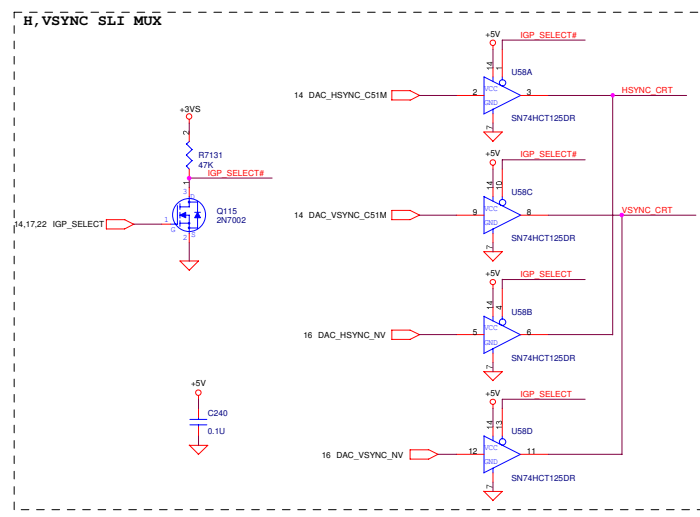
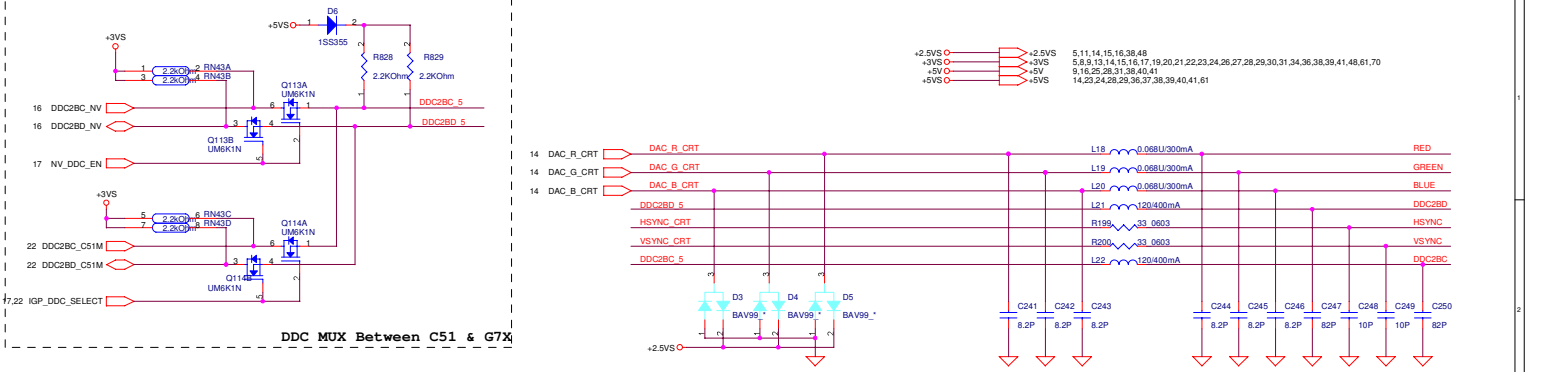
ASUS	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: VGA_CONN	SCHMATIC FILE NAME: _____	DESIGN ENGINEER: Albert Su
		SHEET 16 OF 55			RELEASE DATE: _____	

<< Kennedy_Zhang >>



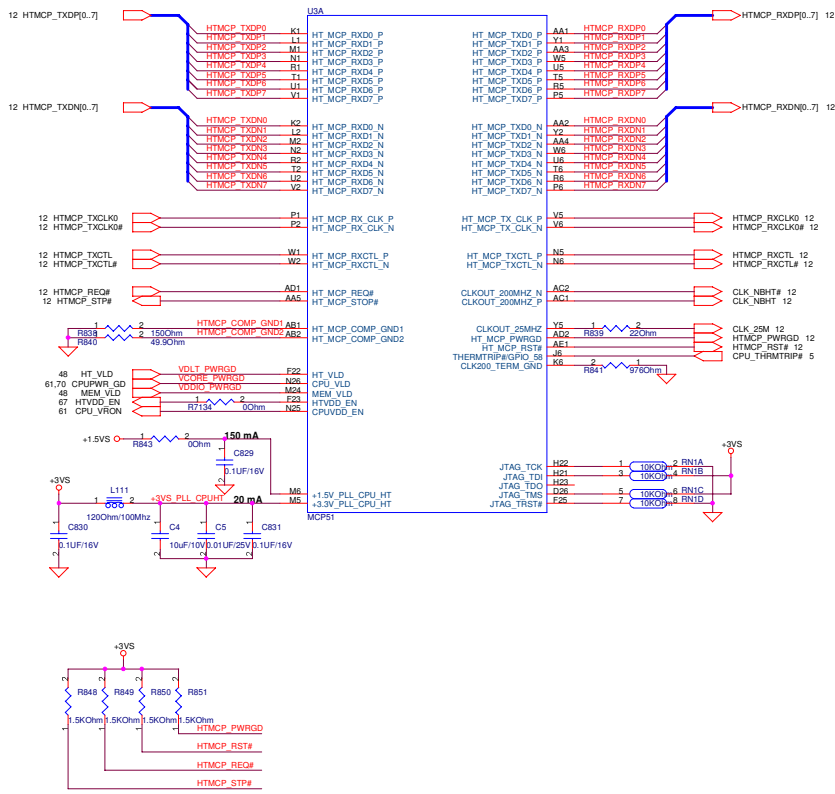
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			SHEET 17 OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>



ASUS	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: CRT & TV OUT	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		2.1	SHEET 18 OF 55		RELEASE DATE :	

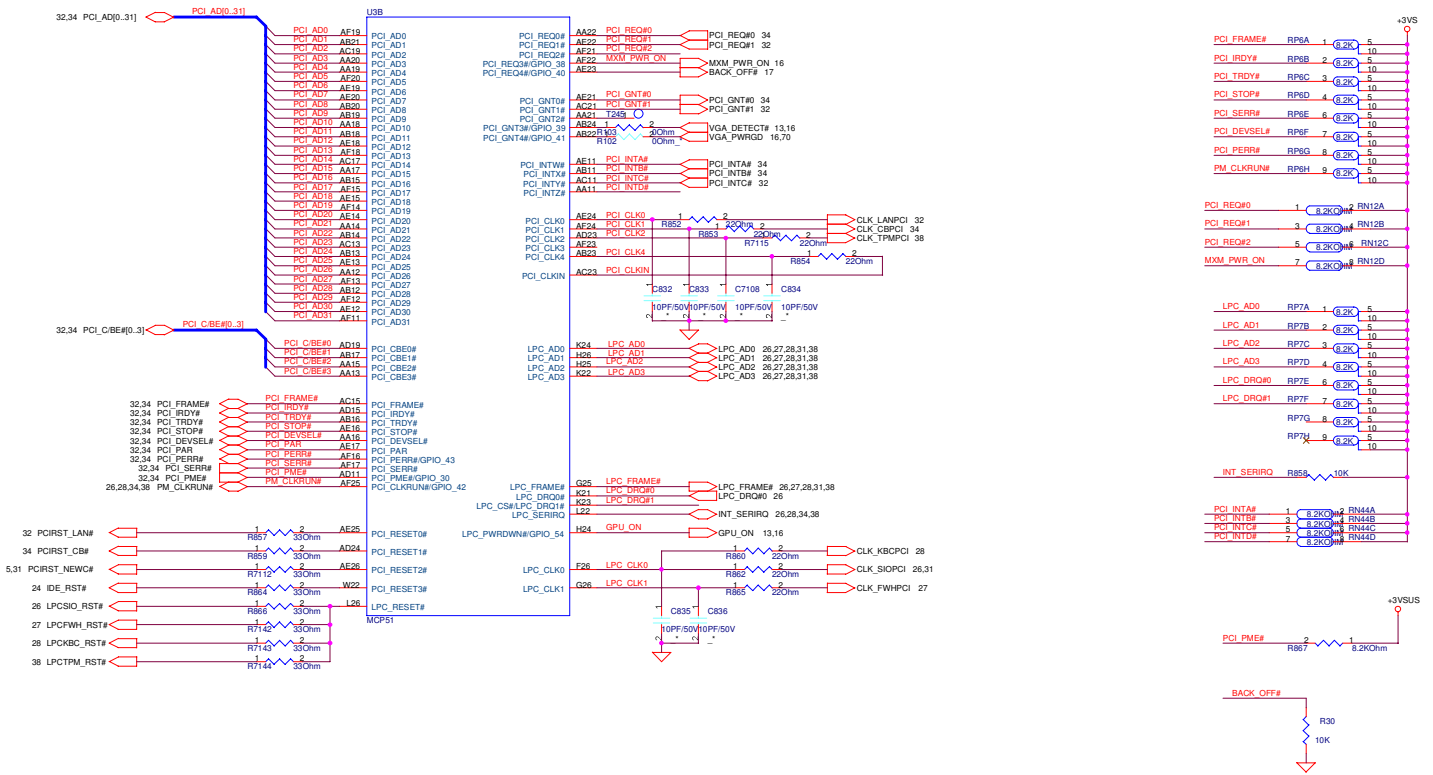
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Core Designs

	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 HT I/F	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		SHEET: 19 OF 55			RELEASE DATE:	

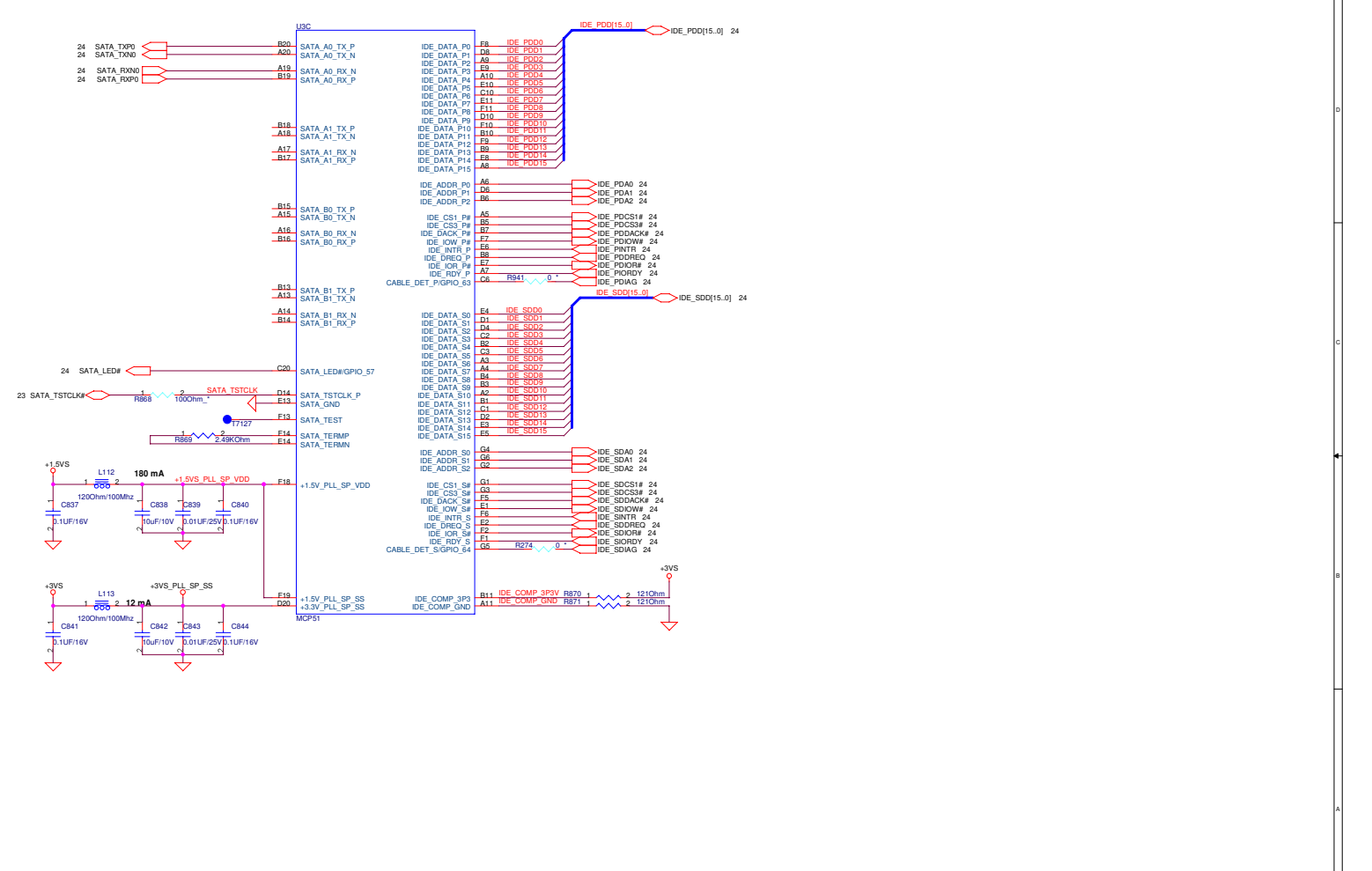
<< Kennedy_Zhang >>



Core Designs

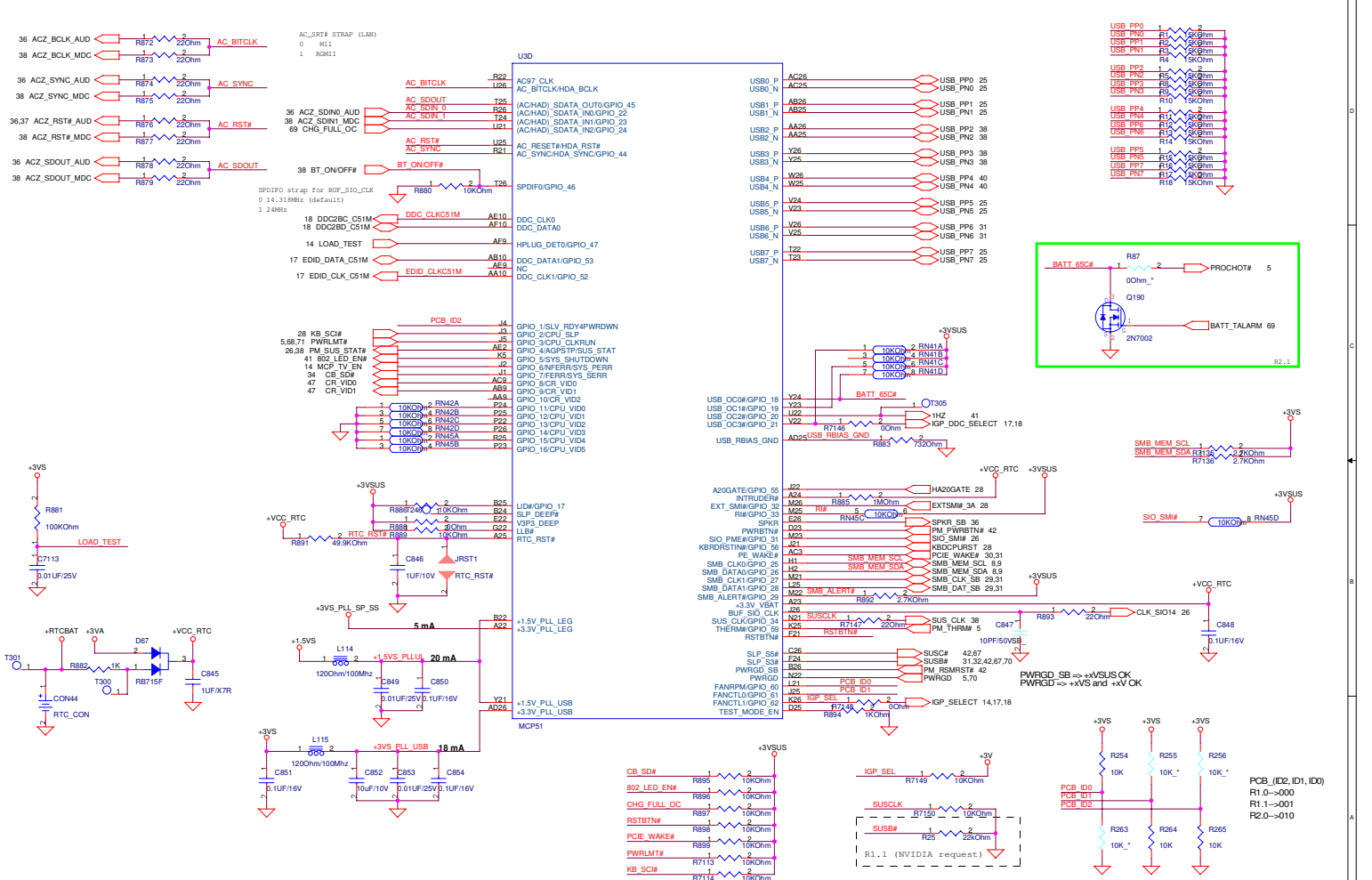
	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 PCI	SCHEMATIC FILE NAME: 	DESIGN ENGINEER: Albert Su
		SHEET: 20	OF: 55		RELEASE DATE: 	

<< Kennedy_Zhang >>



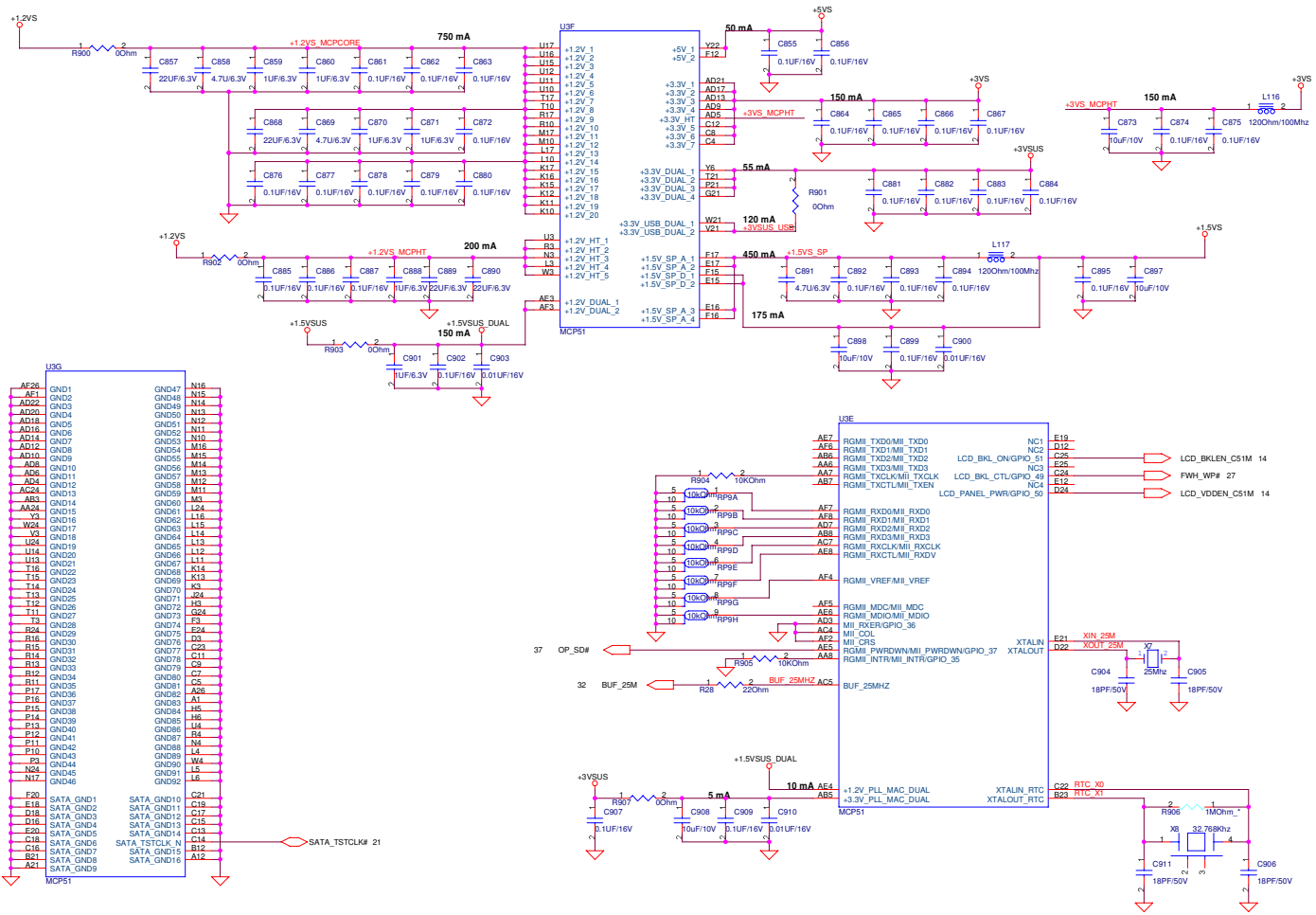
PROJECT: A8T		REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 IDE	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		SHEET 21 OF 55			RELEASE DATE :	

<< Kennedy_Zhang >>



ASUS	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MCP51 USB/HDA	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		SHEET: 22	OF: 55	RELEASE DATE:		

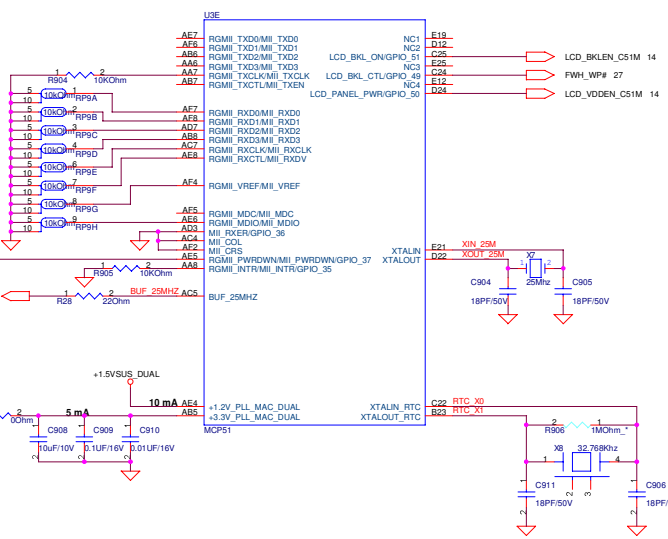
<< Kennedy_Zhang >>



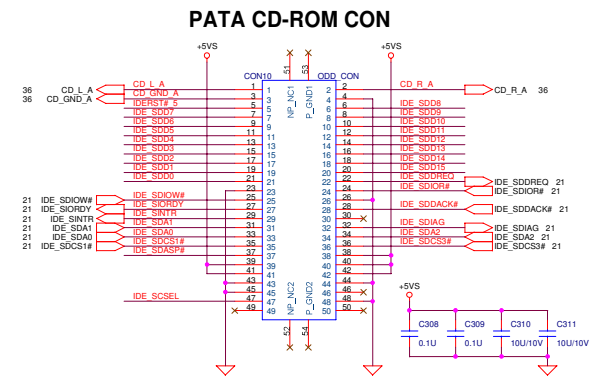
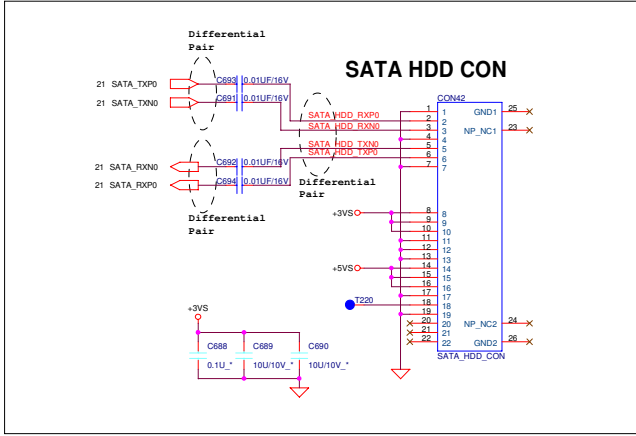
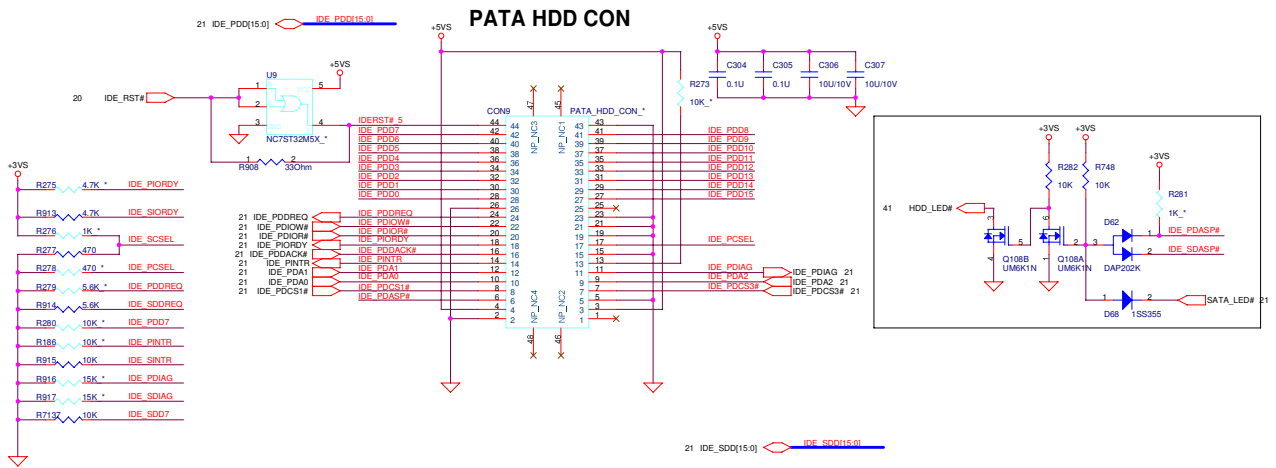
USG

AE26	GND1	NH6
AE1	GND2	NH5
AD22	GND3	NH4
GND4	NH3	
AD16	GND5	NH2
AD18	GND6	NH1
AD12	GND7	NH0
AD14	GND8	MH6
AD10	GND9	MH5
GND10	MH4	
AD5	GND11	MH3
AD4	GND12	MH2
AC24	GND13	MH1
AS	GND14	MH0
AA4	GND15	LH6
LH	GND16	LH5
W24	GND17	LH4
Y4	GND18	LH3
U8	GND19	LH2
LH4	GND20	LH1
LH5	GND21	LH0
T6	GND22	KH6
GND23	KH5	
GND24	KH4	
L14	GND25	KH3
GND26	KH2	
GND27	KH1	
R24	GND28	JH6
R16	GND29	JH5
R14	GND30	JH4
GND31	JH3	
R15	GND32	JH2
R16	GND33	JH1
R12	GND34	IH6
GND35	IH5	
P17	GND36	IH4
P16	GND37	IH3
P15	GND38	IH2
P14	GND39	IH1
P15	GND40	IH0
P12	GND41	GH6
P11	GND42	GH5
P10	GND43	GH4
P9	GND44	GH3
N24	GND45	GH2
GND46	GH1	
F20	SATA_GND1	C21
D18	SATA_GND2	C19
D16	SATA_GND3	C17
D16	SATA_GND4	C15
E20	SATA_GND5	C13
C16	SATA_GND6	C14
C16	SATA_GND7	C14
B21	SATA_GND8	B12
AE1	SATA_GND9	A12

MCP51



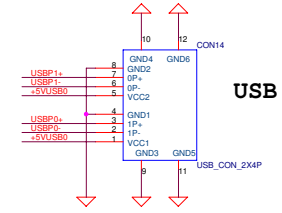
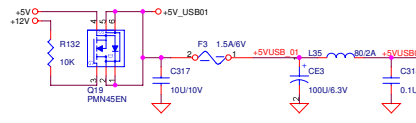
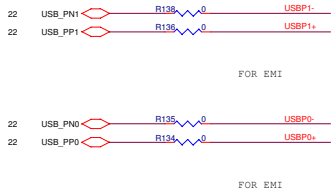
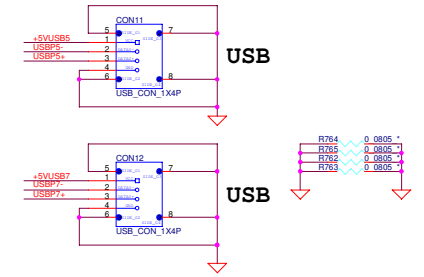
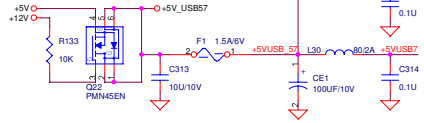
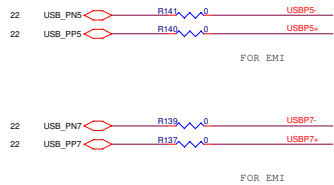
<< Kennedy_Zhang >>



- +3VS ○ → +3VS 5,8,9,13,14,15,16,17,18,19,20,21,22,23,26,27,28,29,30,31,34,36,38,39,41,48,61,70
- +5VS ○ → +5VS 14,16,23,28,29,36,37,38,39,40,41,61
- +5V ○ → +5V 9,16,18,25,28,31,38,40,41

ASUS PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: HDD & CD-ROM CONN	SCHMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
	2.1	SHEET 24 OF 55		RELEASE DATE:	

« Kennedy_Zhang »



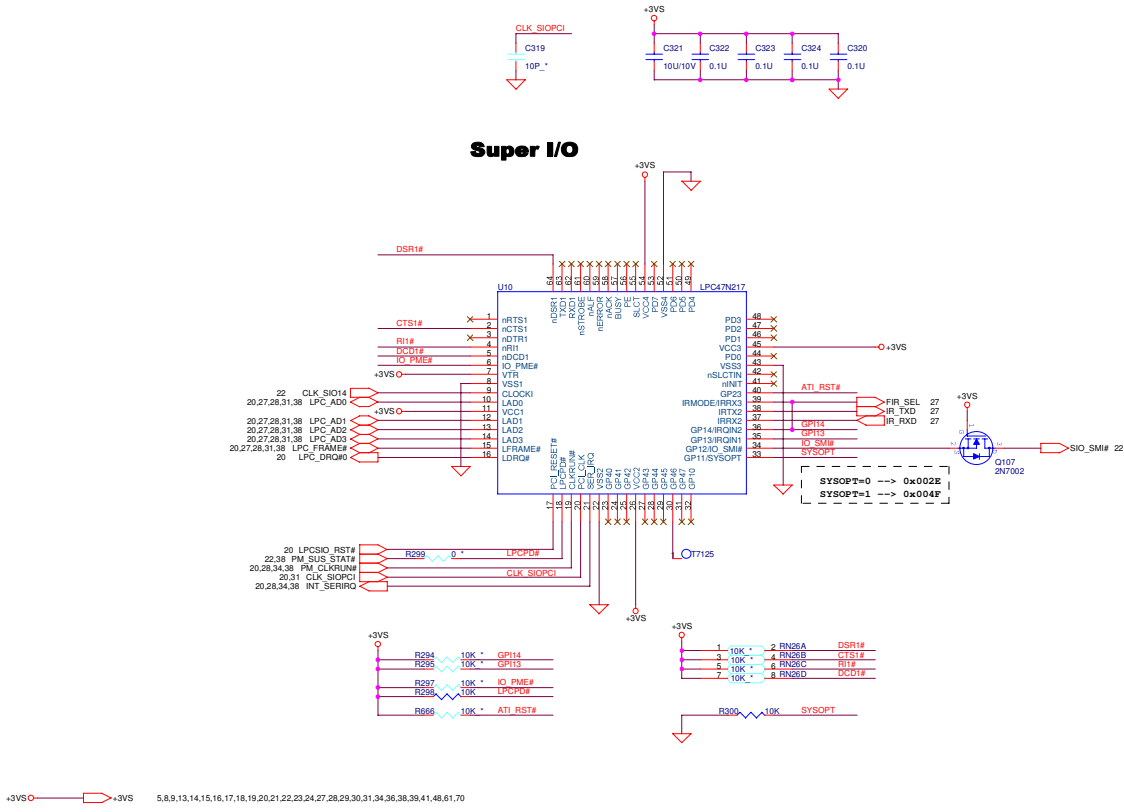
+5V → +5V 9,16,18,28,31,38,40,41

Core Design

	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: USB PORTS	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		2.1	SHEET 25 OF 55		RELEASE DATE:	

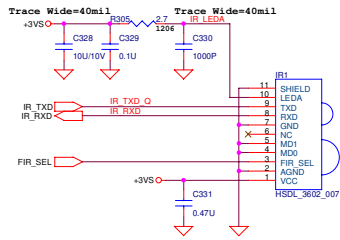
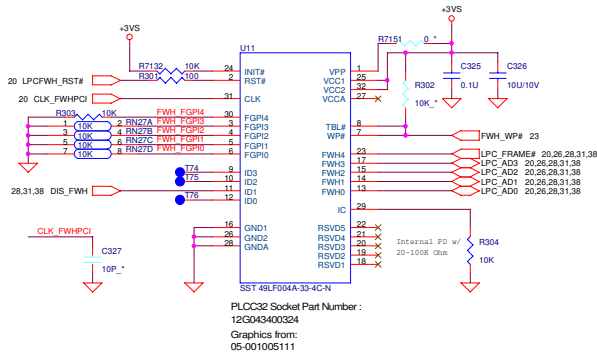
<< Kennedy_Zhang >>

Super I/O



Core Design		PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: SUPER IO LPC47N217	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
			SHEET: 26	OF: 55		RELEASE DATE:	

<< Kennedy_Zhang >>



+3VS → +3VS 5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,26,28,29,30,31,34,36,38,39,41,48,61,70

Core Designs

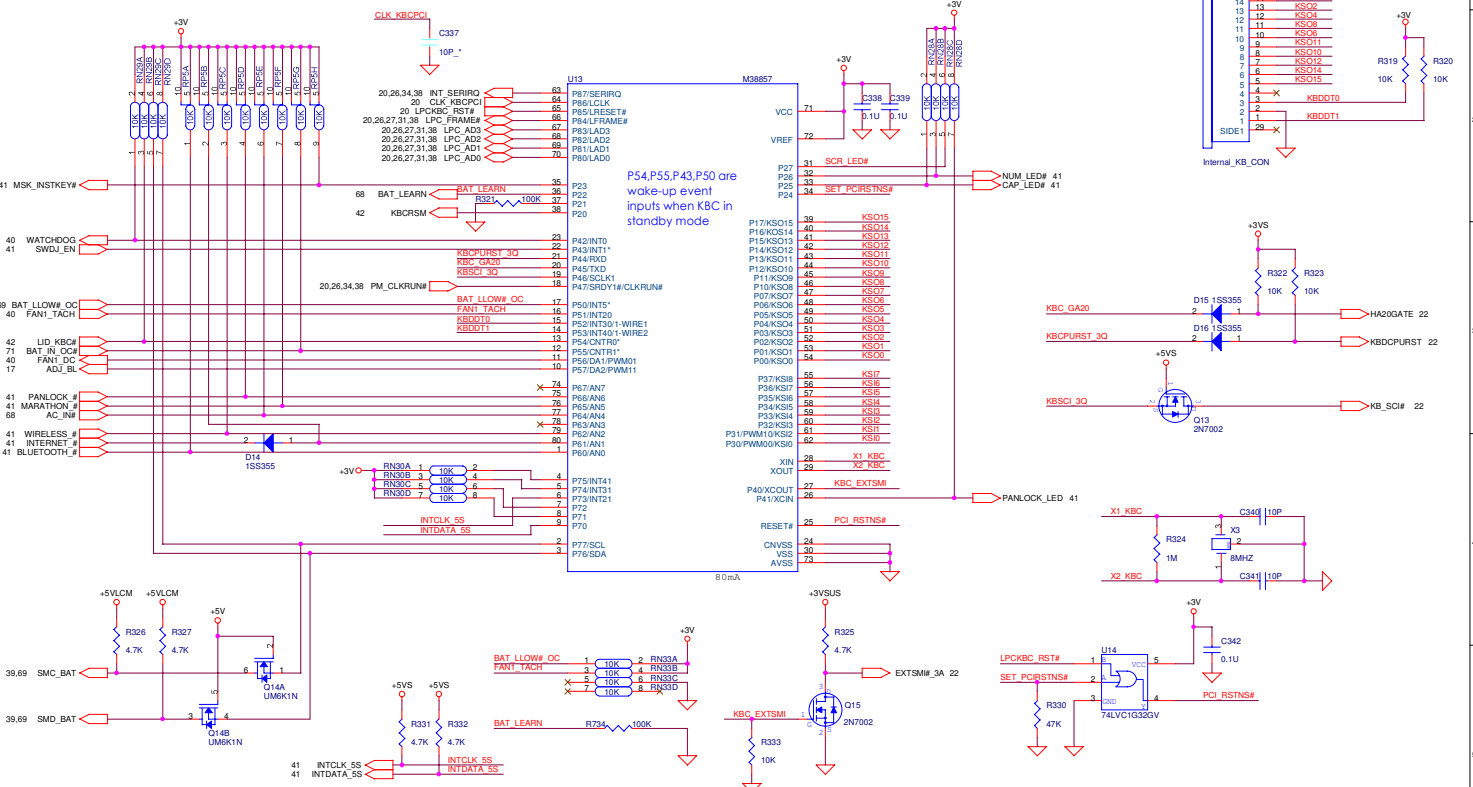
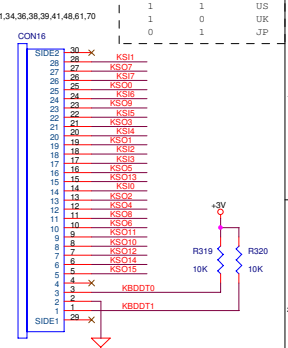
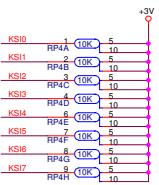
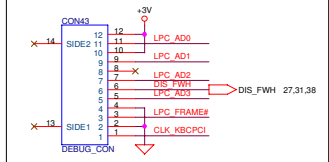
	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: BIOS , IR	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
		2.1	SHEET 27 OF 55		RELEASE DATE :	

<< Kennedy_Zhang >>

P2.1 Low : Power Button Override disable
 Input Event only at P54, P55, P60 - P67

P50, P43, P54, P55 are wake-up event
 inputs when KBC in standby mode

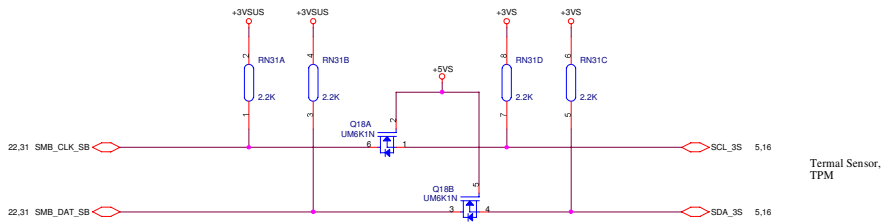
EC should set
 OP_SD low in S3,
 keep from
 leakage



ASUS	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: KBC 38857	SHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		SHEET 28 OF 55			RELEASE DATE:	

<< Kennedy_Zhang >>

MCP51

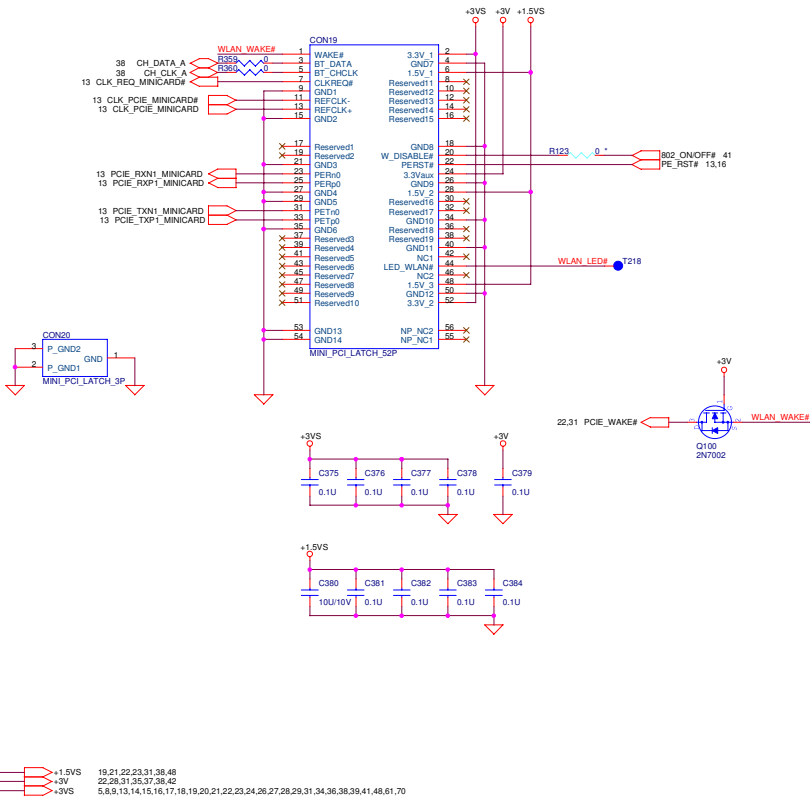


+3VA	→	+3VA	22,38,41,42,48,71
+3VSUS	→	+3VSUS	5,17,20,22,23,28,32,42,46,48,70
+0.9VS	→	+0.9VS	16
+1.5VS	→	+1.5VS	19,21,22,23,30,31,38,48
+2.5VSC	→	+2.5VSC	5,11,14,15,16,18,38,48
+3VS	→	+3VS	5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,30,31,34,38,39,41,48,61,70
+5VS	→	+5VS	14,18,23,24,28,36,37,38,39,40,41,61
+12VS	→	+12VS	16,17
+1.8V	→	+1.8V	5,7,8,9,10,38,65
+3V	→	+3V	22,28,30,31,35,37,38,42
+5V	→	+5V	9,16,18,25,28,31,38,40,41
+12V	→	+12V	25,40
+VCCORE	→	+VCCORE	5,7,61
+5VLCM	→	+5VLCM	28,68,69,70,71

Core Designs

	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: SM BUS & POWER PORT	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		2.1	SHEET 29 OF 55		RELEASE DATE :	Albert Su

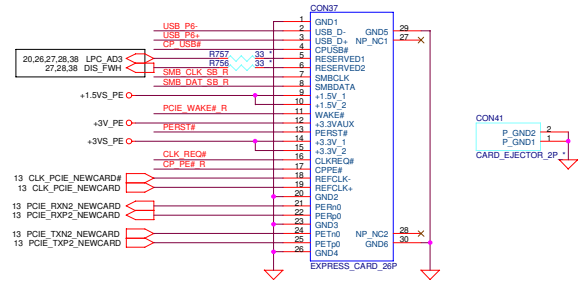
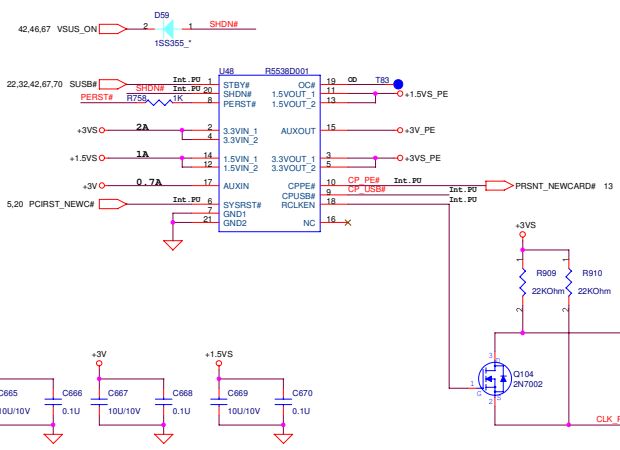
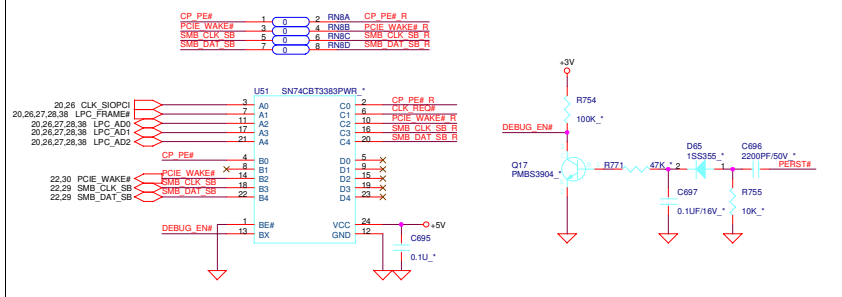
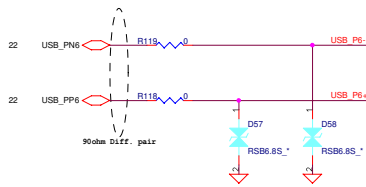
<< Kennedy_Zhang >>



+1.5VS → +1.5VS 19,21,22,23,31,38,48
 +3V → +3V 22,28,31,35,37,38,42
 +3VS → +3VS 5,6,8,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,29,31,34,36,38,39,41,48,61,70

ASUS PROJECT: A8T		REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: MINI CARD	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		SHEET: 30	OF: 55		RELEASE DATE:	

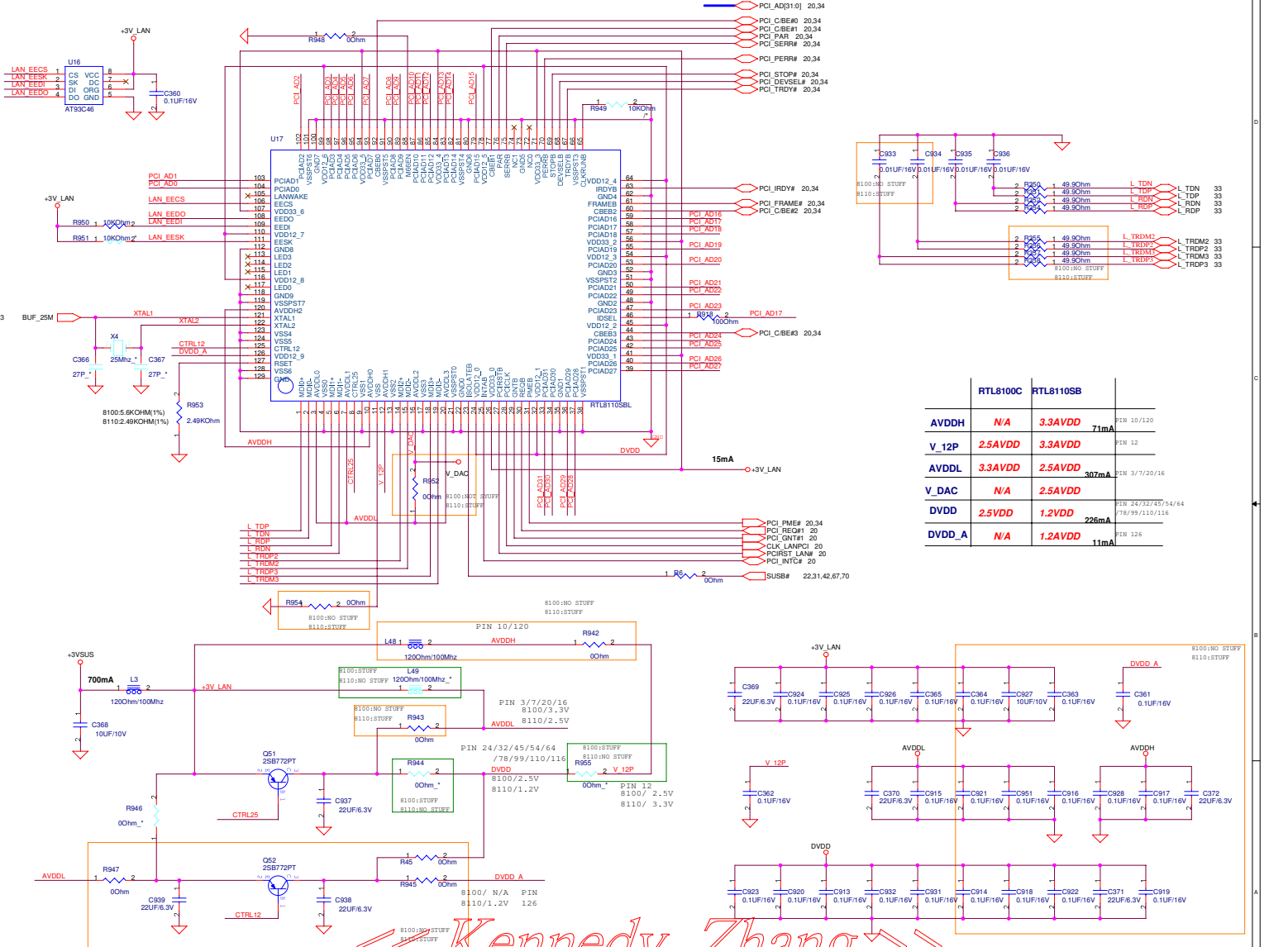
<< Kennedy_Zhang >>



+1.5V_C	+1.5V	19,21,22,23,30,38,48
+3V_C	+3V	5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,29,30,34,36,38,39,41,48,61,70
+3V_C	+3V	22,28,30,35,37,38,42

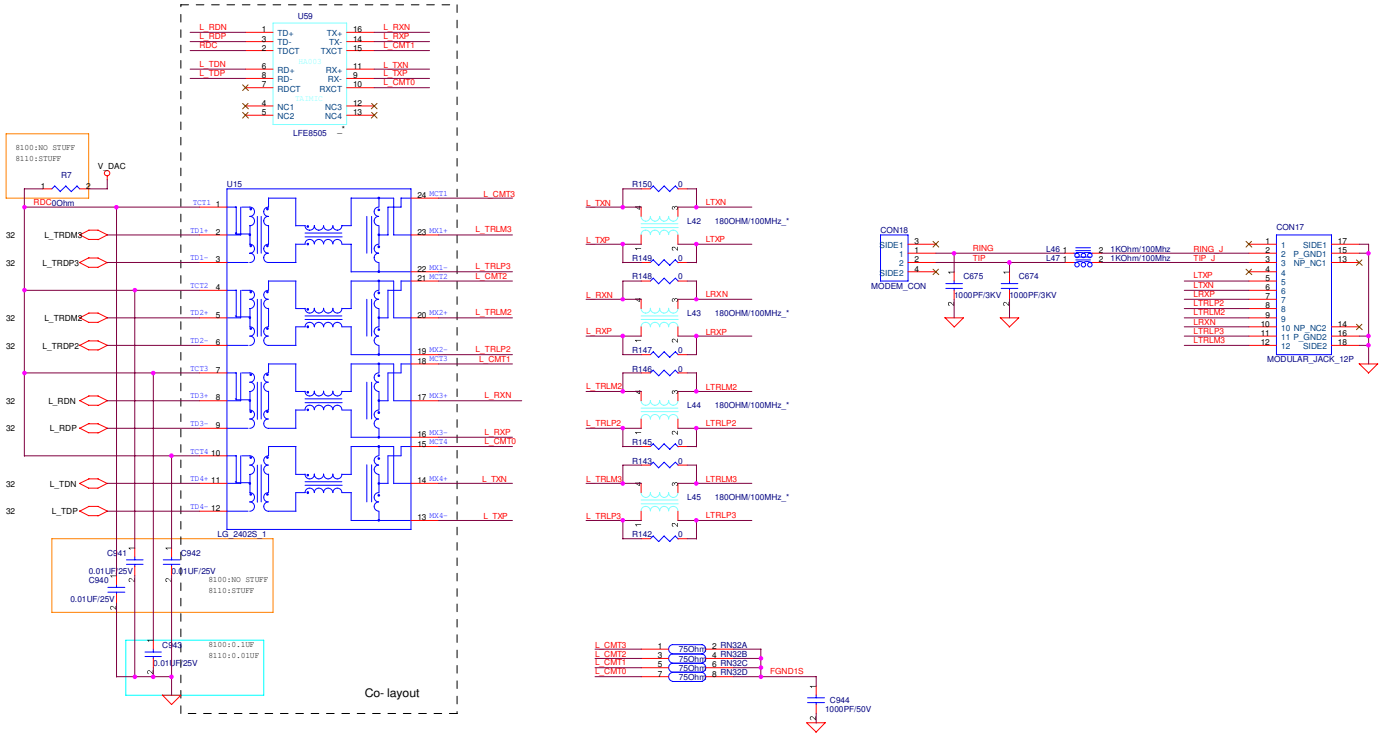
ASUS PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: NEW CARD	SCHEMATIC FILE NAME: _____	DESIGN ENGINEER: Albert Su
	SHEET: 31	OF: 55	RELEASE DATE: _____		

<< Kennedy_Zhang >>



	RTL8100C	RTL8110SB	
AVDDH	N/A	3.3AVDD	PIN 10/120
V_12P	2.5AVDD	3.3AVDD	PIN 12
AVDDL	3.3AVDD	2.5AVDD	307mA PIN 3/7/20/16
V_DAC	N/A	2.5AVDD	
DVDD	2.5VDD	1.2VDD	226mA PIN 24/32/45/54/64 78/99/110/116
DVDD_A	N/A	1.2AVDD	11mA PIN 126

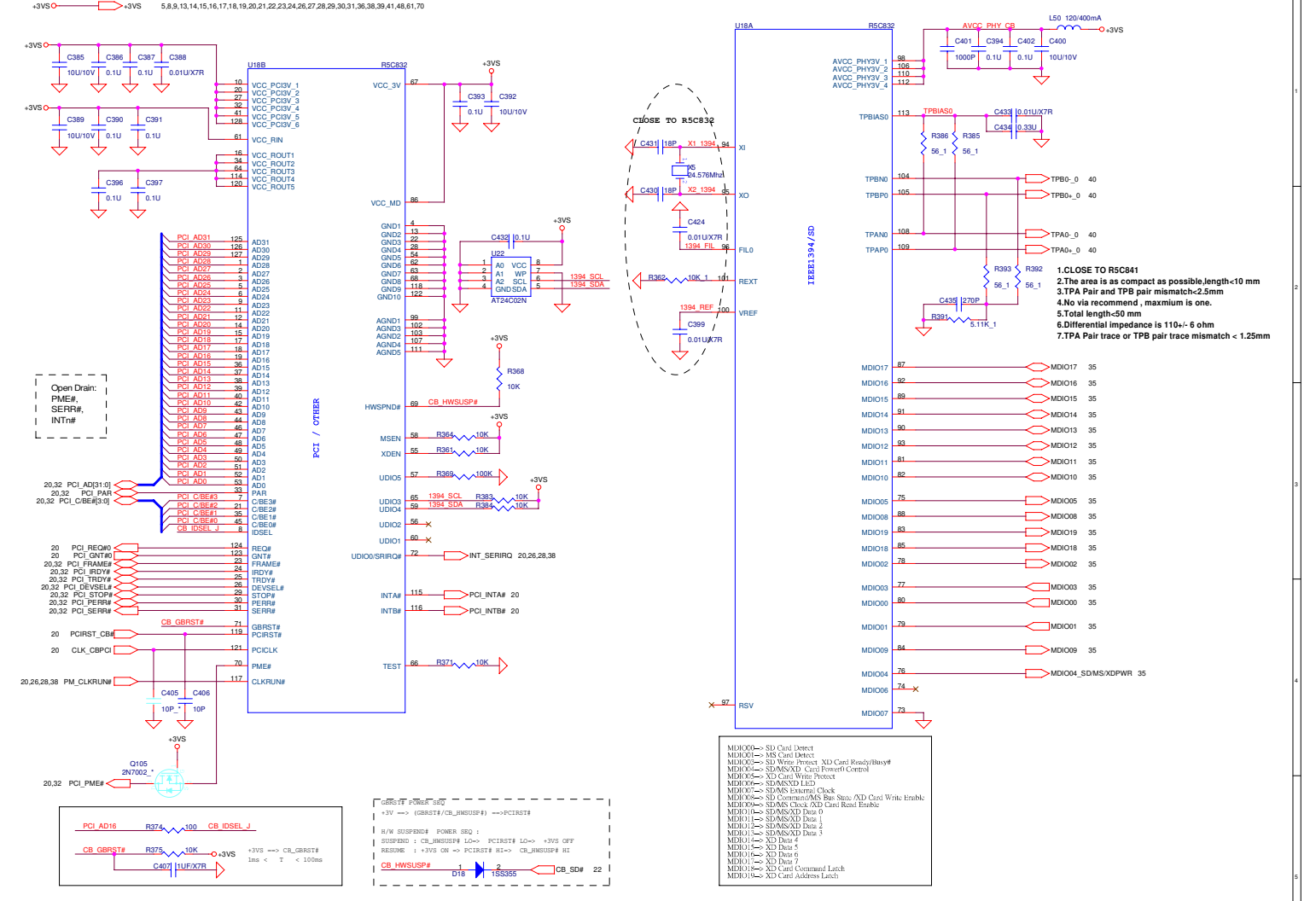
Kennedy Zhang

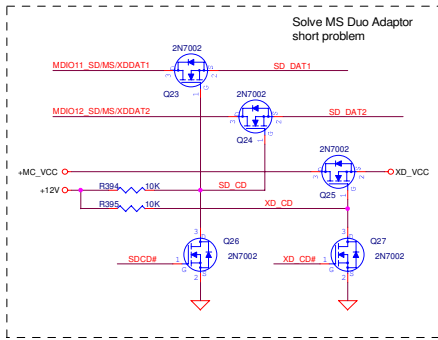
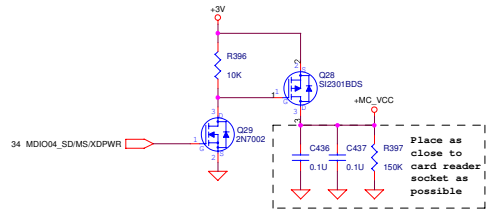


Core Design

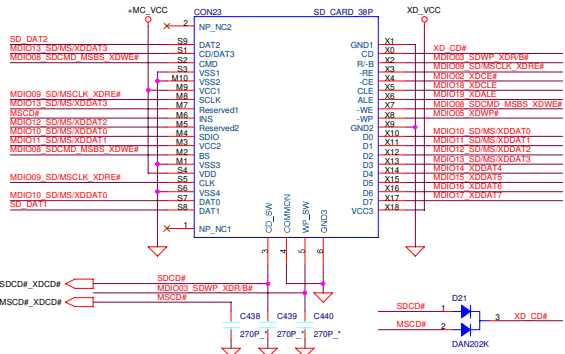
	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: RJ45 & RJ11	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
			SHEET: 33 OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>





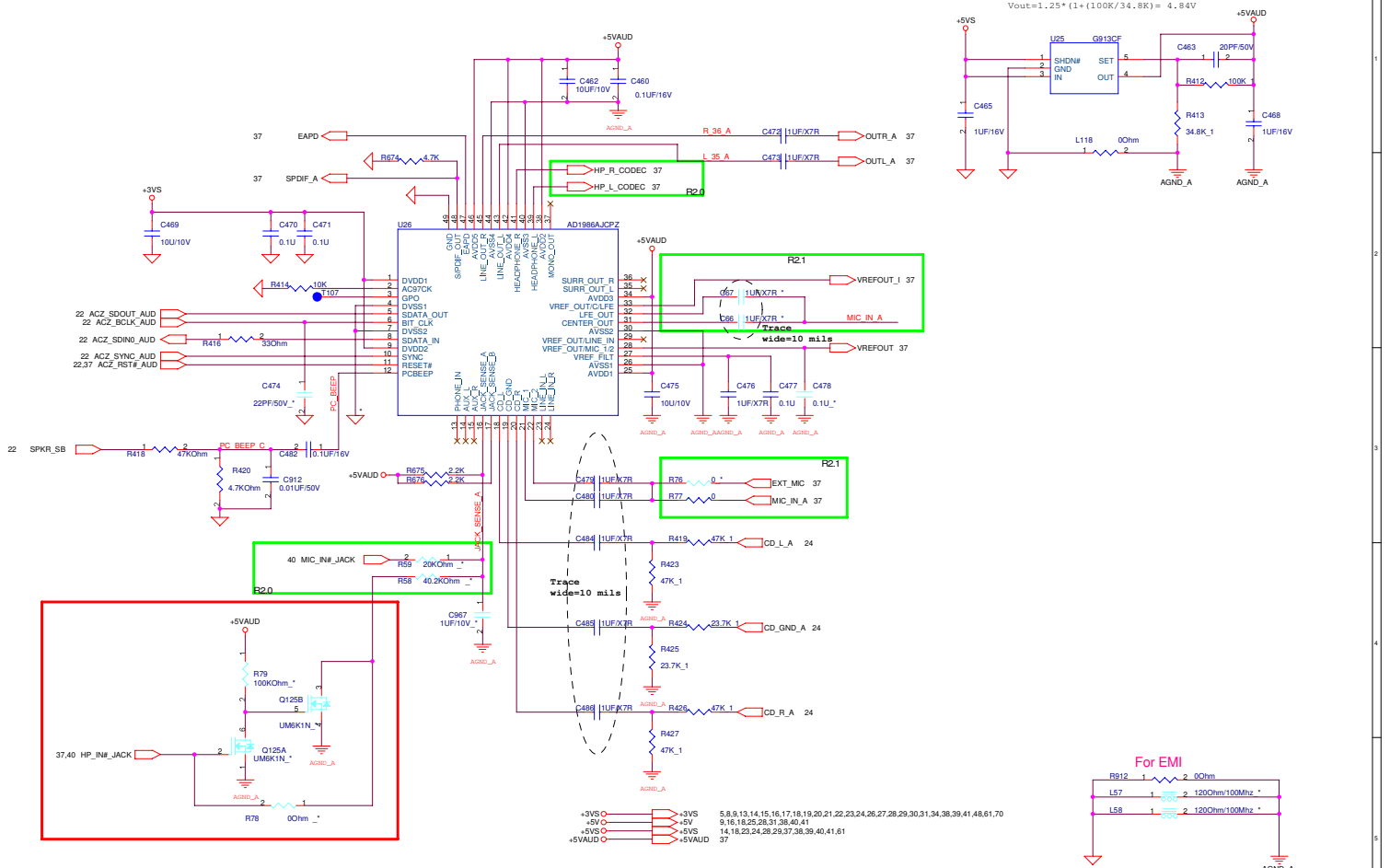
+3V O → +3V 22,28,30,31,37,38,42
 +12V O → +12V 25,37,40,67



<Core Design>

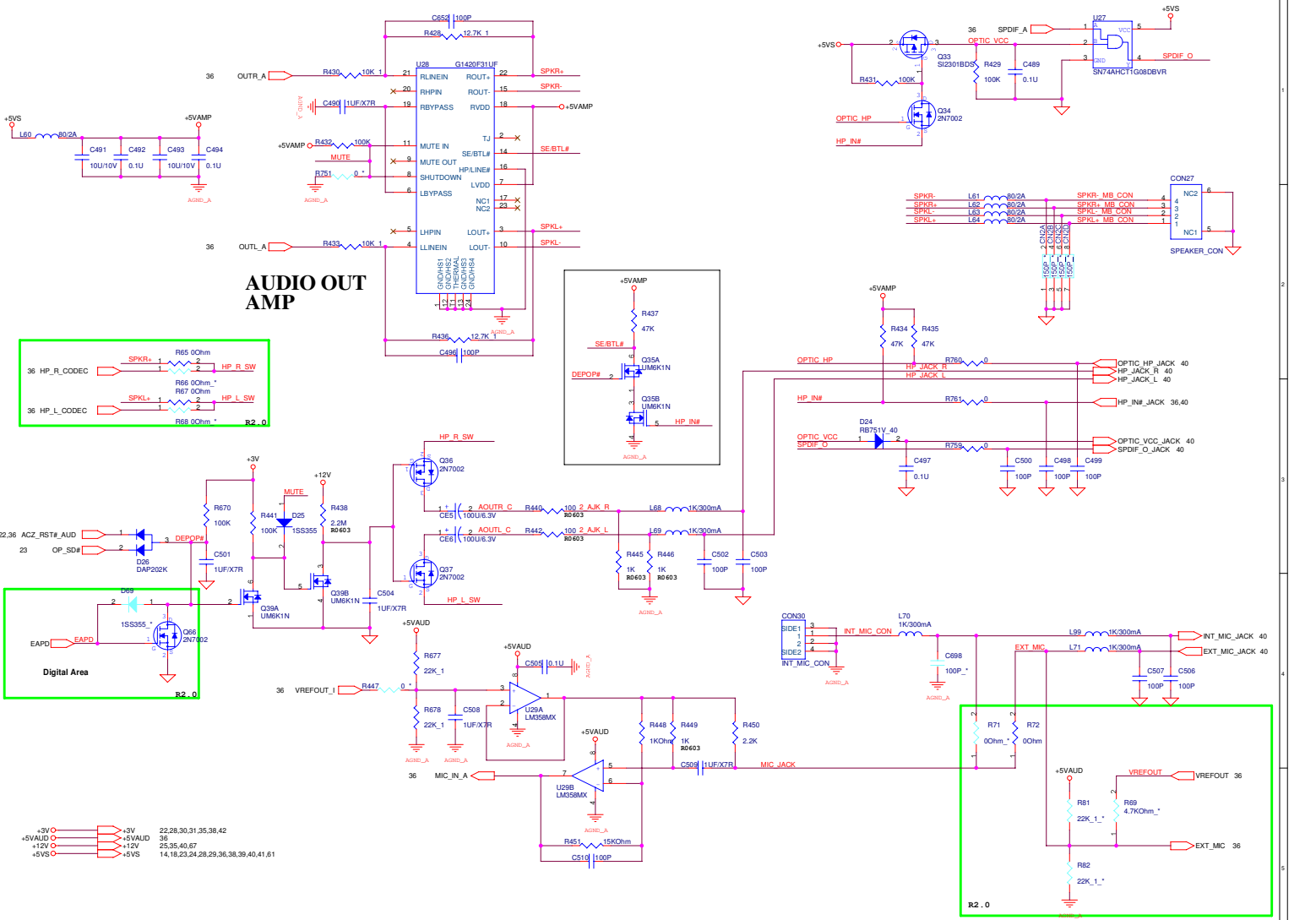
	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: 4 IN 1 CONN	SCHMATIC FILE NAME: _____	DESIGN ENGINEER: Albert Su
			SHEET 35 OF 55		RELEASE DATE: _____	

<< Kennedy_Zhang >>

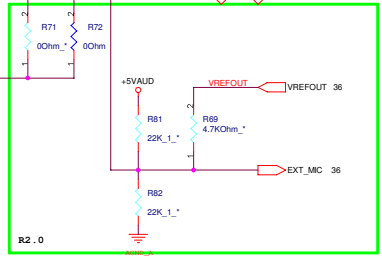
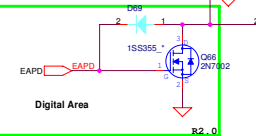
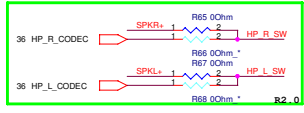


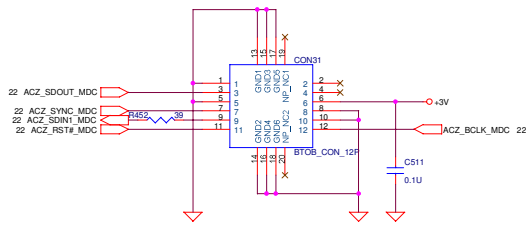
Core Design:		PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: CODEC_ADI1986A	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
			SHEET: 36	OF: 55		RELEASE DATE:	

<< Kennedy_Zhang >>

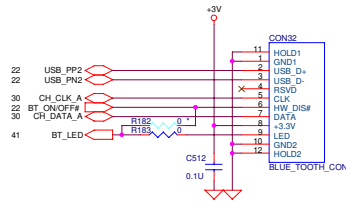


AUDIO OUT AMP

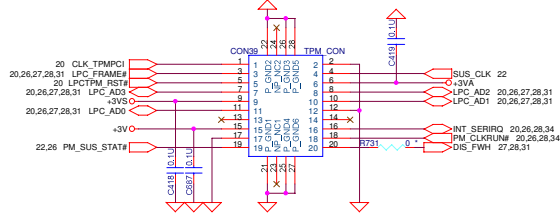




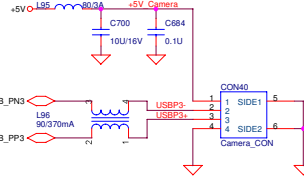
Azalia MDC MODEM CON



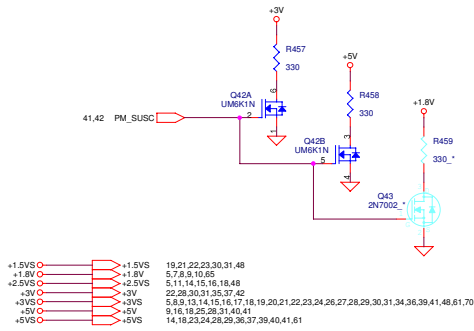
Bluetooth Module CON



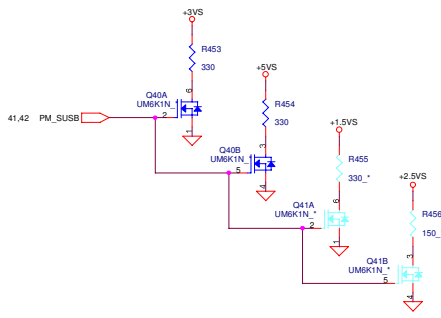
TPM Module CON



Camera Module CON



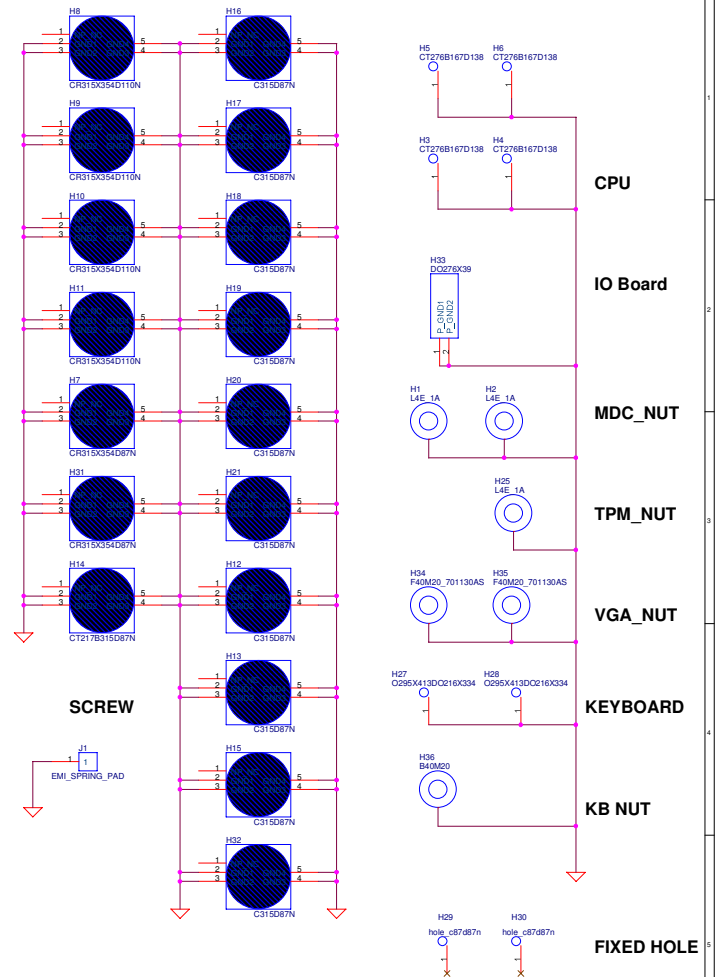
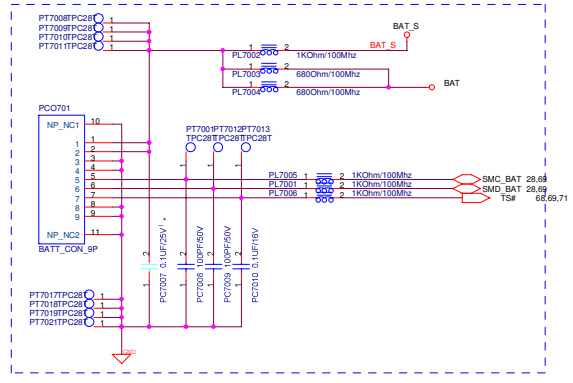
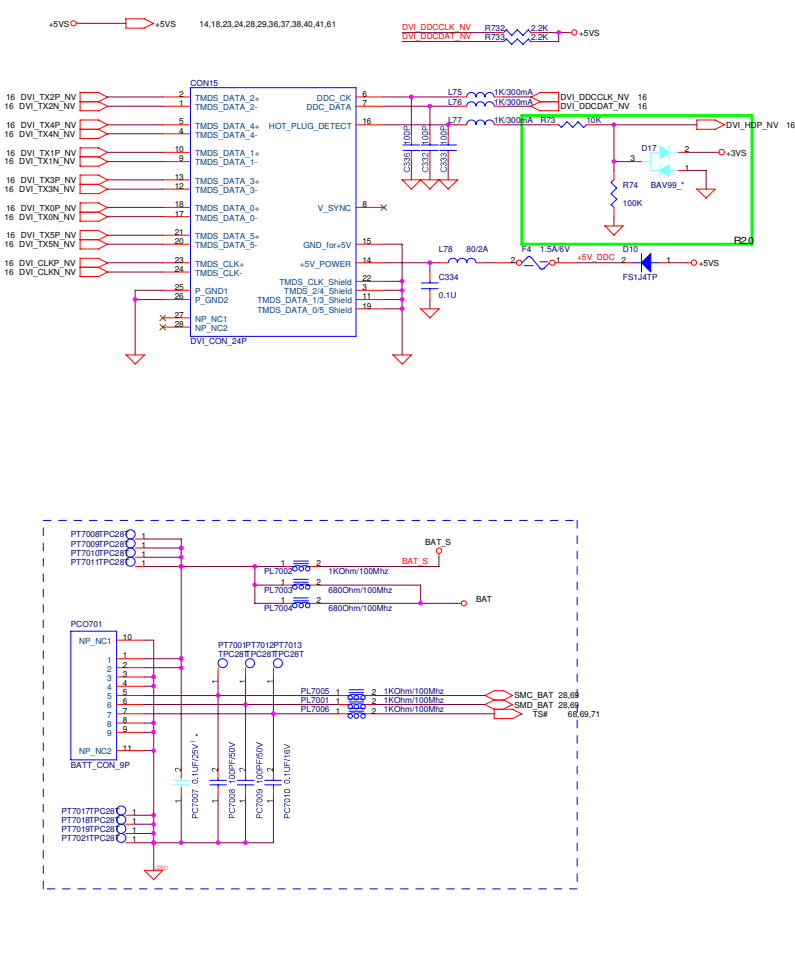
+1.5VS	+1.5V	19,21,22,23,30,31,48
+1.8V	+1.8V	5,7,8,9,10,65
+2.5VS	+2.5V	5,11,14,15,16,18,48
+3V	+3V	22,28,30,31,35,37,42
+3VS	+3V	5,8,9,13,14,15,16,17,18,19,20,21,22,23,24,26,27,28,29,30,31,34,36,39,41,48,61,70
+5V	+5V	3,16,18,25,28,31,40,41
+5VS	+5V	14,18,23,24,28,29,36,37,39,40,41,61



Core Design

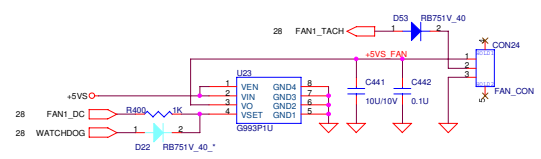
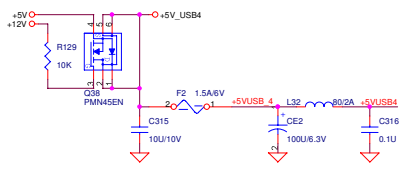
ASUS PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION:	SCHMATIC FILE NAME :	DESIGN ENGINEER :
	2.1	SHEET 38 OF 55	MDC, B/T, TPM, Camera & DISCHG	RELEASE DATE :	Albert Su

<< Kennedy_Zhang >>

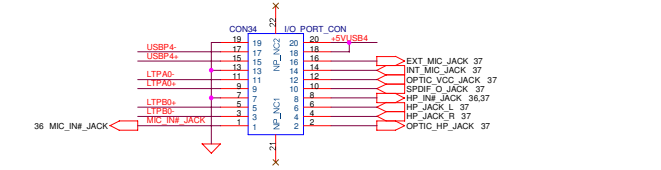
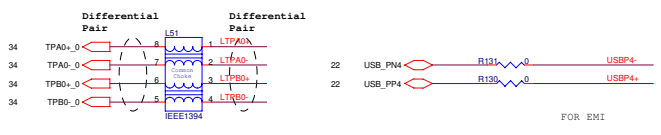


PROJECT: A8T		REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: DVI CONN & HOLE	SCHMATIC FILE NAME: _____	DESIGN ENGINEER: Albert Su
		SHEET: 39	OF: 55		RELEASE DATE: _____	

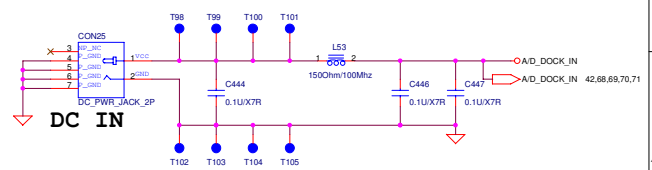
<< Kennedy_Zhang >>



FAN CONTROL



I/O PORT

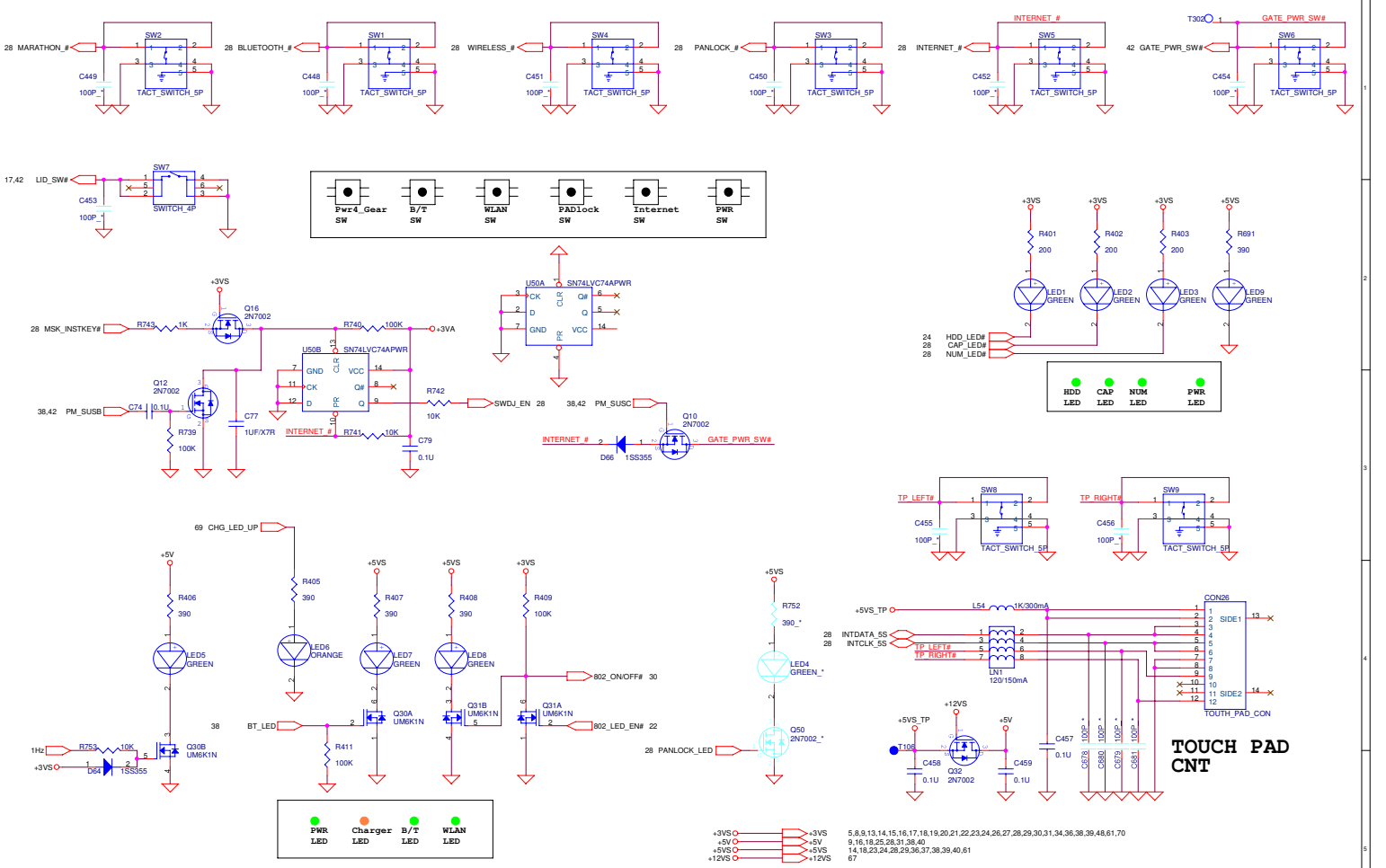


ACIN_CONN

+5V 9,16,18,25,28,31,38,41
+5VS 14,16,23,24,28,29,36,37,38,39,41,61

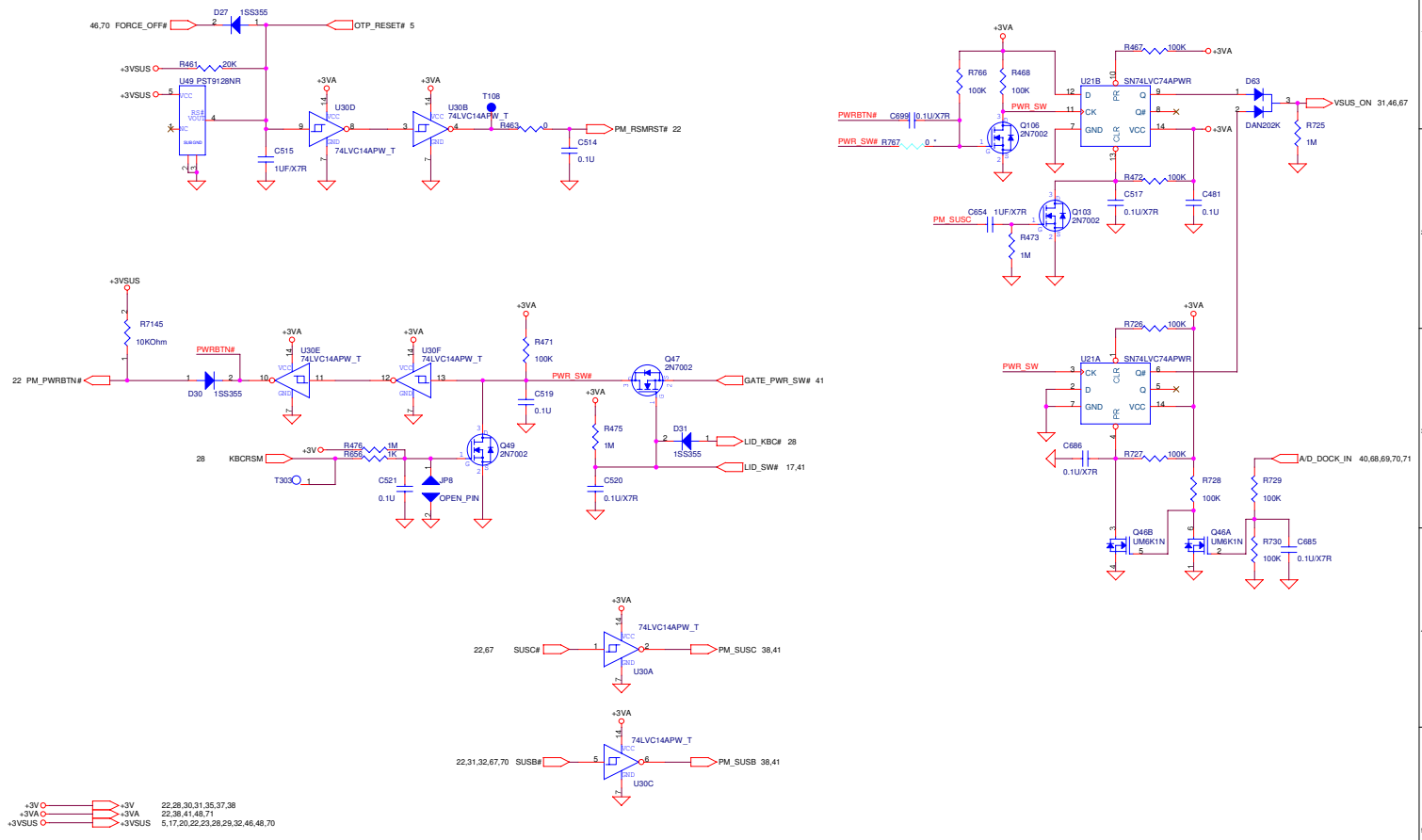
ASUS	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: FAN_CTRL & ACIN	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		2.1	SHEET 40 OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>



ASUS	PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: SW & LED & TP	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
		2.1	SHEET 41 OF 55		RELEASE DATE:	

<< Kennedy_Zhang >>



+3V → 22.28,30.31,35,37,38
 +3VA → 22.38,41,45,71
 +3VUSUS → 5,17,20,22,23,28,29,32,46,48,70

ASUS PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: POWER-ON SEQUENCE	SCHEMATIC FILE NAME:	DESIGN ENGINEER: Albert Su
	2.1	SHEET 42 OF 55		RELEASE DATE:	


<< Kennedy_Zhang >>

Revision History

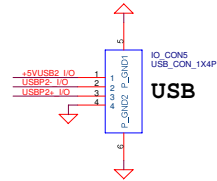
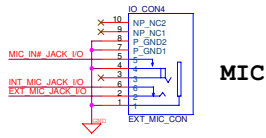
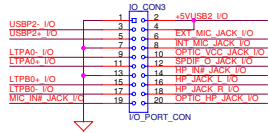
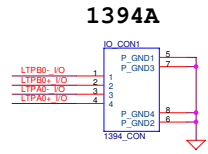
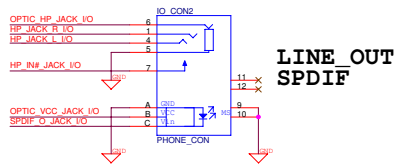
Power:

System:

Core Design

 PROJECT: A8T	REVISION	DATE: Friday, July 21, 2006	DESCRIPTION: HISTORY	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Albert Su
	2.1	SHEET 43 OF 55		RELEASE DATE :	

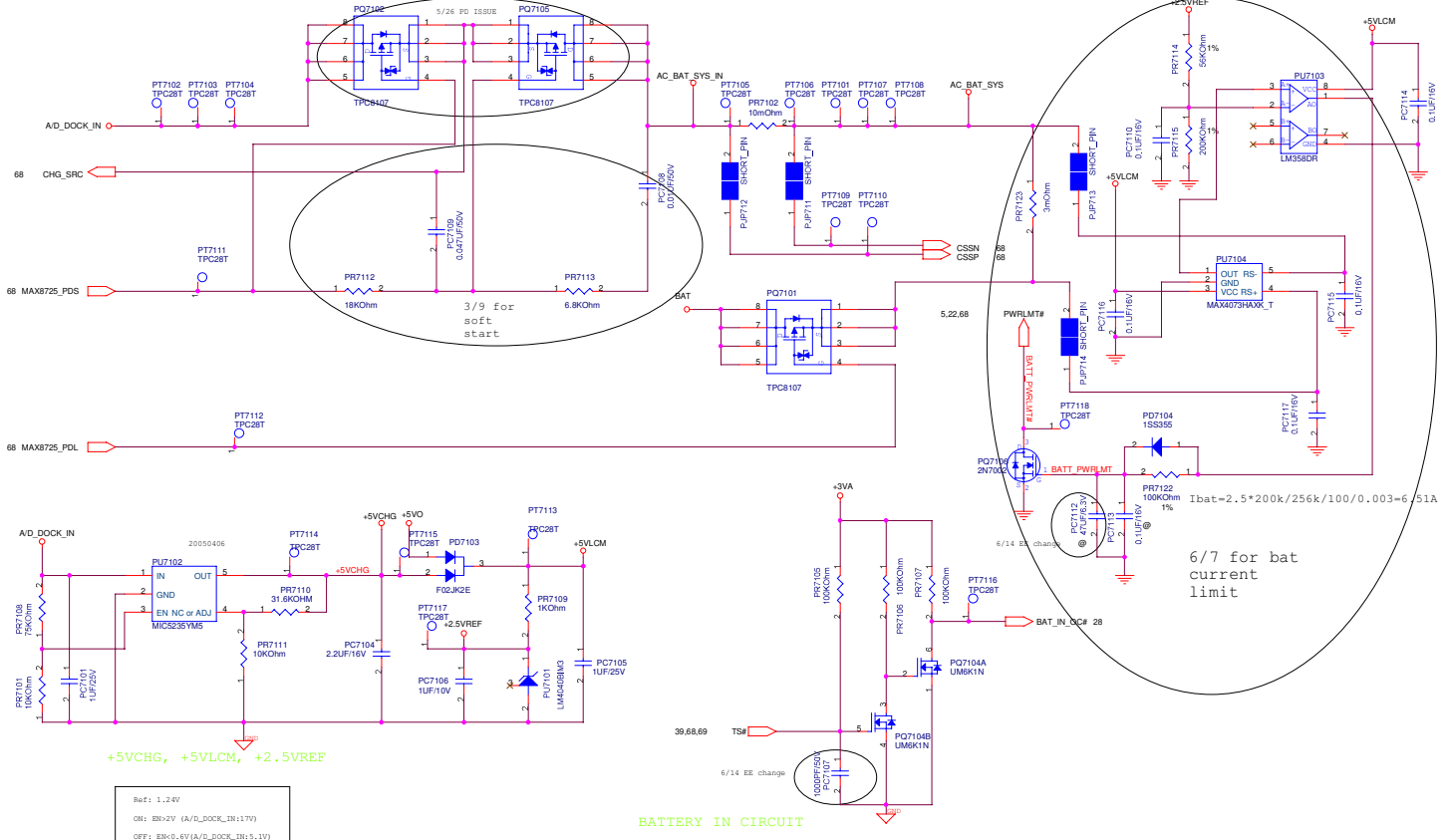
<< Kennedy_Zhang >>



Core Design

	PROJECT: A8T	REVISION: 2.1	DATE: Friday, July 21, 2006	DESCRIPTION: I/O PORT	SCHEMATIC FILE NAME: _____	DESIGN ENGINEER: Albert Su
			SHEET: 44 OF 55		RELEASE DATE: _____	

<< Kennedy_Zhang >>



+5VCHG, +5VLCM, +2.5VREF

Ref: 1.24V
 ON: EN=2V (A/D_DOCK_IN=17V)
 OFF: EN=0.6V (A/D_DOCK_IN=5.1V)

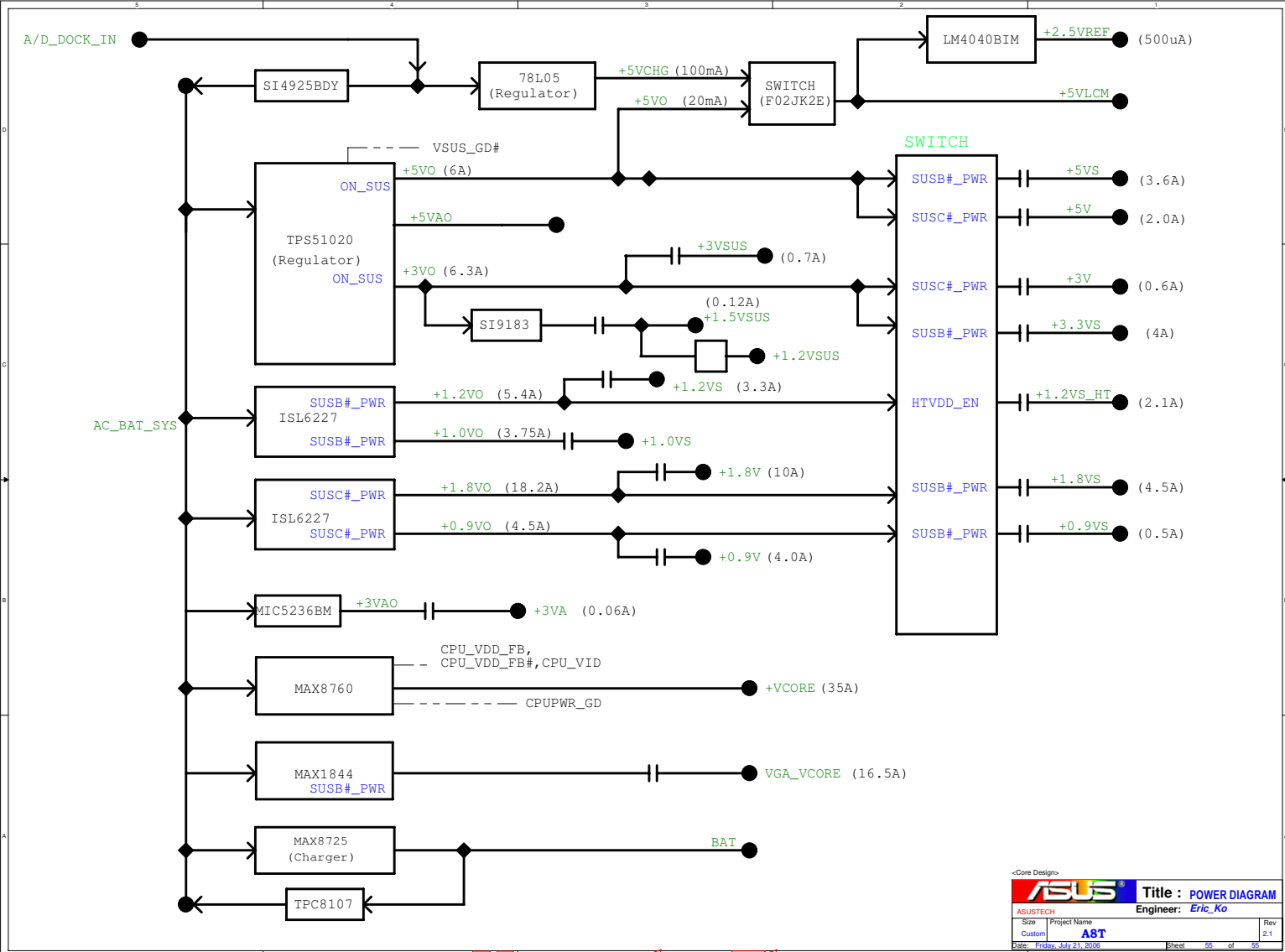
BATTERY IN CIRCUIT

6/7 for bat current limit

<Core Design>

ASUSTECH		Title : POWER_SWITCH_5VLCM	
Size	Project Name	Engineer:	Eric_Ko
Custom	ABT		
Date: Friday, July 21, 2006	Sheet	64	of 95
			Rev 2.1

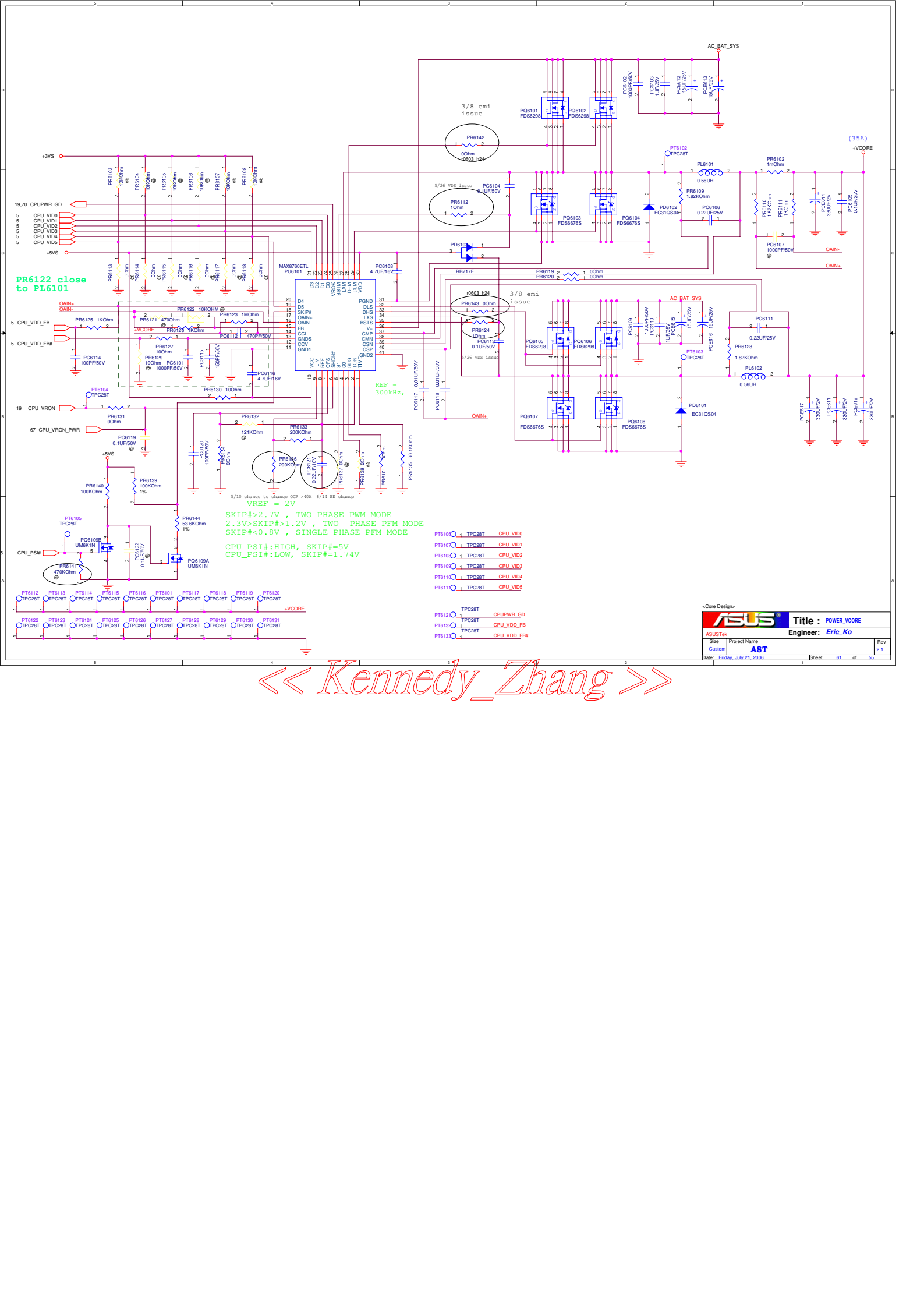
<< Kennedy_Zhang >>



<Core Design>

ASUS		Title : POWER DIAGRAM	
ASUSTECH	Project Name	Engineer: Eric_Ko	Rev
Size	Custom	ABT	2.1
Date: Friday, July 23, 2006	Sheet	66	of 66

<< Kennedy_Zhang >>



PR6122 close to PL6101

5/10 change to change OCP >40A 5/14 SE change
VREF = 2V

SKIP#>2.7V , TWO PHASE PWM MODE
2.3V>SKIP#>1.2V , TWO PHASE PWM MODE
SKIP#<0.8V , SINGLE PHASE PWM MODE

CPU_PSI#:HIGH, SKIP#=5V
CPU_PSI#:LOW, SKIP#=1.74V

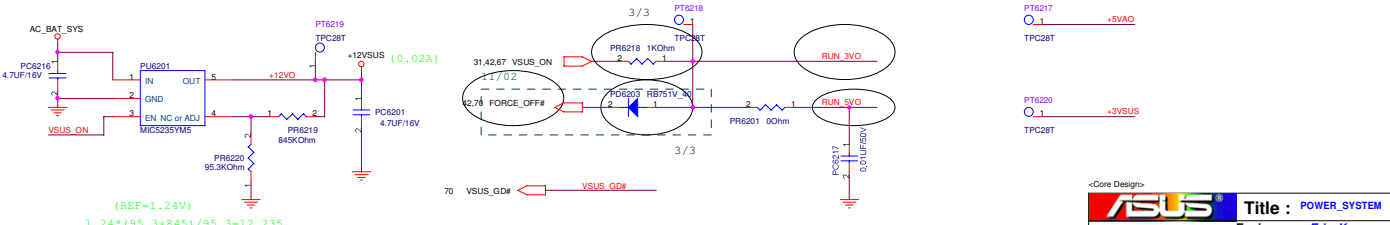
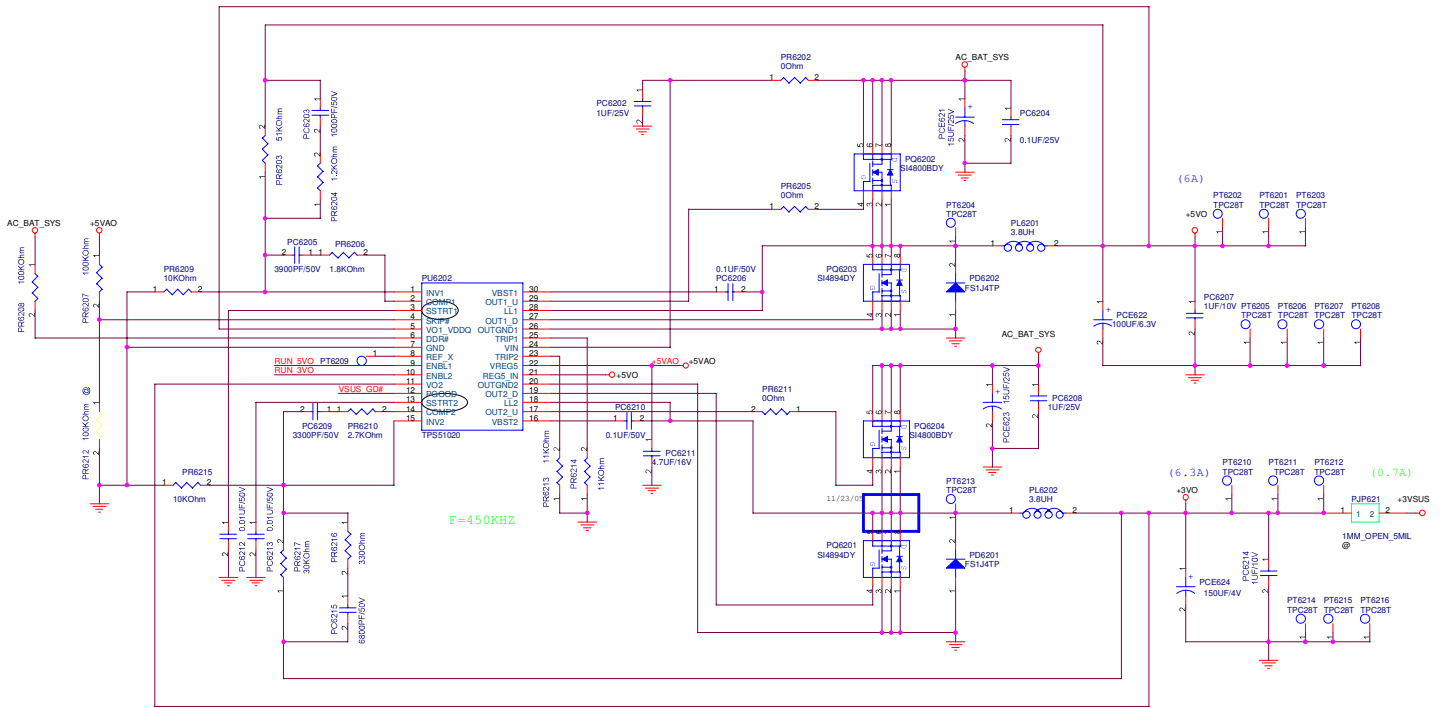
- PT6100 1 TPC28T CPU VID0
- PT6100 1 TPC28T CPU VID1
- PT6100 1 TPC28T CPU VID2
- PT6100 1 TPC28T CPU VID3
- PT6110 1 TPC28T CPU VID4
- PT6111 1 TPC28T CPU VID5

- PT612 1 TPC28T CPU_PWR_GD
- PT613 1 TPC28T CPU_VDD_FB
- PT613 1 TPC28T CPU_VDD_FB#

<Core Design>

		Title : POWER_VCORE
ASUSTek	Project Name	Engineer: Eric_Ko
Custom	ABT	Rev 2.1
Date: Friday, July 21, 2006	Sheet 61	of 65

<< Kennedy_Zhang >>



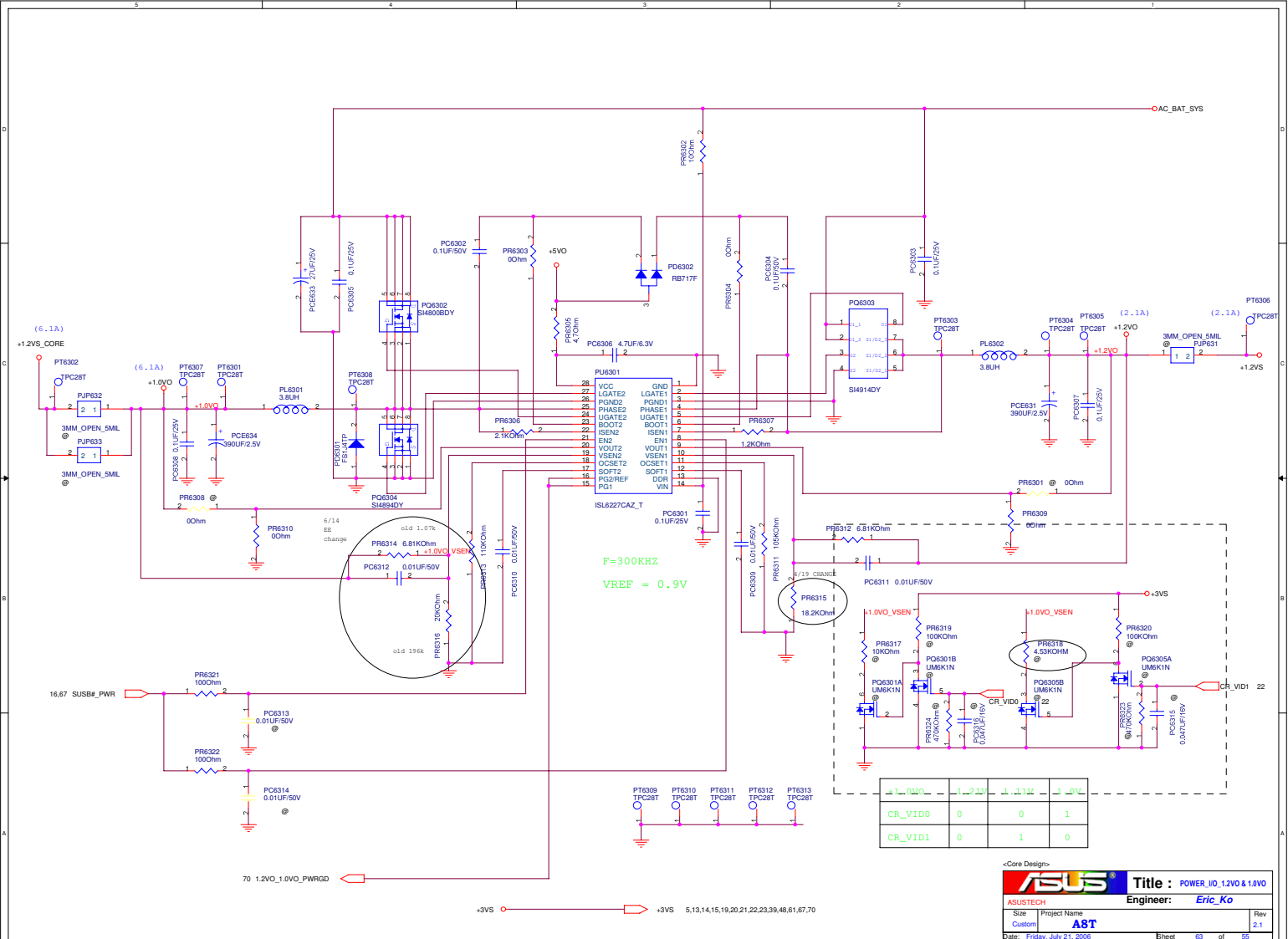
(REF=1.24V)
 $1.24 * (95.3 + 845) / 95.3 = 12.235$

31.4267 VSUS_ON
 2.74 FORCE_OFF#

<Core Design>

ASUS		Title : POWER_SYSTEM	
ASUSTECH	Project Name	Engineer:	Eric_Ko
Size	Custom	ABT	Rev 2.1
Date: Friday, July 21, 2006	Sheet 62	of 95	

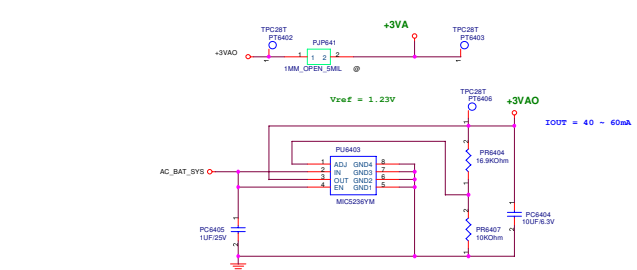
<< Kennedy_Zhang >>



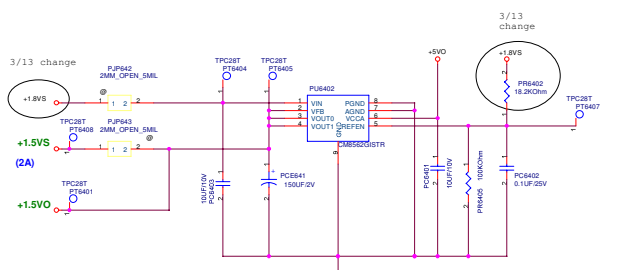
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ASUS Title: POWER_IO_1.2V0 & 1.0V0
 ASUSTECH Engineer: Eric_Ko
 Size: Custom Project Name: AST Rev: 2.1
 Date: Friday, July 21, 2006 Sheet: 63 of 69

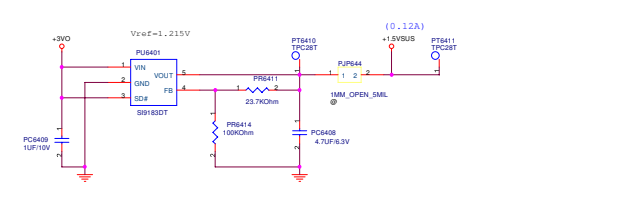
<< Kennedy_Zhang >>



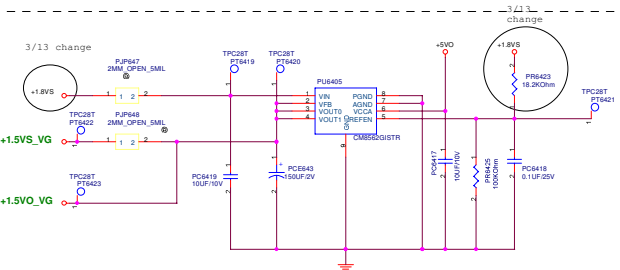
+3VA



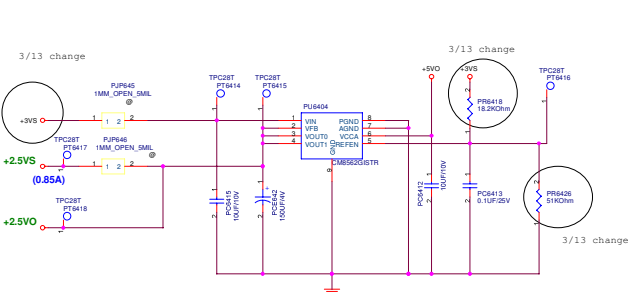
+1.5VS



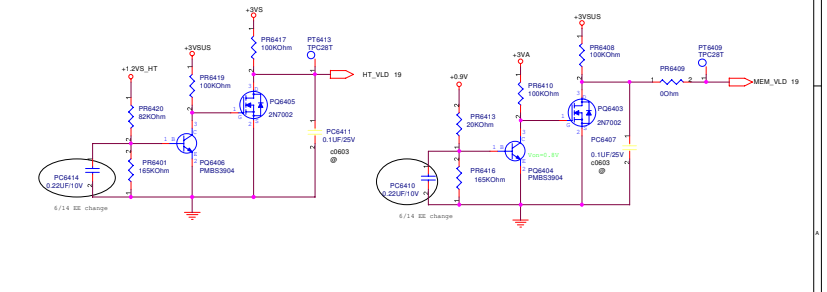
+1.5VSUS



+1.5VS_VG

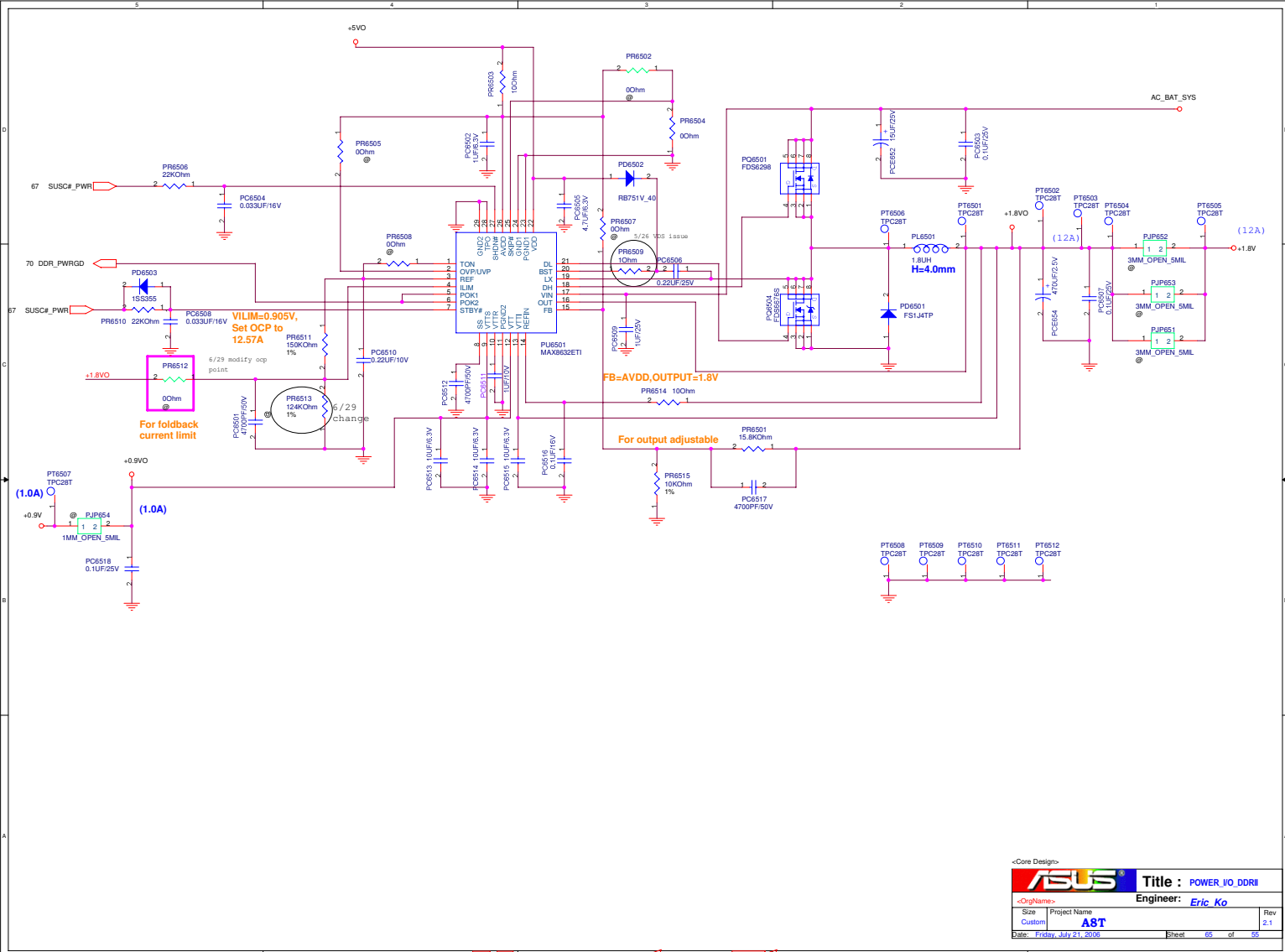


+2.5VS



ASUS		Title : POWER_IO_LDO	
ASUSTECH	Project Name	Engineer: Eric_Ko	
Rev	Rev	Rev	Rev
1	1	1	1
Date: 2009-09-21-2009	Sheet: 44	of	56

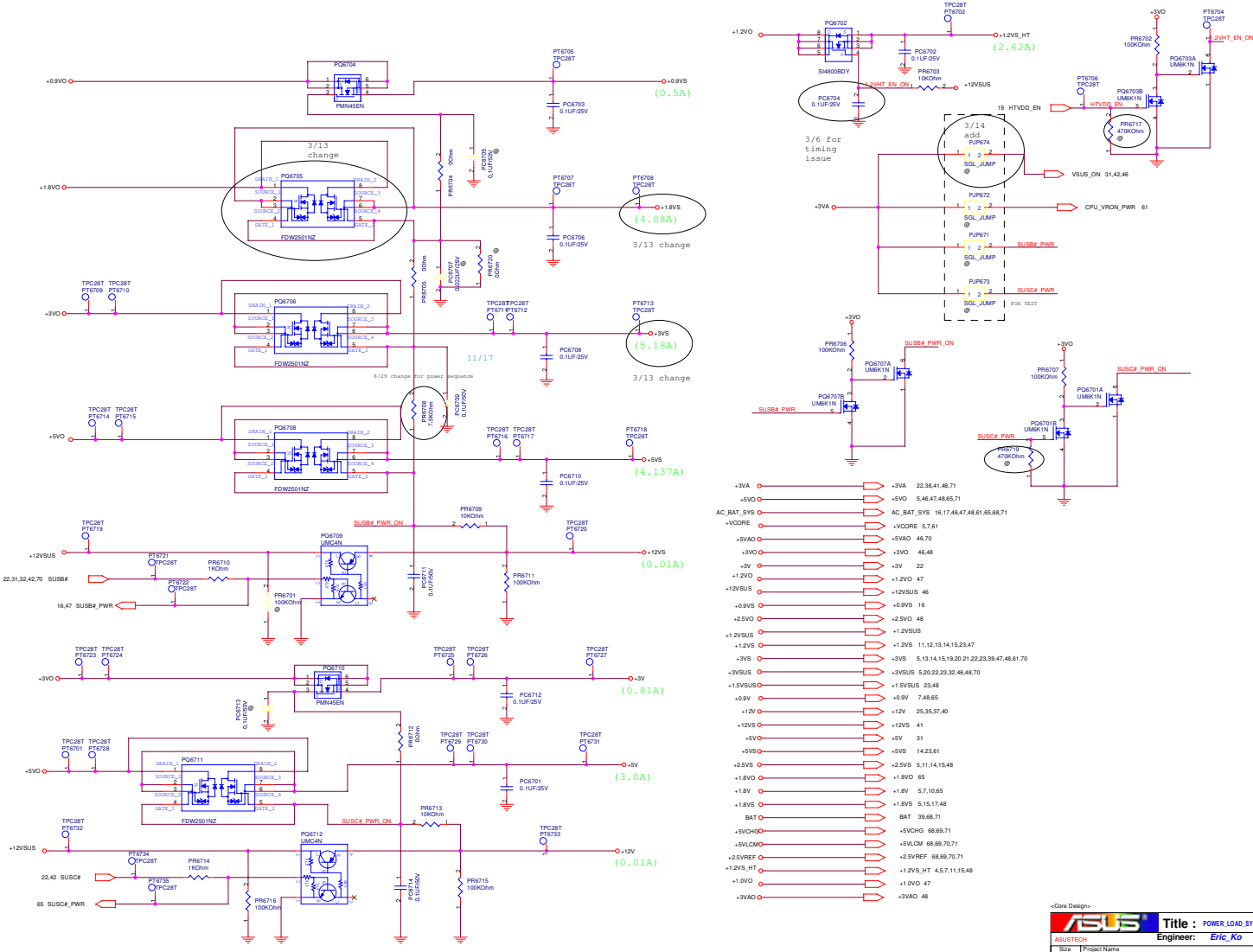
« Kennedy_Zhang »



-Core Design-

ASUS		Title : POWER_IO_DDR1
Engineer: Eric Ko		
Size: Custom	Project Name: ABT	Rev: 2.1
Date: Friday, July 21, 2006	Sheet: 66	of 69

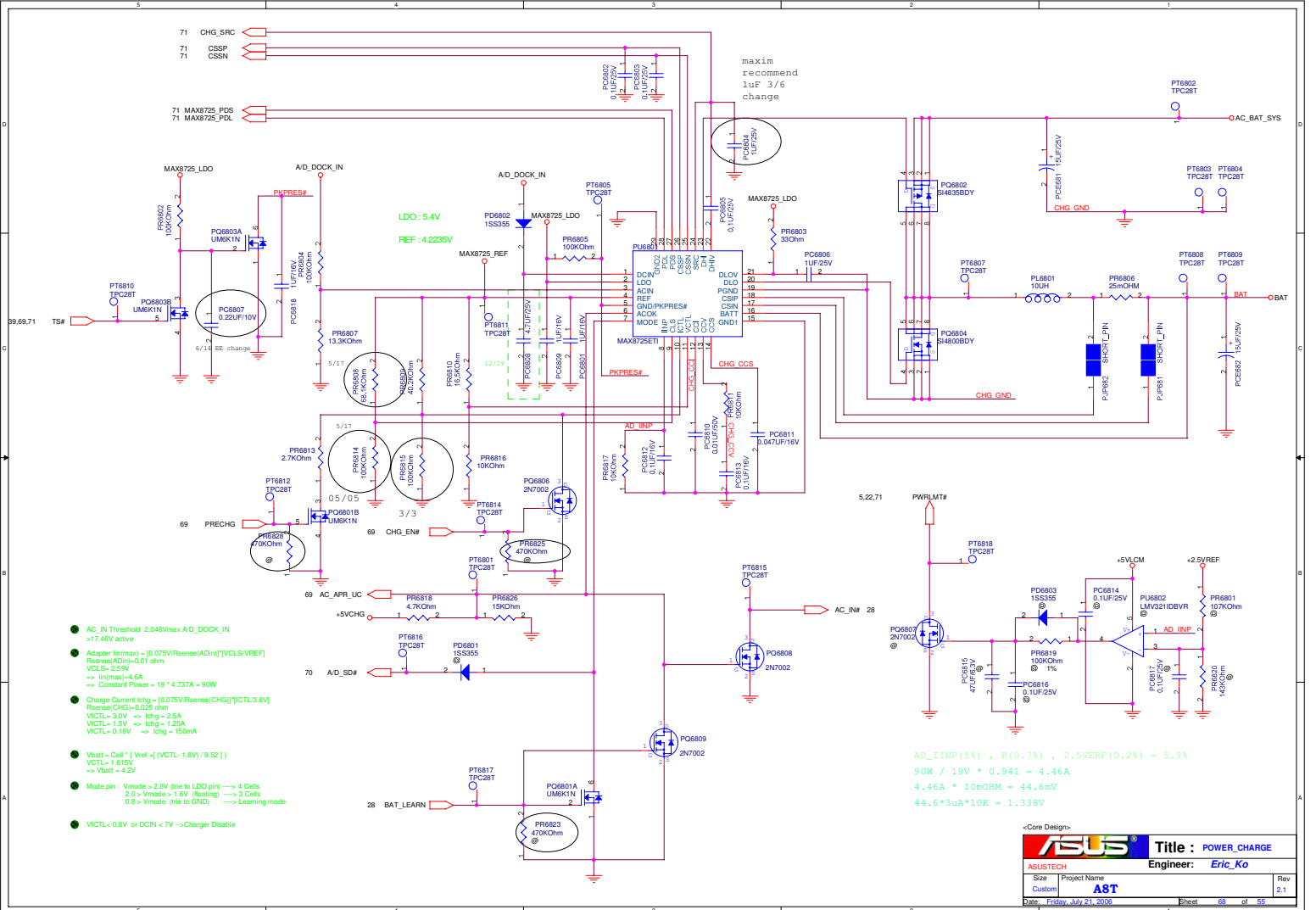
<< Kennedy_Zhang >>



+3VA	22.38,41,48,71
+5VA	5.46,47,48,65,71
AC_BAT_SYS	16,17,48,47,48,61,65,68,71
+VDDRE	5,76
+5VAD	46,70
+3V	22
+12VDD	47
+12VSUS	48
+0.9VS	15
+5VIO	48
+1.2VSUS	11,12,13,14,15,23,47
+3VS	5,13,14,15,16,20,21,22,23,30,47,48,61,70
+3VSUS	5,20,22,23,32,48,48,70
+1.5VSUS	23,48
+0.9V	7,48,65
+12V	25,35,37,40
+12VS	41
+5V	31
+5VS	14,23,61
+2.5VS	5,11,14,15,48
+1.8V0	65
+1.8V	5,7,10,65
+1.8VS	5,15,17,48
BAT	39,68,71
+5VCHG0	+5VCHG 68,69,71
+5VLCM0	+5VLCM 68,69,70,71
+2.5VREF	68,69,70,71
+1.2VS_HT	+1.2VS_HT 4,5,7,11,15,48
+1.0V0	47
+3VAD	48

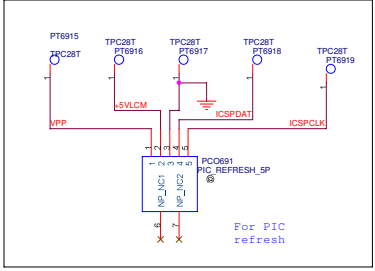
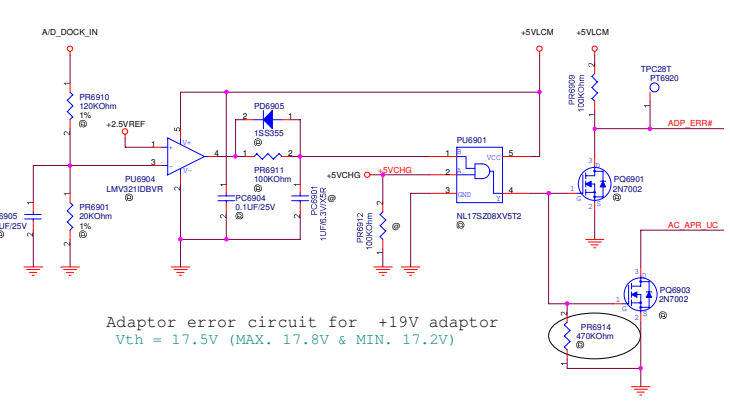
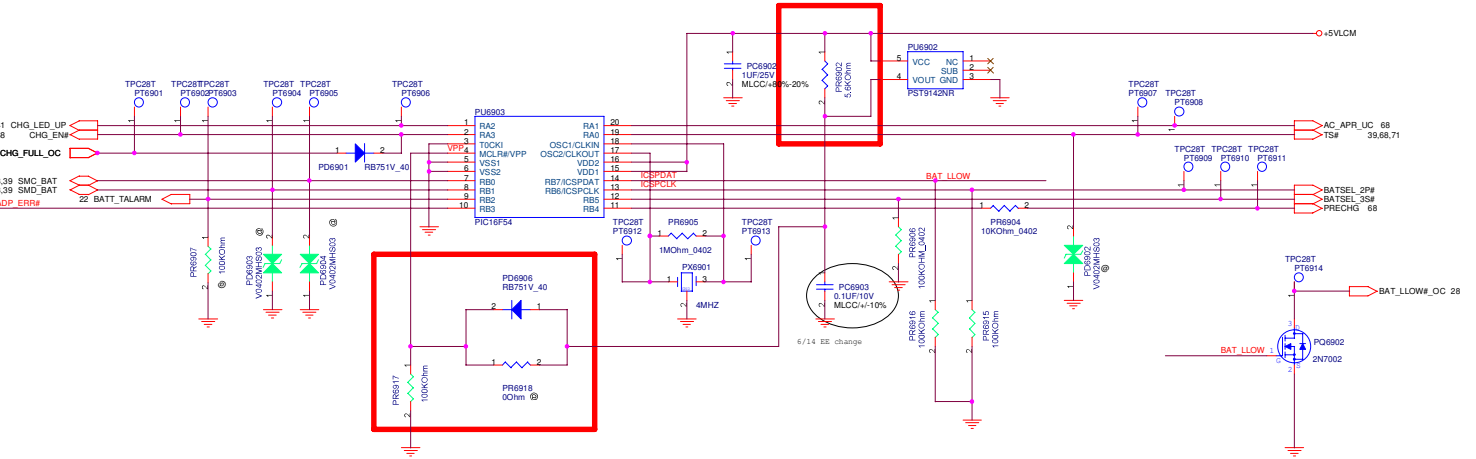
ASUS
 Title : POWER_LOAD_SYSTEM
 Engineer: Eric_Ko
 Rev: 2.1
 Date: Friday, July 21, 2006
 EScan 87 of 88

<< Kennedy_Zhang >>



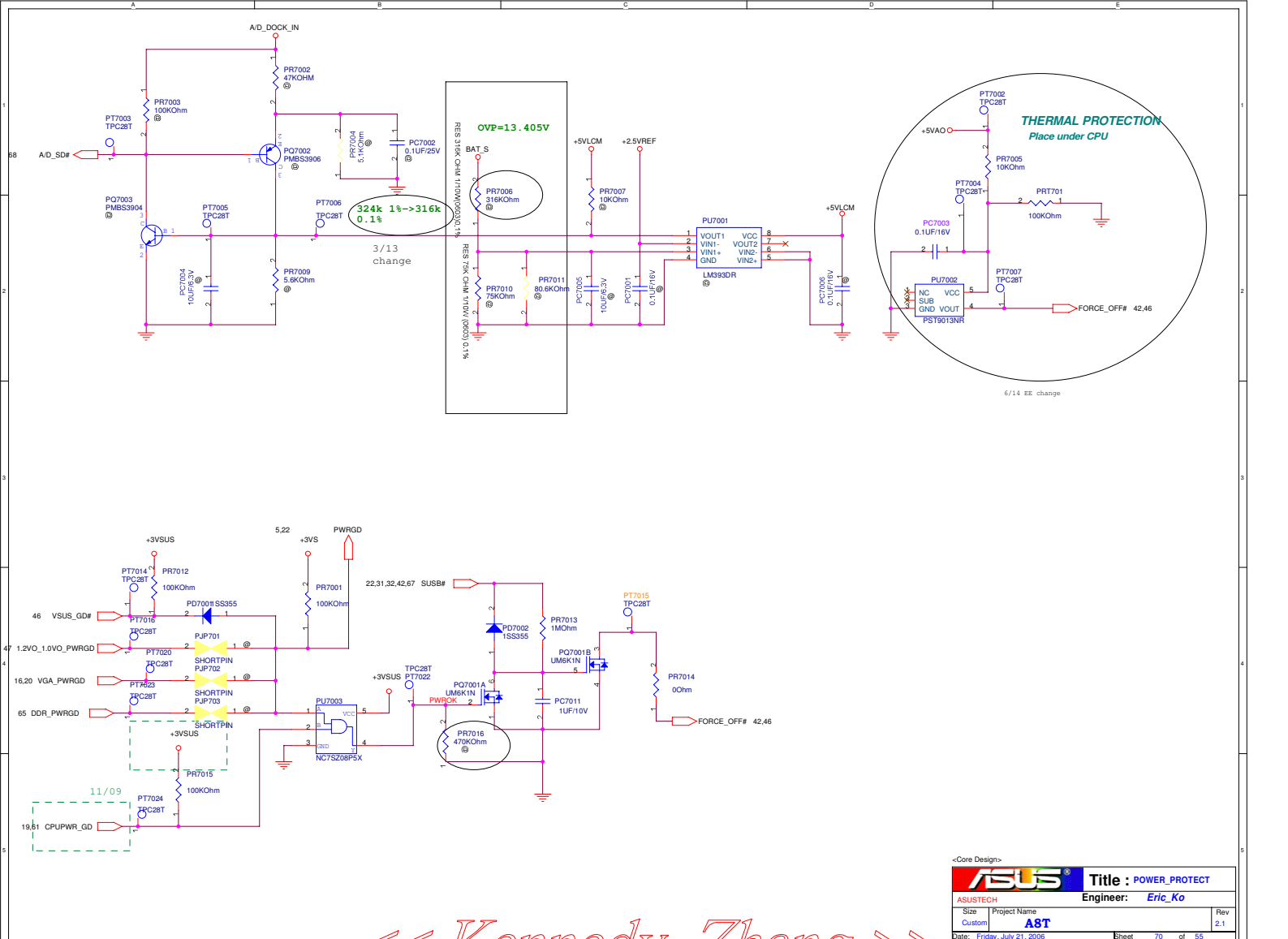
<< Kennedy_Zhang >>

PIC16F54



<Core Design>			
		Title : POWER PIC	
<OrigName>		Engineer: Eric_Ko	
Size	Project Name		Rev
Custom	ABT		2.1
Date: Friday, July 21, 2006		Sheet	69 of 95

<< Kennedy_Zhang >>



~Core Design~

ASUS		Title : POWER_PROTECT
ASUSTECH	Project Name	Engineer: Eric_Ko
Size	A8T	Rev 2.1
Date: Friday, July 21, 2006	Sheet 70	of 55

« Kennedy_Zhang »