Biwa Block Diagram

Project code: 91.4H001.001
PCB P/N : 55.4H001.XXX
REVISION : 06237-2(GCE, Hannstar)

-2-0226

CLK GEN.
ICS 9LPR502
(RTM875T-605) 3

Mobile CPU
Merom 479
2G/2.33G
2.0G : B0, QLYV
2.2G : B0, QLFS
4, 5

G792 20

HOST BUS 800MHz@1.05V

DDR2 533/667 MHz 12,13
533/667MHz

DDR2 533/667 MHz 12,13
533/667MHz

Crestline
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
71.CREST.M02, B0, QN12
6,7,8,9,10,11

SVIDEO/COMP → TVOUT 15
LVDS → 14" WXGA LCD 14
RGB CRT → CRT 15

X4 DMI 400M Byte/s
C-Link0

ICH8M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 1.1
3 SATA
1 PATA 66/100
10 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
71.0ICH8.A0U, B1, QN23
16,17,18,19

Line In 30
Mic In 30
INT.MIC
INT.SPKR 30
Line Out (No-SPDIF) 30

Codec ALC268 29
AZALIA

OP AMP APA2031 30
G1412 30

MODEM MDC Card 22
RJ11 24

PCI BUS

TI 7412 CardBus 1394 CardReader 25,26
PCMCIA I/F
PWR SW TPS2211 27
PCMCIA SLOT Support TypeII 27
1394 CONN 26
MS/MS Pro/xD/ MMC/SD/SDIO 6 in 1 27

LAN Giga LAN BCM5787MKMLG 23
TXFM 24
RJ45 24

New card 28
PWR SW P2231NFC 28

PCIex1
Mini Card Kedron a/b/g/n 28
C Link1

LPC BUS

SATA
PATA

HDD 21
USB 4 PORT 22
CCD 14
CDROM 21
MINI USB 22 Blue-tooth
Finger PT 22

Super I/O Winbond PC87381 33
FIR 32

KBC Winbond WPC8763L 31
Touch Pad 32
INT. KB 32

SPI I/F
BIOS 33 W25X80-VSSI-G

LPC DEBUG CONN. 33

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

CPU DC/DC MAX8770 36	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

SYSTEM DC/DC ISL6236 37	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(5A) 3D3V_S5(5A) 5V_AUX_S5

SYSTEM DC/DC MAX8717 38	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(13A) 1D8V_S3(10A)

G971 39	
1D8V_S3	1D5V_S0 (4A)

APL5913 39	
1D8V_S3	1D25V_S0 (1.5A)

G2997F6U 39	
1D8V_S3	DDR_VREF_S0 (1.2A) DDR_VREF_S3

G909 34	
5V_AUX_S5	3D3V_AUX_S5 (100mA)

MAXIM CHARGER ISL6255 40	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 19V 4.0A UP+5V 5V 100mA

55.4H001.S03G

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Title: BLOCK DIAGRAM
Size: Biwa
Rev: -2
Date: 2007
Sheet 1 of 42

ICH8M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	USB3
3	USB4
4	MINIC1
5	BT
6	CCD
7	Finger
8	NEW
9	NC

ICH8M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K (?)
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K (?)
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Crestline Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode **1 = Low Power mode** (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWORK in signal.

History

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2007/02/16
1.Page 33: Add SIO 87381 for FIR Issue.
2.Page 31, change KBC from 8768L to 8763L.
3.Page 33, del U33(LPC golden Finger).
4.Page 24/32, change ERC1/ERC2 due to 77.61021.02L is Obsoleted Part !
5.Page 37, del TC22/TC19.
6.Page 38, del TC1/TC4.
============================================================
2007/02/09
1.Page 14:Modify "Q14" "BTBTN1" "WLBTN1" symbol.
2.Page 36, 37, 38: Replace 0ohm with 0ohm pad.
============================================================
2007/02/08a
1.Page 14:Modify R428 to“FRONT_PWRLED#_1”and RN58 pin7 to“STBY_LED#_2”due to LED brightness issue.
2.Page 38:Replace "TC26" with "77.C1561.01L".
============================================================
2007/02/08
1.Page 10:Replace "R244" with "0603-PAD".
2.Page 36:Replace open power gap with close power gap.
3.Page 38:Add capacitor "TC26" for acoustic noise
============================================================
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55.4H001.S03G

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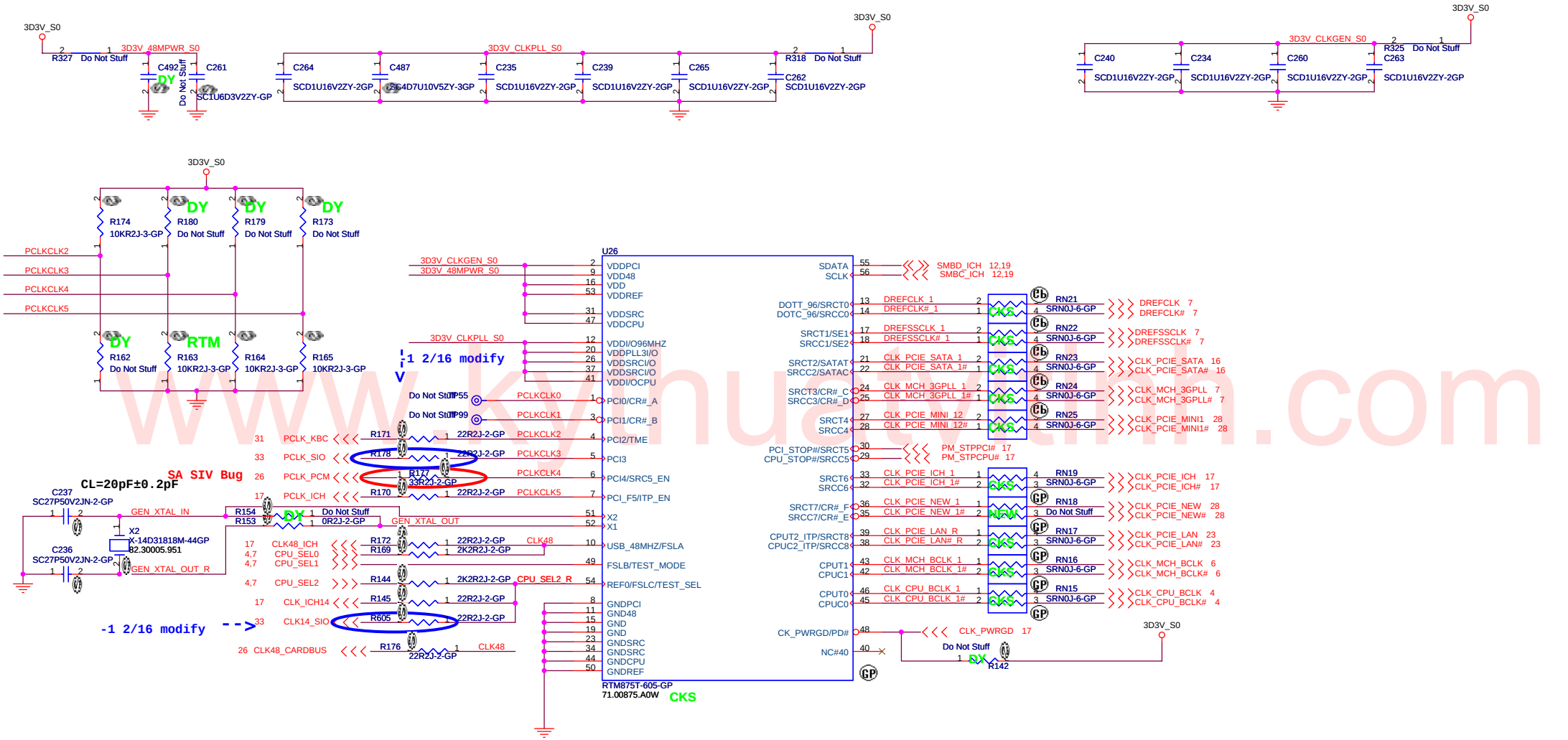
Title: Reference
Size: A3 | Document Number: Biwa | Rev: -2
Date: Thursday, March 01, 2007 | Sheet 2 of 42



ICS9LPR502HGLFT-GP setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI4/SRC5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

RTM875T-605 setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/SRC-5_EN	0 = Pin29 as CPU_STOP# , pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

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Title: **Clock Generator**

Size	Document Number	Rev
	Biwa	-2

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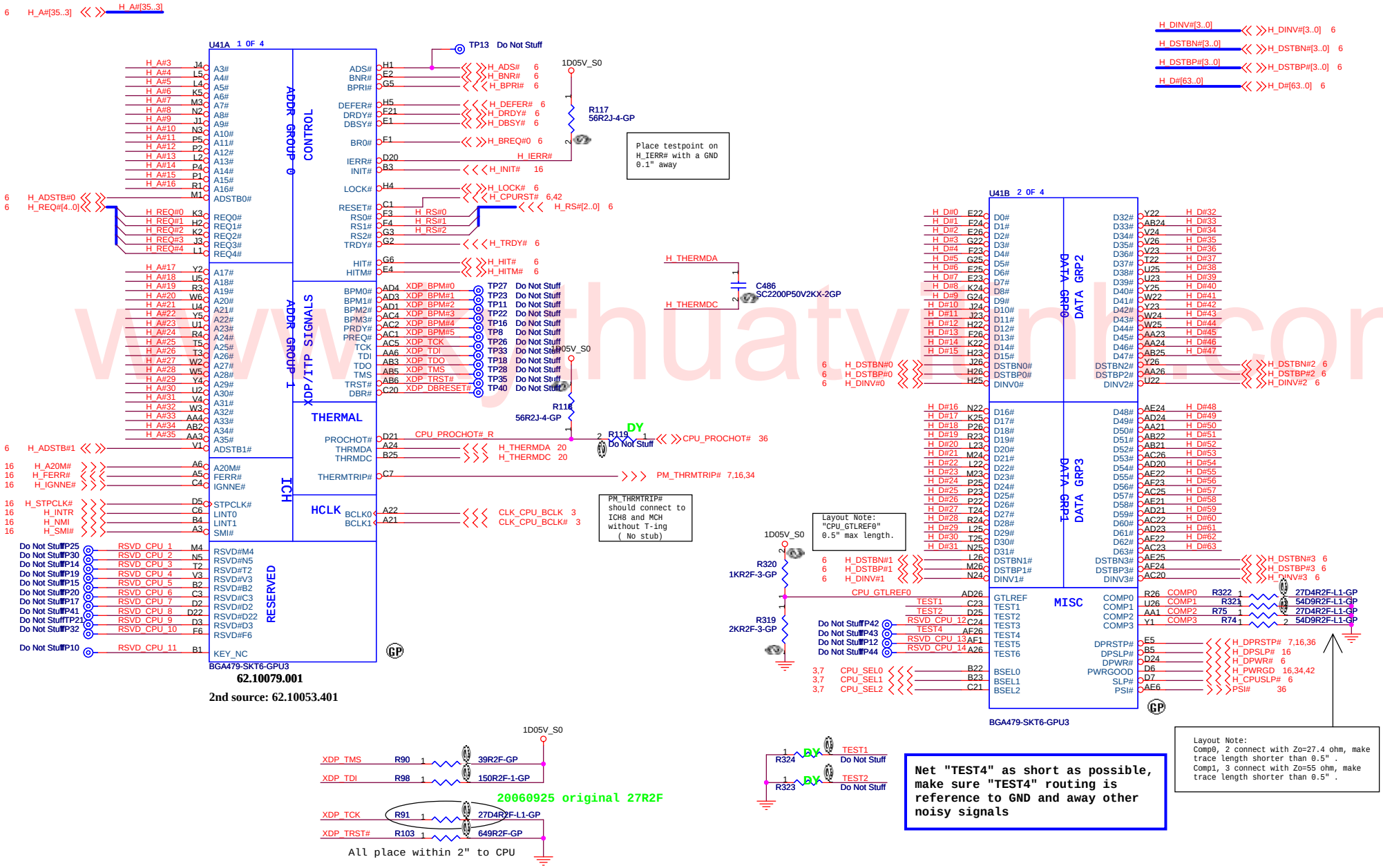

62.10079.001

2nd source: 62.10053.401

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Title: CPU (1 of 2)

Size: | Document Number: Biwa | Rev: SA

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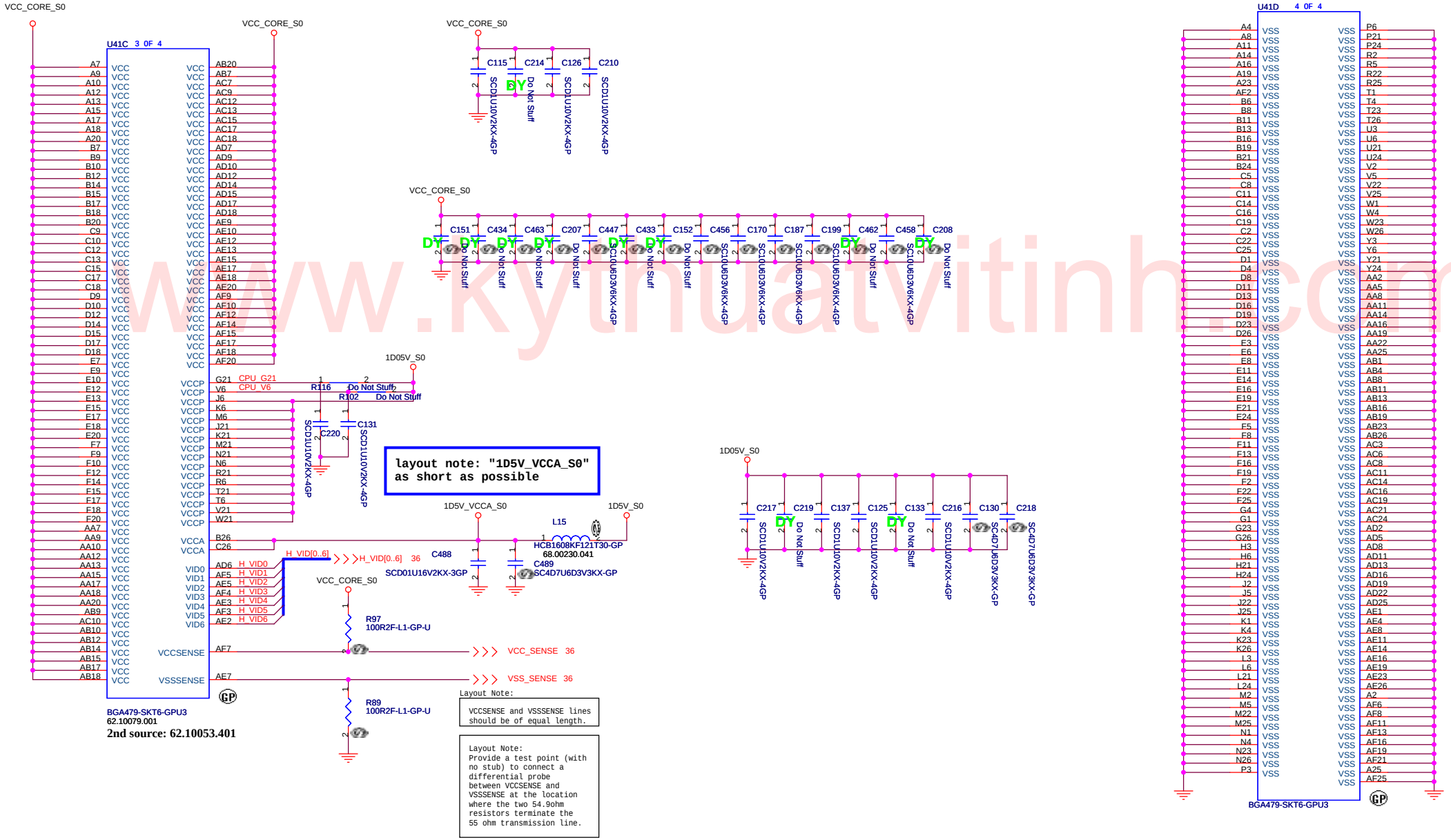

Company	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU (2 of 2)
Size	
Document Number	Biwa
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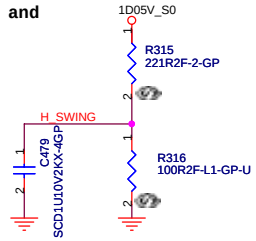
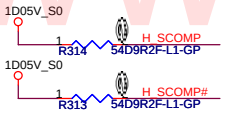
H_SWING routing Trace width and Spacing use 10 / 20 mil

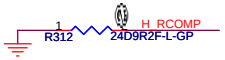
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)

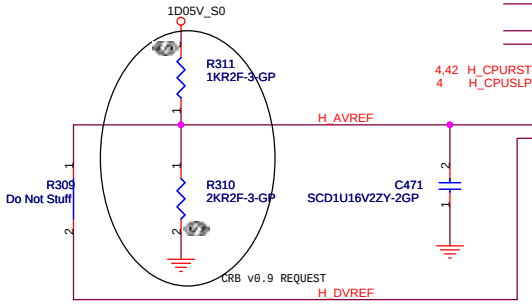


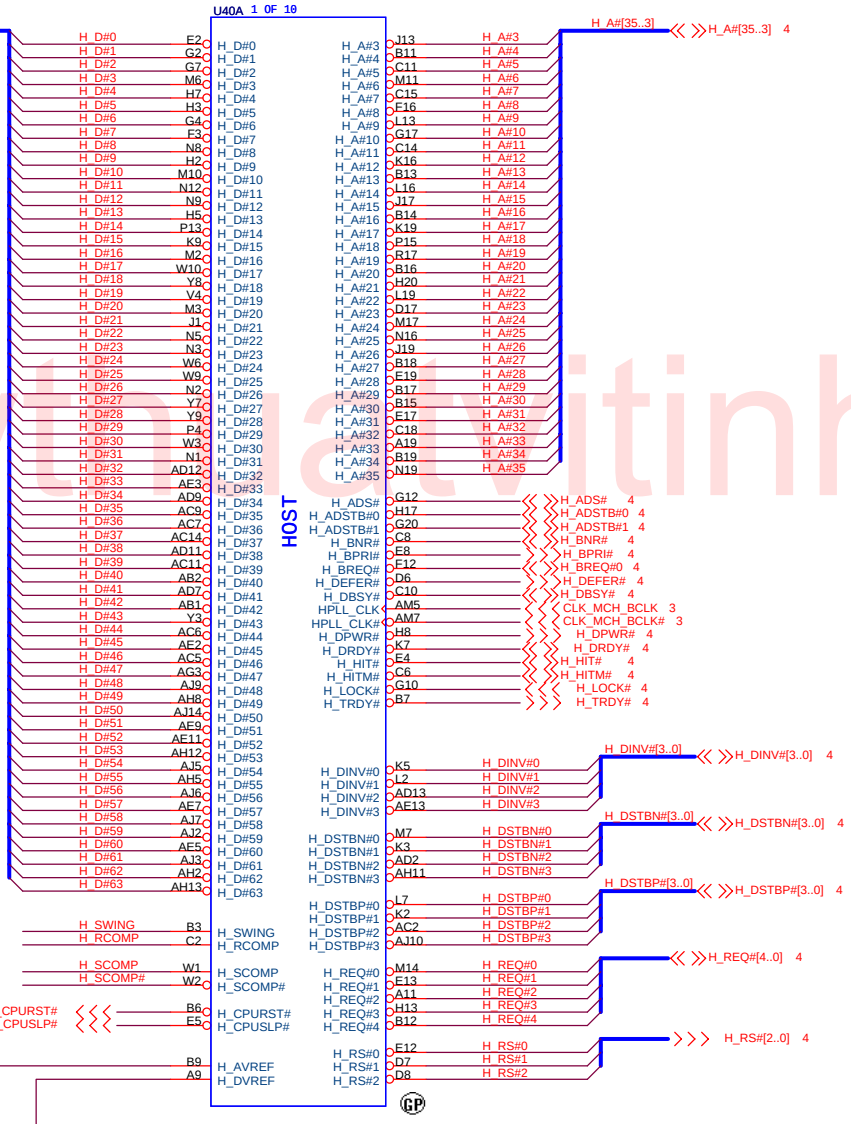
H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")

H_REF Decoupling Crestline close Crestline 100 mil





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Title: ***GMCH (1 of 6)***

Size | Document Number: **Biwa** | Rev: SA

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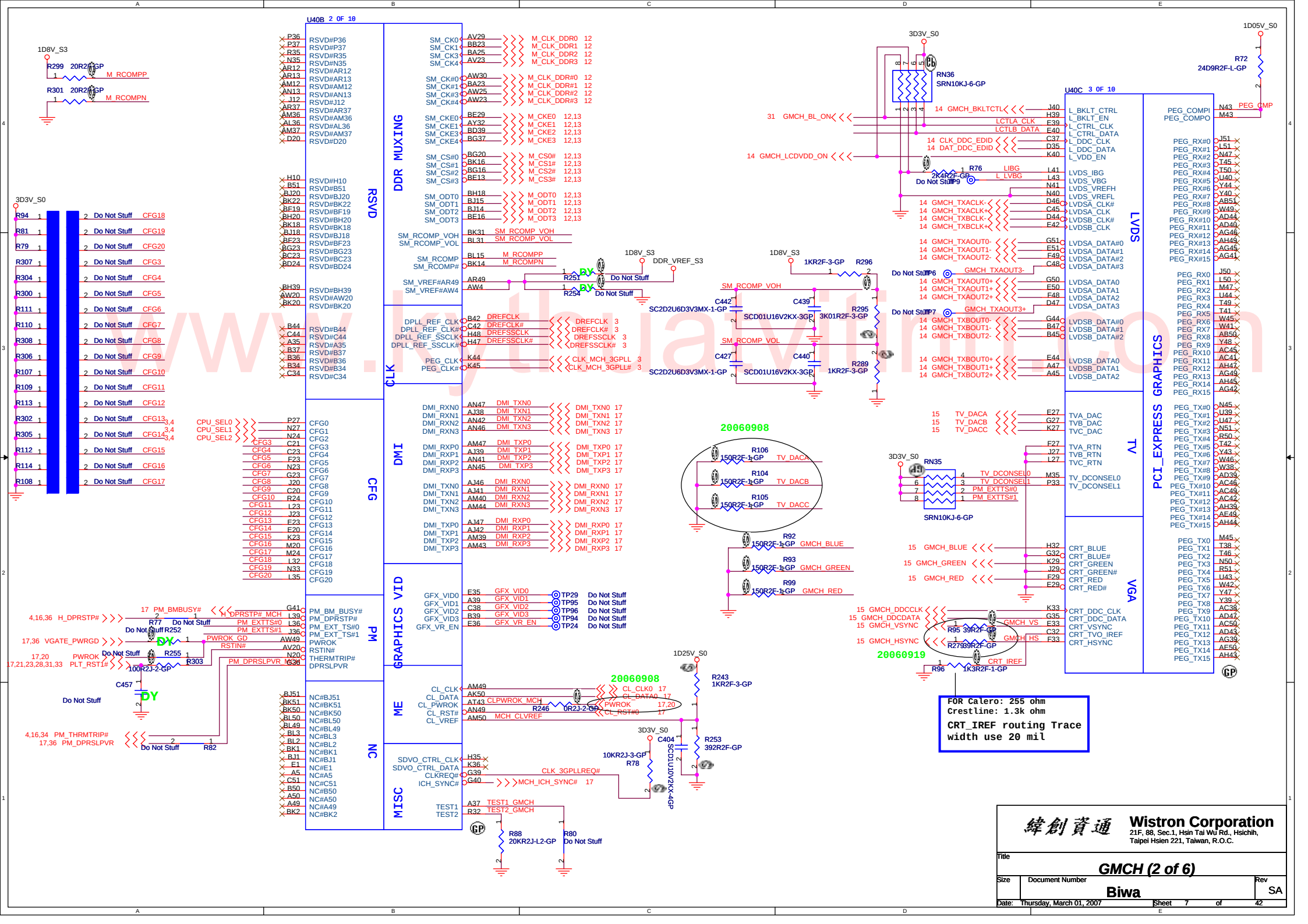
U40B 2 OF 10
RSVD
DDR MUXING
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
U40C 3 OF 10
LVDS
TV
VGA
PCI_EXPRESS GRAPHICS
1D8V_S3
3D3V_S0
1D05V_S0
1D25V_S0
DDR_VREF_S3
20060908
20060919
FOR Calero: 255 ohm
Crestline: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
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GMCH (2 of 6)
Biwa
Rev SA
Date: Thursday, March 01, 2007
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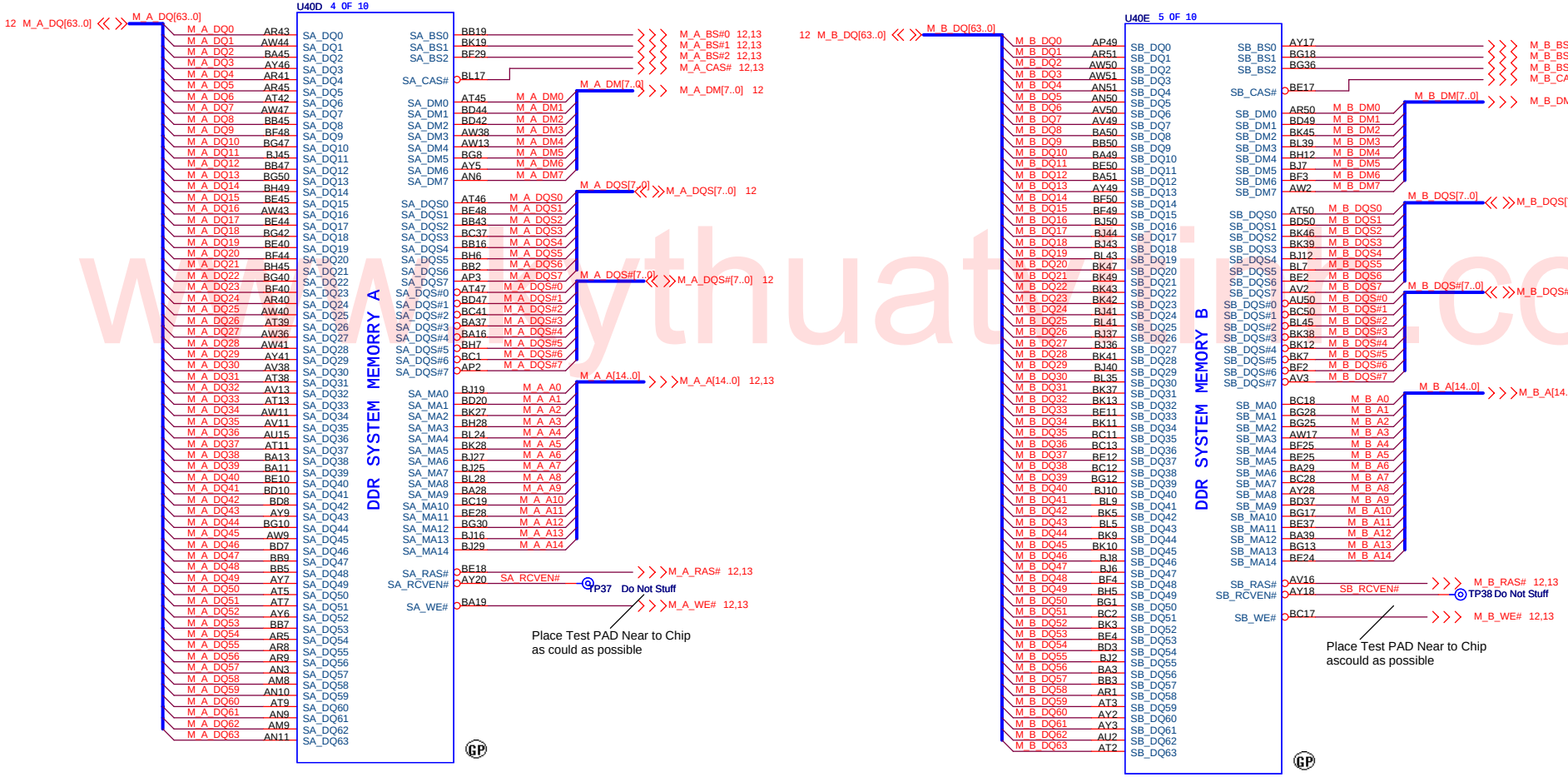

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Size	Document Number **Biwa**	Rev SA
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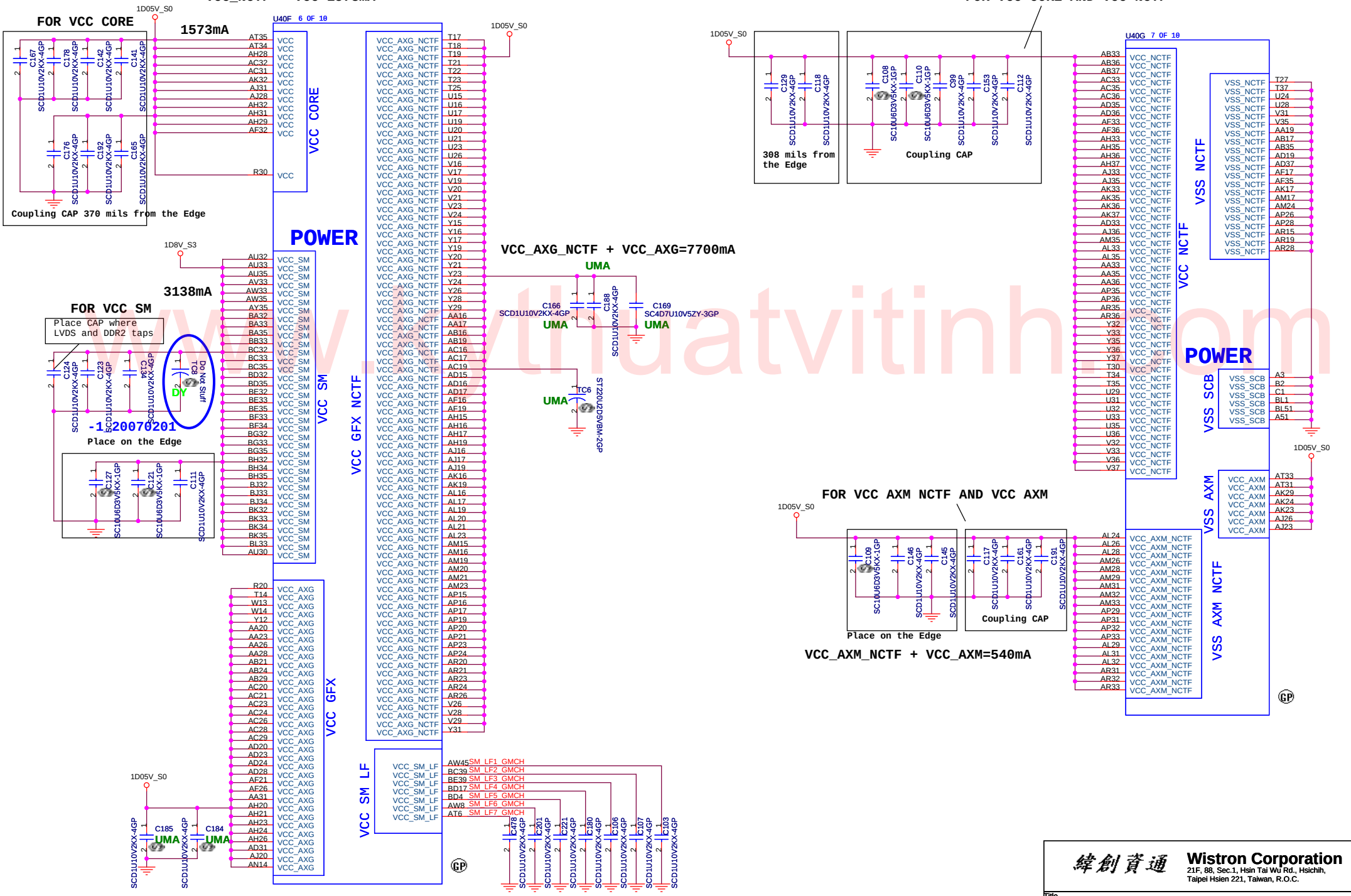

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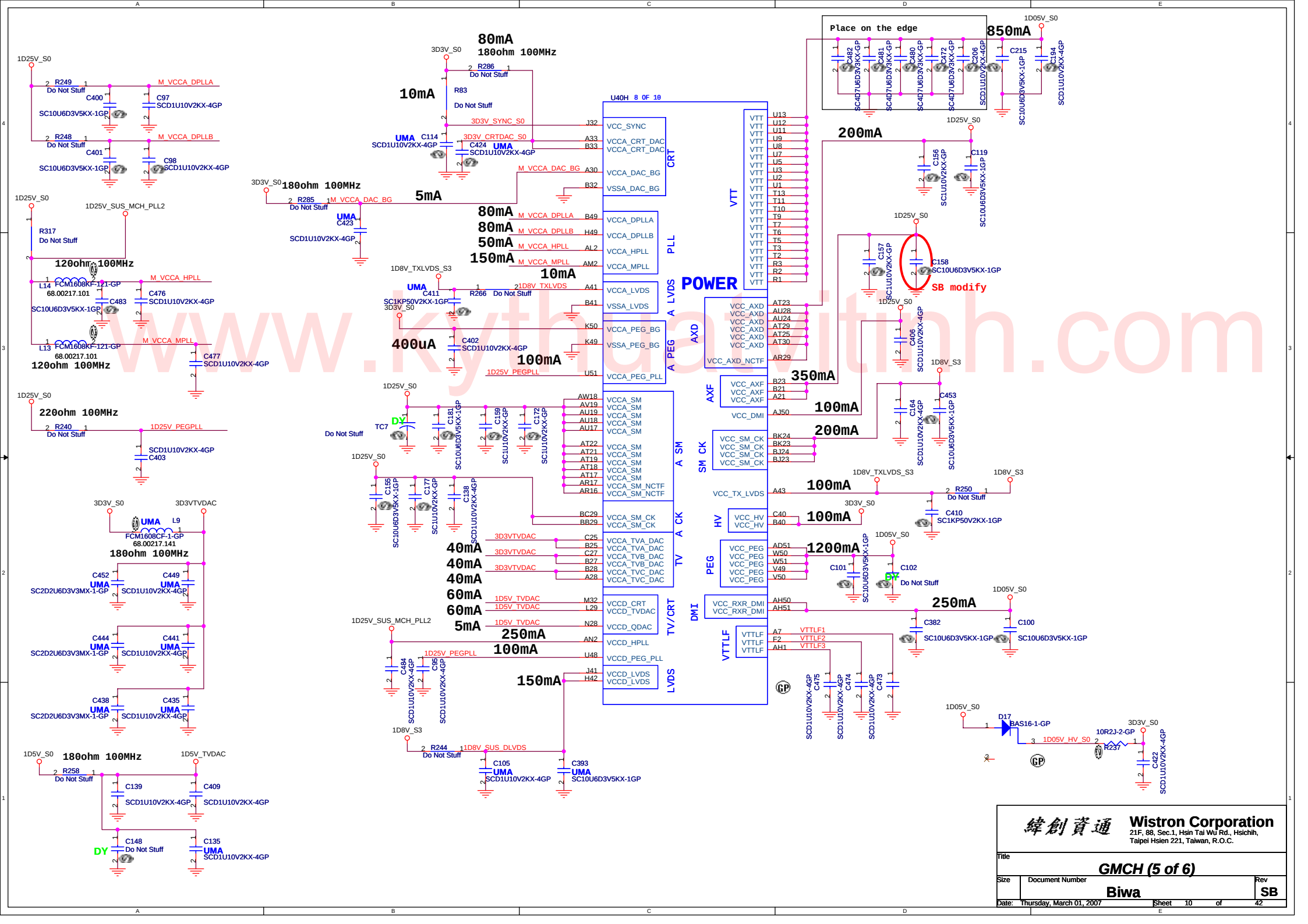
Place on the edge
850mA
200mA
SB modify
POWER
80mA
180ohm 100MHz
10mA
5mA
400uA
100mA
350mA
1200mA
250mA
150mA
40mA
60mA
220ohm 100MHz
120ohm 100MHz
180ohm 100MHz
Do Not Stuff
UMA
DY
TC7
U40H 8 OF 10
CRT
PLL
LVDS
AXD
PEG
SM
CK
TV
TV/CRT
DMI
HV
AXF
SM CK
VTTLF
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GMCH (5 of 6)
Biwa
SB
Thursday, March 01, 2007
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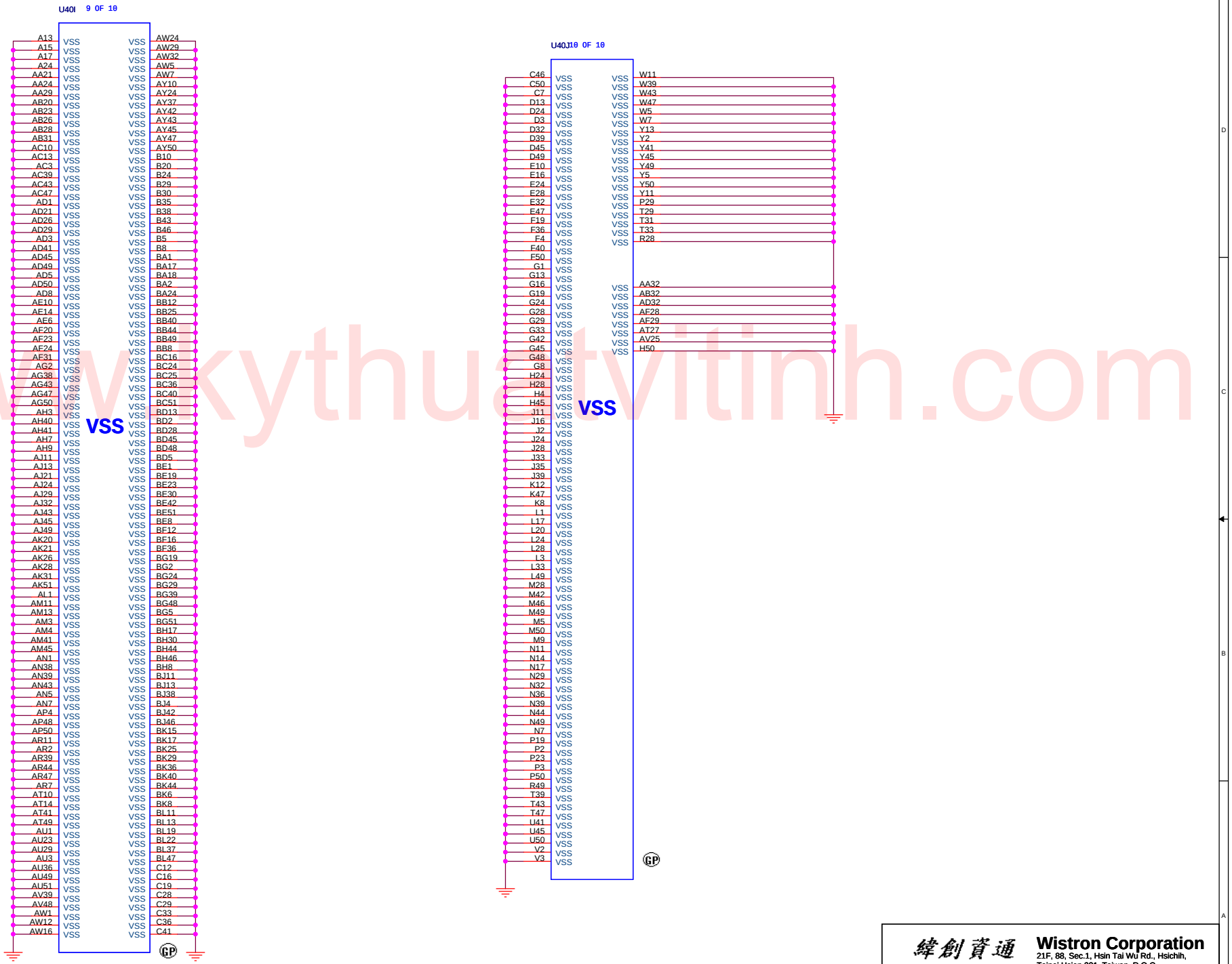

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Size	Document Number: **Biwa** — Rev: SA
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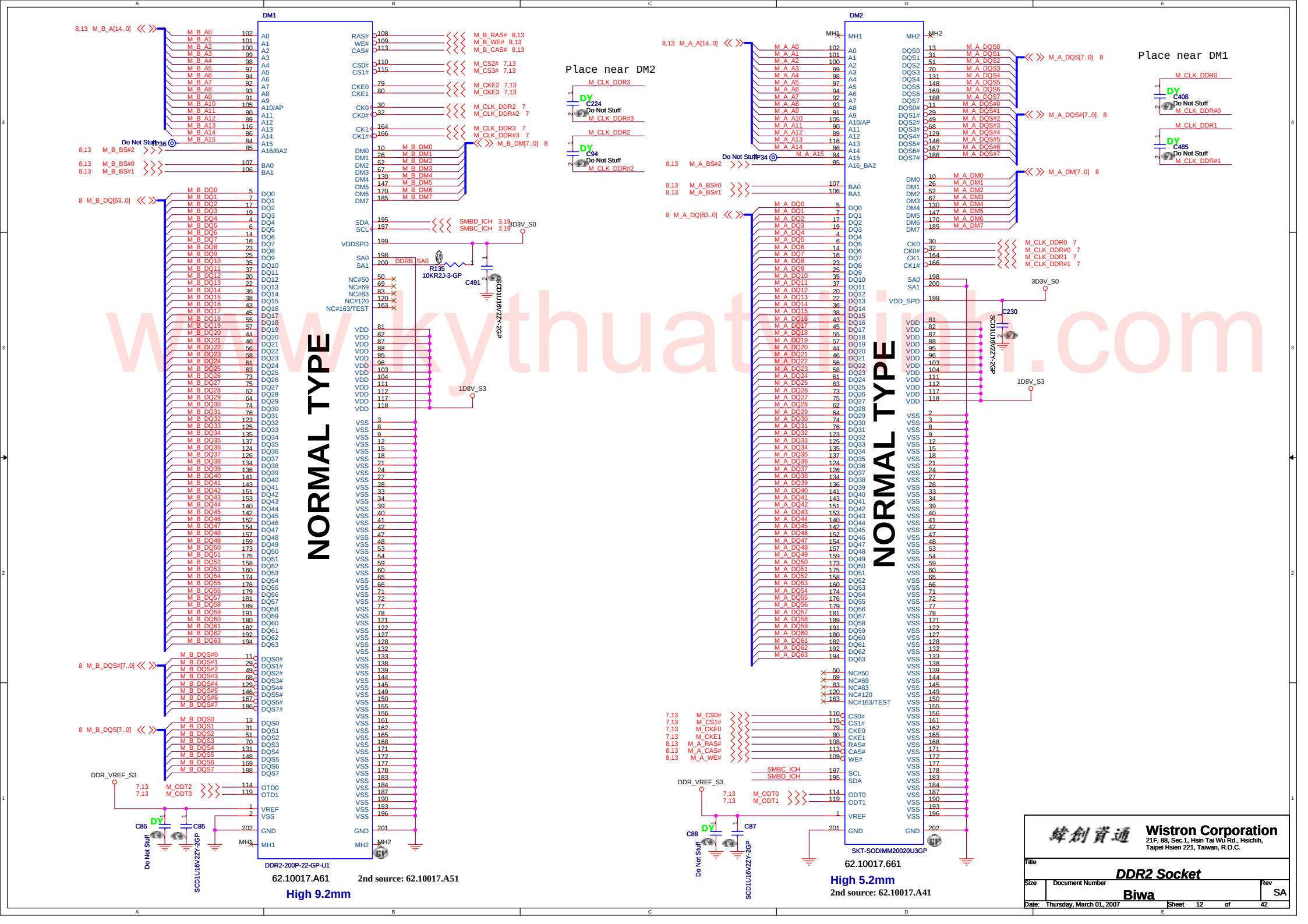
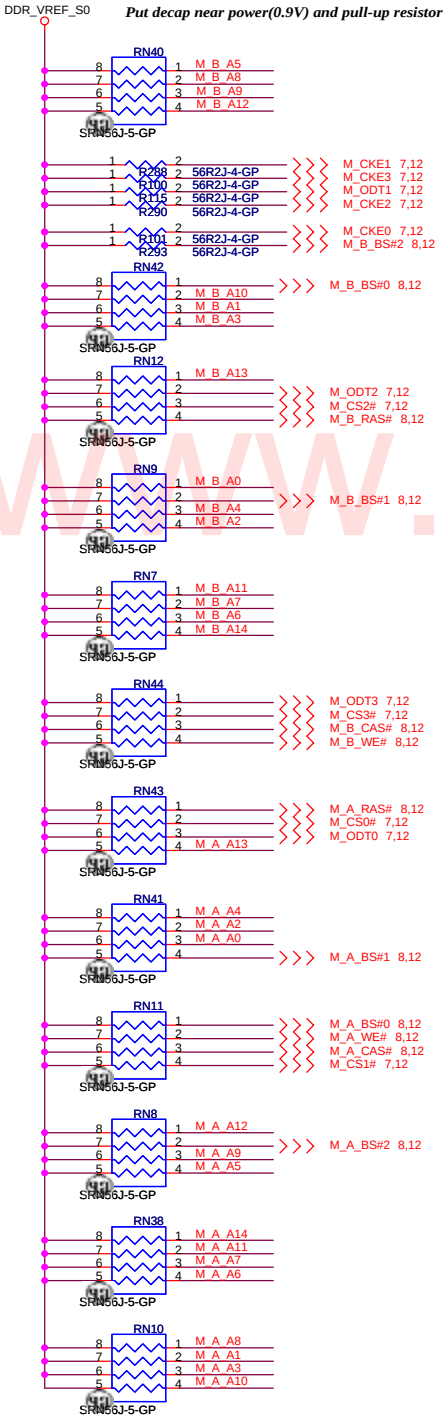


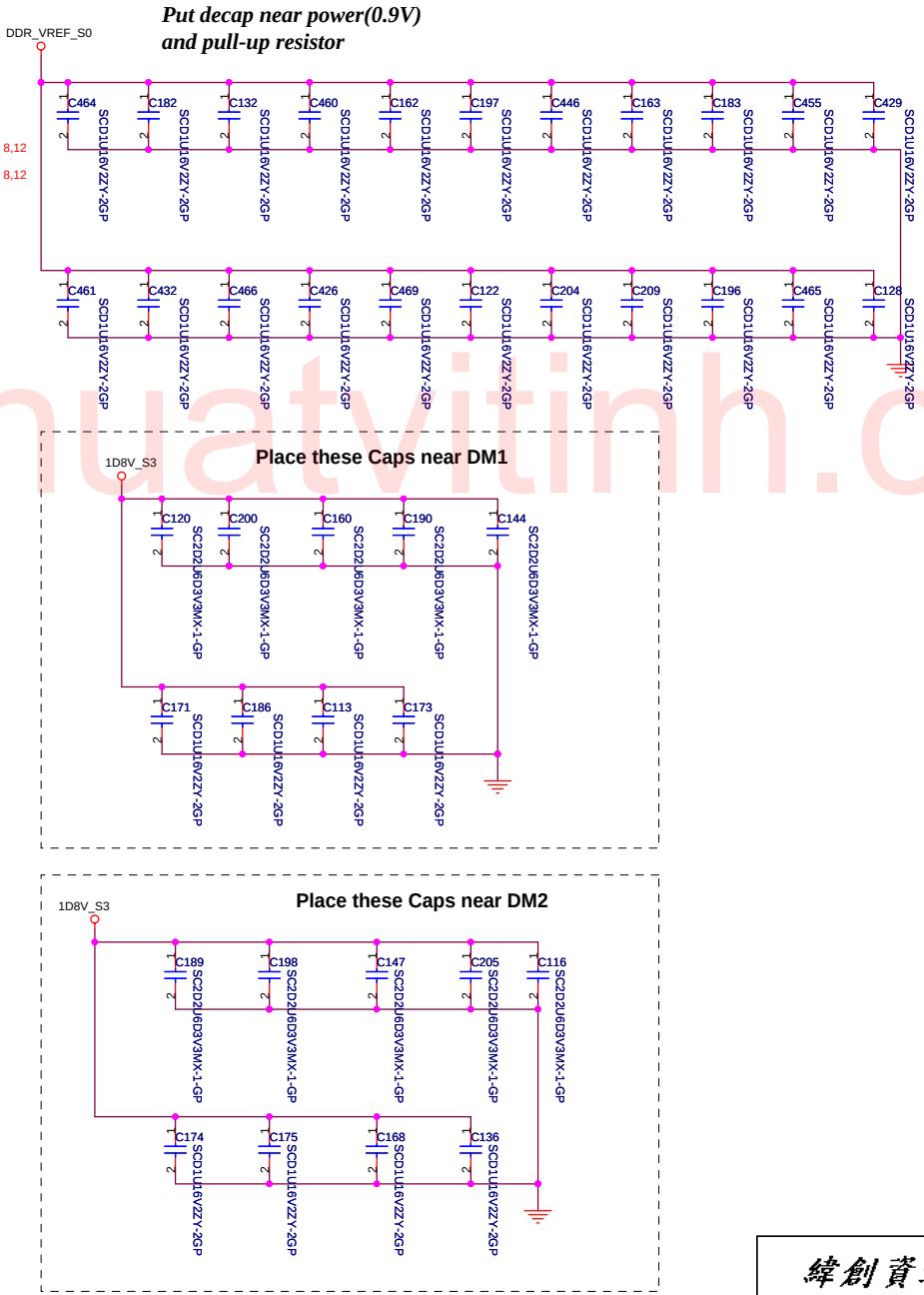
PARALLEL TERMINATION



M_A_A[14..0] M_A_A[14..0] 8,12

M_B_A[14..0] M_B_A[14..0] 8,12

Decoupling Capacitor



緯創資通 **Wistron Corporation**
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Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
	Biwa	SB

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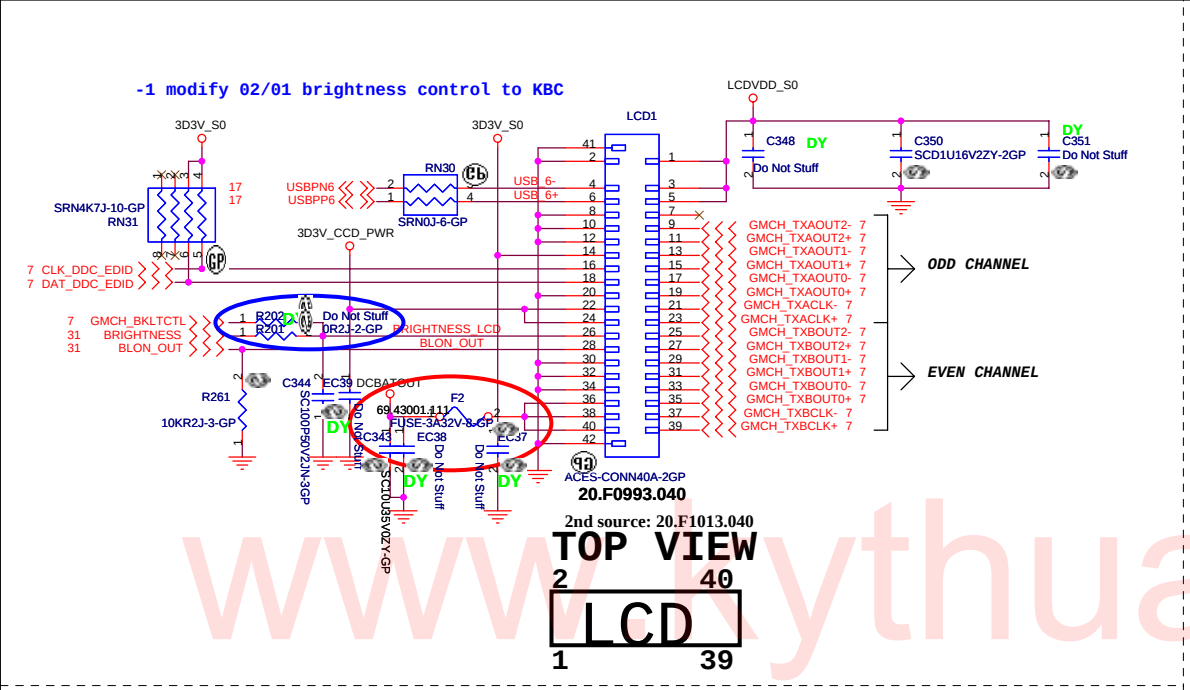

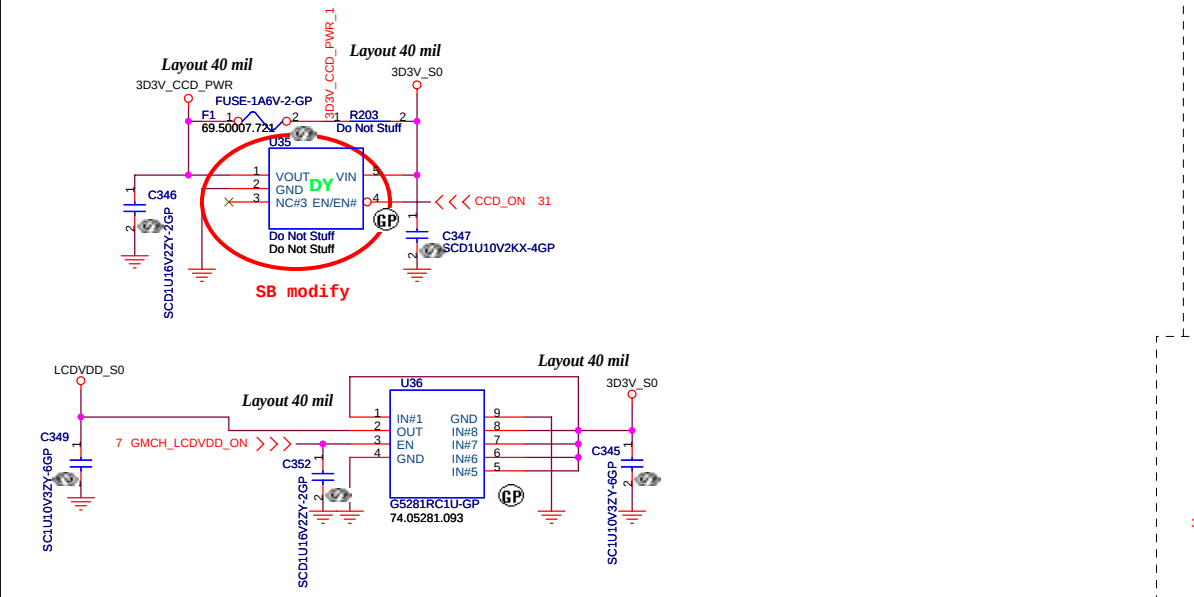

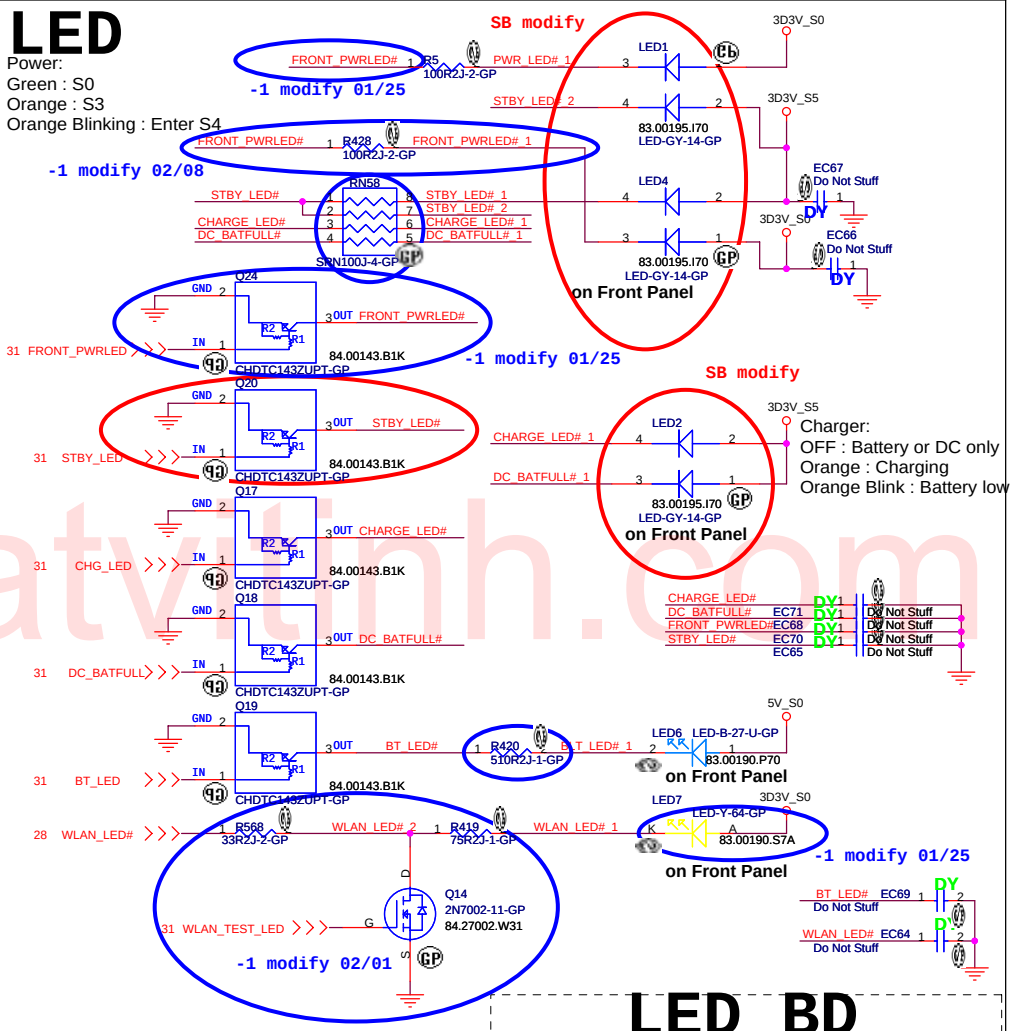

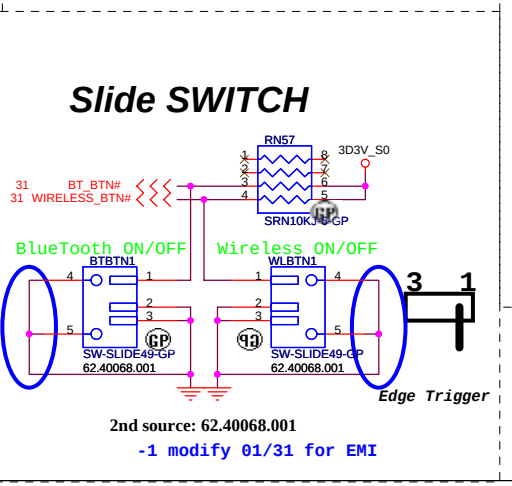

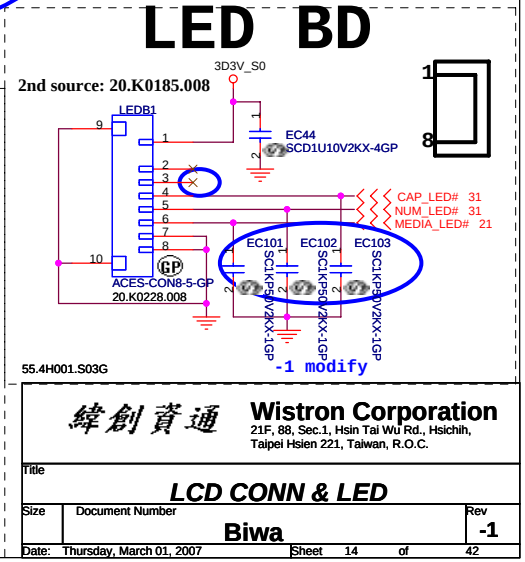

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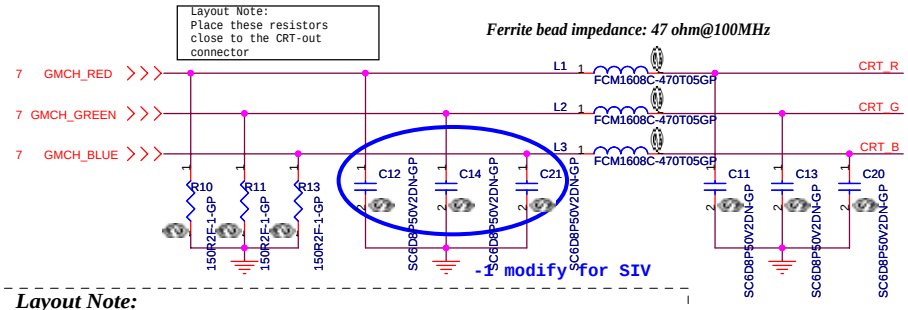
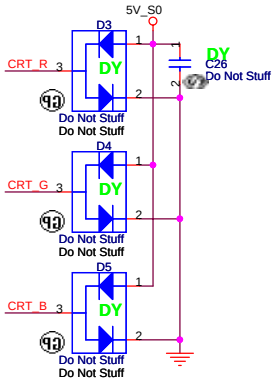
Title: LCD CONN & LED

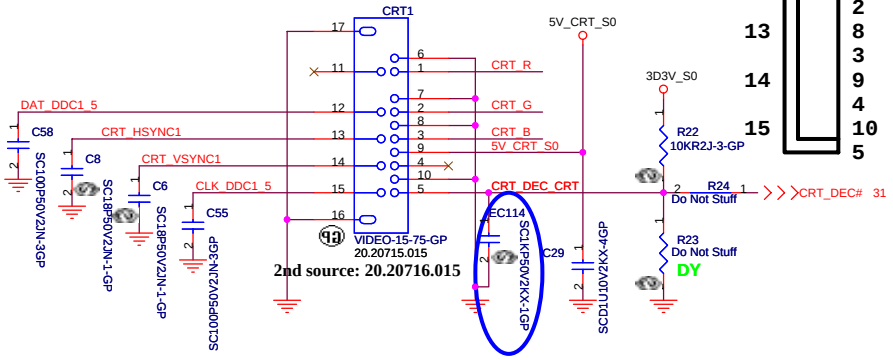
Size	Document Number	Rev
	Biwa	-1

Date: Thursday, March 01, 2007 Sheet 14 of 42

CRT I/F & CONNECTOR

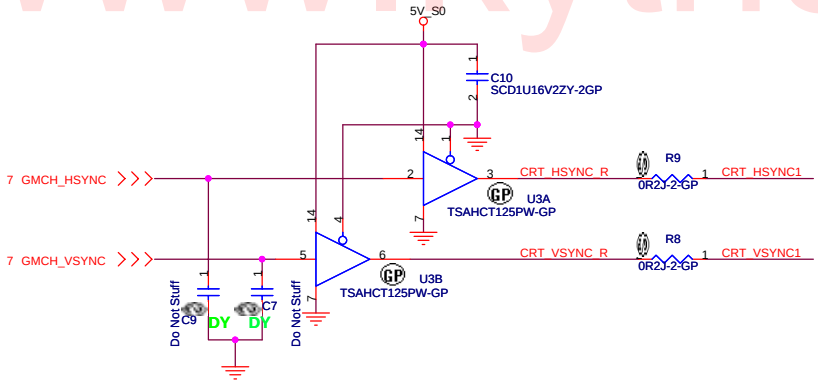


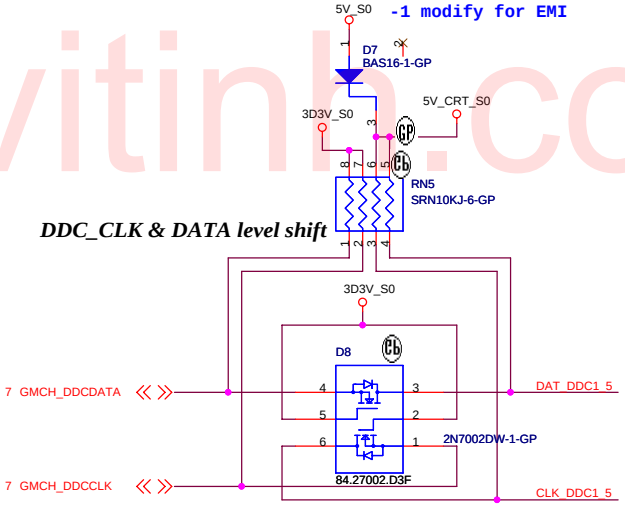




Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

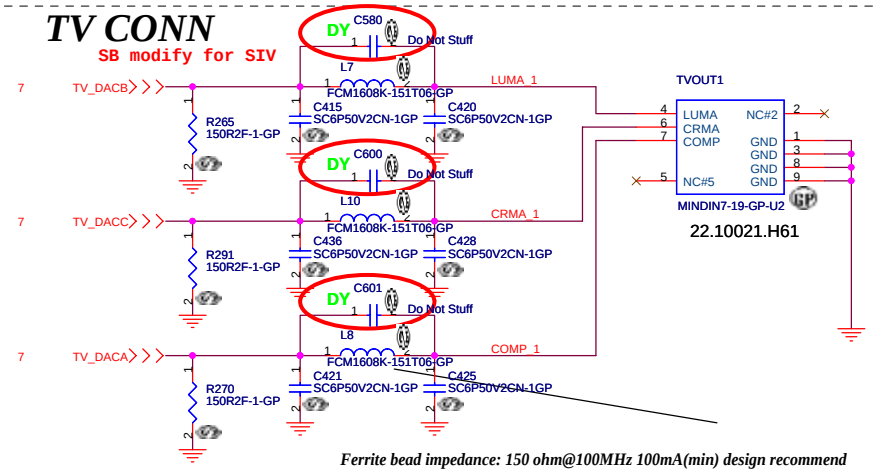
Hsync & Vsync level shift

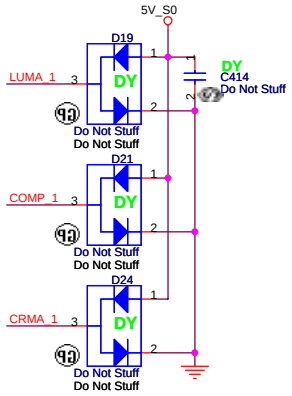




TV CONN

SB modify for SIV





Ferrite bead impedance: 150 ohm@100MHz 100mA(min) design recommend

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CRT/TV Connector**	
Size	Document Number **Biwa**	Rev **-1**
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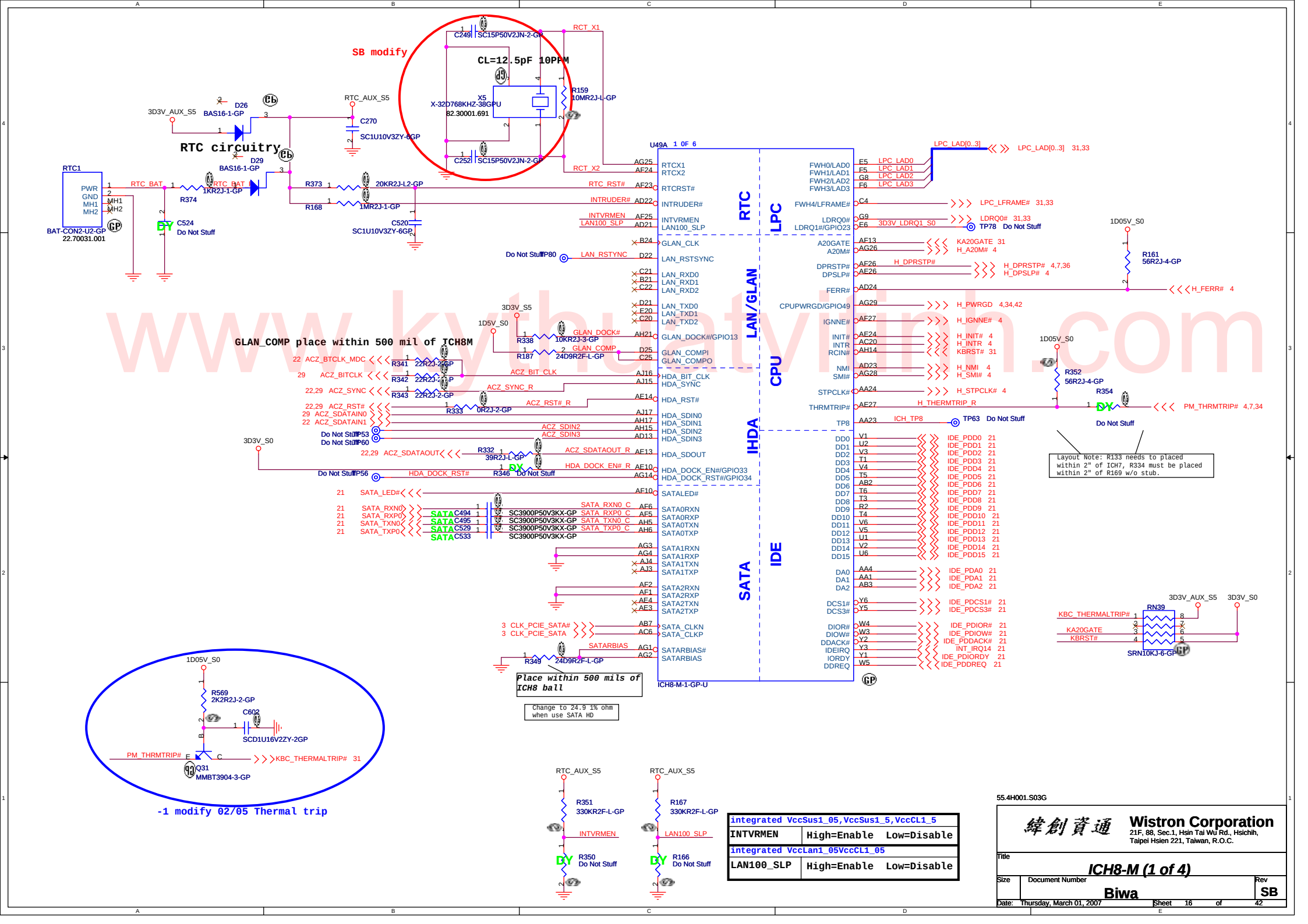

55.4H001.S03G

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Title: ICH8-M (1 of 4)

Size | Document Number: Biwa | Rev: SB

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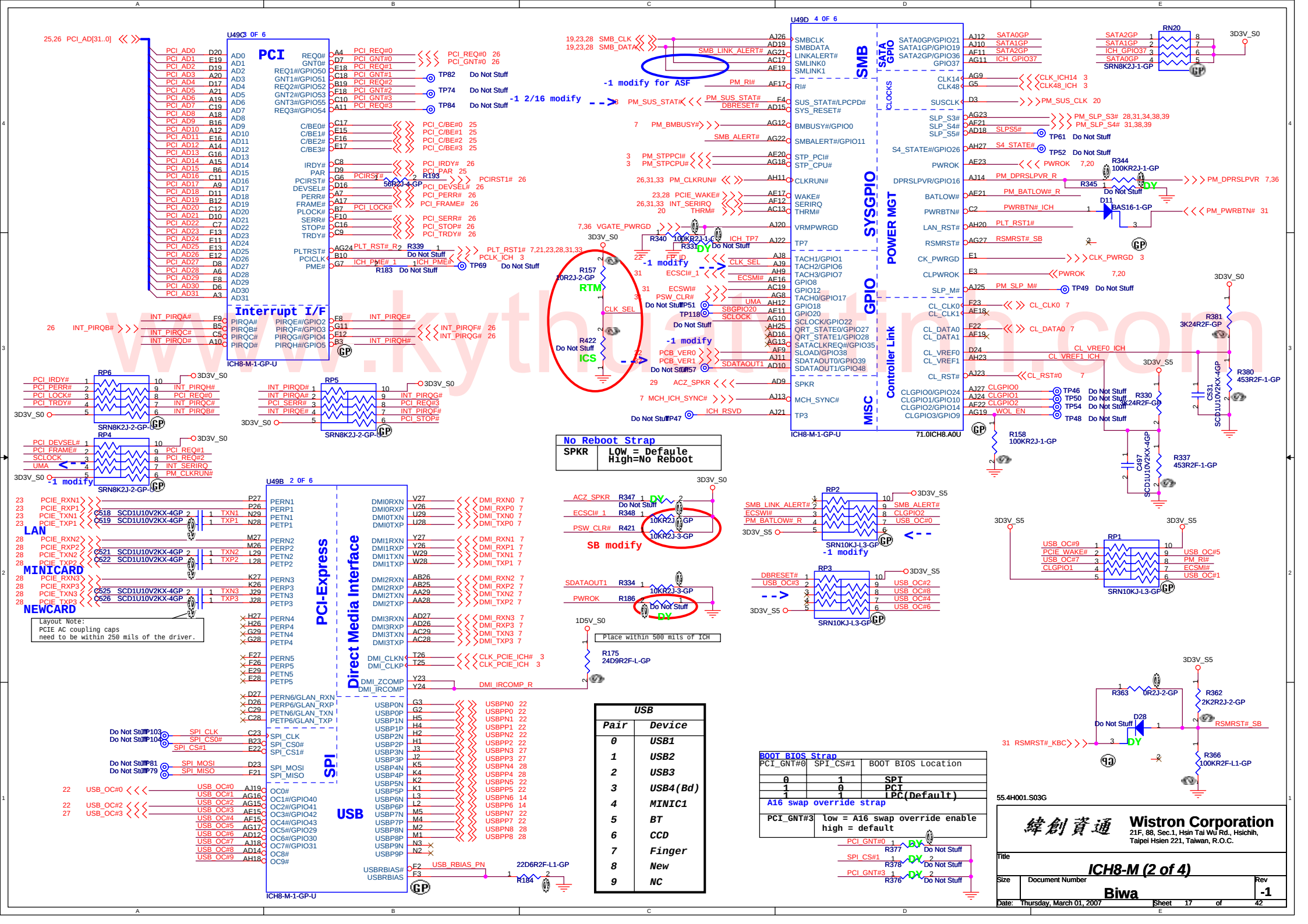
U49C 3 OF 6
PCI
Interrupt I/F
ICH8-M-1-GP-U
U49D 4 OF 6
SMB
SATA GPIO
CLOCKS
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
ICH8-M-1-GP-U
71.0ICH8.A0U
U49B 2 OF 6
PCI-Express
Direct Media Interface
SPI
USB
ICH8-M-1-GP-U
-1 modify for ASF
-1 2/16 modify
-1 modify
RTM
ICS
SB modify
LAN
MINICARD
NEWCARD
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
No Reboot Strap
SPKR | LOW = Defaule
High=No Reboot
Place within 500 mils of ICH
USB
Pair | Device
0 | USB1
1 | USB2
2 | USB3
3 | USB4(Bd)
4 | MINIC1
5 | BT
6 | CCD
7 | Finger
8 | New
9 | NC
BOOT BIOS Strap
PCI_GNT#0 | SPI_CS#1 | BOOT BIOS Location
0 | 1 | SPI
1 | 0 | PCI
1 | 1 | LPC(Default)
A16 swap override strap
PCI_GNT#3 | low = A16 swap override enable
high = default
55.4H001.S03G
Wistron Corporation
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Title
ICH8-M (2 of 4)
Size
Document Number
Biwa
Rev
-1
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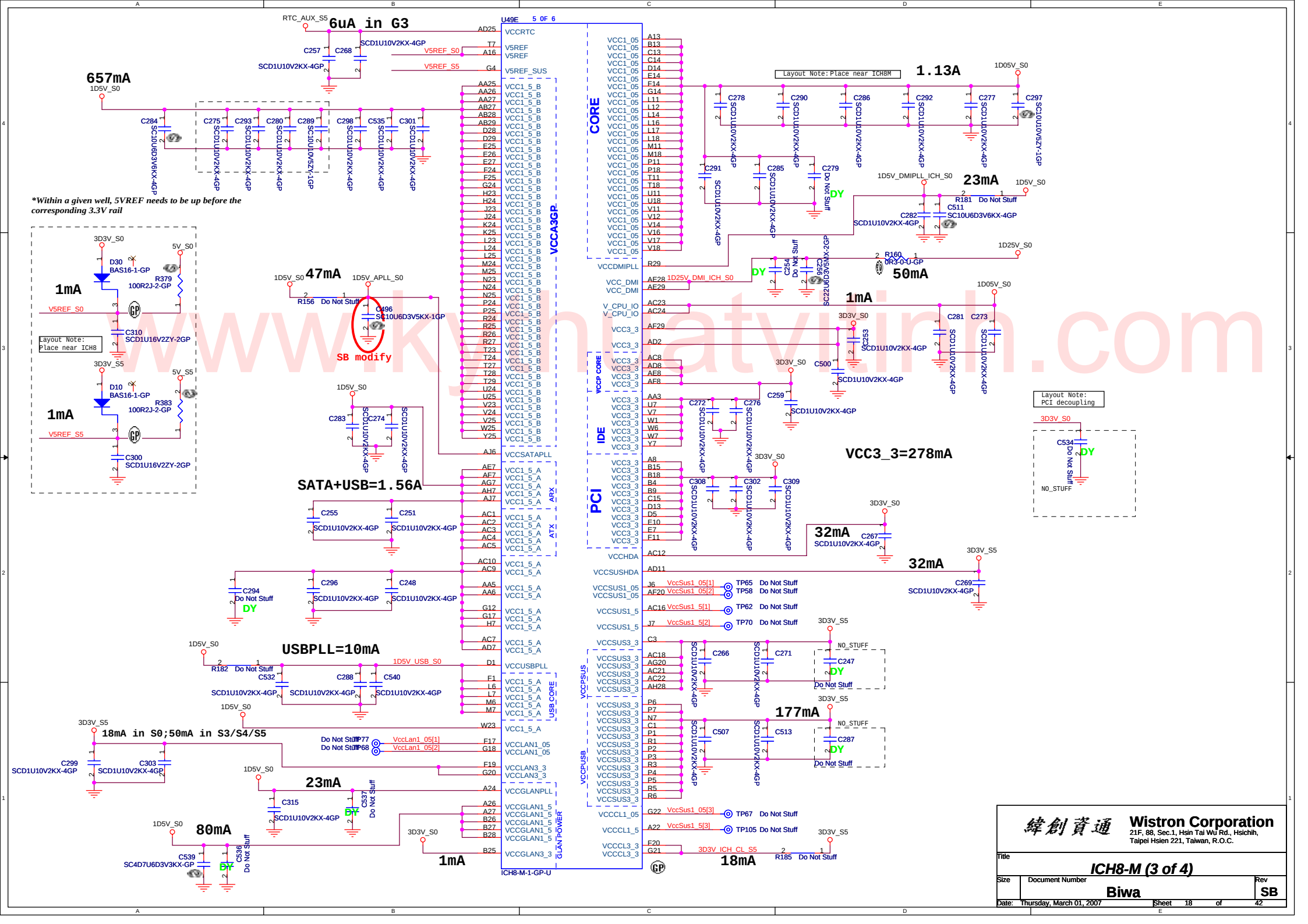
6uA in G3
657mA
1.13A
23mA
47mA
1mA
50mA
SB modify
SATA+USB=1.56A
USBPLL=10mA
18mA in S0;50mA in S3/S4/S5
23mA
80mA
1mA
VCC3_3=278mA
32mA
32mA
177mA
18mA
1mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near ICH8M
Layout Note: Place near ICH8
Layout Note: PCI decoupling
U49E 5 OF 6
ICH8-M-1-GP-U
CORE
VCCA3GP
IDE
PCI
USB CORE
GLAN POWER
Do Not Stuff
NO_STUFF
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH8-M (3 of 4)
Biwa
SB
Thursday, March 01, 2007
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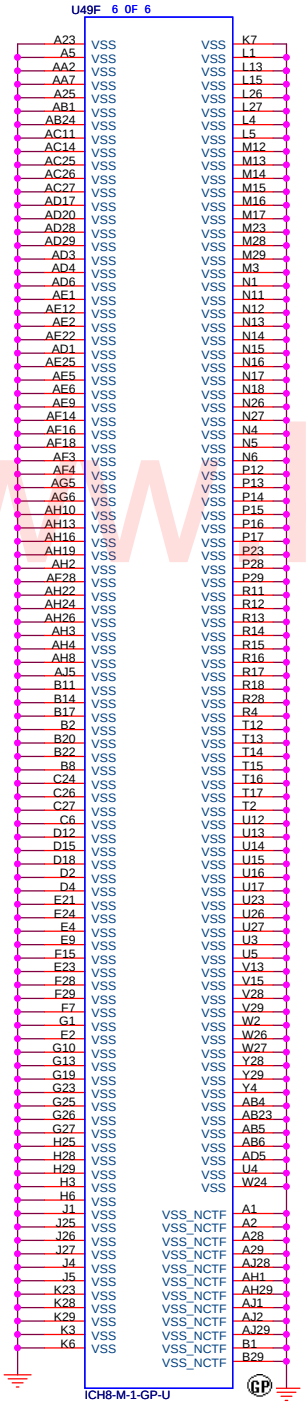

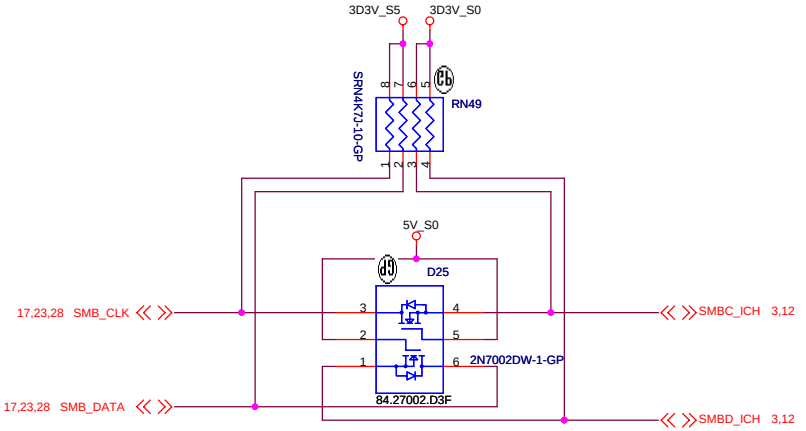

D55 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

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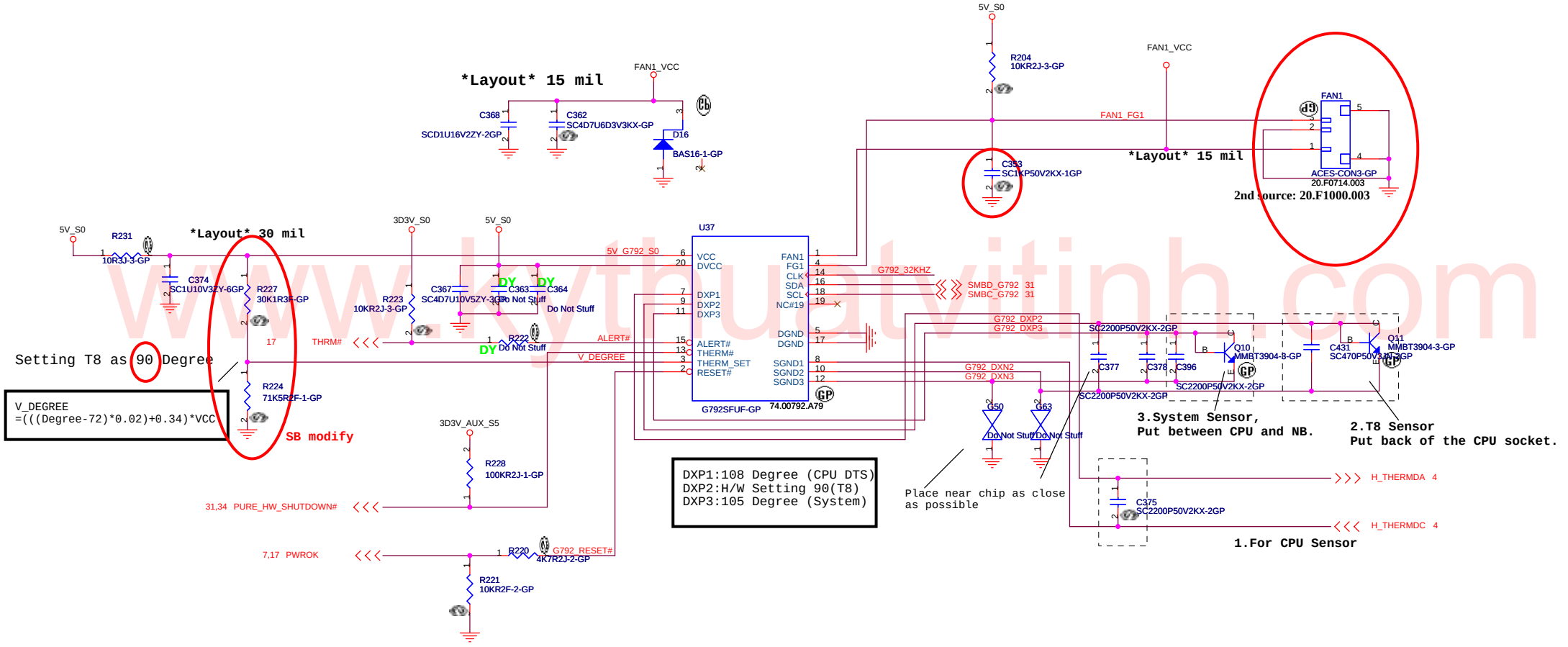
Title	*ICH8-M (4 of 4)*	
Size	Document Number: **Biwa**	Rev: SA
Date: Thursday, March 01, 2007	Sheet 19 of 42	



TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

Biwa Thermal Table 1106

		T6	T7
Sencor 0	CPU DTS	100	102
Sencor 1	CPU G792 Analog	110	113
Sencor 2	System G792	85	87
Sencor 3	T8		
Sencor 4	ADIA status		

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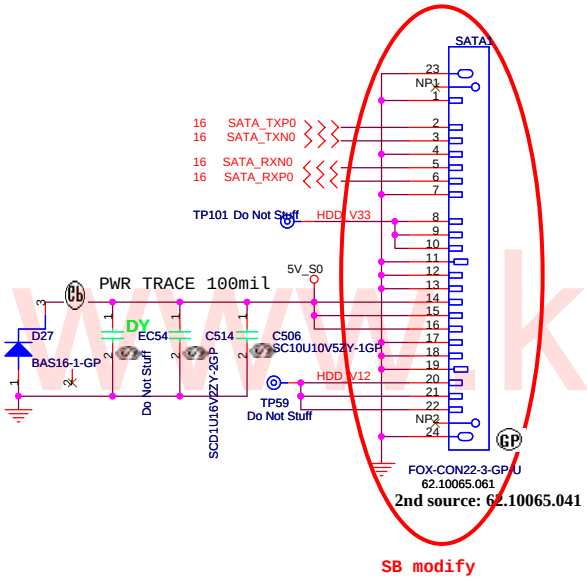
Title: Thermal/Fan Controllor

Size | Document Number: Biwa | Rev: SB

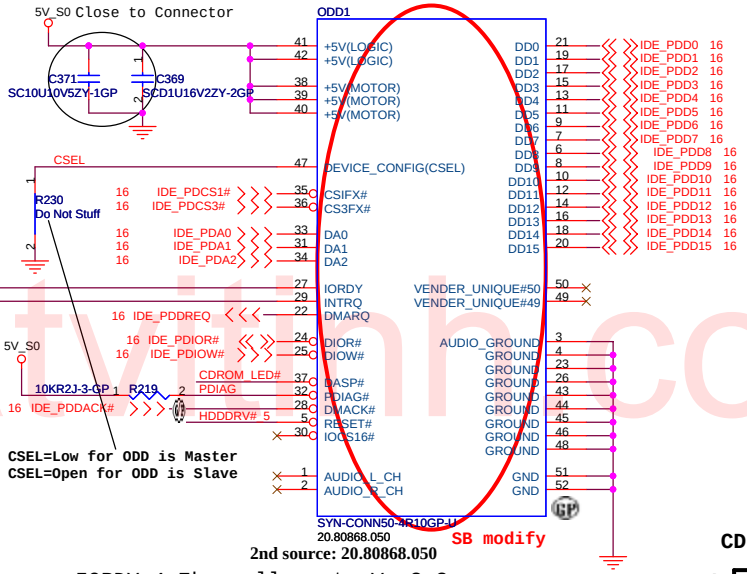
Date: Thursday, March 01, 2007 | Sheet 20 of 42

SATA Connector



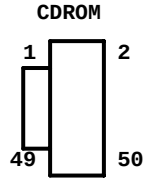
SB modify

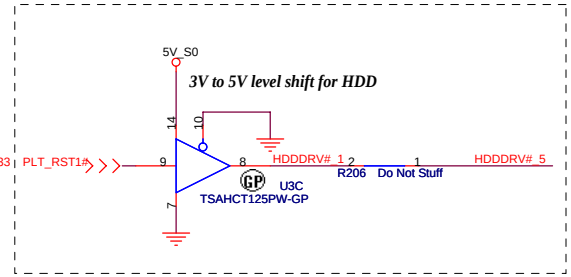
ODD Connector

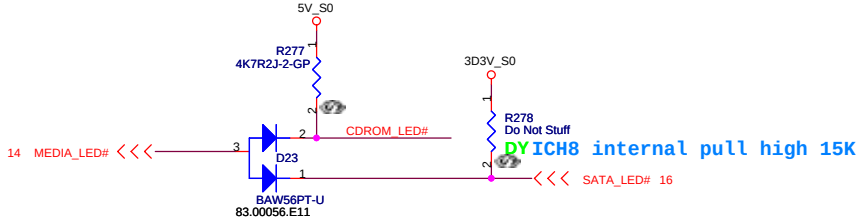


SB modify

IORDY 4.7k pull-up to Vcc3_3
IDEIRQ 8.2k to 10k pull-up to Vcc3_3







ICH8 internal pull high 15K

55.4H001.S03G

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Title: HDD and CDROM

Size	Document Number	Rev
	Biwa	SB

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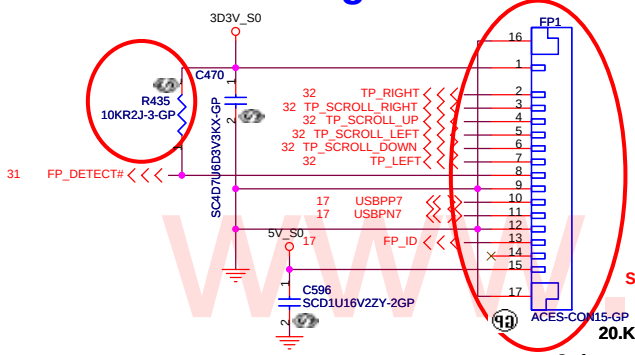
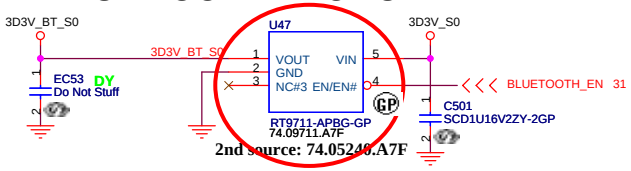
Finger Print



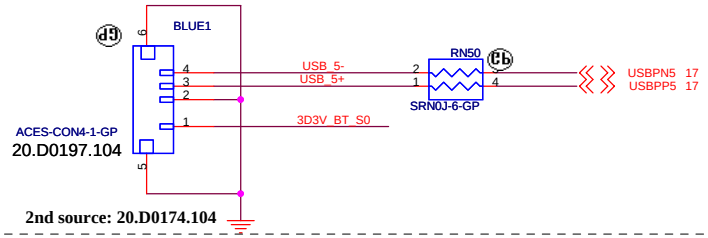
2nd source: 20.K0185.015

BLUETOOTH MODULE



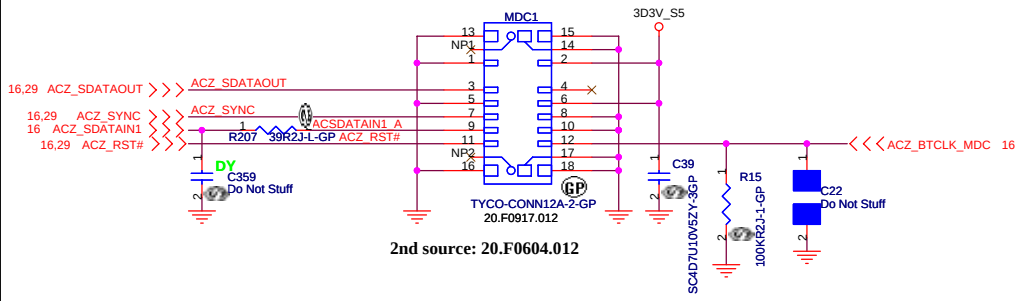
2nd source: 74.05240.A7F

EC21 put near BLUE1 / all USB put one choke near connector by EMI request



2nd source: 20.D0174.104

MDC 1.5 CONN



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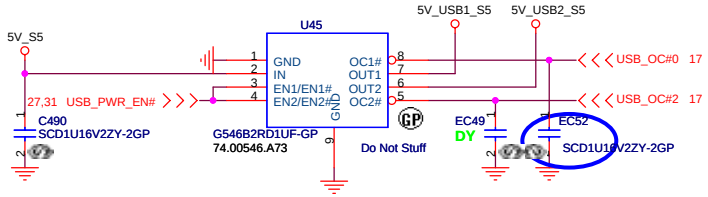
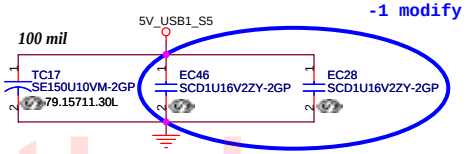
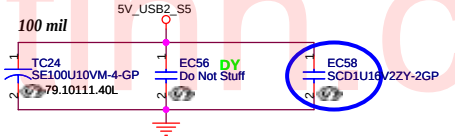
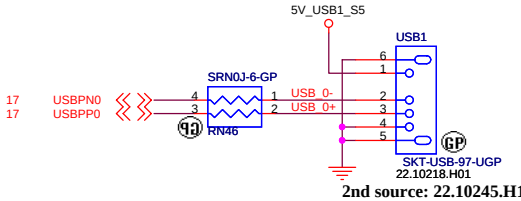


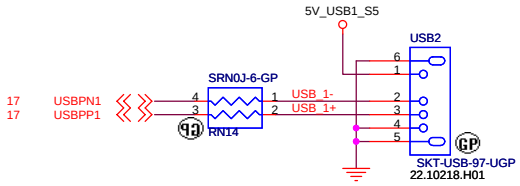
-1 modify for EMC



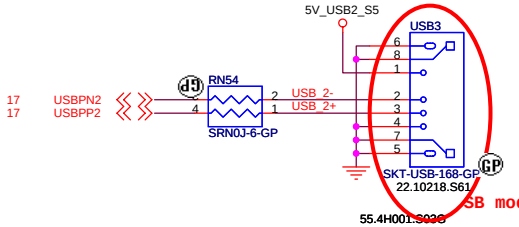




2nd source: 22.10245.H11



2nd source: 22.10245.H11



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Title: USB / MDC / BLUETOOTH / FP

Size | Document Number: Biwa | Rev: -1

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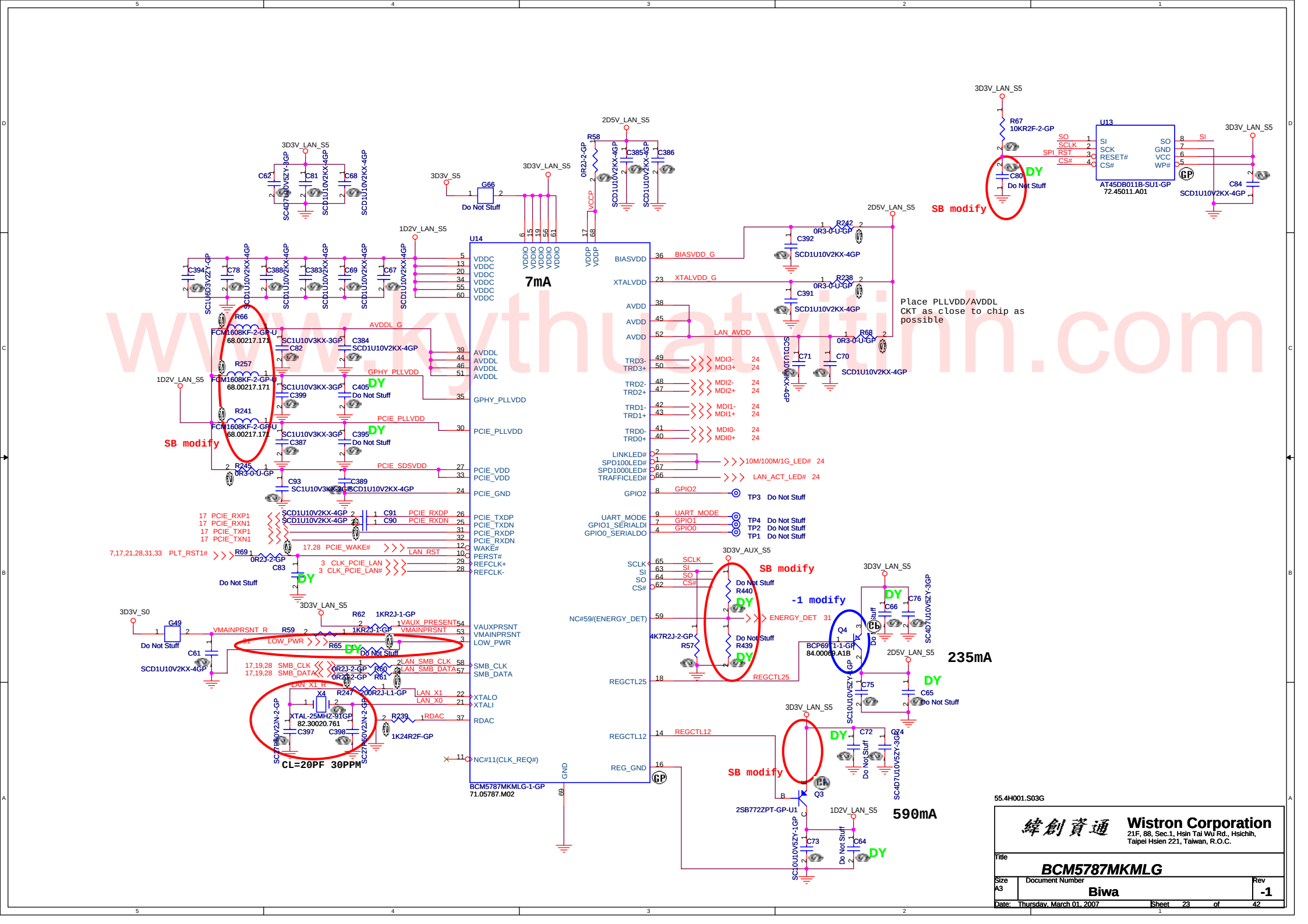
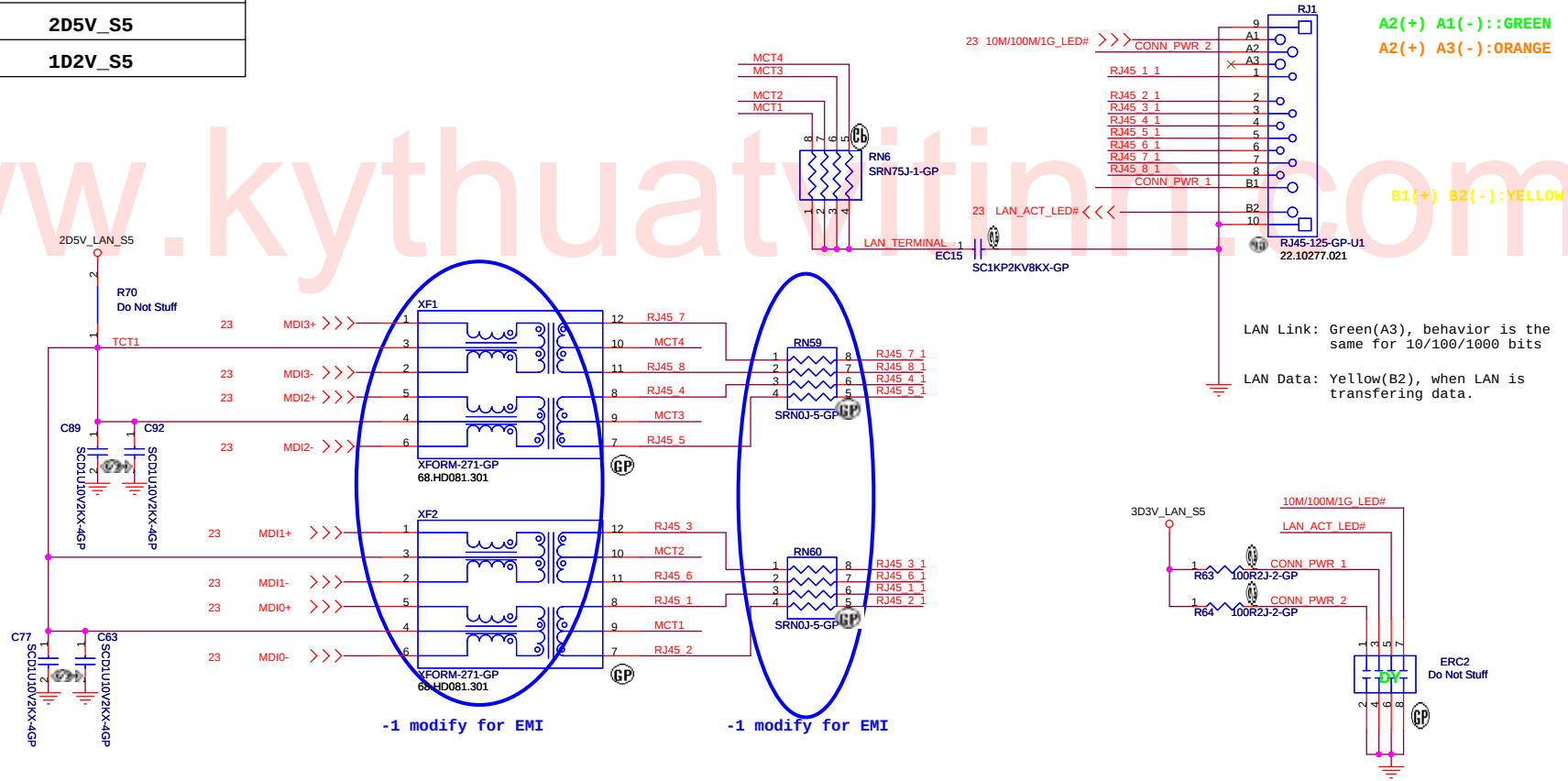


Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

LAN Connector



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

55.4H001.S03G

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Title: **LAN Connector**

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C782 should close Pin-P15
and Pin-R17.

TI PCI7412

U34A

1 0F 2

71.07412.B0U

PCI7412ZHK-GP

* All 1394 signals must be routed on top side only
* Differential pairs of each ports should have equal trace length
* Stubs must be keep as short as possible

Bypass/Decupoling Capacitors
Should be places as close to
PCI7412 as possible

55.4H001.S03G

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: TI PCI7412 (1 of 2)

Size | Document Number: Biwa | Rev: SA

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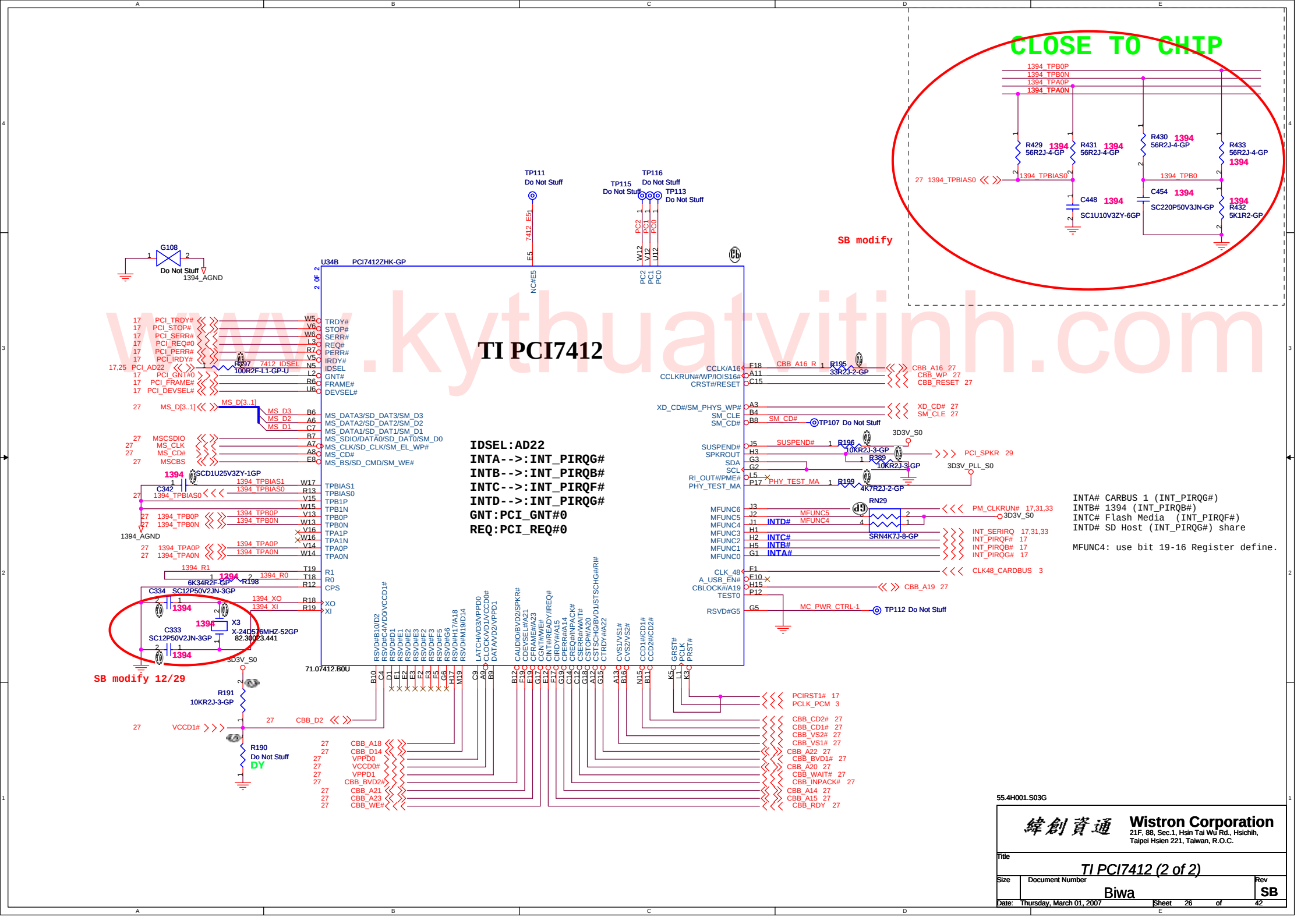
CLOSE TO CHIP
SB modify
TI PCI7412
U34B PCI7412ZHK-GP
IDSEL:AD22
INTA-->:INT_PIRQG#
INTB-->:INT_PIRQB#
INTC-->:INT_PIRQF#
INTD-->:INT_PIRQG#
GNT:PCI_GNT#0
REQ:PCI_REQ#0
INTA# CARBUS 1 (INT_PIRQG#)
INTB# 1394 (INT_PIRQB#)
INTC# Flash Media (INT_PIRQF#)
INTD# SD Host (INT_PIRQG#) share
MFUNC4: use bit 19-16 Register define.
SB modify 12/29
Do Not Stuff
DY
55.4H001.S03G
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TI PCI7412 (2 of 2)
Size
Document Number
Biwa
Rev
SB
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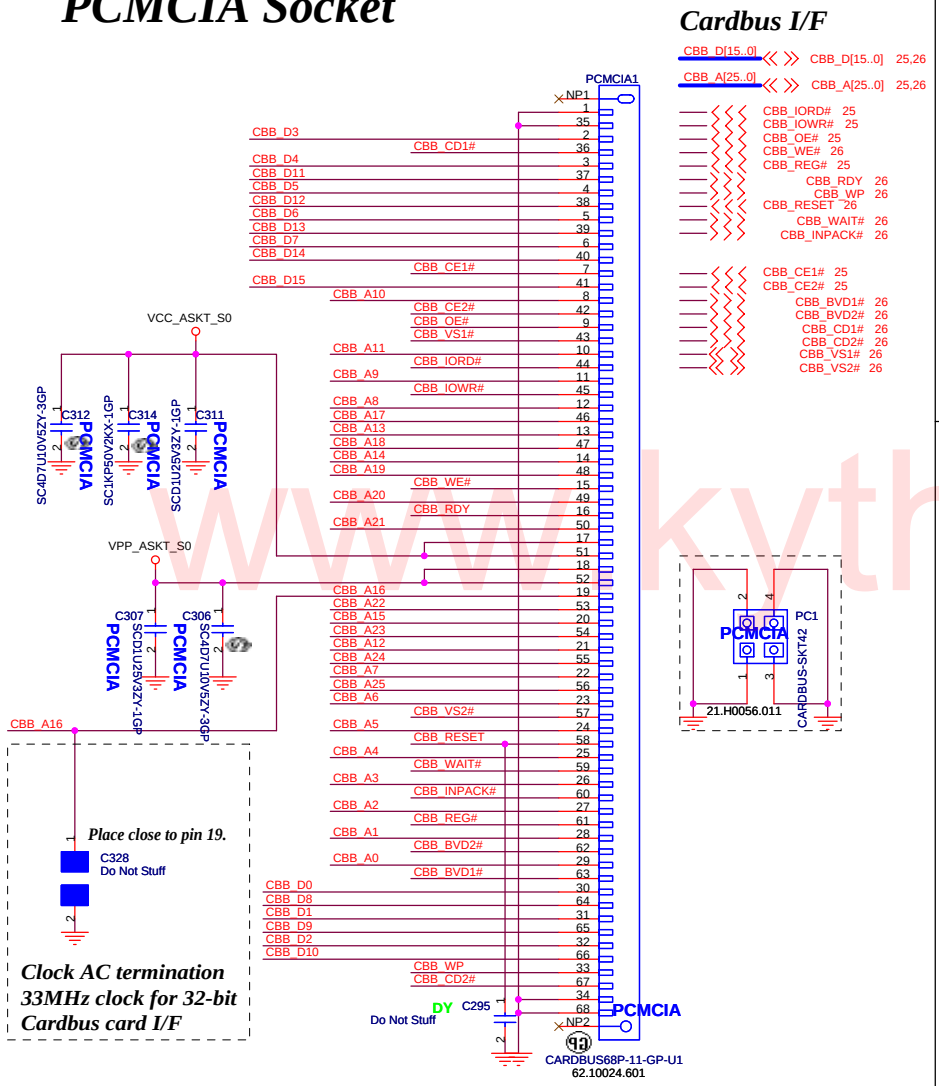
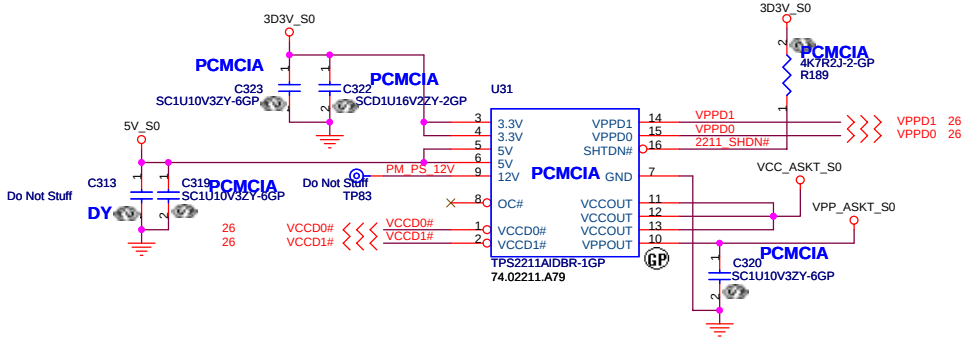
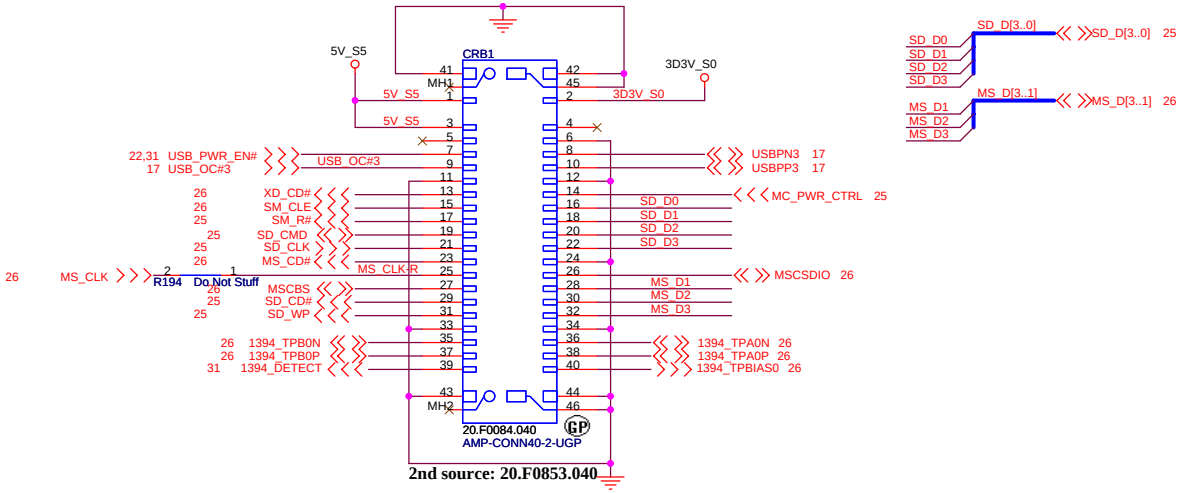
Sheet 26 of 42

PCMCIA Socket







XD
MS / MS PRO
SD / SD IO / MMC

55.4H001.S03G

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA / CARD READER BD

Size	Document Number	Rev
	Biwa	SA

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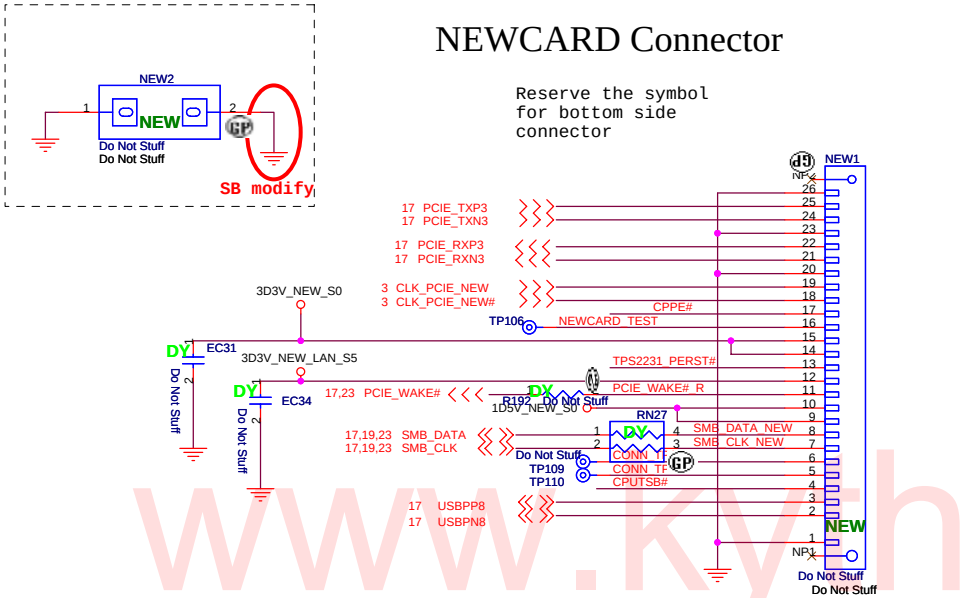
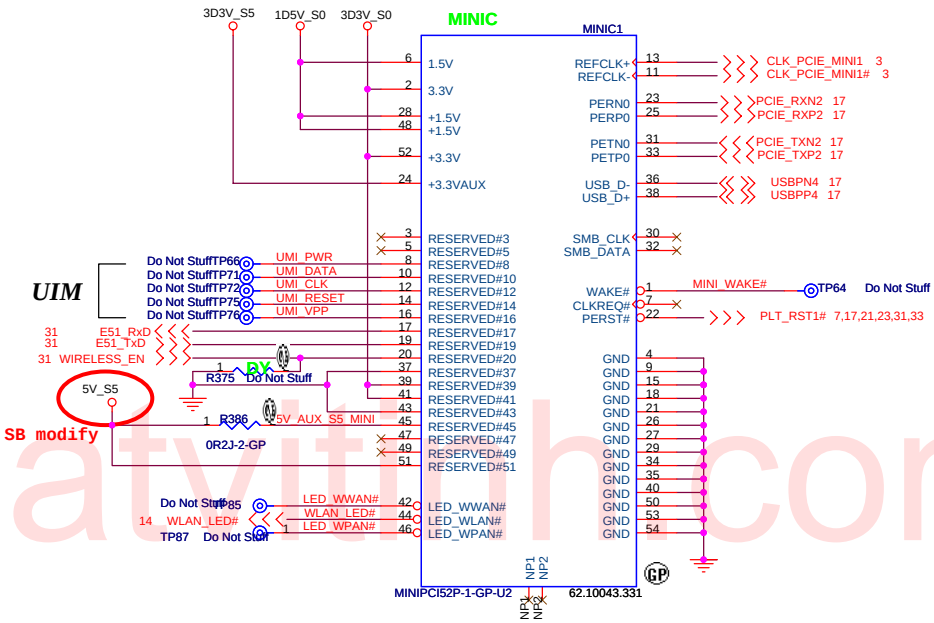
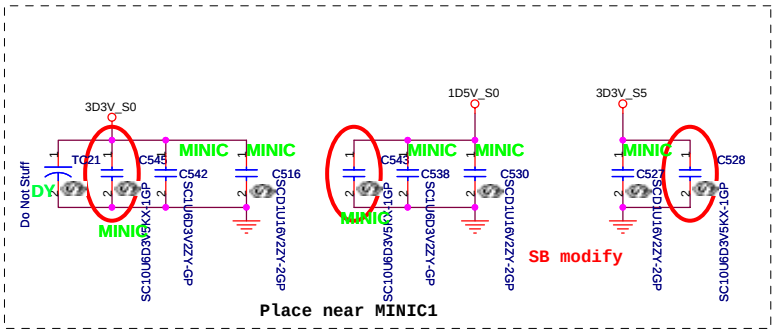
NEWCARD Connector



Mini Card Connector

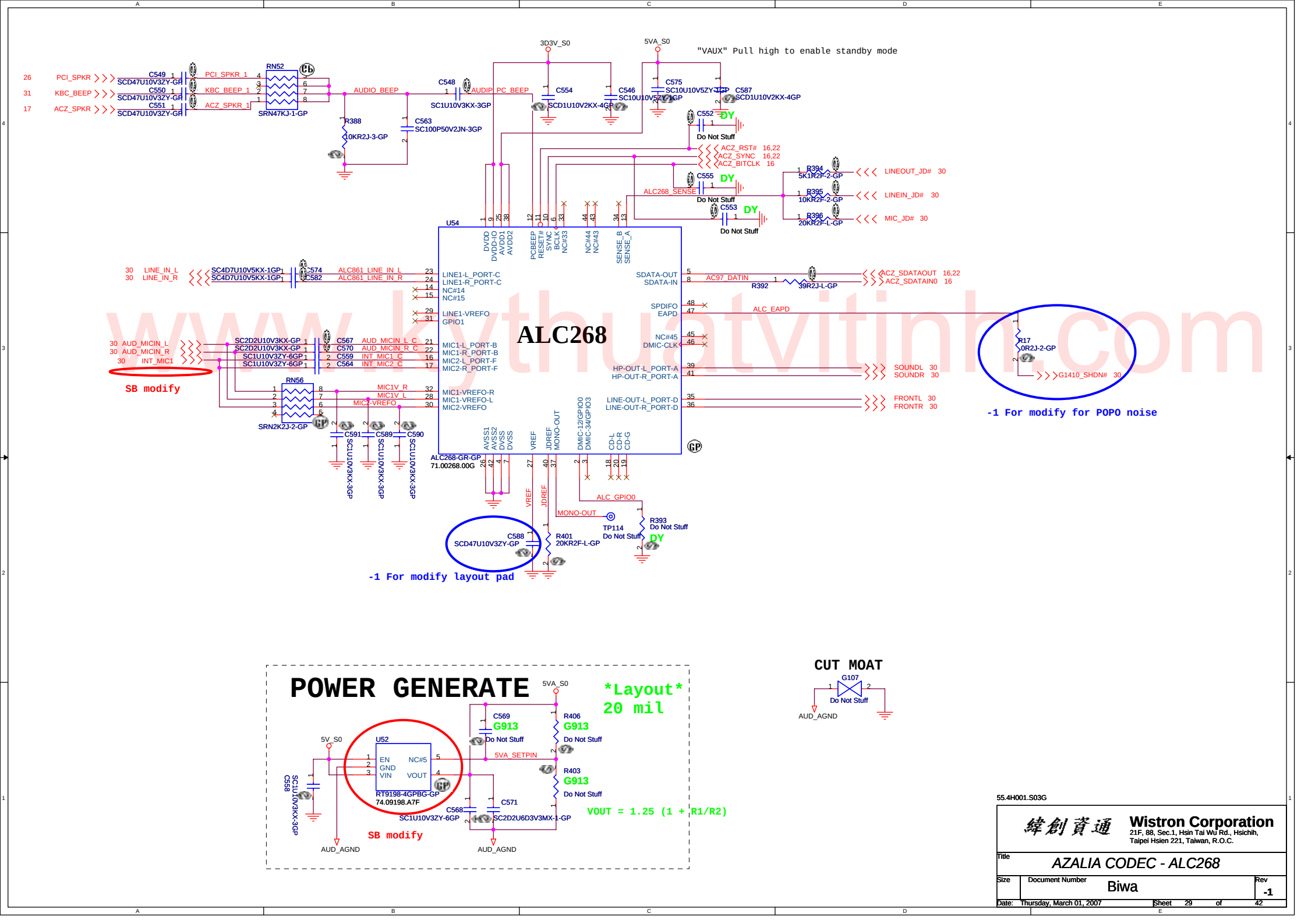




55.4H001.S03G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MINI CARD / NEW CARD	
Size	Document Number: Biwa	Rev: SB
Date: Thursday, March 01, 2007	Sheet 28 of 42	



55.4H001.S03G

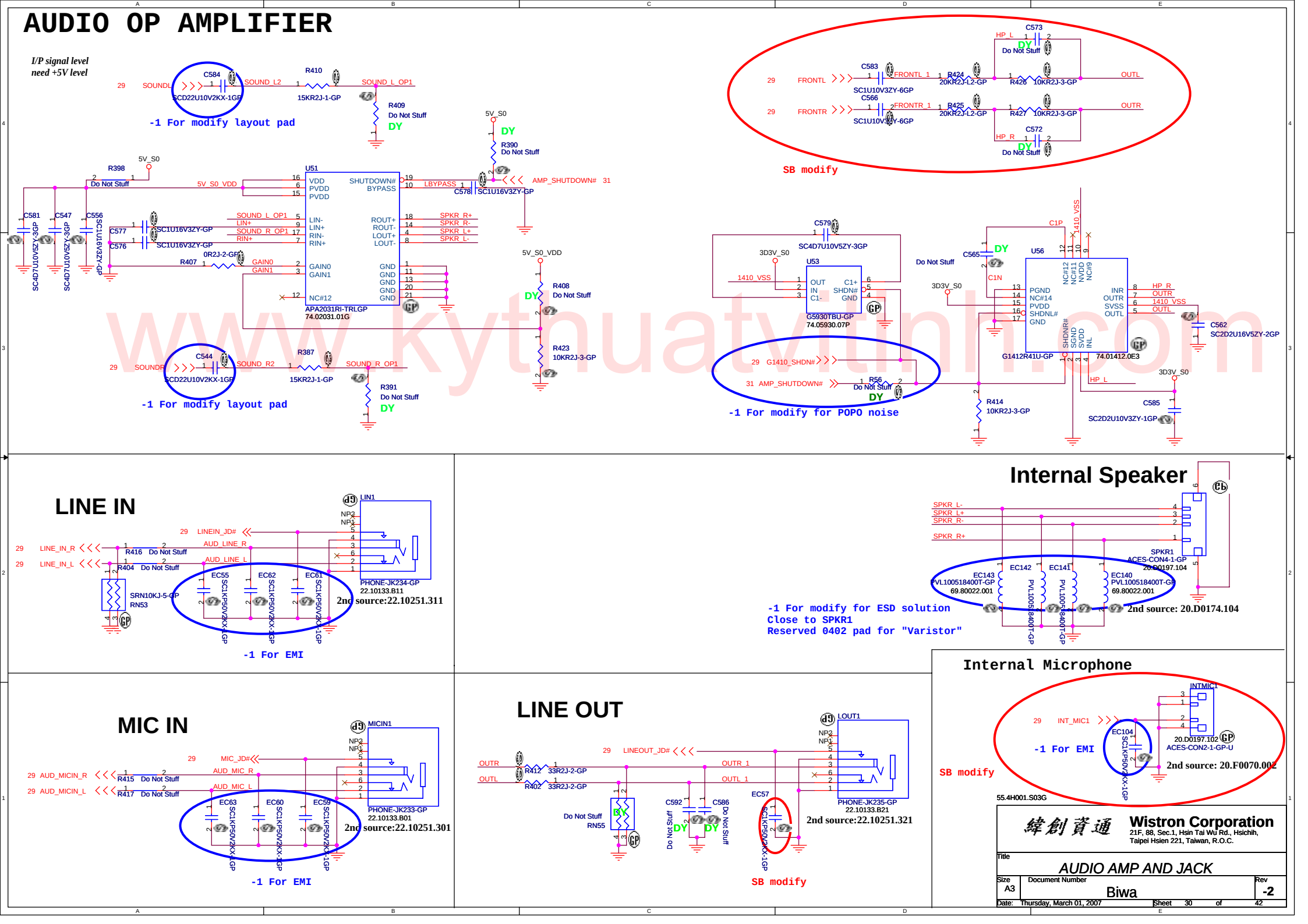
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

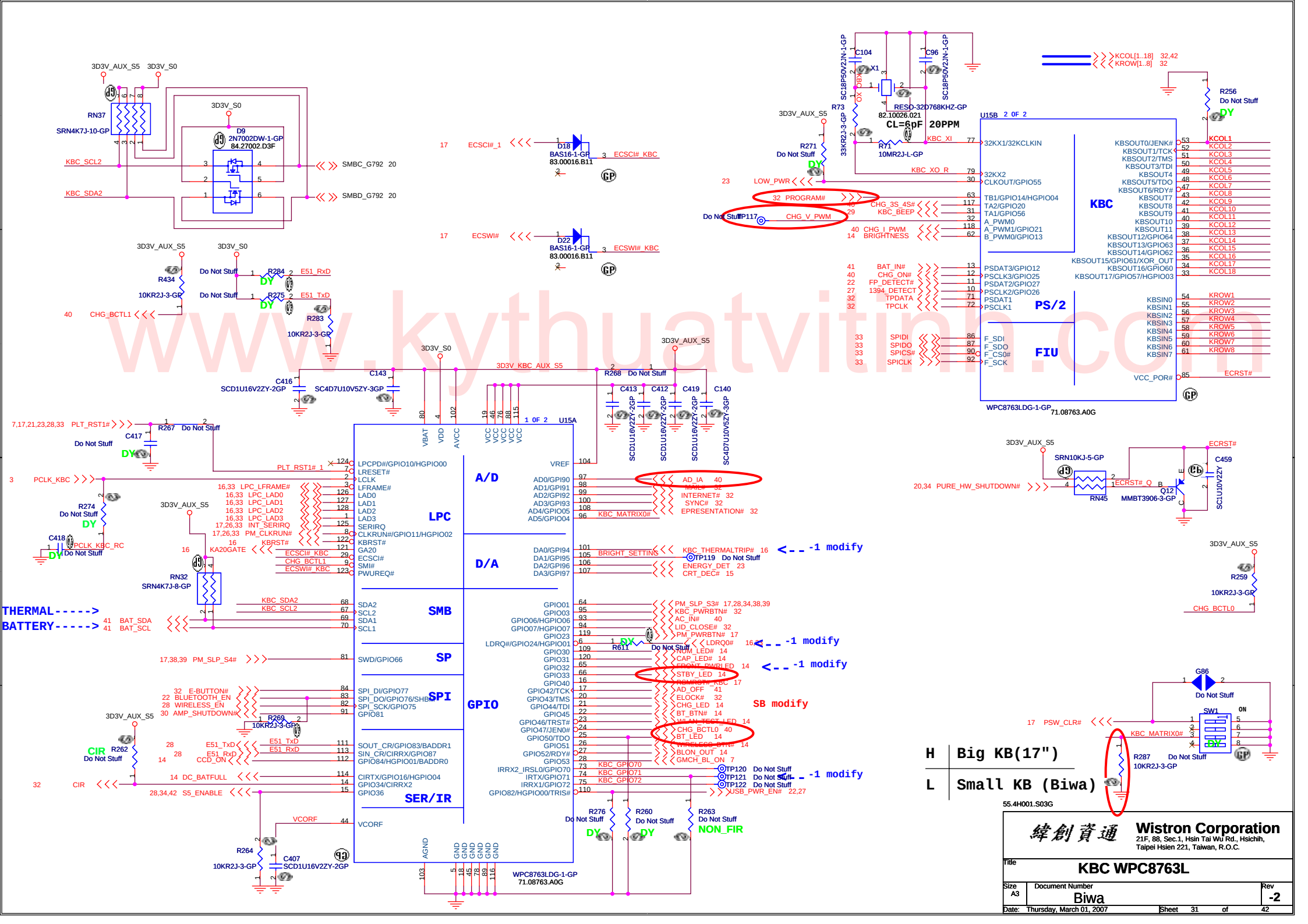
Title: AZALIA CODEC - ALC268

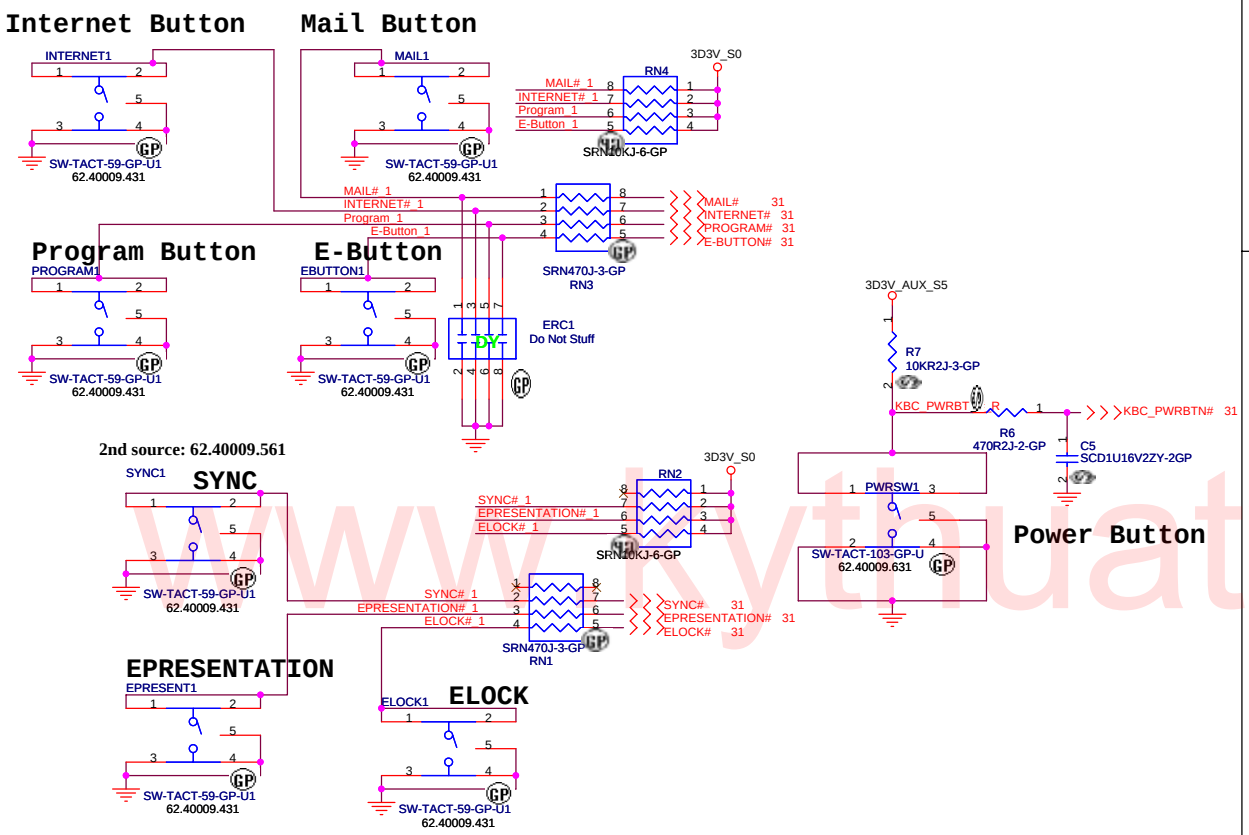
Size | Document Number: Biwa | Rev: -1

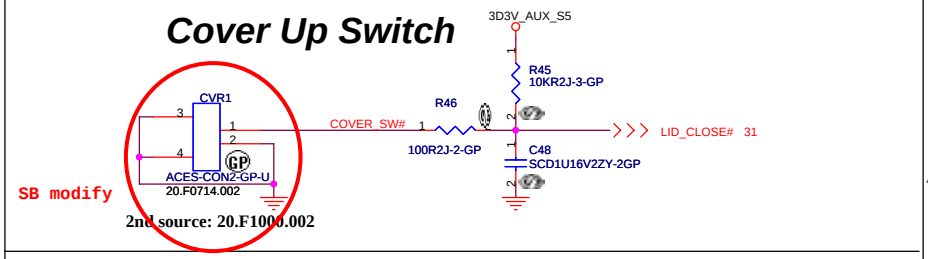
Date: Thursday, March 01, 2007 | Sheet 29 of 42

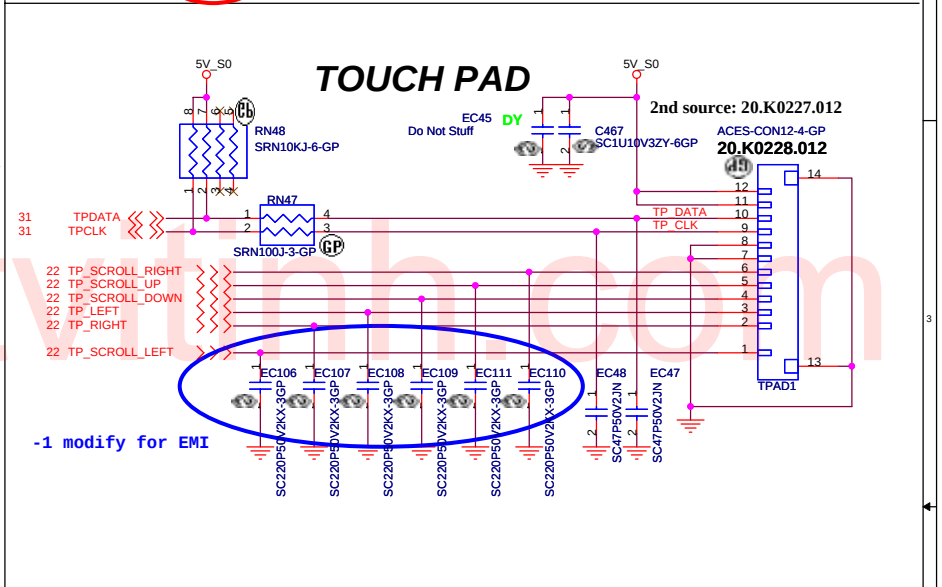
AUDIO OP AMPLIFIER

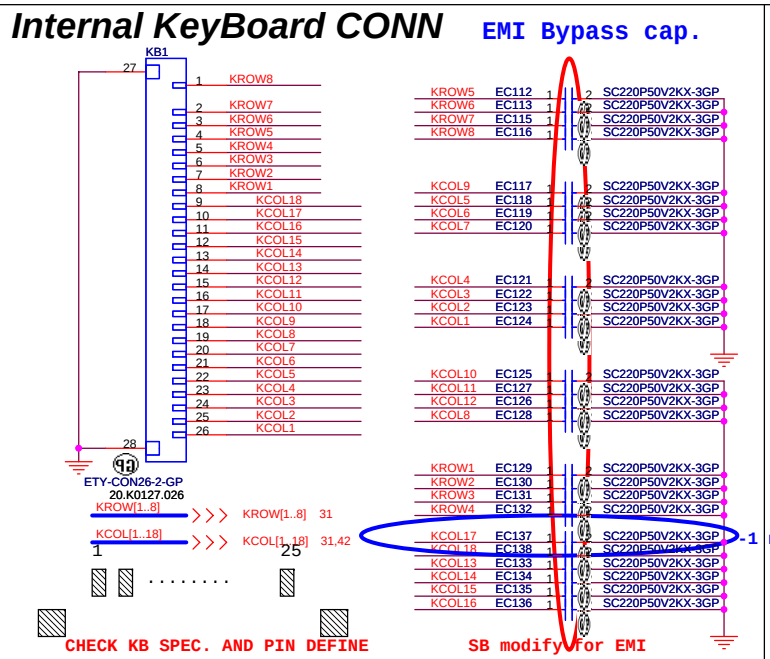


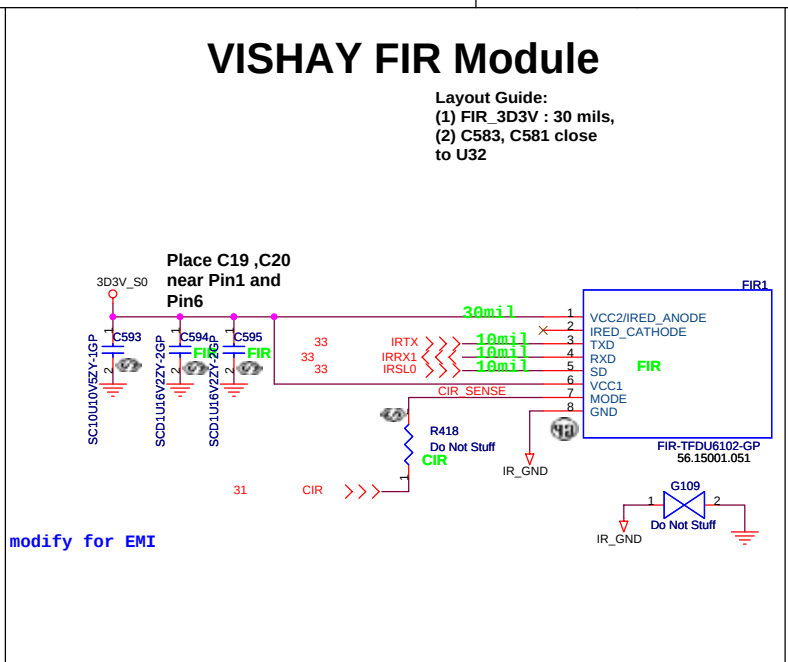


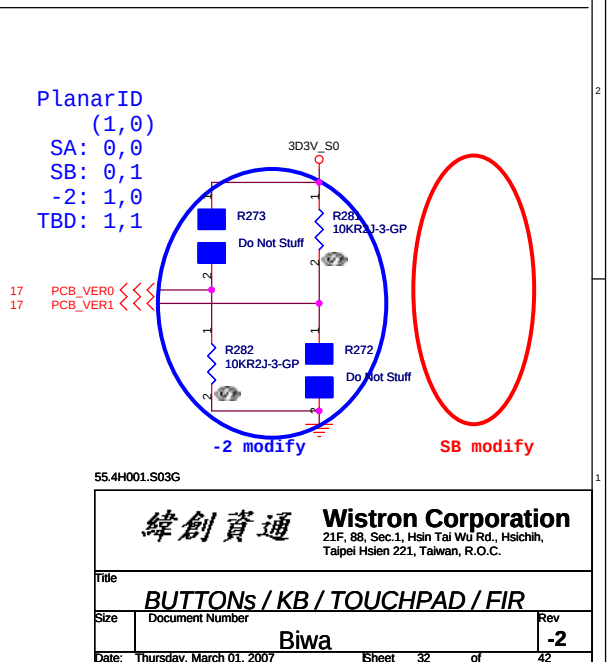












55.4H001.S03G

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*BUTTONs / KB / TOUCHPAD / FIR*	
Size	Document Number: Biwa	Rev: -2
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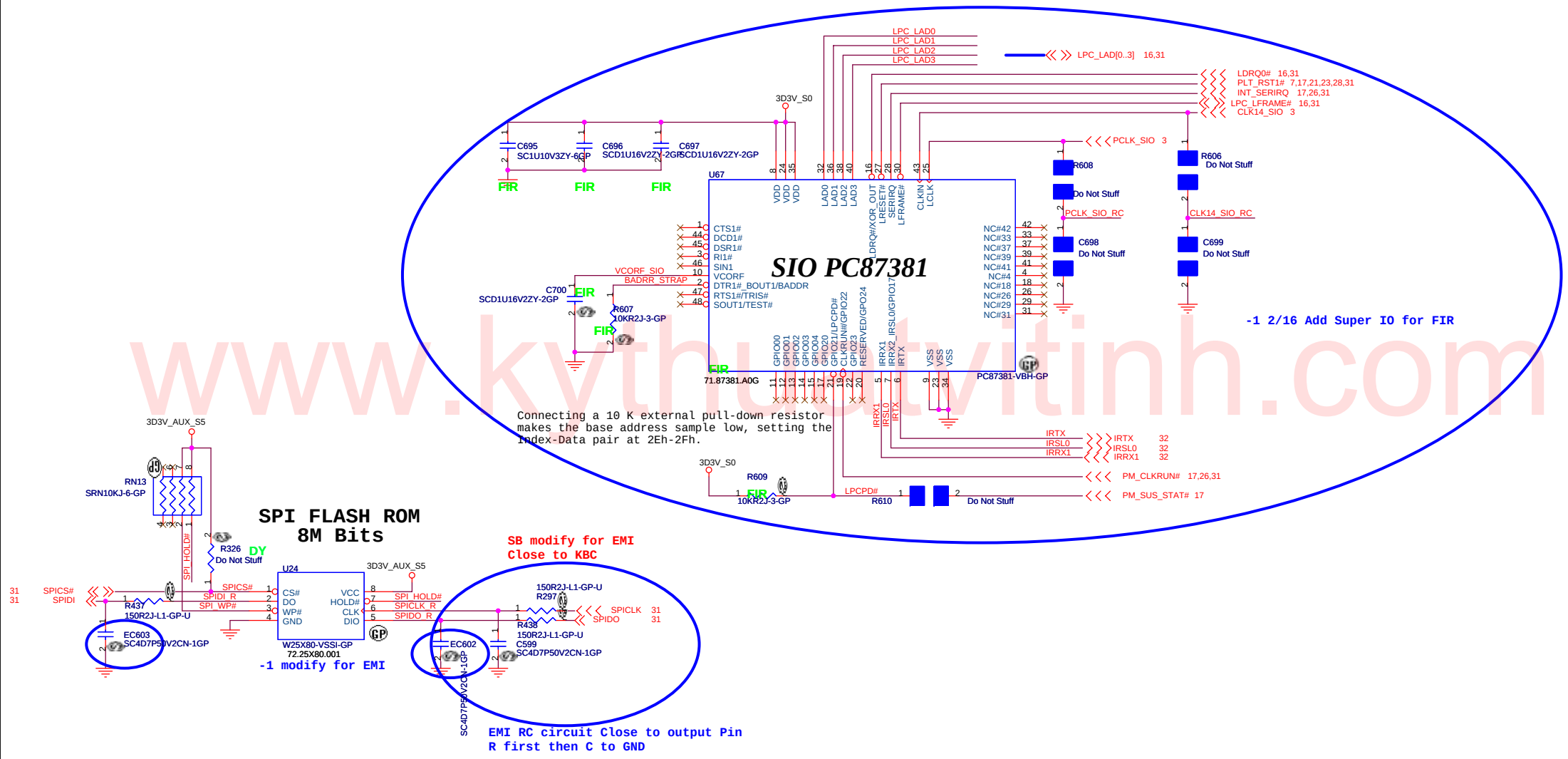

55.4H001.S03G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS & Super IO

Size	Document Number	Rev
A3	Biwa	-2

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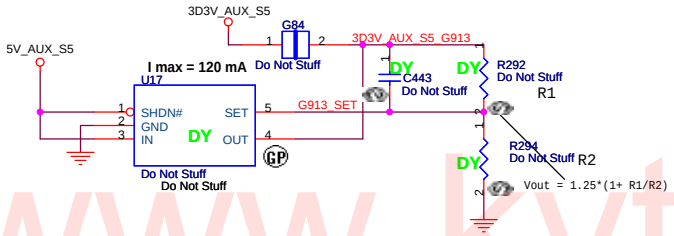
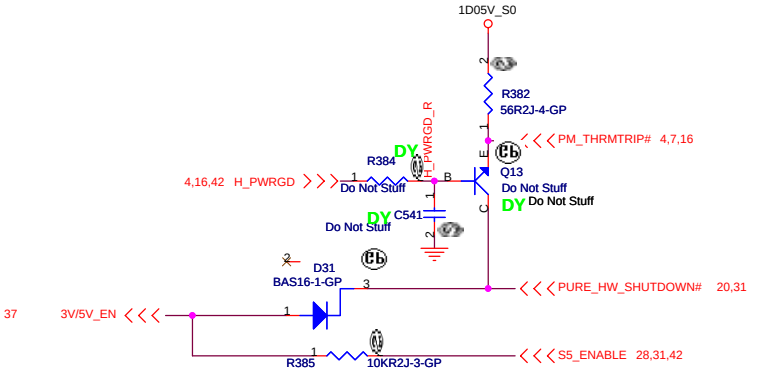
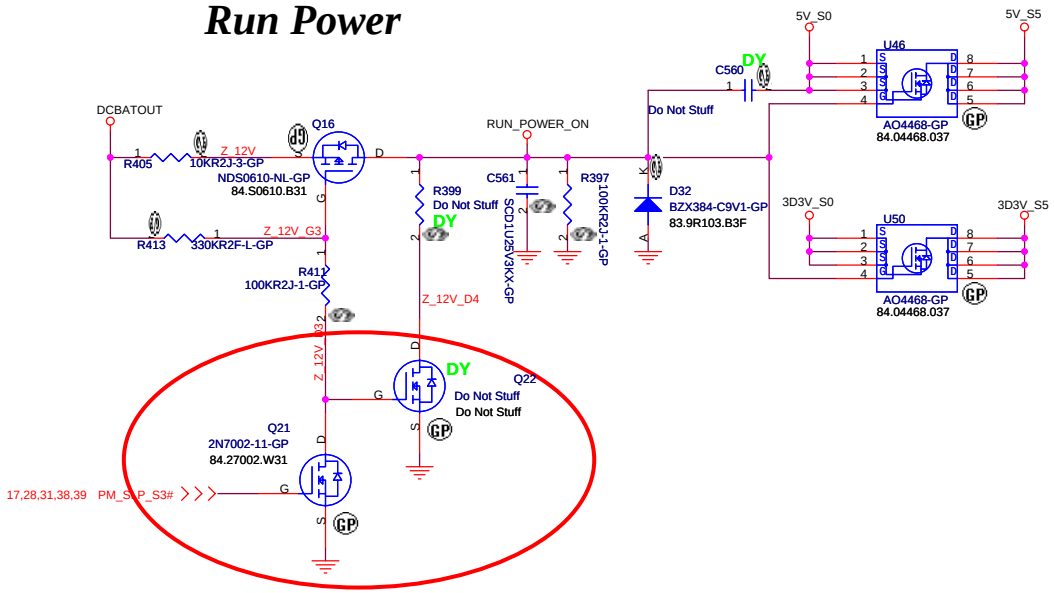
Aux Power 3D3V_AUX_S5

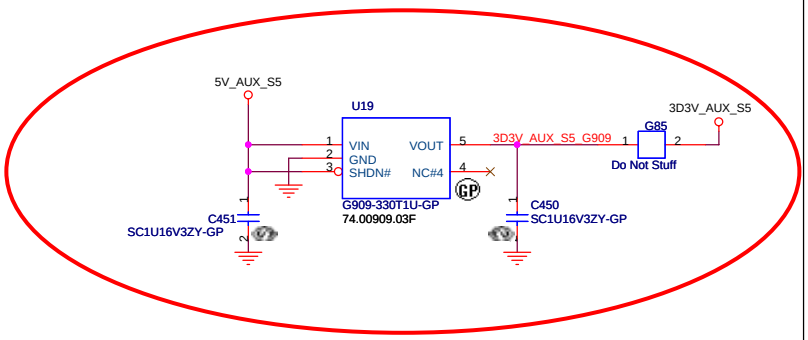




Run Power



Aux Power 3D3V_AUX_S5



SB modify

55.4H001.S03G

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RUN POWER and 3D3V_AUX_S5		
Size	Document Number: Biwa	Rev: -1
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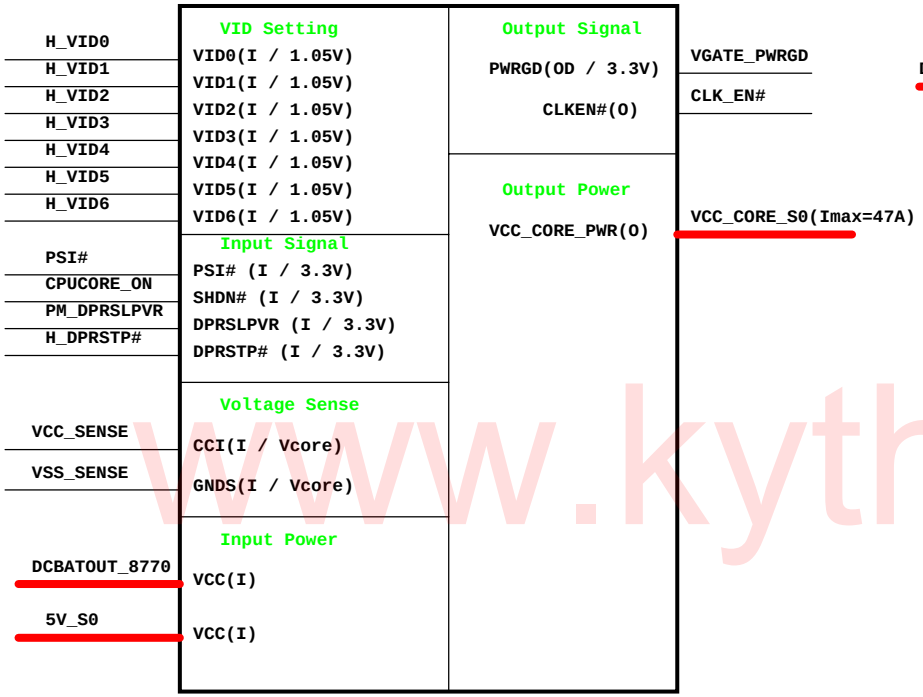
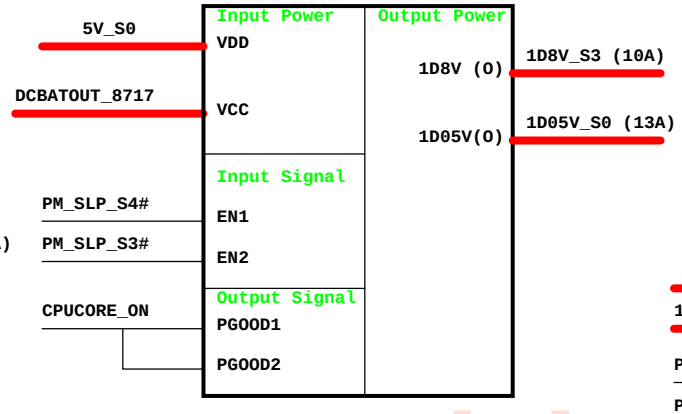
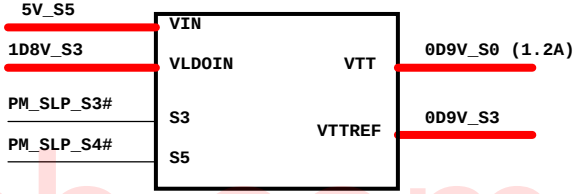
CPU_CORE
MAXIM MAX8770



MAX8717
1D8V/1D05V

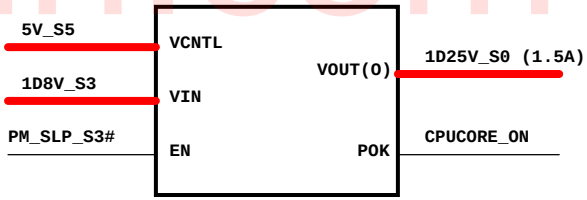


0D9V_S0



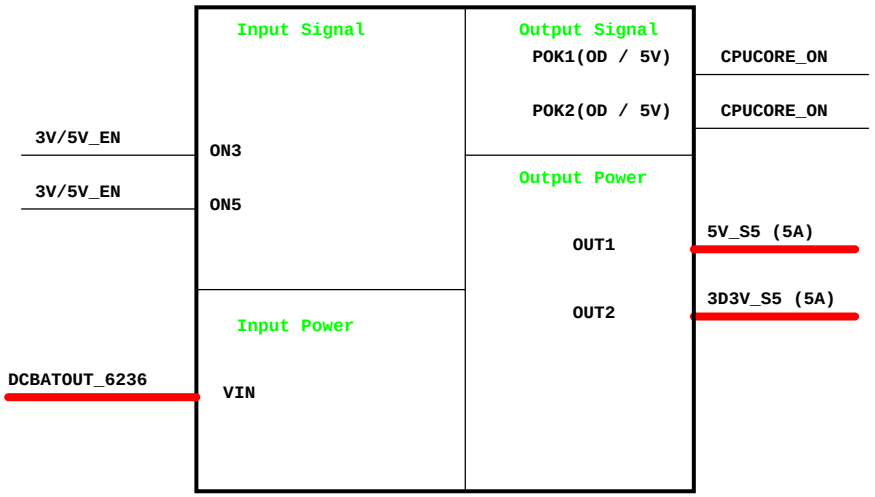
TPS51100

1D25V_S0

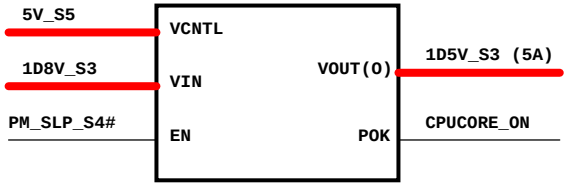


APL5915

ISL6236
5V/3D3V

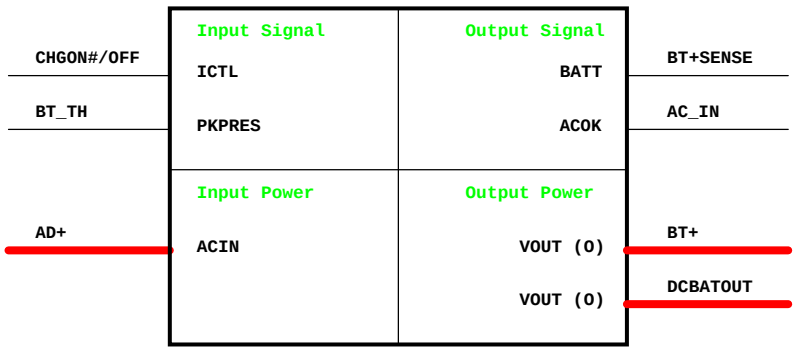


1D5V_S3



APL5912

Charger ISL6255



55.4H001.S03G

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

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A3	Biwa	SA

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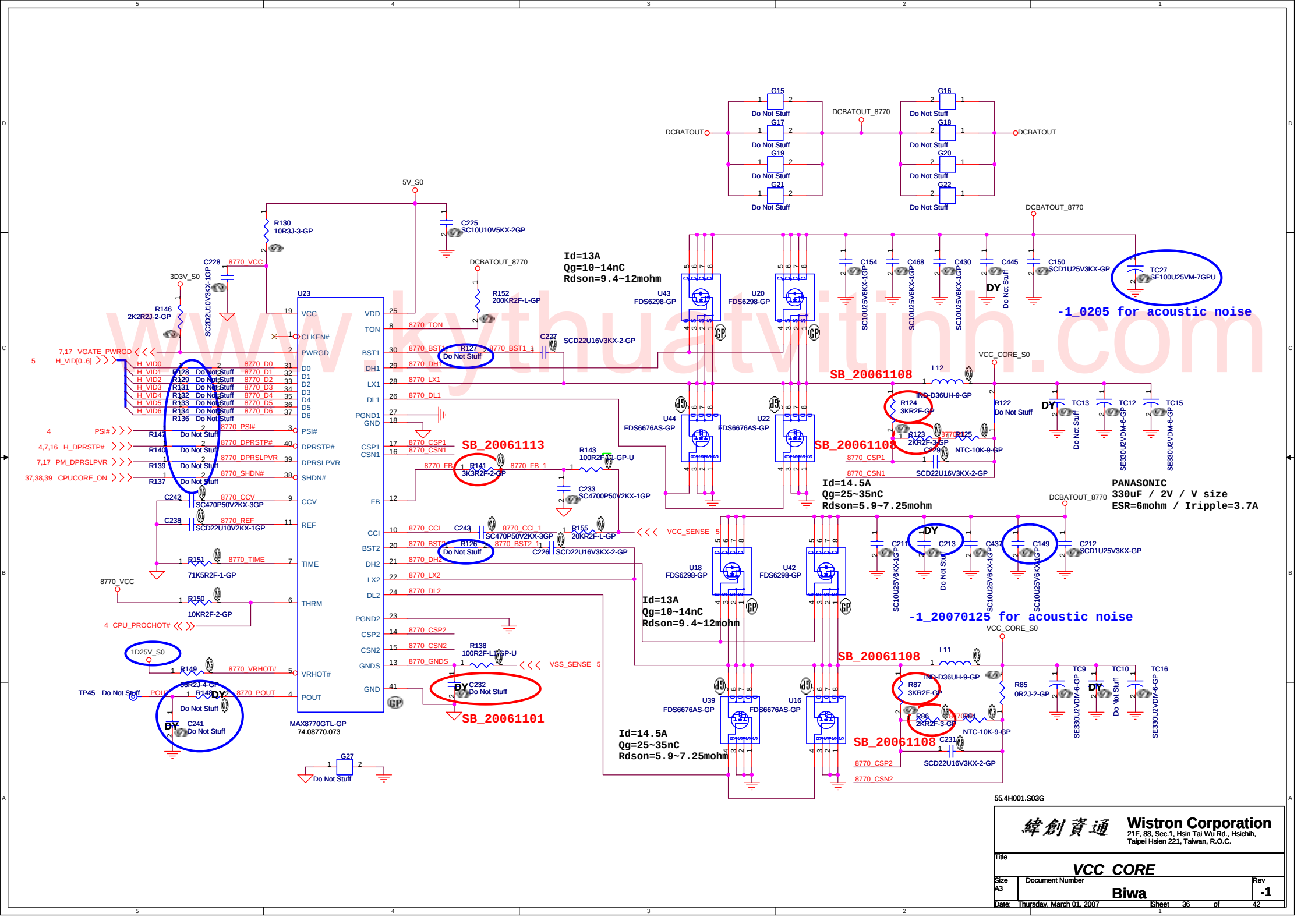

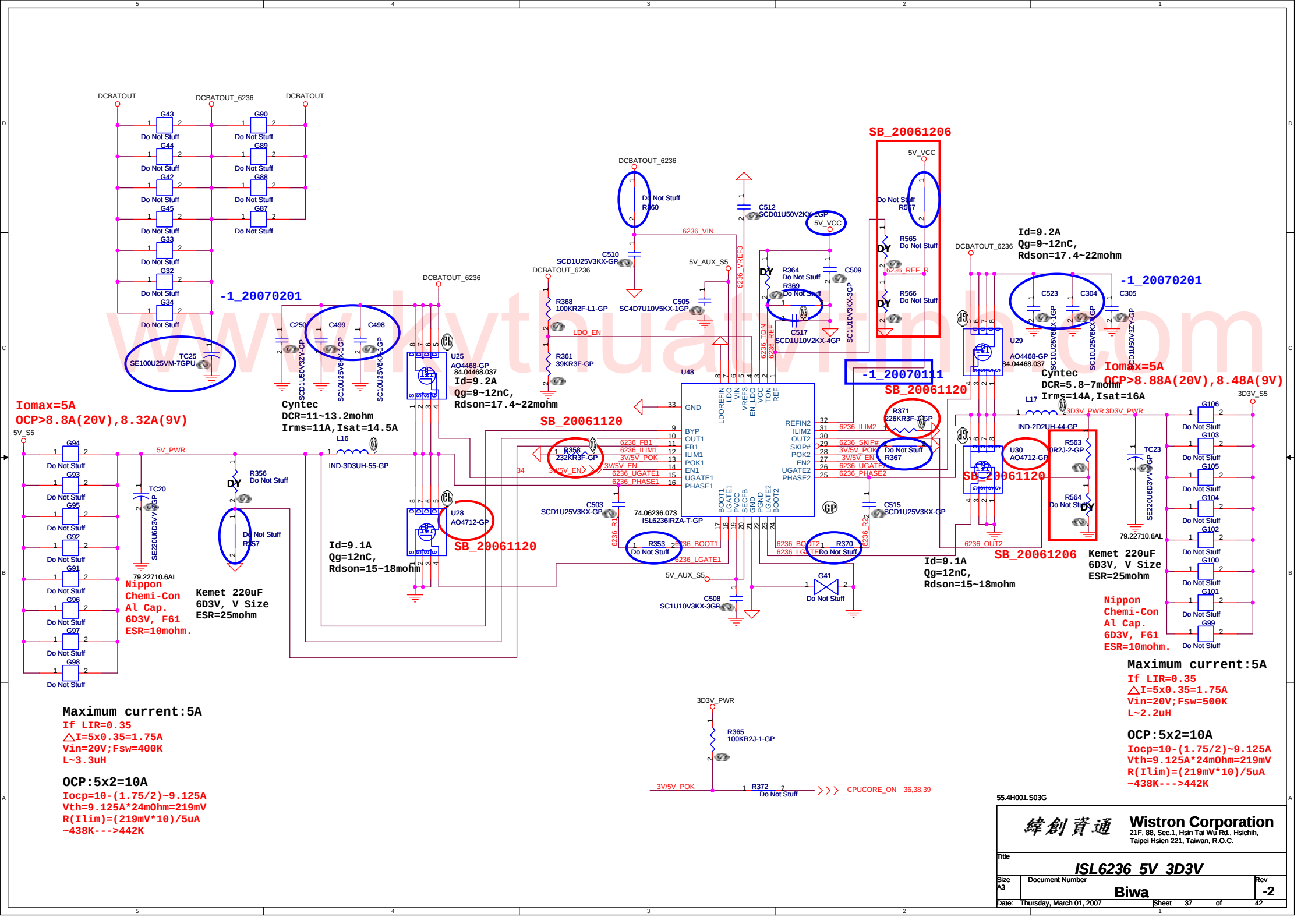
DCBATOUT
DCBATOUT_6236
G43
G44
G42
G45
G33
G32
G34
G90
G89
G88
G87
Do Not Stuff
-1_20070201
TC25
SE100U25VM-7GPU
C250
C499
C498
SCD1U50V3ZY-GP
SC10U25V6KX-1GP
U25
AO4468-GP
84.04468.037
Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm
Cyntec
DCR=11~13.2mohm
Irms=11A,Isat=14.5A
Iomax=5A
OCP>8.8A(20V),8.32A(9V)
SB_20061120
5V_S5
G94
G93
G95
G92
G91
G96
G97
G98
5V_PWR
TC20
SE220U6D3VM-GP
79.22710.6AL
Nippon
Chemi-Con
Al Cap.
6D3V, F61
ESR=10mohm.
R356
R357
L16
IND-3D3UH-55-GP
U28
AO4712-GP
Id=9.1A
Qg=12nC,
Rdson=15~18mohm
Kemet 220uF
6D3V, V Size
ESR=25mohm
Maximum current:5A
If LIR=0.35
△I=5x0.35=1.75A
Vin=20V;Fsw=400K
L~3.3uH
OCP:5x2=10A
Iocp=10-(1.75/2)~9.125A
Vth=9.125A*24mOhm=219mV
R(Ilim)=(219mV*10)/5uA
~438K--->442K
R360
C512
SCD01U50V2KX-1GP
5V_VCC
C510
SCD1U25V3KX-GP
6236_VIN
5V_AUX_S5
R368
100KR2F-L1-GP
LDO_EN
R361
39KR3F-GP
C505
SC4D7U10V5KX-1GP
R364
R369
C509
C517
SCD1U10V2KX-4GP
SC1U10V3KX-3GP
6236_VREF3
6236_TON
6236_REF
SB_20061206
R567
R565
R566
6236_REF_R
-1_20070111
SB_20061120
U48
GND
BYP
OUT1
FB1
ILIM1
POK1
EN1
UGATE1
PHASE1
LDOREFIN
LDO
VIN
VREF3
EN_LDO
VCC
TON
REF
REFIN2
ILIM2
OUT2
SKIP#
POK2
EN2
UGATE2
PHASE2
BOOT1
LGATE1
PVCC
SECFB
GND
PGND
LGATE2
BOOT2
74.06236.073
ISL6236IRZA-T-GP
R358
232KR3F-GP
6236_FB1
6236_ILIM1
3V/5V_POK
3V/5V_EN
6236_UGATE1
6236_PHASE1
C503
SCD1U25V3KX-GP
R353
6236_BOOT1
6236_LGATE1
R371
226KR3F-GP
R367
6236_ILIM2
6236_SKIP#
6236_UGATE2
6236_PHASE2
C515
6236_BOOT2
6236_LGATE2
R370
6236_OUT2
G41
C508
SC1U10V3KX-3GP
Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm
-1_20070201
C523
C304
C305
U29
AO4468-GP
84.04468.037
Cyntec
DCR=5.8~7mohm
Irms=14A,Isat=16A
Iomax=5A
OCP>8.88A(20V),8.48A(9V)
L17
IND-2D2UH-44-GP
3D3V_PWR
U30
AO4712-GP
R563
0R2J-2-GP
R564
TC23
SE220U6D3VM-GP
79.22710.6AL
Kemet 220uF
6D3V, V Size
ESR=25mohm
Nippon
Chemi-Con
Al Cap.
6D3V, F61
ESR=10mohm.
3D3V_S5
G106
G103
G105
G104
G102
G100
G101
G99
Id=9.1A
Qg=12nC,
Rdson=15~18mohm
Maximum current:5A
If LIR=0.35
△I=5x0.35=1.75A
Vin=20V;Fsw=500K
L~2.2uH
OCP:5x2=10A
Iocp=10-(1.75/2)~9.125A
Vth=9.125A*24mOhm=219mV
R(Ilim)=(219mV*10)/5uA
~438K--->442K
3D3V_PWR
R365
100KR2J-1-GP
3V/5V_POK
R372
CPUCORE_ON 36,38,39
55.4H001.S03G
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6236 5V 3D3V
Size
A3
Document Number
Biwa
Rev
-2
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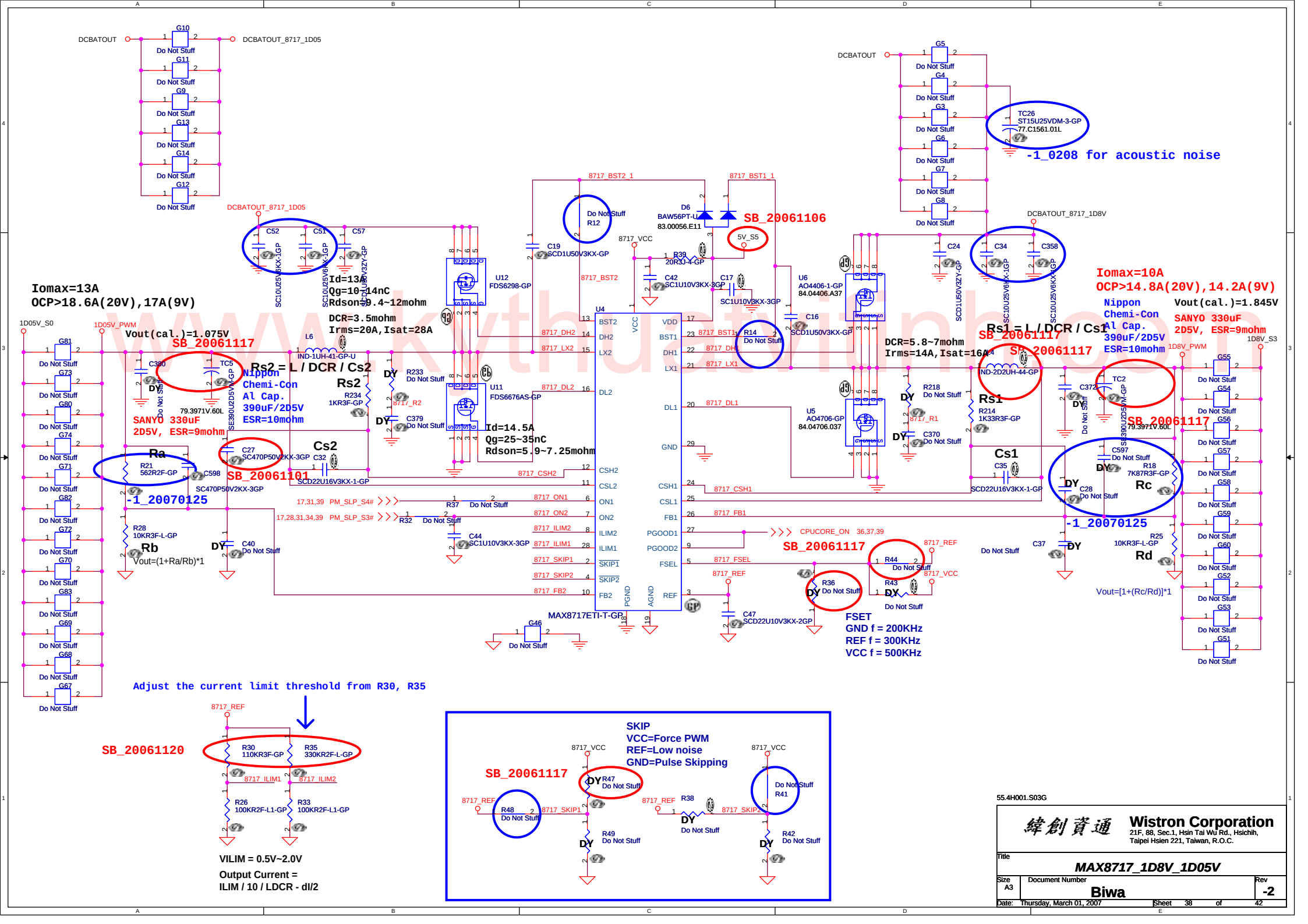
DCBATOUT
DCBATOUT_8717_1D05
DCBATOUT_8717_1D8V
Do Not Stuff
Iomax=13A
OCP>18.6A(20V),17A(9V)
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
DCR=3.5mohm
Irms=20A,Isat=28A
Vout(cal.)=1.075V
SB_20061117
Rs2 = L / DCR / Cs2
Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=10mohm
SANYO 330uF
2D5V, ESR=9mohm
Rs2
Cs2
Ra
Rb
Vout=(1+Ra/Rb)*1
SB_20061101
-1_20070125
SB_20061106
SB_20061120
Adjust the current limit threshold from R30, R35
VILIM = 0.5V~2.0V
Output Current =
ILIM / 10 / LDCR - dI/2
SKIP
VCC=Force PWM
REF=Low noise
GND=Pulse Skipping
SB_20061117
Iomax=10A
OCP>14.8A(20V),14.2A(9V)
Vout(cal.)=1.845V
DCR=5.8~7mohm
Irms=14A,Isat=16A
Rs1 = L / DCR / Cs1
Rs1
Cs1
Rc
Rd
Vout=[1+(Rc/Rd)]*1
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
FSET
GND f = 200KHz
REF f = 300KHz
VCC f = 500KHz
-1_0208 for acoustic noise
MAX8717ETI-T-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
MAX8717_1D8V_1D05V
Biwa
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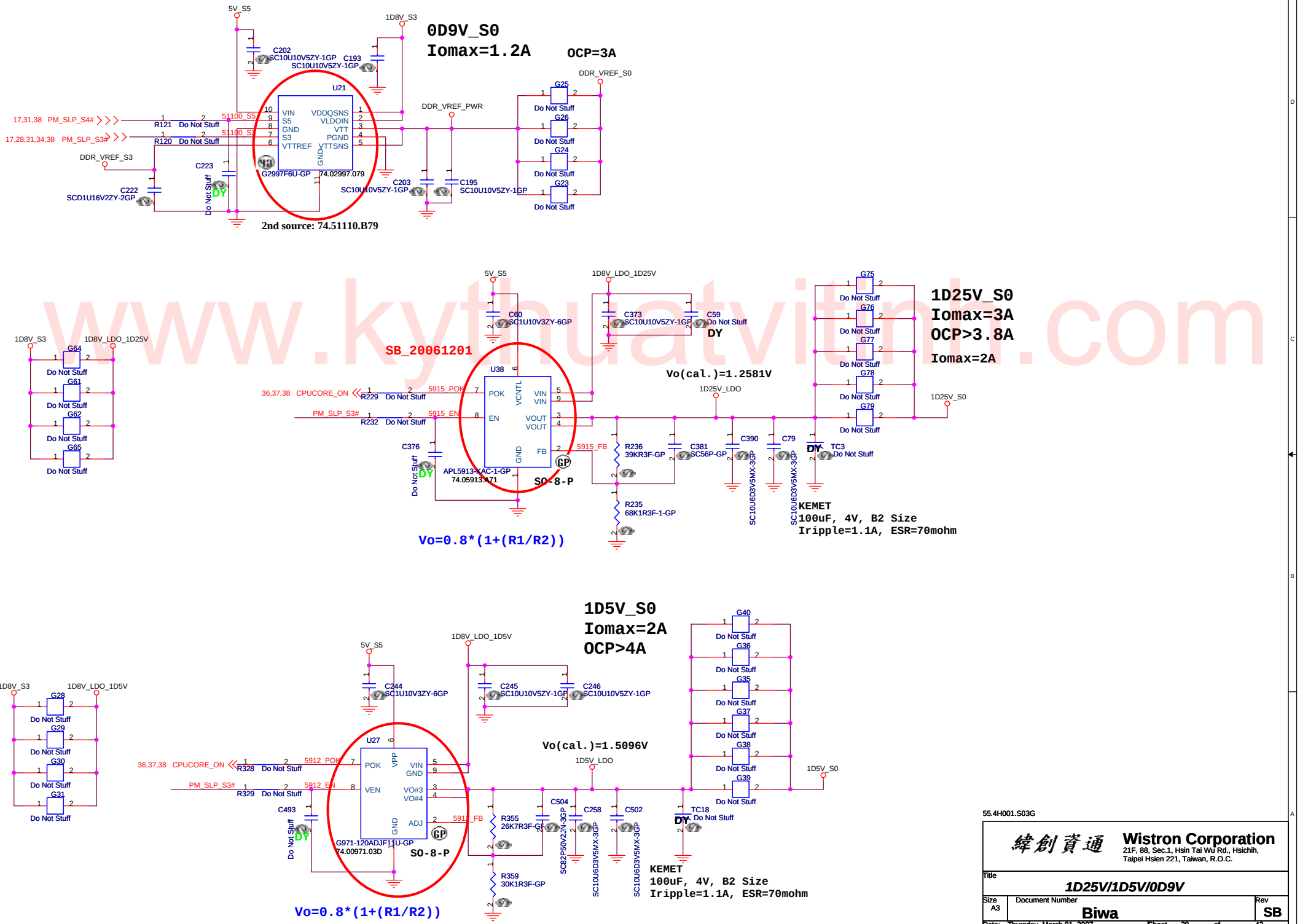

55.4H001.S03G

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D25V/1D5V/0D9V

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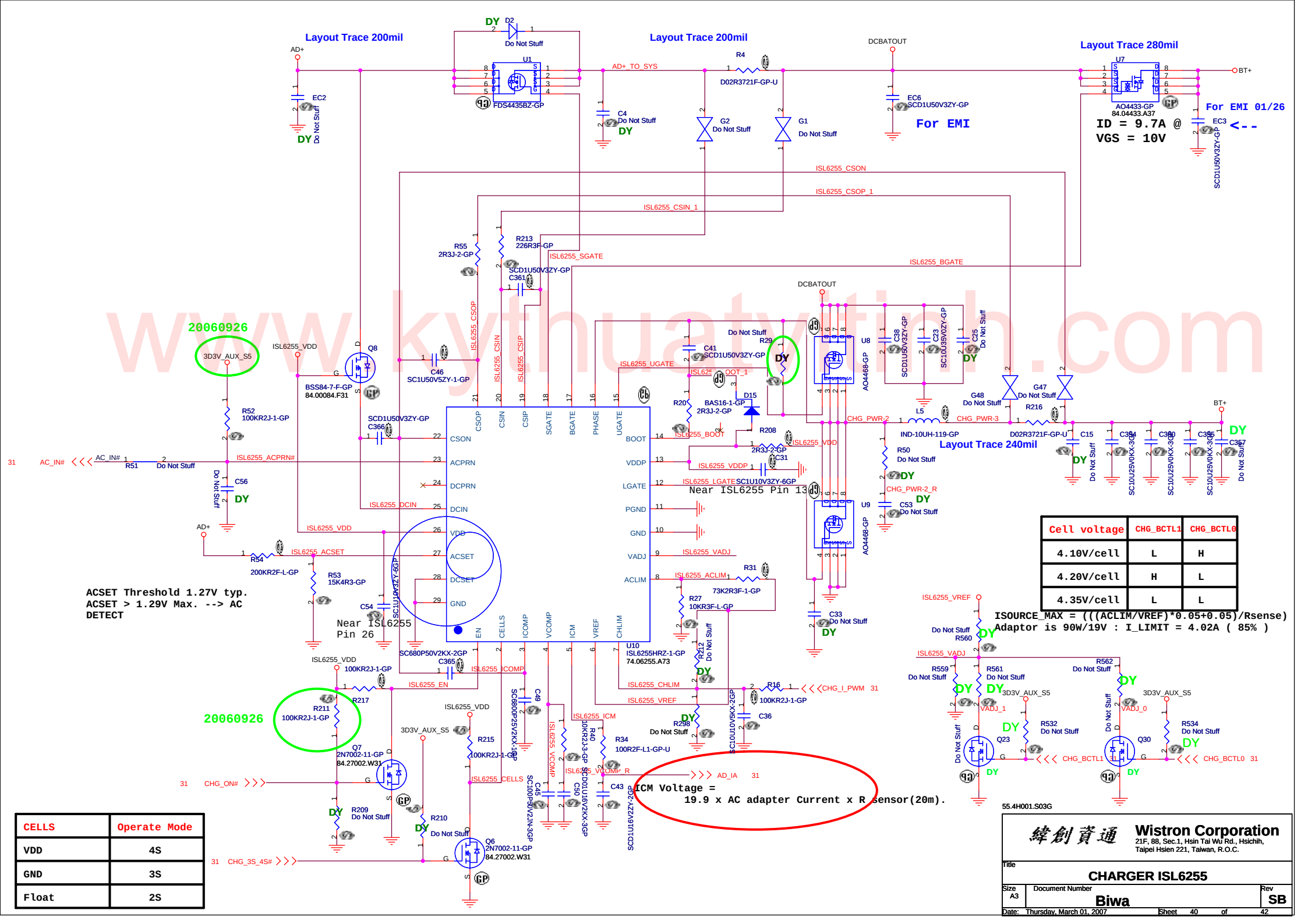

Cell voltage	CHG_BCTL1	CHG_BCTL0
4.10V/cell	L	H
4.20V/cell	H	L
4.35V/cell	L	L

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER ISL6255

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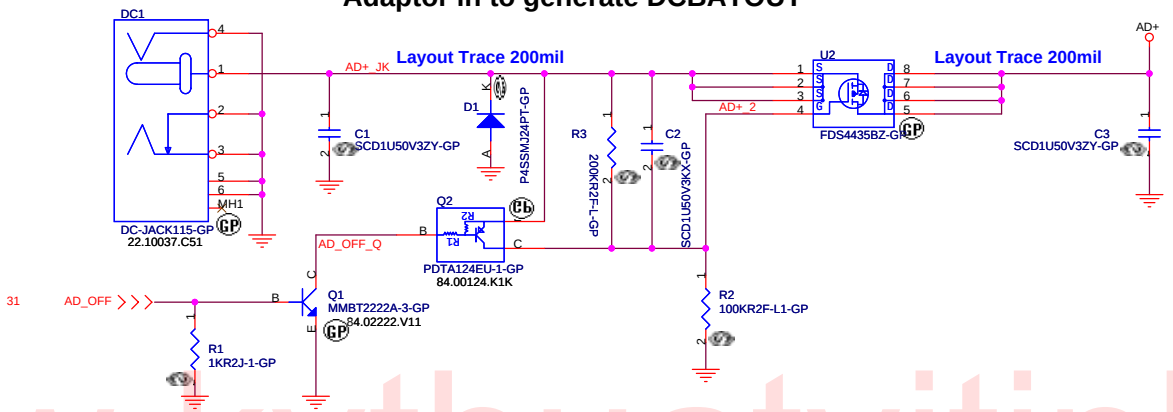
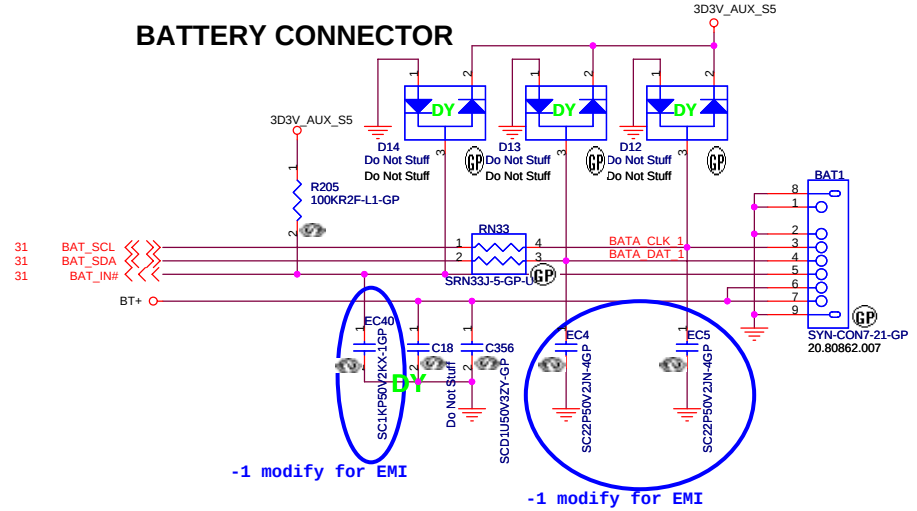
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

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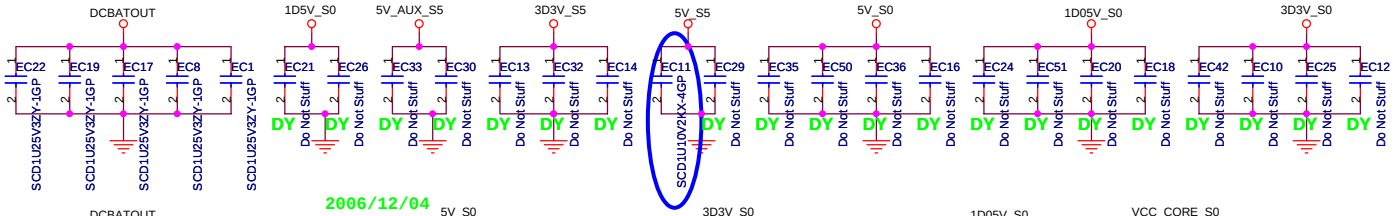
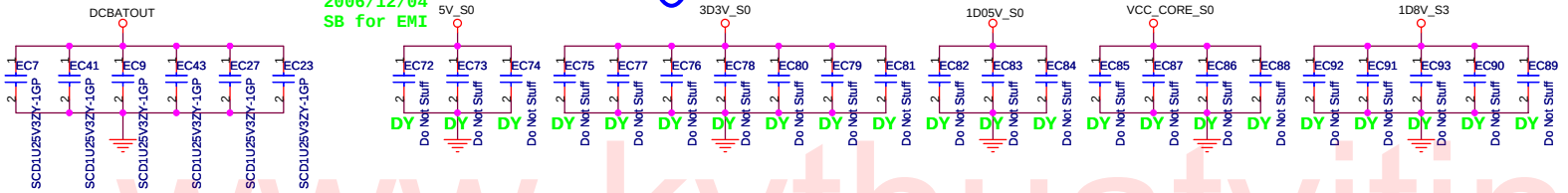
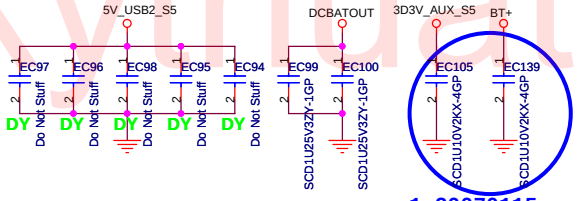
EMI Capacitor



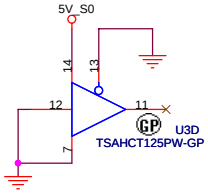
2006/12/04
SB for EMI



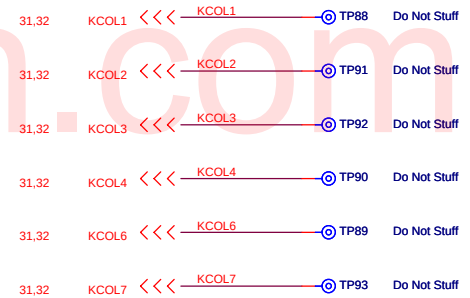


-1_20070115

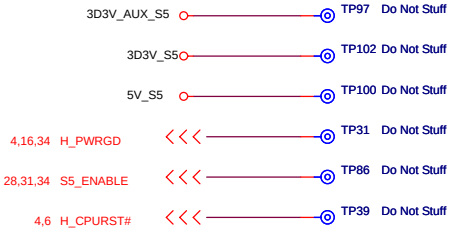
Unused gate



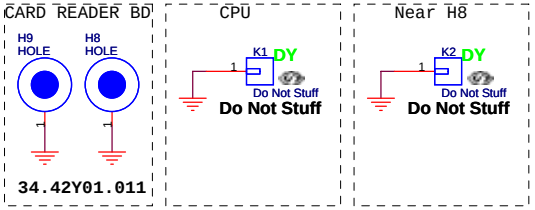
KBC JTAG Test Pad



DFX Test Point

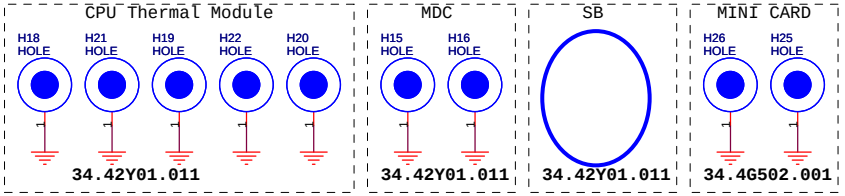


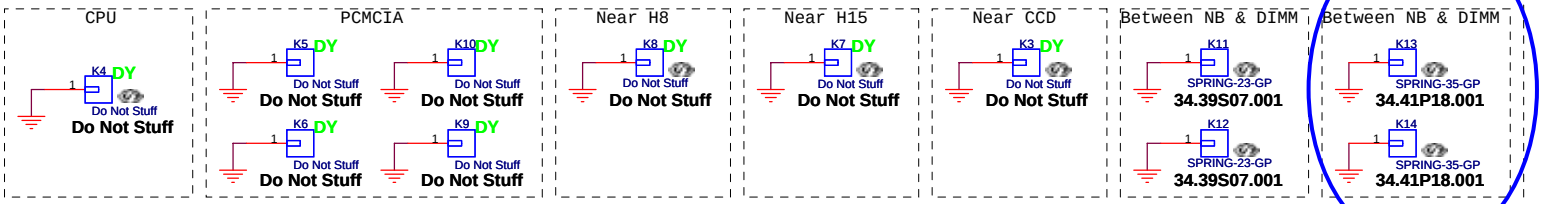
TOP



-1_0131 for thermal

BOTTOM





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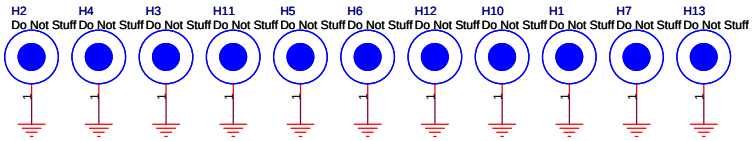

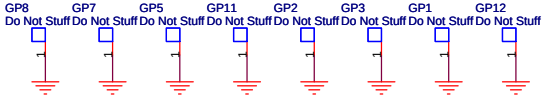

Test Point放在Dimm Door打開可量測處

55.4H001.S03G

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