TIA 1A

TELEVISION INTERFACE ADAPTOR (MODEL 1A)

GENERAL DESCRIPTION

The TIA1A is an MOS integrated circuit designed to interface between an eight (8) bit microprocessor and a television video modulator and to convert eight (8) bit parallel data into serial outputs for the color, luminosity, and composite sync required by a video modulator.

This circuit operates on a "line by line" basis, always outputing the same information every television line unless new data is written into it by the microprocessor.

A hardware sync counter produces horizontal sync timing independent of the microprocessor.

Vertical sync timing is supplied to this circuit by the microprocessor and combined into composite sync.

Horizontal position counters are used to trigger the serial output of five (5) horizontally moveable objects; two players, two missiles, and a ball. The microprocessor can add or subtract from these position counters to move these objects right or left.

The microprocessor determines all vertical position and motion by writing zeros or ones into object registers before each appropriate horizontal line.

Walls, clouds and other seldom moved objects are produced by a low resolution data register called the playfield register.

A fifteen (15) bit collision register detects all fifteen possible two object collisions between these six (6) objects (five moveable and one playfield). This collision register can be read and reset by the microprocessor. Six input ports are also provided on this chip that can be read by the microprocessor. These input ports and the collision register are the only chip addresses that can be read by the microprocessor. All other addresses are WRITE only.

Color luminosity registers are included that can be programmed by the microprocessor with eight (8) luminosity and fifteen (15) color values. A digital phase shifter is included on this chip to provide a single color output with fifteen (15) phase angles.

Two (2) independent audio generating circuits are included, each with programmable frequency, noise content, and volume control registers.

DETAIL DESCRIPTION

1. Data and addressing

Registers on this chip are addressed by the microprocessor as part of its overall RAM-ROM memory space. The attached table of read-write addresses summarizes the addressable functions. There are no registers that are both read and write. Some addresses however are both read and write, with write data going into one register and read data returning from a different register.
If the read-write line is low, the data bits indicated in this table will be written into the addressed write location when the Φ2 clock goes from high to low. Some registers are eight bits wide, some only one bit, an some (strobes) have no bits, performing only control functions (such as resets) when their address is written.
If the read-write line is high, the addressed location can be read by the microprocessor on data lines 6 and 7 while the Φ2 clock is high.
The addresses given in the table refer only to the six (6) real address lines. If any of the four (4) chip select lines are used for addressing, the addresses must be modified accordingly.

2. Syncronization

A. Horizontal Timing

A hardware counter on this chip produces all horizontal timing (such as sync, blank, burst) independent of the microprocessor, This counter is driven from an external 3.58 MHZ oscillator and has a total count of 228. Blank is decoded as 68 counts and sync and color burst as 16 counts.

B. Vertical Timing

There are one bit, addressable registers on this chip for vertical sync and vertical blank. The timing for these functions is established by the microprocessor by writing zero or one into these bits. (VSYNC, V BLANK)

C. Composite Sync

Horizontal sync and the output of the vertical sync bit are combined together to produce composite sync. This composite sync signal drives a chip output pad to an external composite video resistor network.

D. Microprocessor Synchronization

The 3.58 MHZ oscillator also clocks a divide by

three counter on this chip whose output (1.19 MHZ) is buffered to drive an output pad called $\phi 0$. This pad provides the input phase zero clock to the microprocessor which then produces the system $\phi 2$ clock (1.19 MHZ).

Software program loops require different lengths of time to run depending on branch decisions made within the program. Additional synchronization (Shown in Figure 2) is, therefore, required between the software and hardware. This is done with a one bit latch called WSYNC (wait for sync). When the microprocessor finishes a routine such as loading registers for a horizontal line, or computing new vertical locations during vertical blank, it can address WSYNC, setting this latch high. When this latch is high, it drives an output pad to zero connected to the microprocessor ready line (RDY). A zero on this line causes the microprocessor to halt and wait.As shown in figure 2,WSYNC latch is automatically reset to zero by the leading edge of the next horizontal blank timing signal, releasing the RDY line, allowing the microprocessor to begin its computation and register writing for this horizontal television line or line pair.

3. Playfield graphics Register

A. Description

Objects,(such as walls, clouds, and score) which are not required to move, are written into a 20 bit register called the playfield register. This register (Figure 5) is loaded from the data bus by three separate write addresses (PF0, PF1, PF2). Playfield may be loaded at any time. To clear the playfield, zeros must be written into all three addresses.

B. Normal Serial Output

The playfield register is automatically scanned (and converted to serial output) by a bi-directional shift register clocked at a rate which spreads the twenty (20) bits out over the left half of a horizontal line. This scanning is initiated by the end of horizontal blank (left edge of television screen). Normally the same scan is then repeated, duplicating the same twenty (20) bit sequence over the right half of the horizontal line.

C. Reflected Serial Output

A relected playfield may be requested by writing

a one into bit zero of the playfield control register (CTRLPF). When this bit is true the scanning shift register will scan the opposite direction during the right half of the horizontal line, reversing the twenty (20) bit sequence.

D. Timing Constraints

Even though the playfield bytes (PF0, PF1, PF2) may be written at any time, if one of them is changed while being serially scanned, part of the new value may both show up on the television horizontal line.

4. Horizontal Position Counters

A. Description

The playfield is a "fixed" graphics register, always starting its serial output when triggered by the beginning of each television line. This chip also includes five "moveable" graphics registers, whose serial outputs are triggered by five separate horizontal position counters every time these counters pass through zero count. These position counters are clocked continuously during the unblanke portion of every horizontal line and their count length is exactly equal to the normal number of clocks supplied to them during this time. They will therefore pass through zero at the same time during each horizontal television line and the triggered outputs will have no horizontal motion. A typical horizontal counter is shown in figure 4.
If extra clocks are supplied to these counters (or normal clocks suppressed) the zero crossing time will shift and the object will have moved left (extra clocks) or right (fewer Clocks). Some position counters have extra decodes (in addition to a zero decode) to trigger multiple copies of the same object across a horizontal line.
All position counters can be reset to zero count by the microprocessor at any time, by a write instruction to the reset addresses (RESBL, RESM0, RESM1, RESP0, RESP1). If reset occurs during horizontal blank, the object will appear at the left side of the television screen. Properly timed resets may position an object. at any horizontal location consistent with the microprocessor cycle time.

B. Ball Position Counter

The ball position counter has only the zero

crossing decode and therefore cannot trigger multiple copies of the ball graphics.

C. Player Position Counters

Each player position counter has three decodes in addition to the zero crossing decode. These decodes are controlled by bits 0,1,2 of the number size control registers (NUSIZ0, NUSIZ1), and trigger 1,2, or 3 copies of the player (at various spacings) across a horizontal line as shown on page 20. These same control bits are used for the decodes on the missile position counter, insuring an equal number of players and missiles.

D. Missile Position Counters

Missile position counters are identical to player positon counters except that they have another type of reset in addition to the previously discussed horizontal position reset. These extra reset addresses (RESMP0, RESMP1) write data bit 1 into a one bit register whose output is used to position the missile (horizontally) directly on top of its corresponding player, and to disable the missile serial output.

5. Horizontal Motion Registers

A. General Description

There are five write only registers on this chip that contain the horizontal motion values for each of the five moving objects. A typical horizontal motion register is shown in figure 4. The data bus (bits4 through7) is written into these addresses (HMP0, HMP1, HMM0, HMM1, HMBL) to load these registers with motion values. These registers supply extra (or fewer) clocks to the horizontal position counters only when commanded to do so by an HMOVE address from the microprocessor. These registers may all be cleared to zero (no motion) simultaneously by an HMCLR command from the microprocessor, or individually by loading zeros into each register. These registers are each four bits in length and may be loaded with positive (left motion), negative (right motion) or zero (no motion) values. Negative values are represented in twos complement format.

D. Timing Constraints

These registers may be loaded or cleared at almost any time. The motion values they contain will be used only when an RMOVE command is addressed, and then all five motion values will be used simultaneously into all five horizontal position counters once. The only timing constraint on this operation involves the RMOVE command. The RMOVE command must be located in the microprocessor program immediately after a wait for sync (WSYNC) command. This insures that the RMOVE operation begins at the leading edge of horizontal blank, and has the full blank time to supply extra or fewer clocks to the horizontal position counters. These registers should not be modified for at least 24 Computer cycles after the RMove command.

6. Moving Object Graphics Registers

A. General Description

There are five graphics registers for moving objects on this chip. These graphics registers are loaded (written) in parallel by the microprocessor and like the playfield register are scanned and converted to serial output. Unlike the playfield register, which is always scanned beginning at the left side of each horizontal line, moving object graphics registers are scanned only when triggered by a start decode from their horizontal position counter. A typical graphics register is shown in figure 4

B. Missile Graphics

The graphics registers for both missiles are identical and very simple. They each consist of a one bit register called missile enable (ENAM0, ENAM1). This graphics bit is scanned (outputed) only when triggered by its corresponding position counter. There are control bits (bits 4,5, of NUSIZ0, NUSIZ1) that can stretch this single graphics bit out over widths of 1, 2, 4, or 8 clocks of horizontal line time. (A full line is 160 clocks).

C. Player Graphics

The graphics registers for both players are identical and are rather complex. They each consist of eight bit parallel registers (GRP0, GRP1) and a bi-directional parallel to serial

scan counter that converts the parallel data into serial output.
A one bit control register (REFP0, REFP1) determines the direction (reflection) of the parallel to serial scan, outputing either D7 through D0, or D0 through D7. This allows reflection (horizontal flipping) of player serial graphics data without having to flip the microprocessor data.
The clock into the scan counter can be controlled (three bits of NUSIZ0 and NUSIZ1) to slow the scan rate and stretch the eight bits of serial graphics out over widths of 8, 16, or 32 clocks of horizontal line time. These same control bits are used in the player-missile motion counters to control multiple copies, so only three player widths (scan rates) are available.

D. Vertical Delay.

Each of the player graphics registers actually consists of two 8 bit parallel registers. The first (GRP0, GRP1) is loaded (written) from the microprocessor 8 bit data bus. The second is automatically loaded from the output of the first. The reason for this is a complex subject called vertical delay.
A large amount of microprocessor time is required to generate player, missile and playfield graphics (table look up, masking, comparisons,-ect.) and load these into this chip's registers. For most game programs this time is just too large to fit into one horizontal line time. In fact for most games it will barely fit into two line times (127 microseconds). Therefore, individual graphics registers are loaded (written) every two lines, and used twice for serial output between loads.
This type of programming will obviously limit the vertical height resolution of objects to multiples of two lines. It also will limit the resolution of vertical motion to two lines jumps.
Nothing can be done about the vertical height resolution; however, vertical motion can be resolved to a single line by addition of a second graphics register that is automatically parallel loaded from the output of the first, one line time after the first was loaded from the data bus. This second graphics register output is therefore always delayed vertically by one line. A control bit called

vertical delay (VDEL0, VDEL1) selects which of these two registers is to be used for serial output. If this control bit is set by the microprocessor between picture frames the object will be moved down (delayed) by one line during the next frame.
In most programming applications player 0 graphics and player 1 graphics are loaded (written) alternately, during the blank time just prior to each line as shown in (figure 1). Since GRP0 and GRP1 addresses from the microprocessor alternate, they are delayed by one line from each other. The GRP0 address decode can therefore be used to load the delayed graphics register for player 1, and GRP1 likewise to load the delayed graphics register for player 0. The two vertical delay bits (VDEL0, VDEL1) then select delayed or undelayed registers for player 0 and player 1 as serial outputs.

E. Ball Graphics

The ball graphics register is almost identical to the missile graphics register. It also consists of a single enable bit (ENABL) whose output is triggered by the ball position counter. It also has two control bits (bits 4, 5 of CTRLPF) that can stretch this single graphics bit out over widths of 1, 2, 4, or 8 clocks of horizontal line time.
Unlike the missile graphics, however, the ball graphics register has capability for vertical delay similar to the player graphics. A second graphics (enable) bit is alternately loaded from the output of the first, one line after the first was loaded from the data bus. A ball vertical delay bit (VDELBL) selects which of these two graphics bits is used for the ball serial output. The first graphics bit (ENABL) should be loaded during the same horizontal blank time as player 0 (GRP0), because GRP1 is used to load the second enable bit from the output of the first on alternate lines.

7. Collision Detection Latches

A. Definitions

The serial outputs from all the graphics registers represent real time horizontal location of objects on the television screen. If any of these outputs occur at the same time,

they will overlap (collide) on the screen. There are six objects generated on this chip (five moving and playfield allowing fifteen possible two object collisions. These overlaps (collisions) are detected by fifteen "and" gates whenever they occur, and are stored in fifteen individual latch register bits, as shown in figure 6.

B. Reading Collisions

The microprocessor can read these fifteen collision bits on data lines 6 and 7 by addressing them two at a time. This could be done at any time but is usually done between frames (during vertical blank) after all possible collisions have serially occured.

C. Reset

All collision bits are reset simultaneously by the microprocessor using the reset address CXCLR. This is usually done near the end of vertical blank, after collisions have been tested.

8. Input ports

A. General Description

There are 6 input ports on this chip whose logic state may be read on data line 7 with read addresses INPT0 through INPT5. These 6 ports are divided into two types, "dumped" and "latched". See figure 8.

B. Dumped Input Ports (I0 through I3)

These 4 input ports are normally used to read paddle position from an external potentiometer-capacitor circuit. In order to discharge these capacitors each of these input ports has a large transistor, which may be turned on grounding the input ports) by writing into bit 7 of the register VBLANK. When this control bit is cleared the potentimeters begin to recharge the capacitors and the microprocessor measures the time required to detect a logic 1 at each input port.

As long as bit 7 of register VBLANK is zero, these four ports are general purpose high inpedance input ports. When this bit is a 1 these ports are grounded.

C. Latched Input ports (I4, I5)

These two input ports have latches which can be enabled or disabled by writing into bit 6 of register VBLANK.

When disabled, these latches are removed from the circuit completly and these ports become two general purpose input ports, whose present logic state can be read directly by the microprocessor.

When enabled, these latches will store negative zero logic level) signals appearing on these two input ports, and the input port addresses will read the latches instead of the input ports.

Latched Input Ports (I4, I5) - continued
When first enabled these latches will remain positive as long as the input ports remain positive (logic one). A zero input port signal will clear a latch value to zero, where it will remain (even after the port returns positive) until disabled. Both latches may be simultaneously disabled by writing a zero into bit 6 of register VBLANK.

6.5 Priority Encoder

A. Purpose

As discussed in the section on collisions, simultaneous serial outputs from the graphics registers represent overlap on the television screen. In order to have color-luminosity values assigned to individual objects it is necessary to establish priorities between objects when overlapped. The priority encoder is shown in figure 3.

B. Priority Assignment

The lack of any objects results in a color-lum value called the background. The background (BK) has lowest priority and only appears when no objects are outputing. In order to simplify the logic each missile is given the same color-lum value and priority as it's corresponding player (P0, M0) and the ball is given the same color-lum value and priority as the playfield (PF, BL).
The following table illustrates the normal priority assignment:

Highest Priority	P0, M0
Second Highest	P1, M1
Third Highest	PF, BL
Lowest Priority	BK

Objects with higher priority will appear to move in front of objects with lower priority. Players will therefore move in front of playfield (clouds, walls, etc.).

C. Priority Control

There are two playfield control bits that affect priority, one called playfield priority(PFP) (bit 2 of CTRLPF) and one called score (bit 1 of CTRLPF). When a one is written into the PFP bit the priority assignment is modified as shown below.

Highest Priority	PF, BL
Second Highest	P0, M0
Third Highest	P1, M1
Lowest Priority	BK

Players will then move behind playfield (clouds, wall, etc.).
When a one is written into the score control bit, the playfield is forced to take the color-lum of player 0 in the left half of the screen and player 1 in the right half of the screen. This is used when displaying score and identifies the score with the correct player.
The priority enco der produces 4 register select lines (shown in figure 3) that are mutually exclusive. These 4 lines select either background, player 0, player 1 or playfield, and only one of them can be true at a time.

9. Color Luminance Registers

A. Description

There are four registers (shown in figure 3) that contain color-lum codes. Four bits of color code and three bits of luminance code may be written into each of these registers (COLUP0, COLUP1, COLUPF, COLUBK) by the microprocessor at any time. These codes (representing 16 color values and 8 luminance values) are given in the Detailed Address List.

B. Multiplexing

The serial graphics output from all six objects is examined by the priority encoder which activates one of the four select lines into a 4 X 7 multiplexer. This multiplexer (shown in figure 3) then selects one of the four color-lum registers as a 7 line output. Three of these lines are binary coded luminosity and go directly to chip output pads. The other four lines go to the color phase shifter.

10. Color Phase Shifter

This portion of the chip (shown in figure 3) produces a reference color output (color burst) during horizontal blank and then during the unblanked portion of the line it produces a color output shifted in phase with respect to the color burst.. The The amount of phase shift determines the color and is selected by the four color code lines from the Color-lum multiplexer. Binary code 0 selects no color. Code 1 selects gold (same phase as color burst). Codes 2 (0010) through 15 (1111) shift the phase from zero through almost 360 degrees allowing selection of 15 total colors around the television color wheel.

11. Audio Circuits

Two audio circuits are incorporated on this chip. They are identical and completely independent, although their outputs could be combined externally into one speaker. Each audio circuit consists of parts described below, and in figure 7.

A. Frequency Select

Clock pulses (at approximately 30 KHZ) from the horizontal sync counter pass through a "divide by N" circuit which is controlled by the output code from a five bit frequency register (AUDF). This register can be loaded (written) by the microprocessor at any time, and causes the 30 KHZ clocks to be divided by 1 (code 00000) through 32 (code 11111). This produces pulses that are digitally adjustable from approximately 30 KHZ to 1 KHZ and are used to clock the noise-tone generator.

B. Noise-Tone Generator

This circuit contains a nine bit shift counter which may be controlled by the ouput code from a four bit audio control register (AUDC), and is clocked by the frequency select circuit. The control register can be loaded by the microprocessor at any time, and selects different shift counter feedback taps and count lengths to produce a variety of noise and tone qualities.

C. Volume Select

The shift counter ouput is used to drive the audio output pad through four driver transistors that are graduated in size. Each transistor is twice as large as the previous one and is enabled by one bit from the audio volume register (AUDV). This audio volume register may be loaded by the microprocessor at any time. As binary codes 0 through 15 are loaded, the pad drive transistors are enabled in a binary sequence. The shift counter output therefore can pull down on the audio ouput pad with 16 selectable impedance levels.

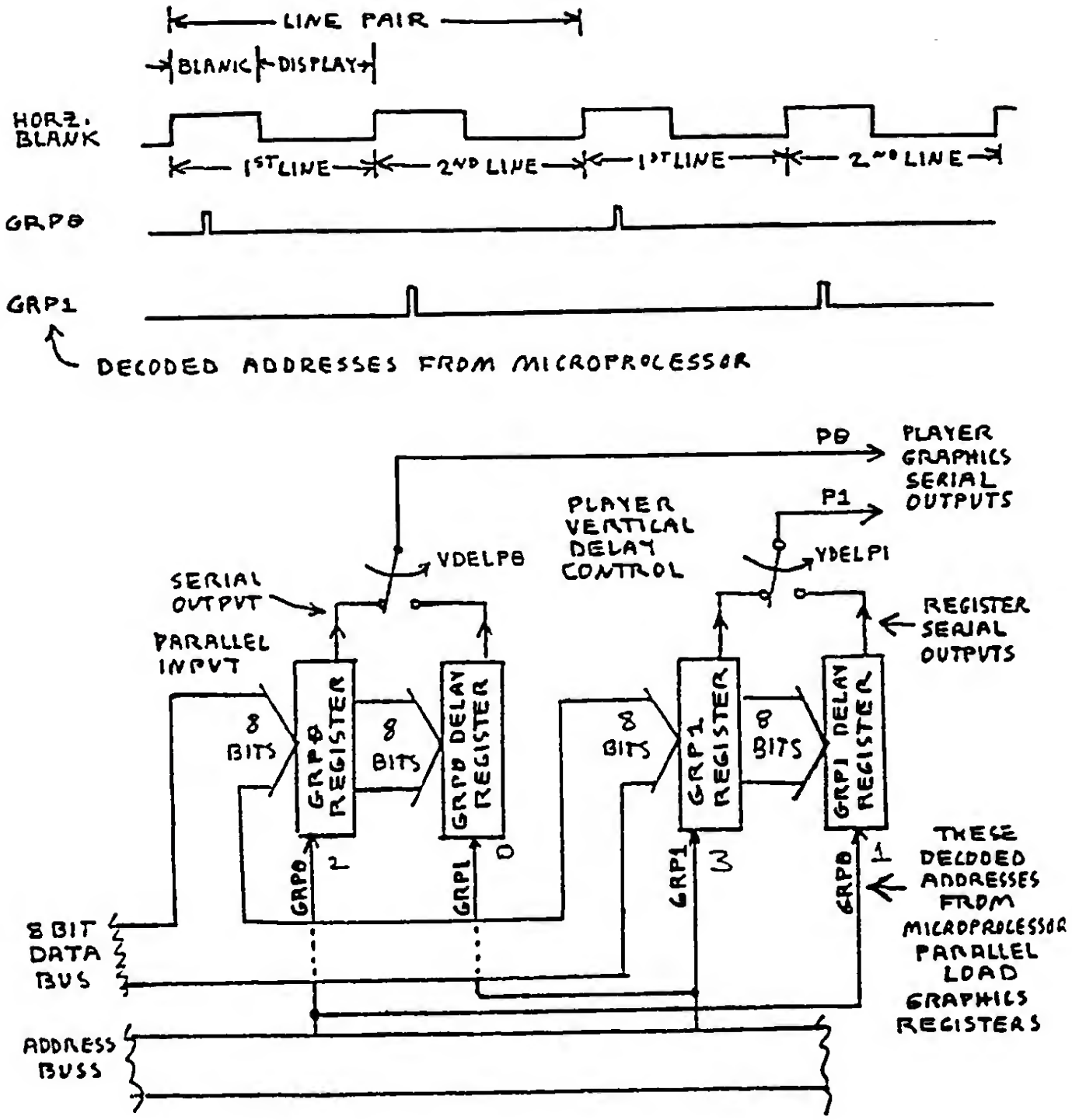


FIGURE 1. VERTICAL DELAY

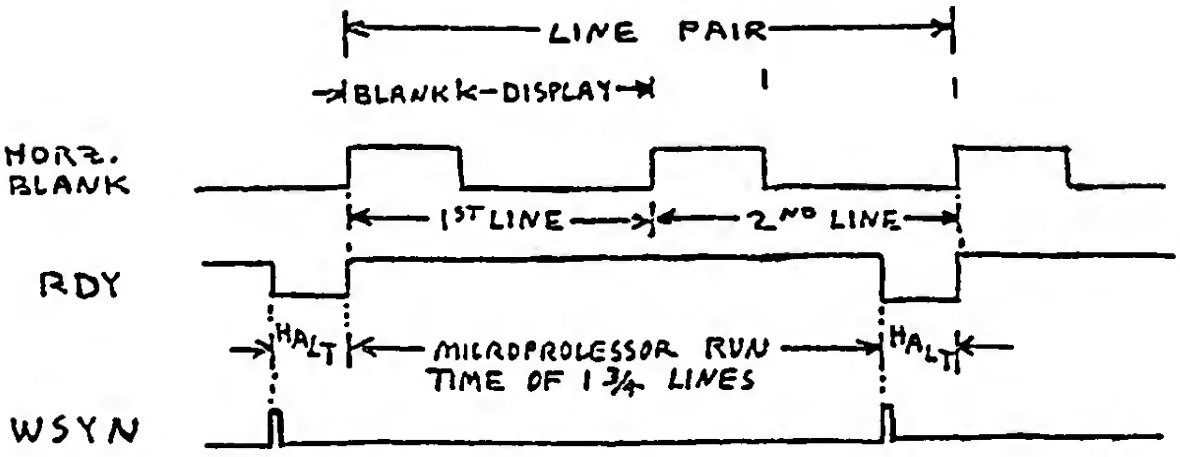


FIG. 2 SYNCRONIZATION

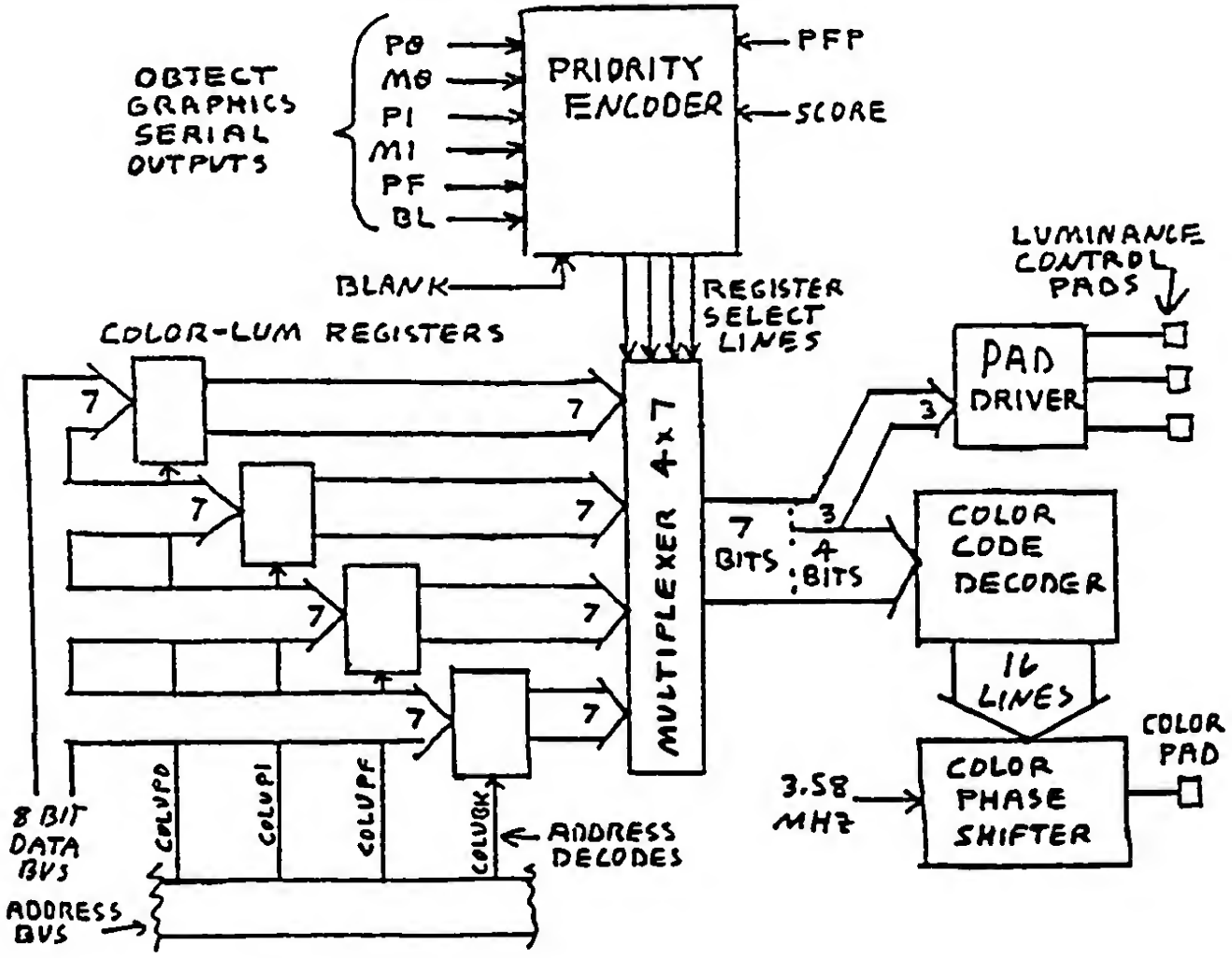
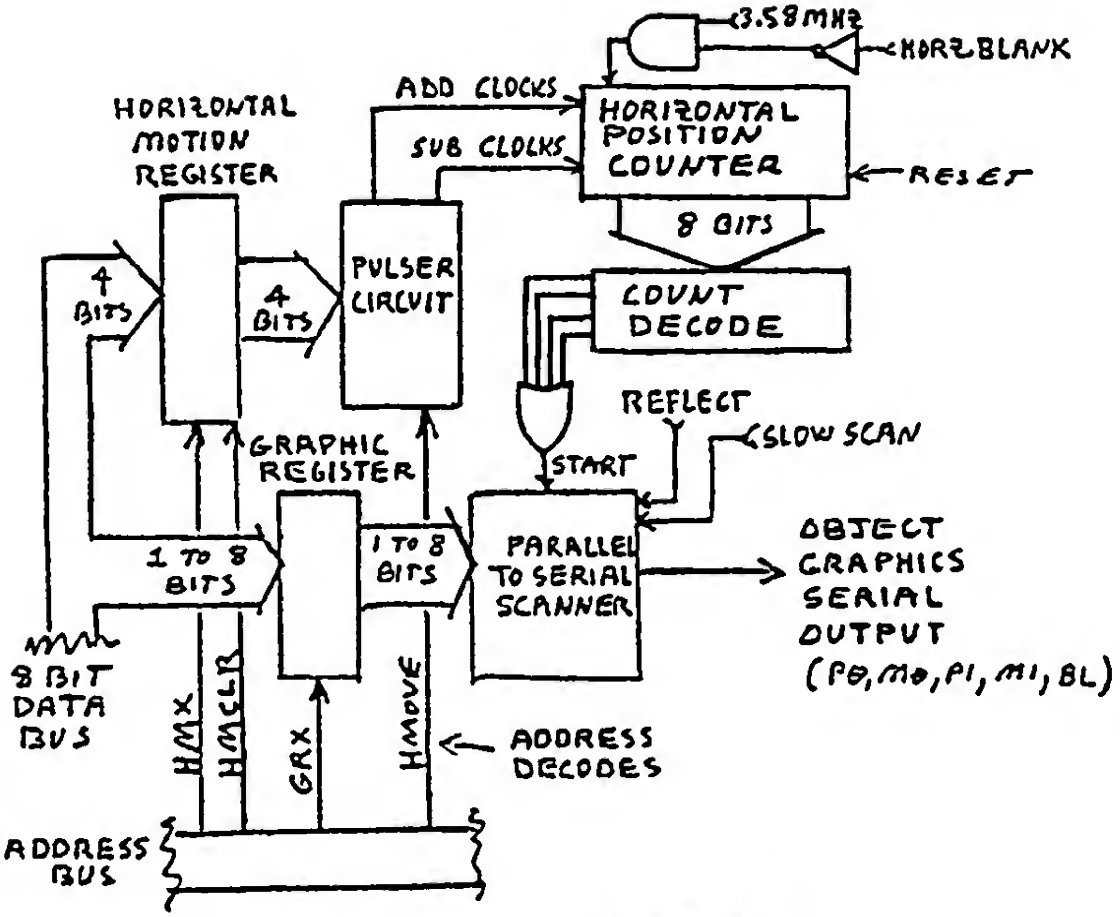


FIGURE 3. COLOR-LUMINANCE



TYPICAL

FIGURE 4. HORIZONTAL MOTION CIRCUIT

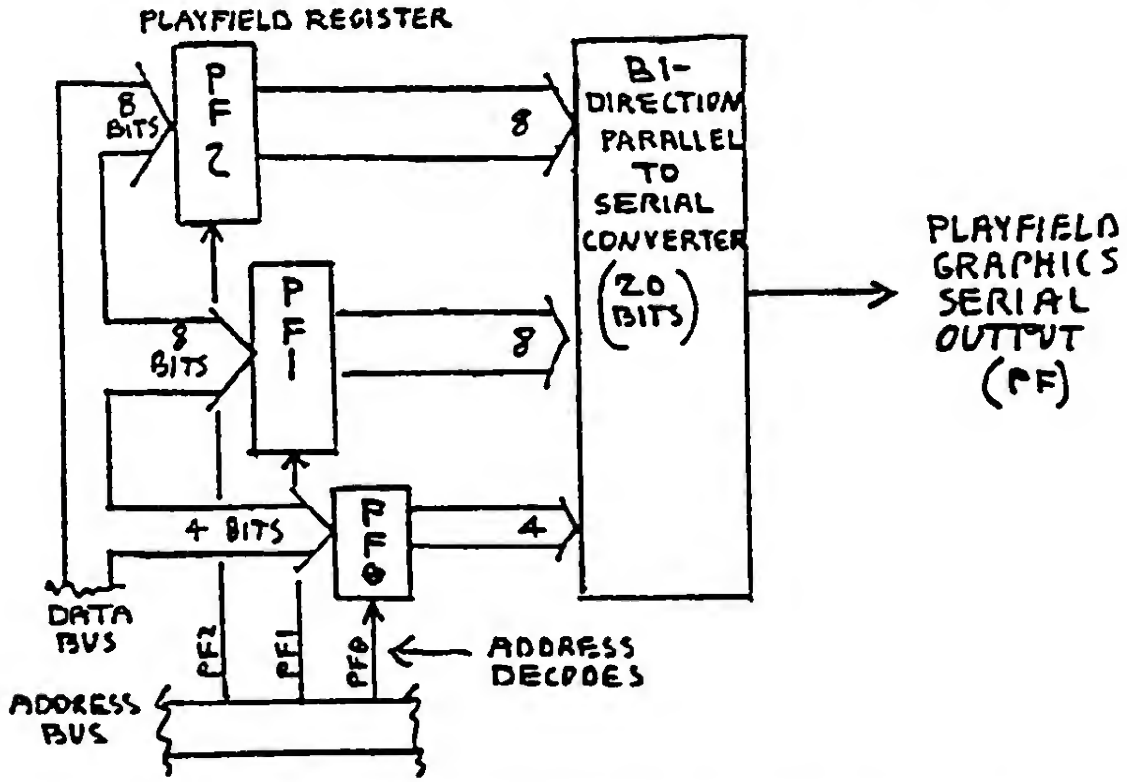


FIGURE 5. PLAYFIELD GRAPHICS

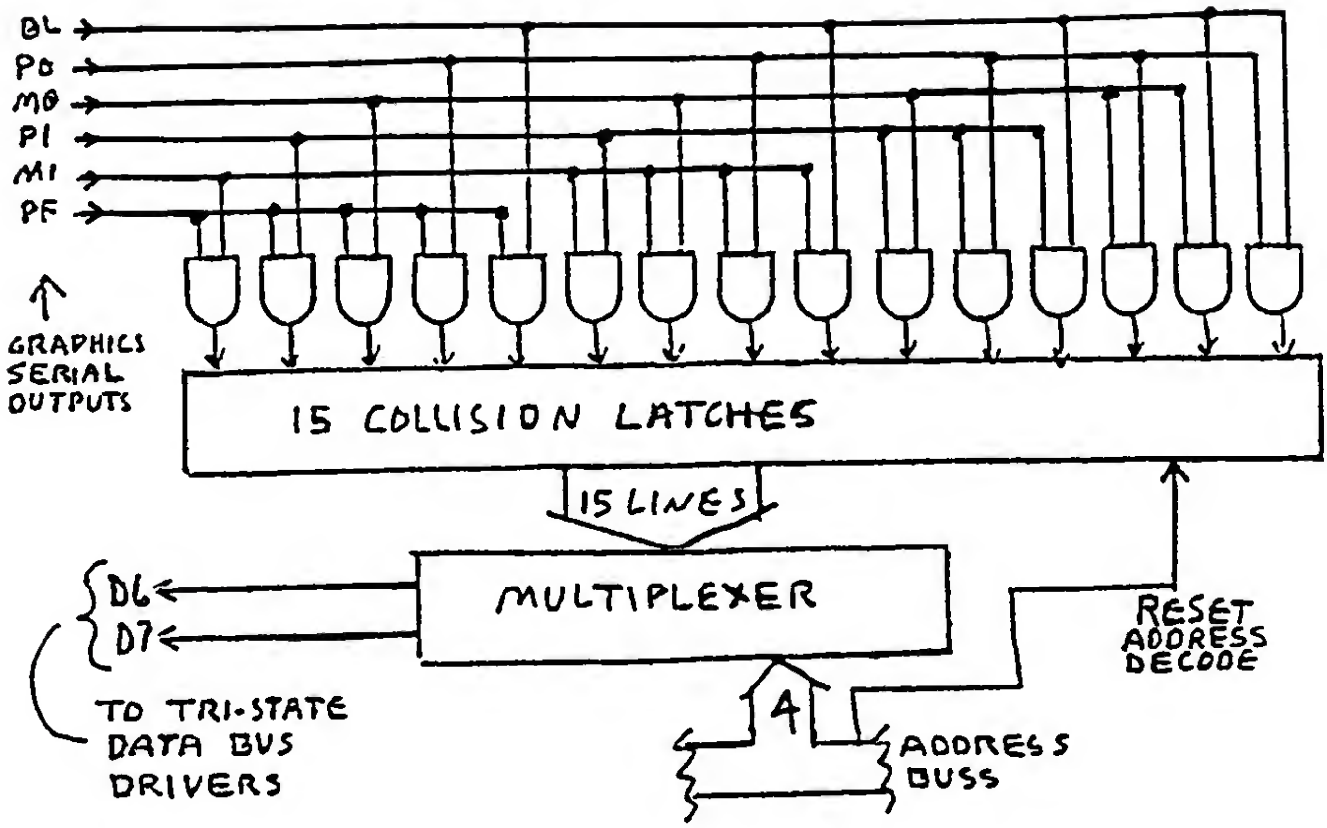


FIGURE 6. COLLISION DETECTION

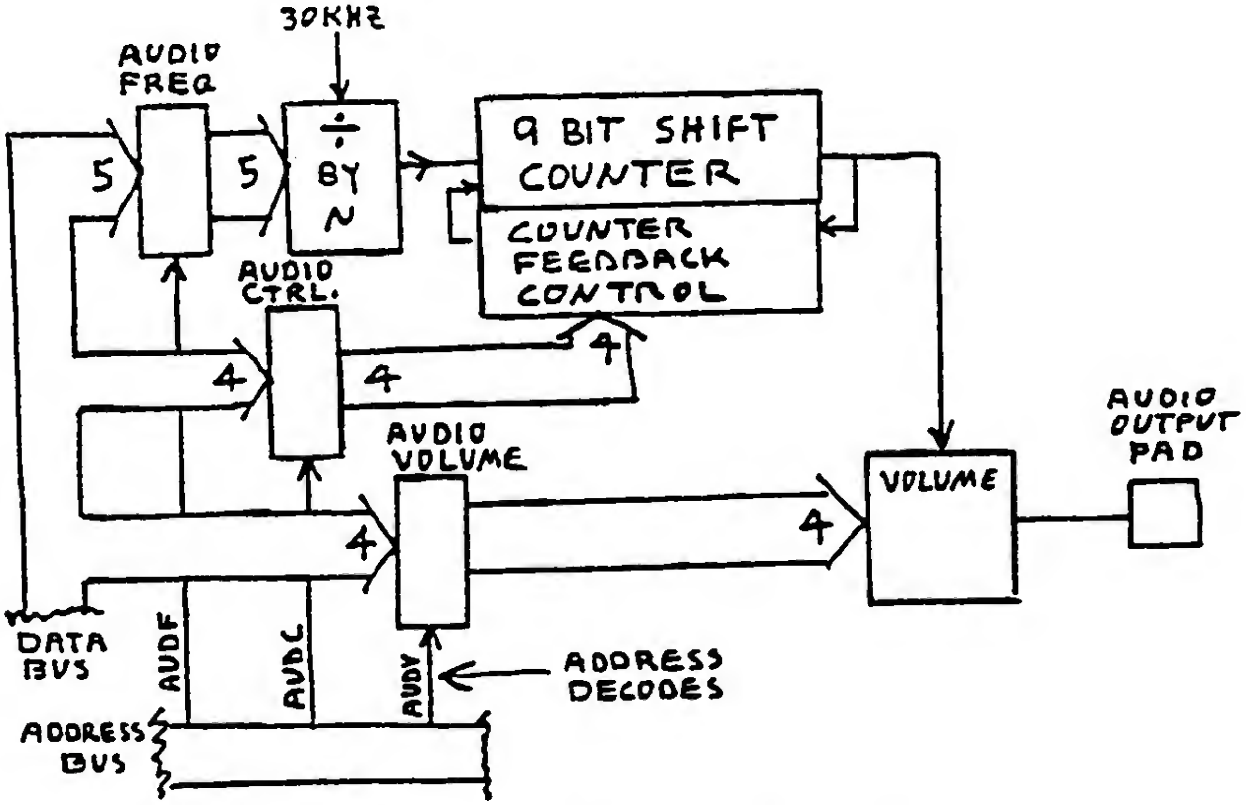


FIGURE 7. AUDIO CIRCUIT

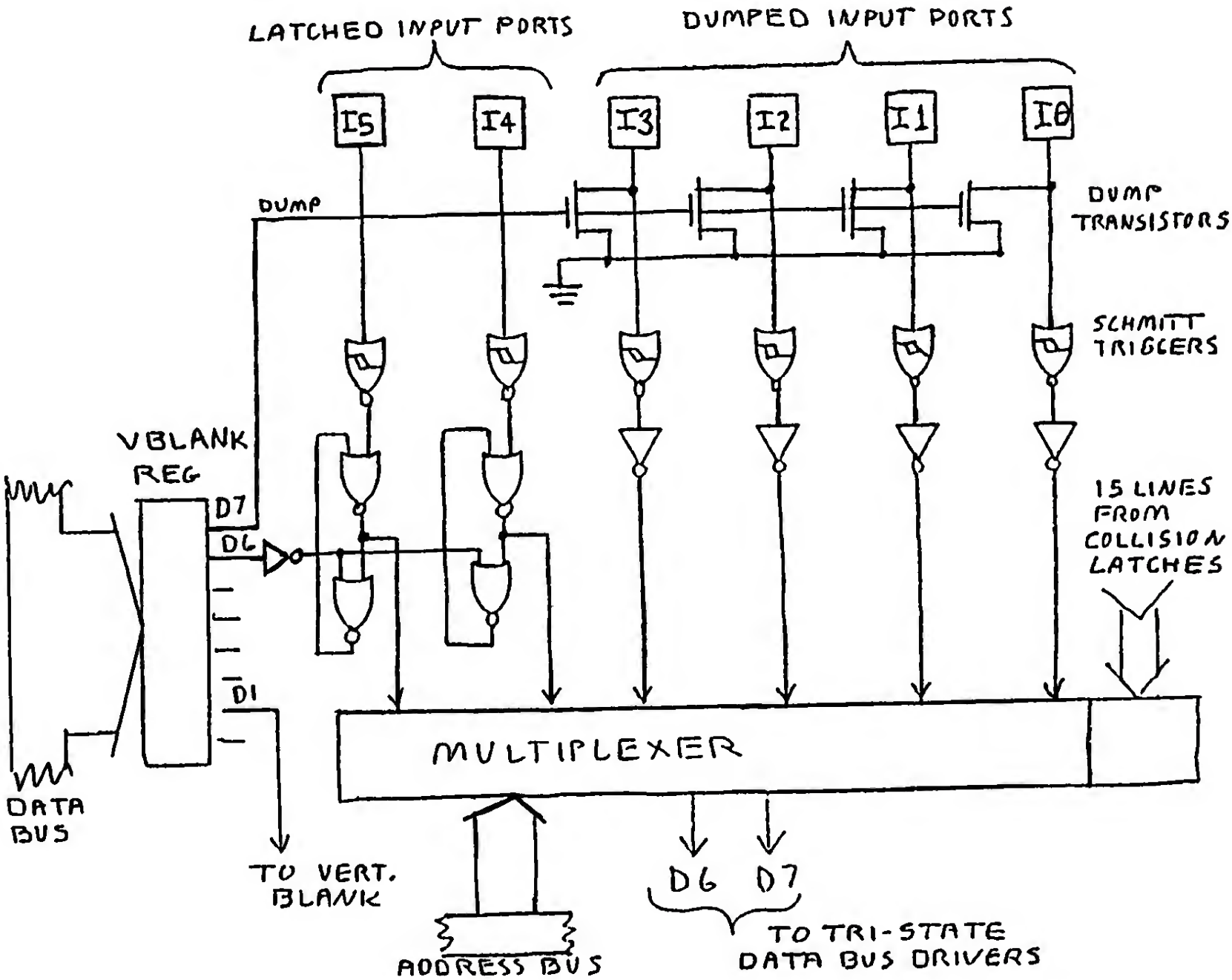


FIGURE 8. INPUT PORTS

WRITE ADDRESS DETAILED FUNCTIONS

WSYNC wait for sync

THIS ADDRESS HALTS MICROPROCESSOR BY CLEARING RDY LATCH TO ZERO. RDY IS SET TRUE AGAIN BY THE LEADING EDGE OF HORIZONTAL BLANK.

DATA BITS NOT USED

RSYNC reset sync

THIS ADDRESS RESETS THE HORIZONTAL SYNC COUNTER TO DEFINE THE BEGINNING OF HORIZONTAL BLANK TIME, AND IS USED IN CHIP TESTING.

DATA BITS NOT USED

VSYNC

THIS ADDRESS CONTROLS VERTICAL SYNC TIME BY WRITING D1 INTO THE VSYNC LATCH.

.... NOT USED	D1	---

1 START VERT. SYNC
0 STOP VERT. SYNC

VBLANK THIS ADDRESS CONTROLS VERTICAL BLANK AND THE LATCHES AND DUMPING TRANSISTORS ON THE INPUT PORTS BY WRITING INTO BITS D7, D6 AND D1 OF THE VBLANK REGISTER.

D7	D6	⨯	D1	X

D1 { 1 START VERT. BLANK; 0 STOP VERT. BLANK }

D6 { 1 ENABLE I_4 I_5 LATCHES; 0 DISSABLE I_4 I_5 LATCHES }

NOTE; DISSABLE LATCHES (D6=0) ALSO RESETS LATCHES TO LOGIC TRUE

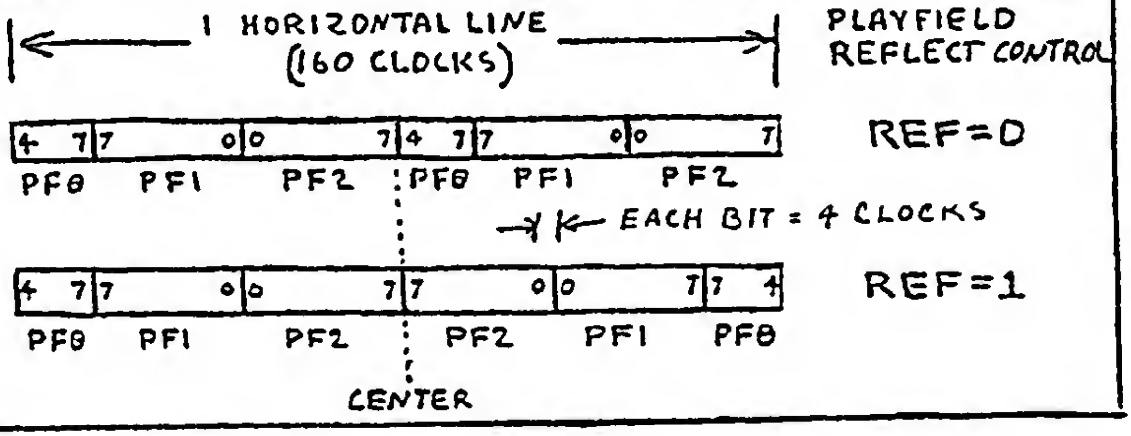
D7 { 1 DUMP I_0 I_1 I_2 I_3 PORTS TO GROUND; 0 REMOVE DUMP PATH TO GROUND }

PF0 (PF1, PF2)

THESE ADDRESSES ARE USED TO WRITE INTO THE PLAYFIELD REGISTERS

D7	D6	D5	D4	X	X	X	X	PF0
D7	D6	D5	D4	D3	D2	D1	D0	PF1
D7	D6	D5	D4	D3	D2	D1	D0	PF2

PLAYFIELD REGISTERS SERIAL OUTPUT



CTRLPF

THIS ADDRESS IS USED TO WRITE INTO THE PLAYFIELD CONTROL REGISTER (A LOGIC 1 CAUSES ACTION AS DESCRIBED BELOW)

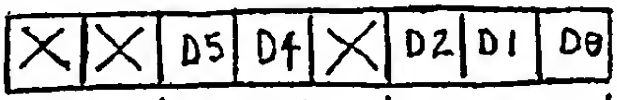
X	X	D5	D4	X	D2	D1	D0

- D0 — REF (REFLECT PLAYFIELD)
- D1 — SCORE (LEFT HALF OF PLAYFIELD GETS COLOR OF PLAYER 0 RIGHT HALF GETS COLOR OF PLAYER 1)
- D2 — PFP (PLAYFIELD GETS PRIORITY OVER PLAYERS SO THEY MOVE BEHIND PLAYFIELD)
- D4, D5 — BALL SIZE

D5	D4	WIDTH
0	0	1 CLOCK
0	1	2 CLOCKS
1	0	4 CLOCKS
1	1	8 CLOCKS

NUSIZ0 (NUSIZ1)

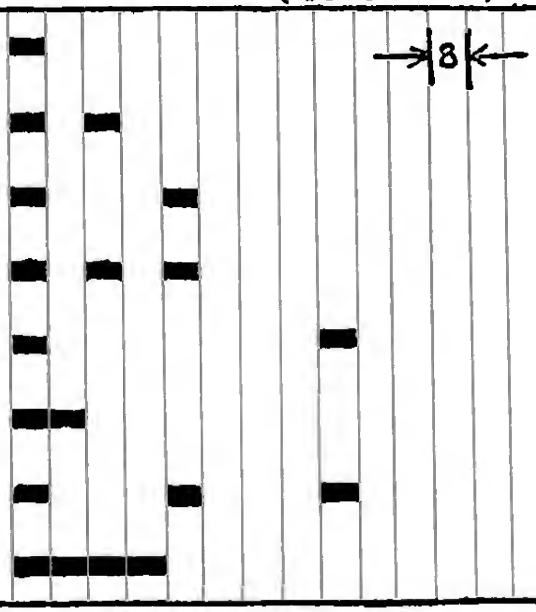
THESE ADDRESSES CONTROL THE NUMBER AND SIZE OF PLAYERS AND MISSILES.



MISSILE SIZE

D5	D4	WIDTH
0	0	1 CLOCK
0	1	2 CLOCKS
1	0	4 CLOCKS
1	1	8 CLOCKS

PLAYER-MISSILE NUMBER & PLAYER SIZE

D2 D1 D0	1 TELIVISION LINE (160 CLOCKS)	DESCRIPTION
0 0 0		ONE COPY
0 0 1		TWO COPIES CLOSE
0 1 0		TWO COPIES MED
0 1 1		THREE COPIES CLOSE
1 0 0		TWO COPIES WIDE
1 0 1		DOUBLE SIZE PLAYER
1 1 0		3 COPIES MEDIUM
1 1 1		QUAD SIZE PLAYER

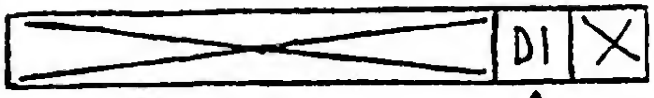
RESP0 (RESP1, RESM0, RESM1, RESBL)

THESE ADDRESSES ARE USED TO RESET PLAYERS MISSILES AND THE BALL. THE OBJECT WILL BEGIN ITS SERIAL GRAPHICS AT THAT TIME OF A HORIZONTAL LINE AT WHICH THE RESET ADDRESS OCCURS.

NO DATA BITS ARE USED

RESMP0 (RESMP1)

THESE ADDRESSES ARE USED TO RESET THE HORIZ. LOCATION OF A MISSILE TO THE CENTER OF IT'S CORRESPONDING PLAYER. AS LONG AS THIS CONTROL BIT IS TRUE (1) THE MISSILE WILL REMAIN LOCKED TO THE CENTER OF IT'S PLAYER AND THE MISSILE GRAPHICS WILL BE DISSABLED. WHEN A ZERO IS WRITTEN INTO THIS LOCATION THE MISSILE IS ENABLED, AND CAN BE MOVED INDEPENDENTLY FROM THE PLAYER.



RESMP (MISSILE-PLAYER RESET)

HMOVE

THIS ADDRESS CAUSES THE HORIZONTAL MOTION REGISTER VALUES TO BE ACTED UPON DURING THE HORIZONTAL BLANK TIME IN WHICH IT OCCURS. IT MUST OCCUR AT THE BEGINNING OF HORIZ. BLANK IN ORDER TO ALLOW TIME FOR GENERATION OF EXTRA CLOCK PULSES INTO THE HORIZONTAL POSITION COUNTERS. IF MOTION IS DESIRED, THIS COMMAND MUST IMMEDIATELY FOLLOW A WSYNC COMMAND IN THE PROGRAM.

NO DATA BITS ARE USED

HMCLR

THIS ADDRESS CLEARS ALL HORIZONTAL MOTION REGISTERS TO ZERO (NO MOTION)

NO DATA BITS ARE USED

HMP0 (HMP1, HMM0, HMM1, HMBL)

THESE ADDRESSES WRITE DATA (HORIZONTAL MOTION VALUES) INTO THE HORIZONTAL MOTION REGISTERS. THESE REGISTERS WILL CAUSE HORIZONTAL MOTION ONLY WHEN COMMANDED TO DO SO BY THE HORIZ. MOVE COMMAND HMOVE.

THE MOTION VALUES ARE CODED AS SHOWN BELOW

D7	D6	D5	D4		
0	1	1	1	+7	MOVE LEFT INDICATED NUMBER OF CLOCKS
0	1	1	0	+6	
0	1	0	1	+5	
0	1	0	0	+4	
0	0	1	1	+3	
0	0	1	0	+2	
0	0	0	1	+1	
0	0	0	0	0	NO MOTION
1	1	1	1	-1	MOVE RIGHT INDICATED NUMBER OF CLOCKS
1	1	1	0	-2	
1	1	0	1	-3	
1	1	0	0	-4	
1	0	1	1	-5	
1	0	1	0	-6	
1	0	0	1	-7	
1	0	0	0	-8	

WARNING: These motion registers should not be modified during the 24 Computer cycles immediately following an E Move command. Unpredictable motion values may result.

ENAM0 (ENAM1, ENABL)

THESE ADDRESSES WRITE D1 INTO THE 1 BIT MISSILE OR BALL GRAPHICS REGISTERS.

	D1	

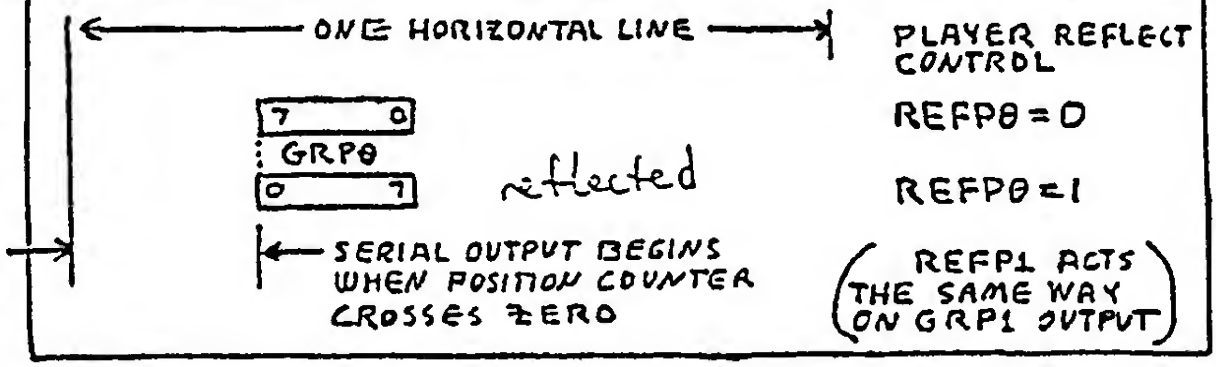
0 DISSABLES OBJECT
1 ENABLES OBJECT

GRP0(GRP1)

THESE ADDRESSES WRITE DATA INTO THE PLAYER GRAPHICS REGISTERS

D7	D6	D5	D4	D3	D2	D1	D0

PLAYER GRAPHICS REGISTER SERIAL OUTPUT



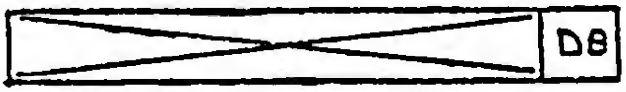
REFP0(REFP1)

THESE ADDRESSES WRITE D3 INTO THE 1 BIT PLAYER REFLECT REGISTERS.

0 NO REFLECT (D7 OF GRP ON LEFT)
1 REFLECT (D0 OF GRP ON LEFT)

VDELP0(VDELP1, VDELBL)

THESE ADDRESSES WRITE D0 INTO THE 1 BIT VERTICAL DELAY REGISTERS, TO DELAY PLAYERS OR BALL BY ONE VERTICAL LINE.



0 NO DELAY
1 DELAY

CXCLR

THIS ADDRESS CLEARS ALL COLLISION LATCHES TO ZERO (NO COLLISION)

DATA BITS NOT USED

COLUP0 (COLUP1, COLUPF, COLUBK)

THESE ADDRESSES WRITE DATA INTO THE PLAYER, PLAYFIELD, AND BACKGROUND COLOR-LUMINENCE REGISTERS.

COLOR	D7	D6	D5	D4	D3	D2	D1	X	LUM
	COLOR				LUM				
GREY-GOLD	0	0	0	0	0	0	0		BLACK
	0	0	0	1	0	0	1		DARK GREY
ORANGE, RED-ORG	0	0	1	0	0	1	0		⋮
	0	0	1	1	0	1	1		GREY
PINK-PURPLE	0	1	0	0	1	0	0		⋮
	0	1	0	1	1	0	1		⋮
PURP-BLUE BLUE	0	1	1	0	1	1	0		LIGHT GREY
	0	1	1	1	1	1	1		WHITE
BLUE-LT. BLUE	1	0	0	0					
	1	0	0	1					
TORQ-GRN. BLUE	1	0	1	0					
	1	0	1	1					
GRN.-YEL., GRN.	1	1	0	0					
	1	1	0	1					
ORG. GRN-LT. ORG.	1	1	1	0					
	1	1	1	1					

AUDF0 (AUDF1)

THESE ADDRESSES WRITE DATA INTO THE AUDIO FREQUENCY DIVIDER REGISTERS.

X	D4	D3	D2	D1	D0	30KHZ DIVIDED BY
	0	0	0	0	0	DIVIDE BY 1 (NO DIVISION)
	0	0	0	0	1	DIVIDE BY 2
	0	0	0	1	0	DIVIDE BY 3
	-	-	-	-	-	⋮
	1	1	1	1	0	DIVIDE BY 31
	1	1	1	1	1	DIVIDE BY 32

AUDC0(AUDC1)

THESE ADDRESSES WRITE DATA INTO THE AUDIO CONTROL REGISTERS WHICH CONTROL THE NOISE CONTENT AND ADDITIONAL DIVISION OF THE AUDIO OUTPUT.

HEX CODE	D3	D2	D1	D0	TYPE OF NOISE OR DIVISION
0	0	0	0	0	SET TO 1
1	0	0	0	1	4 BIT POLY
2	0	0	1	0	÷15 → 4 BIT POLY
3	0	0	1	1	5 BIT POLY → 4 BIT POLY
4	0	1	0	0	÷2 } pure tone
5	0	1	0	1	÷2 } pure tone
6	0	1	1	0	÷31 } pure tone
7	0	1	1	1	5 BIT POLY → ÷2
8	1	0	0	0	9 BIT POLY (WHITE NOISE)
9	1	0	0	1	5 BIT POLY
A	1	0	1	0	÷31 } pure tone
B	1	0	1	1	SET LAST 4 BITS TO 1
C	1	1	0	0	÷6 } pure tone
D	1	1	0	1	÷6 } pure tone
E	1	1	1	0	÷93 } pure tone
F	1	1	1	1	5 BIT POLY ÷6

AUDV0(AUDV1)

THESE ADDRESSES WRITE DATA INTO THE AUDIO VOLUME REGISTERS WHICH SET THE PULL DOWN IMPEDANCE DRIVING THE AUDIO OUTPUT PADS.

D3	D2	D1	D0	AUDIO OUTPUT PULLDOWN CURRENT
0	0	0	0	NO OUTPUT CURRENT
0	0	0	1	LOWEST
0	0	1	0	
–	–	–	–	
1	1	1	0	
1	1	1	1	HIGHEST

WRITE ADDRESS SUMMARY

REV. NOV 1977

6 BIT ADDRESS		ADDRESS NAME	DATA BITS USED		FUNCTION
OCT	HEX		7 6 5 4 3 2 1 0		
00	00	VSYNC		1	VERTICAL SYNC SET-CLEAR
01	01	VBLANK	1 1	1	VERTICAL BLANK SET-CLEAR
02	02	WSYNC	STROBE		WAIT FOR LEADING EDGE OF HORIZONTAL BLANK
03	03	RSYNC	STROBE		RESET HORIZONTAL SYNC COUNTER
04	04	NUSIZ 0	1 1	1 1 1	NUMBER-SIZE PLAYER-MISSILE 0
05	05	NUSIZ 1	1 1	1 1 1	NUMBER-SIZE PLAYER-MISSILE 1
06	06	COLUP0	1 1 1 1	1 1 1	COLOR-LUM PLAYER 0
07	07	COLUP1	1 1 1 1	1 1 1	COLOR-LUM PLAYER 1
10	08	COLUPF	1 1 1 1	1 1 1	COLOR-LUM PLAYFIELD
11	09	COLUBK	1 1 1 1	1 1 1	COLOR-LUM BACKGROUND
12	0A	CTRLPF	1 1	1 1 1	CONTROL PLAYFIELD BALL SIZE AND COLLISIONS
13	0B	REFP0		1	REFLECT PLAYER 0
14	0C	REFP1		1	REFLECT PLAYER 1
15	0D	PF0	1 1 1 1		PLAYFIELD REG. BYTE 0
16	0E	PF1	1 1 1 1	1 1 1 1	PLAY FIELD REG. BYTE 1
17	0F	PF2	1 1 1 1	1 1 1 1	PLAY FIELD REG. BYTE 2
20	10	RESP0	STROBE		RESET PLAYER 0
21	11	RESP1	STROBE		RESET PLAYER 1
22	12	RESM0	STROBE		RESET MISSILE 0
23	13	RESM1	STROBE		RESET MISSILE 1
24	14	RESBL	STROBE		RESET BALL
25	15	AUDC0		1 1 1 1	AUDIO CONTROL 0
26	16	AUDC1		1 1 1 1	AUDIO CONTROL 1

WRITE ADDRESS SUMMARY

6 BIT ADDRESS		ADDRESS NAME	DATA BITS USED		FUNCTION
OCT	HEX		7 6 5 4	3 2 1 0	
27	17	AUDF0	1	1 1 1 1	AUDIO FREQUENCY 0
30	18	AUDF1	1	1 1 1 1	AUDIO FREQUENCY 1
31	19	AUDV0		1 1 1 1	AUDIO VOLUME 0
32	1A	AUDV1		1 1 1 1	AUDIO VOLUME 1
33	1B	GRP0	1 1 1 1	1 1 1 1	GRAPHICS PLAYER 0
34	1C	GRP1	1 1 1 1	1 1 1 1	GRAPHICS PLAYER 1
35	1D	ENAM0		1	GRAPHICS (ENABLE) MISSILE 0
36	1E	ENAM1		1	GRAPHICS (ENABLE) MISSILE 1
37	1F	ENABL		1	GRAPHICS (ENABLE) BALL
40	20	HMP0	1 1 1 1		HORIZONTAL MOTION PLAYER 0
41	21	HMP1	1 1 1 1		HORIZONTAL MOTION PLAYER 1
42	22	HMM0	1 1 1 1		HORIZONTAL MOTION MISSILE 0
43	23	HMM1	1 1 1 1		HORIZONTAL MOTION MISSILE 1
44	24	HMBL	1 1 1 1		HORIZONTAL MOTION BALL
45	25	VDELP0		1	VERTICAL DELAY PLAYER 0
46	26	VDELP1		1	VERTICAL DELAY PLAYER 1
47	27	VDELBL		1	VERTICAL DELAY BALL
50	28	RESMP0		1	RESET MISSILE 0 TO PLAYER 0
51	29	RESMP1		1	RESET MISSILE 1 TO PLAYER 1
52	2A	HMOVE	STROBE		APPLY HORIZONTAL MOTION
53	2B	HMCLR	STROBE		CLEAR HORIZ. MOTION REGS.
54	2C	CXCLR	STROBE		CLEAR COLLISION LATCHES

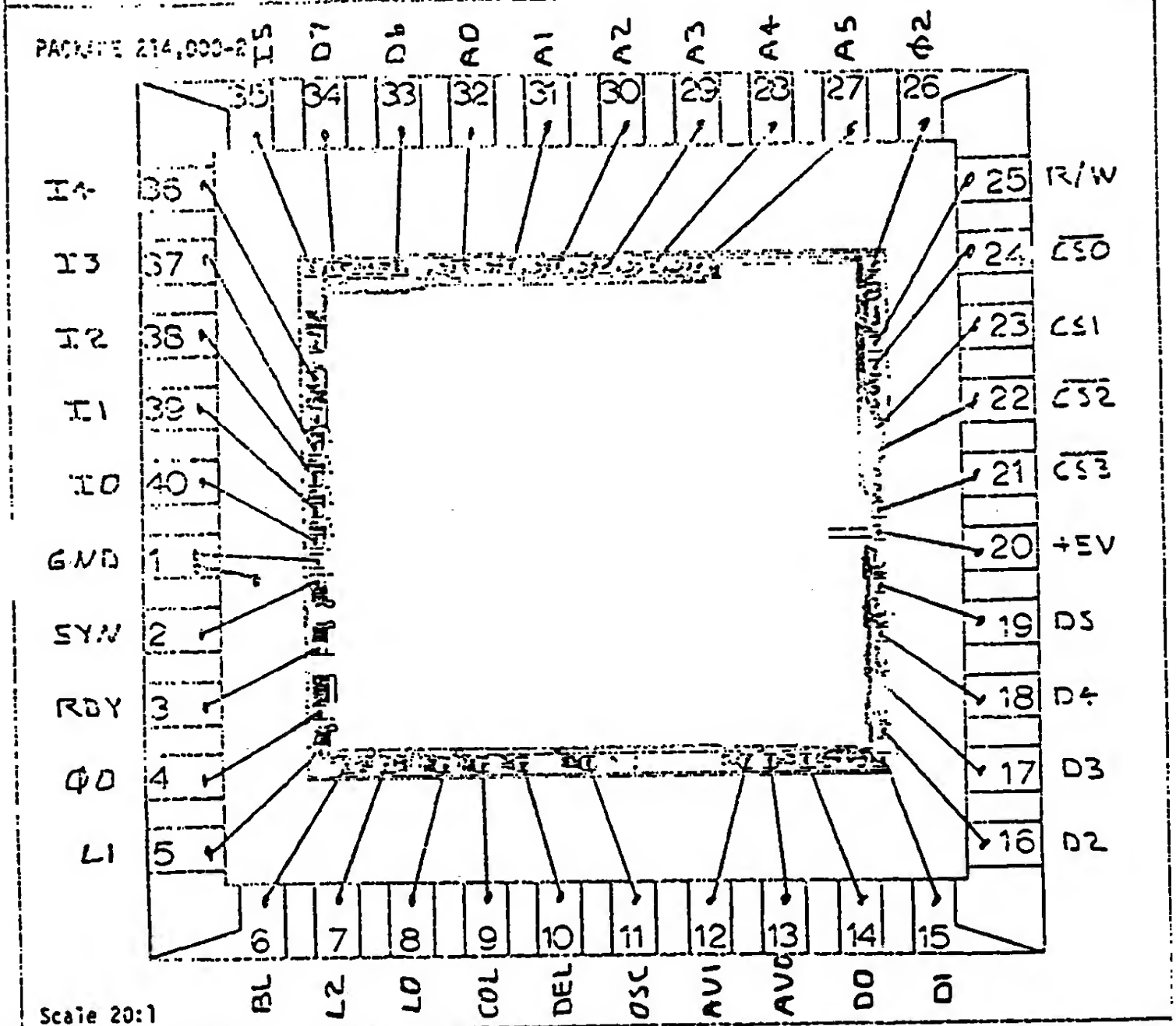
READ ADDRESS SUMMARY

REV NOV 2 1976

6 BIT ADDRESS		ADDRESS NAME	DATA BITS USED		FUNCTION		
OCT	HEX		7 6 5 4 3 2 1 0			D7	D6
00	00	CXM0P	1 1		READ COLLISION	M0·P1	M0·P0
01	01	CXM1P	1 1		"	M1·P0	M1·P1
02	02	CXP0FB	1 1		"	P0·PF	P0·BL
03	03	CXP1FB	1 1		"	P1·PF	P1·BL
04	04	CXM0FB	1 1			M0·PF	M0·BL
05	05	CXM1FB	1 1			M1·PF	M1·BL
06	06	CXBLPF	1			BL·PF	~~NOT USED~~
07	07	CXPPMM	1 1			P0·P1	M0·M1
10	08	INPT0	1		READ POT PORT	I0	
11	09	INPT1	1		READ POT PORT	I1	
12	0A	INPT2	1		READ POT PORT	I2	
13	0B	INPT3	1		READ POT PORT	I3	
14	0C	INPT4	1		READ INPUT	I4	
15	0D	INPT5	1		READ INPUT	I5	

NOTE: I0, I1, I2, I3 CAN be grounded under SOFTWARE CONTROL.

I4, I5 CAN be CONVERTED TO LATCHED INPUTS UNDER SOFTWARE CONTROL.



Scale 20:1

Basic Die Type C10291

Die Size 202 x 181

Process Flow ☒ Standard NSJO

☐ Process per

Wire Bond 1.25 mil aluminum U.S.

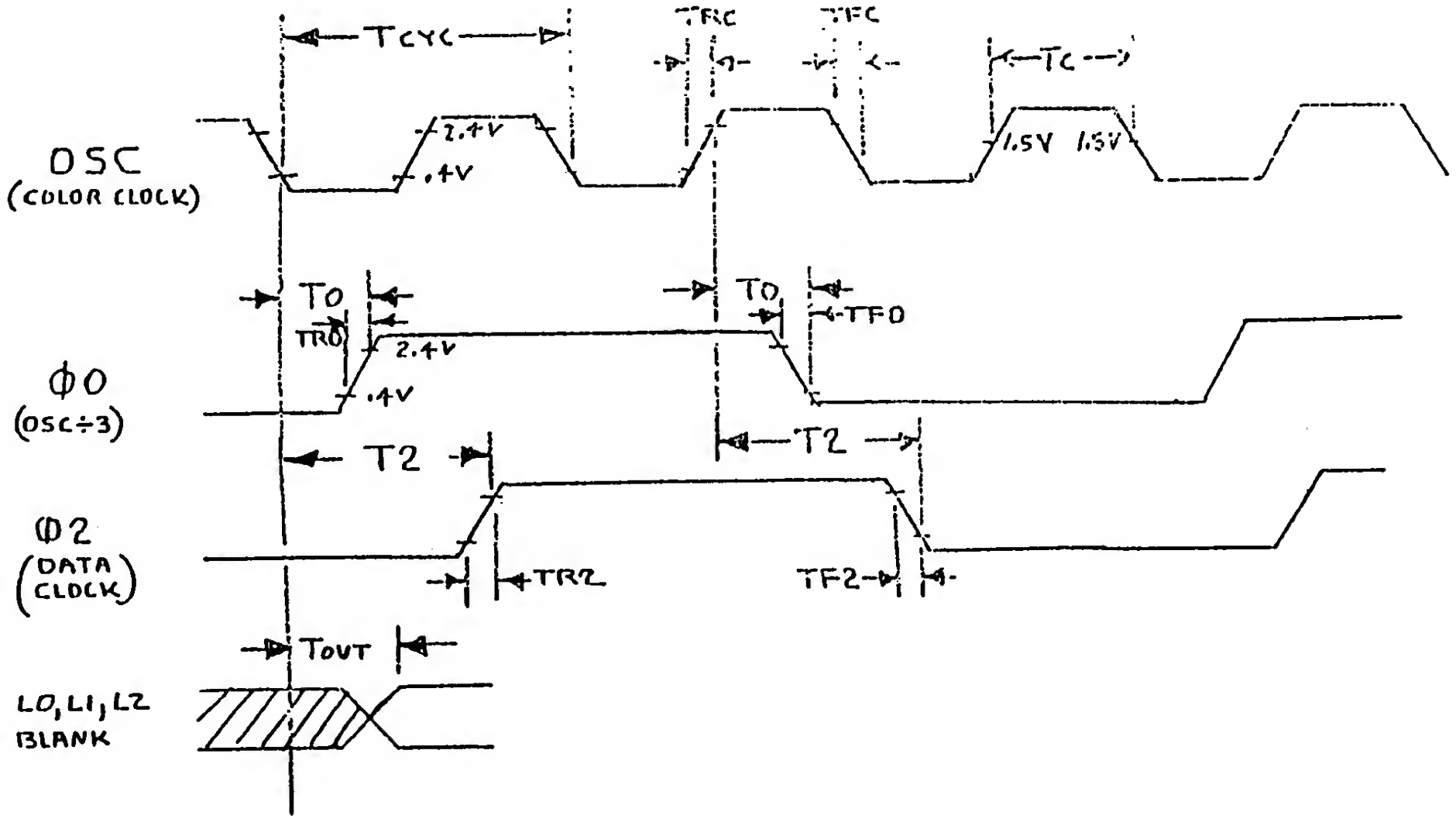
Die Attach Cavity 240 sq.

Die Attach Preform

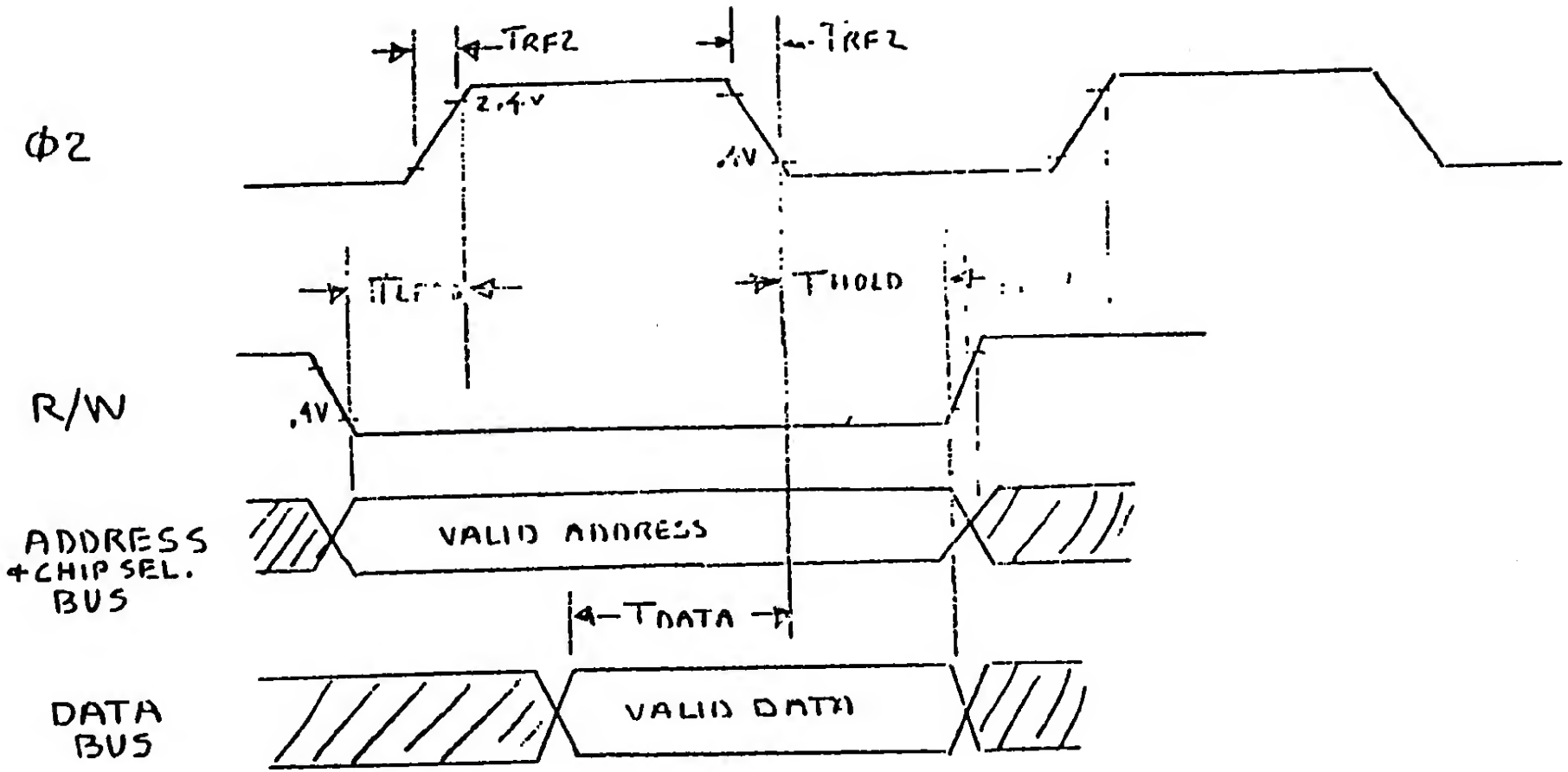
Synertek 1050 TORADALE DRIVE SANTA CLARA, CA 95051	CERAMIC PACKAGE BONDING DIAGRAM	DOCUMENT NUMBER	REV.
		SHEET	

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
OSC CYCLE TIME	TCYC	260	280	-	NSEC
OSC DUTY CYCLE	TC/TCYC	45	50	55	PERCENT
OSC RISE-FALL TIMES	TRC-TFC			25	NSEC
Φ0 (OSC÷3) DELAY	TO			100	NSEC
Φ0 RISE-FALL TIMES	TRO-TFO			25	NSEC
Φ2 (DATA CLOCK) DELAY	T2			250	NSEC
LUMINANCE DELAY	TOUT			100	NSEC
HORIZ SYNC DELAY	TVS			100	NSEC
VERT SYNC DELAY	THS			100	NSEC
WAIT FOR SYNC DELAY	TWS			100	NSEC
READY DELAY	TRDY			100	NSEC
R/W-ADD LEAD TIME	TLEAD	180			NSEC
DATA BUS LEAD TIME	TDATA	300			NSEC
R/W-DATA HOLD TIME	THOLD	10			NSEC
Φ2 RISE-FALL TIME	TRF2			25	NSEC
READ DATA LAG TIME	TDLAG			395	NSEC

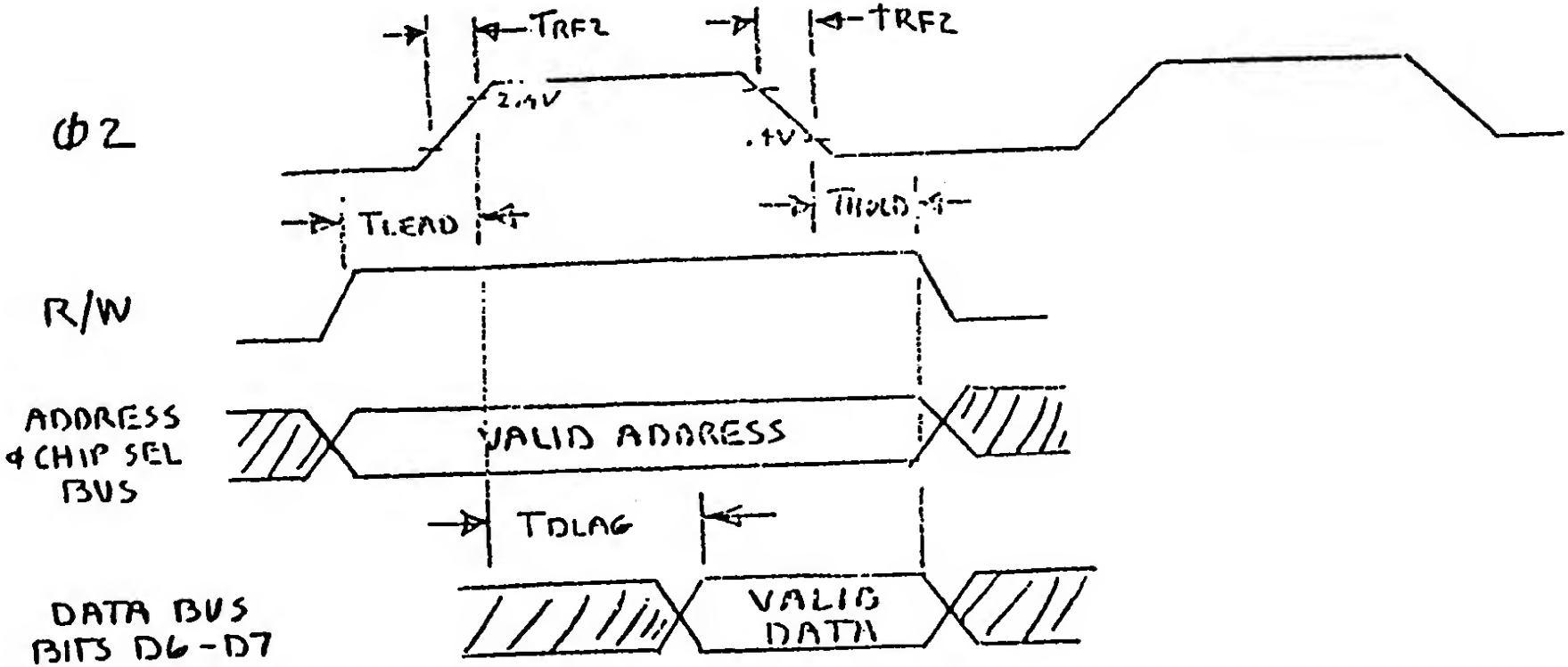
TIA TIMING CHARACTERISTICS



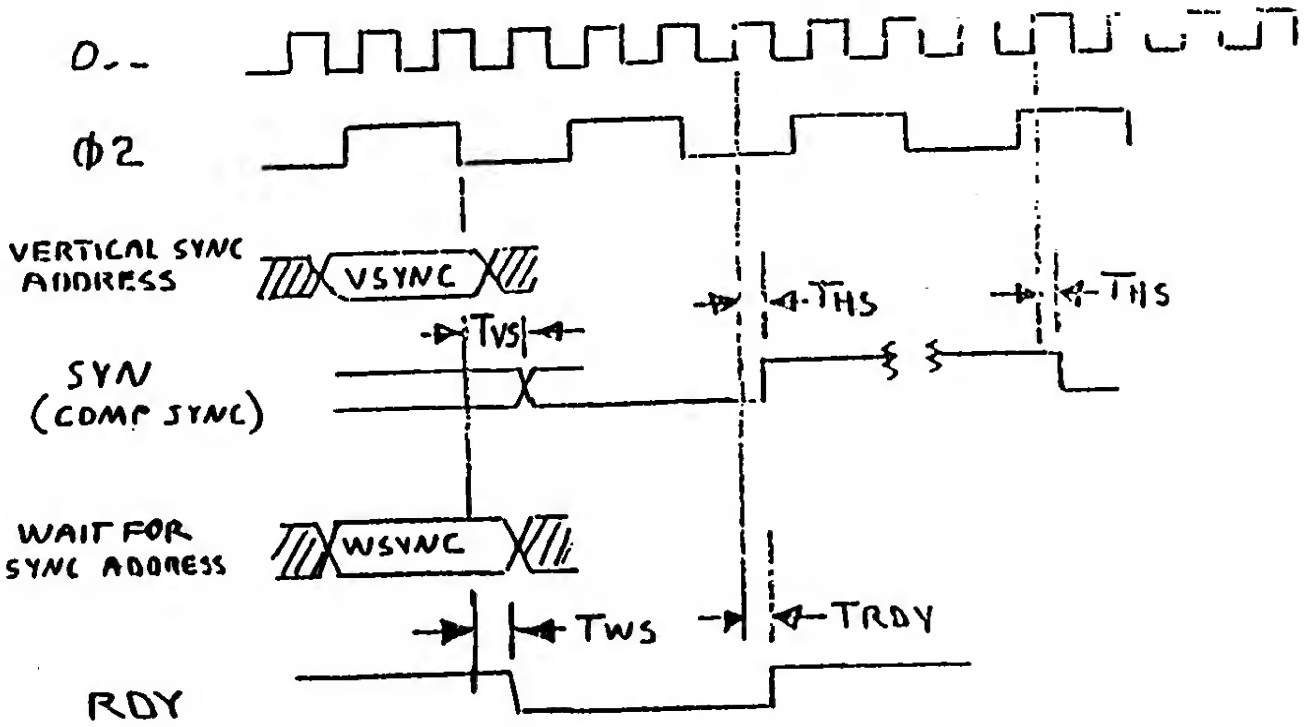
TIA ϕ0 – ϕ2 AND LUM TIMING



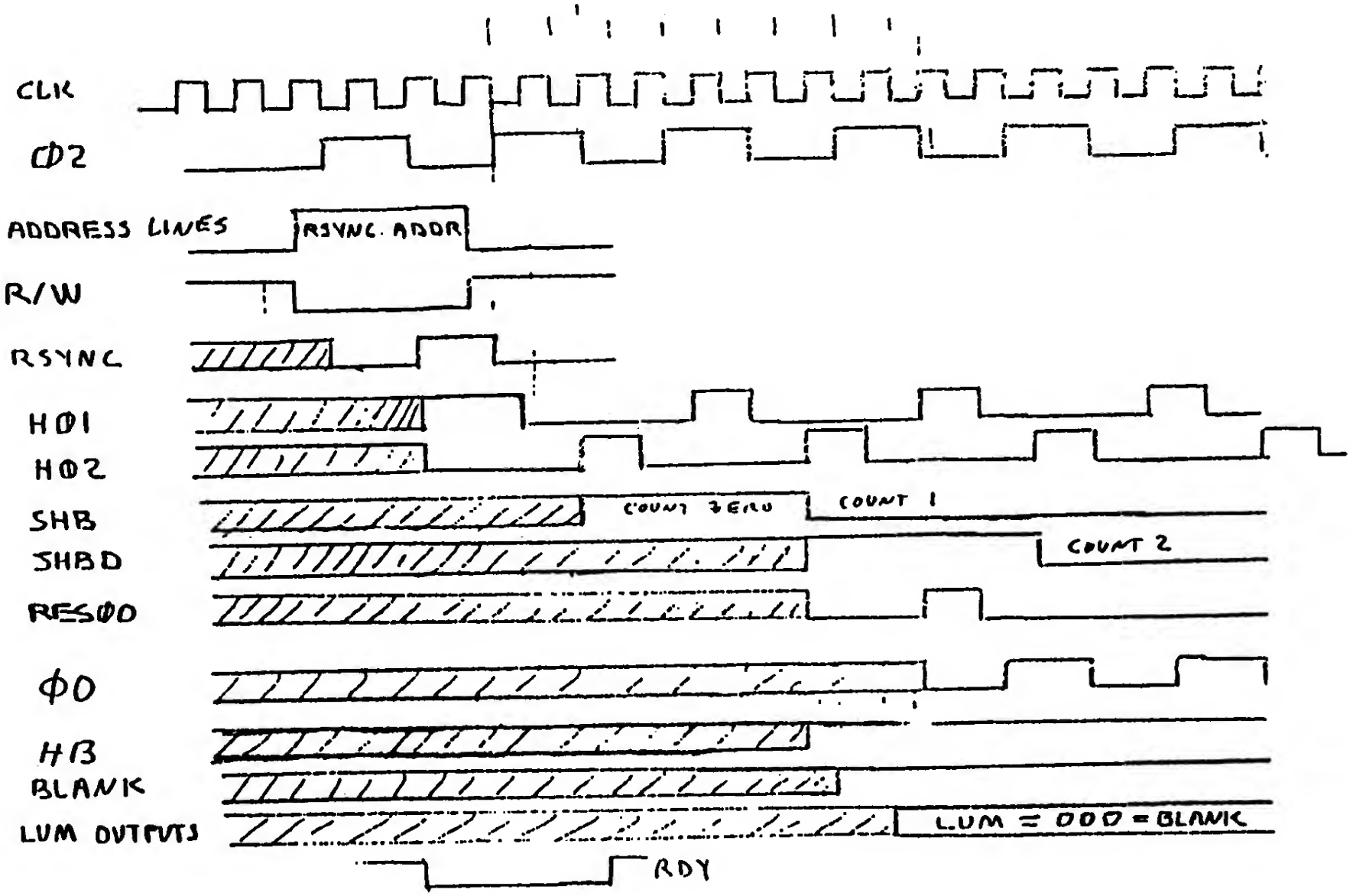
TIM WRITE TIMING CHARACTERISTICS



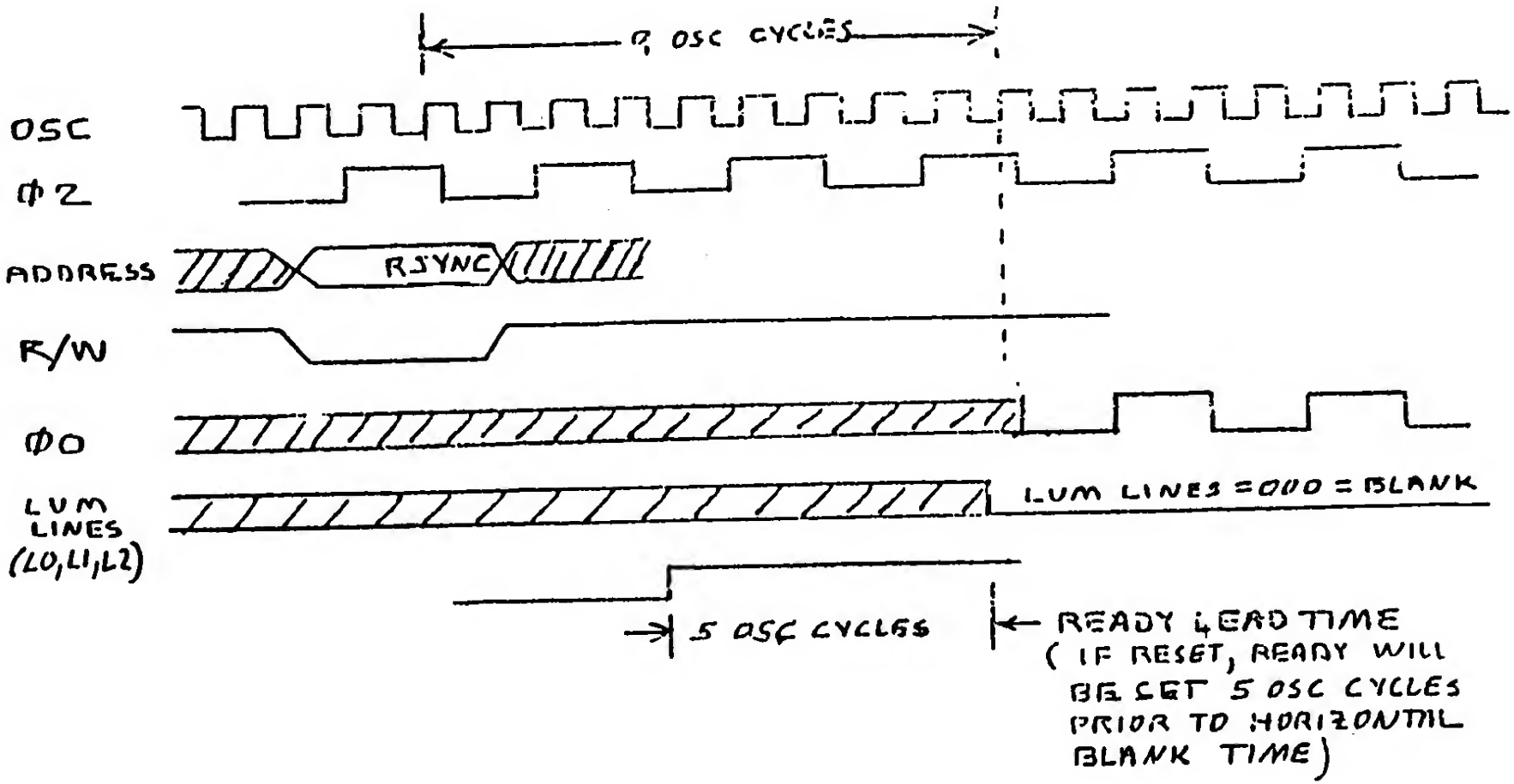
TIA READ TIMING CHARACTERISTICS



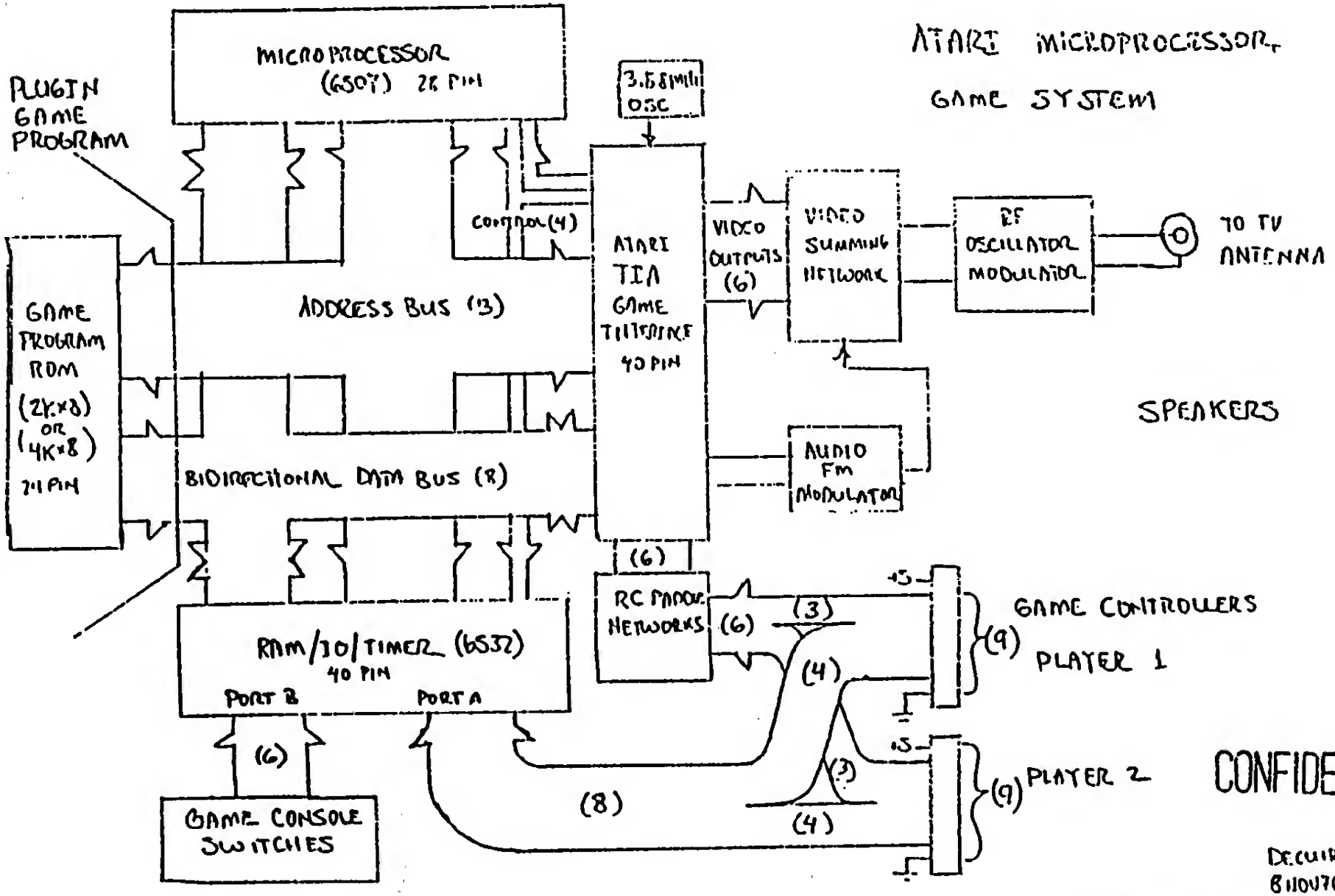
TIA COMP-SYN AND READY TIMING



RSYNC - RESØD - HØ1 - HØ2 - SHB - Ø2 - ØO



TIA RSYNC AND BLANK AND READY TIMING


ATARI MICROPROCESSOR
GAME SYSTEM
MICROPROCESSOR (6507) 28 PIN
3.58MHz OSC
PLUGIN GAME PROGRAM
CONTROL (4)
ATARI TIA GAME INTERFACE 40 PIN
VIDEO OUTPUTS (6)
VIDEO SUMMING NETWORK
RF OSCILLATOR MODULATOR
TO TV ANTENNA
GAME PROGRAM ROM (2K×8) OR (4K×8) 24 PIN
ADDRESS BUS (13)
BIDIRECTIONAL DATA BUS (8)
AUDIO FM MODULATOR
SPEAKERS
(6)
RC PADDLE NETWORKS
+5
(6)
(3)
(4)
(9)
GAME CONTROLLERS
PLAYER 1
RAM/IO/TIMER (6532) 40 PIN
PORT B
PORT A
(6)
(8)
(3)
(4)
(9)
PLAYER 2
GAME CONSOLE SWITCHES
CONFIDENTIAL
DECUIR
BIIOU76
CC: TIA DESCRIPTIONS, PRU 17FEB77
PAIGE ADDUCTS

SARA PROGRAMMING INSTRUCTIONS

Sara is a 128 by 8 RAM that is Memory mapped into the VCS cartridge slot (F000 to FFFF). RAM write addresses are F000 to F07F. RAM read addresses are F080 to F0FF. The RAM read and write adresses over ride the ROM in that address space. Sara RAM cannot be used as program space i.e., data storage only.

Accessing Sara can be done by most instructions with address modes: absolute, absolute indexed by X, absolute indexed by Y, indexed indirect, or indirect indexed by Y. The exceptions are any instruction that required the 6507 to read RAM, modify the data, and write that data back into memory. Also in the indexing modes, the address plus the index cannot cross a page boundry, where a page boundry size is 256 bytes.

VCS CARTRIDGE MEMORY MAP