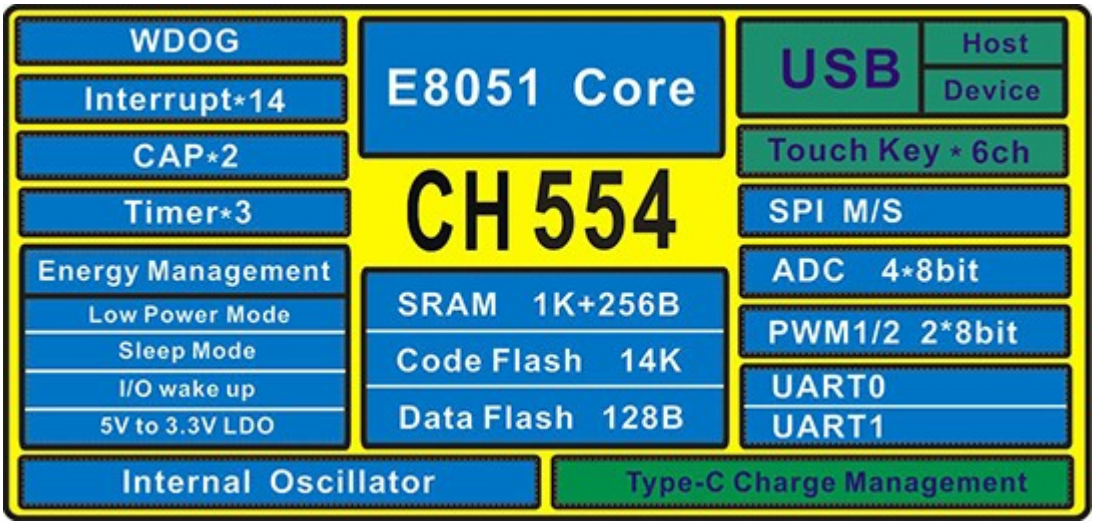
8-bit enhanced USB microcontroller CH554, CH553

Manual

Version: 1E
http://wch.cn
Translated to the English by Blinkinlabs

1. Overview



The CH554 chip is an enhanced E8051 core microcontroller compatible with the MCS51 instruction set. Its 79% instruction is a single-byte single-cycle instruction, and the average instruction speed is 8 to 15 times faster than the standard MCS51.

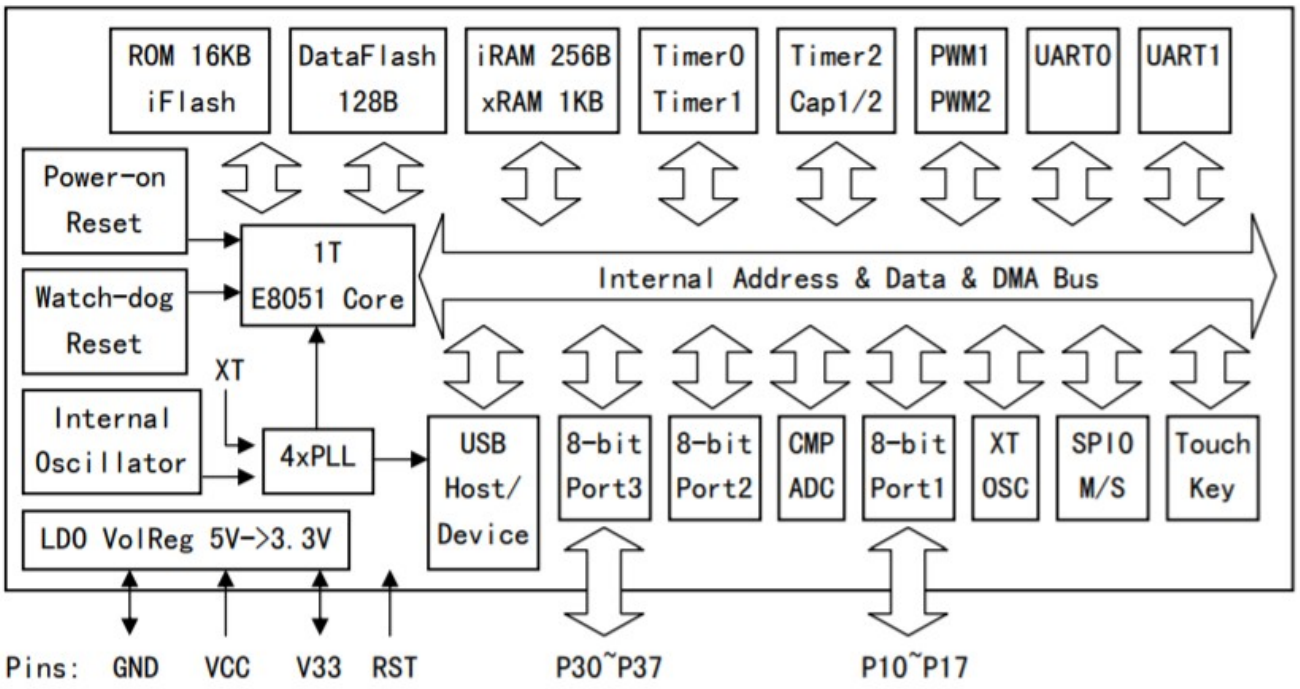
CH554 supports up to 24MHz system main frequency, built-in 16K program memory ROM and 256 bytes internal iRAM and 1K bytes of on-chip xRAM, xRAM supports DMA direct memory access.

CH554 has built-in ADC analog-to-digital conversion, touch button capacitance detection, 3 groups of timers and signal capture and PWM, dual asynchronous serial port, SPI and other functional modules, support USB-Host host mode and USB-Device device mode.

CH553 is a simplified version of CH554, program memory ROM is 10K, on-chip xRAM is 512 bytes, asynchronous serial port is only UART0, package form is only SOP16, touch button is only 4 channels, other is the same as CH554, can refer to CH554 manual and data directly.

Model	ROM	RAM	Data Flash	USB Host	USB device	Timer	PWM	UART	SPI	ADC	Touch inputs
CH554	16KB	1280	128	Full/low speed	Full/low speed	3	2	2	master /slave	4	6
CH553	10KB	768						1			4

The following is an internal block diagram of CH554, for reference only.



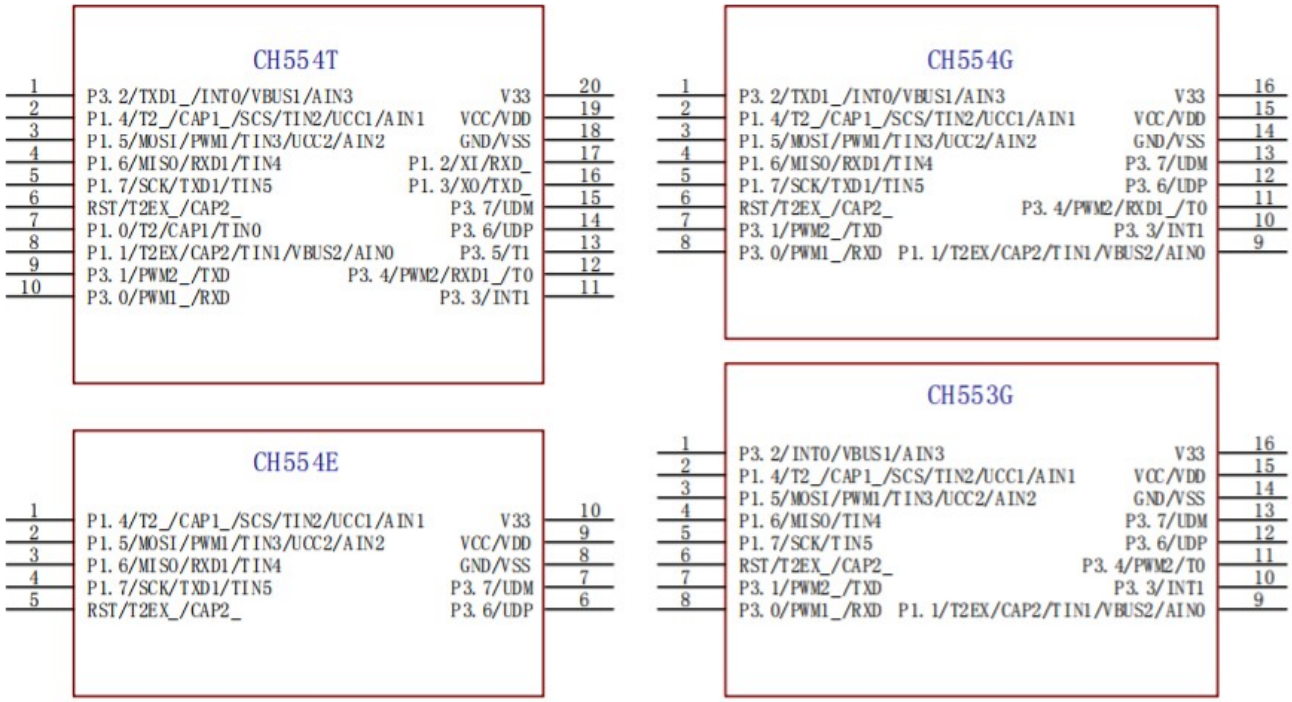
2. Features

- Core: Enhanced E8051 core compatible with MCS51 instruction set, 79% of its instructions are single-byte single-cycle instructions, the average instruction speed 8-15 times faster than the standard MCS51, unique XRAM data fast copy instructions, dual DPTR pointer.
- ROM: 16KB of multiprogrammable non-volatile memory ROM, can be used for program storage space; or can be divided into 14KB program memory and 2KB boot code BootLoader / ISP program area.
- DataFlash: 128 bytes of non-volatile data memory that can be erased many times, and support overwriting data in bytes.
- RAM: 256 bytes internal iRAM for fast data staging and stacking; 1KB on-chip xRAM for large amounts of data staging and DMA direct memory access.
- USB: embedded USB controller and USB transceiver, support USB-Host host mode and USB-Device device mode, support USB type-C master-slave detection, support USB 2.0 full speed

12Mbps or low speed 1.5Mbps. Support up to 64 bytes of data packets, built-in FIFO, support for DMA.

- Timer: 3 timers, T0 / T1 / T2 are standard MCS51 timers.
- Capture: Timer T2 extended to support 2-way signal capture.
- PWM: 2 sets of PWM output, PWM1 / PWM2 2 8-bit PWM output.
- UART: 2 asynchronous serial ports, both support higher communication baud rate, UART0 is a standard MCS51 serial port.
- SPI: SPI controller built-in FIFO, the clock frequency up to half the system clock frequency Fsys, serial data input and output to support simplex multiplexing, support Master / Slave master-slave mode.
- ADC: 4-channel 8-bit A / D analog-to-digital converter that supports voltage comparison.
- Touch-Key: 6-channel capacitance detection, supports up to 15 touch buttons, support for independent timer interrupt.
- GPIO: Supports up to 17 GPIO pins (including XI / XO and RST and USB signal pins).
- Interrupt: Support 14 groups of interrupt sources, including 6 groups of interrupts compatible with standard MCS51 (INT0, T0, INT1, T1, UART0, T2), and an extended group of 8 interrupts (SPI0, TKEY, USB, ADC, UART1, PWMX, GPIO, WDOG). GPIO interrupts can be selected from seven pins.
- Watch-Dog: 8-bit watchdog timer WDOG can be preset to support the timer interrupt.
- Reset: Supports 4 kinds of reset signal source, built-in power-on reset, software reset and watchdog overflow reset, optional pin external input reset.
- Clock: Built-in 24MHz clock source, can support external crystal through multiplexing GPIO pin.
- Power: Built-in 5V to 3.3V low dropout voltage regulator, supporting 5V or 3.3V or even 2.8V supply voltage. Support low-power sleep, support USB, UART0, UART1, SPI0 and some GPIO external wake-up.
- Chip built-in unique ID number.

3. Package



Package	Plastic body width		Pitch spacing		Packaging instructions	Order model
TSSOP-20	4.40mm	173mil	0.65mm	25mil	Thin 20-foot patch	CH554T
SOP-16	3.9mm	150mil	1.27mm	50mil	Standard 16 foot patch	CH554G
MSOP-10	3.0mm	118mil	0.50mm	19.7mil	Tiny 10-foot patch	CH554E
SOP-16	3.9mm	150mil	1.27mm	50mil	Standard 16 foot patch	CH553G

4. Pins

Package			Pin name	Other function names (Left function is preferred)	Other function description
TSSOP 20	SOP 16	MSOP 10			
19	15	9	VCC	VDD	Power input, need external 0.1uF power decoupling capacitor.
20	16	10	V33		Internal USB Power Regulator Output and Internal USB Power Input, When the power supply voltage is less than 3.6V connect VCC input external power supply,

					When the supply voltage is greater than 3.6V external 0.1uF power decoupling capacitor
18	14	8	GND	VSS	Common ground.
6	6	5	RST	RST/T2EX_/CAP2_	Underlined suffix pin is the same name without underscores pin mapping. RST pin built-in pull-down resistor; other GPIO default pull-up resistor. RST: External reset input. T2: Timer / Counter 2 external count input / clock output. T2EX: Timer / Counter 2 Overload / Capture Input. CAP1, CAP2: Timer / Counter 2 capture inputs 1,2. TIN0 ~ TIN5: 0 # ~ 5 # channel touch button capacitance detection input. AIN0 ~ AIN3: 0 # ~ 3 # channel ADC analog signal input. UCC1, UCC2: USB type-C bidirectional configuration channel. VBUS1, VBUS2: USB type-C bus voltage detection input. XI, XO: external crystal oscillator input, inverting output. RXD, TXD: UART0 serial data input, serial data output. SCS, MOSI, MISO, SCK: SPI0 interface, SCS is the chip select input, MOSI is the host output / slave input, MISO is the host input / slave output, SCK is the serial clock. PWM1, PWM2: PWM1 output, PWM2 output. RXD1, TXD1: UART1 serial data input, serial data output. INT0, INT1: External interrupt 0, External interrupt 1 input. T0, T1: Timer 0, Timer 1 external input. UDM, UDP: D-, D + signal terminal of a USB host or USB device. Note: P3.6 and P3.7 internal use V33 as I / O power supply, so the high level of its input and output only to V33 voltage does not support 5V
7	-	-	P1.0	T2/CAP1/TIN0	
8	9	-	P1.1	T2EX/CAP2/TIN1 /VBUS2/AIN0	
17	-	-	P1.2	XI/RXD_	
16	-	-	P1.3	XO/TXD_	
2	2	1	P1.4	T2_/CAP1_/SCS /TIN2/UCC1/AIN1	
3	3	2	P1.5	MOSI/PWM1/TIN3 / UCC2/AIN2	
4	4	3	P1.6	MISO/RXD1/TIN4	
5	5	4	P1.7	SCK/TXD1/TIN5	
10	8	-	P3.0	PWM1_/RXD	
9	7	-	P3.1	PWM2_/TXD	
1	1	-	P3.2	TXD1_/INT0 /VBUS1/AIN3	
11	10	-	P3.3	INT1	
12	11	-	P3.4	PWM2/RXD1_/T0	
13	-	-	P3.5	T1	
14	12	6	P3.6	UDP	
15	13	7	P3.7	UDM	

5. Special Function Registers (SFR)

The following abbreviations may be used in describing the registers in this manual:

Abbreviation	Description
RO	Indicates the type of access: read only
WO	Indicates the type of access: write only
RW	Indicates the type of access: read and write
H	Indicates a hexadecimal number
B	Indicates a binary number

5.1 SFR Introduction and Address Distribution

The CH554 is controlled by special function registers SFR, manages the device, and sets the operating mode.

The SFR occupies the 80h-FFh address range of the internal data memory space and can only be accessed by direct address mode instructions. Among them the address is x0h or x8h registers can be bit-based addressing, so that you can avoid access to a specific bit and modify the value of other bits; other address non-8 multiple registers can only be accessed by bytes.

Some SFRs write data only in safe mode and read-only states in non-secure mode, for example: GLOBAL_CFG, CLOCK_CFG, WAKE_CTRL.

Some SFRs have one or more aliases, for example: SPI0_CK_SE / SPI0_S_PRE, UDEV_CTRL / UHOST_CTRL, UEP1_CTRL / UH_SETUP, UEP2_CTRL / UH_RX_CTRL, UEP2_T_LEN / UH_EP_PID, UEP3_CTRL / UH_TX_CTRL, UEP3_T_LEN / UH_TX_LEN.

The partial address corresponds to multiple independent SFRs, for example: SAFE_MOD / CHIP_ID, ROM_CTRL / ROM_STATUS.

CH554 contains 8051 standard SFR registers, while adding other device control registers. Specific SFR see table below.

Table 5.1 Special Function Register Table

SFR	0, 8	1, 9	2, A	3, B	4, C	5, D	6, E	7, F
0xF8	SPI0_STAT	SPI0_DATA	SPI0_CTRL	SPI0_CK_SE SPI0_S_PRT	SPI0_SETUP		RESET_KEEP	WDOG_COUNT
0xF0	B							
0xE8	IE_EX	IP_EX	UEP4_1_MOD	UEP2_3_MOD UH_EP_MOD	UEP0_DMA_L	UEP0_DMA_H	UEP1_DMA_L	UEP1_DMA_H
0xE0	ACC	US_INT_EN	USB_CTRL	USB_DEV_AD	UEP2_DMA_L	UEP2_DMA_H	UEP3_DMA_L	UEP3_DMA_H

					UH_RX_DMA_L	UH_RX_DMA_H	UH_TX_DMA_L	UH_TX_DMA_H
0xD8	USB_INT_FG	USB_INT_ST	USB_MIS_ST	USB_RX_LEN	UEP0_CTRL	UEP0_T_LEN	UEP4_CTRL	UEP4_T_LEN
0xD0	PSW	UDEV_CTRL UHOST_CTRL	UEP1_CTRL UH_SETUP	UEP1_T_LEN	UEP2_CTRL UH_RX_CTRL	UEP2_T_LEN UH_EP_PID	UEP3_CTRL UH_TX_CTRL	UEP3_T_LEN UH_TX_LEN
0xC8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	T2CAP1L	T2CAP1H
0xC0	SCON1	SBUF1	SBAUD1	TKEY_CTRL	TKEY_DATL	TKEY_DATH	PIN_FUNC	GPIO_IE
0xB8	IP	CLOCK_CFG						
0xB0	P3	GLOBAL_CFG						
0xA8	IE	WAKE_CTRL						
0xA0	P2	SAFE_MOD CHIP_ID	XBUS_AUX					
0x98	SCON	SBUF	ADC_CFG	PWM_DATA2	PWM_DATA1	PWM_CTRL	PWM_CK_SE	ADC_DATA
0x90	P1	USB_C_CTRL	P1_MOD_OC	P1_DIR_PU			P3_MOD_OC	P3_DIR_PU
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	ROM_DATA_L	ROM_DATA_H
0x80	ADC_CTRL	SP	DPL	DPH	ROM_ADDR_L	ROM_ADDR_H	ROM_CTRL ROM_STATUS	PCON

Remark: (1), the red text represents bit-by-bit addressing; (2) The following is the corresponding description of the color box

0xXX	Register address
	SPI0 related register
	ADC related register
	Touch-Key related register
	USB related register
	Timer / Counter 2 Related Registers
	Port setting related register
	PWM1 or PWM2 related register
	UART1 related register
	Flash-ROM related register

5.2 SFR classification and reset value

[section omitted]

5.3 General 8051 Register

Table 5.3.1 General 8051 Register List

Name	Address	Description	Reset Value
B	F0h		00h
A, ACC	D0h		00h
PSW	D0h		00h
GLOBAL_CFG	B1h	Global Configuration Register (CH554 Bootloader Status)	20h
		Global Configuration Register (CH554 Application Status)	00h
		Global Configuration Register (CH553 Bootloader Status)	60h
		Global Configuration Register (CH553 Application Status)	40h
CHIP_ID	A1h	CH554 chip ID number (read only)	54h
		CH553 chip ID number (read only)	53h
SAFE_MOD	A1h	Safety Mode Control Register (Write Only)	00h
PCON	87h	Power Control Register (Power-on Reset)	10h
DPH	83h	Data address pointer high 8 bits	00h
DPL	82h	Data address pointer low 8 bits	00h
DPTR	82h	DPL and DPH make up 16 SFRs	0000h
SP	81h	Stack pointer	07h

B register (B):

Bit	Name	Access	Description	Reset Value
[7:0]	B	RW	Arithmetic operation registers, mainly used for multiplication and division operations, bit-addressable	00h

A Accumulator (A, ACC):

Bit	Name	Access	Description	Reset Value
[7:0]	AA/ACC	RW	Arithmetic operation accumulator, bit-addressable	00h

Program Status Register (PSW):

Bit	Name	Access	Description	Reset Value
7	CY	RW	Carry flag: When performing arithmetic and logic instructions, it is used to record the carry or borrow of the most significant bit. When the 8-bit addition is performed, the most significant bit will be set, otherwise it will be cleared. When 8-bit subtraction is performed , If borrow, the bit is set, otherwise cleared; logic instruction can set or clear this bit	0
6	AC	RW	Auxiliary carry flag: Record addition and subtraction operation, the low 4 to the high 4 carry or borrow, AC is set, otherwise cleared	0
5	F0	RW	Bit-addressable general purpose flag 0: User definable, software cleared or set	0
4	RS1	RW	Register bank select bit high	0
3	RS0	RW	Register bank select bit low	0
2	OV	RW	Overflow flag: Addition and subtraction operations, the result exceeds 8 binary numbers, OV is set to 1, the flag overflows, otherwise cleared	0
1	F1	RW	Bit-addressable general purpose flag 1: User-definable, software cleared or set	0
0	P	RO	Parity Flag: Records the parity of 1 in Accumulator A after the instruction is executed. If odd, 1 is set, P is set and if it is even, then 1 is cleared	0

The state of the processor is saved in the status register PSW and PSW supports bit-wise addressing. Status words include carry flag, auxiliary carry flag for BCD processing, parity flag, overflow flag, and RS0 and RS1 for working register bank selection. The area where the working register file is located can be accessed directly or indirectly.

Table 5.3.2 RS1 and RS0 working register bank selection table

RS1	RS0	Working register group
0	0	Group 0 (00h-07h)
0	1	Group 1 (08h-0Fh)
1	0	Group 2 (10h-17h)
1	1	Group 3 (18h-1Fh)

Table 5.1.3 operation of the flag (X indicates that the flag is related to the operation result)

Opcode	CY	OV	AC	Opcode	CY	OV	AC
ADD	X	X	X	**SETB C**	1		

ADDC	X	X	X	**CLR C**	0		
SUBB	X	X	X	**CPL C**	X		
MUL	0	X		**MOV C, bit**	X		
DIV	0	X		**ANL C, bit**	X		
DA A	X			**ANL C, /bit**	X		
RRC A	X			**ORL C, bit**	X		
RLC A	X			**ORL C, /bit**	X		
CJNE	X						

Data Address Pointer (DPTR):

Bit	Name	Access	Description	Reset Value
[7:0]	DPL	RW	Data pointer low byte	00h
[7:0]	DPH	RW	Data pointer high byte	00h

DPL and DPH form a 16-bit data pointer, DPTR, to access the xRAM data memory or program memory. The actual DPTR corresponds to two sets of physical 16-bit data pointers, DPTR0 and DPTR1, dynamically selected by the DPS in XBUS_AUX.

Stack pointer (SP):

Bit	Name	Access	Description	Reset Value
[7:0]	SP	RW	Stack pointer, mainly used for program calls and interrupt calls and data in and out of the stack	07h

Stack specific functions: protection of the endpoint and the protection of the site, according to the principles of management out. When the stack pointer SP automatically increase 1, save the data or breakpoint information; when the stack pointer to point SP data unit, SP pointer automatically reduced by 1. The initial value of SP after reset is 07h, and the corresponding default stack storage starts from 08h.

5.4 Special Register

Global Configuration Register (GLOBAL_CFG), writable only in safe mode:

Bit	Name	Access	Description	Reset Value
[7:6]	Reserved	RO	For CH554, a fixed value of 00	00b
[7:6]	Reserved	RO	For CH553, a fixed value of 01	01b
5	bBOOT_LOAD	RO	Boot loader status bit, used to distinguish ISP boot program status or application status: Set at power-on	1

			and cleared at software reset. For a chip with an ISP bootloader, this bit is 1 to indicate that the software has not been reset before, and is usually the ISP bootloader running after power-on. A 0 indicates that a software reset has occurred and is usually the application state	
4	bSW_RESET	RW	Software reset control bit: Set to cause a software reset, the hardware automatically cleared	0
3	bCODE_WE	RW	Flash-ROM and DataFlash write enable bit: This bit is 0 write-protected; a Flash-ROM and Data can be rewritten	0
2	bDATA_WE	RW	Flash-ROM DataFlash area write enable bit: This bit is 0 then write protection; a DataFlash area can be rewritten	0
1	bLDO3V3_OFF	RW	USB Power Regulator LDO Disable Control: This bit is 0 to allow LDO, can generate 3.3V voltage from 5V power supply for USB and internal clock oscillator; An LDO of 1 disables the V33 pin and must input an external 3.3V power supply	0
0	bWDOG_EN	RW	Watchdog reset enable bit: This bit is 0 Watchdog is only used as a timer; this bit is 1 to allow watchdog reset when timing overflow occurs	0

Chip identification code ID (CHIP_ID):

Bit	**Name**	**Access**	**Description**	**Reset Value**
[7:0]	CHIP_ID	RO	For CH554, a fixed value of 54h, used to identify the chip	54h
[7:0]	CHIP_ID	RO	For CH553, a fixed value of 53h, used to identify the chip	53h

Safety Mode Control Register (SAFE_MOD):

Bit	**Name**	**Access**	**Description**	**Reset Value**
[7:0]	SAFE_MOD	WO	Used to enter or terminate safe mode	00hh

Some SFRs write data only in safe mode and always read-only in non-secure mode. Step into safe mode:

1. Write 55h to this register;
2. Then write AAh to this register;
3. After that, about 13 to 23 system clock cycles are in safe mode, and one or more safety SFRs or normal SFRs can be overwritten during the valid period.

4. Beyond the validity of the automatic termination of safe mode;
5. Additionally, writing any further value to this register can terminate Safe Mode early.

6. Memory Structure

6.1 memory space

CH554 addressing space is divided into program storage space, internal data storage space, external data storage space.

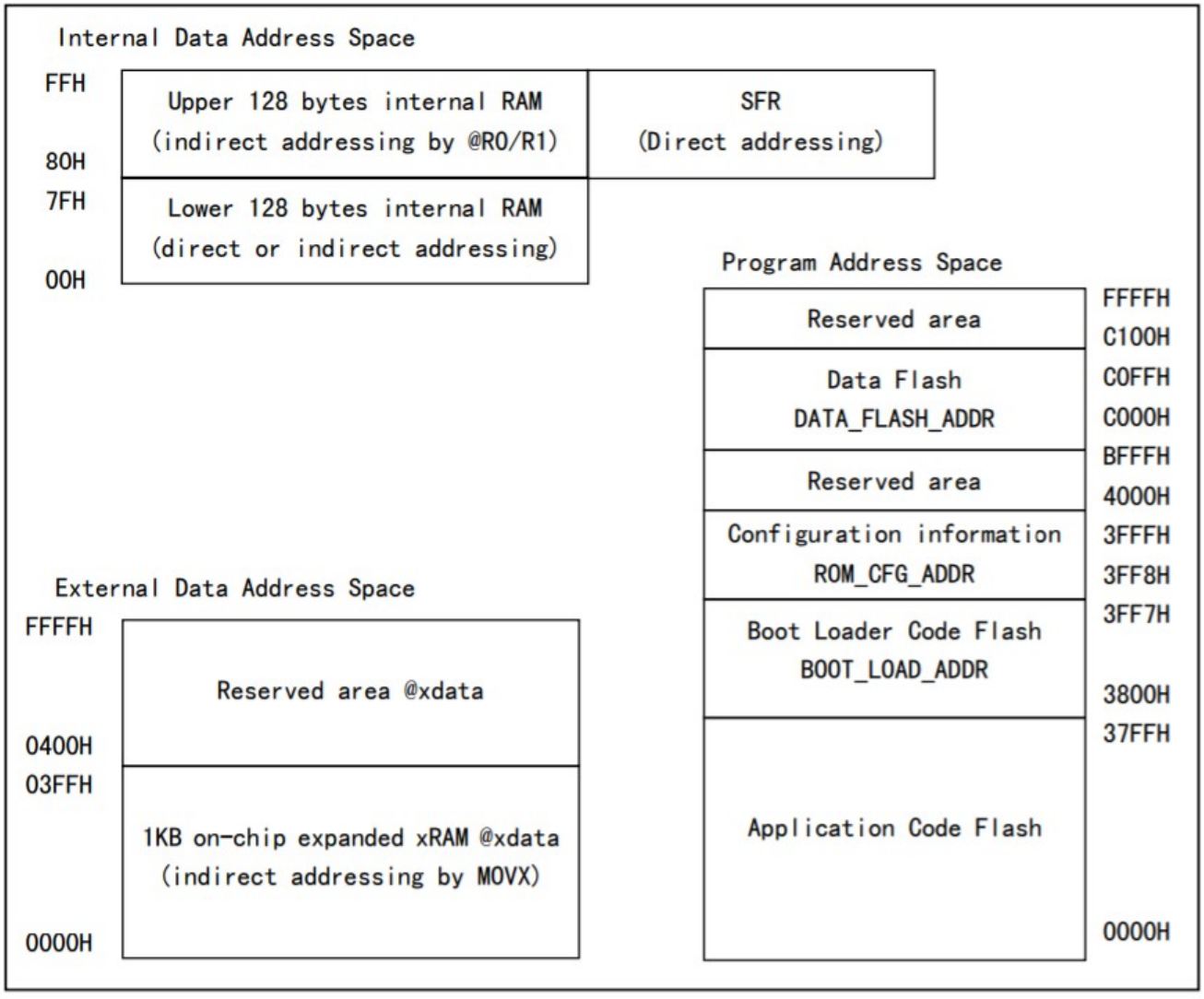


Figure 6.1 Memory Block Diagram

6.2 Program Address Space

The total program storage space is 64KB, as shown in Figure 6.1, of which 16KB is for ROM, including the Code Flash area where the instruction code is stored and the configuration information Configuration Information area.

Code Flash includes application code for low address areas and boot code for high address areas. You can also combine these two areas to hold a single application code.

For CH553, the Code Flash application code area is only 10KB.

The ROM is an iFlash ™ process that can be programmed about 200 times with a 5V supply for a finished blank ROM package.

The Data Flash address range is from C000h to C0FFH (only the address is valid, actually there is one memory cell every other byte), only supports single-byte (8-bit) read and write operations, and the data remains unchanged after the chip is powered off. Data Flash supports about 10,000 erasing and writing. It is recommended to use equalization. It is forbidden to erase more than 10K times for the same memory unit. If there are more erasing times, it is recommended to use CH559 or CH548/9.

Configuration Information Configuration Information includes four 16-bit data at 3FF8H to 3FFFH addresses, the last three groups are read-only and provide the chip ID. The configuration data at the 3FF8H address is set by the programmer as needed, refer to Table 6.2.

Table 6.2 flash-ROM configuration information description

Bit	**Name**	**Description**	**Suggested Value**
15	Code_Protect	Flash-ROM code and data protection mode: 0 - programmer is prohibited to read, the program is confidential; 1 - allowed to read	0/1
14	No_Boot_Load	Enable BootLoader Boot Code Boot Mode: 0 - application start from 0000h address; 1- Boot from 3800h address started	1
13	En_Long_Reset	Enable additional delay reset during power-on reset: 0- standard short reset; 1-wide reset, an additional 44mS reset time	0
12	En_RST_RESET	Enable RST pin as manual reset input pin: 0-disabled; 1-enabled RST	0
[11:10]	Reserved	(Programmed by the programmer automatically set to 00)	00
9	Must_1	(Programmed by the programmer automatically set to 1)	1
8	Must_0	(Programmed by the programmer automatically set to 0)	0

[7:0]	All_1	(Programmed by the programmer automatically set to FFh)	FFh

6.3 Data Address Space

The total internal data space is 256 bytes, as shown in Figure 6.1, all of which are used for SFR and iRAM, where iRAM is used for stacking and fast data staging and can be subdivided into working registers R0-R7, bit variables bdata, bytes Variables data, idata and so on.

External data storage space a total of 64KB, as shown in Figure 6.1, part of the expansion for 1KB chip xRAM, the remaining reserved area.

For CH553, on-chip expansion of xRAM is only 512 bytes.

6.4 Flash-ROM register

[Section omitted]

6.5 flash-ROM steps

[Section omitted]

6.6 Board Programming and ISP Download

When the configuration information Code_Protect = 1, the code in the flash-ROM and the data in Data Flash of the CH554 chip can be read and written by the external programmer through the synchronous serial interface. When the configuration information Code_Protect = 0, the code in the flash-ROM And Data Flash Data is protected, can not be read out, but can be erased, erase and then re-unlock the code protection.

When the CH554 chip is preset BootLoader boot program, CH554 can support USB or asynchronous serial port and other ISP download methods to load the application; but in the absence of a boot program, CH554 can only be written by an external programmer boot loader Or application. In order to support board programming, you must temporarily use the 5V supply voltage, and the circuit needs to reserve four connection pins between the CH554 and the programmer, the minimum necessary connection pin is three: P1.4, P1.6, P1.7.

Table 6.6.1 Connection Pin with Programmer

Pin	**GPIO**	**Description**
RST	RST	Reset control pin in programming state, high level allows programming
SCS	P1.4	Chip Select Input Pin (Required) in Programming State, Default High, Active Low
SCK	P1.7	Clock input pin in programming state (required)

MISO	P1.6	Data output pin in programming state (required)

Note: The 5V supply voltage must be used temporarily either in board programming or via serial or USB download.

6.7 Chip Unique ID Number

Each microcontroller has a unique ID number from the factory, which is the chip identification number. The ID data is 5 bytes and is stored in the address 3FFAH to 3FFFH in the configuration information Configuration Information area. Of which 3FFBH address for the retention unit, 3FFCH and 3FFEH address of the two 16-bit data and 3FFAH address 8-bit data into 40-bit chip ID data.

Program space address	**ID data description**
3FFAh、3FFBh	ID end of the word data, followed by the 40-bit ID number of the highest byte, reserved bytes
3FFCh、3FFDh	ID first word data, followed by the ID number of the lowest byte, second low byte
3FFEh、3FFFh	ID sub-word data, followed by the ID number of the next high byte, high byte

The ID data can be obtained by reading Code Flash. ID number can be used with the download tool for the target program to be encrypted, the general application, just use the first 32-bit ID number, you can ignore 3FFAH address 8-bit data.

7. Power Management, Sleep and Reset

7.1 External power input

CH554 chip built-in 5V to 3.3V low dropout voltage regulator supports external 5V or 3.3V or even 2.8V supply voltage input, the two power supply voltage input mode refer to the table below.

External supply voltage	**VCC pin voltage: external voltage 3V ~ 5V**	**V33 pin voltage: 3.3V internal voltage**
3.3V or 3V Including less than 3.6V	Input an external 3.3V voltage to the voltage regulator must be connected to ground not less than 0.1uF decoupling capacitor	3.3V external input as the internal work of the power supply must be connected to not less than 0.1uF decoupling capacitor
5V Including more than 3.6V	Input external 5V voltage to the voltage regulator, must be connected to ground not less than 0.1uF decoupling capacitor	3.3V internal voltage regulator output and 3.3V internal power supply input, must be connected to ground not less than 0.1uF decoupling capacitor

After power on or system reset, CH554 is running by default. In the premise of the performance to meet the requirements, properly reduce the system frequency can reduce power consumption during operation. When the CH554 does not need to run at all, you can set the PD in PCON to sleep state, and you can choose external wake-up through USB, UART0, UART1, SPI0 and some GPIOs in sleep mode.

7.2 Power and Sleep Control Registers

Table 7.2.1 Power and Sleep Control Registers List

Name	Address	Description	Reset Value
WDOG_COUNT	FFh	Watchdog counter register	00h
RESET_KEEP	FEh	Reset holding register	00h
WAKE_CTRL	A9h	Sleep wake-up control register	00h
PCON	87h	Power Control Register	10h

Watchdog Count Register (WDOG_COUNT):

Bit	Name	Access	Description	Reset Value
[7:0]	WDOG_COUNT	RW	Watchdog current count, overflow over 0FFh 00h, over overflow automatically set interrupt flag bWDOG_IF_TO is 1	00h

Reset hold register (RESET_KEEP):

Bit	Name	Access	Description	Reset Value
[7:0]	RESET_KEEP	RW	Reset holding register, the value can be artificially modified, in addition to power-on reset can be cleared, any other reset does not affect the value	00h

Sleep Wakeup Control Register (WAKE_CTRL), writable only in Safe Mode:

Bit	Name	Access	Description	Reset Value
7	bWAK_BY_USB	RW	USB event wake-up enable, this bit is 0 to disable wake-up	0
6	bWAK_RXD1_LO	RW	UART1 receive input low wake-up enable, this bit is 0 to disable wake-up. Select RXD1 or RXD1_ pin according to bUART1_PIN_X = 0/1	0

5	bWAK_P1_5_LO	RW	P1.5 low wake-up enable, 0 wake-up prohibited	0
4	bWAK_P1_4_LO	RW	P1.4 low wake-up enable, 0 wake-up prohibited	0
3	bWAK_P1_3_LO	RW	P1.3 low wake-up enable, 0 wake-up prohibited	0
2	bWAK_RST_HI	RW	RST high wake-up enable, disable wake-up from 0.	0
1	bWAK_P3_2E_3L	RW	P3.2 edge change and P3.3 wake-up enable low, wake-up from 0 to disable	0
0	bWAK_RXD0_LO	RW	UART0 receive input low wake-up enable, disable wake-up from 0. Select the RXD0 or RXD0_ pin according to bUART0_PIN_X = 0/1	0

Power Control Register (PCON):

Bit	**Name**	**Access**	**Description**	**Reset Value**
7	SMOD	RW	When using UART1 to generate UART0 baud rate, UART0 mode 1, 2 and 3 communication baud rate is selected: 0 - slow mode; 1 - fast mode	0
6	Reserved	RO	Reserved	0
5	bRST_FLAG1	RO	The chip reset flag high recently	0
4	bRST_FLAG0	RO	The chip reset flag low recently	0
3	GF1	RW	General flags bit 1: Users can define their own, software can be cleared or set	0
2	GF0	RW	General flags 0: users can define their own, software can be cleared or set	0
1	PD	RW	Sleep mode is enabled, set to sleep after wake-up hardware automatically cleared	0
0	Reserved	RO	Reserved	0

Table 7.2.2 Description of the most recent reset flag of the chip

bRST_FLAG1	**bRST_FLAG0**	**Reset flag description**
0	0	Software Reset, Source: bSW_RESET = 1 and (bBOOT_LOAD = 0 or bWDOG_EN = 1)
0	1	Power on reset, source: VCC pin voltage is below detection level
1	0	Watchdog reset, source: bWDOG_EN = 1 and watchdog timeout expired
1	1	External Pin Manual Reset Source: En_RST_RESET = 1 and RST Input High

7.3 Reset control

CH554 has 4 reset sources: power-on reset, external reset, software reset, watchdog reset, the latter three belong to the thermal reset.

7.3.1 Power-on reset

Power-on reset POR by the on-chip voltage detection circuit. The POR circuit continuously monitors the supply voltage of the VCC pin. A power-on reset is generated when the voltage level is lower than the detection level Vpot, and the hardware automatically delays Tpor to maintain the reset state. The CH554 operates after the delay time expires.

Only the power-on reset to make CH554 reload configuration information and reset RESET_KEEP, other thermal reset does not affect.

7.3.2 External reset

The external reset is generated by the high level applied to the RST pin. The reset process is triggered when the configuration information En_RST_RESET is 1 and the high level on the RST pin lasts longer than Trst. When the external high signal is removed, the hardware automatically Trdl delayed to maintain the reset state, after the end of the delay CH554 0 address from the beginning.

7.3.3 Software reset

The CH554 supports internal software reset to proactively reset the CPU state and rerun without external intervention. Set the global configuration register bSW_RESET in GLOBAL_CFG to 1 to reset the software and automatically delay Trdl to maintain the reset state. After the delay expires, CH554 starts from address 0 and the bSW_RESET bit is automatically cleared by hardware.

When bSW_RESET is set, bRST_FLAG1 / 0 will indicate a software reset after reset if bBOOT_LOAD = 0 or bWDOG_EN = 1; bRST_FLAG1 / 0 will not be generated if bBOOT_LOAD = 1 and bWDOG_EN = 0 when bSW_RESET is set Reset flag, but to keep the reset flag unchanged.

For the chip with ISP boot program, after the power is reset, the bootloader should be run first. The program will reset the chip according to the software needed to switch to the application state. This software reset only causes bBOOT_LOAD to be cleared and does not affect the state of bRST_FLAG1 / 0 (Due to bBOOT_LOAD = 1 prior to reset), bRST_FLAG1 / 0 still indicates the power-on reset state when switching to the application state.

7.3.4 Watchdog reset

Watchdog reset generated by watchdog timer timeout. The watchdog timer is an 8-bit counter whose clock frequency is the system clock frequency of Fsys / 65536. An overflow signal is generated when 0FFh transitions to 00h.

The watchdog timer overflow signal will trigger the interrupt flag bWDOG_IF_TO to 1, which is automatically cleared when WDOG_COUNT is reloaded or when it enters the corresponding interrupt service routine.

By writing a different count initial value to WDOG_COUNT, a different timing period Twdc is achieved. Watchdog timing period Twdc when writing 00h is about 2.8 seconds at 6MHz frequency, and about 1.4 seconds when writing 80h. Halved at 12MHz clock speed.

If the watchdog timer overflow bWDOG_EN = 1, then the watchdog reset, and automatically delay Trdl to maintain the reset state, after the end of the delay CH554 0 address from the beginning.

To avoid being reset by watchdog when bWDOG_EN = 1, WDOG_COUNT must be reset in time to avoid overflow.

8 System Clock

8.1 Clock Block Diagram

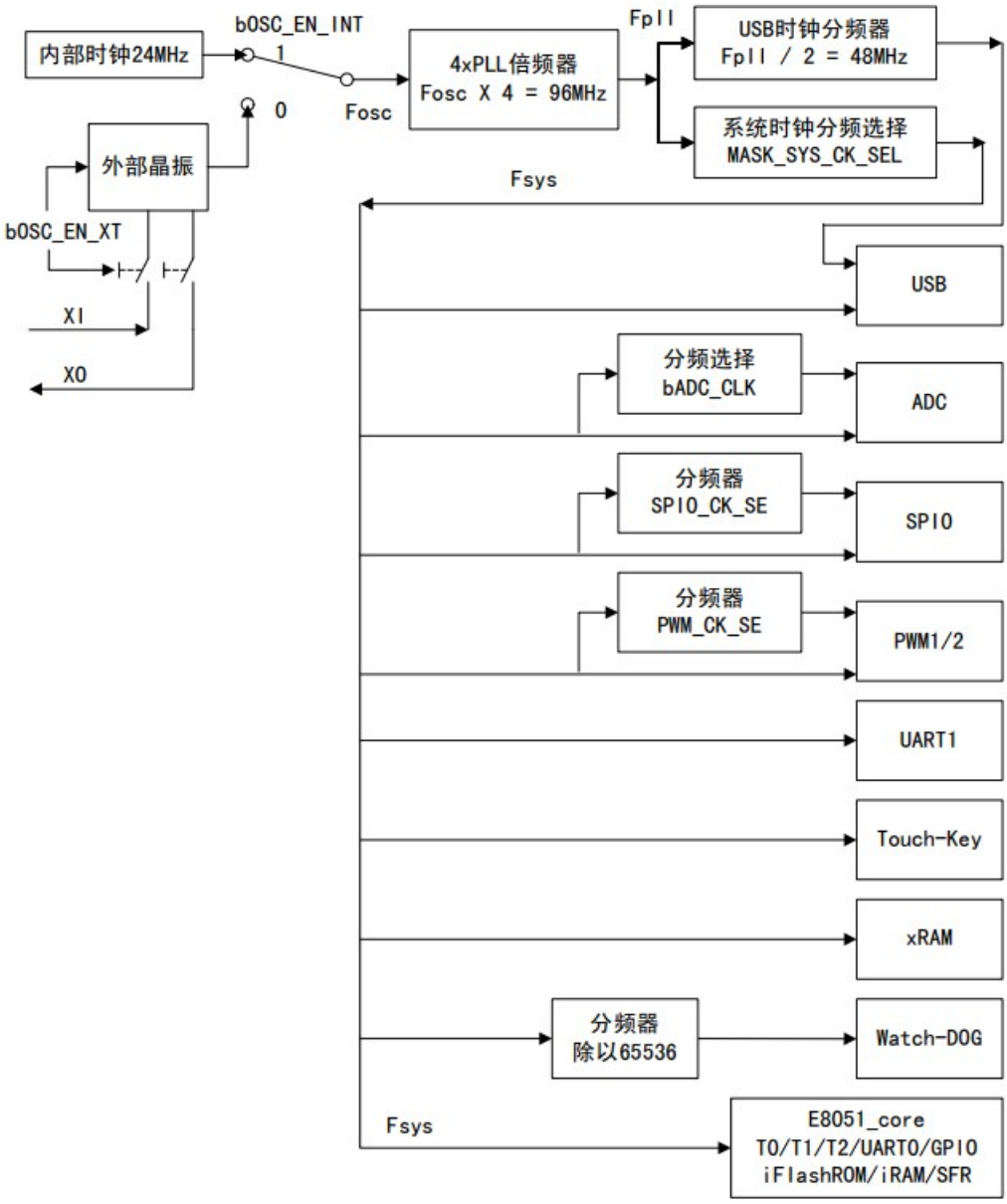


Figure 8.1.1 Clock System and Structure

After the internal clock or the external clock is selected as the original clock Fosc, the Fpll high-frequency clock is generated after multiplying the 4xPLL frequency. Finally, the system clock Fsys and the clock Fusb4x of the USB module are obtained through two sets of frequency divider respectively. The system clock Fsys is provided directly to the various modules of the CH554.

8.2 Register Description

Table 8.2.1 Clock Control Register List

Name	Address	Description	Reset Value
CLOCK_CFG	B9h	System clock configuration register	83h

System Clock Configuration Register (CLOCK_CFG), writable only in safe mode:

Bit	Name	Access	Description	Reset Value
7	bOSC_EN_INT	RW	The internal clock oscillator is enabled. When this bit is 1, the internal clock oscillator is enabled and the internal clock is selected. When this bit is '0', the internal clock oscillator is off and the external crystal oscillator is used to provide the clock	1
6	bOSC_EN_XT	RW	This bit is set to 1 by an external crystal oscillator. The P1.2 / P1.3 pins function as XI / XO and enable the oscillator. An external crystal or ceramic oscillator is required between XI and XO. This bit is set to 0 External oscillator	0
5	bWDOG_IF_TO	RO	Watchdog timer interrupt flag, the bit is 1 indicates an interrupt, triggered by the timer overflow signal; the bit is 0 means no interruption. This bit is cleared automatically when the watchdog counter WDOG_COUNT is reloaded or after entering the corresponding interrupt service routine	0
4	bROM_CLK_FAST	RW	flash-ROM reference clock frequency selection: 0 - normal (if Fosc> = 16MHz); 1- accelerated (if Fosc <16MHz)	0
3	bRST	RO	RST pin status input bit	0
[2:0]	MASK_SYS_CK_SEL	RW	System clock frequency selection, refer to table 8.2.2 below	011b

Table 8.2.2 system frequency selection table

MASK_SYS_CK_SEL	System Frequency Fsys	Fxt relationship with the crystal frequency	Fsys when Fosc = 24 MHz
000	Fpll / 512	Fxt / 128	187.5KHz
001	Fpll / 128	Fxt / 32	750KHz
010	Fpll / 32	Fxt / 8	3MHz
011	Fpll / 16	Fxt / 4	6MHz
100	Fpll / 8	Fxt / 2	12MHz
101	Fpll / 6	Fxt / 1.5	16MHz
110	Fpll / 4	Fxt / 1	24MHz
111	Fpll / 3	Fxt / 0.75	Reserved, disabled

8.3 Clock Configuration

CH554 chip power on the default use of internal clock, the internal clock frequency is 24MHz. The internal clock or the external crystal oscillator clock can be selected by CLOCK_CFG, and the X1 and XO pins can be used as P1.2 and P1.3 normal I / O ports if the external crystal oscillator is turned off. If an external crystal oscillator is used to provide the clock, the crystal should be bridged between the XI and XO pins, and the X1 and XO pins should be connected to GND for the oscillation capacitor, respectively. If a clock signal is input directly from the outside, Pin input, XO pin left open.

The original clock frequency Fosc = bOSC_EN_INT? 24MHz: Fxt

PLL Frequency Fpll = Fosc * 4 = 96MHz

USB clock frequency Fusb4x = Fpll / 2 = 48MHz

System frequency Fsys reference table 8.2.2 obtained by the Fpll frequency

After reset, Fosc = 24MHz, Fpll = 96MHz, Fusb4x = 48MHz, Fsys = 6MHz.

Switch to the external crystal oscillator to provide the clock as follows:

1. Enter safe mode, step one SAFE_MOD = 55h; step two SAFE_MOD = AAh;
2. Set bOSC_EN_XT in CLOCK_CFG to 1 with "bit or" operation, and leave the other bits unchanged to enable the crystal oscillator;
3. a few milliseconds delay, usually 5mS ~ 10mS, waiting for the crystal oscillator stable;
4. Enter safe mode again, step one SAFE_MOD = 55h; step two SAFE_MOD = AAh;
5. Clear "bOSC_EN_INT" in CLOCK_CFG with "and" and leave the other bits unchanged to switch to the external clock;
6. Turn off safety mode, write any value to SAFE_MOD and terminate safety mode prematurely.

Modify the system frequency steps are as follows:

1. Enter safe mode, step one SAFE_MOD = 55h; step two SAFE_MOD = AAh;
2. Write a new value to CLOCK_CFG;
3. Turn off safety mode, write any value to SAFE_MOD, and terminate safety mode ahead of time.

Notes:

1. If the USB module is used, the Fusb4x must be 48MHz. When using full-speed USB, the system clock speed is not lower than 6MHz. When using low-speed USB, the system clock speed is not lower than 1.5MHz.
2. Preferentially use a lower system clock frequency, Fsys, to reduce system dynamic power consumption and widen the operating temperature range.

3. The internal clock oscillator is powered by V33, so V33 voltage changes, especially the low voltage, affect the internal clock frequency.

9. Interrupts

The CH554 chip supports 14 interrupt sources including 6 groups of interrupts compatible with standard MCS51: INT0, T0, INT1, T1, UART0, T2 and extended 8 groups of interrupts: SPI0, TKEY, USB, ADC, UART1, PWMX, GPIO, WDOG, among them GPIO interrupts can choose from 7 I / O pins.

9.1 Register Description

Table 9.1.1 Interrupt vector table

Source	Address	Number	Description	Default Priority
INT_NO_INT0	0x0003	0	External interrupt 0	High priority ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ Low priority
INT_NO_TMR0	0x000B	1	Timer 0 interrupt	
INT_NO_INT1	0x0013	2	External interrupt 1	
INT_NO_TMR1	0x001B	3	Timer 1 interrupt	
INT_NO_UART0	0x0023	4	UART0 interrupt	
INT_NO_TMR2	0x002B	5	Timer 2 interrupt	
INT_NO_SPI0	0x0033	6	SPI0 interrupt	
INT_NO_TKEY	0x003B	7	Touch-key timer interrupt	
INT_NO_USB	0x0043	8	USB interrupt	
INT_NO_ADC	0x004B	9	ADC interrupt	
INT_NO_UART1	0x0053	10	UART1 interupt	
INT_NO_PWMX	0x005B	11	PWM1 / PWM2 interrupt	
INT_NO_GPIO	0x0063	12	GPIO interrupt	
INT_NO_WDOG	0x006B	13	Watchdog timer interrupt	

Table 9.1.2 Interrupt Related Registers List

Name	Address	Description	Reset Value
IP_EX	E9h	Extended interrupt priority control register	00h
IE_EX	E8h	Extended interrupt enable register	00h
GPIO_IE	C7h	GPIO interrupt enable register	00h
IP	B8h	Interrupt priority control register	00h
IE	A8h	Interrupt enable register	00h

Interrupt Enable Register (IE):

Bit	Name	Access	Description	Reset Value
7	EA	RW	Global interrupt enable control bit, this bit is 1 and E_DIS is 0 to allow interrupt; this bit is 0 to mask all interrupt requests	0
6	E_DIS	RW	The global interrupt disable control bit, which bit masks all interrupt requests; this bit is 0 and an EA of 1 allows interrupts. This bit is normally used to temporarily disable interrupts during flash-ROM operations	0
5	ET2	RW	Timer 2 interrupt enable bit, this bit is 1 to allow T2 interrupt; 0 mask	0
4	ES	RW	Asynchronous serial 0 interrupt enable bit, this bit is 1 to allow UART0 interrupt; 0 mask	0
3	ET1	RW	Timer 1 interrupt enable bit, this bit is 1 to allow T1 interrupt; 0 mask	0
2	EX1	RW	External interrupt 1 enable bit, this bit is 1 INT1 interrupt is enabled; 0 is masked	0
1	ET0	RW	Timer 0 interrupt enable bit, this bit is 1 to allow T0 interrupt; 0 mask	0
0	EX0	RW	External interrupt 0 enable bit, this bit is 1 to allow INT0 interrupt; 0 mask	0

Extended Interrupt Enable Register (IE_EX):

Bit	Name	Access	Description	Reset Value
7	IE_WDOG	RW	Watchdog timer interrupt enable bit, this bit is 1 to allow WDOG interrupt; 0 mask	0
6	IE_GPIO	RW	GPIO Interrupt Enable bit, this bit is 1 to enable the interrupt enabled in GPIO_IE; 0 to mask all interrupts in GPIO_IE	0
5	IE_PWMX	RW	PWM1 / PWM2 interrupt enable bit, this bit is 1 to enable PWM1 / 2 interrupt;	0
4	IE_UART1	RW	Asynchronous serial 1 interrupt enable bit, this bit is 1 to allow UART1 interrupt; 0 mask	0
3	IE_ADC	RW	ADC Analog-to-Digital Interrupt Enable bit, this bit is 1 to allow ADC interrupt; 0 mask	0
2	IE_USB	RW	USB interrupt enable bit, this bit is 1 to allow USB interrupt; 0 mask	0

1	IE_TKEY	RW	Touch the Key Timer Interrupt Enable bit, this bit is 1 to allow timer interrupt; 0 mask	0
0	IE_SPI0	RW	SPI0 interrupt enable bit, this bit is 1 to allow SPI0 interrupt; 0 mask	0

GPIO Interrupt Enable Register (GPIO_IE):

Bit	**Name**	**Access**	**Description**	**Reset Value**
7	bIE_IO_EDGE	RW	GPIO edge interrupt mode enable: This bit is 0 to select the interrupt mode. When the GPIO pin is valid, bIO_INT_ACT is 1 and interrupts are always requested. When the GPIO input is inactive, bIO_INT_ACT is 0 and the interrupt request is canceled. This bit is set to 1 to select the edge interrupt mode. The GPIO pin will generate an interrupt flag, bIO_INT_ACT, and request an interrupt when it enters a valid edge. The interrupt flag can not be cleared by software. The interrupt flag can only be cleared during reset or interrupt mode or by entering the corresponding interrupt service routine Be automatically cleared	0
6	bIE_RXD1_LO	RW	This bit enables UART1 receive pin interrupts (active low level, falling edge mode); this bit is disabled. Select the RXD1 or RXD1_ pin according to bUART1_PIN_X = 0/1	0
5	bIE_P1_5_LO	RW	This bit is set to 1 to enable the P1.5 interrupt (active low in edge mode, falling edge in edge mode); this bit is set to '0'	0
4	bIE_P1_4_LO	RW	This bit is set to 1 to enable the P1.4 interrupt (active low in edge mode, falling edge in edge mode); this bit is set to '0'	0
3	bIE_P1_3_LO	RW	This bit is set to 1 to enable the P1.3 interrupt (active low in edge mode, falling edge in edge mode); this bit is set to '0'	0
2	bIE_RST_HI	RW	This bit is set to 1 to enable the RST interrupt (active high in edge mode, valid on rising edge); this bit is set to '0'	0
1	bIE_P3_1_LO	RW	This bit is set to 1 to enable the P3.1 interrupt (active low level mode, falling edge mode only); this bit is set to '0'	0
0	bIE_RXD0_LO	RW	This bit enables UART0 receive pin interrupts (level mode active low, falling edge mode enabled); this bit	0

			is disabled. Select the RXD0 or RXD0_ pin according to bUART0_PIN_X = 0/1	

Interrupt Priority Control Register (IP):

Bit	Name	Access	Description	Reset Value
7	PH_FLAG	RW	High-priority interrupt is in progress	0
6	PL_FLAG	RW	Low priority interrupt is in progress	0
5	PT2	RW	Timer 2 interrupt priority control bit	0
4	PS	RW	UART0 interrupt priority control bit	0
3	PT1	RW	Timer 1 interrupt priority control bit	0
2	PX1	RW	External interrupt 1 interrupt priority control bit	0
1	PT0	RW	Timer 0 interrupt priority control bit	0
0	PX0	RW	External interrupt 0 interrupt priority control bit	0

Extended Interrupt Priority Control Register (IP_EX):

Bit	Name	Access	Description	Reset Value
7	bIP_LEVEL	RW	The current interrupt nesting level flag, the bit is 0 no interrupt or nesting level 2 interrupt; the bit is 1 that the current level of 1 nesting interrupt	0
6	bIP_GPIO	RW	GPIO interrupt priority control bit	0
5	bIP_PWMX	RW	PWM1 / PWM2 interrupt priority control bit	0
4	bIP_UART1	RW	UART1 interrupt priority control bit	0
3	bIP_ADC	RW	ADC interrupt priority control bit	0
2	bIP_USB	RW	USB interrupt priority control bit	0
1	bIP_TKEY	RW	Touch the key timer interrupt priority control bit	0
0	bIP_SPI0	RW	SPI0 interrupt priority control bit	0

The IP and IP_EX registers are used to set the interrupt priority. If a bit is set, the corresponding interrupt source is set to high priority. If a bit is clear, the corresponding interrupt source is set to low priority . For peer interrupt sources, the system has the default priority order. The default priority order is shown in Table 9.1.1. The combination of PH_FLAG and PL_FLAG indicates the priority of the current interrupt.

Table 9.1.3 Current Interrupt Priority Status Indication

PH_FLAG	PL_FLAG	Current interrupt priority status
0	0	No interruption at this time
0	1	Low priority interrupt is currently executing
1	0	High priority interrupt is currently executing
1	1	Unexpected status, unknown error

10. I/O Ports

10.1 Introduction to GPIO

The CH554 provides up to 17 I / O pins and some pins have alternate functions. Among them, the port P1 and P3 of the input and output can be bit-based addressing. Port P2 is an internal port that is only used to select xRAM pages for MOVX access with R0 or R1.

If the pin is not configured as an alternate function, the default is the general purpose I / O pin status. When used as general-purpose digital I / O, all I / O ports have true Read-Modify-Write functions and support SETB or CLR alphanumeric operation instructions to independently change the orientation or port level of certain pins.

10.2 GPIO register

All registers and bits in this section are expressed in a common format: lower case "n" indicates port number (n = 1 or 3) and lower case "x" indicates bit serial number (x = 0,1,2,3, 4,5,6,7).

Name	Address	Description	Reset Value
P1	90h	P1 port input output register	ffh
P1_MOD_OC	92h	P1 port output mode register	ffh
P1_DIR_PU	93h	P1 port direction control and pull-up enable register	ffh
P2	A0h	P2 port output register	ffh
P3	B0h	P3 port input and output registers	ffh
P3_MOD_OC	96h	P3 port output mode register	ffh
P3_DIR_PU	97h	P3 port direction control and pull-up enable register	ffh
PIN_FUNC	C6h	Pin Function Selection Register	80h
XBUS_AUX	A2h	Bus Auxiliary Setup Register	00h

Pn port input / output register (Pn):

Bit	Name	Access	Description	Reset Value
[7:0]	Pn.0～Pn.7	RW	Pn.x pin status input and data output bits can be bit-addressed	ffh

Pn port output mode register (Pn_MOD_OC):

Bit	Name	Access	Description	Reset Value
[7:0]	Pn_MOD_OC	RW	Pn.x pin output mode setting: 0-push-pull output; 1-open drain output	ffh

Pn port direction control and pull-up enable register (Pn_DIR_PU):

Bit	Name	Access	Description	Reset Value
[7:0]	Pn_DIR_PU	RW	Pn.x pin direction control in push-pull output mode: 0-input; 1-output; Pn.x pin pull-up resistor enabled in open-drain output mode Control: 0 - Pull-up resistor disabled; 1 - Pull-up resistor enabled	ffh

The Pn port configuration is implemented by a combination of Pn_MOD_OC [x] and Pn_DIR_PU [x] as follows.

Table 10.2.2 Port Configuration Register Combination

Pn_MOD_OC	Pn_DIR_PU	Description
0	0	High-impedance input mode, there is no pull-up resistor on the pin
0	1	Push-pull output mode, with symmetrical drive capability, can output or absorb large current
1	0	Open drain output, high impedance input, no pull-up resistor on pin
1	1	Bidirectional mode (standard 8051), open-drain output, support for input, pull-up resistor on pin, automatically drives 2 clock cycles high to accelerate conversion when output goes low from low

P1 and P3 ports support pure input or push-pull output and quasi-bidirectional modes. Each pin has an internal pull-up resistor that is freely controllable, as well as a protection diode connected to VCC and GND.

Figure 10.2.1 is an equivalent schematic of the P1 pin's P1.x pin. After removing AIN, it can be applied to P3 port. The figure after VCC changed to V33 for P3.6 and P3.7, that is, P3.6 and P3.7 pull-up or input or output high only to V33 voltage.

P3.6 and P3.7 Select a standard pull-up resistor (up to V33), a 15KΩ pull-down resistor or a 1.5KΩ strong pull-up resistor (to V33) for one of the pins. The standard pull-up resistor is only active in bIOB_IO_EN = 0 ie GPIO mode and is controlled by bit 7, bit 6 of P3_DIR_PU; the pull-down resistor is controlled by bUD_PD_DIS or bUH_PD_DIS at bUC_RESET_SIE = 0 regardless of bUSB_IO_EN; the 1.5KΩ pull- Resistor, controlled by bUC_DEV_PU_EN when bUC_RESET_SIE = 0, is independent of bUSB_IO_EN.

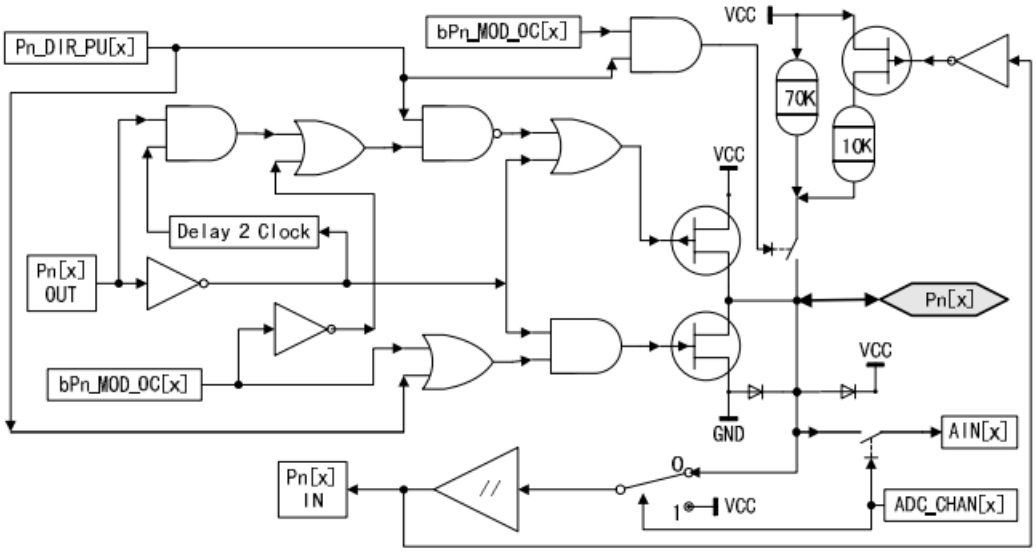


Figure 10.2.1 I / O Pin Equivalent Schematic

[section 10.3 missing in original document]

10.4 GPIO multiplexing and mapping

Some I / O pins of CH554 have alternate functions. After power-on, the default I / O pins are general-purpose I / O pins. When different function modules are enabled, the corresponding pins are configured as the corresponding function pins of the respective function modules.

Pin Function Selection Register (PIN_FUNC):

Bit	Name	Access	Description	Reset Value
7	bUSB_IO_EN	RW	USB UDP / UDM pin enable bit, this bit is 0 P3.6 / P3.7 is used for GPIO, P3_DIR_PU control pull-up resistor is supported, P3_MOD_OC is supported; this bit is 1 P3.6 / P3.7 is used for UDP / UDM controlled by USB module, P3_DIR_PU and P3_MOD_OC are invalid	1
6	bIO_INT_ACT	RO	GPIO interrupt request activation status:	0

			When bIE_IO_EDGE = 0, this bit is 1, it indicates the active level of GPIO input, interrupt will be requested and 0 means invalid input level; when bIE_IO_EDGE = 1, this bit will be used as edge interrupt flag, 1 means valid edge detected, This bit can not be cleared by software and can only be cleared automatically on reset or in the level interrupt mode or on entering the corresponding interrupt service routine	
5	bUART1_PIN_X	RW	UART1 pin mapping enable bit. When this bit is 0, RXD1 / TXD1 will use P1.6 / P1.7; if this bit is 1, RXD1 / TXD1 will use P3.4 / P3.2	0
4	bUART0_PIN_X	RW	UART0 pin mapping enable bit, if this bit is 0 then RXD0 / TXD0 will use P3.0 / P3.1; if this bit is 1 then RXD0 / TXD0 will use P1.2 / P1.3	0
3	bPWM2_PIN_X	RW	PWM2 pin mapping enable bit. When this bit is 0, PWM2 will use P3.4. When this bit is 1, PWM2 will use P3.1	0
2	bPWM1_PIN_X	RW	PWM1 pin mapping enable bit. When this bit is 0, PWM1 uses P1.5. When this bit is 1, PWM1 uses P3.0	0
1	bT2EX_PIN_X	RW	T2EX / CAP2 pin mapping enable bit, when this bit is 0 then T2EX / CAP2 will use P1.1; if this bit is 1 then T2EX / CAP2 will use RST	0
0	bT2_PIN_X	RW	T2 / CAP1 pin mapping enable bit. When this bit is 0, T2 / CAP1 will use P1.0. When this bit is 1, T2 / CAP1 will use P1.4	0

Table 10.4.1 GPIO Pin Alternate Function List

GPIO	**Other features: From left to right prioritization**
RST	RST、bT2EX_、bCAP2_、bRST
P1[0]	T2/bT2、CAP1/bCAP1、TIN0、P1.0
P1[1]	T2EX/bT2EX、CAP2/bCAP2、TIN1、VBUS2、AIN0、P1.1
P1[2]	XI、RXD_/bRXD_、P1.2
P1[3]	XO、TXD_/bTXD_、P1.3
P1[4]	T2_/bT2_、CAP1_/bCAP1_、SCS/bSCS、TIN2、UCC1、AIN1、P1.4
P1[5]	MOSI/bMOSI、PWM1/bPWM1、TIN3、UCC2、AIN2、P1.5
P1[6]	MISO/bMISO、RXD1/bRXD1、TIN4、P1.6
P1[7]	SCK/bSCK、TXD1/bTXD1、TIN5、P1.7
P3[0]	PWM1_/bPWM1_、RXD/bRXD、P3.0
P3[1]	PWM2_/bPWM2_、TXD/bTXD、P3.1

P3[2]	TXD1_/bTXD1_、INT0/bINT0、VBUS1、AIN3、P3.2
P3[3]	INT1/bINT1、P3.3
P3[4]	PWM2/bPWM2、RXD1_/bRXD1_、T0/bT0、P3.4
P3[5]	T1/bT1、P3.5
P3[6]	UDP/bUDP、P3.6
P3[6]	UDM/bUDM、P3.7

The left-to-right prioritization described in the table above refers to the order in which multiple functional modules compete for use of the GPIO. For example, P3.0 can still be used for the higher priority PWM1 output when P3.1 is used for TXD serial transmission.

11. External Bus

The CH554 does not provide a bus signal to the outside of the chip, does not support the external bus, but can access the on-chip xRAM normally.

External Bus Auxiliary Setup Register (XBUS_AUX):

Bit	**Name**	**Access**	**Description**	**Reset Value**
7	bUART0_TX	RO	Indicates the transmit status of UART0, a 1 indicates that it is transmitting	0
6	bUART0_RX	RO	Indicates the receive status of UART0, a 1 indicates that it is receiving	0
5	bSAFE_MOD_ACT	RO	Indicates the safety mode status, a 1 indicates that it is currently in safety mode	0
4	Reserved	RO	Reserved	0
3	GF2	RW	General flag 2: users can define their own, software can be cleared or set	0
2	bDPTR_AUTO_INC	RW	Enabled DPTR increments automatically after MOVX_ @ DPTR instruction completes	0
1	Reserved	RO	Reserved	0
0	DPS	RW	Dual DPTR Data Pointer Select Bits: This bit is 0 to select DPTR0; this bit is 1 to select DPTR1	0

12. Timer

12.1 Timer 0/1

Timer0 / 1 is two 16-bit timer / timers configured by TCON and TMOD for Timer0 and Timer1. TCON is used for the start-up and overflow interrupts of Timer / Counters T0 and T1 as well as external interrupt control. Each timer is a 16-bit timer unit consisting of two 8-bit registers. Timer 0 high byte counter is TH0, low byte is TL0; Timer 1 high byte counter is TH1, low byte is TL1. Timer 1 can also be used as the UART0 baud rate generator.

12.1.1 Timer / Counter 0/1 Related register list

Name	Address	Description	Reset Value
TH1	8Dh	Timer 1 counter high byte	xxh
TH0	8Ch	Timer 0 counter high byte	xxh
TL1	8Bh	Timer 1 counter low byte	xxh
TL0	8Ah	Timer 0 counter low byte	xxh
TMOD	89h	Timer 0/1 mode register	00h
TCON	88h	Timer 0/1 control register	00h

Timer / Counter 0/1 Control Register (TCON):

Bit	Name	Access	Description	Reset Value
7	TF1	RW	Timer 1 Overflow interrupt flag, enter the timer 1 interrupt automatically cleared	0
6	TR1	RW	Timer 1 Start / stop bit, set to start, set or cleared by software	0
5	TF0	RW	Timer 0 Overflow interrupt flag, enter the timer 1 interrupt automatically cleared	0
4	TR0	RW	Timer 0 Start / stop bit, set to start, set or cleared by software	0
3	IE1	RW	INT1 External interrupt 1 interrupt request flag, enter the interrupt automatically cleared	0
2	IT1	RW	INT1 External interrupt 1 trigger mode control bit, this bit is 0 Select the external interrupt is low-level trigger; This bit is 1 Select external interrupt as falling-edge trigger	0
1	IE0	RW	INT0 External interrupt 1 interrupt request flag, enter the interrupt automatically cleared	0
0	IT0	RW	INT0 External interrupt 1 trigger mode control bit, this bit is 0 Select the external interrupt is low-level trigger; This bit is 1 Select external interrupt as falling-edge trigger	0

Timer / Counter 0/1 Mode Register (TMOD):

Bit	Name	Access	Description	Reset Value
7	bT1_GATE	RW	Gating enable bit to control whether Timer1 start-up is affected by external interrupt signal INT1. When this bit is 0, the operation of timer / event counter 1 is independent of INT1. When this bit is 1, only the INT1 pin is high and TR1 is 1	0
6	bT1_CT	RW	Timing or counting mode selection bit, this bit is 0 working in timing mode; this bit is 1 working in counting mode, using the falling edge of T1 pin as clock	0
5	bT1_M1	RW	Timer / Counter 1 Mode Select High	0
4	bT1_M0	RW	Timer / Counter 1 Mode Select Low	0
3	bT0_GATE	RW	Gating enable bit to control whether Timer0 start-up is affected by external interrupt signal INT0. When this bit is 0, the operation of timer / event counter 0 is independent of INT0. When this bit is 1, only the INT0 pin is high and TR0 is 1	0
2	bT0_CT	RW	Timing or counting mode selection bit, this bit is 0 working in timing mode; this bit is 1 working in counting mode, using the falling edge of T0 pin as clock	0
1	bT0_M1	RW	Timer / Counter 0 Mode Select High	0
0	bT0_M0	RW	Timer / Counter 0 Mode Select Low	0

Table 12.1.2 bTn_M1 and bTn_M0 Selection of Timer n Operating Mode (n = 0, 1)

bTn_M1	bTn_M0	Timer n working mode (n= 0,1)
0	0	Mode 0: 13-bit timer / counter n, counting unit consists of the lower 5 bits of TLn and THn, the upper 3 bits of TLn are invalid. When the count changes from 13 bits to 1 bits to 0 bits, set the overflow flag TFn and reset the initial value
0	1	Mode 1: 16-bit timer / counter n, counting unit consists of TLn and THn. Count from 16 to 1 for all into all 0, set the overflow flag TFn, and reset the initial value
1	0	Mode 2: 8-bit reload timer / counter n. The counting unit uses TLn, THn as the overloaded counting unit. When the count is changed from 8 bits to 1 bits and all 0s, the overflow flag TFn is set and the initial value is automatically loaded from THn
1	1	Mode 3: Timer / Counter 0 is divided into two sections, TL0 and TH0, for Timer / Counter 0, which takes up all Timer0 control bits, while Timer / Counter0 also uses another 8-bit timer Use, occupy Timer1 TR1, TF1 and interrupt resources, and Timer1 is still available, but can not use the start control bit TR1 and overflow flag TF1. If Timer / Event Counter 1 is set,

		entering Mode 3 will stop Timer / Counter 1.

Timer n count low byte (TLn) (n = 0, 1):

Bit	Name	Access	Description	Reset Value
[7:0]	TLn	RW	Timer n count low byte	xxh

Timer n count high byte (THn) (n = 0, 1):

Bit	Name	Access	Description	Reset Value
[7:0]	THn	RW	Timer n count high byte	xxh

12.2 Timer 2

Timer2 is a 16-bit auto-reload timer configured by the T2CON and T2MOD registers. The upper byte counter of Timer 2 is TH2 and the lower byte is TL2. Timer2 can be used as UART0 baud rate generator, but also has 2 signal level capture function, the capture count is stored in the RCAP2 and T2CAP1 registers.

Table 12.2.1 Timer2 Related Registers List

Name	Address	Description	Reset Value
TH2	CDh	Timer2 counter high byte	00h
TL2	CCh	Timer2 counter low byte	00h
T2COUNT	CCh	TL2 and TH2 form a 16-bit SFR	0000h
T2CAP1H	CFh	Timer2 Capture 1 Data High Byte (Read Only)	xxh
T2CAP1L	CEh	Timer2 Capture 1 Data Low Byte (Read Only)	xxh
T2CAP1	CEh	T2CAP1L and T2CAP1H make up a 16-bit SFR	xxxxh
RCAP2H	CBh	Count Reload / Capture 2 Data Register High Byte	00h
RCAP2L	CAh	Count Reload / Capture 2 Data Register Low Byte	00h
RCAP2	CAh	RCAP2L and RCAP2H make up a 16-bit SFR	0000h
T2MOD	C9h	Timer 2 mode register	00h
T2CON	C8h	Timer 2 control register	00h

Timer/Counter 2 Control Register (T2CON):

Bit	Name	Access	Description	Reset Value
7	TF2	RW	When bT2_CAP1_EN = 0, this is the overflow interrupt flag of Timer2. When the Timer2 count changes from 16 to 1, the overflow flag is set to 1 and needs to be cleared by software;	0

			when RCLK=1 or TCLK=1 , this bit will not be set to 1	
7	CAP1F	RW	When bT2_CAP1_EN=1, it is Timer2 Capture 1 interrupt flag triggered by T2 valid edge and requires software clear	0
6	EXF2	RW	Timer2 external trigger flag, set by T2EX active edge trigger when EXEN2 = 1, requires software clear	0
5	RCLK	RW	UART0 receive clock select, this bit is 0. Select Timer1 overflow pulse to generate baud rate; this bit is 1 to select Timer2 overflow pulse to generate baud rate.	0
4	TCLK	RW	UART0 transmit clock selection, this bit is 0. Select Timer1 overflow pulse to generate baud rate; this bit is 1 to select Timer2 overflow pulse to generate baud rate.	0
3	EXEN2	RW	T2EX trigger enable bit. This bit is 0. Ignore T2EX; this bit is 1 to enable reload or capture on T2EX active edge.	0
2	TR2	RW	Timer2 start/stop bit, set to start, set or cleared by software	0
1	C_T2	RW	Timer2 clock source select bit, this bit is 0 Use internal clock; this bit is 1 Use edge count based on falling edge of T2 pin	0
0	CP_RL2	RW	Timer2 function select bit. This bit should be forced to 0 if RCLK or TCLK is 1. When this bit is 0, Timer2 acts as a timer/counter, and can automatically reload the initial count value when the counter overflows or the T2EX level changes; this bit is 1 to enable Timer2's Capture 2 function to capture the T2EX active edge.	0

Timer/Counter 2 Mode Register (T2MOD):

Bit	**Name**	**Access**	**Description**	**Reset Value**
7	bTMR_CLK	RW	The fastest clock mode is enabled for the T0/T1/T2 timer that has been selected for the fast clock. If this bit is set to 1, the system clock frequency Fsys without frequency division is used as the count clock; if this bit is 0, the clock frequency is used. This bit has no effect on the timer that selects the standard clock	0
6	bT2_CLK	RW	Timer2 internal clock frequency selection bit, this bit is 0 to select the standard clock, timer/counter mode is Fsys/12, UART0 clock mode is Fsys/4; this bit is 1 to select fast clock, timer/count mode is Fsys/4 (bTMR_CLK =0) or Fsys (bTMR_CLK=1), UART0 clock mode is Fsys/2 (bTMR_CLK=0) or Fsys (bTMR_CLK=1)	0
5	bT1_CLK	RW	Timer1 internal clock frequency selection bit, this bit is 0. Select the standard clock Fsys/12; select the fast clock Fsys/4 (bTMR_CLK=0) or Fsys	0

			(bTMR_CLK=1)		
4	BT0_CLK	RW	Timer0 internal clock frequency selection bit, this bit is 0. Select the standard clock Fsys/12; select the fast clock Fsys/4 (bTMR_CLK=0) or Fsys (bTMR_CLK=1)		0
3	bT2_CAP_M1	RW	Timer2 capture mode high	Capture mode selection: X0: From falling edge to falling edge 01: From any edge to any edge, that is, change in level 11: From the rising edge to the rising edge	0
2	bT2_CAP_M0	RW	Timer2 capture mode low		0
1	T2OE	RW	Timer2 clock output enable bit. This bit is 0. Disable output. This bit is 1 to enable T2 pin output clock with half the Timer2 overflow rate.		0
0	bT2_CAP1_EN	RW	Capture 1 mode is enabled when RCLK = 0, TCLK = 0, CP_RL2 = 1, C_T2 = 0, and T2OE = 0. This bit is set to 1 to enable the capture 1 function to capture the active edge of T2; this bit 0 disables capture 1		0

Counting Reload/Capture 2 Data Registers (RCAP2):

Bit	**Name**	**Access**	**Description**	**Reset Value**
[7:0]	RCAP2H	RW	High byte of reload value in timer/counter mode; high byte of timer captured by CAP2 in capture mode	00h
[7:0]	RCAP2L	RW	The low byte of the reload value in timer/counter mode; the low byte of the timer captured by CAP2 in capture mode	00h

Timer2 Counter (T2COUNT):

Bit	**Name**	**Access**	**Description**	**Reset Value**
[7:0]	TH2	RW	Current counter high byte	00h
[7:0]	TL2	RW	Current counter low byte	00h

Timer2 capture 1 data (T2CAP1):

Bit	**Name**	**Access**	**Description**	**Reset Value**
[7:0]	T2CAP1H	RO	High byte of the timer captured by CAP1	xxh

[7:0]	T2CAP1L	RO	The low byte of the timer captured by CAP1	xxh

12.3 PWM function

CH554 provides two 8-bit PWM, PWM can choose the default output polarity is low or high, you can dynamically modify the PWM output duty cycle, through a simple RC resistor capacitor integrated low-pass filter, you can Get a variety of output voltage, equivalent to low-speed digital-to-analog converter DAC.

PWM1 output duty cycle = PWM_DATA1 / 256, support range 0% to 99.6%.
PWM2 output duty cycle = PWM_DATA2 / 256, support range 0% to 99.6%.

In practice, it is recommended to allow PWM pin output and set the PWM output pin to push-pull output mode.

12.3.1 PWM1 and PWM2

Table 12.3.1 PWM1 and PWM2 related register list

Name	Address	Description	Reset Value
PWM_CK_SE	9Eh	PWM clock divider setting register	00h
PWM_CTRL	9Dh	PWM control register	02h
PWM_DATA1	9Ch	PWM1 data register	xxh
PWM_DATA2	9Bh	PWM2 data register	xxh

PWM2 Data Register (PWM_DATA2):

Bit	Name	Access	Description	Reset Value
[7:0]	PWM_DATA2	RW	Store the current data of PWM2, PWM2 output active level duty cycle = PWM_DATA2 / 256	xxh

PWM1 Data Register (PWM_DATA1):

Bit	Name	Access	Description	Reset Value
[7:0]	PWM_DATA1	RW	Store the current data of PWM1, PWM1 output active level duty cycle = PWM_DATA1 / 256	xxh

PWM Control Register (PWM_CTRL):

Bit	Name	Access	Description	Reset Value
7	bPWM_IE_END	RW	This bit is set to 1 to enable the end of the PWM cycle or to leave the MFM buffer empty	0

6	bPWM2_POLAR	RW	Control PWM2 output polarity, the bit is 0, the default low, high effective; the bit is 1, the default high, low active	0
5	bPWM1_POLAR	RW	Control PWM1 output polarity, the bit is 0, the default low, high effective; the bit is 1, the default high, low active	0
4	4 bPWM_IF_END	RW	PWM cycle end interrupt flag bit, this bit is 1 indicates interrupt, write 1 cleared or reload PWM_DATA1 data cleared	0
3	bPWM2_OUT_EN	RW	PWM2 output enable, setting this bit to 1 enables the PWM2 output	0
2	bPWM1_OUT_EN	RW	PWM1 output enable, setting this bit to 1 enables the PWM1 output	0
1	bPWM_CLR_ALL	RW	This bit is set to 1 to clear PWM1 and PWM2 counts and FIFOs and requires software reset	1
0	Reserved	RO	Reserved	0

PWM Clock Divider Setting Register (PWM_CK_SE):

Bit	**Name**	**Access**	**Description**	**Reset Value**
[7:0]	PWM_CK_SE	RW	Set the PWM clock divider	00h

12.4 Timer Function

12.4.1 Timer 0 / 1

1. Set T2MOD to select the internal clock frequency of Timer. If bTn_CLK (n = 0/1) is 0, then the corresponding clock of Timer0 / 1 is Fsys / 12; if bTn_CLK is 1, select bsMR_CLK = 0 or 1 to select Fsys / 4 or Fsys as the clock.
2. Set the TMOD configuration Timer work mode.
3. Set timer / counter initial value TLn and THn (n = 0/1).
4. Setting bit TRn (n = 0/1) in TCON Enables or disables the timer, which can be interrogated by bit TFn (n = 0/1) or by interrupt.

Mode 0:13 bit timer / counter

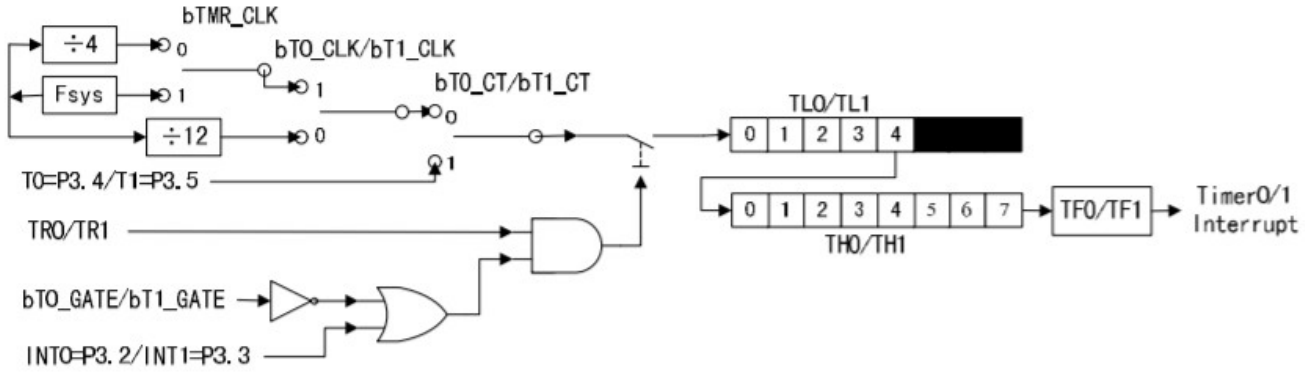


Figure 12.4.1.1 Timer0 / 1 Mode 0

Mode 1:16 bit timer / counter

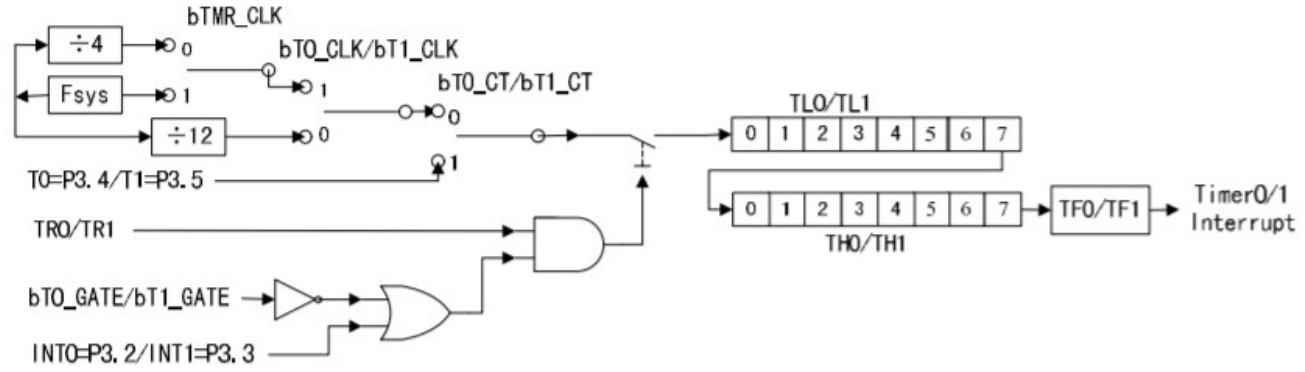


Figure 12.4.1.2 Timer0 / 1 Mode 1

Mode 2: Automatic reload of 8-bit timer / counter

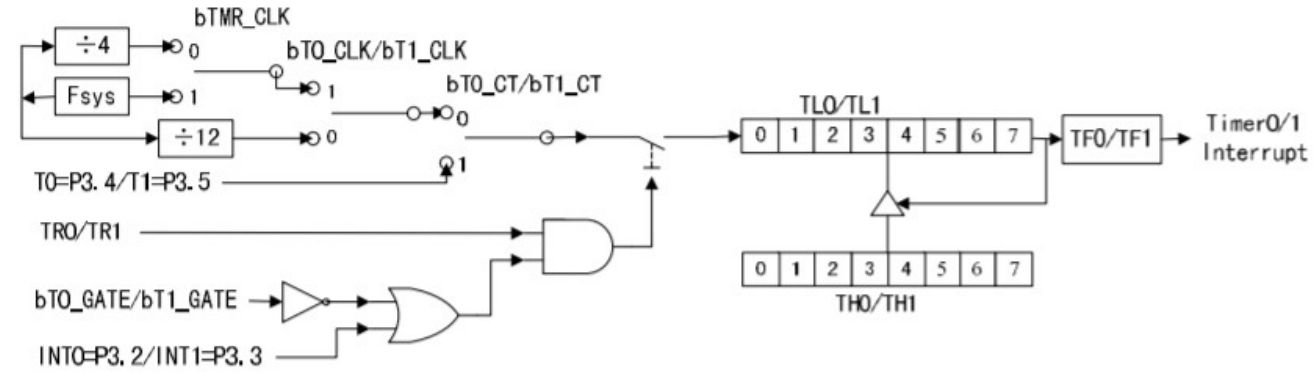


Figure 12.4.1.3 Timer0 / 1 Mode 2

Mode 3: Timer0 is split into two independent 8-bit Timer / Counters and borrows the TR1 control bit of Timer1. Timer1 stops running by entering Start Mode 3 in place of the borrowed TR1 control bit.

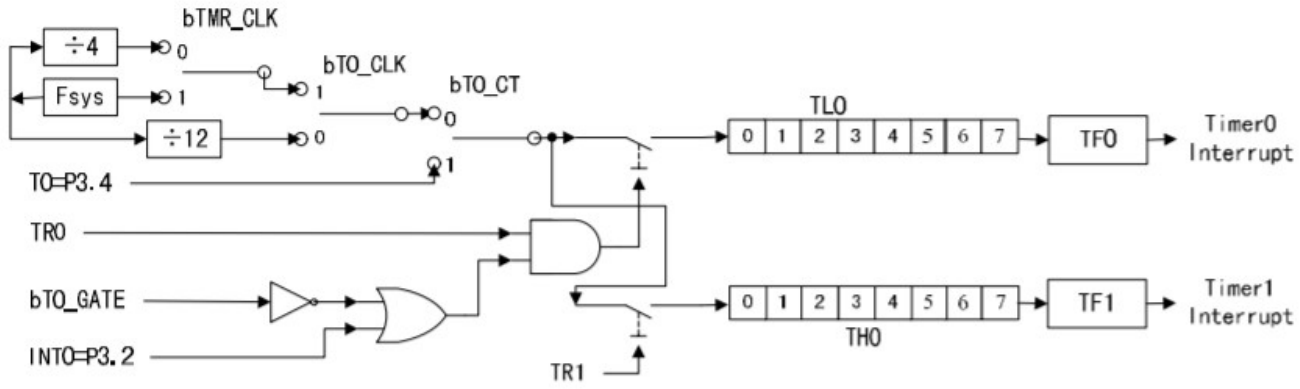


Figure 12.4.1.4 Timer0 Mode 3

12.4.2 Timer2

Timer2 16-bit reload timer / counter mode:

1. Set bits RCLK and TCLK in T2CON to 0 to select non-serial port baud rate generator mode.
2. To set bit T2 in C_T2 to 0 to use internal clock, go to step (3); set to 1 to select the falling edge of T2 pin

   As the count clock, skip step (3).
3. Set T2MOD to select the internal clock frequency of Timer. If bT2_CLK is 0, then the clock of Timer2 is Fsys / 12.

   If bT2_CLK is 1, then bsMR_CLK = 0 or 1 selects Fsys / 4 or Fsys as the clock.
4. Set the bit CP_RL2 of T2CON to 0 to select the Timer2 16-bit reload timer function.
5. Set RCAP2L and RCAP2H as reload value after timer overflow, set TL2 and TH2 as initial value of timer (Generally the same as RCAP2L and RCAP2H), set TR2 to 1 and turn on Timer2.
6. The current timer / counter status can be retrieved by interrogating TF2 or Timer 2 interrupts.

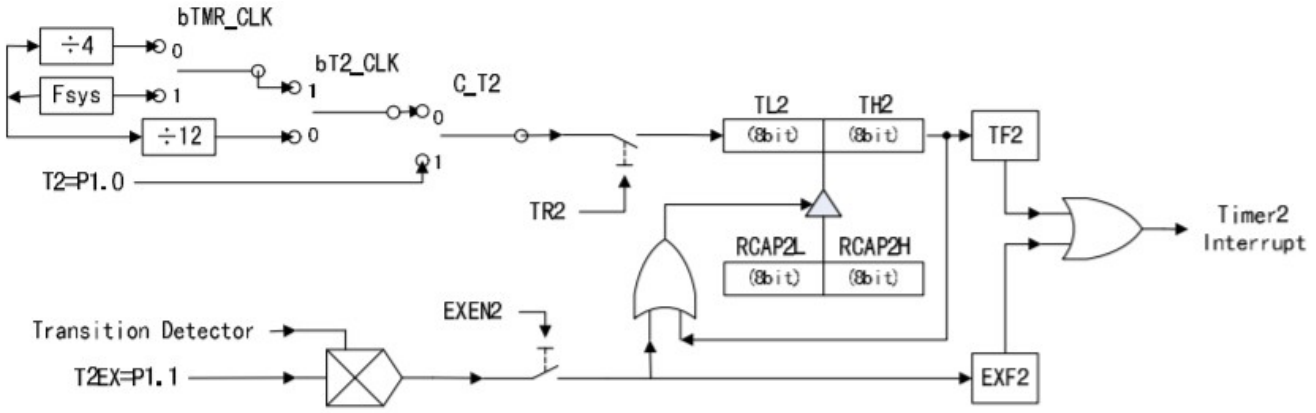


Figure 12.4.2.1 Timer2 16-Bit Reload Timer / Counter

Timer2 clock output mode:

Referring to the 16-bit reload timer / counter mode and setting bit T2OE in T2MOD to 1, the divide-by-2 clock of the TF2 frequency output from the T2 pin is enabled.

Timer2 Serial Port 0 Baud Rate Generator Mode:

1. Set bit C_T2 in T2CON to 0 Select to use internal clock, or set to select the falling edge of T2 pin as clock. Set bits RCLK and TCLK in T2CON to 1 or 1 if necessary, Select serial baud rate generator mode.
2. Set T2MOD to select the internal clock frequency of Timer. If bT2_CLK is 0, then Timer2 clock is Fsys / 4; if bT2_CLK is 1, select bsMR / 2 or Fsys as the clock by bTMR_CLK = 0 or 1.
3. Set RCAP2L and RCAP2H as reload value after timer overflow, set TR2 to 1 and enable Timer2.

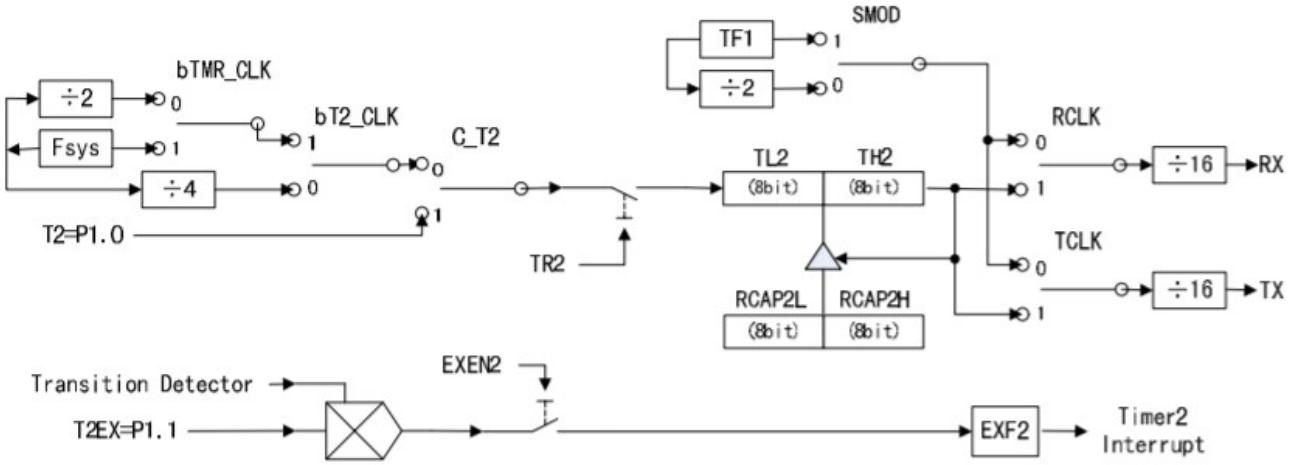


Figure 12.4.2.2 Timer2 UART0 Baud Rate Generator

Timer2 dual channel capture mode:

1. Set bits RCLK and TCLK in T2CON to 0 to select non-serial port baud rate generator mode.
2. Set bit C_T2 in T2CON to 0. Select to use internal clock and go to step (3). Set to 1 to select the falling edge of T2 pin as the count clock and skip step (3).
3. Set T2MOD to select the internal clock frequency of Timer. If bT2_CLK is 0, then the clock of Timer2 is Fsys / 12; if bT2_CLK is 1, then bsMR_CLK = 0 or 1 selects Fsys / 4 or Fsys as the clock.
4. Set the T2MOD bits bT2_CAP_M1 and bT2_CAP_M0 to select the corresponding edge capture mode.
5. Set bit T2_CONT of CP2 to 1 to select the capture function of Timer2 on the T2EX pin.
6. Set TL2 and TH2 as the initial value of the timer, set TR2 to 1 and enable Timer2.
7. When CAP2 capture is completed, RCAP2L and RCAP2H will save the current TL2 and TH2 count values and set EXF2 to generate an interrupt. The next capture between RCAP2L and RCAP2H and the last captured RCAP2L and RCAP2H The difference is the signal width between the two valid edges.
8. If T2CON bit C_T2 is 0 and T2MOD bit bT2_CAP1_EN is 1, the capture function of Timer2 on T2 pin will be enabled. When CAP1 capture is completed, T2CAP1L and T2CAP1H will save the current TL2 and TH2 The count value, and set CAP1F, resulting in an interrupt.

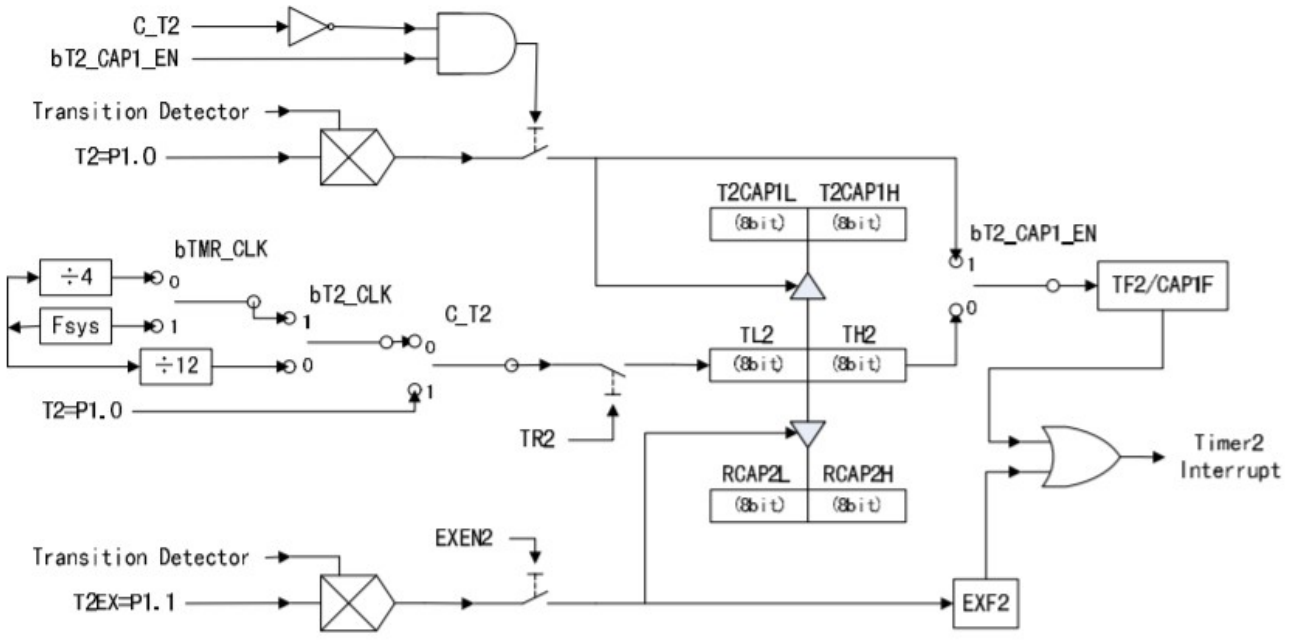


Figure 12.4.2.3 Timer2 Capture Mode

13. Universal Asynchronous Receiver Transmitter (UART)

13.1 UART Introduction

CH554 chip provides two full duplex asynchronous serial ports: UART0 and UART1. CH553 only provides UART0.

UART0 is a standard MCS51 serial port, the data is received and sent through the SBUF access physically separate receive / send registers to achieve. The data written to SBUF is loaded into the transmit register and the read from SBUF corresponds to the receive buffer register.

UART1 is a simplified MCS51 serial port, the data is received and sent through the SBUF1 access physically separate receive / send registers to achieve. The data written to SBUF1 is loaded into the transmit register and the read from SBUF1 corresponds to the receive buffer register. Compared with UART1, UART1 eliminates the multi-machine communication mode and fixed baud rate. UART1 has an independent baud rate generator.

13.2 UART Register

Table 13.2.1 UART related register list

Name	Address	Description	Reset Value
SCON	98h	UART0 control register	00h
SBUF	99h	UART0 data register	xxh
SCON1	C0h	UART1 control register	40h
SBUF1	C1h	UART1 data register	xxh
SBAUD1	C2h	UART1 baud rate setting register	xxh

13.2.1 UART0 Register Description

UART0 Control Register (SCON):

Bit	Name	Access	Description	Reset Value
7	SM0	RW	UART0 working mode select bit 0, this bit is 0 select 8-bit data asynchronous communication; this bit is 1 select 9-bit data asynchronous communication	0
6	SM1	RW	UART0 work mode select bit 1, this bit is 0 to set a fixed baud rate; this bit is 1 to set variable baud rate, generated by timer T1 or T2	0
5	SM2	RW	UART0 multi-machine communication control bit: In modes 2 and 3, when SM2 = 1 when SM2 = 1 when receiving data, RI is not set and reception is invalid if RB8 is 0; RI is set and reception is	0

			enabled if RB8 is 1; and when SM2 = 0, 0 or 1, RI is set when receiving data, receiving is valid In mode 1, if SM2 = 1, reception is only valid if a valid stop bit is received; In mode 0, SM2 bit must be set to 0	
4	REN	RW	UART0 allows to receive the control bit, this bit is 0 forbidden to receive; This bit is 1 to allow to receive	0
3	TB8	RW	The ninth bit of data to be transmitted, in modes 2 and 3, TB8 is used to write the ninth bit of the transmit data, which can be a parity bit. In multi-machine communication, TB8 is used to indicate whether the host sends an address byte or not Data byte, TB8 = 0 for data, TB8 = 1 for address	0
2	RB8	RW	The 9th bit of receive data, in mode 2 and 3, RB8 is used to store the 9th bit of receive data In mode 1, if SM2 = 0 then RB8 is used to store the received stop bit In mode 0, RB8 is not used	0
1	TI	RW	Send interrupt flag, set by hardware after a data byte is sent, software needs to be cleared	0
0	RI	RW	Receive interrupt flag, set by hardware after a data byte is received, software reset	0

Table 13.2.1.1 UART0 Operating Mode Selection

SM0	**SM1**	**Description**
0	0	Mode 0, shift register mode, fixed baud rate is Fsys / 12
0	1	Mode 1,8-bit asynchronous communication mode, the baud rate variable, generated by the timer T1 or T2
1	0	Mode 2, 9-bit asynchronous communication mode, the baud rate is Fsys / 128 (SMOD = 0) or Fsys / 32 (SMOD = 1)
1	1	Mode 3, 9 asynchronous communication mode, baud rate variable, generated by the timer T1 or T2

Under modes 1 and 3, UART0 baud rate is generated by timer T1 when RCLK = 0 and TCLK = 0. T1 should be mode 2 automatic reload 8-bit timer mode, bT1_CT and bT1_GATE must be 0, divided into the following types of clock conditions.

Table 13.2.1.2 Calculating the UART0 baud rate from T1

bTMR_CLK	**bT1_CLK**	**SMOD**	**Description**
1	1	0	TH1 = 256 - Fsys / 32 / baud rate

1	1	1	TH1 = 256 - Fsys / 16 / baud rate
0	1	0	TH1 = 256 - Fsys / 4 / 32 / baud rate
0	1	1	TH1 = 256 - Fsys / 4 / 16 / baud rate
x	0	0	TH1 = 256 - Fsys / 12 / 32 / baud rate
x	0	1	TH1 = 256 - Fsys / 12 / 16 / baud rate

In modes 1 and 3, UART0 baud rate is generated by Timer T2 when RCLK = 1 or TCLK = 1. T2 should be set to 16-bit auto-reload baud rate generator mode, C_T2 and CP_RL2 must be 0, divided into the following types of clock conditions.

Table 13.2.1.3 Calculating the UART0 Baud Rate from T2

bTMR_CLK	**bT2_CLK**	**Description**
1	1	RCAP2 = 65536 - Fsys / 16 / baud rate
0	1	RCAP2 = 65536 - Fsys / 2 / 16 / baud rate
x	0	RCAP2 = 65536 - Fsys / 4 / 16 / baud rate

UART0 Data Register (SBUF):

Bit	**Name**	**Access**	**Description**	**Reset Value**
[7:0]	SBUF	RW	UART0 data register, including sending and receiving two physically separate registers. Write data to SBUF corresponding to send data register; Read data from SBUF corresponding to receive data register	xxh

13.2.2 UART1 Register Description

UART1 Control Register (SCON1):

Bit	**Name**	**Access**	**Description**	**Reset Value**
7	U1SM0	RW	UART1 work mode select bit, this bit is 0 Select 8-bit data asynchronous communication; This bit is 1 Select 9-bit data asynchronous communication	0
6	Reserved	RO	Reserved	1
5	U1SMOD	RW	Select UART1 communication baud rate: 0 - slow mode; 1 - fast mode	0
4	U1REN	RW	UART1 allows to receive the control bit, this bit is 0 forbidden to receive; This bit is 1 to allow to receive	0

3	U1TB8	RW	The 9th bit of data to be transmitted. In 9-bit data mode, TB8 is used to write the 9th bit of the transmit data and can be a parity bit. In 8-bit data mode, TB8 is ignored	0
2	U1RB8	RW	In the 9-bit data mode, RB8 is used to store the 9th bit of receive data. In 8-bit data mode, RB8 is used to store the received stop bits	0
1	U1TI	RW	Send interrupt flag, set by hardware after a data byte is sent, software needs to be cleared	0
0	U1RI	RW	Receive interrupt flag, set by hardware after a data byte is received, software reset	0

UART1 baud rate generated by the SBAUD1 settings, according to the choice of U1SMOD is divided into two cases:

- When U1SMOD = 0, SBAUD1 = 256 - Fsys / 32 / baud rate
- When U1SMOD = 1, SBAUD1 = 256 - Fsys / 16 / baud rate
-

UART1 Data Register (SBUF1):

Bit	**Name**	**Access**	**Description**	**Reset Value**
[7:0]	SBUF1	RW	UART1 data register, including sending and receiving two physically separate registers. Write data to SBUF1 corresponding to send data register; read data from SBUF1 corresponding receive data register	xxh

13.3 UART Applications

UART0 Application:

1. Select UART0 baud rate generator, you can choose from the timer T1 or T2, and configure the corresponding counter.
2. Turn on the timer T1 or T2.
3. Set SCON's SM0, SM1, SM2 select the serial port 0 operating mode. Set REN to 1 to enable UART0 reception.
4. You can set the serial port interrupt or query RI and TI interrupt status.
5. Read and write SBUF send and receive serial data, serial port receive signal baud rate error of not more than 2%.

UART1 Application:

1. Select U1SMOD and set SBAUD1 according to the baud rate.
2. Set U1SM0 of SCON1 to select the working mode of serial port 1. Set U1REN to 1 to enable UART1 reception.
3. You can set the serial port 1 interrupt or query U1RI and U1TI interrupt status.
4. Read and write serial port 1 SBUF1 send and receive data, the serial port receive signal baud rate error of not more than 2%.

14. Synchronous Serial Interface (SPI)

14.1 Introduction to SPI

CH554 chip provides SPI interface for high-speed synchronous data transfer between peripherals.

1. Support master master mode and slave slave mode;
2. Support mode 0 and mode 3 clock mode;
3. Optional 3-line full-duplex or 2-wire half-duplex mode;
4. Optional MSB high first sent or LSB low first sent;
5. Adjustable clock frequency, up to nearly half of the system clock speed;
6. Built-in 1 byte receive FIFO and 1 byte transmit FIFO;
7. The first byte in the slave mode to support preloading data, easy for the host to get the first byte immediately return data.

14.2 SPI Register

Table 14.2.1 SPI related register list

Name	Address	Description	Reset Value
SPI0_SETUP	FCh	SPI0 setting register	00h
SPI0_S_PRE	FBh	SPI0 Slave Mode Preset Data Register	20h
SPI0_CK_SE	FBh	SPI0 clock frequency division setting register	20h
SPI0_CTRL	FAh	SPI0 control register	02h
SPI0_DATA	F9h	SPI0 data transceiver register	xxh
SPI0_STAT	F8h	SPI0 status register	08h

SPI0 setting register (SPI0_SETUP):

Bit	Name	Access	Description	Reset Value

7	bS0_MODE_SLV	RW	SPI0 master / slave mode select bit. When this bit is 0, SPI0 is master mode. When this bit is 1, SPI0 is slave mode / device mode	0
6	bS0_IE_FIFO_OV	RW	FIFO overflow interrupt enable bit in slave mode, this bit enables the FIFO overflow interrupt by 1; this bit causes the FIFO overflow without interrupt	0
5	bS0_IE_FIRST	RW	Interrupt enable bit is received in Slave mode when the first byte is complete. This bit is 1. Interrupt is triggered when the first data byte is received in slave mode. When this bit is 0, no interrupt is generated when the first byte is received	0
4	bS0_IE_BYTE	RW	Data byte transfer complete interrupt enable bit, the bit is 1 to allow byte transfer complete interrupt; the bit is 0, the byte transfer is completed without interruption	0
3	bS0_BIT_ORDER	RW	Data byte bit control bit, this bit is 0 MSB high in the front; this bit is 1 LSB low in the former	0
2	Reserved	RO	Reserved	0
1	bS0_SLV_SELT	RO	Chip select active status bit in slave mode, this bit is 0 to indicate that it is not currently selected; this bit indicates that it is currently selected	0
0	bS0_SLV_PRELOAD	RO	Pre-load data status bit in slave mode, which indicates that the current pre-load state has not been transferred after the chip select is valid	0

SPI0 Clock Divider Setting Register (SPI0_CK_SE):

Bit	**Name**	**Access**	**Description**	**Reset Value**
[7:0]	SPI0_CK_SE	RW	Set the SPI0 clock division factor in master mode	20h

SPI0 Slave Mode Preset Data Register (SPI0_S_PRE):

Bit	**Name**	**Access**	**Description**	**Reset Value**
[7:0]	SPI0_S_PRE	RW	Load the first transmission data in slave mode beforehand	20h

SPI0 Control Register (SPI0_CTRL):

Bit	**Name**	**Access**	**Description**	**Reset Value**

7	bS0_MISO_OE	RW	SPI0 MISO output enable control bit, the bit is 1 to allow output; this bit is 0 to disable the output	0
6	bS0_MOSI_OE	RW	SPI0 MOSI output enable control bit, this bit is 1 enable output; this bit is 0 disable output	0
5	bS0_SCK_OE	RW	SPI0 SCK output enable control bit, this bit is 1 enable output; this bit is 0 disable output	0
4	bS0_DATA_DIR	RW	SPI0 Data Direction Control bit. When this bit is 0, the data is output. Only the write FIFO is validated, an SPI transfer is enabled. When this bit is 1, data is input. The write or read FIFO is used as a valid operation to start an SPI transfer	0
3	bS0_MST_CLK	RW	SPI0 master clock mode control bit, the bit is 0 then mode 0, SCK idle default low; the bit is 1 mode 3, SCK default high	0
2	bS0_2_WIRE	RW	SPI0 2-wire half-duplex mode enable bit, the bit is 0 3-wire full duplex mode, including SCK, MOSI, MISO; This bit is 1 2-wire half duplex mode, including SCK, MISO	0
1	bS0_CLR_ALL	RW	This bit is cleared to 1 by the SPI0 interrupt flag and FIFO. This bit is cleared by software	1
0	bS0_AUTO_IF	RW	Enable effective operation through the FIFO Auto-clear byte Receive complete interrupt flag enable bit, the bit is 1, the FIFO is automatically cleared when a valid read and write Byte Completion Interrupt flag S0_IF_BYTE Clear	0

SPI0 Data Transceiver Register (SPI0_DATA):

Bit	**Name**	**Access**	**Description**	**Reset Value**
[7:0]	SPI0_DATA	RW	Including sending and receiving two physically separate FIFOs, reading data into a receive data FIFO, writing data to a transmit data FIFO, and valid reads and writes to initiate an SPI transfer	xxh

SPI0 Status Register (SPI0_STAT):

Bit	**Name**	**Access**	**Description**	**Reset Value**
7	S0_FST_ACT	RO	This bit is 1 to indicate that the current state is completed when the first byte is received in slave mode	0
6	S0_IF_OV	RW	FIFO overflow flag in slave mode. This bit indicates a 1-out-of-FIFO interrupt. A 0 bit indicates no interrupt. Direct bit access to clear or write a clear zero. Interrupt triggered by	0

			transmit FIFO empty when bS0_DATA_DIR = 0; triggered by receive FIFO full interrupt when bS0_DATA_DIR = 1	
5	S0_IF_FIRST	RW	The first byte received in slave mode completes the interrupt flag. A 1 bit indicates the first byte was received. Direct bit access to clear or write a clear zero	0
4	S0_IF_BYTE	RW	Data byte transfer completed interrupt flag, the bit is 1 that a byte transfer is complete. Direct bit access clear or write 1 clear, or cleared by FIFO valid operation when bS0_AUTO_IF = 1	0
3	S0_FREE	RO	SPI0 free flag, the bit is 1 that there is no current SPI shift, usually in the data bytes between the neutral period	1
2	S0_T_FIFO	RO	SPI0 transmit FIFO counter, valid value is 0 or 1	0
1	Reserved	RO	Reserved	0
0	S0_R_FIFO	RO	SPI0 receive FIFO counter, valid value is 0 or 1	0

14.3 SPI Transfer Format

The SPI master mode supports two transfer formats, mode 0 and mode 3, which can be selected by setting bit bSn_MST_CLK in the SPI control register SPIn_CTRL, which always samples the MISO data on the rising edge of CLK. Data transmission format as shown below.

Mode 0: bSn_MST_CLK = 0

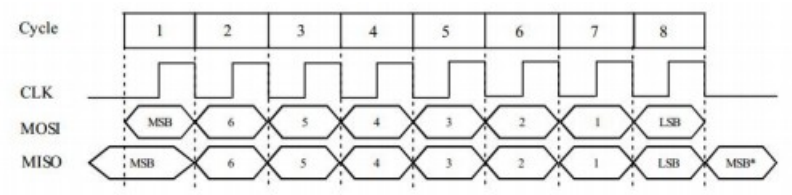


Figure 14.3.1 SPI Mode 0 Timing Diagram

Mode 3: bSn_MST_CLK = 1

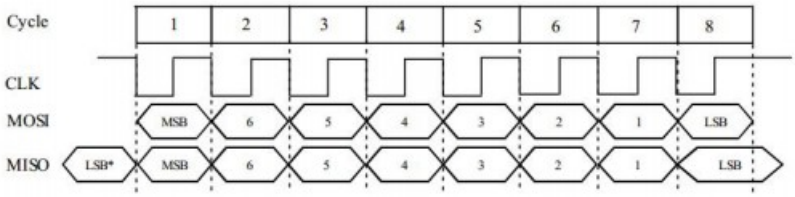


Figure 14.3.2 SPI Mode 3 Timing Diagram

14.4 SPI Configuration

14.4.1 SPI Master Mode Configuration

In SPI master mode, the SCK pin outputs a serial clock and the chip select output pin can be specified as any I / O pin. SPI0 configuration steps:

1. Set the SPI clock frequency division setting register SPI0_CK_SE, configure the SPI clock frequency.
2. Set bit bS0_MODE_SLV of SPI setting register SPI0_SETUP to 0 to configure as master mode.
3. Set bit bS0_MST_CLK in SPI control register SPI0_CTRL and set to mode 0 or 3 according to the requirement.
4. Set the bits bS0_SCK_OE and bS0_MOSI_OE of the SPI control register SPI0_CTRL to 1 and the bS0_MISO_OE bit to 0 to set the P1 port direction bSCK, bMOSI to output, bMISO to input, and chip select to output.

Data transmission process:

1. Write SPI0_DATA register, write to the FIFO to send data, automatically start an SPI transfer.
2. Waiting for S0_FREE to 1, indicating that the transmission is completed, you can continue to send the next byte.

Data reception process:

1. Write the SPI0_DATA register and write any data such as 0FFh to the FIFO to initiate an SPI transfer.
2. Wait for S0_FREE to 1, indicating that the reception is completed, SPI0_DATA can be read to get the received data.
3. If the previous bS0_DATA_DIR has been set, then the above read operation will also start the next SPI transfer, otherwise it will not start.

14.4.2 SPI Slave Mode Configuration

Only SPI0 supports slave mode. In slave mode, the SCK pin is used to receive the serial clock of the connected SPI master.

1. Set bit bS0_MODE_SLV of SPI0 setting register SPI0_SETUP to 1 to configure slave mode.
2. Set bits bS0_SCK_OE and bS0_MOSI_OE of SPI0 control register SPI0_CTRL to 0, set bS0_MISO_OE to 1, set P1 port direction bSCK, bMOSI and bMISO, and chip select pins as inputs. When the SCS chip select active (low), MISO will automatically enable the output. It is also recommended to set the MISO pin to high-impedance input mode (P1_MOD_OC [6] = 0, P1_DIR_PU [6] = 0) to disable MISO output during the chip select period.

3. Optionally, set the SPI slave mode preset data memory SPI0_S_PRE for the first time automatically loaded into the buffer after being selected for output to the external buffer. After 8 serial clocks, ie the first data byte transfer is completed, the CH554 gets the first byte of data (possibly the command code) from the external SPI master and the external SPI master exchanges the preset data in SPI0_S_PRE (possibly Is the status value). Bit 7 of register SPI0_S_PRE is automatically loaded onto the MISO pin during the SCK low level after the SPI chip select is asserted. For SPI mode 0, if CH554 is preset to bit 7 of SPI0_S_PRE, the external SPI master will select on the SPI chip select When data is valid but not yet transmitted, the value of bit 7 of SPI0_S_PRE can be obtained by querying the MISO pin for bit 7 of the SPI0_S_PRE, thereby obtaining the value of bit 7 of SPI0_S_PRE by simply validating the SPI chip select.

Data transmission process:

1. Query S0_IF_BYTE or wait for an interrupt. After each SPI data byte transfer, write the SPI0_DATA register and write the data to be sent to the FIFO. Or wait for S0_FREE to change from 0 to 1, you can continue to send the next byte.

Data reception process:

1. Query S0_IF_BYTE or wait for an interrupt. After each SPI data byte transfer completes, read the SPI0_DATA register and receive the data from the FIFO. Query S0_R_FIFO FIFO can be found in the remaining bytes.

15. ADC and voltage comparator (ADC)

15.1 Introduction to ADC

The CH554 provides an 8-bit analog-to-digital converter including a voltage comparator and an ADC module. The converter has four analog signal input channels, can be collected in time, support 0 to VCC analog input voltage range.

15.2 ADC Register

Table 15.2.1 ADC related register list

Name	Address	Description	Reset Value
ADC_CTRL	80h	ADC control register	x0h
ADC_CFG	9AH	ADC Configuration Register	00h
ADC_DATA	9Fh	ADC data register	xxh

ADC Control Register (ADC_CTRL):

Bit	Name	Access	Description	Reset Value

7	CMPO	RO	Voltage Comparator result output bit, this bit is 0 Description The voltage at the non-inverting input is lower than the voltage at the inverting input. When this bit is 1, the voltage at the non-inverting input is higher than the voltage at the inverting input	x
6	CMP_IF	RW	Voltage comparator results change flag, the bit is 1 that the voltage comparator results have changed, direct bit access clear	0
5	ADC_IF	RW	ADC conversion completed interrupt flag, the bit is 1 that an ADC conversion is completed, direct bit access to clear	0
4	ADC_START	RW	ADC start-up control bit, set to 1 to start the ADC conversion. This bit is automatically cleared after the ADC conversion is completed	0
3	CMP_CHAN	RW	Voltage comparator inverting input selection: 0-AIN1; 1-AIN3	0
2	Reserved	RO	Reserved	0
1	ADC_CHAN1	RW	Voltage comparator positive input and ADC input channel selection high	0
0	ADC_CHAN0	RW	Voltage comparator positive input and ADC input channel selection low	0

The voltage comparator positive-phase input and ADC channel are selected by ADC_CHAN1 and ADC_CHAN0.

ADC_CHAN1	**ADC_CHAN0**	**Select the voltage comparator positive input and ADC input channel**
0	0	AIN0（P1.1）
0	1	AIN1（P1.4）
1	0	AIN2（P1.5）
1	1	AIN3（P3.2）

ADC Configuration Register (ADC_CFG):

Bit	**Name**	**Access**	**Description**	**Reset Value**
[7:4]	Reserved	RO	Reserved	0000b
3	ADC_EN	RW	ADC module power control bit, the bit is 0 to turn off the ADC module power to sleep; the bit is 1 to open	0
2	CMP_EN	RW	Voltage comparator power control bit, the bit is 0 to turn off the voltage comparator power to	0

			sleep; the bit is 1 to open	
1	Reserved	RO	Reserved	0
0	ADC_CLK	RW	ADC reference clock frequency select bit, this bit is 0 Select slow clock, 384 Fosc cycles per ADC; this bit is 1 Select fast clock, each ADC requires 96 Fosc cycles	0

ADC Data Register (ADC_DATA):

Bit	**Name**	**Access**	**Description**	**Reset Value**
[7:0]	ADC_DATA	RO	ADC sampling result data	xxh

15.3 ADC Function

ADC sampling mode configuration steps:

1. Set the ADC_EN bit in the ADC_CFG register to 1, turn on the ADC module, and set the bADC_CLK selection frequency.
2. Set ADC_CHAN1 / 0 in the ADC_CTRL register to select the input channel.
3. Optionally, clear the interrupt flag ADC_IF. Optionally, if you use interrupt mode, you also need to enable interrupts there.
4. Set ADC_START in the ADC_CTRL register to start an ADC conversion.
5. Wait for ADC_START to change to 0, or set ADC_IF to 1 (if previously cleared) to indicate that the ADC conversion is complete and that the result data can be read by ADC_DATA. The data is an equal 255 input voltage relative to the VCC supply voltage. For example, the resulting data is 47, indicating that the input voltage is approximately 47/255 VCC. If the VCC power supply voltage is not certain, then another certain reference voltage value can be measured, and then the measured input voltage value and the VCC power supply voltage value can be calculated proportionally.
6. If ADC_START is set again, the next ADC conversion can be started.

Voltage comparator mode configuration steps:

1. Set the CMP_EN bit in the ADC_CFG register to 1 to turn on the voltage comparator module.
2. Set ADC_CHAN1 / 0 and CMP_CHAN in the ADC_CTRL register to select the positive and negative inputs.
3. Optional, clear flag CMP_IF.
4. The status of the CMPO bit can be queried at any time to get the result of the current comparator.

5. If CMP_IF is changed to 1, the result of the comparator has changed.

The selected analog signal input channel must have its GPIO pin set to high impedance input mode or open drain output mode with output 1 (equivalent to high impedance input), and Pn_DIR_PU [x] = 0 and recommended Turn off the pull-up and pull-down resistors.

16. USB controller

16.1 USB Controller Introduction

CH554 embedded USB controller and USB transceiver, the characteristics are as follows:

1. Support USB Host host function and USB Device device function;
2. Support USB 2.0 full speed 12Mbps or low speed 1.5Mbps;
3. Support USB control transfer, bulk transfer, interrupt transfer, synchronous / real-time transfer;
4. Support up to 64 bytes of data packets, built-in FIFO, interrupt support and DMA.

The USB related register of CH554 is divided into 3 parts, some registers are multiplexed in the mode of the host computer and the apparatus.

1. USB global register;
2. USB device controller register;
3. USB host controller register.

16.2 Global Registers

Table 16.2.1 USB Global Registers List (Standard gray reset by bUC_RESET_SIE)

Name	**Address**	**Description**	**Reset Value**
USB_C_CTRL	91h	USB type-C Configures the channel control register	0000 0000b
USB_INT_FG	D8h	USB interrupt flag register	0010 0000b
USB_INT_ST	D9h	USB Interrupt Status Register (Read Only)	00xx xxxxb
USB_MIS_ST	DAh	USB Miscellaneous Status Register (read only)	Xx10 1000b
USB_RX_LEN	DBh	USB Receive Length Register (read only)	0xxx xxxxb
USB_INT_EN	E1h	USB interrupt enable register	0000 0000b
USB_CTRL	E2h	USB control register	0000 0110b
USB_DEV_AD	E3h	USB device address register	0000 0000b

USB type-C Configuration Channel Control Register (USB_C_CTRL):

Bit	Name	Access	Description	Reset Value
7	bVBUS2_PD_EN	RW	This bit is set to 1 to enable the internal 10K pull-down resistor on the VBUS2 pin. Disable to 0	0
6	bUCC2_PD_EN	RW	This bit is 1 to enable the internal 5.1K pull-down resistor on the UCC2 pin. Disable to 0	0
5	bUCC2_PU1_EN	RW	This bit is the internal pull-up resistor control select high for the UCC2 pin	0
4	bUCC2_PU0_EN	RW	This bit is the internal pull-up resistor control select low for the UCC2 pin	0
3	bVBUS1_PD_EN	RW	This bit is set to 1 to enable the internal 10K pull-down resistor on the VBUS1 pin. 0 is not allowed	0
2	bUCC1_PD_EN	RW	This bit is set to 1 to enable the internal 5.1K pull-down resistor on the UCC1 pin. Disable to 0	0
1	bUCC1_PU1_EN	RW	This bit is the internal pull-up resistor control select high for the UCC1 pin	0
0	bUCC1_PU0_EN	RW	This bit is the internal pull-up resistor control select low for the UCC1 pin	0

The pull-up resistor internal to the UCCn pin is selected by bUCCn_PU1_EN and bUCCn_PU0_EN.

bUCCn_PU1_EN	bUCCn_PU0_EN	Select the internal pull-up resistor on the UCCn pin
0	0	Internal pull-up resistor is disabled
0	1	Enable internal 56KΩ pull-up resistor to provide default USB current
1	0	Enable internal 22KΩ pull-up resistor, said it can provide 1.5A current
1	1	Enable internal 10KΩ pull-up resistor, which can provide 3A current

The above USB type-C pull-up and pull-down resistors are independent of the port pull-up resistors controlled by the Pn_DIR_PU port direction control and pull-up enable register. When a pin is used for USB type-C, the pin corresponding to this pin should be disabled As a port pull-up resistor, it is recommended to enable high-impedance input mode for this pin (to prevent this pin from outputting a low level or high level).
For detailed control and input detection of USB type-C configuration channels, refer to USB type-C Application Notes and Routines

USB Interrupt Flag Register (USB_INT_FG):

Bit	Name	Access	Description	Reset Value
7	U_IS_NAK	RO	In USB device mode, a 1 indicates that a NAK	0

			busy response was received during the current USB transfer. A 0 indicates that a non-NAK response was received	
6	U_TOG_OK	RO	The current USB transmission DATA0 / 1 synchronization flag match status, the bit is 1 that synchronization, the data is valid; the bit is 0 that does not synchronize, the data may be invalid	0
5	U_SIE_FREE	RO	USB protocol processor idle status bit, this bit is 0 for busy, USB transfer is in progress; this bit is 1 for USB free	1
4	UIF_FIFO_OV	RW	USB FIFO Overflow Interrupt Flag bit, this bit is 1 for FIFO overflow interrupt; this bit is 0 for no interrupt. Direct bit access to clear or write a clear zero	0
3	UIF_HST_SOF	RW	USB host mode SOF timer interrupt flag, the bit is 1, said the SOF timer interrupt, the interrupt is triggered by the SOF packet transfer is complete; the bit is 0 means no interruption. Direct bit access to clear or write a clear zero	0
2	UIF_SUSPEND	RW	The USB bus suspends or wakes up the event interrupt flag bit. When this bit is set to 1, it indicates that there is an interrupt triggered by a USB suspend event or a wake-up event. A 0 indicates no interruption. Direct bit access to clear or write a clear zero	0
1	UIF_TRANSFER	RW	The USB Transfer Complete Interrupt Flag bit, when set to 1, indicates an interrupt that is triggered by a USB transfer completion; a 0 indicates no interruption. Direct bit access to clear or write a clear zero	0
0	UIF_DETECT	RW	In USB host mode, the USB device connects or disconnects the event interrupt flag bit. When this bit is set to 1, it indicates that there is an interrupt which is triggered by detecting the USB device being connected or disconnected. A value of 0 indicates no interruption. Direct bit access to clear or write a clear zero	0
0	UIF_BUS_RST	RW	USB device interrupt USB interrupt event flag bit, the bit indicates an interrupt, the interrupt triggered by the USB bus reset event; the bit is 0 for no interruption. Direct bit access to clear or write a clear zero	0

USB Interrupt Status Register (USB_INT_ST):

Bit	Name	Access	Description	Reset Value
7	bUIS_IS_NAK	RO	In USB device mode, a 1 indicates that a NAK BUSY response was received during the current USB transfer. With U_IS_NAK	0
6	bUIS_TOG_OK	RO	The current USB transmission DATA0 / 1 synchronization flag match status, the bit is 1 that synchronization; the bit is 0 that does not sync. With U_TOG_OK	0
5	bUIS_TOKEN1	RO	The Token PID ID of the current USB transfer transaction in device mode is high	x
4	bUIS_TOKEN0	RO	Token PID identification low for current USB transfer transaction in device mode	x
[3:0]	MASK_UIS_ENDP	RO	USB device mode current USB transfer transaction endpoint number, 0000 represents the endpoint 0; ...; 1111 represents the endpoint 15	xxxxb
[3:0]	MASK_UIS_H_RES	RO	USB host mode response to the current USB transaction PID identification, 0000 means no response or timeout device; Other values that the response PID	xxxxb

bUIS_TOKEN1 and bUIS_TOKEN0 make up MASK_UIS_TOKEN for the token PID identifying the current USB transaction in USB device mode: 00 means OUT packet; 01 means SOF packet; 10 means IN packet; 11 means SETUP packet.

USB Miscellaneous Status Register (USB_MIS_ST):

Bit	Name	Access	Description	Reset Value
7	bUMS_SOF_PRES	RO	USB host mode SOF packet indicates the status bit, the bit is 1 that will send SOF packet, at this time if there are other USB packets will be automatically delayed	x
6	bUMS_SOF_ACT	RO	USB host mode SOF packet transmission status, the bit is 1 SOF packet is being sent; this bit is 0, said the transmission is complete or idle	x
5	bUMS_SIE_FREE	RO	USB protocol processor idle status bit, the bit is 0 for busy, ongoing USB transmission; the bit is 1 that USB free. With U_SIE_FREE	1
4	bUMS_R_FIFO_RDY	RO	USB receive FIFO data ready status bit, this bit is 0 indicates that the receive FIFO is empty; the bit is 1 that the receive FIFO is not	0

			empty	
3	bUMS_BUS_RESET	RO	USB bus reset status bit, this bit is 0 that there is no USB bus reset; the bit is 1 that is currently USB bus reset	1
2	bUMS_SUSPEND	RO	USB suspend status bit, this bit is 0 indicates that the current USB activity; the bit is 1 that there has been no USB activity for a period of time, the request to suspend	0
1	bUMS_DM_LEVEL	RO	The state of the DM pin when the USB device is connected to the USB port is recorded in the USB host mode, and 0 indicates a low level and 1 indicates a high level. Used to determine full speed or low speed	0
0	bUMS_DEV_ATTACH	RO	USB host mode USB device connection status bit, the bit is 1 that the port has been connected to the USB device; the bit is 0 means no	0

USB Receive Length Register (USB_RX_LEN):

Bit	**Name**	**Access**	**Description**	**Reset Value**
[7:0]	bUSB_RX_LEN	RO	The current number of bytes of data received by the USB endpoint	xxh

USB Interrupt Enable Register (USB_INT_EN):

Bit	**Name**	**Access**	**Description**	**Reset Value**
7	bUIE_DEV_SOF	RW	This bit is set to 1 to enable USB device mode receive SOF packet interrupt; disable to 0	0
6	bUIE_DEV_NAK	RW	This bit is 1 Enable USB Device Mode Receive NAK interrupt; 0 disable	0
5	Reserved	RO	Reserved	0
4	bUIE_FIFO_OV	RW	This bit enables a FIFO overflow interrupt. This bit is set to 0 to disable	0
3	bUIE_HST_SOF	RW	This bit is 1 to enable USB host mode SOF timer interrupt;	0
2	bUIE_SUSPEND	RW	This bit is 1 to enable USB bus suspend or wake event interrupt; 0 is disabled	0
1	bUIE_TRANSFER	RW	This bit is 1 to enable USB transfer complete interrupt; this bit is 0 disable	0

0	bUIE_DETECT	RW	This bit is set to 1 to enable USB device connection or disconnect event interrupt in USB host mode;	0
0	bUIE_BUS_RST	RW	This bit is set to 1 to enable the USB bus event interrupt in USB device mode; this bit is disabled	0

USB Control Register (USB_CTRL):

Bit	**Name**	**Access**	**Description**	**Reset Value**
7	bUC_HOST_MODE	RW	USB operation mode select bit, this bit is 0 to select USB device mode (DEVICE); this bit is 1 to select USB host mode (HOST)	0
6	bUC_LOW_SPEED	RW	USB bus signal transmission rate select bit, this bit is 0 to select full speed 12Mbps; this bit is 1 to select low speed 1.5Mbps	0
5	bUC_DEV_PU_EN	RW	USB device enable and internal pull-up resistor control bits in USB device mode, setting this bit to 1 enables USB device transfer and enables the internal pull-up resistor	0
5	bUC_SYS_CTRL1	RW	USB system control high	0
4	bUC_SYS_CTRL0	RW	USB system control low	0
3	bUC_INT_BUSY	RW	USB transfer complete interrupt flag is not cleared before the automatic pause enable bit, the bit is 1 in the interrupt flag UIF_TRANSFER not cleared before automatically suspended for the device mode will automatically busy NAK, for the host mode will automatically suspend subsequent transmission; the Bit 0 is not suspended	0
2	bUC_RESET_SIE	RW	USB protocol processor software reset control bit, the bit is forced to reset the USB protocol processor and most of the USB control registers, the need to clear the software	1
1	bUC_CLR_ALL	RW	This bit is cleared by 1 to clear the USB interrupt flag and FIFO and requires software reset	1
0	bUC_DMA_EN	RW	This bit is 1 to enable USB DMA and DMA interrupts; 0 is disabled	0

Composed of bUC_HOST_MODE, bUC_SYS_CTRL1, and bUC_SYS_CTRL0 USB system control combination:

bUC_HOST_MODE	**bUC_SYS_CTRL1**	**bUC_SYS_CTRL0**	**USB system control description**

0	0	0	Disable USB device function, turn off the internal pull-up resistor
0	0	1	Enable USB device function, turn off internal pull-up, need to add external pull-up
0	1	X	Enable USB device function, enable internal 1.5KΩ pull-up resistor. This pull-up resistor takes precedence over the pull-down resistor and can also be used in GPIO mode
1	0	0	Select USB host mode, normal working condition
1	0	1	Select USB host mode, force DP / DM output SE0 state
1	1	0	Select USB host mode, force the DP / DM output J state
1	1	1	Select USB host mode, force DP / DM output K state / wake up

USB Device Address Register (USB_DEV_AD):

Bit	Name	Access	Description	Reset Value
7	bUDA_GP_BIT	RW	USB universal flag: Users can customize, software can be cleared or set	0
[6:0]	MASK_USB_ADDR	RW	Host mode is the address of the current operating USB device; Device mode is the address of the USB device	00h

16.3 Device Register

In USB device mode, CH554 provides 5 groups of bidirectional endpoints of 0, 1, 2, 3 and 4, and the maximum data packet length of all endpoints is 64 bytes.

Endpoint 0 is the default endpoint that supports control transfers, sending and receiving share a 64-byte data buffer.

Endpoint 1, Endpoint 2 and Endpoint 3 each include a transmit endpoint IN and a receive endpoint OUT, each having an independent 64-byte or double 64-byte data buffer for sending and receiving, supporting control transfers, bulk transfers, interrupt transfers and Real-time / synchronous transmission

Endpoint 4 includes a transmit endpoint IN and a receive endpoint OUT, sending and receiving each have a separate 64-byte data buffer, support control transfer, bulk transfer, interrupt transfer and real-time / synchronous transfer.

Each set of endpoints has a control register, UEPn_CTRL, and a transmit length register, UEPn_T_LEN (n = 0/1/2/3/4), for setting the synchronization trigger bit for this endpoint, responding to OUT transactions and IN transactions, and sending data Length and so on.

The USB bus pull-up resistor necessary as a USB device can be set by the software at any time. When the bUC_DEV_PU_EN in the USB control register USB_CTRL is set to 1, the CH554 internally pulls up the DP pin or the DM pin of the USB bus according to bUD_LOW_SPEED Resistor and enable USB device function.

After detecting the USB bus reset, USB bus suspend or wake-up event, or USB successfully finishes sending data or receiving data, the USB protocol processor will set the corresponding interrupt flag and generate an interrupt request. The application can directly query or query and analyze the interrupt flag register USB_INT_FG in the USB interrupt service routine and perform the corresponding processing according to UIF_BUS_RST and UIF_SUSPEND; and if the UIF_TRANSFER is valid, the USB interrupt status register USB_INT_ST needs to be further analyzed, and according to the current endpoint number MASK_UIS_ENDP and the current transaction token PID identifier MASK_UIS_TOKEN for the appropriate treatment. If the synchronization trigger bit bUEP_R_TOG of the OUT transaction of each endpoint is set in advance, whether the synchronization trigger bit of the currently received data packet matches the synchronization trigger bit of the endpoint can be determined by U_TOG_OK or bUIS_TOG_OK. If the data is synchronized, the data Effective; if the data is not synchronized, the data should be discarded. After each processing USB send or receive interrupt, it should correctly modify the corresponding endpoint synchronization trigger bit, used to synchronize the next data packet sent and detect the next received data packet is synchronized; In addition, by setting bUEP_AUTO_TOG Achieve the success of the transmission or receive success automatically flip the corresponding synchronization trigger bit.

The data to be sent by each endpoint is in its own buffer, the length of the data to be sent is set independently in UEPn_T_LEN; the data received by each endpoint is in its own buffer, but the received data length is within the USB receive length Register USB_RX_LEN, USB receiver can be interrupted according to the current endpoint number distinction.

Table 16.3.1 USB Device Related Registers List (Standard gray reset by bUC_RESET_SIE)

Name	**Address**	**Description**	**Reset Value**
UDEV_CTRL	D1h	USB device physical port control register	10xx 0000b
UEP1_CTRL	D2h	Endpoint 1 control register	0000 0000b
UEP1_T_LEN	D3h	Endpoint 1 send length register	0xxx xxxxb
UEP2_CTRL	D4h	Endpoint 2 control register	0000 0000b
UEP2_T_LEN	D5h	Endpoint 2 send length register	0000 0000b

UEP3_CTRL	D6h	Endpoint 3 control register	0000 0000b
UEP3_T_LEN	D7h	Endpoint 3 send length register	0xxx xxxxb
UEP0_CTRL	DCh	Endpoint 0 control register	0000 0000b
UEP0_T_LEN	DDh	Endpoint 0 send length register	0xxx xxxxb
UEP4_CTRL	DEh	Endpoint 4 control register	0000 0000b
UEP4_T_LEN	DFh	Endpoint 4 send length register	0xxx xxxxb
UEP4_1_MOD	EAh	Endpoint 1, 4 mode control register	0000 0000b
UEP2_3_MOD	EBh	Endpoint 2, 3 mode control register	0000 0000b
UEP0_DMA_H	EDh	Endpoint 0 and 4 buffer start address high byte	0000 00xxb
UEP0_DMA_L	ECh	Endpoint 0 and 4 buffer start address low byte	xxxx xxxxb
UEP0_DMA	ECh	UEP0_DMA_L and UEP0_DMA_H form a 16-bit SFR	0xxxh
UEP1_DMA_H	DFh	Endpoint 1 buffer start address high byte	0000 00xxb
UEP1_DMA_L	EEh	Endpoint 1 buffer start address low byte	xxxx xxxxb
UEP1_DMA	EEh	UEP1_DMA_L and UEP1_DMA_H form a 16-bit SFR	0xxxh
UEP2_DMA_H	E5h	Endpoint 2 buffer start address high byte	0000 00xxb
UEP2_DMA_L	E4h	Endpoint 2 buffer start address low byte	xxxx xxxxb
UEP2_DMA	E4h	UEP2_DMA_L and UEP2_DMA_H form a 16-bit SFR	0xxxh
UEP3_DMA_H	E7h	Endpoint 3 buffer start address high byte	0000 00xxb
UEP3_DMA_L	E6h	Endpoint buffer start address low byte	xxxx xxxxb
UEP3_DMA	E6h	UEP3_DMA_L and UEP3_DMA_H form a 16-bit SFR	0xxxh

USB Device Physical Port Control Register (UDEV_CTRL), controlled by bUC_RESET_SIE Reset:

Bit	**Name**	**Access**	**Description**	**Reset Value**
7	bUD_PD_DIS	RW	USB Device Port UDP / UDM Pin Internal Pull-down Resistor Disable bit. This bit disables the internal pull-down resistor. Setting this bit to 0 enables the internal pull-down resistor. This bit is not controlled by bUSB_IO_EN and can also be used to provide pull-down resistors in GPIO mode	1
6	Reserved	RO	Reserved	0
5	bUD_DP_PIN	RO	Current UDP pin state, 0 means low; 1 means high	x
4	bUD_DM_PIN	RO	Current UDM pin state, 0 for low; 1 for high	x
3	Reserved	RO	Reserved	0
2	bUD_LOW_SPEED	RW	USB device physical port low speed mode	0

			enable bit, this bit is 1 to select 1.5Mbps low speed mode; this bit is 0 to select 12Mbps full speed mode	
1	bUD_GP_BIT	RW	USB device mode common flag: the user can define their own, software can be cleared or set	0
0	bUD_PORT_EN	RW	USB device physical port enable bit, this bit is 1 to enable the physical port; this bit is 0 to disable the physical port	0

Endpoint n Control Register (UEPn_CTRL):

Bit	**Name**	**Access**	**Description**	**Reset Value**
7	bUEP_R_TOG	RW	The desired synchronization trigger for the receiver of the USB endpoint n (handling SETUP / OUT transactions), which indicates that DATA0 is expected; a value of 1 indicates the expected DATA1	0
6	bUEP_T_TOG	RW	USB endpoint n transmitter (processing IN transaction) to prepare the synchronization trigger bit, the bit is 0 to send DATA0; 1 to send DATA1	0
5	Reserved	RO	Reserved	0
4	bUEP_AUTO_TOG	RW	Synchronous trigger bit automatically flip enable control bit, the bit is 1, said the success of the transmission or receive the appropriate flip automatically flip the corresponding trigger bit; 0 means not automatically flip, but you can manually switch. Only endpoints 1/2/3 are supported	0
3	bUEP_R_RES1	RW	The receiver of endpoint n controls the SETUP / OUT transaction in response to a high order	0
2	bUEP_R_RES0	RW	The receiver of endpoint n controls the SETUP / OUT transaction in response to the low order	0
1	bUEP_T_RES1	RW	The response of the sender of endpoint n to IN transaction is high	0
0	bUEP_T_RES0	RW	The response of the sender of endpoint n to the IN transaction is controlled low	0

MASK_UEP_R_RES consisting of bUEP_R_RES1 and bUEP_R_RES0 Controls how the receiver of endpoint n responds to the SETUP / OUT transaction: 00 for ACK or Ready; 01 for timeout / no response for real-time / synchronous transfer of non-endpoint 0; 10 means answering NAK or busy; 11 means answering STALL or error.

MASK_UEP_T_RES, consisting of bUEP_T_RES1 and bUEP_T_RES0, is used to control how the sender of endpoint n responds to an IN transaction: 00 means DATA0 / DATA1 or data ready and expected ACK; 01 means DATA0 / DATA1 is acknowledged and expect no response for non- Endpoint 0 real-time / synchronous transmission; 10 means NAK or busy; 11 means STALL or error.

[remainder of 16.3 omitted]

16.4 Host Register

In USB host mode, the CH554 provides a set of bidirectional host endpoints including a transmit endpoint OUT and a receive endpoint IN. The maximum packet length is 64 bytes and supports control transfers, bulk transfers, interrupt transfers, and real-time / synchronous transfers.

Each USB transaction initiated by the host endpoint automatically sets the interrupt flag, UIF_TRANSFER, at the end of processing. The application can directly query or query and analyze the interrupt flag register USB_INT_FG in the USB interrupt service routine, and perform corresponding processing according to each interrupt flag. Moreover, if the UIF_TRANSFER is valid, the USB interrupt status register USB_INT_ST needs to be further analyzed, and the current USB The reply transaction identifier MASK_UIS_H_RES of the transaction is processed accordingly.

If a host receives the synchronization trigger bit bUH_R_TOG of the IN transaction of the receiving endpoint, it can determine whether the synchronization trigger bit of the currently received data packet matches the synchronization trigger bit of the host receiving endpoint by using U_TOG_OK or bUIS_TOG_OK. If the data is synchronized, The data is valid; if the data is out of sync, the data should be discarded. After each processing USB send or receive interrupt, should correct the corresponding host endpoint synchronization trigger bit, used to synchronize the next data packet sent and detect the next received data packet is synchronized; In addition, by setting bUEP_AUTO_TOG Can be achieved after the success of the transmission or receive the success of the corresponding automatic flip synchronization trigger bit.

The USB host token setting register UH_EP_PID is a multiplexing of USB endpoint 1 control registers in USB device mode and is used to set the endpoint number of the target device to be operated and the Token PID packet identifier of this USB transfer transaction. Data corresponding to the SETUP token and the OUT token are provided by the host sending endpoint. The data to be sent is in the UH_TX_DMA buffer and the data length to be sent is set in UH_TX_LEN. The data corresponding to the IN token is returned by the target device to the host Receiving endpoint, the received data is stored in the UH_RX_DMA buffer and the received data length is stored in USB_RX_LEN.

Table 16.4.1 USB Host Related Registers List (Standard gray reset by bUC_RESET_SIE)

Name	Address	Description	Reset Value
UHOST_CTRL	D1h	USB host physical port control register	10xx 0000b
UH_SETUP	D2h	USB Host Auxiliary Setting Register	0000 0000b
UH_RX_CTRL	D4h	USB host receive endpoint control register	0000 0000b

UH_EP_PID	D5h	USB host token setting register	0000 0000b
UH_TX_CTRL	D6h	USB host sends endpoint control register	0000 0000b
UH_TX_LEN	D7h	USB host send length register	0xxx xxxxb
UH_EP_MOD	EBh	USB host endpoint mode control register	0000 0000b
UH_RX_DMA_H	E5h	USB host receive buffer start address high byte	0000 00xxb
UH_RX_DMA_L	E4h	USB host receive buffer start address low byte	xxxx xxxxb
UH_RX_DMA	E4h	The 16-bit SFRs are composed of UH_RX_DMA_L and UH_RX_DMA_H	0xxxh
UH_TX_DMA_H	E7h	USB host send buffer start address high byte	0000 00xxb
UH_TX_DMA_L	E6h	USB host send buffer start address low byte	Xxxx xxxxb
UH_TX_DMA	E6h	The 16-bit SFR consists of UH_TX_DMA_L and UH_TX_DMA_H	0xxxh

USB host physical port control register (UHOST_CTRL), reset control by bUC_RESET_SIE:

Bit	Name	Access	Description	Reset Value
7	bUH_PD_DIS	RW	USB Host Port UDP / UDM Pin Internal Pull-down Resistor Disable bit. This bit disables the internal pull-down resistor. Setting this bit to 0 enables the internal pull-down resistor. This bit is not controlled by bUSB_IO_EN and can also be used to provide pull-down resistors in GPIO mode	1
6	Reserved	RO	Reserved	0
5	bUH_DP_PIN	RO	Current UDP pin state, 0 means low; 1 means high	x
4	bUH_DM_PIN	RO	Current UDM pin state, 0 for low; 1 for high	x
3	Reserved	RO	Reserved	0
2	bUH_LOW_SPEED	RW	USB host physical port low speed mode enable bit, this bit is 1 to select 1.5Mbps low speed mode; this bit is 0 to select 12Mbps full speed mode	0
1	bUH_BUS_RESET	RW	USB host port bus reset control bit, this bit is 1 to force the host port to output USB bus reset; this bit is 0 to end output	0
0	bUH_PORT_EN	RW	USB Host Port Enable bit, this bit disables the host port by 0; this bit enables the host port by 1. This bit is automatically cleared when the USB device is disconnected	0

USB Host Auxiliary Setup Register (UH_SETUP):

Bit	Name	Access	Description	Reset Value

7	bUH_PRE_PID_EN	RW	Low Preamble Packet PRE PID enable bit, this bit is 1 Enable USB host to communicate with low-speed USB device through external HUB; Disable low-speed leading packet to 0, HUB not between USB host and low-speed USB device	0
6	bUH_SOF_EN	RW	Automatically generated SOF packet enable bit, the bit is automatically generated by the USB host SOF packet; 0 is not automatically generated, but can be generated by hand	0
[5:0]	Reserved	RO	Reserved	00h

USB Host Receive Endpoint Control Register (UH_RX_CTRL):

Bit	**Name**	**Access**	**Description**	**Reset Value**
7	bUH_R_TOG	RW	USB host receiver (handling IN transaction) expected synchronization trigger bit, the bit is 0 indicates the expected DATA0; 1 indicates the expected DATA1	0
[6:5]	Reserved	RO	Reserved	00b
4	bUH_R_AUTO_TOG	RW	Automatically turn bUH_R_TOG enable control bit, the bit is 1 that the USB host automatically flip the bUH_R_TOG flag after receiving the success; 0 means that does not automatically flip, but you can manually switch	0
3	Reserved	RO	Reserved	0
2	bUH_R_RES	RW	USB host receiver response to IN transaction control bit, 0 means ACK or Ready; 1 means no response for non-endpoint 0 with the target device for real-time / synchronous transmission	0
[1:0]	Reserved	RO	Reserved	00b

USB Host Token Setting Register (UH_EP_PID):

Bit	**Name**	**Access**	**Description**	**Reset Value**
[7:4]	MASK_UH_TOKEN	RW	Set the Token PID packet identifier of this USB transfer transaction	0000b
[3:0]	MASK_UH_ENDP	RW	Set the endpoint number of the target device to be operated this time	0000b

USB Host Transmit Endpoint Control Register (UH_TX_CTRL):

Bit	Name	Access	Description	Reset Value
7	Reserved	RO	Reserved	0
6	bUH_T_TOG	RW	USB host transmitter (processing SETUP / OUT transaction) to prepare the synchronization trigger bit, the bit is 0 to send DATA0; 1 to send DATA1	0
5	Reserved	RO	Reserved	0
4	bUH_T_AUTO_TOG	RW	Automatically flip bUH_T_TOG enable control bit, the bit is 1 means that the USB host automatically sends the bUH_T_TOG flag after it is successfully sent; 0 means it does not automatically flip, but it can be manually switched	0
[3:1]	Reserved	RO	Reserved	000b
0	bUH_T_RES	RW	The USB host transmitter's response control bit to the SETUP / OUT transaction, 0 to indicate expected response ACK or ready; 1 to indicate no response expected, for real-time / synchronous transfer with non-endpoint 0 of the target device	0

USB Host Transmit Length Register (UH_TX_LEN):

Bit	Name	Access	Description	Reset Value
[7:0]	UH_TX_LEN	RW	Set the number of bytes of data to be sent by the USB host to send the endpoint	xxh

USB Host Endpoint Mode Control Register (UH_EP_MOD):

Bit	Name	Access	Description	Reset Value
7	Reserved	RO	Reserved	0
6	bUH_EP_TX_EN	RW	This bit is 0 to disable the USB host from sending data to the endpoint. This bit is set to 1 to enable the USB host to send data to the endpoint (SETUP / OUT)	0
5	Reserved	RO	Reserved	0
4	bUH_EP_TBUF_MOD		The USB host sends the endpoint data buffer mode control bit	0
3	bUH_EP_RX_EN		This bit is 0 to disable USB host receive endpoint receive data; this bit is 1 to enable USB host receive endpoint receive data (IN)	0

[2:1]	Reserved	RO	Reserved	00b
0	bUH_EP_RBUF_MOD	RW	The USB host receives the endpoint data buffer mode control bit	0

The combination of bUH_EP_TX_EN and bUH_EP_TBUF_MOD controls the USB host to send endpoint data buffer mode, refer to the following table.

Table 16.4.2 Host Transmit Buffer Modes

bUH_EP_TX_EN	**bUH_EP_TBUF_MOD**	**Structure Description: Starting address UH_TX_DMA**
0	x	Endpoints are disabled and no UH_TX_DMA buffer is used
1	0	Single 64-byte send buffer (SETUP / OUT)
1	1	Double 64 bytes send buffer, select by bUH_T_TOG: Select the first 64 bytes of buffer when bUH_T_TOG = 0; When bUH_T_TOG = 1, select the last 64 bytes of buffer

The combination of bUH_EP_RX_EN and bUH_EP_RBUF_MOD controls the USB host receive endpoint data buffer mode, refer to the following table.

Table 16.4.3 Host Receive Buffer Modes

bUH_EP_RX_EN	**bUH_EP_RBUF_MOD**	**Structure Description: Starting address UH_RX_DMA**
0	x	Endpoints are disabled and no UH_RX_DMA buffer is used
1	0	Single 64-byte send buffer (IN)
1	1	Double 64 bytes send buffer, select by bUH_R_TOG: Select the first 64 bytes of buffer when bUH_R_TOG = 0; When bUH_R_TOG = 1, select the last 64 bytes of buffer

USB host receive buffer start address (UH_RX_DMA):

Bit	**Name**	**Access**	**Description**	**Reset Value**
[7:0]	UH_RX_DMA_H	RW	USB host receiver buffer high byte start address, only the lower 2 effective, high 6 fixed to 0	0xh
[7:0]	UH_RX_DMA_L	RO	USB host receive buffer start address low byte	xxh

USB host then send red zone start address (UH_TX_DMA):

Bit	Name	Access	Description	Reset Value
[7:0]	UH_TX_DMA_H	RW	USB host send buffer high byte start address, only the lower 2 effective, high 6 fixed to 0	0xh
[7:0]	UH_TX_DMA_L	RO	USB host send buffer start address low byte	xxh

17. Touch-Key

17.1 Introduction to Touch-Key

CH554 chip provides capacitance detection module and related timers, with 6 input channels, supporting capacitance range 5pF ~ 150pF. Self capacitance mode can support up to 6 touch keys, mutual capacitance mode can support up to 15 touch keys.

17.2 Touch-Key register

Table 17.2.1 Touch-Key related register list

Name	Address	Description	Reset Value
TKEY_CTRL	C3h	Touch-Key control register	x0h
TKEY_DATH	C5h	Touch-Key Data High Byte (Read Only)	00h
TKEY_DATL	C4h	Touch-Key Data Low Byte (Read Only)	xxh
TKEY_DAT	C4h	TKEY_DATL and TKEY_DATH form a 16-bit SFR	00xxh

Touch-Key Control Register (TKEY_CTRL):

Bit	Name	Access	Description	Reset Value
7	bTKC_IF	RW	Timer interrupt flag. If bTKD_CHG = 0, the request interrupt is automatically set at the end of the current timing period, automatically cleared when the preparation phase ends, or cleared by writing TKEY_CTRL. Auto-clear if bTKD_CHG = 1, do not request interrupts, skip the current cycle, then re-prepare and detect on the next cycle, and set the request interrupt automatically at the end of the next cycle	x
[6:5]	Reserved	RO	Reserved	00b
4	bTKC_2MS	RW	Capacitor detection timer cycle selection: 0-1mS; 1-2mS. The first 87uS per cycle is the preparation phase and the remaining time detection phase. The above time is based on the time when Fosc = 24 MHz	0

3	Reserved	RO	Reserved	0
2	bTKC_CHAN2	RW	Touch the button Capacitor Detection Input Select Low	0
1	bTKC_CHAN1	RW	Touch the button Capacitor Detection Input Select High	0
0	bTKC_CHAN0	RW	Touch the button Capacitor Detection Input Select Low	0

By bTKC_CHAN2 ~ bTKC_CHAN0 select the touch button capacitance detection input channel.

bTKC_CHAN2	**bTKC_CHAN1**	**bTKC_CHAN0**	**Select the touch button capacitance detection input channel**
0	0	0	Turn off the power of the capacitance detection module and only serve as a separate timer interrupt with a period of 1mS or 2mS
0	0	1	TIN0（P1.0）
0	1	0	TIN1（P1.1)
0	1	1	TIN2（P1.4）
1	0	0	TIN3（P1.5）
1	0	1	TIN4（P1.6）
1	1	0	TIN5（P1.7)
1	1	1	Turn on the power detection module but do not connect any channels

Touch-Key Data Register (TKEY_DAT):

Bit	**Name**	**Access**	**Description**	**Reset Value**
7	bTKD_CHG TKEY_DATH[7]	RO	Touch-Key control change flag. This bit is 1 to indicate that TKEY_CTRL has been rewritten during the capacitance detection phase. This may invalidate the TKEY_DAT data and will not set bTKC_IF at the end of the current cycle. This bit is automatically cleared at the end of the preparation phase of each timing period. The data needs to be masked	0
6	Reserved	RO	Reserved	0
[5:0]	TKEY_DATH	RO	Touch-Key data high byte. Cleared automatically at the end of the preparation phase of each timing period; counted automatically during the capacitance detection phase; held unchanged during the preparation phase so that the timing interrupt routine reads	00h

[7:0]	TKEY_DATL	RO	Touch-Key data low byte. Cleared automatically at the end of the preparation phase of each timing period; counted automatically during the capacitance detection phase; held unchanged during the preparation phase so that the timing interrupt routine reads	xxh

17.3 Touch-Key function

Capacitance detection steps:

1. Set bTKC_2MS and bTKC_CHAN2 ~ bTKC_CHAN0 in TKEY_CTRL register, select the period and input channel. The selected input channel, its GPIO pin must be set to high impedance input mode, or open drain output mode and in output 1 state (equivalent to high impedance input), Pn_DIR_PU [x] = 0.
2. Clear bTKC_IF and start the interrupt IE_TKEY Wait for the timer interrupt, or through active query bTKC_IF interrupt program.
3. The bTKC_IF request interrupt will be automatically set after the current channel capacitance detection is completed, and the preparation phase of the next cycle will be entered at the same time, and the TKEY_DAT data will remain unchanged for about 87uS
4. Into the interrupt program, first read the current channel capacitance data from TKEY_DAT, and shield the highest bTKD_CHG, the data is relative value, and the capacitance is inversely proportional to the data when the touch button is pressed than not pressed Under the data is small.
5. Set bTKC_2MS and bTKC_CHAN2 ~ bTKC_CHAN0 in the TKEY_CTRL register to select the next input channel. This write will automatically clear bTKC_IF to complete the interrupt request.
6. Compare the TKEY_DAT data read in step (4) with the previously saved data of the channel without the key to determine whether the capacitance is changed and whether any key is pressed.
7. The interrupt is returned, and when the capacitance of the next channel is detected, it will go to step (3).

18. Parameters

18.1 ABSOLUTE MAXIMUM (Critical or Exceeds Absolute Maximum will probably cause the chip to malfunction or even be damaged)

Name	Parameter Description	Min	Max	Unit

TA	System frequency Fsys less than 28MHz ambient temperature when working	-40	85	℃
TA32M	System frequency Fsys greater than 28MHz ambient temperature when working	-20	70	℃
TS	Ambient temperature when stored	-55	125	℃
VCC	Power supply voltage (VCC power supply, GND ground)	-0.4	5.8	V
VIO	Voltage on other input or output pins other than P3.6 / P3.7	-0.4	VCC+0.4	V
VIOU	P3.6 / P3.7 Input or output pin voltage	-0.4	V33+0.4	V

18.2 Electrical Specifications 5V (Test Conditions: TA = 25 ° C, VCC = 5V, Fsys = 6MHz)

Name	**Parameter Description**		**Mind**	**Typical**	**Max**	**Unit**
VCC5	VCC pin supply voltage	V33 connected to external capacitor	3.7	5	5.5	V
V33	Internal USB power regulator output voltage		3.14	3.27	3.4	V
ICC24M5	Fsys = total supply current at 24MHz operation		8	11		mA
ICC6M5	Fsys = Total operating current at 6MHz operation		4	6		mA
ICC750K5	Fsys = total supply current at 750KHz operation		2	3		mA
ISLP5	Total power supply current after sleep			0.1	.02	mA
ISLP5L	VCC = V33 = 5V, and choose the external crystal clock, and bLDO3V3_OFF = 1 turn off the LDO, the total power supply current after a complete sleep			0.008	0.02	mA
IADC5	ADC analog-digital conversion module operating current			200	800	uA
ICMP5	Voltage comparator module operating current			100	500	uA
ITKEY5	Touch button capacitance detection module operating current			150	250	uA
VIL5	Low level input voltage		-0.4		1.2	V
VIH5	High level input voltage		2.4		VCC+0.4	V
VOL5	Low level output voltage (12mA sink current)				0.4	V
VOH5	High level output voltage (8mA output current)		VCC-0.4			V
VOH5U	P3.6 / P3.7 high level output voltage (8mA output current)		V33-0.4			V

IIN	No pull-up input input current	-5	0	0	uA
IDN5	Input current with pull-down resistor input	-35	-70	-140	uA
IUP5	Input current with pull-up resistor input	35	70	140	uA
IUP5X	With pull-up input from low to high flip input current	250	400	600	uA
Vpot	Power-on reset threshold voltage	2.1	2.3	2.5	V

18.3 Electrical Specifications 3.3V (Test Conditions: TA = 25 ° C, VCC = V33 = 3.3V, Fsys = 6MHz)

Name	**Parameter Description**		**Min**	**Typical**	**Max**	**Unit**
VCC3	VCC pin supply voltage	V33 shorted to VCC, USB enabled	3.0	3.3	3.6	V
		V33 shorted to VCC, USB disabled	2.7	3.3	3.6	V
ICC16M3	Fsys = total supply current at 16MHz operation		4	6		mA
ICC6M3	Fsys = Total operating current at 6MHz operation		2	4		mA
ICC750K3	Fsys = total supply current at 750KHz operation		1	2		mA
ISLP3	Total power supply current after sleep			0.07	.15	mA
ISLP3L	VCC = V33 = 5V, and choose the external crystal clock, and bLDO3V3_OFF = 1 turn off the LDO, the total power supply current after a complete sleep			0.004	0.01	mA
IADC3	ADC analog-digital conversion module operating current			150	500	uA
ICMP3	Voltage comparator module operating current			70	300	uA
ITKEY3	Touch button capacitance detection module operating current			130	200	uA
VIL3	Low level input voltage		-0.4		0.8	V
VIH3	High level input voltage		1.9		VCC+0.4	V
VOL3	Low level output voltage (12mA sink current)				0.4	V
VOH3	High level output voltage (8mA output current)		VCC-0.4			V
VOH3U	P3.6 / P3.7 high level output voltage (8mA output current)		V33-0.4			V
IIN	No pull-up input input current		-5	0	5	uA
IDN3	Input current with pull-down resistor input		-15	-30	-60	uA
IUP3	Input current with pull-up resistor input		15	30	60	uA

IUP3X	With pull-up input from low to high flip input current	100	170	250	uA
Vpot	Power-on reset threshold voltage	2.1	2.3	2.5	V

18.4 Timing Parameters (Test Conditions: TA = 25 ° C, VCC = 5V or VCC = V33 = 3.3V, Fsys = 6MHz)

Name	**Parameter Description**	**Min**	**Typical**	**Max**	**Unit**
Fxt	External crystal frequency or XI input clock frequency	6	24	24	MHz
Fosc	Calibrated internal clock frequency at 3=3V to 3.6V	23.64	24	24.36	MHz
Fosc28	Calibrated internal clock frequency when V33=2.8V~3V	23.28	24	24.72	MHz
Fosc27	Calibrated internal clock frequency at V33=2.7V	21	24	25	MHz
Fpll	Internally multiplied PLL frequency	24	96	100	MHz
Fusb4x	USB sampling clock frequency when using the USB host function	47.98	48	48.02	MHz
	USB sampling clock frequency when using USB device function	47.04	48	48.96	MHz
Fsys	System frequency clock frequency (VCC> = 4.4V)	0.1	6	24	MHz
	System frequency clock frequency (4.4V> VCC> = 3.3V)	0.1	6	16	MHz
	System frequency clock frequency (VCC <3.3V)	0.1	6	12	MHz
Tpor	Power on reset delay	9	11	15	mS
Trst	Enter the width of the valid reset signal from outside RST	70			nS
Trdl	Thermal reset delay	30	45	60	uS
Twdc	Watchdog overflow period / timing period calculation formula	65536 * (0x100 - WDOG_COUNT) / Fsys			
Tusp	USB host mode to detect USB auto-suspend time	2	3	4	mS
	Detects USB auto-suspend time in USB device mode	4	5	6	mS
Twak	Wakeup completion time after chip sleep	1	2	10	uS