

# NALAA

## *Hamburg 10*

# LA-6041P REV 1.0 Schematic

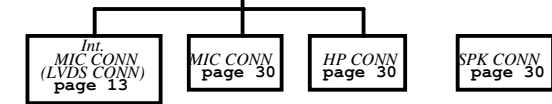
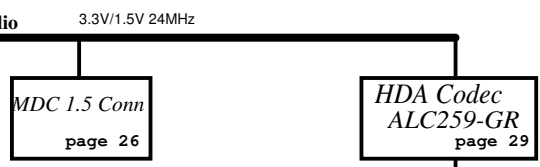
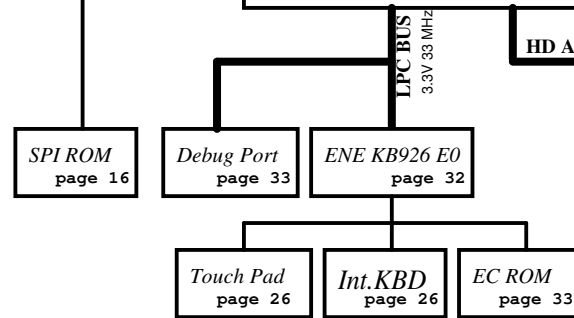
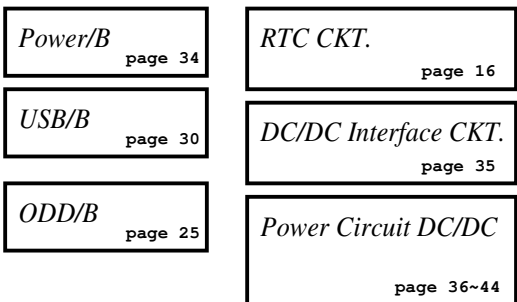
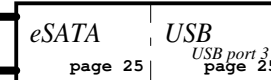
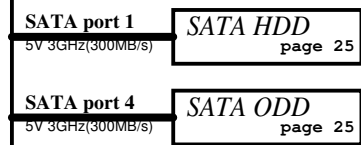
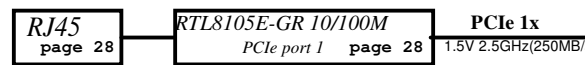
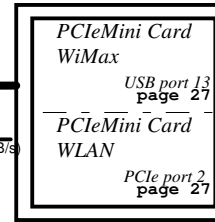
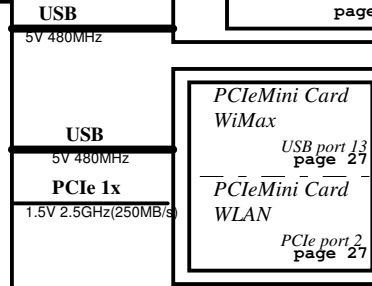
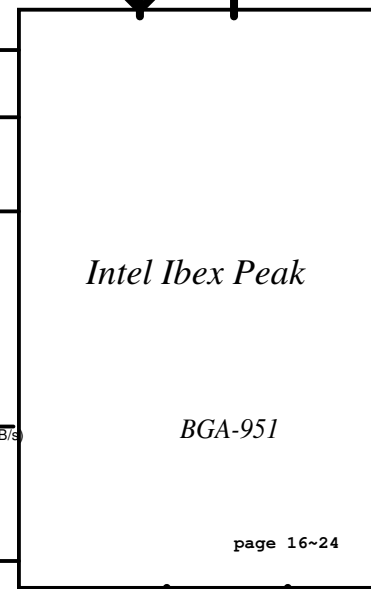
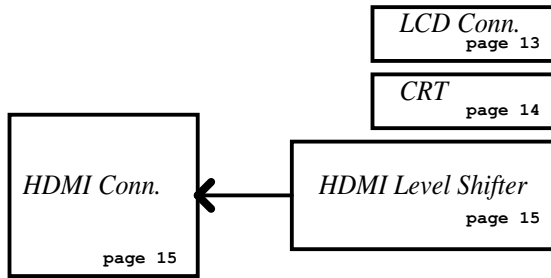
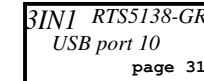
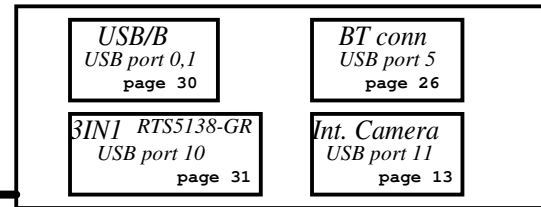
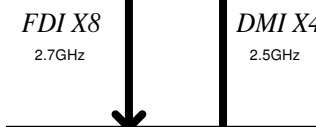
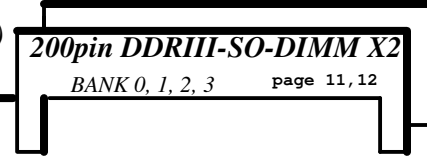
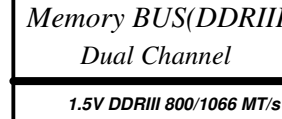
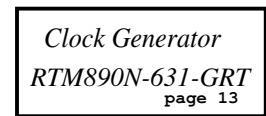
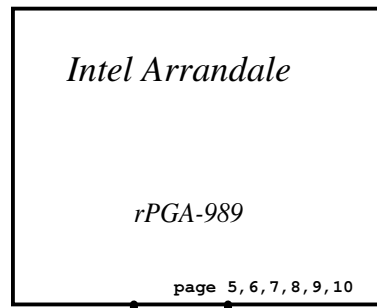
Intel Arrandale /IBEX PEAK

2009-10-01 Rev 1.0

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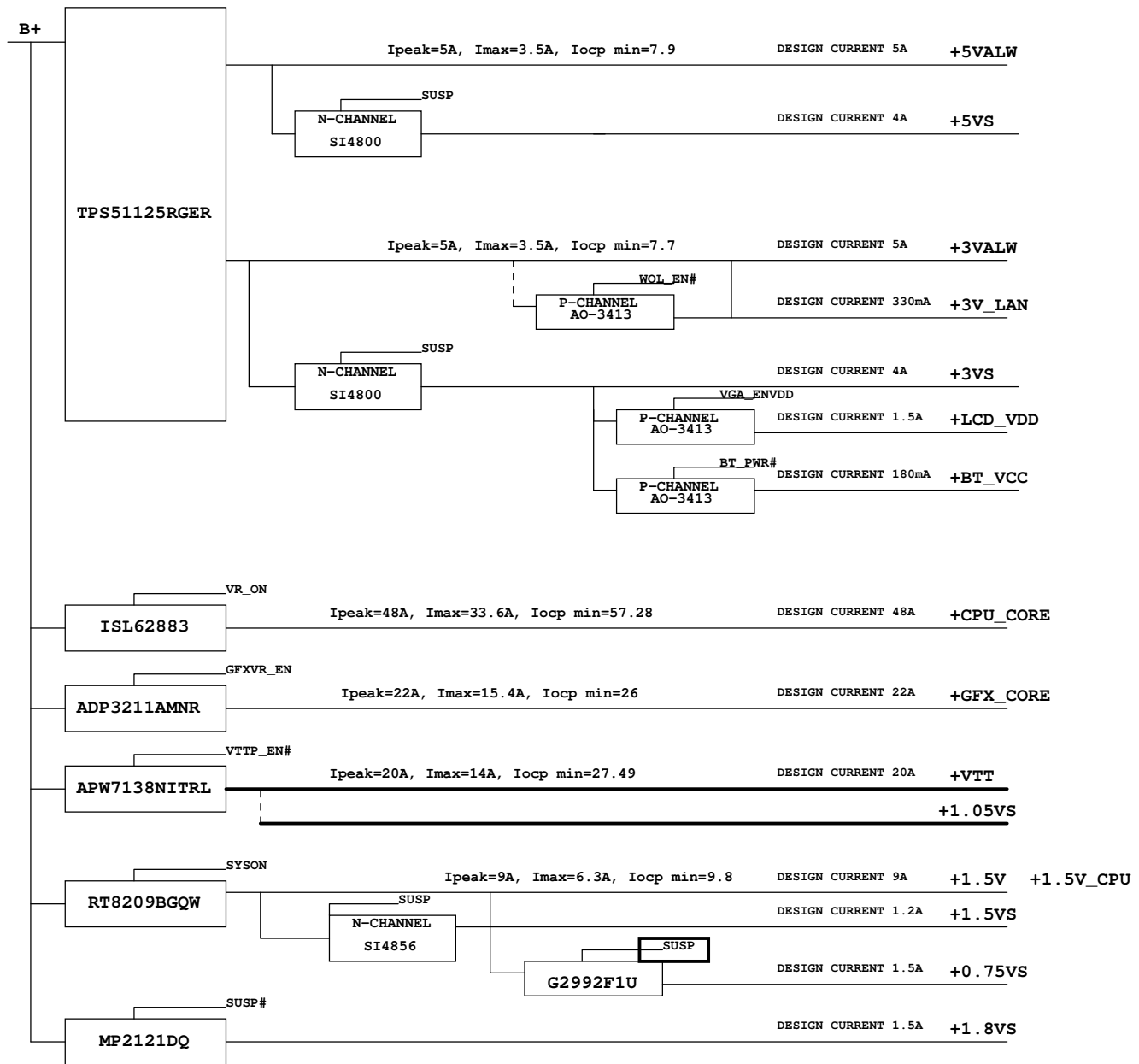
# Compal Confidential

Model Name : NALAA  
File Name : LA-6041P



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NALAA Hamburg Intel Arrandale (UMA)



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### Voltage Rails

( O MEANS ON X MEANS OFF )

power plane / State	+RTCVCC	+B	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

### BTO Option Table

Function	Bluetooth	RJ11	LAN	HDMI	Card Reader	Express Card	Mini Card
description	(B)	(R)	(E)	(Y)	(W)		
explain	Bluetooth	MDC	LAN	HDMI	Card Reader	New Card	PCMCIA WIRELESS
BTO	BT@	MDC@		IHDMI@	CARD@		WLAN@

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

### EC SM Bus1 address

### EC SM Bus2 address

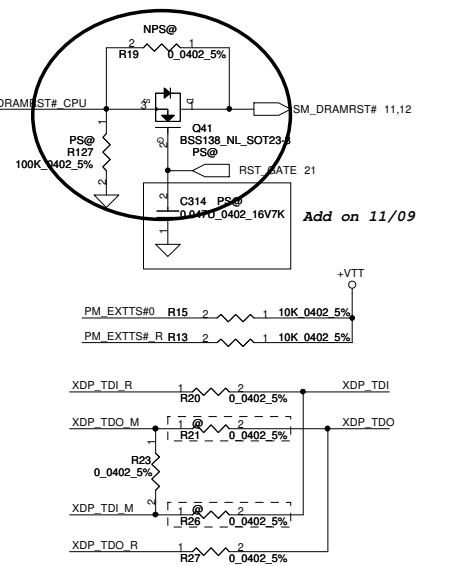
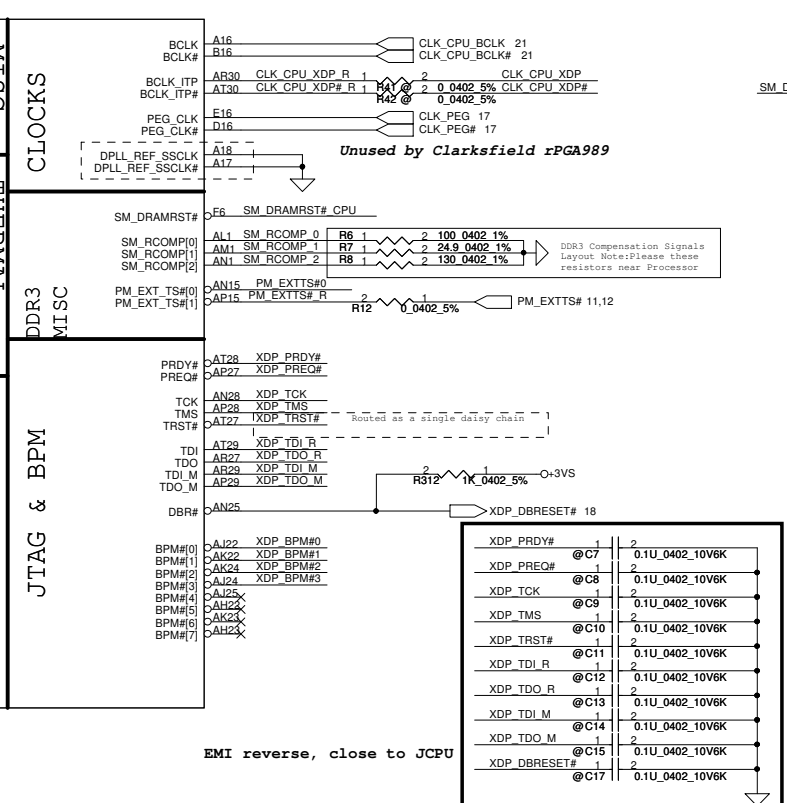
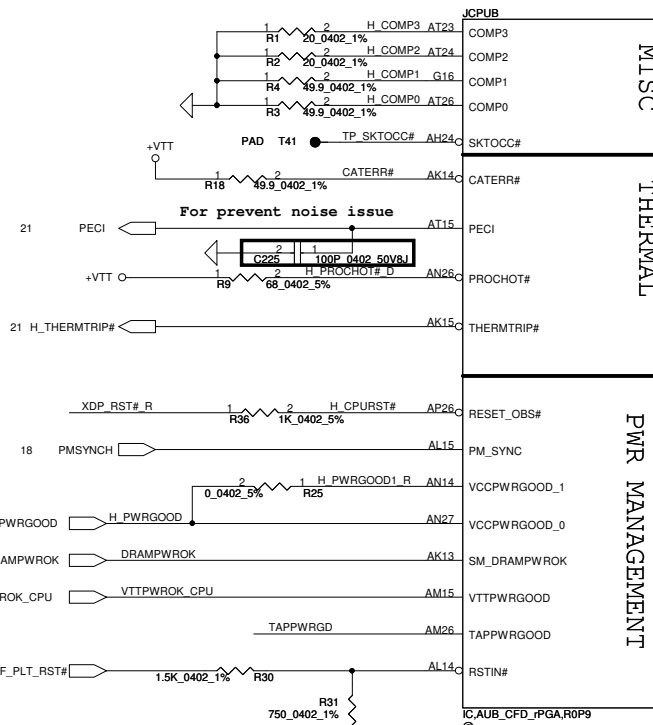
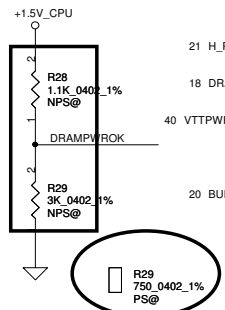
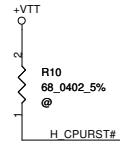
Power	Device	Address	Power	Device	Address
+3VALW	EC KB926 D3		+3VS	EC KB926 D3	
+3VALW	Smart Battery	0001 011x b	+3VS	VGA THM Sensor ADM1032ARMZ	1001 110x b
			+3VS	PCH	0100 110x b

### PCH SM Bus address

Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMM0	1001 000x b
+3VS	DDR DIMM1	1001 010x b
+3VS	Express	
+3VS	WLAN/Wimax/3G	

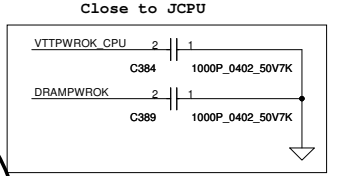
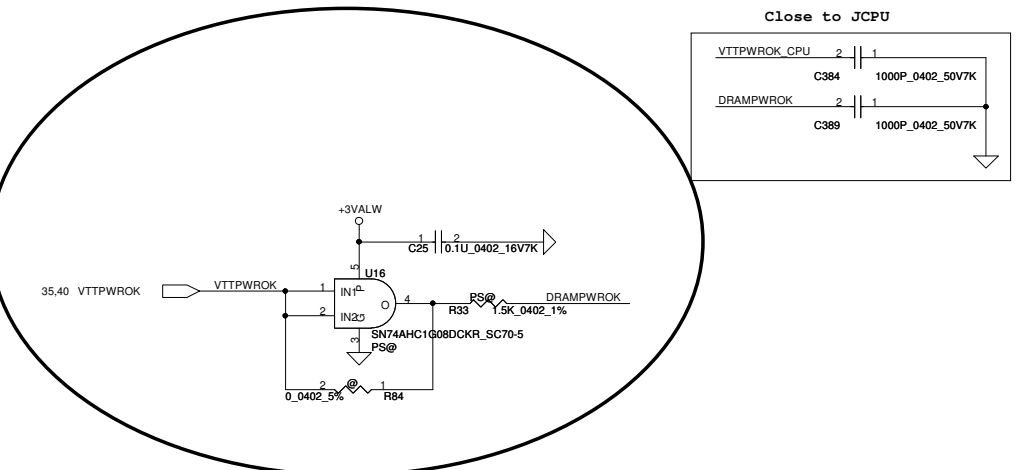
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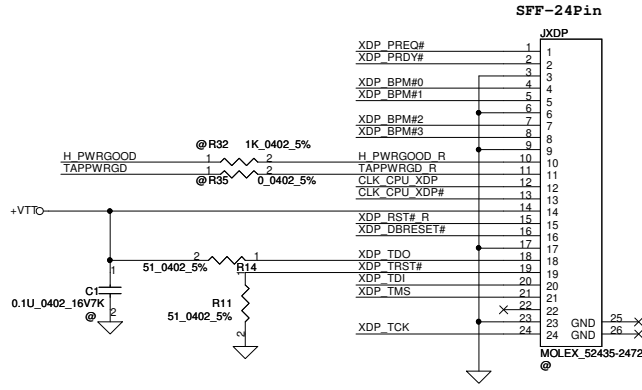


**JTAG MAPPING**

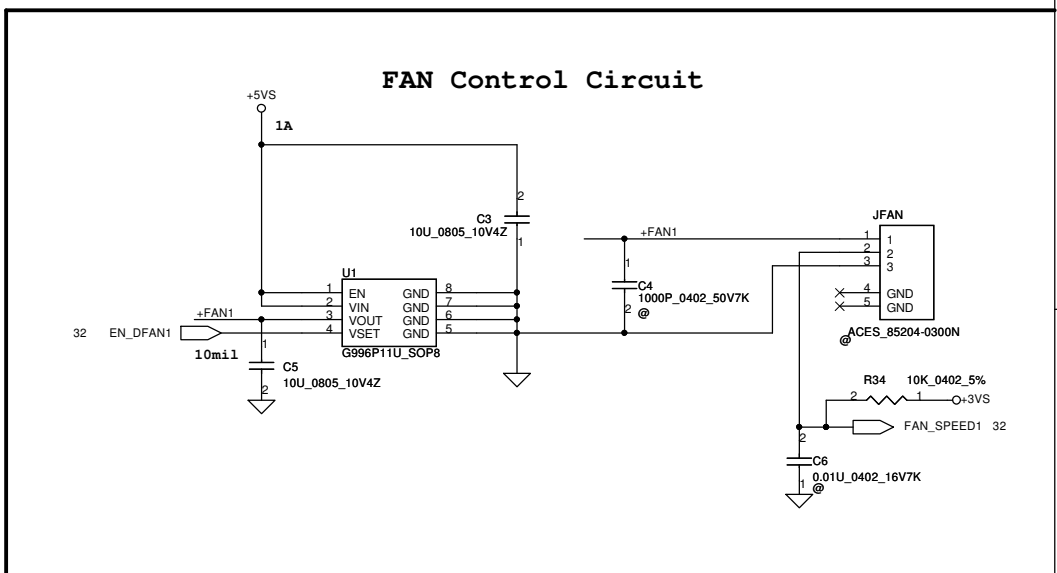
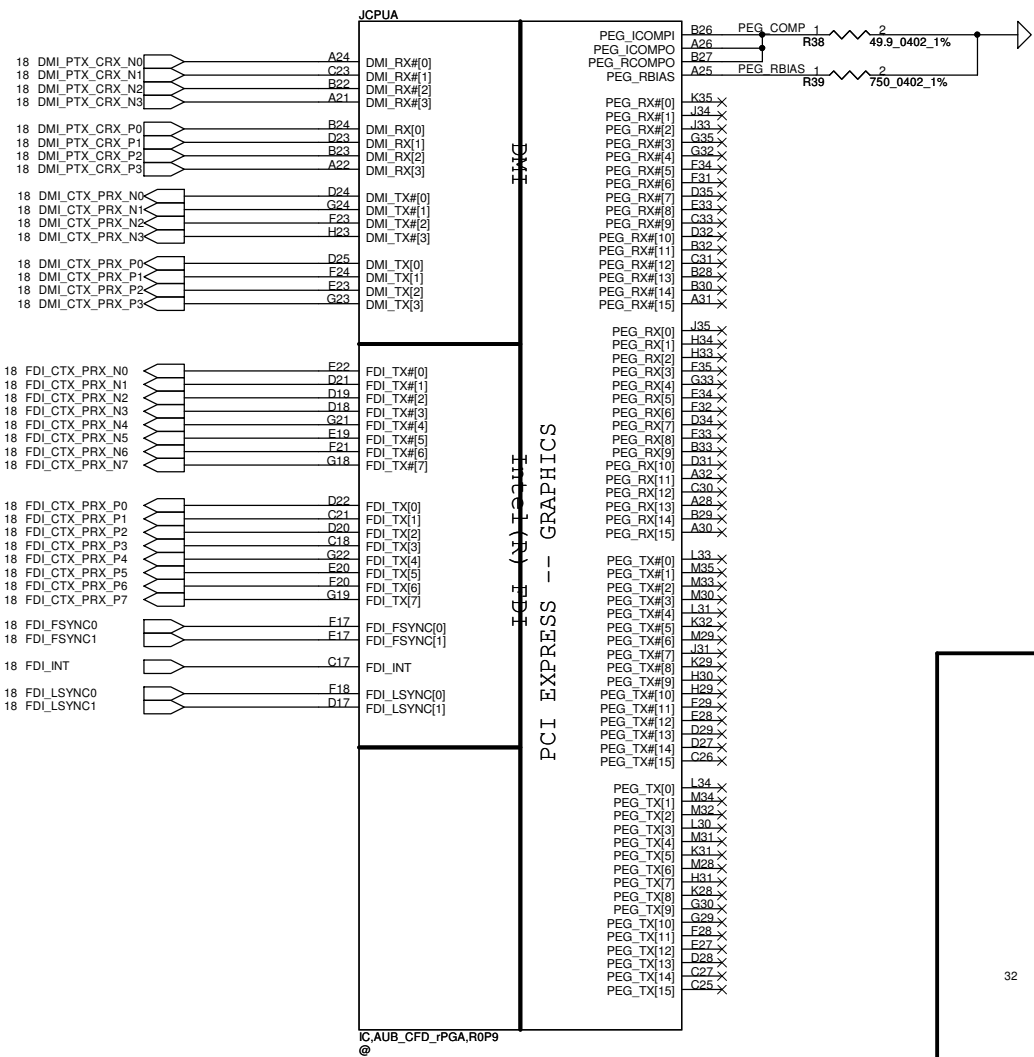
Scan Chain (Default)	STUFF -> R20, R23, R27 NO STUFF -> R21, R26
CPU Only	STUFF -> R20, R21 NO STUFF -> R23, R26, R27
GMCH Only	STUFF -> R26, R27 NO STUFF -> R20, R21, R23



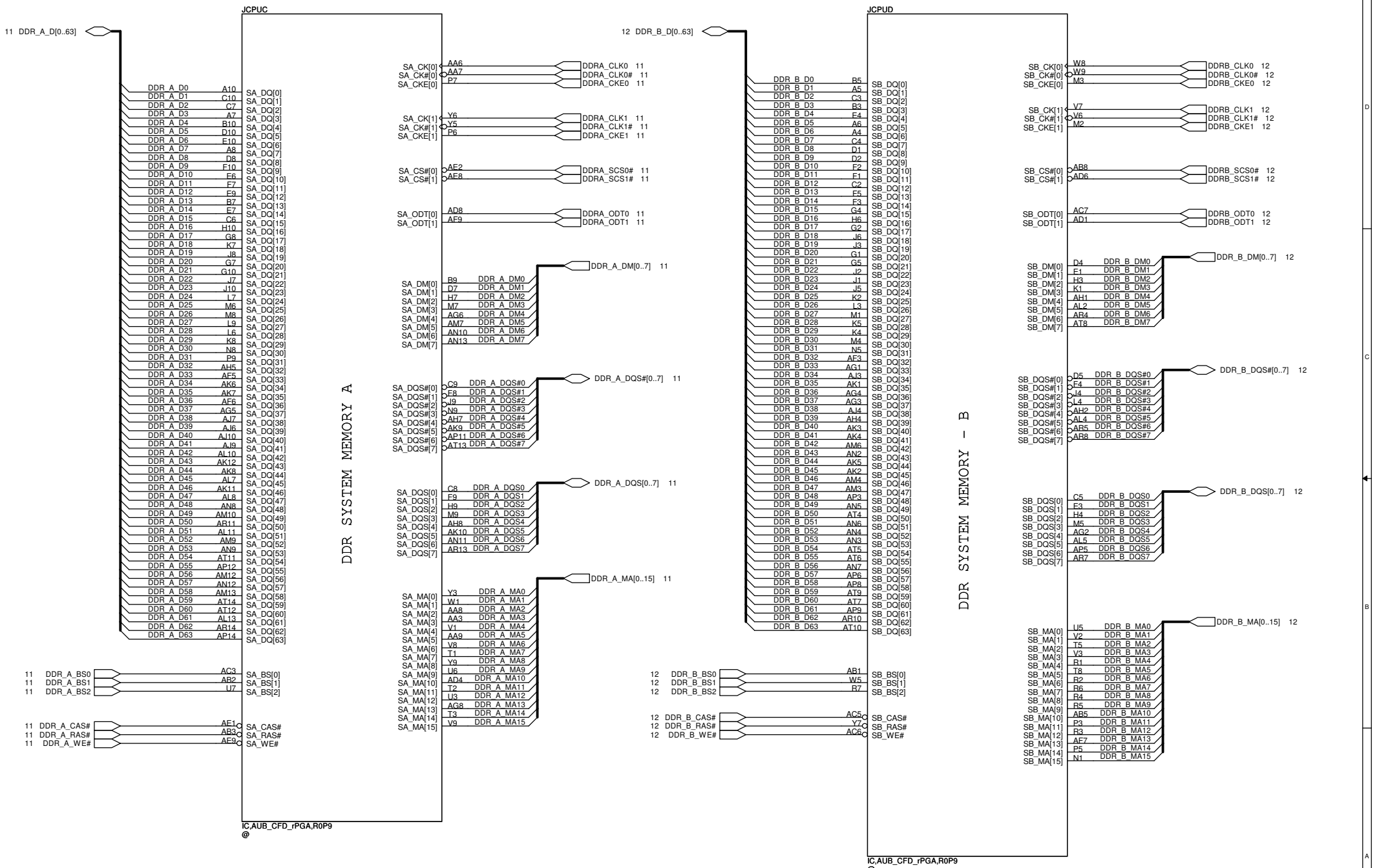
**XDP Connector**



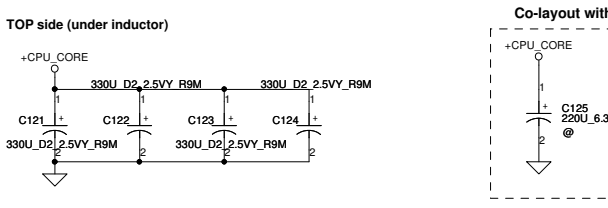
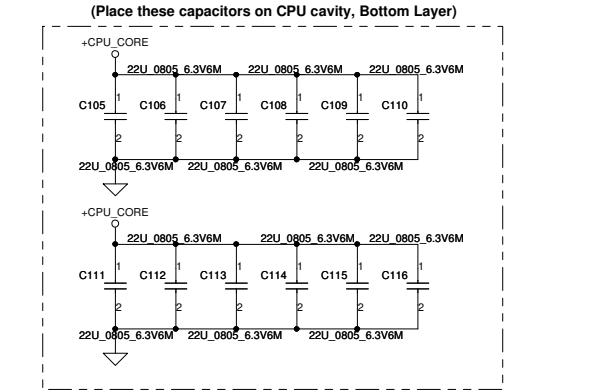
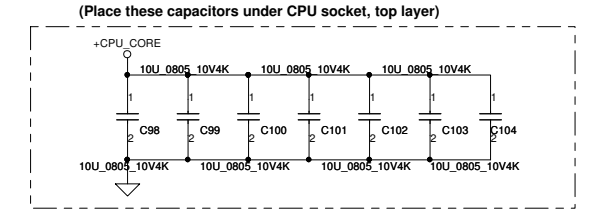
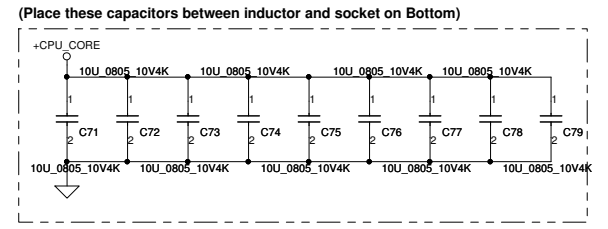
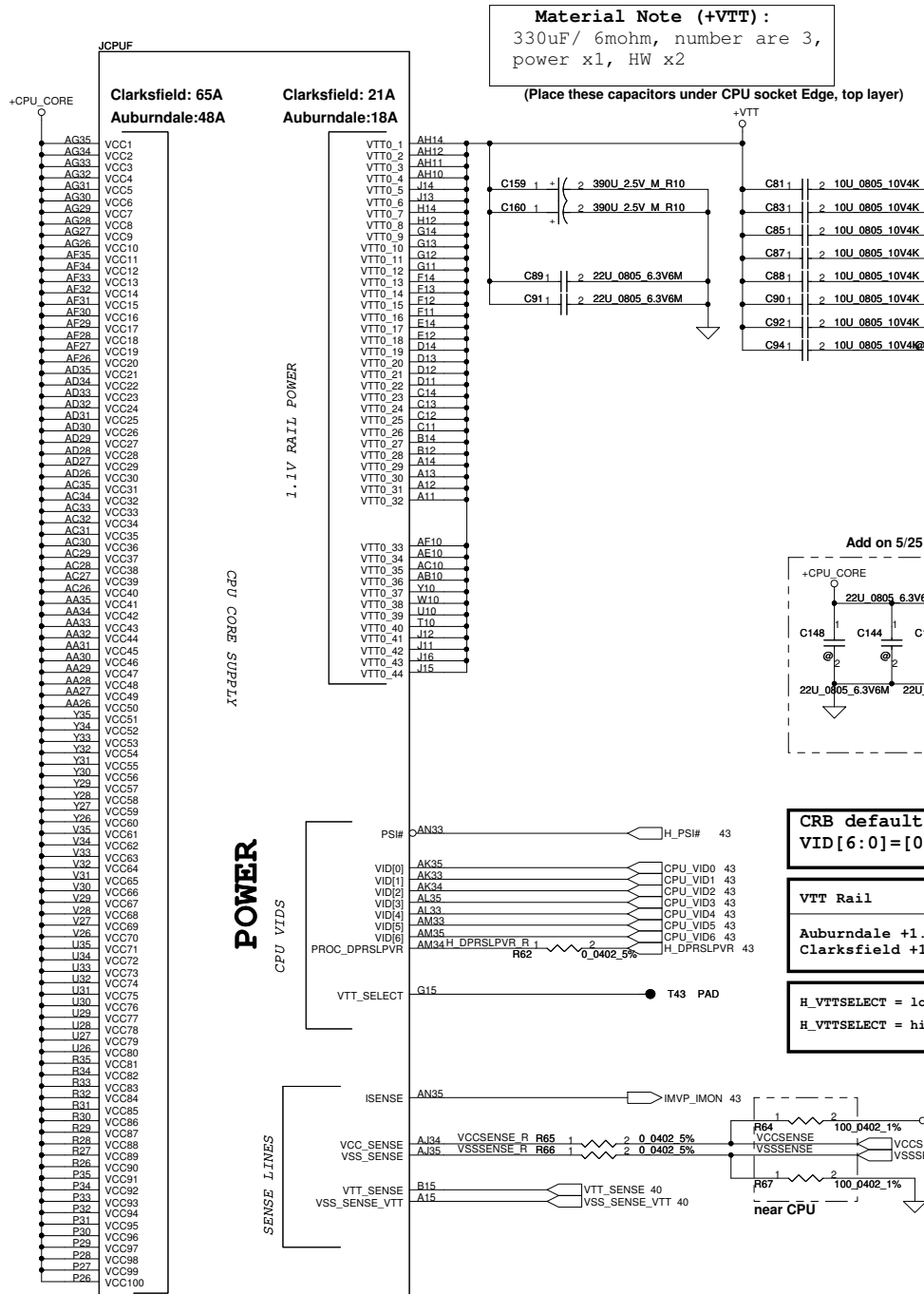
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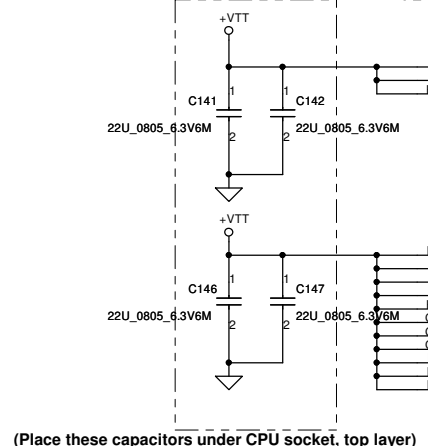
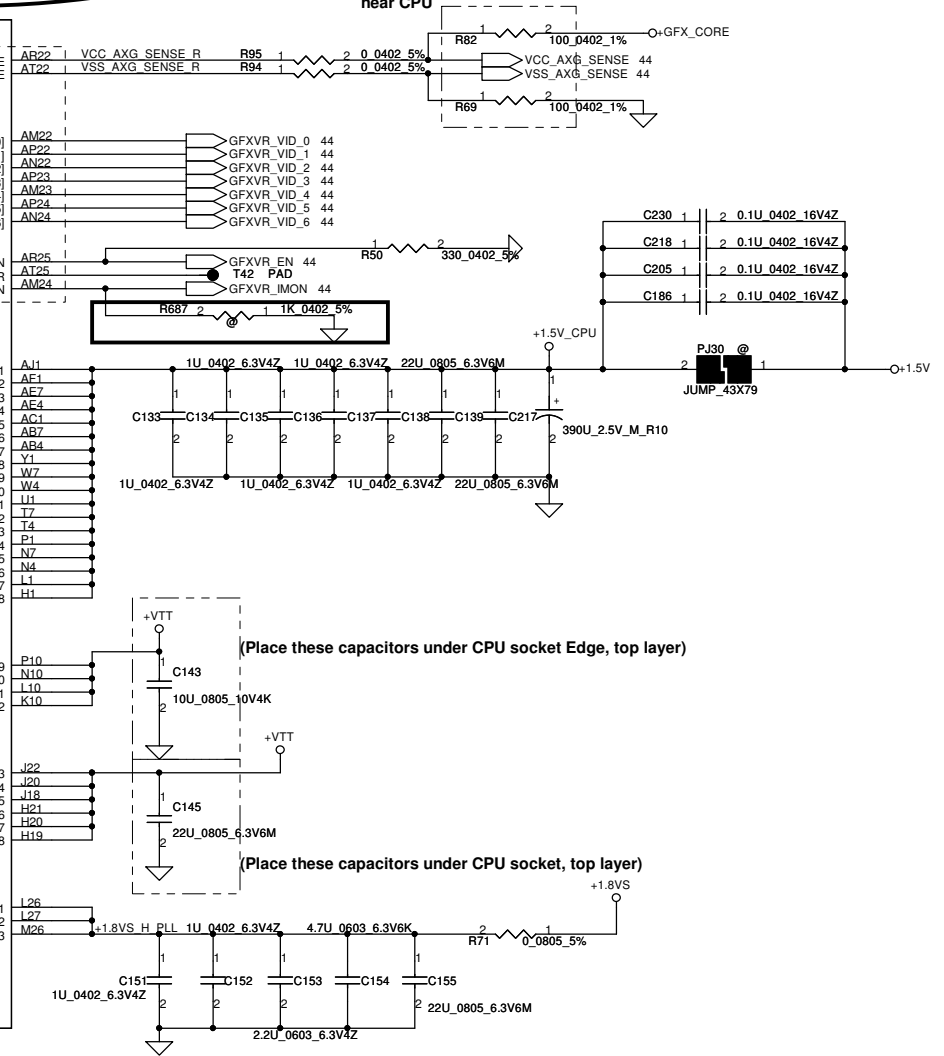
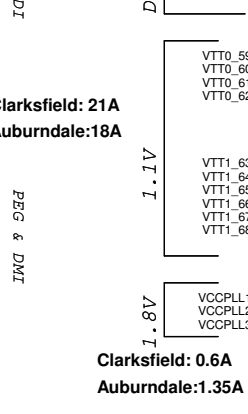
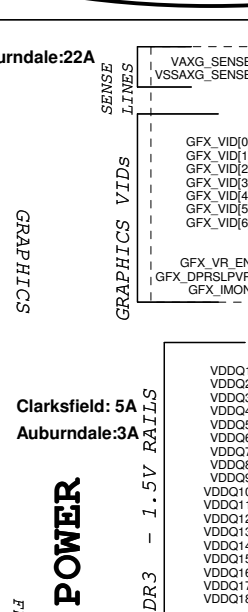
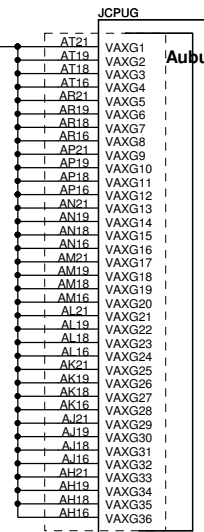
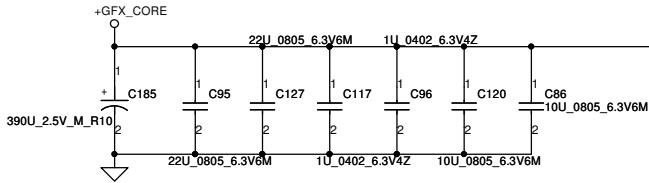
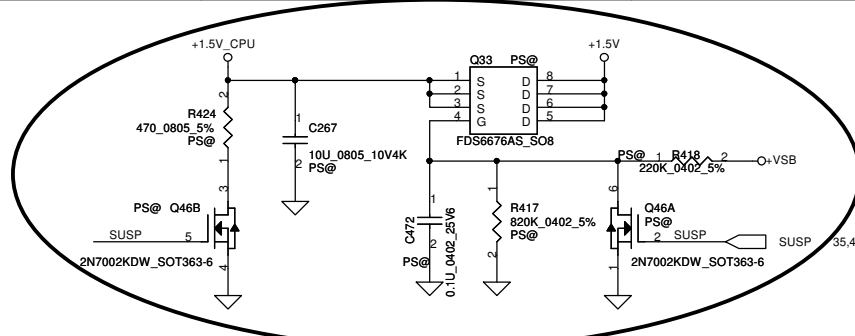
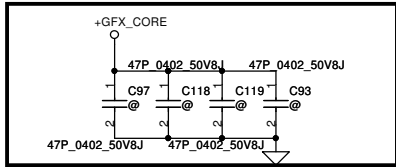


**Check list:**  
+CPU\_CORE: 6x 470uF, 12x 22uF, 16x 10uF  
+VTT: 4x 330uF, 7x 22uF, 8x 10uF

IC\_AUB\_CFD\_rPGA\_R0P9  
@

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				CPU POWER-1	
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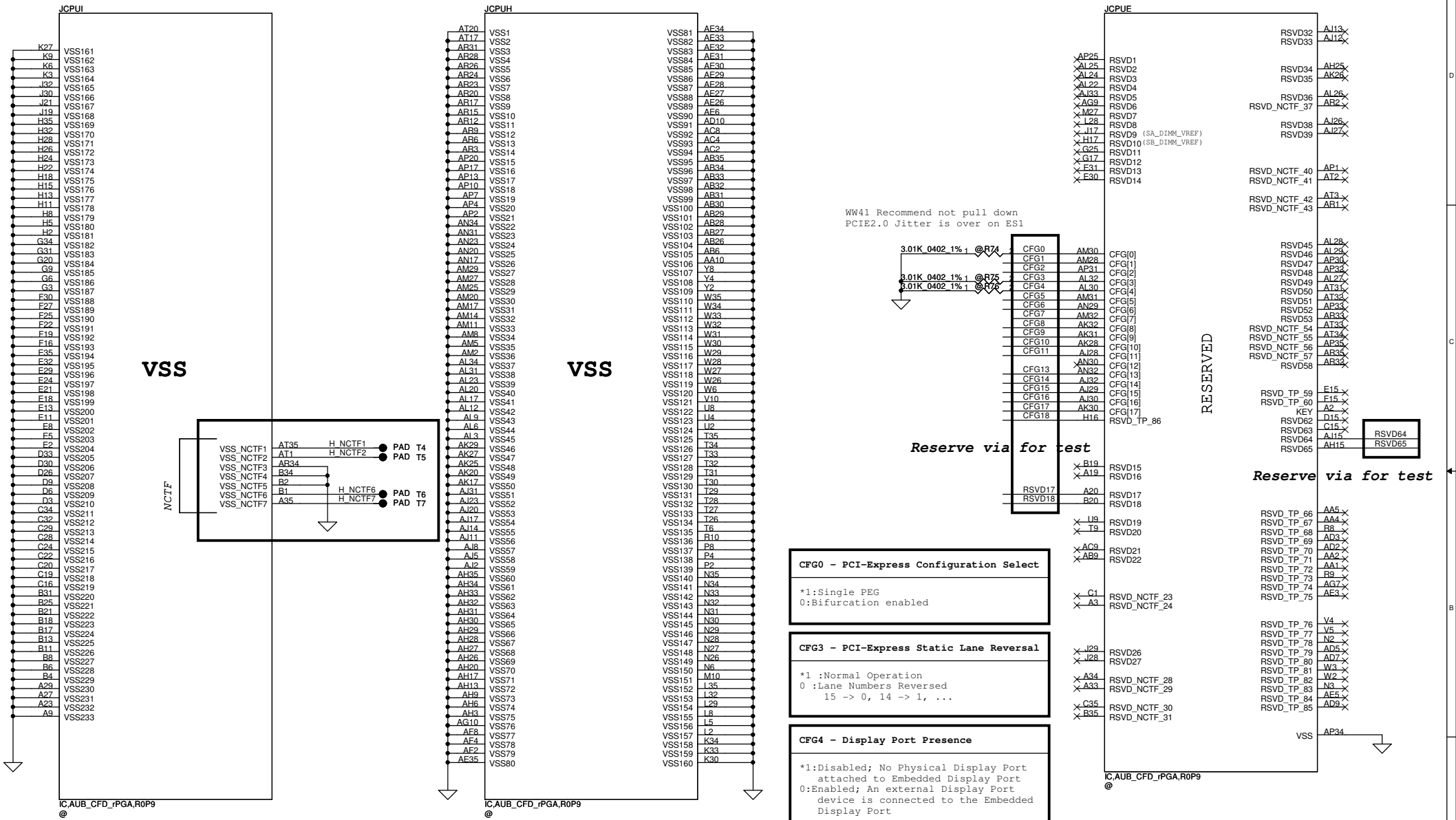


(Place these capacitors under CPU socket, top layer)

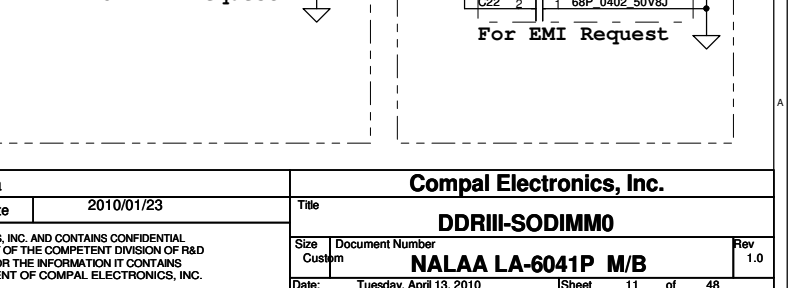
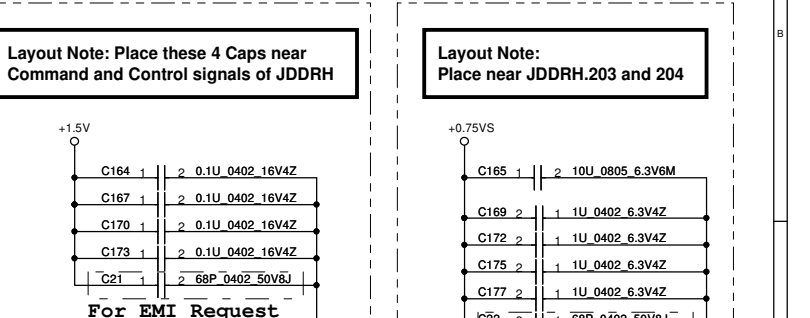
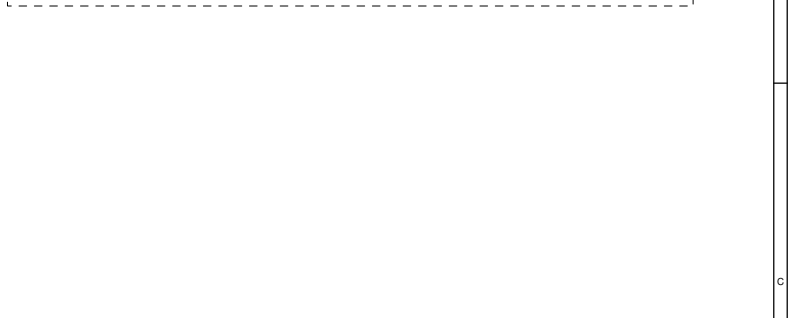
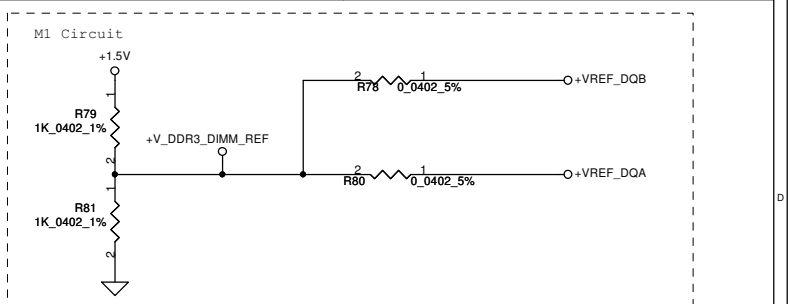
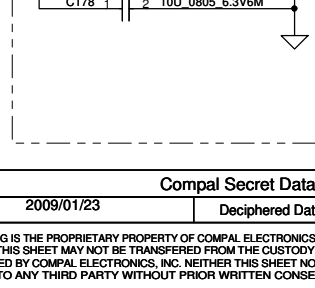
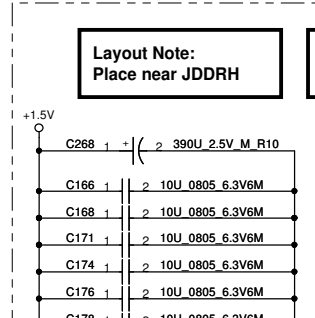
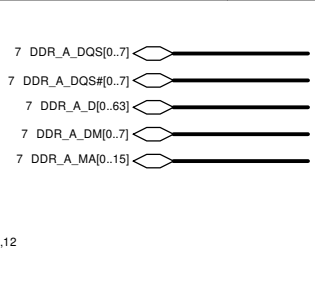
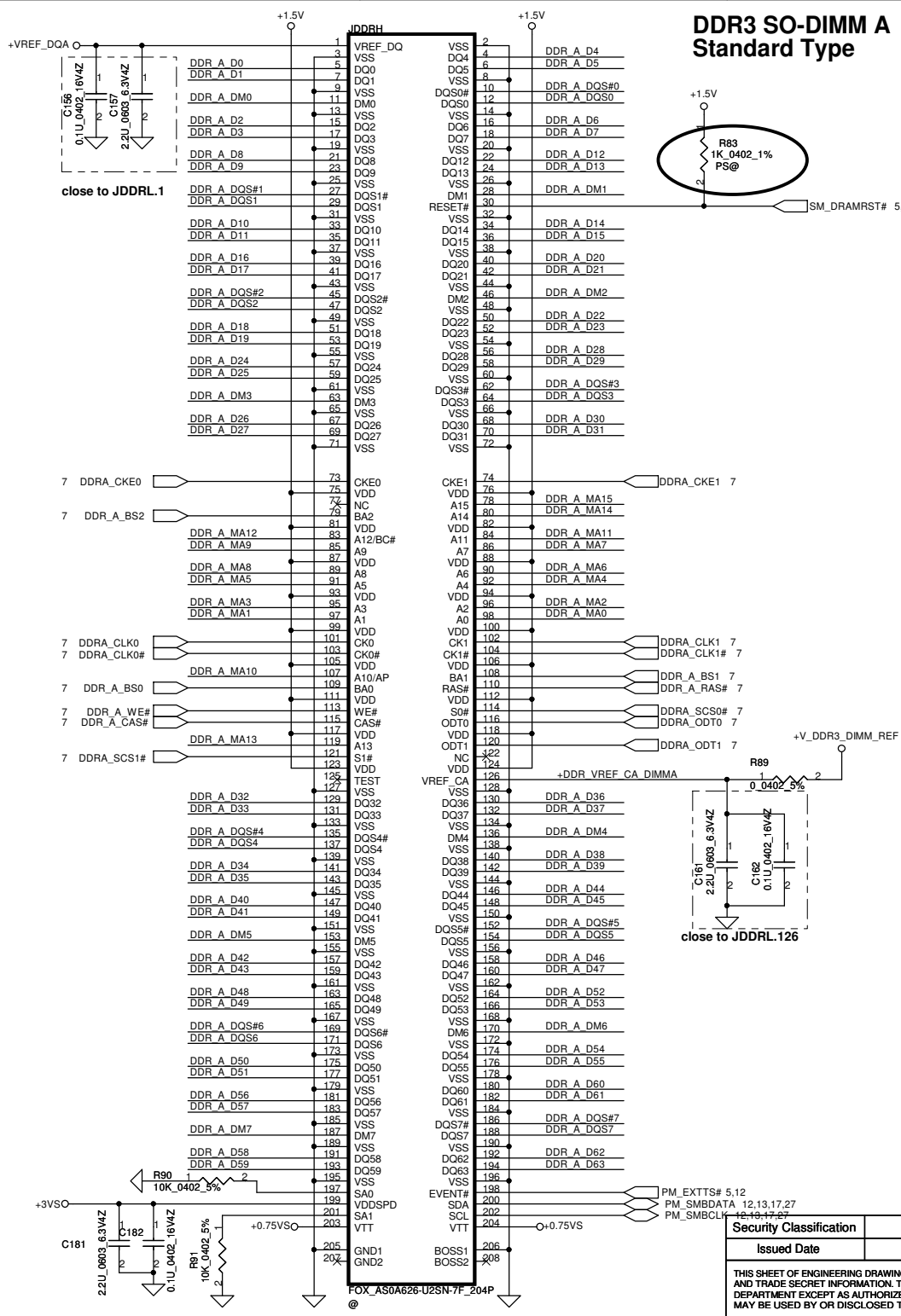
(Place these capacitors under CPU socket Edge, top layer)

(Place these capacitors under CPU socket, top layer)

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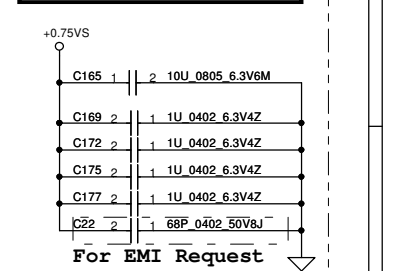
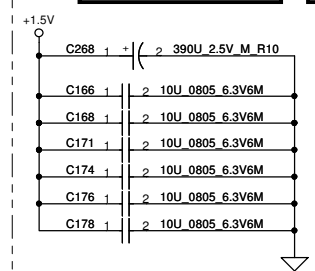
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				CPU GND/RESERVED	
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**Layout Note:**  
Place near JDDRH

**Layout Note:** Place these 4 Caps near Command and Control signals of JDDRH

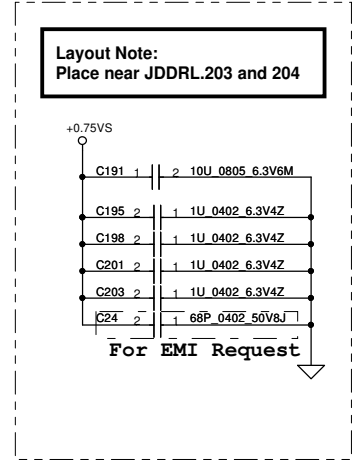
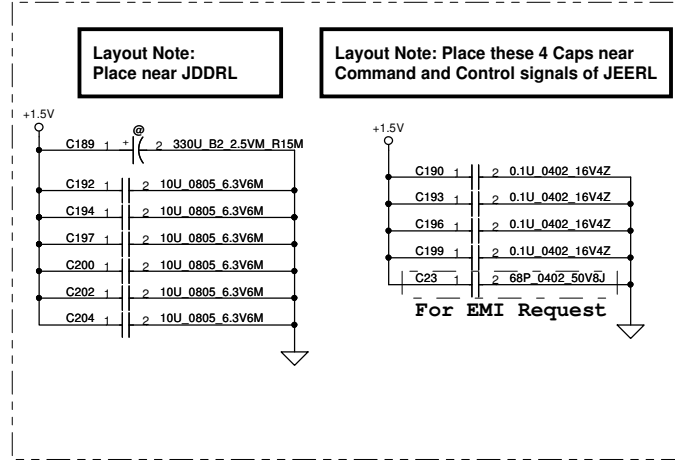
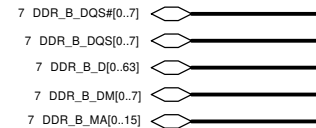
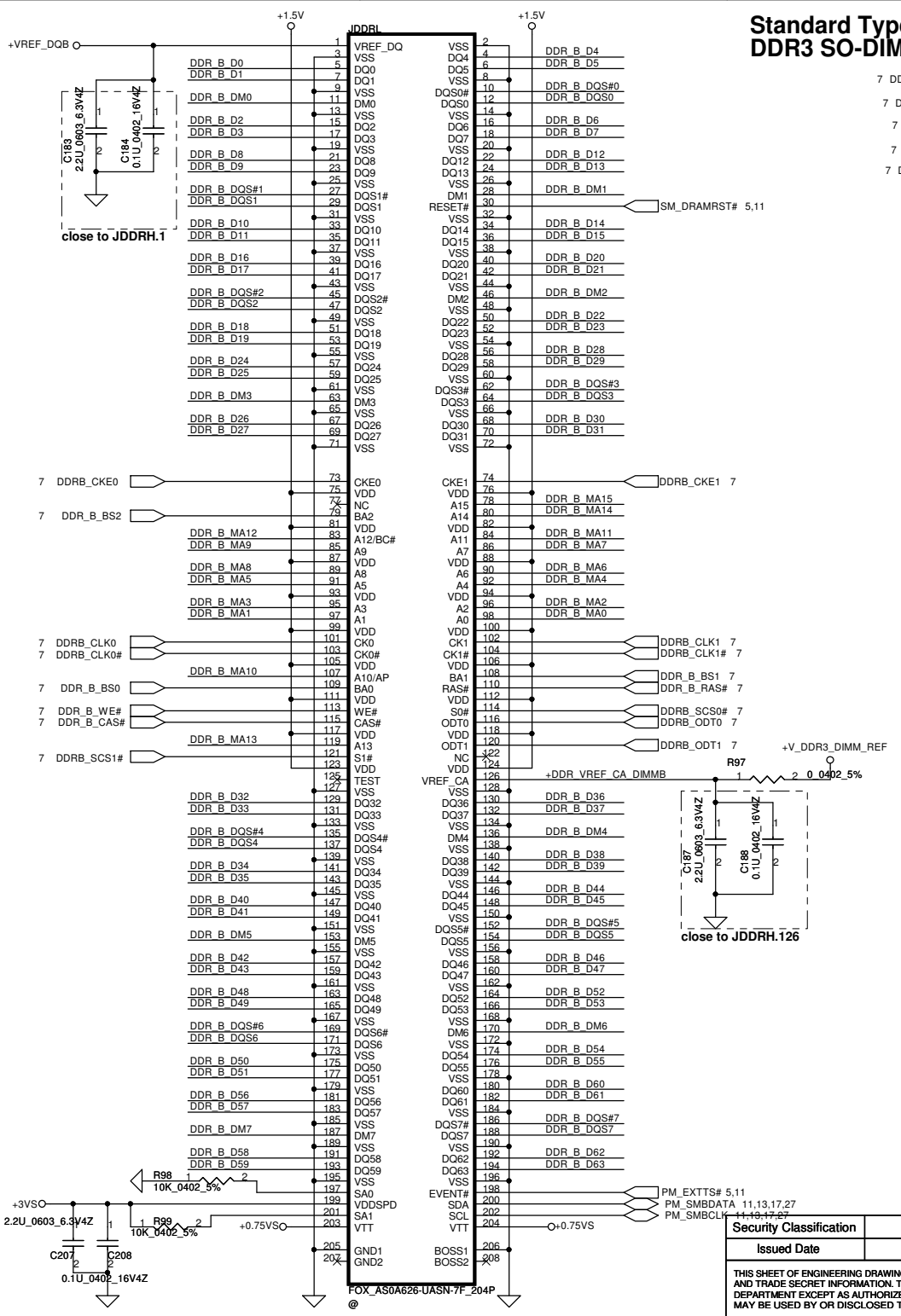
**Layout Note:** Place near JDDRH.203 and 204



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<b>DDRIII-SODIMMO</b>			
Size	Document Number	Rev	
Custom	<b>NALAA LA-6041P M/B</b>	1.0	
Date:	Tuesday, April 13, 2010	Sheet	11 of 48

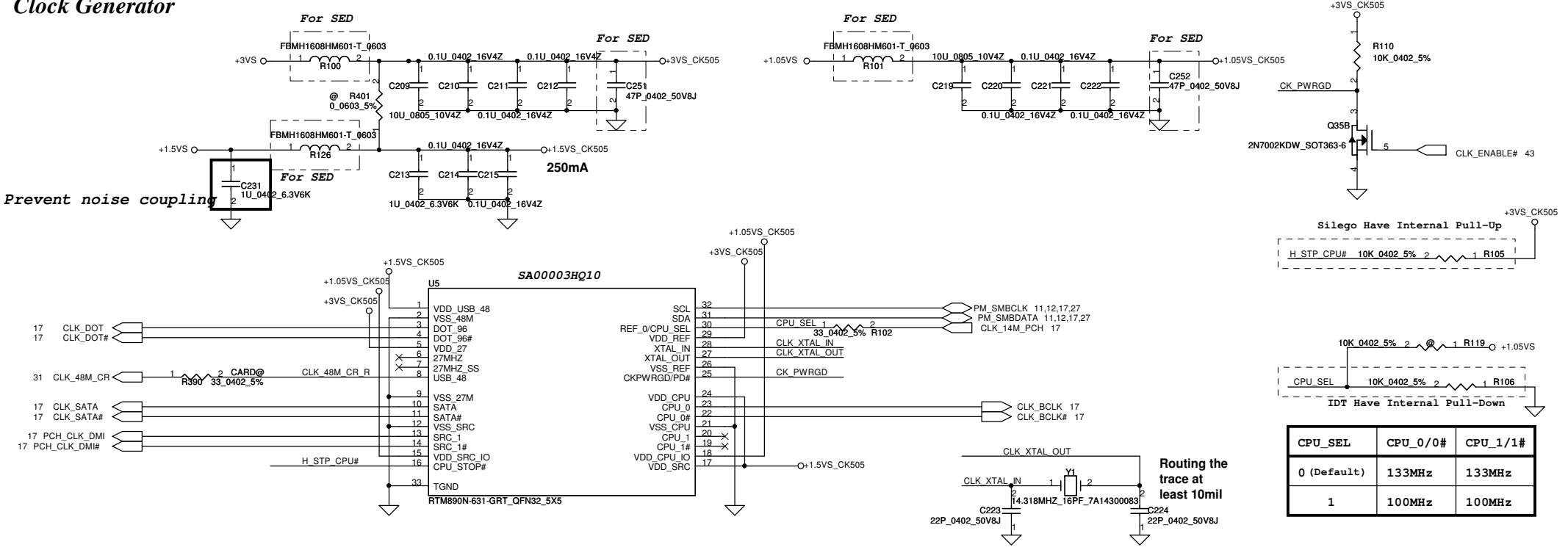
# Standard Type DDR3 SO-DIMM B



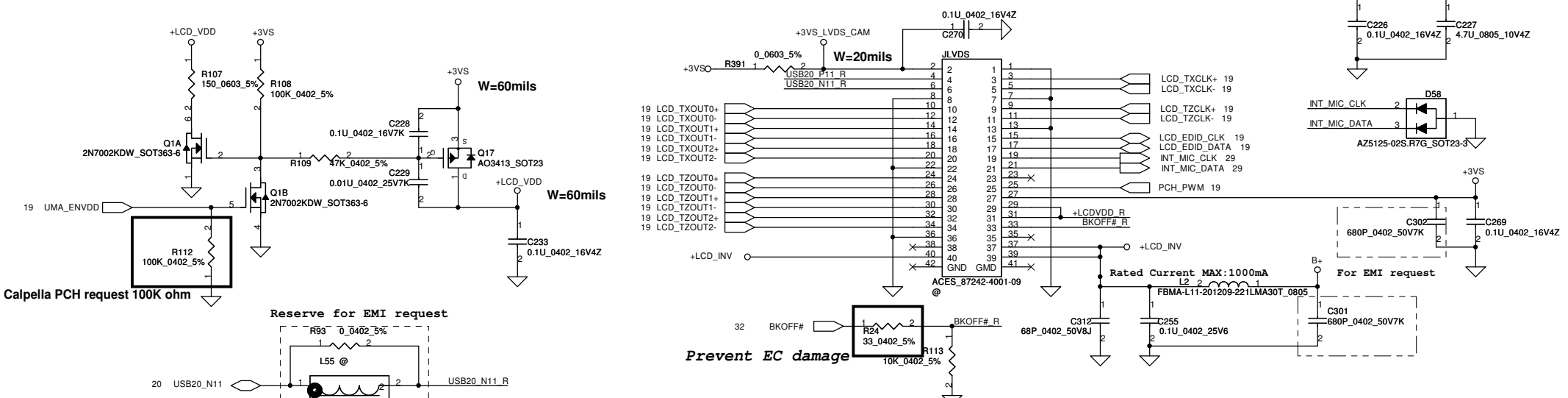
Security Classification		Compal Secret Data	
Issued Date	2009/01/23	Deciphered Date	2010/01/23
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Title <b>DDRIII-SODIMM1</b>		
Size Custom	Document Number <b>NALAA LA-6041P M/B</b>	Rev 1.0
Date:	Tuesday, April 13, 2010	Sheet 12 of 48

# Clock Generator

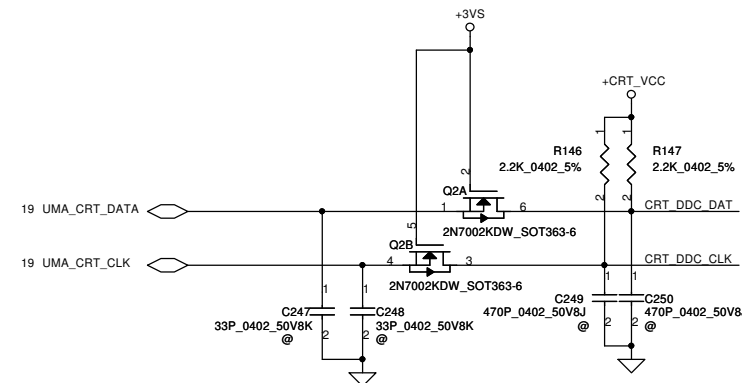
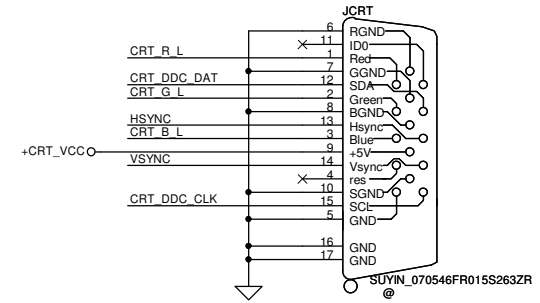
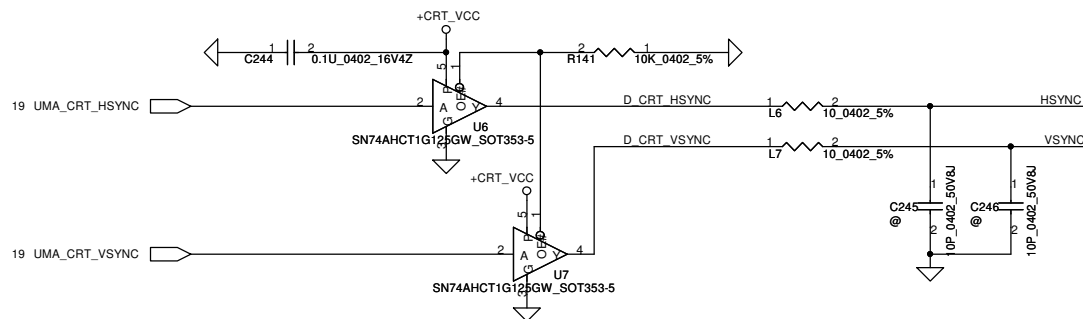
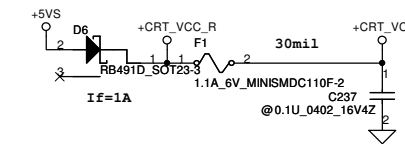
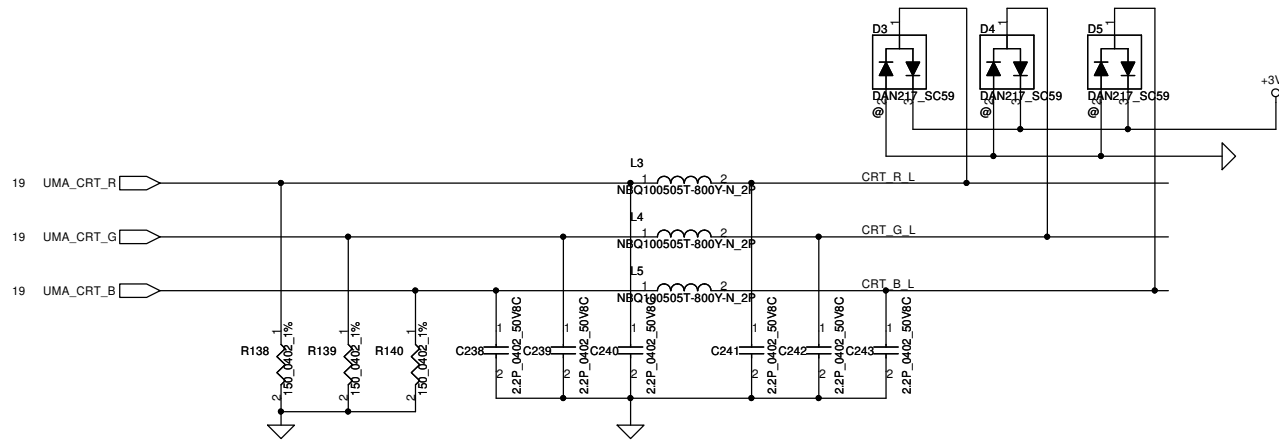


## LCD/PANEL BD. Conn.



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Size	Document Number	Date		Rev	
Custom	NALAA LA-6041P M/B	Tuesday, April 13, 2010		1.0	
				Sheet	13 of 48

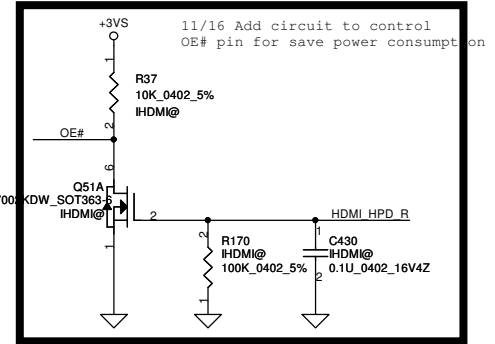
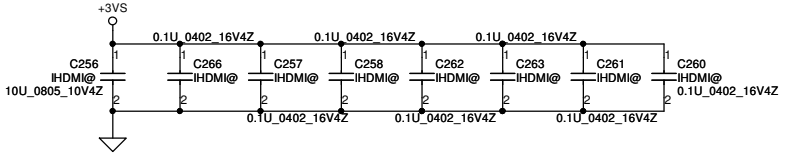
# CRT CONNECTOR



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Size	Document Number	Rev		1.0	
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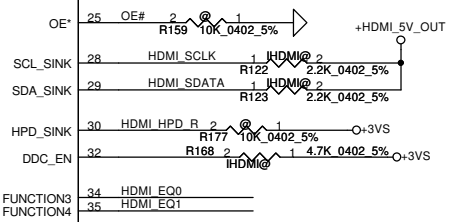
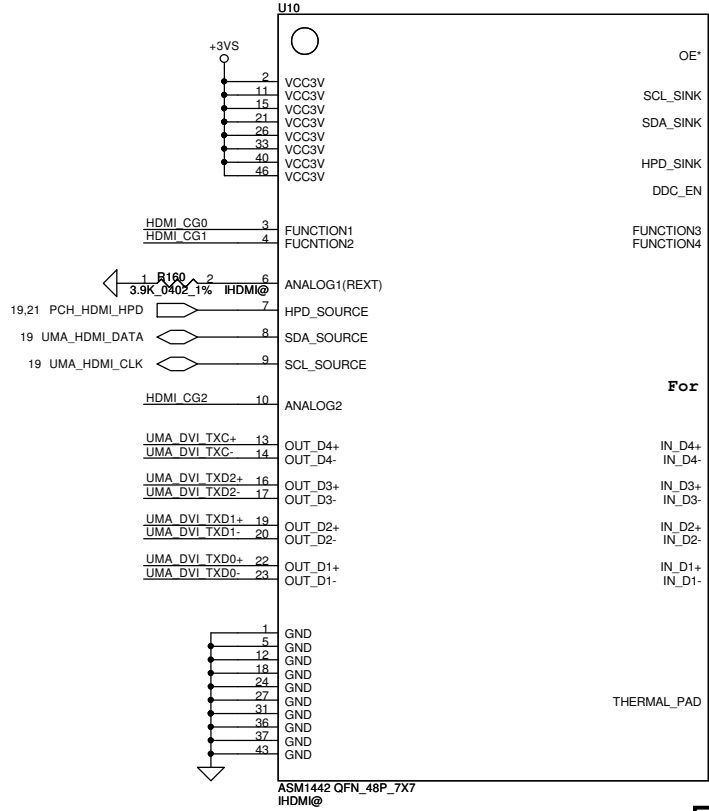
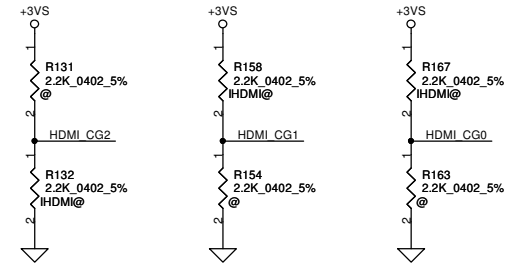
CG2	CG1	CG0	Swing	Pre-amp	Slew-rate	
0	0	0	450	0	0	
0	0	1	420	0	-3dB	Shortest trace
0	1	0	450	0	-3dB	Shortest trace
0	1	1	460	0	-4dB	
1	0	0	340	0	0	
1	0	1	400	2dB	0	Longest trace
1	1	0	400	2dB	0	Longest trace
1	1	1	420	0	0	

\* 0

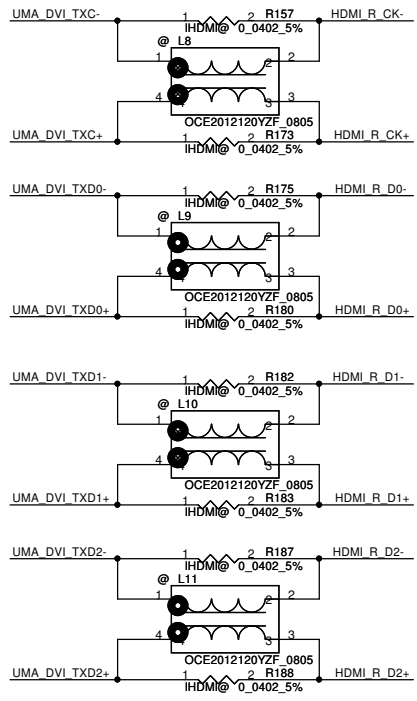
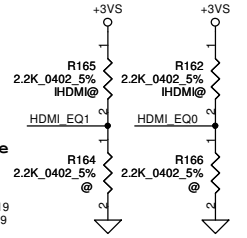
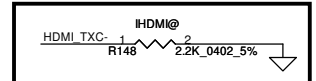


EQ1	EQ0	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB

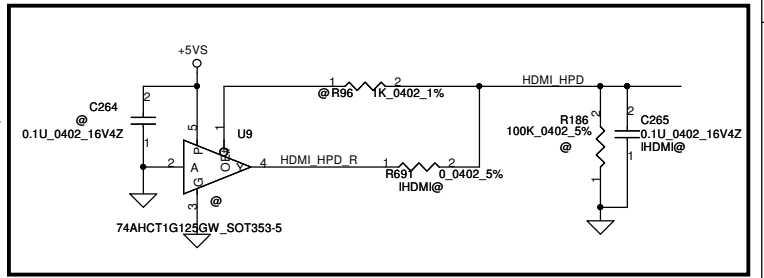
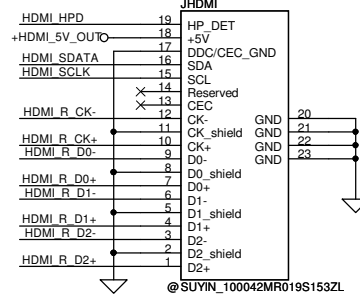
\* 1



For UMA HDMI level shift display compatibility issue

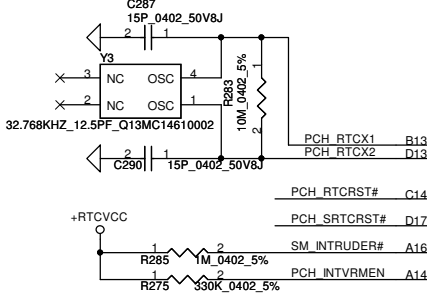
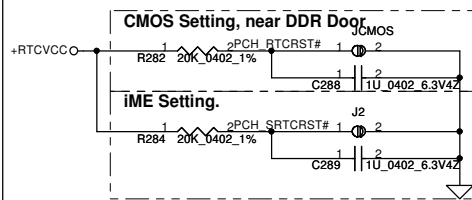


### HDMI Connector



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				HDMI Connector	
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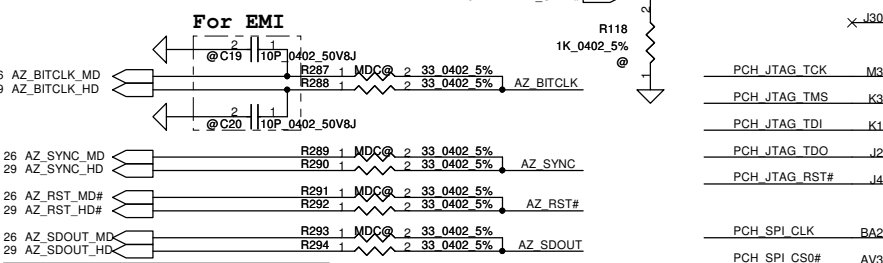


<b>Integrated SUS 1.05V VRM Enable</b>	
PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)

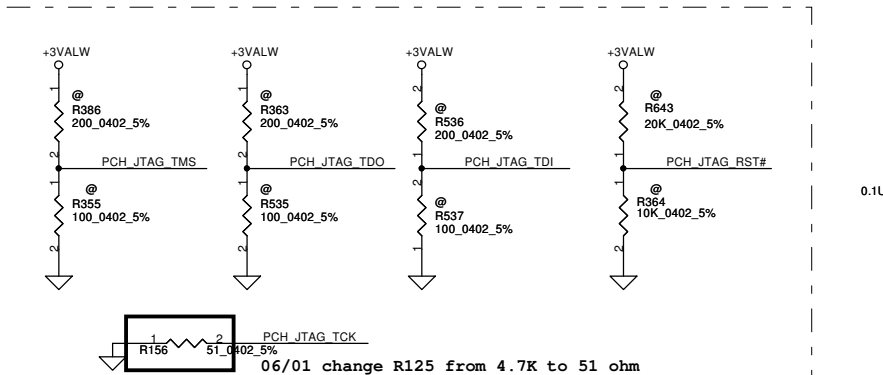
**HDA\_SYNC**  
 This signal has a weak internal pull down.  
 H=>On Die PLL is supplied by 1.5V  
 \*L=>On Die PLL is supplied by 1.8V

**HDA\_SDO**  
 This signal has a weak internal pull down.  
 This signal can't PU

<b>Flash Descriptor Security Override</b>	
HDA_DOCK_EN#	Low = Enabled High = Disabled *

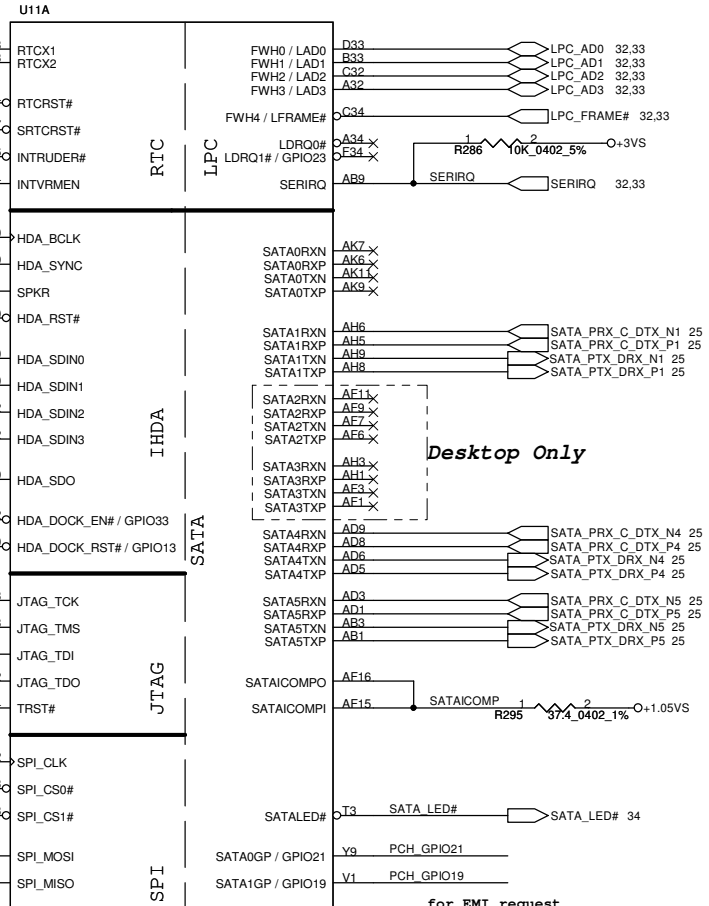


<b>ITPM Enabled Internal: Pull down 20k</b>	
SPI_MOSI	High = Enabled Low = Disabled (Default)



06/01 change R125 from 4.7K to 51 ohm

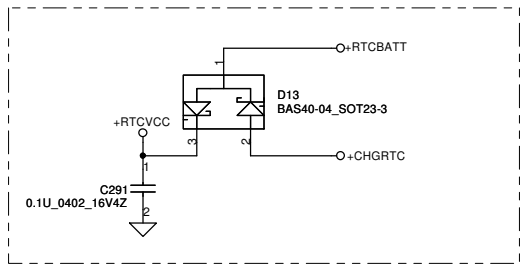
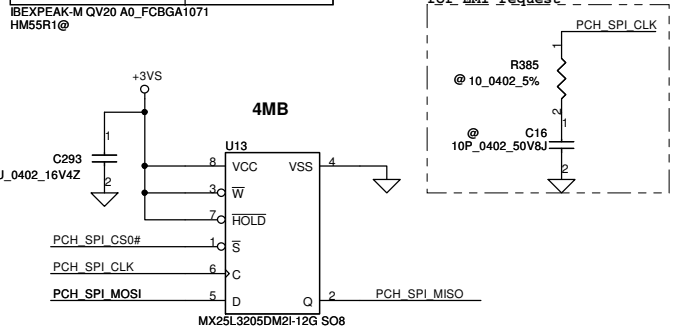
PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
PCH_JTAG_TMS	R355	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDI	R536	200ohm	200ohm	20kohm	No Install
PCH_JTAG_TDI	R537	100ohm	100ohm	10kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20kohm	20kohm	No Install	No Install
PCH_JTAG_RST#	R353	10kohm	10kohm	No Install	No Install



1ST HDD

SATA ODD

eSATA



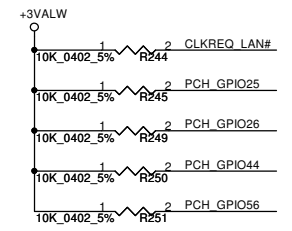
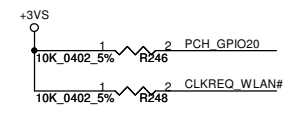
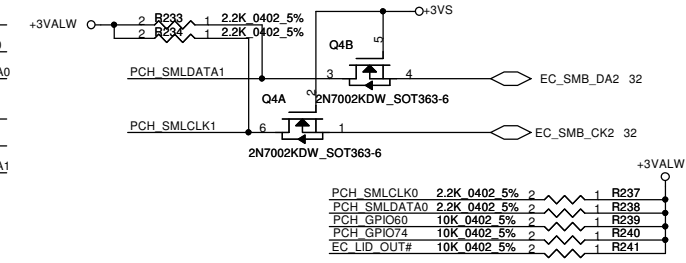
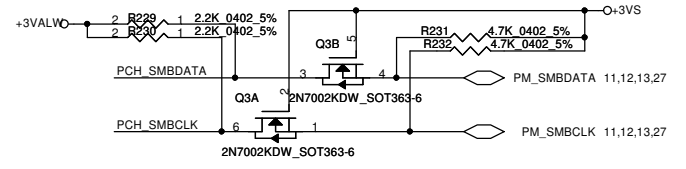
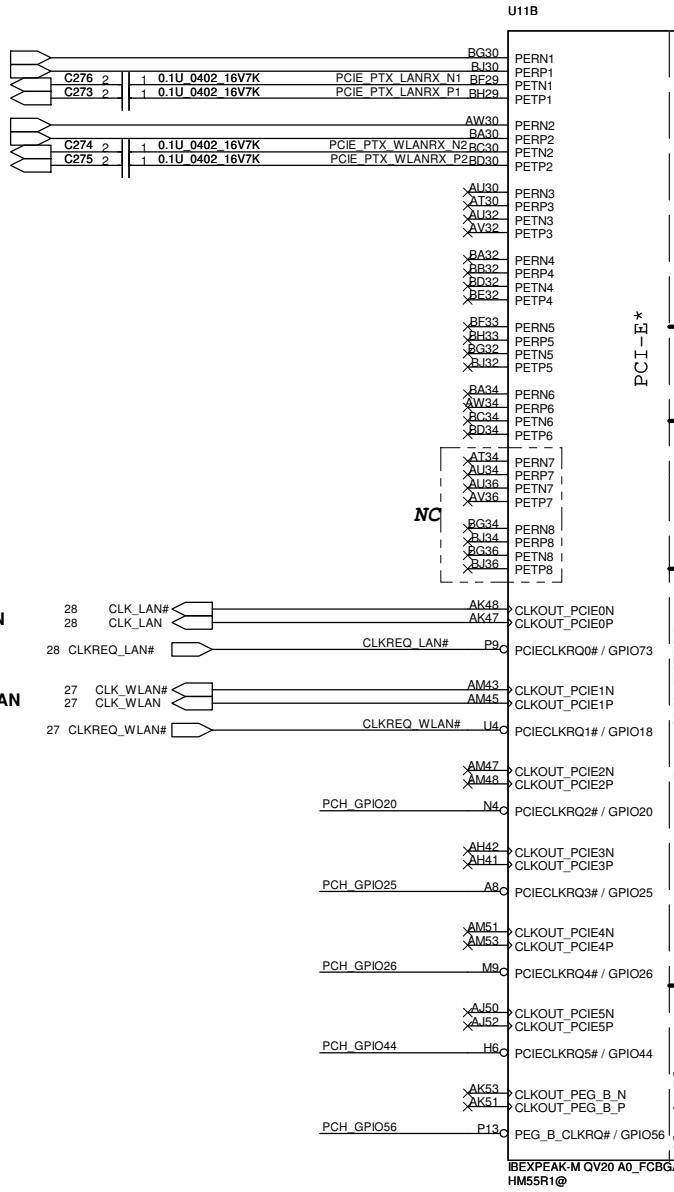
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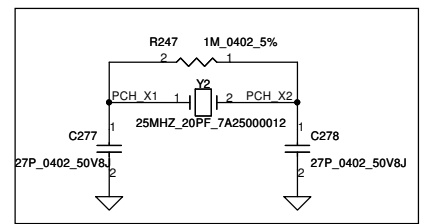


**For LAN**  
 28 PCIE\_PRX\_C\_LANTX\_N1  
 28 PCIE\_PRX\_C\_LANTX\_P1  
 28 PCIE\_PT\_X\_C\_LANRX\_N1  
 28 PCIE\_PT\_X\_C\_LANRX\_P1

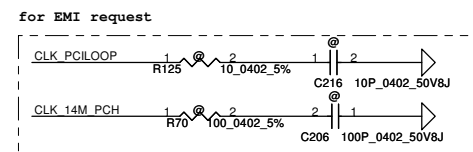
**For WLAN**  
 27 PCIE\_PRX\_WLANTX\_N2  
 27 PCIE\_PRX\_WLANTX\_P2  
 27 PCIE\_PT\_X\_C\_WLANRX\_N2  
 27 PCIE\_PT\_X\_C\_WLANRX\_P2



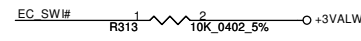
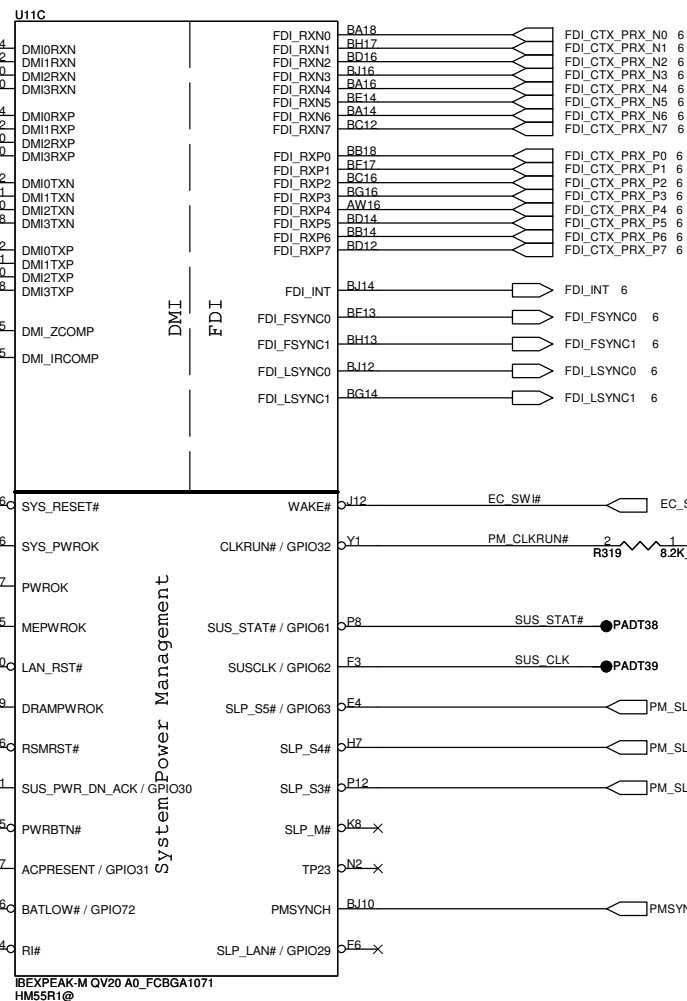
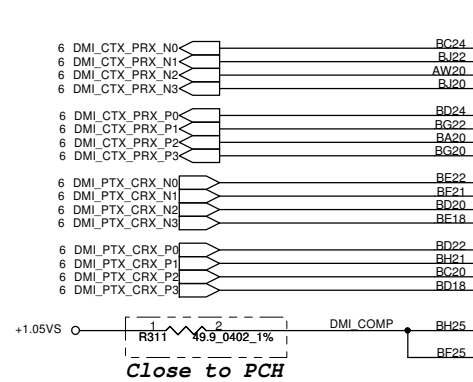
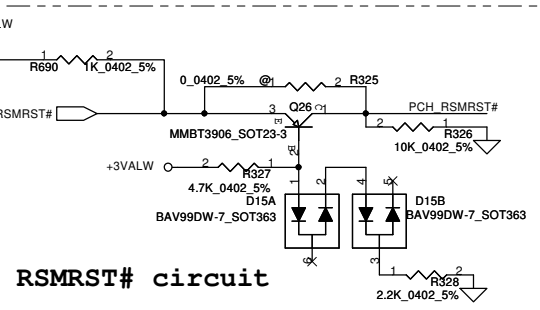
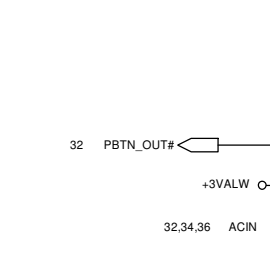
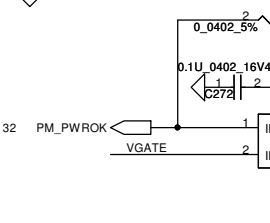
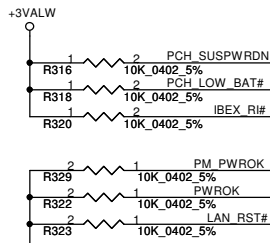
**FROM CLK GEN FOR: 133/100/96/14.318 MHZ**



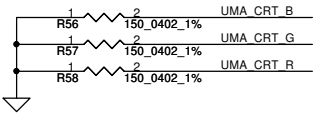
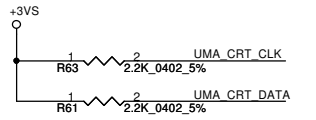
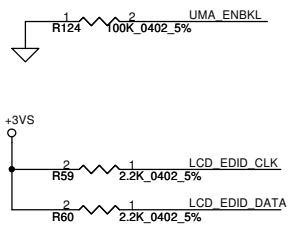
Note: Stuff 0 ohm if 25MHz crystal un-stuff



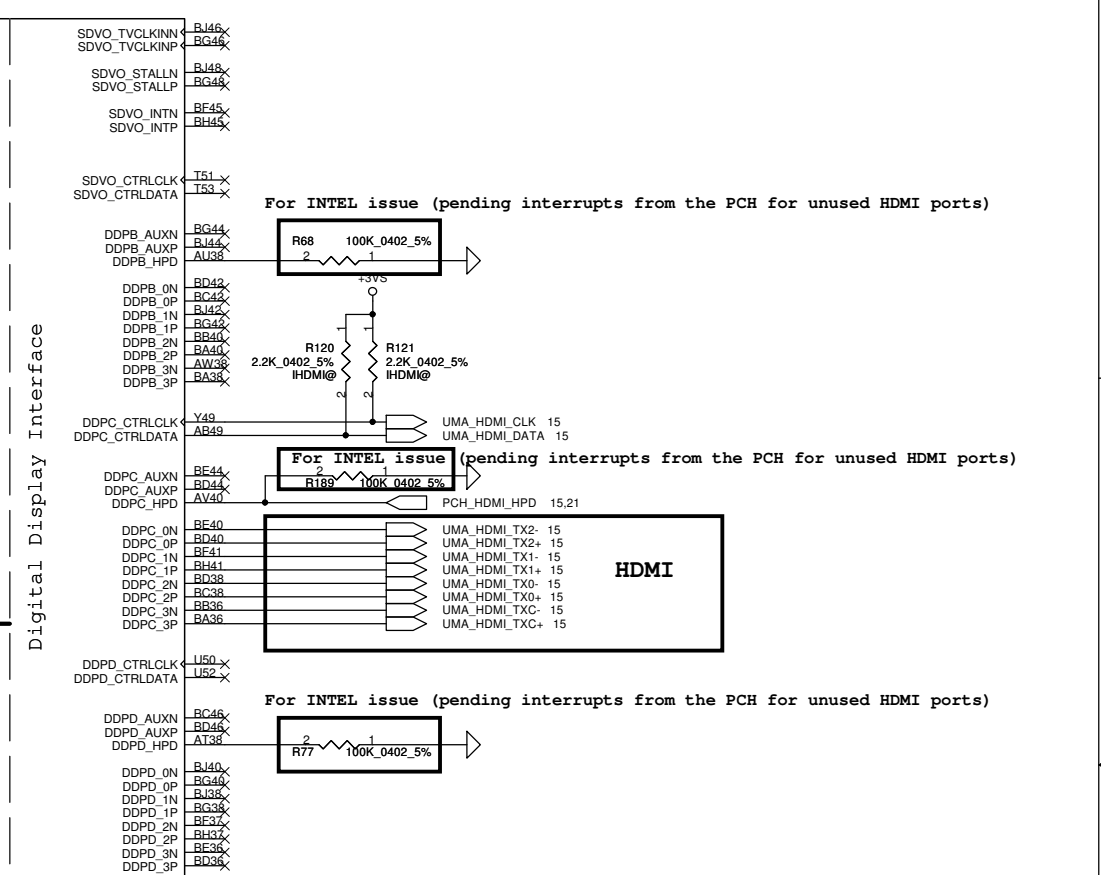
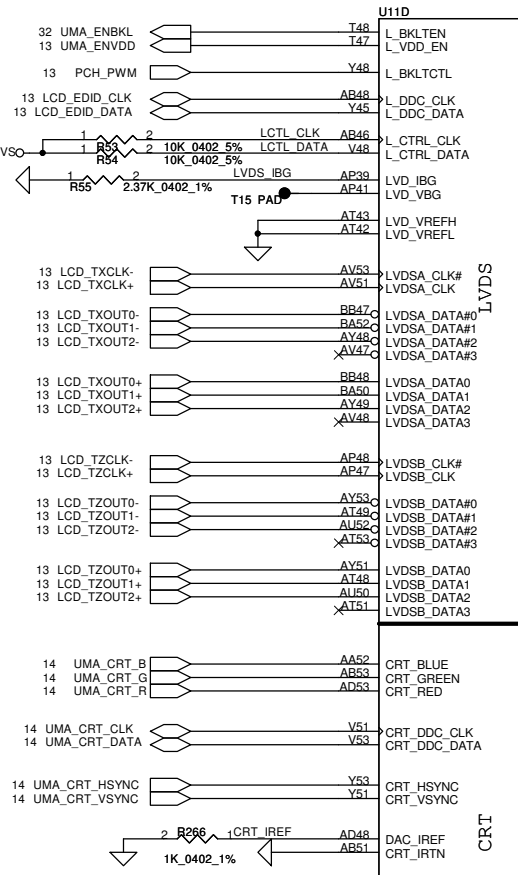
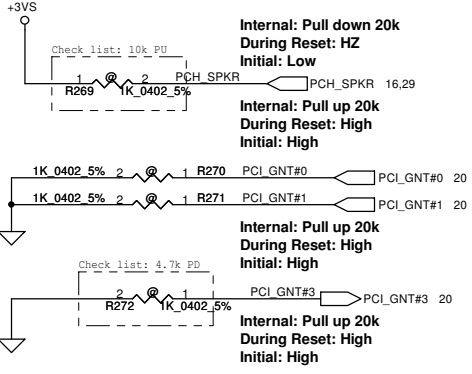
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				PCH-DMI/FDI/PWM	
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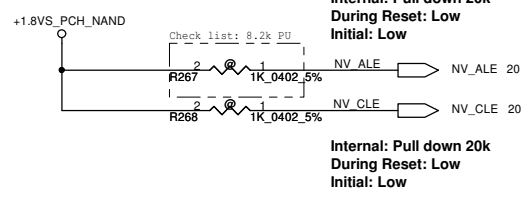
### PCH Strap Pin



NO REBOOT Strap		
PCH_SPKR	Low= Disable	High= Enable

Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Loaction
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable

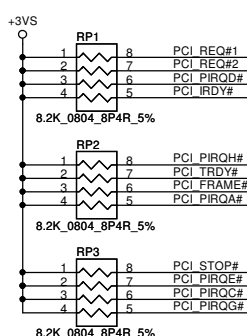
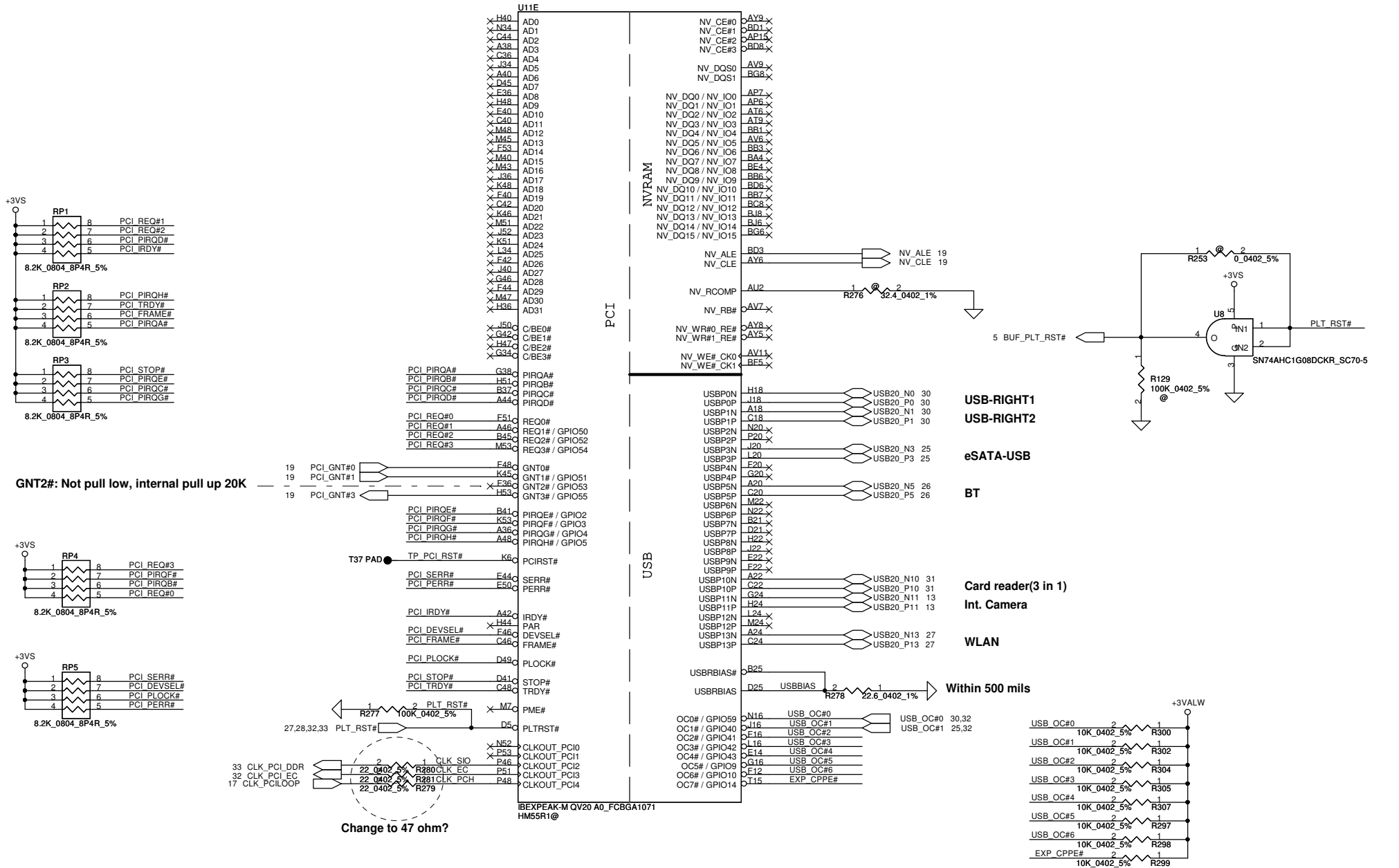


Internal: Pull down 20k  
During Reset: Low  
Initial: Low

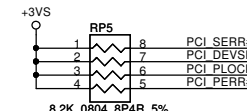
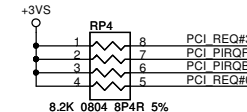
Internal: Pull down 20k  
During Reset: Low  
Initial: Low

Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)

DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc



GNT2#: Not pull low, internal pull up 20K



Change to 47 ohm?

- USB-RIGHT1
- USB-RIGHT2
- eSATA-USB
- BT
- Card reader(3 in 1)
- Int. Camera
- WLAN

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**GPIO8**  
**Not pull down**  
**Internal: Pull up 20k**  
**During Reset: High**  
**Initial: High**

**GPIO15**  
**a Strong pull up may be needed**  
**for GPIO Functionality**  
**Internal: Pull down 20k**  
**During Reset: Low**  
**Initial: Low**

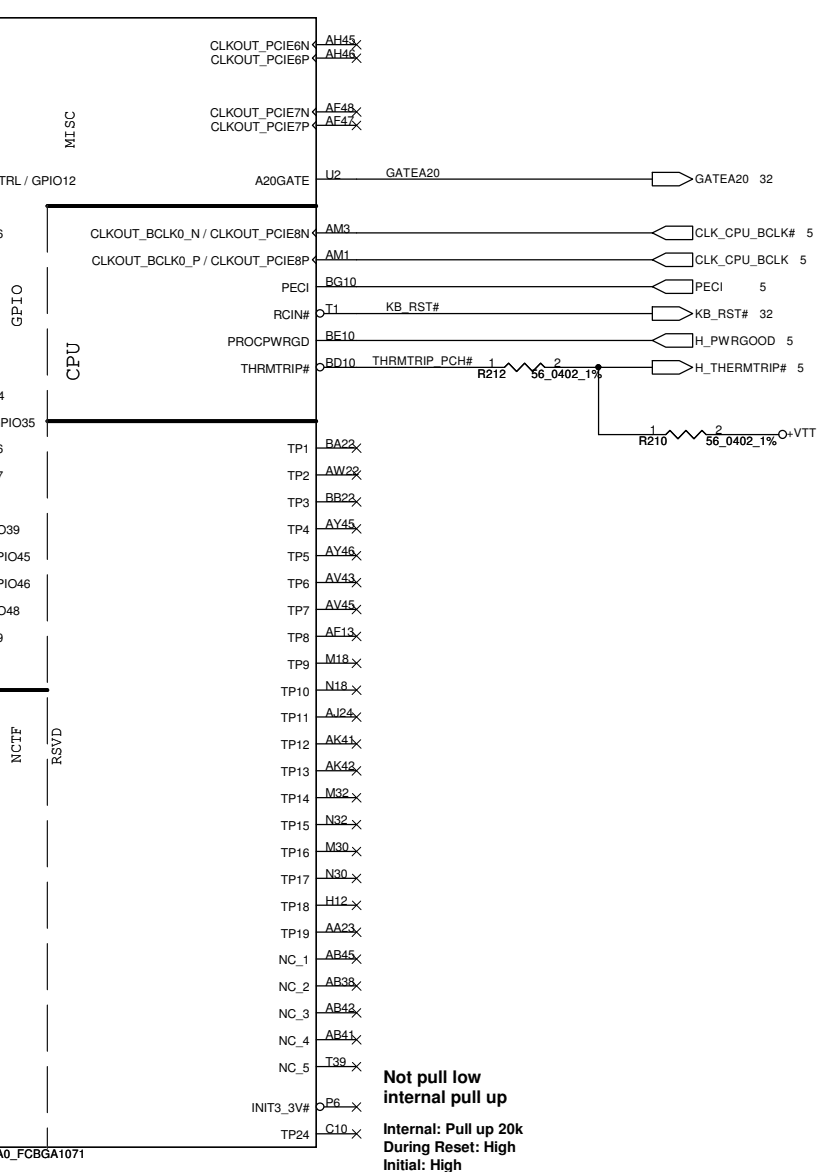
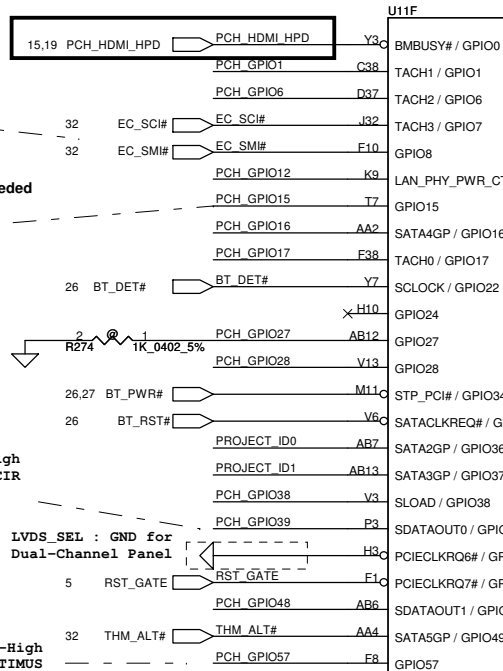
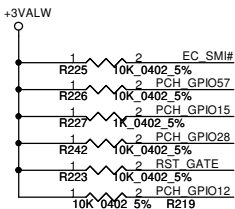
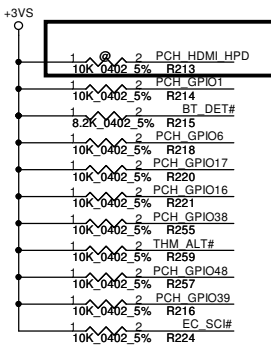
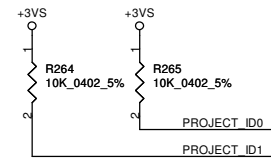
On-Die PLL VR	
PCH_GPIO27	High = Enabled (Default) Low = Disabled

**GPIO39:**  
**CIR\_EN# : Pull-High**  
**for non-support CIR**

**LVDS\_SEL : GND for**  
**Dual-Channel Panel**

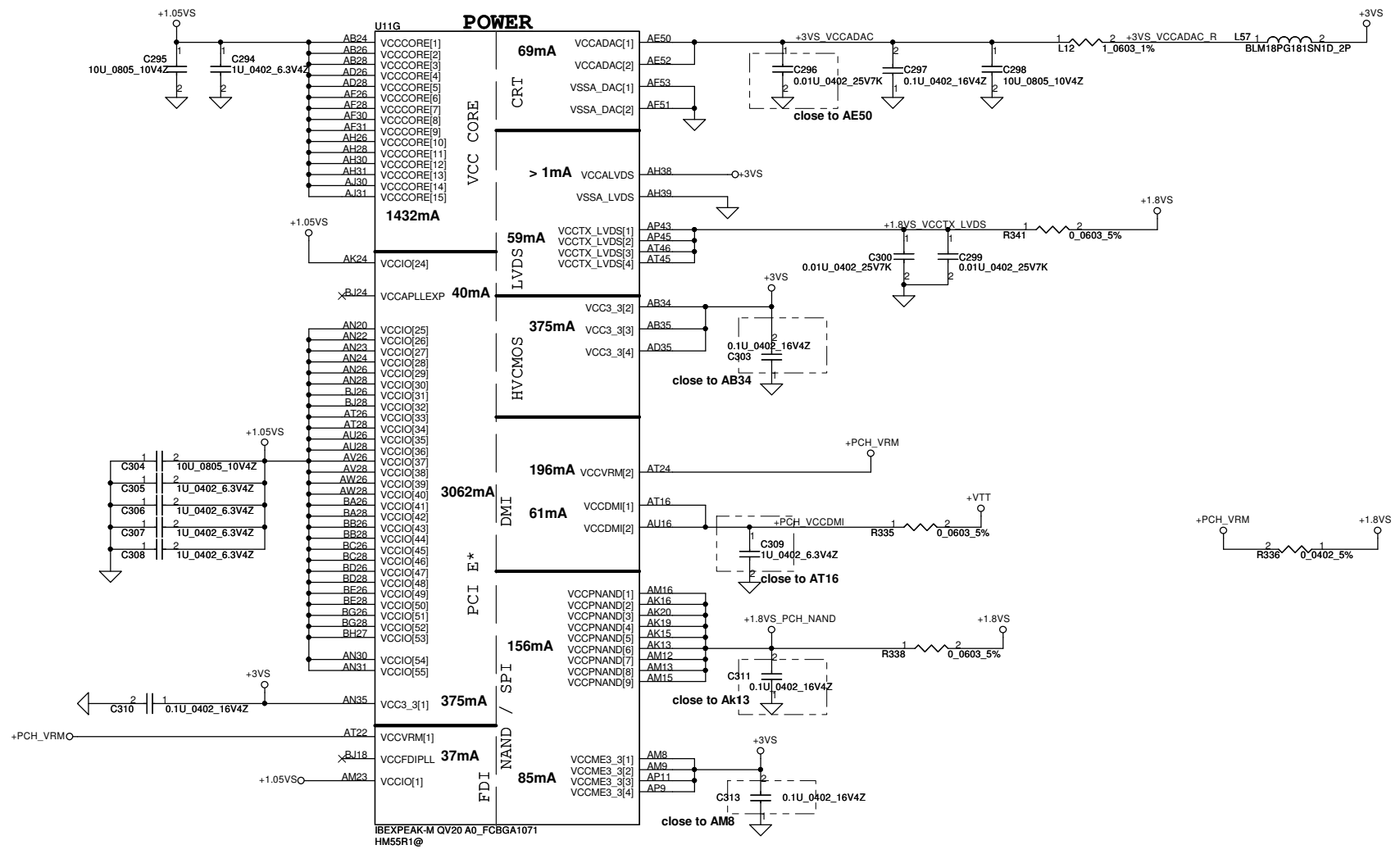
**GPIO57:**  
**OPTIMUS\_EN# : Pull-High**  
**for non-support OPTIMUS**

PROJECT_ID			
Name	ID0	ID1	
NBQAA 11.6/13.3"	L	L	
NBQAA 14"	L	H	
NWQAA 16"	H	L	
*NALAA 17.3"	H	H	



**Not pull low**  
**internal pull up**  
**Internal: Pull up 20k**  
**During Reset: High**  
**Initial: High**

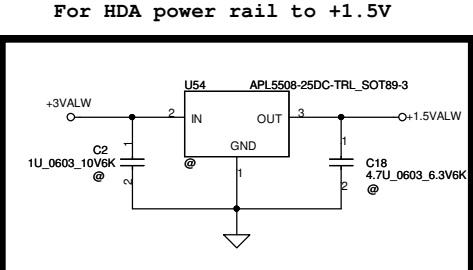
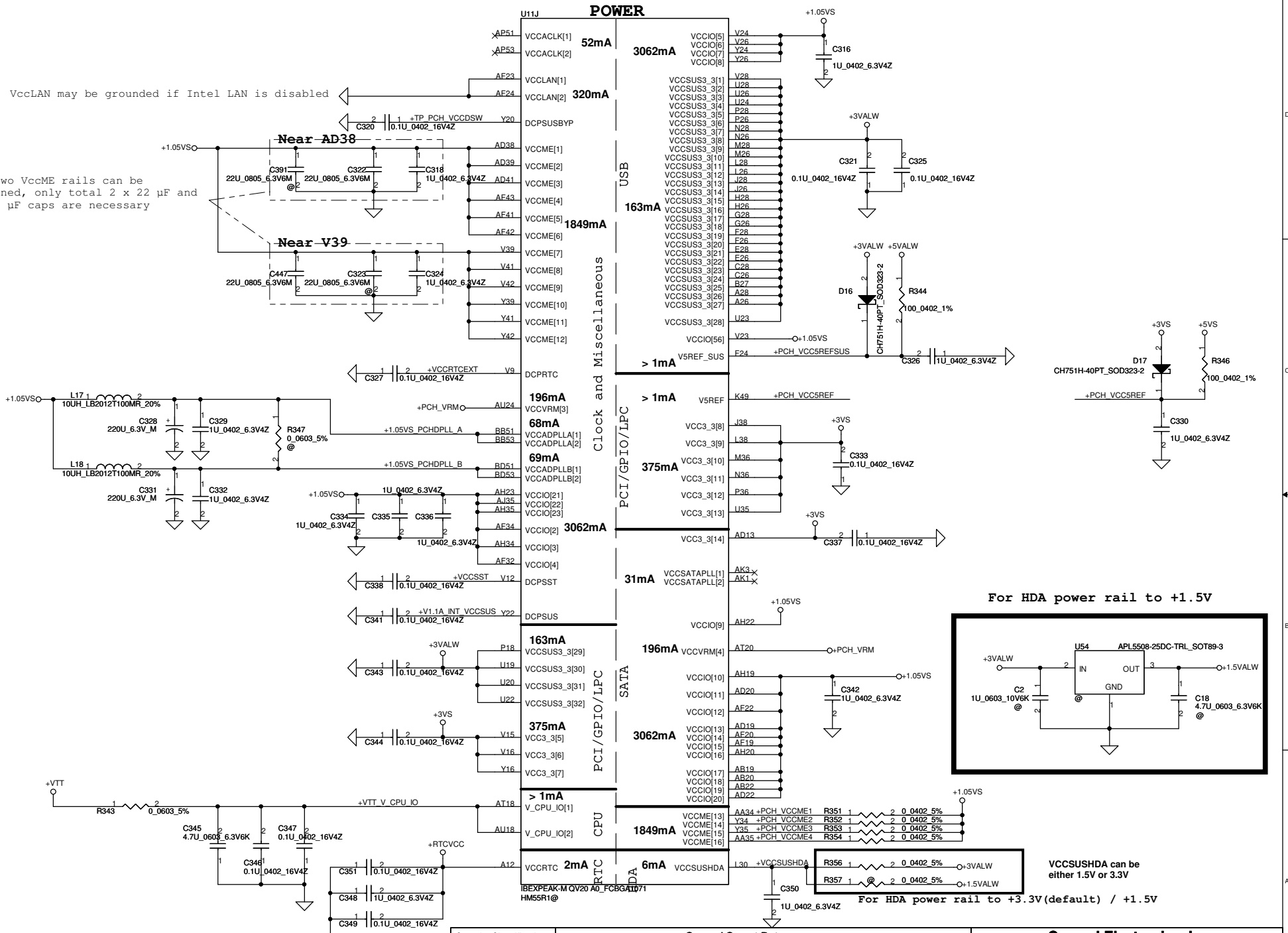
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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	
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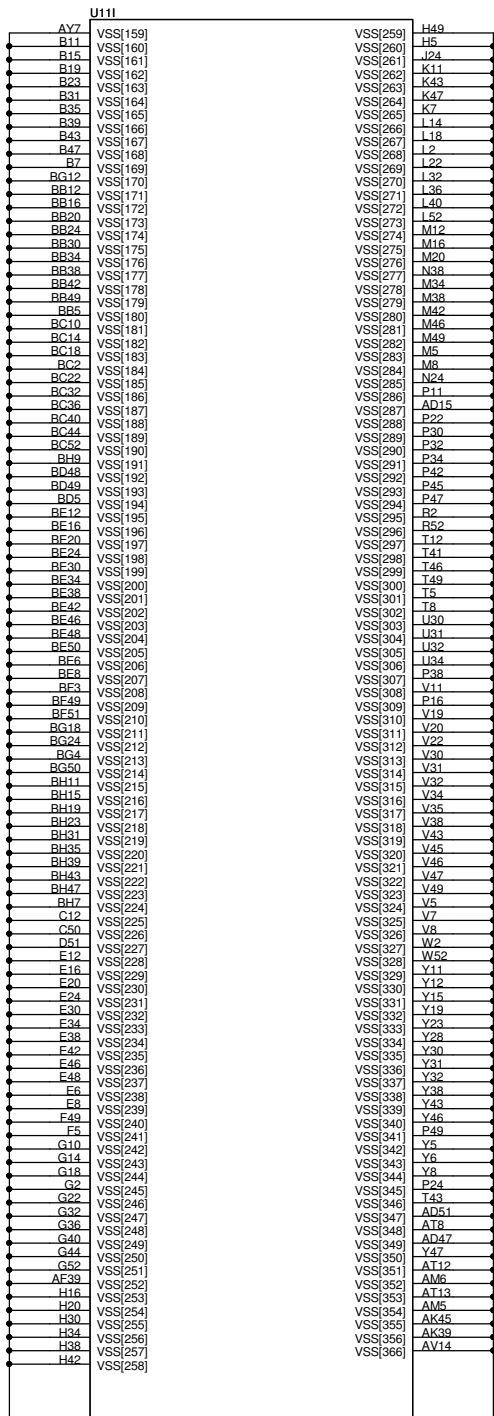
VccLAN may be grounded if Intel LAN is disabled

If two VccME rails can be combined, only total 2 x 22 µF and 2 x 1 µF caps are necessary

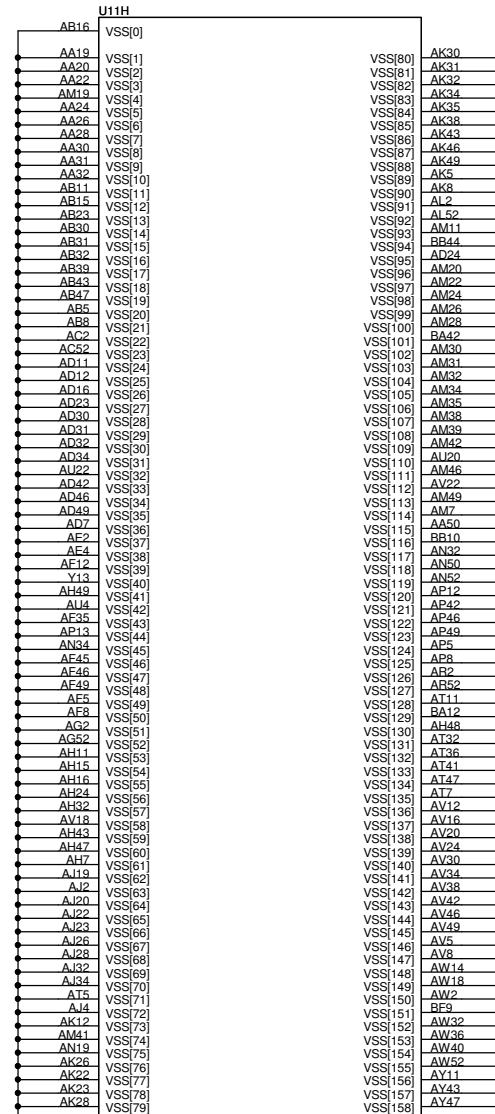


VCCSUS\_HDA can be either 1.5V or 3.3V  
For HDA power rail to +3.3V(default) / +1.5V

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Size		Document Number		Rev	
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Date:		Tuesday, April 13, 2010		Sheet 23 of 48	



IBEXPEAK-M QV20 A0\_FCBGA1071  
HM55R1@

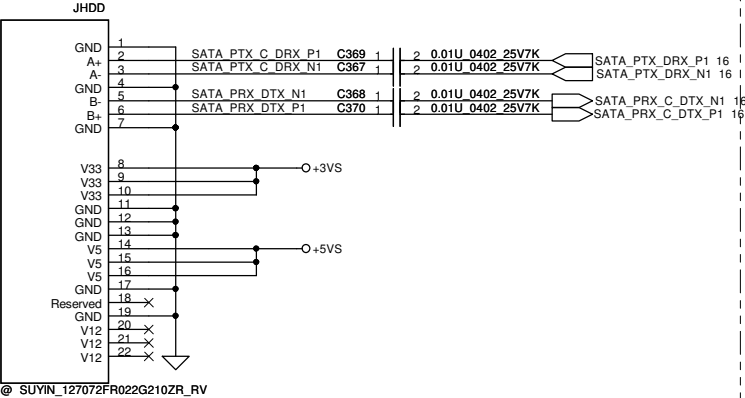
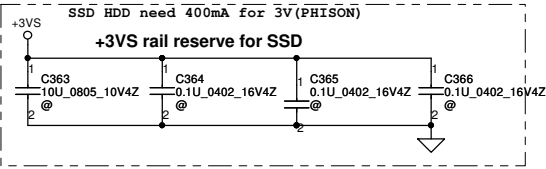
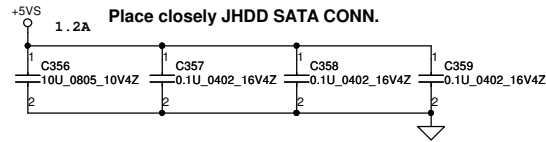


IBEXPEAK-M QV20 A0\_FCBGA1071  
HM55R1@

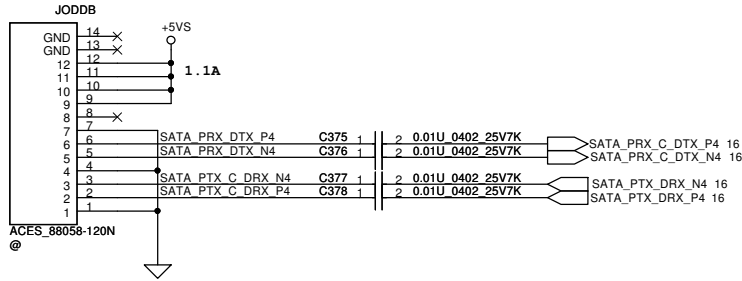
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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	
				PCH-GND	
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		Customer	NALAA LA-6041P M/B		
Date:	Tuesday, April 13, 2010	Sheet	24	of	48



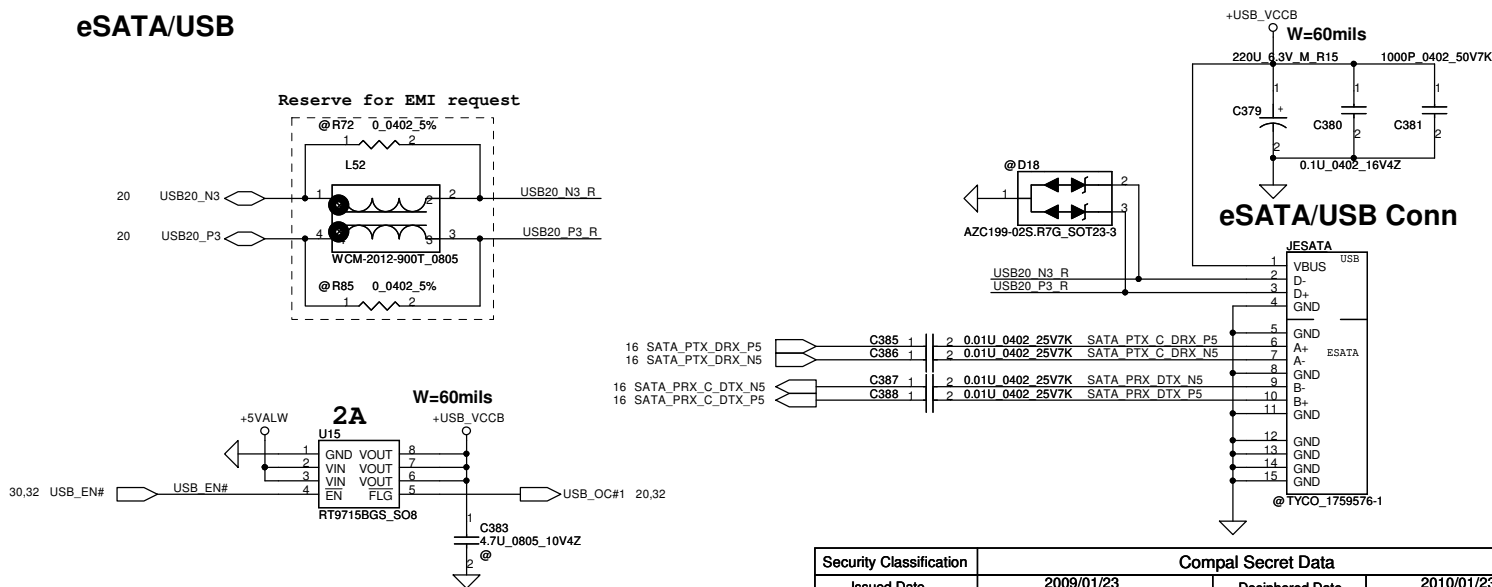
# SATA HDD Conn.



# SATA ODD Conn



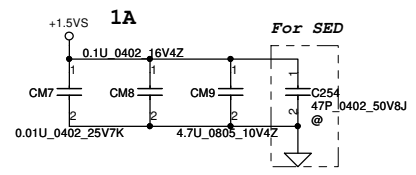
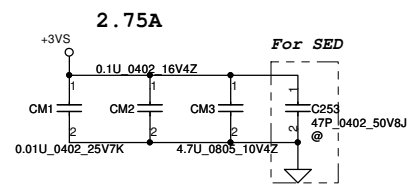
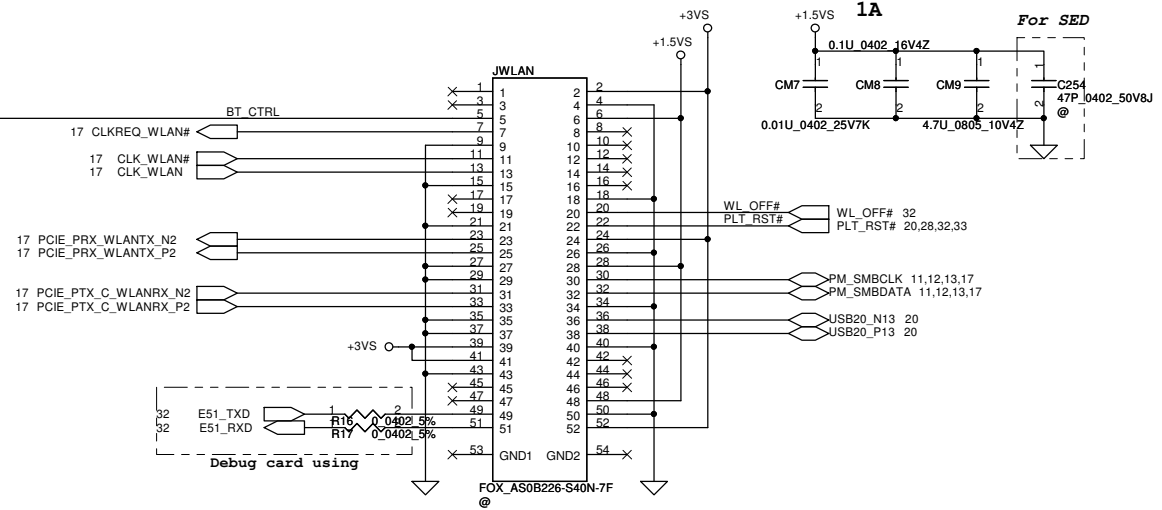
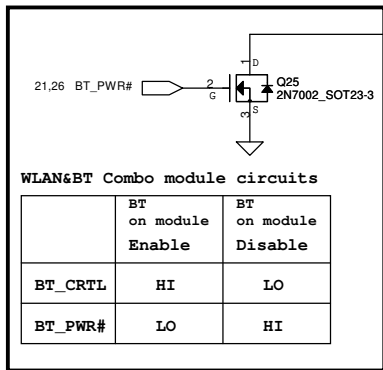
# eSATA/USB



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				Size	Document Number
				NALAA LA-6041P M/B	
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# PCIe Mini Card-WLAN/WiMax



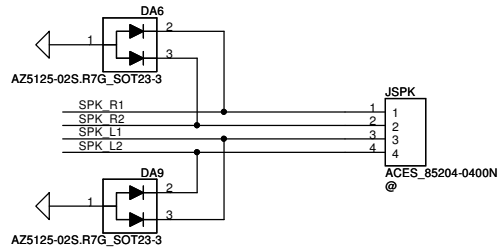
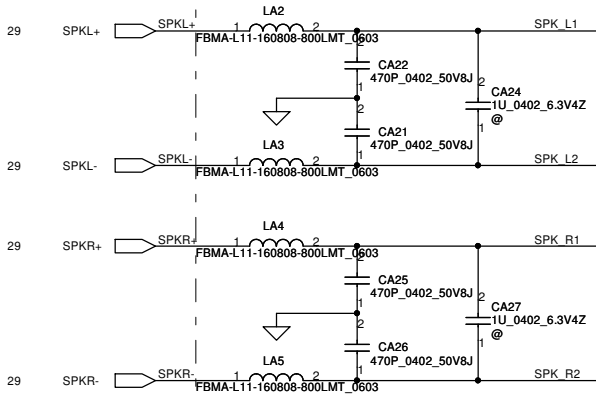
Security Classification	Compal Secret Data		Title	
Issued Date	2009/01/23	Deciphered Date	2010/01/23	Compal Electronics, Inc.
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Size	Document Number			Rev
	NALAA LA-6041P M/B			1.0
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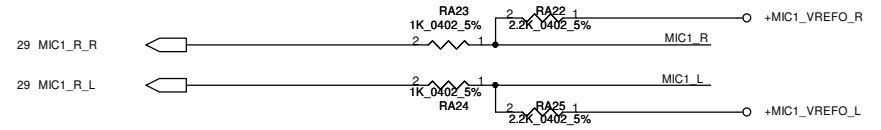


# Speaker Connector

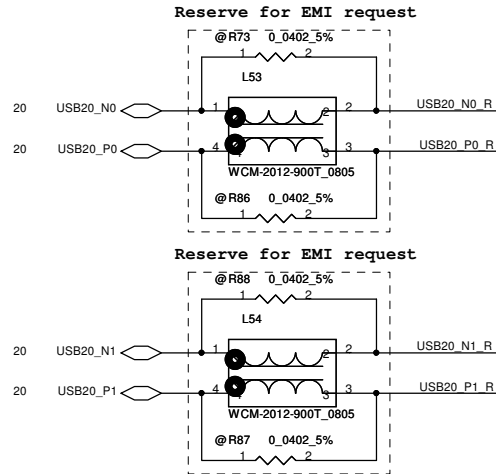
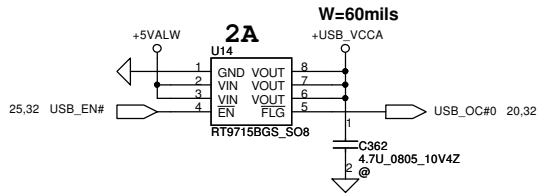
placement near Audio Codec



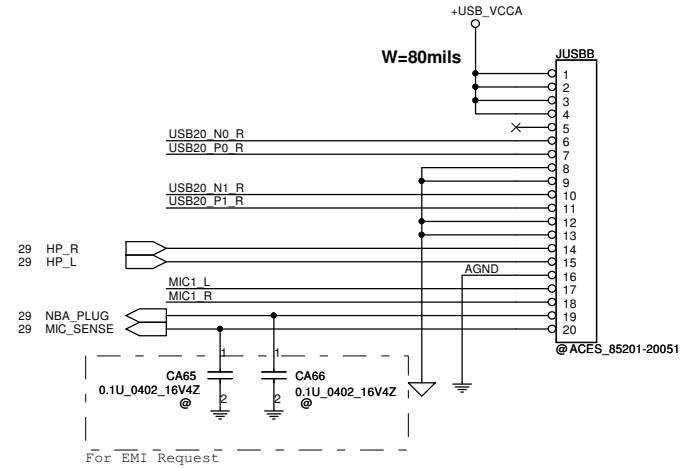
## Ext.MIC/LINE IN



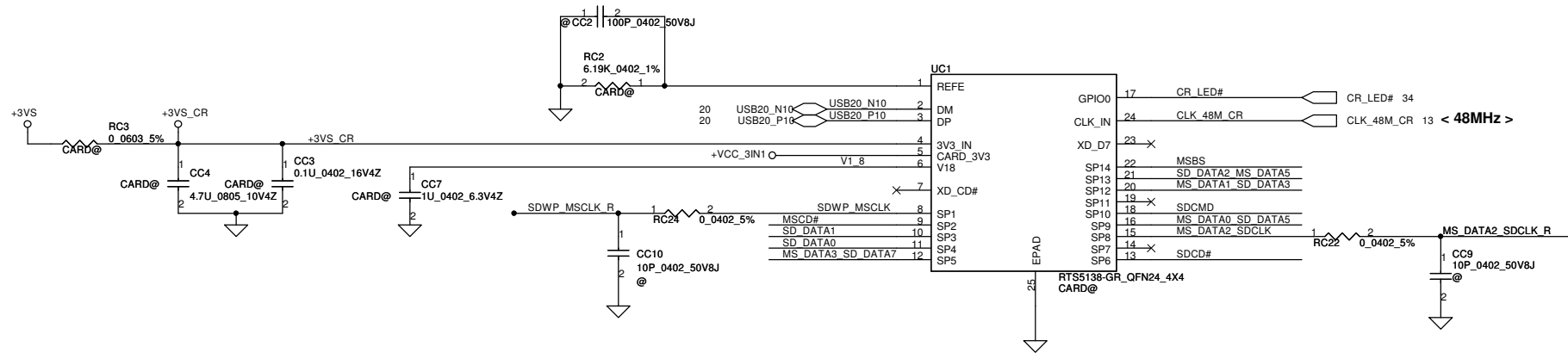
# USB Board



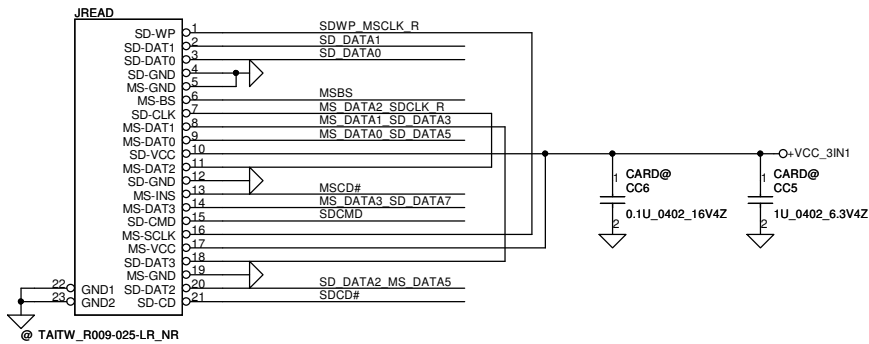
## Audio & USB Sub-Board Conn.



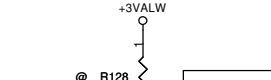
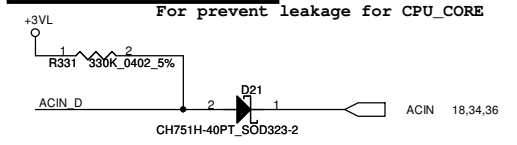
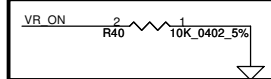
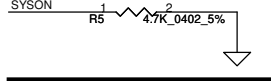
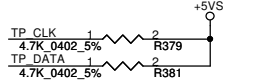
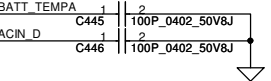
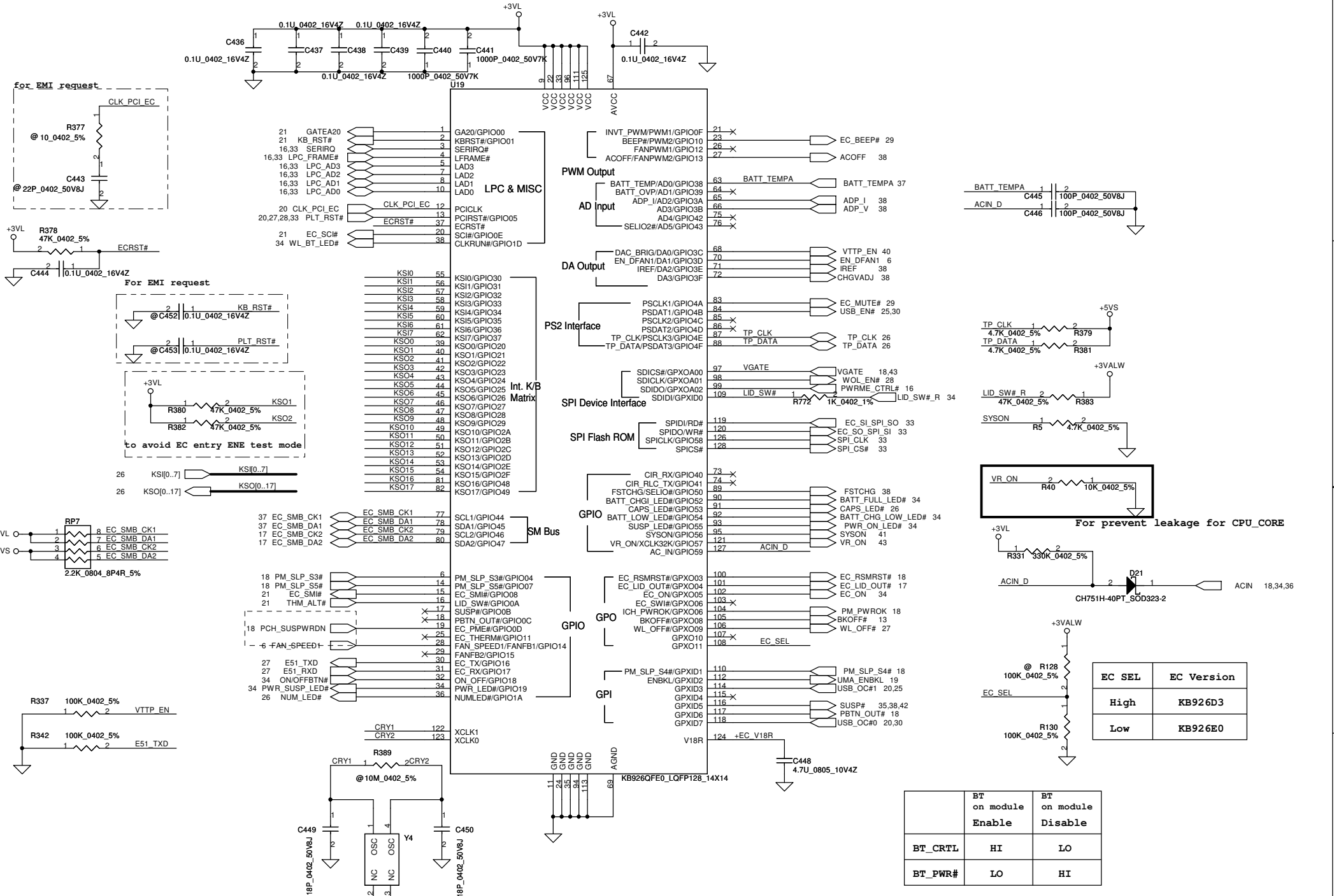
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< 3 in 1 Card Reader >



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				Date:	Tuesday, April 13, 2010
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EC SEL	EC Version
High	KB926D3
Low	KB926E0

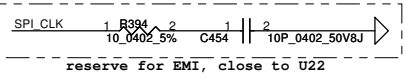
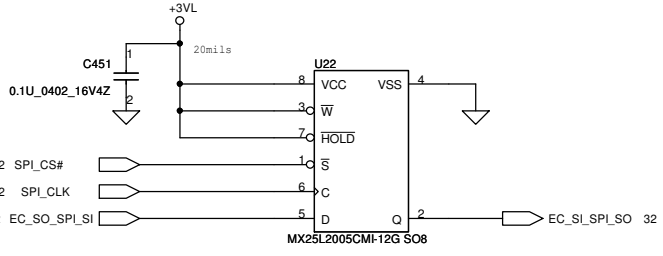
	BT on module Enable	BT on module Disable
BT_CTRL	HI	LO
BT_PWR#	LO	HI

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Size	Document Number	NALAA LA-6041P M/B		Rev	1.0
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# SPI Flash (256KB)

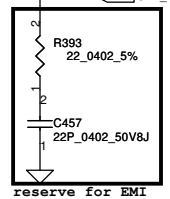
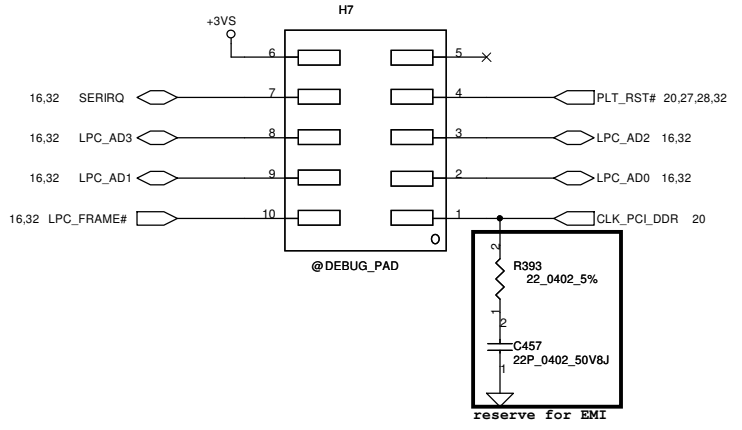
Socket: SP07000F500 & SP07000H900



reserve for EMI, close to U22

# LPC Debug Port

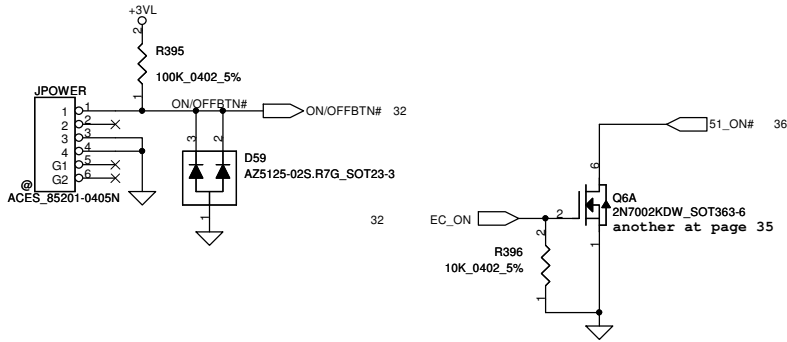
Please place the PAD under DDR DIMM.



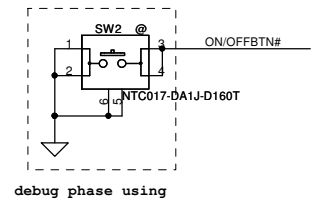
reserve for EMI

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				Size
				NALAA LA-6041P M/B
				1.0
Date: Tuesday, April 13, 2010			Sheet	33 of 48

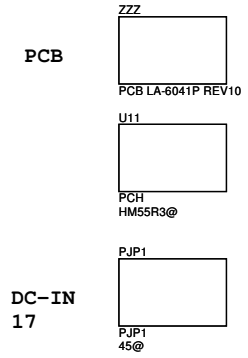
# Power Button



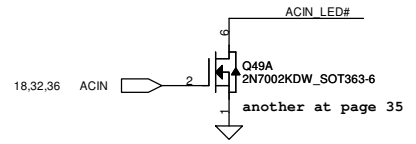
# Debug Button



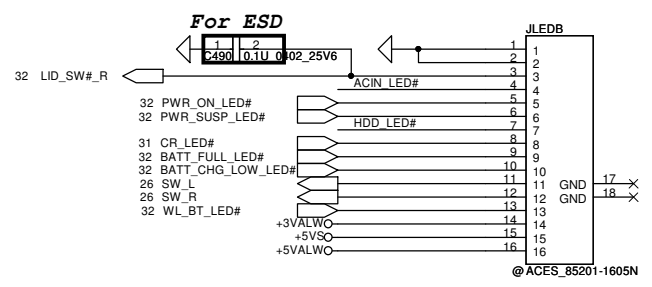
# ISPD



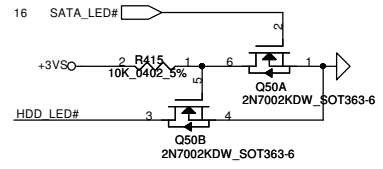
# DC-IN LED Control Circuit



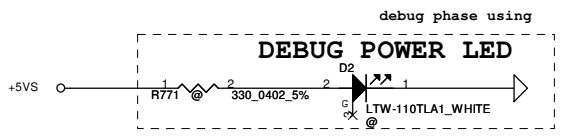
# LED/B Conn.



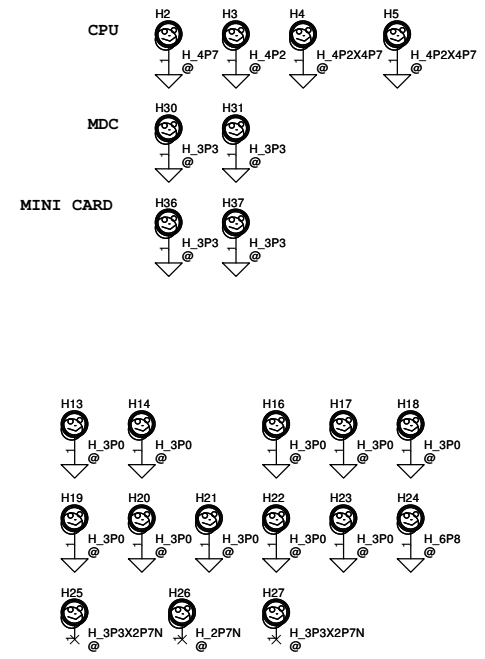
# HDD LED Control Circuit



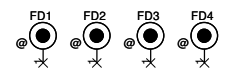
# POWER LED Control Circuit



# Screw Hole

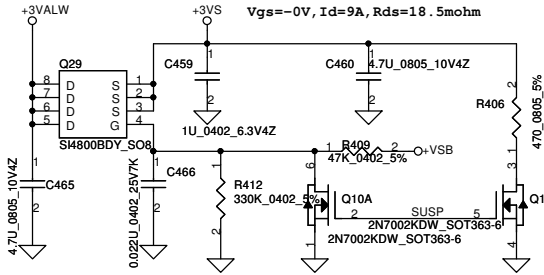


# PCB Fedical Mark PAD

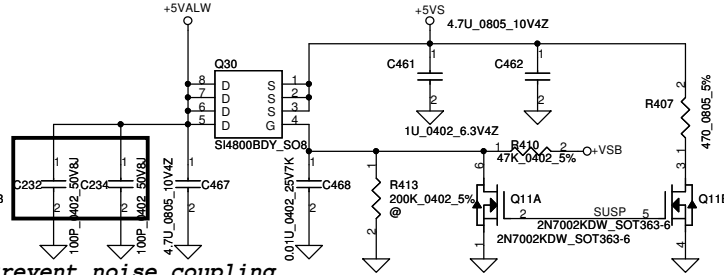


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Size	Document Number	NALAA LA-6041P M/B		Rev	1.0
Date:	Tuesday, April 13, 2010	Sheet	34	of	48

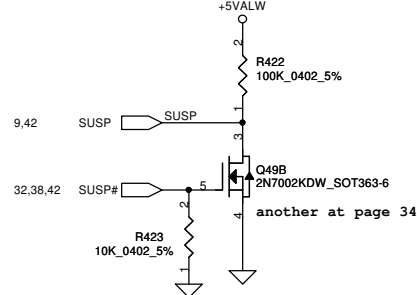
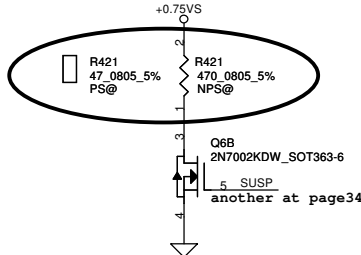
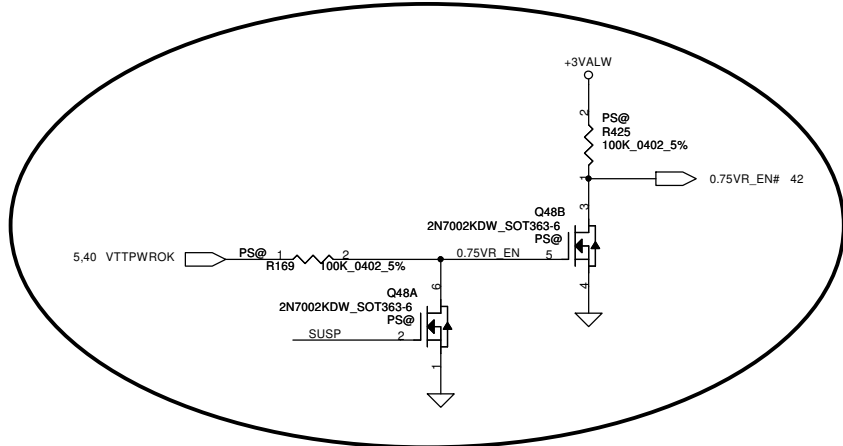
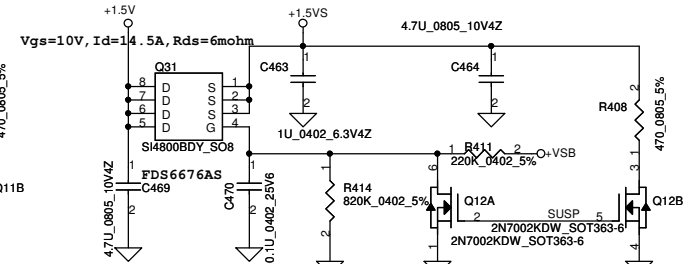
**+3VALW TO +3VS**



**+5VALW TO +5VS**

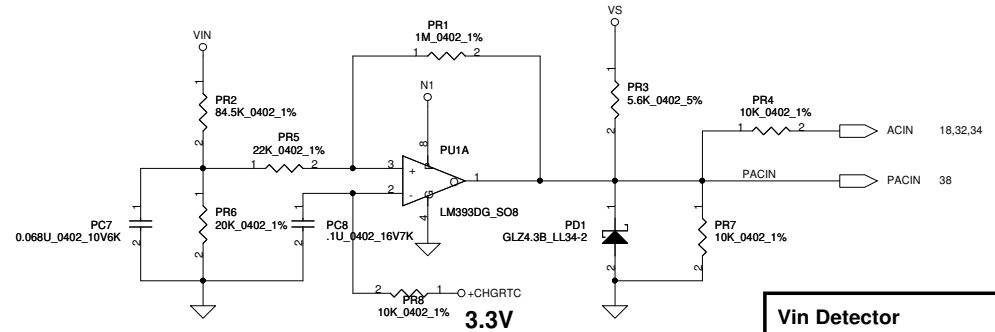
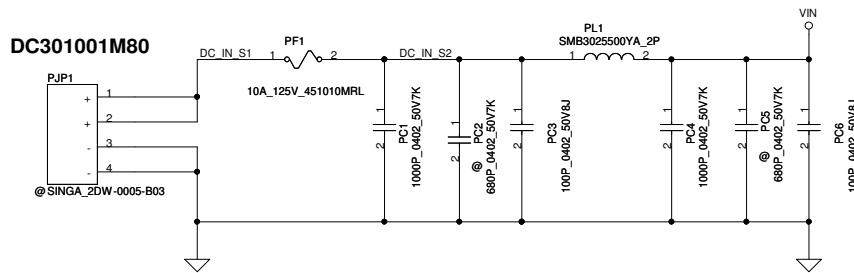


**+1.5V to +1.5VS**

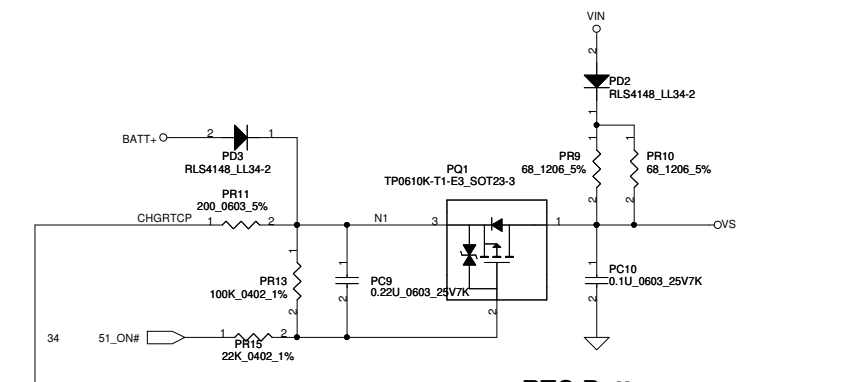


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2009/01/23		2010/01/23		NALAA LA-6041P M/B	
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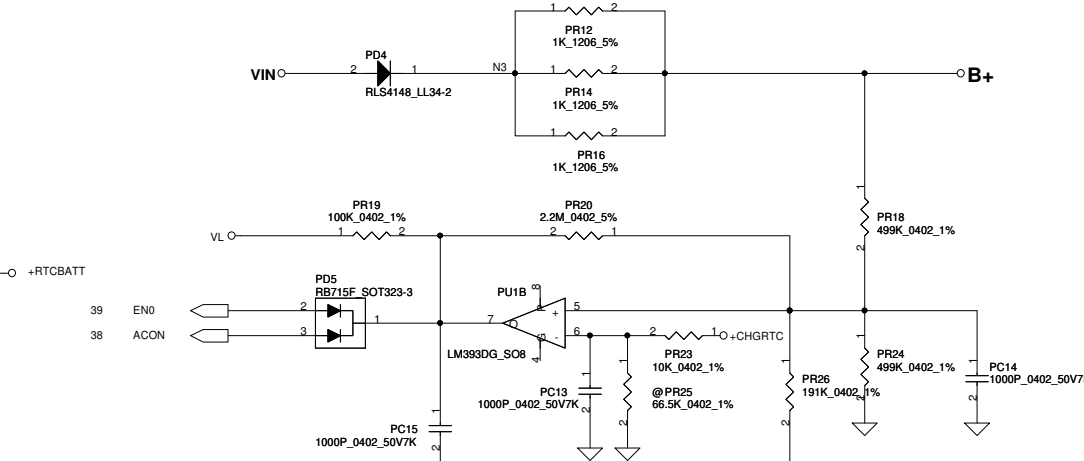
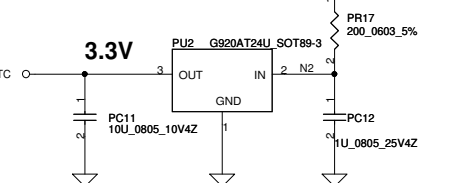
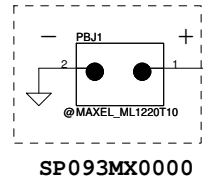
**DC301001M80**



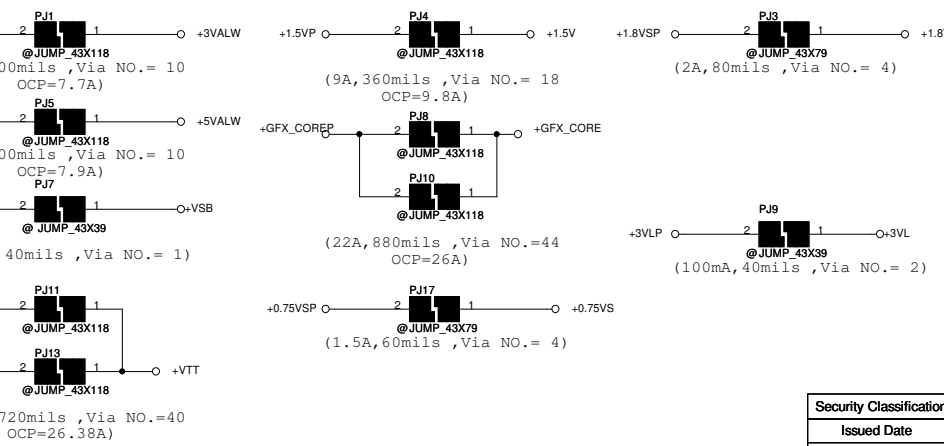
**Vin Detector**  
 High 18.384 17.901 17.430  
 Low 17.728 17.257 16.976



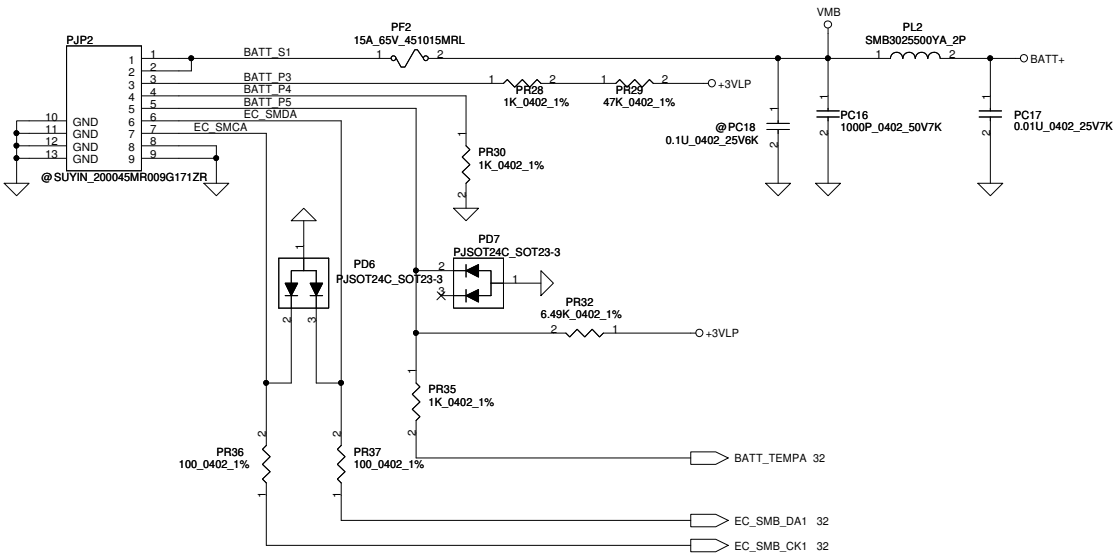
**RTC Battery**



**Precharge detector**  
 15.97V/14.84V FOR  
 ADAPTOR

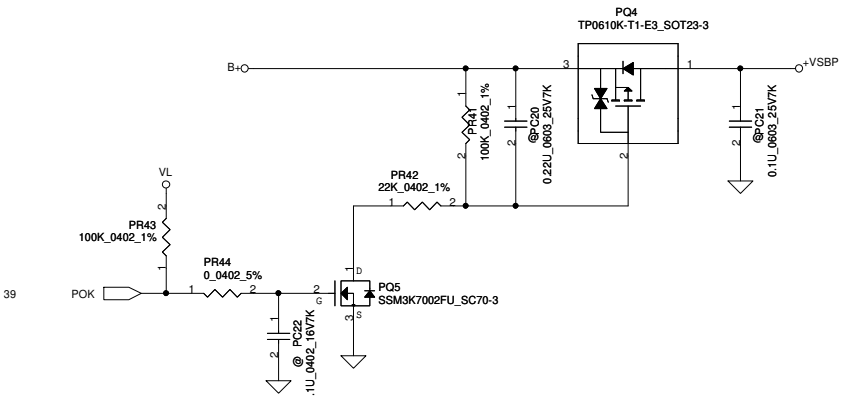
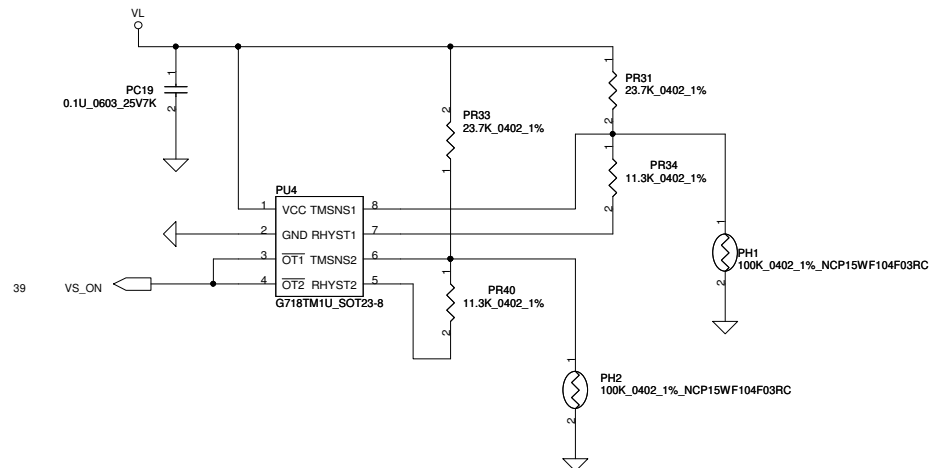


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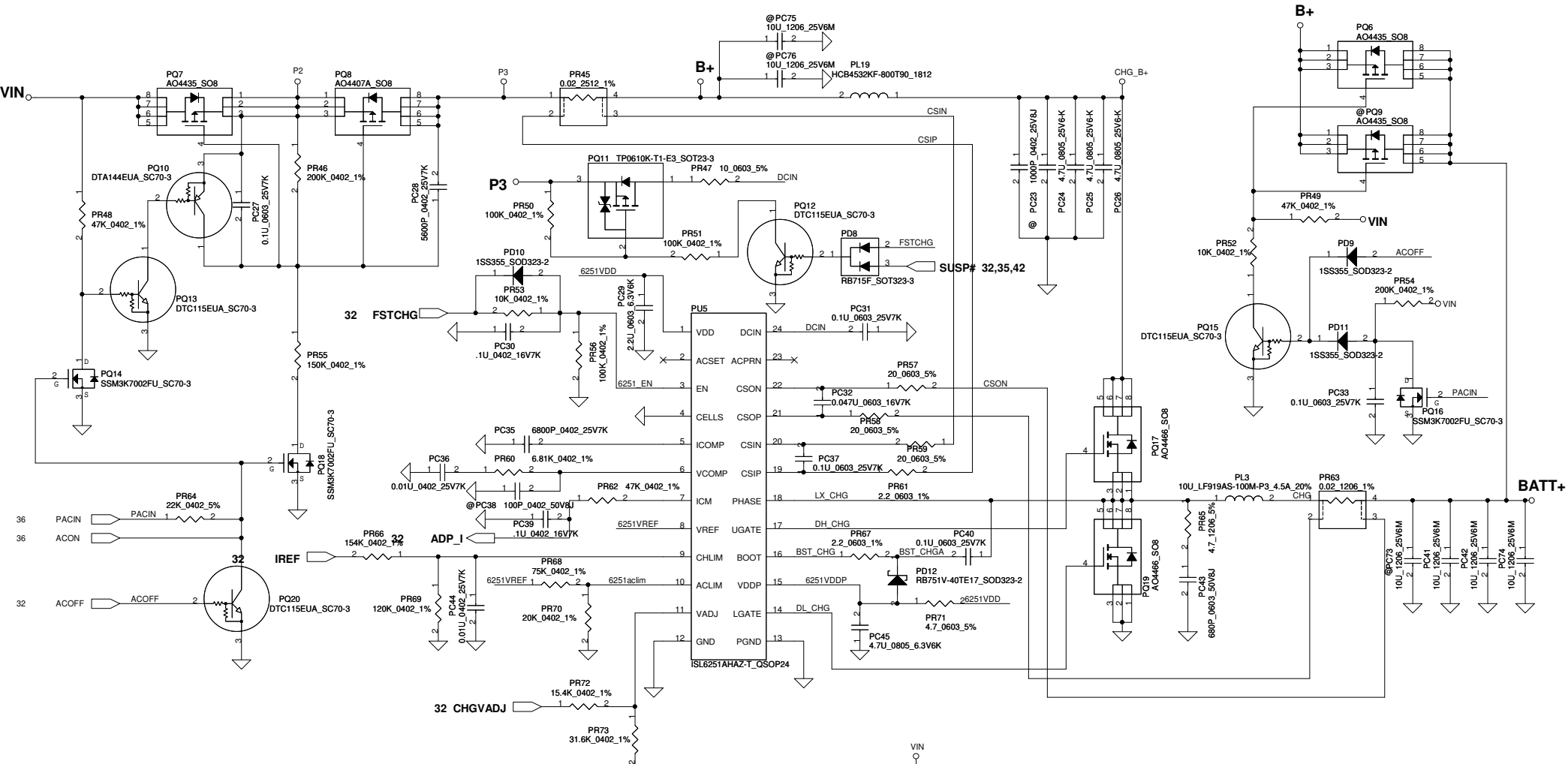


**PH1 under CPU botten side :**  
 CPU thermal protection at 90 degree C  
 Recovery at 56 degree C

**PH2 near main Battery CONN :**  
 BAT. thermal protection at 90 degree C  
 Recovery at 56 degree C



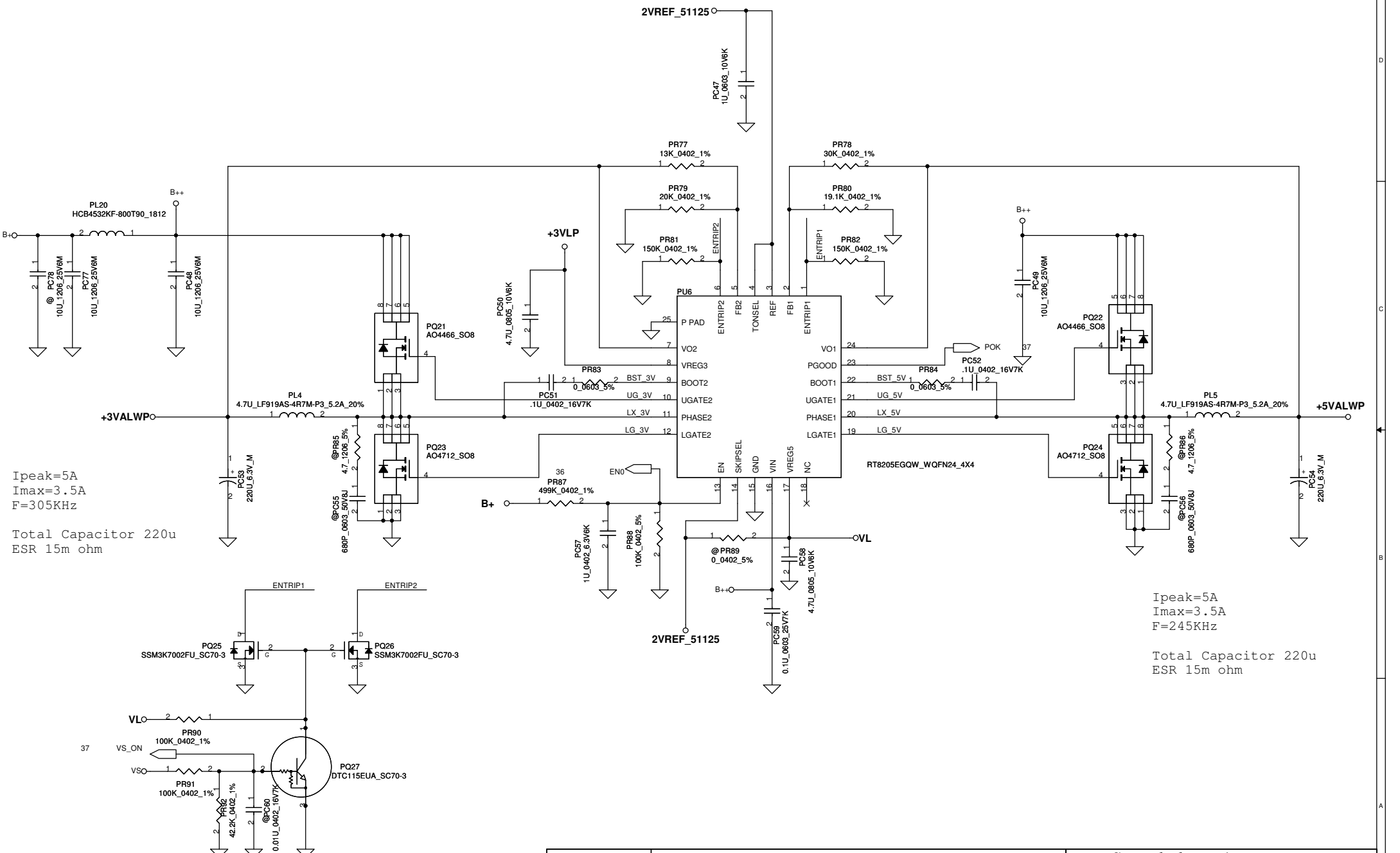
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Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	
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CP mode  
 $I_{ada} = 0 \sim 3.42A (65W)$  CP =  $92\% * I_{ada}$ ; CP = 3.147A  
 $V_{acLim} = 1.08V (65W)$  PR68 = 75k PR45 = 0.02

CC = 0.25A - 3A  
 $I_{REF} = 1.016 * I_{charge}$   
 $I_{REF} = 0.254V \sim 3.048V$   
 VCHLIM need over 95mV

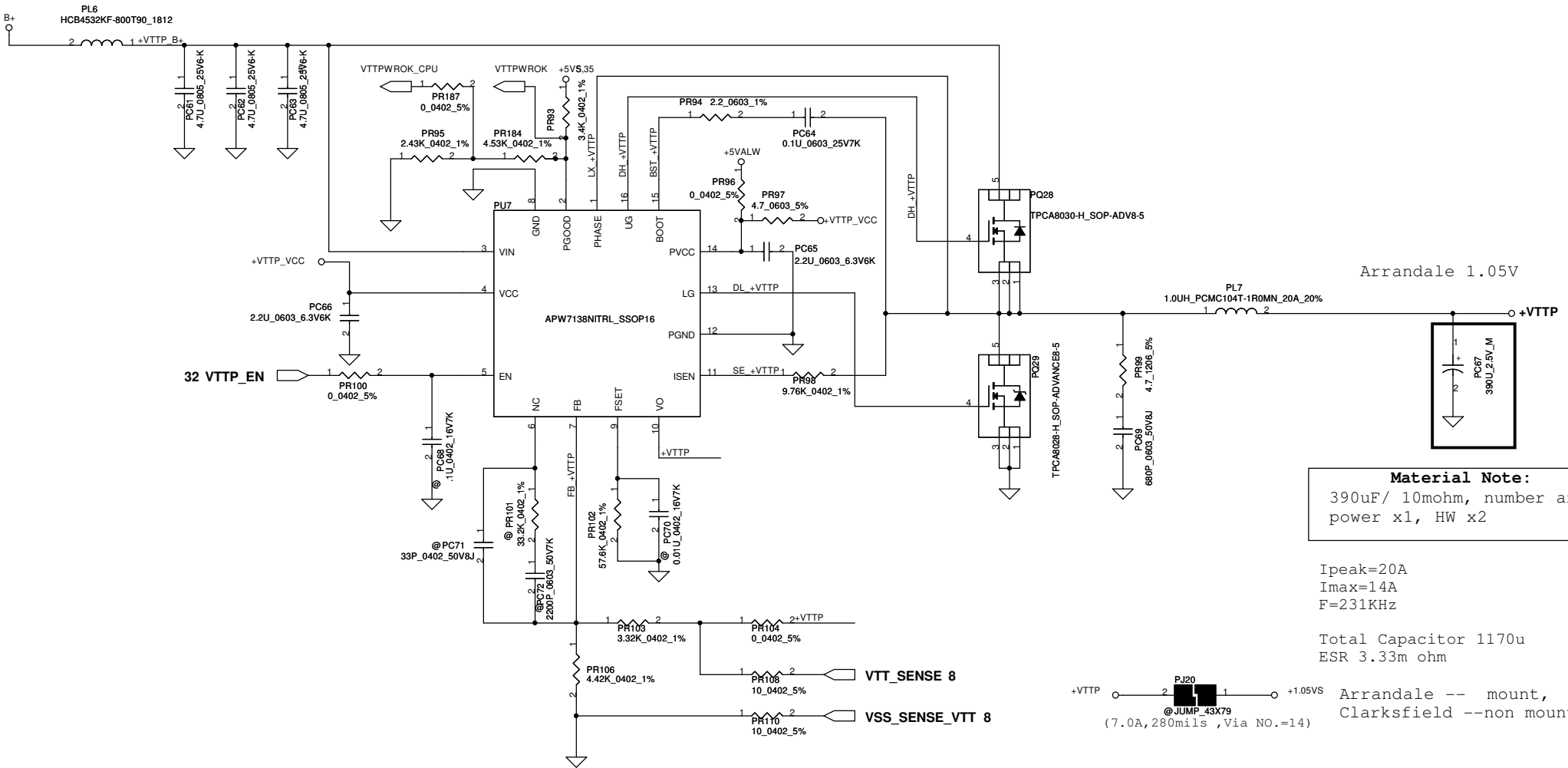
CHGVADJ = $(V_{cell} - 4) / 0.10627$	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V



Ipeak=5A  
 Imax=3.5A  
 F=305KHz  
 Total Capacitor 220u  
 ESR 15m ohm

Ipeak=5A  
 Imax=3.5A  
 F=245KHz  
 Total Capacitor 220u  
 ESR 15m ohm

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				3VALWP/5VALWP	
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**Material Note:**  
 390uF/ 10mohm, number are 3,  
 power x1, HW x2

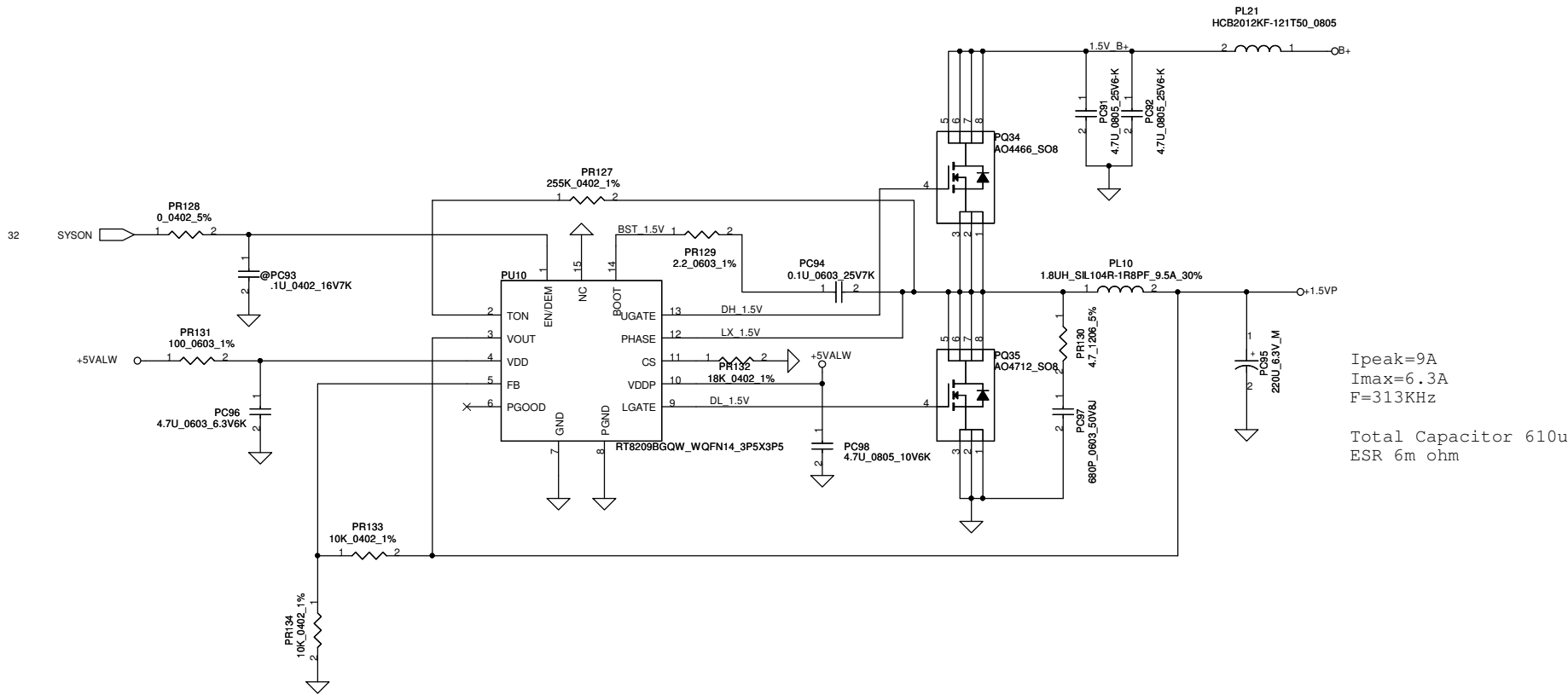
Ipeak=20A  
 Imax=14A  
 F=231KHz

Total Capacitor 1170u  
 ESR 3.33m ohm

Arrandale 1.05V  
 +VTTP  
 1.05VS  
 Arrandale -- mount,  
 Clarksfield --non mount @  
 (7.0A, 280mils, Via NO.=14)

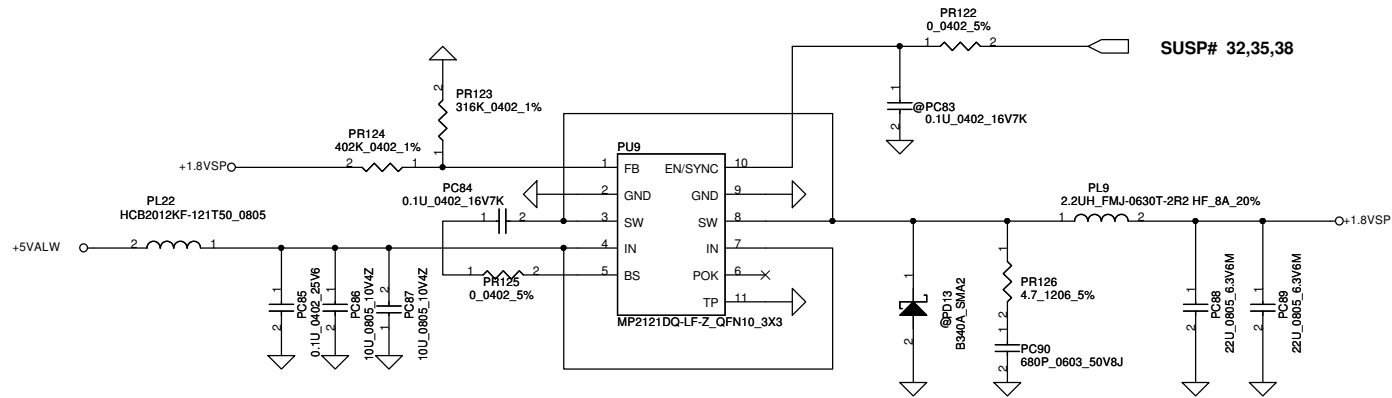
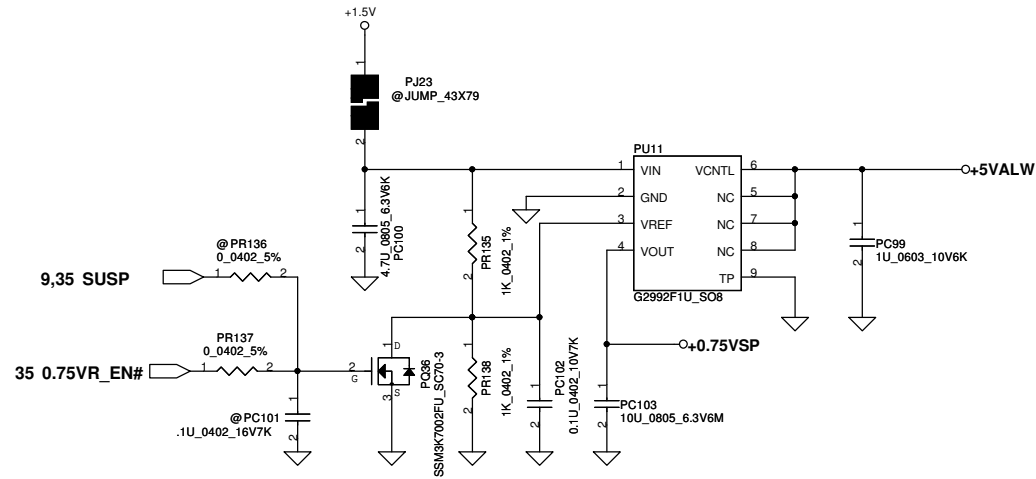
Security Classification		Compal Secret Data		Title <b>+VTTP</b>	
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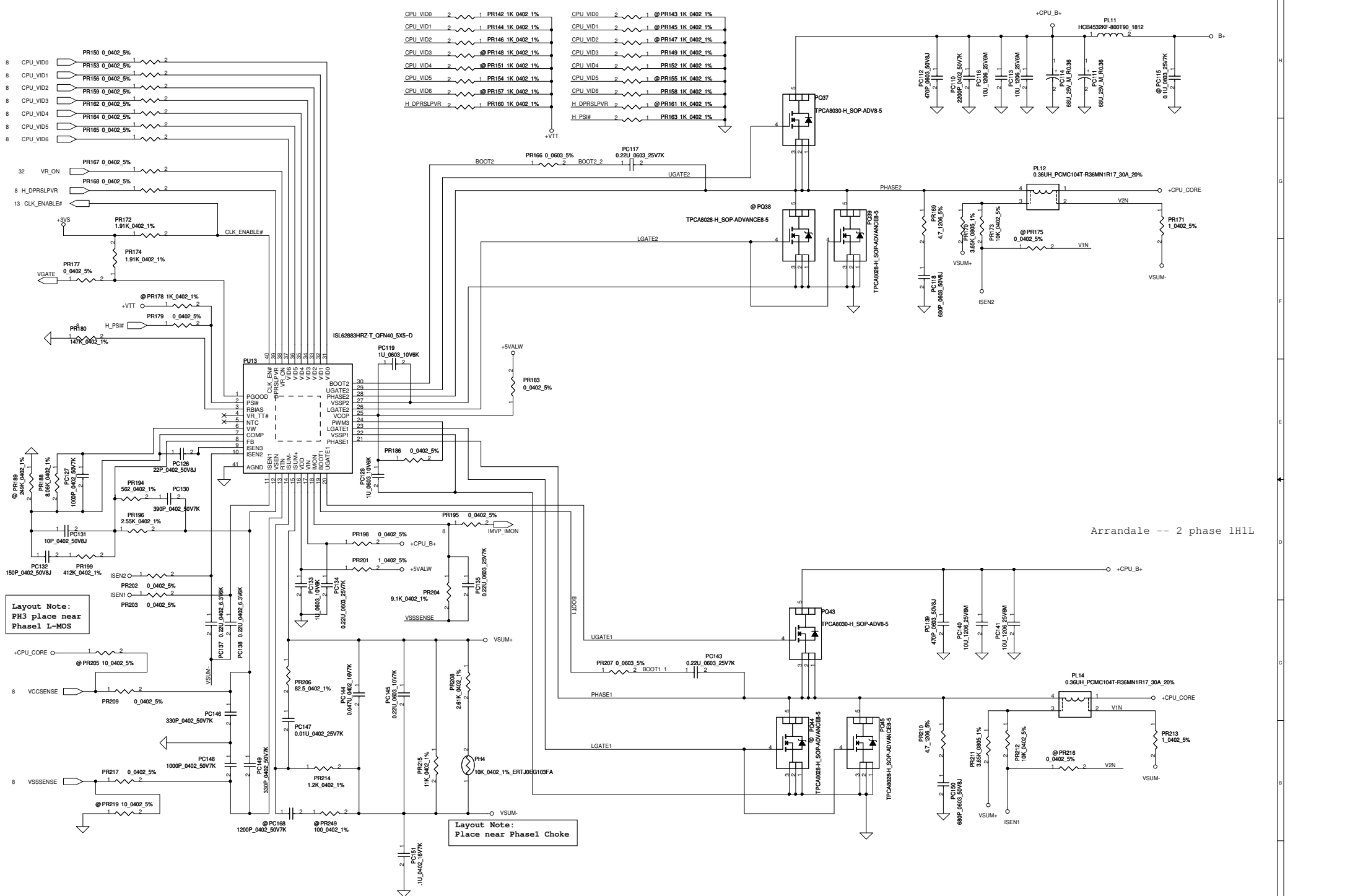
$I_{peak}=9A$   
 $I_{max}=6.3A$   
 $F=313KHz$   
 Total Capacitor 610u  
 ESR 6m ohm

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<b>Compal Electronics, Inc.</b>	
<b>0.75VSP/+1.8VSP</b>	
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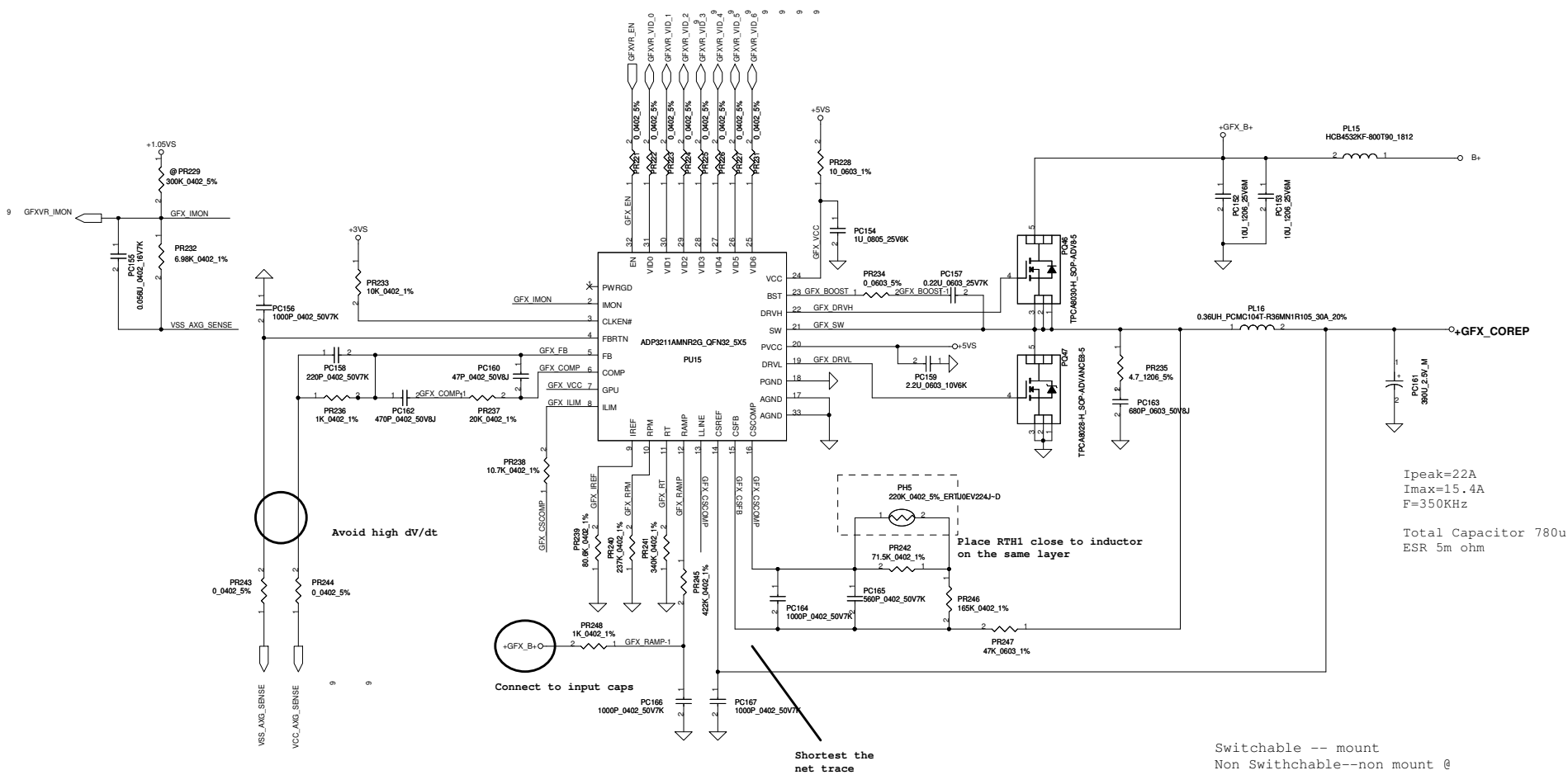


Arrandale -- 2 phase 1H1L

Layout Note:  
PH3 place near  
Phasel L-MOS

Layout Note:  
Place near Phasel Choke

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Title	+CPU_CORE			
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Ipeak=22A  
 I<sub>max</sub>=15.4A  
 F=350KHz  
 Total Capacitor 780u  
 ESR 5m ohm

Switchable -- mount  
 Non Switchable--non mount @

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# PIR (Product Improve Record)

## NALAA LA-6041P SCHEMATIC CHANGE LIST REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
11/26	34		Change C296,C299,C300,CA64,CM1,CM7 from SE072103280 to SE068103K80	For reduce BOM type
12/09	34		Connect JLEDB.15&16 to GND	For T/P SW issue
12/09	25,30		Change U14 & U15 from SA00002XX00 to SA000033H00	For material issue
12/16	15		Change R159 from IHDMI@ to @	For HDMI level shift disable function
12/16	31		Change CC2 from CARD@ to @	For Card Reader issue
12/16	34		Modify JLEDB pin define	For customer concern
12/16	21		Del R222 and connect PCH GPIO45 to GND	For LVDS_SEL (Dual-Channel)
12/16	13		Change U5 from SA00003HQ00 to SA00003HQ10	For CLK GEN update
12/16	27		Add R22 and Net BT_PWR#_R to connect JWLAN Pin5	For BT/WLAN combo Mini Card
12/16	16		Change U13 footprint to M25P80-VMW6TP_S08 and delete BOM structure.	For delete ROM socket
12/16	34		Change H36, H37 from H_3P3 to H_3P8.	For ME modify
12/16	26		Reverse JBT pin definition	For ME modify
12/16	31		Change CC2 from 0.1u to 100P (SE071101J80) and add BOM structure @.	For Card Reader issue
12/16	34		Change JPOWER footprint to ACES_85201-0405N_4P.	For ME modify
12/16	26		Change JTPB footprint to P-TWO_161011-04021_4P-T.	For ME modify
12/16	34		Change JLEDB footprint to ACES_85201-1605N_16P	For ME modify
12/16	30		Change JUSBB footprint to ACES_85201-20051_20P	For ME modify
12/16	34		Del H15	For ME modify
12/21	34		Change H36,H37 from H_3P8 to H_3P3	For ME modify
12/21	13		Change +LCD_INV from JLVDS.35 to JLVDS.40	For prevent burn issue
12/21	13		Change BKOFF#_R from JLVDS.40 to JLVDS.35	For prevent burn issue
12/23	16,32		Change net name from PWRME_CTRL to PWRME_CTRL#	For signal is LOW active
12/23	08		Add C125 SF000002Y00	For co-lay with C123
12/23	09		Del C128	For del co-lay with C185
12/23	09		Del C140	For del co-lay with C217
12/23	17		Change Y2 P/N from SJ125P0M200 to SJ100003300	For cost down plan
12/23	27		Delete R22 and BT_PWR#_R and add Q25 and BT_CTRL at JWLAN pin5	For BT/WLAN combo Mini Card
12/24	29		Change RA26 to L56 bead 300 ohm FBMA-L10-160808-301LMT(SM010017710)	For EMI issue
12/24	15		Add R96 1K ohm to connect HDMI_HPD and U9.1	For prevent U9 ESD damage issue
12/24	30		Change LA2,LA3,LA4,LA5 to 80 Ohm bead FBMA-L11-160808-800LMT (SM010015410)	For EMI request
12/24	30		Change CA21,CA22,CA25,CA26 to 470P (SE071471J80)	For EMI request
12/24	26		Del R361 BOM structure BT@ (always mount)	For BT function
12/28	26		Change R392 BOM structure from BT@ to @.	For BT function
12/28	26		Change C159,C160,C185,C217,C268 footprint from C_PXC6P3VC220MF60 to C_MP2VU390MC5R7.	
12/28	25		Change JODDB footprint to ACES_88058-120N_12P-T.	For DFX request
12/29	13		Del C292	Only for NSWAA
12/29	28		Change UL3 P/N from SP050005W00 to SP050005V00	For EMI request
12/29	28		Change UL1 P/N from SA00003PO00 to SA00003PO10	For IC chip revise version
01/05	06		Change C4 from SE068102J80 to SE074102K80	For component common design

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				HW PIR 0.1 TO 0.2	
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**NALAA LA-6041P SCHEMATIC CHANGE LIST REVISION CHANGE: 0.2 TO 0.3**

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
01/19		13	Change BKOFF#_R from JLVDS.35 to JLVDS.33	For prevent burn issue
01/27		32	Add pull down R40 10Kohm at VR_ON.	For prevent leakage for CPU_CORE
01/27		25	Change D18 from SCA00000A00 to SC600001600	For ESD request
01/27	13,26,30,34		Change D57,D58,D59,DA6,DA9 from SCA00000G00 to SCA00001A00	For ESD request
01/27		15	Add pull down R148 2.2Kohm at HDMI_TXC-.	For UMA HDMI level shift display compatibility issue
01/27		28	Change UL3 from SP050005W00 to SP050005V00	For ESD request
01/27		29	Change UA1 from SA00003QR00 to SA00003QR10	For Realtek update
01/27		32	Change R128 BOM structure from mount to un-mount.	For EC update
01/27		32	Change R130 BOM structure from un-mount to mount.	For EC update
01/27		32	Change U19 from SA00001J580 to SA00001J5A0.	For EC update
02/01		30	Change JSPK pin define	For common SPK material
02/01		16	Add D19 & R133 between +RTCVCC and RTCVREF.	For prevent RTC empty then can not boot up issue
02/01		19	Change R77 from SD028100280 to SD028100380	For INTEL issue (pending interrupts from the PCH for unused HDMI ports)
02/01		05	Add C225	For prevent noise issue
02/04		22	Change L12 from SM010028480 to SHI00002K00	For CRT wave issue
02/04		28	Change LL1 from SHI00004T00 to SHI0000AA00	For package limitation, Realtek criteria, 2ND source reason
02/04		28	Change CL13 from SE000000I10 to SE107475K80	For package limitation, Realtek criteria, 2ND source reason

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**NALAA LA-6041P SCHEMATIC CHANGE LIST REVISION CHANGE: 0.3 TO 1.0**

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
02/23	15		Change R167 BOM structure from @ to IHDMI@.	For reduce HDMI choke plan
02/23	15		Change R163 BOM structure from IHDMI@ to @.	For reduce HDMI choke plan
02/23	15		Change R160 from SD028330180 (3.3K ohm) to SD034390180 (3.9K ohm).	For reduce HDMI choke plan
02/23	15		Change L8,L9,L10,L11 BOM structure from IHDMI@ to @.	For reduce HDMI choke plan
02/23	15		Change R157,R173,R175,R180,R182,R183,R187,R188 BOM structure from @ to IHDMI@.	For reduce HDMI choke plan
02/23	22		Change L12 from SHI00002K00 (10UH +-20%) to SD008100B80 (1 ohm +-1% 0805).	For CRT wave issue
02/23	16		Delete D19 & R133	For prevent RTC empty then can not boot up issue
02/23	23		Change U54,C2,C18 BOM structure to @.	For reserve HDA power rail to +1.5V
02/23	26,34		Change SW2,SW4 from SN100000F00 to SN100002Y00 and add BOM structure @ at SW2.	For cost concern
03/09	29,32		Add Net EC_MUTE# from EC pin 83 to codec Pin4	For system has abnormally noise after S3 resume.
03/09	29		Add pull Low RA45 4.7K ohm.	For system has abnormally noise after S3 resume.
03/09	29		Change CA16 BOM structure to @.	For system has abnormally noise after S3 resume.
03/11	22		Add L57.	For prevent EMI and CRT wave issue.
03/11	25,30		Change U14,U15 from SA000033H00 to SA00002XX00.	For sourcer suggestion.
03/11	25,30		Change ZZZ from DA60000GC00 to DAZ0CK00100.	For Pre-MP phase.
03/11	06		Change U1 from SA00002XA00 to SA000035G00.	For voltage drop issue.
03/11	34		Change R771,D2 BOM structure to @.	For Pre-MP phase.
03/11	22		Add net name +3VS_VCCADAC_R	For net nameing rule
03/15	34		Add R772 & C490 and net name LID_SW#_R	For prevent ESD damage
03/15	22		Change L12 from SD008100B80 to SD014100B80.	For package size
03/16	29		Change CA12.1, RA12.2, CA18.2 connect to GNDA	For high frequency noise issue at S0
03/16	13		Add C231	For prevent noise coupling
03/17	35		Add C232,C234	For prevent noise coupling
03/17	31		Add CC9,CC10,RC22,RC24	For EMI request
03/17	31		Del RC2,RC3,CC7,CC8	For EMI request
03/20	13		Change C213 from SE070104Z80 to SE000000K80.	For prevent noise coupling
03/20	13		Change C231 from SE071101J80 to SE000000K80.	For prevent noise coupling
03/23	25		Change D18 BOM structure to @.	For EMI remove

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
	2009/10/20	45-54	Release	
	2009/12/21	39	Change PR92 to 42.2K ohm	circuit modify
	2009/12/21	40	Change PR95 to 2.43K ohm,PR101,PC71,PC72 to unmount ,PR98 to 6.49K ohm	circuit modify
	2009/12/21	42	Change PR136 to unmount,PR137 to mount,PC90 to SE024681J80	circuit modify
	2009/12/21	43	Change PQ44 to unmount,PQ45 to mount	EMI request
	2009/12/28	43	Change PC111,PC114 to 68U	DFB request
	2009/12/29	37	Change PR31 and PR33 to 19.6K ohm, PR34 to 8.66K ohm,PR40 to 7.87K ohm	circuit modify
	2009/12/29	38	Add PR139(0_0402_5%)	EMI test request
	2009/12/29	44	Change PH5 to SL200000500	circuit modify
	2010/01/05	43	Change PR169,PR210,PC118 and PC150 to mount	EMI request
	2010/01/05	44	Change PR235 and PC163 to mount	EMI request
	2010/02/03		Change PR196 to 2.55K ohm,PR204 to 9.1K ohm	circuit modify
	2010/02/03	38	Change PC24,PC25,PC26 to 10U_1206,PR67 to 2.2 ohm PC74 to mount,PC23 to 1000P	EMI request
			Delete PR139	circuit modify
	2010/02/03	39	Change PQ27 to DTC115EUA_SC70-3 Add PC77	EMI request
	2010/02/26	37	Change PR31,PR33 to 23.7K ohm,PR34,PR40 to 11.3K ohm Add PD6,PD7	Thermal request EMI request
	2010/03/16	38	Change PC24,PC25,PC26 to 4.7U_0805, PC75,PC76 to unmount,	For PCB noise issue
	2010/03/18	40	Change PR247 to 47K ohm	Modify GFX load line
	2010/04/02	40	Change PR98 to 9.76K ohm	circuit modify(cut in AON6718L)

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>		
Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title		
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