5.1 MC68B09E/MBL68B09E/HD68B09E (IC1)

The heart of any computer system is the Central Processing Unit, CPU. In the Color Computer 3, as well as in most modern microprocessors, the CPU is a single Large Scale Integration Circuit (LSI). The CPU gathers instructions and data from memory, interprets and executes the instructions, and stores the results of the data operations into memory. Additionally, the CPU stores data to and retrieves data from various input/output (I/O) devices.

The 68B09E microprocessor is perhaps the most powerful 8-bit microprocessor available today. There are several ways to determine the "size" of a microprocessor (whether it is 8-bit, 16-bit, 32-bit, or whatever). One way involves the number of data interconnecting lines the processor possesses. Another is the size of the internal registers and the size of the mathematical and logical operations supported by the processor. Although the 68B09E has an 8-bit data bus, internally it contains four 16-bit registers and two additional 8-bit registers which may be linked together to form another 16-bit register. The 68B09E also supports some 16-bit mathematical and logical operations. Therefore, although it is technically an 8-bit processor, it has some of the power of the 16-bit machines.

Figure 5-1 is a "programming model" of the 68B09E CPU. Additional information may be obtained from the 68B09E data sheet.

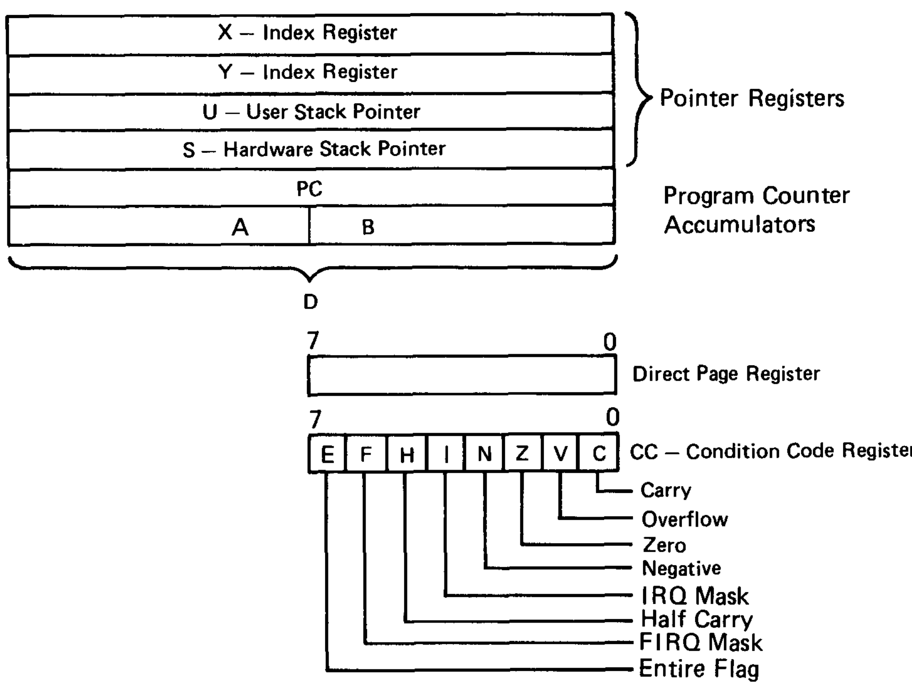


Figure 5-1. 68B09E Programming Model

Figure 5-2 shows the pinouts of IC1, the 68B09E CPU. Note that there are sixteen address lines (A0 through A15). These address lines are output from the CPU and are used to select one of 65,536 different memory locations. The memory and I/O devices must be wired to accept the correct combination of highs and lows on the address lines. The order of the devices and how they respond to the different lines are called the memory map.

The CPU has eight data lines (D0 -D7). These data lines are bidirectional and are used by the processor to both route data to and retrieve data from memory or I/O devices through Bus Transceiver 74LS 245 (IC3).

The remaining lines on the CPU are used for control functions, both input control and output control. Of course, the Vcc pin is the power input line to the CPU and the GND line is the return reference for both power and signal. The E and Q lines are the clock inputs to the CPU. These clock signals must be present for the CPU to function. In the Color Computer 3, these signals are provided by the advanced color video chip (IC6) and are 50% duty cycle clocks at a frequency of 0.89 MHz or 1.78 MHz. As shown in Figure 5-3, Q is a quadrature clock signal which leads E by 90 degrees.

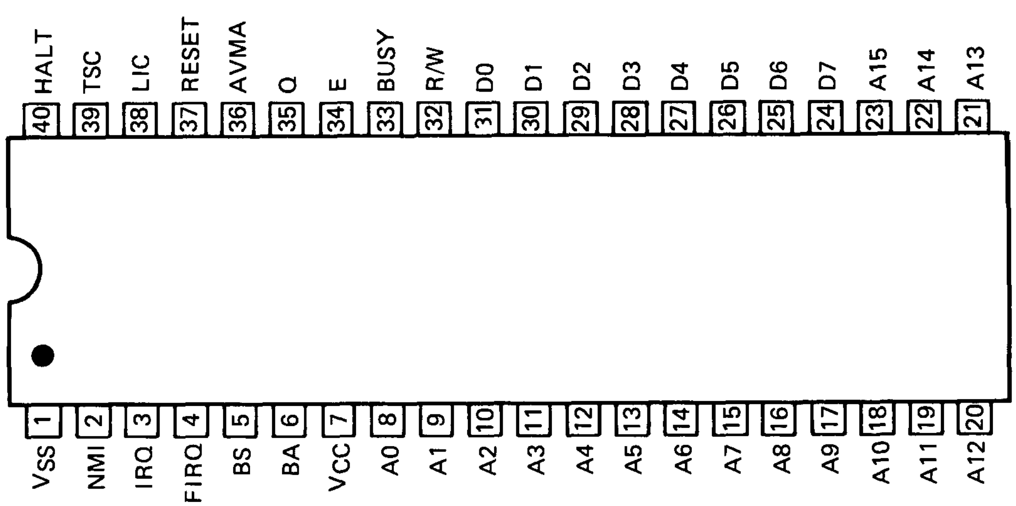


Figure 5-2. MC68B09E Pin Assignments

The CPU contains a number of inputs which serve to initiate specific sequences of events. The ones used by the Color Computer 3 are:

RESET* - Used on power up and to reinitialize the CPU.

HALT* - Stops the program flow after the completion of current instruction. Execution will continue after HALT is removed.

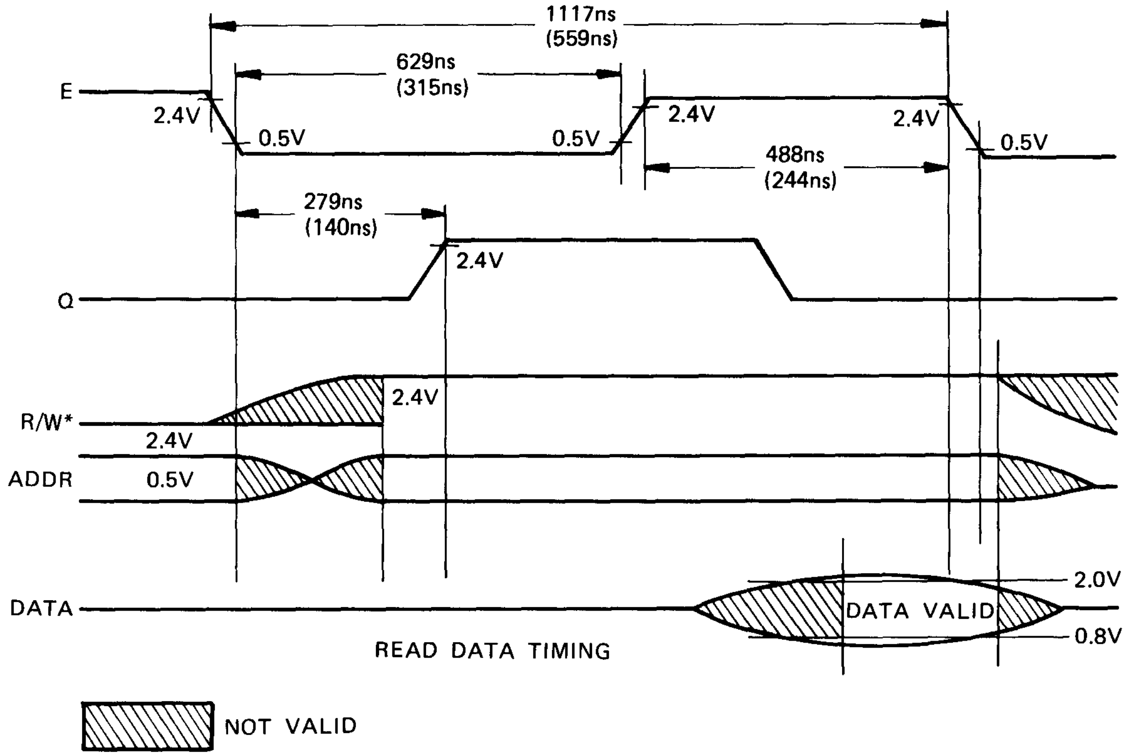
NMI* - Non-Maskable Interrupt always causes the CPU to "interrupt" its normal program flow and execute a special "interrupt handler" routine.

IRQ* - Interrupt Request. Similar to NMI but may be masked (defeated) by setting the I bit in the CC register.

FIRQ* - Fast Interrupt Request. Similar to IRQ, but masked by the F bit. It is faster because it doesn't preserve all registers (as do the other interrupts).

Upon receipt of the RESET signal, or any of the interrupts (if enabled), the CPU will get the appropriate subroutine address from the Vector Table (see the memory map in Section I, System Description). For the interrupt routines, registers are preserved on the Stack to be restored upon receipt of the RTI (Return-from-Interrupt) instruction.

Other control lines used in the Color Computer 3 are TSC (Three-State Control) and the R/W* (Read/Write*) line. The TSC line is an input intended for use in multiprocessor or DMA environment and will cause the address and data lines to go into a three-state condition if high. Since the Color Computer 3 does not require multiprocessing, this line is permanently grounded. The R/W* line is an output used by the CPU to inform the external memory and devices whether the data transfer is from the CPU (a write) or to the CPU (a read). Standard 68B09E Read/Write timing is shown in Figure 5-3. However, in the Color Computer 3, this timing is modified by the ACVC chip so that the addresses are available to the memory only during the active E time. This presents no problem as long as the memory is sufficiently fast.



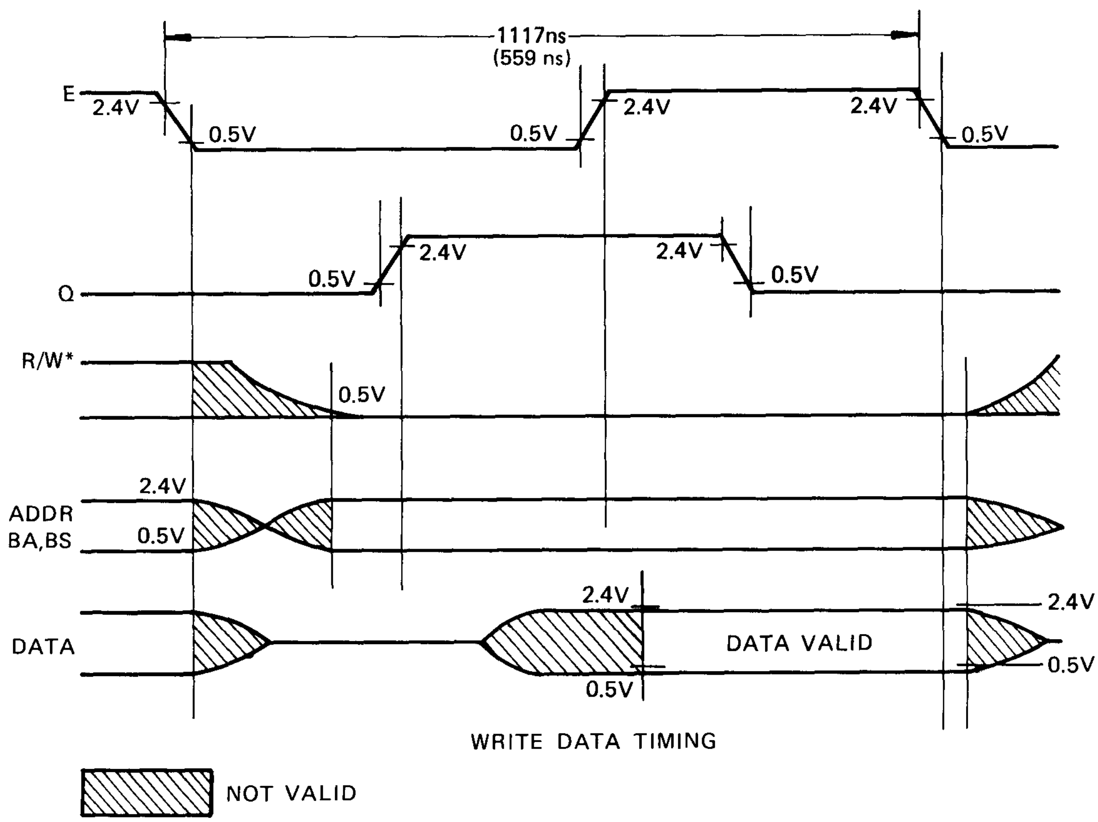


Figure 5-3. MC68B09E Read/Write Timing at 0.89 MHz

* Values within parentheses are for 1.78 MHz

5.2 Memory (RAM)

The Color Computer 3 uses Dynamic Random Access Memories (DRAMs - IC16 through IC19). Each memory chip is capable of storing 262,144 bits (64K x 4), any one of which may be accessed at any given time. Since the CPU needs to access eight data bits at a time, two DRAMs are used. Therefore, the memory array is said to be 64K x 8. The dual Write Enable signals (WE0*, WE1*) to the DRAM control 2 banks of 64K x 8 memory (total of 128K x 8). The DRAMs in the Color Computer 3 operate off of a single +5 volt supply.

In order to address a 64K location in each chip, 16 address lines are required. However, since the DRAM package has only 18 pins, the addresses are multiplexed into two groups of 8 and 8, called row address and column address. (See Figure 5-4.) The row address is presented first, and the DRAM is informed that this is the row address by the presence of RAS* (row address strobe) and the absence of CAS* (column address strobe). After the DRAM has latched the least significant eight addresses (the row addresses), the column addresses are presented, along with CAS*. If the present cycle is a read cycle, WE* (Write Enable) is held high, and the data is retrieved from the appropriate cell and presented at the output pin some time later. The actual time depends on the access time of the DRAM. During a write cycle, the data and WE* signal are active prior to CAS* and are latched in at CAS* time. Figure 5-5 shows the read and write timing cycles for DRAM.

Dynamic memory is called dynamic because it requires refreshing at periodic intervals in order to remember. Refresh is accomplished by providing the DRAMs with RAS* signal and an address count. The address count must toggle through all 256 row address possibilities in 4 milliseconds or less. (If you don't remind the DRAM of what it knew at least once every 4 milliseconds, it will forget.)

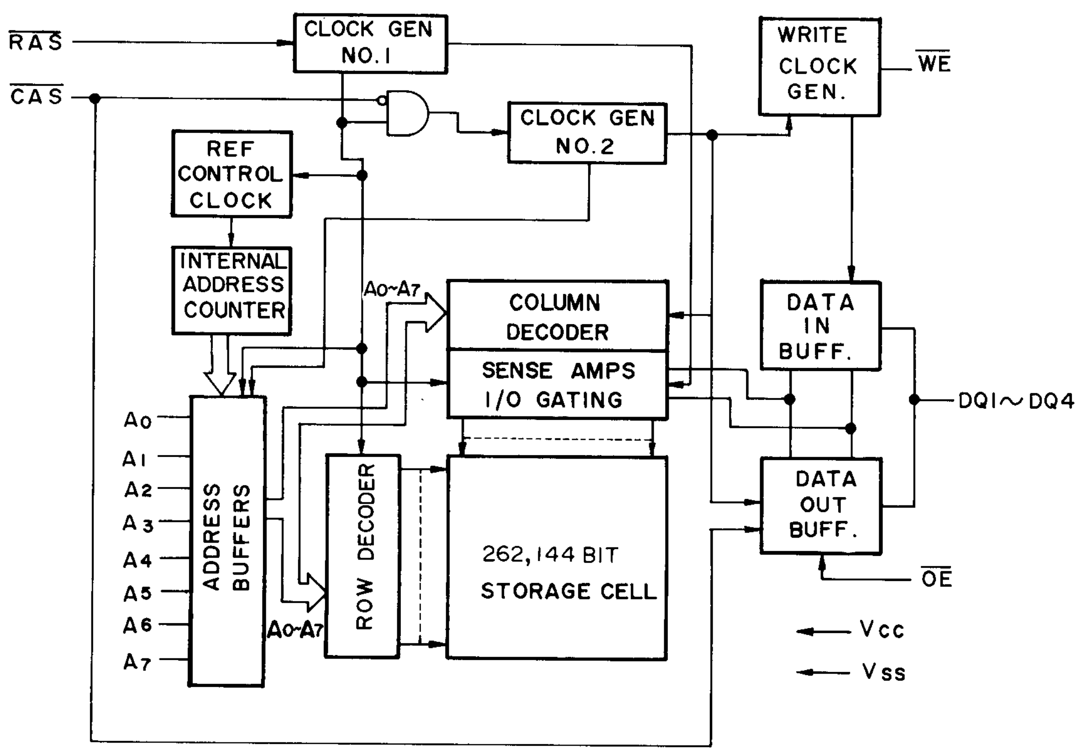
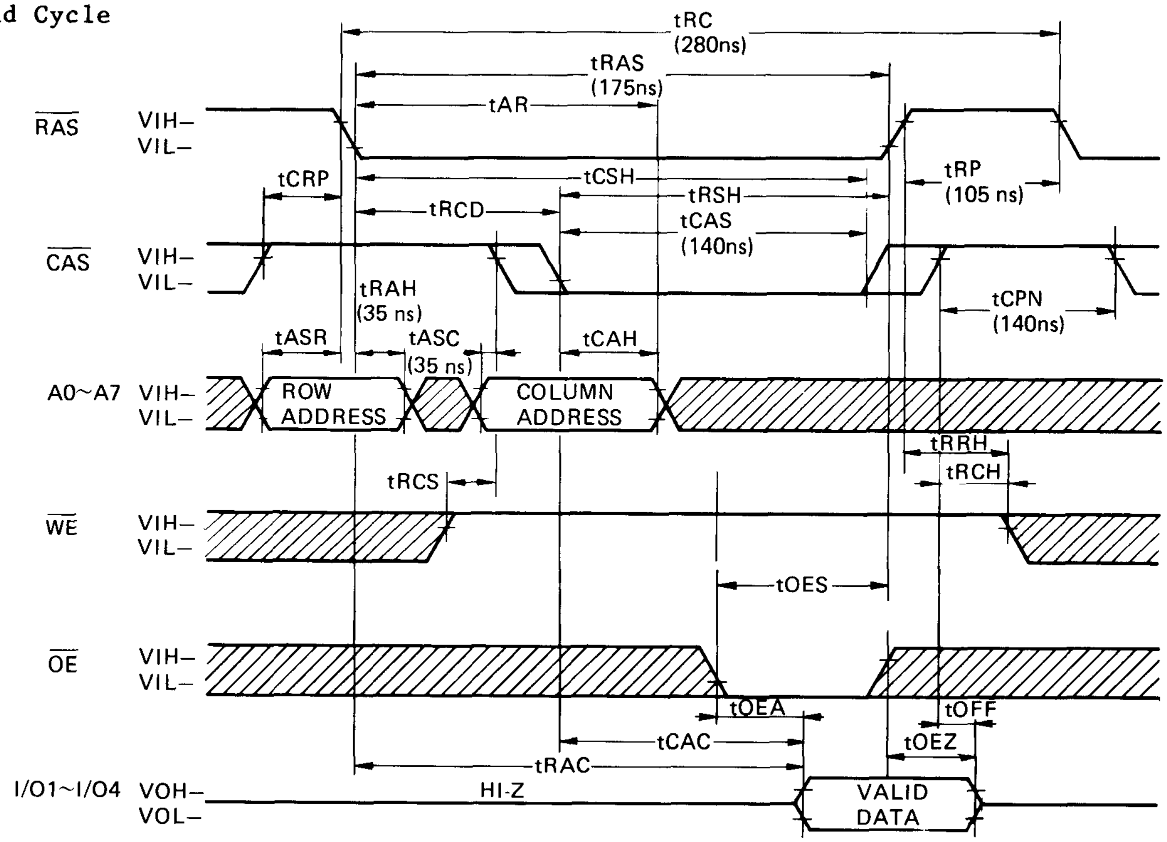


Figure 5-4. DRAM Block Diagram

Read Cycle



Write Cycle

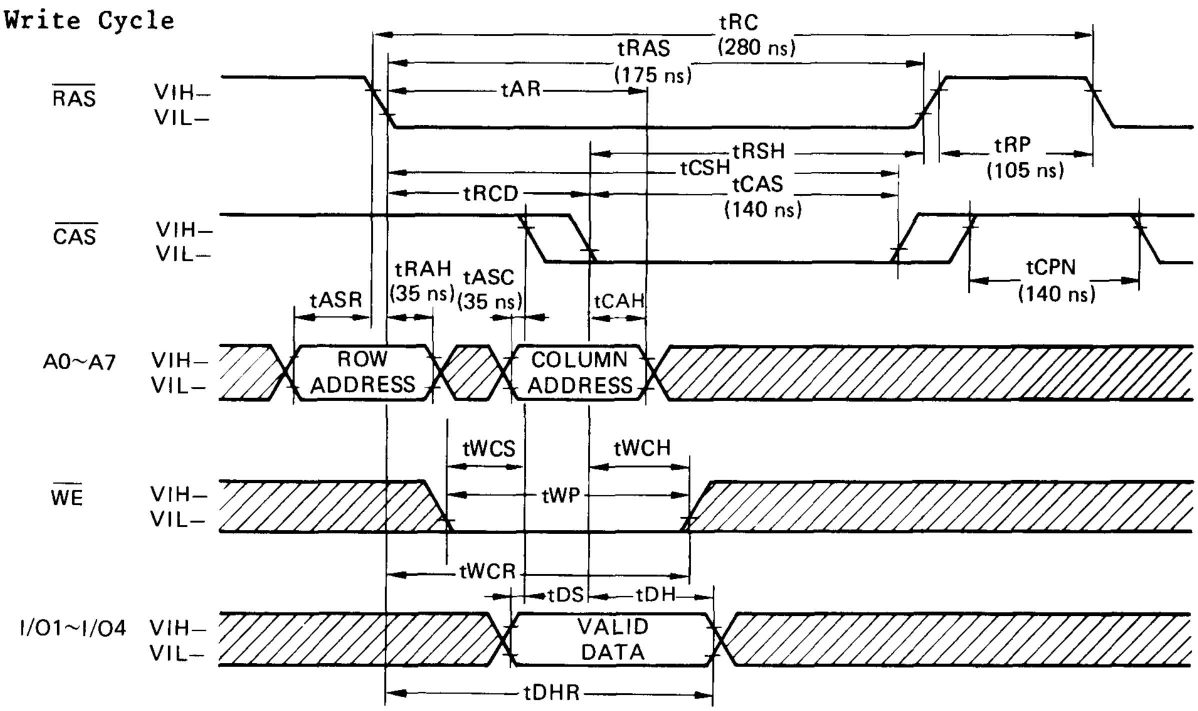


Fig 5-5. DRAM Timing

5.3 TCC1014 (VC2645QC)

1) System Timing, Address Multiplex, Device Select, MMU

By now, it should be apparent that controlling DRAMs is a fairly complex task. In the Color Computer 3, it is done by the TCC1014 (VC2645QC: ACVC). In addition to address multiplexing, RAS* and CAS* generation, WE0*, WE1* timing control, and refresh generation, the ACVC performs other tasks. It contains the Master Oscillator, the frequency of which is controlled by a 28.63636 MHz (PAL: 28.4750 MHz) crystal (X1). The Master Oscillator is divided by eight to give a 3.579545 MHz color reference signal to the Video Display Generator LOGIC and Composite Video Signal (NTSC version only). This reference signal is then divided by 4 (or 2) again to provide the 0.89 MHz (1.78 MHz) E and Q clock signals for the processor.
In the PAL version, the Master Oscillator frequency is slightly shifted down than in the NTSC version for fitting with the PAL encoder circuit.

The ACVC (IC6) also controls access to the memory, granting access to the processor during the high time of E (CPU portion) and access to the VDG LOGIC during the low time of E (Video portion). During each access, whether by the CPU or the Video, the ACVC must provide appropriately synchronized RAS* and CAS* signals, as well as the corresponding address signals, to the DRAMs. Note that the DRAM access time must be twice as fast as that required by the CPU alone in order to be able to respond to VDG accesses.

In order for the ACVC chip to provide the appropriate addresses to the DRAMs, all 16 CPU address lines are input to the ACVC. It then multiplexes these into low order and high order addresses (Z0 through Z8, refer to MMU) which are sent to the DRAMs along with RAS* and CAS*.

Another function of this section is to provide address decoding and device selection for the computer. Figure 5-6 shows how the S0, S1, and S2 lines are connected to IC9, a 74LS138, in order to provide appropriate signals to enable ROM selection, PIA selection, and various cartridge selection signals. Due to the nature of the ROMs and in order to prevent data bus contention, the ROMs are enabled only during the E portion of a read cycle.

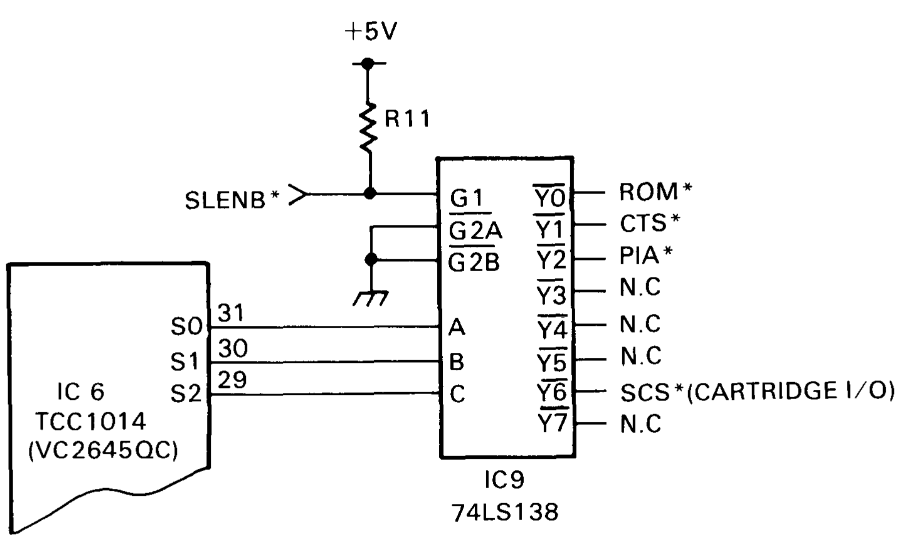


Fig 5-6. Color Computer 3 Address Decoding

As it is clear from the Memory Map, the memory area of the CoCo3 is from &00000 through &7FFFF (512K bytes). The Memory Management Unit (MMU) inside of the TCC1014, pins FFA0 through FFAF, selects A13 - A18 (actually A16 - A18). Figure 5-7 shows the Block Diagram of the MMU.

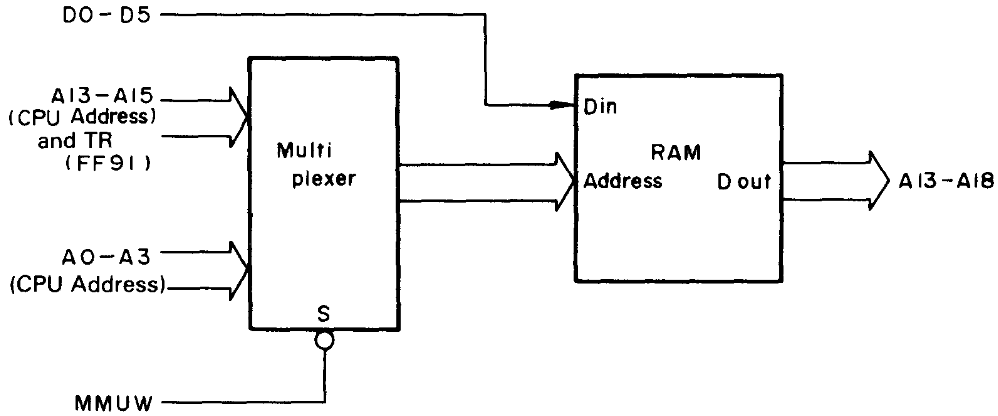


Figure 5-7. MMU Block Diagram

2) Video Generation Circuit

For NTSC Version

In Color Computer 2, the composite video signal is created in Modulator IC (MC1372), while the intensity control signal (Y) and the color information signals ØA and ØB are generated in VDG (MC6847). In Color Computer 3, all of these signals are generated in ACVC (IC6), and output from pin 65 as the composite video signal. This signal is provided to the video output terminal through buffer (Q2, Q3) and to the modulator.

For PAL Version

The ACVC is designed to output both composite video signal and analog RGB signal. Since composite video signal is specially designed for NTSC system, the PAL Encoder circuit is used to encode the RGB signal to the PAL signal. For this purpose, the VSYNC and HSYNC output from pins 55 and 56 of IC6 are provided to the PAL Encoder as a composite sync signal through the inverter IC15 and mixing circuit (Q11, D15 - D17). The output of PAL Encoder, that is the PAL system composite video signal, is then provided to the RF Modulator via buffer Q3, and to the video output terminal via Q3 and Q2.

ACVC also contains analog RGB output and a total of 64 color selections. For the video generation circuit where the control register is designated via software, please refer to the Memory Map in section 1.3.

3) Interrupt IN/OUT

In CoCo2, the three interrupt sources CART*, HSYNC* and VSYNC requested an interrupt to the CPU from PIA as IRQ* and FIRQ*. In CoCo3, in addition to the above mentioned interrupt sources, an interrupt to the CPU can be requested as IRQ* or FIRQ* from serial I/O, keyboard, and 12-Bit interval timer. It has higher selectivity. Refer to FF90 and FF92 through FF95 in the Memory Map.

5.4 PAL ENCODER (PAL Version Only)

PAL version uses IC101, IC102 and IC103 to encode the RGB signals to the PAL signal. The majority of the work is performed by IC103, the RGB to PAL ENCODER chip. This chip is designed to generate a composite video signal from baseband red, blue, green and composite sync input from sync mixer Q11 and D15 - D17. The chip contains color subcarrier oscillator, voltage controlled 90 degrees phase shifter, two double-sideband suppressed carrier chroma modulators, RGB input matrix, and blanking level clamps.

In the PAL version, an extra voltage-controlled crystal oscillator is needed for the PAL color burst frequency of 4.433618 MHz. For this purpose, the internal oscillator circuit of the IC103 is used.
If the oscillator does not synchronize with the master oscillator, an apparent motion will exist whenever a color transition occurs.

This synchronization problem is solved by slightly shifting of the master oscillator frequency and the addition of a phase-locked-loop circuit. The master crystal oscillator frequency of the PAL version is 28.475 MHz. This allows the two oscillator to be divided down to the horizontal frequency of 15.611 kHz and phase-locked at this frequency.

IC101 is a programmable divider and operates in a divisor of 71. The output from the divider is connected to the programmable divider part of IC102 where a divisor of 4 is used to complete the count-down to 15.611 kHz. IC102 also contains a phase comparator part, and it compares this divided 15.611 kHz with the HSYNC signal which is counted down to 15.611 kHz from the master oscillator in IC6. The phase comparator then generates a control voltage in proportion to the phase and frequency difference between these 2 signals of 15.611 kHz and output it at pin 13.

This control voltage is passed through a simple R-C low pass filter and used to control a varactor diode D101. The capacitance of the varactor is changed to tune the 4.433618 MHz oscillator by varying the control voltage. This tuning allows the two oscillators to be synchronized at any time except during reset or power-on.

5.5 PIAs (IC4 and IC5)

The Color Computer 3 uses two Peripheral Interface Adapters (PIAs). These devices provide a universal interface to the 68B09E CPU. They support all of the I/O functions in the Color Computer 3.

The functional configuration of the PIA is programmed by the CPU during the reset routine. Each of the peripheral data lines may be programmed to act as an input or output, and each of four control/interrupt lines may be programmed for one of several control modes. Figure 5-8 shows a block diagram of a PIA.

A PIA consists of two 8-bit data registers and 4 control/interrupt lines. The two 8-bit data registers are controlled by two data direction registers. These direction control registers are set up by the reset routine and normally will not be changed.

The four control/interrupt lines are controlled by the two control registers. The control registers also handle device selection within the PIA. Two of the four lines function only as interrupt inputs, and the other two lines may be used as interrupt inputs or data outputs.

PIA IC5 is used mainly for the keyboard. Data register B (pins 10-17) is programmed as an output and is used to strobe the keyboard columns. The first seven lines of data register A (pins 2-8) are programmed as inputs and are used to read the keyboard rows. Pins 2 through 5 are also used as fire button inputs for the joysticks.

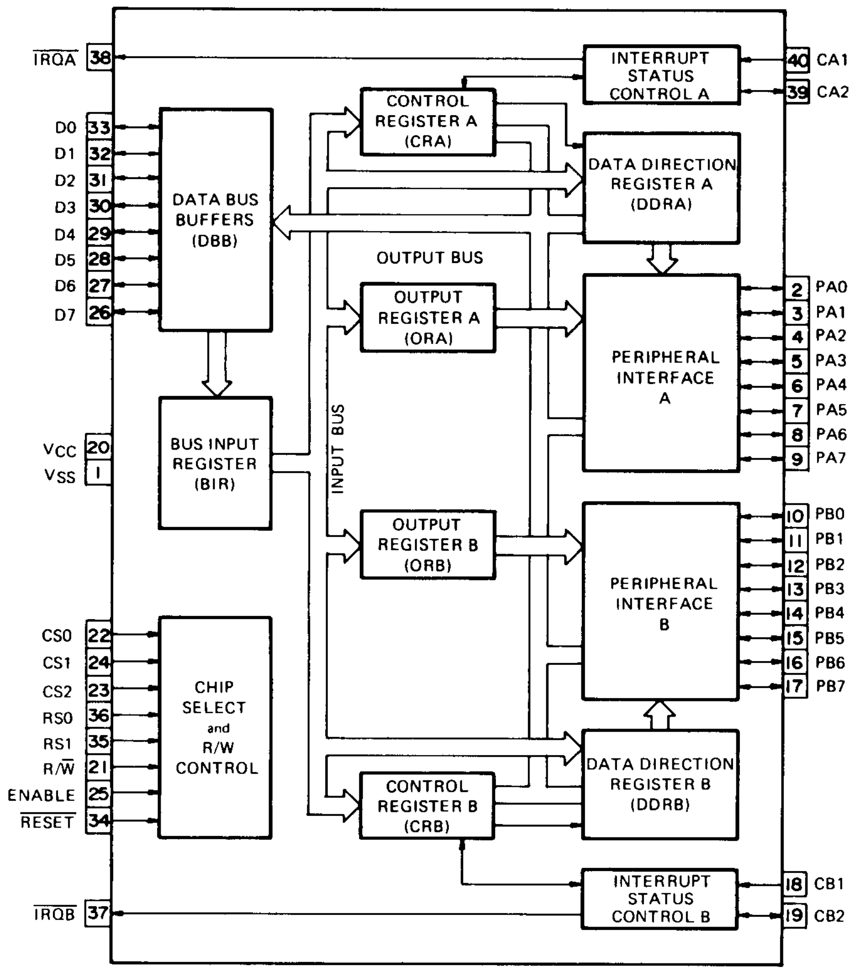


Figure 5-8. PIA Block Diagram

5.6 Keyboard Interface (IC5)

PIA IC5 is the only active component in the keyboard interface circuit. The B side of this PIA is configured as outputs and connects to the column lines of the keyboard matrix. The A side of IC5 is configured as inputs and connects to the row lines of the keyboard matrix. PIA IC5 is a select device. The use of PIA compensates for a possible increase in key contact resistance due to prolonged use and therefore should result in a highly reliable keyboard interface.

To read the keyboard, only one column is enabled by writing a zero in the bit that corresponds to that column and by writing ones in all the other bits. If a key is being pressed in that column, one of the input lines will be a zero, and the key location will correspond to the bit that is low. By scanning each column in the keyboard, all of the keys may be checked. Figure 5-9 shows the keyboard matrix.

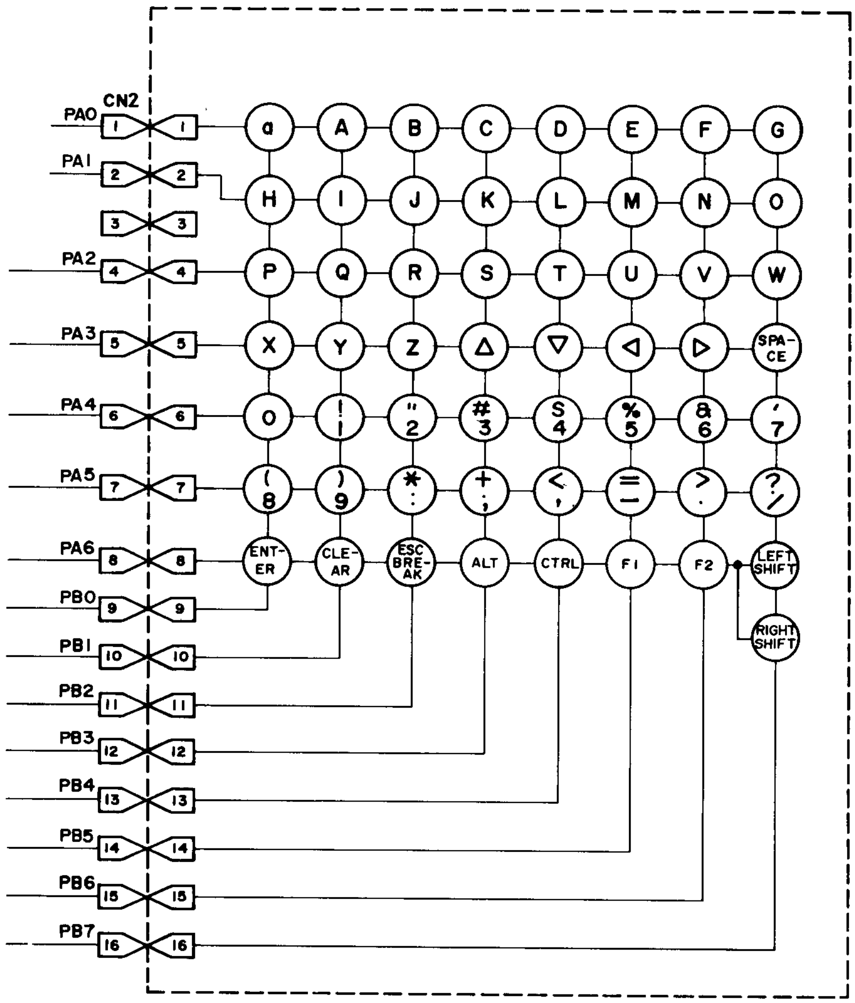


Figure 5-9. Color Computer 3 Keyboard Array

The other pins of PIA IC5 serve various functions. The most significant bit of data register A (pin 9) is programmed as an input for the joystick interface. CA2 and CB2 (pins 19 and 39) are used as outputs. These two lines select one of four joystick or sound inputs. The last two pins of PIA IC5, CA1 (pin 40) and CB1 (pin 18), are used as interrupt inputs. They are both tied to SYNC clock outputs from the ACVC (IC6). If enabled, CA1 provides an interrupt after each SYNC line. CB1, if enabled, provides an interrupt after each screen of data (NTSC: 60Hz/PAL: 50Hz).

PIA IC4 is used for several different functions. Pins 4-9 of data register A are used for the 6-bit digital to analog converter. Pin 3 of register A is the RS232-C output signal, which is used to drive the printer and other RS-232C-type devices. Pin 2 of register A is the input for data from the cassette. Pin 13 of IC4 is the sense input for the RGB monitor (CM-8). Pin 12 of register B is an input for the memory size. Pin 11 of register B is the single-bit sound output. Pin 10 is the RS-232C signal input pin.

The control and interrupt pins of PIA IC4 also serve various functions. CA1 (pin 40) is the input for the signal CD (a status interrupt input for the RS-232C interface). CA2 is an output used to control the cassette motor. CB1 is the cartridge interrupt input. Whenever a cartridge is inserted into the computer, this input will interrupt BASIC and jump to the program in the cartridge. Finally, CB2 is used as an output to enable sound from the DAC chip (IC7).

5.7 ROM (IC2)

ROM stands for Read Only Memory, which is a type of memory that retains its data when power is removed from it. When power is applied to the CPU, it immediately attempts to fetch a vector and begin executing instructions. If there were no ROM, the CPU would read random floating states on the data bus, attempt to execute this, and promptly go haywire.

The Color Computer 3 contains 256K (32K BYTE) ROM which contains Extended Color BASIC (Vers.2.0). This ROM is programmed to provide the user with certain BASIC commands and functions.

5.8 DAC Circuitry (IC7)

Two special analog integrated circuits are used in the Color Computer 3 to implement a multitude of analog functions, including power supply regulation, cassette operation, the RS-232C serial interface, the joystick interface, and sound production/selection. The DAC chip (IC7) is one of the custom linear integrated circuits used in the Color Computer 3. As its name implies, it contains a Digital to Analog Converter. This chip also contains a sound multiplexer and the circuitry necessary to interface the joystick controllers to the microprocessor. Figure 5-10 shows a block diagram of the DAC chip.

The DAC performs most of the functions of this chip. Six bits of control are used by the DAC to specify a discrete internal analog level. This level is one of the sound inputs to the sound multiplexer. It is also used as a reference for a comparator, the other input of which is one of the four joystick inputs. Finally, the DAC signal is attenuated and used as the cassette recording signal for data storage.

There are two select inputs to the DAC chip: Sel A and Sel B. These determine which of the joystick inputs is to be compared against the DAC, as well as which sound source is coupled to the sound output pin according to the table on the next page.

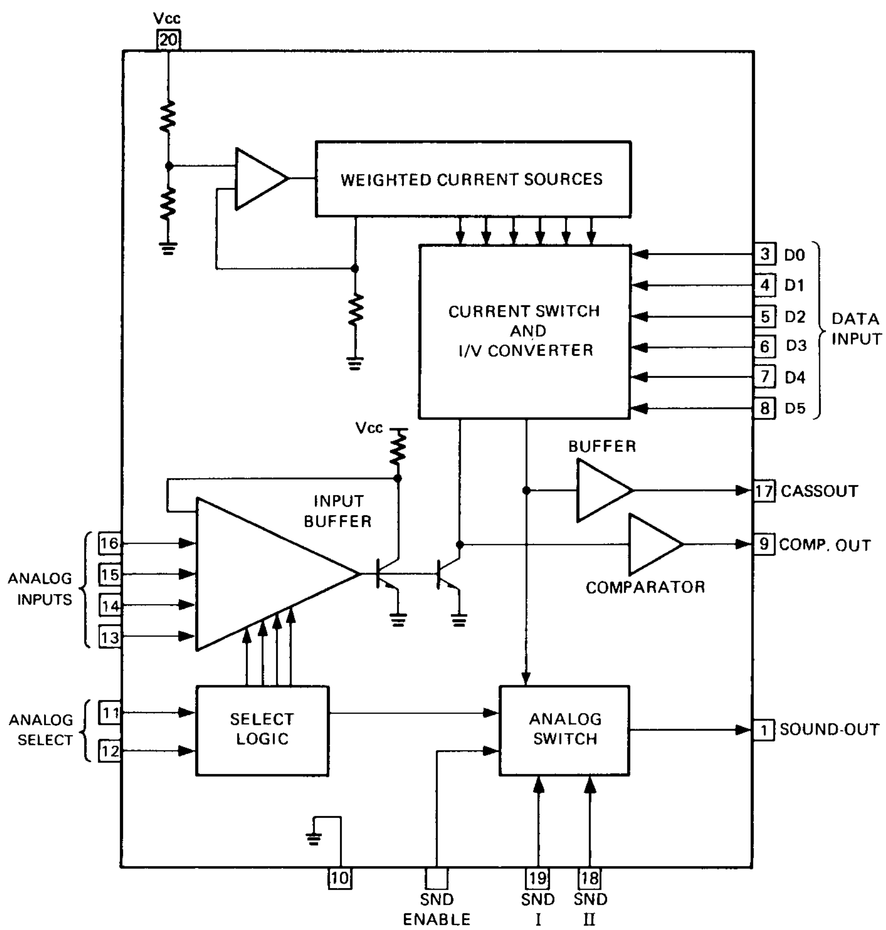


Figure 5-10. DAC Block Diagram (IC7)

Sel B	Sel A	Joystick Input	Sound Source
0	0	Joy 0	DAC
0	1	Joy 1	Cassette
1	0	Joy 2	Cartridge
1	1	Joy 3	(no sound)

The Digital to Analog Converter employs a 64-collector transistor as a current source which gives good linearity over the entire voltage range. In order to determine the position of the joystick, the microprocessor uses a technique called "Successive Approximation". The microprocessor first selects the desired joystick input by means of the select pins (which are connected to PIA IC5).

The sound multiplexing section is very simple. According to the above table, different sound sources are selected by the Sel A and Sel B inputs, and the selected input is routed to the sound output. If the DAC is used as a sound source, the microprocessor simply feeds a succession of values to the six bits of the DAC in order to produce the desired waveshape. The output of the DAC is then buffered and attenuated to provide approximately 3.9 volts p-p, which is the level required by the modulator to produce maximum volume. If the cassette is the selected input, then sound from the cassette recorder is routed to the sound output. This level follows the input level up to 3.9 volts p-p, at which point it clips the input waveform. Therefore, the volume control on the cassette should not be set higher than the level which provides 3.9 volts p-p to the DAC chip. Similarly, the cartridge may supply the sound source (from AC coupled) since the SND IN (2) input to the DAC chip biases the input at the midpoint of the allowable voltage swing, which is 3.9 volts p-p. Any greater signal amplitude will result in clipping (distortion) of the sound waveform.

In addition to the Select inputs, the sound must be enabled by bringing SNDEN to a high level. This input is controlled by PIA IC4. If this pin is at a low level, all sound (except single-bit sound) is disabled.

The final function of the DAC chip is to provide the output signal for recording of cassette data. This is, quite simply, a buffered output of the DAC which is attenuated to produce approximately 1 volt p-p into a 2-kohm load. Therefore, it is up to the microprocessor to produce the necessary FSK signals through the DAC and the proper software.

5.9 SALT Circuitry

The SALT chip IC8 (Supply and Level Translator) is responsible for supply regulation, RS-232C interface level translation, cassette read operations, and driving the cassette relay, as is shown in the block diagram in Figure 5-11.

Figure 5-12 shows the complete power supply circuit. AC voltage is brought into the primary of transformer T1. The secondary of the power transformer provides 16.2 VAC (18.52 VAC for PAL version), center-tapped, at AC 2.2 amps (AC 1.0 amps for PAL version) to the Color Computer 3 circuit board. If switch SW1 is closed, this AC voltage is applied to the cathodes of D3 and D4, and to the anodes of D1 and D2. D3 and D4 form a full-wave, center- tapped rectifier with a negative output. This is filtered by electrolytic capacitor C31. This negative voltage is then applied to pin 15 of the SALT chip, where it is internally regulated to -5 VDC and used for the RS-232C output drivers. The negative voltage is not used anywhere else in the computer.

D1 and D2 form a full-wave, center-tapped rectifier with a positive output which is filtered by electrolytic capacitor C29. This positive voltage is applied to the collector of pass transistor Q1 and is used to power the SALT chip at pin 16. The SALT chip internally regulates the positive voltage to +5 VDC and provides the base drive current for Q1. The current for the computer is drawn from the emitter of Q1 through resistor R19. The voltage at this point is monitored by pin 3 of the SALT chip and the base drive adjusted to keep the voltage at a steady +5 VDC ±5%.

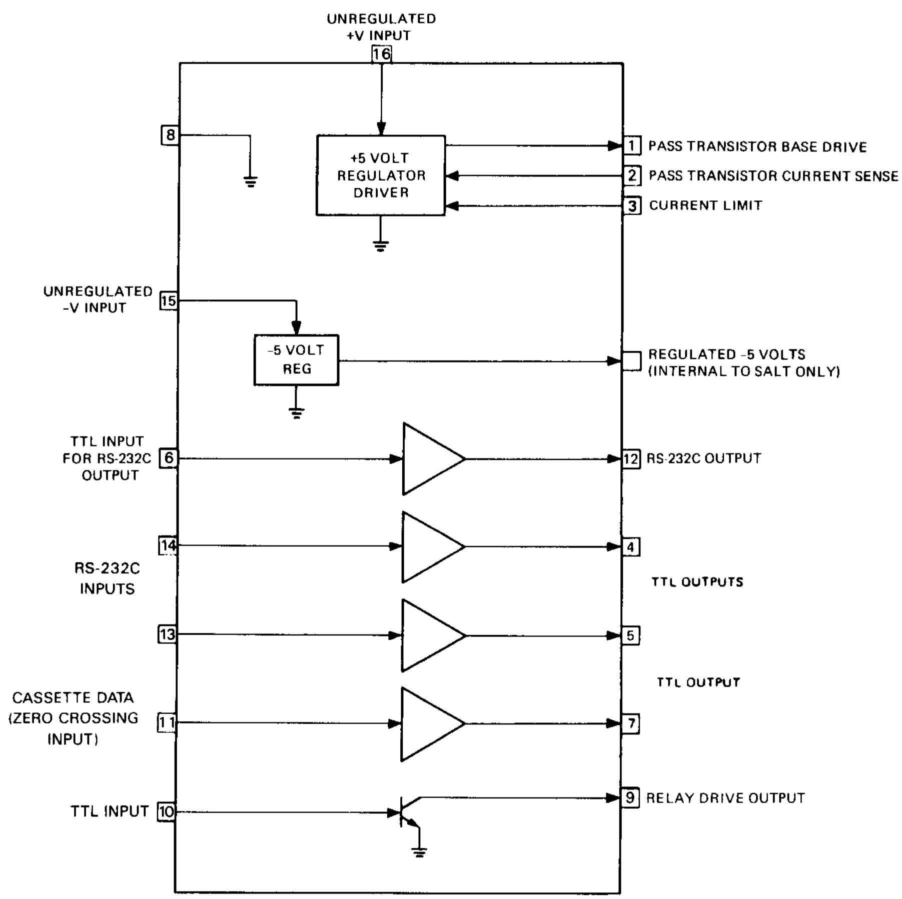


Figure 5-11. SALT Block Diagram (IC8)

The SALT chip senses, at pin 2, the amount of current drawn from the supply through R19. If excessive current is drawn, as in the case of a short or component failure, the SALT will "fold back" the voltage output of the supply by reducing the base drive current, thus protecting the supply.

Inductors FB1 and FB2, as well as capacitors C32 through C36, serve to decouple and prevent any digital "noise" which might be present on the DC supply from entering the AC line.

There are two types of level translators contained in the SALT chip for use with the RS-232C interface. The output level converter takes as its input a standard TTL signal from PIA IC4, inverts it, and uses it to drive the output to approximately +5 VDC for a space and -5 VDC for a mark. This output is coupled through a 270-ohm resistor, R15 to the output connector. R15 serves to limit the amount of current drawn from this output and prevents damage to the SALT chip if the output (at the connector) is inadvertently shorted to an external voltage (such as $\pm$12 VDC, which may be present on some RS-232C connectors).

The input level converters have the task of converting incoming RS-232C voltage levels to standard TTL signals. These voltages are defined as follows: a "mark" is a negative voltage between -3 and -25 VDC; a "space" is a positive voltage between +3 and +25 VDC. To simplify the task for the SALT chip, the circuit shown in Figure 5-13 is employed. The incoming signals are compared to a reference of 2.0 VDC. If less than that, they are considered to be a mark. If greater than that, they are considered to be a space. The space or mark is then output from the SALT chip at an LS TTL-compatible level and is coupled into PIA IC4.

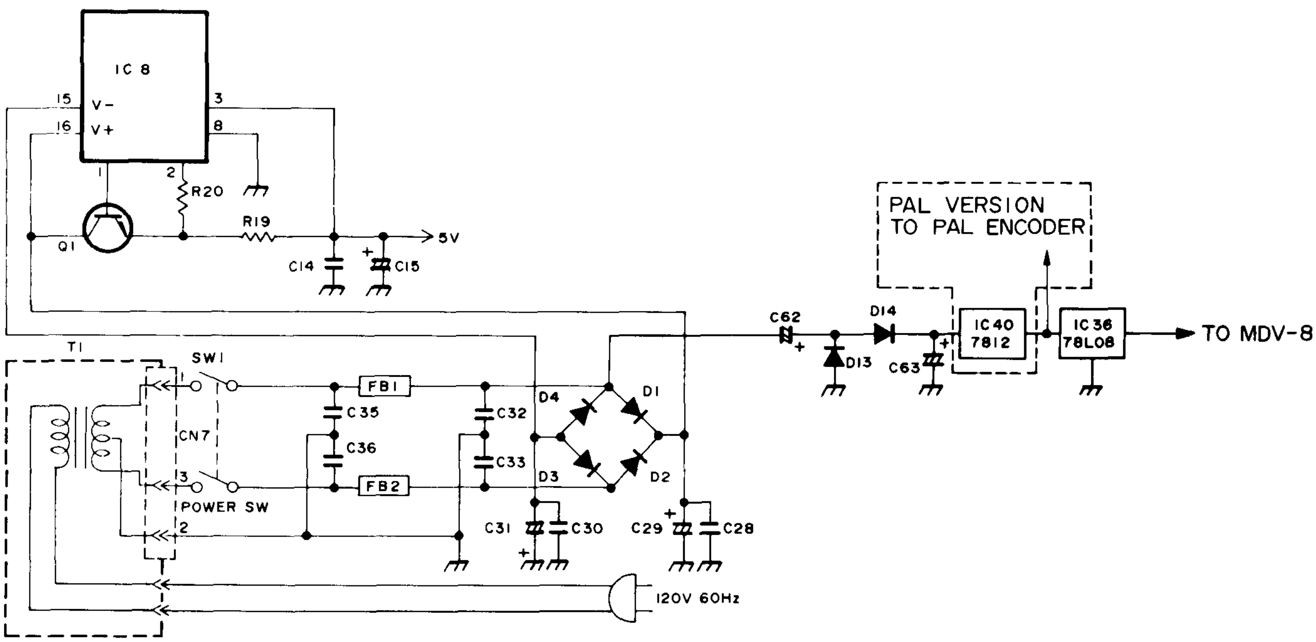


Figure 5-12. Color Computer 3 Power Supply

The cassette-loading circuitry, internal to the SALT chip, is composed of a zero-crossing detector. Figure 5-13 shows the input from the cassette being loaded by a 220-ohm resistor, R14, then coupled into the SALT chip through a 510-ohm resistor, R18. R14 serves to load the capacitively-coupled output characteristic of most portable cassette recorders, and R18 limits the current of the incoming signal to prevent damage to the SALT chip if an excessively large peak-to-peak voltage is fed into the cassette input. Although Tandy's computer cassette recorders do not produce more than 6 volts p-p, the circuitry is protected from voltages as high as 18 volts p-p. The zero-crossing detector internal to the SALT changes state each time the incoming signal passes through zero volt. There is a small amount of hysteresis built in which provides noise immunity and prevents false triggering of the zero-crossing detector.

The output of the zero-crossing detector is an LS TTL-compatible level and is coupled into PIA IC4.

The final function of the SALT chip is to drive the cassette relay. A TTL signal from PIA IC4 enters pin 10 of the SALT chip where it is connected to the base of an internal Darlington transistor, the emitter of which is grounded. The collector exits the SALT chip at pin 9 and is connected to one end of the cassette relay. The other end of the relay connects to +5 VDC. When the incoming signal goes high, the transistor becomes saturated and connects its end of the cassette relay to ground, causing the relay to energize. When the incoming signal is low, the transistor is cut off. There is no ground return for the +5 volts at the other end of the relay, so it is de-energized. Diode D5 protects the transistor in the SALT from the surge current caused by the coil of the relay (when the relay is de-energized).

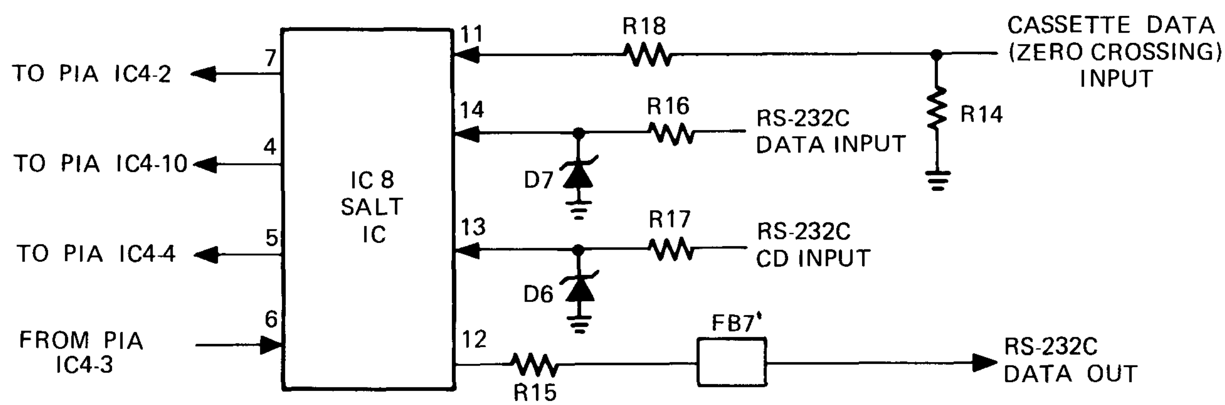


Figure 5-13. I/O Circuitry

5.10 Cassette Tape Format Information

The standard Color Computer 3 tape is composed of the following items:
1. A leader consisting of 128 bytes of 55H
2. A Namefile block
3. A blank section of tape equal to approximately 0.5 seconds in length to allow BASIC time to evaluate the Namefile
4. A second leader of 128 bytes of 55H
5. One or more Data blocks
6. An End of File block

The block format for Data blocks, Namefile blocks or an End of File block is as follows:
1. One leader byte - 55H
2. One sync byte - 3CH
3. One block type byte:
   - 01H = Data block
   - FFH = End of File block
   - 00H - Namefile block
4. One block length byte - 00H to FFH.
5. Data - 0 to 255 bytes
6. One checksum byte - the sum of all the data bytes plus block type and block length bytes
7. One trailer byte - 55H

The End of File block is a standard block with a length of 0.

The Namefile block is standard block with a length of 15 bytes (0FH). The 15 bytes of data provide information to BASIC and are employed as described below:
1. Eight bytes for the program name
2. One file type byte:
   - 00H = BASIC Program
   - 01H = Data File
   - 02H = Machine Code Program
3. One ASCII flag byte - 00H = Binary, FFH = ASCII
4. One Gap flag byte - 01H - continuous, FFH = gaps
5. Two bytes for the start address of a machine language program
6. Two bytes for the load address of a machine language program

5.11 RS-232C Connector (JK3)

The RS-232C interface utilizes a 4-pin DIN connector. This interface allows the computer to have serial communications with printers, modems, other computers or any device capable of interfacing with RS-232C signals. The four signals used by the interface are:

CD	- a status line
RS-232C IN	- serial data input
GROUND	- zero voltage reference
RS-232C OUT	- serial data out

The pinout for the DIN connector is shown in Figure 5-14.

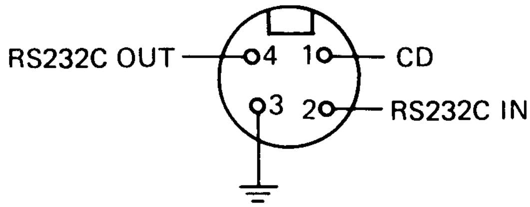


Figure 5-14. RS-232C Connector Pinout

The RS-232C interface hardware in the Color Computer 3 is capable of communication with any device which will operate with the minimum three signal interface. It is also possible that devices which use a larger set of RS-232C signals may be used with the Color Computer 3. This would be accomplished by connecting unused device inputs to the correct high or low level.

In software, the only RS-232C device supported by the BASIC ROM is a serial printer. For use with the printer, the pin assignment of the connector differs slightly from the above description:

1. No Connection
2. Connected to the BUSY output (or status line) of the printer
3. Ground
4. Connected to the Serial Data Input of the printer

If your printer does not provide a status line, then pin 2 must be connected to a positive voltage of +3 to +12 volts. This tells the computer that the printer is ready all of the time.

In order to operate, the software must make several assumptions about the printer. These assumptions are:

1. The printer operates at 600 baud.
2. The printer width is 132 columns.
3. The printer generates a BUSY when it is not ready.
4. The printer will automatically return the carriage at the end of the line. It will also do a line feed at this time.
5. The data format is one start bit, eight data bits, two stop bits, and no parity.

Some printers will require that these assumptions be modified. This may be accomplished by changing RAM variables or by a special driver routine.

A list of all the printer variables is given in Table 1. Also, Table 2 lists some alternate values for these variables.

5.12 Cartridge Connector (CN1)

A 40-pin cartridge connector provides the possibility of expanding the TANDY Color Computer 3 in almost any manner. All of the important CPU bus signals are tied to this connector. A complete list and brief description of these signals is provided in Table 3.

The most common usage of the cartridge connector is with the ROM cartridge. For cartridge detection, the Q clock is connected to the cartridge interrupt pin, which generates an interrupt anytime the cartridge is plugged in and forces the computer to jump to the program in ROM.

> **CAUTION**
>
> **DO NOT PLUG A CARTRIDGE IN WITH POWER APPLIED TO THE COLOR COMPUTER 3 AS SERIOUS DAMAGE TO THE UNIT AND/OR THE CARTRIDGE MAY RESULT.**

In addition to the expected data, address and R/W* lines, several control and special purpose signals are available on the cartridge connector. They are as follows:

HALT* - This active-low signal places the processor in a HALT state immediately following the execution of the current instruction. While in the HALTed state, the processor address and data lines are in the high impedance mode, making it possible for external devices to access RAM and ROM. The processor may be HALTed indefinitely without any loss of internal data.

NMI* - This is the non-maskable interrupt input to the CPU.

RESET* - This is the master system reset and power-up clear signal.

E, Q - These are the two clock signals for the MC68B09E CPU.

CART* - This is an interrupt input into PIA IC4. It is used to detect the presence of a cartridge.

CTS* - This is the Cartridge Select Signal. It is valid when the processor reads any location from C000 Hex to DFFF Hex, as long as the ACVC is in Map Type 0. Note that it is not active while writing to these locations.

SND - This signal is connected directly to the sound input of the DAC chip and allows cartridge-generated sound signals to be fed through the TV sound system. The signal should be AC coupled and should not exceed 3.9 volts p-p.

SCS* - This is a second chip-select signal from IC9. It is active for both reads from and writes to addresses, FF40H through FF5FH, regardless of the map type.

SLENB* - This signal disables the internal device selection. This allows decoded but unused sections of memory to be used by the cartridge hardware.

VARIABLE	HEXADECIMAL ADDRESS	DECIMAL ADDRESS	INITIAL VALUE HEXA-DECIMAL	DECIMAL
BAUD RATE MSB	0095	149	00	0
BAUD RATE LSB	0096	150	57	87
LINE DELAY MSB	0097	151	00	0
LINE DELAY LSB	0098	152	01	1
COMMA FIELD WIDTH	0099	153	10	16
LAST COMMA FIELD	009A	154	70	112
LINE PRINTER WIDTH	009B	155	84	132

Table 1. Line Printer Variables

BAUD RATE:	DECIMAL VALUE MSB	LSB	HEXADECIMAL VALUE MSB	LSB
120 BAUD	1	202	01	CA
300 BAUD	0	180	00	BE
600 BAUD	0	87	00	57
1200 BAUD	0	41	00	29
2400 BAUD	0	18	00	12
LINE DELAY:	DECIMAL VALUE MSB	LSB	HEXADECIMAL VALUE MSB	LSB
.288 SECONDS	64	0	40	00
.576 SECONDS	128	0	80	00
1.15 SECONDS	255	255	FF	FF
WIDTH:	DECIMAL VALUE		HEXADECIMAL VALUE	
16 CHARACTERS/LINE	16		10	
32 CHARACTERS/LINE	32		20	
64 CHARACTERS/LINE	64		40	
255 CHARACTERS/LINE	255		FF	

Table 2. Alternate Line Printer Variable Values

NOTE: LSB = Least Significant Byte
MSB = Most Significant Byte

PIN	SIGNAL NAME	DESCRIPTION
1	NC	
2	NC	
3	HALT*	Halt Input to the CPU
4	NMI*	Non-Maskable Interrupt to the CPU*
5	RESET*	Main Reset and Power-up Clear Signal to the System
6	E	Main CPU Clock (0.89 MHz/1.78MHz)
7	Q	Quadrative Clock Signal which Leads E
8	CART*	Interrupt Input for Cartridge Detection
9	+5V	+5 Volts (300 MA)
10	DO	CPU Data Bit 0
11	D1	CPU Data Bit 1
12	D2	CPU Data Bit 2
13	D3	CPU Data Bit 3
14	D4	CPU Data Bit 4
15	D5	CPU Data Bit 5
16	D6	CPU Data Bit 6
17	D7	CPU Data Bit 7
18	R/W*	CPU Read-Write Signal
19	AO	CPU Address Bit 0
20	A1	CPU Address Bit 1
21	A2	CPU Address Bit 2
22	A3	CPU Address Bit 3
23	A4	CPU Address Bit 4
24	A5	CPU Address Bit 5
25	A6	CPU Address Bit 6
26	A7	CPU Address Bit 7
27	A8	CPU Address Bit 8
28	A9	CPU Address Bit 9
29	A10	CPU Address Bit 10
30	A11	CPU Address Bit 11
31	A12	CPU Address Bit 12
32	CTS*	Cartridge Select Signal
33	GND	Signal Ground
34	GND	Signal Ground
35	SND	Sound Input
36	SCS*	Spare Select Signal
37	A13	CPU Address Bit 13
38	A14	CPU Address Bit 14
39	A15	CPU Address Bit 15
40	SLENB*	Input to Disable Device Selection

Table 3. Cartridge Connector Signals

5.13 Power Transformer

The Color Computer 3 power transformer accepts 120 VAC, 60 Hz (240 VAC, 50Hz: PAL) input and transforms it to 16.2 VAC (18.52 VAC: PAL) center-tapped for use by the power supply. The current rating of the secondary of the transformer is AC 2.2 amps (AC1.0 amps: PAL). The transformer should only be replaced with genuine Tandy replacement parts.

5.14 Joysticks

The optional joystick controllers are two identical assemblies which can be plugged into JK1 and JK2. Figure 5-15 shows a schematic of the Joystick Assembly. It simply consists of a push-button switch for the fire button and the dual potentiometers connected by a mechanical assembly.

The mechanical assembly allows both potentiometers to be changed at the same time. This gives the effect of a two-dimensional control.
The potentiometers are connected so that 5 volts are applied to one side of the variable resistor, and ground is connected to the other. This allows the center wiper to vary from 0 to 5 volts as the handle is moved. The push-button switch merely provides a momentary ground contact for an input signal.

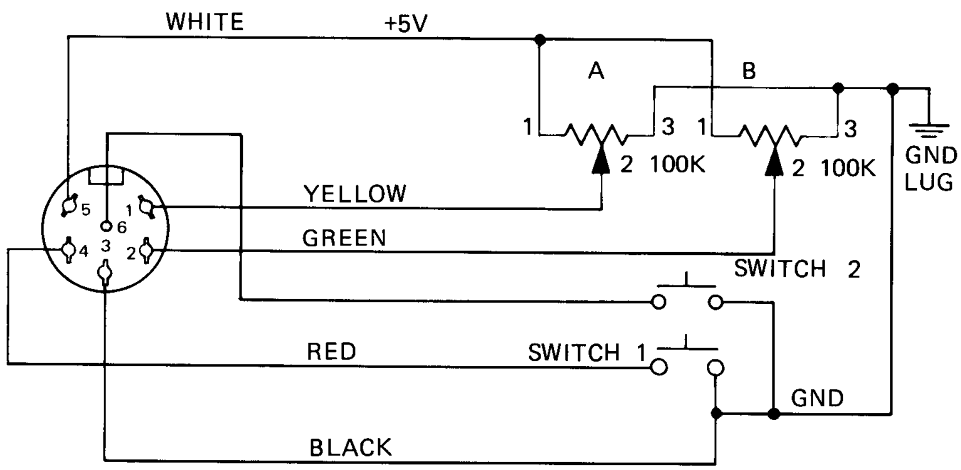


Figure 5-15. Joystick Schematic

5.15 TV Switch Box (NTSC Version Only)

The antenna switch box consists of a switch and a balun, with connectors provided for attachment to the computer, the TV antenna, and the home TV. The switch box is connected to the customer's TV through the 300-ohm twin-lead output. The TV antenna is attached directly to the switch box. The computer output is connected through a 75-ohm coaxial cable to the phono plug input on the switch box.

Figure 5-16 shows a schematic of the antenna switch box.

From the computer, the signal is connected to a balun in the switch box which matches the modulator's 75-ohm output impedance to a TV's 300-ohm antenna input impedance. This signal is then connected to the switch. The switch is specially designed to provide the 60 dB of isolation required between the computer and the TV antenna.

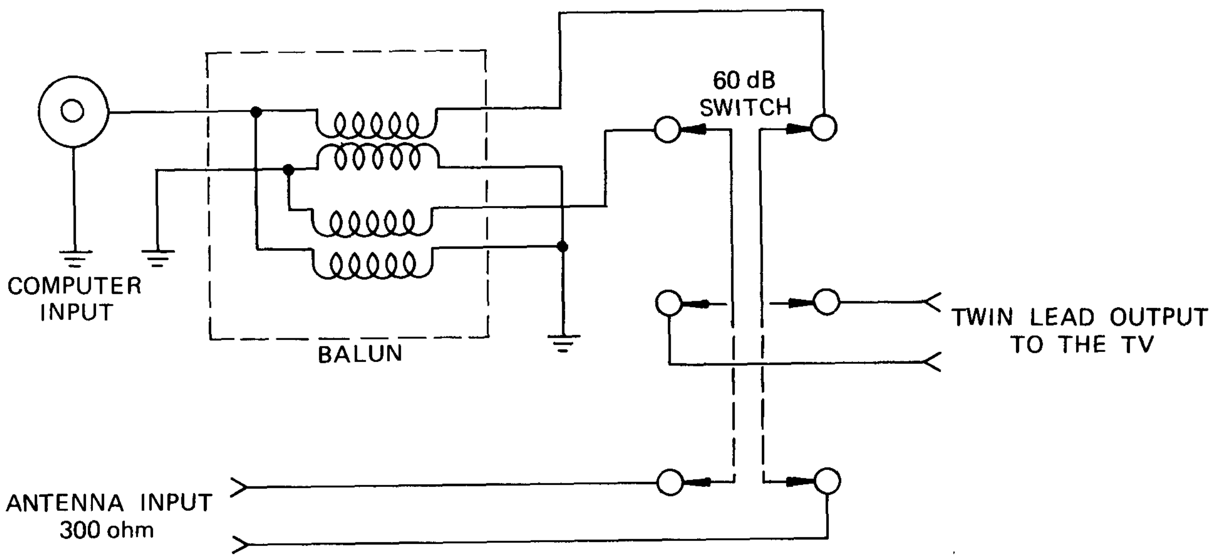


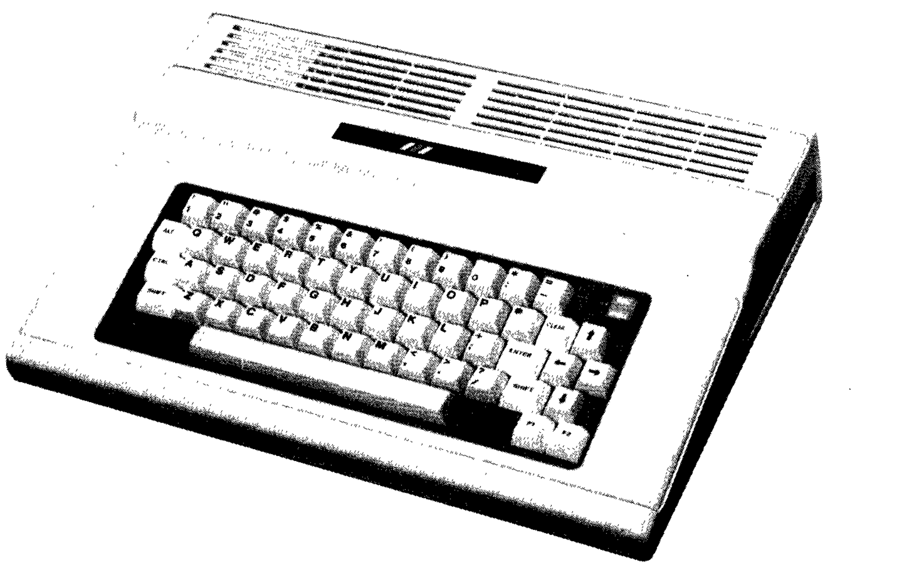
Figure 5-16. Antenna Switch Box Schematic

TANDY®

Service Manual

26-3334

COLOR COMPUTER 3
NTSC/PAL VERSION
with 512K Expansion RAM Card
Catalog Number: 26-3334



CUSTOM MANUFACTURED FOR RADIO SHACK, A DIVISION OF TANDY CORPORATION

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1.1 Introduction

The Color Computer 3 is a refined version of Tandy's popular Color Computer 2. It is designed to provide the same reliable operation as its predecessor, but it incorporates the latest in electronic technology. Figure 1-1 shows a typical installation of the Color Computer 3.

The Color Computer 3 contains an internal BASIC program in ROM which is accessed when the unit is powered up. Other program modules/cartridges may be inserted into the receptacle on the right side of the unit. An optional Multi-pak Interface module allows up to four program paks to be installed at the same time, with selection of the specific module active at any one time selected either by software or by a switch on the Multi-pak Interface. Additional peripheral devices, such as an external disk drive, may be added to the Color Computer 3 for additional memory storage and retrieval.

All input and output ports for the Color Computer 3, with the exception of the program module/cartridge slot and the RGB monitor output (for CM-8), are located on the rear panel of the unit. These include the joystick input ports (right and left), Serial I/O, Cassette I/O, TV output jack (for standard color television set and composite monitor), POWER ON/OFF switch and RESET switch. A recessed channel switch (for selecting either channel on the TV - 3/4 for NTSC and 1/2 for PAL version) is also located on the rear panel of the unit.

Note: Before installing any peripheral device, always remember to unplug the Color Computer's power cord. This will prevent damage to the device or to the Color Computer 3.

1.2 System Description

The primary functions of the Color Computer 3 are performed by four Large Scale Integration (LSI) chips, plus Random Access Memory (RAM) and Read Only Memory (ROM). These four chips are labeled on the block diagram as CPU, ACVC and two PIAs. With only these four chips, plus Random Access Memory (RAM), Read Only Memory (ROM) and a power supply, the Color Computer 3 will operate and provide video output (RF, Composite, Analog RGB). However, to allow communication with the outside world, I/O interfaces must be added.

The main component of any computer system is the Central Processing Unit (CPU, IC1). It is the function of the CPU to provide or request data and select the proper address for this data. In addition, the CPU is capable of performing a limited set of mathematical and logical operations on the data.

ROM (IC2) has the function of providing the CPU with a predefined set of instructions. Without ROM, the CPU would run wild and randomly execute instructions. In normal operation, the CPU jumps to the start address in ROM, after the reset switch has been pressed, and then performs the reset program to set up all of the programmable devices. Following this, the BASIC interpreter residing in ROM is in control of the CPU.

RAM (IC16 - IC19) provides storage for the programs and/or data currently being executed. In the standard unit, these four ICs are 64K x 4 but may be upgraded to sixteen 256K x 1 ICs as an option. (See Paragraph 3.3 on page 28 for instructions.) In addition, the same RAM is used to generate the video display. Normally, no conflict will be observed because the program will use one portion of RAM and the display will use another. During normal usage, the BASIC interpreter, located in ROM, will control the execution of programs located in RAM.

A central component in the Color Computer 3 is the Advanced Color Video Chip (IC6). This chip provides refresh and address multiplexing for the RAM. It also provides all of the system timing and device selection.

ACVC comprises the VDG (Video Display Generator) function which supports High-Resolution mode, in addition to all other modes included in the Color Computer 2. During High-Resolution mode, it generates 40 x 24 or 80 x 24 text screen, and 320 x 192 or 640 x 192 graphics screen. It is also designed to output two different video signals - composite video and analog RGB.

ACVC can expand memory space up to 512K bytes. Having a built-in MMU (Memory Management Unit), it can support 2 banks of 256K-byte RAM, each with a 9-line address bus, even though the CPU possesses only 16 address lines.

The remaining circuitry in the Color Computer 3 is devoted to Input/Output (I/O) communication. The most important part of this circuitry is the keyboard, which allows the operator to enter information. Other I/O circuits are provided to allow joystick input, cassette input and output, and RS-232C input and output.

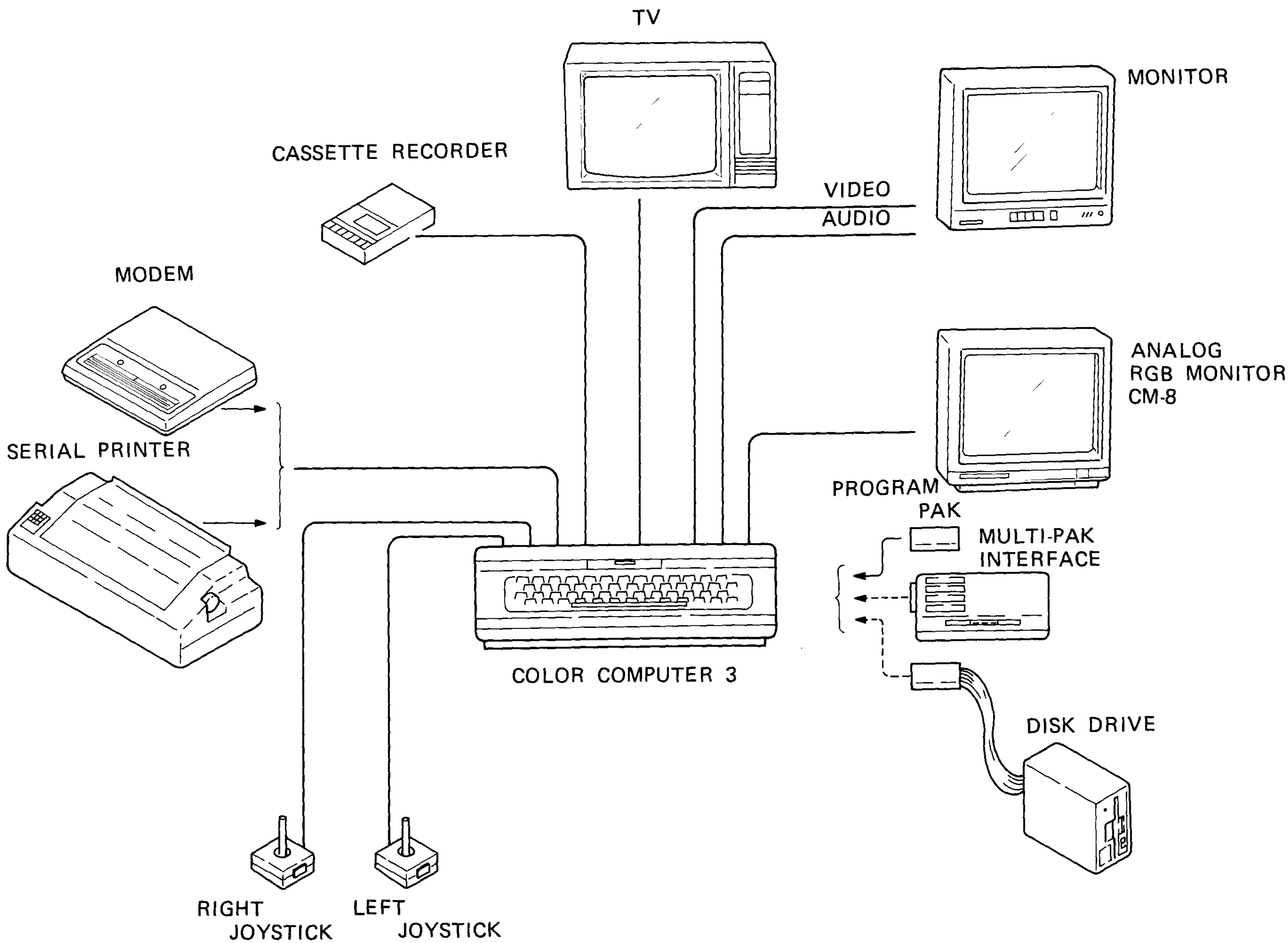


Figure 1-1. Color Computer 3 Installation

1.3 Memory Map

Figure 1-2 shows the breakdown of the large blocks of memory in the Color Computer 3.

The rest of the section itemizes the following registers:

- I/O Control Register
- Chip Control Register
- 68B09E Vector Register

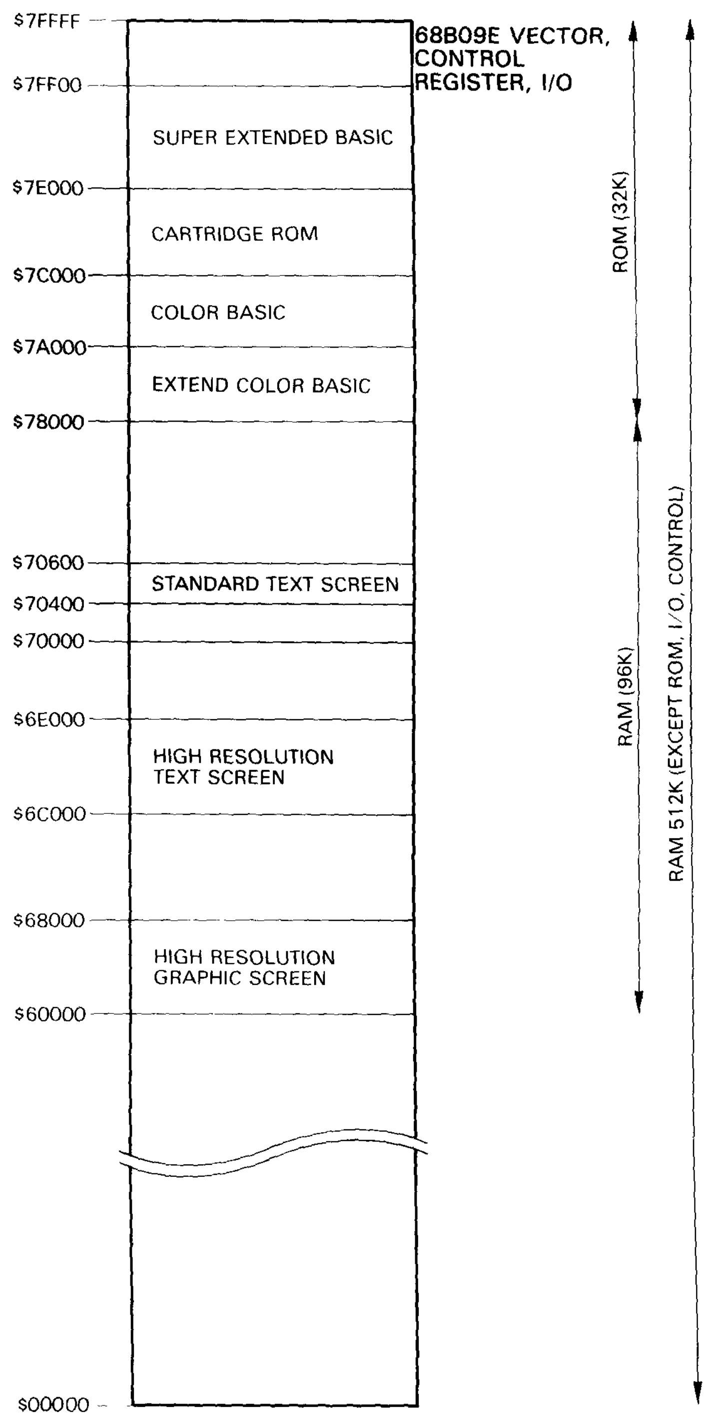


Figure 1-2. Color Computer 3 Memory Map

1.4 I/O Control Registers

FF00 - FF03	PIA	IC5

FF00:

BIT 0 = KEYBOARD ROW 1 and right joystick switch 1
BIT 1 = KEYBOARD ROW 2 and left joystick switch 1
BIT 2 = KEYBOARD ROW 3 and right joystick switch 2
BIT 3 = KEYBOARD ROW 4 and left joystick switch 2
BIT 4 = KEYBOARD ROW 5
BIT 5 = KEYBOARD ROW 6
BIT 6 = KEYBOARD ROW 7
BIT 7 = JOYSTICK COMPARISON INPUT

FF01:

BIT 0	Control of HSYNC (63.5μs) Interrupt	0 = IRQ* to CPU Disabled 1 = IRQ* to CPU Enabled
BIT 1	Control of Interrupt Polarity	0 = Flag set on the falling edge of HS 1 = Flag set on the rising edge of HS

BIT 2 = Normally 1: 0 = Changes FF00 to the data direction register
BIT 3 = SEL 1: LSB of the two analog MUX select lines
BIT 4 = 1 Always
BIT 5 = 1 Always
BIT 6 = Not used
BIT 7 = Horizontal sync interrupt flag

FF02:

BIT 0 = KEYBOARD COLUMN 1
BIT 1 = KEYBOARD COLUMN 2
BIT 2 = KEYBOARD COLUMN 3
BIT 3 = KEYBOARD COLUMN 4
BIT 4 = KEYBOARD COLUMN 5
BIT 5 = KEYBOARD COLUMN 6
BIT 6 = KEYBOARD COLUMN 7/RAM SIZE OUTPUT
BIT 7 = KEYBOARD COLUMN 8

FF03:

BIT 0	Control of VSYNC (16.667ms) Interrupt	0 = IRQ* to CPU Disabled 1 = IRQ* to CPU Enabled
BIT 1	Control of Interrupt Polarity	0 = sets flag on falling edge FS 1 = sets flag on rising edge FS

BIT 2 = NORMALLY 1: 0 = changes FF02 to the data direction register
BIT 3 = SEL 2: MSB of the two analog MUX select lines
BIT 4 = 1 Always
BIT 5 = 1 Always
BIT 6 = Not used
BIT 7 = Field sync interrupt flag

FF20 - FF23	PIA	IC4

FF20:

BIT 0 = CASSETTE DATA INPUT
BIT 1 = RS-232C DATA OUTPUT
BIT 2 = 6 BIT D/A LSB
BIT 3 = 6 BIT D/A
BIT 4 = 6 BIT D/A
BIT 5 = 6 BIT D/A
BIT 6 = 6 BIT D/A
BIT 7 = 6 BIT D/A MSB

FF21:

BIT 0	Control of the CD (RS-232C status) Interrupt	0 = FIRQ* to CPU Disabled 1 = FIRQ* to CPU Enabled
BIT 1	Control of Interrupt Polarity	0 = sets flag on falling edge CD 1 = sets flag on rising edge CD

BIT 2 = Normally 1: 0 = changes FF20 to the data direction register
BIT 3 = Cassette Motor Control: 0 = OFF 1 = ON
BIT 4 = 1 Always
BIT 5 = 1 Always
BIT 6 = Not Used
BIT 7 = CD Interrupt Flag

FF22:

BIT 0 = RS-232C DATA INPUT	
BIT 1 = SINGLE BIT SOUND OUTPUT	
BIT 2 = RAM SIZE INPUT	
BIT 3 = RGB Monitor Sensing INPUT	CSS
BIT 4 = VDG CONTROL OUTPUT	GM0 & UPPER/LOWER CASE*
BIT 5 = VDG CONTROL OUTPUT	GM1 & INVERT
BIT 6 = VDG CONTROL OUTPUT	GM2
BIT 7 = VDG CONTROL OUTPUT	A*/G

FF23:

BIT 0	Control of the Cartridge Interrupt	0 = FIRQ* to CPU Disabled 1 = FIRQ* to CPU Enabled
BIT 1	Control of Interrupt Polarity	0 = sets flag on falling edge CART* 1 = sets flag on rising edge CART*

BIT 2 = Normally 1: 0 = changes FF22 to the data direction register
BIT 3 = Sound Enable
BIT 4 = 1 Always
BIT 5 = 1 Always
BIT 6 = Not used
BIT 7 = Cartridge Interrupt Flag

FF40 - FFBF: Not used

Note: FF22, FF23 are duplicated in tcc1014 (VC2645QC), and V.D.G Control Bit (Bit 3 through Bit 7) affects this IC (TCC1014) only.

1.5 Chip Control Registers

FF90 - FFDF	ACVC	IC6

FF90: Initialization Register 0 (INIT0)

BIT 7	= COCO	1 = Color Computer 1 and 2 Compatible
BIT 6	= M/P	1 = MMU enabled
BIT 5	= IEN	1 = Chip IRQ output enabled
BIT 4	= FEN	1 = Chip FIRQ output enabled
BIT 3	= MC3	1 = DRAM at XFEXX is constant
BIT 2	= MC2	1 = Standard SCS
BIT 1	= MC1	ROM map control (See table below)
BIT 0	= MC0	ROM map control (See table below)

MC1	MC0	ROM mapping
0	x	16K Internal, 16K External
1	0	32K Internal
1	1	32K External (except for vectors)

FF91: Initialization Register 1 (INIT1)

BIT 7	-	
BIT 6	-	
BIT 5	= TINS	Timer Input Select: 1 = 70 nsec / 0 = 63 µsec
BIT 4	-	
BIT 3	-	
BIT 2	-	
BIT 1	-	
BIT 0	= TR	MMU Task Register Select

FF92: Interrupt Request Enable Register (IRQENR)

BIT 7	-	
BIT 6	-	
BIT 5	= TMR	Interrupt from Timer enabled
BIT 4	= HBORD	Horizontal Border IRQ enabled
BIT 3	= VBORD	Vertical Border IRQ enabled
BIT 2	= EI2	Serial Data IRQ enabled
BIT 1	= EI1	Keyboard IRQ enabled
BIT 0	= EI0	Cartridge IRQ enabled

FF93: Fast Interrupt Request Enable Register (FIRQENR)

BIT 7	-	
BIT 6	-	
BIT 5	= TMR	Interrupt from Timer enabled
BIT 4	= HBORD	Horizontal Border FIRQ enabled
BIT 3	= VBORD	Vertical Border FIRQ enabled
BIT 2	= EI2	Serial Data FIRQ enabled
BIT 1	= EI1	Keyboard FIRQ enabled
BIT 0	= EI0	Cartridge FIRQ enabled

FF94: Timer Most Significant Nibble
FF95: Timer Least Significant Byte

TIMER: This is a 12-bit interval timer. When a value is loaded into the MSB, the count is automatically begun. The input clock is either 14 MHz or horizontal sync, as selected by TINS (bit 5 of FF91). As the count falls through zero, an interrupt is generated (if enabled), and the count is automatically reloaded.

FF96: Reserved
FF97: Reserved
FF98: Video Mode Register

BIT 7 = BP		0 = alphanumeric, 1 = bit plane
BIT 6	-	
BIT 5 = BPI		1 = Burst phase inverted
BIT 4 = MOCH		1 = monochrome (on composite)
BIT 3 = H50		1 = 50 Hz vertical sync
BIT 2 = LPR2		Lines per row (See table below)
BIT 1 = LPR1		Lines per row (See table below)
BIT 0 = LPR0		Lines per row (See table below)

LPR2	LPR1	LPR0	Lines per character row	
0	0	0	one	(Graphics modes)
0	0	1	two	(CoCo 1 and CoCo 2 only)
0	1	0	three	(CoCo 1 and CoCo 2 only)
0	1	1	eight	
1	0	0	nine	
1	0	1	(reserved)	
1	1	0	twelve	(CoCo 1 and CoCo 2 only)
1	1	1	(reserved)	

FF99: Video Resolution Register

BIT 7	-	
BIT 6 = LPF1		Lines per field (See table below)
BIT 5 = LPF0		Lines per field
BIT 4 = HRES2		Horizontal resolution (See Video resolution on page 17)
BIT 3 = HRES1		Horizontal resolution
BIT 2 = HRES0		Horizontal resolution
BIT 1 = CRES1		Color resolution (See Video resolution)
BIT 0 = CRES0		Color resolution

LPF1	LPF0	Lines per field
0	0	192
0	1	200
1	0	Reserved
1	1	225

FF9A: Border Register (All bits are 0 for CoCo 1 and CoCo 2 compatibility).

BIT 7	-	
BIT 6	-	
BIT 5 = RED1		Most significant red bit
BIT 4 = GRN1		Most significant green bit
BIT 3 = BLU1		Most significant blue bit
BIT 2 = RED0		Least significant red bit
BIT 1 = GRN0		Least significant green bit
BIT 0 = BLU0		Least significant blue bit

FF9B: Reserved

FF9C: Vertical Scroll Register

BIT 7	-	
BIT 6	-	
BIT 5	-	
BIT 4	-	
BIT 3 = VSC3		(Vert. Scroll)
BIT 2 = VSC2		
BIT 1 = VSC1		
BIT 0 = VSC0		

NOTE: In the CoCo mode, the VSC's must be initialized to 0F hex.

FF9D: Vertical Offset 1 Register

BIT 7 = Y18	(Vert. Offset)
BIT 6 = Y17	
BIT 5 = Y16	
BIT 4 = Y15	
BIT 3 = Y14	
BIT 2 = Y13	
BIT 1 = Y12	
BIT 0 = Y11	

FF9E: Vertical Offset 0 Register

BIT 7 = Y10	(Vert. Offset)
BIT 6 = Y9	
BIT 5 = Y8	
BIT 4 = Y7	
BIT 3 = Y6	
BIT 2 = Y5	
BIT 1 = Y4	
BIT 0 = Y3	

NOTE: In CoCo mode, Y15 - Y9 are not effective, and are controlled by SAM bits F6 - F0. Also in CoCo mode, Y18 - Y16 should be 1, all others 0.

FF9F: Horizontal Offset 0 Register

BIT 7 = HVEN		Horizontal Virtual Enable
BIT 6 = X6		Horizontal Offset address
BIT 5 = X5		Horizontal Offset address
BIT 4 = X4		Horizontal Offset address
BIT 3 = X3		Horizontal Offset address
BIT 2 = X2		Horizontal Offset address
BIT 1 = X1		Horizontal Offset address
BIT 0 = X0		Horizontal Offset address

NOTE: HVEN enables a horizontal screen width of 128 bytes regardless of the HRES bits and CRES bits selected. This will allow a "virtual" screen somewhat larger than the displayed screen. The user can move the "window" (the displayed screen) by means of the horizontal offset bits. In character mode, the screen width is 128 characters regardless of attribute (or 64, if double-wide is selected).

Memory Management Unit (MMU)

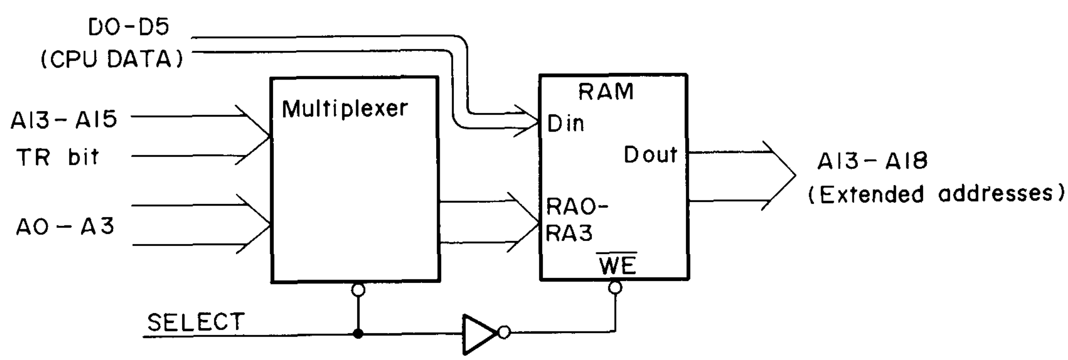
XFFA0 - XFFAF, 6 bits (Write only)

The 8-bit CPU in the Color Computer 3 can directly address only 64K bytes of memory with its 16 address lines (A0 - A15). The memory management unit (MMU) extends the address lines to 19 (A0 - A18). This allows the computer to address up to 512K bytes of memory ($00000 - $7FFFF).

The MMU consists of a multiplexer and a 16 x 6-bit of RAM array. Each of the 6-bit elements in this RAM array is an MMU task register, and the task registers are used by the computer to determine the proper 8K segment of memory to address. These registers are divided into 2 sets, 8 registers per set. The TR bit of FF91 (task register select bit) determines which set is selected.

The relationship between the data in the task register and the generated address is as follows:

Bit	D5	D4	D3	D2	D1	D0
Corresponding memory address	A18	A17	A16	A15	A14	A13



When the CPU needs to access memory outside the standard I/O and control range (XFF00 - XFFFF), CPU address lines A13 - A15 and the TR bit determine the address of the task register which the MMU will access while SELECT is low. When the CPU writes data to the MMU, A0 - A3 determine the address of the task register to be written to when SELECT goes high.

The data from the MMU is then used as the upper 6 address lines (A13 - A18) for memory access, according to the following:

TR	A15	A14	A13	(Address range)	MMU location address
0	0	0	0	X0000 - X1FFF	FFA0
0	0	0	1	X2000 - X3FFF	FFA1
0	0	1	0	X4000 - X5FFF	FFA2
0	0	1	1	X6000 - X7FFF	FFA3
0	1	0	0	X8000 - X9FFF	FFA4
0	1	0	1	XA000 - XBFFF	FFA5
0	1	1	0	XC000 - XDFFF	FFA6
0	1	1	1	XE000 - XFFFF	FFA7
1	0	0	0	X0000 - X1FFF	FFA8
1	0	0	1	X2000 - X3FFF	FFA9
1	0	1	0	X4000 - X5FFF	FFAA
1	0	1	1	X6000 - X7FFF	FFAB
1	1	0	0	X8000 - X9FFF	FFAC
1	1	0	1	XA000 - XBFFF	FFAD
1	1	1	0	XC000 - XDFFF	FFAE
1	1	1	1	XE000 - XFFFF	FFAF

It is important to note that, in order for the MMU to function, the CoCo bit of FF90 must be cleared, and the M/P bit of FF90 must be set. Prior to doing this, the desired addressing information for each segment must be loaded into the designated set of task registers. For example, if a standard 64K map is desired in the top of 512K RAM, with the TR bit set to 0, the following values should be pre-loaded into the MMU:

MMU Location address	Data (Hex)	Data (Bin)	Address range
FFA0	38	111000	70000 - 71FFF
FFA1	39	111001	72000 - 73FFF
FFA2	3A	111010	74000 - 75FFF
FFA3	3B	111011	76000 - 77FFF
FFA4	3C	111100	78000 - 79FFF
FFA5	3D	111101	7A000 - 7BFFF
FFA6	3E	111110	7C000 - 7DFFF
FFA7	3F	111111	7E000 - 7FFFF

NOTE: Data loaded can be selected freely within the range of \$00 - \$3F.

COLOR PALETTE

FFB0 - FFBF: 16 addresses, 6 bits each
For the RGB output, the bits are defined as follows:

Data Bit	D5	D4	D3	D2	D1	D0
Corresponding RGB output	R1	G1	B1	R0	G0	B0

For the Composite output, the bits are defined as follows, where I is intensity level and P is phase:

Data Bit	D5	D4	D3	D2	D1	D0
Corresponding composite output	I1	I0	P3	P2	P1	P0

Some Color Examples:

Color	RGB		Composite	
	Binary	Hex	Binary	Hex
White	111111	(3F)	110000	(30)
Black	000000	(00)	000000	(00)
Bright Green	010010	(12)	100010	(22)
Medium Green	010000	(10)	010010	(12)
Dark Green	000010	(02)	000010	(02)
Medium Magenta	101000	(28)	010101	(15)

For CoCo compatibility, the following values should be loaded upon initialization. (**NOTE:** These are the RGB values.)

FFB0	--	Green	(12)
FFB1	--	Yellow	(36)
FFB2	--	Blue	(09)
FFB3	--	Red	(24)
FFB4	--	Buff	(3F)
FFB5	--	Cyan	(10)
FFB6	--	Magenta	(2D)
FFB7	--	Orange	(26)
FFB8	--	Black	(00)
FFB9	--	Green	(12)
FFBA	--	Black	(00)
FFBB	--	Buff	(3F)
FFBC	--	Black	(00)
FFBD	--	Green	(12)
FFBE	--	Black	(00)
FFBF	--	Orange	(26)

NOTE: For the PAL version, ignore the table attributed to composite.

VIDEO RESOLUTION

The combination of HRES and CRES bits determine the resolution of the screen. The following resolutions are supported:

Alphanumerics: BP = 0, CoCo = 0

RES Bit / Mode	HRES2	HRES1	HRES0	CRES1	CRES0
32 character	0	-	0	-	1
40 character	0	-	1	-	1
80 character	1	-	1	-	1

Graphics: BP = 1, CoCo = 0

Pixels	Colors	HRES2	HRES1	HRES0	CRES1	CRES0
640	4	1	1	1	0	1
640	2	1	0	1	0	0
512	4	1	1	0	0	1
512	2	1	0	0	0	0
320	16	1	1	1	1	0
320	4	1	0	1	0	1
256	16	1	1	0	1	0
256	4	1	0	0	0	1
256	2	0	1	0	0	0
160	16	1	0	1	1	0

In addition to the above modes, the previous CoCo modes are available.

COLOR COMPUTER MODE SELECTION

	MC6883 (SAM) DISPLAY MODE			REG. FF22				
	V2	V1	V0	7	6	5	4	3
Alphanumerics	0	0	0	0	X	X	0	CSS
Alphanumerics Inverted	0	0	0	0	X	X	0	CSS
Semigraphics - 4	0	0	0	0	X	X	0	X
64 X 64 Color Graphics	0	0	1	1	0	0	0	CSS
128 X 64 Graphics	0	0	1	1	0	0	1	CSS
128 X 64 Color Graphics	0	1	0	1	0	1	0	CSS
128 X 96 Graphics	0	1	1	1	0	1	1	CSS
128 X 96 Color Graphics	1	0	0	1	1	0	0	CSS
128 X 192 Graphics	1	0	1	1	1	0	1	CSS
128 X 192 Color Graphics	1	1	0	1	1	1	0	CSS
256 X 192 Graphics	1	1	0	1	1	1	1	CSS

ALPHANUMERIC MODES

Text screen memory:

```
Even Byte (Character byte)
--------------------------
BIT 7    -
BIT 6 = Character bit 6
BIT 5 = Character bit 5
BIT 4 = Character bit 4
BIT 3 = Character bit 3
BIT 2 = Character bit 2
BIT 1 = Character bit 1
BIT 0 = Character bit 0

Odd Byte (Attribute byte)
-------------------------
BIT 7 = BLINK      Characters blink at 1/2 sec. rate
BIT 6 = UNDLN      Characters are underlined
BIT 5 = FGND2      Foreground color bit (pallette addr.)
BIT 4 = FGND1      Foreground color bit (pallette addr.)
BIT 3 = FGND0      Foreground color bit (pallette addr.)
BIT 2 = BGND2      Background color bit (pallette addr.)
BIT 1 = BGND1      Background color bit (pallette addr.)
BIT 0 = BGND0      Background color bit (pallette addr.)
```

NOTE: Attributes are not available when CoCo = 1.

GRAPHICS MODES

16 Color Modes: (CRES1 = 1, CRES0 = 0)

Byte from DRAM

Bit 7	PA3, First Pixel
Bit 6	PA2, First Pixel
Bit 5	PA1, First Pixel
Bit 4	PA0, First Pixel
Bit 3	PA3, Second Pixel
Bit 2	PA2, Second Pixel
Bit 1	PA1, Second Pixel
Bit 0	PA0, Second Pixel

4 Color Modes: (CRES1 = 0, CRES0 = 1)

Byte from DRAM

Bit 7	PA1, First Pixel
Bit 6	PA0, First Pixel
Bit 5	PA1, Second Pixel
Bit 4	PA0, Second Pixel
Bit 3	PA1, Third Pixel
Bit 2	PA0, Third Pixel
Bit 1	PA1, Fourth Pixel
Bit 0	PA0, Fourth Pixel

2 Color Modes: (CRES1 = 0, CRES0 = 0)

Byte from DRAM

Bit 7	PA0, First Pixel
Bit 6	PA0, Second Pixel
Bit 5	PA0, Third Pixel
Bit 4	PA0, Fourth Pixel
Bit 3	PA0, Fifth Pixel
Bit 2	PA0, Sixth Pixel
Bit 1	PA0, Seventh Pixel
Bit 0	PA0, Eighth Pixel

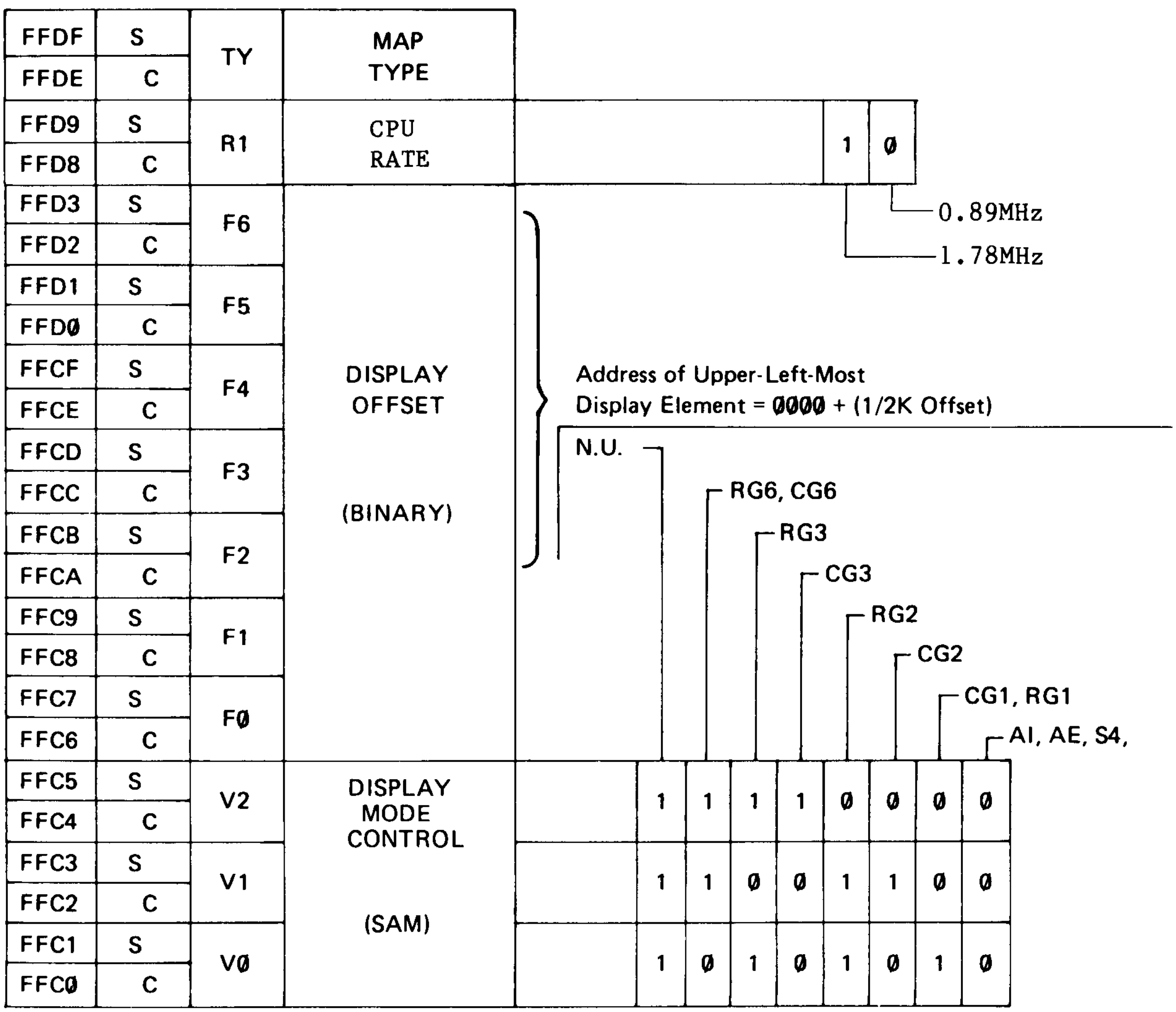
Pallette Addresses

PA3	PA2	PA1	PA0	Address of Contents Displayed
0	0	0	0	FFB0
0	0	0	1	FFB1
0	0	1	0	FFB2
0	0	1	1	FFB3
0	1	0	0	FFB4
0	1	0	1	FFB5
0	1	1	0	FFB6
0	1	1	1	FFB7
1	0	0	0	FFB8
1	0	0	1	FFB9
1	0	1	0	FFBA
1	0	1	1	FFBB
1	1	0	0	FFBC
1	1	0	1	FFBD
1	1	1	0	FFBE
1	1	1	1	FFBF

SAM CONTROL REGISTERS: (FFC0 - FFDF)

Clear		Set		
FFC0	-	FFC1	V0	CoCo graphics mode select
FFC2	-	FFC3	V1	CoCo graphics mode select
FFC4	-	FFC5	V2	CoCo graphics mode select
FFC6	-	FFC7	F0	CoCo Vertical offset
FFC8	-	FFC9	F1	CoCo Vertical offset
FFCA	-	FFCB	F2	CoCo Vertical offset
FFCC	-	FFCD	F3	CoCo Vertical offset
FFCE	-	FFCF	F4	CoCo Vertical offset
FFD0	-	FFD1	F5	CoCo Vertical offset
FFD2	-	FFD3	F6	CoCo Vertical offset
FFD8	-	FFD9	R1	MPU Speed
FFDE	-	FFDF	TY	ROM disable

NOTE: These bits work like the ones in the Motorola SAM chip (MC6883/SN74LS785) in that by writing to the upper address of each two-address group (data is don't care), the bit is set; by writing to the lower address, the bit is cleared. The graphics modes and vertical offset bits are valid only in the CoCo mode, but the other two bits are valid anytime. Note the only semigraphics mode supported is Semi Four.



(S=Set Bit, C=Clear Bit, all Bits are cleared when SAM is reset)

Figure 1-3. Memory Map for SAM Control Register

1.6 68B09E Vector Registers

FFE0 - FFFF	CPU	IC1

FFFF: Reset vector LS

FFFE: Reset vector MS

FFFD: NMI vector LS

FFFC: NMI vector MS

FFFB: SWI1 vector LS

FFFA: SWI1 vector MS

FFF9: IRQ vector LS

FFF8: IRQ vector MS

FFF7: FIRQ vector LS

FFF6: FIRQ vector MS

FFF5: SWI2 vector LS

FFF4: SWI2 vector MS

FFF3: SWI3 vector LS

FFF2: SWI3 vector MS

FFF1: Reserved

FFF0: Reserved

FFEF - FFE0: Not used

LS: Least significant address byte
MS: Most significant address byte

SECTION II. SPECIFICATIONS

2.1 Technical

CPU:	68B09E 8-bit processor Clock Speed - 0.89 MHz/1.78 MHz
MEMORY SIZE:	ROM: 32K Byte (for BASIC) RAM: 128K Byte (Expandable up to 512K)
KEYBOARD:	57 keys, microprocessor-scanned matrix
Number of keys:	57 keys
Alphabetical characters:	26 keys (A to Z)
Numeric characters:	10 keys (0 to 9)
Space key:	1 key
Shift key:	2 keys
Clear key:	1 key
Enter key:	1 key
Break (ESC) key:	1 key
Punctuation key:	7 keys
Directional Control key:	4 keys
Function key:	2 keys (F1 and F2)
Control key:	1 key
Alternate key:	1 key
	57 keys

VIDEO DISPLAY:

Character display:	512 (32 x 16)	upper case characters
	960 (40 x 24)	upper/lower case characters
	1920 (80 x 24)	upper/lower case characters

Graphic display:	256 x 192 dots	8 colors
	320 x 192 dots	16 colors
	640 x 192 dots	4 colors

INTERFACE:

Serial interface: RS-232C 4P-DIN

Cassette interface: 5P DIN 1500 baud

Analog input interface (for JOYSTICK): 6P DIN x 2

Bus line: 40 PIN connector for cartridge

CONTROLS:

Power switch: Push

Reset switch: Key

Channel selector switch: Slide

RF OUTPUT:

	CH	Frequency (Video)	Frequency (Sound)
NTSC	3	61.25 ± 0.25 MHz	4.5 ± 0.02 MHz
	4	67.25 ± 0.25 MHz	4.5 ± 0.02 MHz

	CH	Frequency (Video)	Frequency (Sound)
PAL	1	57.25 ± 0.25 MHz	5.5 ± 0.02 MHz
	2	64.25 ± 0.25 MHz	5.5 ± 0.02 MHz

Output impedance: 75 ohm

RF Output terminal: RCA JACK

RF Output level: NTSC 67^{+2}_{-4} dBμ

PAL 70 ± 5dBμ

VIDEO/SOUND OUTPUT:

Output terminal: RCA JACK

Output level: 1Vp-p

Video: 0.71V ± 0.1V (RL = 75ohm)

Sync: 0.29V ± 0.1V (RL = 75ohm)

Sound: Less than 1.0Vp-p (RL = 600ohm)

RGB (Analog)/Sound OUTPUT

Output terminal: 10pin pin header (Bottom side)

Output level:

NTSC	Red:	0.8(±0.1) - 2.0(±0.2)Vdc (RL = 75ohm) positive
	Green:	0.8(±0.1) - 2.0(±0.2)Vdc (RL = 75ohm) positive
	Blue:	0.8(±0.1) - 2.0(±0.2)Vdc (RL = 75ohm) positive
PAL	Red:	0.6(±0.1) - 1.8(±0.2)Vdc (RL = 75ohm) positive
	Green:	0.6(±0.1) - 1.8(±0.2)Vdc (RL = 75ohm) positive
	Blue:	0.6(±0.1) - 1.8(±0.2)Vdc (RL = 75ohm) positive
	Hsync:	TTL level positive
	Vsync:	TTL level positive
	Sound:	Less than 1.0Vp-p (RL = 600ohm)

POWER SUPPLY: NTSC AC 120V/60Hz, 0.2 Amp RMS typical

PAL AC 240V/50Hz, 0.125 Amp RMS typical

2.2 Physical

DIMENSIONS (Cabinet size):

Width: 14-3/4" (375 mm)

Height: 3-1/8" (79 mm)

Depth: 10-3/8" (264 mm)

NET WEIGHT: 4.85 lbs (2.3 kg)

3.1 Disassembly

1. Disconnect power and remove signal cables from the unit.
2. Remove cartridge from slot (if applicable).
3. Turn the unit over and place it on a soft surface to prevent damage to the keyboard or top cover.
4. Loosen and remove the six (four screws S1 and two longer screws S2) mounting screws which attach the base to the top cover. (Figure 3-1)
5. Disconnect the cable from the wire connector which is attached to the keyboard (Figure 3-2).
6. Then disconnect the power transformer at the 3-pin connector on the main PCB (Figure 3-2).
7. Remove four (two screws S3 and two screws S4) screws which attach the PCB to the bottom case cover (Figure 3-2). If it is necessary to remove the shield from the PCB, do so by removing the 16 rivets which attach it to the PCB.

3.2 Assembly

Assemble the Color Computer 3 in the reverse order of disassembly. The PCB shield is attached to the PCB with metal rivets. These shields must be in place to provide proper RFI shielding.

Set the wire assembly from the transformer and flat cable from the keyboard to the connector on the PCB. Two different types of screws are used to mount the PCB and the top and bottom cabinet. Ensure that the correct type is used when reassembling.

The strain relief on the power cord consists of wrapping the cord around the plastic bosses on the rear side of the unit. Ensure that the power cord is properly routed to afford strain relief to the transformer connections.

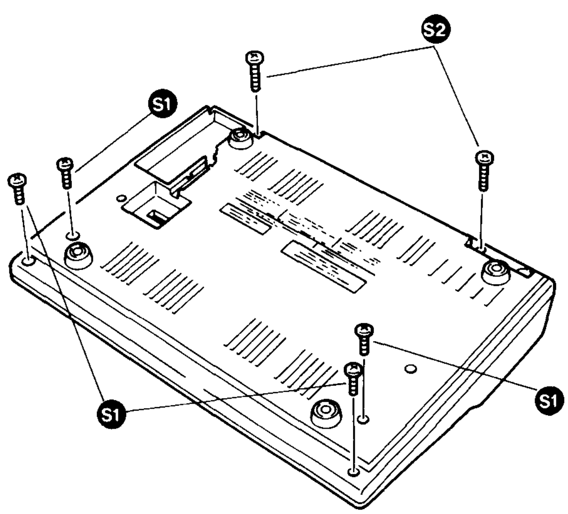


Figure 3-1. Removal of Top Cover

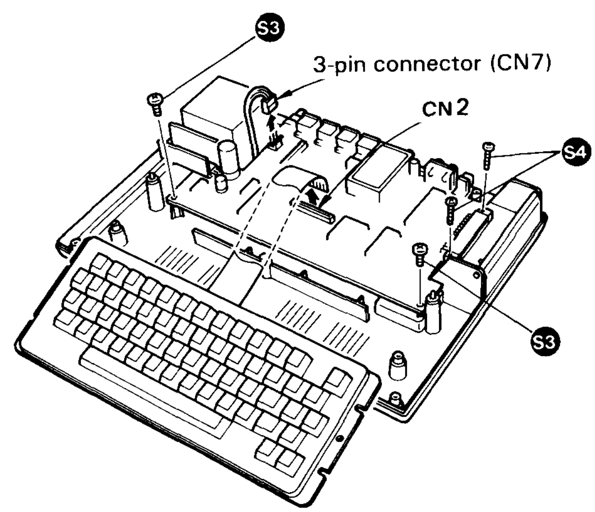


Figure 3-2. Removal of Main PCB

3.3 512K RAM Upgrade Instructions

To upgrade a 128K memory unit to a 512K memory unit, follow the procedure below.

1. Remove the top cabinet as described in 3.1. Remove four ICs (IC16 - IC19) from the IC sockets of the PCB (Figure 3-3), unsolder C65 82 pF ceramic capacitor and remove it.

2. Three nylon stand-offs are packaged with the RAM card. Insert them into corresponding holes of the RAM card (Figure 3-4).

3. Align the pin socket of the RAM card over CN4 through CN6, then slowly lower the Board.

4. Snap each stand-off into the corresponding hole on the computer PCB.

5. Connect the computer's AC cord and signal cables to a TV monitor and run the following program to verify proper operation of the new memory chips.

6. Secure the top and bottom cabinets.

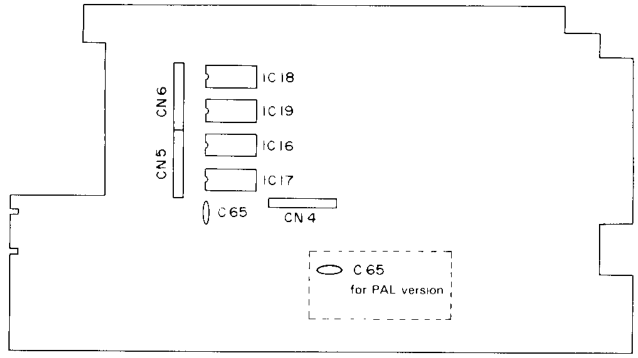


Figure 3-3. Main PCB

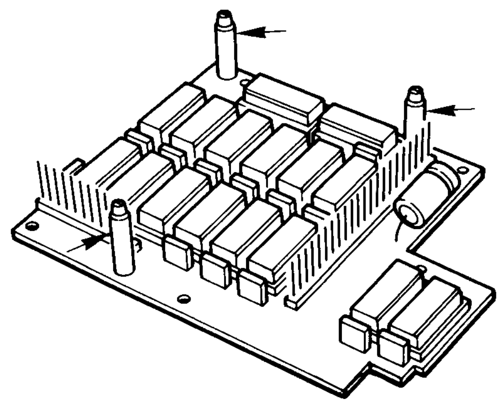


Figure 3-4. 512K RAM Card

<Test Program>

```
10 WIDTH 40:PALETTE 0,0:PALETTE 7,63: CLS8
20 POKE&HFFD9,0
30 FOR A=&H00000 TO &H5FFFF STEP 512
40 D=RND(255)
50 LPOKE A,D
60 B=LPEEK(A)
70 LOCATE 10,2: PRINT"ADDRESS=";A
80 LOCATE 10,4: PRINT"DATA=";D
90 IF B<>D THEN 130
100 NEXT A
110 LOCATE 10,10: PRINT"RAM TEST IS GOOD!"
120 POKE&HFFD8,0: END
130 LOCATE 10,6: PRINT"ERROR!"
140 POKE&HFFD8,0: END
```

SECTION IV. BLOCK DIAGRAM
NTSC VERSION

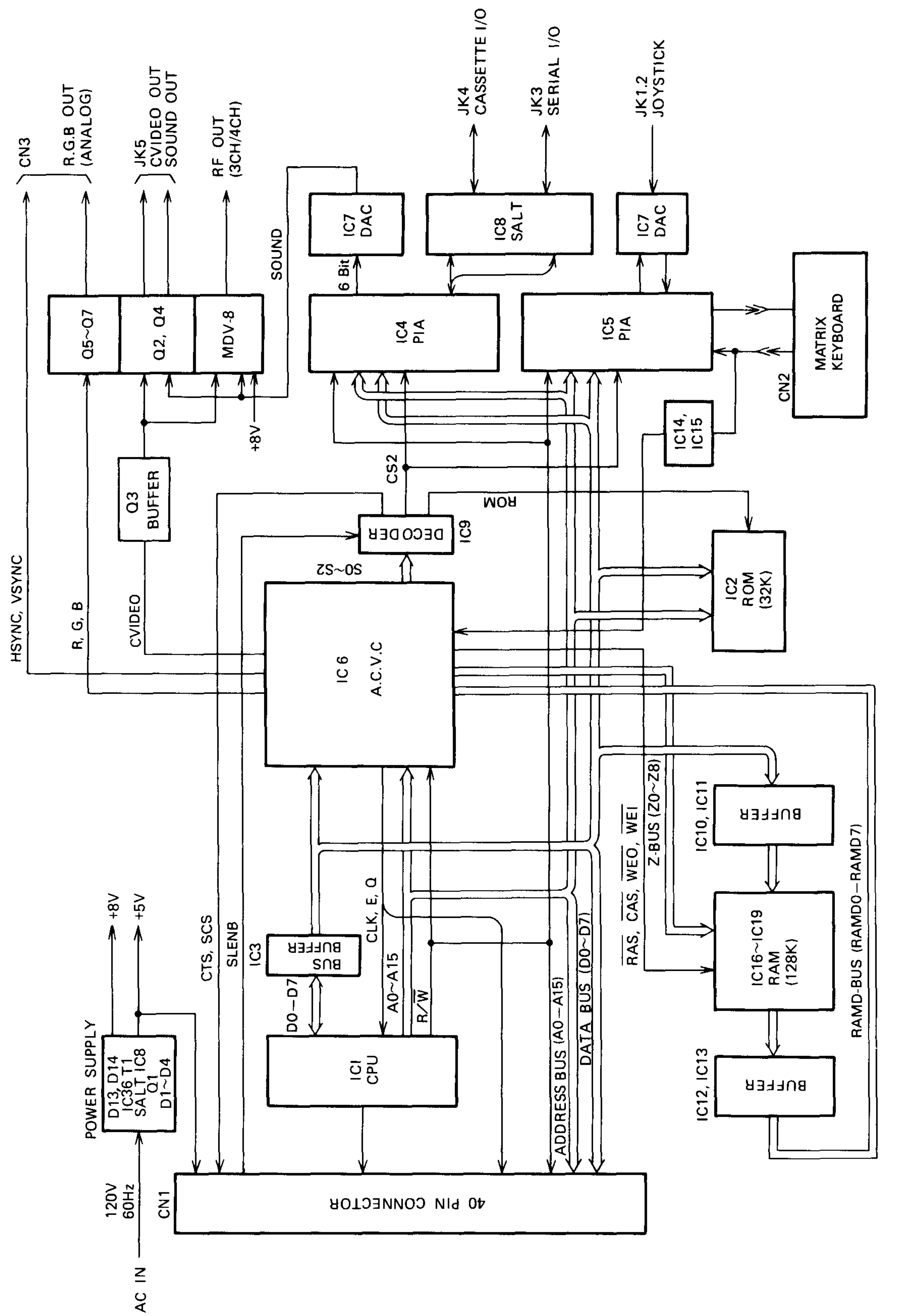
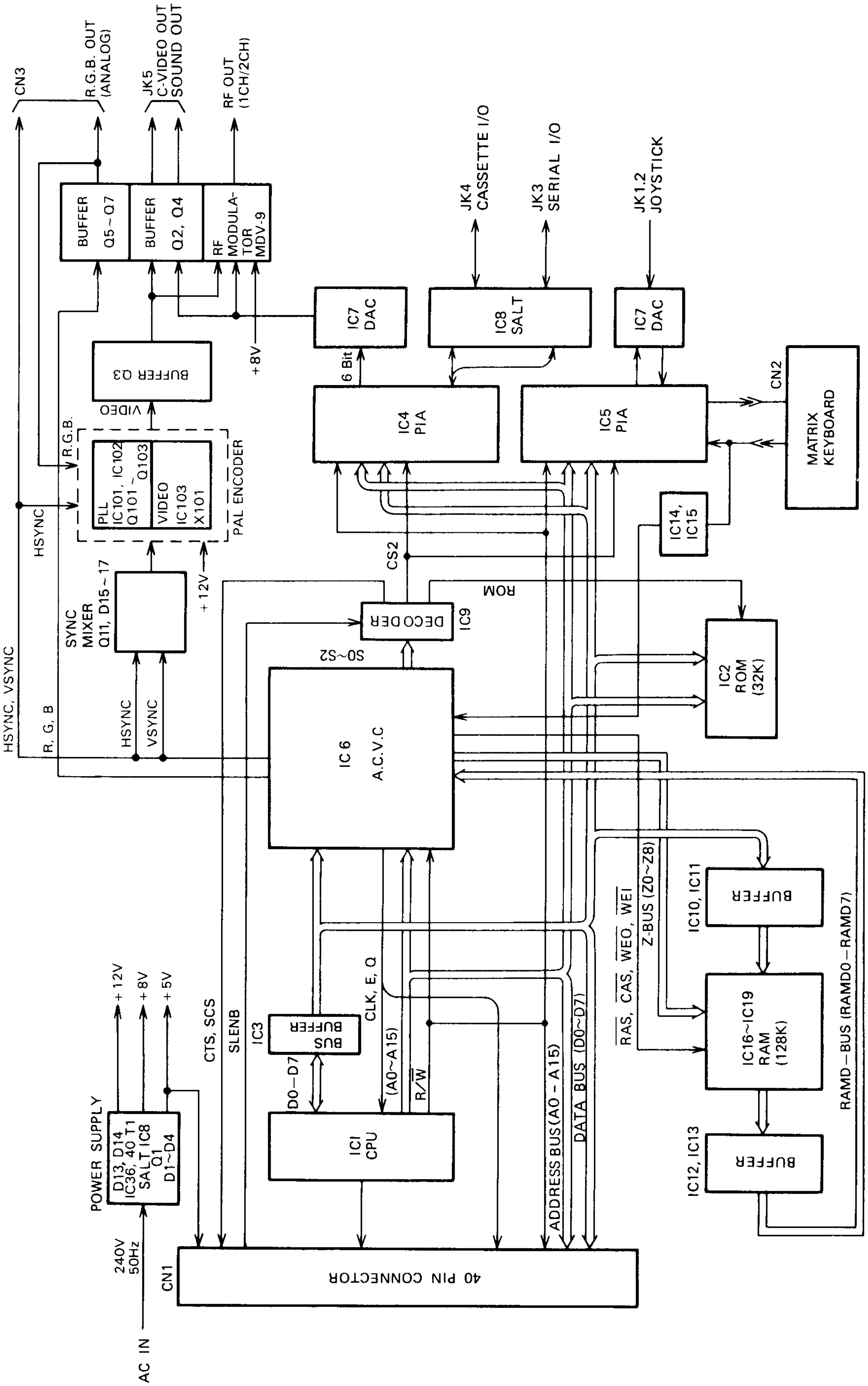


Figure 4-1. Block Diagram

PAL VERSION



CN3
R.G.B. OUT (ANALOG)
JK5 C-VIDEO OUT SOUND OUT
RF OUT (1CH/2CH)
BUFFER Q5~Q7
BUFFER Q2, Q4
RF MODULA-TOR MDV-9
BUFFER Q3
VIDEO
R.G.B.
PLL IC101, IC102 Q101~Q103
VIDEO IC103 X101
PAL ENCODER
HSYNC
SYNC MIXER Q11, D15~17
+12V
+8V
HSYNC, VSYNC
R, G, B
HSYNC
VSYNC
JK4 CASSETTE I/O
JK3 SERIAL I/O
JK1.2 JOYSTICK
IC7 DAC
IC8 SALT
IC7 DAC
6 Bit
IC4 PIA
IC5 PIA
CN2
MATRIX KEYBOARD
IC14, IC15
CS2
ROM
DECODER
IC9
S0~S2
IC2 ROM (32K)
IC 6 A.C.V.C
BUFFER
IC10, IC11
Z-BUS (Z0~Z8)
RAS, CAS, WEO, WEI
IC16~IC19 RAM (128K)
RAMD-BUS (RAMD0-RAMD7)
BUFFER
IC12, IC13
POWER SUPPLY
D13, D14 IC36, 40 T1 SALT IC8 Q1 D1~D4
+12V
+8V
+5V
CTS, SCS
SLENB
IC3
BUS BUFFER
D0-D7
CLK, E, Q
(A0~A15)
R/W
IC1 CPU
ADDRESS BUS (A0 - A15)
DATA BUS (D0~D7)
240V 50Hz
AC IN
CN1
40 PIN CONNECTOR

This section of the manual contains troubleshooting hints, diagnostic routines, and scope waveforms for both NTSC and PAL version for the Color Computer 3. Scope settings are noted on the individual waveform diagrams.

6.1 Introduction

The Color Computer 3 should be serviced only by qualified technicians. Throughout this guide a basic knowledge of computers will be assumed, as well as the ability to use a dual-trace oscilloscope. When servicing any computer, it is important to distinguish a hardware problem from a software problem. Stated another way, just because a particular program does not yield the results desired by the user, the hardware is not necessarily at fault. It is, therefore, recommended that the technician be thoroughly familiar with the operation of the Color Computer 3, as well as the Theory of Operation. Diagnostic aids are available from Radio Shack National Parts to assist the technician in the servicing of the Color Computer 3.

Standard troubleshooting techniques include these steps: identification, localization, and isolation. The first step, identification, consists largely of making sure that a problem exists. In this step it is wise to check the obvious. Doing so can save hours of troubleshooting time only to find out that a cable was bad, or that it was some other relatively minor problem. After identifying that a problem really does exist, localization can usually be accomplished by merely observing the symptoms. Isolating a problem down to the defective component will often involve the use of test equipment, and sometimes, by part substitution.

Following is a list of virtually all of the problems that might be identified on the Color Computer 3:

- 6.2 Video
- 6.3 Keyboard
- 6.4 Processing problems
- 6.5 Cassette
- 6.6 RS-232C
- 6.7 Sound
- 6.8 Joystick
- 6.9 Cartridge problems

If a problem exists in more than one area, the first course of action should be to look for a common cause. Although it is possible to have two or more independent problems, it is more likely that a single failure can cause a multitude of symptoms. It is apparent, for example, that all of the above areas will have problems when the power supply is dead.

Once a problem has been identified in one of the above areas, it can be localized by observing the specific symptom. For example, if a Cassette problem exists, is it a Read problem, a Write problem, or a Motor Control problem? After the problem is localized, isolating it to a specific component is usually not very difficult.

6.2 Video Problems

1) No Display/No Sync/Noisy Video

- Check Cable and Cable Connection
- Check Power Supply and Transistor Bias Voltage (Q2, Q3)
- NTSC: Check Video Signal at TP6
  PAL: Check Video Signal at CVIDEO OUT of CN8

*Before proceeding next check, load Diagnostic Program Pak (Color Bar) or run the program below

- Check Video Signal at Emitter of Q3 and check C67
- Check Video Signal at Emitter of Q2 and check C54
- Check Video level at TP7 (Waveform 1)
- PAL: Check Sync Signal at Collector of Q11 (Waveform 16)
- PAL: Check the items in 5) RGB Problem

```
 10 '**COLOR BAR TEST**
 30 ON BRK GOTO 1000
 40 HSCREEN 2
 50 GOSUB 500
 100 FOR R=0 TO 7
 110 HCOLOR R,8
 120 HLINE(R*40,0)-((R+1)*40,192),
 PSET,BF
 130 NEXT R
 140 GOTO 140
*500 DATA 63,36,31,18
*510 DATA 9,7,11,0
 520 FOR X=0 TO 7
 530 READ A(X):NEXT X
 540 FOR R=0 TO 7
 550 PALETTE R,A(R):NEXT R
 560 RETURN
 1000 PALETTE CMP:END

 * For PAL
   500 DATA 63,54,27,18
   510 DATA 45,36,9,0
```

2) Wrong Color

- Check Video Signal (TP7) and Chroma level (Waveforms 1 and 2)
- Adjust TV control

3) No Color

- Check Video Signal at TP6 (PAL: CVIDEO OUT of CN8) and Color Burst Signal (Waveform 2)

4) Random Character/Clear Screen/No Sign-on

- Check RAS* (TP4), CAS* (TP5)
- Check pin 1 and pin 2 of IC15
- Check pin 20 of IC2
- Check IC16 -19 (Dynamic RAM)
- Check the items in 6.4 Processing Problem

5) RGB Problem

- Check Red, Green, Blue Signal (Waveforms 3 through 5) using Program Pak or Test program below
- Check HSYNC, VSYNC (Waveform 6)

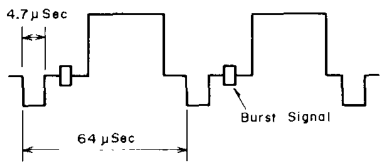
```
 10 'RGB LEVEL CHECK
 11 '*COLOR-D* 4/3/1986
 20 PALETTE RGB
 30 ON BRK GOTO 1000
 40 HSCREEN 2
 50 GOSUB 500
 100 FOR R=0 TO 15
 110 HCOLOR R,0
 120 HLINE(R*20,0)-((R+1)*20,192),
 PSET,BF
 130 NEXT R
 140 GOTO 140
*500 DATA 63,54,27,36
*510 DATA 18,9,32,16
*520 DATA 8,4,2,1
*530 DATA 45,40,5,0
 535 DIM A(16)
 540 FOR X=0 TO 15
 550 READ A(X):NEXT X
 560 FOR R=0 TO 15
 570 PALETTE R,A(R):NEXT R
 580 RETURN
 1000 PALETTE CMP:END

 * For PAL
   500 DATA 63,54,27,18
   510 DATA 45,36,9,0
   520 DATA 56,48,24,16
   530 DATA 40,32,8,7
```

6) Composite Video Signal Adjustment (PAL Version Only)

A. Horizontal Sync Pulse Width adjustment

Connection: connect oscilloscope to JK5 (Composite VIDEO OUT)

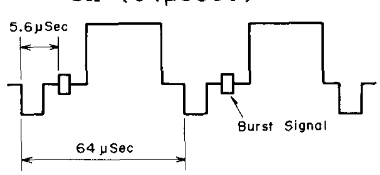
Procedure: adjust VR2 to get 4.7 µsec. sync pulse width.



B. Burst Start Position adjustment

Connection: connect oscilloscope to JK5 (Composite VIDEO OUT).

Procedure:
1. Turn VR101 to fully counterclockwise.
2. Turn VR101 clockwise to obtain 5.6µsec. burst start position.
3. If the start position does not become 5.6µsec, adjust it for maximum.
4. Check to see the burst appears every 1H (64µsec.)



C. Composite Video Output Level adjustment

Connection: connect Oscilloscope to JK5 (Composite VIDEO OUT) terminated by 75 ohms.

Procedure: adjust VR1 to get output level of 1.0Vp -P.

6.3 Keyboard Problems

No Keyboard Entry/Wrong Character

- Check Flex Cable and CN2
- Check pin 23 (CS2*) of IC5
- Check D8 - D11, C18, 19, 22, 23 and IC14

6.4 Processing Problem

- Check OSC Circuit (IC6)
- Check TP2 and TP3 (ECLK and QCLK) (Waveform 7)
- Check TP4 and TP5 (RAS*, CAS*) (Waveforms 8 and 9) and pins 10 and 11 of IC6 (WEO*, WE1*)
- Check Address decode circuit (IC9)
- Check S0 - S2
- Check pin 40 of IC5 (HSYNC*), pin 18 of IC5 (VSYNC*) and pins 37, 38 of IC5 (IRQ*)
- Check pin 40 of IC1 (HALT*), pin 2 of IC1 (NMI*) and pin 4 of ICI (FIRQ*) - these pins are normally High

6.5 Cassette Problems

1) Motor Control Problem

- Run the following program and check pin 39 of IC4 (Waveform 14)
- Check pin 9 of IC8 (SALT)

```
10 POKE 65313,60
20 GOSUB 100
30 POKE 65313,52
40 GOSUB 100
50 GOTO 10
100 FOR A=1 TO 10:NEXT A
110 RETURN
```

2) Write Problem

- Run the following Program and Check pin 17 of IC7 and Pin 1 of IC7. (Waveform 13)

```
10 SOUND 200,255
20 GOTO 10
```

3) Read Problem

- Connect pin 4 and pin 5 of JK4
- Run the above program and check pin 11 of IC8
- Check pin 7 of IC8
- Check R14, C25

6.6 RS-232C Problem

- Run the following program and check pin 3 of IC4 and pin 12 of IC8 (Refer to Waveform 15)

```
10 POKE 65312,2
20 POKE 65312,0
30 GOTO 10
```

- Connect pin 4 and pin 2 of JK3 and run the above program. Check pin 14 of IC8 and check pin 4 of IC8
- Check Resistors R15, R16, R17 and R66 and Diodes D6 and D7

6.7 Sound Problem

- Check TV volume
- Run the following program and check pin 1 of IC7 (Waveform 13)
- Check Bias Voltage of Q4, C55 and C56
- Check TP11
- Check JK5 and pin 7 of CN3

```
10 SOUND 200,255
20 GOTO 10
```

6.8 Joystick Problem

- Run the following program and check if the numbers vary with joystick position or depressing fire button.
- Check D8 - D11 and Components around them (example: C18, C19, C22, C23)

```
5 CLS
10 A=JOYSTK(0)
20 B=JOYSTK(1)
30 C=JOYSTK(2)
40 D=JOYSTK(3)
50 E=(PEEK(65280) AND 1)
60 F=(PEEK(65280) AND 2)/2
70 PRINT @0,A,B,C,D,F,E
80 GOTO 10
```

6.9 Cartridge Problem

- Check CTS* signal
- Check Address/Data Bus (short or open)
- Check pin 8 of CN1 (CART* input) and pin 7 of CN1 (QCLK Output)

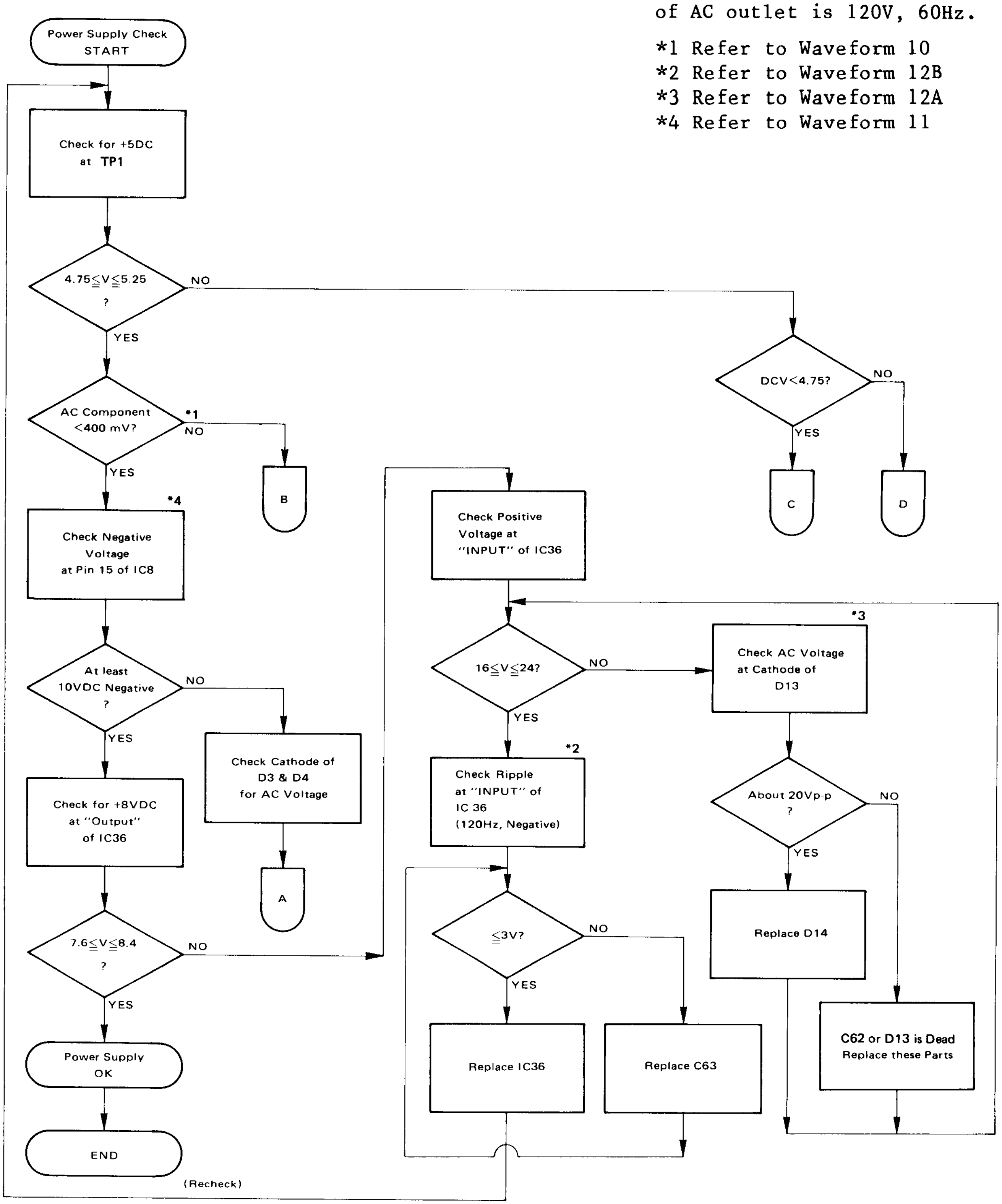
NTSC

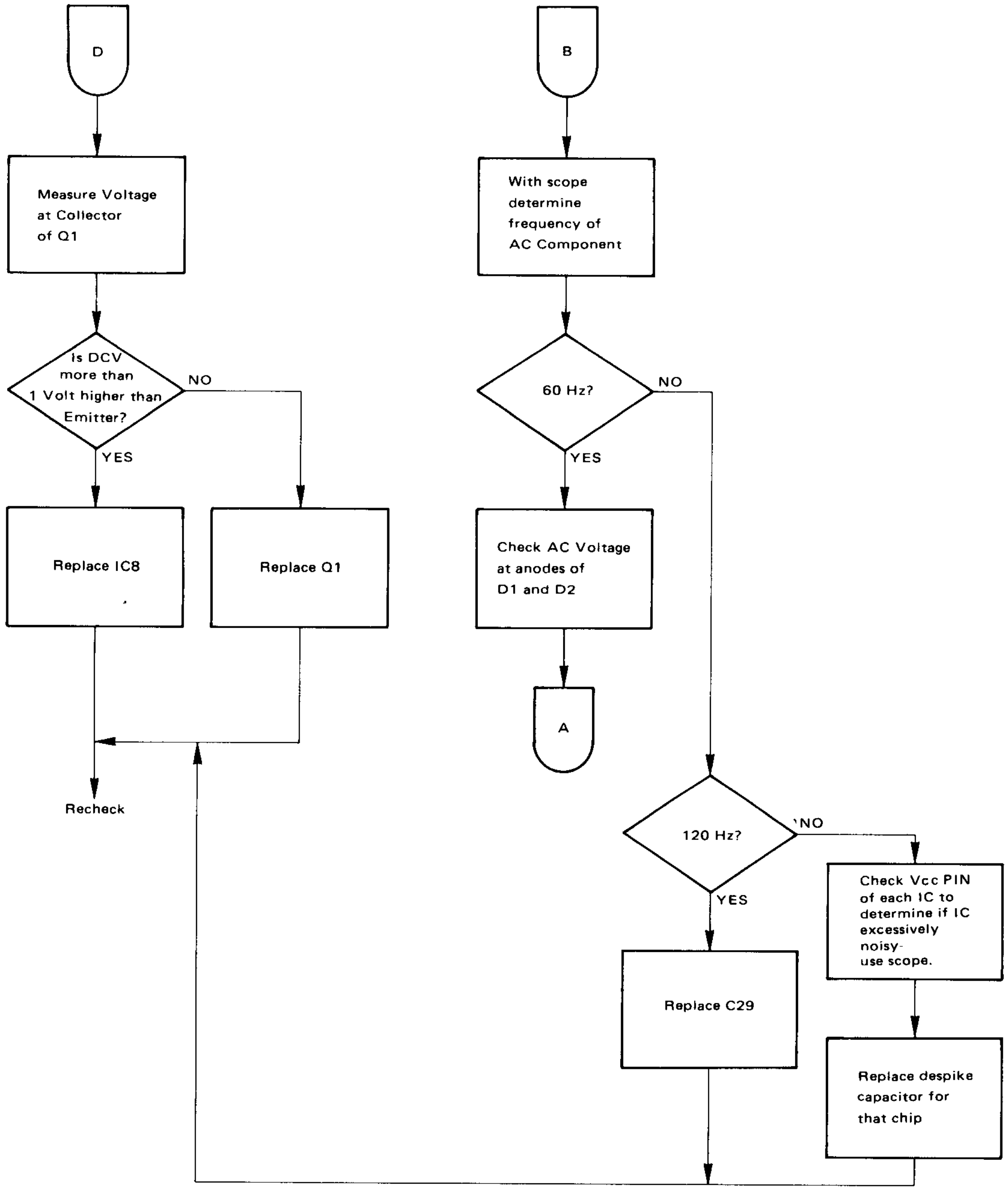
6.10 Power Supply Check

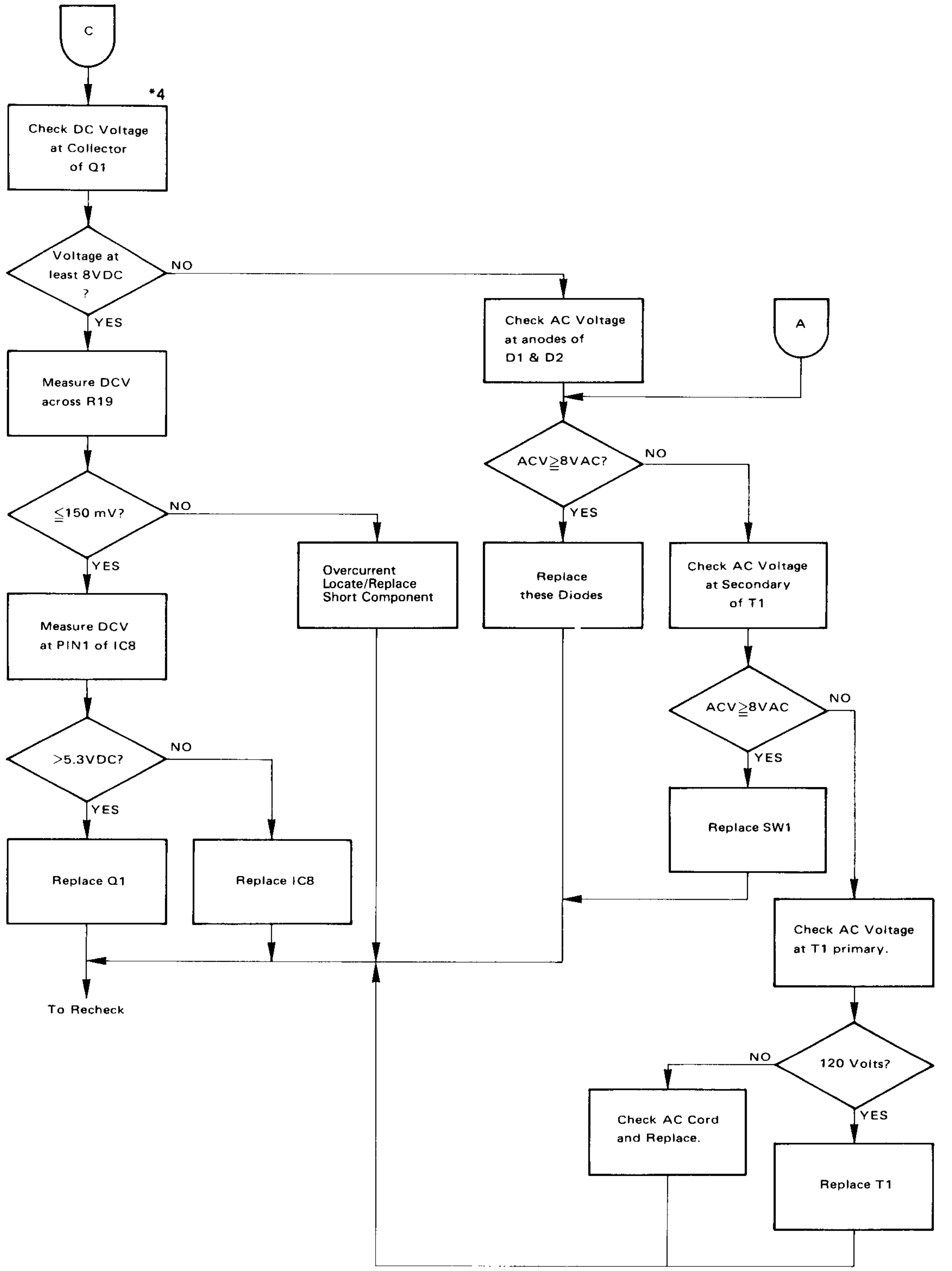
NTSC Version

Note: Check to Confirm the voltage of AC outlet is 120V, 60Hz.

*1 Refer to Waveform 10
*2 Refer to Waveform 12B
*3 Refer to Waveform 12A
*4 Refer to Waveform 11



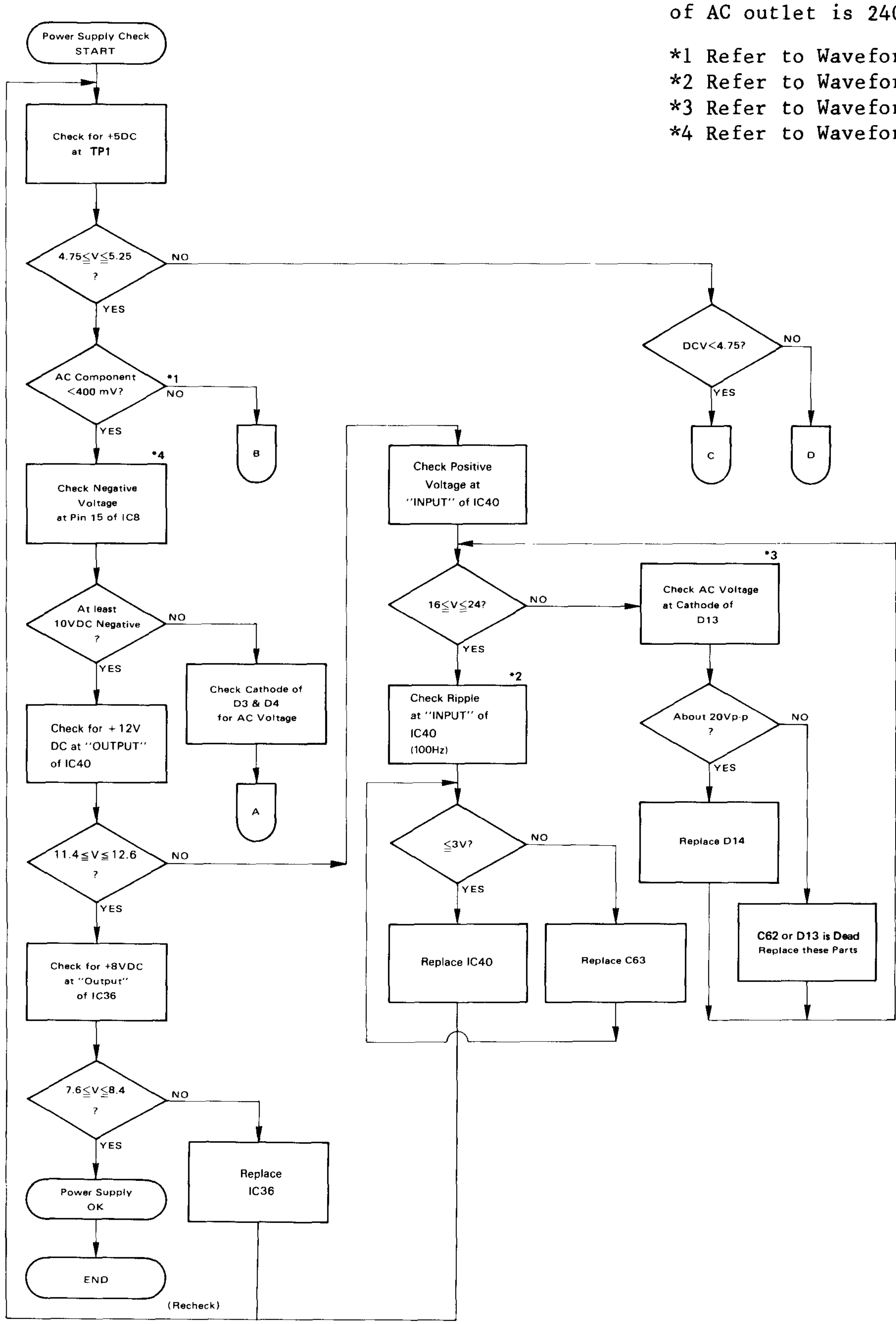

D
Measure Voltage at Collector of Q1
Is DCV more than 1 Volt higher than Emitter?
NO
YES
Replace IC8
Replace Q1
Recheck
B
With scope determine frequency of AC Component
60 Hz?
NO
YES
Check AC Voltage at anodes of D1 and D2
A
120 Hz?
NO
YES
Check Vcc PIN of each IC to determine if IC excessively noisy-use scope.
Replace C29
Replace despike capacitor for that chip

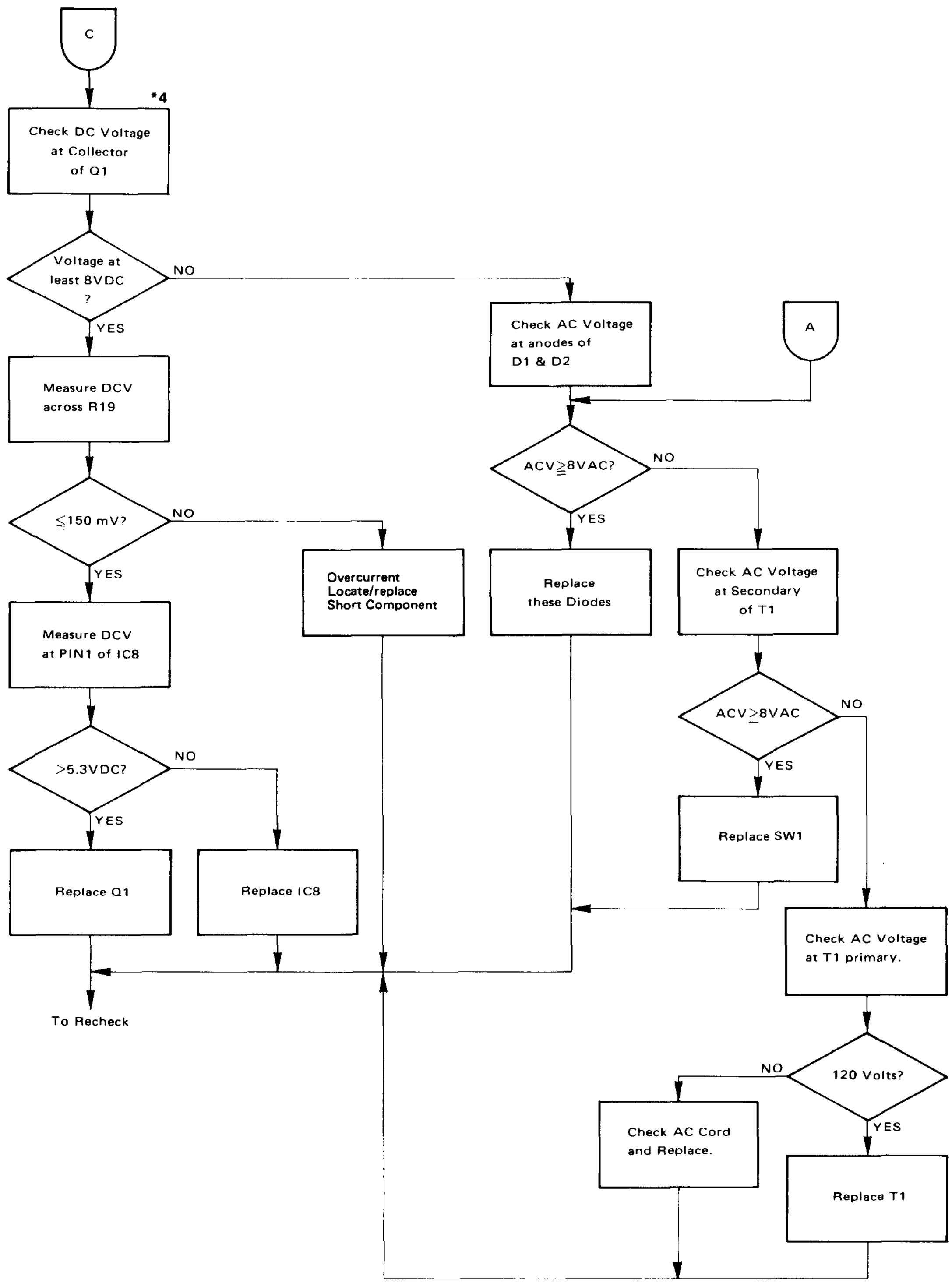

C
*4
Check DC Voltage at Collector of Q1
Voltage at least 8VDC ?
NO
YES
Measure DCV across R19
≦150 mV?
NO
YES
Measure DCV at PIN1 of IC8
>5.3VDC?
NO
YES
Replace Q1
Replace IC8
To Recheck
Overcurrent Locate/Replace Short Component
Check AC Voltage at anodes of D1 & D2
A
ACV≧8VAC?
NO
YES
Replace these Diodes
Check AC Voltage at Secondary of T1
ACV≧8VAC
NO
YES
Replace SW1
Check AC Voltage at T1 primary.
120 Volts?
NO
YES
Check AC Cord and Replace.
Replace T1

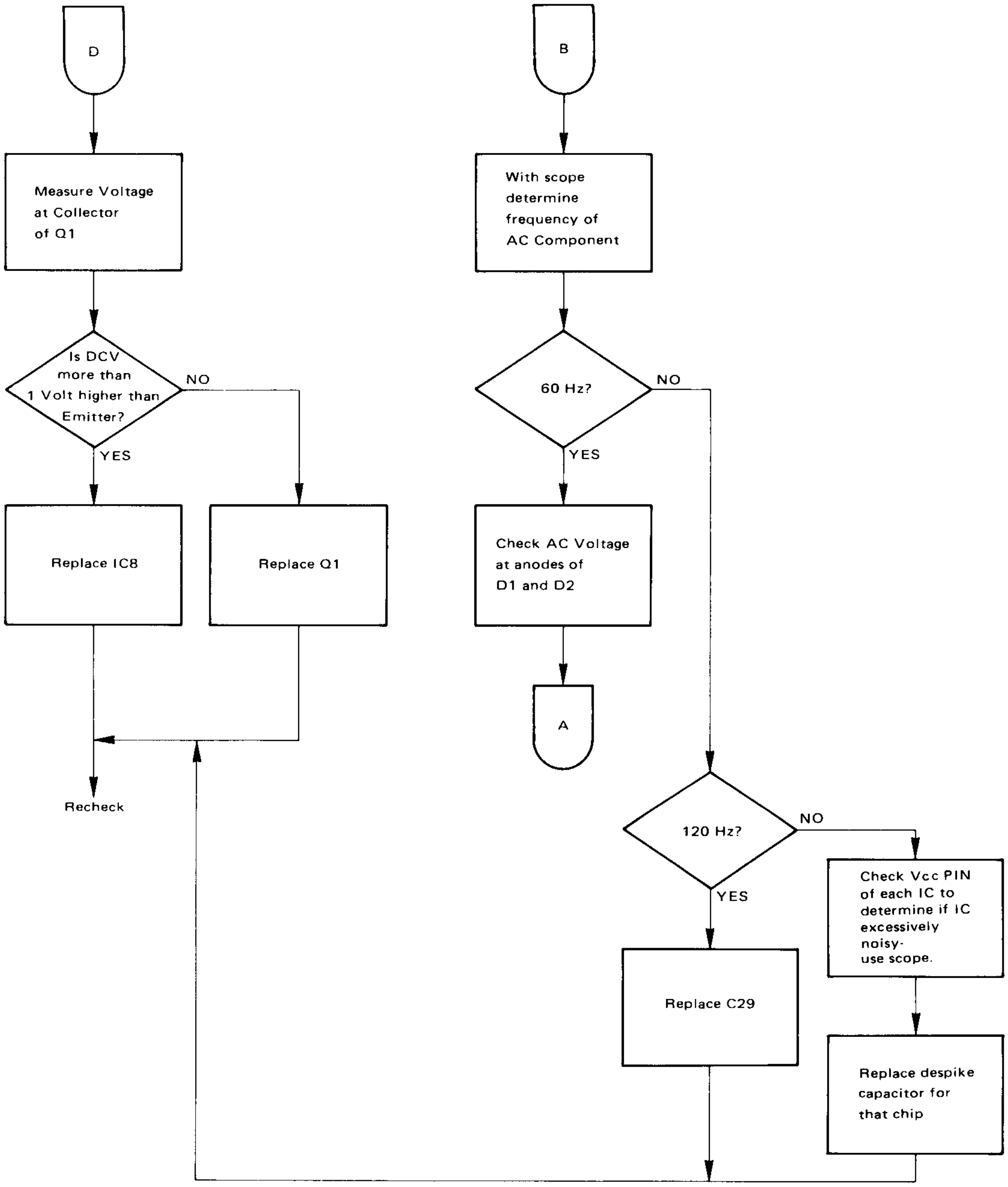
PAL Version

Note: Check to Confirm the voltage of AC outlet is 240V, 50Hz.

*1 Refer to Waveform 10
*2 Refer to Waveform 12B
*3 Refer to Waveform 12A
*4 Refer to Waveform 11



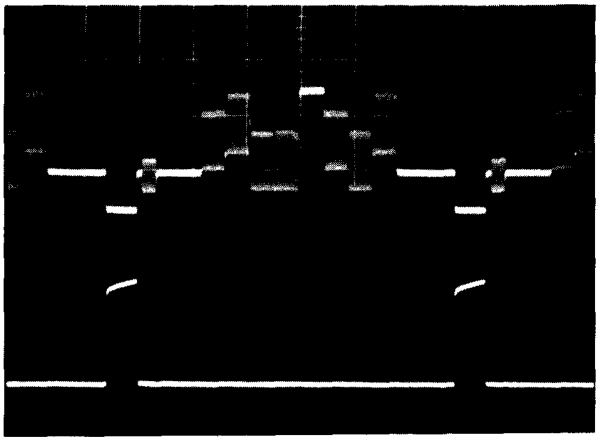

C
*4
Check DC Voltage at Collector of Q1
Voltage at least 8VDC ?
NO
YES
Check AC Voltage at anodes of D1 & D2
A
Measure DCV across R19
ACV≧8VAC?
NO
YES
≦150 mV?
NO
YES
Overcurrent Locate/replace Short Component
Replace these Diodes
Check AC Voltage at Secondary of T1
Measure DCV at PIN1 of IC8
ACV≧8VAC
NO
YES
>5.3VDC?
NO
YES
Replace SW1
Replace Q1
Replace IC8
Check AC Voltage at T1 primary.
To Recheck
NO
120 Volts?
YES
Check AC Cord and Replace.
Replace T1


D
Measure Voltage at Collector of Q1
Is DCV more than 1 Volt higher than Emitter?
NO
YES
Replace IC8
Replace Q1
Recheck
B
With scope determine frequency of AC Component
60 Hz?
NO
YES
Check AC Voltage at anodes of D1 and D2
A
120 Hz?
NO
YES
Check Vcc PIN of each IC to determine if IC excessively noisy- use scope.
Replace C29
Replace despike capacitor for that chip

6.11 Major Waveforms

NTSC Version

Waveform 1 CVIDEO & HSYNC

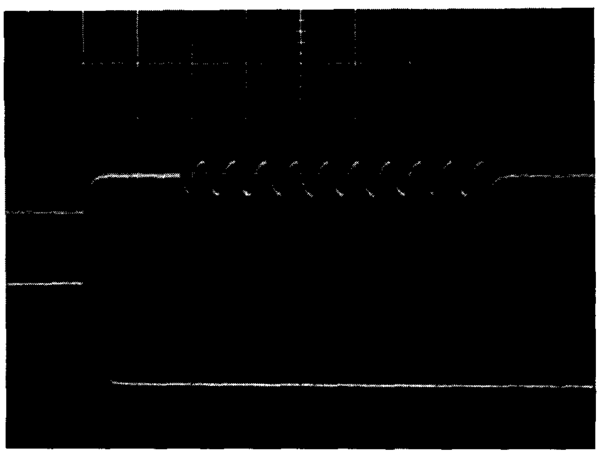


CH A: Composite Video (TP.7)
0.5V/DIV
CH B: HSYNC (Pin 8 of CN3)
2V/DIV

Horizontal: 10μsec/DIV

Trigger: INTERNAL CH A

Waveform 2 Color Burst Signal & HSYNC

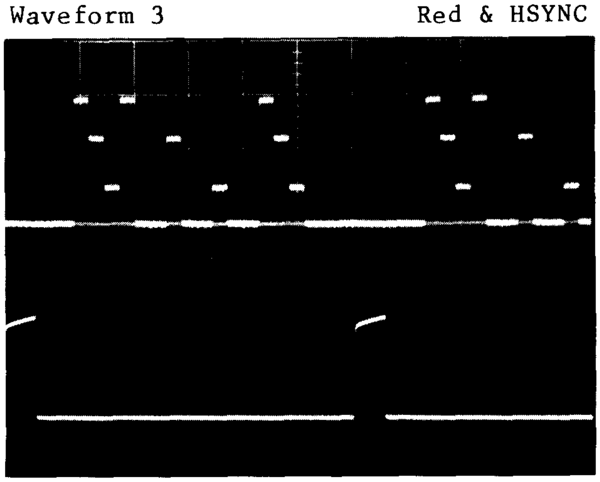


CH A: Color Burst Signal (TP.7)
0.5V/DIV
CH B: HSYNC (Pin 8 of CN3)
2V/DIV

Horizontal: 0.5μsec/DIV

Trigger: INTERNAL CH A

Waveform 3 Red & HSYNC

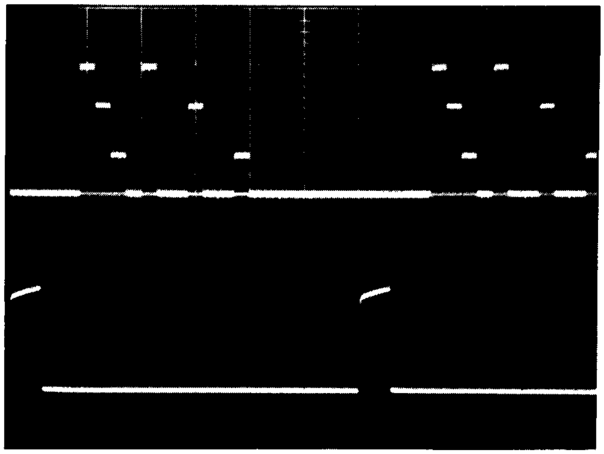


CH A: Red Signal of RGB (TP.8)
0.5V/DIV
CH B: HSYNC (Pin 8 of CN3)
2V/DIV

Horizontal: 10μsec/DIV

Trigger: INTERNAL CH B

Waveform 4 Green & HSYNC

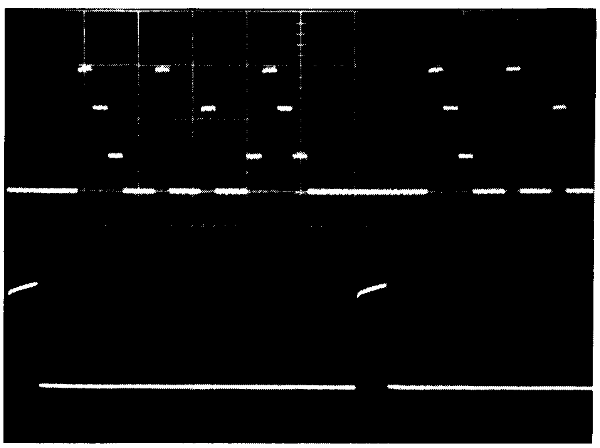


CH A: Green Signal of RGB (TP.9)
0.5V/DIV
CH B: HSYNC
2V/DIV

Horizontal: 10μsec/DIV

Trigger: INTERNAL CH B

Waveform 5 Blue & HSYNC

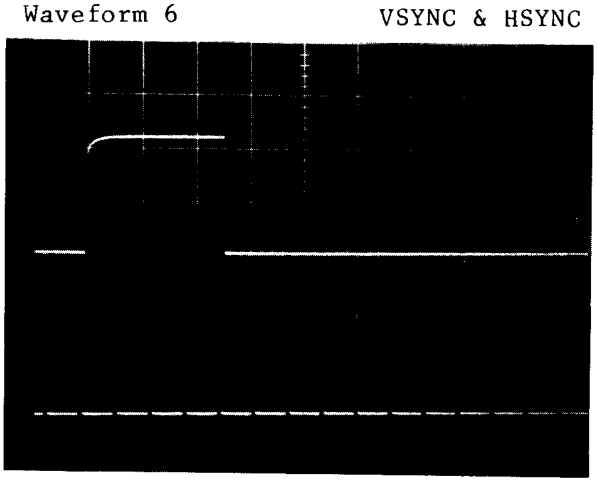


CH A: Blue Signal of RGB (TP.10)
0.5V/DIV
CH B: HSYNC
2V/DIV

Horizontal: 10μsec/DIV

Trigger: INTERNAL CH B

Waveform 6 VSYNC & HSYNC



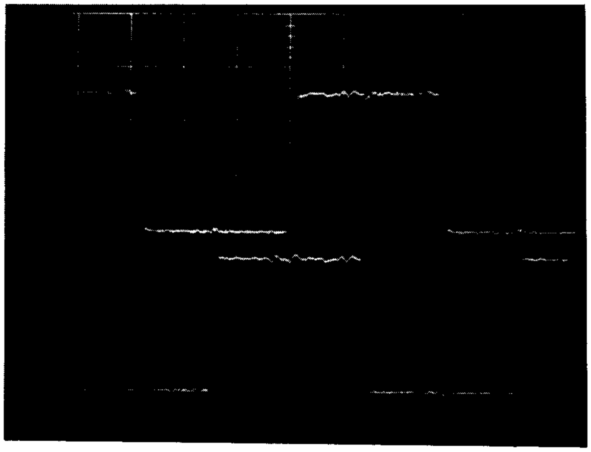
CH A: VSYNC (Pin 9 of CN3)
2V/DIV
CH B: HSYNC
2V/DIV

Horizontal: 0.1msec/DIV

Trigger: CH B INTERNAL

NTSC

Waveform 7 ECLK & QCLK

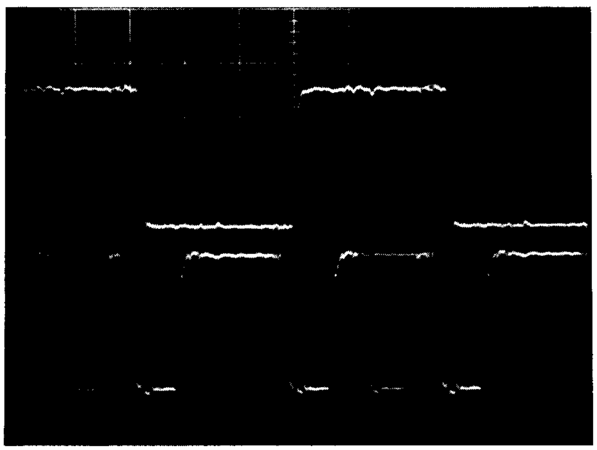


CH A: ECLK (TP.2)
2V/DIV
CH B: QCLK (TP.3)
2V/DIV

Horizontal: 0.2μsec/DIV

Trigger: INTERNAL CH A

Waveform 8 ECLK & RAS*

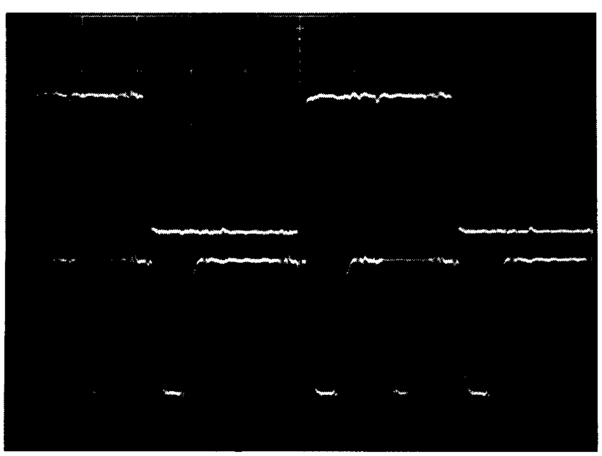


CH A: ECLK (TP.2)
2V/DIV
CH B: RAS* (TP.4)
2V/DIV

Horizontal: 0.2μsec/DIV

Trigger: INTERNAL CH A

Waveform 9 ECLK & CAS*

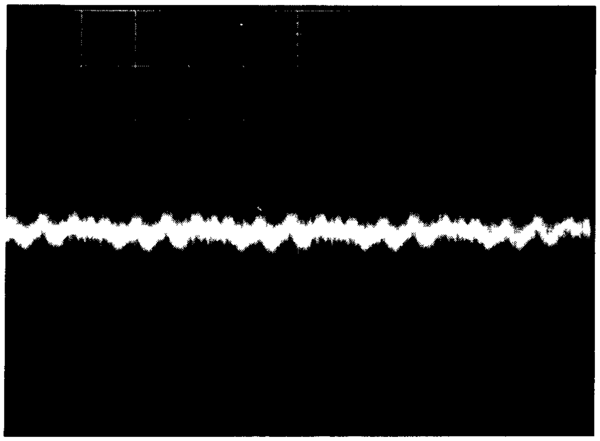


CH A: ECLK (TP.2)
2V/DIV
CH B: CAS* (TP.5)
2V/DIV

Horizontal: 0.2μsec/DIV

Trigger: INTERNAL CH A

Waveform 10 AC Component at +5V

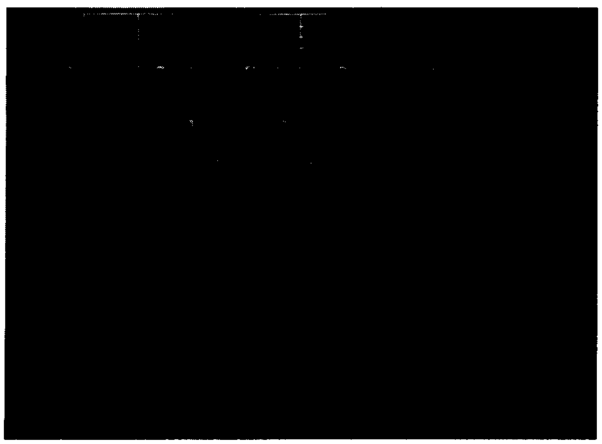


Vertical: 100mV/DIV

Horizontal: 2μsec/DIV

Trigger: INTERNAL

Waveform 11
AC Ripple Positive (Cathode of D1)
& Negative (Anode of D3)

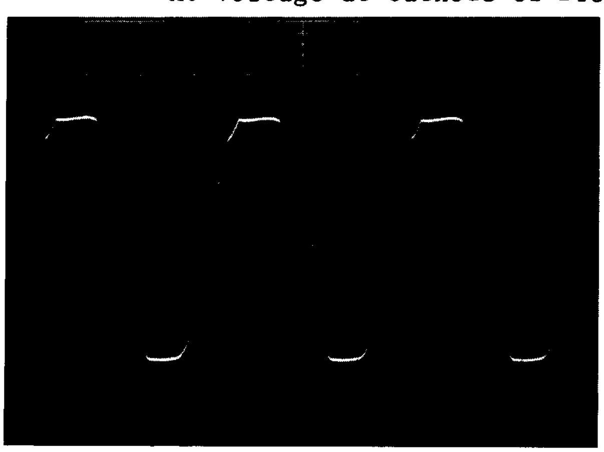


CH A: AC Ripple (Cathode of D1)
0.5V/DIV
CH B: AC Ripple (Anode of D3)
0.2V/DIV

Horizontal: 5msec/DIV

Trigger: INTERNAL CH A

Waveform 12A
AC Voltage at Cathode of D13



Vertical: 5V/DIV

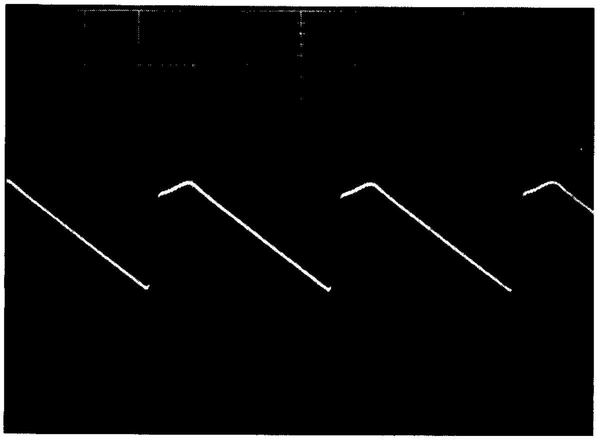
Horizontal: 5msec/DIV

Trigger: INTERNAL

NTSC

Waveform 12B

AC Ripple at Cathode of D14

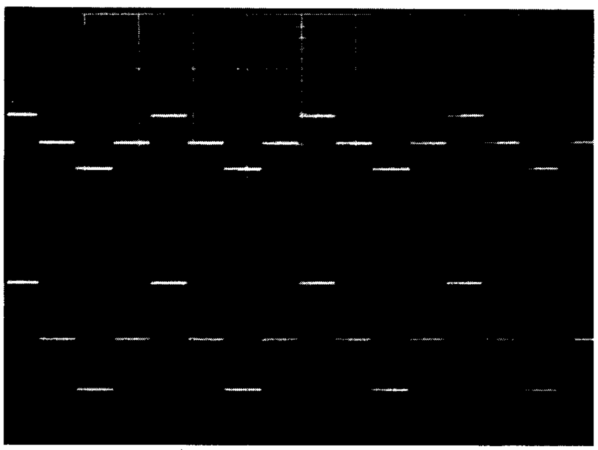


Vertical: 1V/DIV

Horizontal: 5msec/DIV

Trigger: INTERNAL

Waveform 13 SOUND OUT

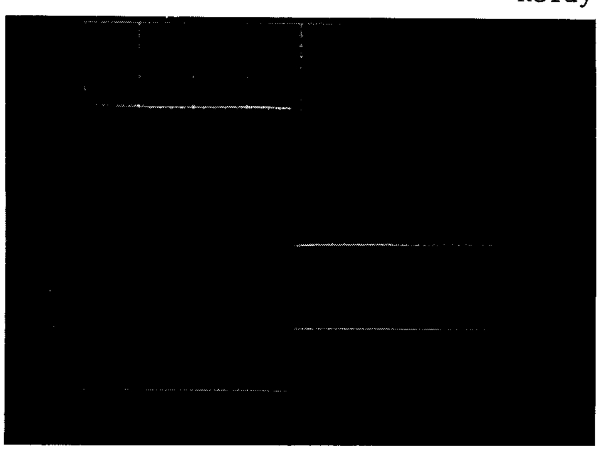


CH A: Pin 17 of IC7
1V/DIV
CH B: Pin 1 of IC7
2V/DIV

Horizontal: 0.5msec/DIV

Trigger: INTERNAL CH A

Waveform 14 Relay

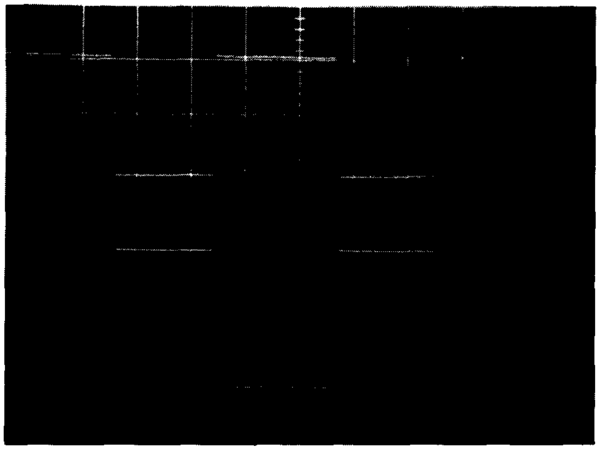


CH A: Pin 9 of IC8
2V/DIV
CH B: Pin 39 of IC4
2V/DIV

Horizontal: 10msec/DIV

Trigger: INTERNAL CH A

Waveform 15



CH A: Pin 12 of IC8
5V/DIV
CH B: Pin 3 of IC4
2V/DIV

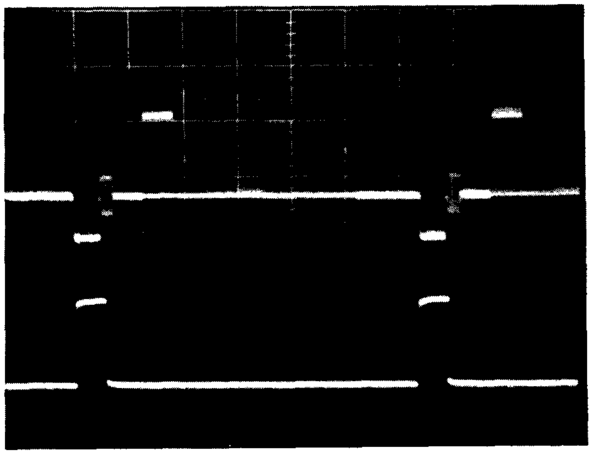
Horizontal: 5msec/DIV

Trigger: INTERNAL CH A

PAL

PAL Version

Waveform 1 CVIDEO & HSYNC

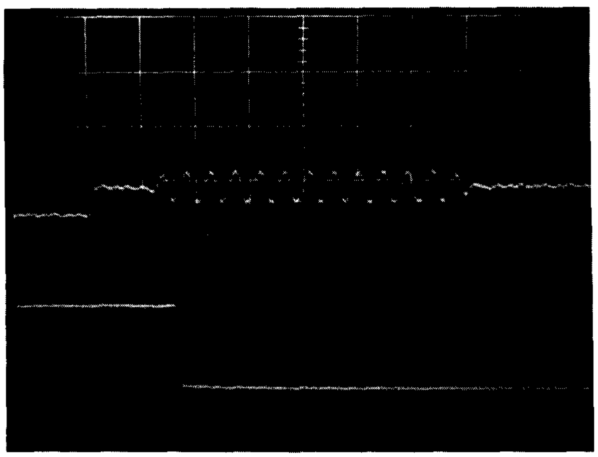


CH A: Composite Video (TP.7)
0.5V/DIV
CH B: HSYNC (Pin 8 of CN3)
2V/DIV

Horizontal: 10μsec/DIV

Trigger: INTERNAL CH A

Waveform 2 Color Burst Signal & HSYNC

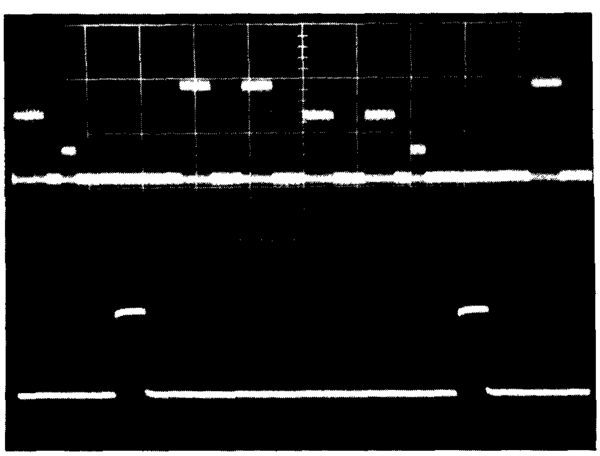


CH A: Color Burst Signal (TP.7)
0.5V/DIV
CH B: HSYNC (Pin 8 of CN3)
2V/DIV

Horizontal: 0.5μsec/DIV

Trigger: INTERNAL CH A

Waveform 3 Red & HSYNC

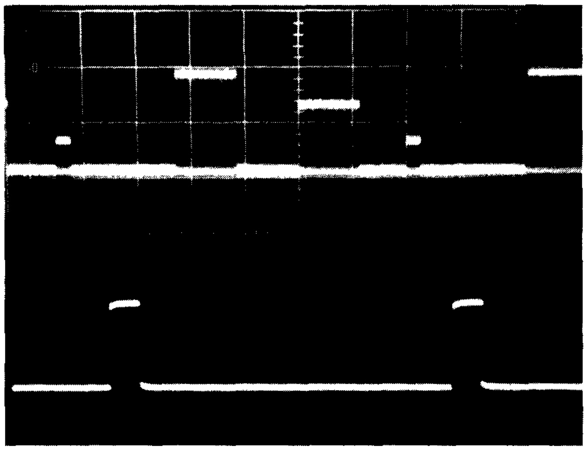


CH A: Red Signal of RGB (TP.8)
0.5V/DIV
CH B: HSYNC (Pin 8 of CN3)
2V/DIV

Horizontal: 10μsec/DIV

Trigger: INTERNAL CH B

Waveform 4 Green & HSYNC

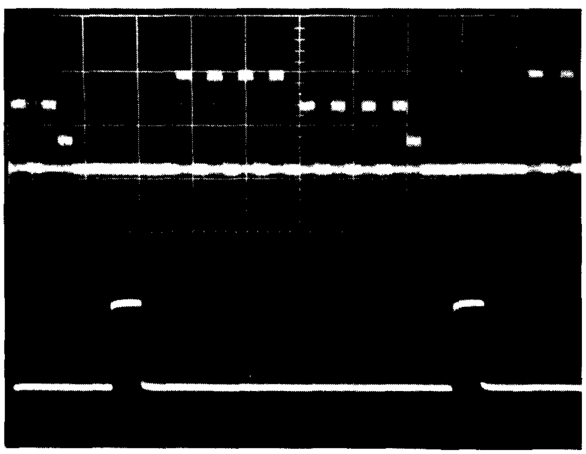


CH A: Green Signal of RGB (TP.9)
0.5V/DIV
CH B: HSYNC
2V/DIV

Horizontal: 10μsec/DIV

Trigger: INTERNAL CH B

Waveform 5 Blue & HSYNC

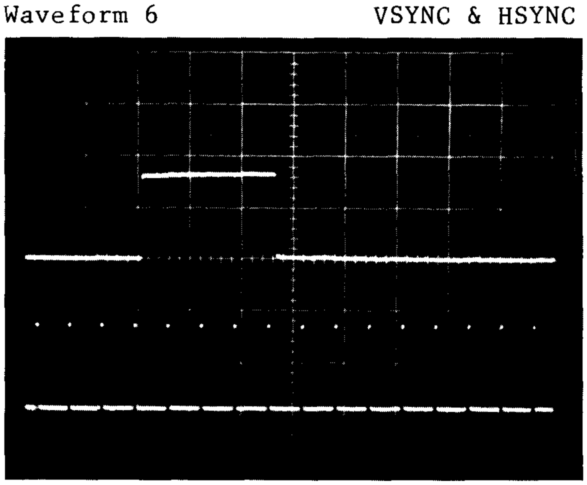


CH A: Blue Signal of RGB (TP.10)
0.5V/DIV
CH B: HSYNC
2V/DIV

Horizontal: 10μsec/DIV

Trigger: INTERNAL CH B

Waveform 6 VSYNC & HSYNC



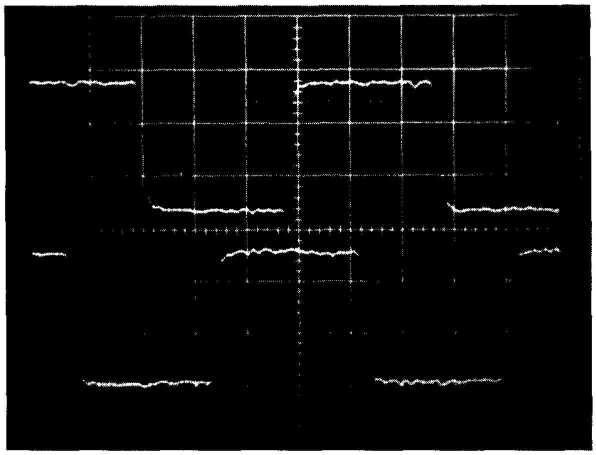
CH A: VSYNC (Pin 9 of CN3)
2V/DIV
CH B: HSYNC
2V/DIV

Horizontal: 0.1msec/DIV

Trigger: CH B INTERNAL

PAL

Waveform 7 ECLK & QCLK

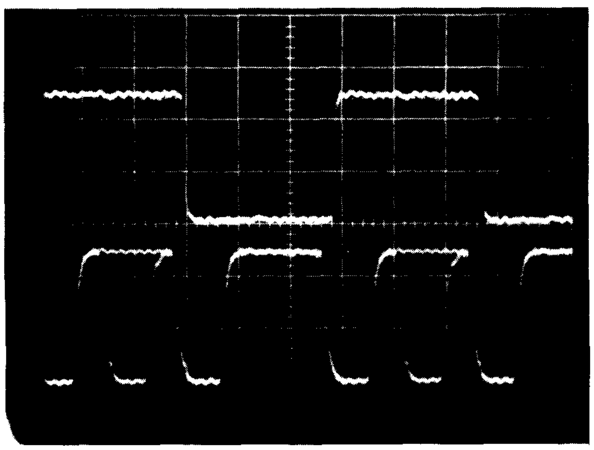


CH A: ECLK (TP.2)
2V/DIV
CH B: QCLK (TP.3)
2V/DIV

Horizontal: 0.2μsec/DIV

Trigger: INTERNAL CH A

Waveform 8 ECLK & RAS*

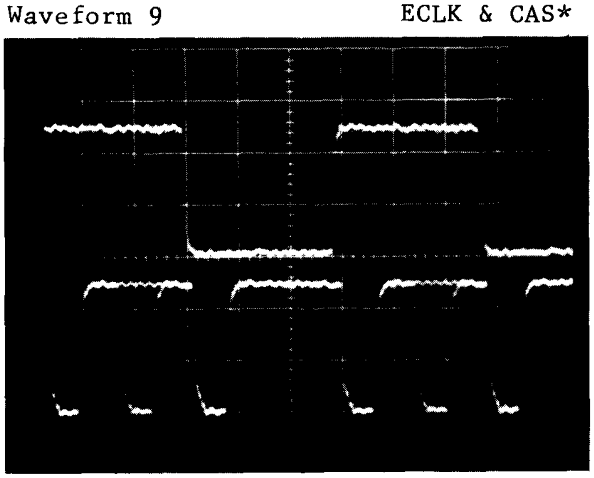


CH A: ECLK (TP.2)
2V/DIV
CH B: RAS* (TP.4)
2V/DIV

Horizontal: 0.2μsec/DIV

Trigger: INTERNAL CH A

Waveform 9 ECLK & CAS*

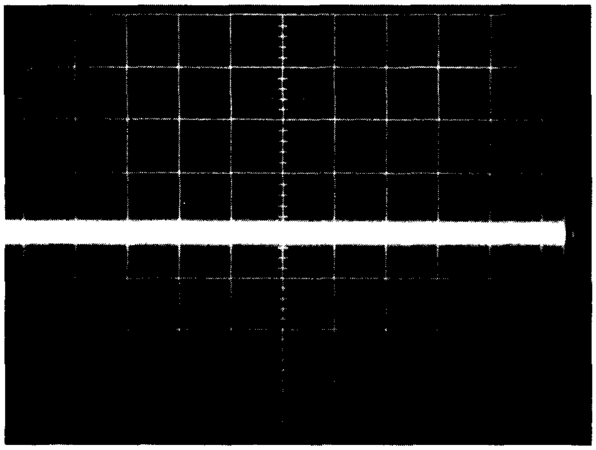


CH A: ECLK (TP.2)
2V/DIV
CH B: CAS* (TP.5)
2V/DIV

Horizontal: 0.2μsec/DIV

Trigger: INTERNAL CH A

Waveform 10 AC Component at +5V



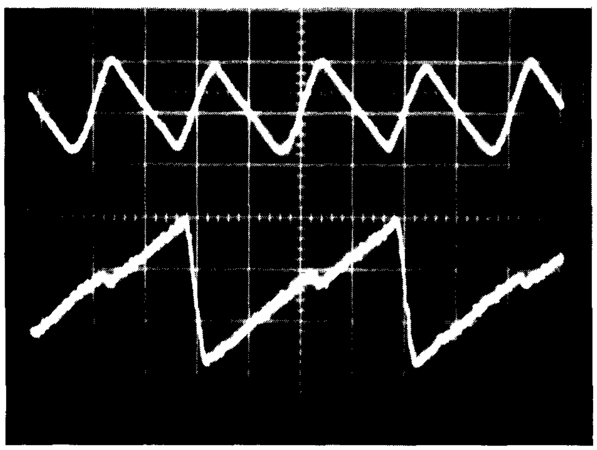
Vertical: 100mV/DIV

Horizontal: 2μsec/DIV

Trigger: INTERNAL

Waveform 11

AC Ripple Positive (Cathode of D1)
& Negative (Anode of D3)



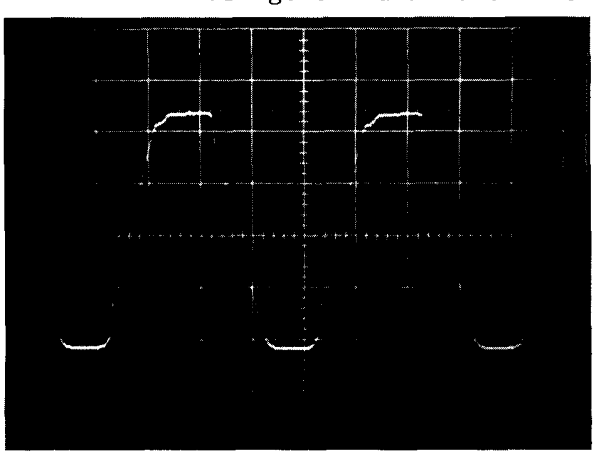
CH A: AC Ripple (Cathode of D1)
0.5V/DIV
CH B: AC Ripple (Anode of D3)
0.2V/DIV

Horizontal: 5msec/DIV

Trigger: INTERNAL CH A

Waveform 12A

AC Voltage at Cathode of D13



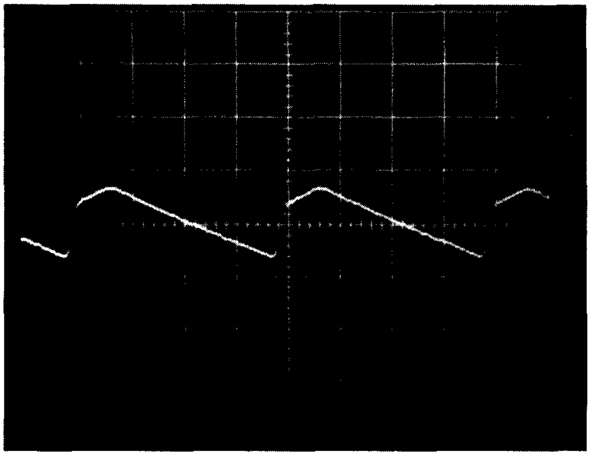
Vertical: 5V/DIV

Horizontal: 5msec/DIV

Trigger: INTERNAL

Waveform 12B

AC Ripple at Cathode of D14

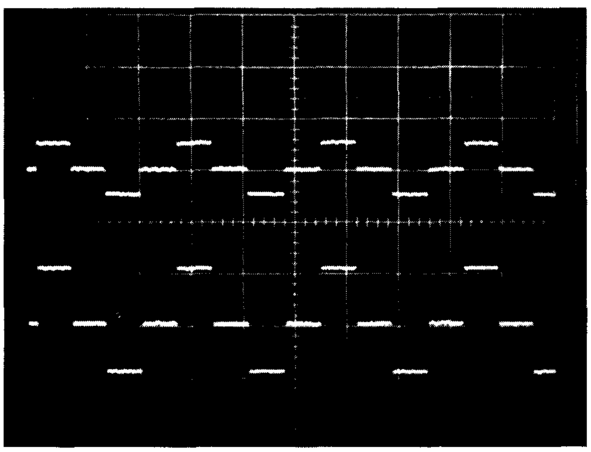


Vertical: 1V/DIV

Horizontal: 5msec/DIV

Trigger: INTERNAL

Waveform 13 SOUND OUT



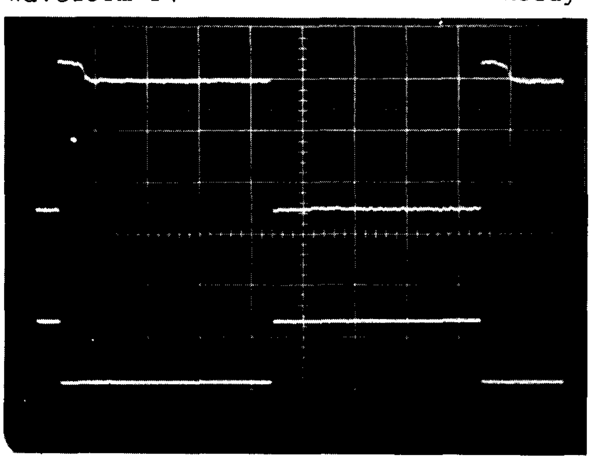
CH A: Pin 17 of IC7
1V/DIV

CH B: Pin 1 of IC7
2V/DIV

Horizontal: 0.5msec/DIV

Trigger: INTERNAL CH A

Waveform 14 Relay



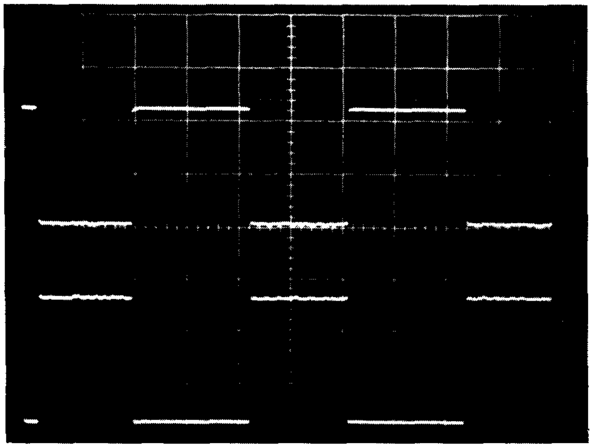
CH A: Pin 9 of IC8
2V/DIV

CH B: Pin 39 of IC4
2V/DIV

Horizontal: 10msec/DIV

Trigger: INTERNAL CH A

Waveform 15

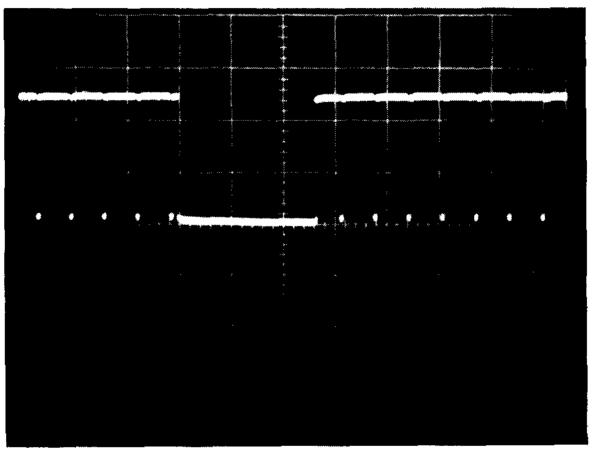


CH A: Pin 12 of IC8
5V/DIV
CH B: Pin 3 of IC4
2V/DIV

Horizontal: 5msec/DIV

Trigger: INTERNAL CH A

Waveform 16



Collector of Q11

Horizontal: 0.1 msec/DIV

Vertical: 2V/DIV

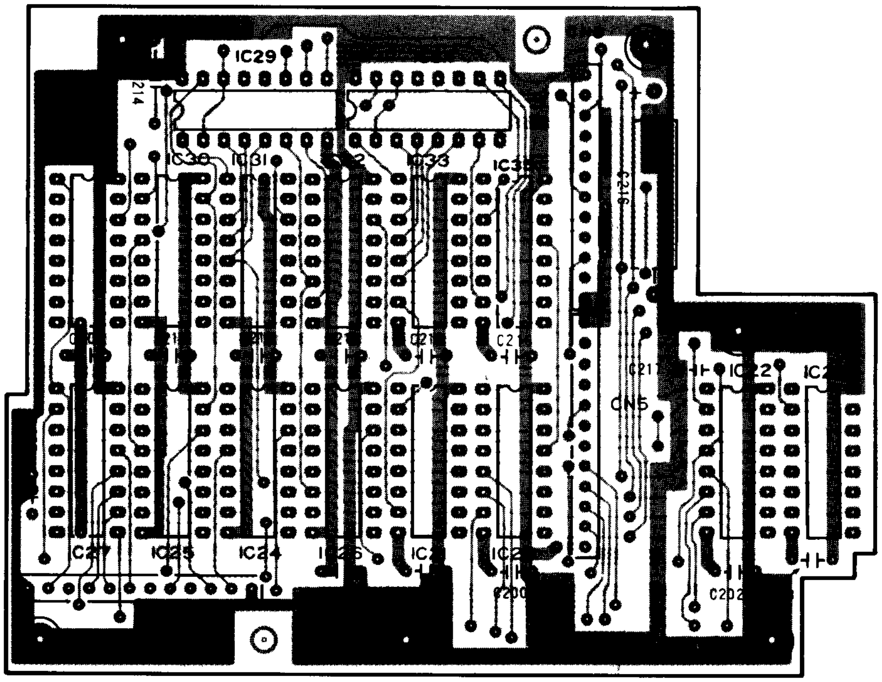
Trigger: INTERNAL

SECTION VII

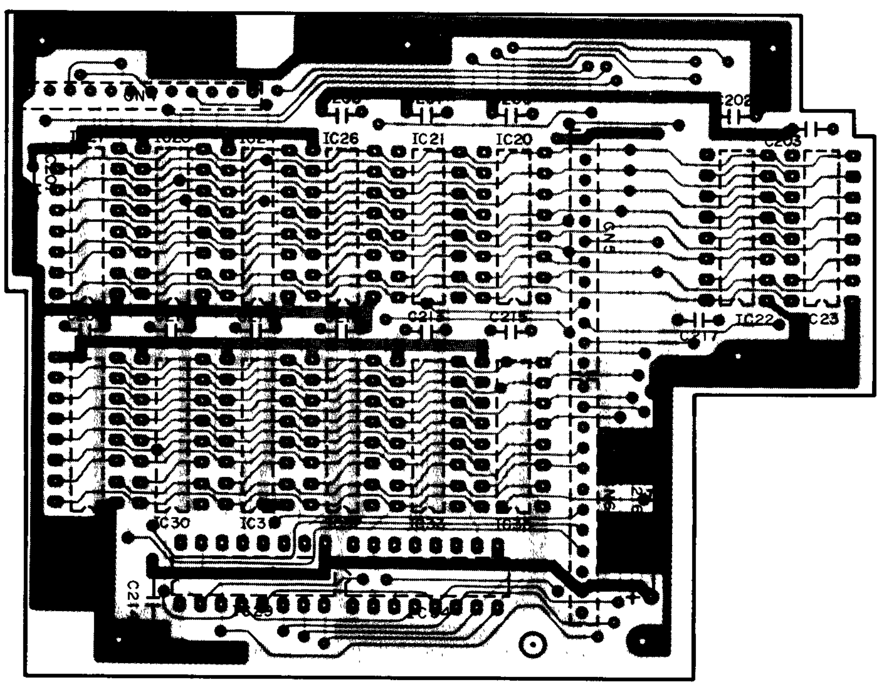
512K Expansion RAM Card

PCB VIEWS

TOP VIEW



BOTTOM VIEW



ELECTRICAL PARTS LIST

CAPACITORS

Ref. No.	Description	RS Part No.	Mfr's Part No.
C200-203	M-Plastic 0.1μF 50V +-5% or		CFQMK104JL or
	M-Plastic 0.1μF 63V +-10%		CFSSLA01KQ
C204/205	Not Used		
C206-208	M-Plastic 0.1μF 50V +-5% or		CFQMK104JL or
	M-Plastic 0.1μF 63V +-10%		CFSSLA01KQ
C209	Not Used		
C210-213	M-Plastic 0.1μF 50V +-5% or		CFQMK104JL or
	M-Plastic 0.1μF 63V +-10%		CFSSLA01KQ
C214	Ceramic 0.033μF 12V +-30%		CGBUF333NT
C215	M-Plastic 0.1μF 50V +-5% or		CFQMK104JL or
	M-Plastic 0.1μF 63V +-10%		CFSSLA01KQ
C216	Electrolytic 100μF 16V +-20%		CEAAG107M*
C217	Ceramic 27μF 50V +-5%		CCJBK270J*

CONNECTORS

Ref. No.	Description	RS Part No.	Mfr's Part No.
CN4-6	Pin, To Main PCB		194113590A

ICs

Ref. No.	Description	RS Part No.	Mfr's Part No.
IC20-35	μPD41256C-15 N-MOS Memory		SIPD256-15

MISCELLANEOUS

Ref. No.	Description	RS Part No.	Mfr's Part No.
	RAM Card PCB Ass'y		U-32056
	Socket, IC 16-Pin or		195110400A or
	C8816-41 or		195110240A or
	DILB16P-8J		195110140A
	Sheet, Shield PVC+AL FOIL		473311070A
	Rivet, SK51 or		HARRA003SN or
	Rivet, SUS301		HARRA003UT
	Holder, MSP-10N		413101410A

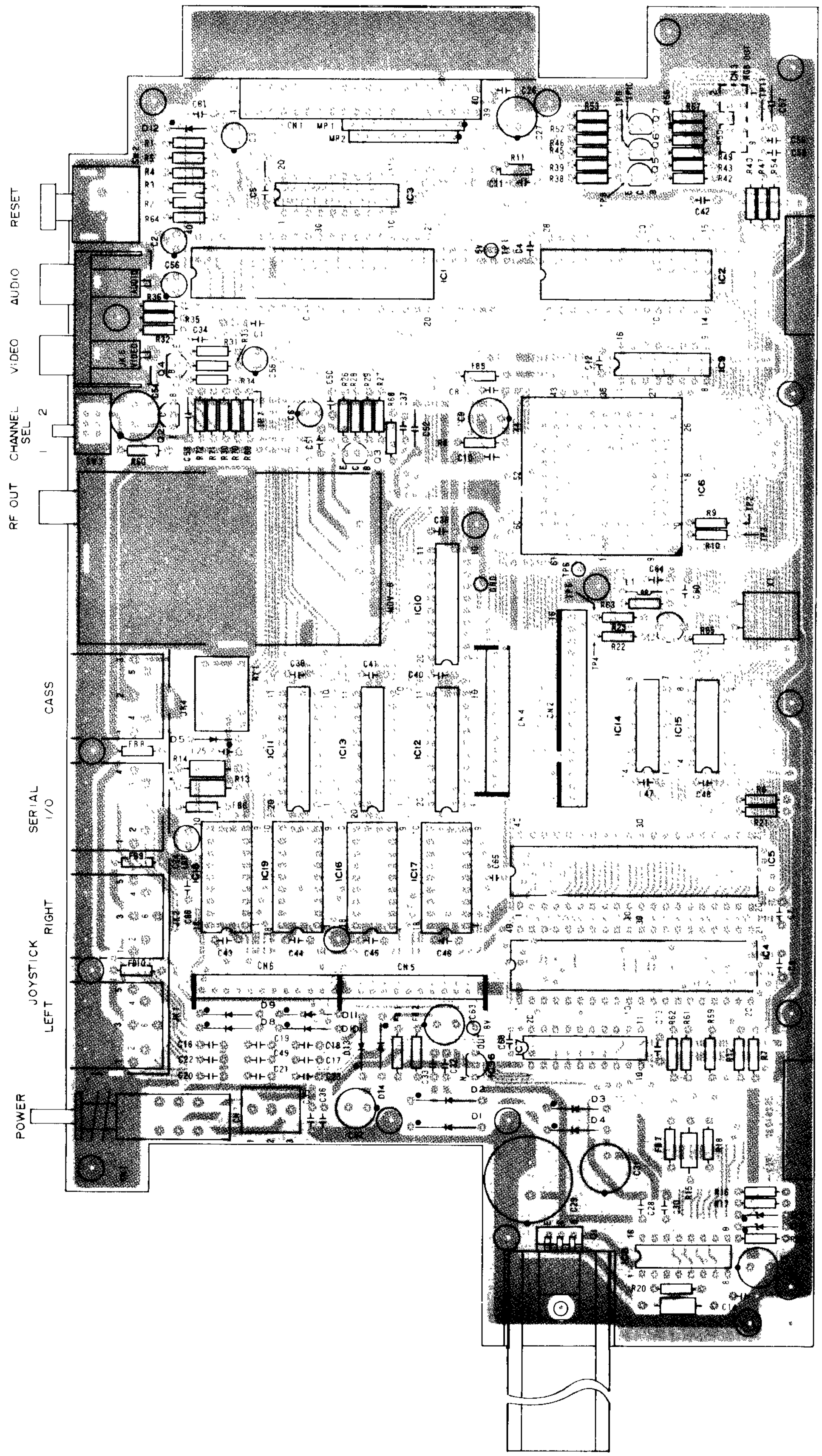
SECTION VIII

NTSC Version

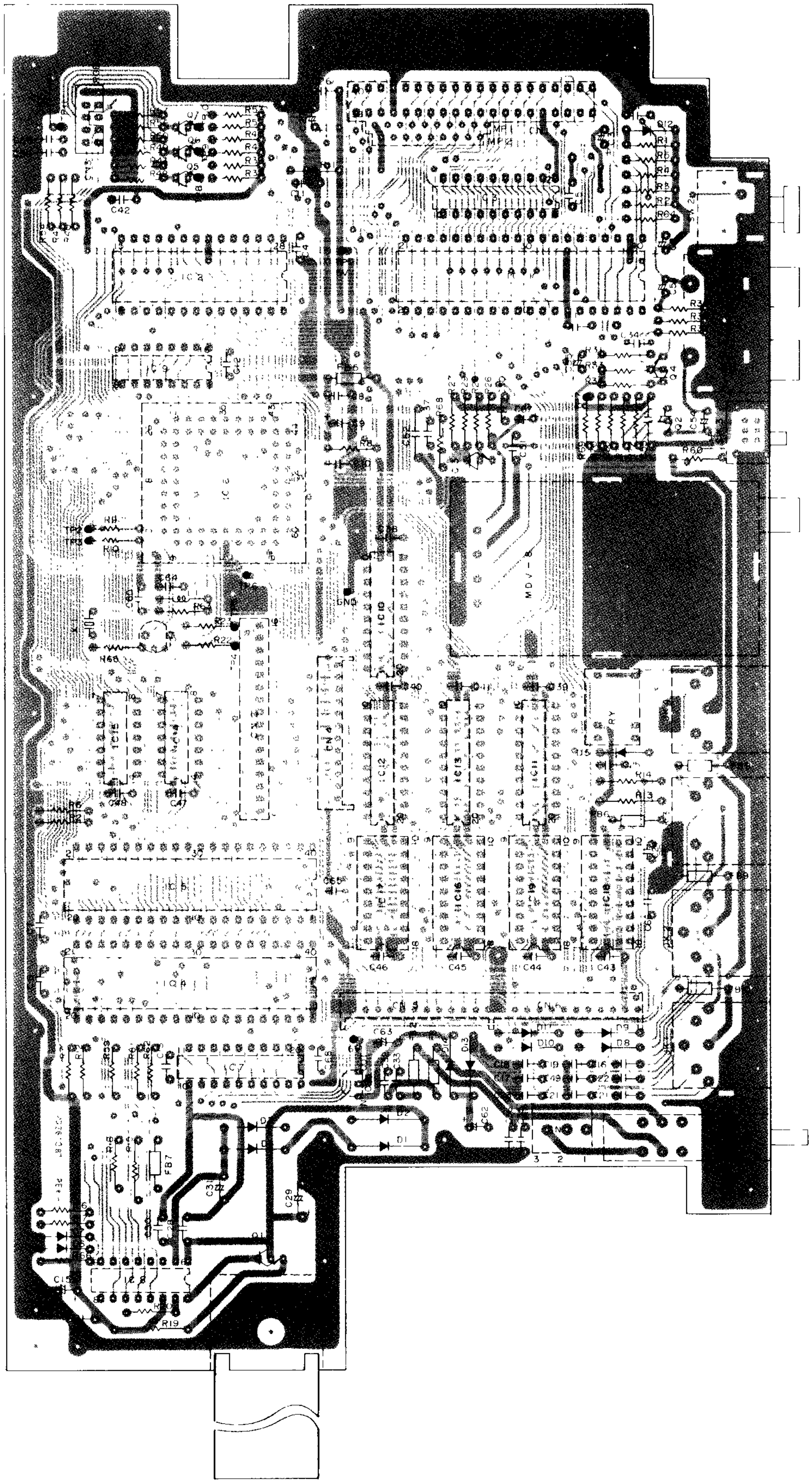
NTSC

PCB VIEWS

TOP VIEW



BOTTOM VIEW



ELECTRICAL PARTS LIST

CAPACITORS

Ref. No.	Description				RS Part No.	Mfr's Part No.
C1	M-Plastic	0.1µF	50V	+-5% or	CC-104JLBY	CFQMK104JL or
	M-Plastic	0.1µF	63V	+-10% or		CFSSLA01KQ or
	Ceramic	0.1µF	50V+80-20%			CJRPK104ZM
C2	Electrolytic	10µF	25V	+-20%	CC-106MFBA	CEACI106M*
C3	Electrolytic	1µF	50V	+-20%	CC-105MJBA	CEACK105M*
C4	M-Plastic	0.1µF	50V	+-5% or		CFQMK104JL or
	M-Plastic	0.1µF	63V	+-10% or		CFSSLA01KQ or
	Ceramic	0.1µF	50V+80-20%			CJRPK104ZM
C5	Ceramic	0.033µF	12V	+-30%		CGBUF333NT
C6-8	M-Plastic	0.1µF	50V	+-5% or		CFQMK104JL or
	M-Plastic	0.1µF	63V	+-10% or		CFSSLA01KQ or
	Ceramic	0.1µF	50V+80-20%			CJRPK104ZM
C9	Electrolytic	100µF	16V	+-20%		CEACG107M*
C10/11	Ceramic SL	39pF	50V	+-5%	CF-2433	CCJVK390J*
C12-14	M-Plastic	0.1µF	50V	+-5% or	CC-104JLBY	CFQMK104JL or
	M-Plastic	0.1µF	63V	+-10% or		CFSSLA01KQ or
	Ceramic	0.1µF	50V+80-20%			CJRPK104ZM
C15	Electrolytic	100µF	16V	+-20%	CC-107MDCA	CEACG107M*
C16/17	Ceramic	0.022µF	50V+80-20%		CC-223JJBC	CKKPK223Z*
C18/19	Mylar*	1800pF	50V	+-10%	CC-182JJBM	CQQMK182K* or
					CC-182JJBM	CQQMK182KL
C20/21	Ceramic	0.022µF	50V+80-20%		CC-223JJBC	CKKPK223Z*
C22/23	Mylar	1800pF	50V	+-10%	CC-182JJBM	CQQMK182K* or
						CQQMK182KL
C24	Elec NP/LN	10µF	25V	+-20%	CF-2408	CEPCI106M*
C25	Ceramic	0.022µF	50V+80-20%		CC-223JJBC	CKJPK223Z*
C26	M-Plastic	0.1µF	50V	+-5% or	CC-104JLBY	CFQMK104JL or
	M-Plastic	0.1µF	63V	+-10% or		CFSSLA01KQ or
	Ceramic	0.1µF	50V+80-20%			CJRPK104ZM
C27	Electrolytic	100µF	16V	+-20%	CC-107MDCA	CEACG107M*
C28	M-Plastic	0.1µF	50V	+-5% or	CC-104JLBY	CFQMK104JL or
	M-Plastic	0.1µF	63V	+-10% or		CFSSLA01KQ or
	Ceramic	0.1µF	50V+80-20%			CJRPK104ZM
C29	Electrolytic	4700µF	16V	+-20%	CC-478MDCA	CEACG478M*
C30	M-Plastic	0.1µF	50V	+-5% or	CC-104JLBY	CFQMK104JL or
	M-Plastic	0.1µF	63V	+-10% or		CFSSLA01KQ or
	Ceramic	0.1µF	50V+80-20%			CJRPK104ZM
C31	Electrolytic	220µF	16V	+-20%	CC-227MDCA	CEACG227M*
C32/33	Ceramic	0.022µF	50V+80-20%		CC-223JJBC	CKJPK223Z*
C34	Ceramic	100pF	50V	+-5%		CCJVK101J*
C35/36	Ceramic	0.022µF	50V+80-20%		CC-223JJBC	CKKPK223Z*
C37	Ceramic SL	39pF	50V	+-5%		CCJVK390J*
C38-41	M-Plastic	0.1µF	50V	+-5% or	CC-104JLBY	CFQMK104JL or
	M-Plastic	0.1µF	63V	+-10% or		CFSSLA01KQ or
	Ceramic	0.1µF	50V+80-20%			CJRPK104ZM
C42-48	M-Plastic	0.1µF	50V	+-5% or	CC-104JLBY	CFQMK104JL or
	M-Plastic	0.1µF	63V	+-10% or		CFSSLA01KQ or
	Ceramic	0.1µF	50V+80-20%			CJRPK104ZM
C49	Ceramic	0.022µF	50V+80-20%		CC-223JJBC	CKKPK223Z*

NOTE: *Mylar is a registered trademark of E. I. Du Pont de Nemours and Company.

Ref. No.	Description	RS Part No.	Mfr's Part No.
C50/51	M-Plastic 0.1μF 50V +-5% or	CC-104JLBY	CFQMK104JL or
	M-Plastic 0.1μF 63V +-10% or		CFSSLA01KQ or
	Ceramic 0.1μF 50V+80-20%		CJRPK104ZM
C52/53	Ceramic 0.033μF 12V +-30%		CGBUF333NT
C54	Electrolytic 470μF 16V +-20%		CEACG477M*
C55/56	Electrolytic 10μF 25V +-20%	CC-106MFBA	CEACI106M*
C57	Ceramic 0.022μF 16V +-30%		CGBUG223NT
C58/59	Ceramic 1000pF 50V +-5%		CCJVK102J*
C60	Ceramic NPO 33pF 50V +-5%	CF-1300	CCJBK330J*
C61	Ceramic SL 39pF 50V +-5%	CF-2433	CCJVK390J*
C62/63	Electrolytic 220μF 25V +-20%	CC-227MFBA	CECCI227M*
C64	Ceramic NPO 150pF 50V +-5%	CF-2345	CCJBK151J*
C65	Ceramic SL 82pF 50V +-5%		CCJVK820J*
C66	Ceramic 27pF 50V +-5%		CCJVK270J*
C67	Electrolytic 10μF 25V +-20%	CC-106MFBA	CEACI106M*
C68	Mylar 0.01μF 50V +-10%		CQQMK103K*
	COIL		
L1	Inductor 1.8μH	CA-2159	142011310A
	CONNECTORS		
CN1	PCB 40P Cartridge	AJ-7572	194210060A or
			194210140A
CN2	Wire 16P Keyboard	AJ-7567	193910680A or
			193911090A
CN3	Pin RGB 10P	AJ-5116	194112500A
CN4-6	Pin For RAM Option	AJ-7619	194010510A
CN7	Pin 5273-03A		194111250A
	CORES		
FB1/2	Core, Noise		588010060A or
			588010070A or
			588010130A
FB3/4	Not Used		
FB5-10	Core, Noise		588010060A or
			588010070A or
			588010130A
	CRYSTAL		
X1	Crystal, 28.63636MHz Clock OSC	MX-0102	391012220A
	DIODES		
D1/2	Silicon GP20B Rectifier	DX-0847	SDSI00140-
D3/4	Silicon 1N4002 Rectifier or	DX-0206	SDSI00036- or
	SR1K-2 or	DX-0475	SDSI00026- or
	10E1 or	DX-1039	SDSI00003- or
	1N4002	DX-0206	SDSI00007-

Ref. No.	Description	RS Part No.	Mfr's Part No.
D5	Silicon 1S953 Switching or	DX-0259	SDSI00015- or
	1N4148		SDSI00057- or
			SDSI00064-
D6/7	Zener RD3.9E-B or	DX-2323	SZRD3.9EB- or
	RD3.9E-L or		SZRD3.9EL- or
	RD3.9E-N		SZRD3.9EN-
D8-11	Germanium 1KF20-04 Switching	DX-2322	SDGE00012-
D12	Silicon 1S953 Switching or	DX-0259	SDSI00015- or
	1N4148	DX-0022	SDSI00057- or
			SDSI00064-
D13/14	Silicon 1N4002 Rectifier or	DX-0206	SDSI00036- or
	SR1K-2 or	DX-0475	SDSI00026- or
	10E1 or	DX-1039	SDSI00003- or
	1N4002	DX-0206	SDSI00007-
	ICs		
IC1	MC68B09EP MPU N-MOS or	MX-7243	SIMC68B09E or
	MBL68B09E-P-G or		SIBL68B09E or
	HD68B09EP		SIHD68B09E
IC2	μPD27C256D-20 ROM N-MOS or	MX-7263	SIPD256-20 or
	TCC1017(μPD23C256EC)		SICC1017--
IC3	SN74LS245N TTL BUS Transceiver or	MX-6740	SIRNS245N- or
	MB74LS245M or		SIMBS245M- or
	M74LS245P or		SIM-S245P- or
	HD74LS245P		SIHDS245P-
IC4	MC68B21P PIA Select N-MOS or	MX-7260	SIMC68B21- or
	MB8874HM-G or		SIMB74HM-G or
	HD68B21P		SIHD68B21-
IC5	LSC81001P PIA Select N-MOS	MX-7259	SILS81001P
IC6	TCC1014(VC2645QC) PLCC ACVC C-MOS	MX-7261	SICC1014--
IC7	8050526 (SC77526P) Bipola DA-Converter	MX-6202	SISC50526-
IC8	8050527 (SC77527P) Bipola Regulator	MX-6201	SISC50527-
IC9	SN74LS138N TTL Decoder or	AMX-4583	SIRNS138N- or
	MB74LS138M or		SIMBS138M- or
	M74LS138P or		SIM-S138P- or
	HD74LS138P		SIHDS138P-
IC10-12	SN74LS244N TTL Buffer or	AMX-3864	SIRNS244N- or
	MB74LS244M or		SIMBS244M- or
	M74LS244P or		SIM-S244P- or
	HD74LS244P		SIHDS244P-
IC13	SN74LS374N TTL D-Latch or	AMX-3928	SIRNS374N- or
	MB74LS374M or		SIMBS374M- or
	M74LS374P or		SIM-S374P- or
	HD74LS374P		SIHDS374P-
IC14	SN74LS30N TTL 8In Nand or		SIRNS30N-- or
	MB74LS30M or		SIMBS30M-- or
	M74LS30P or		SIM-S30P-- or
	HD74LS30P	MX-6843	SIHDS30P--
IC15	SN74LS04N TTL Inverter or	AMX-3552	SIRNS04N-- or
	MB74LS04M or		SIMBS04M-- or
	M74LS04P or		SIM-S04P-- or
	HD74LS04P		SIHDS04P--

Ref. No.	Description	RS Part No.	Mfr's Part No.
IC16-19	HM50464P-1 or		SIHM464-15 or
	M5M4464P-15 or		SIM-464-15 or
	µPD41464C-15 or		SIPD464-15 or
	µPD41464C-12 or		SIPD464-12 or
	TMS4464-15NL		SITS464-15
IC20-35	Not Used		
IC36	MC78L08ACP Bipola Regulator or	MX-5399	SIMCL08A-- or
	NJM78L08(A)		SINM78L08A
	JACKS		
JK1/2	DIN Joystick	AJ-7566	193410040A or
		AJ-7566	193410070A
JK3	DIN Serial In/Out	AJ-7357	193410020A or
			193410050A
JK4	DIN Cassette In/Out	AJ-7356	193410030A or
			193410060A
JK5	RCA Video/Sound 2P	AJ-2002	192010400A
	RELAY		
RY1	Remote Control On/Off for Cassette	AR-8166	581010140A or
		AR-8166	581010160A or
			581010710A
	RESISTORS		
R1	Carbon 100kohm 1/4W +-5%		RCSQP104J*
R2-8	Carbon 4.7kohm 1/4W +-5%	N-0247EEC	RCSQP472J*
R9/10	Carbon 47 ohm 1/4W +-5%	N-0099EEC	RCSQP470J*
R11	Carbon 4.7kohm 1/4W +-5%	N-0247EEC	RCSQP472J*
R12	Carbon 10kohm 1/4W +-5%	N-0281EEC	RCSQP103J*
R13	Carbon 100 ohm 1/2W +-5%	N-0132EEC	RCSHP101J*
R14	Carbon 220 ohm 1/2W +-5%	N-0149EEC	RCSHP221J*
R15	Carbon 270 ohm 1/2W +-5%	N-0155EEC	RCSHP271J*
R16/17	Carbon 1.0kohm 1/4W +-5%	N-0196EEC	RCSQP102J*
R18	Carbon 510 ohm 1/4W +-5%	N-0173EEC	RCSQP511J*
R19	M-Film 0.1 ohm 1W +-5%	N-0063EGE	RM01HR10J*
R20	Carbon 51 ohm 1/4W +-5%	N-0103EEC	RCSQP510J*
R21	Carbon 4.7kohm 1/4W +-5%	N-0247EEC	RCSQP472J*
R22	Carbon 120 ohm 1/4W +-5%		RCSQP121J*
R23	Carbon 82 ohm 1/4W +-5%		RCSQP820J*
R24/25	Not used		
R26	Carbon 2.2kohm 1/4W +-5%	N-0216EEC	RCSQP222J*
R27	Carbon 1.5kohm 1/4W +-5%		RCSQP152J*
R28	Carbon 10 ohm 1/4W +-5%	N-0063EEC	RCSQP100J*
R29	Carbon 3.9kohm 1/4W +-5%		RCSQP392J*
R30	Carbon 100 ohm 1/4W +-5%	N-0132EEC	RCSQP101J*
R31	Carbon 39kohm 1/4W +-5%		RCSQP393J*
R32	Carbon 20kohm 1/4W +-5%	N-0306EEC	RCSQP203J*

Ref. No.	Description	RS Part No.	Mfr's Part No.
R33	Carbon 220kohm 1/4W +-5%	N-0396EEC	RCSQP224J*
R34	Carbon 100 ohm 1/4W +-5%		RCSQP101J*
R35	Carbon 220kohm 1/4W +-5%	N-0396EEC	RCSQP224J*
R36	Carbon 1.0kohm 1/4W +-5%		RCSQP102J*
R37	Not used		
R38	Carbon 3.0kohm 1/4W +-5%		RCSQP302J*
R39	Carbon 10 ohm 1/4W +-5%	N-0063EEC	RCSQP100J*
R40	Carbon 1.0kohm 1/4W +-5%	N-0196EEC	RCSQP102J*
R41	Not used		
R42	Carbon 2.0kohm 1/4W +-5%		RCSQP202J*
R43	Carbon 120 ohm 1/4W +-5%	N-0136EEC	RCSQP121J*
R44	Not used		
R45	Carbon 3.0kohm 1/4W +-5%		RCSQP302J*
R46	Carbon 10 ohm 1/4W +-5%	N-0063EEC	RCSQP100J*
R47	Carbon 1.0kohm 1/4W +-5%	N-0196EEC	RCSQP102J*
R48	Not used		
R49	Carbon 2.0kohm 1/4W +-5%		RCSQP202J*
R50	Carbon 120 ohm 1/4W +-5%	N-0136EEC	RCSQP121J*
R51	Not used		
R52	Carbon 3.0kohm 1/4W +-5%		RCSQP302J*
R53	Carbon 10 ohm 1/4W +-5%	N-0063EEC	RCSQP100J*
R54	Carbon 1.0kohm 1/4W +-5%	N-0196EEC	RCSQP102J*
R55	Not used		
R56	Carbon 2.0kohm 1/4W +-5%		RCSQP202J*
R57	Carbon 120 ohm 1/4W +-5%	N-0136EEC	RCSQP121J*
R58	Not Used		
R59	Carbon 4.7kohm 1/4W +-5%	N-0247EEC	RCSQP472J*
R60	Carbon 100 ohm 1/4W +-5%	N-0132EEC	RCSQP101J*
R61/62	Carbon 4.7kohm 1/4W +-5%	N-0247EEC	RCSQP472J*
R63	Carbon 150 ohm 1/4W +-5%	N-0142EEC	RCSQP151J*
R64	Carbon 47 ohm 1/4W +-5%	N-0099EEC	RCSQP470J*
R65	Carbon 1Mohm 1/4W +-5%	N-0445EEC	RCSQP105J*
R66	Carbon 7.5kohm 1/4W +-5%	N-0196EEC	RCSQP752J*
R67	Not Used		
R68	Carbon 10 ohm 1/4W +-5%		RCSQP100J*
R69	Carbon 100 ohm 1/4W +-5%		RCSQP101J*
R70	Carbon 470 ohm 1/4W +-5%		RCSQP471J*
R71	Carbon 10 ohm 1/4W +-5%		RCSQP100J*
R72	Carbon 120 ohm 1/4W +-5%		RCSQP121J*
	RESISTOR-BLOCKS		
MP1	RGLD9X472J		522110530A
MP2	RGLD8X472J		522110520A
	SWITCHES		
SW1	Push Power	AS-2900	182110240A
SW2	Key Reset	AS-2849	187010040A
SW3	Slide Channel Select	AS-3016	183111400A

Ref. No.	Description	RS Part No.	Mfr's Part No.
	TRANSFORMER		
T1	Power EI54 120V US/CA	ATA-0027	10102601SA
	TRANSISTORS		
Q1	KTD880(Y) NPN Regulator or	2SD-880Y	STKD880--Y or
	KTD880(GR)		STKD880--G
Q2/Q3	2SC945(P) NPN Buffer Amp or	2SC-945P	ST2C945--P or
	LC945(P)		STLC945--P
Q4	MPSA13 PNP Amp	MX-3293	STMS-A13--
Q5-7	2SC945(P) NPN Buffer Amp or	2SC-945P	ST2C945--P or
	LC945(P)		STLC945--P
	TRIMMER CAPACITOR		
TC1	Capacitor F-Adjust	AC-0988	154010240A

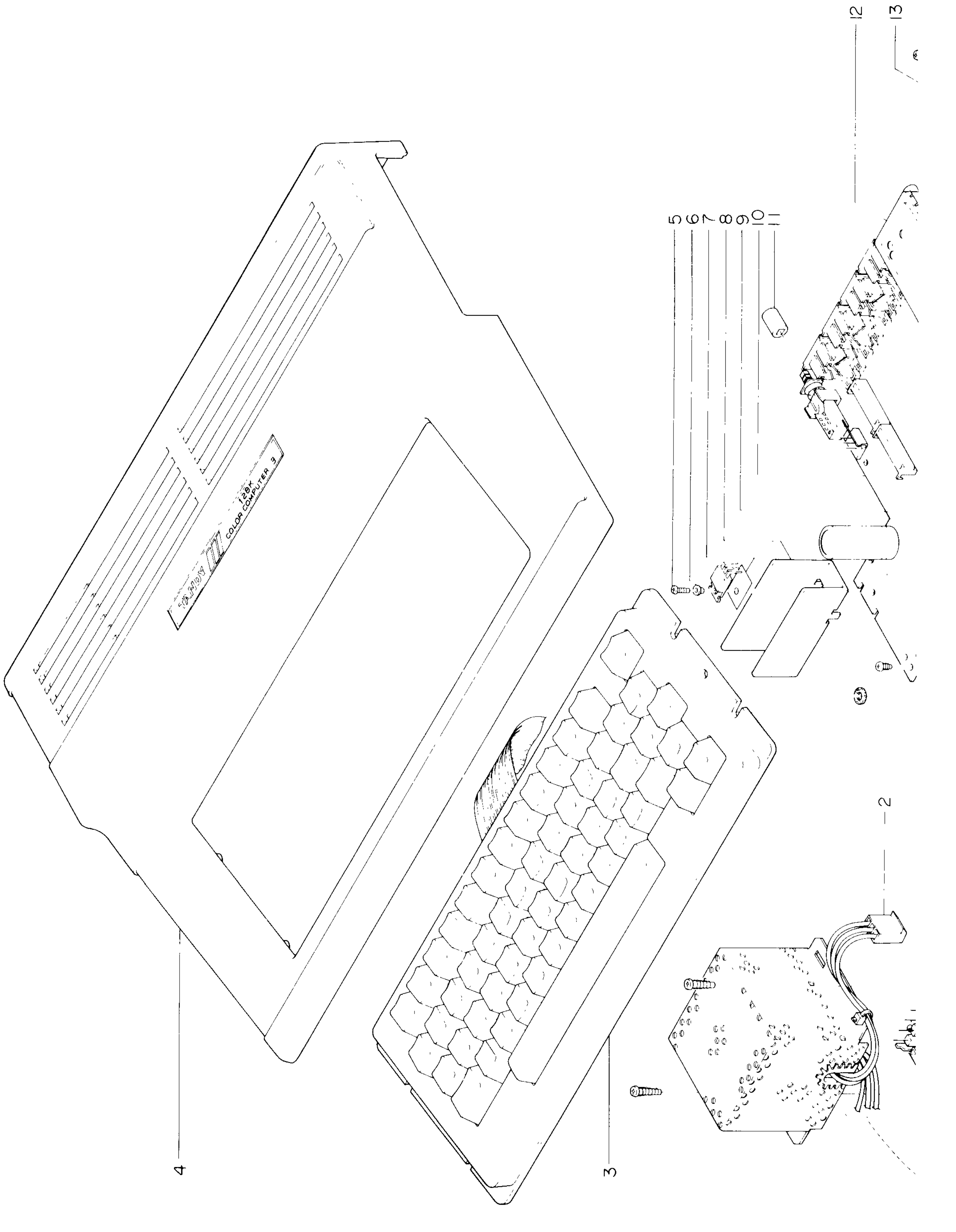
MISCELLANEOUS

Ref. No.	Description	RS Part No.	Mfr's Part No.
	Cord, Patch RCA-RCA		313510110A or
			313510130A
	Box, Switch TV/Computer		189510030A or
			189510040A
	Socket, IC(for IC6) 68 Pin PLCC		195110470A or
			195110480A
	Socket, IC(for IC16-19) 18 Pin DIP		195110410A or
			195110150A or
			195110290A

NTSC

EXPLODED VIEW PARTS LIST

Ref. No.	Description				RS Part No.	Mfr's Part No.
1	Bottom Cabinet Assembly				AZ-0107	M-00634
	Cabinet, Bottom			US		601311370A
				CA		601311380A
	Door					603610370A
	Spring, Torsion				ARB-7725	434810040A
	Foot				AF-0382	608010060A or
						608010350A
2	Pin Socket Assembly				AJ-7089	M-00632
	Socket,	Pin For Power Transformer				194011090A
	Pin,	Crimp			AJ-7566	194310070A
3	Keyboard		94HB		AXX-0245	187510370A
4	Top Cabinet Assembly				AZ-0106	M-00633
	Cabinet, Top			US		601211560A
				CA		601211570A
	Plate,	Top				711010470A
	Net			CA		851310440A
	Holder		For Net	CA		413100810B
5	Screw,		3x10P		AHD-0088	HMP03010SN
6	Grommet,		M			481110120A
7	Sheet,	Insulation			AHC-0304	483011470A
8	Heat Sink,	For Q1				471010310A
9	Nut,	Flange	3FN		AHD-7020	HANF300-SY
10	PCB Unit, Main					U-32052-
11	Knob		For Power		K-5012	655000940A
12	Modulator,		MDV-8		AC-4001	525010240A
13	Knob		For Reset		AK-5638	659510850A
14	Holder		For Key SW		AHC-2199	411101870A
15	Holder				AHC-2447	411103110A
16	Sheet,	Shield	For PCB		AHC-0305	473310990B
17	Rivet		For Shield		AHC-2449	HARRA003SN
18	Cord,	AC			W-1000	311010160A
	Hardware Kit					HWK2603334
	Screw, Taptite		4x20PT-B/ZnY			HCPB4020SY
	Screw, Taptite		4x25PT-B/ZnY			HCPB4025SY



128K
COLOR COMPUTER 3
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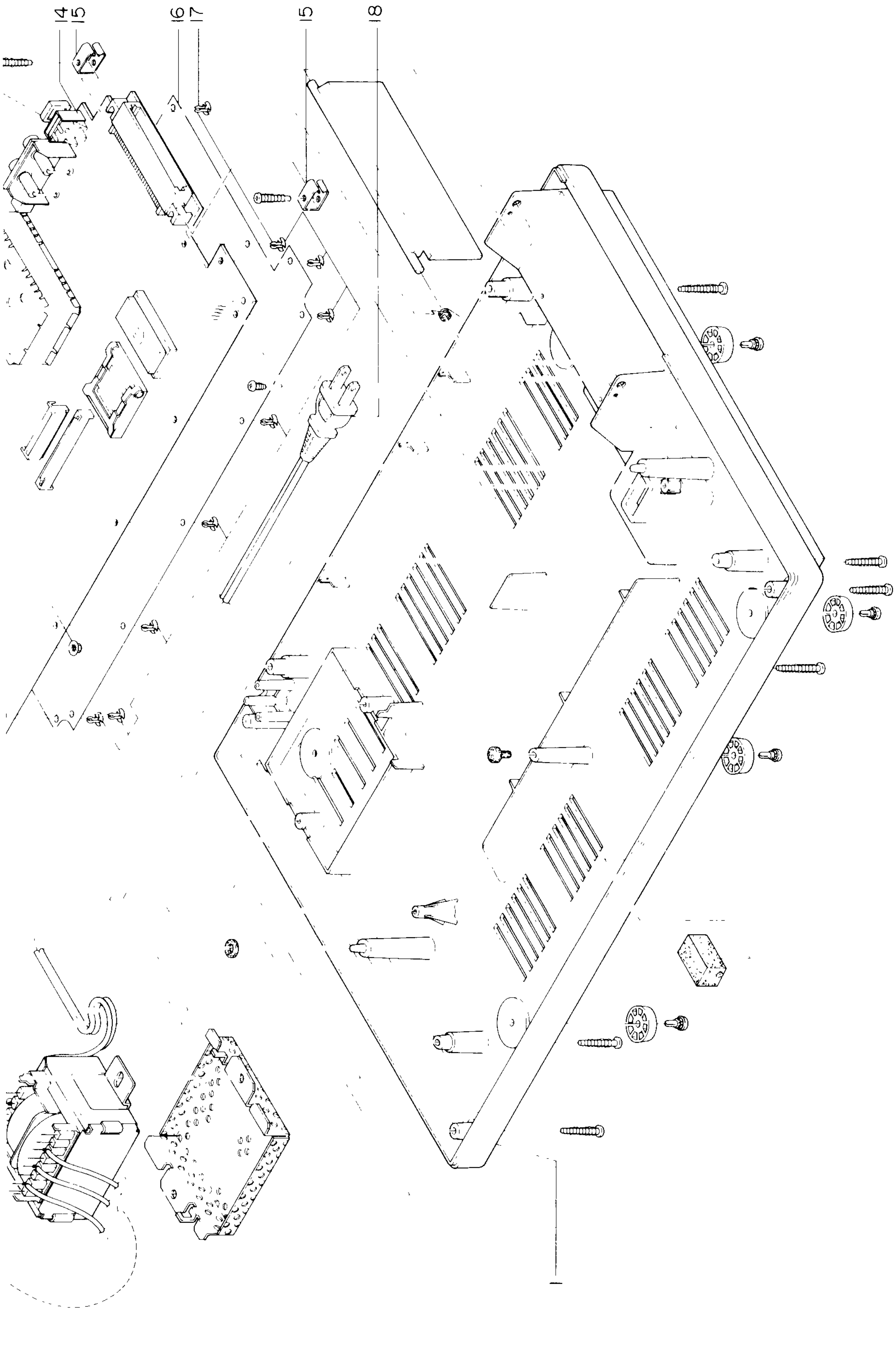
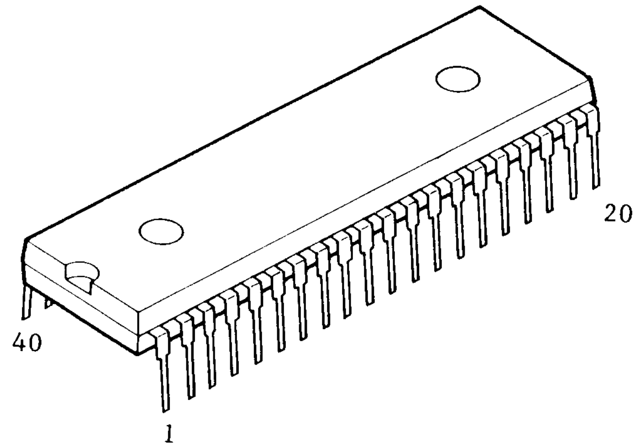
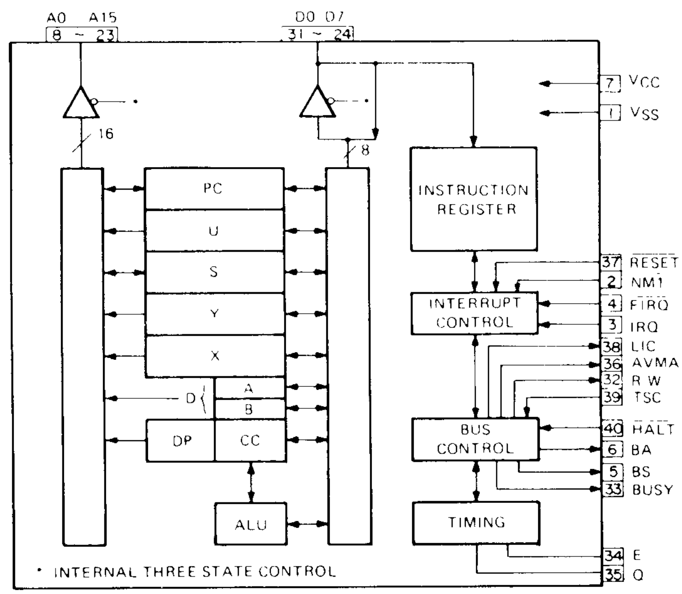


SEMICONDUCTOR INFORMATION

IC1: MC68B09EP





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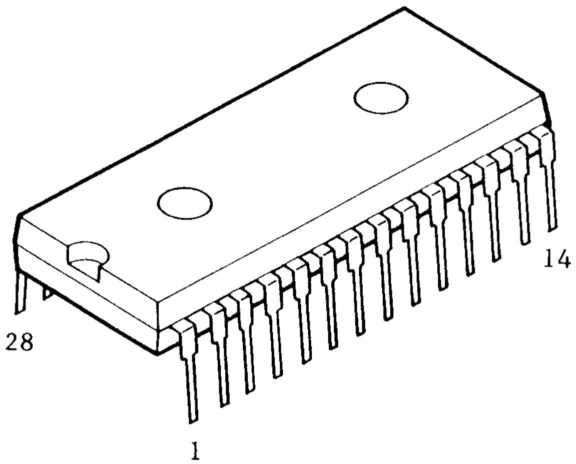
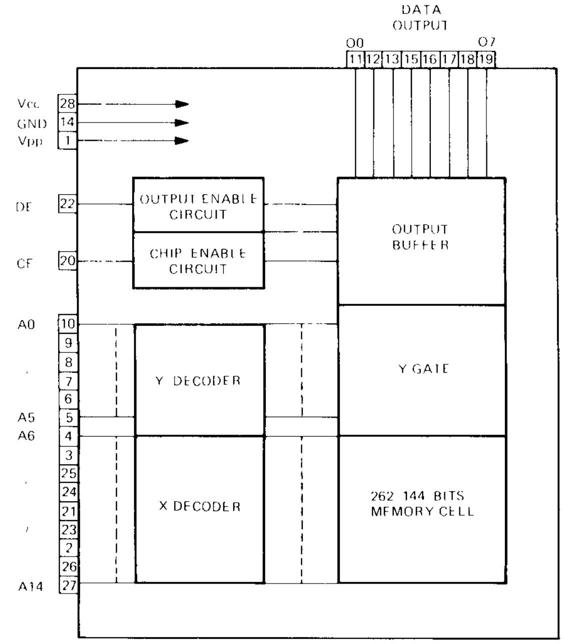
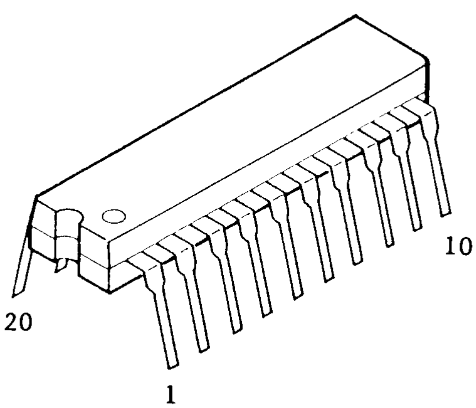
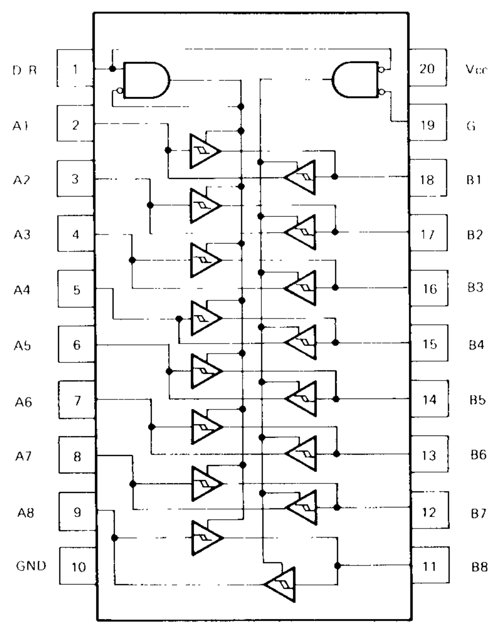


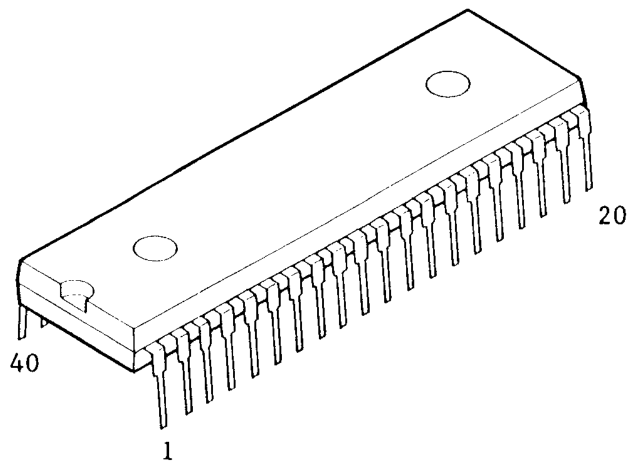


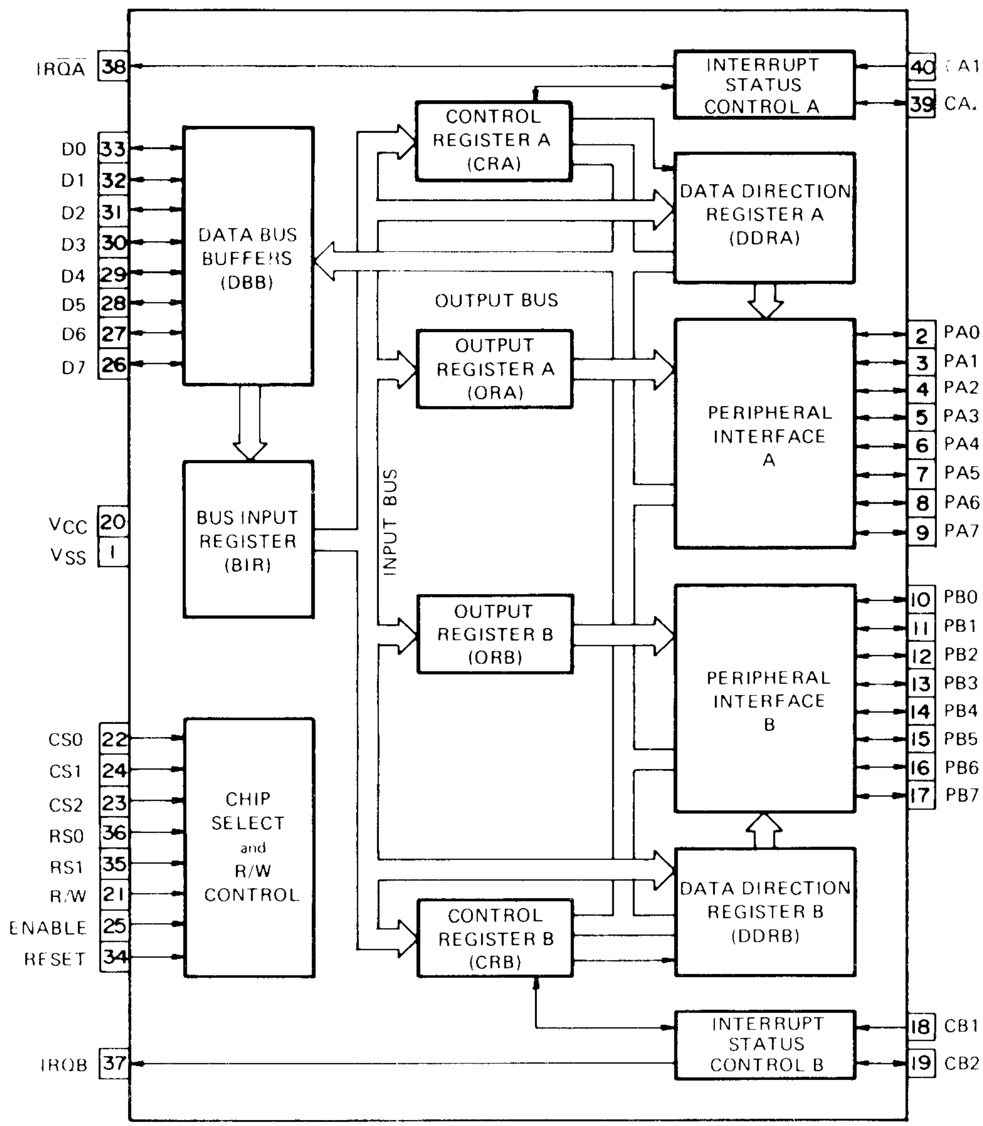
IC3: SN74LS245N



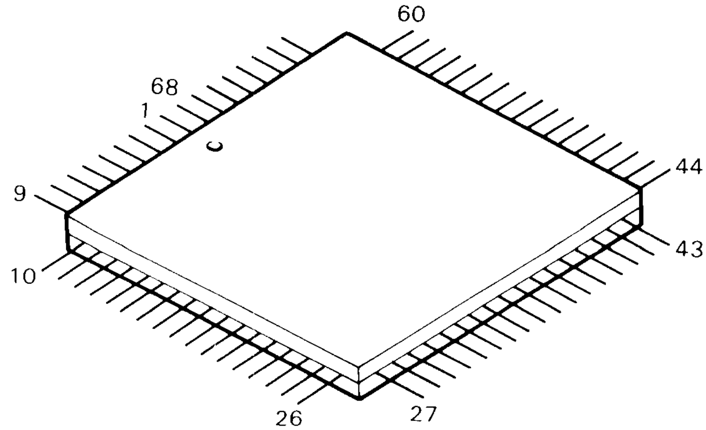


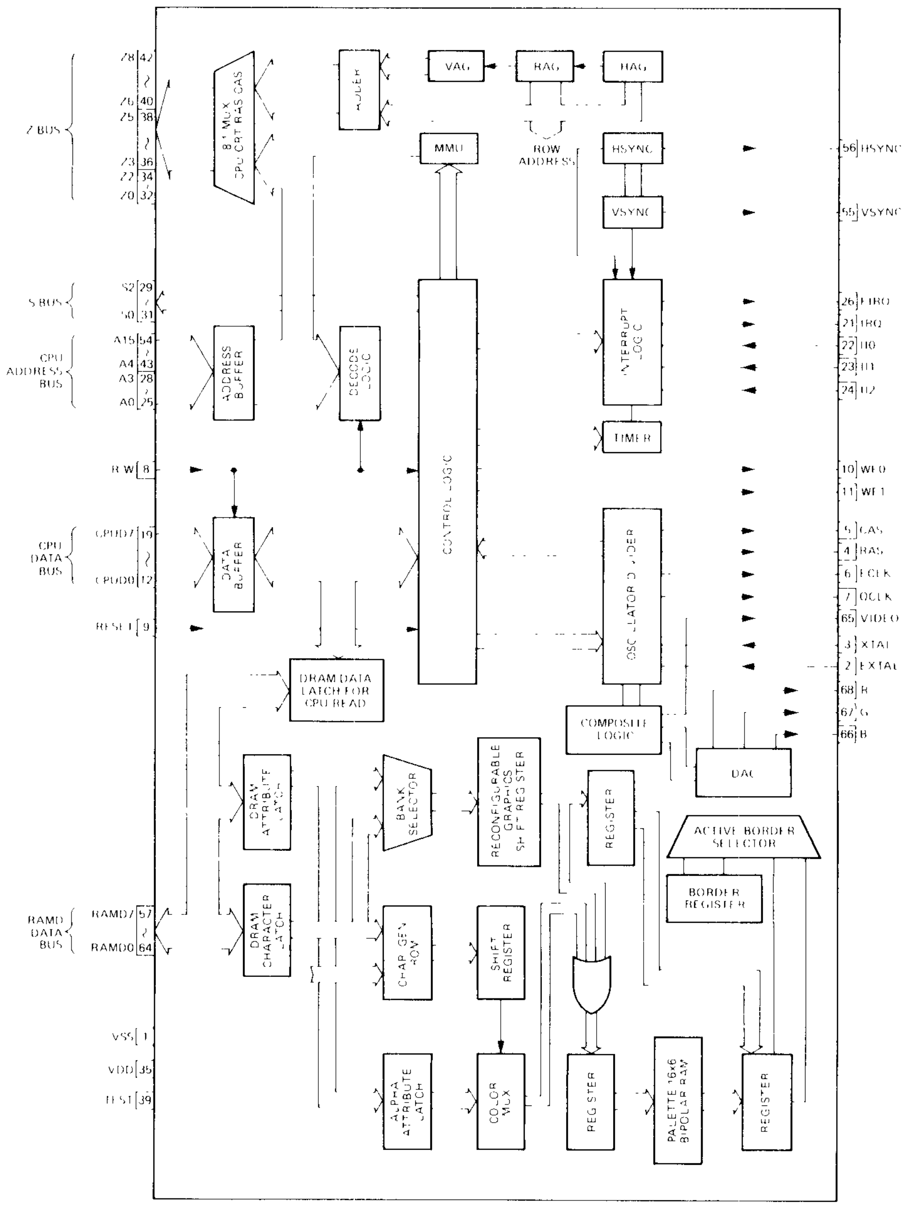
IC4: MC68B21P
IC5: LSC81001P



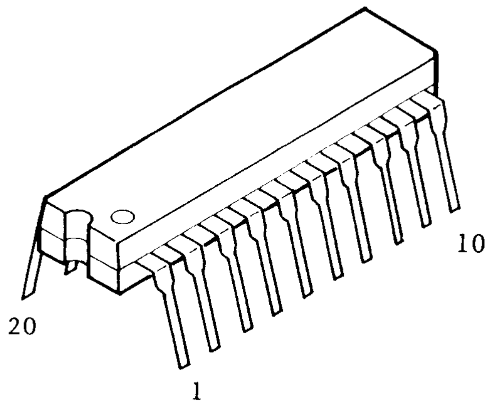


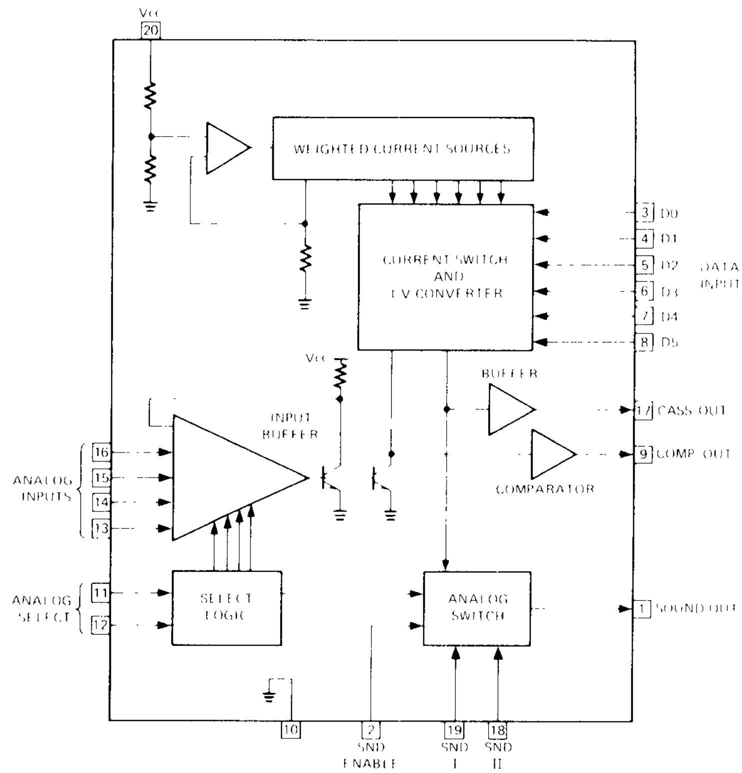
IC6: TCC1014


60
68
1
9
10
44
43
26
27

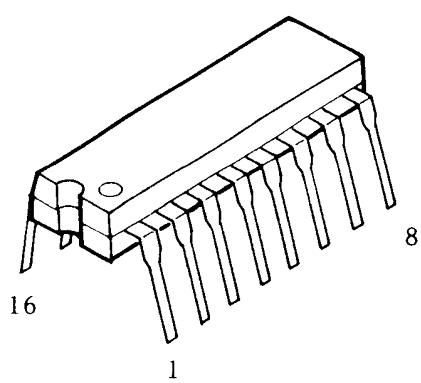

Z BUS
S BUS
CPU ADDRESS BUS
CPU DATA BUS
RAMD DATA BUS
R/W
RESET
VSS
VDD
TEST
8:1 MUX CPU CRT RAS CAS
ADDRESS BUFFER
DATA BUFFER
DECODE LOGIC
MMU
VAG
RAG
HAG
ROW ADDRESS
HSYNC
VSYNC
INTERRUPT LOGIC
TIMER
CONTROL LOGIC
OSCILLATOR DIVIDER
COMPOSITE LOGIC
DAC
ACTIVE BORDER SELECTOR
BORDER REGISTER
DRAM DATA LATCH FOR CPU READ
DRAM ATTRIBUTE LATCH
DRAM CHARACTER LATCH
BANK SELECTOR
CHAR GEN ROW
ALPHA ATTRIBUTE LATCH
RECONFIGURABLE GRAPHICS SHIFT REGISTER
SHIFT REGISTER
COLOR MUX
REGISTER
PALETTE 16x6 BIPOLAR RAM
HSYNC
VSYNC
FIRQ
IRQ
WE0
WE1
CAS
RAS
ECLK
QCLK
VIDEO
XTAL
EXTAL
R
G
B

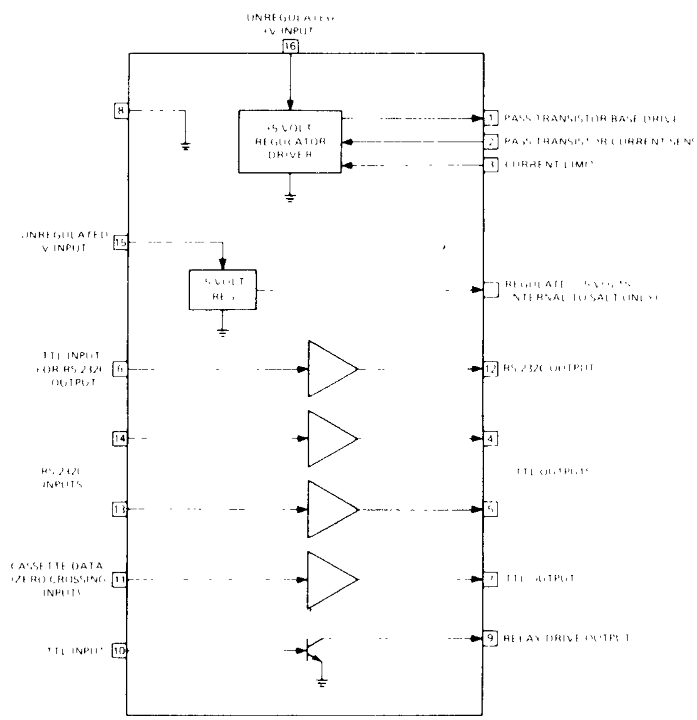
IC7: 8050526





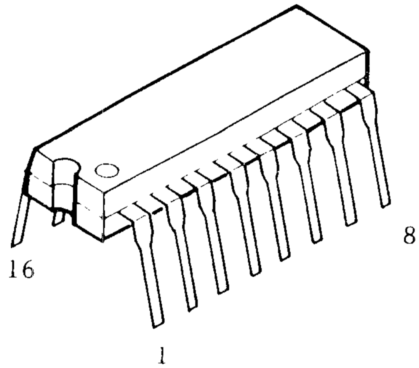
IC8: 8050527

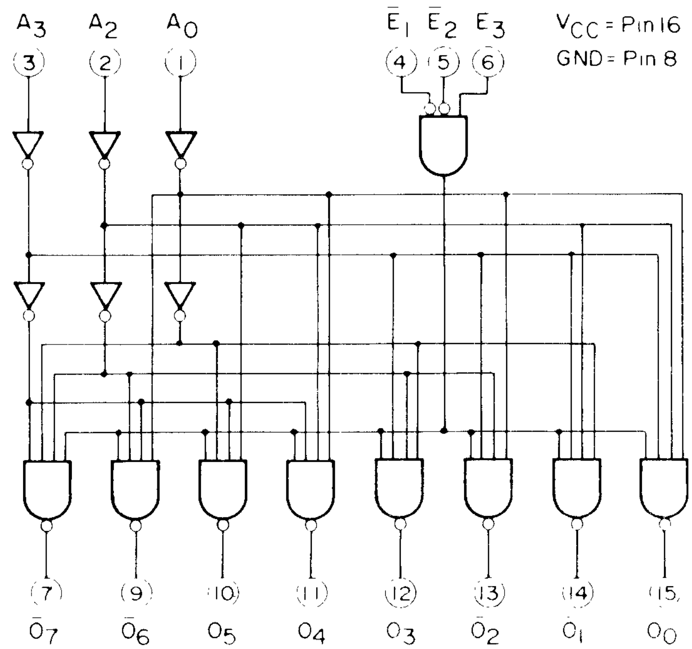




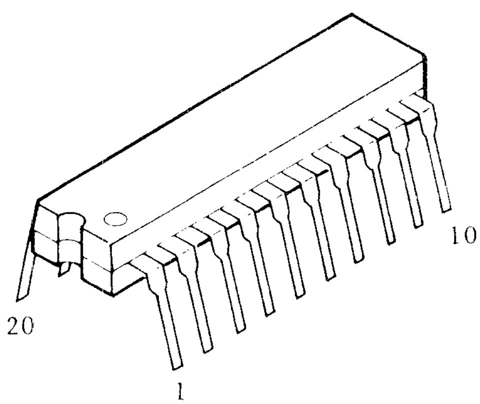
NTSC

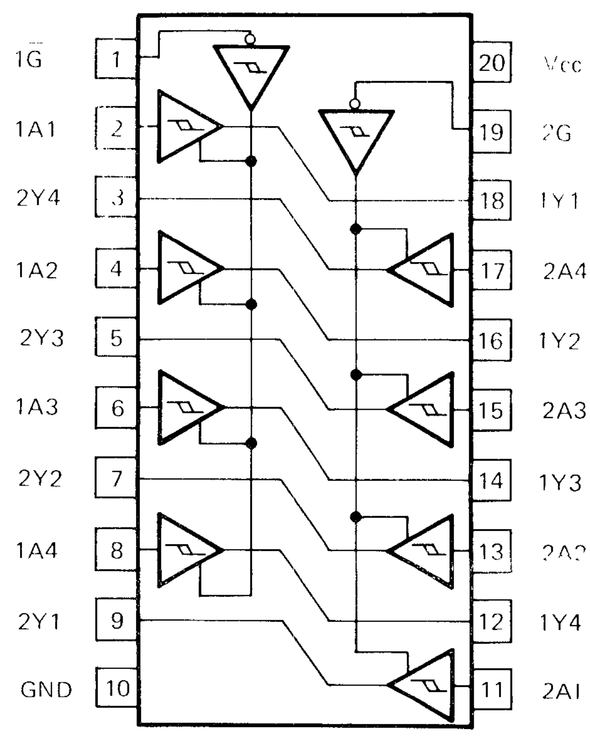
IC9: SN74LS138N



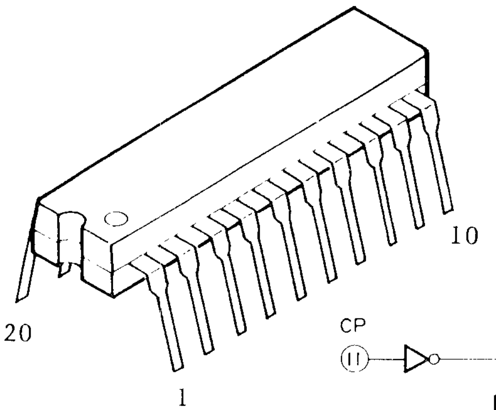


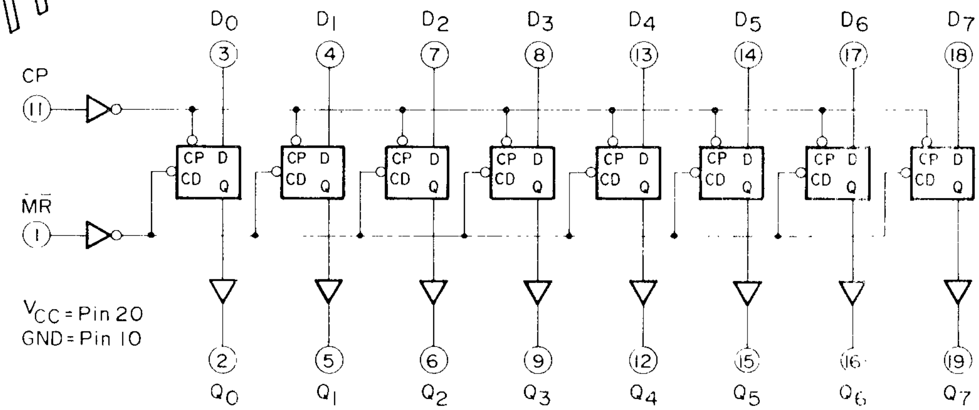
IC10-12: SN74LS244N



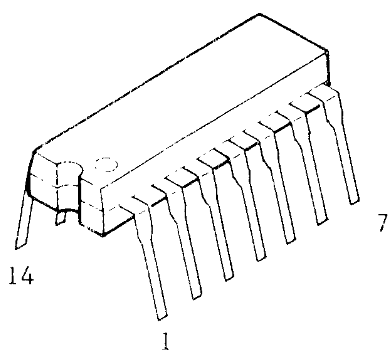


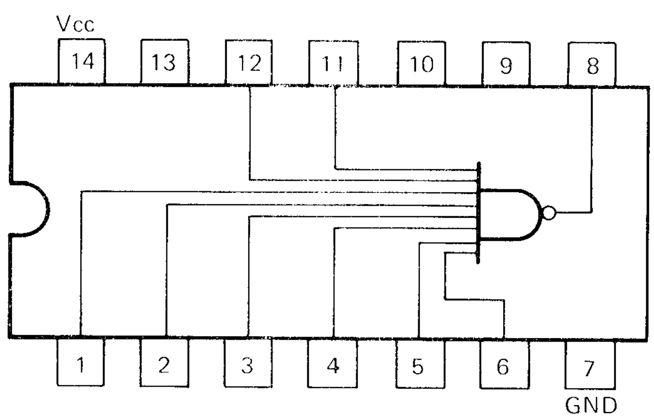
IC13: SN74LS374N



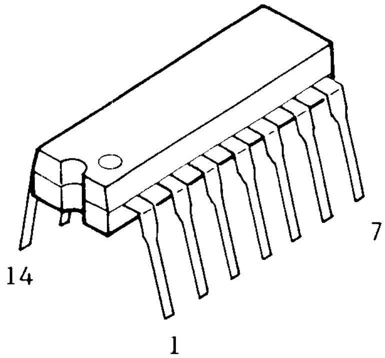


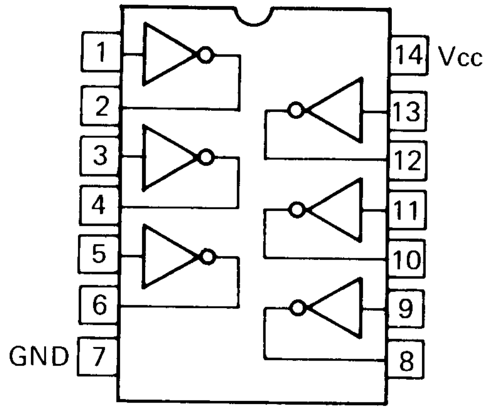
IC14: SN74LS30N



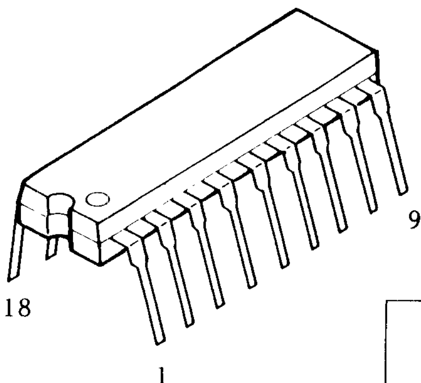


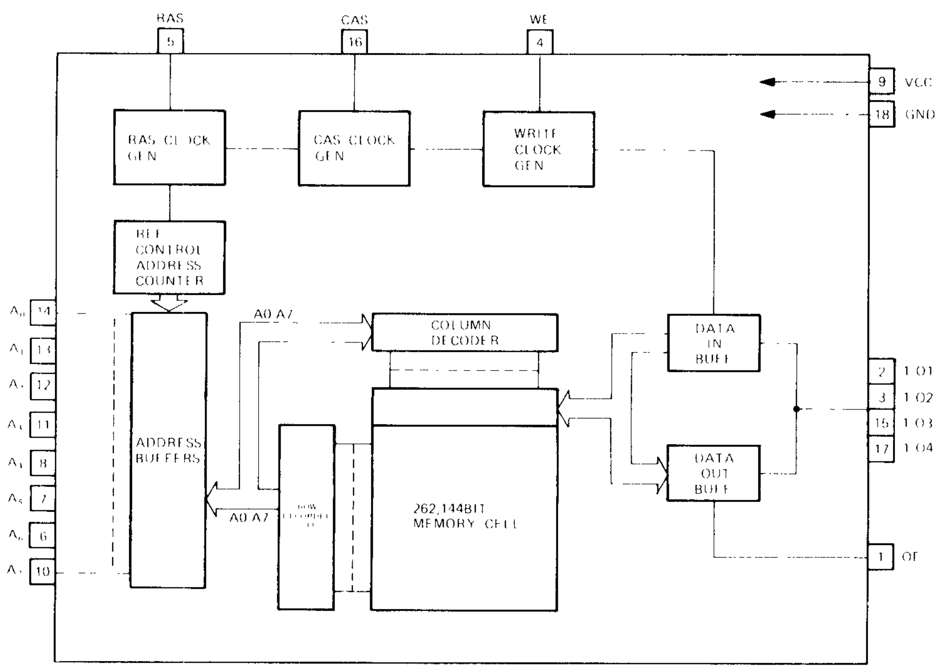
IC15: SN74LS04N



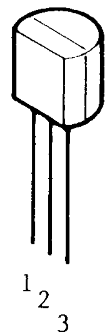


IC16-19: HM50464P-1

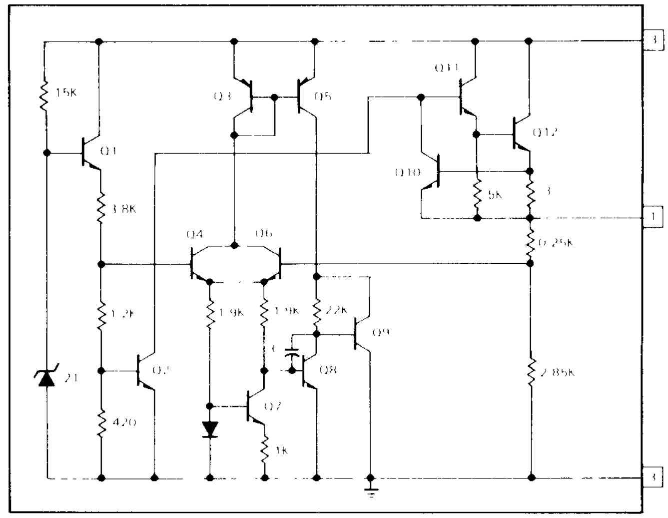




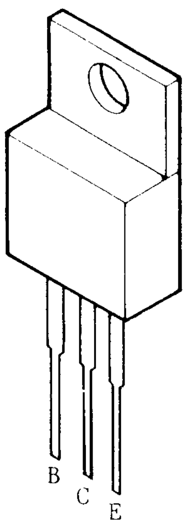
IC36: MC78L08ACP



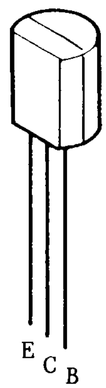
1: OUTPUT
2: GND
3: INPUT



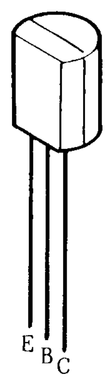
Q1: KTD880

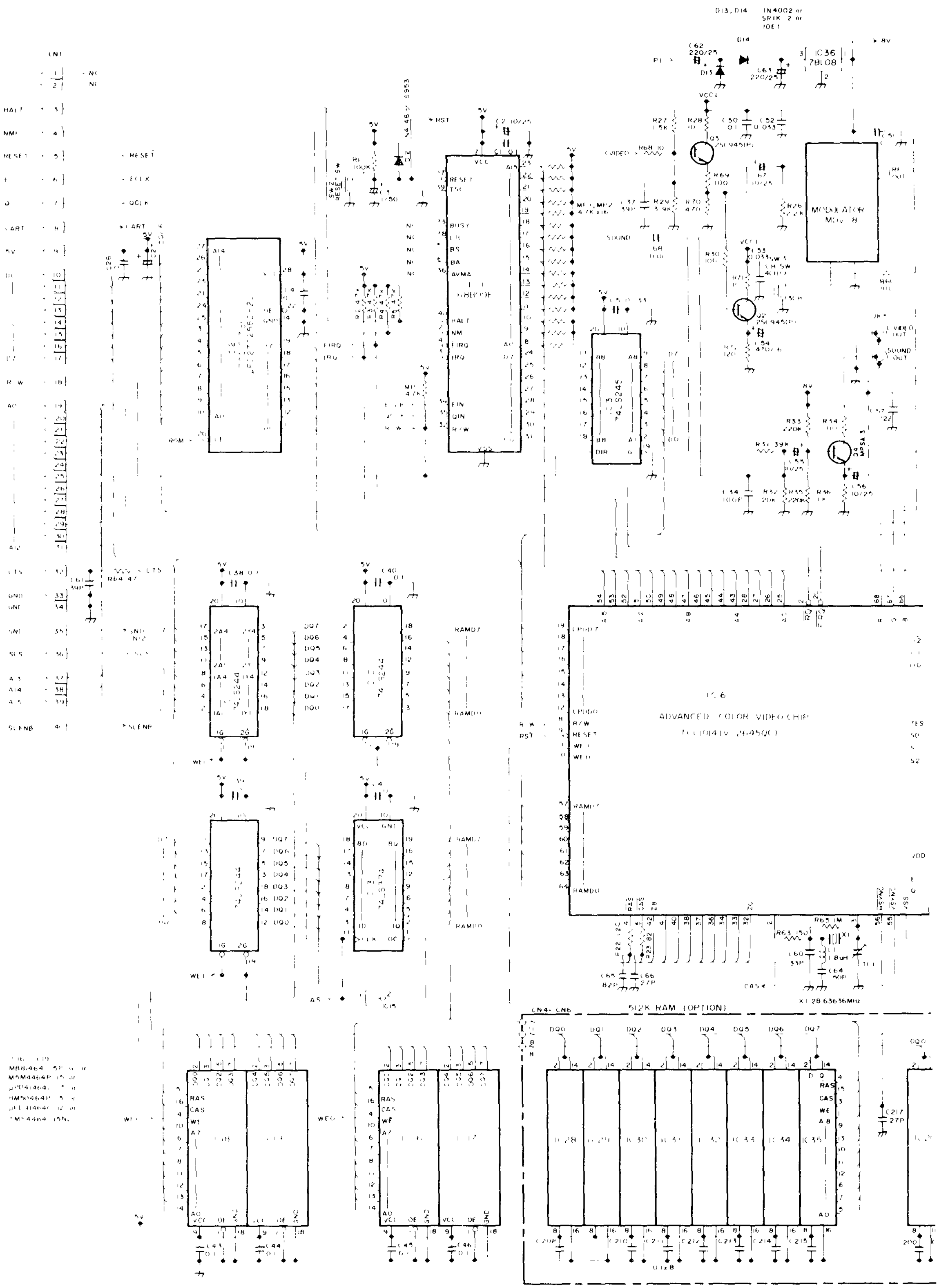


Q2,Q3,Q5 - Q7: 2SC945



Q4: MPSA13

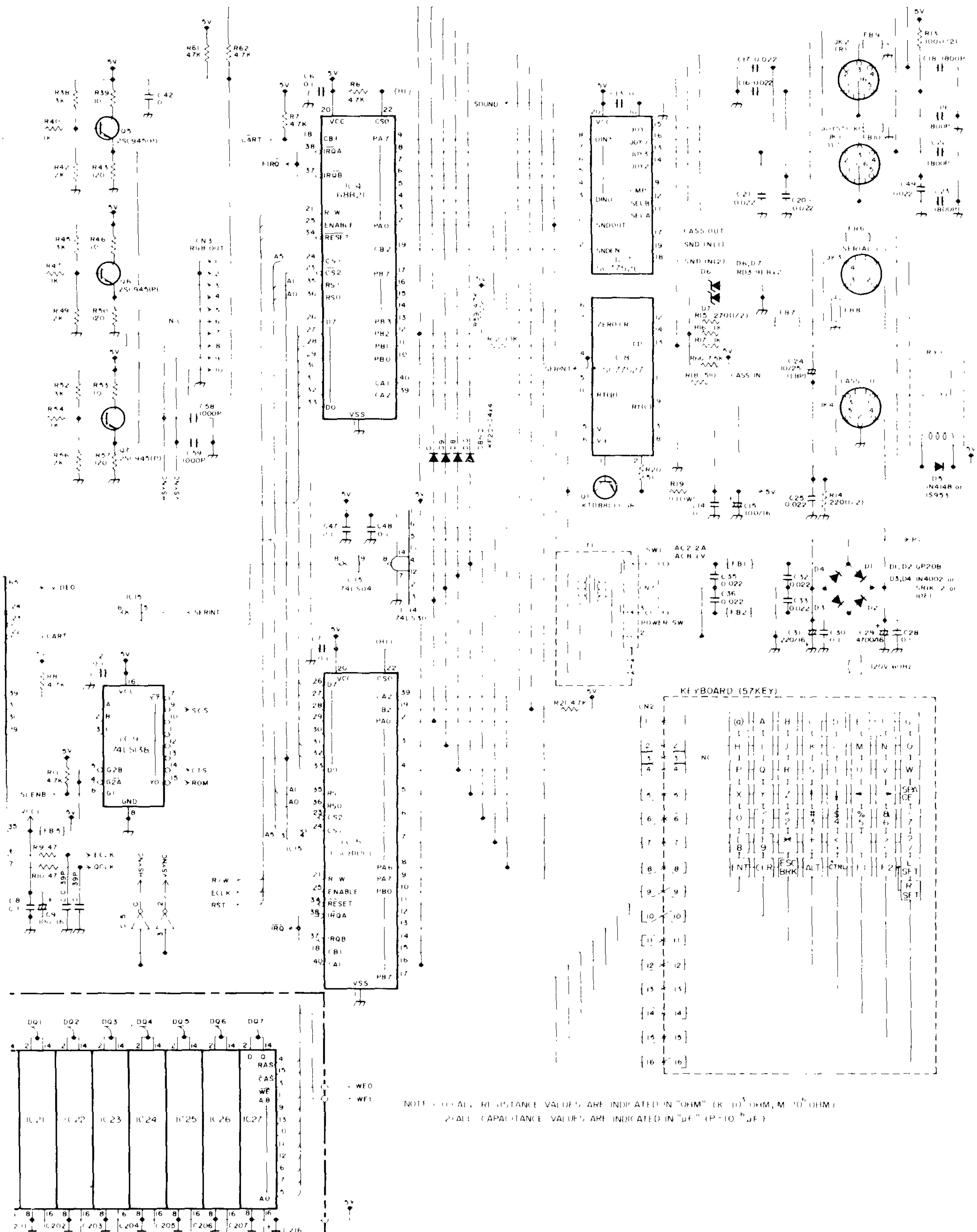




ADVANCED COLOR VIDEO CHIP
MODULATOR
512K RAM (OPTION)
6809E
74LS245
74LS244
74LS374
IC36 78L08

C DIAGRAM

Cat. No. 26-3334



NOTE: 1) ALL RESISTANCE VALUES ARE INDICATED IN "OHM" (K=10³ OHM, M=10⁶ OHM)
2) ALL CAPACITANCE VALUES ARE INDICATED IN "μF" (P=10⁻⁶ μF)

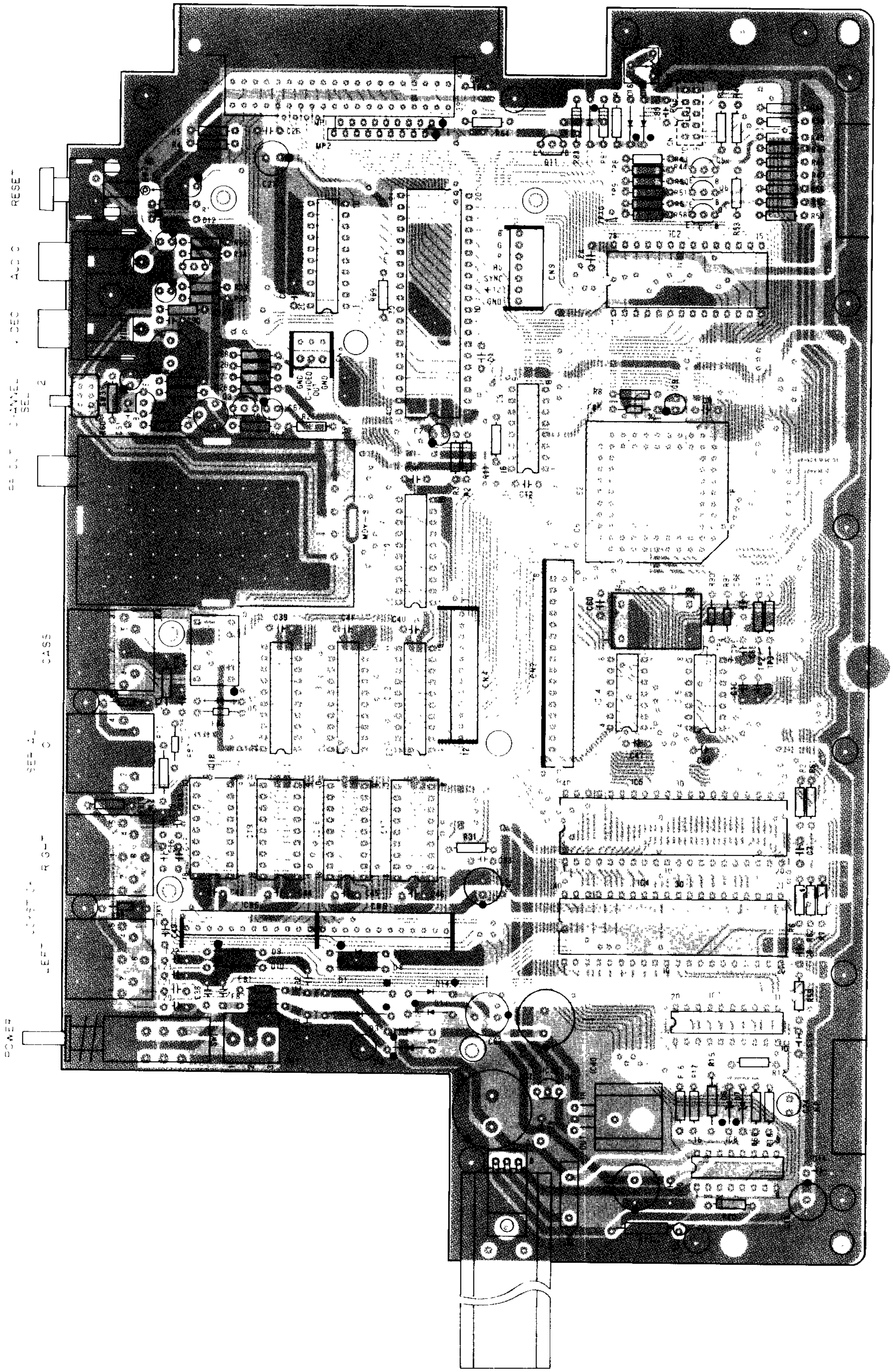
SECTION IX

PAL Version

PAL

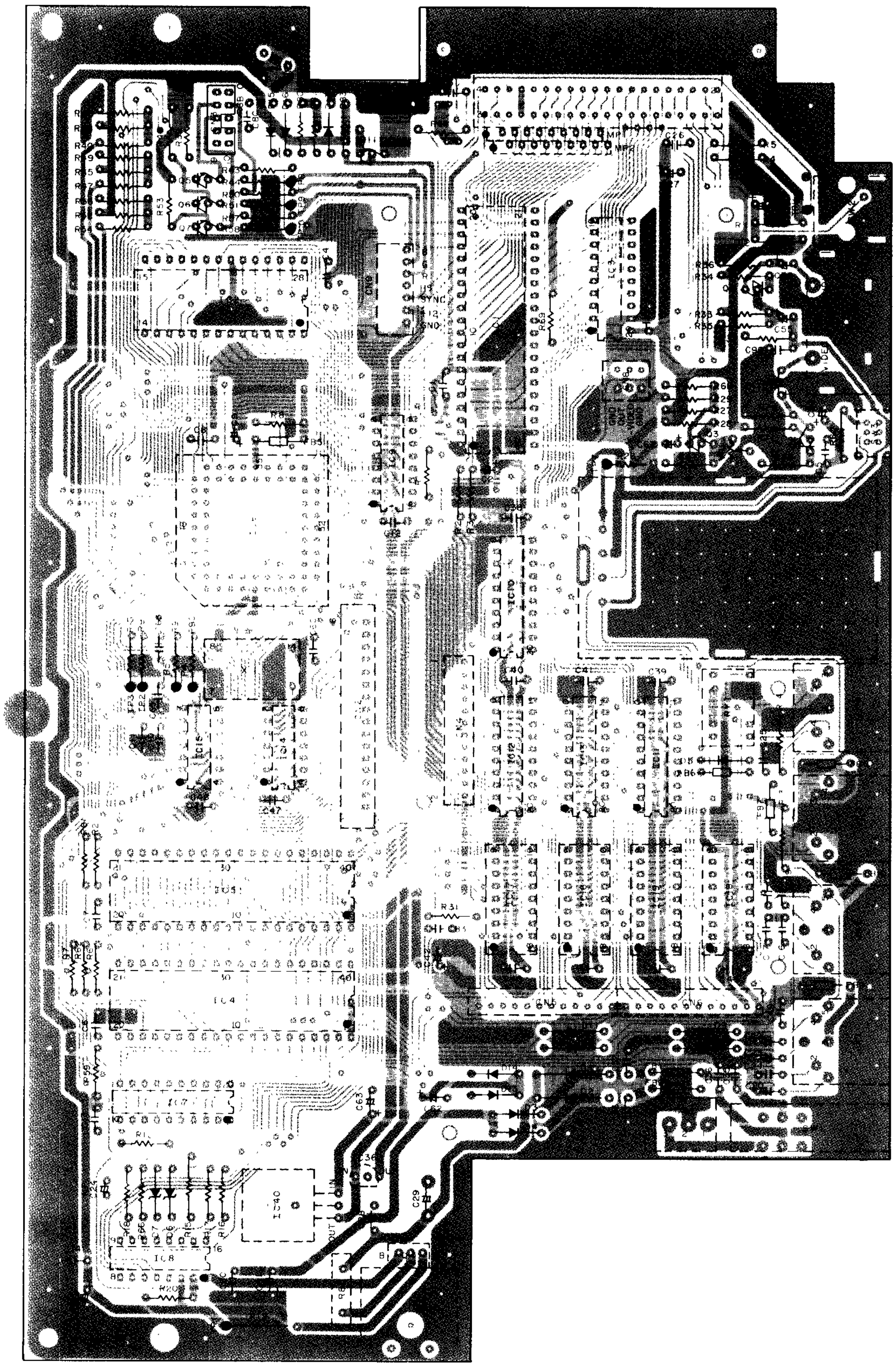
PCB VIEWS

TOP VIEW



PAL

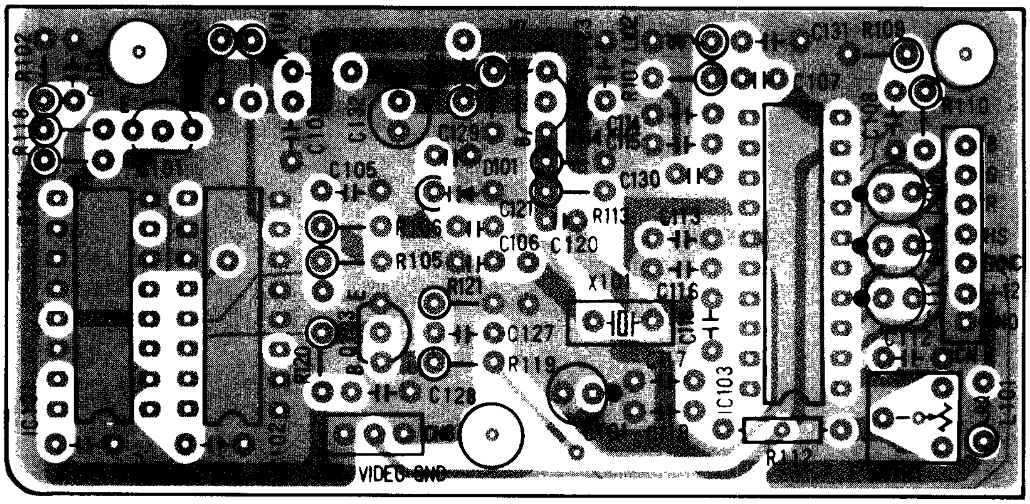
BOTTOM VIEW



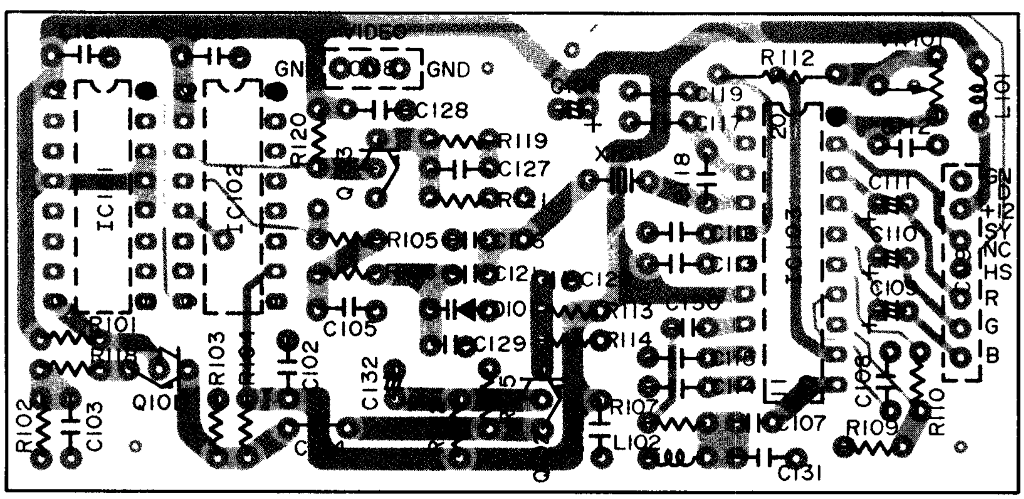
PAL

PAL SUB PCB

TOP VIEW



BOTTOM VIEW



ELECTRICAL PARTS LIST

CAPACITORS

Ref. No.	Description				RS Part No.	Mfr's Part No.
C1	M-Plastic	0.1µF	50V	+-5% or		CFQMK104JL or
	M-Plastic	0.1µF	63V	+-10% or		CFSSLA01KQ or
	Ceramic	0.1µF	50V+80-20%			CJRPK104ZM
C2	Electrolytic	10µF	25V	+-20%		CEACI106M*
C3	Electrolytic	1µF	50V	+-20%		CEACK105M*
C4-8	M-Plastic	0.1µF	50V	+-5% or		CFQMK104JL or
	M-Plastic	0.1µF	63V	+-10% or		CFSSLA01KQ or
	Ceramic	0.1µF	50V+80-20%			CJRPK104ZM
C9	Electrolytic	10µF	25V	+-20%		CEACI106M*
C10/11	Ceramic SL	39pF	50V	+-5%		CCJVK390J*
C12-14	M-Plastic	0.1µF	50V	+-5% or		CFQMK104JL or
	M-Plastic	0.1µF	63V	+-10% or		CFSSLA01KQ or
	Ceramic	0.1µF	50V+80-20%			CJRPK104ZM
C15	Electrolytic	100µF	16V	+-20%		CEACG107M*
C16/17	Ceramic	0.022µF	50V+80-20%			CKKPK223Z*
C18/19	Mylar*	1800pF	50V	+-10%		CQQMK182K* or
						CQQMK182KL
C20/21	Ceramic	0.022µF	50V+80-20%			CKKPK223Z*
C22/23	Mylar	1800pF	50V	+-10%		CQQMK182K* or
						CQQMK182KL
C24	Electro NP/LN	10µF	25V	+-20%		CEPCI106M*
C25	Ceramic	0.022µF	50V+80-20%			CKKPK223Z*
C26	M-Plastic	0.1µF	50V	+-5% or		CFQMK104JL or
	M-Plastic	0.1µF	63V	+-10% or		CFSSLA01KQ or
	Ceramic	0.1µF	50V+80-20%			CJRPK104ZM
C27	Electrolytic	100µF	16V	+-20%		CEACG107M*
C28	M-Plastic	0.1µF	50V	+-5% or		CFQMK104JL or
	M-Plastic	0.1µF	63V	+-10% or		CFSSLA01KQ or
	Ceramic	0.1µF	50V+80-20%			CJRPK104ZM
C29	Electrolytic	4700µF	16V	+-20%		CEACG478M*
C30	M-Plastic	0.1µF	50V	+-5% or		CFQMK104JL or
	M-Plastic	0.1µF	63V	+-10% or		CFSSLA01KQ or
	Ceramic	0.1µF	50V+80-20%			CJRPK104ZM
C31	Electrolytic	220µF	16V	+-20%		CEACG227M*
C32/33	Ceramic	0.022µF	50V+80-20%			CKKPK223Z*
C34	Not Used					
C35/36	Ceramic	0.022µF	50V+80-20%			CKKPK223Z*
C37	Not Used					
C38-41	M-Plastic	0.1µF	50V	+-5% or		CFQMK104JL or
	M-Plastic	0.1µF	63V	+-10% or		CFSSLA01KQ or
	Ceramic	0.1µF	50V+80-20%			CJRPK104ZM
C42	Electrolytic	100µF	16V	+-20%		CEACG107M*
C43-48	M-Plastic	0.1µF	50V	+-5% or		CFQMK104JL or
	M-Plastic	0.1µF	63V	+-10% or		CFSSLA01KQ or
	Ceramic	0.1µF	50V+80-20%			CJRPK104ZM
C49	Ceramic	0.022µF	50V+80-20%			CKKPK223Z*
C50	Electrolytic	10µF	25V	+-20%		CEACI106M*

NOTE: *Mylar is a registered trademark of E. I. Du Pont de Nemours and Company.

Ref. No.	Description				
C51	M-Plastic	0.1μF	50V +-5% or		CFQMK104JL or
	M-Plastic	0.1μF	63V +-10% or		CFSSLA01KQ or
	Ceramic	0.1μF	50V+80-20%		CJRPK104ZM
C54	Electrolytic	470μF	16V +-20%		CEACG477M*
C55/56	Electrolytic	10μF	25V +-20%		CEACI106M*
C57	Ceramic	0.022μF	50V+80-20%		CKKPK223Z*
C58/59	Not Used				
C60	M-Plastic	0.1μF	50V +-5% or		CFQMK104JL or
	M-Plastic	0.1μF	63V +-10% or		CFSSLA01KQ or
	Ceramic	0.1μF	50V+80-20%		CJRPK104ZM
C61	Ceramic SL	39pF	50V +-5%		CCJVK390J*
C62	Electrolytic	1000μF	16V +-20%		CECCG108M*
C63	Electrolytic	1000μF	25V +-20%		CECCI108M*
C64	Not Used				
C65	Ceramic SL	82pF	50V +-5%		CCJBK820J*
C66	Ceramic	27pF	50V +-5%		CCJBK270J*
C67	Electrolytic	47μF	16V +-20%		CEDCG476M*
C68-79	Not Used				
C80	Mylar	1500pF	50V +-5%		CQQMK152J* or
					CQQMK152JL
C81/82	Not Used				
C83	Mylar	0.01μF	50V +-5%		CQQMK103J* or
					CQQMK103JL
C84-89	Not Used				
C90	Ceramic NPO	10μF	50V +-5%		CCJBK101J*
C91-100	Not Used				
C101	Electrolytic	100μF	16V +-20%		CECCG107M*
C102	M-Plastic	0.1μF	50V +-5% or		CFQMK104JL or
	M-Plastic	0.1μF	63V +-10%		CFSSLA01KQ
C103	Mylar	0.01μF	50V +-5% or		CQQMK103JL or
	M-Plastic	0.01μF	50V +-5%		CFQMK103JL
C104	Ceramic	1000pF	50V+80-20%		CKJPK102Z*
C105	Mylar	2200pF	50V +-5%		CQQMK222JL or
					CFQMK222JL
C106	Ceramic NPO	15pF	50V +-5%		CCJBK150J*
C107	Ceramic	1000pF	50V+80-20%		CKJPK102Z*
C108	Mylar	0.01μF	50V +-5% or		CQQMK103JL or
	M-Plastic	0.01μF	50V +-5%		CFQMK103JL
C109-111	Electrolytic	10μF	16V +-20%		CEDCG106M*
C112	Mylar	1000pF	50V +-5%		CQQMK102J*
C113-116	M-Plastic	0.1μF	50V +-5% or		CFQMK104JL or
	M-Plastic	0.1μF	63V +-10%		CFSSLA01KQ
C117/118	Ceramic NPO	100pF	50V +-5%		CCJBK101J*
C119	Mylar	0.01μF	50V +-5% or		CQQMK103JL or
	M-Plastic	0.01μF	50V +-5%		CFQMK103JL
C120	Ceramic	1000pF	50V+80-20%		CKJPK102Z*
C121	Ceramic NPO	30pF	50V +-5%		CCJBK300J*
C122	Not Used				
C123-125	M-Plastic	0.1μF	50V +-5% or		CFQMK104JL or
	M-Plastic	0.1μF	63V +-10%		CFSSLA01KQ
C126	Not Used				
C127	Mylar	1800pF	50V +-5%		CQQMK182J*
C128	M-Plastic	0.1μF	50V +-5% or		CFQMK104JL or
	M-Plastic	0.1μF	63V +-10%		CFSSLA01KQ

Ref. No.	Description	RS Part No.	Mfr's Part No.
C129	Ceramic 5p 50V+-0.25pF		CCJBK5R0C*
C130	Ceramic 1000pF 50V+80-20%		CKJPK102Z
C131	Ceramic NPO 39pF 50V +-5%		CCJBK390J*
C132	Electrolytic 47μF 16V +-20%		CEDCG476M*
	COIL		
L101	Inductor 100μH K		142011510A
L102	Inductor 22μH K		142011430A
	CONNECTORS		
CN1	PCB 40Pin Cartridge or		194210060A or
	PCB		194210140A
CN2	Wire 16Pin Keyboard or		193910680A or
	Wire		193911090A
CN3	Pin 10Pin RGB		194112500A
CN4-6	Pin 12Pin		194010510A
CN7	Pin 3Pin		194111250A
CN8	Pin 3Pin		194011120A
	Pin		194112550A
CN9	Pin 7Pin		194011130A
	Pin		194112560A
	CORES		
FB1/2	for Noise		588010060A or
			588010070A or
			588010130A
FB3/4	Not Used		
FB5-10	for Noise		588010060A or
			588010070A or
			588010130A
	CRYSTALS		
X1	28.475MHz Clock OSC		391012290A
X101	4.433618MHz HC-18/U		391010251A
	DIODES		
D1/2	Silicon GP20B Rectifier		SDSI00140-
D3/4	Silicon 1N4002 or		SDSI00036- or
	SR1K-2 or		SDSI00026- or
	10E1 or		SDSI00003- or
	1N4002		SDSI00007-
D5	Silicon 1S953 Switchihg or		SDSI00015- or
	1N4148		SDSI00057- or
			SDSI00064-

Ref. No.	Description				RS Part No.	Mfr's Part No.
D6/7	Zener	RD3.9E-B	Switching	or		SZRD3.9EB- or
		RD3.9E-L		or		SZRD3.9EL- or
		RD3.9E-N				SZRD3.9EN-
D8-11	Germanium	1KF20-04	Switching			SDGE00012-
D12	Silicon	1S953	Switchihg	or		SDSI00015- or
		1N4148				SDSI00057- or
						SDSI00064-
D13/14	Silicon	1N4002		or		SDSI00036- or
		SR1K-2		or		SDSI00026- or
		10E1		or		SDSI00003- or
		1N4002				SDSI00007-
D15-17	Silicon	1S953	Switchihg	or		SDSI00015- or
		1N4148				SDSI00057- or
						SDSI00064-
D101	Varicap	ITT310				SDVC00005-
	FUSE					
F1	250V 0.4A	(S504)				251201420A
	ICs					
IC1	MC68B09EP	N-MOS	MPU	or		SIMC68B09E or
	MBL68B09E-P-G			or		SIBL68B09E or
	HD68B09EP					SIHD68B09E
IC2	MBM27C256-25CZG	N-MOS	EP-ROM	or		SIBM256-25 or
	TC57256D-20			or		SITC#0003-
	MBM27C256A-25CZG					SIBM256A25
IC3	SN74LS245N	TTL	BUS	or		SIRNS245N- or
	MB74LS245M			or		SIMBS245M- or
	M74LS245P			or		SIM-S245P- or
	HD74LS245P					SIHDS245P-
IC4	MC68B21P	N-MOS	PIA	or		SIMC68B21- or
	MB8874HM-G			or		SIMB74HM-G or
	HD68B21P					SIHD68B21-
IC5	LSC81001P	N-MOS	PIA Select			SILS81001P
IC6	TCC1014	C-MOS	ACVC			SICC1014--
	IC Socket	68Pin				195110470A or
						195110480A
IC7	8050526	Bipola	DA Convertor			SISC50526-
IC8	8050527	Bipola	Regulator			SISC50527-
IC9	SN74LS138N	TTL	Decoder	or		SIRNS138N- or
	MB74LS138M			or		SIMBS138M- or
	M74LS138P			or		SIM-S138P- or
	HD74LS138P					SIHDS138P-
IC10-12	SN74LS244N	TTL	Buffer	or		SIRNS244N- or
	MB74LS244M			or		SIMBS244M- or
	M74LS244P			or		SIM-S244P- or
	HD74LS244P					SIHDS244P-
IC13	SN74LS374N	TTL	D-TYPE	or		SIRNS374N- or
	MB74LS374M			or		SIMBS374M- or
	M74LS374P			or		SIM-S374P- or
	HD74LS374P					SIHDS374P-

Ref. No.	Description	RS Part No.	Mfr's Part No.
IC14	SN74LS30N TTL 8IN NAND or		SIRNS30N-- or
	MB74LS30M or		SIMBS30M-- or
	M74LS30P or		SIM-S30P-- or
	HD74LS30P		SIHDS30P--
IC15	SN74LS04N TTL Inverter or		SIRNS04N-- or
	MB74LS04M or		SIMBS04M-- or
	M74LS04P or		SIM-S04P-- or
	HD74LS04P		SIHDS04P--
IC16-19	MB81464-15P-G N-MOS DRAM or		SIMB464-15 or
	HM50464P-15 or		SIHM464-15 or
	M5M4464P-15 or		SIM-464-15 or
	μPD41464C-15 or		SIPD464-15 or
	μPD41464C-15 or		SIPD464-12 or
	TMS4464-15NL		SITS464-15
	IC Socket 18Pin		195110410A or
			195110150A or
			195110290A
IC36	MC78L08ACP Bipola Regulator or		SIMCL08A-- or
	NJM78L08(A)		SINM78L08A
IC37-39	Not Used		
IC40	MC7812CT Bipola Regulator or		SIMC#0006- or
	μPC7812H		SIPC7812H-
IC101	MC14569BCP C-MOS Counter		SIMD4569B-
IC102	MC14568BCP C-MOS Counter		SIMD4568B-
IC103	MC1377P Bipola RGB		SIMC1377P-
	JACKS		
JK1/2	DIN Joystick		193410040A or
			193410070A
JK3	DIN Serial I/O		193410020A or
			193410050A
JK4	DIN Cassette I/O		193410030A or
			193410060A
JK5	RCA 2P Video/Sound		192010400A
	POTENTIOMETERS		
VR1	Semi-Fixed 500B V-Level Adjust		177110470A
VR2	Semi-Fixed 10kB HSYNC Pulse Width		177310220A or
			177310080A
VR101	Semi-Fixed 20kB Burst Position		177310230A or
			177310070A
	RELAY		
RY1	Remote Control ON/OFF for Cassette		581010140A or
			581010160A or
			581010710A

RESISTORS

Ref. No.	Description	RS Part No.	Mfr's Part No.
R1	Carbon 100kohm 1/4W +-5%		RCSQP104J*
R2-8	Carbon 4.7kohm 1/4W +-5%		RCSQP472J*
R9/10	Carbon 47 ohm 1/4W +-5%		RCSQP470J*
R11	Carbon 4.7kohm 1/4W +-5%		RCSQP472J*
R12	Carbon 10kohm 1/4W +-5%		RCSQP103J*
R13	Carbon 100 ohm 1/2W +-5%		RCSHP101J*
R14	Carbon 220 ohm 1/2W +-5%		RCSHP221J*
R15	Carbon 270 ohm 1/2W +-5%		RCSHP271J*
R16/17	Carbon 1.0kohm 1/4W +-5%		RCSQP102J*
R18	Carbon 510 ohm 1/4W +-5%		RCSQP511J*
R19	M-Film 10 ohm 1W +-5%		RM01HR10J*
R20	Carbon 51 ohm 1/4W +-5%		RCSQP510J*
R21	Carbon 4.7kohm 1/4W +-5%		RCSQP472J*
R22-25	Not Used		
R26	Carbon 2.2kohm 1/4W +-5%		RCSQP222J*
R27	Carbon 120kohm 1/4W +-5%		RCSQP124J*
R28	Carbon 10 ohm 1W +-5%		RCSQP100J*
R29	Carbon 82kohm 1/4W +-5%		RCSQP823J*
R30	Carbon 100 ohm 1/4W +-5%		RCSQP101J*
R31	Carbon 39kohm 1/4W +-5%		RCSQP393J*
R32	Carbon 20kohm 1/4W +-5%		RCSQP203J*
R33	Carbon 220kohm 1/4W +-5%		RCSQP224J*
R34	Carbon 100 ohm 1/4W +-5%		RCSQP101J*
R35	Carbon 220kohm 1/4W +-5%		RCSQP224J*
R36	Carbon 1.0kohm 1/4W +-5%		RCSQP102J*
R37	Not Used		
R38	Carbon 4.7kohm 1/4W +-5%		RCSQP472J*
R39	Carbon 10 ohm 1W +-5%		RCSQP100J*
R40	Carbon 1.0kohm 1/4W +-5%		RCSQP102J*
R41	Not Used		
R42	Carbon 3.9kohm 1/4W +-5%		RCSQP392J*
R43	Carbon 43 ohm 1/4W +-5%		RCSQP430J*
R44	Carbon 82 ohm 1/4W +-5%		RCSQP820J*
R45	Carbon 4.7kohm 1/4W +-5%		RCSQP472J*
R46	Carbon 10 ohm 1W +-5%		RCSQP100J*
R47	Carbon 1.0kohm 1/4W +-5%		RCSQP102J*
R49	Carbon 3.9kohm 1/4W +-5%		RCSQP392J*
R50	Carbon 43 ohm 1/4W +-5%		RCSQP430J*
R51	Carbon 82 ohm 1/4W +-5%		RCSQP820J*
R52	Carbon 4.7kohm 1/4W +-5%		RCSQP472J*
R53	Carbon 10 ohm 1W +-5%		RCSQP100J*
R54	Carbon 1.0kohm 1/4W +-5%		RCSQP102J*
R56	Carbon 3.9kohm 1/4W +-5%		RCSQP392J*
R57	Carbon 43 ohm 1/4W +-5%		RCSQP430J*
R58	Carbon 82 ohm 1/4W +-5%		RCSQP820J*
R59	Carbon 4.7kohm 1/4W +-5%		RCSQP472J*
R60	Carbon 100 ohm 1/4W +-5%		RCSQP101J*
R61/62	Carbon 4.7kohm 1/4W +-5%		RCSQP472J*
R63	Not Used		
R64	Carbon 47 ohm 1/4W +-5%		RCSQP470J*
R65	Not Used		
R66	Carbon 7.5kohm 1/4W +-5%		RCSQP752J*

Ref. No.	Description	RS Part No.	Mfr's Part No.
R67	Carbon 1.0kohm 1/4W +-5%		RCSQP102J*
R68	Carbon 200 ohm 1/4W +-5%		RCSQP201J*
R69	Carbon 4.7kohm 1/4W +-5%		RCSQP472J*
R70	Not Used		
R71	Carbon 10 ohm 1W +-5%		RCSQP100J*
R72	Carbon 62 ohm 1/4W +-5%		RCSQP620J*
R73-79	Not Used		
R80	Carbon 820 ohm 1/4W +-5%		RCSQP821J*
R81	Carbon 1.8kohm 1/4W +-5%		RCSQP182J*
R82	Not Used		
R83	Carbon 470 ohm 1/4W +-5%		RCSQP471J*
R84/85	Not Used		
R86	Cement 2 ohm 5W +-10%		RT05Y2R0KT
R87-89	Not Used		
R90	Carbon 110 ohm 1/4W +-5%		RCSQP111J*
R91	Carbon 82 ohm 1/4W +-5%		RCSQP820J*
R92-100	Not Used		
R101	Carbon 820 ohm 1/4W +-5%		RCSQP821J*
R102	Carbon 33 ohm 1/4W +-5%		RCSQP330J*
R103	Carbon 2.2kohm 1/4W +-5%		RCSQP222J*
R104	Carbon 27kohm 1/4W +-5%		RCSQP273J*
R105	Carbon 680 ohm 1/4W +-5%		RCSQP681J*
R106	Carbon 100kohm 1/4W +-5%		RCSQP104J*
R107	Carbon 1.0kohm 1/4W +-5%		RCSQP102J*
R108	Not Used		
R109/110	Carbon 1.0kohm 1/4W +-5%		RCSQP102J*
R111	Not Used		
R112	Carbon 47kohm 1/4W +-5%		RCSQP473J*
R113/114	Carbon 10kohm 1/4W +-5%		RCSQP103J*
R115	Carbon 2.2kohm 1/4W +-5%		RCSQP222J*
R116/117	Not Used		
R118	Carbon 22 ohm 1/4W +-5%		RCSQP220J*
R119	Carbon 680 ohm 1/4W +-5%		RCSQP681J*
R120	Carbon 1.0kohm 1/4W +-5%		RCSQP102J*
R121	Carbon 470 ohm 1/4W +-5%		RCSQP471J*
R122	Carbon 1.0kohm 1/4W +-5%		RCSQP102J*
	RESISTOR BLOCKS		
MP1/2	RGLD8X472J		522110520A
	SWITCHES		
SW1	Push for Power		182110240A
SW2	Key for Reset		187010040A
SW3	Slide for Channel Select		183111400A
	TRANSFORMER		
T1	Power EI54 240V		10102861SA

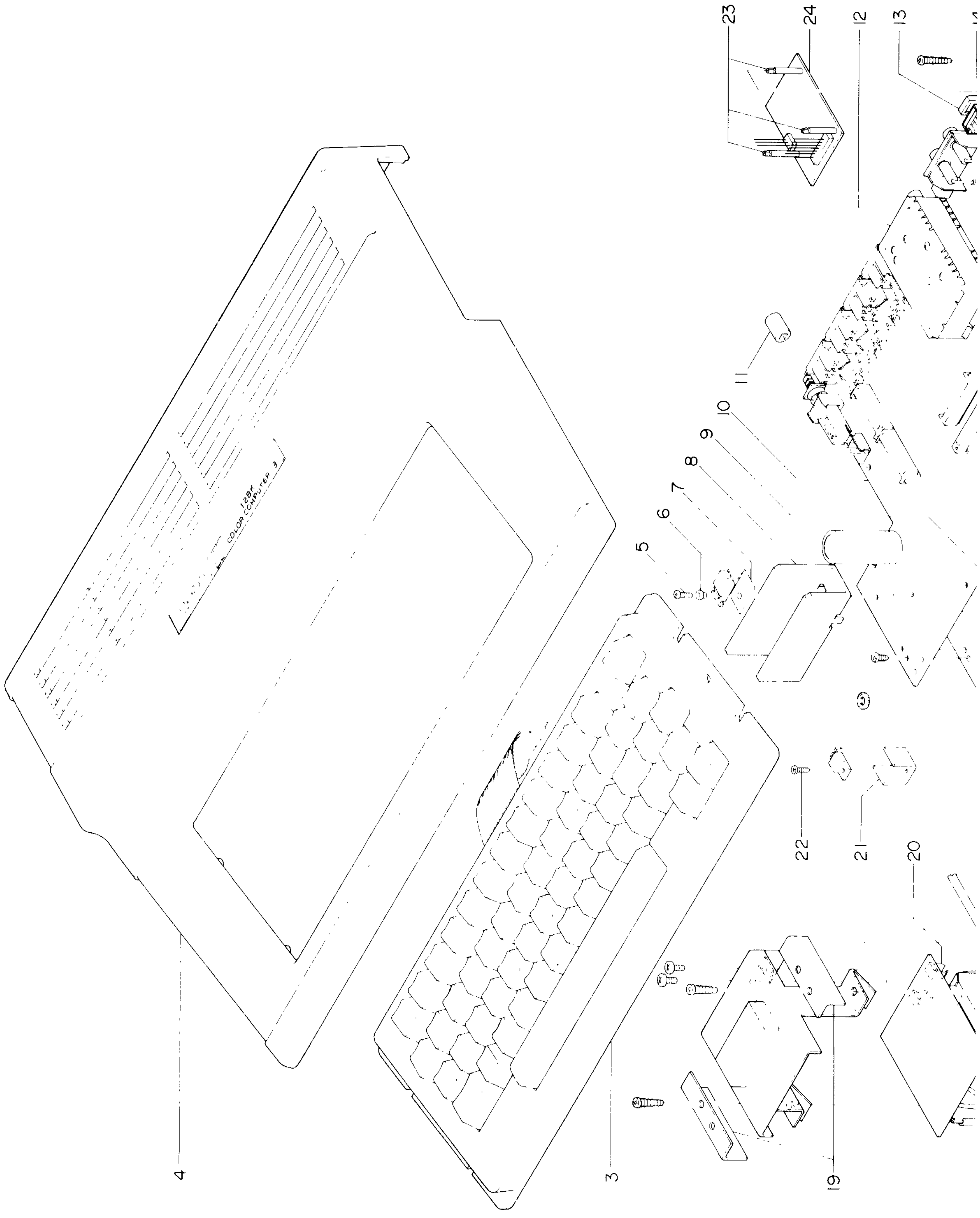
TRANSISTORS			
Ref. No.	Description	RS Part No.	Mfr's Part No.
Q1	KTD880(Y) NPN Regulator or		STKD880--Y or
	KTD880(GR)		STKD880--G
Q2/3	2SC1730(L) NPN Amp		ST2C1730-L
Q4	MPSA13 NPN Amp		STMS-A13--
Q5-7	2SC1730(L) NPN Amp		ST2C1730-L
Q8-10	Not Used		
Q11	2SC536(H) NPN		ST2C536--H
Q101	2SC536(H) NPN Amp		ST2C536--H
Q102	2SC1674(L) NPN		ST2C1674-L
Q103	2SC2786(LF)NPN Amp		ST2C2786LF

EXPLODED VIEW PARTS LIST

Ref. No.	Description	RS Part No.	Mfr's Part No.
1	Bottom Cabinet Ass'y		M-00726
	Cabinet, Bottom		601311370A
	Door		603610370A
	Spring, Torsion		434810040A
	Foot		608010060A or
			608010350A
2	Pin Socket Ass'y with Lead Wire		M-00762
	Socket, Pin for Power Transformer		194011090A
	Pin, Crimp 5167TL		194310070A
3	Keyboard		187510370A
4	Top Cabinet Ass'y		M-00725
	Cabinet, Top		601211560A
	Plate, Top		711010470A
	Plate, Control		711310430A
5	Screw, 3x12P/Ni-3 for Q1		HMP03012SN
6	Grommet, M for Q1		481110120A
7	Sheet, Insulation for Q1		483011470A
8	Heat Sink, for Q1		471010780A
9	Nut, Flange 3FN for Q1 and IC40		HANF300-SY
10	PCB Unit, Main		U-32055-1
11	Knob, for Power		655000940A
12	Modulator, MDV-9		525010250A
13	Knob, for Reset		659510850A
14	Holder		411101870A
15	Holder		411103110A
16	Sheet, Shield PAL IN		473311060A
17	Rivet, PAL IN		HARRA003SN
18	AC Cord Ass'y		M-00765
	Cord, AC KP-560 7F		311010430A
	Socket, Pin		194011670A
	Crimp, Pin		194310190A
19	Holder		411103650A
20	Clip, Fuse		197303320C
21	Heat Sink, for IC40		471010770A
22	Screw, 3x10P/Ni-3 for IC40		HMP03010SN
23	Holder		413101410A
24	PCB Ass'y, Encoder		U-25596
	Hardware Kit		HWK263334P
	Screw, Taptite 4x20PT-B/ZNY Top/Bottom		HCPB4020SY
	Screw, Taptite 4x25PT-B/ZNY Top/Bottom		HCPB4025SY

MISCELLANEOUS

Ref. No.	Description	RS Part No.	Mfr's Part No.
	Cord, Patch RCA-PAL L3.7M 2.5C2		313510120A
	Connector, Pin for Power Transformer		194101351A


23
24
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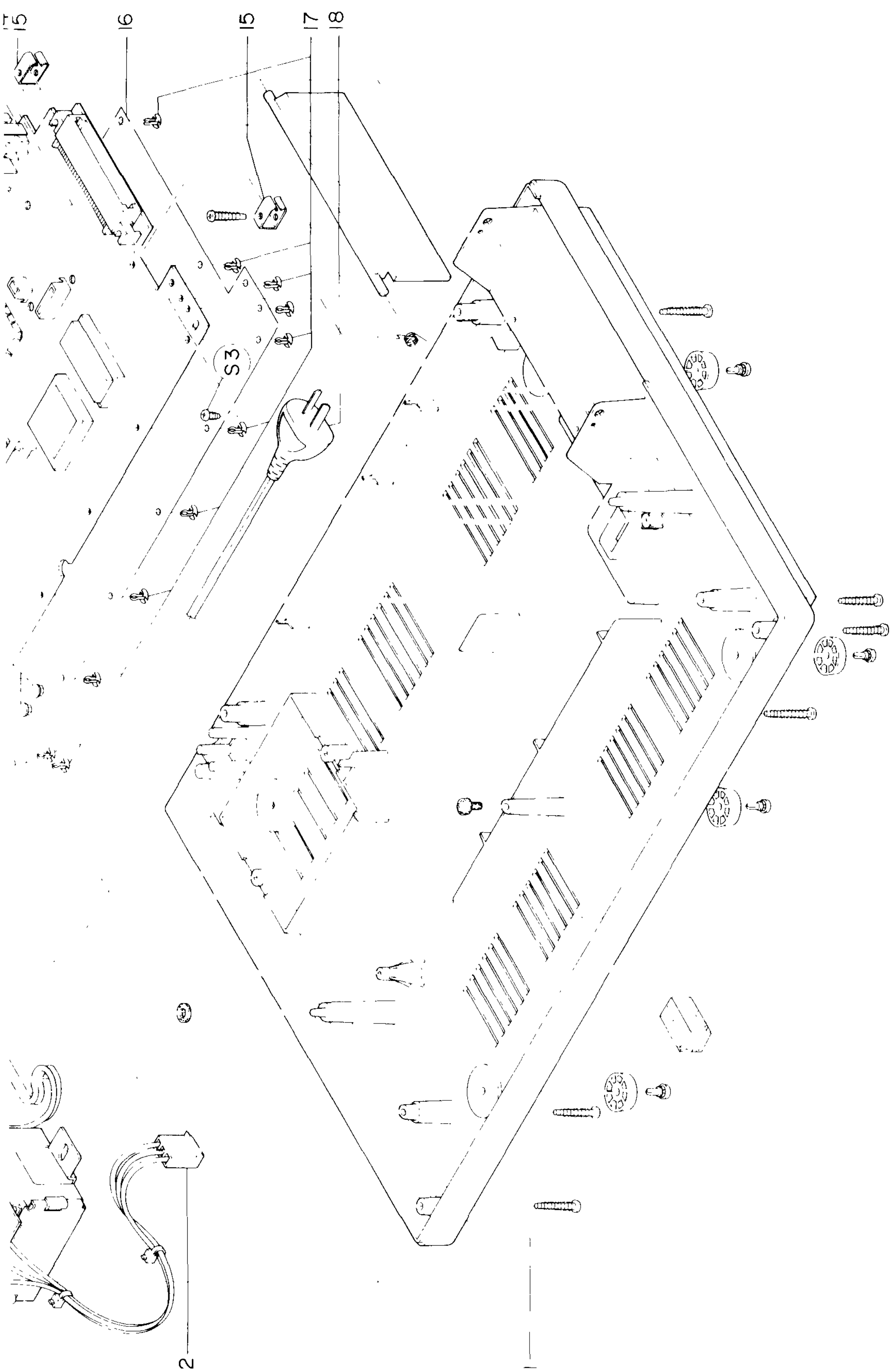
128K
COLOR COMPUTER 3

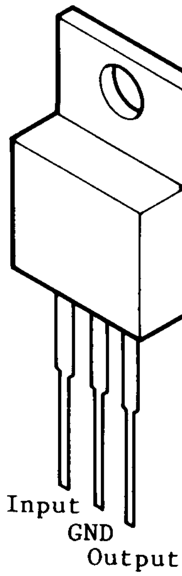
PAL

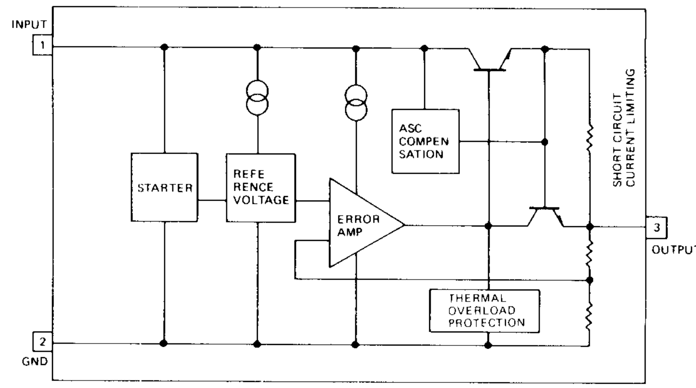


SEMICONDUCTOR INFORMATION

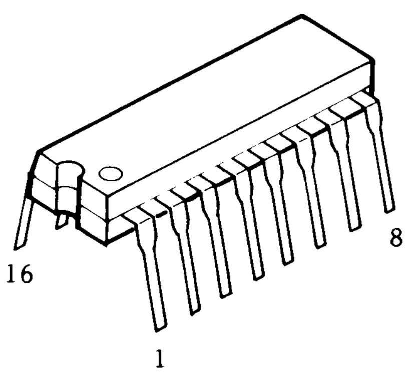
This section contains ICs and Transistors which differ from the NTSC version.

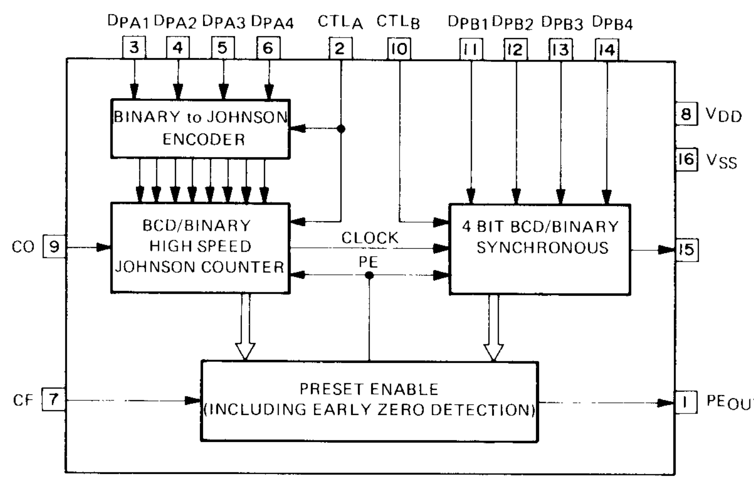
IC40: MC7812CT



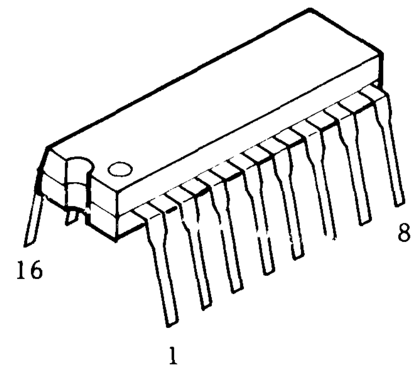


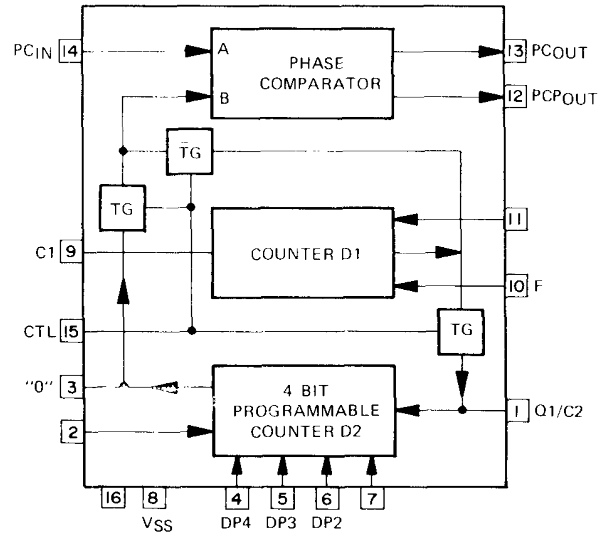
IC101: MC14569BCP



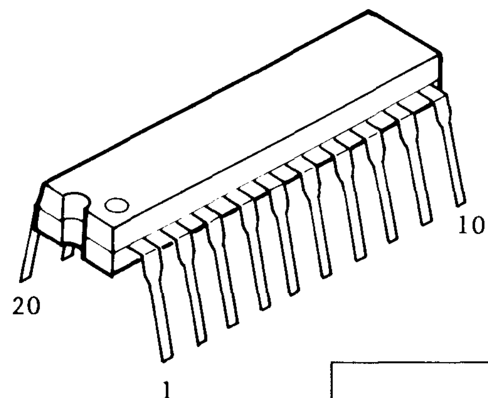


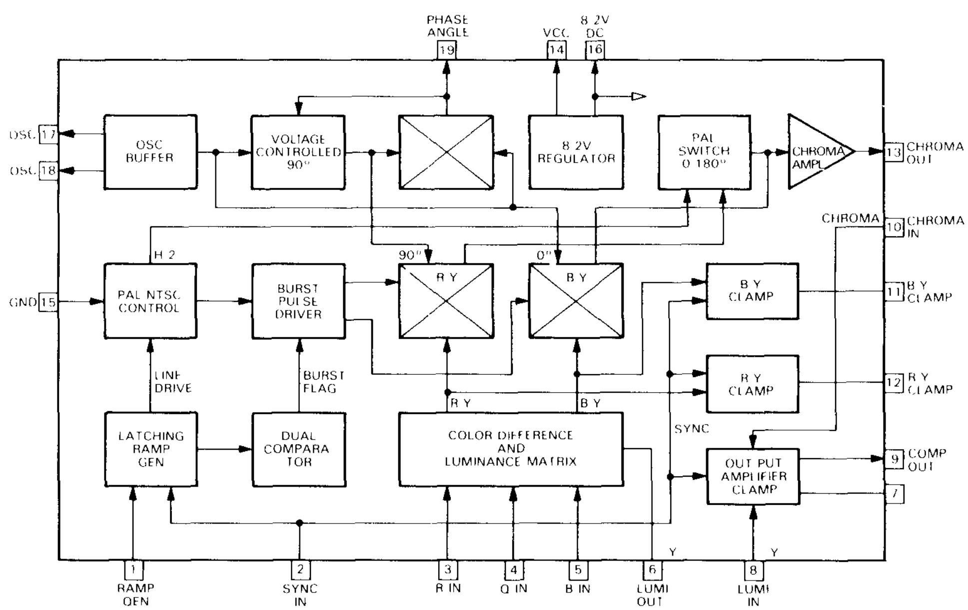
IC102: MC14568BCP





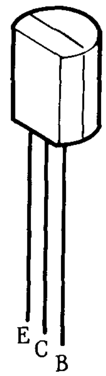
IC103: MC1377P



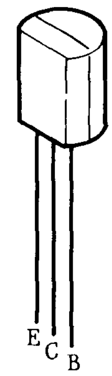


PAL

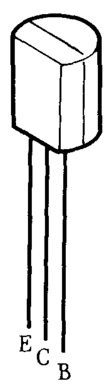
Q2,Q3,Q5-Q7: 2SC1730



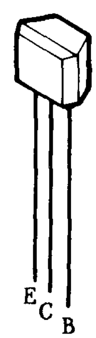
Q11,Q101: 2SC536



Q102: 2SC1674



Q103: 2SC2786

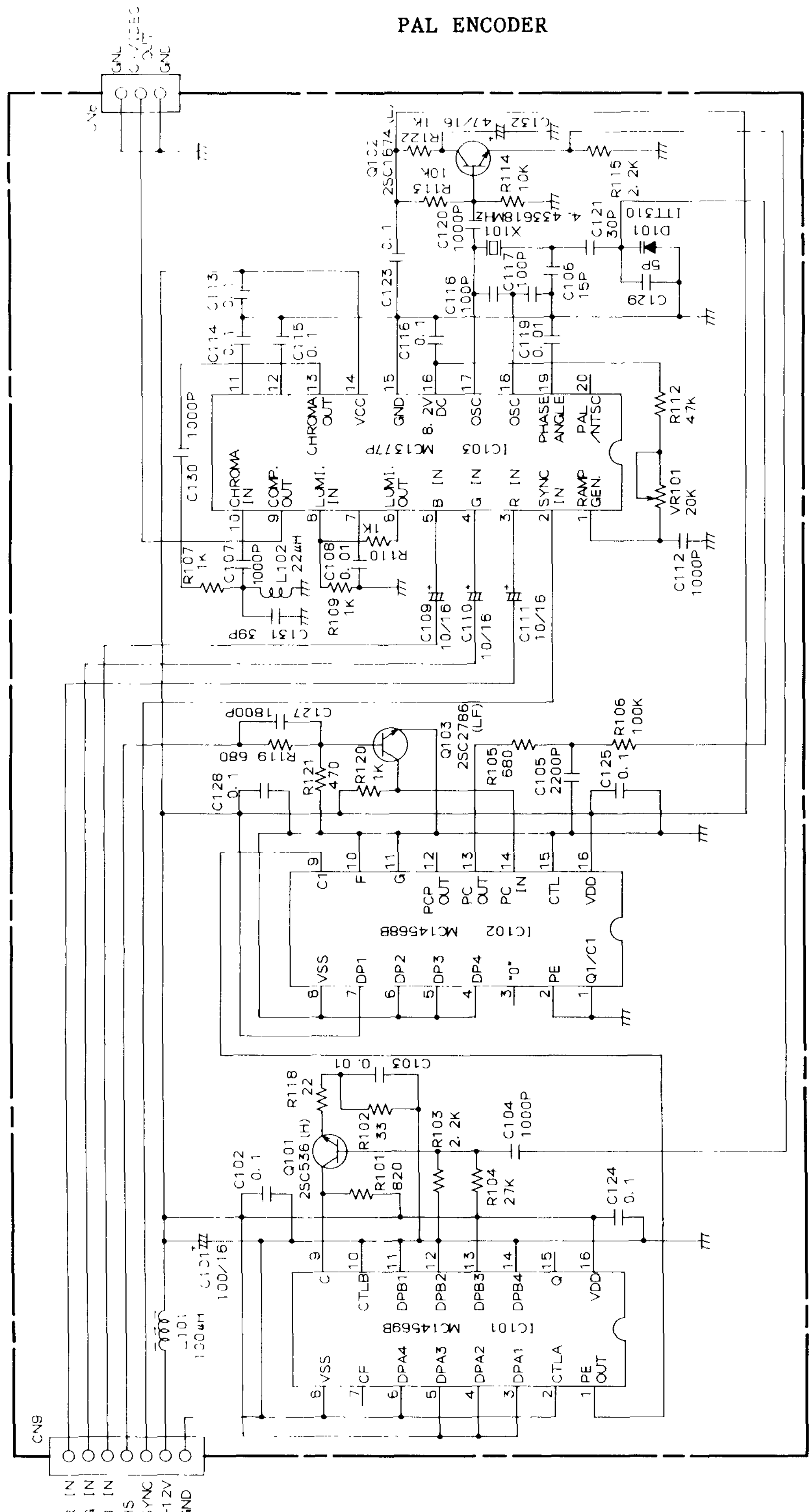


PAL

SCHEMATIC DIAGRAM

Cat. No. 26-3334

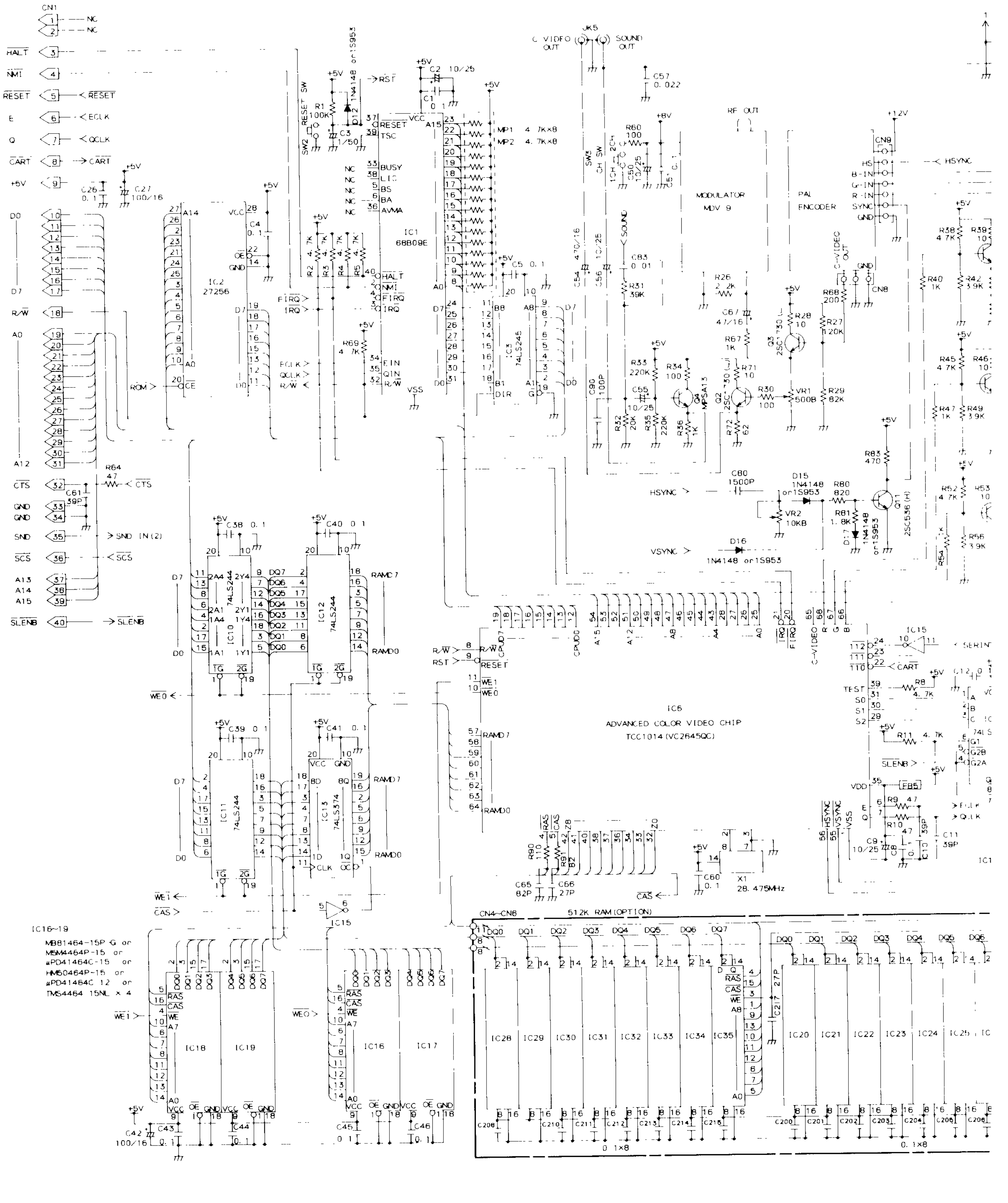
PAL ENCODER



NOTES (1) ALL RESISTANCE VALUES ARE INDICATED IN "OHM" ($K=10^3$ OHM).

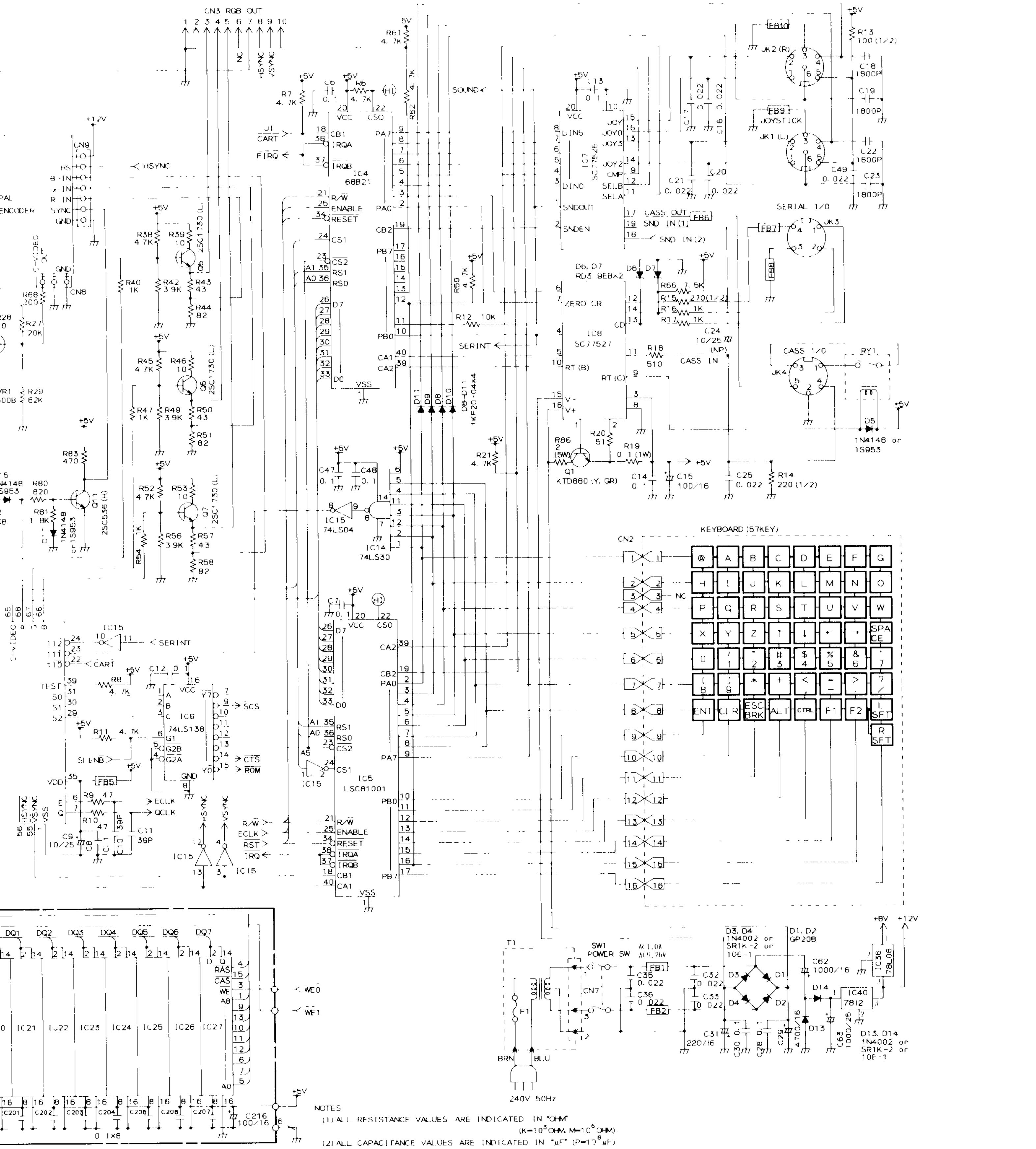
(2) ALL CAPACITANCE VALUES ARE INDICATED IN "μF" ($P=10^{-6}$ μF).

SCHEMATIC DIAGRAM



ATIC DIAGRAM

Cat. No. 26-3334



NOTES
(1) ALL RESISTANCE VALUES ARE INDICATED IN "OHM" ($K=10^3$ OHM, $M=10^6$ OHM).
(2) ALL CAPACITANCE VALUES ARE INDICATED IN "μF" ($P=10^{-6}\mu F$)

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