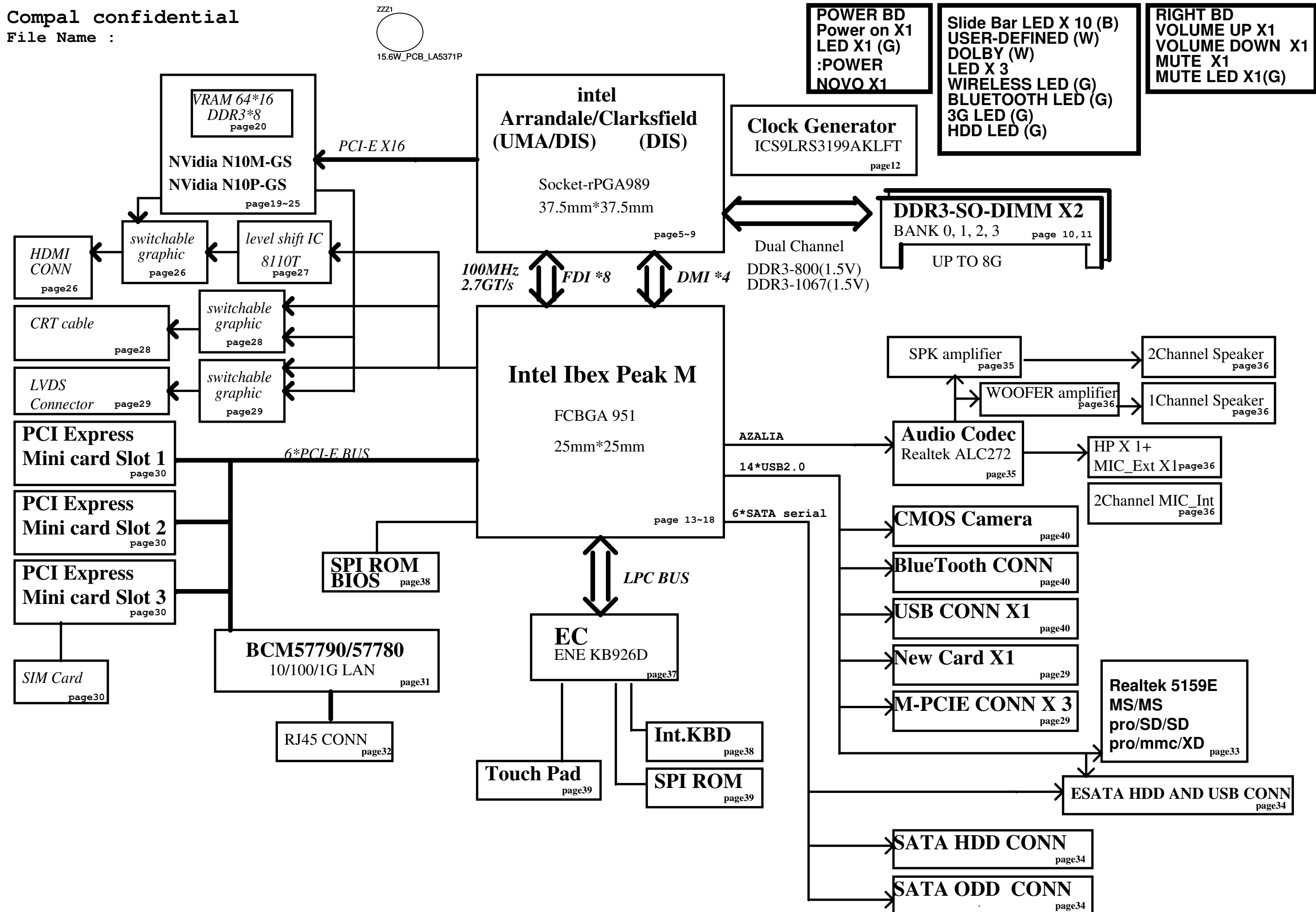
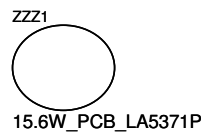


Compal Confidential
Schematics Document
Arrandale/Clarksville
with Intel IBEX PEAK-M core logic
NIWBA

REV: 0.1

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			Size Custom	Document Number
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MB Block Diagram
 Rev 0.1
 Tuesday, March 24, 2009

DDR3 Voltage Rails

power plane	+B	+5VALW	+1.5V	+5VS
				+3VS
State		+3VALW		+1.5VS
				+VCCP
				+CPU_CORE
				+VGA_CORE
				+1.8VS
				+0.75VS
				+1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	RAM M2	BATT	KE926	SODIMM	CLK CHIP	WLAN WWAN	N10x Thermal Sensor	N10x	Cap sensor board	NEW CARD	PCH
SMB_EC_CK1	KB926	X	V	X	X	X	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW									
SMB_EC_CK2	KB926	X	X	X	X	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW											+3VALW
SMBCLK	PCH	V	X	X	V	V	X	X	X	X	V	X
SMBDATA	+3VALW	+3VALW			+3VS	+3VS					+3VS	
SML0CLK	PCH	X	X	X	X	X	X	X	X	X	X	X
SML0DATA	+3VALW											
SML1CLK	PCH	X	X	V	X	X	X	V	X	V	X	X
SML1DATA	+3VALW			+3VALW				+3VS		+3VS		

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

@ FUNCTION

EVT		NON-USE	
45@	(45 BOM)		
GIGA@	(GIGA LAN)	100@	(100 LAN)
NO TVSW@	(NON TV POWER SW)	TVSW@	(TV POWER SW)
ARRAY@	(ARRAY MIC)	MONO@	(MONO MIC)
S512@	FOR X76 BOM		
H512@	FOR X76 BOM		
S1024@	FOR X76 BOM		
H1024@	FOR X76 BOM		
X76@	(X76 BOM)		
M1@	(DDR M1 MODE)		
3G@	(3G MODE)		
10M@	FOR 10M CHIP		
10P@	FOR 10P CHIP		
UMA@	FOR Auberndale		
DIS@	FOR Auberndale/Clarksfield		
VGA@	FOR NVIDIA PART		

PORT	DEVICE
1	NEW CARD
2	WLAN
3	LAN
4	3G
5	
6	TV TUNNER
7	
8	

PORT	DEVICE
0	LEFT SIDE
1	RIGHT SIDE
2	CMOS
3	
4	RIGHT SIDE
5	CARD READER
6	
7	
8	WIRELESS
9	TV TUNNER
10	NEW CARD
11	BT
12	
13	3G

VGA and DDR3 Voltage Rails (N10x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	GPU VID2
GPIO8	I/O	L	Thermal Catastrophic Overtemp
GPIO9	OUT	L	Thermal Alert
GPIO10	OUT		Memory VREF switch
GPIO11	I/O	L	SLI raster sync
GPIO12	IN	-	AC power detect pin
GPIO13	OUT	-	MEM_VID or Power supply control
GPIO14	OUT	-	Power supply control
GPIO15	IN	-	Hot plug detect for IFP Link E
GPIO16	OUT	-	Programmable Fan Control
GPIO17	IN	-	
GPIO18	IN	-	
GPIO19	IN	-	Hot plug detect for IFP Link D
GPIO20	IN	-	
GPIO21	IN	-	Hot plug detect for IFP link F
GPIO22	IN	-	SLI swap ready signal
GPIO23	I/O		

GPIO6	GPIO5	N10M-GS	N10P-GS
GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.8V	12
0	1	0.85V	12
1	1	0.9V	0, 10

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

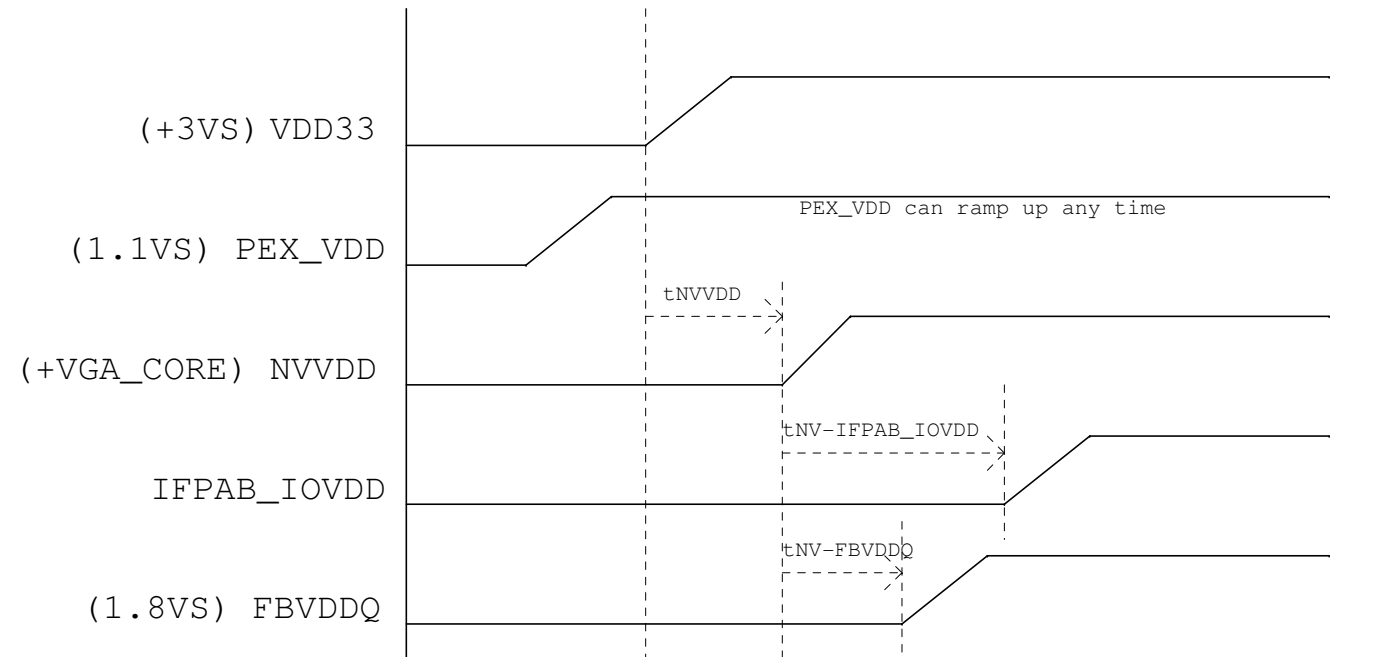
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.5V)		FBVDDQ (GPU+Mem) (1.5V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N10P-GS 128bit 1024MB DDR3	21.07	6.67	TBD	TBD	18.25	17.34	2.06	3.09	4.09	6.14	850	0.89	75	0.14	63	0.07	55	0.18
N10P-GE 128bit 1024MB DDR3	20.97	6.73	TBD	TBD	19.17	17.25	2.03	3.05	4.09	6.14	840	0.88	75	0.14	63	0.07	55	0.18
N10P-LP 128bit 1024MB DDR3	15.48	6.44	TBD	TBD	13.95	11.86	1.90	2.85	3.99	5.99	810	0.85	75	0.14	63	0.07	55	0.18

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.5V)		FBVDDQ (GPU+Mem) (1.5V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N10M-GE 64bit 512MB DDR3	13.36	2.93	TBD	TBD	11.89	10.70	0.66	0.99	2.16	3.24	792	0.83	75	0.14	63	0.07	100	0.33
N10M-GS 64bit 512MB DDR3	14.29	3.10	TBD	TBD	11.53	11.53	0.70	1.05	2.28	3.42	817	0.86	75	0.14	63	0.07	100	0.33
N10M-LP 64bit 512MB DDR3	8.28	2.91	TBD	TBD	6.60	5.61	0.62	0.93	2.20	3.3	782	0.82	75	0.14	63	0.07	100	0.33

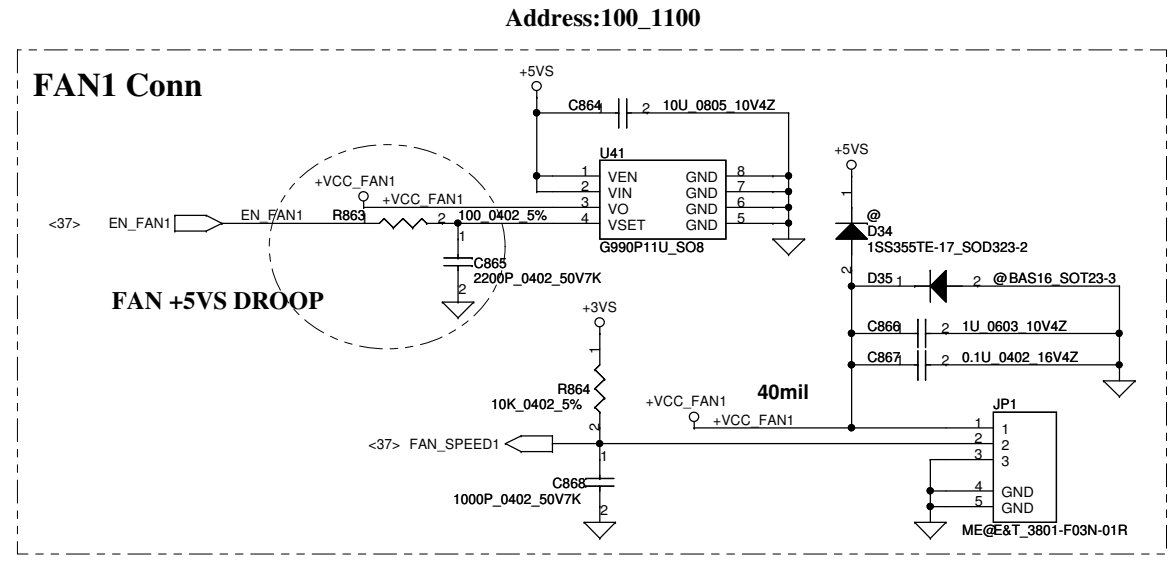
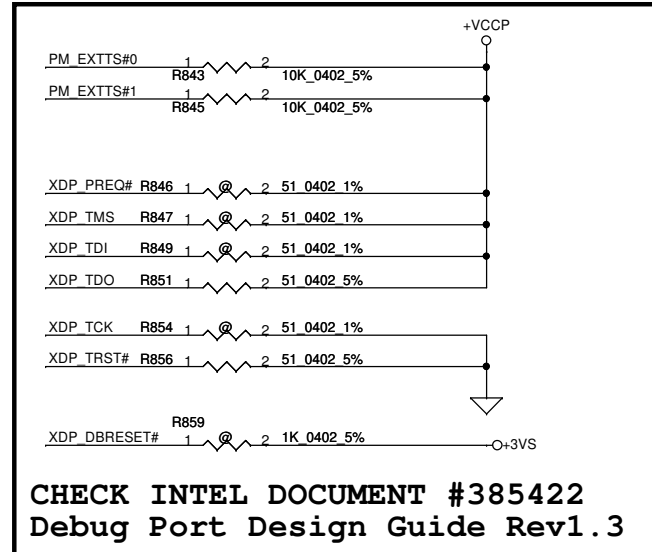
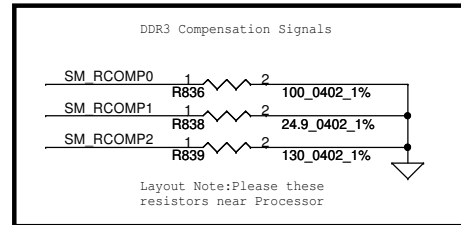
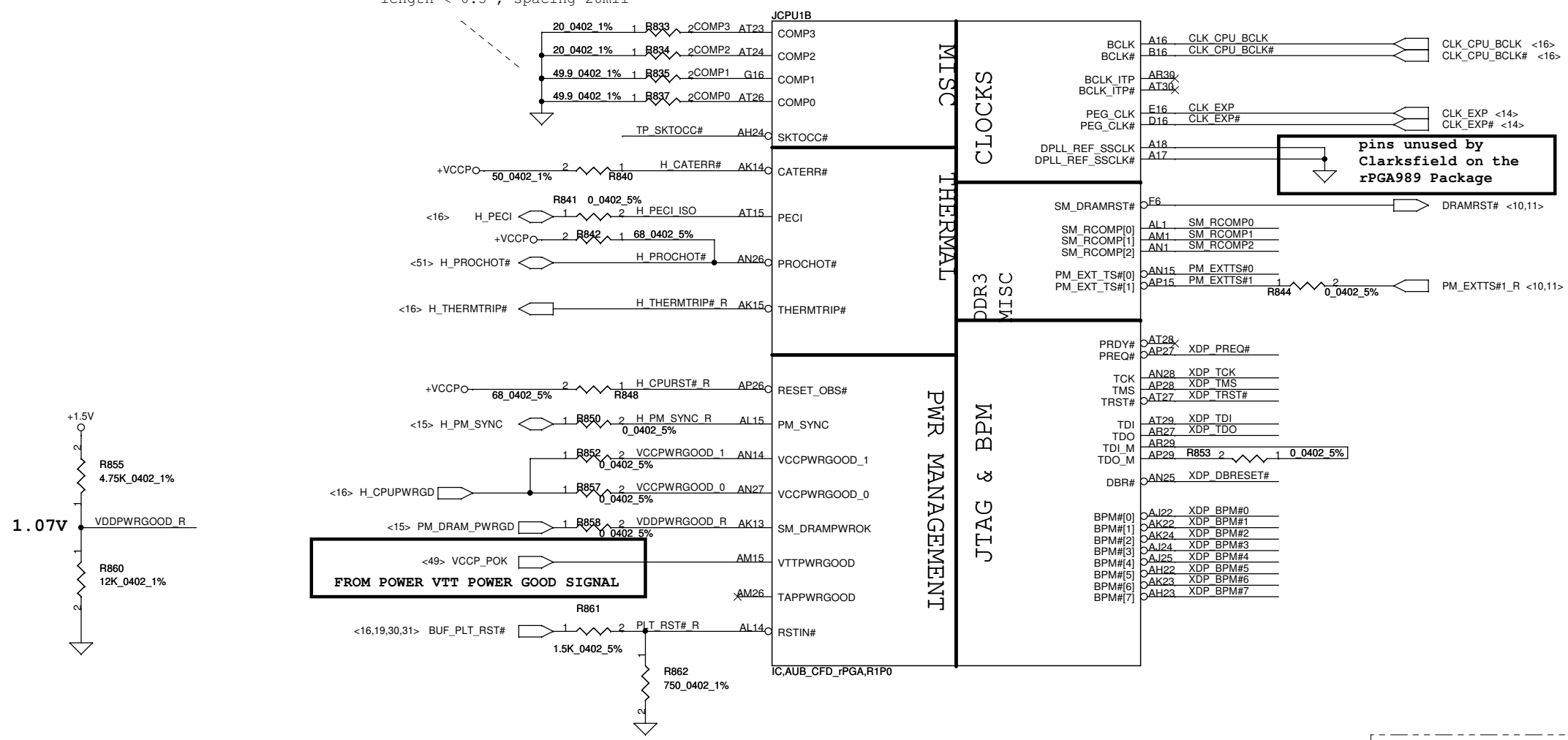
Power Sequence

The ramp time for any rail must be more than 40us



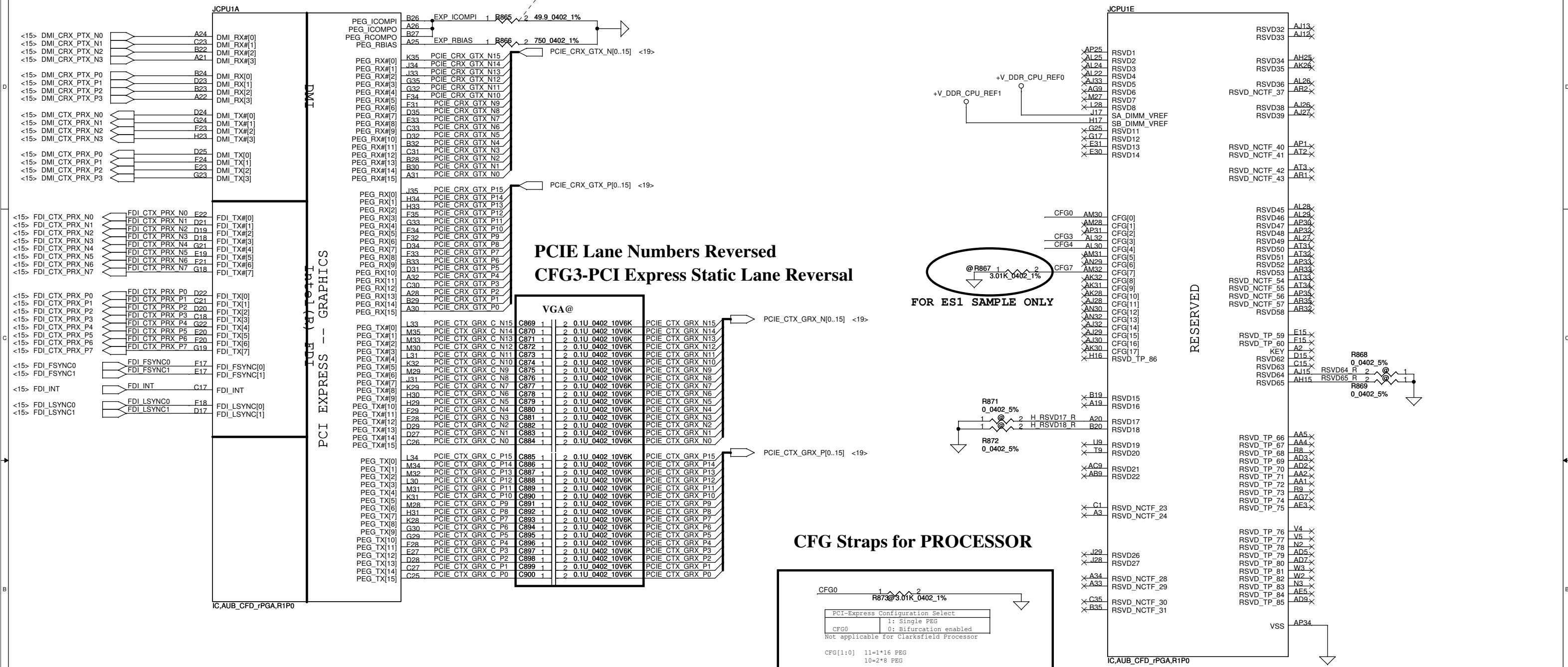
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Layout rule : 10mil width trace
length < 0.5", spacing 20mil



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Layout rule : trace length < 0.5"

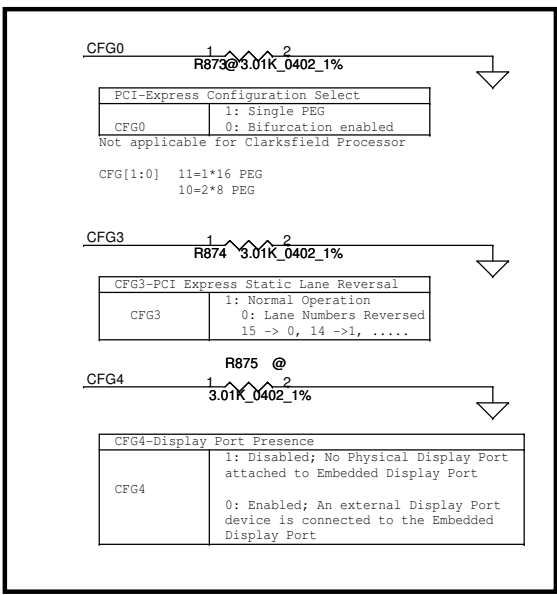


**PCIE Lane Numbers Reversed
CFG3-PCI Express Static Lane Reversal**

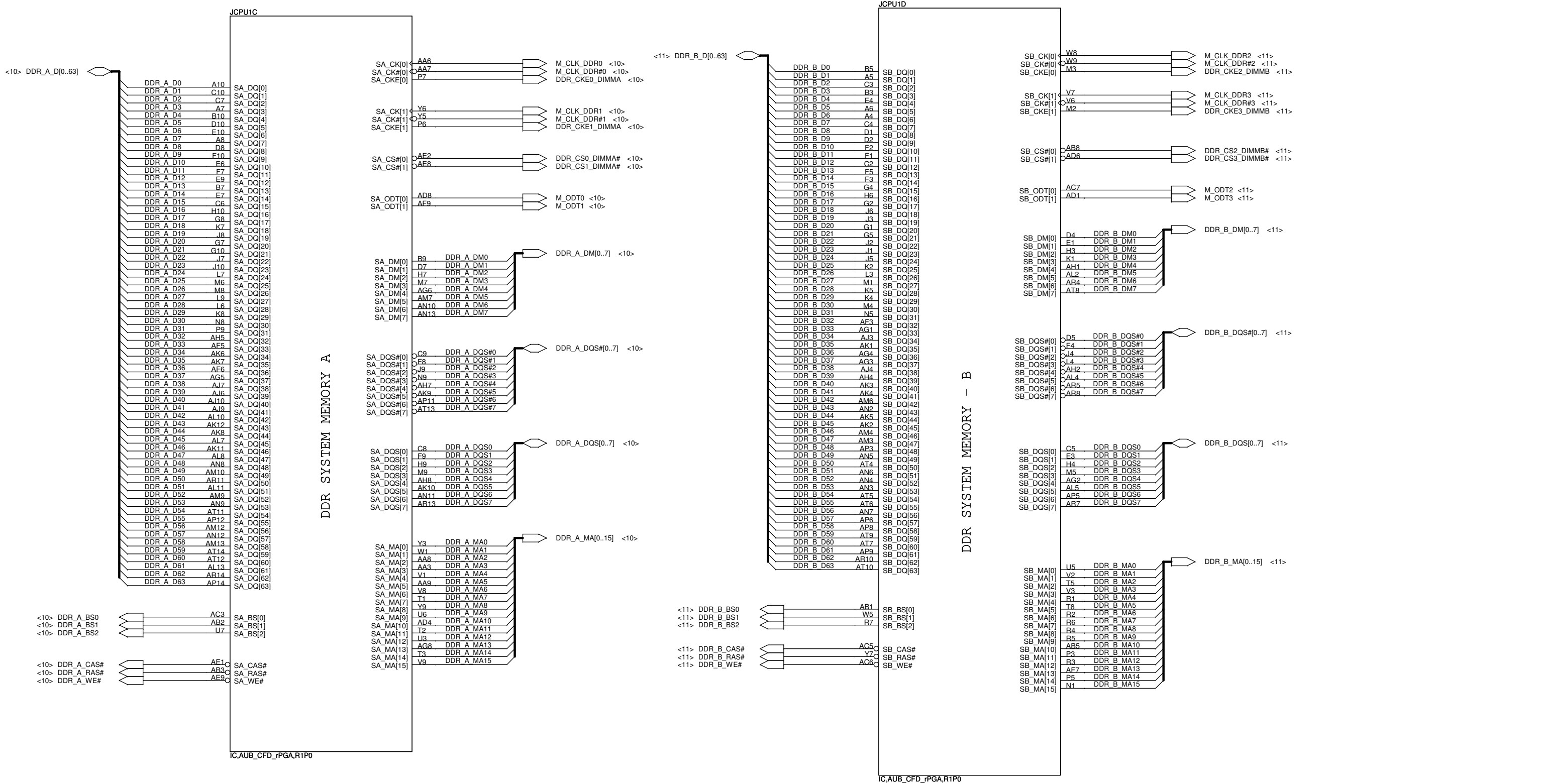
VGA@		PCIE CTX GRX N[0..15] <19>		PCIE CTX GRX P[0..15] <19>	
L33	PCIE CTX GRX C N15	C869	1	2	0.1U 0402 10V6K
M35	PCIE CTX GRX C N14	C870	1	2	0.1U 0402 10V6K
M33	PCIE CTX GRX C N13	C871	1	2	0.1U 0402 10V6K
M30	PCIE CTX GRX C N12	C872	1	2	0.1U 0402 10V6K
L31	PCIE CTX GRX C N11	C873	1	2	0.1U 0402 10V6K
M29	PCIE CTX GRX C N10	C874	1	2	0.1U 0402 10V6K
K32	PCIE CTX GRX C N9	C875	1	2	0.1U 0402 10V6K
J31	PCIE CTX GRX C N8	C876	1	2	0.1U 0402 10V6K
K29	PCIE CTX GRX C N7	C877	1	2	0.1U 0402 10V6K
H30	PCIE CTX GRX C N6	C878	1	2	0.1U 0402 10V6K
H29	PCIE CTX GRX C N5	C879	1	2	0.1U 0402 10V6K
F29	PCIE CTX GRX C N4	C880	1	2	0.1U 0402 10V6K
F28	PCIE CTX GRX C N3	C881	1	2	0.1U 0402 10V6K
D29	PCIE CTX GRX C N2	C882	1	2	0.1U 0402 10V6K
D27	PCIE CTX GRX C N1	C883	1	2	0.1U 0402 10V6K
C26	PCIE CTX GRX C N0	C884	1	2	0.1U 0402 10V6K
L34	PCIE CTX GRX C P15	C885	1	2	0.1U 0402 10V6K
M34	PCIE CTX GRX C P14	C886	1	2	0.1U 0402 10V6K
M32	PCIE CTX GRX C P13	C887	1	2	0.1U 0402 10V6K
L30	PCIE CTX GRX C P12	C888	1	2	0.1U 0402 10V6K
M31	PCIE CTX GRX C P11	C889	1	2	0.1U 0402 10V6K
K31	PCIE CTX GRX C P10	C890	1	2	0.1U 0402 10V6K
M28	PCIE CTX GRX C P9	C891	1	2	0.1U 0402 10V6K
H31	PCIE CTX GRX C P8	C892	1	2	0.1U 0402 10V6K
K28	PCIE CTX GRX C P7	C893	1	2	0.1U 0402 10V6K
G30	PCIE CTX GRX C P6	C894	1	2	0.1U 0402 10V6K
G29	PCIE CTX GRX C P5	C895	1	2	0.1U 0402 10V6K
G28	PCIE CTX GRX C P4	C896	1	2	0.1U 0402 10V6K
E27	PCIE CTX GRX C P3	C897	1	2	0.1U 0402 10V6K
D28	PCIE CTX GRX C P2	C898	1	2	0.1U 0402 10V6K
C27	PCIE CTX GRX C P1	C899	1	2	0.1U 0402 10V6K
C25	PCIE CTX GRX C P0	C900	1	2	0.1U 0402 10V6K

FOR ES1 SAMPLE ONLY

CFG Straps for PROCESSOR



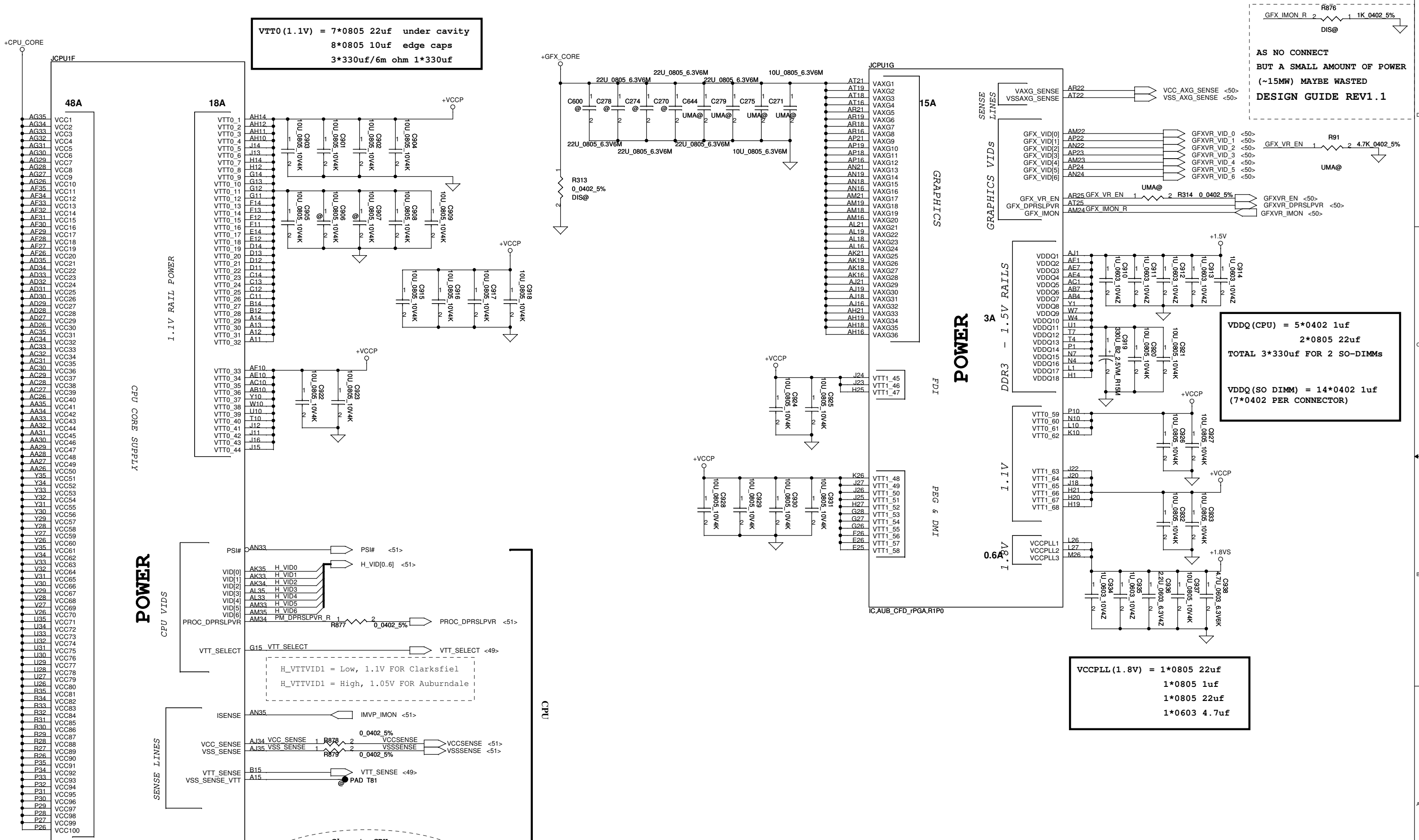
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IC,AUB_CFD_rPGA,R1P0

IC,AUB_CFD_rPGA,R1P0

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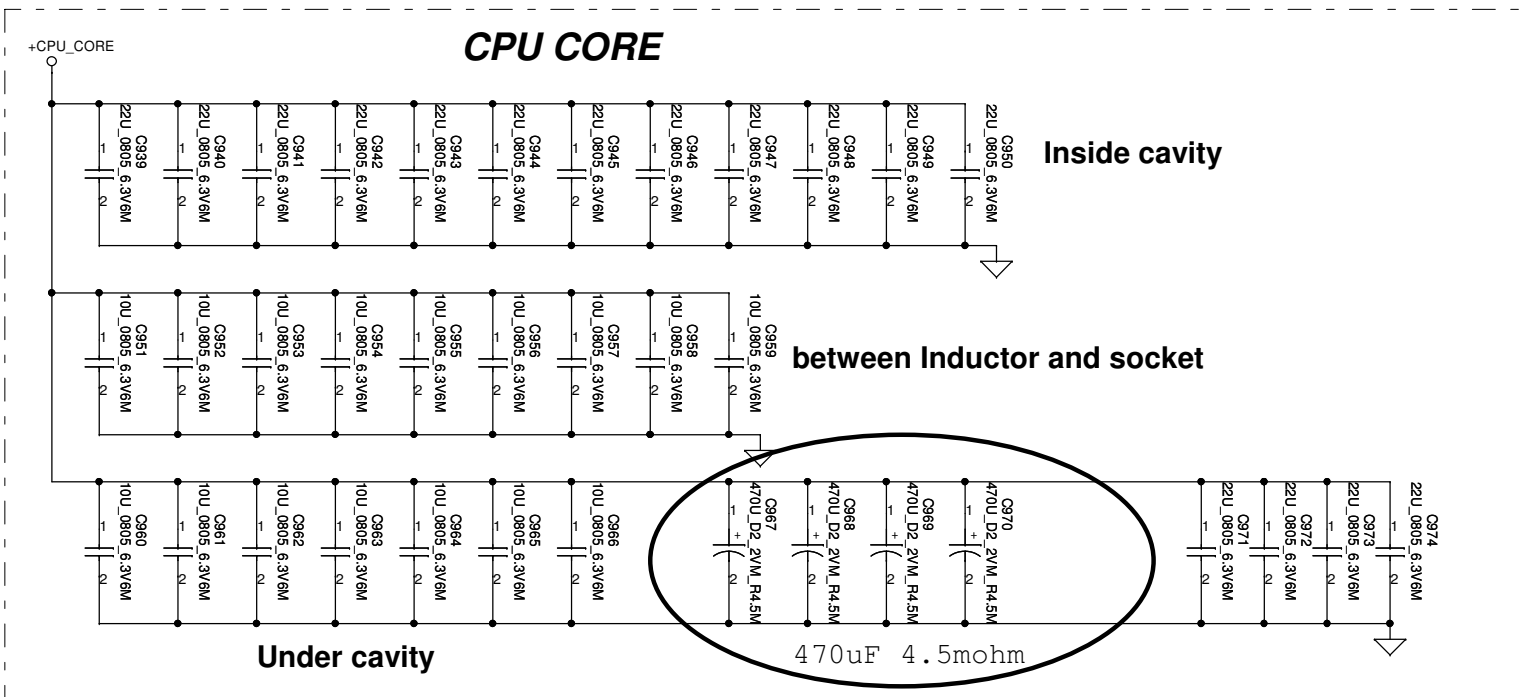
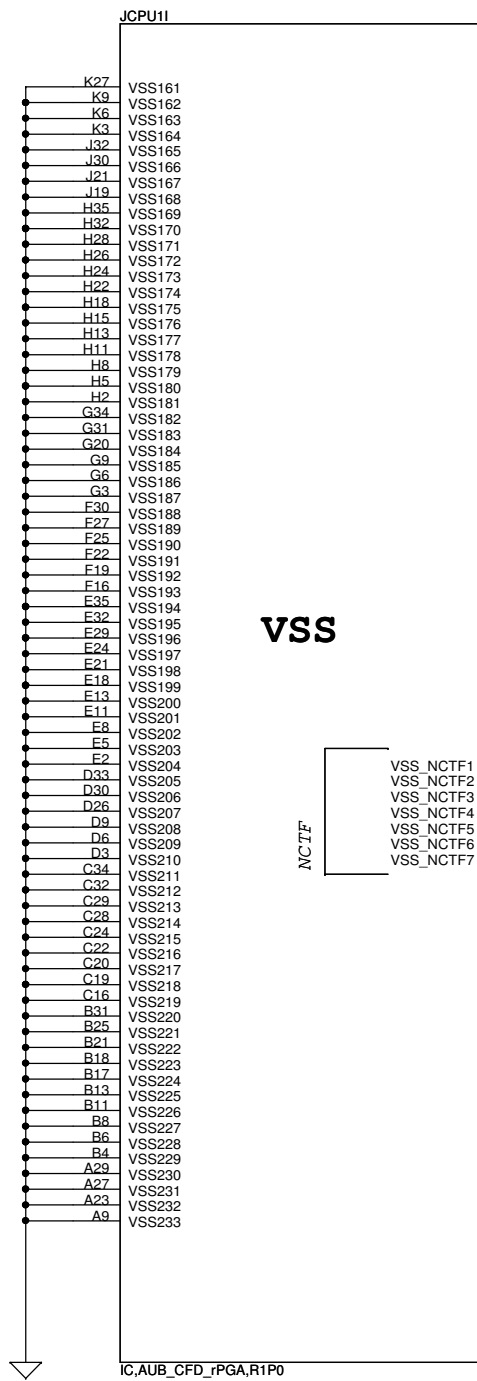
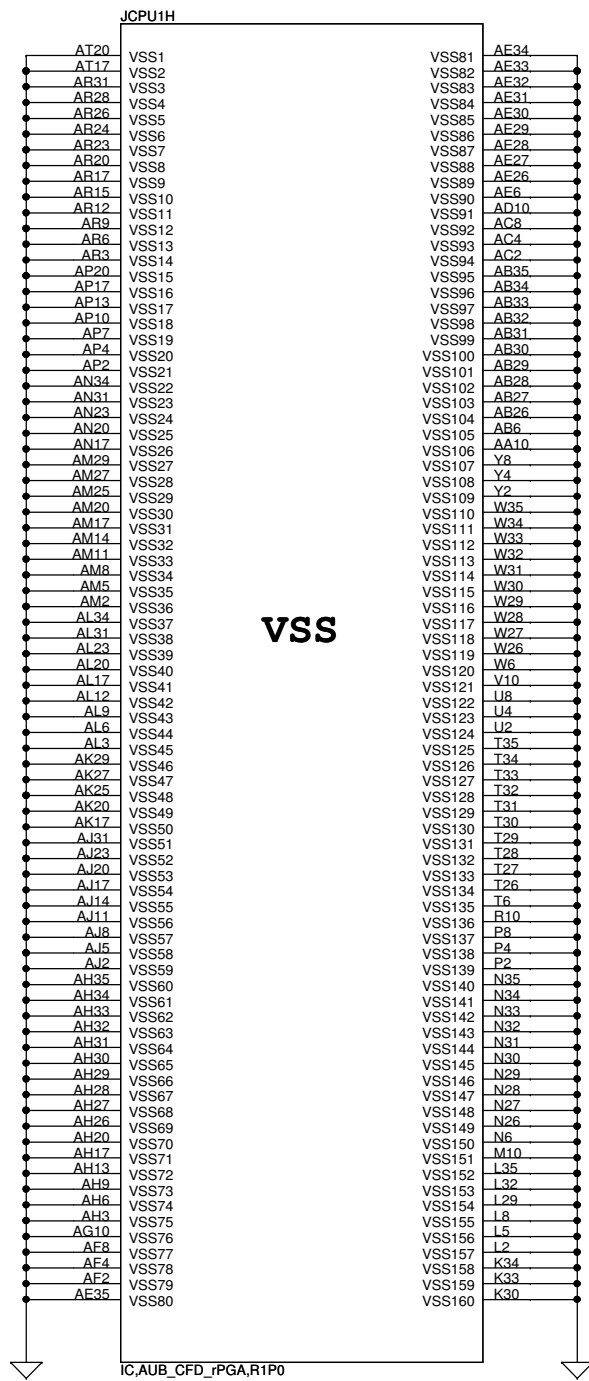
POWER

SENSE LINES

POWER

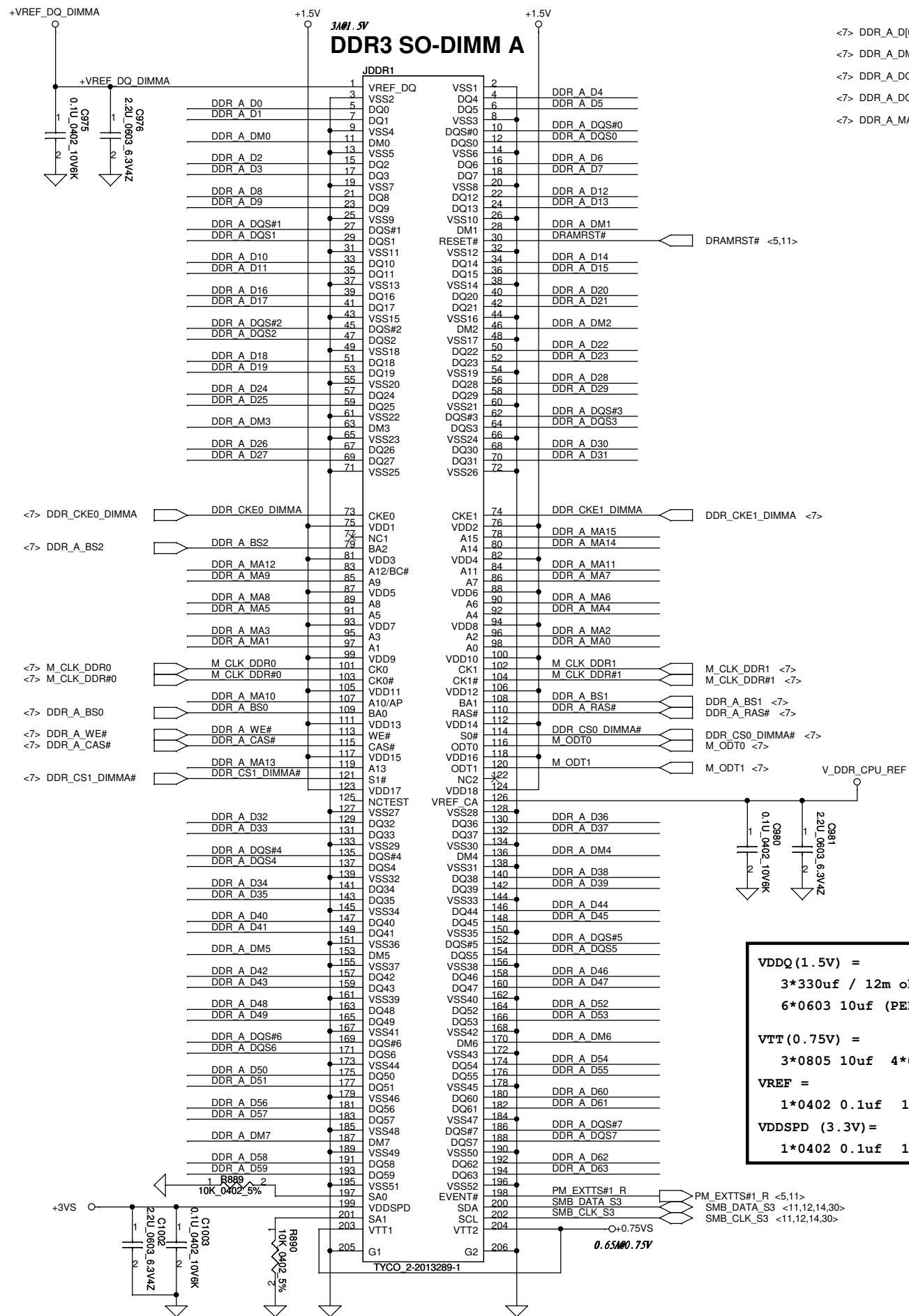
SENSE LINES

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Size Custom	Document Number	Rev		0.2	
	NIWBA_LA5371P				
Date:	Tuesday, March 24, 2009	Sheet	8	of	52

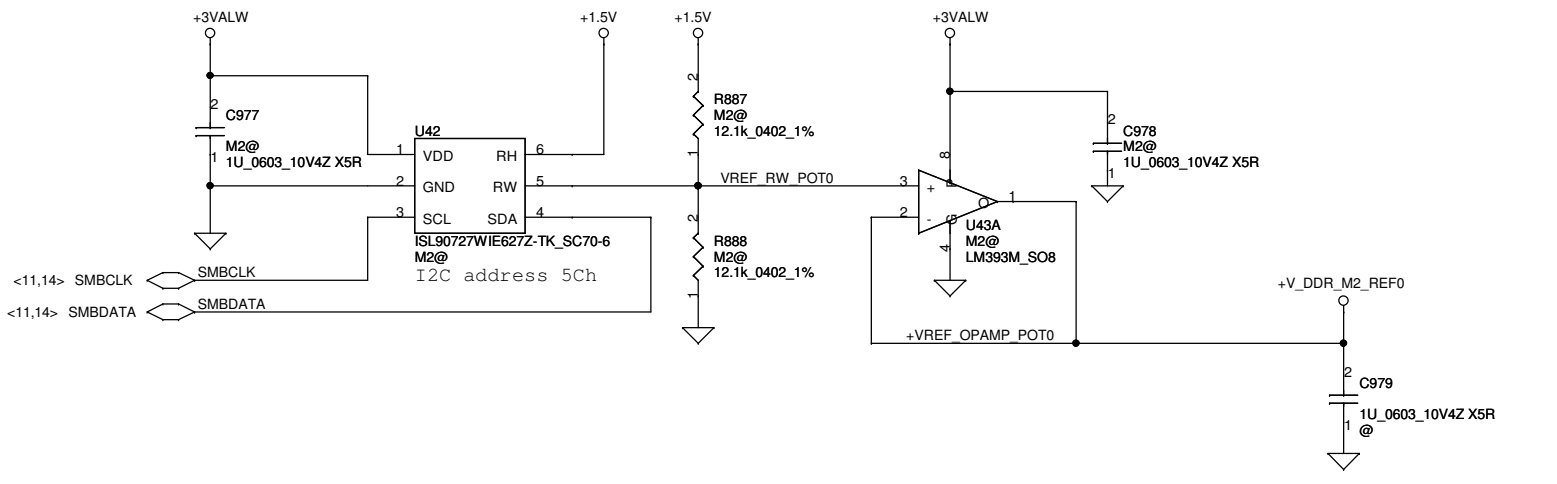
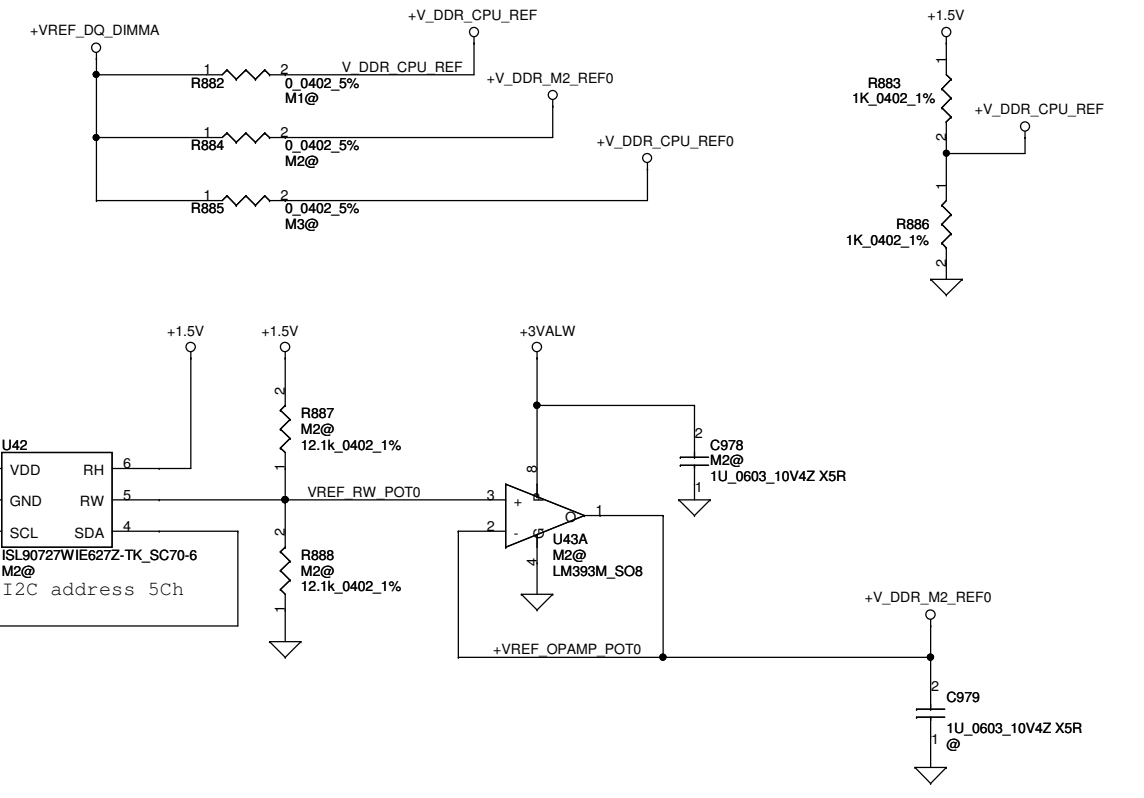


+CPU_CORE = 12*0805 22uf INSIDE CAVITY
7*0805 10uf UNDER CAVITY AND 9*0805 10uf BETWEEN INDUCTOR AND SOCKET ON TOP LAYER
4*470uf/4m ohm 2*470uf

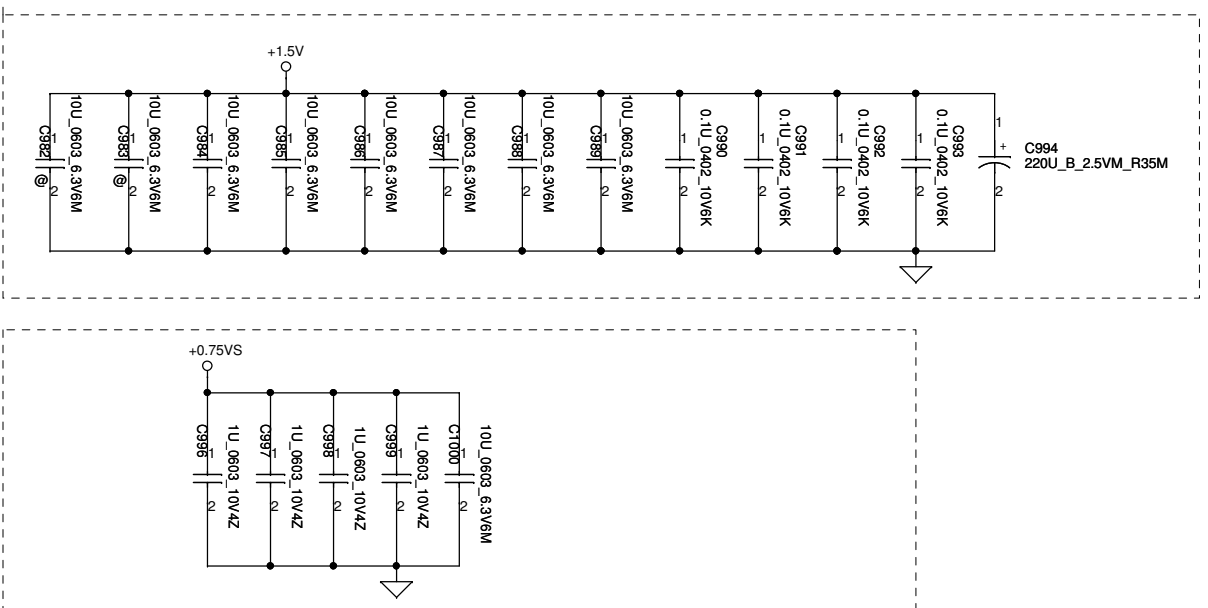
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Size	Custom	Document Number	NIWBA_LA5371P		Rev 0.2
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- <7> DDR_A_D[0..63]
- <7> DDR_A_DM[0..7]
- <7> DDR_A_DQS[0..7]
- <7> DDR_A_DQS#[0..7]
- <7> DDR_A_MA[0..15]



Layout Note:
Place near DIMM



VDDQ (1.5V) =
 3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
 6*0603 10uf (PER CONNECTOR)

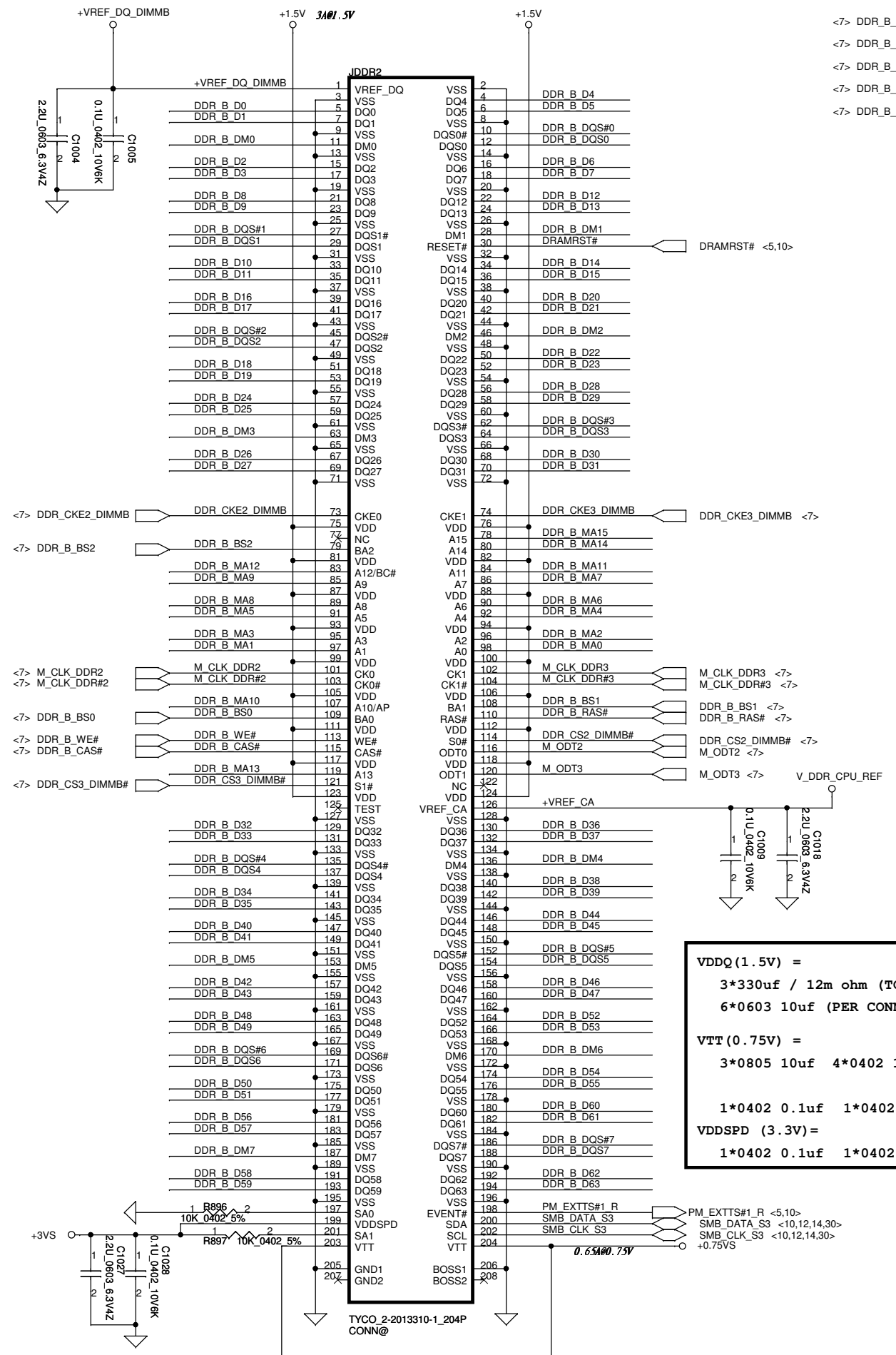
VTT (0.75V) =
 3*0805 10uf 4*0402 1uf

VREF =
 1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V) =
 1*0402 0.1uf 1*0402 2.2uf

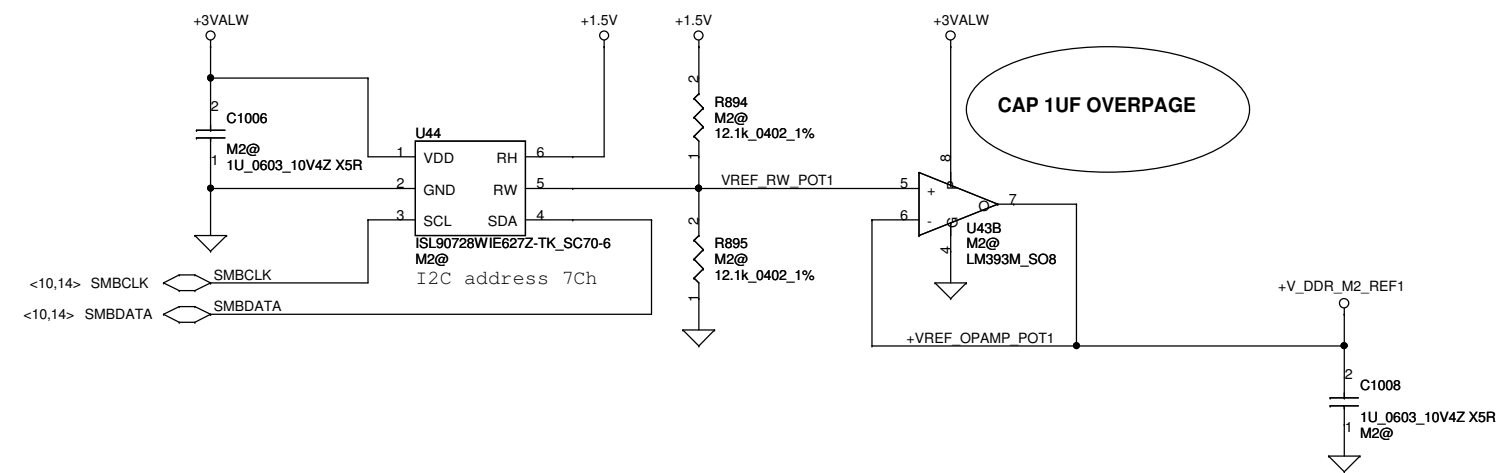
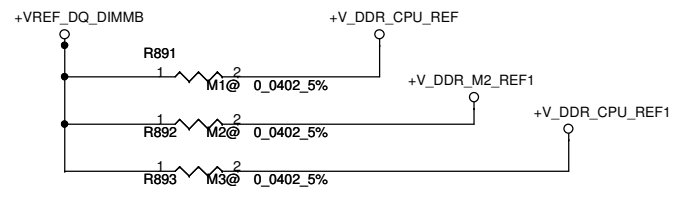
TOP SLOT

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Date:	Tuesday, March 24, 2009	Sheet	10	of	52

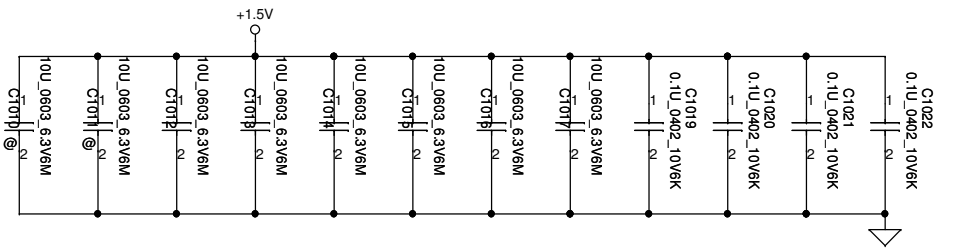


BOT SLOT

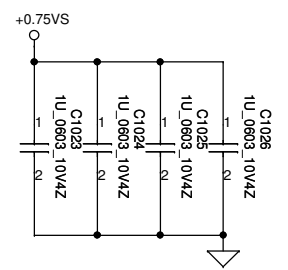
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- <7> DDR_B_D[0..63]
- <7> DDR_B_DM[0..7]
- <7> DDR_B_DQS#0..7
- <7> DDR_B_MA[0..15]



Layout Note:
Place near DIMM



Layout Note:
Place near DIMM



VDDQ (1.5V) =
 $3 \times 330\text{uF} / 12\text{m ohm (TOTAL FOR 2 SO-DIMMs)}$
 $6 \times 0603 10\text{uF (PER CONNECTOR)}$

VTT (0.75V) =
 $3 \times 0805 10\text{uF} \quad 4 \times 0402 1\text{uF}$

VDDSPD (3.3V) =
 $1 \times 0402 0.1\text{uF} \quad 1 \times 0402 2.2\text{uF}$
 $1 \times 0402 0.1\text{uF} \quad 1 \times 0402 2.2\text{uF}$

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Issued Date	2008/10/31	Deciphered Date	2009/10/31	Compal Electronics, Inc.	
				DDR3-SODIMM SLOT2	
Size	Document Number	Rev			
	NIWBA_LA5371P	0.2			
Date:	Tuesday, March 24, 2009	Sheet	11	of 52	

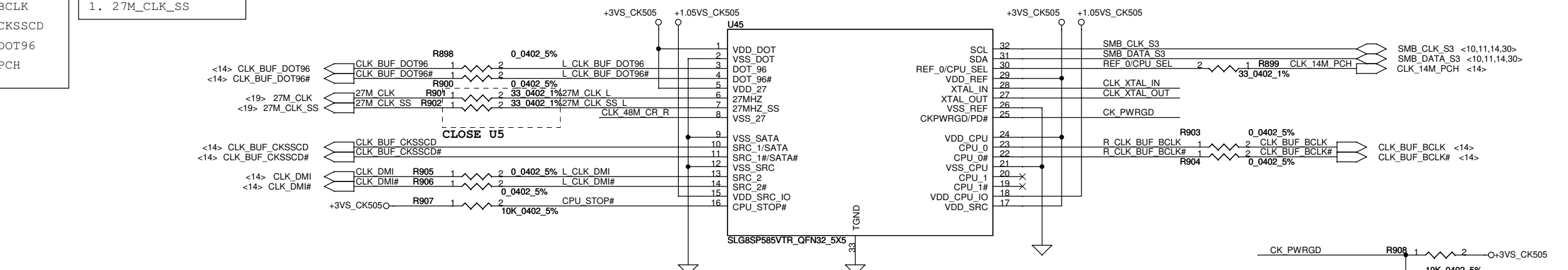
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CLK GEN TO PCH

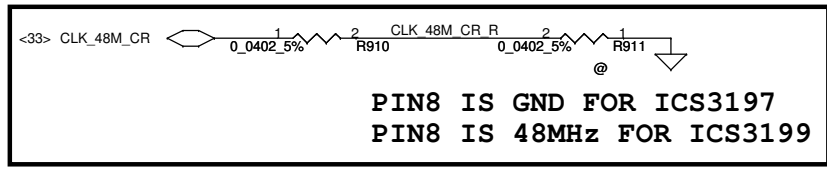
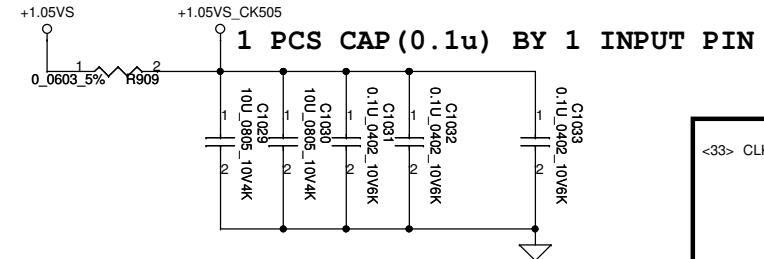
1. CLK_DMI
2. CLK_BUF_BCLK
3. CLK_BUF_CKSSCD
4. CLK_BUF_DOT96
5. CLK_14M_PCH

CLK GEN TO VGA

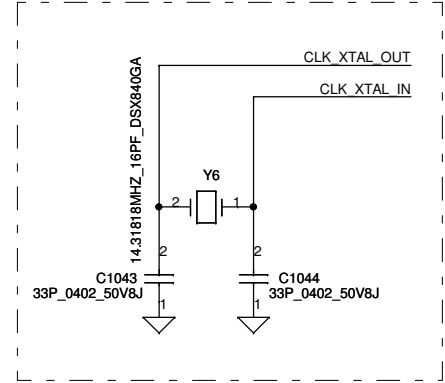
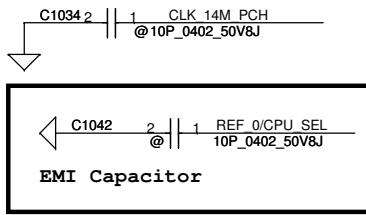
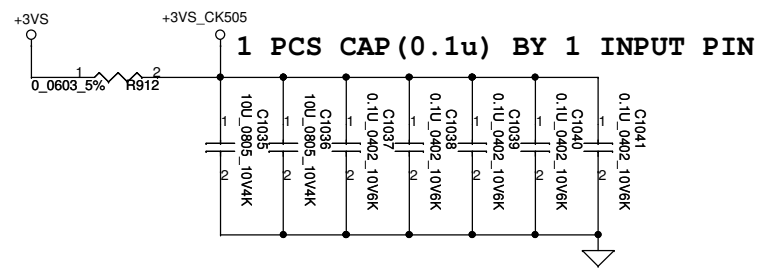
1. 27M_CLK
1. 27M_CLK_SS



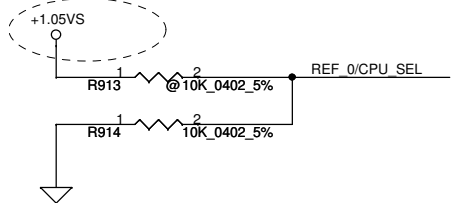
S IC ICS9LRS3199AKLFT MLF 32P CLK GEN (SA000030P00)



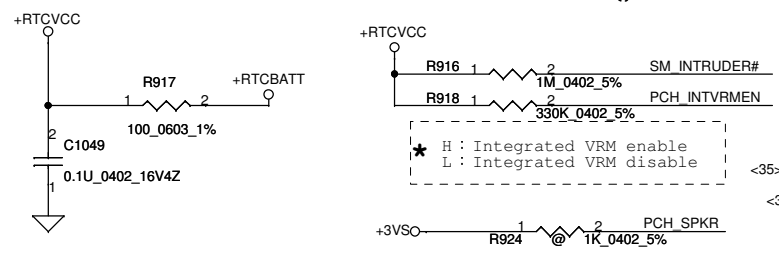
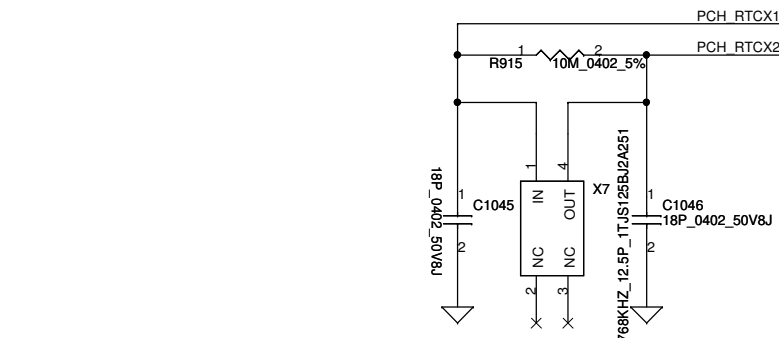
**PIN8 IS GND FOR ICS3197
PIN8 IS 48MHz FOR ICS3199**



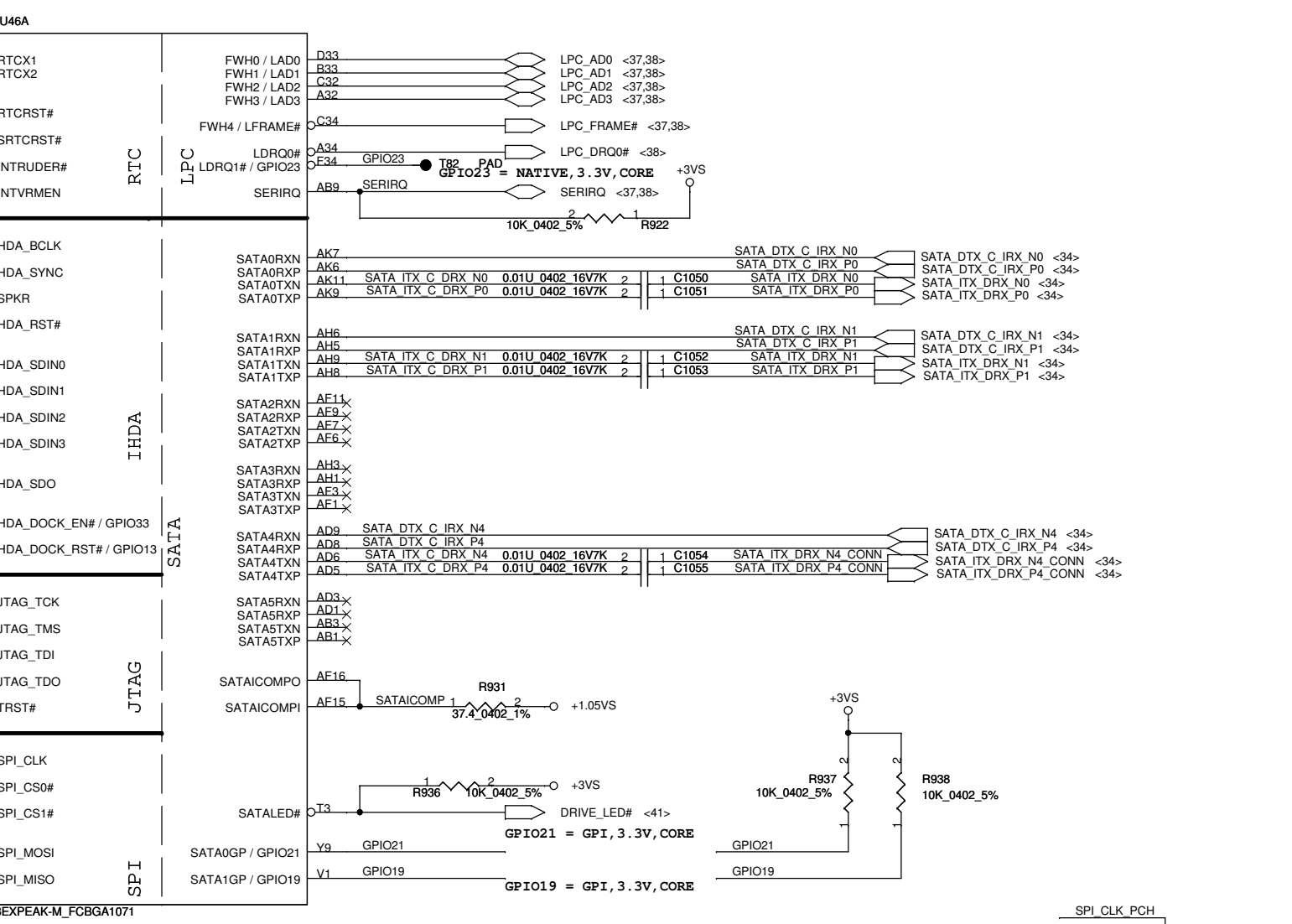
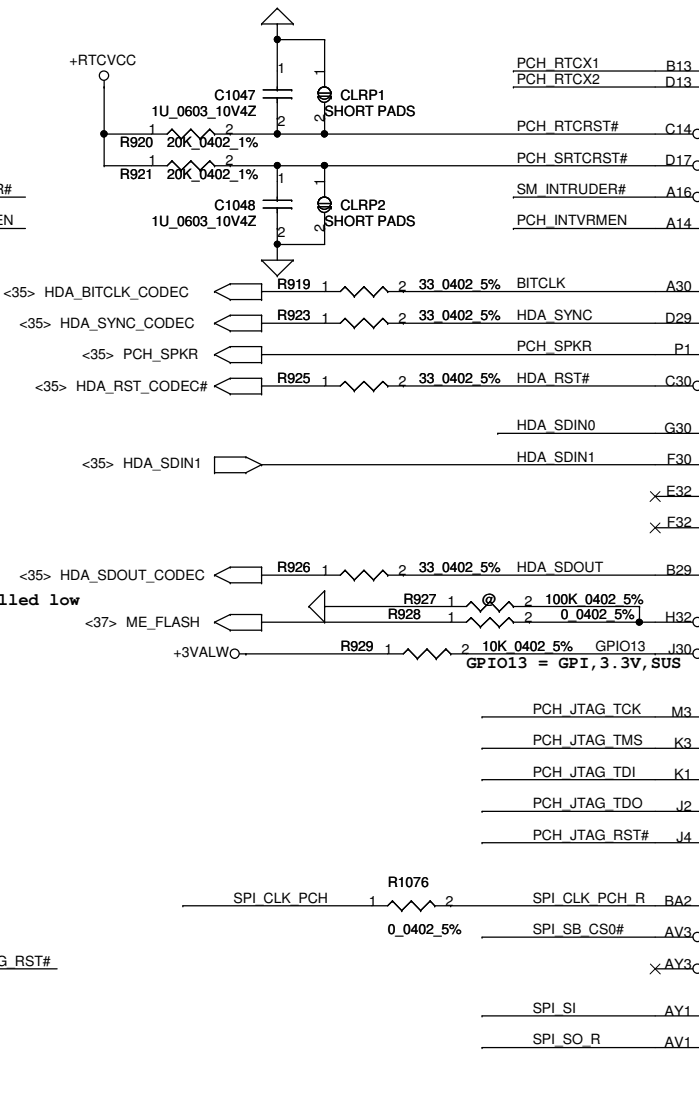
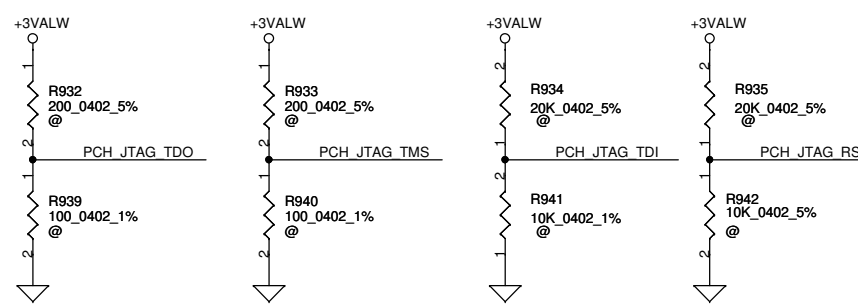
PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz



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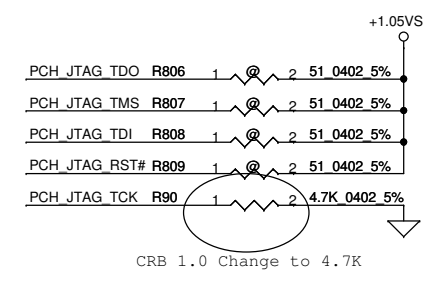


GPIO33 = GPO , internal pull-up, should not be pulled low
flash ME core of strap pin pull down

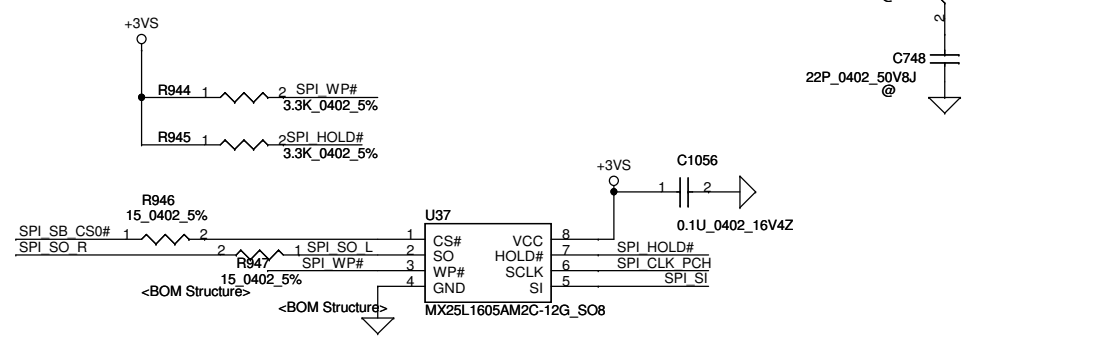


PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R104	No Install	200ohm	No Install	No Install
	R108	No Install	100ohm	No Install	No Install
PCH_JTAG_TMS	R105	200ohm	200ohm	No Install	No Install
	R109	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDI	R106	200ohm	200ohm	20Kohm	No Install
	R110	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R97	51ohm	51ohm	51ohm	51ohm
	R107	20Kohm	20Kohm	No Install	No Install
PCH_JTAG_RST#	R110	10Kohm	10Kohm	No Install	No Install

FOR EVT

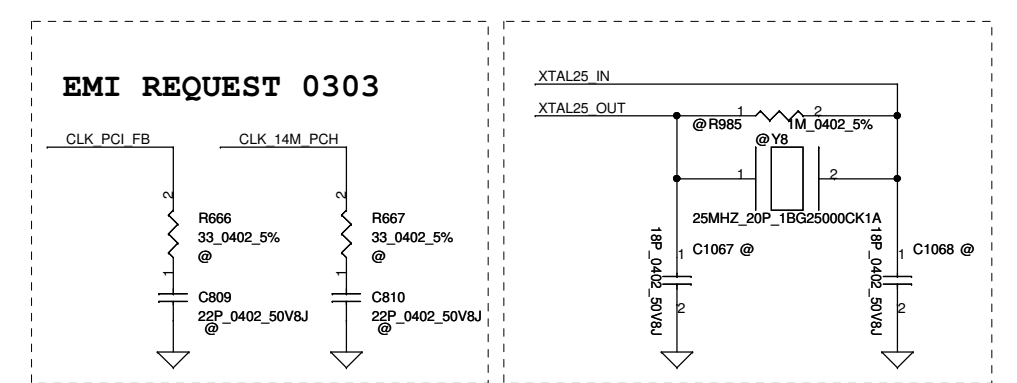
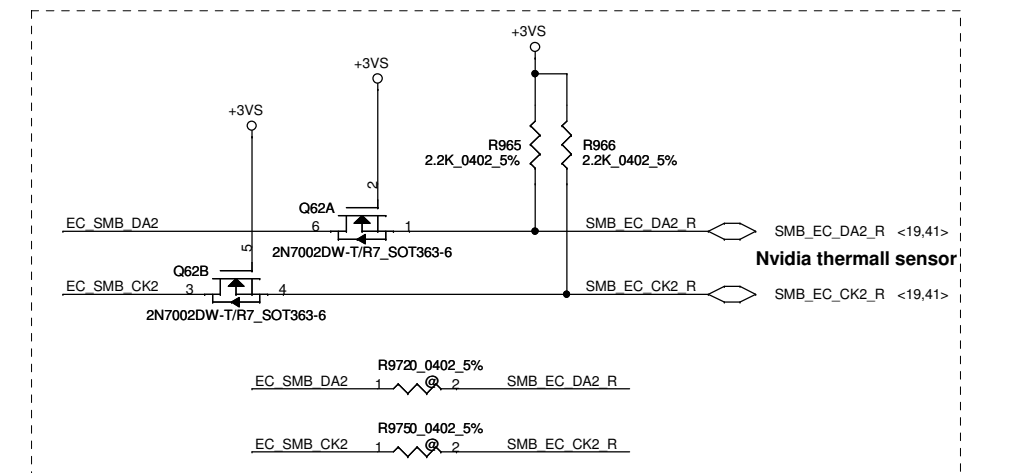
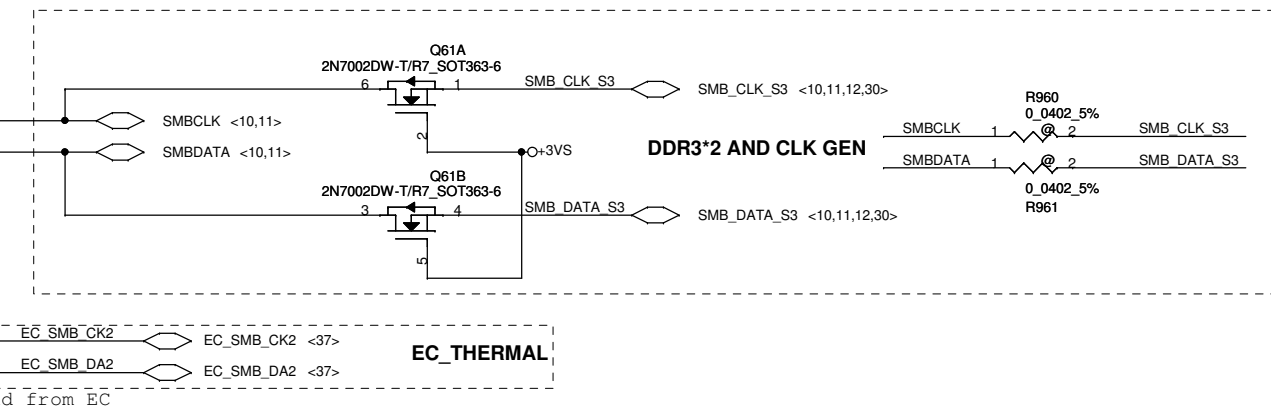
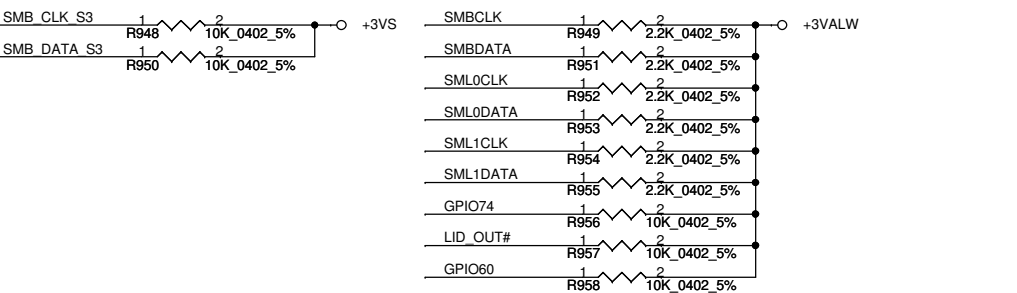
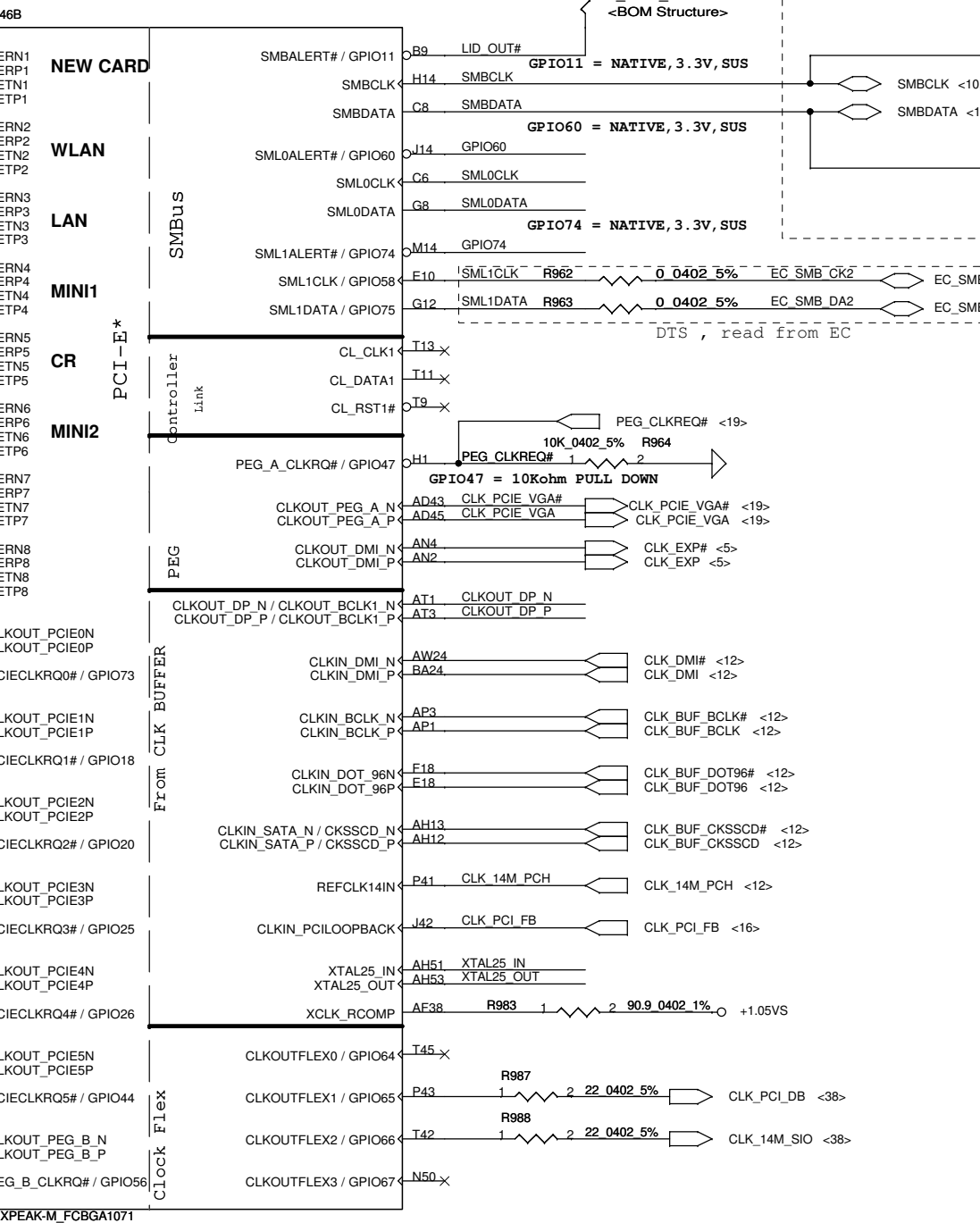
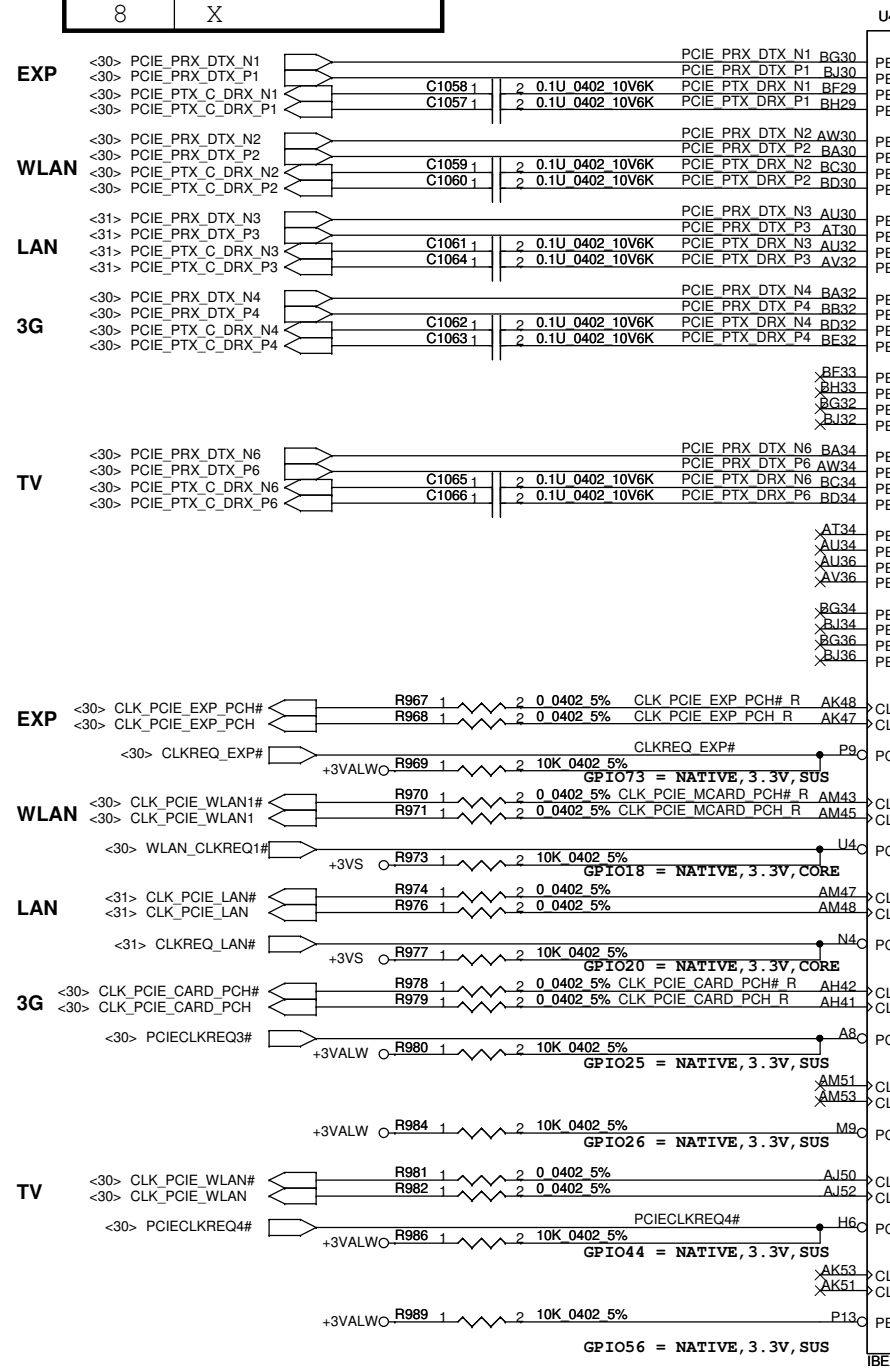


SPI ROM on ME

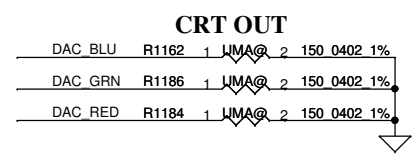
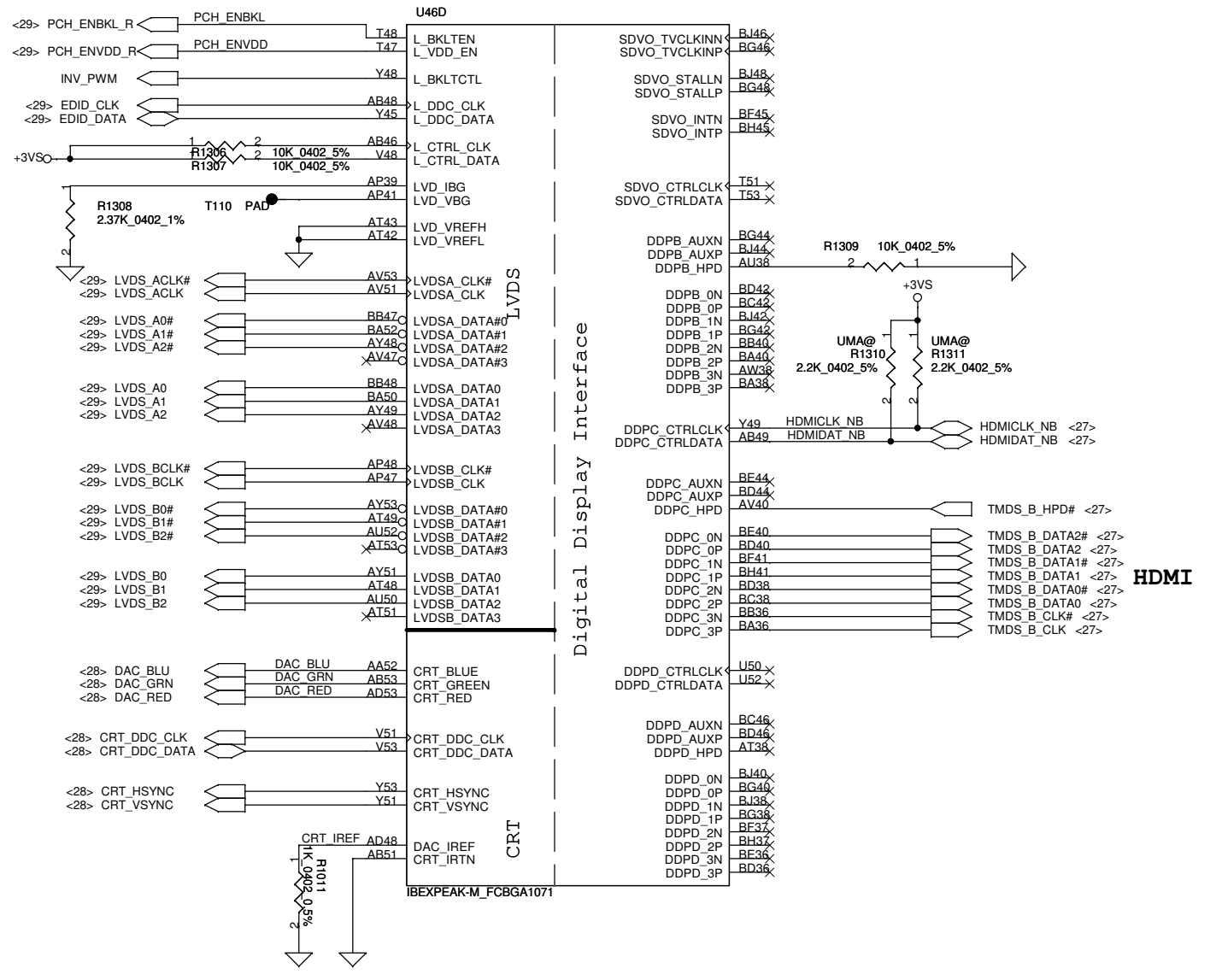
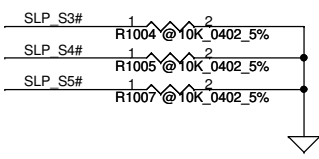
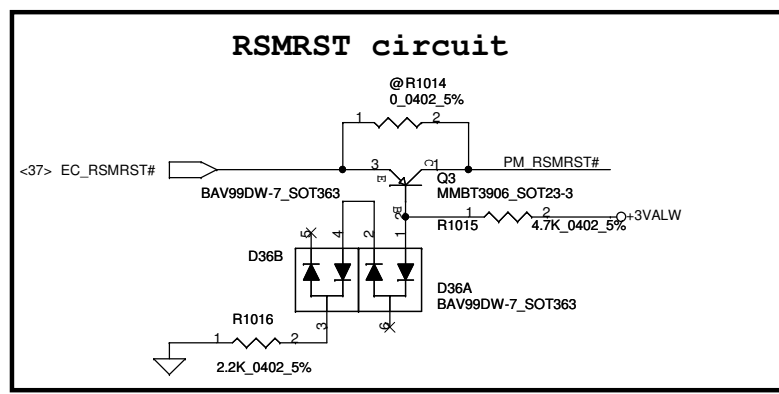
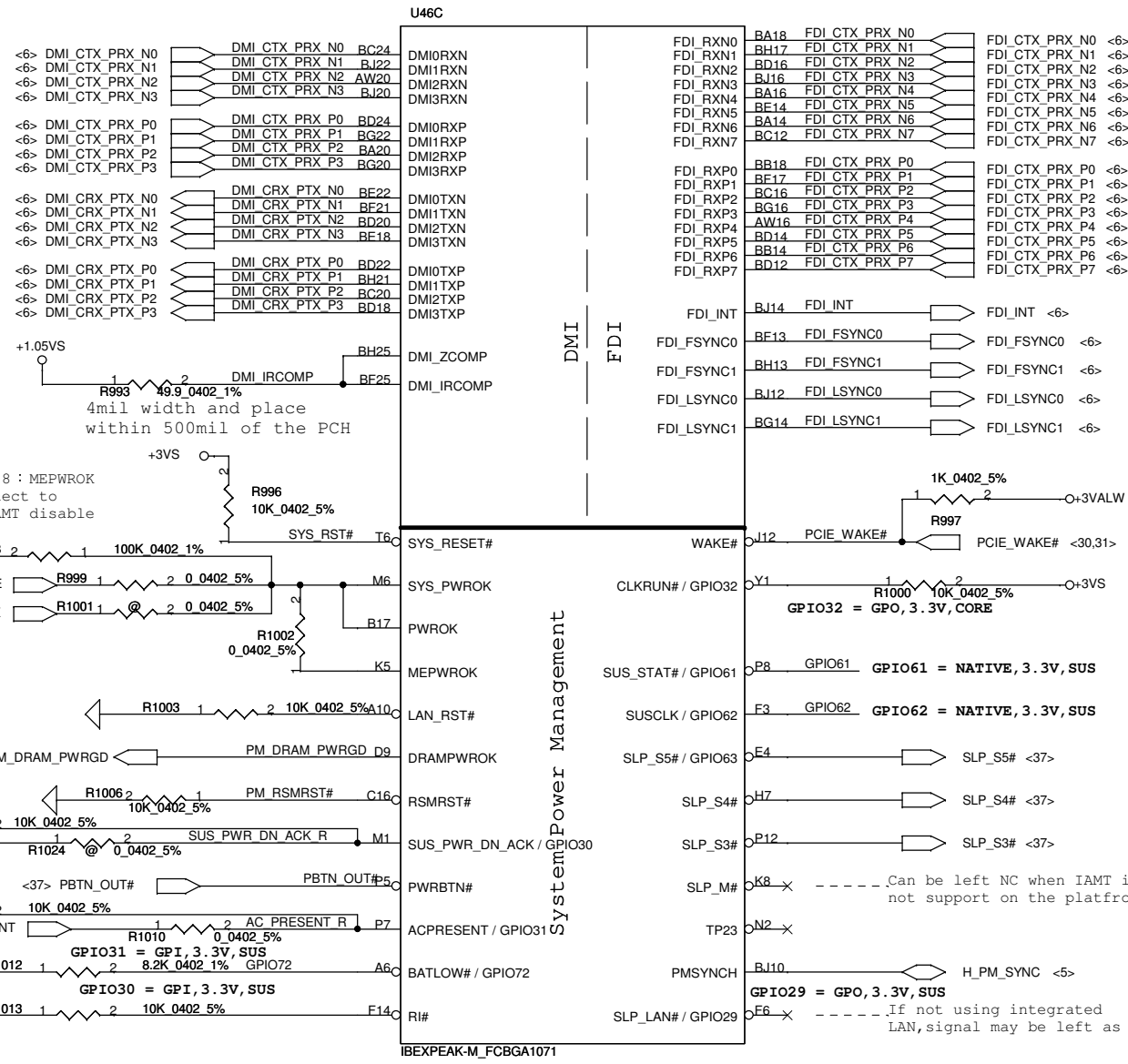


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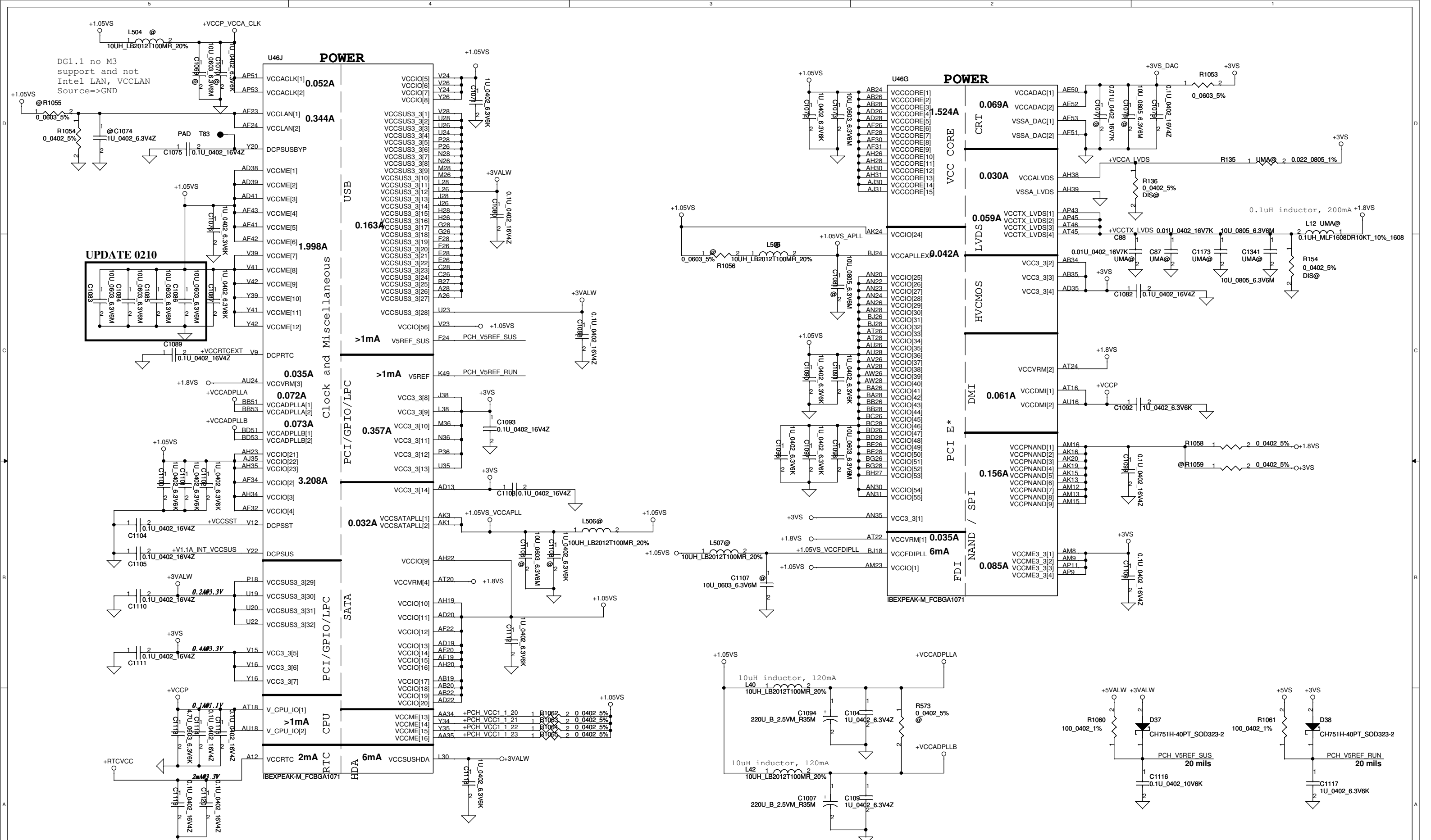
PCI-E PORT LIST	
PORT	DEVICE
1	NEW CARD
2	WLAN
3	LAN
4	3G
5	X
6	TV TUNNER
7	X
8	X



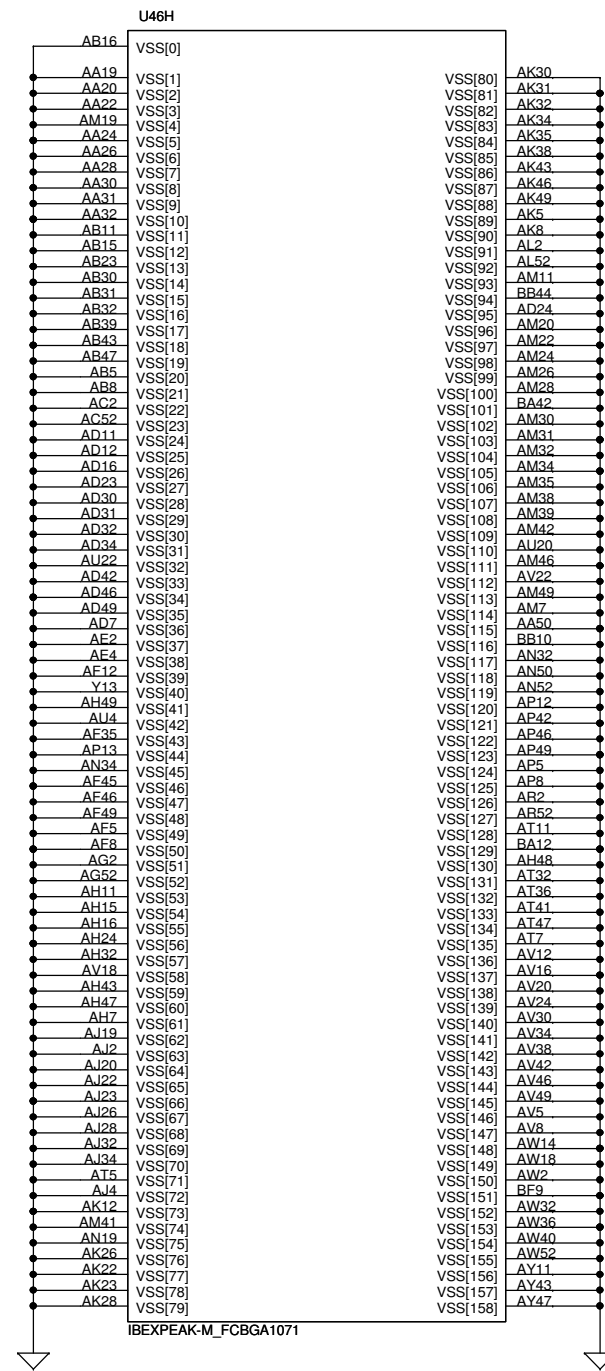
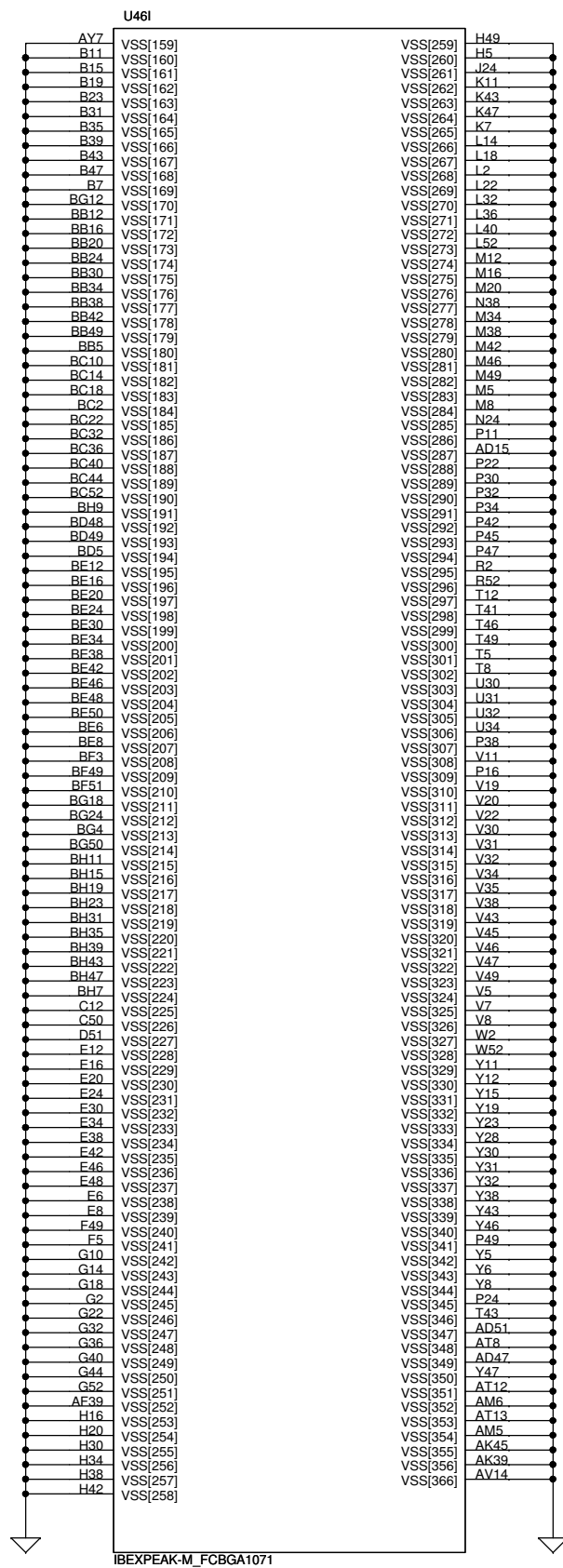
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Date:	Tuesday, March 24, 2009	Sheet	14	of	52



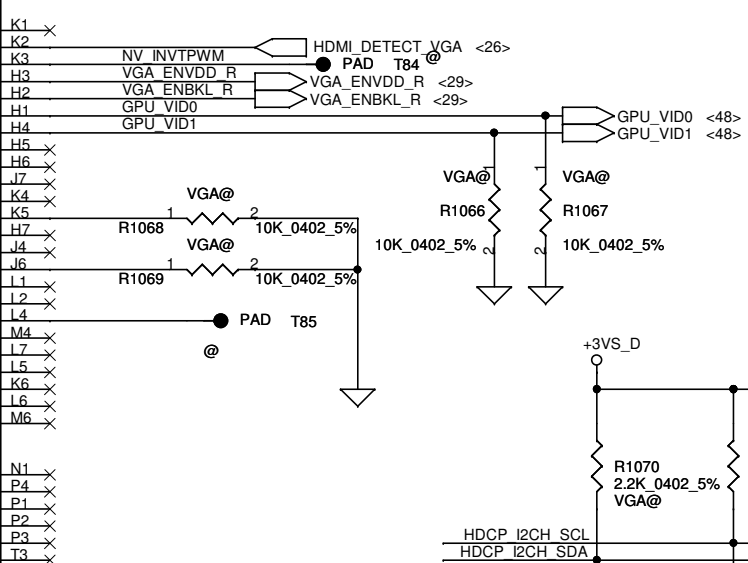
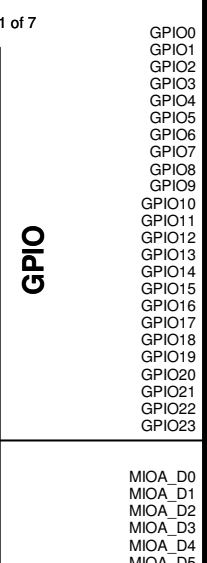
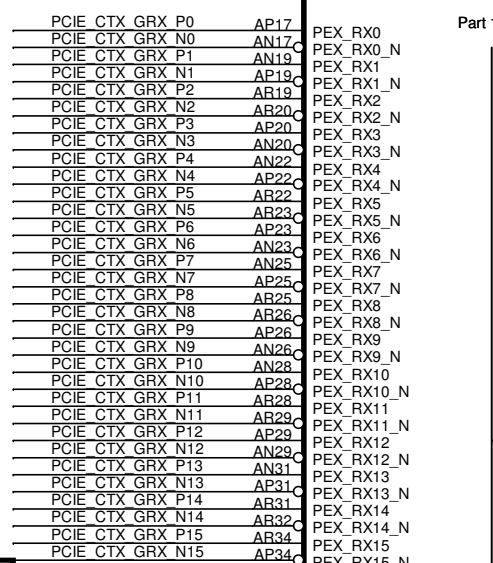
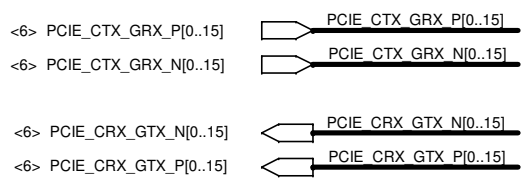
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Issued Date	2008/10/31	Deciphered Date	2009/10/31	Title	IBEX-M(3/6)-DMI/GPIO/LVDS
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Date:	Tuesday, March 24, 2009	Sheet	15	of	52



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Custom	Document Number	NIWBA_LA537IP		0.1	
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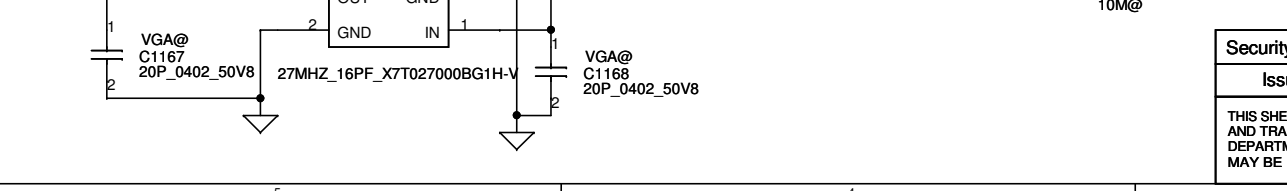
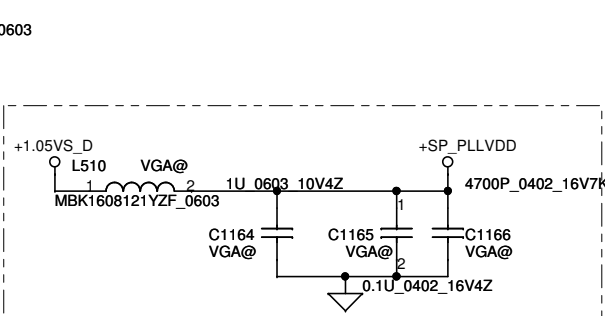
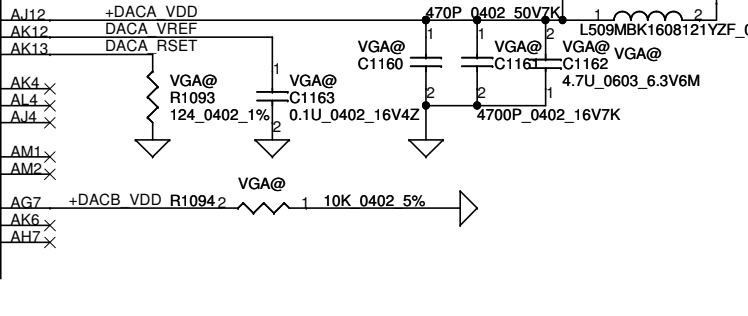
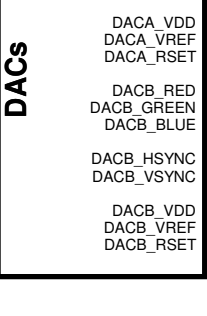
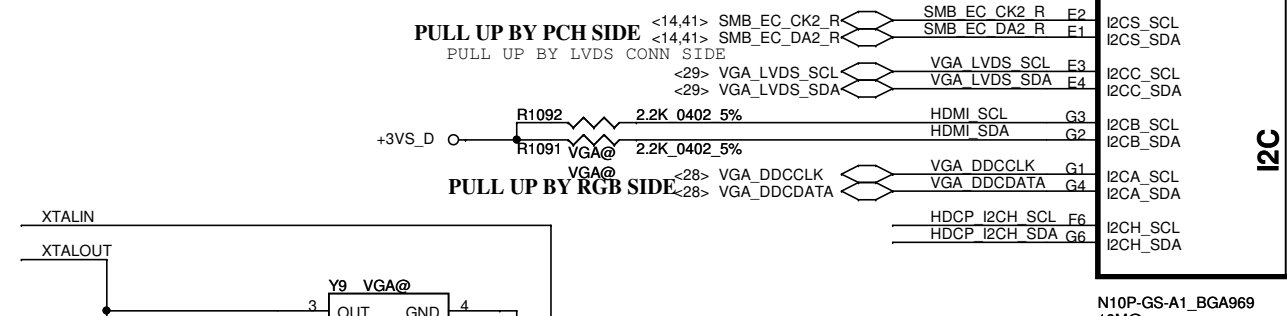
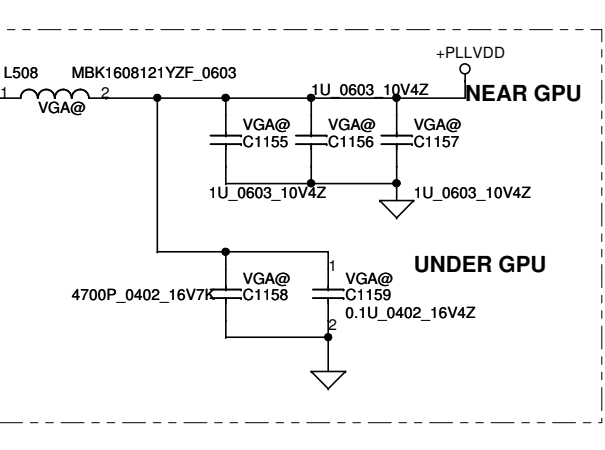
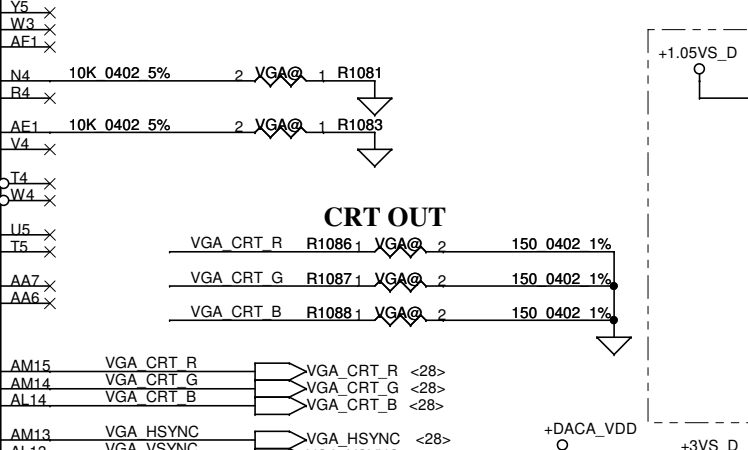
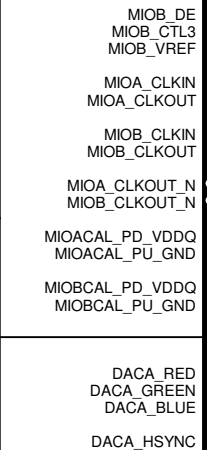
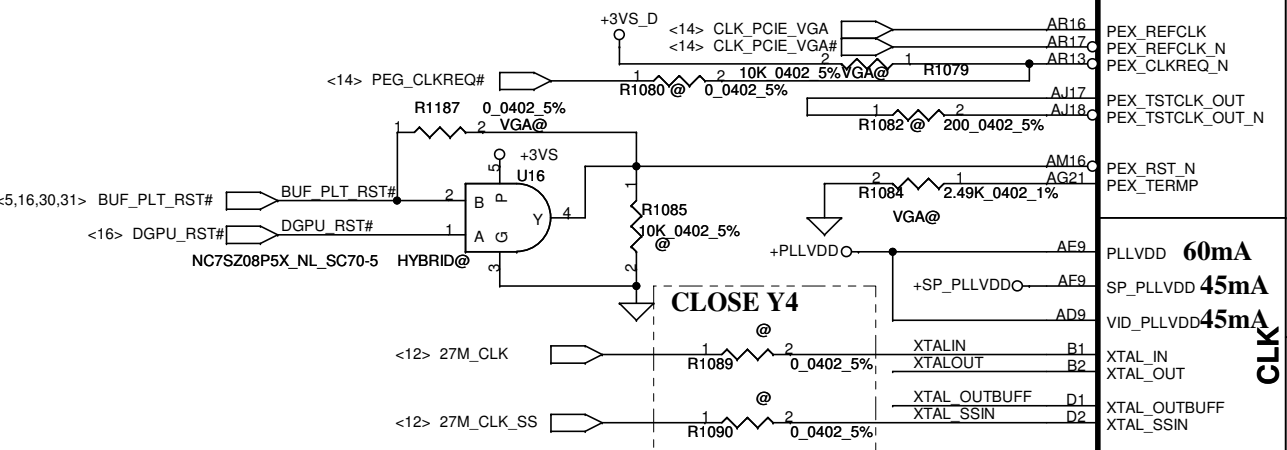
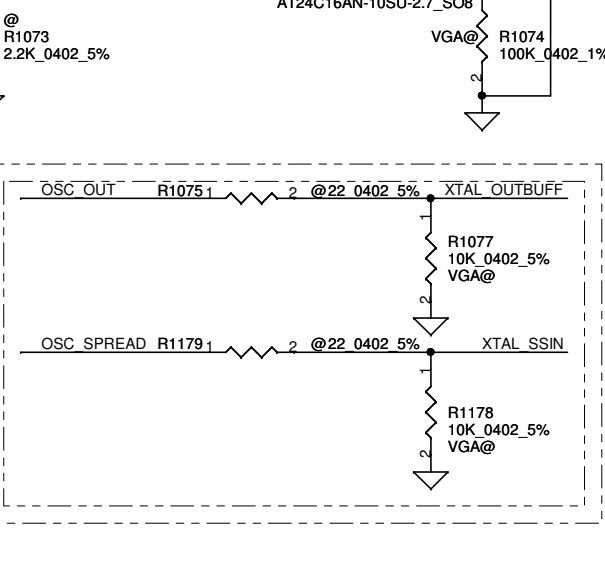
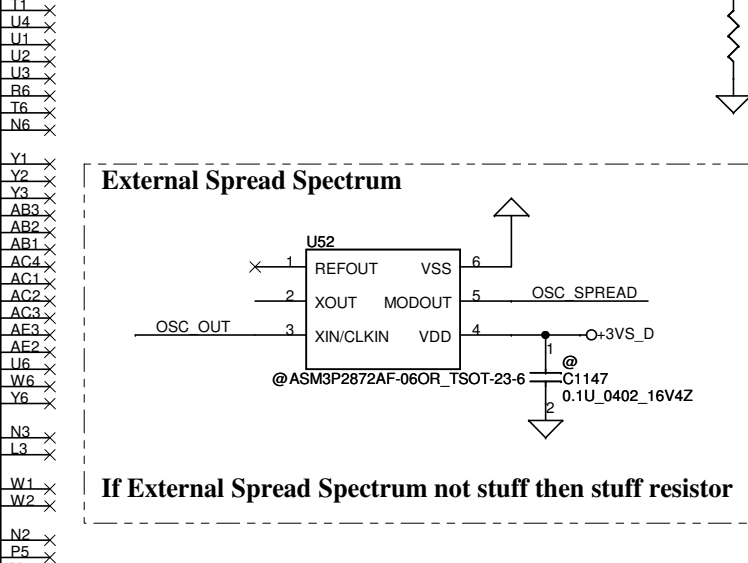
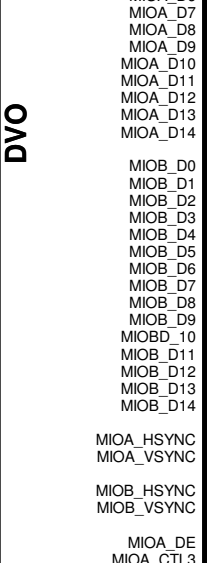
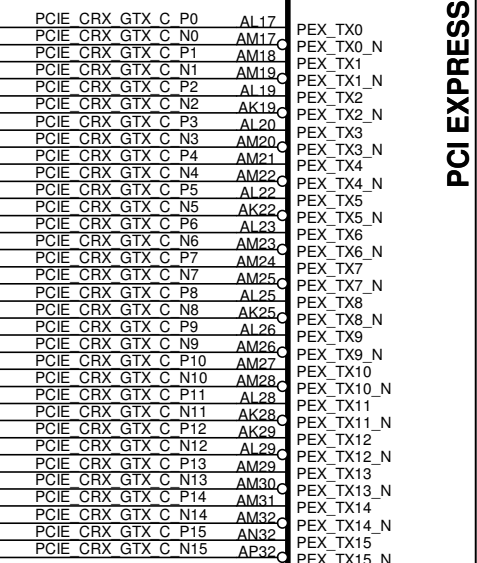


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GPIO6	GPIO5	N10M-GS	N10P-GS
0	0	0.8V	12
0	1	0.85V	12
1	0	0.9V	0,10

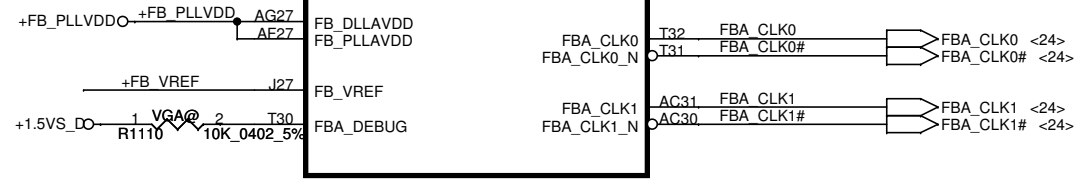
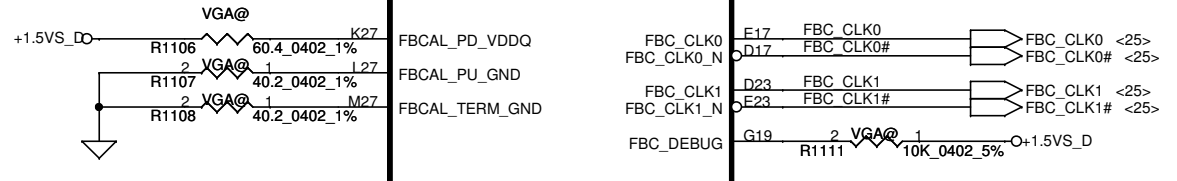
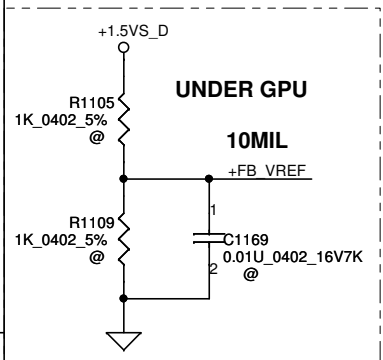
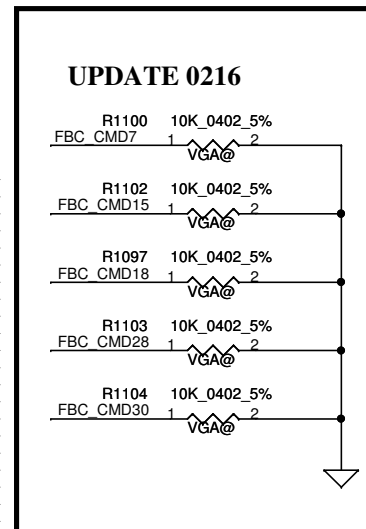
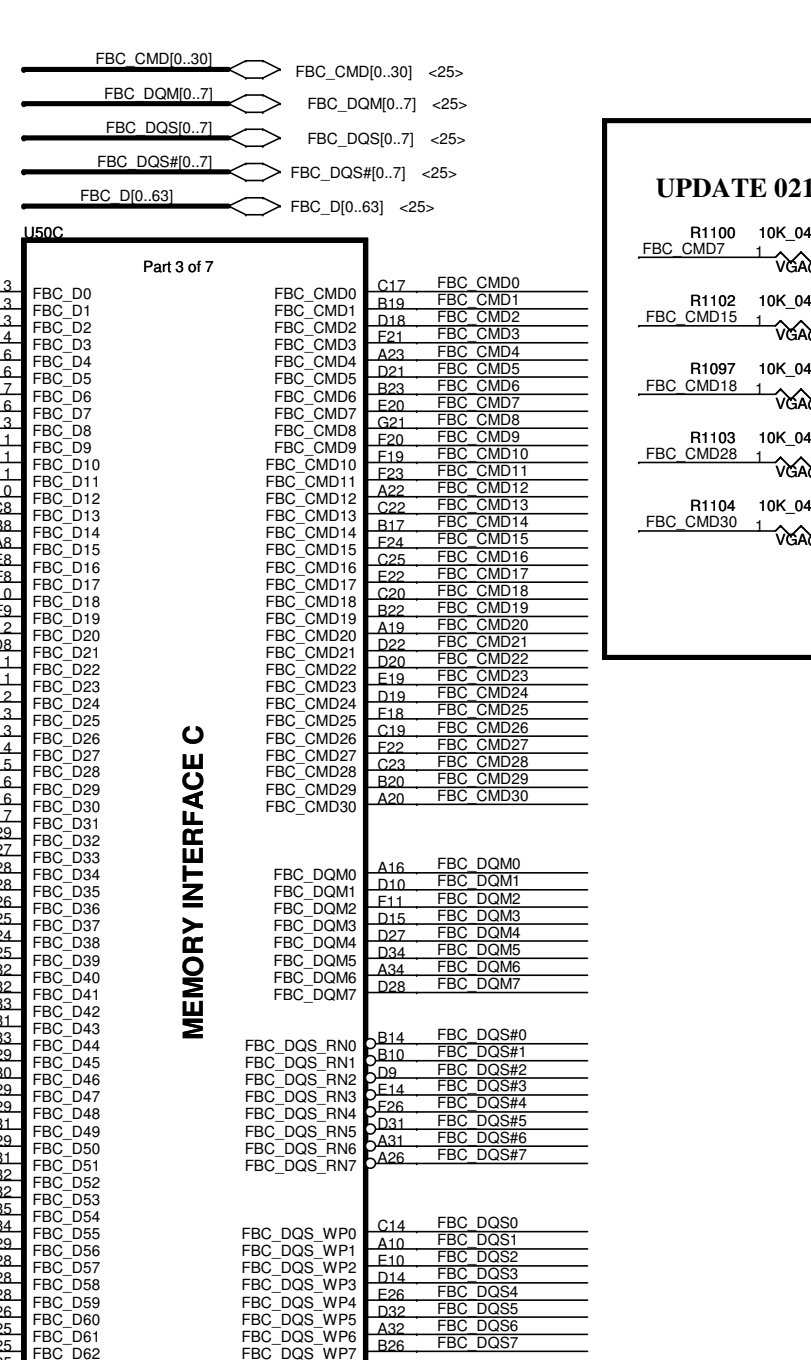
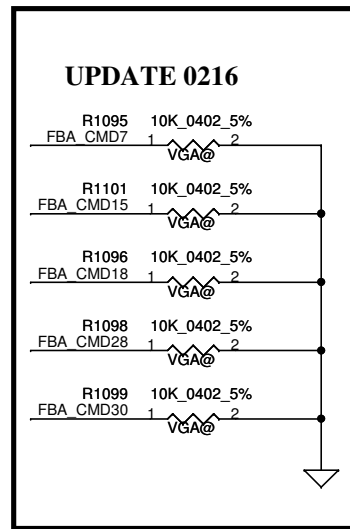
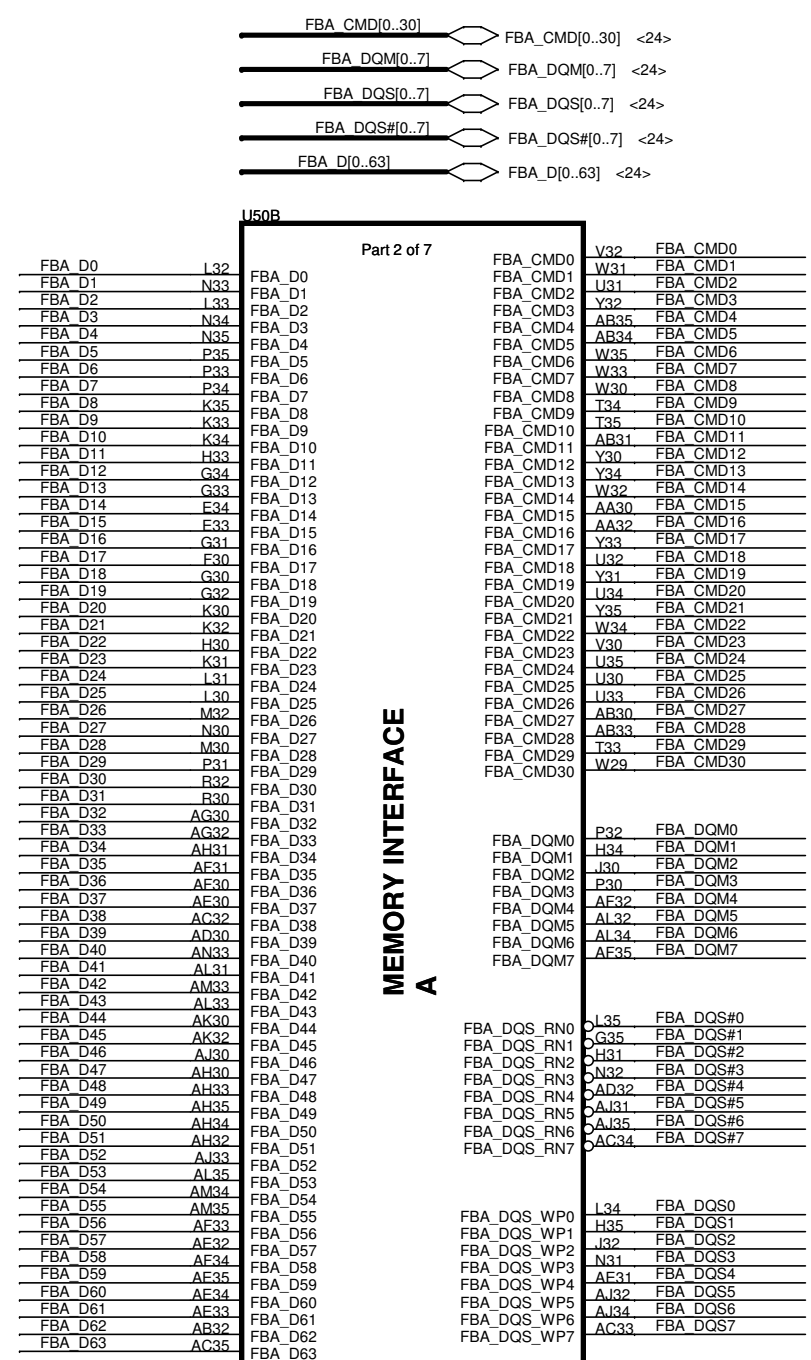
PCIE CRX GTX	PCIE CRX GTX	PCIE CRX GTX	PCIE CRX GTX	PCIE CRX GTX	PCIE CRX GTX
P0	P0	P0	P0	P0	P0
N0	N0	N0	N0	N0	N0
P1	P1	P1	P1	P1	P1
N1	N1	N1	N1	N1	N1
P2	P2	P2	P2	P2	P2
N2	N2	N2	N2	N2	N2
P3	P3	P3	P3	P3	P3
N3	N3	N3	N3	N3	N3
P4	P4	P4	P4	P4	P4
N4	N4	N4	N4	N4	N4
P5	P5	P5	P5	P5	P5
N5	N5	N5	N5	N5	N5
P6	P6	P6	P6	P6	P6
N6	N6	N6	N6	N6	N6
P7	P7	P7	P7	P7	P7
N7	N7	N7	N7	N7	N7
P8	P8	P8	P8	P8	P8
N8	N8	N8	N8	N8	N8
P9	P9	P9	P9	P9	P9
N9	N9	N9	N9	N9	N9
P10	P10	P10	P10	P10	P10
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P14	P14	P14	P14	P14	P14
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P15	P15	P15	P15	P15	P15
N15	N15	N15	N15	N15	N15



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		2008/04/

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Compal Electronics, Ltd.	
Title	
N10x-GS PCIE, LVDS, GPIO, CLK	
Size Custom	Document Number
	NIWBA_LA5371P
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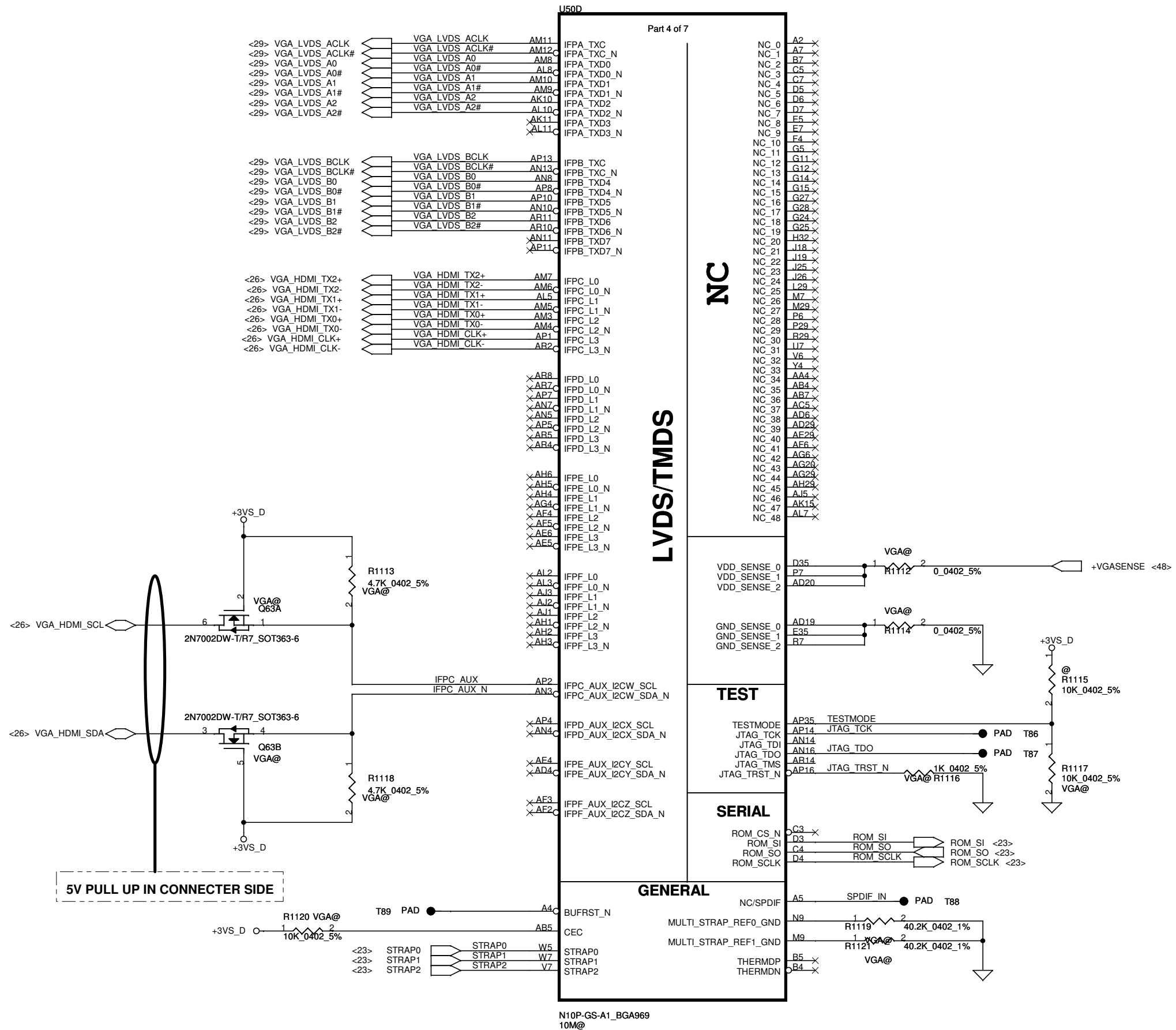


Place Components Close to BGA

Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR3	+1.5VS	40.2 ohm	60.4 ohm	40.2 ohm
GDDR3	+1.8VS	40.2 ohm	60.4 ohm	40.2 ohm

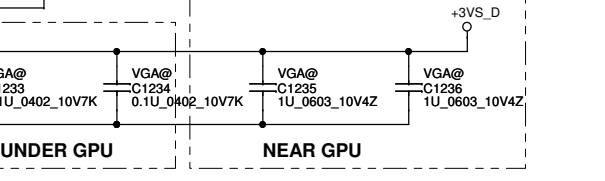
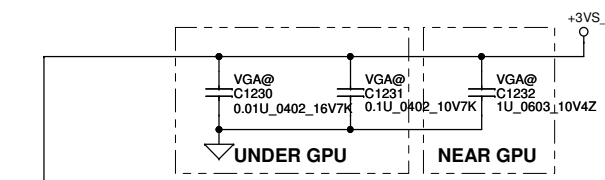
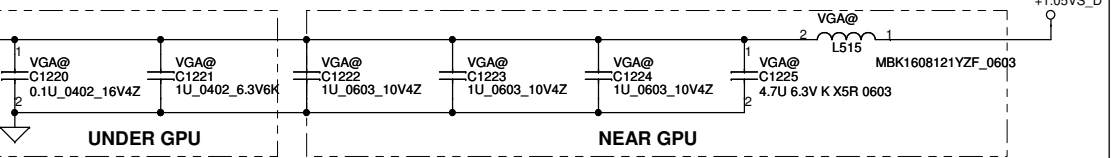
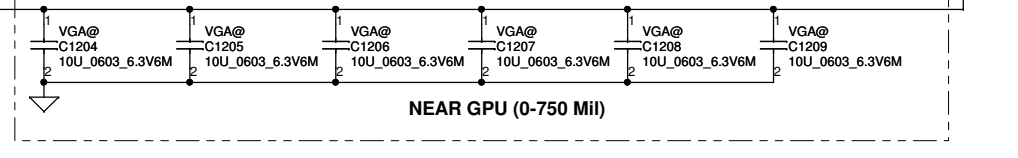
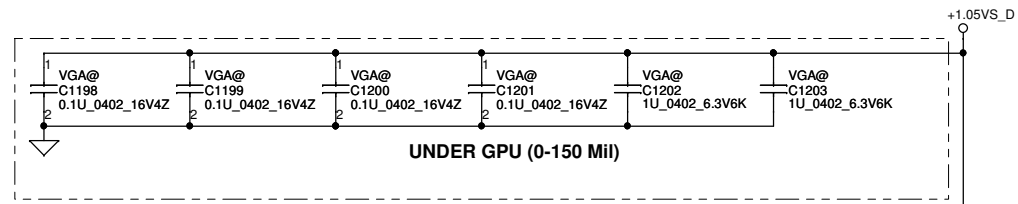
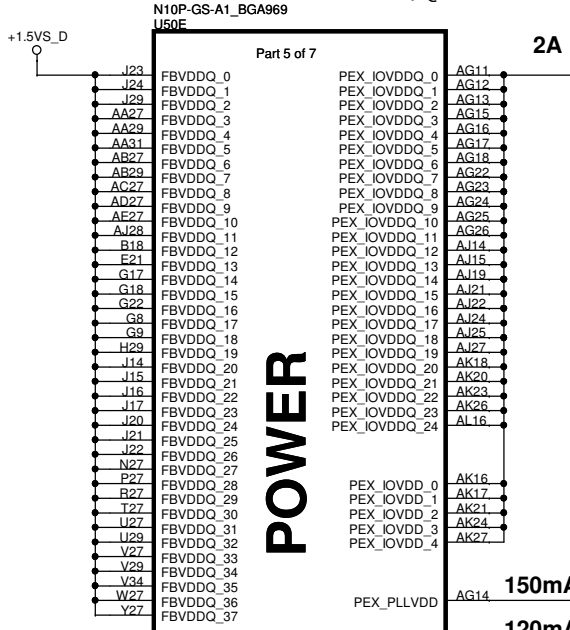
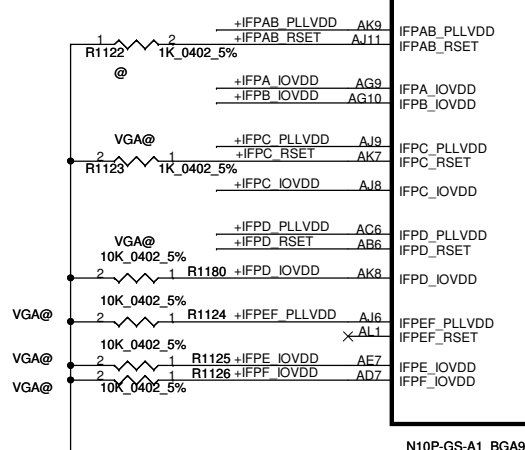
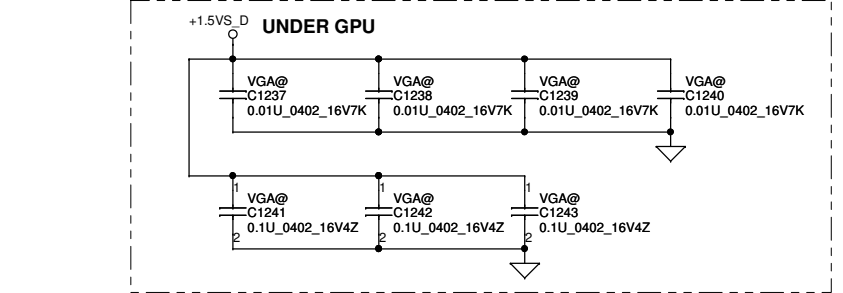
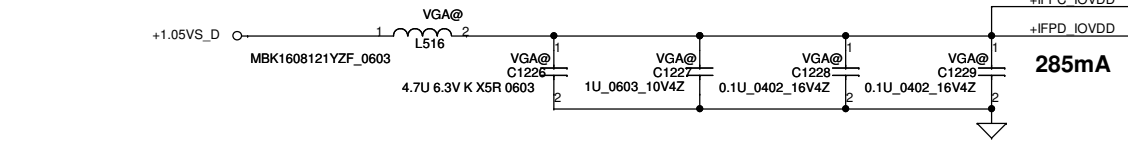
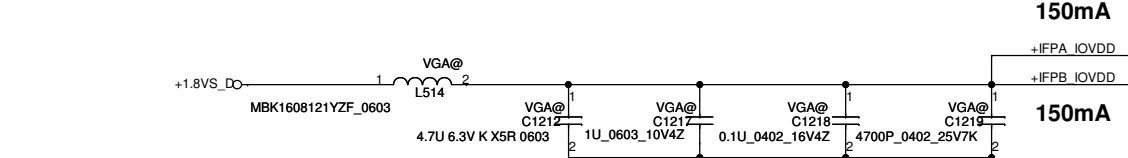
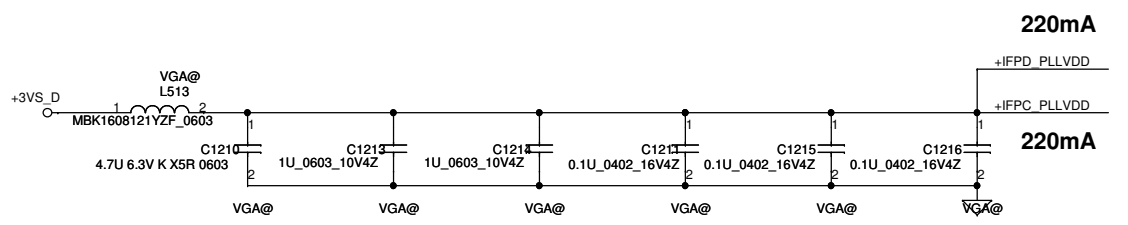
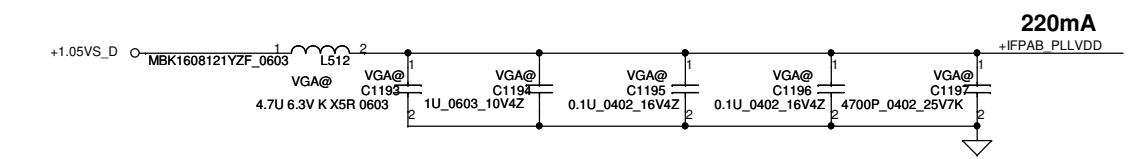
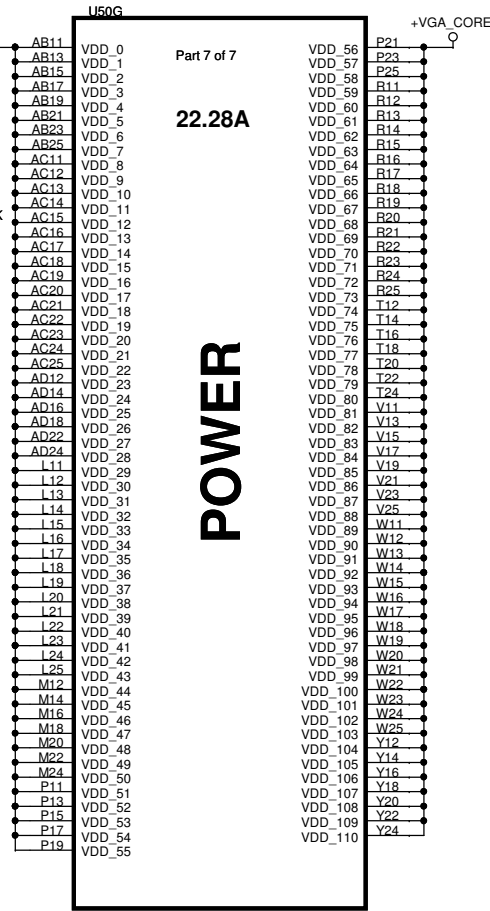
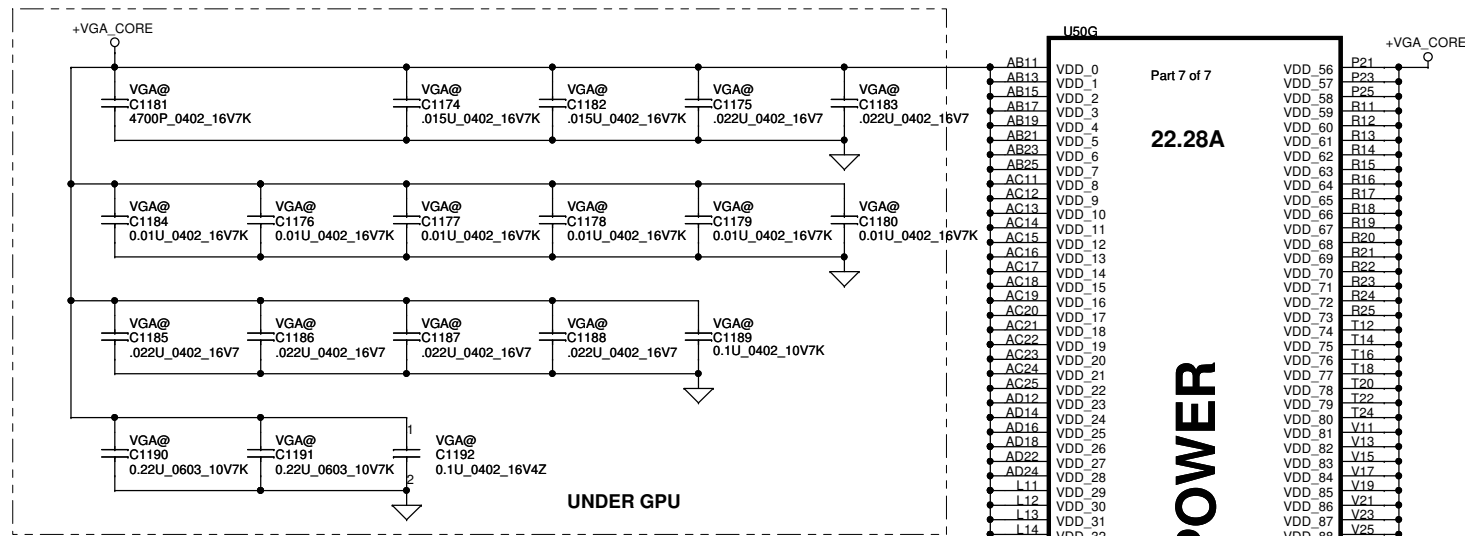
Must be used 1% resistor for driver calibration

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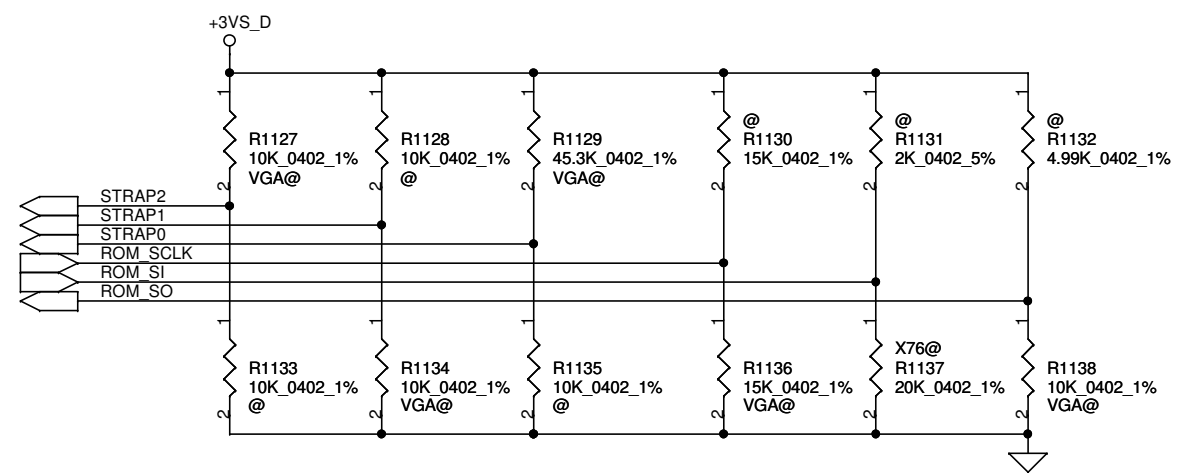
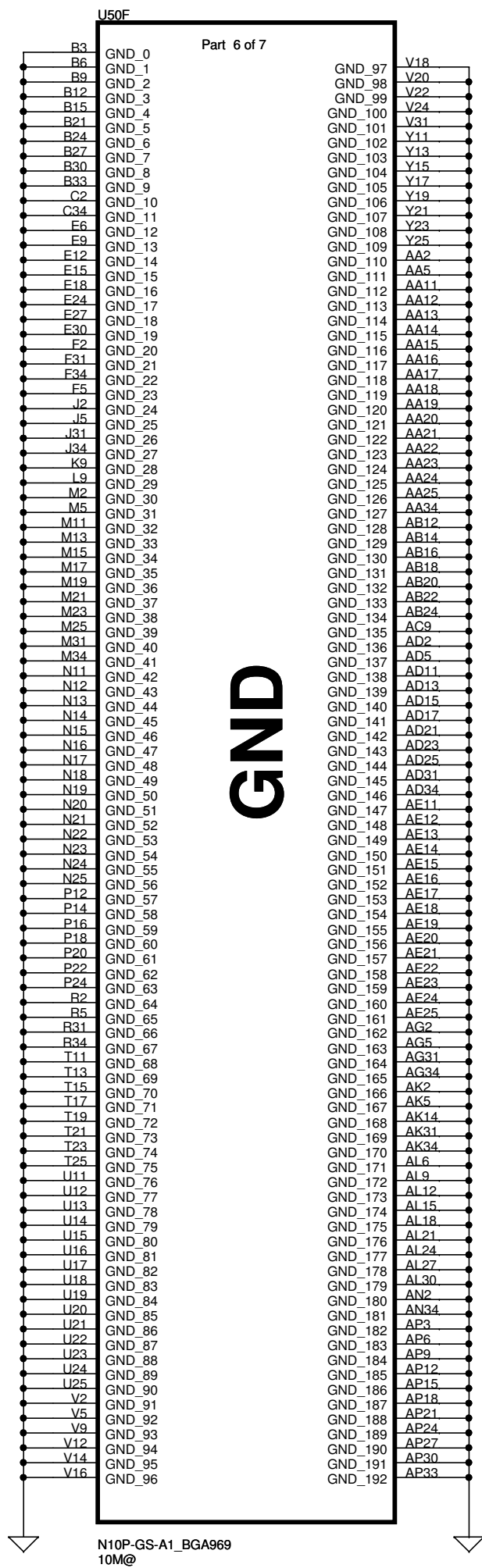


N10P-GS-A1_BGA969
10M@

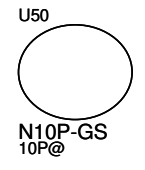
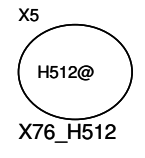
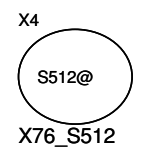
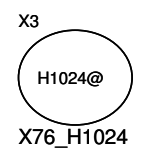
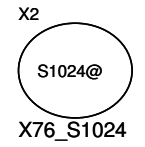
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Size	Custom	Document Number	NIWBA_LA5371P	
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<21> STRAP2
 <21> STRAP1
 <21> STRAP0
 <21> ROM_SCLK
 <21> ROM_SI
 <21> ROM_SO



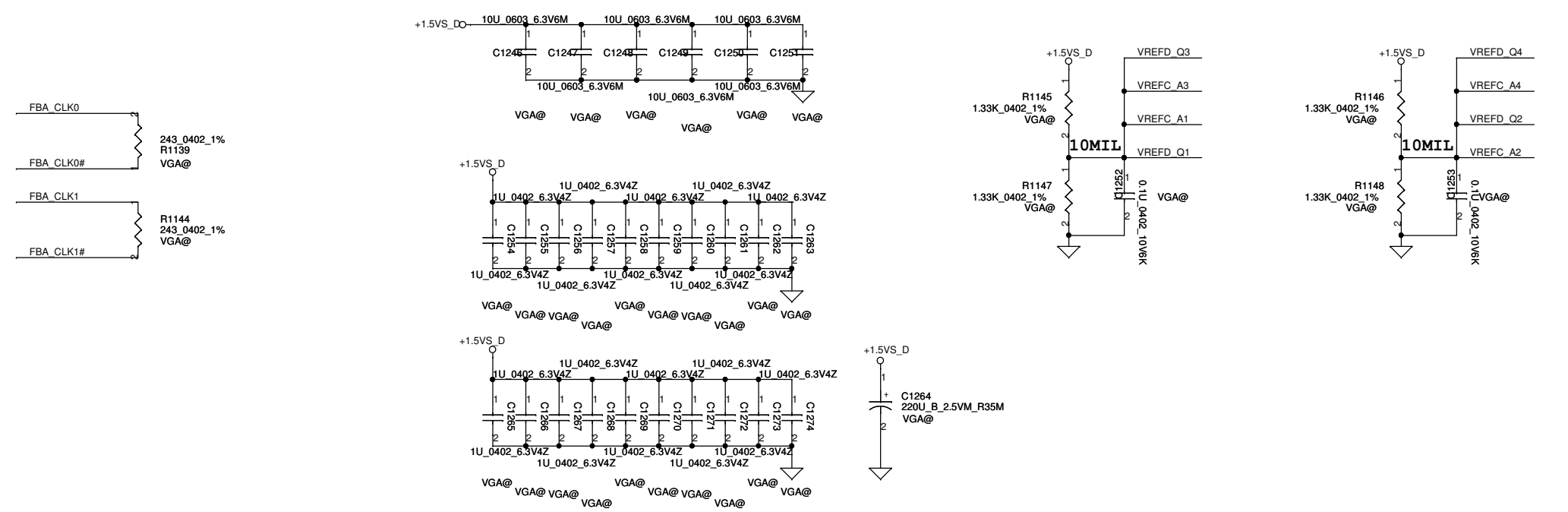
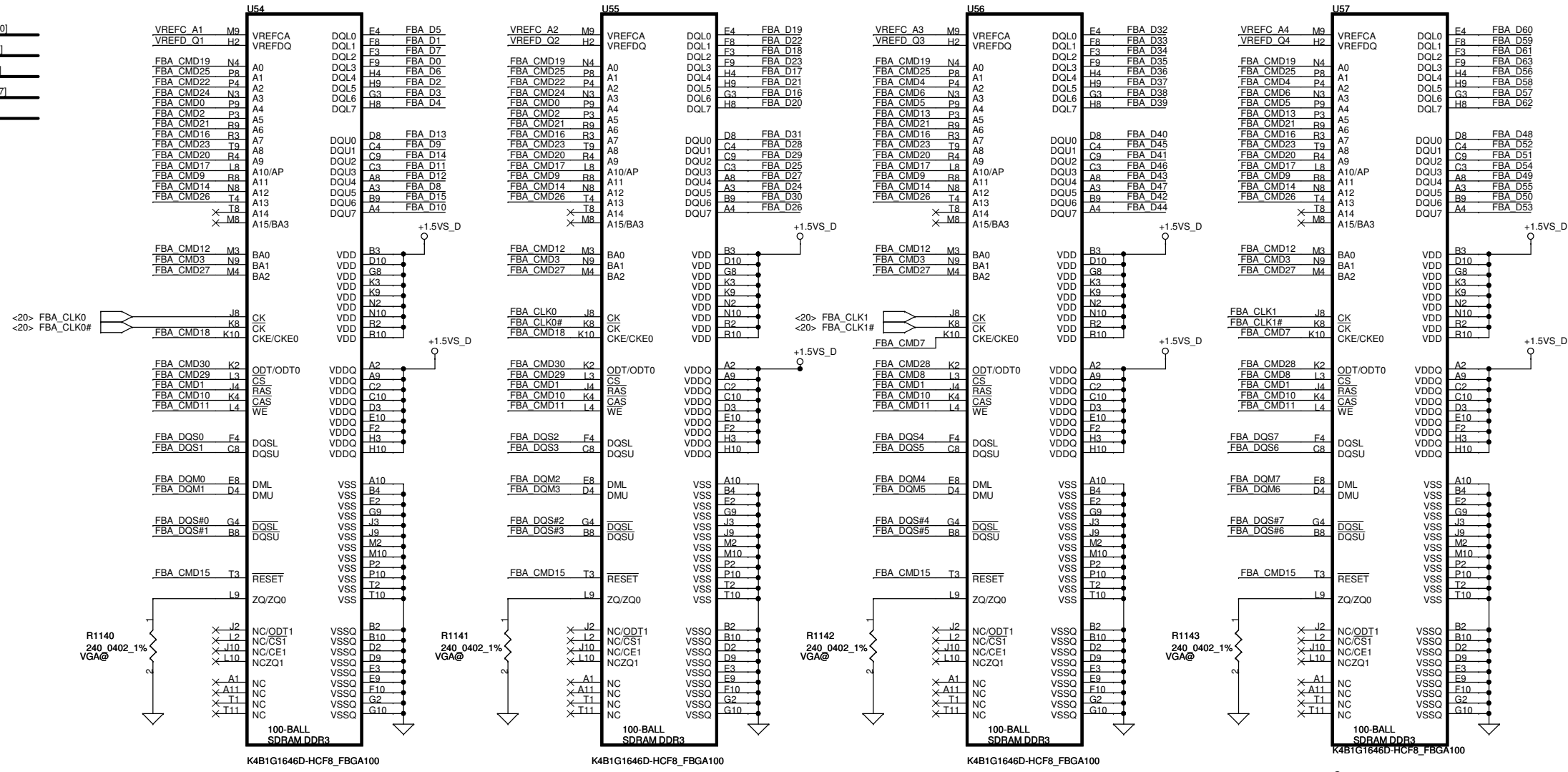
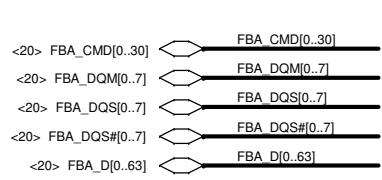
GB1 Family GPU Strap Options

GPU	FB Memory	GPU DEVID RAM_CFG GPU DEVID						
		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0	
N10P-GS (0xA34)	Samsung	64Mx16	PD 10K	PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K

GPU	FB Memory	GPU DEVID RAM_CFG GPU DEVID						
		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0	
N10M-GS (0xA74)	Samsung	64Mx16	PD 10K	PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K

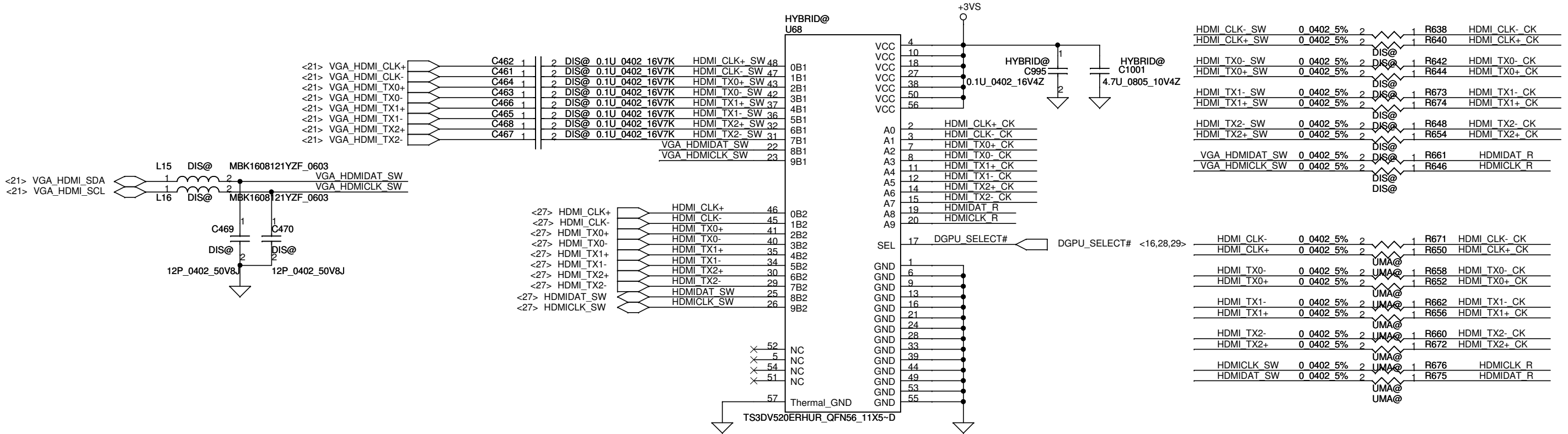
Security Classification	Compal Secret Data			Compal Electronics, Ltd.	
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title N10x-GS GND & STRAP	
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N10x 40nm DDR3 MAPPING
NVIDIA DOCUMENT FOR DA-3978-001

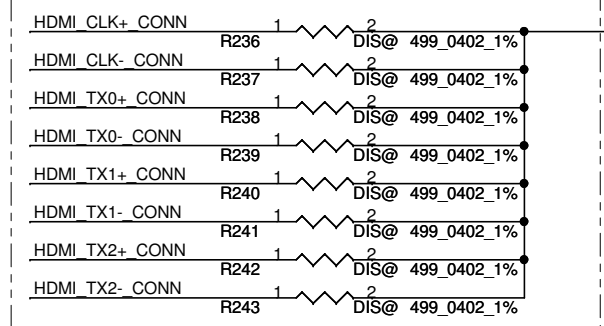


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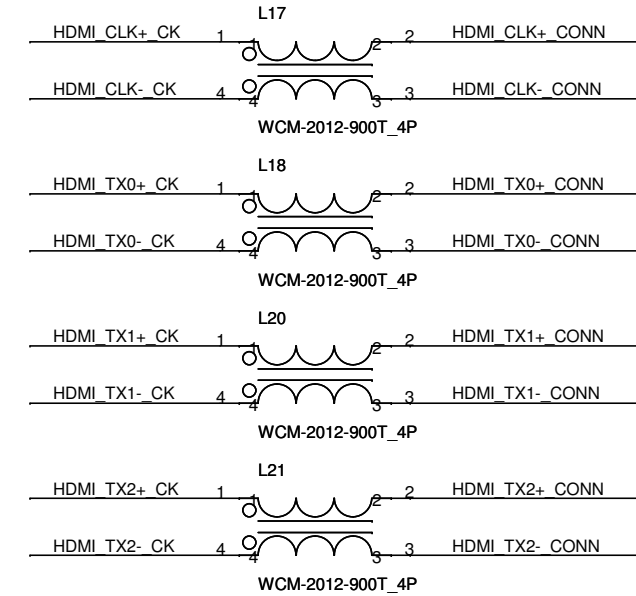
HDMI switch1



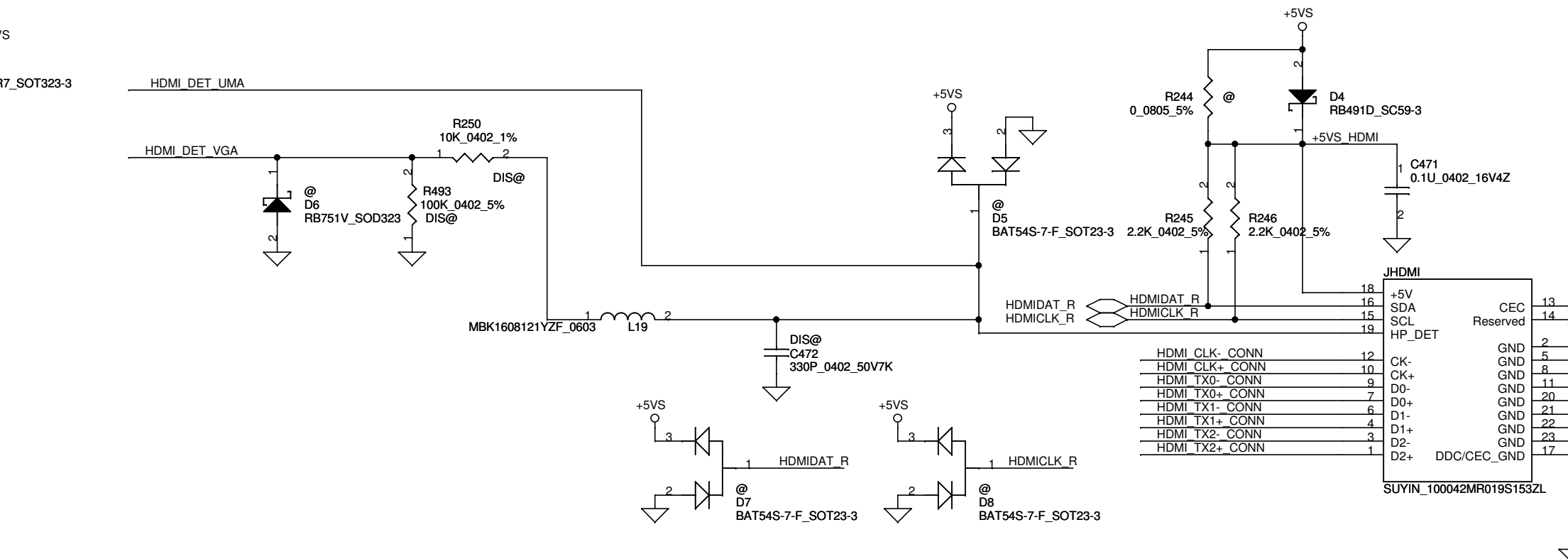
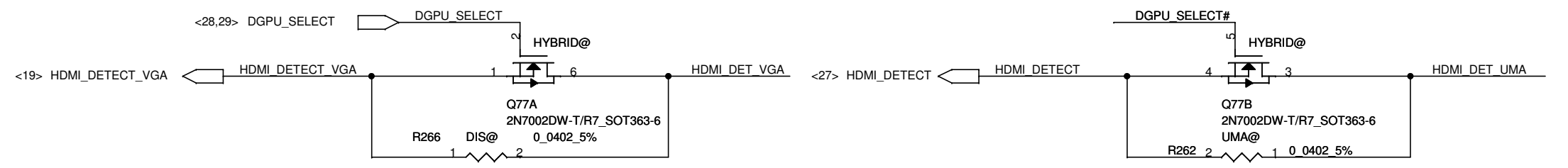
TMDS pull down (500ohm) resistors G9x only



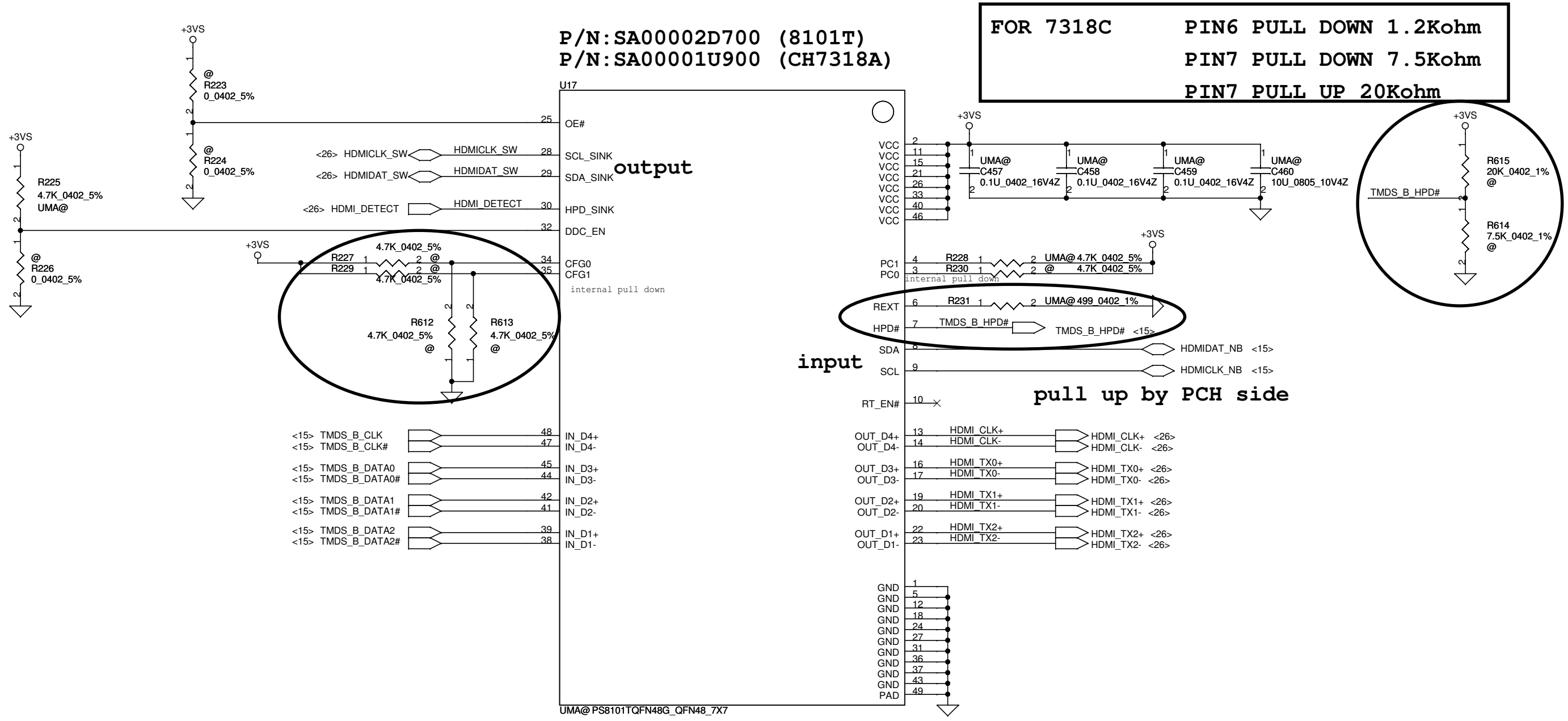
NEAR CONNECT



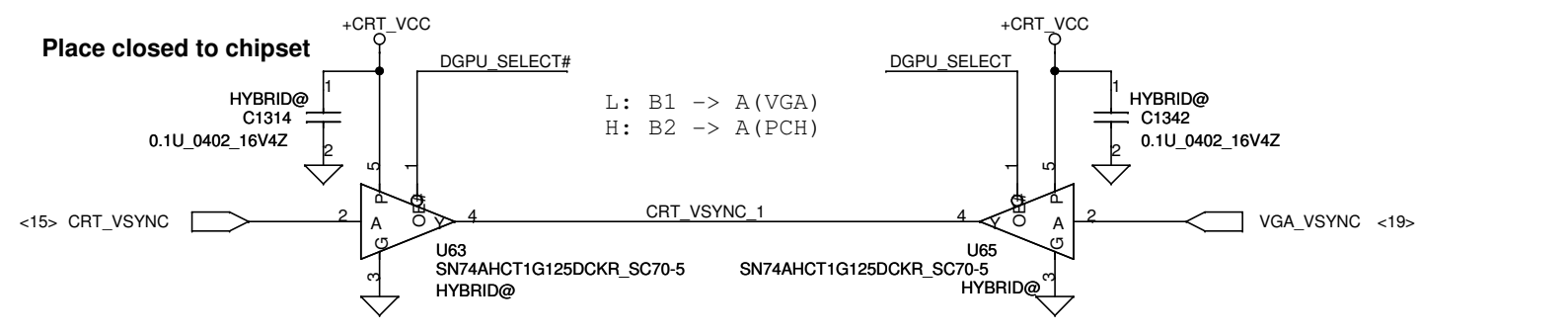
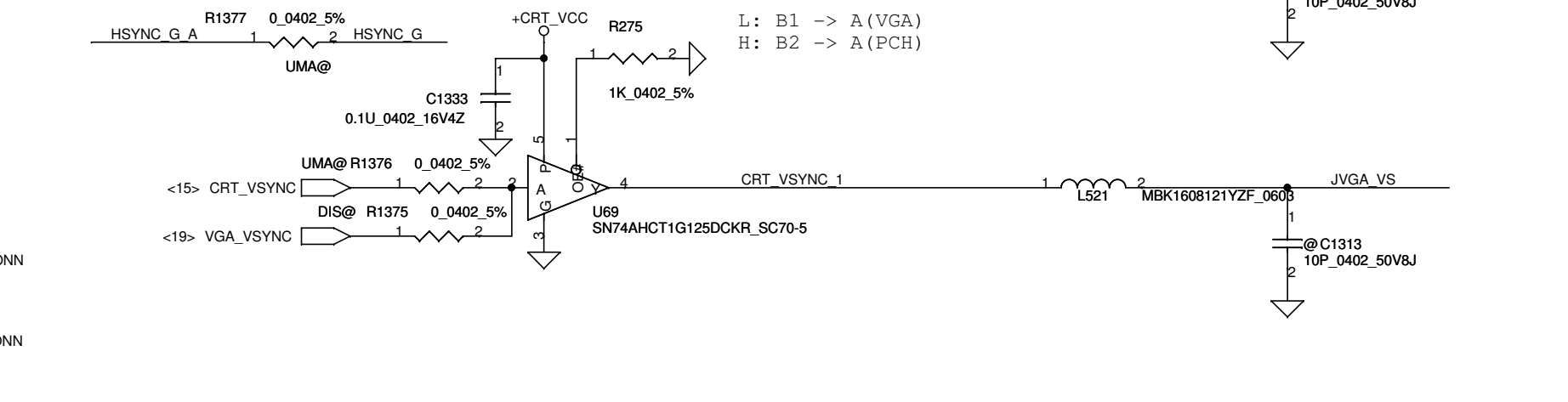
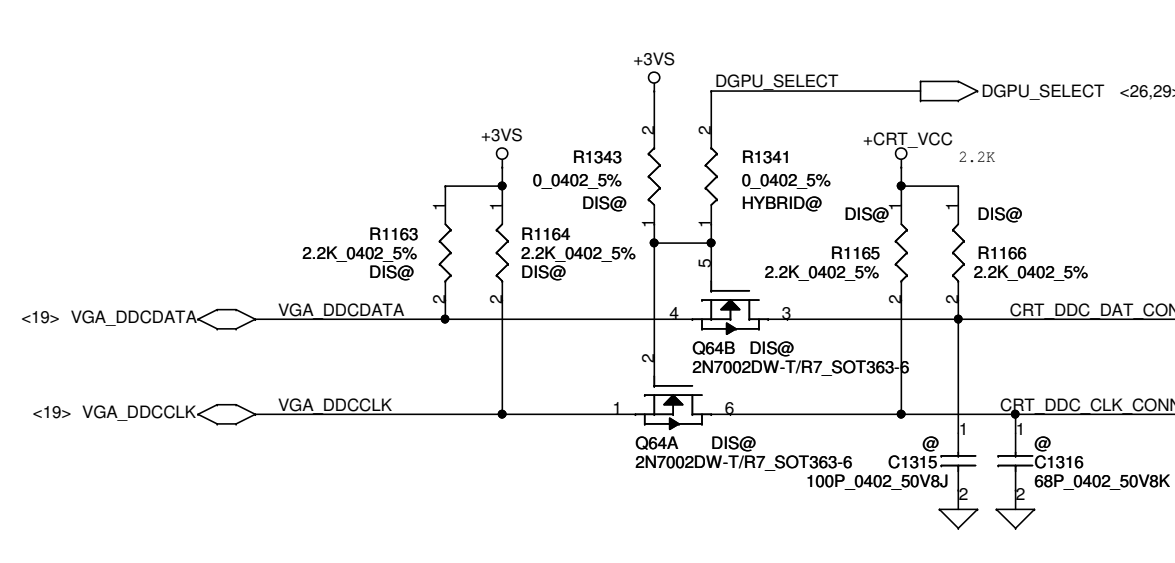
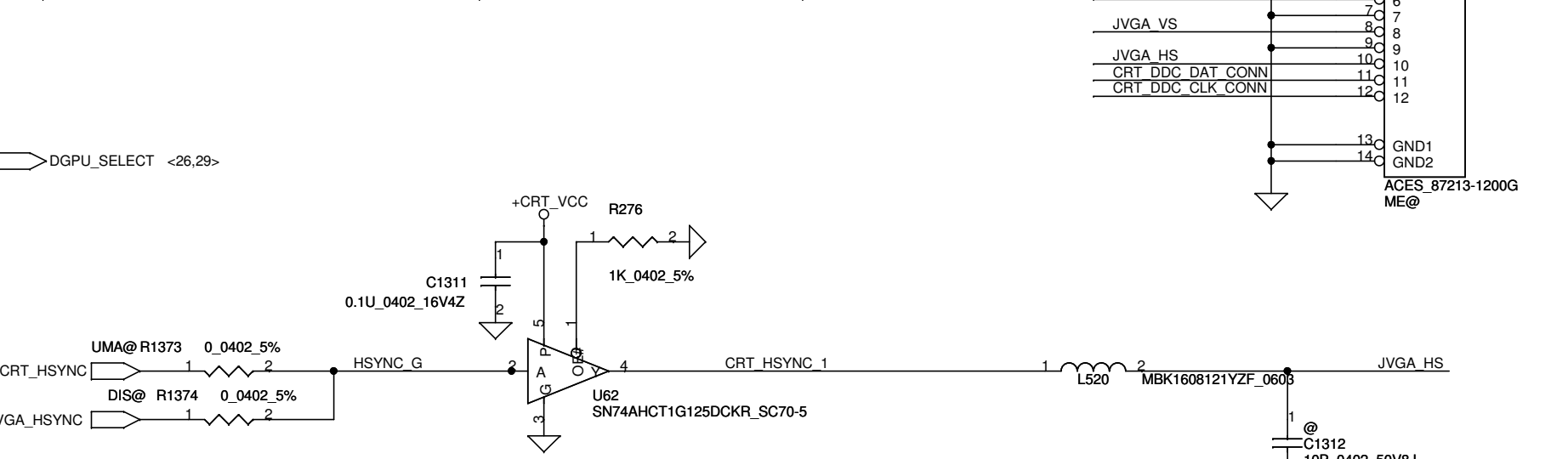
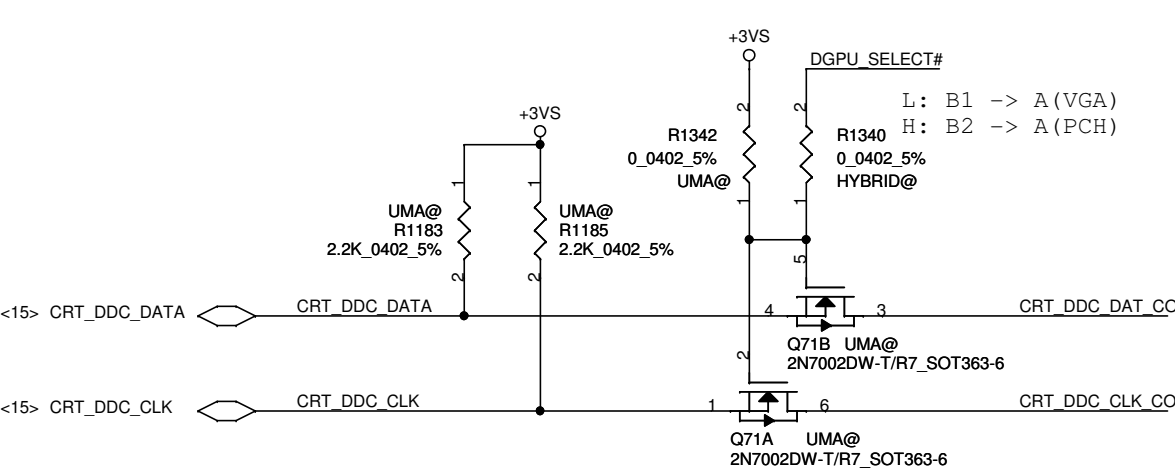
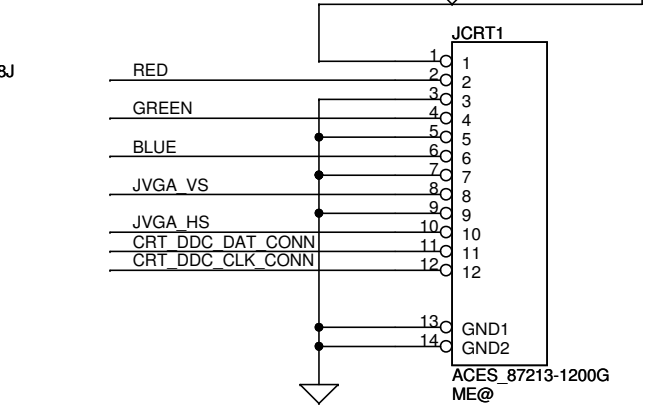
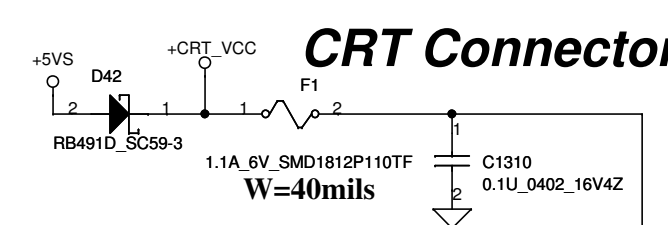
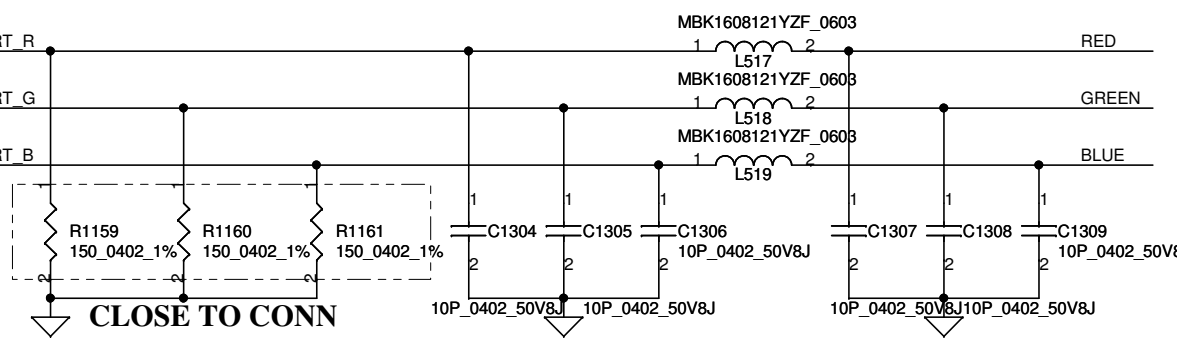
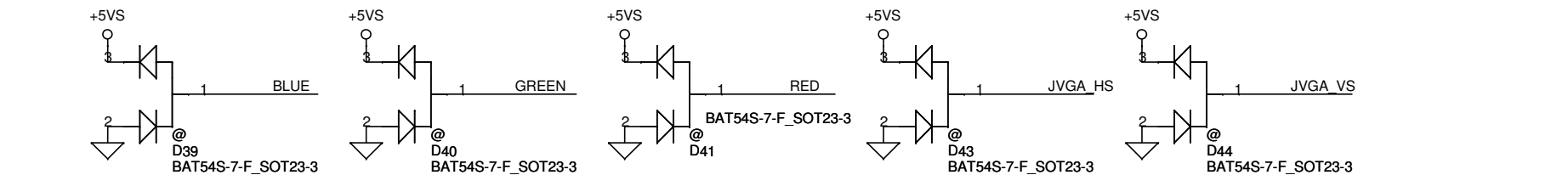
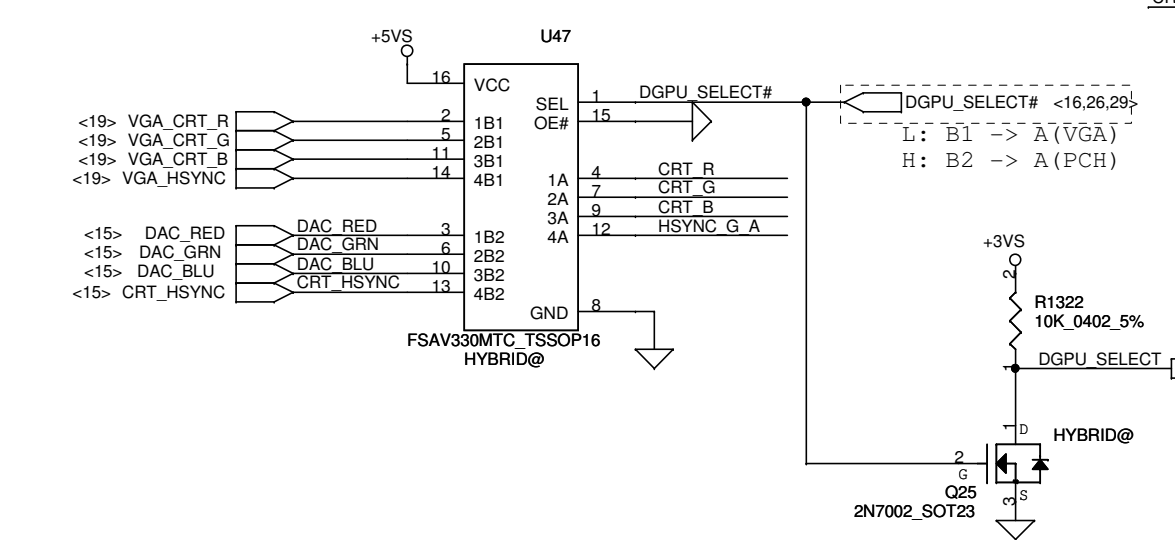
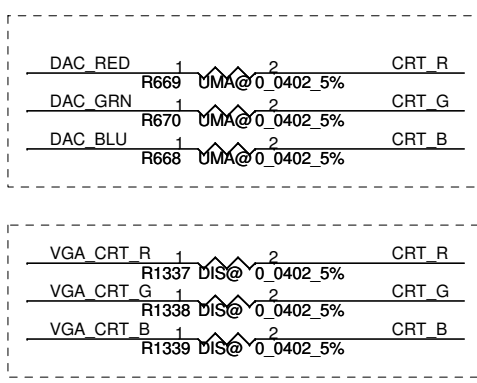
HDMI_CLK+_CONN	R251	1	@	2	0	0402	5%	HDMI_CLK+_CONN
HDMI_CLK-_CONN	R252	1	@	2	0	0402	5%	HDMI_CLK-_CONN
HDMI_TX0+_CONN	R253	1	@	2	0	0402	5%	HDMI_TX0+_CONN
HDMI_TX0-_CONN	R254	1	@	2	0	0402	5%	HDMI_TX0-_CONN
HDMI_TX1+_CONN	R255	1	@	2	0	0402	5%	HDMI_TX1+_CONN
HDMI_TX1-_CONN	R256	1	@	2	0	0402	5%	HDMI_TX1-_CONN
HDMI_TX2+_CONN	R257	1	@	2	0	0402	5%	HDMI_TX2+_CONN
HDMI_TX2-_CONN	R258	1	@	2	0	0402	5%	HDMI_TX2-_CONN



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Size	Custom	Document Number	KIWB1/B2_LA4601P		Rev
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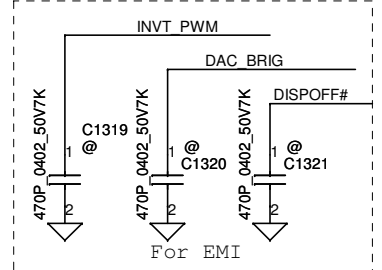
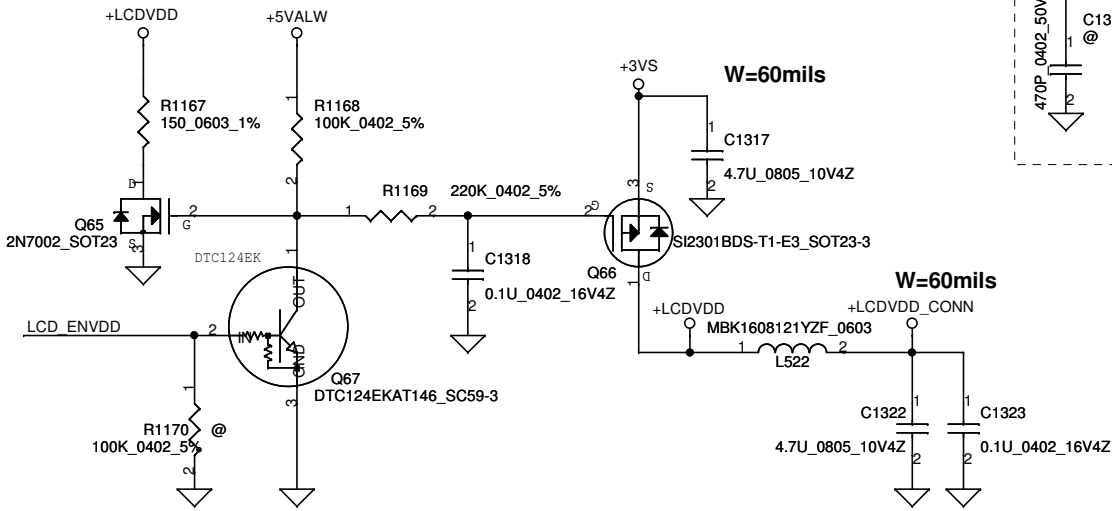


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				Document Number KIWB1/B2_LA4601P
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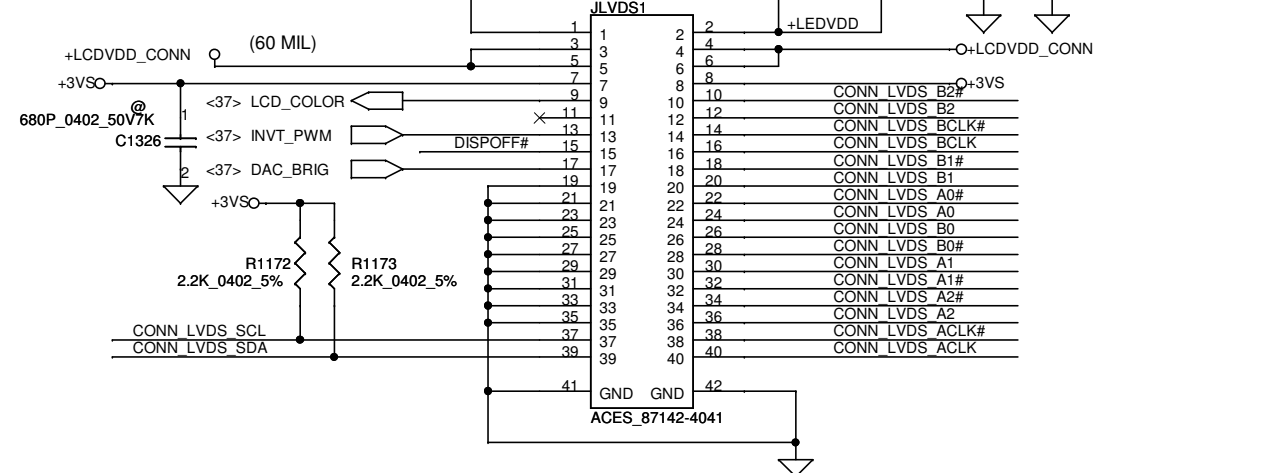


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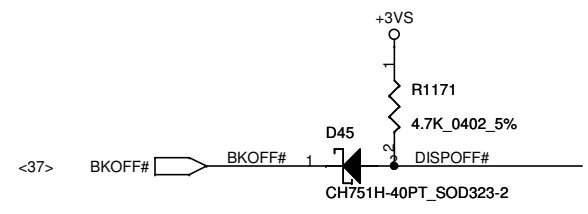
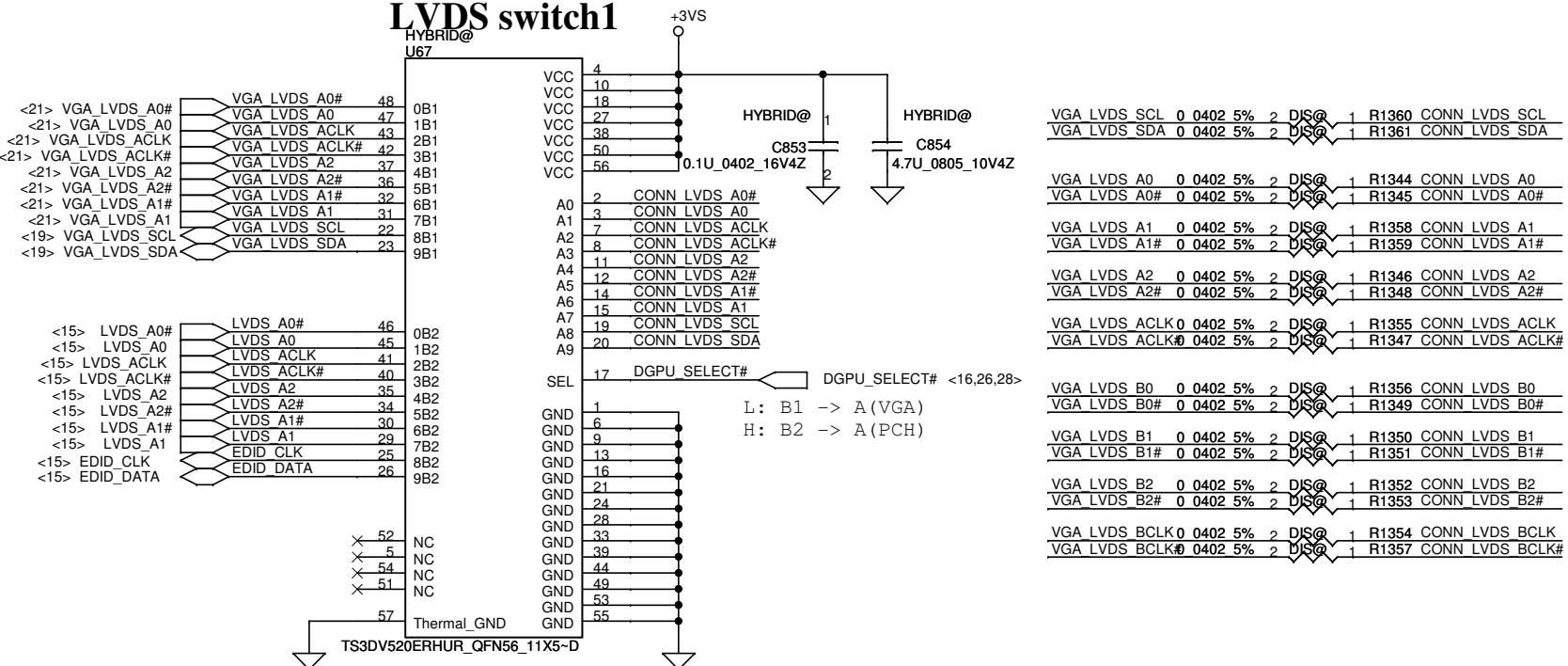
LCD POWER CIRCUIT



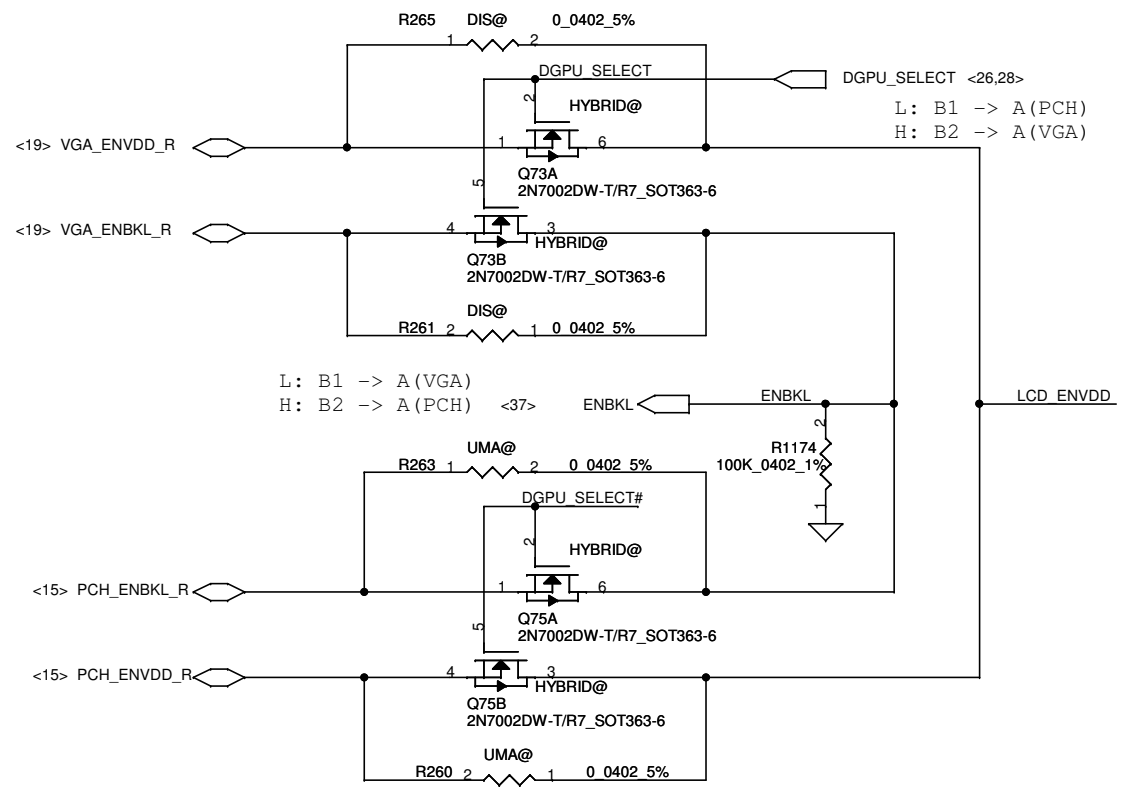
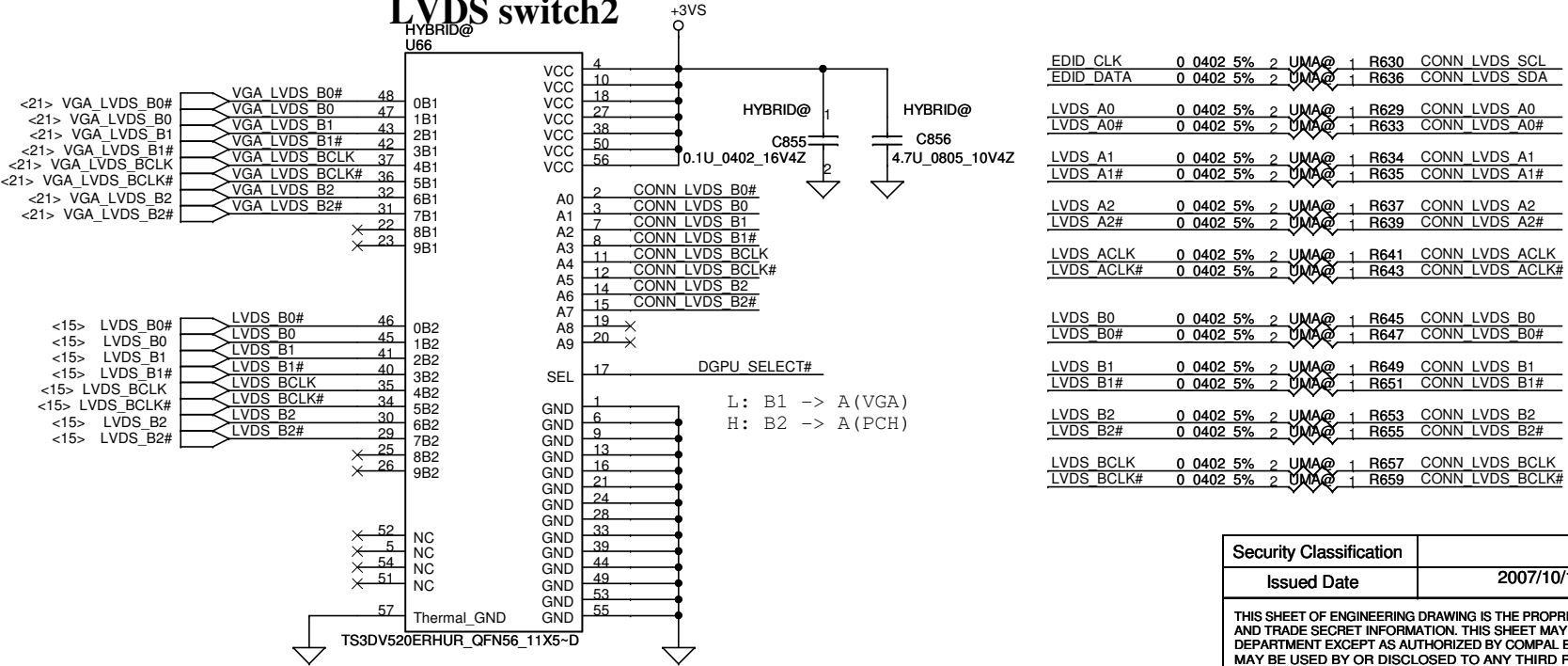
VGA LCD/PANEL BD. Conn.



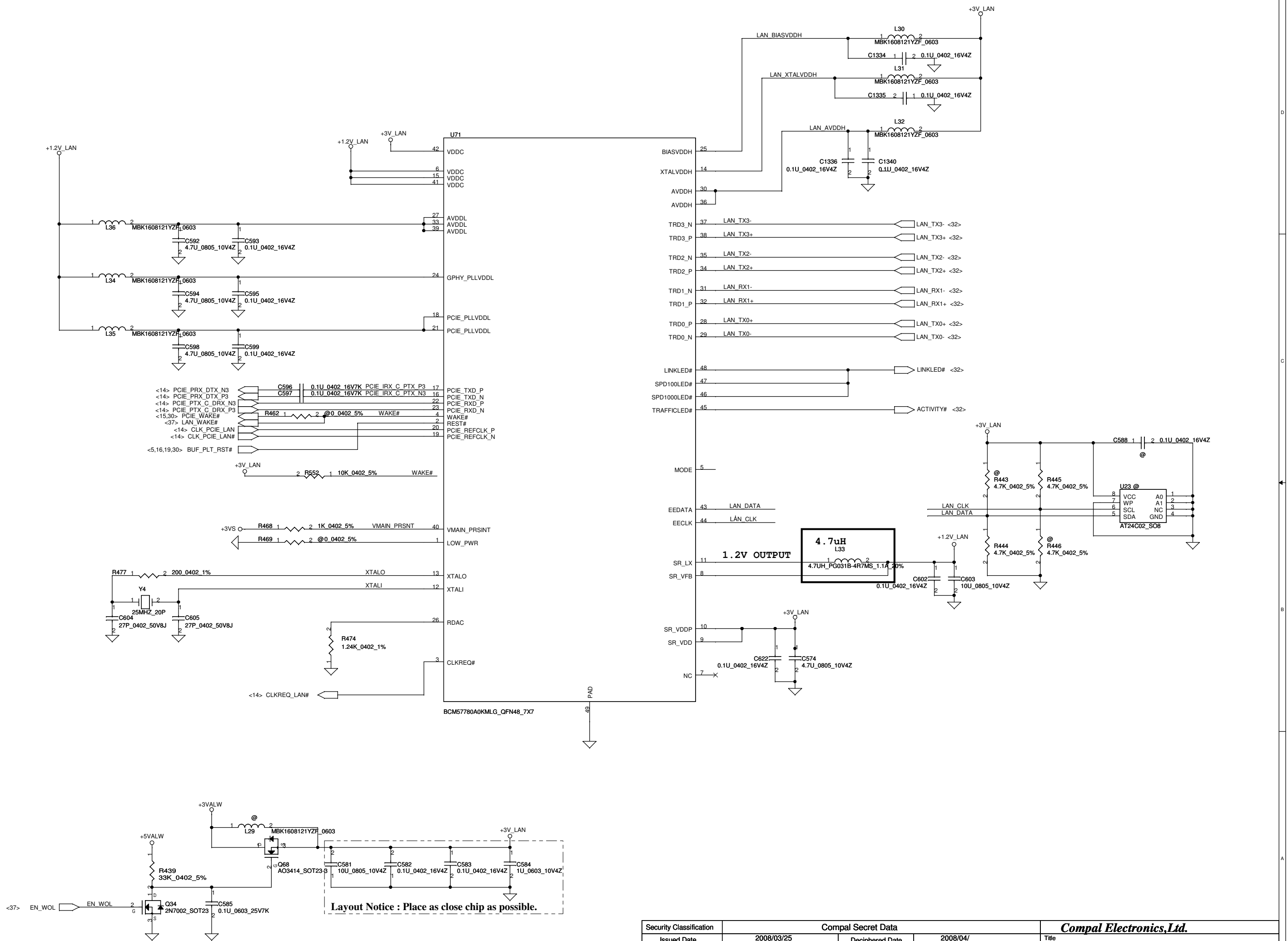
LVDS switch1



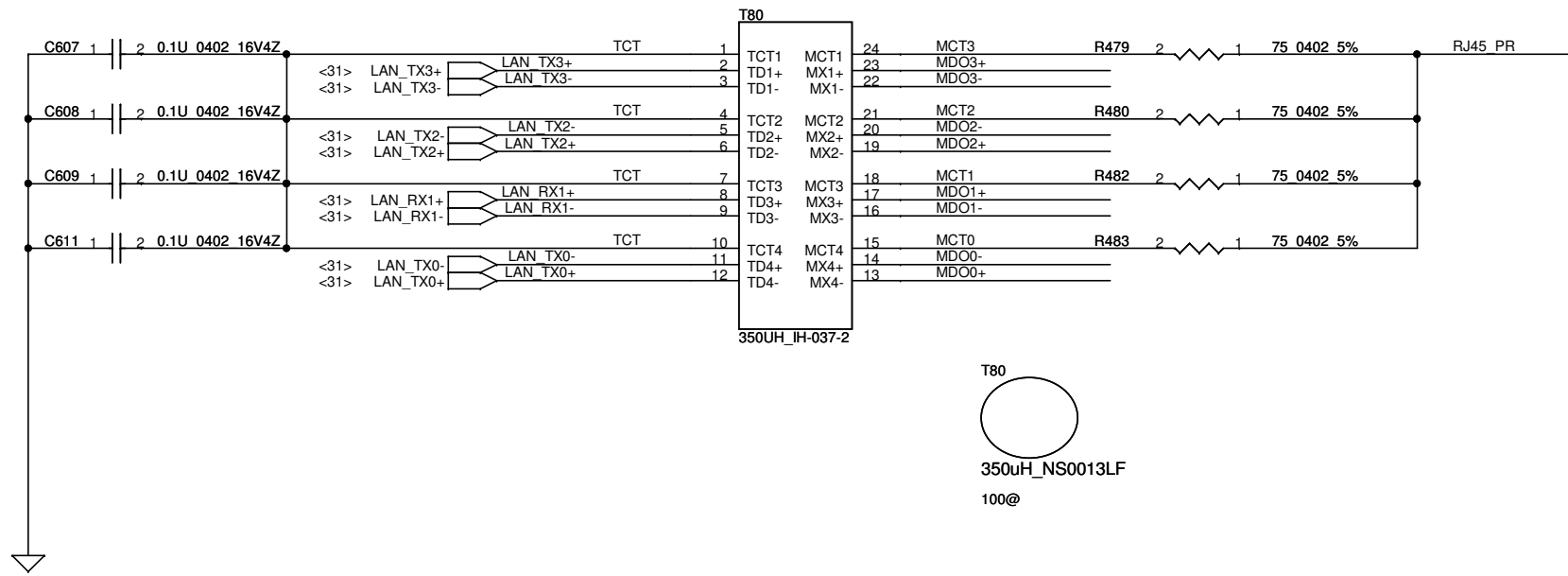
LVDS switch2



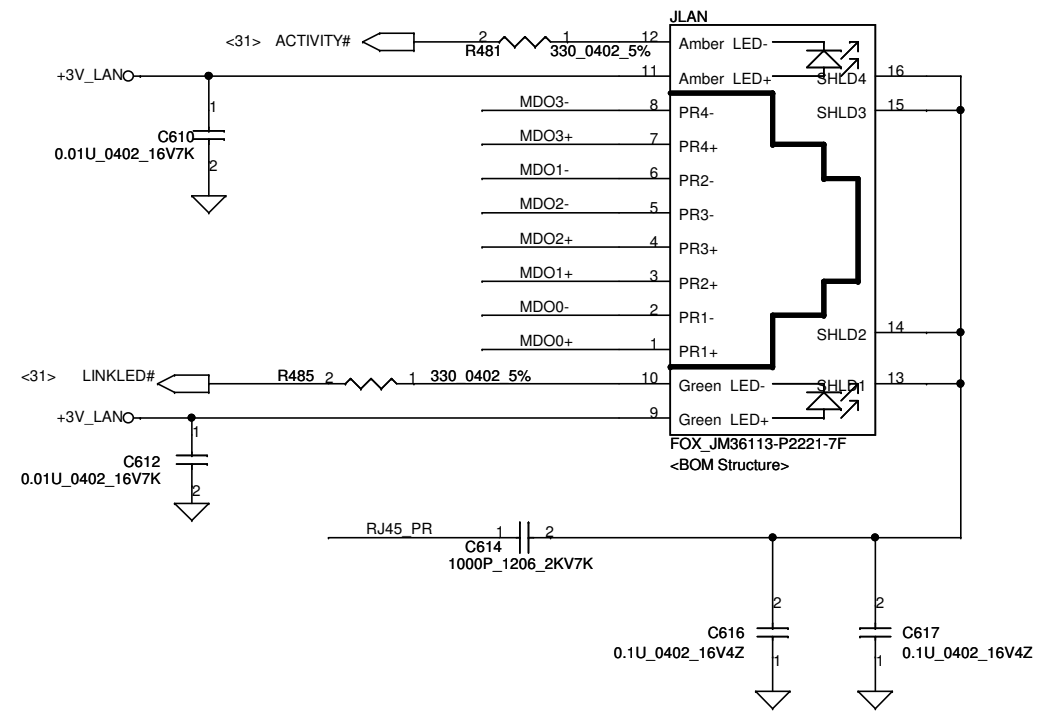
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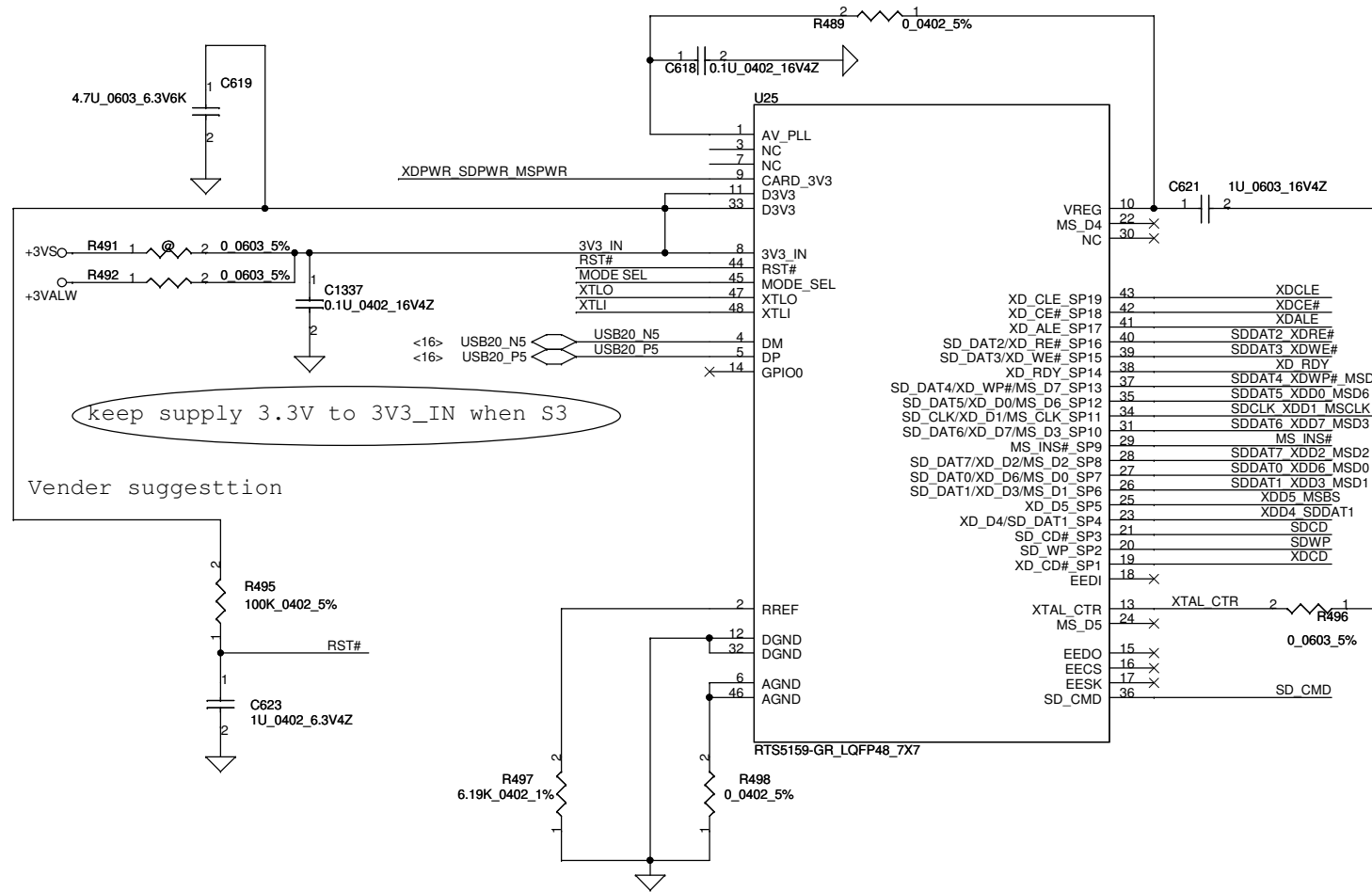


RJ11+RJ45 CONN

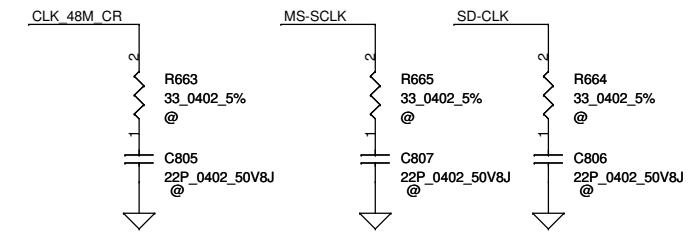
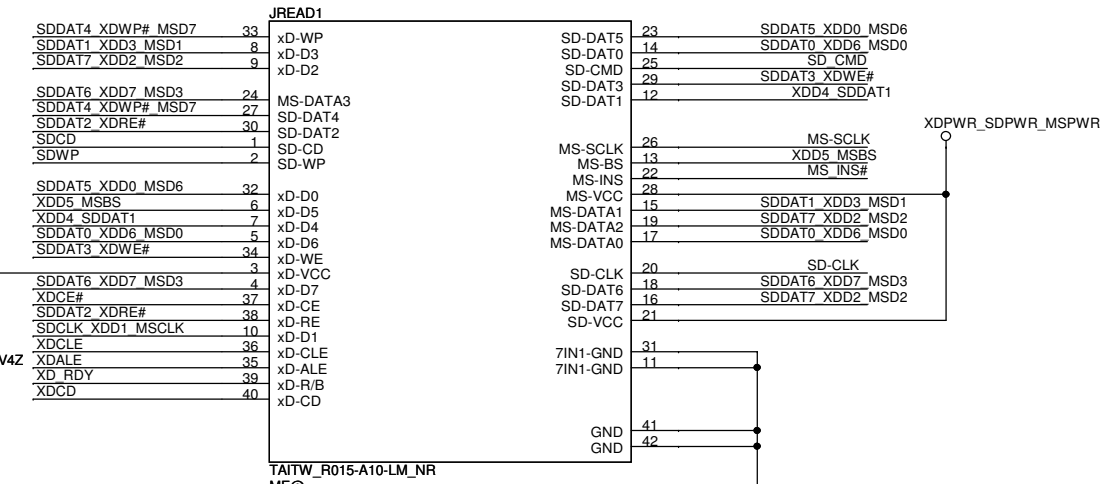


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0513 : CARD_3V3 旁路電阻 100K change to 4.7u CAP==>預留
 0521 : change C79 form 4.7u to 0.1u, add R47 100K ohm,
 change C526 form 1u to 4.7u

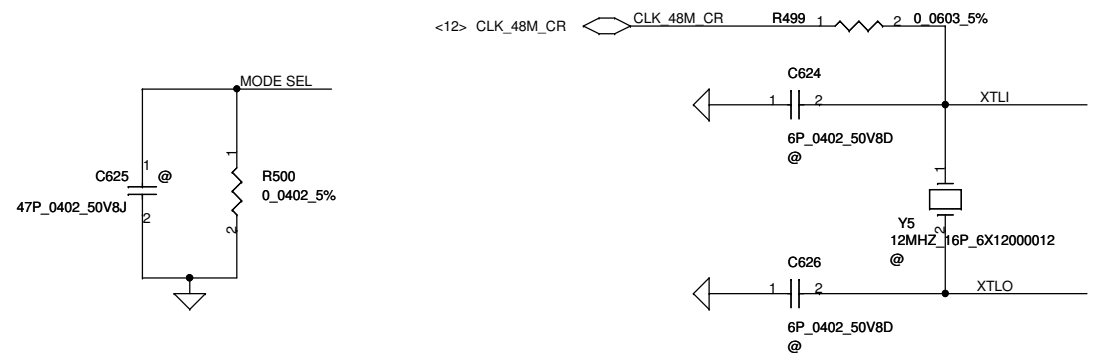


pin 13 (XTAL CTL)	CLOCK SOURCE	REMARK
FLOATING	12MHZ CRYSTAL INPUT	
PULL HIGH	CLOCK GENERATOR'S 48MHZ INPUT	INPUT TO PIN48

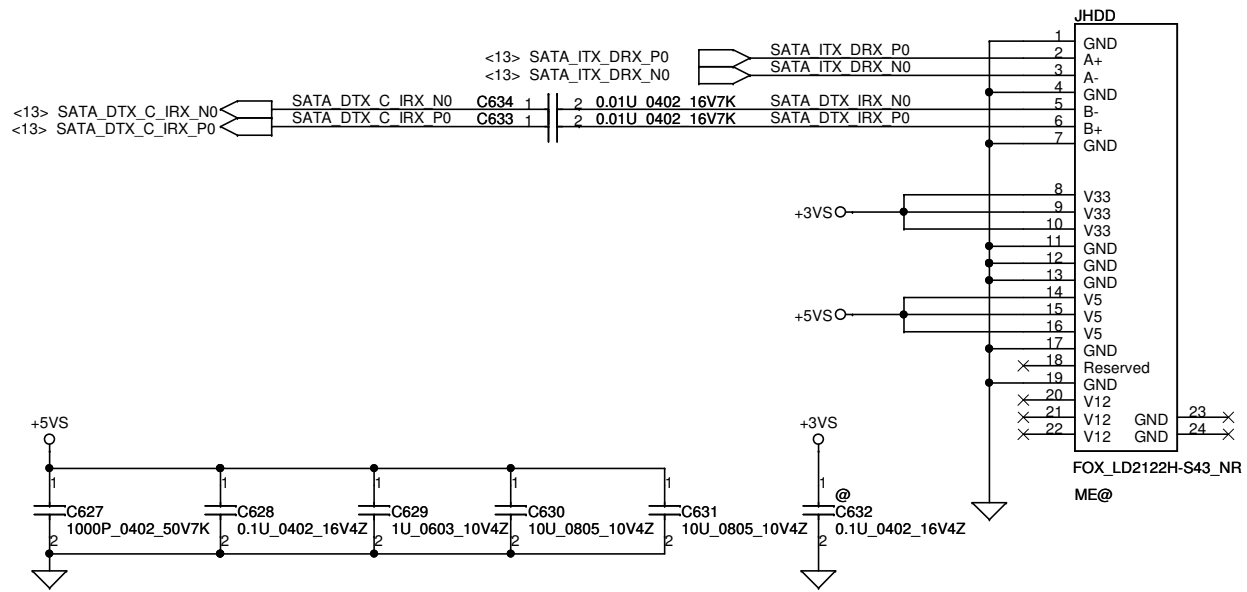


MSCLK and SDCLK 該二電阻是預留給EMI solution使用, (但請靠近RTS5158E側).

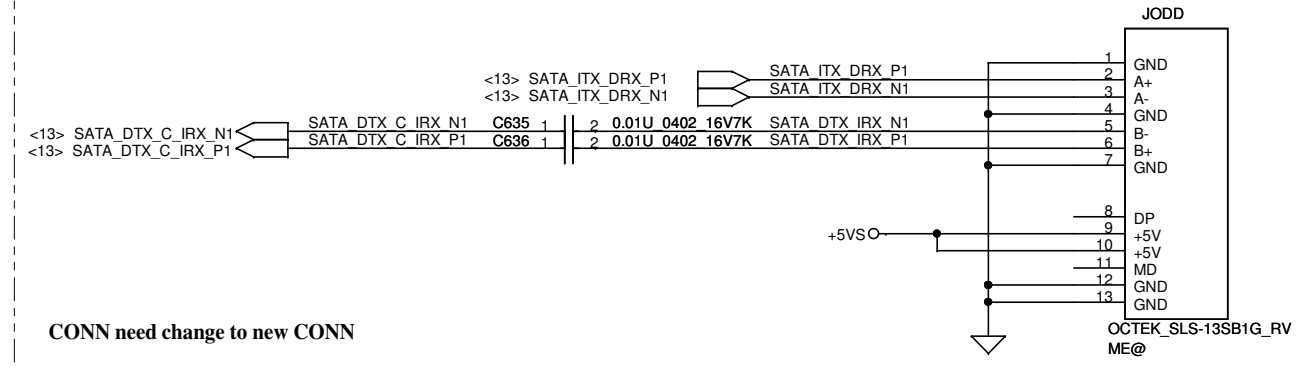
將SD_DAT1 連接到RTS5158E的pin23



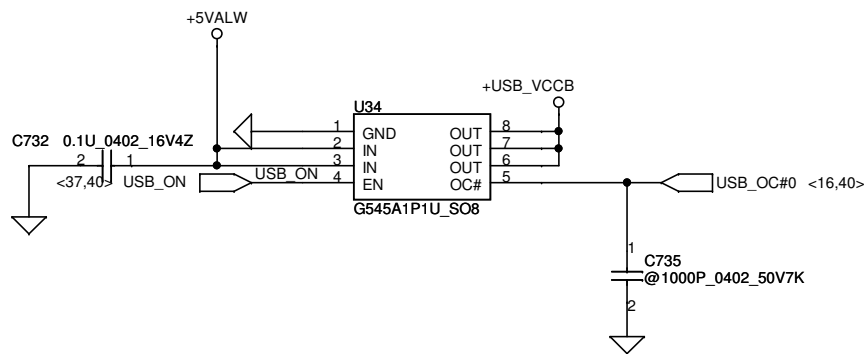
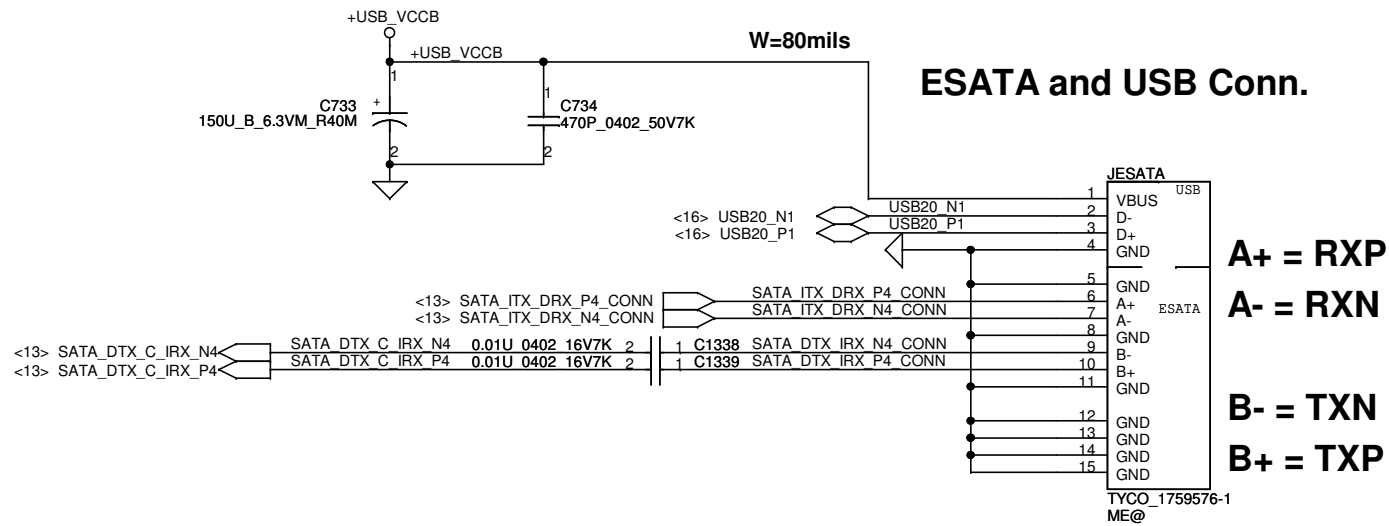
SATA HDD Conn.



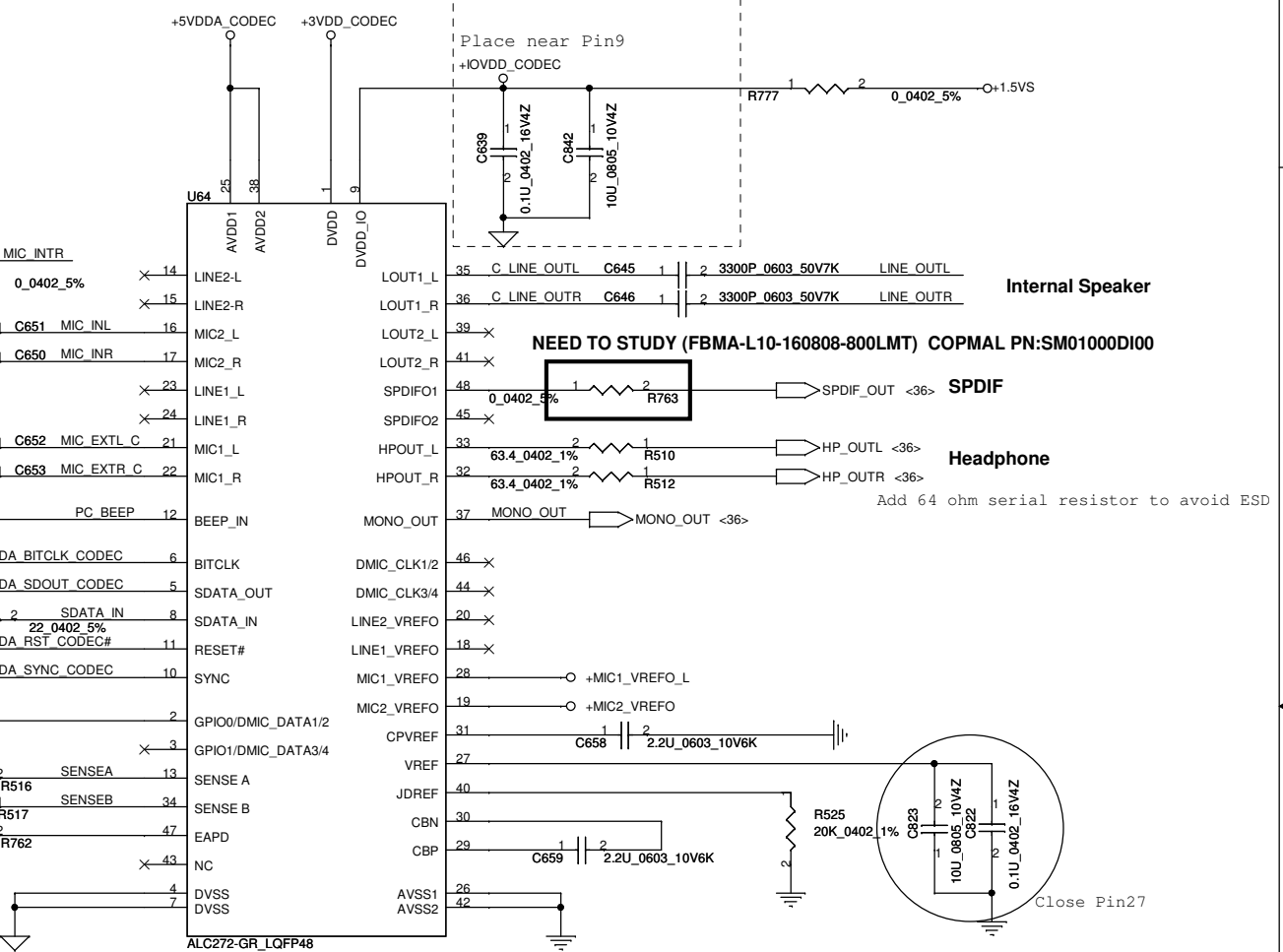
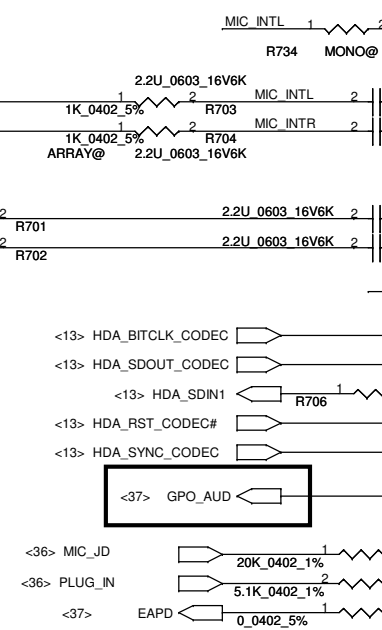
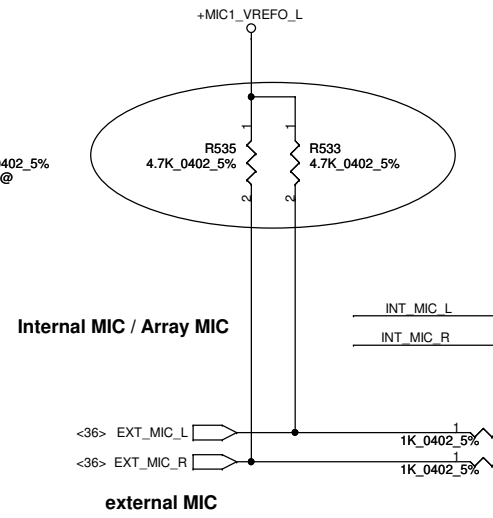
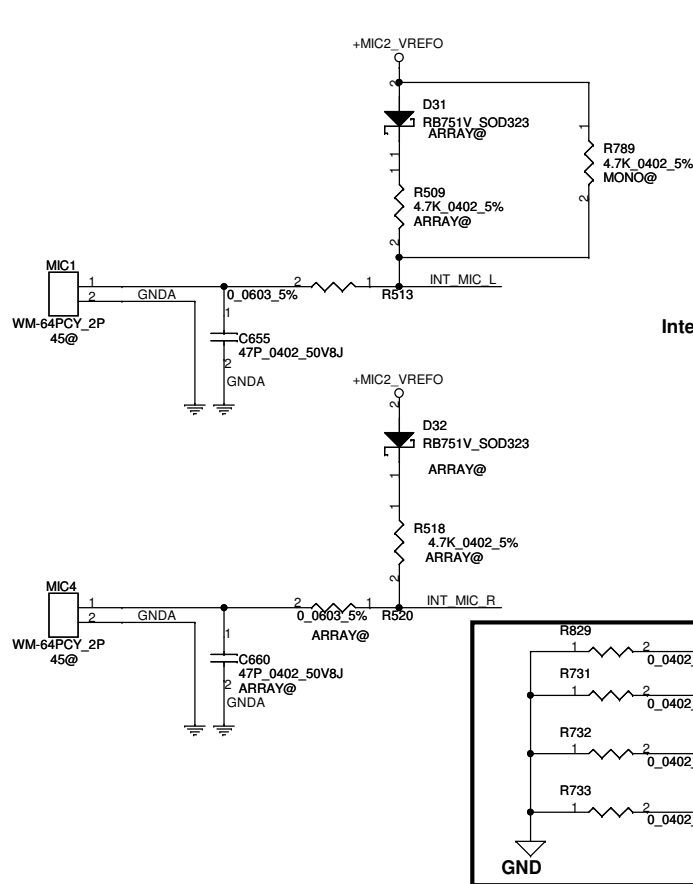
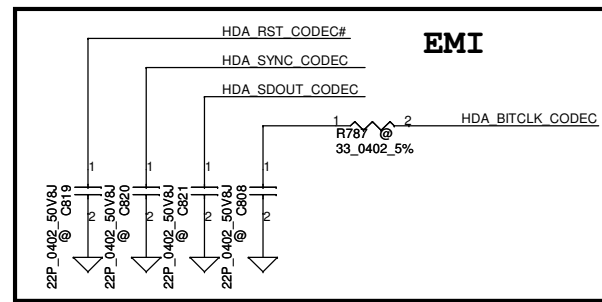
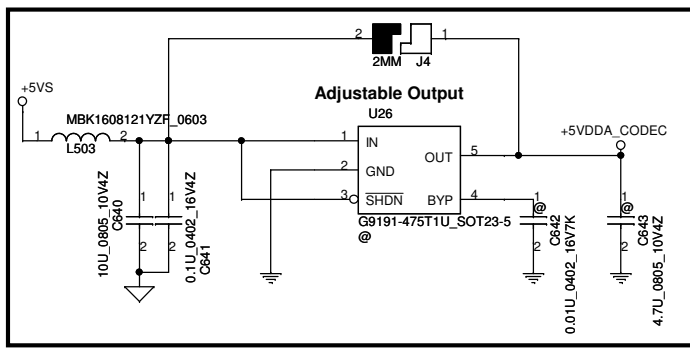
SATA ODD Conn.



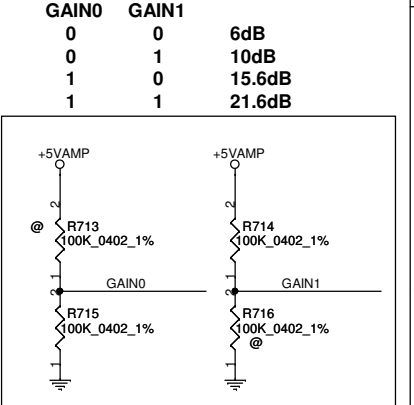
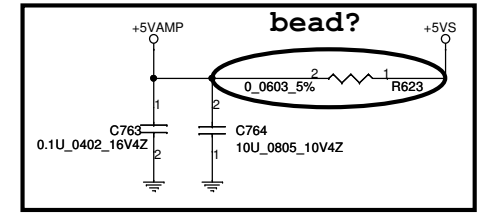
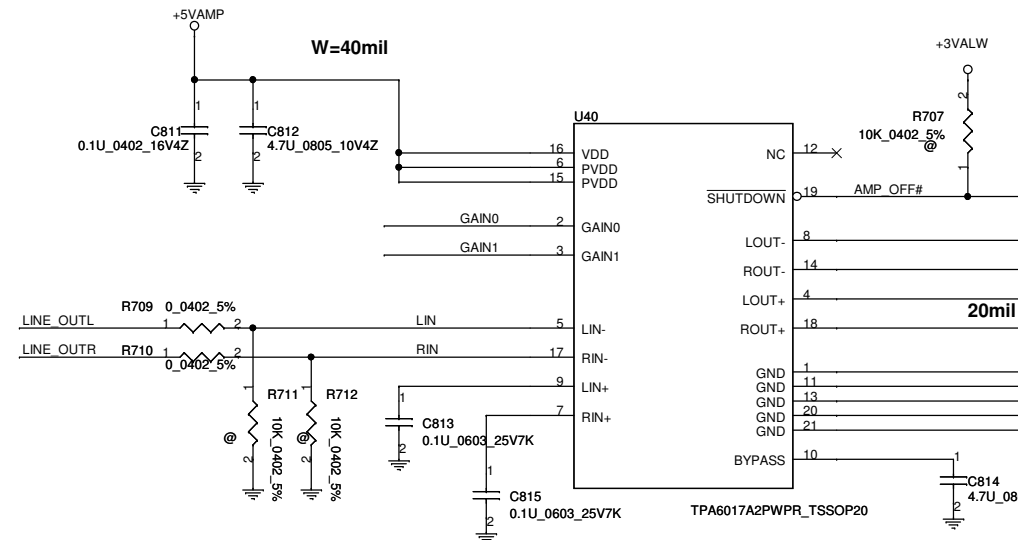
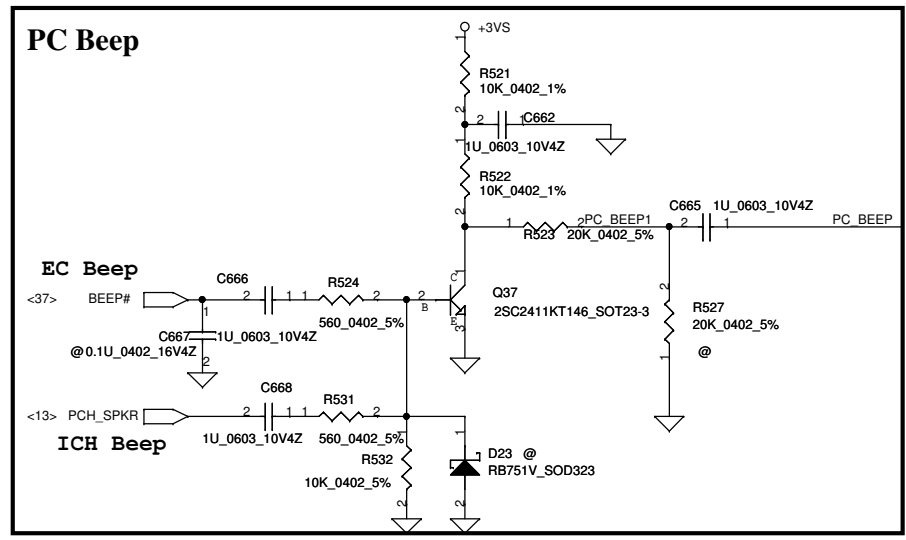
ESATA and USB Conn.



Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		HDD & ODD Connector	
2007/10/15		2008/10/15		NIWBA_LA5371P	
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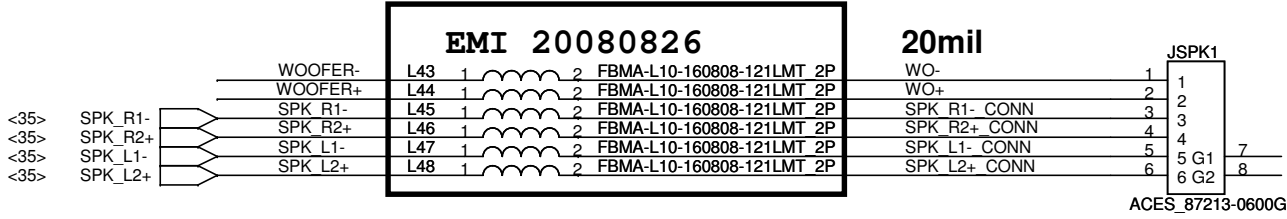


Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	Line in
MIC1 (Pin21/22)	External	Mic in
MONO-OUT (Pin37)	Internal	Internal Subwoofer
MIC2 (Pin16/17)	Internal	Internal Mic

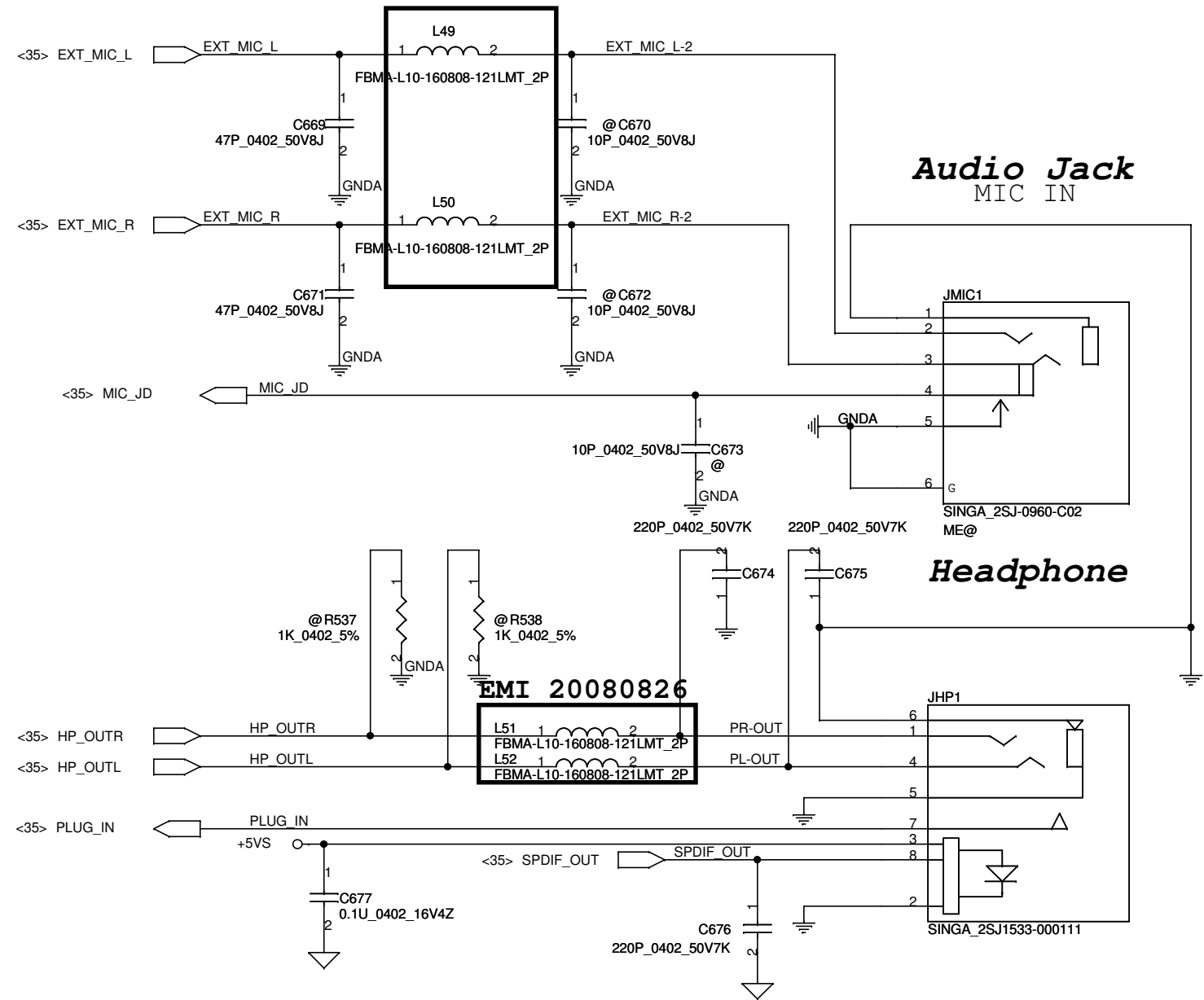


Security Classification	Compal Secret Data		Title HD Audio Codec_ALC272
Issued Date	2008/03/25	Deciphered Date	
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Size	Document Number	Rev	
C	NIWBA_LA5371P	0.1	
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**SubWoofer Conn.
Speaker Connector**

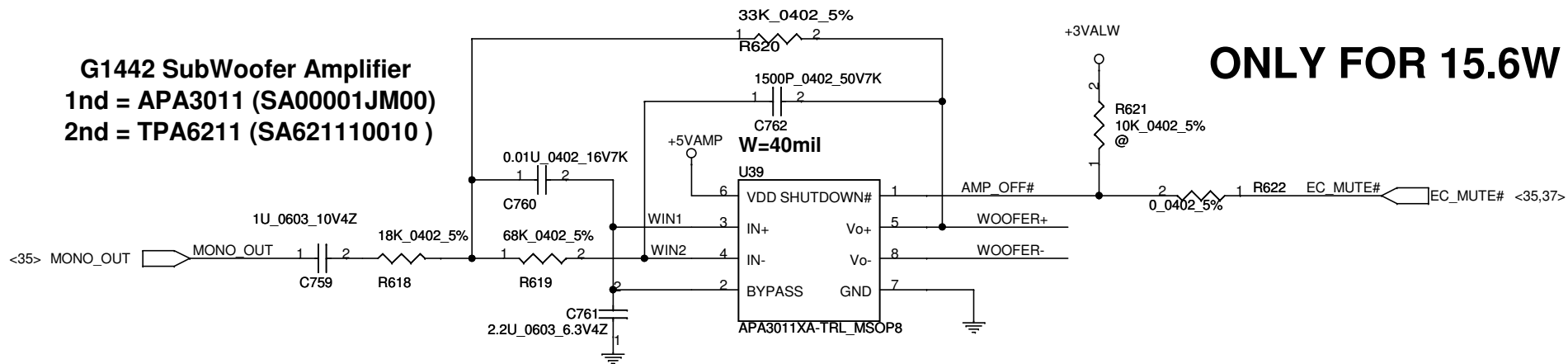


**Audio Jack
EMI 20080826**

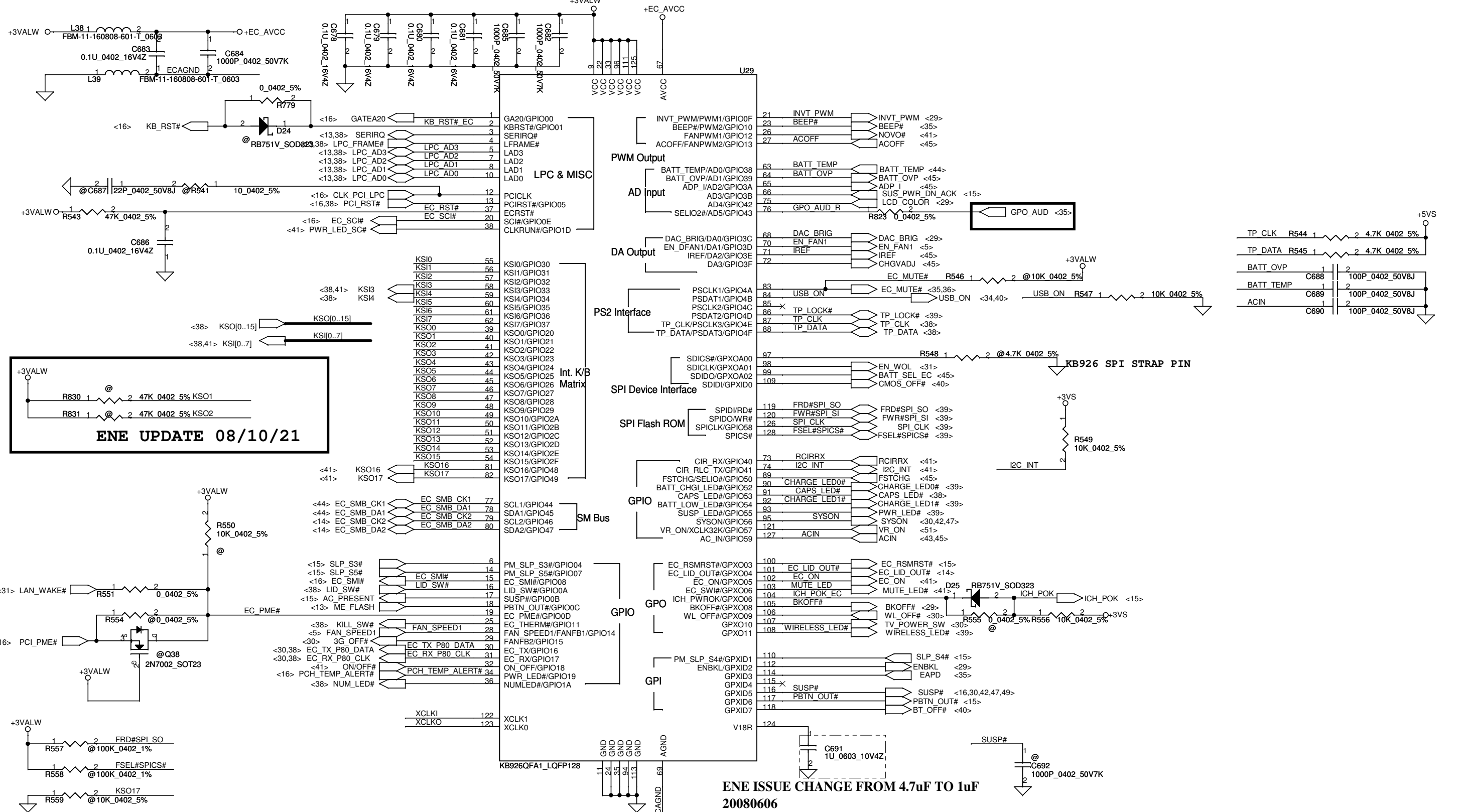


**G1442 SubWoofer Amplifier
1nd = APA3011 (SA00001JM00)
2nd = TPA6211 (SA621110010)**

ONLY FOR 15.6W



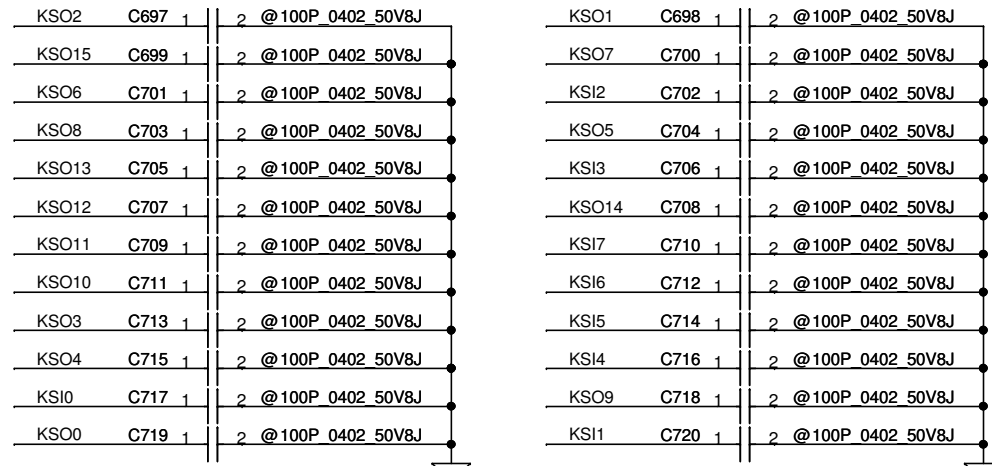
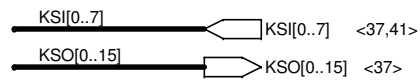
Security Classification	Compal Secret Data		Title AMP,Audio speaker CONN
Issued Date	2008/03/25	Deciphered Date	
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	KIWB1/B2_LA4601P	0.1	
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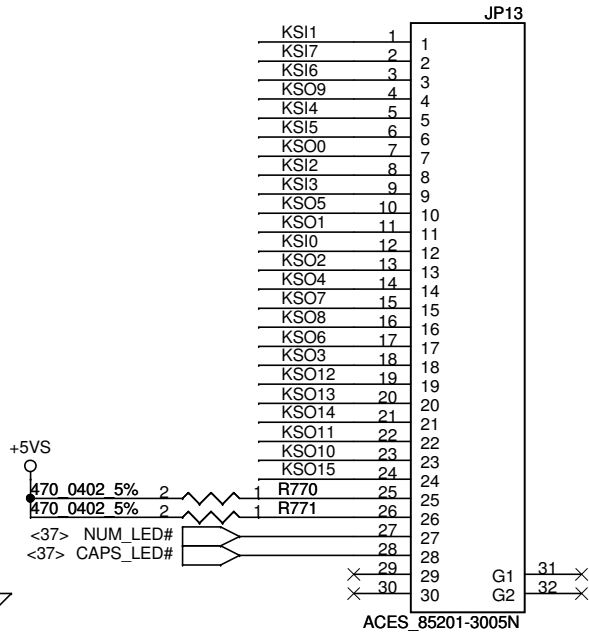
Security Classification	Compal Secret Data		Title BIOS & EC I/O Port
Issued Date	2007/10/15	Deciphered Date	
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Date:	Tuesday, March 24, 2009	Sheet	37 of 52

Compal Electronics, Inc.
BIOS & EC I/O Port
 Rev 0.1
 Date: Tuesday, March 24, 2009 | Sheet 37 of 52

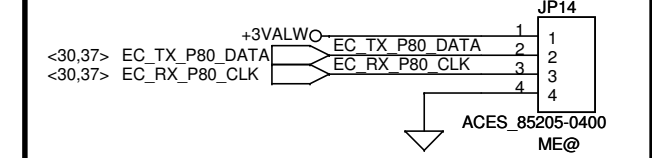
INT_KBD Conn.



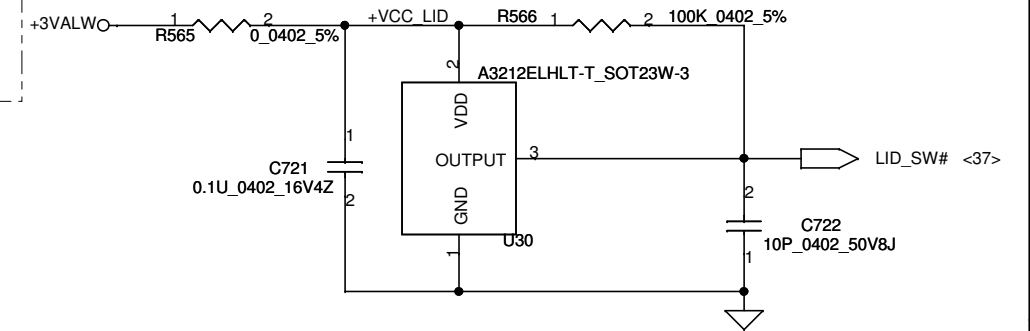
CONN PIN define need double check



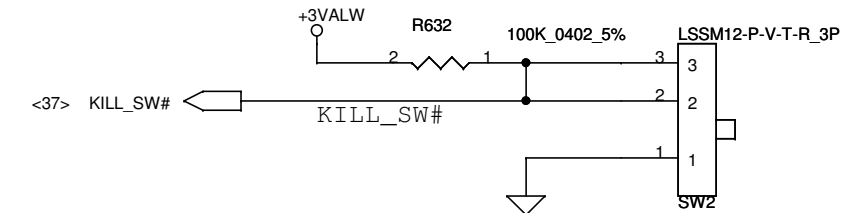
EC DEBUG PORT



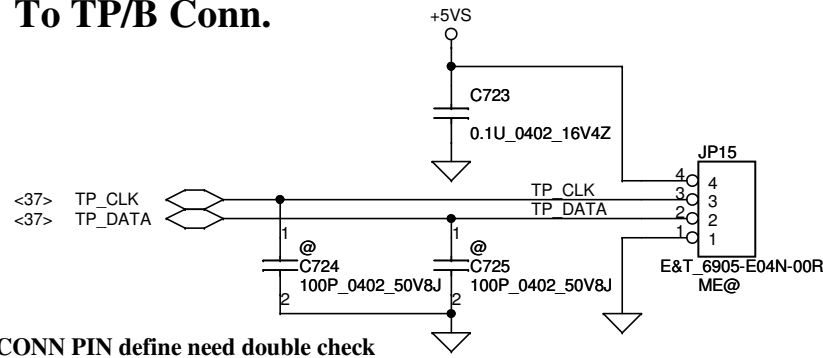
Lid Switch



Kill Switch

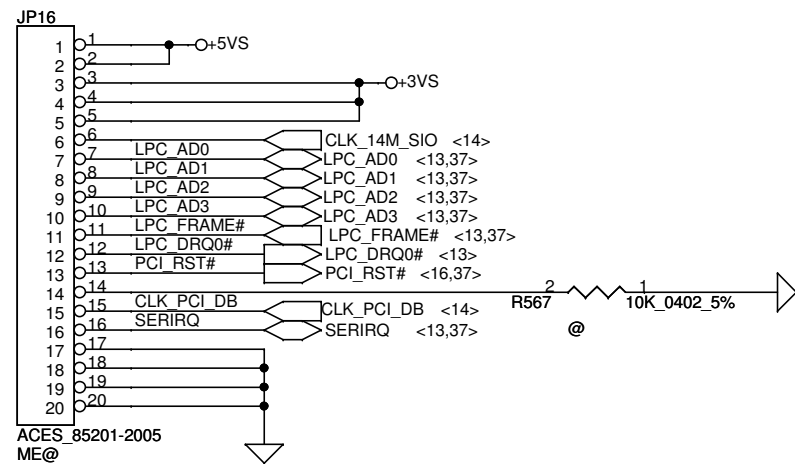


To TP/B Conn.



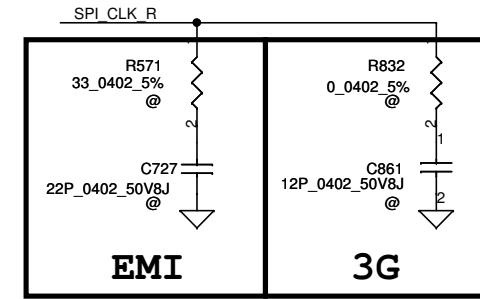
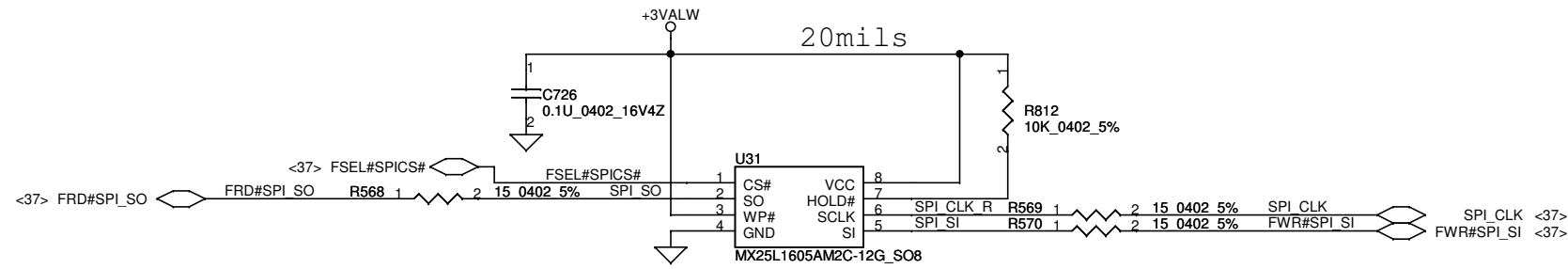
CONN PIN define need double check

FOR LPC SIO DEBUG PORT



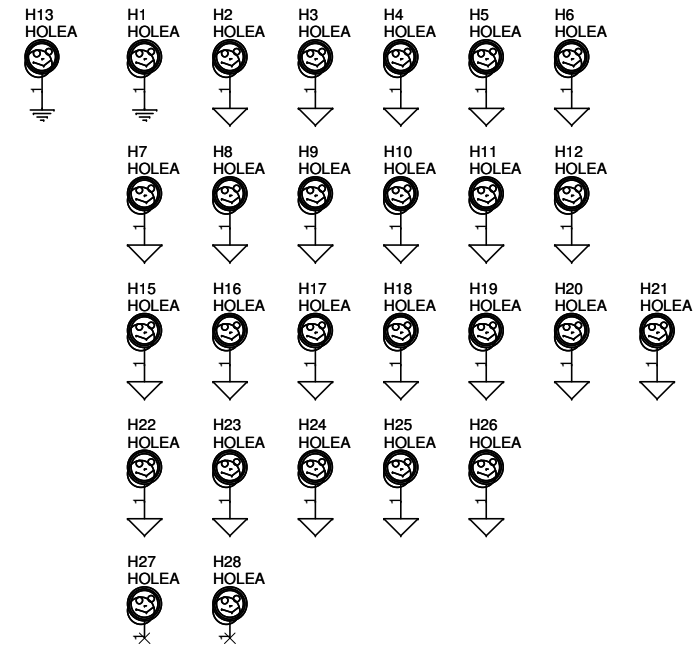
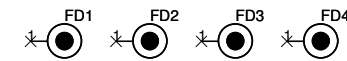
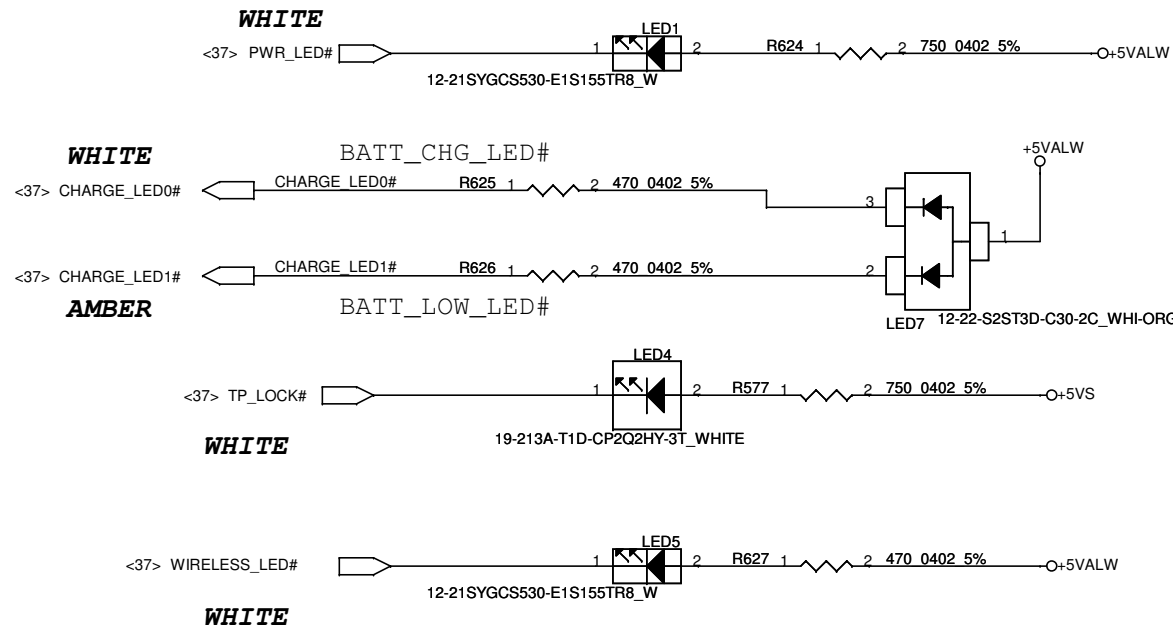
Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	KB /SW /LPC Debug Conn.
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Date:	Tuesday, March 24, 2009	Sheet	38	of 52

FOR EC 16M SPI ROM

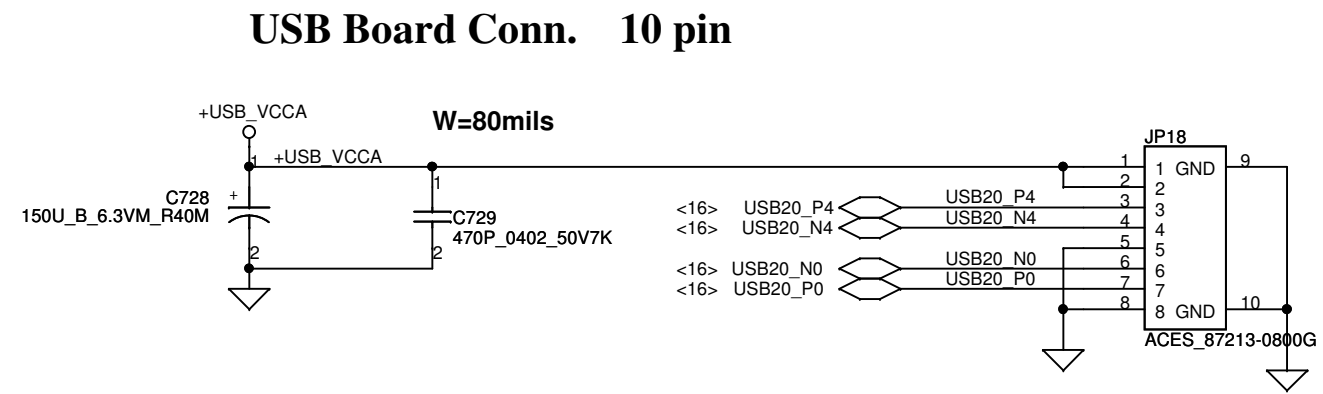
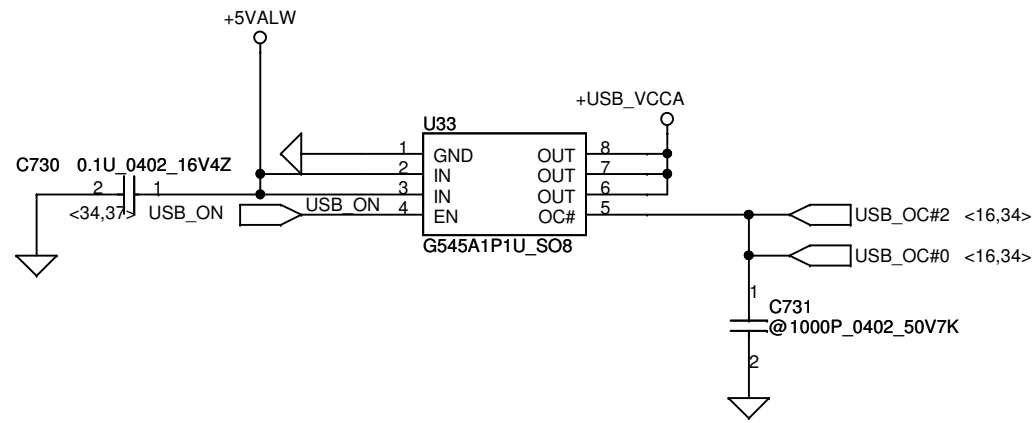


LED

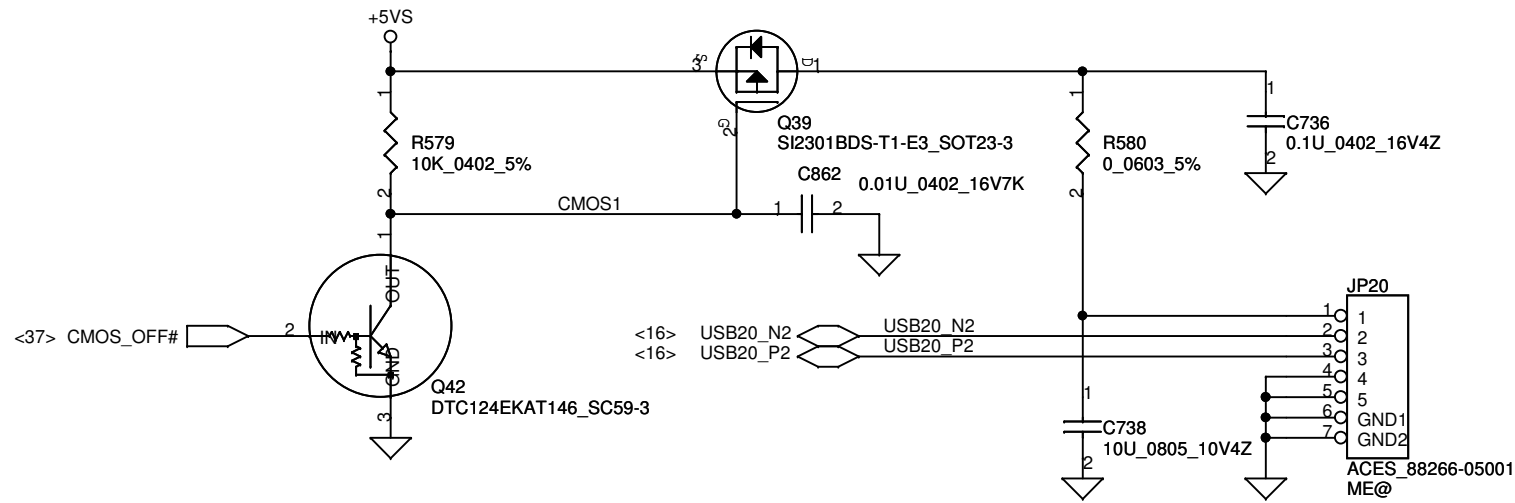
SC500005B00, If=5mA, Vf=2.7V~3.15V, R=460~390ohm



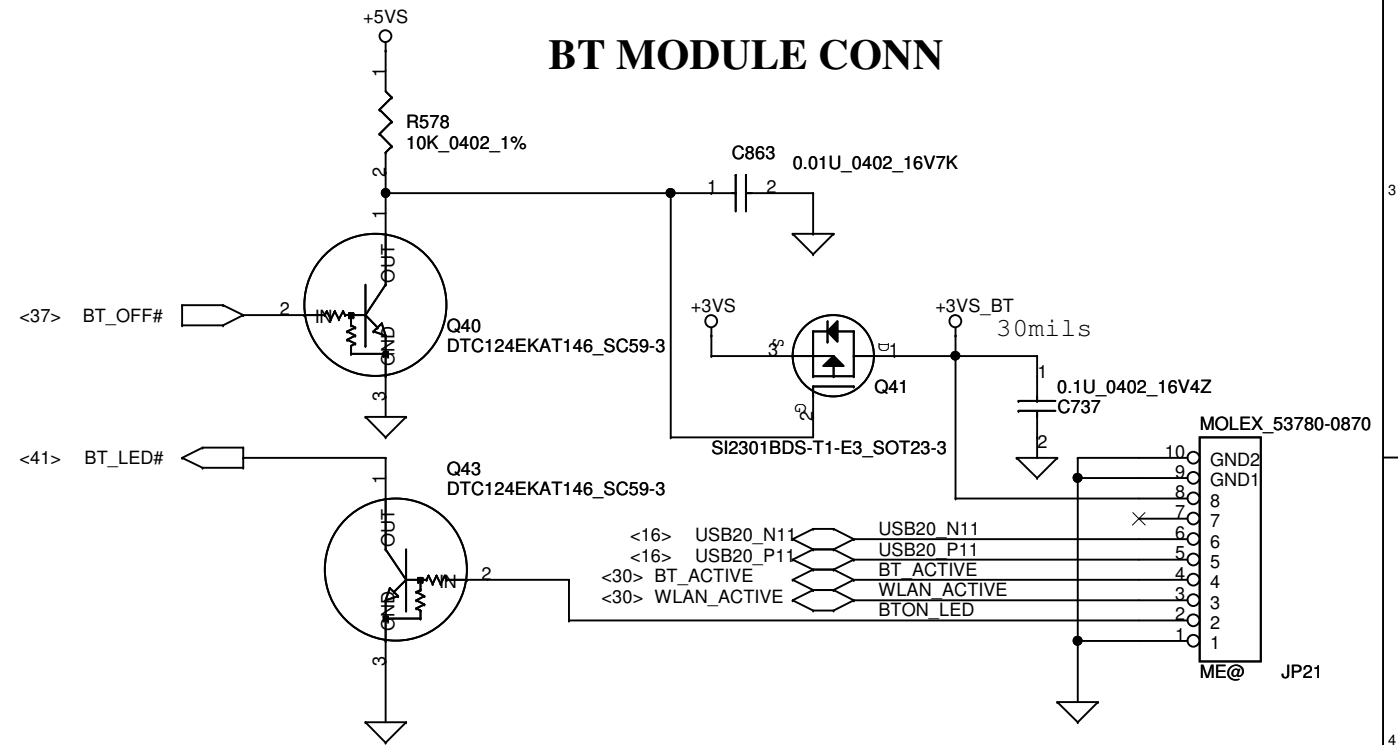
Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	LED/EC SPI ROM
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				Document Number NIWBA_LA5371P
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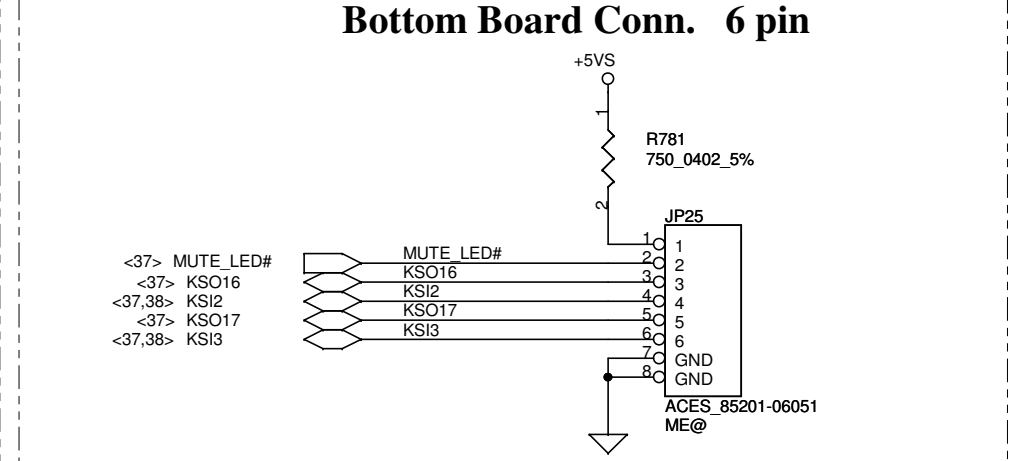
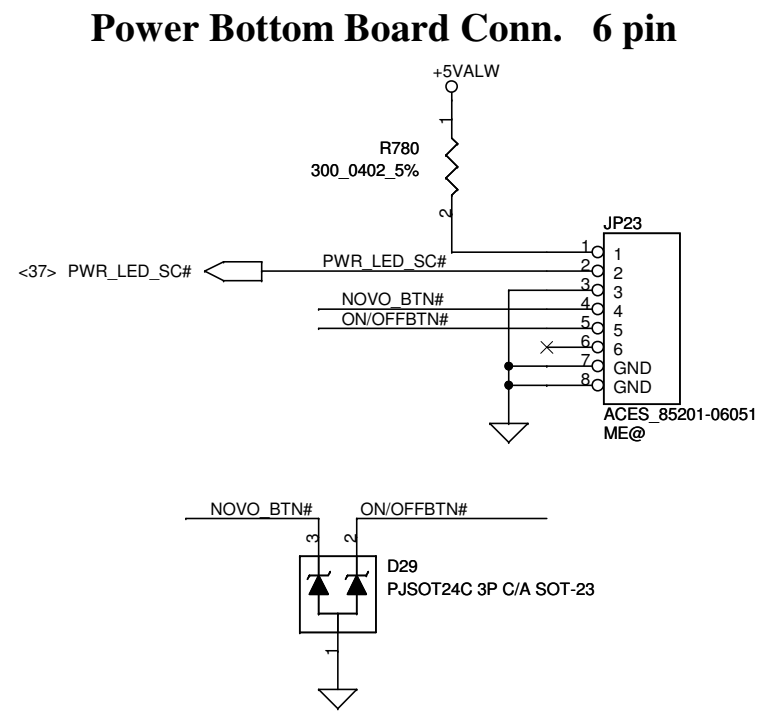
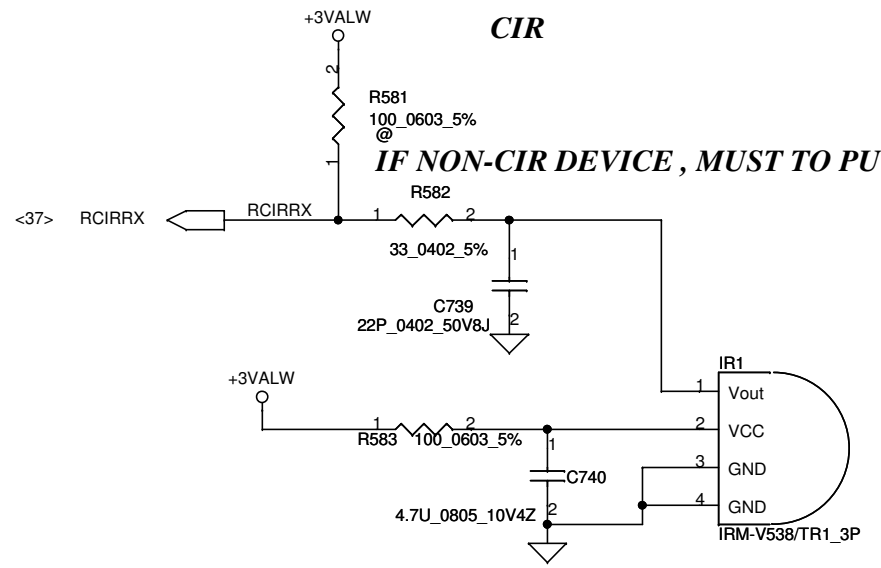
CMOS Camera Conn



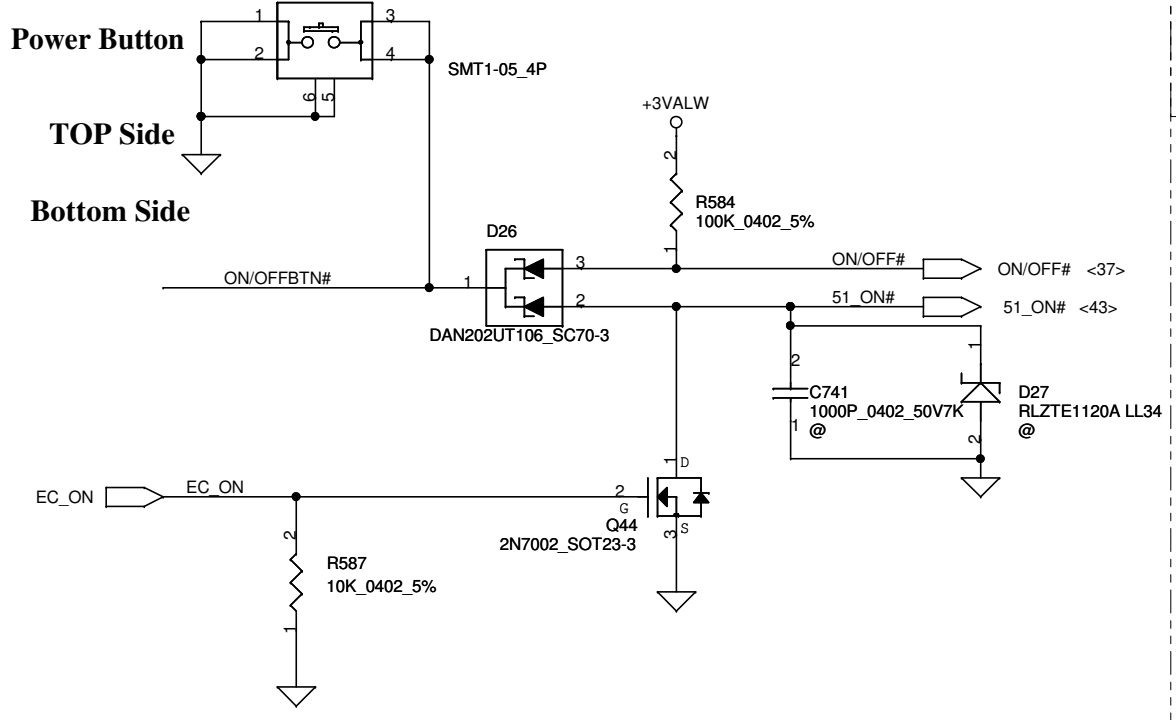
BT MODULE CONN



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Size Custom		Document Number		Rev
		NIWBA_LA5371P		0.1
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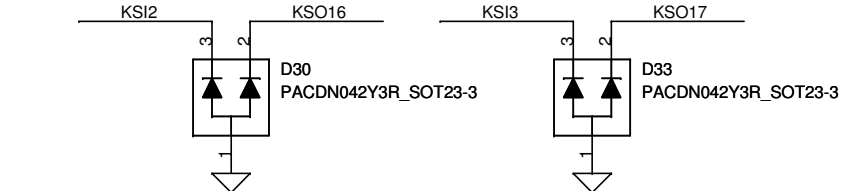


ON/OFF switch



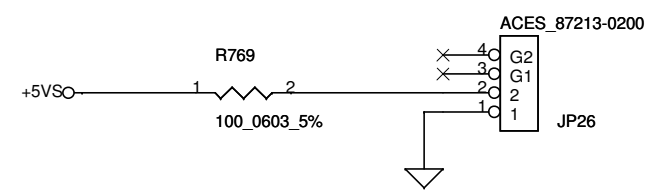
EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

EMI REQUEST 1ST = SCA00000G00
2ST = SCA00000T00

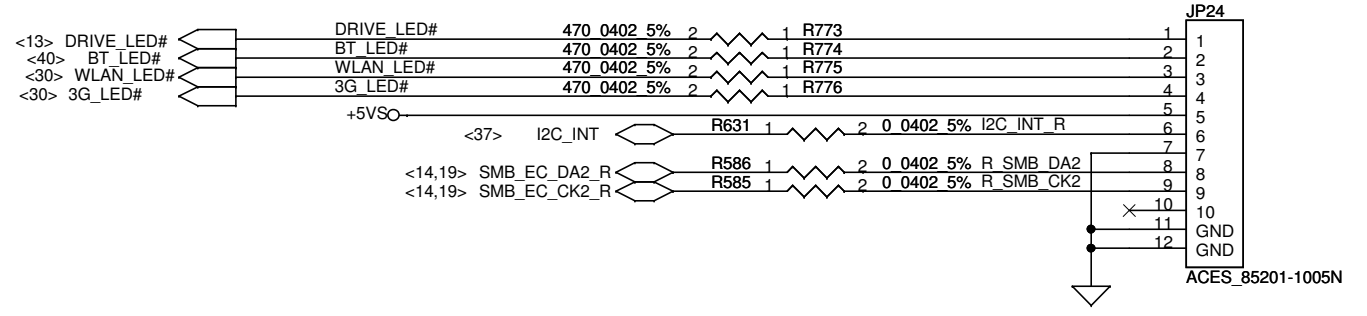
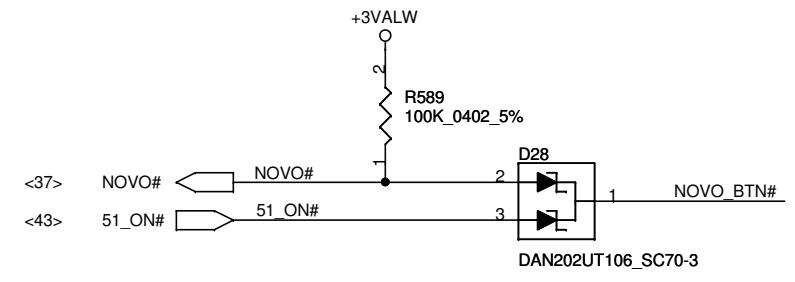


BTN FUNCTION	KEY MATRIX	
	IN	OUT
MUTE BTN	KSO17	KSI3
DOWN	KSO17	KSI2
UP	KSO16	KSI2

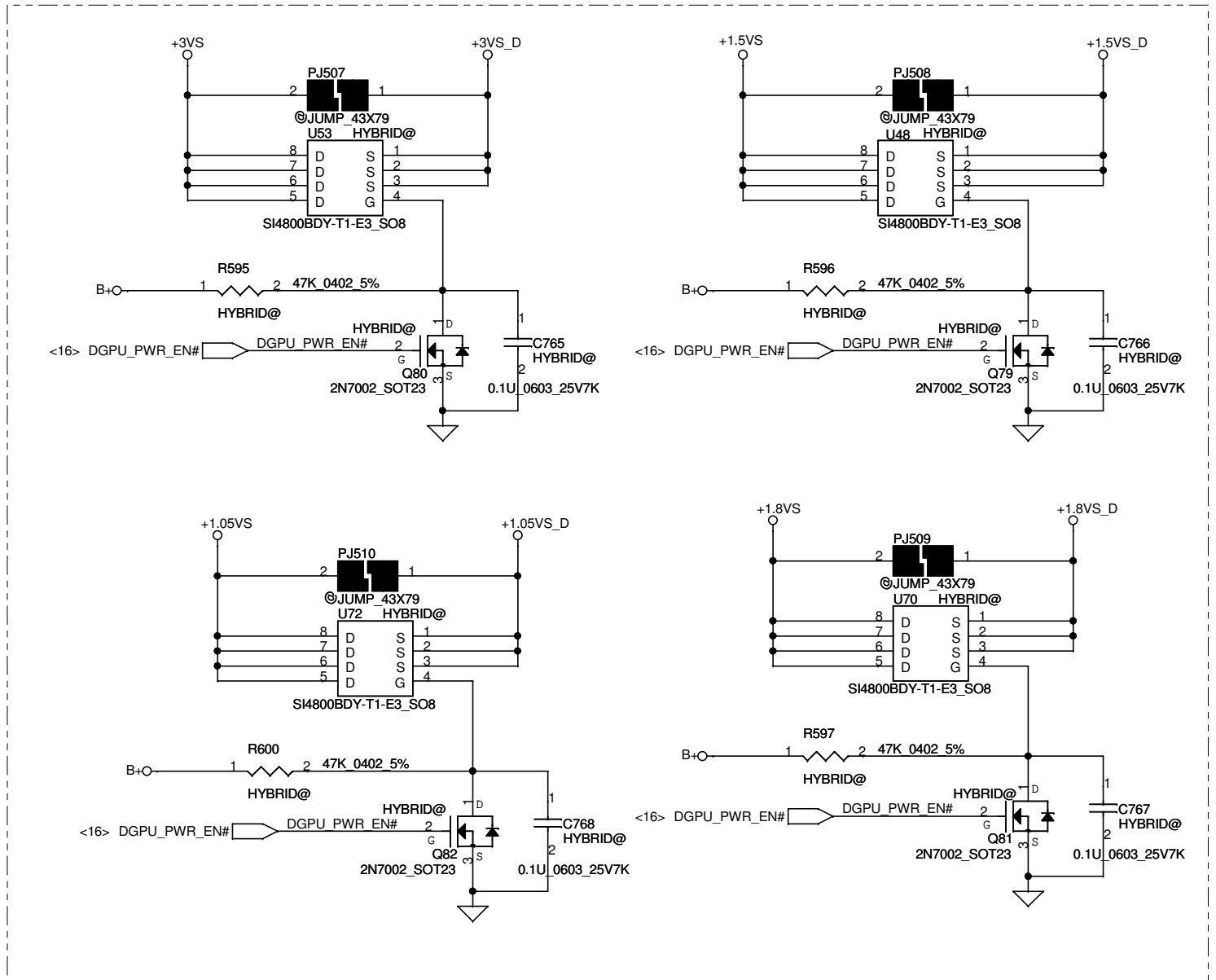
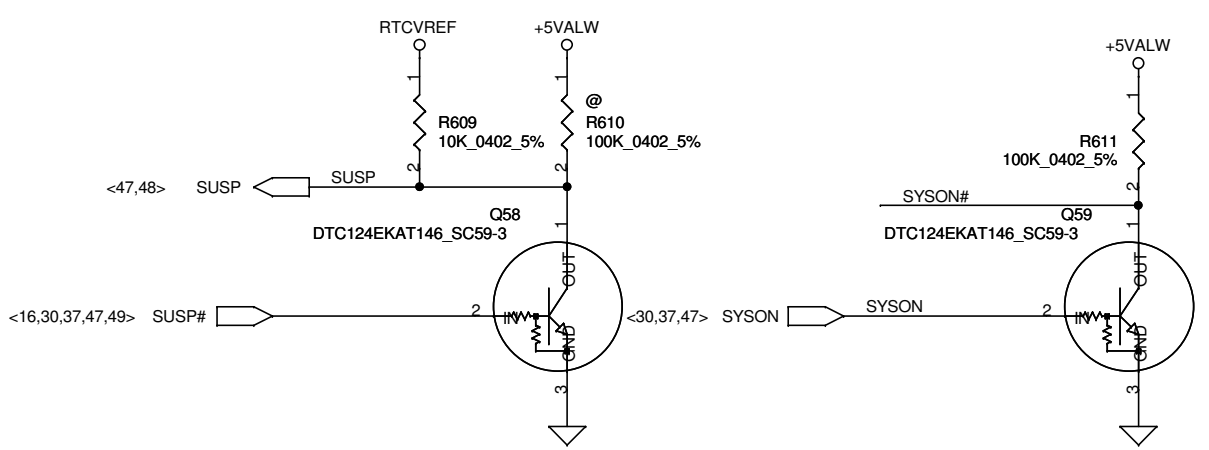
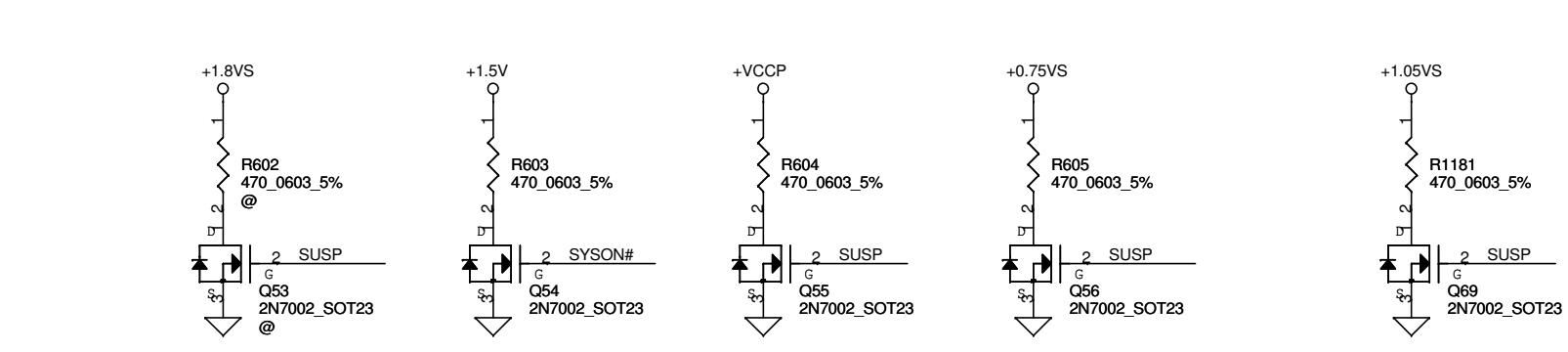
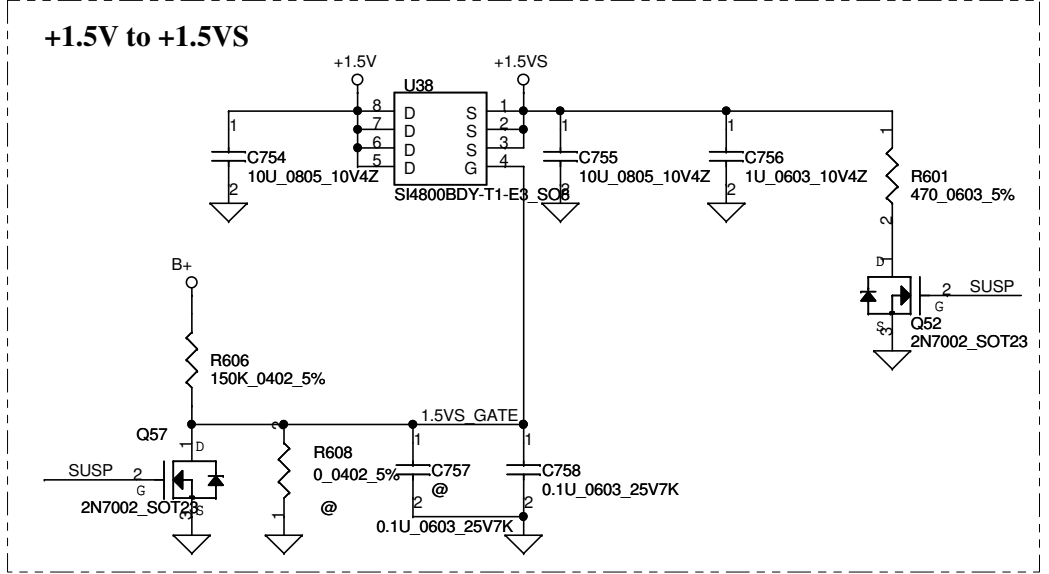
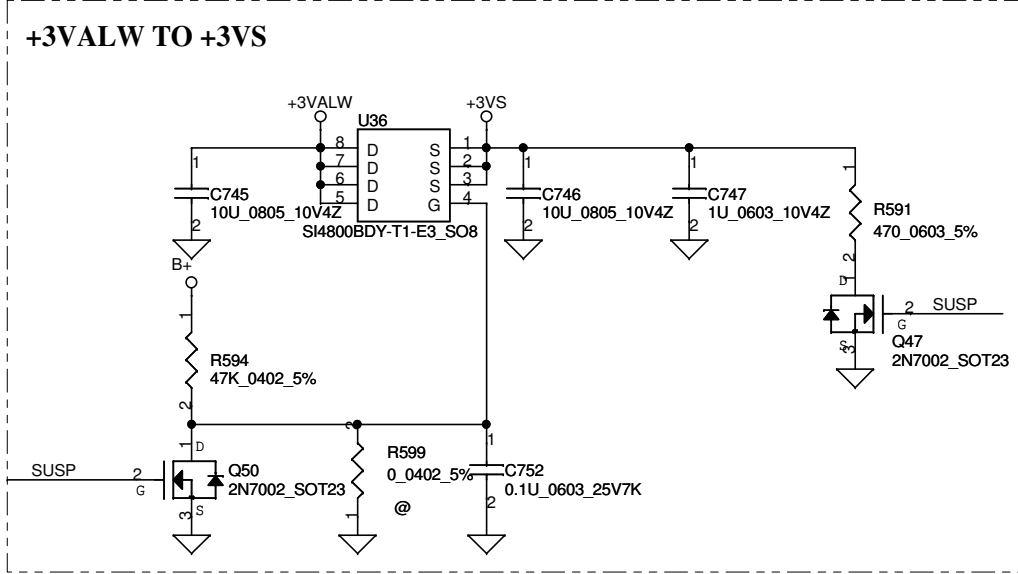
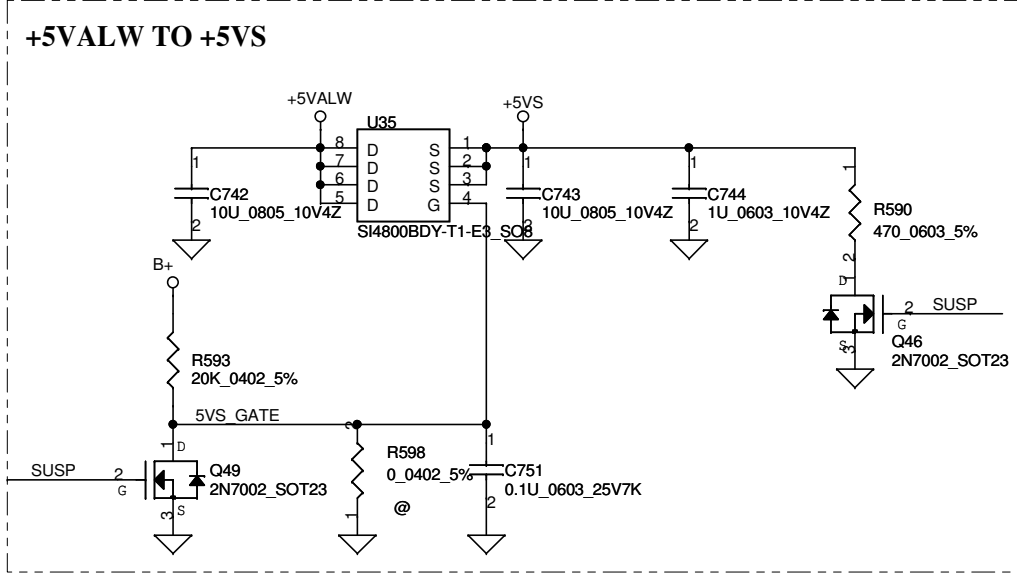
IDEAPAD BOARD 2PIN



Slide Board Conn. 10 pin

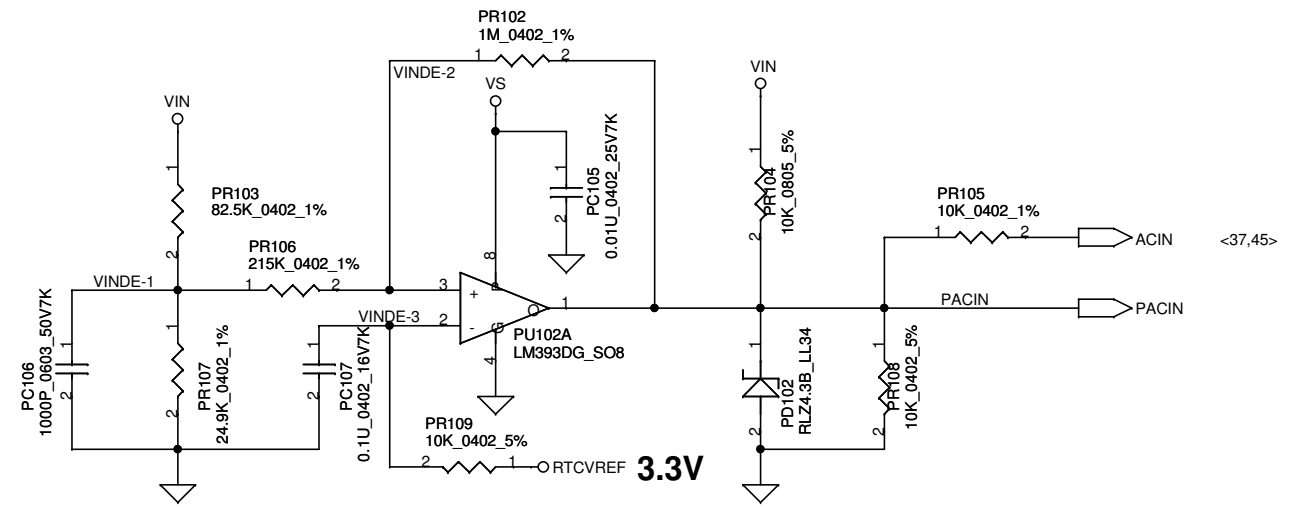
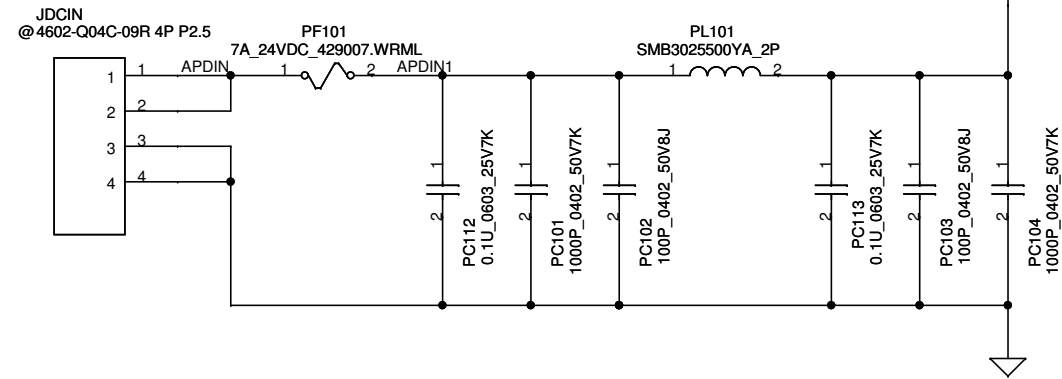


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Size	Document Number	Rev		0.1
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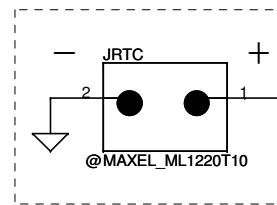
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title		
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				Size	Document Number	Rev
				Custom	NIWBA_LA5371P	0.1
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DC030006J00

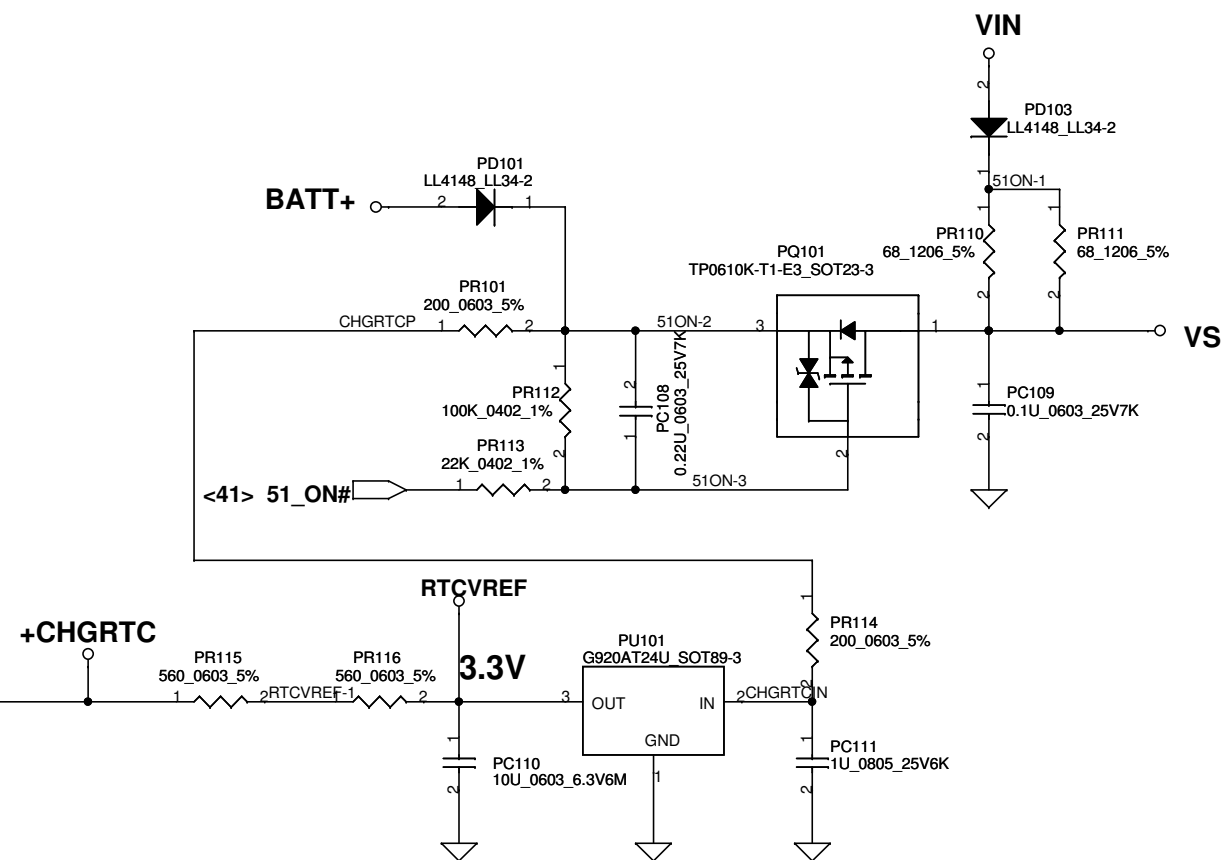


Vin Detector		
High	18.135	17.566
Low	14.866	14.063

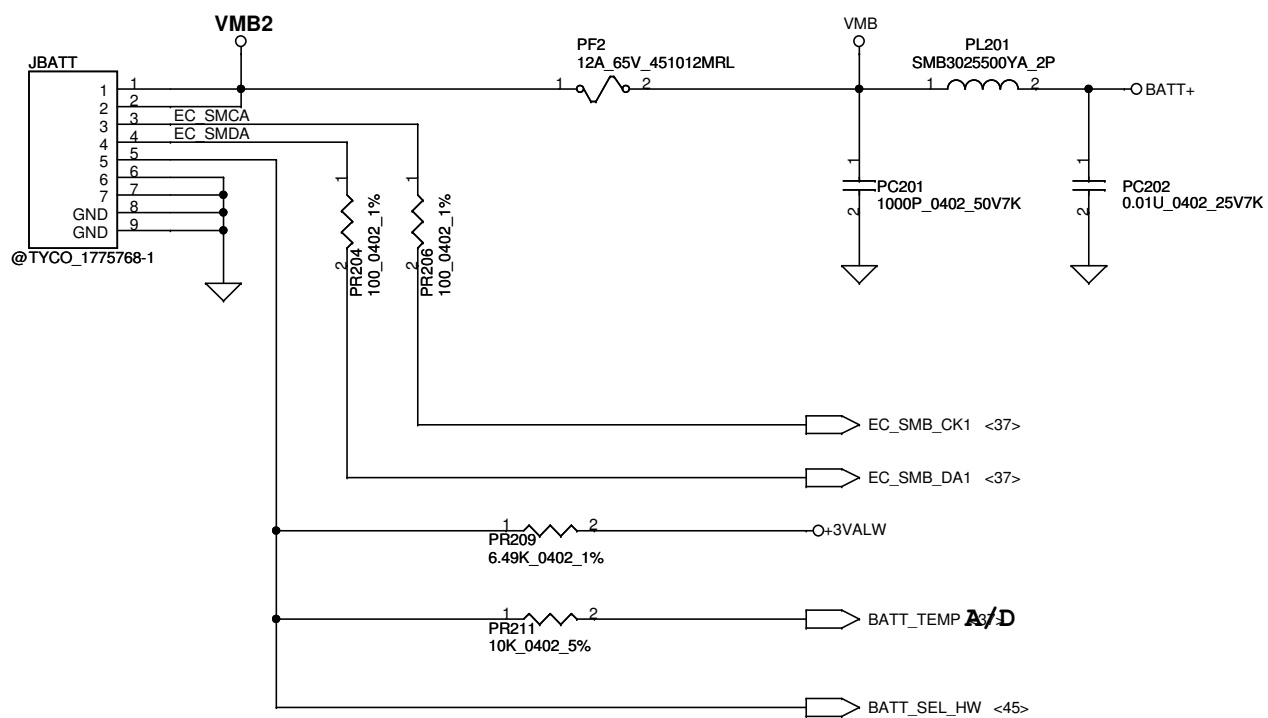
RTC Battery



SP093MX0000

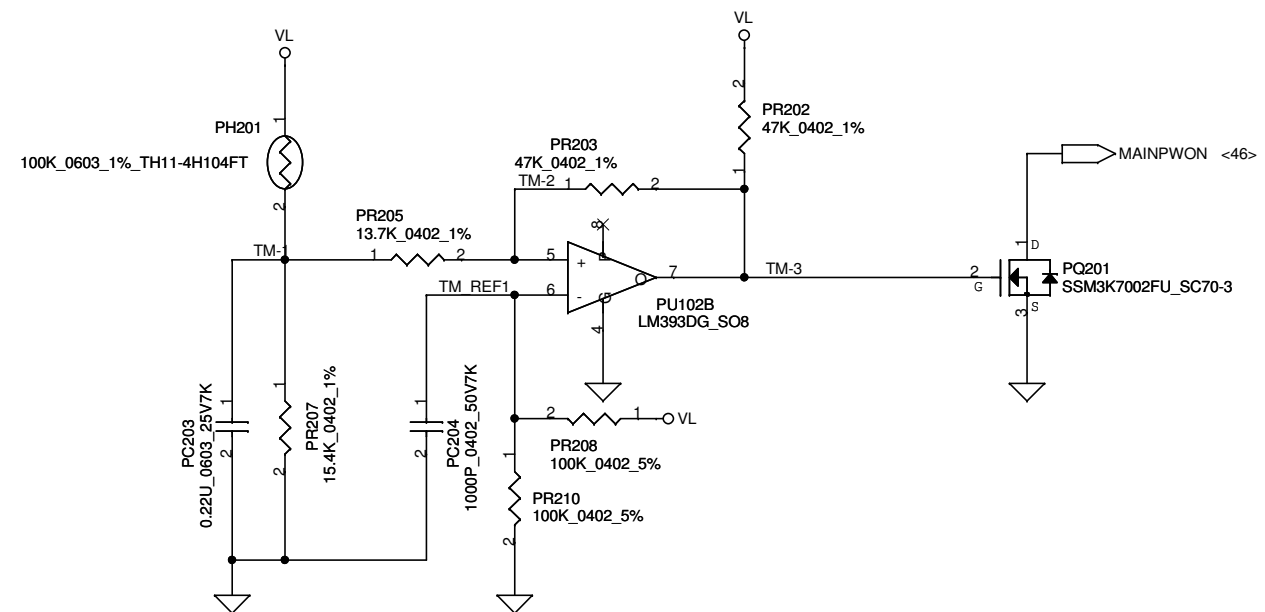


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Date: Tuesday, March 24, 2009			Sheet 43 of 52	Rev 0.1

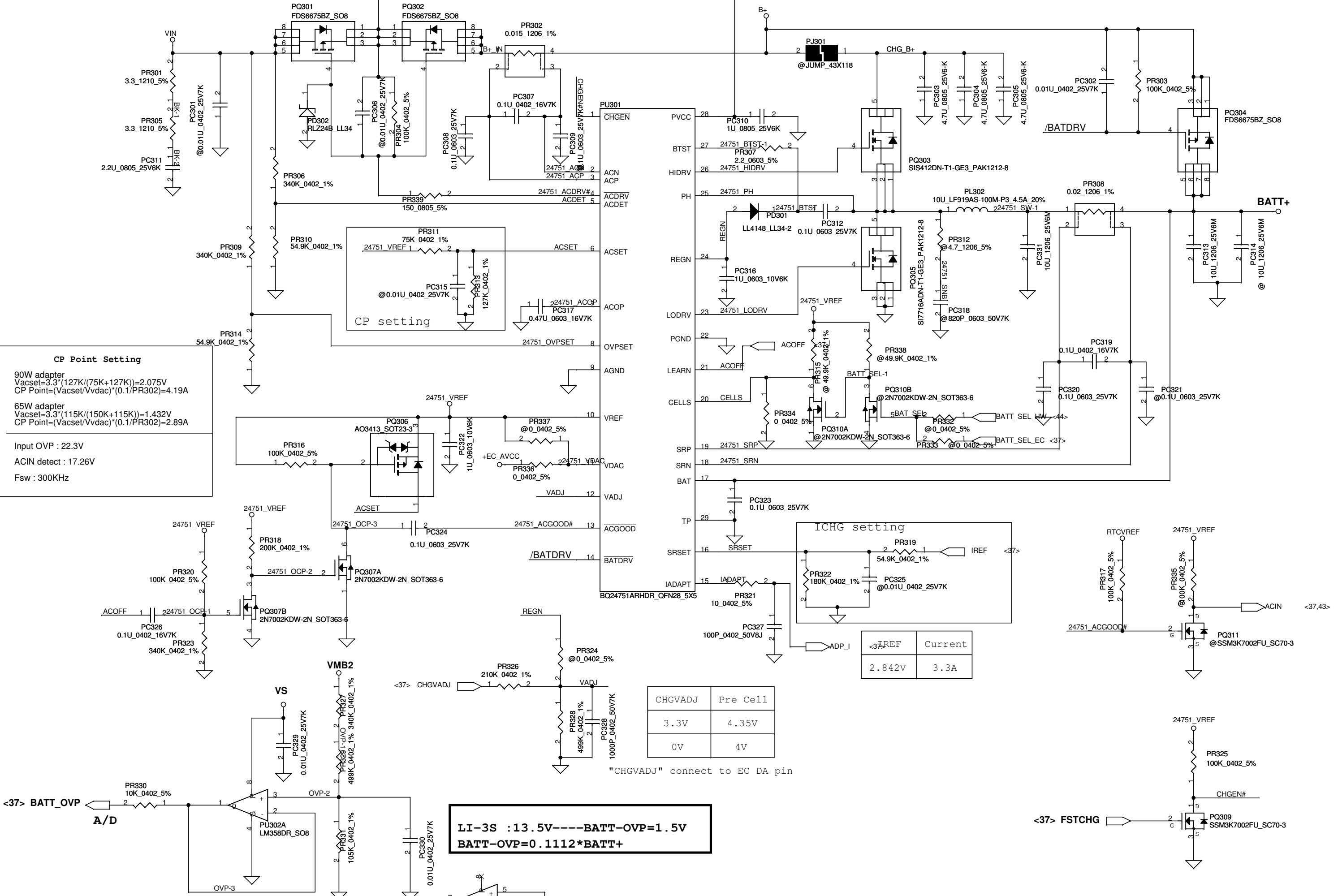


PH1 under CPU botten side :

CPU thermal protection at 92 degree C
Recovery at 56 degree C



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CP Point Setting

90W adapter
 $V_{acset} = 3.3 * (127K / (75K + 127K)) = 2.075V$
 $CP\ Point = (V_{acset} / V_{vdac}) * (0.1 / PR302) = 4.19A$

65W adapter
 $V_{acset} = 3.3 * (115K / (150K + 115K)) = 1.432V$
 $CP\ Point = (V_{acset} / V_{vdac}) * (0.1 / PR302) = 2.89A$

Input OVP : 22.3V
 ACIN detect : 17.26V
 Fsw : 300KHz

ICHG setting

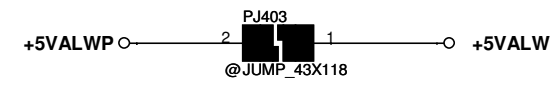
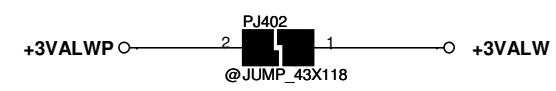
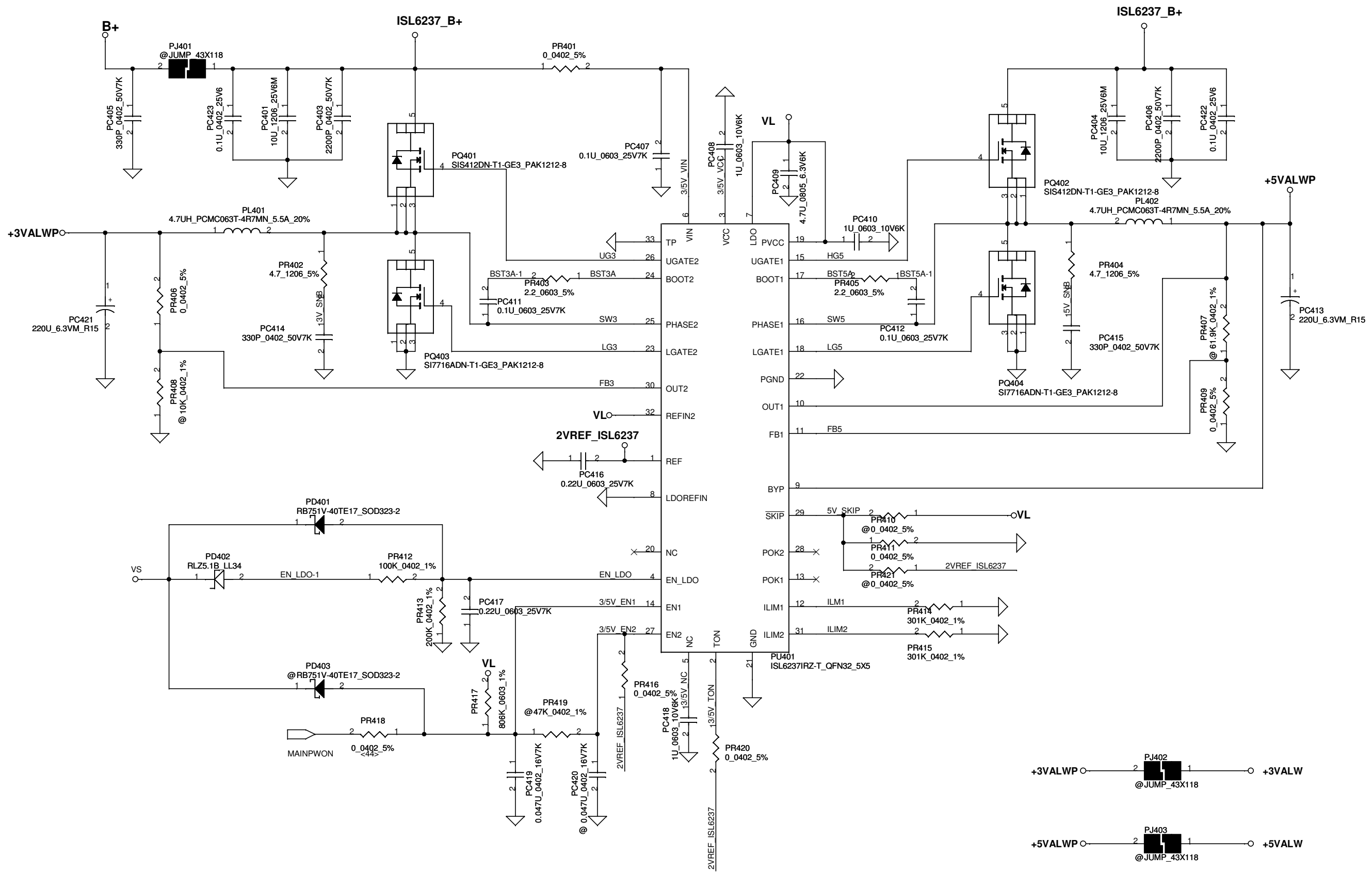
<37>REF	Current
2.842V	3.3A

CHGVADJ	Pre Cell
3.3V	4.35V
0V	4V

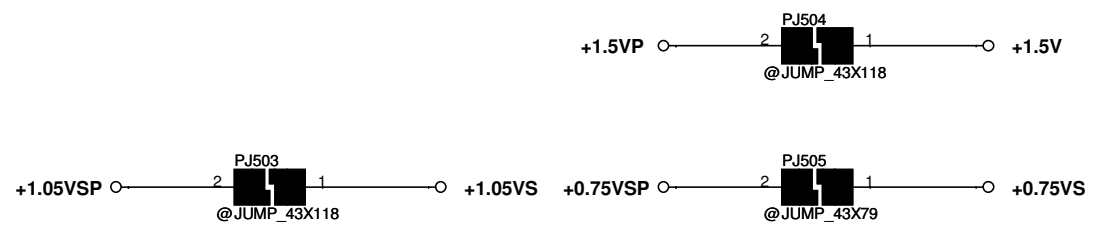
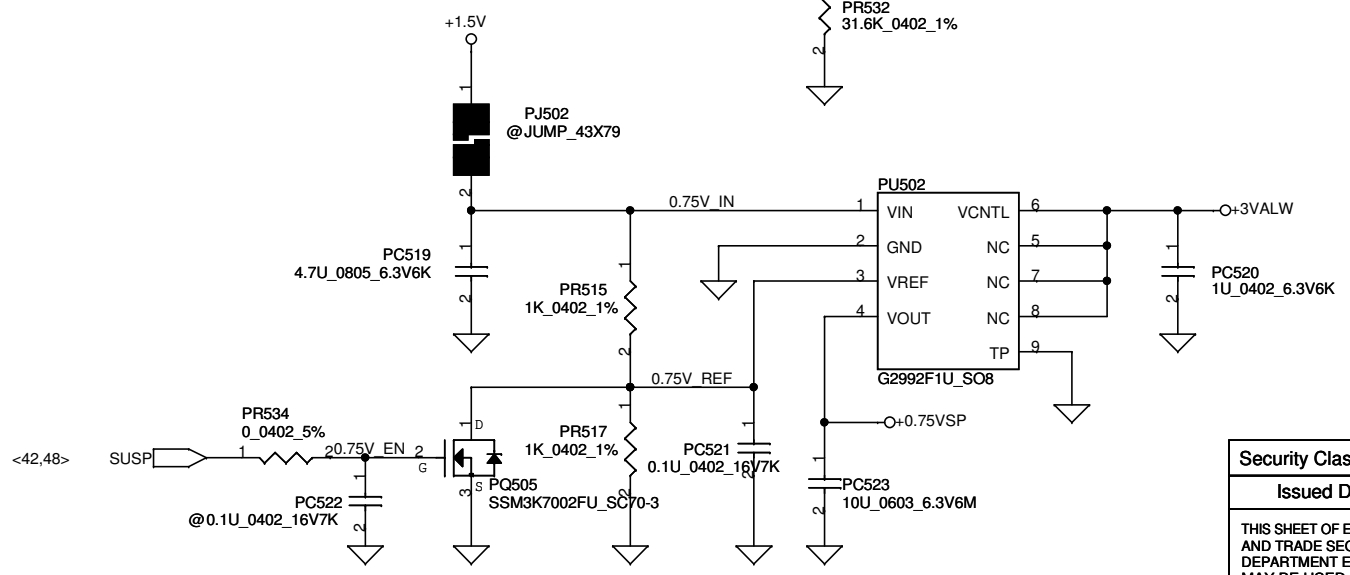
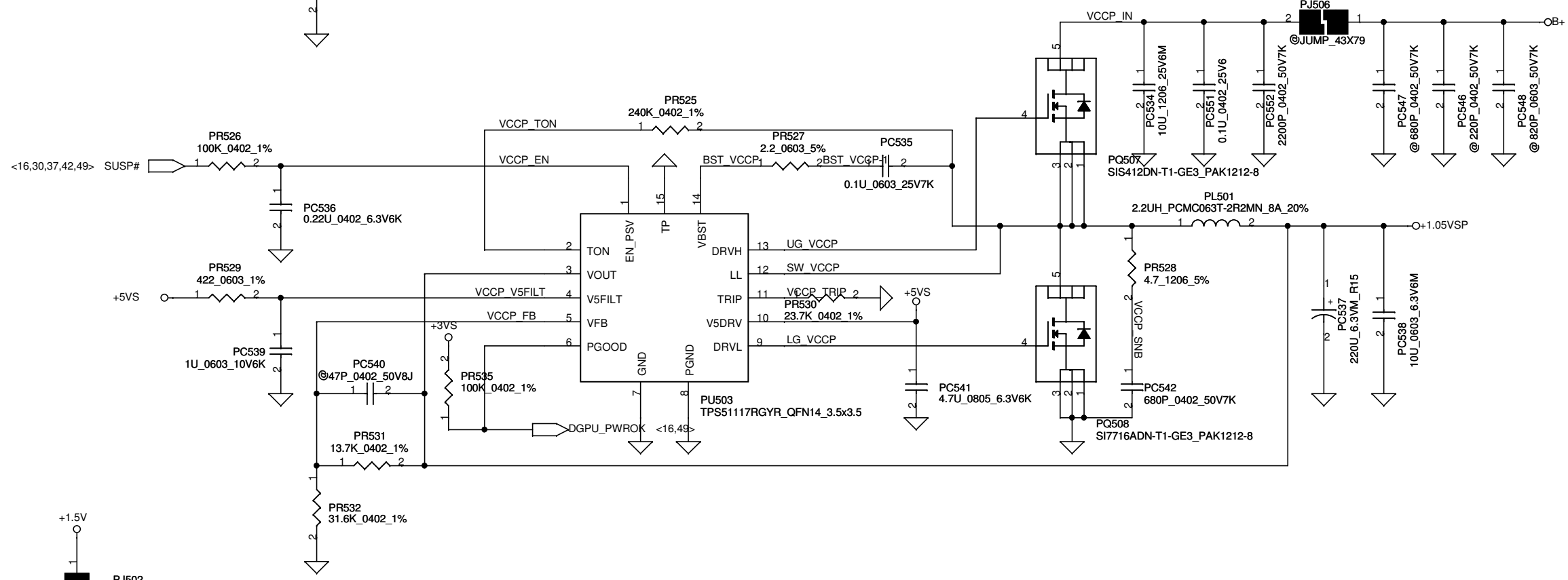
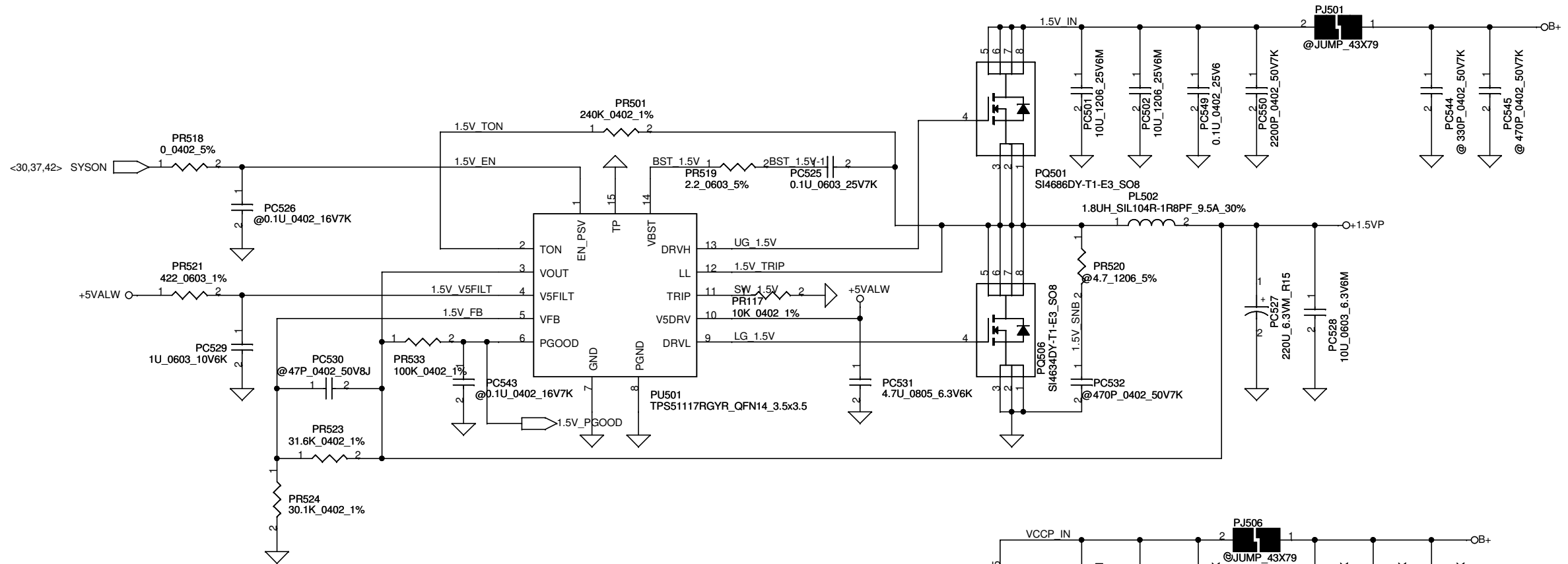
LI-3S : 13.5V ---- BATT-OVP = 1.5V
BATT-OVP = 0.1112 * BATT+

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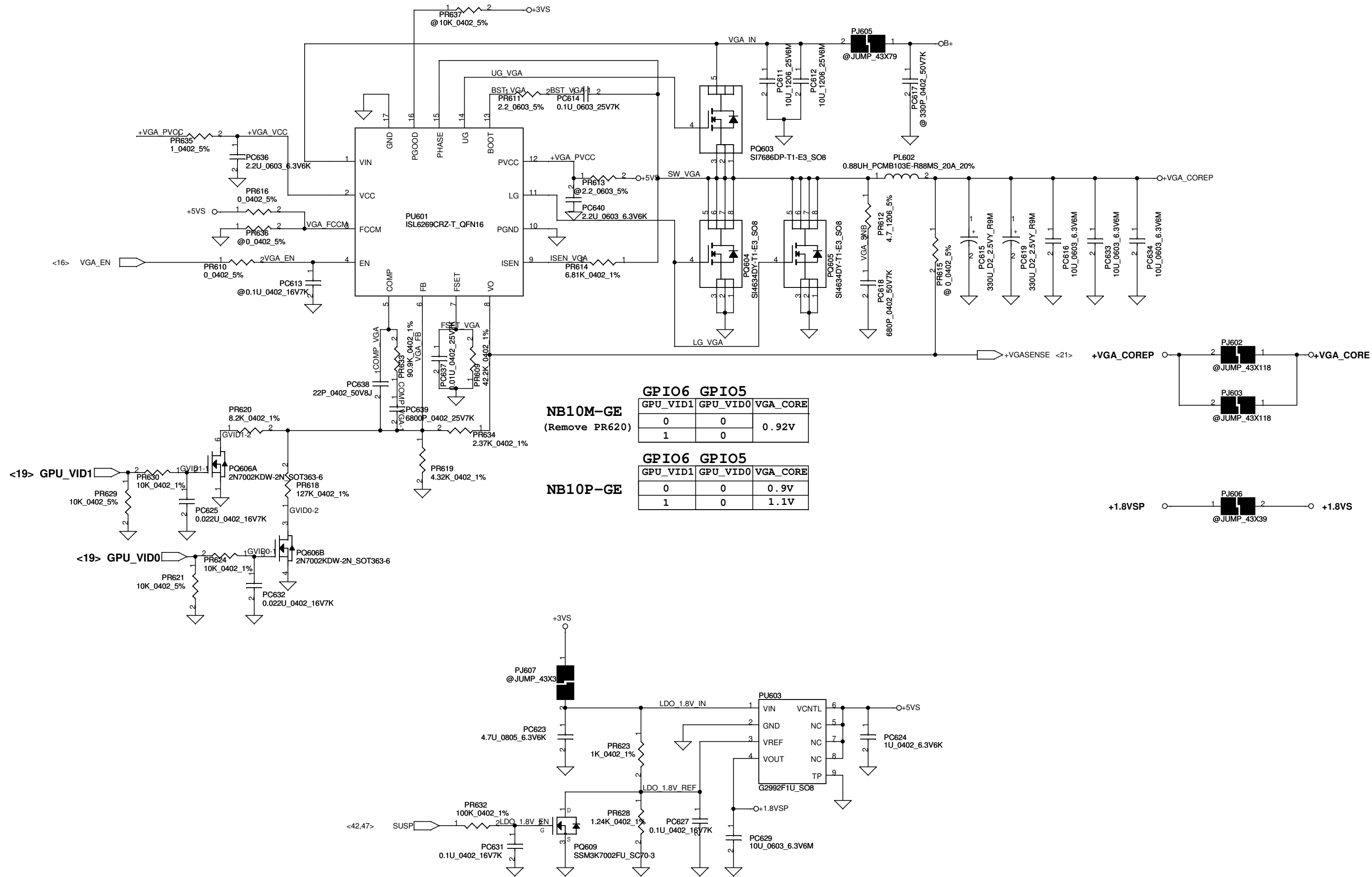
Compal Electronics, Inc.		
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CHARGER		
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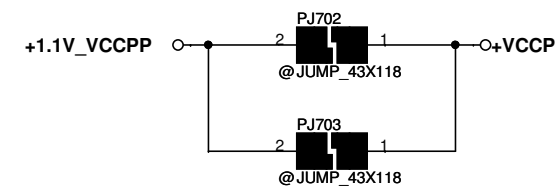
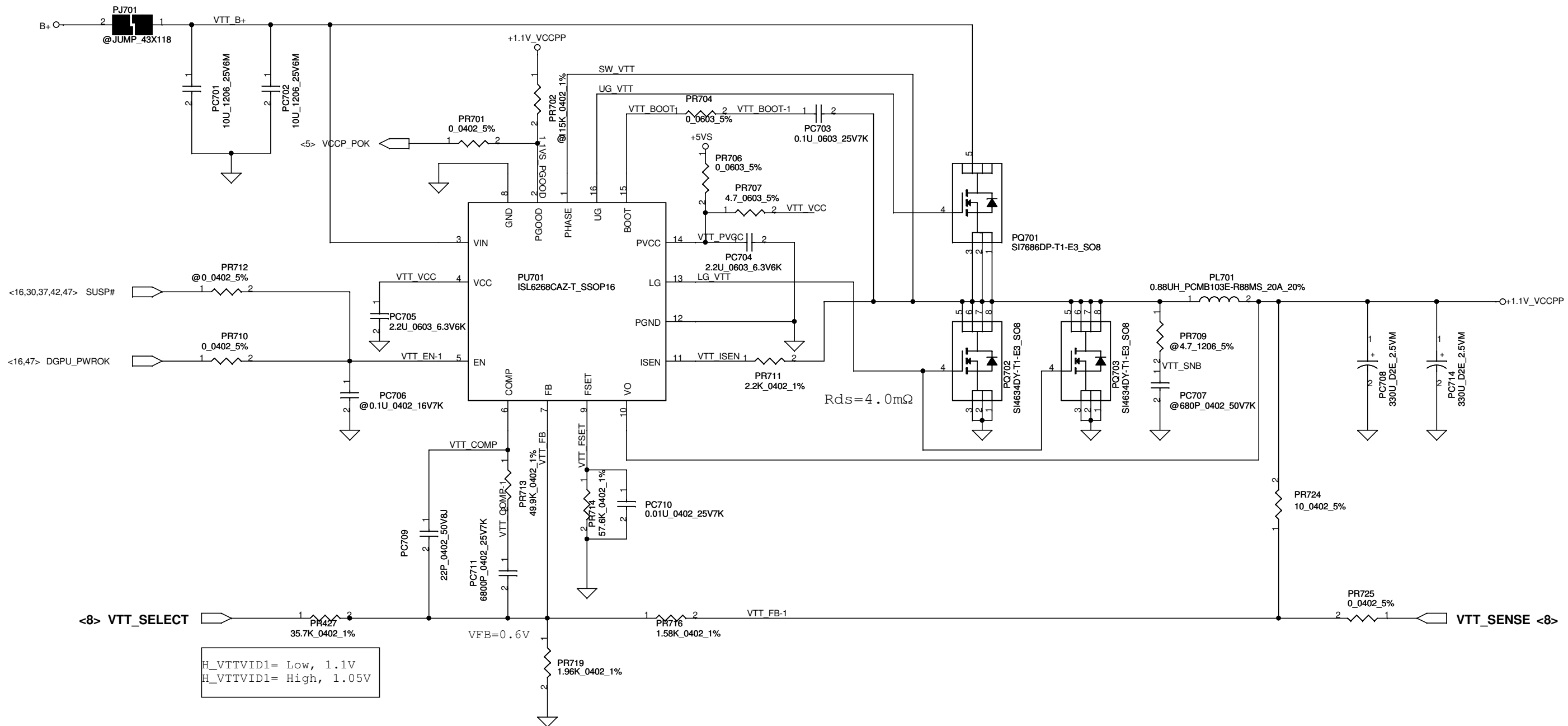
NB10M-GE
(Remove PR620)

GPIO6		GPIO5		VGA_CORE
GPU_VID1	GPU_VID0	GPU_VID1	GPU_VID0	VGA_CORE
0	0	0	0	0.92V
1	0	0	0	0.92V

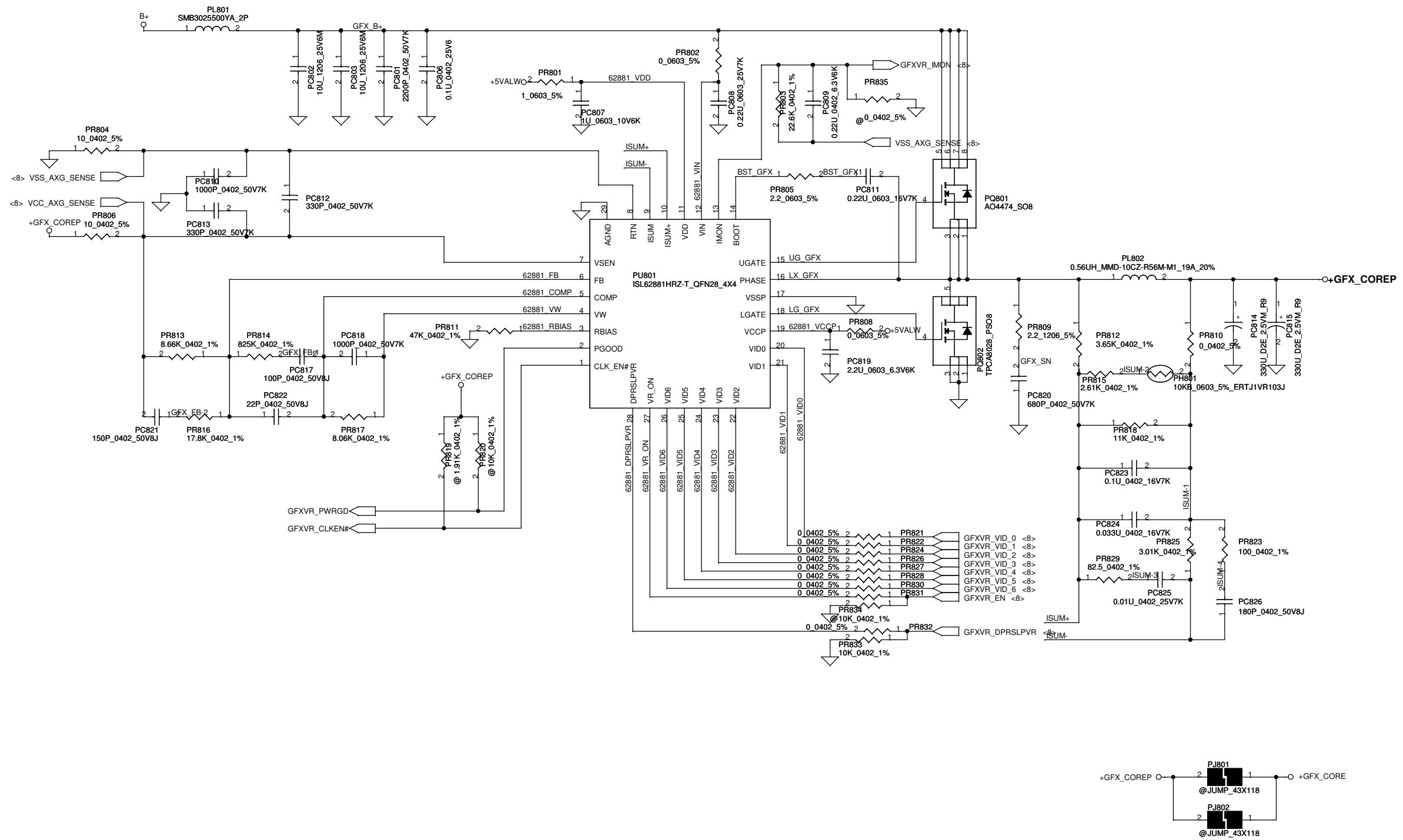
NB10P-GE

GPIO6		GPIO5		VGA_CORE
GPU_VID1	GPU_VID0	GPU_VID1	GPU_VID0	VGA_CORE
0	0	0	0	0.9V
1	0	0	0	1.1V

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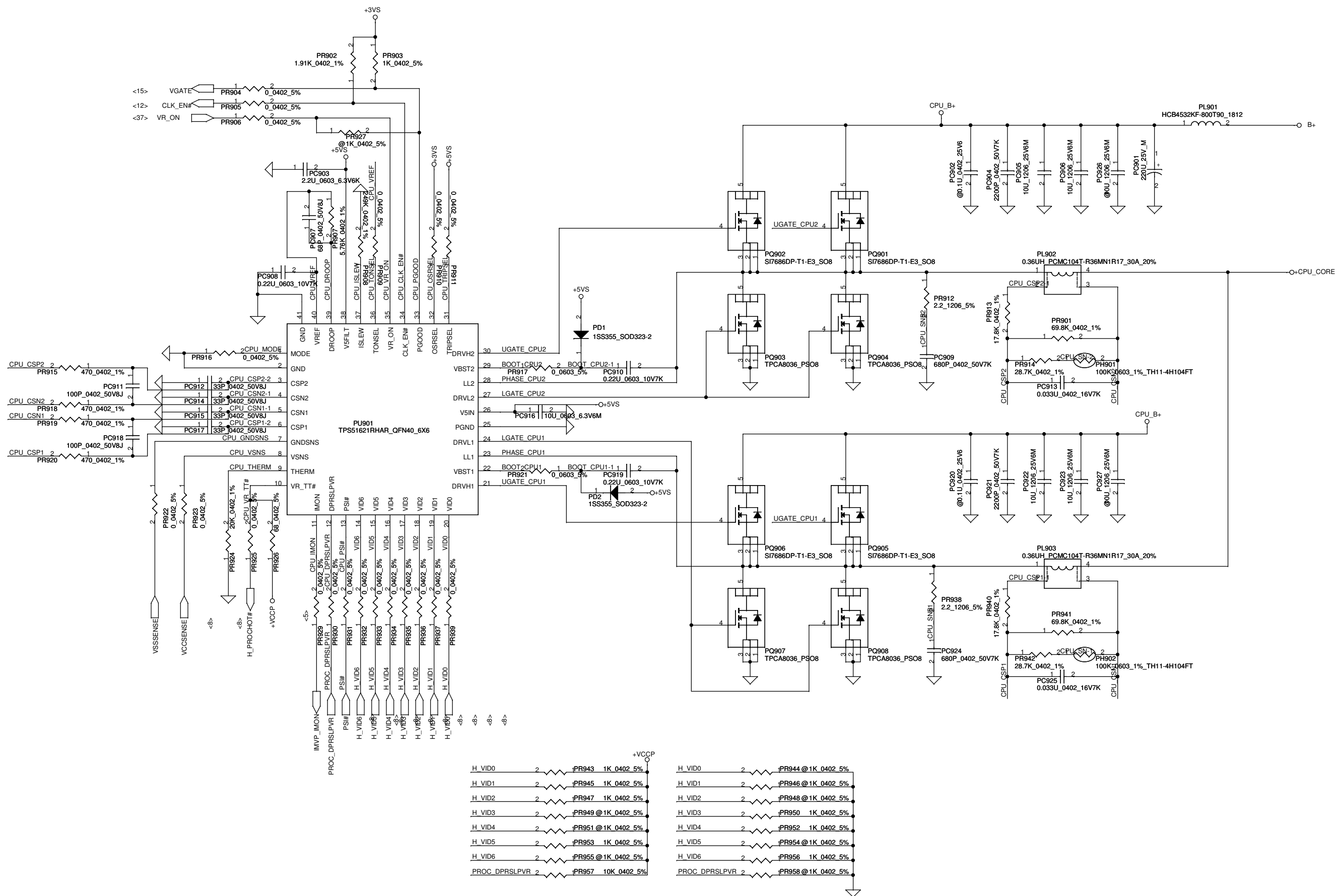


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(15A,600mils ,Via NO.= 30)

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