

MODEL NAME : *PAR00*

PCB NO : *LA-6601P (DAA00002000)*

BOM P/N : *TBD*

Compal Confidential

Voyager

Schematic Document

Rev: 1.0(A00)

2010-11-30

@ : Nopop Component

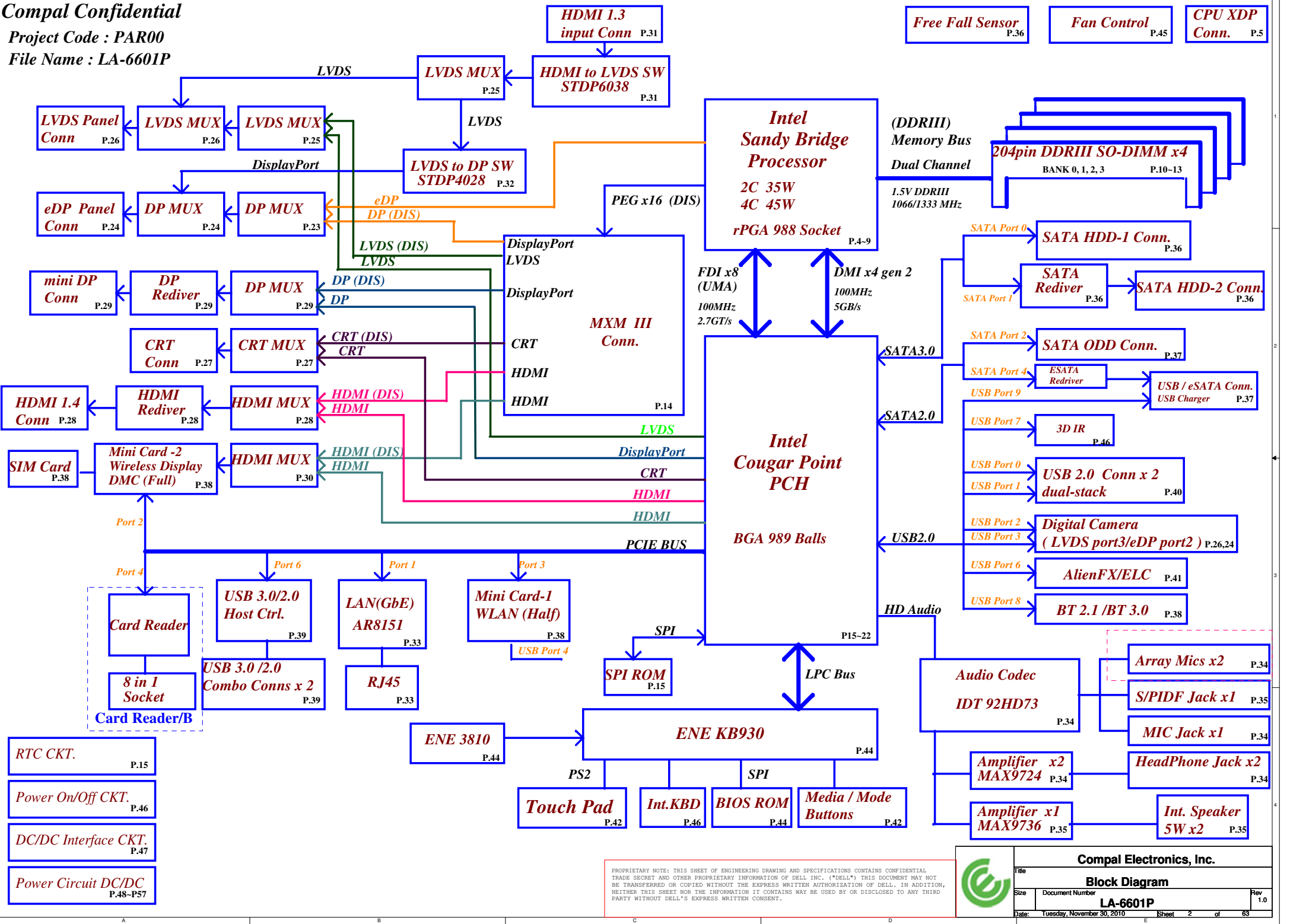
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| Title | | |
| Cover Sheet | | |
| Size | Document Number | Rev |
| | LA-6601P | 1.0 |
| Date: Tuesday, November 30, 2010 | | Sheet 1 of 85 |



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| | | | |
|---------------------------------|----------------------------|-------|---------|
| Compal Electronics, Inc. | | | |
| Block Diagram | | | |
| LA-6601P | | | |
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Board ID Table for AD channel

| Vcc | 3.3V +/- 5% | | | | |
|----------|-------------|-------------------------|-------------------------|-------------------------|-----------|
| Ra | 100K +/- 5% | | | | |
| Board ID | Rb | V _{AD_BID min} | V _{AD_BID typ} | V _{AD_BID max} | EC_AD3 |
| 0 | 0 | 0 V | 0 V | 0.155 V | 0x00-0x0C |
| 1 | 8.2K +/- 5% | 0.168 V | 0.250 V | 0.362 V | 0x0D-0x1C |
| 2 | 18K +/- 5% | 0.375 V | 0.503 V | 0.621 V | 0x1D-0x30 |
| 3 | 33K +/- 5% | 0.634 V | 0.819 V | 0.945 V | 0x31-0x49 |
| 4 | 56K +/- 5% | 0.958 V | 1.185 V | 1.359 V | 0x4A-0x69 |
| 5 | 100K +/- 5% | 1.372 V | 1.650 V | 1.838 V | 0x6A-0x8E |
| 6 | 200K +/- 5% | 1.851 V | 2.200 V | 2.420 V | 0x8F-0xBB |
| 7 | NC | 2.433 V | 3.300 V | 3.300 V | 0xBC-0xFF |

BOARD ID Table

| Board ID | PCB Revision |
|----------|--------------|
| 0 | 0.1 |
| 1 | 0.2 |
| 2 | 0.3 |
| 3 | 0.4 |
| 4 | 1.0 |
| 5 | |
| 6 | |
| 7 | |

SMBUS Control Table

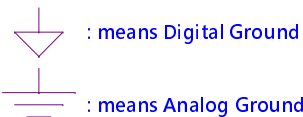
| | SOURCE | MIINI1 | BATT | MINI2 | EXPRESS CARD | SODIMM | MXM |
|---------------------------|--------|--------|------|-------|--------------|--------|-----|
| EC_SMB_CK1 EC_SMB_DA1 | KB930 | X | V | X | X | X | V |
| EC_SMB_CK2 EC_SMB_DA2 | KB930 | X | X | X | X | X | X |
| PCH_SMBCLK PCH_SMBDATA | PCH | V | X | V | V | X | X |
| MEM_SMBCLK MEM_SMBDATA | PCH | X | X | X | X | V | X |

| CLKOUT | DESTINATION |
|--------|--------------|
| PCI0 | PCH_LOOPBACK |
| PCI1 | EC |
| PCI2 | None |
| PCI3 | None |
| PCI4 | None |

| USB | USB PORT# | DESTINATION |
|-----|-----------|---------------|
| | 0 | JUSB1 |
| | 1 | JUSB2 |
| | 2 | eDP CAMERA |
| | 3 | LVDS CAMERA |
| | 4 | JMINI1 (WLAN) |
| | 5 | JMINI2 (DMC) |
| | 6 | AlienFX/ELC |
| | 7 | IR SENSOR |
| | 8 | Bluetooth |
| | 9 | JESATA |
| | 10 | None |
| | 11 | None |
| | 12 | None |
| 13 | None | |

| CLK | DIFFERENTIAL | DESTINATION | FLEX CLOCKS | DESTINATION |
|--------------|--------------|------------------|-------------|-------------|
| | CLKOUT_PCIE0 | None | CLKOUTFLEX0 | None |
| | CLKOUT_PCIE1 | 10/100/1G LAN | CLKOUTFLEX1 | CLK_14M |
| | CLKOUT_PCIE2 | MINI CARD-2 DMC | CLKOUTFLEX2 | None |
| | CLKOUT_PCIE3 | MINI CARD-1 WLAN | CLKOUTFLEX3 | None |
| | CLKOUT_PCIE4 | CARD READER | | |
| | CLKOUT_PCIE5 | None | | |
| | CLKOUT_PCIE6 | USB 3.0 | | |
| | CLKOUT_PCIE7 | None | | |
| CLKOUT_PEG_A | MXM | | | |

Symbol Note :



| SATA | DESTINATION |
|-------|-------------|
| SATA0 | HDD1 |
| SATA1 | HDD2 |
| SATA2 | ODD |
| SATA3 | NA |
| SATA4 | ESATA |
| SATA5 | None |

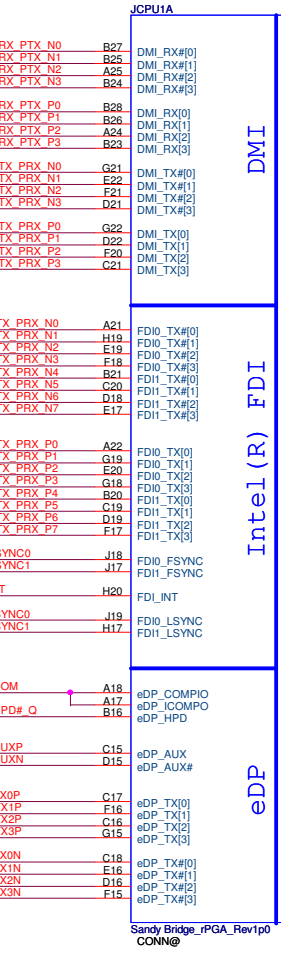
| PCI EXPRESS | DESTINATION |
|-------------|------------------|
| Lane 1 | 10/100/1G LAN |
| Lane 2 | MINI CARD-2 DMC |
| Lane 3 | MINI CARD-1 WLAN |
| Lane 4 | CARD READER |
| Lane 5 | None |
| Lane 6 | USB 3.0 |
| Lane 7 | None |
| Lane 8 | None |

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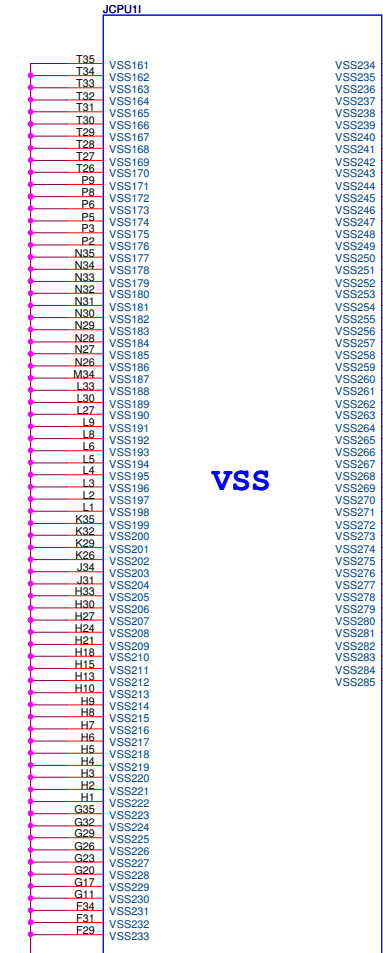
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| Notes List | | | |
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PEG_GTX_HRX_P0..15] 14
 PEG_GTX_HRX_N0..15] 14
 PEG_HTX_C_GRX_P0..15] 14
 PEG_HTX_C_GRX_N0..15] 14



PCI EXPRESS* - GRAPHICS

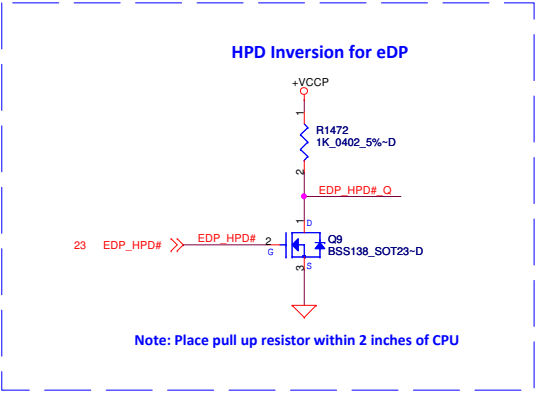
| | | | | | |
|-------------|-----|-------------------|------|---|---------------------------------------|
| PEG_ICOMPI | J22 | PEG_COMP | | | |
| PEG_ICOMPO | J21 | | | | |
| PEG_RCOPMO | H22 | | | | |
| PEG_RX#(0) | K33 | PEG GTX C HRX N0 | CC1 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX N0 |
| PEG_RX#(1) | M35 | PEG GTX C HRX N1 | CC2 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX N1 |
| PEG_RX#(2) | L34 | PEG GTX C HRX N2 | CC3 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX N2 |
| PEG_RX#(3) | J35 | PEG GTX C HRX N3 | CC3 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX N3 |
| PEG_RX#(4) | J32 | PEG GTX C HRX N4 | CC5 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX N4 |
| PEG_RX#(5) | H34 | PEG GTX C HRX N5 | CC13 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX N5 |
| PEG_RX#(6) | H31 | PEG GTX C HRX N6 | CC6 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX N6 |
| PEG_RX#(7) | G33 | PEG GTX C HRX N7 | CC7 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX N7 |
| PEG_RX#(8) | G30 | PEG GTX C HRX N8 | CC8 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX N8 |
| PEG_RX#(9) | F35 | PEG GTX C HRX N9 | CC9 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX N9 |
| PEG_RX#(10) | E34 | PEG GTX C HRX N10 | CC10 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX N10 |
| PEG_RX#(11) | D33 | PEG GTX C HRX N11 | CC12 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX N11 |
| PEG_RX#(12) | D31 | PEG GTX C HRX N12 | CC14 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX N12 |
| PEG_RX#(13) | B33 | PEG GTX C HRX N13 | CC15 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX N13 |
| PEG_RX#(14) | C32 | PEG GTX C HRX N14 | CC16 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX N14 |
| PEG_RX#(15) | C32 | PEG GTX C HRX N15 | CC16 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX N15 |
| PEG_RX#(0) | J33 | PEG GTX C HRX P0 | CC17 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX P0 |
| PEG_RX#(1) | L35 | PEG GTX C HRX P1 | CC18 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX P1 |
| PEG_RX#(2) | K34 | PEG GTX C HRX P2 | CC19 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX P2 |
| PEG_RX#(3) | H35 | PEG GTX C HRX P3 | CC20 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX P3 |
| PEG_RX#(4) | H32 | PEG GTX C HRX P4 | CC21 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX P4 |
| PEG_RX#(5) | G34 | PEG GTX C HRX P5 | CC22 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX P5 |
| PEG_RX#(6) | G31 | PEG GTX C HRX P6 | CC23 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX P6 |
| PEG_RX#(7) | F33 | PEG GTX C HRX P7 | CC24 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX P7 |
| PEG_RX#(8) | F30 | PEG GTX C HRX P8 | CC25 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX P8 |
| PEG_RX#(9) | E35 | PEG GTX C HRX P9 | CC26 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX P9 |
| PEG_RX#(10) | E33 | PEG GTX C HRX P10 | CC27 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX P10 |
| PEG_RX#(11) | D32 | PEG GTX C HRX P11 | CC28 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX P11 |
| PEG_RX#(12) | D34 | PEG GTX C HRX P12 | CC29 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX P12 |
| PEG_RX#(13) | E31 | PEG GTX C HRX P13 | CC30 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX P13 |
| PEG_RX#(14) | C33 | PEG GTX C HRX P14 | CC31 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX P14 |
| PEG_RX#(15) | B32 | PEG GTX C HRX P15 | CC32 | 1 | 2 022U 0402 16V7K-D PEG GTX HRX P15 |
| PEG_TX#(0) | M29 | PEG HTX GRX N0 | CC33 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX N0 |
| PEG_TX#(1) | M32 | PEG HTX GRX N1 | CC34 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX N1 |
| PEG_TX#(2) | L31 | PEG HTX GRX N2 | CC35 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX N2 |
| PEG_TX#(3) | K32 | PEG HTX GRX N3 | CC36 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX N3 |
| PEG_TX#(4) | L29 | PEG HTX GRX N4 | CC37 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX N4 |
| PEG_TX#(5) | K31 | PEG HTX GRX N5 | CC38 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX N5 |
| PEG_TX#(6) | K28 | PEG HTX GRX N6 | CC39 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX N6 |
| PEG_TX#(7) | J30 | PEG HTX GRX N7 | CC40 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX N7 |
| PEG_TX#(8) | J28 | PEG HTX GRX N8 | CC41 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX N8 |
| PEG_TX#(9) | H29 | PEG HTX GRX N9 | CC42 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX N9 |
| PEG_TX#(10) | G27 | PEG HTX GRX N10 | CC43 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX N10 |
| PEG_TX#(11) | E29 | PEG HTX GRX N11 | CC44 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX N11 |
| PEG_TX#(12) | F27 | PEG HTX GRX N12 | CC45 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX N12 |
| PEG_TX#(13) | D28 | PEG HTX GRX N13 | CC46 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX N13 |
| PEG_TX#(14) | F26 | PEG HTX GRX N14 | CC47 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX N14 |
| PEG_TX#(15) | E25 | PEG HTX GRX N15 | CC48 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX N15 |
| PEG_TX#(0) | M28 | PEG HTX GRX P0 | CC49 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX P0 |
| PEG_TX#(1) | M33 | PEG HTX GRX P1 | CC50 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX P1 |
| PEG_TX#(2) | L30 | PEG HTX GRX P2 | CC51 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX P2 |
| PEG_TX#(3) | L28 | PEG HTX GRX P3 | CC52 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX P3 |
| PEG_TX#(4) | L28 | PEG HTX GRX P4 | CC53 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX P4 |
| PEG_TX#(5) | K30 | PEG HTX GRX P5 | CC54 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX P5 |
| PEG_TX#(6) | K27 | PEG HTX GRX P6 | CC55 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX P6 |
| PEG_TX#(7) | J29 | PEG HTX GRX P7 | CC56 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX P7 |
| PEG_TX#(8) | J27 | PEG HTX GRX P8 | CC57 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX P8 |
| PEG_TX#(9) | H28 | PEG HTX GRX P9 | CC58 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX P9 |
| PEG_TX#(10) | G28 | PEG HTX GRX P10 | CC59 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX P10 |
| PEG_TX#(11) | E28 | PEG HTX GRX P11 | CC60 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX P11 |
| PEG_TX#(12) | F28 | PEG HTX GRX P12 | CC61 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX P12 |
| PEG_TX#(13) | D27 | PEG HTX GRX P13 | CC62 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX P13 |
| PEG_TX#(14) | E26 | PEG HTX GRX P14 | CC63 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX P14 |
| PEG_TX#(15) | D25 | PEG HTX GRX P15 | CC64 | 1 | 2 022U 0402 16V7K-D PEG HTX C GRX P15 |



Near MXM Connector

Sandy Bridge_rPGA_Rev1p0
CONN@

Sandy Bridge_rPGA_Rev1p0
CONN@



PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

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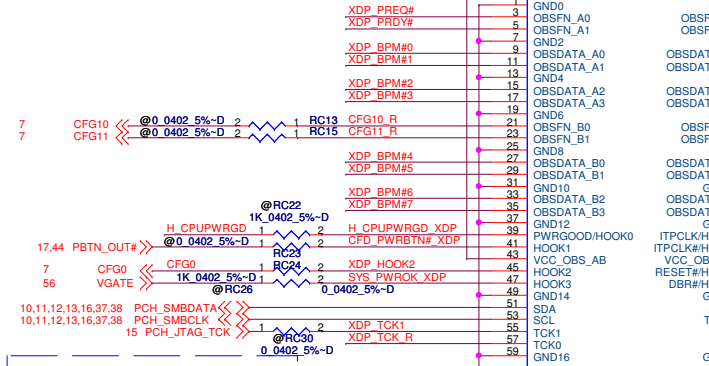
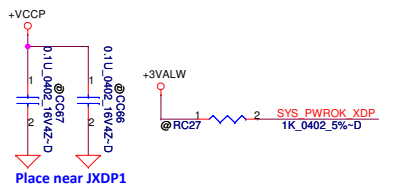
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PROCESSOR(1/6) DMI,FDI,PEG

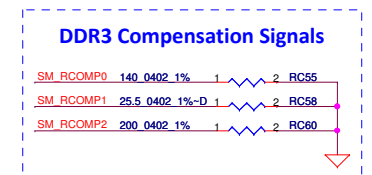
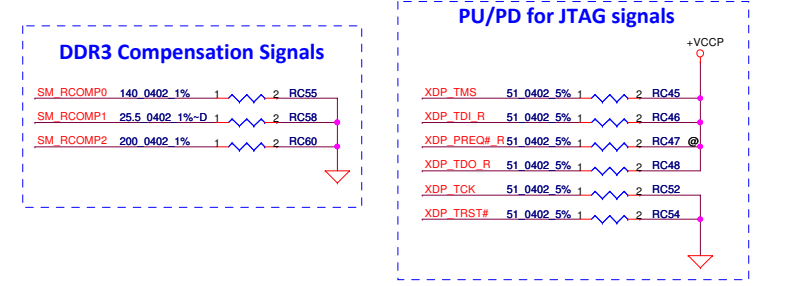
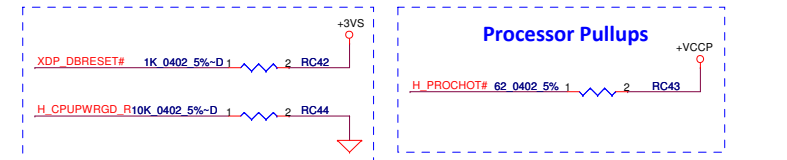
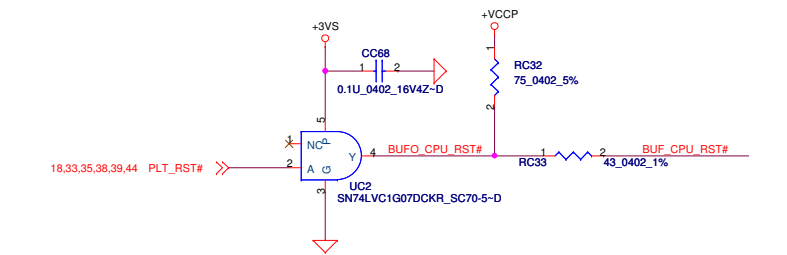
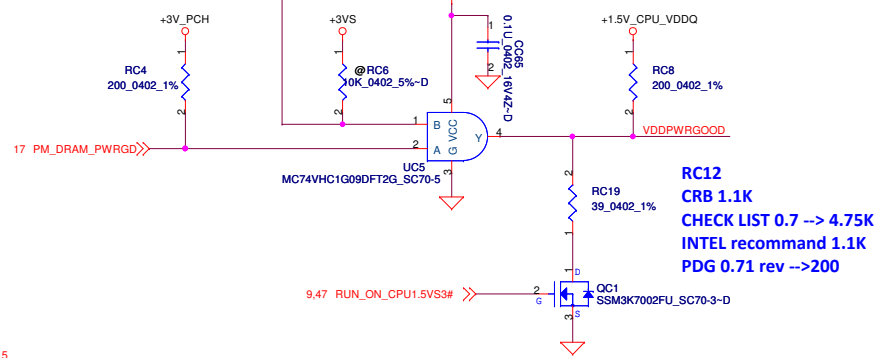
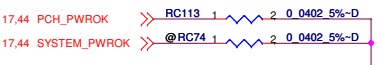
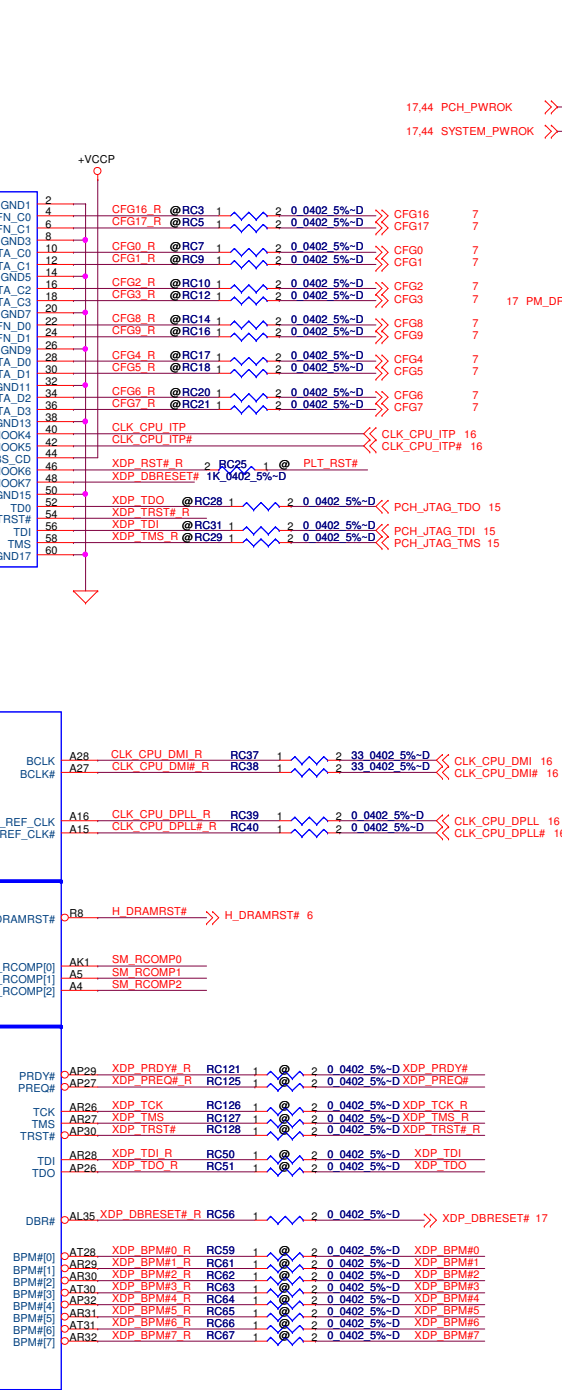
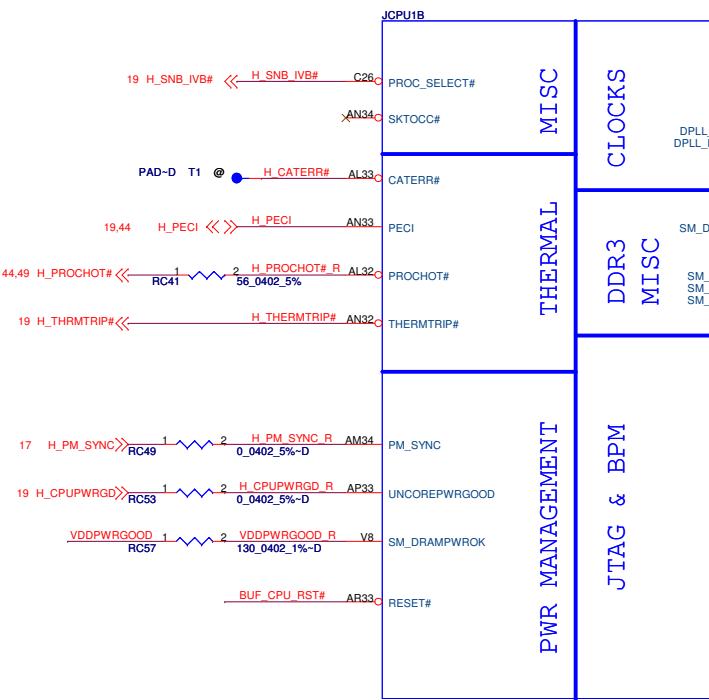
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The resistor for HOOK2 should be placed such that the stub is very small on CFG0 net



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File: **PROCESSOR(2/6) PM,XDP,CLK**

Size: Document Number

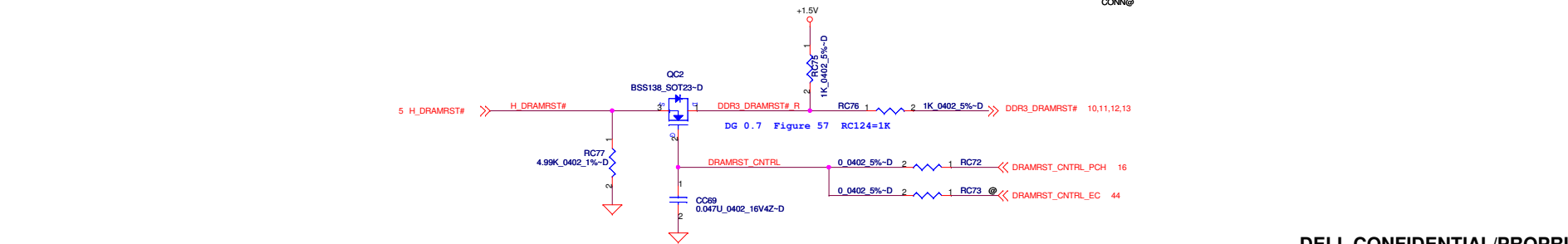
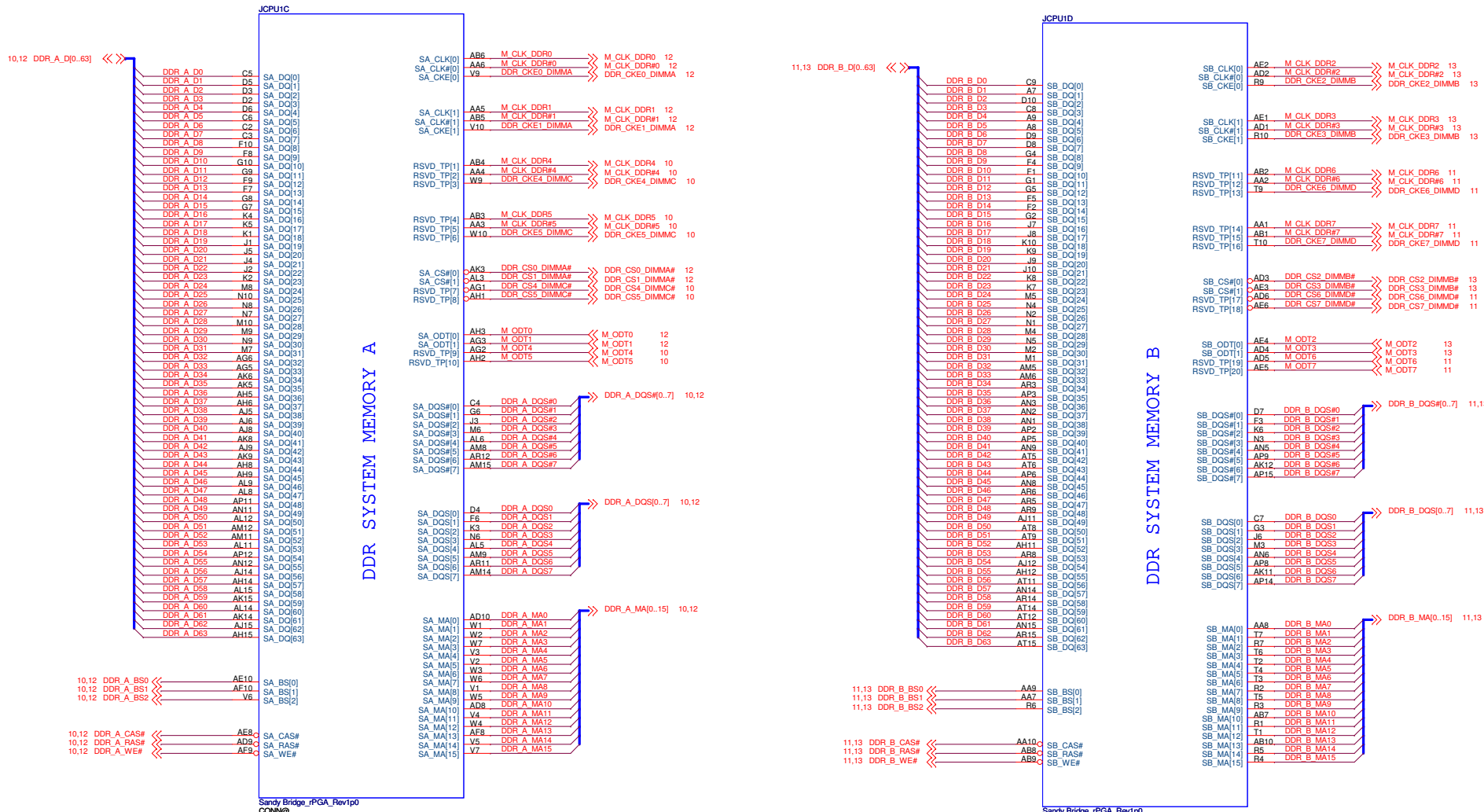
LA-6601P

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Rev 1.0

Need to confired
when Intel spec release.



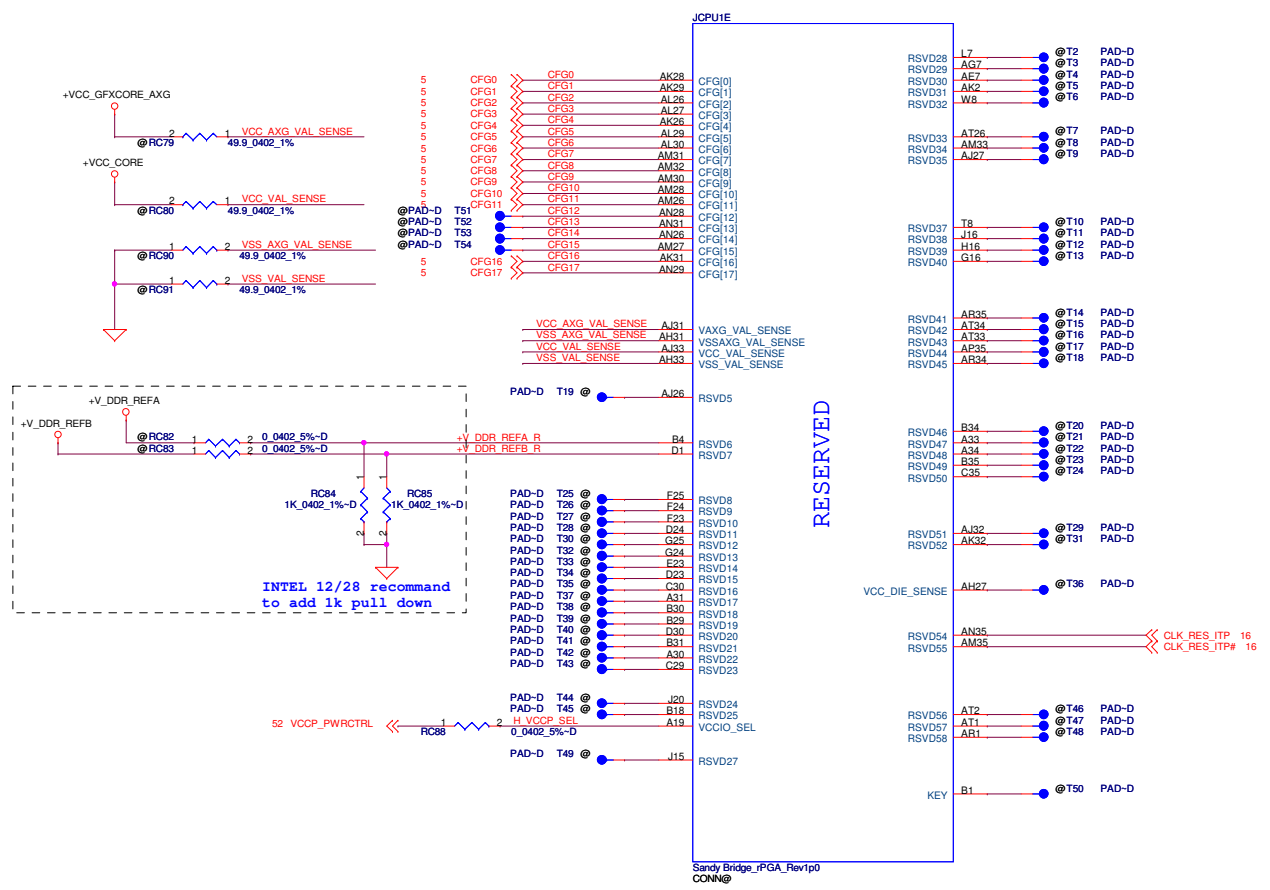
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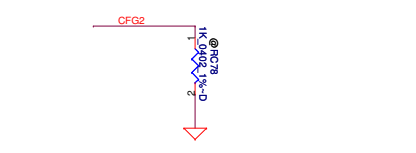
PROCESSOR(3/6) DDRIII

| | | | | |
|-------|----------------------------|----------|-------|---------|
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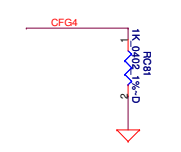
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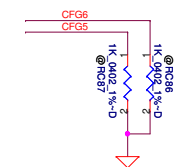
CFG Straps for Processor



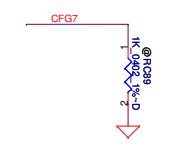
| PEG Static Lane Reversal - CFG2 is for the 16x | |
|--|--|
| CFG2 | 1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed |



| Display Port Presence Strap | |
|-----------------------------|--|
| CFG4 | 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port |



| PCIe Port Bifurcation Straps | |
|------------------------------|--|
| CFG[6:5] | 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled |



| PEG DEFER TRAINING | |
|--------------------|---|
| CFG7 | 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training |

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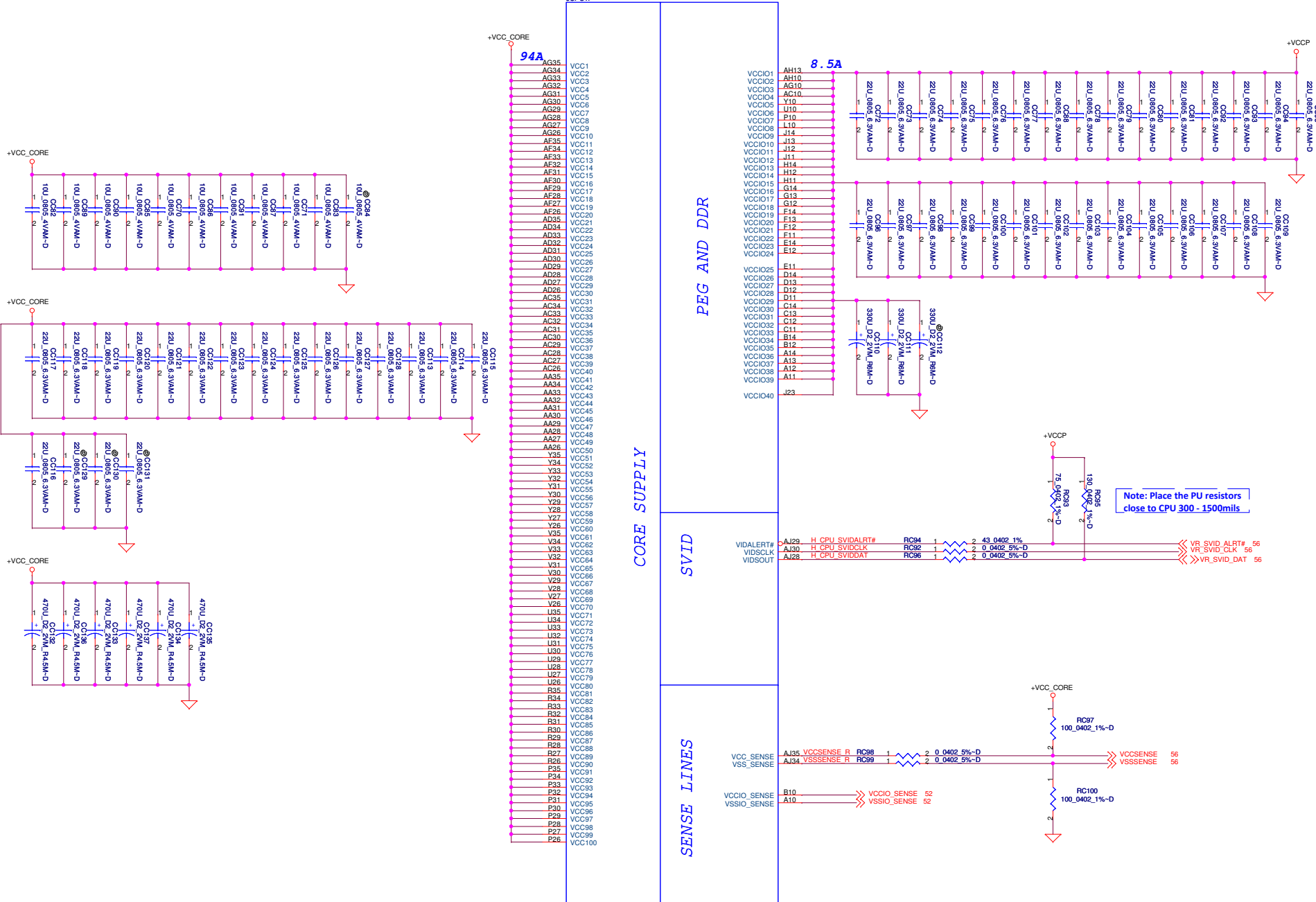
Compal Electronics, Inc.

PROCESSOR(4/6) RSV0,CFG

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| File | LA-6601P | | Rev | 1.0 |
| Size | Document Number | LA-6601P | | |
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POWER



Sandy Bridge_rPGA_Rev1p0
CONN@

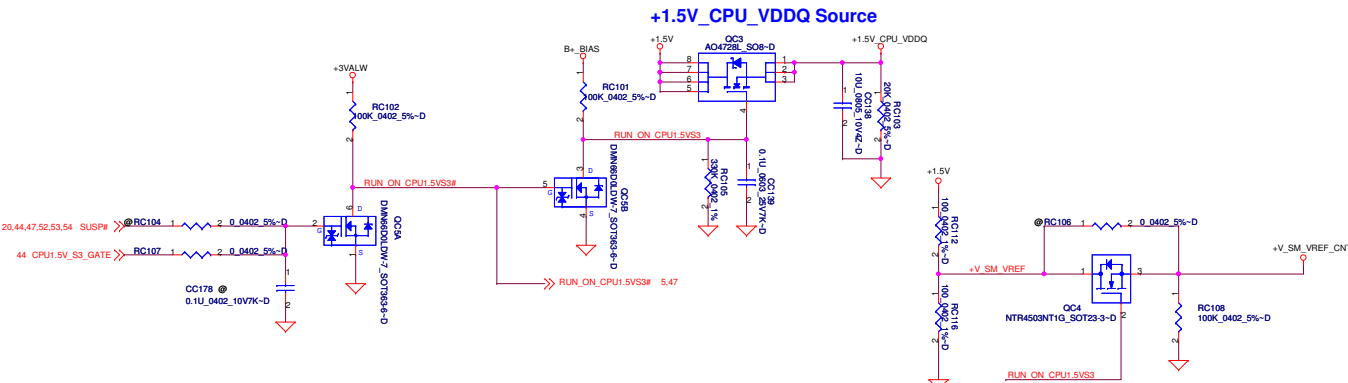
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

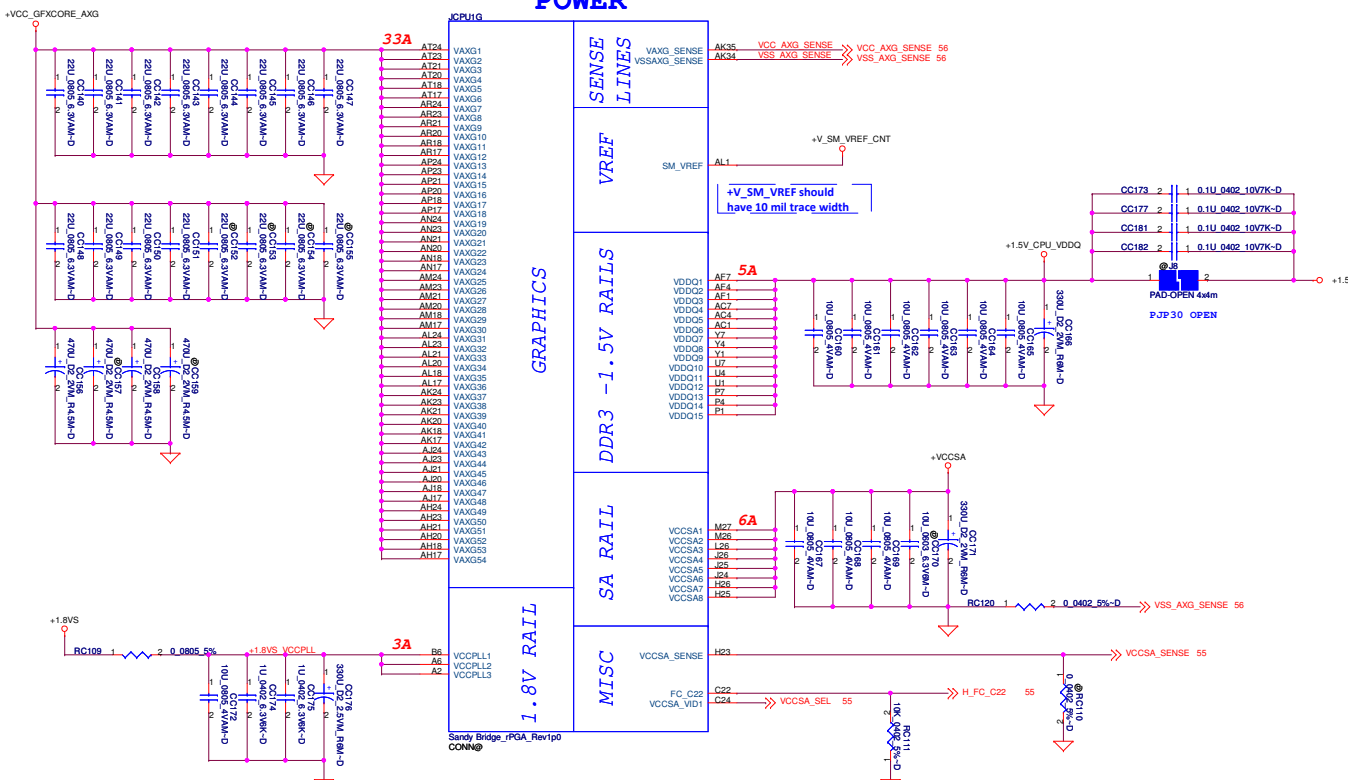
PROCESSOR(5/6) PWR,BYPASS

| | | | |
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| File | LA-6601P | Rev | 1.0 |
| Size | Document Number | Sheet | 8 of 83 |
| Date: | Tuesday, November 30, 2010 | | |

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POWER



JCPU1H

| | | |
|------|-------|------|
| AT35 | VSS1 | AJ22 |
| AT32 | VSS2 | AJ19 |
| AT29 | VSS3 | AH6 |
| AT27 | VSS4 | AJ13 |
| AT25 | VSS4 | AJ10 |
| AT22 | VSS5 | AJ7 |
| VSS6 | VSS6 | AJ4 |
| AT19 | VSS7 | AJ1 |
| AT16 | VSS8 | AJ2 |
| AT13 | VSS9 | AJ1 |
| AT10 | VSS10 | AJ5 |
| AT7 | VSS11 | AH5 |
| AT4 | VSS12 | AH2 |
| AT3 | VSS13 | AH30 |
| AR23 | VSS14 | AH29 |
| AR19 | VSS15 | AH28 |
| AR13 | VSS16 | AH26 |
| AR16 | VSS17 | AH25 |
| AR13 | VSS18 | AH22 |
| AR17 | VSS19 | AH22 |
| AR10 | VSS20 | AH19 |
| AR4 | VSS21 | AH10 |
| AR2 | VSS22 | AH7 |
| AP4 | VSS23 | AH4 |
| AP31 | VSS24 | AG9 |
| AP28 | VSS25 | AG8 |
| AP25 | VSS26 | AG4 |
| AP22 | VSS27 | AF6 |
| AP18 | VSS28 | AF3 |
| AP13 | VSS29 | AF2 |
| AP10 | VSS30 | AF2 |
| AP7 | VSS31 | AE34 |
| AP4 | VSS32 | AE33 |
| AP1 | VSS33 | AE32 |
| AN30 | VSS34 | AE31 |
| AN27 | VSS35 | AE30 |
| AN25 | VSS36 | AE29 |
| AN22 | VSS37 | AE29 |
| AN19 | VSS38 | AE27 |
| AN16 | VSS39 | AE26 |
| AN13 | VSS40 | AE9 |
| AN10 | VSS41 | AD7 |
| AN7 | VSS42 | AC9 |
| AM4 | VSS43 | AC8 |
| AM29 | VSS44 | AC6 |
| AM25 | VSS45 | AC5 |
| AM22 | VSS46 | AC3 |
| AM15 | VSS47 | AC2 |
| AM16 | VSS48 | AB35 |
| AM13 | VSS49 | AB34 |
| AM10 | VSS50 | AB33 |
| AM7 | VSS51 | AB32 |
| AM4 | VSS52 | AB31 |
| AM3 | VSS53 | AB30 |
| AM2 | VSS54 | AB29 |
| AM1 | VSS55 | AB29 |
| AL34 | VSS56 | AB27 |
| AL31 | VSS57 | AB26 |
| AL28 | VSS58 | AB26 |
| AL25 | VSS59 | Y8 |
| AL22 | VSS60 | Y8 |
| AL19 | VSS61 | Y5 |
| AL16 | VSS62 | Y3 |
| AL13 | VSS63 | Y2 |
| AL10 | VSS64 | Y2 |
| AL7 | VSS65 | W35 |
| AL4 | VSS66 | W34 |
| AL1 | VSS67 | W33 |
| AK2 | VSS68 | W32 |
| AK3 | VSS69 | W31 |
| AK0 | VSS70 | W30 |
| AK25 | VSS71 | W29 |
| AK22 | VSS72 | W28 |
| AK19 | VSS73 | W27 |
| AK16 | VSS74 | W26 |
| AK13 | VSS75 | W25 |
| AK10 | VSS76 | W25 |
| AK7 | VSS77 | W25 |
| AK4 | VSS78 | W25 |
| AJ25 | VSS79 | W25 |
| | VSS80 | W25 |

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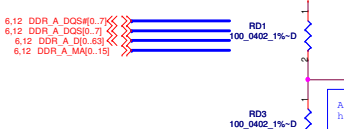
Compal Electronics, Inc.

PROCESSOR(6/6) PWR,VSS

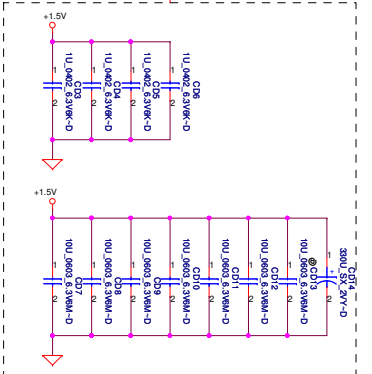
Document Number: **LA-6601P**

Date: Tuesday, November 31 2010 Sheet 9 of 83

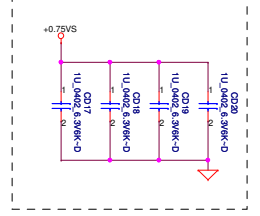
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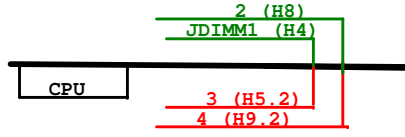
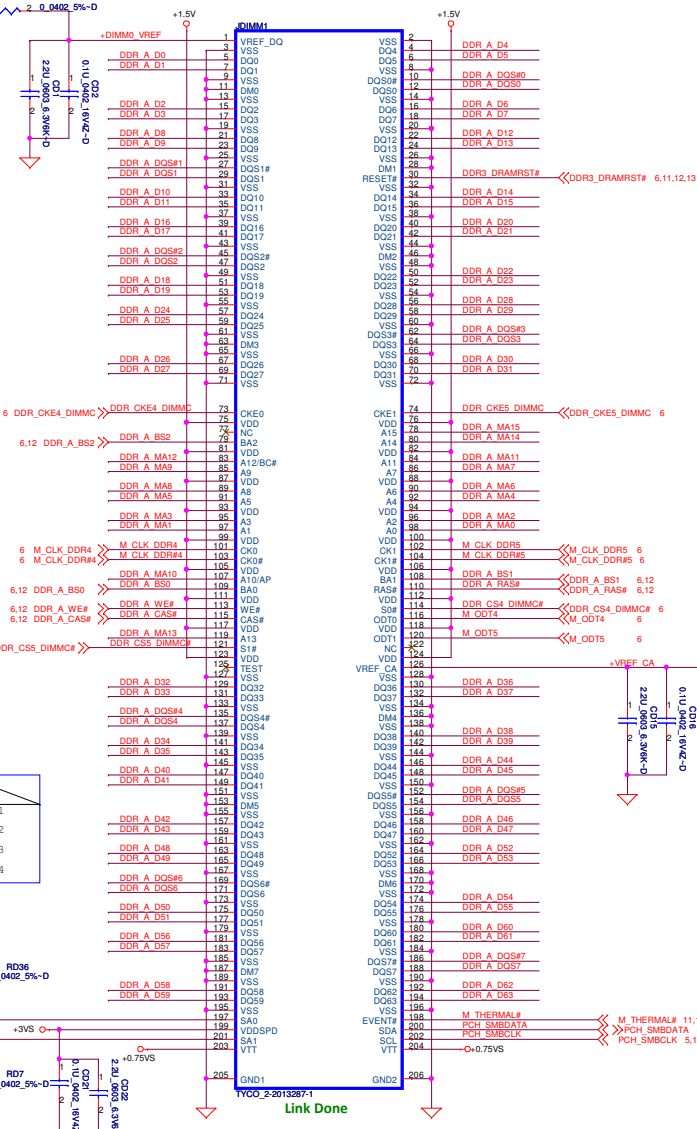
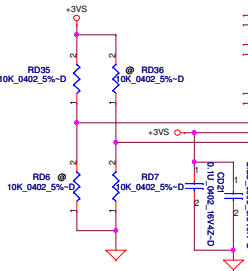
Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203,204



| SA0 | SA1 | |
|-----|-----|-------|
| 1 | 0 | DIMM1 |
| 1 | 1 | DIMM2 |
| 0 | 0 | DIMM3 |
| 0 | 1 | DIMM4 |



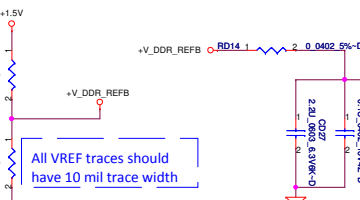
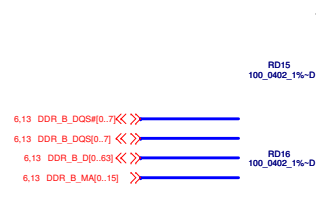
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Compal Electronics, Inc.

| | | |
|-------|----------------------------|----------------|
| File | DDRIII DIMMA | |
| Size | Document Number | Rev |
| | LA-6601P | 1.0 |
| Date: | Tuesday, November 30, 2010 | Sheet 10 of 63 |

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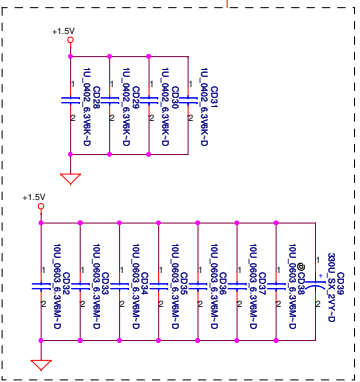




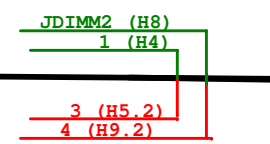
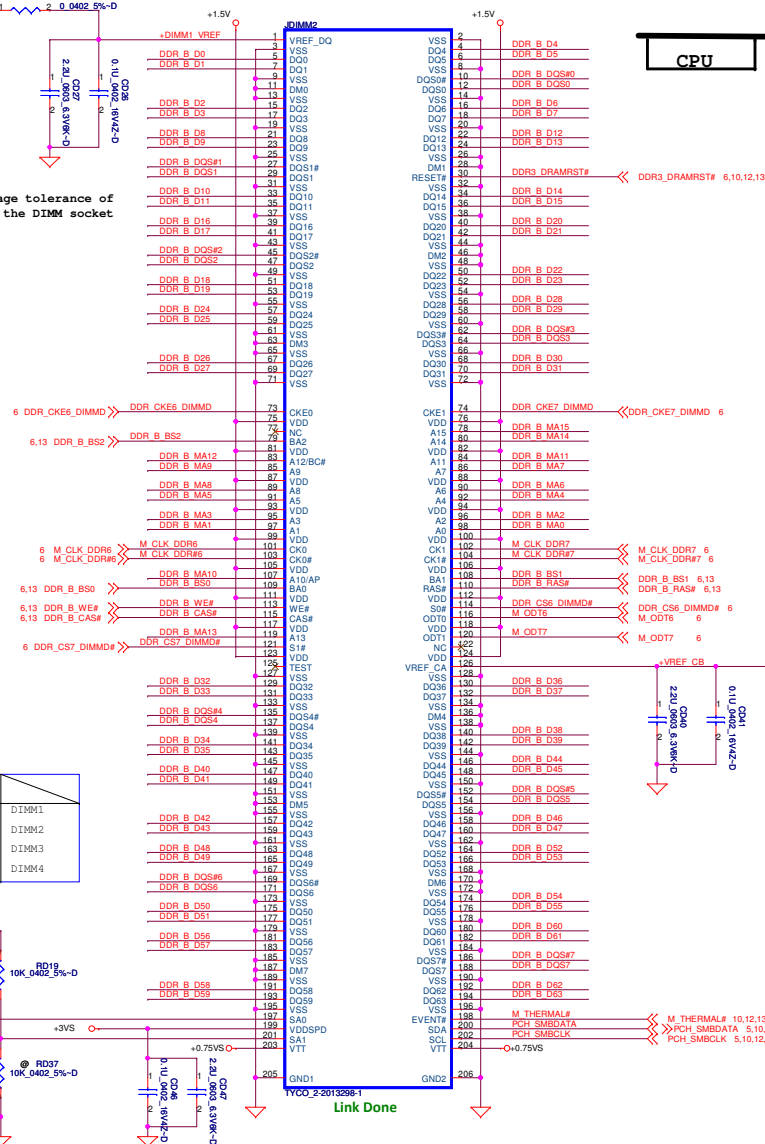
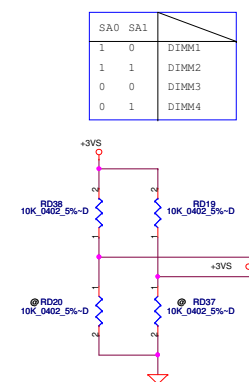
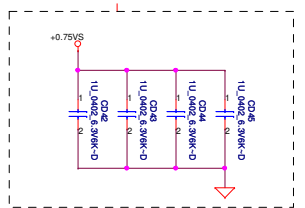
All VREF traces should have 10 mil trace width

Note: Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note: Place near JDIMMB



Layout Note: Place near JDIMMB.203,204



Link Done

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Compal Electronics, Inc.

DDRIII DIMMB

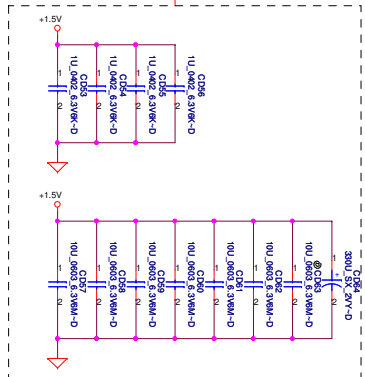
LA-6601P

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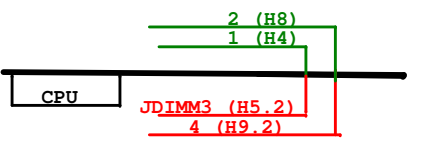
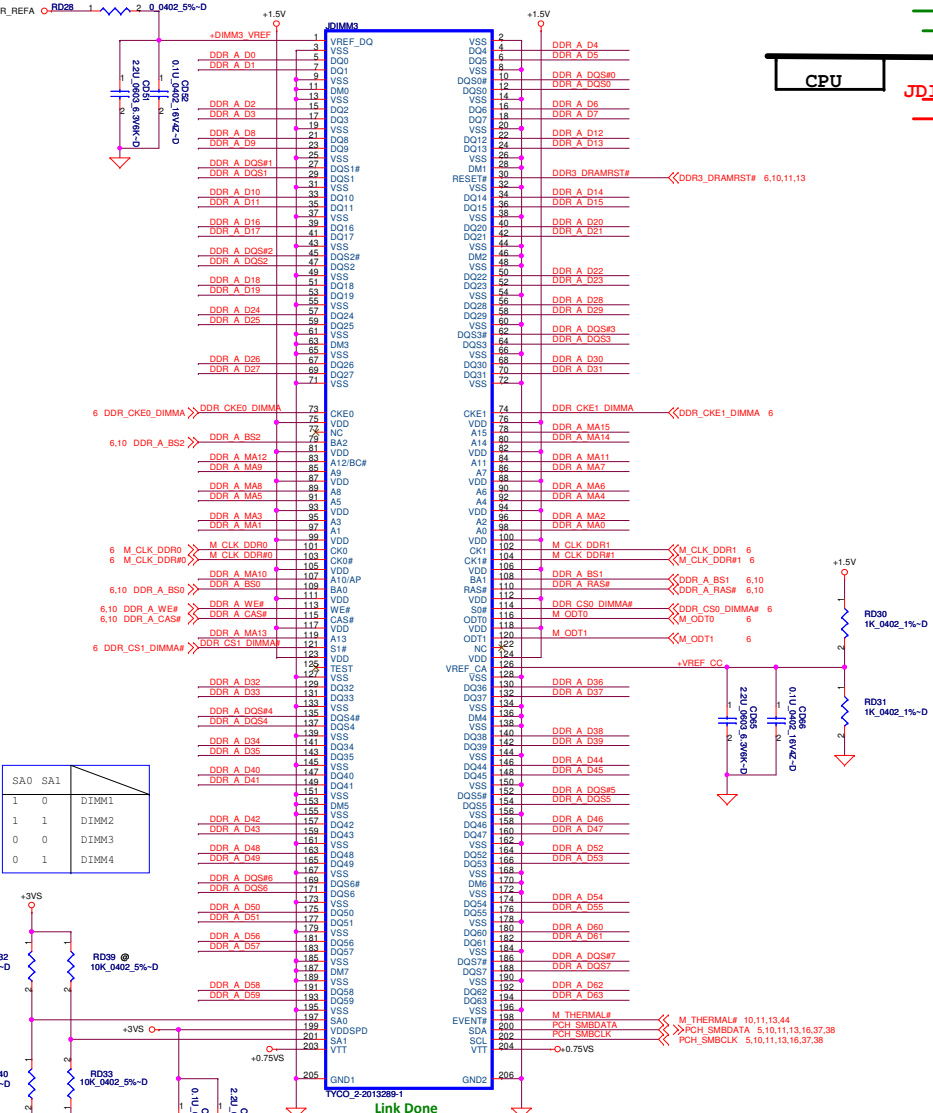
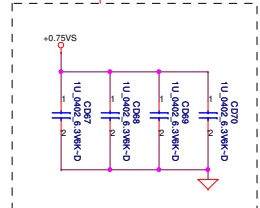


6.10 DDR_A_DQS#(0..7) <<><>
 6.10 DDR_A_DQS(0..7) <<><>
 6.10 DDR_A_D(0..63) <<><>
 6.10 DDR_A_MA(0..15) <<><>

Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203,204



| SA0 | SA1 | |
|-----|-----|-------|
| 1 | 0 | DIMM1 |
| 1 | 1 | DIMM2 |
| 0 | 0 | DIMM3 |
| 0 | 1 | DIMM4 |

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Compaq Electronics, Inc.

DDR III DIMM

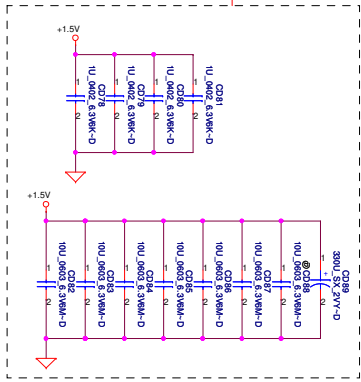
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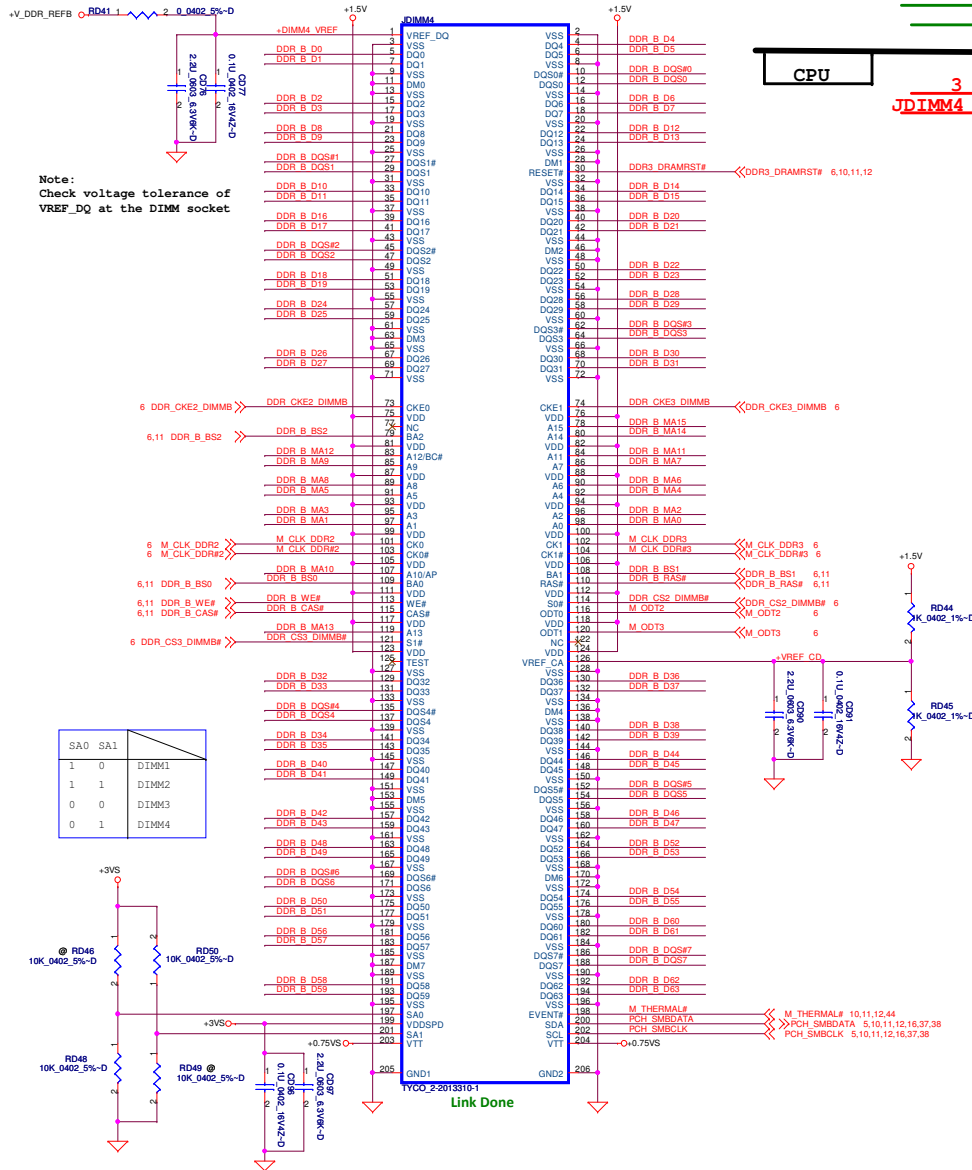
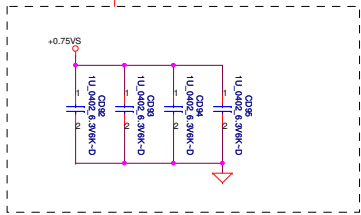


6.11 DDR_B_DQS[0..7] <<<>>>
 6.11 DDR_B_DQS[8..7] <<<>>>
 6.11 DDR_B_DP[0..63] <<<>>>
 6.11 DDR_B_MA[0..15] <<<>>>

Layout Note:
Place near JDIMM8

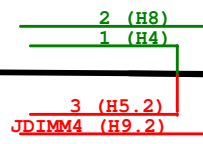


Layout Note:
Place near JDIMM4.203,204

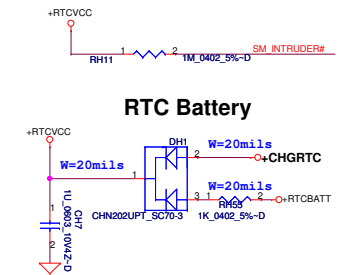


Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

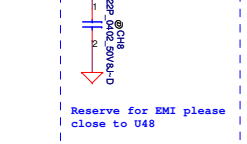
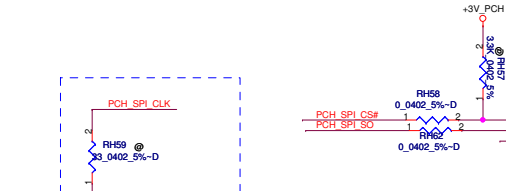
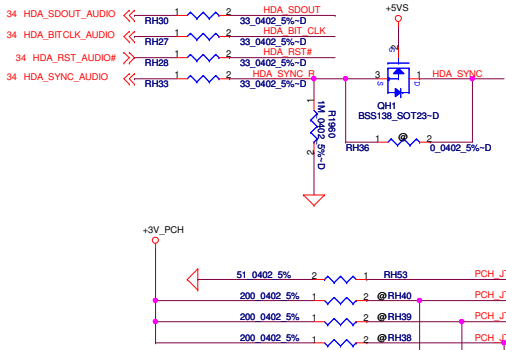
| | | |
|-----|-----|-------|
| SA0 | SA1 | |
| 1 | 0 | DIMM1 |
| 1 | 1 | DIMM2 |
| 0 | 0 | DIMM3 |
| 0 | 1 | DIMM4 |



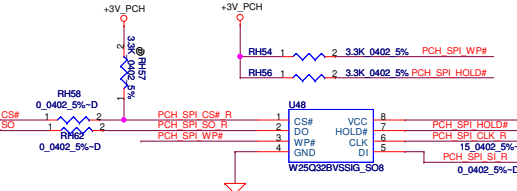
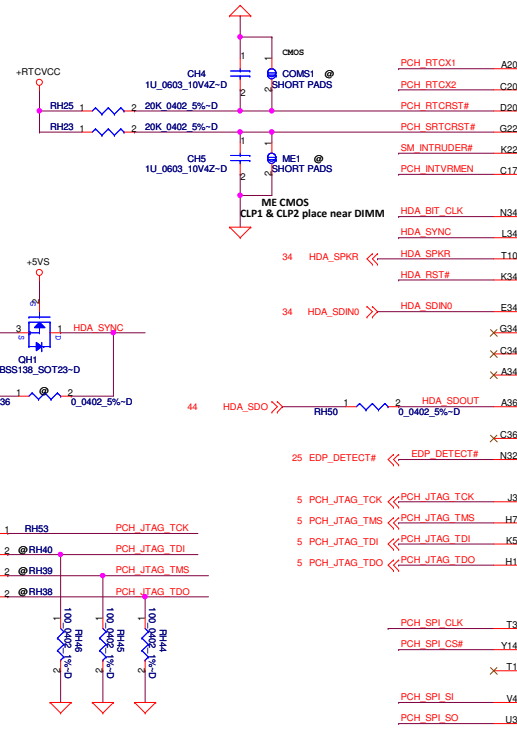
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RTC Battery

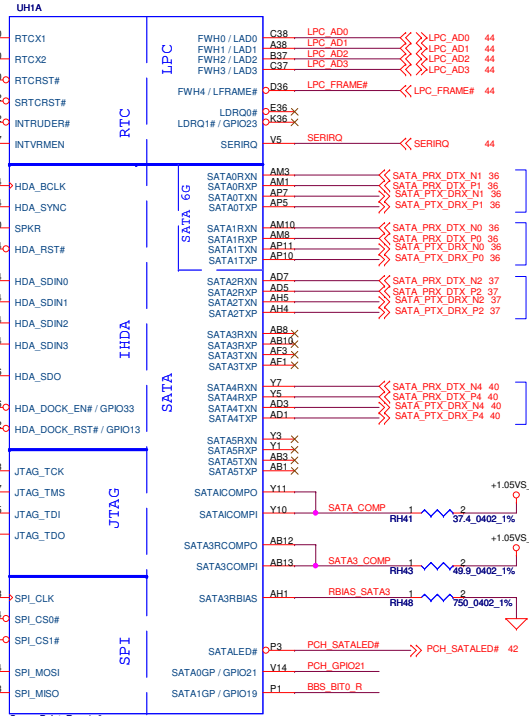


Reserve for EMI please close to U48

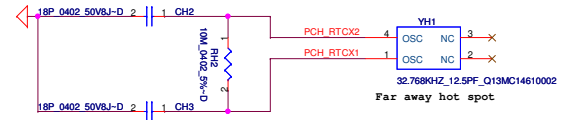


- SPI BIOS Pinout**
- (1) CS# (5) DIO
 - (2) DO (6) CLK
 - (3) WP# (7) HOLD#
 - (4) GND (8) VCC

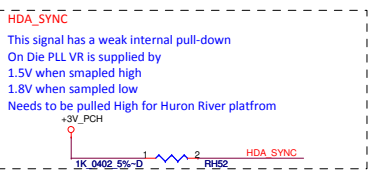
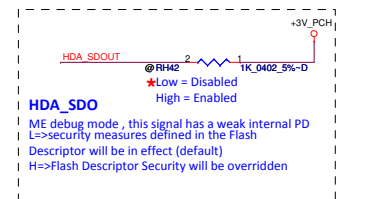
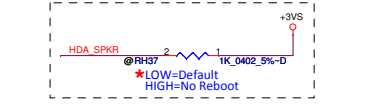
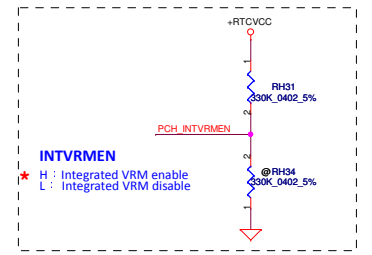
SPI ROM FOR ME (4MByte)



CougarPoint_Rev_Tp0



32.768KHz_12.5PF_Q13MC1461002
Far away hot spot

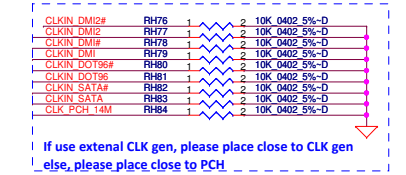
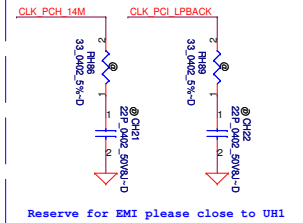
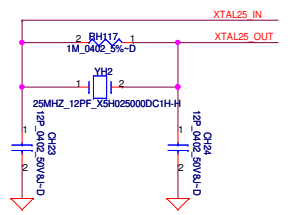
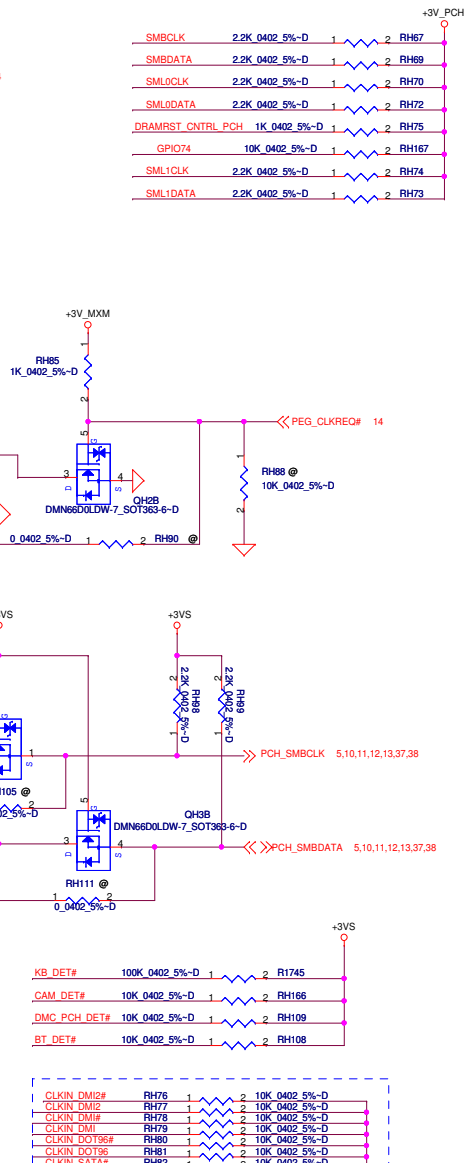
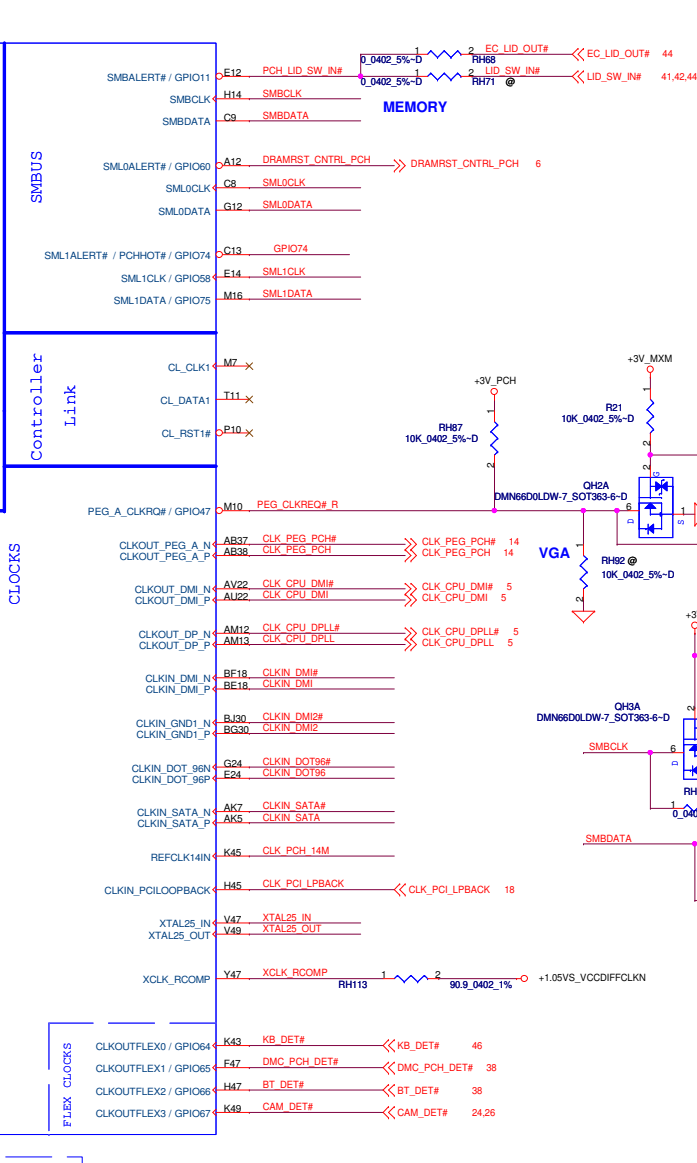
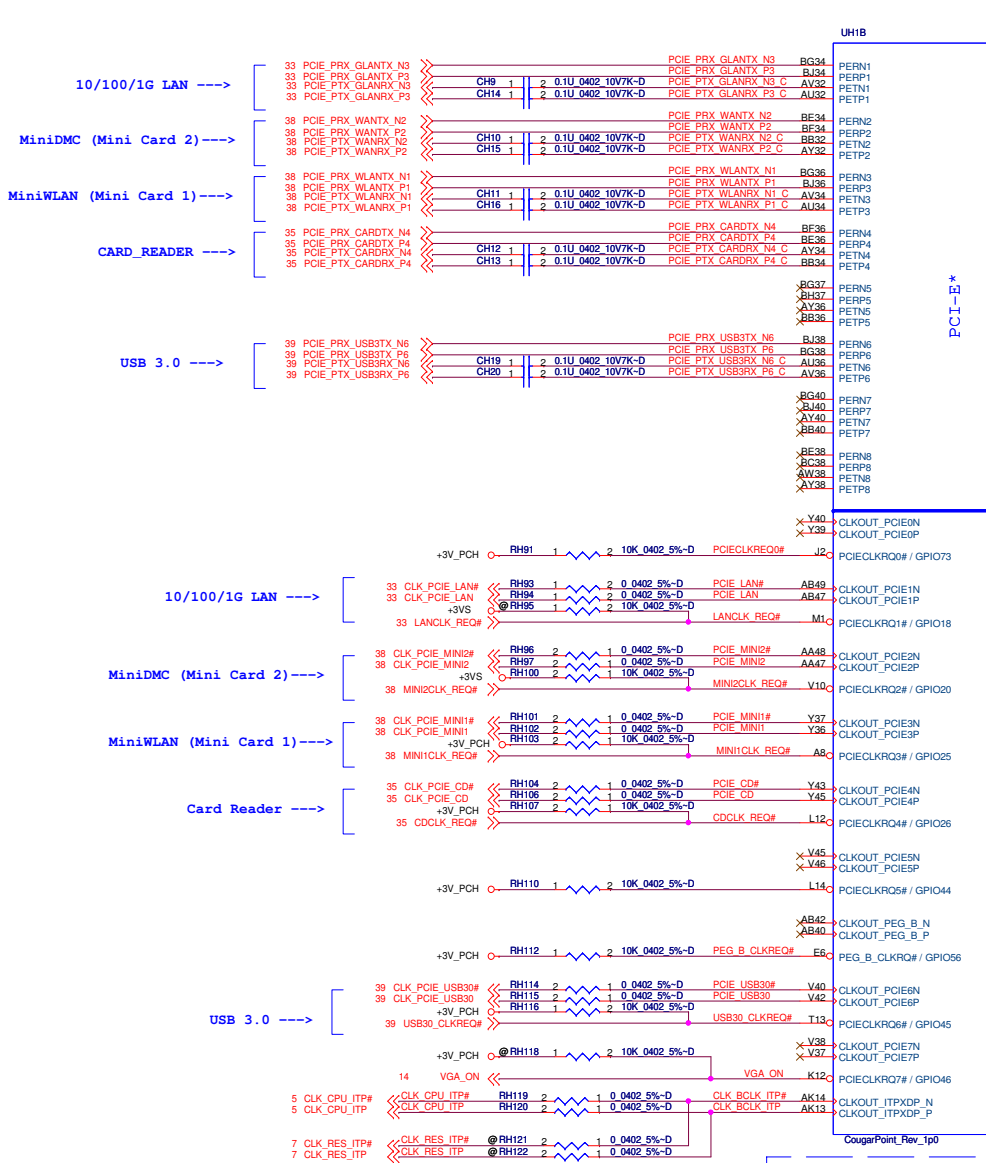


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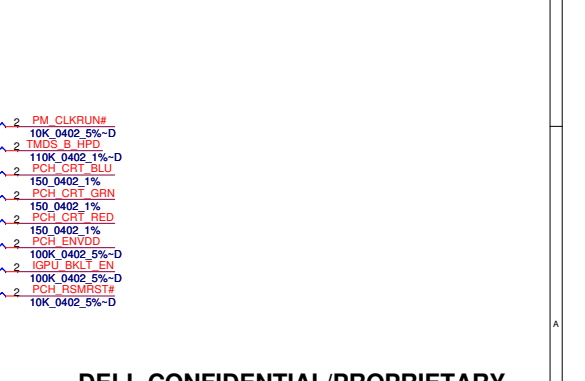
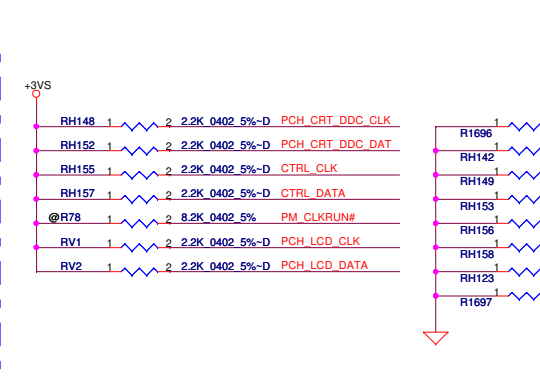
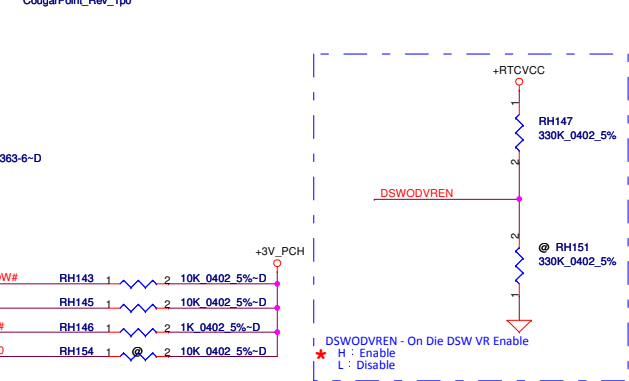
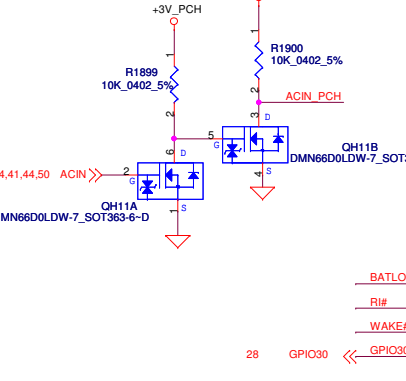
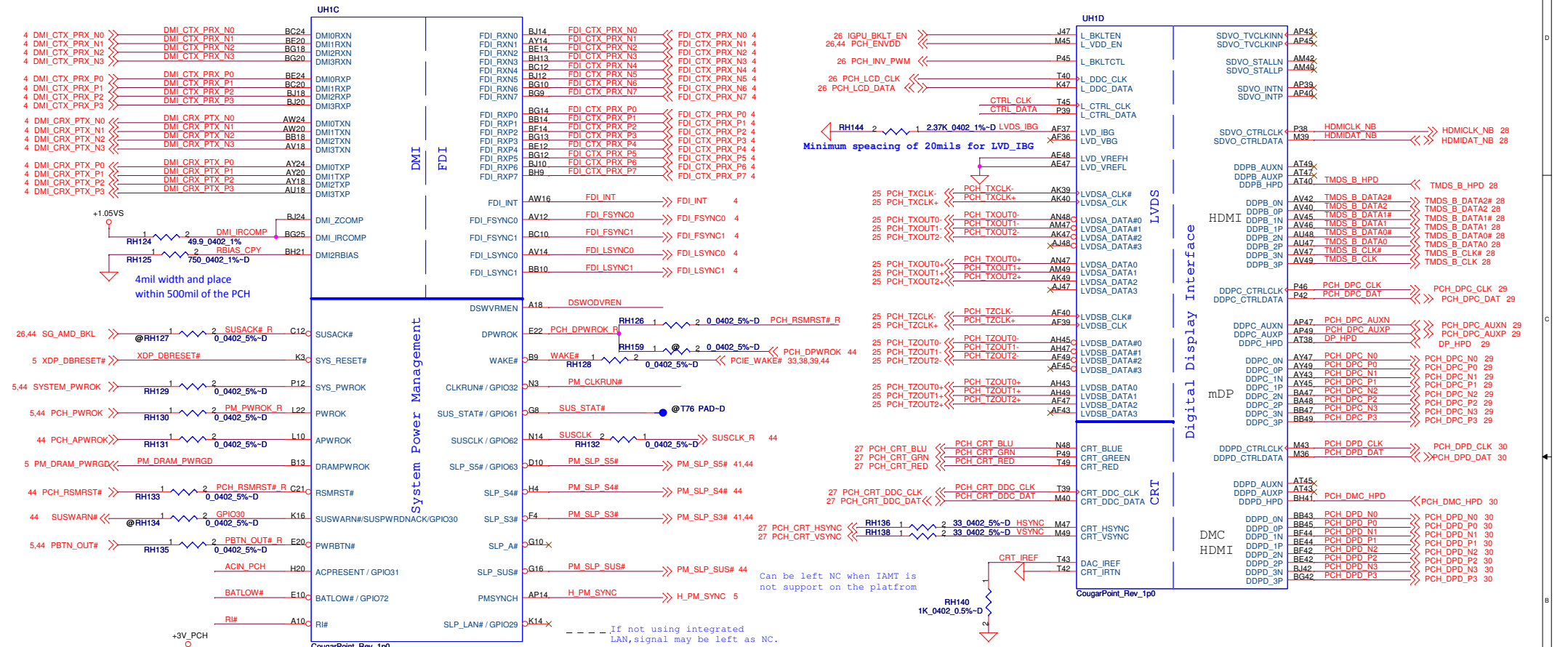
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| Title | | Compal Electronics, Inc. | |
| PCH (1/8) SATA,HDA,SPI, LPC | | | |
| Size | Document Number | Rev | 1.0 |
| | LA-6601P | | |
| Date: | Tuesday, November 30, 2010 | Sheet | 15 of 63 |

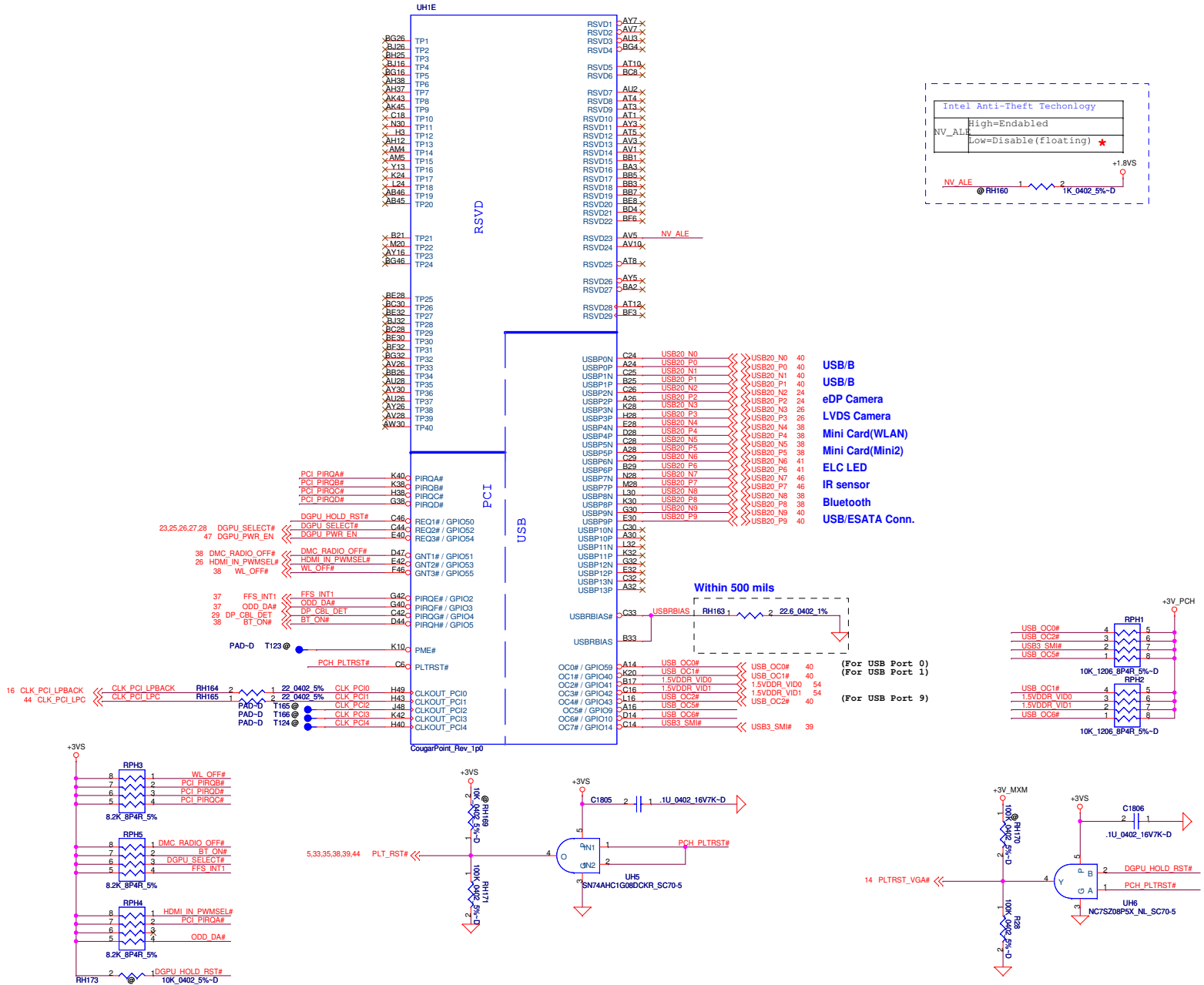
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PCH (2/8) PCIE, SMBUS, CLK
LA-6601P
 Date: Tuesday, November 30, 2010 Sheet 16 of 63

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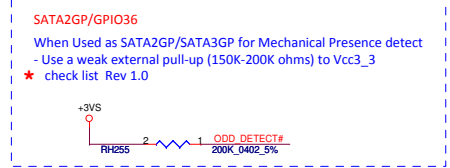
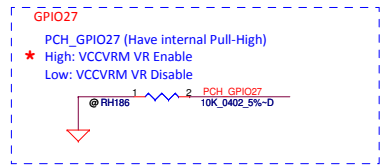
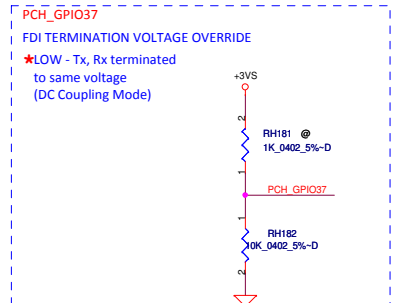
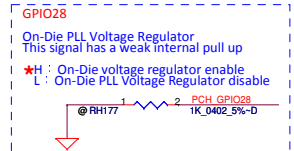
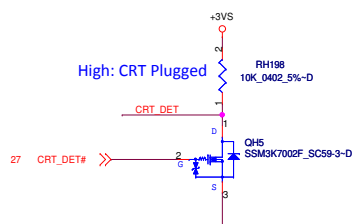
Compal Electronics, Inc.

PCH (4/8) PCI, USB, NVRAM

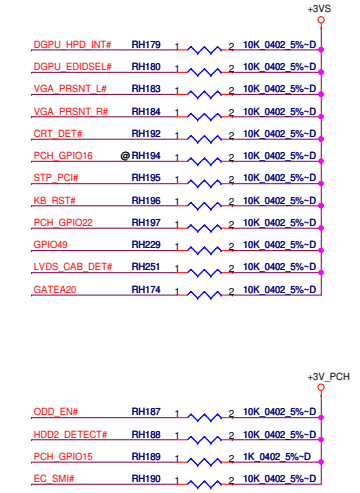
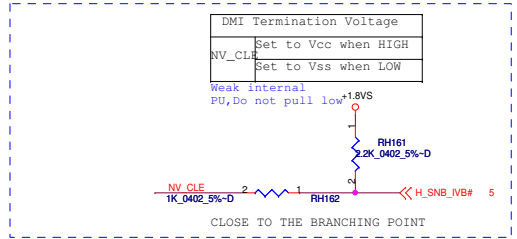
Document Number: **LA-6601P**

Date: Tuesday, November 30, 2010 Sheet 18 of 63

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| Pin | Signal | Component | Value | Notes |
|----------|---------------|---------------|-------|-------|
| 23,26,28 | DGPU_EDIDSEL# | DGPU_EDIDSEL# | A42 | |
| 28 | DGPU_HPD_INT# | DGPU_HPD_INT# | H36 | |
| 44 | EC_SCI# | EC_SCI# | E38 | |
| 44 | EC_SMI# | EC_SMI# | C10 | |
| 38 | BT_RADIO_DIS# | BT_RADIO_DIS# | C4 | |
| | PCH_GPIO15 | | G2 | |
| | PCH_GPIO16 | | U2 | |
| 14 | DGPU_PWROK | DGPU_PWROK | D40 | |
| | PCH_GPIO22 | | T5 | |
| 37 | ODD_EN# | ODD_EN# | E8 | |
| | PCH_GPIO27 | | E16 | |
| | PCH_GPIO28 | | P8 | |
| | STP_PCH# | | K1C | |
| | | | K4C | |
| 37 | ODD_DETECT# | ODD_DETECT# | V8 | |
| | PCH_GPIO37 | | M5 | |
| 14 | VGA_PRSNT_R# | VGA_PRSNT_R# | N2 | |
| 14 | VGA_PRSNT_L# | VGA_PRSNT_L# | M3 | |
| | FFS_INT2 | | V13 | |
| | GPIO49 | | V3 | |
| 36 | HDD2_DETECT# | HDD2_DETECT# | D6 | |
| | VSS_NCTF_1 | | A4 | |
| | VSS_NCTF_2 | | A44 | |
| | VSS_NCTF_3 | | A45 | |
| | VSS_NCTF_4 | | A46 | |
| | VSS_NCTF_5 | | A5 | |
| | VSS_NCTF_6 | | A6 | |
| | VSS_NCTF_7 | | B3 | |
| | VSS_NCTF_8 | | B47 | |
| | VSS_NCTF_9 | | BD1 | |
| | VSS_NCTF_10 | | BD49 | |
| | VSS_NCTF_11 | | BE1 | |
| | VSS_NCTF_12 | | BE49 | |
| | VSS_NCTF_13 | | BE1 | |
| | VSS_NCTF_14 | | BF49 | |
| | VSS_NCTF_15 | | BG2 | |
| | VSS_NCTF_16 | | BG48 | |
| | VSS_NCTF_17 | | BH3 | |
| | VSS_NCTF_18 | | BH47 | |
| | VSS_NCTF_19 | | BJ4 | |
| | VSS_NCTF_20 | | BJ44 | |
| | VSS_NCTF_21 | | BJ45 | |
| | VSS_NCTF_22 | | BJ46 | |
| | VSS_NCTF_23 | | BJ5 | |
| | VSS_NCTF_24 | | BJ6 | |
| | VSS_NCTF_25 | | C2 | |
| | VSS_NCTF_26 | | C48 | |
| | VSS_NCTF_27 | | D1 | |
| | VSS_NCTF_28 | | D49 | |
| | VSS_NCTF_29 | | E1 | |
| | VSS_NCTF_30 | | E49 | |
| | VSS_NCTF_31 | | F1 | |
| | VSS_NCTF_32 | | F49 | |

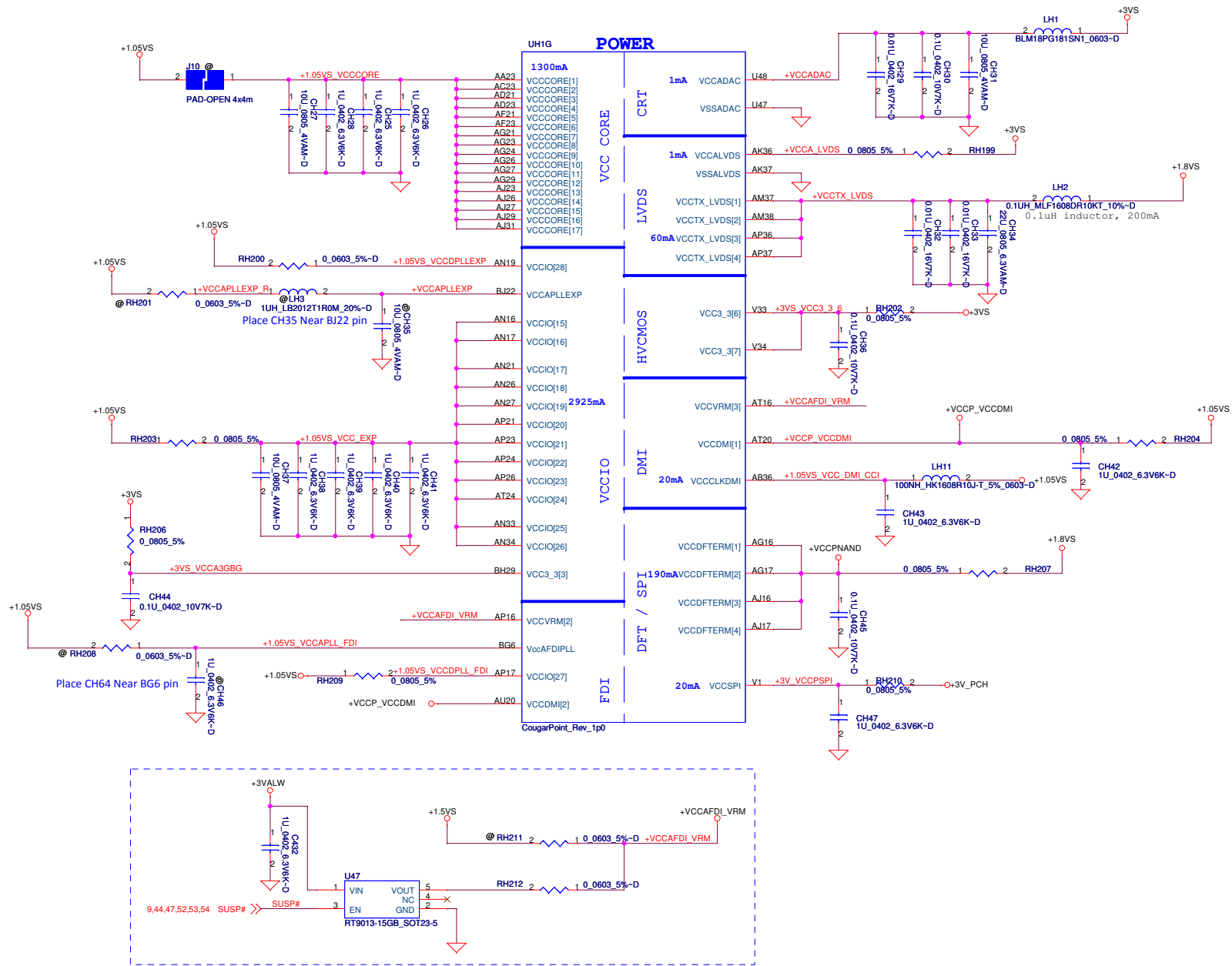


Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.

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| | | | |
|-------|----------------------------|----------------------------------|----------|
| | | Compal Electronics, Inc. | |
| | | PCH (5/8) GPIO, CPU, MISC | |
| Size | Document Number | Rev 1.0 | |
| | | LA-6601P | |
| Date: | Tuesday, November 30, 2010 | Sheet | 19 of 63 |

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PCH Power Rail Table

| Voltage Rail | Voltage | S0 Iccmax Current (A) |
|--------------|-----------|-----------------------|
| V_PROC_IO | 1.05 | 0.001 |
| V5REF | 5 | 0.001 |
| V5REF_Sus | 5 | 0.001 |
| Vcc3_3 | 3.3 | 0.266 |
| VccADAC | 3.3 | 0.001 |
| VccADPLLA | 1.05 | 0.08 |
| VccADPLLB | 1.05 | 0.08 |
| VccCore | 1.05 | 1.3 |
| VccDMI | 1.05 | 0.042 |
| VccIO | 1.05 | 2.925 |
| VccASW | 1.05 | 1.01 |
| VccSPI | 3.3 | 0.02 |
| VccDSW | 3.3 | 0.003 |
| VccPNAND | 1.8 | 0.19 |
| VccRTC | 3.3 | 6 uA |
| VccSus3_3 | 3.3 | 0.119 |
| VccSusHDA | 3.3 / 1.5 | 0.01 |
| VccVRM | 1.8 / 1.5 | 0.16 |
| VccCLKDMI | 1.05 | 0.02 |
| VccSSC | 1.05 | 0.095 |
| VccDIFFCLKN | 1.05 | 0.055 |
| VccALVDS | 3.3 | 0.001 |
| VccTX_LVDS | 1.8 | 0.06 |

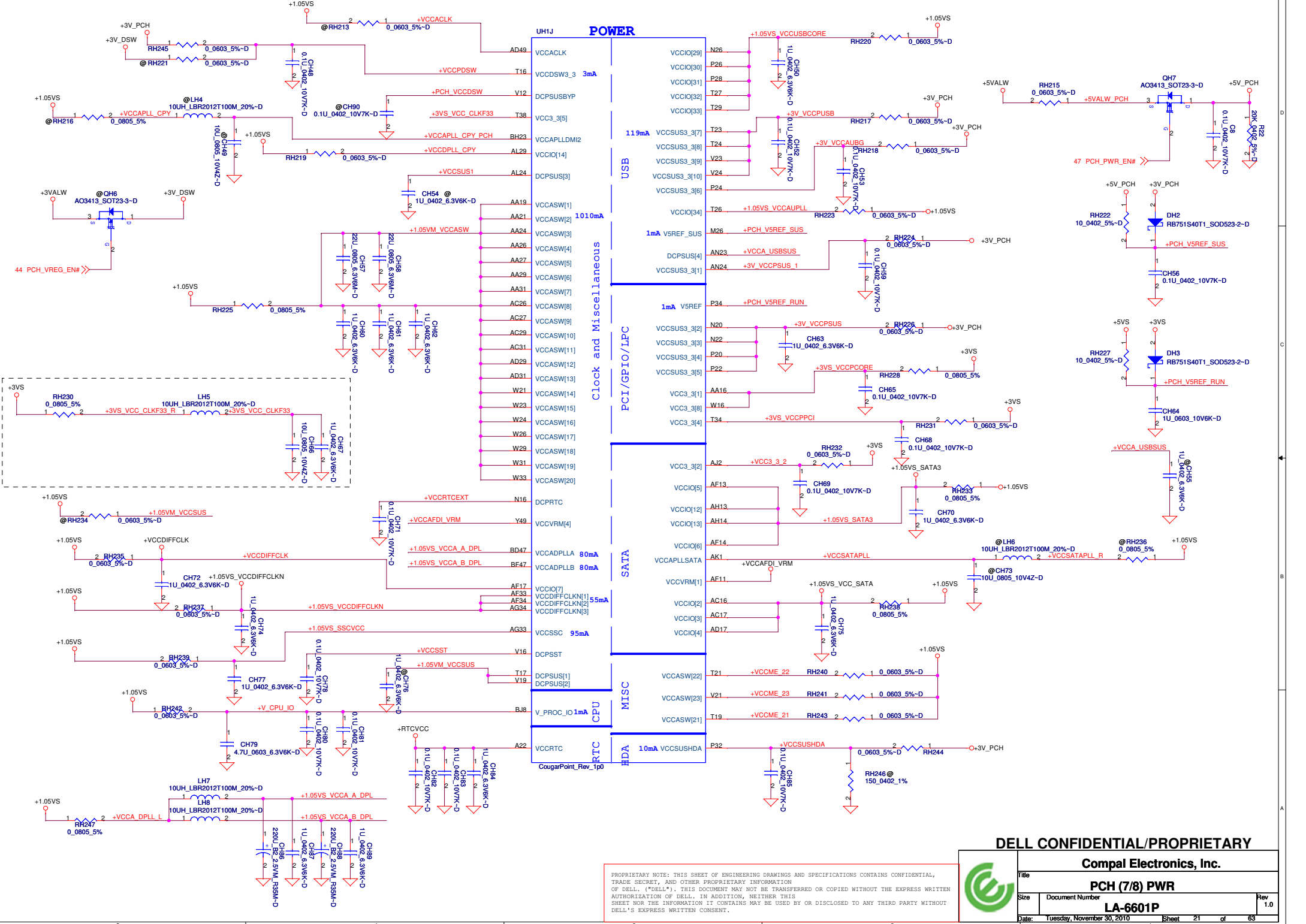
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| | | | | | |
|-------|----------------------------|-------|---------------|----|----|
| Title | | | PCH (6/8) PWR | | |
| Size | Document Number | Rev | | | |
| | LA-6601P | 1.0 | | | |
| Date: | Tuesday, November 30, 2010 | Sheet | 20 | of | 63 |

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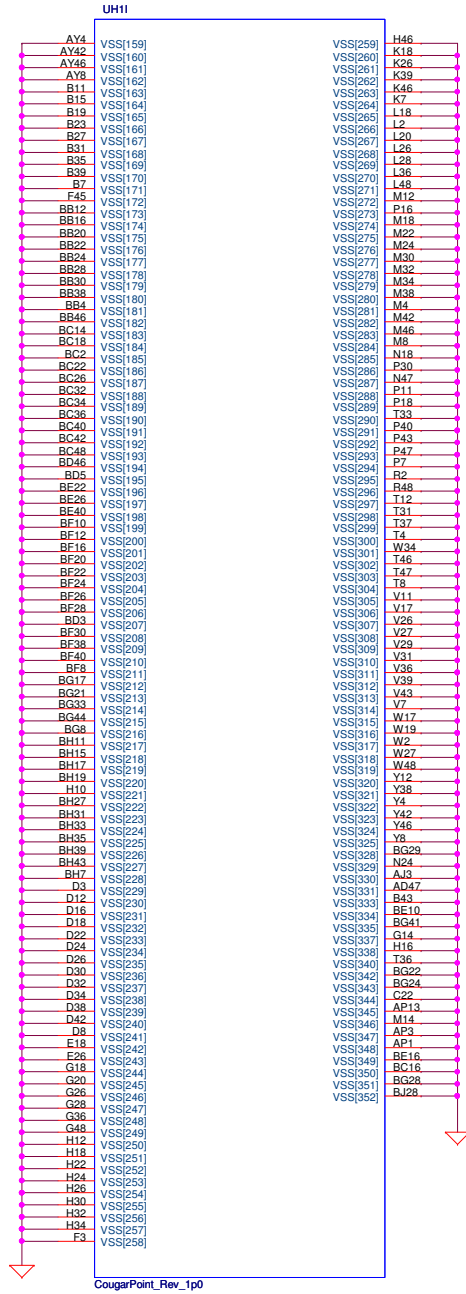
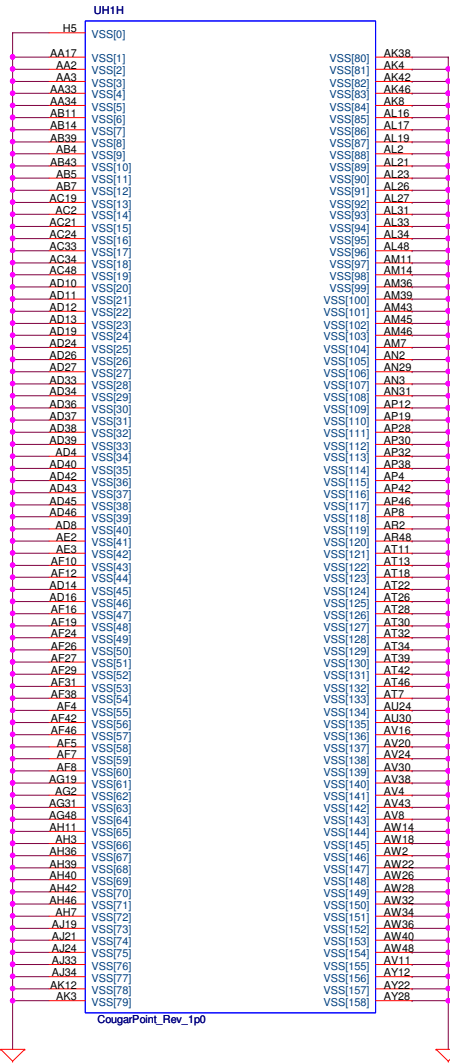


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| | | | |
|---------------------------------|----------------------------|------------|----------|
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| PCH (7/8) PWR | | | |
| File | | | |
| Size | Document Number | Rev | |
| | LA-6601P | 1.0 | |
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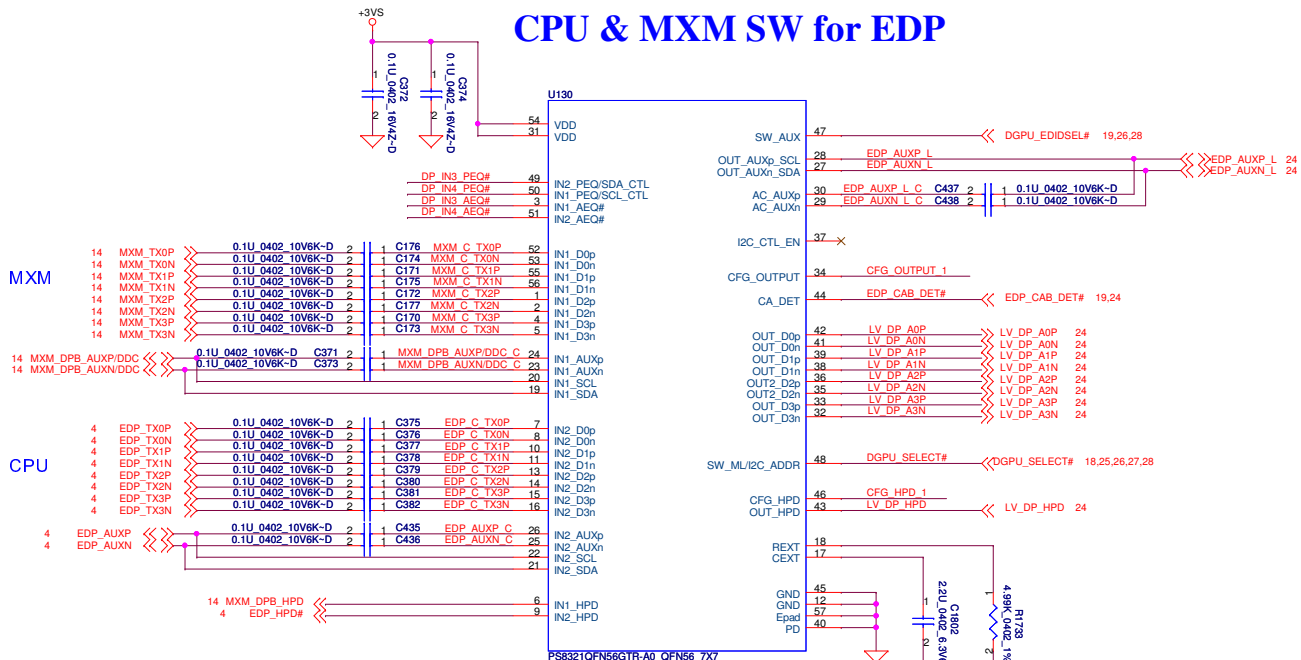
PCH (8/8) VSS

LA-6601P

Rev 1.0

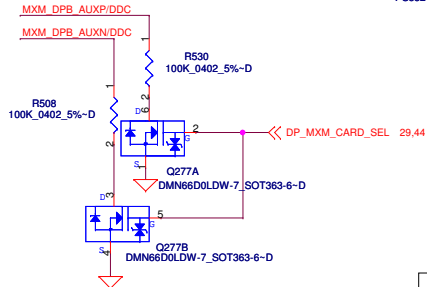
Date: Tuesday, November 30, 2010 Sheet 22 of 63

CPU & MXM SW for EDP



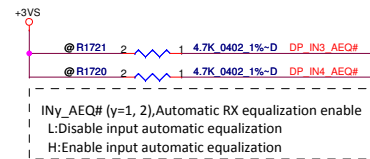
MXM

CPU

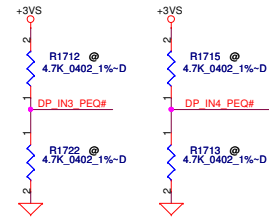


| MXM_MFG_SEL | GPU Source |
|-------------|------------|
| 0 | NVIDIA |
| 1 | ATI |

| AUX_SEL/SEL1&2 | Chanel | Source |
|----------------|--------|--------|
| 0 | A | CPU |
| 1 | B | MXM |

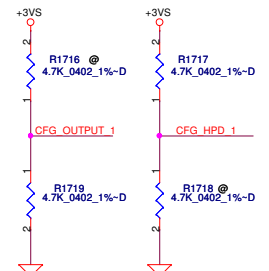


INy_AEQ# (y=1, 2), Automatic RX equalization enable
L: Disable input automatic equalization
H: Enable input automatic equalization



INy_PEQ# (y = 1, 2), Programmable input equalization level setting
L: Low EQ setting (LEQ), default
H: High EQ setting (HEQ)
M: No EQ

CFG_OUTPUT: output configuration
L: Output is tracking DPCD register setting (auto interception)
H: Output swing level fixed at 600mV and no pre-emphasis
M: Output swing level is fixed at 400mV and no pre-emphasis



CFG_HPDP, HPD switching configuration
L: HPD is switched by SW_ML
H: HPD is switched by SW_AUX
M: HPD is switched with overlap

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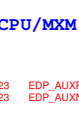
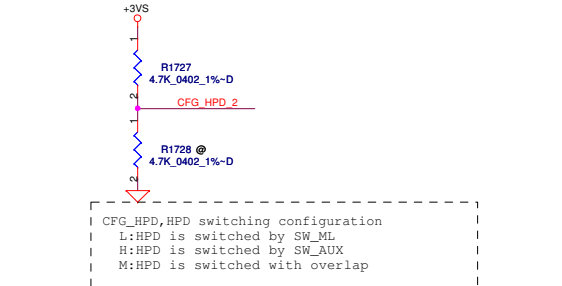
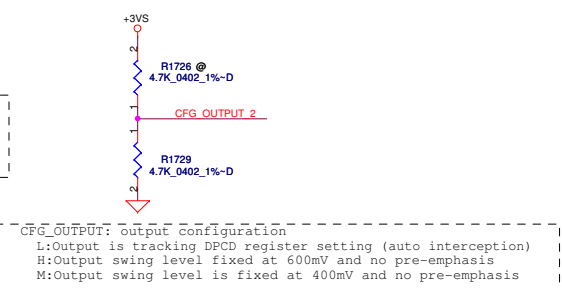
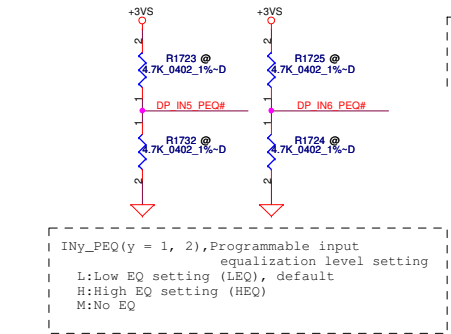
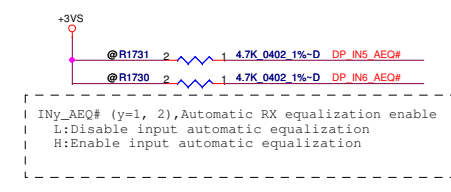
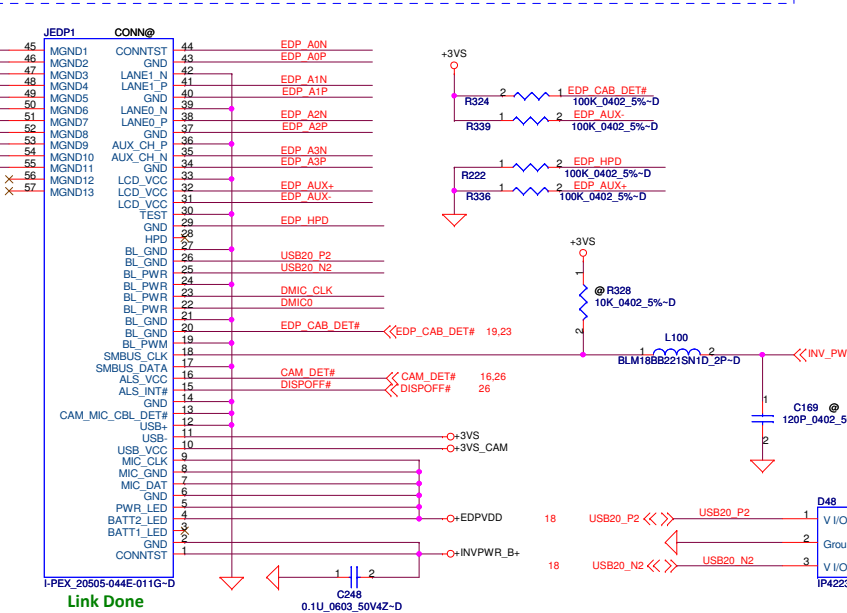
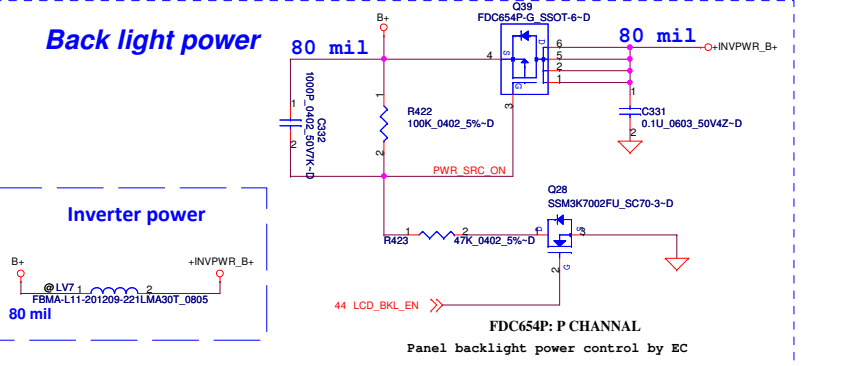
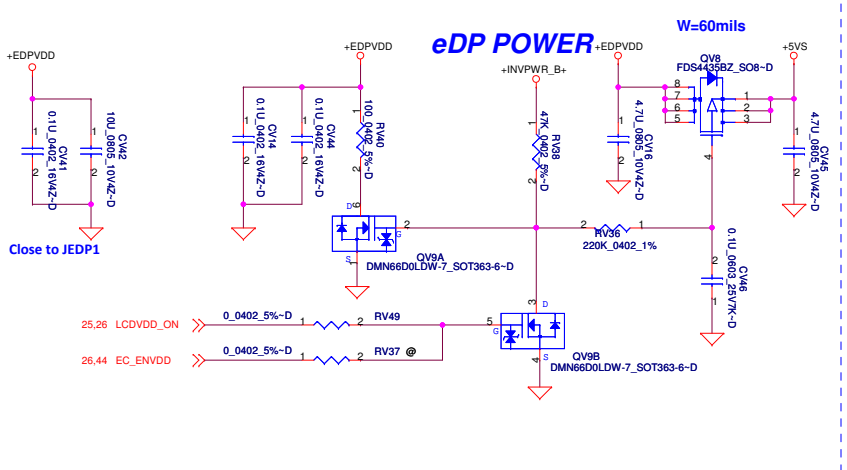
Compal Electronics, Inc.

eDP SW- GPU & CPU

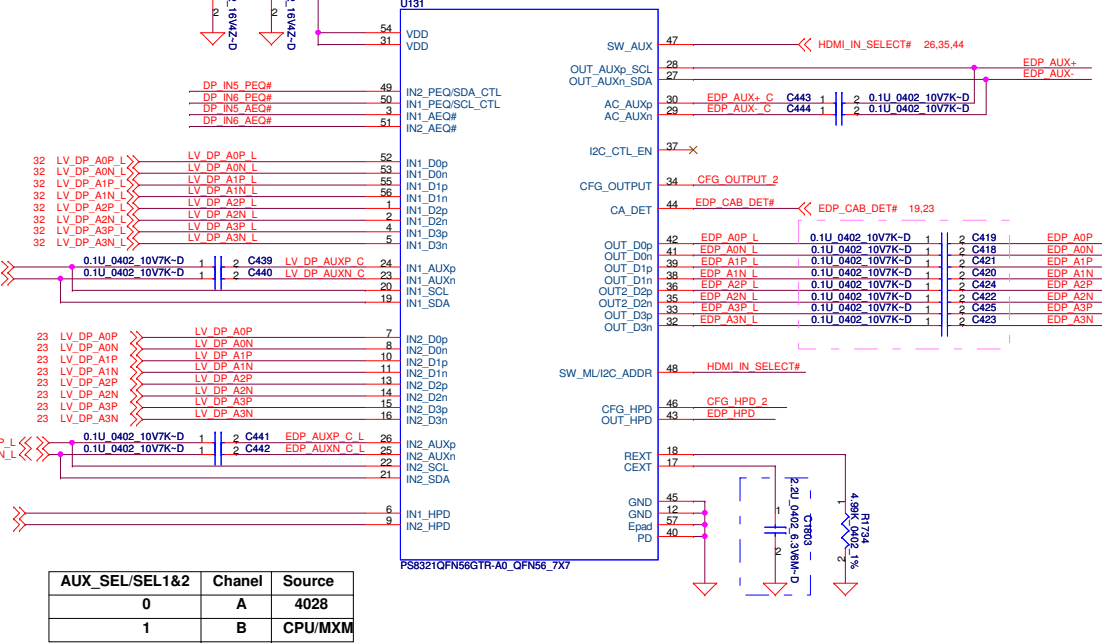
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| Size | Document Number | Rev |
| | | 1.0 |
| Date: | Tuesday, November 30, 2010 | Sheet 23 of 63 |

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CPU/GPU & 4028 SW for DPB

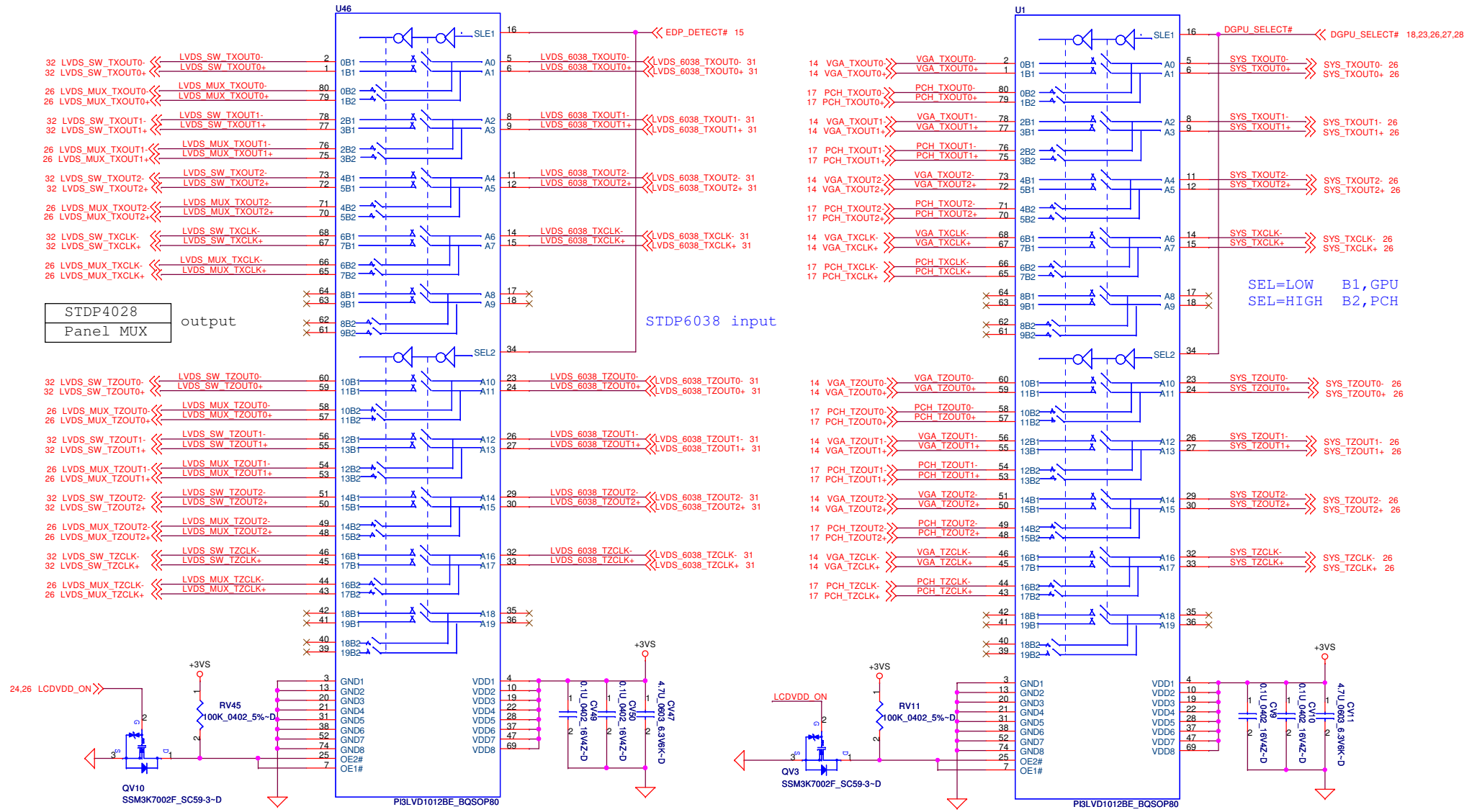


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| Compal Electronics, Inc. | | | |
| eDP SW- 4028 & eDP CONN | | | |
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| | | LA-6601P | |
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| | |
|-----|-----|
| SEL | Y |
| L | GPU |
| H | PCH |

STDP6038 SW STDP4028 PCH/GPU AUX for LVDS



STDP4028
Panel MUX
output

STDP6038 input

SEL=LOW B1, GPU
SEL=HIGH B2, PCH

| | |
|-----|-----------|
| SEL | Y |
| L | STDP4028 |
| H | Panel MUX |

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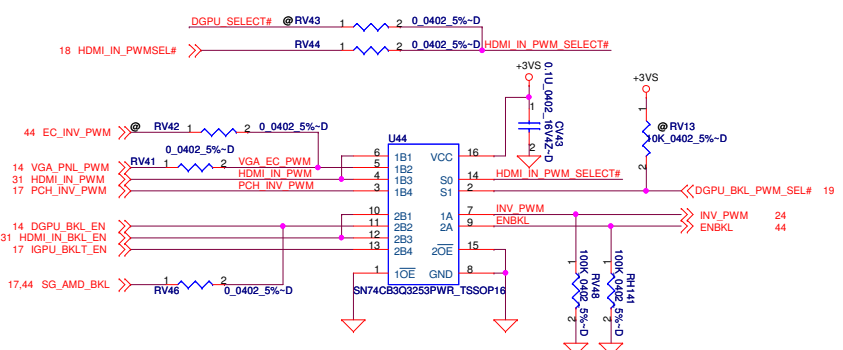
Compal Electronics, Inc.

LVDS SW- 1 to 2 & GPU/PCH

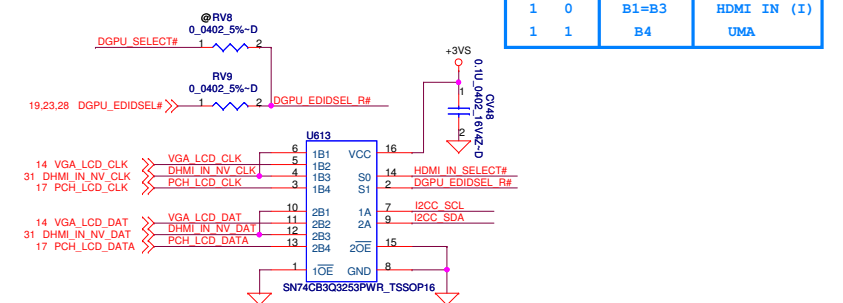
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| Size | Document Number | Rev |
| | LA-6601P | 1.0 |
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LCD Backlight Selector



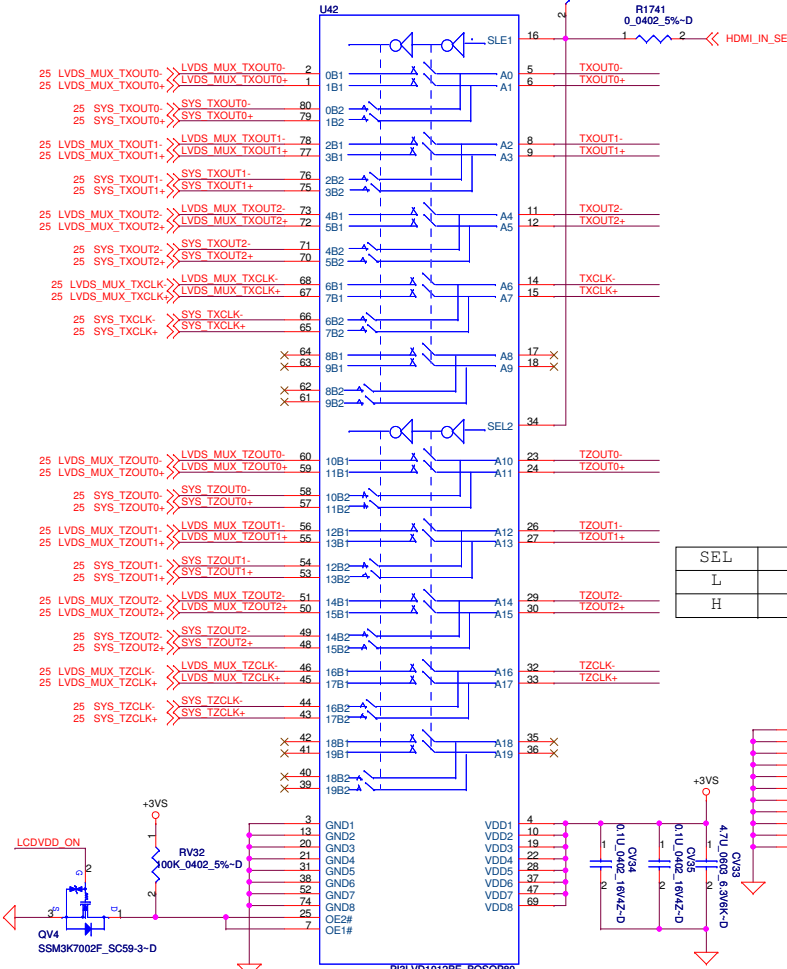
LCD DDC Selector



| S1 | S0 | Output | Y |
|----|----|--------|-------------|
| 0 | 0 | B1=B3 | HDMI IN (D) |
| 0 | 1 | B2 | DSC |
| 1 | 0 | B1=B3 | HDMI IN (I) |
| 1 | 1 | B4 | UMA |

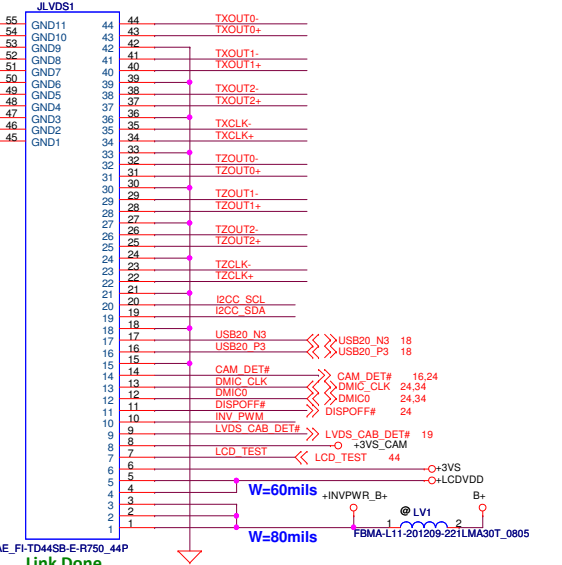
| S1 | S0 | Output | Y |
|----|----|--------|-------------|
| 0 | 0 | B1=B3 | HDMI IN (D) |
| 0 | 1 | B2 | DSC |
| 1 | 0 | B1=B3 | HDMI IN (I) |
| 1 | 1 | B4 | UMA |

PCH/GPU MUX & 6038 MUX SW for LVDS



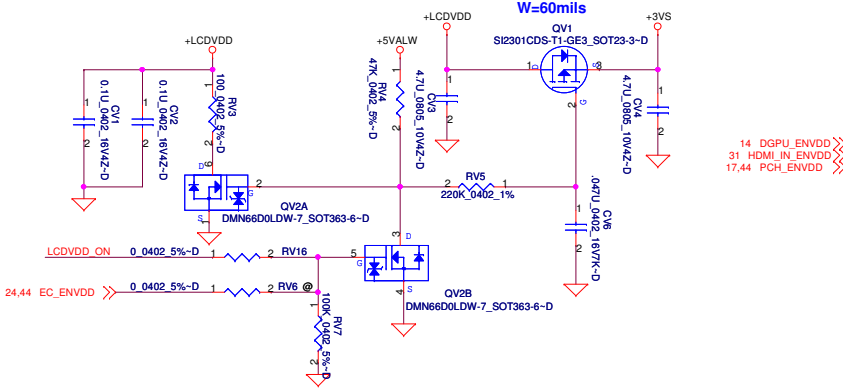
| SEL | Y |
|-----|----|
| L | B1 |
| H | B2 |

LVDS Conn.



| S1 | S0 | YA | YB | Y |
|----|----|----|----|---------|
| 0 | 0 | A0 | B0 | HDMI IN |
| 0 | 1 | A1 | B1 | DSC |
| 1 | 0 | A2 | B2 | HDMI IN |
| 1 | 1 | A3 | B3 | UMA |

LCD POWER



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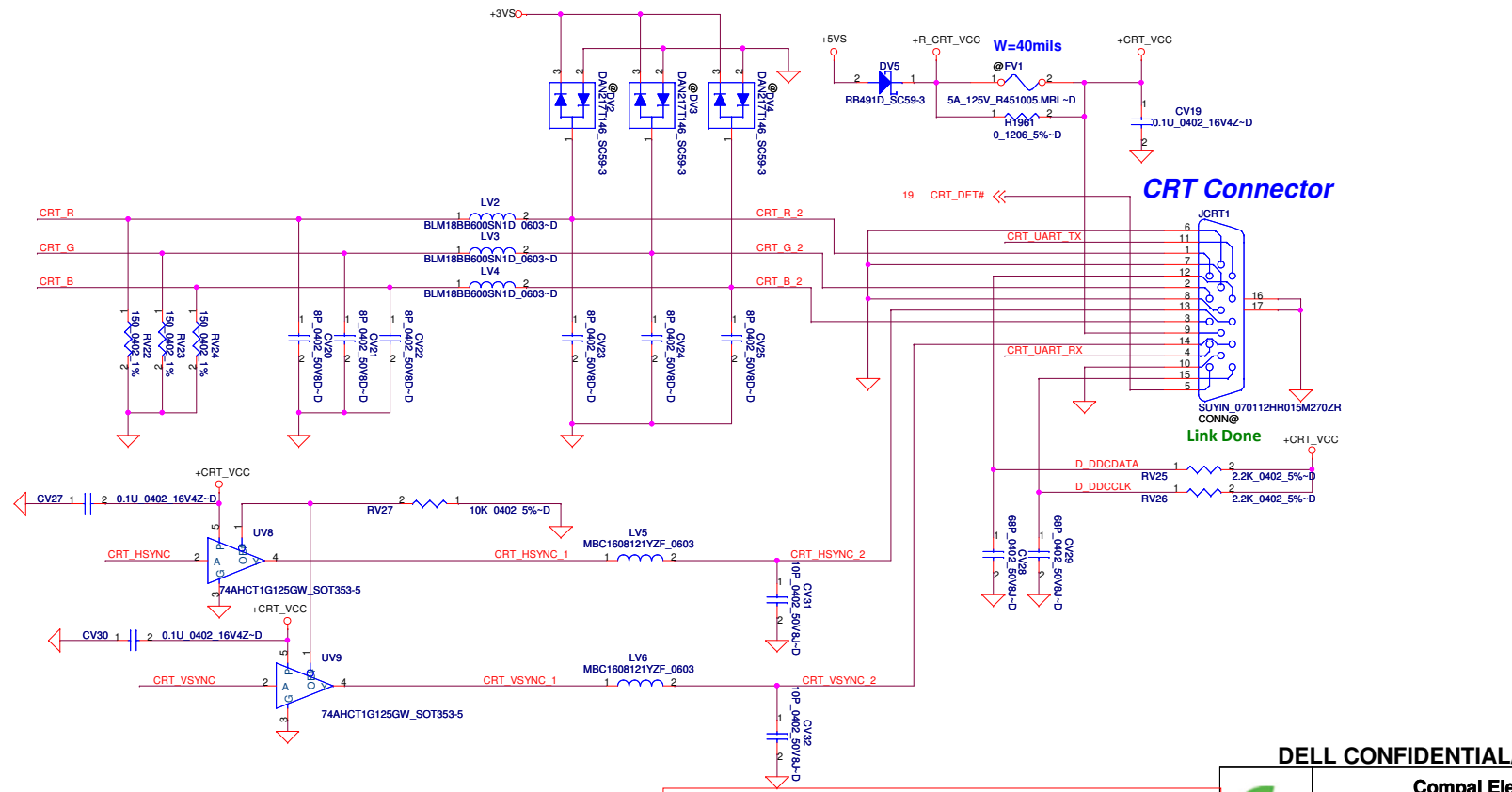
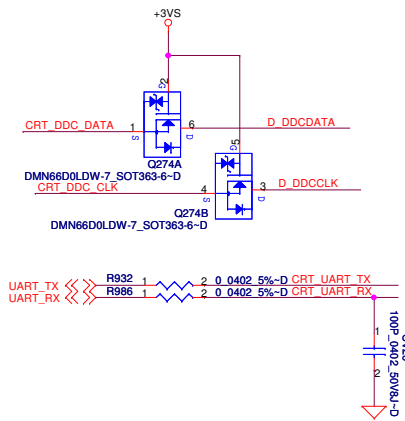
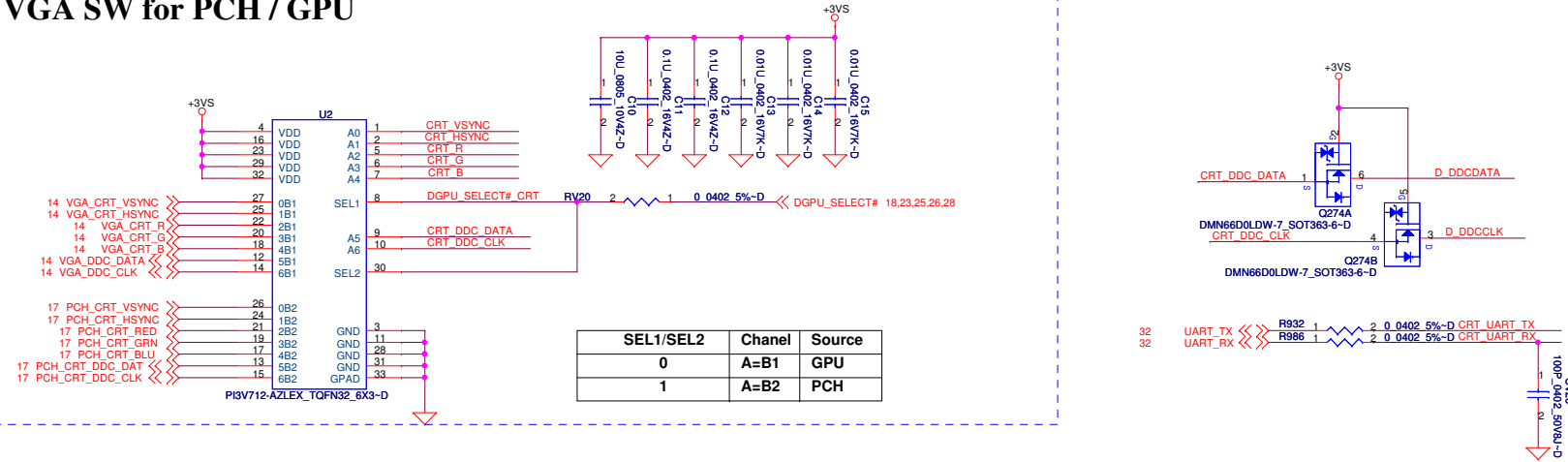
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Size: Document Number LA-6601P Rev 1.0

Date: Tuesday, November 30, 2010 Sheet 26 of 63

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VGA SW for PCH / GPU

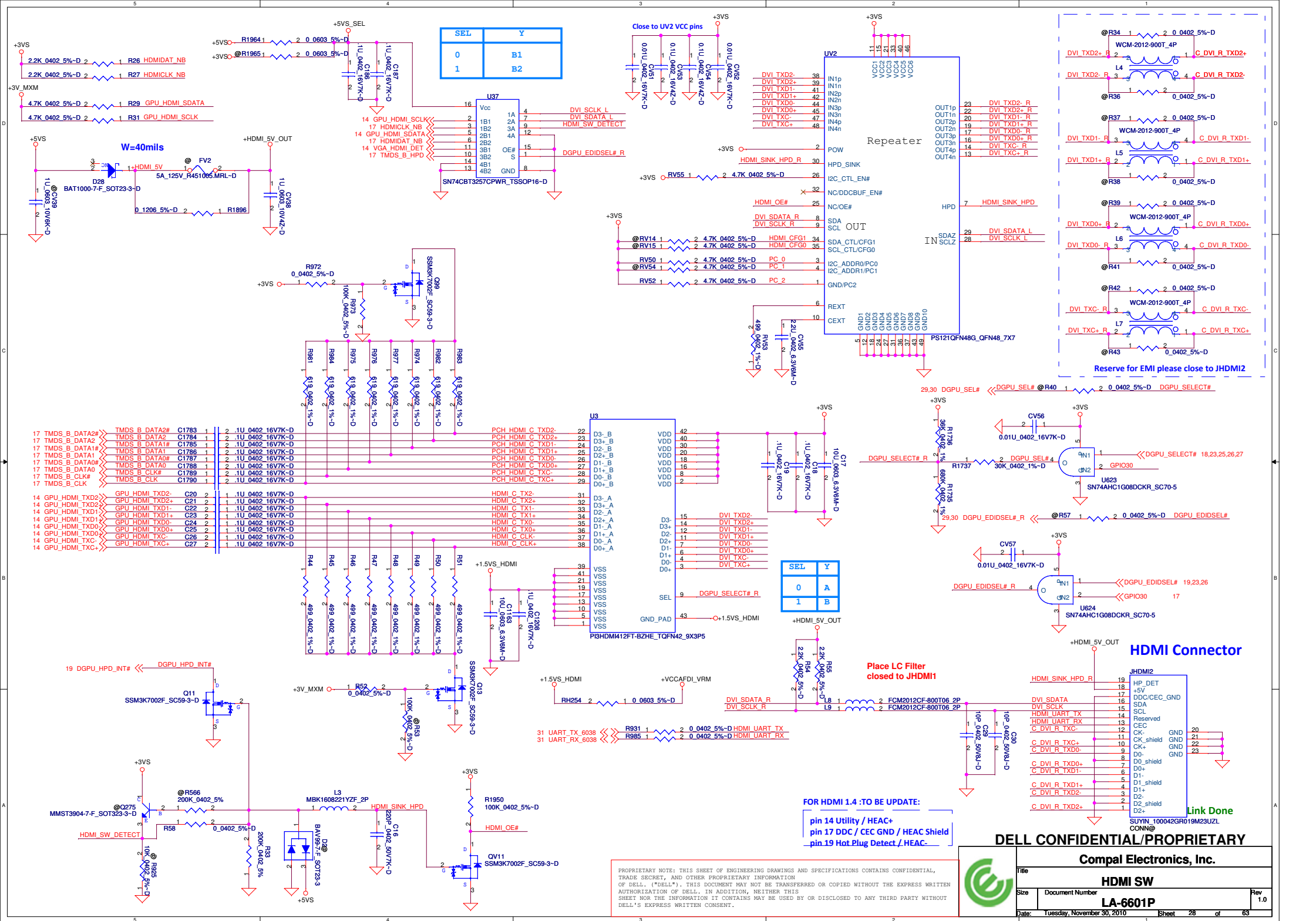


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| | |
|--------------------------|------------------------------------|
| Compal Electronics, Inc. | |
| Title CRT SW | |
| Size | Document Number LA-6601P |
| Date | Tuesday, November 30, 2010 |
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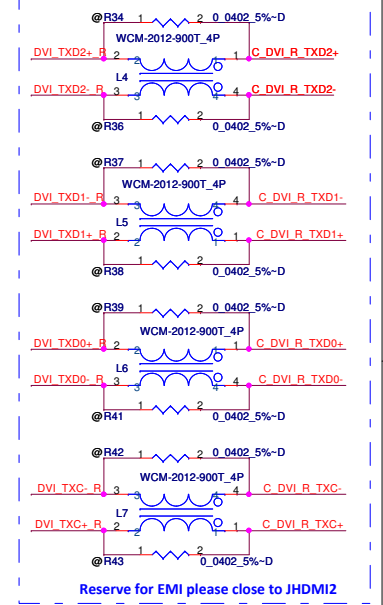


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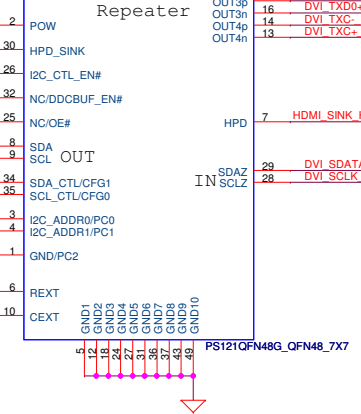
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
HDMI SW
LA-6601P
Date: Tuesday, November 30, 2010 Sheet 28 of 63



| | | | |
|------|-----------------|-----|--|
| File | HDMI SW | | |
| Size | Document Number | Rev | |
| | LA-6601P | 1.0 | |

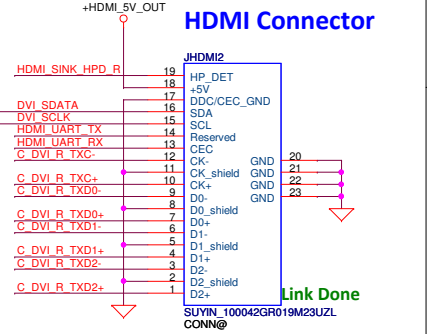


Reserve for EMI please close to JHDMI2

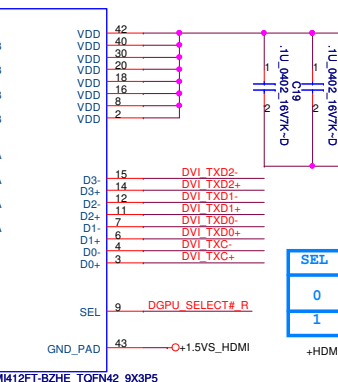


Place LC Filter closed to JHDMI1

FOR HDMI 1.4 :TO BE UPDATE:
pin 14 Utility / HEAC+
pin 17 DDC / CEC GND / HEAC Shield
pin 19 Hot Plug Detect / HEAC-



Link Done
SUVIN 100042GR019M23U2L
CONN@



Place LC Filter closed to JHDMI1

FOR HDMI 1.4 :TO BE UPDATE:
pin 14 Utility / HEAC+
pin 17 DDC / CEC GND / HEAC Shield
pin 19 Hot Plug Detect / HEAC-



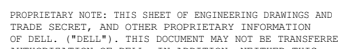
Place LC Filter closed to JHDMI1

FOR HDMI 1.4 :TO BE UPDATE:
pin 14 Utility / HEAC+
pin 17 DDC / CEC GND / HEAC Shield
pin 19 Hot Plug Detect / HEAC-



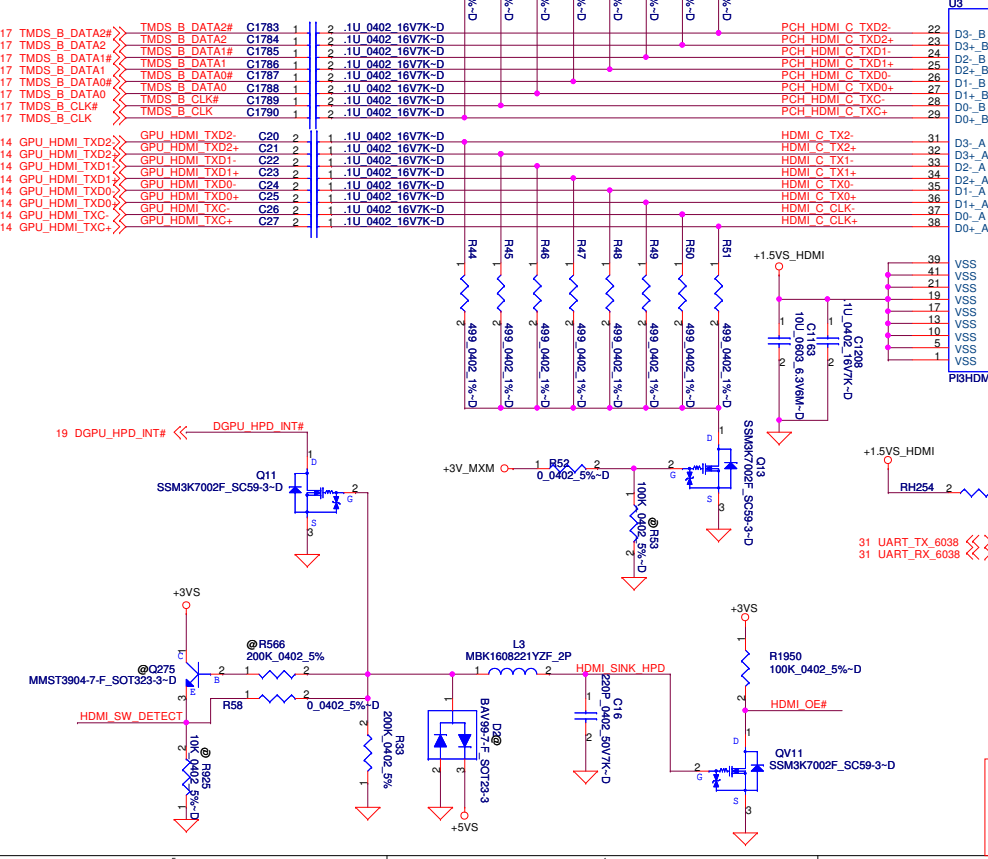
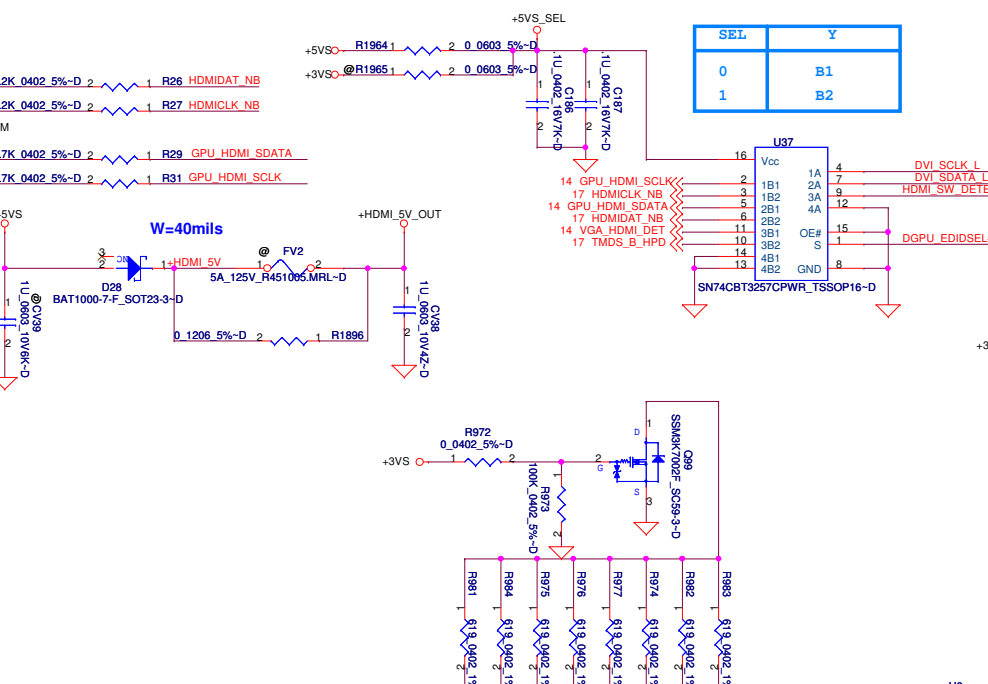
Place LC Filter closed to JHDMI1

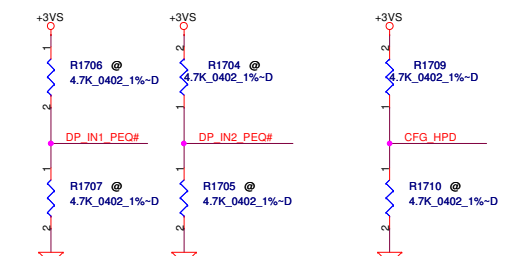
FOR HDMI 1.4 :TO BE UPDATE:
pin 14 Utility / HEAC+
pin 17 DDC / CEC GND / HEAC Shield
pin 19 Hot Plug Detect / HEAC-



Place LC Filter closed to JHDMI1

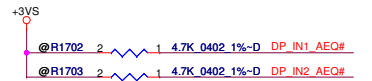
FOR HDMI 1.4 :TO BE UPDATE:
pin 14 Utility / HEAC+
pin 17 DDC / CEC GND / HEAC Shield
pin 19 Hot Plug Detect / HEAC-





Iny_PEQ(y = 1, 2), Programmable input equalization level setting
 L: Low EQ setting (LEQ), default
 H: High EQ setting (HEQ)
 M: No EQ

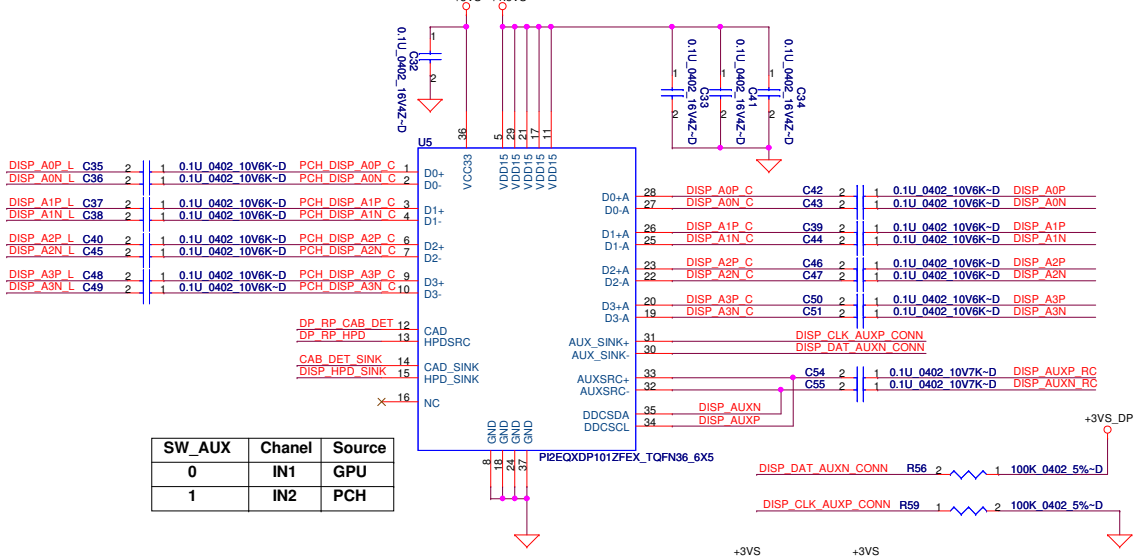
CFG_HPD, HPD switching configuration
 L: HPD is switched by SW_ML
 H: HPD is switched by SW_AUX
 M: HPD is switched with overlap



Iny_AEQ(y = 1, 2), Automatic RX equalization enable
 L: Disable input automatic equalization
 H: Enable input automatic equalization

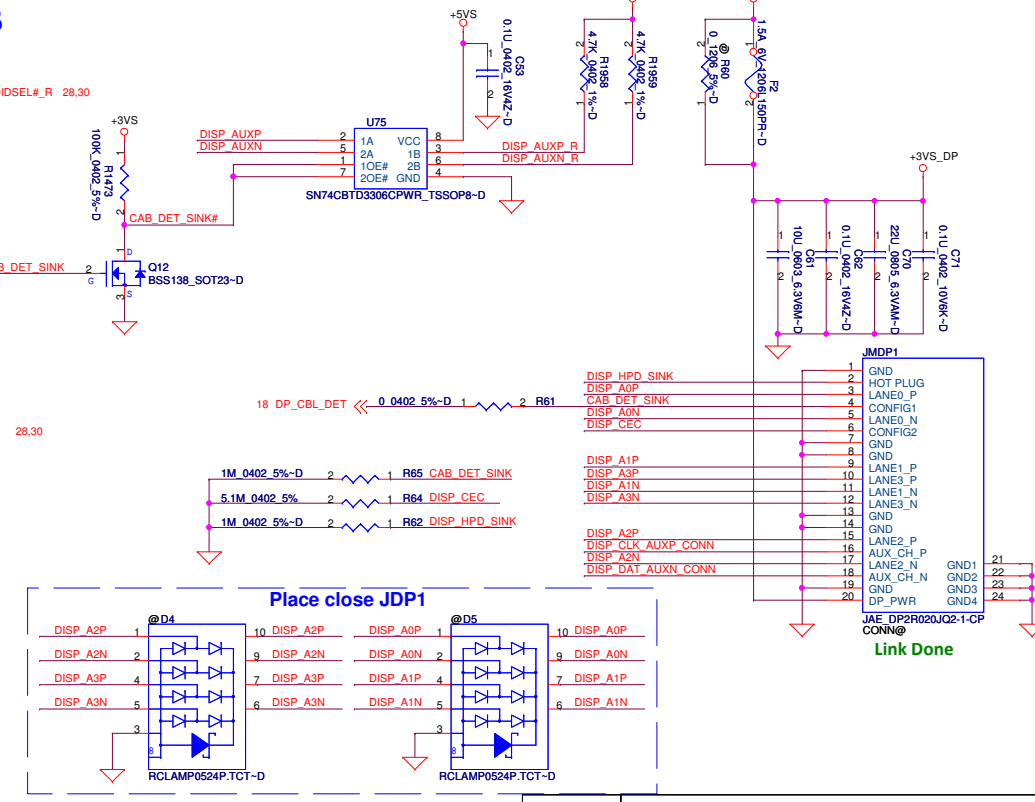
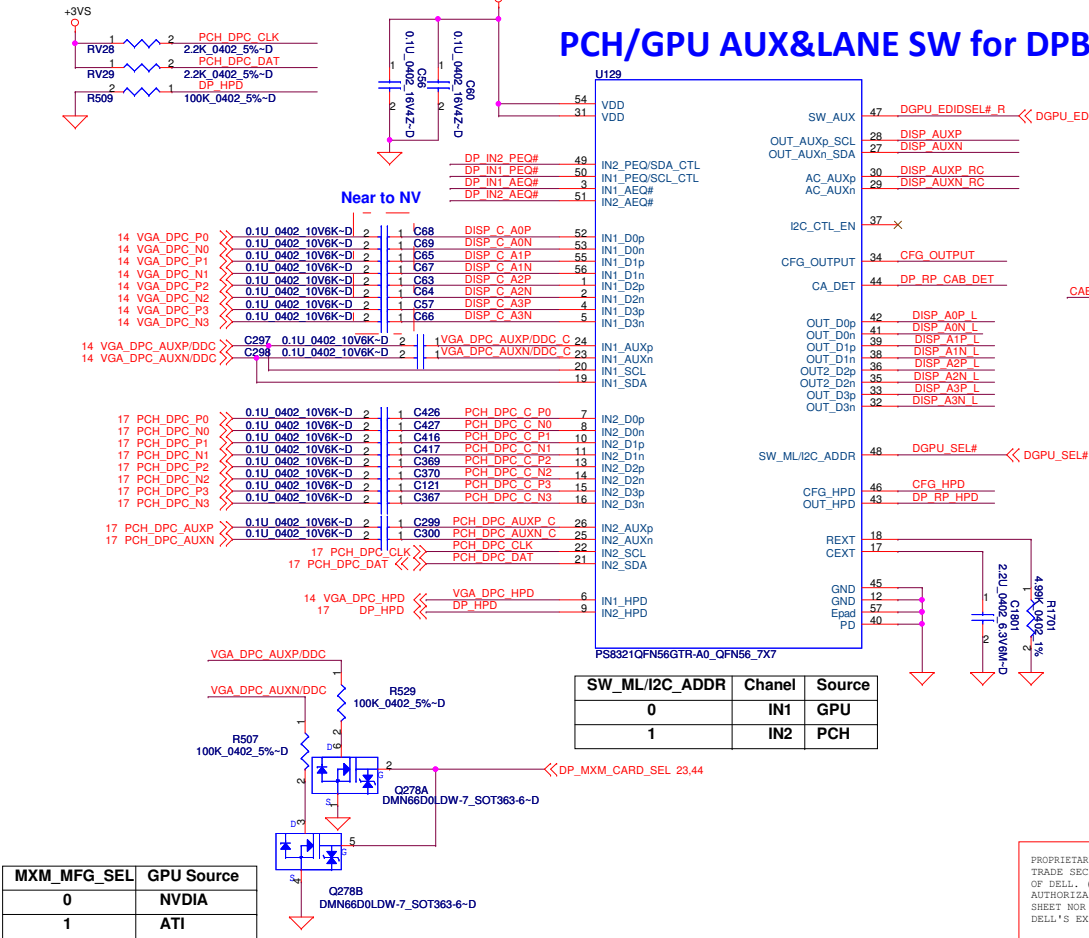
CFG_OUTPUT: output configuration
 L: Output is tracking DPCD register setting (auto interception)
 H: Output swing level fixed at 600mV and no pre-emphasis
 M: Output swing level is fixed at 400mV and no pre-emphasis

DP Redriver



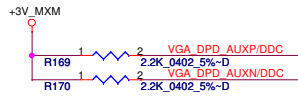
| SW_AUX | Chanel | Source |
|--------|--------|--------|
| 0 | IN1 | GPU |
| 1 | IN2 | PCH |

PCH/GPU AUX&LANE SW for DPB

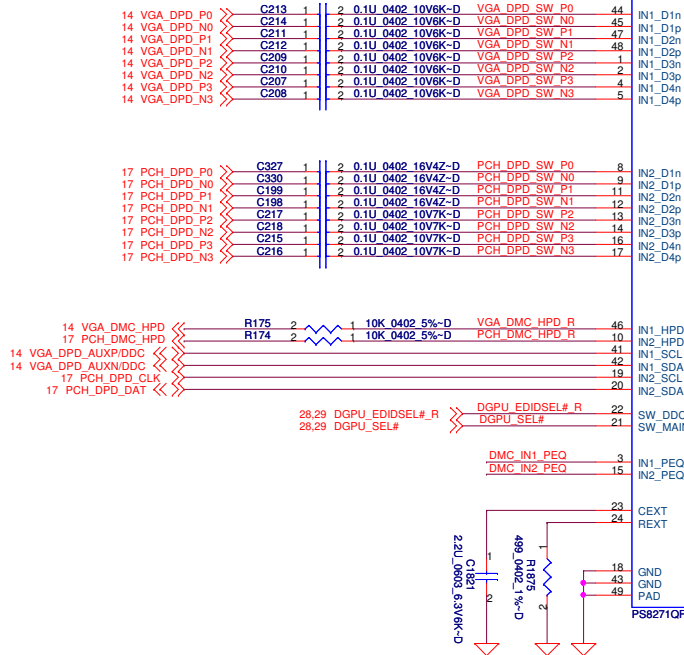


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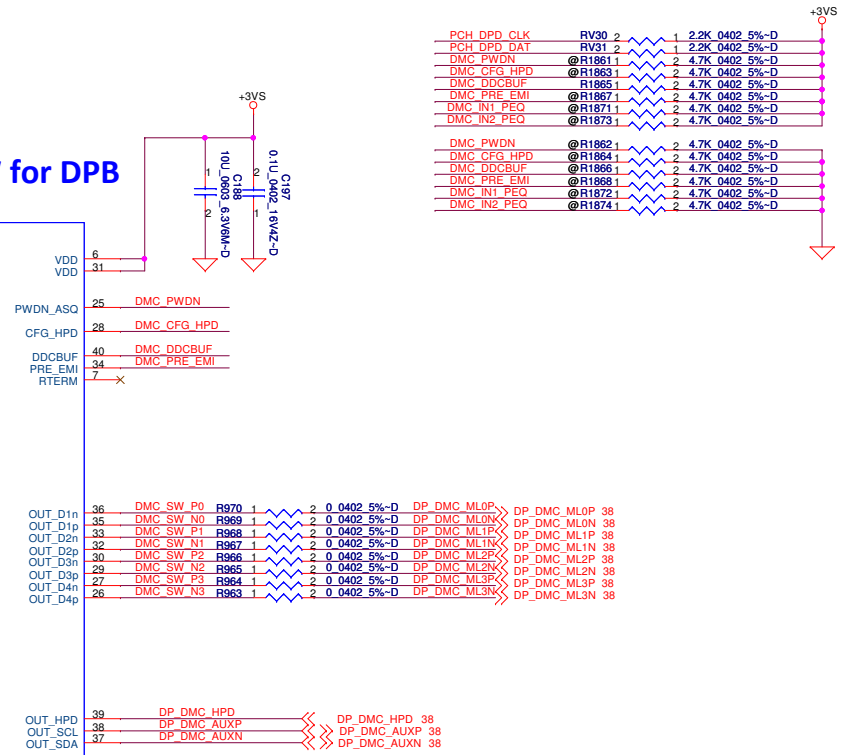




PCH/GPU AUX&LANE SW for DPB



| SEL | Y |
|-----|-----|
| 0 | IN1 |
| 1 | IN2 |

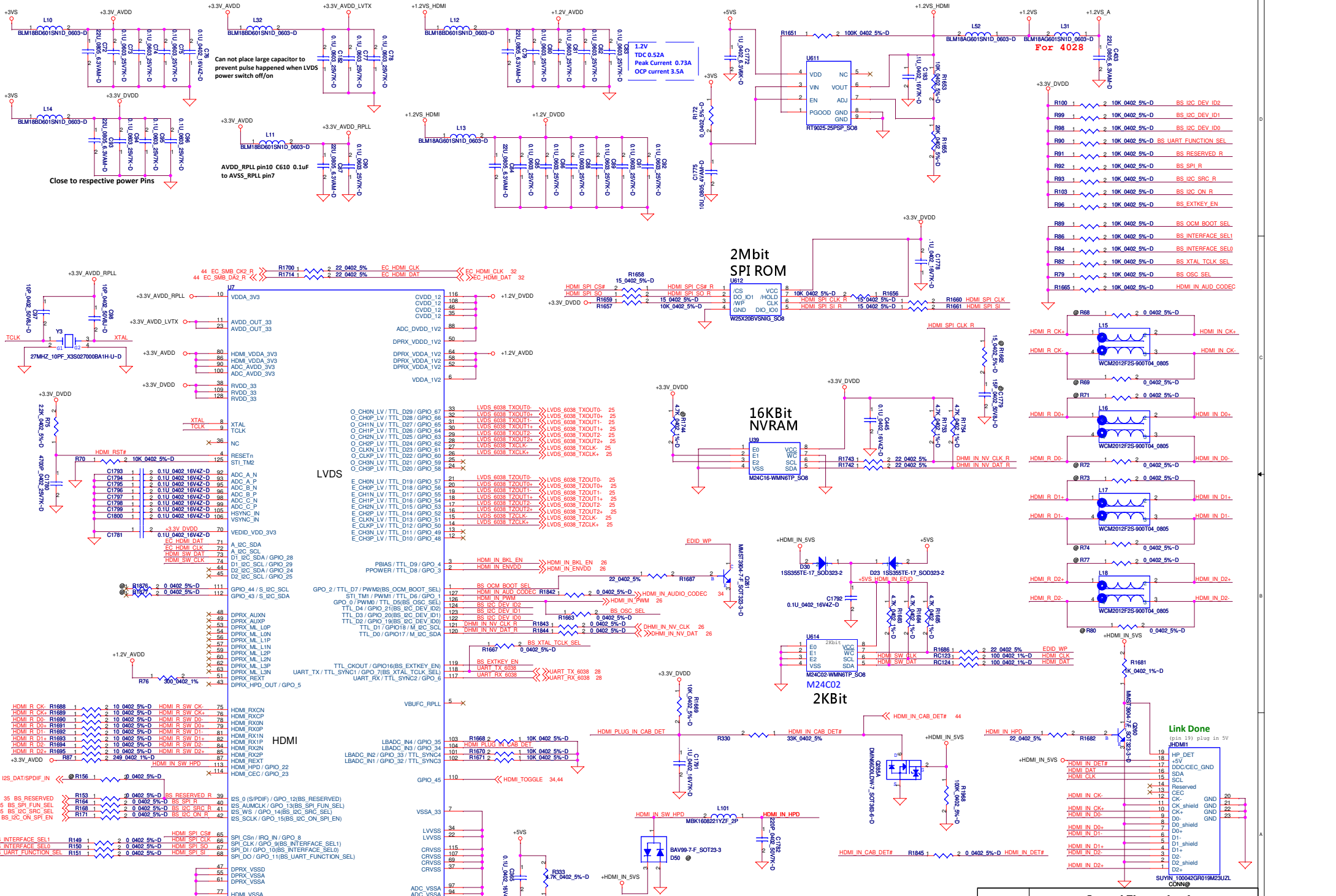


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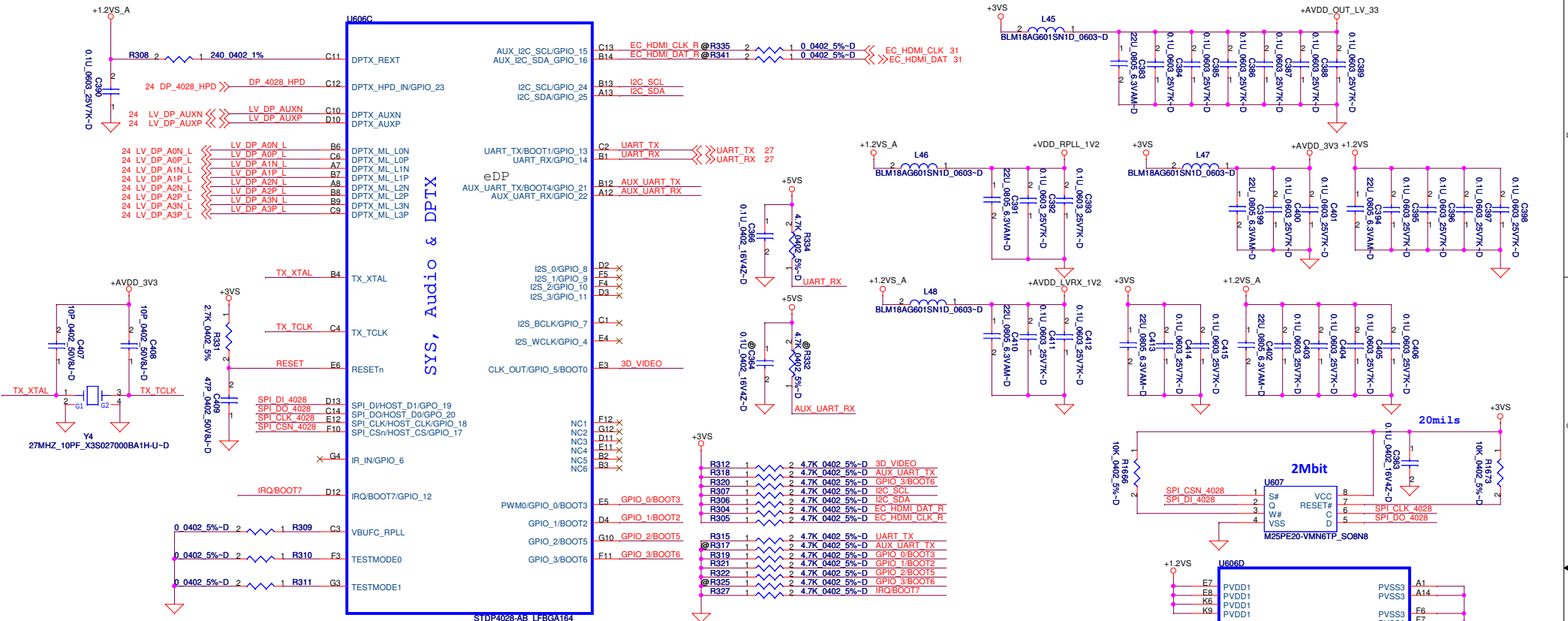
| | |
|---------------------------------|----------------------------|
| Compal Electronics, Inc. | |
| HDMI SW for DMC | |
| File | Rev 1.0 |
| Size | Document Number |
| LA-6601P | |
| Date: | Tuesday, November 30, 2010 |
| Sheet 30 of 63 | |

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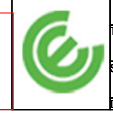


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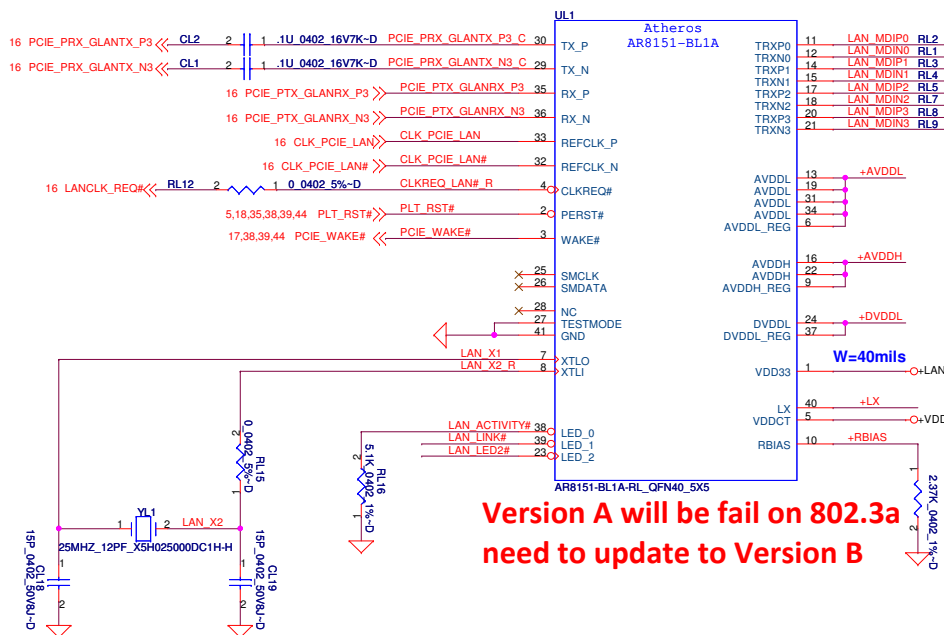
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|-------|----------------------------|---------------------------------|------------|
| | | Compal Electronics, Inc. | |
| | | HDMI input - STDP6038 | |
| File | Document Number | Size | Rev |
| | LA-6601P | | 1.0 |
| Date: | Tuesday, November 30, 2010 | Sheet | 31 of 63 |



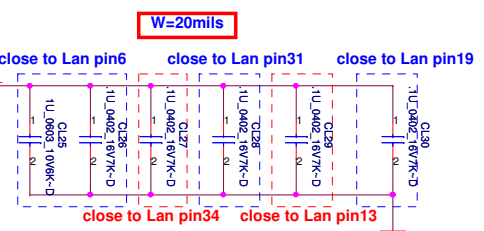
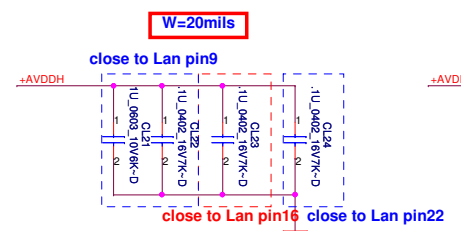
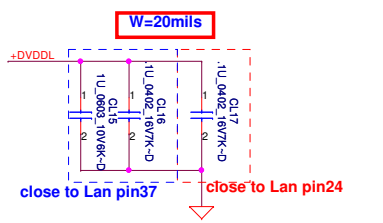
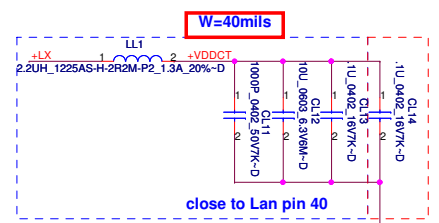
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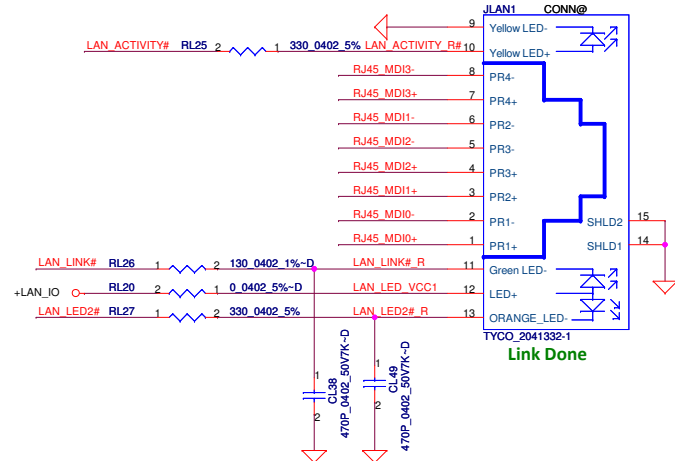
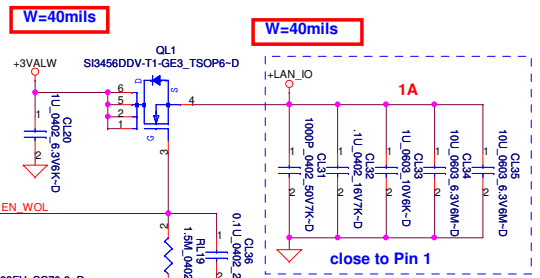
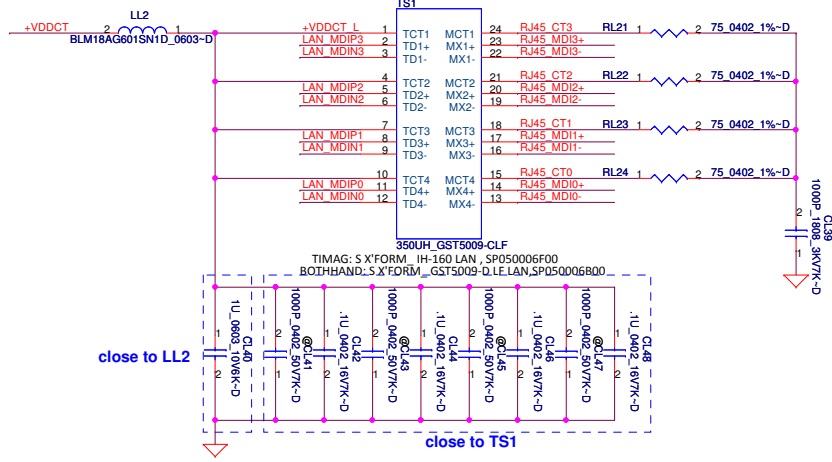
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| Compal Electronics, Inc. | | | |
| LVDS transfer eDP-STDP4028 | | | |
| Title | | Rev 1.0 | |
| Size | | Document Number | |
| | | LA-6601P | |
| Date: | Tuesday, November 30, 2010 | Sheet | 32 of 85 |



close to Lan chip 1000p reserved for EMI



Version A will be fail on 802.3a
need to update to Version B

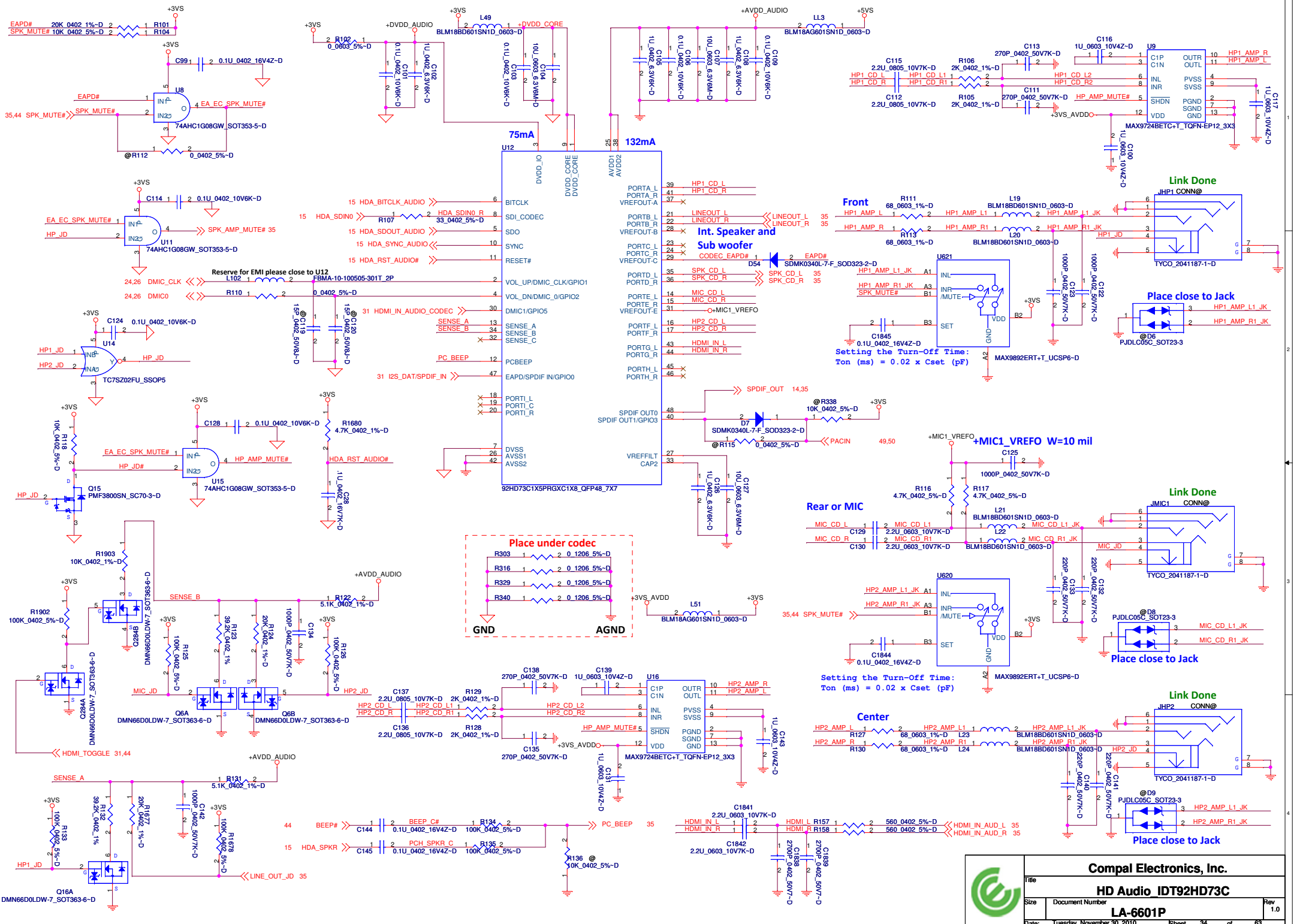


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|----------------------------------|----------------------------|------------|----------|
| Compal Electronics, Inc. | | | |
| Title GLAN AR8151 AL1A | | | |
| Size | Document Number | Rev | |
| | LA-6601P | 1.0 | |
| Date: | Tuesday, November 30, 2010 | Sheet | 33 of 63 |

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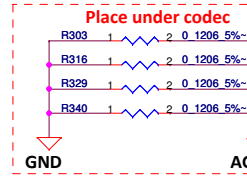
75mA
132mA

Int. Speaker and Subwoofer

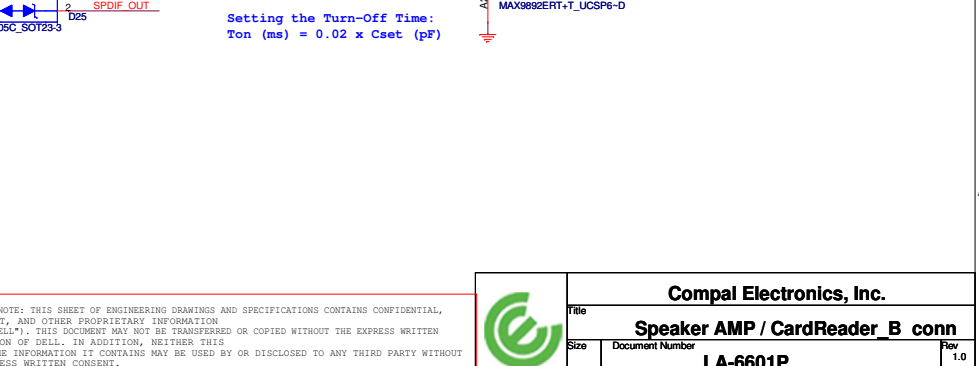
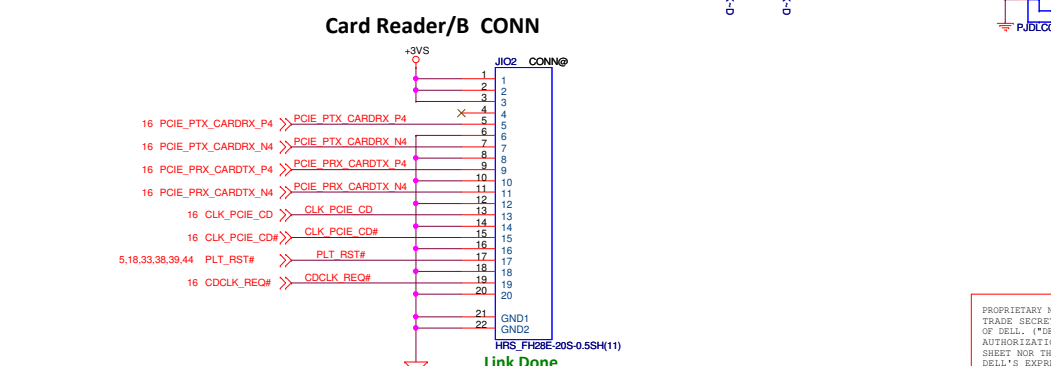
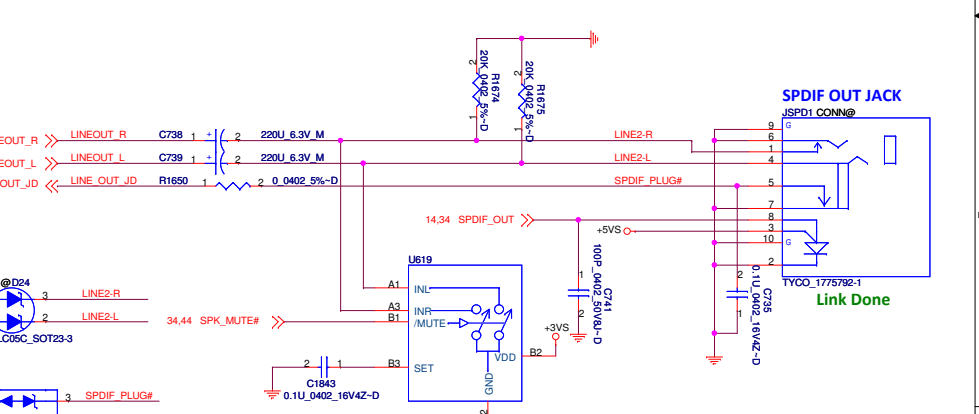
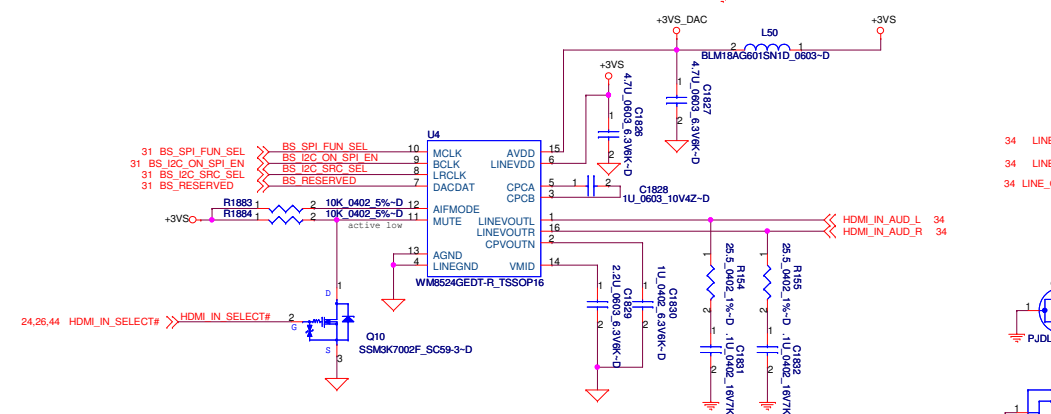
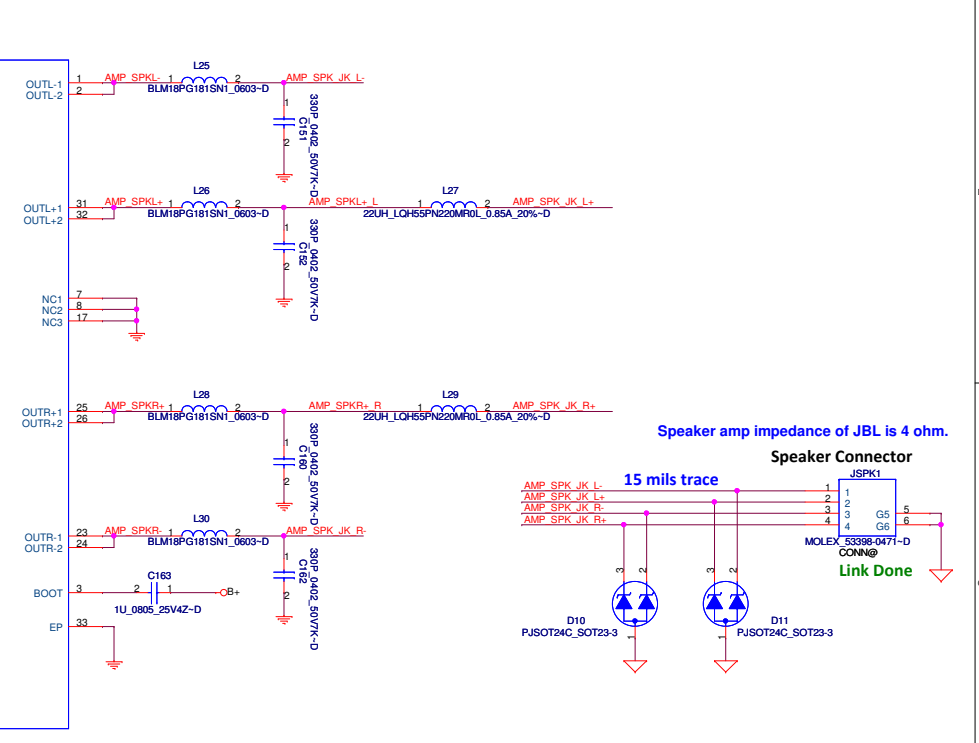
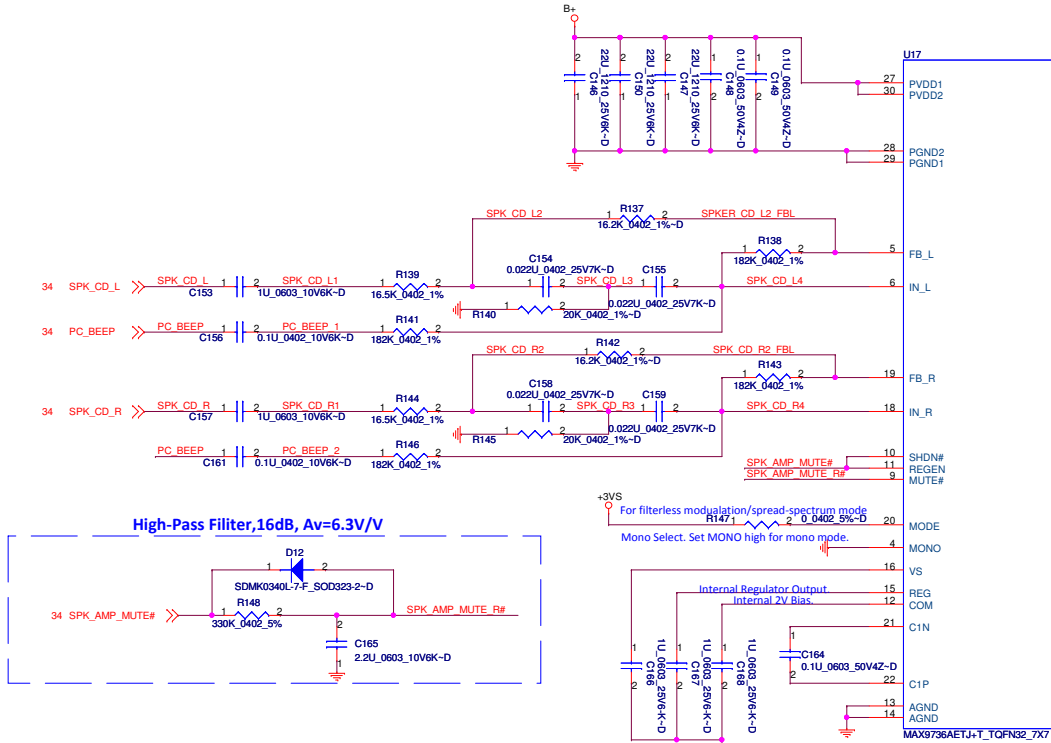
Front

Rear or MIC

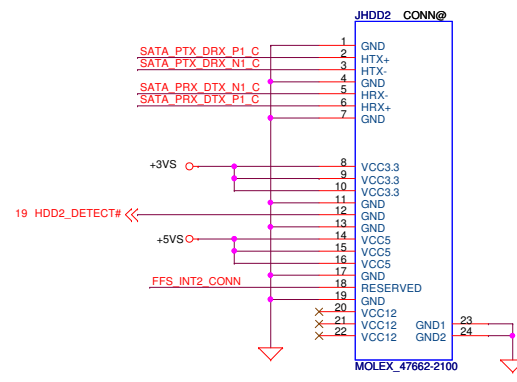
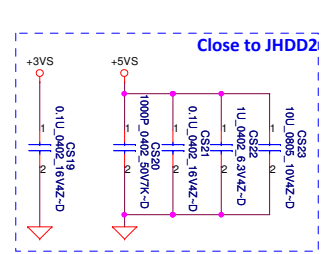
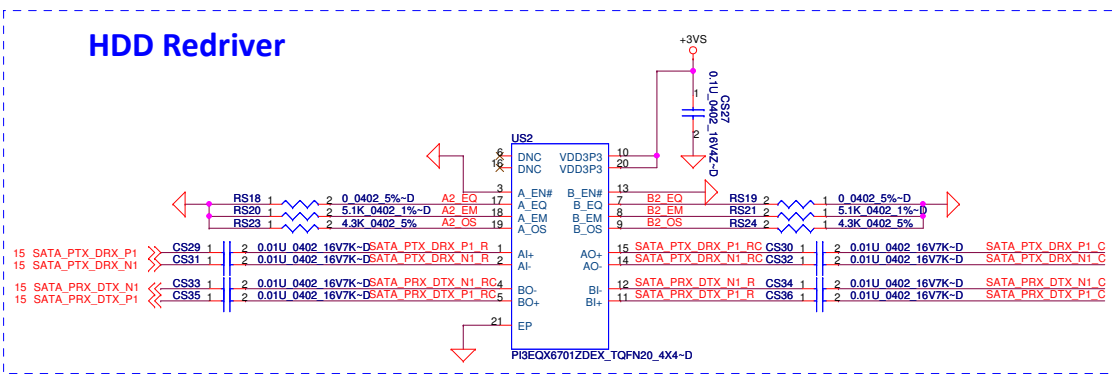
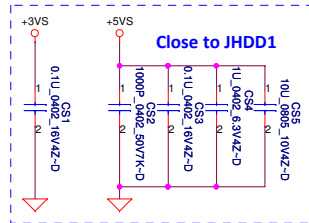
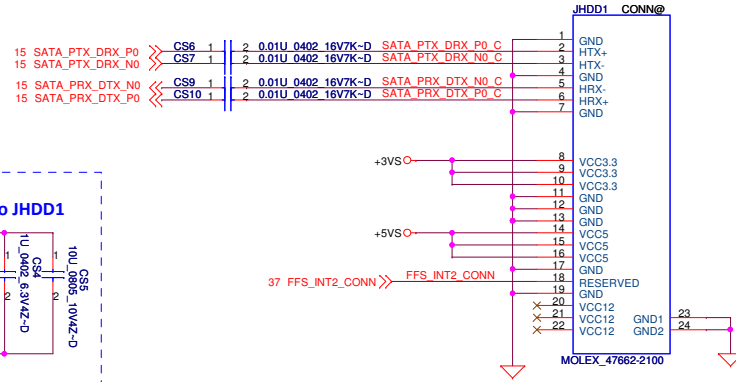
Center



| | | | | | |
|-------|----------------------------|-----------------|-----------------|---------------------------------|------------|
| | | | | Compal Electronics, Inc. | |
| | | | | HD Audio IDT92HD73C | |
| File | Size | Document Number | LA-6601P | | Rev 1.0 |
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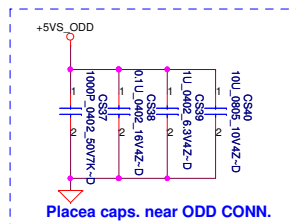
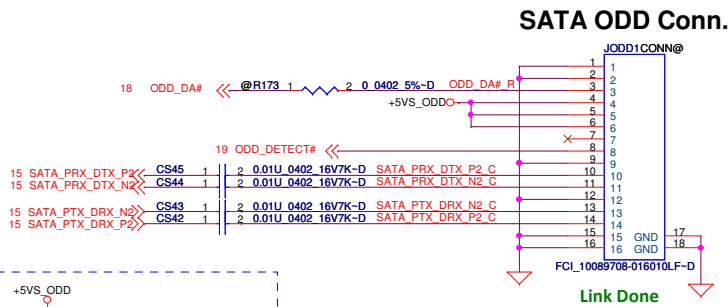
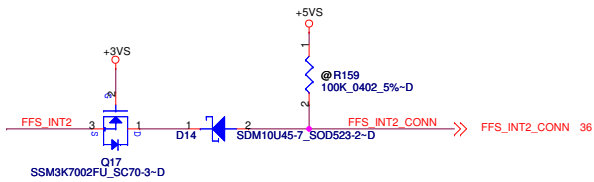
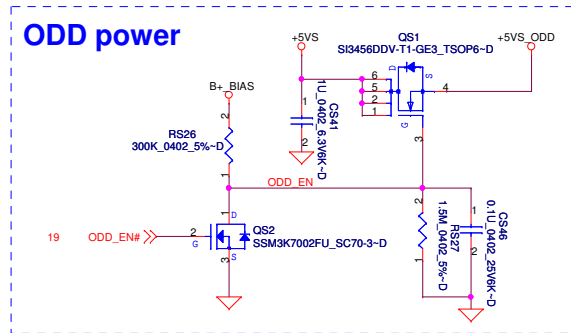
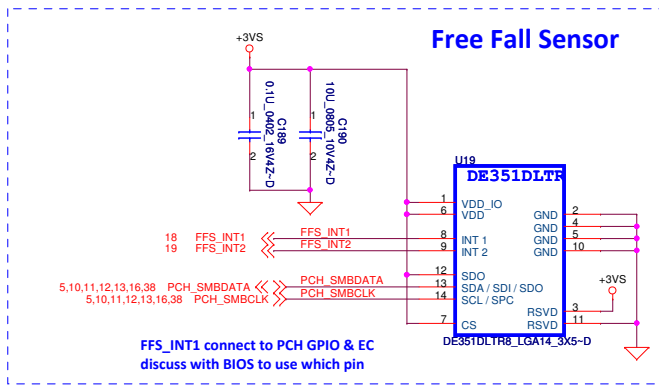
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Compal Electronics, Inc.



| | | | | | |
|-------|----------------------------|--------|------------------|----|----|
| Title | | | SATA HDD1 & HDD2 | | |
| Size | Document Number | Rev | | | |
| | LA-6601P | 1.0 | | | |
| Date: | Tuesday, November 30, 2010 | Esheet | 36 | of | 63 |

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SATA HDD3 & ODD & FFS

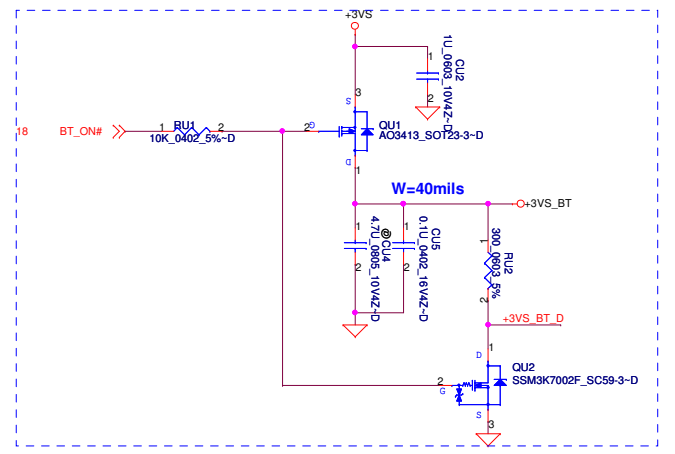
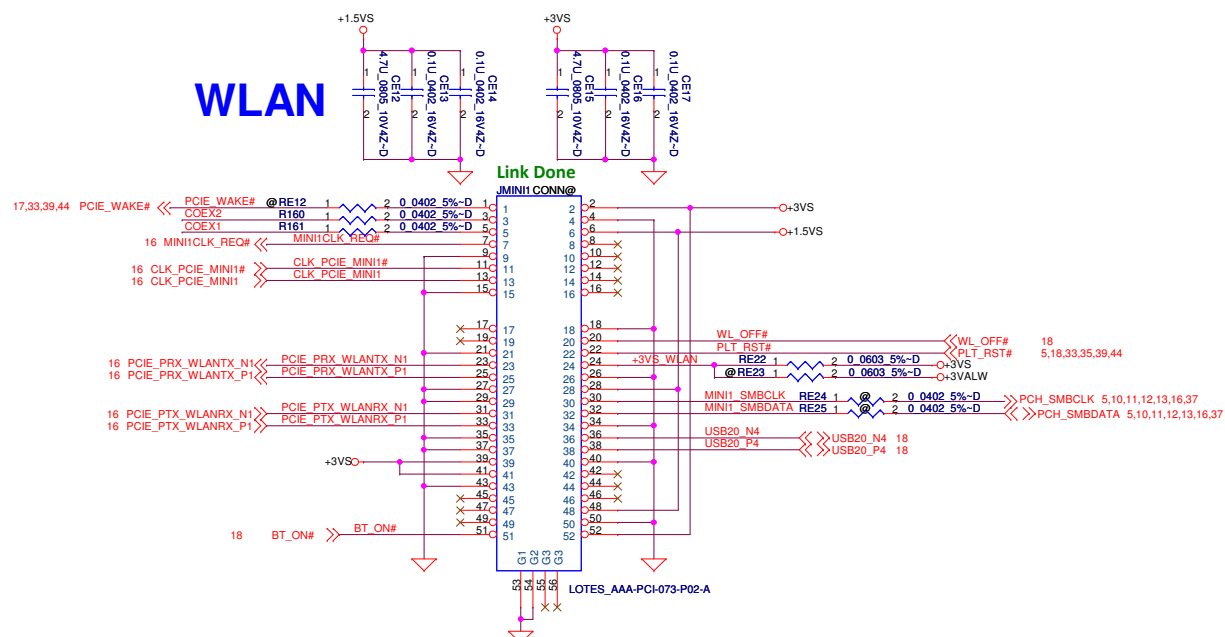
LA-6601P

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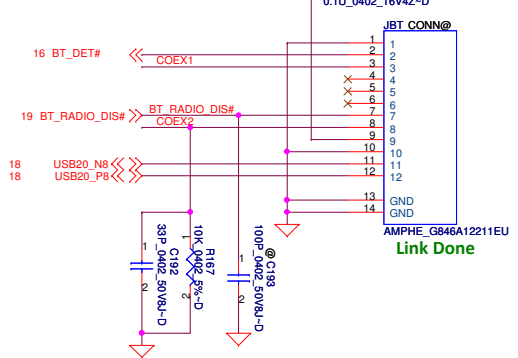


Rev 1.0

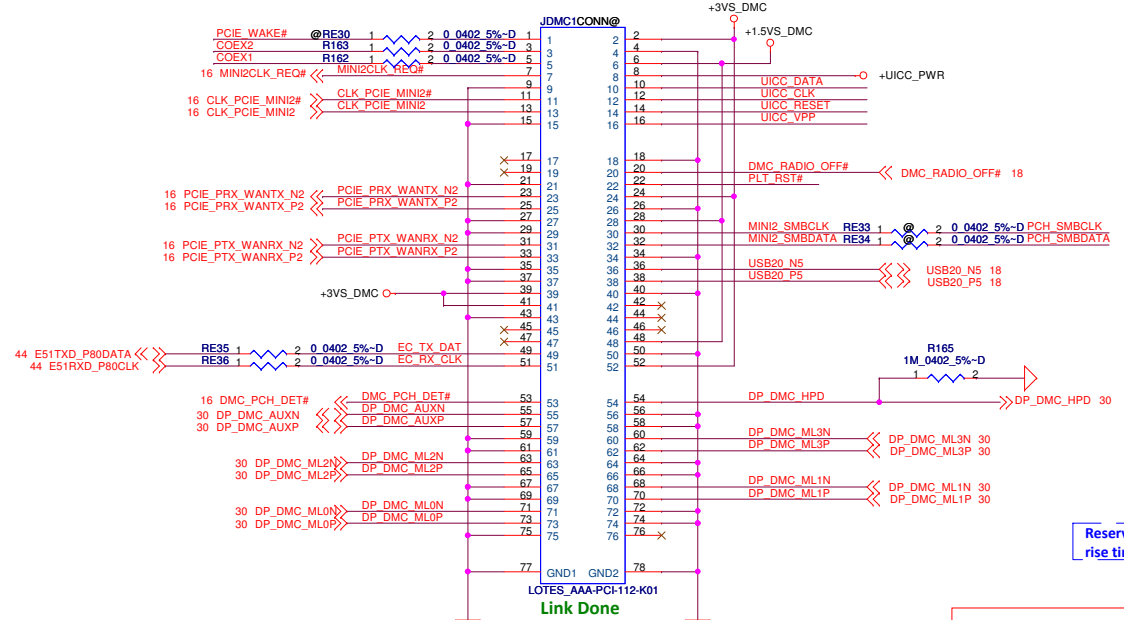
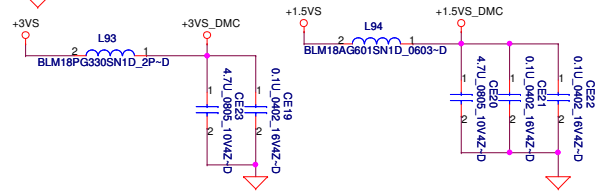
WLAN



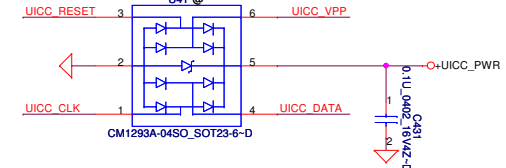
Bluetooth



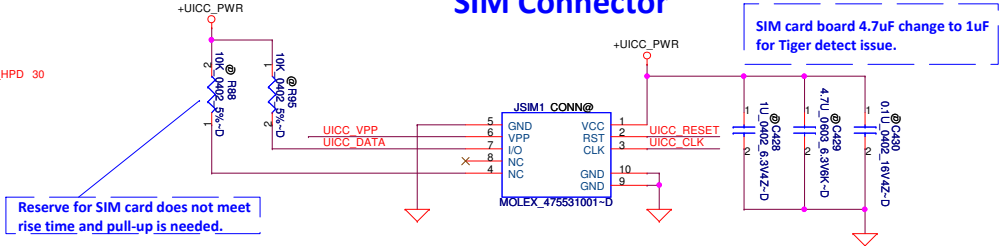
Display Mini Card (DMC)



For ESD Cap close to JSIM1



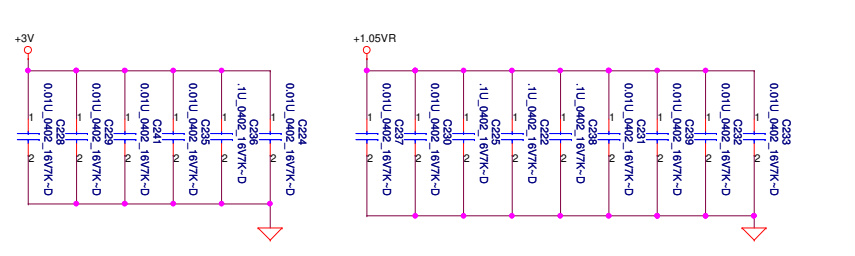
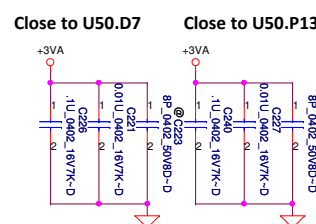
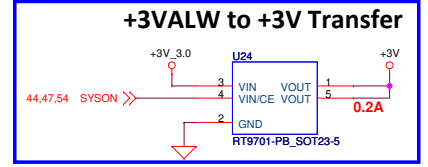
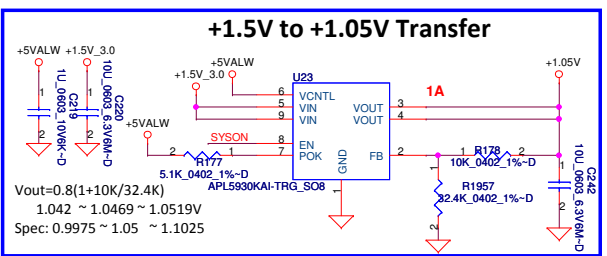
SIM Connector



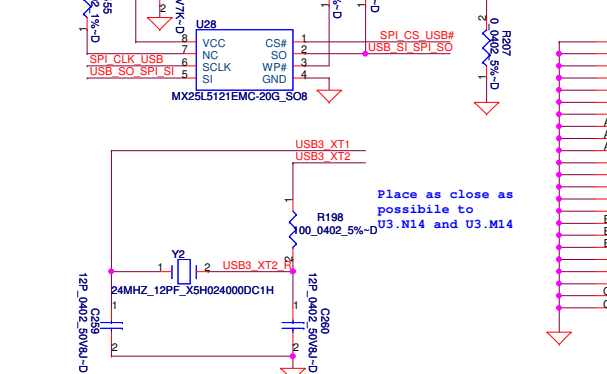
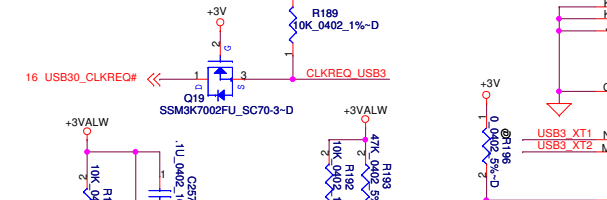
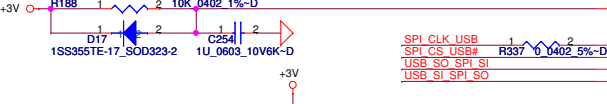
Reserve for SIM card does not meet rise time and pull-up is needed.

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| | | | |
|-------|----------------------------|----------------------------------|----------|
| | | Compal Electronics, Inc. | |
| | | Mini Card WLAN / DMC / BT | |
| File | LA-6601P | | Rev 1.0 |
| Size | Document Number | | |
| Date: | Tuesday, November 30, 2010 | Sheet | 38 of 63 |



- 16 CLK_PCIE_USB30 >> CLK_PCIE_USB30 B2
- 16 CLK_PCIE_USB30# >> CLK_PCIE_USB30# B1
- 16 PCIE_PRX_USB3TX_P6 >> C246 1 2 1U_0402 16V7K-D PCIE_PRX_USB3TX_C_P6 D2
- 16 PCIE_PRX_USB3TX_N6 >> C250 1 2 1U_0402 16V7K-D PCIE_PRX_USB3TX_C_N6 D1
- 16 PCIE_PTX_USB3RX_P6 >> PCIE_PTX_USB3RX_P6 F2
- 16 PCIE_PTX_USB3RX_N6 >> PCIE_PTX_USB3RX_N6 F1



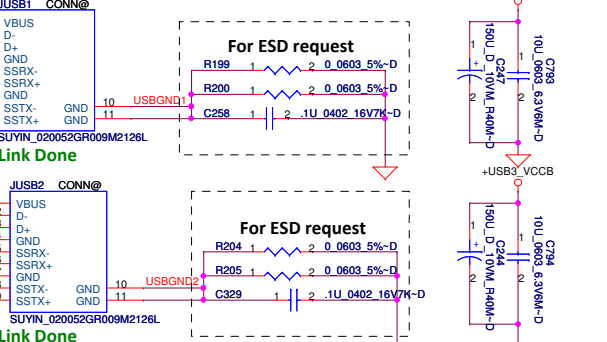
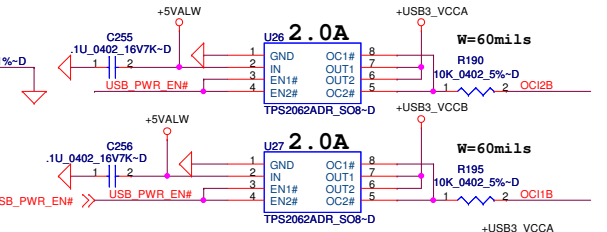
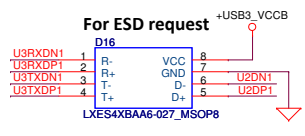
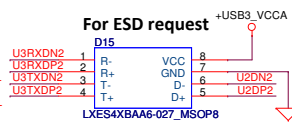
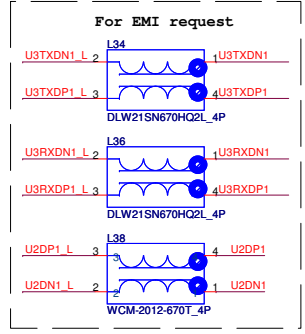
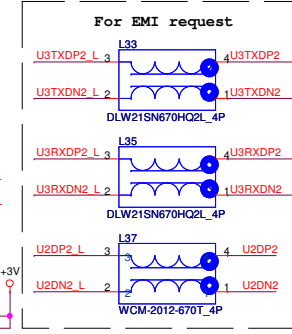
SPEC Max: +3V---200mA; +1.05V---800mA
Idle mode: 0.489W;
+3V---43mA; +1.05V---328mA
D3 mode: 0.066W
+3V---5.4mA; +1.05V---45mA

Can be attach to EC, either.

PCI Express/ExpressCard select signal
 1: others
 0: Express Card or Mini card

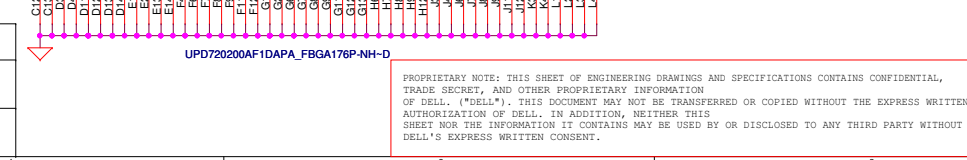
As short as possible

P/N: SA00048H0L (S IC UPD72020AF1-DAP-A FBGA 176P USB3.0)
 A version 8/11 update



Pin compare table for support USB remote wakeup or not

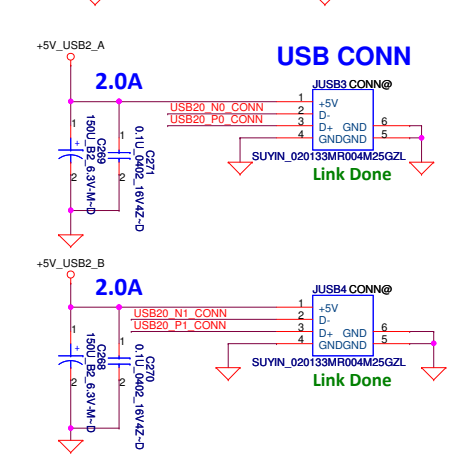
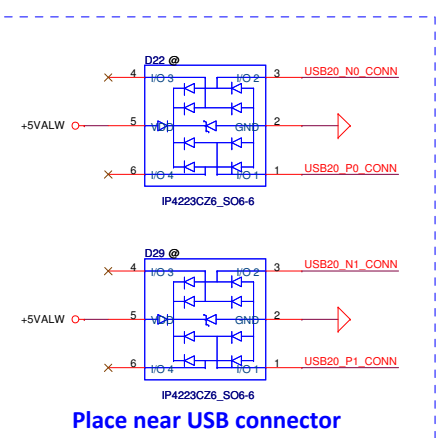
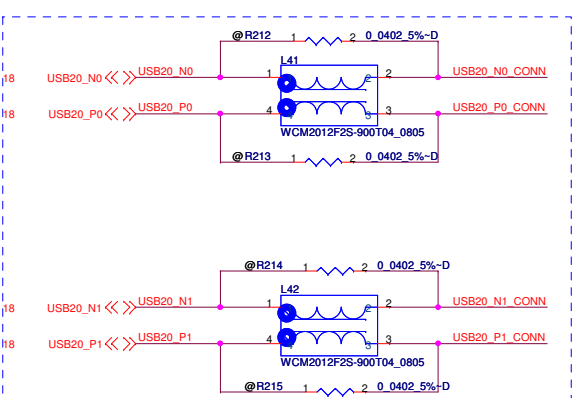
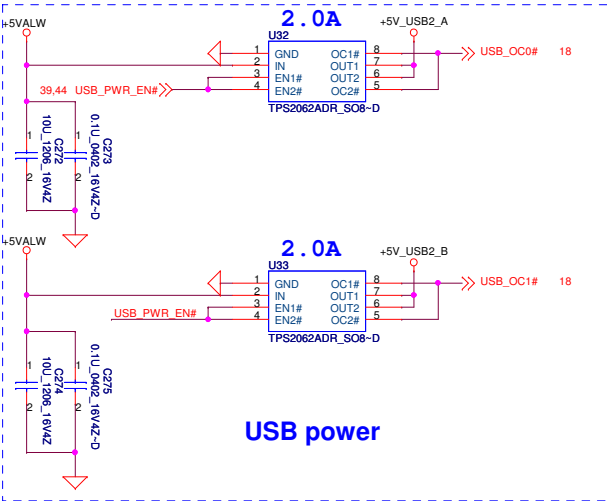
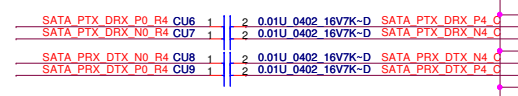
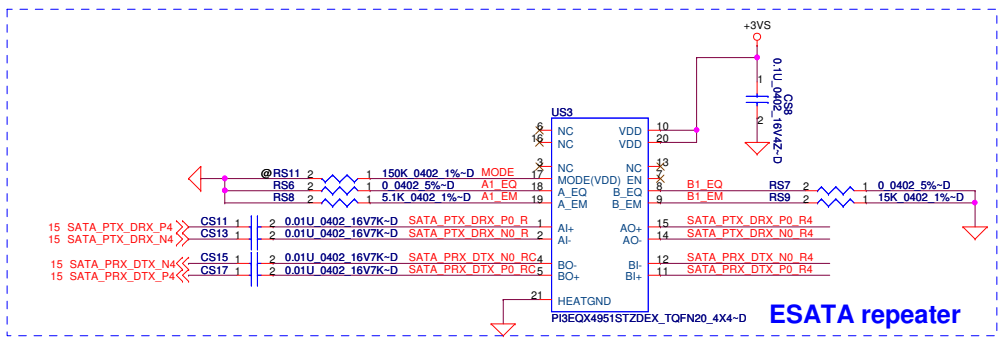
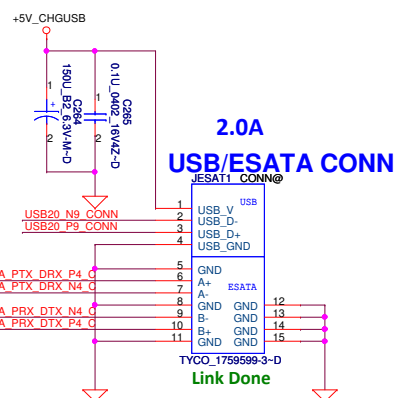
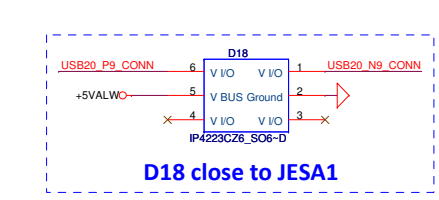
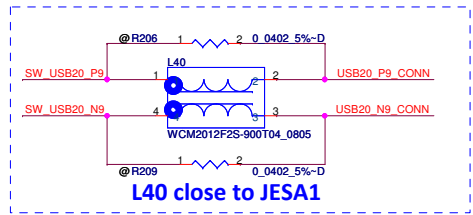
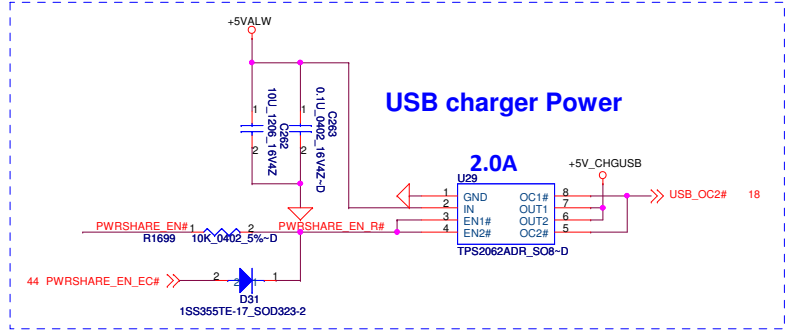
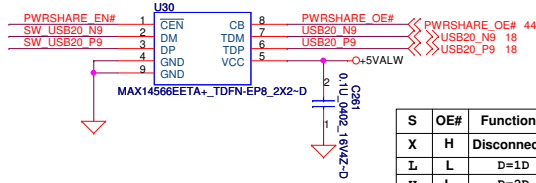
| | AUXDET(Pin J2) | CSEL(Pin P6) | CLK |
|-------------------------------|------------------------|--------------------|---|
| Support USB remote wakeup | pull high 10k to VDD33 | Tied to GND | Must use 24MHz crystal: mount Y1,R19,C40,C41 |
| Not support USB remote wakeup | Tied to GND | pull high to VDD33 | Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25 |



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USB3.0 PD720200
LA-6601P
 Date: Tuesday, November 30, 2010 Sheet 39 of 63

Power share



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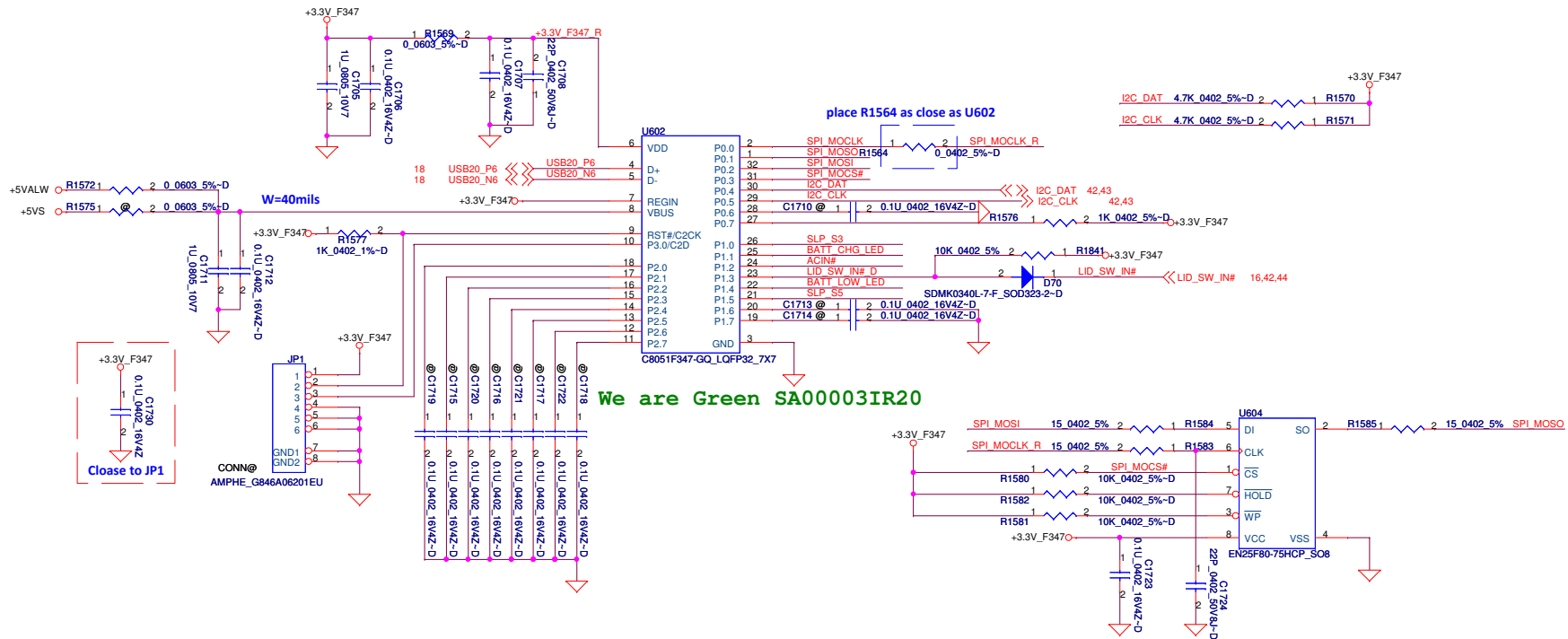
Compal Electronics, Inc.

USB/ESATA TS3USB221RSER

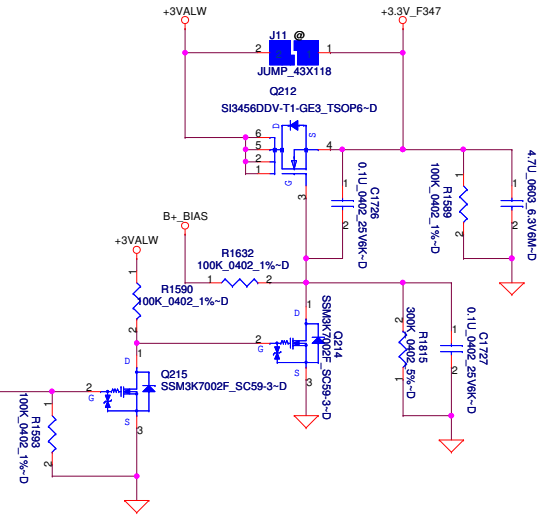
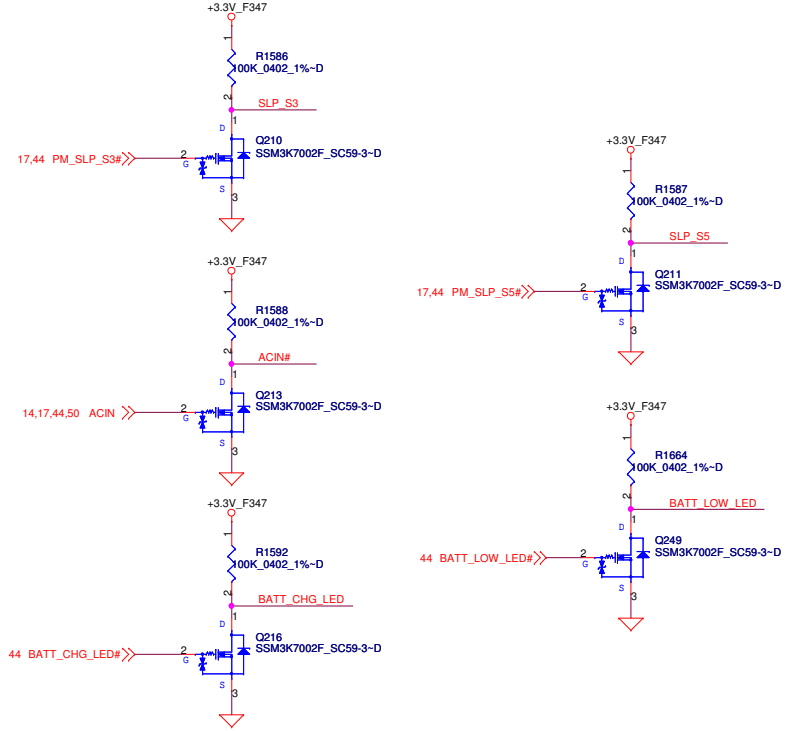
LA-6601P

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| DEVICE | SMBUS ADDRESS |
|--------------|---------------|
| MAXIM - LED | 0100 000b |
| MAXIM - GPIO | 0100 001b |
| I2C EEPROM | 1010 000b |



+3.3V_F347 behavior

| | | | | |
|----------|----|----|-----|-----|
| STATE | S0 | S3 | S4 | S5 |
| | ON | ON | ON | ON |
| AC IN | ON | ON | OFF | OFF |
| BAT only | ON | ON | OFF | OFF |

AC mode battery full in S5: turn off ELC controller

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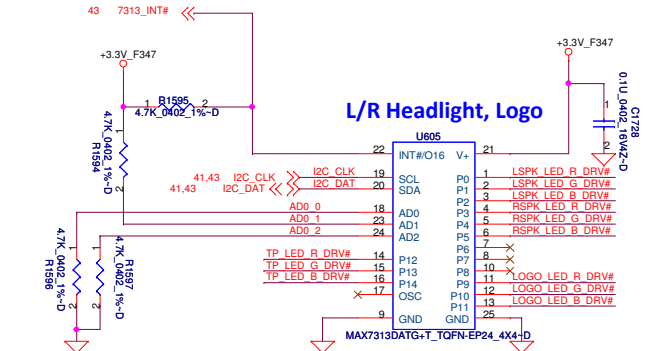
Title: ELC (1)

Size: Document Number LA-6601P

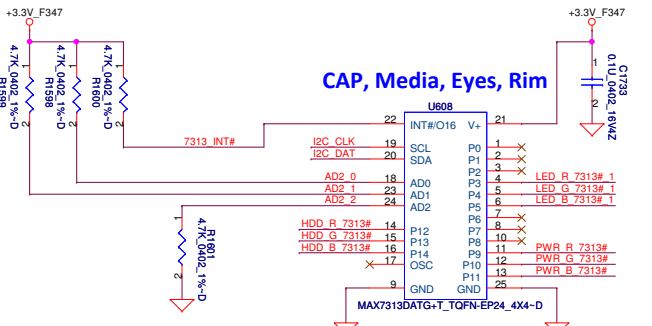
Date: Tuesday, November 30, 2010

Sheet 41 of 85

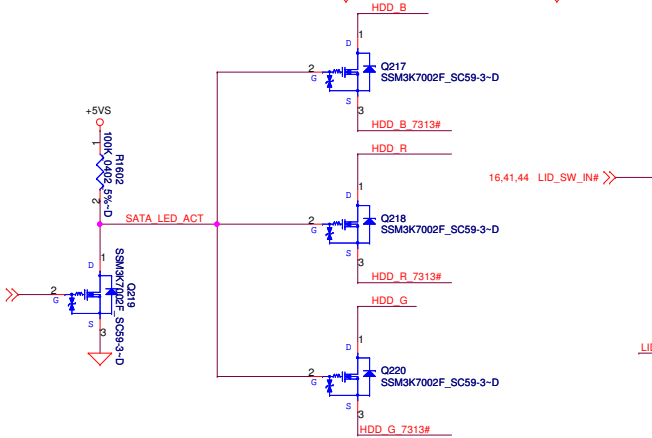
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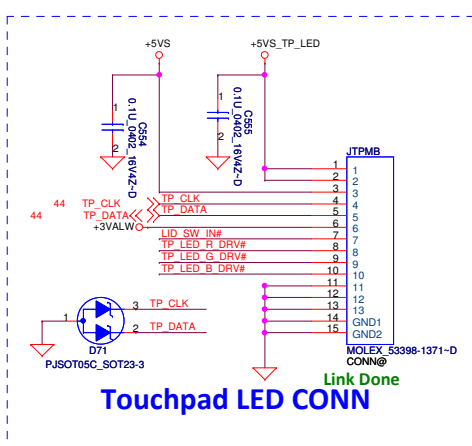
L/R Headlight, Logo



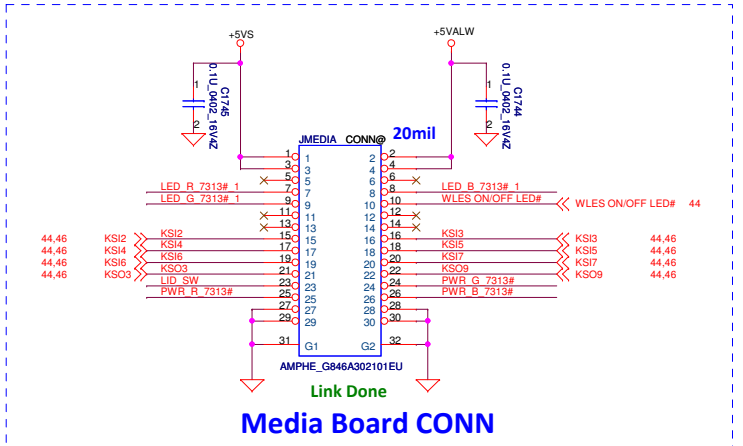
CAP, Media, Eyes, Rim



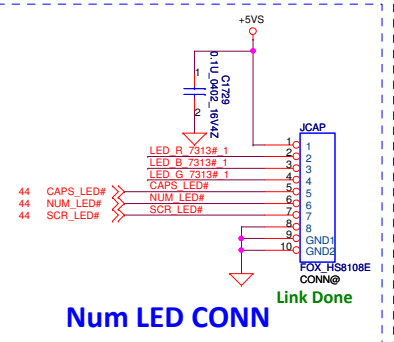
| Reference | AD2 | AD1 | AD0 | MAX7313 |
|-----------|-----|-----|-----|--|
| U605 | 0 | 1 | 0 | L/R Headlight , Logo, TP |
| U608 | 0 | 1 | 1 | Num, CAP , SCR EJECT, REV, PLAY/PAUSE FFWD, Vol_DWN, Vol_UP Wireless ON/OFF AWCC Button Alien Adrenaline Power Button Eyes Power Button Rim |



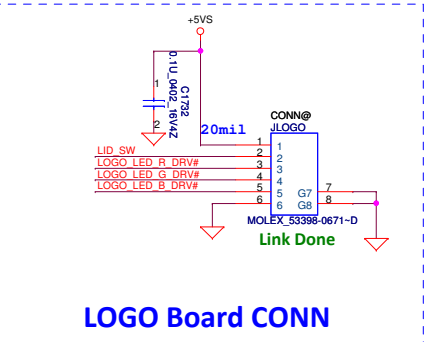
Touchpad LED CONN



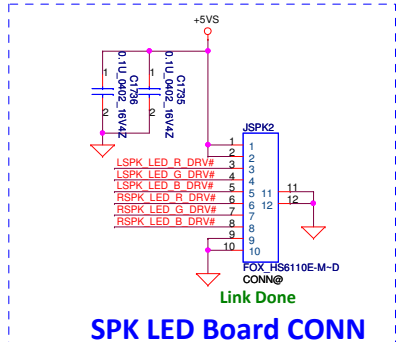
Media Board CONN



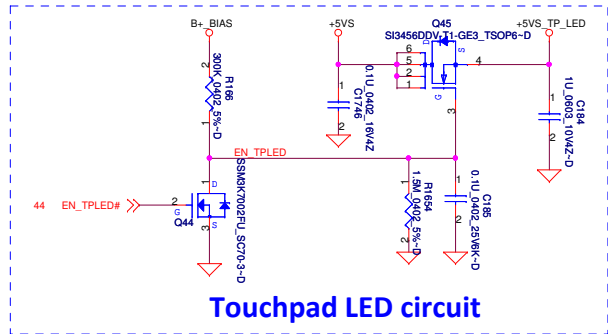
Num LED CONN



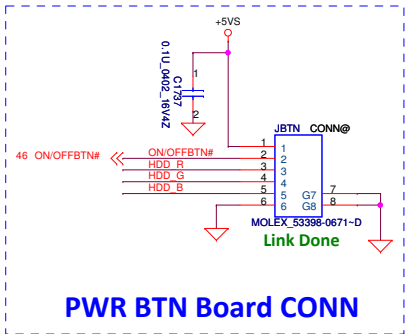
LOGO Board CONN



SPK LED Board CONN



Touchpad LED circuit



PWR BTN Board CONN

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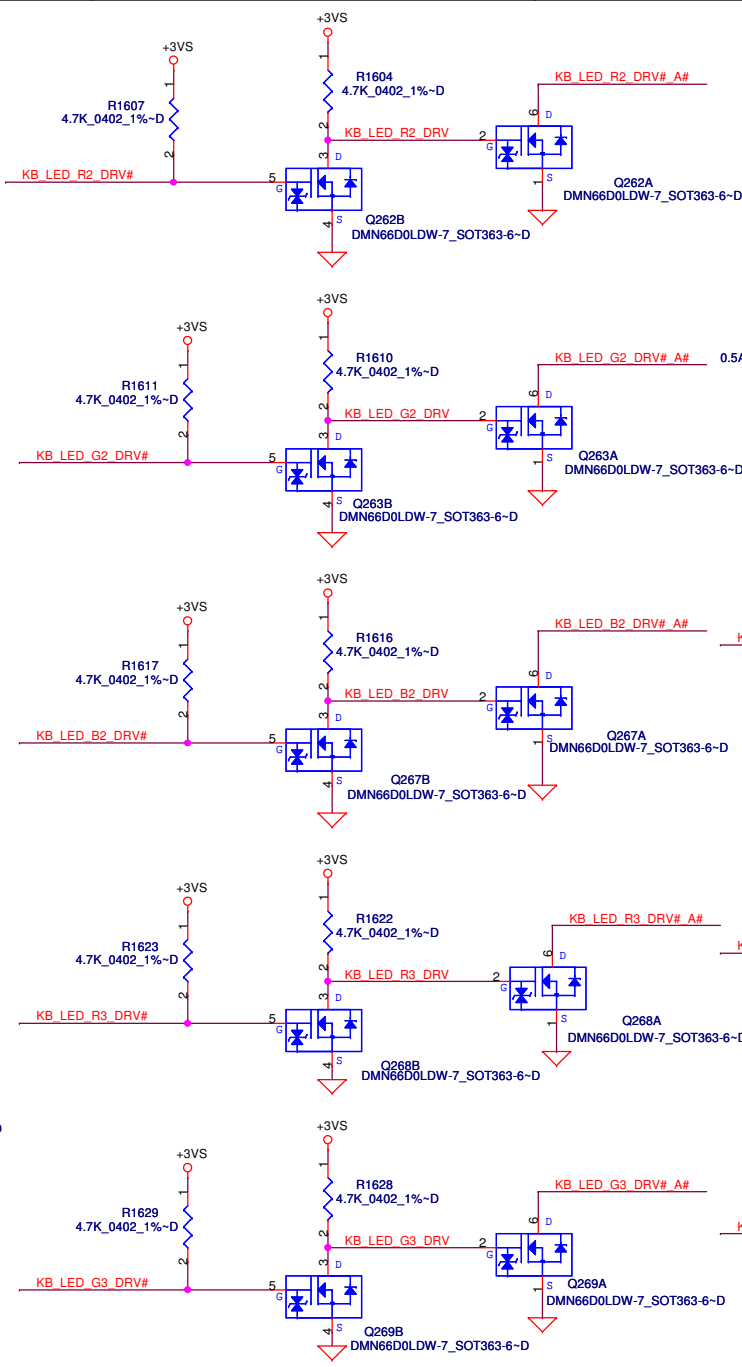
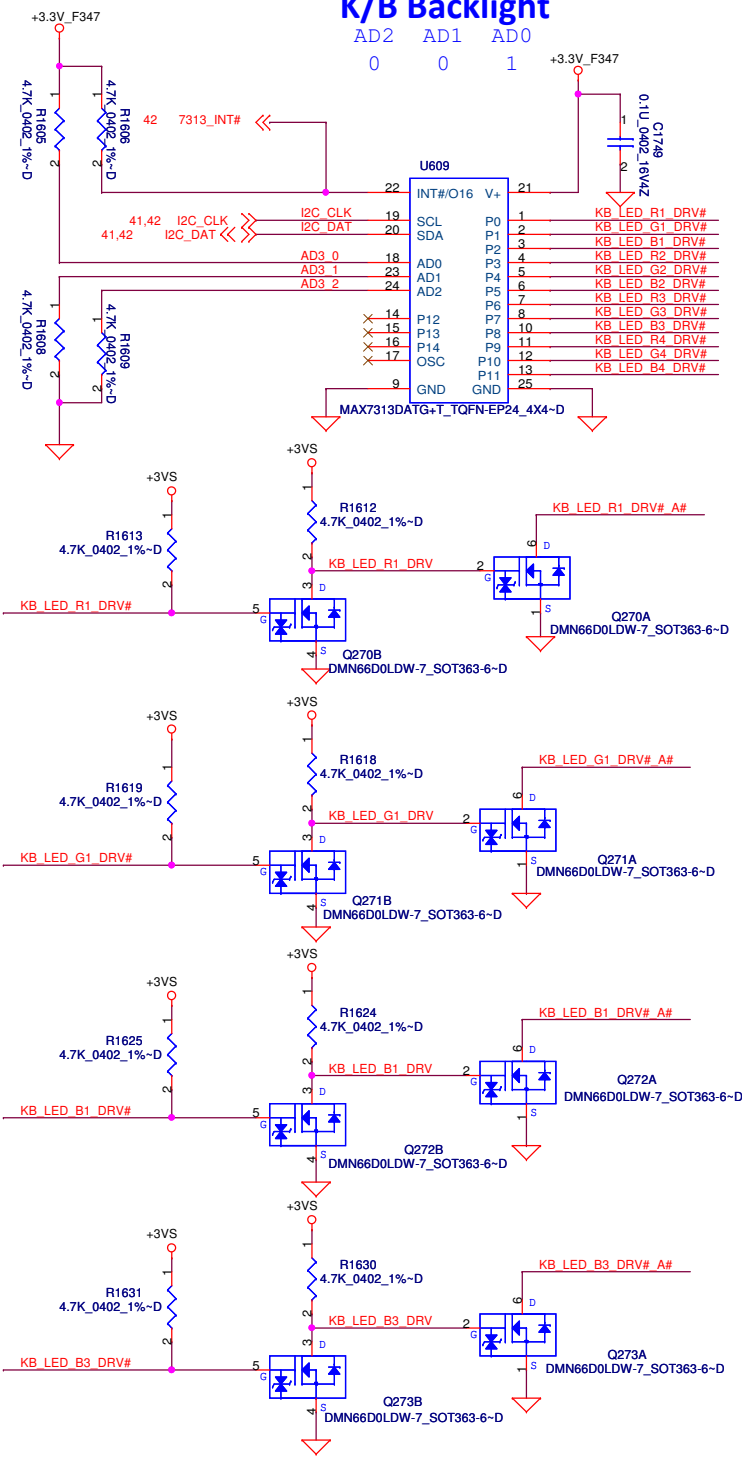
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Size: Document Number **LA-6601P** Rev **1.0**

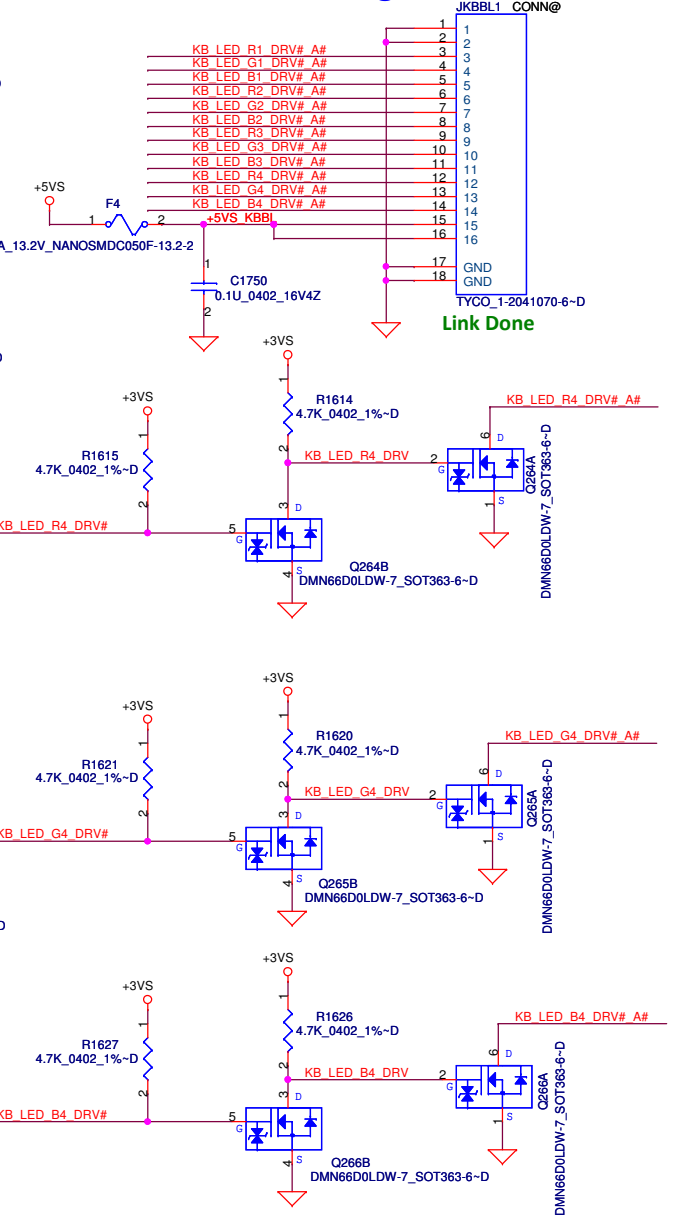
Date: **Tuesday, November 30, 2010** Sheet **42** of **63**

K/B Backlight

AD2 AD1 AD0
0 0 1




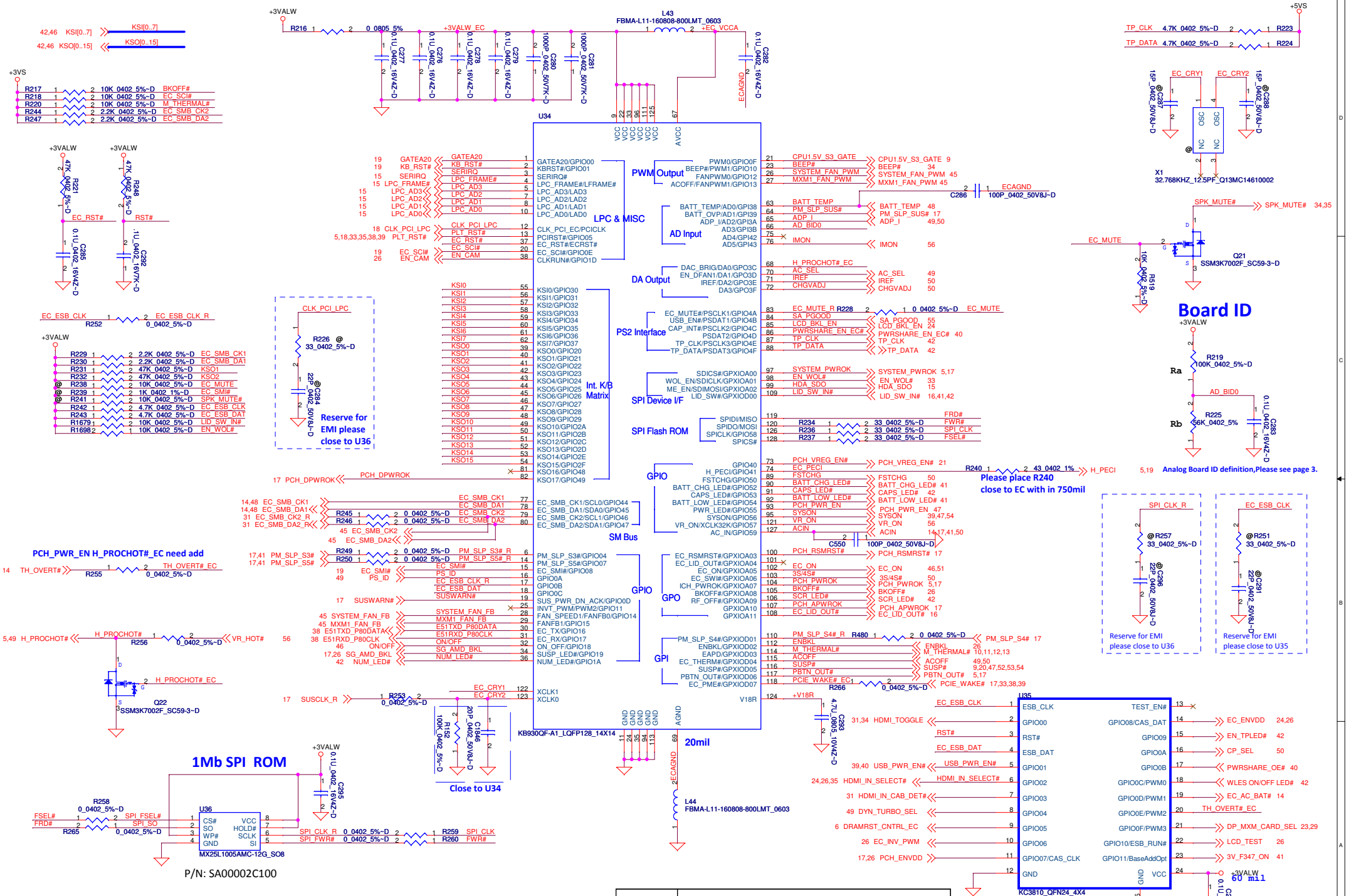
K/B Backlight CONN



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| | | | |
|---|----------------------------|---------------------------------|----------|
|  | | Compal Electronics, Inc. | |
| | | ELC (3) | |
| Size | Document Number | Rev | |
| | LA-6601P | 1.0 | |
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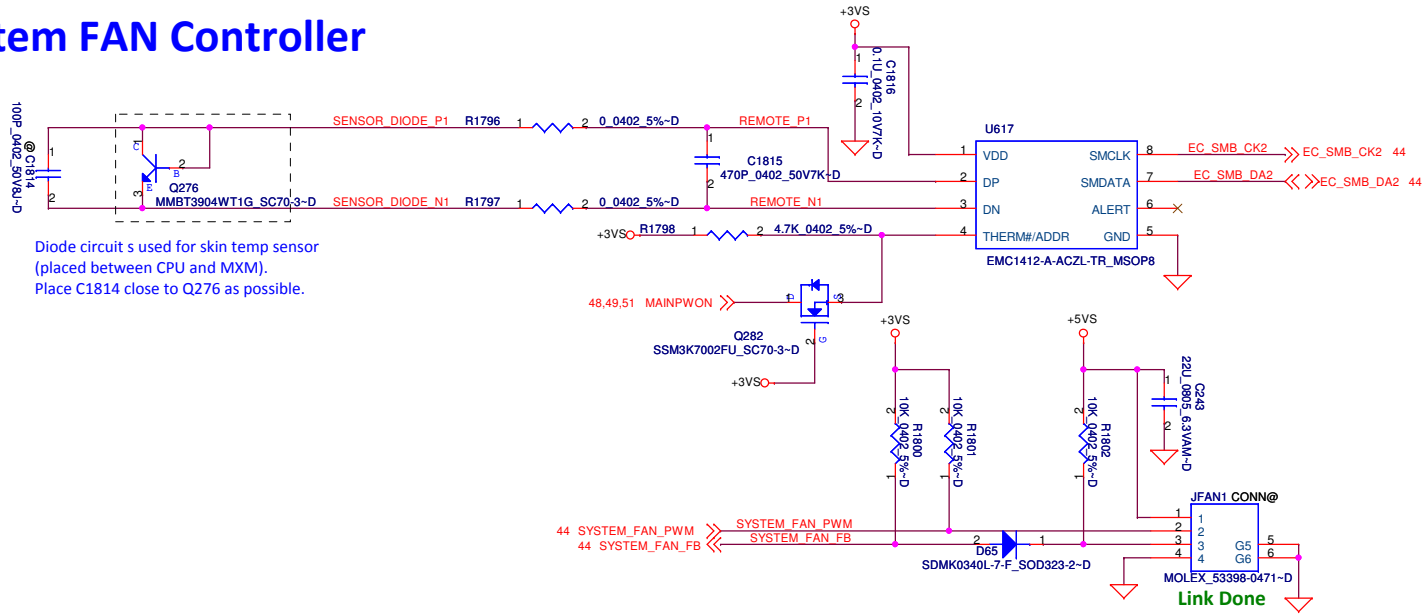
EC ENE-KB930

LA-6601P

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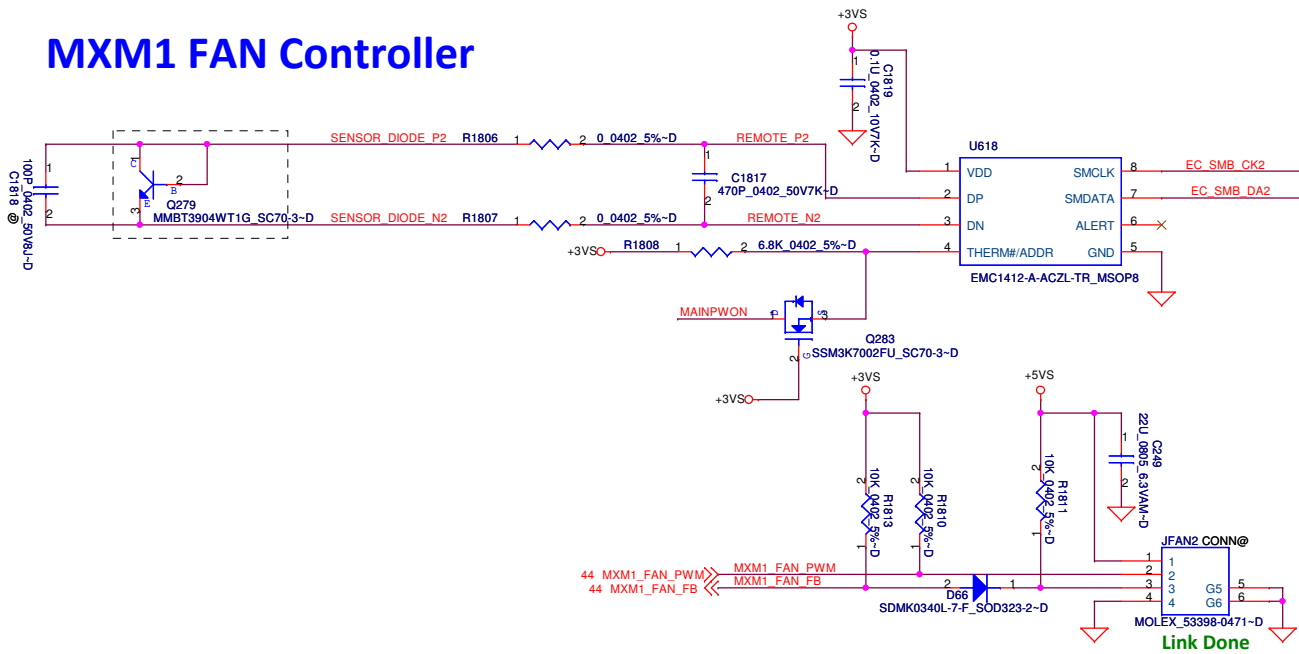
| | | | |
|----|------------------|----|------------------|
| 1 | ESB_CLK | 13 | TEST_EN# |
| 2 | GPI00 | 14 | EC_ENVDD |
| 3 | RST# | 15 | EN_TPLED# |
| 4 | ESB_DAT | 16 | GPI0A |
| 5 | USB_PWR_EN# | 17 | CP_SEL |
| 6 | HDMI_IN_SELECT# | 18 | PWRSHARE_OE# |
| 7 | HDMI_IN_CAB_DET# | 19 | WLES_ON/OFF_LED# |
| 8 | DYN_TURBO_SEL | 20 | AC_BAT# |
| 9 | DRAMRST_CNTRL_EC | 21 | TH_OVRT#_EC |
| 10 | EC_INV_WPM | 22 | DP_MXM_CARD_SEL |
| 11 | PCIE_WAKE#_EC1 | 23 | LCD_TEST |
| 12 | GND | 24 | 3V_F34T_41 |

System FAN Controller



Diode circuit is used for skin temp sensor (placed between CPU and MXM). Place C1814 close to Q276 as possible.

MXM1 FAN Controller



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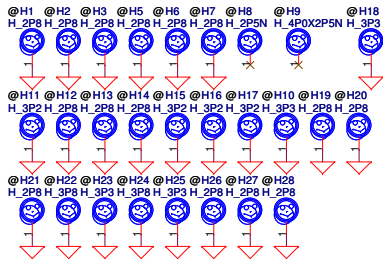
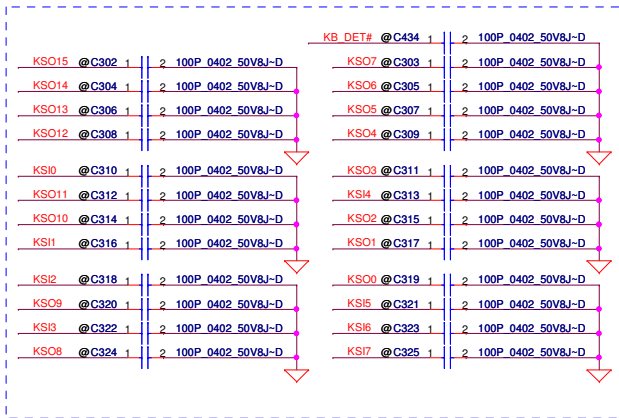
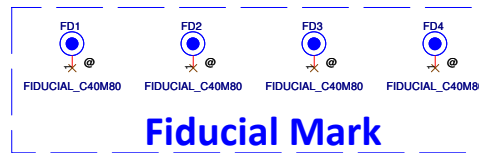
Compal Electronics, Inc.

Thermal Sensor & FAN

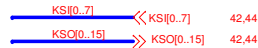
LA-6601P

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| Size | Document Number | Rev |
| | LA-6601P | 1.0 |
| Date: | Tuesday, November 30, 2010 | Sheet 45 of 63 |

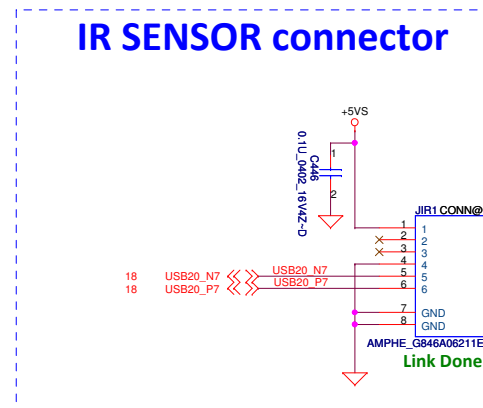
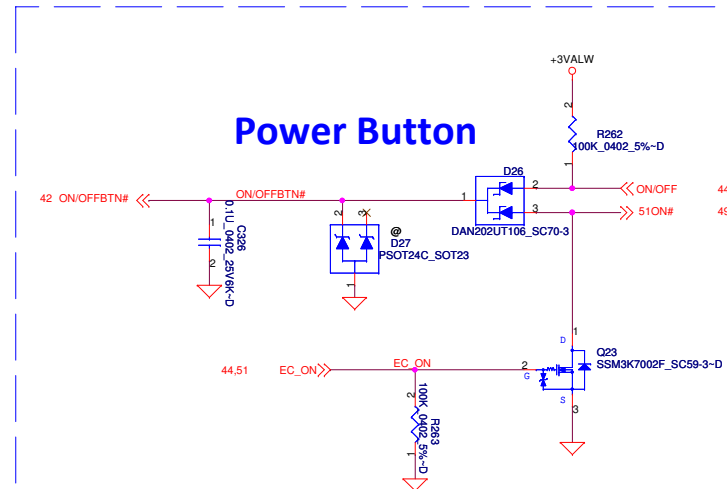
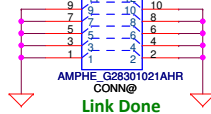




INT_KBD Conn.



| 16 | KB_DET# | KB1 | KB_DET# |
|----|---------|-----|---------|
| | KSO7 | 59 | 60 |
| | KSO0 | 57 | 58 |
| | KSI1 | 55 | 56 |
| | KSI7 | 53 | 54 |
| | KSO9 | 51 | 52 |
| | KSI6 | 49 | 50 |
| | KSI5 | 47 | 48 |
| | KSI4 | 45 | 46 |
| | KSI3 | 43 | 44 |
| | KSI2 | 41 | 42 |
| | KSO1 | 39 | 40 |
| | KSI3 | 37 | 38 |
| | KSI0 | 35 | 36 |
| | KSO13 | 33 | 34 |
| | KSO5 | 31 | 32 |
| | KSO2 | 29 | 30 |
| | KSO4 | 27 | 28 |
| | KSO8 | 25 | 26 |
| | KSO6 | 23 | 24 |
| | KSO11 | 21 | 22 |
| | KSO10 | 19 | 20 |
| | KSO12 | 17 | 18 |
| | KSO14 | 15 | 16 |
| | KSO15 | 13 | 14 |
| | | 11 | 12 |
| | | 9 | 10 |
| | | 7 | 8 |
| | | 5 | 6 |
| | | 3 | 4 |
| | | 1 | 2 |



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KB & Power Button & IR

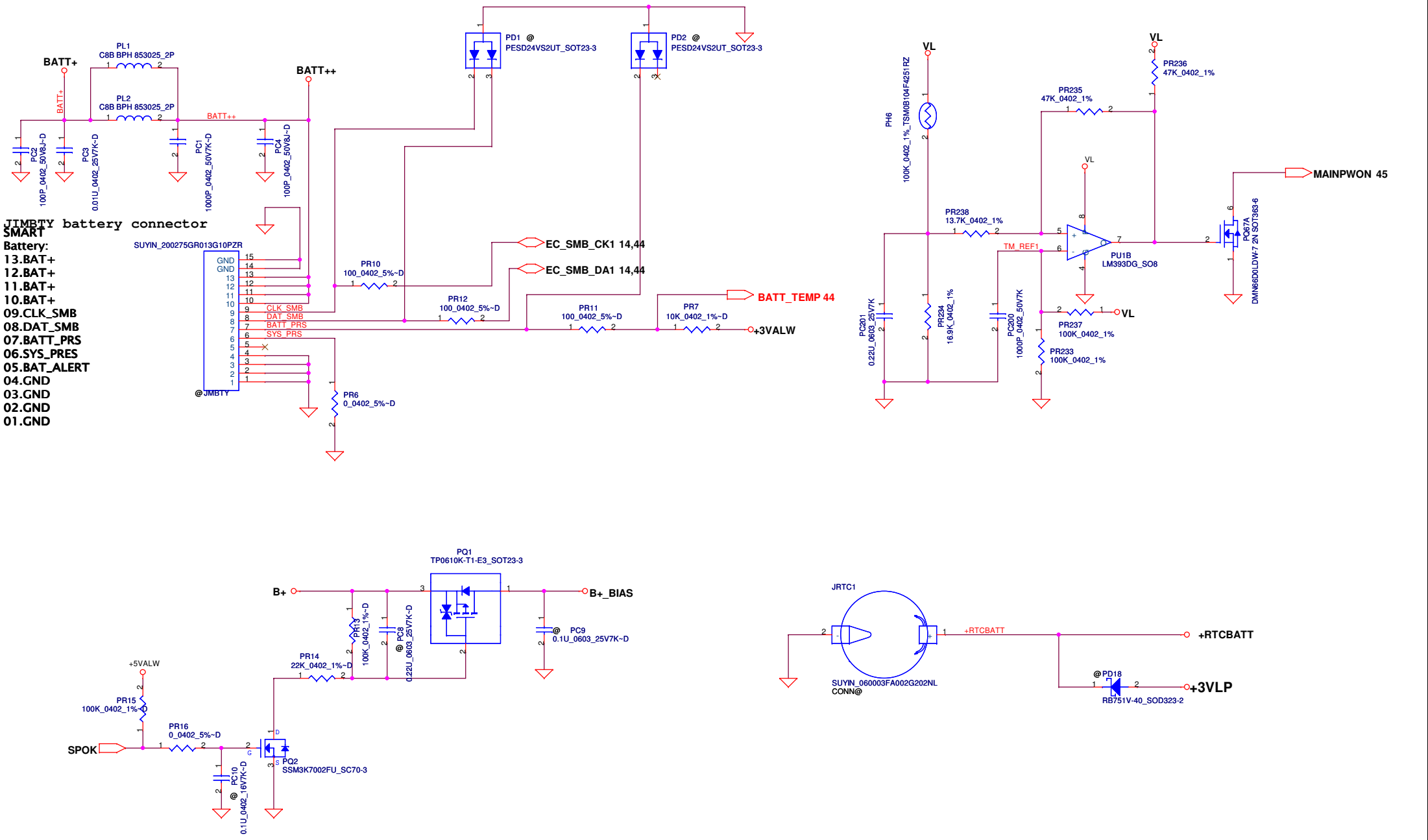
LA-6601P

Rev 1.0

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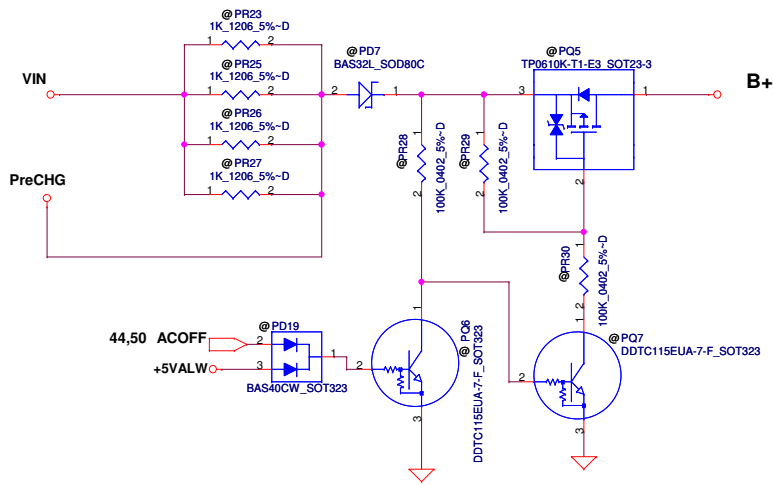
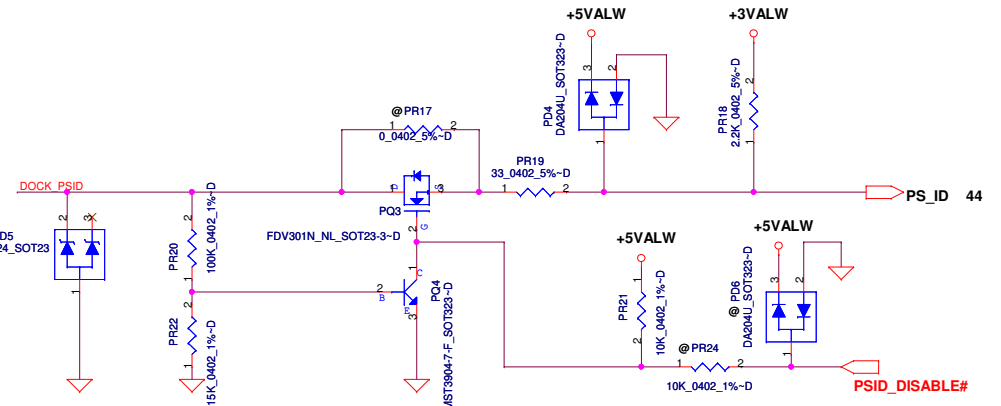
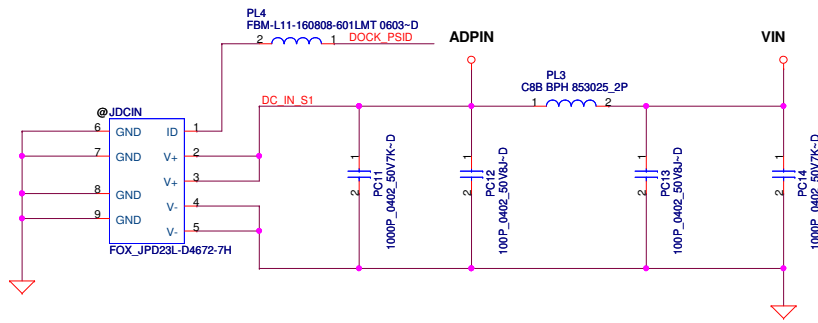
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JMBTY battery connector
SMART
Battery:
 13.BAT+
 12.BAT+
 11.BAT+
 10.BAT+
 09.CLK_SMB
 08.DAT_SMB
 07.BATT_PRS
 06.SYS_PRES
 05.BAT_ALERT
 04.GND
 03.GND
 02.GND
 01.GND



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| | | | |
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| BATTERY CONN/OTP | | | |
| Size | Document Number | Rev | |
| | LA-6601P | 0.3 | |
| Date: | Tuesday, November 30, 2010 | Sheet | 48 of 63 |

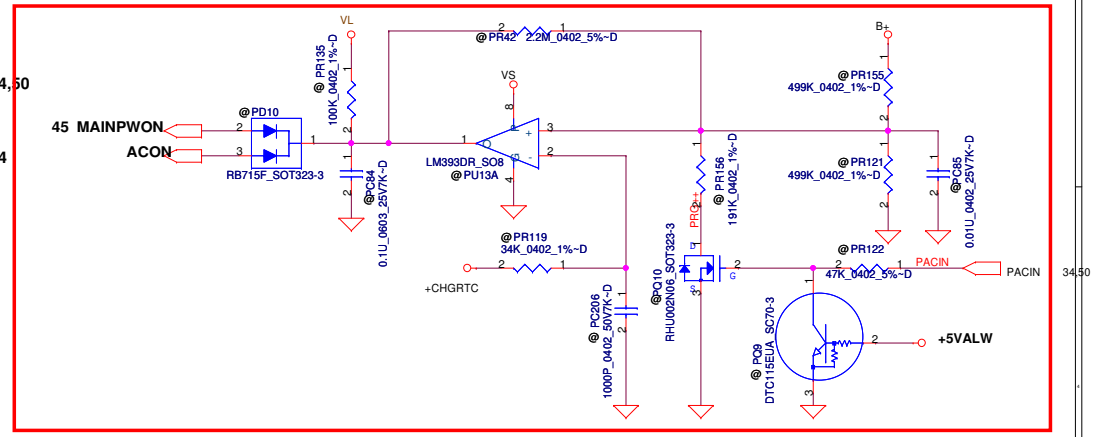
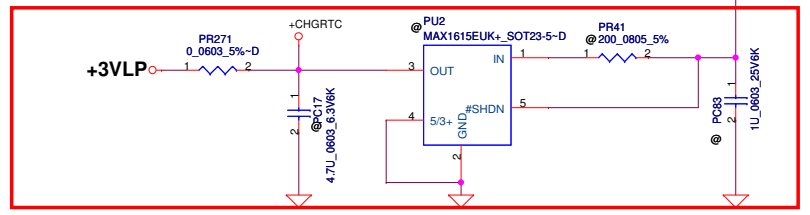
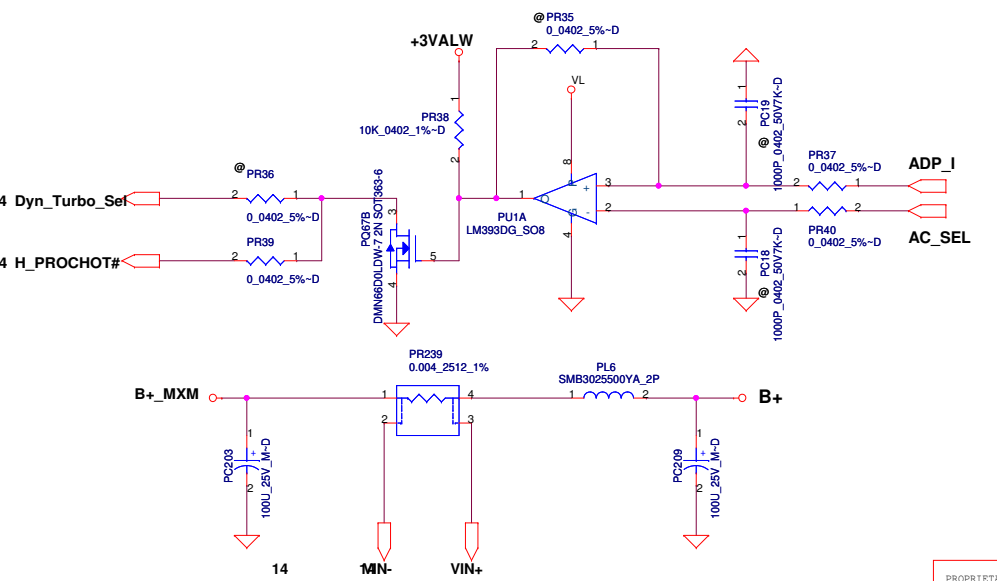
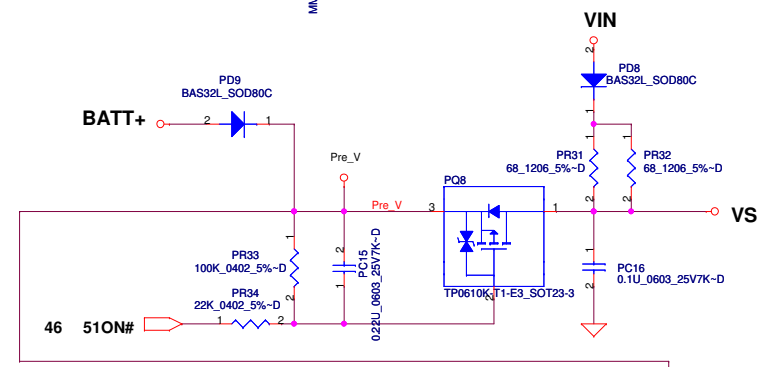


ACIN

| | Precharge detector | Min. | typ. | Max. |
|------|--------------------|--------|---------|------|
| H->L | 14.589V | 14.84V | 15.243V | |
| L->H | 15.562V | 15.97V | 16.388V | |

BATT ONLY

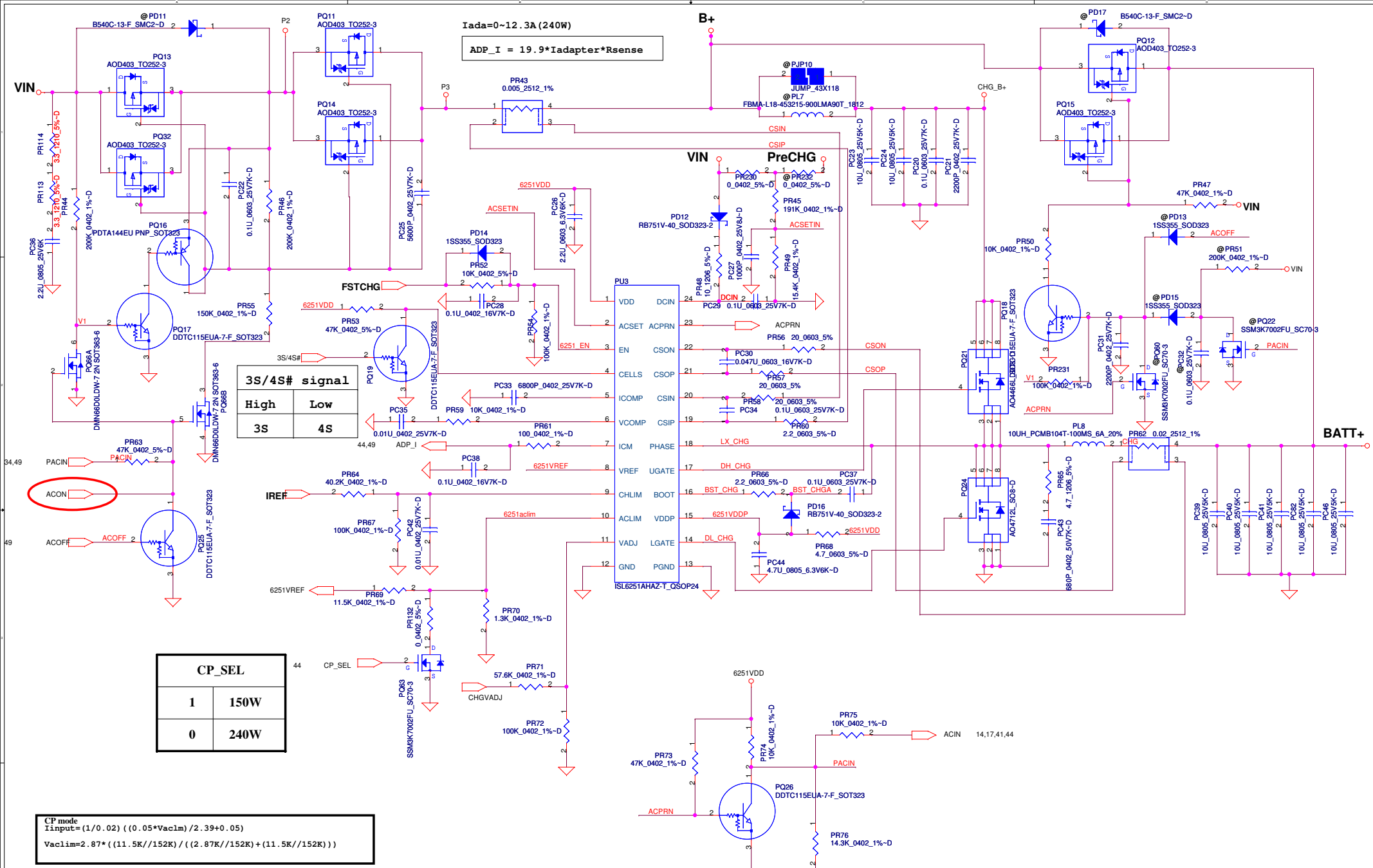
| | Precharge detector | Min. | typ. | Max. |
|------|--------------------|--------|-------|------|
| H->L | 4.92V | 6.1V | 5.25V | |
| L->H | 6.062V | 6.244V | 6.43V | |



Add MXM power net for HW request.

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| | | | |
|---------------------------------|----------------------------|------------|----------|
| Compal Electronics, Inc. | | | |
| DCIN & DETECTOR | | | |
| File | Document Number | Rev | |
| | LA-6601P | 0.3 | |
| Date: | Tuesday, November 30, 2010 | Sheet | 49 of 63 |



Tada=0~12.3A (240W)
 $ADP_I = 19.9 * I_{adapter} * R_{sense}$

| 3S/4S# signal | |
|---------------|-----|
| High | Low |
| 3S | 4S |

| CP_SEL | |
|--------|------|
| 1 | 150W |
| 0 | 240W |

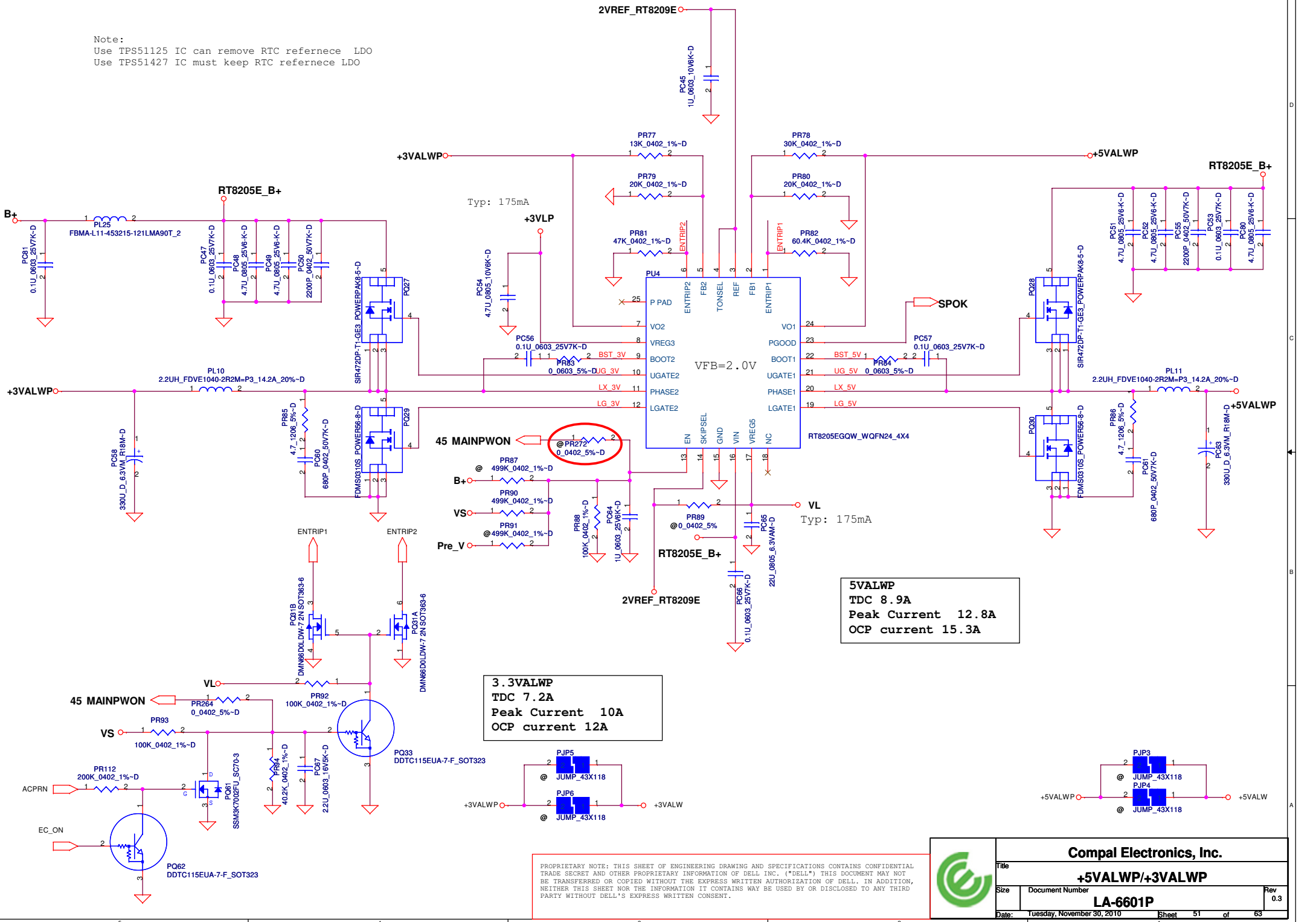
CP mode
 $I_{input} = (1/0.02) * ((0.05 * Vac_{lim}) / 2.39 + 0.05)$
 $Vac_{lim} = 2.87 * ((11.5K / 152K) / ((2.87K / 152K) + (11.5K / 152K)))$

| | | |
|-------------------|---------|----------------|
| CC=0.22~5.04A | CHGVADJ | CV mode |
| IREF=1*Icharge | 0V | 4V per cell |
| IREF=0.22V~3.294V | 1.882V | 4.2V per cell |
| | 3.3V | 4.35V per cell |

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| | | | |
|---------------------------------|----------------------------|-----------------|----------|
| Compal Electronics, Inc. | | | |
| Title | | CHARGER | |
| Size | Document Number | LA-6601P | |
| Date: | Tuesday, November 30, 2010 | Sheet | 50 of 63 |

Note:
 Use TPS51125 IC can remove RTC refernece LDO
 Use TPS51427 IC must keep RTC refernece LDO




Typ: 175mA

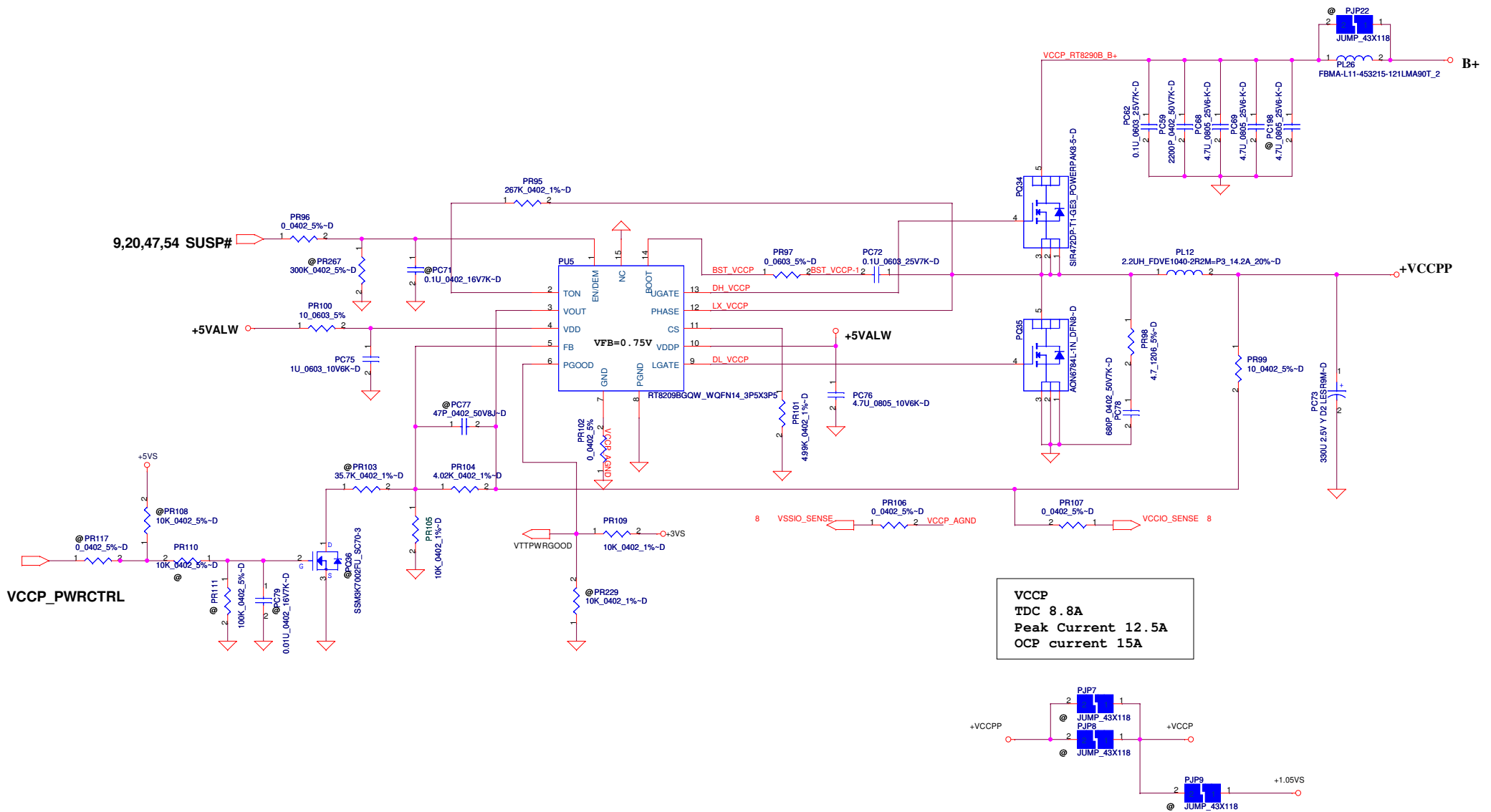
Typ: 175mA

5VALWP
 TDC 8.9A
 Peak Current 12.8A
 OCP current 15.3A


3.3VALWP
 TDC 7.2A
 Peak Current 10A
 OCP current 12A

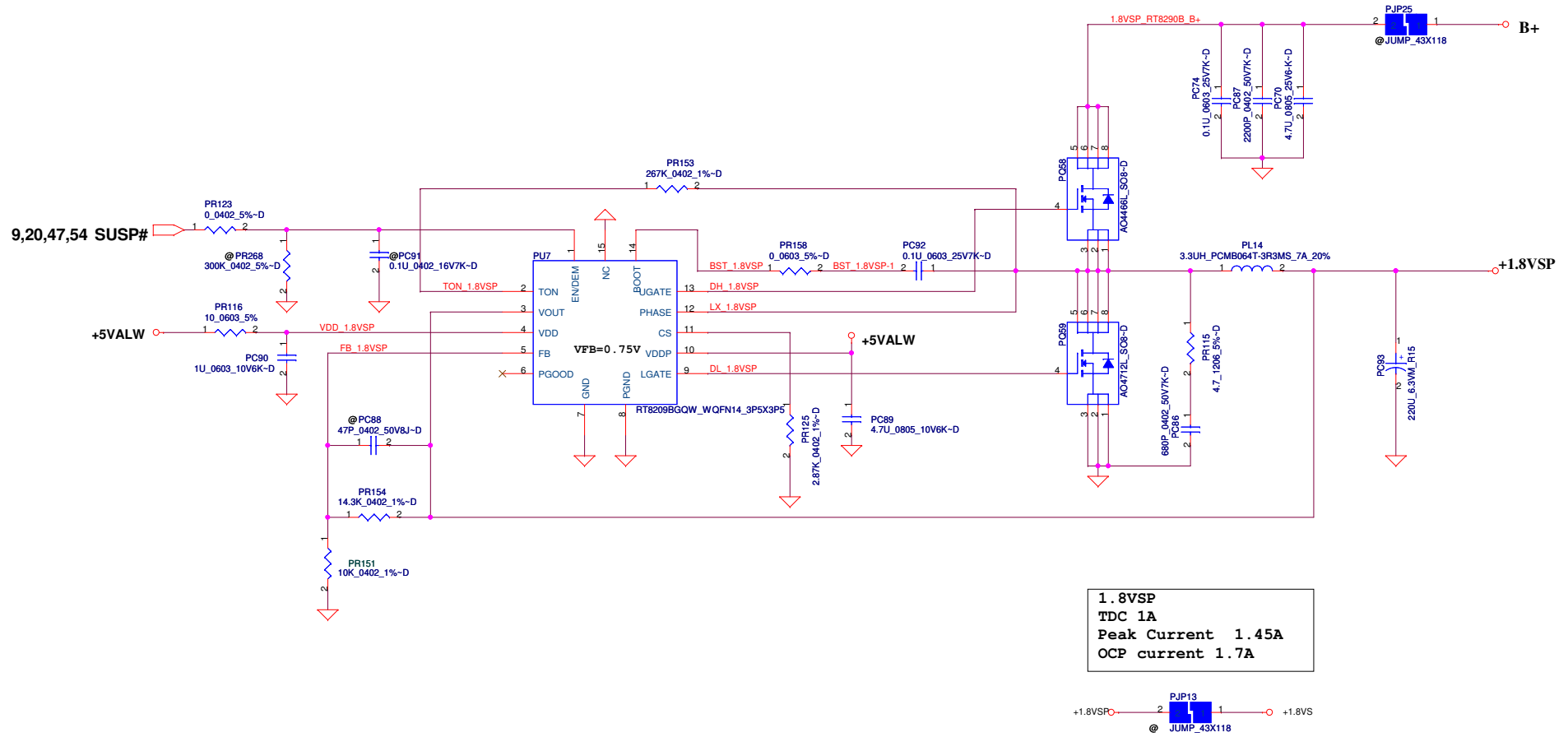
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| | | | | |
|---|----------------------------|--|---------------------------------|----------|
|  | | | Compal Electronics, Inc. | |
| | | | +5VALWP/+3VALWP | |
| Size | Document Number | | | Rev |
| | LA-6601P | | | 0.3 |
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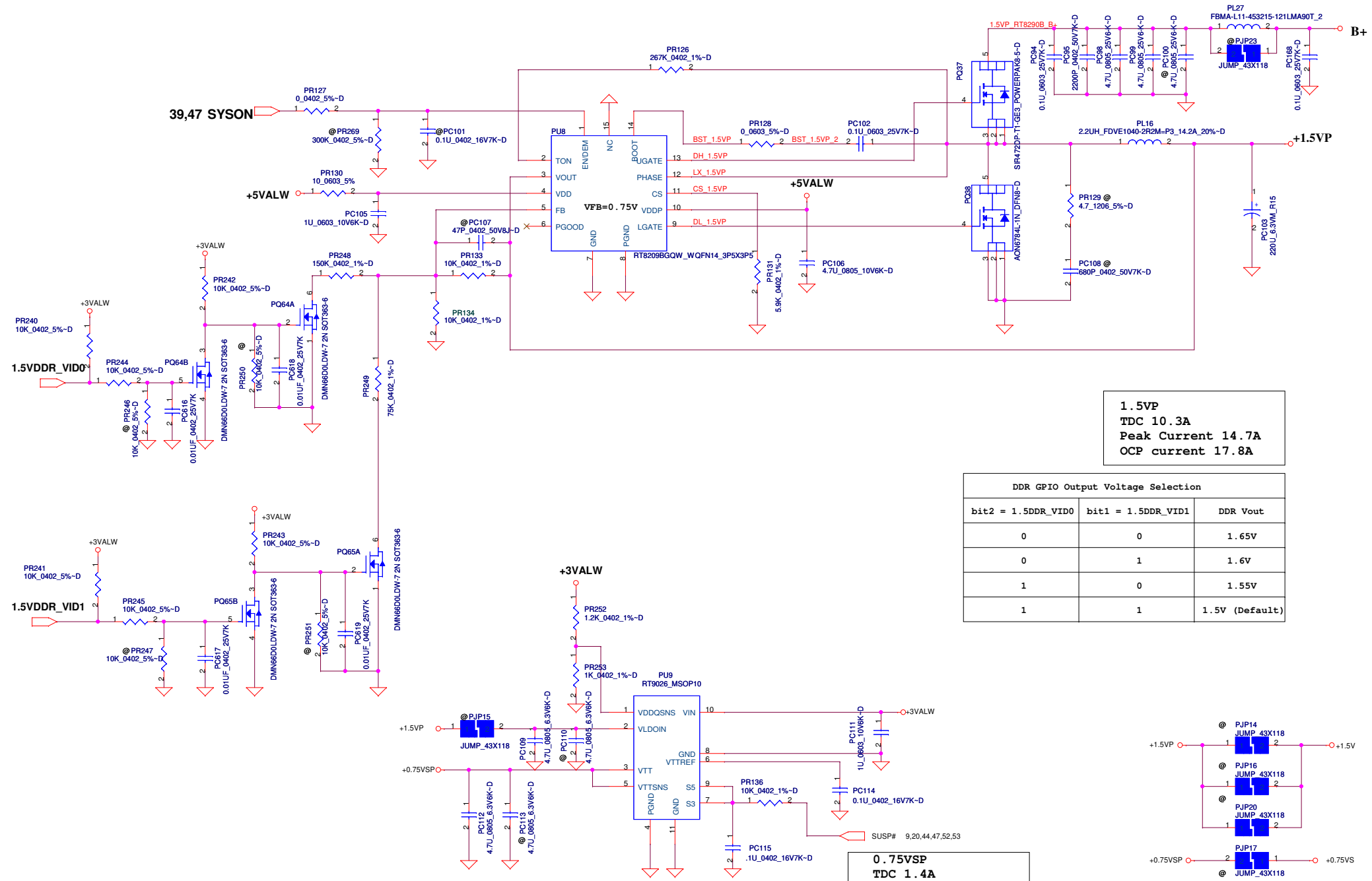
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|  | | | Compal Electronics, Inc. | |
| | | | +VCCPP | |
| Size | Document Number | LA-6601P | | Rev |
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| | | |
| Compal Electronics, Inc. | | |
| Title | | |
| +1.8VSP | | |
| Size | | |
| Document Number | | Rev |
| LA-6601P | | 0.3 |
| Date: Tuesday, November 30, 2010 | | |
| Sheet 53 | | of 63 |

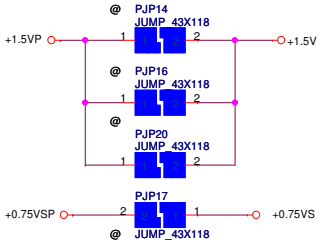
39,47 SYSON



1.5VP
TDC 10.3A
Peak Current 14.7A
OCp current 17.8A

| DDR GPIO Output Voltage Selection | | |
|-----------------------------------|--------------------|----------------|
| bit2 = 1.5DDR_VID0 | bit1 = 1.5DDR_VID1 | DDR Vout |
| 0 | 0 | 1.65V |
| 0 | 1 | 1.6V |
| 1 | 0 | 1.55V |
| 1 | 1 | 1.5V (Default) |

0.75VSP
TDC 1.4A
Peak Current 2A
OCp current 3A



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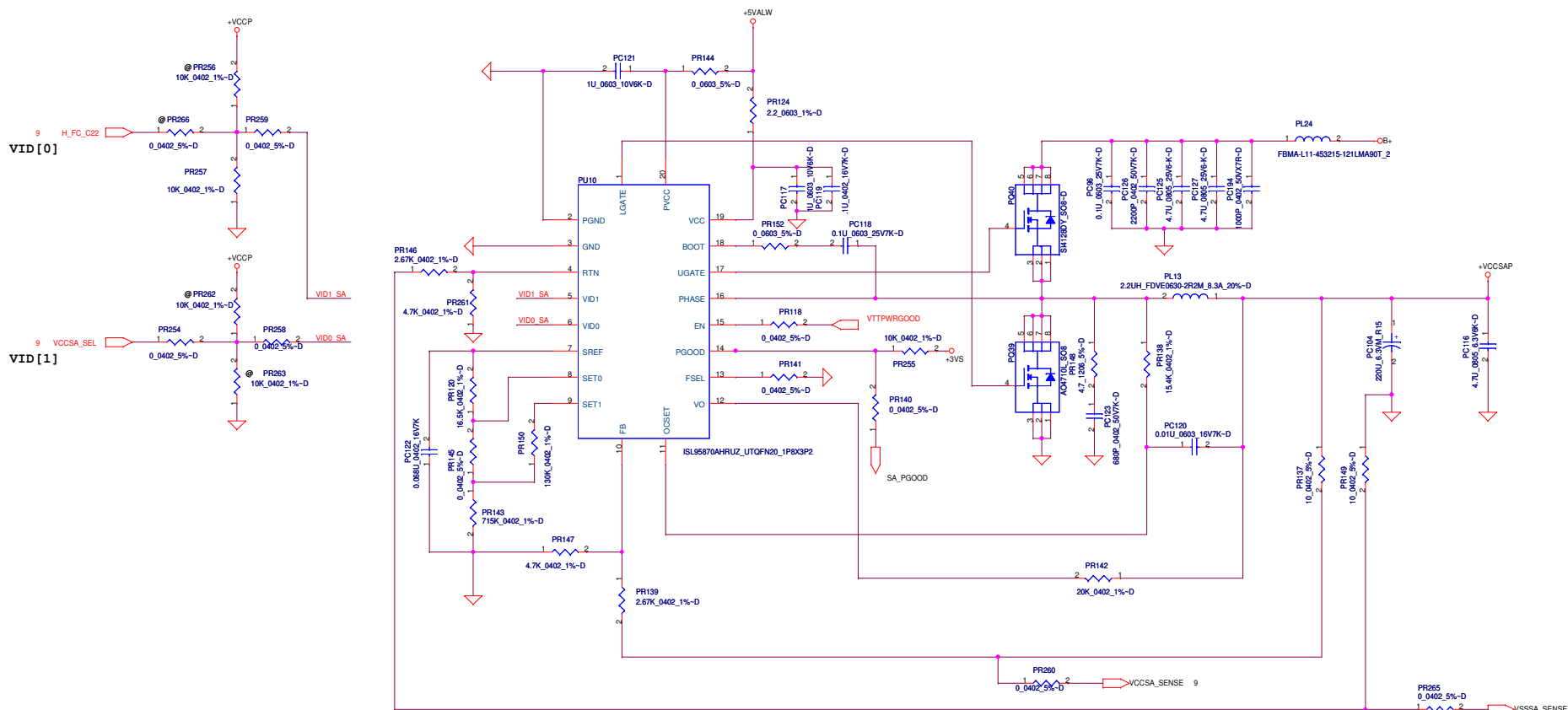
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Title
+1.5VSP/0.75VSP

Size | **Document Number**
LA-6601P

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Rev
0.3




Note:
RIN pin need reference output GND

| VID[0] | VID[1] | VCCSA Vout | Required | Yes | Yes |
|--------|--------|------------|----------|-----|-----|
| 0 | 0 | 0.9V | Yes | Yes | Yes |
| 0 | 1 | 0.8V | Yes | Yes | Yes |

+VCCSAP
TDC 4.2A
Peak Current 6A
OCp current 7.2A



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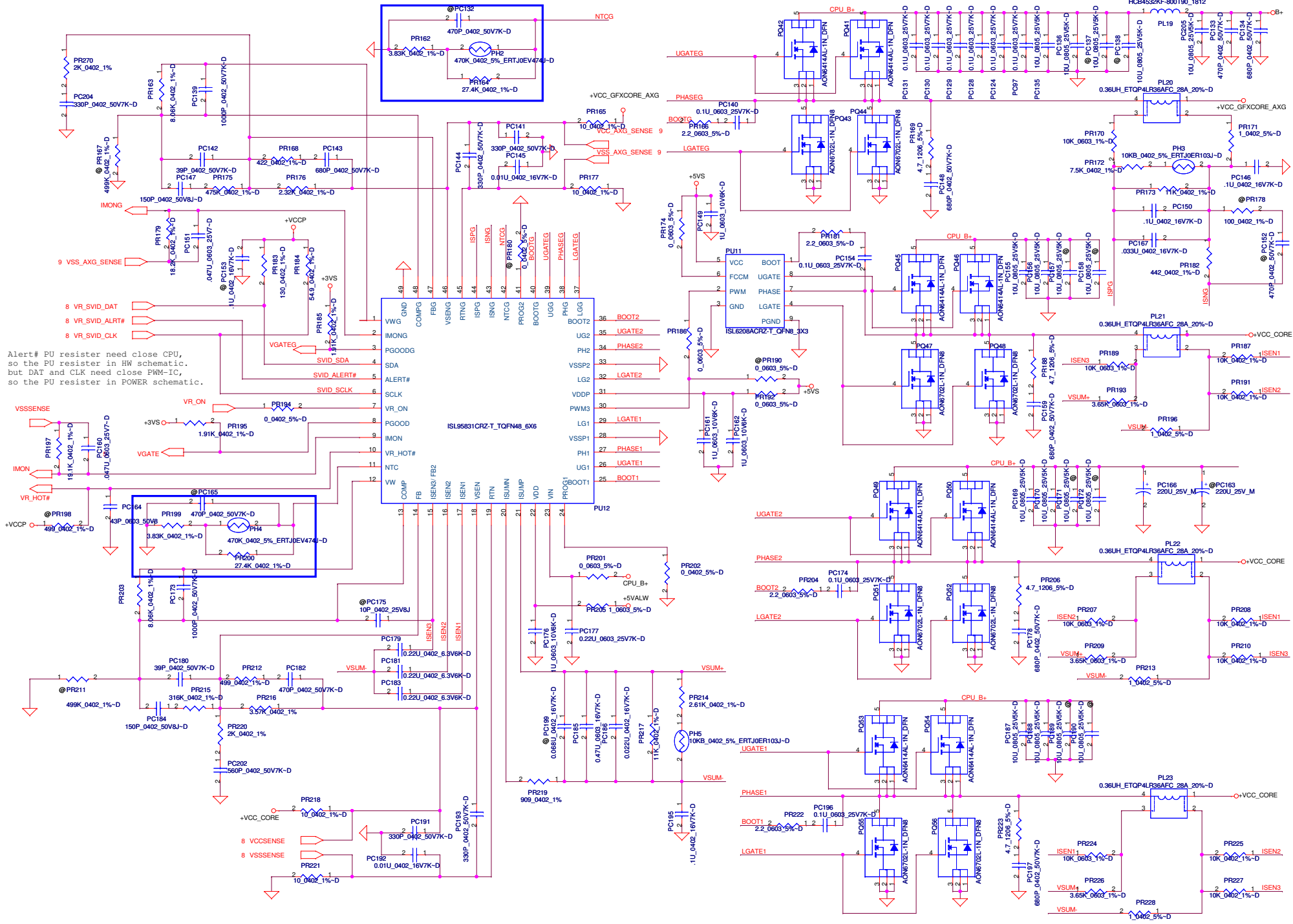


Compal Electronics, Inc.

Title: **PWR-VCCSA COREP**

Size: Document Number **LA-6601P** Rev **0.3**

Date: Tuesday, November 30, 2010 Sheet 55 of 63



Alert# PU resistor need close CPU,
so the PU resistor in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resistor in POWER schematic.

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| File PWR-CPU_CORE | | |
| Size | Document Number | Rev |
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|------|----------|---|----------|---------------|--|---|------|
| 1 | 56 | CPU_CORE | 10'06/17 | Compal_Alvin | Improve thermal compensation. | Change PR164 from 0ohm to 27.4Kohm. | X00 |
| 2 | 51-57 | all DC-DC schematic | 10'06/17 | Compal_Alvin | Improve dc to dc power efficiency. | Delete all snuber for all dc-dc. Delete PR85, PR86, PR98, PR115, PR129, PR148, PR169, PR188, PR206, PR223. Delete PC60, PC61, PC78, PC86, PC108, PC123, PC148, PC159, PC178, PC197. | X00 |
| 3 | 50 | Charger | 10'07/22 | Compal_Alvin | Voltage rating enhancement. | Change PR49 form 14.3K to 15K. | X01 |
| 4 | 50 | Charger | 10'07/22 | Compal_Alvin | Output capacitor rating enhancement. | Add PC46 10uF 0805 to output. | X01 |
| 5 | 51 | +5VALWP/+3VALWP | 10'07/22 | Compal_Alvin | Enhance Input capacitor rating and switch waveform. | Add PC80 4.7uF 0805 to input and change low side to FDMS0310S. | X01 |
| 6 | 56 | CPU_CORE | 10'07/22 | Compal_Alvin | Improve EMC solution. | Add PC97, PC124, PC128, PC129, PC130, PC131 0.1uF 0603. | X01 |
| 7 | 51 | +5VALWP/+3VALWP | 10'07/22 | Compal_Alvin | Improve EMC solution. | Add PC80 0.1uF 0603. | X01 |
| 8 | 54 | +1.5VP/0.75VSP | 10'07/22 | Compal_Alvin | Improve EMC solution. | Add PC168 0.1uF 0603. | X01 |
| 9 | 55 | VCCSAP | 10'07/22 | Compal_Alvin | Improve EMC solution. | Add PL24 120ohm bead, and PC194 1000pF 0402. | X01 |
| 10 | 53 | +1.8VSP | 10'07/22 | Compal_Alvin | Improve low side switching waveform. | Change PQ59 from AO4466 to AO4712L | X01 |
| 11 | 49 | DCIN/DECTOR | 10'08/03 | Compal_Alvin | Add dynmatic trubo function to control trubo. | Add dynamatic trubo function. | X01 |
| 12 | 52 | +VCCPP | 10'08/10 | Compal_Alvin | For met Intel SPEC. | Change VCCPP output CAP to 470uF. | X01 |
| 13 | 56 | CPU_CORE | 10'08/10 | Compal_Alvin | Adjust the CPU loadline and transient to met Intel SPEC. | PC167 and PC186. PR216, PR219, PR202, PR180, PR176, PR179, PR182, PR167, PR186. | X01 |
| 14 | 56 | CPU_CORE | 10'09/28 | Compal_Alvin | Improve CPUCore PWRGOOD signal. | Change VDD power rail from 5VS to 5VALW and add PR220 and PC202. | X02 |
| 15 | 55 | VCCSAP | 10'09/28 | Compal_Alvin | Improve VCCSA PWRGOOD signal. | Change VCC power rail from 5VS to 5VALW. | X02 |
| 16 | 49/50 | DCIN/DECTOR BATTERY CONN/OTP | 10'09/28 | Compal_Alvin | Saving S4/S5 power consumption. | Change PUI Pin8 from Pre_V to VL. | X02 |
| 17 | 51/52/54 | +5VALWP/+3VALWP +VCCPP +1.5VP/0.75VSP | 10'10/12 | Compal_Alvin | For EMI solution. | Add PL25, PL26, PL27 P/N:SM01000DJ00 (S SUPPRE_FBMA-L11-453215-121LMA90T 1812) Add 10uF PC205 and change PC23, PC24 to 10uF. Pop PC133 and PC134. | X02 |

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|-------------|--------------|---------------------|-------------|----------------------|--|--|-------------|
| 18 | 51-56 | all DC-DC schematic | 10'10/13 | Compal_Alvin | EMI solution. | Add all snuber for all dc-dc. Add PR85, PR86, PR98, PR115, PR129, PR148, PR169, PR188, PR206, PR223. Add PC60, PC61, PC78, PC86, PC108, PC123, PC148, PC159, PC178, PC197. | X02 |
| 19 | 50 | Charger | 10'11/02 | Compal_Alvin | Precharger schematic bom change for old solution | Delete PD13, PD15, PR51, PQ22, PC32. Add PQ60, PR231. | X02 |

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Version Change List (P. I. R. List)

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|---------------|---------------|-----------------------------|---------------------|-----------------------|---|--|----------------|
| 1 | 29 | DP SW for mDP CONN | 10'07/22 | Compal_Yungmao | Mini DP no function | Modified JMDP1 pin define | X00 |
| 2 | 39 | USB 3.0 PD720200 | 10'08/10 | Compal_Yungmao | USB3.0 transfer speed is too low | L33 swap pin3 with pin4, net U3TXDN2_L, U3TXDN2 L34 swap pin3 with pin4, net U3RXDP1_L, U3TXDP1 L35 swap pin3 with pin4, net U3RXDN2_L, U3RXDN2 L36 swap pin3 with pin4, net U3RXDP1_L, U3RXDP1 | X00 |
| 3 | 31 | HDMI input - STDP6038 | 10'07/22 | Compal_Yungmao | HDMI-IN no function | Change U7 pin111, 112 to U7 pin72, pin71 | X00 |
| 4 | 34-35 | HD Audio_IDT92HD73C | 10'08/3 | Compal_Yungmao | S/PDIF jack no function | net LINE_OUT_JD connect to R1677 pin2 delete R721, R722, C740 | X00 |
| 5 | 38 | Mini Card -WLAN / DMC / BT | 10'08/11 | Compal_Yungmao | Install Bluetooth module might be cause system can't bootable | remove net name BT_ACTIVE | X00 |
| 6 | 33 | GLAN AR8151 AL1A | 10'08/9 | Compal_Yungmao | LOM can't work in 1000Mbps speed and no LED is on | swap JLAN1 pin11 with pin13, net LAN_LINK#, LAN_LED2# | X00 |
| 7 | 34 | HD Audio_IDT92HD73C | 10'08/10 | Compal_Yungmao | Audio left and right channel reverse | swap U9, U16 pin6 with pin8 | X00 |
| 8 | 40 | USB/ESATA TS3USB221RSER | 10'08/3 | Compal_Yungmao | USB charging Device can't be charging in S4/S5 with " AC and Battery " mode | change D18 from +5VS to +5VALW | X00 |
| 9 | 14 | MXMIII Connector A | 10'07/22 | Compal_Yungmao | -9% of 3.3V (3.003) will cause no display when system power on | add R1817, R1816, Q281 | X00 |
| 10 | 5 | PROCESSOR(2/6) PM, XDP, CLK | 10'07/15 | Compal_Yungmao | for EMI/EDS requirement | add RC121, RC125, RC126, RC127, RC128 | X00 |
| 11 | 10-13 | DDRIII DIMMA ~ DDRIII DIMMD | 10'07/15 | Compal_Yungmao | for DDR3 module can select serial address | add RD35, RD36, RD37, RD38, RD39, RD47, RD49 | X00 |
| 12 | 14 | MXMIII Connector A | 10'08/4 | Compal_Yungmao | for MXM3.0 module power saving | add R1818, R1819 pull high | X00 |
| 13 | 25 | LVDS SW- 1 to 2 & GPU/PCH | 10'07/13 | Compal_Yungmao | STDP6038 chipset vendor require to add for debug used | add R313, R314 | X00 |
| 14 | 04 | PROCESSOR(6/6) | 10'09/20 | Compal_Ray | derating fail | QC4 change to SB00000090L | X02 |
| 15 | 14 | MXMIII Connector | 10'09/20 | Compal_Ray | battery can't charge | R1818, R1819 depop, change connection EC_SMB_DA1 to VGA_SMB_DA1 | X02 |
| 16 | 17 | PCH (3/8) | 10'09/20 | Compal_Ray | can't boot when plug bluetooth module. | pop RH95 | X02 |
| 17 | 26 | LVDS SW & CONN | 10'09/20 | Compal_Ray | Web CAM can't work. | Change CAM power to 3VS | X02 |

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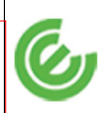


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|---------------|---------------|----------------------|---------------------|-----------------------|--|--|----------------|
| 17 | 28 | HDMI SW | 10'09/20 | Compal_Ray | Follow A18 +HDMI_5V_OUT circuit | remove QV5,CV40,RV35,QV6,RV34,Add R1896 | X02 |
| 18 | 28 | HDMI SW | 10'09/20 | Compal_Ray | HDMI can't work | Change UV2 HPD connection | X02 |
| 19 | 30 | HDMI SW for DMC | 10'09/20 | Compal_Ray | DP can't work | pop R1865 add R1958,R1959, remove C52,C53 | X02 |
| 20 | 40 | USB/ESATA | 10'09/20 | Compal_Ray | eSATA can't work | remove RS12 | X02 |
| 21 | 40 | USB/ESATA | 10'09/20 | Compal_Ray | update for eSATA power share function | PWRSHARE_EN# GPIO assign to EC pin 86 Add R97 for PWRSHARE_EN# pull down add R1699,D31 | X02 |
| 22 | 15 | PCH (1/8) | 10'09/20 | Compal_Ray | ME position redifned for HDD. | Swap HDD1(Port 1) ,HDD2(Port 0) | X02 |
| 23 | 39 | USB3.0 PD720200 | 10'09/27 | Compal_Ray | USB3.0 can't work | depop R201, pop R202 0 ohm | X02 |
| 24 | 17 | PCH (3/8) | 10'09/27 | Compal_Ray | AV17 doesn't support deep sleep mode | pop RH126, add RH159 and depop it depop RH139 ,RH134 | X02 |
| 25 | 15 | PCH (1/8) | 10'09/27 | Compal_Ray | Add HDA BUS ON/OFF control circuit, | add CH17,UH9,RH30,RH50,QH10,RH267 | X02 |
| 26 | 15 | PCH (1/8) | 10'09/27 | Compal_Ray | follow Design guide | Add RH47 for BBS_BIT0_R | X02 |
| 27 | 17 | PCH (3/8) | 10'09/27 | Compal_Ray | follow Design guide | Add R1687 for PCH_RSMRST# pull down | X02 |
| 28 | 17 | PCH (3/8) | 10'09/27 | Compal_Ray | Change ACIN connection | Remove RH150 ,RH137,Add R1900,R1899,QH11 | X02 |
| 29 | 35 | Speaker AMP | 10'09/27 | Compal_Ray | To solve po noise when HDMI IN toggling | add Q10 | X02 |
| 30 | 04 | PROCESSOR(6/6) | 10'09/27 | Compal_Ray | derating fail | QC4 change to SB00000090L | X02 |
| 31 | 34 | HD Audio | 10'09/27 | Compal_Ray | Add HDMI IN audio sense circuit. | add Q284 R1902,R1903 | X02 |
| 32 | 34 | HD Audio | 10'09/27 | Compal_Ray | to solve backdrive issue on +3VS | add D54 | X02 |
| 33 | 15 | PCH (1/8) | 10'09/27 | Compal_Ray | follow DG1.5 recommend | Add R1960 | X02 |


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|------|---------|------------------|----------|---------------|---|---|------|
| 34 | 16 | PCH (4/8) | 10'09/27 | Compal_Ray | PLTREST_VGA issue | Add R28 D13 and change RH170 to 0 ohm | X02 |
| 35 | 28 | HDMI SW | 10'10/01 | Compal_Ray | Add R58 for HMI_SW_DETECT bypass direct due to it's desn't need level shift to 5V | Add R58 | X02 |
| 36 | 35 | Speaker AMP | 10'10/01 | Compal_Ray | add mute siwtch to solve po noise issue | Add U619 ,C1843 | X02 |
| 37 | 33 | GLAN AR8151 AL1A | 10'10/01 | Compal_Ray | Change CL39 to 3KV spec for Hi-port test | change CL39 to 1000P_1808_3KV7K-D | X02 |
| 38 | 15 | PCH | 10'10/07 | Compal_Ray | Rename location | Change CLIP1 to COMS1 and CLIP2 to ME1 | X02 |
| 39 | 39 | USB 3.0 | 10'10/07 | Compal_Ray | Add power option | Add R1964,R1965,R1966,R1967 for U37 power option | X02 |
| 40 | 31 | HDMI | 10'10/07 | Compal_Ray | For double pull high | Remove R81,R83 | X02 |
| 41 | 15 | PCH | 10'10/07 | Compal_Ray | Change RTC circuit | Change RTC circuit and change DH1 to CHN202UPT,Reomve RH250 | X02 |
| 42 | 33 | GLAN AR8151 AL1A | 10'10/07 | Compal_Ray | Crystal EA result | Change CL18,CL19 to 15pF by crystal EA result | X02 |
| 43 | 9,10,11 | CPU | 10'10/07 | Compal_Ray | Remove XDP 0 ohm resistor | CPU XDP depop, Remove:RC68~RC71, Change to depop RC59,RC61~RC67,RC121,RC121,RC125~RC128,RC50,RC51 Add T51~T54 | X02 |
| 44 | 16 | PCH | 10'10/07 | Compal_Ray | Crystal EA result | Change YH2 to X5H025000DC1H-H, CH23,CH24 to 12pF by crystal EA result | X02 |
| 45 | 5 | CPU | 10'10/07 | Compal_Ray | Follow Design guide 1.5 | Add RC113 to reserve PCH_PWROK for VDDPWROOD | X02 |
| 46 | 31 | ST6038 | 10'10/07 | Compal_Ray | Derating issue | Change L13 to BLM18AG601SN1D for derating issue | X02 |
| 47 | 9 | CPU | 10'10/07 | Compal_Ray | S3 issue | Reserve CC178 for CPU1.5V_S3_GATE timing delay | X02 |
| 48 | 31 | ST6038 | 10'10/07 | Compal_Ray | By vendor review | Follow vendor to depop R1744 | X02 |
| 49 | 32 | ST4028 | 10'10/07 | Compal_Ray | By vendor review | Change U607 to M25PE20 | X02 |
| 50 | 31 | ST6038 | 10'10/08 | Compal_Ray | Timing issue | Add R172 for LDO timing enable timing delay | X02 |

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|------|--------|--------------|------------|---------------|--|---|------|
| 51 | 16 | Codec | 2010/10/8 | Compal_Ray | Mute issue | Add U620,C1844,U621,C1845 for mute | X02 |
| 52 | 28 | MXM | 2010/10/8 | Compal_Ray | Follow A18 | Change AC_BATT# to EC_AC_BAT# , and remove R1817,D72, add U622,C1823 | X02 |
| 53 | 35 | USB3.0 | 2010/10/8 | Compal_Ray | EMI issue | Change L33~L38 to DLW21SN670HQ2L | X02 |
| 54 | 26 | LVDS SW | 2010/10/8 | Compal_Ray | Remove resistor for double pull high | Remove R323 ,R326 | X02 |
| 55 | 35 | Audio | 2010/10/12 | Compal_Ray | By Maxim review result | Change C154,C158 to .022uF and R140,R145 to 20K | X02 |
| 56 | 15 | PCH | 2010/10/12 | Compal_Ray | Reserve 0 ohm for HDA_SDOUT | Add RH51 | X02 |
| 57 | 44 | ENE | 2010/10/12 | Compal_Ray | Change GPIO | Change GPIO46 to VGA_ON and depop RH118 | X02 |
| 58 | 24, 44 | ENE | 2010/10/12 | Compal_Ray | Change GPIO, and add backlight control circuit | Change VGA_ON to LCD_BKL_EN, and add backlight control circuit, add Q39,C332,R422,R423,Q28,C331 | X02 |
| 59 | 29 | DP | 2010/10/12 | Compal_Ray | DP dual mode can't display | Remove C301,C308 | X02 |
| 60 | 35 | Audio | 2010/10/12 | Compal_Ray | To reach 16dB | Change R137,R142 to 16.2K | X02 |
| 61 | 15 | PCH | 2010/10/22 | Compal_Ray | Pop RH50 for ME lock issue | Pop RH50 | A00 |
| 62 | 37 | ODD | 2010/10/22 | Compal_Ray | Re define ODD pin | For ODD power require, add one more power pin | A00 |
| 63 | 37 | ODD | 2010/10/22 | Compal_Ray | Remove zero power ODD switch. | Remove SW1 and add R173 0 ohm for ODD_DA# | A00 |
| 64 | 46 | power switch | 2010/10/22 | Compal_Ray | Remove reserve power switch | Remove SW4,SW5 | A00 |
| 65 | 24, 44 | LCD | 2010/10/22 | Compal_Ray | Correct net name | Rename LCD_BKL_EN# to LCD_BKL_EN | A00 |
| 66 | 44 | BID | 2010/10/22 | Compal_Ray | Change BID | Change BID, R225 to 56K | A00 |
| 67 | 34 | BID | 2010/10/22 | Compal_Ray | HDMI in audio issue. | change HDMI_IN_SELECT# to HDMI_TOGGLE | A00 |

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| | | Rev | 1.0 |

Version Change List (P. I. R. List)

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| Item | Page# | Title | Date | Request Owner | Issue Description | Solution Description | Rev. |
|------|----------------|-------|------------|---------------|--|--|------|
| 68 | 26 | AMD | 2010/10/22 | Compal_Ray | AMD MXM card Brightness Contrl Hot/Key issue | add RV46 and connect to SG_AMD_BKL. | A00 |
| 69 | 17, 28, 29, 30 | NV | 2010/10/22 | Compal_Ray | Meet NV Optimus V1.2 | Change AC_BATT# to EC_AC_BAT# , and remove R1817,D72, add U622,C1823 | A00 |
| 70 | 27 | CRT | 2010/10/22 | Compal_Ray | CRT switch high EOS failure rate | Change C13~C15 to 0.01uF. | A00 |
| 71 | 31 | HDMI | 2010/10/22 | Compal_Ray | HDMI in cable detect issue | Add R1968,Q285,R1845 | A00 |
| 72 | 44 | ENE | 2010/10/22 | Compal_Ray | Crystal remove for ENE | Add C1846 for not use crystal for ENE | A00 |
| 73 | 24 | EDP | 2010/10/29 | Compal_Ray | Remove RV39 | Remove RV39 for LCDVDD_ON double pull down | A00 |
| 74 | 36 | HDD | 2010/10/30 | Compal_Ray | Left HDD pin to NC | Left JHDD2 Pin 20,21,22 to NC | A00 |
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|  | | | Compal Electronics, Inc. | | |
| Title: EE PIR(2) | | | | | |
| Size: LA-6601P | | | | Rev: 1.0 | |
| Date: Tuesday, November 30, 2010 | | | Sheet 63 of 63 | | |