

# Compal confidential

## *Brazos-Delhi 10AB*

### PWWBE LA-6849P Schematics Document

Mobile AMD APU ZACATE-FT1 + FCH Hudson-M1

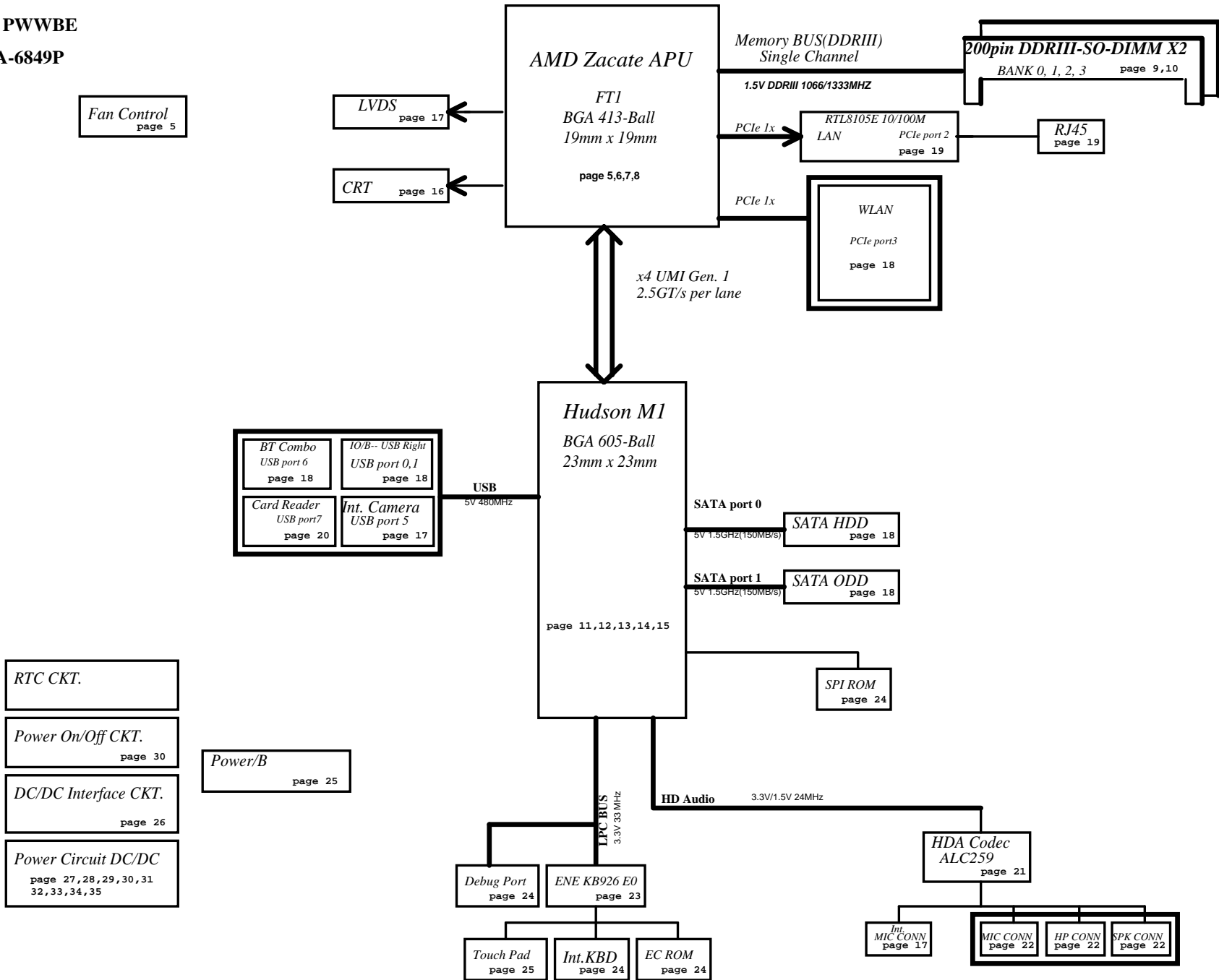
2010-11-22 Rev. 1.0

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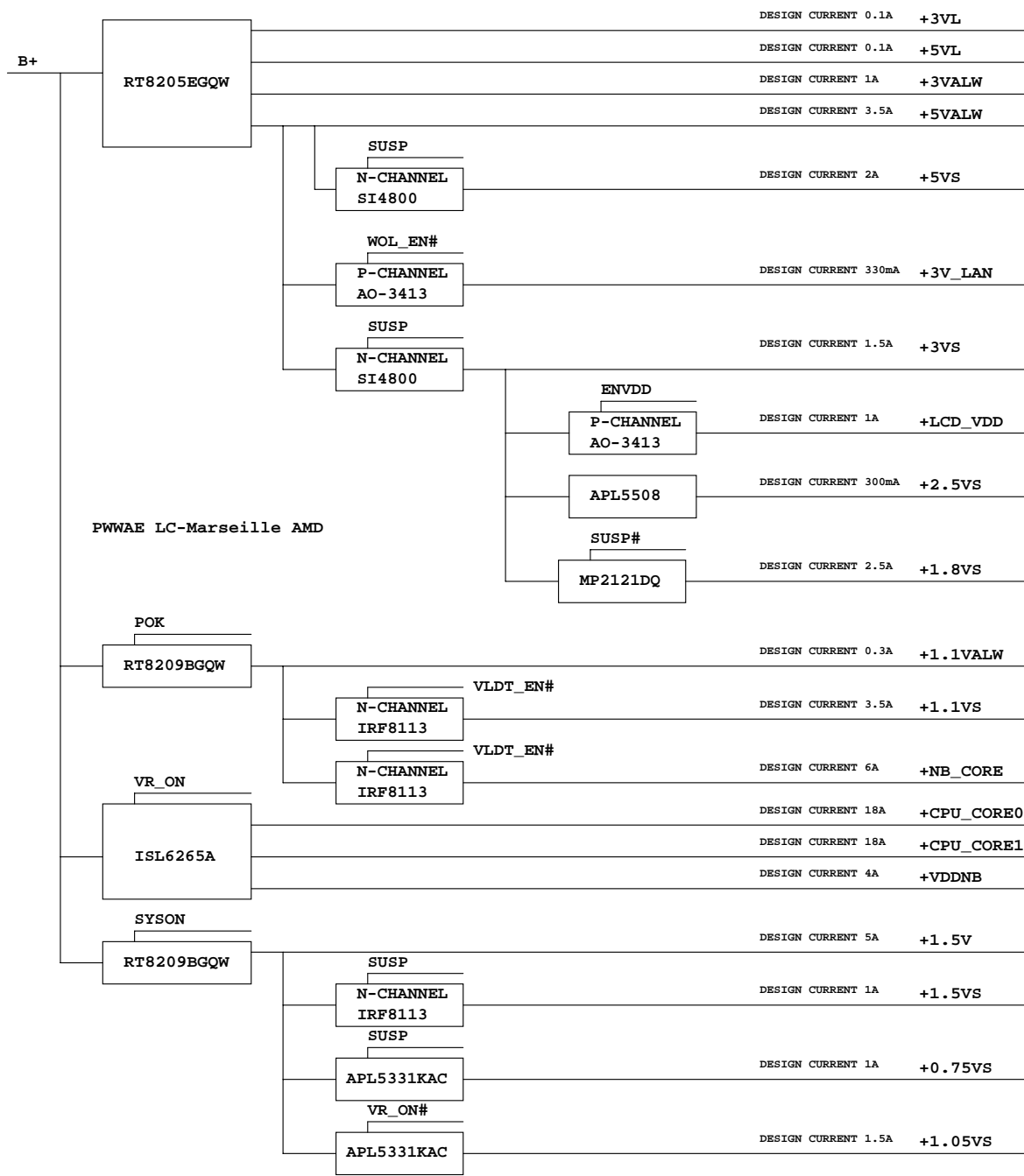
# Compal Confidential

Model Name : PWWBE

File Name : LA-6849P



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# Voltage Rails

O : ON  
X : OFF

power plane / State	+B +3VL +5VL +RTCVCC	+5VALW +3VALW +1.1VALW	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.1VS +1.05VS +0.75VS +AGP_CORE +APU_VDDNB
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Platform	CPU	SB	VGA	EC	Comment
Brazos	APU FT1	FCH M1	NA	KB926	

@ : just reserve , no build  
 CONN@ : just reserve for Connector only  
 8105E\_VC@: just reserve for 10/100 LAN VC version only  
 8105E\_VB@: just reserve for 10/100 LAN VBversion only  
 HDT@:just reserve for JHDT connector  
 E240@ : AMD E240 1.5Ghz CPU only  
 E350@ : AMD E350 1.6Ghz CPU only

## FCH SM Bus0 address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0 A0 H		1010 0000 b
+3VS	DDR SO-DIMM 1 A4 H		1010 0100 b

## FCH SM Bus1 address

Power	Device	HEX	Address
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## EC SM Bus1 address

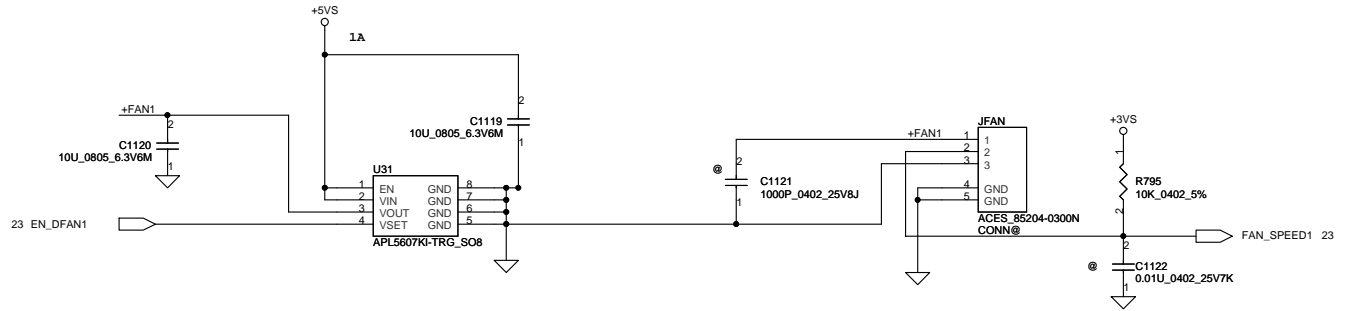
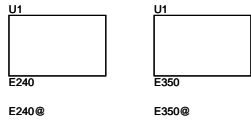
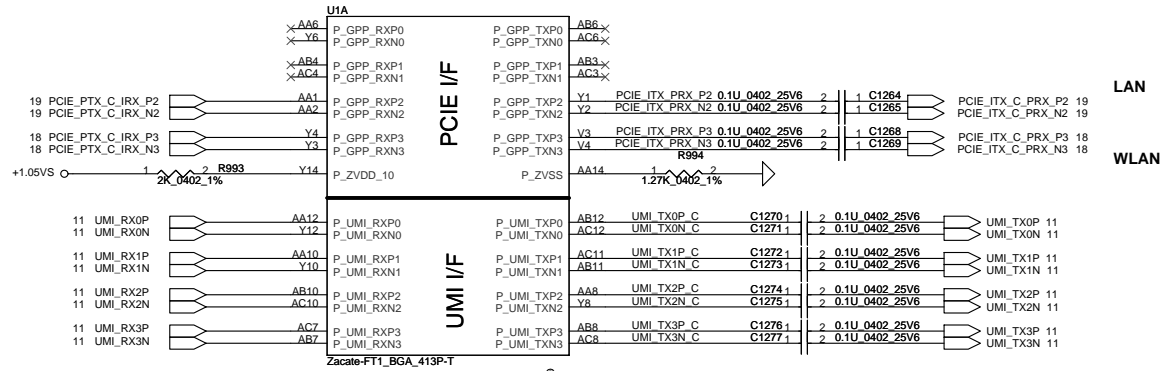
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+3VL	Smart Battery 16H		0001 011X b

## EC SM Bus2 address

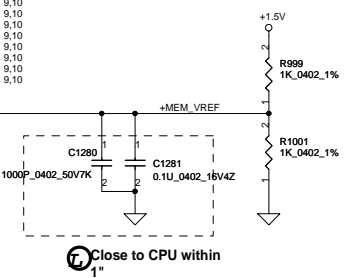
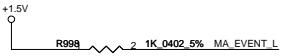
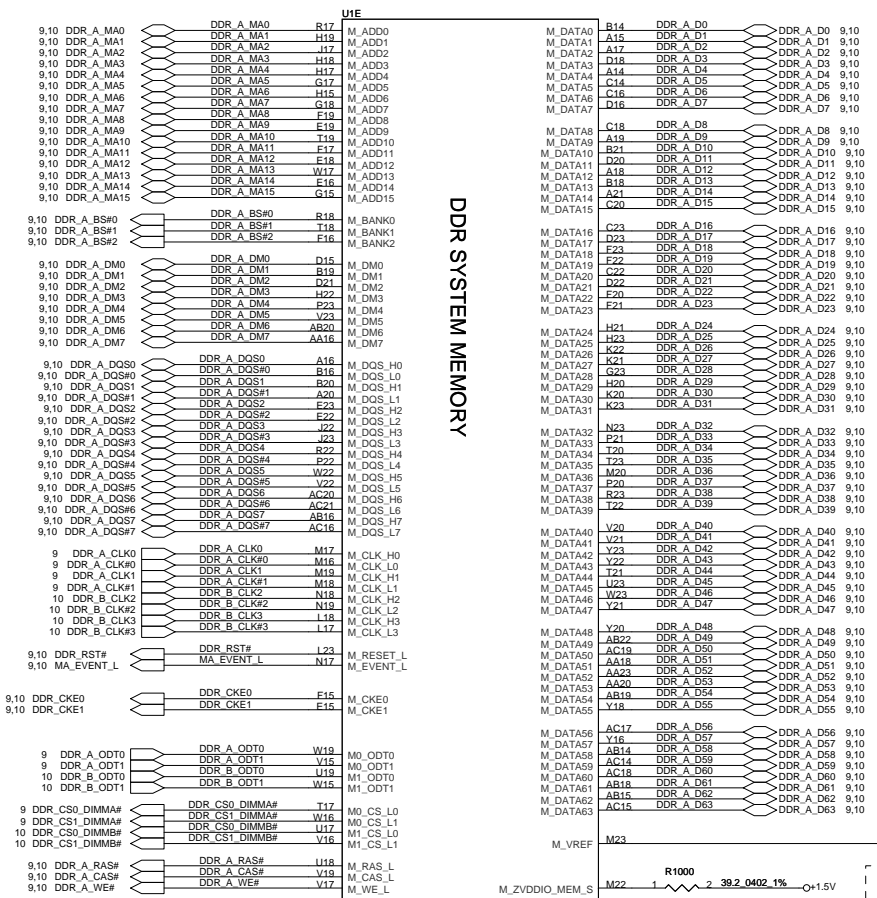
Power	Device	HEX	Address
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## SMBUS Control Table

	SOURCE	BATT	SODIMM I/II	CRT DDC ROM	WLAN	LCD DDC ROM	APU
EC_SMB_CK1 EC_SMB_DA1	KB926	V					
EC_SMB_CK2 EC_SMB_DA2	KB926						V
LCD_EDID_CLK LCD_EDID_DATA	APU FT1					V	
D_DDCCLK D_DDCDATA	APU FT1			V			
FCH_SMCLK0 FCH_SMDAT0	FCH M1		V				
FCH_SMCLK1 FCH_SMDAT1	FCH M1				V		

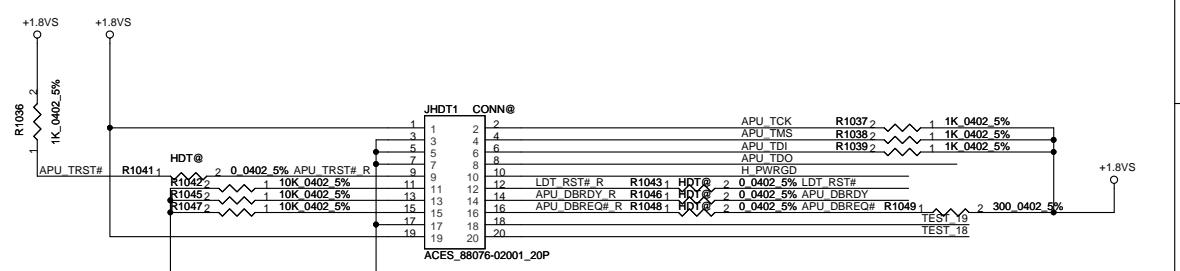
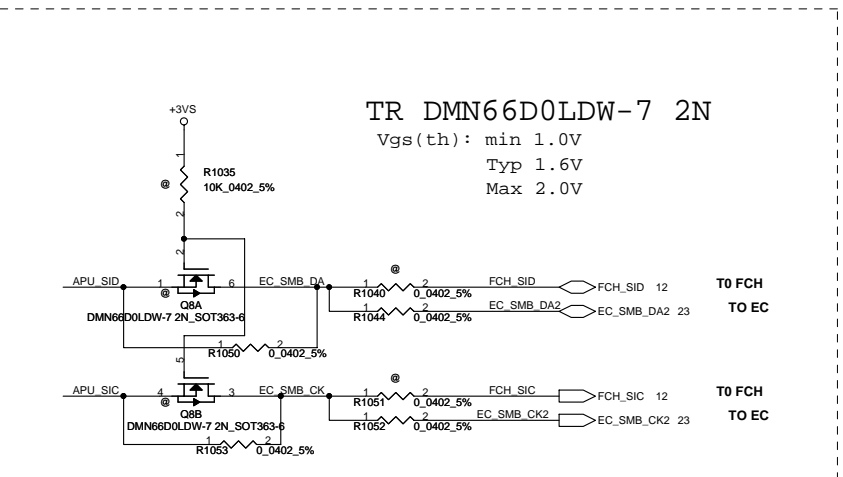
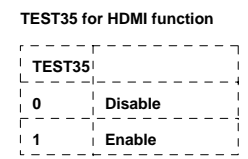
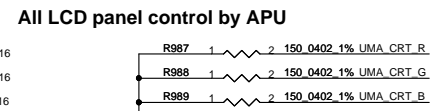
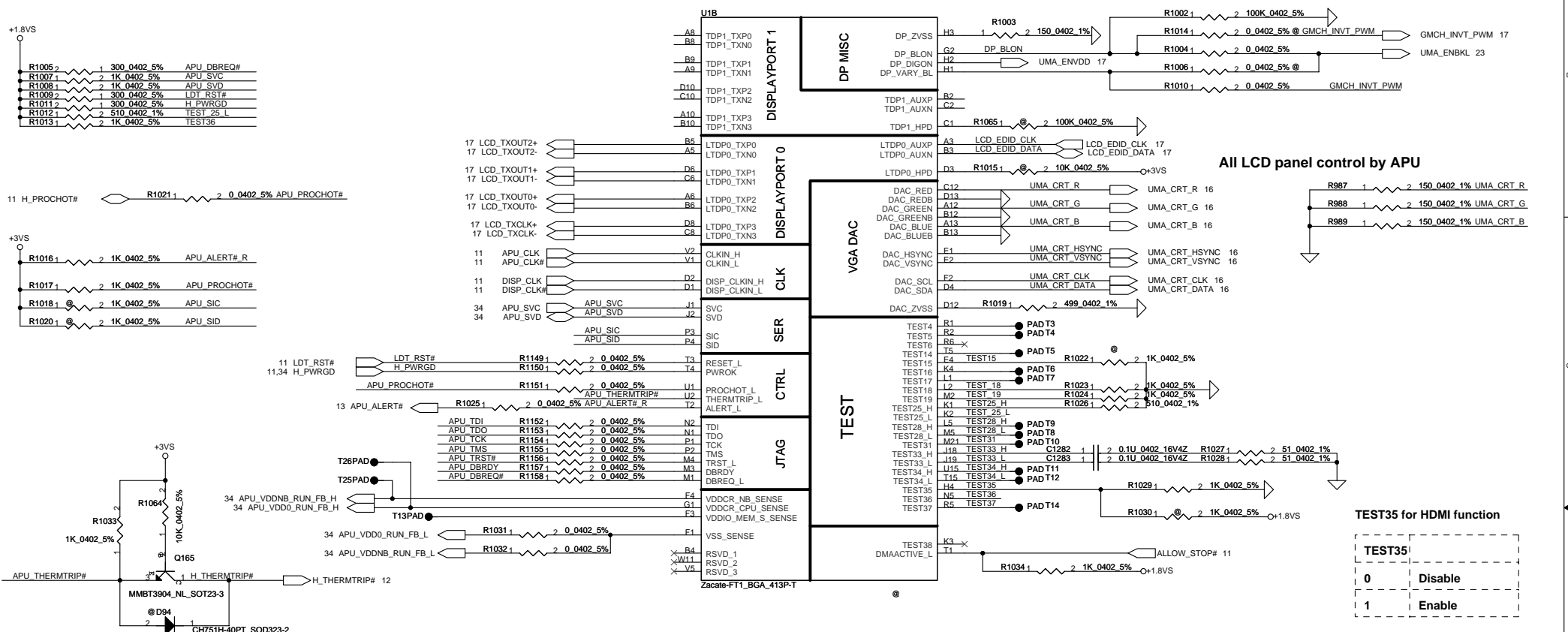


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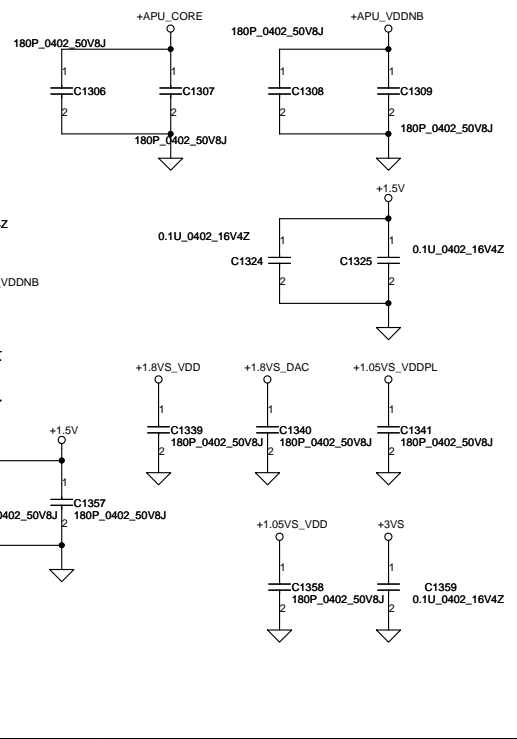
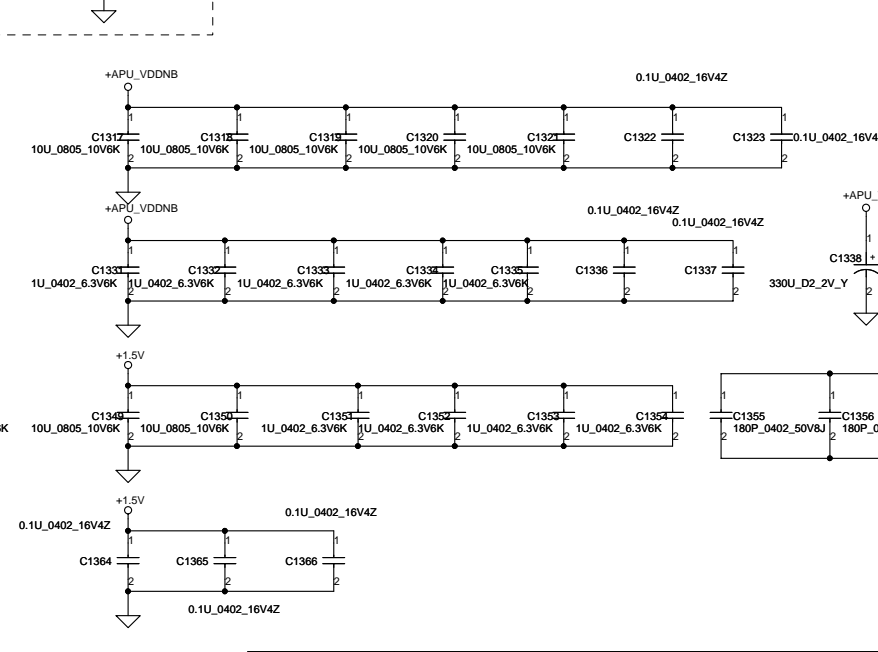
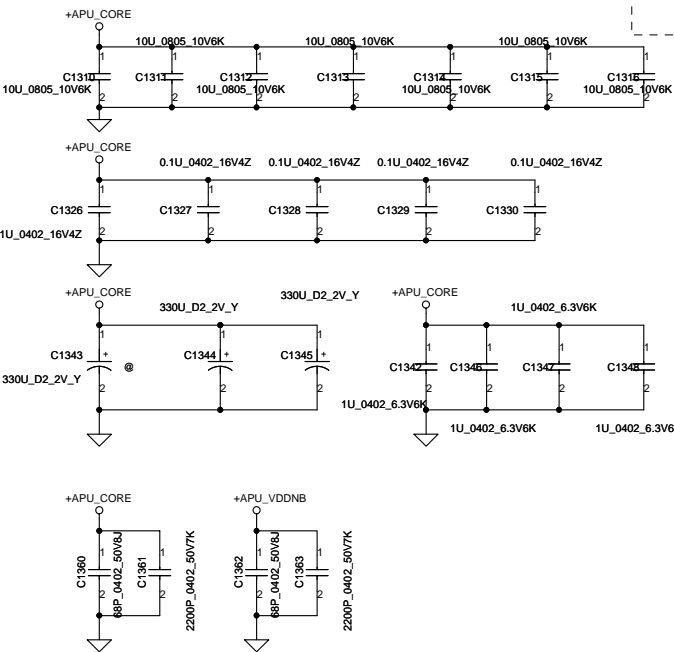
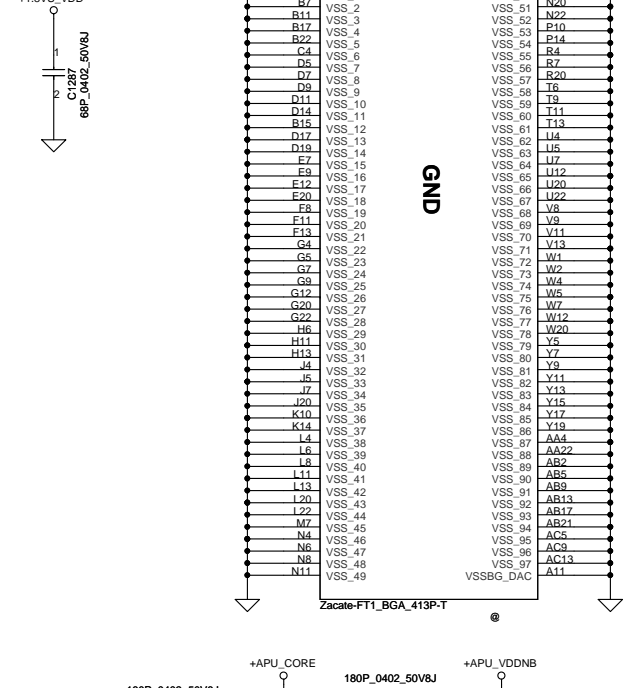
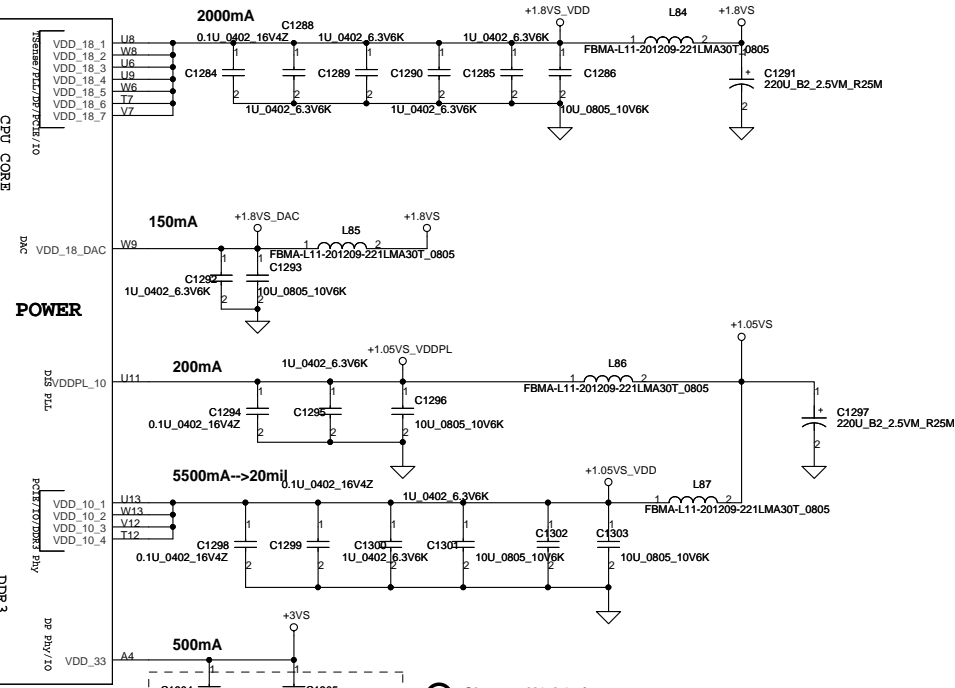
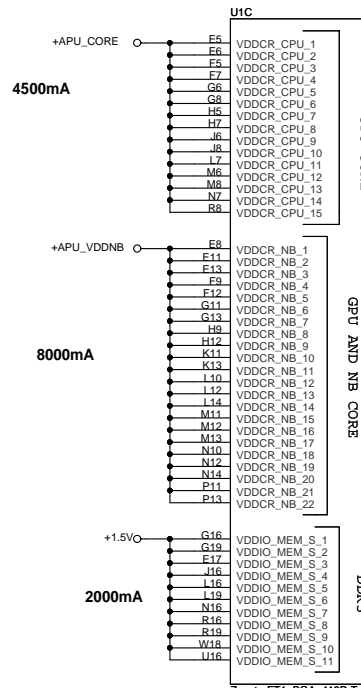


Zscate-FT1\_BGA\_413P-T

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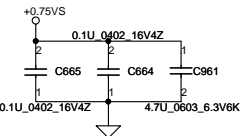
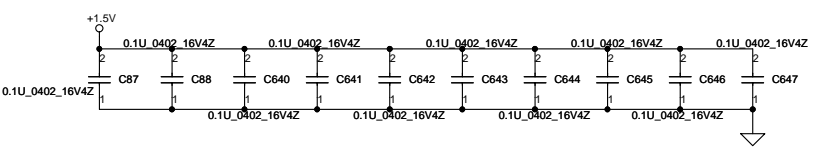
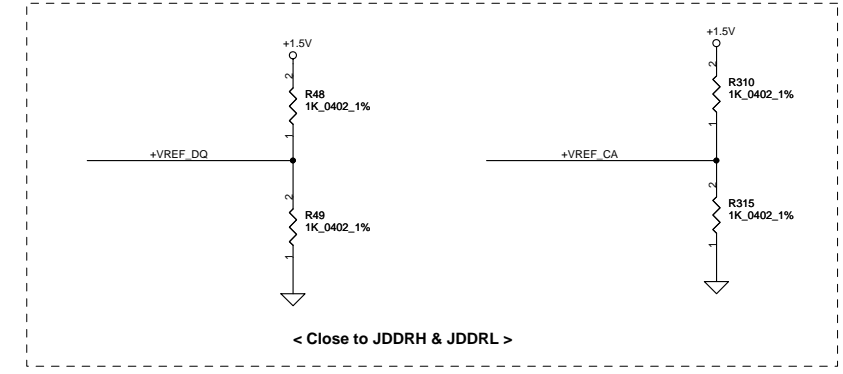
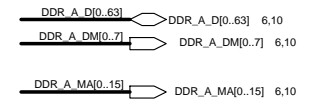
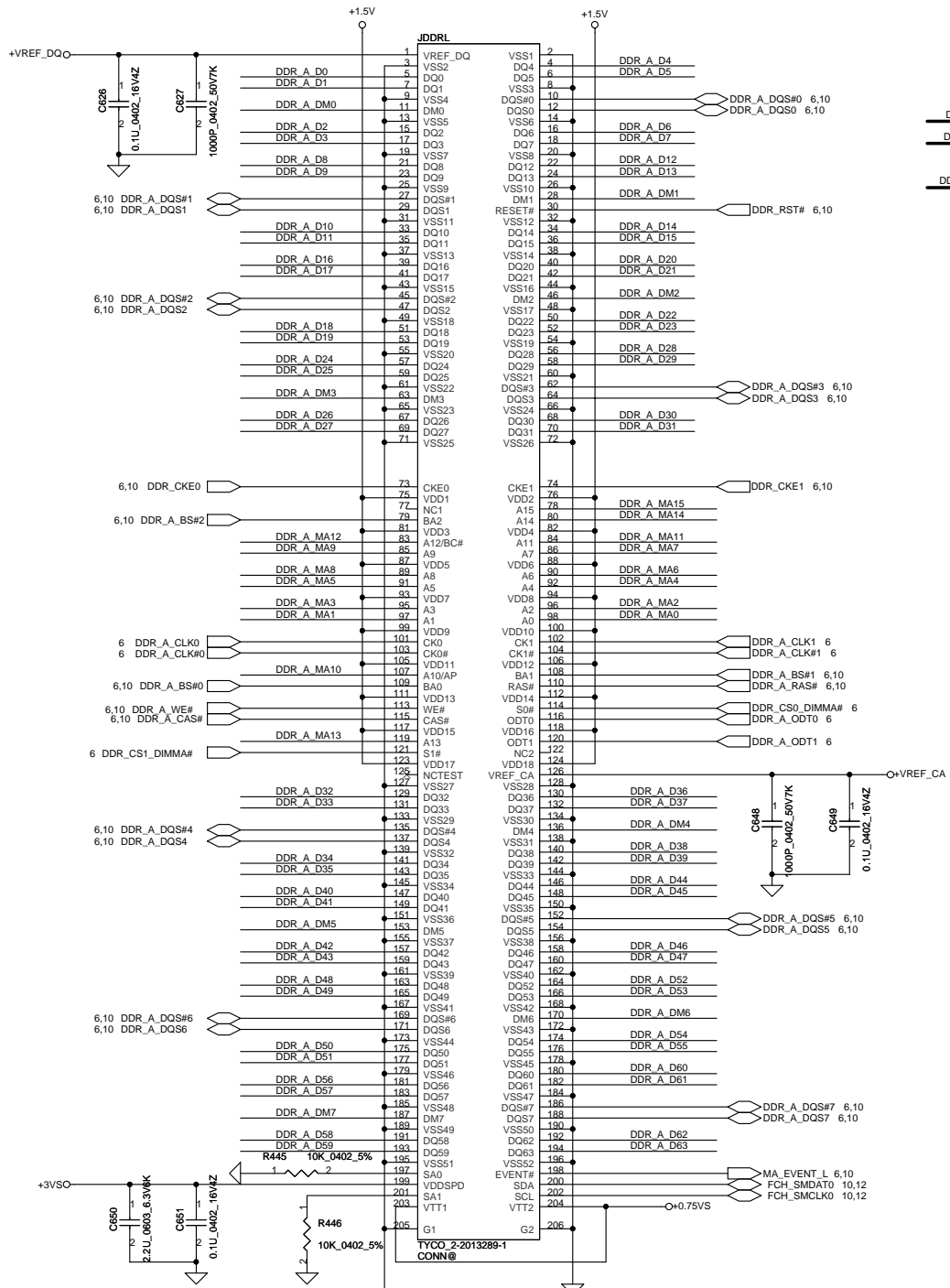
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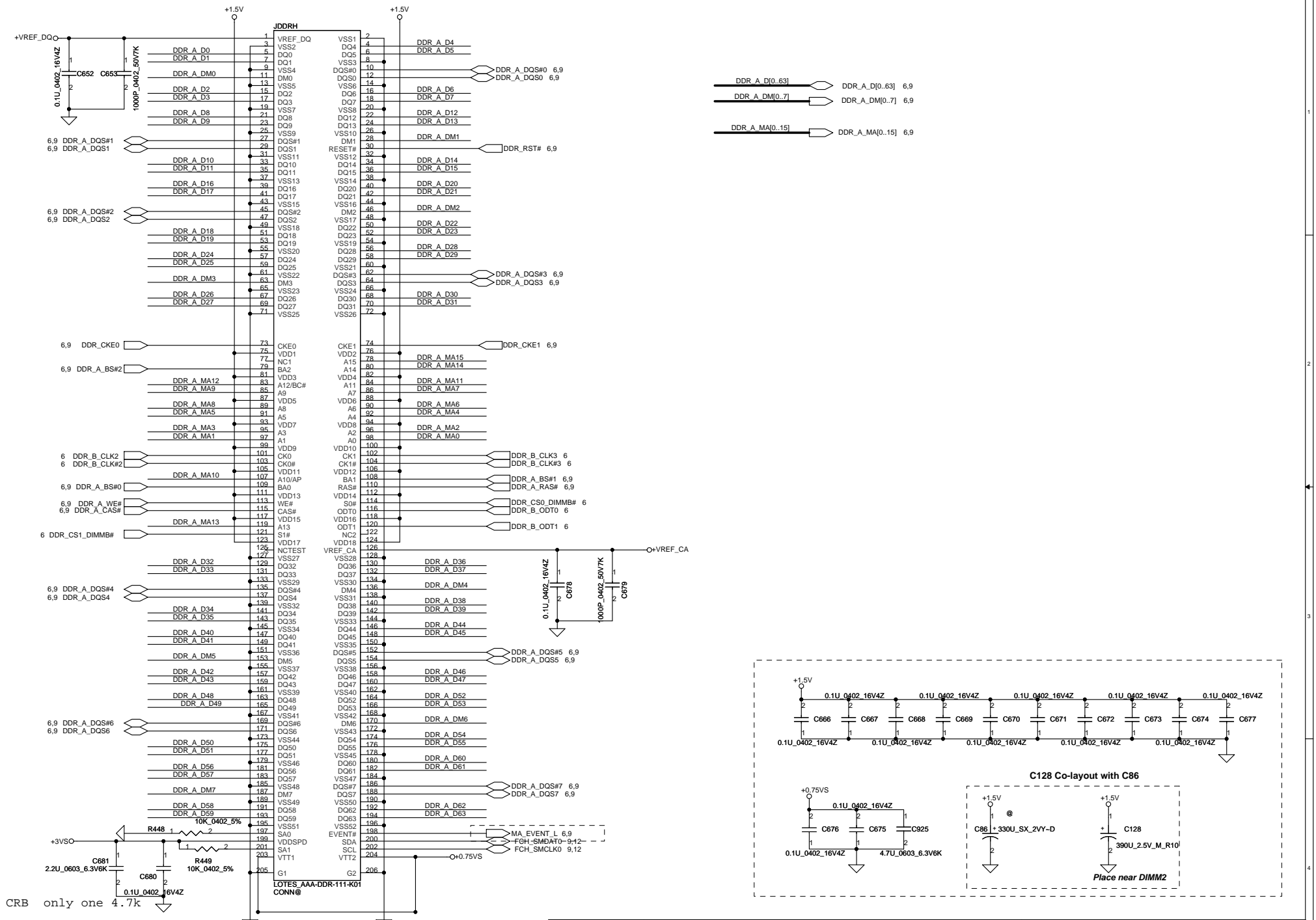
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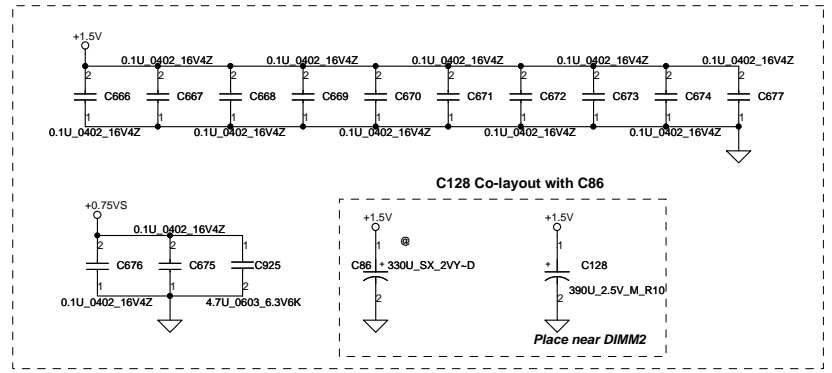
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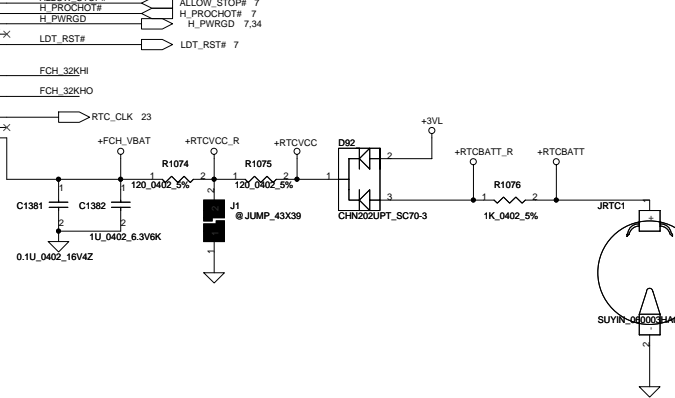
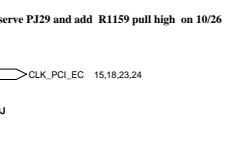
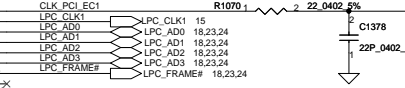
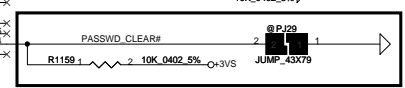
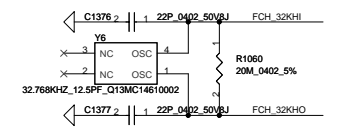
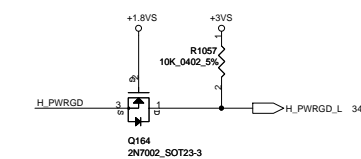
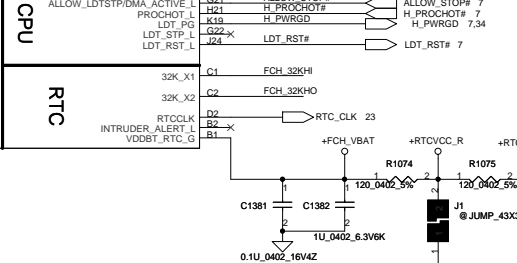
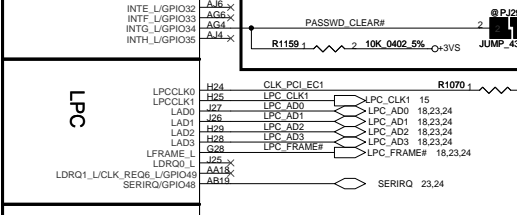
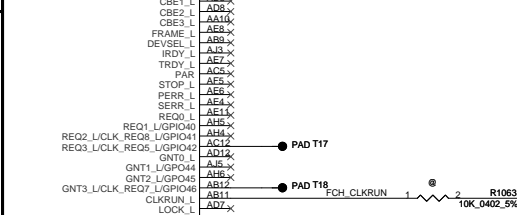
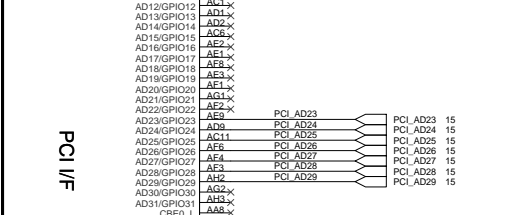
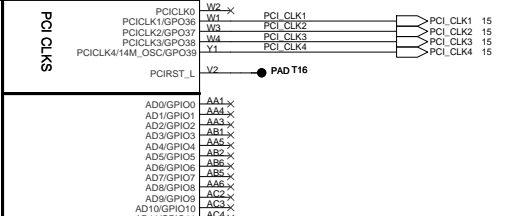
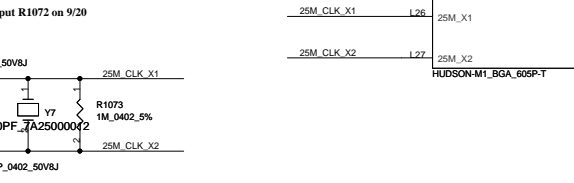
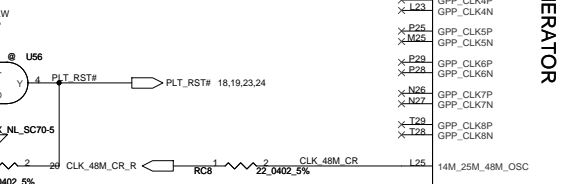
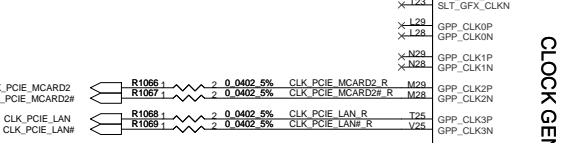
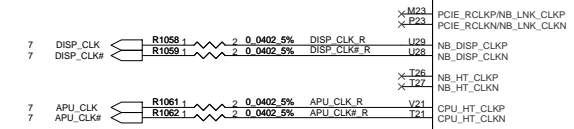
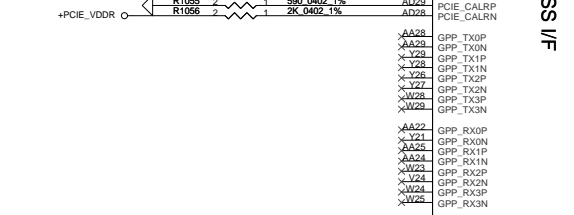
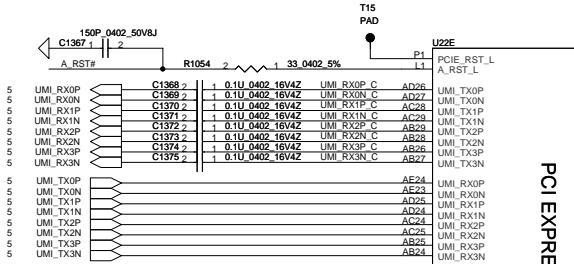
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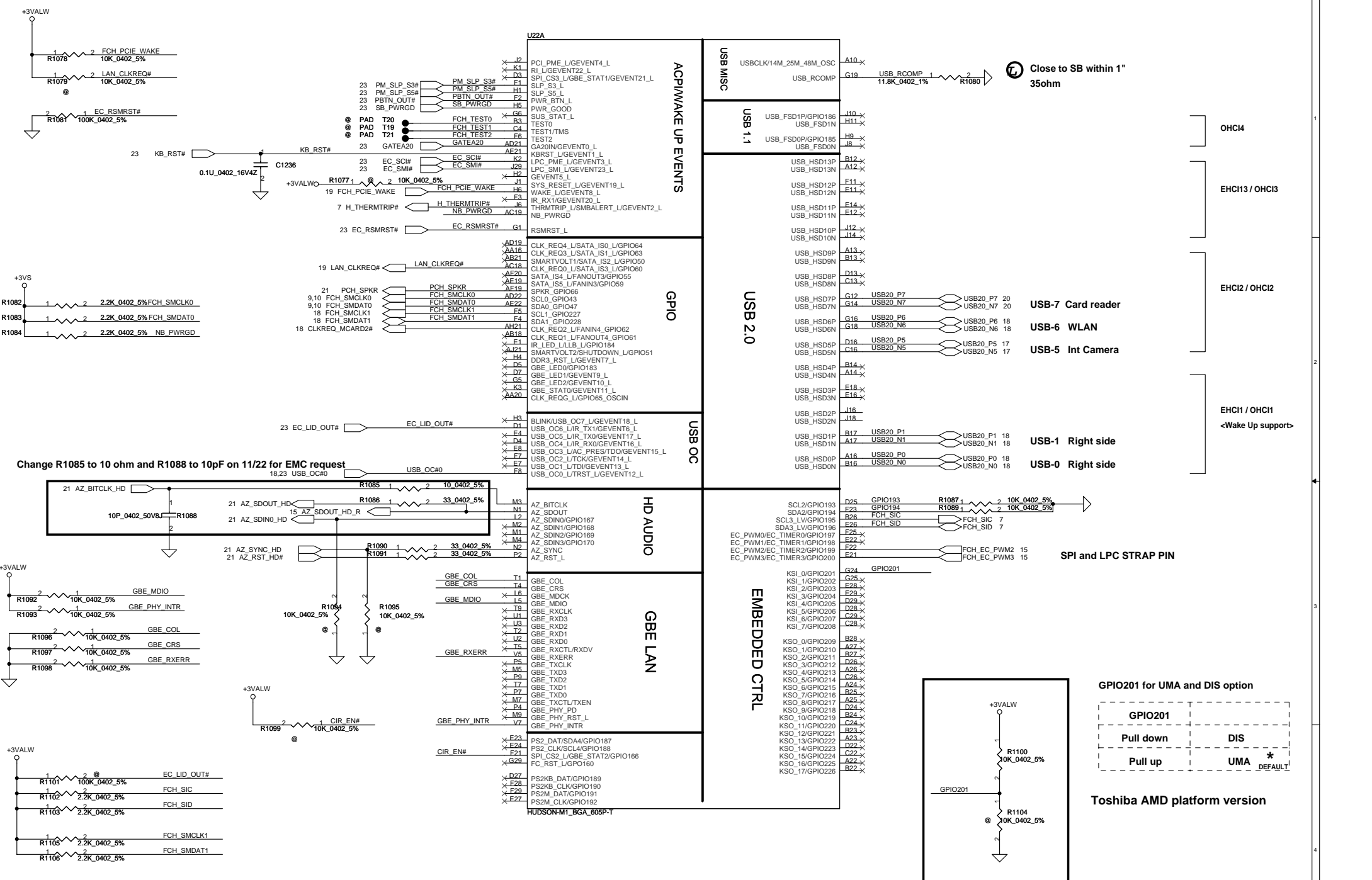


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Close to SB within 1" 35ohm

USB-7 Card reader

USB-6 WLAN

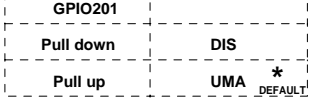
USB-5 Int Camera

USB-1 Right side

USB-0 Right side

SPI and LPC STRAP PIN

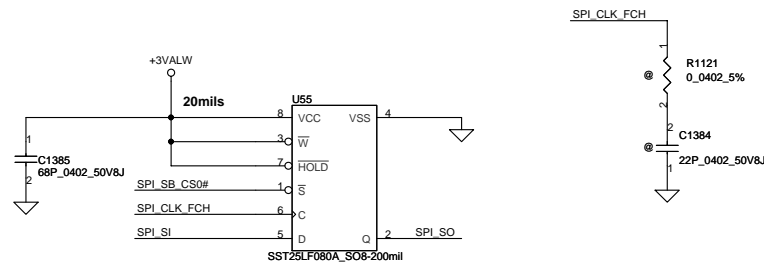
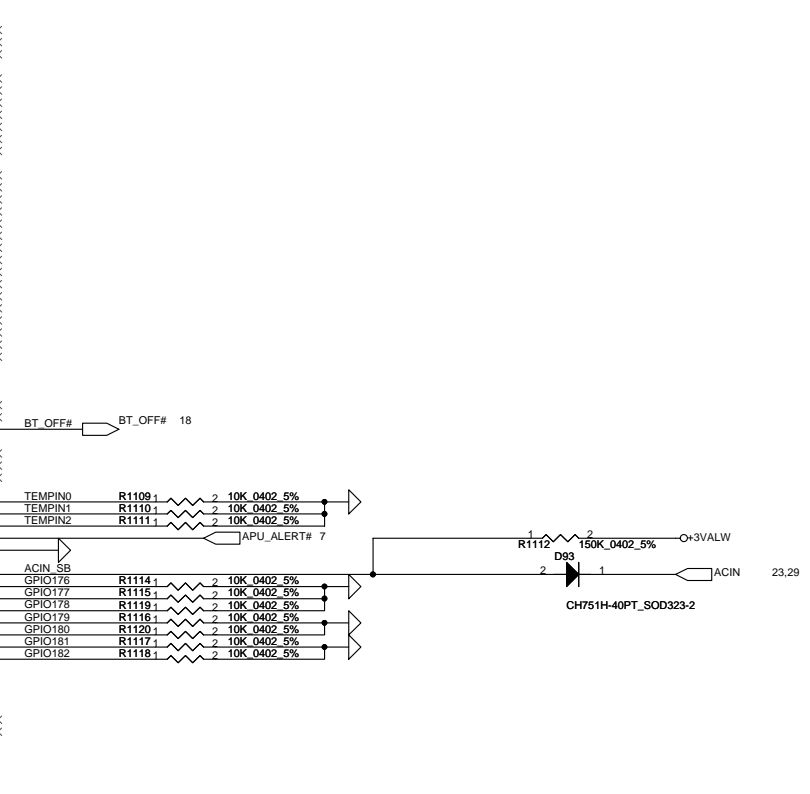
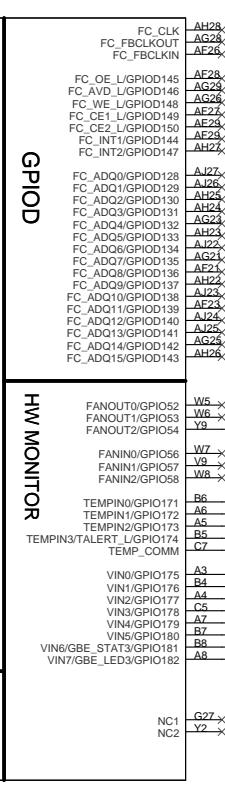
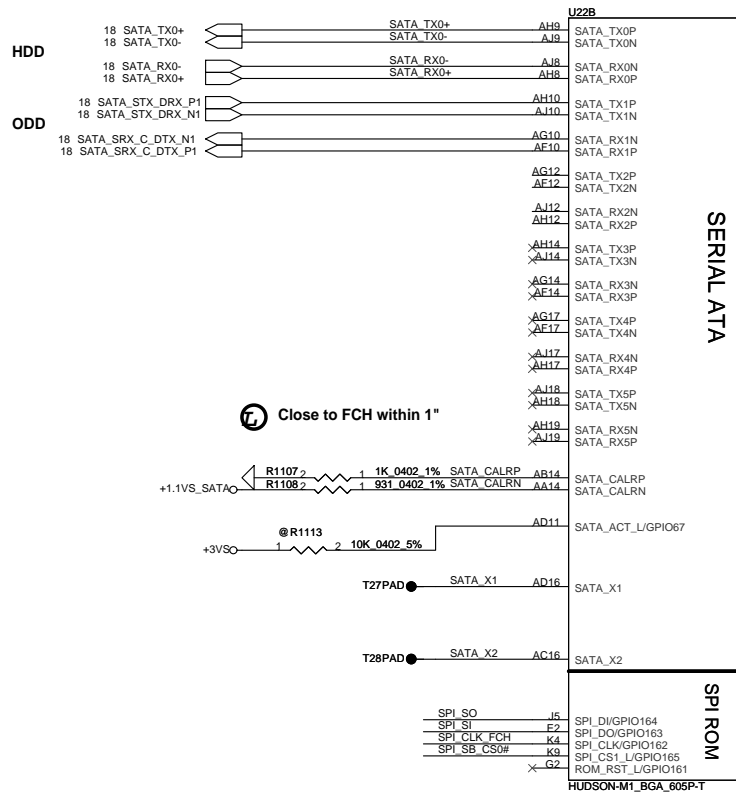
GPIO201 for UMA and DIS option



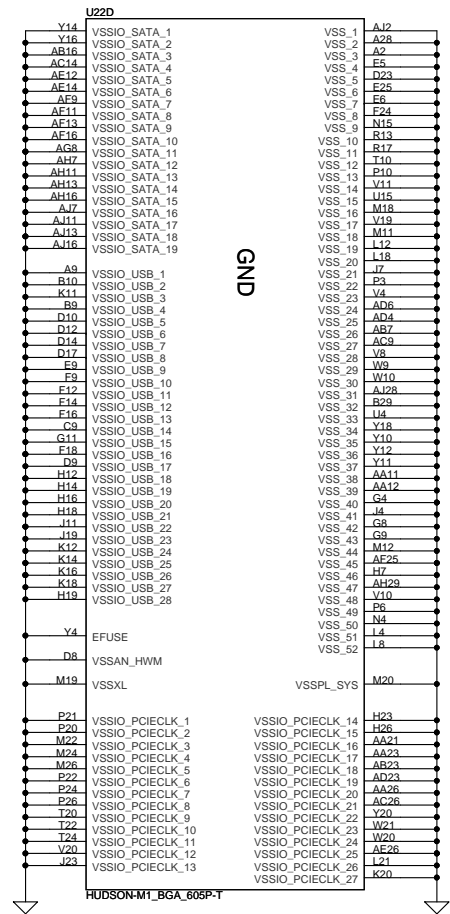
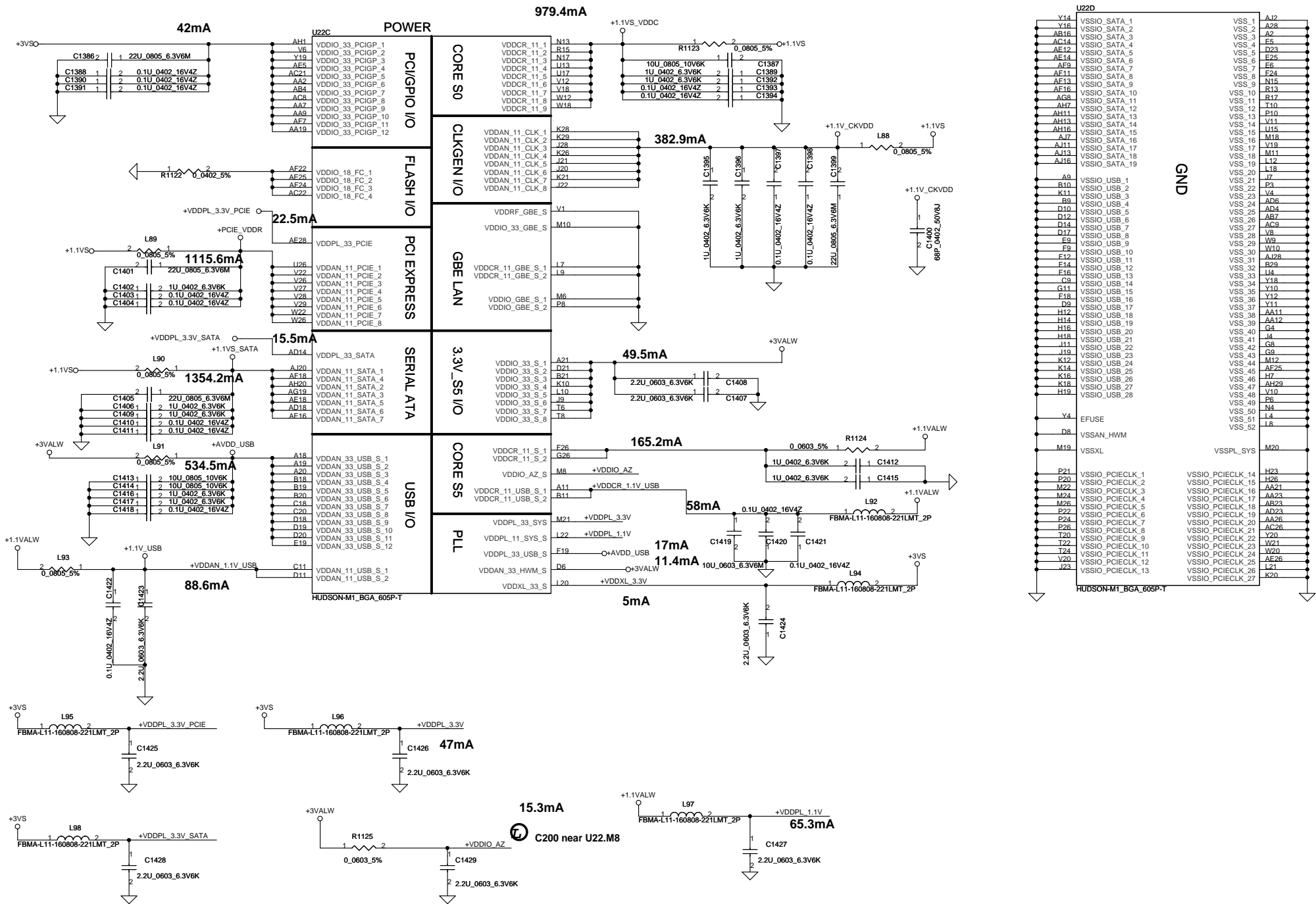
Toshiba AMD platform version

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**SCHMATIC, MB A6849**



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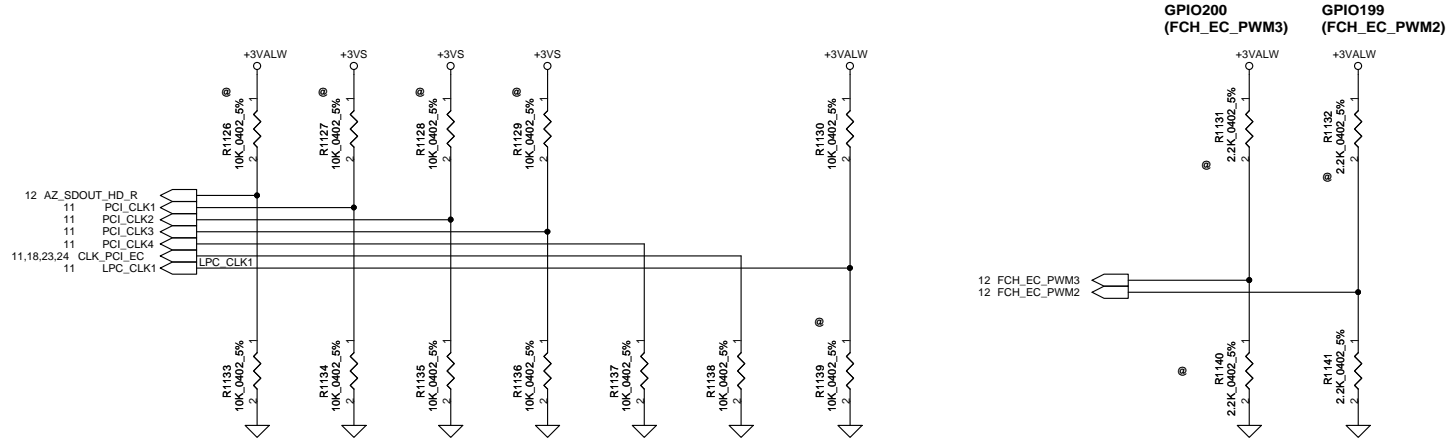
# REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1
<b>PULL HIGH</b>	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Disable	EC ENABLE	CLOCKGEN ENABLE
							* DEFAULT
<b>PULL LOW</b>	Performance MODE	FORCE PCIE GEN1	WATCHDOG TIMER DISABLE	IGNORE DEBUG STRAP	Inter CLK Gen Mode Enable	EC DISABLE	CLOCKGEN DISABLE
	* DEFAULT	* DEFAULT	* DEFAULT	* DEFAULT	* DEFAULT	* DEFAULT	

	GPIO200 (FCH_EC_PWM3)	GPIO199 (FCH_EC_PWM2)
Reserved	2.2k pull down	2.2k pull down
* SPI	Not contact	2.2k pull down
LPC	2.2k pull down	Not contact
Reserved	Not contact	Not contact

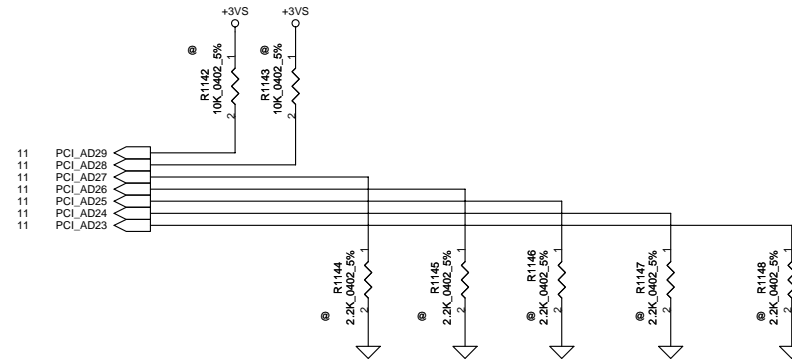
DEFAULT



# DEBUG STRAPS

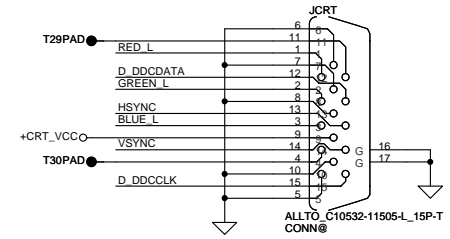
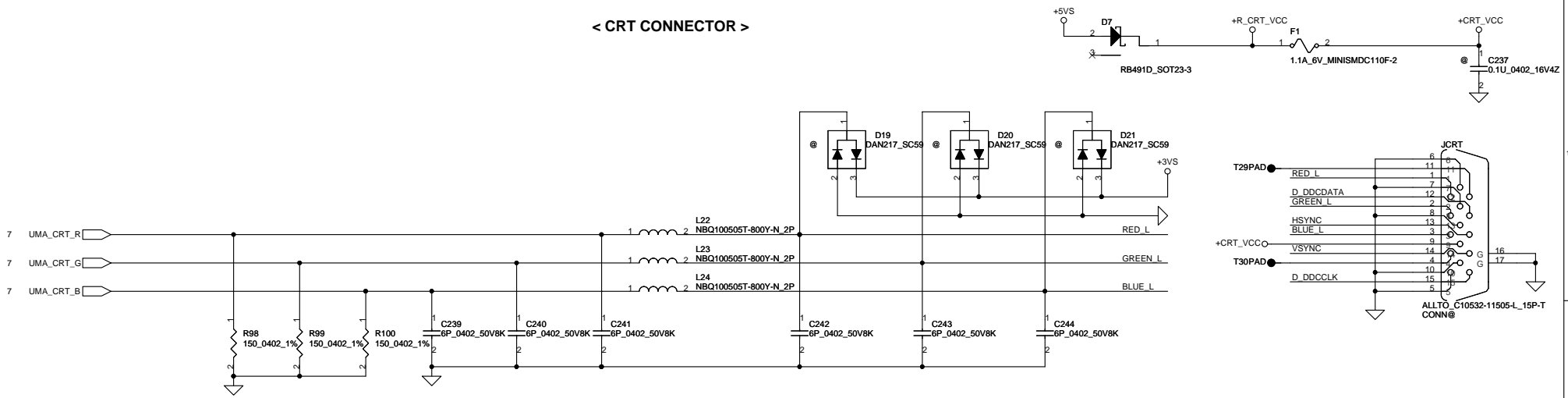
M1 HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

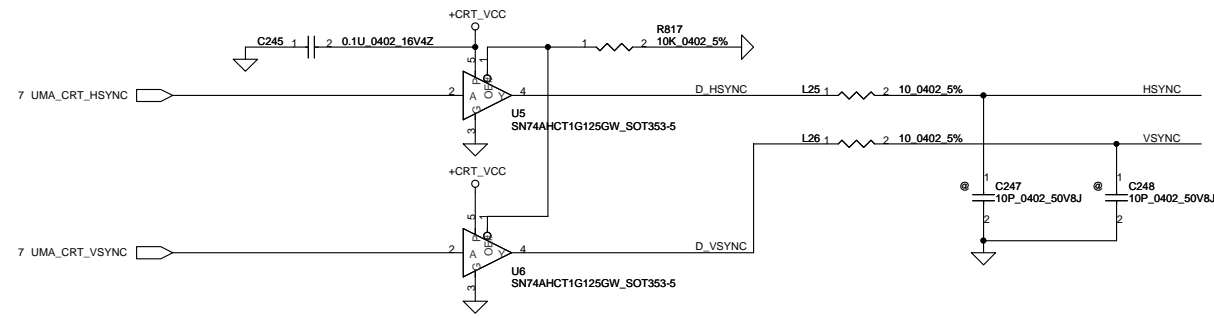


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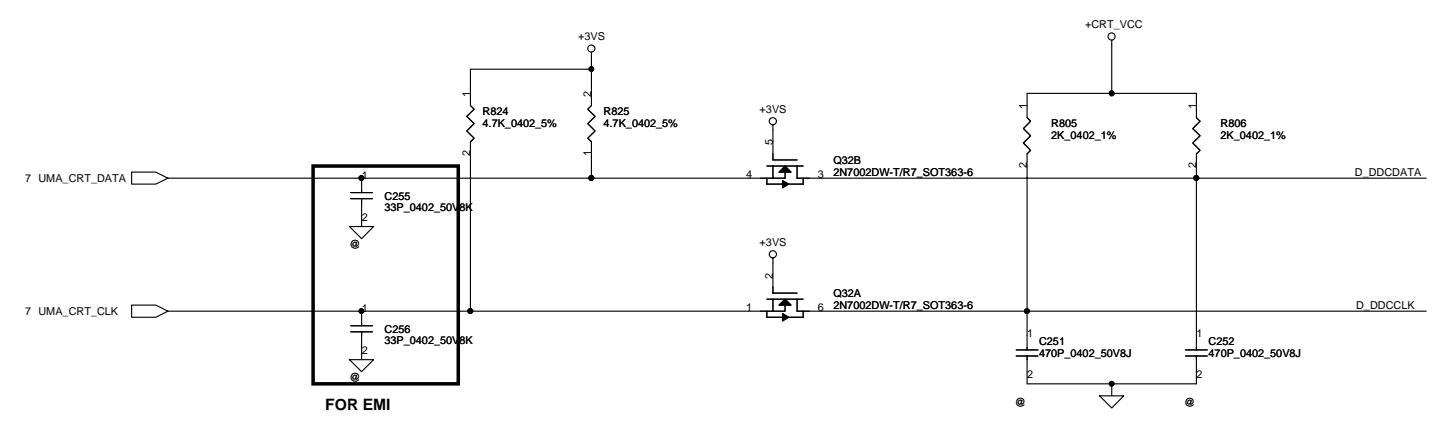
< CRT CONNECTOR >



< SYNC SIGNAL >



< Display Data Channel >



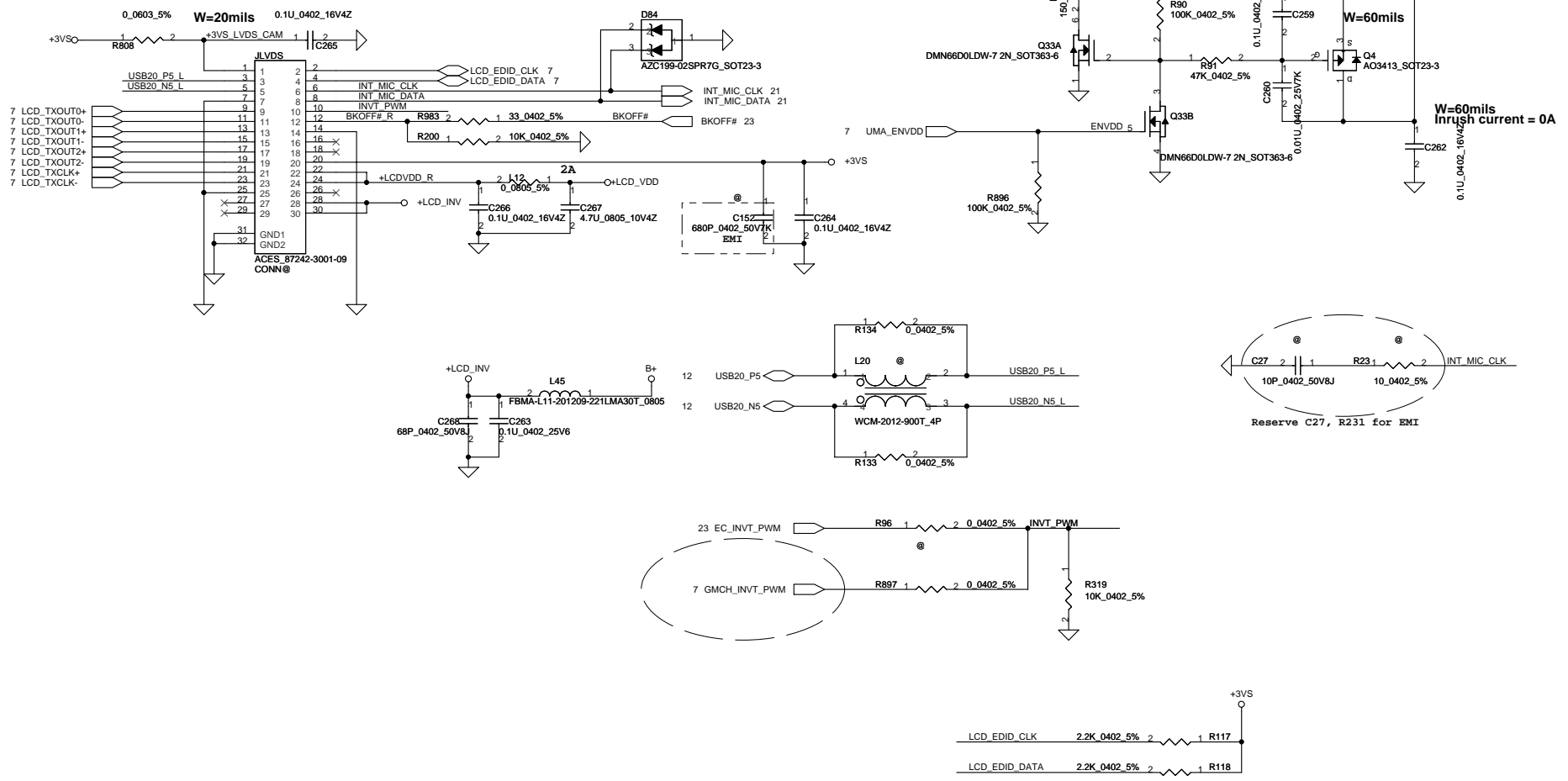
FOR EMI

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SCHMATICS, MB A6849

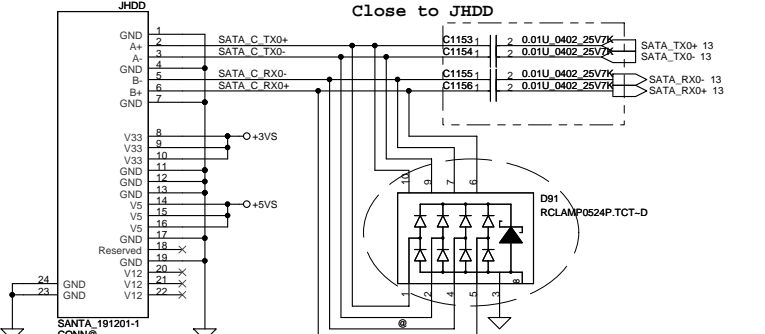
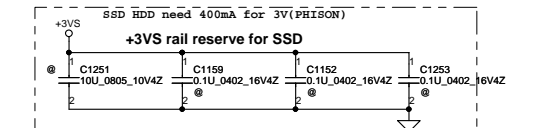
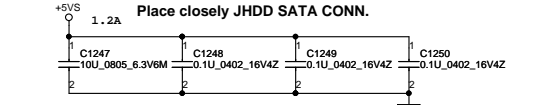


# LCD/PANEL BD. Conn.

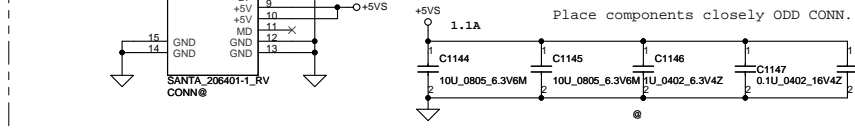
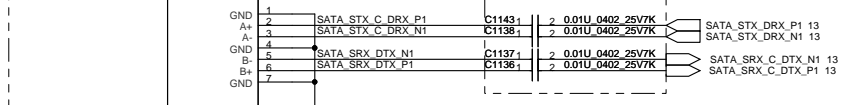


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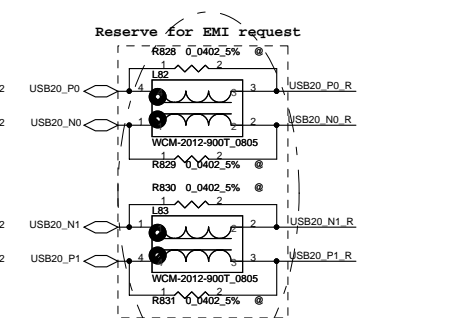
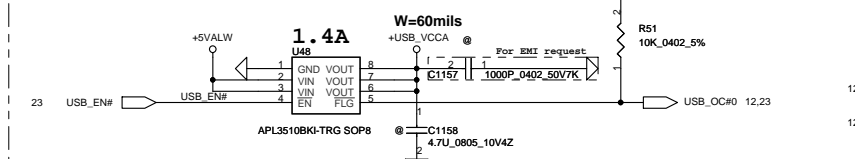
# SATA HDD Conn.



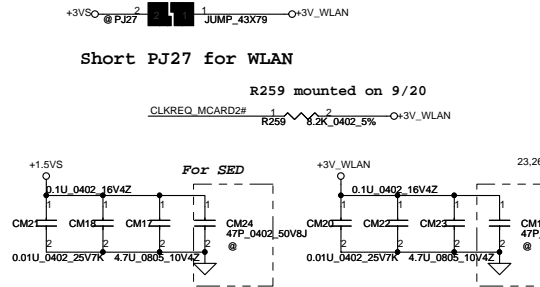
# SATA ODD Conn



# USB Port 0 & Port 1



# Slot#1 Half PCIe Mini Card-WLAN

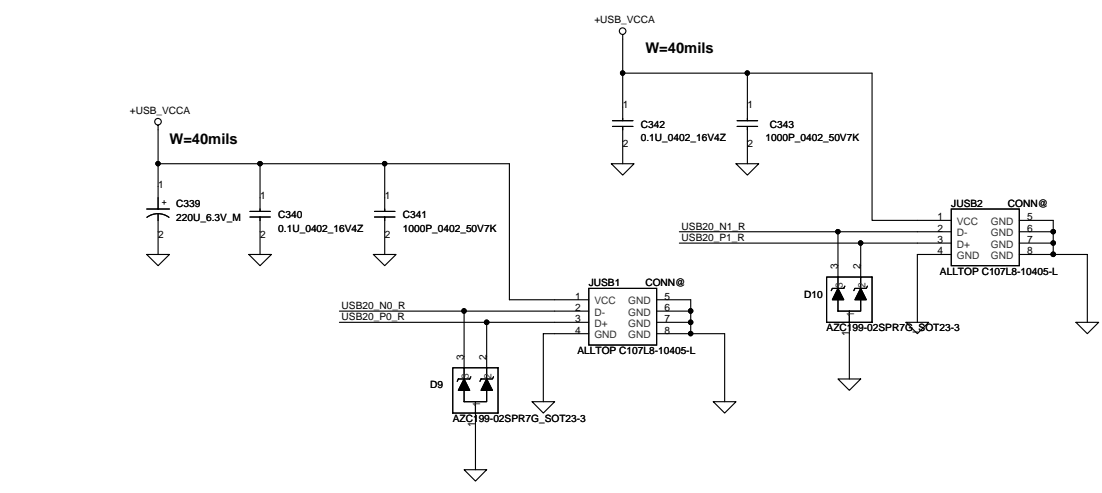
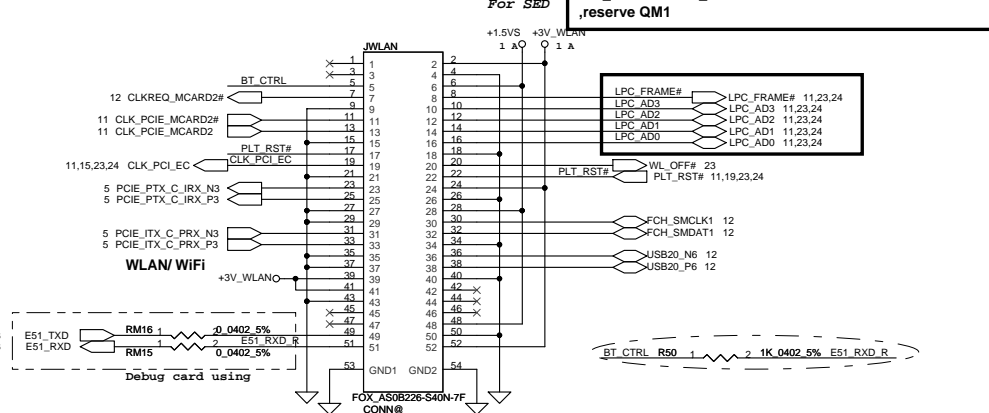


WLAN&BT Combo module circuits

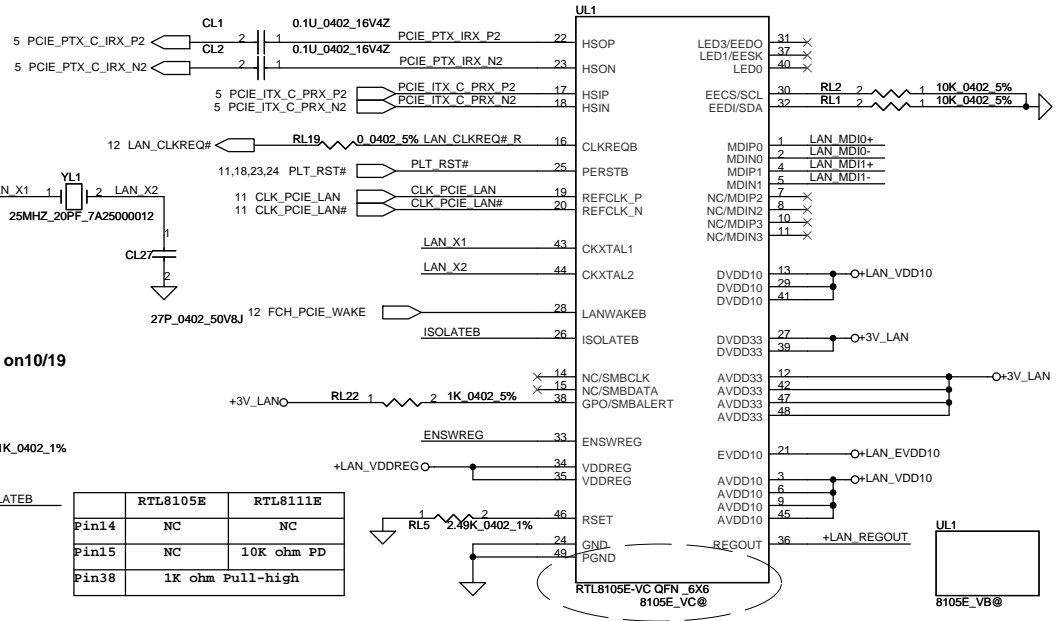
	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_PWR#	L	H

\*\*If +3V\_WLAN is +3VS, please remove DM2

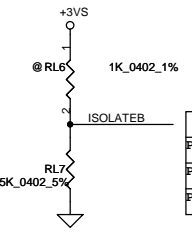
Add R316 to bypass BT\_OFF#; change control pin from BT\_PWR# to BT\_OFF# on 9/26, reserve QM1



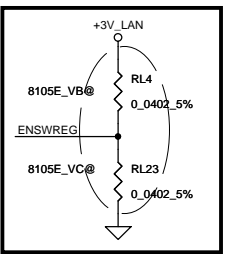
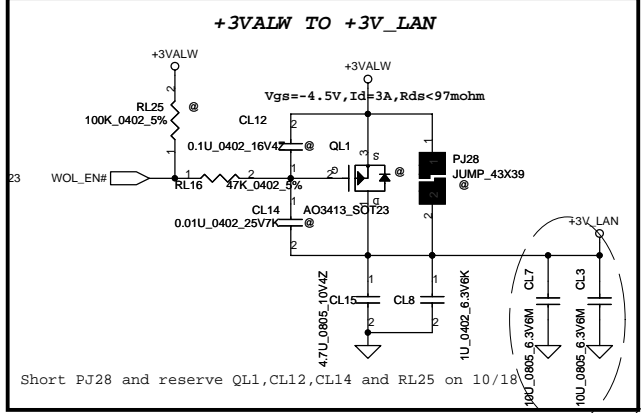
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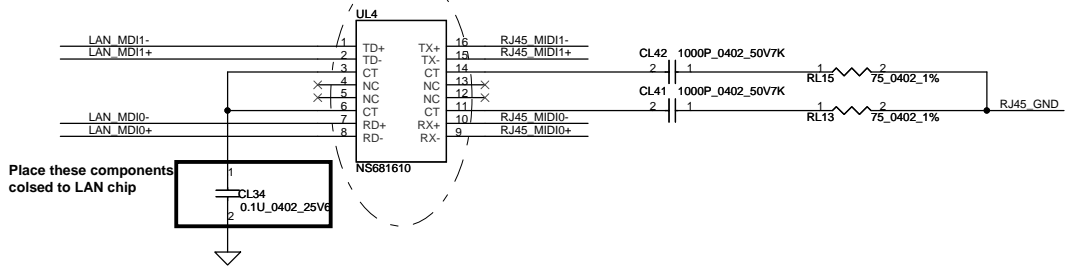
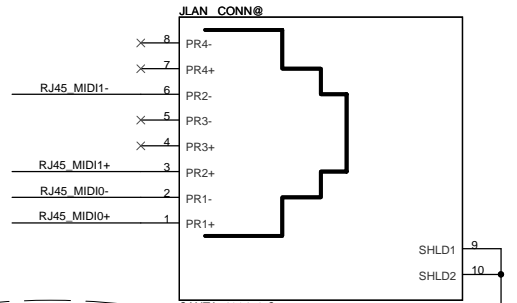
Reserve RL6 on10/19



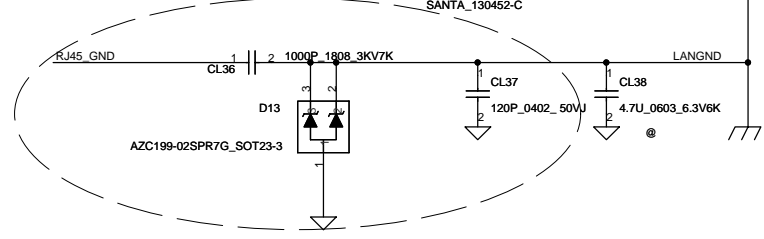
	RTL8105E	RTL8111E
Pin14	NC	NC
Pin15	NC	10K ohm PD
Pin38	1K ohm Pull-high	



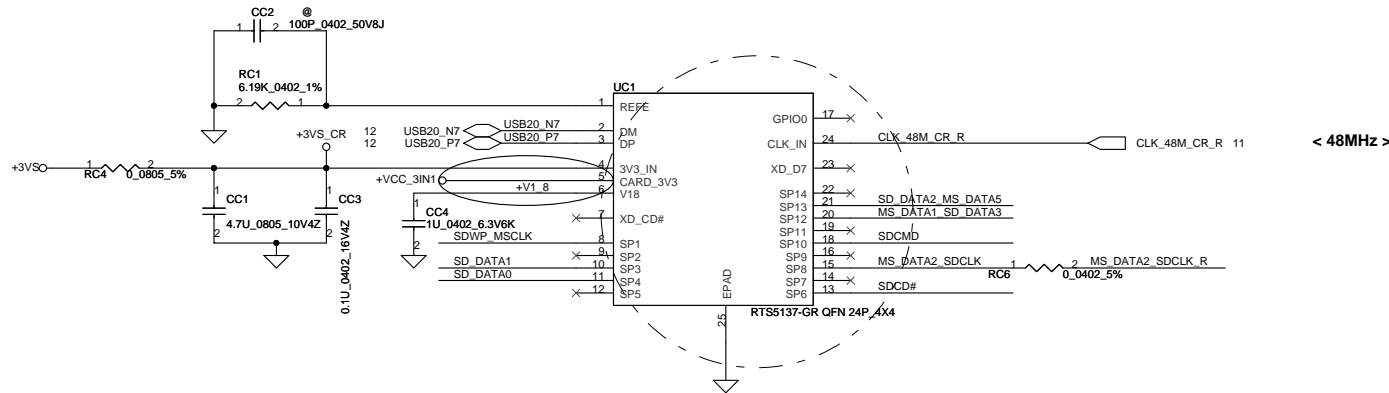
LAN Conn.



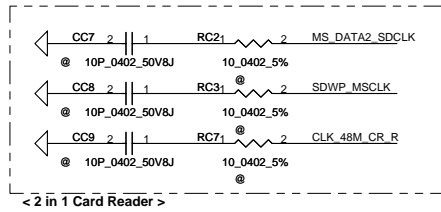
Place these components coiled to LAN chip



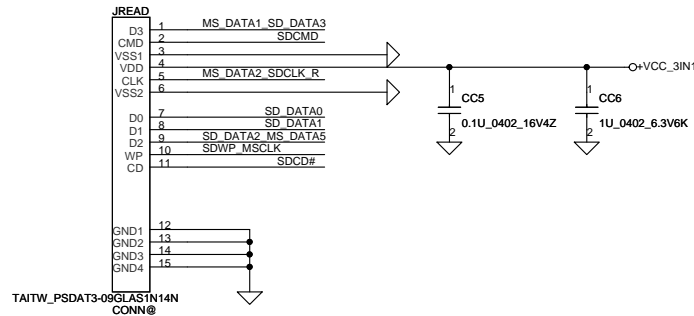
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for EMI request

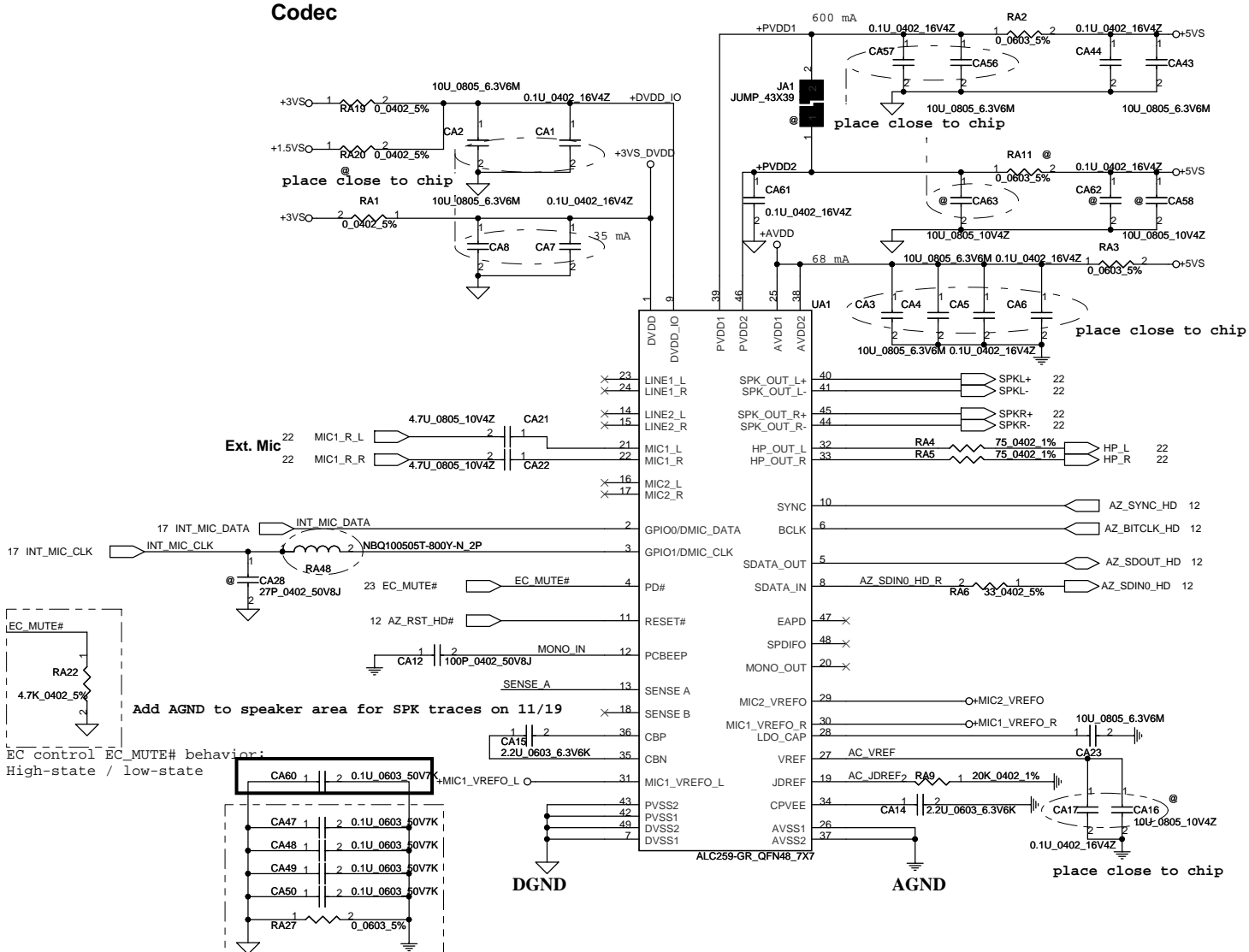


< 2 in 1 Card Reader >

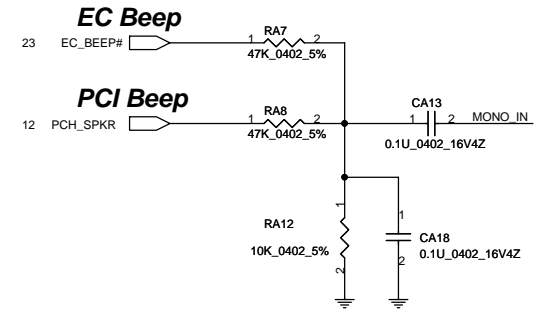


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# Codec

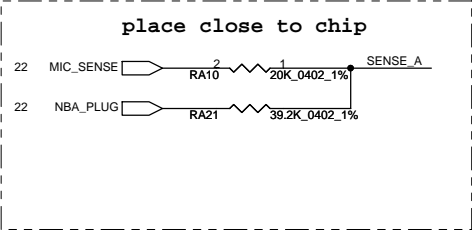


## Beep sound



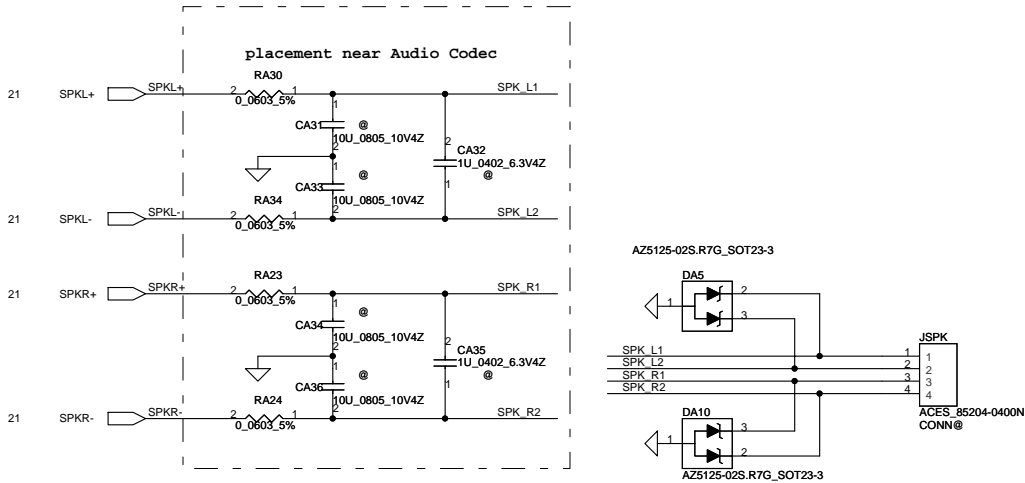
EC control EC\_MUTE# behavior:  
High-state / low-state

Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

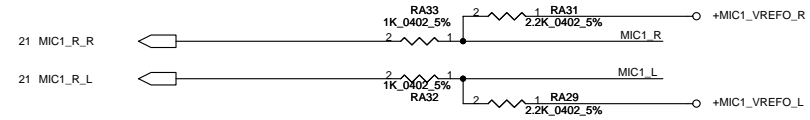


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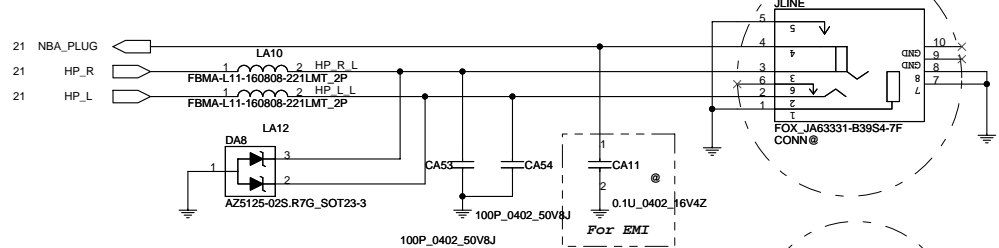
### Speaker Connector



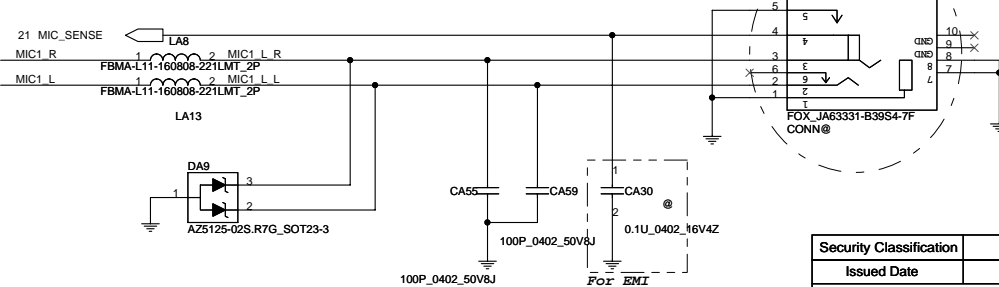
### Ext.MIC/LINE IN JACK



### HeadPhone/LINE Out JACK

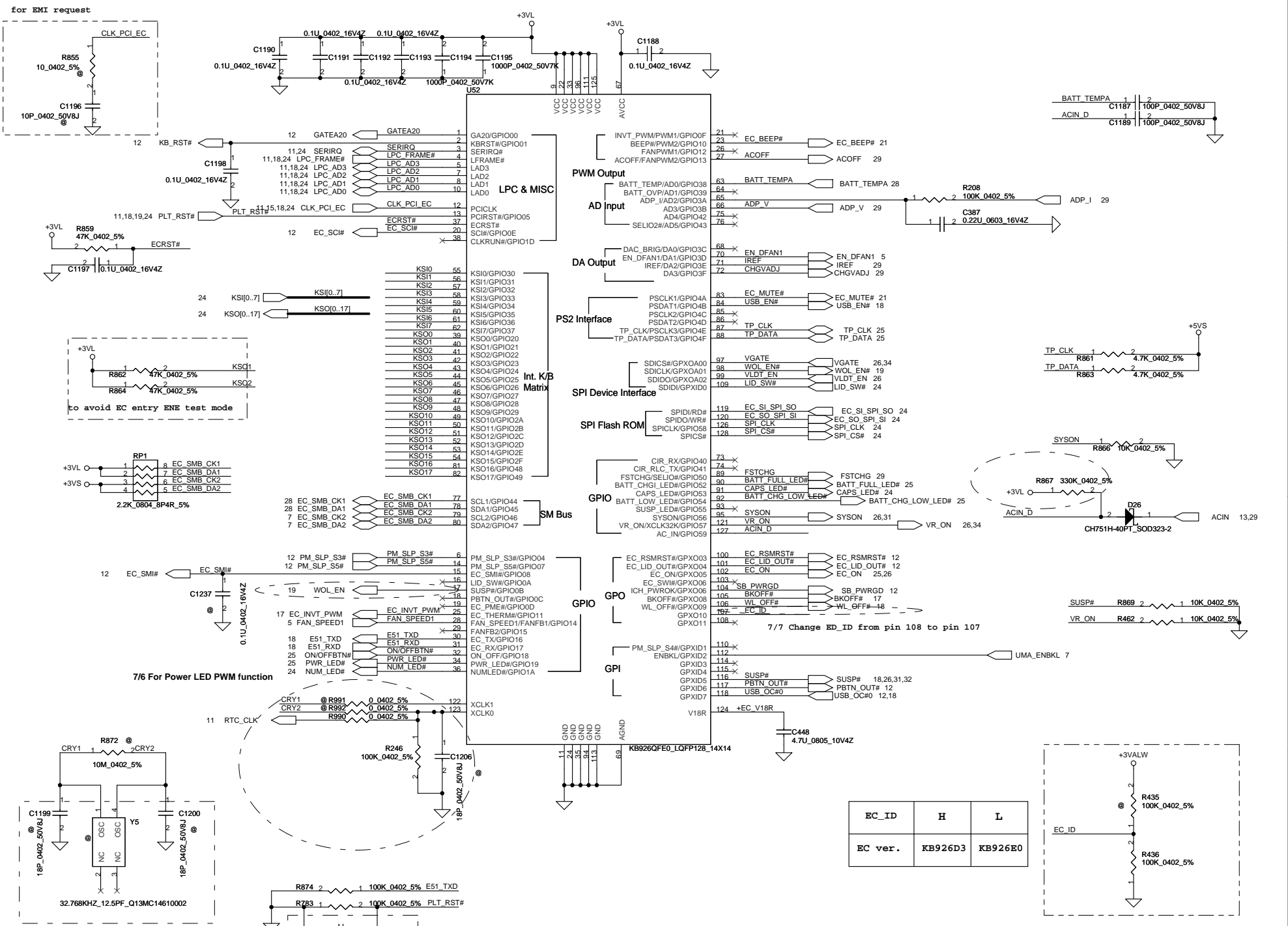


### Ext.MIC/LINE IN JACK



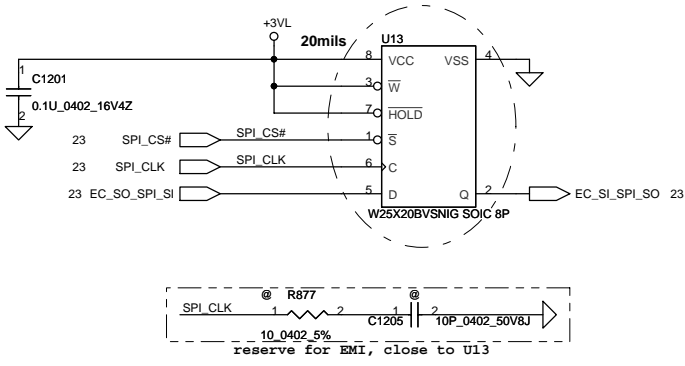
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**SCHEMATICS, MB A6849**

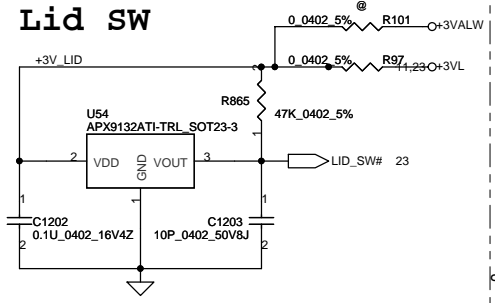


EC_ID	H	L
EC ver.	KB926D3	KB926E0

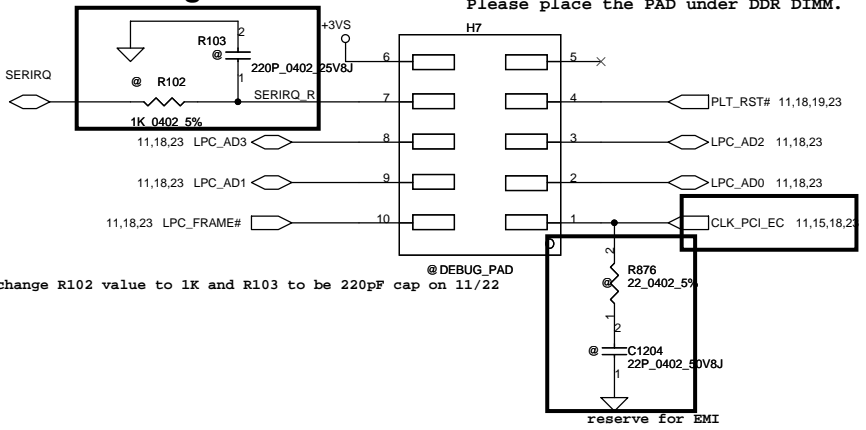
# SPI Flash (256KB)



# Lid SW

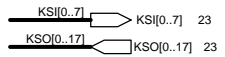


# LPC Debug Port



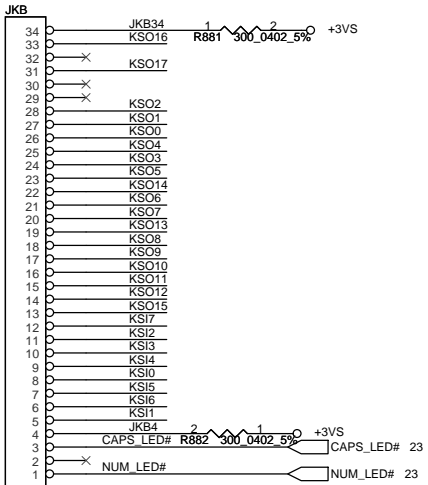
# KEYBOARD CONN.

Notice:KB Connector Pin Definition Reversed with KB Membrane Pin Definition



please close to JKB1

KSO16	1	2	100P_0402_50V8J
KSO17	1	2	100P_0402_50V8J
KSO2	1	2	100P_0402_50V8J
KSO1	1	2	100P_0402_50V8J
KSO0	1	2	100P_0402_50V8J
KSO4	1	2	100P_0402_50V8J
KSO3	1	2	100P_0402_50V8J
KSO5	1	2	100P_0402_50V8J
KSO14	1	2	100P_0402_50V8J
KSO6	1	2	100P_0402_50V8J
KSO7	1	2	100P_0402_50V8J
KSO13	1	2	100P_0402_50V8J
KSO8	1	2	100P_0402_50V8J
KSO9	1	2	100P_0402_50V8J
KSO10	1	2	100P_0402_50V8J
KSO11	1	2	100P_0402_50V8J
KSO12	1	2	100P_0402_50V8J
KSO15	1	2	100P_0402_50V8J
KSI7	1	2	100P_0402_50V8J
KSI2	1	2	100P_0402_50V8J
KSI3	1	2	100P_0402_50V8J
KSI4	1	2	100P_0402_50V8J
KSI0	1	2	100P_0402_50V8J
KSI5	1	2	100P_0402_50V8J
KSI6	1	2	100P_0402_50V8J
KSI1	1	2	100P_0402_50V8J
CAPS_LED#	1	2	100P_0402_50V8J
NUM_LED#	1	2	100P_0402_50V8J

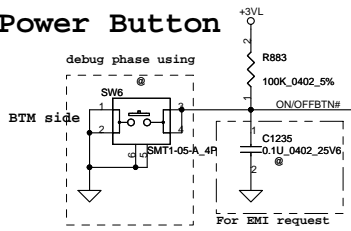


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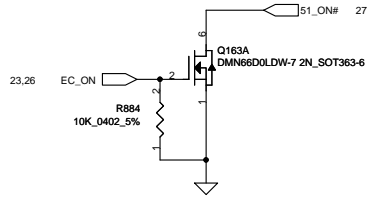
ACES\_88170-3400  
CONN@



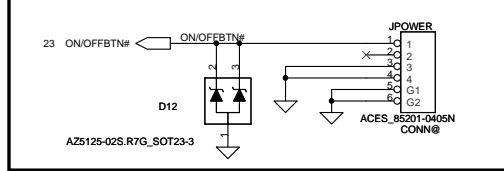
### Power Button



Q163A change part number from SB00000AR00 to SB00000DH00 on 9/15

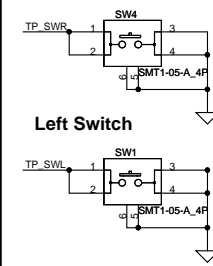


### < Power / B Connector >

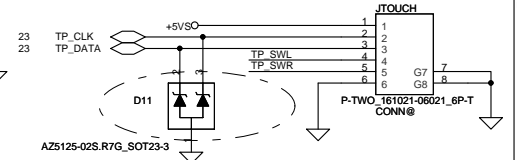
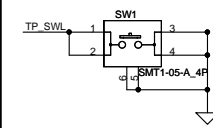


### < Touch / B Connector >

#### Right Switch

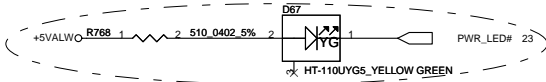


#### Left Switch



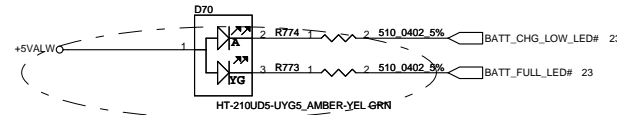
### POWER/SUSPEND LED

Vf=1.9V(typ), 2.4V(max)  
If=20mA(max)

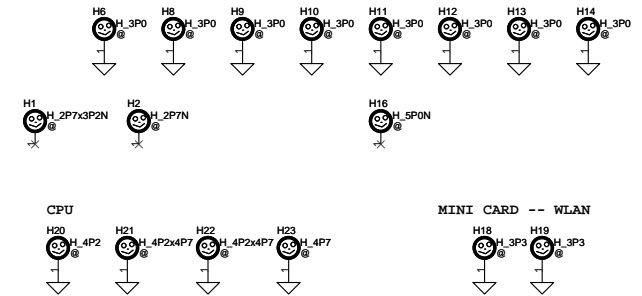


### DC IN/ BATT CHARGE

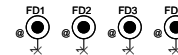
Vf=1.8V(typ), 2.0V(max) for amber  
Vf=1.8V(typ), 2.0V(max) for green  
If=20mA(max)



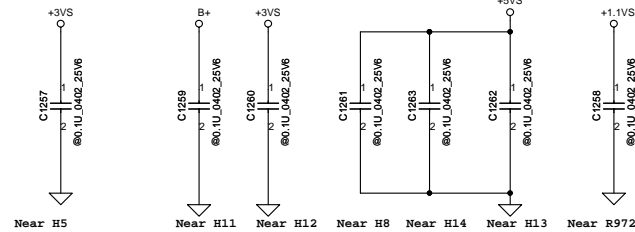
### Screw Hole



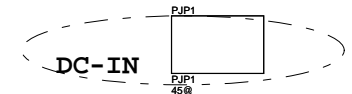
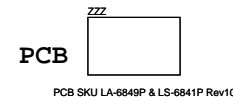
### PCB Fedical Mark PAD



### ESD reserved

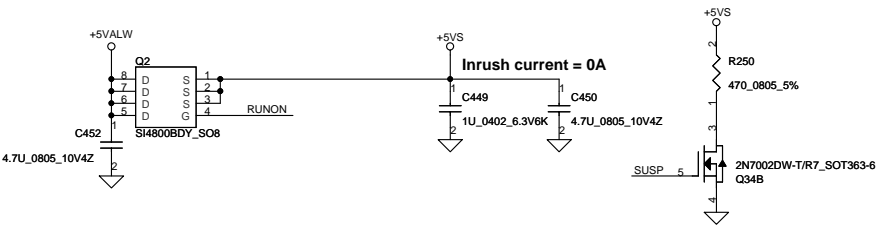


### ISPD

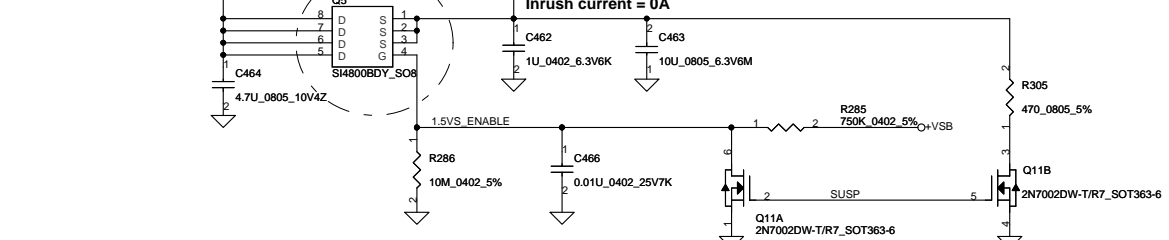


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PCB			Document Number	Rev B
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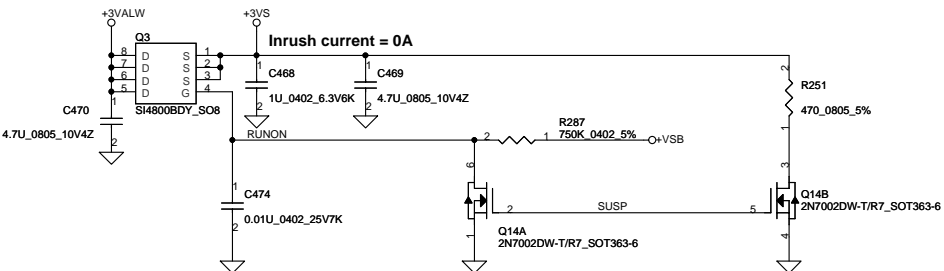
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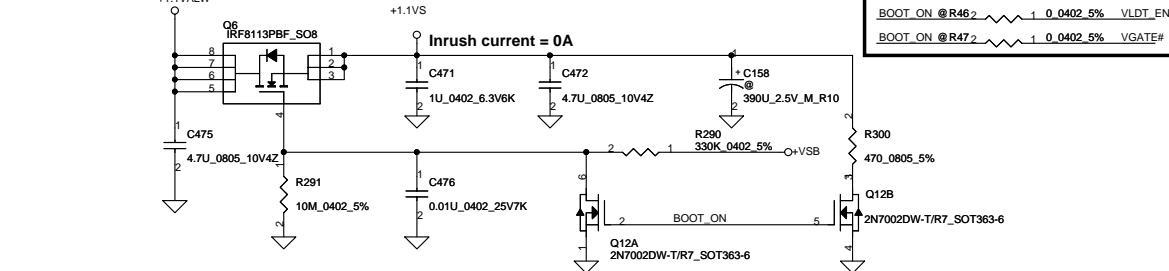
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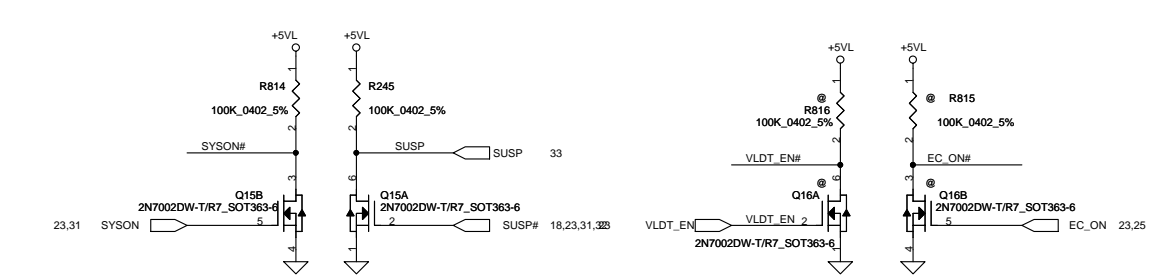


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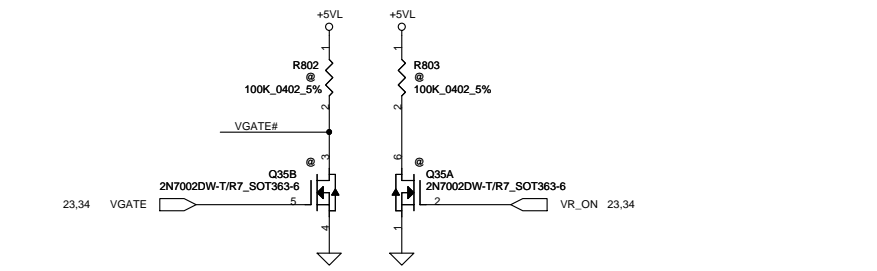
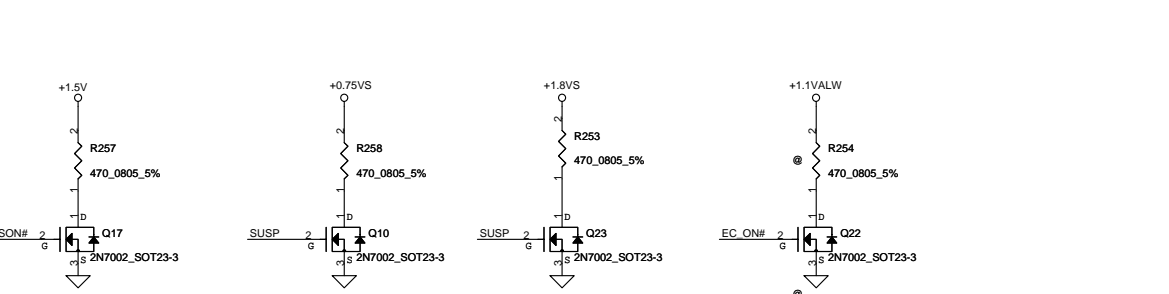


BOOT_ON @ R45	1	0.0402_5%	SUSP
BOOT_ON @ R46	1	0.0402_5%	VLDT_EN#
BOOT_ON @ R47	2	0.0402_5%	VGATE#

< Inversion of SYSON, SUSP#, VLDT\_EN, EC\_ON >

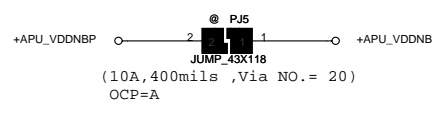
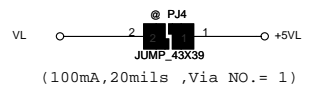
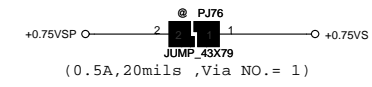
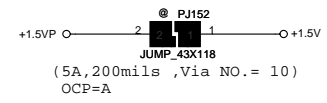
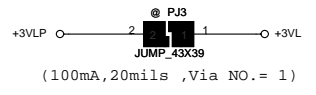
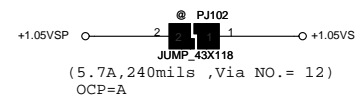
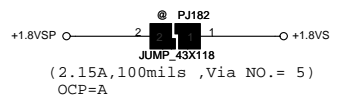
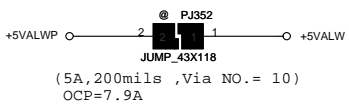
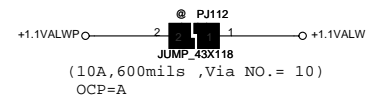
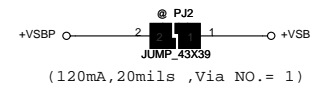
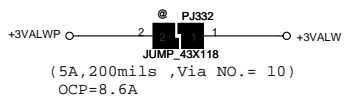
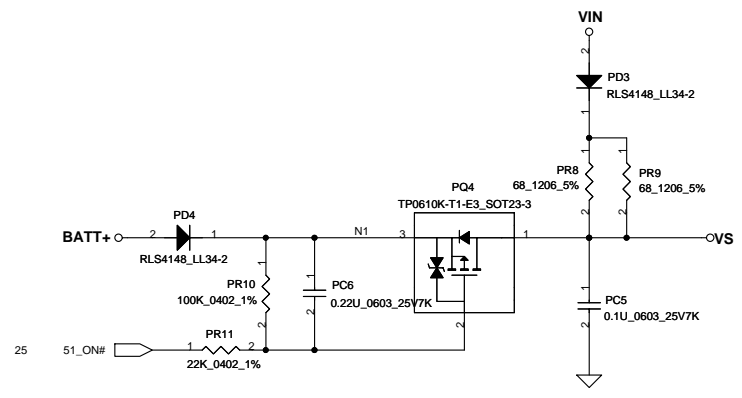
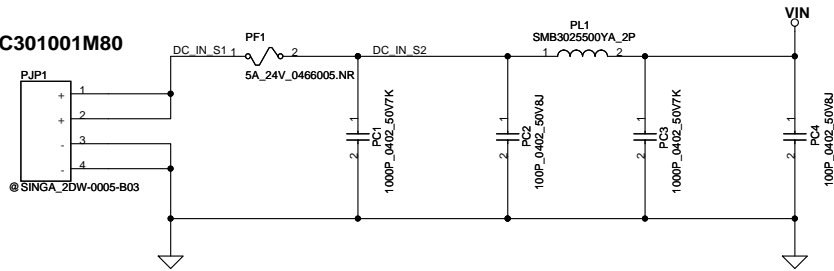


< Discharge circuit >



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**DC301001M80**

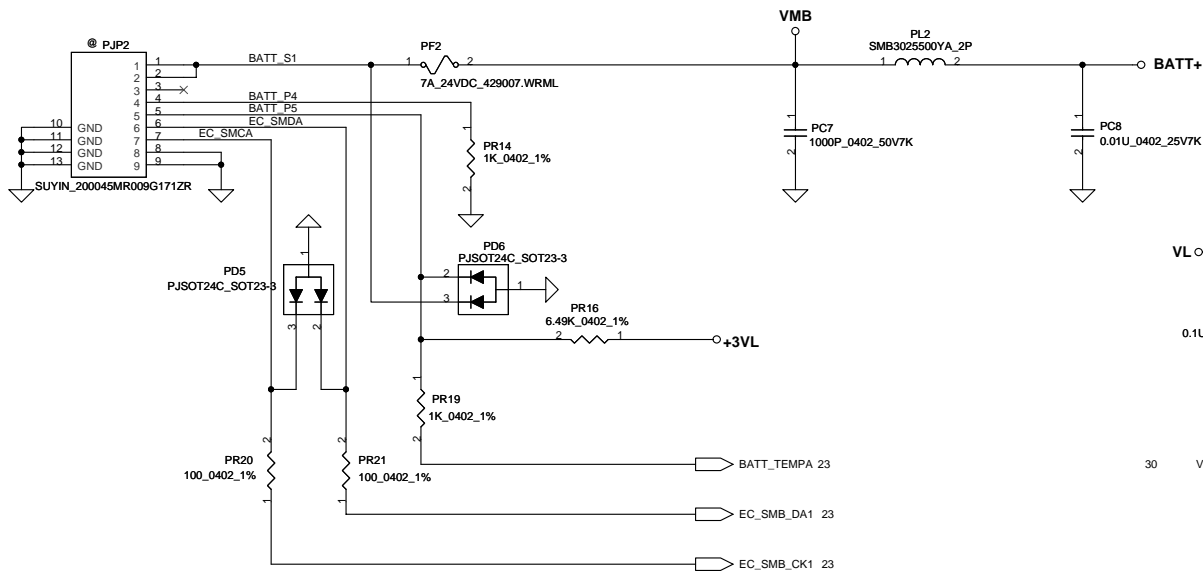


**ACIN**

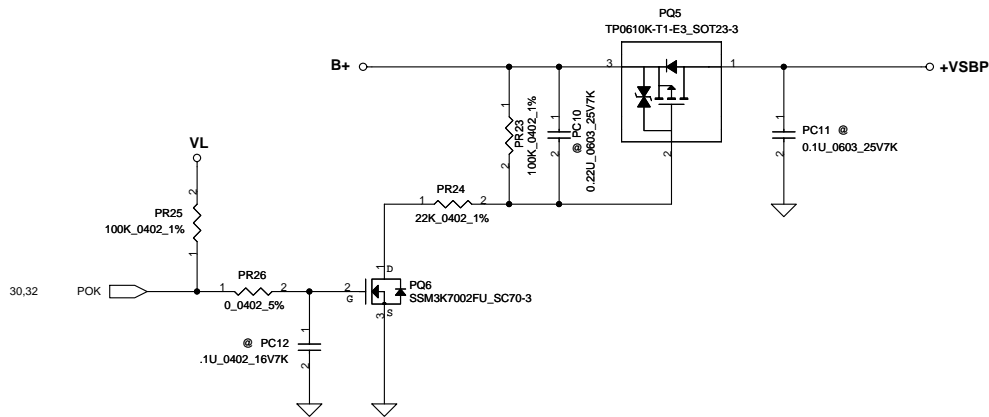
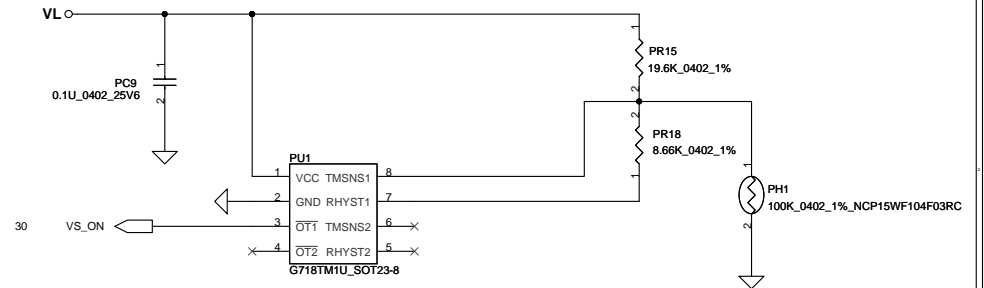
	Min.	typ.	Max
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

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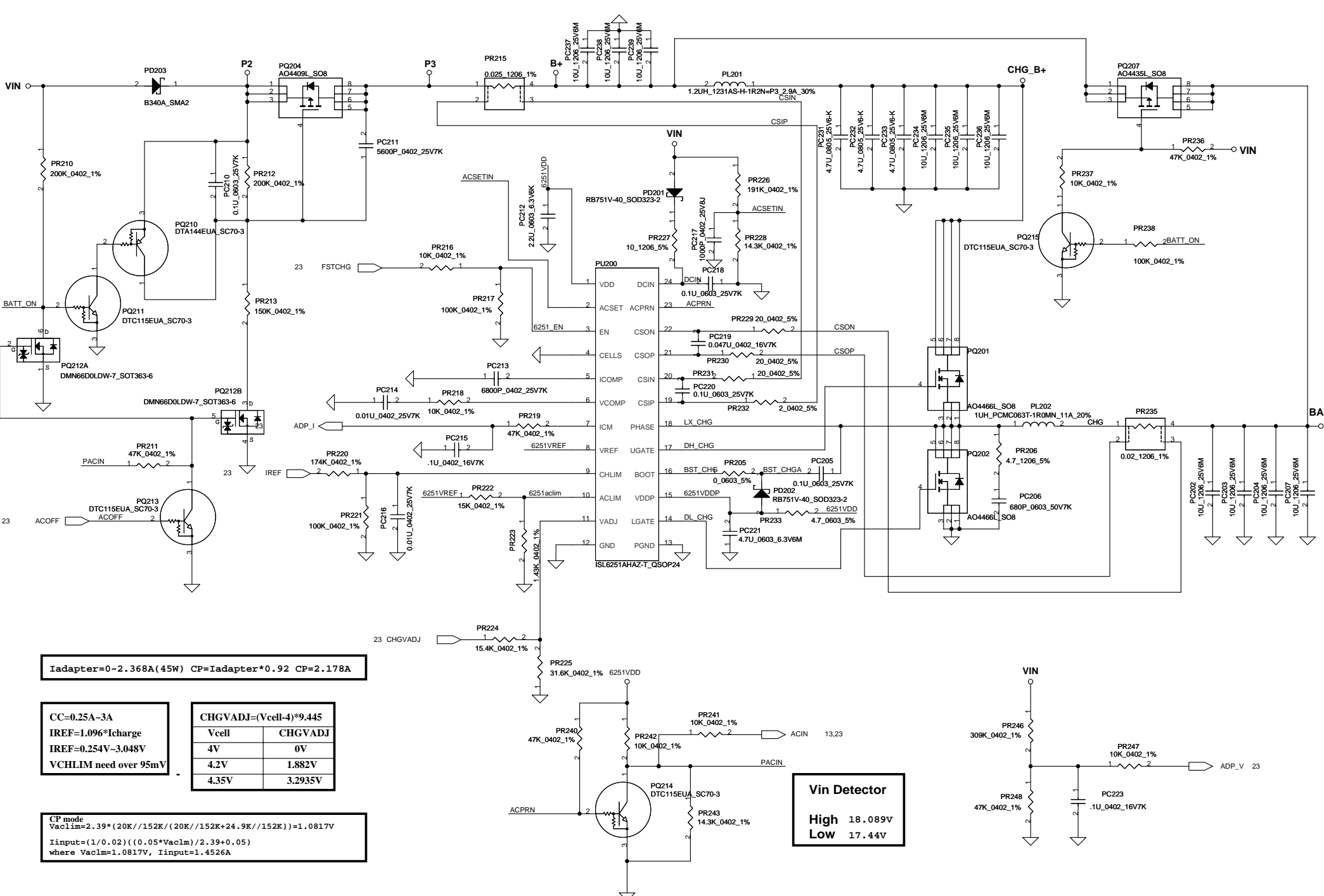
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PH1 under CPU botten side :  
 CPU thermal protection at 95 degree C  
 Recovery at 56 degree C



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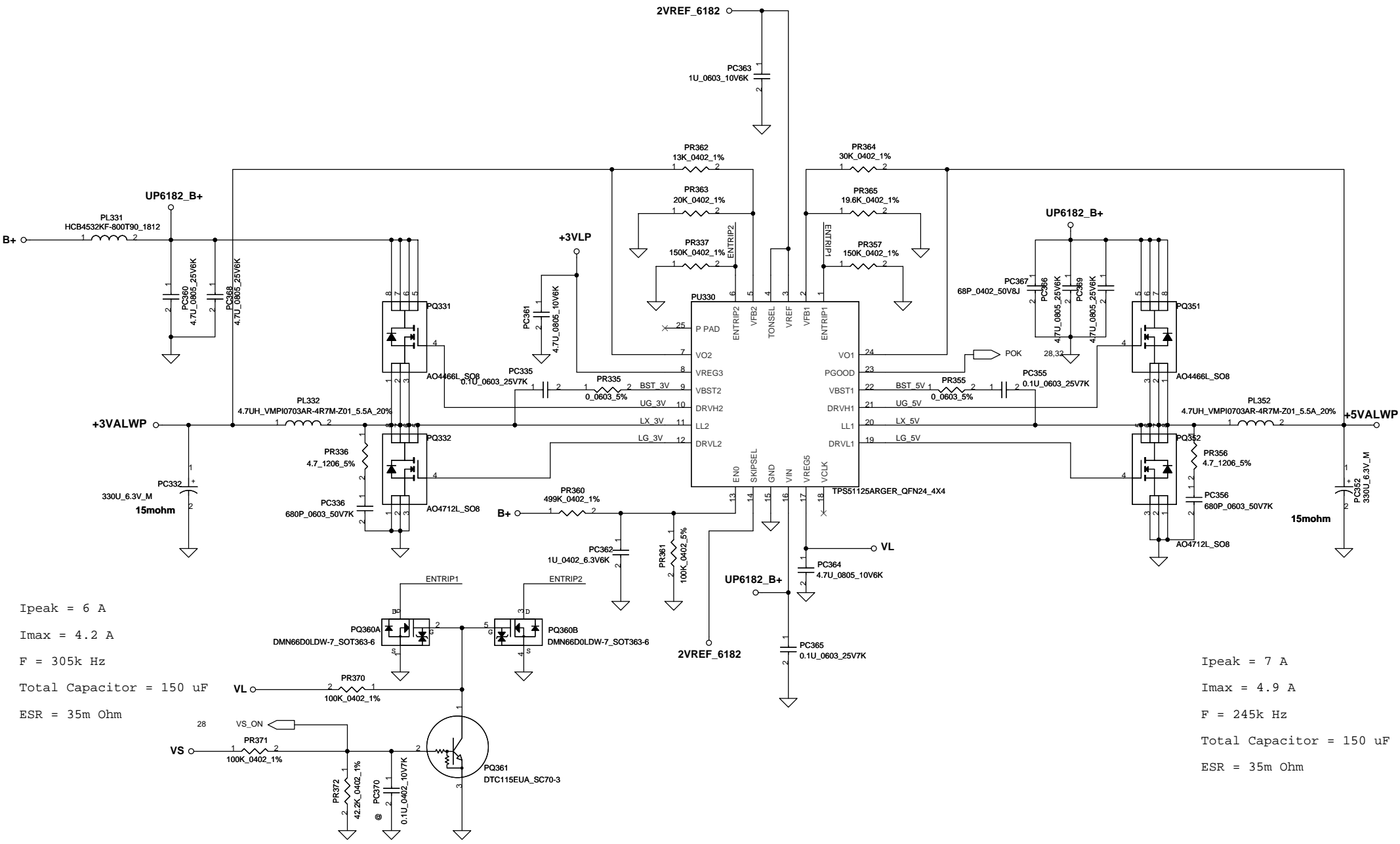
Iadapter=0-2.368A(45W) CP=Iadapter\*0.92 CP=2.178A

CC=0.25A-3A  
 IREF=1.096\*Icharge  
 IREF=0.254V-3.048V  
 VCHLIM need over 95mV

CHGVADJ=(Vcell-4)*9.445	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CP mode  
 $V_{aclim} = 2.39 * (20K // 152K) / (20K // 152K + 24.9K // 152K) = 1.0817V$   
 $I_{input} = (1/0.02) * ((0.05 * V_{aclim}) / 2.39 + 0.05)$   
 where  $V_{aclim} = 1.0817V$ ,  $I_{input} = 1.4526A$

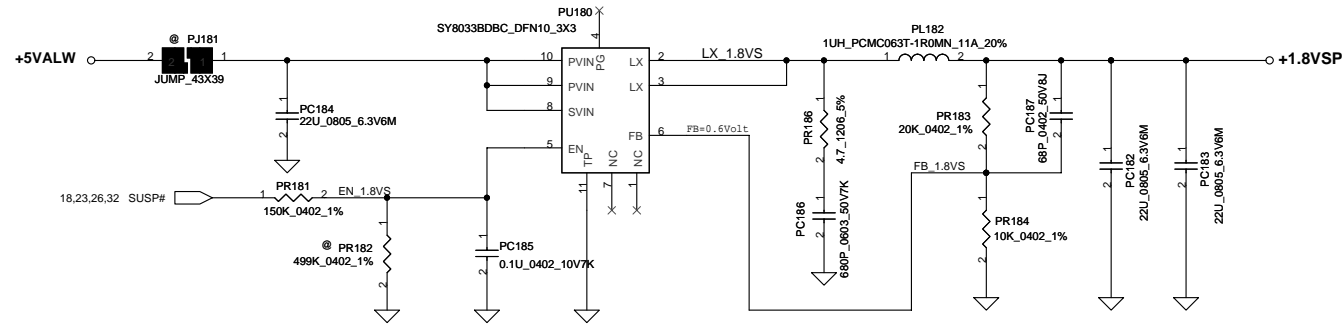
**Vin Detector**  
 High 18.089V  
 Low 17.44V



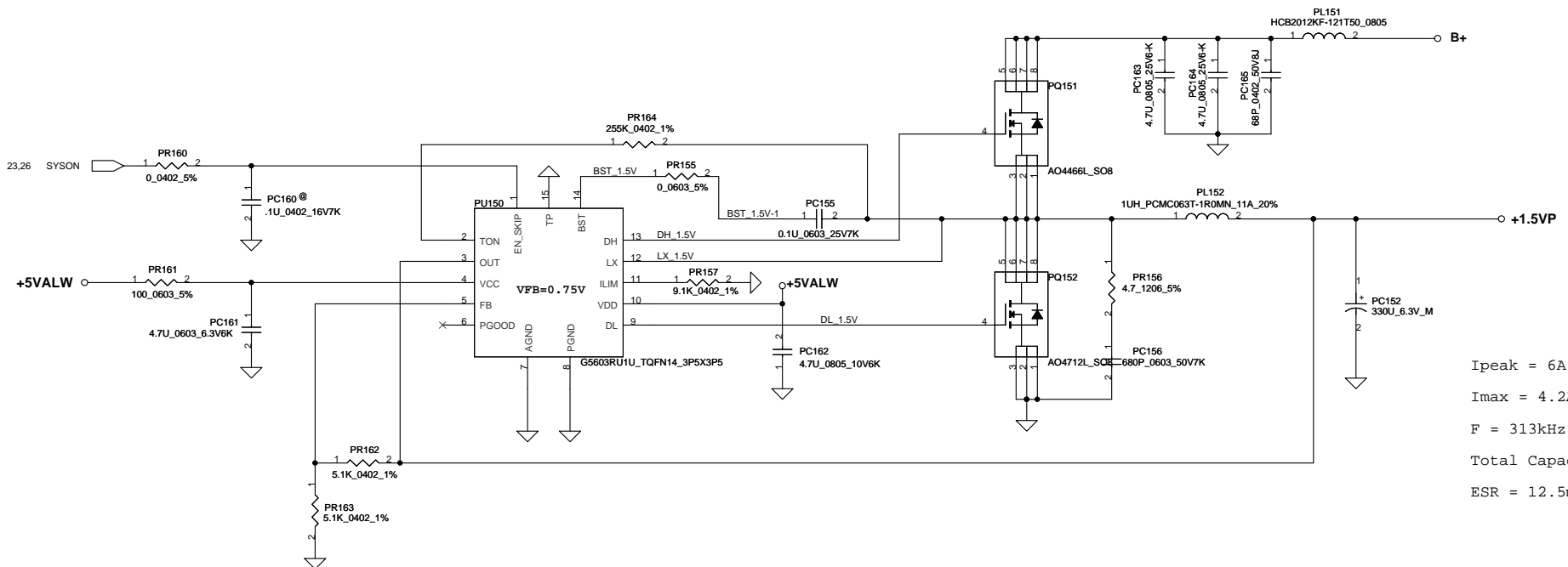
$I_{peak} = 6 \text{ A}$   
 $I_{max} = 4.2 \text{ A}$   
 $F = 305 \text{ kHz}$   
 Total Capacitor = 150  $\mu\text{F}$   
 ESR = 35m Ohm

$I_{peak} = 7 \text{ A}$   
 $I_{max} = 4.9 \text{ A}$   
 $F = 245 \text{ kHz}$   
 Total Capacitor = 150  $\mu\text{F}$   
 ESR = 35m Ohm

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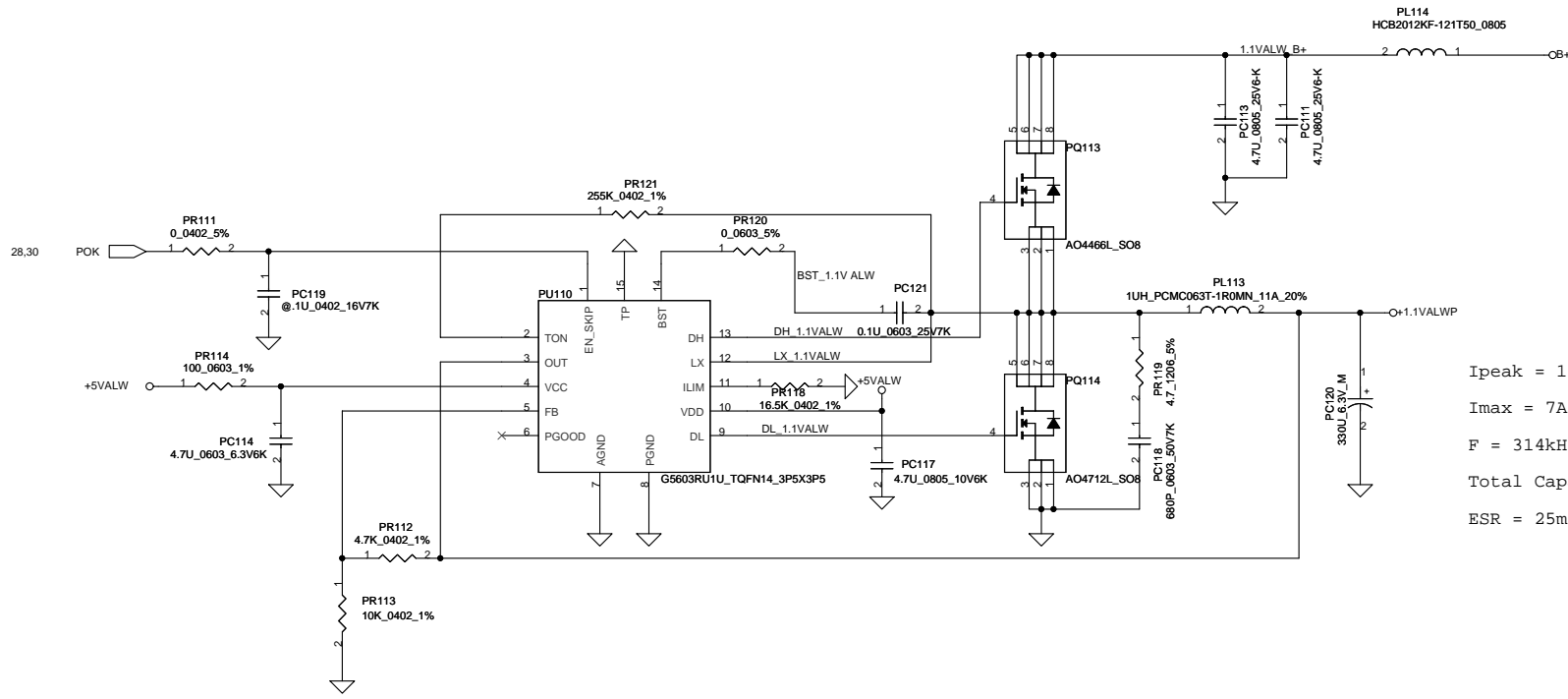


$I_{peak} = 2.15A$   
 $I_{max} = 1.505A$   
 $ILIM = 4A$   
 $F = 1M\ Hz$   
 $Total\ Capacitor = 264\ \mu F$   
 $ESR = 2.273m\ \Omega$

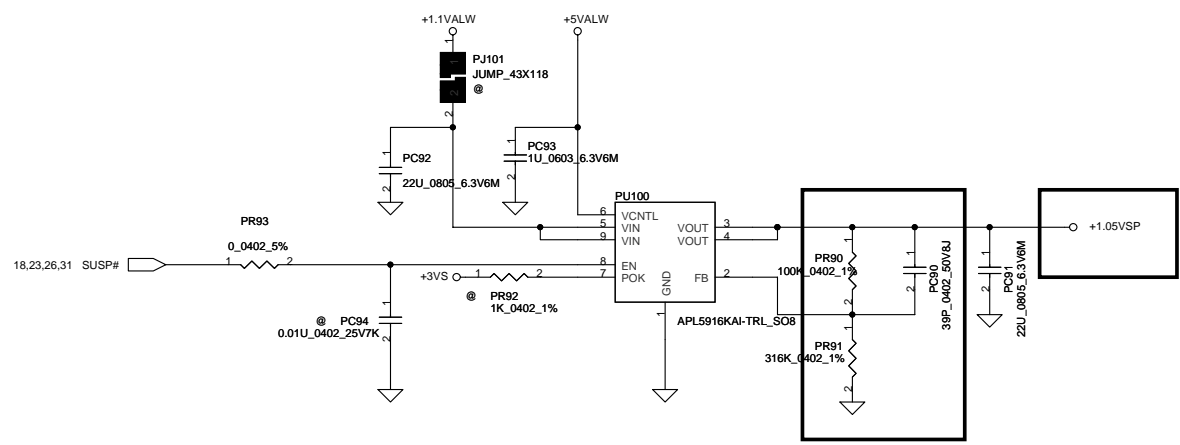


$I_{peak} = 6A$   
 $I_{max} = 4.2A$   
 $F = 313kHz$   
 $Total\ Capacitor = 440\ \mu F$   
 $ESR = 12.5m\ \Omega$

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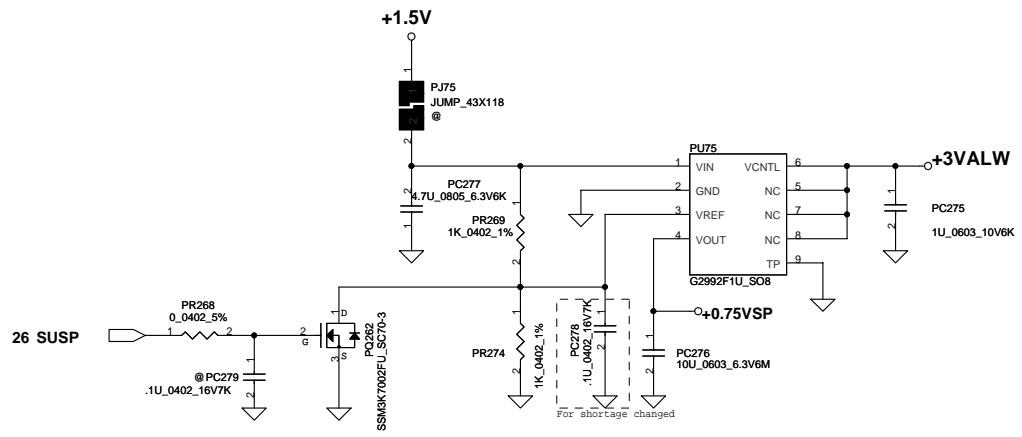


$I_{peak} = 10A$   
 $I_{max} = 7A$   
 $F = 314kHz$   
 Total Capacitor = 220 uF  
 ESR = 25m Ohm



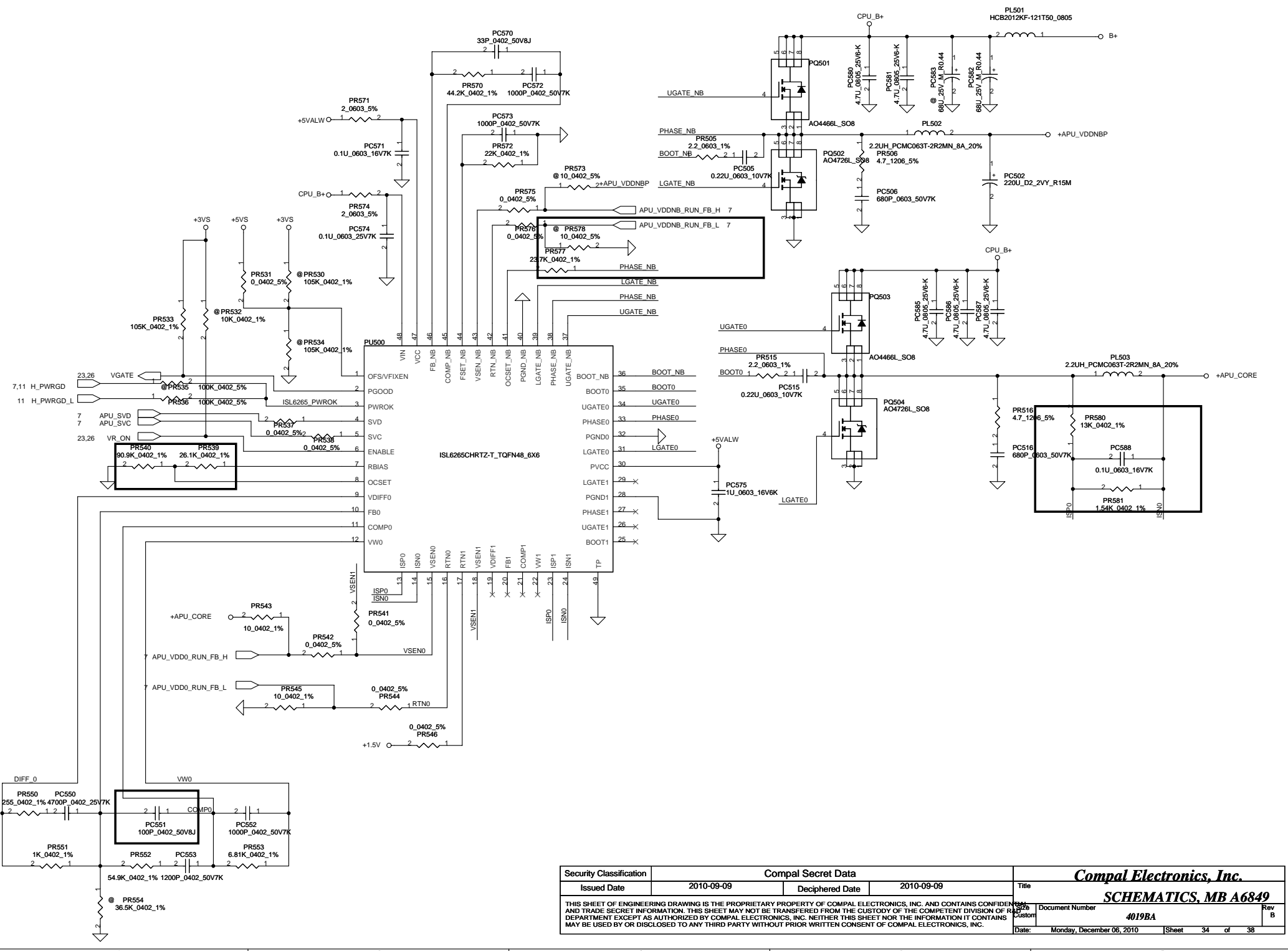
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# Version Change List ( P. I. R. List ) for Power Circuit

Page#	Title	Date	Request Owner	Issue Description	Solution Description
		2010/08/01	POWER		Release
P31	BATTERY CONN / OTP	2010/09/02	POWER	Add PD5,PD6 (For ESD)	DVT
P32	CHARGER	2010/09/02	POWER	Add PR246,PR247,PR248,PC223 (ADP_V)	DVT
P33	3VALWP/5VALWP	2010/09/02	POWER	PR337,PR357 change to 121k	DVT
P33	3VALWP/5VALWP	2010/09/02	POWER	PR365 change to 19.6k	DVT
P34	1.8VSP/1.5VP	2010/09/02	POWER	PR181 change to 150k, PC185 0.1uF	DVT
P35	1.1VALWP/1.0VSP	2010/09/02	POWER	PR91 change to 316k(For 1.05VSP)	DVT
P35	1.1VALWP/1.0VSP	2010/09/02	POWER	PC90 change to 39pF(1.05VSP)	DVT
P37	ACPU_CORE	2010/09/02	POWER	Add PR578 10_0402_5% , PR573 unpop.	DVT
P37	ACPU_CORE	2010/09/02	POWER	PR577 change to 23.7k	DVT
P37	ACPU_CORE	2010/09/02	POWER	PR539 change to 26.1k	DVT
P37	ACPU_CORE	2010/09/02	POWER	PR540 change to 90.9k	DVT
P37	ACPU_CORE	2010/09/02	POWER	PC551 change to 100pF	DVT
P37	ACPU_CORE	2010/09/02	POWER	PR546 change to 0_0402_5%	DVT
P37	ACPU_CORE	2010/09/02	POWER	PR580 change to 6.98k	DVT
P37	ACPU_CORE	2010/09/02	POWER	PR581 change to 1.87k	DVT
P32	CHARGER	2010/09/06	POWER	Add PC207,PC239 10uF (EMI)	DVT

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Version change list (P.I.R. List)

H/W section

Item	Reason for change	PG#	Modify List	Date	Ver#
1	Change pull up voltage from +5VALW to +5VL	26	Change Q15A,Q15B,Q16A,Q16B,Q35A,Q35B from +5VALW to +5VL	2010/09/15	
2	Net VR_ON# is unused	26	Delete net VR_ON# on 9/15	2010/09/15	
3	Sleep and Charge function unused	13	Delete R1119 & R1120 & net SLP_CHK_M3, & SLP_CHK_M4	2010/09/15	
4	Change power from 1.0V to 1.05V	8	Net +1.0V8_VDDOL --->+1.0V8_VDDOL Net +1.0V8_VDD --->+1.0V8_VDD	2010/09/15	
5	Add debug card port on wlan connector	18	Add LPC_AD0,LPC_AD1,LPC_AD2,LPC_AD3,LPC_FRAME# on Jwlan	2010/09/15	
6	Change H7 Pin	24	Connect H7 Pin1 from CLK_PCI_IO to LPC_CLK1	2010/09/15	
7	Add debug card port on Jwlan	18	Pin17 -> PLT_RST# and Pin19 -> CLK_PCI_EC	2010/09/15	
8	Change Q33A,Q33B,Q8A,Q8B,Q163 Part Number	7,17,25	change part number from SB00000A800 to SB00000D800	2010/09/15	
9	For EMS request	12,23	Add C1198,C1236,C1237	2010/09/15	
10	For EMS request	7	Add R1149 to R1158	2010/09/15	
11	H_THERMTRIP# leakage risk	7	Add Q185 and R1084 and W094 to enable H_THERMTRIP# on 9/18	2010/09/18	
12	Change H7 Pin	24	Connect H7 Pin1 from LPC_CLK1 to CLK_PCI_EC	2010/09/20	
13	Remove 75W_65W net name in UMA platform.	23	Remove 75W_65W net name in UMA platform.	2010/09/20	
14	USB_OC#0 add pull high 10K to +3VALW	18	USB_OC#0 add pull high R51 to +3VALW	2010/09/20	
15	use VLDT_EN# to turn on +1.1VALW to +1.1VS	26	Reserve R46 and stuff R45	2010/09/20	
16	use BT_OFF# to control BT_CTRL	11	Delete net BT_SW#	2010/09/20	
17	use BT_OFF# to control BT_CTRL	13	Add net BT_OFF# on U22.Y9	2010/09/20	
18	use BT_OFF# to control BT_CTRL	18	Change control net from BT_SW# to BT_OFF# and add R316 bypass BT_OFF# & BT_CTRL, and reserve QM1	2010/09/20	
19	For desigh change	26	Reserve Q16A,Q16B,Q35A,Q35B,R802 ,R803,R825,R816	2010/09/20	
20	For desigh change	18	Put R259	2010/09/20	
21	For desigh change	11	Reserve U56 and put R1072	2010/09/20	
22	HDMI unused	11	TEST35 pull down through R1029	2010/09/20	
23	For desigh change	7	Reserve R1014 and R1006,put R1002 ,R1004, and R1010	2010/09/20	
24	For desigh change	7	Remove R92 ,R93, and R94 pull up and down resistor	2010/09/23	
25	For desigh change	13	Pull down GP10178 and GP10180 with R1119 & R1120	2010/09/23	
26	For desigh change	19	Mount RL6 on 10/4	2010/10/04	
27	For desigh change	25	Delete H3 and H5	2010/10/04	
28	Change +3VL_LID power rail from +3VALW to +3VL	24	Add R97 and reserve R101,Add net name +3VL_LID	2010/10/13	
29	Change +3VL_LAN turn on pin from WOL_EN# to +3VALW	19	Short D728 and reserve Q1,CL12,CL14 and RL25	2010/10/18	
30	Use WOL_EN to enable ISOLATEB	19	Reserve RL6 on 10/4	2010/10/19	
31	Change Q164 footprint to SOT23-3	15	Change Q164 P/N to SB8570020020	2010/10/19	
32	Add clearing password feature controlled by bios	15	Reserve D129 and add R1159 pull high	2010/10/26	
33	For mechanical desigh change	25	Delete H15	2010/10/27	
34	H7 debug port function unused	25	Add R103 and reserve R102	2010/11/17	
35	H7 debug port function unused	24	Change R102 value to 1K and R103 to be 220pF cap	2010/11/22	
36	For EMS request	21	Change R1085 to 10 ohm and R1088 to 10pF	2010/11/22	
37	Add AGND to speaker area for SPK traces	21	Add CA60 capacitor to short GND and AGND	2010/11/19	

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<small>DATE: Monday, October 04, 2010 10:58 AM</small>				Page 1 of 38

# Version Change List (P. I. R. List) for Power Circuit

NO DATE	PAGE	MODIFICATION LIST	PURPOSE	Rev.
<b>2010 . 06 . 21 Release</b>				
<b>2010 . 07.25 modification list</b>				
	P 33	PC16 change to SE070104Z80	Defore material EOL	PVT
	P 38	PU12 change to SA000022M80	Before material MP schedule will impact PWWAE MP schedule	PVT
	P 33	Remove PD6 , PD8 @	ESD test fail	PVT
	P 34	Add PC132 , remove PC130 , PC131 , PR69 , PC41 @	For EMI fail	PVT
	P 35	Add PC51 , remove PC49 , PC46 , PC57 , PC58 , PR89 , PR90 @	For EMI fail	PVT
	P 36	Add PC79 , PC91 , PC133 , remove PR100 , PR108 , PC68 , PC77 @	For EMI fail	PVT
	P 38	Remove PR125 , PR139 , PR151 , PC106 , PC111 , PC117 @	For EMI fail	PVT
<b>2010 . 08.10 modification list</b>				
	P 37	Change PU9 , PU11 to SA053310110	UP7711 stop using from now on	Pre-MP
	P 38	Add PC218 , PC219 , PC371	For VCORE Ripple	Pre-MP
	P 32	Add PR8	For Precharge rising current	Pre-MP
	P 32 , P 33	PQ1 , PQ2 , PQ6 change to SB900840003	SB906100210 material delivery had problem	Pre-MP
<b>2010 . 08.16 modification list</b>				
	P 35	Change PU5 to SA000020C80	UPI product stop using	Pre-MP
<b>2010 . 08.17 modification list</b>				
	P 34	Change PU4 to SA00001EP80	SA00003TK00 stop using	Pre-MP
	P 38	Remove PR127 @	To solve +1.1VALW noise	Pre-MP
<b>2010 . 08.23 modification list</b>				
	P 34	Remove PR193 , PQ39 @	For PWWAE MP use 25W CPU	Pre-MP

Security Classification	Compal Secret Data			Title	
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# AC POWER ON

# AMD APU Brazos FT1+FCH Hudson M1

