

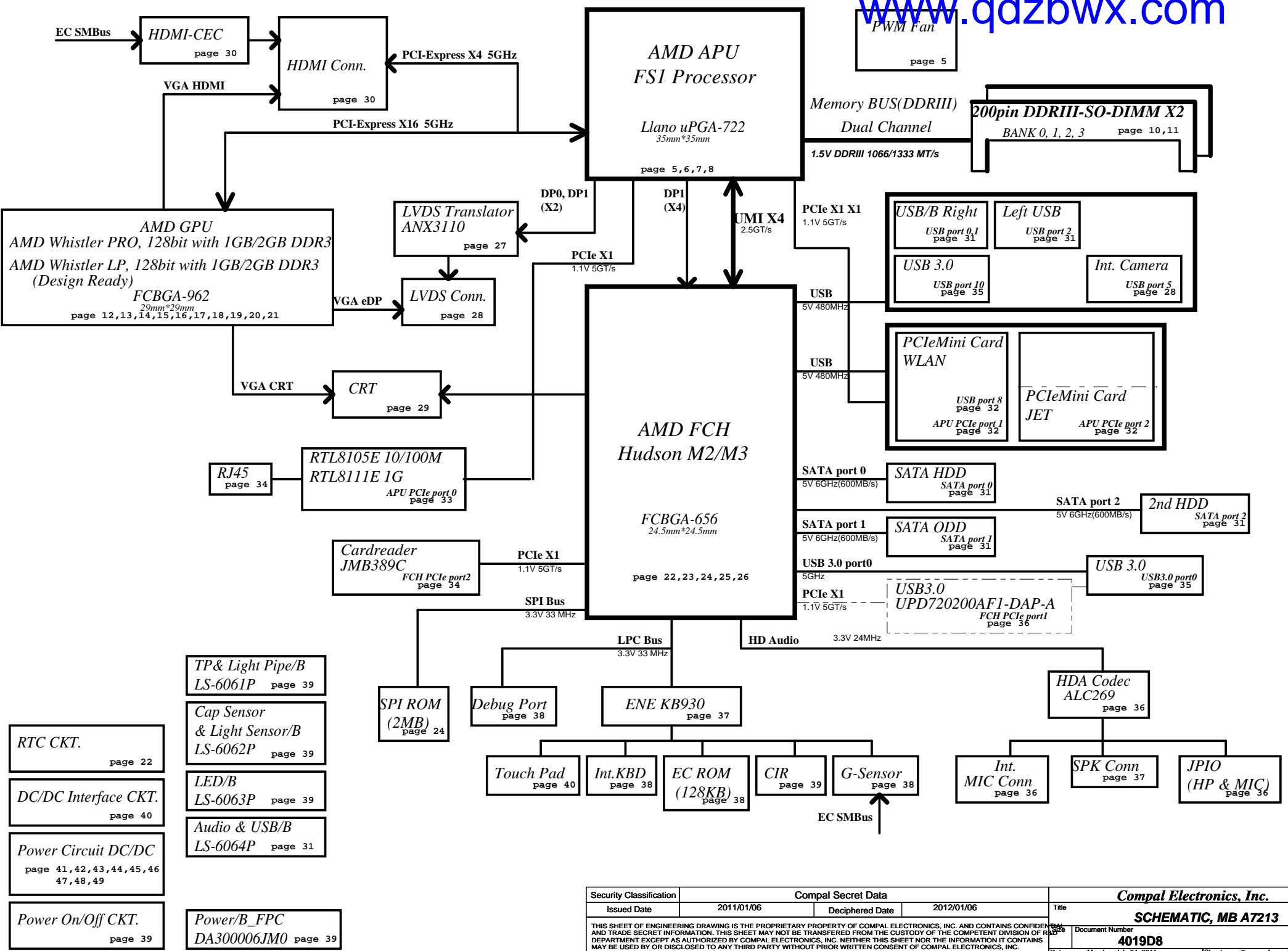
QHRAE

Superior 10AS/10ASG

LA-7213P REV 1.0 Schematic

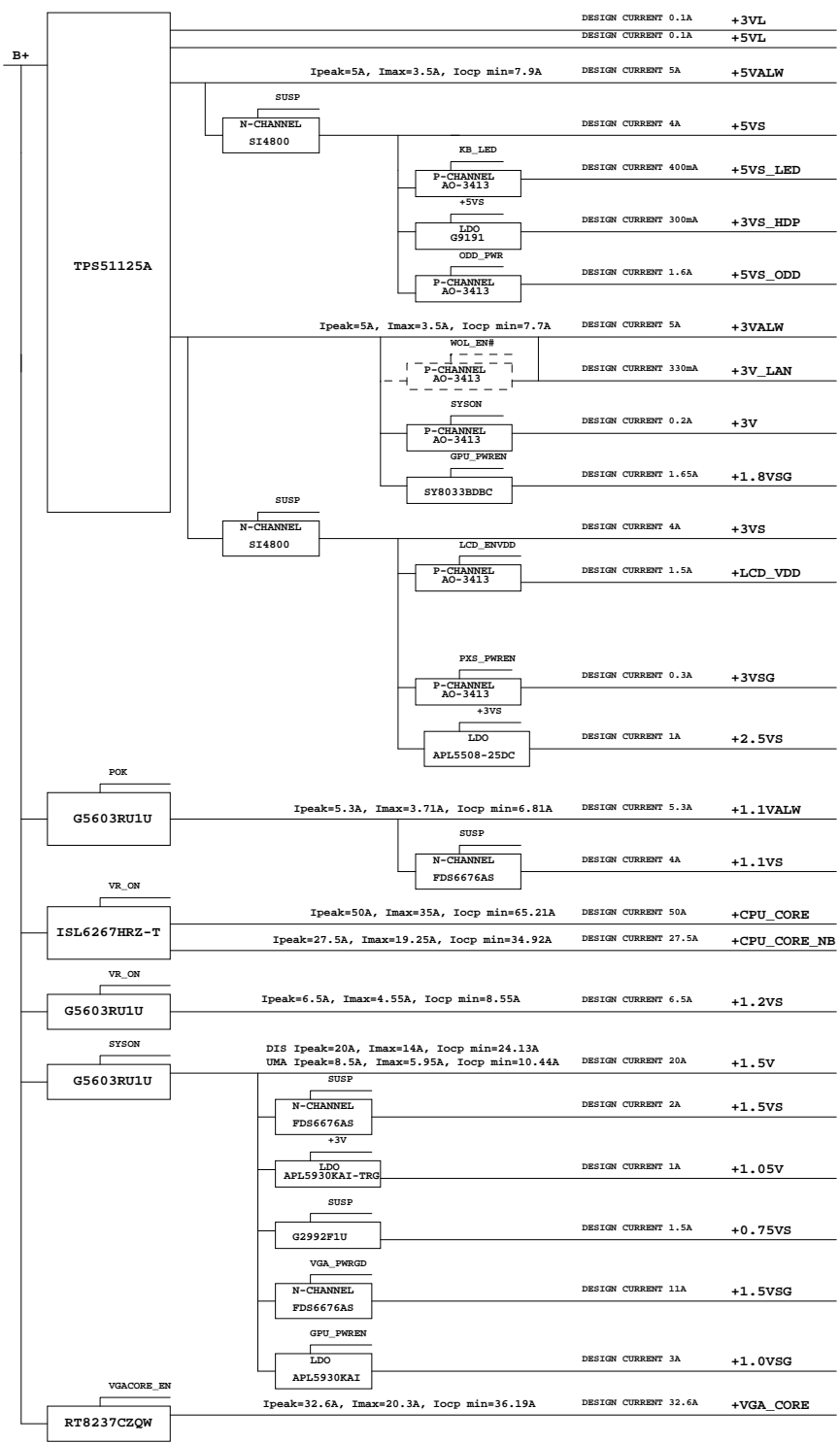
<p>AMD Llano FS1 Processor / Hudson M2/M3 Whistler Pro 2011-04-30 Rev 1.0</p>

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- DC/DC Interface CKT. page 40
- Power Circuit DC/DC page 41,42,43,44,45,46,47,48,49
- Power On/Off CKT. page 39
- TP & Light Pipe/B LS-6061P page 39
- Cap Sensor & Light Sensor/B LS-6062P page 39
- LED/B LS-6063P page 39
- Audio & USB/B LS-6064P page 31
- Power/B_FPC DA300006JM0 page 39

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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.1VALW +VSB	+1.5V +3V +1.05V	+5VS
						+3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +CPU_CORE +CPU_CORE_NB +VGA_CORE +3VSG +1.8VSG +1.5VSG +1.0VSG
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function	HDMI				SKU		
description	HDMI				SKU		
explain	UMA PowerXpress	Discrete	COMMON	CEC	UMA	PowerXpress	Discrete
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	UMA@	UMA@+VGA@+PXS@	VGA@+DIS@

Function	LAN		CIR	KB Light
description	LAN		CIR	KB Light
explain	10/100M		GIGA	KB Light
BTO	8105E@		8111E@	CIR@ KBL@

Function	G-SENSOR	Cam & Mic	Panel		
description	G-SENSOR	Cam & Mic	Panel (DIS@)		
explain	G-SENSOR	Cam & Mic	3D LVDS	eDP	Non-3D & EDP
BTO	GSSENSOR@	CAM@	3D@+NOEDP@	EDP@	NO3D@+NOEDP@

Function	GPIO for PowerXpress		Chipset			
description	PowerXpress (PXS@)		FCH		GPU	
explain	PowerXpress Enable	Crossfire Enable	Hudson-M3		Whistler Pro	
BTO	PXSEN@	CROSSEN@	HUDM3R1@	HUDM3R3@	WHPROR1@	WHPROR3@

Function	PowerXpress		Renesas USB3.0	FCH	EC	
description	PowerXpress (PXS@)		Renesas USB3.0	FCH	EC	
explain	BACO mode	Non-BACO	Renesas USB3.0	Hudson-M2	Hudson-M3	KB-930 KB-9012
BTO	BACO@	NOBACO@	RENE@	M2@	M3@	KB930@ KB9012@

FCH SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	WLAN		
+3VS	3G		

EC SM Bus1 Address

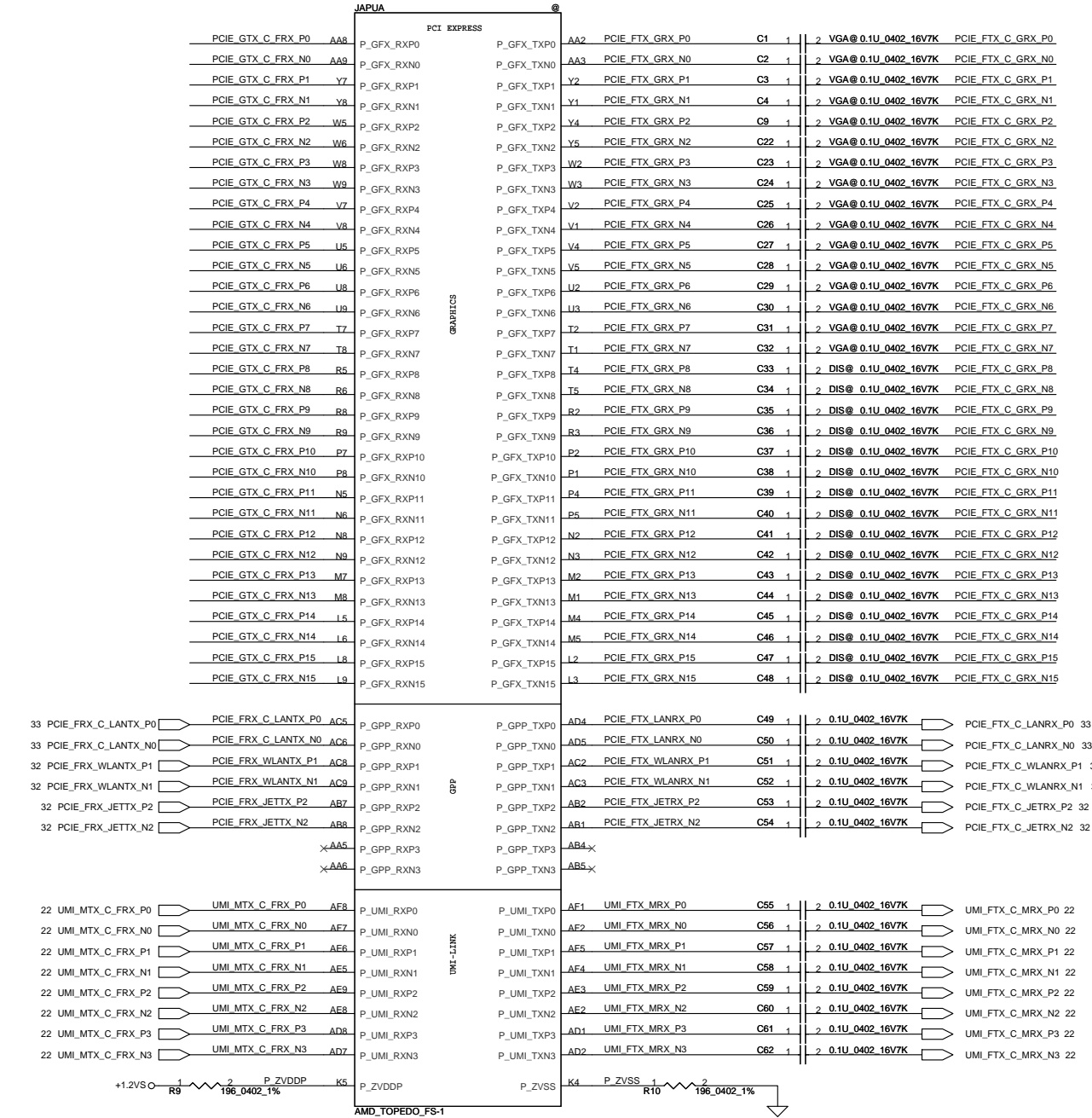
EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	CPU Thermal Sensor	98 H	1001 1001 b
+3VL	HDMI-CEC	34 H	0011 0100 b	+3VS	GPU Thermal Sensor	41 H	0100 0001 b
				+3VS	G-Sensor	40 H	0100 0000 b
				+3VS	Light Sensor	52 H	0101 0010 b
				+3VS	3D - Bootloader	C0 H	1100 0000 b
				+3VS	3D - Slave	C0 H	1100 0000 b
Power	Device	HEX	Address				
+3VL	Cap. Sensor		Virtual I2C				

STATE	SIGNAL	SLP_S3#	SLP_S5#
Full ON		HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH
S4 (Suspend to Disk)		LOW	HIGH
S5 (Soft OFF)		LOW	LOW
G3		LOW	LOW

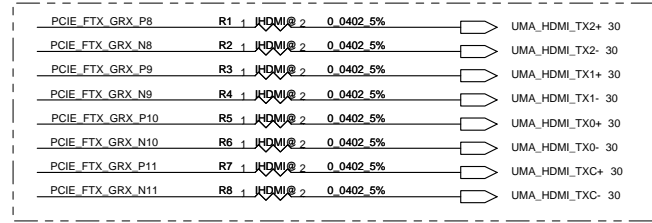
12 PCIe_GTX_C_FRX_P0[0..15]
 12 PCIe_GTX_C_FRX_N0[0..15]

PCIe_FTX_C_GRX_P0[0..15] 12
 PCIe_FTX_C_GRX_N0[0..15] 12



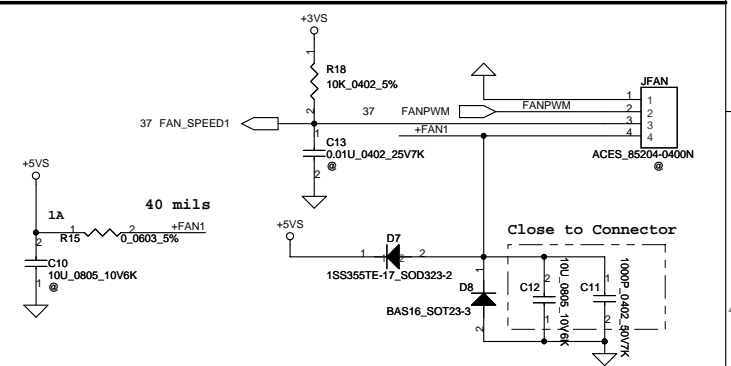
For PowerXpress

Place R1 ~ R8 close to C33 ~ C40

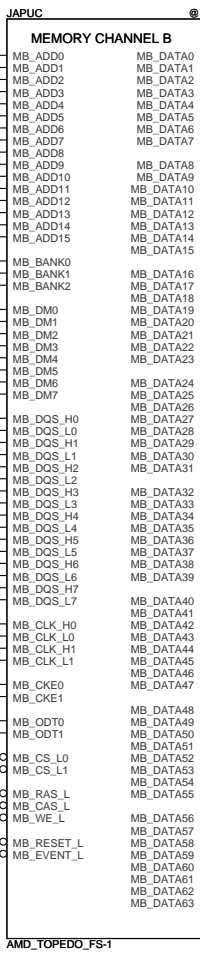
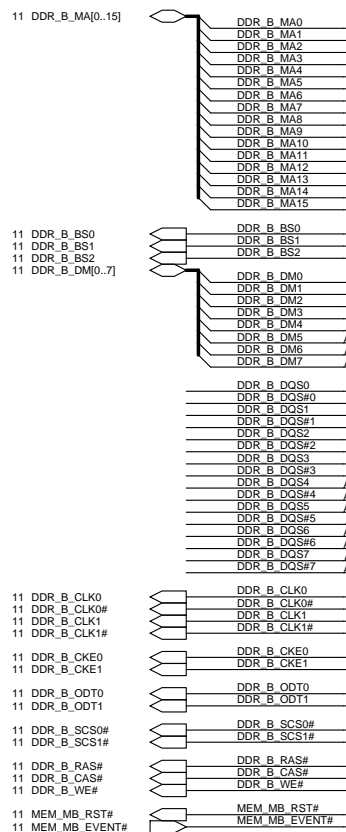
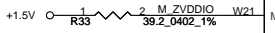
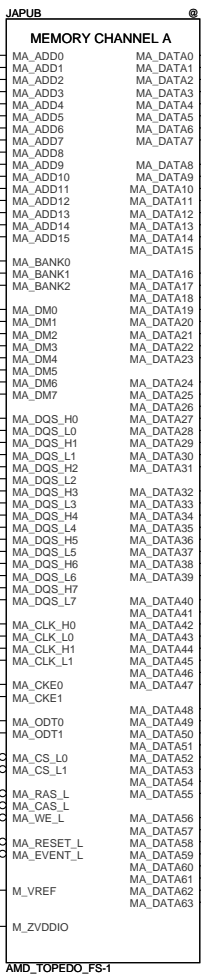
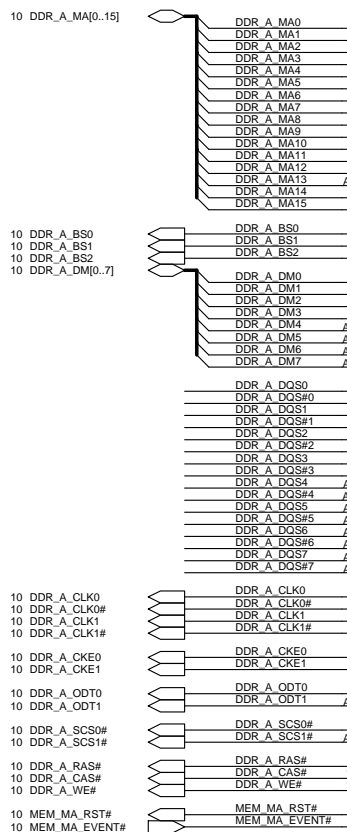


LAN
WLAN
JET

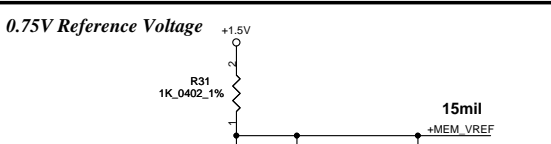
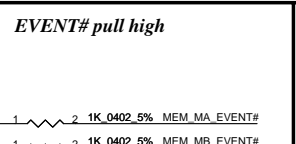
FAN Control Circuit



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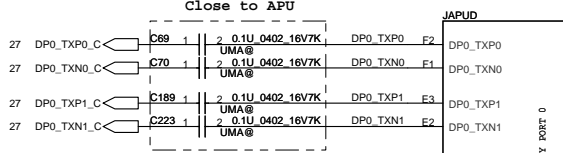
AMD_TOPEDO_FS-1



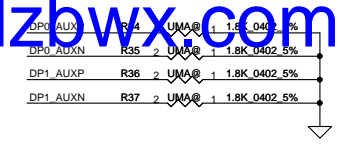
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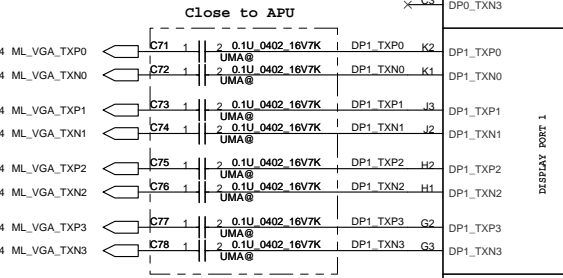
To LVDS Translator



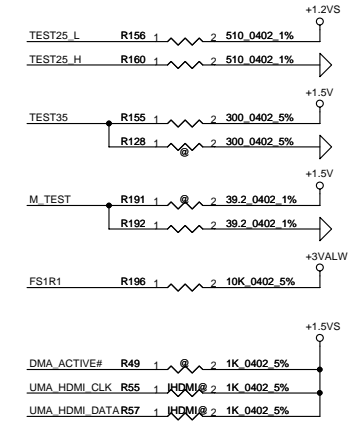
To LVDS Translator



To FCH

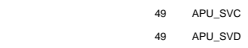


To FCH

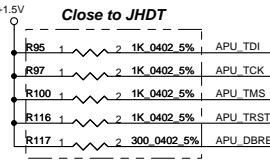
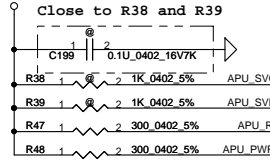
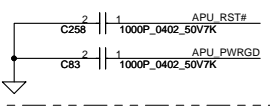


100MHz (SS)

100MHz (NSS)

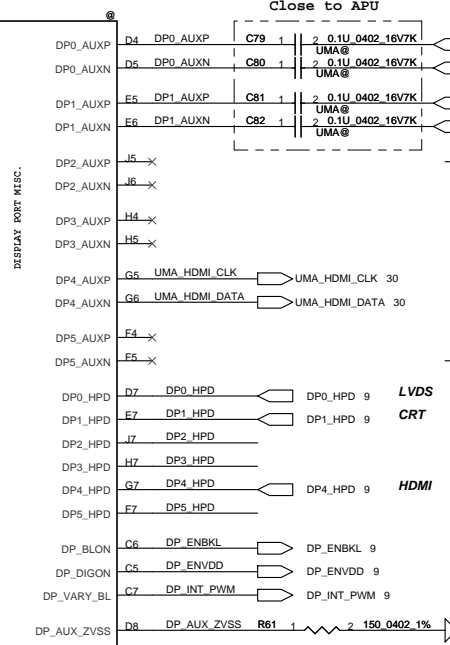


SB-TSI



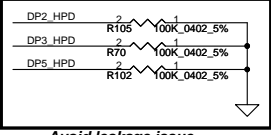
Reserve test point for debug use

Avoid leakage issue

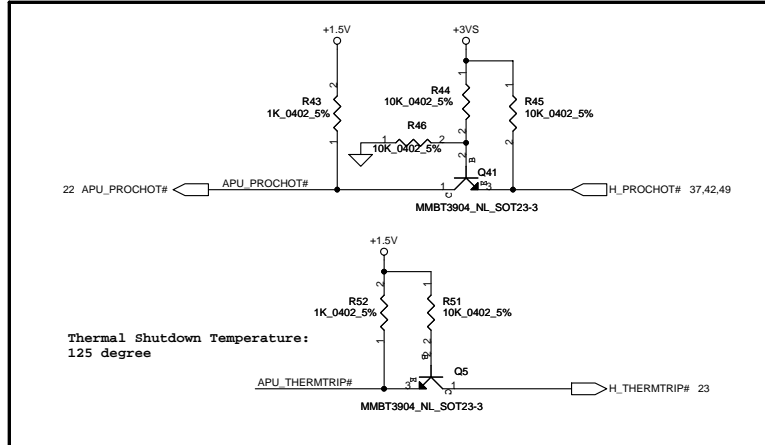
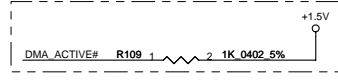


AUX 2-5 are for GFX interface use, they could be selected to DDC or AUX logic

VDDIO level Need level shifter



Avoid leakage issue



Thermal Shutdown Temperature: 125 degree

HDT Debug conn

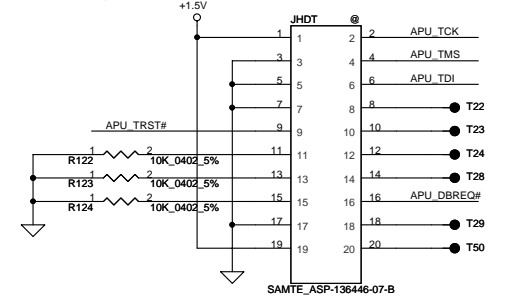
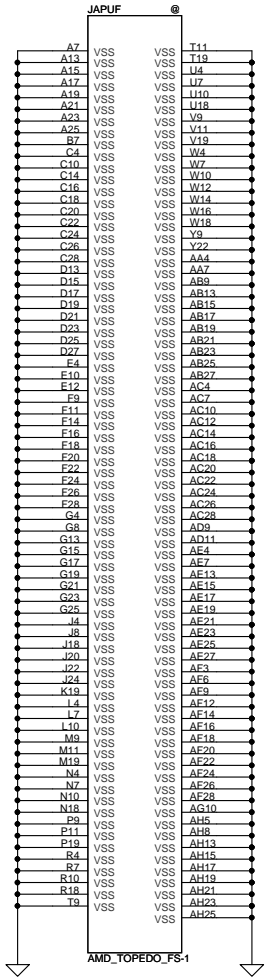
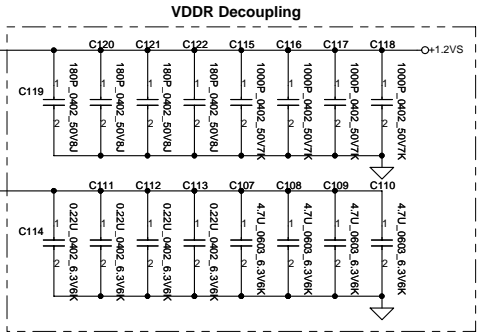
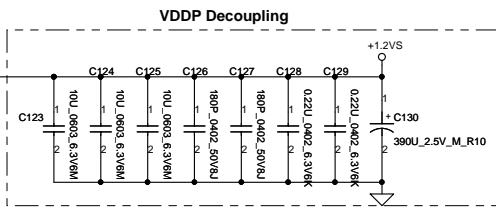
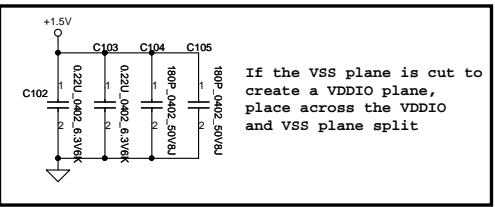
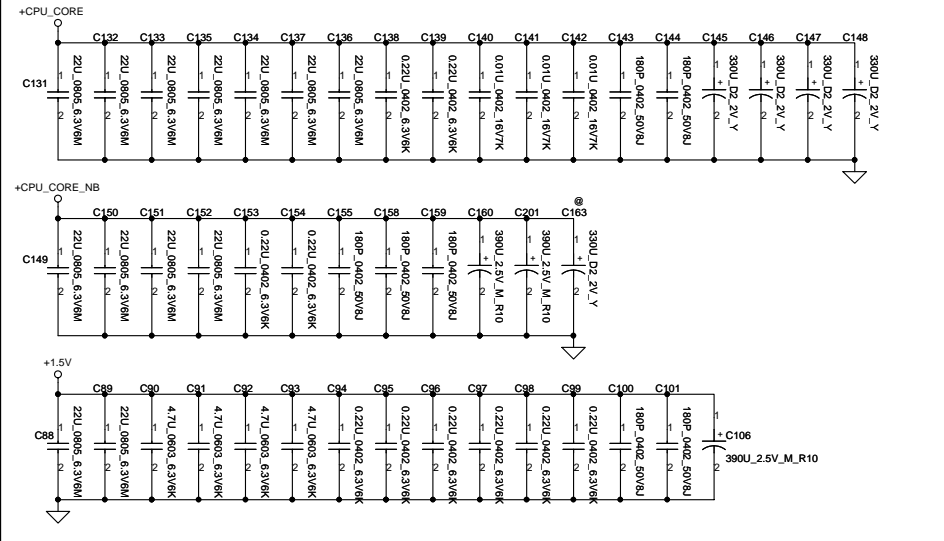
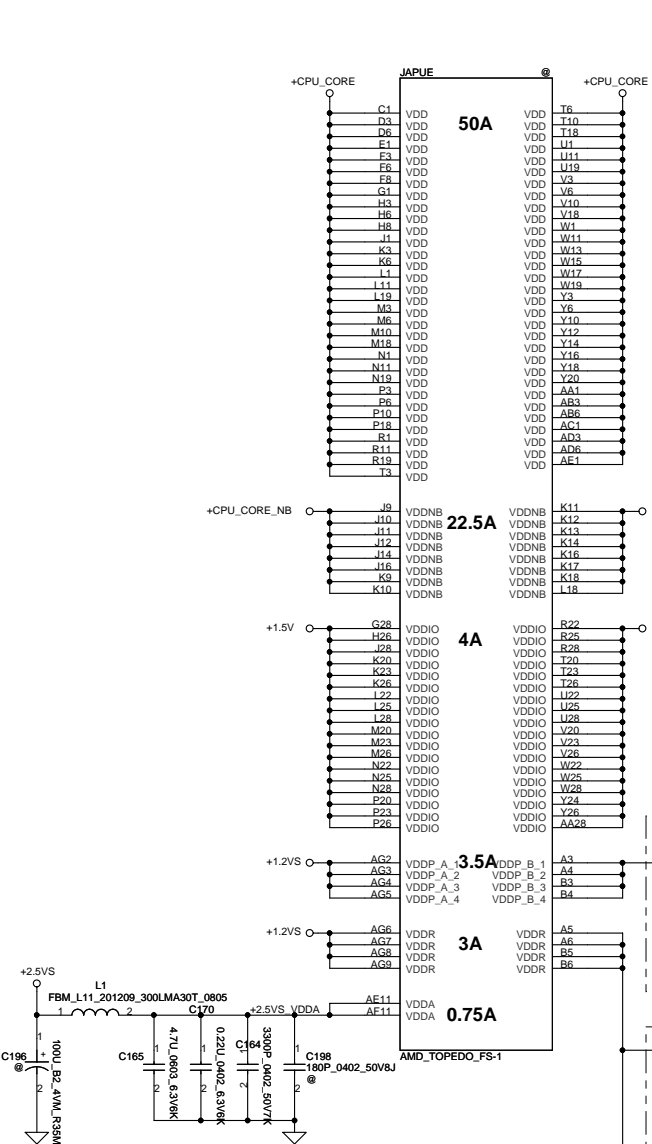


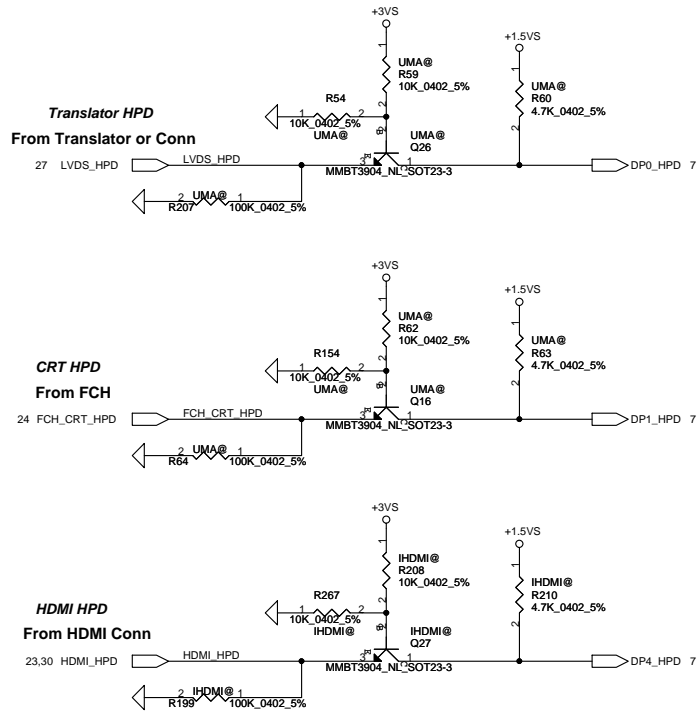
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CPU BOTTOM SIDE DECOUPLING

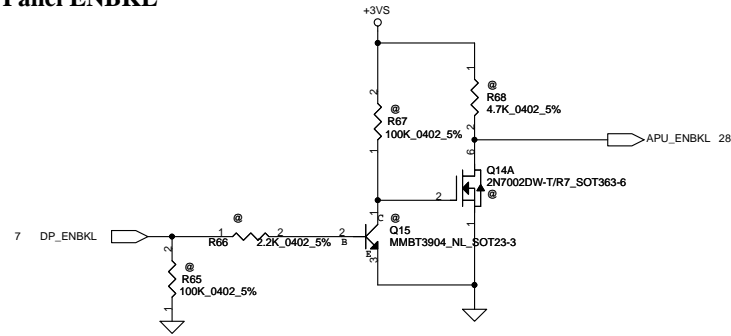


CRB Decoupling Capacitor (include PWM side) :						
VDD: 470uF x 6 22uF x 9 0.22uF x 2 0.01uF x 3 180pF x 2	VDDNB: 470uF x 4 22uF x 6 0.22uF x 2 180pF x 3	VDDIO: 680uF x 1 330uF x 1 22uF x 2 4.7uF x 4 0.22uF x 8 180pF x 4	VDDP/R_PWM: 470uF x 2 10uF x 1	VDDP: 10uF x 3 0.22uF x 2 180pF x 2	VDDR: 4.7uF x 4 0.22uF x 4 1nF x 4 180pF x 4	VDDA: 100uF x 1 4.7uF x 1 0.22uF x 1 3.3nF x 1

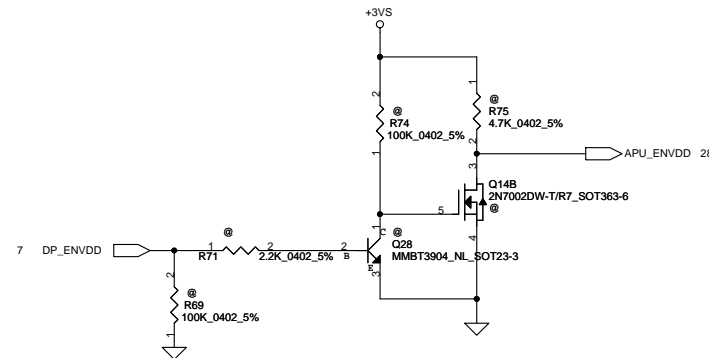
HPD



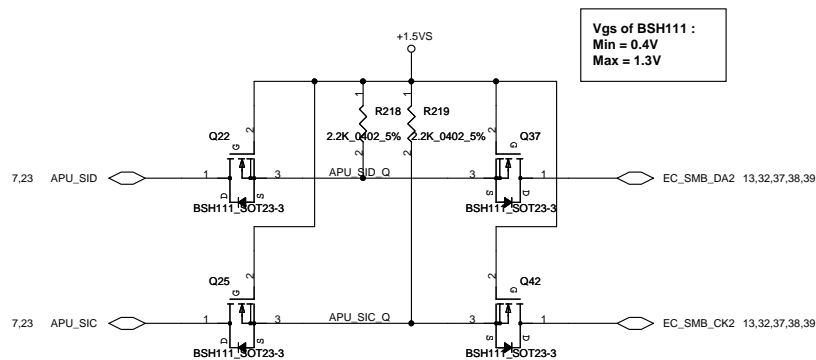
Panel ENBKL



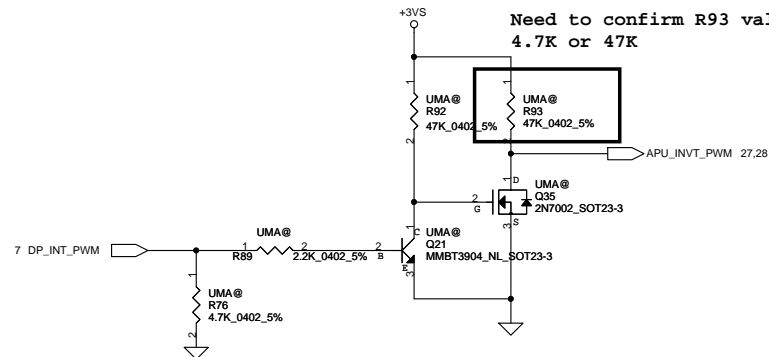
Panel ENVDD



SB-TSI

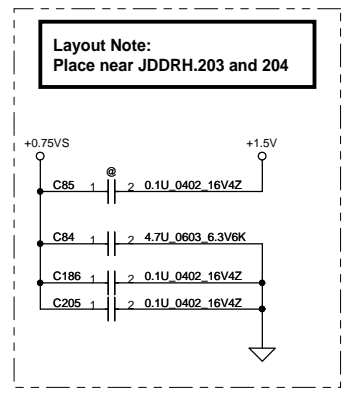
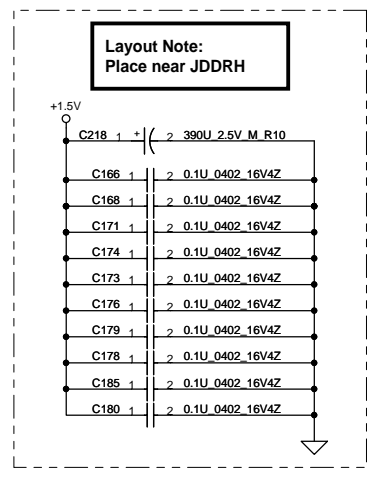
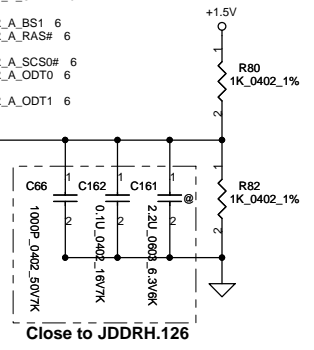
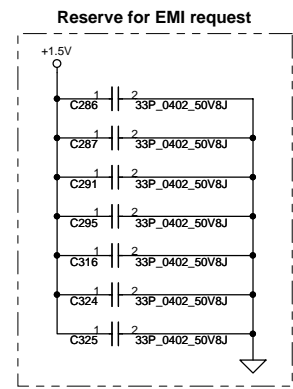
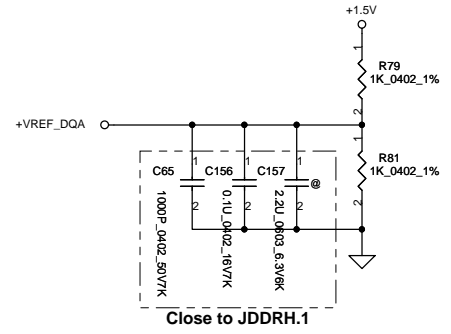
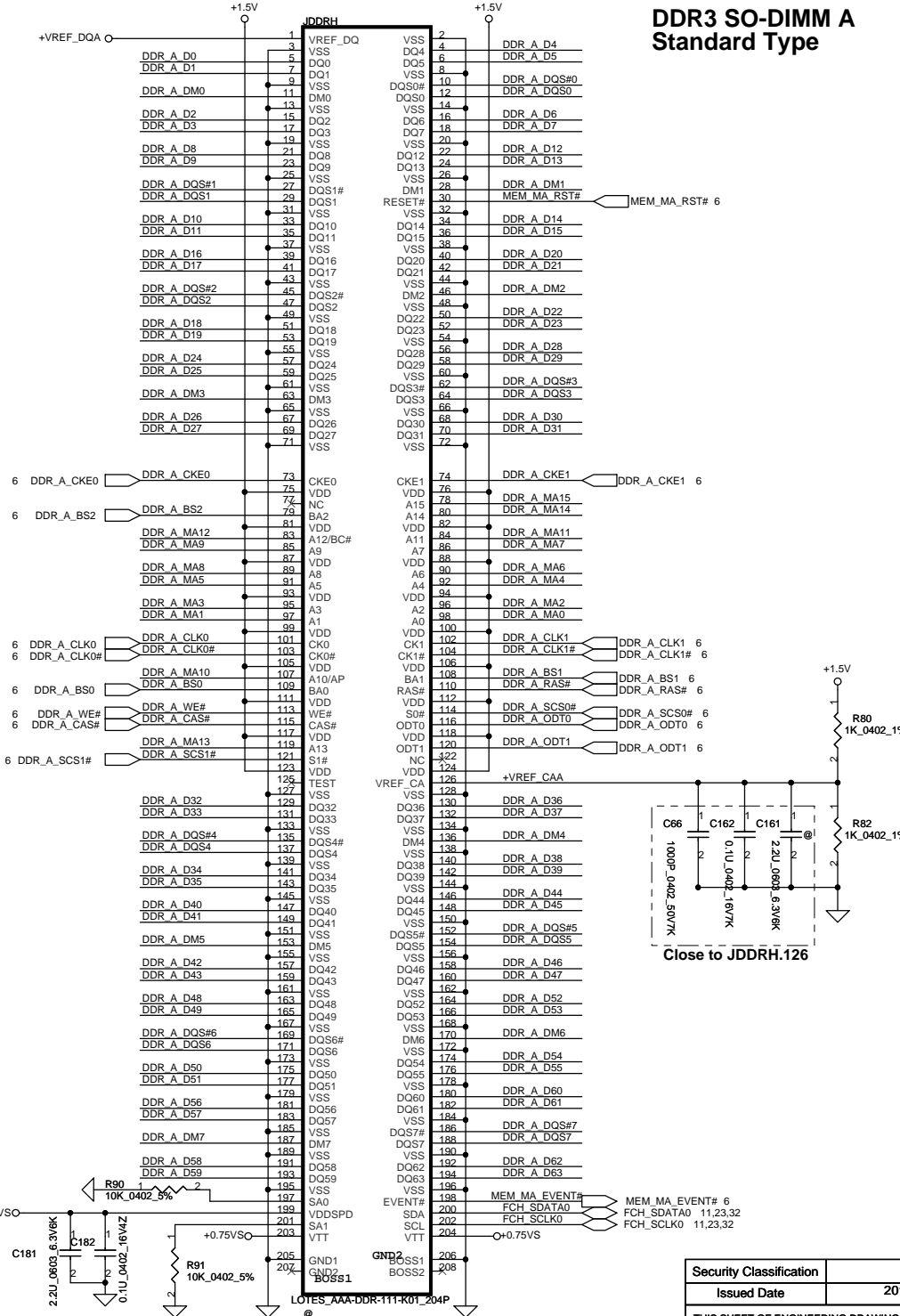


Panel PWM



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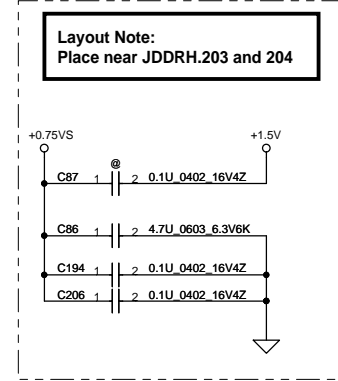
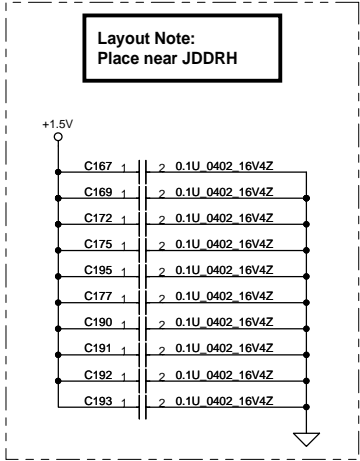
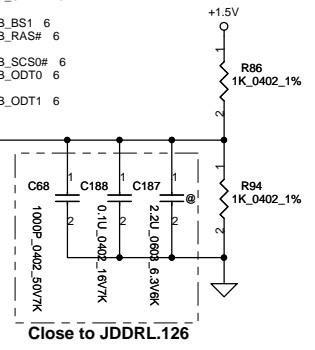
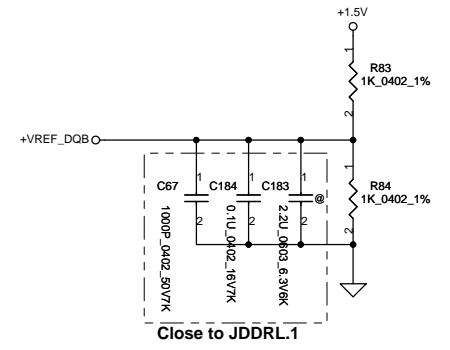
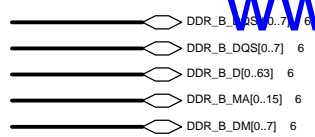
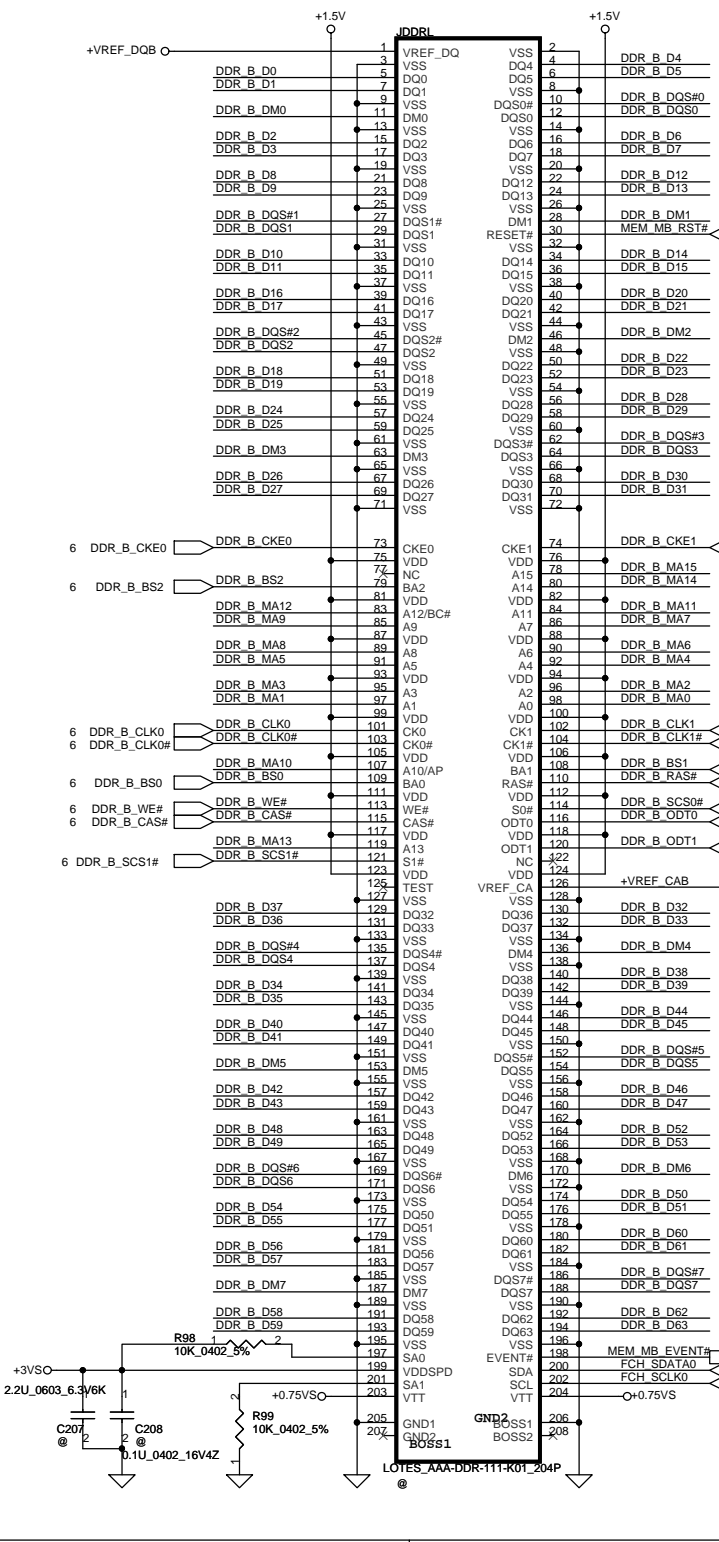
DDR3 SO-DIMM A Standard Type



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DDR3 SO-DIMM B Standard Type



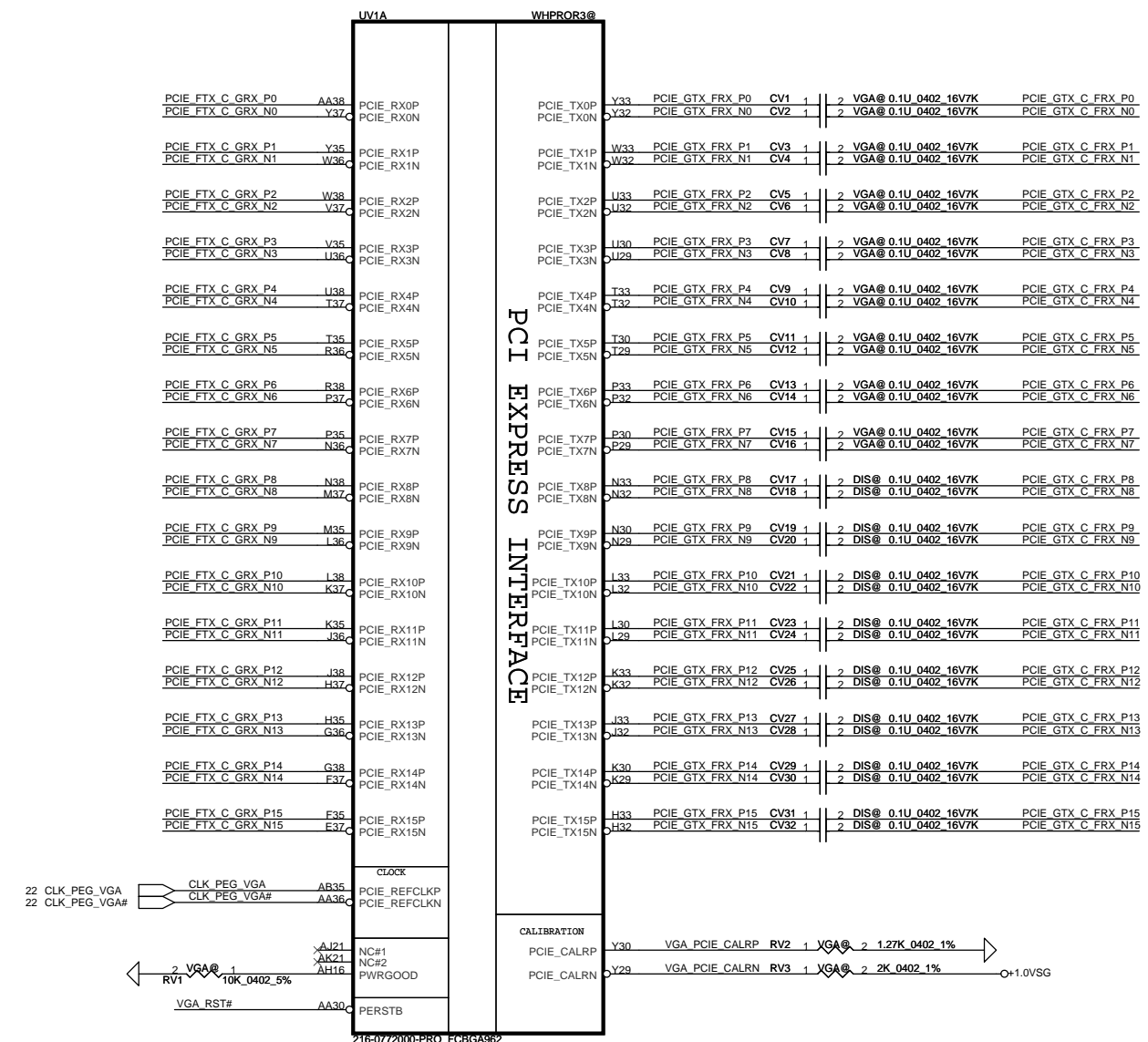
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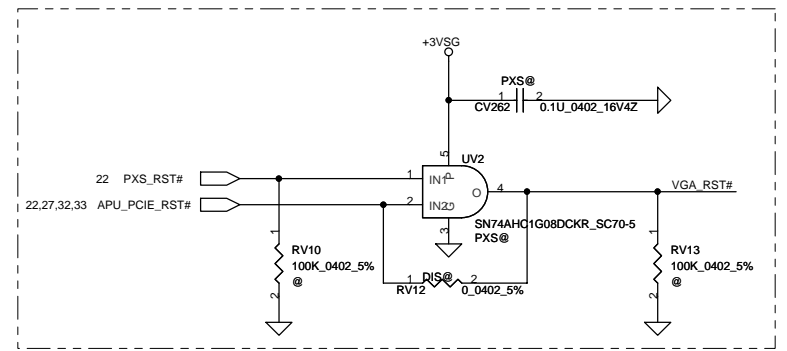
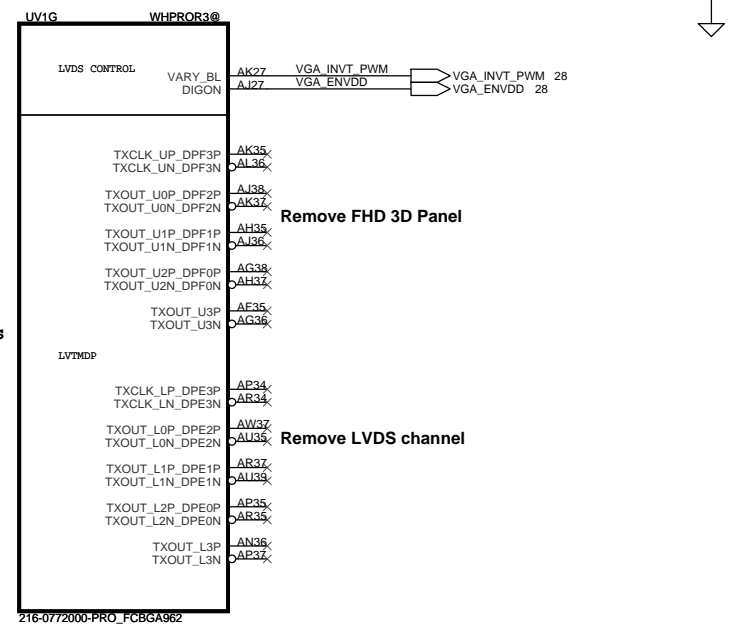
5 PCIE_FTX_C_GRX_P0[0..15] PCIE_FTX_C_GRX_P0[0..15]
 5 PCIE_FTX_C_GRX_N0[0..15] PCIE_FTX_C_GRX_N0[0..15]

PCIE GTX C FRX P0[0..15] PCIE GTX_C_FRX_P0[0..15] 5
 PCIE GTX C FRX N0[0..15] PCIE GTX_C_FRX_N0[0..15] 5

VGA_INVTT_WM RV4 1 10K_0402_5%
 VGA_ENVDD RV5 1 10K_0402_5%



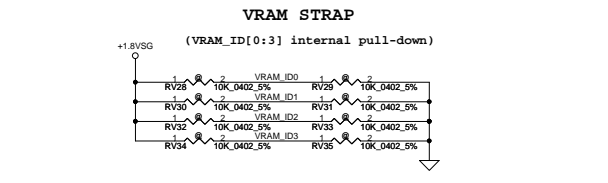
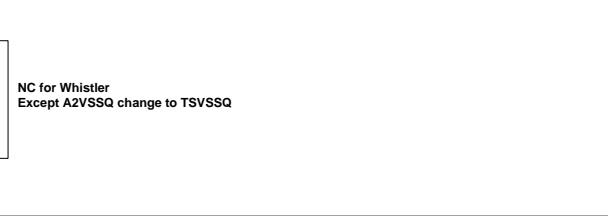
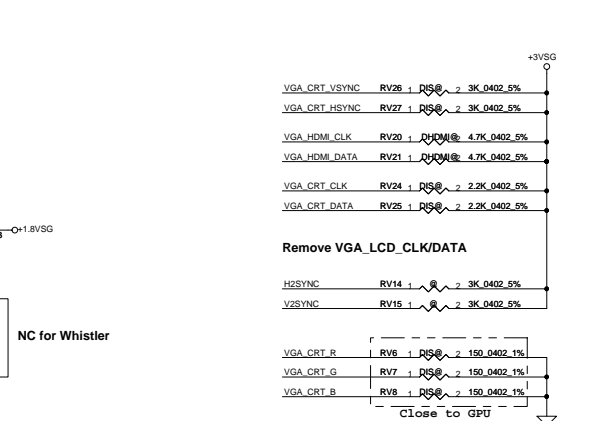
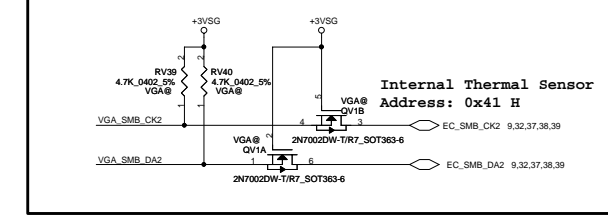
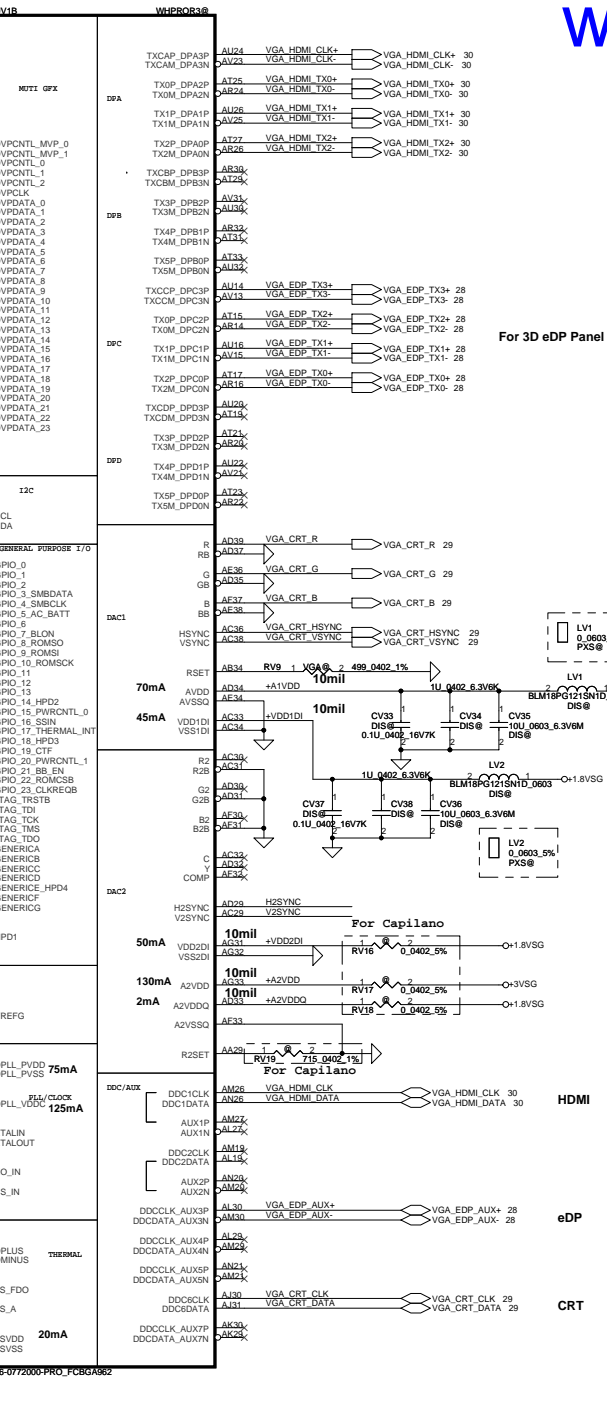
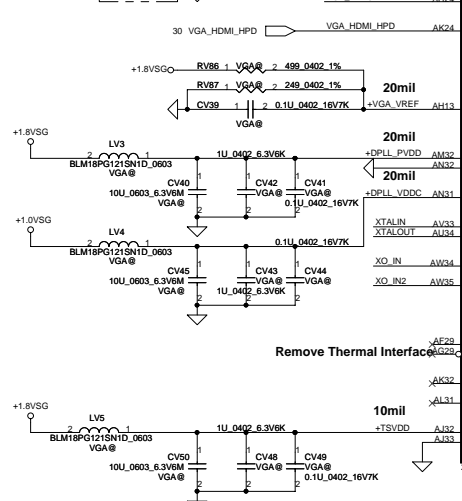
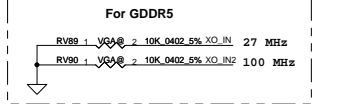
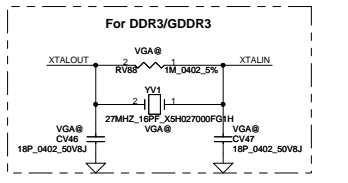
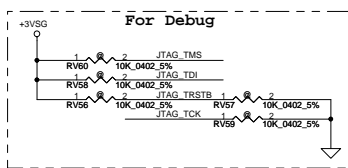
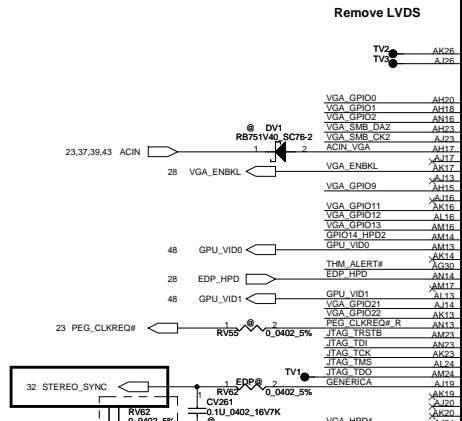
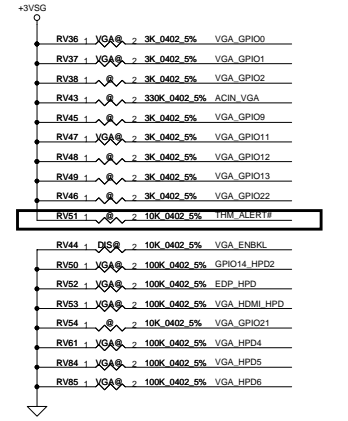
For PowerXpress



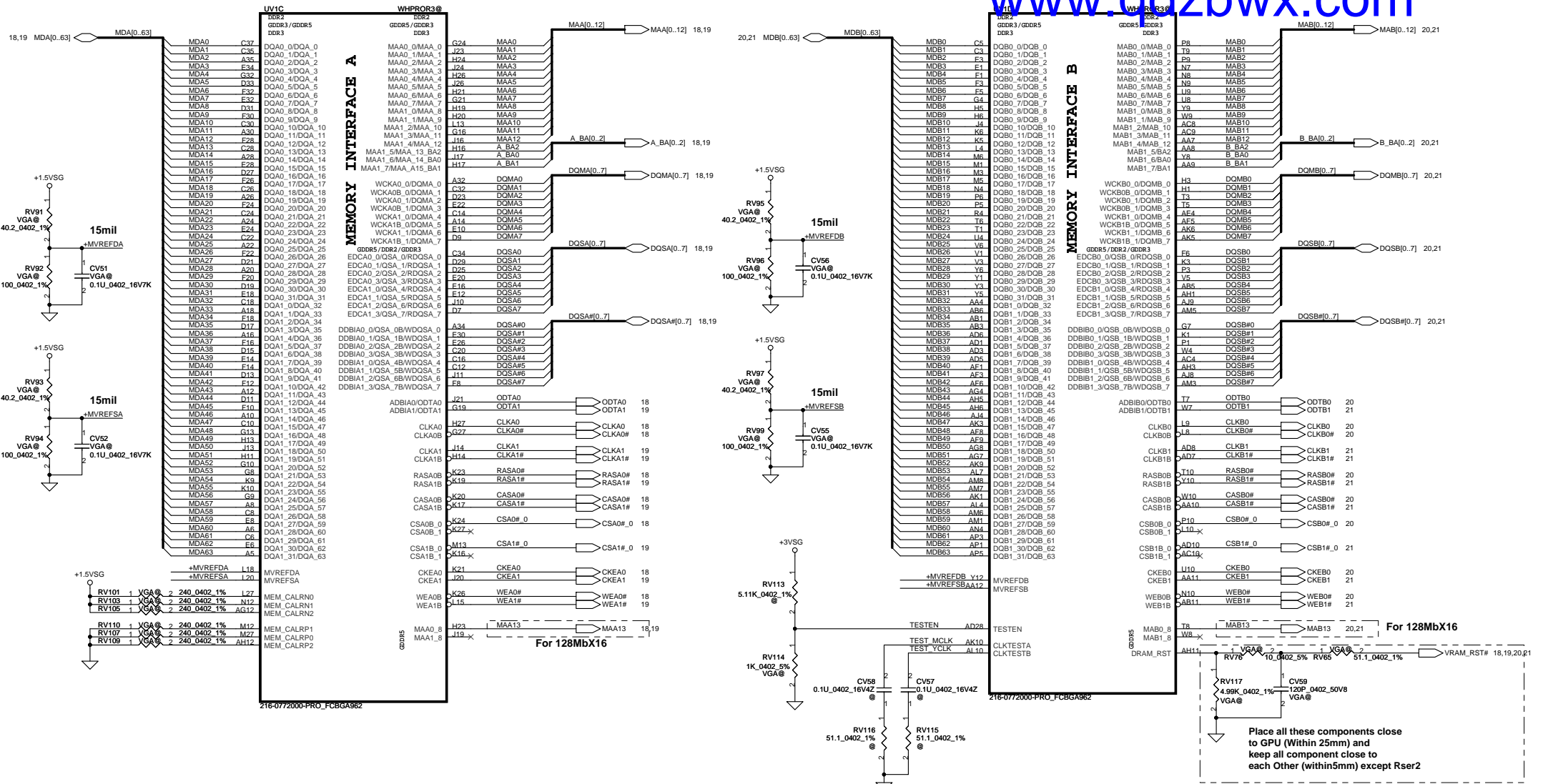
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Strap Name	Pin Name	Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	HSVSYNC (GENLK_VSYN)	VIP Device Strap Enable indicates to the software driver (Internal PD) 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines (Internal PD) 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable (Internal PD) 0: 50% Tx output swing 1: full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable (Internal PD) 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
CONFIG[2]	GPIO13	GPIO13,12,11 (config 2,1,0) : (Internal PD) a) If BIOS_ROM_EN = 1, then Config[2:0] defines the memory apertures CONFIG[3:0] 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 64 MB 011 32 MB 010	001
CONFIG[1]	GPIO12		
CONFIG[0]	GPIO11		
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device (Internal PD) 1: Enable 0: Disable	0
AUD[1]	HSYNC	00: No audio function; 1B: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected	11
AUD[0]	VSYNC	11: Audio for both DisplayPort and HDMI	
BIF_GEN2_EN	GPIO2	0: Advertises the PCI-E device as 2.5 GT/s capable at power-on 1: Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	NC

Don't have this strap for Whistler

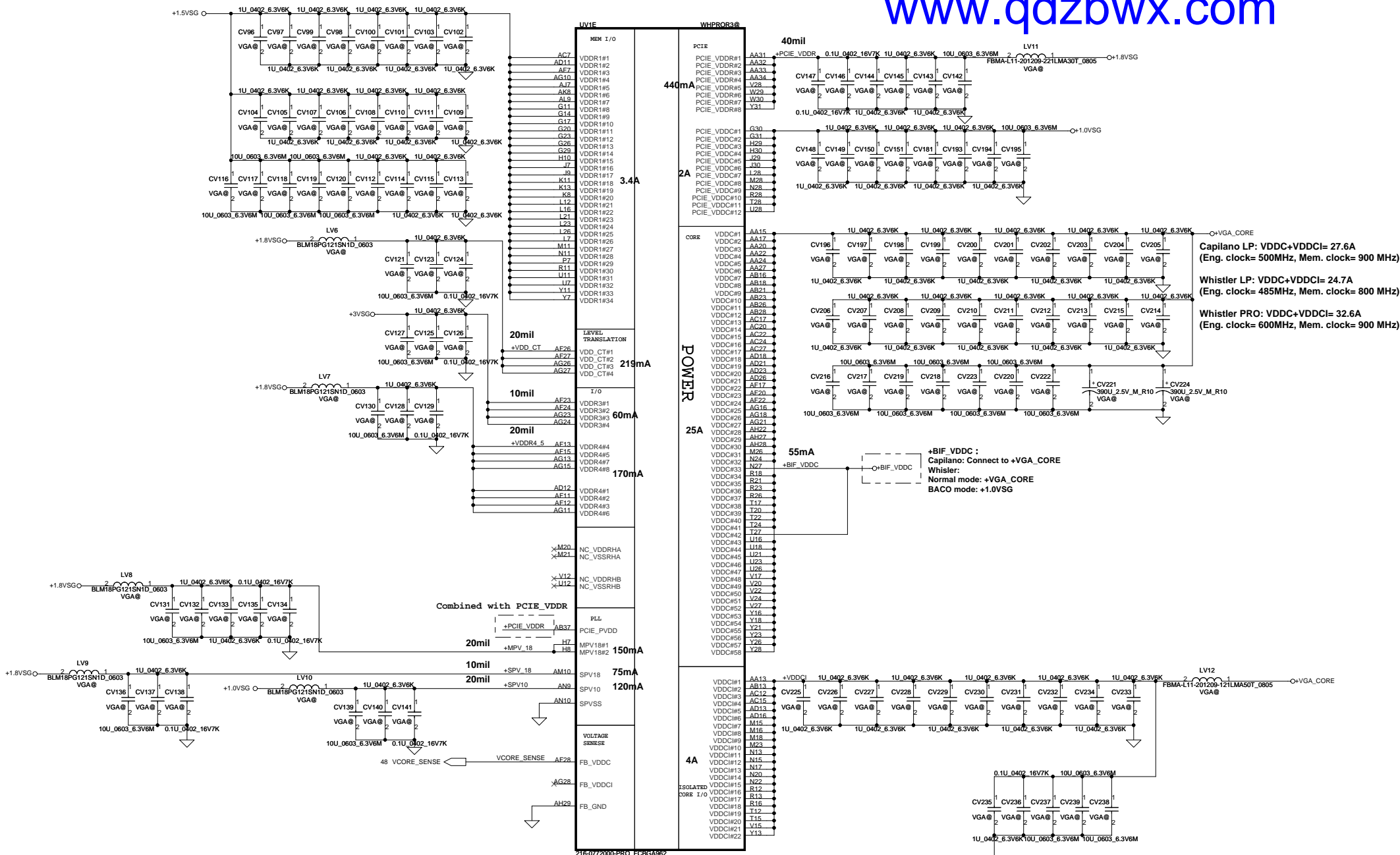


Location	DDR3 Type	Part Number	VRAM_ID0	VRAM_ID1	VRAM_ID2	VRAM_ID3
VRAM						
Samsung (1GB)	64Mx16 900MHz	K4W1G1646C-BC11	0	0	0	0
HYNIX (1GB)	64Mx16 900MHz	H5TQ1G63DFR-11C	1	0	0	0
Samsung (2GB)	128Mx16 900MHz	K4W2G1646C-HC11	0	1	0	0
HYNIX (2GB)	128Mx16 900MHz	H5TQ2G63BFR-11C	1	1	0	0

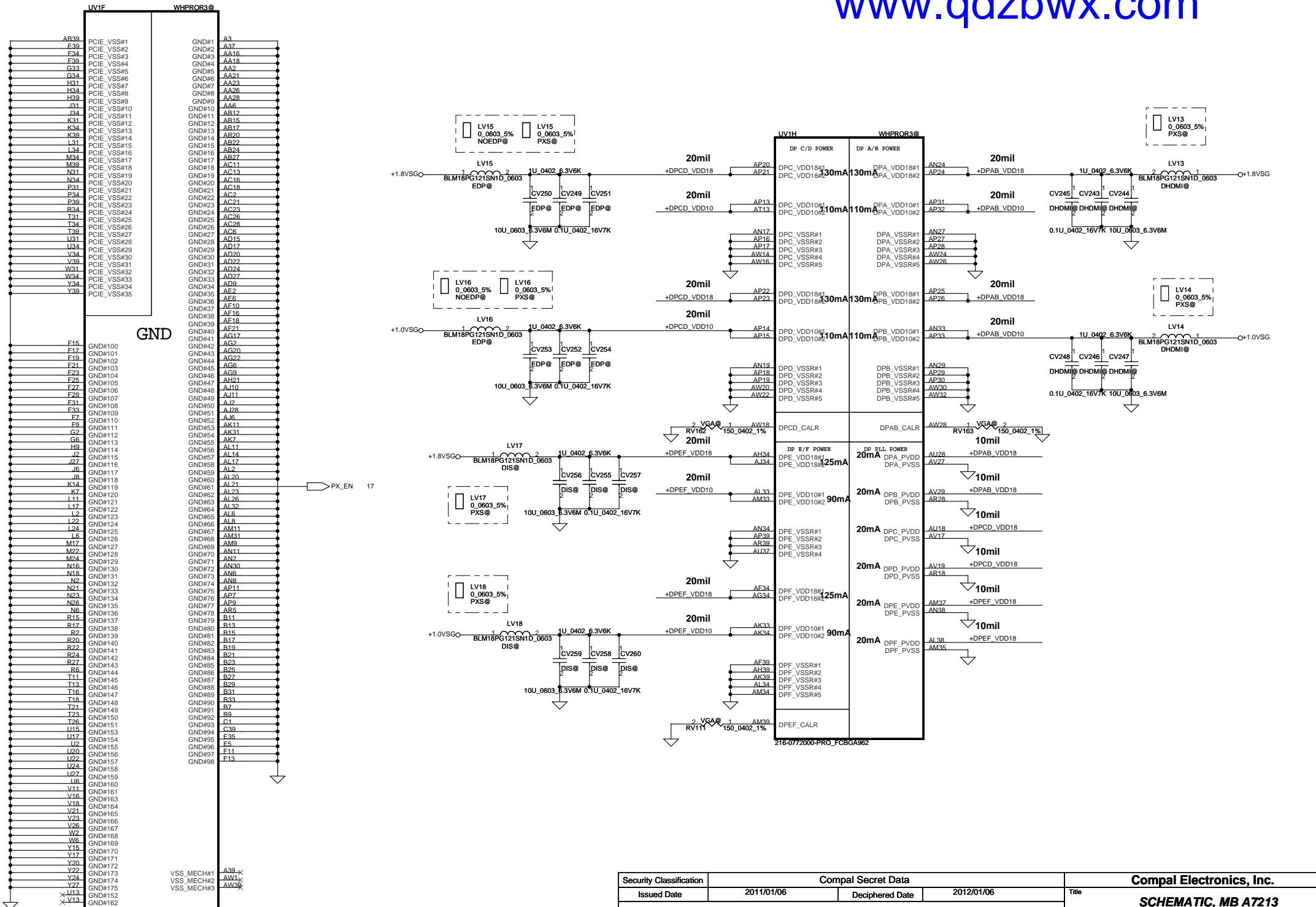


Place all these components close to GPU (Within 25mm) and keep all component close to each other (within5mm) except Rser2

Route 50ohm single-ended and 100ohm diff and keep short



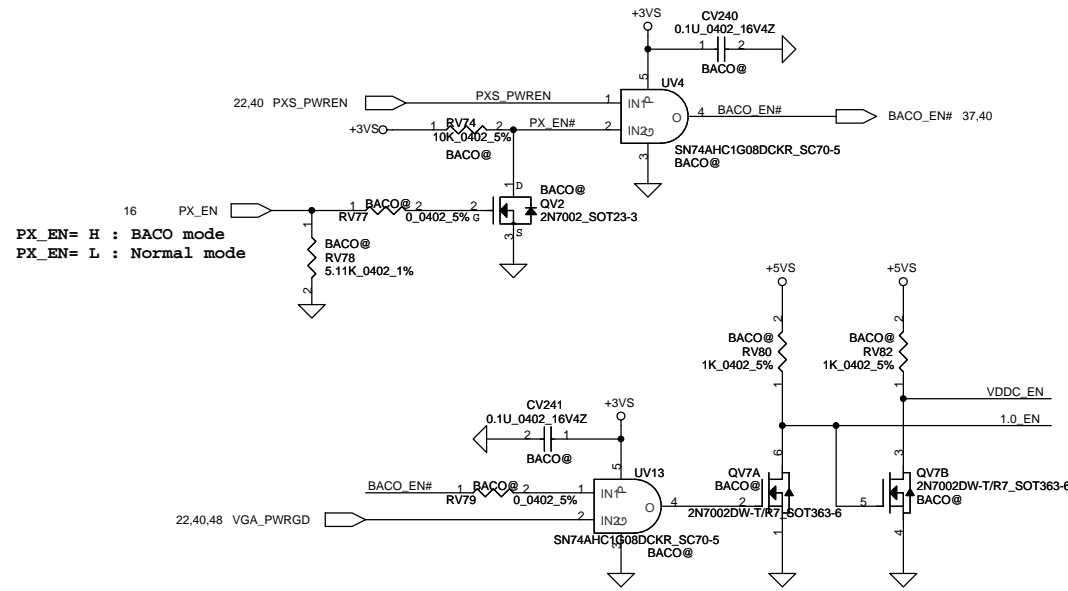
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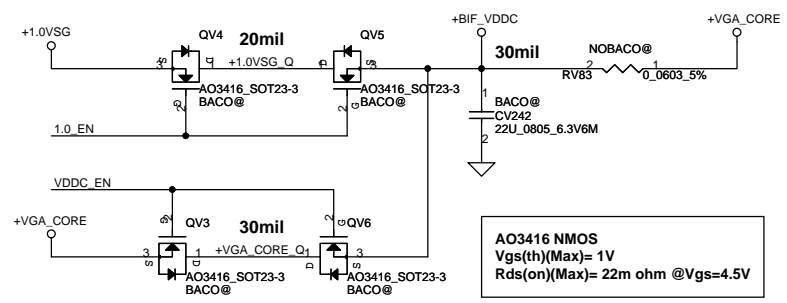
SCHEMATIC, MB A7213



PX_EN= H : BACO mode
 PX_EN= L : Normal mode

BACO mode:
 +VGA_CORE: off
 +1.5VSG: off
 +BIF_VDDC= +1.0VSG

Normal mode:
 +BIF_VDDC= +VGA_CORE

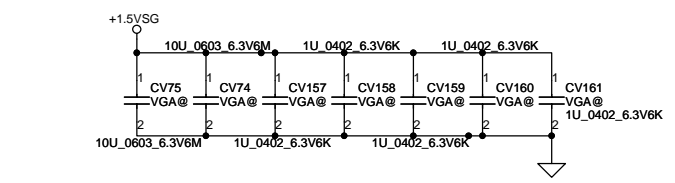
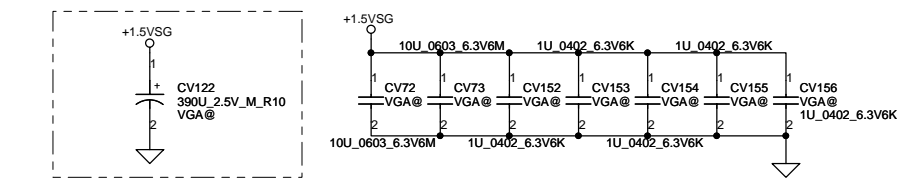
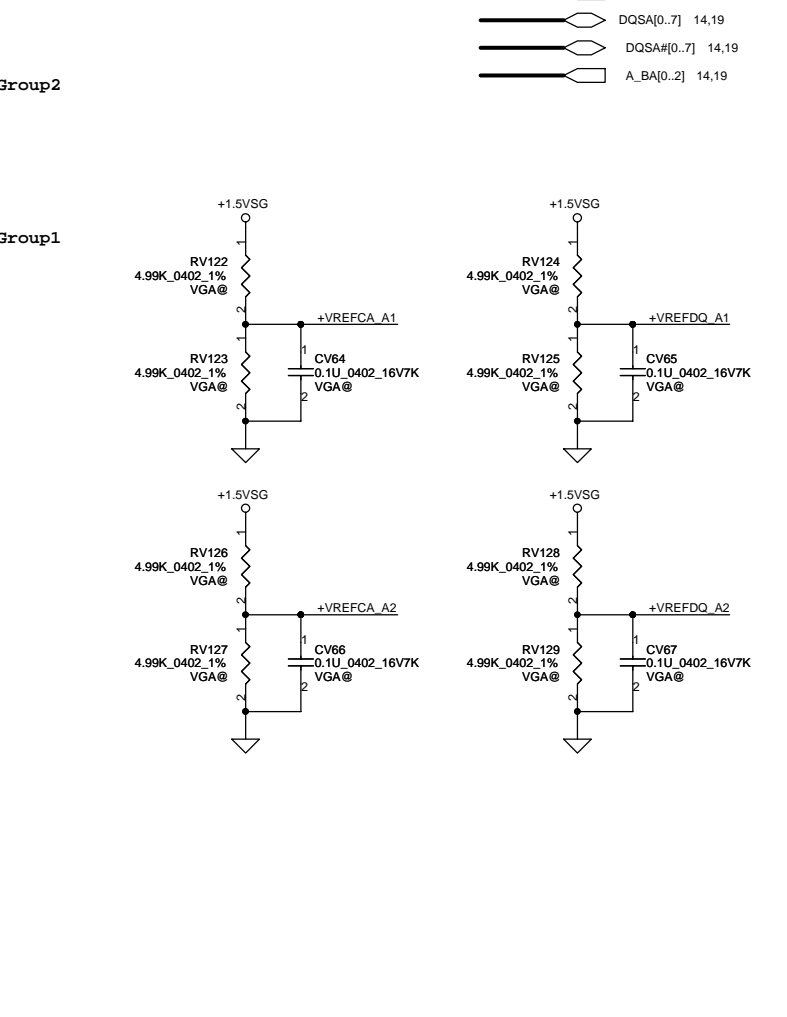
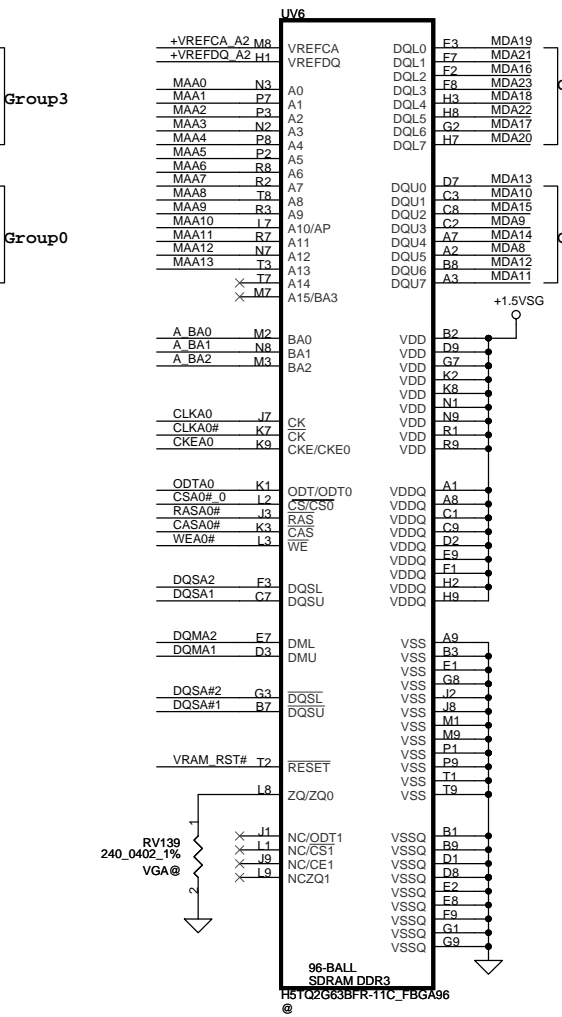
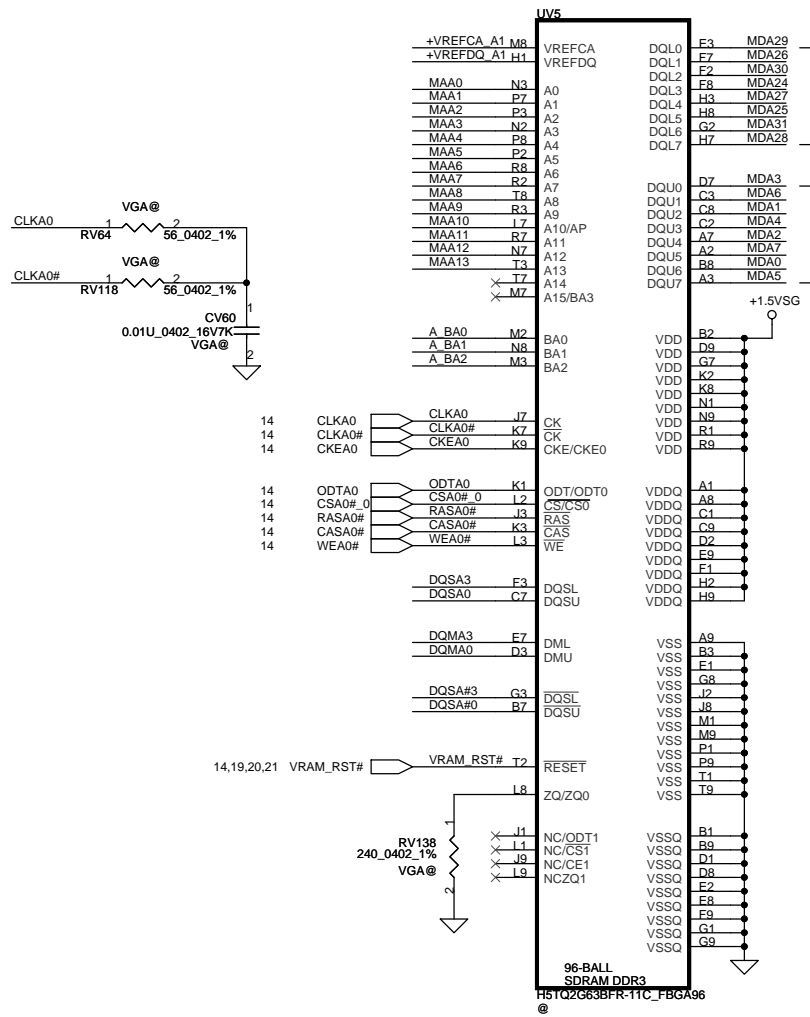


AO3416 NMOS
 Vgs(th)(Max)= 1V
 Rds(on)(Max)= 22m ohm @Vgs=4.5V

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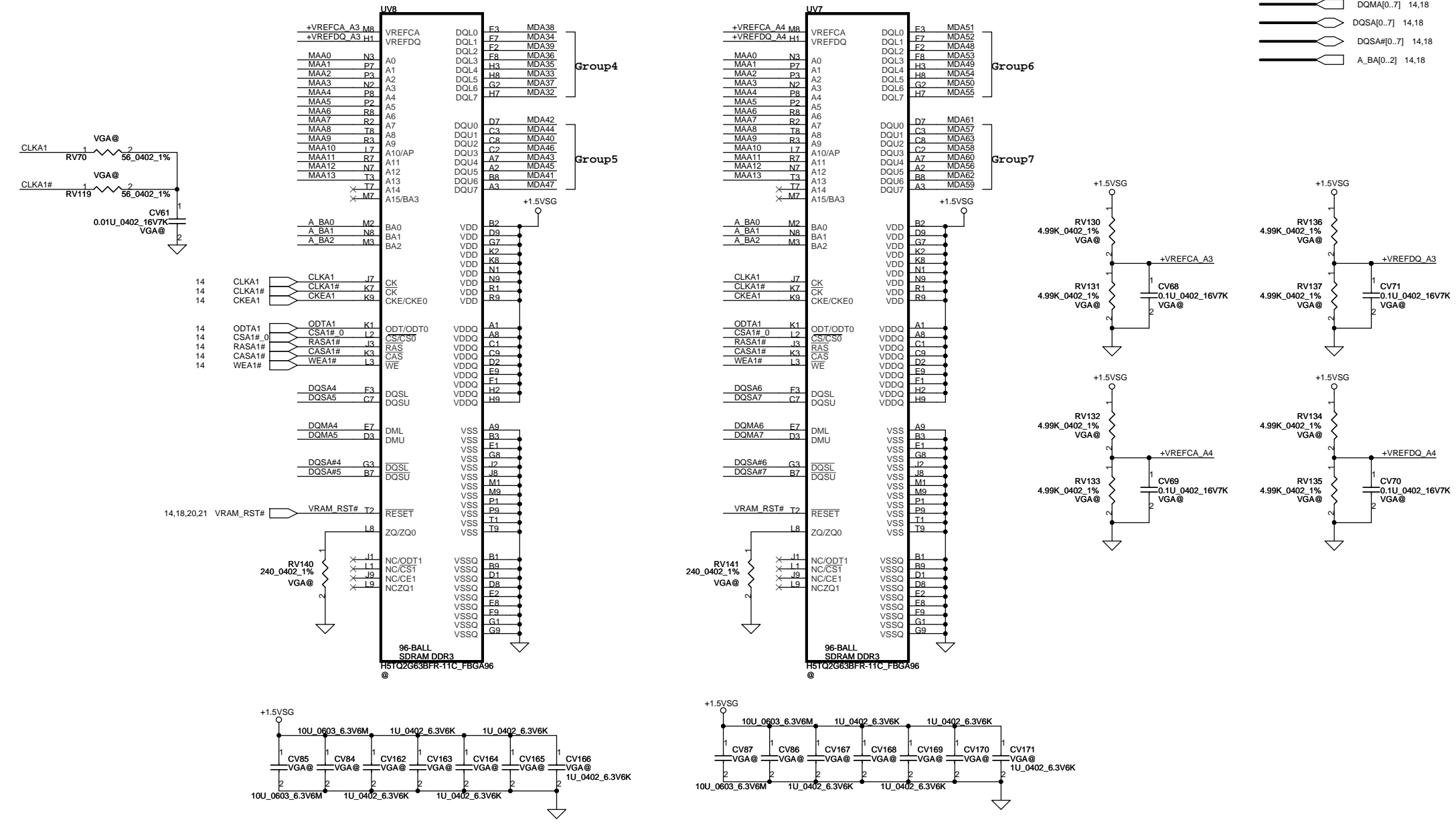
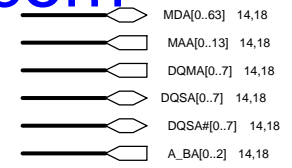
Memory Partition A - Lower 32 bits

- MDA[0..63] 14,19
- MAA[0..13] 14,19
- DQMA[0..7] 14,19
- DQSA[0..7] 14,19
- A_BA[0..2] 14,19



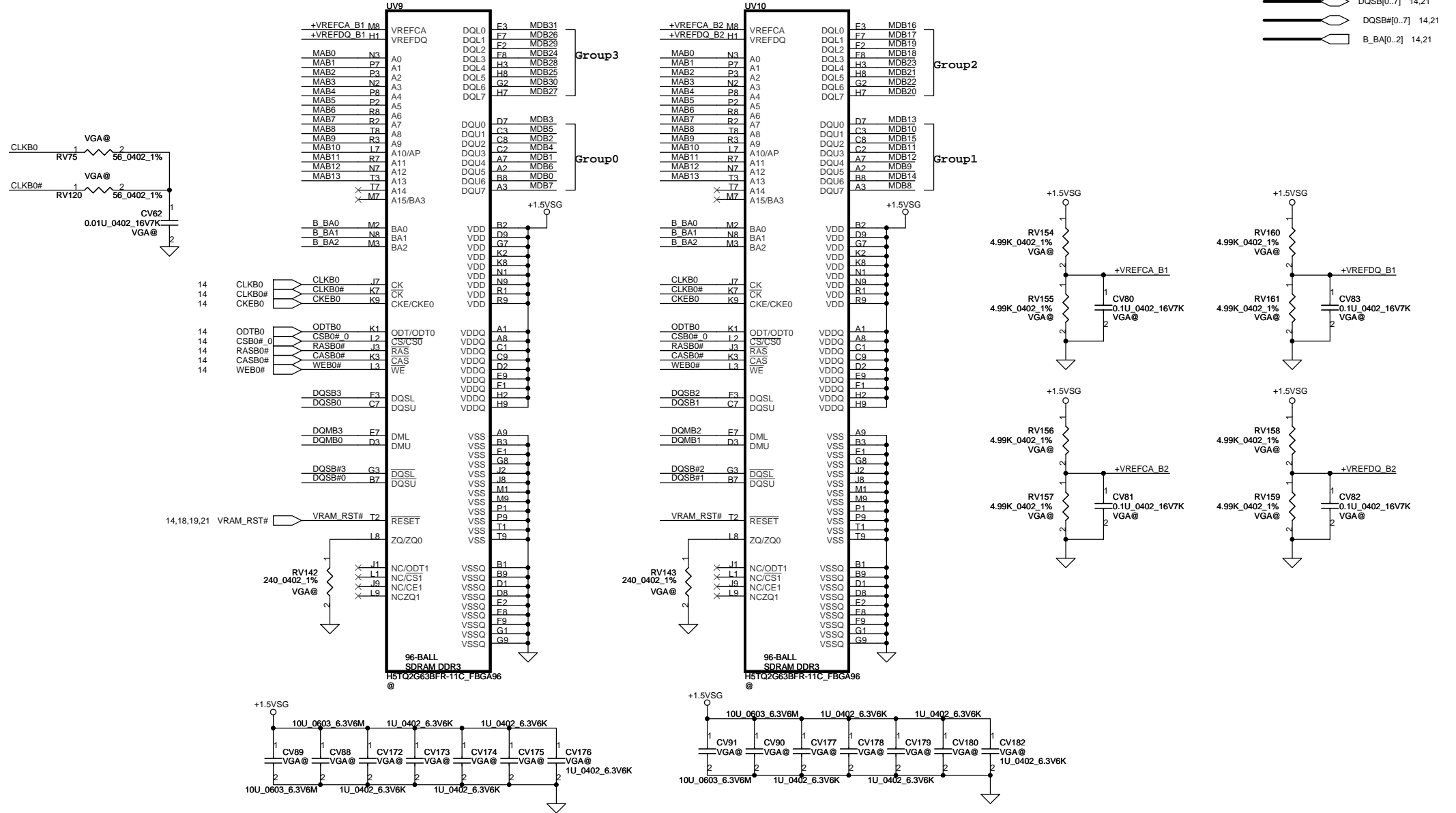
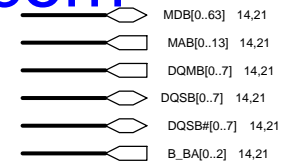
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Memory Partition A - Upper 32 bits



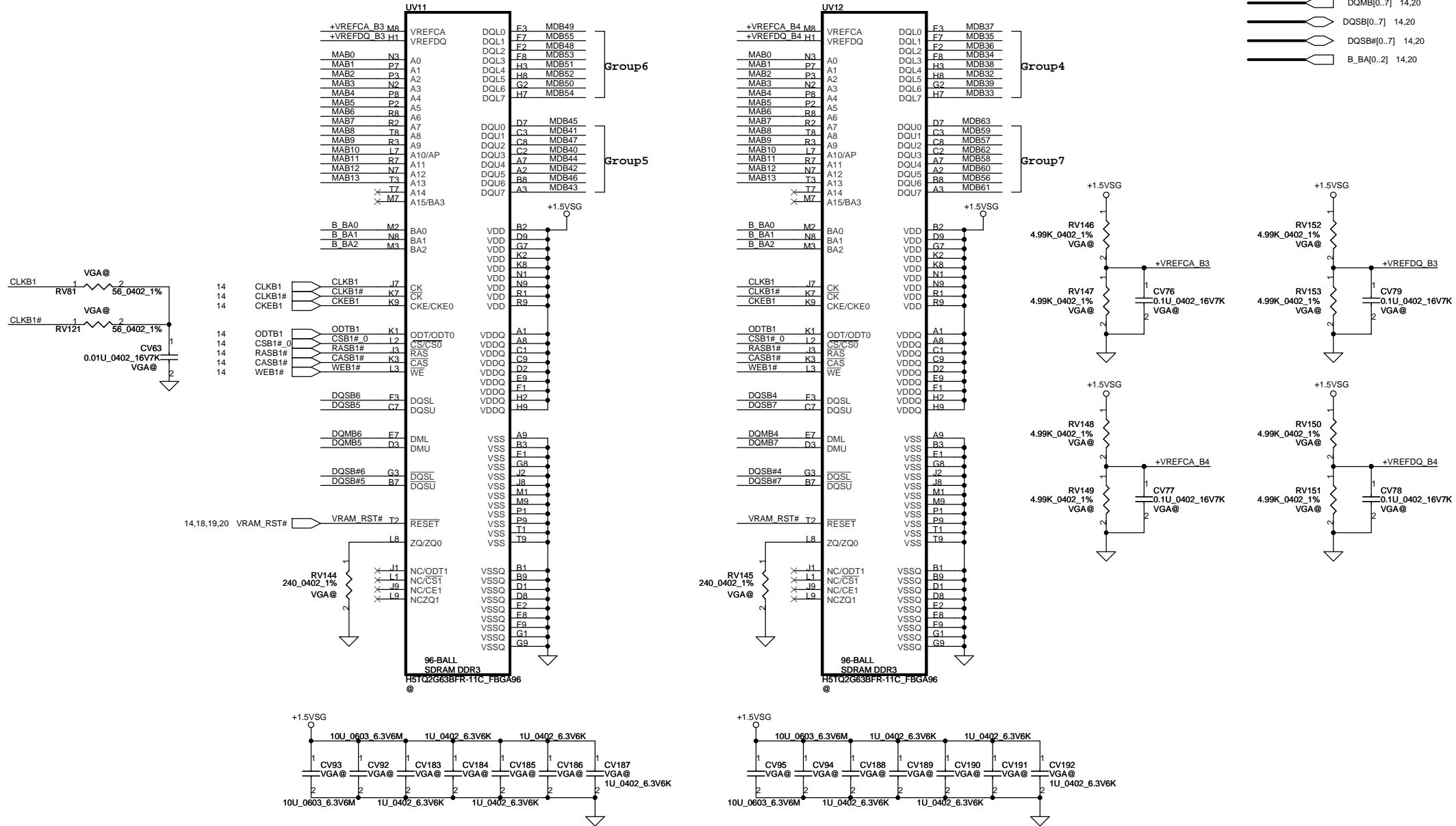
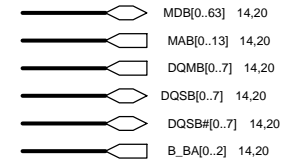
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Memory Partition C - Lower 32 bits

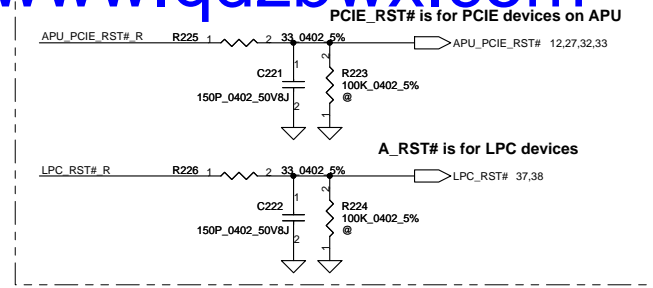


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Memory Partition C - Upper 32 bits



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3D_EN# (Internal 15K PU)

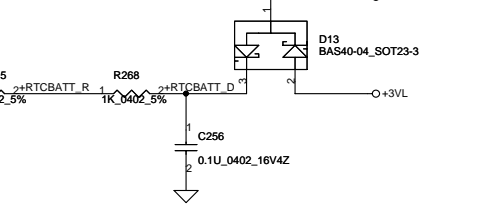
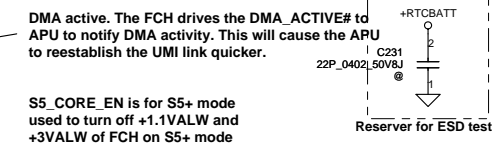
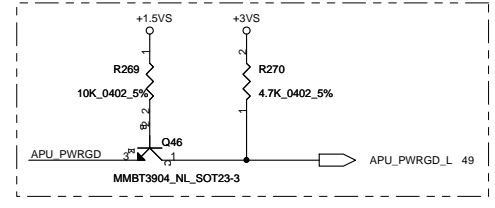
3D_EN#	H	L
SKU	Non-3D	3D (LVDS/eDP)

PXS_EN# (Internal 15K PU)

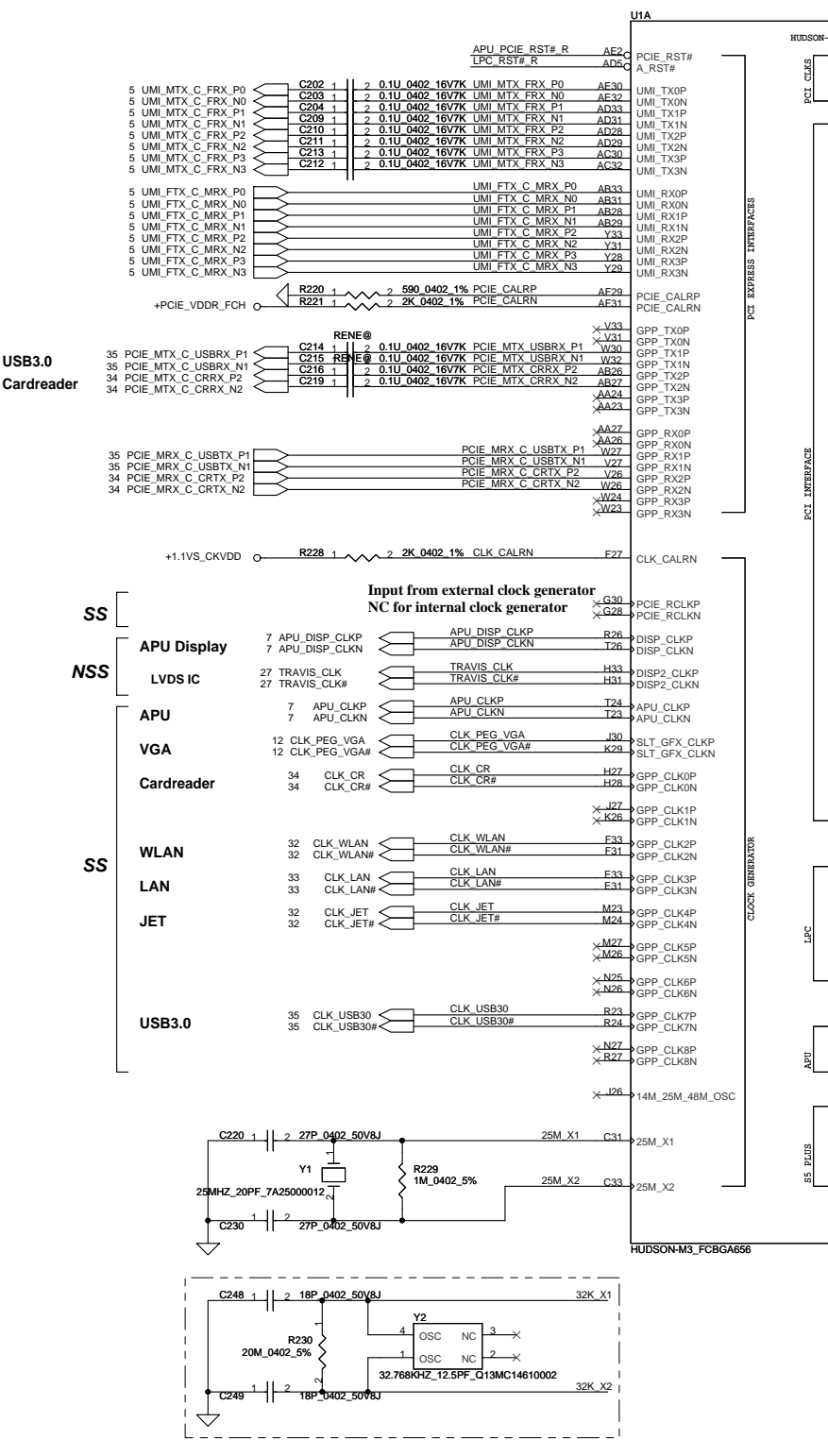
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SKU	Non-PowerXpress	PowerXpress

CROSS_EN# (Internal 8.2K PU)

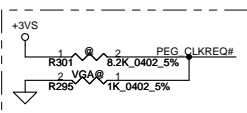
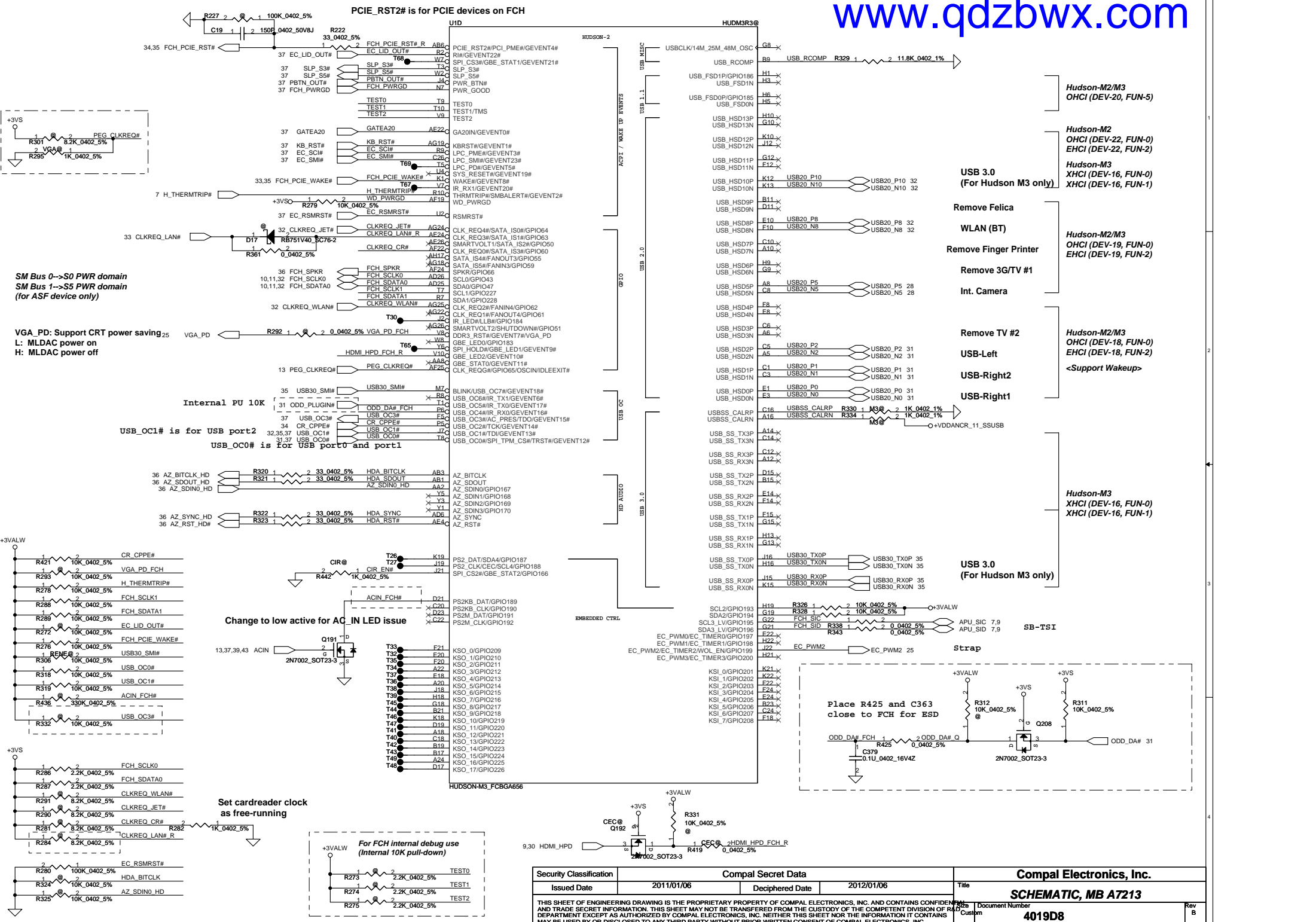
CROSS_EN#	H	L
SKU	Non-CrossFire	CrossFire



CMOS Setting Place under DDR Door



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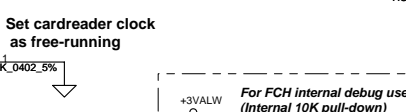
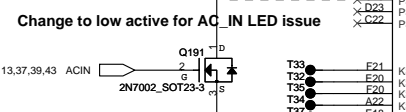
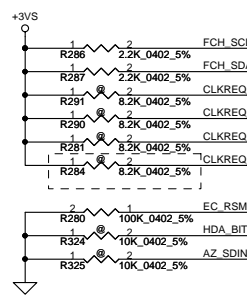
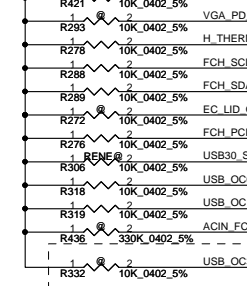
SM Bus 0->S0 PWR domain
SM Bus 1->S5 PWR domain
(for ASF device only)

VGA_PD: Support CRT power saving
L: MLDAC power on
H: MLDAC power off

Internal PU 10K
USB_OC1# is for USB port2
USB_OC0# is for USB port0 and port1

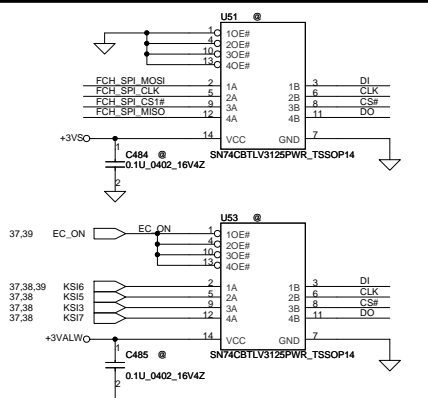
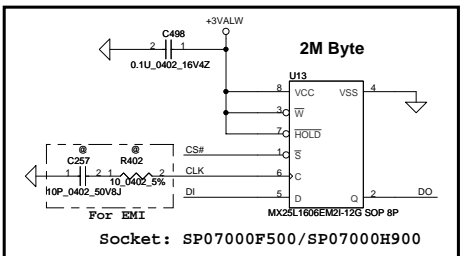
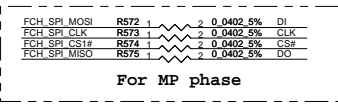
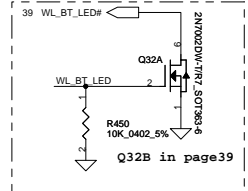
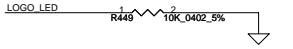
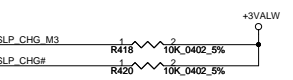
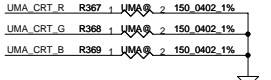
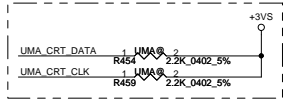
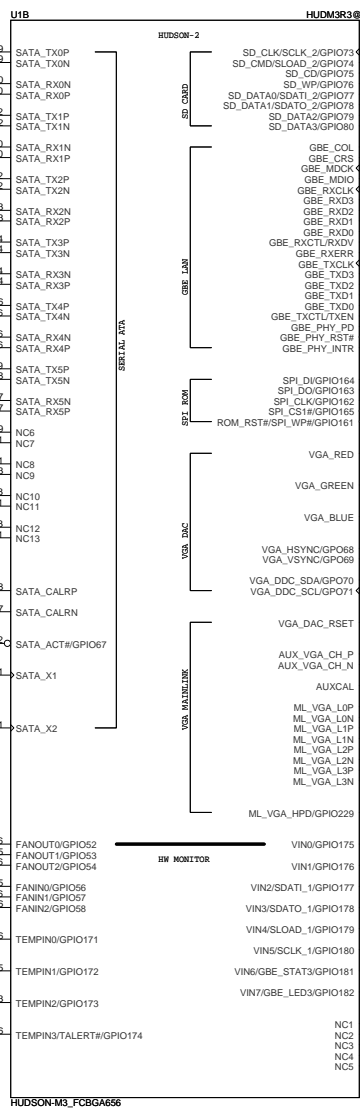
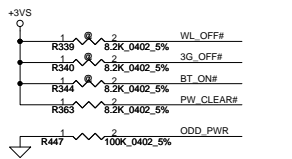
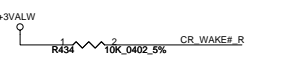
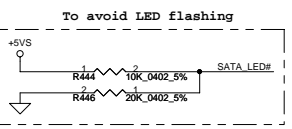
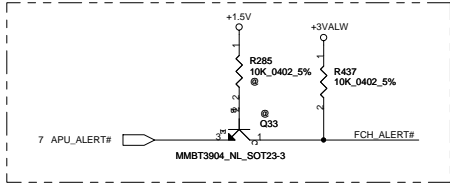
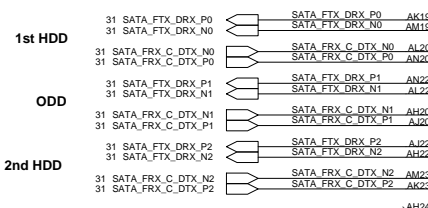
36 AZ_BITCLK_HD
36 AZ_SDOUT_HD
36 AZ_SDINO_HD

36 AZ_SYNC_HD
36 AZ_RST_HD#



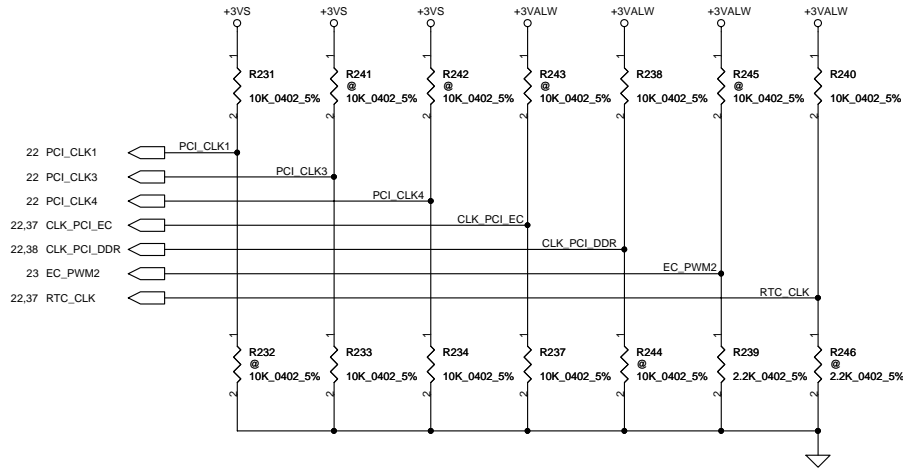
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HDMI_EN#	H	L
SKU	Non-HDMI SKU	HDMI SKU



STRAP PINS

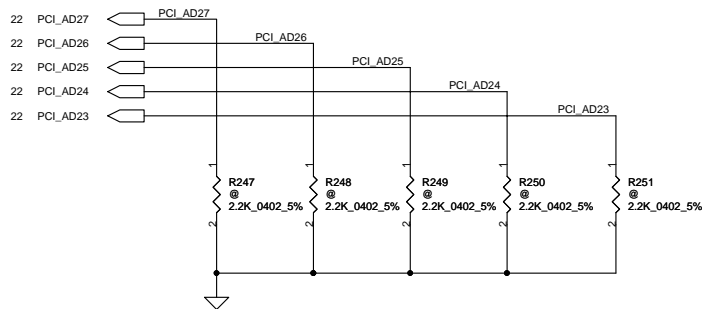
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	ENABLE DEBUG STRAP	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED	LPC ROM (INTERNAL 10K PULL-UP)	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	DISABLE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



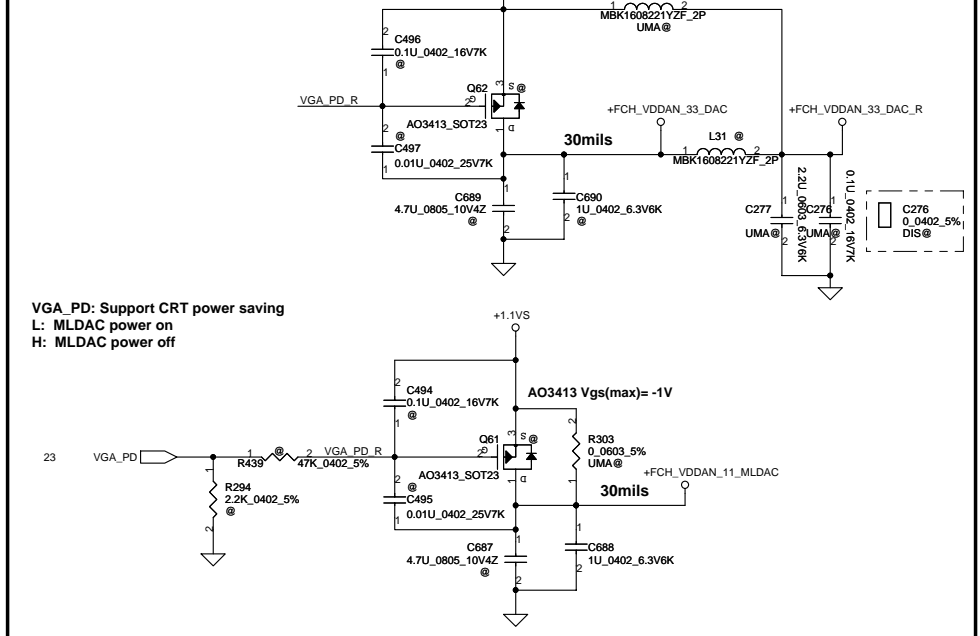
DEBUG STRAPS

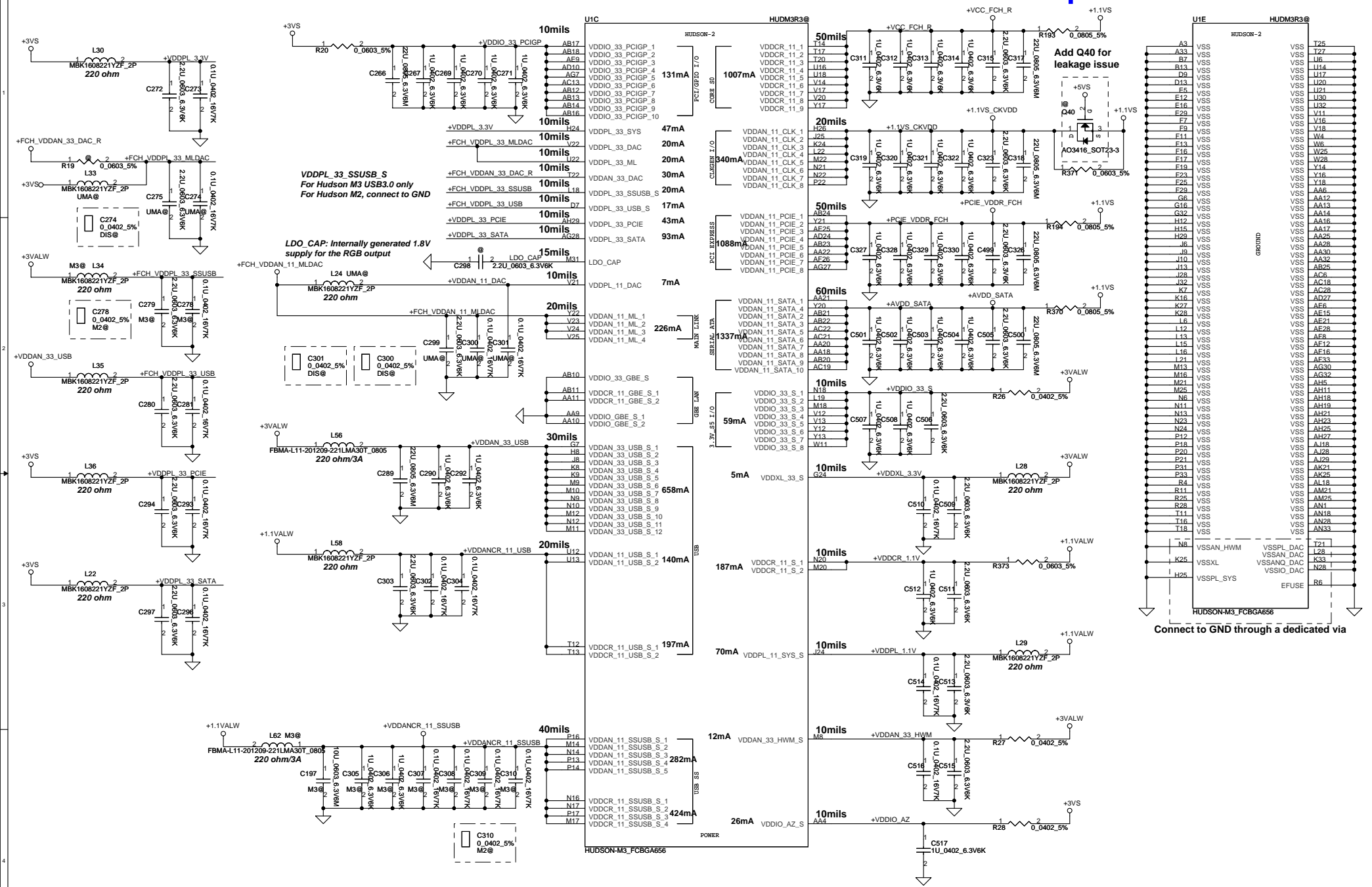
FCH HAS 15K INTERNAL PU-UP FOR PCI_AD[27:23]

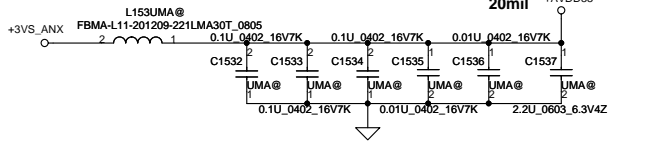
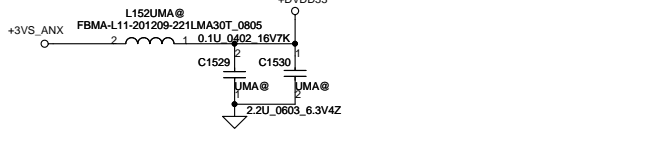
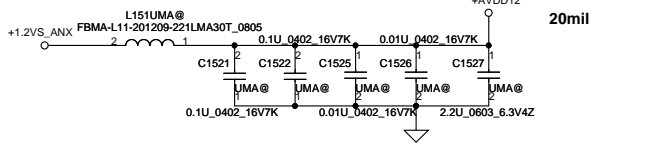
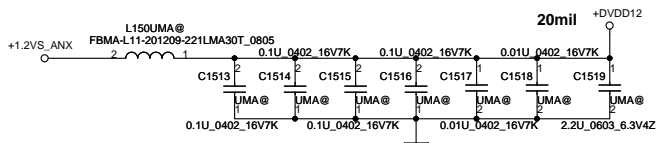
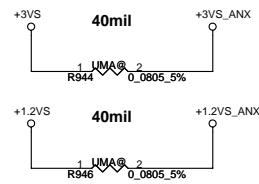
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



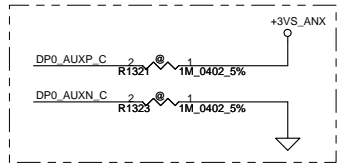
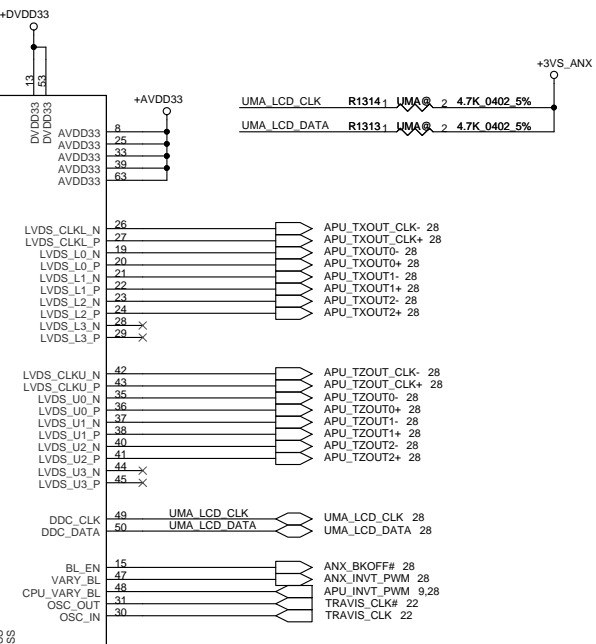
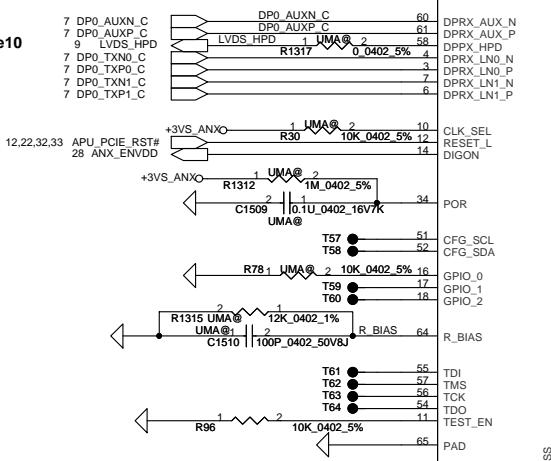
CRT Power Down Circuit







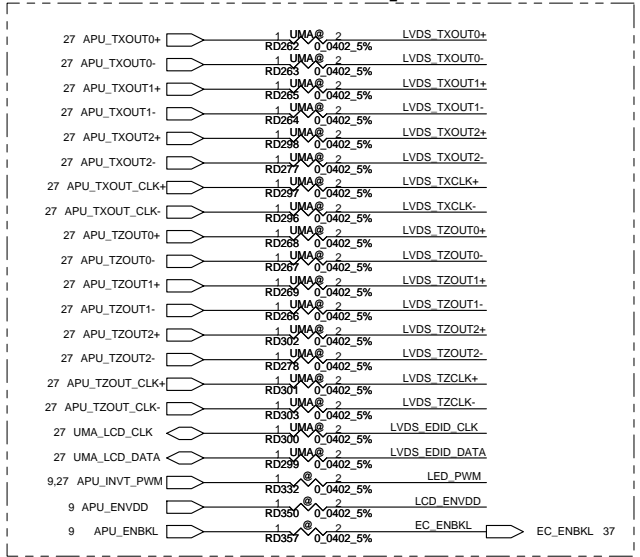
PD 100K at Page10



Place via on each trace bus and let resistor very close the via.

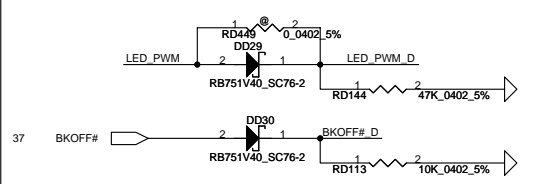
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For UMA & PowerXpress

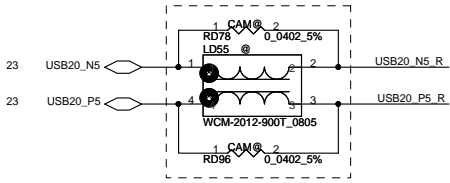


Close to LVDS Connector

To prevent EC pin damage



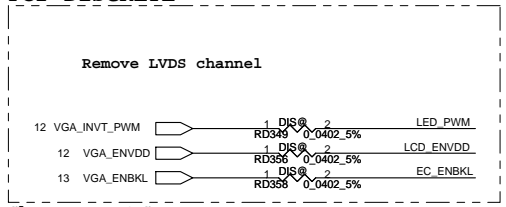
Reserve for EMI request



EC PWM

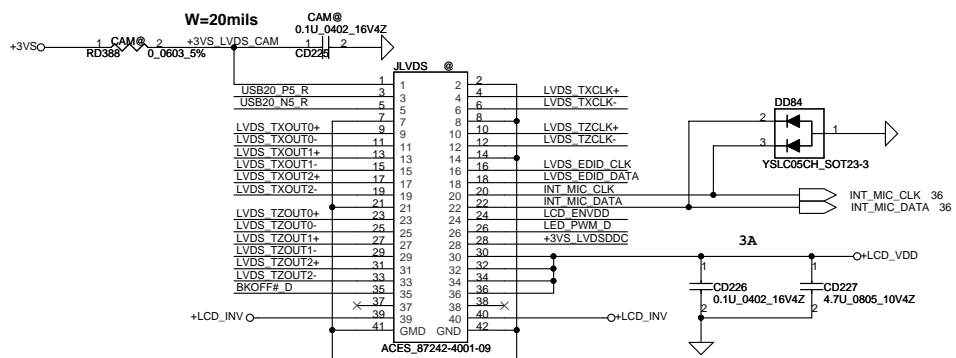


For DISCRETE

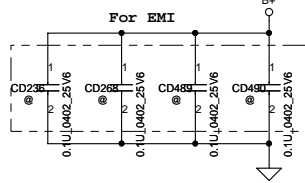
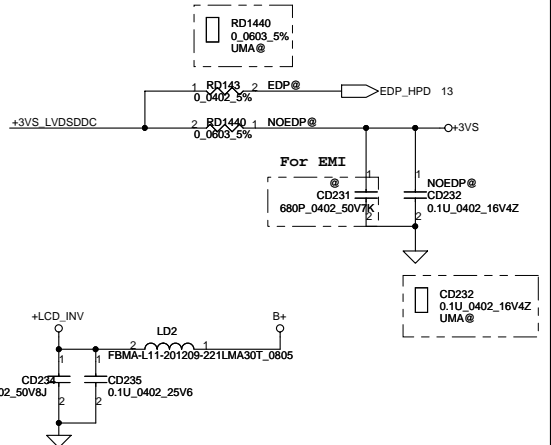
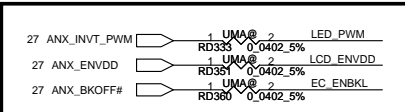


Close to LVDS Connector

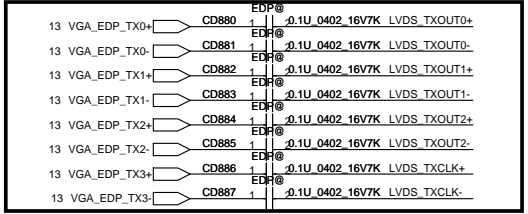
LCD/PANEL BD. Conn.



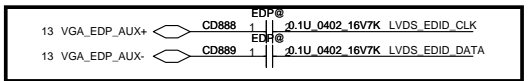
For LVDS Translator



DISCRETE for 3D eDP Panel



Close to LVDS1 Connector



Close to LVDS Connector

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SCHEMATIC, MB A7213					

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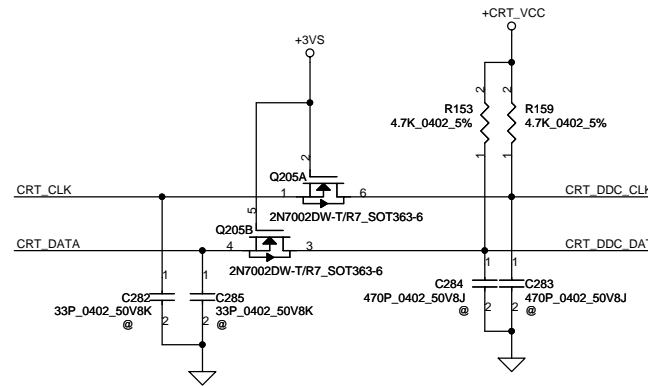
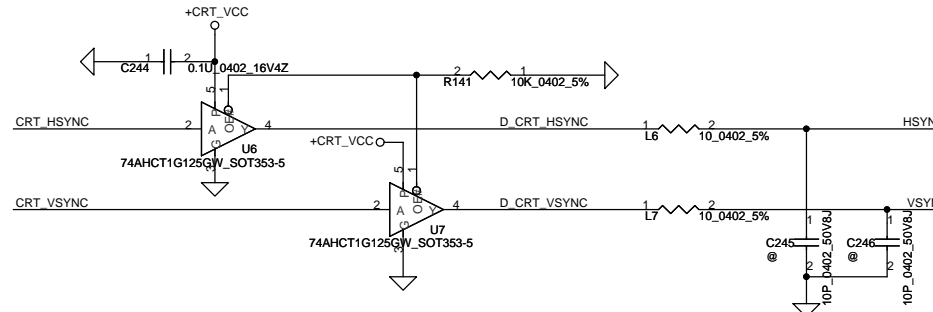
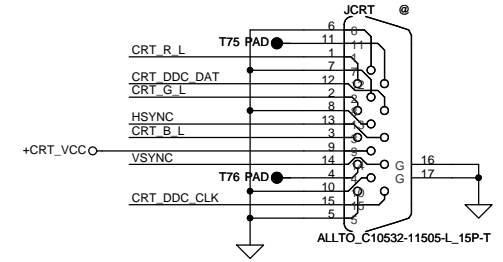
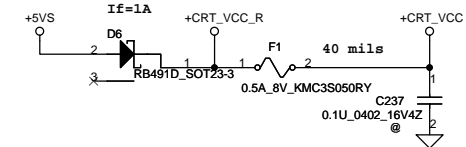
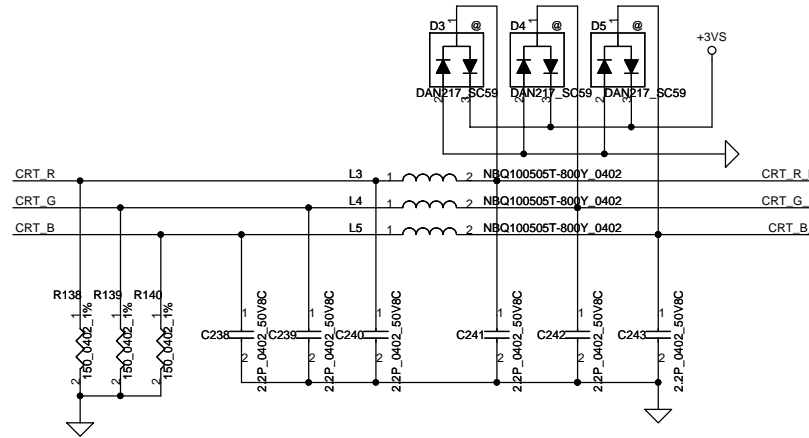
24	UMA_CRT_R	1	UMA@	2	CRT_R
		R200		0.0402_5%	
24	UMA_CRT_G	1	UMA@	2	CRT_G
		R204		0.0402_5%	
24	UMA_CRT_B	1	UMA@	2	CRT_B
		R211		0.0402_5%	
24	UMA_CRT_HSYNC	1	UMA@	2	CRT_HSYNC
		R213		0.0402_5%	
24	UMA_CRT_VSYNC	1	UMA@	2	CRT_VSYNC
		R235		0.0402_5%	
24	UMA_CRT_CLK	1	UMA@	2	CRT_CLK
		R236		0.0402_5%	
24	UMA_CRT_DATA	1	UMA@	2	CRT_DATA
		R261		0.0402_5%	

Close to CRT Connector

For DISCRETE

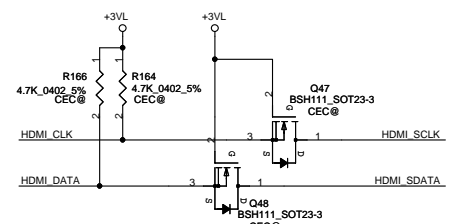
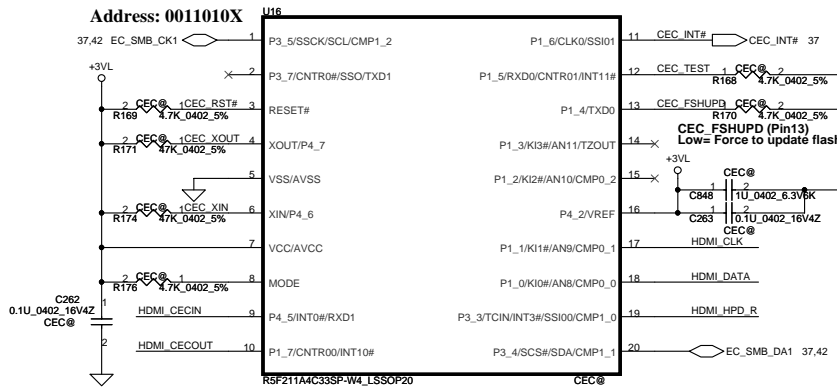
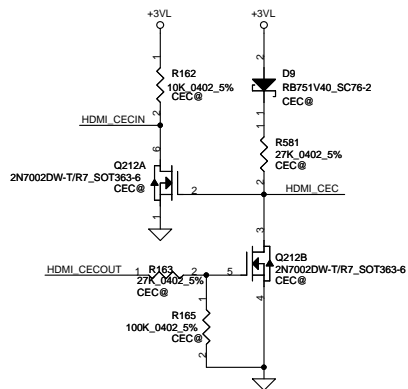
13	VGA_CRT_R	1	DIS@	2	CRT_R
		R178		0.0402_5%	
13	VGA_CRT_G	1	DIS@	2	CRT_G
		R181		0.0402_5%	
13	VGA_CRT_B	1	DIS@	2	CRT_B
		R167		0.0402_5%	
13	VGA_CRT_HSYNC	1	DIS@	2	CRT_HSYNC
		R177		0.0402_5%	
13	VGA_CRT_VSYNC	1	DIS@	2	CRT_VSYNC
		R179		0.0402_5%	
13	VGA_CRT_CLK	1	DIS@	2	CRT_CLK
		R209		0.0402_5%	
13	VGA_CRT_DATA	1	DIS@	2	CRT_DATA
		R256		0.0402_5%	

Close to CRT Connector

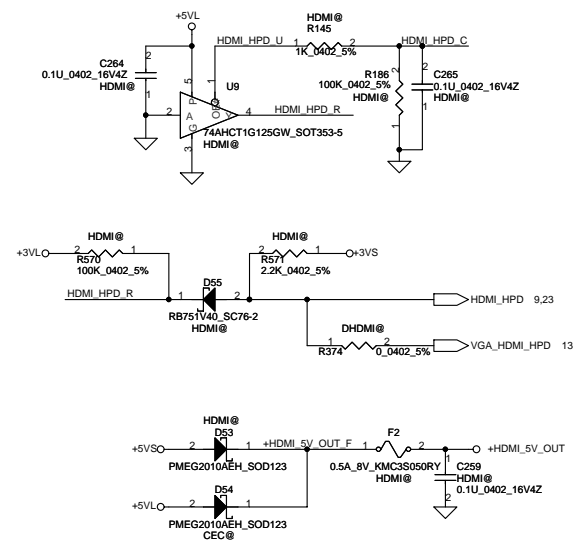
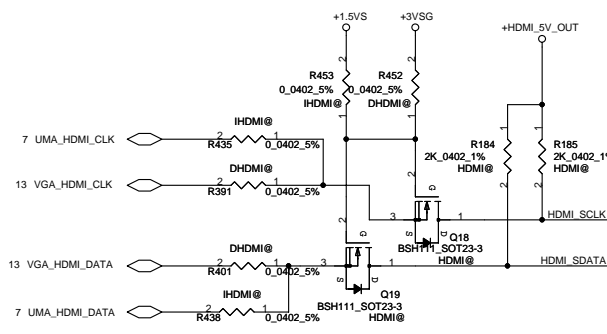
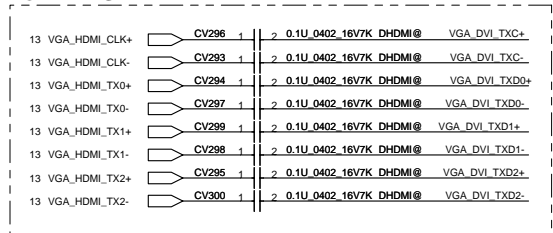


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				Document Number	Rev B
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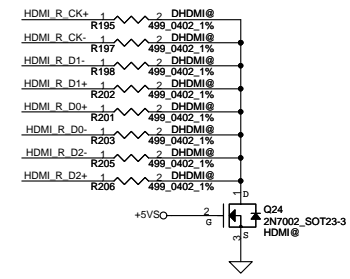
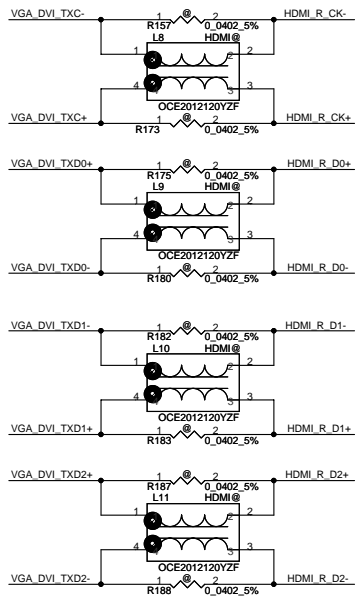
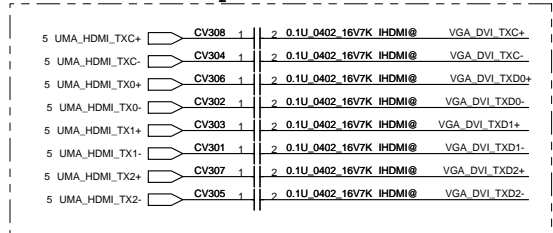
HDMI CEC Controller



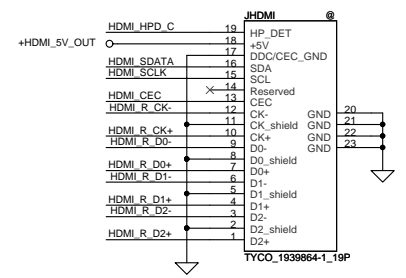
For DISCRETE



For UMA & PowerXpress



HDMI Connector

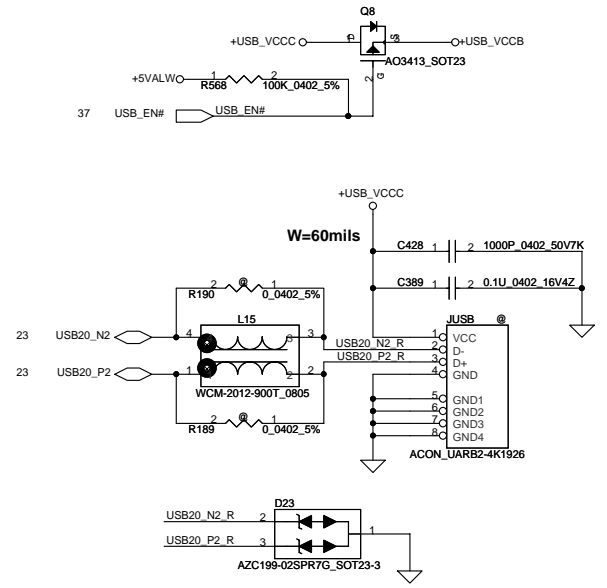
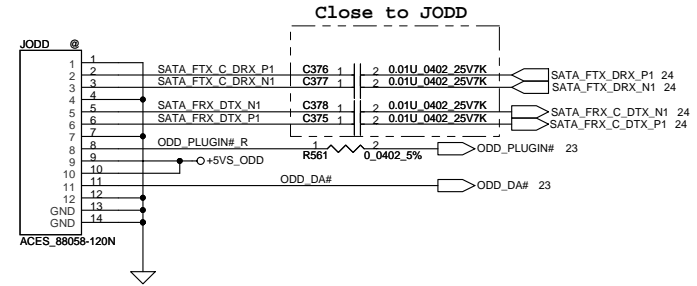
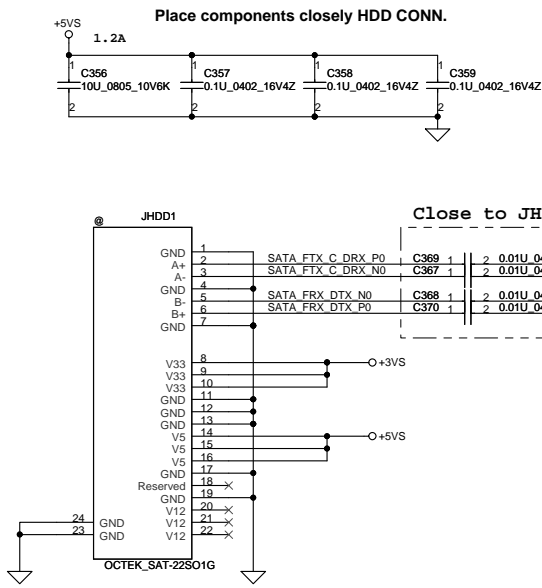


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SATA HDD Conn.

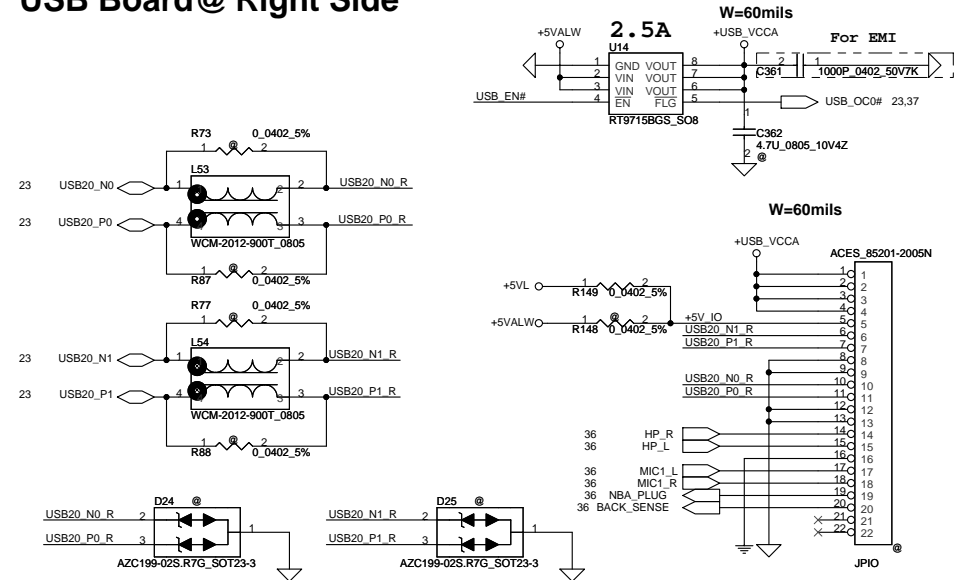
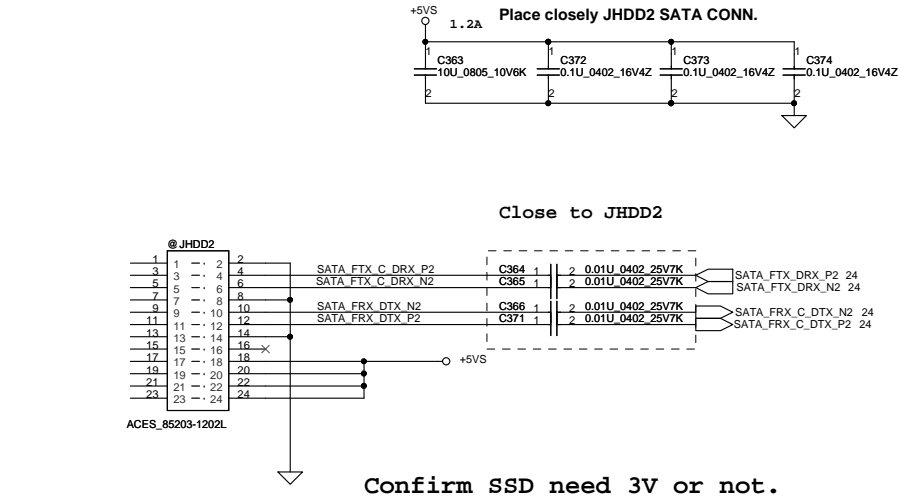
SATA ODD Conn.

USB Board @ Left Side



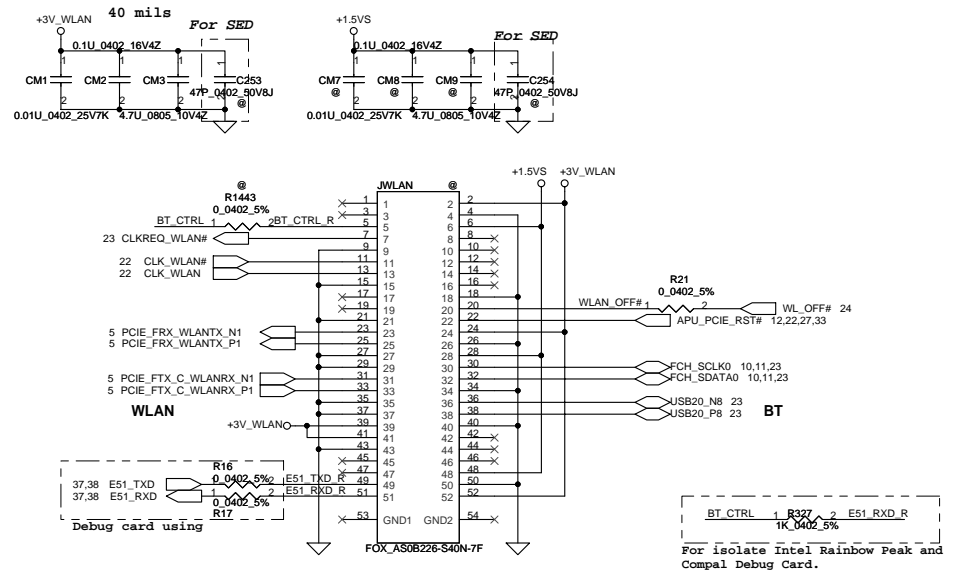
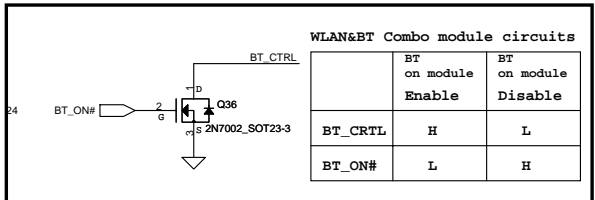
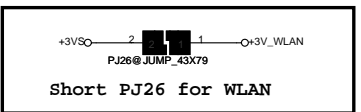
SATA 2nd HDD Conn.

USB Board @ Right Side



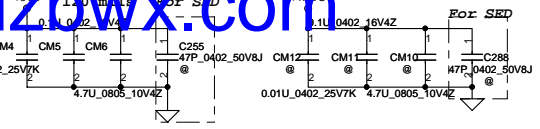
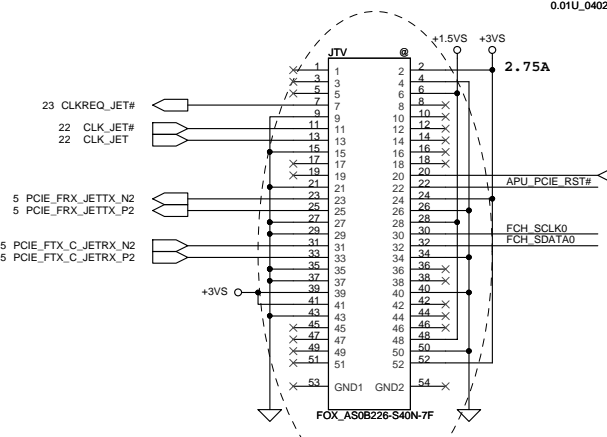
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				Date:	Monday, July 04, 2011
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Slot 1 Half PCIe Mini Card-WLAN

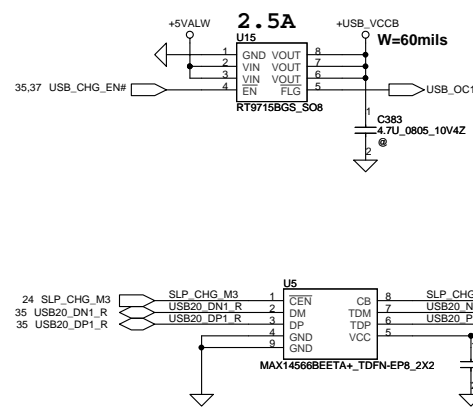


Slot 2 Half PCIe Mini Card- JET

Remove 3G/TV tuner

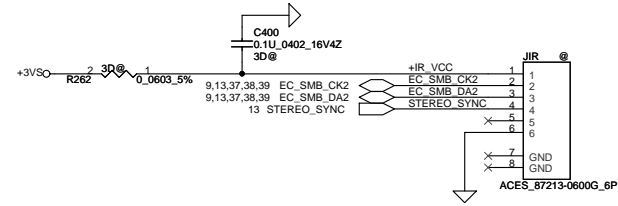


USB Sleep & Charge: Auto-Mode Mode3

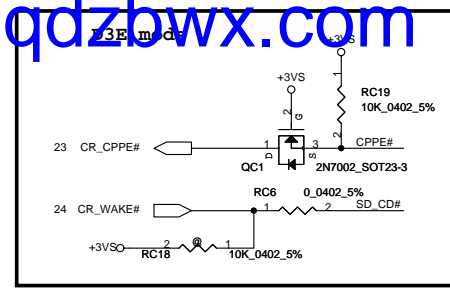
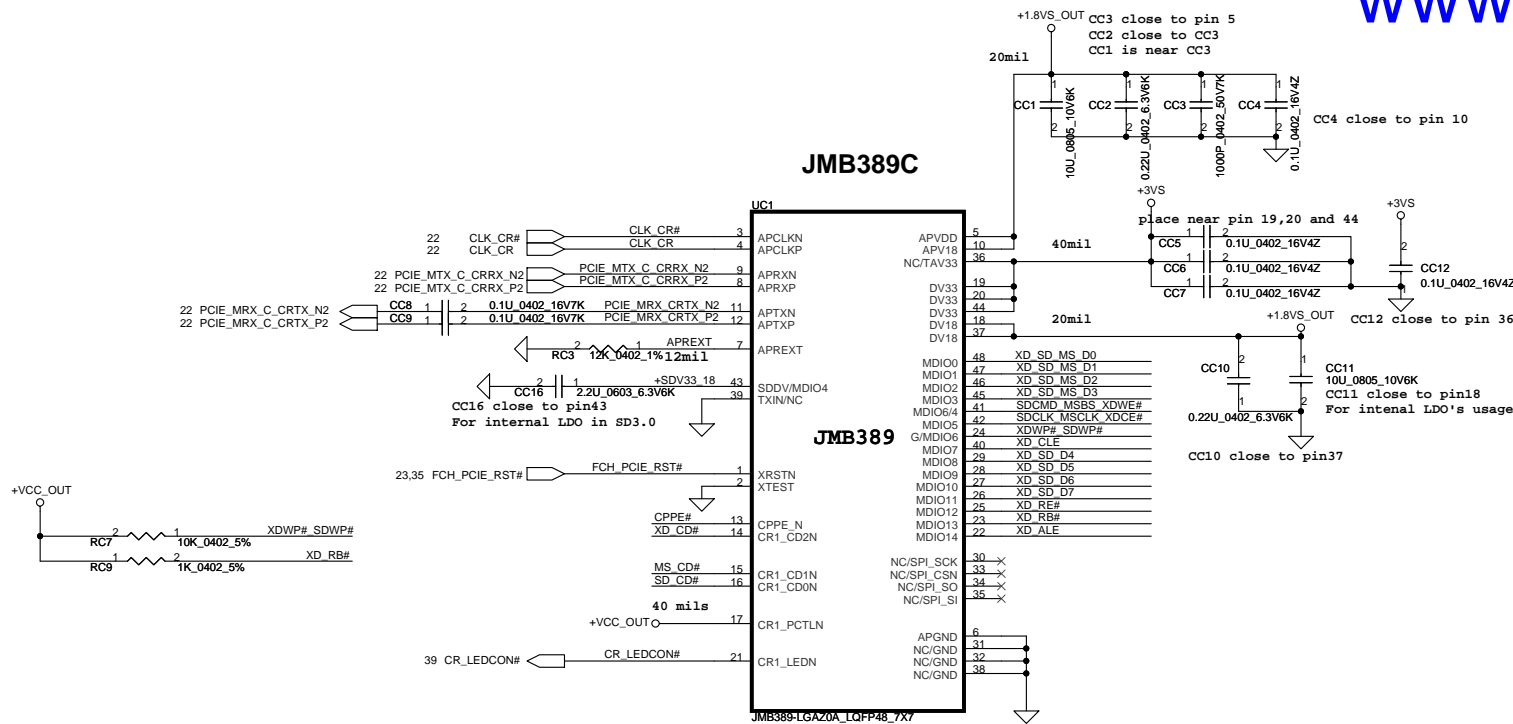


MAX14566B		
CB SLP_CHG#	CEN# SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	Force Dedicated charger mode (MODE3)
1	X	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

IR Emitter Connector

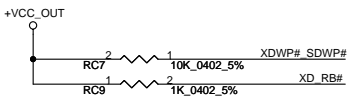


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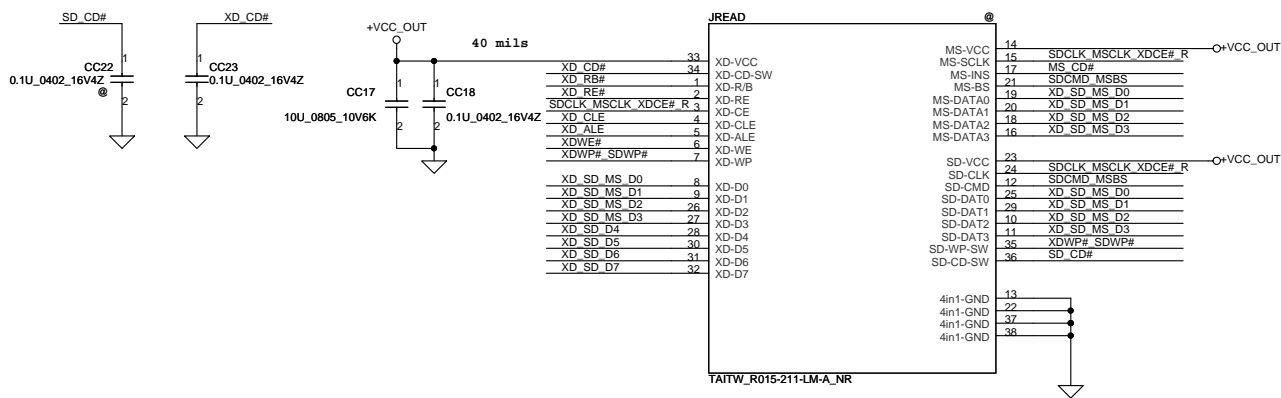


Power On Strapping setting

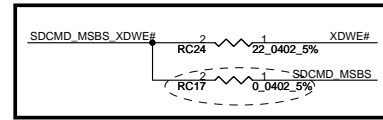
Pin name	Description	
	High	low
MDIO7	on-board	add-in card
MDIO14	CR_LEDCON# high active	CR_LEDCON# low active



5 in 1 Card Reader

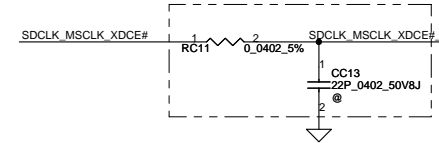


Add RC24 and RC17 close to UCI for xD issue



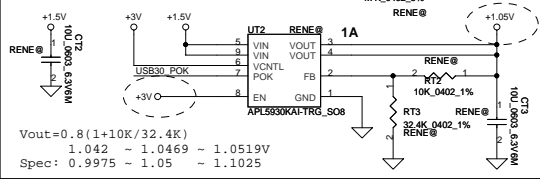
Change RC17 to 0 ohm for SDXC performance low issue

Reserved for EMI, close to UCI.42

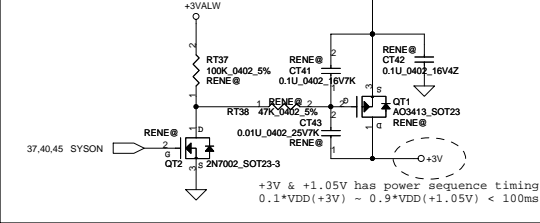


Change MDIO5 clock trace routing for SDHC issue

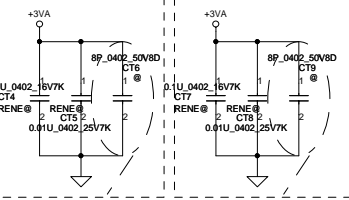
+1.5V to +1.05V Transfer



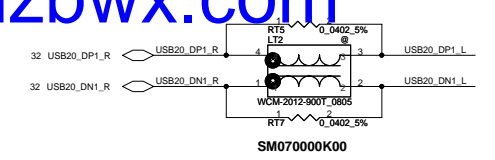
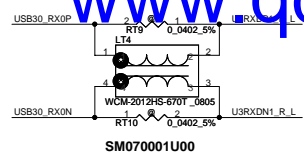
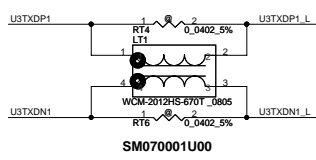
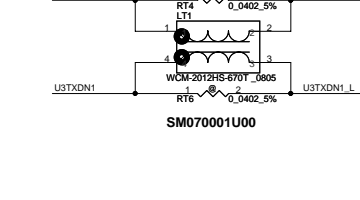
+3VALW to +3V Transfer



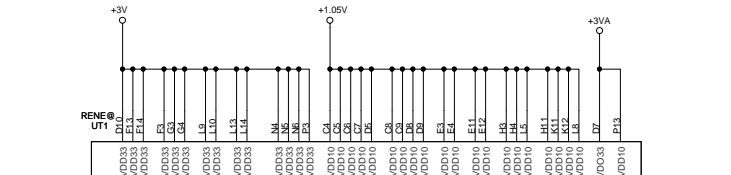
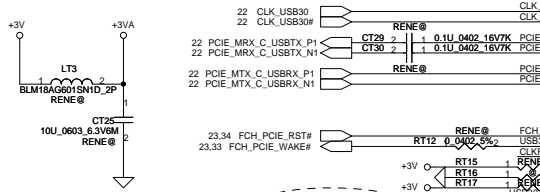
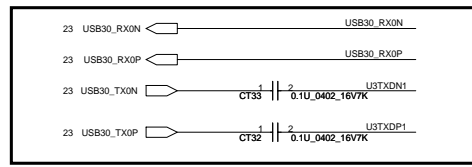
Close to U102.D7



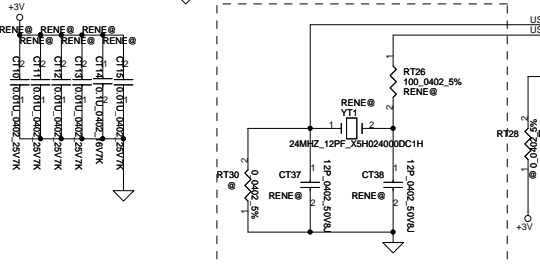
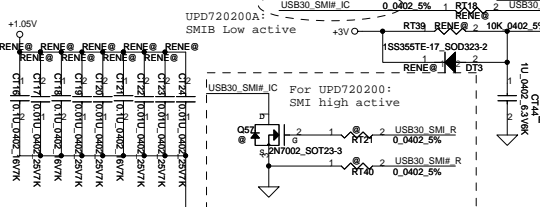
Close to U102.P13



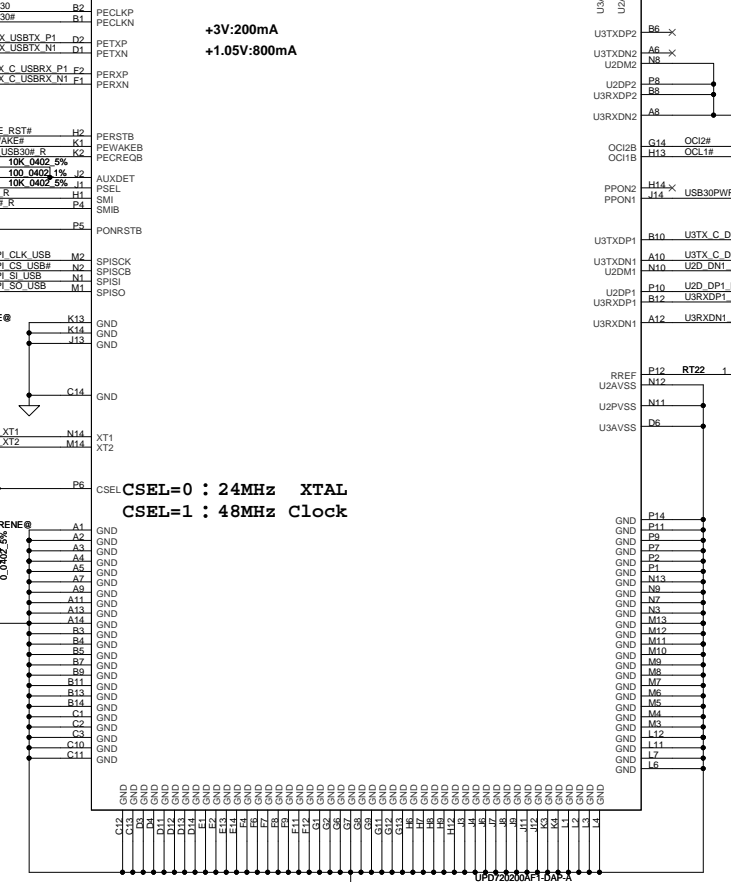
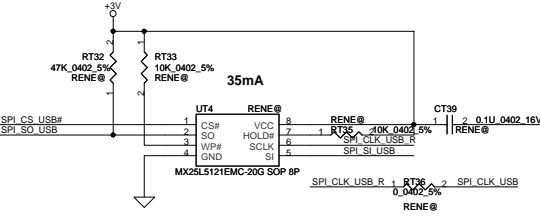
Co-Layout with Hudson M3 internal USB3.0 Place co-layout resistors close to UT1



+3V:200mA +1.05V:800mA

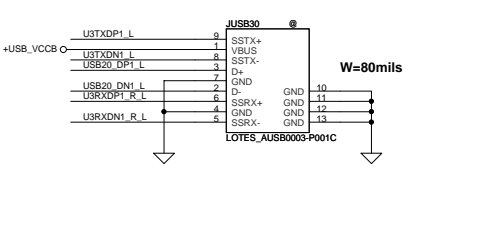
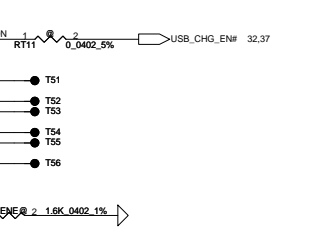
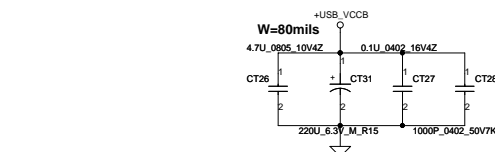
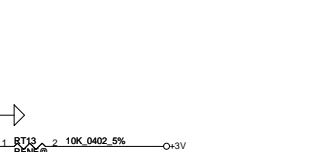


Place as close as possible to UT1.N14 and UT1.M14

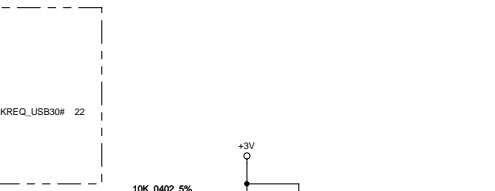
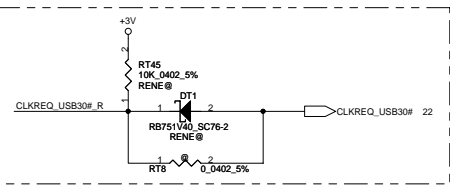


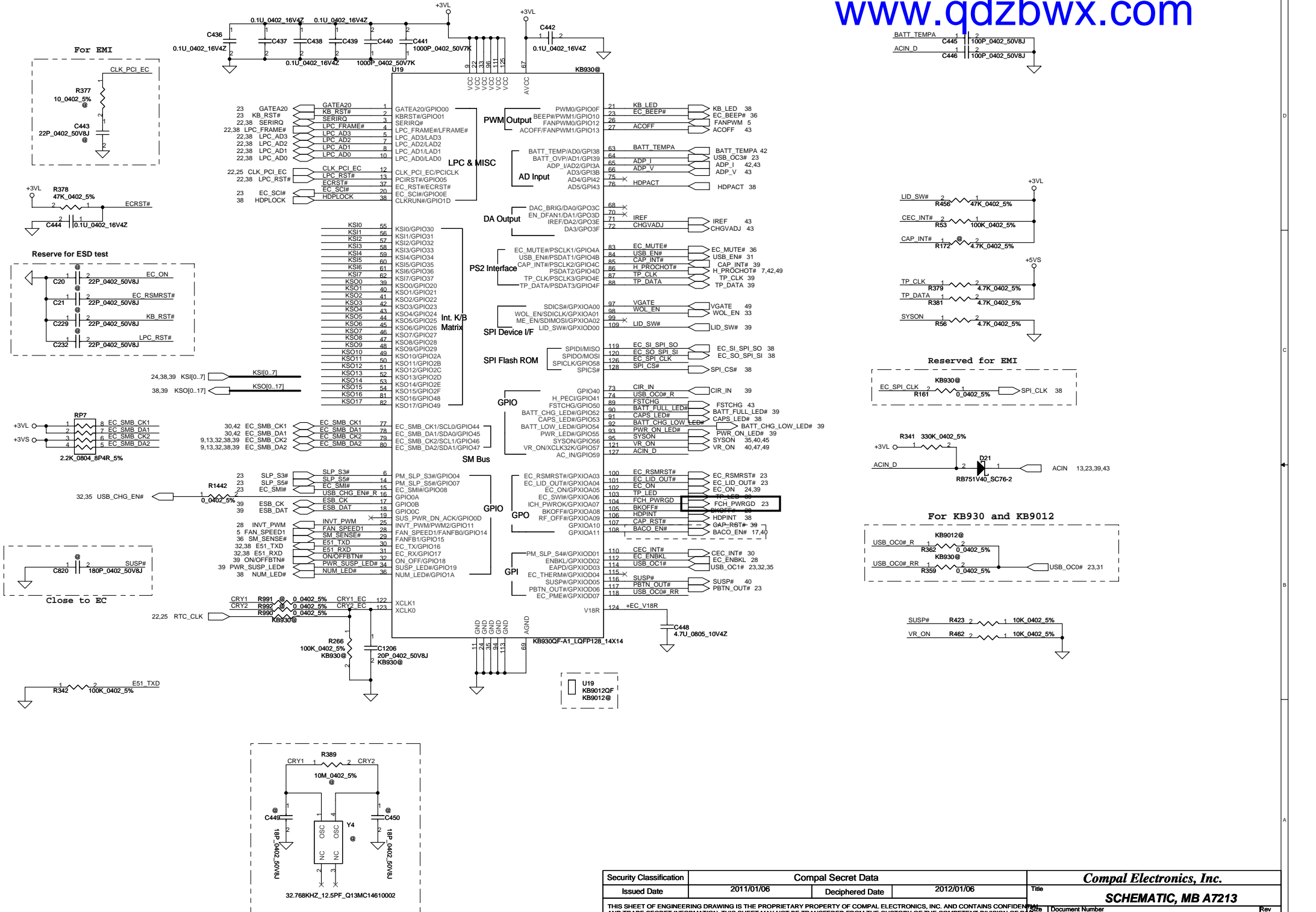
CSEL=CSEL=0 : 24MHz XTAL CSEL=1 : 48MHz Clock

Close to UT1.M2



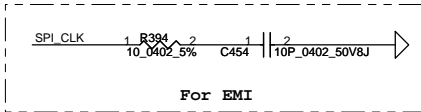
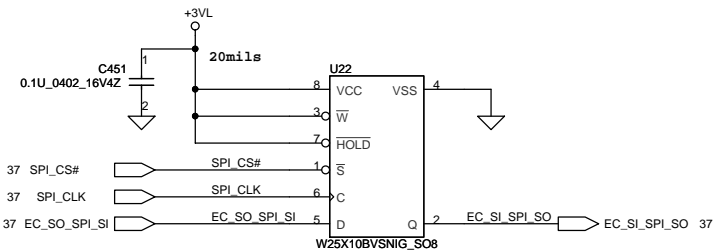
Change ESD Diode for EMI request





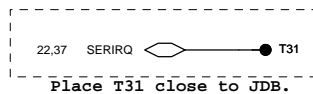
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SPI Flash (128KB)

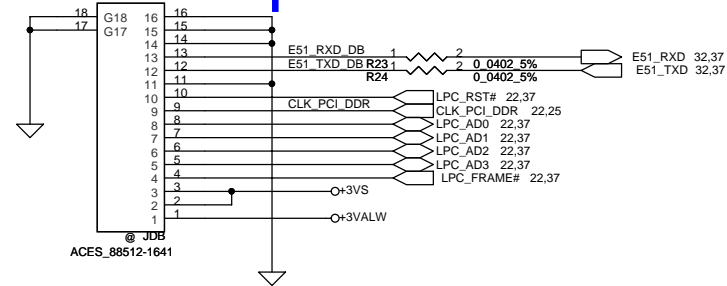


LPC Debug Port

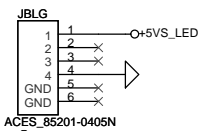
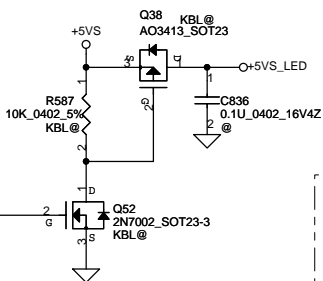
Place JDB under DDR DIMM.



www.qdzbwx.com



Keyboard LED

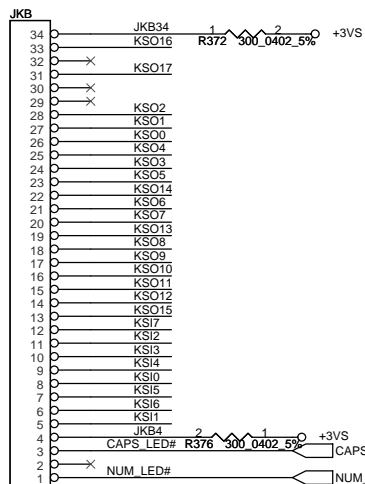


For EMI

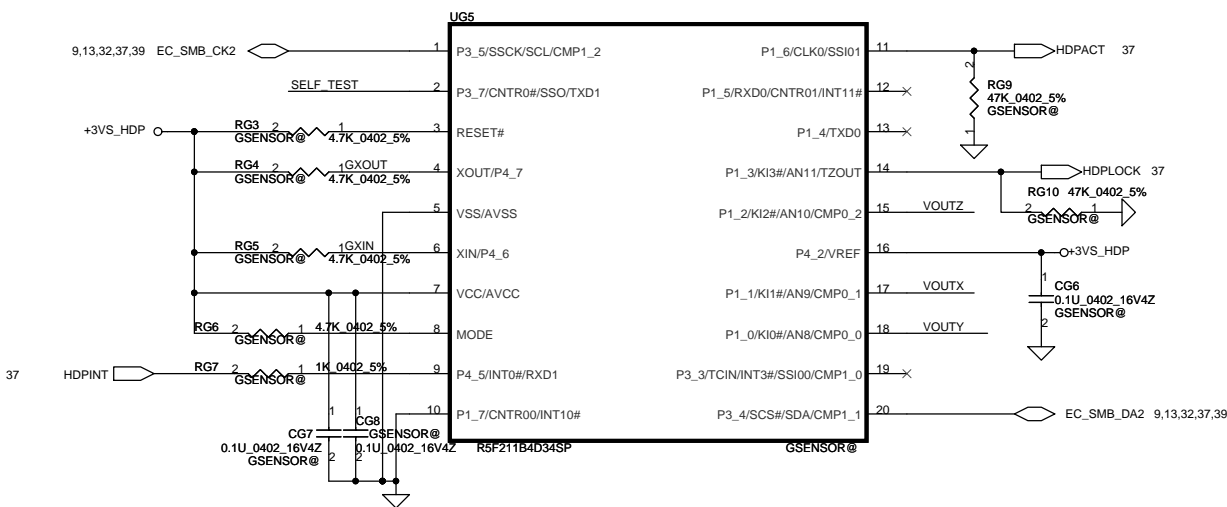
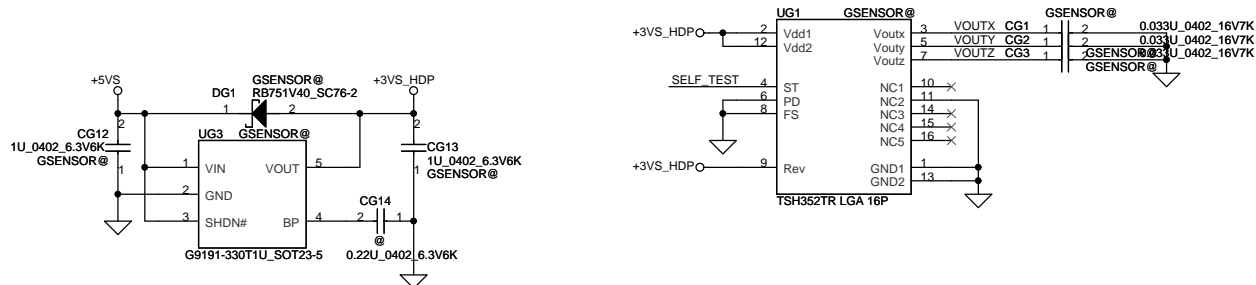
Close to JKB

KSO16	C401	100P_0402_50V8J
KSO17	1	100P_0402_50V8J
KSO2	C402	100P_0402_50V8J
KSO1	C404	100P_0402_50V8J
KSO0	C405	100P_0402_50V8J
KSO4	C406	100P_0402_50V8J
KSO3	C407	100P_0402_50V8J
KSO5	C408	100P_0402_50V8J
KSO14	C409	100P_0402_50V8J
KSO6	C410	100P_0402_50V8J
KSO7	C411	100P_0402_50V8J
KSO13	C412	100P_0402_50V8J
KSO8	C413	100P_0402_50V8J
KSO9	C415	100P_0402_50V8J
KSO10	C416	100P_0402_50V8J
KSO11	C417	100P_0402_50V8J
KSO12	C418	100P_0402_50V8J
KSO15	C419	100P_0402_50V8J
KSO15	C420	100P_0402_50V8J
KSI7	C421	100P_0402_50V8J
KSI2	C422	100P_0402_50V8J
KSI3	C423	100P_0402_50V8J
KSI4	C424	100P_0402_50V8J
KSI0	C425	100P_0402_50V8J
KSI5	C427	100P_0402_50V8J
KSI6	C429	100P_0402_50V8J
KSI1	C431	100P_0402_50V8J
CAPS_LED#	C433	100P_0402_50V8J
NUM_LED#	C435	100P_0402_50V8J

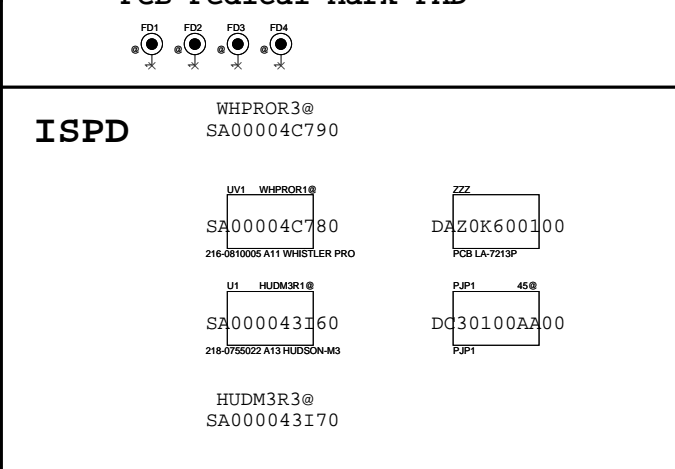
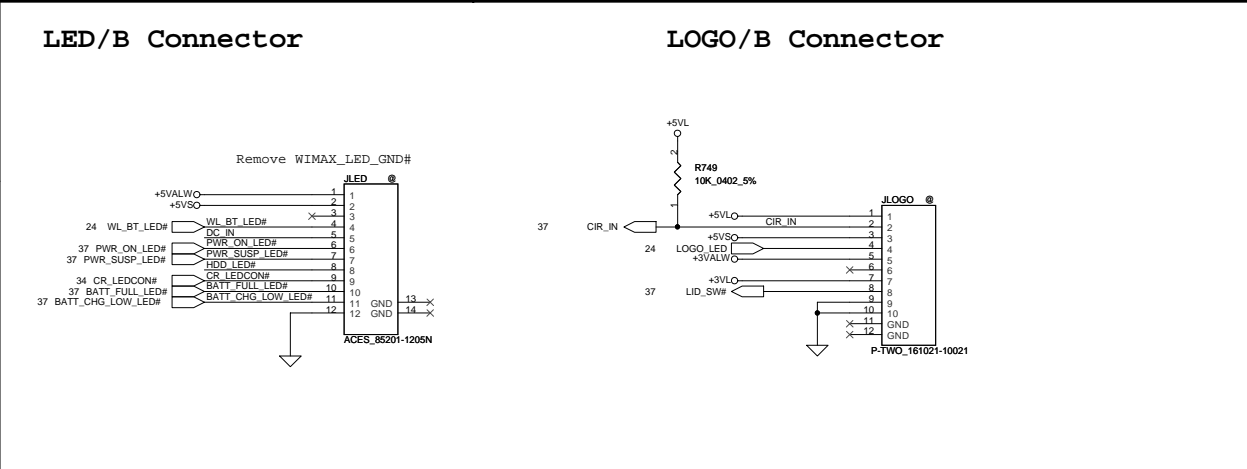
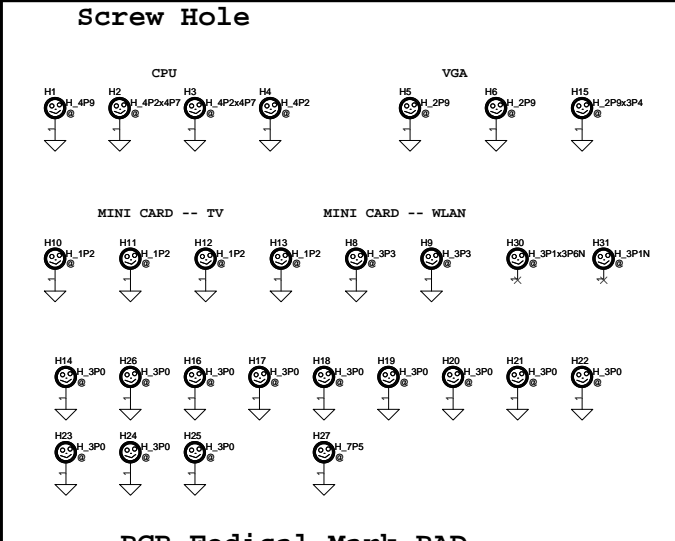
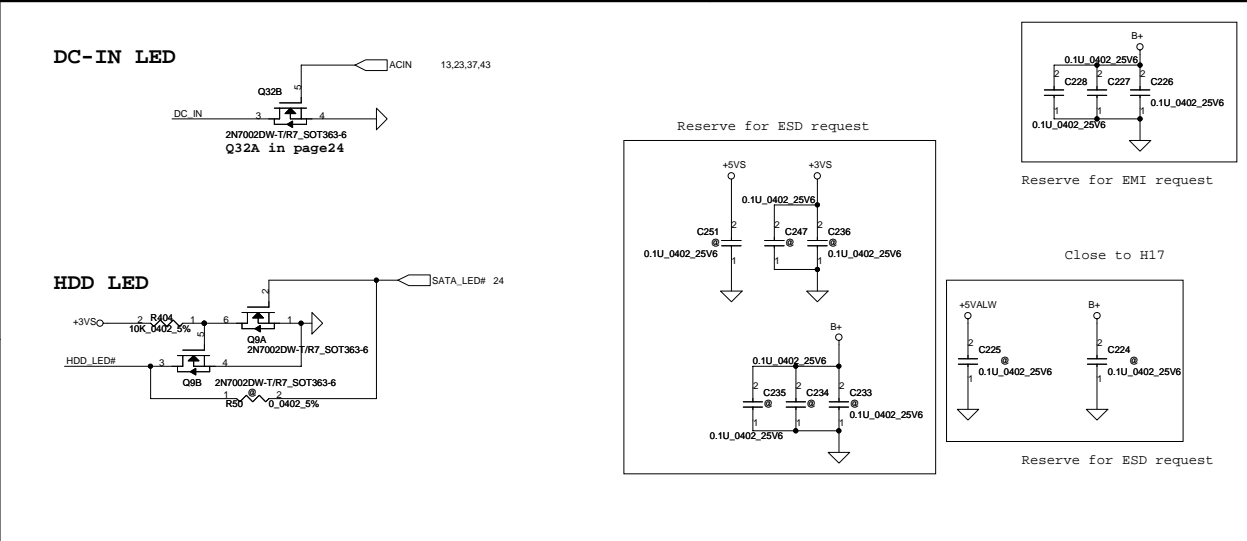
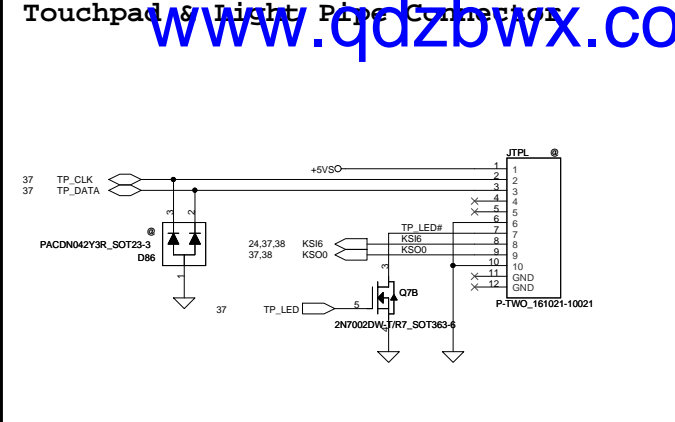
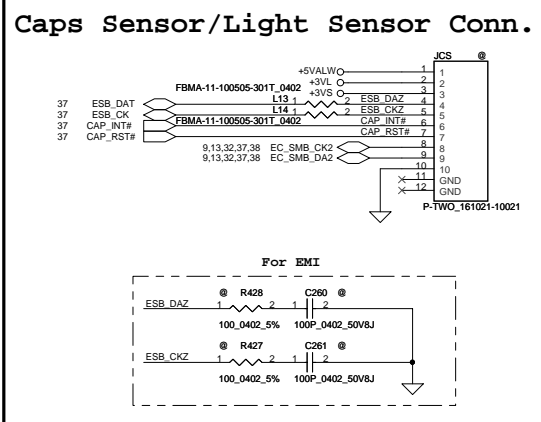
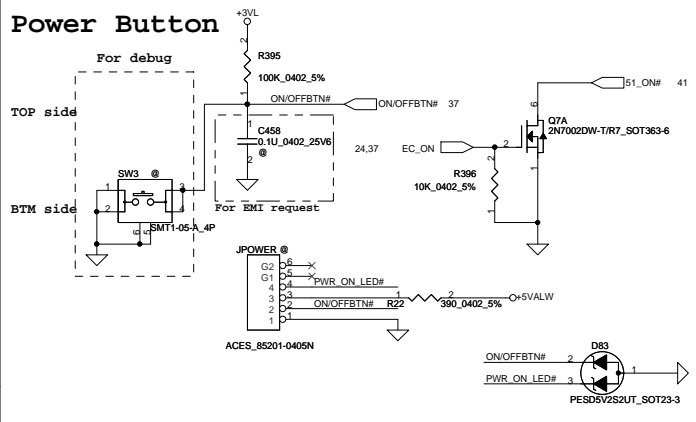
KEYBOARD CONN.



Place UG1 on TOP Layer

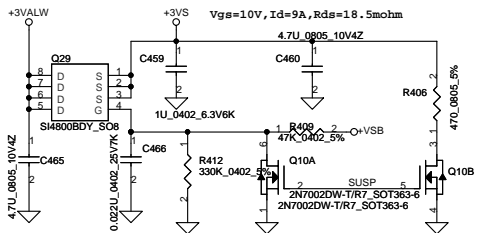


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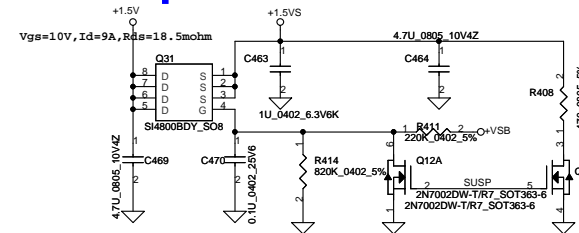
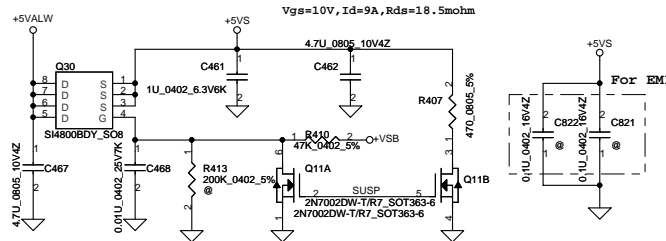


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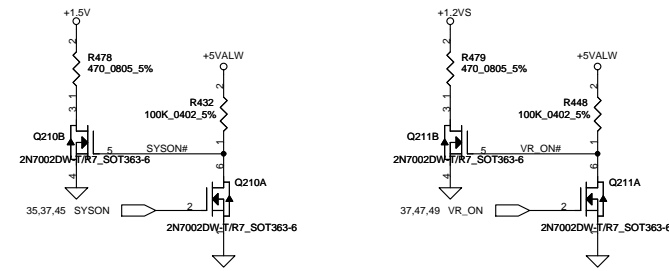
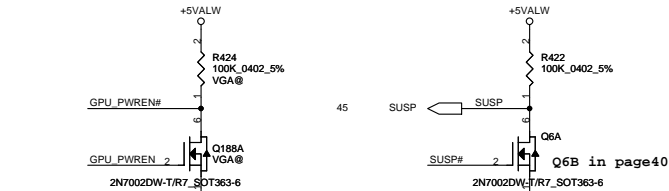
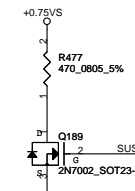
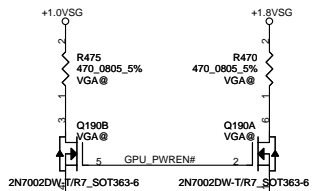
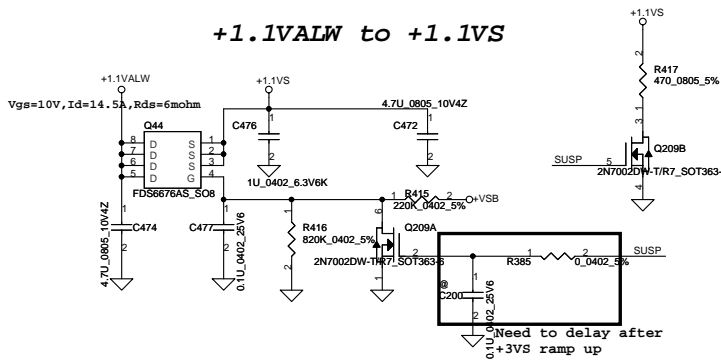
+3VALW TO +3VS



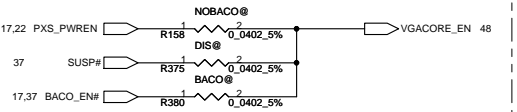
+5VALW TO +5VS



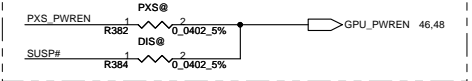
+1.1VALW to +1.1VS



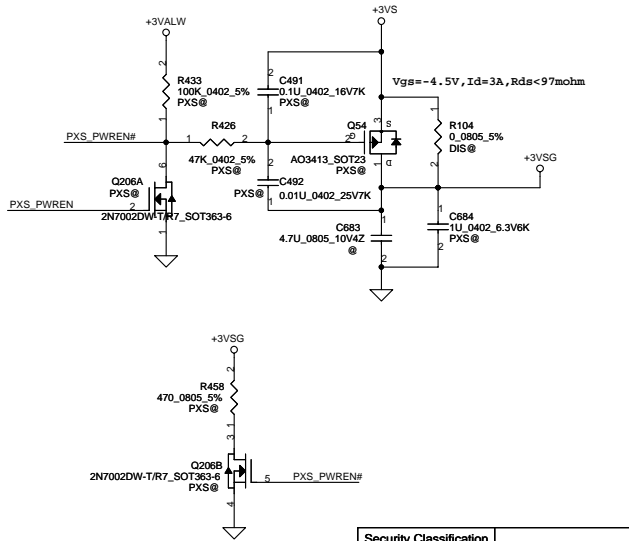
For +VGA_CORE power enable



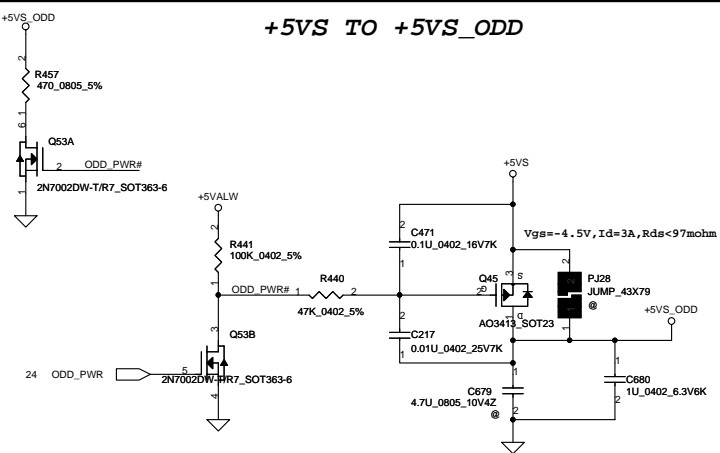
For GPU power enable



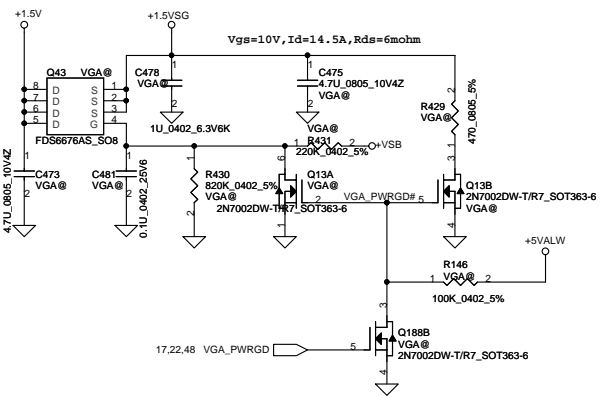
+3VS to +3VSG



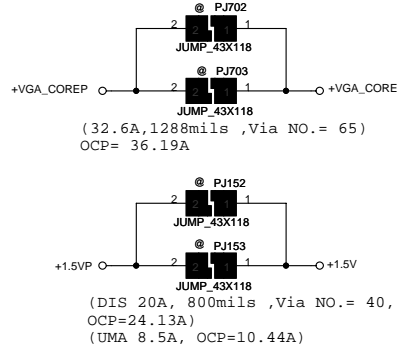
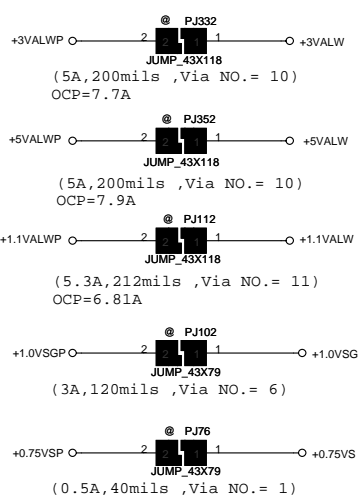
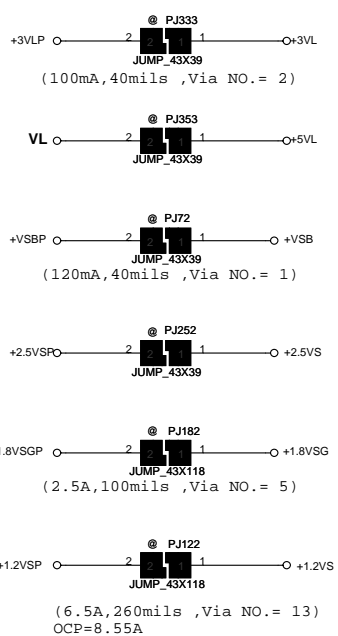
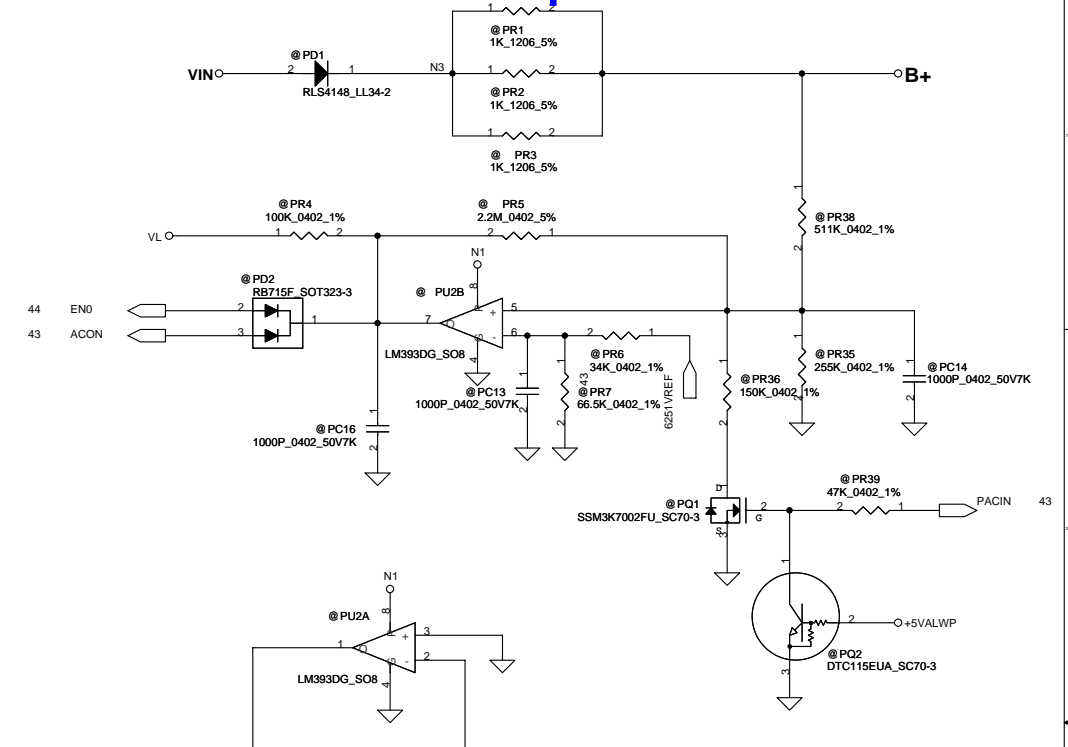
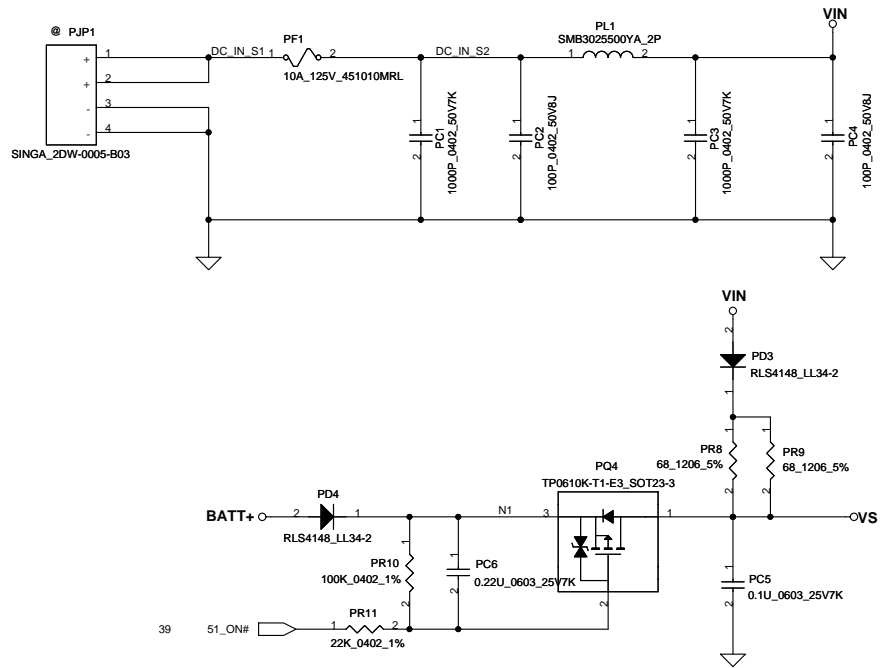
+5VS TO +5VS_ODD



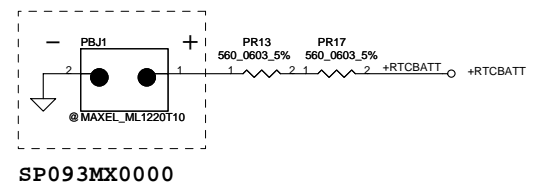
+1.5V to +1.5VSG



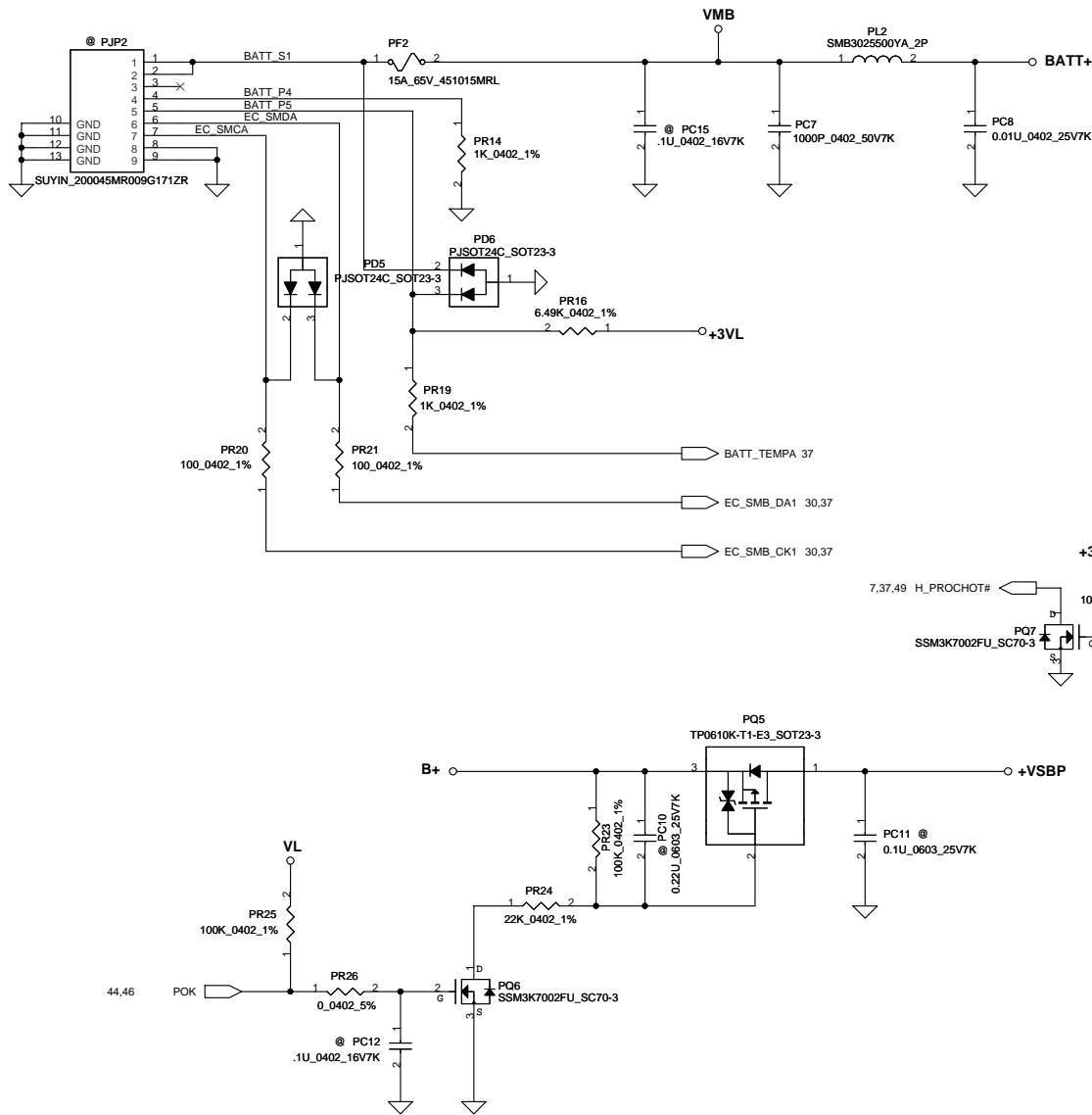
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RTC Battery



ACIN			
Precharge detector			
	Min.	typ.	Max
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

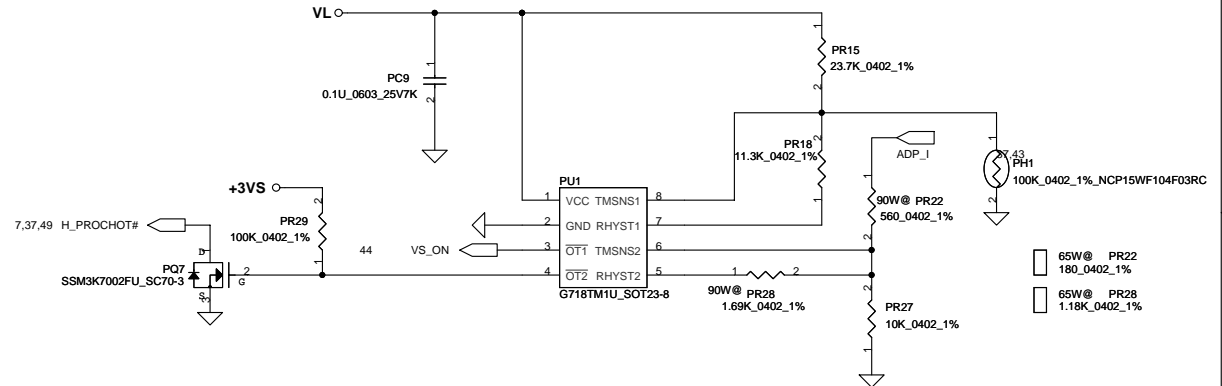


PH1 under CPU bottom side :
 CPU thermal protection at 90 degree C
 Recovery at 56 degree C

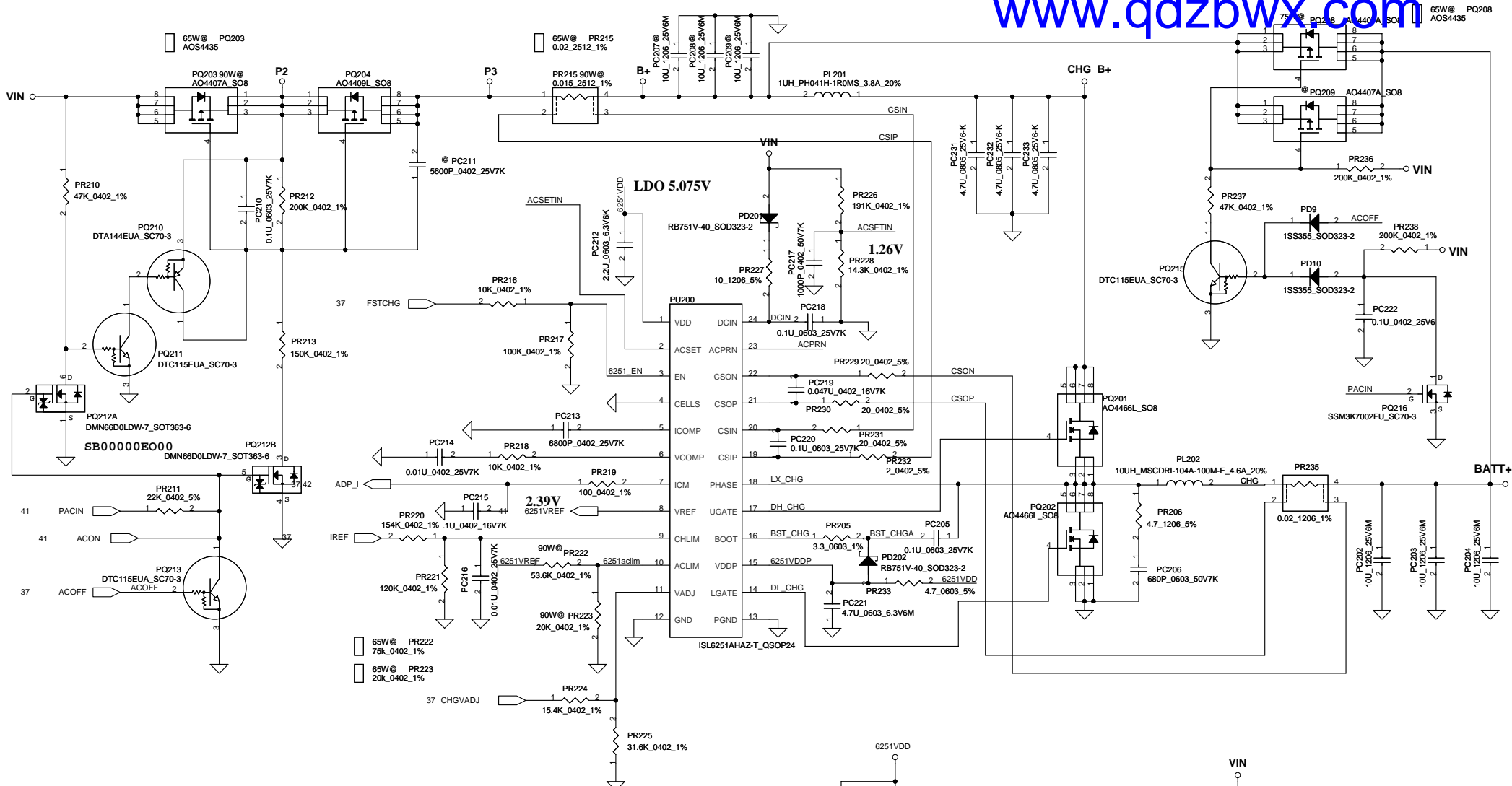
$$R_{set} = 3 * R_{tmh}$$

$$R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$$

Rtmh at 90C = 7.87K, Rtml at 56C = 26.1K
 Rset = 3 * 7.87K = 23.61K ==> 23.7K
 Rhyst = (23.7K * 26.1K) / (3 * 26.1K - 23.7K) = 11.33K ==> 11.3K



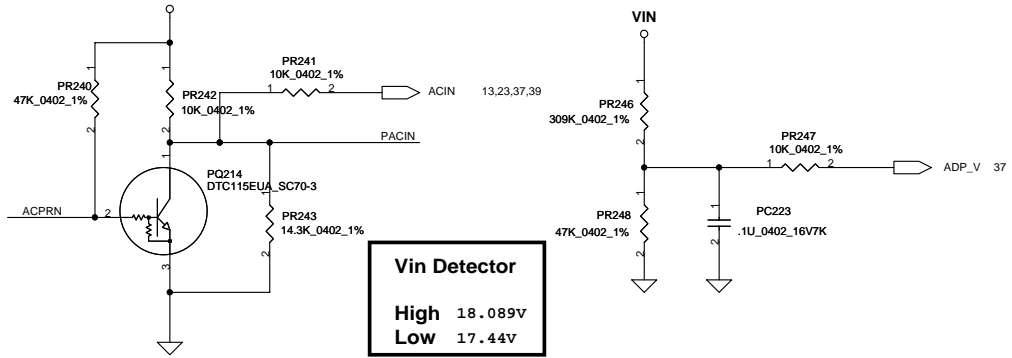
Adaptor protection				
Adaptor	Throttling point	ADP_I	Recovery point	ADP_I
90W	113.5W	1.783V	86.4W	1.357V
65W	71.8W	1.5V	62.44W	1.3V



CC=0.25A-3.6A
 IREF=0.9133*Icharge
 IREF=0.228V-3.288V
 VCHLIM need over 88mV

CHGVADJ=(Vcell-4)*9.445	
Vcell	CHGVADJ
4V	0V
4.2V	1.889V
4.35V	3.30575V

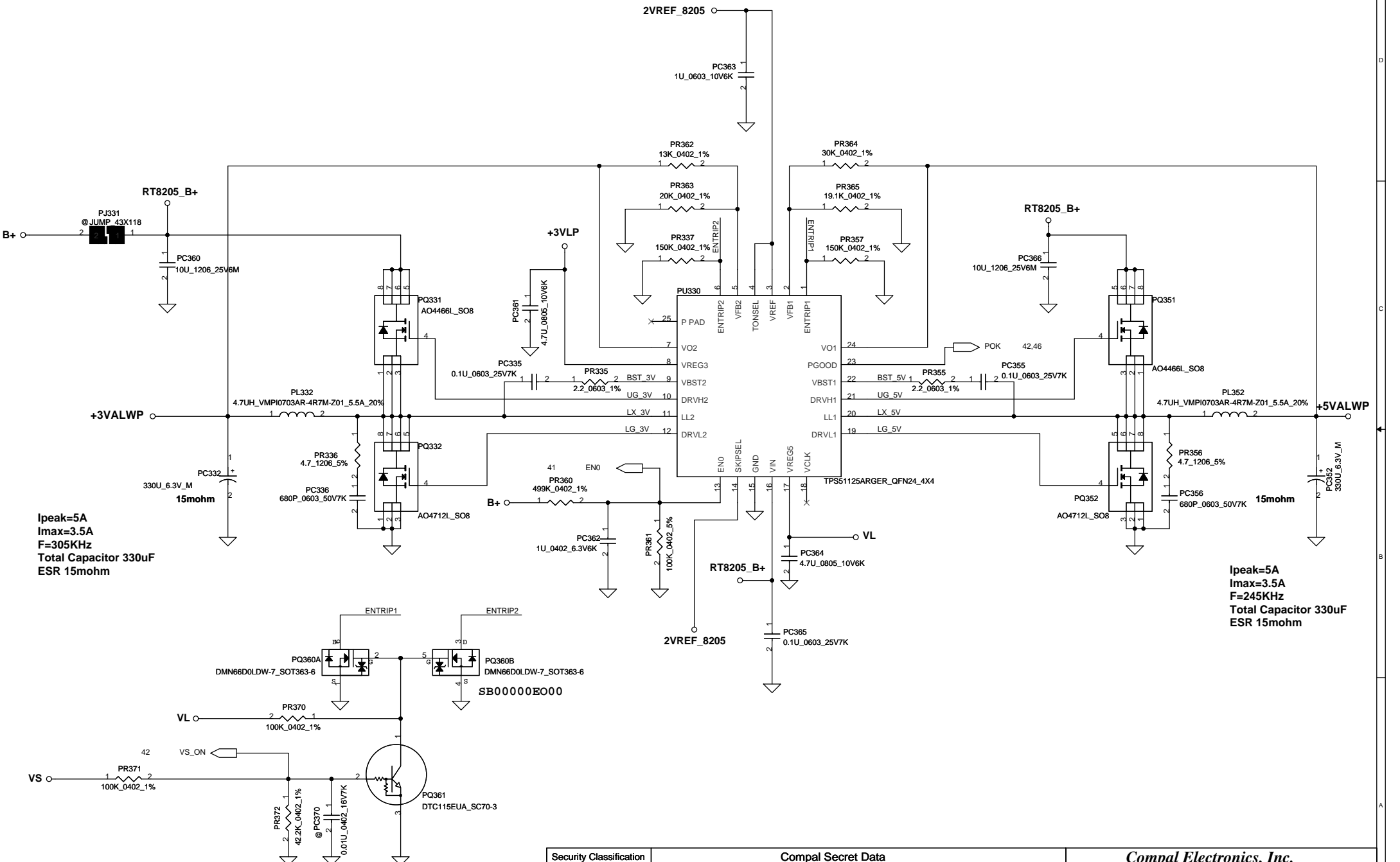
CP mode CP= 92%*Iada
 UMA
 Iada=0-3.421A (65W) CP=3.147A
 Vaclim=0.619V(65W) PR222=75k, PR223=20k, PR215=0.02
 DIS
 Iada=0-4.74A (90W) CP=4.36A
 Vaclim=0.735V(90W) PR222=53.6k, PR223=20k, PR215=0.015



Vin Detector
 High 18.089V
 Low 17.44V

$1.26 / 14.3 * 205.3 = 18.089V$

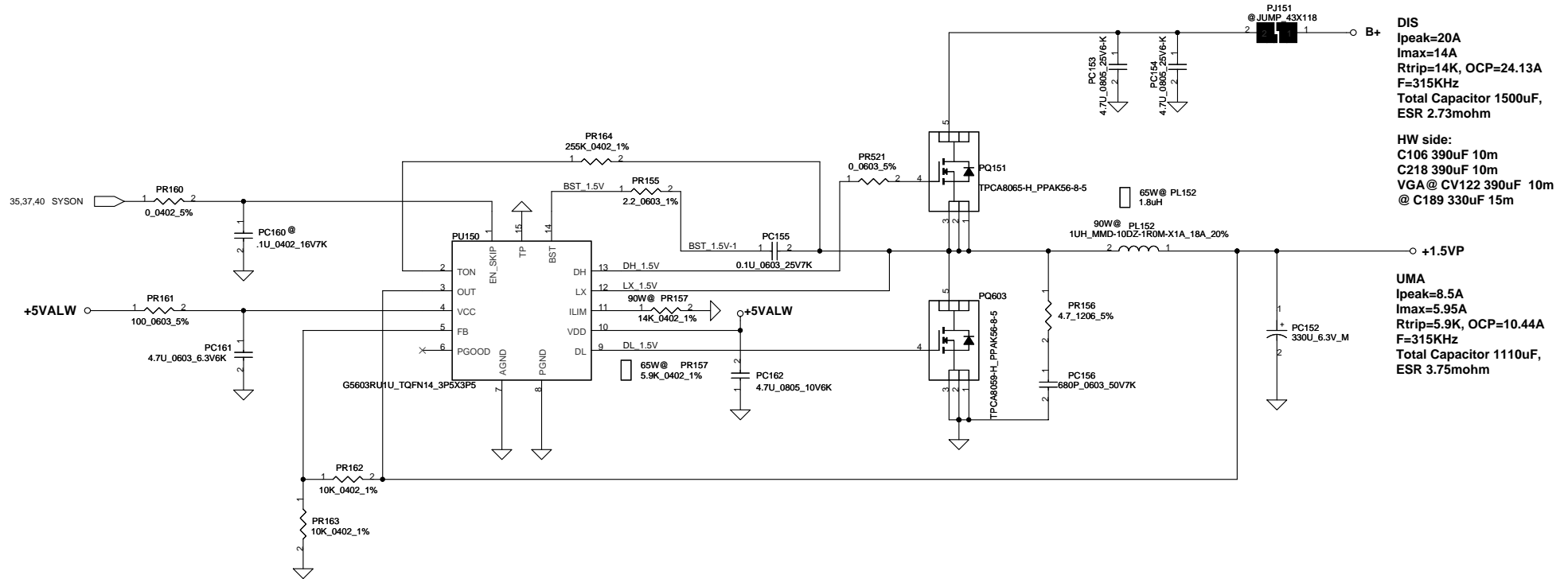
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Ipeak=5A
 Imax=3.5A
 F=305KHz
 Total Capacitor 330uF
 ESR 15mohm

Ipeak=5A
 Imax=3.5A
 F=245KHz
 Total Capacitor 330uF
 ESR 15mohm

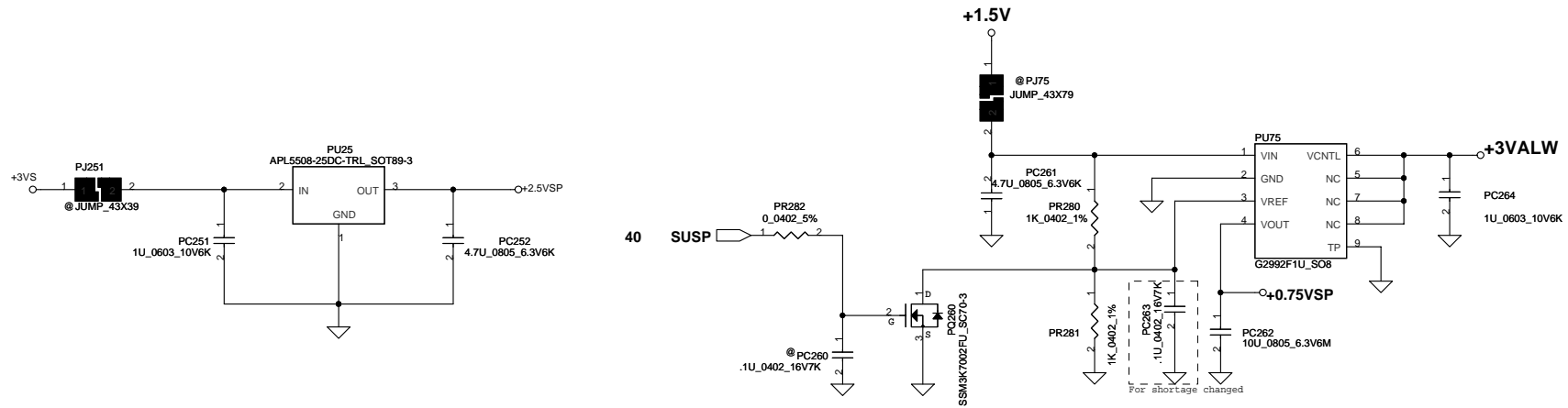
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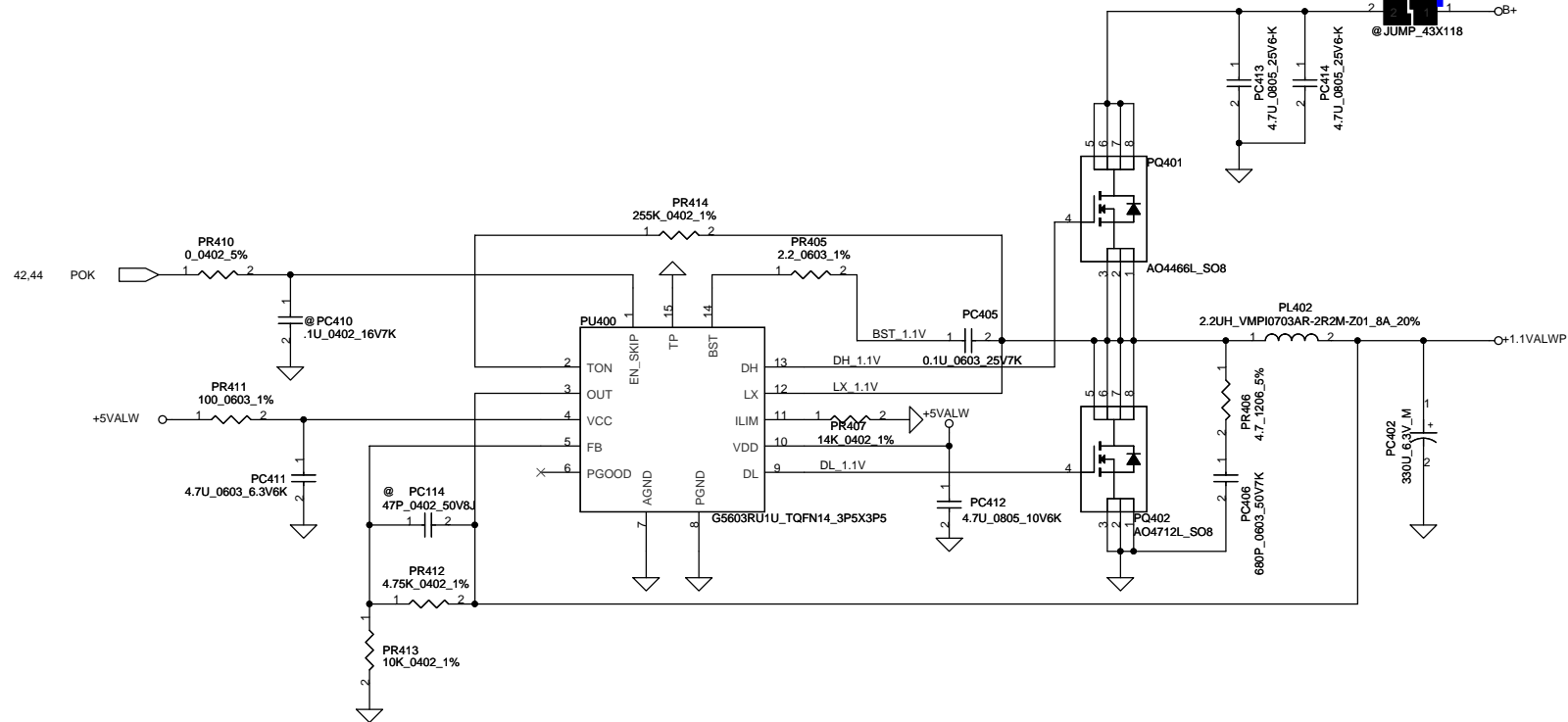
DIS
 $I_{peak}=20A$
 $I_{max}=14A$
 $R_{trip}=14K$, $OCP=24.13A$
 $F=315KHz$
 Total Capacitor 1500uF,
 ESR 2.73mohm

HW side:
 $C106$ 390uF 10m
 $C218$ 390uF 10m
 $VGA@ CV122$ 390uF 10m
 $C189$ 330uF 15m

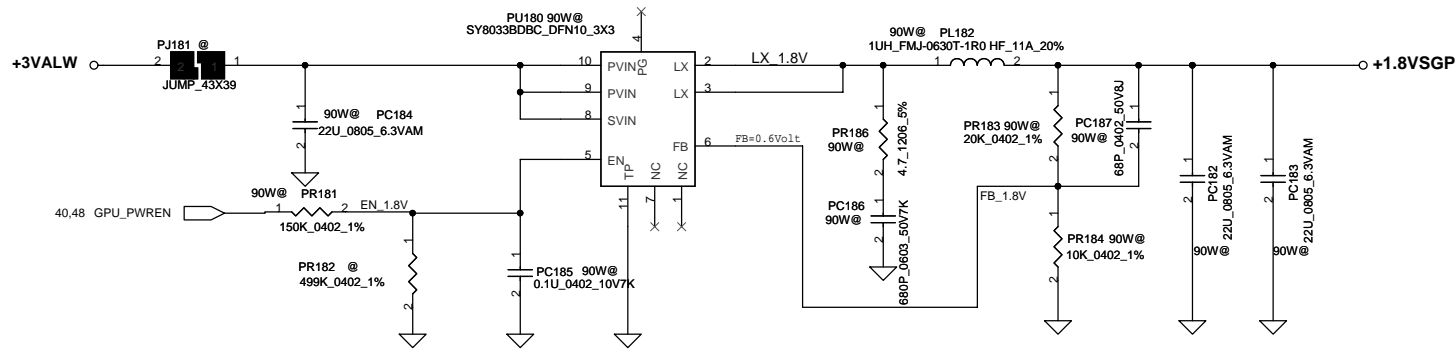
UMA
 $I_{peak}=8.5A$
 $I_{max}=5.95A$
 $R_{trip}=5.9K$, $OCP=10.44A$
 $F=315KHz$
 Total Capacitor 1110uF,
 ESR 3.75mohm



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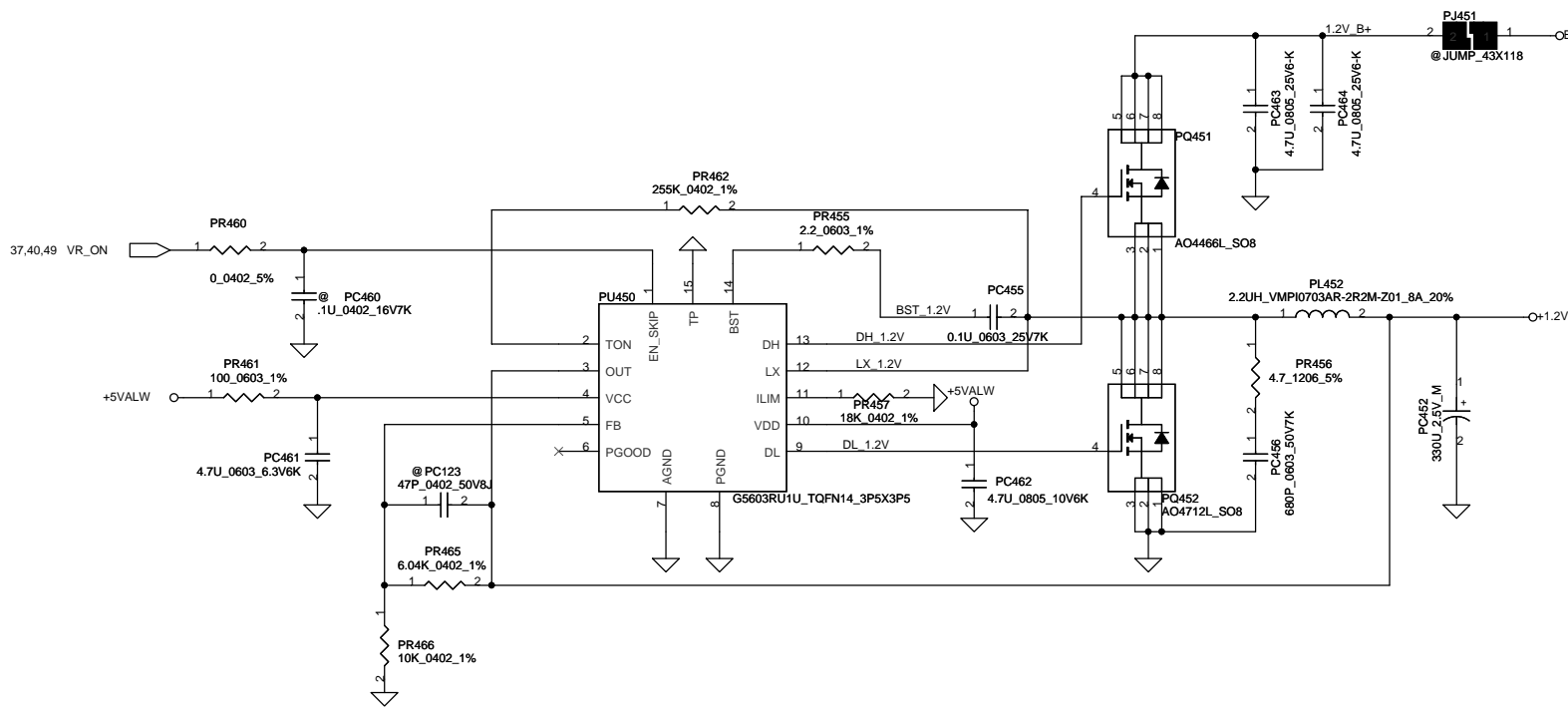


Ipeak=5.3A
 I_{max}=3.71A
 R_{trip}=14K, OCP=6.64A
 F=315KHz
 Total Capacitor 330uF,
 ESR 15mohm



Ipeak=2.5A
 ILIM = 4A
 F=1MHz
 Total Capacitor 44uF,

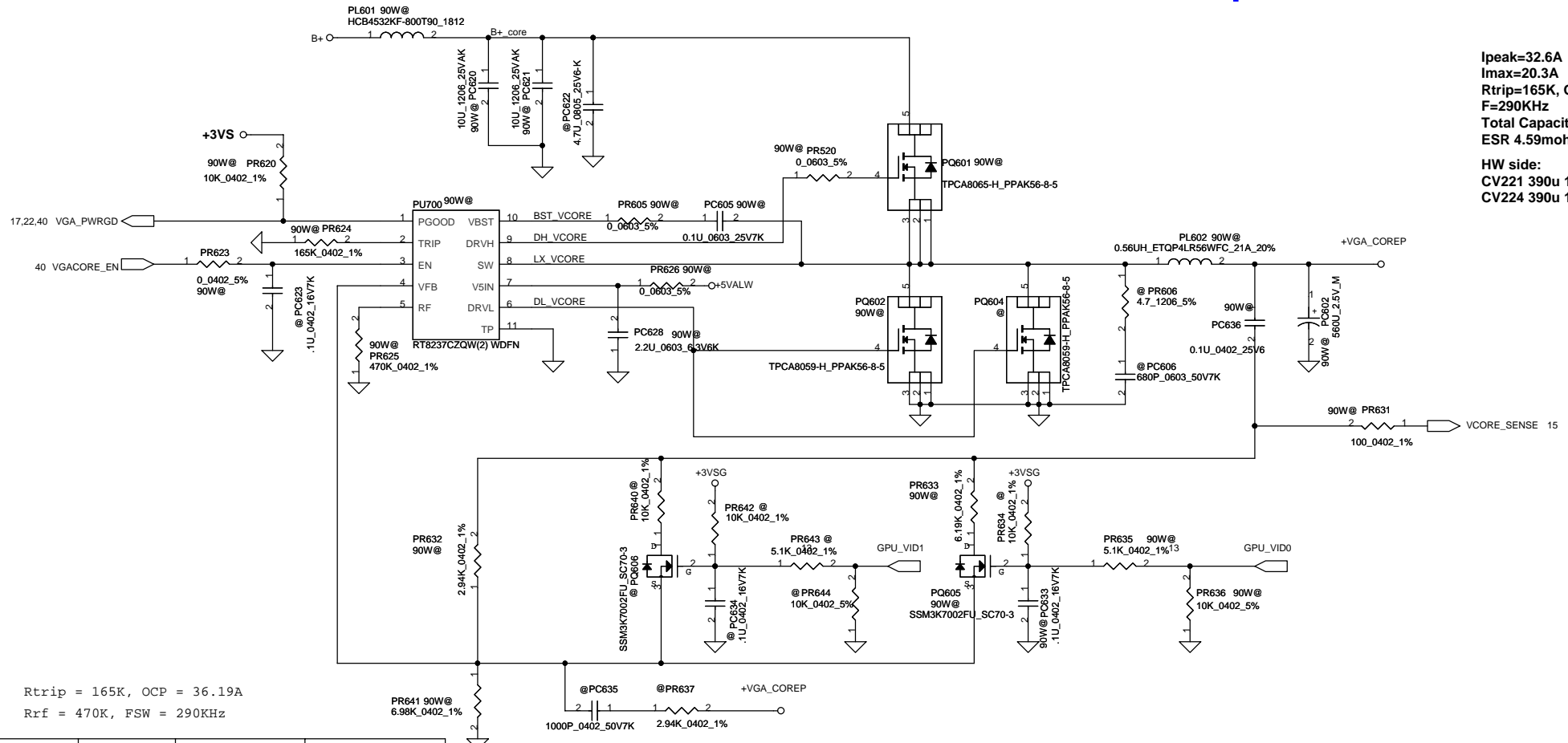
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I_{peak}=6.5A
I_{max}=4.55A
R_{trip}=18K, OCP=8.37A
F=315KHz
Total Capacitor 720uF,
ESR 6mohm
HW side:
C130 390uF 10m

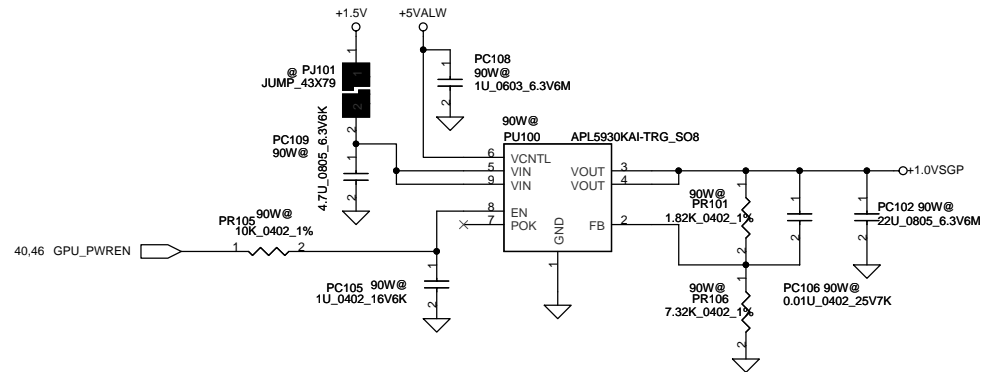
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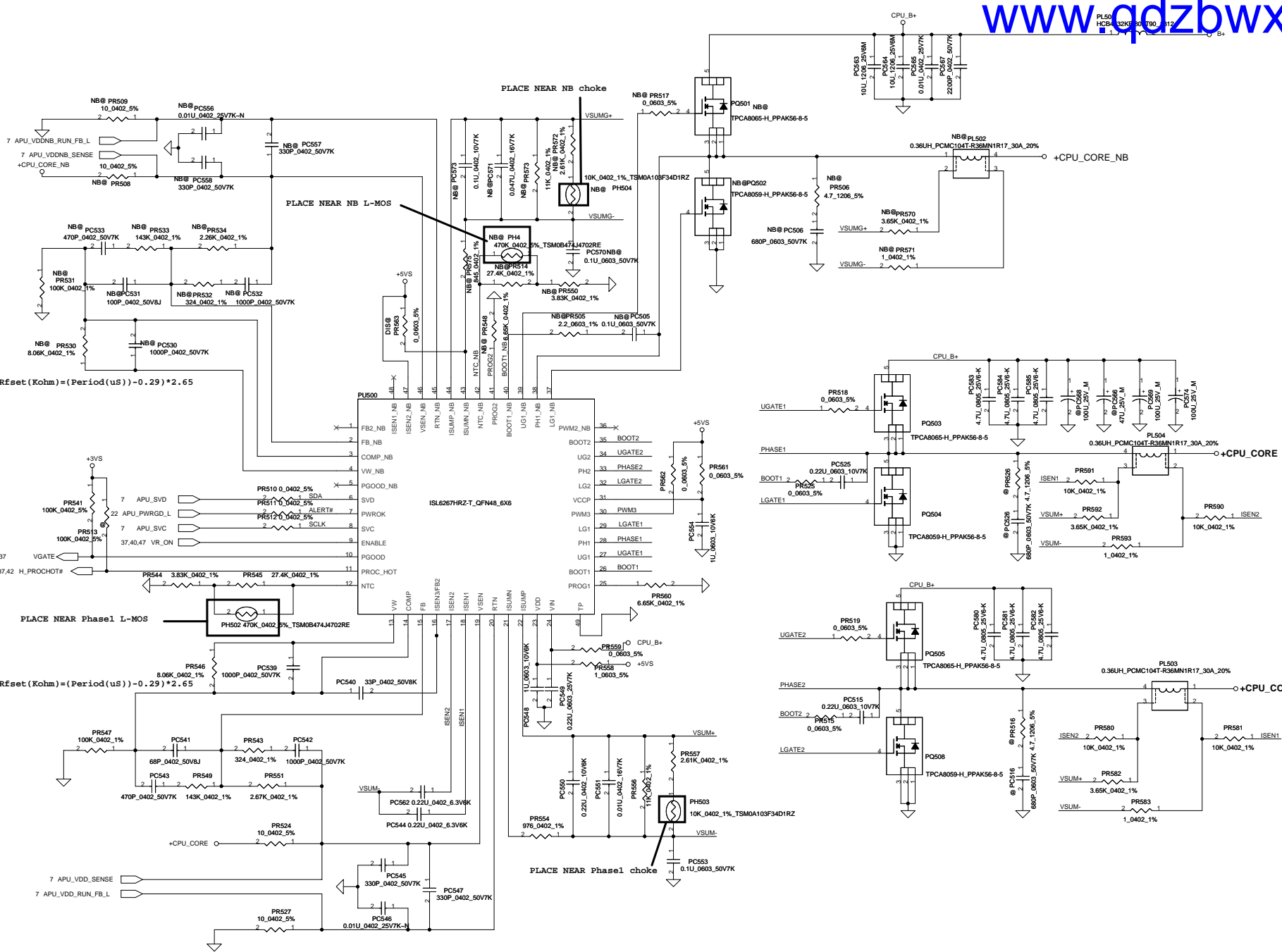
Ipeak=32.6A
 I_{max}=20.3A
 R_{trip}=165K, OCP=36.19A
 F=290KHz
 Total Capacitor 1220uF,
 ESR 4.59mohm
 HW side:
 CV221 390u 17m
 CV224 390u 17m



R_{trip} = 165K, OCP = 36.19A
 R_{rf} = 470K, FSW = 290KHz

GPU VID1	GPU VID0	Capilano LP	Whistler Pro
X	L	1	1
X	H	0.9	0.9
H	L		
H	H		





Ipeak=27.5A
 Imax=15.75A
 Ri=845, Rdroop=976, OCP=34.92A
 F=300KHz
 Total Capacitor 660uF,
 ESR 8.5mohm
 HW side:
 C160 330u 17m
 C201 330u 17m
 @C163 330u 9m

Rfset (Kohm) = (Period(us)) - 0.29 * 2.65

Rfset (Kohm) = (Period(us)) - 0.29 * 2.65

If the layout of each phase to CPU is symmetric, the two res. can be removed. They are used for phase current balance adjustment.

Ipeak=54A
 Imax=36A
 Ri=976, Rdroop=2.67K, OCP=65.21A
 F=300KHz
 Total Capacitor 1320uF,
 ESR 2.25mohm

HW side:
 C145 330u 9m
 C146 330u 9m
 C147 330u 9m
 C148 330u 9m

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
2011/03/30		42	Change PR22 to 180Ω,PR28 to 1.18KΩ Change PR22 to 523Ω,PR28 to 3KΩ	For 65W SKU For 90W SKU
		43	Change PC217 to SE074102K80,PR236 to 200KΩ,PR237 to 47KΩ PR205 to 3.3Ω,PR235 to SD00000S120,Add PR206,PC206, Delete PC211 Change PR222 to 53.6KΩ,PR223 to 20KΩ,Delate PQ209 Change PR222 to 75KΩ	Circuit modify For 90W SKU For 65W SKU
		44	Change PR335,PR355 to 2.2Ω,PC332,PC352 to SF000002080 ,PL332,PL352 to SH00000KN00,Add PR336,PR356,PC336,PC356	Circuit modify
		45	Change PR155 to 2.2Ω,PC152 to SF000002080, Add PR156,PC156,PR521,Delete PC260 Change PR157 to 5.9KΩ,PL152 to SH00000IP00 Change PR157 to 14KΩ,PL152 to SH00000CN00	Circuit modify For 90W SKU For 65W SKU
		46	Change PR405 to 2.2Ω,PC402 to SF000002080,Add PR406,PC406 Change PR407 to 14KΩ,PL402 to 2.2UH 7*7	Circuit modify
		47	Change PR455 to 2.2Ω,PR457 to 18KΩ,PL452 to 2.2UH 7*7 Add PR456,PC456	Circuit modify
		48	Change PR624 to 165KΩ,PR631 to 100Ω,Delete PR630, Add PC636,PR520	Circuit modify
		49	Change PR505 to 2.2Ω,PR560 to 6.65KΩ,PR551 to 2.67KΩ Change PH503,PH504 to SL200000W00,PC569,PC574 to SF000003W00 Add PC506,PR506,PR517,PR518,PR519	Circuit modify

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HW PIR (Product Improve Record)

QHRAE LA-7213P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

Item	Date	Page	Solution	Request
1.	3/17	P23	Remove level-shifter for ODD_PLUGIN#	ODD has internal 1K pull-down
2.	3/17	P34	Add level-shifter for CR_CPPE#	For leakage issue
3.	3/17	P23	Change HDMI_HPD to GEVENT10# and reserve GEVENT19#	GEVENT9# has issue
4.	3/17	P24	Change LOGO_LED to GPIO176 and WL_BT_LED to GPIO177	For LED flash issue after power-on
5.	3/24	P10	Add C295,C316,C324,C325	For EMI test
6.	3/28	P39	Reserve C20,C21,C229,C231~C236,C247,C251	For ESD test)
7.	3/29	P38	Change LPC debug port to 16pins connector	To support new debug card
8.	3/30	P07	Add R70,R102,R105	Pull-down for unused HPD port

REVISION CHANGE: 0.2 TO 1.0

Item	Date	Page	Solution	Request
1.	4/15	P31	Reserve D24, D25	
2.	4/27	P22	Change R257 form 100k to 10k for leakage issue.	
3.	4/27	P37	Add BACO_EN# to EC	To inform EC GPU thermal sensor status

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