

Compal Confidential

Model Name : QILE1 & QILE2
File Name : LA-8131P, LA-8133P
BOM P/N:

QILE1:
4319GG39L01 : SMT MB A8131 QILE1 DIS-N13P
4319GG39L02 : SMT MB A8131 QILE1 DIS GPU-N13M
4319GG39L03 : SMT MB A8131 QILE1 UMA

QILE2:
4319GJ39L01 : SMT MB A8133 QILE2 DIS-N13P
4319GJ39L02 : SMT MB A8133 QILE2 DIS GPU-N13M
4319GJ39L03 : SMT MB A8133 QILE2 UMA

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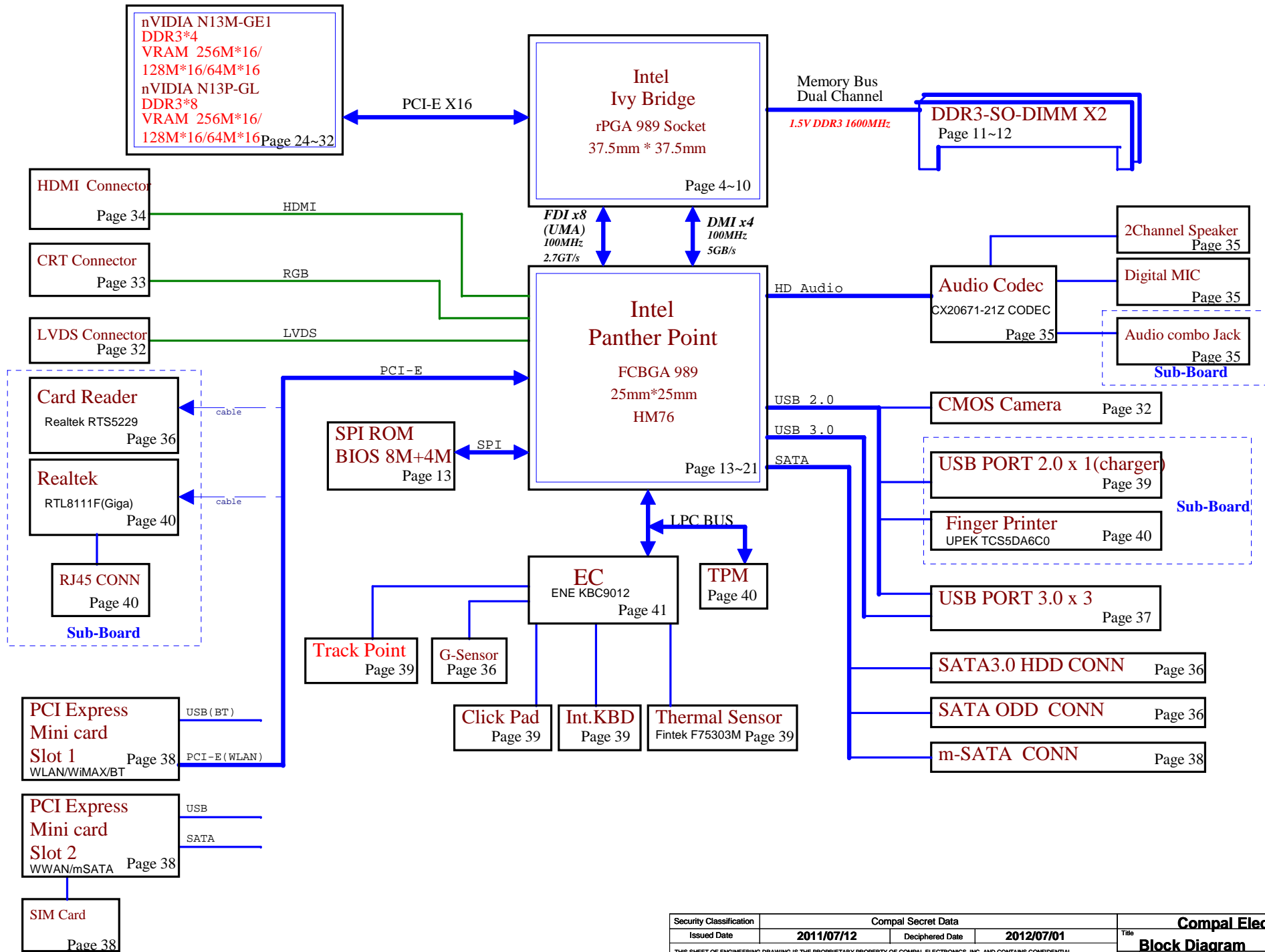
M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH
GPU nVIDIA N13M-GE1 / N13P-GL

2012-01-11

REV:1.0

Security Classification	Compal Secret Data		Title	
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Voltage Rails

power plane	State	+B	+5VALW	+3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS	+3VM +1.05VM
S0		○	○	○	○	○	○ M3 Supported
S3		○	○	○	○	✗	○ M3 Supported
S5 S4/AC		○	○	✗	✗	✗	○ M3 Supported
S5 S4/ Battery only		✗	✗	✗	✗	✗	
S5 S4/AC & Battery don't exist		✗	✗	✗	✗	✗	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	0.6
6	
7	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor Fintek F75303M	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

USB Port Table

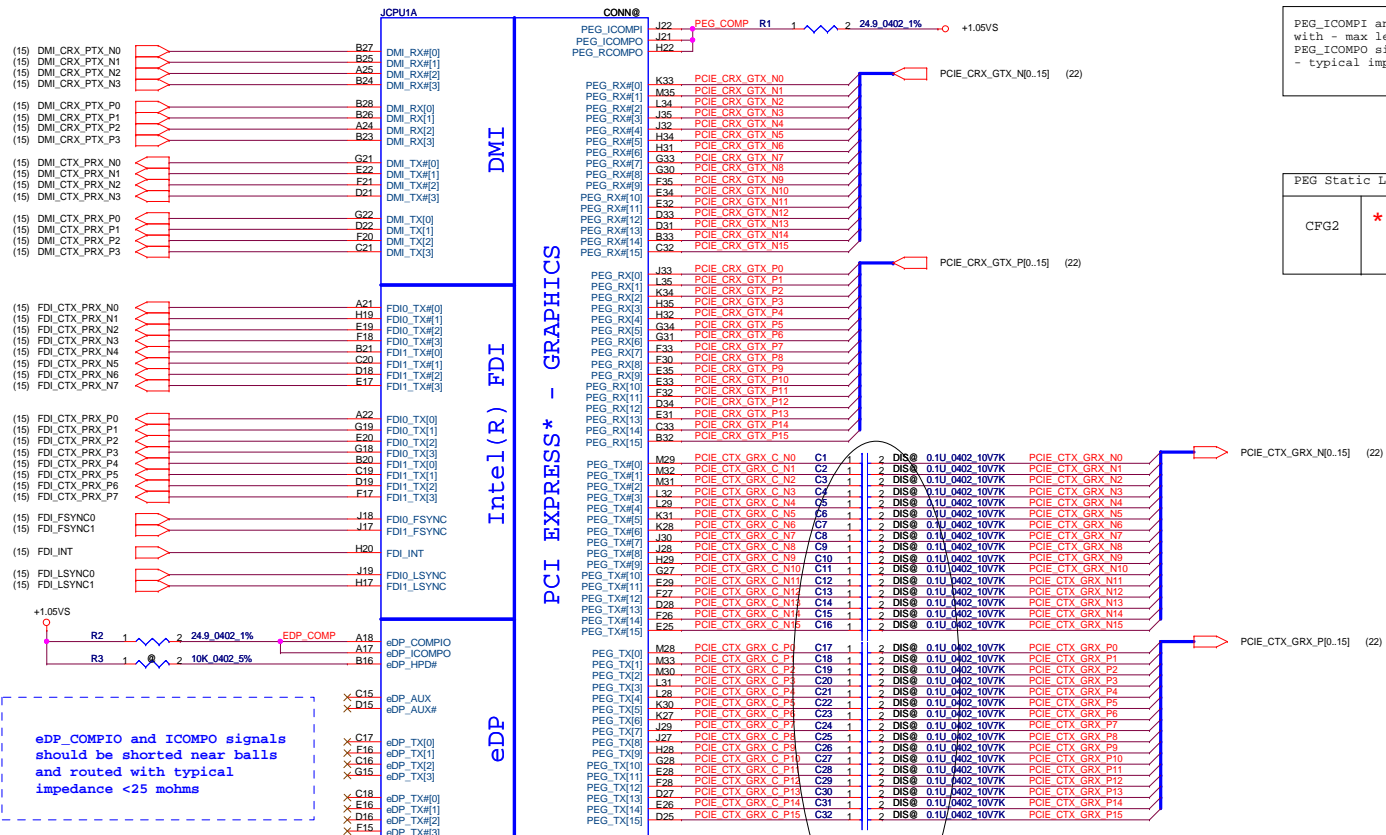
	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	
		1	USB 3.0 Port (Left Side)
	UHCI1	2	USB 3.0 Port (Left Side)
		3	USB 3.0 Port (Left Side)
	UHCI2	4	
		5	Camera
EHCI2	UHCI3	6	
		7	
		8	
	UHCI4	9	USB Port (Right Side)
		10	Mini Card(WLAN/BT)
	UHCI5	11	FPR
		12	Mini Card(WWAN)
UHCI6	13	Blue Tooth	

BOM Structure Table

BTO Item	BOM Structure
Connector	CONN@
45 LEVEL	45@
Unpop	@
nVidia	DIS@
INTEL DD3 M3	M3@
SIM Card Slot	3G@
Intel UMA	UMA@
VRAM Option	X76@
Intel SBA	SBA@
Intel AOAC	AOAC@
TPM	TPM@
GPU N13M	N13M@
GPU N13P	N13MP

SMBUS Control Table

	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW					
SMB_EC_CK2	KB9012	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW							+3VS
SMBCLK	PCH	X	X	X	V	V	X	X
SMBDATA	+3VALW				+3VS	+3VS		
SMLCLK	PCH	X	X	X	X	X	X	X
SMLDATA	+3VALW							
SML1CLK	PCH	V	X	V	X	X	V	X
SML1DATA	+3VALW	+3VS		+3VS			+3VS	



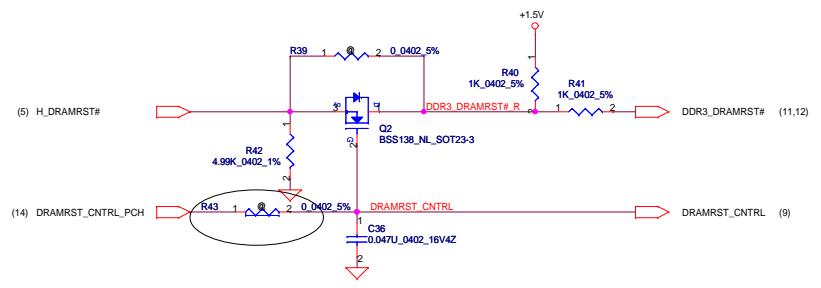
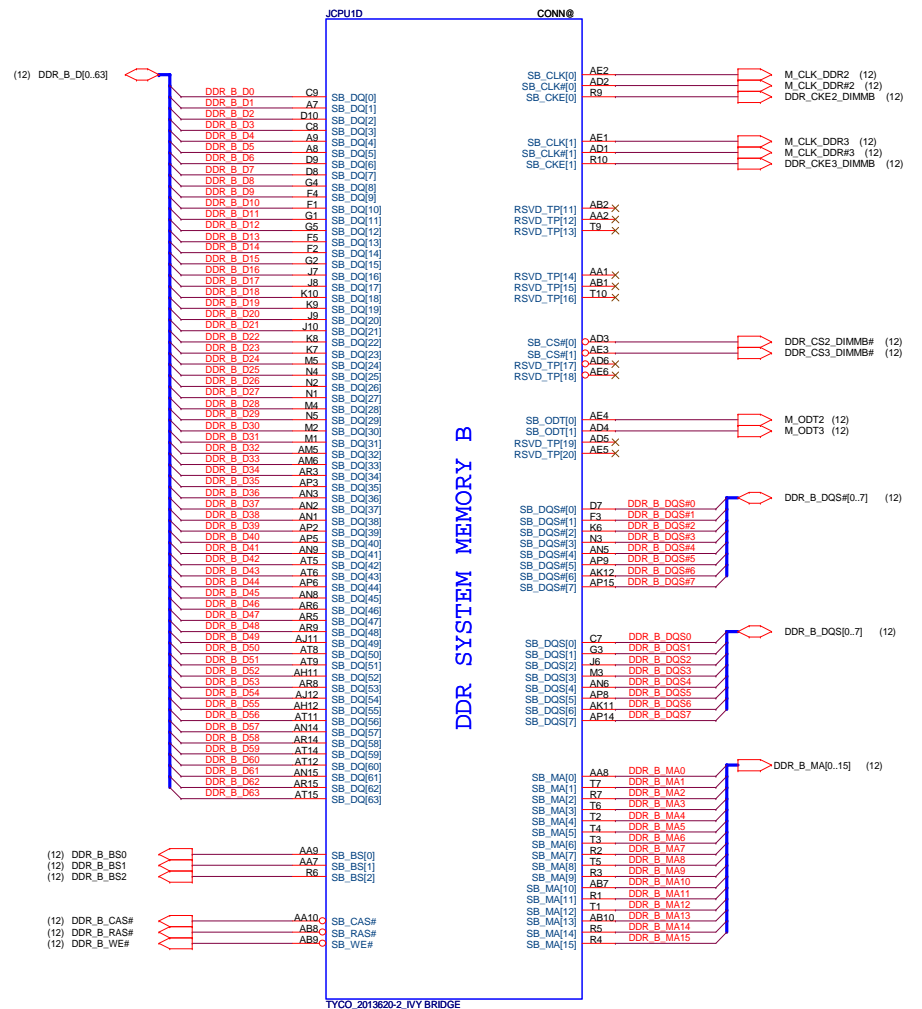
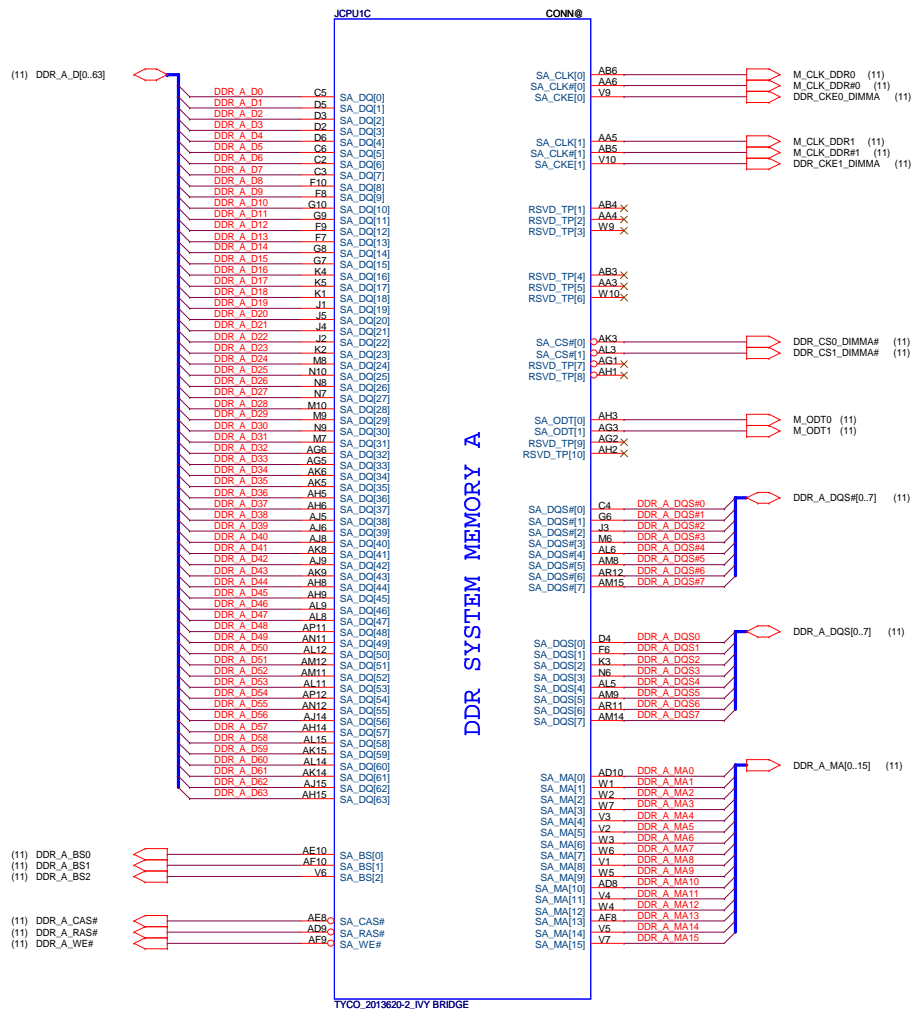
eDP_COMPIO and ICOMPO signals should be shorted and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

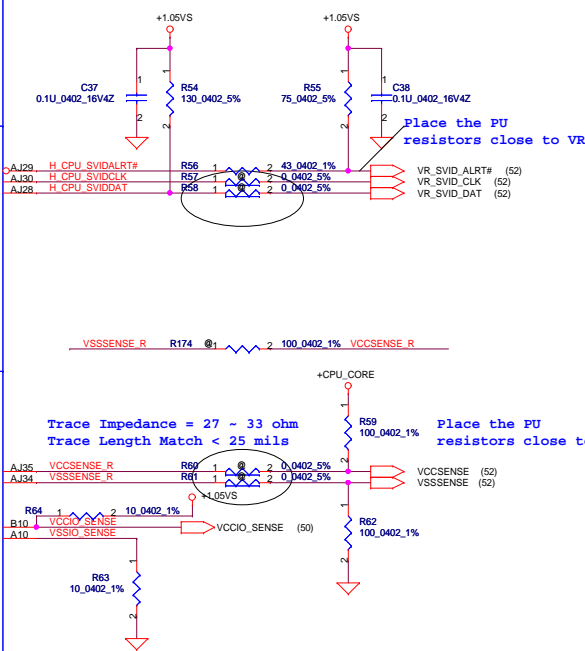
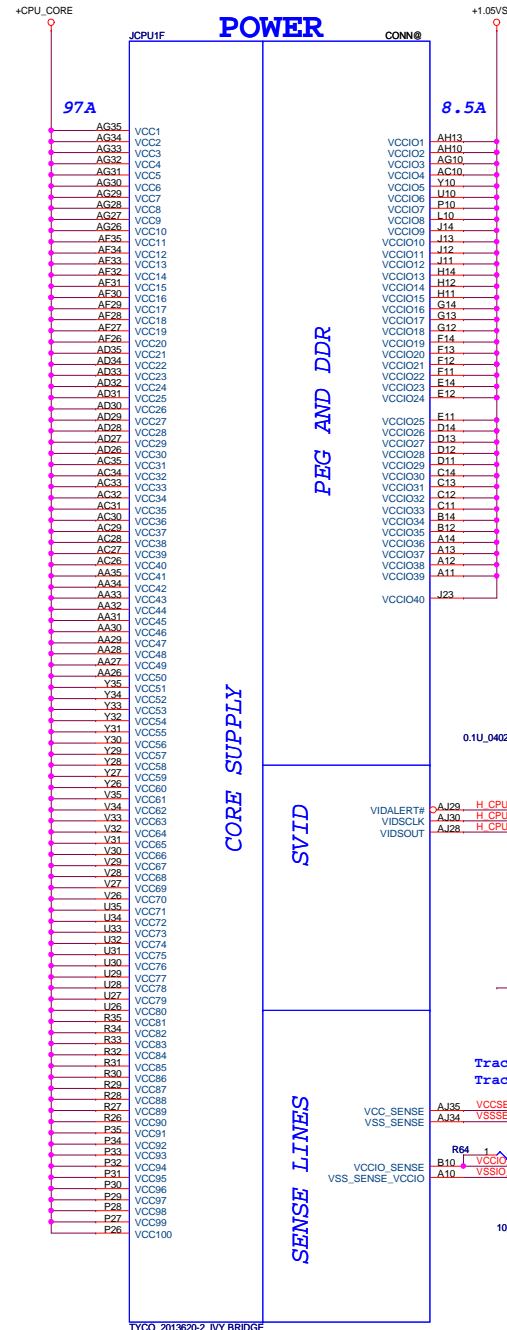
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed

Nvidia support PCIe Gen2

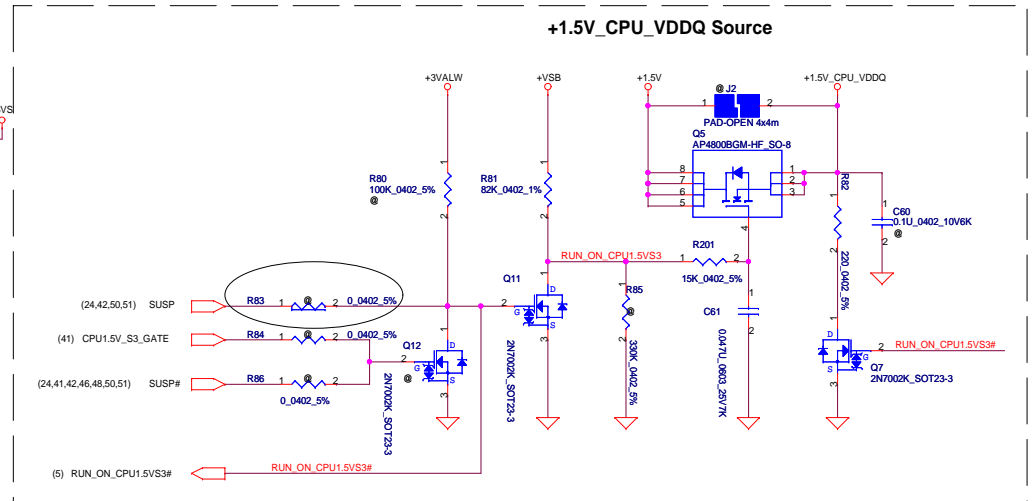
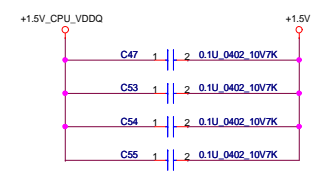
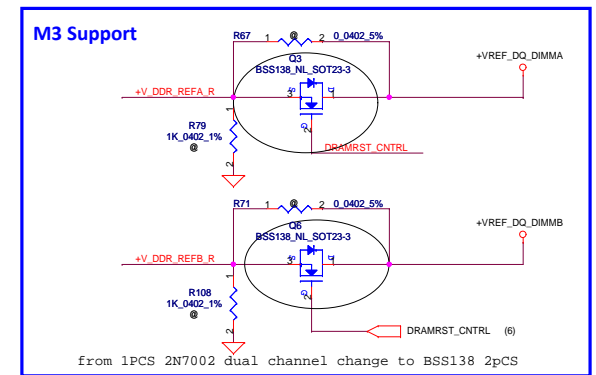
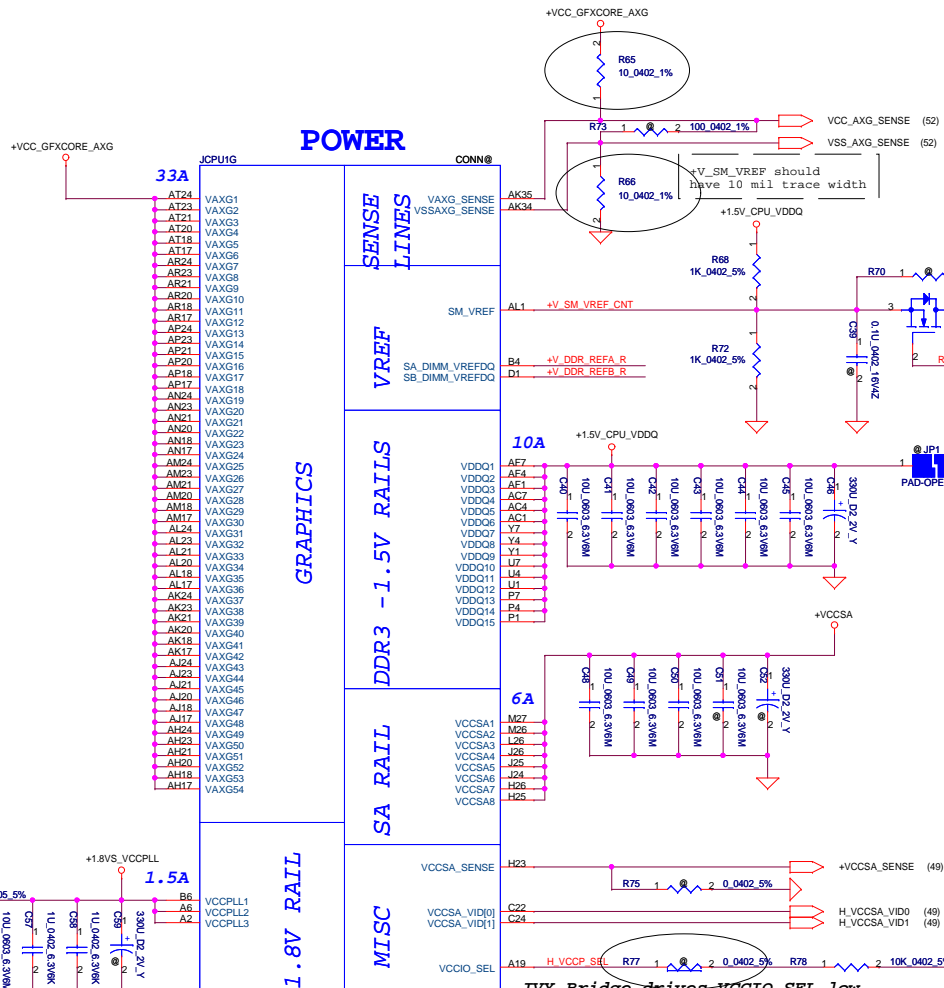


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Issued Date	2011/07/12	Deciphered Date	2012/07/01	PROCESSOR(3/7) DDRIII	
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TYCO_2013620-2_IVY BRIDGE

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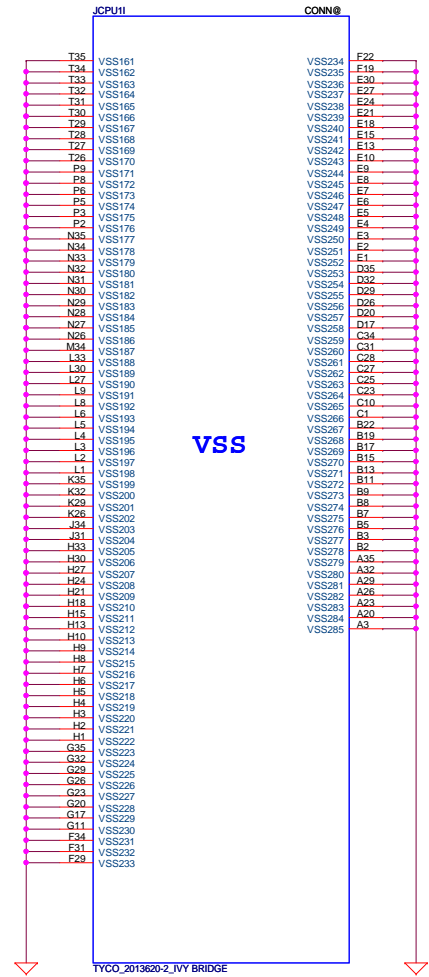
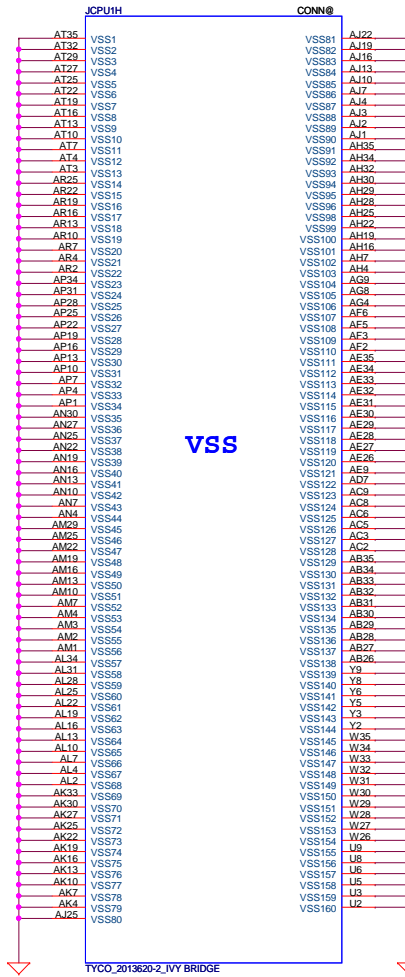
Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

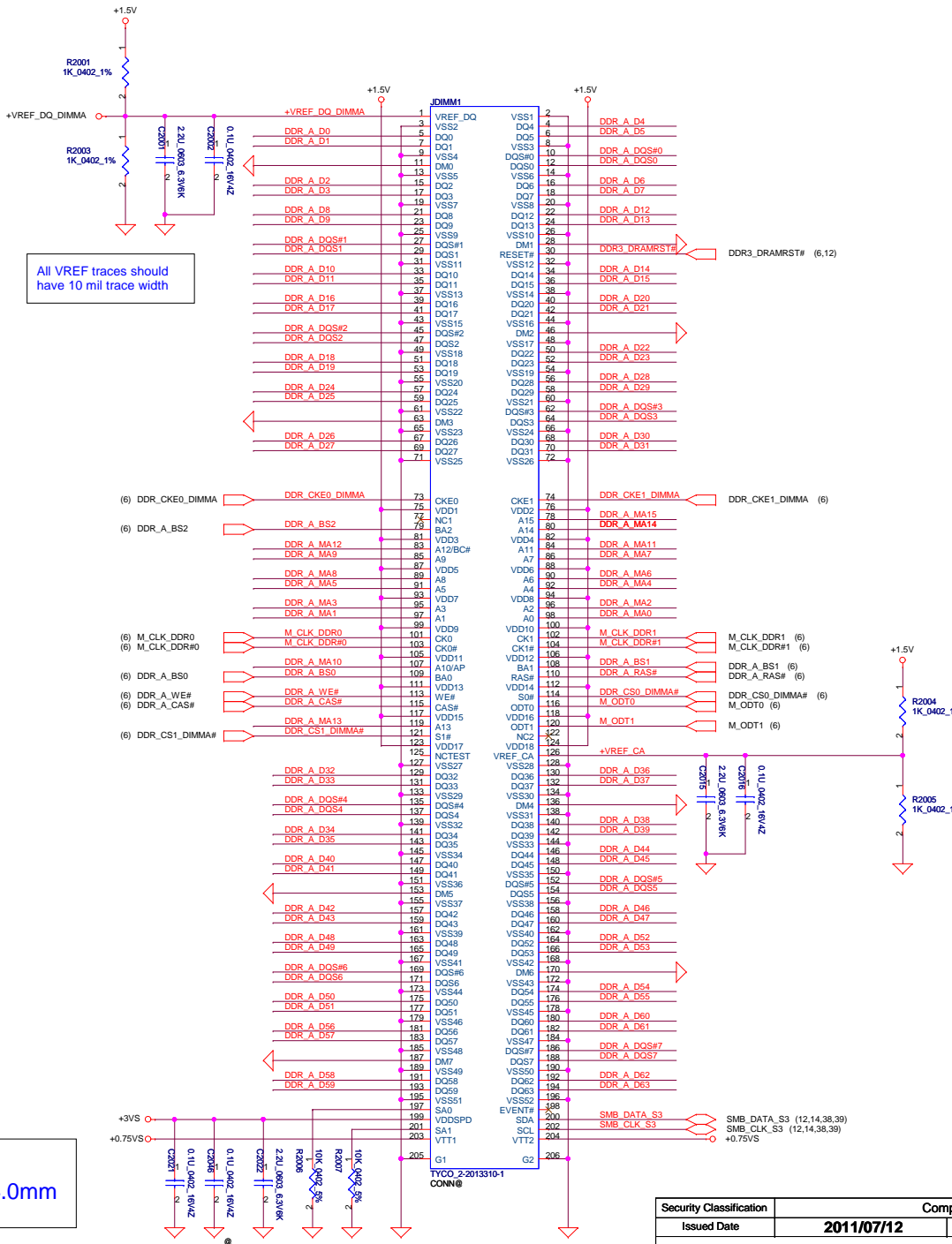
IVY Bridge drives VCCIO_SEL low
VCCP_PWRCTRL:0

Sandy Bridge is NC for A19
VCCP_PWRCTRL:1

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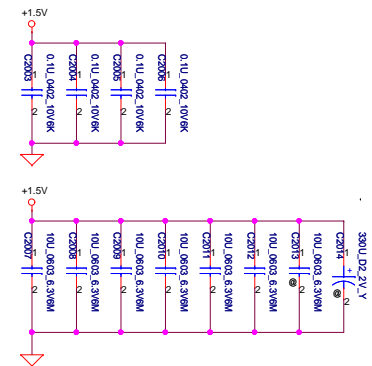


All VREF traces should have 10 mil trace width

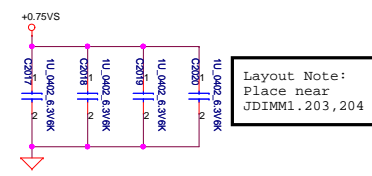
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DIMM_A Reserve H:4.0mm

- DDR_A_DQS#(0..7) (6)
- DDR_A_DQS(0..7) (6)
- DDR_A_D(0..63) (6)
- DDR_A_MA(0..15) (6)

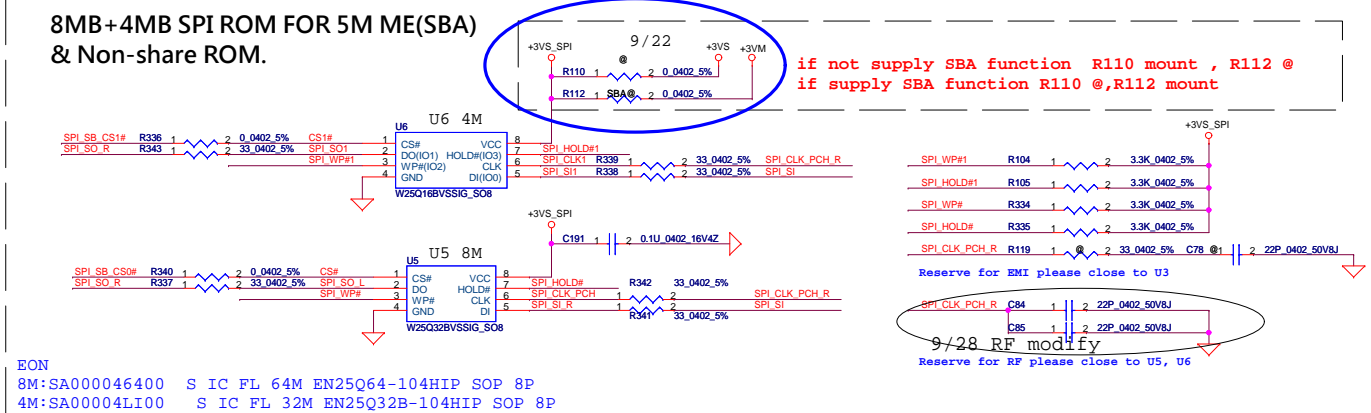
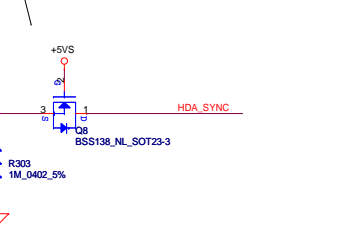
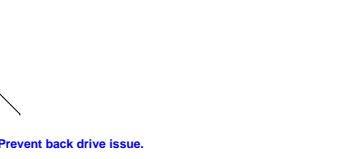
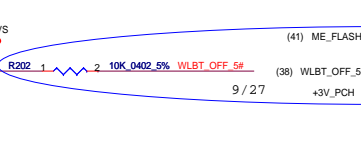
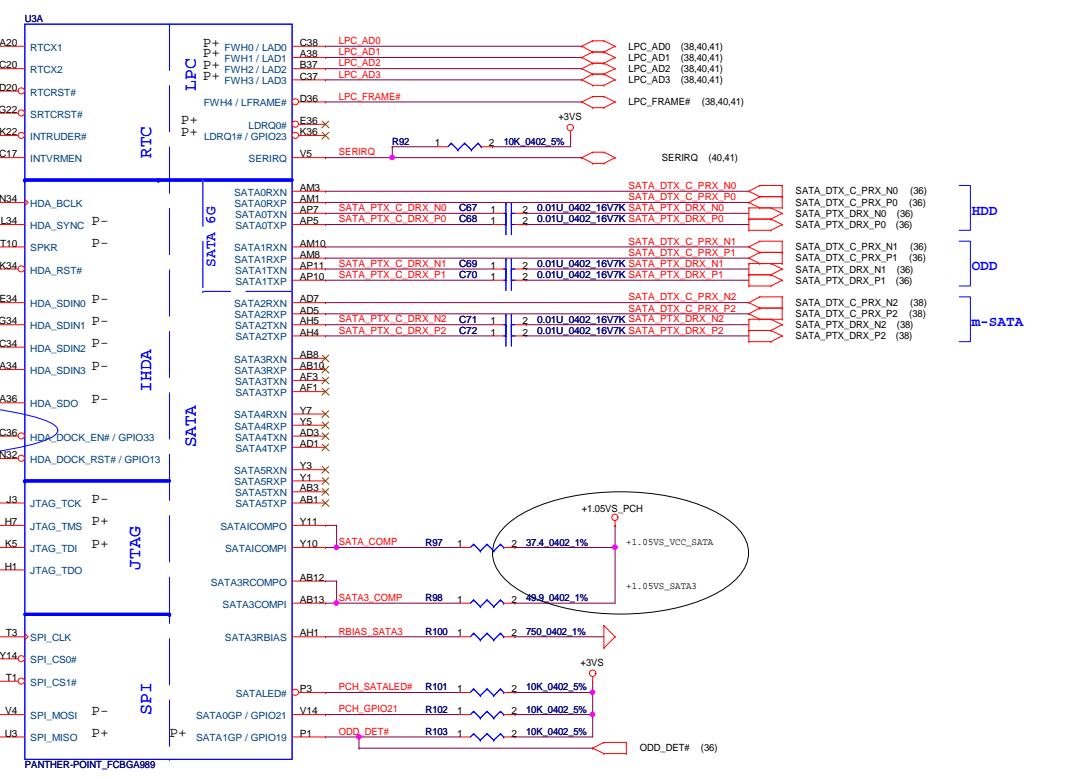
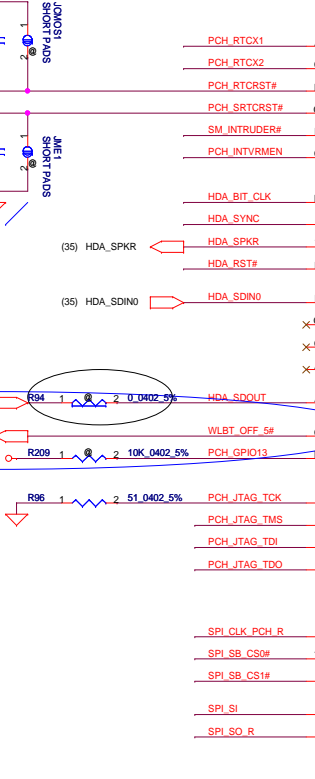
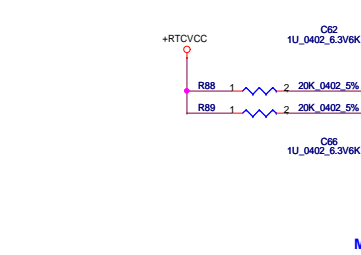
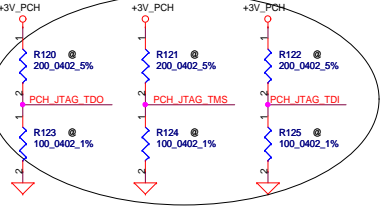
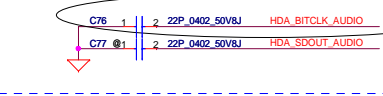
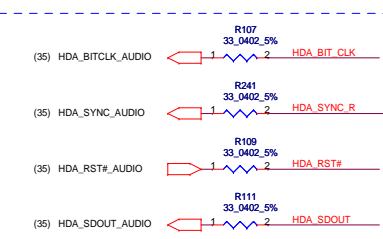
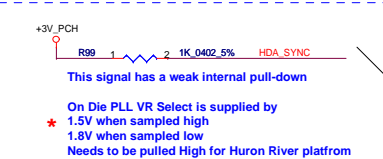
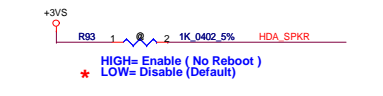
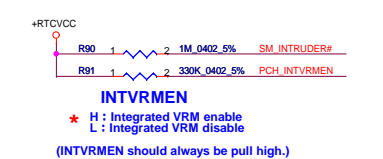
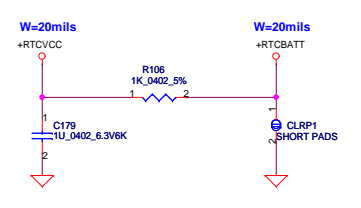
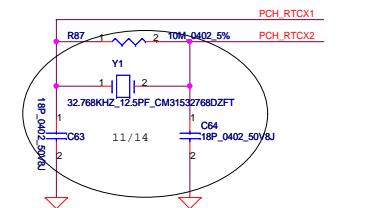
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JDIMM1



Layout Note:
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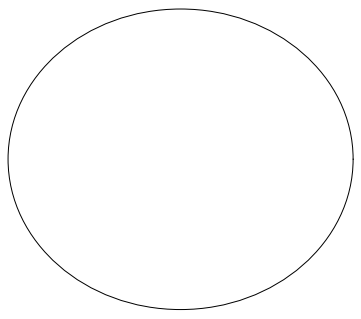
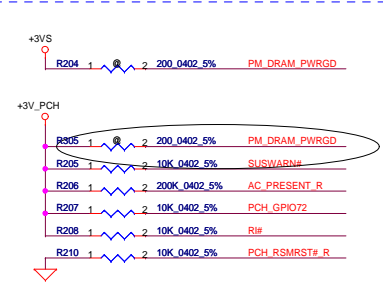
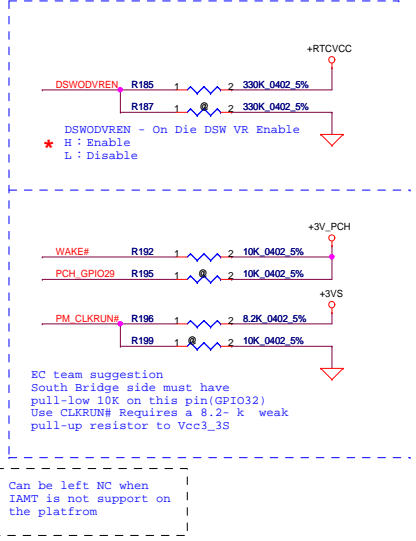
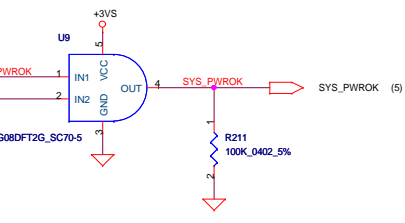
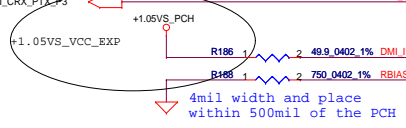
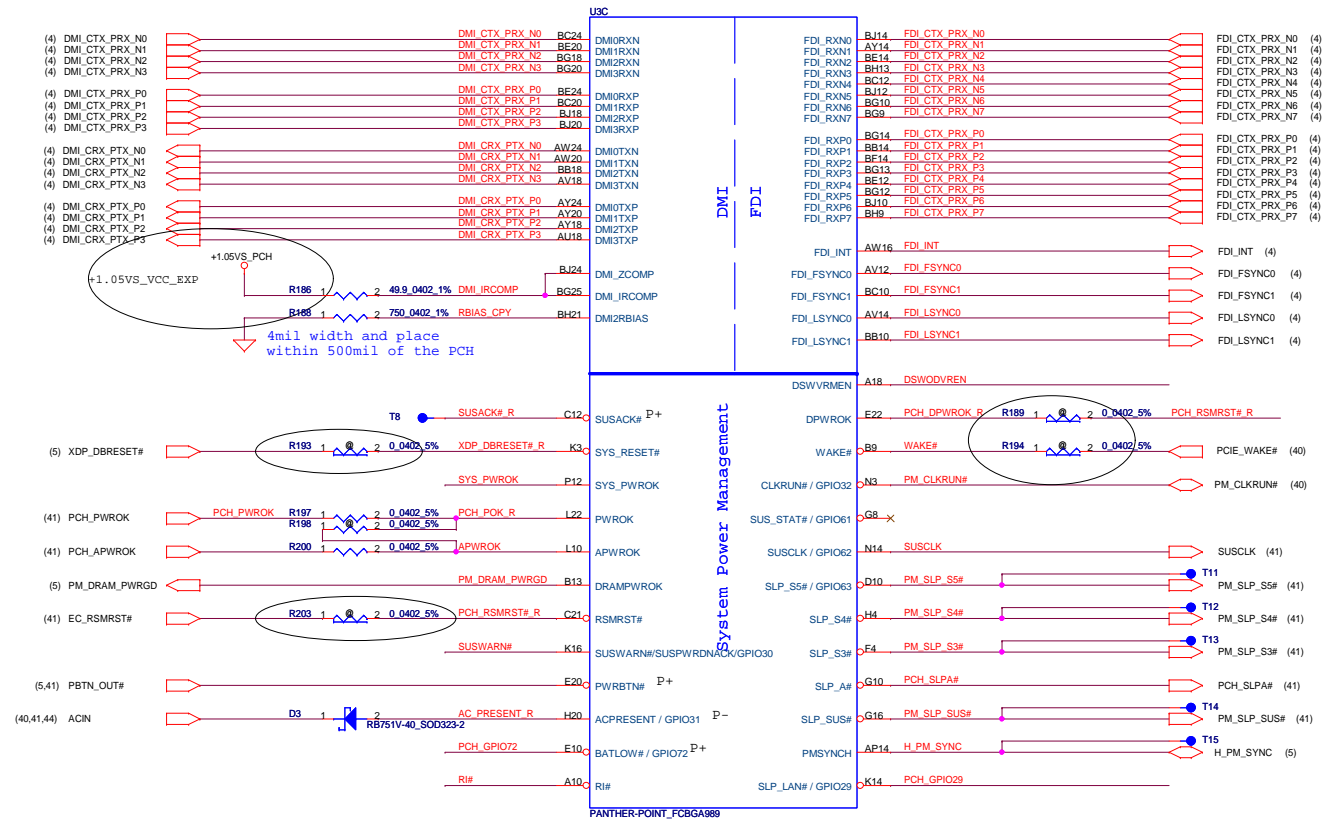


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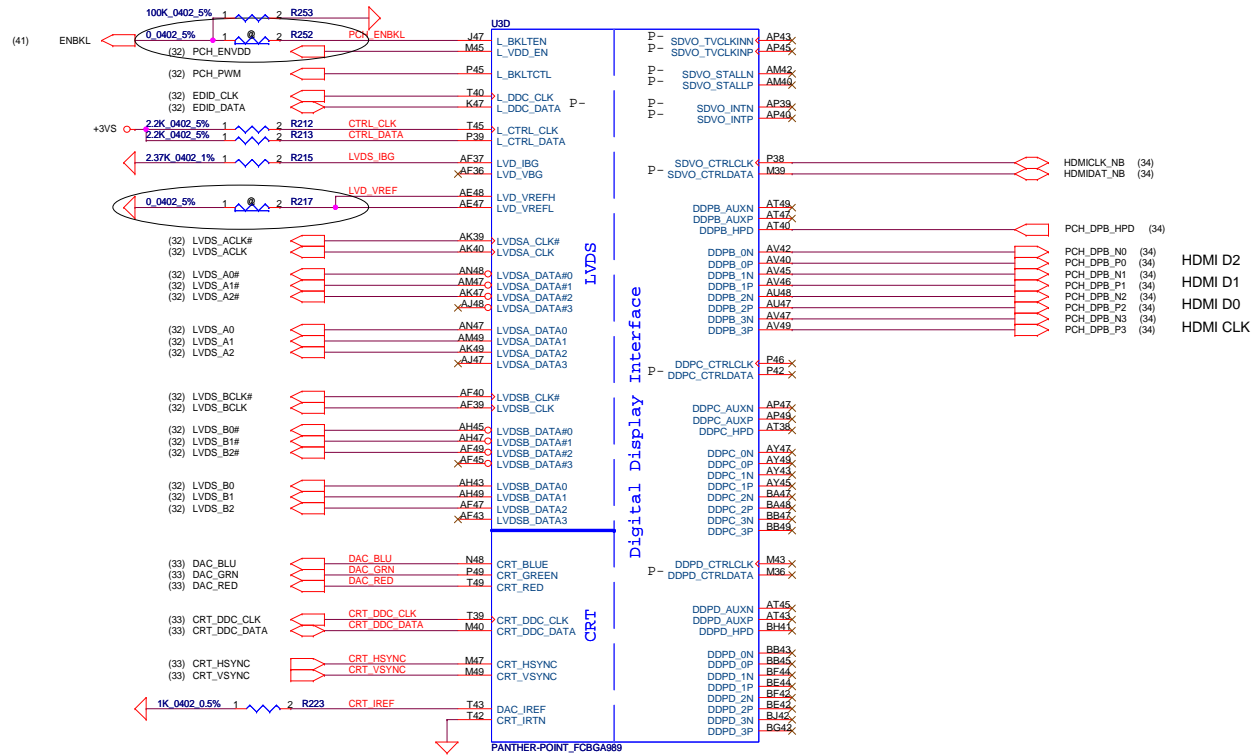


BON
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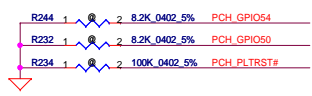
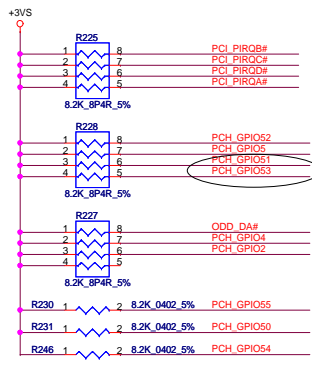
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Issued Date	2011/07/12	Deciphered Date	2012/07/01	PCH (1/9) SATA,HDA,SPI, LPC	
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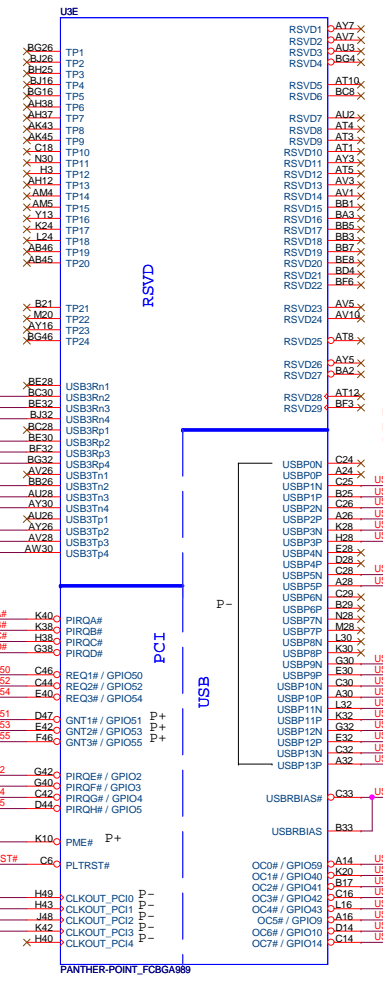
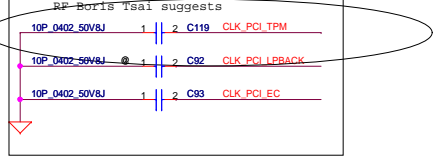
R243 1K 0402_5% PCH_GPIO51

Boot BIOS Strap bit1 BBS1		
GPIO51	GPIO19	Boot BIOS Destination
Bit11	Bit10	
0	1	Reserved
1	0	PCI
1	1	SPI (Default)
0	0	LPC

R245 1K 0402_5% PCH_GPIO55

A16 swap override Strap/Top-Block Swap Override jumper

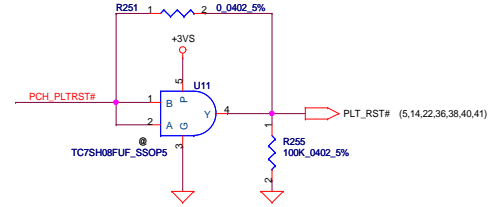
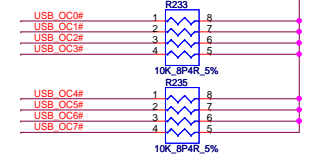
PCI_GNT3# Low=A16 swap override/Top-Block Swap Override enabled High=Default *



PCH HM65 config not support USB port 6 & 7.

- USB 3.0
- USB 3.0
- USB 3.0
- CMOS Camera (LVDS)
- USB 2.0
- Mini Card(WLAN/BT)
- FingerPrint
- Mini Card(WWAN)
- Bluetooth Module

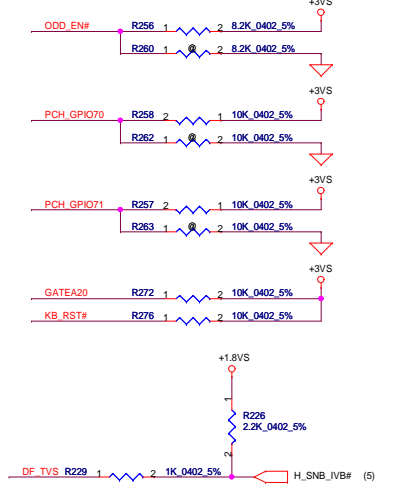
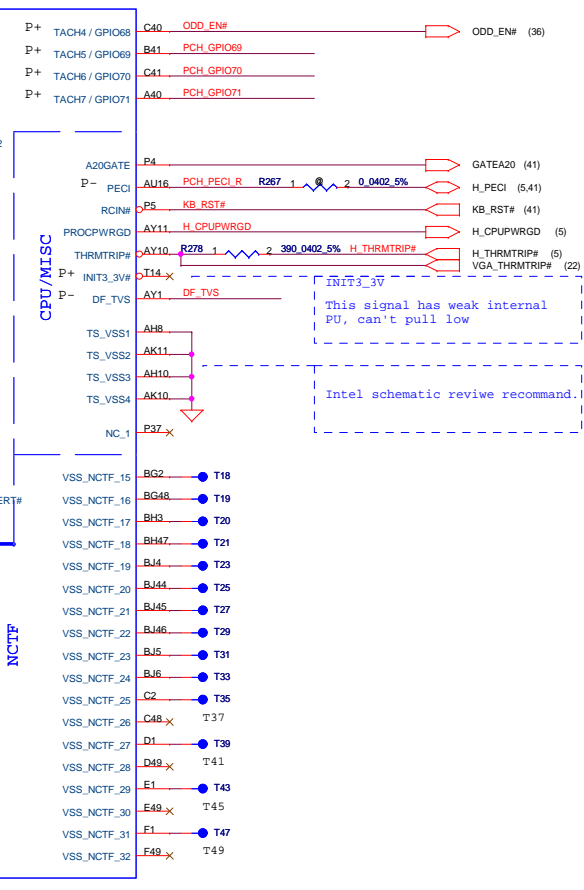
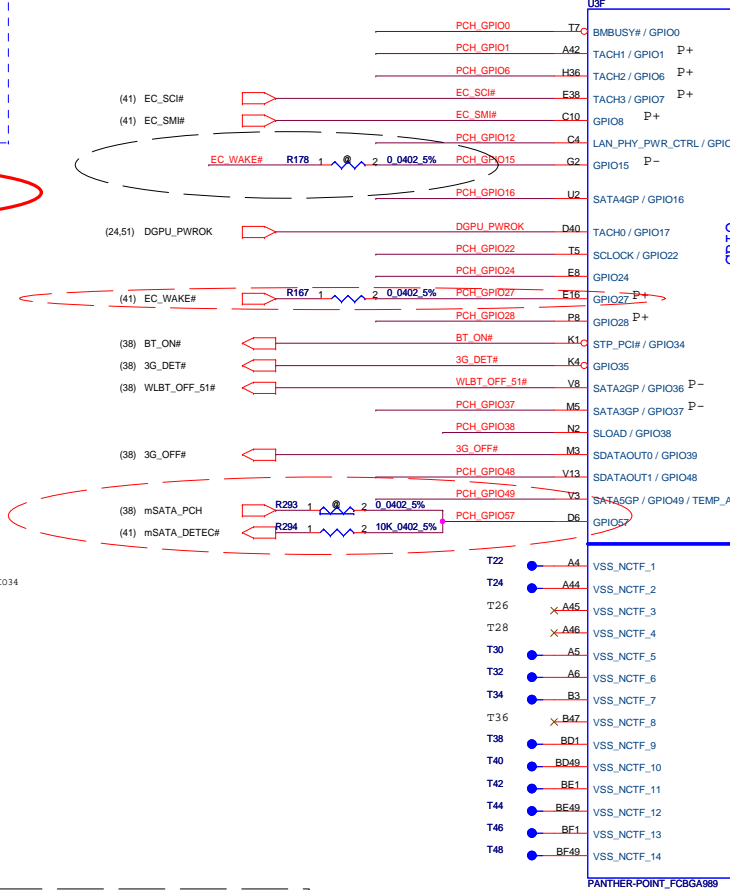
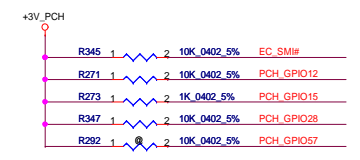
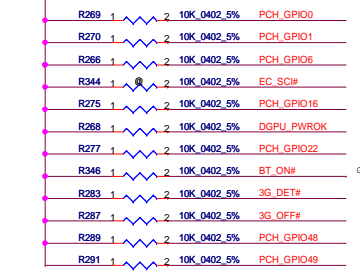
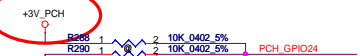
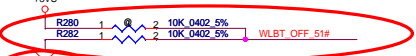
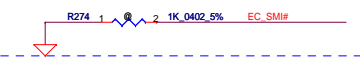
OC[0..3] use for EHCI 1
 OC[4..7] use for EHCI 2



GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable



GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

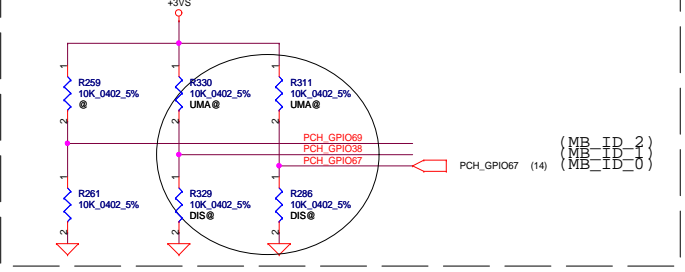


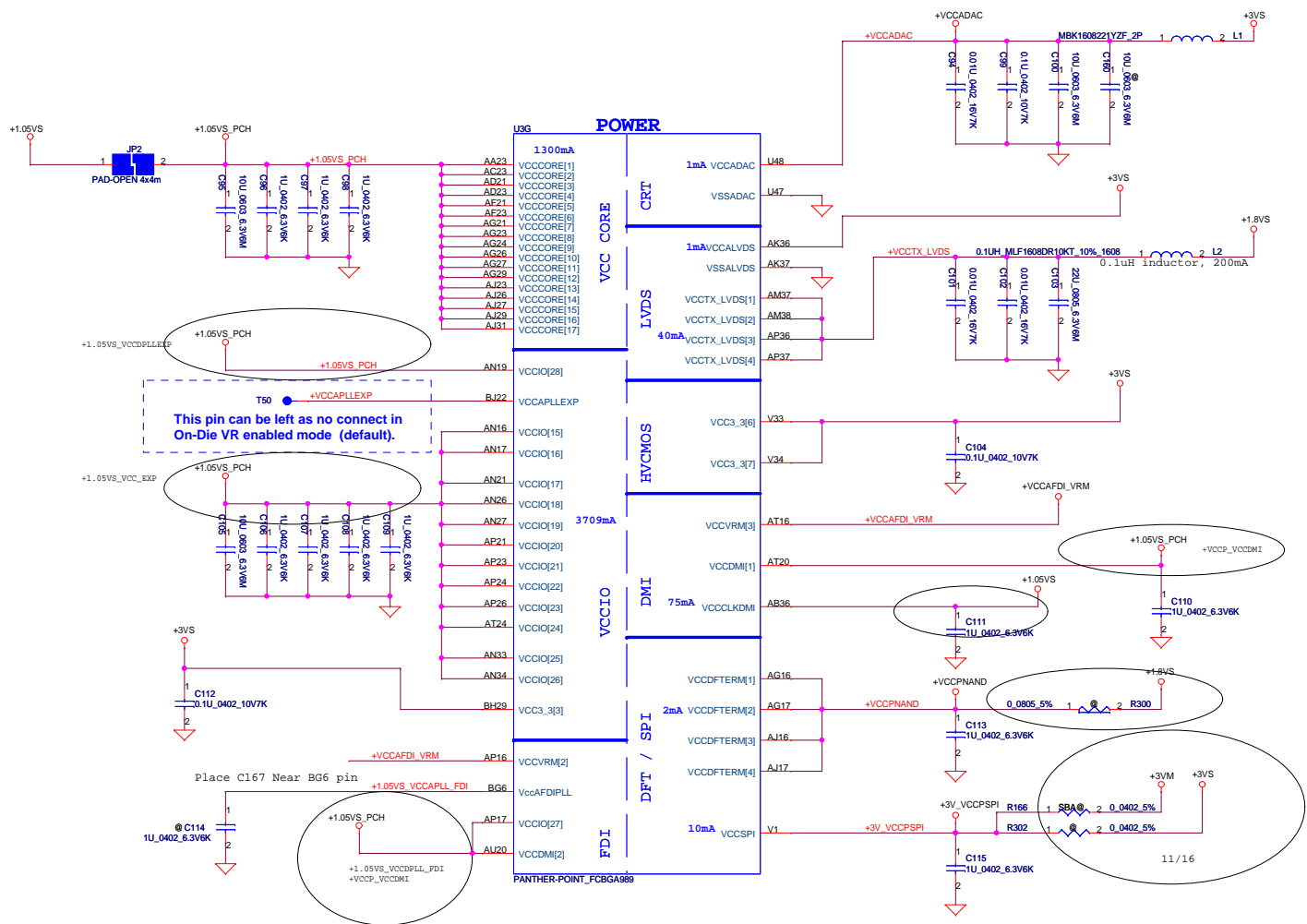
DMI Termination Voltage	
NV_CLB	Set to Vcc when HIGH
	Set to Vss when LOW

CLOSE TO THE BRANCHING POINT

For Edge code setting

PCH_GPIO69	PCH_GPIO38	PCH_GPIO67	Function
0	0	0	Optimus
0	0	1	Reserved
0	1	0	DIS
0	1	1	UMA





+1.05VS_VCCDFLLEXP

+1.05VS_PCH

+1.05VS_VCC_EXP

+1.05VS_PCH

+1.05VS_PCH

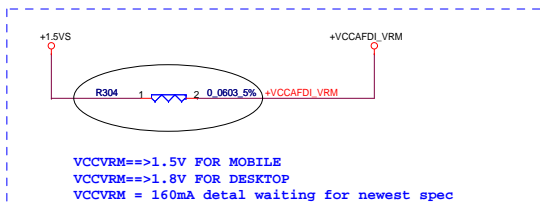
+3VS

+VCCAFDI_VRM

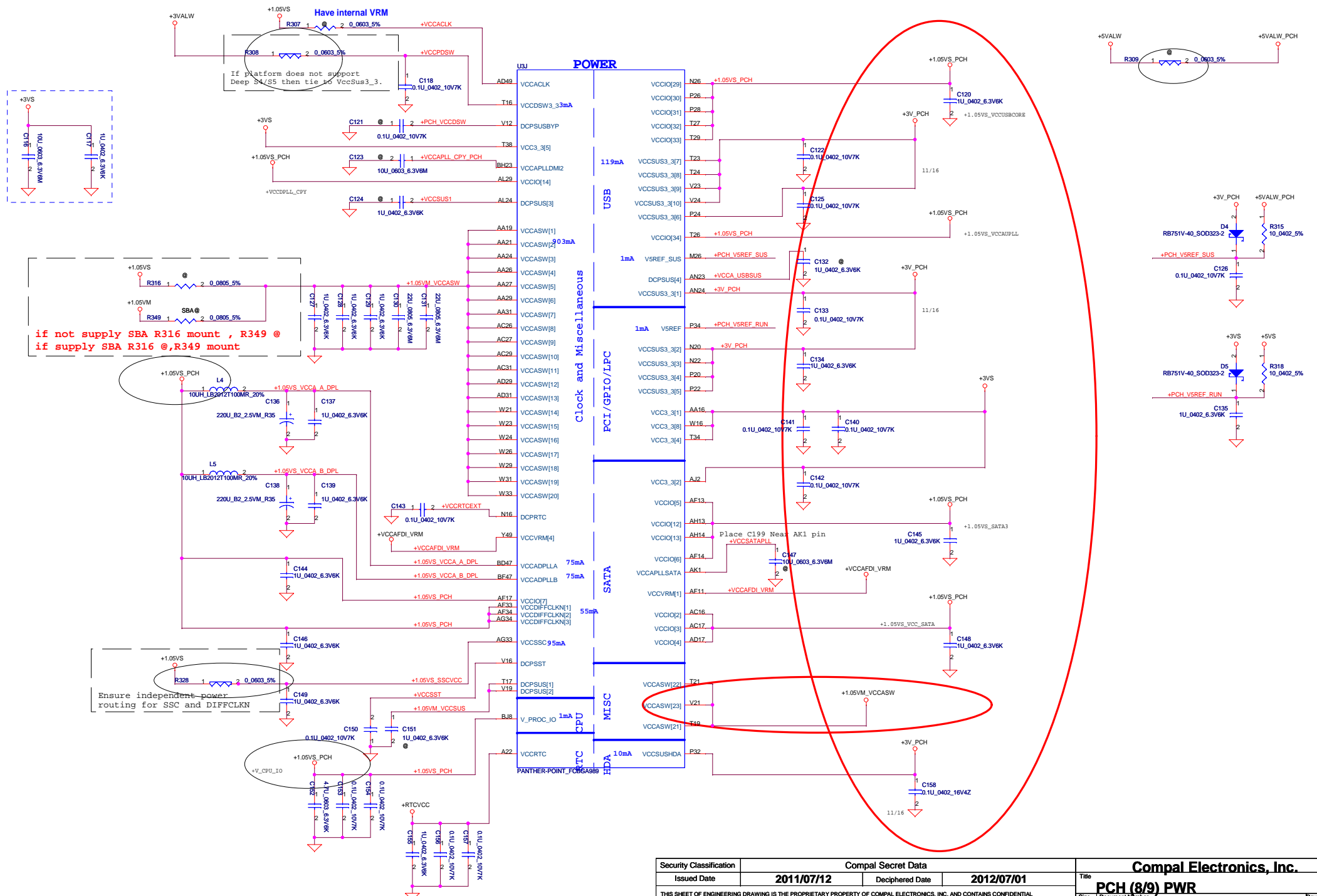
+1.05VS_VCCDFLL_FDI +VCCP_VCCDMI

+1.05VS_PCH

+1.05VS_VCCDFLL_FDI +VCCP_VCCDMI



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Compal Electronics, Inc.			PCH (7/9) PWR	
Size			Document Number	
Date			LA-8133P	
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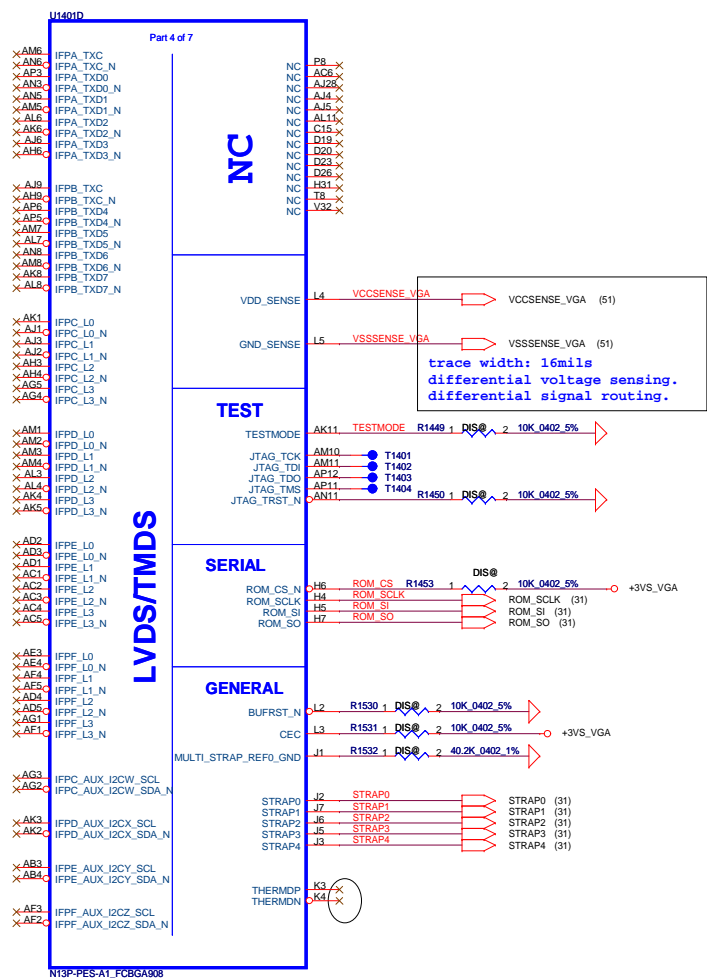
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Date:	Friday, January 13, 2012	Sheet	20	of 58	

U3H		U3I	
H5	VSS[0]	AK38	VSS[159]
AA17	VSS[1]	AK4	VSS[160]
AA2	VSS[2]	AK42	VSS[161]
AA3	VSS[3]	AK46	VSS[162]
AA33	VSS[4]	AK6	VSS[163]
AA34	VSS[5]	AL16	VSS[164]
AB11	VSS[6]	AL17	VSS[165]
AB14	VSS[7]	AL2	VSS[166]
AB30	VSS[8]	AL21	VSS[167]
AB4	VSS[9]	AL22	VSS[168]
AB43	VSS[10]	AL26	VSS[169]
AB5	VSS[11]	AL27	VSS[170]
AB7	VSS[12]	AL31	VSS[171]
AC19	VSS[13]	AL33	VSS[172]
AC2	VSS[14]	AL34	VSS[173]
AC21	VSS[15]	AL48	VSS[174]
AC24	VSS[16]	AM11	VSS[175]
AC33	VSS[17]	AM14	VSS[176]
AC34	VSS[18]	AM36	VSS[177]
AC48	VSS[19]	AM39	VSS[178]
AD10	VSS[20]	AM43	VSS[179]
AD11	VSS[21]	AM45	VSS[180]
AD12	VSS[22]	AM6	VSS[181]
AD13	VSS[23]	AM7	VSS[182]
AD19	VSS[24]	AN2	VSS[183]
AD24	VSS[25]	AN2	VSS[184]
AD26	VSS[26]	AN2	VSS[185]
AD27	VSS[27]	AN2	VSS[186]
AD33	VSS[28]	AN3	VSS[187]
AD34	VSS[29]	AN31	VSS[188]
AD36	VSS[30]	AP12	VSS[189]
AD37	VSS[31]	AP19	VSS[190]
AD38	VSS[32]	AP28	VSS[191]
AD39	VSS[33]	AP30	VSS[192]
AD4	VSS[34]	AP32	VSS[193]
AD40	VSS[35]	AP38	VSS[194]
AD42	VSS[36]	AP4	VSS[195]
AD43	VSS[37]	AP42	VSS[196]
AD45	VSS[38]	AP46	VSS[197]
AD46	VSS[39]	AP8	VSS[198]
AD8	VSS[40]	AR2	VSS[199]
AE2	VSS[41]	AR48	VSS[200]
AE3	VSS[42]	AT11	VSS[201]
AE10	VSS[43]	AT13	VSS[202]
AE12	VSS[44]	AT18	VSS[203]
AD14	VSS[45]	AT22	VSS[204]
AD16	VSS[46]	AT26	VSS[205]
AE19	VSS[47]	AT28	VSS[206]
AF24	VSS[48]	AT30	VSS[207]
AF25	VSS[49]	AT32	VSS[208]
AF26	VSS[50]	AT34	VSS[209]
AF27	VSS[51]	AT39	VSS[210]
AF29	VSS[52]	AT42	VSS[211]
AF31	VSS[53]	AT46	VSS[212]
AF4	VSS[54]	AT7	VSS[213]
AE42	VSS[55]	AU24	VSS[214]
AE4	VSS[56]	AU30	VSS[215]
AE5	VSS[57]	AV16	VSS[216]
AE7	VSS[58]	AV20	VSS[217]
AE7	VSS[59]	AV24	VSS[218]
AF8	VSS[60]	AV30	VSS[219]
AG19	VSS[61]	AV38	VSS[220]
AG2	VSS[62]	AV4	VSS[221]
AG31	VSS[63]	AV43	VSS[222]
AG48	VSS[64]	AV8	VSS[223]
AH11	VSS[65]	AW14	VSS[224]
AH3	VSS[66]	AW18	VSS[225]
AH36	VSS[67]	AW2	VSS[226]
AH39	VSS[68]	AW22	VSS[227]
AH40	VSS[69]	AW26	VSS[228]
AH42	VSS[70]	AW28	VSS[229]
AH46	VSS[71]	AW32	VSS[230]
AH7	VSS[72]	AW34	VSS[231]
AJ19	VSS[73]	AW36	VSS[232]
AJ21	VSS[74]	AW40	VSS[233]
AJ24	VSS[75]	AW48	VSS[234]
AJ33	VSS[76]	AV11	VSS[235]
AJ34	VSS[77]	AY12	VSS[236]
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AK	VSS[79]	AY28	VSS[238]
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		AY8	VSS[242]
		B11	VSS[243]
		B15	VSS[244]
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		B7	VSS[251]
		F45	VSS[252]
		BB12	VSS[253]
		BB16	VSS[254]
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		BC32	VSS[267]
		BC34	VSS[268]
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		BC42	VSS[270]
		BC48	VSS[271]
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		BE22	VSS[273]
		BE40	VSS[274]
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		BF16	VSS[277]
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		BF26	VSS[281]
		BF28	VSS[282]
		BF30	VSS[283]
		BF38	VSS[284]
		BF40	VSS[285]
		BG17	VSS[286]
		BG21	VSS[287]
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		BH15	VSS[292]
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		BH19	VSS[294]
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		BH33	VSS[297]
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		H32	VSS[329]
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		F3	VSS[331]
		VSS[259]	HA6
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		VSS[262]	K30
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		VSS[276]	M24
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		VSS[279]	M38
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		VSS[282]	M6
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		VSS[301]	W34
		VSS[302]	T46
		VSS[303]	T47
		VSS[304]	T8
		VSS[305]	V11
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		VSS[307]	V26
		VSS[308]	V27
		VSS[309]	V29
		VSS[310]	V31
		VSS[311]	V36
		VSS[312]	V39
		VSS[313]	V43
		VSS[314]	V7
		VSS[315]	W17
		VSS[316]	W19
		VSS[317]	W2
		VSS[318]	W27
		VSS[319]	W48
		VSS[320]	Y26
		VSS[321]	Y4
		VSS[322]	Y42
		VSS[323]	Y46
		VSS[324]	Y8
		VSS[325]	BG29
		VSS[326]	N24
		VSS[327]	AJ3
		VSS[328]	AD47
		VSS[329]	B43
		VSS[330]	BE10
		VSS[331]	BG41
		VSS[332]	G14
		VSS[333]	H16
		VSS[334]	T36
		VSS[335]	BG22
		VSS[336]	BG24
		VSS[337]	C27
		VSS[338]	AP13
		VSS[339]	M14
		VSS[340]	AP3
		VSS[341]	AP1
		VSS[342]	BE16
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		VSS[344]	BG28
		VSS[345]	BJ28
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		VSS[352]	

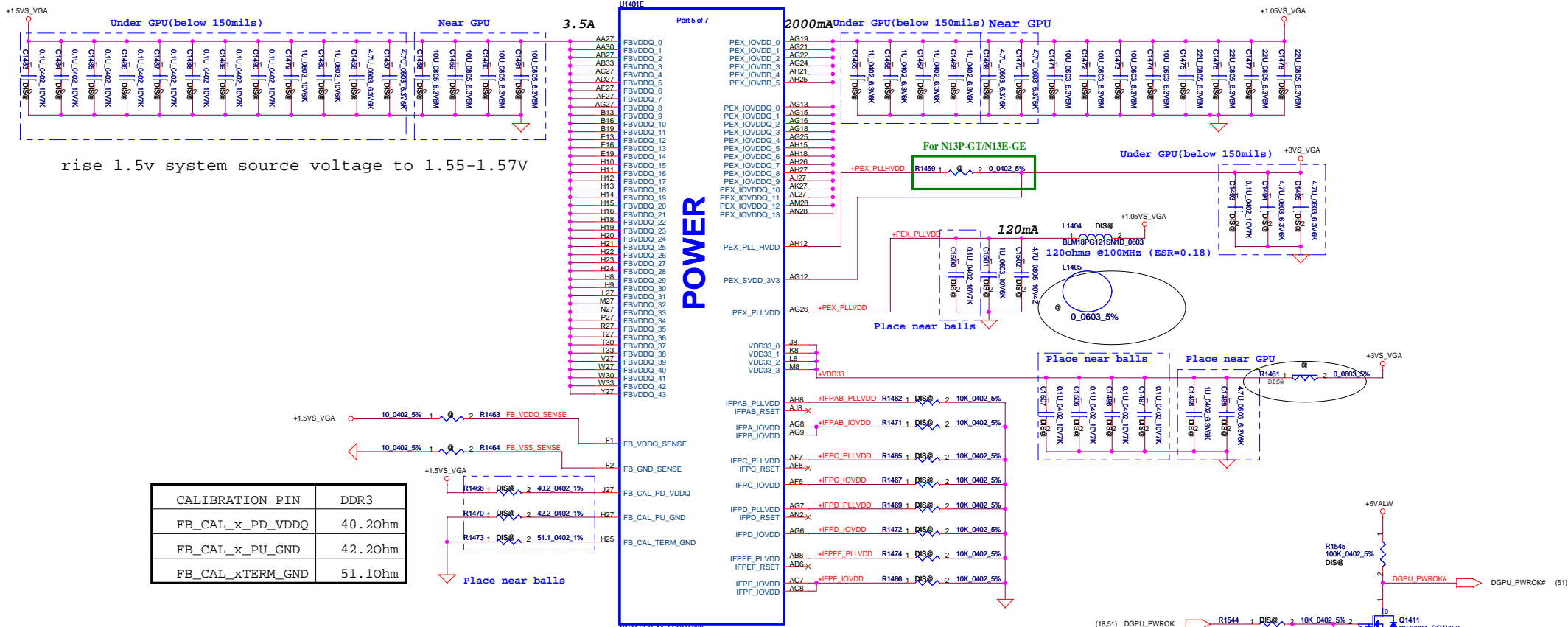
PANTHER-POINT_FCBGA989

PANTHER-POINT_FCBGA989

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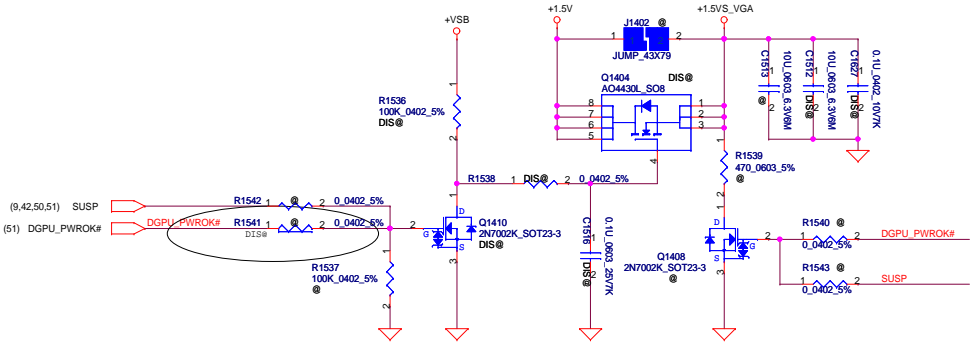
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				Custom	1.0
				Date	Friday, January 13, 2012
				Sheet	23 of 58



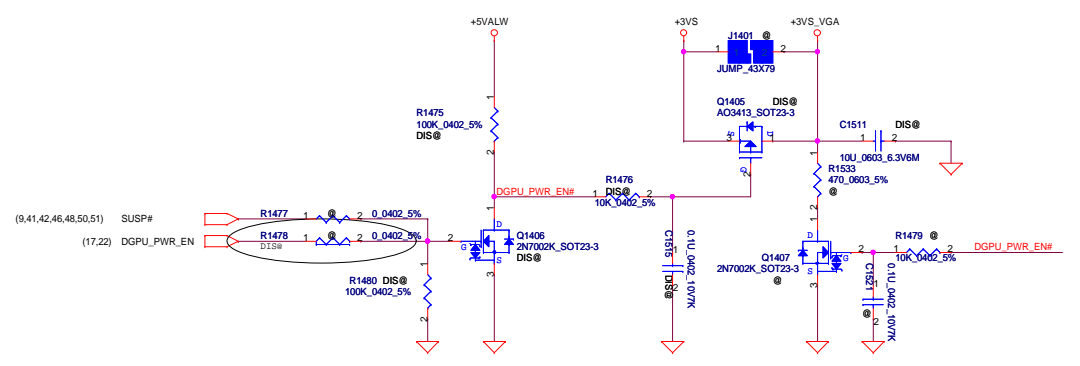
rise 1.5v system source voltage to 1.55-1.57V

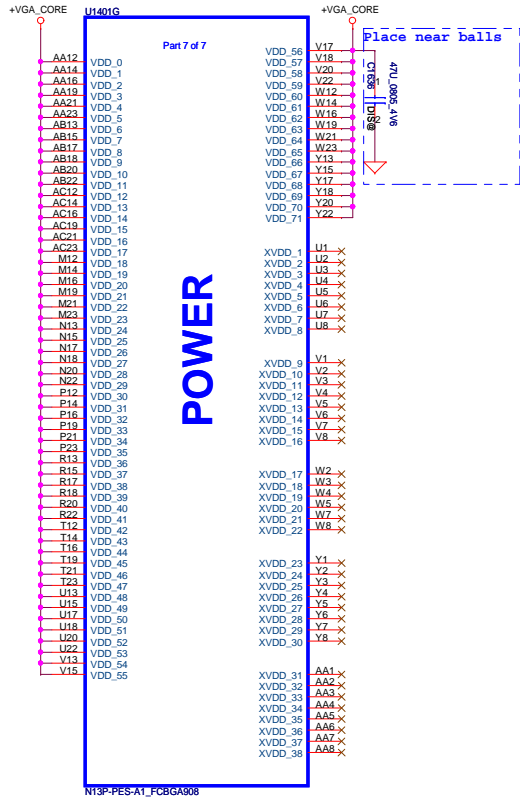
CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	42.2Ohm
FB_CAL_x_TERM_GND	51.1Ohm

+1.5V to +1.5VS_VGA



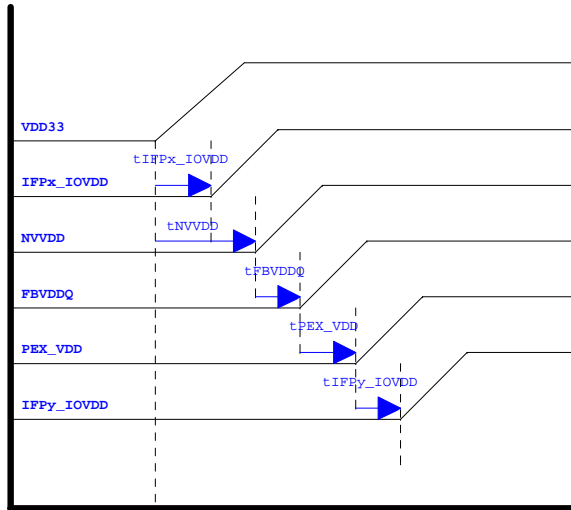
+3VS to +3VS_VGA





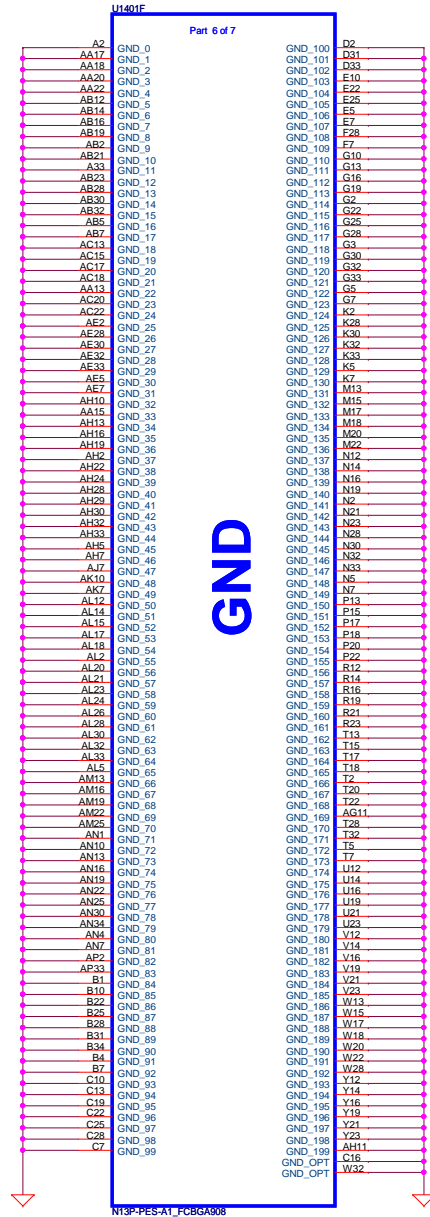
N13P-PES-A1_FcBGA008

DIS@



NV Recommended Power On Sequencing Order

X=A and B
Y=C,D,E and F

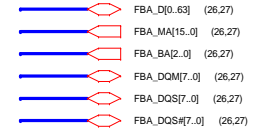
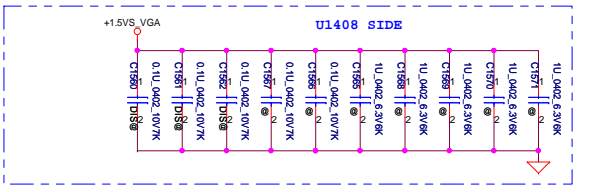
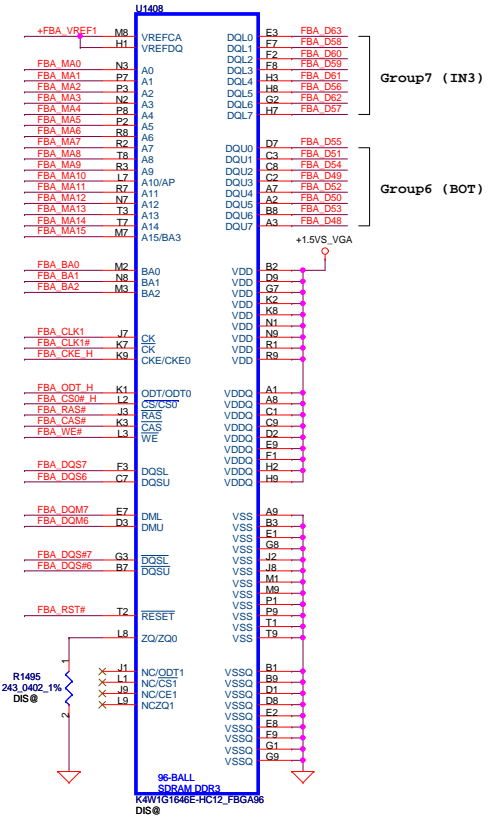
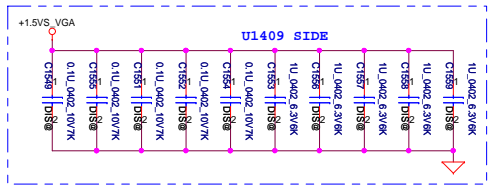
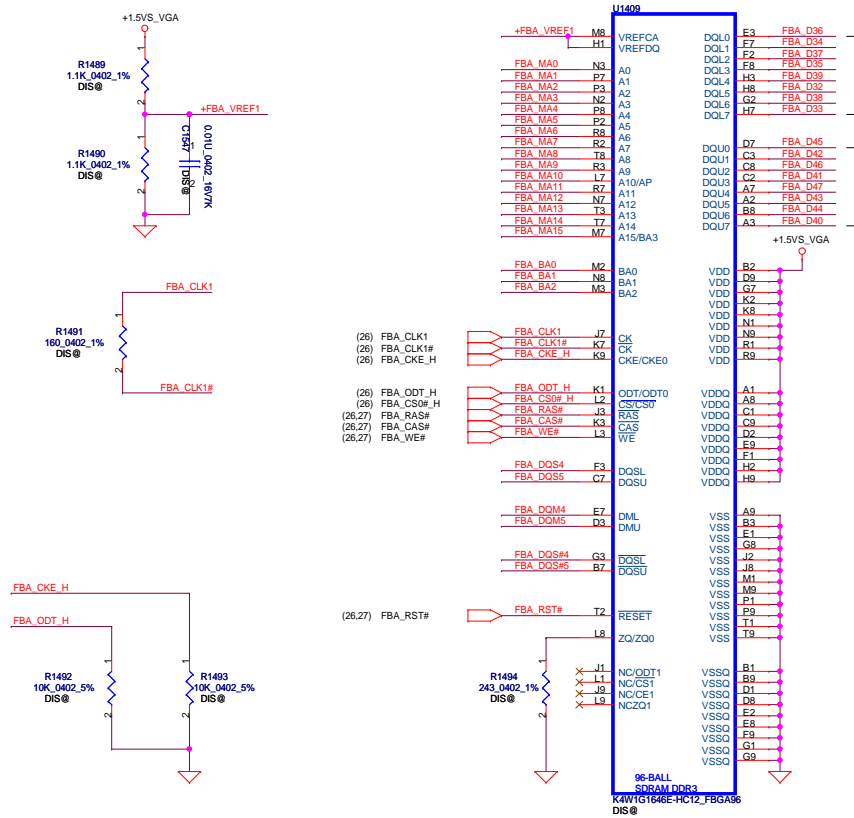


N13P-PES-A1_FcBGA008

DIS@

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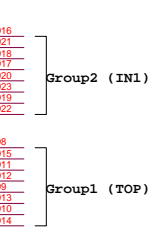
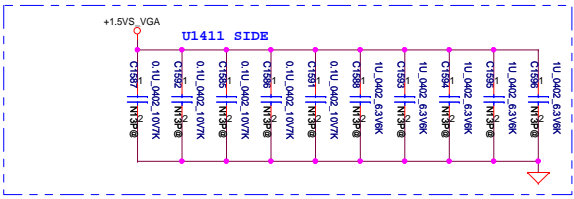
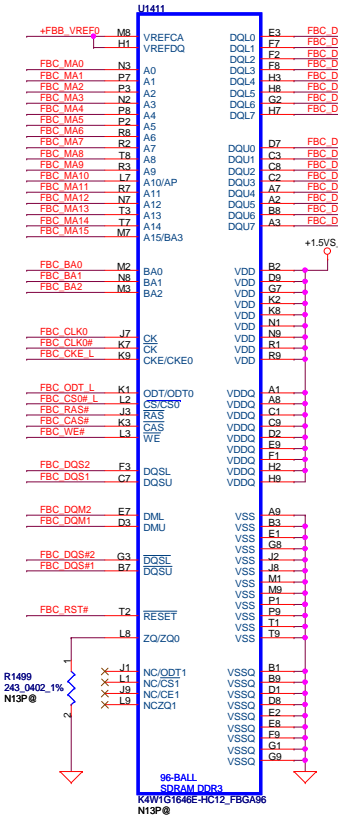
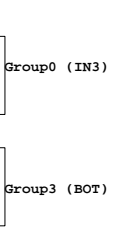
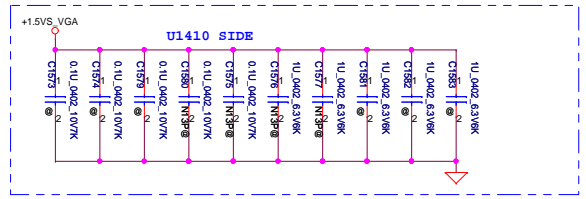
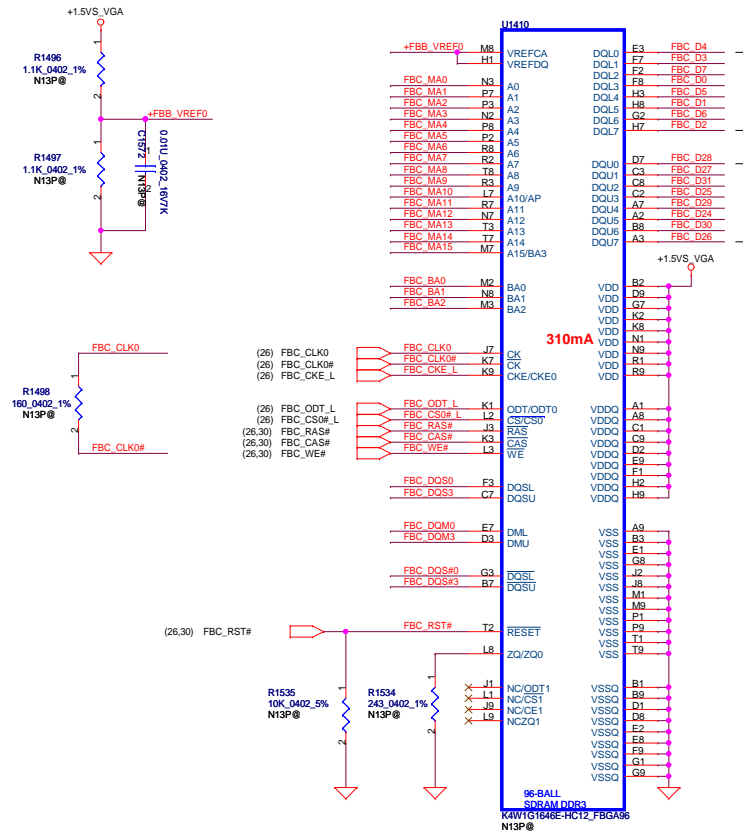
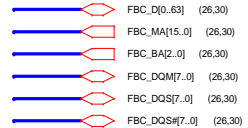
Memory Partition A - Upper 32 bits



Mode D - Mirror Mode Mapping

Address	DATA Bus	
0..31	32..63	
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16	CS0#_H	
FBx_CMD17		
FBx_CMD18	ODT_H	
FBx_CMD19	CKE_H	
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

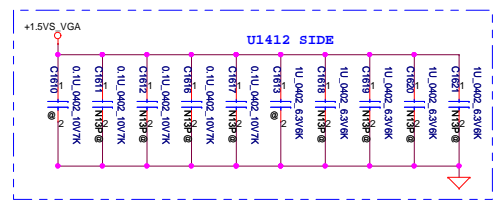
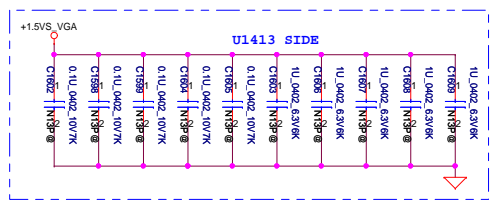
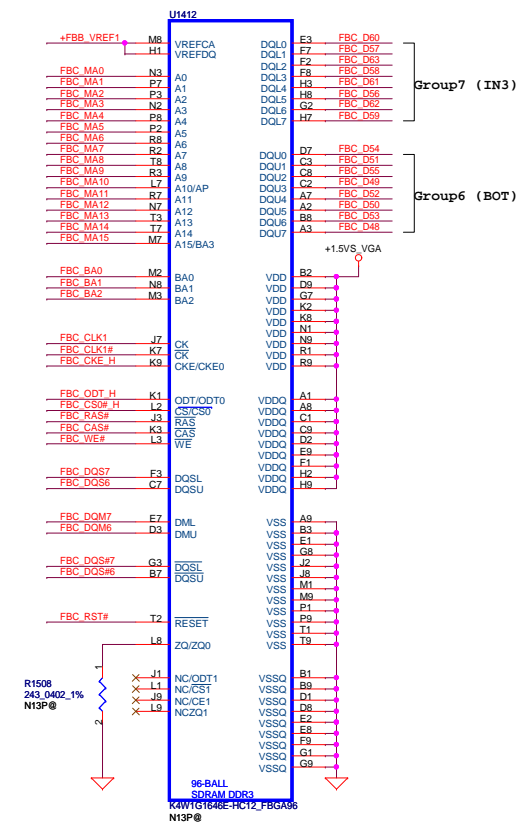
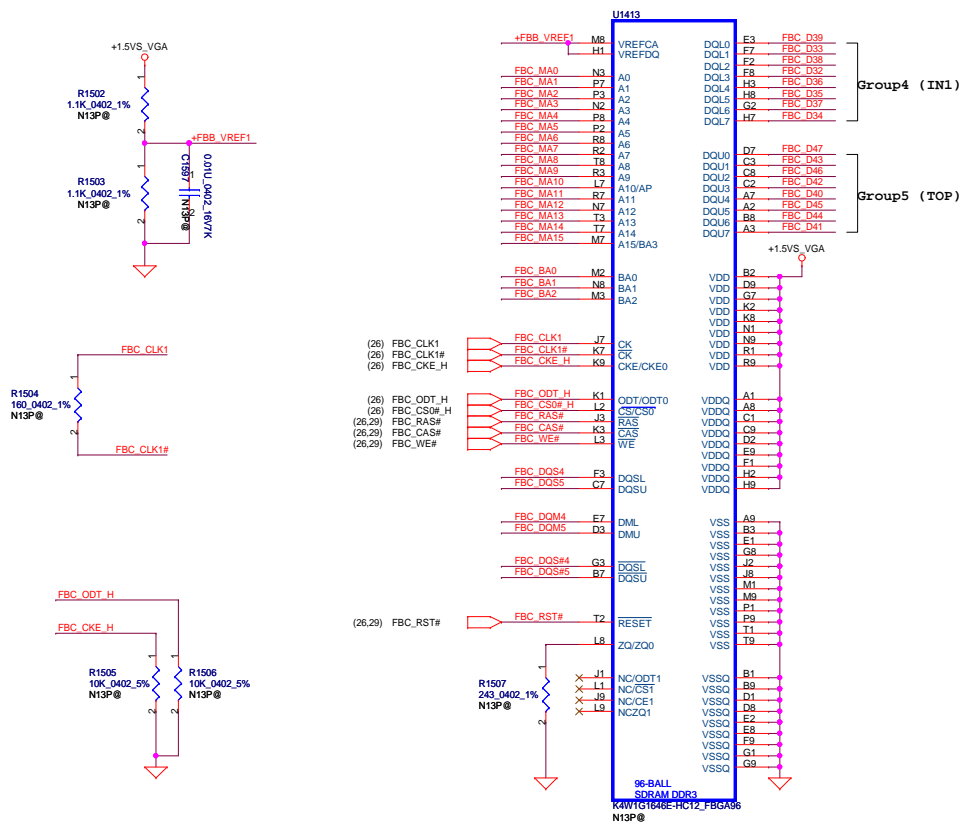
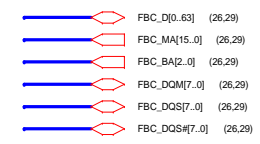
Memory Partition C - Lower 32 bits



Mode D - Mirror Mode Mapping

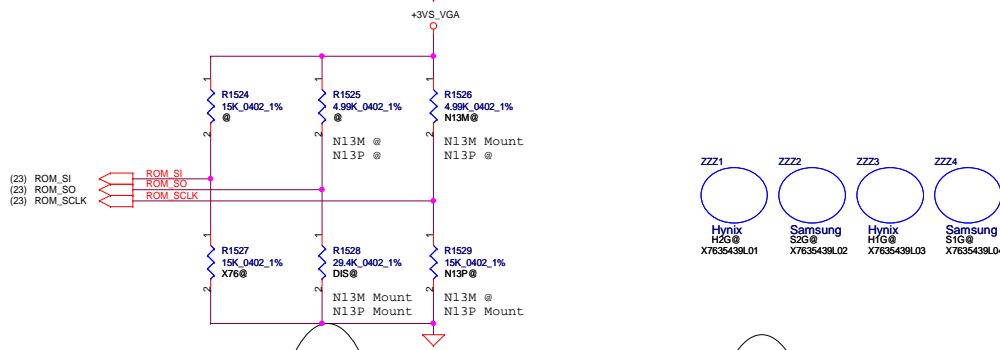
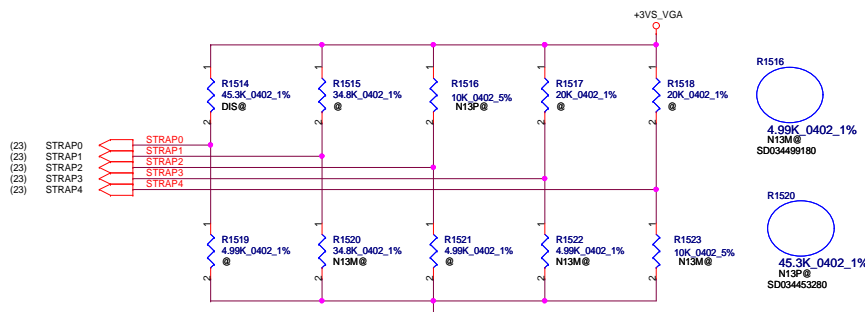
	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

Memory Partition C - Upper 32 bits



Mode D - Mirror Mode Mapping

Address	DATA Bus
0..31	32..63
FBx_CMD0	CS0#_L
FBx_CMD1	
FBx_CMD2	ODT_L
FBx_CMD3	CKE_L
FBx_CMD4	A14 A14
FBx_CMD5	RST RST
FBx_CMD6	A9 A9
FBx_CMD7	A7 A7
FBx_CMD8	A2 A2
FBx_CMD9	A0 A0
FBx_CMD10	A4 A4
FBx_CMD11	A1 A1
FBx_CMD12	BA0 BA0
FBx_CMD13	WE# WE#
FBx_CMD14	A15 A15
FBx_CMD15	CAS# CAS#
FBx_CMD16	CS0#_H
FBx_CMD17	
FBx_CMD18	ODT_H
FBx_CMD19	CKE_H
FBx_CMD20	A13 A13
FBx_CMD21	A8 A8
FBx_CMD22	A6 A6
FBx_CMD23	A11 A11
FBx_CMD24	A5 A5
FBx_CMD25	A3 A3
FBx_CMD26	BA2 BA2
FBx_CMD27	BA1 BA1
FBx_CMD28	A12 A12
FBx_CMD29	A10 A10
FBx_CMD30	RAS# RAS#



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

USER Straps	
User[3:0]	
1000-1100	Customer defined

PCIE_MAX_SPEED	
0	Limit to PCIe Gen1
1	PCIe Gen 2/3 Capable

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

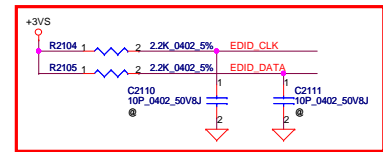
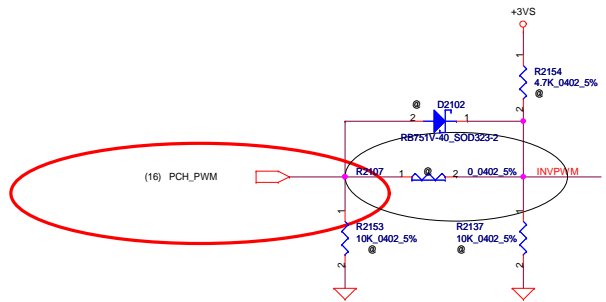
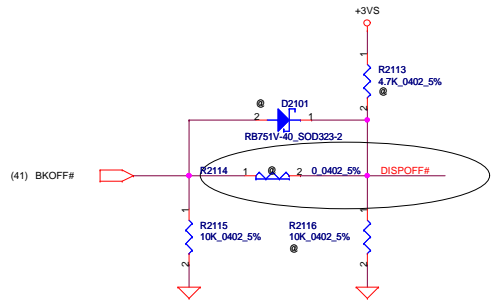
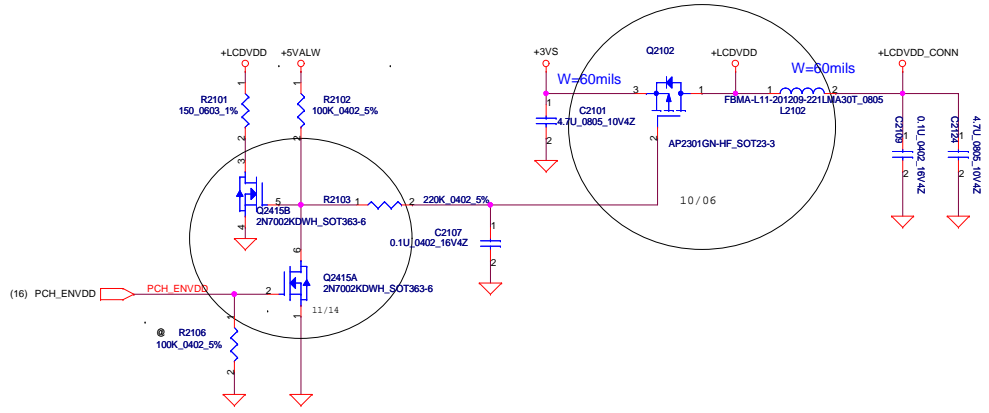
GPU	FB Memory gDDR3	ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P-GL	Samsung 900MHz K4W1G1646G-BC11	PD 10K	PD 15K	PD 20K	PU 45K	PD 45K	PU 10K	NC	NC
	64Mx16						PU 45K(ES)		
	Hynix 900MHz H5TQ1G63DFR-11C	PD 10K	PD 15K	PD 15K	PU 45K	PD 45K	PU 10K	NC	NC
	64Mx16						PU 45K(ES)		
N13M-GE1	Samsung 900MHz K4W2G1646C-HC11	PD 10K	PD 15K	PD 45K	PU 45K	PD 45K	PU 10K	NC	NC
	128Mx16						PU 45K(ES)		
	Hynix 900MHz H5TQ2G63BFR-11C	PD 10K	PD 15K	PD 35K	PU 45K	PD 45K	PU 10K	NC	NC
	128Mx16						PU 45K(ES)		

GPU	FB Memory gDDR3	ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13M-GE1	Samsung 900MHz K4W1G1646G-BC11	PD 30K	PU 5K	PD 20K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
	64Mx16								
	Hynix 900MHz H5TQ1G63DFR-11C	PD 30K	PU 5K	PD 15K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
	64Mx16								
N13M-GE1	Samsung 900MHz K4W2G1646C-HC11	PD 30K	PU 5K	PD 45K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
	128Mx16								
	Hynix 900MHz H5TQ2G63BFR-11C	PD 30K	PU 5K	PD 35K	PU 45K	PD 35K	PU 5K	PD 5K	PD 10K
	128Mx16								

9/27
from 15K to 5K

Security Classification		Compal Secret Data		Title	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	N13X-MISC	
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				LA-8133P	
				Date	Friday, January 13, 2012
				Sheet	31 of 58

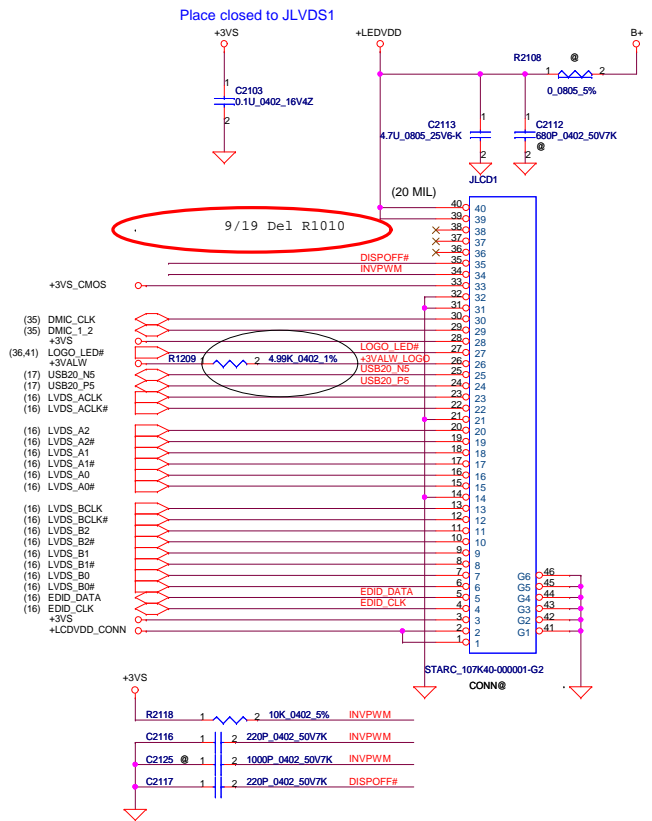
LCD POWER CIRCUIT



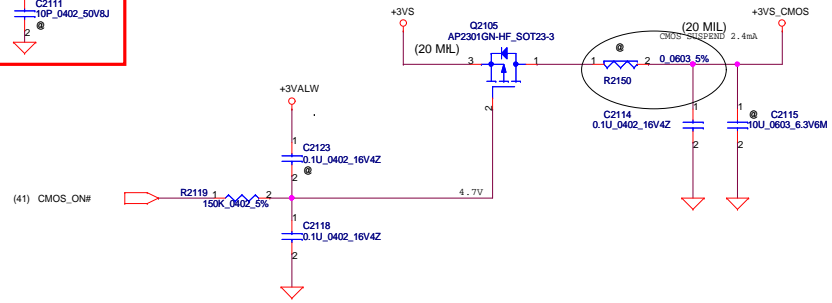
A LOGO RED LIGHT
CMOS

LCD/LED PANEL Conn.

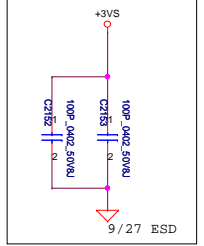
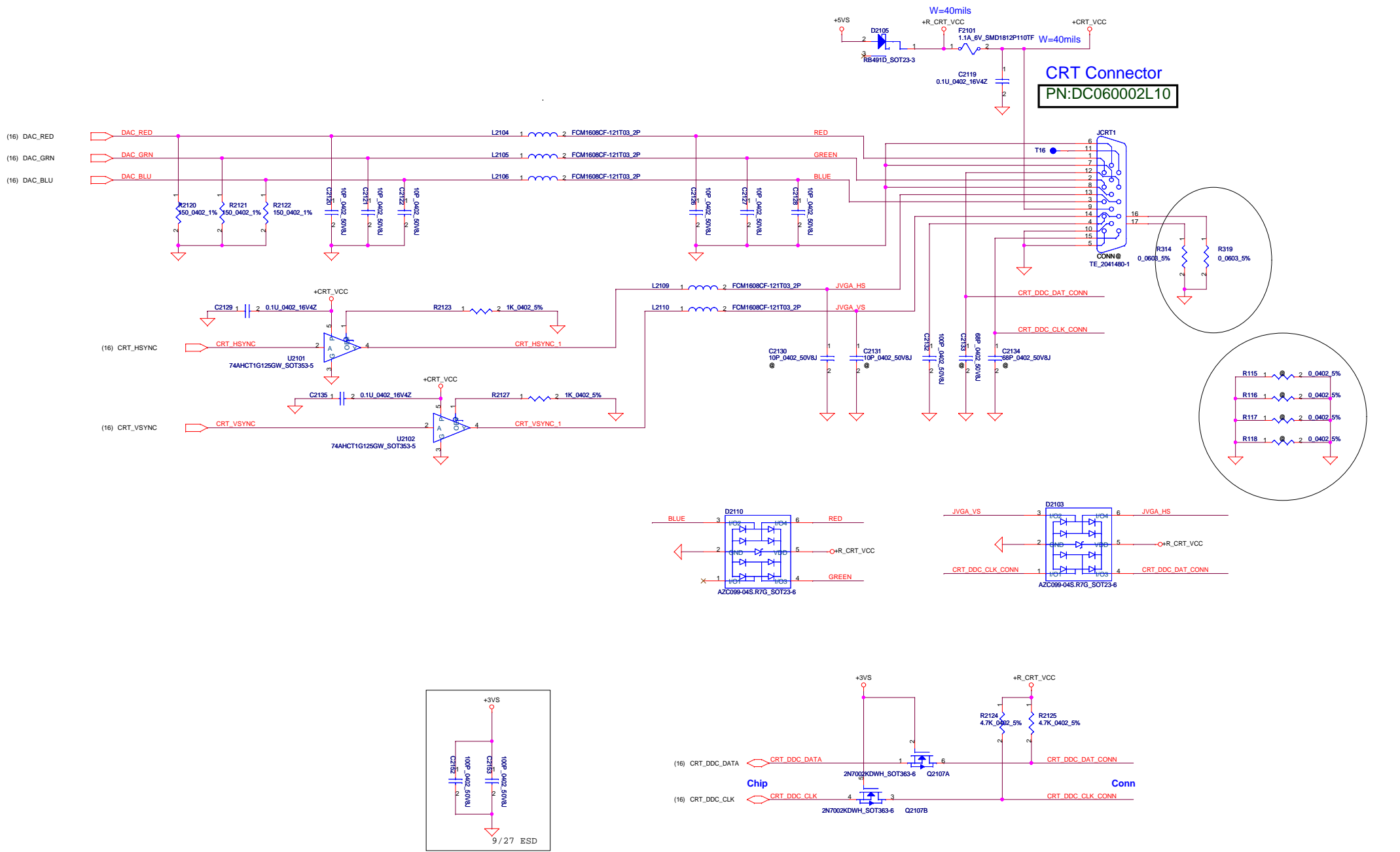
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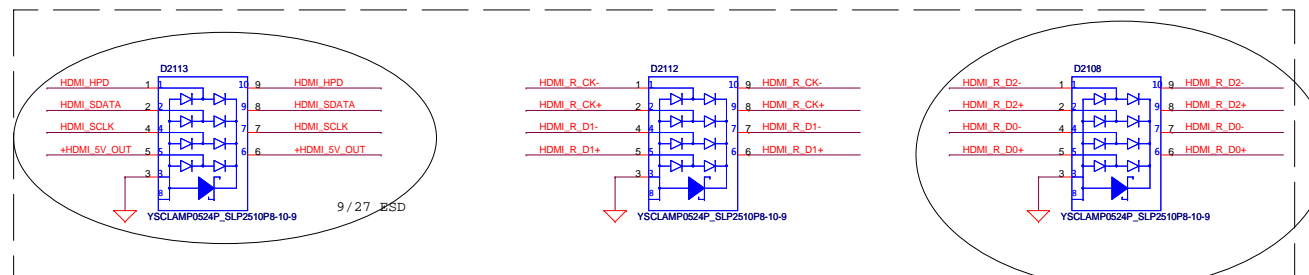
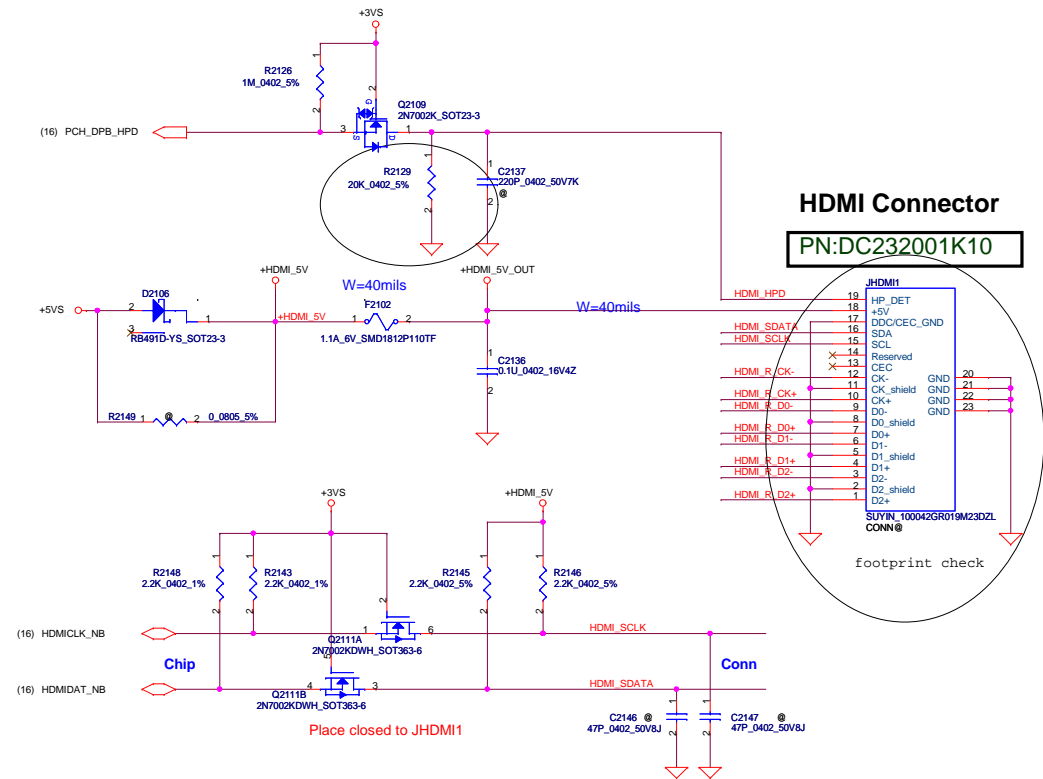
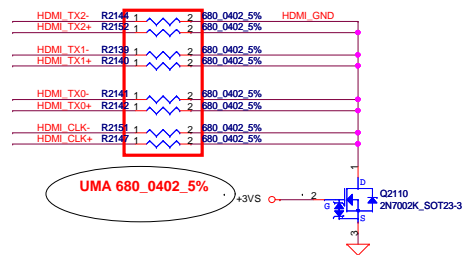
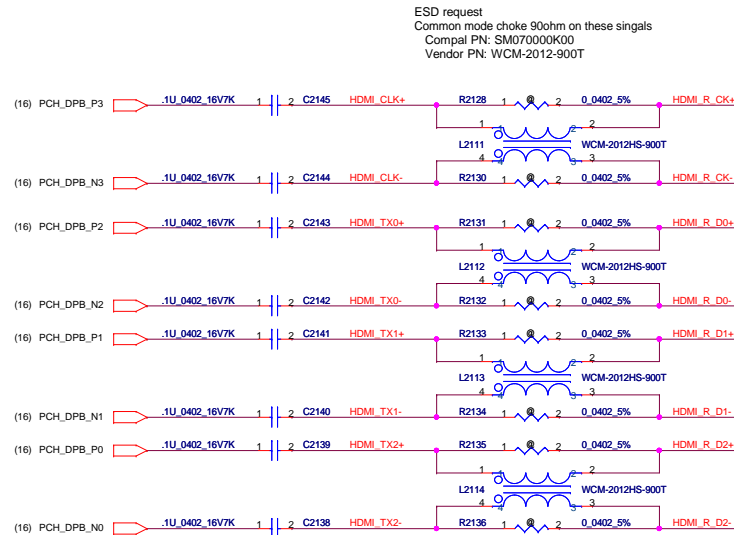
CMOS Camera Conn



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				Custom	1.0
				LA-8133P	
				Date	Friday, January 13, 2012
				Sheet	32 of 58

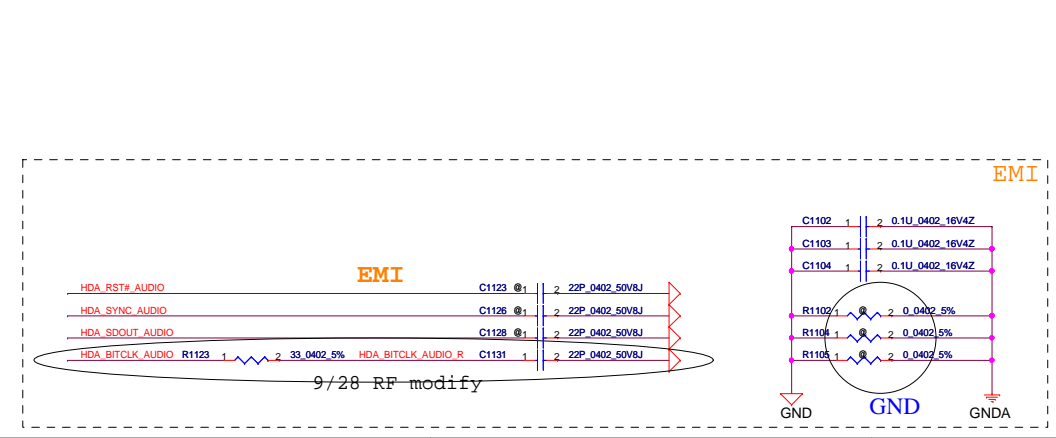
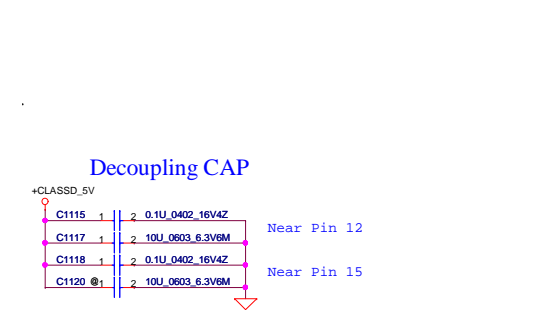
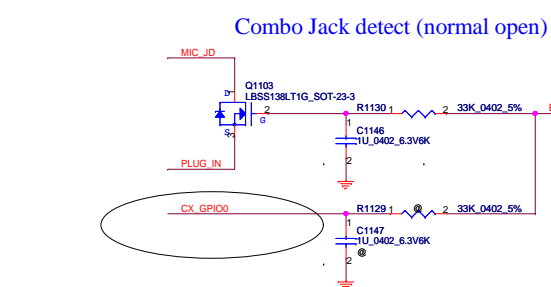
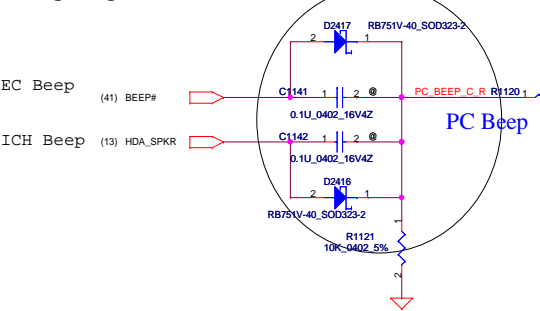


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				Sheet		33 of 58	
				Rev		1.0	
				Date		LA-8133P	



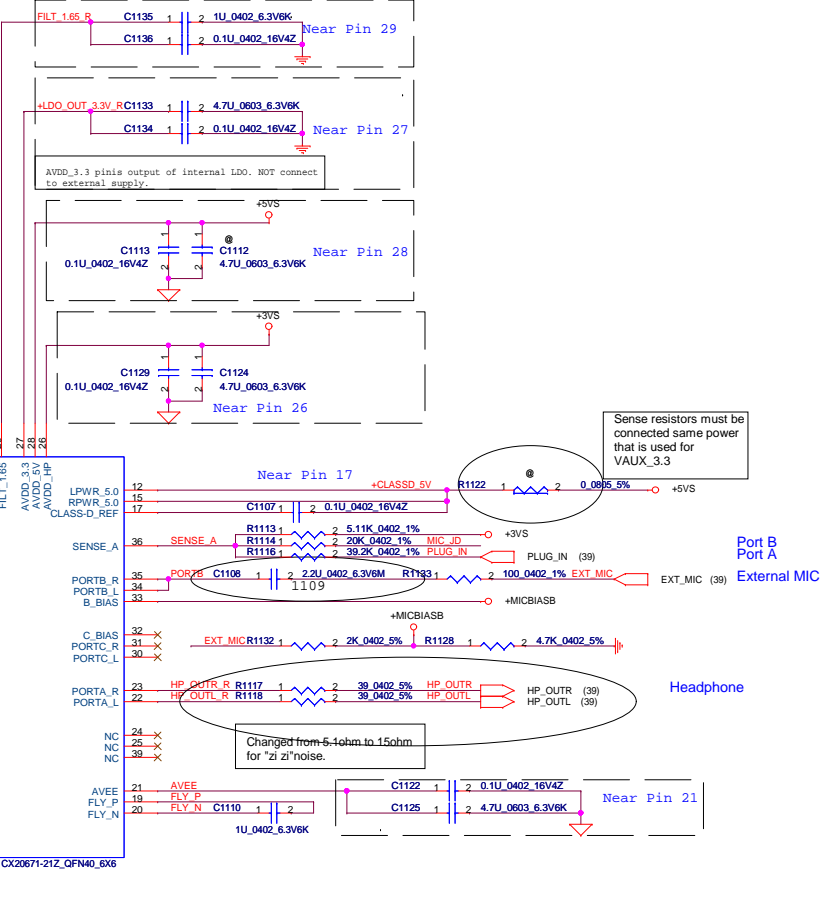
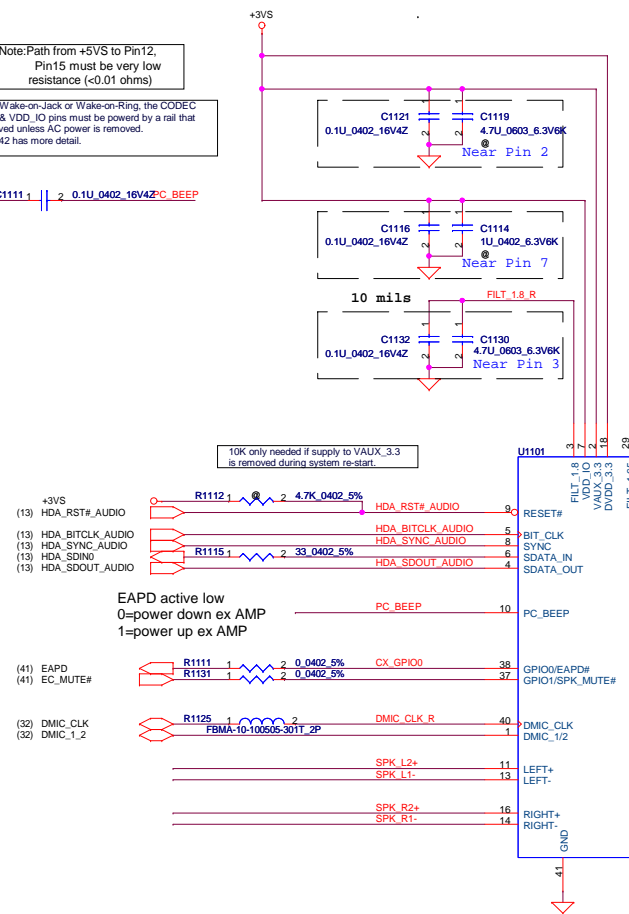
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Issued Date	2011/07/12	Deciphered Date	2012/07/01	HDMI Connector	
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Date: Friday, January 13, 2012				Sheet 34	of 58

CX20671
 High Definition Audio Codec SoC
 With Integrated Class-D Stereo
 Amplifier.
 An integrated 5 V to 3.3 V Low-dropout
 voltage regulator (LDO).
 An integrated 3.3 V to 1.8V Low-dropout
 voltage regulator (LDO).



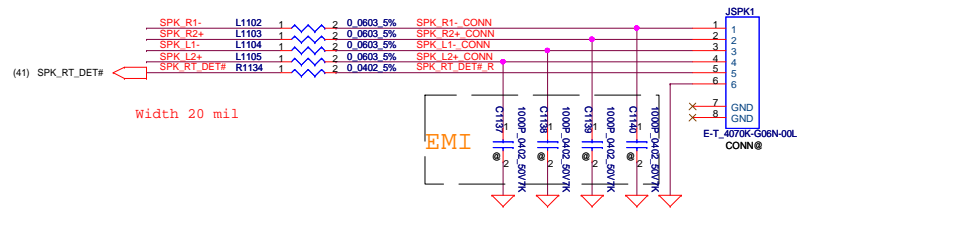
Layout Note: Path from +5VS to Pin12,
 Pin15 must be very low
 resistance (<0.01 ohms)

To support Wake-on-Jack or Wake-on-Ring, the CODEC
 VAUX_3.3 & VDD_IO pins must be powered by a rail that
 is not removed unless AC power is removed.
 *DSH page42 has more detail.



EMC request
 Bead 120ohm on these singals
 Compal PN: SM010016720
 Vendor PN: FBMA-L11-160808-121LMT
 Rdc < 0.05 ohms
 Rated Current > 2A

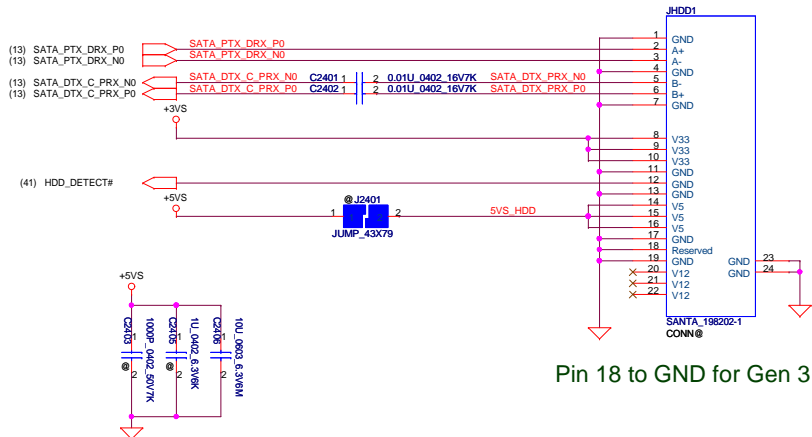
Internal Speaker
 SP02000N010
 SP02000SM10



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Issued Date	2011/07/12	Deciphered Date	2012/07/01	HD Audio Codec CX20671	
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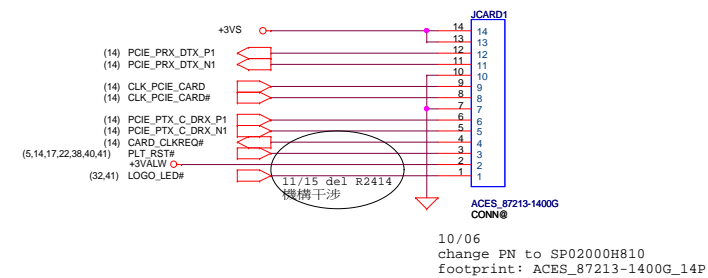
SATA HDD CONN.

PN:DC010004C00



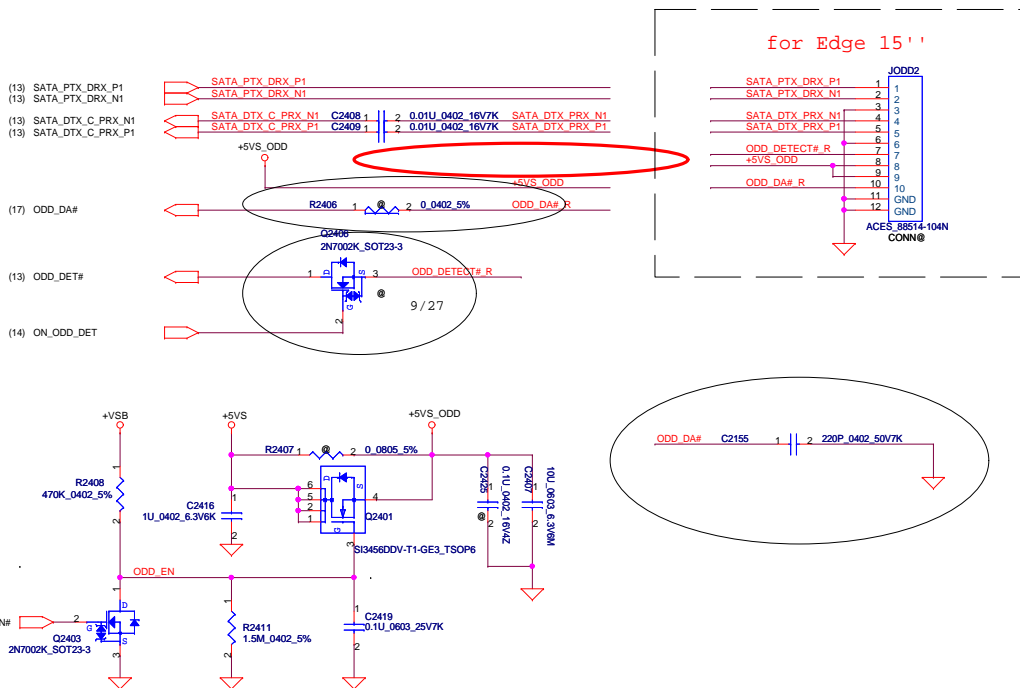
Card Reader CONN.

PN:SP01001BF00

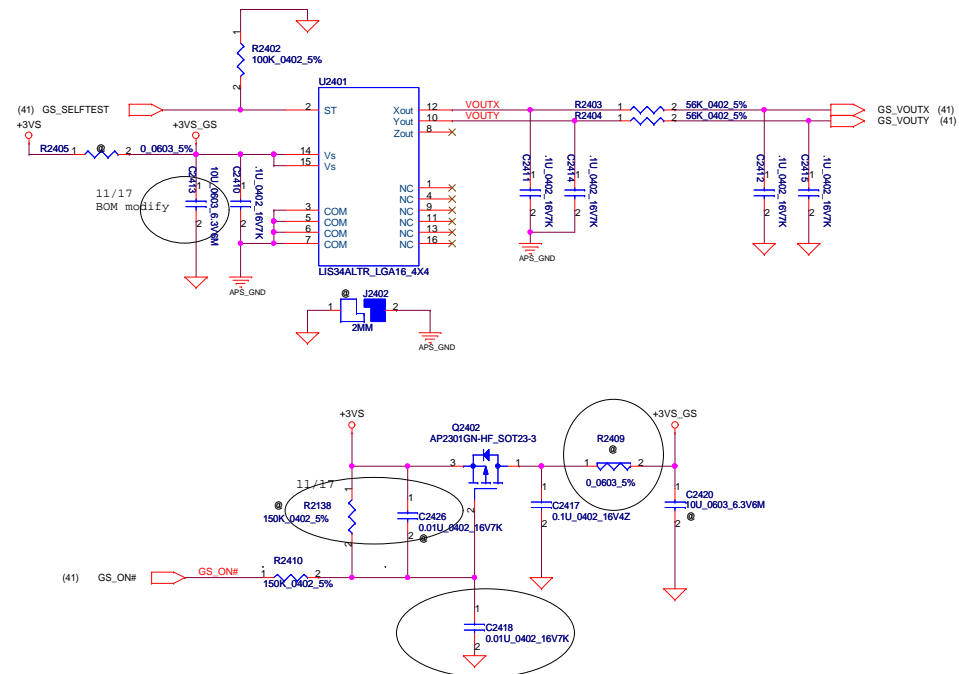


SATA ODD CONN.

PN:SP01000TU10

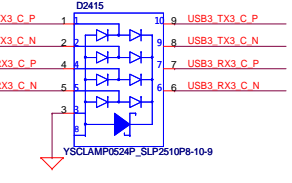
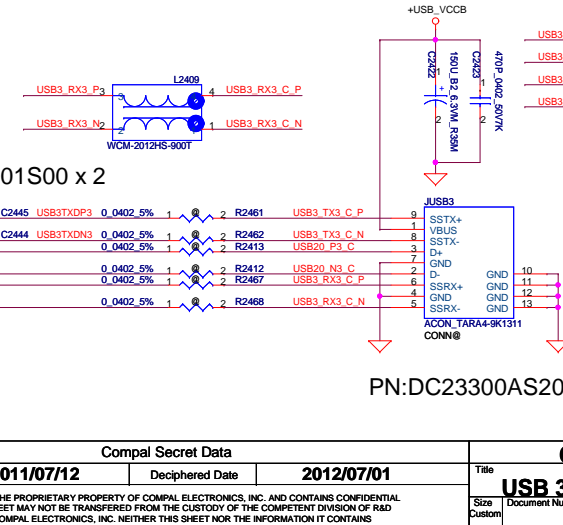
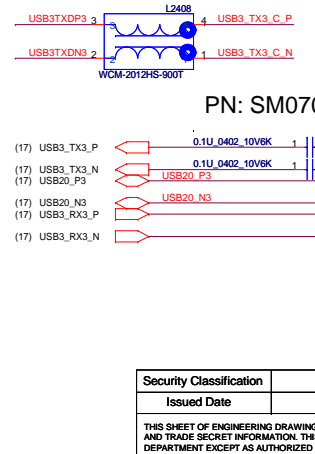
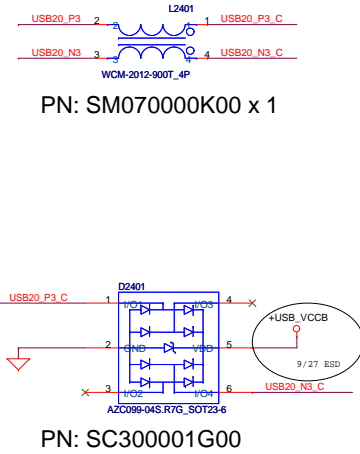
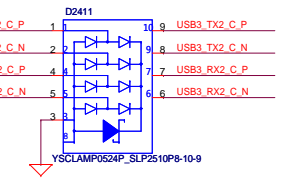
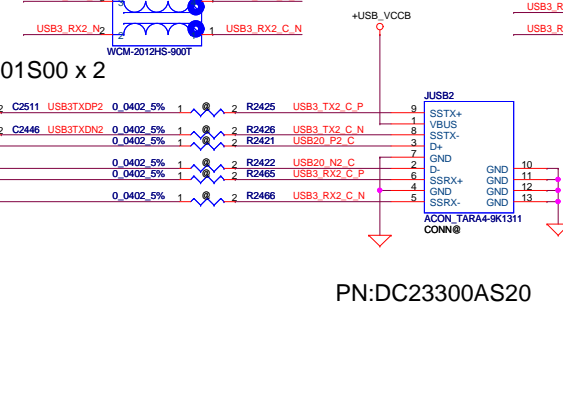
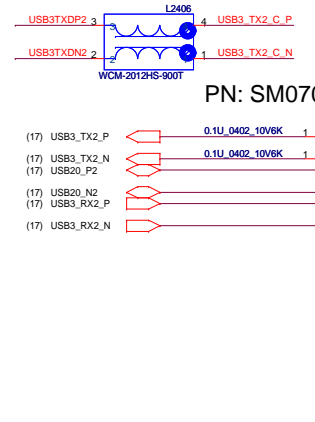
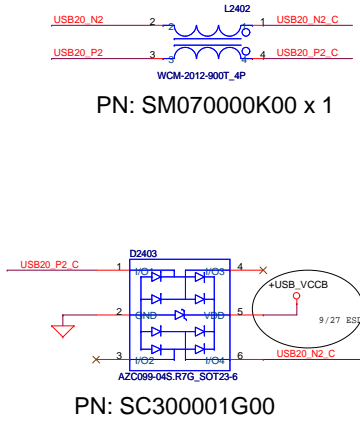
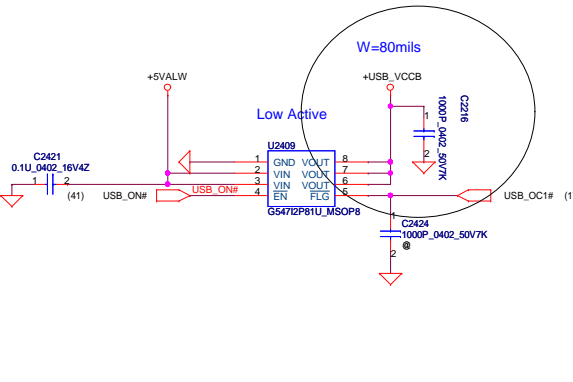
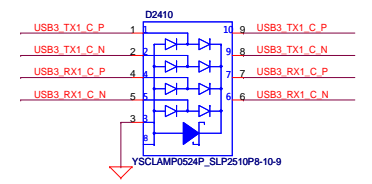
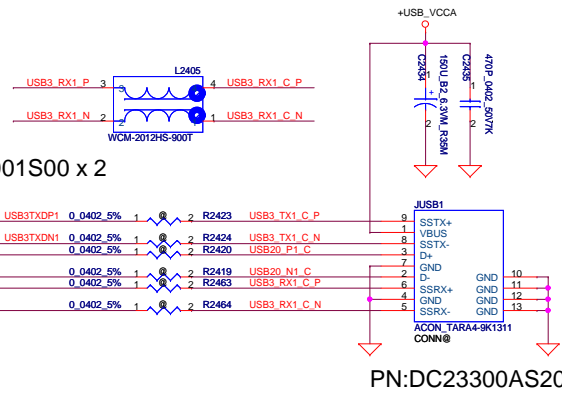
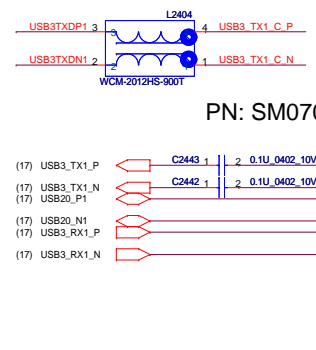
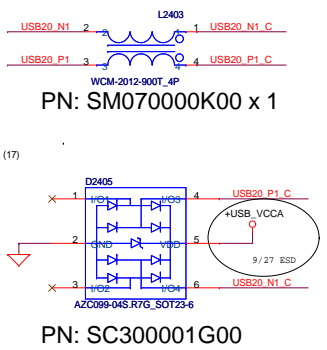
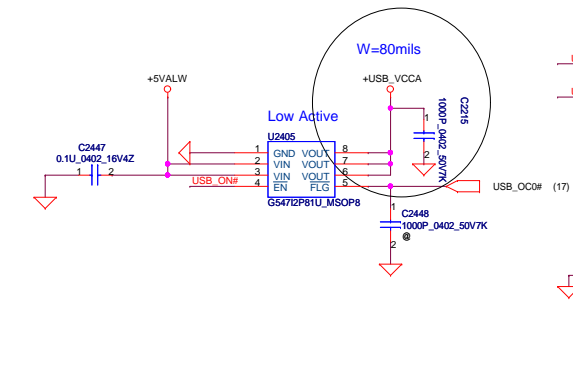


APS G-Sensor



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Date	Friday, January 13, 2012	Sheet	36	of	58	Rev 1.0

USB 3.0 Conn.

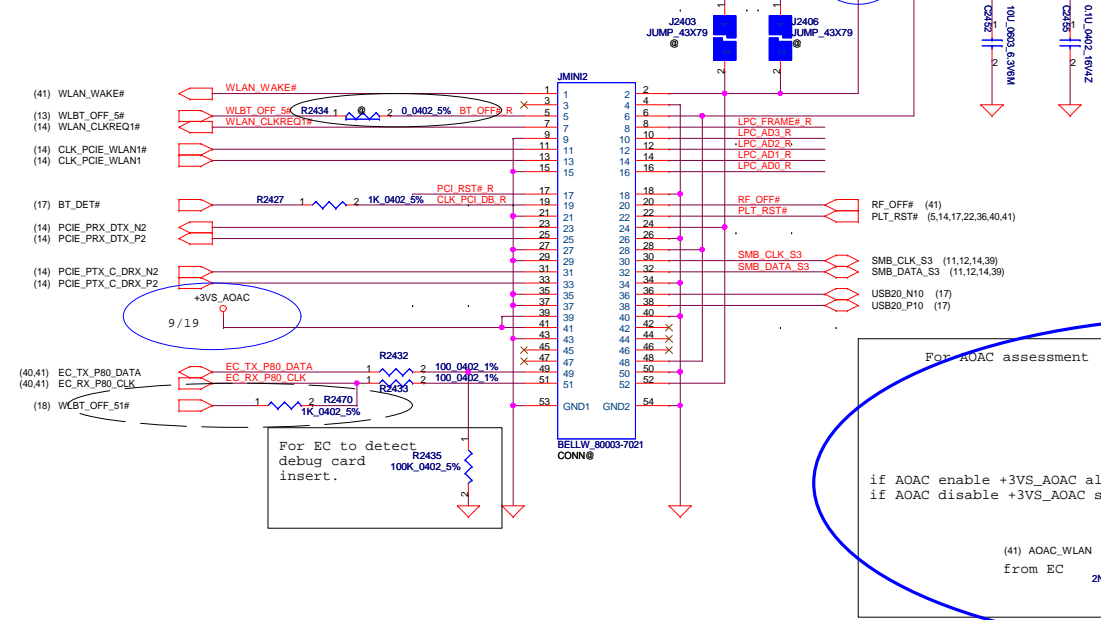


Security Classification		Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	USB 3.0 Connector		Rev 1.0	
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				Date		LA-8133P	
				Date		Friday, January 13, 2012	
				Sheet		37 of 58	

Mini-Express Card for WLAN/WiMAX(Half)

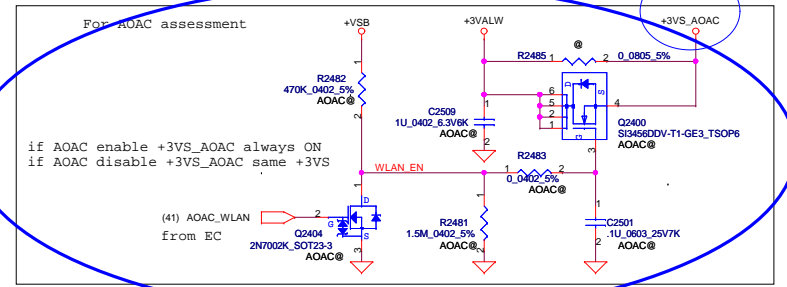
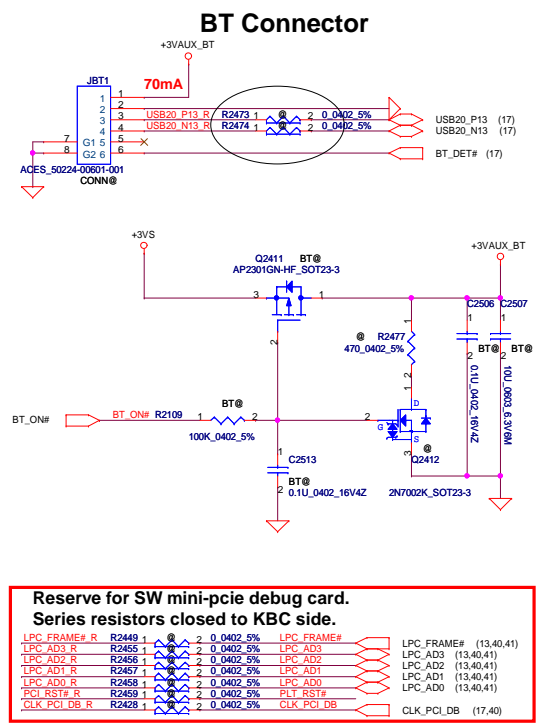
Mini-Express Card(WLAN/WiMAX)

PN:SP07000JP00



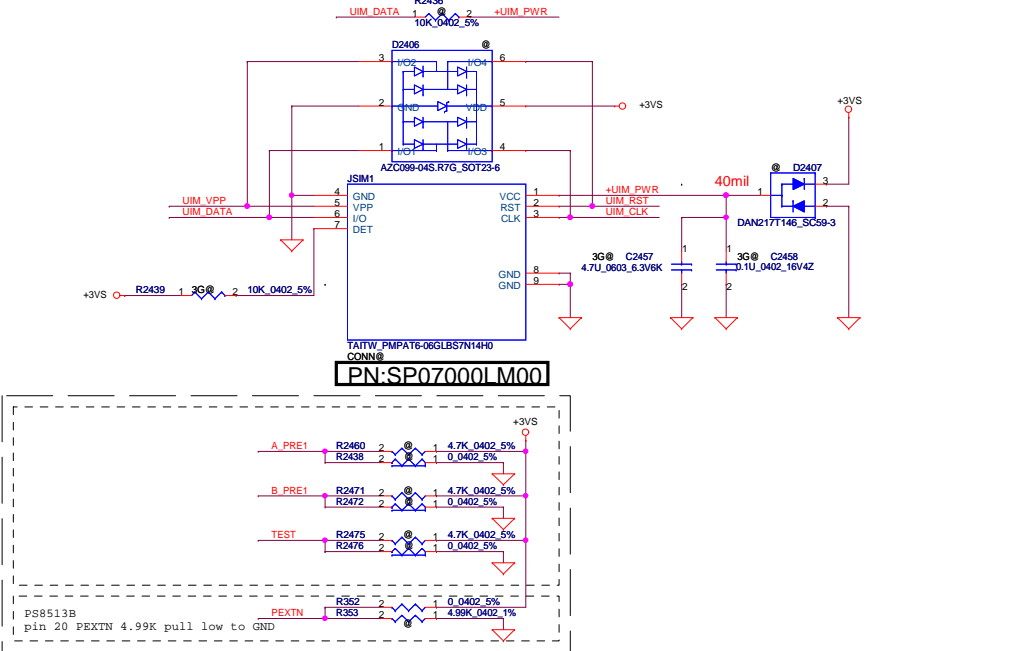
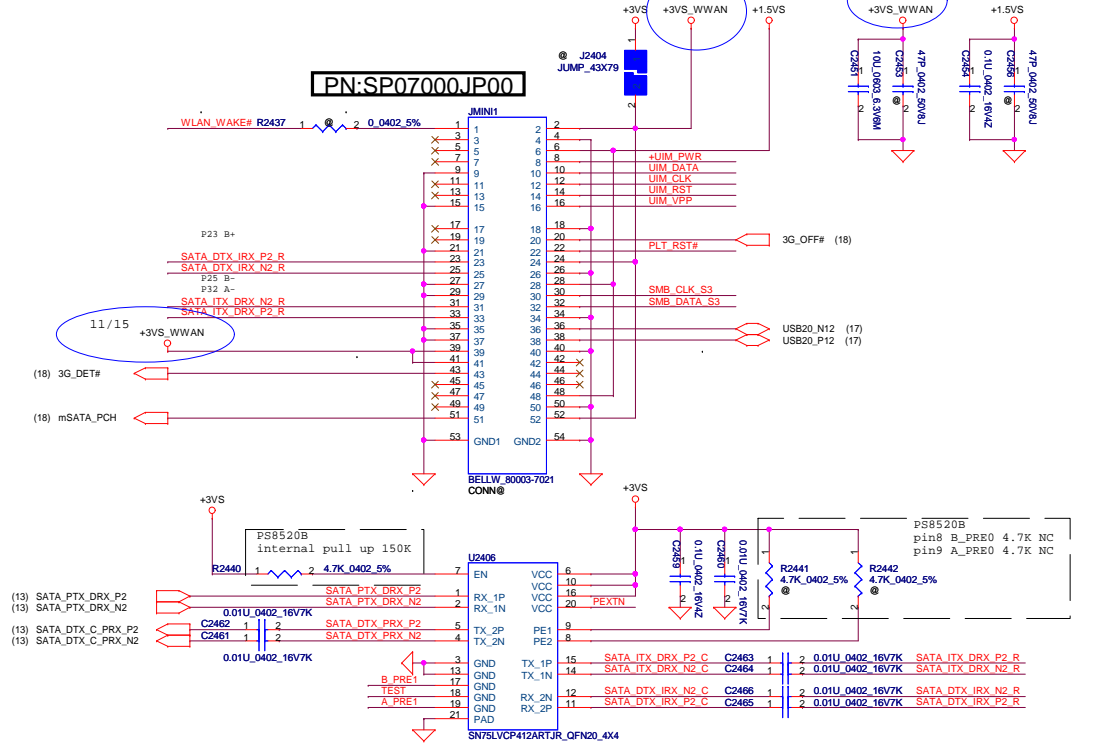
Mini Card Power Rating

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



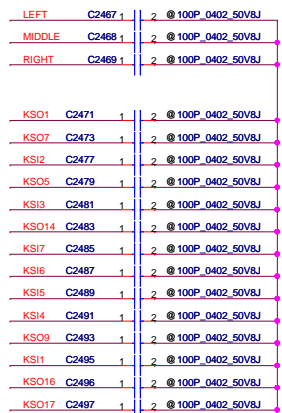
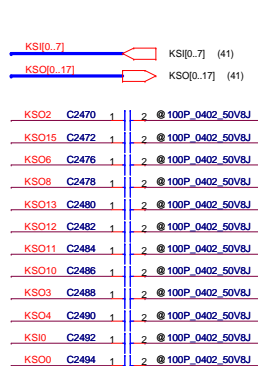
Mini-Express Card for WWAN/mSATA(Full)

PN:SP07000JP00



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Issued Date	2011/07/12	Deciphered Date	2012/07/01	WLAN and WWAN/mSATA	
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Size	Custom	Document Number	LA-8133P		Rev
Date	Friday, January 13, 2012	Sheet	38	of	58

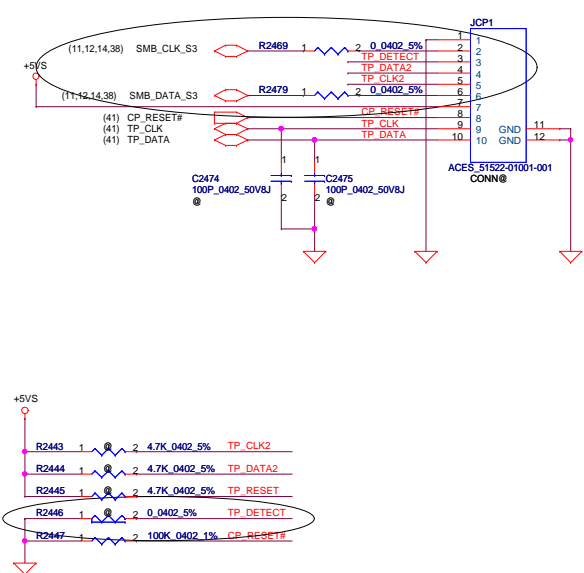
INT_KBD Conn.



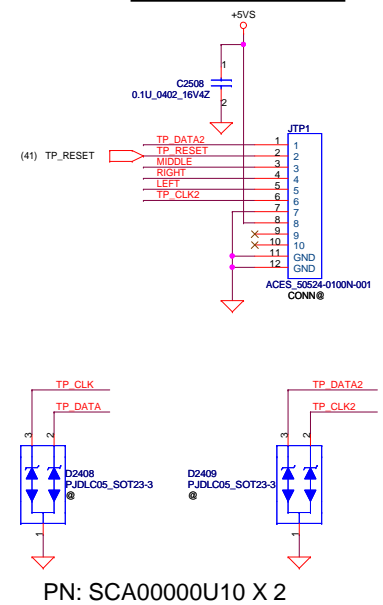
CONN PIN define need double check

Reserve for ESD.

Click pad PN:SP01001AL00

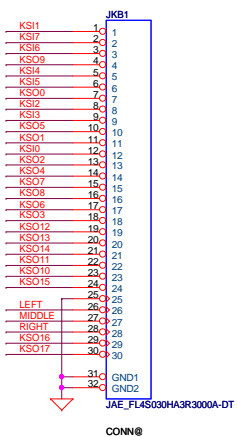


Track point PN:SP01001CH00



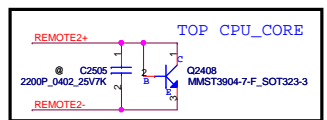
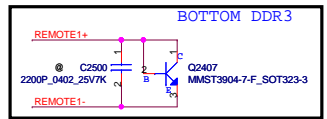
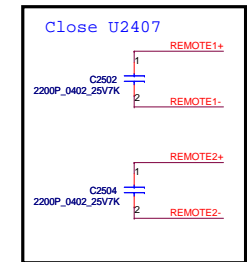
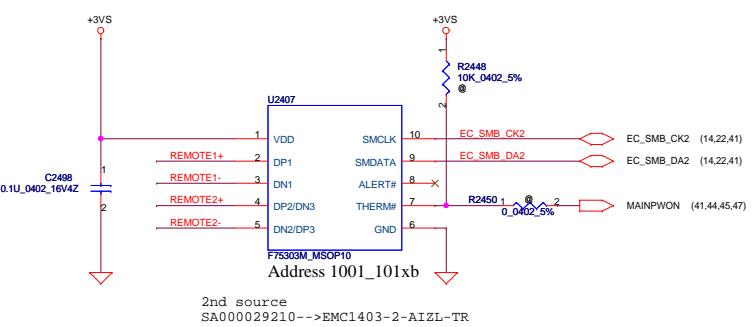
PN: SCA00000U10 X 2

PN:SP01000YH00



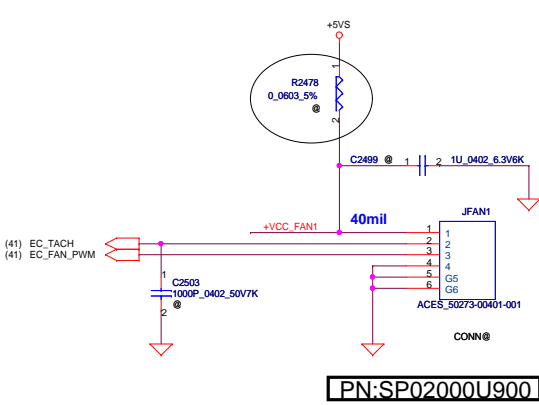
M1(Left BUTTON)
M2(Center BUTTON)
M3(Right BUTTON)

Fintek thermal sensor placed near by TOP DDR3



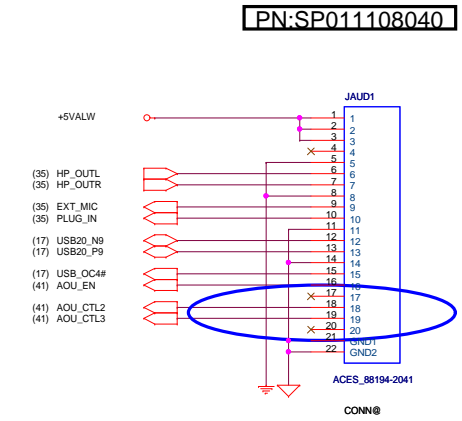
REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN CONN.



PN:SP02000U900

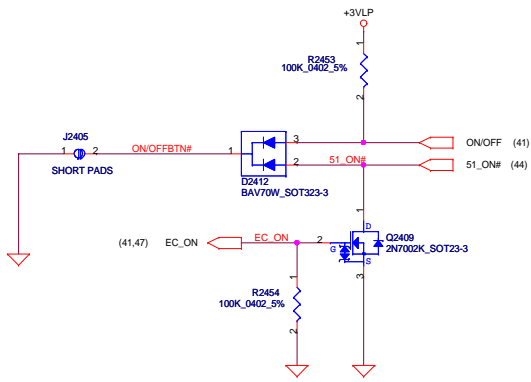
Audio Board



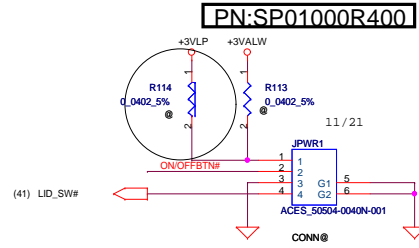
PN:SP011108040

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Issued Date	2011/07/12	Deciphered Date	2012/07/01	KB/TP/Thermal Sensor/Audio	
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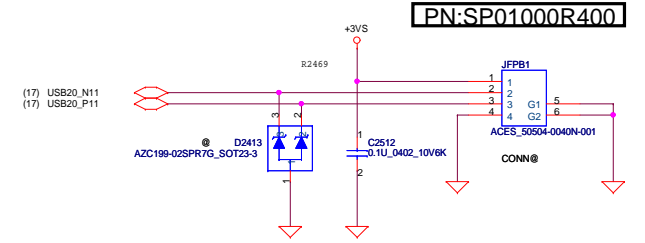
Power Button



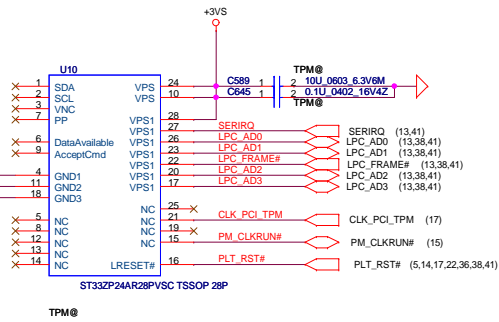
Power Button CONN.



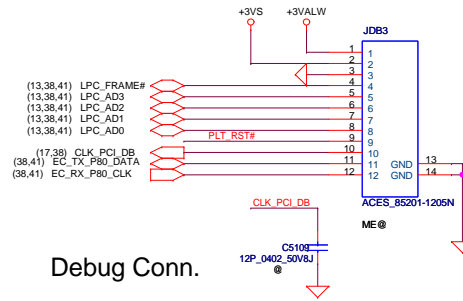
Finger Print Board



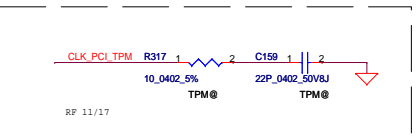
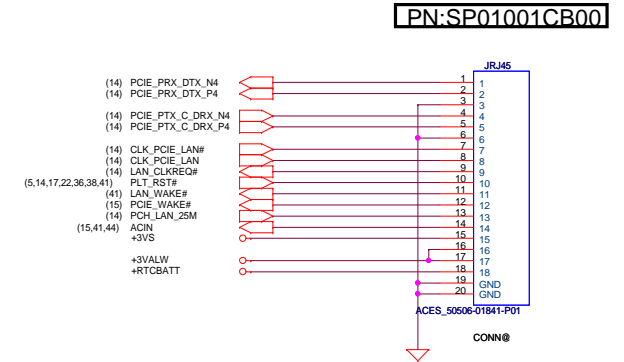
TPM



Debug Conn.

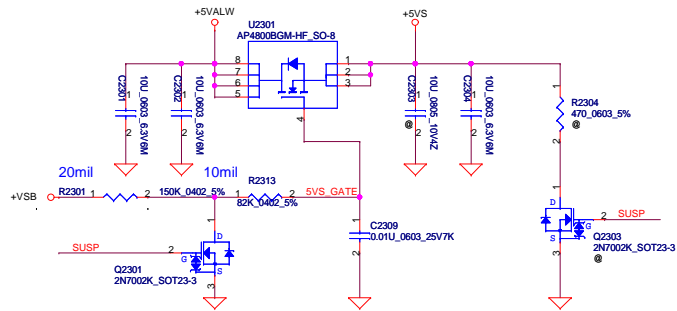


RJ45 Board

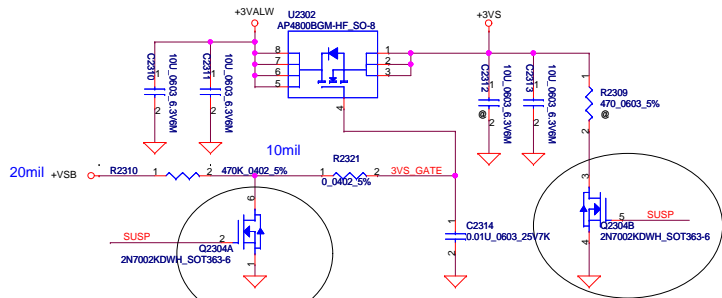


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				Sheet		40 of 58	

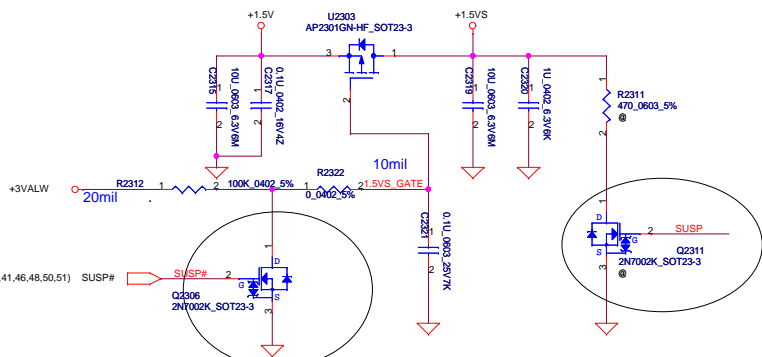
+5VALW TO +5VS



+3VALW TO +3VS

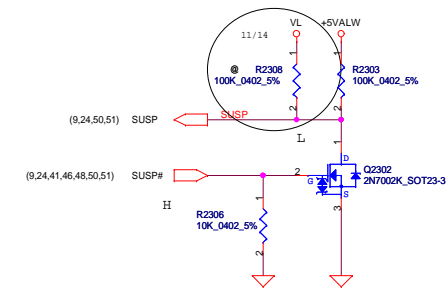
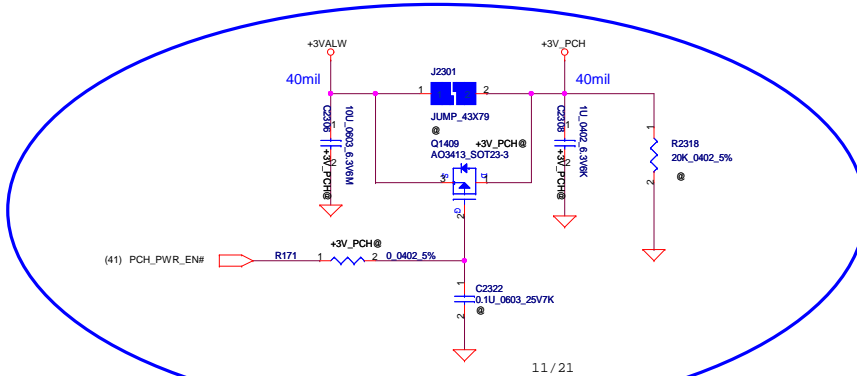


+1.5V to +1.5VS

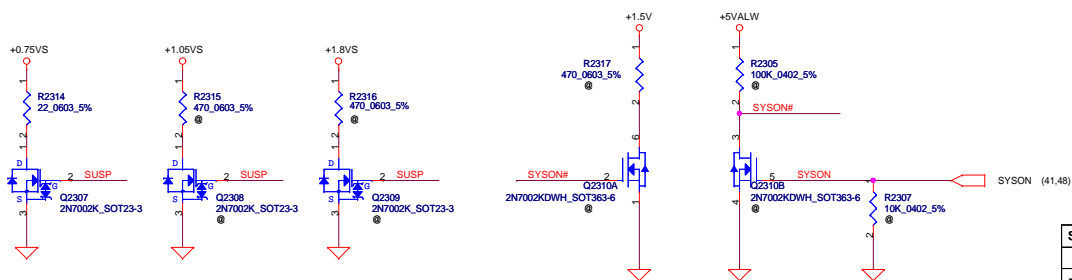
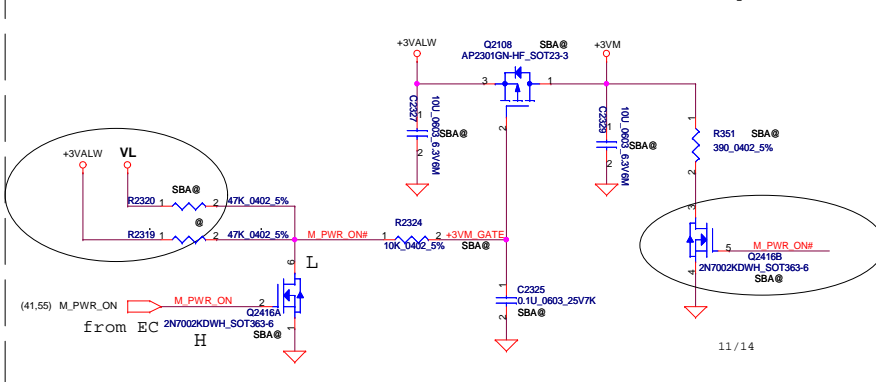


+3VALW TO +3VALW(PCH AUX Power)

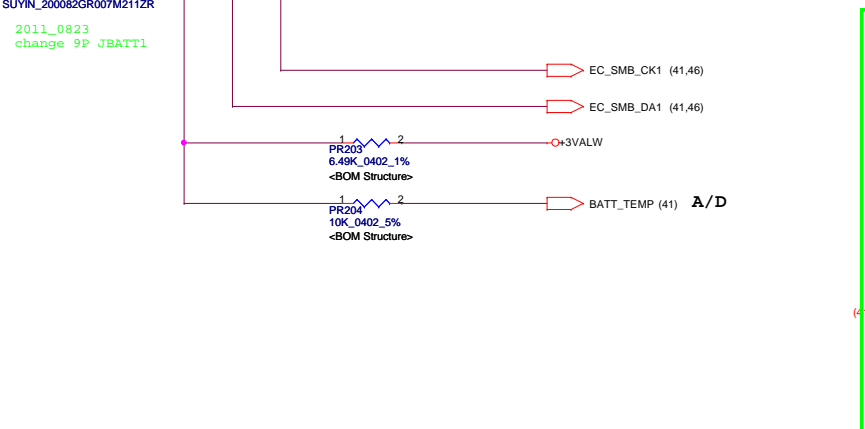
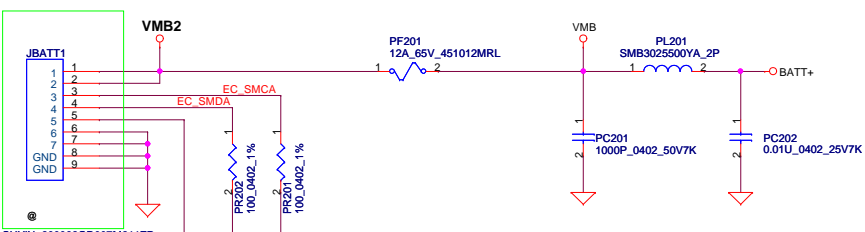
Short J2301 for PCH VCCSUS3.3



FOR SBA Function POWER(always mount)



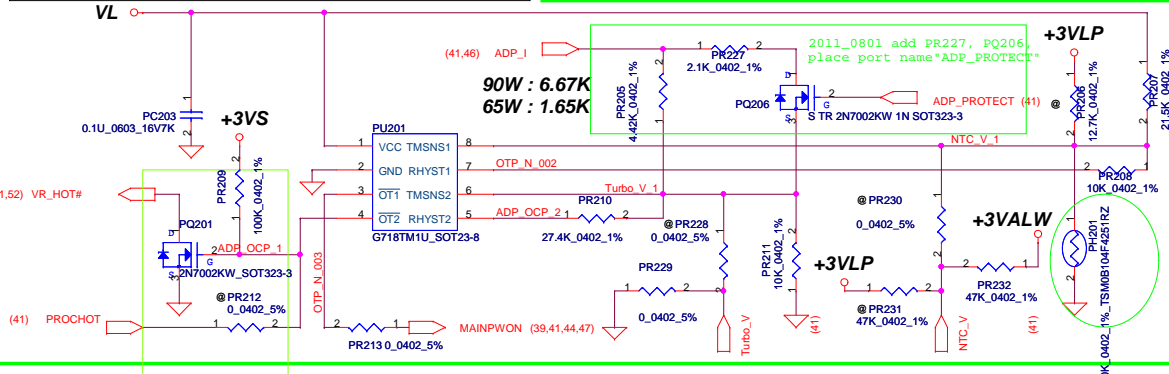
Security Classification		Compal Secret Data		Title	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	DC Interface	
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				Custom	1.0
				LA-8133P	
				Date	Friday, January 13, 2012
				Sheet	42 of 58



2011_1128
Add OTP
PR212 and PR206 unmount

PH1 under CPU bottom side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

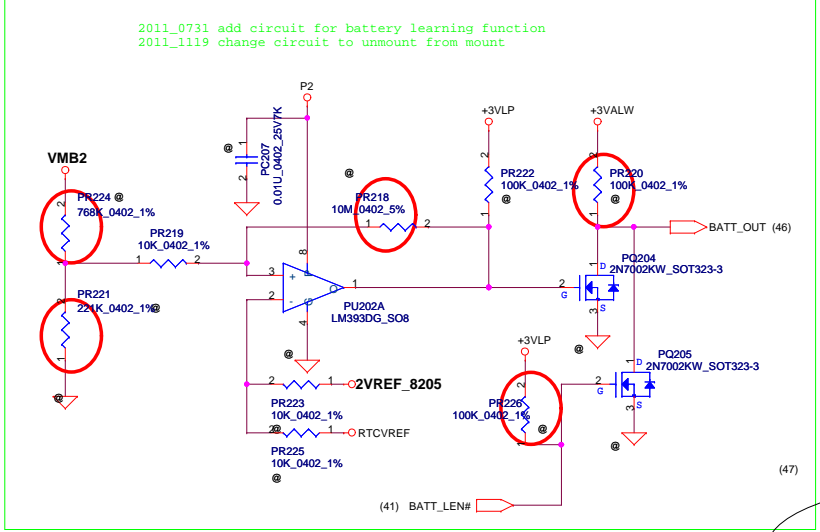
For KB930 --> Keep PU201 circuit
(Vth = 1.25V)
For KB9012 (Red square) --> Remove PU201 circuit, but keep PR206
PH201, PR205, PR211, PQ201, PR208, PR212



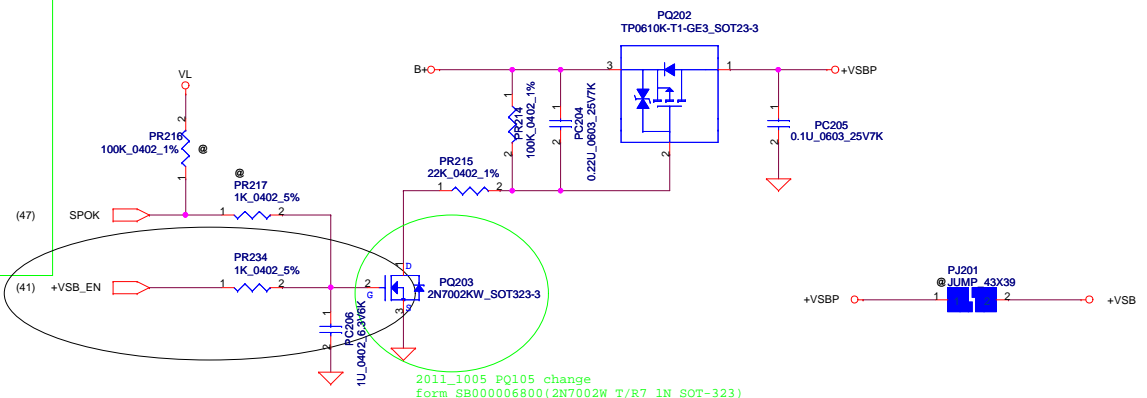
2011_1119
Change PQ201, PR209, PR212 to mount from unmount

2011_0808
PR227, PQ206
change place

2011_1005
PH201 form SL200000V00
100K +-1% NCP15WF104F03RC 0402
change to SL200000U00
100K +-1% TSM0B104F4251RZ 0402



2011_0731 add circuit for battery learning function
2011_1119 change circuit to unmount from mount

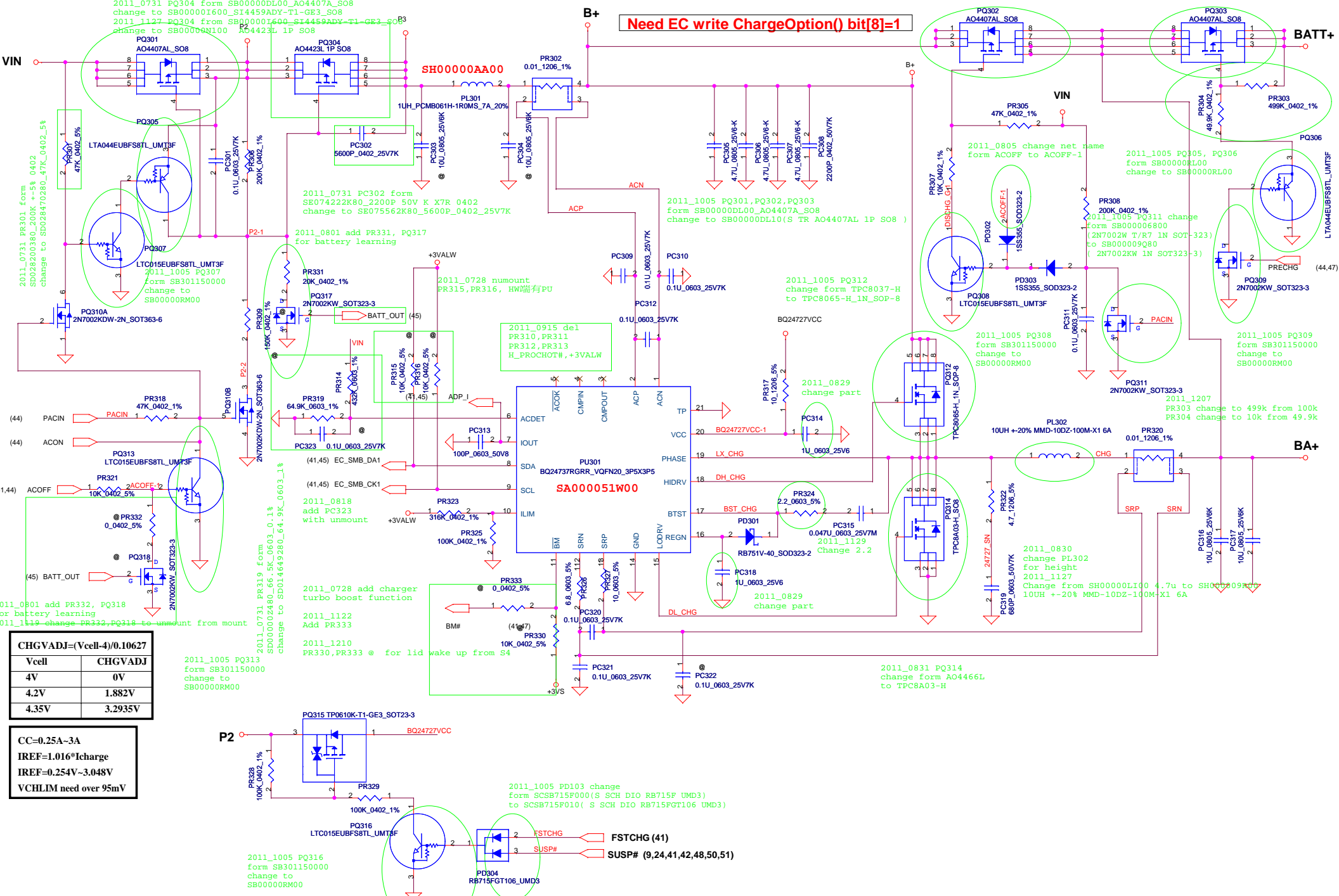


2011_1005 PQ105 change
form SB000006800(2N7002W T/R/ 1N SOT-323)
to SB000009Q80(2N7002KW 1N SOT323-3)

Security Classification	Compal Secret Data	
Issued Date	2011/07/12	Deciphered Date
		2012/07/01

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Compal Electronics, Inc.		
PWR-BATTERY CONN/OTP		
Title	Document Number	Rev
	LA-8133P	0.4
Date:	Friday, January 13, 2012	Sheet 45 of 58



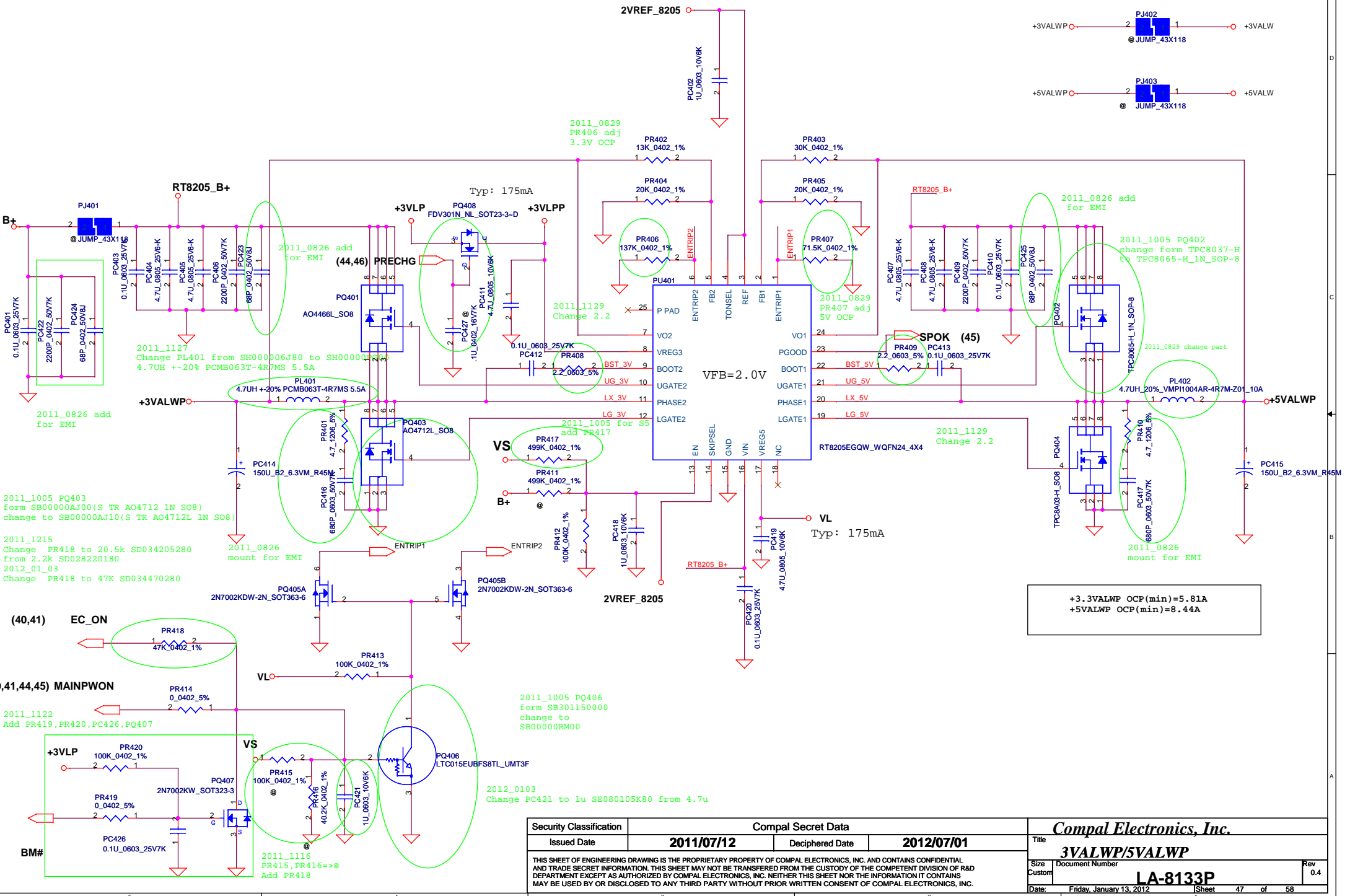
Need EC write ChargeOption() bit[8]=1

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A-3A
IREF=1.016*Icharge
IREF=0.254V-3.048V
VCHLIM need over 95mV

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title
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Date:	Friday, January 13, 2012	Sheet	46	of 58

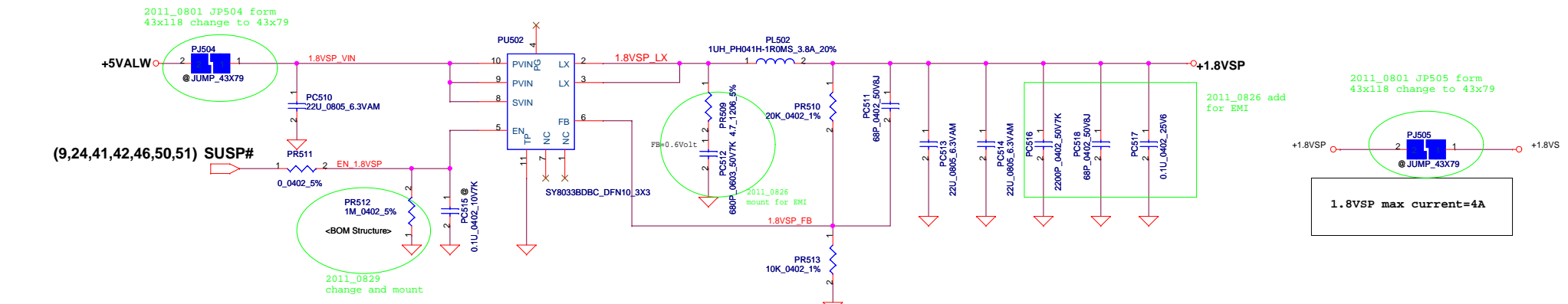
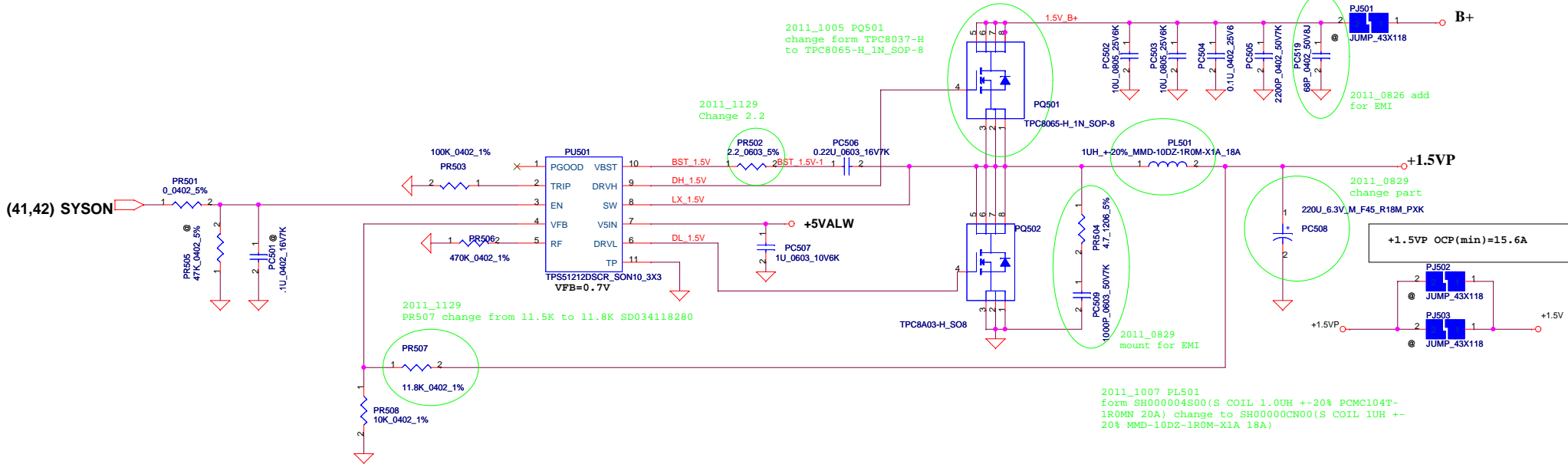
Note:
 Use TPS51125 IC can remove RTC referenece LDO
 Use TPS51427 IC must keep RTC referenece LDO



+3.3VALWP OCP (min)=5.81A
 +5VALWP OCP (min)=8.44A

Security Classification		Compal Secret Data	
Issued Date	2011/07/12	Deciphered Date	2012/07/01
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Compal Electronics, Inc.			
Title	3VALWP/5VALWP		
Size	Document Number	Rev	
Custom	LA-8133P	0.4	
Date:	Friday, January 13, 2012	Sheet	47 of 58

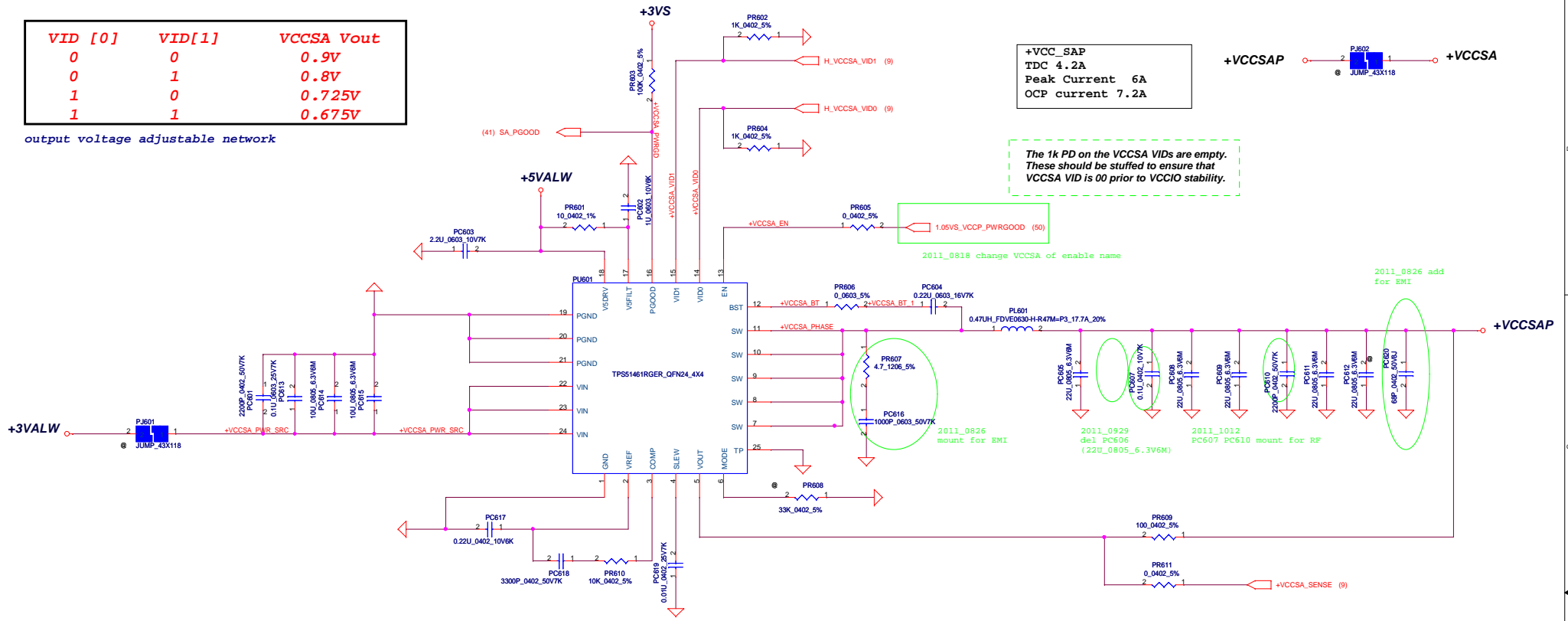


Security Classification	Compal Secret Data	
Issued Date	2011/07/12	Deciphered Date
		2012/07/01
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Compal Electronics, Inc.		
Title	PWR-+1.5V/+1.8VSP	
Size	Document Number	Rev
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VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network



+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

+VCCSAP JUMP_43X118 +VCCSA

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

2011_0818 change VCCSA of enable name

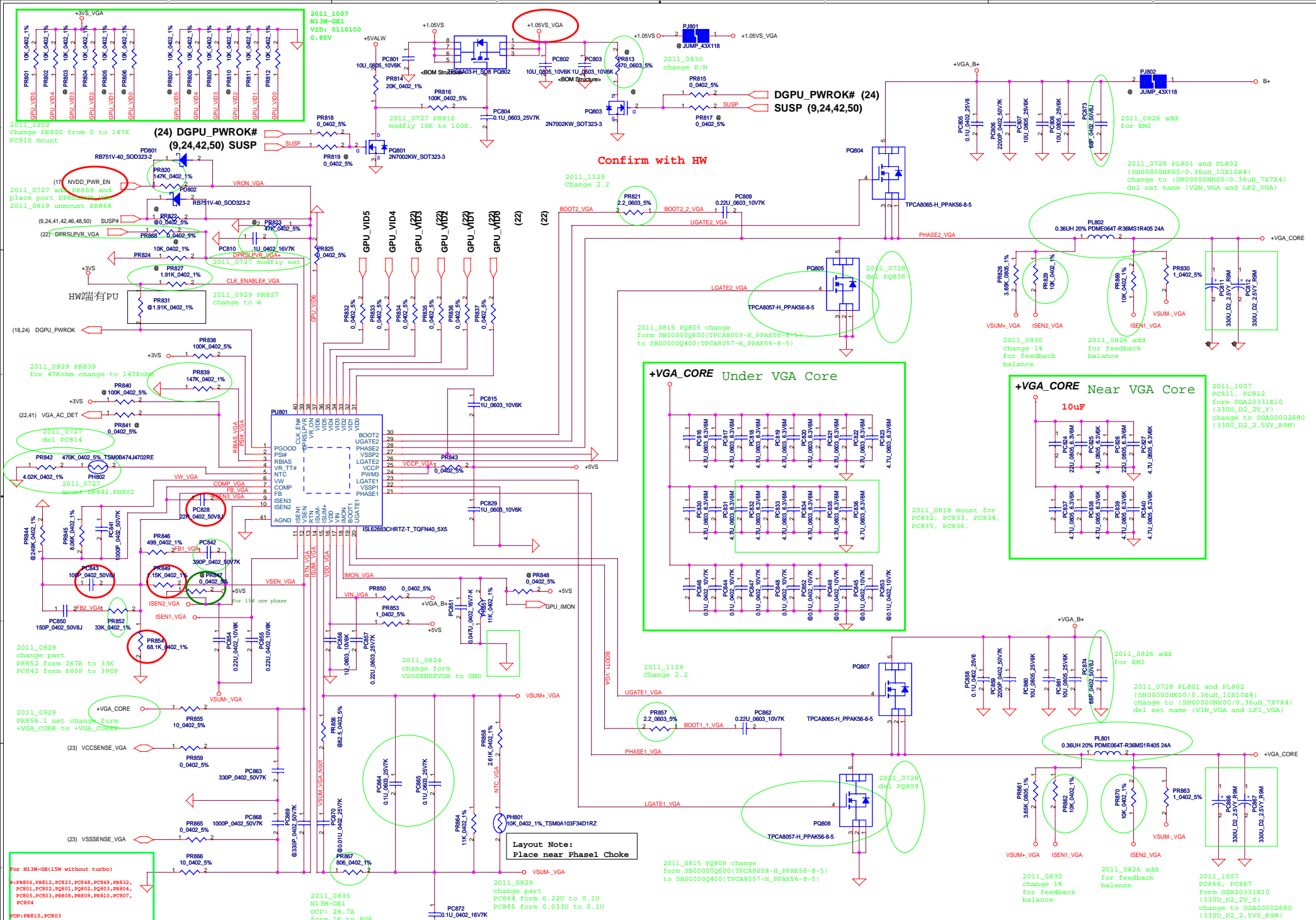
2011_0826 add for EMI

2011_0826 mount for EMI

2011_0929 del PC606 (220_0805_6.3V6M)

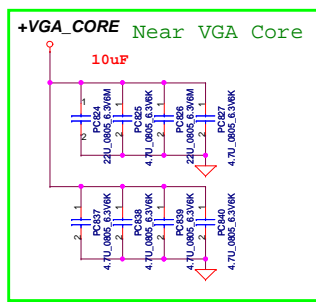
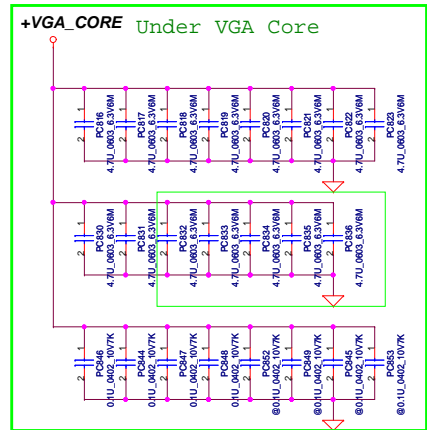
2011_1012 PC607 PC610 mount for RF

2011_0801 del +V1.05S_VCCPP circuit



(24) DGPU_PWROK# (9,24,42,50) SUSP

Confirm with HW



Layout Note:
Place near Phasel Choke

For N13M-G1E(15W without turbo)
 PR816->120K(SD034120380)
 PR820->1.69K(SD00002B80)
 PR822->22K(SD034220280)
 PR837->86K(SD03486080)
 PC858->0.1uF(SD026104M80)
 PC859->0.069uF(SD026683880)
 PR850->22.1K(SD034221280)

POP: PR815, PC803
 PR816->120K(SD034120380)
 PR820->1.69K(SD00002B80)
 PR822->22K(SD034220280)
 PR837->86K(SD03486080)
 PC858->0.1uF(SD026104M80)
 PC859->0.069uF(SD026683880)
 PR850->22.1K(SD034221280)

Security Classification		Compal Secret Data	
Issued Date	2011/07/12	Deciphered Date	2012/07/01

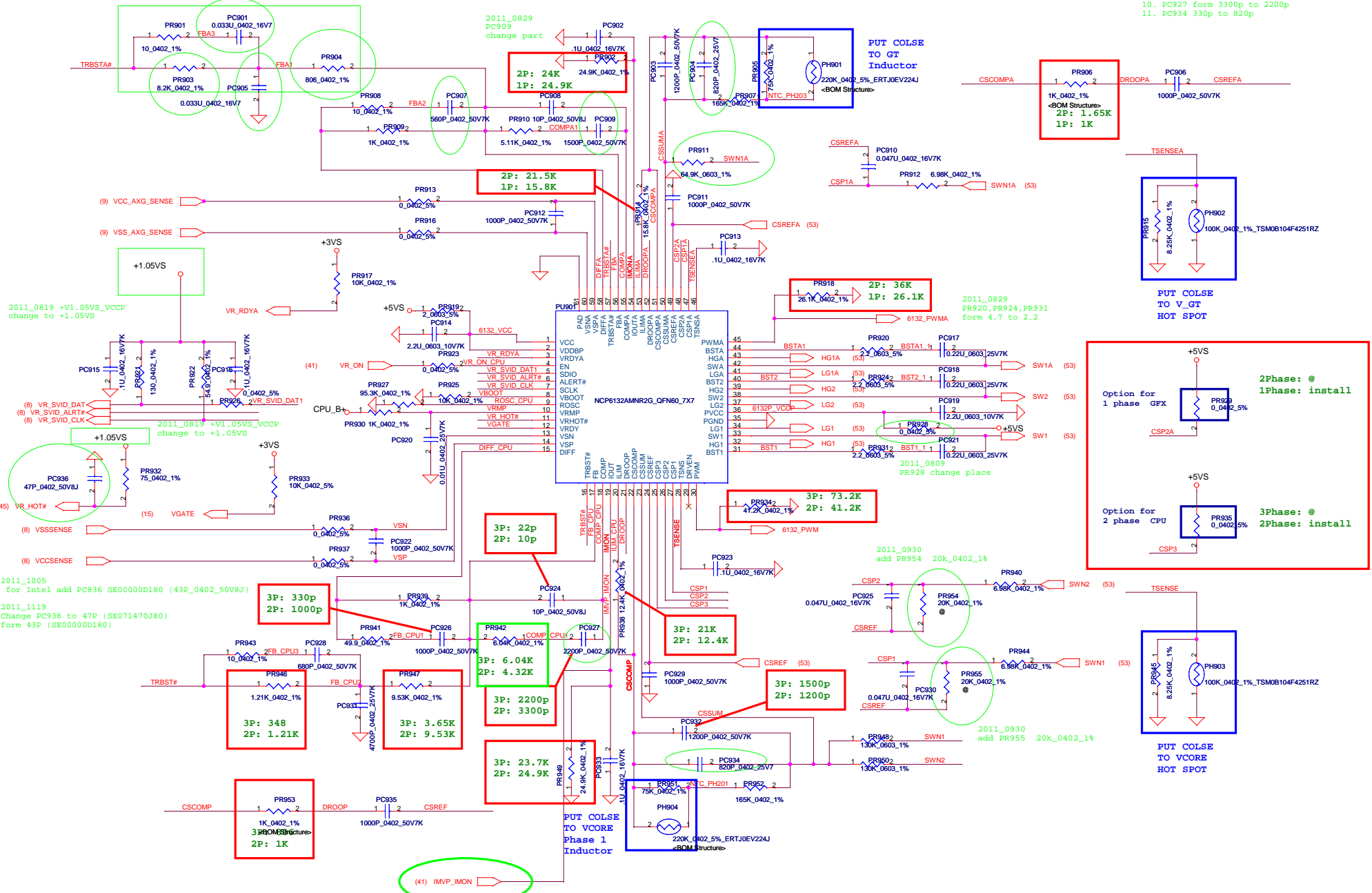
Compal Electronics, Inc.
PWR - VGA CORE

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2011_0830
PC901, PC905, PR901, PR903, PR904 mount

2011_1119
Change PC901, PC905 to 0.033u (SE076333K80)
from 0.033u (SE076333KNO)

- 2011_1007 for function test
1. modify PR903 form 1.21K to 8.2K,
2. PC905 form 4700p to 33n,
3. PC901 form 680p to 33n,
4. PR904 form 10.7K to 806,
5. PC907 form 330p to 560p
6. PC909 form 3300p to 1500p
7. PC904 form 330p to 820p
8. PR911 form 63.4K to 66.5K
9. PR942 form 4.32K to 6.04K
10. PC927 form 3300p to 2200p
11. PC934 330p to 820p



(9) VCC_AXG_SENSE

(9) VSS_AXG_SENSE

+1.05VS

2011_0819 +V1.05VS_VCCP
change to +1.05VS

(8) VR_SVID_DAT

(8) VR_SVID_ALRT#

(8) VR_SVID_CLK

+1.05VS

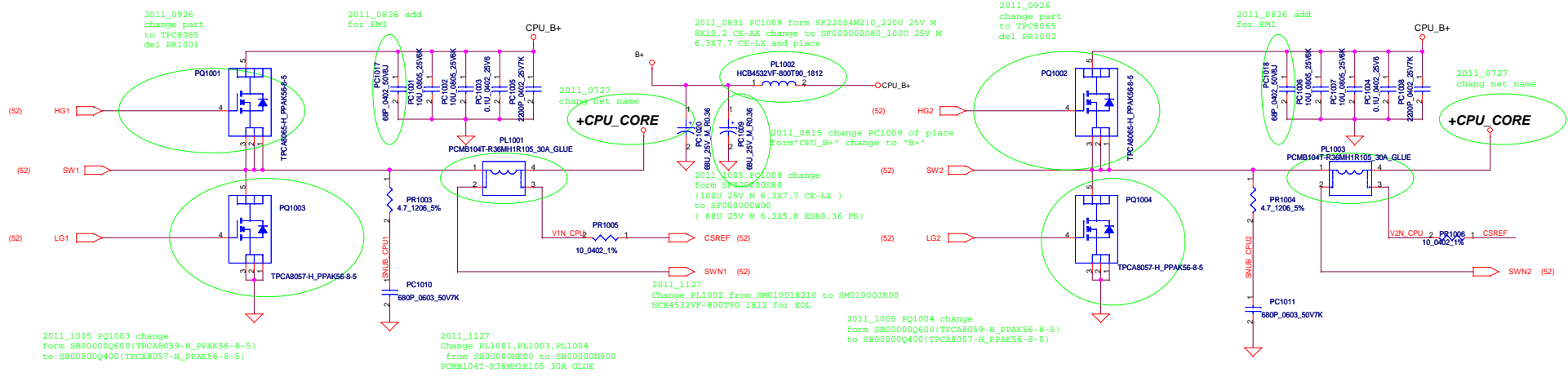
2011_0819 +V1.05VS_VCCP
change to +1.05VS

2011_1005
for Intel add PC836 SE00000D180 (43P_0402_50V87)

2011_1119
Change PC936 to 47P (SE071470J80)
form 43P (SE00000D180)

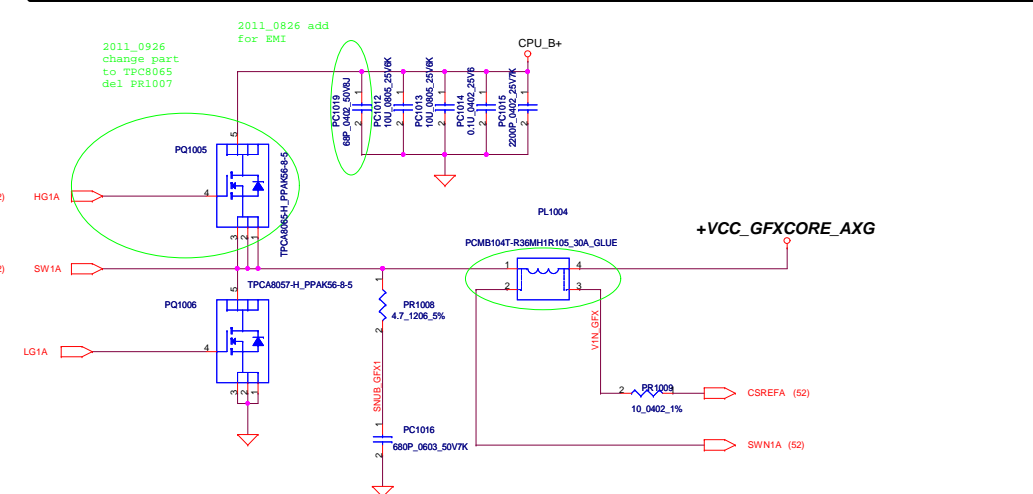
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Issued Date	2011/07/12	Deciphered Date
		2012/07/01
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Compal Electronics, Inc.		
Title		
PWR-CPU_CORE1		
Size	Document Number	Rev
Custom	IA-8133P	0.4
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QC 45W CPU
 VID1=0.9V
 IccMax=94A
 Icc_Dyn=66A
 Icc_TDC=52A
 R_LL=1.9m ohm
 OCP-110A

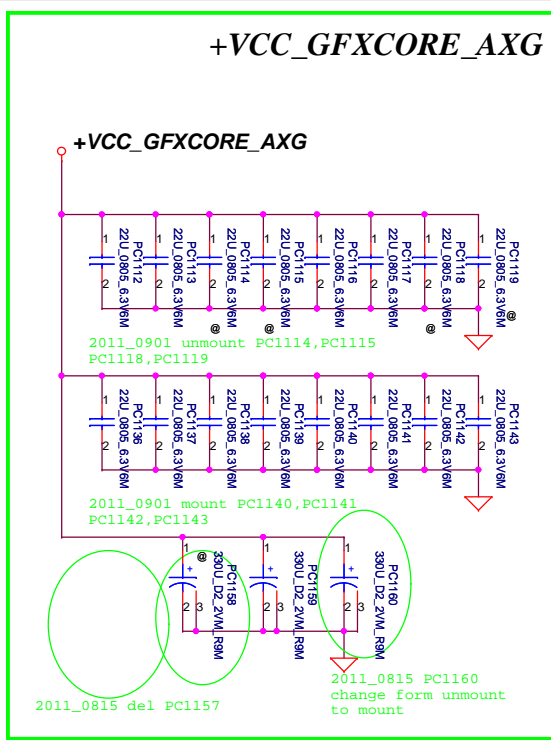
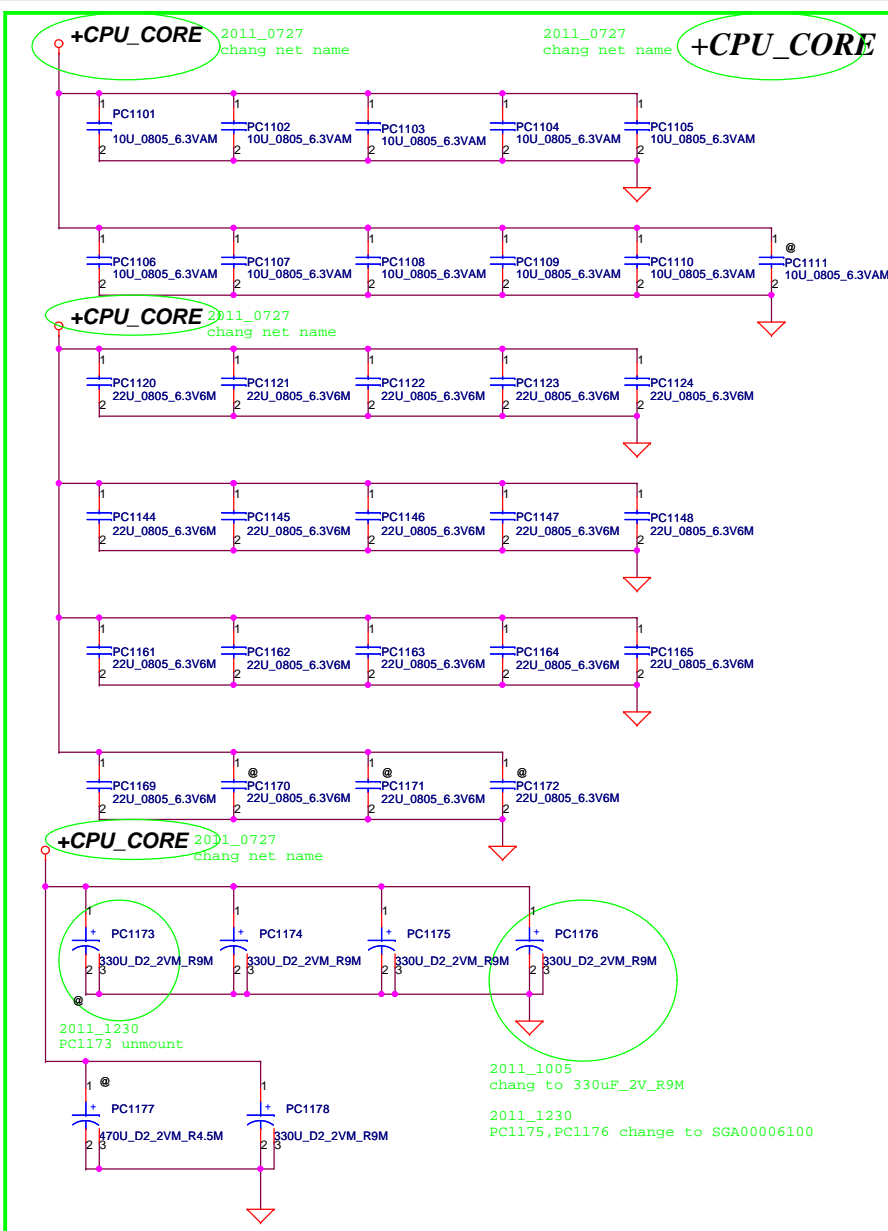
DC 35W CPU
 VID1=1.05V
 IccMax=53A
 Icc_Dyn=43A
 Icc_TDC=36A
 R_LL=1.9m ohm
 OCP-65A



QC 45W GT2
 VID1=1.23V
 IccMax=46A
 Icc_Dyn=37A
 Icc_TDC=38A
 R_LL=3.9m ohm
 OCP-55A

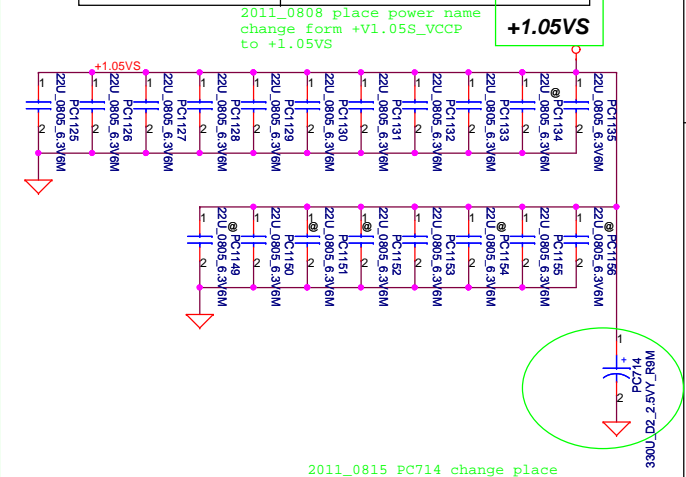
DC 35W GT2
 VID1=1.23V
 IccMax=33A
 Icc_Dyn=20.2A
 Icc_TDC=21.5A
 R_LL=3.9m ohm
 OCP-40A

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Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites



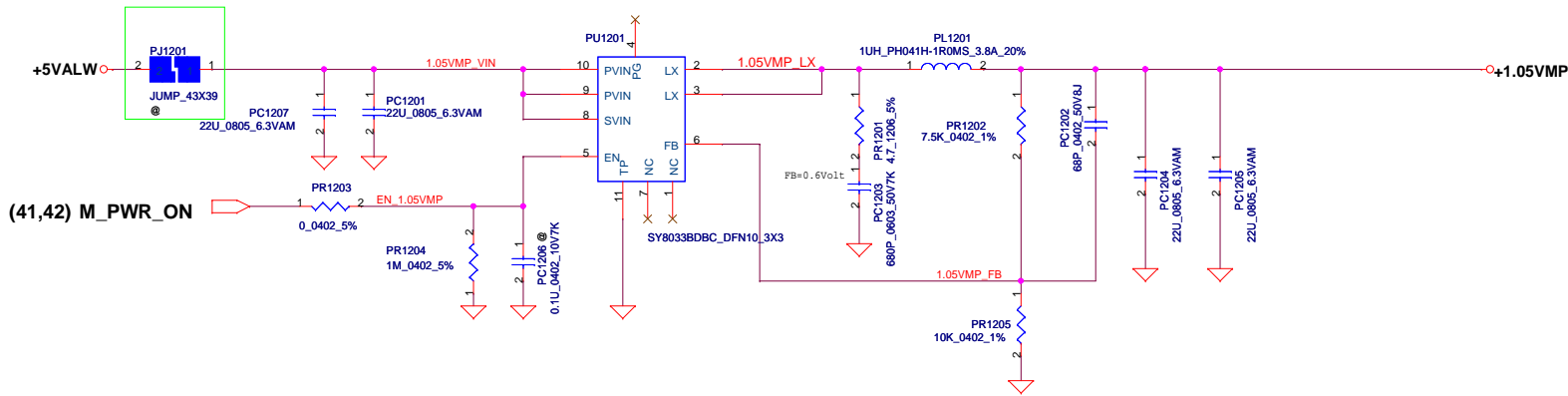
2011_0815 PC714 change place form "+1.05VS_VCCPP" to "+1.05VS"

2011_1005 PC714 change to 330uF_2V_R9M

2011_1007 PC714 form SGA00001Q802 (S POLY C 330U 2V M X LESR6M SX H1.9) change to SGA00002680 (330U_D2_2.5VY_R9M)

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2011_0923 JUMP form 43X79 change to 43X79

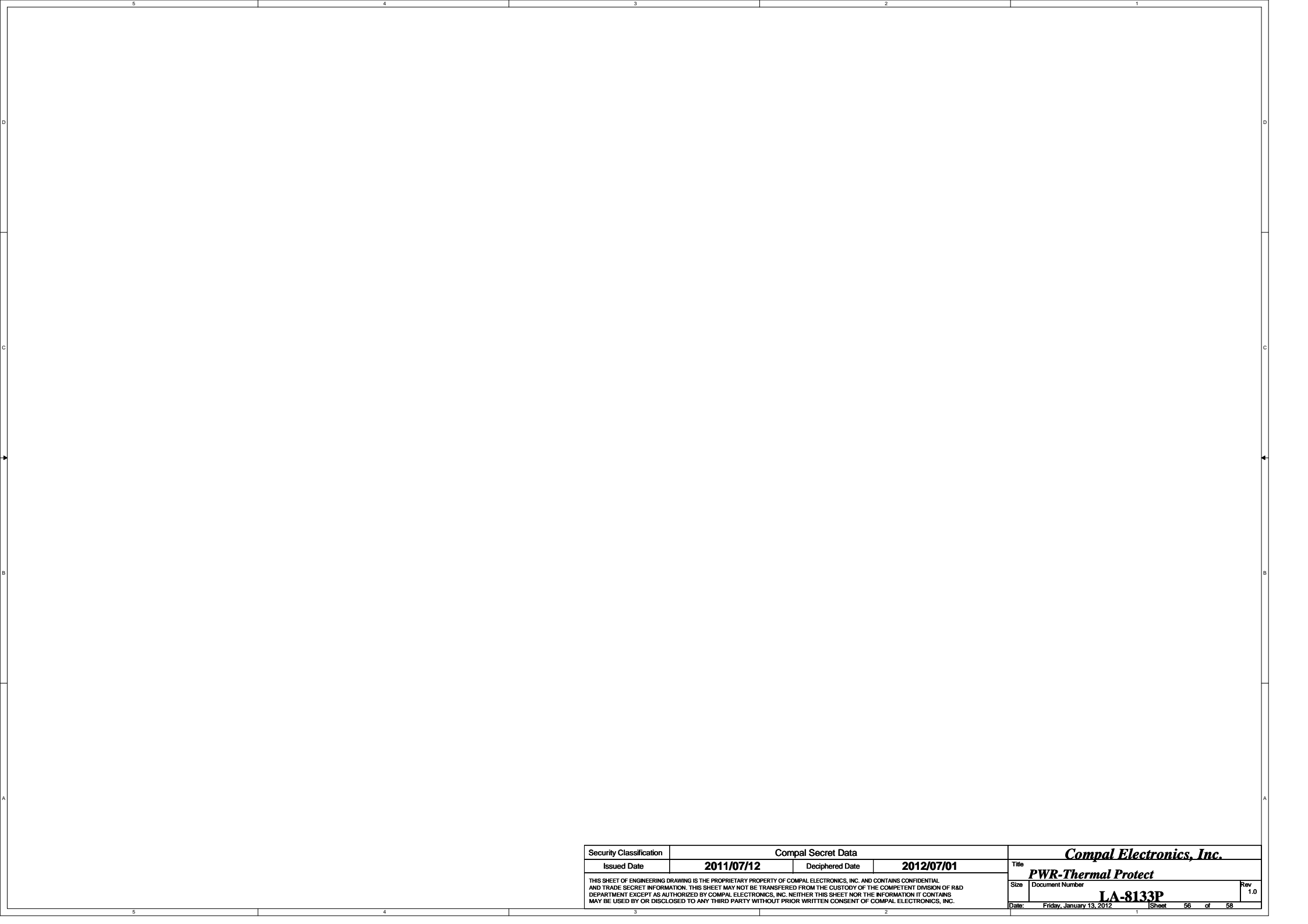


(41,42) M_PWR_ON



1.05VMP max current=1A

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				Rev	0.4



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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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				Size	Document Number
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Version Change List (P.I.R. List)

Phase	Date	No.	BOM	Sch	Layout	Description	function
	2011/09/13	No1		V	V	Add C2325,C2326,C2327,C2328,C2329,R2319,R2324,Q2312	Add SBA function (+3VM) power
	2011/09/15	No2		V		Del Q2305	Del SYSYON#
	2011/09/15	No3		V		Add EC pin 119(M_PWR_ON) for SBA function	Add SBA function
	2011/09/15	No4		V		Add EC pin 120(PCH_SLP#) from PCH to EC for SBA function	Add SBA function
	2011/09/15	No5		V		Add EC pin72 (Muxless_STAT) for GPU STAT	Add Muxless_STAT function
	2011/09/15	No6		V		Del PR310, PR311, PR312, PR313, net name:"H_PROCHOT#", +3VALW.	PWR-CHARGER-BQ24727
	2011/09/15	No7	V			mount PC832	
	2011/09/15	No8		V	V	Add R2482,Q2404,C2509,R2481,R2485,Q2400,R2483,C2501	AOAC Function
	2011/09/15	No9		V	V	change net name BT_OFF# to BT_ON# and change PCH EN GPIO from GPIO34 to GPIO36 R280 from @ to mount,R282 from mount to @	BT Function
	2011/09/15	No10		V	V	change net name(Mini-Express) from BT_OFF# to WLBT_OFF# PCH EN GPIO change to GPIO34	BT Function
	2011/09/19	No11		V	V	change +3VS_WLAN net name to +3VS_AOAC change +3VS_WWAN net name to +3VS_AOAC	AOAC Function
	2011/09/19	No12		V	V	Del R1010 for LVDS CONN plug high voltage	LVDS CONN
	2011/09/19	No13		V	V	R1102,R1104,R1105 from @ to mount fix MIC(ECR97236)issue	MIC function
	2011/09/19	No14		V	V	Add R2470 for 80 port function	80 port function
	2011/09/19	No15		V	V	Del R2476 Add Q2405	BT Function
	2011/09/20	No16		V	V	Add power schematic 9/15 again modify RF PC423, PC425, PC519, PC620, PC717, PC873, PC874, PC424, PC518, PC1017, PC1018, PC1019, PC422, PC516, PC517 modify POWER在VGA的PWM IC 加的零件PR869, PR870	
	2011/09/22	No17		V	V	Add U10,C589,C645 for TPM function	TPM function
	2011/09/22	No18		V	V	Add R110,R112 for SPI POWER choose(SBA function)	
	2011/09/23	No19		V	V	modify power page 44-57(PJ1201 JUMP form 43X79 change to 43X79)	
	2011/09/26	No20		V	V	change CPU footprint from TYCO_2013620-2_989P-T to TYCO_2013620-2_989P-T-A39 change PCH footprint from PANTHER-POINT_FCBGA_989P-T to PANTHER-POINT_FCBGA_989P-T-A39 change GPU footprint N13P-PES-A1_FCBGA_908P to N13P-PES-A1_FCBGA_908P-A39 change VRAM footprint K4W1G1646E-HC12_FBGA_96P to K4W1G1646E-HC12_FBGA_96P-A39	
	2011/09/26	No21		V	V	change PCH_GPIO24(R288) pull up to +3V_PCH	
	2011/09/26	No22		V	V	change P18 (R311,R330,R286,R329) for UMA and Optimus memon	
	2011/09/26	No23		V	V	change net name PCH_THRMTRIP#_R to VGA_THRMTRIP#	
	2011/09/26	No24		V	V	PQ702 change to TPC8065,Del PR705 PQ1001,PQ1002,PQ1005 change to TPC8065,Del PR1001,PR1002,PR1007	
	2011/09/26	No25		V	V	p43 change Q2304 dual channel 2n7002 to single channel Q2304,Q2305(Q2305 @) p43 change Q2306 dual channel 2n7002 to single channel Q2306,Q2311(Q2311 @)	
	2011/09/27	No27	V			modify EC Board ID R2213 to 18K	
	2011/09/27	No28		V	V	net name CX_GPIO0 connect to U1101 pin 38	
	2011/09/27	No29		V	V	Add C2152,C2153,D2113 for ESD	
	2011/09/27	No30		V	V	change NVidia N13W ROM_SCLK from 15K PU to 5K PU	
	2011/09/27	No31		V	V	change ESD part D2401,D2403,D2405 power from +5VALW to +USB VCCA	
	2011/09/27	No32		V	V	Add C2108 for GPU_CLKREQA	
	2011/09/27	No33		V	V	Add Q2406 , modify R2401,Change PCH_GPIO19 to ODD_DET#,for zero power ODD	
	2011/09/27	No34		V	V	change WLBT_OFF# to PCH_GPIO34	
	2011/09/27	No35		V	V	change PCH_GPIO34 to WLBT_OFF#(mini card pin5)	
	2011/09/27	No36		V	V	change BT_ON# connect to WLBT_OFF#(mini card pin51)	
	2011/09/28	No37		V	V	C76 , R1123 , c1131 , R2201.C2209 C84,C85 from @ to mount for RF team	
	2011/09/29	No38		V	V	R1529 change to 15K	
	2011/09/29	No39		V	V	Add CONN JDB3 fo debug	
	2011/09/29	No40		V	V	Add R2460,R2438,R2471,R2472,R2475,R2476 for PS8520B	
	2011/09/29	No41		V	V	change D2403 ,D2401 power to +USB_VCCB,and del D2403 ,D2401,D2405 Pin3 net	
	2011/09/29	No42		V	V	change power schematic del PC606 (22U_0805_6_3V6M) PR855:1 net change form +VGA_CORE to +VGA_COREP PR827 mount change to @(non-mount) PR839 for 47Kohm change to 147Kohm PR103 for 0ohm change to 270ohm PC1166 non-mount,PC1173 non-mount,PC1158 non-mount	
	2011/09/29	No44		V	V	Add Q2313,C2305,C2306,C2307,C2308,R2318,R2320,R2320,C2322 for +3V_PCH change CRT CONN to DC061109231(footprint pin modify) Add PR954,PR955	
	2011/09/29	No45		V	V	Add H16,H27 change Q2304,Q2305 to Q2304 modify PTH H11,H18 ,H21 Del T10 for SUS_STAT(SLP_S3# 走不出来)	
	2011/10/04	No46		V	V	reserve R352,R353 for SATA re-drive PS-8131B change net name from WLBT_OFF to WLBT_OFF_5# modify PCH_GPIO34 connect to BT_ON# for BT module modify PCH_GPIO36 from BT_ON# connect to WLBT_OFF_51# for mini card BT combo module change Q2301 to 2N7002	
	2011/10/05	No47		V	V	Del R2469,T49,T45,T41,T37,T36,T28,T26 for ME 限高0 changer power net +3VS_FP to +3VS update power schematics P44-P57	
	2011/10/06	No48		V	V	change Q1202 part to SB000007H10. change JCARD1 FN to SP02000H810 footprint: ACES_87213-1400G_14P change some CONN part NO. for ME CONN list Add D2416	

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