

Compal Confidential

QML70 Schematics Document

AMD Comal

APU Trinity / Hudson M3 / Thames XT M2
UMA Only / PX Muxless with BACO

2011-10-17

LA-8371P REV: 0.2



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Model Name : QML70

Comal



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64M x 16 x 8
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Thermal Sensor
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+3VSG, +VGA_CORE, +VDDCI
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+1.5V, +1.2VS, +2.5VS
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APU HDMI (UMA / Muxless)

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LVDS

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GEN1

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USB3.0 Port 1 USB2.0 Port 11
USB2.0 Port 0
USB2.0 Port 1
USB2.0 Port 2
USB2.0 Port 3

HD Audio 3.3V 24.576MHz/48MHz
USB2.0 Port 4

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port 1
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Int.KBD
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LED
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RTC CKT.
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DC/DC Interface CKT.
page 39

VGA DC/DC Interface CKT.
page 26

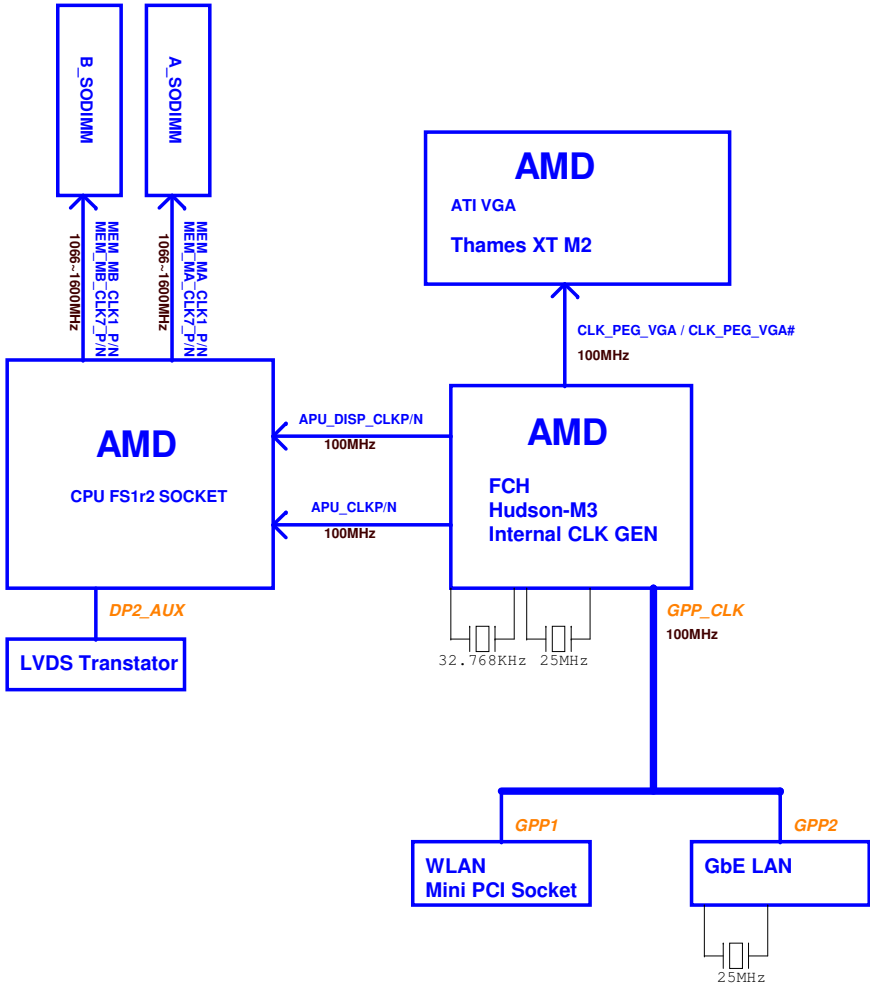
Power Circuit
page 40~50



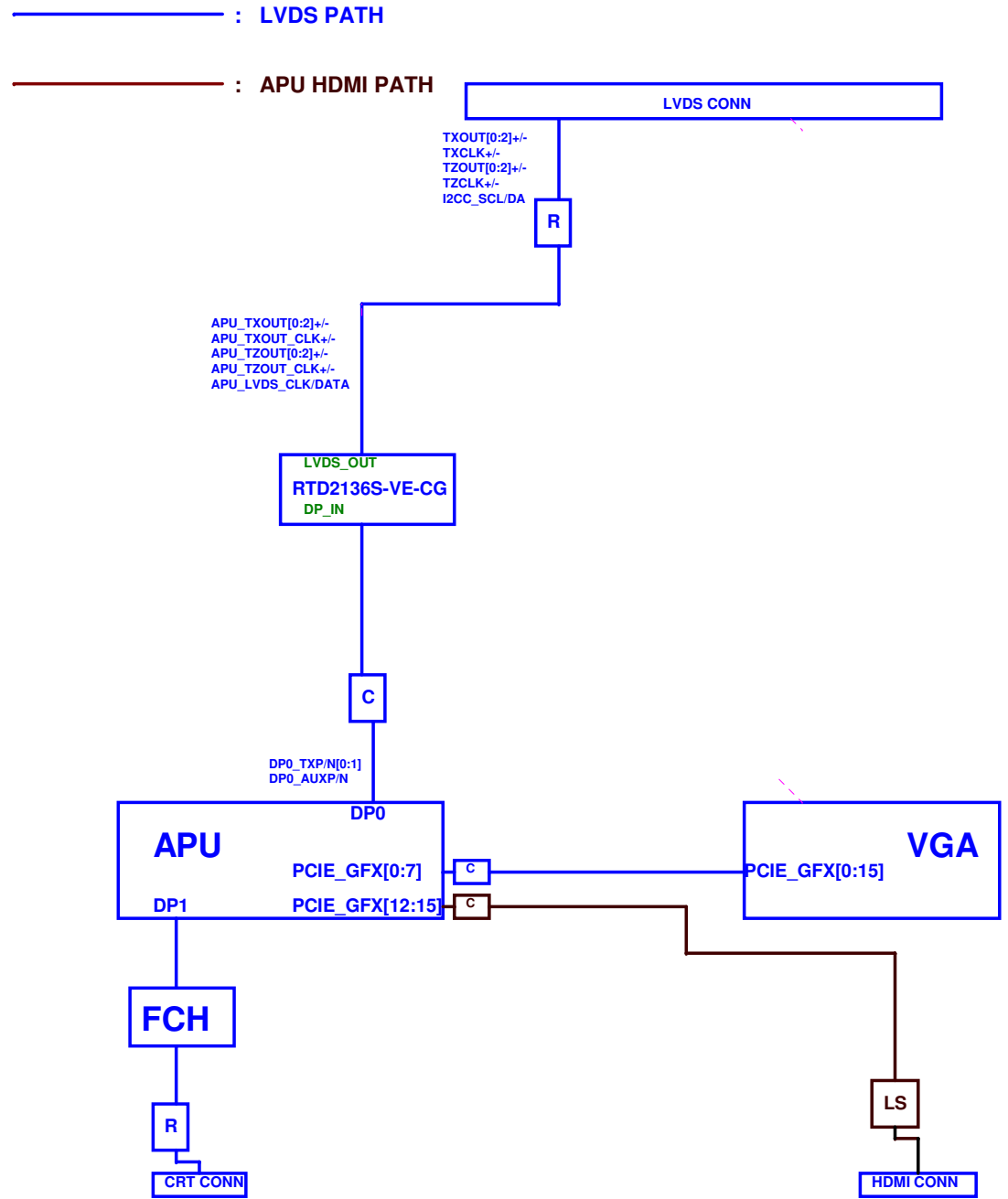
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CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION



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Voltage Rails

Power Plane	Description	S1	S3	S4/S5	Deep S3
VIN	Adapter power supply (19V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF	ON
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	ON*	OFF
+3V_PCH	3.3V switched power rail for FCH	ON	ON	ON*	OFF
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF	OFF
+3VSG	1.8V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF	ON
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*	ON
+LAN_IO	3.3V power rail for LAN	ON	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*	ON
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*	ON
+RTCVCC	RTC power	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

x = 1 is read cmd, x= 0 is write cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032	1001 101X b	9AH
			AMD Thames XT M2	1000 001X b	82H
			AMD FS12 (APU)	1001 1000 b	98H
			RTD2132S (TL)	1010 1000 b	A8H

FCH SM Bus 0 address

Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1101 000X b	D0			
DDR DIMM2	1101 001X b	D2			

FCH SM Bus 1 address

Device	Address	HEX	Device	Address	HEX

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

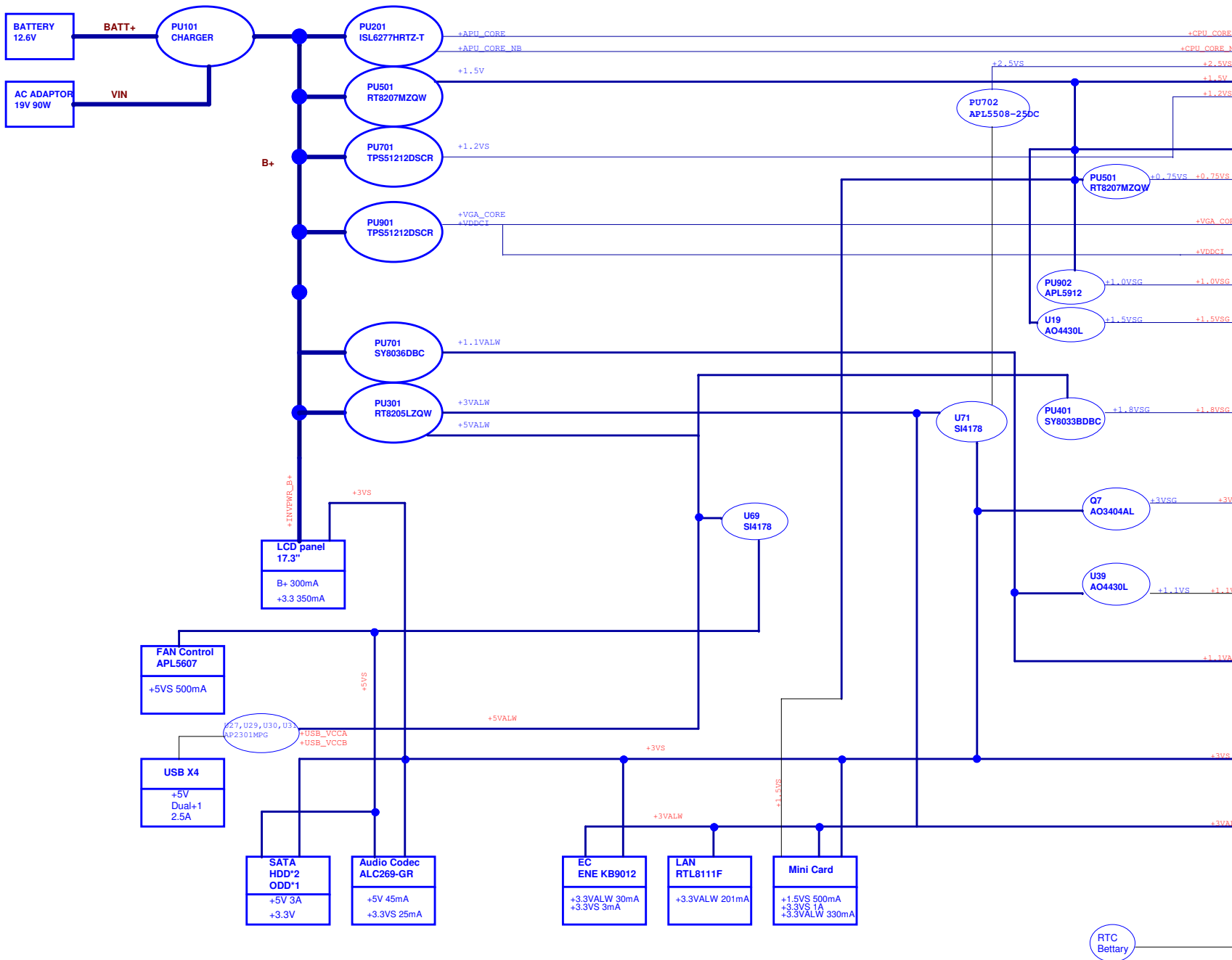
BOM Structure	BTO Item
PX@	Use VGA (Mux)
X76@	VRAM ID Table
AI	Use AI Charger
nonAI@	Do not use AI Charger
CARD@	Use Card Reader IC
nonCARD@	do not use Card Reader IC
X76L01@	Use Hynix GDDR3 1GB VRAM
X76L02@	Use Hynix GDDR3 2GB VRAM
X76L03@	Use Samsung GDDR3 1GB VRAM
X76L04@	Use Samsung GDDR3 2GB VRAM
930@	Use EC KB930
9012@	Use EC KB9012

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max
0	0 +/- 5%	0 V	0 V	0.155 V
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V

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AMD APU FS1	
1.025~1.475V	VDD CORE 54A
0.7~1.475V	VDDNB 27.5A
+2.5VS	VDDA 500mA
+1.5V	VDDIO 4.6A
+1.2VS	VDDR 6.7A

RAM DDRIII SODIMMX2	
+1.5V	VDD_MEM 4A
+0.75VS	VTT_MEM 0.5A

VGA ATI Whistler/Seymour/Granville	
0.85~1.1V	VDDC 47A
0.9~1.0V	VDDCI 4.6A
+1.0VSG	DPLL_VDDC: 125 mA SPV10: 120 mA PCIE_VDDC: 2000 mA DP[A]E_VDD10: 680 mA
+1.5VSG	VDDR1: 3400 mA
+1.8VSG	PLL_PVDD: 75 mA TSVDD: 20 mA AVDD: 70 mA VDD1D1: 100 mA VDD2D1: 50 mA AZVDD: 1.5 mA VDD_CT: 110 mA VDDR4: 170 mA PCIE_PVDD: 40 mA MPV18: 150 mA SPV18: 75 mA PCIE_VDDR: 400 mA DP[A]F_VDD18: 920 mA DP[A]F_PVDD: 120 mA
+3VSG	AZVDD: 130 mA VDDR3: 60 mA

VRAM 1GB/2GB 64M / 128Mx16 * 4 / 8	
+1.5VSG	2.4 A

FCH AMD Hudson M2/M3	
+1.1VS	VDDPL_11_DAC: 7 mA VDDAN_11_ML: 226 mA VDDCR_11: 1007 mA VDDAN_11_CLK: 340 mA VDDAN_11_PCIE: 1088 mA VDDAN_11_SATA: 1337 mA
+1.1VALW	VDDAN_11_USB_S: 140 mA VDDCR_11_USB_S: 197 mA VDDAN_11_SSUSB_S: 282 mA VDDCR_11_SSUSB_S: 424 mA VDDCR_11_S: 187 mA VDDPL_11_SYS: 70 mA
+3VS	VDDIO_33_PCIE: 131 mA VDDPL_33_SYS: 47 mA VDDPL_33_DAC: 20 mA VDDPL_33_ML: 20 mA VDDAN_33_DAC: 200 mA VDDPL_33_PCIE: 43 mA VDDPL_33_SATA: 93 mA VDDIO_AZ_S: 26 mA
+3VALW	VDDPL_33_SSUSB_S: 20 mA VDDPL_33_USB_S: 17 mA VDDAN_33_USB_S: 658 mA VDDIO_33_S: 59 mA VDDXL_33_S: 5 mA VDDAN_33_HWM_S: 12 mA
GND	VDDIO_33_GBE_S VDDCR_11_GBE_S VDDIO_GBE_S
RTC BAT	VDDBT_RTC_G

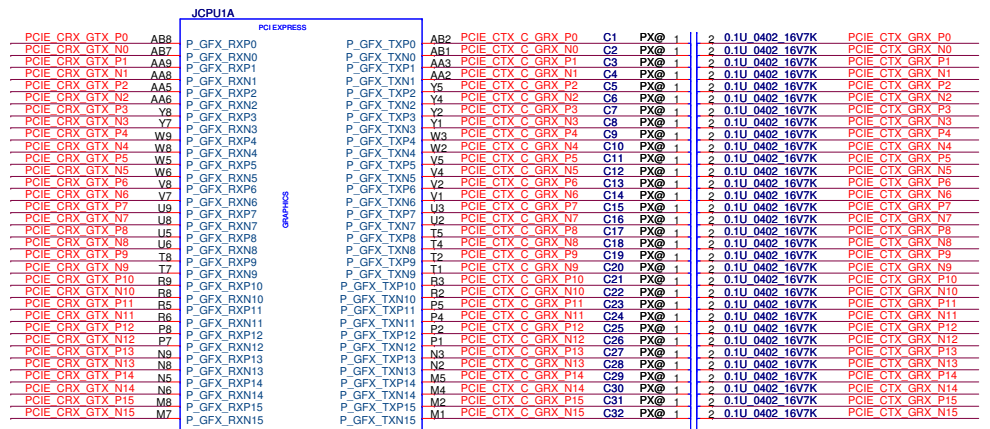
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18 PCIE_CRX_GTX_P[0..15]

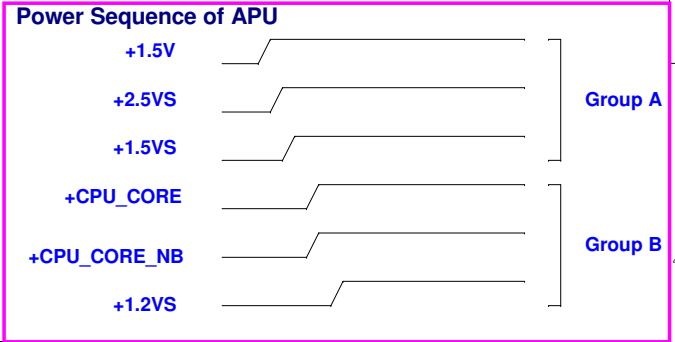
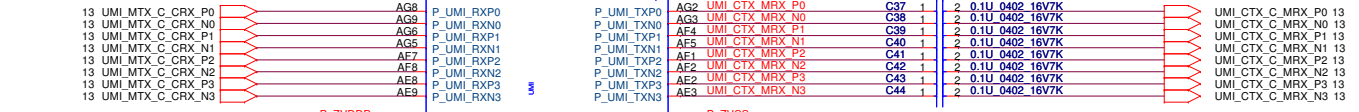
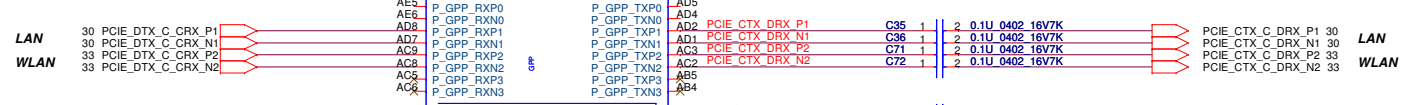
18 PCIE_CRX_GTX_N[0..15]

PCIE_CTX_GRX_P[0..15] 18

PCIE_CTX_GRX_N[0..15] 18

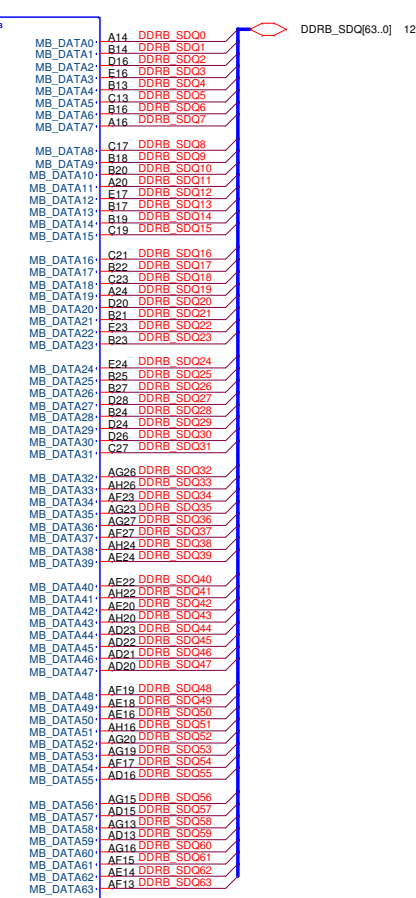
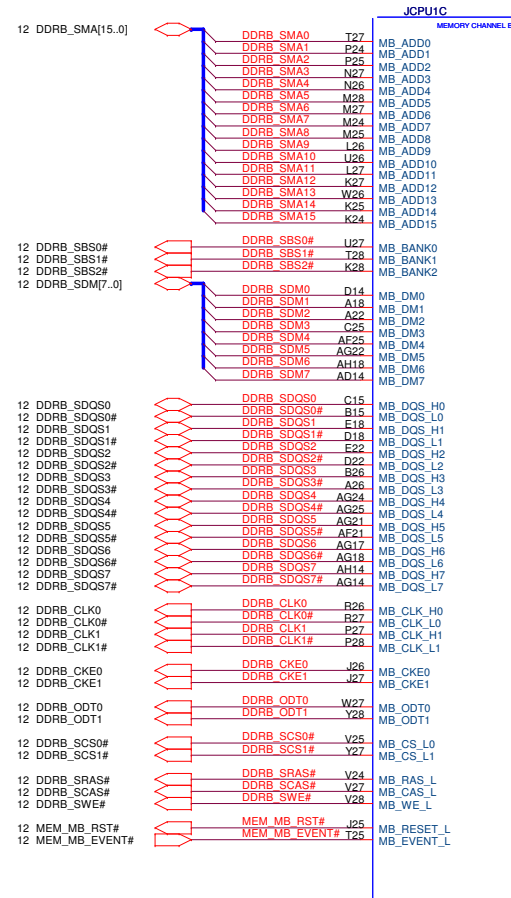
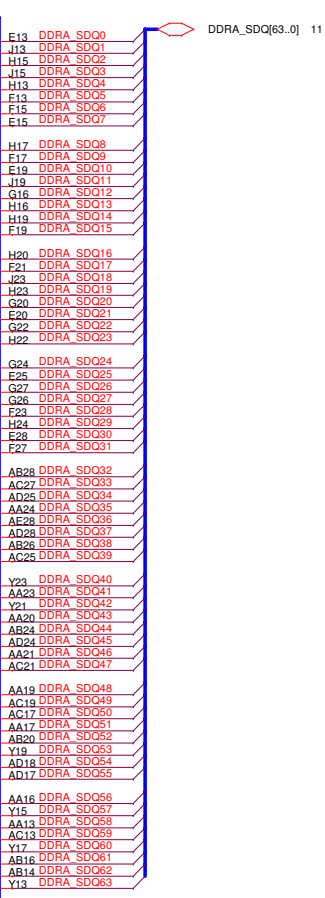
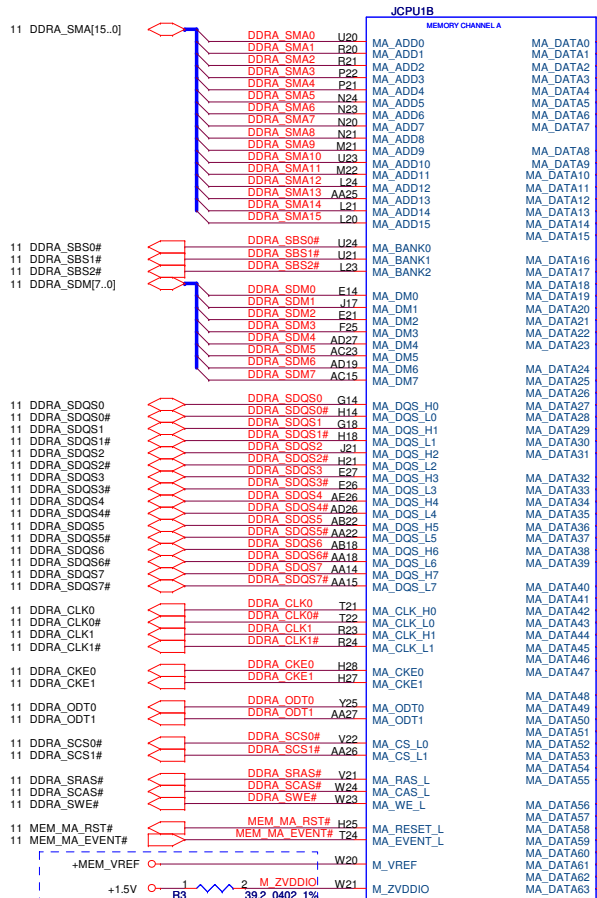


LAN
WLAN



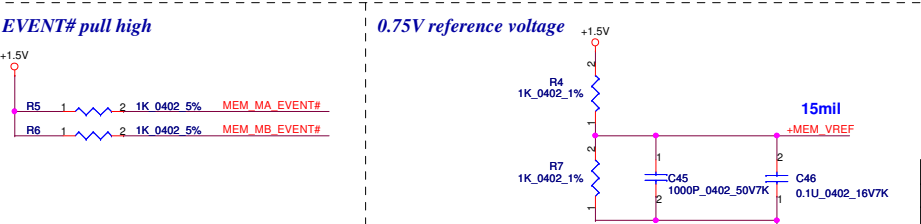
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				FS1r2 PCIE/UMI		
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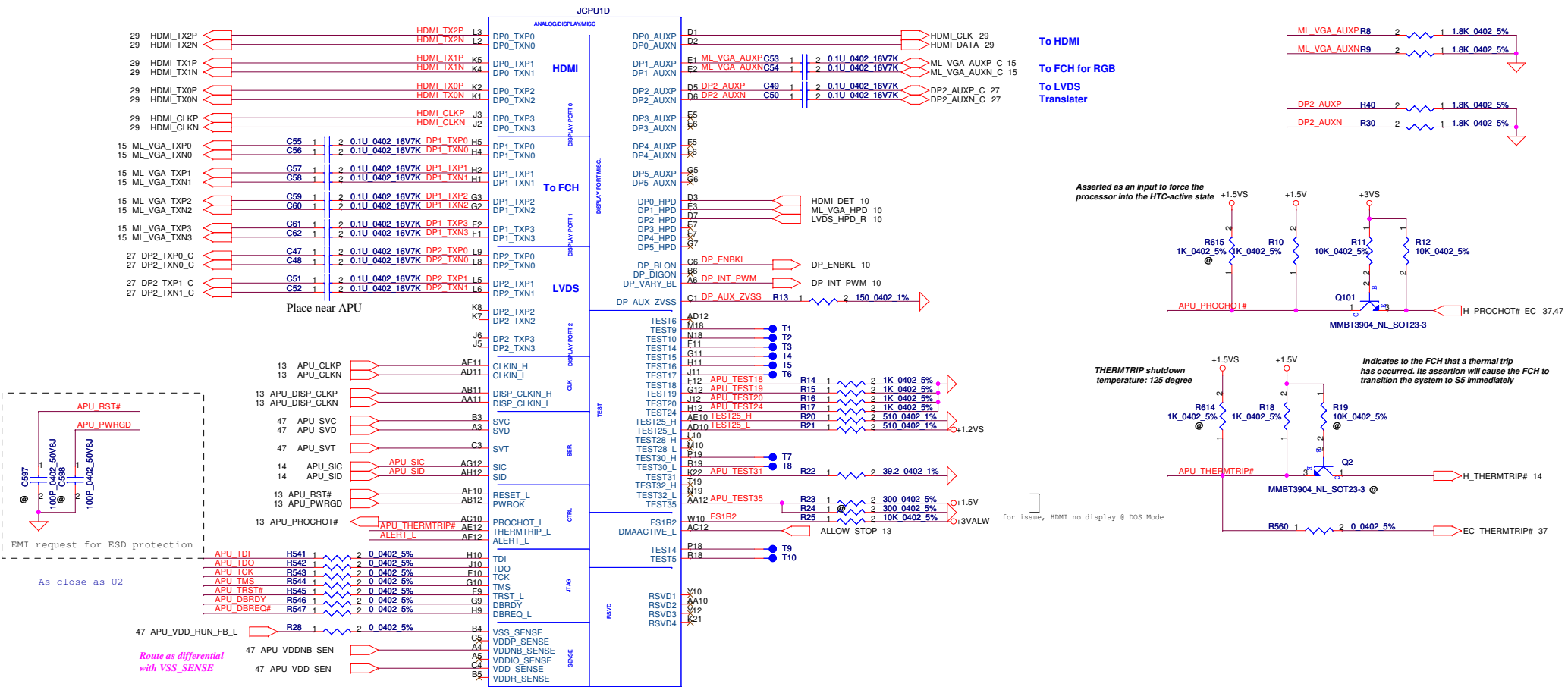


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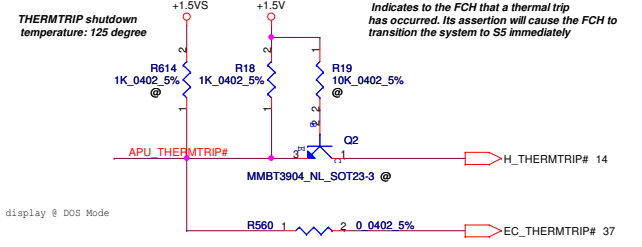
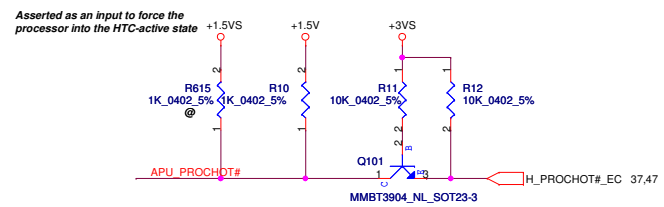
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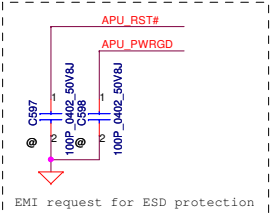
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To HDMI
To FCH for RGB
To LVDS
Translator



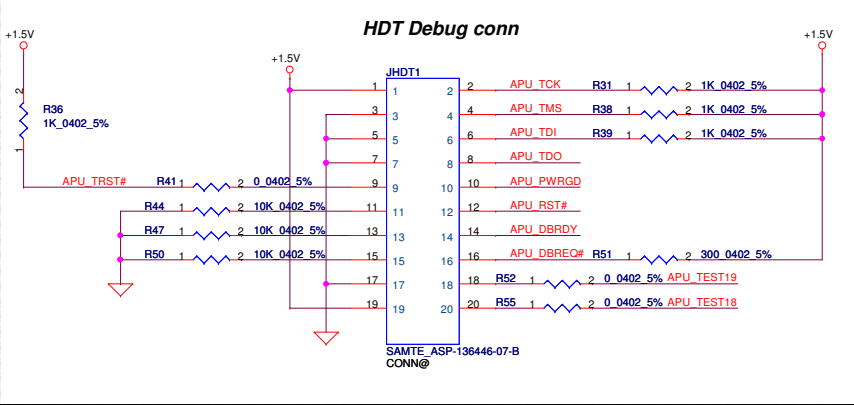
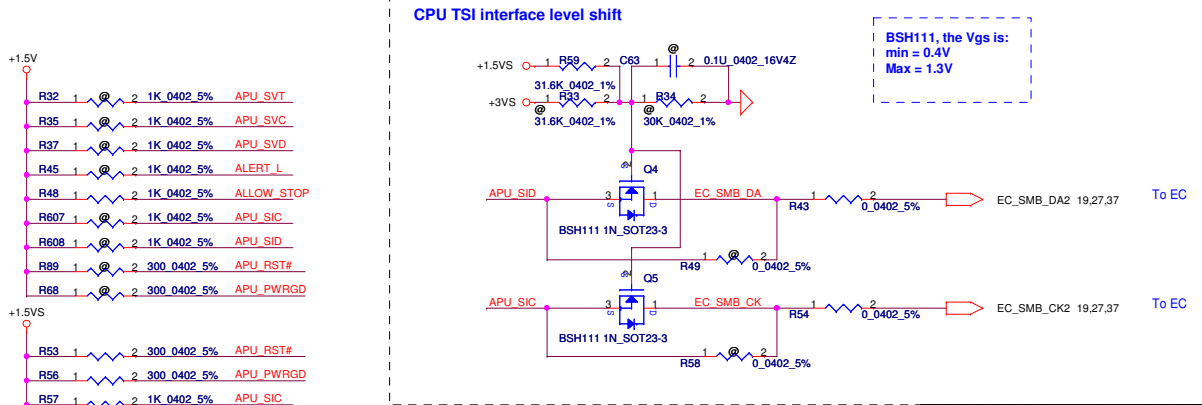
for issue, HDMI no display @ DOS Mode



EMI request for ESD protection

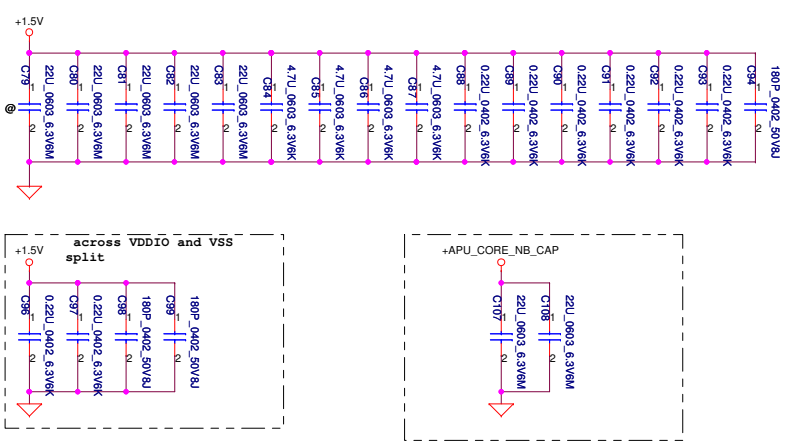
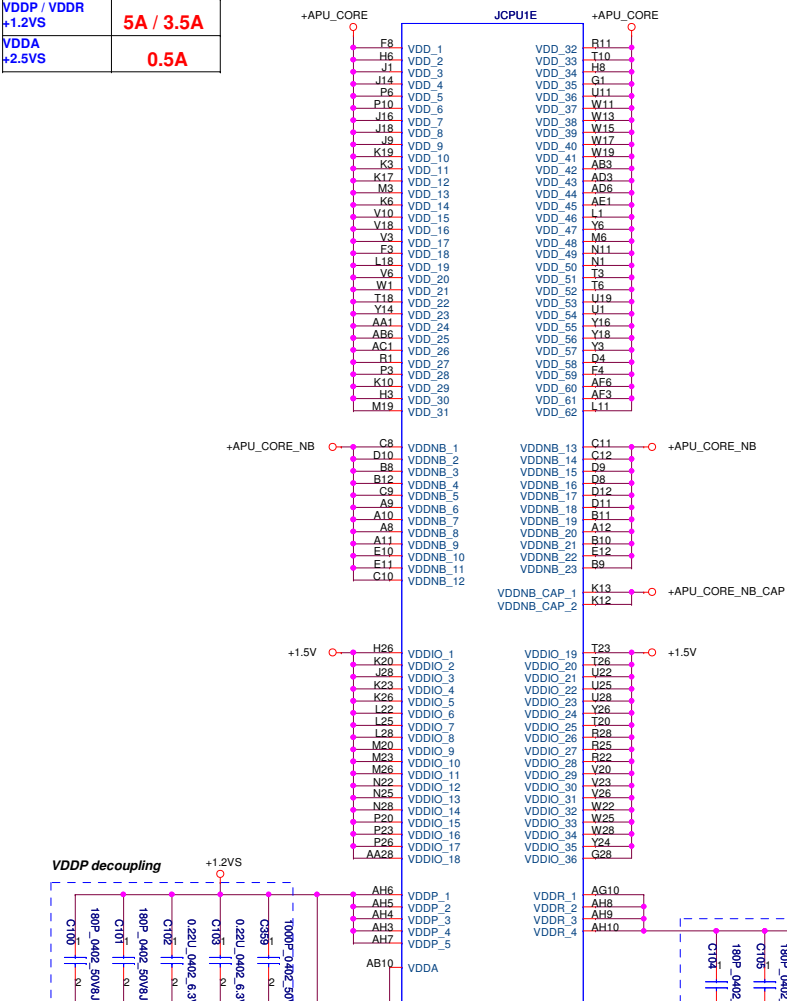
As close as U2

Route as differential with VSS_SENSE

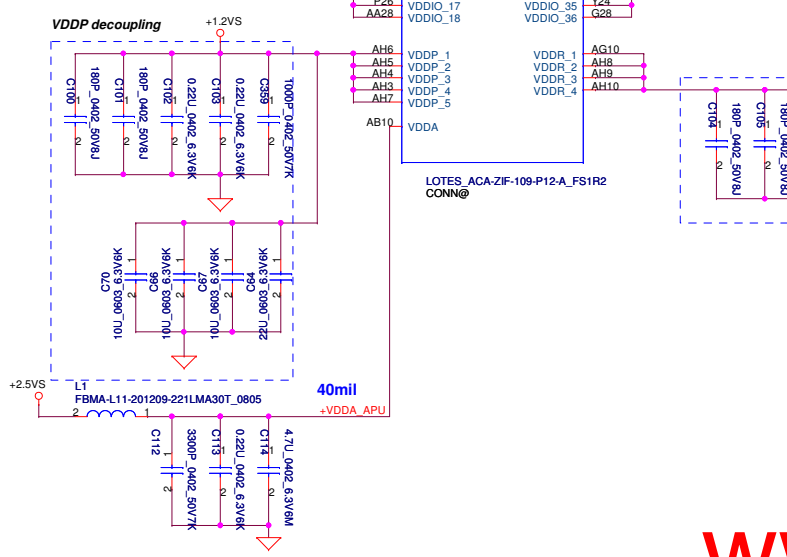


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Power Name	Consumption
VDD +CPU_CORE	60A
VDDNB +CPU_CORE_NB	29A
VDDIO +1.5V	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.5A



JCPU1F		
J20	VSS_1	A19
L4	VSS_2	A21
R7	VSS_3	A23
W18	VSS_4	A25
A15	VSS_5	A27
AB17	VSS_6	AA4
AC22	VSS_7	AA7
AE21	VSS_8	AB13
AF24	VSS_9	AB15
AH23	VSS_10	AB19
AH25	VSS_11	AB21
B7	VSS_12	AB23
C14	VSS_13	AB25
C2	VSS_14	AB27
C20	VSS_15	AB8
C22	VSS_16	AC14
C24	VSS_17	AC18
C26	VSS_18	AC20
C28	VSS_19	AC22
D13	VSS_20	AC26
D15	VSS_21	AC28
D17	VSS_22	AC4
D19	VSS_24	AC7
D23	VSS_25	AD9
D27	VSS_27	AE13
E4	VSS_28	AE17
F14	VSS_29	M9
F16	VSS_30	N4
F18	VSS_31	N7
F20	VSS_33	N10
F22	VSS_34	N11
F24	VSS_35	N14
F26	VSS_36	N15
F28	VSS_38	T9
G15	VSS_39	U10
G17	VSS_40	U4
G19	VSS_41	U7
G21	VSS_42	V11
G23	VSS_44	AE19
G25	VSS_45	AE23
G4	VSS_43	AE25
J22	VSS_45	AE27
J24	VSS_46	AE4
J4	VSS_47	AE7
J7	VSS_48	AF14
K11	VSS_49	AF16
K14	VSS_50	AF18
K9	VSS_51	AF20
AC11	VSS_52	AF22
L19	VSS_53	AF26
L7	VSS_54	AF28
M11	VSS_55	AG4
AF11	VSS_56	AG7
V19	VSS_57	AH13
V9	VSS_58	AH17
W4	VSS_59	AH19
W7	VSS_60	AH21
Y11	VSS_62	C18
Y20	VSS_63	D21
Y22	VSS_64	W14
Y9	VSS_65	P11
A17	VSS_66	P9
A13	VSS_67	E8
K16	VSS_68	K18
F24	VSS_69	W12
G8	VSS_70	
H7	VSS_71	
J8	VSS_72	



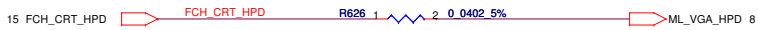
Demo Board Capacitor		
APU_CORE	CORE_NB	CORE_NB_CAP
22uF x 7	22uF x 2	22uF x 2
0.22uF x 2	10uF x 1	
0.01uF x 3	0.22uF x 2	
180pF x 2	180pF x 3	
VDDP	VDDR	VDDA
22uF x 1	10uF x 3	4.7uF x 1
10uF x 3	0.22uF x 2	0.22uF x 1
0.22uF x 2	1nF x 1	3.3nF x 1
180pF x 2	180pF x 2	
1nF x 1		

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HPD

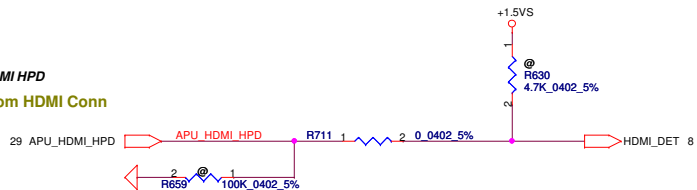
CRT HPD From FCH



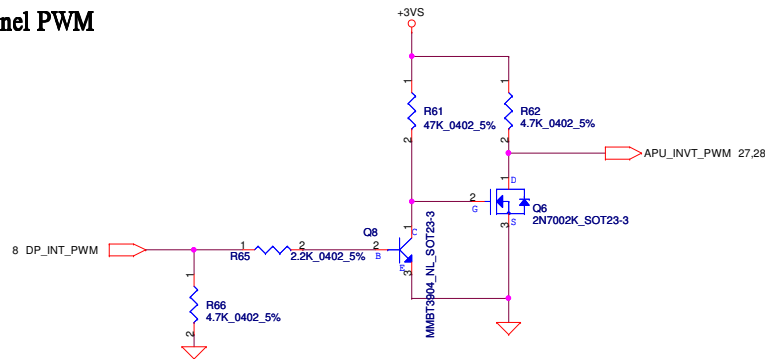
Translator HPD From Translator



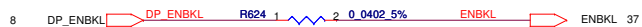
HDMI HPD From HDMI Conn



Panel PWM

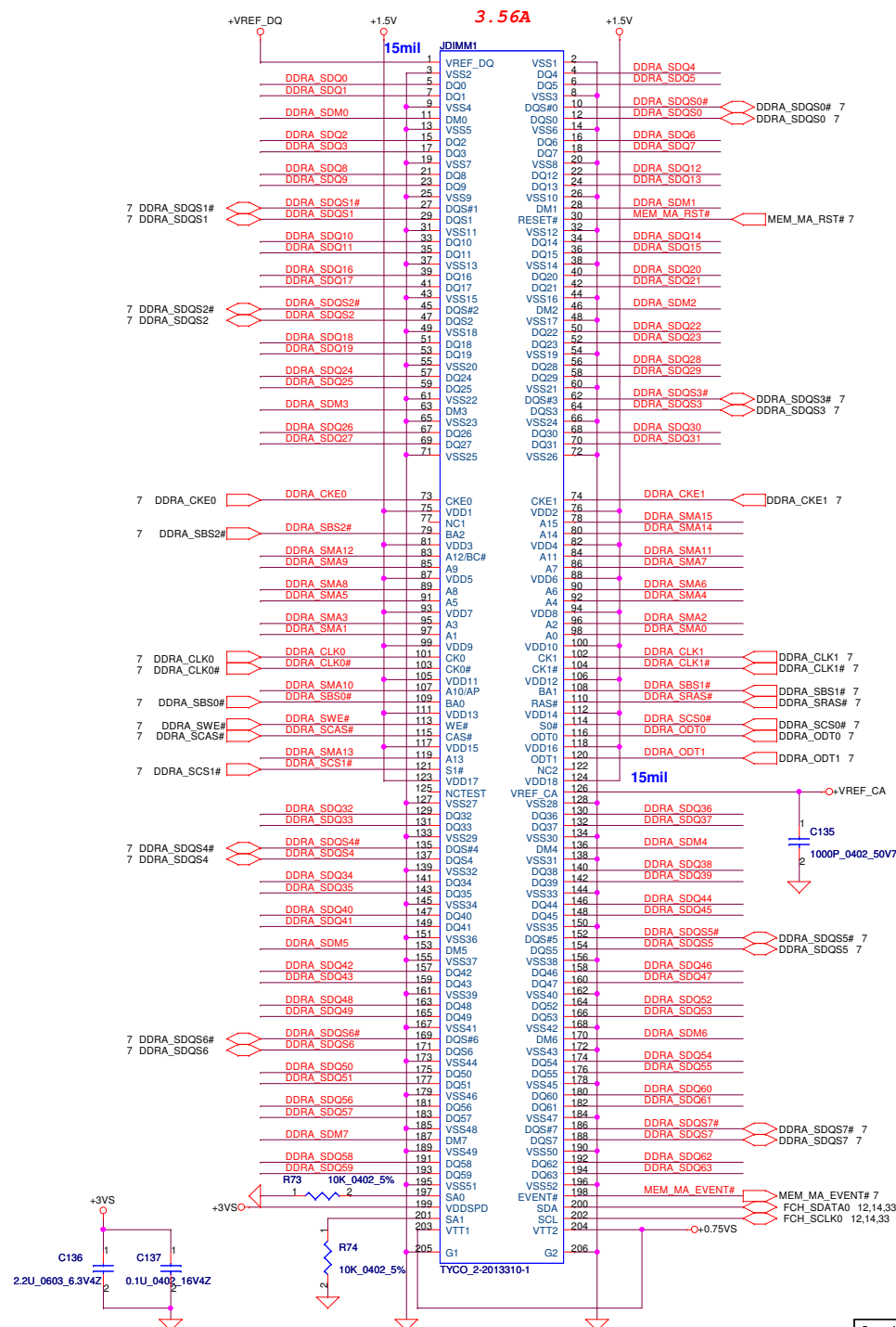


Panel ENBKL



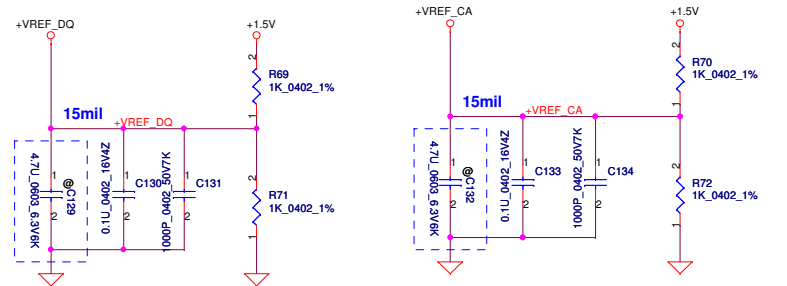
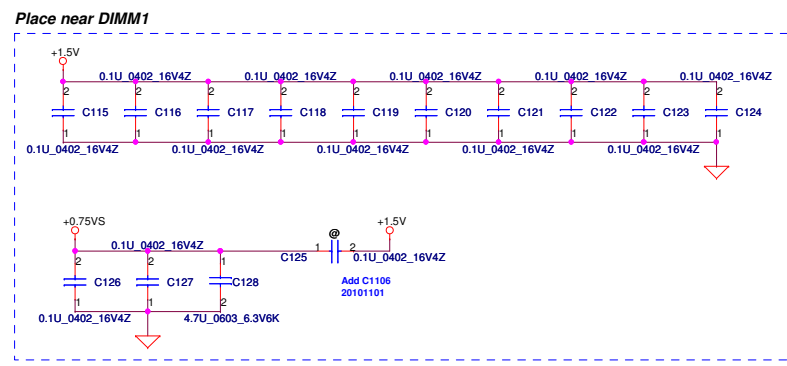
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Issued Date		2011/07/29		Deciphered Date		2012/07/29		Title					
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								Custom		QML70 LA-8371P		0.2	
								Date: Wednesday, October 19, 2011 Sheet 10 of 53					

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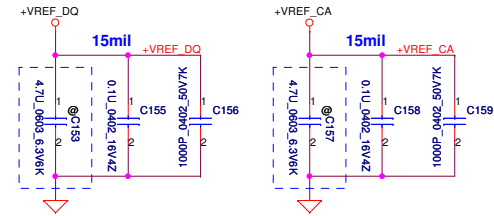
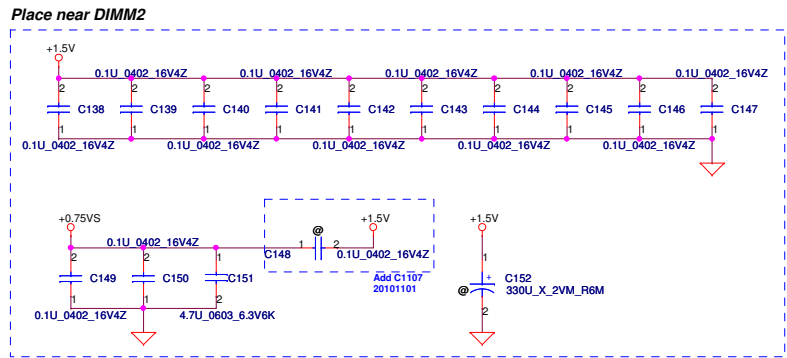
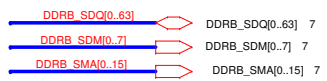
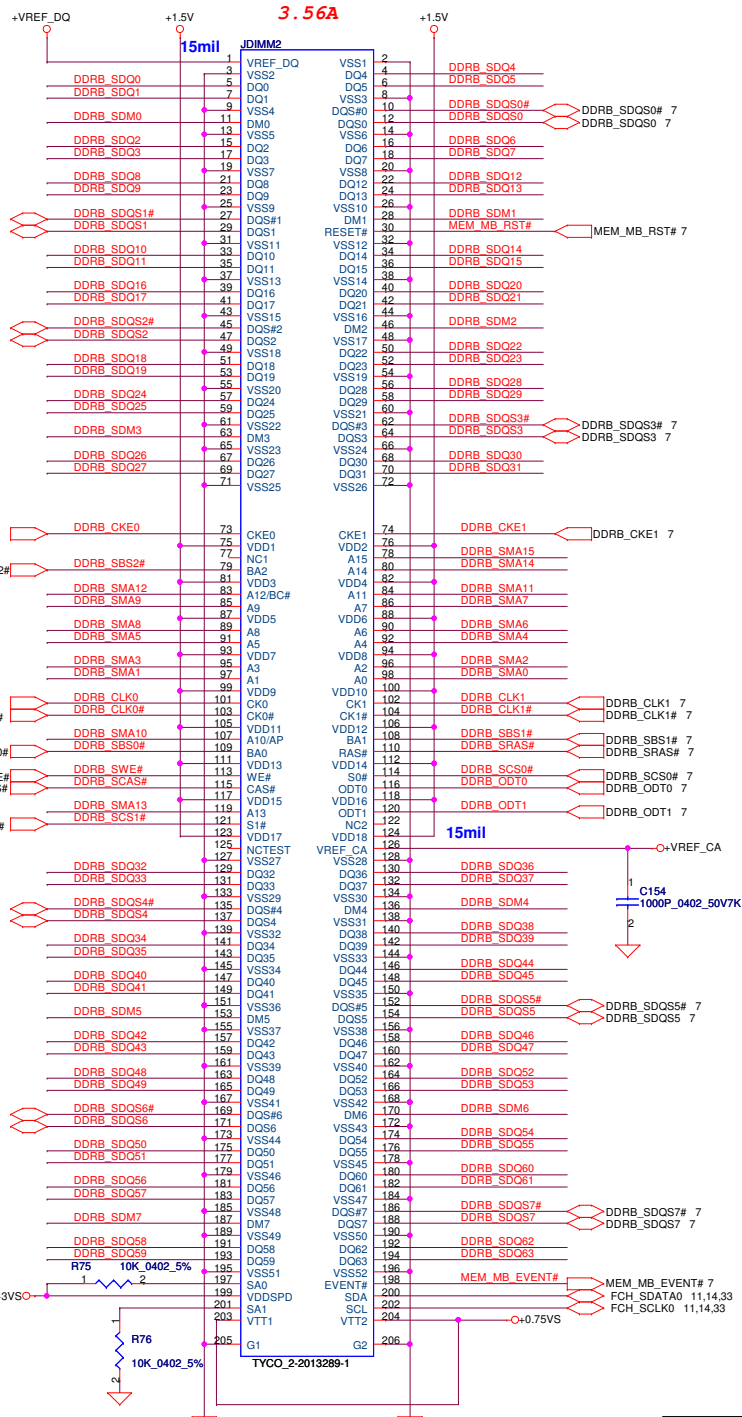
DIMM_A STD H:9.2mm
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- DDRA_SDO[0..63] DDRA_SDO[0..63] 7
- DDRA_SDM[0..7] DDRA_SDM[0..7] 7
- DDRA_SMA[0..15] DDRA_SMA[0..15] 7



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Size	Document Number	Rev	Date: Wednesday, October 19, 2011 Sheet 11 of 53		
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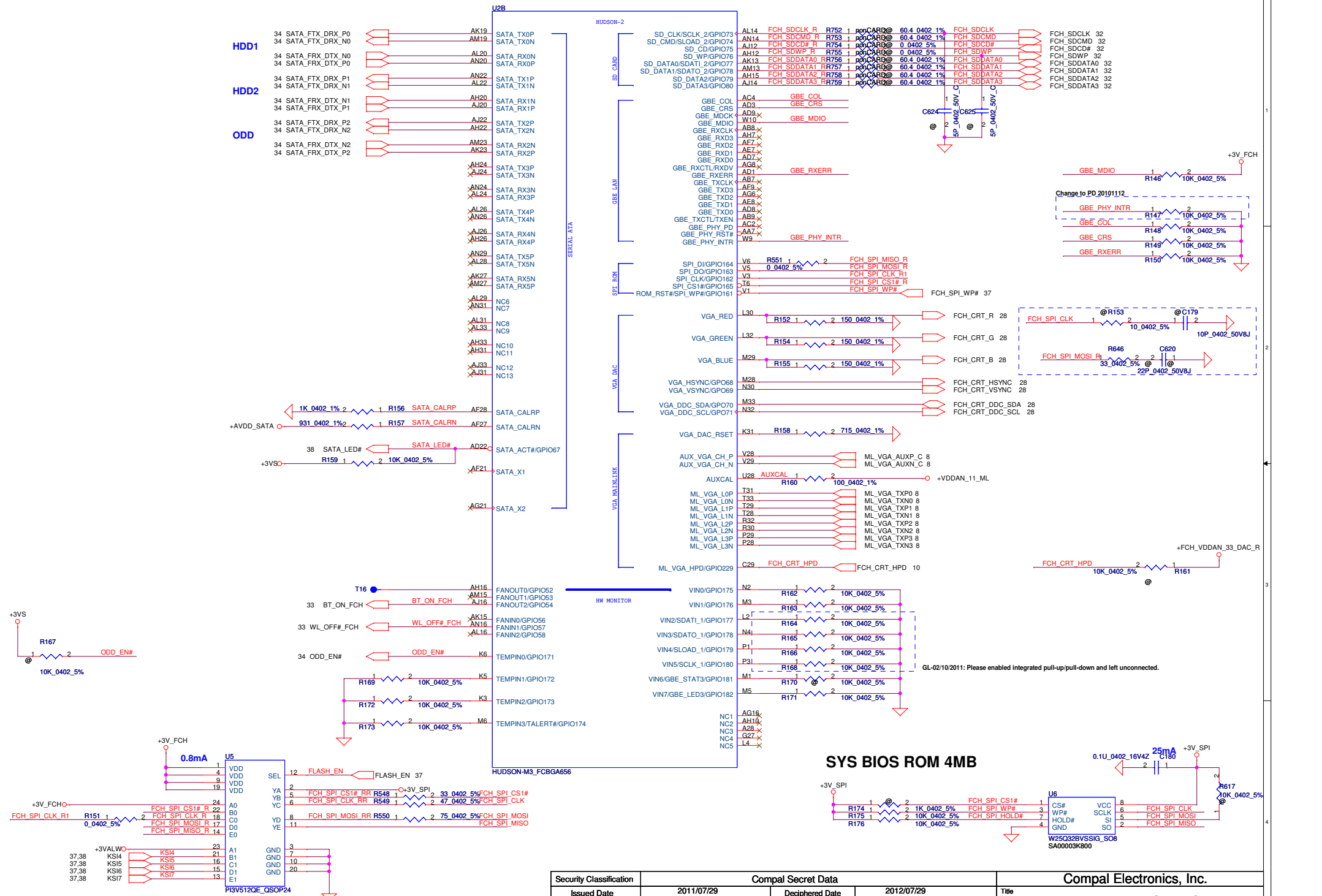


DIMM_B STD H:5.2mm
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		2012/07/29

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Title		
DDRIII SO-DIMM 2		
Size	Document Number	Rev
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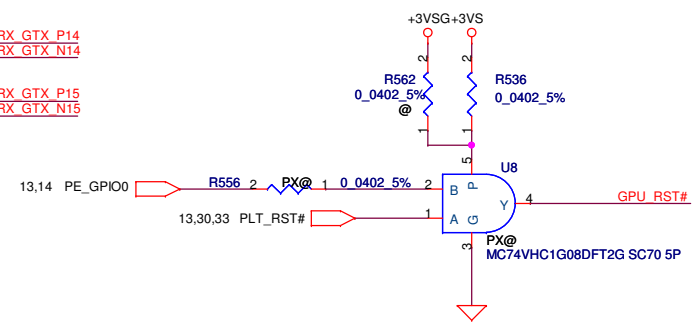
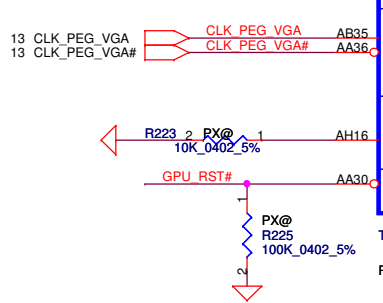
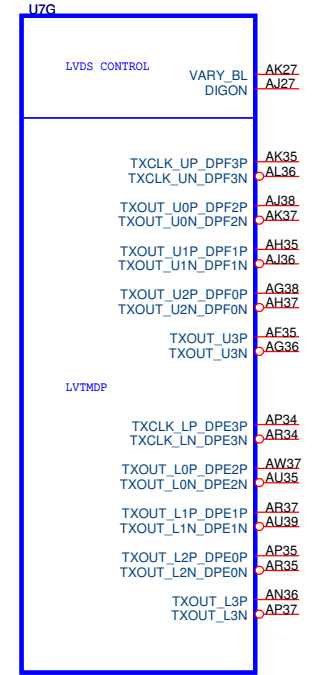
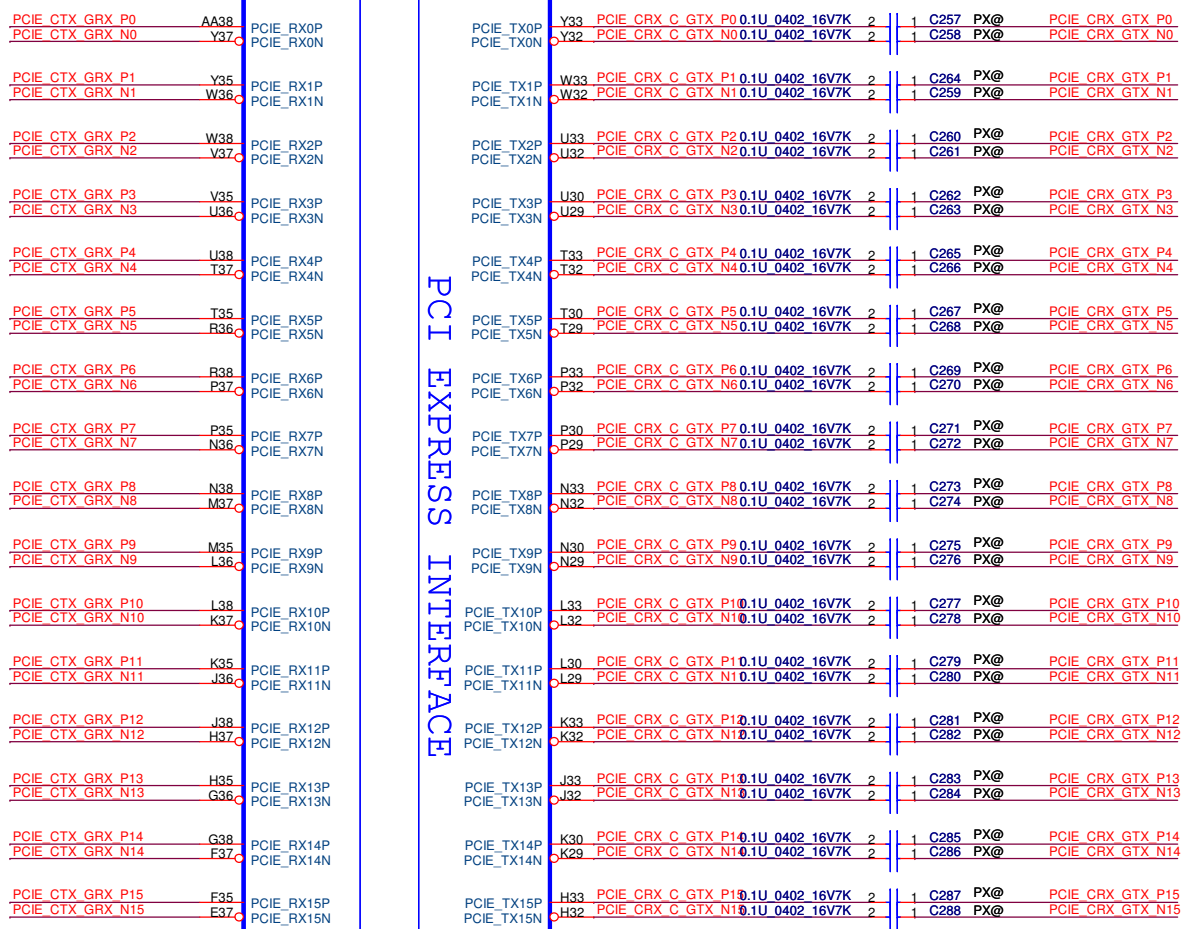
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6 PCIE_CTX_GRX_P[15..0] → PCIE_CTX_GRX_P[15..0]
 6 PCIE_CTX_GRX_N[15..0] → PCIE_CTX_GRX_N[15..0]

PCIE_CRX_GTX_P[15..0] → PCIE_CRX_GTX_P[15..0] 6
 PCIE_CRX_GTX_N[15..0] → PCIE_CRX_GTX_N[15..0] 6

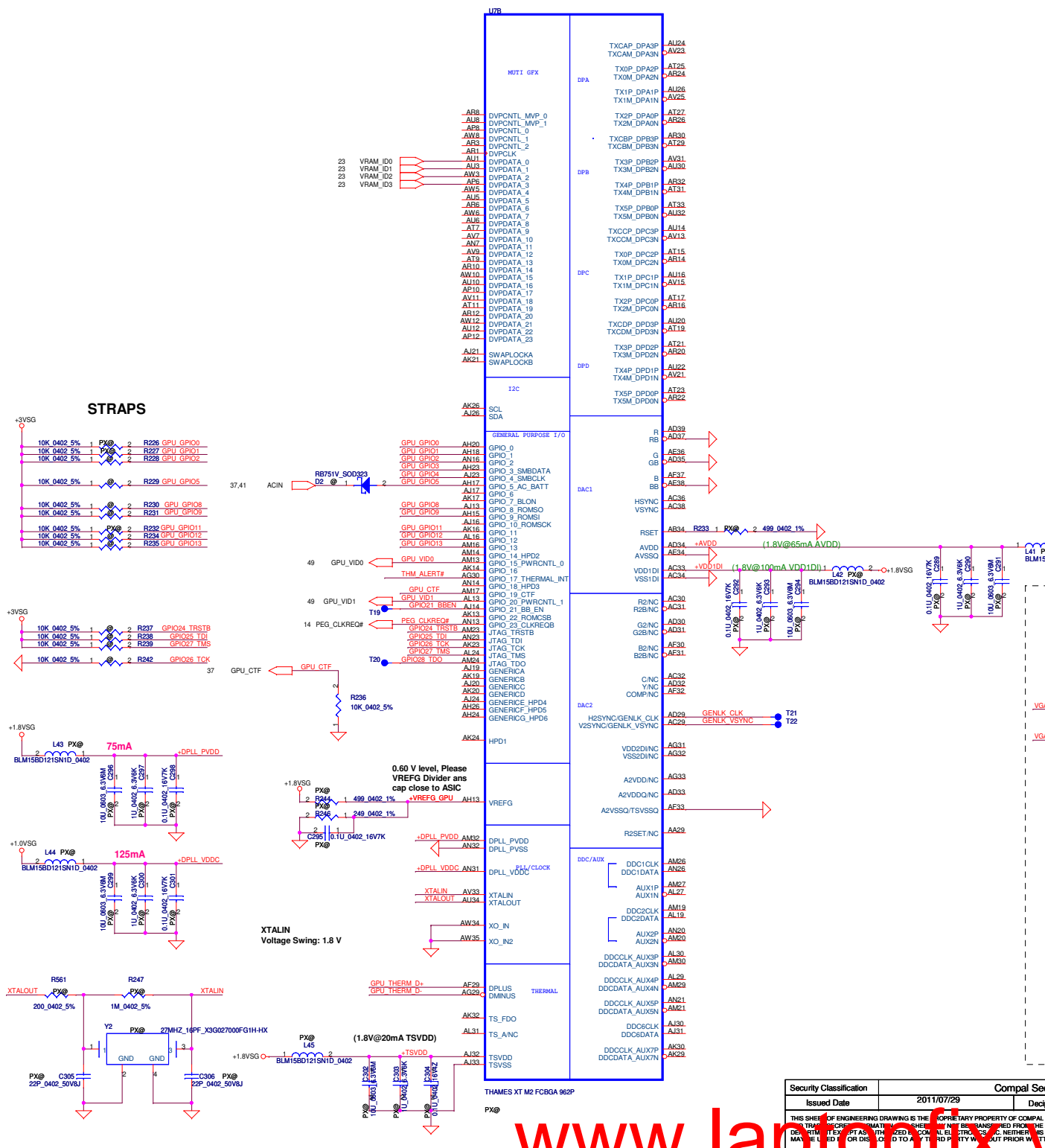
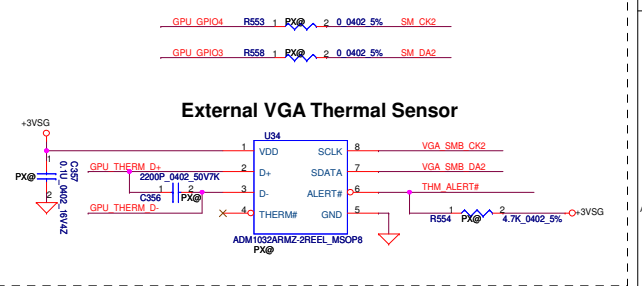
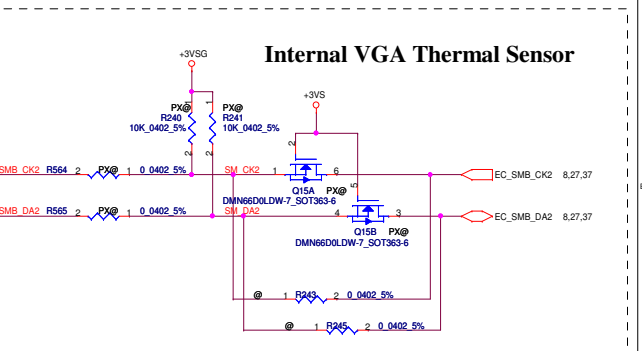
LVDS Interface

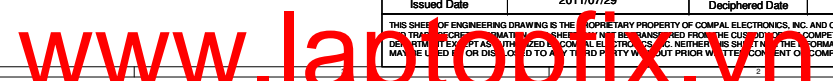
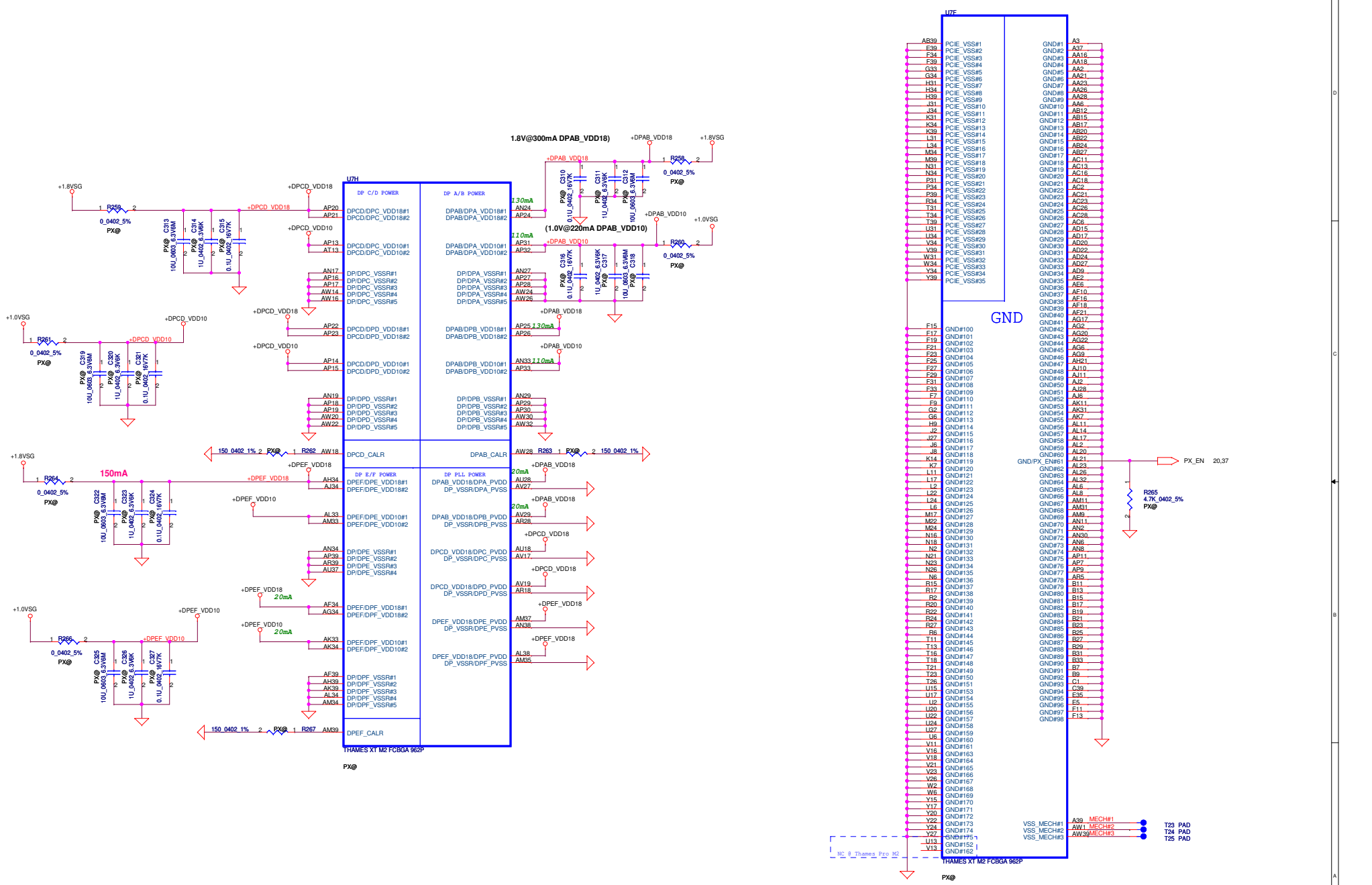


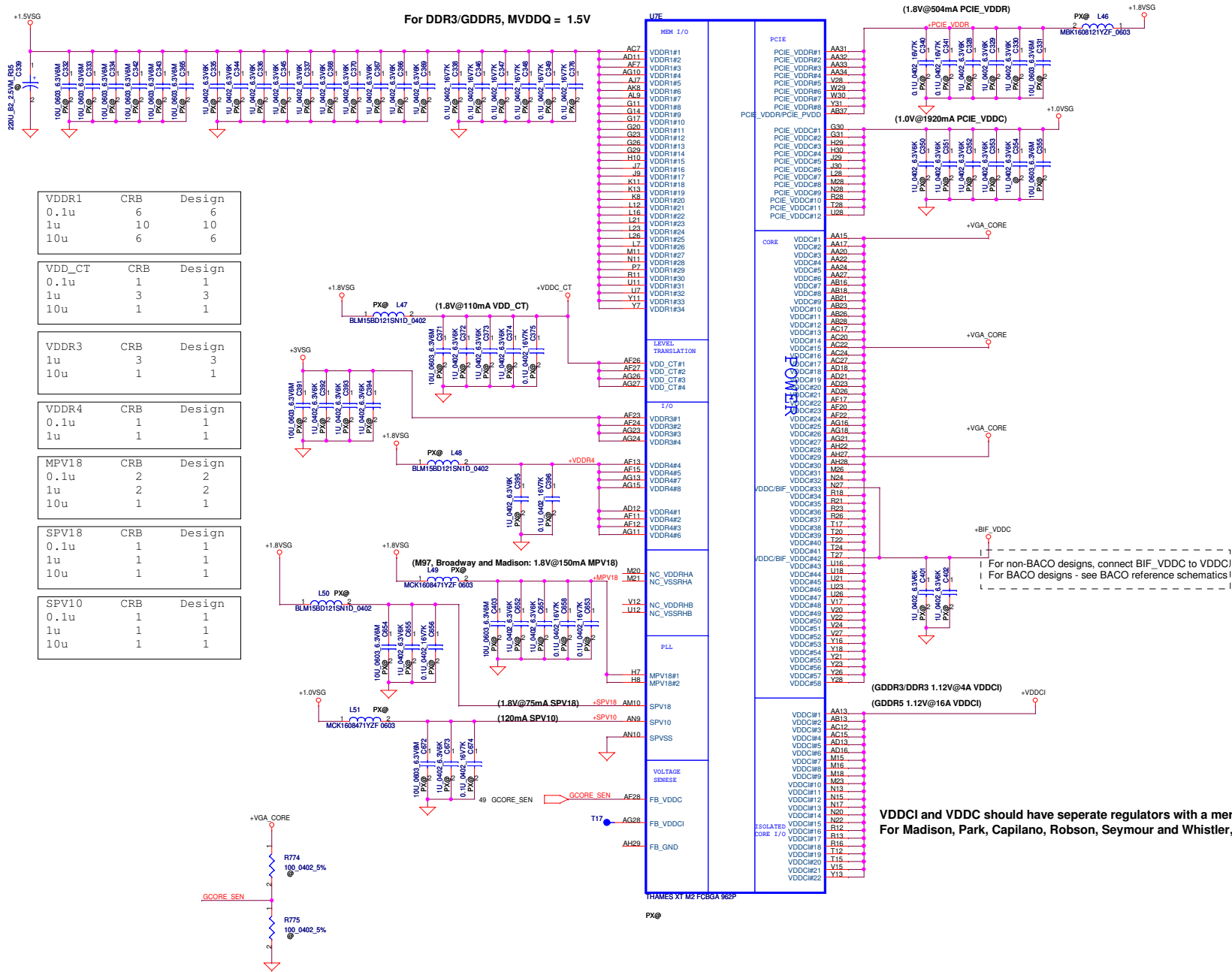
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Size B	Document Number	QML70 LA-8371P		Rev	0.2
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CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X= DESIGN DEPENDANT NA= NOT APPLICABLE			
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIe FULL TX OUTPUT SWING 0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS 0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIe speed when compliance test 0: 2.5Gt/s 1: 5Gt/s	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1]	HSYNC	AUD[1] AUD[0] 0: 0 No audio function 0: 1 Audio for DisplayPort only 1: 0 Audio for DisplayPort and HDMI, if dongle is detected. 1: 1 Audio for both DisplayPort and HDMI	11
AUD[0]	VSYSN		

AMD RESERVED CONFIGURATION STRAPS ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET			
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	







For DDR3/GDDR5, MVDDQ = 1.5V

(1.8V@504mA PCIE_VDDR)

(1.0V@1920mA PCIE_VDDC)

(1.8V@110mA VDD_CT)

(M97, Broadway and Madison: 1.8V@150mA MPV18)

(1.8V@75mA SPV18)

(120mA SPV10)

(GDDR3/DDR3 1.12V@4A VDDCI)

(GDDR5 1.12V@16A VDDCI)

PCIE_VDDR	CRB	Design
0.1u	2	2
1u	3	3
10u	1	1

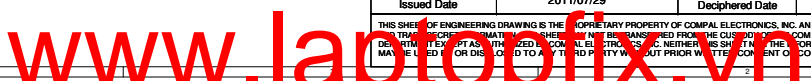
PCIE_VDDC	CRB	Design
1u	7	5 (1@)
10u	1	1

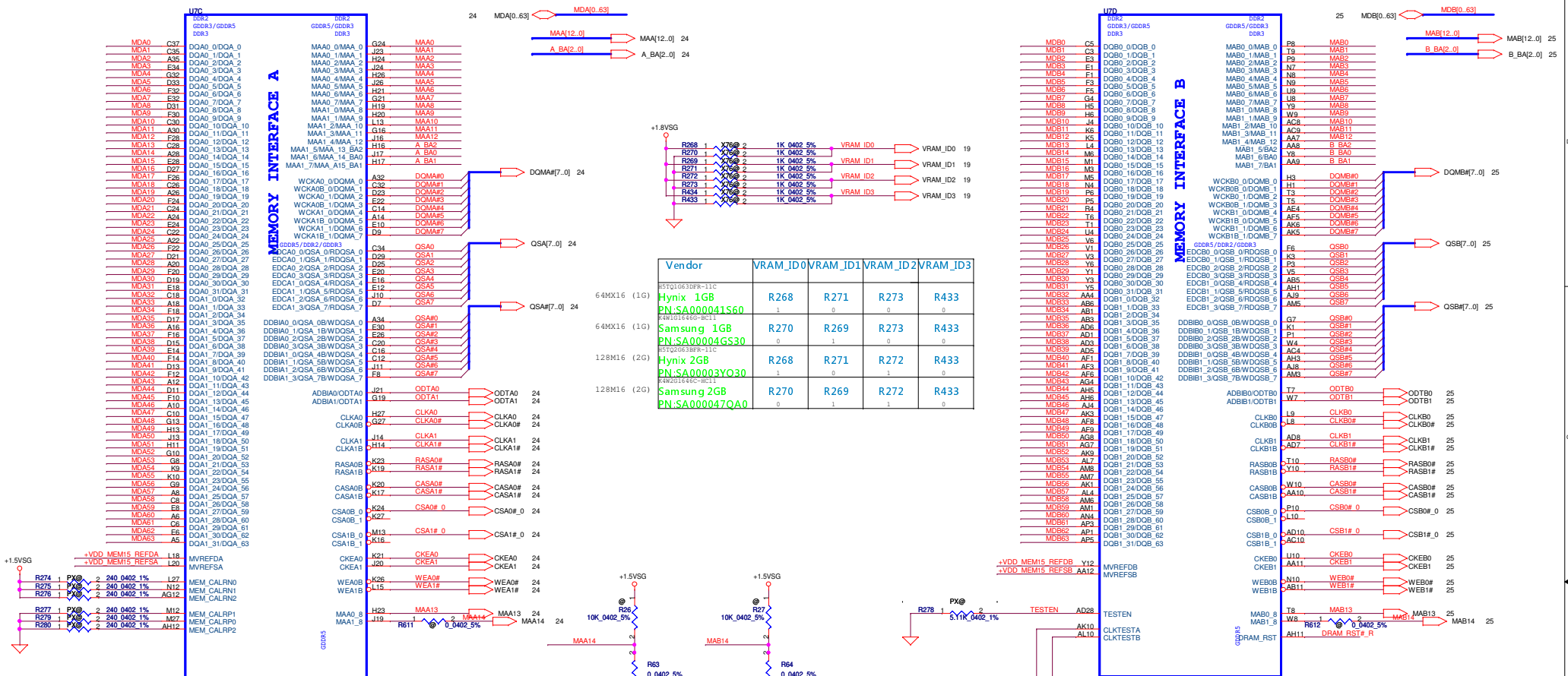
VDDC	CRB	Design
1u	30	30
10u	10	3
22u	0	1

VDDCI	CRB	Design
1u	10	10
10u	3	4 (3@)
22u	0	1

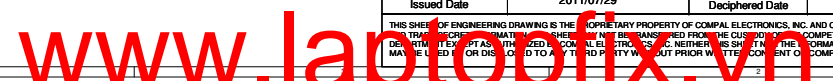
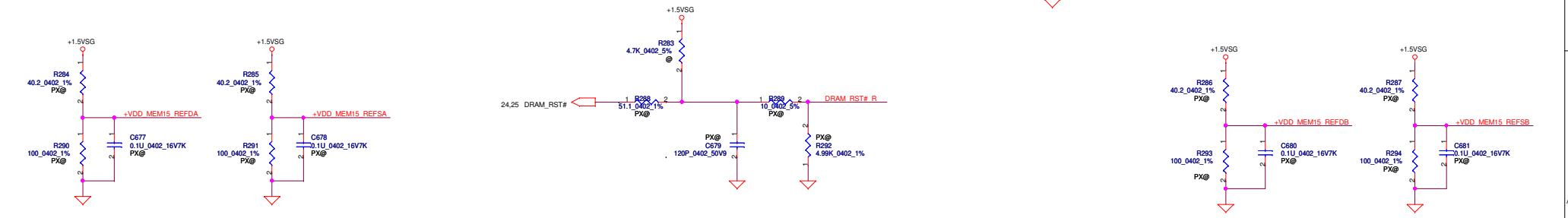
For non-BACO designs, connect BIF_VDDC to VDDCI
For BACO designs - see BACO reference schematics!

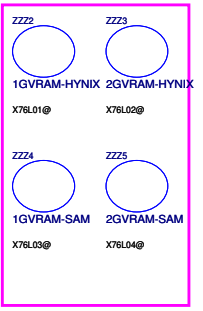
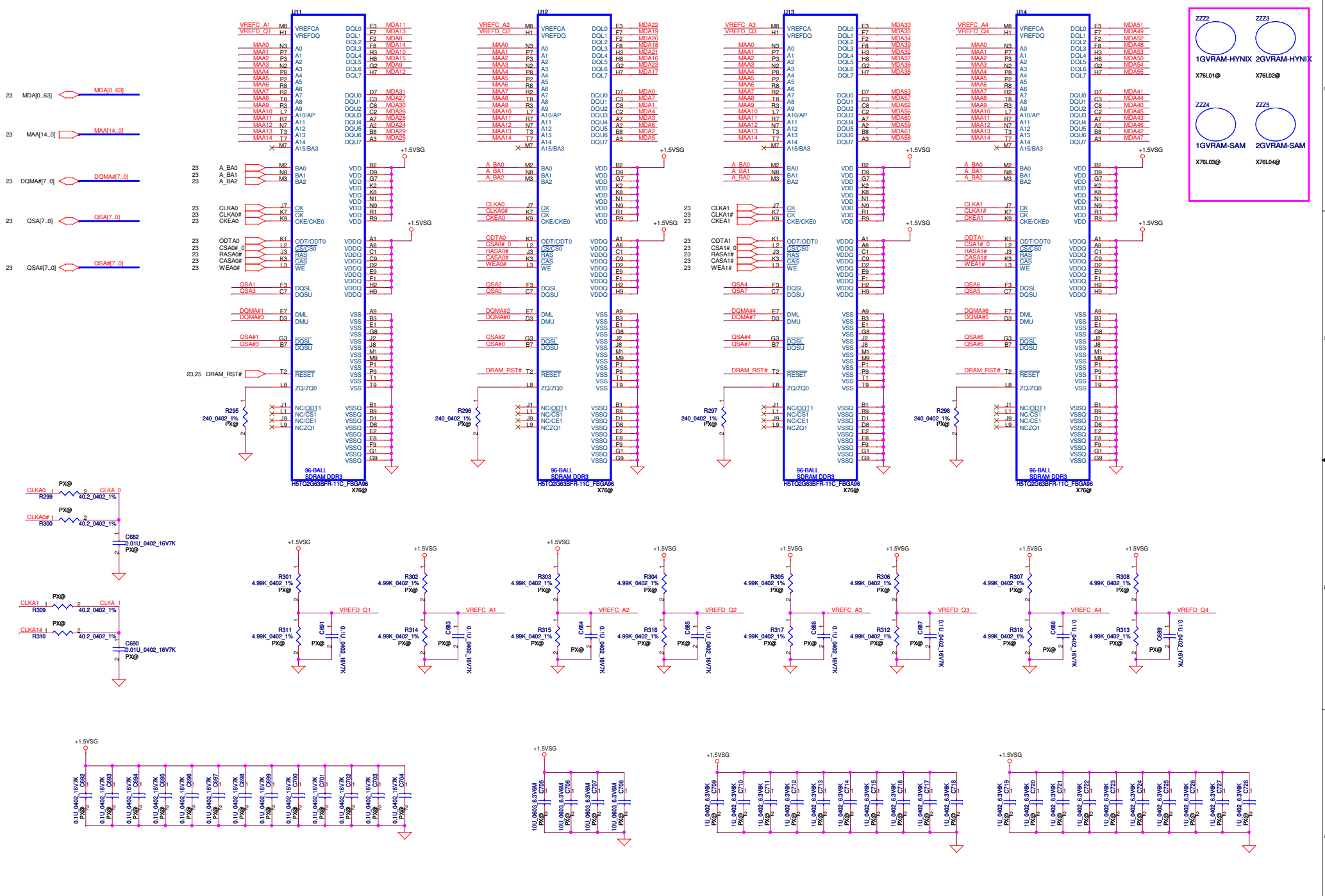
VDDCI and VDDC should have separate regulators with a merge option on PCB
For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator





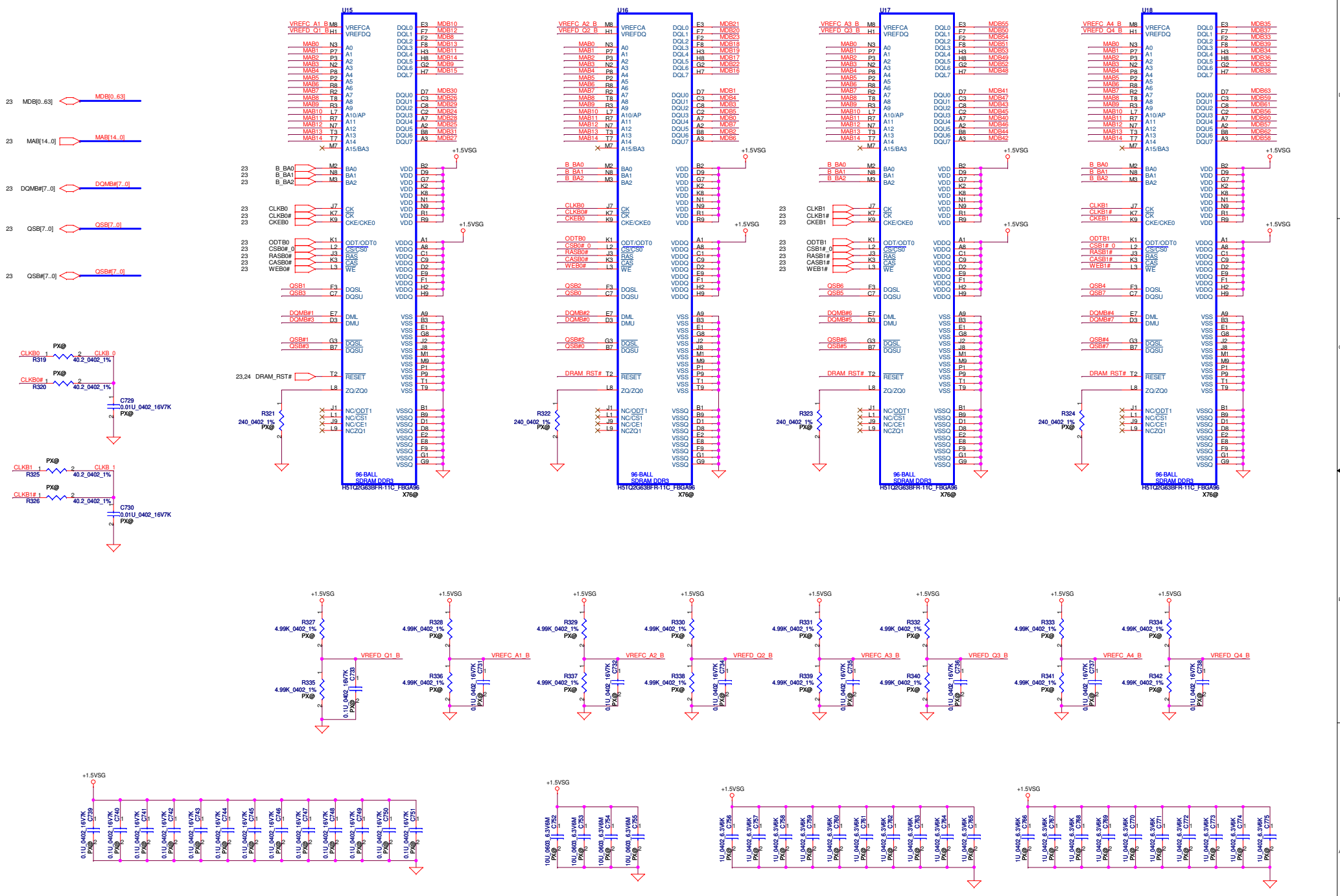
This basic topology should be used for DRAM_RST# for DDR3/GDDR5. These capacitors and Resistor values are an example only. The Series R and | Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except Rser2





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Size	Document Number	QML70-LA-8371P	Rev 0.2
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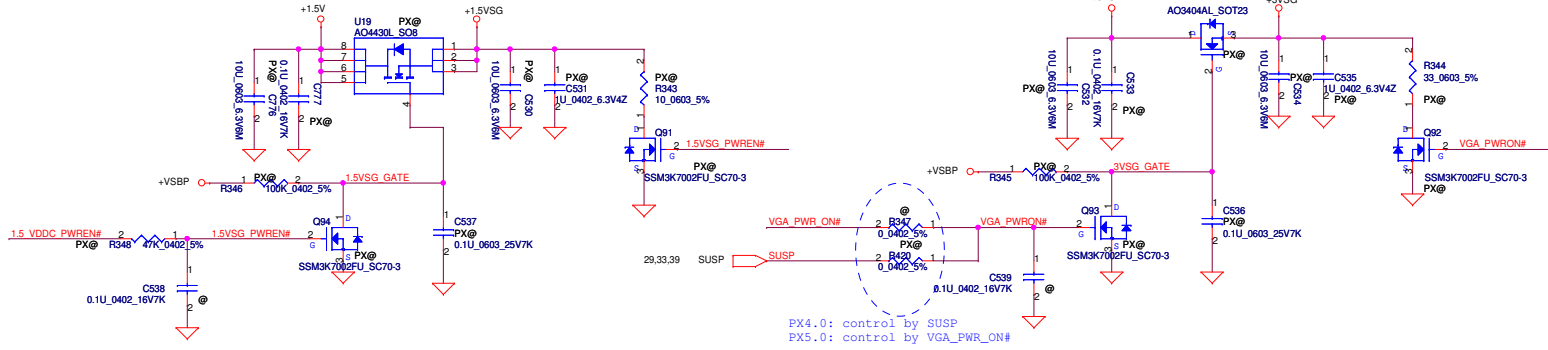
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Size	Document Number	QML70-LA-8371P	Rev 0.2
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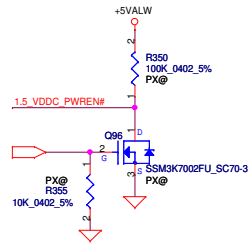
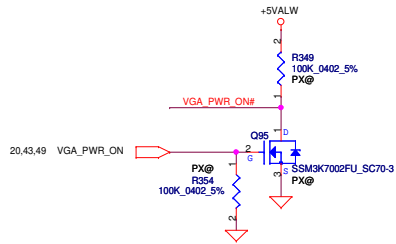
VGA Power

+1.5V to +1.5VSG (5.2A)

+3VS to +3VSG (60mA)

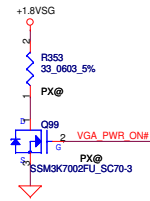
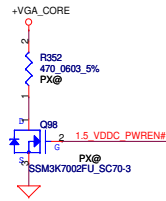
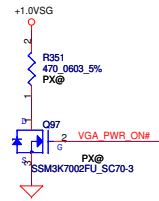


PX4.0: control by SUSP
PX5.0: control by VGA_PWR_ON#

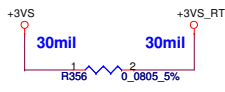


20.43.49 VGA_PWR_ON

20.49 1.5_VDD_PWREN

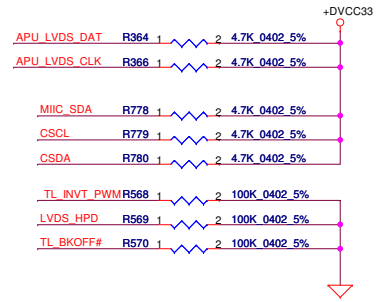
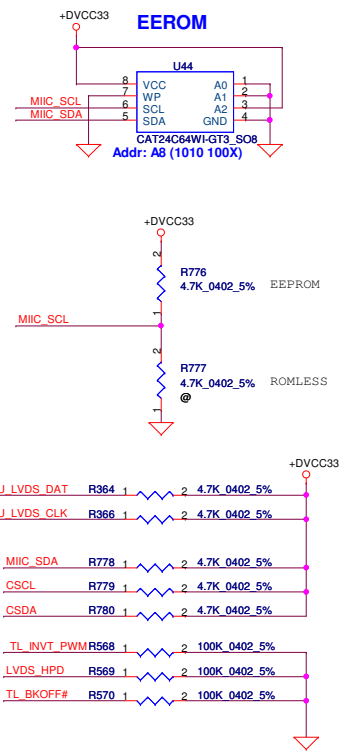
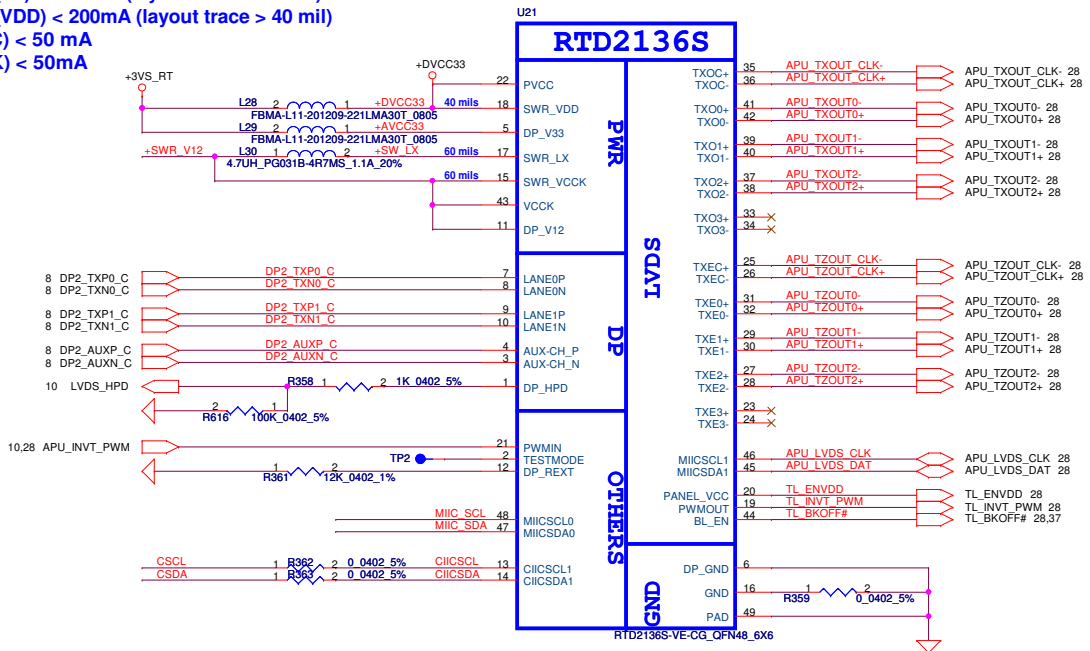
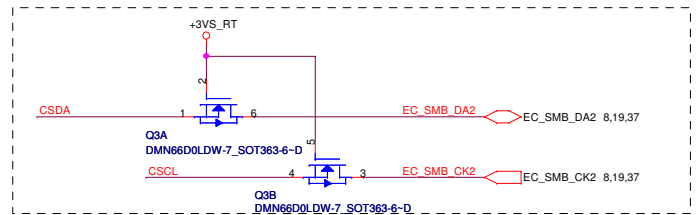
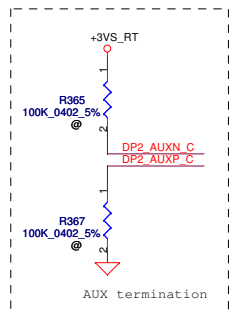
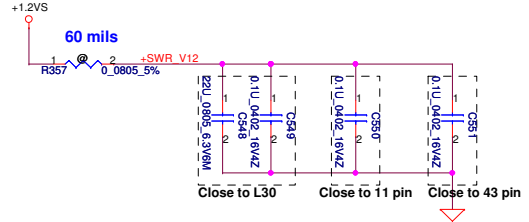
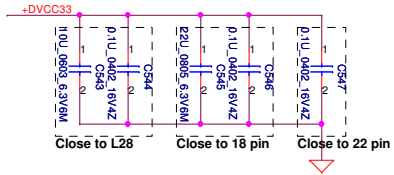
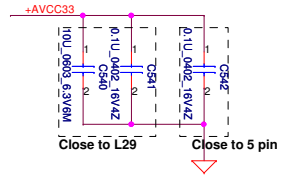


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Power Consumption:

- Pin5 (DPV33) < 20mA
- Pin 11 (DPV12) < 100mA
- Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)
- Pin 17 (SWR_LX) < 600mA (layout trace > 60 mil)
- Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)
- Pin 22 (PVCC) < 50 mA
- Pin 43 (VCCK) < 50mA



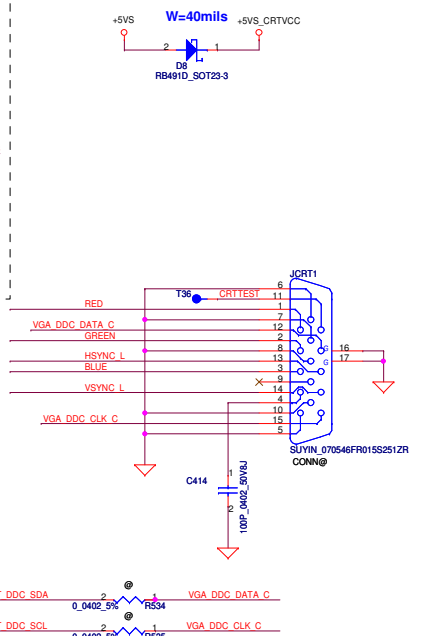
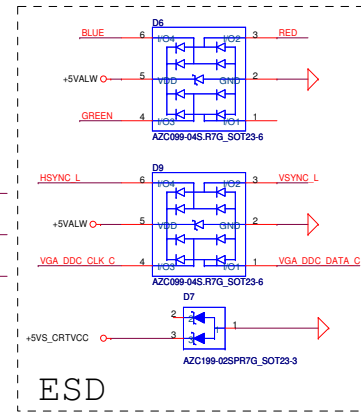
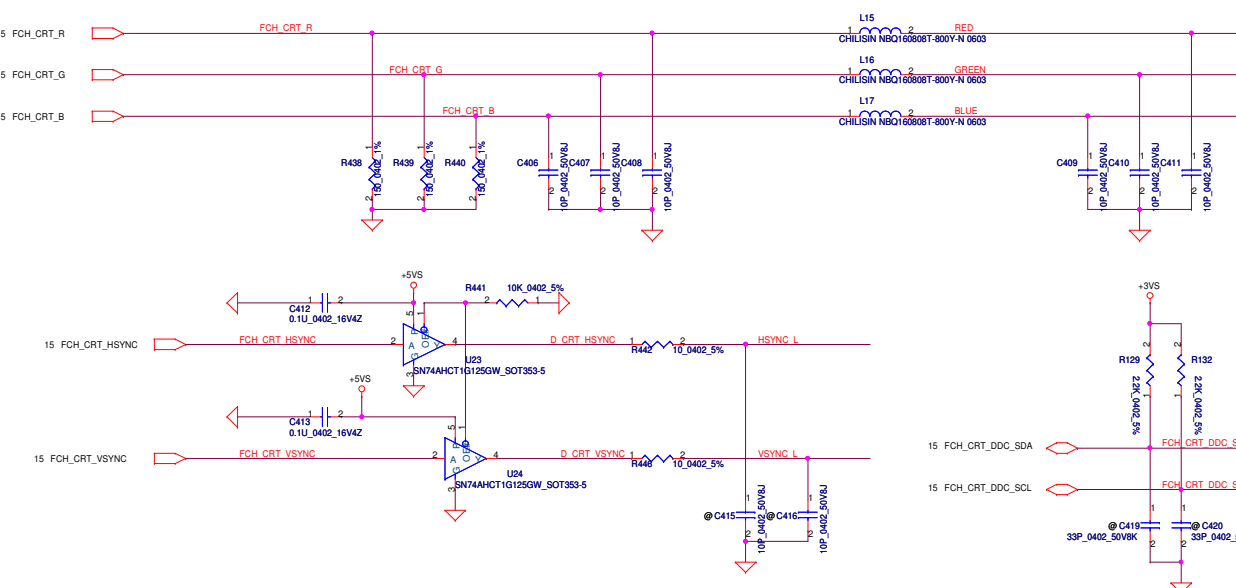
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		2012/07/29

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Title LVDS Translator - RTD2132S			
Size	Document Number	Rev	
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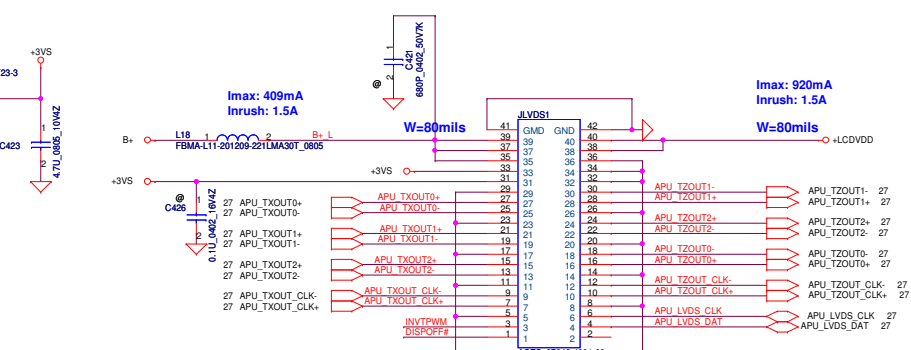
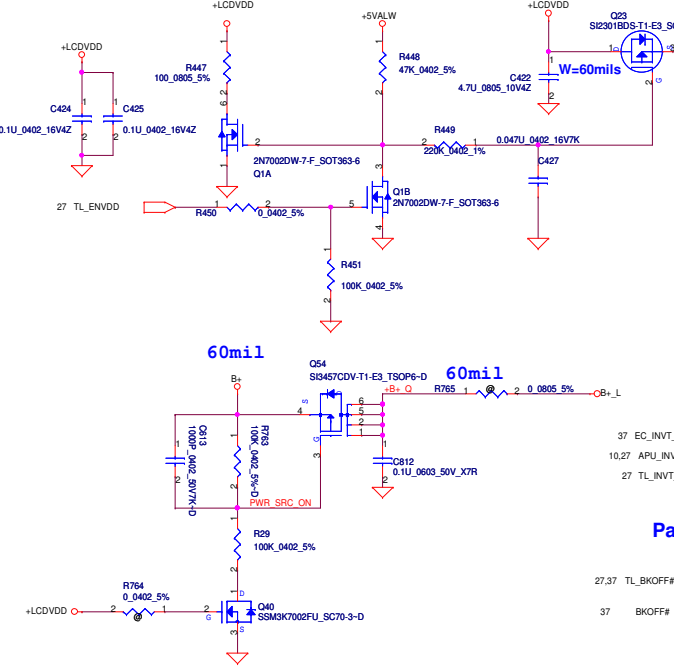
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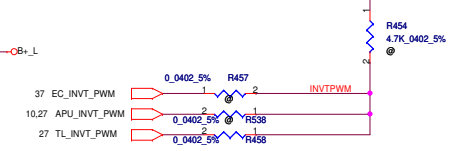
CRT



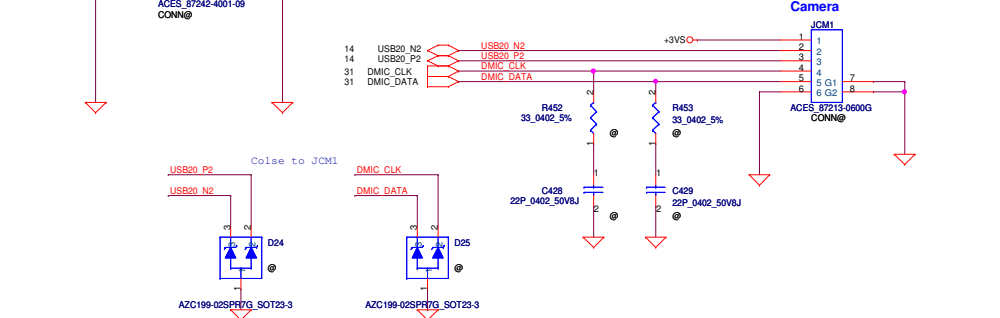
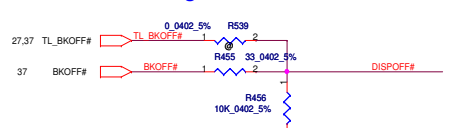
LCD POWER CIRCUIT



Panel PWM Control

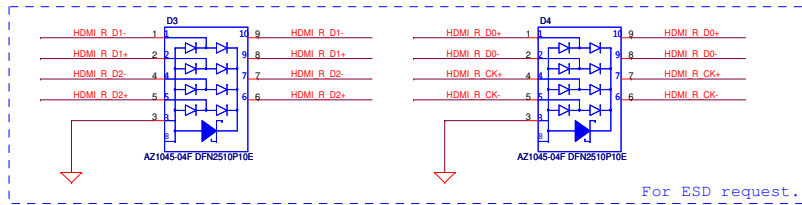


Panel Backlight Control

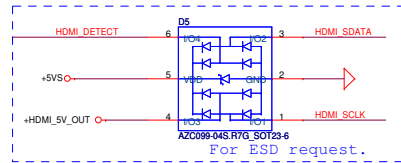


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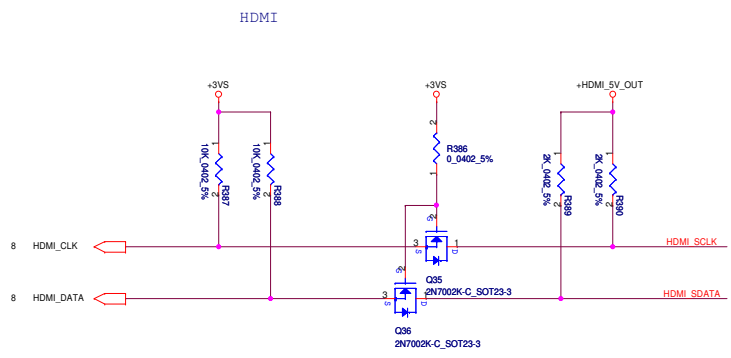
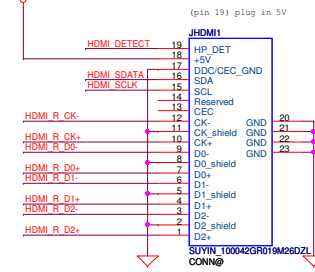
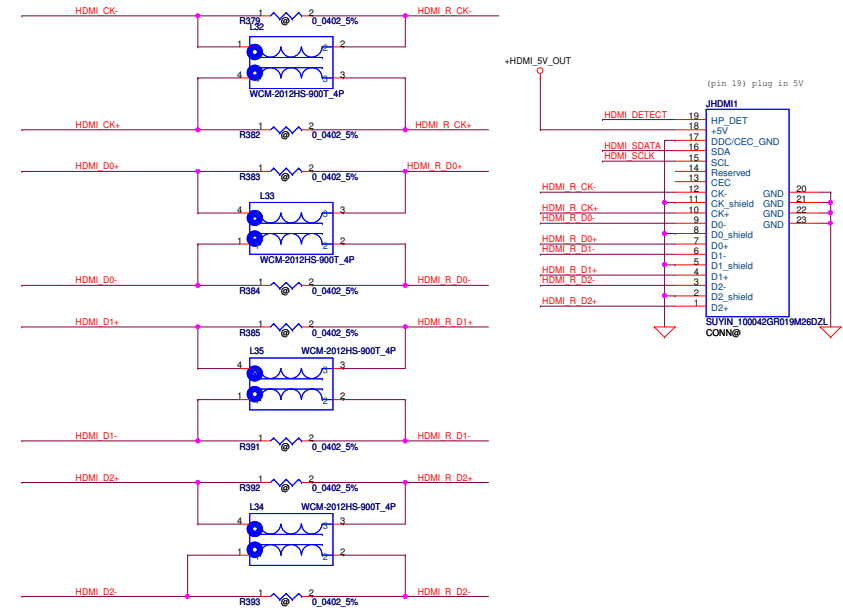
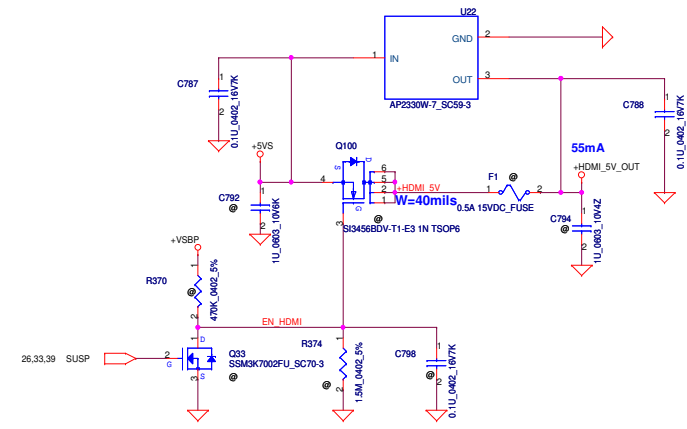
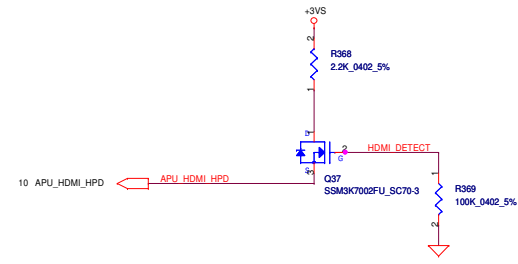
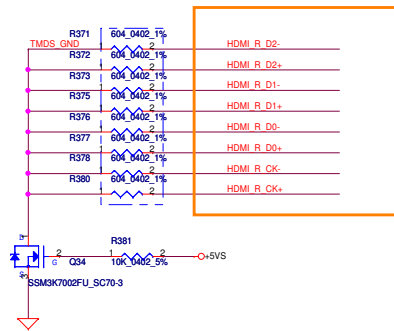


For ESD request.



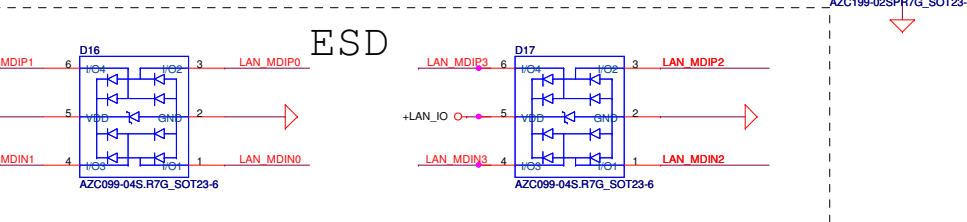
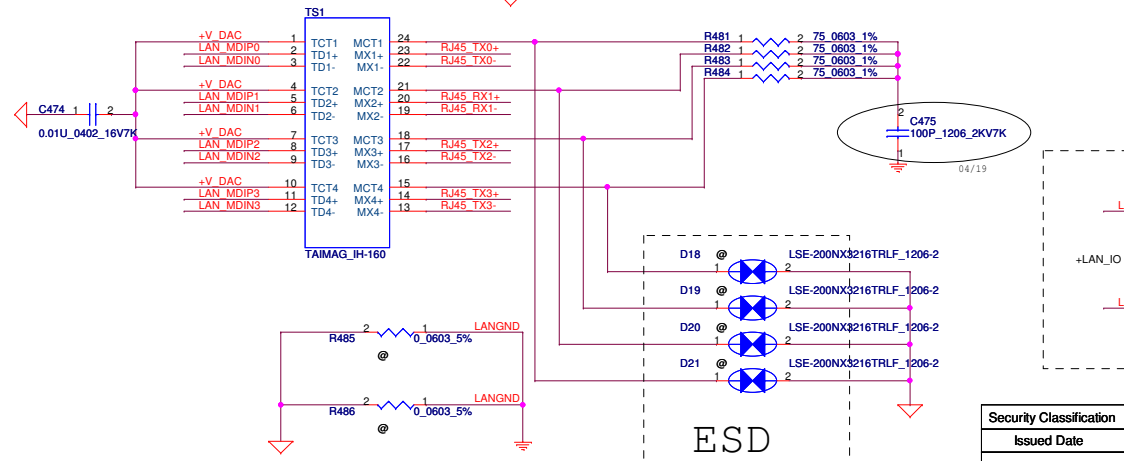
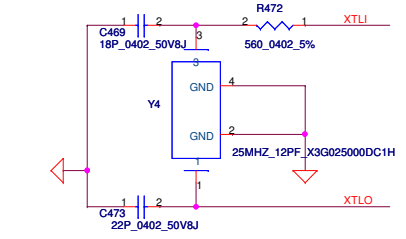
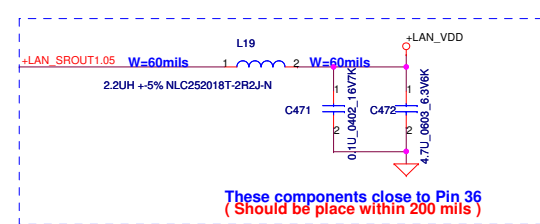
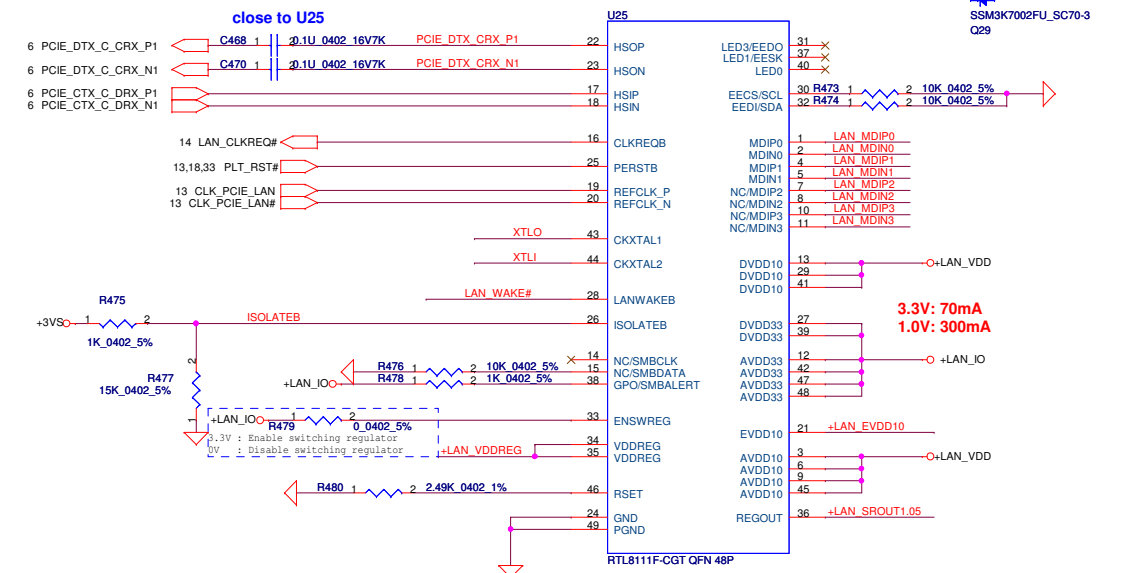
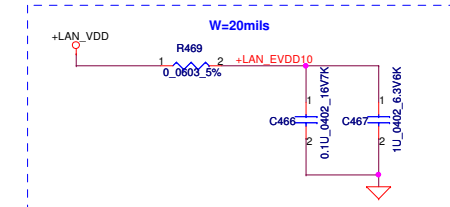
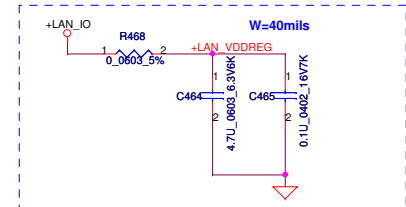
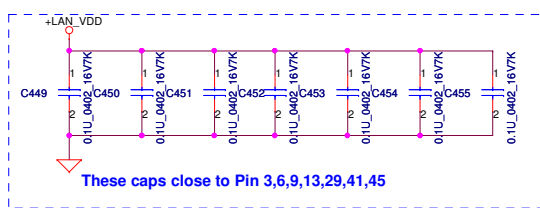
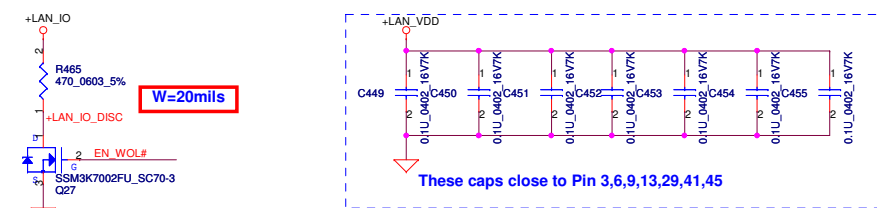
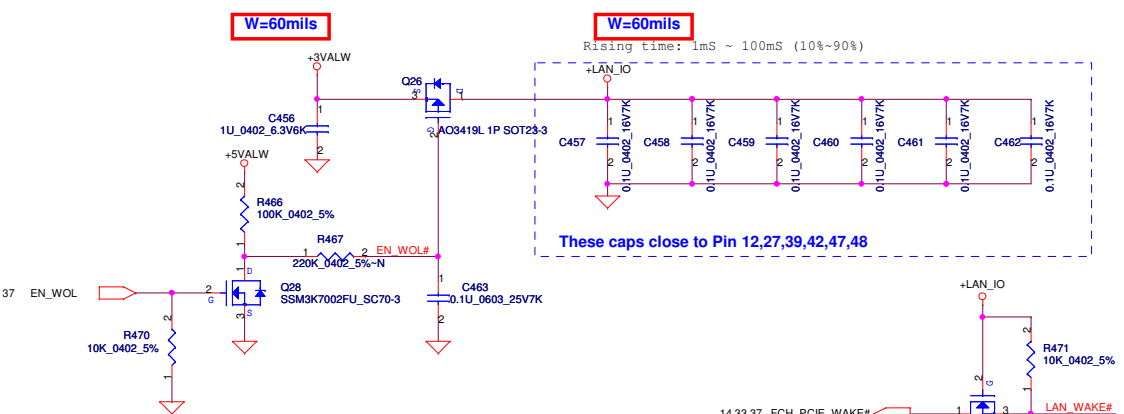
For ESD request.

8	HDMI_CLKP	HDMI_CLKP	0.1U_0402_16V7K	2	1	HDMI_CK+
8	HDMI_CLKN	HDMI_CLKN	0.1U_0402_16V7K	2	1	HDMI_CK-
8	HDMI_TX0P	HDMI_TX0P	0.1U_0402_16V7K	2	1	HDMI_D0+
8	HDMI_TX0N	HDMI_TX0N	0.1U_0402_16V7K	2	1	HDMI_D0-
8	HDMI_TX1P	HDMI_TX1P	0.1U_0402_16V7K	2	1	HDMI_D1+
8	HDMI_TX1N	HDMI_TX1N	0.1U_0402_16V7K	2	1	HDMI_D1-
8	HDMI_TX2P	HDMI_TX2P	0.1U_0402_16V7K	2	1	HDMI_D2+
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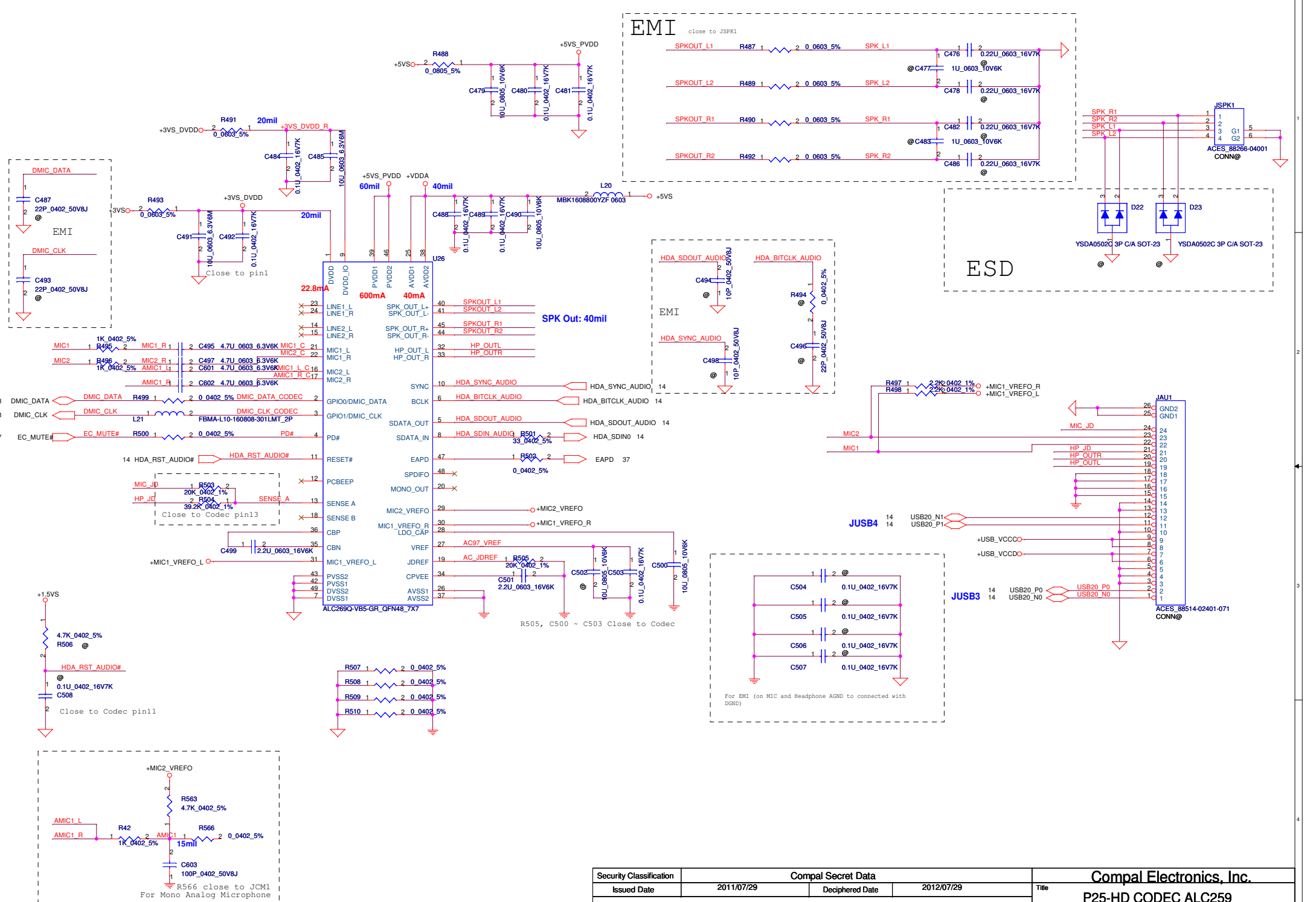


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		Date:	Wednesday, October 19, 2011	Sheet 30 of 53



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Issued Date	2011/07/29	Deciphered Date
		2012/07/29

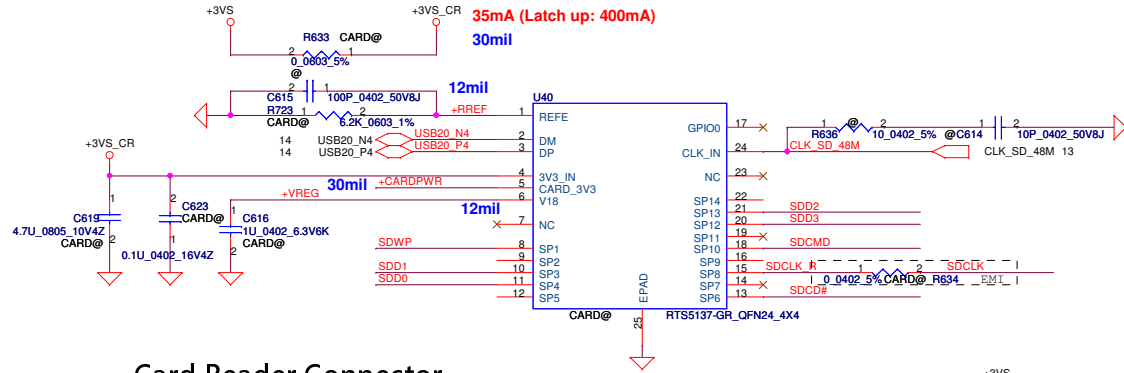
Title		
Compal Electronics, Inc.		
P25-HD CODEC ALC259		

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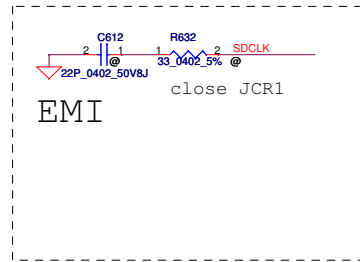
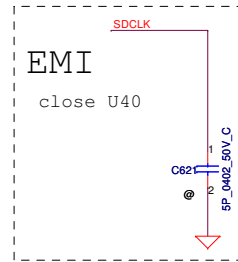
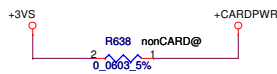
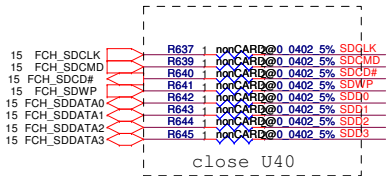
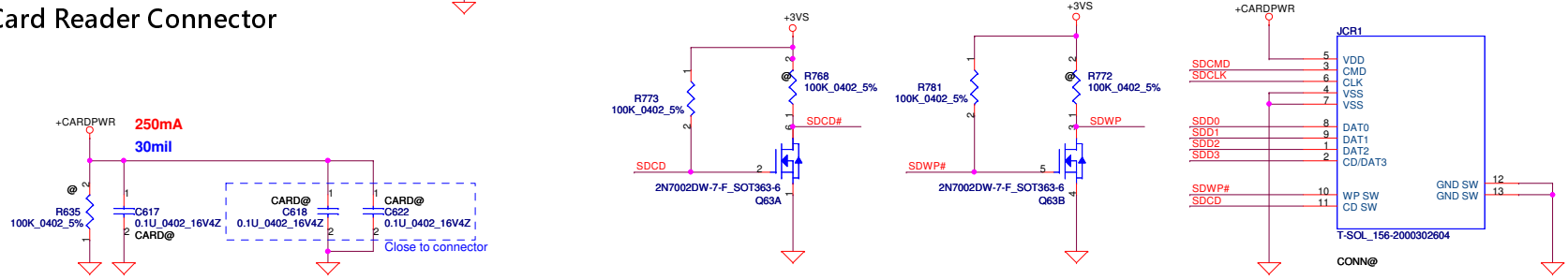
Size	Document Number	Rev
Customer	QML70 LA-8371P	0.2
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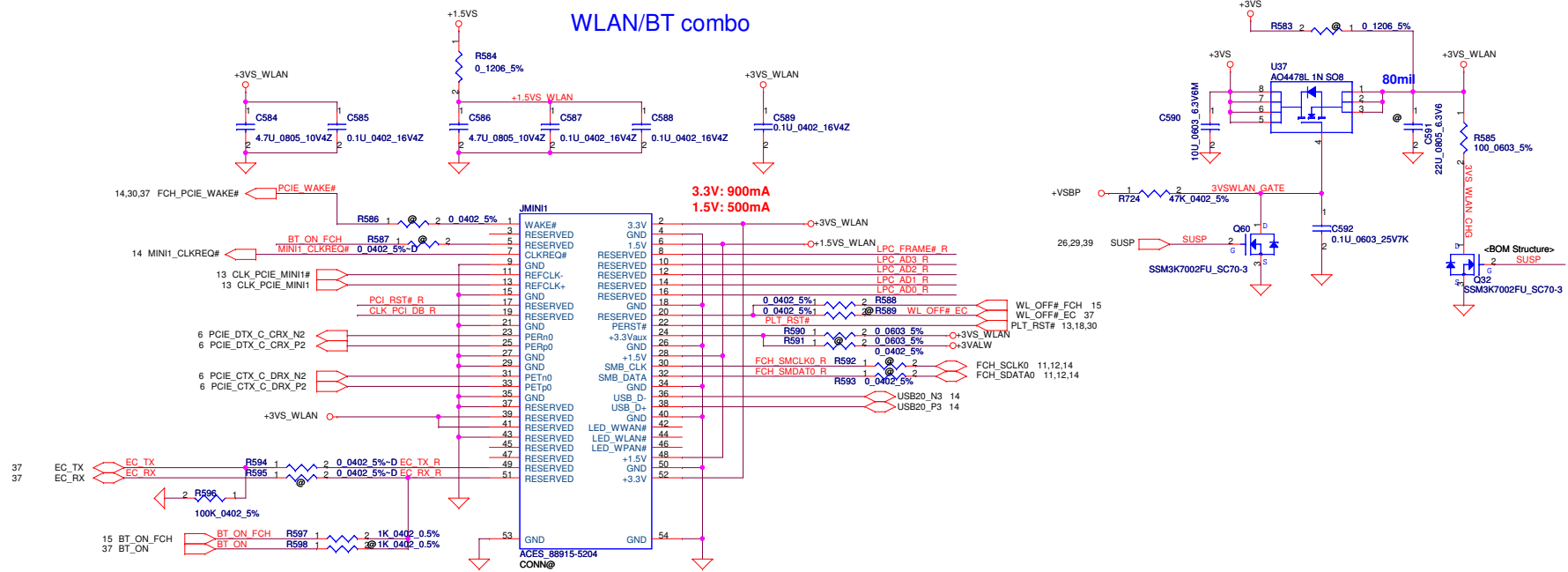
Card Reader RTS5137 (only SD/MMC/MS function)



Card Reader Connector



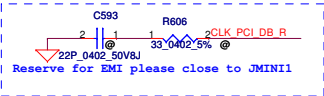
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Issued Date	2011/07/29	Deciphered Date	2012/07/29	Title	
				P26-RTS5137 Media Card Controller	
Size	Document Number			Rev	0.11
Custom	QML70 LA-8371P				
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5.2 mm High

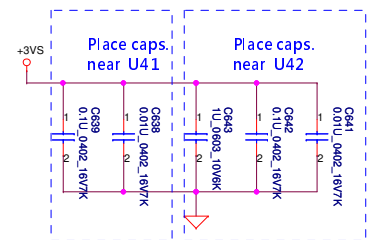
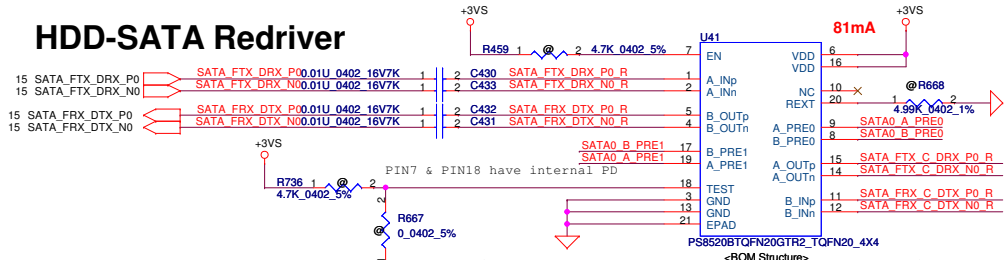
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME#_R	R599	1	2	0.0402 5%	LPC_FRAME#	13.37
LPC_AD3#_R	R600	1	2	0.0402 5%	LPC_AD3	13.37
LPC_AD2#_R	R601	1	2	0.0402 5%	LPC_AD2	13.37
LPC_AD1#_R	R602	1	2	0.0402 5%	LPC_AD1	13.37
LPC_AD0#_R	R603	1	2	0.0402 5%	LPC_AD0	13.37
PCI_RST#_R	R604	1	2	0.0402 5%	PLT_RST#	13.37
CLK_PCI_DB#_R	R605	1	2	0.0402 5%	CLK_PCI_DB	13

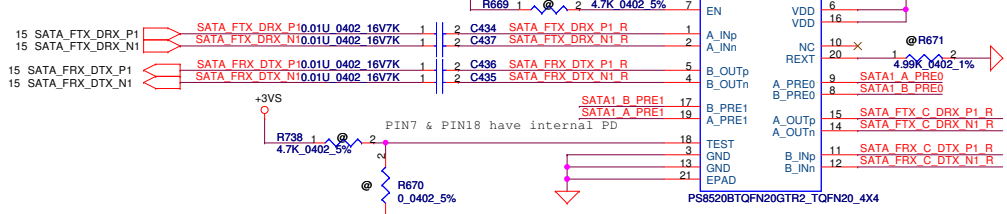


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Size Custom	Document Number	QML70 LA-837IP		Rev 0.2
Date:	Wednesday, October 19, 2011	Sheet	33	of 53

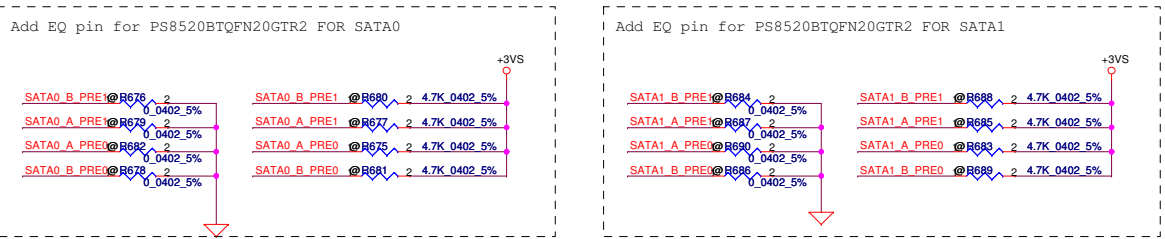
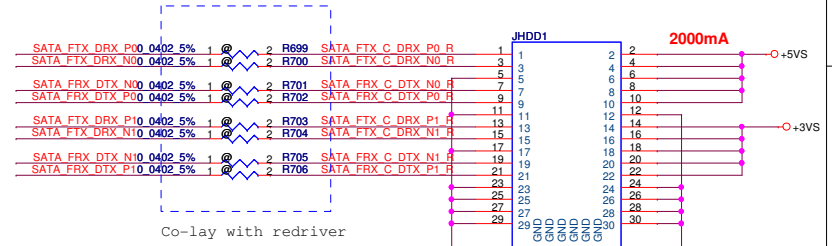
HDD-SATA Redriver



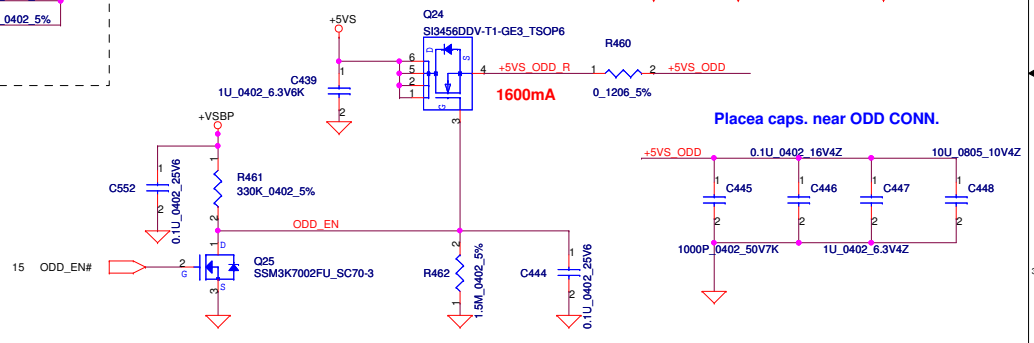
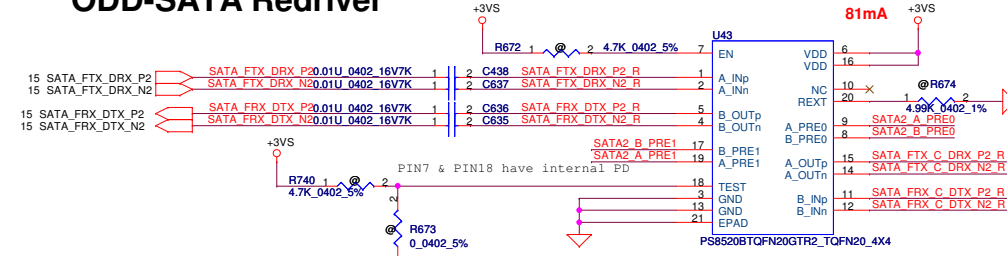
HDD-SATA Redriver



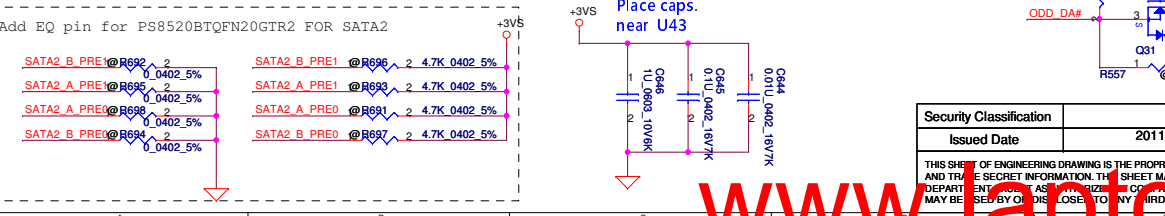
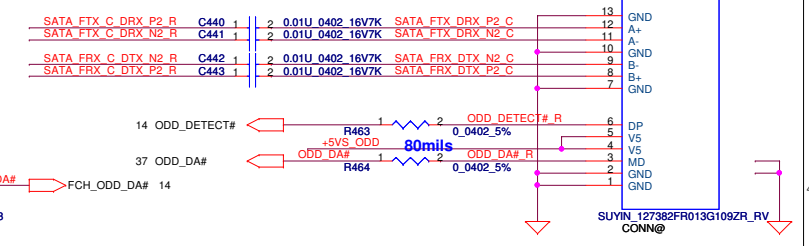
SATA HDD BTB Conn.



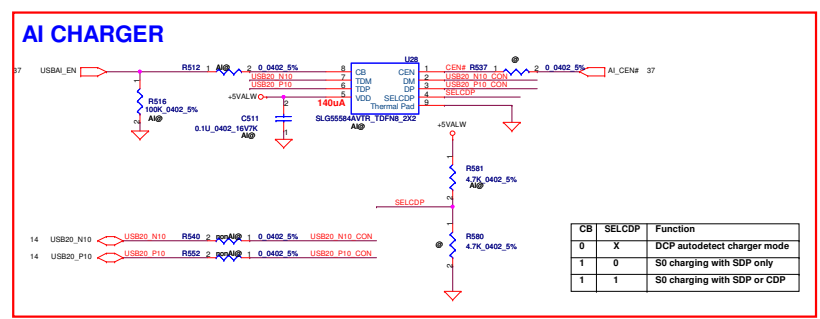
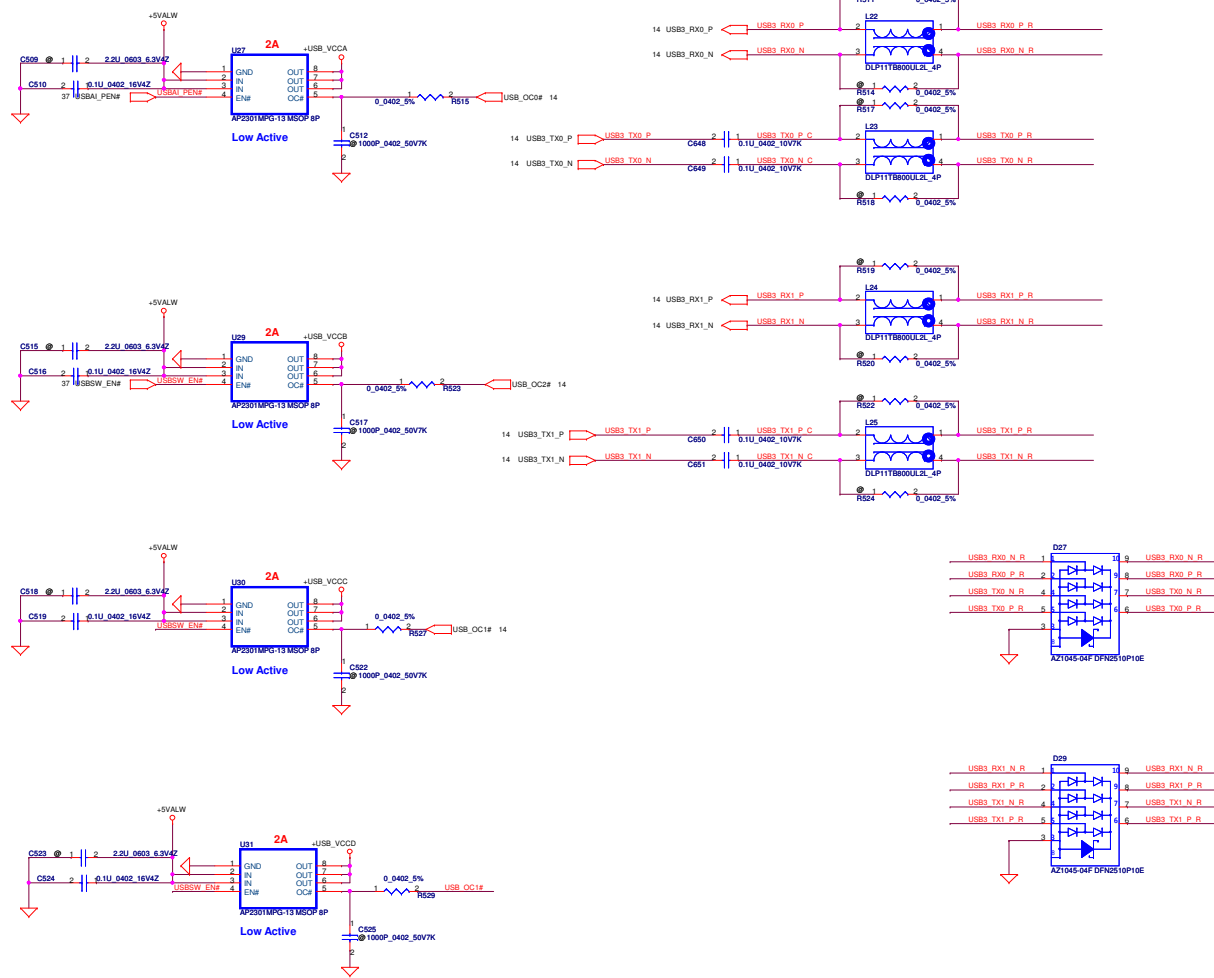
ODD-SATA Redriver



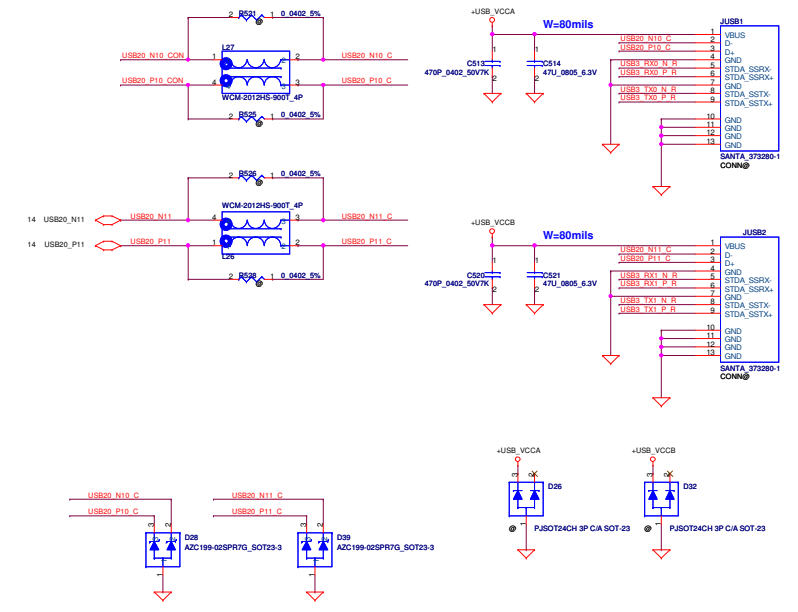
SATA ODD Conn.



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				P28-HDD & ODD CONN	
				QML70 LA-8371P	
				Date:	Wednesday, October 19, 2011
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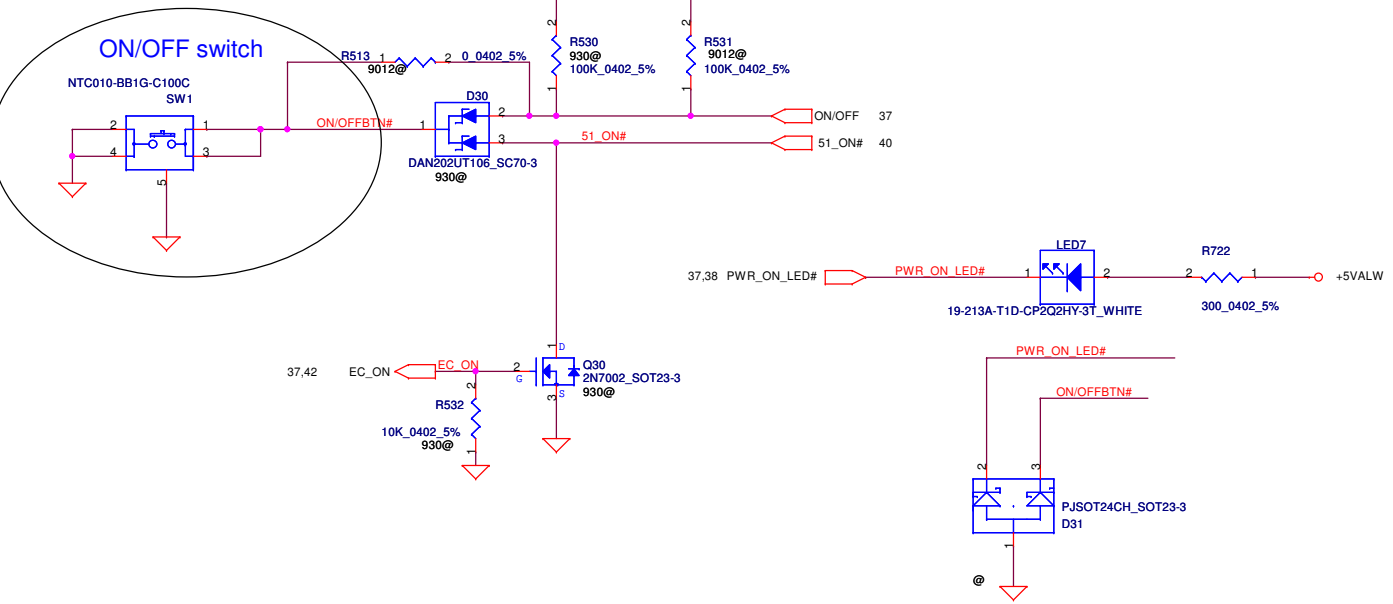


charger port: left side & near user

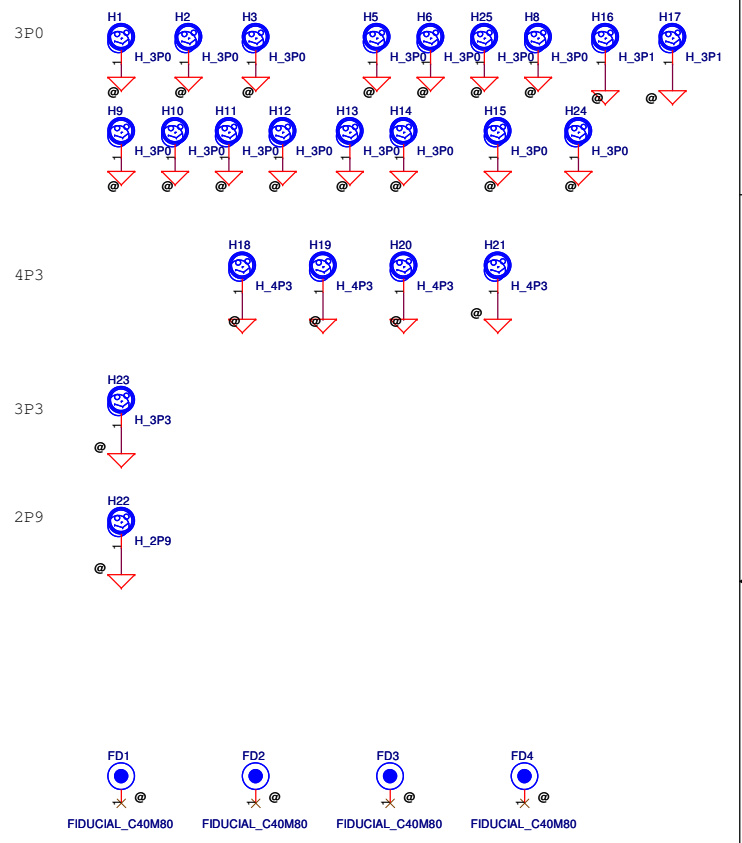


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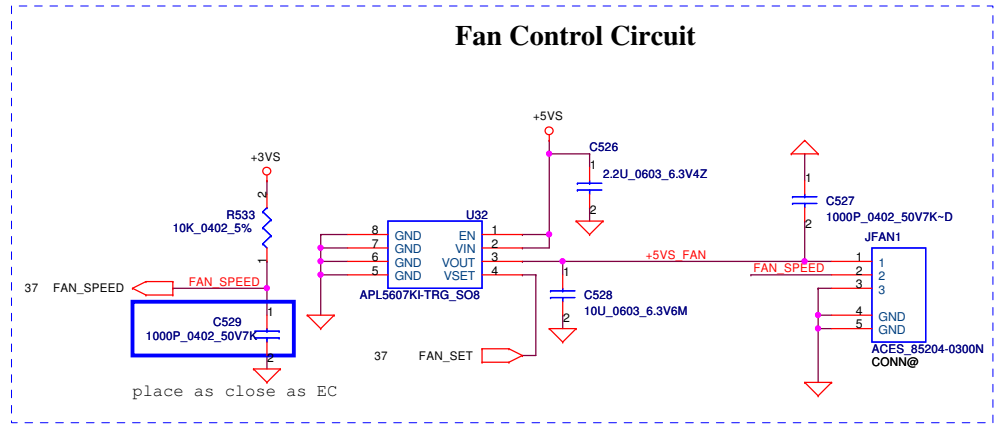
Power Button



Screw Hole

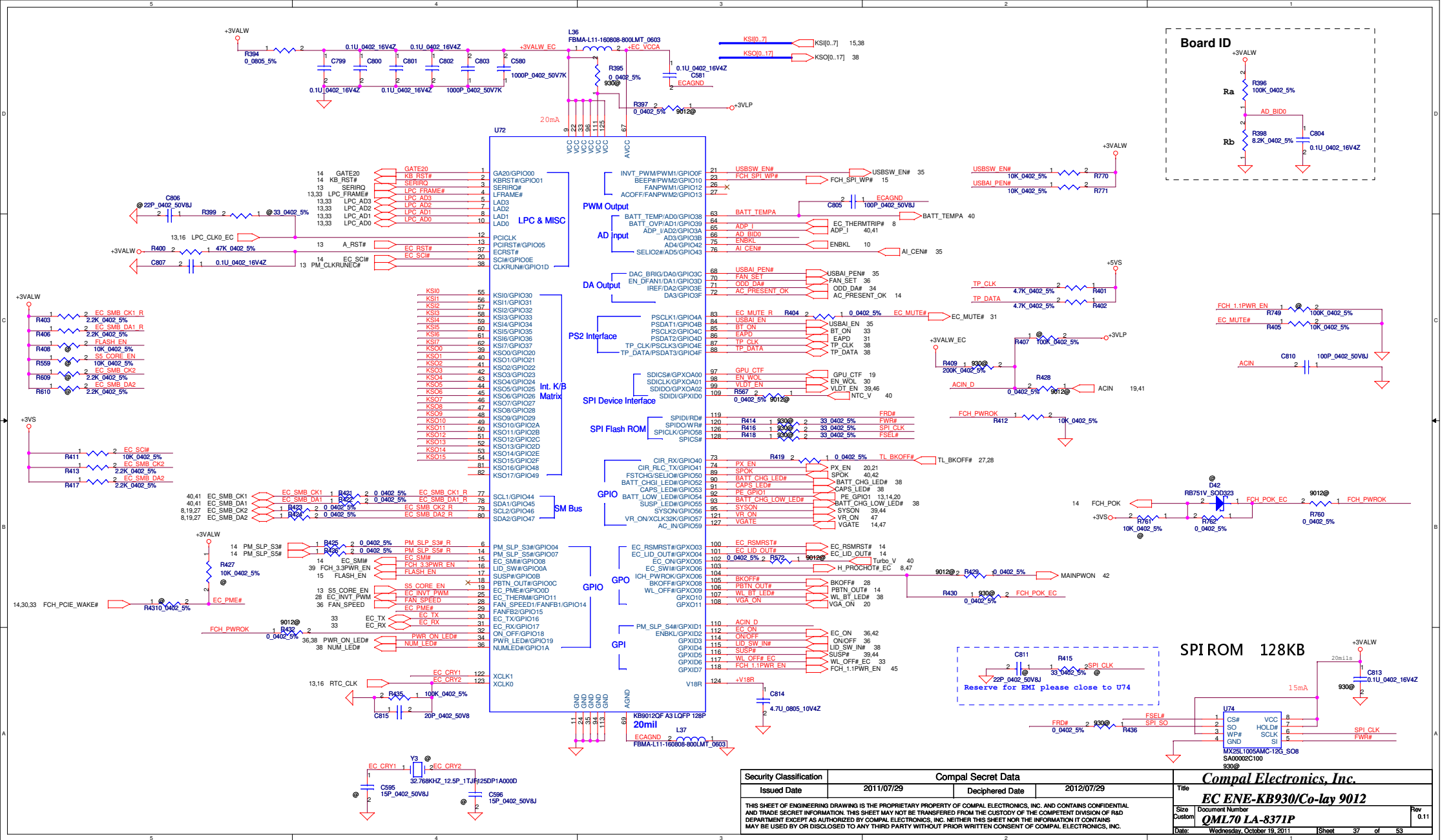


Fan Control Circuit

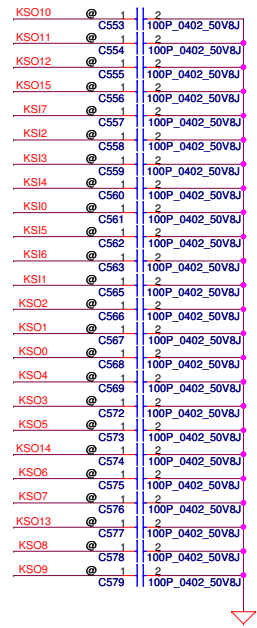


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Size	Document Number			Rev	0.11
Custom	QML70 LA-8371P			Date:	Wednesday, October 19, 2011
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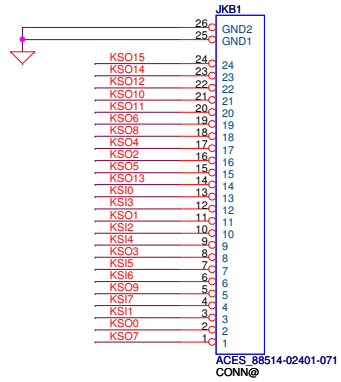
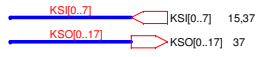
www.iaplofix.vn



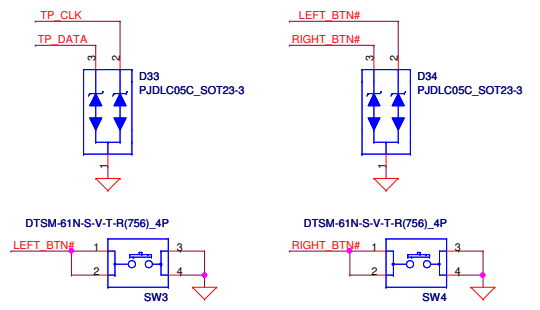
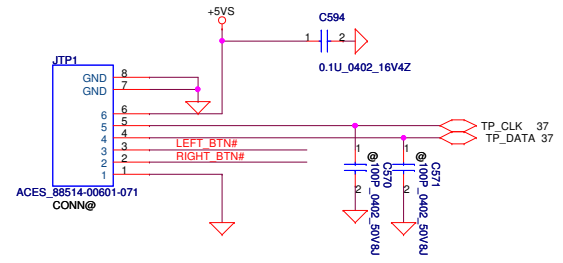
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Issued Date	2011/07/29	Deciphered Date	2012/07/29
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Title		Compal Electronics, Inc.	
Document Number		EC ENE-KB930/Co-lay 9012	
Size	Custom	Revision	0.11
Date: Wednesday, October 19, 2011		Sheet 37 of 53	



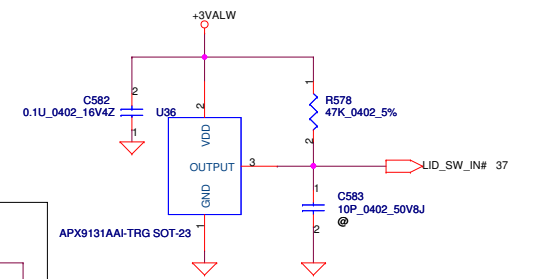
INT_KBD Conn.



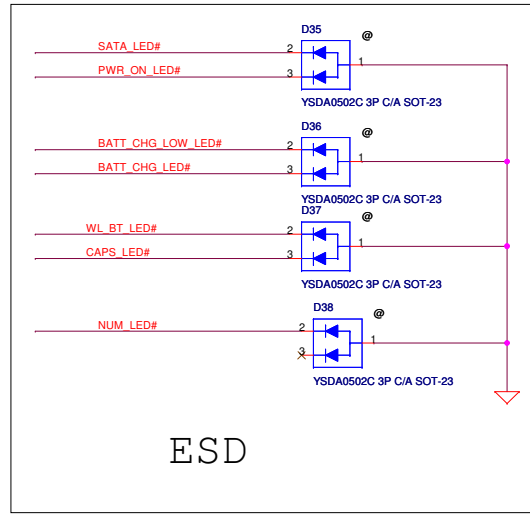
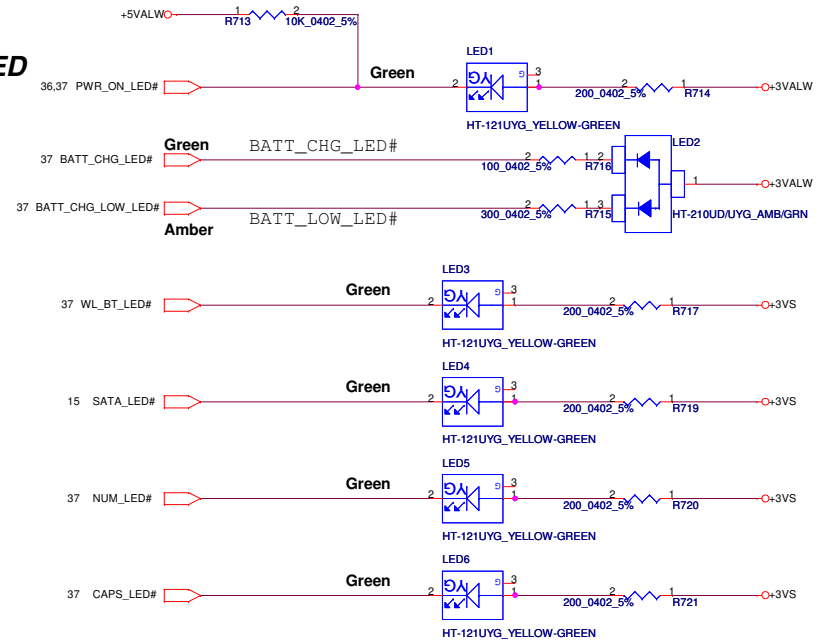
Touch/B Connector



Lid Switch (Hall Effect Switch)

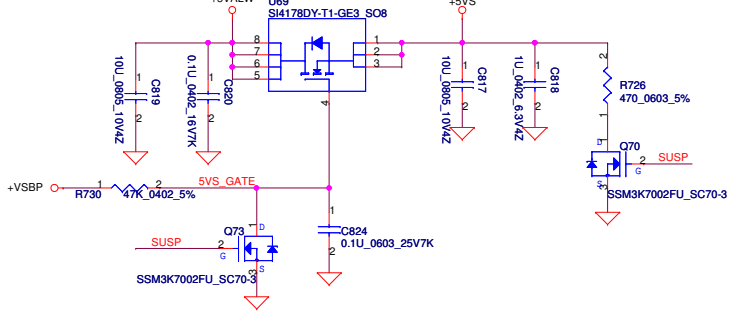


LED

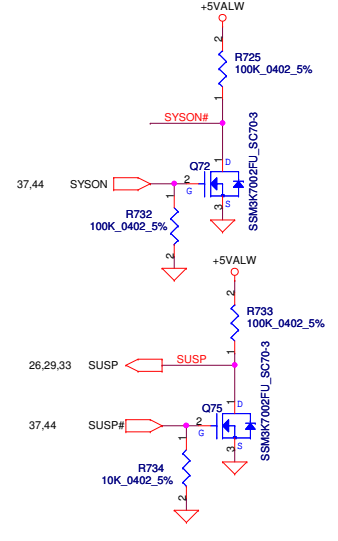
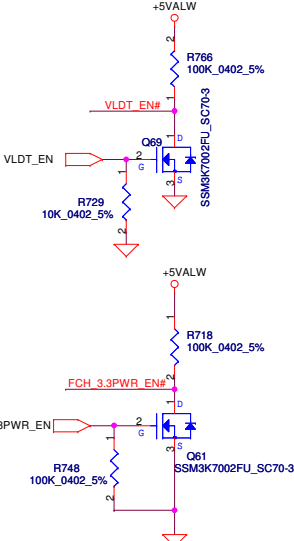
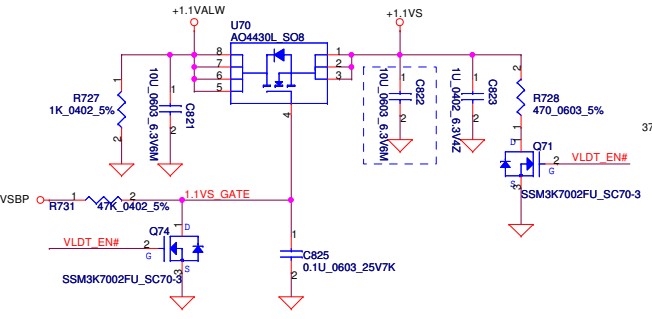


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Size	Rev	Sheet	of	53
3	0.2	38		

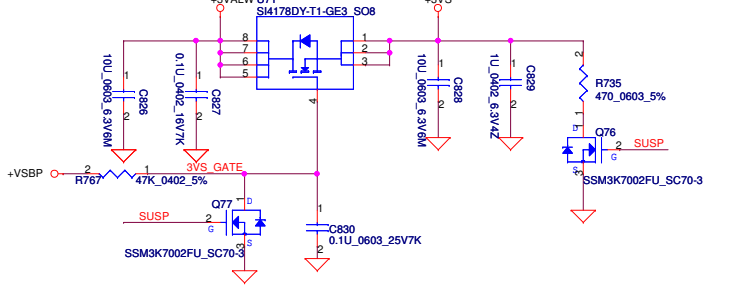
+5VALW TO +5VS (5.35A)



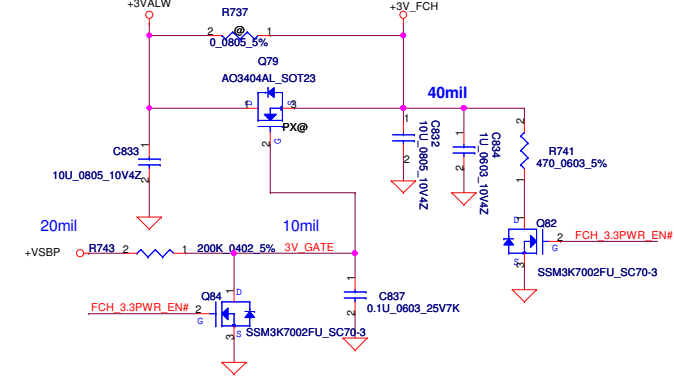
+1.1VALW TO +1.1VS (4A)



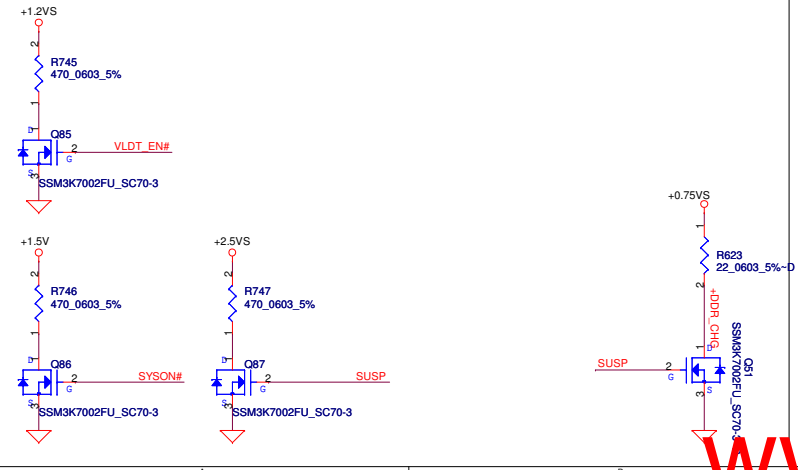
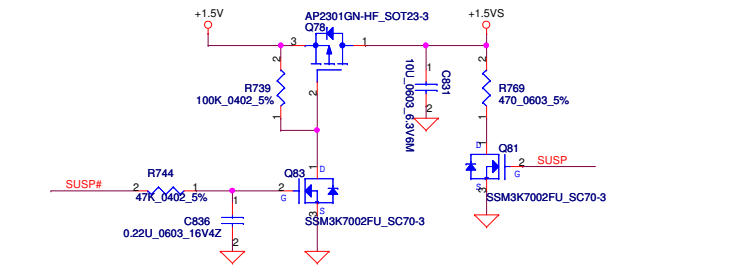
+3VALW TO +3VS (3A)



Instant On +3VALW TO +3V_FCH (1A)



+1.5V TO +1.5VS (0.5A)

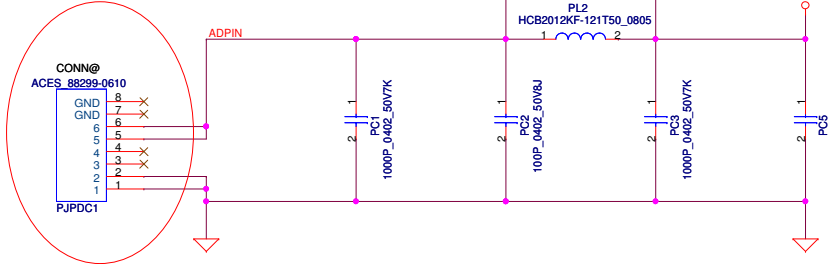


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Issued Date	2011/07/29	Deciphered Date
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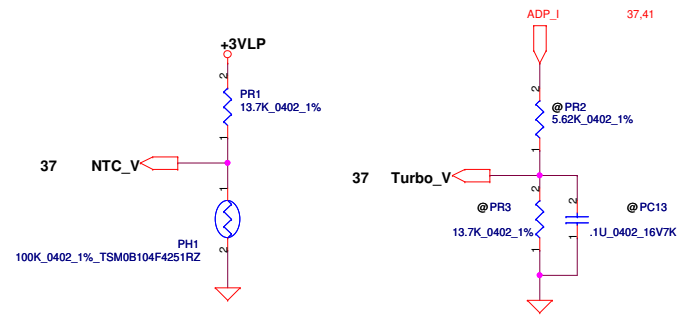
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Compal Electronics, Inc.		
DC Interface		
Title	Document Number	Rev
	QML70 LA-8371P	0.11
Date:	Wednesday, October 19, 2011	Sheet 39 of 53

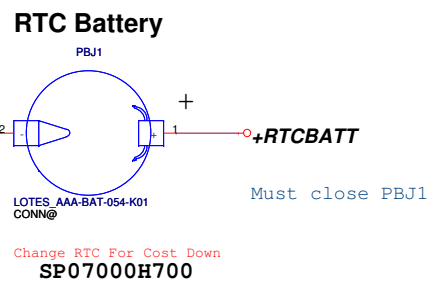
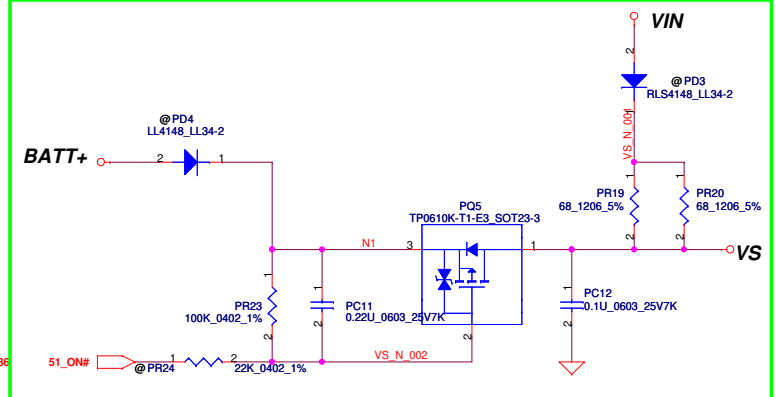
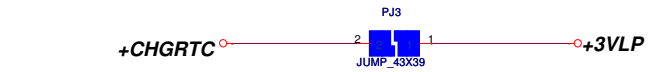
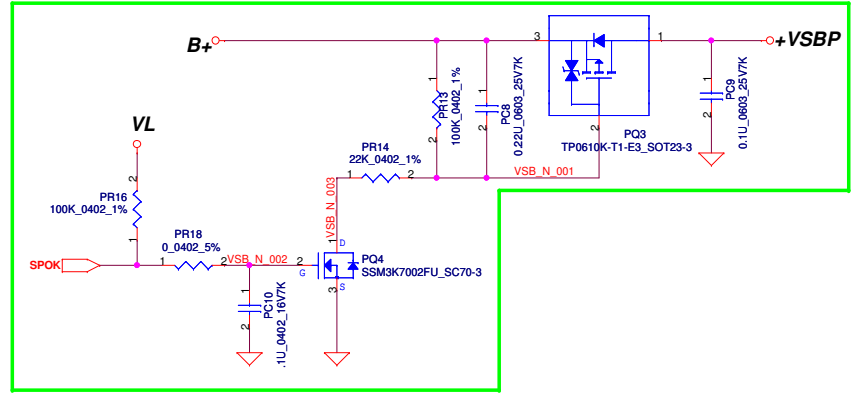
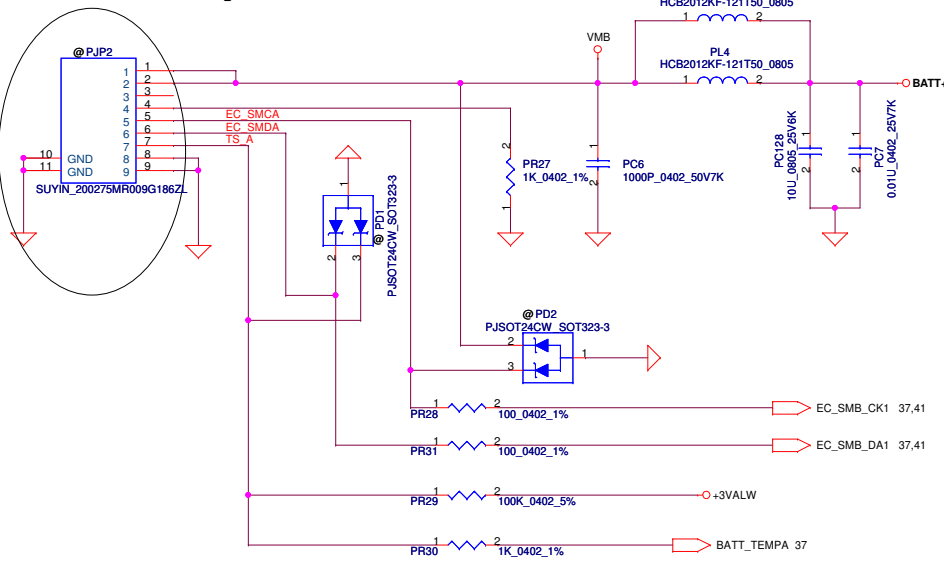
DCIN jack P/N:SP02000N00,
need doble confirm P/N with ME



PH901 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 50 degree C



Change DC040007T0L to DC040004L00
(Use DC040001V00 symbol)

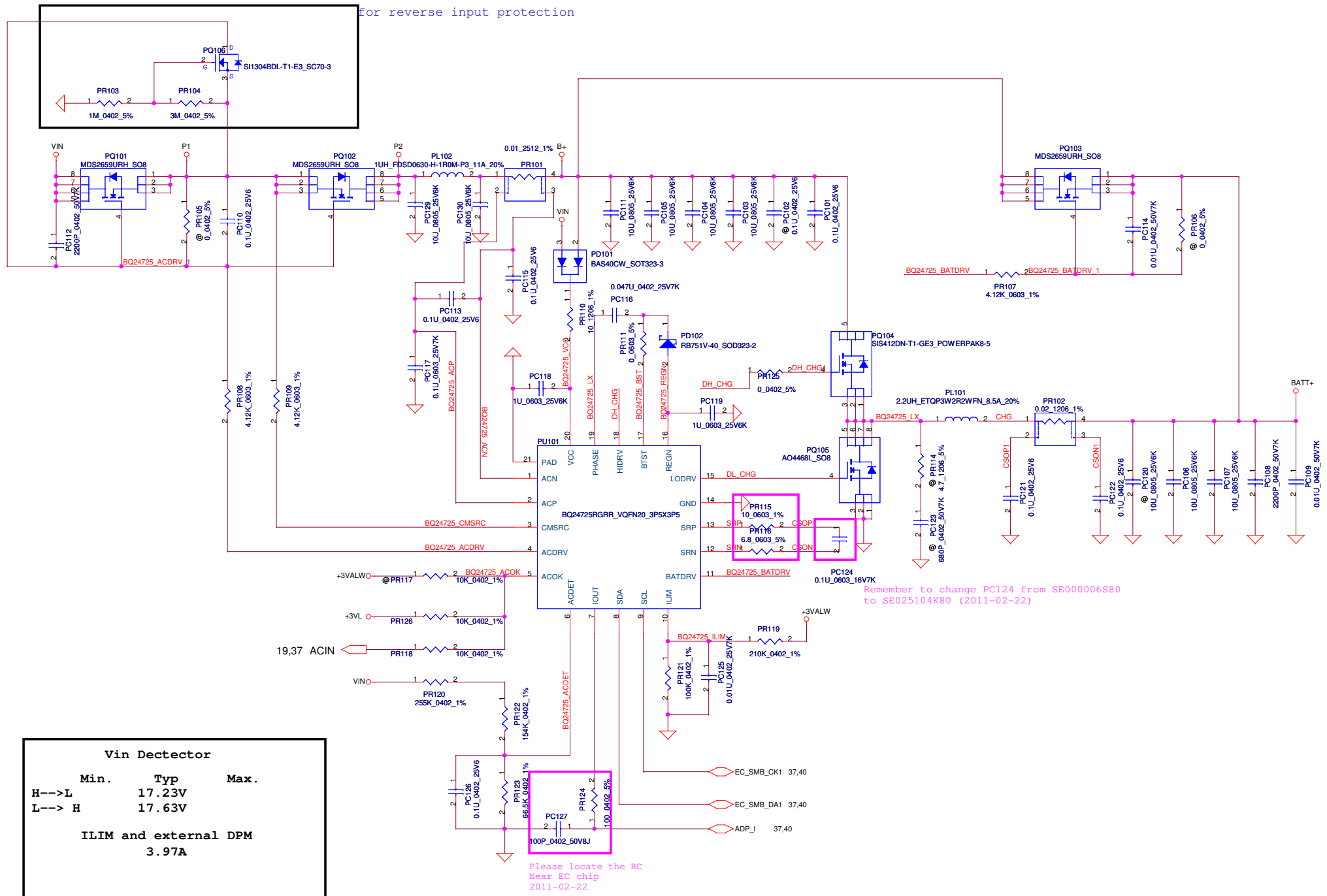


For KB9012 --> Remove all 51_ON# circuit

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DEPARTMENT EXECUTIVE AUTHORIZED BY COMPAL ELECTRONICS, INC. WITH THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Date	Wednesday, October 19, 2011
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for reverse input protection

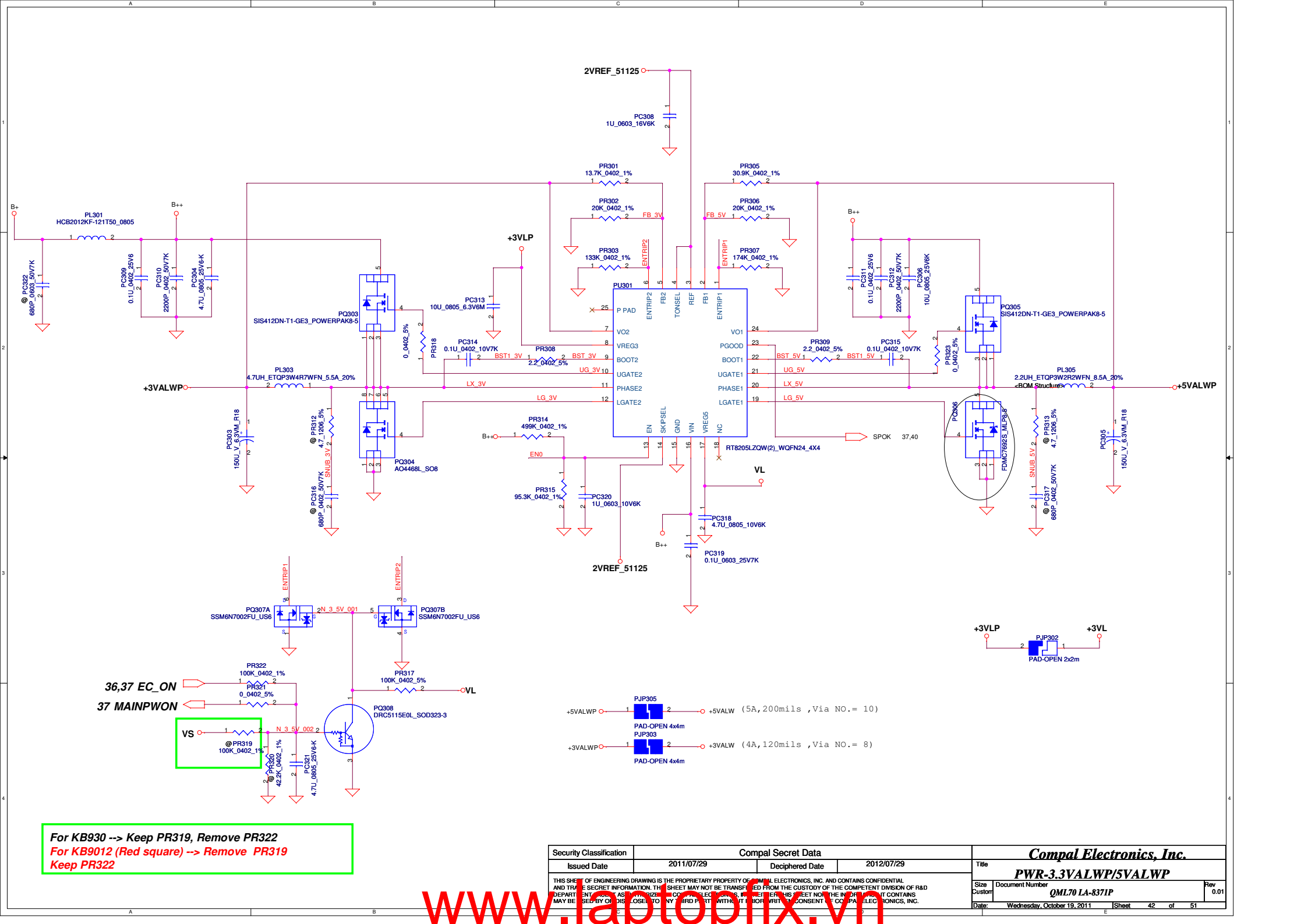


Vin Detector			
	Min.	Typ	Max.
H-->L		17.23V	
L-->H		17.63V	
ILIM and external DPM			
3.97A			

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Title			
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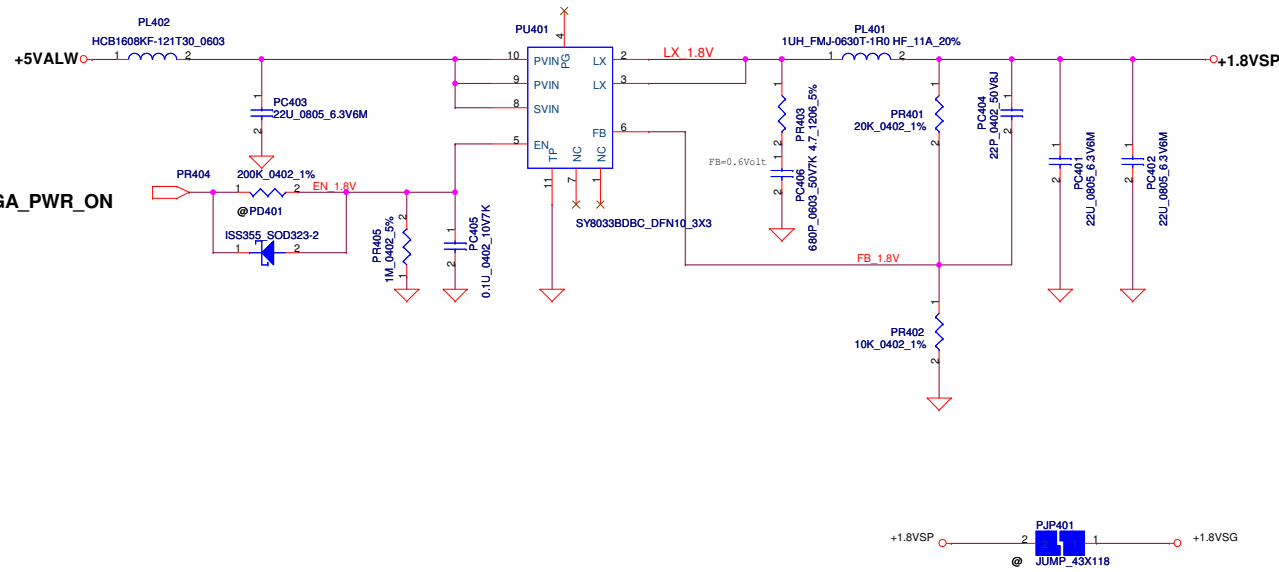


For KB930 --> Keep PR319, Remove PR322
 For KB9012 (Red square) --> Remove PR319
 Keep PR322

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			Custort	QML70 LA-837IP	0.01
			Date:	Wednesday, October 19, 2011	Sheet 42 of 51

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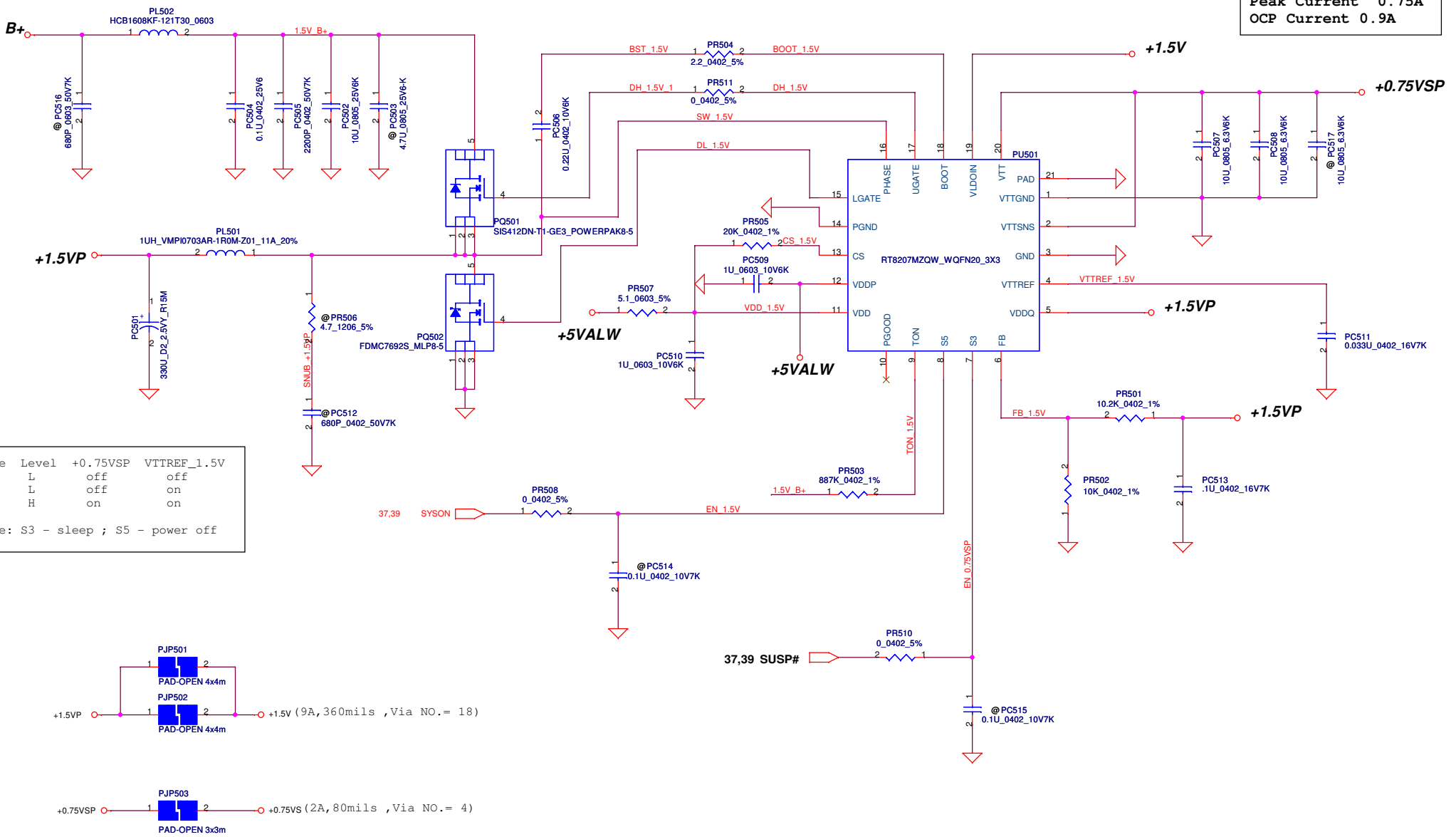
20,26,49 VGA_PWR_ON



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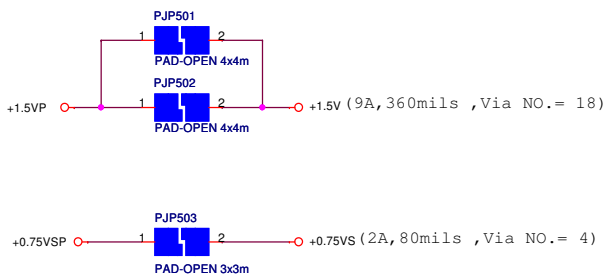
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0.75Volt +/- 5%
 TDC 0.525A
 Peak Current 0.75A
 OCP Current 0.9A



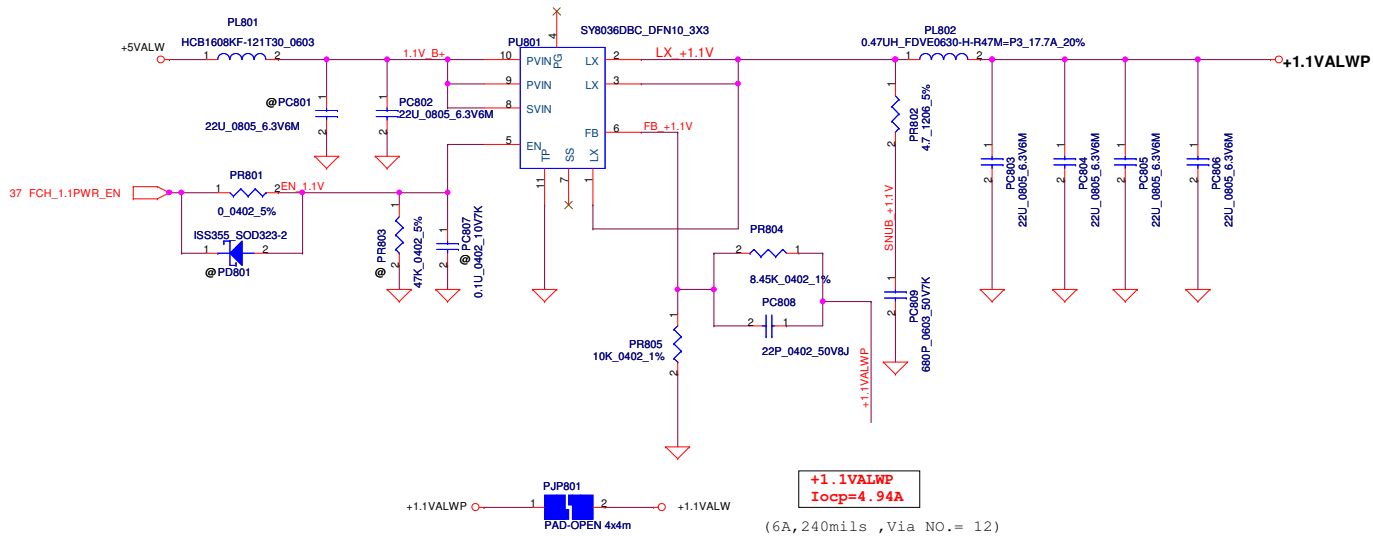
Mode	Level	+0.75VSP	VITREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off



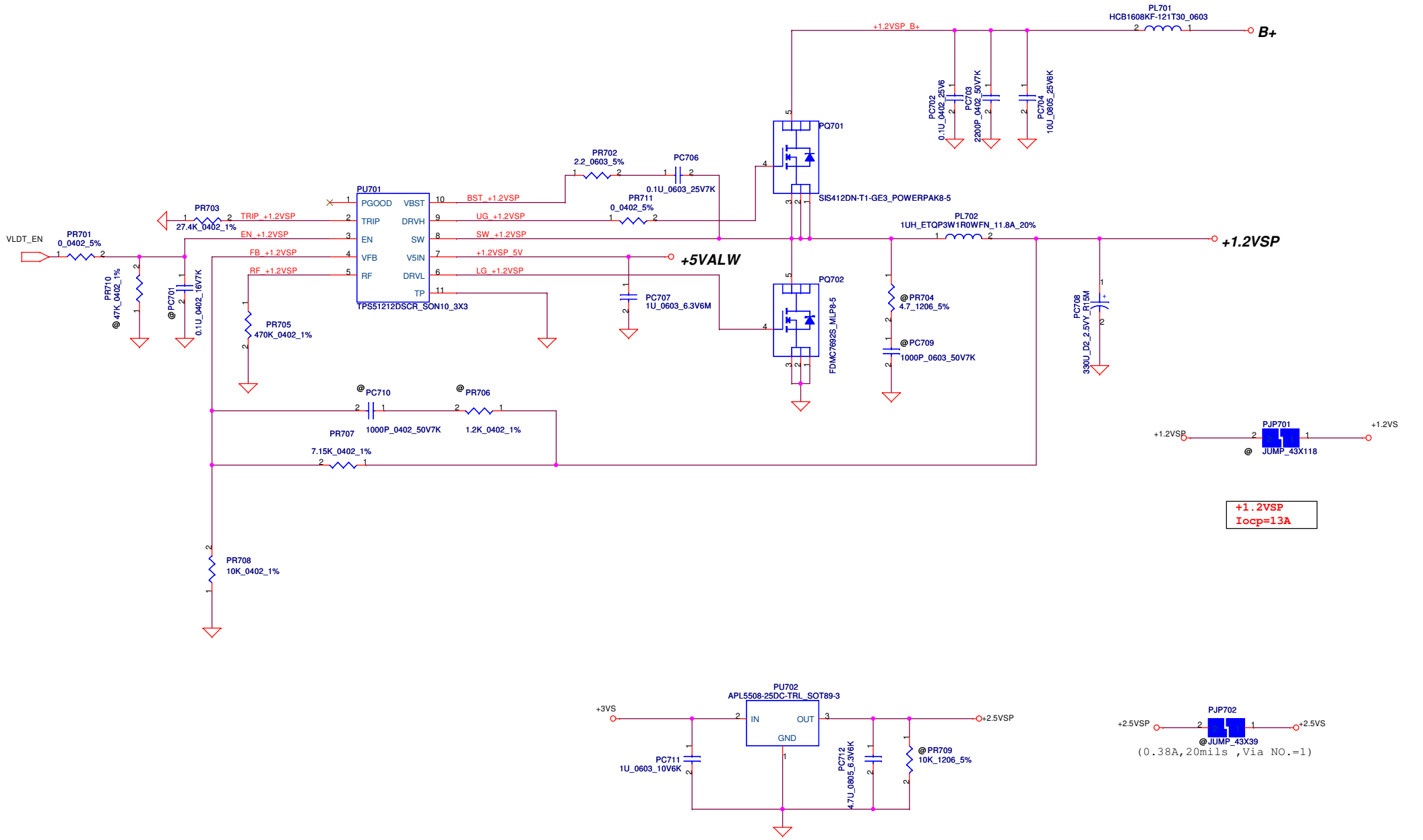
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			Date: Wednesday, October 19, 2011	Sheet 45 of 51

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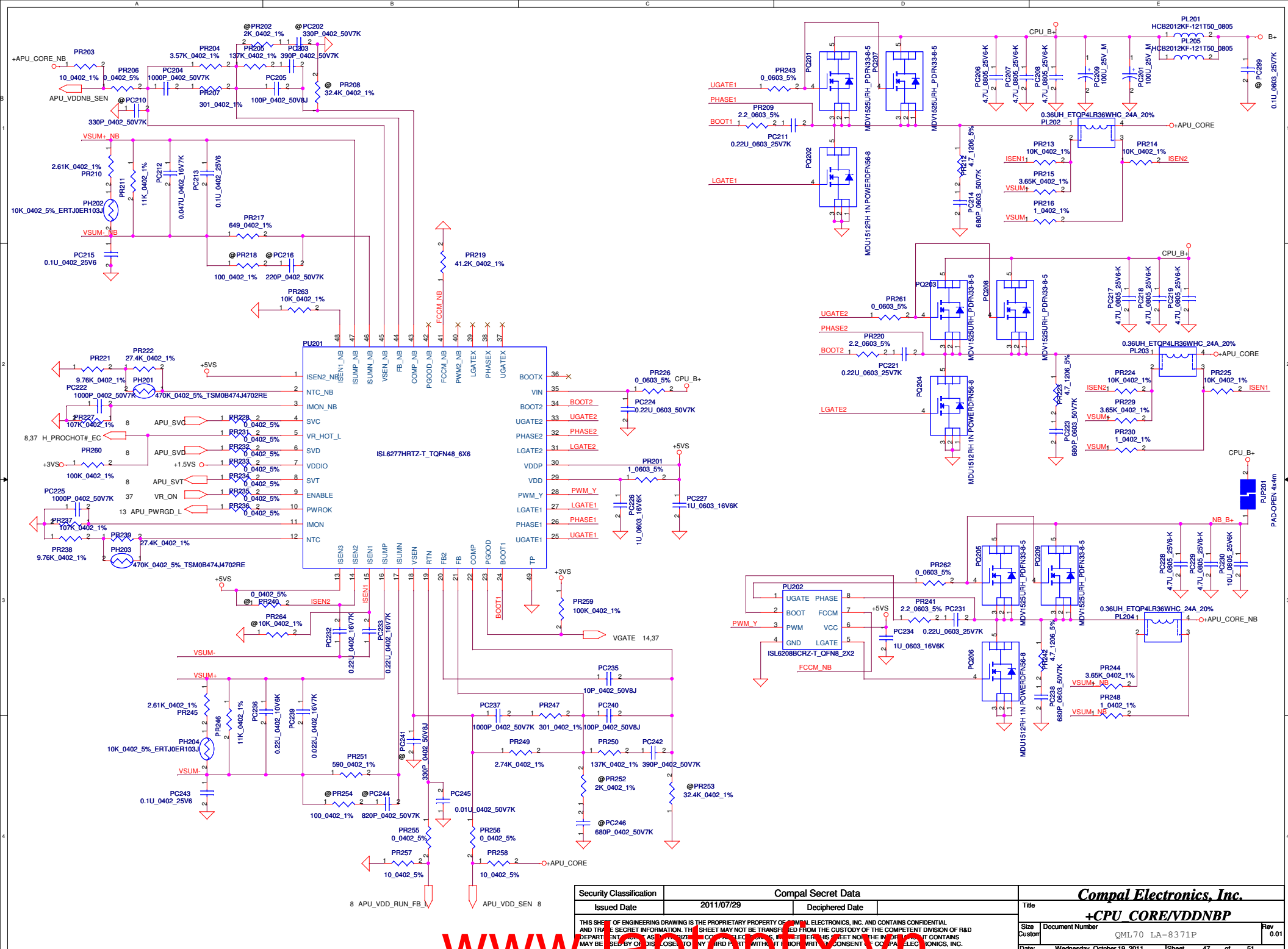


+1.2VSP
I_{ocp}=13A

PJP702
@JUMP_43X39
(0.38A, 20mils, Via NO.=1)

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Size		Document Number	Rev	0.01
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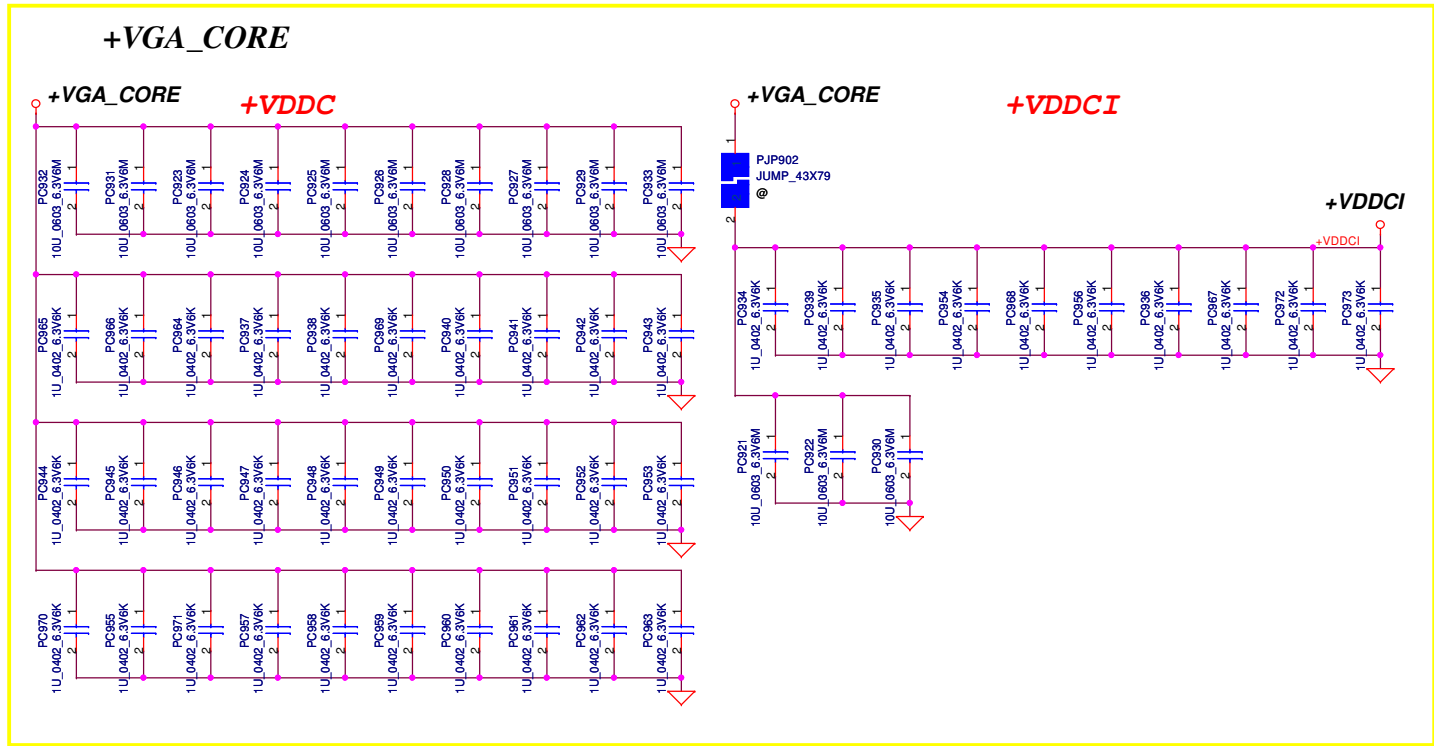
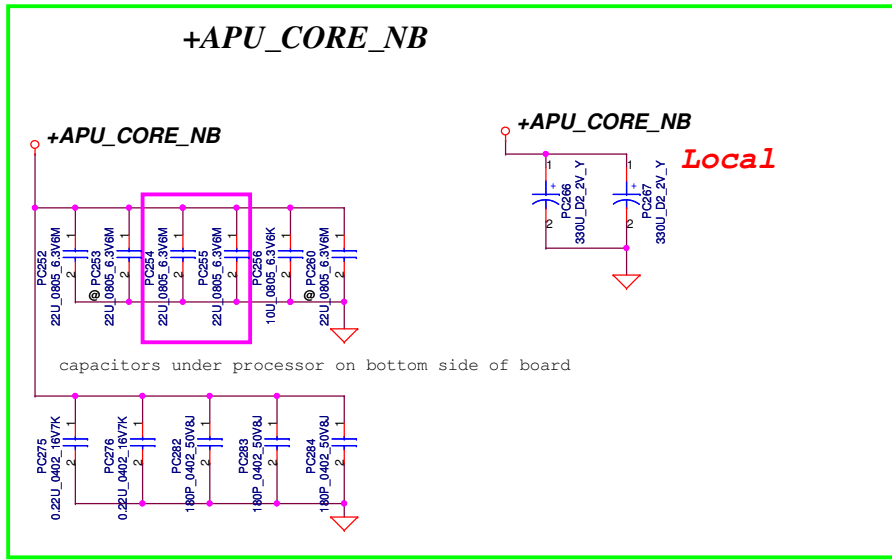
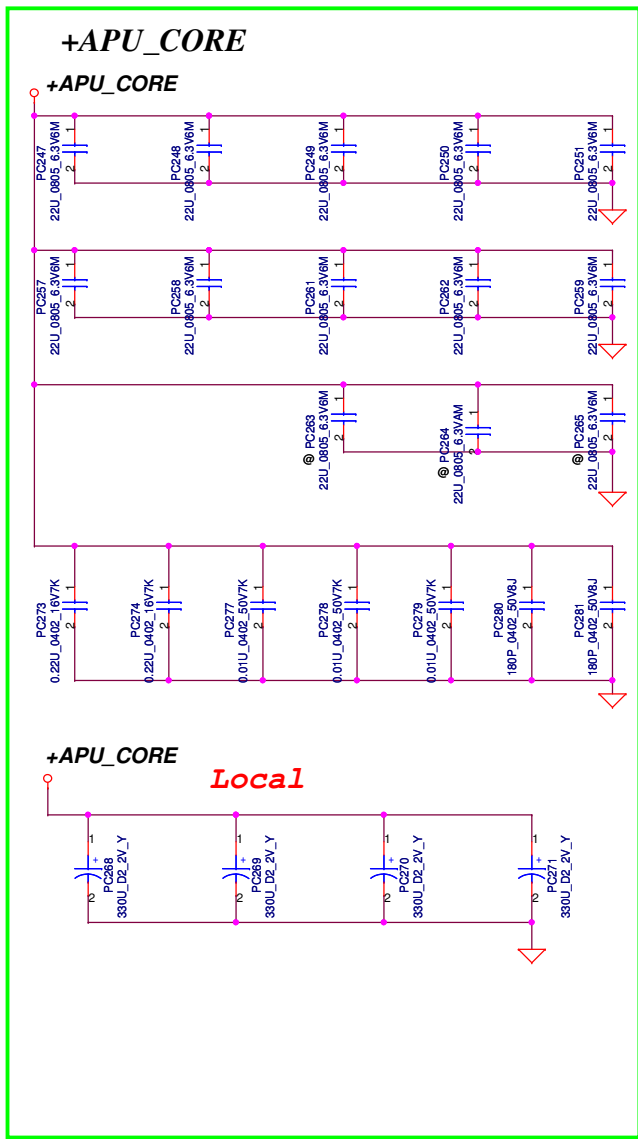
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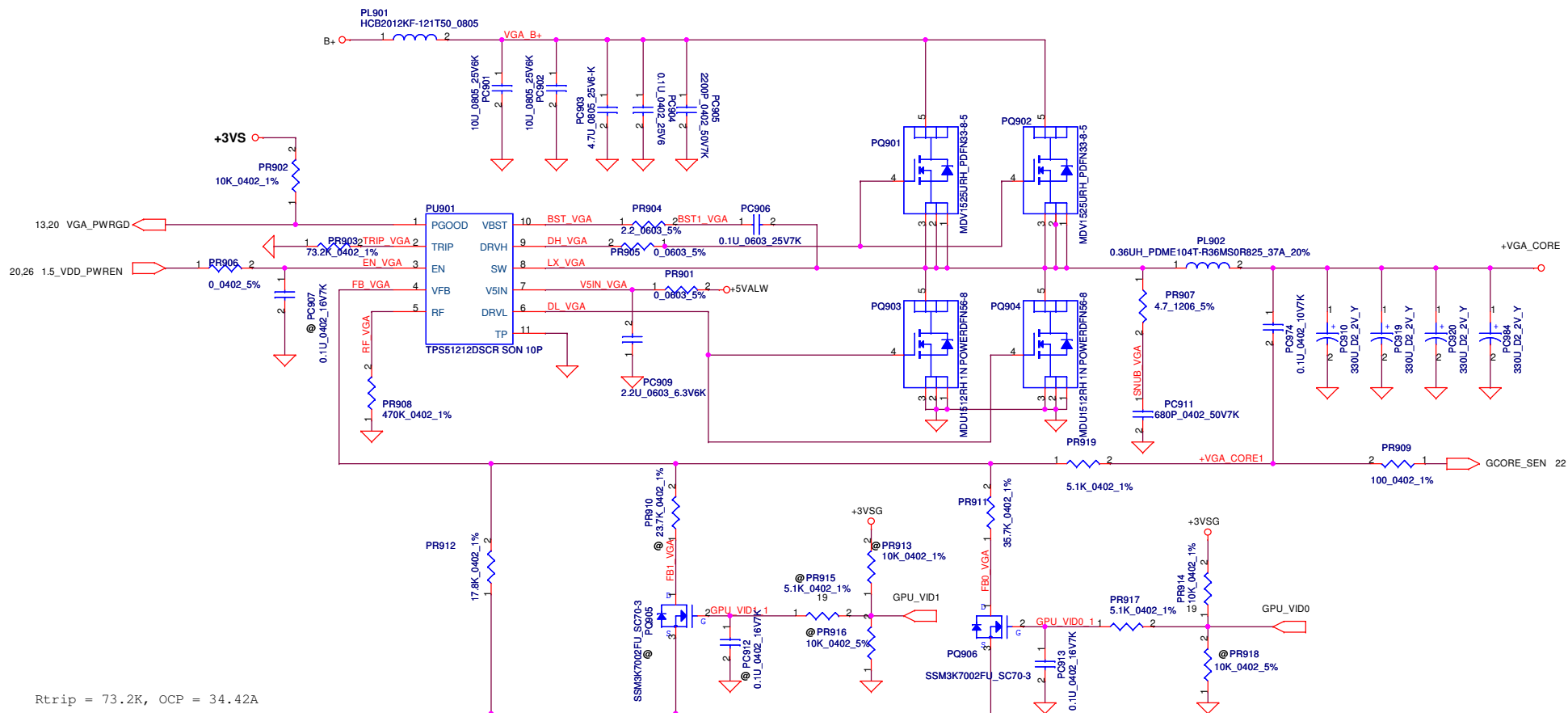
Compal Electronics, Inc.			
+CPU CORE/VDDNB			
Title	Document Number	QML70 LA-8371P	Rev 0.01
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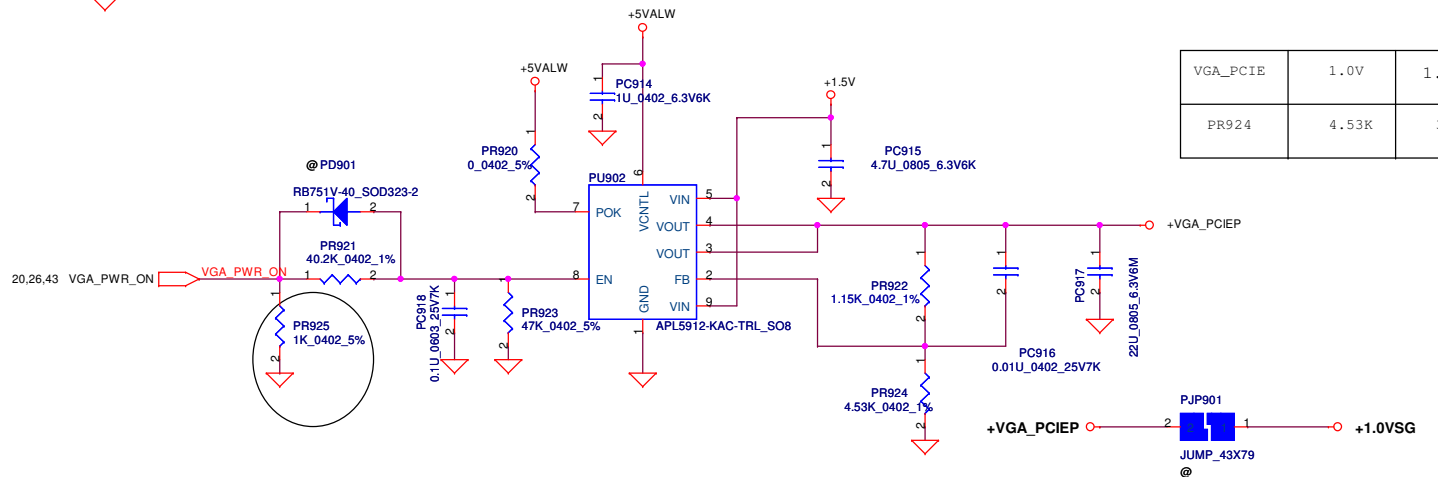
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Rtrip = 73.2K, OCP = 34.42A
 Rrf = 470K, FSW = 290KHz

For Whistler (Thames)
 $1/2\Delta I = 4.05A$
 $V_{trip} = 36.5K * 10\mu A = 0.365V$
 $I_{ocpmin} = 0.365V / (8 * 1.6m) + 1/2\Delta I = 28.51A + 4.05A = 32.56A$

Thames	
GPU_VID0	Core Voltage Level
1	0.9V
0	1.0V



VGA_PCIE	1.0V	1.1 V
PR924	4.53K	3K

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Version Change List (P. I. R. List) for Power Circuit

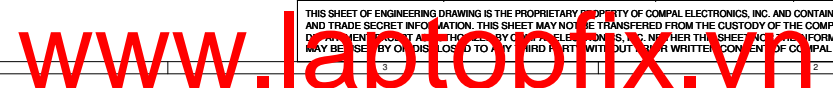
Page#	Title	Date	Request Owner	Issue Description	Solution Description
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Base on GPU Reference schematic	0.02	22	Reserve pull-up / pull-down resistor 100ohm on GCORE_SEN	08/30	SR
2			0.02	15	Modify Netname of SPI signal of U5	08/30	SR
3			0.02	26	Change Q91.2 from 1.5_VDDC_PWREN# to 1.5VSG_PWREN#	08/30	SR
4		These components are for VGA	0.02	26	Change BOM Structure of R349, R350, R354, R355, Q95, Q96 to PX0	08/30	SR
5		Base on AMD Comal CRB	0.02	8	Change pull-up voltage of APU_RST#, APU_PWRGD, APU_SVT, APU_SVC, APU_SVD, ALERT_L, ALLOW_STOP from +1.5V to +1.5VS	08/30	SR
6		For EMI request	0.02	15	Reserve R559, R561, C624, C625 @ FCH_SDCLK / FCH_SDWP	08/30	SR
7			0.02	36	Remove USB3.0 Host contorller circuit	09/01	SR
8			0.02	17	Remove componets of HUDSON_M2	09/01	SR
9		Set PCIE FULL TX OUTPUT SWING to High (Full Swing)	0.02	19	Modify GPU Straps: GPU_GPI00 pull-high	09/01	SR
10			0.02	23	Reserve pull-high and pull-down resistor of MAA14/MBB14	09/01	SR
11		Base on Thames M2 datasheet	0.02	21	Modify U7.U13, U7.14 to NC	09/01	SR
12			0.02	19	Add THM_ALERT# to from U7.AG30 (GPU_THERMAL INT) to U34.6 (ADM1032) Add GPU_CTF from U7.AM17 (GPU_CTF) to U72.97 (EC)	09/02	SR
13			0.02	31	Reserve Analog microphone circuit	09/02	SR
14			0.02	9, 39, 45	Change contorl singal of 1.1VALWP from SPOK to FCH_1.1PWR_EN Change +1.1V_FCH to +1.1VALW	09/02	SR
15			0.02	15, 37	Connect U72.92 (EC) to U2.V1 (FCH)for SYS ROM Write Protect	09/02	SR
16			0.02	35	Co-lay AI Charger	09/02	SR
17			0.03	31	Modify Analog Microhpone circuit base on Vendor suggestion	09/05	SR
18			0.03	22	Add decoupling cap. base on GPU check list	09/06	SR
19			0.03	17	Change decoupling cap. base on FCH check list	09/06	SR
20			0.03	27	Change LVDS translator to RTD2136	09/06	SR
21			0.03	28	Add pull-up resistor R129, R132 (2.2K) of FCH_CRT_DDC_SDA / SCL	09/06	SR
22			0.03	13	Change R99 to 22ohm (CLK_SD_48M)	09/07	SR
23			0.03	14	Pull-down PEG_CLKREQ#	09/08	SR
24			0.03	37	Change Board ID, R398: 0ohm	09/08	SR
25			0.03	34	Change Power source of ODD from +5VS to +5VALW	09/09	SR
26			0.03	33	Change Power source of WLAN from +3VALW to +3VS	09/09	SR
27			0.03	32	Add power source for none Card Reader IC solution	09/09	SR

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				HW-PIR1	
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1			0.2	15	Change U5 power from +3V_PCH to +3V_FCH	10/11	SR2
2			0.2	15	Change GBE_MDIO pull-up voltage from +3VALW to +3V_FCH	10/11	SR2
3	Blue Screen after install VGA Driver		0.2	25	SWAP QSB7 and QSB#7	10/11	SR2
4			0.2	32	Delete Net SDCD, SDWP# that connect to EC Add MOSFET inverter of SDWP#	10/11	SR2
5			0.2	8	Un-mount pull-high resistor of APU_SVT, APU_SVC, APU_SVD	10/11	SR2
6			0.2	28	Follow QCL70 pin define	10/11	SR2
7			0.2	38	Modify Touch Pad pin define	10/11	SR2
8		For voltage leakage	0.2	8	Change pull-high voltage of APU_PROCHOT#, APU_THERMTRIP#, APU_SVT, APU_SVC, APU_SVD, ALERT_L, ALLOW_STOP, APU_RST#, APU_PWRGD, APU_SIC, APU_SID	10/11	SR2
9		Base on AMD recommend	0.2	24, 25	Change R299, R300, R309, R310, R319, R320, R325, R326 from 56ohm to 40.2ohm	10/11	SR2
10			0.2	37	Change Board ID to "1" for SR2	10/13	SR2
11			0.2	22	Seperate VDDC and VDDCI of VGA	10/14	SR2
12			0.2	23	Reserve R611, R612 for MAA14, MAB14	10/14	SR2
13							
14							
15							
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