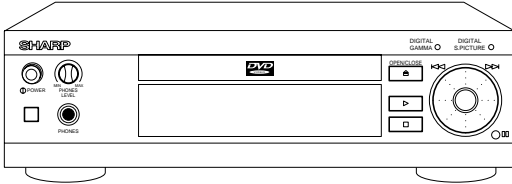


# SHARP SERVICE MANUAL

S59F9DV-600S/

## DVD VIDEO PLAYER



# MODELS DV-600S DV-600H



In the interests of user-safety (Required by safety regulations in some countries) the set should be restored to its original condition and only parts identical to those specified be used.

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# 1. IMPORTANT SAFEGUARDS AND PRECAUTIONS

## CAUTION

BEFORE OPERATING YOUR NEW DVD PLAYER, PLEASE CAREFULLY READ THIS OPERATION MANUAL AND THEN SAVE IT FOR FUTURE REFERENCE AS IT WILL BE USEFUL IF YOU HAVE ANY PROBLEMS OPERATING YOUR DVD PLAYER IN THE FUTURE.

### Note:

This unit can be used only where the power supply is AC 110V-240V, 50/60Hz. It cannot be used elsewhere.

### CAUTION:

**USE OF CONTROLS OR ADJUSTMENTS OR PERFORMANCE OF PROCEDURES OTHER THAN THOSE SPECIFIED HEREIN MAY RESULT IN HAZARDOUS RADIATION EXPOSURE.**

**AS THE LASER BEAM USED IN THIS DVD PLAYER IS HARMFUL TO THE EYES, DO NOT ATTEMPT TO DISASSEMBLE THE CABINET. REFER SERVICING TO QUALIFIED PERSONNEL ONLY.**

### WARNING:

**TO REDUCE THE RISK OF FIRE OR ELECTRIC SHOCK, DO NOT EXPOSE THIS EQUIPMENT TO RAIN OR MOISTURE.**

**TO REDUCE THE RISK OF FIRE OR ELECTRIC SHOCK, AND ANNOYING INTERFERENCE, USE THE RECOMMENDED ACCESSORIES ONLY.**

### Laser Diode Properties

Material: AlGaInP

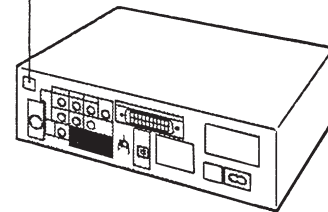
Wave length: 650 nm

Emission Duration: Continuous

Laser output: Max. 0.7 mW

- This DVD player is classified as a CLASS 1 LASER product.
- The CLASS 1 LASER PRODUCT label is located on the rear cover.
- This product contains a low power laser device. To ensure continued safety do not remove any cover or attempt to gain access to the inside of the product. Refer all servicing to qualified personnel.

CLASS 1  
LASER PRODUCT



(Back of product)

CAUTION-WHEN OPEN DO NOT STARE INTO BEAM OR VIEW DIRECTLY WITH OPTICAL INSTRUMENTS.

VARNING-NÄR DENNA DEL ÄR ÖPPNAD, STARRA EJ IN I STRÅLEN OCH BETRAKTA EJ STRÅLEN MED OPTISKA INSTRUMENT.

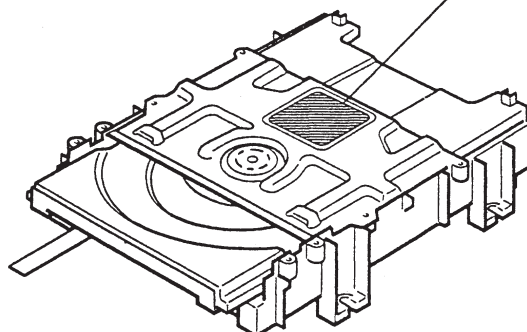
ADVARSEL-VED ÅBNING SE IKKE IND I STRÅLEN-HELLER IKKE MED OPTISKE INSTRUMENTER.

VARO! AVATTAESSA OLET ALITTIIN. ÄLÄ TUJOTTA SÄTEESSEEN ALAKÄ KATSO SITÄ OPTISEN LAITTEEN LÄPI.

VARNING-NÄR DENNA DEL ÄR ÖPPNAD, STARRA EJ IN I STRÅLEN OCH BETRAKTA EJ STRÅLEN GENOM OPTISKT INSTRUMENT.

ADVARSEL-NÄR DEKSEL ÅPNES, STARR IKKE INN I STRÅLEN ELLER SE DIREKTE MED OPTISKE INSTRUMENTER.

ここを開くとレーザー光が出ます。  
レーザー光をのぞき込まないでください。  
光学機器で直接ビームを見ないでください。



## 2. FEATURES

- Plays DVD, video CD and CD (Digital Audio) discs
- Built-in Dolby Digital (AC-3) decoder supporting Dolby Pro Logic\*<sup>1</sup> decoding and Virtual Surround
- MPEG 2-channel (STEREO) decoder (From AUDIO L/R)
- MPEG MULTI digital out capability (5.1ch)
- New Digital Gamma correction and New Digital Super Picture functions
- RGB OUT (LINE1 OUT)/S-VIDEO OUT
- DTS\*<sup>2</sup> digital output capability

\*<sup>1</sup> Manufactured under license from Dolby Laboratories, "Dolby", "Pro Logic" and the double-D symbol are trademarks of Dolby Laboratories.

\*<sup>2</sup> "DTS" and "DTS Digital Surround" are trademarks of Digital Theater Systems, Inc.

## 3. SPECIFICATIONS

Signal System:	NTSC* <sup>1</sup> /PAL (* <sup>1</sup> : A played back NTSC is a modified PAL signal.)
Video output:	Output connector: Pin-jack/21-pin Euro-SCART Output level: 1 Vp-p (75Ω)
S video output:	Y output level: 1 Vp-p (75Ω) C output level: 0.30 Vp-p (75Ω) Output connector: S connector
Audio output:	Output connector: Pin-jack/21-pin Euro-SCART Output level: 2 Vrms (1 kHz, 0 dB)
Digital audio I/F:	Optical digital output: Optical connector
Audio output:	Coaxial digital output: Pin-jack
Headphone output:	Output connector: Standard jack
Video signal horizontal resolution:	500 lines (DVD)
S/N ratio:	60 dB (DVD)
Audio signal frequency characteristics:	For DVD linear PCM playback: 4 Hz to 22 kHz (48 kHz sampling) 4 Hz to 44 kHz (96 kHz sampling) CD playback: 4Hz to 20 kHz (EIAJ) (MPEG 1/2 Audio)
S/N ratio:	CD: 105 dB, 1 kHz (EIAJ)
Dynamic range:	DVD linear PCM: 94 dB (EIAJ) CD: 94 dB (EIAJ)
Total harmonic distortion ratio:	CD: 0.006% or less (EIAJ)
Operating temperature:	5°C to 40°C
Storage temperature:	-20°C to 55°C
Power supply :	220 V to 240 V AC, 50/60 Hz
Power consumption:	16 W (0 W when switched off)
Dimensions:	270 mm × 338 mm × 80 mm (W × D × H) (Including attachments)
Weight:	2.5 kg

Specifications are subject to change without notice.  
Weight and dimensions are approximate.

### Digital Output

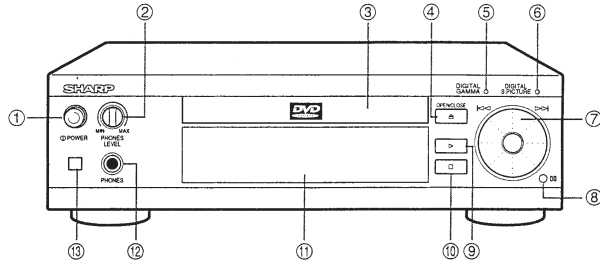
- The digital output format (optical or coaxial) used in this DVD player is linear PCM audio sampling at 44.1 kHz or 48 kHz. Linear PCM sound for DVD video discs sampled at 96 kHz cannot be output digitally. Check the disc jacket for information on the audio sampling used.

### 3-1. ACCESSORIES

Accessories: Video/audio cord x 1, AC power cord x 1, UM3 battery x 2,  
Remote Control Unit x 1

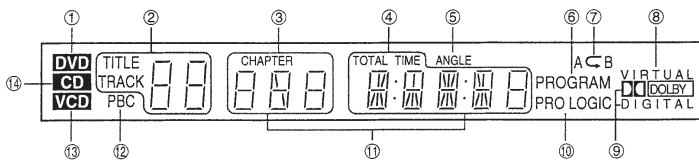
## 4. PART NAMES

### Front



- ① POWER ON/OFF (⏻) button  
If the DVD player is stopped and not used in any way for 5 minutes, the stop display disappears and "----" appears on the Front Panel display.
- ② PHONES LEVEL knob
- ③ DISC tray
- ④ OPEN/CLOSE (⏏) button for tray
- ⑤ DIGITAL GAMMA indicator
- ⑥ DIGITAL S.PICTURE indicator
- ⑦ CHAPTER DIRECT SKIP shuttle dial (Reverse/Forward) (◀/▶)
- ⑧ STILL/PAUSE (⏸) button
- ⑨ PLAY (▶) button
- ⑩ STOP (■) button
- ⑪ Front panel display (see below)
- ⑫ PHONES jack
- ⑬ Remote Control receptor

### Front Panel Display



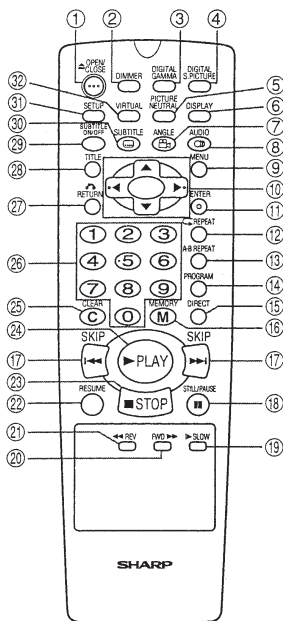
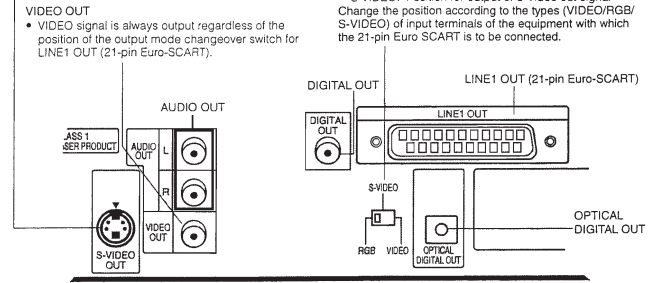
The figure above shows the front panel with all the displays on.

- ① Lights when a DVD is loaded
- ② Shows the title number [DVD only]/Shows the track number [Video CD and Audio CD]
- ③ Shows the chapter number [DVD only]
- ④ Shows the total time elapsed since the disc started playing.
- ⑤ Lights when it is possible to switch the angle. [DVD only]
- ⑥ PROGRAM indicator  
Lights during PROGRAM play.
- ⑦ Lights during repeat play  
C : Repeat    A C B: A-B repeat
- ⑧ Virtual Surround indicator
- ⑨ Dolby Digital (AC-3) indicator
- ⑩ PRO LOGIC indicator
- ⑪ Operating mode indicator (Messages)  
<Display examples>  
ND 3:5C    PLAY    PAUSE  
OPEN    FWD    CLOSE  
LDR    REV    SLOW  
STOP    STILL
- ⑫ Lights during video CD with playback control only
- ⑬ Lights when a video CD is loaded
- ⑭ Lights when an audio CD is loaded

### Rear

- S-VIDEO OUT**
- S-VIDEO signal is always output regardless of the position of the output mode changeover switch for LINE1 OUT (21-pin Euro-SCART).

- VIDEO output mode changeover switch for LINE1 OUT (21-pin Euro-SCART)**
- VIDEO: Position for output of Video signal
  - RGB: Position for output of Video signal by RGB signal
  - S-VIDEO: Position for output of S-Video out signal
- Change the position according to the types (VIDEO/RGB/S-VIDEO) of input terminals of the equipment with which the 21-pin Euro SCART is to be connected.



- ① OPEN/CLOSE (⏏) button
- \*② DIMMER button (see "DIMMER button" below)
- ③ DIGITAL GAMMA button
- ④ DIGITAL S.PICTURE button
- ⑤ PICTURE NEUTRAL button
- ⑥ DISPLAY (OSD) button
- ⑦ ANGLE (◀▶) button
- ⑧ AUDIO (🔊) button
- ⑨ MENU button
- ⑩ ▲/▼, ◀/▶ buttons
- ⑪ ENTER button
- ⑫ REPEAT (⏮) button
- ⑬ A-B REPEAT button
- ⑭ PROGRAM button
- ⑮ DIRECT button
- ⑯ MEMORY (M) button
- ⑰ SKIP button (◀▶) (Reverse/Forward)
- ⑱ STILL/PAUSE (⏸) button
- ⑲ SLOW button (▶)
- ⑳ FWD (▶) button
- ㉑ REV (◀) button
- ㉒ RESUME button
- ㉓ STOP (■) button
- ㉔ PLAY (▶) button
- ㉕ CLEAR (C) button
- ㉖ Number buttons
- ㉗ RETURN (⏪) button
- ㉘ TITLE button
- ㉙ SUBTITLE ON/OFF button
- ㉚ SUBTITLE (⏏) button
- ㉛ SETUP button
- ㉜ VIRTUAL button

\*DIMMER feature  
Use this button to set the front panel display brightness to Bright or Dark.

## 5. MAINTENANCE CHECK ITEMS AND EXECUTION TIME

### MECHANICAL PARTS REQUIRING PERIODICAL INSPECTION

Use the following table as a guide to maintain the mechanical parts in good operating condition.

Parts	Maintained	1,000 hrs.	2,000 hrs.
	Pickup		○
Spindle Unit		□	○
Sled Motor			○
Loading Motor			○
Belt		□	○

**Note**

○ : Part Replacement

□ : Cleaning

(For cleaning, use a lint-free cloth dampened with pure isopropyl alcohol.)

### CARES WHEN USING THE PICKUP

1. The laser light having wavelength 650 nm is emitted from the objective lens. BE CAREFUL SO THAT THE LASER LIGHT DOES NOT ENTER DIRECTLY INTO YOUR EYE.
2. The semiconductor laser may be easily damaged by electrostatic charges. When handling the pickup, take care so that the electrostatic charge is not generated.
3. The semiconductor laser may be easily damaged by overcurrent. Use the power supply unit which does not give any spike current when the power is turned on and off.
4. Carefully remove the dust and dirt from the objective lens with the lens blower.  
When handling the objective lens, take due care so that it is not contaminated with fingerprint, etc. If the objective lens is contaminated, impregnate the cleaning paper with a small quantity of solvent (isopropyl alcohol), and gently wipe to clean.
5. The ozone layer depleting components (ODC) are not used in the production process for the product.

## 6. DISASSEMBLY AND REPLACEMENT OF MAIN PARTS

### 6-1. DISASSEMBLY

1. Remove five screws (A), and remove the cabinet.

**Note:** When assembling it, tighten the screws in order of ①-②.  
(Because the set may rise a little by tightening the screws.)

2. Remove two screws (B).

3. Remove one screw (C).

4. Release the hooks of the front panel at two places on both sides and at three places on the bottom, and slide the front panel toward you.

5. Disconnect the connectors (D) and (E).

6. Remove four screws (F) which install the mechanical unit.

7. Disconnect the lead lines (G) and (H) and (J) from the main PWB under the mechanism.

8. Remove two screws (K) on both sides of the terminal angle frame.

9. Remove three screws (L) which install the terminal PWB.

10. Remove seven screws (M) and one screw (N) which install the terminal block.

11. Remove three screws (P) of the display PWB.

12. Remove two screws (Q) of the decorative leg.

13. Push out the middle pin (R) of the setting leg in the direction opposite to insertion. (Two places)

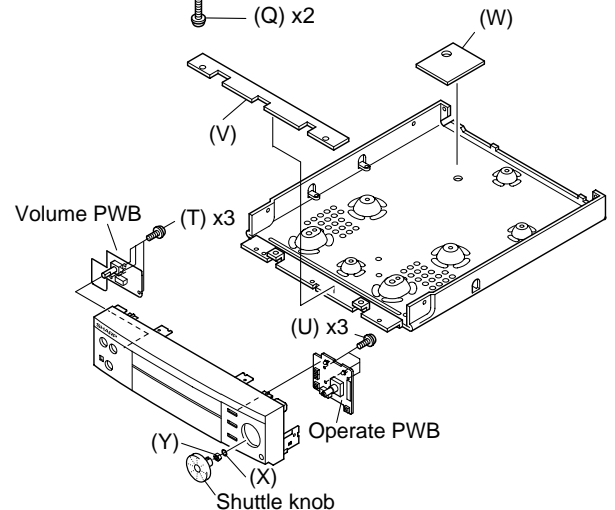
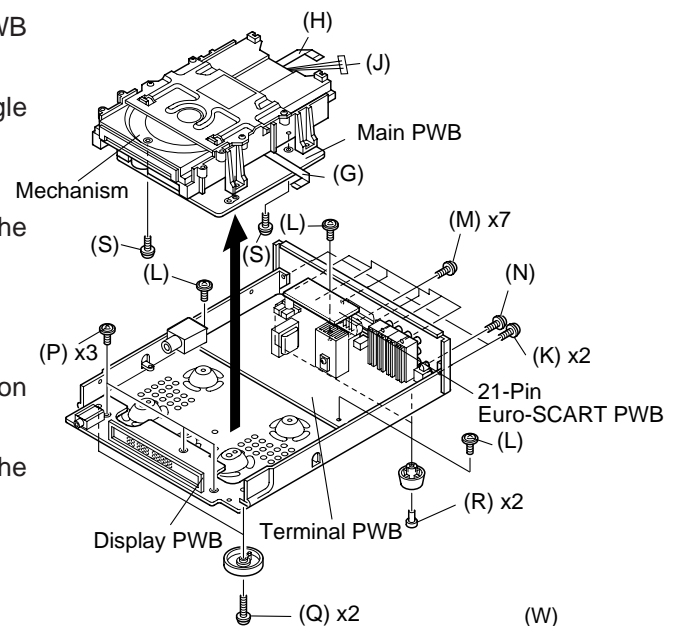
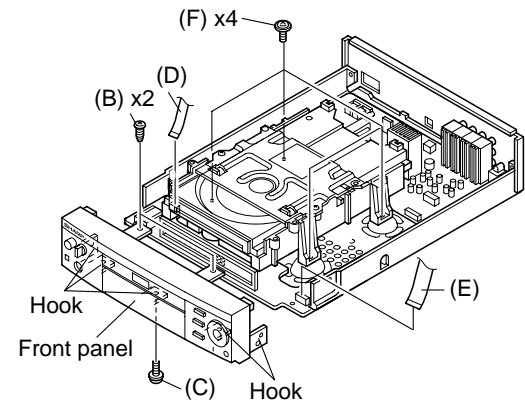
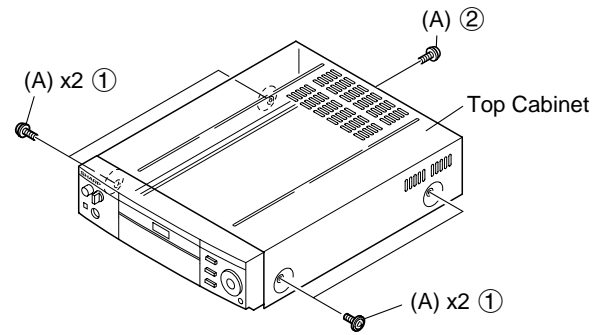
14. Remove two screws (S) which install the main PWB under the mechanical unit.

15. Remove three screws (T) which install the volume PWB of the front panel.

16. Remove three screws (U) which install the operate PWB.

\* The spacer and insulation seat under the indication tube of (V) and (W) are bonded with both-side sticking tape.

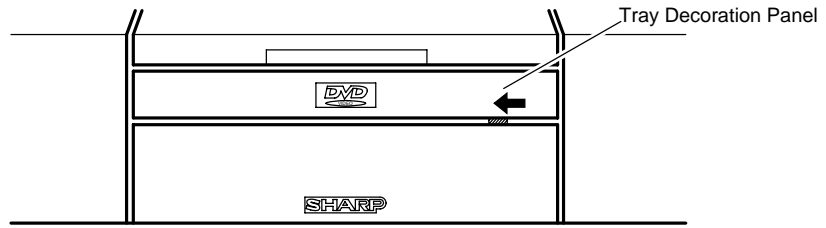
17. Remove one washer (X) and one nut (Y) which install the shuttle knob.



## 6-2. REPLACEMENT OF MAIN PARTS

<Disassembling and assembling procedure>

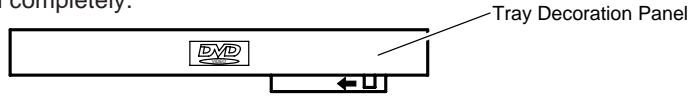
- Removing the tray (emergency ejection)
- Removing the tray lock (set state)



Insert a thin plate into the hatching part, slowly move the it in the arrow direction so that the tray is moved out a little in the arrow direction.

**Note:** In this state the tray cannot be removed completely.

- Drive Unit State



Slowly move in the arrow direction, using the screwdriver having a fine head.

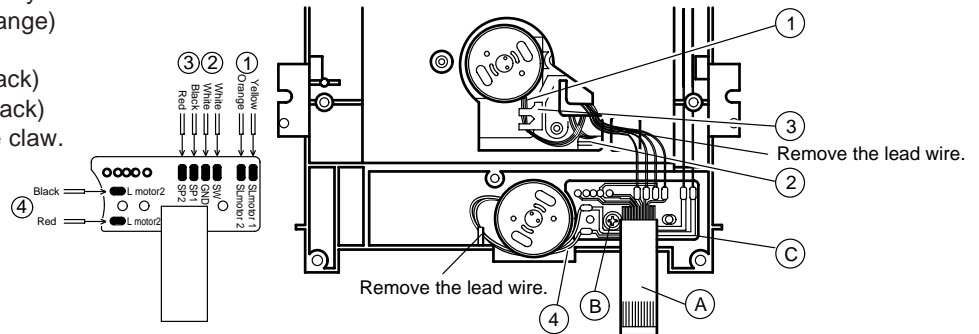
<Disassembling and assembling the mechanism chassis>

1. Remove the pickup FPC and loading relay FFC (A) from the main PWB.

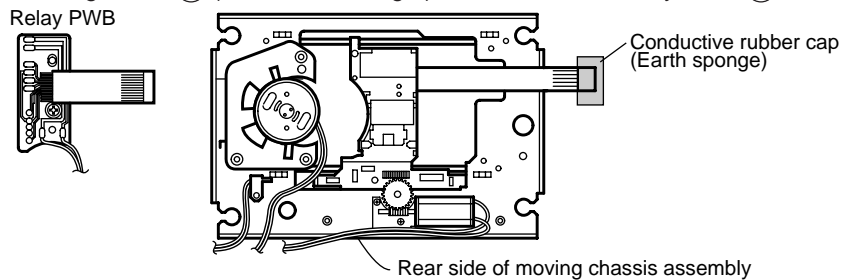
**Note:** Fit the conductive rubber cap to the front end of pickup FPC (short-circuit).

2. Remove the solder joint of loading relay PWB at drive unit rear side.

- ① Sled motor lead wire (Yellow-Orange)
- ② IN SW lead wire 2 (White)
- ③ Spindle motor lead wire (Red-Black)
- ④ Loading motor lead wire (Red-Black)
- ⑤ Remove each lead wire from the claw.

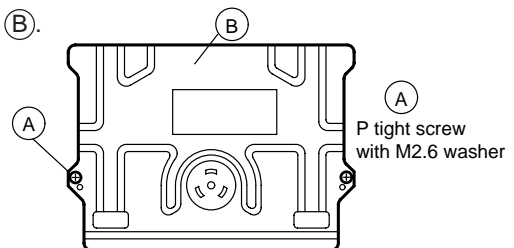
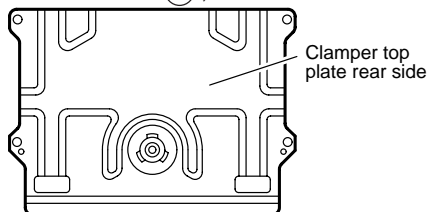


3. Remove the relay PWB mounting screw (B) (M2.6S + 6S S tight), and remove the relay PWB (C).



4. Disassembling the mechanism chassis moving chassis assembly

- (1) Remove the four M2.6 screws (A), and remove the clamped top plate (B).

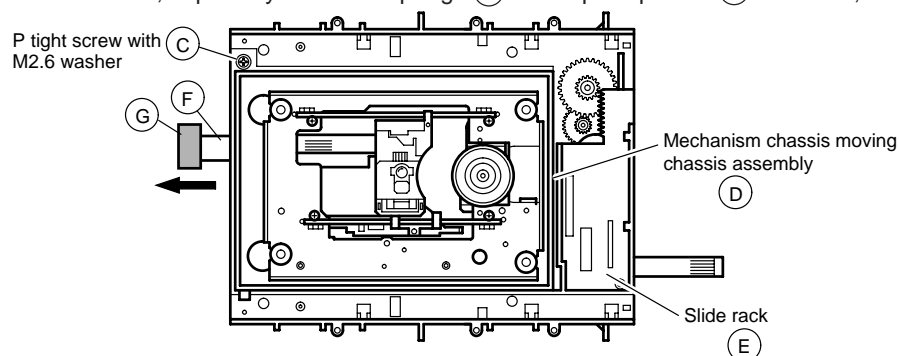


- (2) Remove the M2.6 screw (C).

- (3) Holding aslant upward the mechanism chassis moving chassis assembly (D) in the arrow direction, remove.

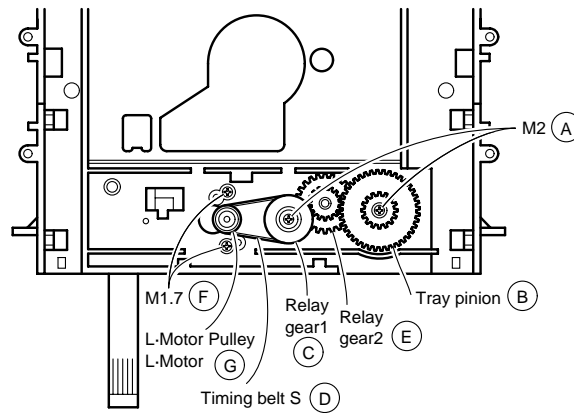
**Note:** The slide rack (E) must be moved to the left side as shown in diagram.

Take care so that the lead wires, especially the earth sponge (G) at the pickup FPC (F) front end, must not beremoved.



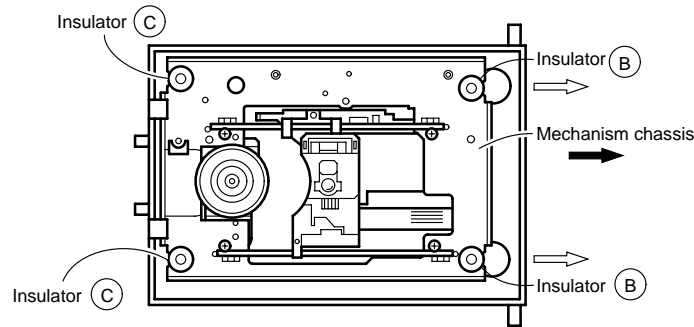
5. Disassembling the loading drive system

- (1) Remove the two M2 screws (A).
- (2) Remove the tray pinion (B).
- (3) Remove the relay gear 1 (C) together with the timing belt S (D).
- (4) Remove relay gear 2 (E).
- (5) Remove the two M1.7 screws (F).
- (6) Remove the L motor (G) (with pulley) downward.



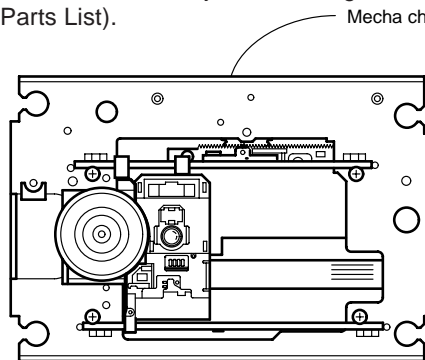
6. Disassembling the mechanism chassis from the moving chassis

- (2) Remove the insulator (B) (2 pcs. at the right side in diagram) parallel in the arrow direction. (At this time it is better to insert the fine head of screw driver at the ID side of insulator and to move in the arrow direction, which facilitates removal.)
- (3) Remove the mechanism chassis in the arrow direction, pulling upward aslant. At this time take care so that the insulator (C) (left side, 2 pcs.) is not damaged. (Do not put at once the mechanism chassis assembly.)



7. Replacing the pickup and the spindle motor

Since the pickup optical axis and turntable inclination of DVD are adjusted with higher accuracy than of CD/MD, make a replacement as a mechanism service chassis ass'y (refer to Parts List).

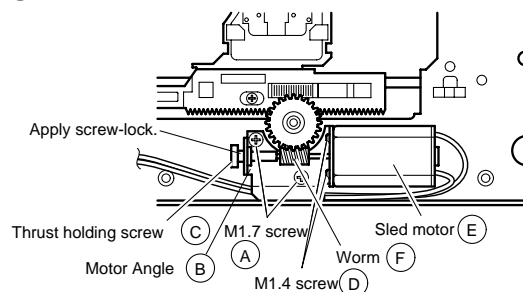


8. Replacing the Sled Motor

- (1) At the rear side of chassis remove the two M1.7 screws (A), and remove the motor angle (B).
- (2) Remove the thrust holding screw (C) (for easier removing wipe off the thread lock).
- (3) Remove the two motor fitting screws M1.4 (D), and replace the motor (E). Motor is replaced in the state while the worm (F) is kept press-fitted to the output shaft.

**Note:** When installing the motor, take care so that the worm does not damage the ANG (B) hole.

- (4) Screw in the thrust holding screw (C), adjust the worm front end clearance to 0 to 0.1 mm, and apply screw lock.





## 7. EXPLANATION OF MECHANISM

### (1) Tray loading mechanism

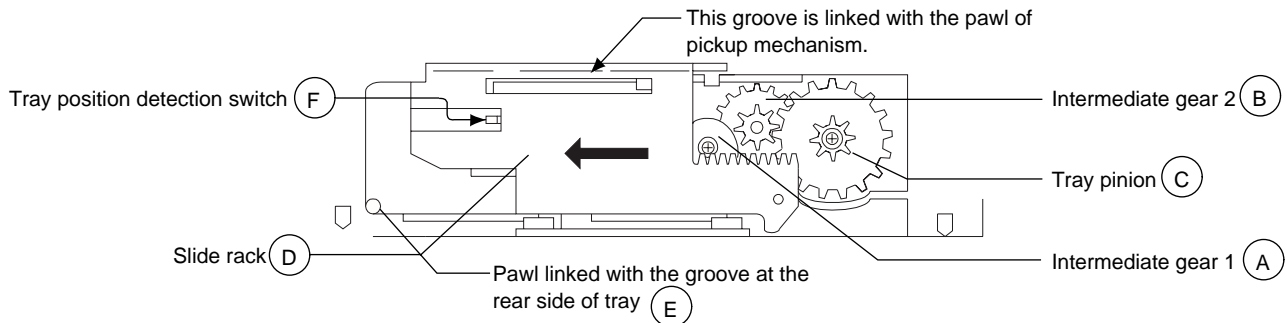
When the tray loading motor rotates counterclockwise, motion is transmitted to the slide rack (D) through the intermediate gear 1 (A), intermediate gear 2 (B) and tray pinion (C), resulting in insignificant motion in the arrow direction.

The slide rack is linked with the operating chassis. It lowers the pickup mechanism.

The protrusion of slide rack (E) is linked with the tray through the groove at the rear side of tray, so that the tray is pushed ahead a little. When the tray is pushed out, the slide rack is disconnected from the tray pinion, and at the same time the gear at the rear side of tray is connected with the tray pinion, and the tray is pushed ahead.

When the tray is pushed out fully, the slide rack moves further in the arrow direction through the groove at the rear side of tray. The tray position detection switch (F) is turned on, and the tray loading motor stops.

When the tray closes the operation is as follows. If the tray OPEN/CLOSE button or tray is pressed and the detection switch is turned off, the tray loading motor rotates clockwise, so that the tray is retracted. When the detection switch is turned on again, the tray loading motor stops.



### (2) Pickup feed mechanism

When the sled motor (A) rotates, the rack (C) moves through the sled pinion (B) so that the pickup (D) is moved to the internal or external periphery.

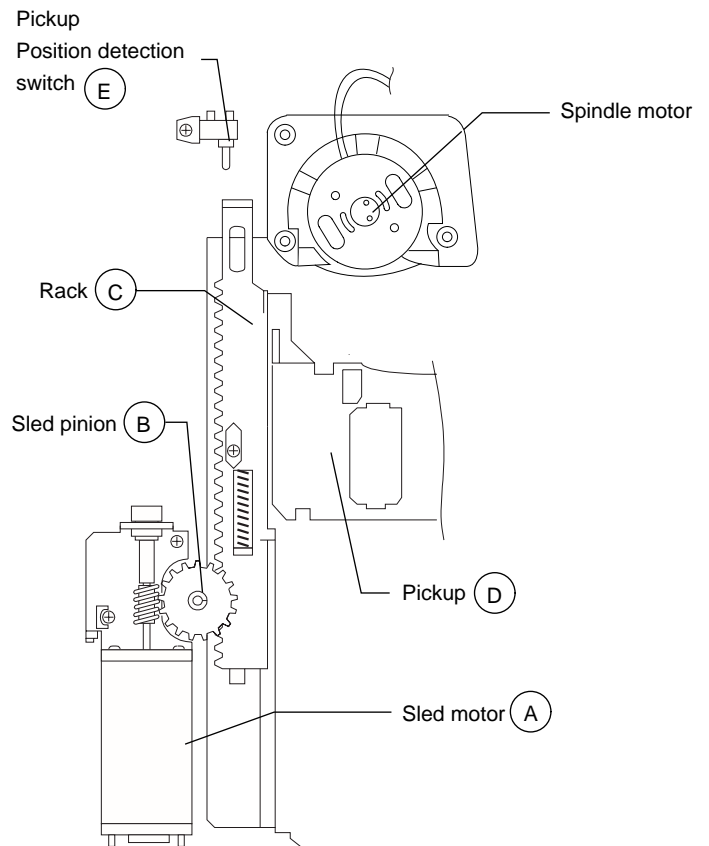
When it is moved to the innermost periphery, the position detection switch (E) is pushed by the rack, so that the position of pickup is initialized.

### (3) Disc rotation mechanism

The spindle motor is used to rotate.

IC701 is used to control.

When the spindle motor is replaced, replace the spindle unit.

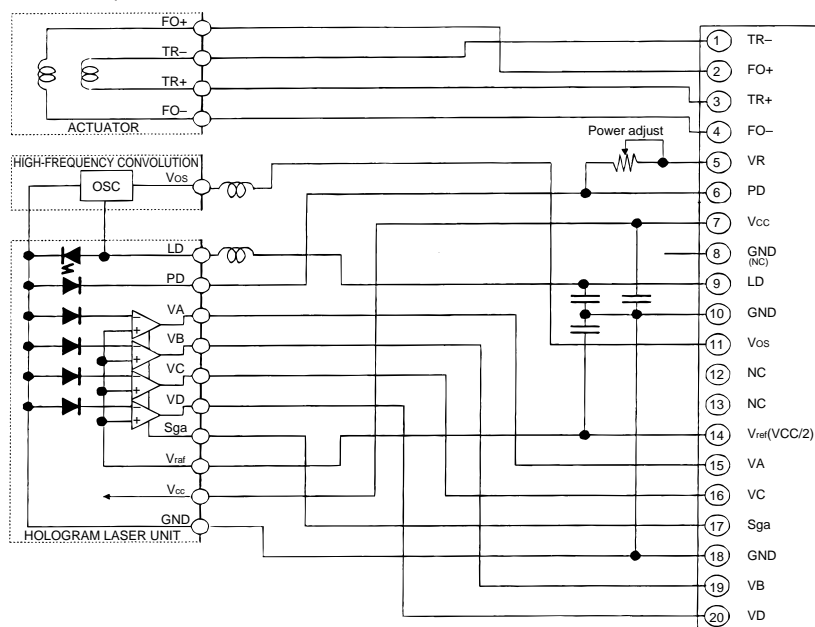


## 8. OPERATION OF PICKUP

### 8-1. CIRCUIT CONFIGURATION OF PICKUP

The pickup unit reads signals from the disk, and the flexible cable is connected to the board. The following signals flow through the cable.

### 8-2. EQUIVALENT CIRCUIT OF PICKUP



### 8-3. POLARITIES OF SIGNAL

Focus FO+, FO-	When electric current is flowed from FO+ to FO-, the lens comes to near the disk.	
Tracking TR+, TR-	When electric current is flowed from TR+ to TR-, the lens goes toward the outer circumference.	
Gain switching Sga	DVD one Layer DVD two Layer CD	High gain Sga : +5V

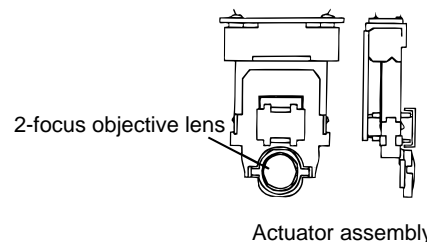
### 8-4. SIGNALS OF PICKUP

#### 8-4-1. Tracking drive signal (TR+, TR-)

The signal drives the tracking servo mechanism which projects the beam on the track by moving the objective lens (OL) to the outer or inner circumference (at a right angle against the track) of the disk.

#### 8-4-2. Focus drive signal (FO+, FO-)

The signal drives the focus servo mechanism which aligns the focus on the pit of the disk by elevating OL (vertically against the disk surface.)



The VR terminal is connected to GND.

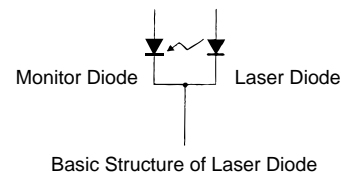
#### 8-4-3. Monitor Diode (PD)

Since the laser diode largely varies output of the laser light even if the flowing current is slightly varied, the projection light is detected with the monitor diode to control the laser light to be equally output.

Since the current varies on the monitor diode according to the intensity of the received light of the laser diode, the drive current of the laser diode is reduced if the current of the monitor diode increases. On the contrary, the drive current of the laser diode is increased if the current of the monitor diode decreases.

As the projection light of the laser diode becomes stronger, the current of the monitor diode increases to increase the current which flows into the monitor diode output (PD). This is input to the pin 44 of IC303 and is compared with the reference voltage to control the drive current of the laser diode.

The circuit is called ALPC (Automatic Laser Power Control).



#### 8-4-4. Laser diode drive current control (LD)

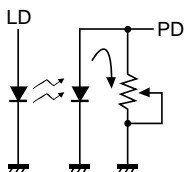
Power supply to drive the laser diode

#### 8-4-5. High-frequency convolution module power supply (VOSC)

The high-frequency convolution imposes the high-frequency signal on the DC current to impose the high frequency on the drive current of the laser. Thus, the interference of outgoing light and reflected light is prevented.

#### 8-4-6. HF Signal (VA, VB, VC, VD)

Signals recorded in the disk



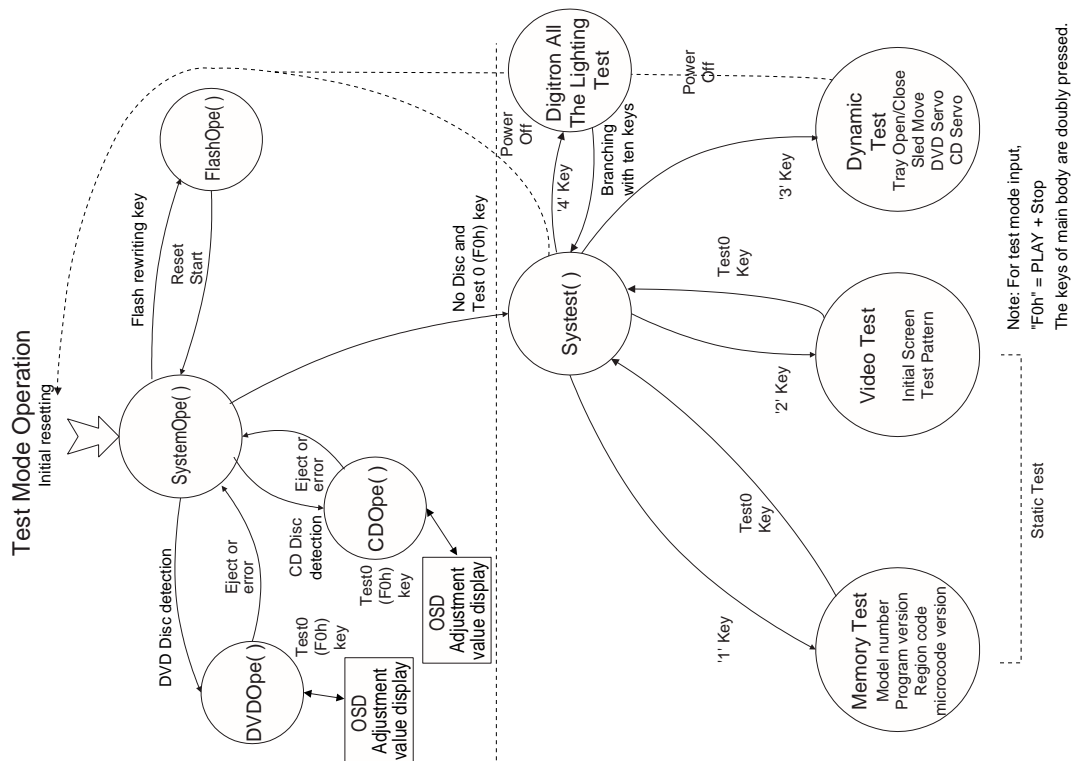
When the quantity of laser light increases, the current shown in figure increases and the PD terminal voltage rises.

IC303 is used to control. The LD terminal voltage lowers, and the quantity of light reduces. (IC303 is actuated by voltage input.)

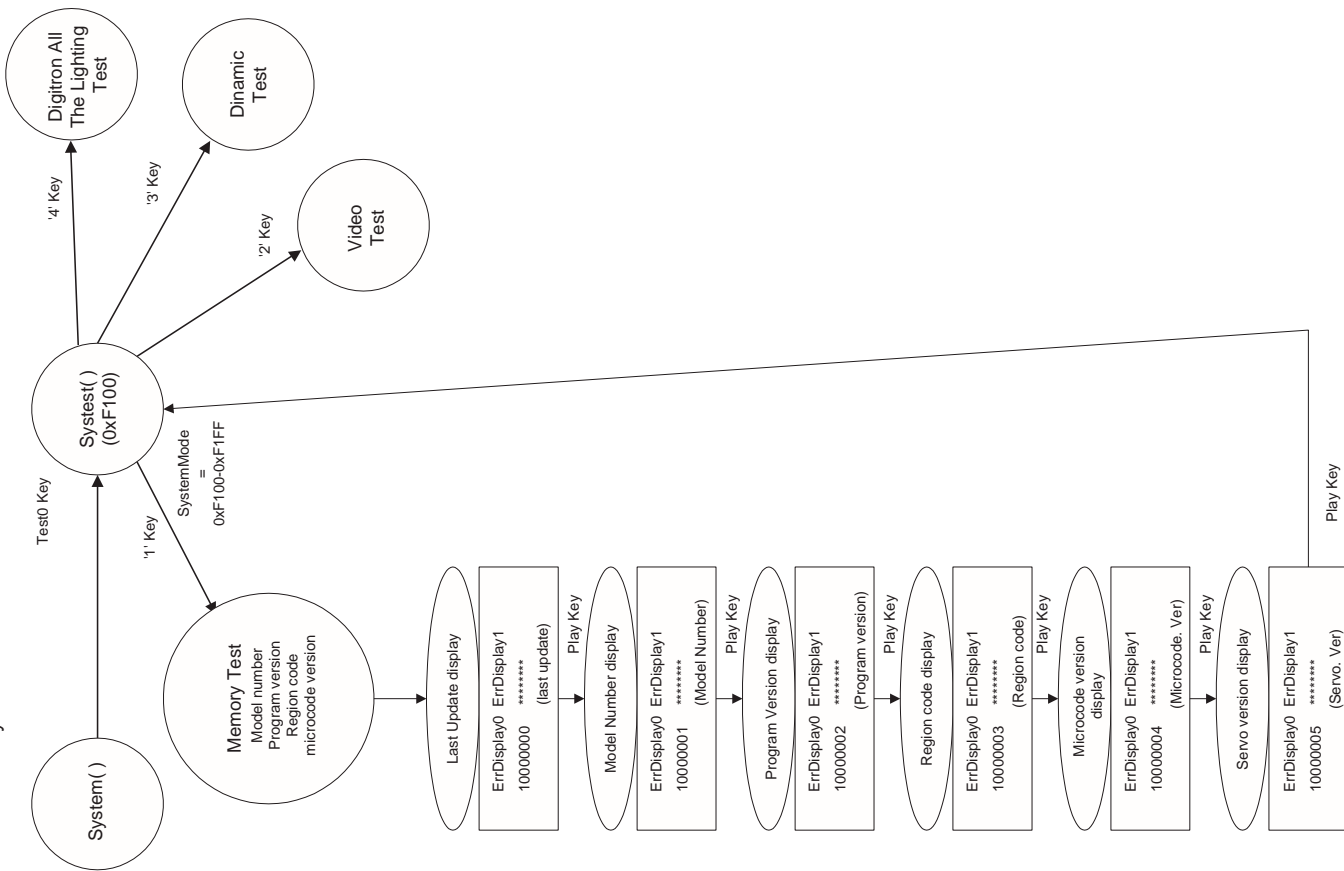
## 9. TEST MODE

Memory Test Mode	Program version indication.
Video Test Mode	Ordinary test pattern indication, and copy guard signal added test pattern indication are given.
Mecha Test Mode	Servo system initialization, tray opening and closing, laser, servo, continuous playback, jump test are performed.
Servo adjustment value read mode	Servo version indication, VC/FE/TE/RF AVRG, TRVSC, RF LEVEL, FO BIAS, FO GAIN, TR GAIN indication are given.

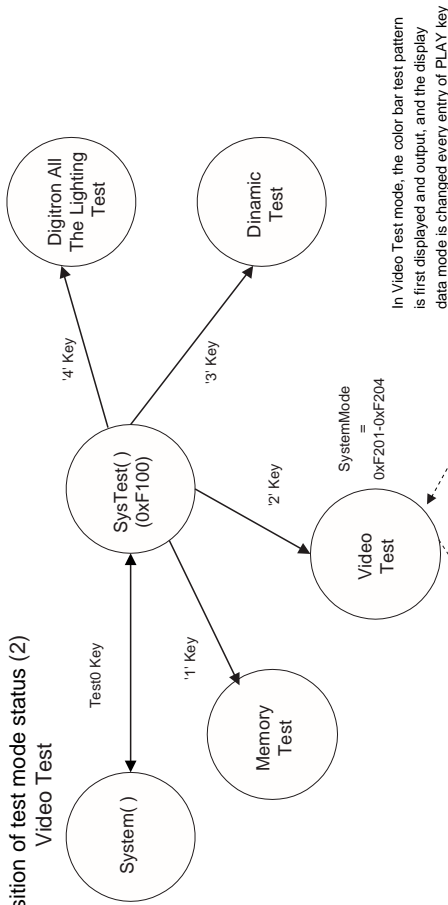
### 9-1. EXPLANATION OF OPERATION AT THE SYSTEM START



### Transition of test mode status (1) Memory Test

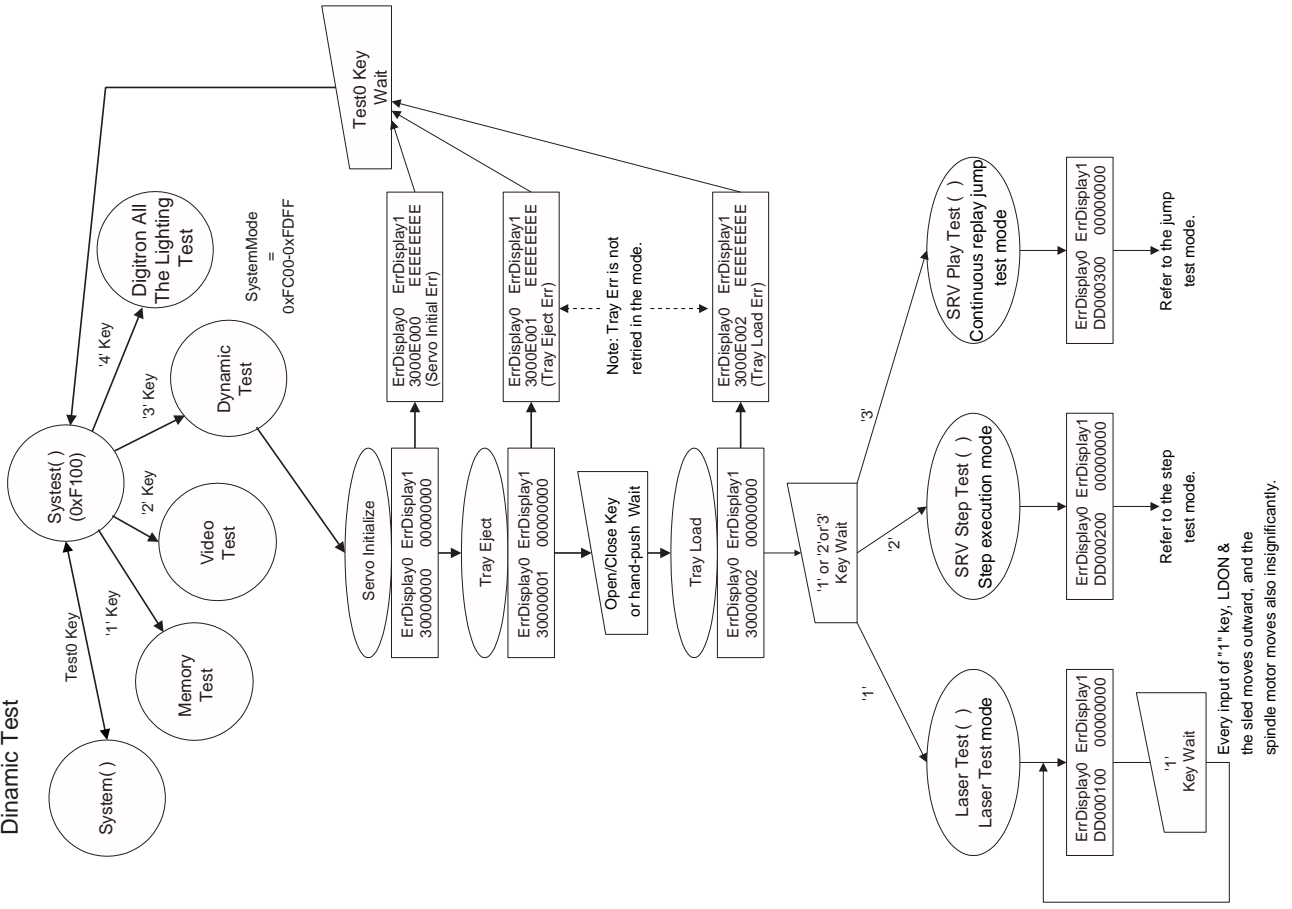


Transition of test mode status (2)  
Video Test



In Video Test mode, the color bar test pattern is first displayed and output, and the display data mode is changed every entry of PLAY key as shown in the right. Here, it returns to SysTest ( ) if any Test 0 (F0h) key is input in the test display.

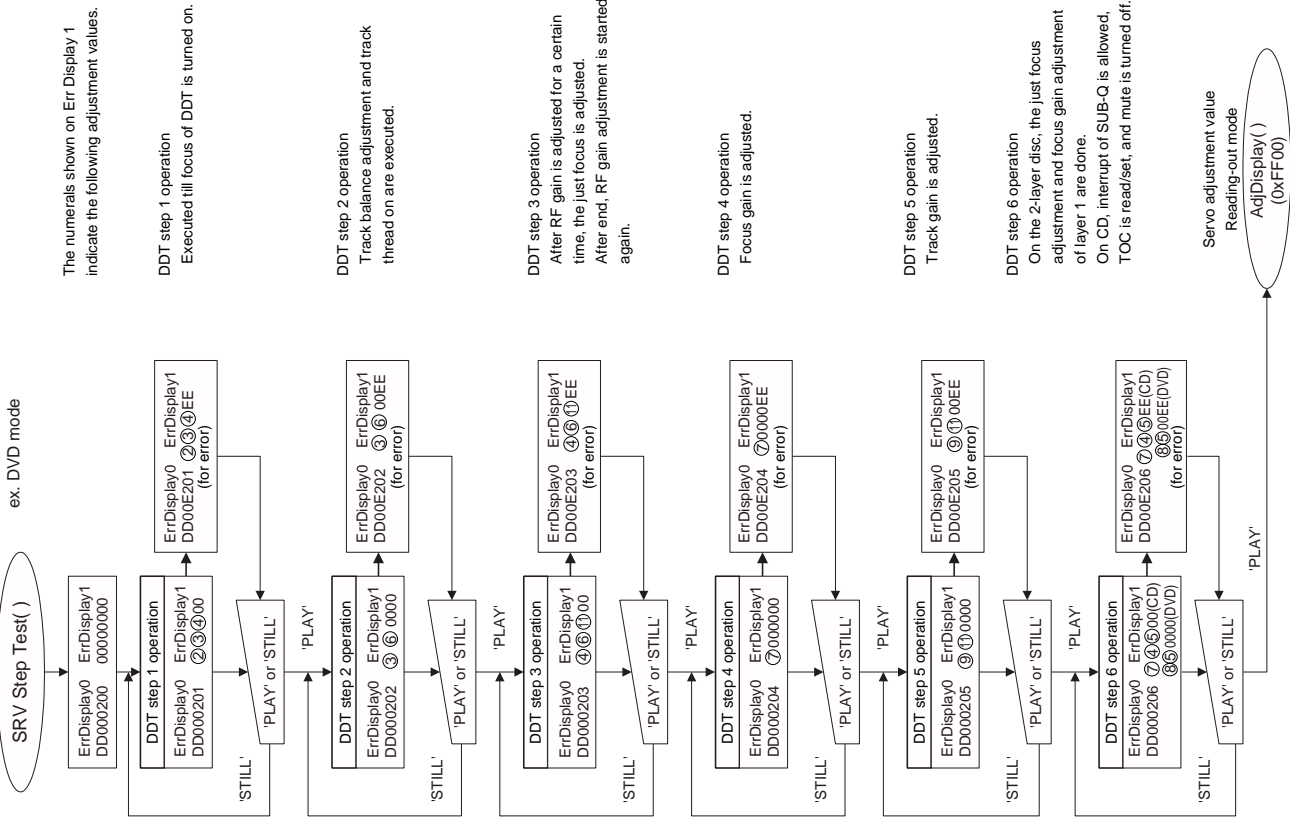
Transition of test mode status (3)  
Dynamic Test



Every input of '1' key, LDON & the sled moves outward, and the spindle motor moves also insignificantly.

SRV Step Test()  
Step Test Mode

ex. DVD mode



The numerals shown on Err Display 1 indicate the following adjustment values.

DDT step 1 operation  
Executed till focus of DDT is turned on.

DDT step 2 operation  
Track balance adjustment and track thread on are executed.

DDT step 3 operation  
After RF gain is adjusted for a certain time, the just focus is adjusted.  
After end, RF gain adjustment is started again.

DDT step 4 operation  
Focus gain is adjusted.

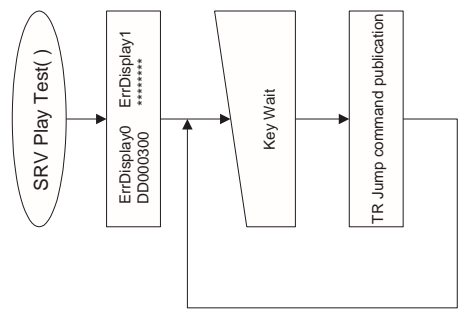
DDT step 5 operation  
Track gain is adjusted.

DDT step 6 operation  
On the 2-layer disc, the just focus adjustment and focus gain adjustment of layer 1 are done.  
On CD, interrupt of SUB-Q is allowed, TOC is read/set, and mute is turned off.

- ②..... Focus Offset
- ③..... Track Offset
- ④..... 0-Layer Focus Balance
- ⑤..... 1-Layer Focus Balance
- ⑥..... Track Balance
- ⑦..... 0-Layer Focus Gain
- ⑧..... 1-Layer Focus Gain
- ⑨..... Track Gain
- ⑩..... RF Gain

In case of CD, focus balance after correction.

SRVPlayTest()  
Continuous replay & jump mode



In the continuous replay mode, the current sector address is displayed on ErrDisplay 1.

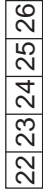
In SRV Play Test ( ), key is input and number of TR jumps is specified as follows.

Key Name	(Code)	Jump	Number of TRs	Key Name	(Code)	Jump	Number of TRs
[1]	01h	-1		[3]	02h	+1	
[4]	04h	-102		[6]	06h	+102	
[7]	07h	-510		[9]	09h	+510	
[Clear]	1Fh	-511	[Memory]	[Repeat]	1Ch	+511	
[2]	02h	-765		[A-B]	35h	+765	
[5]	05h	-766		[Program]	36h	+766	
[8]	08h	-7000		[Skip(+)]	1Eh	+7000	
[Skip(-)]	2Dh	-15000			2Eh	+15000	

[Next replay] = Layer Jump

\* Here, key allocation may be changed.  
\* Layer jump operation is not guaranteed except during 2-layer DVD test.

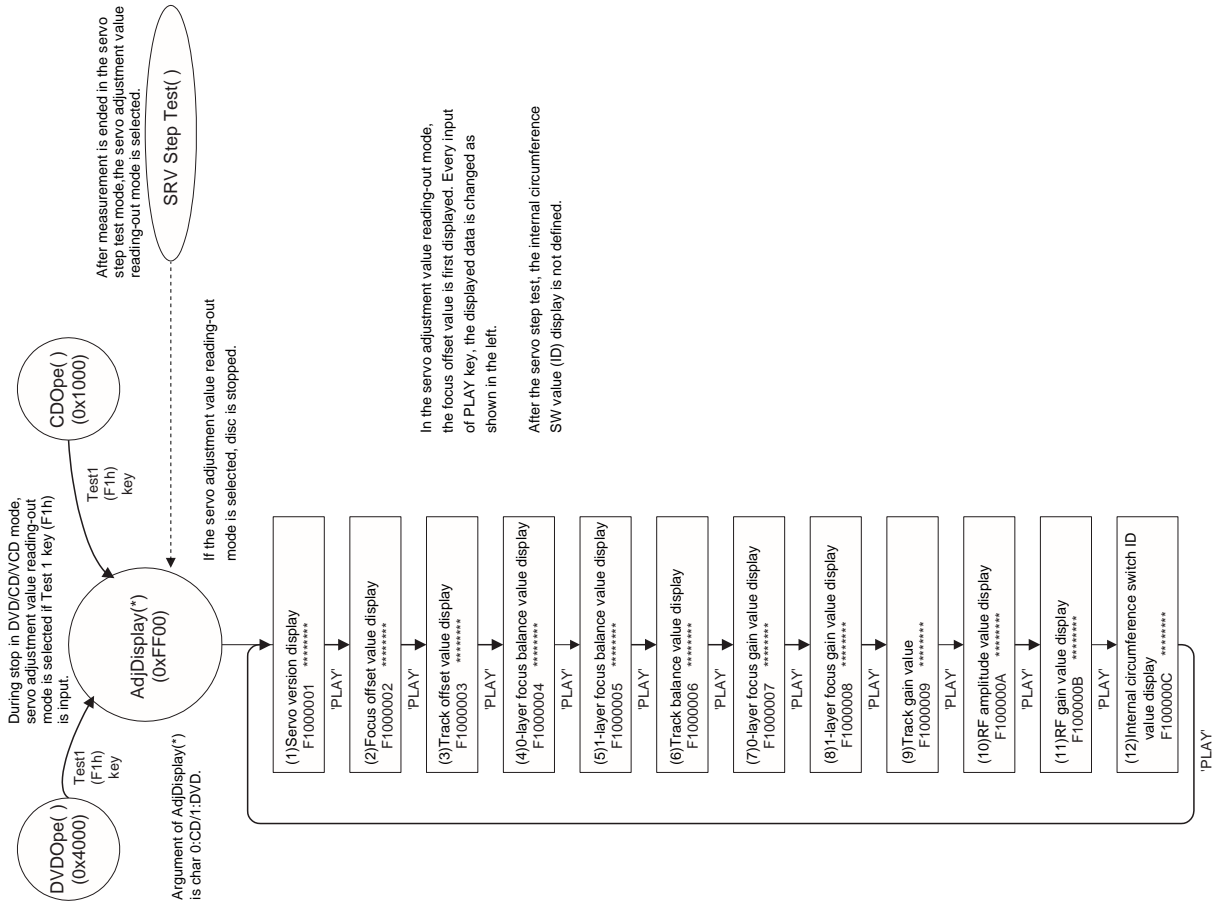
OSD adjustment value display  
 1. Press "FOh" key during disc replay. (Multiple press of S. PICTURE and STOP)  
 2. The following screen is displayed on OSD.  
 3. OSD display is turned off with "FOh" key.



- (1) 1, 2 ..... 0-layer focus gain
- (2) 3, 4 ..... 1-layer focus gain
- (3) 5, 6 ..... 0-layer focus balance
- (4) 7, 8 ..... 1-layer focus balance (In case of CD, 0-Layer focus balance after correction.)
- (5) 9, 10 ..... Track offset
- (6) 11, 12 ..... Track gain
- (7) 13, 14 ..... Track balance
- (8) 15, 16 ..... RF gain

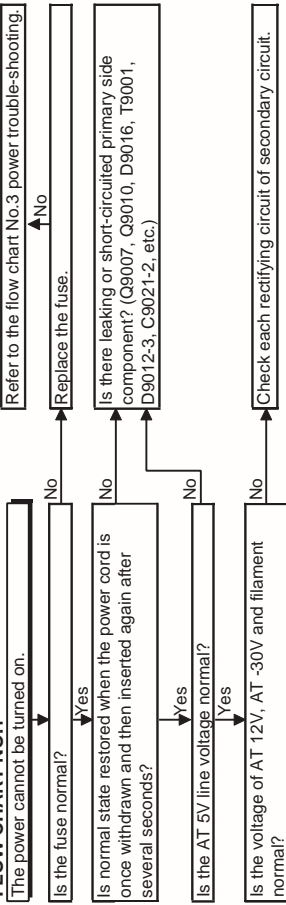
Hexadecimal data from (1) to (8).

Servo adjustment value reading-out mode

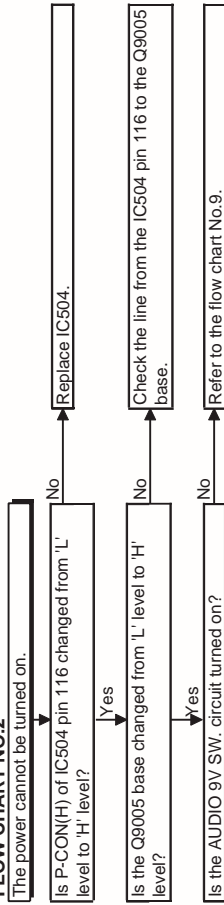


# 10. TROUBLESHOOTING

## FLOW CHART NO.1



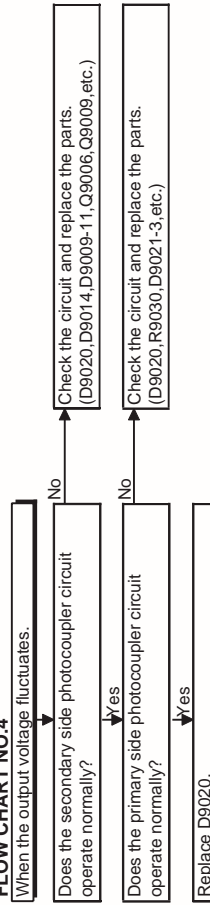
## FLOW CHART NO.2



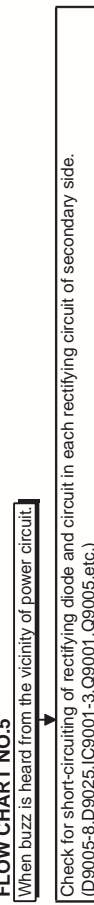
## FLOW CHART NO.3



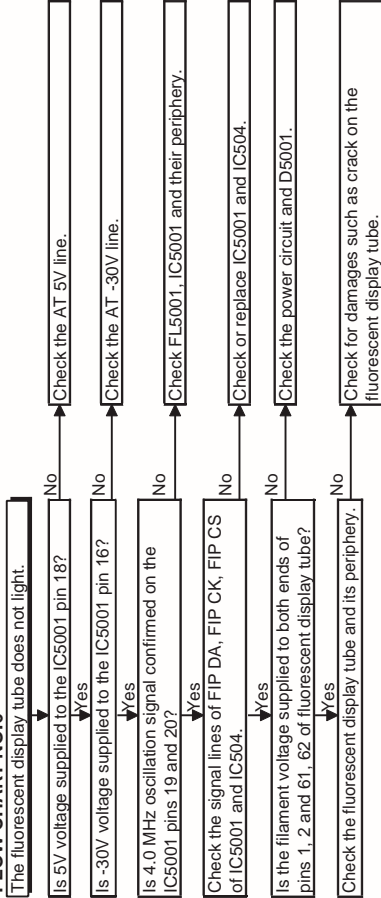
## FLOW CHART NO.4



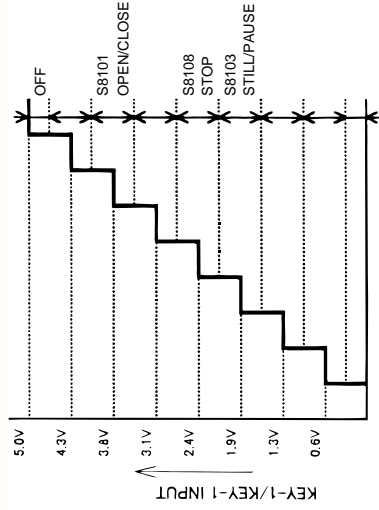
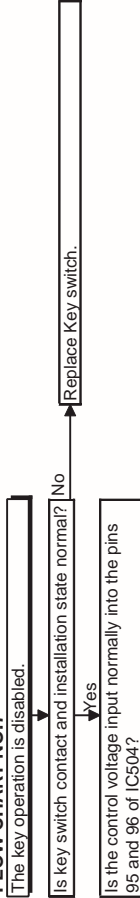
## FLOW CHART NO.5



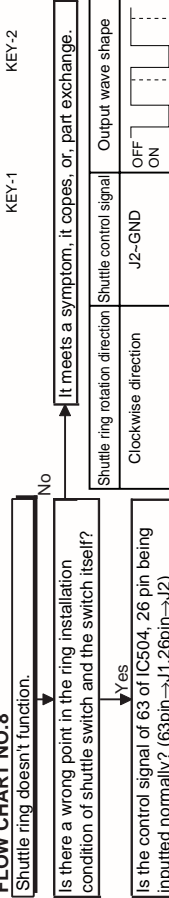
## FLOW CHART NO.6



## FLOW CHART NO.7

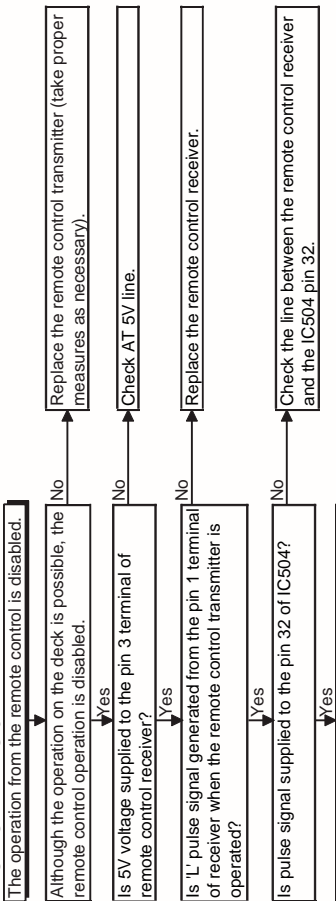


## FLOW CHART NO.8

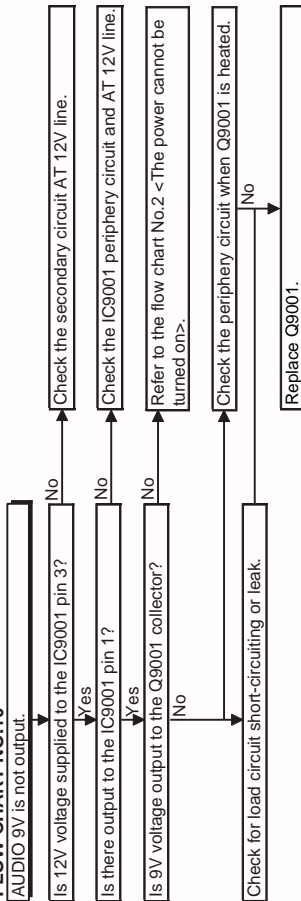


Shuttle ring rotation direction	Shuttle control signal	Output wave shape
Clockwise direction	J2-GND	OFF ON
	J1-GND	OFF ON
Counterclockwise direction	J2-GND	OFF ON
	J1-GND	OFF ON

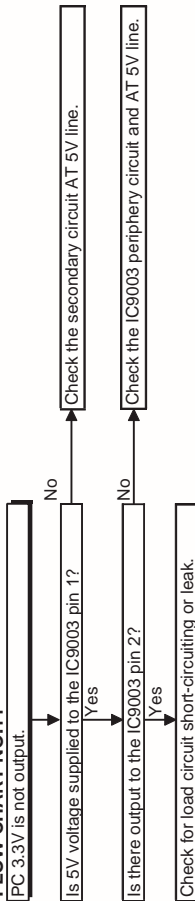
**FLOW CHART NO.9**



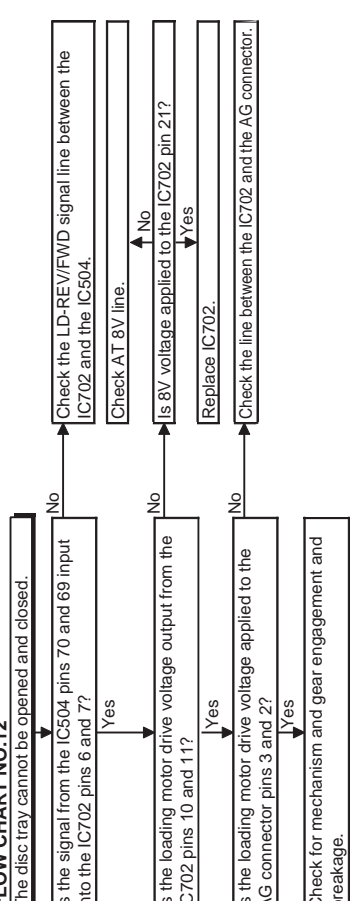
**FLOW CHART NO.10**



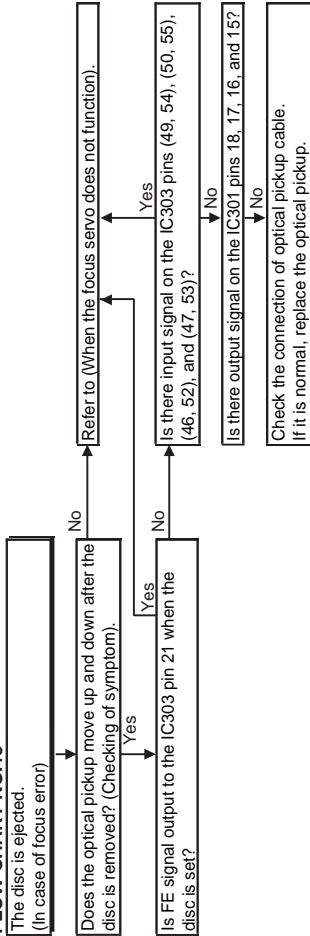
**FLOW CHART NO.11**



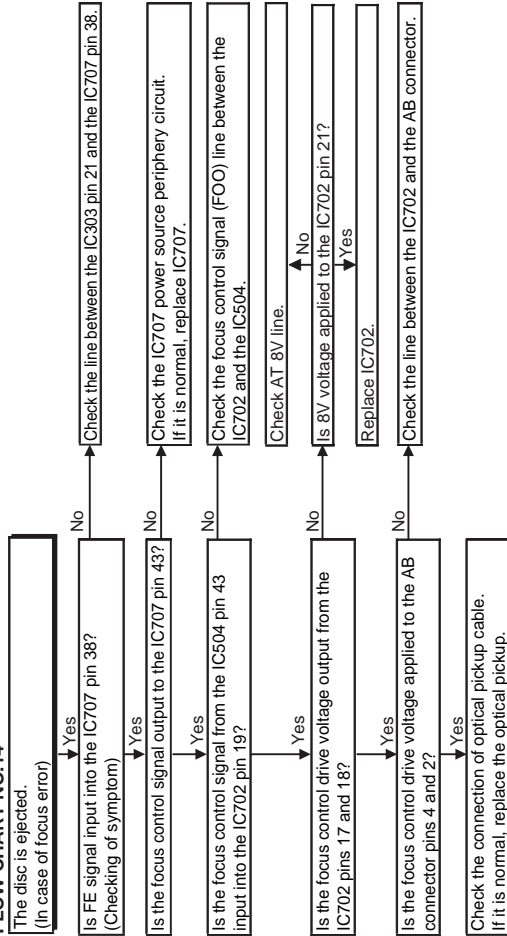
**FLOW CHART NO.12**



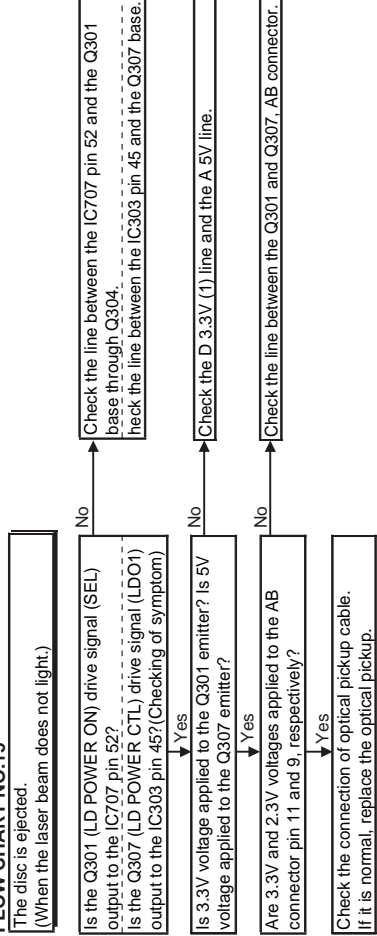
**FLOW CHART NO.13**



**FLOW CHART NO.14**

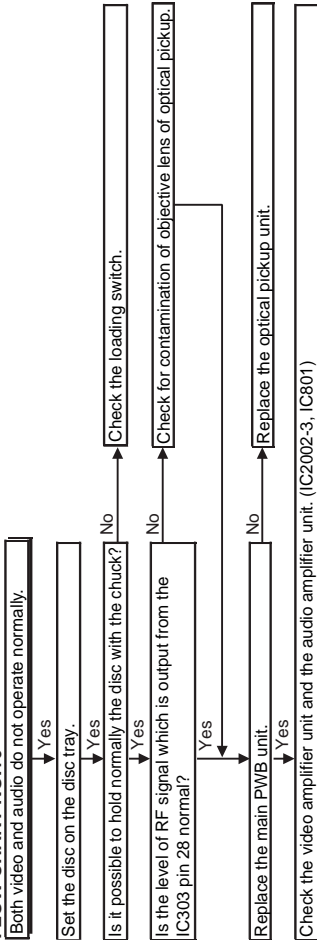


**FLOW CHART NO.15**

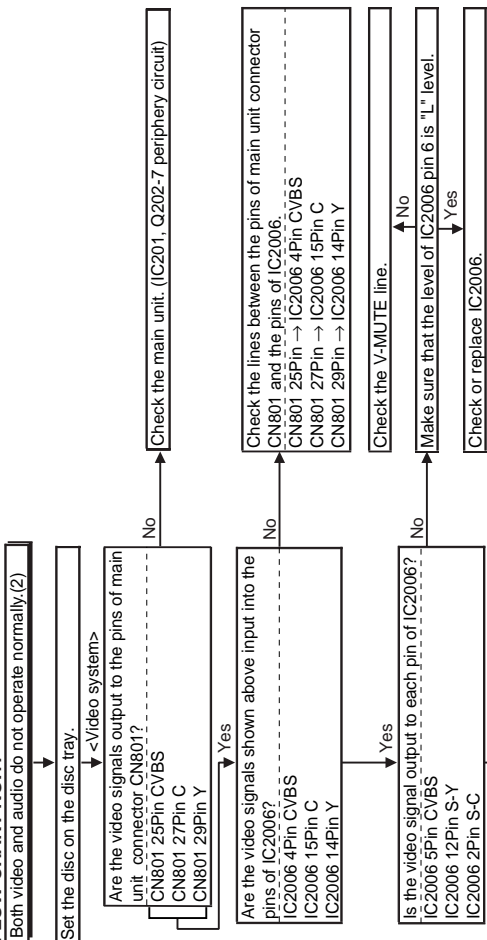




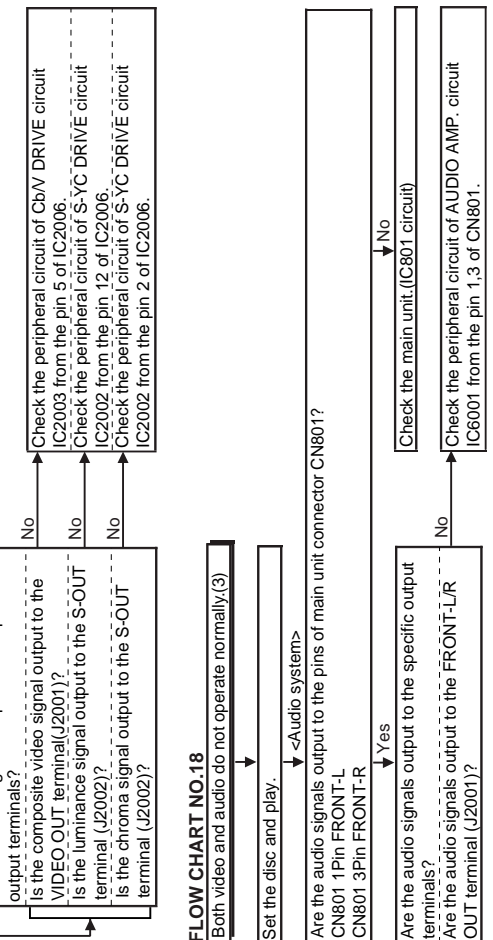
**FLOW CHART NO.16**



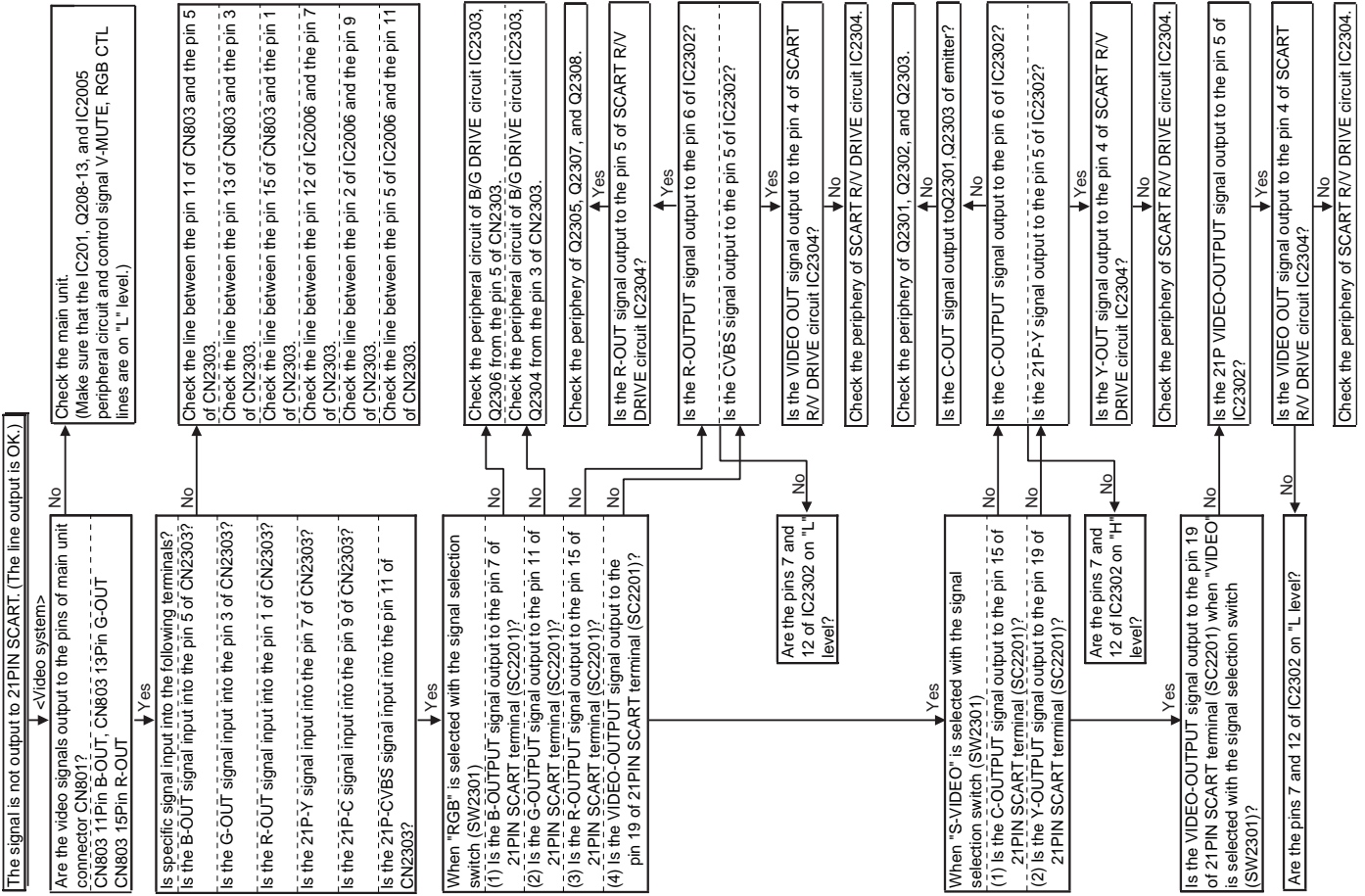
**FLOW CHART NO.17**



**FLOW CHART NO.18**



**FLOW CHART NO.19**

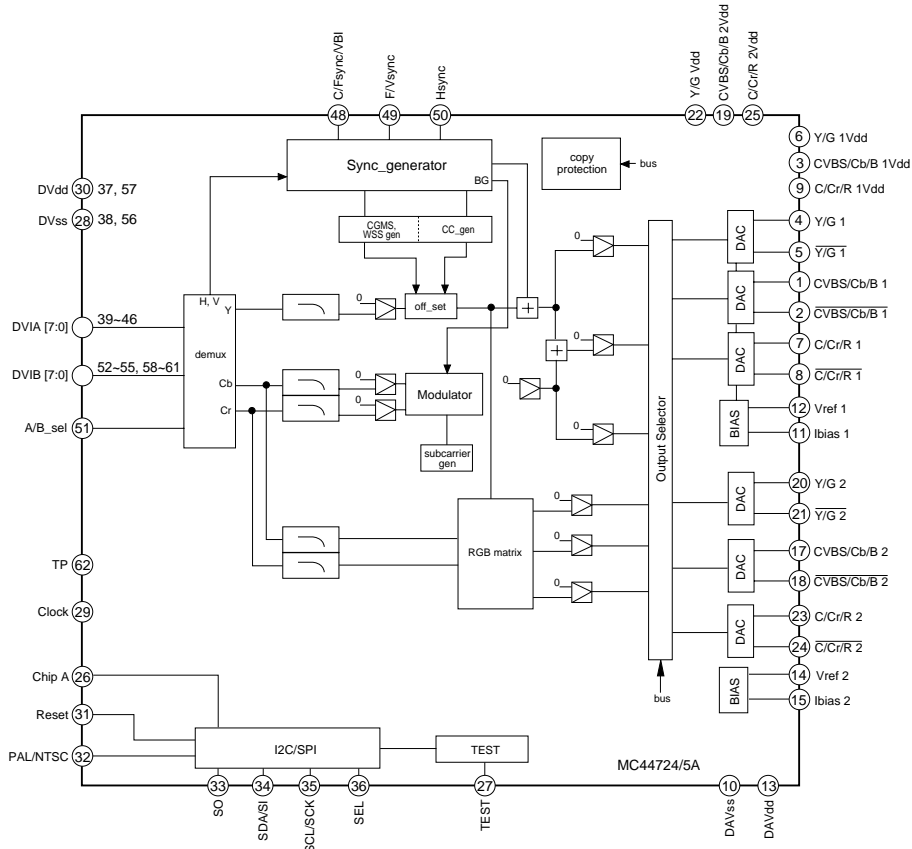


## 11. IC FUNCTION LIST

### 11-1. IC201 MC44724A DIGITAL VIDEO ENCODER

Pin No.	Terminal name	I/O	Operation function
1	CVBS/Cb/B1	O	Analog composite video signal output or Cb or B signal output current drive (positive)
2	$\overline{\text{CVBS/Cb/B1}}$	O	Analog composite video signal output or Cb or B signal output current drive (negative)
3	CVBS/Cb/B1 Vdd		Power Supply for CVBS / Cb/B DAC1 circuit
4	Y/G 1	O	Analog luminance or G signal output current drive (positive)
5	$\overline{\text{Y/G 1}}$	O	Analog luminance or G signal output current drive (negative)
6	Y/G 1Vdd		Power Supply for Y/G DAC1 circuit
7	C/Cr/R 1	O	Analog chrominance signal output or Cr or R signal output current drive (positive)
8	$\overline{\text{C/Cr/R 1}}$	O	Analog chrominance signal output or Cr or R signal output current drive (negative)
9	C/Cr/R 1Vdd		Power Supply for C/Cr/R DAC1 circuit
10	DA Vss		Ground for DAC circuit
11	Ibias 1	O	Reference current for the 1st set of 3 DACs
12	VRef 1		Reference full scale voltage for the 1st set of 3 DACs
13	DA Vdd		Power Supply for DACs
14	VRef 2		Reference full scale voltage for the 2nd set of 3 DACs
15	Ibias 2	O	Reference current for 2nd set of the 3 DACs
16	NC		No connect to pin
17	CVBS/Cb/B2	O	Analog composite video signal output or Cb or B signal output current drive (positive)
18	$\overline{\text{CVBS/Cb/B2}}$	O	Analog composite video signal output or Cb or B signal output current drive (negative)
19	CVBS/Cb/B2 Vdd		Power Supply for CVBS / Cb/B DAC2 circuit
20	Y/G 2	O	Analog luminance or G signal output current drive (positive)
21	$\overline{\text{Y/G 2}}$	O	Analog luminance or G signal output current drive (negative)
22	Y/G Vdd		Power Supply for Y/G DAC2 circuit
23	C/Cr/R 2	O	Analog chrominance signal output or Cr or R signal output current drive (positive)
24	$\overline{\text{C/Cr/R 2}}$	O	Analog chrominance signal output or Cr or R signal output current drive (negative)
25	C/Cr/R 2Vdd		Power Supply for C/Cr/R DAC2 circuit
26	ChipA		I2C chip address select {0 : 40(hex)/41(hex) 1 : 1D(hex)/1E(hex)}
27	TEST	I	TEST pin (Ground)
28	DVss		Ground for Digital circuit
29	CLOCK	I	27MHz clock input
30	DVdd		Power Supply for Digital circuit
31	Reset	I	Reset signal, active LOW
32	PAL/NTSC	I	NTSC/PAL select. This pin is sampled only at Reset.(NTSC : Low PAL : High)
33	SO	z(O)	In SPI mode, serial data output / In I2C mode, grounded.
34	SDA/SI	I/O(I)	Serial data input, Open drain output / If SPI mode, serial data input
35	SCL/SCK	I	Serial clock
36	SEL	I/(I)	Connect to Ground / If SPI mode, this pin is chip select
37	DVdd		Power supply for Digital circuit
38	DVss		Ground for Digital circuit
39-46	DVIA7-0	I/O	8-bit Multiplexed Y/Cr/Cb 4:2:2 data (ITU Rec656/601) input (DVIA) or Multiplexed Y data (ITU-Rec656/601) input in 16-bit input mode
47	Vmute	I	Video mute on Reset (0: normal, 1: mute)
48	C/Fsync/VBI	I/O	Csync/Frame sync input/output
49	F/Vsync	I/O	Frame sync or Vertical sync input/output
50	Hsync	I/O	Horizontal sync input/output
51	A/B sel	I	Switch control for 8-bit x 2 Multiplexed 4:2:2 data (ITU Rec656/601) input (DVIA) or (DVIB)
52-55	DVIB7-4	I/O	8-bit Multiplexed 4:2:2 data (ITU Rec656-601) input (DVIB), or Multiplexed Cr/Cb data (ITU Rec656/601) input in 16-bit input mode
56	DVss		Ground for Digital circuit
57	DVdd		Power Supply for Digital circuit
58-61	DVIB3-0	I/O	Multiplexed 4:2:2 data (ITU Rec656/601) input (DVIB), or Multiplexed Cr/Cb data (ITU Rec656/601) input in 16-bit input mode
62	TP	I/O	Test data input/output (Grounded)
63,64	NC		No connect to pin (Ground)

• Block Diagram



11-2. IC301 IX1461GE RF PRE AMP.

Pin No.	Terminal name	I/O	Operation function
1	EIN	I	RF signal input. Input of RF signal output of optical pickup.
2	GND1	-	Ground
3	S/DUAL	I	Single layer/dual layer selection signal input.
4	AIN	I	RF signal input. Input of RF signal output of optical pickup.
5	BIN	I	RF signal input. Input of RF signal output of optical pickup.
6	CIN	I	RF signal input. Input of RF signal output of optical pickup.
7	DIN	I	RF signal input. Input of RF signal output of optical pickup.
8	VrefIN	I	Reference voltage input. (2.1V)
9	FIN	I	RF signal input. Input of RF signal output of optical pickup.
10	GAINsel1	I	Amp gain selection input 1.
11	VCC1	-	Power terminal. (5.0V)
12	GAINsel2	I	Amp gain selection input 2.
13	FOUT	O	RF signal output. Input RF signal is current-voltage-converted and output.
14	EOUT	O	RF signal output. Input RF signal is current-voltage-converted and output.
15	DOUT	O	RF signal output. Input RF signal is current-voltage-converted and output.
16	COUT	O	RF signal output. Input RF signal is current-voltage-converted and output.
17	BOUT	O	RF signal output. Input RF signal is current-voltage-converted and output.
18	AOUT	O	RF signal output. Input RF signal is current-voltage-converted and output.
19	VCC2	-	Power terminal. (5.0V)
20	RFPOUT	O	Data read signal output. The same phase as MIXIN.
21	RFNOUT	O	Data read signal output. Reverse phase with respect to MIXIN.
22	MIXIN	I	Data read signal input.
23	MIXOUT	O	Data read signal output.
24	GND2	-	Ground

• Mode selection table

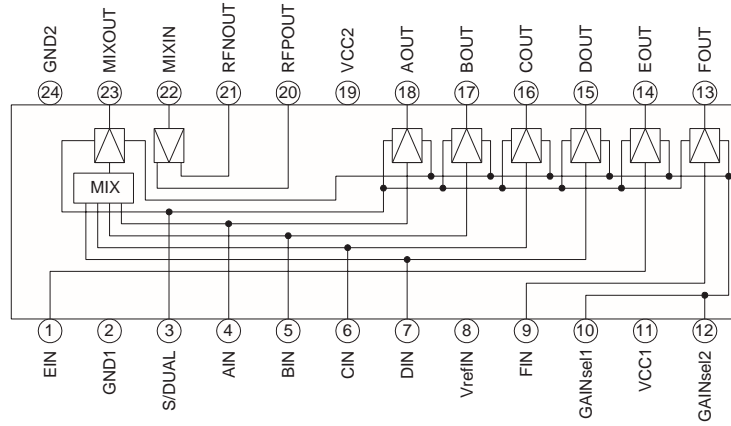
Single layer/dual layer selection

Layer	S/DSEL (Terminal 3)	Amp gain
Single	L, OPEN	0dB
Dual	H	+10dB

Amp. gain selection

GAINsel1 (Terminal 10)	GAINsel2 (Terminal 12)	Amp gain
L	L	+6dB
H, OPEN	L	-2dB
L	H, OPEN	+2dB
H, OPEN	H, OPEN	-6dB

• Block Diagram

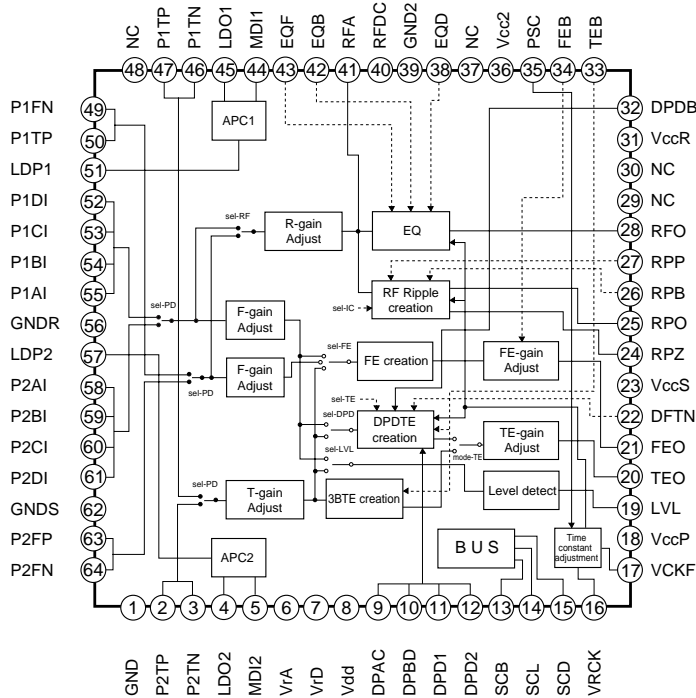


11-3. IC303 IX1517GE RF SIGNAL PROCESSOR

Pin No.	Terminal name	I/O	Operation function	Terminal DC Voltage(TYP.)	Remarks
1	GND	–	GND terminal.	–	
2	P2TP	I	TE+input (CD)	VrA	
3	P2TN	I	TE–input (CD)	VrA	
4	LDO2	O	Drive ouput	–	
5	MDI2	I	Monitor input	–	
6	VrA	O	Analog VREF	2.1[V]	
7	VrD	O	Digital VREF	–	Vdd 1/2
8	Vdd	I	Power terminal	–	4.2V (3.3V)
9	DPAC	–	DPD AC combination capacity 1	–	
10	DPBD	–	DPD AC combination capacity 2	–	
11	DPD1	–	DPD integral capacity 1	–	
12	DPD2	–	DPD integral capacity 2	–	
13	SCB	I	Control line (Bit clock)	2.2[V]	
14	SCL	I	Control line (Latch signal)	2.2[V]	
15	SCD	I	Control line (Serial Data)	2.2[V]	
16	VRCK	I	Reference clock input	2.3[V]	When frequency is increased, the filters excepting the servo LPF are shifted to high frequency side.
17	VCKF	–	Capacity for time constant adjustment	–	
18	VccP	–	Power terminal	–	
19	LVL	O	Servo addition output	Vrd x (1/2)	
20	TEO	O	TE output	VrD	
21	FEO	O	FE output	VrD	
22	DFTN	I	DPD difect	–	Low DPD output: Mute
23	VccS	–	Power terminal (servo)	–	
24	RPZ	O	RF ripple center voltage	VrD	
25	RPO	O	RF ripple output	VrD	
26	RPB	O	RF ripple bottom	–	
27	RPP	O	RF ripple peak	–	
28	RFO	O	Equalizing RF output	2.3[V]	
29	NC	–	NC terminal	–	To be connected to GND
30	NC	–	NC terminal	–	To be connected to GND
31	VccR	–	Power terminal (RF)	–	
32	DPDB	I	Pit depth adjustment	VrD	When D PDB is raised, the A/B side delay increases.
33	TEB	I	TE balance	VrD	When TEB is raised, the TP side gain increases and the A+C side delay increases.
34	FEB	I	FE balance	VrD	When FEB is raised, the A+C (FP) side gain increases.
35	PSC	I	VRCK frequency division ON/OFF	–	High: Frequency division OFF
36	Vcc2	–	Power terminal	–	
37	NC	–	NC terminal	VrD	To be connected to VrD, or to GND through C
38	EQD	I	Group delay correction	VrD	When EQD is raised, the group delay increases at the right side.
39	GND2	–	GND terminal.	–	
40	RFDC	–	DC feedback capacity	–	

Pin No.	Terminal name	I/O	Operation function	Terminal DC Voltage(TYP.)	Remarks
41	RFA	O	RF total addition output	2.2[V]	
42	EQB	I	Boost adjustment	VrD	When EQB is raised, the boost increases.
43	EQF	I	Frequency adjustment	VrD	When EQF is raised, shift to the high frequency side occurs.
44	MDI1	I	Monitor input	-	
45	LDO1	O	Drive output	-	
46	P1TN	I	TE-input (DVD)	VrA	
47	P1TP	I	TE+input (DVD)	VrA	
48	NC	-	NC terminal	-	To be connected to GND
49	P1FN	I	FE-input (DVD)	VrA	
50	P1TP	I	FE+input (DVD)	VrA	
51	LDP1	I	APC polarity 1	-	Positive polarity when this terminal is connected to Vcc.
52	P1DI	I	D input (DVD)		
53	P1CI	I	C input (DVD)	VrA	
54	P1BI	I	B input (DVD)	VrA	
55	P1AI	I	A input (DVD)	VrA	
56	GNDR	-	GND terminal (RF)	-	
57	LDP2	I	APC polarity 2	-	Positive polarity when this terminal is connected to Vcc.
58	P2AI	I	A input (CD)	VrA	
59	P2BI	I	B input (CD)	VrA	
60	P2CI	I	C input (CD)	VrA	
61	P2DI	I	D input (CD)	VrA	
62	GNDS	-	GND terminal (Servo)	-	
63	P2FP	I	FE+input (CD)	VrA	
64	P2FN	I	FE-input (CD)	VrA	

• Block Diagram



11-4. IC401 IX1484GE 4M DRAM

Terminal	Terminal name	Function
10~13,16~20,9	A0~A8,A9R	Address input
8	RAS	Row address strobe
23	CAS	Column address strobe
1~5,24~27	DQ1~DQ8	Data input/Data output
22	OE	Output enable
7	WE	Light enable
1, 14	Vcc	Power (5V)
15, 28	Vss	Ground (0V)
6, 21	NC	Not connected

### 11-5. IC402 IX1474GE DEM/ECC (DVD)

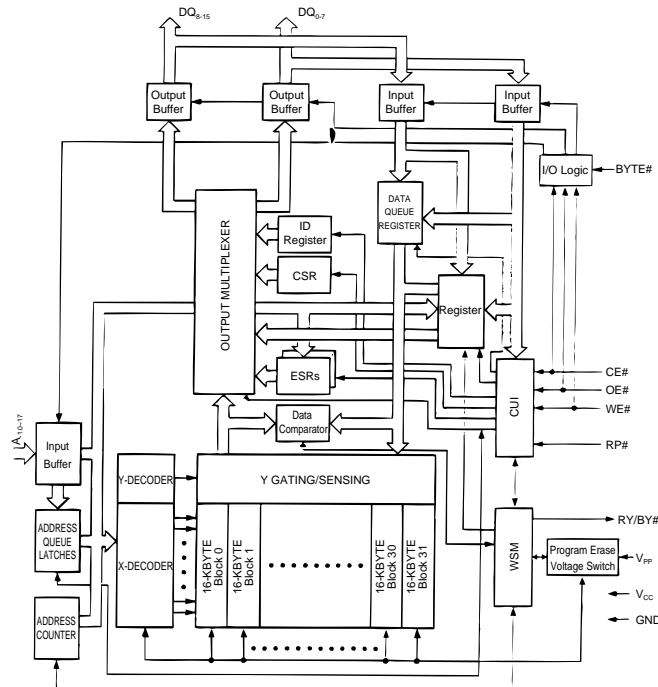
Pin No.	Terminal name	I/O	Operation function	Remarks
1	DPCK1	I	Signal processing reference clock input.	0.5-3.3Vp-p Feedback resistor built in.
2	DVDD3	-	Digital power. (3.3V)	For logic cell
3	SVCK1	I	Servo reference clock input. (Oscillation circuit input terminal)	3.3V-I/F Feedback resistor built in.
4	SVCK0	O	Servo reference clock output. (Oscillation circuit input terminal)	
5	DVSS	-	Digital power. (0V)	For logic cell
6	DVDD2	-	Digital power. (3.3V)	For logic cell
7	N.C.	-	User use prohibited.	Open
8	HDWR	I	MPU write signal.	TTL level
9	HDRD	I	MPU read signal.	TTL level
10	ECCCS	I	MPU chip selection.	TTL level
11	D8	I/O	MPU data bus.	TTL level
12	D9	I/O	MPU data bus.	TTL level
13	D10	I/O	MPU data bus.	TTL level
14	D11	I/O	MPU data bus.	TTL level
15	D12	I/O	MPU data bus.	TTL level
16	D13	I/O	MPU data bus.	TTL level
17	D14	I/O	MPU data bus.	TTL level
18	D15	I/O	MPU data bus.	TTL level
19	DVSS	-	Digital power. (0V)	For I/O cell
20	DVDD5	-	Digital power. (5V)	For I/O cell
21	HINT	O	MPU interruption signal. (Occurrence of interruption = "L")	OPEN DRAIN
22	HA0	I	MPU address bus.	TTL level
23	HA1	I	MPU address bus.	TTL level
24	PLCK	I/O	Read channel clock input/output terminal.	
25	ED0	-	User use is prohibited (N.C.) since it is for shipping adjustment.	Open
26	ED1	-		
27	ED2	-		
28	ED3	-		
29	ED4	-		
30	ED5	-		
31	ED6	-		
32	ED7	-		
33	TEST	I	For shipping adjustment.	Set to "L"
34	PDON	O	PLL phase error signal output. (Negative polarity)	
35	PDOP	O	PLL phase error signal output. (Positive polarity)	
36	RLLD	O	RLL detection result output.	
37	LPFN	I	PLL loop filter amp. reverse input.	
38	LPFO	O	PLL loop filter amp. output.	
39	VCOF	O	VCO filter terminal.	
40	SLCO	O	Built-in comparator reference voltage output terminal.	
41	AVSS	-	Analog power. (0V)	
42	AVR	O	Non-PLL system analog reference potential. (1.65V)	
43	VRC	-	Resistance division point potential. (For analog reference potential generation: 1.65)	
44	PVR	O	PLL system analog reference potential. (1.65V)	
45	AVDD	-	Analog power. (3.3V)	
46	RVR2	-	2nd reference voltage. (For capacitor connection)	
47	RVDD	-	Exclusive-use power terminal. (3.3V)	
48	RFIN	I	RF signal input.	
49	RVSS	-	Exclusive-use power terminal. (0V)	
50	RVR1	-	1nd reference voltage. (For capacitor connection)	
51	DVR	I	DMO reference potential. (1.65V recommended)	
52	DMO	O	Disc equalizer output for DVD. (Triple value PWM + HiZ)	
53	RASN	O	External RAM row address selection. (Negative logic)	
54	CASN	O	External RAM row address selection. (Negative logic)	

Pin No.	Terminal name	I/O	Operation function	Remarks
55	MOEN	O	External RAM output permission signal.	
56	MWEN	O	External RAM read/write selection.	
57	DVSS	–	Digital power. (0V)	For logic cell
58	DVDD3	–	Digital power. (3.3V)	For logic cell
59	MA9	O	External RAM address bus.	
60	MA8	O	External RAM address bus.	
61	MA7	O	External RAM address bus.	
62	MA6	O	External RAM address bus.	
63	MA5	O	External RAM address bus.	
64	MA4	O	External RAM address bus.	
65	MA3	O	External RAM address bus.	
66	MA2	O	External RAM address bus.	
67	MA1	O	External RAM address bus.	
68	MA0	O	External RAM address bus.	
69	DVSS	–	Digital power. (0V)	For I/O cell
70	DVDD5	–	Digital power. (5V)	For I/O cell
71	MD7	I/O	External RAM data bus.	TTL level
72	MD6	I/O	External RAM data bus.	TTL level
73	MD5	I/O	External RAM data bus.	TTL level
74	MD4	I/O	External RAM data bus.	TTL level
75	MD3	I/O	External RAM data bus.	TTL level
76	MD2	I/O	External RAM data bus.	TTL level
77	MD1	I/O	External RAM data bus.	TTL level
78	MD0	I/O	External RAM data bus.	TTL level
79	SD7	O	MPEG data output.	
80	SD6	O	MPEG data output.	
81	SD5	O	MPEG data output.	
82	SD4	O	MPEG data output.	
83	DVSS	–	Digital power. (0V)	For logic cell
84	DVDD3	–	Digital power. (3.3V)	For logic cell
85	SD3	O	MPEG data output.	
86	SD2	O	MPEG data output.	
87	SD1	O	MPEG data output.	
88	SD0	O	MPEG data output.	
89	SERR	O	MPEG data reliability flag. (Data error: "L")	
90	SOSO	O	MPEG output sector sync signal. (Sector top: "L")	
91	SVAL	O	MPEG data effective flag. (Effective state: "L")	
92	SDCK	O	MPEG data transfer clock.	
93	DVSS	–	Digital power. (0V)	For logic cell
94	SREQ	I	MPEG data request flag. (Request state: "L")	TTL level
95	RSTN	I	Hard reset input. (Reset state: "L")	
96	DVDD3	–	Digital power. (3.3V)	For logic cell
97	STDA	O	Operation state monitor data. (Output synchronizing with SDCK fall)	Common with PWM.
98	STCK	O	Operation state monitor sync signal. (Data top bit: "L")	Common with PWM.
99	UPWM	O	General-use PWM output.	4mA, 5V-I/F
100	DVSS	–	Digital power. (0V)	For logic cell

11-6. IC501 IX1539GE FLASH

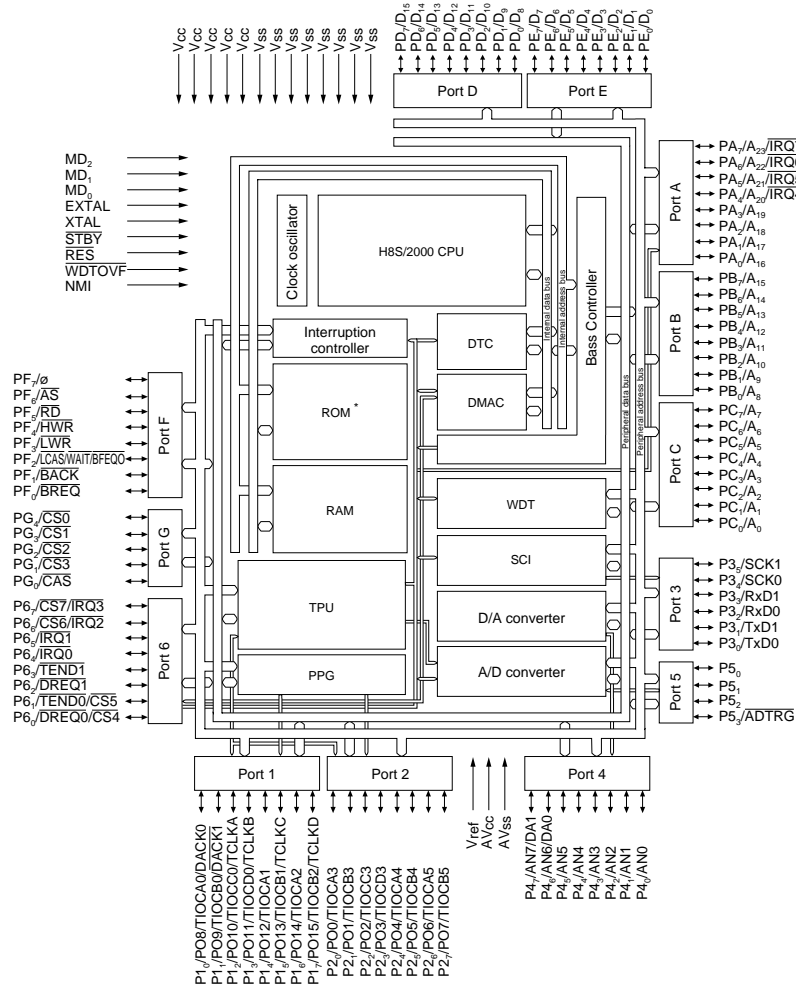
Symbol	Type	Name and function
DQ <sub>15</sub> /A <sub>-1</sub>	Input	Byte selection address: When the device is in the x8 mode, the low or high order byte is selected. It is not used in the x16 mode. (If BYTE# is high, DQ <sub>15</sub> /A <sub>-1</sub> input circuit does not operate.)
A <sub>0</sub> -A <sub>12</sub>	Input	Word selection address: Selection of one word of 16k byte block. These addresses are latched during data wiring operation.
A <sub>13</sub> -A <sub>17</sub>	Input	Block selection address: Selection of 1/32 erase block. These addresses are latched during data writing, erasing and lock block operation.
DQ <sub>0</sub> -DQ <sub>7</sub>	Input/Output	Low order byte data input/output: Command user interface writing cycle data and command input. Various data read memory identifier and status data output Chip nonselection or output disable: Float state
DQ <sub>8</sub> -DQ <sub>15</sub>	Input/Output	High order byte data input/output: The function is the same as that of low order byte data input/output. Operative only in x16 mode. x8 mode: Float state DQ <sub>15</sub> /A <sub>-1</sub> is address.
CE#	Input	Chip enable: Device control logic, input buffer, decoder and sense amp. are activated. Chip becomes active only when CE# is "Low".
RP#	Input	Reset/Power down: If RP# is set to "Low", the control circuit is initialized when power is turned on. Hence, the RP#pin is set to "Low". When power is turned on or off or in case of fluctuation it is kept at "Low" so as to protect data from noise. When RP# is in "Low" state, the device is in deep power down state. 480 ns is required to recover from the deep power down state. If the RP# pin becomes "Low", the whole chip operation is interrupted and reset. After recovery the device is set to array read state.
OE#	Input	Output enable: When OE# is set to "Low", data is output from the DQ pin. When OE# is set to "High", the DQ pin is set to float state.
WE#	Input	Write enable: Command user interface, data Q register and address Q latch access is controlled. In "Low" state WE# becomes active. At rise edge the address and data are fetched.
RY/BY#	Output	Ready/busy: The state of internal write state machine is output. In "Low" state it is indicated that the write state machine is in operation. If the write state machine waits for next operation instruction, erase is suspended or it is in deep power down state, the RY/BY# pin is in float state.
BYTE#	Input	Byte enable: When BYTE# is set to "Low", the device is set to the x8 mode. At this time the DQ <sub>8</sub> -DQ <sub>15</sub> pin becomes float state. Address A <sub>-1</sub> selects high order/low order byte. When BYTE# is "High", the device is set to the x16 mode. The A <sub>-1</sub> input circuit is disabled.
V <sub>pp</sub>		Write/erase power supply: 5.0 ± 0.5V is applied during writing/erasing.
V <sub>cc</sub>		Device power supply: 5.0 ± 0.5V
GND		Ground
NC		Nonconnection

• Block Diagram

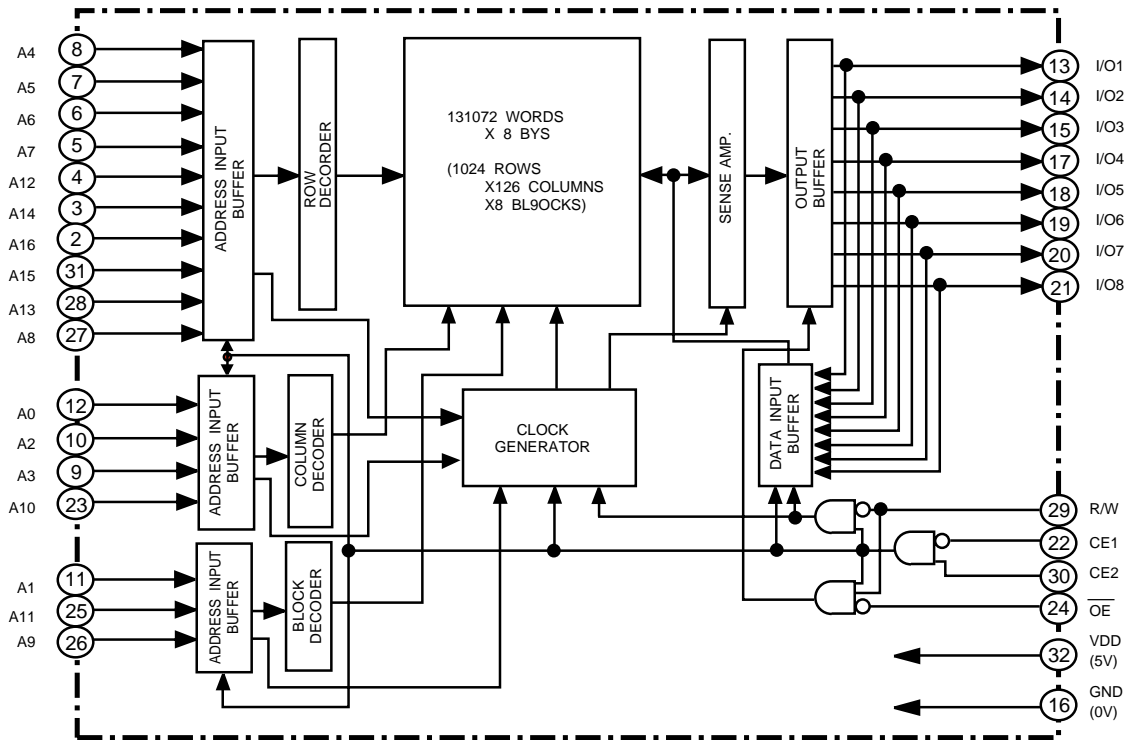




11-7. IC504 IX1478GE SYSCON



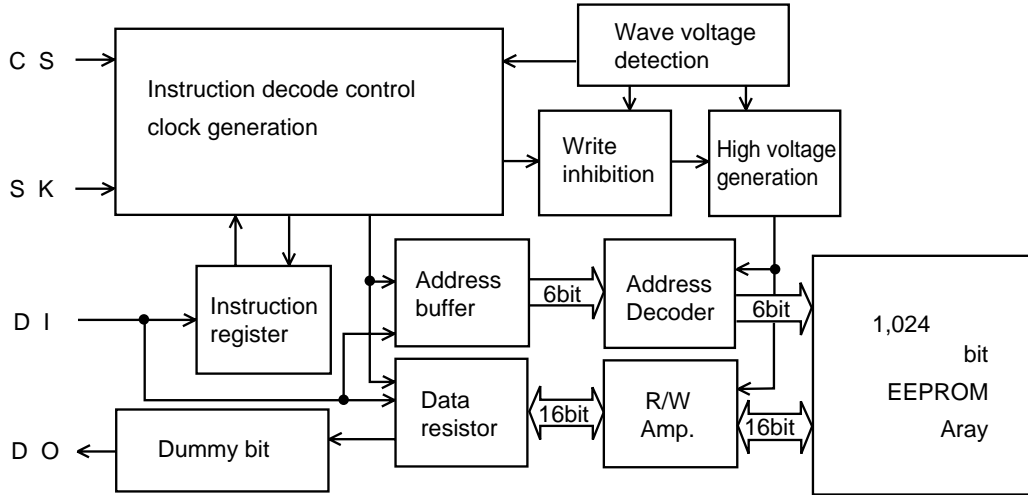
11-8. IC506 M51008BF 1M SRAM



### 11-9. IC507 BR93L46F EEPROM

Terminal	Terminal name	In/Output	Function
2	VCC	–	Power
7	GND	–	All input/output reference voltage, 0V
3	CS	Input	Tip select input
4	CLK	Input	Serial clock input
5	DIN	Input	Start bit, operation code, address and serial data input
6	OCNT	Output	Serial data output, READY/BUSY internal status indication output

• Block Diagram

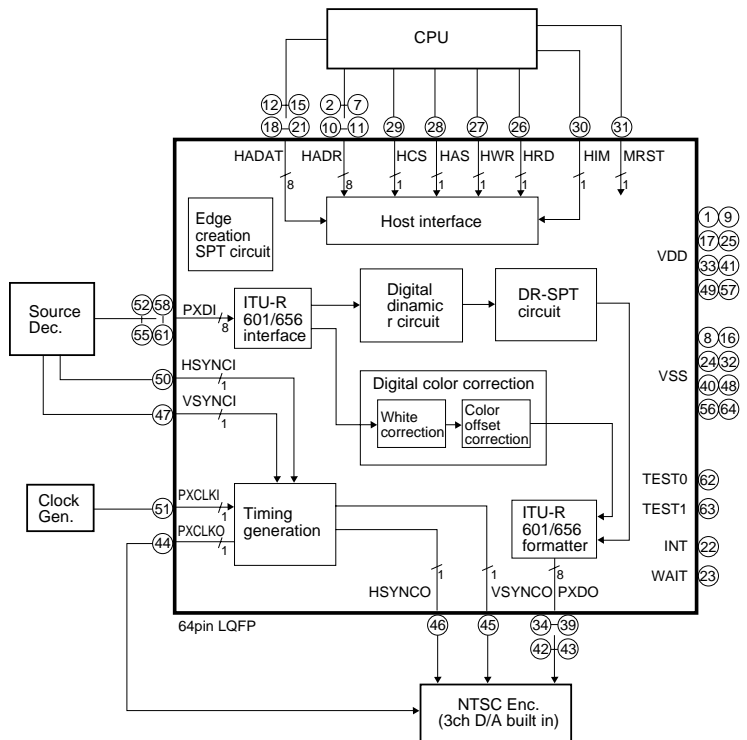


### 11-10. IC508 IX1516GE GAMMA S-P-TONE

Terminal	Terminal name	In/Output	Function
1	VDD	–	Digital power +3.3V
2	HADR (0)	Input	CPU Address bus
3	HADR (1)	Input	CPU Address bus
4	HADR (2)	Input	CPU Address bus
5	HADR (3)	Input	CPU Address bus
6	HADR (4)	Input	CPU Address bus
7	HADR (5)	Input	CPU Address bus
8	VSS	–	Digital GND
9	VDD	–	Digital power +3.3V
10	HADR (6)	Input	CPU Address bus
11	HADR (7)	Input	CPU Address bus
12	HADAT (0)	Input	CPU Data bus
13	HADAT (1)	Input	CPU Data bus
14	HADAT (2)	Input	CPU Data bus
15	HADAT (3)	Input	CPU Data bus
16	VSS	–	Digital GND
17	VDD	–	Digital power +3.3V
18	HADAT (4)	Input	CPU Data bus
19	HADAT (5)	Input	CPU Data bus
20	HADAT (6)	Input	CPU Data bus
21	HADAT (7)	Input	CPU Data bus
22	INT	Input	CPU Data bus
23	WAIT	Input	CPU Data bus
24	VSS	–	Digital GND
25	VDD	–	Digital power +3.3V
26	HRD	Input	CPU read signal
27	HWR	Input	CPU write signal
28	HAS	Input	CPU address strobe signal
29	HCS	Input	CPU tip select signal
30	HIM	Input	CPU bus control selection signal (I/M mode = H/L)

Terminal	Terminal name	In/Output	Function
31	MRST	Input	Reset signal
32	VSS	-	Digital GND
33	VDD	-	Digital power +3.3V
34	PXDO (0)	Output	Pixel data output 8-bit parallel video data conforming to ITU-R BT.601 and BT.656 standard (Cb/Y/Cr/Y) MSB=PXDO(7), LSB=PXDO(0)
35	PXDO (1)	Output	
36	PXDO (2)	Output	
37	PXDO (3)	Output	
38	PXDO (4)	Output	
39	PXDO (5)	Output	
40	VSS	-	Digital GND
41	VDD	-	Digital power +3.3V
42	PXDO (6)	Output	
43	PXDO (7)	Output	
44	PXCLKO	Output	Reference clock output for pixel data. 27 MHz
45	VSYNCO	Output	Vertical sync signal output
46	HSYNCO	Output	Horizontal sync signal output
47	VSYNCI	Input	Vertical sync signal output
48	VSS	-	Digital GND
49	VDD	-	Digital power +3.3V
50	HSYNCI	Input	Horizontal sync signal output
51	PXCLKI	Input	Reference clock output for pixel data. 27 MHz
52	PXDI (0)	Input	Pixel data output 8-bit parallel video data conforming to ITU-R BT.601 and BT.656 standard (Cb/Y/Cr/Y) MSB=PXDI(7), LSB=PXDI(0)
53	PXDI (1)	Input	
54	PXDI (2)	Input	
55	PXDI (3)	Input	
56	VSS	-	Digital GND
57	VDD	-	Digital power +3.3V
58	PXDI (4)	Input	
59	PXDI (5)	Input	
60	PXDI (6)	Input	
61	PXDI (7)	Input	
62	TEST0	Input	Test terminal
63	TEST1	Input	Test terminal
64	VSS	-	Digital GND

• Block Diagram



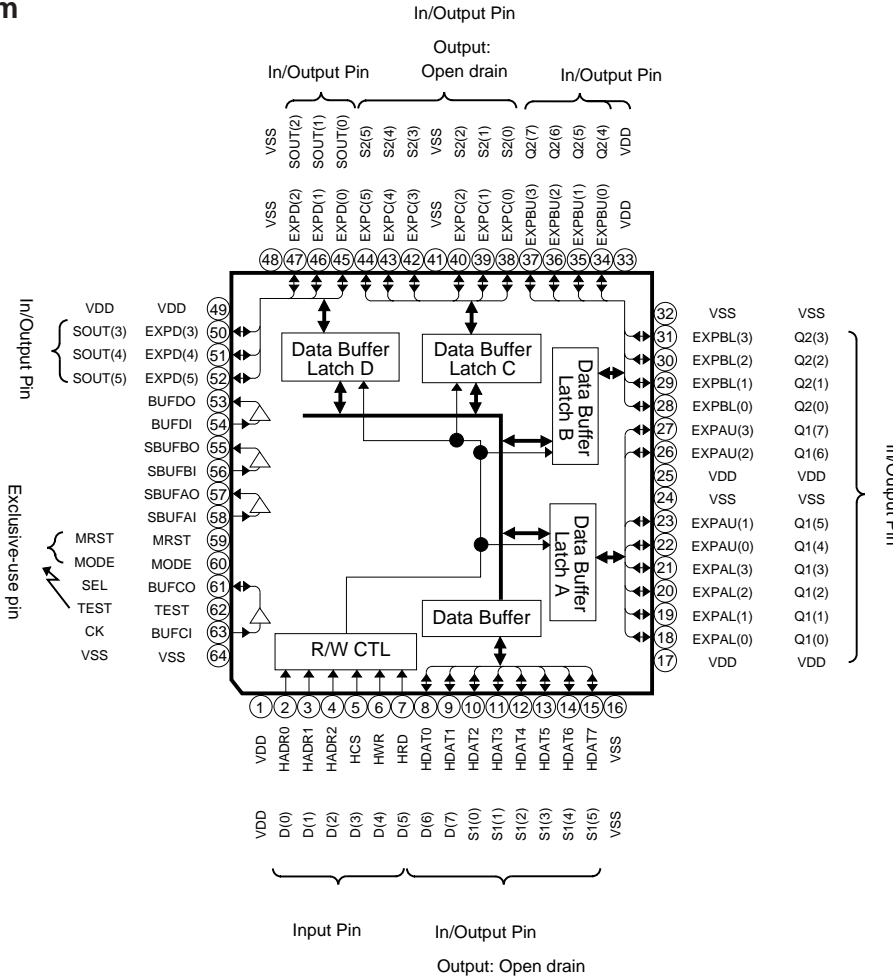
### 11-11. IC512 IX1535GE HOST I/F

Terminal	Terminal name	In/Output	Function
1	VDD	–	Power +3.3V
2	HADR0	Input	CPU Address bus
3	HADR1	Input	CPU Address bus
4	HADR2	Input	CPU Address bus
5	HCS	Input	CPU Tip select
6	HWR	Input	CPU Write signal
7	HRD	Input	CPU Read signal
8	HDATA0	In/Output	CPU Data bus
9	HDATA1	In/Output	CPU Data bus
10	HDATA2	In/Output	CPU Data bus
11	HDATA3	In/Output	CPU Data bus
12	HDATA4	In/Output	CPU Data bus
13	HDATA5	In/Output	CPU Data bus
14	HDATA6	In/Output	CPU Data bus
15	HDATA7	In/Output	CPU Data bus
16	VSS	–	Digital GND
17	VDD	–	Power +3.3V
18	EXPAL (0)	In/Output	General-use input/output terminal Gr.A
19	EXPAL (1)	In/Output	General-use input/output terminal Gr.A
20	EXPAL (2)	In/Output	General-use input/output terminal Gr.A
21	EXPAL (3)	In/Output	General-use input/output terminal Gr.A
22	EXPAU (0)	In/Output	General-use input/output terminal Gr.A
23	EXPAU (1)	In/Output	General-use input/output terminal Gr.A
24	VSS	–	Digital GND
25	VDD	–	Power +3.3V
26	EXPAU (2)	In/Output	General-use input/output terminal Gr.A
27	EXPAU (3)	In/Output	General-use input/output terminal Gr.A
28	EXPBL (0)	In/Output	General-use input/output terminal Gr.B
29	EXPBL (1)	In/Output	General-use input/output terminal Gr.B
30	EXPBL (2)	In/Output	General-use input/output terminal Gr.B
31	EXPBL (3)	In/Output	General-use input/output terminal Gr.B
32	VSS	–	Digital GND
33	VDD	–	Power +3.3V
34	EXPBU (0)	In/Output	General-use input/output terminal Gr.B
35	EXPBU (1)	In/Output	General-use input/output terminal Gr.B
36	EXPBU (2)	In/Output	General-use input/output terminal Gr.B
37	EXPBU (3)	In/Output	General-use input/output terminal Gr.B
38	EXPC (0)	In/Output	General-use input/output terminal Gr.C
39	EXPC (1)	In/Output	General-use input/output terminal Gr.C
40	EXPC (2)	In/Output	General-use input/output terminal Gr.C
41	VSS	–	Digital GND
42	EXPC (3)	In/Output	General-use input/output terminal Gr.C
43	EXPC (4)	In/Output	General-use input/output terminal Gr.C
44	EXPC (5)	In/Output	General-use input/output terminal Gr.C
45	EXPD (0)	In/Output	General-use input/output terminal Gr.D
46	EXPD (1)	In/Output	General-use input/output terminal Gr.D
47	EXPD (2)	In/Output	General-use input/output terminal Gr.D
48	VSS	–	Digital GND
49	VDD	–	Power +3.3V
50	EXPD (3)	In/Output	General-use input/output terminal Gr.D
51	EXPD (4)	In/Output	General-use input/output terminal Gr.D
52	EXPD (5)	In/Output	General-use input/output terminal Gr.D
53	BUFDO	Output	Buffer output D
54	BUFDI	Input	Buffer input D
55	SBUFBO	Output	Schmidt buffer output B
56	SBUFBI	Input	Schmidt buffer input B
57	SBUFAO	Output	Schmidt buffer output A
58	SBUFAI	Input	Schmidt buffer input A
59	MRST	Input	Reset terminal
60	MODE	Input	Mode selection terminal
61	BUFCO	In/Output	Buffer output C
62	TEST	Input	Test terminal (for Epson)
63	BUFCI	Input	Buffer input C
64	VSS	–	Digital GND

Pin1~15..... There is a possibility of simultaneous change.  
 Pin18~47 ..... There is a possibility of simultaneous change.(Static signal)  
 Pin50~57 ..... There is almost no possibility of simultaneous change.  
 Pin63 ..... Not used

Operating frequency: Approx. 10 MHz  
 Operating frequency: Approx. 1 MHz  
 Operating frequency: Approx. 1 MHz

• **Block Diagram**



**11-12. IC601 IX1521GE SOURCE DECODER**

Pin No.	Pin name	Type	Direction	Function	
Microcomputer interface					
22	HA[3:0]	I	I	Address bus input for microcomputer connection.	
24-26				Used for register access and so on	
27				HWR# (HR/W#)	HTYPE = L It works as HR/W#(read/write) input terminal for connection to Motorola type microcomputer. HTYPE = H It works as HWR# (write) input terminal for connection to general purpose microcomputer.
29				HCS#	Chip select input for connection to microcomputer
30	HRD# (HDS#)	I	I	HTYPE = L It works as HDS#(data strobe) input terminal for connection to Motorola type microcomputer. HTYPE = H It works as HRD# (read) input terminal for connection to general purpose microcomputer.	
31	HRDY	3-S	O	Bit stream input ready output terminal If the bit stream is input from microcomputer, the terminal is bored. For 3-state output, connect the pull-up resistor. HRDY = L Bit stream can not be input. HRDY = H The number of bytes which are set by CodBurstLen parameter can be transferred from the microcomputer. During the time from transfer start of the number of set bytes to transfer end, the terminal varies in 3 states.	

Microcomputer interface terminal list

Pin No.	Pin name	Type	Direction	Function
Microcomputer interface				
32	HACK# (HR/W#)			HTYPE = L It works as HACK# (acknowledge) output terminal for connection to Motorola type microcomputer. It can be used as the weight terminal for connection to the general purpose microcomputer. For 3-state output, connect the pull-up resistor.
34	HIRQ#	3-S	O	Interrupt request. If interrupt status register is read, interrupt is masked or device is reset, the signal is deasserted. For 3-state output, connect the pull-up resistor.
35	HWID	I	I	The bus width of the microcomputer interface If the device is worked as CD-G decoder or CD-DSP is connected, select the 8-bit bus mode. Fix it before power up. L=8bit bus mode H=16bit bus mode
36	HORD	I	I	When HWID is H (16-bit bus MODE), byte order is set. Setting is valid only when HWID is H. Fix it before power up. L=HD [15:8] is regarded as m.s. byte. (Motorola type) H=HD [7:0] is regarded as m.s. byte. (Intel type)
37	HTYPE	I	I	Bus type of microcomputer interface is set. Fix it before power up. L=Motorola type H=General purpose type
141	RESET#	I	I	RESET is input.
142	IDLE	3-S	O	It is output to indicate the idle state.

Microcomputer / CD-subcode interface terminal list

Pin No.	Pin name	Type	Direction	Function
Microcomputer interface / CD-subcode interface				
3	HD15 (CDERR)	3-S (I)	I/O (I)	When 16-bit bus width is selected, (HWID=low) It works as the microcomputer data bus of 15th bit. When 8-bit bus width is selected, (HWID=high) It works as the terminal to input bit clock from DC-DSP.
4	HD14 (CDFRM)	3-S (I)	I/O (I)	When 16-bit bus width is selected, (HWID=low) It works as the microcomputer data bus of 14th bit. When 8-bit bus width is selected, (HWID=high) It works as the terminal to input the stream/PCM data from CD-DSP.
5	HD13 (CDDAT)	3-S (I)	I/O (I)	When 16-bit bus width is selected, (HWID=low) It works as the microcomputer data bus of 13th bit. When 8-bit bus width is selected, (HWID=high) It works as the terminal to input frame synchronous signal from CD-DSP.
6	HD12 (CDCLK)	3-S (I)	I/O (I)	When 16-bit bus width is selected, (HWID=low) It works as the microcomputer data bus of 12th bit. When 8-bit bus width is selected, (HWID=high) It works as the terminal to input error signal to CD-DSP.
7	HD11 (SCCLK)	3-S (O)	I/O (O)	When 16-bit bus width is selected, (HWID=low) It works as the microcomputer data bus of 11th bit. When 8-bit bus width is selected, (HWID=high) It works as the terminal to output the subcode reading clock to the subcode interface of CD-DSP.
9	HD10 (SCDAT)	3-S (I)	I/O (I)	When 16-bit bus width is selected, (HWID=low) It works as the microcomputer data bus of 10th bit. When 8-bit bus width is selected, (HWID=high) It works as the terminal to input subcode data from subcode interface of CD-DSP.

General port terminal list

Pin No.	Pin name	Type	Direction	Function
General port				
2	GPSI	I	I	General purpose terminal.
122-123	GPAIO[1:0]	3-S	I/O	General input/output terminal. After resetting, it becomes the input direction.
159	GPSO	O	O	General output terminal.

Microcomputer / CD-subcode interface terminal list

Pin No.	Pin name	Type	Direction	Function
Microcomputer interface / CD-subcode interface				
10	HD9 (SCSYN)	3-S (I)	I/O (I)	When 16-bit bus width is selected, (HWID=low) It works as the microcomputer data bus of 9th bit. When 8-bit bus width is selected, (HWID=high) It works as the terminal to input the subcode synchronous signal from the subcode interface of CD-DSP.
11	HD8 (SCFRM)	3-S (I)	I/O (I)	When 16-bit bus width is selected, (HWID=low) It works as the microcomputer data bus of 9th bit. When 8-bit bus width is selected, (HWID=high) It works as the terminal to input the frame synchronous signal from the subcode interface of CD-DSP.
12 14-17 19-21	HD[7:0]	3-S	I/O	It works as the microcomputer bus of bits 7 thru 0.

PLL interface terminal list

Pin No.	Pin name	Type	Direction	Function
PLL interface				
126	GCLK1	I	I	Test terminal. Don't connect it.
128	XO	O	O	If quartz oscillator is connected to GCLK terminal, connect the other terminal of quartz oscillator to this pin.
129	GCLK	I	I	Master clock input terminal of device Input 27 MHz.
135, 137	PLLGFG[1:0]	I	I	PLL is set. Before power-up, fix it.
136	PLLCA	-	-	External capacitor terminal for PLL.

Video/OSD interface terminal list

Pin No.	Pin name	Type	Direction	Function
Video interface · OSD interface				
102	C7 (N.C.)	3-S (3-S)	O (O)	Video8 register = 0 Color difference signal output terminal of 7th bit. Video8 register = 1 The terminal becomes invalid.
104	C6 (N.C.)	3-S (3-S)	O (O)	Video8 register = 0 Color difference signal output terminal of 6th bit. Video8 register = 1 The terminal becomes invalid.
105	C5 (N.C.)	3-S (3-S)	O (O)	Video8 register = 0 Color difference signal output terminal of 5th bit. Video8 register = 1 The terminal becomes invalid.
106	C4 (OSDPLT)	3-S (3-S)	O (I)	Video8 register = 0 Color difference signal output terminal of 4th bit. Video8 register = 1 Input terminal to select pallet table of OSD. For OSDPLT=low, pallet table 0 is used. For OSDPLT=high, pallet table 1 is used.
107	C3 (OSDPEL3)	3-S (3-S)	O (I)	Video8 register = 0 Color difference signal output terminal of 3th bit. Video8 register = 1 It works as the OSD pallet data input terminal of 3rd bit.

Video/OSD interface terminal list

Pin No.	Pin name	Type	Direction	Function
Video interface · OSD interface				
109	C2 (OSDPEL2)	3-S (3-S)	O (I)	Video8 register = 0 Color difference signal output terminal of 2th bit. Video8 register = 1 It works as the OSD pallet data input terminal of 2rd bit.
110	C1 (OSDPEL1)	3-S (3-S)	O (I)	Video8 register = 0 Color difference signal output terminal of 1th bit. Video8 register = 1 It works as the OSD pallet data input terminal of 1rd bit.
111	C0 (OSDPEL0)	3-S (3-S)	O (I)	Video8 register = 0 Color difference signal output terminal of 0th bit. Video8 register = 1 It works as the OSD pallet data input terminal of 0rd bit.

Video interface terminal list

Pin No.	Pin name	Type	Direction	Function
Video interface				
84	VCLK	3-S	I/O	Clock gained by dividing VCLK x 2 signal into halves.
85	VMASTER	I	I	Input terminal to switch video master/slave. VMASTER=L Video master mode. Video synchronizing signal and video clock are internally generated. HTYPE=H Video slave mode. Video synchronizing signal and video clock are received from the external.
87	VDEN#	I	I	Video output enable input terminal VDEN#=H Y [7:0] and C [7:0] terminals are made to be disable (3-state). VDEN#=L Y [7:0] and C [7:0] terminals are made to be enable. Note: C [7:0] terminal is the multiplexed terminal as OSDPLT [3:0] and so on. For Video8 register = 0, VDEN# terminal is valid for Y [7:0] alone.
88	CBLANK	O	O	Composite blank output terminal. Horizontal/vertical blanking area and polarity are programmable.
89	VSYNC	3-S	I/O	Input/output terminal of vertically synchronous signal. Polarity and synchronous signal length are programmable.
90	HSYNC	3-S	I/O	Input/output terminal of horizontally synchronous signal. Polarity and synchronous signal length are programmable.
91	FI	3-S	I/O	Input/output terminal for identification of even/odd number field. Polarity is programmable.
92 94-97 99-101	Y[7:0]	3-S	O	Video8 register = 0 Brightness signal output/input terminal. Video8 register = 1 Brightness/color difference multiplex terminal as ITU-T656
124	VCLK X 2	3-S	I/O	Terminal to input video clock or output 27 MHz.

Audio interface terminal list

Pin No.	Pin name	Type	Direction	Function
Audio interface				
112	AIN	I	I	Audio (PCM) input terminal. Stereo x1
114-116	AOUT[2:0]	O	O	Audio (PCM) output terminal. Stereo x3
117	S/PDIF (AOUT[3])	O	O	S/PDIF output terminal AC-3 stream or PCM stream can be output. Moreover, it works as the audio output terminal of 7th and 8th channels
118	ALRCLK	O	O	Left/Right clock output terminal of AOUT [2:0] and AIN. The polarity is programmable.
119	ABCLK	O	O	Bit clock output terminal of AOUT [2:0] and AIN. The polarity is programmable.
132	AMCLK	3-S	I/O	Audio master clock input/output terminal. 256 Fs or 386 Fs can be used.



DVD-DSP interface terminal list

Pin No.	Pin name	Type	Direction	Function
DVD-DSP interface				
143	DVDERR	I	I	Data error input for DVD-DSP connection.
144	DVDSOS	I	I	Sector start input for DVD-DSP connection.
146	DVDVALID	I	I	Data valid input for DVD-DSP connection.
147	DVDSTRB	I	I	Data strobe input for DVD-DSP connection.
148	DVDREQ	O	O	Data request output for DVD-DSP connection.
149 151-154 156-158	DVDDAT[7:0]	I	I	Stream input for DVD-DSP connection

SD-RAM interface terminal list

Pin No.	Pin name	Type	Direction	Function
SDRAM interface				
38-39 42-47 49-52	RAMADD[11:0]	O	O	Address bus output for SDRAM connection.
54	RAMCS0#	O	O	Tip select output for SDRAM connection.
55	RAMCS1#	O	O	Tip select output terminal for SDRAM connection. It is connected to 2nd SDRAM.
56	RAMRAS#	O	O	RAS output terminal for SDRAM connection.
57	PCLK	O	O	Clock output terminal for SDRAM connection.
59	RAMCAS#	O	O	CAS output terminal for SDRAM connection.
60	RAMWE#	O	O	Write enable output terminal for SDRAM.
61	RAMDQM	O	O	Data masking output terminal for SDRAM.
62 64-67 69-72 74-79 82	RAMDAT[15:0]	3-S	I/O	Bi-directional data bus for SDRAM.

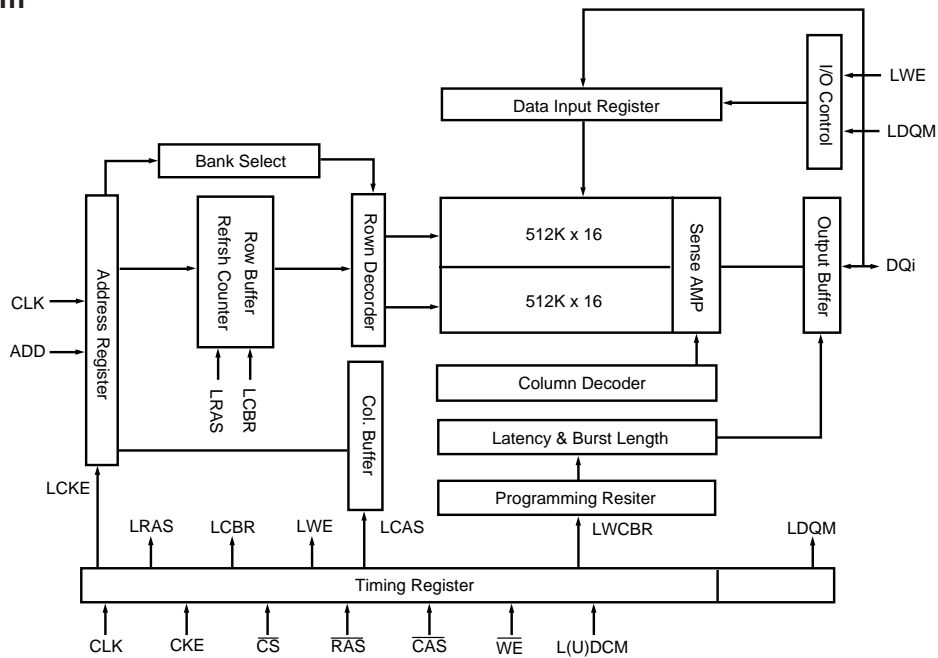
Power terminal · other list

Pin No.	Pin name	Type	Direction	Function
Power terminal · other				
1, 13, 23 40, 41 53, 68 80, 81 93, 108 120, 121 125, 131 145, 160	GND			Ground terminal
8, 18, 28 33, 48 58, 63 73, 86 98, 103 113, 133 140, 150, 155	VDD			+ 3.3V power input terminal
83	TESTMODE	I	I	Test terminal. Pull it down to GND.
127	SCNENBL	I	I	Test terminal. Pull it up to VDD.
130	PWRDN#	I	I	Power-down terminal. When it is [low], current consumption becomes minimum with all functions of the device stopped. (Power-down mode) To return it to normal state, set the terminal at [high]. Then, reset the device with RESET# terminal.
134	PLLGNDD			Ground terminal for internal PLL.
138	PLLVD			Internal PLL + 3.3V power input terminal.
139	ICEMODE	I	I	Test terminal. Pull it down to GND.

**11-13. IC602 IX1537GE 16M SDARM**

Terminal	Terminal Name	Name	Input Function
35	CLK	System Clock	Active on the positive going edge to sample all inputs.
18	CS	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK. CKE and L(U)DQM
34	CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in stanby.
21~24 27~32 20	A0~A10/AP	Address	Row/column address are multiplexed on the same pins. Row address: RA0~RA10, column address: CA0~CA7
19	BA	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read/write during clumn address latch time.
17	RAS	Row Address Strobe	Latches row address on the positive going edge of the CLK with RAS low. Enables row access & precharge.
16	CAS	Column Address Strobe	Latches addresses on the positive going edge of the CLK with CAS low. Enables row access.
15	WE	Write Enable	Enable write operation and row precharge. Latches data in starting from CAS, WE active.
14, 36	L(U)DOM	Data Input/Output Mask	Makes data output Hi-Z, tsHZ after the clock and masks the output. Blocks data input when L(U)DQM active.
2, 3, 5, 6, 8, 9, 11, 42, 43, 45, 46, 48, 49	DQ0~15	Data Input/Output	Data inputs/outputs are multiplexed on the same pins.
25, 1/26, 50	Vcc/Vss	Power Supply/Ground	Power and ground for the input buffers and the core logic.
44, 38, 13, 7/4, 10, 41, 47	Vcc/VssO	Data Output Power/Ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
37	NC/RFU	No Connection/ Reserved for Future Use	This pin is recommended to be left No Connection on the device

• **Block Diagram**



• Samsung Electronics reserves the right to change products or specification without

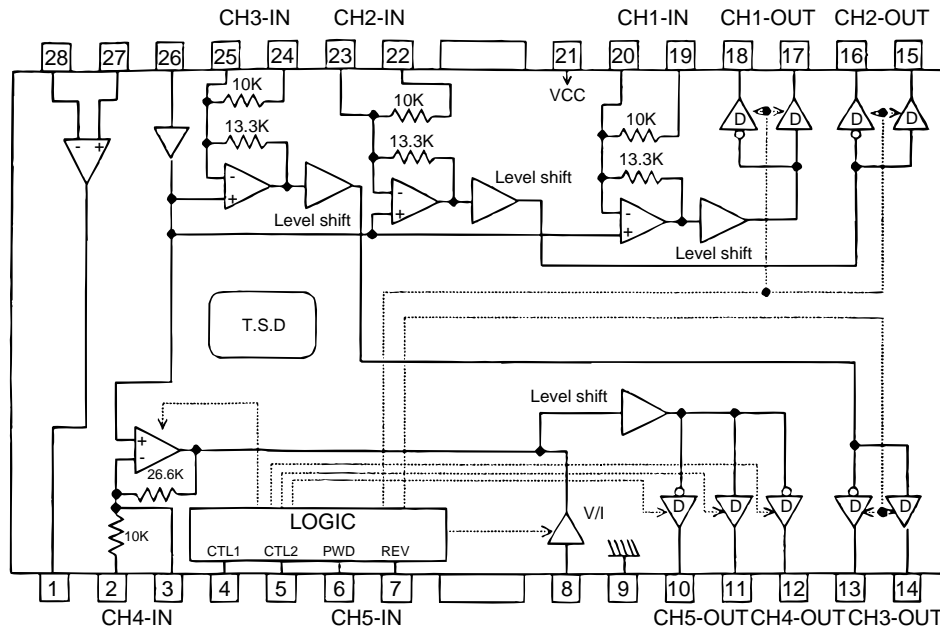
### 11-14. IC702 BA6796FP MOTOR DRIVER

Pin No.	Terminal name	Operation function	Pin No.	Terminal name	Operation function
1	OPOUT	Ope amp. output terminal	15	CH2-OUT-	CH2 Negative output terminal
2	CH4-IN	CH4 Input terminal	16	CH2-OUT+	CH2 Positive output terminal
3	CH4-IN'	CH4 Gain adjustment input terminal	17	CH1-OUT-	CH1 Negative output terminal
4	CTL1	Contorol 1 input terminal	18	CH1-OUT+	CH1 Positive output terminal
5	CTL2	Contorol 2 input terminal	19	CH1-IN	CH1 Input terminal
6	FWD	Tray forward input terminal	20	CH1-IN'	CH1 Input terminal for gain adjustment
7	REV	Tray reverse input terminal	21	VCC	VCC
8	TRAY-IN	Tray input terminal	22	CH2-IN	CH2 Input terminal
9	GND	Sub-straight GND	23	CH2-IN'	CH2 Input terminal for gain adjustment
10	CH5-OUT-	Tray negative output terminal	24	CH3-IN	CH3 Input terminal
11	COM-OUT	Tray positive output terminal/CH4 negative output terminal	25	CH3-IN'	CH3 Input terminal for gain adjustment
12	CH4-OUT+	CH4 Positive output terminal	26	VREF-IN	Bias amp. input terminal
13	CH3-OUT+	CH3 Positive output terminal	27	OPIN+	Operational amplifier nonreverse input terminal
14	CH3-OUT-	CH3 Negative output terminal	28	OPIN-	Operational amplifier reverse input terminal

**Note 1:** Positive and negative output have polarity with respect to input. (An example: 19 pin input 'H': 18 pin output 'H')

**Note 2:** Tray positive output and tray negative output have polarity with respect to mode. (An example: 11 pin output 'H' in FORWARD mode)

• **Block Diagram**



T.S.D ; Thermal shutdown  
D; Drive buffer  
Unit of resistance is [ $\Omega$ ].

• **Mode change table**

CTL1 and CTL2

CTL1	CTL2	CH1	CH2	CH3	CH4	CH5
L	L	OFF				ON
L	H	OFF				ON
H	L	OFF				OFF
H	H	OFF	ON	OFF	OFF	ON

**Note:** OFF state: Output has high impedance.

For F and R (CH5 control, valid only when CH5 is ON)

F	R	Output mode
L	L	High impedance
L	H	Reversing (reverse)
H	L	Forward rotation (forward)
H	H	Brake

11-15. IC707 IX1473GE

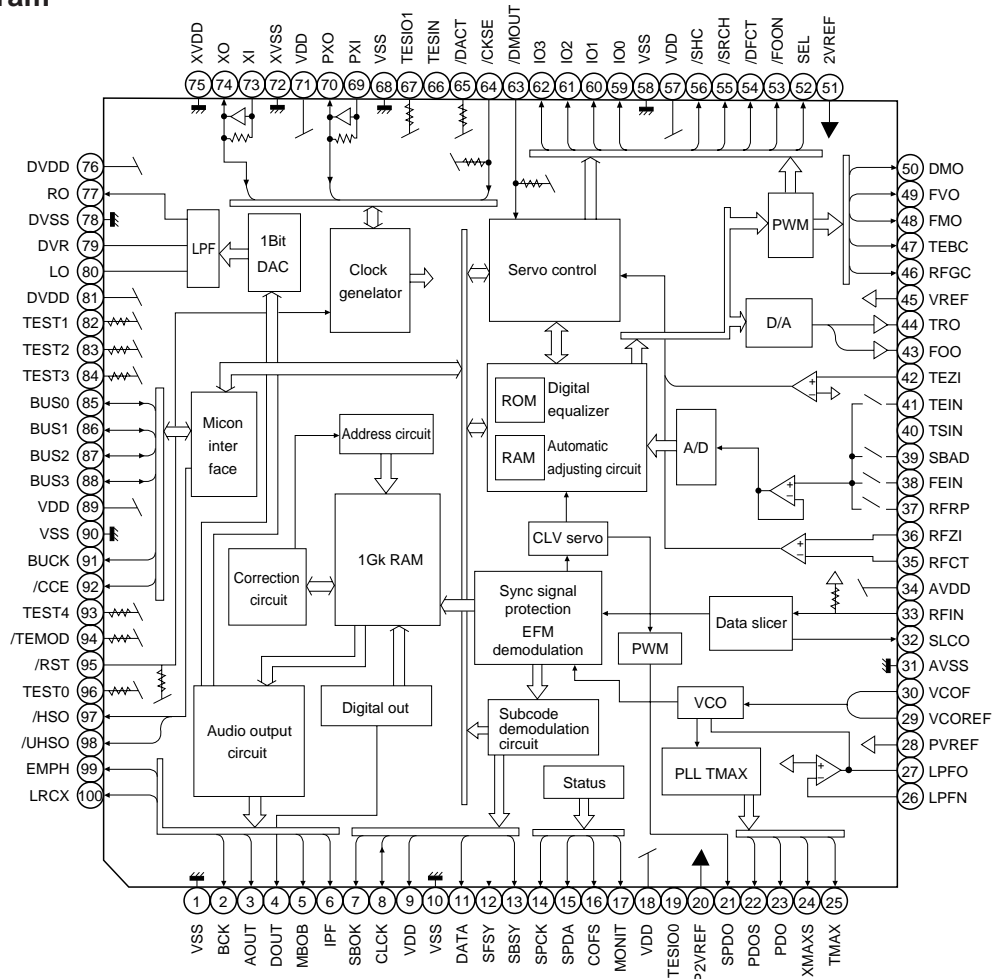
SERVO PROCESSOR

Pin No.	Terminal name	I/O	Operation function	Remarks								
1	VSS	–	Digital ground terminal.									
2	BCK	O	Bit clock (1.4122MHz) output terminal.									
3	AOUT	O	Audio data output terminal.									
4	DOUT	O	Digital out output terminal.									
5	MBOB	O	Buffer memory over signal output terminal. Over: "H"									
6	IPF	O	Correction flag output terminal. When correction disable symbol is given if AOUT output is C2 correction: "H".									
7	SBOK	O	Sub-code Q data CRCC judgment result output terminal. Judgment result OK: "H".									
8	CLCK	I/O	Sub-code P to W data read clock output/input terminal. Selectable with command bit.									
9	VDD	–	Digital + power terminal									
10	VSS	–	Digital ground terminal									
11	DATA	O	Sub code P-W data output terminal.									
12	SFSY	O	Playback system frame sync signal output terminal.									
13	SBSY	O	Subcode block sync output terminal. When subcode sync is detected, S1 position: "H".									
14	SPCK	O	Processor status signal read clock (176.4 kHz) output terminal.									
15	SPDA	O	Processor status signal output terminal.									
16	COFS	O	Correction system frame clock (7.35 kHz) output terminal.									
17	MONIT	O	LSI internal signal monitor terminal. DSP internal flag and PLL system clock can be monitored with microcomputer command.									
18	VDD	–	Digital + power terminal.									
19	TESIO0	I	Test input/output terminal. Usually fixed to "L".									
20	P2VREF	–	PLL system 2VREF terminal.									
21	SPDO	O	VCO center frequency shift terminal.									
22	PDOS	O	EFM and PLCK signal phase error signal output terminal. (To be used when x8 speed operation is used)									
23	PDO	O	EFM and PLCK signal phase error signal output terminal.									
24	XMAXS	O	TMAX detection result output terminal. To be selected with command bit TMPS.									
25	TMAX	O	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>TMAX detection result</th> <th>TMAXoutput</th> </tr> </thead> <tbody> <tr> <td>Longer than specific period</td> <td>"P2VREFF"</td> </tr> <tr> <td>Shorter than specific period</td> <td>"VSS"</td> </tr> <tr> <td>Within specified period</td> <td>"HiZ"</td> </tr> </tbody> </table>	TMAX detection result	TMAXoutput	Longer than specific period	"P2VREFF"	Shorter than specific period	"VSS"	Within specified period	"HiZ"	
TMAX detection result	TMAXoutput											
Longer than specific period	"P2VREFF"											
Shorter than specific period	"VSS"											
Within specified period	"HiZ"											
26	LPFN	I	Reverse input terminal for low pass filter amplifier.									
27	LPFO	O	Output terminal for low pass filter amplifier.									
28	PVREF	–	PLL system VREF terminal.									
29	VCOREF	I	VCO center frequency reference level terminal. To be fixed usually to "PVREF".									
30	VCOF	O	Filter terminal for VCO.									
31	AVSS	–	Analog system ground terminal.									
32	SLCO	O	Data slice level generation DAC output terminal.									
33	RFIN	I	RF signal input terminal.									
34	AVDD	–	Analog system power terminal.									
35	RFCT	I	RFRP signal center level input terminal.									
36	RFZI	I	RFRP zero cross input terminal.									
37	RFRP	I	RF ripple signal input terminal.									
38	FEIN	I	Focus error signal input terminal.									
39	SBAD	I	Sub-beam addition signal input terminal.									
40	TSIN	I	Test input terminal. To be fixed usually to "Vref"									
41	TEIN	I	Tracking error signal input terminal. (Fetching when tracking servo is ON)									
42	TEZI	I	Tracking error zero cross input terminal.									
43	FOO	O	Focus equalizer output terminal.									

Pin No.	Terminal name	I/O	Operation function	Remarks
44	TRO	O	Tracking equalizer output terminal.	
45	VREF	–	Analog reference power terminal.	
46	RFGC	O	RF amplitude adjustment control signal output terminal. Output of 3-pole PWM signal. (PWM carrier = 88.2 kHz)	
47	TEBC	O	Tracking balance control signal output terminal. Output of 3-pole PWM signal. (PWM carrier = 88.2 kHz)	
48	FMO	O	Feed equalizer output terminal. Output of 3-pole PWM signal. (PWM carrier = 88.2 kHz)	
49	FVO	O	Speed error signal or feed search EQ output terminal. Output of 3-pole PWM signal. (PWM carrier = 88.2 kHz)	
50	DMO	O	Disc equalizer output terminal. Output of 3-pole PWM signal. (PWM carrier = DSP system 88.2kHz, to be synchronized with PXO)	
51	2VREF	–		
52	SEL	O		
53	/FOON	O		
54	/DFCT	O		
55	/SRCH	O		
56	/SHC	O		
57	VDD	–		
58	VSS	–		
59	IO0	I/O	General use I/O port. It is possible to select the input port and output port according to command. In case of input port the terminal state (H/L) can be read with the read command. In case of output port the terminal state (H/L/HiZ) can be controlled with the command.	
60	IO1			
61	IO2			
62	IO3			
63	/DMOUT		Terminal to set the mode to output dual value PWM of feed equalizer from the IO0,1 terminal and to output the dual value PWM from disc equalizer of IO2,3 terminal "L" Active.	
64	/CKSE		X'tal selection terminal. When 16.9344 MHz: "H" When 33.8688 MHz: "L"	
65	/DACT		Test terminal.	
66	TESIN		Test input terminal.	
67	TESIO1		Test input/output terminal.	
68	VSS		Digital ground terminal.	
69	PXI		DSP system clock oscillation circuit input terminal.	
70	PXO		DSP system clock oscillation circuit output terminal.	
71	VDD		Digital + power terminal.	
72	XVSS		Ground terminal for system clock oscillation circuit.	
73	XI		System clock oscillation circuit input terminal.	
74	XO		System clock oscillation circuit output terminal.	
75	XVDD		Positive power terminal for system clock oscillation circuit.	
76	DVDD	–	D/A converting section power terminal.	
77	RO	O	R channel data forward rotation output terminal.	
78	DVSS	–	D/A converting section analog ground terminal.	
79	DVR	–	D/A converting section reference voltage terminal.	
80	LO	O	L channel data forward rotation output terminal.	
81	DVDD	–	D/A converting section power terminal.	
82	TEST1	I	Test terminal. To be opened usually.	Pull-up resistor built in.
83	TEST2	I	Test terminal. To be opened usually.	Pull-up resistor built in.
84	TEST3	I	Test terminal. To be opened usually.	Pull-up resistor built in.
85	BUS0	I/O	Microcomputer interface data input/output terminal.	Schmidt input CMOS port
86	BUS1	I/O		
87	BUS2	I/O		

Pin No.	Terminal name	I/O	Operation function	Remarks															
88	BUS3	I/O																	
89	VDD	-	Digital + power terminal.																
90	VSS	-	Digital ground terminal.																
91	BUCK	I	Microcomputer interface clock input terminal.	Schmidt input															
92	/CCE	I	Microcomputer interface chip enable signal input terminal. BUS0 to 3 is active in "L" state.	Schmidt input															
93	TEST4	I	Test terminal. To be opened usually.	Pull-up resistor built in.															
94	/TEMOD	I	Local test mode selection terminal.	Pull-up resistor built in.															
95	/RST	I	Reset signal input terminal. Reset state: "L"	Pull-up resistor built in.															
96	TEST0	I	Test terminal. To be opened usually.	Pull-up resistor built in.															
97	/HSO	O	Playback speed mode flag output terminal.																
98	/UHSO	O																	
			<table border="1"> <thead> <tr> <th>/UHSO</th> <th>/HSO</th> <th>Playback speed</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>x1 speed playback</td> </tr> <tr> <td>H</td> <td>L</td> <td>x2 speed playback</td> </tr> <tr> <td>L</td> <td>H</td> <td>x4 speed playback</td> </tr> <tr> <td>L</td> <td>L</td> <td>x8 speed playback</td> </tr> </tbody> </table>	/UHSO	/HSO	Playback speed	H	H	x1 speed playback	H	L	x2 speed playback	L	H	x4 speed playback	L	L	x8 speed playback	
/UHSO	/HSO	Playback speed																	
H	H	x1 speed playback																	
H	L	x2 speed playback																	
L	H	x4 speed playback																	
L	L	x8 speed playback																	
99	EMPH	O	Subcode Q data emphasis flag output terminal. Emphasis ON: "H" OFF: "L" Output polarity can be inverted by the command.																
100	LRCK	O	Channel clock (44.1 kHz) output terminal. L channel "L" R channel: "H" Output polarity can be inverted by the command.																

• Block Diagram

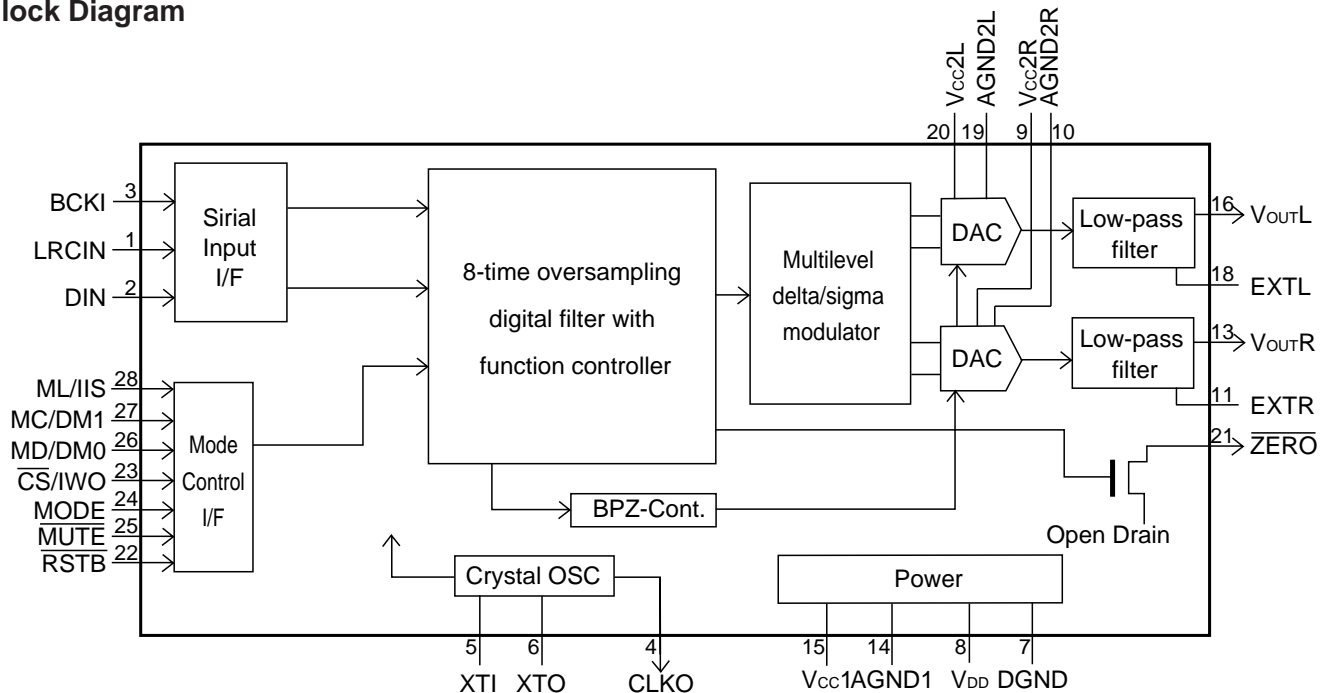


11-16. IC801 PCM1716E AUDIO D/A CONVERTER

Pin No.	Terminal name	I/O	Operation function
1	LRCIN	I	LRCK clock input (fs) <sup>(3)</sup>
2	DIN	I	Data input <sup>(3)</sup>
3	BCKI	I	Bit clock input for data.
4	CLKO	O	System clock buffered output.
5	XTI	I	Connection of crystal oscillator or external clock input.
6	XTO	O	Connection of crystal oscillator
7	DGND	-	Digital GND
8	V <sub>DD</sub>	-	Digital power +5V
9	V <sub>CC2R</sub>	-	Analog power +5V
10	AGND2R	-	Analog GND
11	EXTR	O	Rch Analog output amp. • common
12	NC	-	Not connected.
13	V <sub>OUTR</sub>	O	Rch Analog voltage output
14	AGND1	-	Analog GND
15	V <sub>CC1</sub>	-	Analog power +5V
16	V <sub>OUTL</sub>	O	Lch Analog voltage output
17	NC	-	Not connected.
18	EXTL	O	Lch Analog output amp. • common
19	AGND2L	-	Analog GND
20	V <sub>CC2L</sub>	-	Analog power +5V
21	ZERO	O	Zero data • flug
22	RSTB	I	Resetting. While this pin is in "L" state, the DF and delta -sigma modulator is in reset state. <sup>(1)</sup>
23	CS/IWO	I	Chip selection/input format selection <sup>(2)</sup>
24	MODE	I	Mode control selection (H: Software, L: Hardware) <sup>(1)</sup>
25	MUTE	I	Mute control <sup>(1)</sup>
26	MD/DM0	I	Mode control data/deemphasis selection 1 <sup>(1)</sup>
27	MC/DM1	I	Mode control BCK/deemphasis selection 2 <sup>(2)</sup>
28	ML/IIS	I	Mode control latch/input format selection <sup>(1)</sup>

**Note:** (1) Pins 22, 24, 25, 26, 27, and 28: With Schmidt trigger input pull-up resistor (2) Pin 23: With Schmidt trigger input pull-down resistor (3) Pins 1, 2, and 3: Schmidt trigger input

• Block Diagram

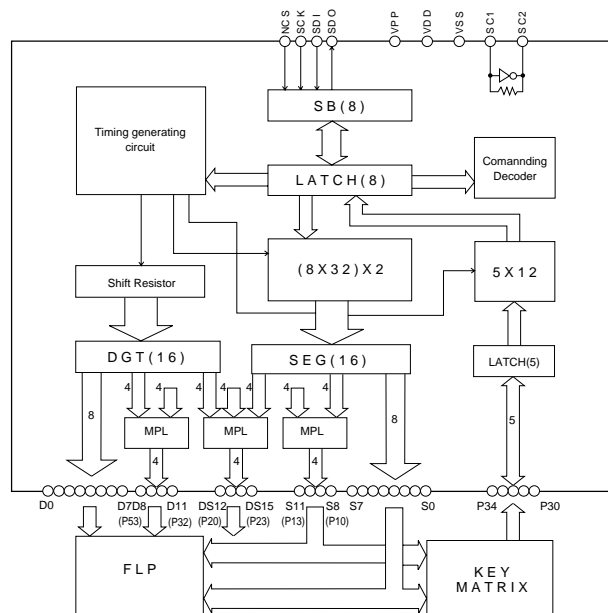


11-17. IC5001 IMN12510F

FL DRIVER

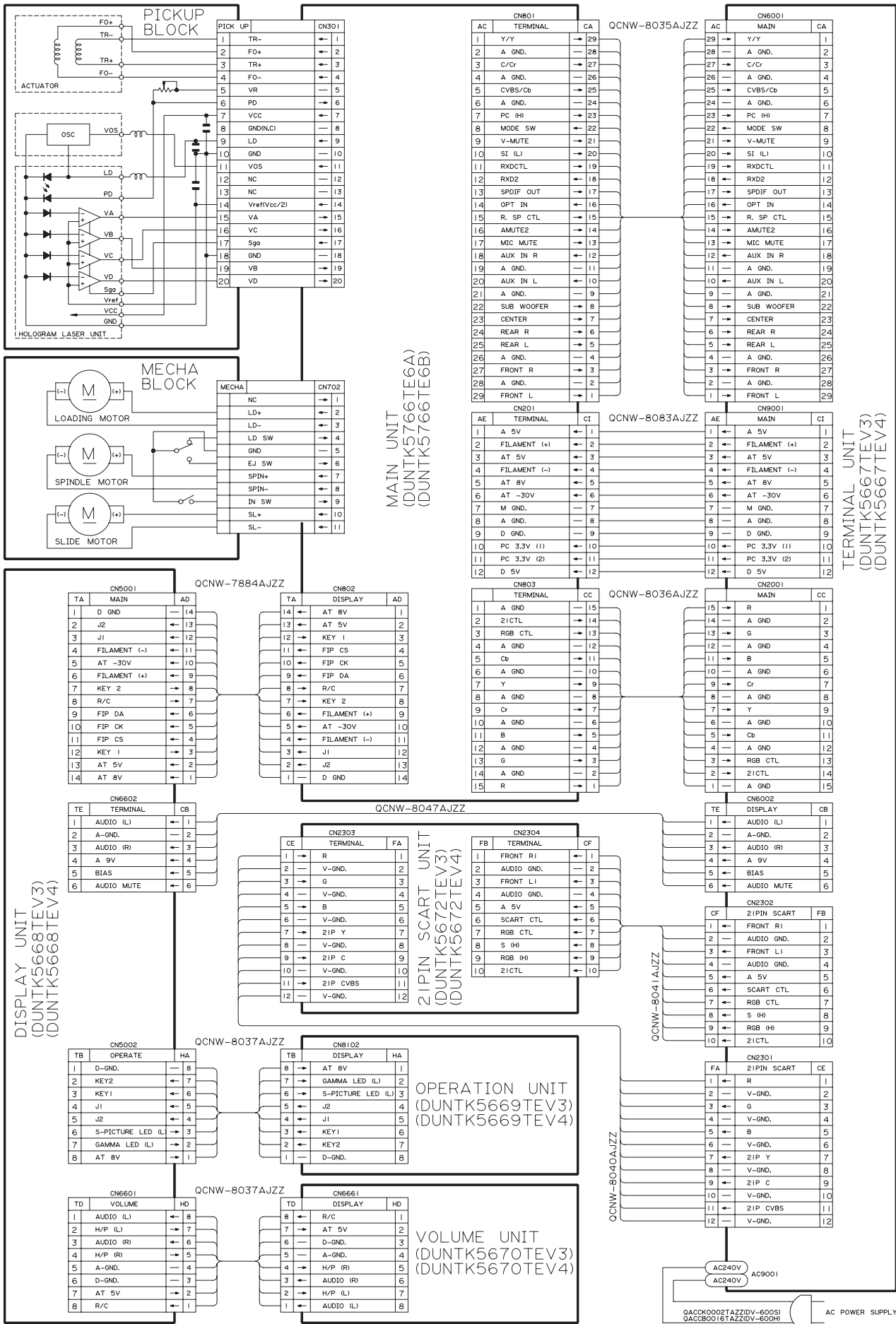
Terminal	Terminal Name	Name	In/Output	Function
18 21	VDD VSS	Power supply terminal	Input	VDD: +5V±0.5V VSS: 0V
16	VPP	FLP driver power	Input	VPP: VDD-35V The voltage to be supplied to the SEG 0 to 7, DGT 0 to 7 pull-down resistor is applied.
19 20	OSCI OSCO	Clock input Clock output	Input	Oscillation input terminal ) A terminal to which the ceramic Oscillation output terminal ) oscillation terminal is connected. To OSCI in case of clock input from outside in case of separate excitation
22 23 24	NCS SCK SDI	Chip select input Serial clock input Serial data input	Input Input Input	"L": Serial input allowed "H": Serial input inhibited Serial transfer clock input Serial data input The command data, address data, indication data, control register data, and port output data are input.
25	SDO	Serial data output	Output	Serial data output The key scan input data and port input data are output.
26~30	P30~P34	Key scan input	In/Output	There are 5 bits. Bitwise selection of key scan input/general-use input/general-use output is enabled. The pull-down resistor is provided between this terminal and the VSS terminal. The general-use output is large current output for LED drive.
31~38	SEG0~SEG7	High voltage resistance output	Output	8-bit high voltage resistance output port. (Segment output) The output type is Pch open drain. The pull-down resistor is built in between this terminal and the VPP terminal.
39~42	P10~P13 SEG8~SEG11	High voltage resistance output	Output	4-bit high voltage resistance output port. Bitwise selection of general-use output/segment output is enabled. The output type is Pch open drain.
43, 44 1, 2	P20~23 DGT12/SEG15 DGT15/SEG12	High voltage resistance output	In/Output	4-bit high voltage resistance output port. Bitwise selection of general-use input/general-use output/segment output/digit output is enabled. The output type is Pch open drain. Large current output for LED drive
3~6	P00~P03 DGT8~DGT11	High voltage resistance output	Output	4-bit high voltage resistance output port. Bitwise selection of general-use output/digit output is enabled. The output type is Pch open drain.
7~10 12~15	DGT0~DGT7	High voltage resistance output	Output	8-bit high voltage resistance output port. (Digit output) The output type is Pch open drain. The pull-down resistor is built in between this terminal and the VPP terminal.

• Block Diagram



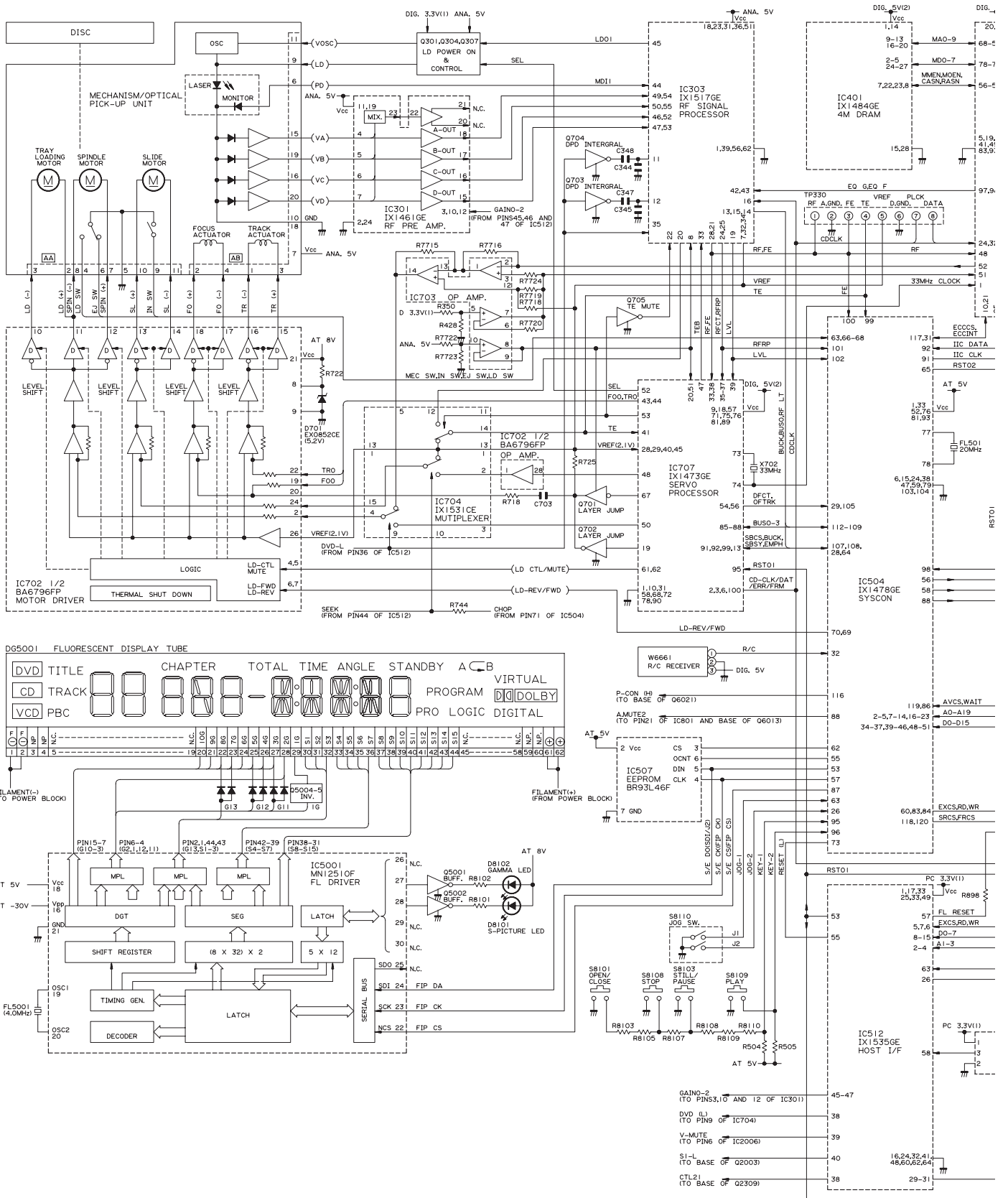


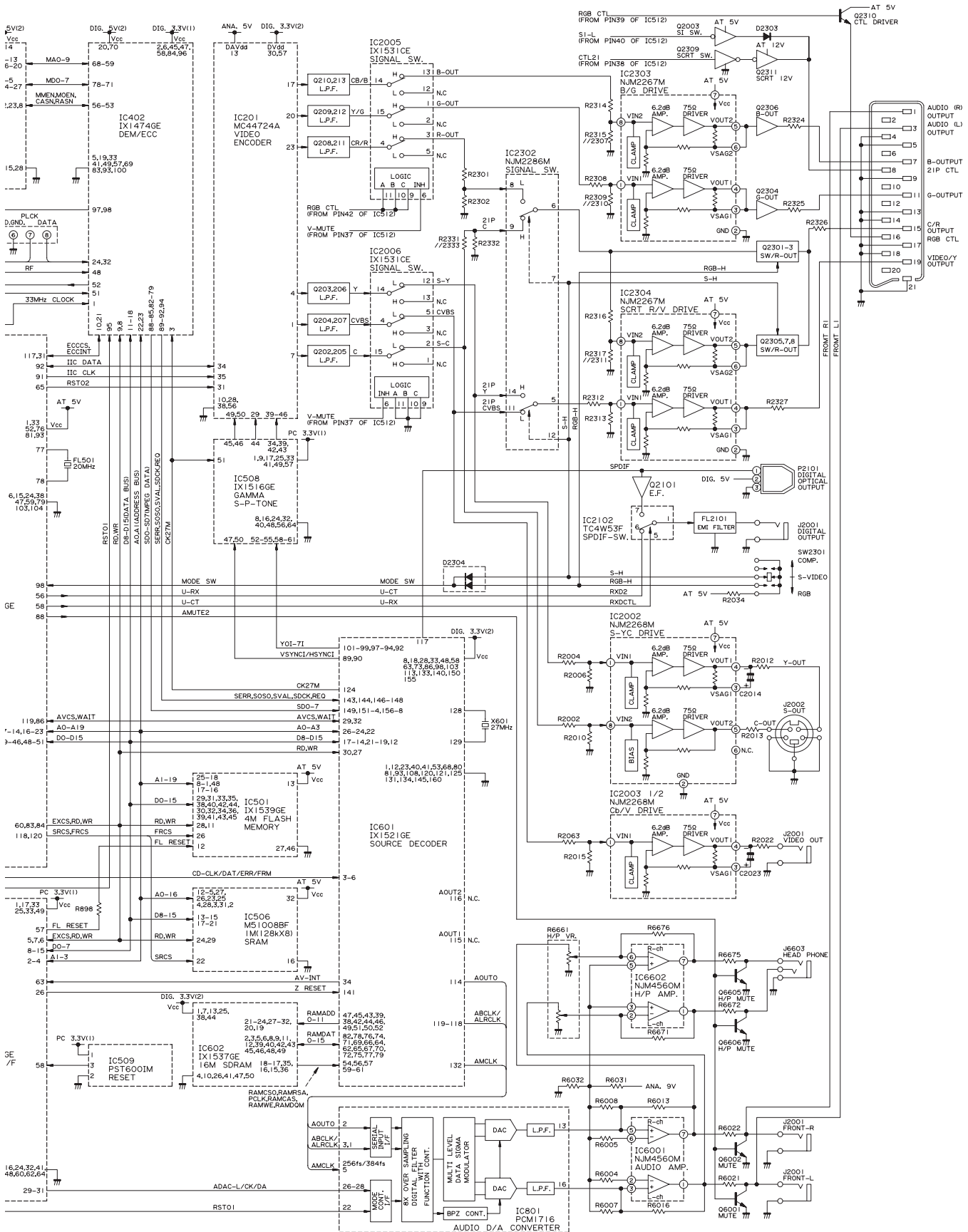
# 12. WIRING DIAGRAM



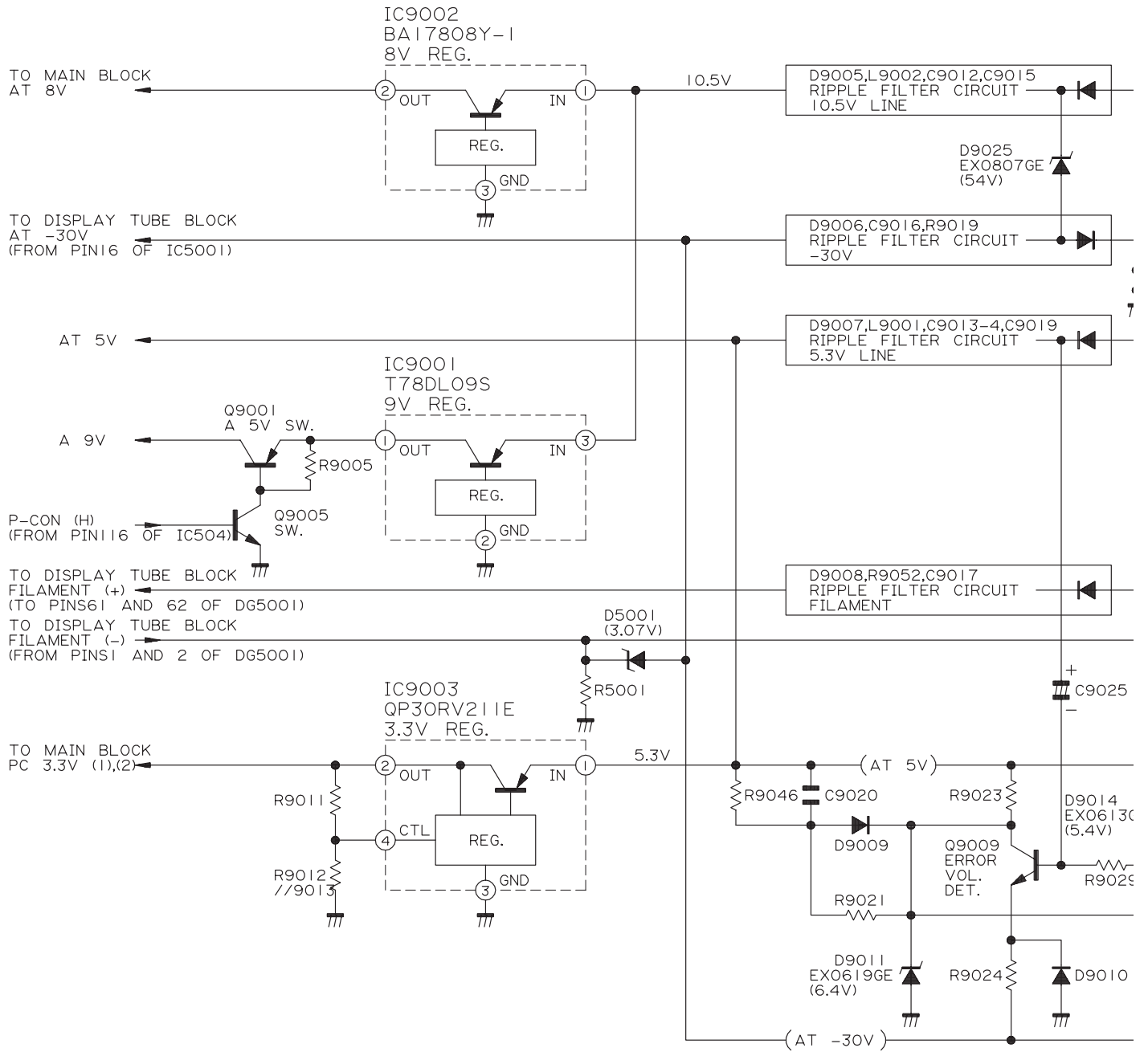
# 13. BLOCK DIAGRAMS

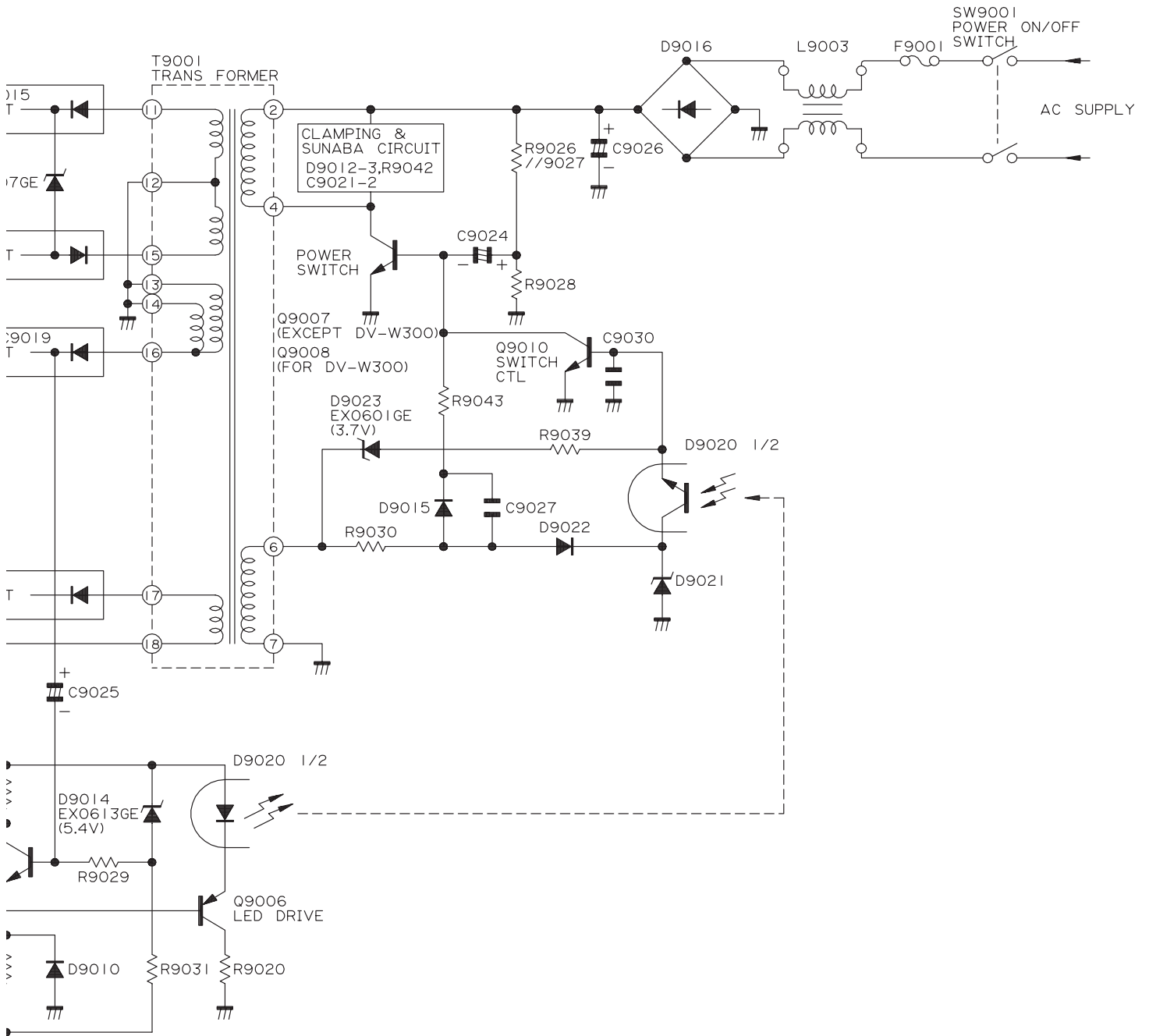
## 13-1. MAIN BLOCK DIAGRAM





### 13-2. POWER BLOCK DIAGRAM



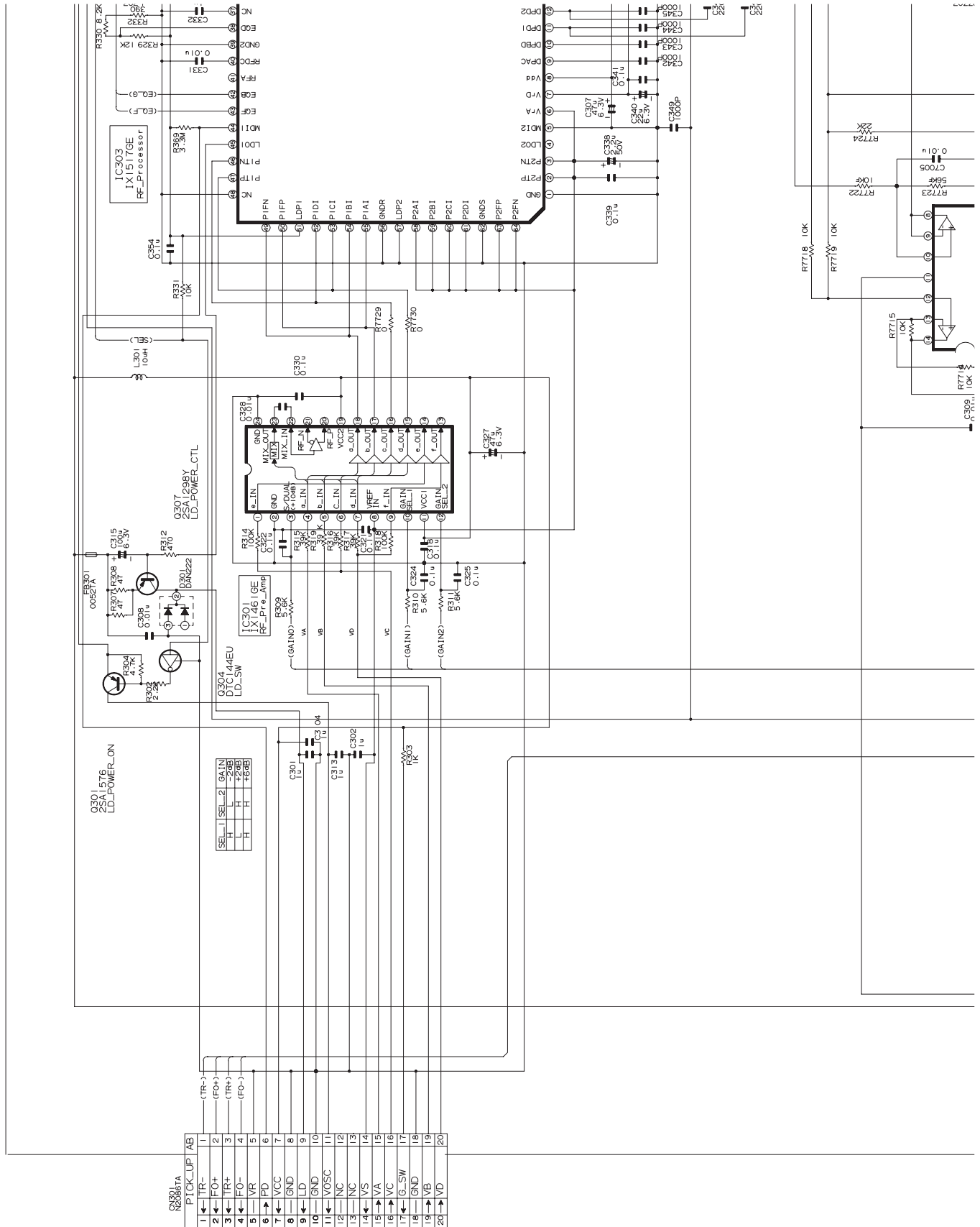


# 14. SCHEMATIC DIAGRAMS 14-1. MAIN (1) CIRCUIT SCHEMATIC DIAGRAM

LOCATION MAP: 

3
2 1 4

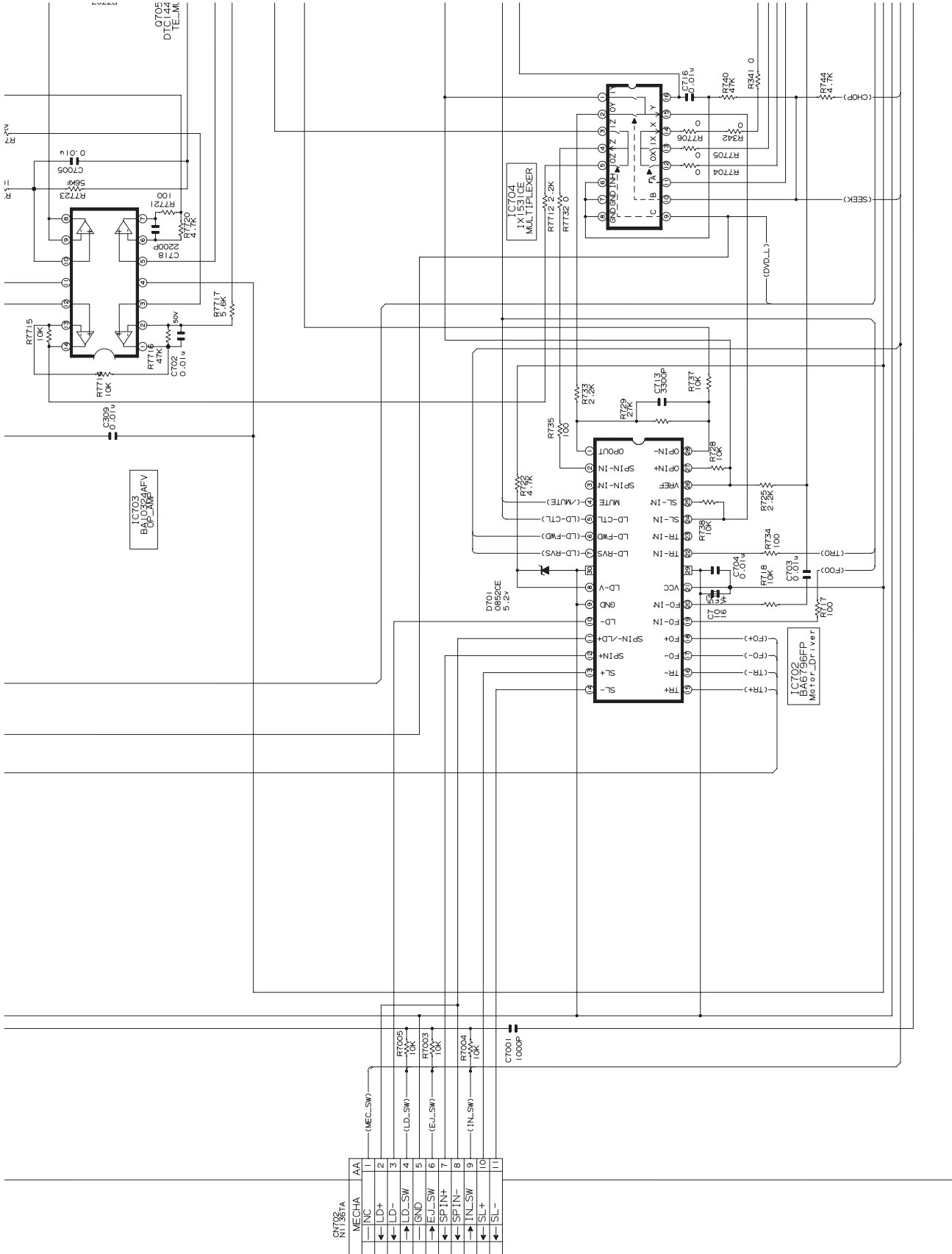
 (1/4)



LOCATION MAP: 

1	2	3	4
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 (2/4)

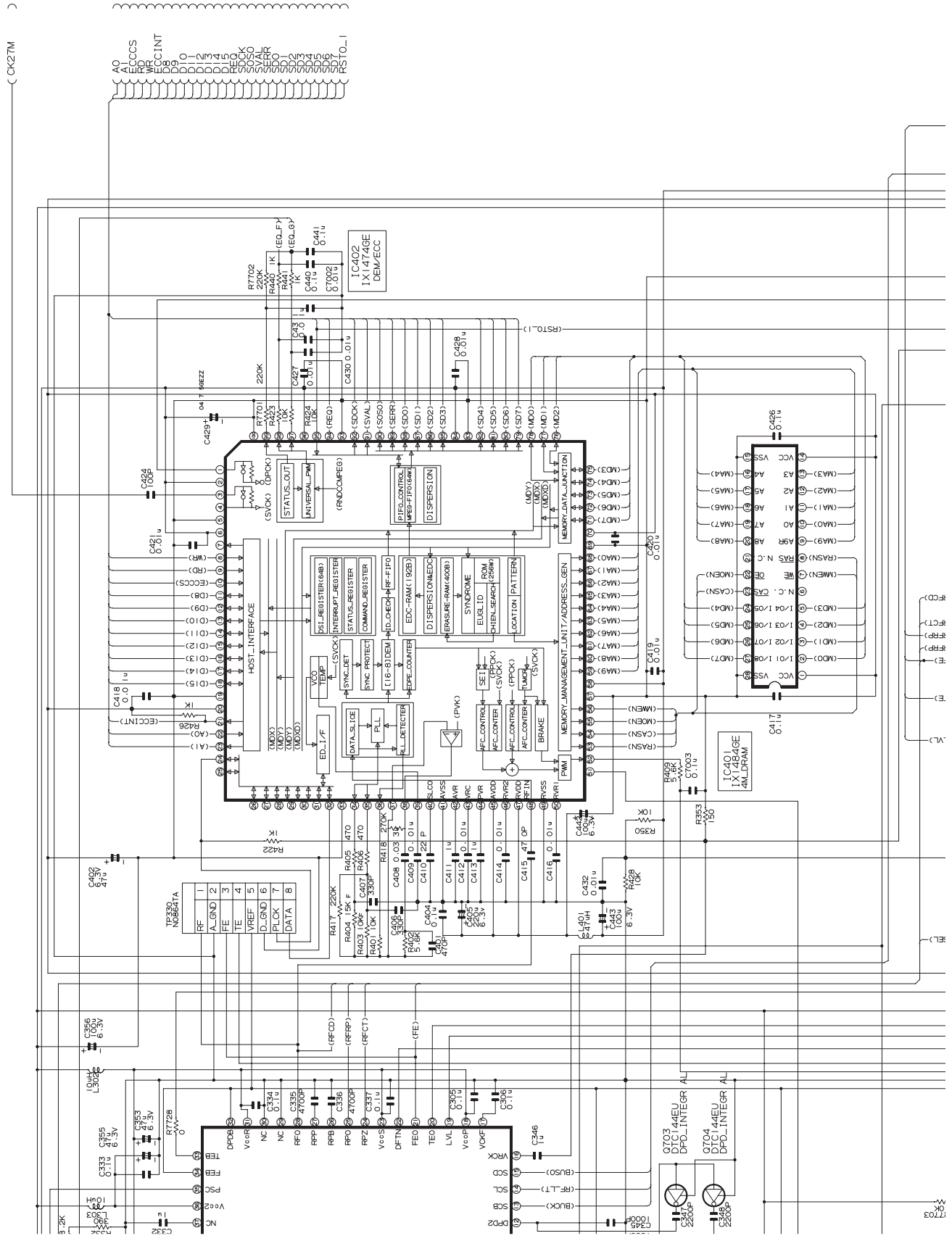


10	9	8	7	6	5	4	3	2	1
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LOCATION MAP: 

1	2	4
1	2	4

 (3/4)

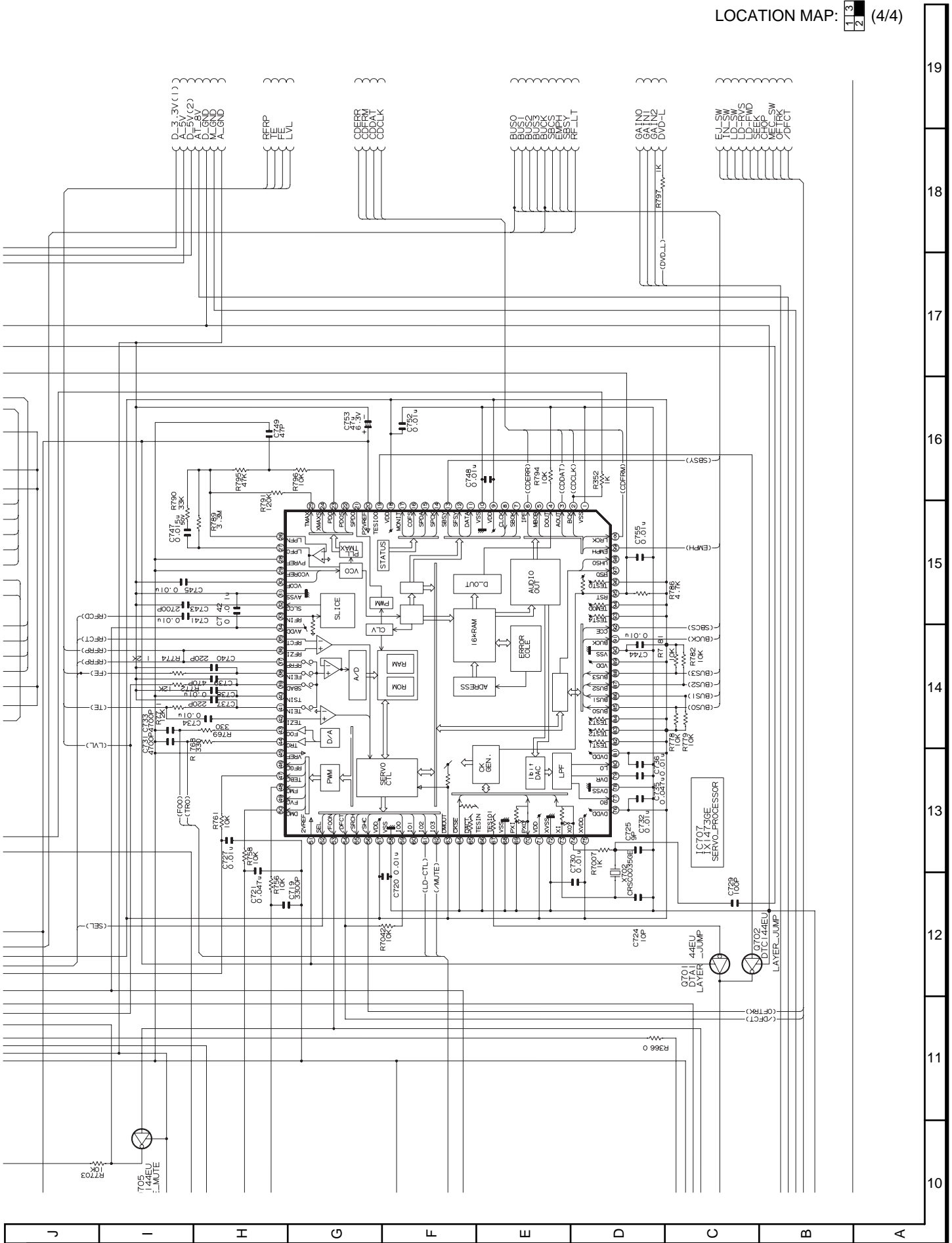




LOCATION MAP: 

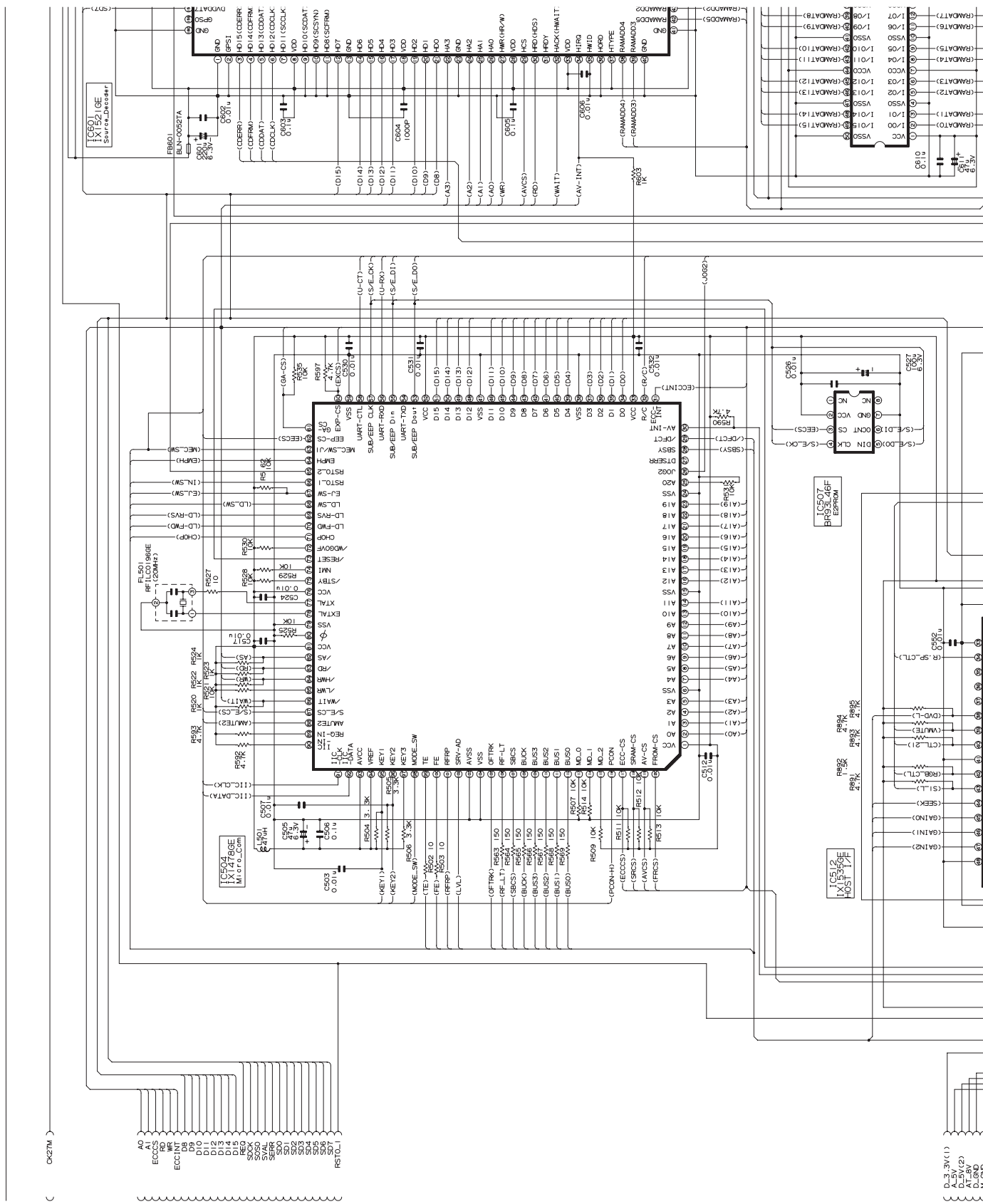
1	2	3
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 (4/4)



# 14-2. MAIN (2) CIRCUIT SCHEMATIC DIAGRAM

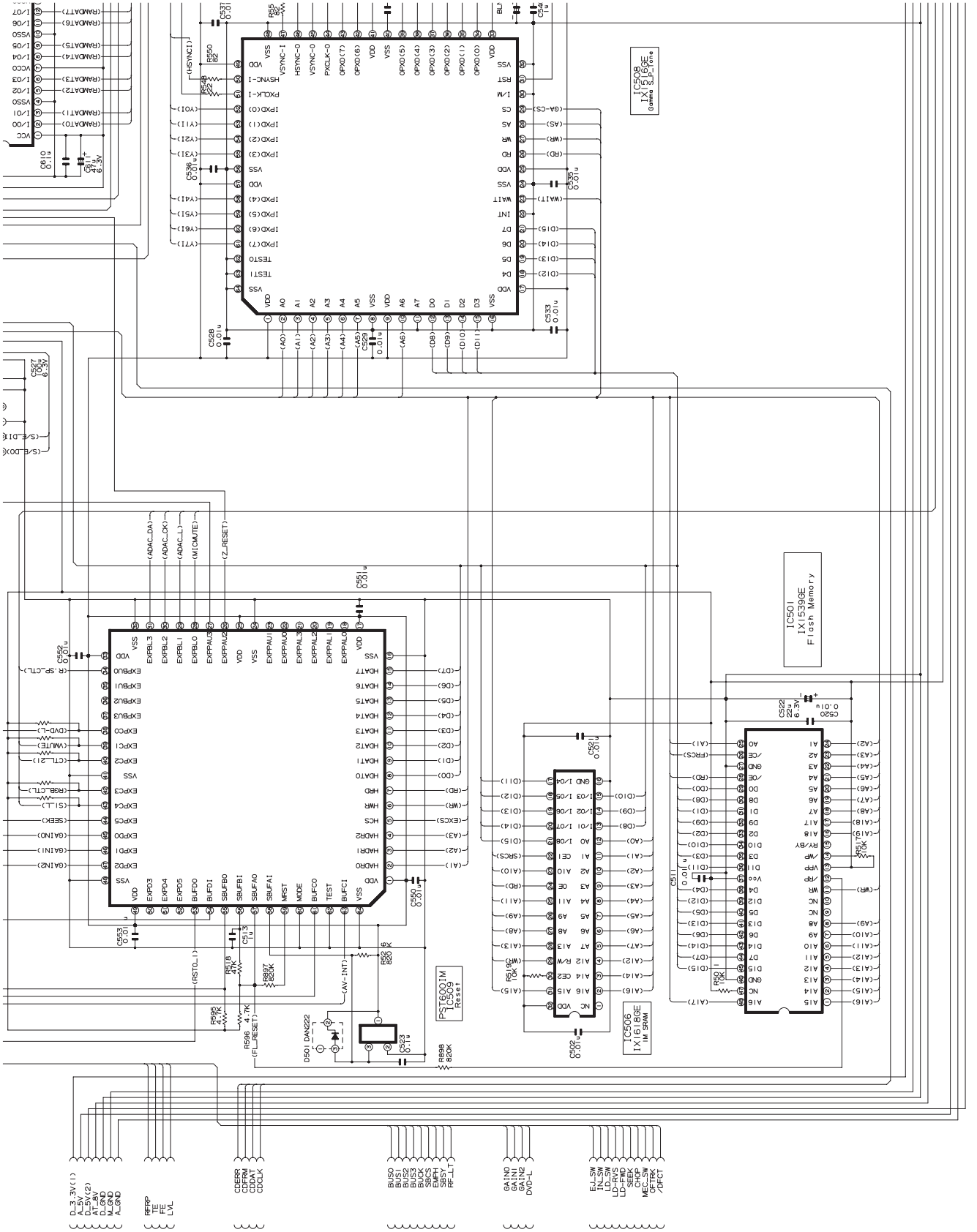
LOCATION MAP: 2 1 4 (1/4)



LOCATION MAP: 

1	2	3	4
---	---	---	---

 (2/4)

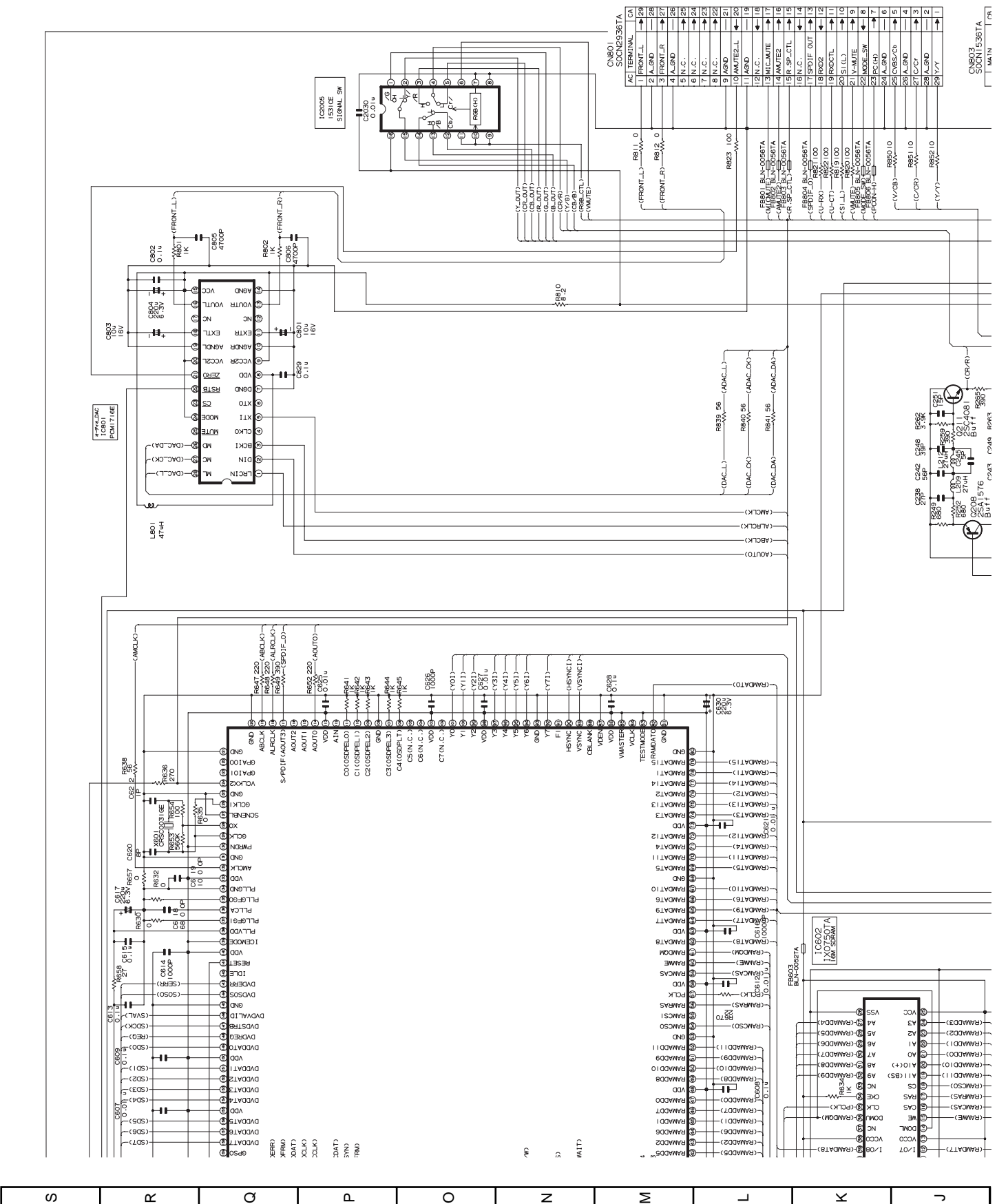


10	9	8	7	6	5	4	3	2	1
----	---	---	---	---	---	---	---	---	---

LOCATION MAP: 

1	2	3	4
---	---	---	---

 (3/4)

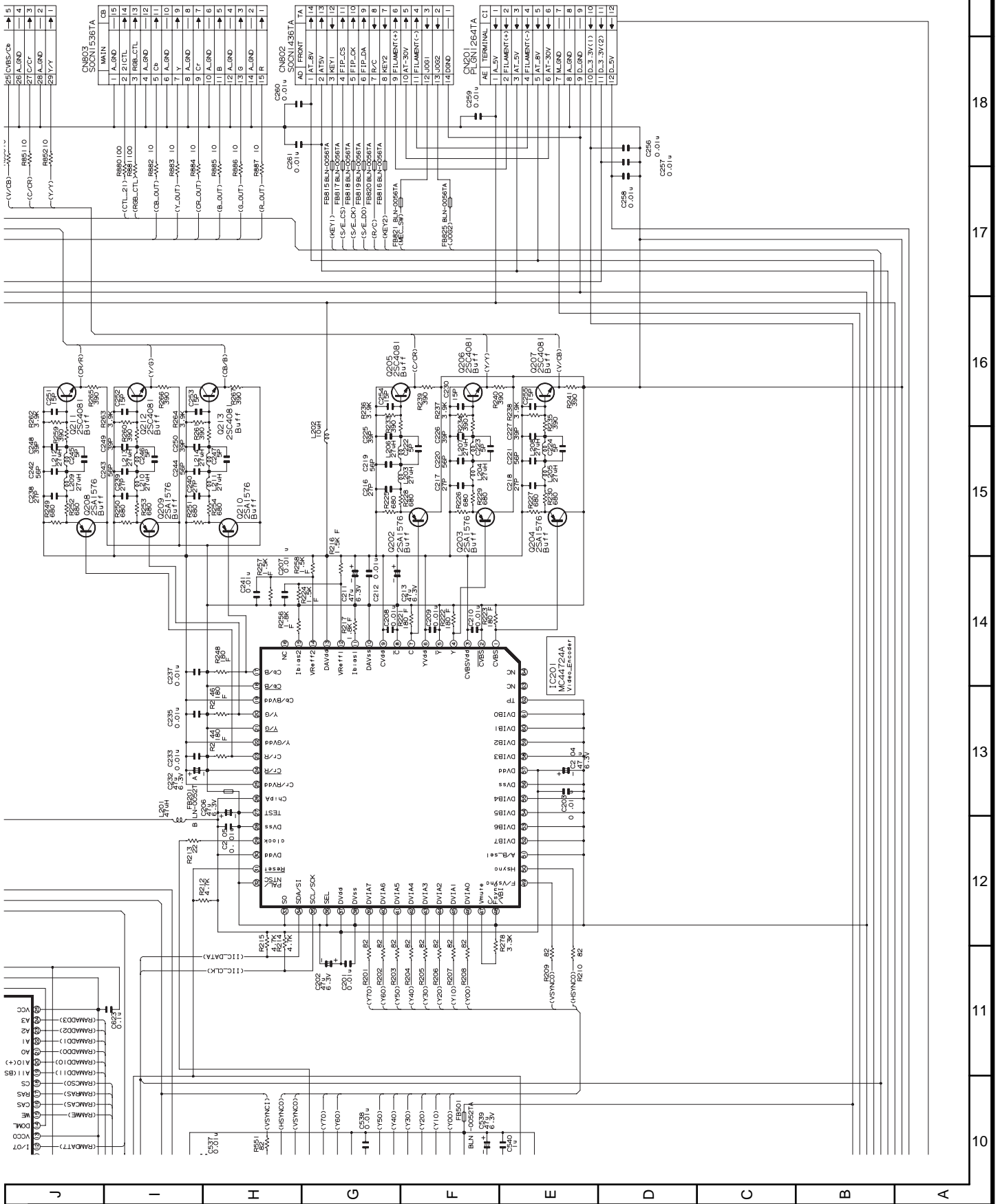


S	R	Q	P	O	N	M	L	K	J
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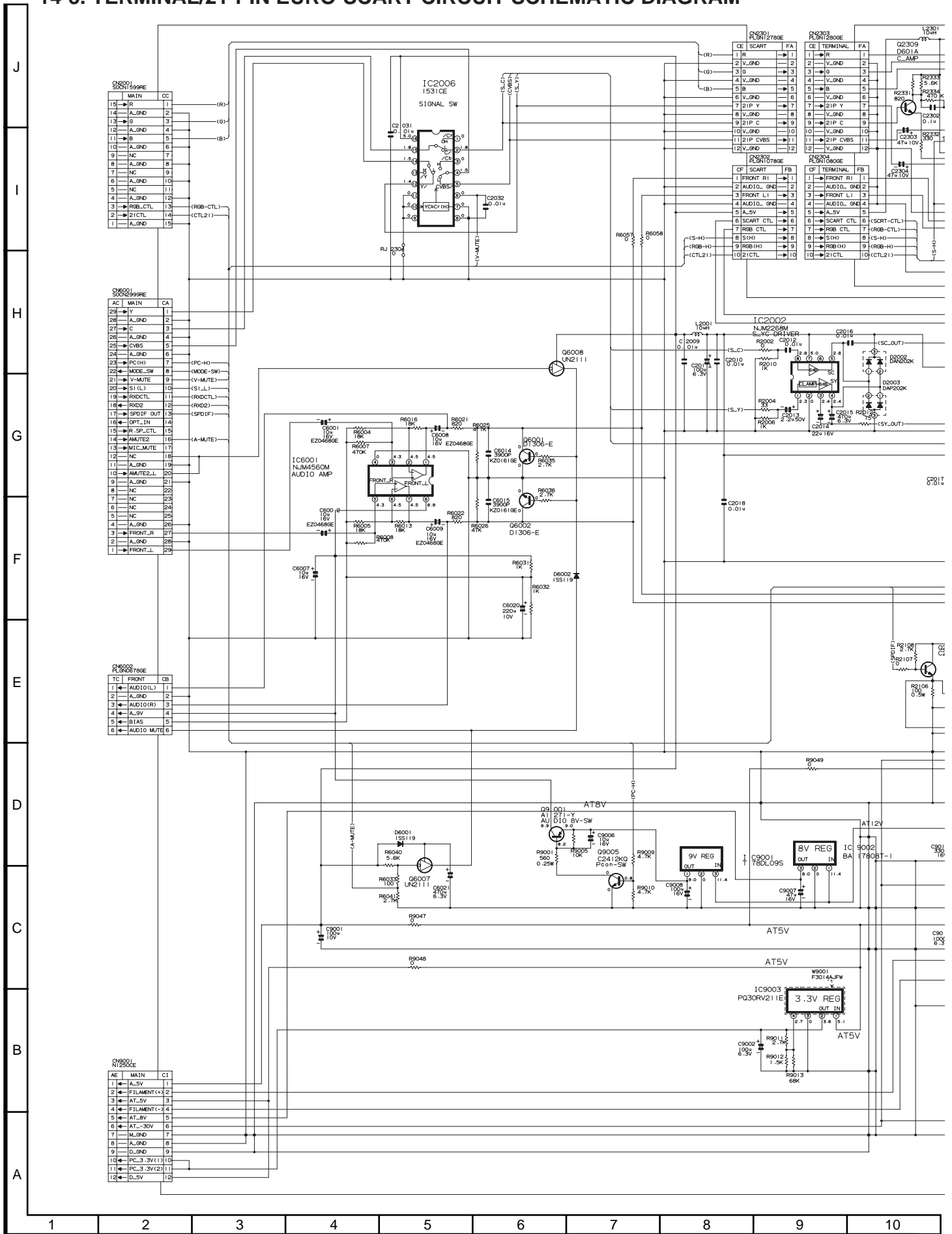
LOCATION MAP: 

1	3
2	

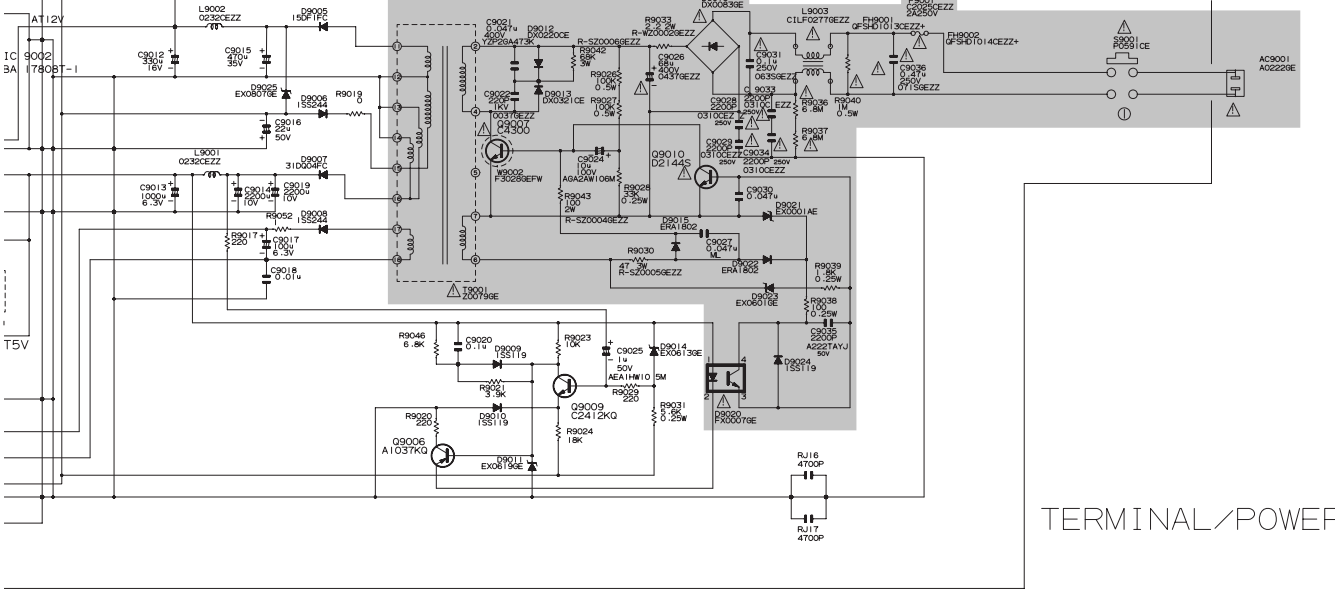
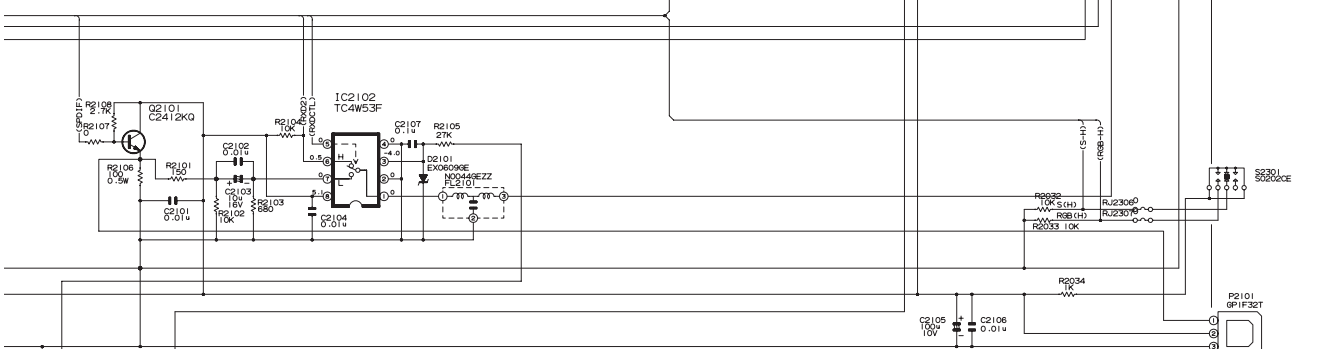
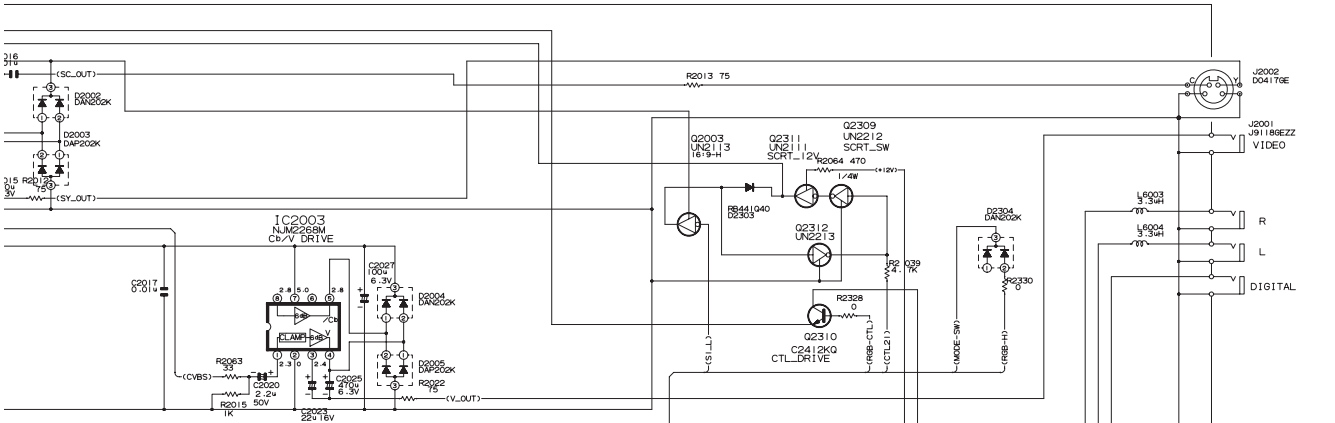
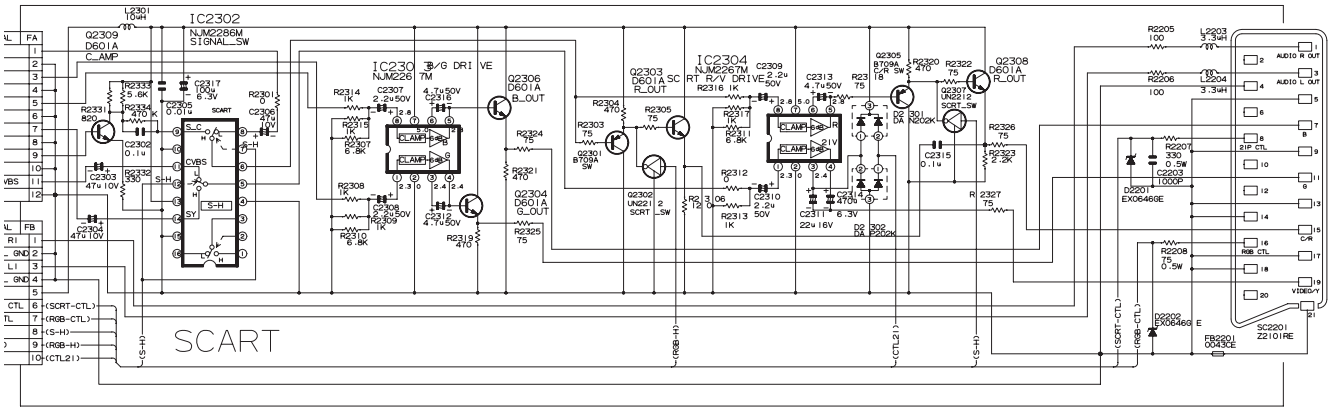
 (4/4)



### 14-3. TERMINAL/21-PIN EURO-SCART CIRCUI T SCHEMATIC DIAGRAM



⚠ AND SHADED COMPONENTS=SAFETY RELATED PARTS



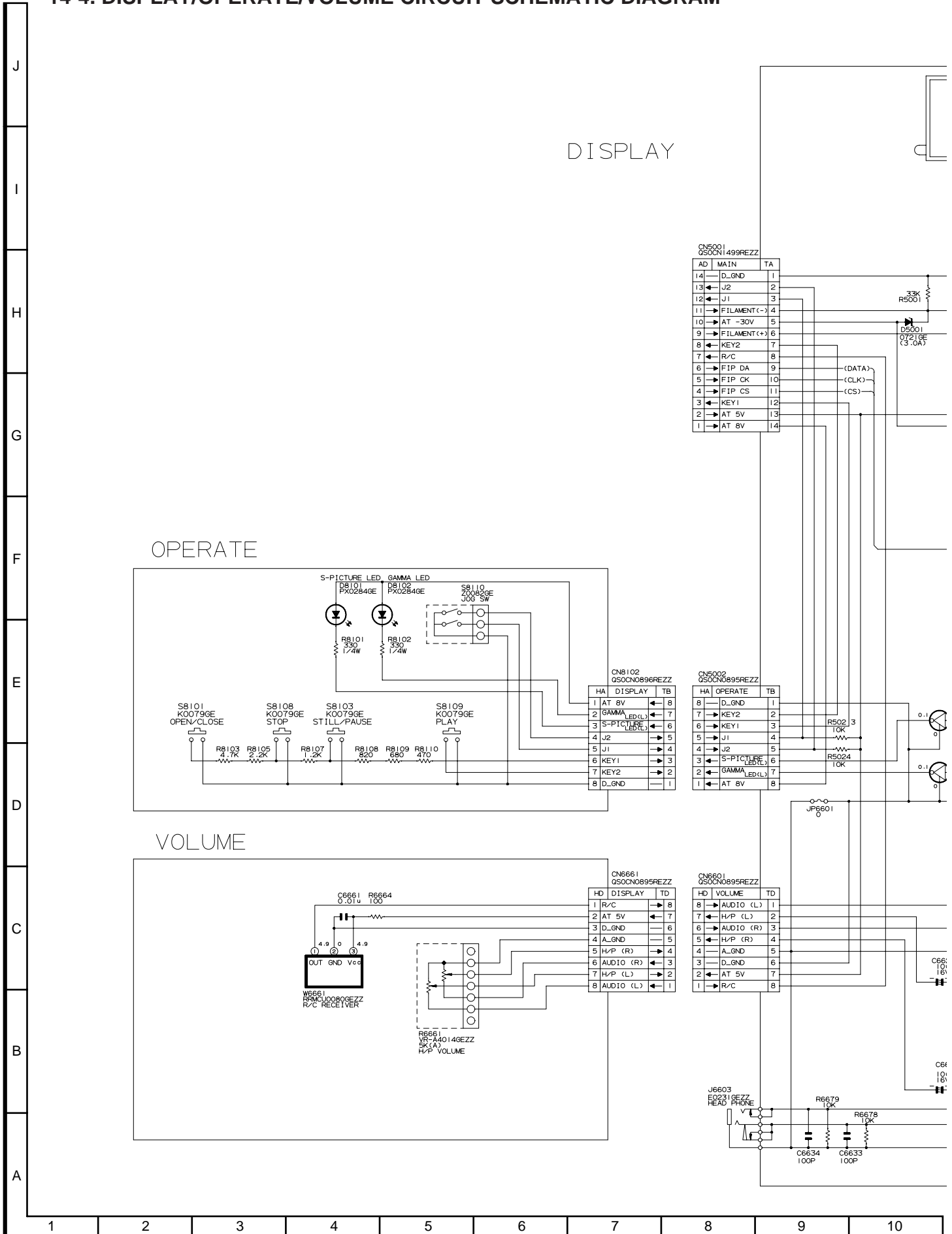
10	11	12	13	14	15	16	17	18	19
----	----	----	----	----	----	----	----	----	----

14-4. DISPLAY/OPERATE/VOLUME CIRCUIT SCHEMATIC DIAGRAM

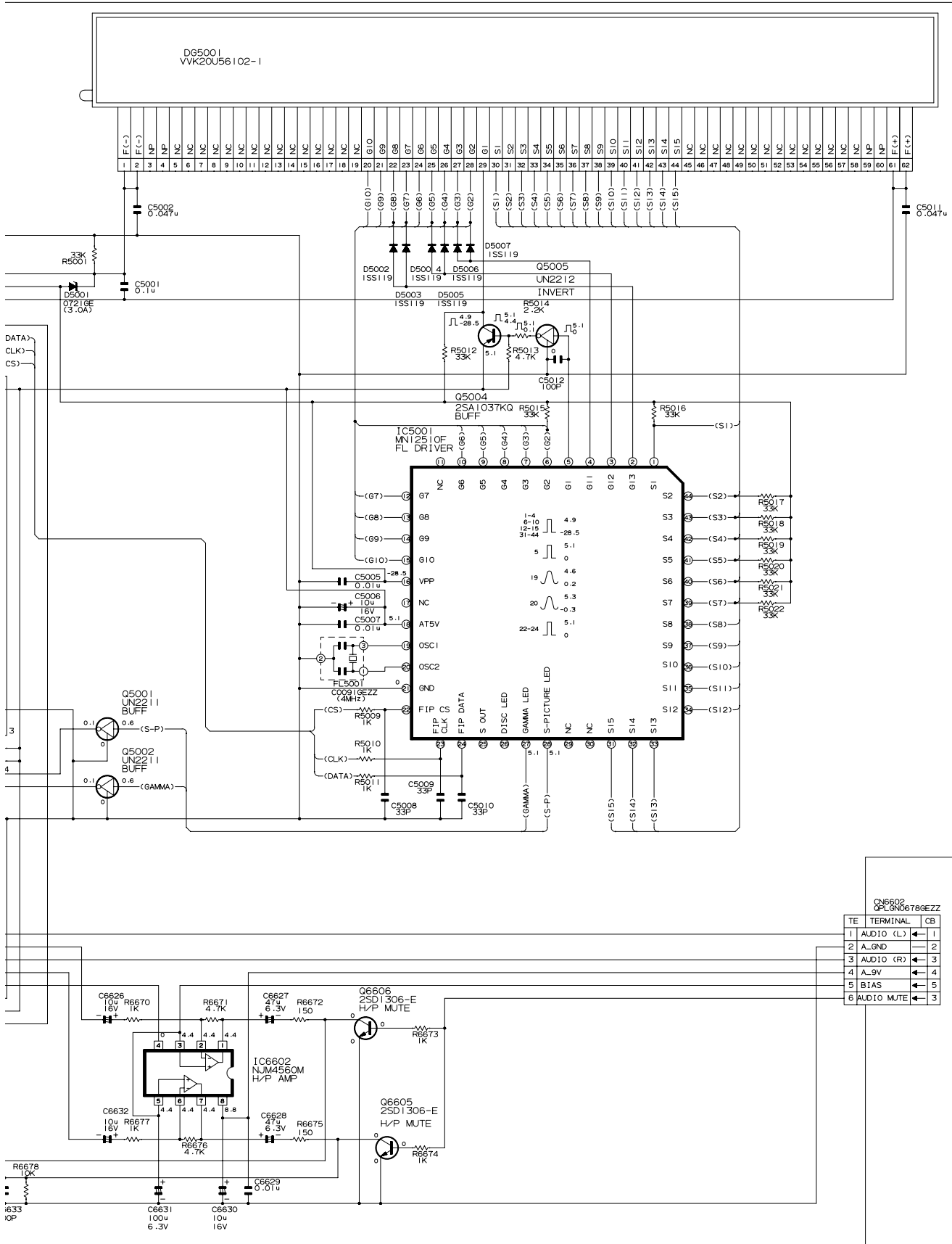
DISPLAY

OPERATE

VOLUME





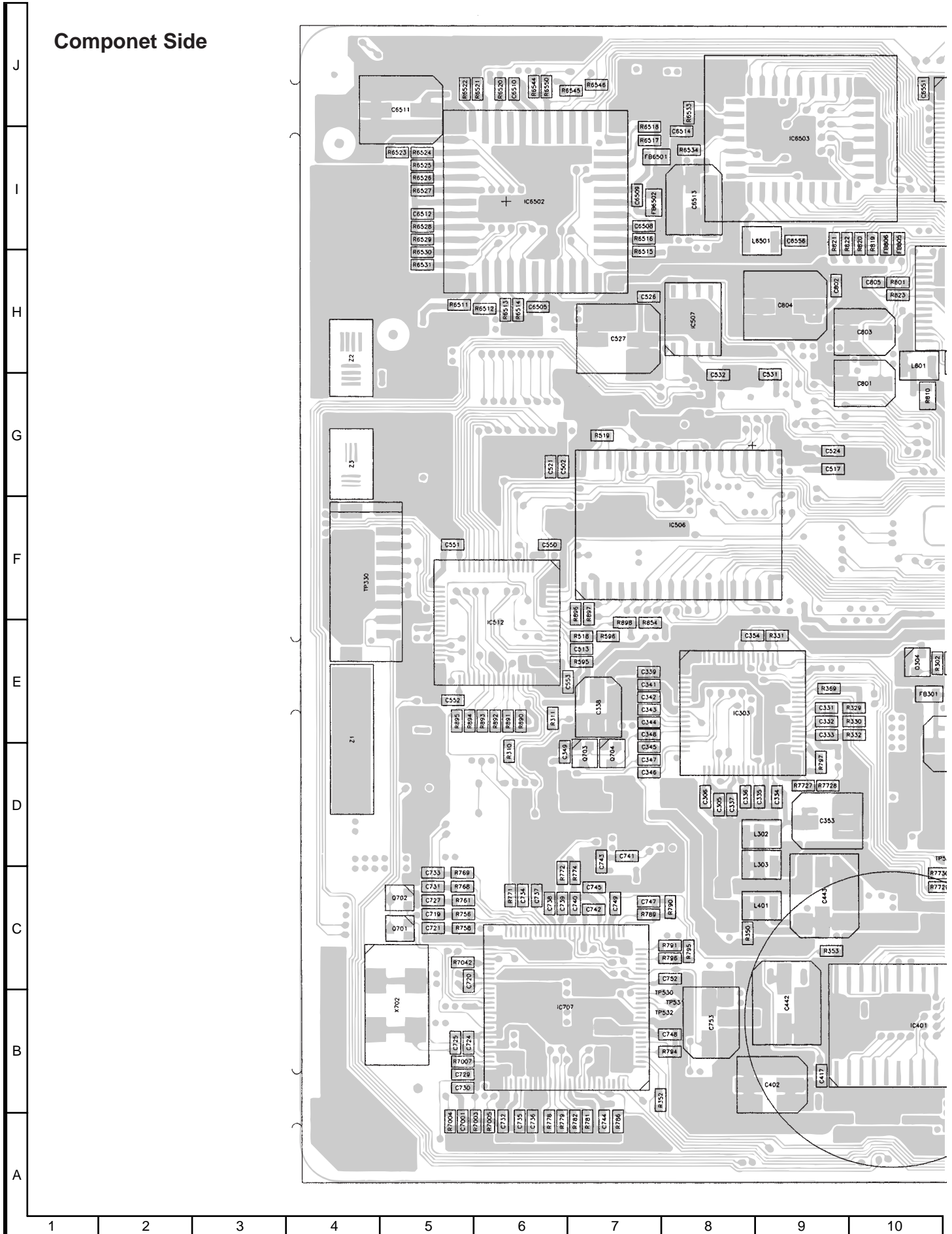


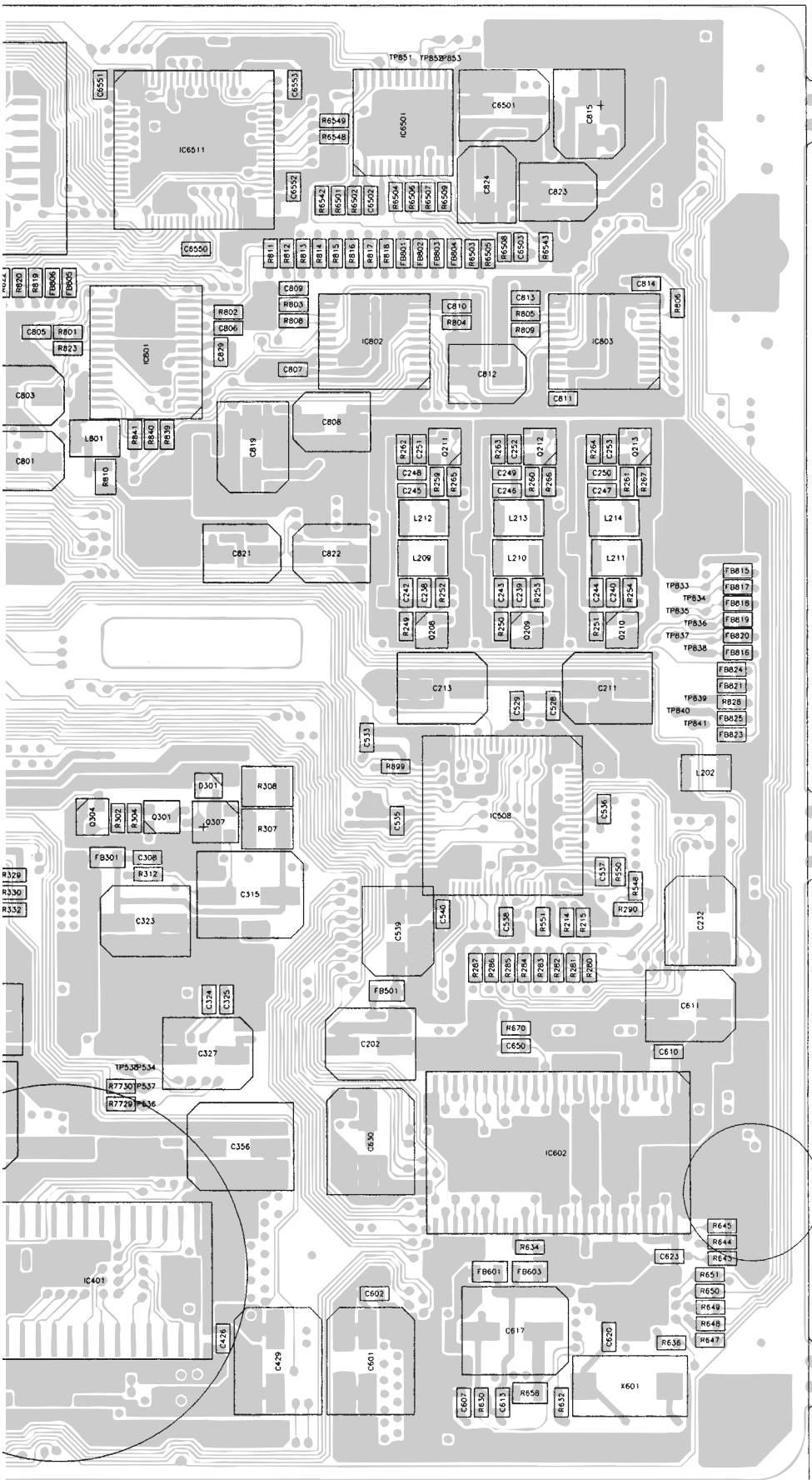
CN6602  
OPLGN0678GEZZ

TE	TERMINAL	CB
1	AUDIO (L)	1
2	A_GND	2
3	AUDIO (R)	3
4	A_3V	4
5	BIAS	5
6	AUDIO MUTE	3

# 15. PRINTED WIRING BOARD ASSEMBLIES 15-1. MAIN P.W.B.

Componet Side

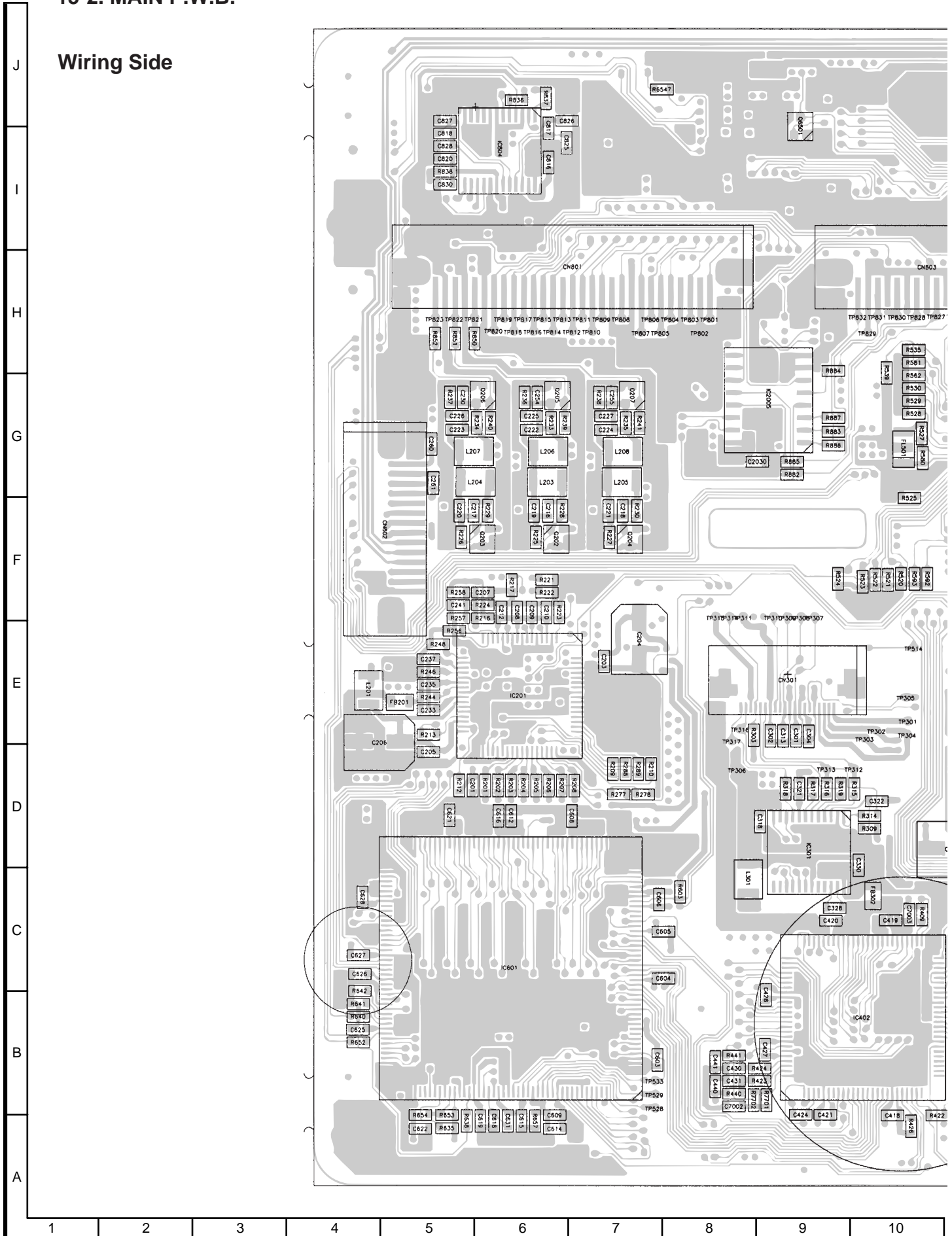


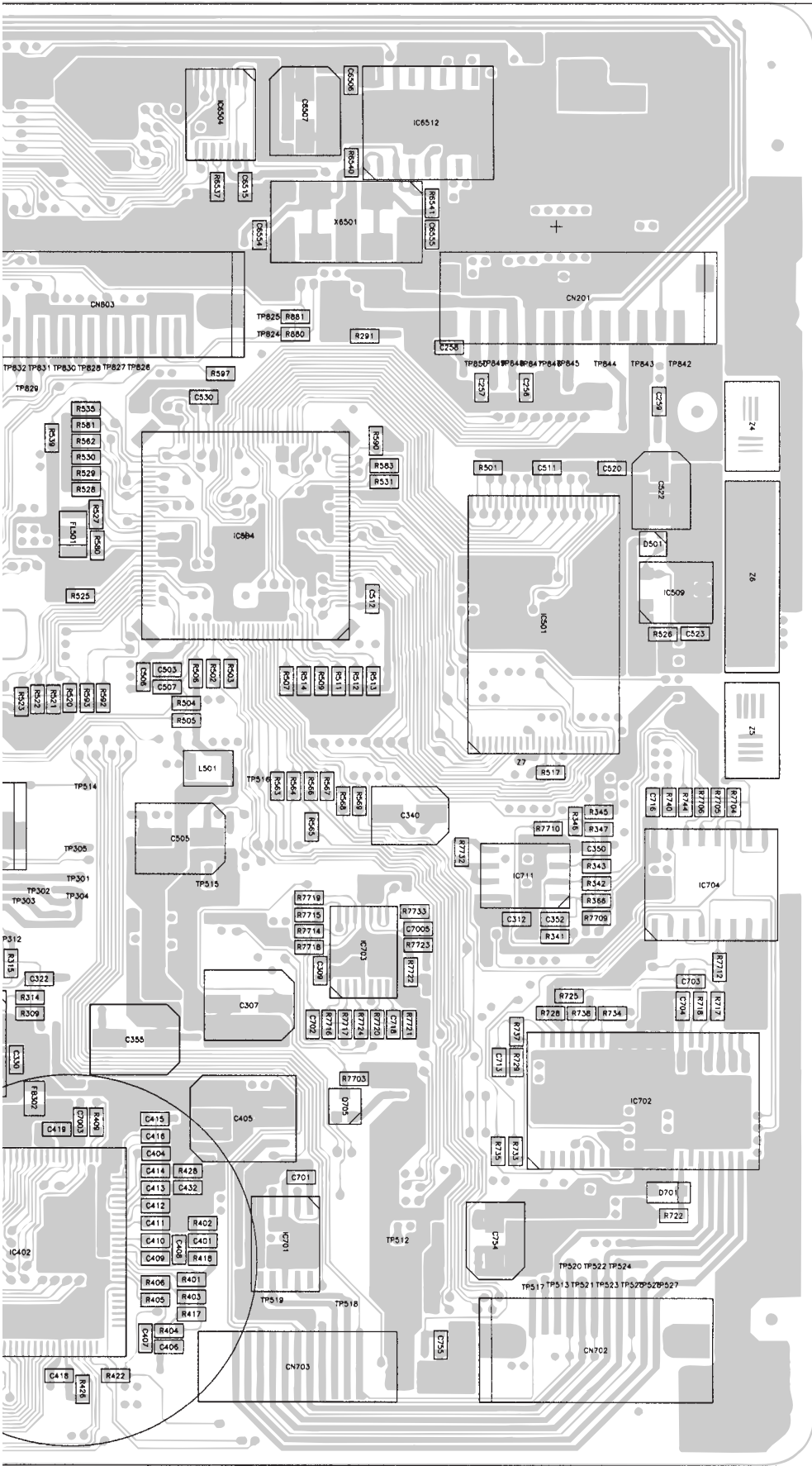


10	11	12	13	14	15	16	17	18	19
----	----	----	----	----	----	----	----	----	----

15-2. MAIN P.W.B.

Wiring Side

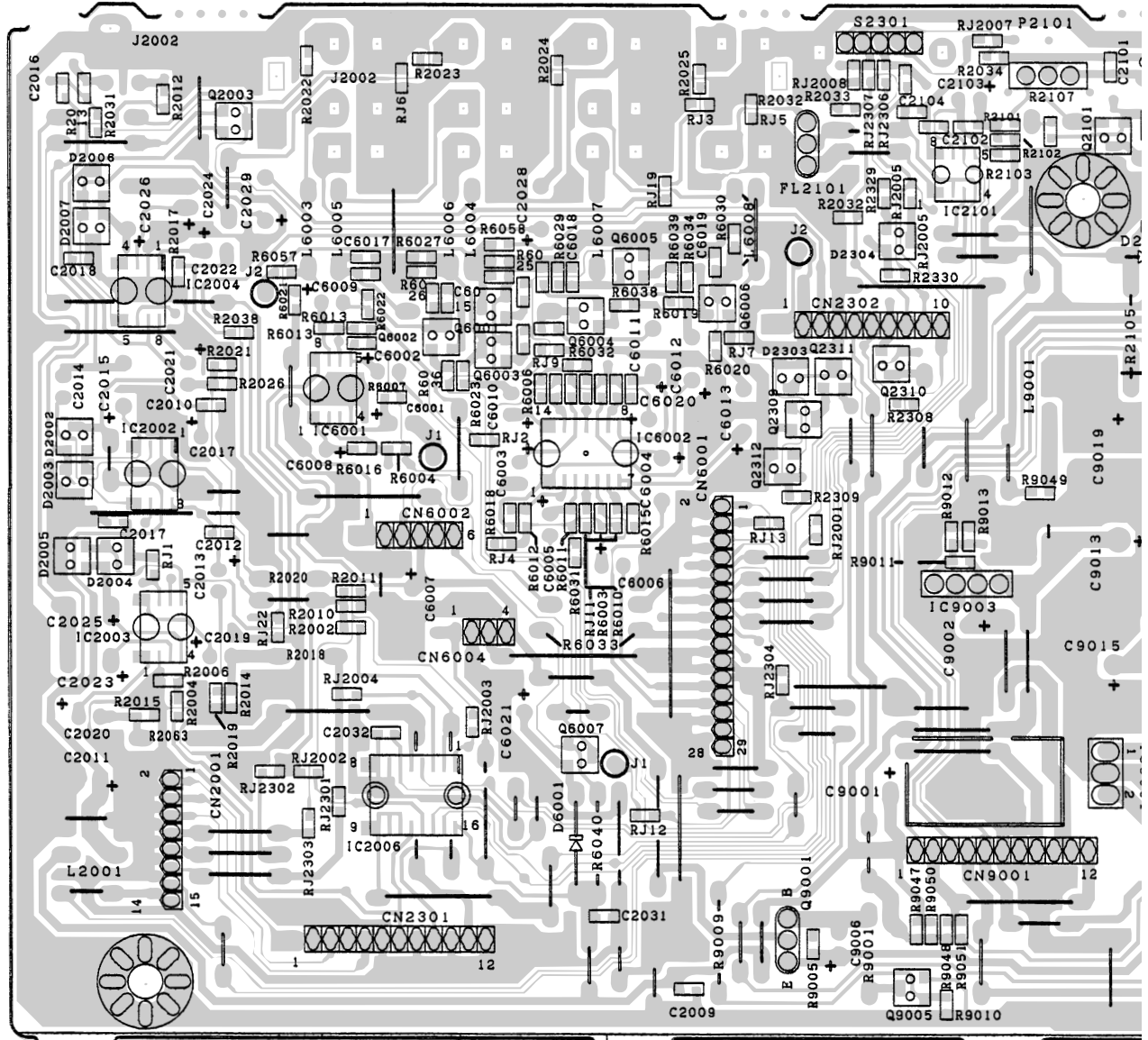




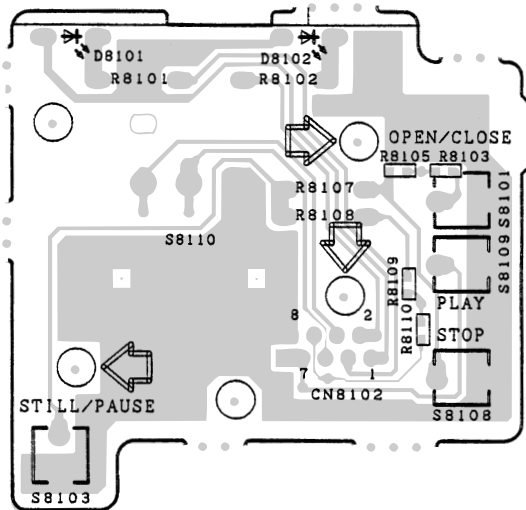
10	11	12	13	14	15	16	17	18	19
----	----	----	----	----	----	----	----	----	----

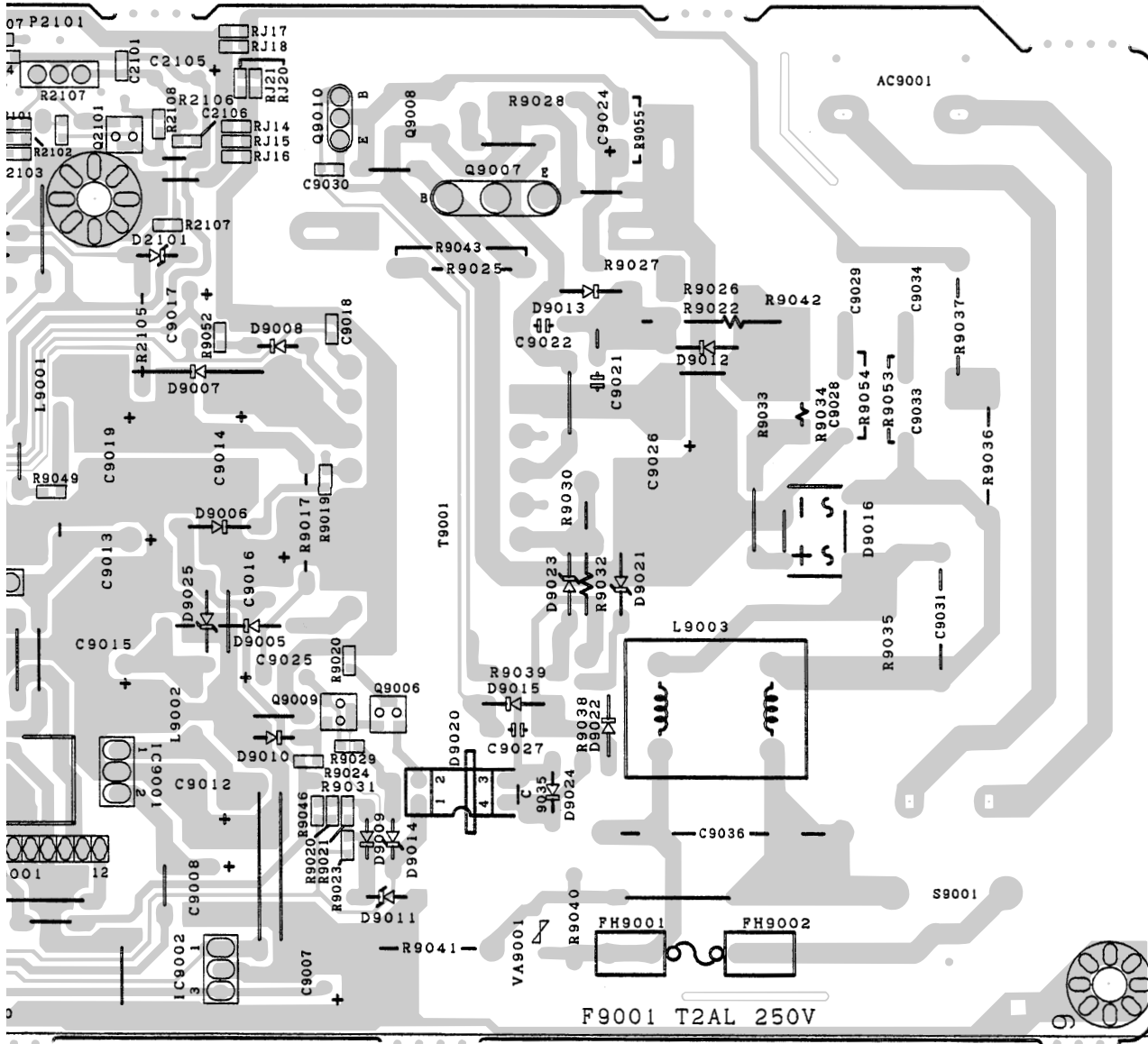
### 15-3. TERMINAL/OPERATE/VOLUME P.W.B.

#### TERMINAL

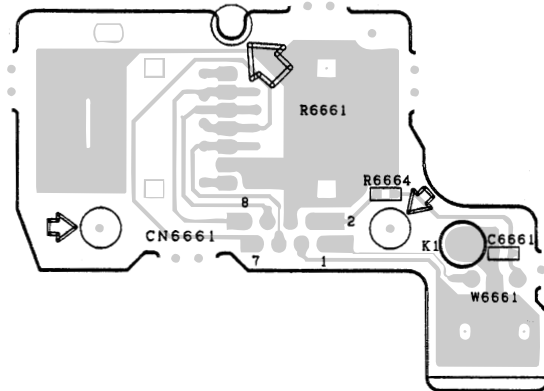


#### OPERATE



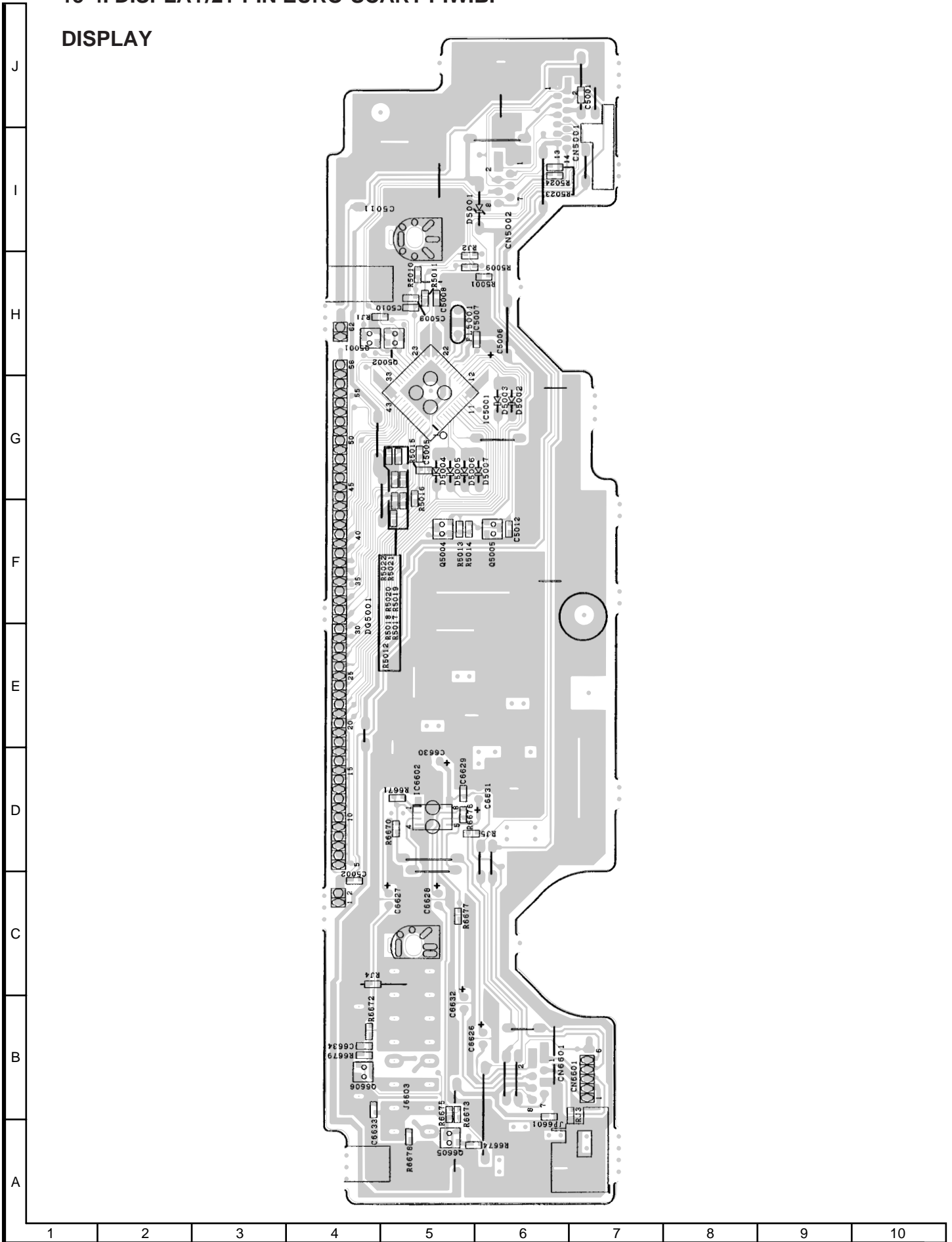


VOLUME



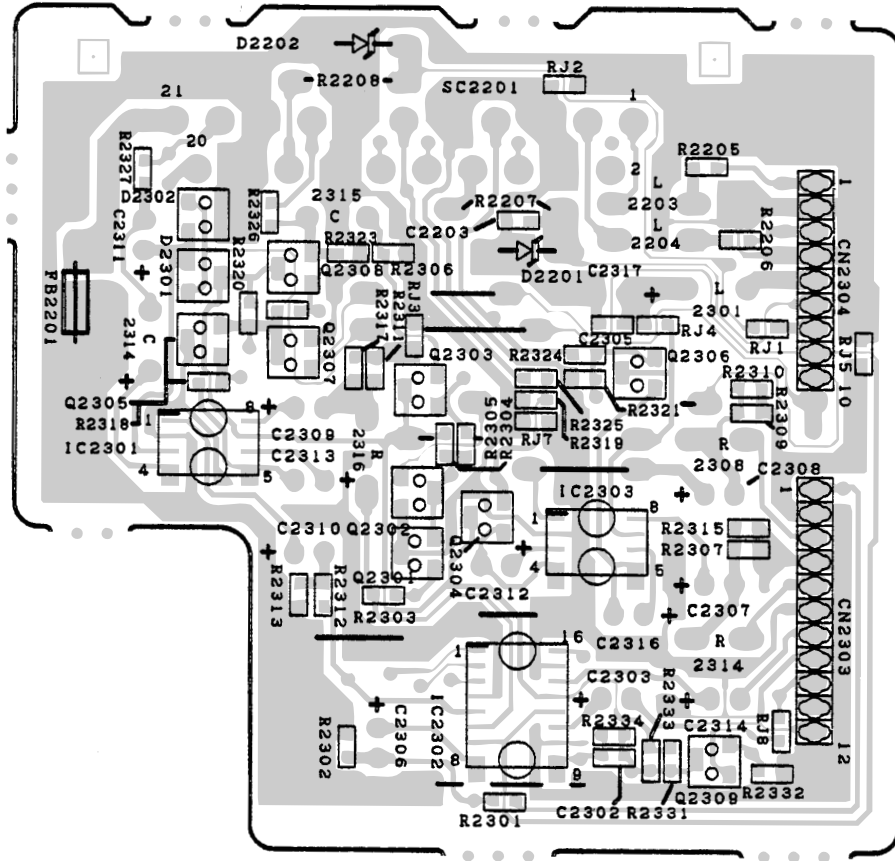
### 15-4. DISPLAY/21-PIN EURO-SCART P.W.B.

### DISPLAY

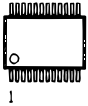
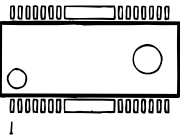
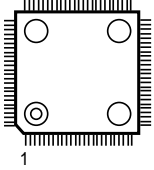
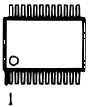
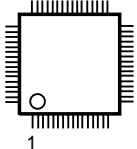

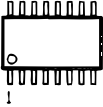
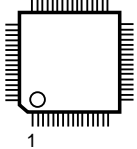
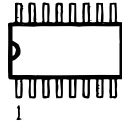
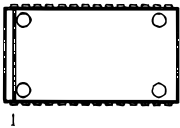
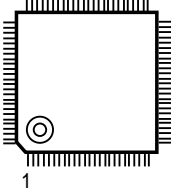
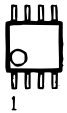
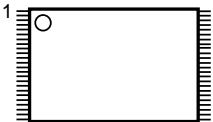
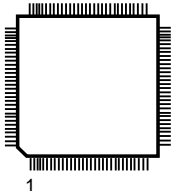

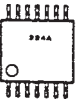
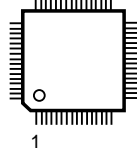
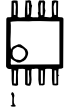
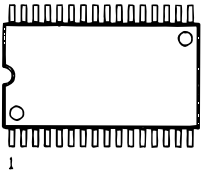
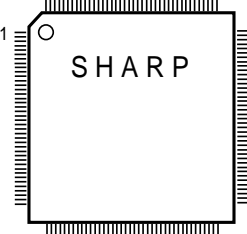
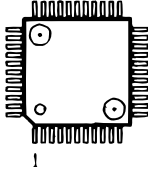
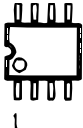
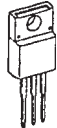


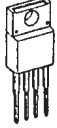




### 21-PIN EURO-SCART



## 16. SEMICONDUCTOR LEAD IDENTIFICATION

	IC301 RH-iX1461GEZZ		IC702 VHiBA6796FP-1		IC707 RH-iX1473GEZZ
	IC801 VHiPCM1716E-1		IC201 VHiMC44724A-1		X601 RCRSC0031GEZZ X702 RCRSC0035GEZZ
	IC2302 VHiNJM2286M-1		IC303 RH-iX1517GEZZ		IC2006 IC2005 IC704 RH-iX1531CEZZ
	IC401 RH-iX1484GEZZ		IC402 RH-iX1474GEZZ		IC2002 IC2003 VHiNJM2268M-1 IC2303 IC2304 VHiNJM2267M-1
	IC501 RH-iX1539GEZZ		IC504 RH-iX1478GEZZ		IC2102 VHiTC4W53F/-1
	IC703 VHi10324AFV-1		IC508 RH-iX1516GEZZ IC512 RH-iX1535GEZZ		IC6001 IC6602 VHiNJM4560M-1
	IC506 RH-iX1618GEZZ		IC601 RH-iX1521GEZZ		IC5001 VHiMN12510F-1
	IC507 VHiBR93L46F-1		IC9001 VHiT78DL09S-1 IC9002 VHiBA17808T-1		IC509 VHiPST600iM-1
	IC602 RH-iX0750TAZZ		IC9003 VHiPQ30RV211E		













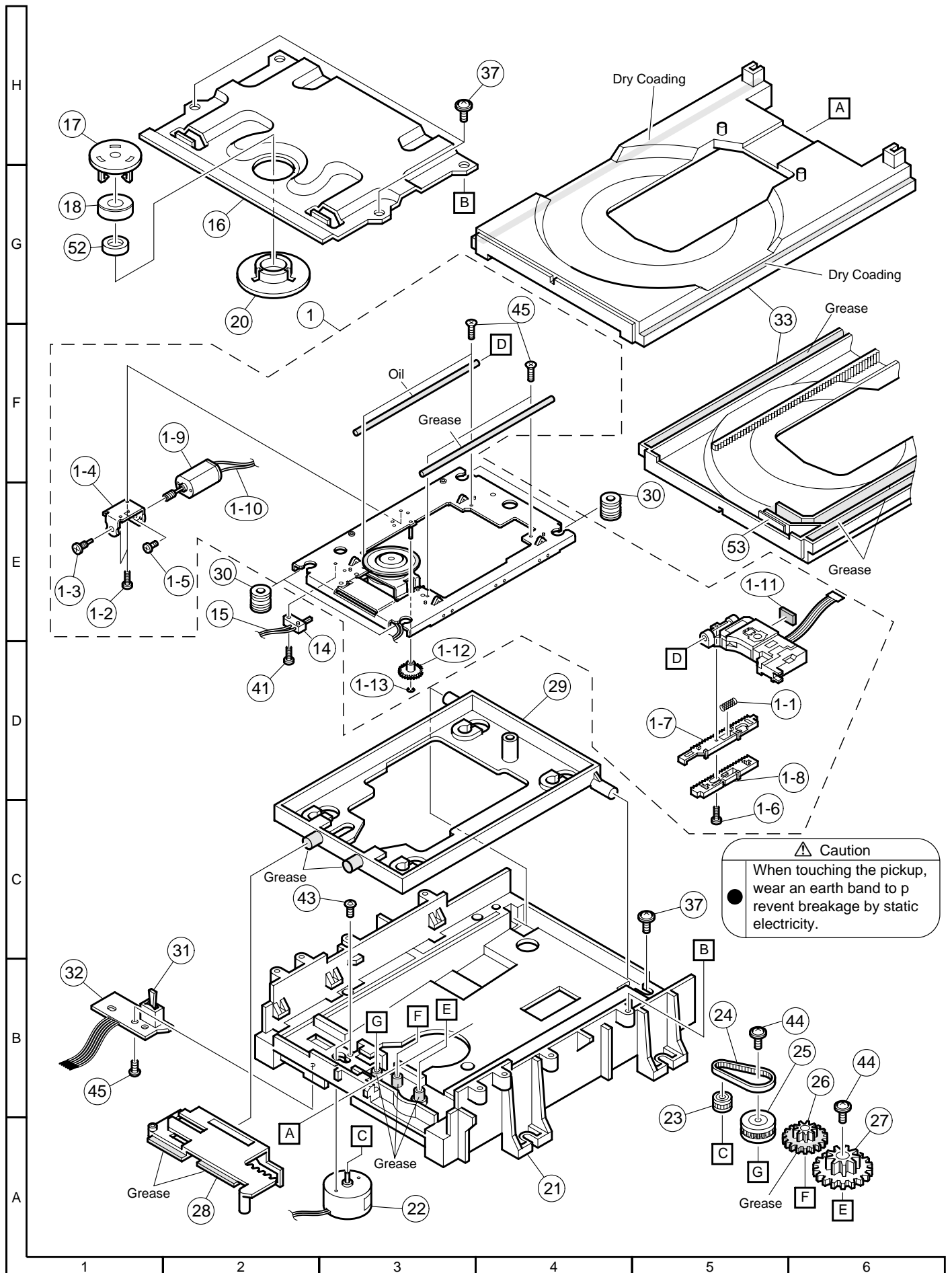




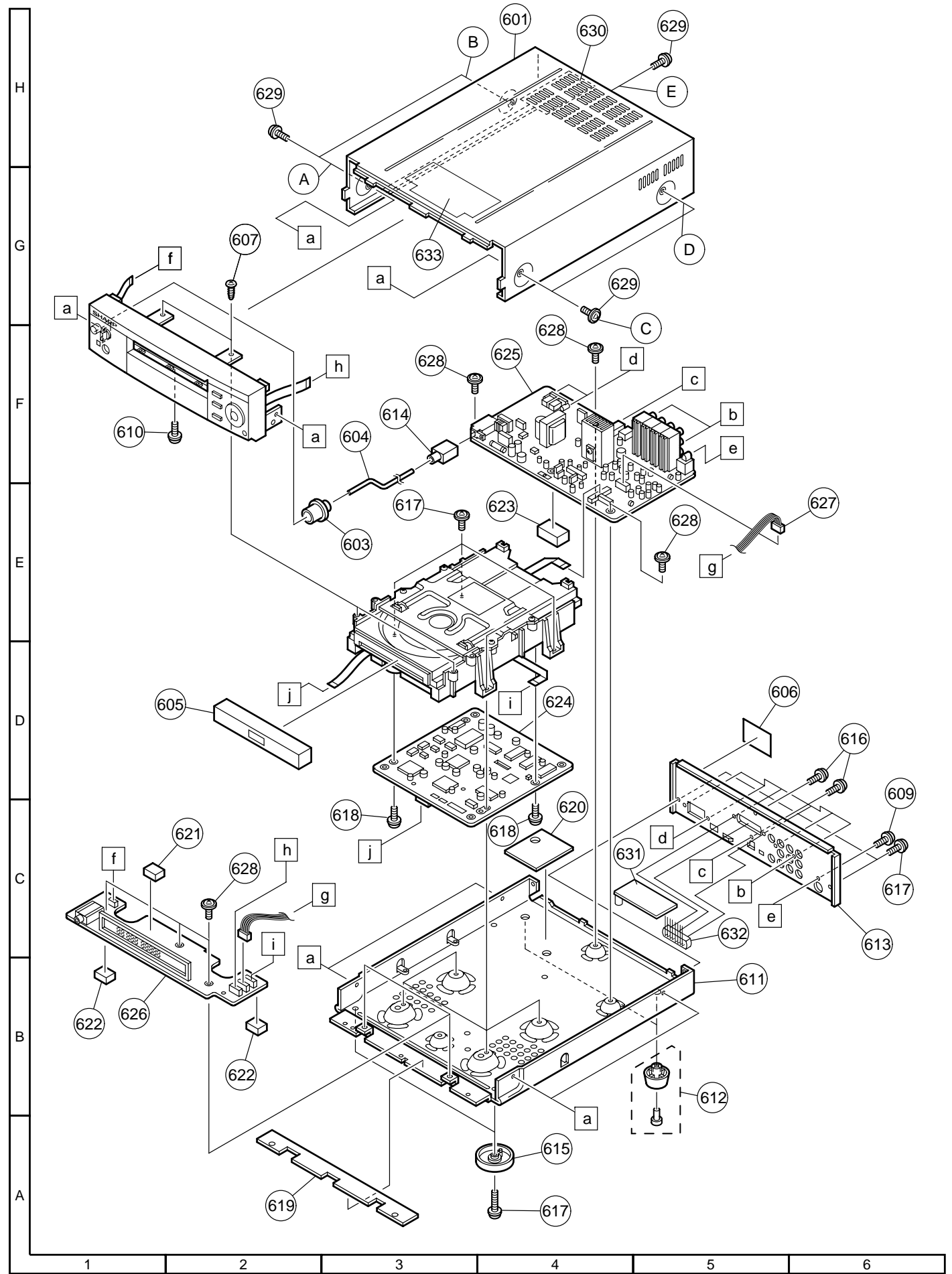




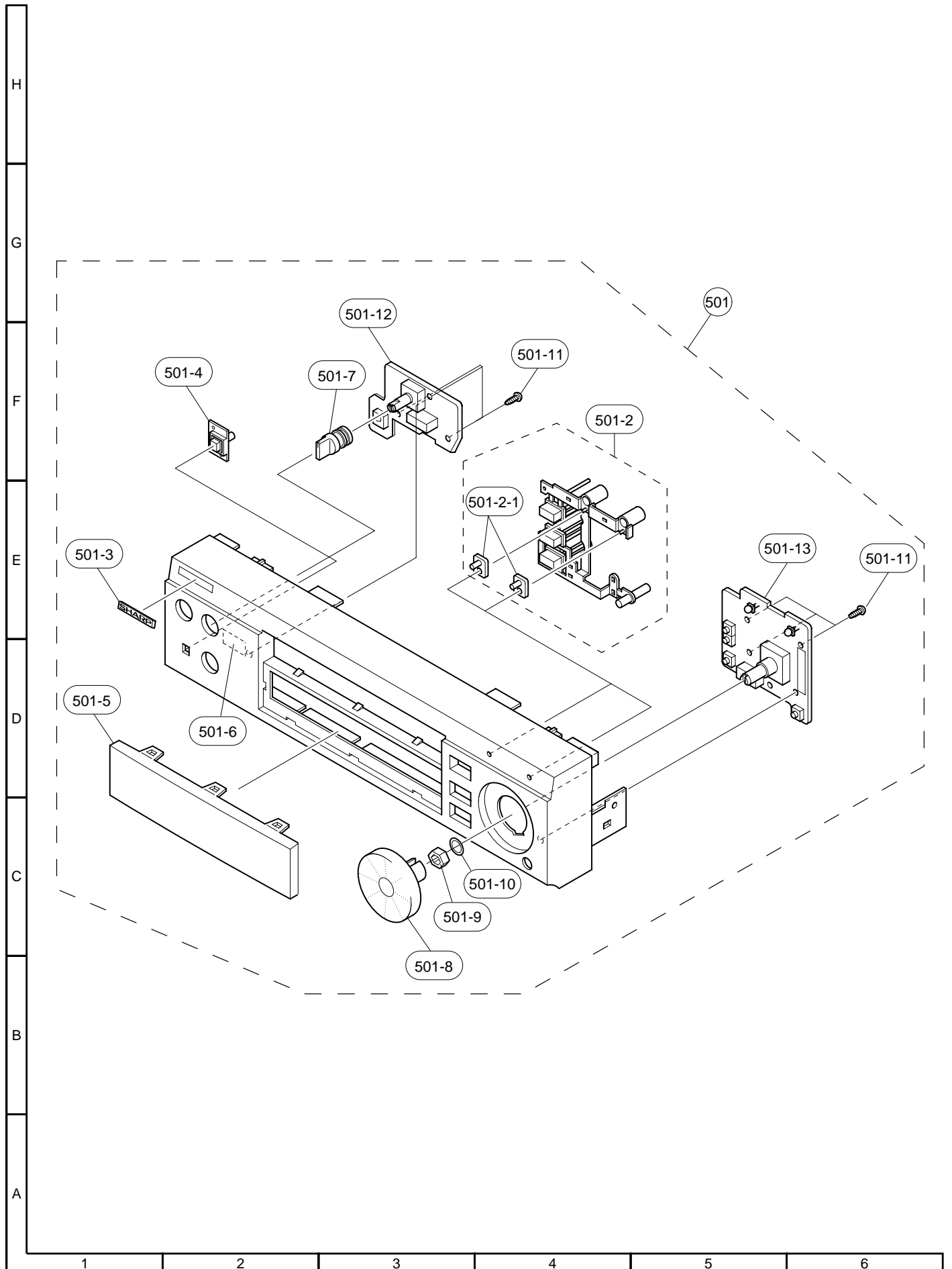
MECHANISM EXPLODED VIEW



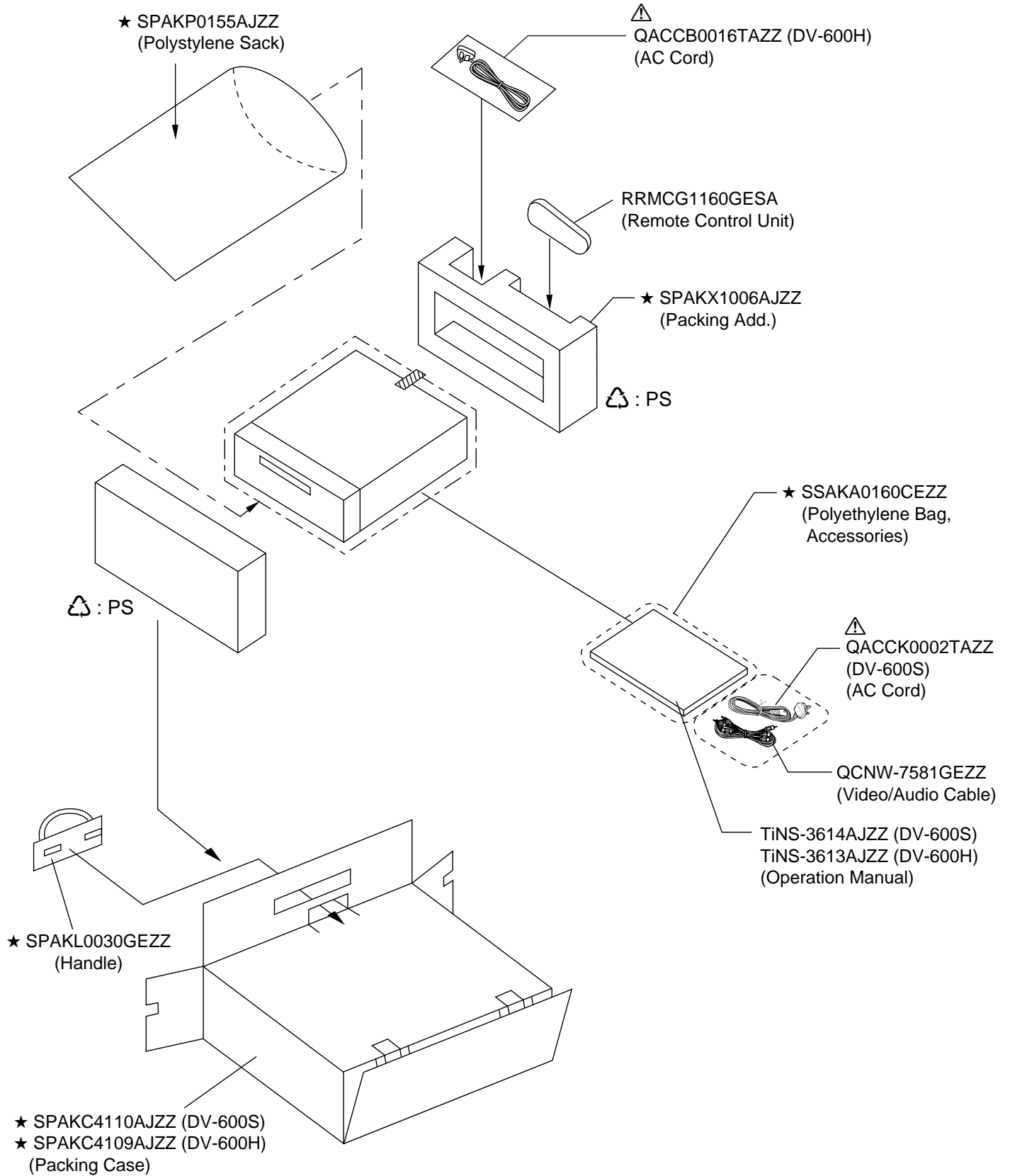
# CABINET EXPLODED VIEW



# FRONT PANEL PARTS EXPLODED VIEW



# 18. PACKING OF THE SET



★ Not Replacement Items

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