DVD4250D

DVD PLAYER

SERVICE MANUAL

1. GENERAL DESCRIPTION

1.1 ES66x8

The ES66x8 Vibratto II processor is a highly integrated single-chip DVD solution that integrates read channel, ECC, Servo DSP, MCU, and MPEG-2/MPEG-4/DivX decoder that has a state-of-the-art 480p/576p progressive-scan video feature to provide brilliant and sharp, flicker-free video output to the display, and with built-in gamma correction and S/PDIF input and output support. The 66x8 performs audio/video stream data processing, TV encoding, Macrovision copy protection, DVD system navigation, system control, and housekeeping functions.

The Vibratto II DVD processor is built on the ESS proprietary dual CPU Programmable Multimedia Processor (PMP) core consisting of 32-bit RISC and 64-bit DSP processors and offers the best DVD feature set.

These features can be listed as follows:

General Features:

- Single-chip DVD processor incorporating all front-end and back-end functions.
- Unified memory architecture.
- Built-in ADCs and DACs for servo control signals.
- DVD-Video, DVD-VR, VCD 1.1 and 2.0 and SVCD
- Proven ECC, EFM/EFM+ demodulation, and EDC circuit.
- Direct interface of 16-bit DRAM up to 128-Mb capacity.
- Direct interface of 8- or 16-bit SDRAM up to 128-Mb capacity.
- Direct interface for up to 4 banks of 8-bit EPROM or Flash EPROM for up to 4 MB per bank.
- Direct interface to the ES6603 servo AFE chip.

Video Related Features:

- Integrated NTSC/PAL encoder with pixel-adaptive de-interlacer and five 10-bit 54 MHz video DACs.
- DivX and MPEG-4 Advanced Simple Profile at full screen.
- Media playback with CD-ROM, CD-R/RW, DVD-R/RW and DVD+R/RW.
- Macrovision 7.1 for NTSC/PAL interlaced video.
- Macrovision NTSC/PAL (480p/576p) progressive scan video.
- Simultaneous composite, S-video and YUV outputs.
- CCIR656/601 YUV 4:2:2 output.
- OSD controller supports 256 colors in 8 degrees of transparency.
- JPEG digital photo CD support (Kodak Picture CD and Fujifilm FujiColor CD).

Audio Related Features:

- Full DVD-Audio support including MLP and LPCM decode, CPPM decryption, and watermark detection.
- Up to 7.1 channel audio outputs.
- Bass management.
- Dolby Digital (AC-3), Dolby Pro Logic, and Pro Logic II.
- DTS surround (ES6698 only).
- S/PDIF digital audio input and output.
- SRS TruSurround.
- Professional karaoke with full scoring scheme.

1.2 MEMORY

1.2.1 System SRAM Interface

The system SRAM interface controls access to optional external SRAM, which can be used for RISC code, stack, and data. The SRAM bus supports four independent address spaces, each having programmable bus width and wait states. The interface can support not only SRAM, but also
ROM/EPROM and memory-mapped I/O ports for standalone applications are supported.

1.2.2 DRAM Memory Interface

The Vibratto II provides a glueless 16-bit interface to DRAM memory devices used as video memory for a DVD player. The maximum amount of memory supported is 16 MB of Synchronous DRAM (SDRAM). The memory interface is configurable in depth to support 128-Mb addressing. The memory interface controls access to both external SDRAM or EDO memories, which can be the sole unified external read/write memory acting as program and data memory as well as various decoding and display buffers.

1.3 FRONT PANEL

The front panel is based around an Futaba VFD and a common front panel controller chip, (uPT6311). The ES66x8 controls the uPT6311 using several control signals, (clock, data, chip select). The infrared remote control signal is passed directly to the ES66x8 for decoding.

1.4 REAR PANEL

A typical rear panel is included in the reference design. This rear panel supports:

- six channel and two channel audio outputs
- Optical and coax S/PDIF outputs.
- Composite, S-Video, and SCART outputs

The six-video signals used to provide CVBS, S-Video, and RGB are generated by the ES66x8's internal video DAC. The video signals are buffered by external circuitry.

Six channel audio output by the ES66x8 in the form of three I^2S (or similar) data streams. The S/PDIF serial stream is also generated by the ES66x8 output by the rear panel. A six channel audio DAC are used for six channel audio output with ES66x8, and similarly one Audio DAC is used for two channel audio output with ES66x8.

2. System Block Diagram and ES66x8 Pin Description

2.1 ES66x8 Pin Description

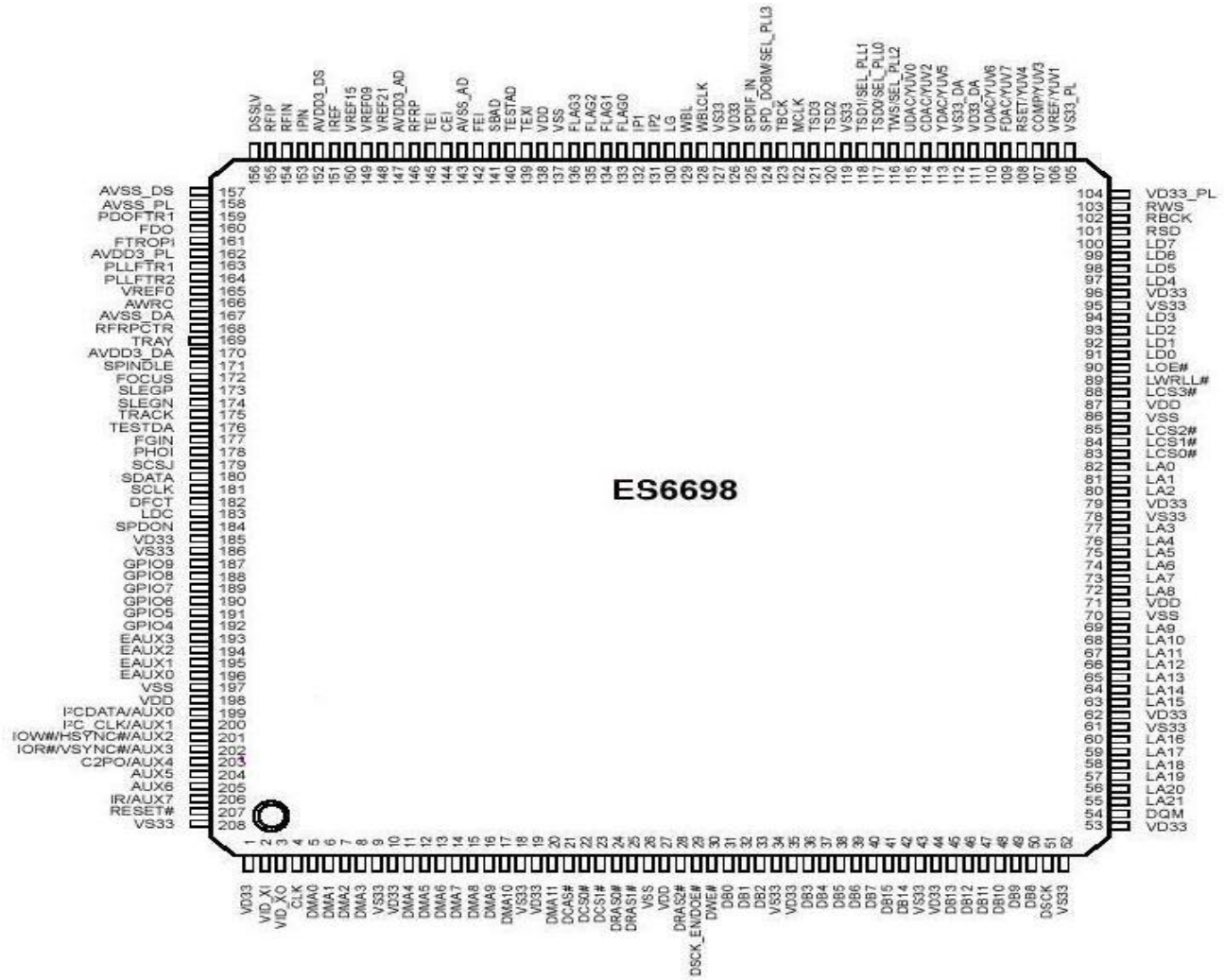


Table 1 ES6698 Pin Description

Names	Pin Numbers	I/O	Definitions
VD33	1, 10, 19, 35, 44, 53, 62, 79, 96, 126, 185	P	I/O power supply.
VID_XI	2	I	Crystal input.
VID_XO	3	O	Crystal output.
CLK	4	I	System clock.
DMA[11:0]	5:8 11:17, 20	O	DRAM address bus.
VS33	9, 18, 34, 43, 52, 61, 78, 95, 119, 127, 186, 208	G	Ground for I/O power supply.
DCAS#	21	O	DRAM column address strobe (active-low)
DCS[1:0]#	22, 23	O	DRAM chip select (active-low).
DRAS[2:0]#	24, 25, 28	O	DRAM row address strobe (active-low).
VSS	26, 70, 86, 137, 197	G	Ground for core power supply.
VDD	27, 71, 87, 138, 198	P	Core power supply.
DSCK_EN	29	O	DRAM clock enable output.
DOE#		O	DRAM output enable (active-low).
DWE#	30	O	DRAM write enable (active-low).
DB[15:0]	31:33, 36:42, 45:50	I/O	DRAM data bus.
DSCK	51	O	Output clock to DRAM.
DQM	54	O	Data input/output mask.
LA[21:0]	55:60, 63:69, 72:77, 80:82	O	RISC port address bus.
LCS[3:0]#	83:85, 88	O	RISC port chip select (active-low).
LWRLL#	89	O	RISC port low-byte write enable (active-low).
LOE#	90	O	RISC port output enable (active-low).
LD[7:0]	91:94, 97:100	I/O	RISC port data bus; (5V tolerant input).
RSD	101	I	Audio receive serial data; (5V tolerant input).
RBCK	102	I	Audio receive bit clock; (5V tolerant input).
RWS	103	I	Audio receive frame sync; (5V tolerant input).
VD33_PL	104	P	Power for PLL blocks.
VS33_PL	105	G	Ground for PLL blocks.
VREF	106	I	Internal voltage reference to video DAC.
YUV1		O	YUV pixel 1 output data.
COMP	107	I	Compensation input.
YUV3		O	YUV pixel 3 output data.

Table 1 ES6698 Pin Description (Continued)

<table>
<tr><th>Names</th><th>Pin Numbers</th><th>I/O</th><th>Definitions</th></tr>
<tr><td>RSET</td><td rowspan="2">108</td><td>I</td><td>DAC current adjustment resistor input.</td></tr>
<tr><td>YUV4</td><td>O</td><td>YUV pixel 4 output data.</td></tr>
<tr><td>FDAC</td><td rowspan="2">109</td><td>O</td><td>Video DAC output. Refer to description and matrix for UDAC pin 115.</td></tr>
<tr><td>YUV7</td><td>O</td><td>YUV pixel 7 output data.</td></tr>
<tr><td>VDAC</td><td rowspan="2">110</td><td>O</td><td>Video DAC output. Refer to description and matrix for UDAC pin 115.</td></tr>
<tr><td>YUV6</td><td>O</td><td>YUV pixel 6 output data.</td></tr>
<tr><td>VD33_DA</td><td>111</td><td>P</td><td>Power for I/O power supply for VDAC.</td></tr>
<tr><td>VS33_DA</td><td>112</td><td>G</td><td>Ground for I/O power supply for VDAC.</td></tr>
<tr><td>YDAC</td><td rowspan="2">113</td><td>O</td><td>Video DAC output. Refer to description and matrix for UDAC pin 115.</td></tr>
<tr><td>YUV5</td><td>O</td><td>YUV pixel 5 output data.</td></tr>
<tr><td>CDAC</td><td rowspan="2">114</td><td>O</td><td>Video DAC output. Refer to description and matrix for UDAC pin 115.</td></tr>
<tr><td>YUV2</td><td>O</td><td>YUV pixel 2 output data.</td></tr>
<tr><td>UDAC</td><td rowspan="2">115</td><td>O</td><td>Video DAC output.
<table>
<tr><th>Pin</th><th>109</th><th>110</th><th>113</th><th>114</th><th>115</th></tr>
<tr><th>Value</th><th>F DAC</th><th>V DAC</th><th>Y DAC</th><th>C DAC</th><th>U DAC</th></tr>
<tr><td>0</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>C</td><td>N/A</td></tr>
<tr><td>1</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>C</td><td>CVBS2</td></tr>
<tr><td>2</td><td>CVBS/Chroma</td><td>N/A</td><td>Y</td><td>C</td><td>N/A</td></tr>
<tr><td>3</td><td>CVBS/Chroma</td><td>CVBS1</td><td>N/A</td><td>N/A</td><td>CVBS2</td></tr>
<tr><td>4</td><td>CVBS/Chroma</td><td>CVBS1</td><td>N/A</td><td>N/A</td><td>N/A</td></tr>
<tr><td>5</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>Pb</td><td>Pr</td></tr>
<tr><td>6</td><td>CVBS/Chroma</td><td>N/A</td><td>Y</td><td>Pb</td><td>Pr</td></tr>
<tr><td>7</td><td>N/A</td><td>SYNC</td><td>G</td><td>B</td><td>R</td></tr>
<tr><td>8</td><td>CVBS/Chroma</td><td>Chroma</td><td>Y</td><td>Pb</td><td>Pr</td></tr>
<tr><td>9</td><td>CVBS</td><td>CVBS1</td><td>G</td><td>B</td><td>R</td></tr>
<tr><td>10</td><td>CVBS</td><td>CVBS1</td><td>G</td><td>R</td><td>B</td></tr>
<tr><td>11</td><td>N/A</td><td>SYNC</td><td>G</td><td>R</td><td>B</td></tr>
<tr><td>12</td><td>CVBS/Chroma</td><td>N/A</td><td>Y</td><td>Pr</td><td>Pb</td></tr>
<tr><td>13</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>Pr</td><td>Pb</td></tr>
<tr><td>14</td><td>Chroma</td><td>Y</td><td>G</td><td>R</td><td>B</td></tr>
</table>
F: CVBS/chroma signal for simultaneous mode.
Y: Luma component for YUV and Y/C processing.
C: Chrominance signal for Y/C processing.
U: Chrominance component signal for YUV mode.
V: Chrominance component signal for YUV mode.</td></tr>
<tr><td>YUV0</td><td>O</td><td>YUV pixel 0 output data.</td></tr>
</table>

Table 1 ES6698 Pin Description (Continued)

<table>
<tr><th>Names</th><th>Pin Numbers</th><th>I/O</th><th>Definitions</th></tr>
<tr><td>TWS</td><td rowspan="2">116</td><td>O</td><td>Audio transmit frame sync output.</td></tr>
<tr><td>SEL_PLL2</td><td>I</td><td>System and DSCK output clock frequency selection is made at the rising edge of RESET#. The matrix below lists the available clock frequencies and their respective PLL bit settings. Strapped to VCC or ground via 4.7-kΩ resistor; read-only during reset.
<table>
<tr><th>SEL_PLL2</th><th>SEL_PLL1</th><th>SEL_PLL0</th><th>Clock Type (MHz)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>CLK × 4.5</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>CLK × 5.0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Bypass</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>CLK × 4.0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>CLK × 4.25</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>CLK × 4.75</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>CLK × 5.5</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>CLK × 6.0</td></tr>
</table></td></tr>
<tr><td>TSD0</td><td rowspan="2">117</td><td>O</td><td>Audio transmit serial data port 0.</td></tr>
<tr><td>SEL_PLL0</td><td>I</td><td>Refer to the description and matrix for SEL_PLL2 pin 116.</td></tr>
<tr><td>TSD1</td><td rowspan="2">118</td><td>O</td><td>Audio transmit serial data port 1.</td></tr>
<tr><td>SEL_PLL1</td><td>I</td><td>Refer to the description and matrix for SEL_PLL2 pin 116.</td></tr>
<tr><td>TSD[2:3]</td><td>120, 121</td><td>O</td><td>Audio transmit serial data ports 2 and 3.</td></tr>
<tr><td>MCLK</td><td>122</td><td>I/O</td><td>Audio master clock for audio DAC.</td></tr>
<tr><td>TBCK</td><td>123</td><td>O</td><td>Audio transmit bit clock.</td></tr>
<tr><td>SPD_DOBM</td><td rowspan="2">124</td><td>O</td><td>S/PDIF output.</td></tr>
<tr><td>SEL_PLL3</td><td>I</td><td>Clock source select. Strapped to VCC or ground via 4.7-kΩ resistor; read only during reset.
<table>
<tr><th>SEL_PLL3</th><th>Clock Source</th></tr>
<tr><td>0</td><td>Crystal oscillator</td></tr>
<tr><td>1</td><td>CLK input</td></tr>
</table></td></tr>
<tr><td>SPDIF_IN</td><td>125</td><td>I</td><td>S/PDIF input; (5V tolerant input).</td></tr>
<tr><td>WBLCLK</td><td>128</td><td>O</td><td>DVD-RAM wobble detector circuit clock source to preamp.</td></tr>
<tr><td>WBL</td><td>129</td><td>O</td><td>DVD-RAM wobble output.</td></tr>
<tr><td>LG</td><td>130</td><td>O</td><td>DVD-RAM land/groove flag.</td></tr>
<tr><td>IP2</td><td>131</td><td>I</td><td>DVD-RAM header position index 2.</td></tr>
<tr><td>IP1</td><td>132</td><td>I</td><td>DVD-RAM header position index 1.</td></tr>
<tr><td>FLAG[3:0]</td><td>133:136</td><td>O</td><td>To monitor servo status.</td></tr>
<tr><td>TEXI</td><td>139</td><td>I</td><td>High-speed tracking error input.</td></tr>
<tr><td>TESTAD</td><td>140</td><td>I</td><td>Test AD input.</td></tr>
<tr><td>SBAD</td><td>141</td><td>I</td><td>Sub-beam addition input signal.</td></tr>
<tr><td>FEI</td><td>142</td><td>I</td><td>Focus input error signal.</td></tr>
</table>

Table 1 ES6698 Pin Description (Continued)

Names	Pin Numbers	I/O	Definitions
AVSS_AD	143	G	Analog ground for ADC block.
CEI	144	I	Center error input signal.
TEI	145	I	Tracking error input signal.
RFRP	146	I	RF ripple/envelope input signal.
AVDD3_AD	147	P	Analog power supply for ADC block.
VREF21	148	O	2.1V reference voltage.
VREF09	149	O	0.9V reference voltage.
VREF15	150	O	1.5V reference voltage.
IREF	151	I	Servo data PLL interface reference current generator. Connect a resistor between this pin and ground to set reference current.
AVDD3_DS	152	P	Analog power supply for data slicer block.
IPIN	153	I	Inverting input of data slicer.
RFIN	154	I	Analog RF signal input after passing through equalizer (minus).
RFIP	155	I	Analog RF signal input after passing through equalizer (plus).
DSSLV	156	O	Data slicer level output.
AVSS_DS	157	G	Analog ground for data slicer block.
AVSS_PL	158	G	Analog ground for data PLL block.
PDOFTR1	159	O	Servo data PLL phase detector filter pin number 1.
FDO	160	O	Servo data PLL output node of frequency detector charge pump.
FTROPI	161	I	Servo data PLL input node of loop filter OP circuit.
AVDD3_PL	162	P	Analog power supply for data PLL block.
PLLFTR1	163	I	Servo data PLL loop filter pin number 1.
PLLFTR2	164	I	Servo data PLL loop filter pin number 2.
VREF0	165	O	Servo data PLL reference voltage output.
AWRC	166	I/O	Auto wide range control VCO signal from/to AWRC DAC.
AVSS_DA	167	G	Analog ground for DAC part.
RFRPCTR	168	I/O	Central level of RFRP.
TRAY	169	O	Output voltage level for tray buffer IC.
AVDD3_DA	170	P	Analog power supply for DAC part.
SPINDLE	171	O	Output voltage level for spindle buffer IC.
FOCUS	172	O	Output voltage level for focus buffer IC.
SLEGP	173	O	Output voltage level for Sledge buffer IC (plus).
SLEGN	174	O	Output voltage level for Sledge buffer IC (minus).
TRACK	175	O	Output voltage level for tracking buffer IC.
TESTDA	176	O	Test DA output.
FGIN	177	I	Spindle hall sensor input.

Table 1 ES6698 Pin Description (Continued)

Names	Pin Numbers	I/O	Definitions
PHOI	178	I	Sledge photo interrupt signal input.
SCSJ	179	O	Chip selection signal to RF chip (serial data enable).
SDATA	180	I/O	Data signal from/to RF chip.
SCLK	181	O	Serial clock source to RF chip.
DFCT	182	I	Defect flag input signal.
LDC	183	O	Laser diode on/off control output.
SPDON	184	O	Spindle power driver on/off control output.
GPIO[9:4]	187:192	I/O	General-purpose input/output used for servo control; (5V tolerant input).
EAUX[3:0]	193:196	I/O	Extended auxilliary ports; (5V tolerant input).
I²CDATA	199	I/O	I²C data I/O; (5V tolerant input).
AUX0		I/O	Auxiliary port (open collector); (5V tolerant input).
I²C_CLK	200	I/O	I²C clock I/O; (5V tolerant input).
AUX1		I/O	Auxiliary port (open collector); (5V tolerant input).
IOW#	201	O	I/O Write strobe (LCS1) (active-low).
HSYNC#		I/O	Horizontal sync (active-low); (5V tolerant input).
AUX2		I/O	Auxiliary port; (5V tolerant input).
IOR#	202	O	I/O Read strobe (LCS1) (active-low).
VSYNC#		I/O	Vertical sync (active-low); (5V tolerant input).
AUX3		I/O	Auxillary port; (5V tolerant input).
C2PO	203	I	Error correction flag from CD; (5V tolerant input).
AUX4		I/O	Auxiliary port; (5V tolerant input).
AUX[5:6]	204, 205	I/O	Auxiliary ports; (5V tolerant input).
IR	206	I	Infrared remote control input; (5V tolerant input).
AUX7		I/O	Auxiliary port; (5V tolerant input).
RESET#	207	I	Reset input (active-low); (5V tolerant input).

2.1 SYSTEM BLOCK DIAGRAM

A sample system block diagram for the ES66x8 Vibratto II DVD player board design is shown in the following figure:

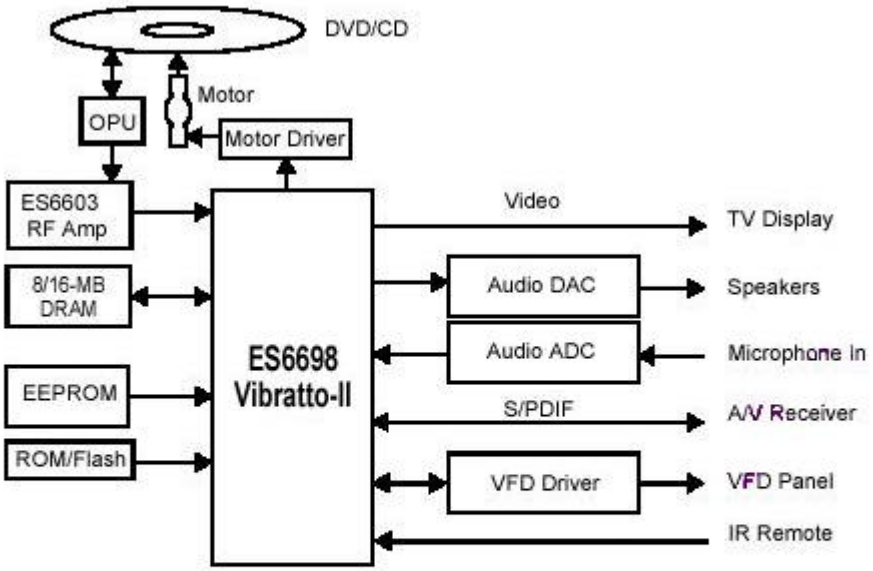


Figure 2 ES6698 Vibratto-II System Block Diagram

3. AUDIO OUTPUT

The ES66x8 supports two-channel analog audio output while ES66x8 supports six-channel analog audio output. In a system configuration with six analog outputs, the front left and right channels can be configured to provide the stereo (2 channel) outputs and Dolby Surround, or the left and right front channels for a 5.1 channel surround system.

The ES6008 also provides digital output in S/PDIF format. The board supports both optical and coaxial S/PDIF outputs.

3. AUDIO DACS

The ES66x8 supports several variations of an I^2S type bus, varying the order of the data bits (leading or no leading zero bit, left or right alignment within frame, and MSB or LSB first) is possible using the ES66x8 internal configuration registers. The I^2S format uses four stereo data lines and three clock lines. The I^2S data and clock lines can be connected directly to one or more audio DAC to generate analog audio output.

The two-channel DAC is an CS4392. The DACs support up to 192kHz sampling rate.

The outputs of the DACs are differential, not single ended so a buffering circuit is required. The buffer circuits use National LM833 op-amps to perform the low-pass filtering and the buffering.

5 VIDEO INTERFACE

5.1 Video Display Output

The video output section controls the transfer of video frames stored in memory to the internal TV encoder of the Vibratto II. The output section consists of a programmable CRT controller capable of operating either in Master or Slave mode.

The video output section features internal line buffers which allow the outgoing luminance and chrominance data to match the internal clock rates with external pixel clock rates, easily facilitating YUV4:2:2 to YUV4:2:0 component and sample conversion. A polyphase filter achieves arbitrary horizontal decimation and interpolation.

Video Bus
The video bus has 8 YUV data pins that transfer luminance and chrominance (YUV) pixels in CCIR1656 pixel format (4:2:2). In this format, there are half as many chrominance (U or V) pixels per line as luminance (Y) pixels; there are as many chrominance lines as luminance.

Video Post-Processing
The Vibratto II video post-processing circuitry provides support for the color conversion, scaling, and filtering functions through a combination of special hardware and software. Horizontal up-sampling and filtering is done with a programmable, 7-tap polyphase filter bank for accurate
non-integer interpolations. Vertical scaling is achieved by repeating and dropping lines in accordance with the applicable scaling ratio.

Video Timing
The video bus can be clocked either by double pixel clock and clock qualifier or by a single pixel clock. The double clock typically is used for TV displays, the single for computer displays.

6 SDRAM MEMORY

The memory bus interface generates all the control signals to interface with external memory. The Vibratto II supports different configurations using the memory configuration bits SDCFG[1:0] (bits 12:11), the SD8BIT bit (bit 14), and SD64M bit (bit 15) in the BUSCON_DRAM_CONTROL register. Configurations can be implemented in many ways. The following table lists the typical SDRAM configurations used by the Vibratto II.

Typical SDRAM Configurations:

Size (MB)	Bit Order				Memory Configuration
	SD64M	SD8BIT	SDCFG1	SDCFG0	
2.0	0	0	0	1	1 pc: 512Kx16x2 (16 Mb)
4.0	0	0	0	0	2 pcs: 512Kx16x2 (16 Mb)
4.0	0	1	0	1	2 pcs: 1Mx8x2 (16 Mb)
8.0	0	1	0	0	4 pcs: 1Mx8x2 (16 Mb)
8.0	1	0	X	X	1 pc: 1Mx16x4 (64 Mb)
16.0	1	0	X	X	2 pc: 1Mx16x4 (64 Mb)
16.0	1	1	X	X	2 pc: 2Mx8x4 (64 Mb)
16.0	1	1	X	X	1 pc: 2Mx16x4 (128 Mb)

The memory interface controls access to both external SDRAM or EDO memories, which can be the sole unified external read/write memory acting as program and data memory as well as various decoding and display buffers. At high clock speeds, the Vibratto II memory bus interface

has sufficient bandwidth to support the decoding and displaying of CCIR1656/601 resolution images at full frame rate.

7 FLASH MEMORY

The decoder board supports AMD class Flash memories. Currently 4 configurations are supported:

FLASH_512K_8b
FLASH_1024K_8b
FLASH_512Kx2_8b
FLASH_512Kx2_16b

The Vibratto II permits both 8- and 16-bit common memory I/O accesses with a removable storage card via the host interface.

8 SERIAL EEPROM MEMORY

An I2C serial EEPROM is used to store user configuration (i.e. language preferences, speaker setup, etc.) and software configuration.. Industry standard EEPROM range in size from 1kbit to 256kbit and share the same IC footprint and pinout. The default device is 2kbit, 256kx 8, SOIC8 SGS Thomson ST24C02M1 or equivalent.

9 AUDIO INTERFACE AUDIO SAMPLING RATE AND PLL COMPONENT CONFIGURATION

The ES66x8 Vibratto II audio mode configuration is selectable, allowing it to interface directly with low-cost audio DACs and ADCs. The audio port provides a standard I^2S interface input and output and S/PDIF (IEC958) audio output. Stereo mode is in I^2S format while six channels Dolby Digital (5.1 channel) audio output can be channeled through the S/PDIF. The S/PDIF interface consists of a bi-phase mark encoder, which has low skew. The transmit I^2S interface supports the 128, 192, 256, 384, and 512 sampling frequency formats, where sampling frequency Fs is usually 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, or 192 kHz. The audio samples for the I^2S transmit interface can be 16, 18, 20, 24, and 32-bit samples.

For Linear PCM audio stream format, the Vibratto II supports 48 kHz and 96 kHz. Dolby Digital audio only supports 48 kHz. The ES6008/18 Vibratto II incorporates a built-in programmable analog PLL in the device architecture in order to generate a master audio clock. The MCLK pin is for the audio DAC clock and can either be an output from or an input to the ES66x8 Vibratto II . Audio data out (TSD) and audio frame sync (TWS) are clocked out of the Vibratto II based on the audio transmit bit clock (TBCK). Audio receive bit clock (RBCK) is used to clock in audio data in (RSD) and audio receive frame sync (RWS).

10 FRONT PANEL

10.1 VFD CONTROLLER

The VFD controller is a PTC PT6311. This controller is not a processor, but does include a simple state machine which scans the VFD and reads the front panel button matrix. The 6311 also includes RAM so it can store the current state of all the VFD icons and segments. Therefore, the 6311 need only be accessed when the VFD status changes and when the button status is read. The ES66x8 can control this chip directly using PIO pins or can allow the front panel PIC to control the VFD.

11 MISCELLANEOUS FUNCTIONS

11.1 RESET CIRCUITRY

Two different chips are supported to provide the power-on-reset and pushbutton reset function: AAT3521 or V6300.

12 CONNECTORS

12.1 SCART CONNECTORS

Pinout of the scart connector:

1 ✍ Audio Right Out
2 ✍ Audio Right In
3 ✍ Audio Left / Monu Out
4 ✍ Audio Gnd
5 ✍ Blue Gnd
6 ✍ Audio Left / Mono In
7 ✍ Blue
8 ✍ Control Voltage
9 ✍ Green Gnd
10 ✍ Comms Data 2
11 ✍ Green
12 ✍ Comms Data 1
13 ✍ Red Gnd
14 ✍ Comms Data Gnd
15 ✍ Red
16 ✍ Fast Blanking
17 ✍ Video Gnd
18 ✍ Fast Blanking Gnd
19 ✍ Composite Video In
20 ✍ Composite Video Out
21 ✍ Shield

Some cheaper SCART cables use unshielded wires, which is just about acceptable for short cable lengths. For longer lengths, shielded coax cable become essential.

Scart Signals:

Audio signals
0.5V RMS, <1K output impedance, >10K input impedance.

Red, Green, Blue
0.7Vpp ? 2dB, 75R input and output impedance. Note that the Red connection (pin 20) can alternatively carry the

S-VHS Chrominance signal, which is 0.3V.

Composite Video / CSync
1Vpp including sync, ?2dB, 75R input and output impedance.Bandwidth = 25Hz to 4.8MHz for normal TV Video de-emphasis to CCIR 405.1 (625-line TV)

Fast Blanking
75R input and output impedance. This control voltage allows devices to over-ride the composite video input with RGB inputs, for example when inserting closed caption text. It is called fast because this can be done at the same speeds as other video signals, which is why it requires the same 75R impedances.

0 to 0.4V: TV is driven by the composite video input signal (pin 19). Left unconnected, it is pulled to 0V by its 75R termination.

1V to 3V: the TV is driven by the signals Red, Green, Blue and composite sync. The latter is sent to the TV on pin 19. This signal is useful when using a TV to display the RGB output of devices such as home computers with TV-compatible frame rates. Tying the signal to 5V via 100R forms a potential divider with the 75R termination, holding the signal at around 2V. Alternatively, if a TTL level (0 to 5V) negative sync pulse is available, this will be high during the display periods, so this can drive the blanking signal via a suitable resistor.

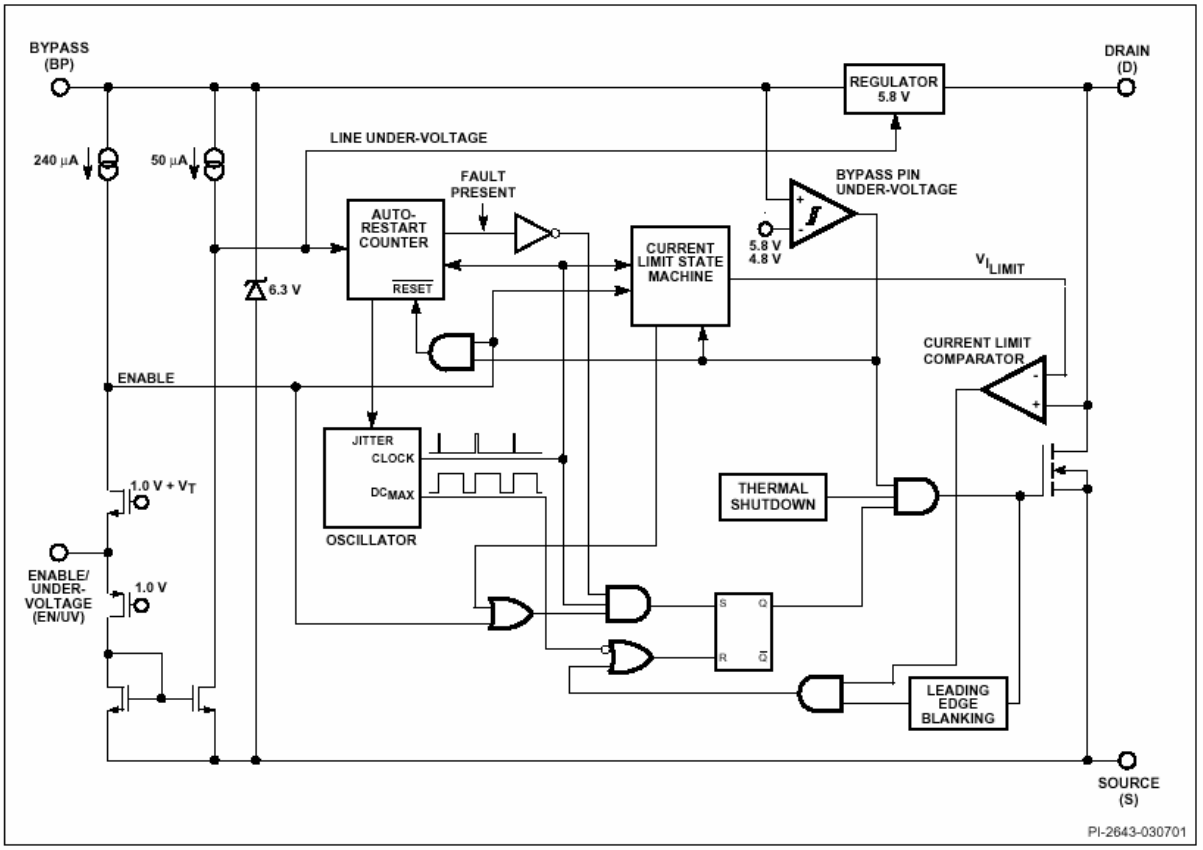
Control Voltage

0 to 2V = TV, Normal.
5 to 8V = TV wide screen
9.5 to 12V = AV mode

13. CIRCUIT DESCRIPTION

13.1 POWER SUPPLY:

- Socket PL2 is the 220VAC input.
- Socket PL3 is used for the power button on the front panel.
- 3.15A fuse F1 is used to protect the device against short circuit.
- Voltage is rectified by using diodes D1, D2, D3 and D4. Using capacitor C33 (47?f) a DC voltage is produced. (310- 320VDC).
- The current in the primary side of the transformer TR2 comes to the SMPS IC (TNY267P). It has a built-in oscillator, over current and thermal protection circuitry and runs at 133kHz. It starts with the current from the primary side of the transformer and follows the current from the feedback winding.
- Voltages on the secondary side are as follows: 12 Volts at pin11 at C42, 5 Volts at C40,3.3 Volts at C38, -22Volts at C44,-12 Volts at D22.
- D14 TL431 is a constant current regulator. TL431 watches the 5 volts and supplies the required current to IC2. There are a LED and a photo transistor in IC2. The LED inside the IC2 transmits the value of the current from D25 to phototransistor. Depending on the current gain of the phototransistor IC3 keeps the voltage on the 5-volt-winding constant.
- –22 Volts is used to feed the VFD (Vacuum Fluorescent Display) driver IC on the front panel.



Functional Block Diagram of Switcher

13.2 FRONT PANEL:

- All the functions on the front panel are controlled by U1 (ES66x8) on the mainboard.
- U1 sends the commands to IC2 PT6311 via socket J2 (pins 3,4 and 5).
- There are 48 keys scanning function, 5 LED outputs, 1 Stand-by output and VFD drivers on PT6311.
- Vacuum fluorescent display is specially designed for DVD.
- The scanned keys are transmitted via PT6311 to U1 on the mainboard.
- IR remote control receiver module sends the commands from the remote control directly to U1.

13.3 BACK PANEL:

- There are 1 SCART connector (con24), 2 pieces RCA audio jacks for audio output, 1 coaxial digital audio output and 1 laser digital audio output on the back panel.
- MOFT3C2 is used for laser output.
- Left and right audio outputs are on RCA Conn 6.
- LUMA and CHROMA signals of S-Video are transmitted to P1 via transistors Q39 and Q37 respectively.

CD Update Procedure of 4250D

1. Download the update file from the convenient link according to your default language choice.

2. While there is no CD in the DVD (No Disc Mode) , press “Menu 1 3 5 7” buttons on the remote control in order to reach the Service Menu of DVD Player:

   2.1. Note the software version described as “b.xx “ to be able to compare the sw. Version after update process.

3. Copy the update file to the desktop and rename it according to the update file name in the hidden menu of the device.
   For example If C2M1AS__ is written then rename it like C2M1AS__.rom
   If P6M1AS__ is written then rename it like P6M1AS__.rom

   (If you receive the update file already renamed (with addition of .rom) from the customer technical support department by giving the SAP code of the product then burn the already renamed file with nero program as it is shown below.)

4. Burn the renamed files by Nero program with below set up.

5. After burning process is completed, place the update CD into the DVD tray and press play button.

6. Wait to see the update process steps as shown below. When the sw. Update is completed unit will switch itself to standby mode.

7. Finally, press the eject button and take out the update CD while DVD Player remains at stand by Mode.

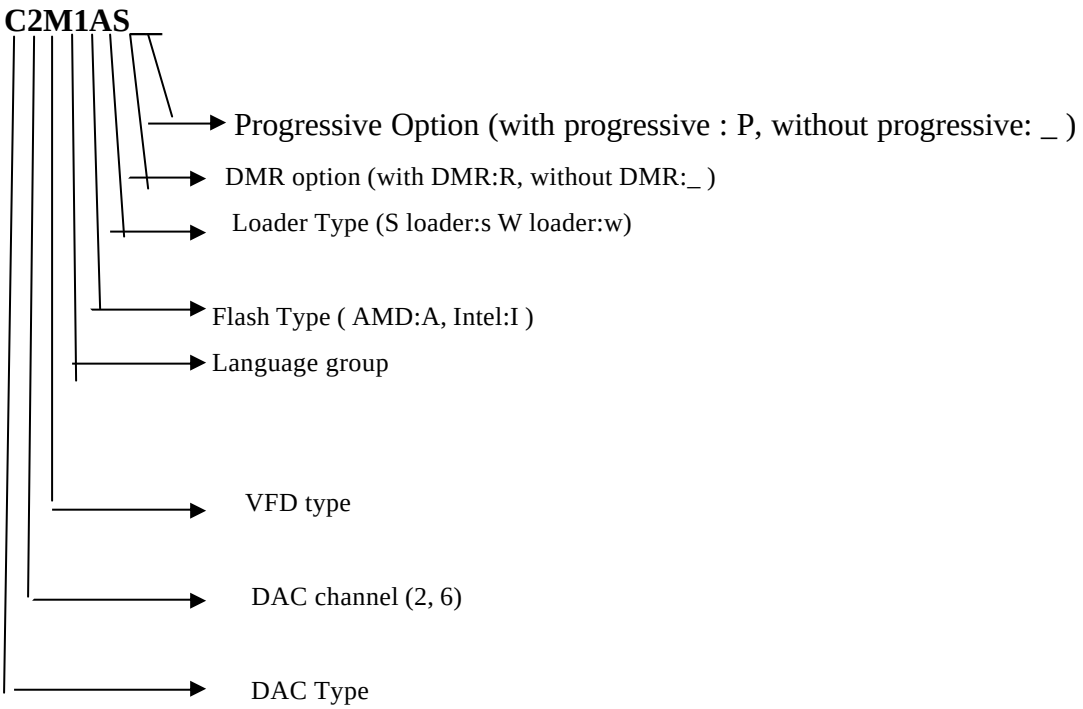
8. Updating process has been completed. To check whether it is updated correctly or not, repeat the first step for comparing software version

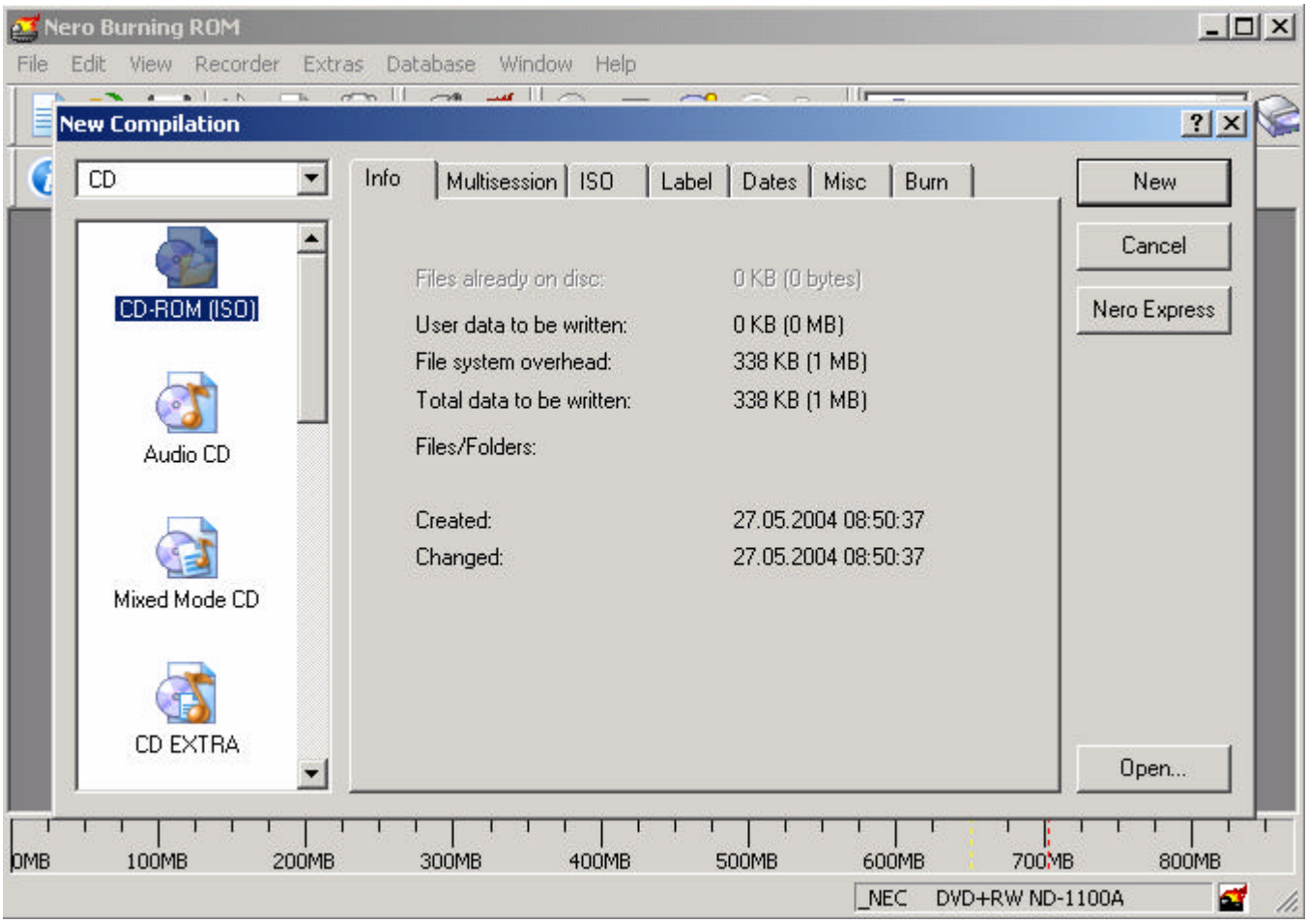
9. If the previous and letter names are different, CD is update has completed successfully. If the name remains same than go through the steps from the beginning.

IMPORTANT NOTE: If the AC source breaks down while the updating the unit (main board) will be totally out of order. This kind of units/boards is out of Warranty.

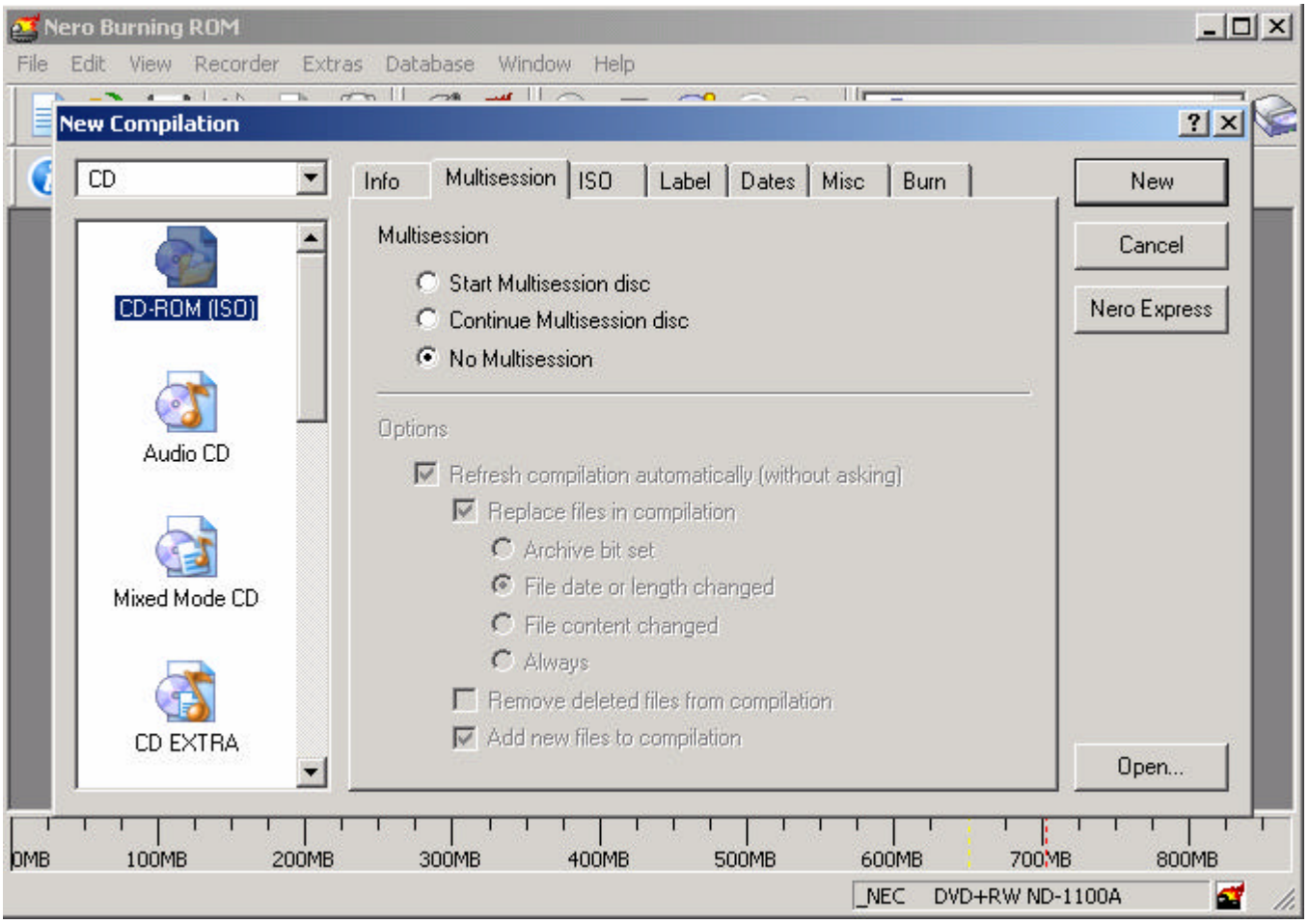
Brief Information of Naming the File

Software version differs from each other depending on front models. 23xx and 24xx are called Old VFD and 25xx and 26xx are called Mini VFD. Each character in the file name is an abbreviation of a description as illustrated below.

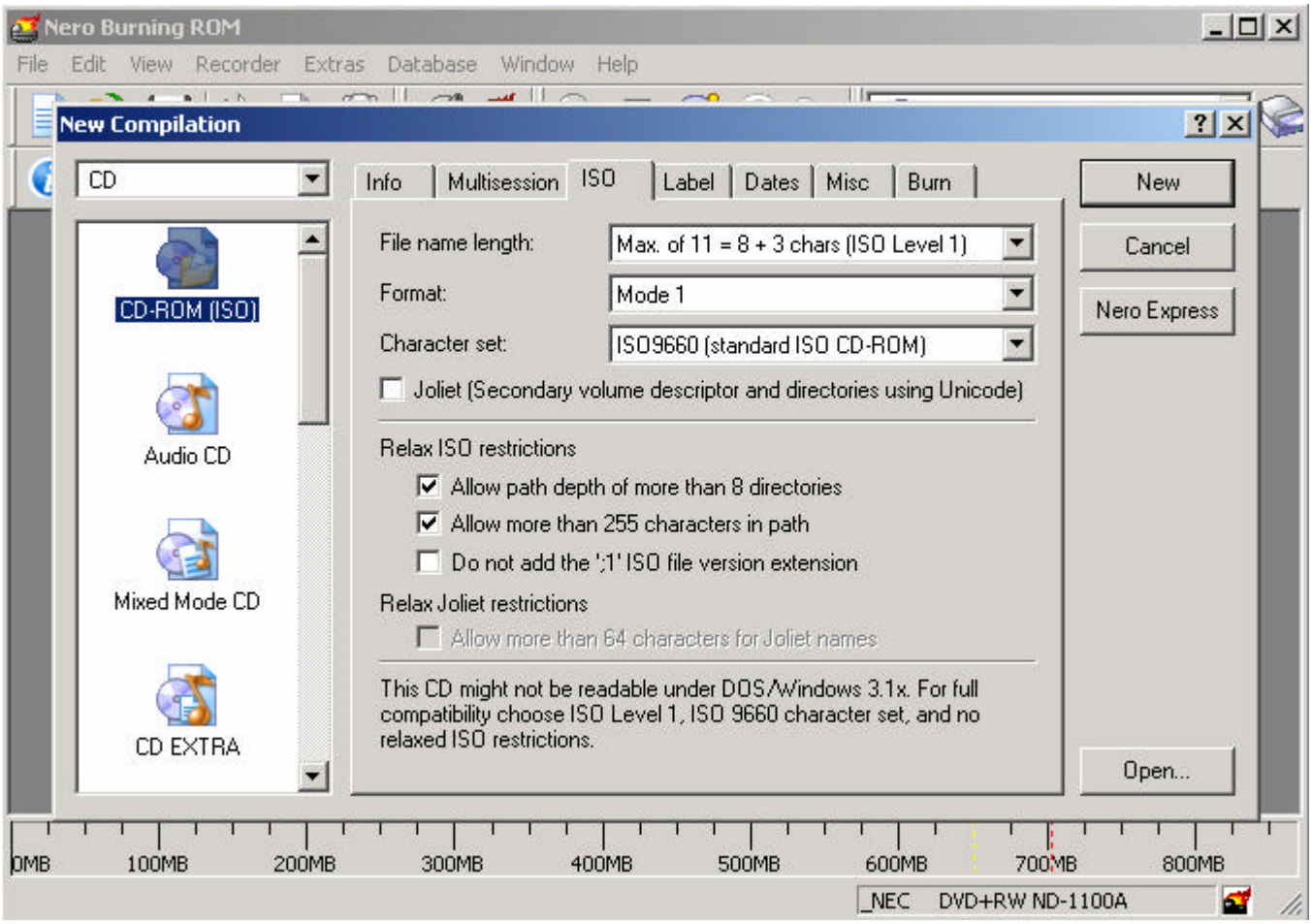




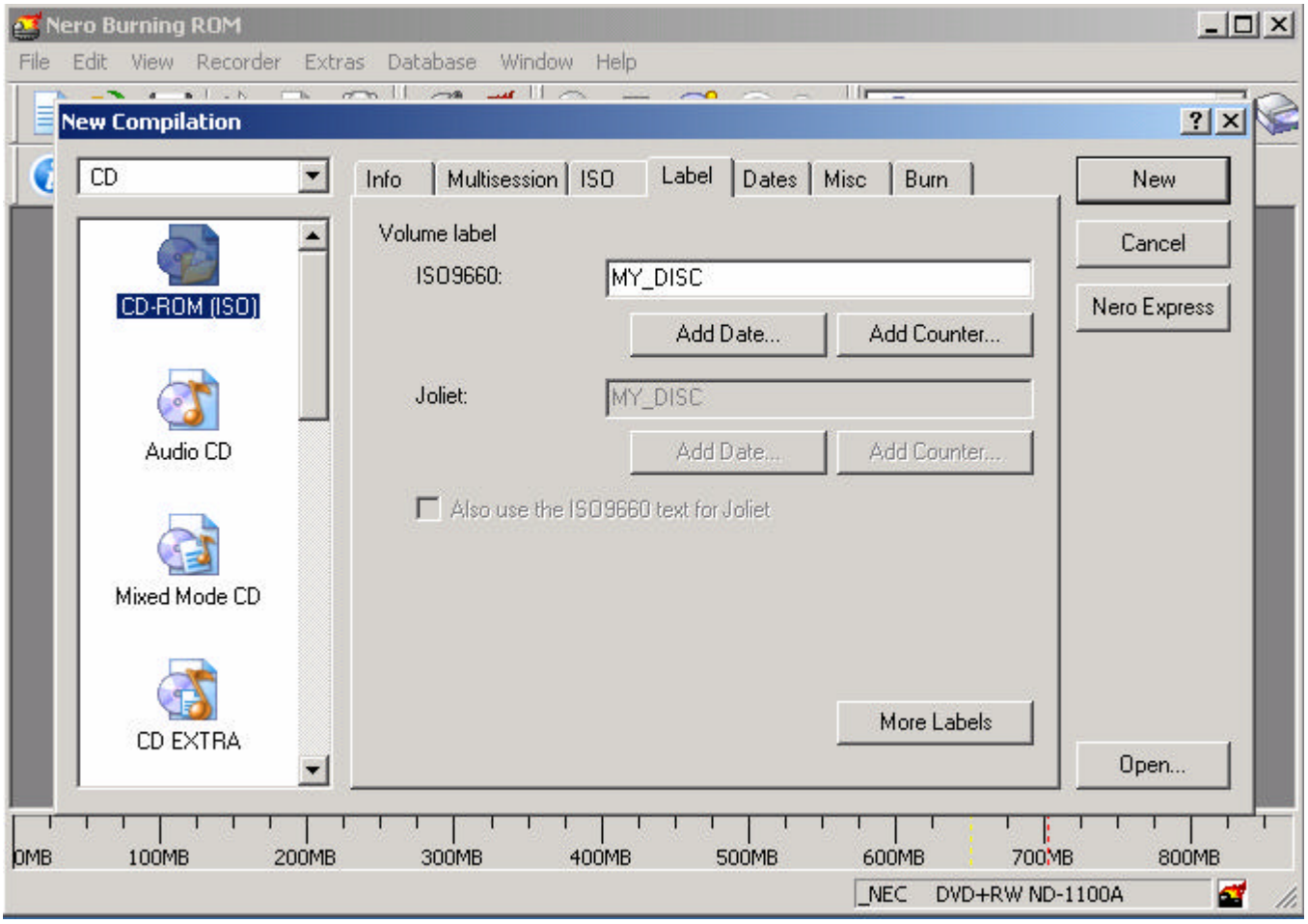
Pay attention the left side. Select **CD and CD_ROM (ISO)** on the upper left side of screen

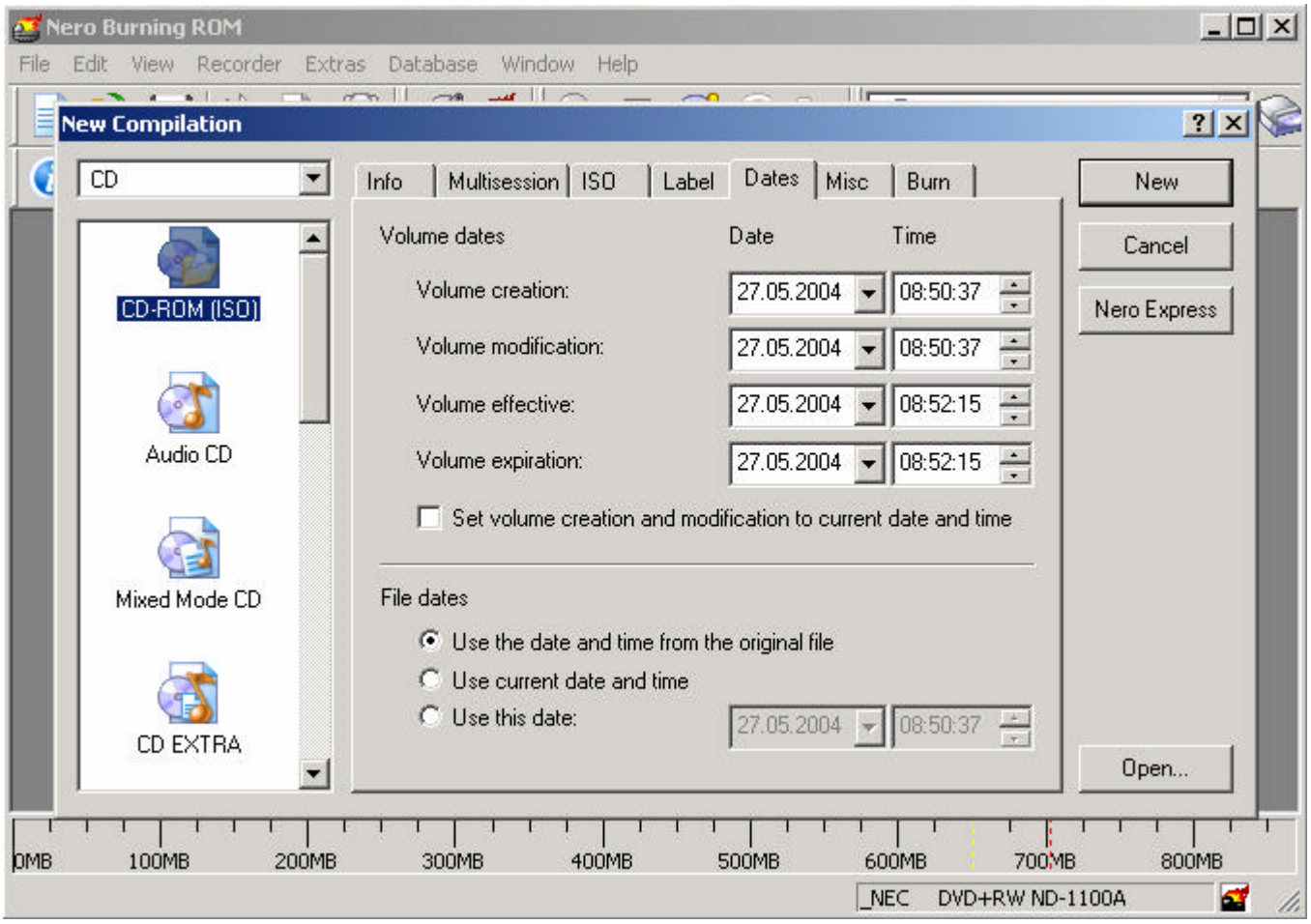


Select **No Multisession**

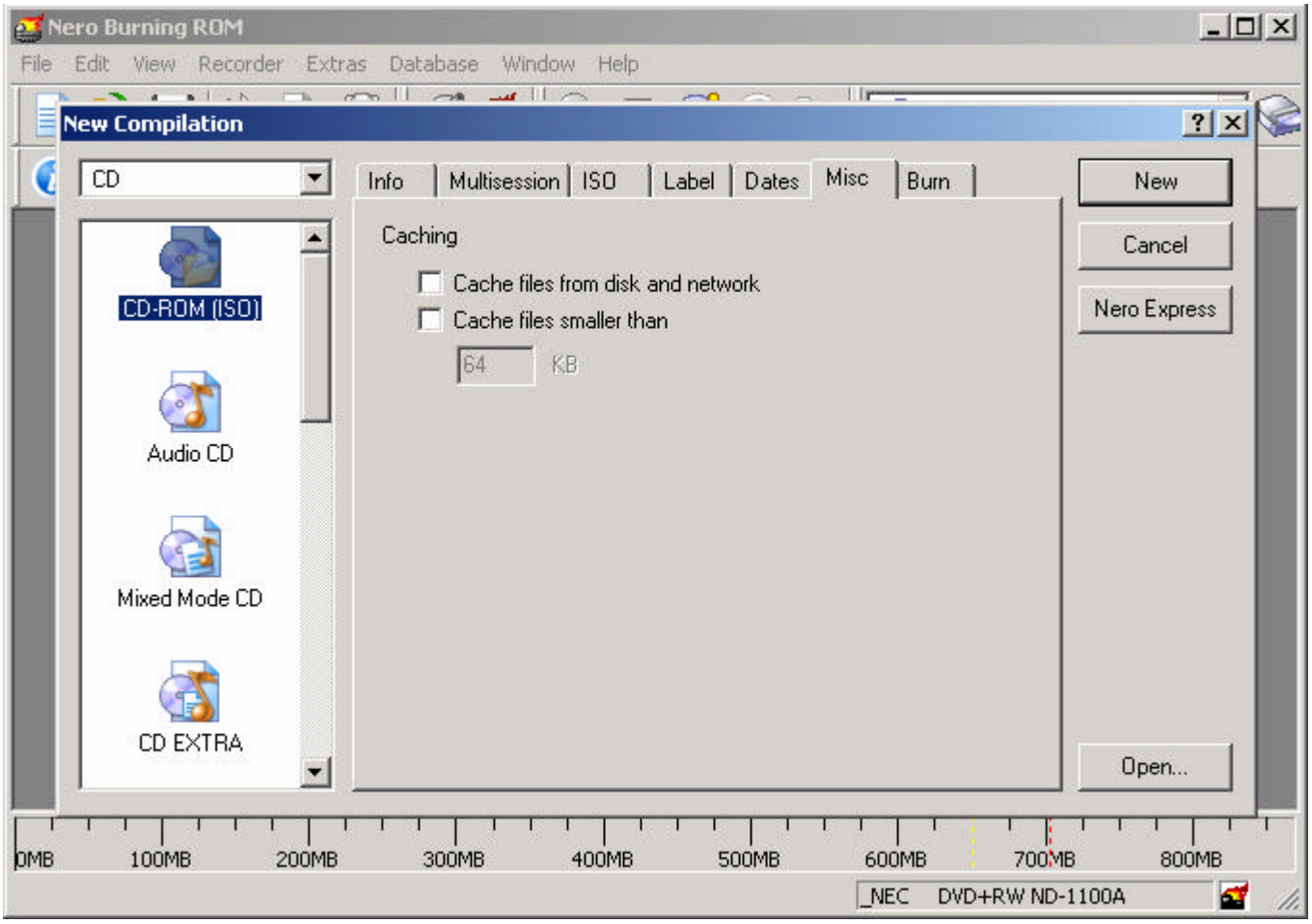


Format is **Mode 1**

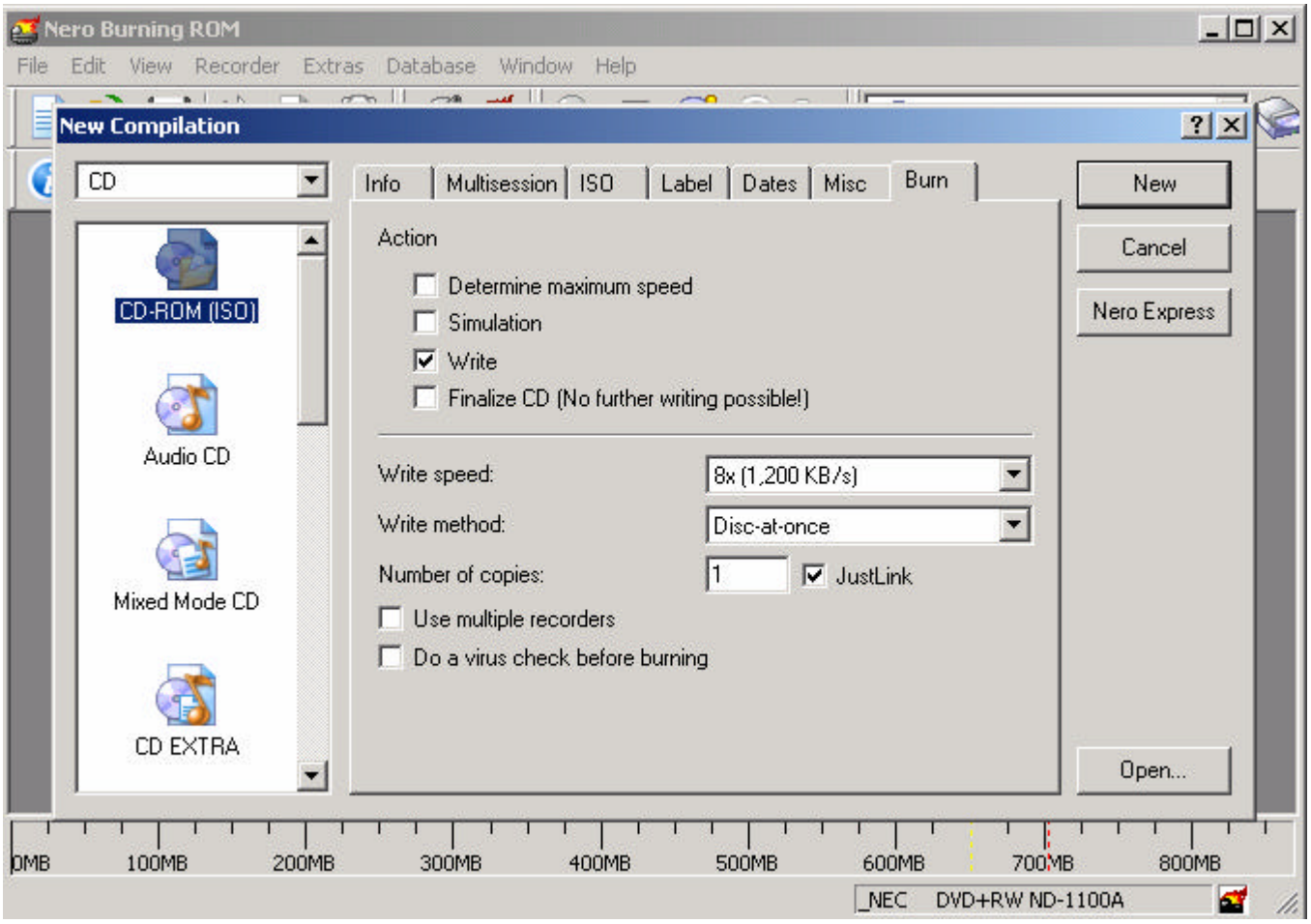

Nero Burning ROM
File Edit View Recorder Extras Database Window Help
New Compilation
CD
CD-ROM (ISO)
Audio CD
Mixed Mode CD
CD EXTRA
Info Multisession ISO Label Dates Misc Burn
Volume label
ISO9660: MY_DISC
Add Date... Add Counter...
Joliet: MY_DISC
Add Date... Add Counter...
Also use the ISO9660 text for Joliet
More Labels
New
Cancel
Nero Express
Open...
0MB 100MB 200MB 300MB 400MB 500MB 600MB 700MB 800MB
_NEC DVD+RW ND-1100A



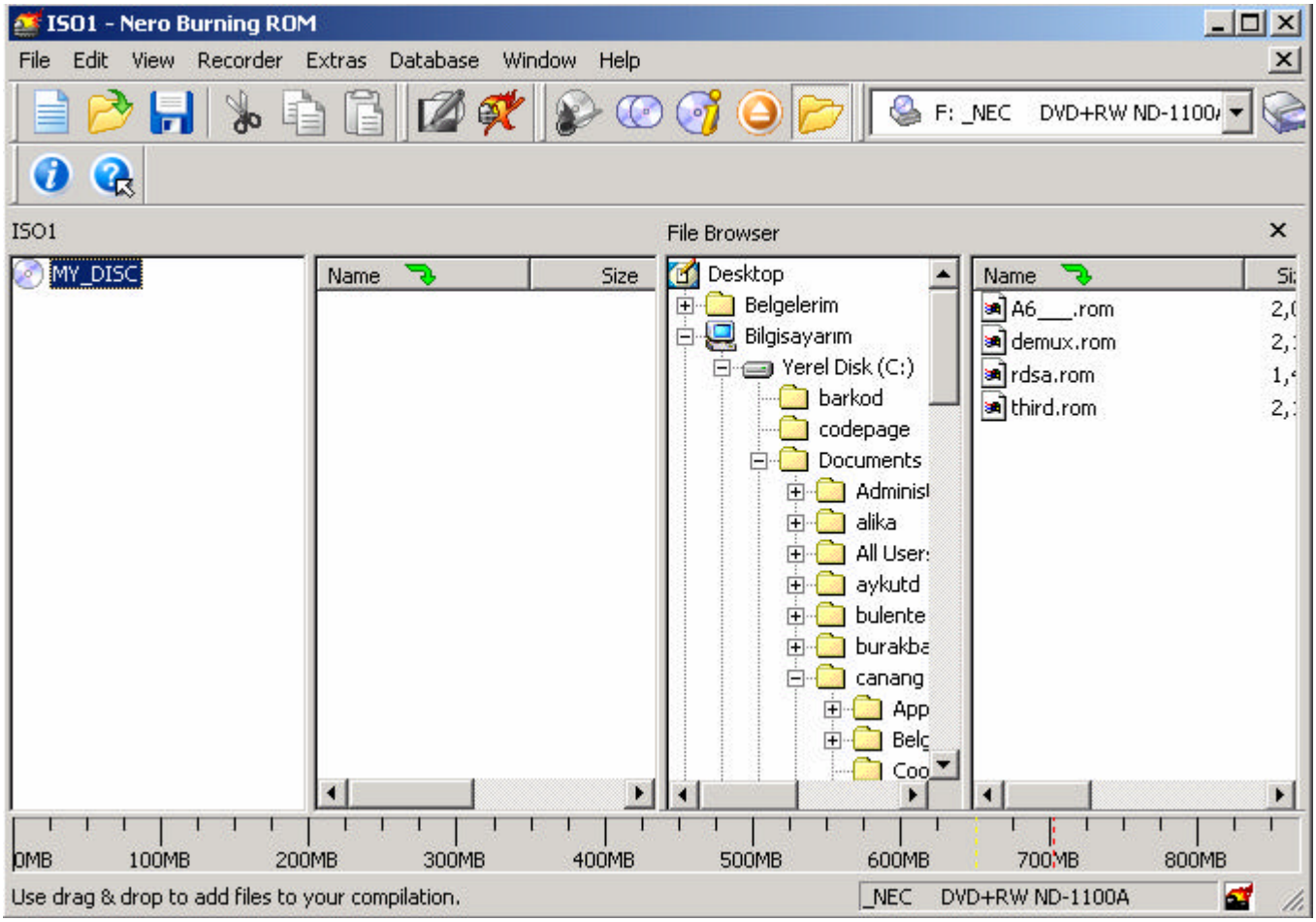
Leave the dates as it is



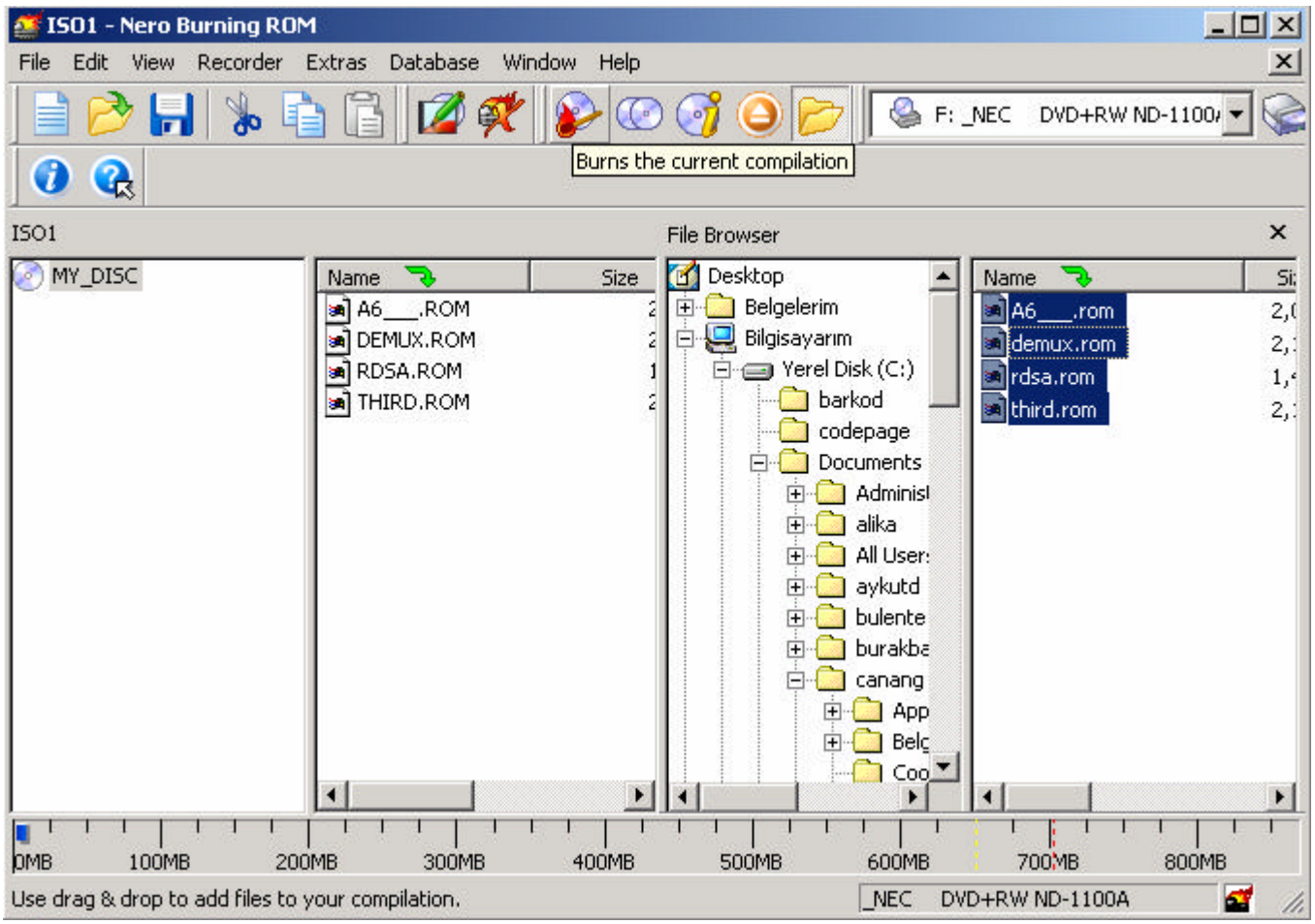
Leave it as it is



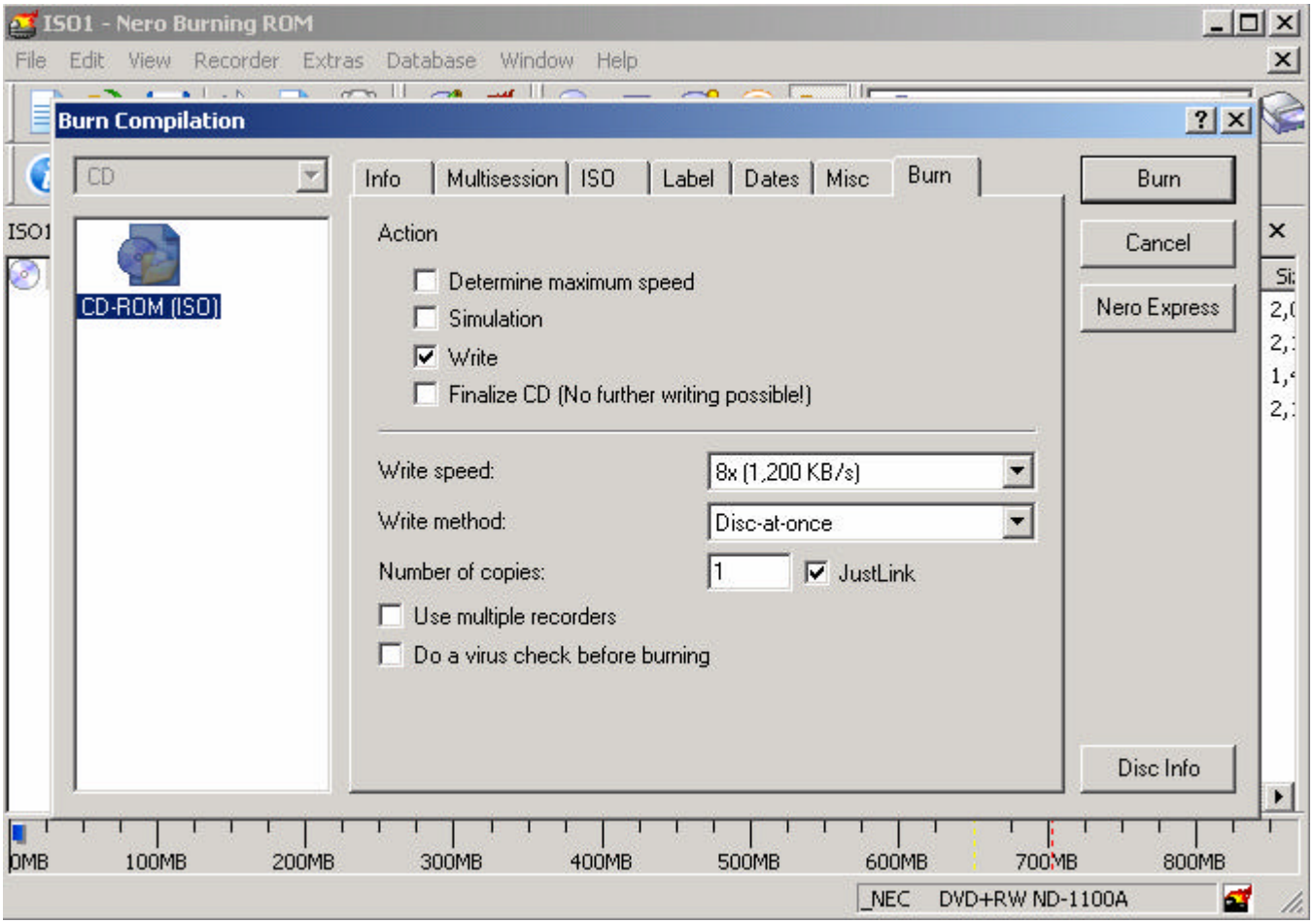
Click the “New” on the upper right corner of the screen



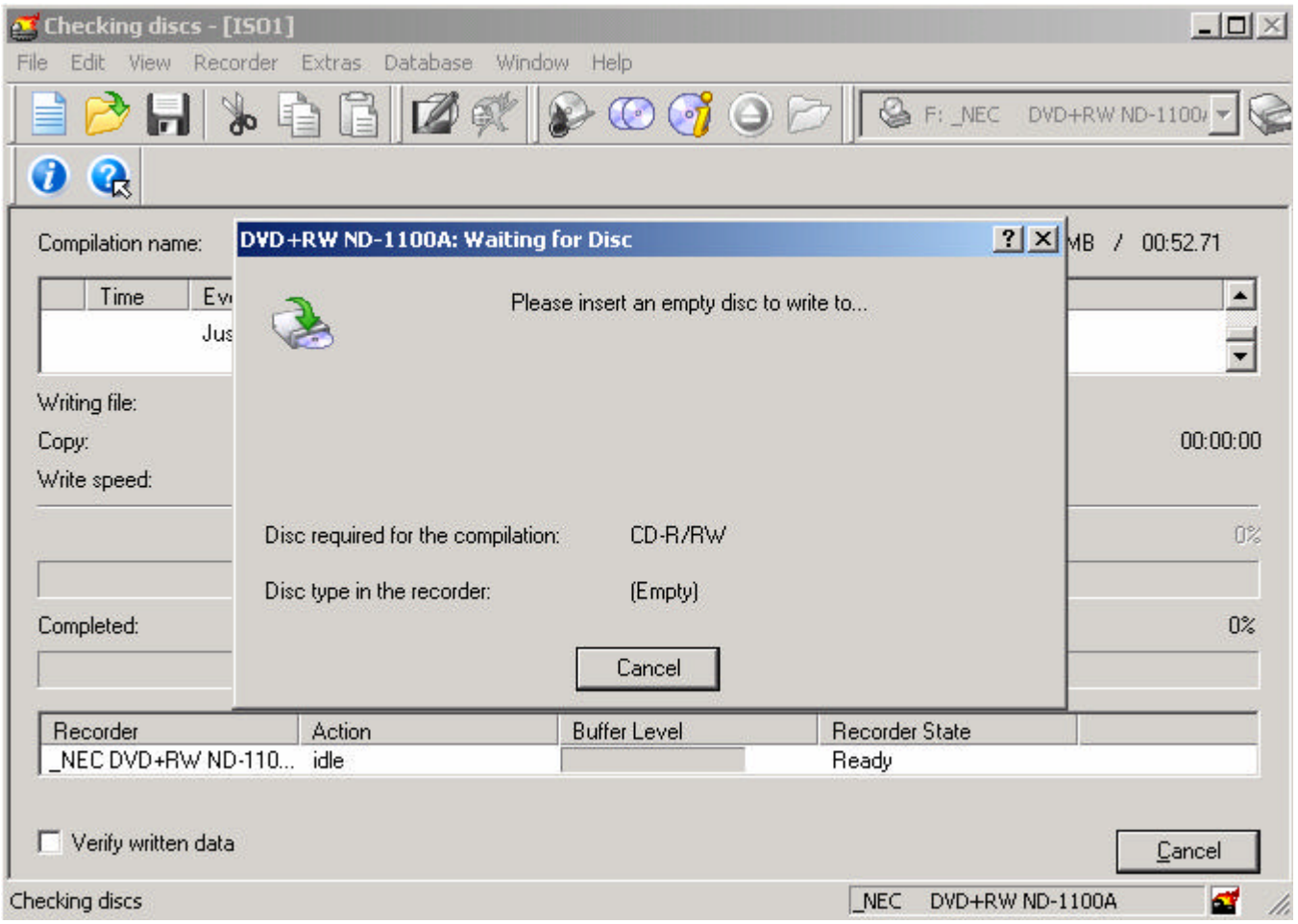
Select your file from file browser then you will see your file in the “Name” section on the right side and then copy the files to under “Name” section on the left side.(this is just an example you will see your file name when you are doing this process)



Click the “Burns the current compilation”



Then you will see this screen and click the “Burn” on the right upper side of screen



You will see this screen and tray will open itself on computer ,then place the CD in CD-ROM
And it will start writing. At the end you will see “burn complited”

.

Vibratto-II

PLL3	CLK SOURCE
1	DCLK INPUT
0	CRSTAL OSC

PLL2	PLL1	PLL0	MULTI DEFAULT	MULTI S-CHIP	Frequency DEFAULT	Frequency S-CHIP
0	0	0	4.25	4.5	114.75	121.5
0	0	1	reserved	5	NA	135
0	1	0	bypass	bypass	27	NA
0	1	1	3.75	4	101.25	108
1	0	0	4.5	4.25	121.5	114.75
1	0	1	reserved	4.75	NA	128.25
1	1	0	3.5	5.5	94.5	148.5
1	1	1	4	6	108	162

VIDEO OUTPUT TABLE

	CVBS + S-VIDEO or CVBS + YUV	CVBS + YUV	S-VIDEO + RGB	CVBS + RGB
VDAC	CVBS	CVBS	Y	CVBS
YDAC	Y	Y	G	G
CDAC	V	V	R	R
UDAC	U	U	B	B
FDAC	C	CVBS	C	CVBS

SERVO MCU DEBUG HEADER

RS232 CONNECTOR 2.54MM

SERIAL EEPROM

4Mx16 SDRAM (9ns)

32/64MBIT SDRAM

EM-MARIN RESET IC

U10	R36	R37
AAT3521	OPEN	0
V6300	0	OPEN

INSTALL	REMOVE	TYPE
R34, R68	R32, R35	EPROM
R32, R35	R34, R68	FLASH

4-PIN EXTENSION FOR ROM EMULATOR INTERFACE

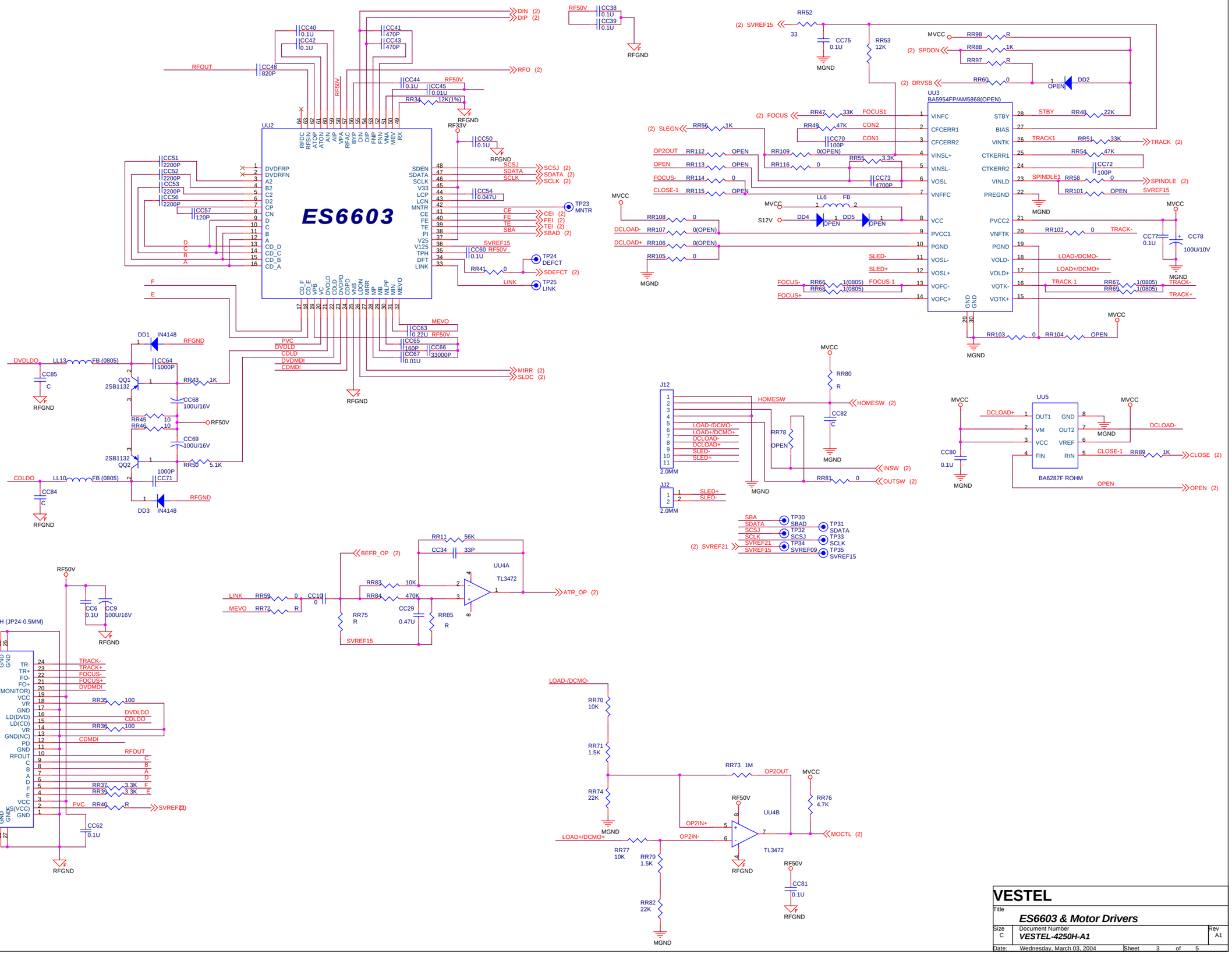
	AM5868	BA6954
CC28	7.5nF	0.015U

VESTEL

Title: Vibratto-II ES66X8

Size: C | Document Number: VESTEL-4250H-A1 | Rev: A1

Date: Wednesday, March 03, 2004 | Sheet 2 of 5



VESTEL		
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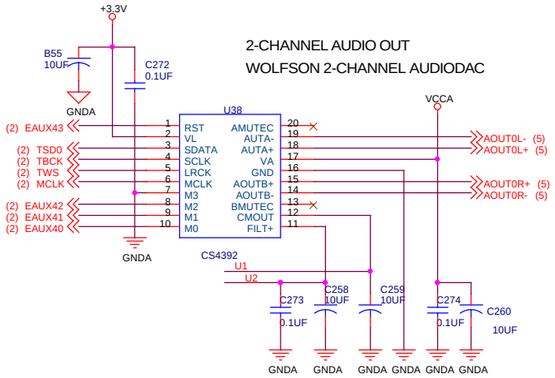
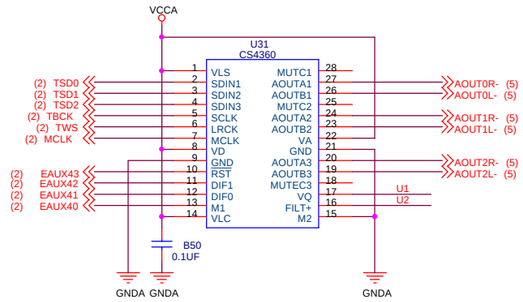
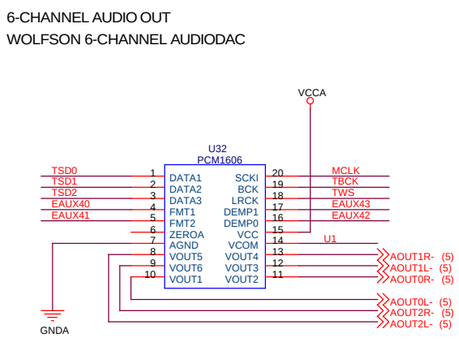
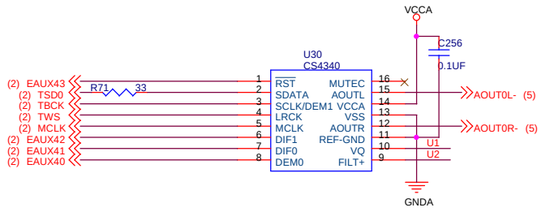
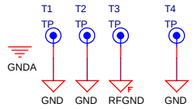
Size C	Document Number ***VESTEL-4250H-A1***	Rev A1
Date: Wednesday, March 03, 2004	Sheet 3 of 5	

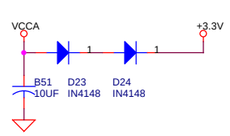


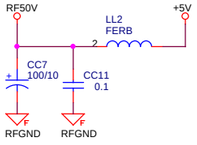


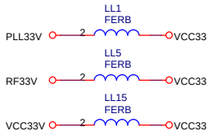


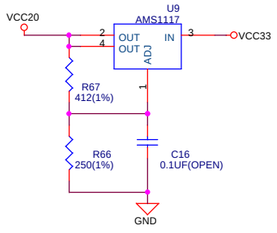


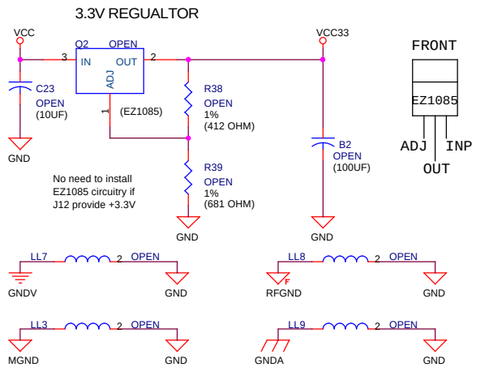


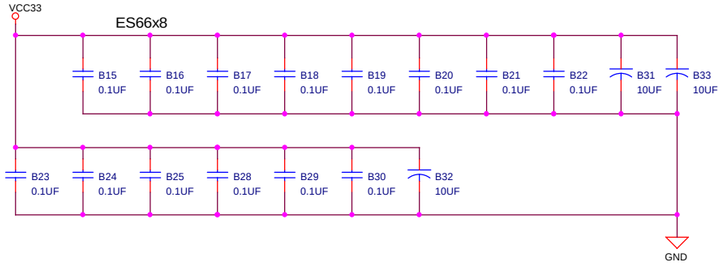


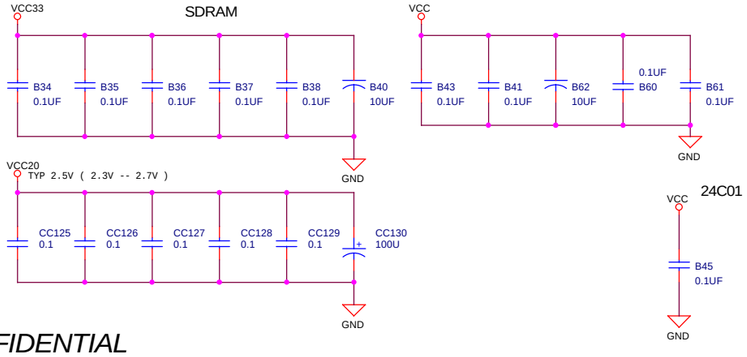


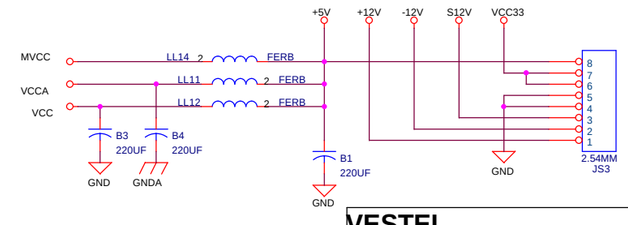












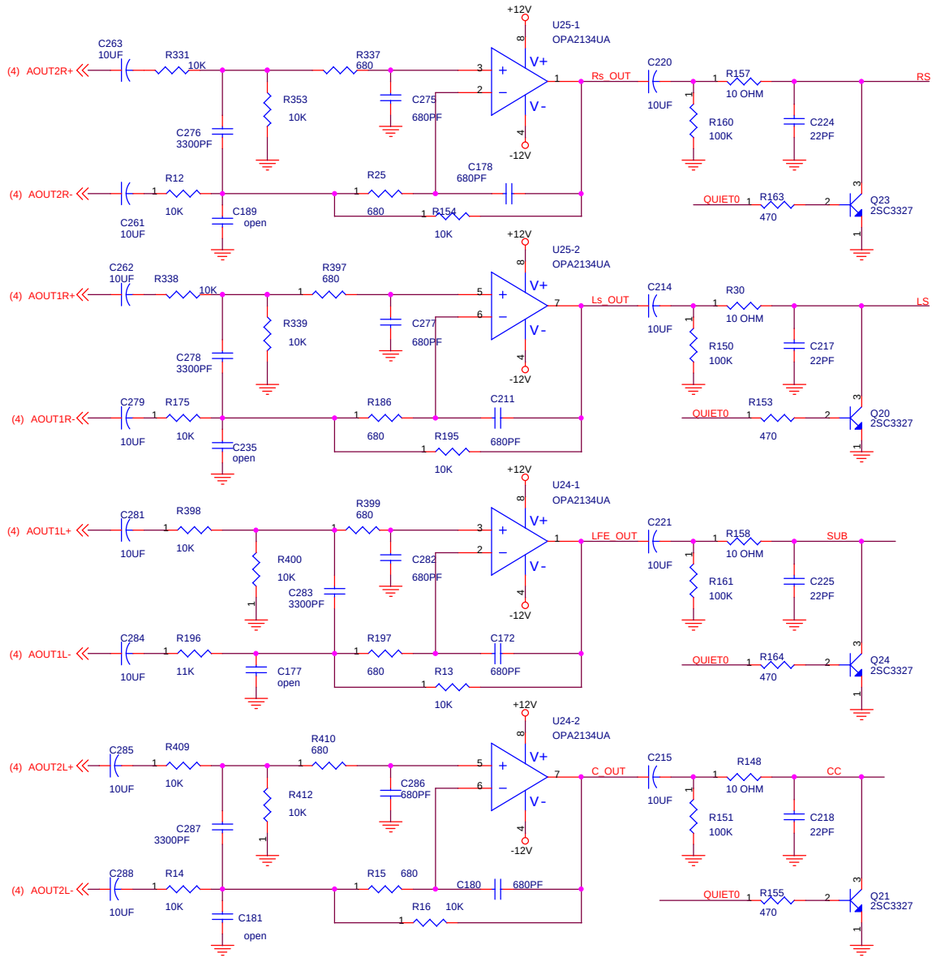
ESS CONFIDENTIAL

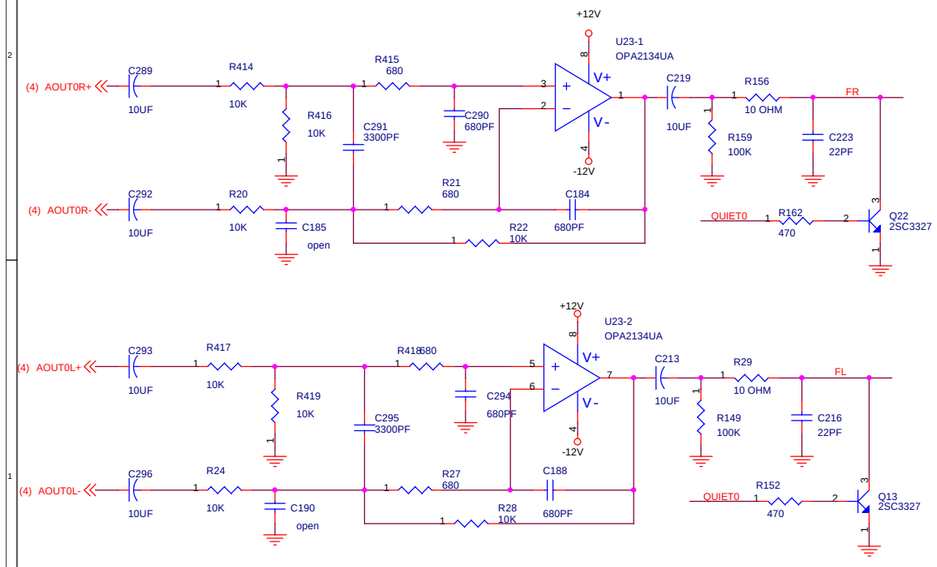
VESTEL

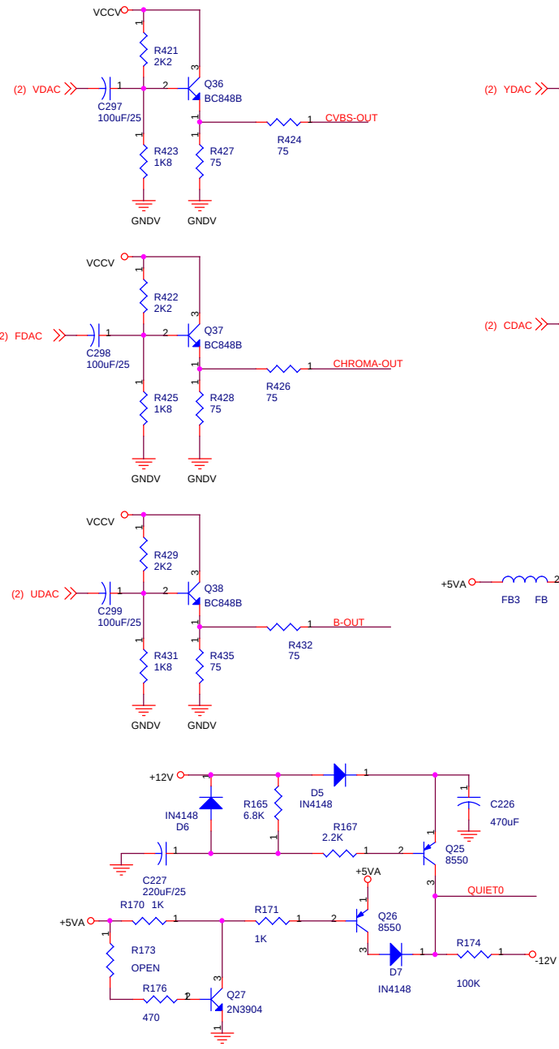
Title: ***MISC***

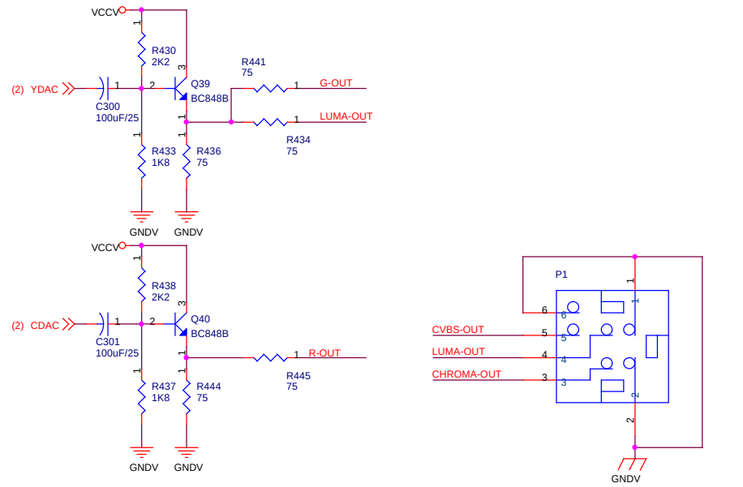
Size: C | Document Number: ***VESTEL-4250H-A1*** | Rev: A1

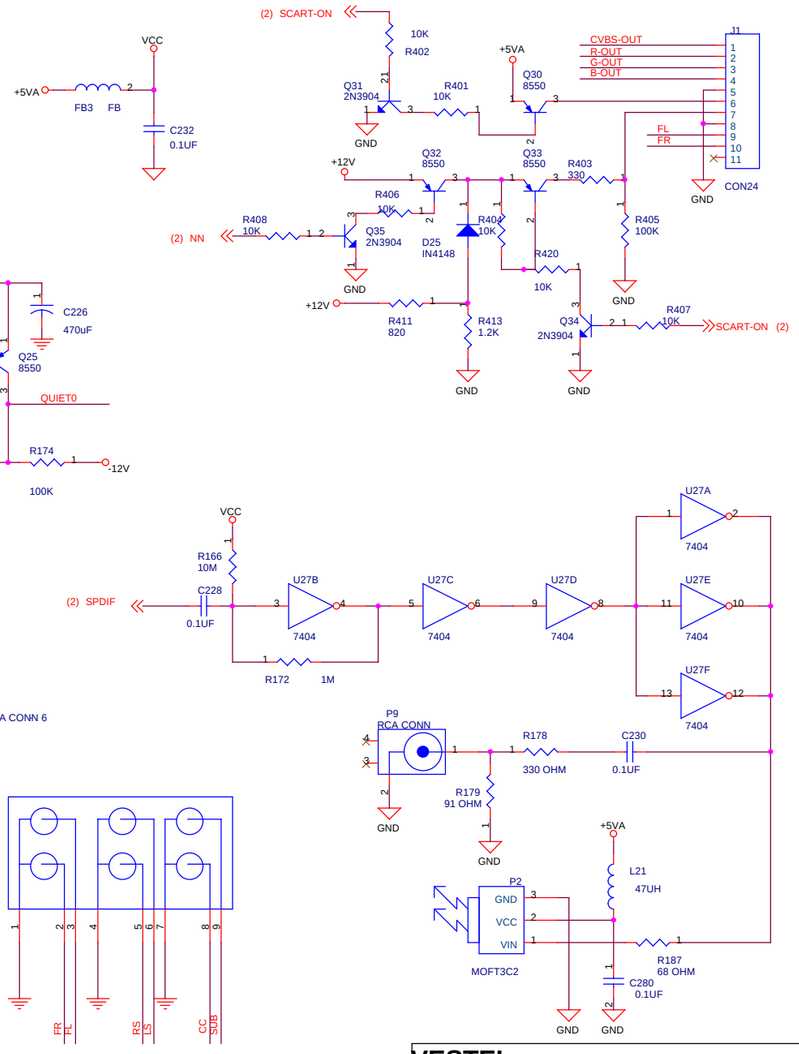
Date: Wednesday, March 03, 2004 | Sheet 4 of 5

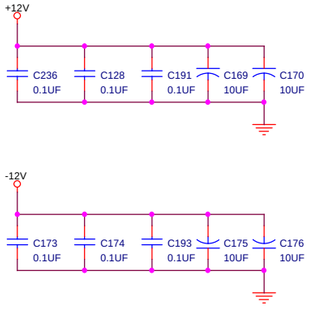




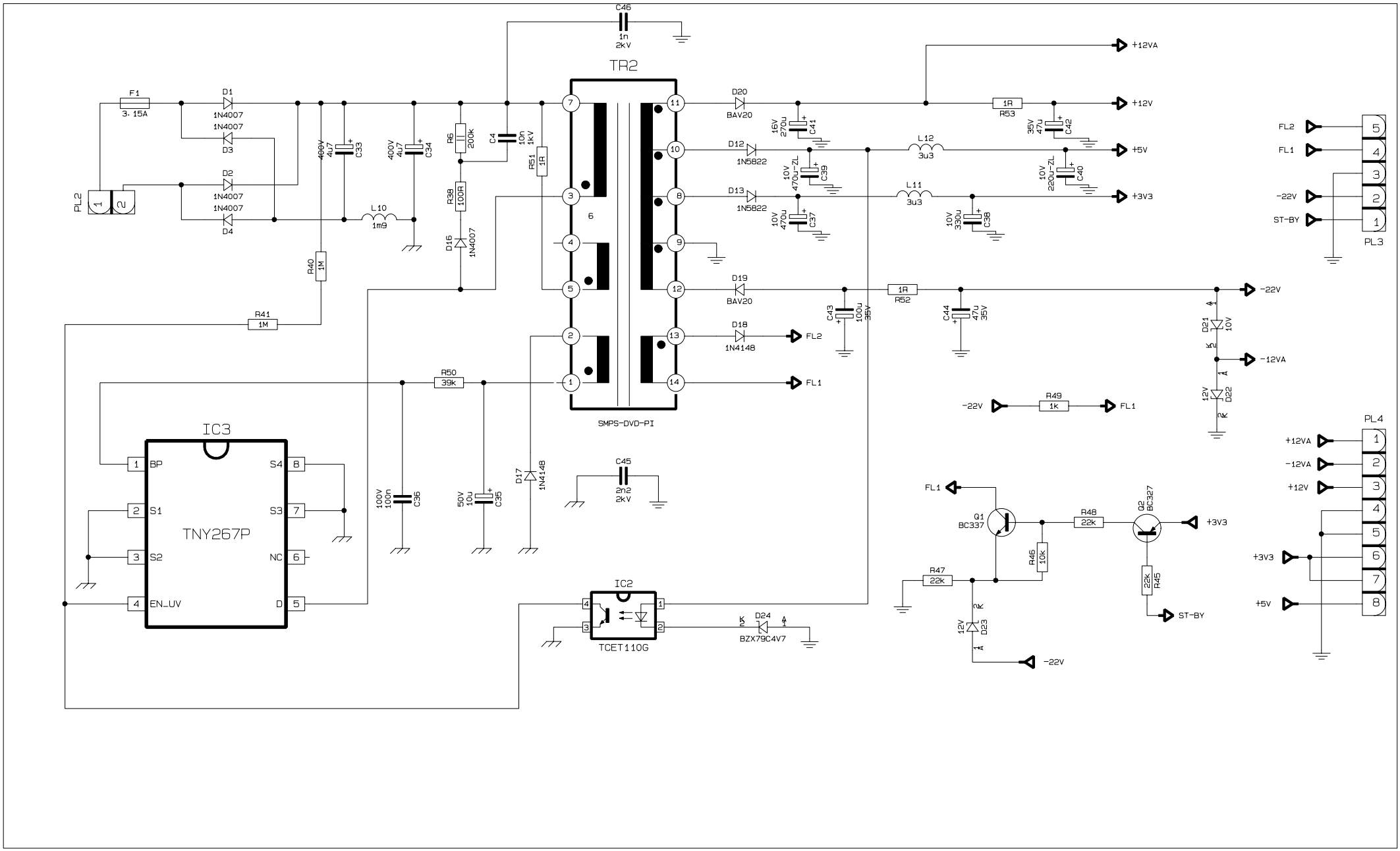


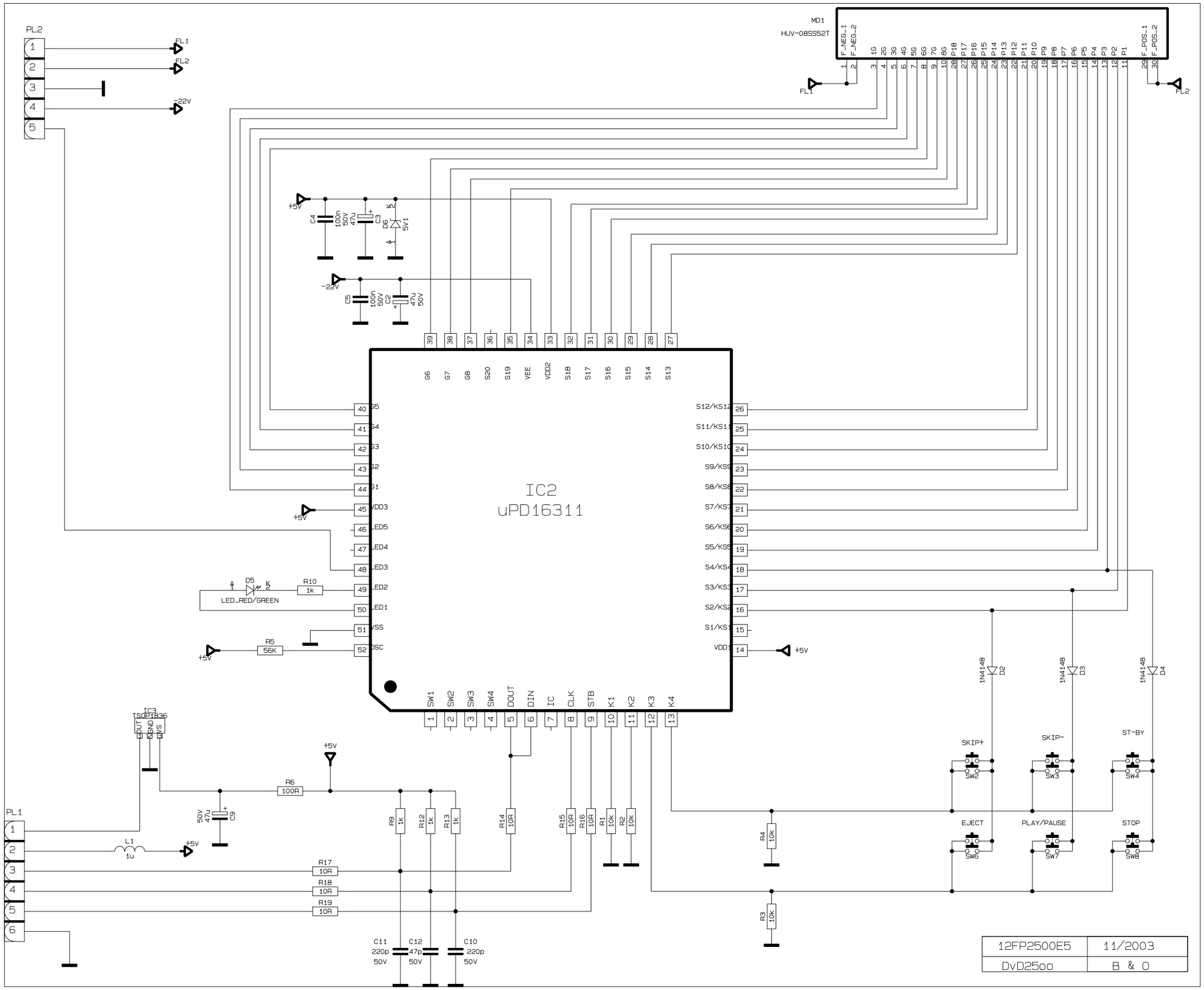






VESTEL			
Title	OUTPUT		
Size C	Document Number VESTEL-4250H-A1		Rev A1
Date: Wednesday, March 03, 2004	Sheet 5 of 5		


TR2
SMPS-DVD-PI
IC3
TNY267P
IC2
TCET110G
PL2
PL3
PL4
F1
3. 15A
D1
1N4007
D2
1N4007
D3
1N4007
D4
1N4007
L10
1mH
L11
3u3
L12
3u3
R6
200k
R38
100R
R40
1M
R41
1M
R51
1R
R52
1R
R53
1R
R46
10k
R47
22k
R48
22k
R49
1k
R50
39k
R45
22k
C4
10n
1kV
C33
400V
4u7
C34
400V
4u7
C35
50V
10u
C36
100V
100n
C37
10V
470u
C38
10V
330u
C39
10V
470u-ZL
C40
10V
220u-ZL
C41
16V
270u
C42
35V
47u
C43
100u
35V
C44
47u
35V
C45
2n2
2kV
C46
1n
2kV
D12
1N5822
D13
1N5822
D16
1N4007
D17
1N4148
D18
1N4148
D19
BAV20
D20
BAV20
D21
10V
D22
12V
D23
12V
D24
BZX79C4V7
Q1
BC337
Q2
BC327
+12VA
+12V
+5V
+3V3
-22V
-12VA
FL1
FL2
ST-BY


PL2
FL1
FL2
-22V
MD1
HUV-0BSS52T
F_NEG-1
F_NEG-2
F_POS-1
F_POS-2
+5V
C4
100n
50V
C3
47u
D6
5V1
-22V
C5
100n
50V
C2
47u
50V
IC2
uPD16311
LED_RED/GREEN
D5
R10
1k
R5
56K
VDD2
VEE
VSS
VDD3
LED5
LED4
LED3
LED2
LED1
OSC
G5
G4
G3
G2
G1
S20
S19
S18
S17
S16
S15
S14
S13
S12/KS12
S11/KS11
S10/KS10
S9/KS9
S8/KS8
S7/KS7
S6/KS6
S5/KS5
S4/KS4
S3/KS3
S2/KS2
S1/KS1
SW1
SW2
SW3
SW4
DOUT
DIN
IC
CLK
STB
K1
K2
K3
K4
1N4148
D2
D3
D4
SKIP+
SKIP-
ST-BY
SW2
SW3
SW4
EJECT
PLAY/PAUSE
STOP
SW6
SW7
SW8
IC3
TSOP1836
OUT
GND
VS
R6
100R
C9
50V
47u
PL1
L1
1u
R17
10R
R18
10R
R19
10R
R9
1k
R12
1k
R13
1k
R14
10R
R15
10R
R16
10R
R1
10k
R2
10k
R4
10k
R3
10k
C11
220p
50V
C12
47p
50V
C10
220p
50V
12FP2500E5
11/2003
DvD2500
B & O