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Service
Service



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Service Manual



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PHILIPS

1. Technical Specifications and Connection Facilities

1.1 General:

Mains voltage	: 220V-240V (198 - 264V AC) for Europe/Asia
Mains frequency	: 50 Hz - 60Hz
Power consumption mains	: 32 W
Power consumption standby	: < 7 W
Power consumption low power stand-by	: < 3 W

1.2 RF Tuner

Test equipment: Fluke 54200 TV Signal generator
 Test streams: PAL BG Philips Standard test pattern

1.2.1 System:

PAL B/G, PAL D/K, SECAM L/L', PAL I

1.2.2 RF - Loop Through:

Frequency range	: 45 MHz - 860 MHz
Gain: (ANT IN - ANT OUT)	: -4 dB \pm 2 dB

1.2.3 Radio Interference:

input voltage /3 tone method (+40 dB min)	: typ. 80 dB μ V at 75 Ω
---	-------------------------------------

1.2.4 Receiver:

PLL tuning with AFC for optimum reception

Frequency range:	: 45.25 MHz - 860 MHz
Sensitivity at 40 dB S/N	: \geq 60dB μ V at 75 Ω (video unweighted)

1.2.5 Video Performance:

Channel 25 / 503,25 MHz,
 Test pattern: PAL BG PHILIPS standard test pattern,
 RF Level 74 dBV
 Measured on SCART 1

Frequency response:	: 1 MHz - 4.00 MHz \pm 2 dB
Group delay (0.1 MHz - 4.4 MHz)	: 0 nsec \pm 30 nsec

1.2.6 Audio Performance:

Audio Performance Analogue - HiFi:

Frequency response at SCART 1 (L+R) output:	: 40 Hz - 15 kHz / \pm 1.5 dB
---	---------------------------------

S/N according to DIN 45405, 7, 1967 and PHILIPS standard test pattern video signal:	: -50 dB unweighted
Harmonic distortion (1 kHz, \pm 25 kHz deviation):	: 0.5 %

Audio Performance NICAM:

Frequency response at SCART 1(L+R) output:	: 40 Hz - 15 kHz \pm 1.5 dB
--	-------------------------------

S/N according to DIN 45405, 7, 1967 and PHILIPS standard test pattern video signal:	: -60 dB unweighted
Harmonic distortion (1 kHz):	: 0.1 %

1.2.7 Tuning

Automatic Search Tuning

scanning time without antenna	: 2.5 min. PAL
stop level (vision carrier)	: 75 V, 75
Maximum tuning error of a recalled program	: \pm 62.5 kHz
Maximum tuning error during operation	: \pm 100 kHz

Tuning Principle

automatic B,G, I, DK and L/L' detection
 manual selection in "STORE" mode

1.3 Analogue Inputs

1.3.1 SCART 1 (Connected to TV)

Pin Signals:

1 - Audio R	1.8V RMS	
2 - Audio R		
3 - Audio L	1.8V RMS	
4 - Audio GND		
5 - Blue/Chroma		
GND		
6 - Audio L		
7 - Blue out/		
Chroma in	0.7Vpp \pm 0.1V into 75 Ohm (*)	
8 - Function switch	<2V = TV >4.5V / <7V = asp. ratio 16:9 DVD >9.5V / <12V = asp. ratio 4:3 DVD	
9 - Green GND		
10 - P50 control		
11 - Green	0.7Vpp \pm 0.1V into 75 Ohm (*)	
12 - Nc		
13 - Red/Chroma		
GND		
14 - fast switch		
GND		
15 - Red out/		
Chroma out	0.7Vpp \pm 0.1V into 75 Ohm (*) \pm 3dB 0.3Vpp Chroma (burst)	
16 - fast switch		
RGB/ CVBS	or Y <0.4V into 75 Ohm = CVBS >1V / <3V into 75 Ohm = RGB	
17 - Y/CVBS GND		
OUT		
18 - Y/CVBS GND		
IN		
19 - CVBS/Y	1Vpp \pm 0.1V into 75 Ohm (*)	
20 - CVBS/Y		
21 - Shield		

1.3.2 SCART 2 (Connected to AUX)

Pin Signals:

1 -Audio R	1.8V RMS	
2 -Audio R		
3 -Audio L	1.8V RMS	
4 -Audio GND		
5 -Blue/Chroma		
GND		
6 -Audio L		
7 -Blue in/		
Chroma out	\pm 3dB 0.3Vpp Chroma (burst)	
8 -Function switch		
9 -Green GND		
10 -P50 control		

11	-Green		SNR C - AM	: > -65 dB
12	-Nc		SNR C - PM	: > -65 dB
13	-Red/Chroma GND		Bandwidth Y	: 5 MHz ± 1 dB
14	-fast switch GND		1.4.3 SCART (RGB)	
15	-Red in/ Chroma in		SNR	: > -65 dB on all output
16	-fast switch RGB/ CVBS or Y		Bandwidth	: 5 MHz ± 1 dB
17	-CVBS GND OUT		1.5 Audio Performance	
18	-CVBS GND IN		1.5.1 Cinch Output Rear	
19	-CVBS/Y/RGB sync 1Vpp ± 0.1V into 75 Ohm (*)		Output voltage 2 channel mode	: 2Vrms ± 1.5dB
20	-CVBS/Y		Output voltage 5.1 channel Dolby	: 1.41Vrms ± 1.5dB
21	-Shield		Channel unbalance (1kHz)	: <0.85dB

(*) for 100% white

1.3.3 Audio/Video Front Input Connectors

Audio

Input voltage : 2 Vrms
Input impedance : >10kΩ

Video - Cinch

Input voltage : 1 Vpp ± 0.1V
Input impedance : 75 Ω

Video - YC (Hosiden)

Input voltage Y : 1Vpp ± 0.1V
Input impedance Y : 75 Ω
Input voltage C : burst 300 mVpp ± {x} dB
Input impedance C : 75 Ω

1.3.4 Cinch Audio/Video Line Input Rear

Audio (EXT1)

Input voltage : 2 Vrms
Input impedance : >10k Ω

Video (EXT4)

Input voltage : 1 Vpp ± 0.1V
Input impedance : 75 Ω

1.3.5 YC Input Rear (Hosiden; EXT3)

1	GND	
2	GND	
3	Input voltage Y 1Vpp ± 0.1V/ 75 Ω	
4	Input voltage C Burst 300 mVpp ± {x} dB/ 75 Ω	

1.4 Video Performance

All outputs loaded with 75 Ohm
SNR measurements over full bandwidth without weighting.

1.4.1 CVBS Output Rear (EXT4)

SNR Luminance : > -65 dB
SNR Chrominance AM : > -65 dB
SNR Chrominance PM : > -65 dB
Bandwidth Luminance : 5 MHz ± 1 dB

1.4.2 YC Output Rear (Hosiden ; EXT3)

SNR : > -65 dB

1.4.3 SCART (RGB)

SNR : > -65 dB on all output
Bandwidth : 5 MHz ± 1 dB

1.5 Audio Performance

1.5.1 Cinch Output Rear

Output voltage 2 channel mode : 2Vrms ± 1.5dB
Output voltage 5.1 channel Dolby : 1.41Vrms ± 1.5dB
Channel unbalance (1kHz) : <0.85dB
Crosstalk 1kHz : >105dB
Crosstalk 20Hz-20kHz : > 95dB
Frequency response 20Hz- 20kHz : ± 0.1dB max
Signal to noise ratio : >100 dB
Dynamic range 1kHz : >90dB
Dynamic range 20Hz-20kHz : >88dB
Distortion and noise 1kHz : >90dB
Distortion and noise20Hz-20kHz : >80dB
Intermodulation distortion : >87dB
Phase non linearity : ± 1o max.
Level non linearity : ± 0.5dB max.
Mute (spin-up, pause, access) : >100dB
Outband attenuation: : > 50dB above 25kHz

1.5.2 Scart Audio

Output voltage 2 channel mode : 2Vrms ± 1.5dB
Output voltage 5.1 channel Dolby : 1.41Vrms ± 1.5dB
Channel unbalance (1kHz) : <0.85dB
Crosstalk 1kHz : >105dB
Crosstalk 20Hz-20kHz : > 95dB
Frequency response 20Hz- 20kHz : ± 0.1dB max
Signal to noise ratio : >100 dB
Dynamic range 1kHz : >90dB
Dynamic range 20Hz-20kHz : >88dB
Distortion and noise 1kHz : >90dB
Distortion and noise20Hz-20kHz : >80dB
Intermodulation distortion : >87dB
Phase non linearity : ± 1o max
Level non linearity : ± 0.5dB max
Mute (spin-up, pause, access) : >100dB
Outband attenuation: : > 50dB above 25kHz

1.6 Digital Output

1.6.1 Coaxial

CDDA/ LPCM (incl MPEG1) : according IEC958
MPEG2, AC3 audio : according IEC1937
DTS : according IEC1937, amendment 1

1.6.2 Optical

identical to coaxial

1.7 Digital Video Input (IEEE 1394)

1.7.1 Applicable Standards

Implementation according:
IEEE Std 1394-1995
IEC 61883 - Part 1
IEC 61883 - Part 2 SD-DVCR (02-01-1997)

Specification of consumer use digital VCR's using 6.3 mm magnetic tape - dec.1994
Mechanical connection according:
Annex A of 61883-1

1.7.2 Audio Quality

Output voltage 2 channel mode	: 2Vrms +/- 1.5dB
Channel unbalance (1kHz)	: Tbd
Crosstalk 1kHz	: > 85 dB
Crosstalk 20Hz-20kHz	: > 95 dB
Frequency response 20Hz- 12kHz	: +/- 1dB max
Signal to noise ratio	: >95 dB
Dynamic range 1kHz	: tbd
Dynamic range 20Hz-20kHz	: Tbd
Distortion and noise 1kHz	: >65dB
Distortion and noise 20Hz-20kHz	: >65dB
Intermodulation distortion	: >80dB
Phase non linearity	: tbd
Level non linearity	: tbd
Outband attenuation	: tbd

1.8 P50 System Control

Via SCART pin nr 10

1.9 Dimensions and Weight

Height of feet	: 12mm
Apparatus tray closed	: WxDxH :435 x 325 x 107
Apparatus tray open	: WxDxH :435 x 465 x 107
Weight without packaging	: 5.67 Kg
Weight accesoiries	: 1.675 Kg

1.10 Laser Output Power & Wavelength

1.10.1 DVD

Output power during reading	: 0.8mW
Output power during writing	: 20mW
Wavelength	: 660nm

1.10.2 CD

Output power	: 0.3mW
Wavelength	: 780nm

2. Safety Instructions, Warnings, Notes, and Service Hints

2.1 Safety Instructions

2.1.1 General Safety

Safety regulations require that during a repair:

- Connect the unit to the mains via an isolation transformer.
- Replace safety components, indicated by the symbol ▲, only by components identical to the original ones. Any other component substitution (other than original type) may increase risk of fire or electrical shock hazard.

Safety regulations require that after a repair, you must return the unit in its original condition. Pay, in particular, attention to the following points:

- Route the wires/cables correctly, and fix them with the mounted cable clamps.
- Check the insulation of the mains lead for external damage.
- Check the electrical DC resistance between the mains plug and the secondary side:
 1. Unplug the mains cord, and connect a wire between the two pins of the mains plug.
 2. Set the mains switch to the 'on' position (keep the mains cord unplugged!).
 3. Measure the resistance value between the mains plug and the front panel, controls, and chassis bottom.
 4. Repair or correct unit when the resistance measurement is less than 1 MΩ.
 5. Verify this, before you return the unit to the customer/user (ref. UL-standard no. 1492).
 6. Switch the unit 'off', and remove the wire between the two pins of the mains plug.

2.1.2 Laser Safety

This unit employs a laser. Only qualified service personnel may remove the cover, or attempt to service this device (due to possible eye injury).

Laser Device Unit

Type	: Semiconductor laser GaAlAs
Wavelength	: 650 nm (DVD) : 780 nm (VCD/CD)
Output Power	: 20 mW (DVD+RW writing) : 0.8 mW (DVD reading) : 0.3 mW (VCD/CD reading)
Beam divergence	: 60 degree



Figure 2-1

Note: Use of controls or adjustments or performance of procedure other than those specified herein, may result in hazardous radiation exposure. Avoid direct exposure to beam.

2.2 Warnings

2.2.1 General

- All ICs and many other semiconductors are susceptible to electrostatic discharges (ESD, ⚡). Careless handling during repair can reduce life drastically. Make sure that, during repair, you are at the same potential as the mass of the set by a wristband with resistance. Keep components and tools at this same potential.

Available ESD protection equipment:

- Complete kit ESD3 (small tablemat, wristband, connection box, extension cable and earth cable) 4822 310 10671.
- Wristband tester 4822 344 13999.
- Be careful during measurements in the live voltage section. The primary side of the power supply (pos. 1005), including the heatsink, carries live mains voltage when you connect the player to the mains (even when the player is 'off!'). It is possible to touch copper tracks and/or components in this unshielded primary area, when you service the player. Service personnel must take precautions to prevent touching this area or components in this area. A 'lightning stroke' and a stripe-marked printing on the printed wiring board, indicate the primary side of the power supply.
- Never replace modules, or components, while the unit is 'on'.

2.2.2 Laser

- The use of optical instruments with this product, will increase eye hazard.
- Only qualified service personnel may remove the cover or attempt to service this device, due to possible eye injury.
- Repair handling should take place as much as possible with a disc loaded inside the player.
- Text below is placed inside the unit, on the laser cover shield:

CAUTION VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID EXPOSURE TO BEAM
 ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING VED ÅBNING UNDGÅ UDSÆTTELSE FOR STRÅLING
 ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING NÅR DEKSEL APNES UNNGÅ EKSPONERING FOR STRÅLEN
 VARNING SYNLIG OCH OSYNLIG LASERSTRÅLING NÅR DENNA DEL ÄR ÖPPNAD BETRÄKTA EJ STRÅLEN
 VARO! AVATT AESSA OLET ALTTIINA NÄKYVÄLLE JA NÄKYMÄTTÖMÄLLE LASER SÄTEILYLLE. ÄLÄ KAT SO SÄT EESSEEN
 VORSICHT SICHTBARE UND UNSICHTBARE LASERSTRAHLUNG WENN ABDECKUNG GEÖFFNET NICHT DEM STRAHL AUSSETZEN
 DANGER VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID DIRECT EXPOSURE TO BEAM
 ATTENTION RAYONNEMENT LASER VISIBLE ET INVISIBLE EN CAS D'OUVERTURE EXPOSITION DANGEREUSE AU FAISCEAU

Figure 2-2

2.2.3 Notes

Dolby

Manufactured under licence from Dolby Laboratories. "Dolby", "Pro Logic" and the double-D symbol are trademarks of Dolby Laboratories. Confidential Unpublished Works.

©1992-1997 Dolby Laboratories, Inc. All rights reserved.



Figure 2-3

Trusurround

TRUSURROUND, SRS and symbol (fig 2-4) are trademarks of SRS Labs, Inc. TRUSURROUND technology is manufactured under licence from SRS Labs, Inc.



Figure 2-4

Video Plus

“Video Plus+” and “PlusCode” are registered trademarks of the Gemstar Development Corporation. The “Video Plus+” system is manufactured under licence from the Gemstar Development Corporation.



Figure 2-5

Macrovision

This product incorporates copyright protection technology that is protected by method claims of certain U.S. patents and other intellectual property rights owned by Macrovision Corporation and other rights owners.

Use of this copyright protection technology must be authorized by Macrovision Corporation, and is intended for home and other limited viewing uses only unless otherwise authorized by Macrovision Corporation. Reverse engineering or disassembly is prohibited.

3. Directions For Use

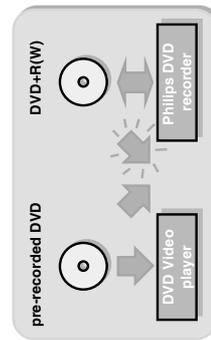
Introduction

DVD Video Recorder

DVD (Digital Versatile Disc) is the new storage medium that combines the convenience of the Compact Disc with the latest advanced digital video technology. DVD-Video uses state-of-the-art MPEG2 data compression technology to register an entire movie on a single 5-inch disc. DVD's variable bitrate compression, running at up to 9.8 Mbits/second, captures even the most complex pictures in their original quality. The crystal-clear digital pictures have a horizontal resolution of over 500 lines, with 720 pixels (picture elements) to each line. This resolution is more than double that of VHS, superior to Laser Disc, and entirely comparable with digital masters made in recording studios.

DVD recording is the next step in video technology. DVD+ReWritable (DVD+RW) uses phase-change media, the same technology that formed the basis for CD-ReWritable. A high-power laser is used to change the reflectivity of the recording layer. This process can be repeated more than a thousand times. DVD+Recordable (DVD+R) uses discs based on an organic dye, a technology pioneered with the successful CD-Recordable format, to produce discs that keep your data for a lifetime.

Your Philips DVD recorder is a **recorder and player** for digital video discs, with a **two-way compatibility** to the universal DVD-Video standard. This means that - existing **pre-recorded DVD-Video** discs can be played on your Philips DVD recorder and - **recordings**, made on your Philips DVD recorder, can be played on most DVD-Video players and DVD-ROM drives.



With it, you will be able to record TV programmes or to edit and archive your own camcorder recordings. Superb digital picture and sound quality, quick access to the tracks you have recorded and extensive playback features contribute to a completely new video experience.

From now on you will enjoy full-length movies with true cinema picture quality, and stereo or Multi-channel sound (depending on the disc, and on your playback set-up). You will find your recorder remarkably easy to use, by way of the On-Screen Display on your TV and the display on the DVD recorder, in combination with the remote control.

Box contents

- First, check and identify the contents of your DVD recorder package, as listed below:
- DVD recorder
 - Remote Control Handset with separately-packed batteries
 - 2-core power cord
 - SCART cable
 - S-video cable
 - Antenna (aerial) cable
 - Audio cable
 - Video cable
 - DVD+RW disc
 - User Manual
 - Warranty card

If any item should be damaged or missing, please inform your supplier without delay.

Keep the packaging materials; you may need them to transport your recorder in the future.

Placement



- Place the recorder on a firm, flat surface.
- Keep away from domestic heating equipment and direct sunlight.
- In a cabinet, allow about 2.5 cm (1 inch) of free space all around the recorder for adequate ventilation.
- The lens may cloud over when the DVD recorder is suddenly moved from cold to warm surroundings. Playing a CD/DVD is not possible then. Leave the DVD recorder in a warm environment for two hours before use, so the moisture can evaporate.
- The recorder should not be exposed to dripping or splashing, no objects filled with liquids, such as vases, should be placed on the recorder.

English

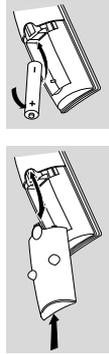
Cleaning discs

Some problems may occur because the disc inside the recorder is dirty. To avoid these problems clean your discs regularly, in the following way:

- When a disc becomes dirty, clean it with a cleaning cloth. Wipe the disc from the centre out.
- Caution:**
Do not use solvents such as benzine, thinner, commercially available cleaners, or anti-static spray intended for analogue discs.
Do not use commercially available cleaning discs to clean the lens, as these discs may damage the optical unit.

Remote control

Loading the batteries



- Open the battery compartment cover.
- Insert two 'AA' (LR-6) batteries as indicated inside the battery compartment.
- Close the cover.

Caution:

Do not mix old and new batteries. Never mix different types of batteries (standard, alkaline, etc.). This may reduce the lifetime of the batteries.

Installation

Connections - back side of your DVD recorder

- Please refer to your TV set, VCR, Stereo System and any other User Manual(s) as necessary to make the optimal connections.
- Do not connect the power until all other connections are made.

- Do not connect your DVD recorder to your TV set via your VCR, because the video quality could be distorted by the copy protection system.
- For better sound reproduction you can connect the recorder audio outputs to your amplifier, receiver, stereo system or A/V equipment. For this see 'Connecting to A/V receiver or A/V amplifier'.

Caution:

Do not connect the recorder's audio output to the phono input of your audio system in order to avoid damage to your equipment.

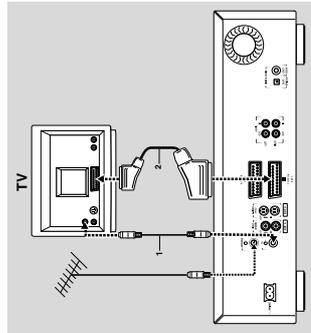
Connecting to the antenna

- Remove the antenna (aerial) cable plug from your TV set and insert it into the antenna socket at the back of the DVD recorder.
- Plug one end of the antenna (aerial) cable supplied (1) into the TV socket on the DVD recorder and the other end into the antenna input socket on your TV set.

Connecting to a TV set

To obtain the highest possible picture and sound quality from your TV set it is recommended to use the SCART connector on both DVD recorder and TV set.

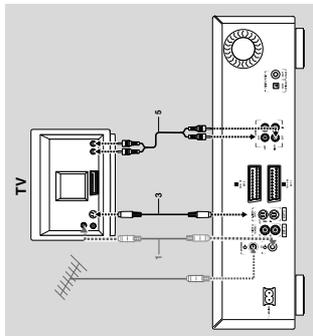
- Connect the bottom SCART connector (EXT 1) to the TV set, using the SCART cable supplied (2) as shown in the drawing. If your TV set is equipped with EasyLink or Cinema Link, make sure you use the correct SCART connector. For this refer to the user manual of your TV set.



If your TV set is not equipped with a SCART connector, you can connect the DVD recorder with the S-video (Y/C) sockets.

S-video (Y/C) connection

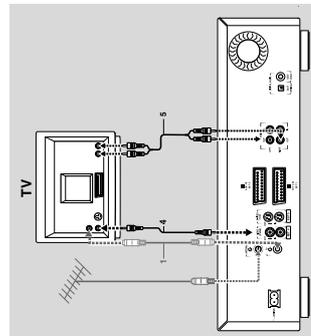
- Connect the S-video output socket to the corresponding input socket on the TV set, using the supplied S-video cable (3).
- Connect the audio Left (white) and Right (red) output sockets to the corresponding sockets on the TV set using the audio cable supplied (5).



If your TV set is not equipped with S-video sockets, then connect the DVD recorder with the CVBS sockets to your TV set.

Video (CVBS) connection

- Connect the Video (CVBS) output socket (yellow) to the corresponding input socket on the TV set using the video cable supplied (4).
- Connect the audio Left (white) and Right (red) output sockets to the corresponding sockets on the TV set using the audio cable supplied (5).



Connecting to audio equipment

Connecting to A/V receiver or A/V amplifier with digital Multi-channel decoder

The best possible sound quality is obtained by connecting your DVD recorder to an A/V receiver with Multi-channel decoder (Dolby Digital, MPEG 2 and DTS).

Digital Multi-channel sound

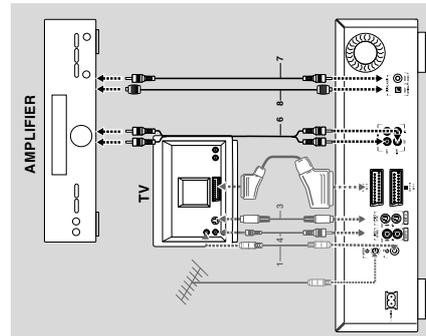
Digital Multi-channel connection provides the optimum sound quality. For this you need a Multi-channel A/V receiver that supports one or more of the audio types supported by your DVD recorder (MPEG 2, Dolby Digital and DTS). For this you can check the receiver manual and the logos on the front of the receiver.

- Connect the recorder's digital audio output to the corresponding input on the receiver. Use a digital coaxial cable (7) or a digital optical audio cable (9).

If you do not own a digital coaxial audio cable (not supplied), you may use the supplied video cable (4).

Note:

If the audio type of the digital output does not match the capabilities of your receiver, the receiver will produce a strong, distorted sound. The audio type of the DVD disc in play is displayed in the Status Window, when changing the language. 6 Channel Digital Surround Sound via digital connection can only be obtained if your receiver is equipped with a Digital Multi-channel decoder.



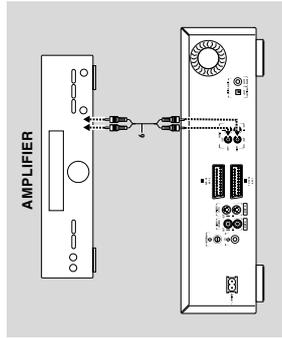
If you cannot connect your DVD recorder to an A/V receiver with Multi-channel decoder, choose one of the following alternatives.

Connecting to a receiver equipped with two channel digital stereo (PCM)

- Connect the recorder's digital audio output to the corresponding input on your receiver. Use the supplied video (CVBS) cable (7) or an optional digital optical audio cable (9).
- After installation you will need to activate PCM on the DVD recorder's digital output (see 'User Preferences').

Connecting to a receiver equipped with Dolby Pro Logic

- Connect the recorder to the TV set and connect the recorder's audio Left and Right output sockets to the corresponding inputs on the Dolby Pro Logic Audio/Video receiver, using the audio cable supplied (6).



- Make the appropriate Sound settings for Analogue Output in the user preferences menu.

Connecting to a TV set equipped with a Dolby Pro Logic decoder

- Connect the recorder to the TV set as described in chapter 'Connecting to a TV set'.

Connecting to a receiver with two channel analogue stereo

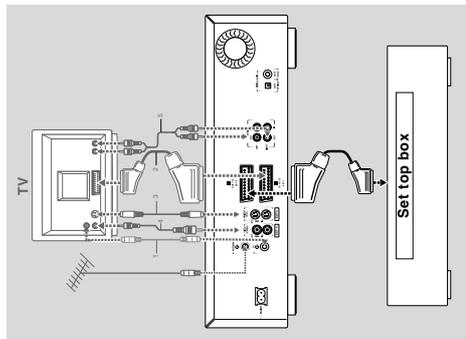
- If you have a receiver with two-channel analogue stereo without any of the above mentioned sound systems, connect the audio Left and Right output sockets to the corresponding sockets on your receiver, amplifier or stereo system. Use the audio cable supplied (6).

Connecting to other equipment

Use the top SCART connector (EXT 2) on your DVD recorder to make connections to a:

- **Satellite receiver or Set top box,**
 - **VCR,**
 - **DVD-Video player**
- Most pre-recorded video cassettes and DVD discs are copy protected. If you try to copy them the display shows 'COPY PROTECT'.

For installation of a decoder, see 'User Preferences' - 'Installation'.

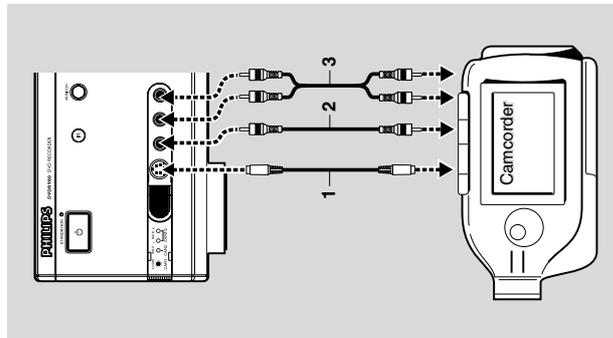


- Notes:
- If the power is off or Low Power Standby is selected (see User Preferences - features), the signal from EXT 2 will not be passed on to the TV set on EXT 1.
 - EasyLink functionality will not be available to devices connected via the DVD recorder's EXT 2 SCART connector.

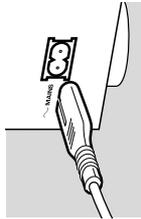
Connections - frontside of your DVD recorder

Camcorder connection

- If you have a DV, Digital 8, Hi-8 or S-VHS(C) camcorder, connect the S-video input socket to the corresponding output socket on the camcorder, using the S-video cable supplied (1) and connect the audio cable (3) supplied.
- Otherwise connect the Video input socket (yellow) to the corresponding output socket on the camcorder using the video cable supplied (2) and connect the audio Left (white) and Right (red) input sockets to the corresponding sockets on the camcorder using the audio cable supplied (3).
- If your camcorder has mono sound, use only the left audio connector. In this case the sound will be recorded on both audio channels.



Power supply



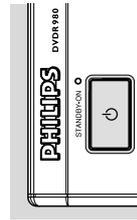
- Make sure that all necessary connections are made before connecting the DVD recorder to the power supply.
- Plug the power cable supplied into the Power connector on the rear of the recorder.
- Plug the mains plug into an AC outlet.

Note:
Always check if the local mains voltage matches the required 220V - 240V.
When the recorder is in the Standby position, it is still consuming some power.

If you wish to disconnect your DVD recorder completely from the mains, withdraw the plug from the AC Outlet.
When the DVD recorder is disconnected from the mains, TV channels and timer data will be stored typically 1 year.

Switching on

- Switch on the TV set and select the programme number that you have chosen for video playback (see operating manual for your TV set).
- Press () **STANDBY/ON**
 - The recorder display lights up. If you have not yet installed your DVD recorder, it will enter 'virgin mode'. In this mode you will have to set your personal preferences.



First time set-up: virgin mode

After switching on the DVD recorder for the very first time the 'virgin mode screen' will appear.

In 'virgin mode' you may have to set your preferences for some of the recorder's features.

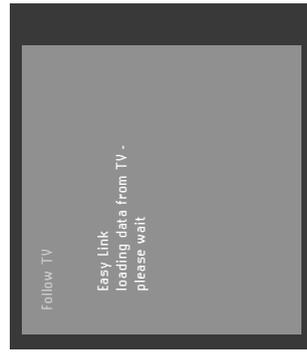
If the 'virgin mode screen' does not appear, your DVD recorder has been installed already. You may still change the settings via the 'Installation menu'. Depending on the kind of TV set, preferences will have to be set manually or they will be taken over automatically from the TV set.

Automatic setting

When your TV set is equipped with EasyLink™, Cinema Link™, NetView™, Link™, SmartLink™, Q-Link™ or MegaLogic™, the TV settings will be taken over from the TV set but they cannot be changed manually afterwards.

When preferences are taken over from your TV set, the message 'Easy Link loading data from TV-please wait' will appear.
Menus for which no preferences are available will be displayed. They have to be set manually.

Note:
Preferences have to be set in the order in which the item menus will appear on the screen.
If the recorder is switched off while setting user preferences, all preferences have to be set again after switching the recorder on again.
The 'virgin mode' will only be concluded after the preferences for the last item have been confirmed.



Manual setting

- When a menu is displayed:
 - Use the ∇/Δ (down/up cursor) keys to go through the options in the menu. The icon of the selected option will be highlighted.
 - Use **OK** to confirm your selection and to select the next menu.

The following items may have to be set in virgin mode:

Menu language

The on-screen menus of DVD-Video discs will be displayed in the language you choose.



Audio language

The sound of DVD-Video discs will be in the language you choose, provided this is available on the disc in play. If not, speech will revert to the first spoken language on the disc. Also the DVD-Video disc menu will be in the language you choose, provided this is available on the disc.



Subtitle language

The subtitles of DVD-Video discs will be in the language you choose provided this is available on the disc. In play, if not, subtitles will revert to the first subtitle language on the disc.

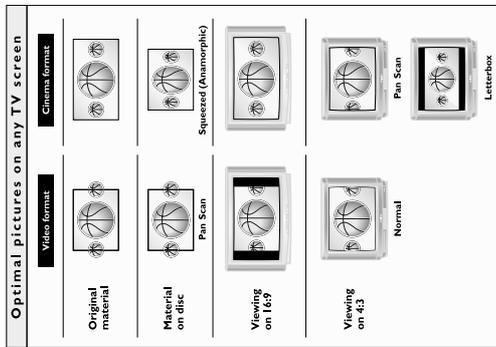


TV Shape



You can choose:

- 16:9 if you have a wide screen (16:9) TV set.
- 4:3 if you have a regular (4:3) TV set. In this case you can also choose between:
 - Letterbox for a 'wide-screen' picture with black bars at the top and bottom.
 - Pan Scan, for a full-height picture with the sides trimmed. If a disc has Pan Scan, the picture then moves (pans) horizontally to keep the main action on the screen.



Country

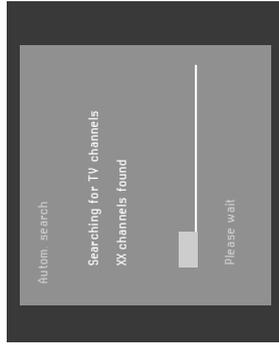
Select your country. This is used as input for the 'Parental Control' feature (see 'Access Control') as well as the searching of TV channels.



Auto TV Channel Search

Make sure the antenna is connected. See 'Connecting to the antenna'. Your DVD recorder will search for all TV channels. It stores channels in the sequence they are found.

- Confirm with **OK**.
- Auto search starts. This can take several minutes.

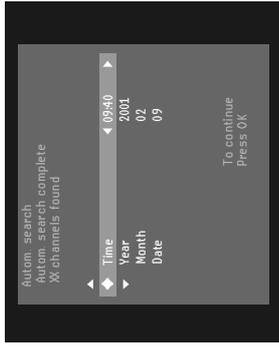


When Auto search is completed 'Autom search complete - XX channels found' appears on the TV screen.

After Auto channel search you can have TV channels stored automatically in the same order as your TV set. See 'User preferences installation' - 'Follow TV'.

Time/Date

When Channel auto search is completed the actual Time and Date are also set automatically. If the time in the DVD recorder display is not correct, the clock must be set manually.



- Adjust 'Time', 'Year', 'Month', 'Date' if required, with the ∇ (down cursor) or Δ (up cursor) key.
- Change values with the \leftarrow (left cursor) or \rightarrow (right cursor) key or the digit keys 0-9.
- To end, press **OK**.

Note:

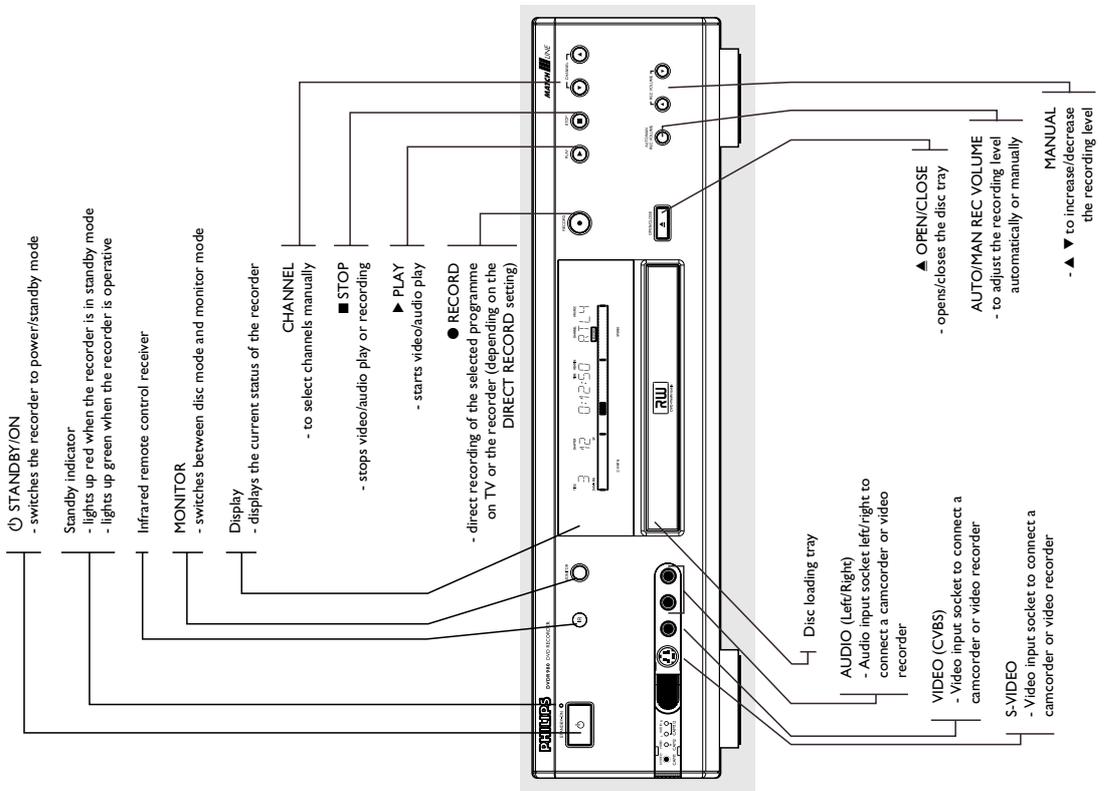
All these items may have to be set after first start up ('virgin mode'). After that they can always be adapted in the user preferences menu. When your TV set is equipped with EasyLink the TV set presets will be taken over from the TV set but they cannot be changed manually afterwards.

Virgin mode settings are now completed. All settings can still be changed. See 'User preferences'.

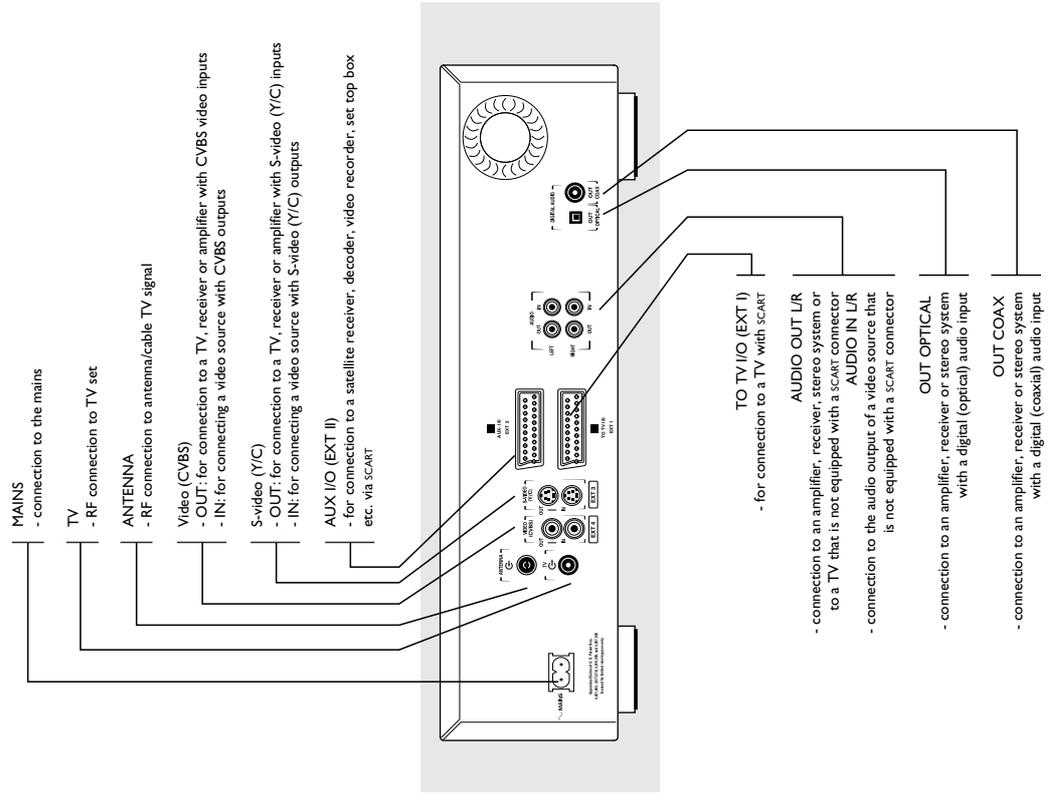
English

Functional overview

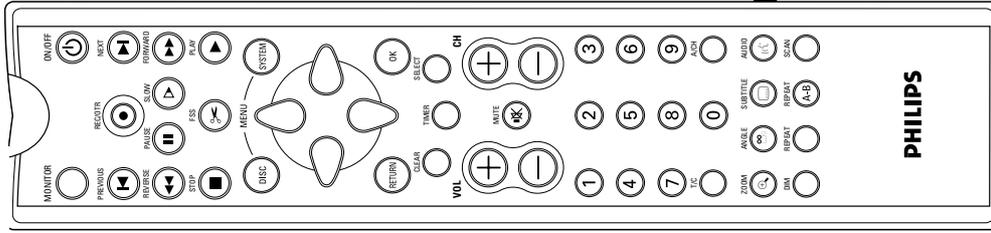
Front of recorder



Rear of recorder



Remote control



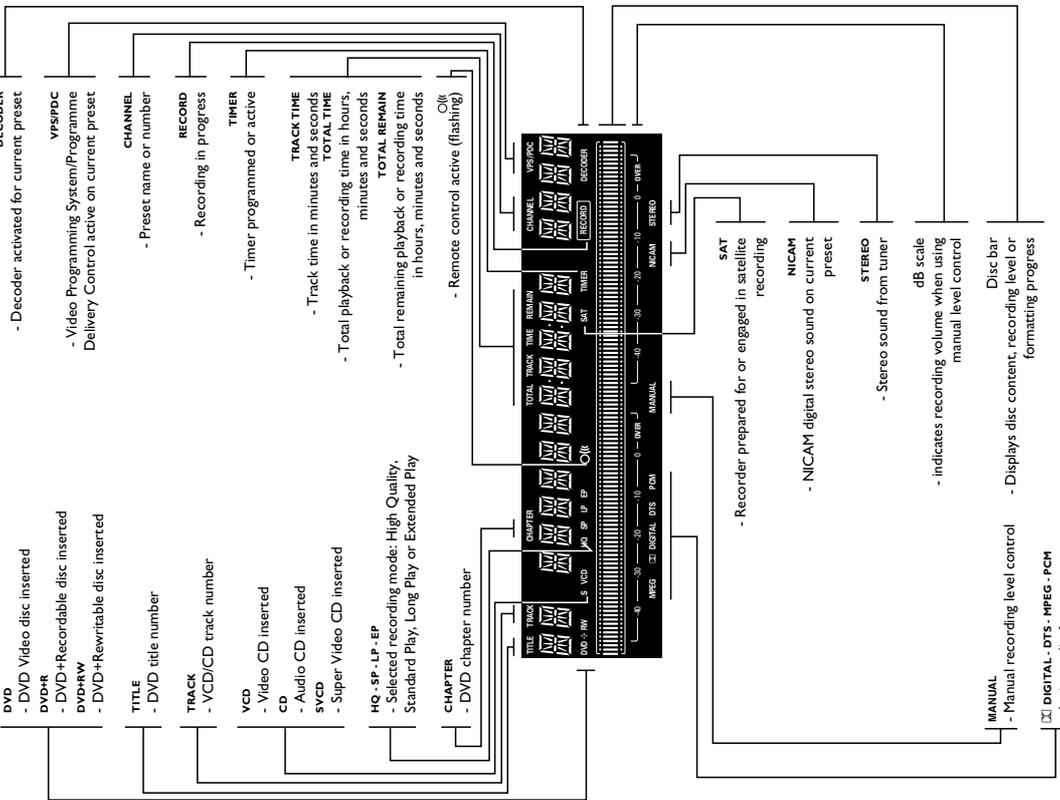
MONITOR
- switches between disc mode and monitor mode

◀ - previous chapter, track or title
● - direct recording of the currently selected programme
▶ - next chapter, track or title
◀◀ - search backward
|| - pause
▶▶ - slow motion
▶▶▶ - search forward
■ - stop
FSS - displays Favorite Scene Selection menu for DVD+RW or DVD+R disc
▶ - play

VOL +/-
- TV volume up/down
MUTE - TV Mute ON/OFF
CH +/-
- programme up/down

ZOOM
- enlarge video image
ANGLE
- select DVD camera angle
SUBTITLE
- subtitle language selector
AUDIO
- audio language selector

Display



DVD
- DVD Video disc inserted
DVD+R
- DVD+Recordable disc inserted
DVD+RW
- DVD+Rewritable disc inserted

TITLE
- DVD title number
TRACK
- VCD/CD track number

VCD
- Video CD inserted
CD
- Audio CD inserted
SVCD
- Super Video CD inserted

HQ-SP-LP-EP
- Selected recording mode: High Quality, Standard Play, Long Play or Extended Play
CHAPTER
- DVD chapter number

DECODER
- Decoder activated for current preset
VSP/PC
- Video Programming System/Programme Delivery Control active on current preset
CHANNEL
- Preset name or number
RECORD
- Recording in progress
TIMER
- Timer programmed or active

TRACK TIME
- Track time in minutes and seconds
TOTAL TIME
- Total playback or recording time in hours, minutes and seconds
TOTAL REMAIN
- Total remaining playback or recording time in hours, minutes and seconds
OK
- Remote control active (flashing)

SAT
- Recorder prepared for or engaged in satellite recording
NICAM
- NICAM digital stereo sound on current preset
STEREO
- Stereo sound from tuner

dB scale
- indicates recording volume when using manual level control
Disc bar
- Displays disc content, recording level or formatting progress

MANUAL
- Manual recording level control
DIGITAL - DTS - MPEG - PCH
- Active audio format

ON/OFF ⏻

DISC MENU
- displays DVD disc menu or index picture screen
SYSTEM MENU
- displays recorder system menu bar
▽ △ ◀ ▶
- down/up/right/left cursor movement

RETURN
- return to previous menu on (SVCD) disc
CLEAR
- delete last entry/clear timer
TIMER
- displays the 'timer menu'

SELECT
- switches between different values in a menu
- switches between record modes in the Index Picture Screen and in monitor mode
OK
- acknowledge menu selection

0-9
- numerical key pad
T/C
- select title
- select chapter
A/CH Alternate Channel
- switches to the previous TV channel

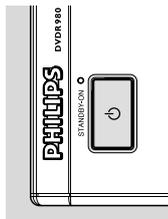
SIDE SWITCH
- enables other keys to operate the TV set (see Appendix)

DIM
- changes brightness setting of display
REPEAT
- repeat chapter, track, title, disc
REPEAT A-B
- repeat sequence
SCAN
- playback of the first 10 seconds of each chapter within a title (DVD) or the first 10 seconds of each track on a disc (VCD/CD)

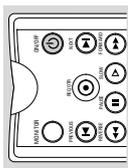
Operation

Important notes for operation

You can switch on the DVD recorder with the **STANDBY/ON** key. Keep your DVD recorder connected to the mains at all times to ensure that programmed recordings can be made and that the television functions normally.



Both the DVD recorder and the remote control have an 'Emergency interrupt' button. You can use the **STANDBY/ON** button to interrupt a function. When you have an operating problem, you can interrupt the function and start again.



When you switch off the DVD recorder, the display will briefly show "OFF".

Loading discs

- 1 Press **▲ OPEN/CLOSE** on the front of the recorder. The disc loading tray opens.
- 2 Lay your chosen disc in the tray, label side up. Make sure it is sitting properly in the correct recess.
- 3 Press **▲ OPEN/CLOSE**, to close the tray.
 - ▶ **"READING"** appears in the status box and on the recorder display. If the inserted disc is pre-recorded or write-protected, playback always starts automatically.

You can always unload a disc by pressing **▲ OPEN/CLOSE** again or pressing **■ STOP** on the remote control for two seconds.

Note:
If 'Child Lock' is set to ON and the disc inserted is not in the 'child safe' list (not authorized), the PIN code must be entered and/or the disc has to be authorized. (see 'Access Control')

Disc types

You will recognize the different types of discs, that can be used in your DVD recorder by the logo. Depending on the disc type you can either use it for recording and playback or playback only. Some discs are not suitable at all to be used in the DVD recorder.

In the next table a summary is given of all existing disc types and their DVD recorder compatibility.

The following disc types can be used for recording and playback:

DVD+RW

Records and plays: In case of a new blank disc, after the first recording, some more time (up to two minutes) is needed to make the disc compatible with DVD-Video players.



DVD+R

Records and plays.



The following disc type can be used for playback only:

DVD-Video



DVD-R

Only plays if it contains DVD-Video.



DVD-RW

Only plays if it is recorded in Video mode and has been finalized.



CD Digital Audio

You can play digital audio CDs in conventional style through a stereo system, using the keys on the remote control and/or front panel, or via the TV set using the on-screen display (OSD).



Super Audio CD

Of hybrid SACD discs, the CD layer can be played.

(Super) Video CD

Depending on the material on the disc (a movie, video clips, a drama series, etc.) these discs may have one or more tracks, and tracks may have one or more indexes, as indicated on the disc case. To make access easy and convenient, your recorder lets you move between tracks, and between indexes.



CD-R/CD-RW

Plays if it contains Audio CD.



The following disc types cannot be used at all, neither for recording nor for playback:

DVD-RAM



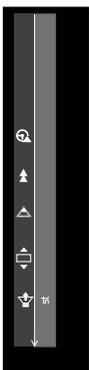
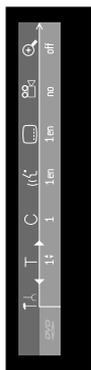
DVD-Audio



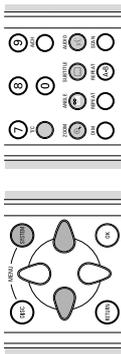
English

On-screen display information

System menu bar



The system menu bar can be called up by pressing any of the following keys on the remote control: **SYSTEM MENU**, **T/C**, **ANGLE**, **SUBTITLE**, **AUDIO** and **ZOOM**.

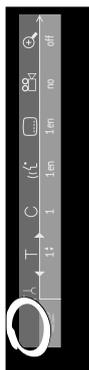


Widescreen (16:9) TV sets may show only part of the system menu bar in certain screen modes. Select a different screen mode on the TV to see the full menu. A number of recorder functions can be controlled via the system menu bar. You can navigate between the two parts of the system menu bar with the **<** (left cursor) and the **>** (right cursor) key.

System menu bar icons

PART 1		PART 2	
User preference	Sound	Step motion	Fast motion
Title/Track	Slow motion	Time search	
Chapter/Index	Audio language		
Subtitle language	Angle		
Zoom			

Temporary Feedback Field



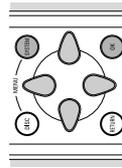
The system menu bar contains a 'Temporary Feedback Field' with information concerning prohibited actions, playback modes, available angles, etc.

English

- Scan
- Repeat All
- Repeat Title
- Repeat Track
- Repeat Chapter
- Repeat A to end
- Repeat A-B
- Angle
- Child Lock On
- Child Safe
- Resume
- Action prohibited

User preference menu operation

- Press **SYSTEM MENU** on the remote control.
- Select **TA** in the system menu bar and press **▽** (down cursor).
 - The user preferences menu appears.
- Use the **◀ ▶ ▷ ▲ ▼** (left, right up down cursor) keys to toggle through the menus, sub menus and submenu options.
 - When a menu item is selected, the cursor keys (on the remote control) to operate the item are displayed next to the item.
- Press **OK** to confirm and return to the main menu.

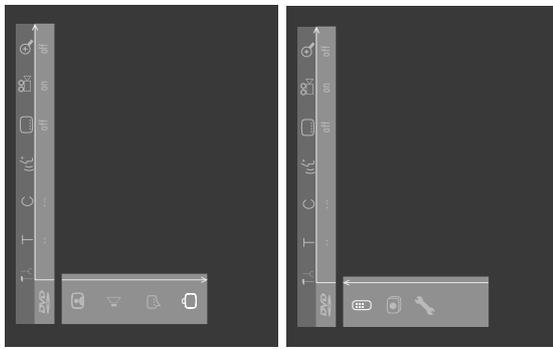


The following functions can be operated via the user preference menu.

User preference menu icons

- Picture settings
- Sound settings
- Language settings
- Feature settings
- Remote control settings
- Record settings
- Installation

- You can navigate between the various items of the user preferences menu with the **△** (up cursor) and the **▽** (down cursor) key. To select an item press **▷** (right cursor) key.



- By pressing **SYSTEM MENU** the system menu bar will disappear from the screen.

Status box

The status box on the left hand side of the screen displays the current status of the recorder and the disc type loaded for several seconds.



Disc type icons

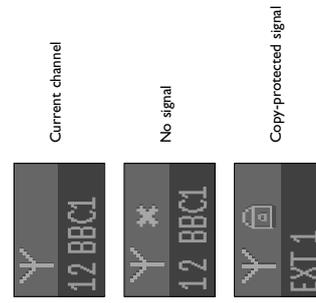
- DVD+RW
- DVD+R
- DVD-V video
- Super Video-CD
- Video-CD
- no disc
- disc error

Disc status icons

- recording
- stop
- playing
- pause play
- record pause
- erasing
- fast forward
- fast reverse
- slow motion

Tuner info box

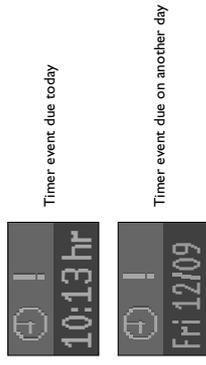
The tuner info box is located at the bottom left of the screen and is displayed in monitor mode (See: Recording Checking input). It displays the currently selected input. When the tuner is selected it shows programme number and/or channel name.



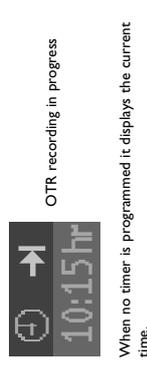
Timer info box

The timer info box is located above the tuner info box and is displayed in monitor mode. It displays the current status of the timer.

When a timer is programmed it shows a timer indication and the start time or date of the first programmed recording.



When an OTR recording is in progress it shows the end time.

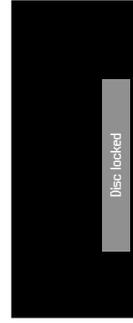


Current time

Note:
Tuner info box and timer info box disappear during playback and after recording is started.

Warning box

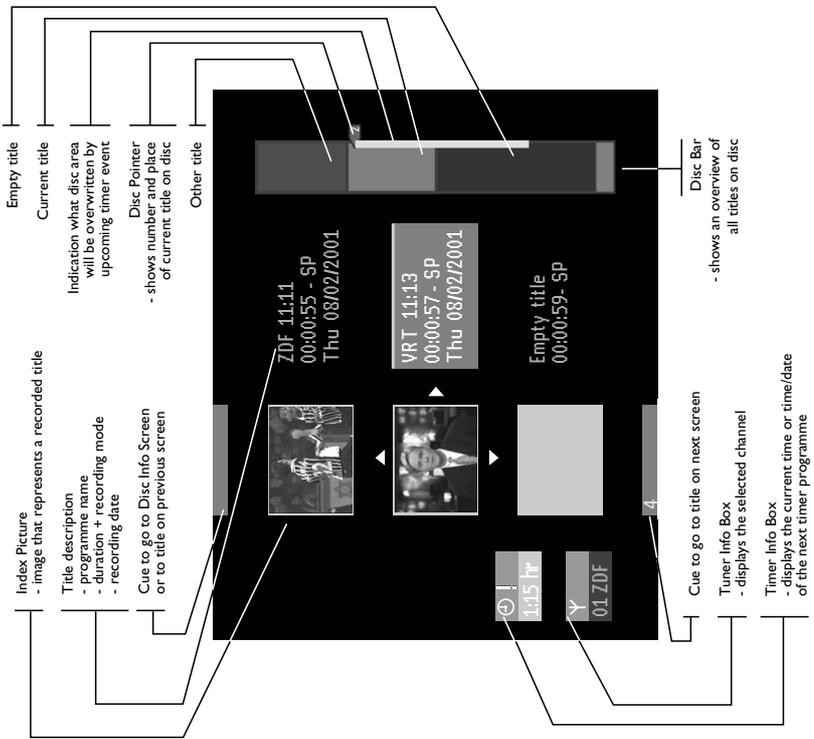
The warning box will be displayed near the bottom of the screen when appropriate. For instance: 'Disc locked'.



Index Picture Screen

The Index Picture Screen displays an overview of the titles recorded on the disc. Each title is represented by an index picture. Next to the index picture the programme name, duration, recording mode and recording date of the title are shown. If no name is known, the DVD recorder will fill in the source and the time of the recording instead.
 Empty spaces (erased titles or blank space at the end of the disc) are also shown as such.
 At maximum three titles will be shown on the screen at once. If more titles are present, you can navigate to those with the ∇ Δ (down/up cursor) keys.

- On the right hand side of the Index Pictures Screen, you can see the disc bar. This gives an overview of all titles on the disc, as well as any empty spaces.
- On the disc bar, an arrow – the disc pointer – indicates your current position on the disc. From this point you may resume playback or recording. If you navigate through the list of titles with ∇ Δ (down/up cursor) or \leftarrow **PREVIOUS** / \rightarrow **NEXT**, the disc pointer will move along.
- Press **STOP** to reset the disc pointer to the beginning of the disc.
- To move the disc pointer to the end of the last title, keep **NEXT** pressed.
- If you navigate from an Index Picture to the box right next to it (containing name, rec mode, etc.), you enter the title settings menu (see under 'Managing disc content' - Title settings).



User preferences

Setting user preferences

You can set your user preferences for some of the recorder features. (See 'Operation' - User preferences menu operation)

The following items can be adapted:

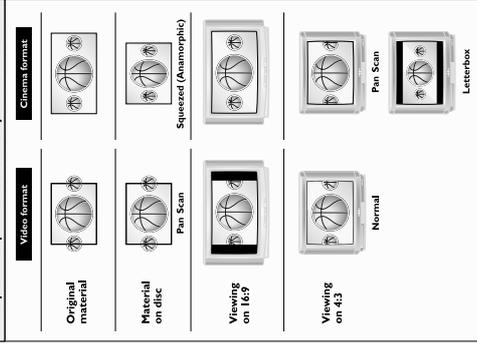
Picture settings

TV Shape

With TV Shape you can adjust the output of your DVD Recorder to optimally fit your TV screen. You can choose:

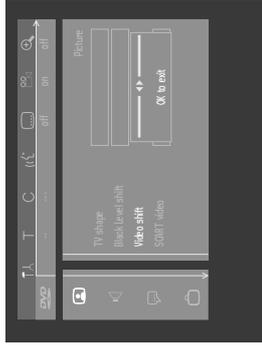
- **16:9** if you have a wide screen (16:9) TV set.
- **4:3** if you have a regular (4:3) TV set. In this case you can also choose between:
 - **letterbox**: for a 'wide-screen' picture with black bars at the top and bottom.
 - **Pan Scan**: for a full-height picture with the sides trimmed. If a disc has Pan Scan, the picture then moves (pans) horizontally to keep the main action on the screen.

Optimal pictures on any TV screen



Black level shift (NTSC only)
 Adapts the colour dynamics to obtain richer contrast. Select **On** or **Off**.

Video shift
 Factory setting is such that the video will be centered on your screen. Use this setting to adjust the position of the picture on your TV set by scrolling it to the left or right.



SCART Video

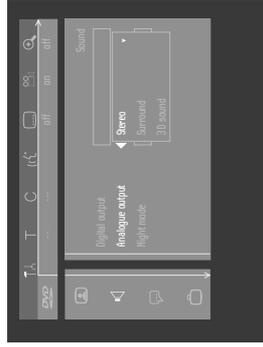
Factory setting is RGB. Select 'S-video' (Y/C) via SCART when connecting to an S-VHS recorder.

Sound settings

Digital output

Factory setting 'All' means that both coaxial and optical outputs are switched on, and that Dolby Digital Multi-channel is fed to the outputs as such MPEG audio is converted to PCM. If your equipment doesn't include a digital Multi-channel decoder, set the digital output to 'PCM only' (Pulse Code Modulation). Both coaxial and optical outputs are then switched on, and Dolby Digital and MPEG audio are converted to PCM. If you are not connecting equipment with a digital input, change the setting to 'Off'.

Analogue output



Select 'Stereo', 'Surround' or '3D Sound'. Factory setting is Stereo.

Surround: Select this setting when using equipment with a Dolby Surround Pro Logic decoder. In this setting the 5.1 audio channels (Dolby Digital, MPEG-2) are downmixed to a Surround-compatible 2-channel output.

3D Sound: In a set-up without rear speakers (analogue stereo output), this option remixes the six channels of digital surround (Dolby Digital, MPEG-2) into a two speaker output, while retaining all of the original audio information. The result is the listening sensation of being surrounded by multiple speakers.

Connected audio system Digital out Analogue out

Amplifier or TV with two channel analogue stereo	Off	Stereo
Amplifier or TV with Dolby Surround or Dolby Pro Logic	Off	Surround
Amplifier with two channel digital stereo	PCM only	Stereo
A/V receiver with Multi-channel decoder (Dolby Digital, MPEG, DTS)	All	Stereo or Surround
Multi-channel A/V receiver with 6-ch connectors	Off	Surround

Night Mode

Night mode optimizes the dynamics of the sound with low volume playback for less disturbance in quiet environments. This only works for Dolby Digital audio on DVD-Video discs.

Language settings

The preferred language can be adapted via the system menu bar. Also see 'Virgin mode'. Settings can be changed for:

- Playback audio language
- Subtitle language
- Menu language
- Country setting.

Feature settings

Access Control

Access Control contains the following features:
Child Lock - When Child Lock is set on, a 4-digit code needs to be entered in order to play discs.
Parental Level - Allows the conditional presentation of DVD discs containing Parental Level information.
Change country - Allows conditional presentation of DVD-Video discs containing country information.
Change code - To change the pin code.
 See 'Access Control'.

PBC

This feature is only available when a (Super) Video CD is loaded. It allows you to disable or enable the PBC (Playback Control) menu of VCD discs. See under 'Special VCD features'. Factory settings is 'On'.

Finalise disc

This option is only available on unfinalised DVD+R discs. See 'Managing disc content' - Finalising a DVD+R disc'.

Remote Control settings

Key sound

The recorder makes a 'beep' sound upon every key command given via recorder or remote control keys. Select 'Off' to disable this sound. Factory setting is 'On'.

Remote control used

If you want to use the remote control of a Philips DVD player instead of the standard DVD recorder remote control, select 'DVD player'. Factory setting is 'DVD recorder'.

System information

When you move further down in the Remote Control settings menu, the system status screen will appear. Press Δ (cursor up) to go back.

Record Settings

Record mode

By selecting a recording mode you define picture quality of recordings and maximum recording time for a disc.

Mode	Picture quality	Total recording time
HQ (High Quality)	best possible picture quality	60 minutes
SP (Standard Play)	pre-recorded DVD quality	120 minutes
LP (Long Play)	better than S-VHS picture quality	180 minutes
EP (Extended Play)	better than VHS picture quality	240 minutes

In practice, the DVD recorder may record a few minutes more than indicated. For playback, the correct recording mode will automatically be selected.

The HQ mode is optimised for recording via the external inputs. For tuner recordings it is recommended to use SP, LP or EP.

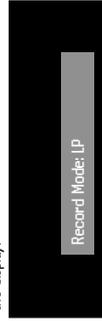
- In the record settings menu, select 'Record mode'.



- Alter the recording mode with \leftarrow or \rightarrow (left-right cursor).
- Confirm with the **OK** key.
- To end, press **SYSTEM MENU**.

An alternative way to select the record mode is available in the Index Picture Screen and in monitor mode:

- Press **SELECT**.
 - ▶ The new record mode appears on the screen and the display.



It is not possible to switch record modes during recording.

Adapt disc format

This option is only available when a DVD+RW or DVD-R disc recorded on a different brand of recorder is loaded. You can adapt the menu to your own recorder.

A DVD+RW video disc that has been recorded on a different type or brand of recorder can be played, but may not provide all features commonly available to DVD+RW discs, such as the on-screen disc bar, the disc settings menu, the title settings menu, and editing. If the disc is not write-protected, the disc format can be adapted to the own recorder, after which these functions are available.

Status box

The status box displays the current status of the recorder and the disc type loaded (See 'Operation' - 'On-screen display information'). You can switch it On or Off.

On = always Off.
On = displayed together with the system menu bar or when changing temporarily (disappears after time-out) when changing the playback or record status. Factory setting is 'On'.

Auto resume

The Auto resume setting only applies to pre-recorded DVD-video and Video CD discs only - not only to the disc in the recorder but also to the last twenty discs you have played.

If 'Auto resume' is set to 'On', playback will start from the point where it was stopped the last time the disc was played.

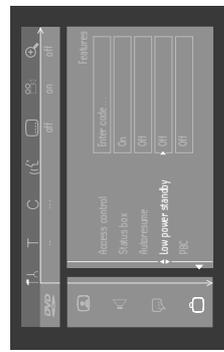
When 'Auto resume' is set to 'Off', the recorder will start playing from the beginning of a disc. In this case you can still resume when \square appears on screen by pressing \blacktriangleright **PLAY**. Factory setting is 'On'.

Low power standby

If low power standby is 'On', the recorder will consume minimum power in standby mode. Factory setting is 'Off'.

Notes:

- When the recorder is in low power standby mode:
 - the output of the equipment connected to EXT 2 will not be passed through to the TV set on EXT 1,
 - the Display will be Off.
 - the Standby indicator on the recorder will still light up in standby mode.



Direct record

With the Direct Record function switched 'On' and the DVD recorder switched to standby, the channel number selected on your television will be automatically taken over by the DVD recorder, at the moment it starts recording. This only applies for televisions connected via SCART, which have video output via SCART or which have EasyLink. Factory setting is 'Off'.

- In the record settings menu, select 'Direct record'.
- Select 'On'. If you select 'Off', the function will be switched off.
- Confirm with **OK**.
- To end, press **SYSTEM MENU**.

SAT record

You can only use this function, when you have a satellite receiver, which can control other equipment by a 'programming' function. In this mode your DVD recorder starts recording when the satellite receiver releases a signal. The start and end of the recording is controlled via one of the SCART sockets.

- In the record settings menu, select 'Sat record'.
 - Select the SCART socket to which the satellite receiver is connected with < or > (left/right cursor).
 - Confirm with **OK**.
 - Insert a recordable DVD+RW disc.
 - Press **STANDBY/ON**.
 - When this function is switched on, SAT appears on the display.
 - The DVD recorder is now prepared for recording.
- Factory setting is 'Off'.

Auto chapters

If autochapters is 'On', every five to six minutes a chapter marker (beginning of a new chapter) is inserted during recording. This enables easy navigation through a title during playback. In either case you can manually insert chapter markers afterwards. (See 'Managing disc content' - 'Edit in playback mode'.)

LPIEP rec mode

In long play or extended play recording mode you can select the 'Sport' setting to optimize the video recording for images that contain fast movements, like sports programmes. The setting does not influence high quality or standard play recording mode.

Factory setting is 'Standr'.

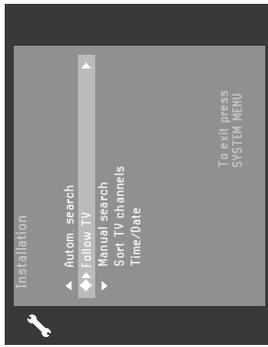
Installation

Auto TV Channel Search
Your DVD recorder will search for all TV channels. It stores channels in the sequence they are found. (See 'Installation - First time Set-up')

Note:
All channels stored so far will be erased.

Follow TV

With Follow TV you can programme the same channel sequence on the DVD recorder as on the TV set. This only functions if the recorder socket (EXT1) and the TV set are connected with a SCART cable. Additional equipment connected to socket EXT2, must be switched off.



- Press **OK**
- If the DVD recorder recognizes that the TV set has been connected with a SCART cable, 'TV' appears on the display.



- When 'TV' (no signal from TV set) appears on the display, the TV channels can not be allocated automatically. In this case read 'Manual TV channel search'.
- Select programme number '1' on the TV set.
- Confirm with **OK** on the remote control of the DVD recorder.
- The DVD recorder compares the TV channels on the TV set and the DVD recorder. If the channels match, this channel is stored at 'P01'.
- Wait until 'TV' appears and repeat the previous two steps for programme number 2 and the rest of the channels you want to store.
- To end, press **SYSTEM MENU**.

Manual TV channel search

You can perform a search to select and store TV channels manually. If the DVD recorder is connected via EasyLink, this function is not available.

- Press **SYSTEM MENU**.
- Select 'Installation'.
- Select 'Manual search'.
- In the line 'Channel/freq', select the display for: Freq.: frequency
- CH: channel
- S-CH: special channel
- If you know the frequency or channel of the desired TV channel, you can enter the data in line 'Entry/search', with the digit keys 0-9. If you don't know the frequency or channel of the TV channel of your choice, press > (right cursor) to start channel search.
- In the line 'Programme number', select the programme number you want, using < or > (left/right cursor) or digit keys 0-9.
- If you want to change the TV channel name, press the > (right cursor) key in line 'TV channel name'.
- Select the character you want to change with the < (left cursor) or > (right cursor) key.
- Change the character with the > (down cursor) or < (up cursor) key.
- Press **OK** to confirm.

This DVD recorder can receive HiFi sound transmissions in NICAM Stereo. However, if sound distortion occurs, due to poor reception, you can switch off NICAM:

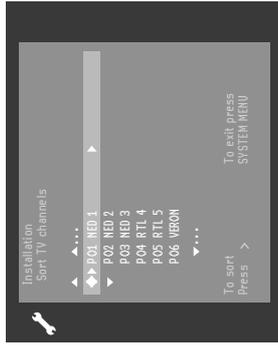
- In the line 'NICAM' select 'On' or 'Off' with the < (left cursor) or > (right cursor) key
- If you want to change the automatic TV channel setting, select the line 'Fine tuning'. With the < (left cursor) or > (right cursor) key you can vary the automatic TV channel setting.

Important: This re-tuning is only necessary and useful in special cases, e.g. when stripes appear on your TV screen when using a cable-TV system.

- Press **OK** to store the TV channel.
 - To end, press **SYSTEM MENU**.
- Connecting a decoder:**
- Switch on the TV set and select the programme number for the DVD recorder.
 - Select the TV programme you wish to link with the decoder function with **CH+** or **CH-**.
 - Press **SYSTEM MENU**
 - Select 'Installation'.
 - Select 'Manual search'.
 - Select 'Decoder'.
 - Select 'On' with < (left cursor) or > (right cursor).
 - Confirm with **OK**.
 - 'DECODER' appears on the display.
 - To end, press **SYSTEM MENU**.

Sort/Clear TV channels manually

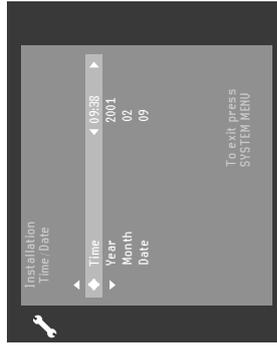
- If the DVD recorder is connected to the TV set with EasyLink or a similar system, manual sort cannot be executed. In all other cases, you can select.
- Press **SYSTEM MENU**.
- Select the line 'Installation'.
- Select the line 'Sort TV channels'.



- Select the TV channel to which you want to allocate a programme number (starting with P01.) with the < (up cursor) or > (down cursor) key and press the < (right cursor) key.
- Select the desired position with < or > (up/down cursor) key.
- To store, press **OK**.
- To end, press **SYSTEM MENU**.

Time/Date

To adjust 'Time', 'Year', 'Month' and 'Date' with the digit keys 0-9. Switch between fields with the < > (down/up cursor) keys.

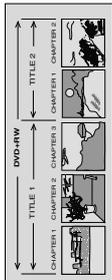


English

Recording

Before you start recording

Recordings on a DVD disc are called 'titles'. Every title consists of one or more chapters.



For more information about how to go to other titles or chapters see 'Playback - general features'.

Important:

Recordings on a DVD-RW disc are normally started from the position of the so-called disc pointer, i.e. the point where the last recording was stopped. From there on earlier recordings may be overwritten without notice, unless the disc is write protected. In this respect your DVD recorder behaves just like a Video Cassette Recorder.

If you want to make a recording without the risk of overwriting earlier recordings use the safe Record Function (see Manual Recording - Safe Record)

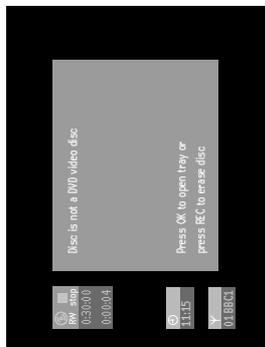
In the Index Picture Screen you can select the point where you want to start your recording. Use the ∇ (down up cursor) and \blacktriangleleft REVERSE/ \blacktriangleright FORWARD keys. You can see the current location on the disc bar, indicated by the arrow.

Your DVD recorder always checks the disc that you have inserted:

- ▶ When a DVD-RW disc is inserted on which recordings have been made, the Index Picture Screen is shown on your TV screen.
- ▶ If the inserted disc is a completely empty recordable disc, the message 'EMPTY DISC' appears on the display.
- ▶ If the inserted disc is a DVD-RW disc with a content that is not DVD-Video compatible (e.g. a data disc), a dialog box is shown with the option to erase or eject the disc. You can only record on this disc after erasing it with the RECORD key.

Note:

- On a disc containing PAL recordings, no NTSC recordings can be made and vice versa. On an empty disc, either type of recordings can be made.
- No recordings can be made from so-called 'psaudio-PAL' or PAL-60 sources.



- ▶ A disc can hold up to 48 titles (including empty titles). When this maximum is reached the on-screen message 'Too many titles' appears, if you want to make a new recording. You have to erase a title first next to an empty title. (See 'Managing Disc Content'.)

Manual recording

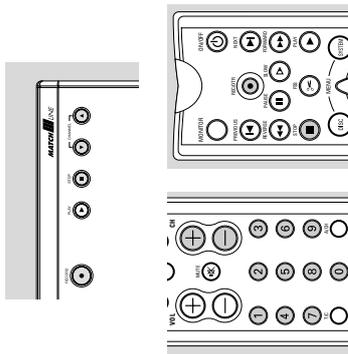
Checking input

Normally, the DVD recorder displays the contents of the disc on screen.

- ▶ Press MONITOR in order to switch to the internal tuner, or whichever other source is selected, if you want to check the input before starting a recording.
- ▶ On the TV screen, you will see the actual picture quality that you will get if you record: the video has been encoded and decoded again. This is why you will see a delay of about 1.5 seconds when using a 'live' source such as a camera.
- ▶ In monitor mode you can choose programme numbers directly with the digit keys 0-9 on the remote control.
- ▶ Press SELECT repeatedly to select the desired record mode.
- ▶ Press MONITOR again to go back to disc mode.

Recording

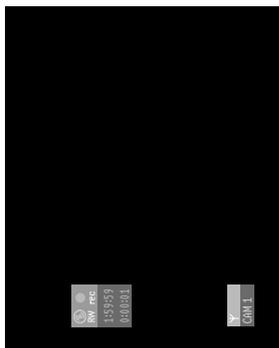
- ▶ Insert a recordable DVD-RW or DVD-R disc.
- ▶ Normally, the DVD recorder displays the contents of the disc on the screen.
- ▶ Use the MONITOR button to see the currently selected TV channel.
- ▶ Use CHANNEL ▲ or CHANNEL ▼ (on the recorder) or CH+ CH- (on the remote control) to select the programme number (programme name) from which you wish to record.
- ▶ When a TV channel transmits a channel name, it will be shown on the display.



The following programme numbers are provided for recording from external sources:

- 'EXT1': TV set via SCART 1 socket
- 'EXT2': for recording from external sources via SCART 2 socket
- 'EXT3': rear S-video
- 'EXT4': rear CVBS
- 'CAM1': front S-video (Y/C)
- 'CAM2': front Video (CVBS)

- ▶ Press RECORD (on the recorder) or REC/OTR (on the remote control).
- ▶ RECORD is shown on the display.
- ▶ The status box is shown on the screen for a few seconds.



- ▶ To bring back the status box during recording press SYSTEM MENU. Pressing SYSTEM MENU once more will remove the status box again.
- ▶ Press PAUSE to pause recording. You can resume recording by pressing PAUSE once more. The DVD recorder will make a seamless connection.
- ▶ Press STOP to stop recording. If you are recording from a camcorder watch the video output of the DVD recorder on the TV - instead of the camcorder viewer - to determine the right moment to stop.

- The Index Picture Screen is updated
- ▶ 'MENU UPDATE' is shown on the display
- After a short recording on a new DVD-RW disc, a few minutes will be needed to complete the formatting of the disc.

Safe Recording

When you start recording on a DVD-RW disc by briefly pressing the RECORD or REC/OTR key, a recording on DVD-RW will be made from the current position of the disc pointer. To prevent this do the following:

- Hold the RECORD key (on the recorder) or REC/OTR key (on the remote control) press for about two seconds until 'SAFE RECORD' appears on the display.
- The recorder automatically jumps to the end of the last title on the disc and starts recording.
- ▶ If no free space is left. The display will show 'DISC FULL'. Safe record is not possible then.

Recordings on DVD-RW are always automatically made after the last title on the disc.

Direct Record

With Direct Record you can start recording immediately from the programme selected on the TV set.

- Make sure 'DIRECT RECORD' is switched 'On'.
- (See record settings).
- On the TV set, select the programme number you want make the recording from.
- Make sure the DVD recorder is switched to standby.
- Press RECORD (on the recorder) or REC/OTR (on the remote control).

Notes :

- Don't select another programme number on your TV set until the 'EXIT' on the display of your DVD recorder disappears. This can take up to one minute.
- When 'NO TV' appears on the display, the programme number could not be found. The DVD recorder switches off automatically.
- If your loudspeakers are connected (via an amplifier / receiver) to your DVD recorder, the sound will be delayed relative to the TV picture when recording directly from the TV set.
- You can use Direct Record in combination with Safe Record.

Manual audio control

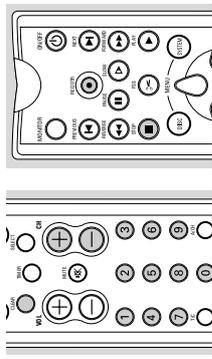
You can control the audio recording level of your DVD recorder manually.

- In monitor mode, press AUTO/MAN REC
- ▶ VOLUME on the DVD recorder.
- ▶ The display will show the current audio level and MANUAL appears.



- Adjust the recording level with **MANUAL** ▲ or ▼ on the DVD recorder, so that the 0 dB mark lights up during the loudest parts of the recording.
- You can switch back to automatic audio level control by pressing **AUTOMAN REC VOLUME** again.
 - The display will show the current disc position and **MANUAL** disappears.

Recording with automatic switch-off (OTR One-Touch Recording)



- Insert a recordable DVD+RW or DVD+R disc.
- Use **CHANNEL ▲** or **CHANNEL ▼** (on the recorder) or **CH+**, **CH-** (on the remote control) to select the programme number (programme name) from which you wish to record.
- Press **RECORD** (on the recorder) or **REC/OTR** (on the remote control) twice.
 - A recording will be made of 30 minutes.
 - The required end time of the recording is shown in the timer box on screen. The remaining recording time is shown on the display.



- Press **RECORD** or **REC/OTR** again to obtain a 30 minute increment.
- Shortly after pressing **REC/OTR**, OTR can be cancelled by pressing **CLEAR**.

Timer programming

The DVD recorder needs the following information for every programmed recording:

- the date on which the recording is to be made;
- the channel;
- the start and stop time of the recording;
- VPS/PDC on or off;
- the recording mode (HQ, SP, LP or EP).

The DVD recorder stores all the information mentioned above in a timer block. You can programme up to six timer blocks, one month in advance.

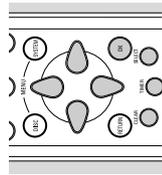
When you have programmed the timer, a red line on the disc bar (both on the display and on the Index Picture Screen) indicates what part of the disc will be overwritten by the programmed recording from the current disc position (on DVD+RW) or after the last title (on DVD+R).

When all timer blocks are full, the options timer programming and VIDEO Plus+ programming cannot be accessed. For clearing a timer block, see 'How to clear a timer block'.

What is VPS/PDC?

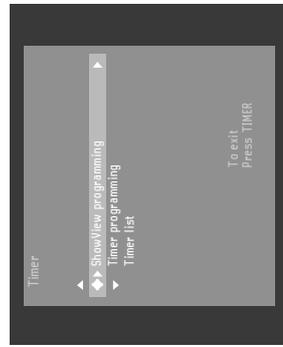
With 'VPS/PDC', the TV station controls the beginning and the length of the programmed recording. This means that the video recorder switches itself on and off at the right time even if a TV programme you have programmed begins earlier or finishes later than expected. Usually the start time is the same as the VPS/PDC time. If, however, in the TV guide, in addition to a TV programmes start time, a different VPS/PDC time is given, e.g.: '20:15 (VPS 20:14)', you must enter '20:14' as the start time exactly to the minutes. If you want to enter a time that differs from the VPS/PDC time, you must switch off VPS/PDC.

Timer programming with the VIDEO Plus+ system

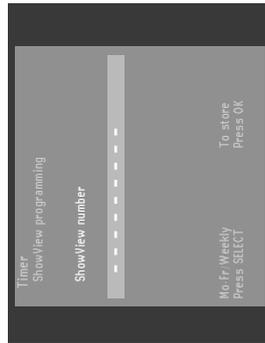


A PlusCode number is a number of up to nine digits, printed in most TV guides next to the start time of a TV programme. All the information required for a programming is contained encoded in the PlusCode programming number.

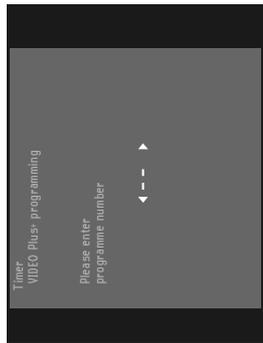
- Select **VIDEO Plus+ programming** with ▲ (up cursor) or ▼ (down cursor).



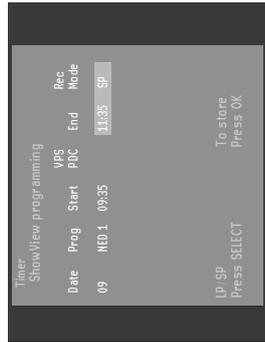
- Press ▷ (right cursor).



- Enter the entire PlusCode number (up to nine digits) printed in your TV guide next to the start time of a TV programme. If you made a mistake, you can correct it with **CLEAR**.
- Confirm with **OK**.
- If the VIDEO Plus+ system does not recognize the TV channel, the message **Please enter programme number** will appear on screen. Select the required programme number (programme name) with <◀> (left/right cursor) or the digit keys 0-9 and confirm with **OK**.

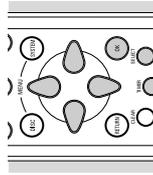


- The data will appear on the TV screen.
- Press ▷ (right cursor).
- Use **SELECT** to select the programming key at daily or weekly intervals. **Mo-Fr**: Recording at daily intervals from Mondays to Fridays inclusive. **Weekly**: Recording at weekly intervals on the same day of the week.
- Press ▷ (right cursor).
- Use **SELECT** to switch VPS/PDC on or off.
- When VPS/PDC is switched on, the start time is marked with an asterisk.
- Press ▷ (right cursor).
- Use **SELECT** to select the recording mode (HQ, SP, LP, EP).

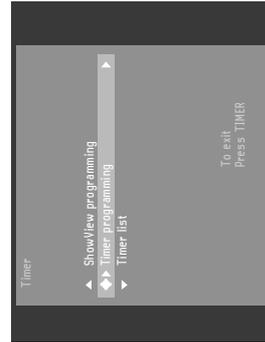


- Confirm with **OK**.
- The data has been stored in a timer block.
- To end, press **TIMER**.
- Make sure that you inserted a recordable disc. If you inserted a write-protected disc recording will be refused.
- Switch off with ⏻ **STANDBY/ON**.

Timer programming without the VIDEO Plus+ system

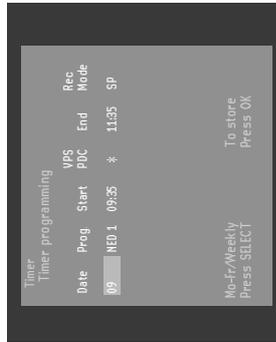


- Press **TIMER** on the remote control.
- Select **'Timer programming'** with ▲ (up cursor) or ▼ (down cursor).



- Press ▷ (right cursor).
- Enter the date with ▲ (up cursor) or ▼ (down cursor), or with the digit keys 0-9.

- If desired, select recording at daily or weekly intervals in the field **Date** with **SELECT**. **Mo-Fr**: Recording to be made from Mondays to Fridays inclusive. **Weekly**: Recording at weekly intervals on the same day of the week.
- Press **▷** (right cursor).
- Enter the programme number from which you want to record. If you want to record from an external source, select **EXT1**; **EXT2**; **EXT3**; **EXT4**; **CAM1** or **CAM2**, with **▷** (up down cursor).
- Press **▷** (right cursor).
- Enter the Start time with **▷** (up down cursor) or the digit keys **0-9**.
- After entering the Start time, use **SELECT** to switch VPS/PDC on or off. With most TV stations the VPS/PDC time is always the same as the start time.
- ▶ When VPS/PDC is switched on, the start time is marked with an asterisk.
- Press **▷** (right cursor).
- Enter the End time with **▷** (up down cursor) or the digit keys **0-9**.
- Use **SELECT** to choose the recording mode **HQ**; **LP**; **SP** or **FP**.
- If you made a mistake, you can go back with **◀** (left cursor).



- Confirm with **OK**.
- ▶ The data has been stored in a timer block.
- To end, press **TIMER**.
- ▶ Make sure that you inserted a disc without write protection. If you inserted a write-protected (locked) disc, recording will be refused.
- Switch off with **STANDBY/ON**.

Programming with 'NEXTVIEW Link'

This DVD recorder is equipped with the function 'NextView Link'. If your television is also equipped with this function, you can mark TV programmes on the television for programming. These TV programmes will automatically be transmitted to a timer block on the DVD recorder. If you clear the marking of the TV programme on the television, the corresponding timer block on the DVD recorder will also be cleared. For more information, read the instruction manual of your TV set.

If a timer setting is incorrect

The following warnings can be displayed in the timer menu:

Collision
recording programme overlaps with another recording programme.

Solution:

- ignore by pressing **TIMER**. The programme with the earlier start time will be recorded completely before the later programme starts.
- Edit one or both timers.
- Delete one of the recording programmes.

Please enter programme number

The VIDEO Plus+ system does not recognize the TV channel.

Solution:

- Select the required programme number (programme name) with **◀** or **▷** (left right cursor).
- Confirm with **OK**.

PlusCode number wrong

You entered an incorrect PlusCode number or the incorrect date.

Solution:

- Repeat the entry or end by pressing **TIMER**.

Weekend programming - not possible

Date was incorrectly entered. Daily programming can only be used for recordings to be made from Mondays to Fridays inclusive.

Memory full

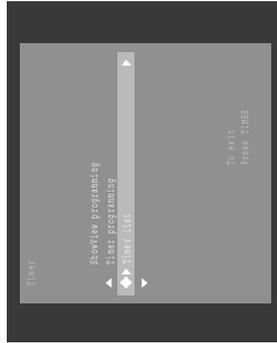
The maximum number of recording programmes is used.

Solution:

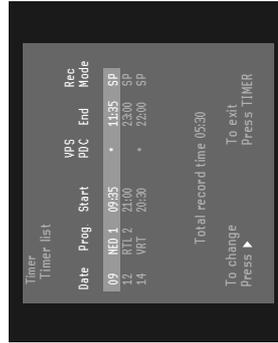
- Delete one of the recording programmes.

How to check or alter a timer block

- Press **TIMER** on the remote control.
- Select **'Timer list'** with **▷** or **◀** (down up cursor).

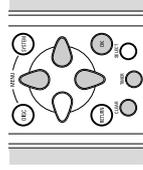


- Press **▷** (right cursor).



- Select the timer block you want to check or alter with **▷** or **◀** (down up cursor).
- Press **▷** (right cursor).
- Select what you want to check or alter with **◀** or **▷** (left right cursor).
- Alter data with **▷** or **◀** (down up cursor) or with the digit keys **0-9**.
- Confirm with **OK**.
- To end, press **TIMER**.
- Switch off by pressing **STANDBY/ON**.

How to clear a timer block



- Press **TIMER** on the remote control.
- Select **'Timer list'** with **▷** or **◀** (down up cursor).
- Press **▷** (right cursor).
- Select the timer block you want to clear with **▷** or **◀** (down up cursor).
- Press **CLEAR**.
- Confirm with **OK**.
- Switch off by pressing **TIMER**.

Playback

Playing a DVD+RW or DVD+R disc



- Insert a DVD+RW or DVD+R disc.
- If the inserted disc is write-protected, playback starts automatically otherwise the Index Picture Screen appears.
- Press **▶ PLAY**.
- Playback starts automatically from the point where it was stopped the last time the disc was played or recorded. If you want to start playback from the beginning of the disc, you can do so via the Index Picture Screen (see 'Index Picture Screen').
- If the disc is a new blank disc, the display will show 'EMPTY DISC'.
- To stop playback at any time, press **■ STOP**.
- You return to the Index Picture Screen.

Playing a pre-recorded DVD-Video disc



Some DVD discs are produced in a way that requires specific operation or allows only limited operation during playback. In these cases the recorder may not respond to all operating commands. When this occurs, please refer to the instructions in the disc inlay. When a [x] appears on the TV screen, the operation is not permitted by the recorder or the disc.

- Insert a pre-recorded DVD-Video disc. Make sure the label is facing up. If the disc is two-sided, make sure the label of the side you want to play is facing up.
- When 'autoresume' is set to 'On' (see 'User Preferences') playback starts automatically from the point where it was stopped, the last time the disc was played.
- When 'autoresume' is set to 'Off', the disc will play from the start of the disc. You can however resume play from the point at which you stopped, the last time the disc was played, by pressing **▶ PLAY** when [x] appears on screen.
- The currently playing title and chapter number are displayed on the recorder display. The elapsed time is shown also.

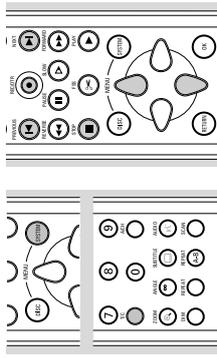
General features



Note:
Unless stated otherwise, all operations described are based on remote control operation. A number of operations can also be carried out via the system menu bar on the screen. (See 'System menu bar operation')

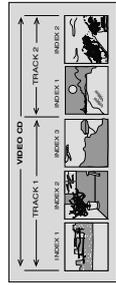
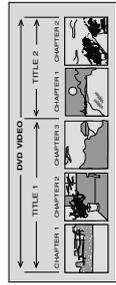
Moving to another title/track

When a disc has more than one title or track, you can move to another title as follows:



- Press **T/C**.
- Press **▶ NEXT** during play to step forward to the next title.
- Press **◀ PREVIOUS** during play to return to the beginning of the current title. Rapidly press **◀ PREVIOUS** twice to step back to the previous title.
- To go directly to any title or track, enter the title number using the numerical keys **0-9**.

Note:
- If the number has more than one digit, press the keys in rapid succession.
- If the system menu bar is on screen, make sure the **T** icon is selected.



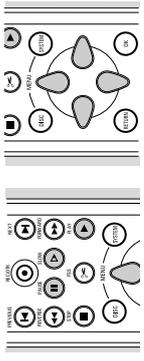
Moving to another chapter/index

When a title on a disc has more than one chapter or a track has more than one index, you can move to another chapter/index as follows:

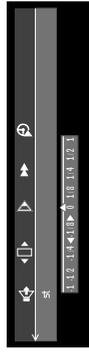
- Press **▶ NEXT** during play to select the next chapter/index.
- Press **◀ PREVIOUS** during play to return to the beginning of the current chapter/index. Rapidly press **◀ PREVIOUS** twice to step back to the previous chapter/index.
- To go directly to any chapter or index, enter the chapter or index number using the numerical keys **0-9**.

Note:
- If the number has more than one digit, press the keys in rapid succession.
- If the system menu bar is on screen, make sure the **C** icon is selected.

Slow Motion

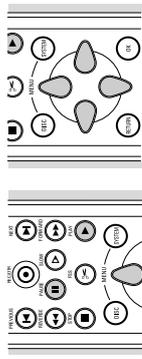


- Select **▶ (Slow motion)** in the system menu bar.
- Use the **▽ (down cursor)** key to enter the slow motion menu.
- The recorder will now go into pause mode.



- Use the **△ (left-right cursor)** keys to select the required speed: **'1'**, **'1/2'**, **'1/4'** or **'-1/8'** (backward); **'1.8'**, **'1/4'**, **'1/2'** or **'1'** (forward).
- Select **'1'** to play at normal speed again.
- If **PAUSE** is pressed, the speed will be set to **'0'**.
- Press **▶ PLAY** to exit slow motion mode.
- Press **△ (up cursor)** to delete the slow motion menu. You can also select Slow Motion speeds by using the **▶ SLOW** key on the remote control.

Still Picture and Step Frame

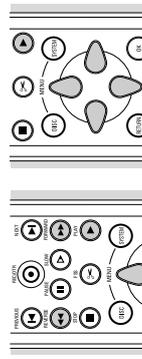


- Select **◀▶** (picture by picture) in the system menu bar.
- Use the **▽** (down cursor) key to enter the picture by picture menu.
- The recorder will now go into pause mode.

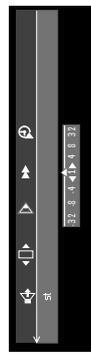


- Use **◀▶** (left/right cursor) keys to select previous or next picture.
 - Press **▶** **PLAY** to exit picture by picture mode.
 - Press **▲** (up cursor) to exit the picture by picture menu.
- You can also step forward by using the **|| PAUSE** repeatedly on the remote control.

Search



- Select **▶** (Fast motion) in the system menu bar.
- Use the **▽** (down cursor) keys to enter the fast motion menu.



- Use the **◀▶** (left/right cursor) keys to select the required speed: **·32'**, **·8'** or **·4'** (backward); **·4'**, **·8'**, **·32'** (forward).
 - Select **1** to play at normal speed again.
 - Press **▶** **PLAY** to exit fast motion mode.
 - Press **▲** (up cursor) to delete the fast motion menu.
- To search forward or backward through different speeds, you can also press **◀◀ REVERSE** or **▶▶ FORWARD** again.

Scan



- Plays the first 10 seconds of each chapter/index on the disc.
- Press **SCAN**.
 - To continue play at your chosen chapter/index, press **SCAN** again or press **▶** **PLAY**.

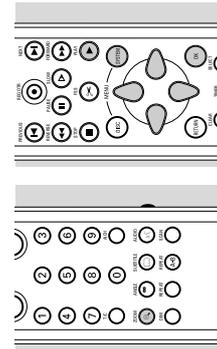
Time search

- The Time Search function allows you to start playing at any chosen time stamp.
- Select **⌚** (Time Search) in the system menu bar.
 - Press **▽** (down cursor).
 - The recorder will now go into pause mode.
 - A time entry box appears on the screen showing the elapsed playing time of the current disc.

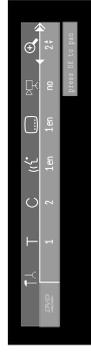


- Use the digit keys **0-9** to enter the required start time. Enter hours, minutes and seconds in the box.
- Each time an item has been entered, the next item will be highlighted.
- Press **OK** to confirm the start time.
- The time entry box will disappear and play starts from the selected time position.

Zoom



- The Zoom function allows you to enlarge the video image and to pan through the enlarged image.
- Select **🔍** Zoom in the system menu bar.
 - Press **▽** **Δ** (down/up cursor) to activate the Zoom function and select the required zoom factor: 1.33 or 2 or 4.
 - The recorder will go into pause mode.
 - The selected zoom factor appears below the Zoom icon in the system menu bar and **Press OK to pan** appears below the system menu bar.



- The picture will change accordingly.
- Press **OK** to confirm the selection.
- The panning icons appear on the screen: **▽** **▶** **◀** (down/up right/left cursor) and **OK**.
- Use the **▽** **▶** **◀** (down/up right/left cursor) keys to pan all over the screen.
- When **OK** is pressed only the zoomed picture will be shown on the screen.
- If you wish to zoom at any moment, press **🔍** Zoom and select the required zoom factor as described above.
- Press **▶** **PLAY** to exit zoom mode.

Repeat



- DVD Discs - Repeat chapter/title/disc REPEAT.**
- To repeat the currently playing chapter, press **REPEAT**.
 - **CHAPTER** appears on screen.
 - To repeat the currently playing title, press **REPEAT** a second time.
 - **TITLE** appears on screen.
 - To repeat the entire disc, press **REPEAT** a third time.
 - **DISC** appears on screen.
 - To exit repeat mode, press **REPEAT** a fourth time.
- Video CDs - Repeat track/disc REPEAT.**
- To repeat the currently playing track, press **REPEAT**.
 - **TRACK** appears on screen.
 - To repeat the entire disc, press **REPEAT** a second time.
 - **REPEAT** appears on screen.
 - To exit repeat mode, press **REPEAT** a third time.

Repeat A-B



- To repeat or loop a sequence in a title:
- Press **REPEAT A-B** at your chosen starting point;
 - **A-B** appears on screen.
 - Press **REPEAT A-B** again at your chosen end point;
 - **A-B** repeat appears on screen, and the repeat sequence begins.
 - To exit the sequence, press **REPEAT A-B**.

Special DVD-Video features

Menus on the disc

For titles and chapters, selection menus may be included on the disc. The DVD's menu feature allows you to make selections from these menus. Press the appropriate numerical key; or use the $\nabla \Delta \triangleright \triangleleft$ (down up right left cursor) keys to highlight your selection, and press OK.

Title menus



- Press DISC MENU .
 - ▶ If the current title has a menu, this appears on the screen. If no menu is present in the title, the disc menu will be displayed.
- The menu can list camera angles, spoken language and subtitle options, and chapters for the title.
- To exit the title menu, press DISC MENU again.

Note: Most DVD discs do not have separate disc and title menus.

Disc menu



If a DVD-Video disc has separate disc and title menus, you can navigate to the disc menu as follows:

- Press T/C followed by DISC MENU .
- ▶ The disc menu is displayed.
- To remove the disc menu, press DISC MENU again.

Camera Angle

If the disc contains sequences recorded from different camera angles, the angle box appears, showing the number of available angles, and the angle being shown. You can then change the camera angle if you wish.



- Use the $\nabla \Delta$ keys to select the required angle in the angle box.
- To go to any angle directly, enter the angle number using the numerical keys 0-9
 - ▶ After a small delay, play changes to the selected angle. The angle box remains displayed until multiple angles are no longer available.

Changing the audio language



- Select A (Audio) in the system menu bar.
- Press A AUDIO or $\nabla \Delta$ (down up cursor) repeatedly to step through the different languages.
- You can enter the required language number directly using the numerical keys 0-9



Subtitles

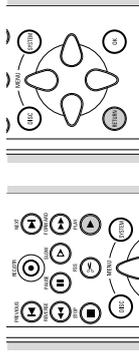


- Select S (Subtitle) in the system menu bar.
- Press S SUBTITLE or $\nabla \Delta$ (down up cursor) repeatedly to step through the different subtitles, or to switch the subtitles off.
- You can enter the required subtitle number directly using the numerical keys 0-9



Special VCD features

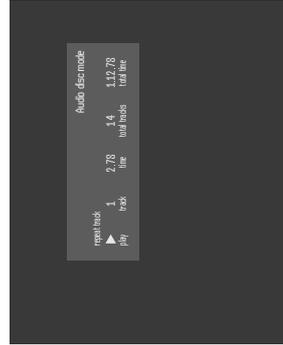
Playback Control (PBC)



- Make sure PBC is switched 'On'. See 'User Preferences-features settings'.
- Load a (Super) Video CD with PBC and press \triangleright PLAY.
- The PBC menu appears on screen.
- Go through the menu with the keys indicated on the TV screen until your chosen passage starts to play. If a PBC menu consists of a list of titles, you can select a title directly.
- Enter your choice with the numerical keys 0-9.
- Press RETURN to go back to the previous menu.

Playing an audio CD

- Insert the disc.
- After loading the disc, playback starts automatically.
- If the TV set is on, the Audio CD screen appears.
- During play, the current track number and its elapsed playing time will be shown on the screen and the recorder display.



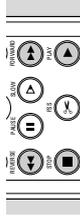
- To stop play at any time, press \blacksquare STOP.
- The number of tracks and the total playing time will be shown on the screen and the recorder display.

Pause



- Press II PAUSE during play.
- To return to play, press \triangleright PLAY.

Search

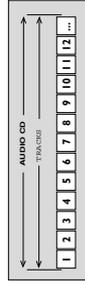


- To search forwards or backwards through the disc at 4x normal speed, press FF REVERSE or FF FORWARD.
- ▶ Search begins.
- To step up to 8x normal speed, press FF REVERSE or FF FORWARD again.
- ▶ Search goes to 8x speed, and the sound is muted.
- To return to 4x normal speed, press FF REVERSE or FF FORWARD again.
- If the TV set is on, search speed and direction are indicated on the screen each time FF REVERSE or FF FORWARD is pressed.
- To end the search, press \triangleright PLAY or \blacksquare STOP as desired.

Moving to another track



- Press P NEXT during play to step forward to the next track.
- Press N PREVIOUS during play to return to the beginning of the current track. Rapidly press N PREVIOUS twice to step back to the previous track.
- To go directly to any track, enter the track number using the numerical keys 0-9.

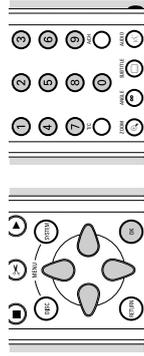


Access control

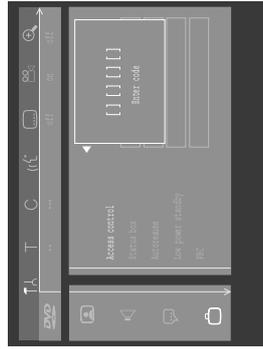
Child Lock (DVD and VCD)

When activating Child lock, only discs that are authorised can be played without PIN code. The recorder memory maintains a list of 50 authorized ('Child safe') disc titles. A disc will be placed in the list when 'Play Always' is selected in the 'Child protect' dialog. Each time a 'Child safe' disc is played it will be placed on top of the list. When the list is full and a new disc is added, the least recently used will be removed from the list.

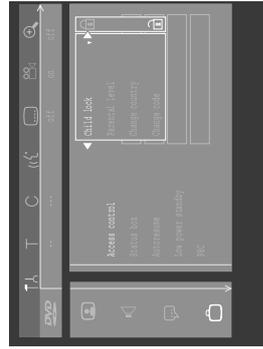
Activating/deactivating the child lock



- Select 'Access control' in the features menu using ∇/Δ (down/up cursor) and press \triangleright (right cursor).



- Enter a 4-digit PIN code of your own choice using the digit keys 0-9.
- Enter the code a second time.
- Move to 'Child lock' using ∇/Δ (down/up cursor).
- Move to \triangleright (right cursor) key.



Repeat track/disc



- To repeat the currently playing track, press **REPEAT**.
- **Repeat track** appears on screen.
- To repeat the entire disc, press **REPEAT** a second time.
- **Repeat disc** appears on screen.
- To exit repeat mode, press **REPEAT** a third time.

Repeat A-B



- To repeat or loop a sequence:
- Press **REPEAT A-B** at your chosen starting point;
- **Repeat A-B** appears on screen.
- Press **REPEAT A-B** again at your chosen end point;
- **Repeat A-B** appears on the display, and the repeat sequence begins.
- To exit the sequence, press **REPEAT A-B** again.

Scan



- Plays the first 10 seconds of each track on the disc.
- Press **SCAN**.
- To continue play at your chosen track, press **SCAN** again or press **PLAY**.

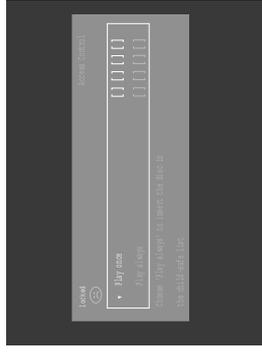
- Select ∇/Δ using ∇/Δ (down/up cursor).
- Press **OK** or \leftarrow (left cursor) to confirm and press **SYSTEM MENU** again to exit the menu.
- Now unauthorized discs will not be played unless the 4-digit code is entered.
- Select \square to deactivate the Child Lock.

Notes:

Reconfirmation of the 4-digit PIN code is necessary when: The code is entered for the very first time (see above); The code is changed (see 'Changing the 4-digit code'); The code is cancelled (see 'Changing the 4-digit code'); Both Child Lock and Parental Control are switched Off and the code is requested.

Authorizing discs when Child Lock is activated

- Insert the disc.
- The 'Child protect' dialog will appear. You will be asked to enter your secret code for 'Play once', or 'Play always'. If you select 'Play once', the disc can be played as long as it is in the recorder and the recorder is in the On position. If you select 'Play always', the disc will become Child safe (authorized) and can always be played even if the Child lock is set to 'On'.



Note: Double sided DVD discs may have a different ID for each side. In order to make the disc 'Child safe', each side has to be authorized. Multi volume VCD disc may have a different ID for each volume. In order to make the complete set 'Child safe', each volume has to be authorized.

Securing discs

- Insert the disc.
- Playback starts automatically.
- Press **STOP** while \odot is visible.
- \odot will appear and the disc is now banned i.e. it is not Child safe any longer.

Parental Level (DVD-Video only)

Movies on pre-recorded DVD discs may contain scenes not suitable for children. Therefore, discs may contain 'Parental Control' information which applies to the complete disc or to certain scenes on the disc.

These scenes are rated from 1 to 8 and alternative, more suitable scenes are available on the disc. Ratings are country dependent. The 'Parental Control' feature allows you to prevent discs from being played by your children or to have certain discs played with alternative scenes.

Activating/Deactivating Parental Control

- Select **Access control** in the features menu using ∇/Δ (down/up cursor) and press \triangleright (right cursor).
- Enter your 4-digit PIN code using the digit keys **0-9**. If necessary, enter the code a second time.
- Move to **Parental level** using ∇/Δ (down/up cursor).
- Move to the Value Adjustment bar using \triangleright (right cursor).



- Use the ∇/Δ (down/up cursor) keys or the numerical keys **0-9** on the remote control to select a rating from 1 to 8 for the disc inserted.
Rating 0 (displayed as '-'):

Parental Control is not activated. The disc will be played in full.

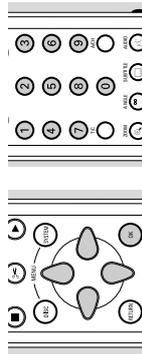
Ratings 1 to 8 (1 = *childsafe* - 8 = *adults only*):

The disc contains scenes not suitable for children. If you set a rating for the recorder, all scenes with the same rating or lower will be played. Higher rated scenes will not be played unless an alternative is available on the disc. The alternative must have the same rating or a lower one. If no suitable alternative is found, play will stop and the 4-digit code has to be entered.

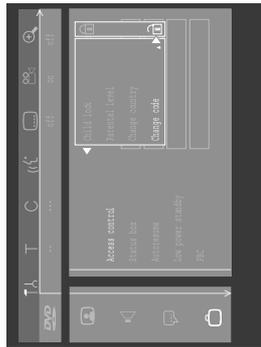
- Press **OK** or \triangleleft (left cursor) to confirm and press **SYSTEM MENU** again to exit the menu.

42. ACCESS CONTROL

Changing the 4-digit code



- Select **Access control** in the features menu using ∇/Δ (down/up cursor) and press \triangleright (right cursor).
- Enter the old code.
- Move to **Change code** using ∇ (down cursor).



- Press \triangleright (right cursor).
- Enter the new 4-digit PIN code.
- Enter the code a second time and reconfirm with **OK**.
- Press **SYSTEM MENU** to exit the menu.

Note:

If you forget your code, press **STOP** four times while in the access control PIN code box and exit with **OK**. Access control is now switched off. You can then enter a new code as described above.

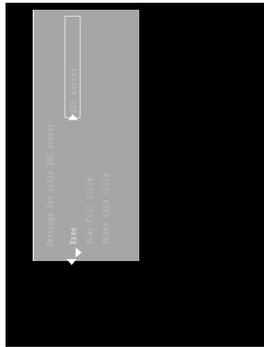
Managing disc content

Title settings

For each title on a DVD+RW or DVD-R disc the default settings can be changed to your personal preference in the title settings menu.

Changing the title name

- In the Index Picture Screen, select the required title with ∇/Δ (down/up cursor).
- Press \triangleright (right cursor) to enter the title settings menu.



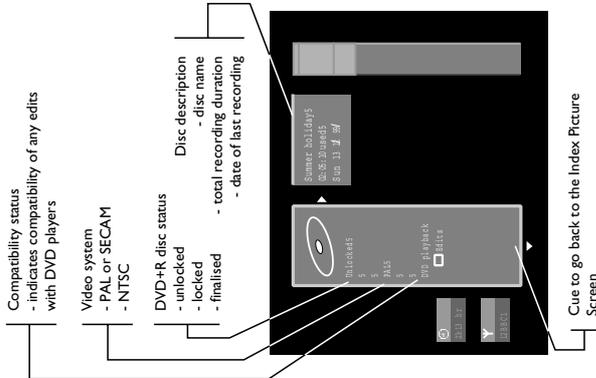
- Press **OK** to confirm.
- 'Erasing title...' is shown until the action is completed.
- After the title has been erased, the Index Picture Screen will show an empty space instead. If there was an empty space in front of or behind this title, then these are combined into one empty space. Empty spaces of less than one minute will not be shown.

On DVD+R titles can also be erased but the space occupied cannot be used anymore. During finalisation erased titles are removed from the Index Picture Screen.

Disc Info Screen

- When on the Index Picture Screen, press **■ STOP**.
- You are now on Title 1.
- Press Δ (up cursor).
- You enter the Disc Info Screen.
- Press ∇ (down cursor) to exit the Disc Info Screen.

The Disc Info Screen contains the following information:



- Enter the new name. A name may contain a maximum of 64 characters.
- Use $\triangleleft/\triangleright$ (left/right cursor) for the position of the characters. Use ∇/Δ (down/up cursor) to change characters.
- Use **SELECT** to toggle between capitals and lower case characters.
- Use **CLEAR** to erase a character.
- Confirm by pressing **OK**.

Play full title

- In the Index Picture Screen, select the required title with ∇/Δ (down/up cursor).
 - Press \triangleright (right cursor) to enter the title settings menu.
 - Select **Play full title**
- When this item is selected the title will be played in full, including hidden chapters. Follow the instructions on the screen. (See 'managing disc content - Favorite Scene Selection')

Erasing a title

- You may simply erase a title on DVD+RW by recording over it, but if you want to erase the whole title instantly, do the following:
- In the Index Picture Screen, select the required title with ∇/Δ (down/up cursor).
 - Press \triangleright (right cursor) to enter the title settings menu.
 - Select **Erase this title**.
 - The message 'This will completely erase this title'. Press **OK** to confirm' is shown.

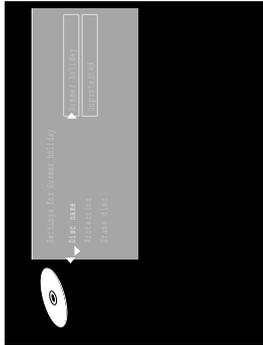
Disc Settings

For each DVD+RW or DVD-R disc the settings can be changed to your personal preference in the disc settings menu.

- In the Disc Info Screen press \triangleright (right cursor).
- You will now enter the 'disc settings' menu.

Changing the Disc Name

- In the Disc Info Screen press \triangleright (right cursor).
- You will now enter the 'disc settings' menu.



- Enter the new name. A name may contain a maximum of 64 characters.
- Use $\triangleleft/\triangleright$ (left/right cursor) for the position of the characters. Use ∇/Δ (down/up cursor) to change characters.
- Use **SELECT** to toggle between capitals and lower case characters.
- Use **CLEAR** to erase a character.
- Confirm by pressing **OK**.

Protection of recordings

- In the Disc Info Screen press \triangleright (right cursor).
- You will now enter the 'disc settings' menu.
- Select **Protection** and press \triangleright (right cursor).
- Select **Protected** with ∇/Δ (down/up cursor).
- Press **OK** on the remote control to confirm.
- No further changes can be made to the disc. It will also disable most title/disc settings options, as well as the complete edit menu.
- Future editing is only possible after resetting the Protection feature to **Unprotected** again.

Erasing a disc

This option is only available for DVD+RW discs that are not erases-protected.

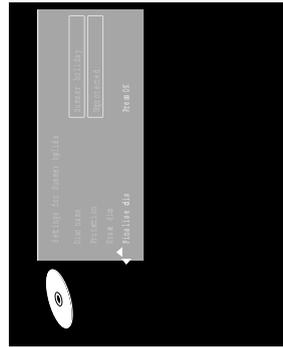
- In the Disc Info Screen press \triangleright (right cursor).
- You will now enter the disc settings' menu.
- Select **Erase disc** and press **OK**.
- The message 'This will erase all titles' is displayed.

- Press **OK** to confirm or \triangleleft (left cursor) to cancel.
- 'Erasing disc' is shown until the action is completed.
- After the disc has been erased, the Index Picture Screen will show the free space on the disc.

Finalising a DVD+R disc

While a DVD+RW disc can be played instantly on most DVD players, a DVD+R disc can be played only on the DVD recorder until it is finalised. After finalisation no changes can be made to the disc anymore.

- In the Disc Info Screen press \triangleright (right cursor).
- You will now enter the 'disc settings' menu.



- Select 'Finalise disc' and press **OK** to confirm.
- 'Finalise disc' is shown until the action is completed.
- After finalisation the Index Picture Screen will appear.

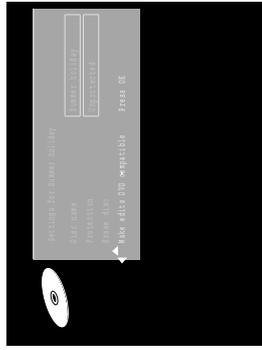
If the DVD+R disc was recorded on a different brand of DVD recorder you may not be able to access the Disc Settings screen. In this case you can use the 'Finalise disc' option in the features menu of the user preferences menu.



Making your edits DVD-compatible

If one or more titles have been edited (see 'Favourite Scene Selection'), then the edits will play on your DVD recorder, but a DVD player may show the original versions instead of the edits. You can prepare your DVD+RW discs so that also a DVD player will show the edited version. This is not possible with DVD+R discs.

- If the Disc Settings menu shows the option 'Make edits DVD compatible', select this option. If the menu does not show this option, then your DVD+RW disc is already compatible, and no conversion is needed.



- Press **OK** on the remote control to confirm.
 - The messages 'This will take ...' and 'Press OK to confirm' will appear to indicate how long the action will take.
- Press **OK** on the remote control to confirm.
 - 'PROCESSING...' and a progress bar are shown until the action is completed.

Favourite Scene Selection

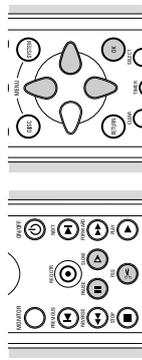
The basic function of any edit operations is to improve accessibility and handling of your recordings. For instance, scenes you do not want to see during playback (e.g. commercials during a movie) can be marked as chapters and made hidden. During playback you will see your recording without the hidden chapters as one sequence.

Note:
In between the scenes the picture may freeze for a short moment.

Each title consists of chapters. With the FSS menu any chapter can be made hidden or made visible again. Normally, during recording, chapter markers are inserted automatically every five to six minutes (this setting can be changed in the record settings menu). After the recording is finished, you can manually add and remove chapter markers via the FSS menu. Both automatically generated and manually inserted chapter markers can be removed.

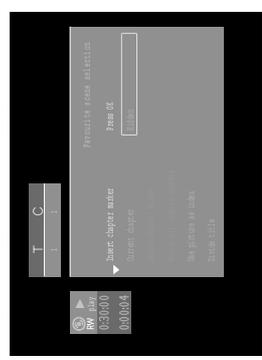
After editing, the modified version of a title is the default playback version. The original can be accessed via the 'Play Full title' option in the title settings menu. Other DVD players may still play the original. To guarantee that the edited version will play on these DVD players, choose 'Make edits DVD-compatible' in the disc settings menu (only available on DVD+RW discs).

Calling up the FSS menu



- Play the title you want to edit.
- Press the **FSS** key on the remote control.
- The video image is overlaid with a transparent edit menu. Title and chapter information appear in an information box at the top of the screen.

Note:
The Favourite Scene Selection menu may disappear after about five minutes if you do not edit any information.



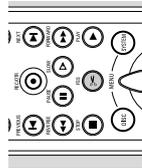
- Use **▽** or **△** (down up cursor) to toggle through the menu's functions.

Inserting chapter markers

- In play mode press **FSS** on the remote control, to call up the FSS menu.
- Select 'Insert chapter marker'.
- Press **OK** on the remote control to insert a marker.

The maximum number of chapter markers is 99. When this maximum is reached, the on-screen message 'Too many chapters' appears. You have to delete some, before inserting new chapter markers.

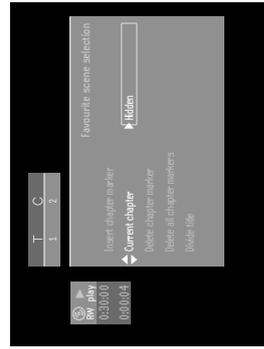
During recording you can add chapter markers by pressing **FSS** on the remote control. The message 'Chapter marker inserted' will appear on the screen.



Hiding chapters

Initially all chapters are visible. You can hide chapters or make them visible again on playback. In FSS mode however hidden chapters are displayed in a dimmed mode.

- In play mode press **FSS** on the remote control to call up the FSS menu.



- Select 'Current chapter', with **▽** or **△** (down up cursor).
- Select 'Visible' or 'Hidden' with the **▷** (right cursor) key.
- You can toggle between 'Visible' and 'Hidden' directly from any line in the FSS menu with the **SELECT** key on the remote control.

Deleting chapter markers

You can combine a chapter with the previous chapter in the current title by deleting the chapter at the beginning of the current chapter.

- In play mode press **FSS** on the remote control to call up the FSS menu.
 - Select 'Delete chapter marker'.
 - Press **OK** on the remote control to confirm
 - 'Deleting marker' will appear.
- You can delete all chapter markers (manually and automatically generated) in the current title.
- In play mode press **FSS** on the remote control to call up the FSS menu.
 - Select 'Delete chapter markers'.
 - Press **OK** on the remote control to confirm
 - 'Deleting markers' will appear.

Changing the index picture

You can define the current video frame as a miniature picture to be used for this title's entry in the Index Picture Screen.

- In play mode press **FSS** on the remote control to call up the FSS menu.
- Select 'New index picture'.
- You can use **IF PAUSE** and/or **▷ SLOW** to accurately choose the desired picture.
- Press **OK** on the remote control to confirm.
- 'Updating menu' will appear.

Troubleshooting

If it appears that the DVD recorder is faulty, first consult this checklist. It may be that something has been overlooked. Under no circumstances attempt to repair the system yourself; this will invalidate the warranty. Look for the specific symptom(s). Then perform only the actions listed to remedy the specific symptom(s).

Symptom	Remedy
The recorder does not respond to the remote control	<ul style="list-style-type: none"> The remote control may be configured for a second DVD recorder. Hold SELECT+1 pressed simultaneously to revert to DVD recorder 1. Aim the remote control directly at the sensor on the front of the recorder. Avoid all obstacles which may interfere with the signal path. Inspect or replace the batteries.
Keys on the DVD recorder do not work	<ul style="list-style-type: none"> The DVD recorder may still be in Virgin mode. See 'First time set-up: virgin mode'. Otherwise disconnect and reconnect the DVD recorder from the mains. If this does not solve the problem, check if the remote control still works. If so, the recorder is probably in trade mode. Disconnect the recorder from the mains and reconnect it while holding ▲ OPEN/CLOSE and ■ STOP pressed.
No picture	<ul style="list-style-type: none"> Check if the TV set is switched on. Check the video connection. When the DVD recorder is connected to the TV set via SCART, you may not see the picture at the DVD recorder after selecting the correct programme number on your TV set when a timer recording takes place. This way, you can still view another device (e.g. a satellite receiver). To view the DVD recorder press TV/DVD on the remote control.
Distorted picture distorted sound	<ul style="list-style-type: none"> Check the disc for fingerprints and clean with a soft cloth, wiping from centre to edge. Sometimes a small amount of picture distortion may appear. This is not a malfunction.
Recorder does not play disc	<ul style="list-style-type: none"> Ensure the disc label is upwards and that the right disc type is inserted. Clean the disc. Check if the disc is defective by trying another disc. Check if the region code of the disc matches the region code of the recorder. (pre-recorded DVD discs only). See 'playing a pre-recorded DVD-Video disc'. Check if Child Lock is activated.
Distorted sound from HiFi amplifier	<ul style="list-style-type: none"> Check to make sure that no audio connections are made to amplifier phono input. Check to make sure that analogue input of the amplifier is not connected to the digital output of the DVD recorder.
Distorted or black and white picture with DVD or Video CD disc	<ul style="list-style-type: none"> The disc format is not according to the TV set used (PAL/NTSC).
No audio at digital output	<ul style="list-style-type: none"> Check the digital connections. Check the settings menu to make sure that the digital output is set to on. Check if the audio format of the selected audio language matches your receiver capabilities.
Recorder does not respond to all operating commands during playback of a DVD-Video disc	<ul style="list-style-type: none"> Some operations are not permitted by the disc. Refer to the instructions in the disc inlay.

Append recording

This function is only available on DVD+RW discs.



If you want to append a video recording to an earlier recorded title, do the following.

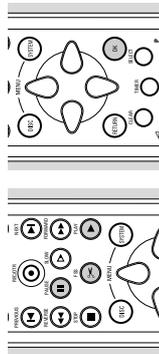
- On the Index Picture Screen, select the title to which you want to add a video recording.
- Press **▶ PLAY**.
- At the point where you want to append the title press **■ PAUSE**.
- To monitor the video input you may press **MONITOR**.
- Press **REC/OVR** (on the recorder) or **REC/OVR** (on the remote control).

The video recording will now be appended from this point. Video material beyond this point is overwritten. This may include titles following the current title.

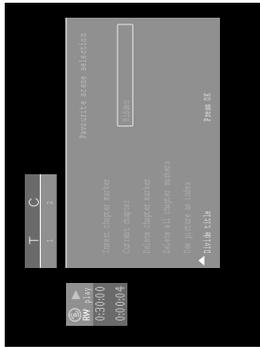
Any remaining video material that is not overwritten, which may include the last part of the original title, is maintained. You can access these titles from the Index Picture Screen.

Dividing a title

On a DVD+RW disc you split one title into two separate titles. (On DVD+R this is not possible.)



- On the Index Picture Screen, select the title you want to divide.
- Press **▶ PLAY**.
- Go to the point where you want to divide the title and press **■ PAUSE**.
- Press **⏏ FSS**.
- The Favourite Scene Selection menu is shown.
- Select 'Divide title'.



- Press **OK** on the remote control to confirm.
- 'Dividing title...' is shown until the action is completed. This divide operation cannot be undone.

The Index Picture Screen will show two titles instead of one. Both will have the same name. If you want to change the name, you can do so in the title settings menu. For one of the two resulting titles, a new index picture is created.

If you want to divide one title into more than two titles, use the above procedure several times.

The recorder does not record timer programme

- Make sure that the recorder is switched to standby before the timer starts.

No new title can be recorded

- Check if the maximum number of titles has been reached (message: 'too many titles' on screen). If so, delete a title next to a free space.
- Check if the disc is write protected. If so, unlock the disc in the disc settings menu (message: 'Disc locked' on screen).
- Check if the (DVD+R) disc has been finalized. If so, no new titles can be recorded anymore.

Service codes on the display

- Clean the disc. The recording was most probably done correctly.

'Disc warning' message on screen

- A write error has occurred, but it could be corrected. No user action is required.

'Disc error' message on screen

- A write error has occurred from which the recorder could not recover. Inspect the disc and clean it if necessary (refer to 'Introduction - Cleaning discs' for cleaning instruction). Record (overwrite) again over the same part of the disc to see if the problem is solved

Disc errors

- A disc might be corrupted because of dust, scratches or fingerprints. If the disc cannot be accessed anymore, use the back-up disc erase procedure to repair it. Proceed as follows:
 1. Clean the disc.
 2. Put disc in the drawer (do not close the tray).
 3. Press and hold **CLEAR** for several seconds until the tray closes.

Two languages are 'mixed' when recording from a stereo VCR

- When the TV set does not automatically detect the dual-language signal, use left/right audio balance on the TV set to amplify the one or the other language.

The disc cannot be erased because the Index Picture Screen does not appear

1. Open the tray while leaving the disc in.
2. Hold **CLEAR** pressed for around 5 seconds until the tray closes. The disc is technically not yet erased but you can start a new recording like on a blank disc.

The Index Picture Screen does not appear but the titles on the disc can still be played

- Take out the disc. Clear the disc. Insert the disc. Choose 'Adapt to own disc format' (See 'User Preferences - Features').

A DVD player shows the Index Picture Screen but does not react to the ► PLAY key

- Press **■ STOP** to exit the Index Picture Screen, then press ► **PLAY**.

A DVD+RW disc does not play on a certain DVD player

- There are DVD Players that will not play recordings made with a DVD Recorder. With a special procedure the recorder will solve this problem for some players. Proceed as follows:
 1. Put the disc in the drawer (do not close the tray)
 2. Press and hold the **2** key on the remote control for several seconds until the tray closes. The disc is now modified.
 3. If the change has no effect, you may perform the same procedure with the **3** key on the remote control.

Note :

Modifying the disc can solve the problem for a specific player model, but playback in other DVD players may no longer be possible. It is therefore recommended to use this procedure carefully and only when needed.

- To revert the disc to the original state, follow the same procedure with the **1** key on the remote control.

System limitations

DVD+RW and DVD+R discs may not play on certain DVD Video players.

A DVD+RW video disc that has been recorded on a different type or brand of recorder can be played, but may not provide all features commonly available to DVD+RW discs, such as the on-screen disc bar, the disc settings menu, the title settings menu, and editing. Refer to 'Adapt disc format'. If the disc is write-protected, the status cannot be changed.

When using manual recording, the DVD recorder will warn before adapting the format of the disc or removing non-video data. When using timer recording however, the DVD recorder will always start to record, unless the disc is write-protected. Menus, edits and other data recorded on a different device (e.g. a PC) may be lost.

Because of the Variable Bit Rate, a title map take up less or more space than the overwritten title, even though the duration is the same. As a result, a part of the original title may remain, or a part of the next title may be lost. The maximum deviation is five minutes.

After a power interruption during recording, the Index Picture Screen will not match with the actual video content on the disc. The last recorded title may be lost.

Diagnosis programme

If the recorder is still faulty you can start the Diagnosis Programme in the recorder.

You can operate the Diagnosis Programme by following the instructions step by step.

Instructions



- Unplug the power cord of the recorder.
- Press the ► **PLAY** key and keep them pressed while you plug the recorder.
 - ▶ On the display the message 'BUSY' appears together with a counter. This counter indicates the termination of the test when zero is reached.
 - ▶ After a few minutes the message on the local display changes over from 'BUSY' to 'FRET' or to 'PRESS'.
 - ▶ If the message 'FRET' appears on the display, there is apparently a failure in your recorder and your recorder should be repaired.
- Consult your dealer or the Philips Customer Care Centre for the nearest Service Repair Shop in your country. The phone number is given in your warranty booklet.
- If the message 'PRESS' appears on the display, there is apparently no failure in your recorder, in this case the failure can be caused by incorrect interpretation of the operating instructions or a wrong disc is used or your recorder is not correctly connected. In this case you should consult your dealer or the Philips Customer Care Centre for further assistance in solving the problem.
- If the problem remains, then consult your Philips Customer Care Centre.

English

Glossary

This section explains most important terms, abbreviations, and acronyms used in this document.

Term	Explanation
AC-3	Audio Coding 3, also known as Dolby Digital. Multi-channel digital audio compression system from Dolby Labs.
A/V	Audio/Video
Chapter	A part of a title.
Disc Bar	A graphical representation of the contents of a (DVD+RW) disc.
Disc Pointer	An arrow indicating the current playback/recording position on the DVD+RW disc, displayed on the disc bar.
DTS	Digital Theater System. A high-end Multi-channel audio compression format.
DV	Digital Video. A camcorder format for high-quality video, different from MPEG. It is converted into MPEG 2 Video when recorded on DVD+RW.
DVD	Digital Versatile Disc
DVD+R	DVD+Recordable. The write-once disc standard used by the DVD recorder.
DVD+RW	DVD+ReWritable. One of the disc standards used by the DVD recorder.
EasyLink	If your TV set and your video recorder are equipped with this feature, they can exchange information to adjust certain settings to each other, such as the TV channel order and other user preferences.
FSS	Favorite Scene Selection. see 'Managing disc content'.
i-LINK	Also known as 'FireWire' and 'IEEE 1394'. A cable for transfer of high-bandwidth digital signals, as used by Digital Video camcorders.
Index Picture Screen	A screen that gives an overview of a DVD+RW disc, with 'index pictures' that each represent a recording.
MPEG	Motion Picture Experts Group. A collection of compression systems for digital audio and video.
NextView Link	A system that enables easy programming of a video recorder via a TV set. Also see EasyLink.
NICAM	System for reception of digital stereo TV sound.
NTSC	See TV system.
OSD	On-screen Display. The 'user interface' by which you can control the DVD recorder via the TV screen.
OTR	One-Touch Recording. With this feature you can easily start a recording (by pushing just one button) and select the switch-off time in intervals of 30 minutes.

PAL See TV system.

PBC Playback Control. A special feature on a VCD 2.0 or Super VCD disc that enables interactive use.

PCM Pulse Code Modulation. A digital audio encoding system.

PDC Program Delivery Control

RGB Red-Green-Blue. A top-quality video connection where red, green and blue components of a video signal are carried through separate wires.

SCART cable Also known as Euro-AV cable. This standard cable is an easy way to connect various AV devices and televisions. In addition to audio and video it can carry control signals.

SECAM See TV system.

S-video Sometimes also called S-VHS or Super-VHS. A high-quality video connection standard.

SVCD Super Video Compact Disc.

Title It is the name given to the unit of recording on the disc. A title, typically, represents one recording.

TruSurround A system for simulating Multi-channel sound reproduction via a two-channel set-up, by SRS Labs, Inc.

TV system There are various systems for transmitting television signals, for example PAL, PAL-I, PAL-BG, SECAM, SECAM-DK, NTSC, etc. The TV system is country dependant.

VCD Video Compact Disc

VCR Video Cassette Recorder

VIDEO Plus+ A system by which you can easily program a timer recording by entering a nine-digit VideoPlus+ number found next to the programme description in most TV guides.

VPS Video Programming System

English

4. Mechanical Instructions

4.1 Service Positions

4.1.1 Front

Front



Figure 4-1

4.1.2 DVIO board

To put the DVIO board in a service position, an extender board must be used. This extender board can be ordered with codenumber 3104 128 07770.

DVIO Extender

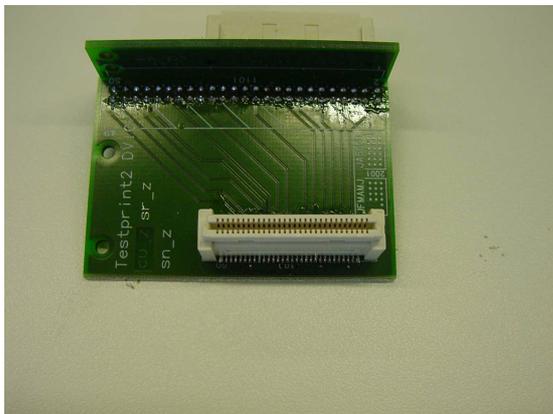


Figure 4-2

DVIO 1

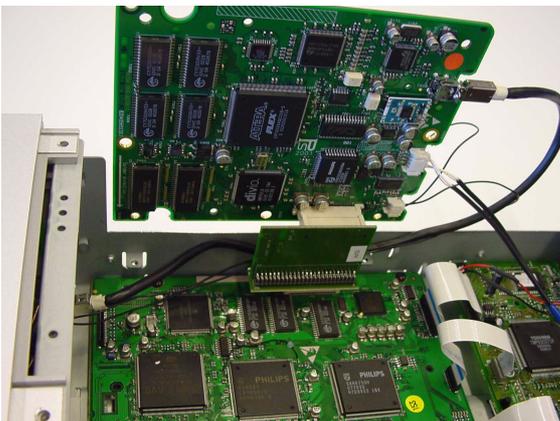


Figure 4-3

DVIO 2



Figure 4-4

4.1.3 Digital board

After demounting of DVIO board, the top side of the digital board is in reach. To reach the bottom side of the digital board, the DVDR module must be demounted together with the digital board. Connected to each other, the assembly can be set in a service position. In this position, the bottom side of the digital board and the servo board are in reach to be serviced.

Digital 1



Figure 4-5

Digital 2



Figure 4-6

4.1.4 Analog board

To put the analog board in service position, demount the assembly of analog board and backplate as follows:

1. Remove 3 screws from the backplate to the frame
2. Remove the screw from the backplate to the mains inlet of the power supply
3. Remove the screw of the analog board to the frame
4. Release the snaps of the 4 spacers of the analog board to the frame.

Turn the assembly of the backplate and the analog board against the loader.

Analog Europe



Figure 4-7

Analog NAFTA



Figure 4-8

4.2 Exploded View of the Front Assembly

Front EV

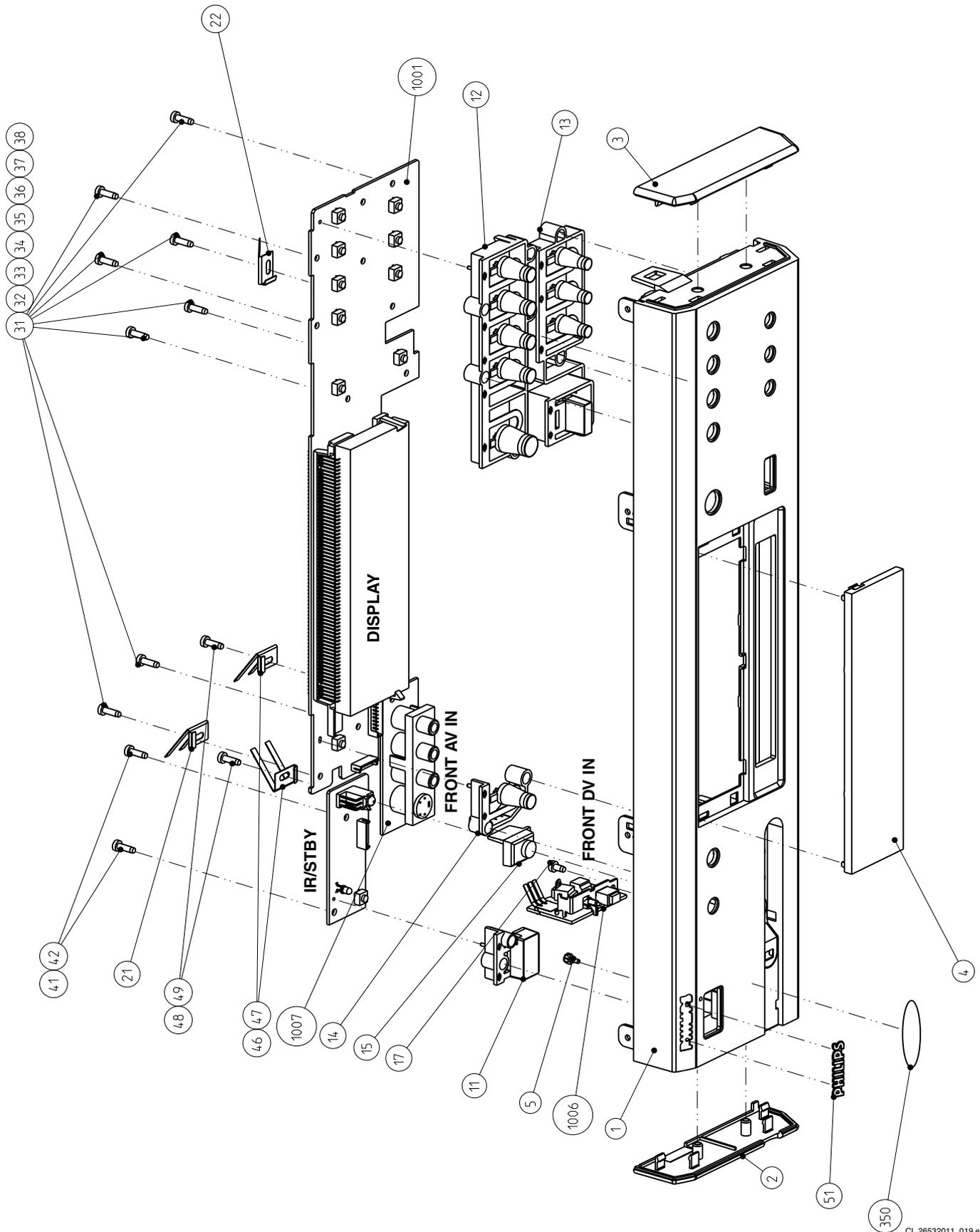
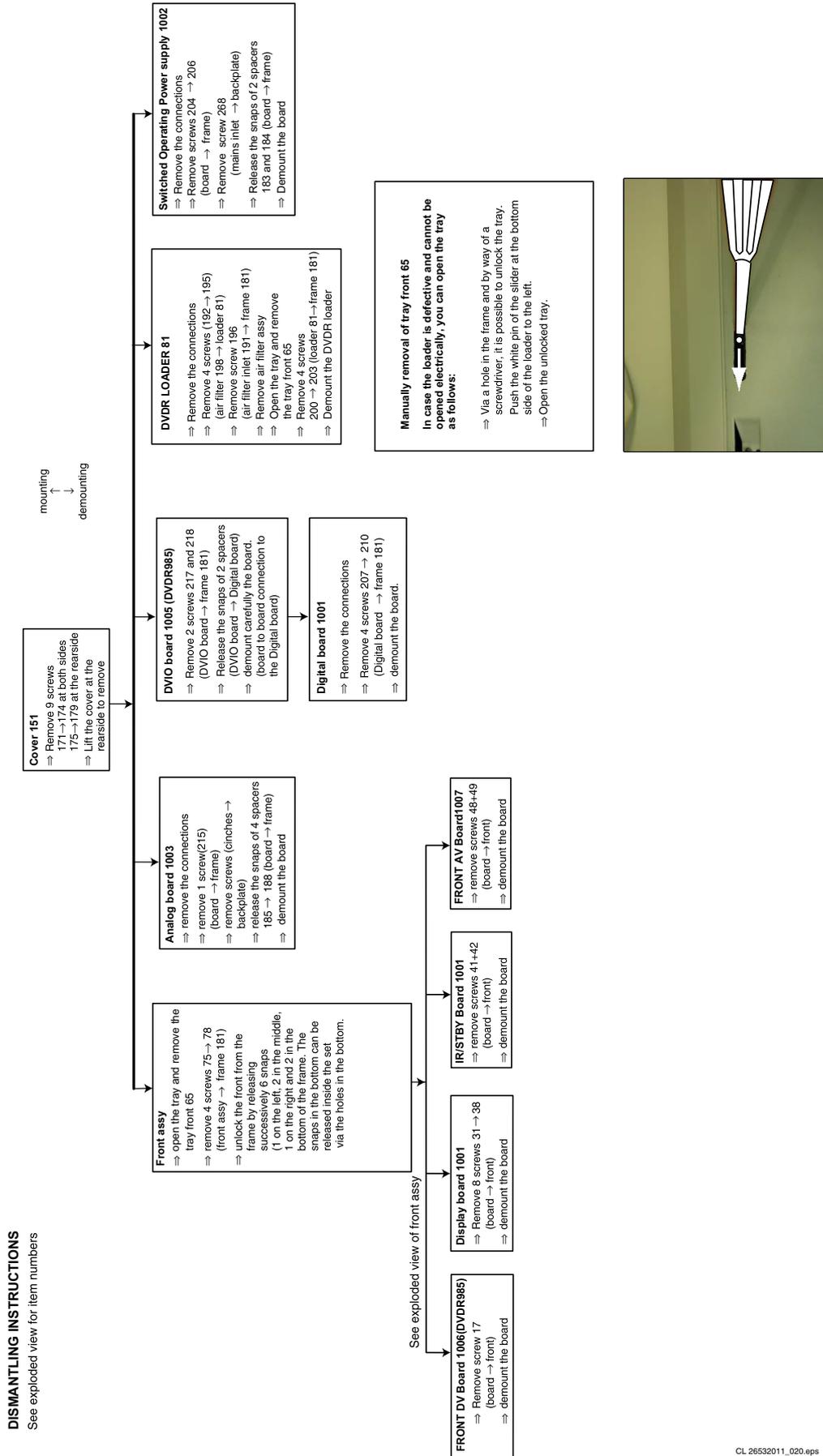


Figure 4-9

4.3 Dismantling Instructions

Dismantling Instructions



DISMANTLING INSTRUCTIONS
See exploded view for item numbers

Figure 4-10

4.4 Exploded View of the Set

Complete Set EV

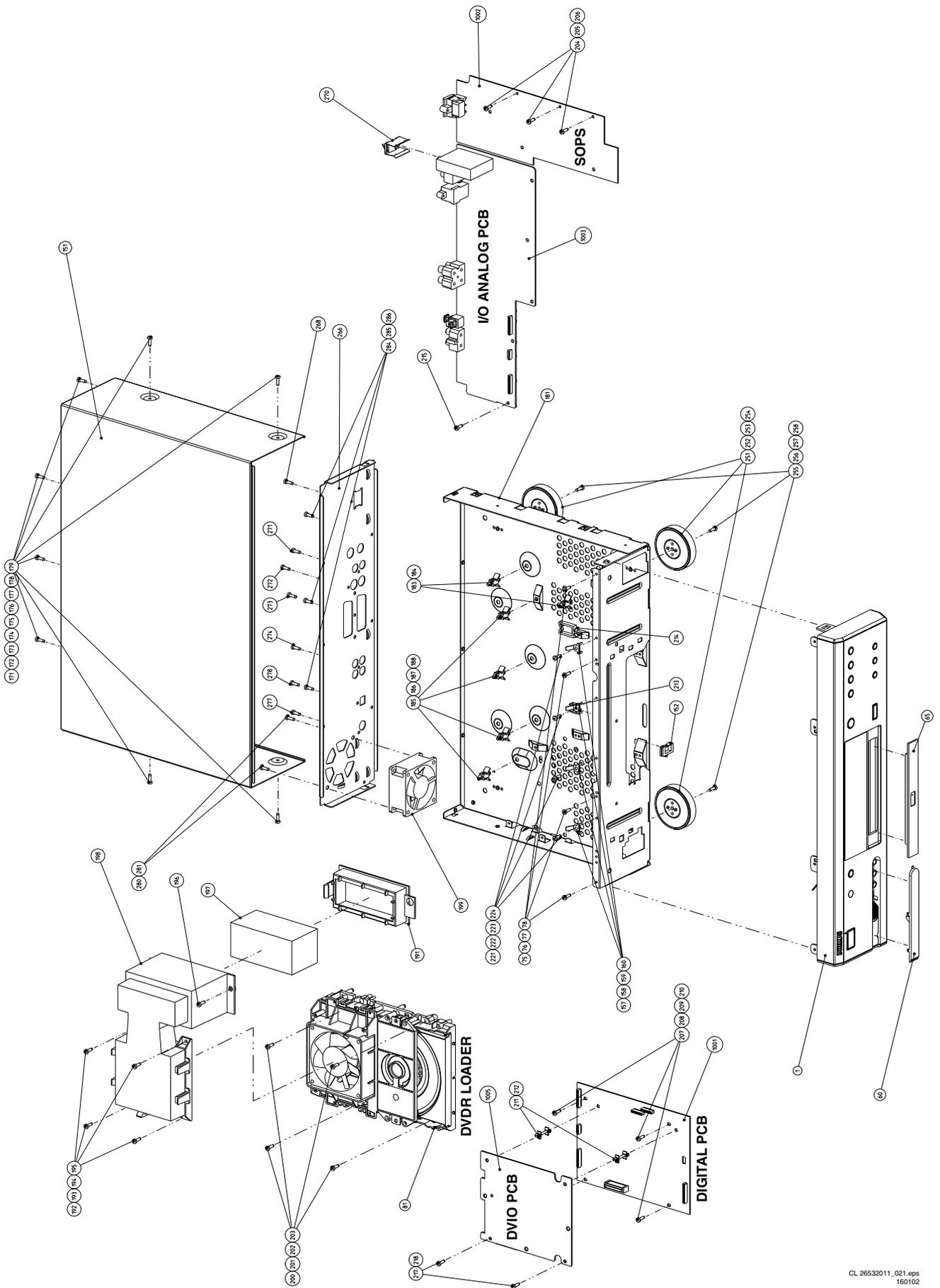


Figure 4-11

5. Diagnostic Software and Faultfinding Trees

Due to the complexity of the DVD recorder, the time to find a defect in the recorder can become long. To reduce this time, the recorder has been equipped with Diagnostic and Service software (DS). The DS offers functionality to diagnose the DVDR hardware and tests the following:

- Interconnections between components
- Accessibility of components
- Functionality of the audio and video paths

This functionality can be accessed via several interfaces:

1. End user/Dealer script interface
2. Player script interface
3. Menu and command interface

5.1 End User/Dealer Script Interface

5.1.1 Description

The End user/Dealer script interface gives a diagnosis on a stand alone DVD recorder; no other equipment is needed. During this mode, a number of hardware tests (nuclei) are automatically executed to check if the recorder is faulty. The diagnosis is simply a "fail" or "pass" message. If the message "FAIL" appears on the display, there is apparently a failure in the recorder. If the message "PASS" appears, the nuclei in this mode have been executed successfully. There can be still a failure in the recorder because the nuclei in this mode don't cover the complete functionality of the recorder.

5.1.2 Contents

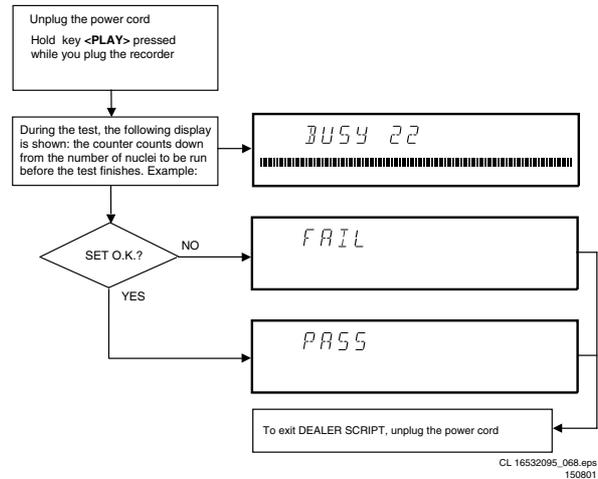


Figure 5-1

The End use/Dealer script executes all diagnostic nuclei that do not need any user interaction and are meaningful on a standalone DVD recorder. The nuclei called in the End user/Dealer script are the following:

Counter	Nucleus	Name	Description
22	104	HostdSdramWrR	checks all memory locations of the 4MB SDRAM
21	106	HostdDramWrR	checks all the DRAM connected to the microprocessor of the digital board
20	123	HostdI2cNvram	checks the data line (SDA) and the clock line (SCL) of the I2C bus between the host decoder and NVRAM
19	202	SAA7118I2c	checks the interface between the Host I2C controller and the AVENC SAA7118 Video Input Processor
18	200	VideoEncI2c	checks the interface between the host I2C controller and Empress SAA6752
17	207	AudioEncI2c	checks the I2C connection between the host decoder and Empress SAA6752
16	204	AudioEncAccess	tests the HIO8 interface lines between the host decoder and the audio encoder
15	203	AudioEncSramAccess	checks the access of the SRAM by the audio encoder (address and data lines).
14	205	AudioEncSramWrR	tests the SRAM connected to the audio encoder
13	206	AudioEncInterrupt	tests the interrupt line between the host decoder and the audio encoder
12	300	VsmAccess	checks whether the VSM interrupt controllers and DRAM are accessible
11	303	VsmInterrupt	checks both interrupt lines between the VSM and the host decoder
10	302	VsmSdramWrR	tests the entire SDRAM of the VSM
9	1400	Clock11_289MHz	switches the A_CLK of the micro clock to 11.2896 MHz
8	1401	Clock12_288MHz	switches the A_CLK of the micro clock to 12.288 MHz
7	601	BeS2Bengine	checks the S2B interface with the Basic Engine by sending an echo command
6	500	DisplayEcho	checks the interface between the host processor and the slave processor on the display board
5	700	AnalogueEcho	checks the interface between the host processor and the microprocessor on the analogue board
4	711	AnalogueNvram	checks the NVRAM on the analogue board
3	706	AnalogueTuner	checks whether the tuner on the analogue board is accessible
2	901	LoopAudioUserDealer	This nucleus tests the components on the audio signal path - The analogue board - The audio encoder - The VSM On the analogue board the audio is internally looped back to the digital board
1	906	LoopVideoUserDealer	Nucleus for testing the components on the video signal system path: - The VIP - The video encoder - The VSM - The host decoder - The analogue board On the analogue the video signal is internally routed back to the digital board.

5.2 Player Script Interface

5.2.2 Structure of the Player Script

5.2.1 Description

The Player script will give the opportunity to perform a test that will determine which of the DVD recorder's modules are faulty, to read the error log and to perform an endurance loop test. To successfully perform the tests, the DVD recorder must be connected to a TV set.

To be able to check results of certain nuclei, the player script expects some interaction of the user (i.e. to approve a test picture or a test sound). Some nuclei (e.g. nuclei that test functionality of the DVDR module) require that a DVD+RW disc is inserted.

Only tests within the scope of the diagnostic software will be executed hence only faults within this scope can be detected.

The player script consists of a set of nuclei testing the hardware modules in the DVD recorder: the Display PWB, the Digital PWB, the Analogue In/Out PWB and the DVDR module.

Nuclei run by the player test need some user interaction; in the next table this interaction is described. The player test is done in two phases:

- **Interactive tests:** this part of the player test depends strongly on user interaction and input to determine nucleus results and to progress through the full test. Reading the error log information can be useful to determine any errors that occurred recently during normal operation of the DVD player.
- **The loop test** will perform the same nuclei as the dealer test, but it will loop through the list of nuclei indefinitely.

STEP	DESCRIPTION	NUCLEUS
1	Press OPEN/CLOSE and PLAY at the same time and POWER ON the recorder to start the playerscript	2
2	The local display shows FPSEGMENTS . Press PLAY to start the test. First the <i>starburst pattern</i> is lit, then the <i>horizontal segments</i> are lit, followed by the <i>vertical segments</i> and the last test is <i>light all segments</i> test. After each of the 4 tests the user has to confirm that the correct pattern was lit. Press PLAY to confirm that the correct pattern was lit (four times if the FPSEGMENTS test was successful). Press RECORD to indicate that the correct pattern was not successfully lit. Press STOP to skip this nucleus.	502
3	The local display shows FPLABELS . Press PLAY to start the test. Press PLAY to confirm that all labels are lit. Press RECORD to indicate that not all labels are lit. Press STOP to skip this nucleus.	503
4	The local display shows FPLIGHT ALL . Press PLAY to start the test. Press PLAY to confirm that everything was lit. Press RECORD to indicate that not all patterns are lit. Press STOP to skip this nucleus.	520
5	The local display shows FPLED . Press PLAY to start the test. Press PLAY to confirm that the led is lit. Press RECORD to indicate that the led is not lit. Press STOP to skip this nucleus.	504
6	The local display shows FPFLAP OPEN . Press PLAY to start the test. Press PLAY to confirm that the flap has opened. Press RECORD to indicate that the flap did not open. Press STOP to skip this nucleus.	522
7	The local display shows FPKEYBOARD . Press PLAY to start the test. Attention all keys have to be pressed to get a positive result! Press PLAY for more than one second to confirm that all the keys were pressed and shown on the local display. If not all the keys were pressed, a FAIL message will appear on the local display. Press RECORD for more than one second to indicate that not all keys were pressed and shown on the local display. Press STOP for more than one second to skip this nucleus.	505
8	The local display shows FPREMOTE CONTROL . Press PLAY to start the test. Press PLAY to confirm that a key on the remote control was pressed and shown on the local display. Only one key has to be pressed to get a successful result. Press RECORD to indicate that the key on the remote control was pressed but not shown on the local display. Press STOP to skip this nucleus.	506
9	The local display shows FPDIMMER . Press PLAY to start the test. Press PLAY to confirm that the text on the local display was dimmed. Press RECORD to indicate that the text on the local display was not dimmed. Press STOP to skip this nucleus.	518
10	The local display shows FPBEEPER . Press PLAY to start the test. Press PLAY to confirm that the beeper on the front panel sounded. Press RECORD to indicate that the beeper on the front panel did not sound. Press STOP to skip this nucleus.	514
11	The local display shows FPFLAP CLOSE . Press PLAY to start the test. Press STOP to skip this nucleus.	523
12	The local display shows ROUTE VIDEO . Press PLAY to start the test. Press STOP to skip this nucleus.	712
13	The local display shows ROUTE AUDIO . Press PLAY to start the test. Press STOP to skip this nucleus.	713
14	The local display shows COLOUR-BAR ON . Press PLAY to start the test. Press STOP to skip this nucleus.	120

STEP	DESCRIPTION	NUCLEUS
15	The local display shows PINK NOISE ON . Press PLAY to start the test. Press STOP to skip this nucleus.	115
16	The local display shows PINK NOISE OFF . Press PLAY to start the test. Press STOP to skip this nucleus.	116
17	The local display shows SINE ON . Press PLAY to start the test. Press STOP to stop the sine. Press STOP to skip this nucleus.	117
18	The local display shows COLOUR-BAR OFF . Press PLAY to start the test. Press STOP to skip this nucleus.	121
19	The local display shows BERESET . Press PLAY to start the test. Press STOP to skip this nucleus.	603
20	The local display shows BETRAY OPEN . Press PLAY to start the test. Press STOP to skip this nucleus.	616
21	The local display shows BETRAY CLOSE . Press PLAY to start the test. Press STOP to skip this nucleus.	615
22	The local display shows BEWRITE READ . Press PLAY to start the test. Press STOP to skip this nucleus.	617
23	The local display shows BETRAY OPEN . Press PLAY to start the test. Press STOP to skip this nucleus.	616
24	The local display shows BETRAY CLOSE . Press PLAY to start the test. Press STOP to skip this nucleus.	615
25	The local display shows READ ERRORLOG . Press PLAY to start the test. Press STOP to skip this nucleus. If the player test succeeded, the user/dealer script will start in an endless loop. If the player test failed, the local display will display FAIL and the error code	633

Remark

In case of failure, the display shows " FAIL XXXXXX ". The description of the shown error code can be retrieved in the survey of Nuclei Error Codes (paragraph 5.4). Once an error occurs, it is not possible to continue the player script. Unplug the set and restart the player script. By pressing the STOP key, it is possible to jump over the failure and to continue the player script.

Player Script

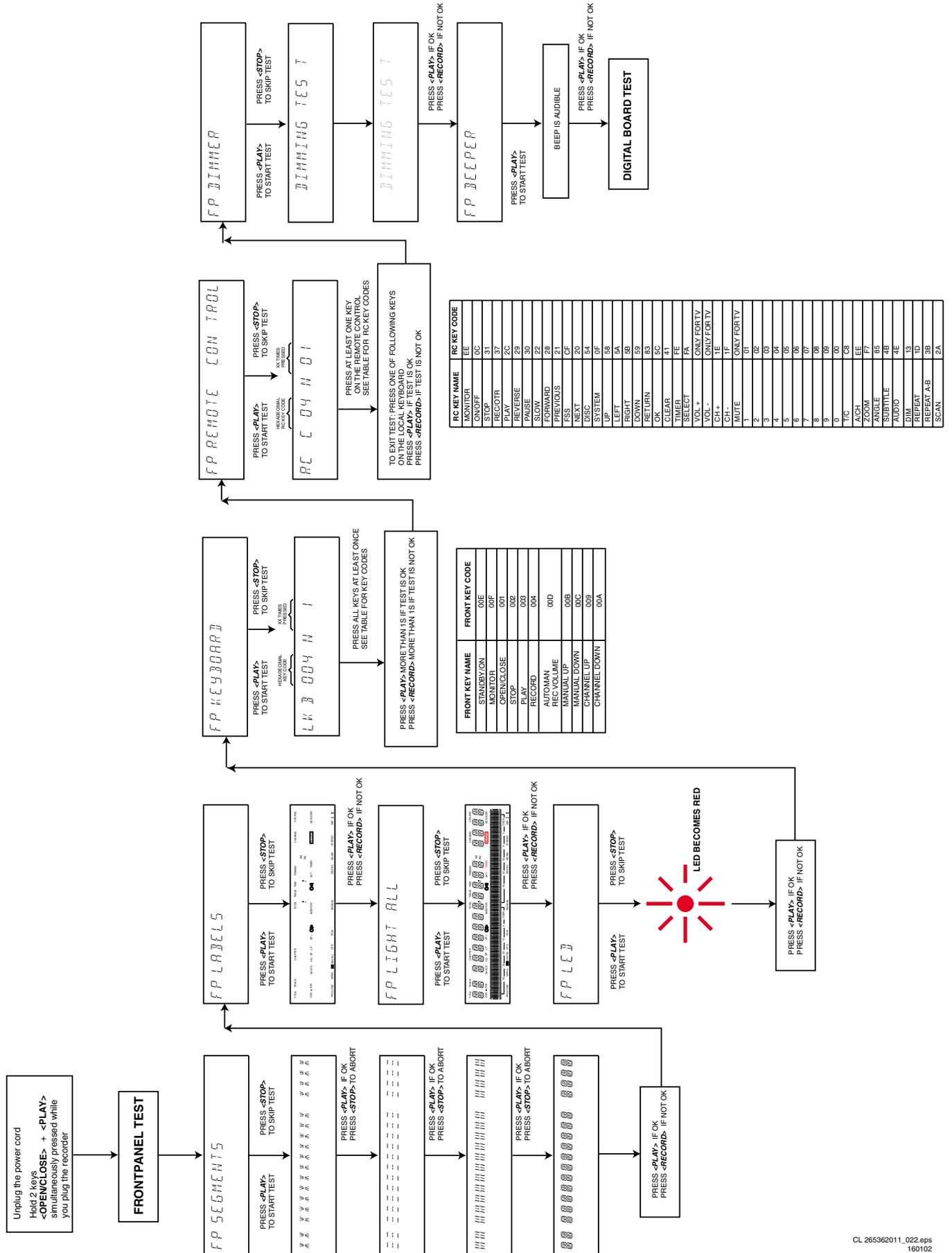
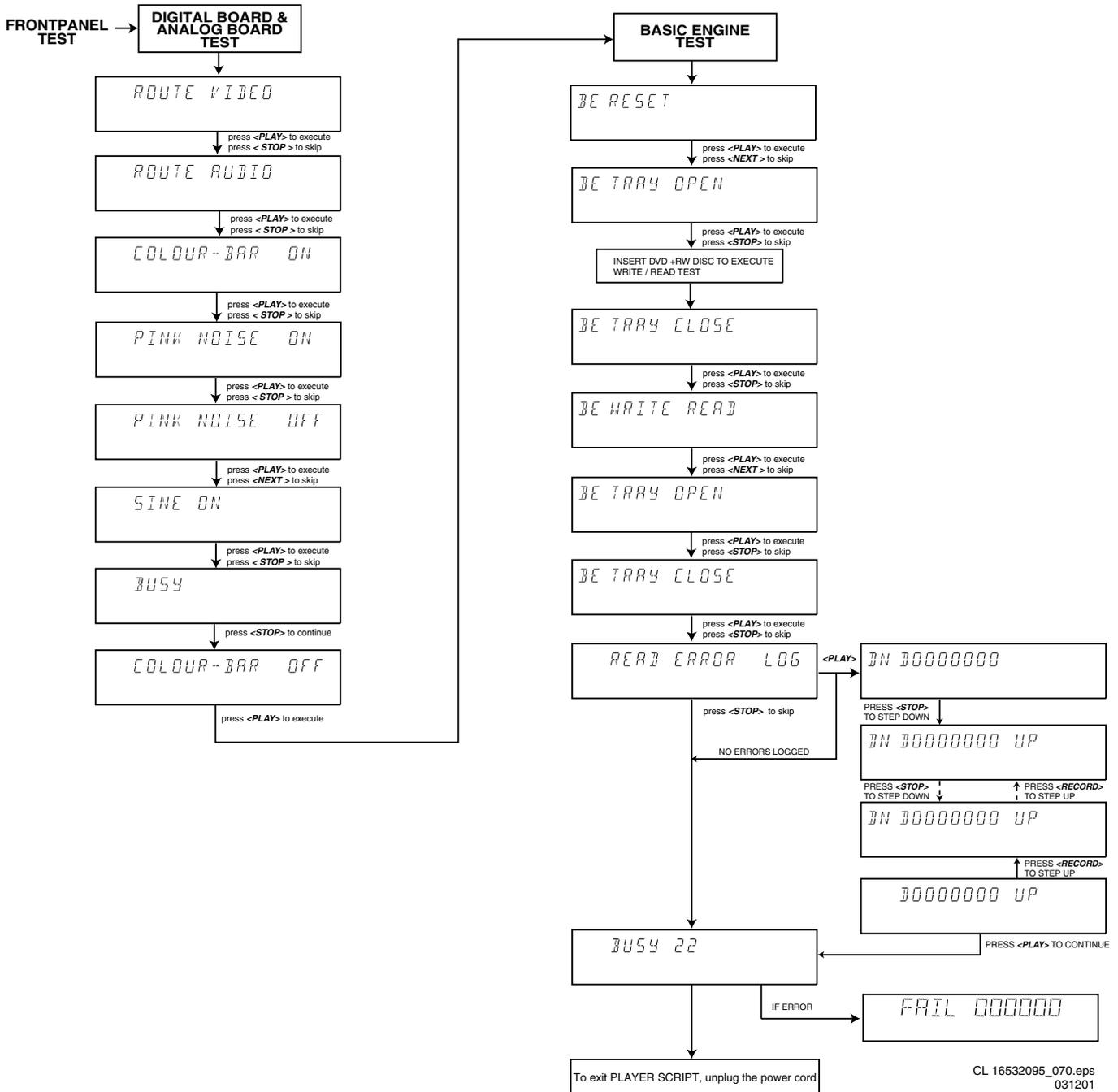


Figure 5-2



CL 16532095_070.eps
031201

Figure 5-3

5.2.3 Error Log

Explanation:

The application errors will be logged in the NVRAM. The maximum number of error bytes that will be visible is 19. The last reported error is shown as DN D0000000, the oldest visible error as D0000000 UP and the errors in between as DN D0000000 UP. DN stands for DOWN, UP stands for UPWARDS. The shown D error codes are identical to the Nuclei Error Codes (paragraph 5.4).

5.2.4 Trade Mode

TRADE MODE

When the recorder is in Trade Mode, the recorder cannot be controlled by means of the front key buttons, but only by means of the remote control.

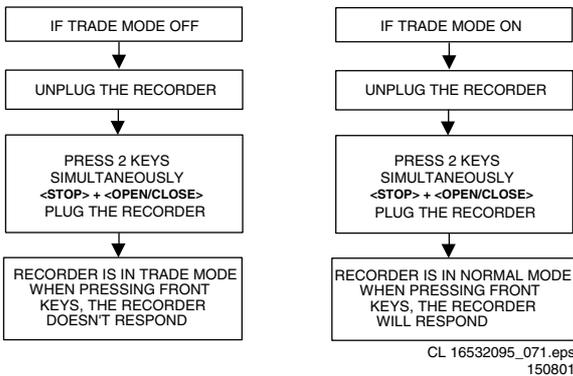


Figure 5-4

5.2.5 Virgin mode

If you want that the recorder starts up in Virgin mode, follow this procedure:

- Unplug the recorder
- plug the recorder again while you keep the STAND BY/ON key pressed
- the set starts up in Virgin mode.

5.3 Menu and Command Mode Interface

5.3.1 Nuclei Numeration

Each nucleus has a unique number of four digits. This number is the input of the command mode.

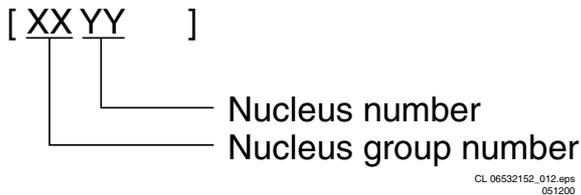


Figure 5-5

The following groups are defined:

Group number	Group name
0	Basic / Scripts
1	Host decoder (Sti5505 and memory)
2	Audio / video encoder (DVDR only)
3	VSM (DVDR only)
4	NVRAM
5	Front Panel
6	Basic Engine
7	Analogue board (DVDR only)
8	DVIO (DVDR only)
9	Loop nuclei (DVDR only)
10	Library sub nuclei (I2C nuclei)
11	User interface
12	Furore (SACD only)
13	DAC (SACD only)
14	Miscellaneous

5.3.2 Error Handling

Each nucleus returns an error code. This code contains six numerals, which means:

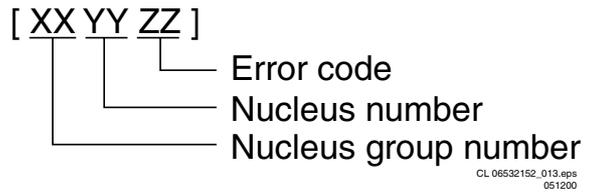


Figure 5-6

The nucleus group numbers and nucleus numbers are the same as above.

5.3.3 Command Mode Interface

Set-Up Physical Interface Components

Hardware required:

- Service PC
 - one free COM port on the Service PC
 - special cable to connect DVD recorder to Service PC
- The service PC must have a terminal emulation program (e.g. OS2 WarpTerminal or Procomm) installed and must have a free COM port (e.g. COM1). Activate the terminal emulation program and check that the port settings for the free COM port are: 19200 bps, 8 data bits, no parity, 1 stop bit and no flow control. The free COM port must be connected via a special cable to the RS232 port of the DVD recorder. This special cable will also connect the test pin, which is available on the connector, to ground (i.e. activate test pin).

Code number of PC interface cable: 3122 785 90017

Activation

Plug the recorder to the mains and the following text will appear on the screen of the terminal (program):

```

DVD Video Recorder Diagnostic Software version 48
Basic SDRAM Data bus test passed
Basic SDRAM Address bus test passed
Basic SDRAM Device test passed

(M) enu, (C) ommand or (S) 2B-interface? [M] : @ c ↵
DD:>
    
```

Figure 5-7

The first line indicates that the Diagnostic software has been activated and contains the version number. The next lines are the successful result of the SDRAM interconnection test and the basic SDRAM test. The last line allows the user to choose between the three possible interface forms. If pressing C has made a choice for Command Interface, the prompt ("DD>") will appear. The diagnostic software is now ready to receive commands. The commands that can be given are the numbers of the nuclei.

Command Overview

We provide an overview of the nuclei and their numbers. This overview is preliminary and subject to modifications.

Host Decoder [01]

[xx yy] Number	Nuclei
100	Checksum Flash
101	Flash Write Access 1
102	Flash Write Access 2
103	Flash Write Read
104	SdRam Write Read
105	SdRam Write Read Fast
106	Dram Write Read
107	Dram Write Read Fast
108	Hardware Version
109	Mute On
110	Mute Off
115	Pink Noise On
116	Pink Noise Off
117	Sine On
118	Sine Burst 1kHz
119	Sine Burst 12kHz
120	Colour-bar On
121	Colour-bar Off
122	NvramWrR
123	NvramI2c
130	Boot Version
131	Application Version
132	Diagnostics Version
133	Download Version
134	Write / read I2C message to / from digital board
135	Video Test Signal On
136	Video Test Signal Off
137	Macrovision Off

Audio Video Decoder [02]

[xx yy] Number	Nuclei
200	Video Encoder I2C
202	SAA7118 I2C
203	Audio Encoder SRAM Access
204	Audio Encoder Access
205	Audio Encoder SRAM Write Read
206	Audio Encoder Interrupts
207	Audio Encoder I2C
208	SAA7118 select input
209	Empress Version

VSM [03]

[xx yy] Number	Nuclei
300	Register Access
301	SDRAM Access
302	SDRAM Write Read
303	Interrupt lines
304	VSM Interconnection
305	UART

NVRAM [04]

[xx yy] Number	Nuclei
400	Reset
401	Read

[xx yy] Number	Nuclei
402	Modify
403	UniqueNr Read
404	Read Error Log
407	Reset Error Log
409	Line2 Region-Code Reset
410	UniqueNr Store

Front Panel [05]

[xx yy] Number	Nuclei
500	Echo
501	Version
502	Segment
503	Label
504	Led
505	Keyboard
506	Remote-Control
507	Segment Starburst
508	Segment Vertical
509	Segment Horizontal
514	Beeper
515	Discbar
516	Discbar Dots
517	Vu / Grid
518	Dimmer
519	Blinking
520	Light All Segments
522	Flap Open
523	Flap Close

Basic Engine [06]

[xx yy] Number	Nuclei
600	S2B Pass
601	S2B Echo
602	Version
603	Reset
604	Focus On
605	Focus Off
606	Disc Motor On
607	Disc Motor Off
608	Radial On
609	Radial Off
615	Tray In
616	Tray Out
617	Write Read
618	Write Read Endless Loop
619	Selftest
620	BE Test
621	Laser Test
622	Spindle (Disc) Motor Test
623	Focus Test
624	Sledge Motor Test
625	Sledge Motor Slow
626	Tilt
627	EEPROM Read
628	EEPROM Write
629	Optimise Jitter
630	Radial ATLS Calibration
631	Get Statistics Information
632	Reset Statistics Information

[xx yy] Number	Nuclei
633	BE Read Error Log
634	BE Reset Error Log
638	Get Self Test Result
639	Radial Initialisation
640	Get OPU info
641	Write read +R
642	Write read +R endless loop

Analog Board [07]

[xx yy] Number	Nuclei
700	Echo
703	Boot Version
704	Hardware Version
705	Clock Adjust
706	Tuner
707	Frequency Download
708	Data Slicer
709	Sound Processor
710	AV Selector
711	Nvram
712	Route Video
713	Route Audio
715	Set Slash Version
716	Application Version
717	Diagnostics Version
718	Download Version
720	Bargraph Level Adjustment
721	Clock correction
722	Clock reference
723	Re-virginise Recorder
724	Flash Checksum
725	Tuner frequency selection
727	Set virgin bit
728	Clear Virgin Bit
729	Write / read I2C message to / from analogue board
730	Store external presets
731	Get slash version
732	AFC Reference Voltage Tuner

DVIO [08]

[xx yy] Number	Nuclei
800	Check DVIO board presence
801	Reset DVIO
802	DVIO Access
803	Get DVIO error codes
804	Get DVIO module Ids
805	Execute DVIO module SelfTest
806	Set DVIO led on.
807	Set DVIO led off.

Loop Nuclei [09]

[xx yy] Number	Nuclei
900	Digital Audio Loop
901	User / Dealer Audio Loop
902	Digital Video Loop
903	Digital Video VBI Loop
904	System Video Loop
905	System Video VBI Loop

[xx yy] Number	Nuclei
906	User / Dealer Video Loop
907	User / Dealer Video VBI Loop
908	System Audio Loop SCART
909	System Audio Loop CINCH
910	Digital DVIO Video Loop
911	System Video Vip

Miscellaneous [14]

[xx yy] Number	Nuclei
1400	Clock 11.289 MHz
1401	Clock 12.288 MHz
1412	Progressive Scan I2C
1413	Progressive Scan test image on
1414	Progressive Scan test image off
1415	Progressive Scan Route Enable
1416	Progressive Scan Route Disable

Scripts [00]

[xx yy] Number	Nuclei
1	UserDealer Script
2	Player Script

5.3.4 Menu Mode Interdace

Activation

Plug the recorder to the mains and the following text will appear on the screen of the terminal (program):

```

DVD Video Recorder Diagnostic Software version 48
Basic SDRAM Data bus test passed
Basic SDRAM Address bus test passed
Basic SDRAM Device test passed

(M) enu, (C) ommand or (S) 2B-interface?   [M] : @ M ↵

Main Menu

1.  Digital Board           ->
2.  Analogue Board         ->
3.  Front Panel            ->
4.  Basic Engine           ->
5.  DVIO                   ->
6.  Progressive Scan Board ->
7.  Loop tests             ->
8.  Log                    ->
9.  Scripts                ->

Select>

```

CL 16532095_074.eps
150801

Figure 5-8

The first line indicates that the Diagnostic software has been activated and contains the version number. The next lines are the successful result of the SDRAM interconnection test and the basic SDRAM test. The last line allows the user to choose between the three possible interface forms. If pressing M has made a choice for Menu Interface, the Main Menu will appear.

Menu Structure

The following menu structure is given after starting up the DVD recorder in menu mode. The symbol -> indicates that the current menu choice will invoke the display of a submenu.

Main Menu

- 1.Digital Board ->
- 2.Analogue Board ->
- 3.Front Panel ->
- 4.Basic Engine ->
- 5.DVIO ->
- 6.Progressive Scan Board ->
- 7.Loop Tests ->
- 8.Log ->
- 9.Scripts ->

Digital Board Menu

- 1.Host Decoder ->
- 2.VSM ->
- 3.AVENC ->
- 4.NVRAM ->

Host Decoder Menu

- 1.Flash Checksum
- 2.Flash1 Write Access
- 3.Flash2 Write Access
- 4.Flash Write/Read
- 5.Host SDRAM Write/Read
- 6.Host SDRAM Fast Write/Read
- 7.Host DRAM Write/Read
- 8.Host DRAM Fast Write/Read
- 9.I2C NVRAM
- 10.NVRAM Write/Read
- 11.Engine S2B Echo
- 12.Versions ->
- 13.Audio Mute ->
- 14.Colourbar ->
- 15.Pink Noise ->
- 16.Sine Generate ->

Digital Board Versions Menu

- 1.Hardware Version
- 2.Bootcode version
- 3.Applications Version
- 4.Diagnostics Version
- 5.Download Version

Audio Mute Menu

- 1.Audio Mute On
- 2.Audio Mute Off

Colourbar Menu

- 1.Colourbar On
- 2.Colourbar Off

Pink Noise Menu

- 1.Pink Noise On
- 2.Pink Noise Off

Sine Generate Menu

- 1.Sine On
- 2.Sine Burst 1kHz
- 3.Sine Burst 12kHz

VSM Menu

- 1.Register Access
- 2.SDRAM Access
- 3.VSM SDRAM Write/Read
- 4.Interrupt Lines
- 5.VSM Interconnection
- 6.UART

AVENC Menu

- 1.Empress ->
- 2.Video Input Processors ->

Empress Menu

- 1.Version number

Video Input Processors Menu

- 1.SAA7118 I2C Access

NVRAM Menu

- 1.Read Error Log
- 2.Reset Error Log
- 3.Read DVIO Unique ID

Analogue Board Menu

- 1.Echo
- 2.Obsolete
- 3.Route Video Input back to Digital board
- 4.Route Audio Input back to Digital board
- 5.Flash Checksum
- 6.Versions ->
- 7.Components ->
- 8.Re-virginize Recorder ->

Analogue Board Versions Menu

- 1.Hardware Version
- 2.Bootcode version
- 3.Application version
- 4.Diagnostics version
- 5.Download version

Analogue Components Menu

- 1.Tuner
- 2.Data Slicer
- 3.Sound Processor
- 4.AV Selector
- 5.NVRAM

Analogue Board Re-virginize Menu

- 1.Re-virginize Recorder
- 2.Set Virgin-bit
- 3.Clear Virgin-bit
- 4.Store external presets

Front Panel Menu

- 1.Echo
- 2.Version
- 3.Flap Control ->
- 4.Segment Test ->
- 5.Light Labels
- 6.Led test
- 7.Keyboard test
- 8.Remote Control
- 9.Beep
- 10.Disc Bar
- 11.Disc Bar Dots
- 12.Vu Grid
- 13.Dimmer
- 14.Blink
- 15.Light All Segments

Flap Control Menu

- 1.Open Flap
- 2.Close Flap

Segment Test Menu

- 1.Starburst
- 2.Light Horizontal Segments
- 3.Light Vertical Segments
- 4.Light All Segments

Basic Engine Menu

- 1.Reset
- 2.S2B Pass-through
- 3.S2B Echo
- 4.Focus On
- 5.Focus Off
- 6.Version
- 7.Self Test
- 8.Get Self Test Result
- 9.Basic Engine Test
- 10.Laser Test
- 11.Focus Test
- 12.Tilt Test
- 13.Optimise Jitter
- 14.Statistics Info
- 15.Log ->
- 16.Spindle Motor ->
- 17.Radial ->
- 18.Sledge ->
- 19.Tray ->

Basic Engine Error Log

- 1.Read Error Log
- 2.Reset Error Log

Basic Engine Spindle Motor Menu

- 1.Spindle Motor On
- 2.Spindle Motor Off
- 3.Spindle Motor Test

Basic Engine Radial Menu

- 1.Radial On
- 2.Radial Off
- 3.Radial Initialisation
- 4.Radial ATLS Calibration

Basic Engine Sledge Menu

- 1.Sledge test
- 2.Sledge test slow

Basic Engine Tray Menu

- 1.Tray In
- 2.Tray Out

DVIO Menu

- 1.Check Presence
- 2.Reset
- 3.Access
- 4.Error Codes
- 5.Module Identifiers
- 6.Led ->

DVIO Led Menu

- 1.Led On
- 2.Led Off

Progressive Scan Board Menu

- 1.I2C Access
- 2.Test Image On
- 3.Test Image Off

Loop Tests Menu

- 1.Digital Board Loops ->
- 2.User/Dealer Loops ->
- 3.System Loops ->
- 4.Basic Engine Loops ->

Digital Board Loops Menu

- 1.Obsolete
- 2.Digital Video Loop
- 3.Digital Video Loop VBI

User/Dealer Loops Menu

- 1.User/Dealer Audio Loop
- 2.User/Dealer Video Loop
- 3.User/Dealer Video Loop VBI

System Loops Menu

- 1.System Video Loop
- 2.System Video Loop VBI
- 3.System Audio Loop SCART(EURO)
- 4.System Audio Loop CINCH (NAFTA)

Basic Engine Loops Menu

- 1.Basic Engine write read
- 2.Basic Engine write read endless loop

Log Menu

- 1.Read Error Log
- 2.Reset Error Log

Script Menu

- 1.User/Dealer Script
- 2.Player Script

5.4 Nuclei Error Codes

In the following table the error codes will be described.

Error Nr	Error String
10000	"Checksum is OK"
10001	"segment name Checksum doesn't match" or "segment name segment not found"
10100	""
10101	"FLASH 1 Write access test failed"
10200	""
10201	"FLASH 2 Write access test failed"
10300	""
10301	"FLASH write test failed"
10302	"FLASH write command failed"
10303	"FLASH write test done max. number of times"
10400	""
10401	"HostDec SDRAM Memory data bus test goes wrong."
10402	" HostDec SDRAM Memory address bus test goes wrong."
10403	" HostDec SDRAM Physical memory device test goes wrong."
10500	""
10501	" HostDec SDRAM Memory data bus test goes wrong."
10502	" HostDec SDRAM Memory address bus test goes wrong."
10503	" HostDec SDRAM Physical memory device test goes wrong."
10600	""
10601	"HostDec DRAM Memory data bus test goes wrong."
10602	"HostDec DRAM Memory address bus test goes wrong."
10603	"HostDec DRAM Physical memory device test goes wrong."
10700	""
10701	"HostDec DRAM Memory data bus test goes wrong."
10702	"HostDec DRAM Memory address bus test goes wrong."
10703	"HostDec DRAM Physical memory device test goes wrong."

Error Nr	Error String
10800	"Host Decoder version(cut) number: version number""Digital hardware version"
10801	"Can not find version in FLASH."
10900	""
10901	"Error muting audio"
11000	""
11001	"Error demuting audio"
11500	""
11501	"Init of I2C failed"
11502	"The selection of the clock source failed"
11504	"The demute of the audio failed"
11600	""
11601	"Init of I2C failed"
11602	"The mute of the audio failed"
11700	""
11701	"Init of I2C failed"
11702	"The muting of the audio failed"
11703	"The demute of the audio failed"
11704	"The selection of the clock source failed"
11707	"Setup of Front panel failed"
11708	"Sine on Front panel keyboard failed"
11800	""
11801	"Init of I2C failed"
11802	"The muting of the audio failed"
11803	"The demute of the audio failed"
11804	"The selection of the clock source failed"
11805	"Error cannot start VSM audio in port"
11900	""
11901	"Init of I2C failed"
11902	"The muting of the audio failed"
11903	"The demute of the audio failed"
11904	"The selection of the clock source failed"
11905	"Error cannot start VSM audio in port"
12000	""
12001	"Invalid input"
12100	""
12200	""
12201	"I2C bus busy before start"
12202	"NVRAM access time-out"
12203	"No NVRAM acknowledge"
12204	"NVRAM time-out"
12205	"NVRAM Write/Read back failed"
12300	""
12301	"I2C bus busy before start"
12302	"NVRAM read access time-out"
12303	"No NVRAM read acknowledge"
12304	"NVRAM read failed"
13000	"Bootcode application version : bootversion"
13001	"Can not find version in FLASH."
13100	"Recorder application version : recorderversion"
13101	"Can not find version in FLASH."
13200	"Diagnostics application version : diagversion"
13201	"Can not find version in FLASH."
13300	"Download application version : downloadversion"
13301	"Can not find version in FLASH."
13700	""
13701	"Turning off MacroVision failed"
20000	""
20001	"I2C bus busy before start"
20002	"Video Encoder access time-out"
20003	"No acknowledge from Video Encoder"

Error Nr	Error String
20004	"No data send/received to or from Video Encoder"
20005	"SAA7118 VIP can not be initialised"
20200	""
20201	"I2C bus busy before start"
20202	"SAA7118 VIP access time-out"
20203	"No acknowledge from SAA7118 VIP"
20204	"No data received from SAA7118 VIP"
20300	""
20301	"Error audio encoder SRAM access cannot initialise I2C"
20302	"Error audio encoder SRAM access cannot reset DSP through I2C"
20303	"Error audio encoder SRAM access cannot download boot"
20304	"Error audio encoder cannot download test code"
20305	"Error audio encoder cannot obtain result of test"
20306	"Error audio encoder SRAM access stuck-at-zero data line "
20307	"Error audio encoder SRAM access stuck-at-one data line "
20308	"Error audio encoder SRAM access stuck-at-one address line "
20309	"Error audio encoder SRAM access address line address line x is connected to data line data line y"
20310	"Error audio encoder SRAM access address lines address line x and address line y are connected "
20311	"Error audio encoder SRAM access data lines data line x and data line y are connected "
20312	"Error audio encoder SRAM access illegal data received"
20400	""
20401	"Error audio encoder access cannot initialise I2C"
20402	"Error audio encoder access cannot reset DSP through I2C"
20403	"Error audio encoder accessing ICR register"
20404	"Error audio encoder access stuck-at-zero of data line "
20405	"Error audio encoder access stuck-at-one of data line "
20406	"Audio encoder access data lines data line x and data line y are interconnected "
20500	""
20501	"Error audio encoder SRAM WRR cannot initialise I2C"
20502	"Error audio encoder SRAM WRR cannot reset DSP through I2C"
20503	"Error audio encoder WRR cannot download boot"
20504	"Error audio encoder cannot download test code"
20505	"Error audio encoder SRAM WRR cannot obtain result of test"
20506	"Error audio encoder WRR SRAM stuck-at-zero data bit "
20507	"Error audio encoder WRR SRAM stuck-at-one data bit "
20508	"Error audio encoder WRR SRAM data lines data line x and data line y are connected"
20509	"Error audio encoder WRR SRAM illegal data received"
20600	""
20601	"Error audio encoder interrupt cannot initialise I2C"
20602	"Error audio encoder interrupt cannot reset DSP through I2C"
20603	"Error audio encoder cannot download test code"
20604	"Error occurred accessing VSM"
20605	"Audio encoder interrupt not received"

Error Nr	Error String
20606	"Error occurred while activating the encoder"
20607	"Error audio encoder interrupt cannot initialise empress"
20608	"Error occurred while getting interrupt reason"
20700	""
20701	"Error audio encoder I2C cannot reset DSP through I2C"
20702	"Error audio encoder cannot download boot"
20703	"Error audio encoder cannot download TEST code"
20704	"Error audio encoder I2C bus busy"
20705	"Error audio encoder I2C cannot write slave address"
20706	"Error audio encoder I2C no acknowledge received"
20707	"Error audio encoder I2C cannot send/receive data"
20708	"Error audio encoder received data through I2C was invalid"
20800	""
20801	"I2C access failed."
20802	"SAA7118 VIP can not be initialised."
20803	"Invalid input"
20900	"B1.B2. B3.B4. B5.B6. B7.B8. B9.B10. B11.B12."
20901	"Firmware download of EMPRESS failed"
20902	"I2C bus busy before start"
20903	"EMPRESS access time-out"
20904	"No acknowledge from the EMPRESS"
20905	"No data send to the EMPRESS"
20906	"No data received from the EMPRESS"
30000	""
30001	"VSM SDRAM Bank1 Memory databus test goes wrong."
30002	"VSM SDRAM Bank1 Memory addressbus test goes wrong."
30003	"VSM SDRAM Bank1 Physical memory device test goes wrong."
30004	" VSM SDRAM Bank2 Memory databus test goes wrong."
30005	" VSM SDRAM Bank2 Memory addressbus test goes wrong."
30006	" VSM SDRAM Bank2 Physical memory device test goes wrong."
30007	"VSM SDRAM Bank1 VSM interrupt register A has a -stuck at- error for value:"
30008	"VSM SDRAM Bank2 VSM interrupt register A has a -stuck at- error for value:"
30100	""
30101	"VSM SDRAM Bank1 Memory databus test goes wrong."
30102	"VSM SDRAM Bank1 Memory addressbus test goes wrong."
30103	"VSM SDRAM Bank1 Physical memory device test goes wrong."
30104	" VSM SDRAM Bank2 Memory databus test goes wrong."
30105	" VSM SDRAM Bank2 Memory addressbus test goes wrong."
30106	" VSM SDRAM Bank2 Physical memory device test goes wrong."
30200	""
30201	"VSM SDRAM Bank1 Memory databus test goes wrong."
30202	"VSM SDRAM Bank1 Memory addressbus test goes wrong."

Error Nr	Error String
30203	"VSM SDRAM Bank1 Physical memory device test goes wrong."
30204	" VSM SDRAM Bank2 Memory databus test goes wrong."
30205	" VSM SDRAM Bank2 Memory addressbus test goes wrong."
30206	" VSM SDRAM Bank2 Physical memory device test goes wrong."
30300	""
30301	"VSM interrupt register A has a -stuck at- error for value:"
30302	"VSM interrupt register B has a -stuck at- error for value:"
30303	"Interrupt A wasn't raised."
30304	"Interrupt B wasn't raised."
30305	"Interrupts A and B were raised."
30400	""
30401	"VSM SDRAM Bank1 Memory databus test goes wrong."
30402	"VSM SDRAM Bank1 Memory addressbus test goes wrong."
30403	"VSM SDRAM Bank1 Physical memory device test goes wrong."
30404	" VSM SDRAM Bank2 Memory databus test goes wrong."
30405	" VSM SDRAM Bank2 Memory addressbus test goes wrong."
30406	" VSM SDRAM Bank2 Physical memory device test goes wrong."
30500	""
30501	"Communication with the analogue board fails."
30502	"Echo test to analogue board returned wrong string."
40000	""
40001	"NVRAM Reset; I2C failed"
40100	"NVRAM address = 0xaddress -> Byte value = 0xvalue"
40101	"NVRAM Read; I2C failed"
40102	"NVRAM Read; Invalid input"
40200	""
40201	"NVRAM Modify; I2C failed"
40202	"NVRAM Modify; Invalid input"
40300	"DV Unique ID = id"
40301	"NVRAM Read DV Unique ID; I2C failed"
40400	"\r\n Error log:\r\n errorString \r\n Ö "
40401	"NVRAM error log; I2C failed"
40402	"NVRAM error log is invalid"
40403	"Front panel failed"
40700	""
40701	"NVRAM error log reset; I2C failed"
40900	"Region code Change counter is reset"
40901	"NVRAM region code reset; I2C failed"
41000	""
41001	"NVRAM Store DV Unique ID; I2C failed"
41002	"NVRAM Store DV Unique ID; Invalid input"
50000	""
50007	"Execution of the command on the analogue board failed."
50008	"The frontpanel could not be accessed by the analogue board."
50009	"The echo from the frontpanel processor was not correct."
50100	" Front panel version: FPversion "

Error Nr	Error String
50102	"Execution of the command on the analogue board failed."
50103	"The frontpanel could not be accessed by the analogue board."
50200	""
50204	"Execution of the command on the analogue board failed."
50205	"The frontpanel could not be accessed by the analogue board."
50206	"The frontpanel did not show a starburst."
50207	"The user skipped the FP-which pattern test."
50208	"The user returned an unknown confirmation: confirmation "
50209	"The frontpanel did not show horizontal segments."
50210	"The frontpanel did not show vertical segments."
50300	""
50304	"Execution of the command on the analogue board failed."
50305	"The frontpanel could not be accessed by the analogue board."
50306	"The frontpanel did not light all labels."
50307	"The user skipped the rest of the FP-label test."
50308	"The user returned an unknown confirmation: confirmation"
50400	""
50404	"Execution of the command on the analogue board failed."
50405	"The frontpanel could not be accessed by the analogue board."
50406	"The LED's could not be turned on."
50407	"The user skipped the rest of the FP-LED test."
50408	"The user returned an unknown confirmation: confirmation"
50500	""
50502	"Front panel Keyboard; test failed"
50503	"Front panel Keyboard; test aborted"
50504	"Front panel Keyboard; not all keys were pressed"
50505	"Front panel keyboard I2C connection failed"
50506	"Unable to get slashversion"
50600	""
50602	"Front panel Remote control; test failed"
50603	"Front panel Remote control; test aborted"
50604	"Front panel remote control; can not access FP"
50605	"Front panel remote control; no user input received"
50700	""
50701	"Execution of the command on the analogue board failed."
50702	"The frontpanel could not be accessed by the analogue board."
50703	"The frontpanel did not show a starburst."
50704	"The user skipped the FP-starburst test."
50705	"The user returned an unknown confirmation: confirmation "
50800	""
50801	"Execution of the command on the analogue board failed."
50802	"The frontpanel could not be accessed by the analogue board."
50803	"The frontpanel did not show vertical segments."
50804	"The user skipped the FP-vertical segments test."
50805	"The user returned an unknown confirmation: confirmation "
50900	""

Error Nr	Error String
50901	"Execution of the command on the analogue board failed."
50902	"The frontpanel could not be accessed by the analogue board."
50903	"The frontpanel did not show horizontal segments."
50904	"The user skipped the FP-horizontal segments test."
50905	"The user returned an unknown confirmation: confirmation "
51400	""
51401	"Execution of the command on the analogue board failed."
51402	"The frontpanel could not be accessed by the analogue board."
51403	"The beeper did not sound."
51404	"The user skipped the FP-Beep test."
51405	"The user returned an unknown confirmation: confirmation"
51500	""
51501	"Execution of the command on the analogue board failed."
51502	"The frontpanel could not be accessed by the analogue board."
51503	"The discbar did not display properly."
51504	"The user skipped the discbar test."
51505	"The user returned an unknown confirmation: confirmation"
51600	""
51601	"Execution of the command on the analogue board failed."
51602	"The frontpanel could not be accessed by the analogue board."
51603	"The discbar dots did not display properly."
51604	"The user skipped the discbar dots test."
51605	"The user returned an unknown confirmation: confirmation"
51700	""
51701	"Execution of the command on the analogue board failed."
51702	"The frontpanel could not be accessed by the analogue board."
51703	"The VU grid did not display properly."
51704	"The user skipped the VU gridtest."
51705	"The user returned an unknown confirmation: confirmation"
51800	""
51801	"Execution of the command on the analogue board failed."
51802	"The frontpanel could not be accessed by the analogue board."
51803	"The frontpanel could not be dimmed."
51804	"The user skipped the FP-Dim test."
51805	"The user returned an unknown confirmation: confirmation"
51900	""
51901	"Execution of the command on the analogue board failed."
51902	"The frontpanel could not be accessed by the analogue board."
51903	"The frontpanel did not show segments blinking."
51904	"The user skipped the FP-blinking test."
51905	"The user returned an unknown confirmation: confirmation"
52000	""

Error Nr	Error String
52001	"Execution of the command on the analogue board failed."
52002	"The frontpanel could not be accessed by the analogue board."
52003	"The frontpanel did not show all segments lit."
52004	"The user skipped the FP-light all segments test."
52005	"The user returned an unknown confirmation: confirmation"
52200	""
52201	"Communication with Analogue Board fails."
52202	"Frontpanel can not be accessed by the Analogue Board."
52300	""
52301	"Communication with Analogue Board fails."
52302	"Frontpanel can not be accessed by the Analogue Board."
60000	""
60100	""
60101	"Basic Engine returned error number 0xerrornumber"
60102	"Parity error from Basic Engine to Serial"
60103	"Communication time-out error"
60104	"Unexpected response from Basic Engine"
60105	"Echo loop could not be closed"
60106	"Wrong echo pattern received"
60200	"Version: nr1.nr2.nr3"
60201	"Basic Engine returned error number 0xerrornumber"
60202	"Parity error from Basic Engine to Serial"
60203	"Communication time-out error"
60204	"Unexpected response from Basic Engine"
60205	"Front Panel failed."
60300	""
60301	"Basic-Engine time-out error"
60400	""
60401	"Basic Engine returned error number 0xerrornumber"
60402	"Parity error from Basic Engine to Serial"
60403	"Communication time-out error"
60404	"Unexpected response from Basic Engine"
60405	"Focus loop could not be closed"
60500	""
60501	"Basic Engine returned error number 0xerrornumber"
60502	"Parity error from Basic Engine to Serial"
60503	"Communication time-out error"
60504	"Unexpected response from Basic Engine"
60600	""
60601	"Basic Engine returned error number 0xerrornumber"
60602	"Parity error from Basic Engine to Serial"
60603	"Communication time-out error"
60604	"Unexpected response from Basic Engine"
60700	""
60701	"Basic Engine returned error number 0xerrornumber"
60702	"Parity error from Basic Engine to Serial"
60703	"Communication time-out error"
60704	"Unexpected response from Basic Engine"
60800	""
60801	"Basic Engine returned error number 0xerrornumber"
60802	"Parity error from Basic Engine to Serial"

Error Nr	Error String
60803	"Communication time-out error"
60804	"Unexpected response from Basic Engine"
60805	"Radial loop could not be closed"
60900	""
60901	"Basic Engine returned error number 0xerrornumber"
60902	"Parity error from Basic Engine to Serial"
60903	"Communication time-out error"
60904	"Unexpected response from Basic Engine"
61500	""
61501	"Basic Engine returned error number 0xerrornumber"
61502	"Parity error from Basic Engine to Serial"
61503	"Communication time-out error"
61504	"Unexpected response from Basic Engine"
61600	""
61601	"Basic Engine returned error number 0xerrornumber"
61602	"Parity error from Basic Engine to Serial"
61603	"Communication time-out error"
61604	"Unexpected response from Basic Engine"
61700	""
61701	"BE tray-in command failed"
61702	"BE read-TOC command failed"
61703	"BE VSM interrupt initialisation failed"
61704	"BE set irq command failed"
61705	"BE no disc or wrong disc inserted"
61706	"BE rec-pause command failed"
61707	"BE VSM BE out DMA initialisation failed"
61708	"BE VSM BE out initialisation failed"
61709	"BE VSM BE out DMA start failed"
61710	"BE VSM BE out start failed"
61711	"BE rec command failed"
61712	"BE VSM out underrun error occurred"
61713	"BE record complete interrupt not raised"
61714	"BE get irq command failed"
61715	"BE no interrupt was raised by BE"
61716	"BE VSM DMA out not finished"
61717	"BE stop command after writing failed"
61718	"BE VSM Sector processor initialisation failed"
61719	"BE VSM sector processor DMA initialisation failed"
61720	"BE VSM sector processor DMA start failed"
61721	"BE VSM sector processor start failed"
61722	"BE seek command failed"
61723	"BE VSM sector processor error occurred"
61724	"BE read timeout occurred"
61725	"BE stop command after reading failed"
61726	"BE difference found in data at disc sector 0xdiscsector"
61727	"This nucleus cannot be executed because the Self-Test failed"
61800	""
61801	"BE i2c initialisation failed"
61802	"This nucleus cannot be executed because the Self-Test failed"
61900	""
61901	"The SelfTest failed with result: 0xnr1 0xnr2 0xnr3"
61902	"Basic Engine returned error number 0xerrornumber"
61903	"Parity error from Basic Engine to Serial"
61904	"Communication time-out error"

Error Nr	Error String
61905	"Unexpected response from Basic Engine"
62000	""
62001	"Self-Test : errorstring1 Laser-Test : errorstring2 SpindleM-Test: errorstring3 SledgeM-Test : errorstring4 Focus-Test : errorstring5"
62100	"The forward sense level is 0xlevel"
62101	"Basic Engine returned error number 0xerrornumber"
62102	"Parity error from Basic Engine to Serial"
62103	"Communication time-out error"
62104	"Unexpected response from Basic Engine"
62200	""
62201	"The BE-self-diagnostic-spindle-motor-test failed"
62202	"Basic Engine returned error number 0xerrornumber"
62203	"Parity error from Basic Engine to Serial"
62204	"Communication time-out error"
62205	"Unexpected response from Basic Engine"
62300	""
62301	"The BE-focus-test failed"
62302	"Basic Engine returned error number 0xerrornumber"
62303	"Parity error from Basic Engine to Serial"
62304	"Communication time-out error"
62305	"Unexpected response from Basic Engine"
62400	""
62401	"The BE-self-diagnostic-sledge-motor-test failed"
62402	"Basic Engine returned error number 0xerrornumber"
62403	"Parity error from Basic Engine to Serial"
62404	"Communication time-out error"
62405	"Unexpected response from Basic Engine"
62500	""
62600	""
62700	"BE EEPROM address = address -> Byte value = 0xvalue"
62701	"Basic Engine returned error number 0xerrornumber"
62702	"Parity error from Basic Engine to Serial"
62703	"Communication time-out error"
62704	"Unexpected response from Basic Engine"
62705	"BE read EEPROM; invalid input"
62800	""
62801	"Basic Engine returned error number 0xerrornumber"
62802	"Parity error from Basic Engine to Serial"
62803	"Communication time-out error"
62804	"Unexpected response from Basic Engine"
62805	"BE write EEPROM; invalid input"
62900	""
62901	"Basic Engine returned error number 0xerrornumber"
62902	"Parity error from Basic Engine to Serial"
62903	"Communication time-out error"
62904	"Unexpected response from Basic Engine"
62905	"Radial loop could not be closed"
63000	""
63001	"Basic Engine returned error number 0xerrornumber"
63002	"Parity error from Basic Engine to Serial"
63003	"Communication time-out error"
63004	"Unexpected response from Basic Engine"

Error Nr	Error String
63100	" Number of times Tray went Open/Closed : nr1"" Total hours the CD laser was on : nr2"" Total hours the DVD laser was on : nr3"" Total hours the write laser was on : nr4"
63101	"Basic Engine returned error number 0xerrornumber"
63102	"Parity error from Basic Engine to Serial"
63103	"Communication time-out error"
63104	"Unexpected response from Basic Engine"
63200	""
63201	"Basic Engine returned error number 0xerrornumber"
63202	"Parity error from Basic Engine to Serial"
63203	"Communication time-out error"
63204	"Unexpected response from Basic Engine"
63300	Momentary errors (Byte 1 - Byte 7) : 0xb1 0xb2 0xb3 0xb4 0xb5 0xb6 0xb7 Cumulative errors (Byte 1 - Byte 7): : 0xb1 0xb2 0xb3 0xb4 0xb5 0xb6 0xb7 Fatal errors (Oldest - Youngest) : : 0xb1 0xb2 0xb3 0xb4 0xb5
63301	"Basic Engine returned error number 0xerrornumber"
63302	"Parity error from Basic Engine to Serial"
63303	"Communication time-out error"
63304	"Unexpected response from Basic Engine"
63400	""
63401	"Basic Engine returned error number 0xerrornumber"
63402	"Parity error from Basic Engine to Serial"
63403	"Communication time-out error"
63404	"Unexpected response from Basic Engine"
63500	""
63501	"Basic Engine returned error number 0xerrornumber"
63502	"Parity error from Basic Engine to Serial"
63503	"Communication time-out error"
63504	"Unexpected response from Basic Engine"
63505	"errorstring 0The basic engine will reject all player commands"
63900	""
63901	"Basic Engine returned error number 0xerrornumber"
63902	"Parity error from Basic Engine to Serial"
63903	"Communication time-out error"
63904	"Unexpected response from Basic Engine"
64000	"BE OPU number = opunumber"
64001	"Basic Engine returned error number 0xerrornumber"
64002	"Parity error from Basic Engine to Serial"
64003	"Communication time-out error"
64004	"Unexpected response from Basic Engine"
64100	"The data was successfully written on and read from a DVD disc"
64101	"The tray-in command failed"
64102	"The read-TOC command failed"
64103	"The VSM interrupt initialisation failed"
64104	"The set irq command failed"
64105	"No disc or wrong disc inserted"
64106	"The rec-pause command failed"
64107	"The VSM BE out DMA initialisation failed"
64108	"The VSM BE out initialisation failed"
64109	"The VSM BE out DMA start failed"
64110	"The VSM BE out start failed"
64111	"The rec command failed"

Error Nr	Error String
64112	"The VSM out underrun error occurred"
64113	"The record complete interrupt was not raised"
64114	"The get irq command failed"
64115	"There was no interrupt raised by BE"
64116	"The VSM DMA did not finished"
64117	"The stop command after writing failed"
64118	"The VSM Sector processor initialisation failed"
64119	"The VSM sector processor DMA initialisation failed"
64120	"The VSM sector processor DMA start failed"
64121	"The VSM sector processor start failed"
64122	"The seek command failed"
64123	"The VSM sector processor error occurred"
64124	"The read timeout occurred"
64125	"The stop command after reading failed"
64126	"There was a difference found in data at a specific disc sector"
64127	"The result of the self test contains errors"
64128	"An error interrupt was raised by BE"
64129	"The calibrate-record command failed"
64130	"To many retries"
64131	"BE update RAI command after writing failed"
64132	"BE find first recordable address command failed"
64133	"DVD+R disc is full"
64200	""
64201	"BE i2c initialisation failed"
64202	"This nucleus cannot be executed because the Self-Test failed"
70000	"Echo test OK"
70001	"Echo test returned wrong string."
70002	"Communication with Analogue Board fails"
70300	"SoftwareVersion"
70301	"Can not find segment in FLASH ROM on the Analogue Board"
70302	"Communication with Analogue Board fails"
70400	"HardwareVersion"
70401	"Can not find segment in FLASH ROM on the Analogue Board"
70402	"Communication with Analogue Board fails"
70500	"Clock adjusted OK"
70501	"Can not adjust the clock on the Analogue Board."
70502	"Wrong date/time text size."
70503	"Communication with Analogue Board fails"
70600	"Tuner accessibility test OK"
70601	"Can not access tuner on the Analogue Board."
70602	"Communication with Analogue Board fails"
70700	"Frequency download OK"
70701	"Wrong frequency table size."
70702	"Can not download the frequency table into the analogue NVRAM."
70703	"Can not download the frequency table into the analogue NVRAM."
70704	"Communication with Analogue Board fails"
70800	"Data slicer test OK"
70801	"Test of the Data slicer on the Analogue Board fails."
70802	"Communication with Analogue Board fails"
70900	"Sound Processor test OK"
70901	"Test of the Sound Processor on the Analogue Board fails."
70902	"Communication with Analogue Board fails"
71000	"AV Selector test OK"

Error Nr	Error String
71001	"Test of the AV Selector on the Analogue Board fails."
71002	"Communication with Analogue Board fails"
71100	"NVRAM test OK"
71101	"Test of the NVRAM on the Analogue Board fails."
71102	"Communication with Analogue Board fails"
71200	"Video routing on the Analogue Board OK"
71201	"Routing the video on the Analogue Board fails."
71202	"Invalid input."
71203	"Communication with Analogue Board fails"
71300	"Audio routing on the Analogue Board OK"
71301	"Routing the audio on the Analogue Board fails."
71302	"Invalid input."
71303	"Communication with Analogue Board fails"
71500	""
71501	"Invalid slash version, default slash version is set."
71502	"Setting the slash version on the Analogue Board fails."
71503	"Communication with Analogue Board fails"
71600	"ApplicationVersion"
71601	"Can not find segment in FLASH ROM on the Analogue Board"
71602	"Communication with Analogue Board fails"
71700	"DiagnosticsVersion"
71701	"Can not find segment in FLASH ROM on the Analogue Board"
71702	"Communication with Analogue Board fails"
71800	"DownloadVersion"
71801	"Can not find segment in FLASH ROM on the Analogue Board"
71802	"Communication with Analogue Board fails"
72300	""
72000	""
72001	"Adjusting BarGraphLevel failed"
72002	"Communication with Analogue Board fails"
72100	""
72101	"Storing clock correction failed"
72102	"Value out of range : default value stored "
72103	"Invalid input."
72104	"Communication with Analogue Board fails"
72200	""
72201	"Initialising the 1Hz signal on the Clock IC failed"
72202	"Communication with Analogue Board fails"
72301	"Clearing the NVRAM on the Analogue Board fails"
72302	"Communication with Analogue Board fails"
72400	"segment checksum is : checksum which is correct" for every segment
72401	"segment could not be found" or "segment checksum is : checksumC ,however it should be : checksumE" for every segment
72402	"Communication with Analogue Board fails"
72900	"Date received"
72901	"Data returned"
72902	"Communication on I2C-bus failed on the Analogue Board fails."
72903	"Communication with Analogue Board fails"
73000	""
73001	"Storing the external presets on the Analogue Board fails"
73002	"Communication with Analogue Board fails"
73100	"Oxslashversion" where slashversion is the slash version read from the analogue board
73101	"Error while reading out slash version."

Error Nr	Error String
73102	"I2C Write error."
73103	"I2C Read error."
73104	"Communication with Analogue Board fails"
73200	""
73201	"Storing the Reference Voltage for the Tuner failed"
73202	"Invalid input."
73203	"Communication with Analogue Board fails"
80000	"The DVIO module is present in the system."
80001	"The DVIO module is not present in the system."
80100	"The DVIO module has been reset OK."
80101	"The DVIO module is not present in the system."
80102	"The DVIO module could not be reset."
80103	"Could not initialise I2C before Reset."
80200	"The accessibility of the DVIO module is OK."
80201	"The DVIO board is not present in this DVDR."
80202	"Could not initialise I2C."
80203	"Unable to reset the DVIO module."
80204	"Unable to receive the reset indication from the DVIO module."
80205	"Unable to send the configuration to the DVIO module."
80206	"Unable to download the chip ID to the DVIO module."
80207	"Unable to set the mode of the DVIO module to IDLE."
80208	"Software Error in function HandleStateAwaitingReply !!"
80209	"Maximal number of retries reached by HandleStateSending !!"
80210	"Maximal number of retries (NACKs) reached (HandleStateSending)"
80211	"We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times !!"
80212	"We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times !!"
80213	"We tried to receive an Ack for DVIO_MAX_RETRIES_ACK times!!"
80214	"VSM UART error timeout transmitting command"
80215	"VSM UART error timeout receiving reply"
80216	"VSM UART frame error occurred receiving from DVIO board"
80217	"VSM UART parity error occurred receiving from DVIO board"
80218	"The confirmation/indication from the DVIO module is invalid."
80300	"The accessibility of the DVIO module is OK."
80301	"The DVIO board is not present in this DVDR."
80302	"Could not initialise I2C."
80303	"Unable to reset the DVIO module."
80304	"Unable to receive the reset indication from the DVIO module."
80305	"Unable to send the configuration to the DVIO module."
80306	"Unable to download the chip ID to the DVIO module."
80307	"Unable to set the mode of the DVIO module to IDLE."
80308	"Software Error in function HandleStateAwaitingReply !!"
80309	"Maximal number of retries reached by HandleStateSending !!"
80310	"Maximal number of retries (NACKs) reached (HandleStateSending)"

Error Nr	Error String
80311	"We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times !!"
80312	"We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times !!"
80313	"We tried to receive an Ack for DVIO_MAX_RETRIES_ACK times!!"
80314	"VSM UART error timeout transmitting command"
80315	"VSM UART error timeout receiving reply"
80316	"VSM UART frame error occurred receiving from DVIO board"
80317	"VSM UART parity error occurred receiving from DVIO board"
80318	"The confirmation/indication from the DVIO module is invalid."
80400	"The accessibility of the DVIO module is OK."
80401	"The DVIO board is not present in this DVDR."
80402	"Could not initialise I2C."
80403	"Unable to reset the DVIO module."
80404	"Unable to receive the reset indication from the DVIO module."
80405	"Unable to send the configuration to the DVIO module."
80406	"Unable to download the chip ID to the DVIO module."
80407	"Unable to set the mode of the DVIO module to IDLE."
80408	"Software Error in function HandleStateAwaitingReply !!"
80409	"Maximal number of retries reached by HandleStateSending !!"
80410	"Maximal number of retries (NACKs) reached (HandleStateSending)"
80411	"We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times !!"
80412	"We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times !!"
80413	"We tried to receive an Ack for DVIO_MAX_RETRIES_ACK times!!"
80414	"VSM UART error timeout transmitting command"
80415	"VSM UART error timeout receiving reply"
80416	"VSM UART frame error occurred receiving from DVIO board"
80417	"VSM UART parity error occurred receiving from DVIO board"
80418	"The confirmation/indication from the DVIO module is invalid."
80500	""
80501	"The DVIO board is not present in this DVDR."
80502	"The I2C could not be initialised."
80503	"The DVIO module could not be reset."
80504	"Unable to receive the reset indication from the DVIO module."
80505	"Unable to send the configuration to the DVIO module."
80506	"Unable to download the chip ID to the DVIO module."
80507	"Unable to set the mode of the DVIO module to IDLE."
80508	"Software Error in HandleStateAwaitingReply function!"
80509	"Maximal number of retries reached by HandleStateSending!"
80510	"Maximal number of retries (NACK's) reached (HandleStateSending)"
80511	"We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times!"

Error Nr	Error String
80512	"We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times!"
80513	"We tried to receive an Acknowledge for DVIO_MAX_RETRIES_ACK times!"
80514	"VSM UART error timeout transmitting command"
80515	"VSM UART error timeout receiving reply"
80516	"VSM UART frame error occurred receiving from DVIO board"
80517	"VSM UART parity error occurred receiving from DVIO board"
80518	"The confirmation/indication from the DVIO module is invalid."
80519	"Setting the DVIO module in/out diagnostics mode failed"
80520	"Invalid input"
80521	"Getting the errors of the self-test failed"
80522	"Self-test failed"
80600	""
80601	"The DVIO board is not present in this DVDR."
80602	"The I2C could not be initialised."
80603	"The DVIO module could not be reset."
80604	"Unable to receive the reset indication from the DVIO module."
80605	"Unable to send the configuration to the DVIO module."
80606	"Unable to download the chip ID to the DVIO module."
80607	"Unable to set the mode of the DVIO module to IDLE."
80608	"Software Error in HandleStateAwaitingReply function!"
80609	"Maximal number of retries reached by HandleStateSending!"
80610	"Maximal number of retries (NACK's) reached (HandleStateSending)"
80611	"We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times!"
80612	"We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times!"
80613	"We tried to receive an Acknowledge for DVIO_MAX_RETRIES_ACK times!"
80614	"VSM UART error timeout transmitting command"
80615	"VSM UART error timeout receiving reply"
80616	"VSM UART frame error occurred receiving from DVIO board"
80617	"VSM UART parity error occurred receiving from DVIO board"
80618	"The confirmation/indication from the DVIO module is invalid."
80619	"Setting the DVIO module in/out diagnostics mode failed"
80700	""
80701	"The DVIO board is not present in this DVDR."
80702	"The I2C could not be initialised."
80703	"The DVIO module could not be reset."
80704	"Unable to receive the reset indication from the DVIO module."
80705	"Unable to send the configuration to the DVIO module."
80706	"Unable to download the chip ID to the DVIO module."
80707	"Unable to set the mode of the DVIO module to IDLE."
80708	"Software Error in HandleStateAwaitingReply function!"

Error Nr	Error String
80709	"Maximal number of retries reached by HandleStateSending!"
80710	"Maximal number of retries (NACK's) reached (HandleStateSending)"
80711	"We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times!"
80712	"We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times!"
80713	"We tried to receive an Acknowledge for DVIO_MAX_RETRIES_ACK times!"
80714	"VSM UART error timeout transmitting command"
80715	"VSM UART error timeout receiving reply"
80716	"VSM UART frame error occurred receiving from DVIO board"
80717	"VSM UART parity error occurred receiving from DVIO board"
80718	"The confirmation/indication from the DVIO module is invalid."
80719	"Setting the DVIO module in/out diagnostics mode failed"
90121	"Error: audio data in host memory contains wrong frequency: frequency Hz"
90122	"Error: audio data in host memory contains silence!"
90123	"There is no correct audio frame in the buffer"
90124	"The audio frame has an illegal version bit"
90125	"The audio frame has an illegal bitrate-index"
90126	"The audio frame has an illegal sampling rate"
90127	"The CRC of the audio frame is wrong"
90128	"The audio frame is not MPEG-I layer II !"
90129	"Error cannot de-mute DAC on analogue board"
90200	""
90201	"Initialisation of I2C failed"
90202	"Initialisation of VIP and EMPIRE failed"
90203	"Initialisation of PLL / Link failed."
90204	"Next descriptor address set wrong."
90205	"Turning on the colourbar failed"
90206	"No I2C communication possible to start video encoder."
90207	"Starting the video encoder failed."
90208	"Transfer of data from video encoder to VSM failed."
90209	"Stopping the encoder failed."
90210	"Turning off the colourbar failed."
90211	"Cannot initialize hostdecoder parallel input"
90212	"Cannot initialise VSM AV-out DMA port"
90213	"Cannot initialise VSM AV-out port"
90214	"Cannot start VSM AV-out DMA port"
90215	"Cannot start VSM AV-out port"
90216	"Transfer of data from VSM to host decoder failed."
90217	"VSM and Hostdec memory do not match (compared after transfer)"
90218	"Decoding of the video data in the hostdecoder memory failed"
90219	"The data in the hostdecoder is not equal to a colourbar"
90220	"The video encoder did not return the Group Of Picture count."
90221	"The video encoder did not receive data from the VIP."
90223	"Initialisation of VIP and EMPRESS failed"
90224	"The video encoder did not return the current status."

Error Nr	Error String
90225	"The video encoder timed out in BUSY mode. (no VIP input)"
90226	"The video encoder did not return the current bitrate."
90227	"The video encoder did not switch to ENCODING mode."
90228	"The video encoder could not start from STOP/IDLE mode."
90229	"The video encoder did not switch from IDLE to STOP mode."
90300	""
90301	"Initialisation of I2C failed"
90302	"I2C communication to VIP failed"
90303	"Initialisation of VIP failed"
90304	"Generation of Close Caption data failed"
90305	"VIP not locked to video signal"
90306	"Initialisation of VBI Extractor failed"
90307	"No CC data received"
90308	"Closed Caption data overrun"
90309	"Closed Caption data does not match"
90310	"Switch off ColourBar failed"
90400	""
90401	"Initialisation of I2C failed"
90402	"Initialisation of VIP and EMPIRE failed"
90403	"Initialisation of PLL / Link failed."
90404	"Next descriptor address set wrong."
90405	"Turning on the colourbar failed"
90406	"No I2C communication possible to start video encoder."
90407	"Starting the video encoder failed."
90408	"Transfer of data from video encoder to VSM failed."
90409	"Stopping the encoder failed."
90410	"Turning off the colourbar failed."
90411	"Cannot initialize hostdecoder parallel input"
90412	"Cannot initialise VSM AV-out DMA port"
90413	"Cannot initialise VSM AV-out port"
90414	"Cannot start VSM AV-out DMA port"
90415	"Cannot start VSM AV-out port"
90416	"Transfer of data from VSM to host decoder failed."
90417	"VSM and Hostdec memory do not match (compared after transfer)"
90418	"Decoding of the video data in the hostdecoder memory failed"
90419	"The data in the hostdecoder is not equal to a colourbar"
90420	"The video encoder did not return the Group Of Picture count."
90421	"The video encoder did not receive data from the VIP."
90422	"Execution of the command on the analogue board failed."
90423	"Initialisation of VIP and EMPRESS failed"
90424	"The video encoder did not return the current status."
90425	"The video encoder timed out in BUSY mode. (no VIP input)"
90426	"The video encoder did not return the current bitrate."
90427	"The video encoder did not switch to ENCODING mode."
90428	"The video encoder could not start from STOP/IDLE mode."

Error Nr	Error String
90429	"The video encoder did not switch from IDLE to STOP mode."
90500	""
90501	"Initialisation of I2C failed"
90502	"I2C communication to VIP failed"
90503	"Initialisation of VIP failed"
90504	"Generation of Close Caption data failed"
90505	"VIP not locked to video signal"
90506	"Initialisation of VBI Extractor failed"
90507	"No CC data received"
90508	"Closed Caption data overrun"
90509	"Closed Caption data does not match"
90510	"Switch off ColourBar failed"
90511	"Execution of the command on the analogue board failed."
90600	""
90601	"Initialisation of I2C failed"
90602	"Initialisation of VIP and EMPIRE failed"
90603	"Initialisation of PLL / Link failed."
90604	"Next descriptor address set wrong."
90605	"Turning on the colourbar failed"
90606	"No I2C communication possible to start video encoder."
90607	"Starting the video encoder failed."
90608	"Transfer of data from video encoder to VSM failed."
90609	"Stopping the encoder failed."
90610	"Turning off the colourbar failed."
90611	"Cannot initialize hostdecoder parallel input"
90612	"Cannot initialise VSM AV-out DMA port"
90613	"Cannot initialise VSM AV-out port"
90614	"Cannot start VSM AV-out DMA port"
90615	"Cannot start VSM AV-out port"
90616	"Transfer of data from VSM to host decoder failed."
90617	"VSM and Hostdec memory do not match (compared after transfer)"
90618	"Decoding of the video data in the hostdecoder memory failed"
90619	"The data in the hostdecoder is not equal to a colourbar"
90620	"The video encoder did not return the Group Of Picture count."
90621	"The video encoder did not receive data from the VIP."
90622	"Execution of the command on the analogue board failed."
90623	"Initialisation of VIP and EMPRESS failed"
90624	"The video encoder did not return the current status."
90625	"The video encoder timed out in BUSY mode. (no VIP input)"
90626	"The video encoder did not return the current bitrate."
90627	"The video encoder did not switch to ENCODING mode."
90628	"The video encoder could not start from STOP/IDLE mode."
90629	"The video encoder did not switch from IDLE to STOP mode."
90700	""
90701	"Initialisation of I2C failed"
90702	"I2C communication to VIP failed"
90703	"Initialisation of VIP failed"
90704	"Generation of Close Caption data failed"

Error Nr	Error String
90705	"VIP not locked to video signal"
90706	"Initialisation of VBI Extractor failed"
90707	"No CC data received"
90708	"Closed Caption data overrun"
90709	"Closed Caption data does not match"
90710	"Switch off ColourBar failed"
90711	"Execution of the command on the analogue board failed."
90800	""
90801	"Error routing the audio back to the digital board."
90802	"Error cannot initialise I2C"
90803	"Error cannot initialise VIP"
90804	"Error cannot set ADC enable pin"
90805	"Error cannot set VSM audio clock"
90806	"Error preparing the 12kHz audio-sine"
90807	"Error cannot initialise audio encoder"
90808	"Error cannot initialise VSM audio in port"
90809	"Error cannot initialise VSM audio in DMA port"
90810	"Error cannot initialise VSM audio out DMA port"
90811	"Error cannot initialise audio VSM out port"
90812	"Error cannot initialise host decoder audio in"
90813	"Error loop audio user/dealer cannot start audio encoder"
90814	"Error cannot start VSM audio in DMA port"
90815	"Error starting the 12kHz audio-sine"
90816	"Error transfer data from audio encoder to VSM"
90817	"Error cannot start VSM AV out DMA port"
90818	"Error cannot start VSM AV out port"
90819	"Error transfer data from VSM to host decoder"
90820	"Error: audio data in host memory and VSM memory differ"
90821	"Error: audio data in host memory contains wrong frequency: frequency Hz"
90822	"Error: audio data in host memory contains silence!"
90823	"There is no correct audio frame in the buffer"
90824	"The audio frame has an illegal version bit"
90825	"The audio frame has an illegal bitrate-index"
90826	"The audio frame has an illegal sampling rate"
90827	"The CRC of the audio frame is wrong"
90828	"The audio frame is not MPEG-I layer II !"
90829	"Error cannot de-mute DAC on analogue board"
90900	""
90901	"Error routing the audio back to the digital board."
90902	"Error cannot initialise I2C"
90903	"Error cannot initialise VIP"
90904	"Error cannot set ADC enable pin"
90905	"Error cannot set VSM audio clock"
90906	"Error preparing the 12kHz audio-sine"
90907	"Error cannot initialise audio encoder"
90908	"Error cannot initialise VSM audio in port"
90909	"Error cannot initialise VSM audio in DMA port"
90910	"Error cannot initialise VSM audio out DMA port"
90911	"Error cannot initialise audio VSM out port"
90912	"Error cannot initialise host decoder audio in"
90913	"Error loop audio user/dealer cannot start audio encoder"
90914	"Error cannot start VSM audio in DMA port"
90915	"Error starting the 12kHz audio-sine"
90916	"Error transfer data from audio encoder to VSM"
90917	"Error cannot start VSM AV out DMA port"
90918	"Error cannot start VSM AV out port"

Error Nr	Error String
90919	"Error transfer data from VSM to host decoder"
90920	"Error: audio data in host memory and VSM memory differ"
90921	"Error: audio data in host memory contains wrong frequency: frequency Hz"
90922	"Error: audio data in host memory contains silence!"
90923	"There is no correct audio frame in the buffer"
90924	"The audio frame has an illegal version bit"
90925	"The audio frame has an illegal bitrate-index"
90926	"The audio frame has an illegal sampling rate"
90927	"The CRC of the audio frame is wrong"
90928	"The audio frame is not MPEG-I layer II !"
90929	"Error cannot de-mute DAC on analogue board"
140000	""
140001	"I2C to Clock failed" or "I2C initialisation failed"
140100	""
140101	"I2C to Clock failed" or "I2C initialisation failed"
141200	""
141201	"Progressive Scan Board I2C bus busy"
141211	"Progressive Scan Board I2C FLI2200 bus busy"
141212	"Progressive Scan Board I2C FLI2200 read access time-out"
141213	"Progressive Scan Board I2C FLI2200 no read acknowledge"
141214	"Progressive Scan Board I2C FLI2200 read failed"
141215	"Progressive Scan Board I2C FLI2200 write access time-out"
141216	"Progressive Scan Board I2C FLI2200 no write acknowledge"
141217	"Progressive Scan Board I2C FLI2200 write failed"
141218	"Progressive Scan Board I2C FLI2200 failed"
141221	"Progressive Scan Board I2C AD7196 bus busy"
141222	"Progressive Scan Board I2C AD7196 read access time-out"
141223	"Progressive Scan Board I2C AD7196 no read acknowledge"
141224	"Progressive Scan Board I2C AD7196 read failed"
141225	"Progressive Scan Board I2C AD7196 write access time-out"
141226	"Progressive Scan Board I2C AD7196 no write acknowledge"
141227	"Progressive Scan Board I2C AD7196 write failed"
141228	"Progressive Scan Board I2C AD7196 failed"
141300	""
141301	"Progressive Scan Route Enable failed"
141302	"Generating test image in Hostdecoder failed"
141400	""
141401	"Progressive Scan Route Disable failed"
141402	"Turning off test image in Hostdecoder failed"
141500	""
141501	"Progressive Scan Board I2C failed"
141600	""
141601	"Progressive Scan Board I2C failed"

5.5 Loop tests

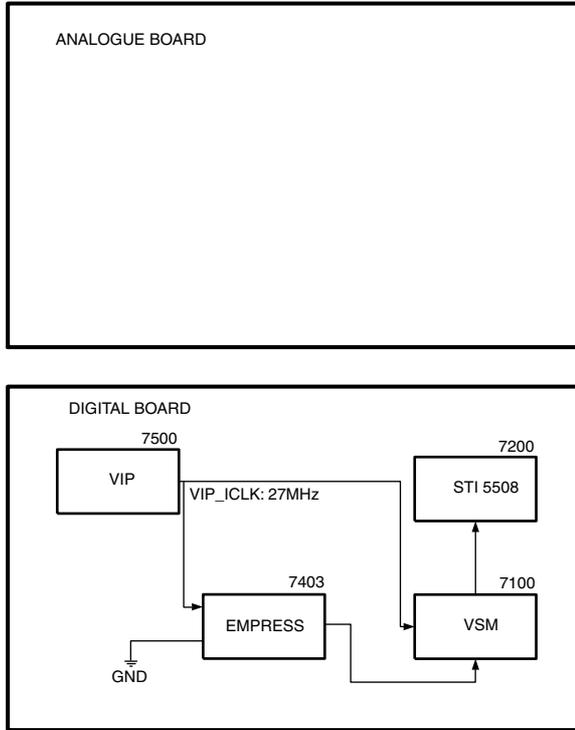
The following loops can be distinguished:

- Loops performed on the digital board only
- User Dealer loops performed on the digital and analogue board
- System loops performed via an external connection: outputs are looped back to the inputs.

5.5.1 Nucleus 900: Digital Audio Loop

This nucleus tests the audio path through the digital board

NUCLEUS 900: AUDIO LOOP DIGITAL



CL 16532145_036.eps
031201

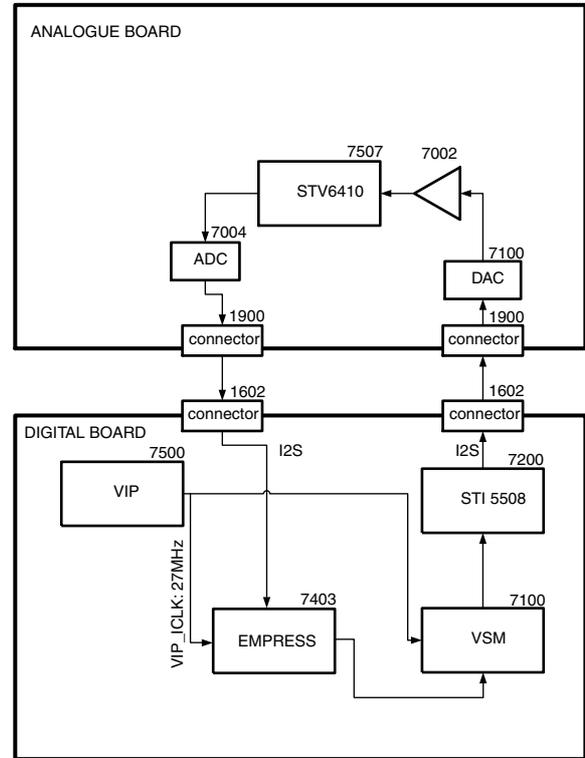
Figure 5-9

5.5.2 Nucleus 901: Audio User Dealer Loop

A PCM audio sine of 12kHz is generated in the Host Decoder for a while and sent to the analogue board. The signal coming from the analogue board is encoded again and sent to the memory of the host decoder for comparison. This nucleus tests the components on the audio signal path:

- Host decoder
- Flex connection between connector 1602 (digital board) and connector 1900 (analogue board)
- DAC
- Op-amp
- Scart switch IC
- ADC
- Audio Encoder
- VIP
- VSM

NUCLEUS 901: AUDIO USER DEALER LOOP



CL 16532145_037.eps
031201

Figure 5-10

5.5.3 Nucleus 902: Digital Video Loop

A colourbar generated in the host decoder is looped through the VIP, Empire, and VSM and checked again in the host decoder. The following components are tested on the video signal path:

- VIP
- Empire
- VSM
- Host decoder

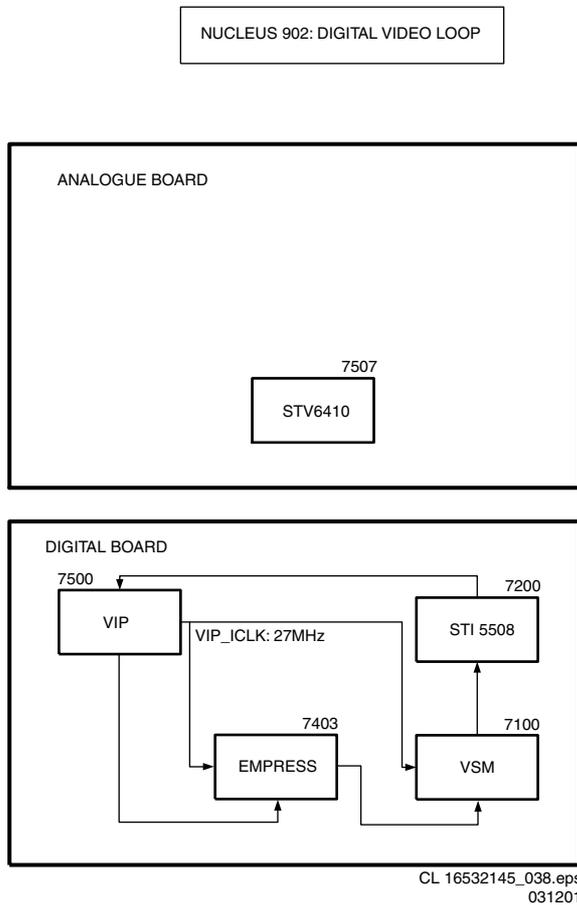


Figure 5-11

5.5.4 Nucleus 903: Digital Video VBI Loop

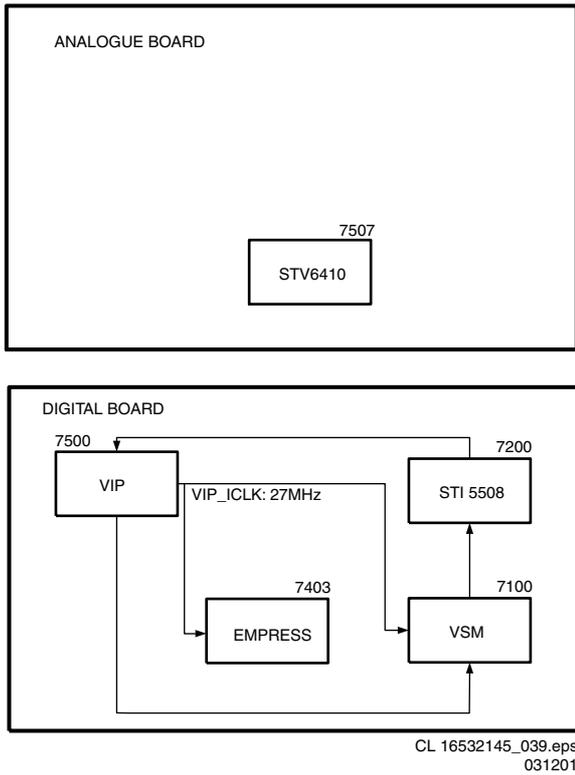
Nucleus for testing the components on the video VBI signal path:

- The VIP
- The VSM
- The Host Decoder

This is done by using the internal test signal source (digital board only)

Remark: this test is only successful if nucleus 121 is carried out first.

NUCLEUS 903: DIGITAL VIDEO VBI LOOP



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031201

Figure 5-12

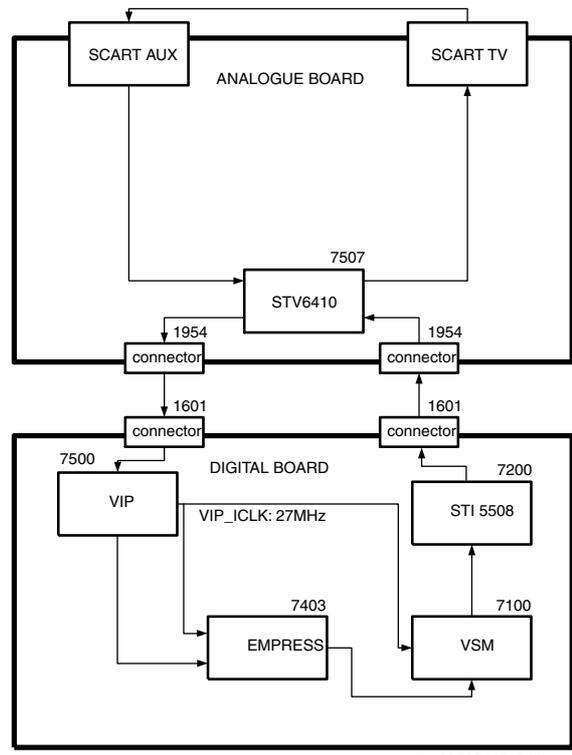
5.5.5 Nucleus 904: System Video Loop

Nucleus for testing the components on the video signal system path:

- The VIP
- The video encoder
- The VSM
- The host decoder
- The analogue board

On the analogue board the video signal will be routed to the SCART (EUROPE) or CINCH (NAFTA). There it will be looped back externally by means of the proper cable

NUCLEUS 904: SYSTEM VIDEO LOOP



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121201

Figure 5-13

5.5.6 Nucleus 905: System Video VBI Loop

This nucleus tests the components on the video signal path:

- The VIP
- The VSM
- The Host Decoder

The video CVBS signal is routed to the output of the analogue board where it will be looped back by means of an external cable

Remark: this test is only successful if nucleus 121 is carried out first.

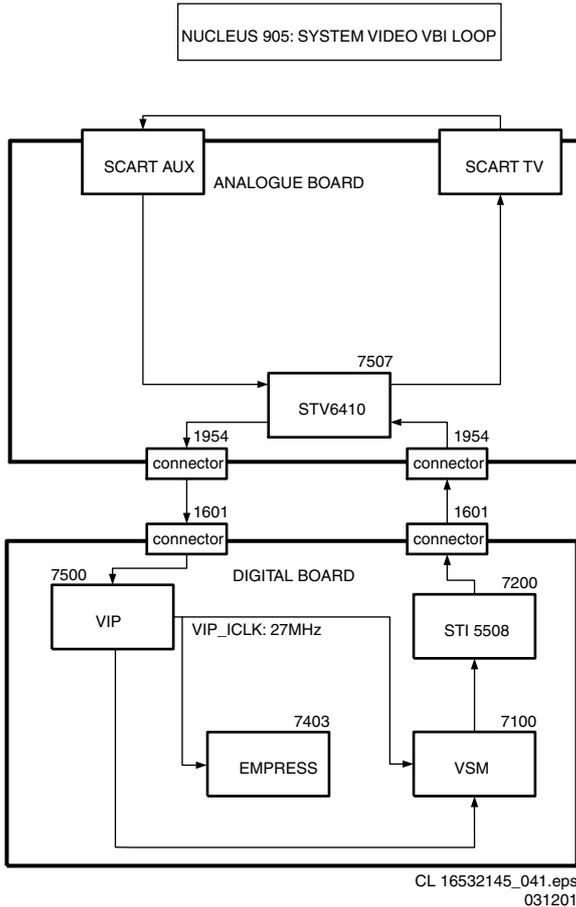


Figure 5-14

5.5.7 Nucleus 906: Video User Dealer Loop

Nucleus for testing the components on the video signal system path:

- The VIP
- The video encoder
- The VSM
- The host decoder
- The analogue board

On the analogue board, the video signal is internally routed back to the digital board.

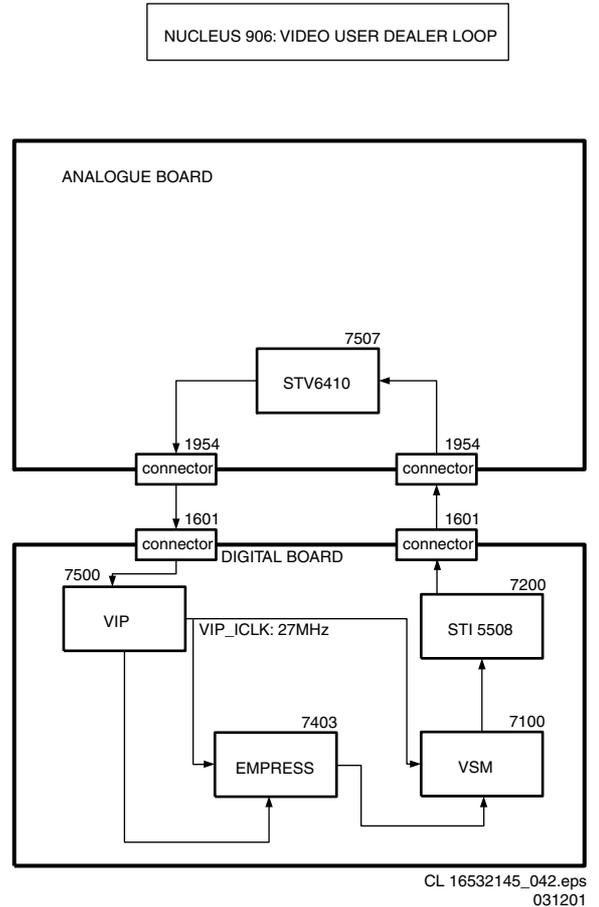


Figure 5-15

5.5.8 Nucleus 907: Video VBI User Dealer Loop

This nucleus tests the components on the video VBI signal path:

- The VIP
- The VSM
- The Host Decoder

The signal is routed back internally on the analogue board

Remark: this test is only successful if nucleus 121 is carried out first.

NUCLEUS 907: VIDEO VBI USER DEALER LOOP

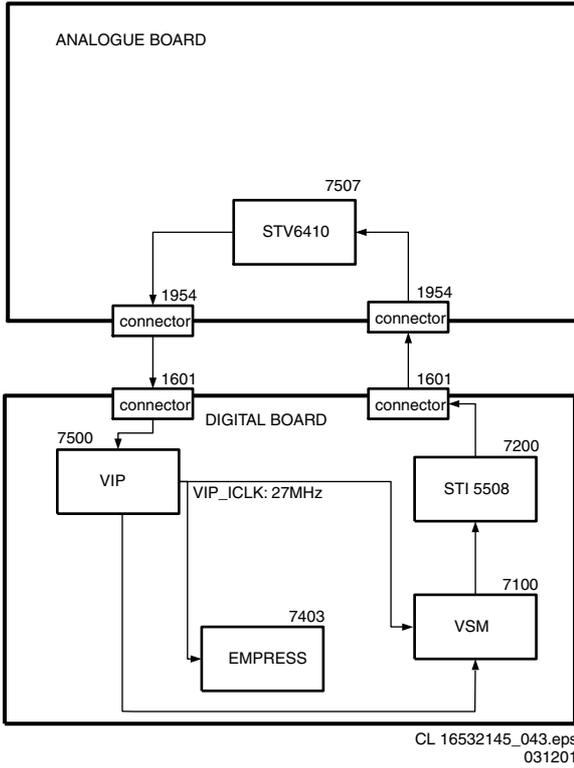


Figure 5-16

5.5.9 Nucleus 908: System Audio Loop Scart (Europe)

Nucleus for testing the components on the audio signal path:

- The hostdecoder
- The analogue board
- The audio encoder
- The VSM

On the analogue board, audio is passed to the SCART connector, where a SCART cable needs to be used to loop back the audio signal to the digital board

NUCLEUS 908: SYSTEM AUDIO LOOP SCART

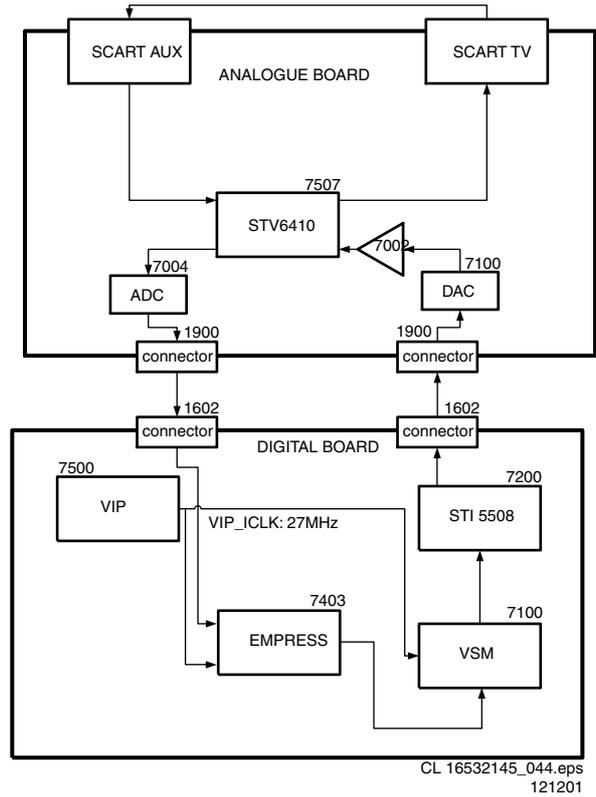


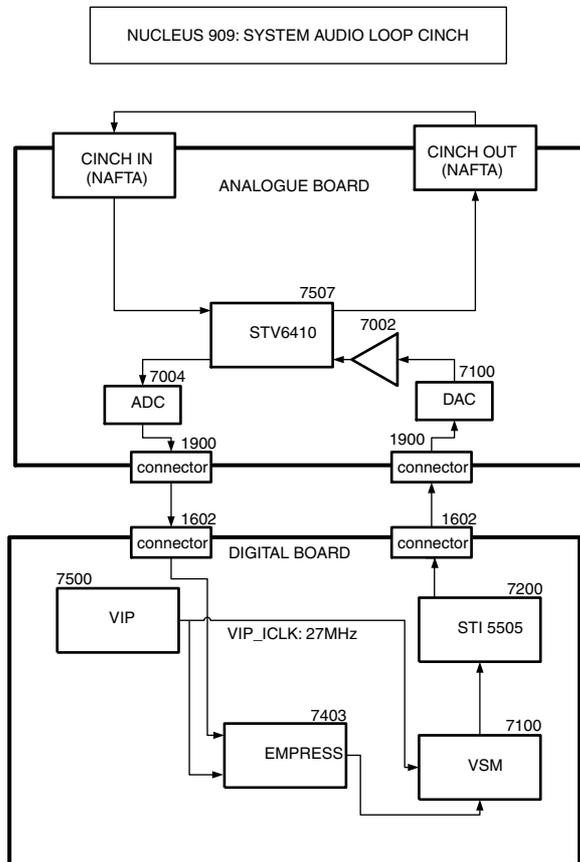
Figure 5-17

5.5.10 Nucleus 909: System Audio Loop CINCH (Nafta)

Nucleus for testing the components on the audio signal path:

- The hostdecoder
- The analogue board
- The audio encoder
- The VSM

On the analogue board the audio is passed to the CINCH connector, where a CINCH cable needs to be used to loop back the audio signal to the digital board



CL 16532145_045.eps
031201

Figure 5-18

5.6 Faultfinding trees

5.6.1 General

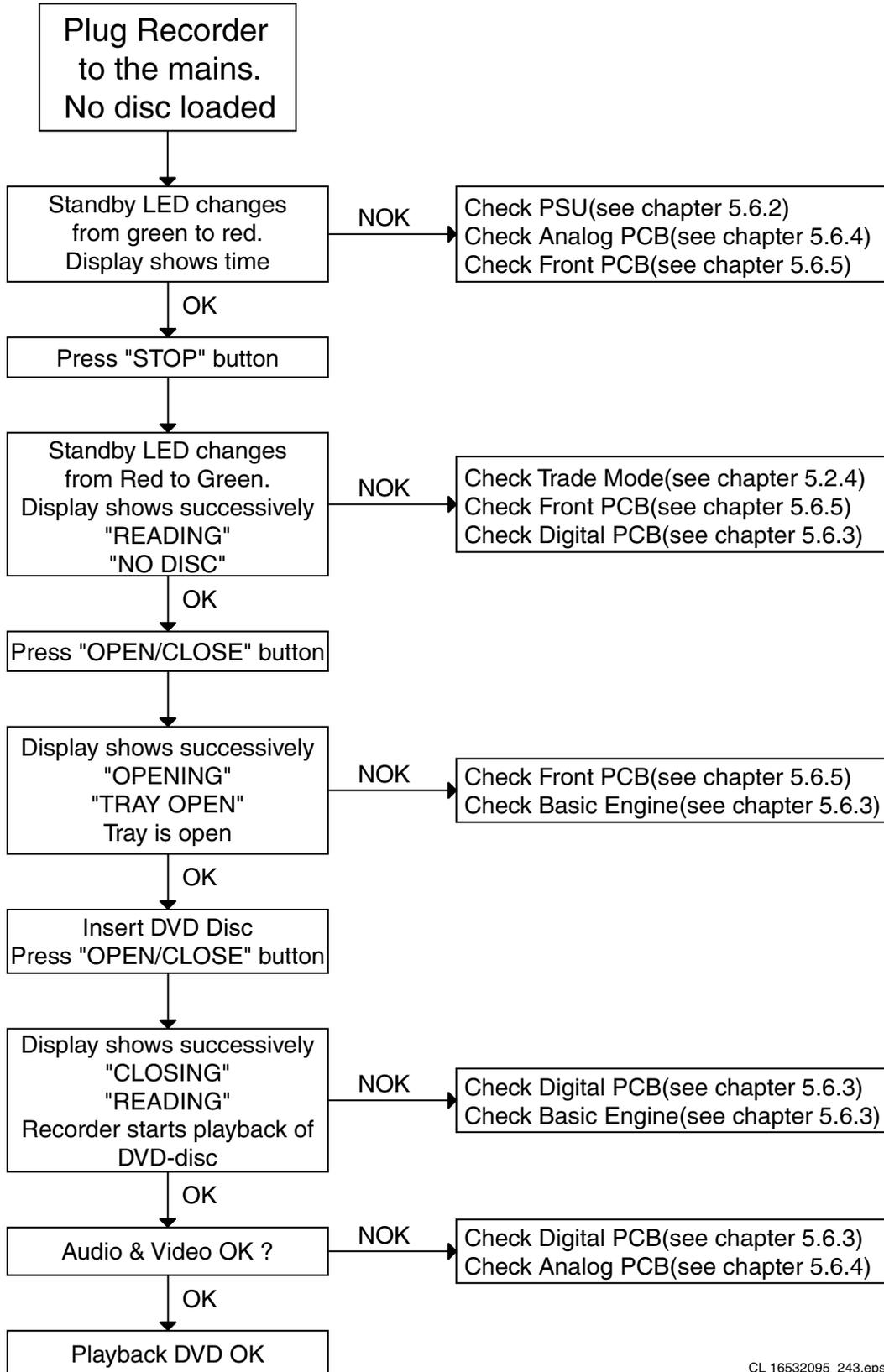
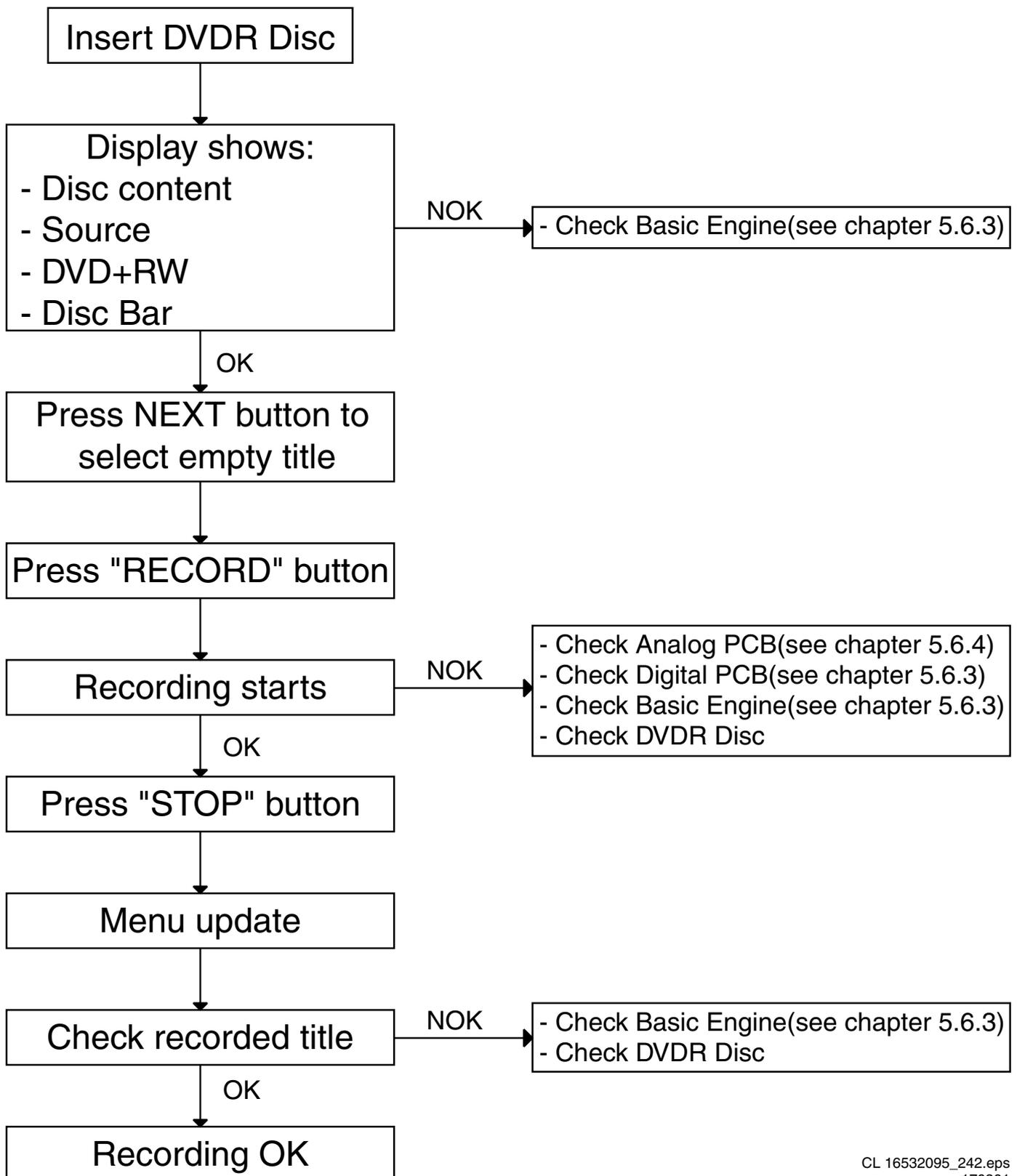
PLAYBACK MODE

Figure 5-19

RECORD MODE



5.6.2 Power supply

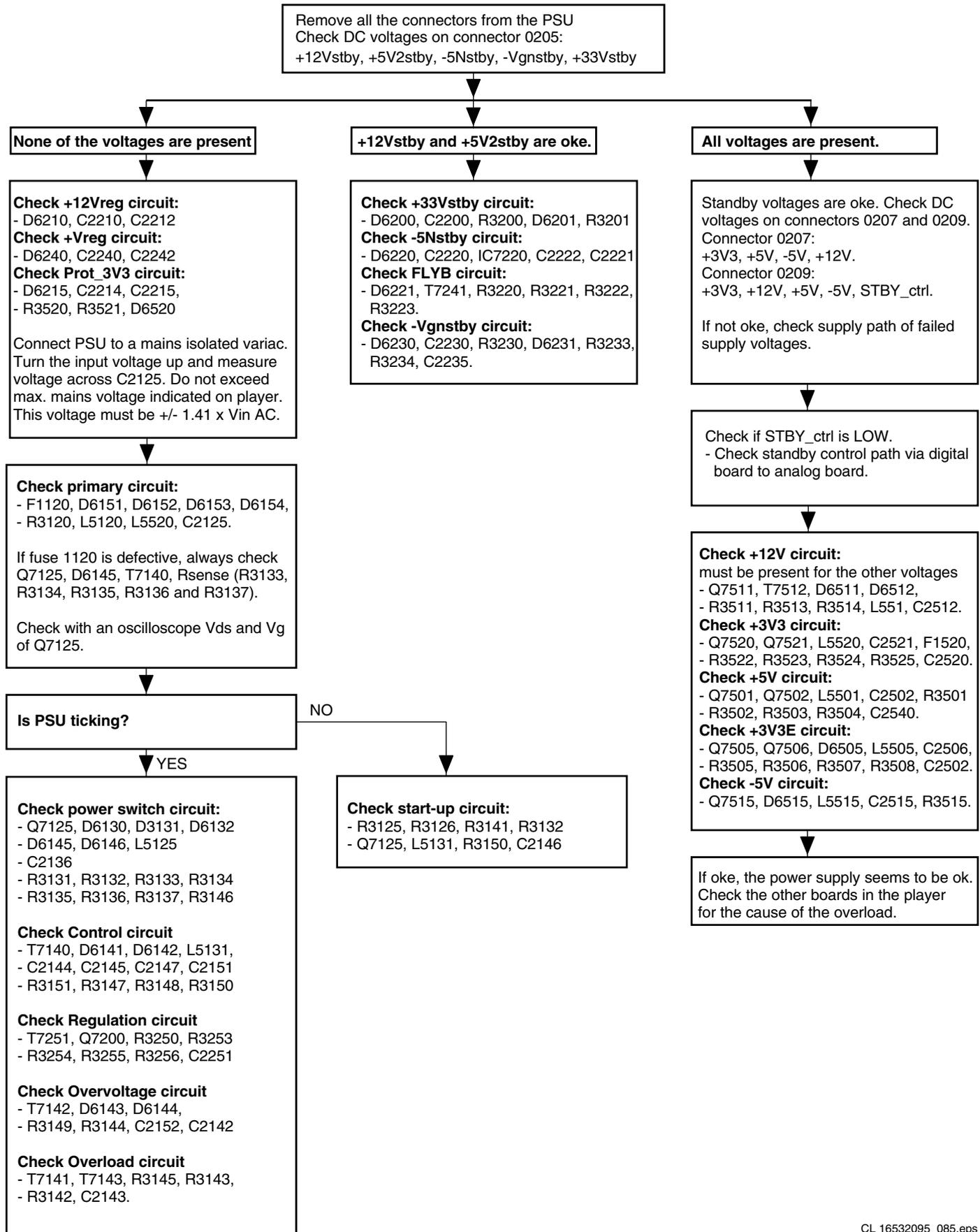


Figure 5-21

5.6.3 Digital Board

Start-up DSW

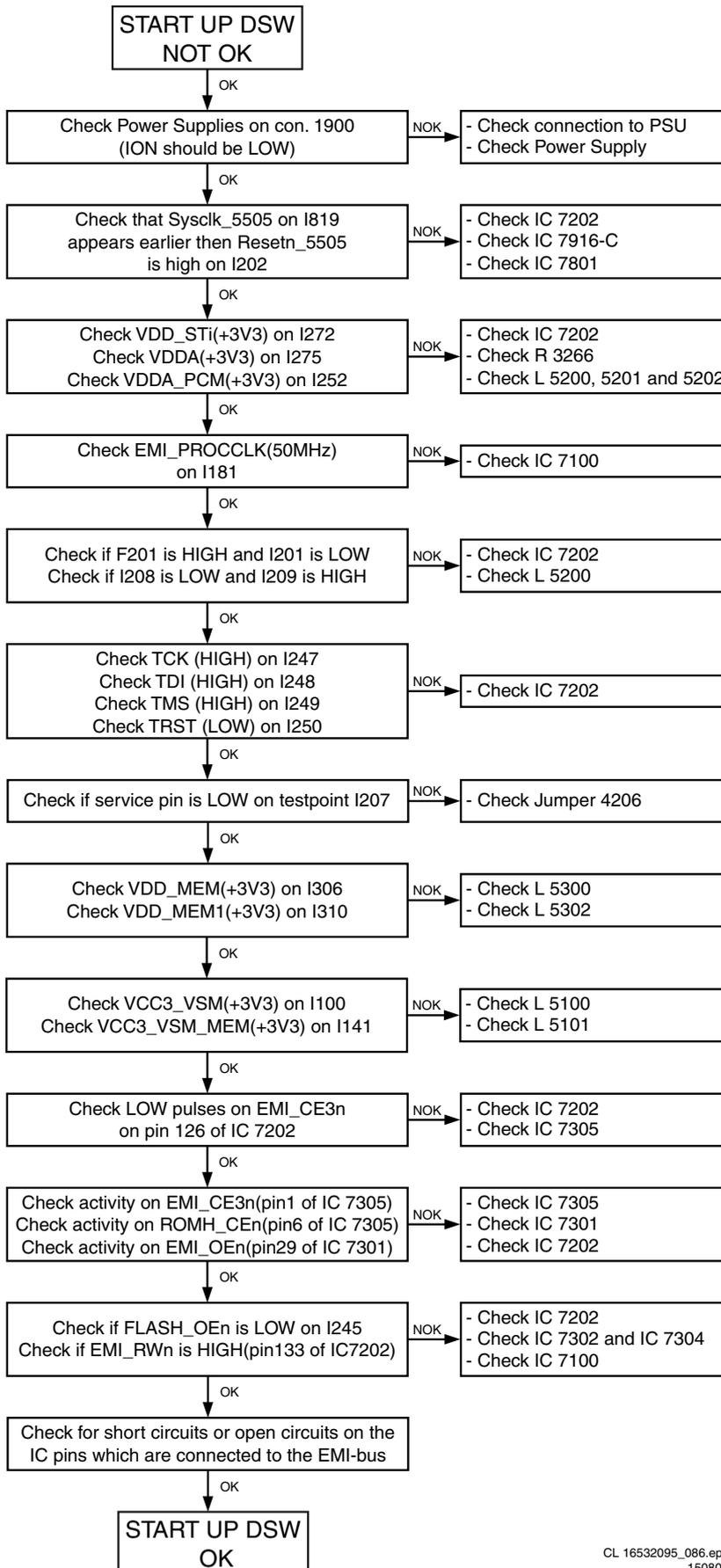


Figure 5-22

Power part check

POWER PART CHECK DIGITAL BOARD

USE DIGITAL BOARD CIRCUIT DIAGRAMS 1 2, 3, 4, 5, 7 AND 8 AND DIGITAL BOARD BOTTOM VIEW TESTPOINTS

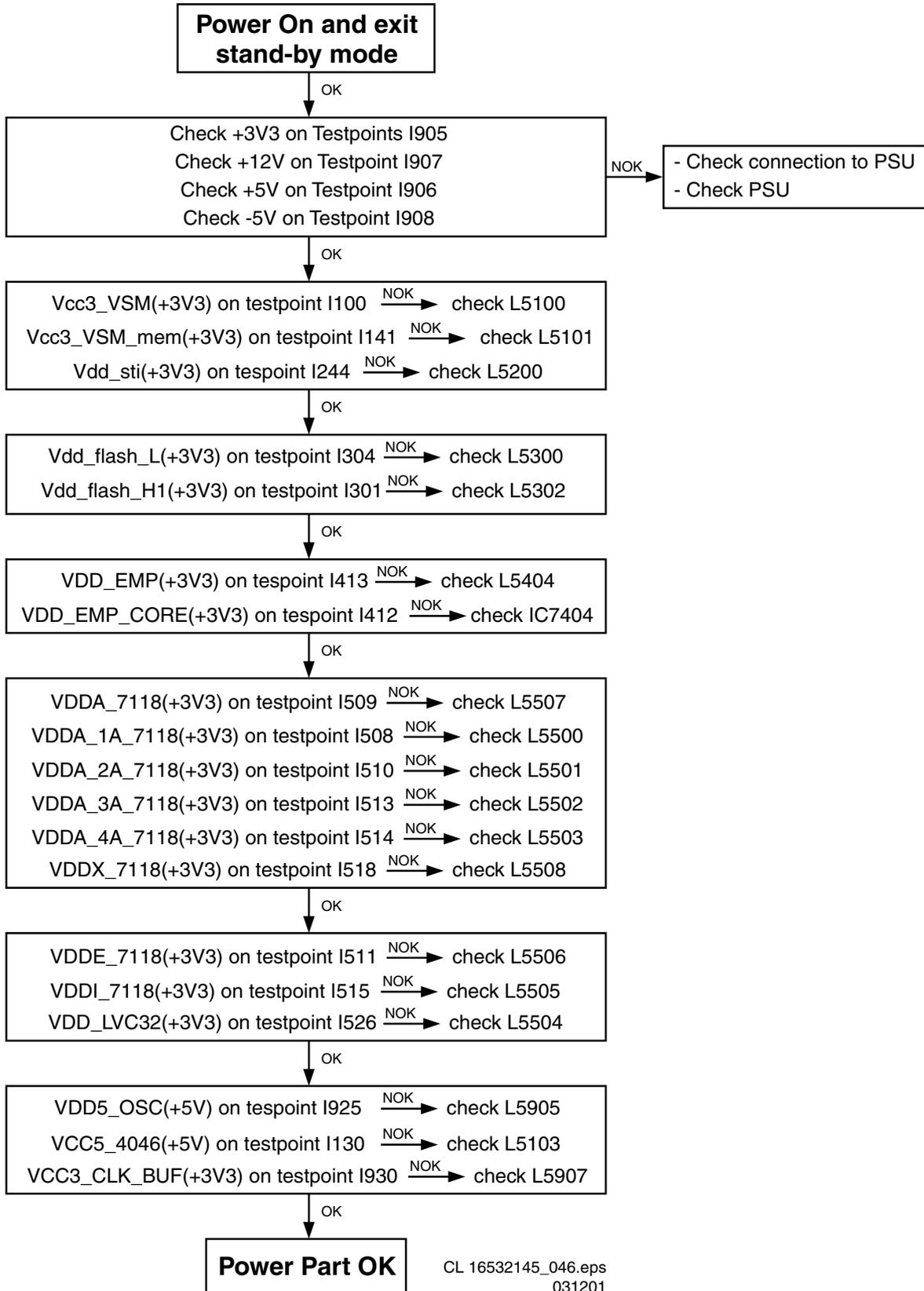


Figure 5-23

RESET & CLOCK CHECK DIGITAL BOARD

USE DIGITAL BOARD CIRCUIT DIAGRAMS 1,2,7 AND 8 AND DIGITAL BOARD BOTTOM VIEW TESTPOINTS

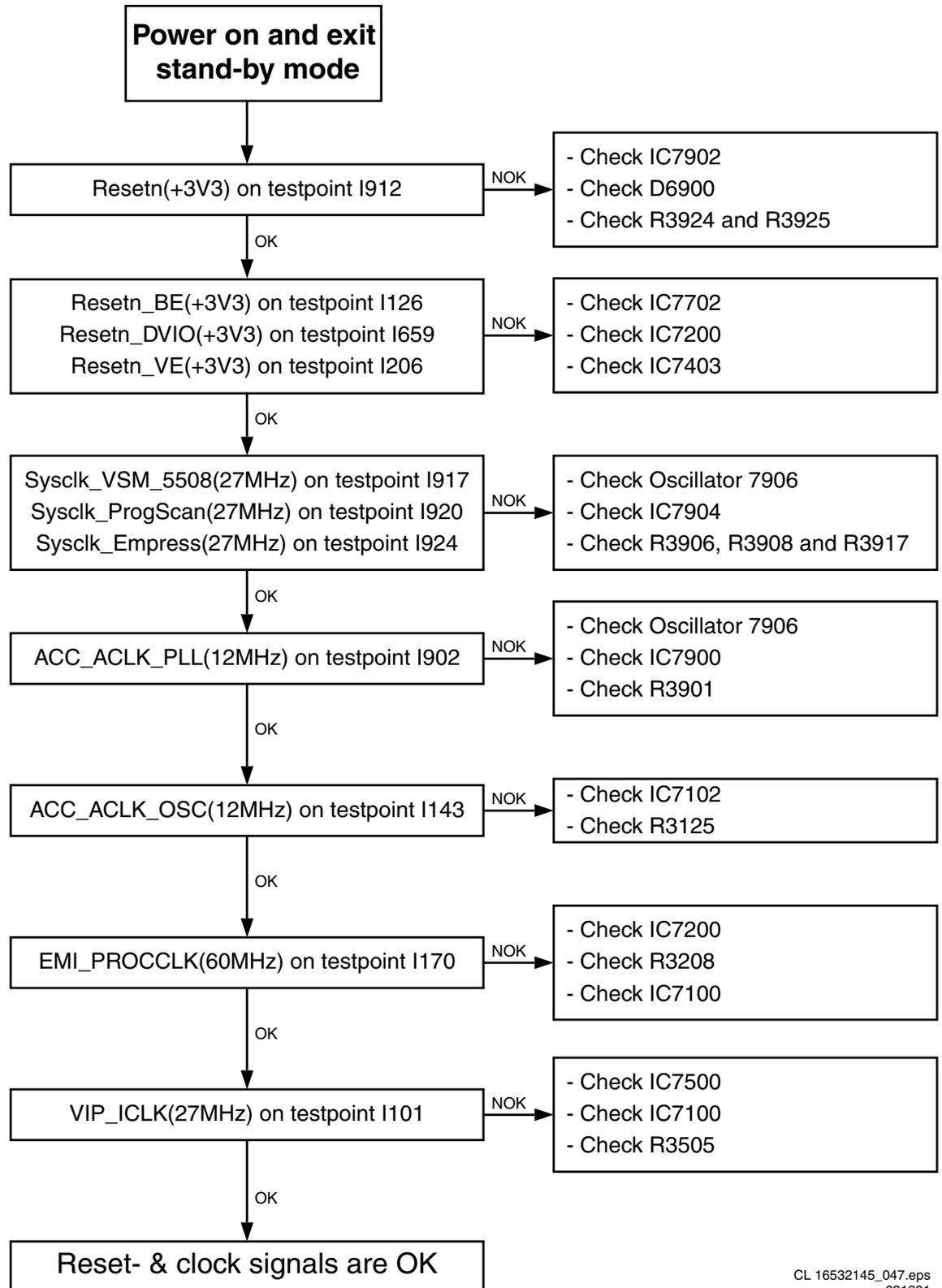


Figure 5-24

DSW MEMORY TESTS

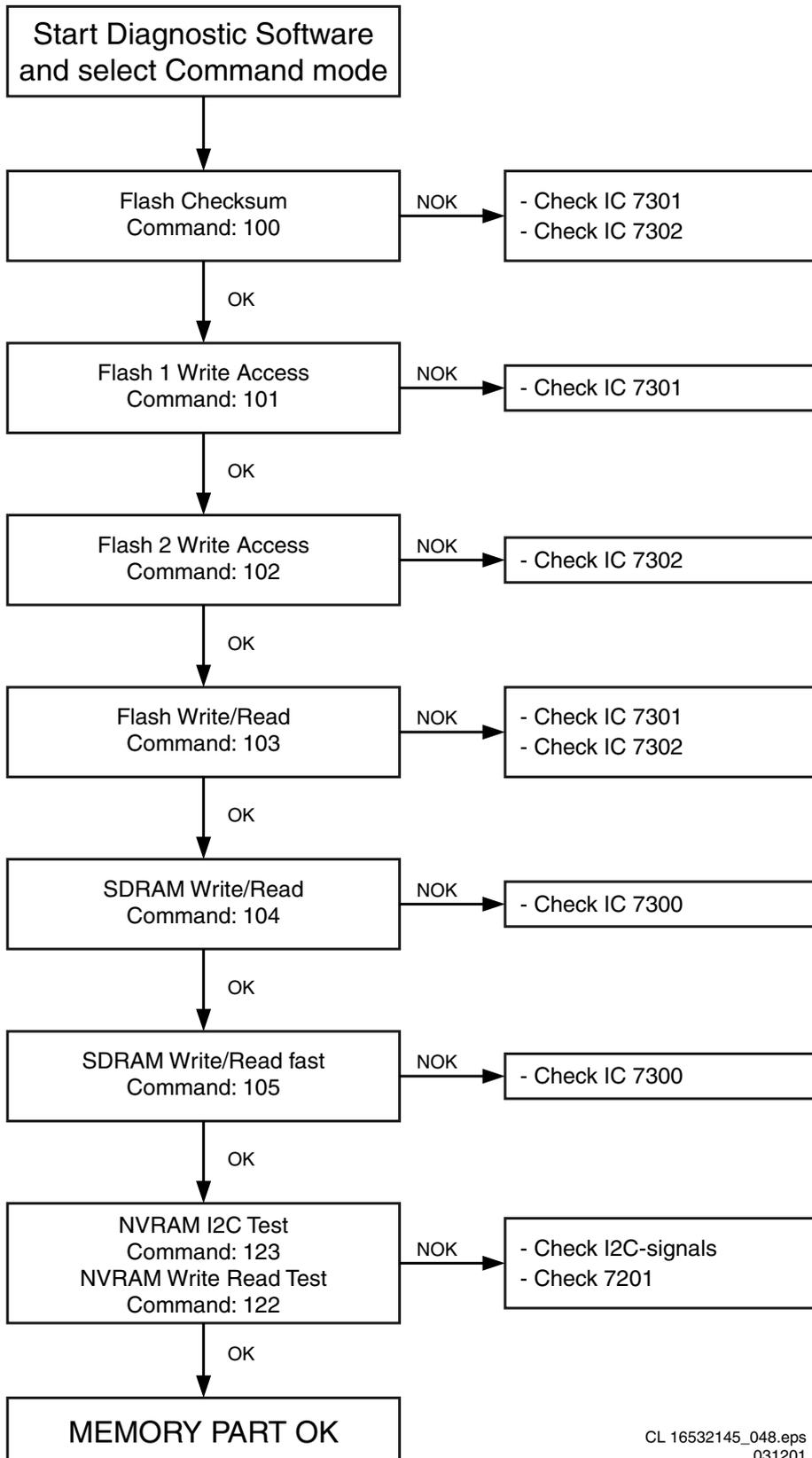
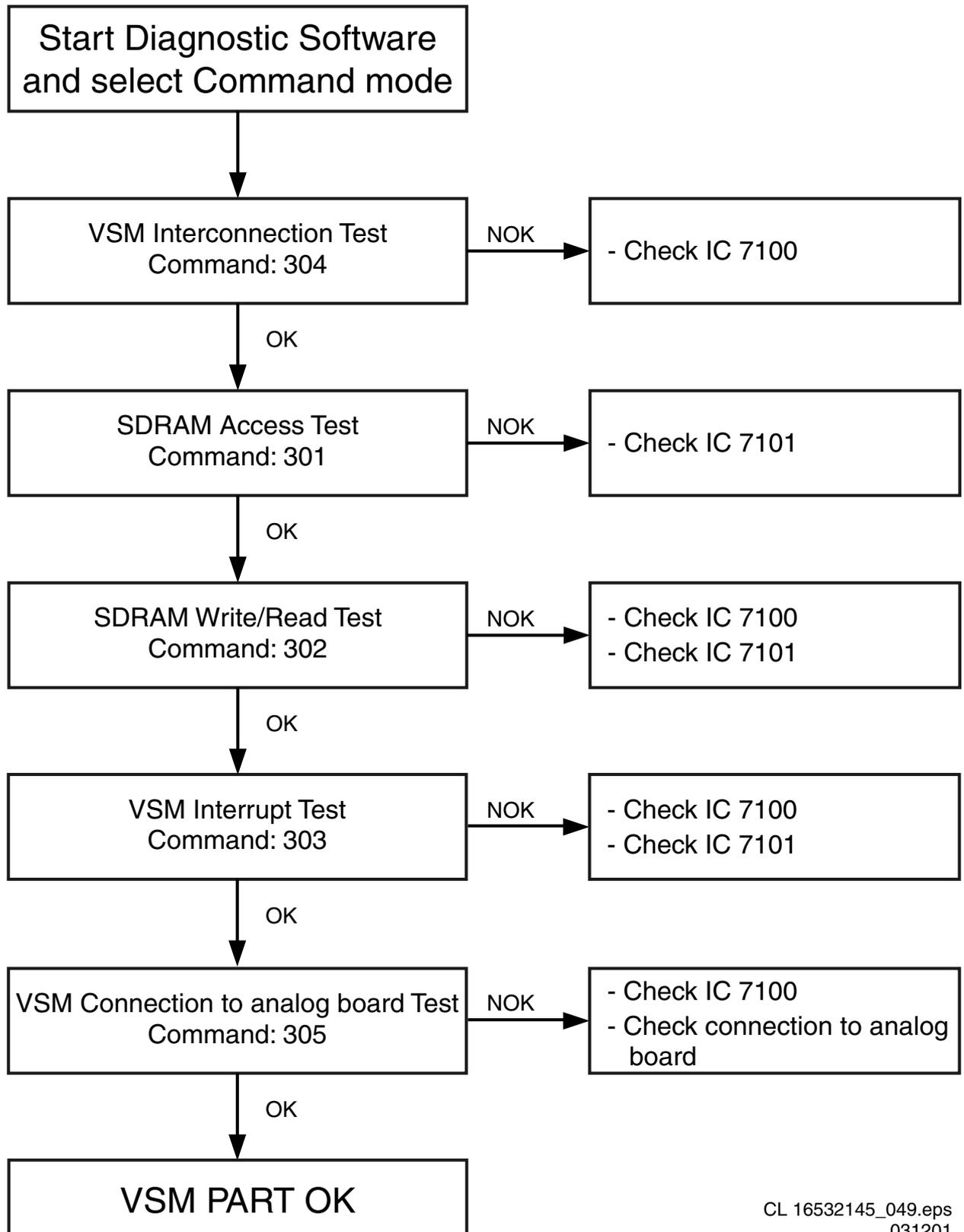


Figure 5-25

DSW VSM TESTS



DSW Audio Part Check

DSW AUDIO PART CHECK

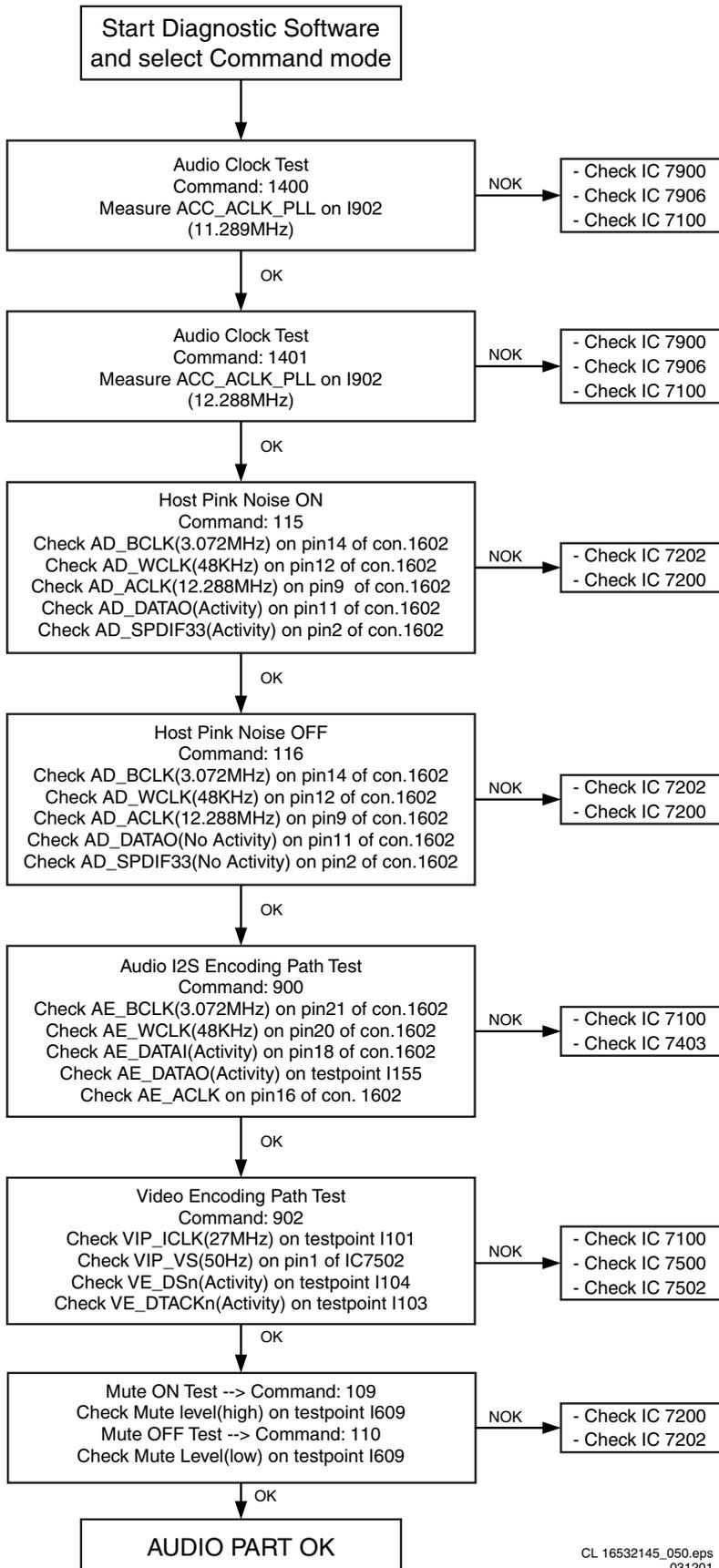
CL 16532145_050.eps
031201

Figure 5-27

DSW Video Part Check

DSW VIDEO PART CHECK

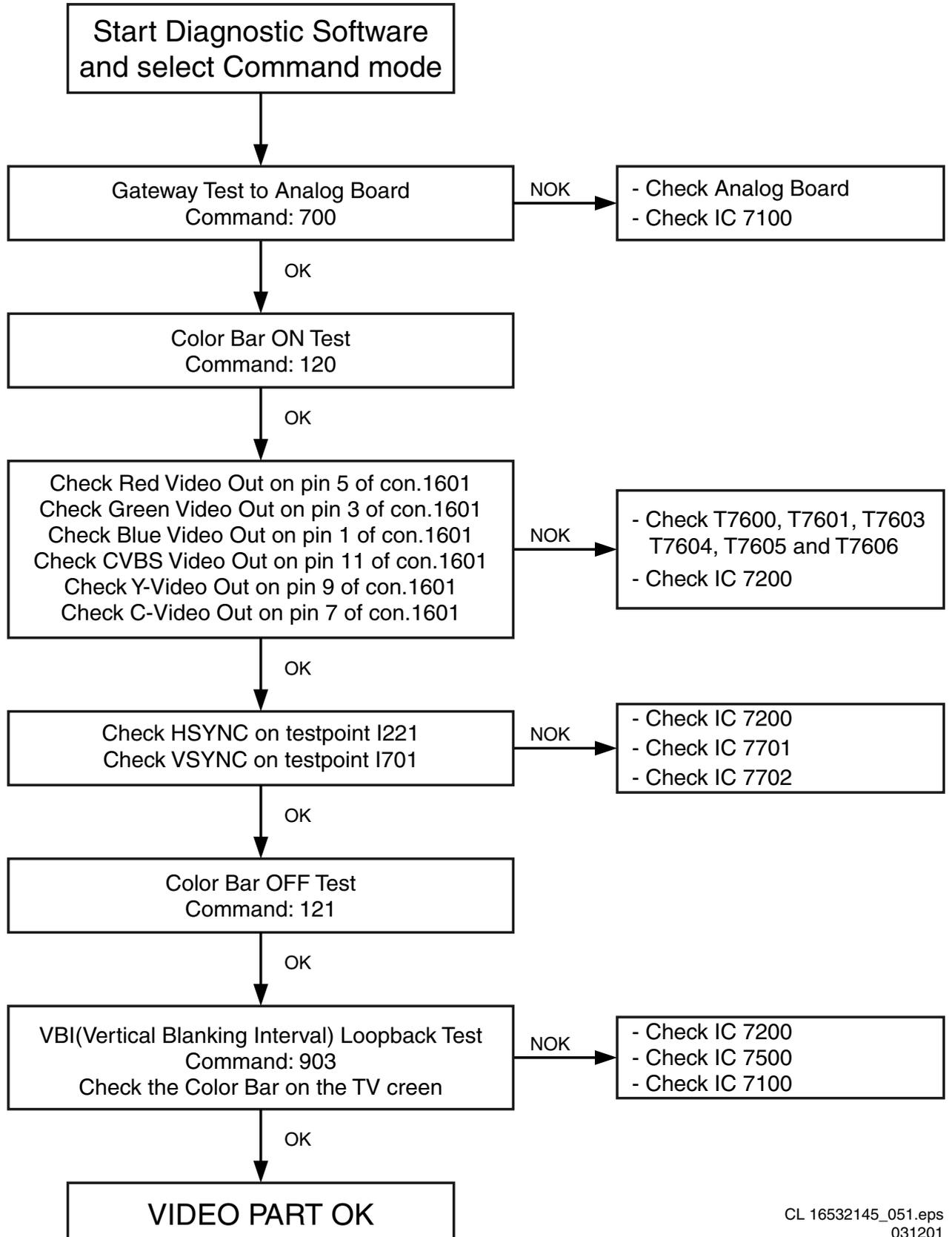
CL 16532145_051.eps
031201

Figure 5-28

VIDEO PART CHECK PROGRESSIVE SCAN

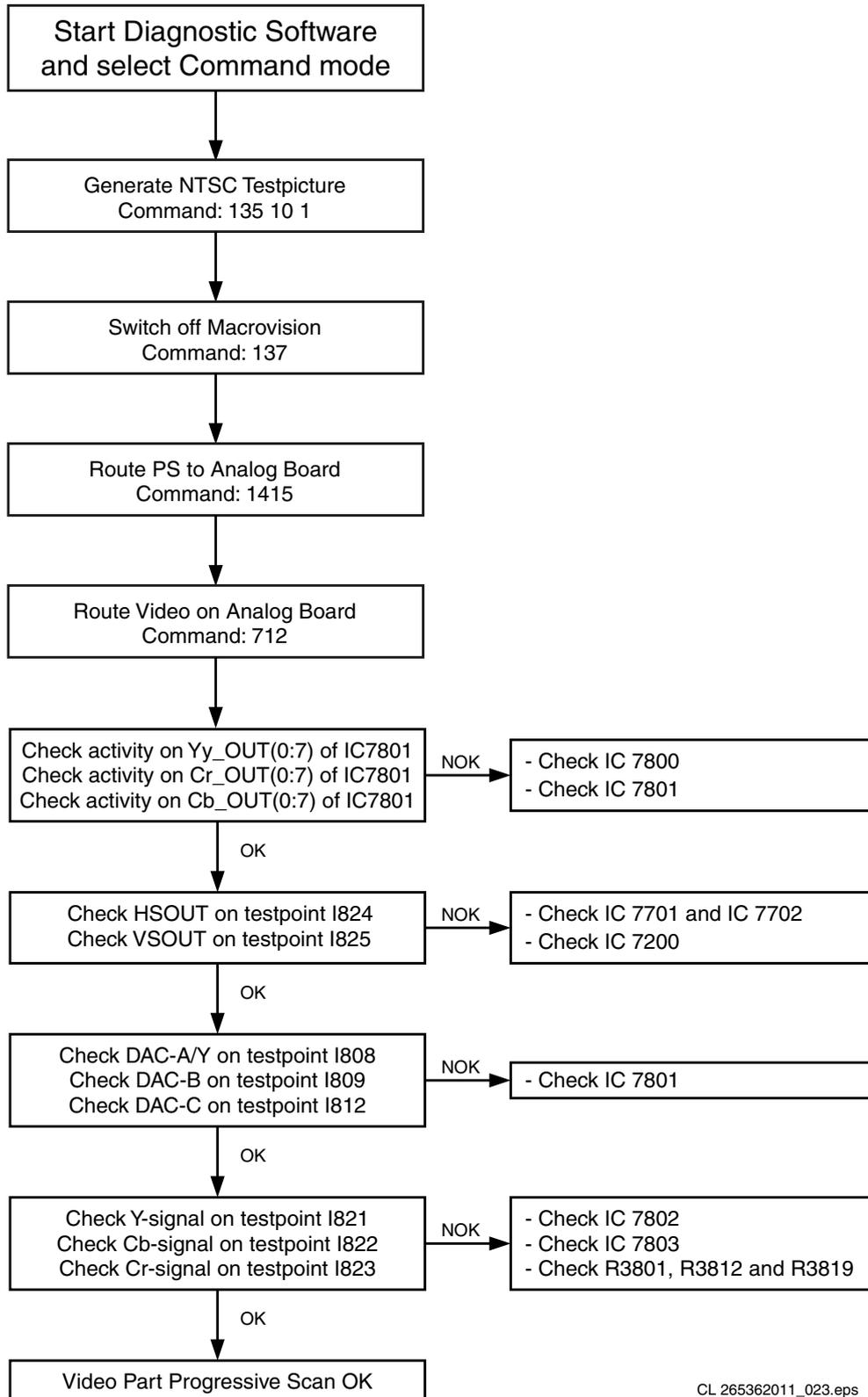
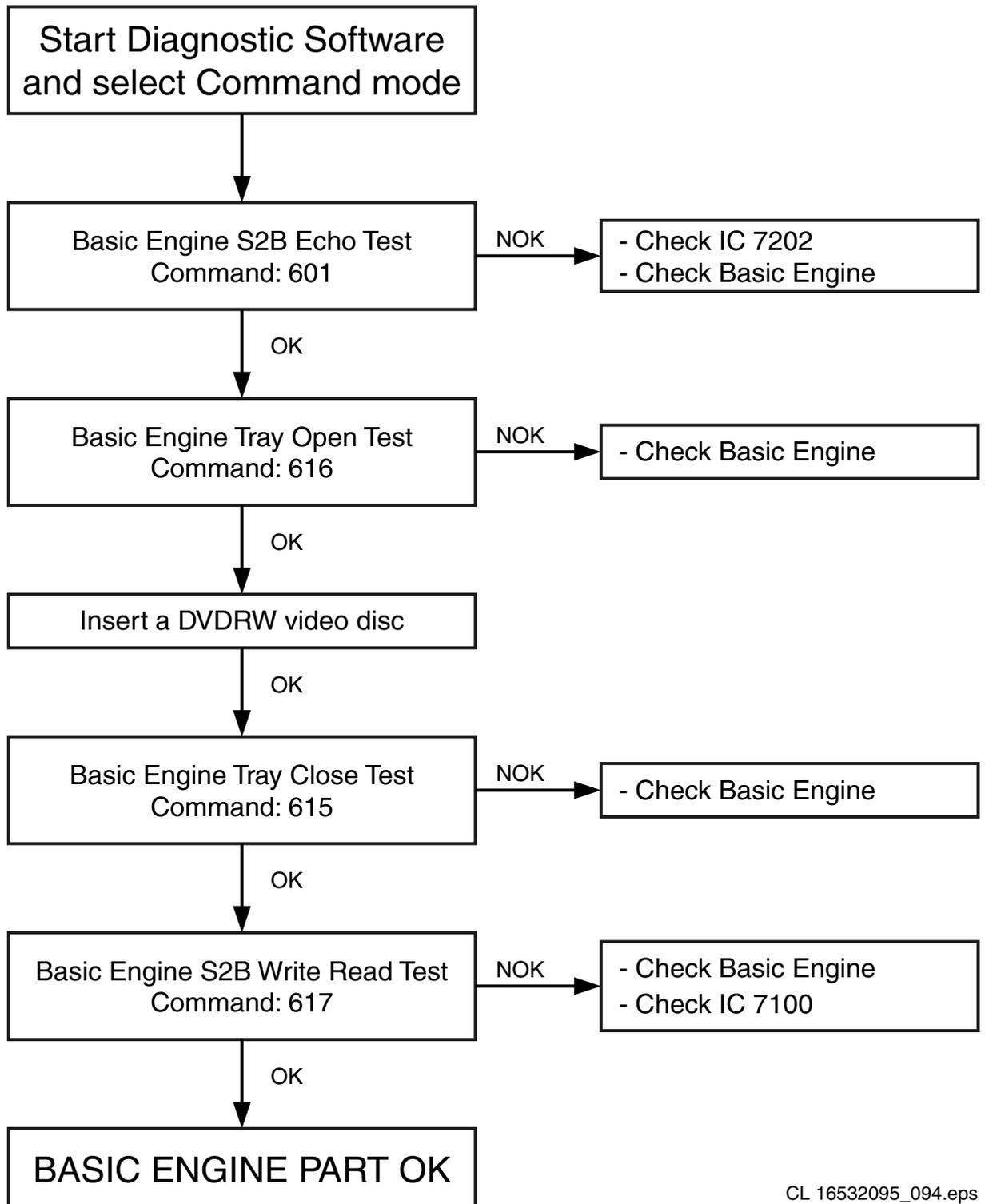


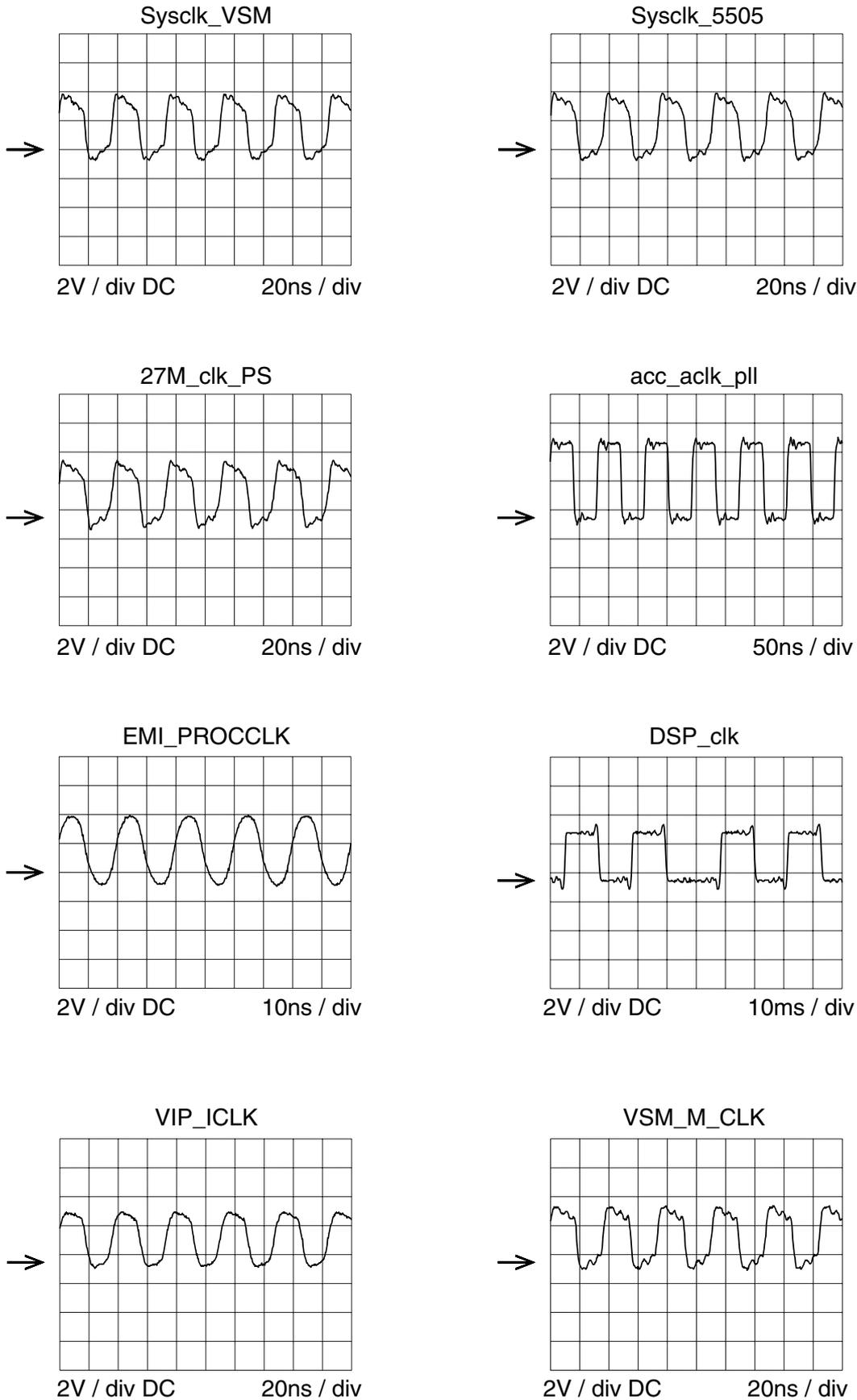
Figure 5-29

DSW BASIC ENGINE TESTS



Waveforms

Waveforms Digital Board



CL 16532145_053.eps
031201

Figure 5-31

Waveforms Digital Board

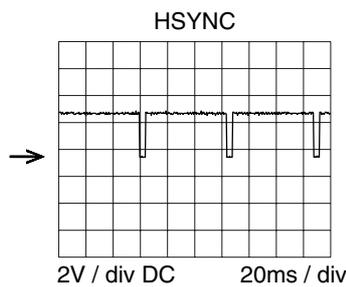
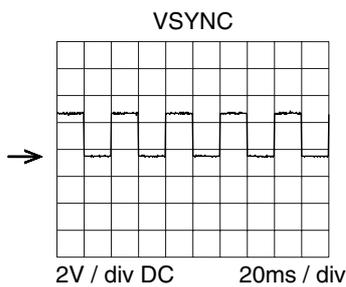
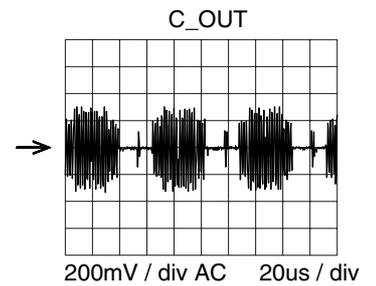
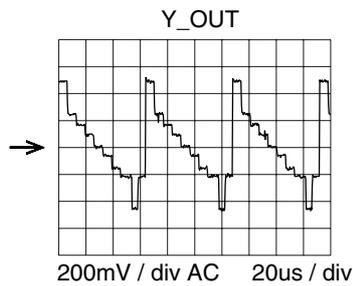
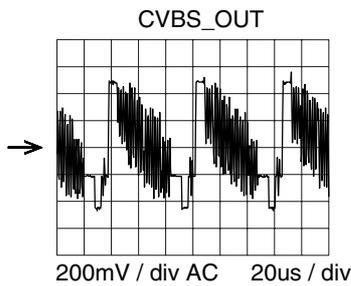
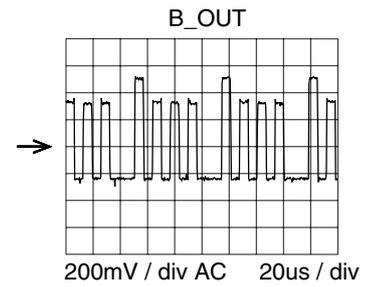
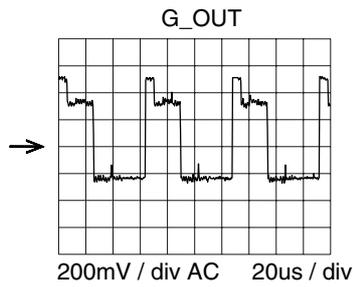
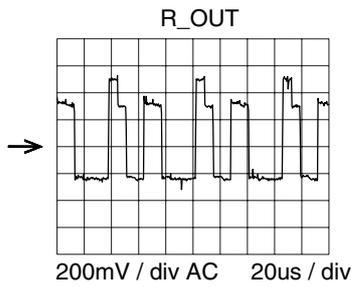
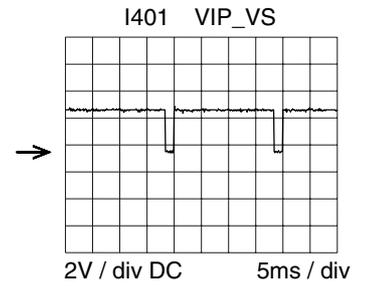
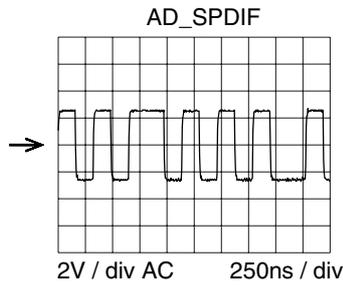
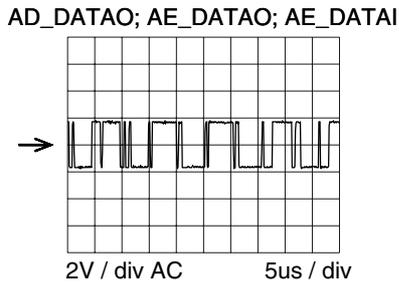
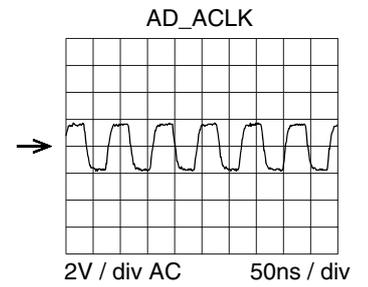
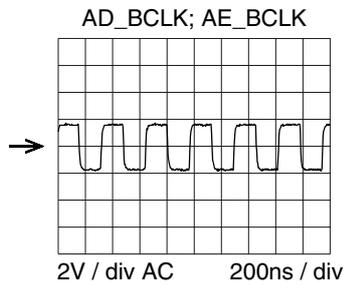
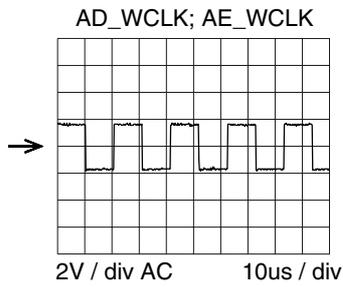


Figure 5-32

Waveforms Digital Board

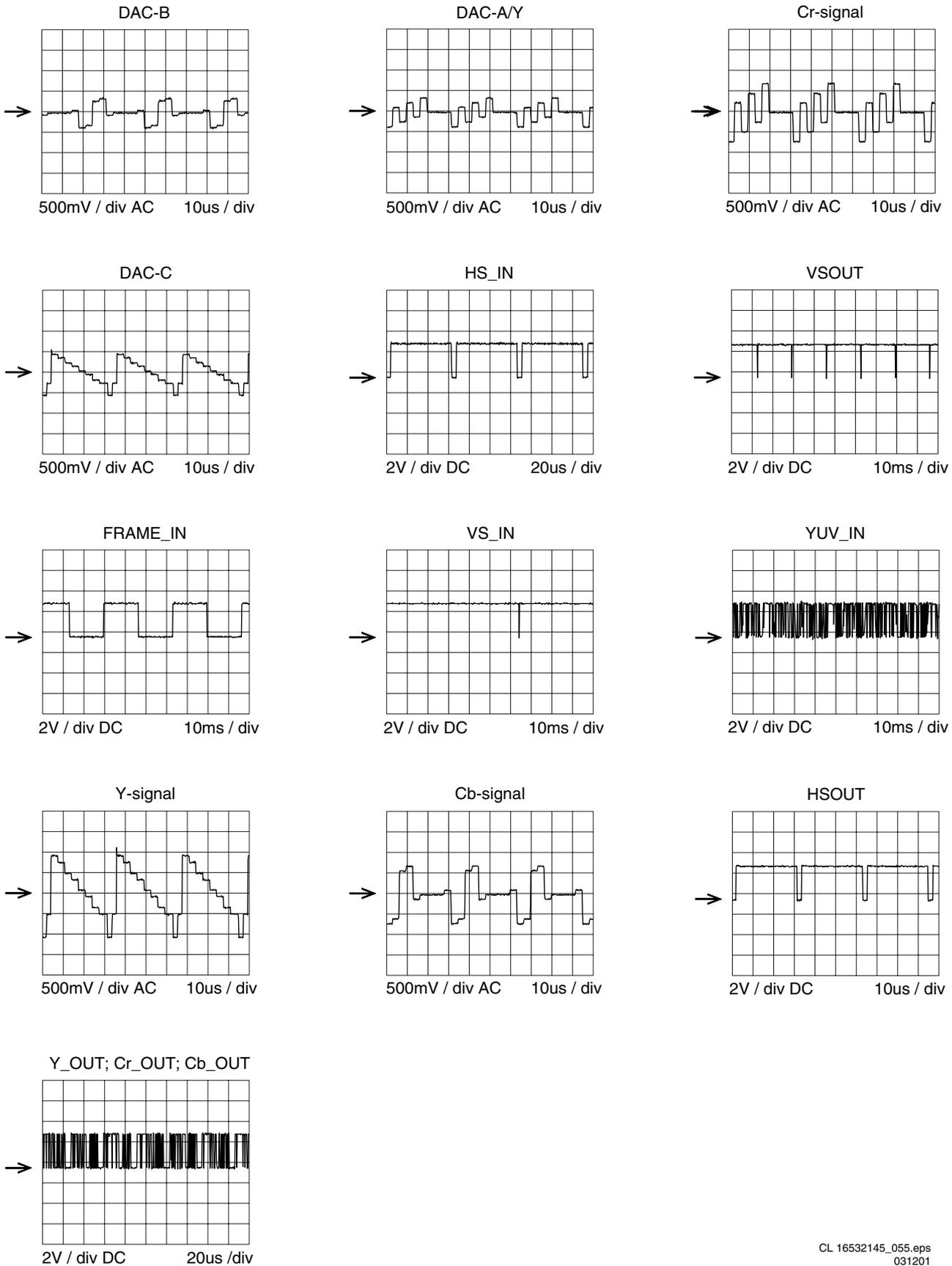


Figure 5-33

5.6.4 Analogue board

Measurement Points Overview

Measurement Point Overview for EURO

MP	X	Y	Signal Name	Signal Description	Signal Type	Part	Schematics Name	Coord.
F5002			ARIn_SC2	SC2 A R IN	NF IN	1950 2B	IO4	C9
F5006			ALIn_SC2	SC2 A L IN	NF IN	1950 6B	IO4	C9
F5020			YCVBSIN_SC2	SC2 Y IN	Sin IN	1950 20B	IO4	F9
F536			BC_SC1	SC1 BC	Sin Out*	1950 7A	IO1	E13
F521			8_SC1	SC1 Ph 8	DC Out	1950 8A	IO1	F13
F515			P50_SC1	SC1 P50	DC Out	1950 10A	IO1	F14
F524			Gout_SC1	SC1 G Out	Sin Out	1950 11A	IO1	F13
F527			RCOut_SC1	SC1 RC Out	Sin Out	1950 15A	IO1	G14
F5007			FBOut_SC1	SC1 FB Out	DC Out	1950 16A	IO1	H13
F5030			BC_SC2	SC2 B IN C Out	Sin In*	1950 7B	IO4	D9
F5008			8_SC2	SC2 Ph 8	DC Out	1950 8B	IO4	D9
F5011			Gin_SC2	SC2 G In	Sin In	1950 11B	IO4	D9
F5015			RCIn_SC2	SC2 RC In	Sin In	1950 15B	IO4	E9
F5016			FBin_SC2	SC2 FB In	DC In	1950 16B	IO4	E9
F5401			A_V	A_V to DIGI	Sin Out	1954 01	IO1	I3
F5402			GNDV	GNDV to DIGI	GND	1954 02	IO1	I4
F5403			A_U	A_U to DIGI	Sin Out	1954 03	IO1	I4
F5405			A_Y	A_Y to DIGI	V Out	1954 05	IO1	I4
F5407			A_C	A_C to DIGI	Sin Out	1954 07	IO1	I4
F5409			A_YCVBS	A YCVBS to DIGI	V Out	1954 09	IO1	I4
F5412			D_CVBS	D CVBS f. DIGI	V In	1954 12	IO1	I5
F5414			D_Y	D_Y f. DIGI	V In	1954 14	IO1	I5
F5416			D_C	D C f. DIGI	Sin In	1954 16	IO1	I5
F5418			D_R	D_T f. DIGI	Sin In	1954 18	IO1	I6
F5420			D_G	D G f. DIGI	Sin In	1954 20	IO1	I6
F5422			D_B	D_B f. DIGI	Sin In	1954 22	IO1	I6
F5301			AFERI	A R from FC	NF In	1953 1	IO1	I1
F5303			AFCLI	A L from FC	NF In	1953 3	IO1	I1
F5304			CVBSFIN	CVBS from FC	V In	1953 4	IO1	I1
F5307			CFIN	C from FC	Sin In	1953 7	IO1	I2
F5309			YFIN	Y from FC	V In	1953 9	IO1	I2
F012			DAINOPT	A D Opt to DIGI		1900 20	DAC	A1
F013			DAINCOAX	A D Coax to DIGI		1900 21	DAC	A1
F014			DAOUT	A D from DIGI		1900 20	DAC	A1
F0002			A_BCLK	BCLK from DIGI	CLK In	1900 2	DAC	E2
F0003			A_WCLK	WCLK from DIGI	CLK In	1900 3	DAC	D2
F0005			A_DAT	A Data to DIGI	Data Out	1900 5	DAC	D2
F0007			A_PCMCLK	PCMCLK from DIGI	CLK In	1900 7	DAC	D2
F0009			D_BCLK	BCLK from DIGI	CLK In	1900 9	DAC	D2
F0011			D_WCLK	WCLK from DIGI	CLK In	1900 11	DAC	D2
F0012			D_DATA0	A Data from DIGI	Data In	1900 12	DAC	C2
F0014			D_PCMCLK	PCMCLK from DIGI	CLK In	1900 14	DAC	C2
F0016			D_KILL	A Kill from DIGI	DC In	1900 16	DAC	C2
F010			ARDAC	A R from DAC	NF Out	7002 1	DAC	C9
F011			ALDAC	A L from DAC	NF Out	7002 7	DAC	E9
F331			RCALOut	A L Rear Cinch Out	NF Out	1958 4B	IO3	E9
F334			RCAROut	A R Rear Cinch Out	NF Out	1958 5B	IO3	E9
F336			RCVBSOut	V Rear Cinch Out	V Out	1959 1B	IO3	C9

MP	X	Y	Signal Name	Signal Description	Signal Type	Part	Schematics Name	Coord.
F800			F_MODE	Fact. Mode	Condition	AIO1	AIO1	C10
F3201			12V	12 V Supply	PS IN	1932 1	PS	C1
F3202			5V	5 V Supply	PS IN	1932 2	PS	C1
F3203			5NSTBY	5 V Supply	PS IN	1932 3	PS	C1
F3204			VGNSTBY	Supply GND	PS IN	1932 4	PS	C1
F3205			33STBY	33 V Supply	PS IN	1932 5	PS	D1
F3206			FLYB	Controls PS	DC Gen	1932 6	PS	D1
F3207			GND A	Ground Analogue	GND	1932 7	PS	D1
F0017			3VD	3V3 Supply	PS IN	1900 17	DAC	B1
F0001			GND D	Ground Digital	GND	1900 01	DAC	E1
F803			INT Clock	Clock Adjust	Count Out	7811 7	AIO1	H5
F900			5STBY2	5V AIO	DC Out	7803 12	AIO2	D3
F902			IReset	Inverse Reset	DC Out *	7803 115	AIO2	D2
F8111			5M	5 V Motor	DC Out	1987 12	AIO1	F14
F303			5SW	5SW	DC Out	7703 21	TU	B10
F9336			8SW	8SW	DC Out	2321	PS	B6
F8105			SDA	IIC1	IIC IO	1981 6	AIO1	E13
F8107			SCL	IIC1	IIC IO	1981 8	AIO1	E13
F810			SCL1	IIC2	IIC IO	3804	AIO1	A9
F811			SDA1	IIC2	IIC IO	3805	AIO1	A9
F8104			IPOR1	IPOR to DC	DC Out	1981 5	AIO1	E13
F8101			12STBY	12 V to DC	DC Out	1981 2	AIO1	D13
F8110			5STBY	5 V to DC	DC Out	1981 11	AIO1	F13
F5306			8SW	8 SW to FRONT	DC Out	1953 6	IO1	I1
F8102			VGNSTBY	VGN to DC	GND	1981 3	AIO1	E13
F8202			A_DATA	To DIGI	DC IN	1982 2	AIO1	H13
F8203			D_DATA	To DIGI	DC IN	1982 3	AIO1	H13
F8204			A_RDY	To DIGI	DC IN	1982 4	AIO1	H13
F8205			D_RDY	To DIGI	DC IN	1982 5	AIO1	H13
F8108			INT	TO DC	DC IN	1981 9	AIO1	F13
F8109			RC	TO DC	DC IN	1981 10	AIO1	F13
F8201			IRESET DIG	TO DIGI	DC IN	1982 1	AIO1	H13
F513			GND A	SC1 GND A	DC IN	1950 4A	IO1	E14
F517			ARIn_SC1	SC1 A R IN	NF IN	1950 2A	IO1	E13
F519			ALIn_SC1	SC1 A L IN	NF IN	1950 6A	IO1	E14
F534			YCVBSIN_SC1	SC1 Y IN	V IN	1950 20A	IO1	I13
F525			GND V	SC1 GND V	GND	1950 21A	IO1	H14
F5001			AROut_SC2	SC2 A R Out	NF Out	1950 1B	IO4	C9
F5003			ALOutSC2	SC2 A L Out	NF Out	1950 3B	IO4	C9
F5004			GND A	SC2 GND A	GND	1950 4B	IO4	C9
F5019			YCVBSOut_SC2	SC2 Y Out	V Out	1950 19B	IO4	C9
F5021			GND V	SC2 GND V	GND	1950 21B	IO4	C9
F516			AROut_SC1	SC1 A R Out	NF Out	1950 1A	IO1	E14
F518			ALOutSC1	SC1 A L Out	NF Out	1950 3A	IO1	E14
F531			YCVBSOut_SC1	SC1 Y Out	V Out	1950 19A	IO1	G13

Figure 5-34

Measurement Point Overview for NAFTA

MP	Signal Name	Signal Description	Signal Type	Part	Schematics Name	Coord.
F5101	ARCRI	A L Rear Cinch In	NF In	1958 1A	IO2	D2
F5103	ARCLI	A R Rear Cinch In	NF In	1958 2A	IO2	E2
F5202	RCVBSIn	V Rear Cinch In	V In	1959 2A	IO2	C2
F5503	RSVHSYIn	Y Rear SVHS In	V In	1955 3B	IO2	B2
F5504	RSVHSCIIn	C Rear SVHS In	Sin In	1955 4B	IO2	B2
F5308	RSVHSYOut	Y Rear SVHS Out	V Out	1955 3A	IO3	A9
F337	RSVHSCOOut	C Rear SVHS Out	Sin Out	1955 4A	IO3	A9
F6001	DVAR	A R from DIGI	Sin In	1960 1	AP	D1
F6002	GND A	GND A	GND	1960 2	AP	D1
F6004	DVAL	A L from DIGI	Sin In	1960 4	AP	D1
F700	IF	IF Out	DC Out	1705 11	TU	C3
F701	IF In	IF In	Sin In	1705 11	TU	C3
F702	GND FV	GND FV	GND	1705 12	TU	C2
F703	GND FV	GND FV	GND	1700 3	TU	B6
F704	40.4	40.4 Trap	Sin Out	1700 1	TU	B5
F705	AGC	AGC	DC Out	3701	TU	A4
F812	SYNC	SYNC from Sepa.	Freq Out	7803 33	AIO1	F6
F4202	DIG OUT L	Digital Out Low	GND	1954 2	DIGI	B4
F4203	DIG OUT H	Digital Out High	Sin Out	1945 3	DIGI	A4
F4204	OPT OUT	Optical Out	DC Out	1943 1	DIGI	D3
F806	FAN OUT	FAN Out	DC Out	1984 1	FACO	C5
F807	FAN IN	FAN In	DC In	1985 1	FACO	F1
F8206	ION	ION_FAN	DC Out	1982 6	AIO1	H13
F8208	BE_FAN	BE_FAN	DC Out	1982 8	AIO1	I13
F8209	FB	FBIN SC2	DC Out	1982 9	AIO1	I13
F8210	GND D	GND D	GND D	1982 10	AIO1	I13

Remark: Indicator * means more than one signal type

MP	Signal Name	Signal Description	Signal Type	Part	Schematics Name	Coord.
F800	F_MODE	12 V Supply	PS IN	1932 1	AIO1	C10
F3201	12V	12 V Supply	PS IN	1932 1	PS	C1
F3202	5V	5 V Supply	PS IN	1932 2	PS	C1
F3203	5VNSTBY	5 V Supply	PS IN	1932 3	PS	C1
F3204	VGNSTBY	Supply GND	PS IN	1932 4	PS	C1
F3205	33STBY	33 V Supply	PS IN	1932 5	PS	D1
F3206	FLYB	Controls PS	DC Gen	1932 6	PS	D1
F3207	GND A	Ground Analogue	GND	1932 7	PS	D1
F0017	3VD	3V3 Supply	PS IN	1900 17	DAC	B1
F001	GND D	Ground Digital	GND	1900 01	DAC	E1
F803	INT Clock	Clock Adjust	Count Out	7811 7	AIO1	H5
F900	5STBY2	5V AIO	DC Out	7803 12	AIO2	D3
F902	IFReset	Inverse Reset	DC Out *	7803 115	AIO2	D2
F8111	5M	5 V Motor	DC Out	1987 12	AIO1	F14
F303	5SW	5SW	DC Out	7703 21	TU	B10
F9336	8SW	8SW	DC Out	2321	PS	B6
F8105	SDA	IIC IO	IIC IO	1981 6	AIO1	E13
F8107	SCL	IIC IO	IIC IO	1981 8	AIO1	E13
F810	SCL1	IIC IO	IIC IO	3804	AIO1	A9
F811	SDA1	IIC IO	IIC IO	3805	AIO1	A9
F8104	IPOR1	IPOR to DC	DC OUT	1981 5	AIO1	E13
F8101	12STBY	12 V to DC	DC Out	1981 2	AIO1	D13
F8110	5STB	5 V to DC	DC Out	1981 11	AIO1	F13
F5306	8SW	8 SW to FRONT	DC Out	1953 6	IO1	I1
F8102	VGNSTBY	VGN to DC	GND	1981 3	AIO1	E13
F8202	A_DATA	To DIGI	DC In	1982 2	AIO1	H13
F8203	D_DATA	To DIGI	DC In	1982 3	AIO1	H13
F8204	A_RDY	To DIGI	DC In	1982 4	AIO1	H13
F8205	D_RDY	To DIGI	DC In	1982 5	AIO1	H13
F8108	INT	To DC	DC In	1981 9	AIO1	F13
F8109	RC	To DC	DC In	1981 10	AIO1	F13
F8201	IRESET_DIG	To DIGI	DC In	1982 1	AIO1	H13
F5103	ARIn_2	A R IN 2	NF IN	1958 3A	IO3	E13
F5101	ALIn_2	A L IN 2	NF IN	1958 1A	IO3	E14
F5906	GND V	GND V	GND	1957 6A	IO1	H12
F5806	GND V	GND V	GND	1956 6A	IO1	I8
F510	AROut_1	A R Out 1	NF Out	1959 5B	IO1	E13
F509	ALOut_1	A L Out 1	NF Out	1959 4B	IO1	D13
F5201	RCVBSOut2	SC1 Y Out	V Out	1997 1B	IO3	A8
F5105	ARIn_1	A R IN 1	NF IN	1959 1A	IO2	E2
F5104	ALIn_1	A L IN 1	NF IN	1959 4A	IO2	E2
F5202	RCVBSIn	Y IN	Sin IN	1997 2A	IO2	C2
F5905	Y_OUT	Y Out	Sin Out*	1957 5A	IO1	I12
F5801	U_IN	U IN	Sin In*	1956 1B	IO1	I10
F5805	Y_IN	Y IN	Sin In	1956 5A	IO1	I9
F5802	V_IN	V IN	Sin In	1956 2B	IO1	I10

Figure 5-35

MP	X	Y	Signal Name	Signal Description	Signal Type	Part	Schematics Name Coord.
F4202			DIG_OUT L	Digital Out Low	GND	1954 2	DIGI B4
F4203			DIG_OUT H	Digital Out High	Sin Out	1945 3	DIGI A4
F4204			OPT_OUT	Optical Out	DC Out	1943 1	DIGI D3
F806			FAN_OUT	FAN Out	DC Out	1984 1	FACO C5
F807			FAN_IN	FAN In	DC In	1985	FACO F1
F8206			ION	ION_FAN	DC Out	1982 6	AIO1 H13
F8208			BE_FAN	BE_FAN	DC Out	1982 8	AIO1 I13
F8209			FB	FBIN SC2	DC Out	1982 9	AIO1 I13
F8210			GNDD	GNDD	GNDD	1982 10	AIO1 I13

Remark:
Indicator * means more than one signal type

MP	X	Y	Signal Name	Signal Description	Signal Type	Part	Schematics Name Coord.
F5401			A_V	A V to DIGI	Sin Out	1954 01	IO1 I3
F5402			GNDV	GNDV to DIGI	GND	1954 02	IO1 I4
F5403			A_U	A U to DIGI	Sin Out	1954 03	IO1 I4
F5405			A_Y	A Y to DIGI	V Out	1954 05	IO1 I4
F5407			A_C	A C to DIGI	Sin Out	1954 07	IO1 I4
F5409			A_YCVBS	A YCVBS to DIGI	V Out	1954 09	IO1 I4
F5412			D_CVBS	D_CVBS f. DIGI	V In	1954 12	IO1 I5
F5414			D_Y	D Y f. DIGI	V In	1954 14	IO1 I5
F5416			D_C	D C f. DIGI	Sin In	1954 16	IO1 I5
F5418			D_R	D R f. DIGI	Sin In	1954 18	IO1 I6
F5420			D_G	D G f. DIGI	Sin In	1954 20	IO1 I6
F5422			D_B	D B f. DIGI	Sin In	1954 22	IO1 I6
F5301			AFCLI	A R from FC	NF In	1953 1	IO1 I1
F5303			AFCLI	A L from FC	NF In	1953 3	IO1 I1
F5304			CVBSFIN	CVBS from FC	V In	1953 4	IO1 I1
F5307			CFIN	C from FC	Sin In	1953 7	IO1 I2
F5309			YFIN	Y from FC	V In	1953 9	IO1 I2
F012			DAINOPT	A D Opt to DIGI		1900 20	DAC A1
F013			DAINCOAX	A D Coax to DIGI		1900 21	DAC A1
F014			DAOUT	A D from DIGI		1900 20	DAC A1
F002			A_BCLK	BCLK from DIGI	CLK In	1900 2	DAC E2
F003			A_WCLK	WCLK from DIGI	CLK In	1900 3	DAC D2
F005			A_DAT	A Data to DIGI	Data Out	1900 5	DAC D2
F007			A_PCMCLK	PCMCLK from DIGI	CLK In	1900 7	DAC D2
F009			D_BCLK	BCLK from DIGI	CLK In	1900 9	DAC D2
F011			D_WCLK	WCLK from DIGI	CLK In	1900 11	DAC D2
F012			D_DATA0	A Data from DIGI	Data In	1900 12	DAC C2
F014			D_PCMCLK	PCMCLK from DIGI	CLK In	1900 14	DAC C2
F0016			D_KILL	A Kill from DIGI	DC In	1900 16	DAC C2
F010			ARDAC	A R from DAC	NF Out	7002 1	DAC C9
F011			ALDAC	A L from DAC	NF Out	7002 7	DAC E9
F513			ALOut_2	A L Rear Out 2	NF Out	1958 4B	IO1 B13
F512			AROut_2	A R Rear Out 2	NF Out	1958 5B	IO1 C13
F5205			RCVBSOut1	V Rear Cinch Out1	V Out	1997 5C	IO3 A8
F5503			RSVHSIn	Y Rear SVHS In	V In	1955 3B	IO2 B2
F5504			RSVHSCIn	C Rear SVHS In	Sin In	1955 4B	IO2 B2
F338			RSVHSYOut	Y Rear SVHS Out	V Out	1955 3A	IO3 A9
F337			RSVHSCOOut	C Rear SVHS Out	Sin Out	1955 4A	IO3 A9
F6001			DVAR	A R from DIGI	Sin In	1960 1	AP D1
F6002			GND A	GND A	GND	1960 2	AP D1
F6004			DVAL	A L from DIGI	Sin In	1960 4	AP D1
F700			IF	IF Out	DC Out	1705 11	TU C3
F701			IF	IF In	Sin In	1705 11	TU C3
F702			GND FV	GND FV	GND	1705 12	TU C2
F703			GND FV	GND FV	GND	1700 3	TU B6
F705			AGC	AGC	DC Out	3701	TU A4
F812			SYNC	SYNC from Sepa.	Freq Out	7803 33	AIO1 F6
F330			RC IN	Remote Control In	DC Out	1993 2	IO3 E2

Figure 5-36

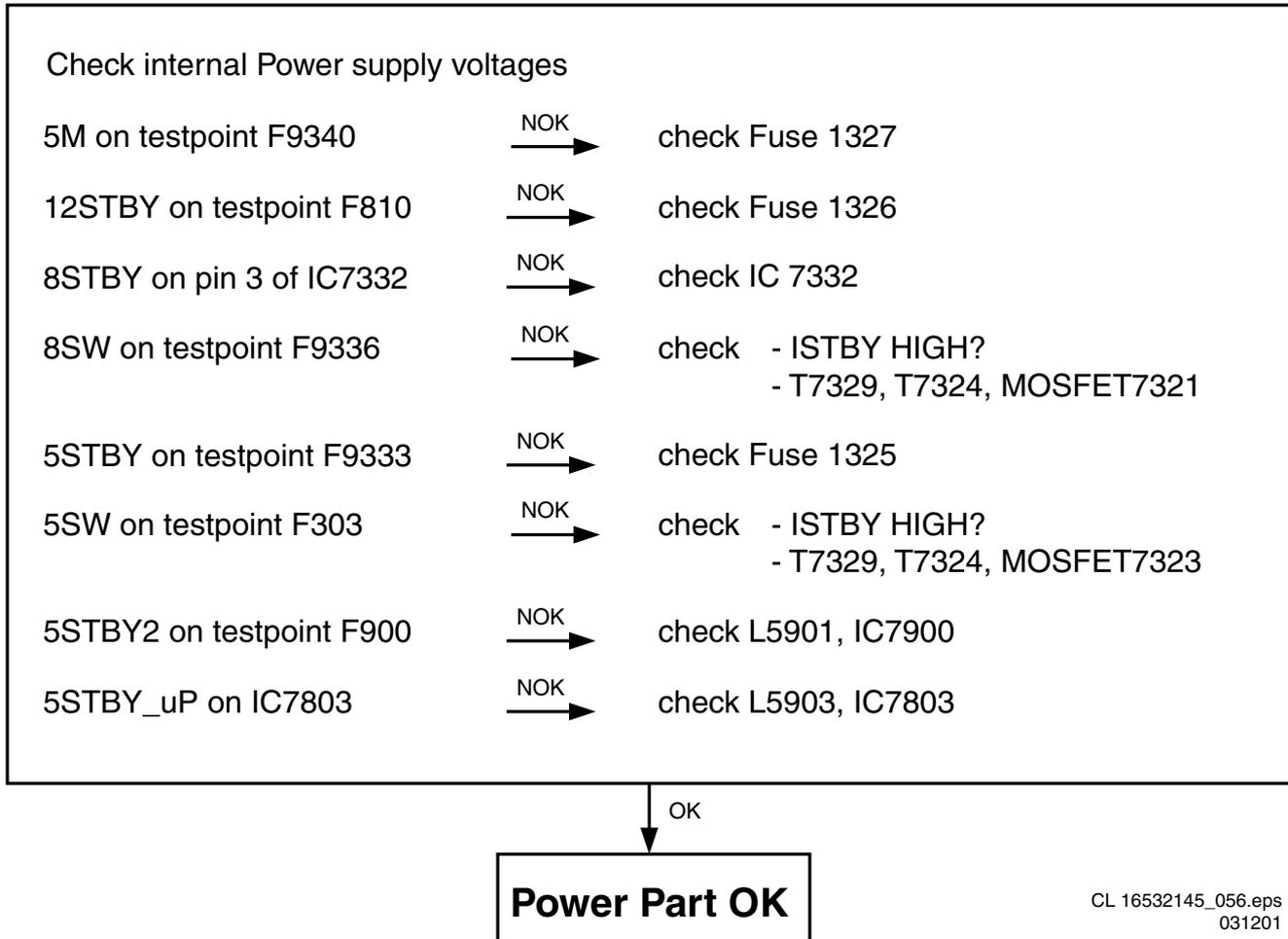
Power Part Check

Figure 5-37

DSW Check Analoge Board

DSW CHECK ANALOGUE BOARD

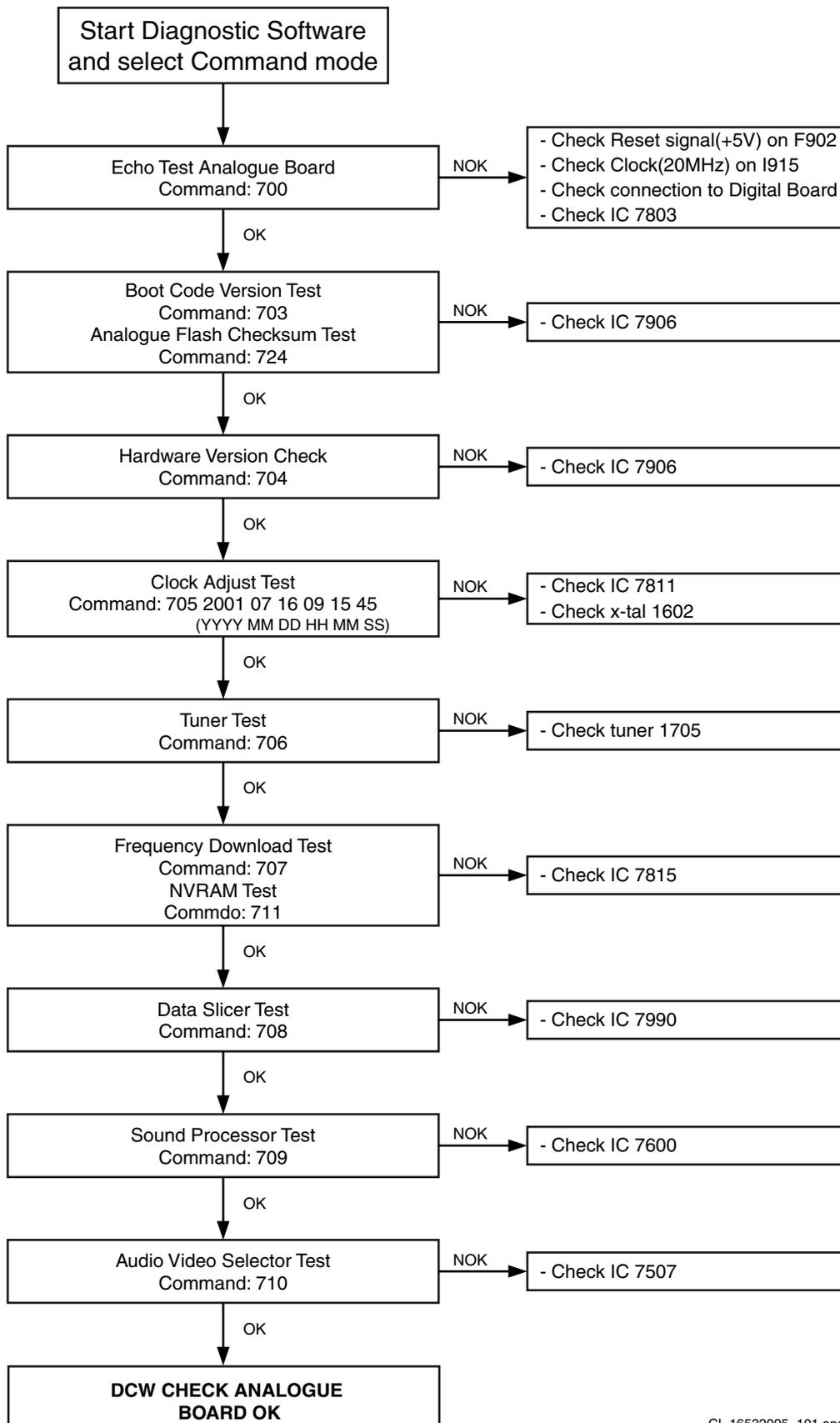
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150801

Figure 5-38

Routing Audio and Video*Route Video*

Nucleus Number: 712

Description

This nucleus routes the video signals on the analogue board to the destination determined by the input parameters

The paths that are available for video routing and their description(Europe version)

PATH ID	DESCRIPTION
00	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.
01	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to the digital board.
02	Input signal is from REAR VIDEO(CVBS) IN and will be routed to the digital board.
03	Input signal is from FRONT S-VIDEO(Y/C) and will be routed to the digital board.
04	Input signal is from REAR S-VIDEO(Y/C) and will be routed to the digital board.
05	Input signal is CVBS from SCART1 and will be routed to the digital board.
06	Input signal is CVBS from SCART2 and will be routed to the digital board.
07	No routing.
08	Input signal is VIDEO(CVBS) from ANTENNA IN and will be routed to SCART1.
09	Input signal is VIDEO(CVBS) from SCART1 and will be routed to SCART2.
10	Input signal is VIDEO(CVBS) from SCART2 and will be routed to SCART1.
11	No routing.
12	Input signal is from REAR VIDEO(CVBS) IN and will be routed to SCART1 and SCART2.
13	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to SCART1.
14	Input signals VIDEO(CVBS and Y/C) from SCART 1 will be routed to SCART2.
15	Input signal is from REAR S-VIDEO(Y/C) IN and will be routed to SCART2.
16	Input signal is from FRONT S-VIDEO(Y/C) IN and will be routed to SCART2.
17	No routing
18	No routing
19	Input signals VIDEO(RGB and FAST BLANKING) from SCART2 will be routed to the corresponding pins of SCART1.
20	Signal path is routed from digital board RGB to RGB SCART1 and from RGB SCART2 to digital board YUV and from digital board CVBS to digital board CVBS.
21	Signal path is routed from digital board YC to REAR S-VIDEO(YC) OUT and from REAR S-VIDEO(YC) IN to digital board YC.

The paths that are available for video routing and their description (Nafta region)

PATH ID	DESCRIPTION
00	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.
01	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to the digital board.
02	Input signal is from REAR VIDEO(CVBS) IN and will be routed to the digital board.
03	Input signal is from FRONT S-VIDEO(Y/C) IN and the signal received will be routed to the digital board.

PATH ID	DESCRIPTION
04	Input signal is from REAR S-VIDEO(Y/C) IN and will be routed to the digital board.
05	Input signal is from YUV IN and will be routed to the digital board.
06	No routing.
07	No routing.
08	Input signal is VIDEO(CVBS) from ANTENNA IN and will be routed to VIDEO(CVBS) OUT and .
09	Input signal is from YUV IN and will be routed to YUV OUT.
10	No routing.
11	No routing.
12	Input signal is from REAR VIDEO(CVBS) IN and will be routed to REAR VIDEO(CVBS) OUT.
13	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to REAR VIDEO(CVBS) OUT.
14	Input signal is from REAR S-VIDEO(Y/C) IN and will be routed to REAR S-VIDEO(Y/C) OUT.
15	Input signal is from FRONT S-VIDEO(Y/C) IN and will be routed to REAR S-VIDEO(Y/C) OUT.
16	No routing.
17	Signal path is routed from digital board RGB to REAR VIDEO(YUV) OUT and from REAR VIDEO(YUV) IN to digital board YUV and from digital board CVBS to digital board CVBS.
18	Signal path is routed from digital board CVBS to REAR VIDEO(CVBS) OUT and from REAR VIDEO(CVBS) IN to digital board CVBS.
19	Signal path is routed from digital board YC to REAR S-VIDEO(YC) OUT and from REAR S-VIDEO(YC) IN to digital board YC.

Example

DD:> 712 01

71200: Video routing on the Analogue Board OK.

Test OK @

Route Audio

Nucleus Number: 713

Description

This nucleus routes the audio on the analogue board to the destination determined by the input parameters

The paths that are available for audio routing and their description (Europe version)

PATH ID	DESCRIPTION
00	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.
01	Input signal is from FRONT AUDIO IN and will be routed to the digital board.
02	Input signal is from REAR AUDIO IN and will be routed to the digital board.
03	Input signal is AUDIO from SCART1 and will be routed to the digital board.
04	Input signal is AUDIO from SCART2 and will be routed to the digital board.
05	No routing.
06	No routing.
07	No routing.
08	Input signal is VIDEO(CVBS) and AUDIO from ANTENNA IN and will be routed to SCART1.
09	Input signal is VIDEO(CVBS) and AUDIO from SCART1 and will be routed to SCART2.
10	Input signal is VIDEO(CVBS) and AUDIO from SCART2 and will be routed to SCART1.
11	Input signal is AUDIO from dvio board and will be routed to SCART1.

PATH ID	DESCRIPTION
12	No routing.
13	No routing.
14	No routing.
15	No routing.
16	No routing.
17	Input signal is from REAR AUDIO IN and will be routed to SCART1.
18	Input signal is from FRONT AUDIO IN and will be routed to SCART1.

The paths that are available for audio routing and their description (Nafta region)

PATH ID	DESCRIPTION
00	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.
01	Input signal is from FRONT AUDIO IN and will be routed to the digital board.
02	Input signal is from REAR AUDIO IN 2 and will be routed to the digital board.
03	Input signal is from FRONT AUDIO IN and will be routed to the digital board.
04	No routing.
05	No routing.
06	No routing.
07	No routing.
08	Input signal is VIDEO(CVBS) and AUDIO from ANTENNA IN and will be routed to VIDEO(CVBS) OUT and REAR CINCH OUT 2.
09	No routing.
10	Input signal is from REAR AUDIO CINCH IN 2 and will be routed to REAR AUDIO CINCH OUT 2.
11	Input signal is from FRONT AUDIO CINCH IN and will be routed to REAR AUDIO CINCH OUT 2.
12	No routing.
13	No routing.
14	No routing.
15	No routing.
16	Input signal is AUDIO from dvio board and will be routed to AUDIO CINCH OUT 2.
17	No routing.
18	No routing.
19	No routing.
20	Input signal is from digital board and will be routed to the REAR AUDIO OUT 1 and input signal is from REAR AUDIO IN 2 and will be routed to the digital board.
21	Input signal is from digital board and will be routed to the REAR AUDIO OUT 1 and input signal is from REAR AUDIO IN 1 and will be routed to the digital board.
22	Input signal is from digital board and will be routed to the REAR AUDIO OUT 2 and input signal is from REAR AUDIO IN 1 and will be routed to the digital board.

EXAMPLE

DD:> 713 00

71300: Audio routing on the Analogue Board OK.

Test OK @

5.6.5 Display Board

TROUBLESHOOTING DISPLAY BOARD

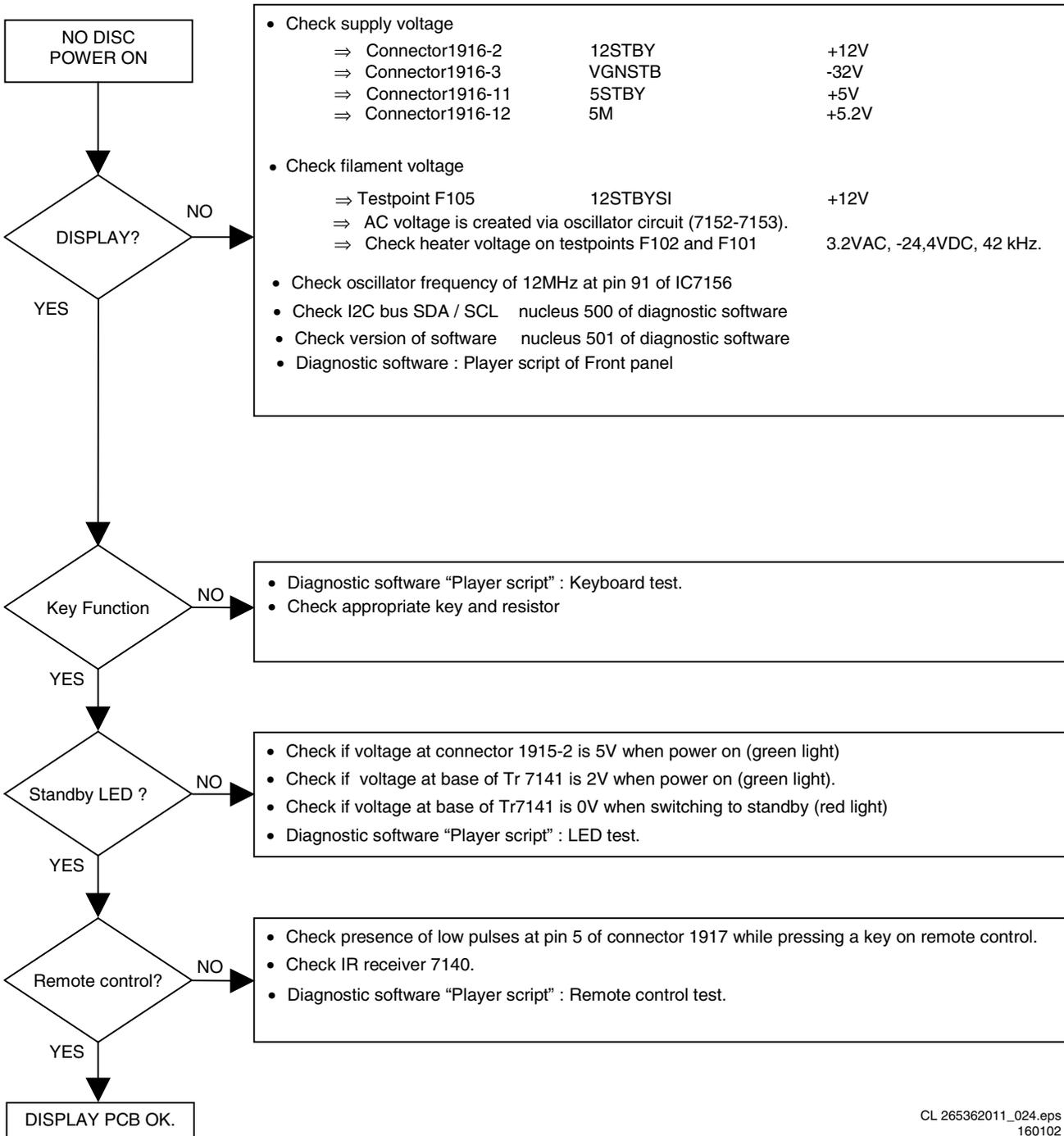


Figure 5-39

DVIO Board

Power part check

POWER PART CHECK DVIO

USE DVIO BOARD CIRCUIT DIAGRAMS 1 2, 3, 4 AND 5 AND DVIO TOP VIEW TESTPOINTS

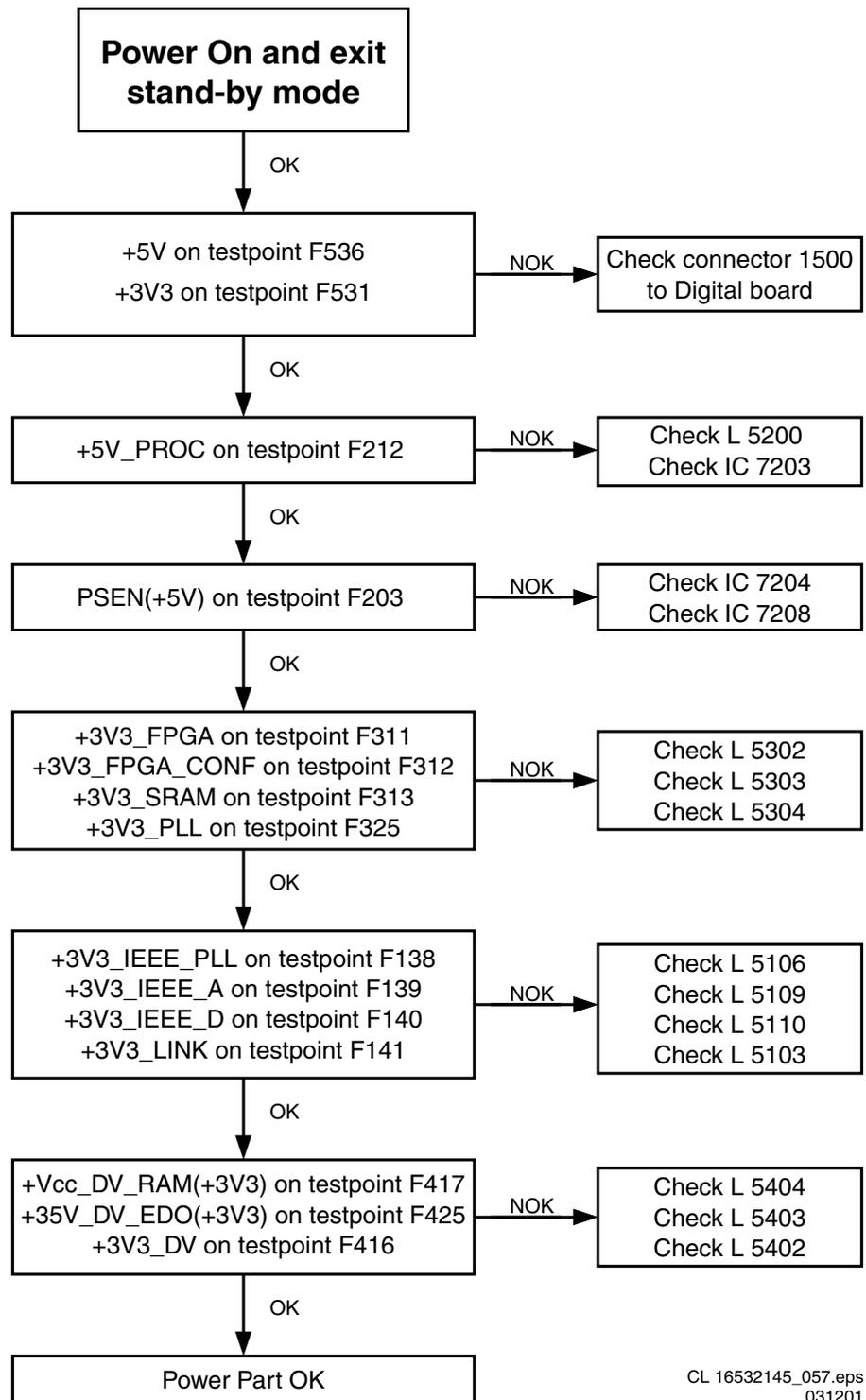
CL 16532145_057.eps
031201

Figure 5-40

RESET & CLOCK CHECK DVIO

USE DVIO BOARD CIRCUIT DIAGRAMS 2, 3, 4 AND 5 AND DVIO TOP VIEW TESTPOINTS

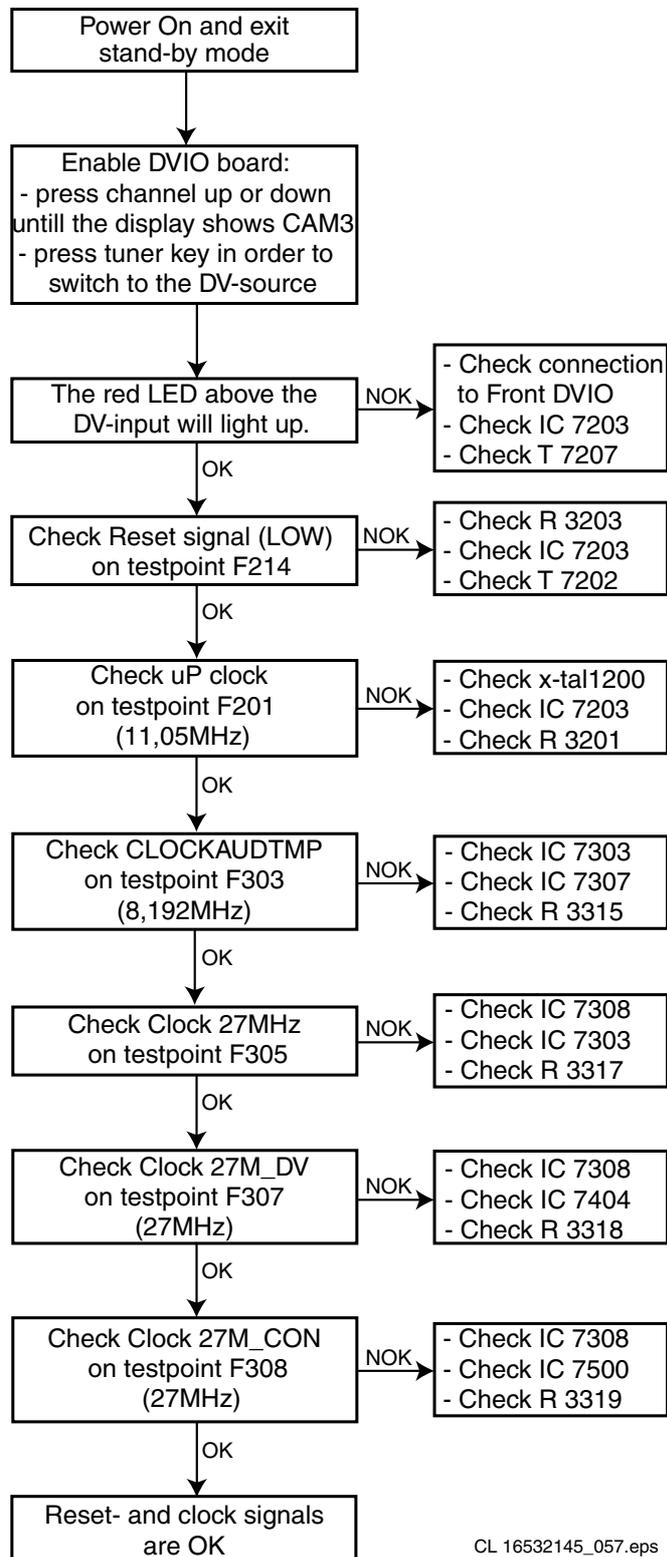


Figure 5-41

DSW DVIO tests

DSW DVIO TESTS

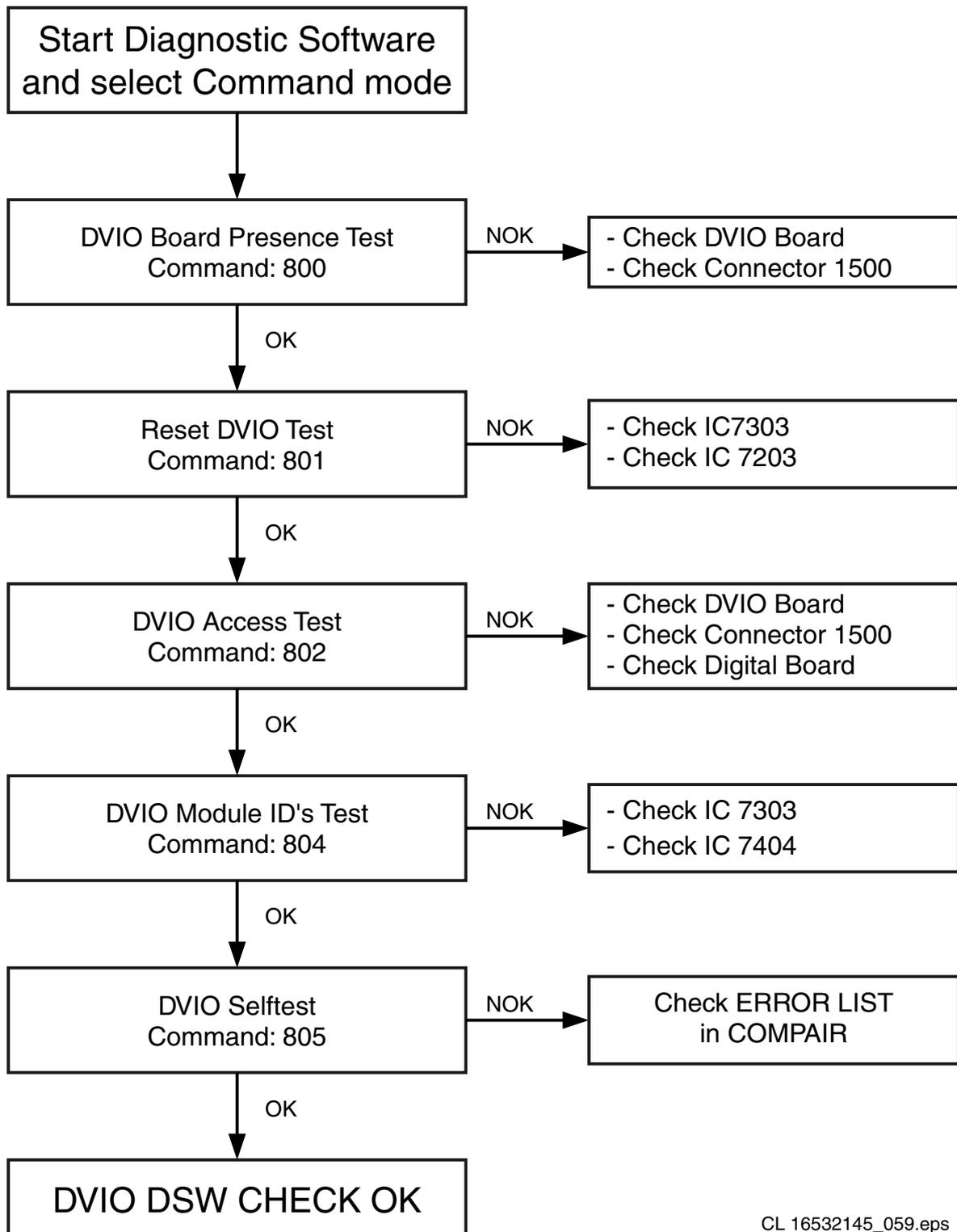
CL 16532145_059.eps
031201

Figure 5-42

Waveforms

Waveforms DVIO

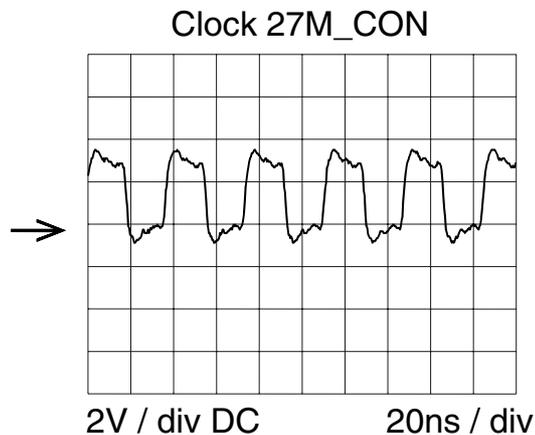
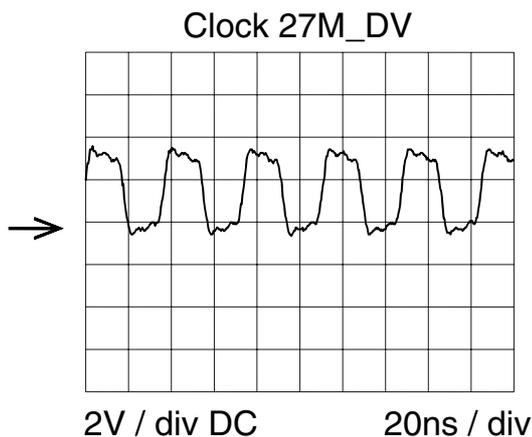
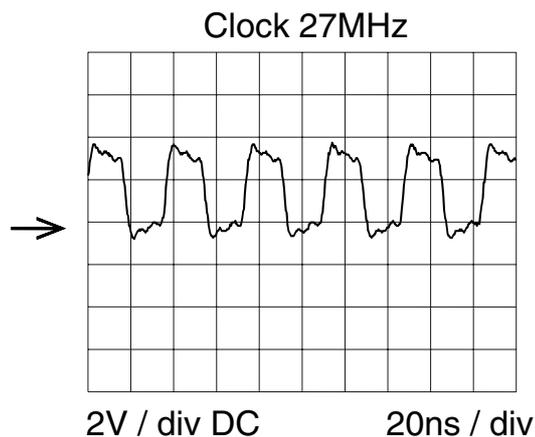
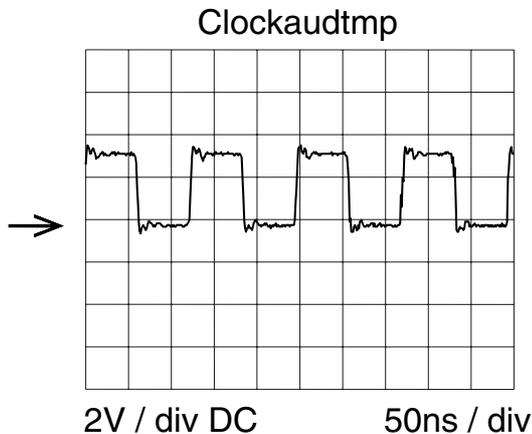
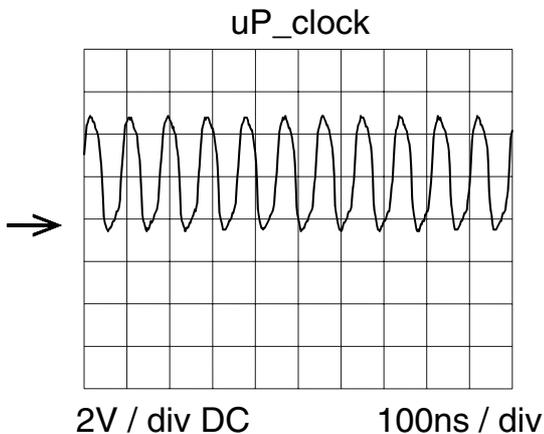
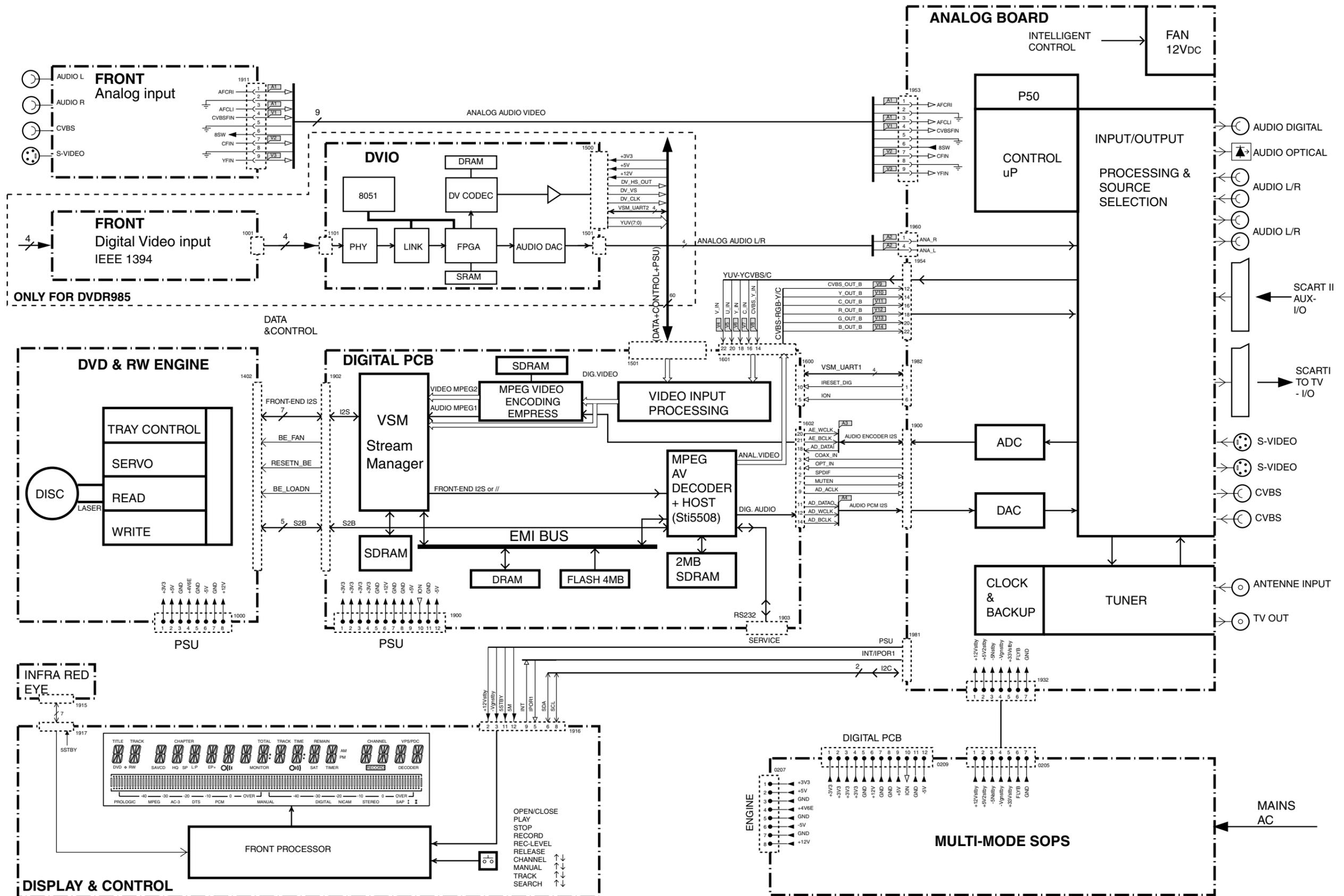


Figure 5-43

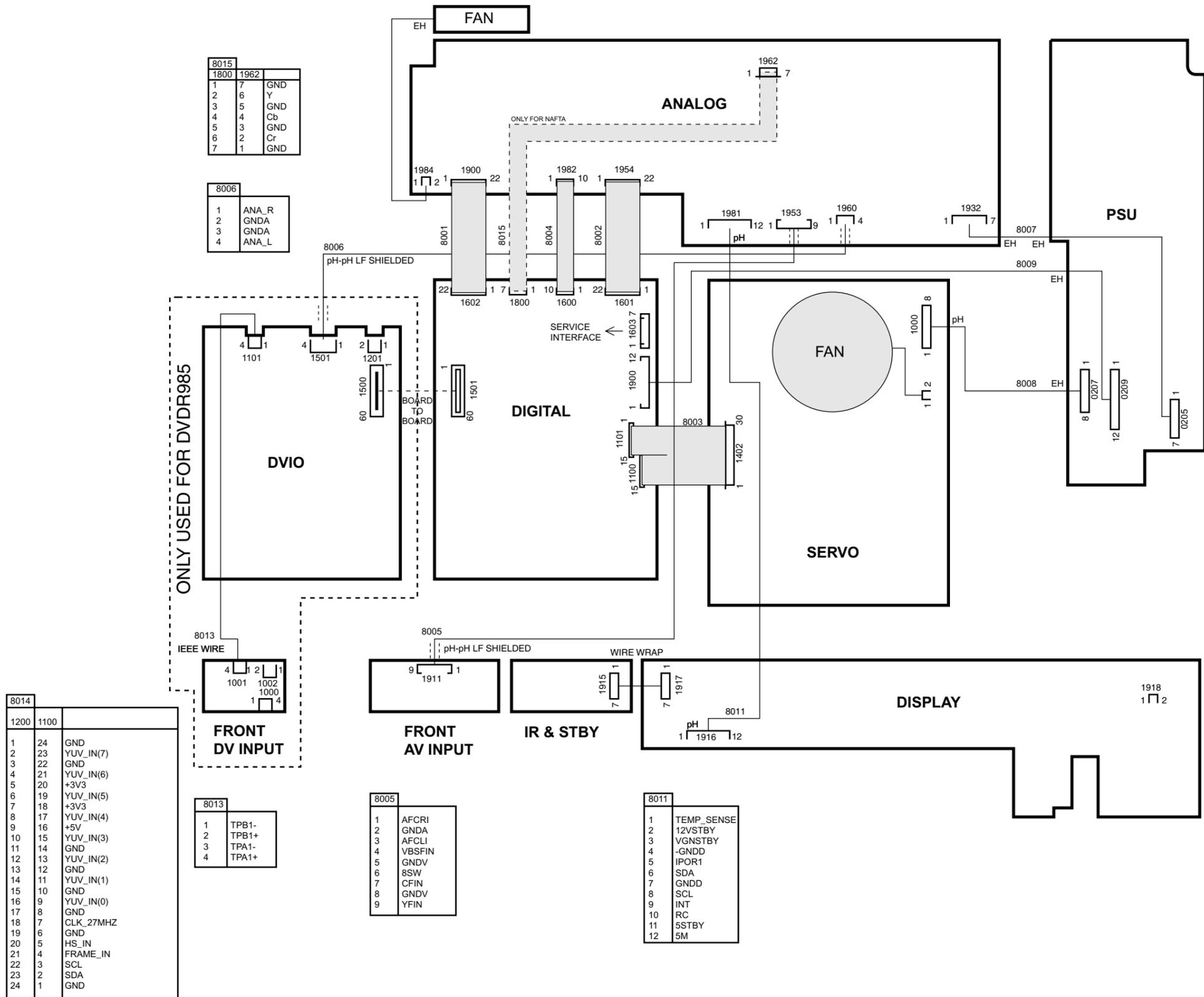
6. Block and Wiring Diagram.

Block Diagram DVDR980-985 EU



Wiring Diagram

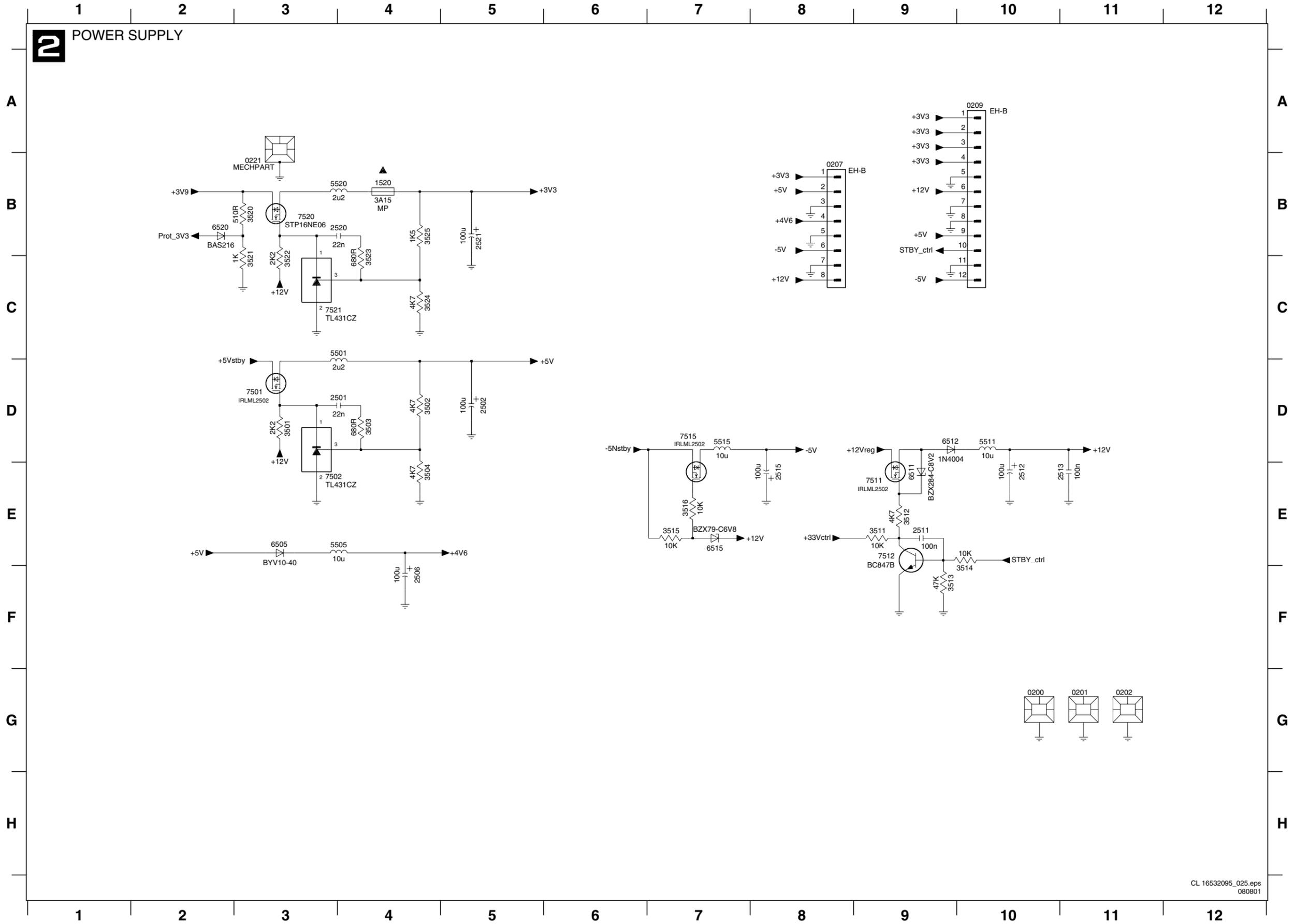
WIRING DIAGRAM



8001	
1602	1900
1	22
2	21
3	20
4	19
5	18
6	17

Power Supply

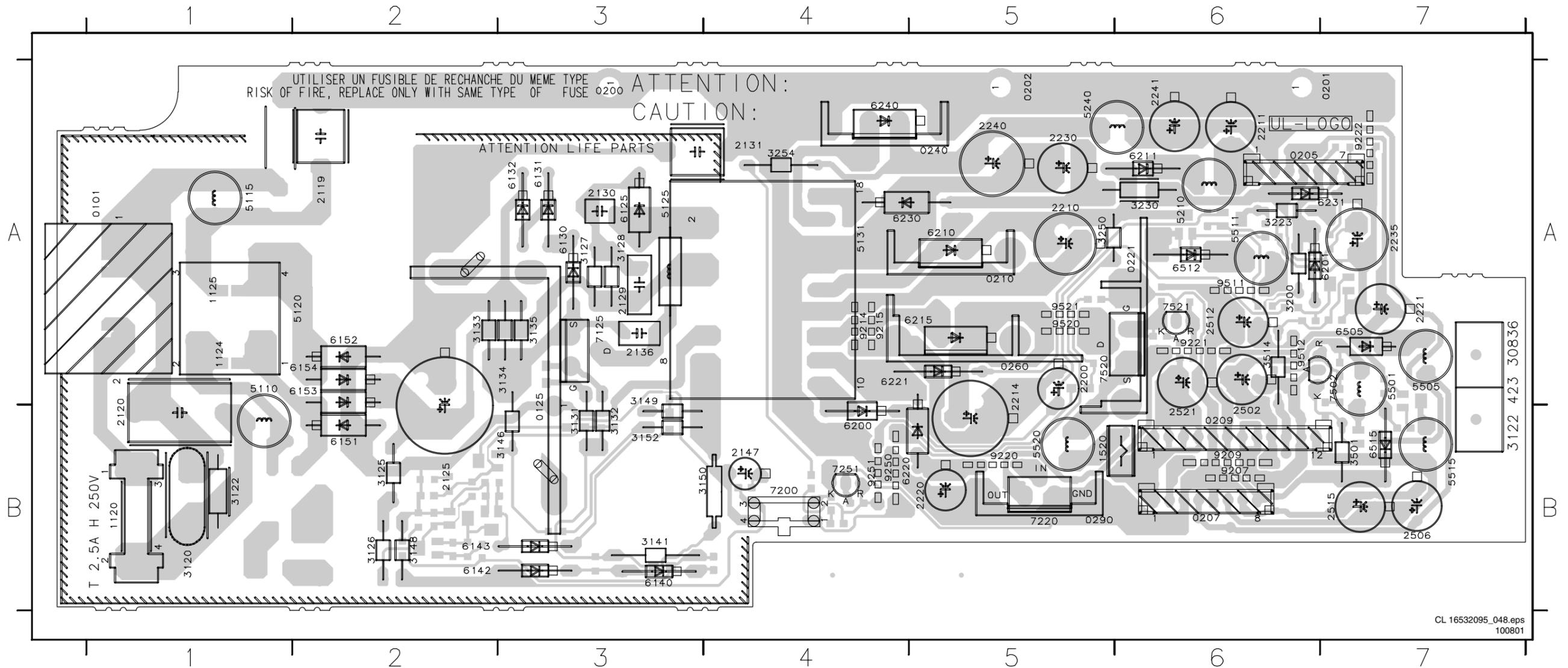
2 POWER SUPPLY



- 0200 G10
- 0201 G11
- 0202 G11
- 0207 B8
- 0209 A10
- 0221 B3
- 1520 B4
- 2501 D4
- 2502 D5
- 2506 F4
- 2511 E9
- 2512 E10
- 2513 E11
- 2515 E8
- 2520 B4
- 2521 B5
- 3501 D3
- 3502 D4
- 3503 D4
- 3504 E4
- 3511 E9
- 3512 E9
- 3513 F9
- 3514 E10
- 3515 E7
- 3516 E7
- 3520 B3
- 3521 C3
- 3522 C3
- 3523 C4
- 3524 C4
- 3525 B4
- 5501 C4
- 5505 E4
- 5511 D10
- 5515 D7
- 5520 B4
- 6505 E3
- 6511 E9
- 6512 D9
- 6515 E7
- 6520 B2
- 7501 D3
- 7502 E3
- 7511 E9
- 7512 E9
- 7515 D7
- 7520 B3
- 7521 C3

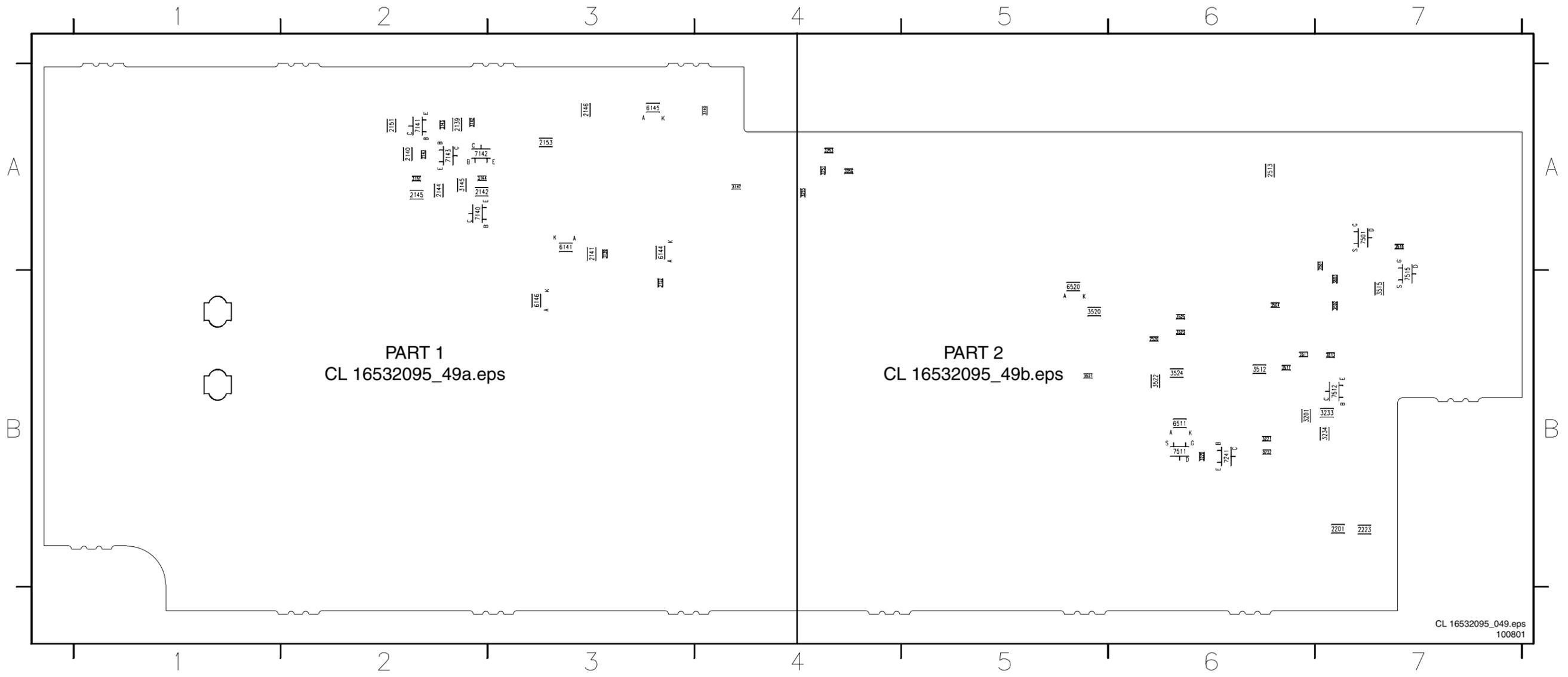
Layout Power Supply (Top View)

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0125B3	0210A5	2119A2	2131A4	2214A5	2241A6	3120B1	3129B2	3146B3	3230A6	5120A2	5505A7	6130A3	6152A2	6215A5	6512A6	7520A5	9215A4	9512A6
0200A3	0221A6	2120B1	2136A3	2215A5	2242A4	3122B1	3131B3	3148B2	3250A5	5121A1	5511A6	6131A3	6153A2	6220B4	6515B7	7521A6	9220B5	9520A5
0201A7	0240A5	2125B2	2147B4	2220B5	2502B6	3123A1	3132B3	3149A3	3254A4	5125A3	5515B7	6132A3	6154A2	6221A4	7125A3	9110B1	9221A6	9521A5
0202A5	0260A5	2126B2	2200A5	2221A7	2506B7	3125B2	3133A2	3150B3	3501B7	5131A4	5520B5	6140B3	6200B4	6230A4	7200B4	9115A1	9222A7	
0205A6	0290B5	2127B1	2210A5	2230A5	2512A6	3126B2	3134A3	3152B3	3514A6	5210A6	6125A3	6142B2	6201A7	6231A7	7220B5	9120B6	9207B6	9250B4
0207B6	1120B1	2129A3	2211A6	2235A7	2515B7	3127A3	3135A3	3200A6	5110A1	5240A5	6128B1	6143B2	6210A5	6240A4	7251B4	9209B6	9251B4	

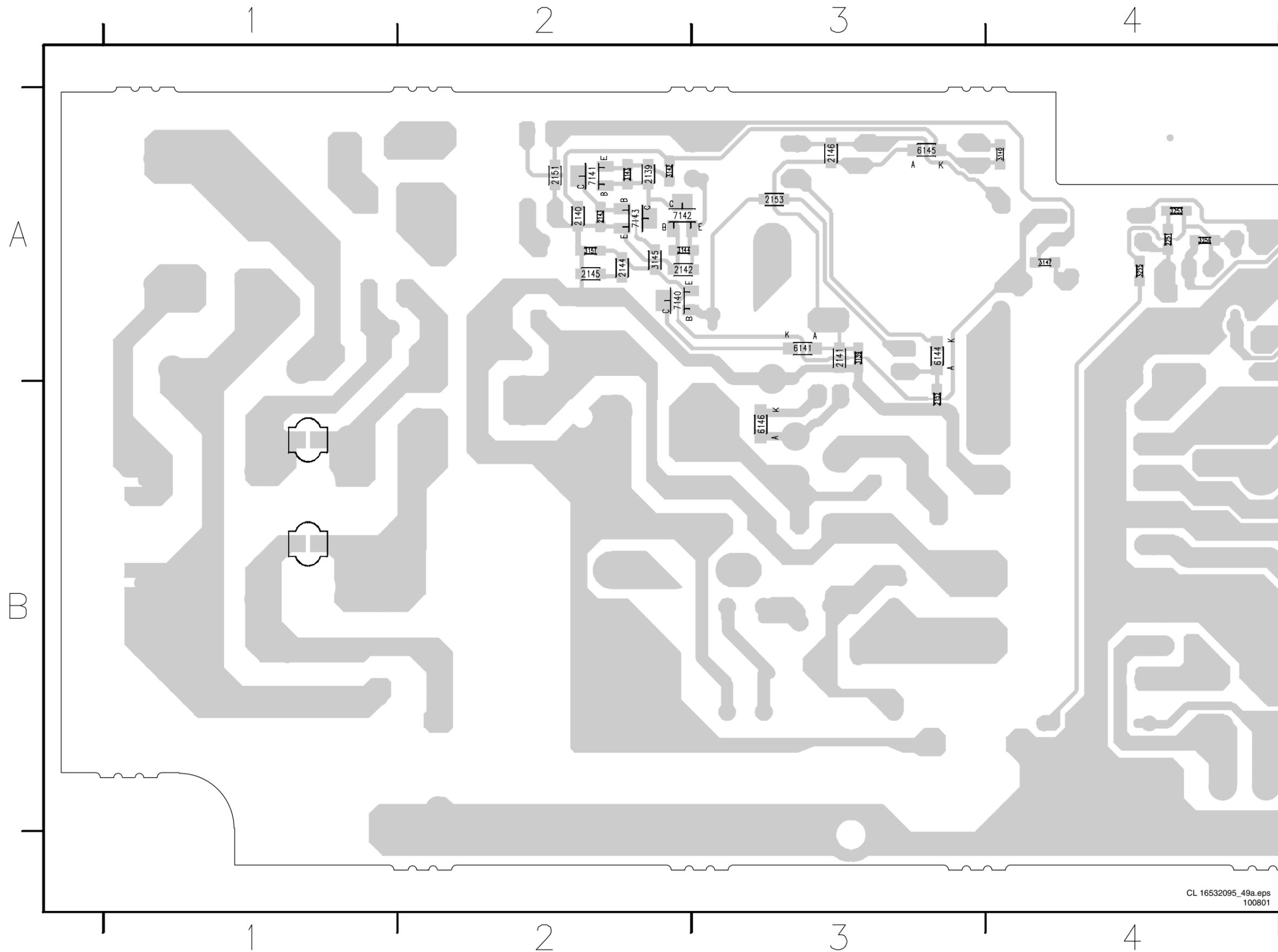


Layout Power Supply (Overview Bottom View)

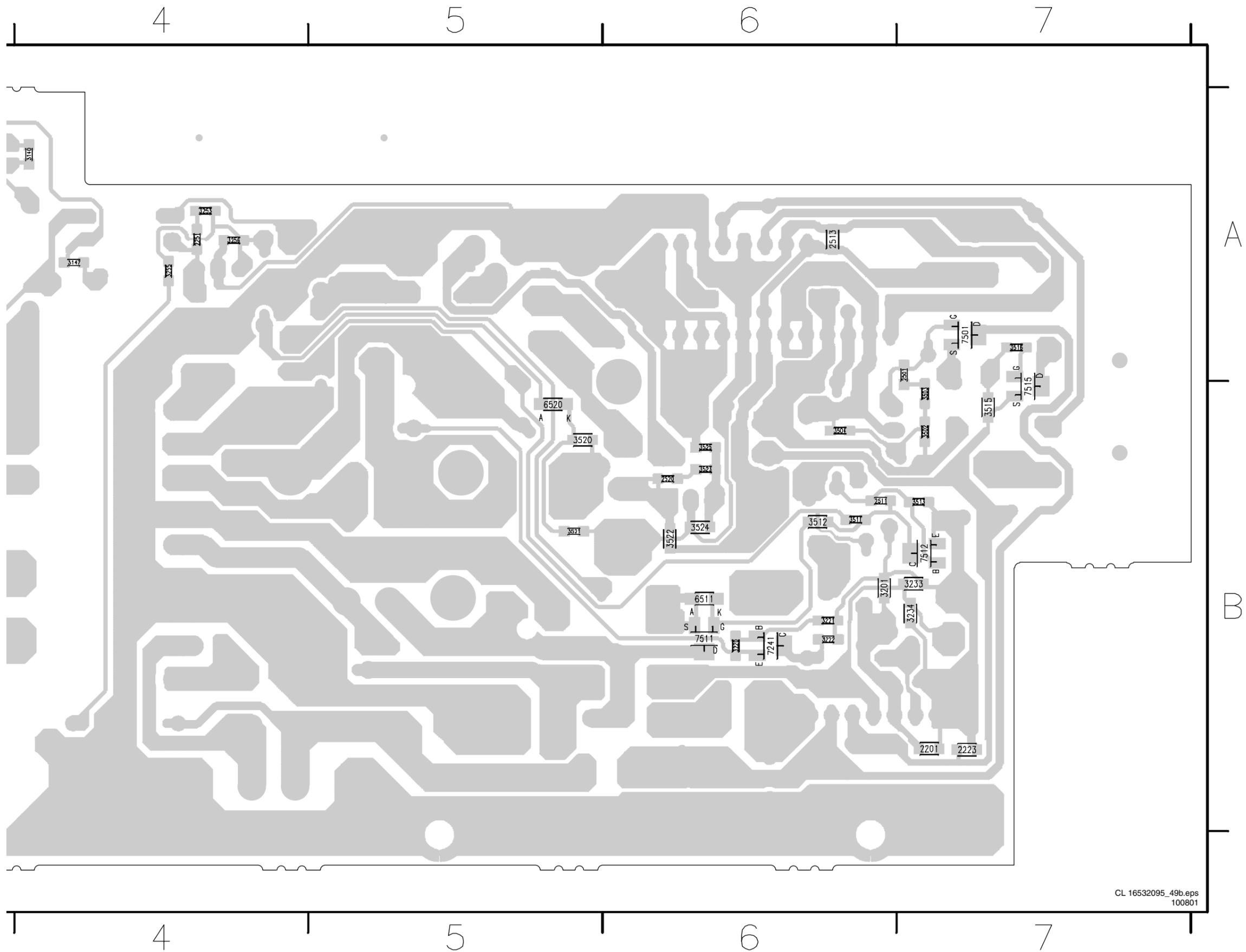
2139 A2	2143 A2	2151 A2	2222 A5	2511 B6	3140 A4	3145 A2	3220 B6	3234 B7	3502 B7	3512 B6	3520 B5	3524 B6	6145 A3	7140 A2	7241 B6	7515 B7
2140 A2	2144 A2	2152 B3	2223 B7	2513 A6	3142 A2	3147 A4	3221 B6	3253 A4	3503 B7	3513 B7	3521 B5	3525 B6	6146 B3	7141 A2	7501 A7	
2141 A3	2145 A2	2153 A3	2251 A4	2520 B6	3143 A2	3151 A2	3222 B6	3255 A4	3504 B6	3515 B7	3522 B6	6141 A3	6511 B6	7142 A2	7511 B6	
2142 A2	2146 A3	2201 B7	2501 A7	3139 A3	3144 A2	3201 B6	3233 B7	3256 A4	3511 B6	3516 A7	3523 B6	6144 A3	6520 B5	7143 A2	7512 B7	



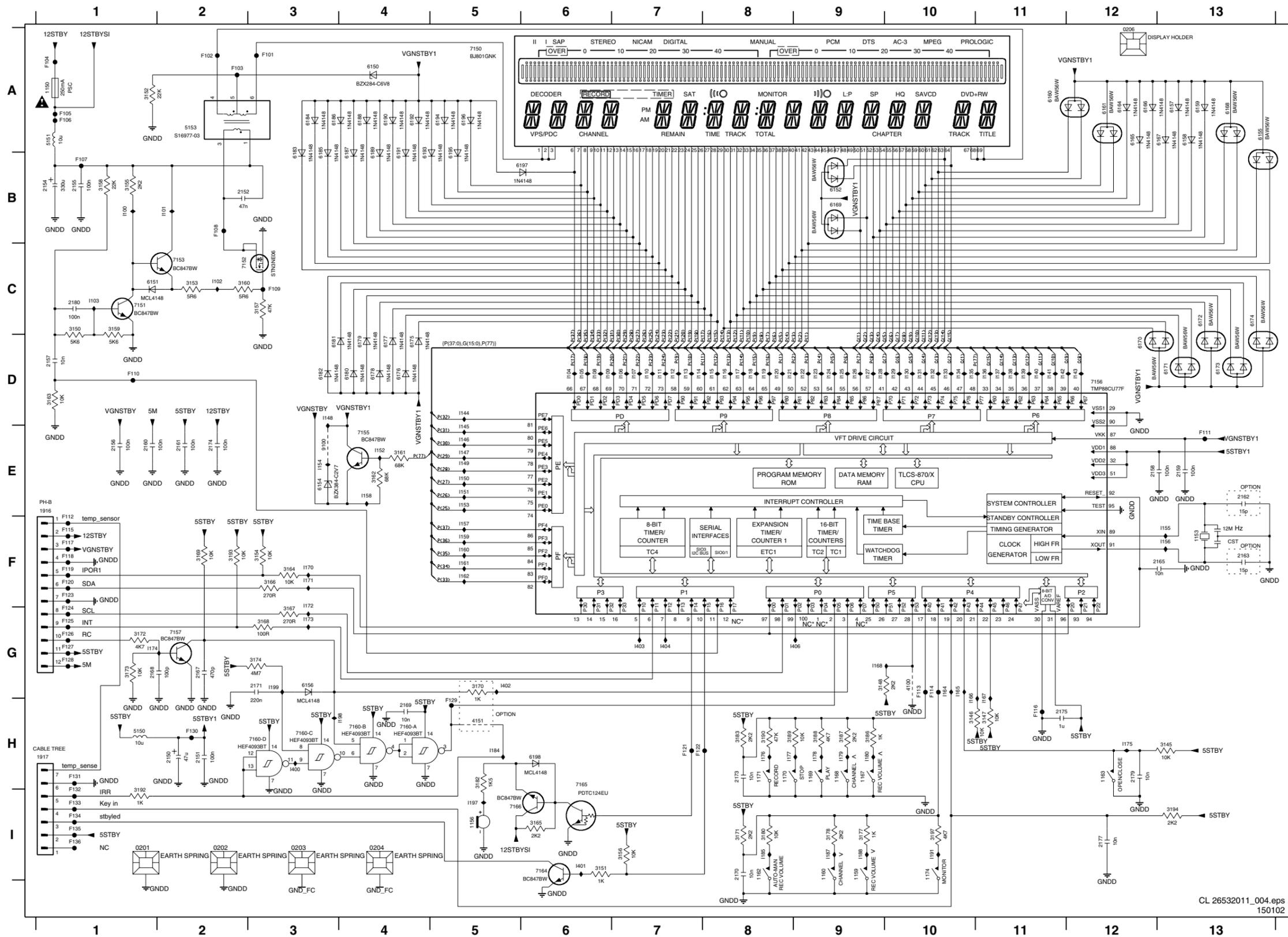
Layout Power Supply (Part 1 Bottom View)



Layout Power Supply (Part 2 Bottom View)



Display Panel

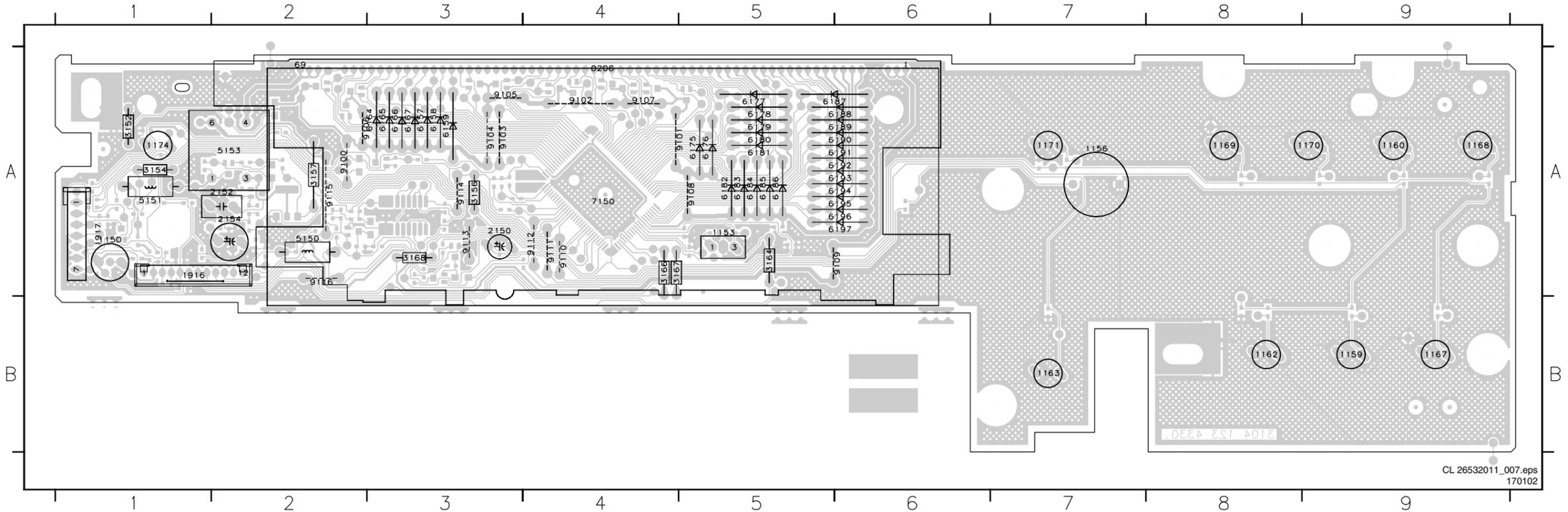


- 0201 H1
- 0202 I2
- 0203 I3
- 0204 I4
- 0206 A12
- 1150 A1
- 1153 F13
- 1155 I5
- 1159 I9
- 1160 I9
- 1162 I8
- 1163 H12
- 1167 H9
- 1168 H9
- 1169 H9
- 1170 H6
- 1171 H8
- 1174 I10
- 1916 E1
- 1917 H1
- 2150 H2
- 2151 H2
- 2152 B2
- 2154 B1
- 2155 B1
- 2156 E1
- 2157 D1
- 2158 E12
- 2159 E13
- 2160 E1
- 2161 E2
- 2162 E13
- 2163 F13
- 2165 F13
- 2167 G2
- 2168 I5
- 2169 H4
- 2170 I8
- 2171 G3
- 2173 H8
- 2174 E2
- 2175 H11
- 2177 I12
- 2179 H12
- 2180 C1
- 3145 H3
- 3146 H10
- 3147 H11
- 3148 G9
- 3150 C1
- 3151 I6
- 3152 A1
- 3153 C2
- 3154 F3
- 3154 F3
- 3155 B1
- 3156 I7
- 3157 C3
- 3158 B1
- 3159 C1
- 3160 C2
- 3161 E4
- 3162 E4
- 3163 D1
- 3164 F3
- 3165 I6
- 3166 F3
- 3167 G3
- 3168 G3
- 3169 F2
- 3170 G5
- 3171 I8
- 3172 G1
- 3173 G1
- 3174 G3
- 3177 I9
- 3178 I9
- 3180 I8
- 3182 H5
- 3183 H8
- 3186 H9
- 3187 H9
- 3188 H9
- 3189 H9
- 3190 H8
- 3192 I1
- 3193 F2
- 3194 I13
- 3197 I10
- 4100 G10
- 4151 H5
- 5150 H1
- 5151 A1
- 5152 A2
- 5153 A4
- 5151 C1
- 5152 B9
- 5154 E3
- 5155 A3
- 5156 G3
- 5157 A13
- 5158 A13
- 5159 A13
- 5160 A11
- 5161 A12
- 5164 A12
- 5165 A12
- 5166 A12
- 5167 A13
- 5168 A13
- 5169 B9
- 5170 D12
- 5171 D13
- 5172 C13
- 5173 D13
- 5174 C13
- 5175 D4
- 5176 D4
- 6177 D4
- 6178 D4
- 6179 D4
- 6180 D4
- 6181 D3
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- 6183 B3
- 6184 A3
- 6185 B3
- 6186 A3
- 6187 B4
- 6188 A4
- 6189 B4
- 6190 A4
- 6191 B4
- 6192 A4
- 6193 B4
- 6194 A5
- 6195 B5
- 6196 A5
- 6197 B6
- 6198 H6
- 6199 H6
- 6200 I3
- 6180 D4
- 6181 D3
- 6182 D3
- 6183 B3
- 6184 A3
- 6185 B3
- 6186 A3
- 6187 B4
- 6188 A4
- 6189 B4
- 6190 A4
- 6191 B4
- 6192 A4
- 6193 B4
- 6194 A5
- 6195 B5
- 6196 A5
- 6197 B6
- 6198 H6
- 6199 H6
- 6200 I3
- 7155 D12
- 7157 G2
- 7160-A H4
- 7160-B H4
- 7160-C H3
- 7160-D H3
- 7164 I6
- 7165 H6
- 7166 I6
- 9100 E3
- 9101 A3
- F102 A2
- F103 A2
- F104 A1
- F105 A1
- F106 A1
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- F108 B1
- F109 C1
- F110 D1
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- F113 G10
- F114 G10
- F115 F1
- F116 H11
- F117 F1
- F118 B1
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- F120 F1
- F121 H7
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- F123 F1
- F124 G1
- F125 G1
- F126 G1
- F127 G1
- F128 G1
- F129 H5
- F130 H2
- F131 H1
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- F134 I1
- F135 I1
- F136 I1
- F137 G3
- F138 G3
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- F142 H5
- F143 H5
- F144 H5
- F145 H5
- F146 H5
- F147 H5
- F148 H5
- F149 H5
- F150 H5
- F151 C1
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- F154 E3
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- F163 A13
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- F165 A13
- F166 A13
- F167 A13
- F168 A13
- F169 B9
- F170 D12
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- F174 C13
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- F176 D4

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150102

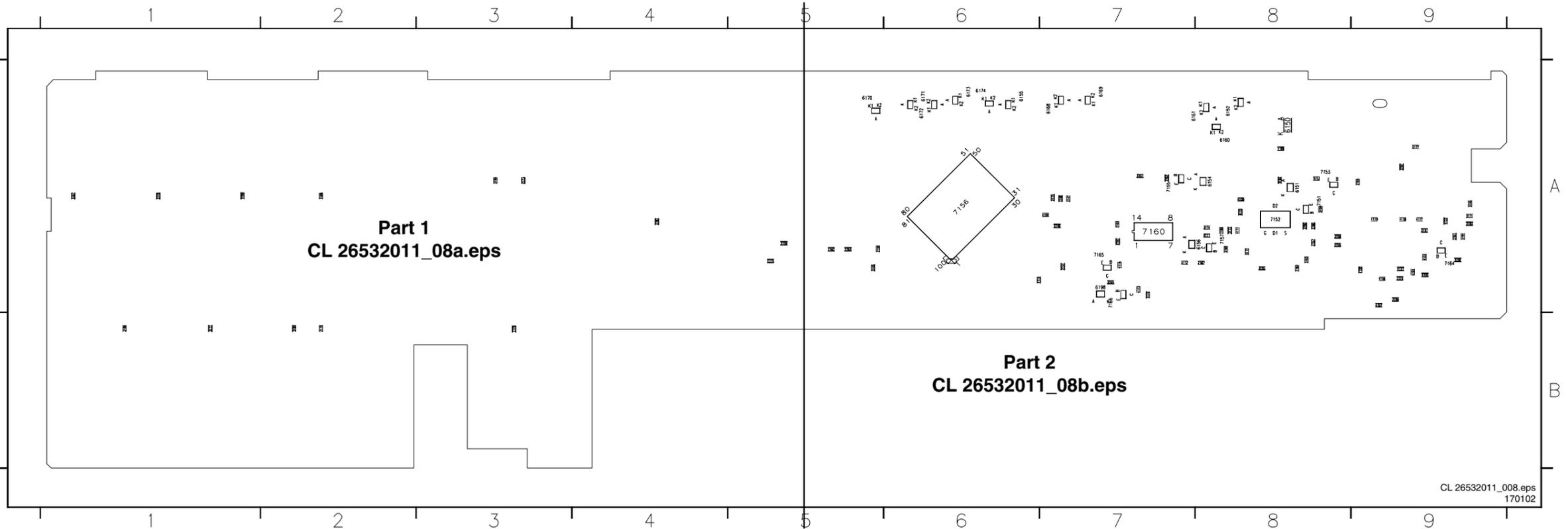
Layout Display Panel (Top View)

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1140 B2	1159 B9	1167 B9	1171 A7	1915 B1	2150 A3	3135 B1	3157 A2	3168 A3	6140 B2	6164 A3	6175 A5	6179 A5	6183 A5	6187 A5	6191 A6	6195 A6	7150 A4	9103 A3	9107 A4	9111 A4	9115 A2
1150 A1	1160 A9	1168 A9	1174 A1	1916 A1	2152 A2	3152 A1	3164 A5	5150 A2	6157 A3	6165 A3	6176 A5	6180 A5	6184 A5	6188 A6	6192 A6	6196 A6	9100 A2	9104 A3	9108 A5	9112 A4	9116 A2
1153 A5	1162 B8	1169 A8	1910 B4	1917 A1	2154 A2	3154 A1	3166 A4	5151 A1	6158 A3	6166 A3	6177 A5	6181 A5	6185 A5	6189 A6	6193 A6	6197 A6	9101 A5	9105 A3	9109 A6	9113 A3	9151 B3

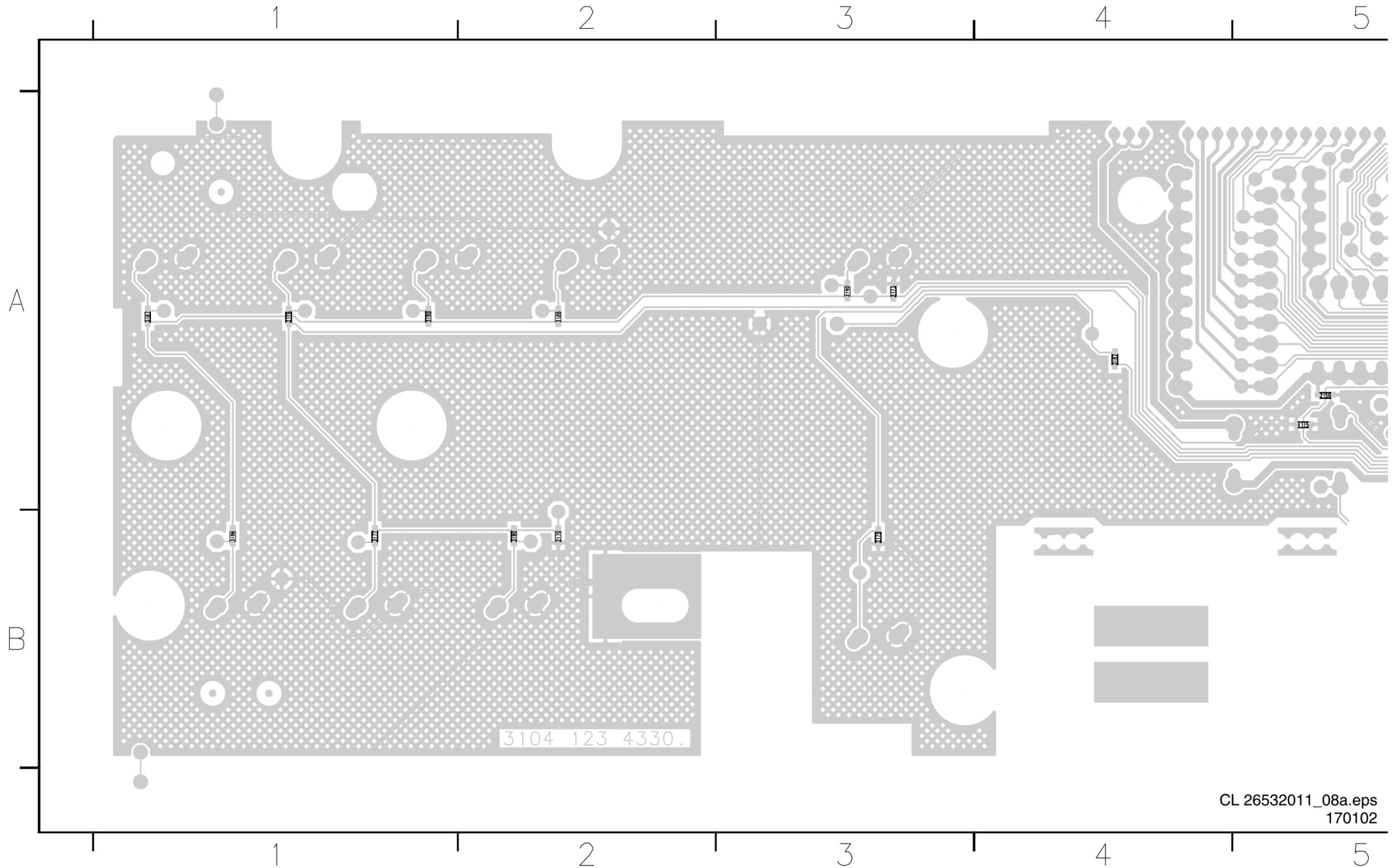


Layout Display Panel (Overview Bottom View)

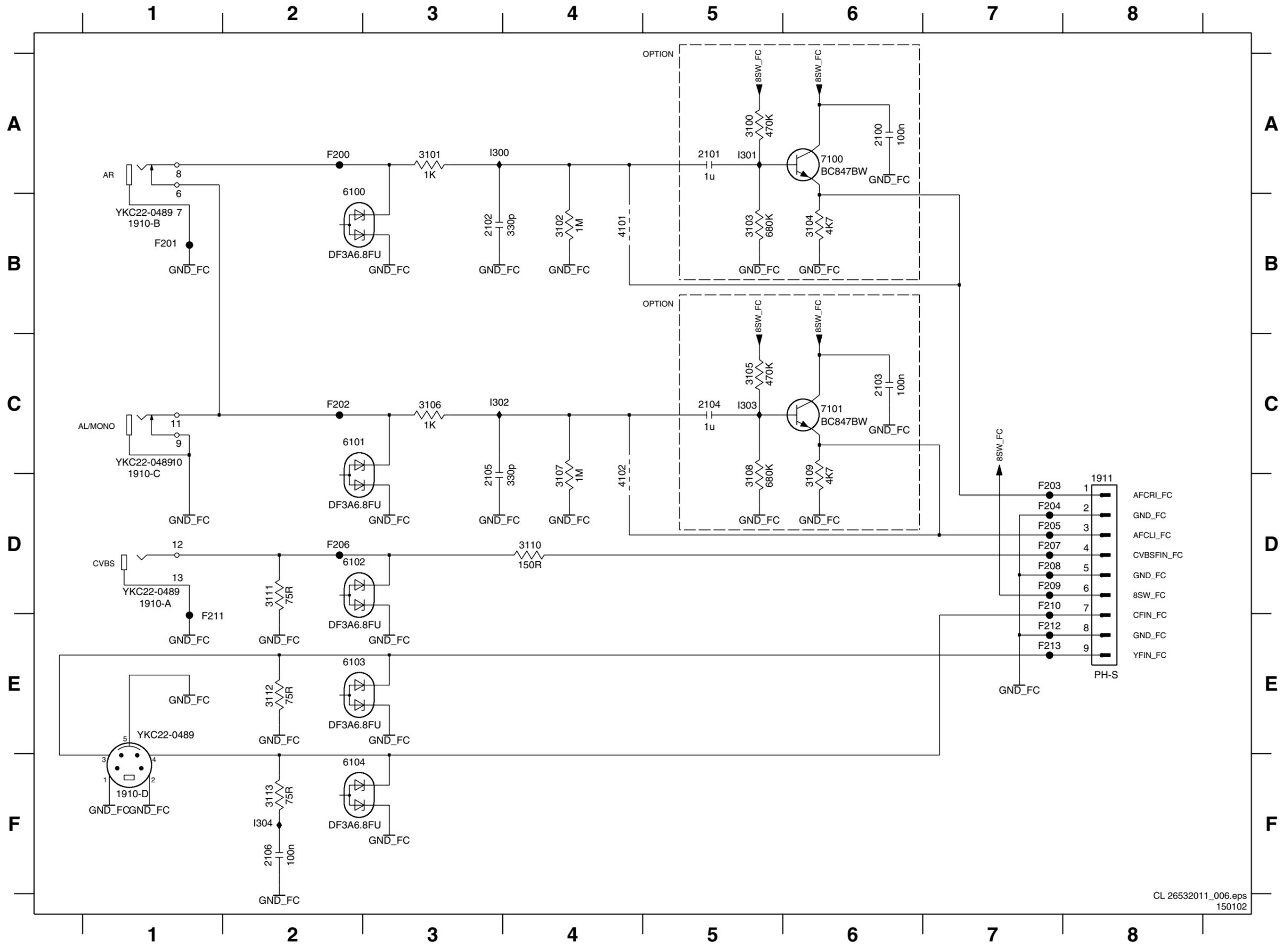
2100 B6	2151 A7	2161 A9	2170 B2	2180 A8	3106 B7	3136 B8	3143 B8	3150 A8	3161 A7	3172 A8	3183 A9	3193 A8	4103 A9	4110 A8	4117 A9	4300 B9	6151 A8	6168 A7	6198 A7	7145 B8	7160 A7
2101 B7	2155 A8	2162 A5	2171 A8	3100 B7	3107 B7	3137 B8	3144 B8	3151 A9	3162 A7	3173 A8	3186 B1	3194 A9	4104 A9	4111 A8	4118 A9	6100 B7	6152 A8	6169 A7	7100 B7	7151 A8	7164 A9
2102 B7	2156 A9	2163 A5	2173 A3	3101 B7	3108 B7	3138 B8	3145 A9	3153 A8	3163 A8	3174 A8	3187 A1	3197 A9	4105 A9	4112 A7	4119 A9	6101 B6	6154 A8	6170 A5	7101 B6	7152 A8	7165 A7
2103 B7	2157 A8	2165 A5	2174 A9	3102 B7	3109 B7	3139 B8	3146 A7	3155 A9	3165 A7	3177 B1	3188 A2	3999 B9	4106 A9	4113 A7	4120 A9	6102 B6	6155 A6	6171 A6	7141 B8	7153 A8	7166 A7
2104 B7	2158 A5	2167 A8	2175 A7	3103 B7	3111 B6	3140 B9	3147 A7	3158 A8	3169 A8	3178 A1	3189 A1	4100 A7	4107 A9	4114 A6	4121 A9	6103 B6	6156 A8	6172 A6	7142 B8	7155 A7	
2105 B7	2159 A5	2168 A8	2177 A9	3104 B7	3112 B6	3141 B8	3148 A7	3159 A8	3170 A7	3180 B2	3190 A3	4101 B7	4108 A8	4115 A5	4122 A9	6104 B6	6160 A8	6173 A6	7143 B8	7156 A6	
2106 B5	2160 A8	2169 A7	2179 B3	3105 B7	3113 B5	3142 B8	3149 B9	3160 A8	3171 A9	3182 A4	3192 A9	4102 B7	4109 A8	4116 A7	4151 A7	6150 A8	6161 A7	6174 A6	7144 B8	7157 A8	



Layout Display Panel (Part 1 Bottom View)

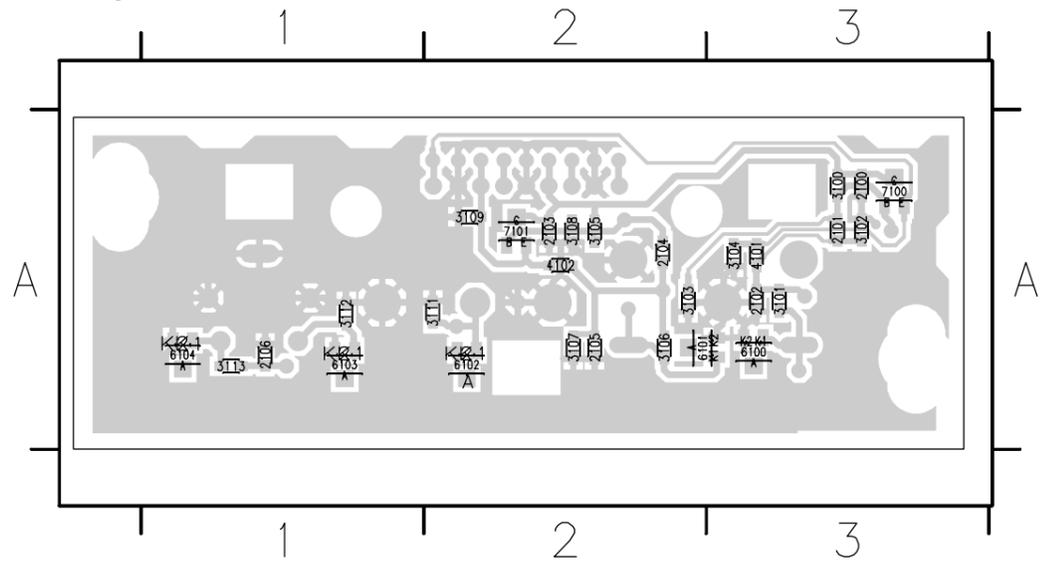


Front AV Part

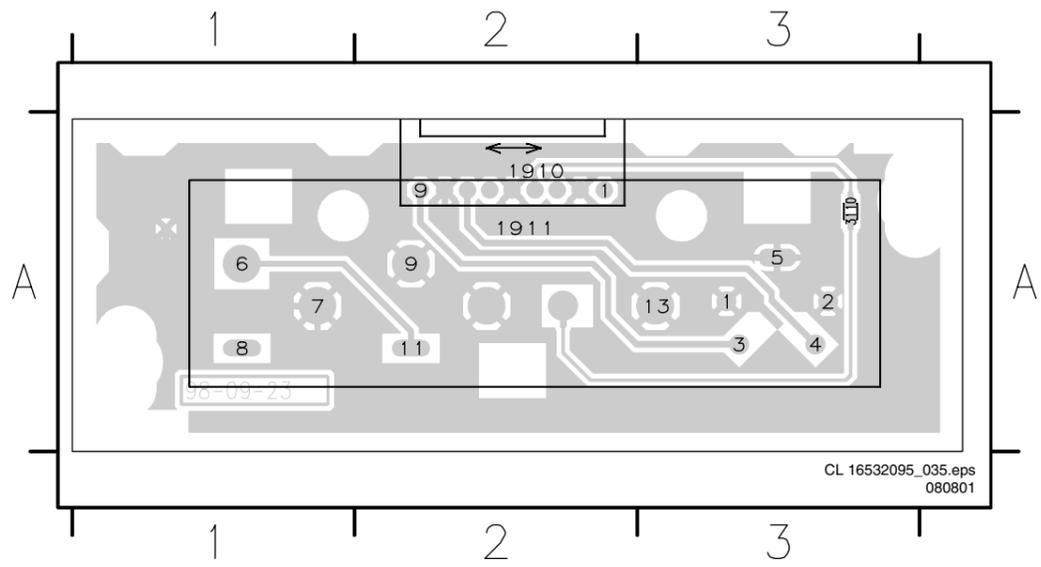


- 1910-A D1
- 1910-B B1
- 1910-C C1
- 1910-D F1
- 1911 D8
- 2100 A6
- 2101 A5
- 2102 B3
- 2103 C6
- 2104 C5
- 2105 D3
- 2106 F2
- 3100 A5
- 3101 A3
- 3102 B4
- 3103 B5
- 3104 B6
- 3105 C5
- 3106 C3
- 3107 D4
- 3108 D5
- 3109 D6
- 3110 D4
- 3111 D2
- 3112 E2
- 3113 F2
- 4101 B4
- 4102 D4
- 6100 A3
- 6101 C3
- 6102 D3
- 6103 E3
- 6104 F3
- 7100 A6
- 7101 C6
- F200 A2
- F201 B1
- F202 C2
- F203 D7
- F204 D7
- F205 D7
- F206 D2
- F207 D7
- F208 D7
- F209 D7
- F210 D7
- F211 E1
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- F213 E7
- I300 A3
- I301 A5
- I302 C3
- I303 C5
- I304 F2

Layout Front AV Part



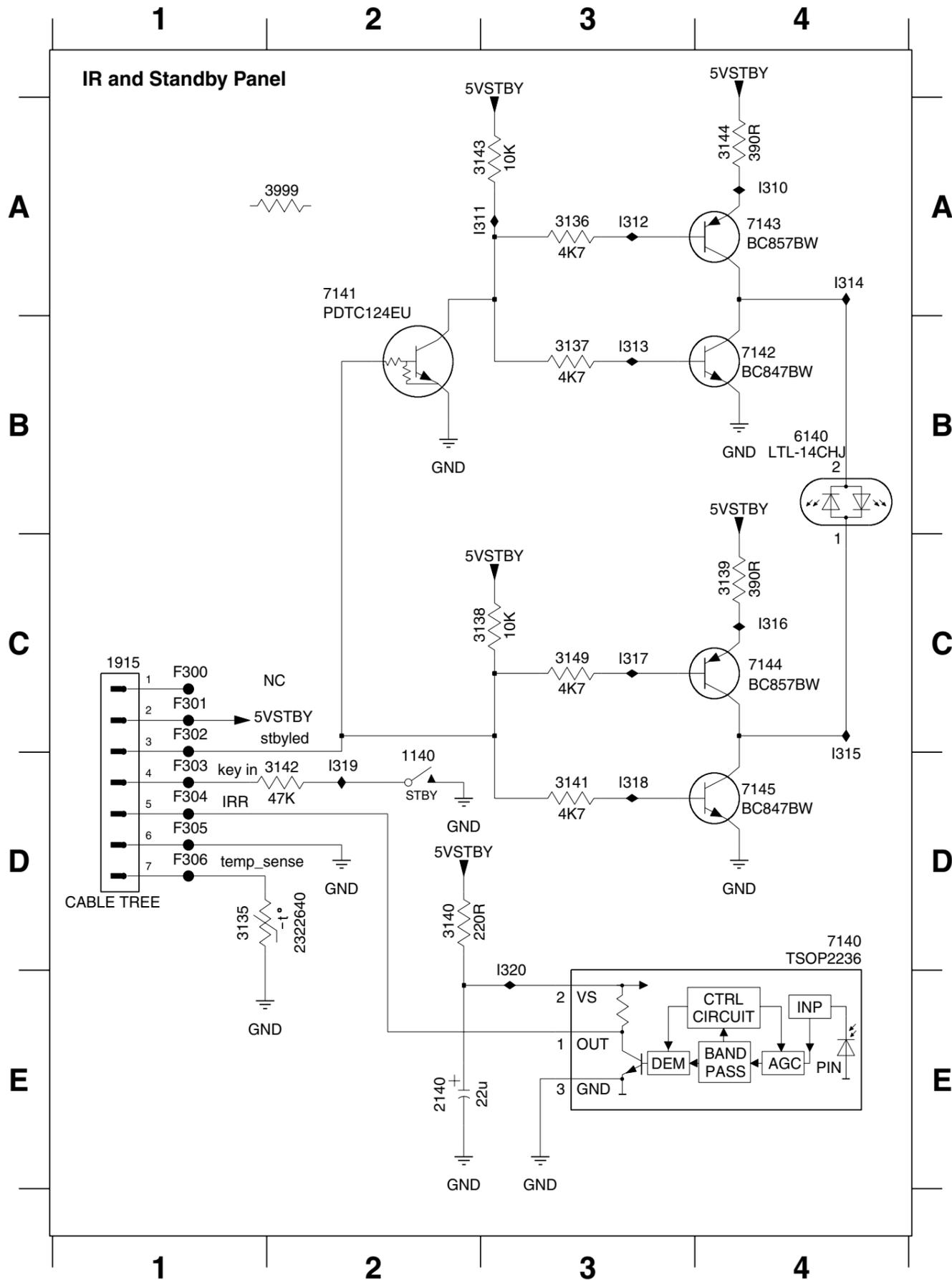
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2102	A3	4102	A2
2103	A2	6100	A3
2104	A2	6101	A3
2105	A2	6102	A2
2106	A1	6103	A1
3100	A3	6104	A1
3101	A3	7100	A3
3102	A3	7101	A2
3103	A3		
3104	A3		
3105	A2		
3106	A2		
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3108	A2		
3109	A2		
3111	A1		
3112	A1		



1910	A2
1911	A2

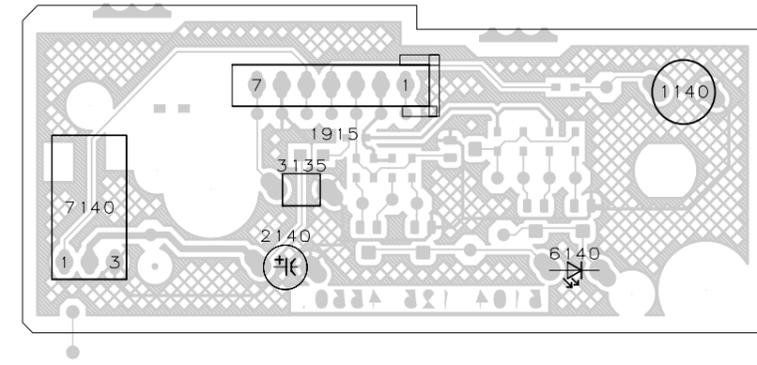
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IR and Standby Panel

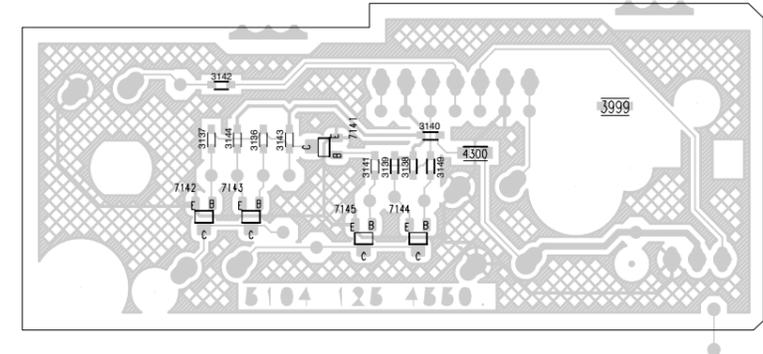


- 1140 D2
- 1915 C1
- 2140 E2
- 3135 D1
- 3136 A3
- 3137 B3
- 3138 C3
- 3139 C4
- 3140 D2
- 3141 D3
- 3142 D2
- 3143 A3
- 3144 A4
- 3149 C3
- 3999 A2
- 6140 B4
- 7140 D4
- 7141 A2
- 7142 B4
- 7143 A4
- 7144 C4
- 7145 D4
- F300 C1
- F301 C1
- F302 C1
- F303 D1
- F304 D1
- F305 D1
- F306 D1
- I310 A4
- I311 A2
- I312 A3
- I313 B3
- I314 A4
- I315 D4
- I316 C4
- I317 C3
- I318 D3
- I319 D2
- I320 D3

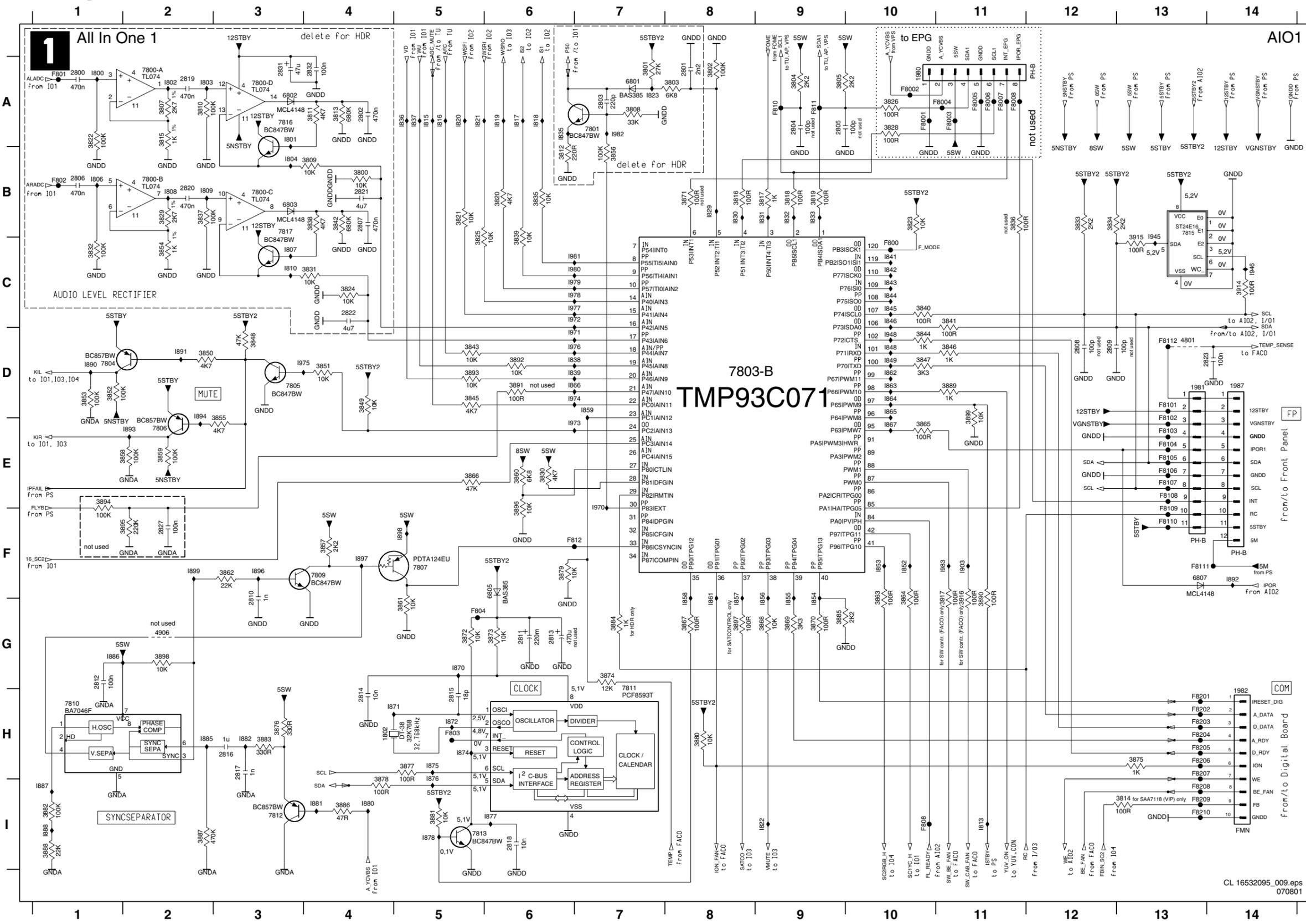
Layout IR and Standby Panel (Top View)



Layout IR and Standby Panel (Bottom View)

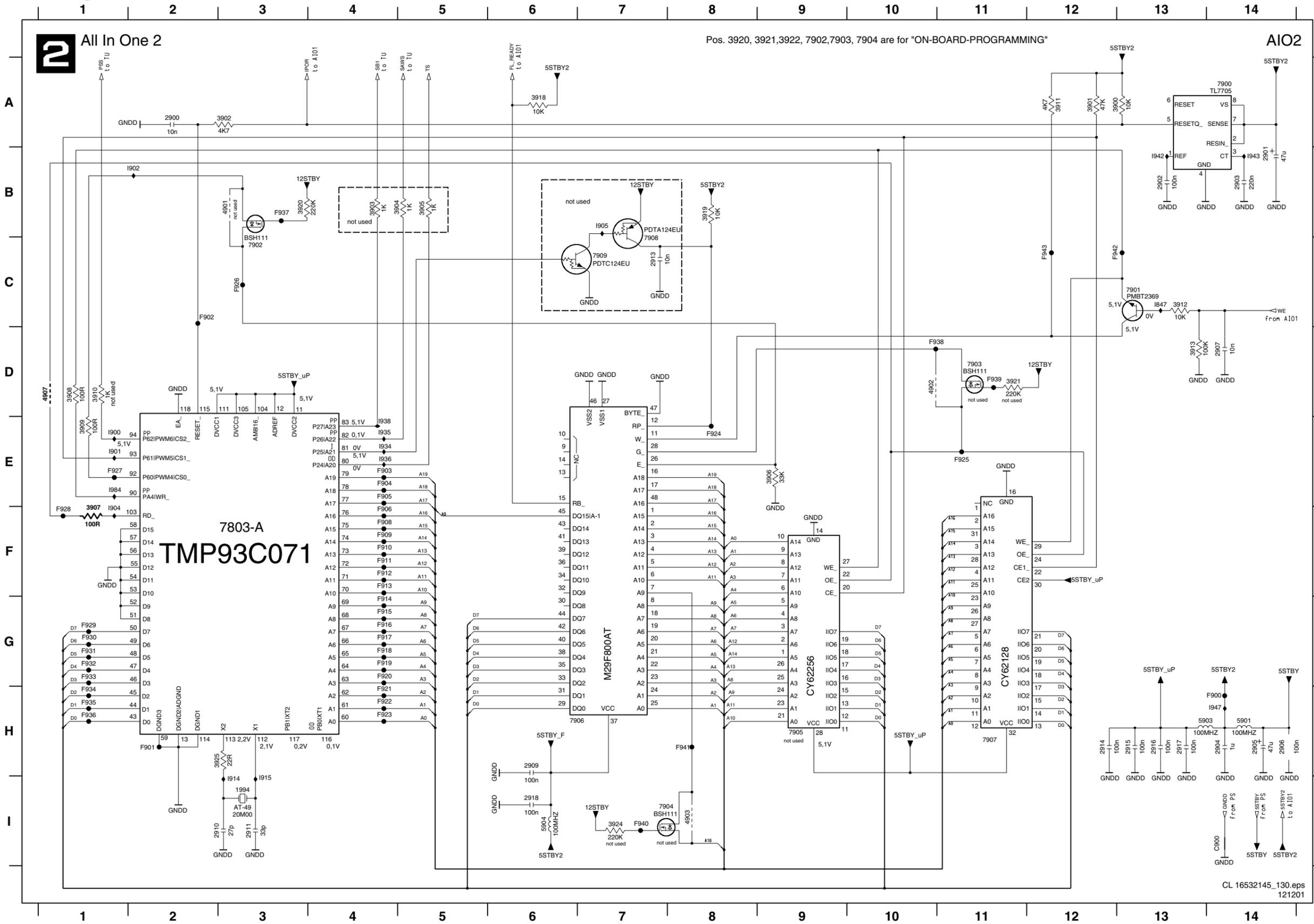


Analog Board: All in One 1



1802 H4	3916 F11	1887 I1
1804 A10	3917 F11	1888 I2
1805 D13	4801 D13	1890 D1
1806 G12	4906 G12	1891 D2
1807 D14	6801 A7	1892 F14
2800 A1	6802 A3	1893 E2
2801 A8	6803 B3	1894 D2
2802 A4	6805 F6	1895 F3
2803 A7	6807 F13	1897 F4
2804 A9	7800-A B2	1898 F5
2805 A9	7800-B A2	1899 F2
2806 B1	7800-C B3	1903 F11
2807 B4	7800-D A3	1904 B3
2808 D12	7801 A7	1946 C14
2809 D12	7803-B D8	1948 D10
2810 F3	7804 D1	1970 E7
2811 G6	7805 D3	1971 D6
2812 G1	7806 E2	1972 C6
2813 G6	7807 F5	1973 E6
2814 H4	7808 F4	1974 D6
2815 H5	7810 H1	1975 D3
2816 H3	7811 H7	1976 D6
2817 H3	7812 I3	1977 C6
2818 I6	7813 I5	1978 C6
2819 A2	7815 B13	1979 C6
2820 B2	7820 B2	1980 C6
2821 B4	7817 B3	1981 C6
2822 C4	F800 C10	1982 A7
2823 D14	F8001 A10	1983 F11
2827 F3	F8002 A10	
2828 A1	F8003 A11	
2832 A4	F8004 A11	
3800 B4	F8005 A11	
3801 A7	F8006 A11	
3802 A8	F8007 A11	
3803 A8	F8008 A11	
3804 A9	F801 A1	
3805 A9	F802 B1	
3807 A2	F803 H5	
3808 A7	F804 G5	
3809 B4	F808 I10	
3810 A2	F810 A9	
3811 A4	F8101 D13	
3812 B6	F8102 E13	
3813 A4	F8103 E13	
3814 H13	F8104 E13	
3815 A2	F8105 E13	
3816 A2	F8106 E13	
3817 B9	F8107 E13	
3818 B9	F8108 E13	
3819 B9	F8109 F13	
3820 B6	F811 A9	
3821 B5	F8110 F13	
3822 A10	F8111 F13	
3823 B10	F8112 D13	
3824 C4	F812 F6	
3825 C5	F8201 H13	
3826 A10	F8202 H13	
3828 A10	F8203 H13	
3829 B2	F8204 H13	
3830 E6	F8205 H13	
3831 C4	F8206 H13	
3832 C1	F8207 H13	
3833 B12	F8208 H13	
3834 B12	F8209 H13	
3835 B6	F8210 H13	
3836 B11	I800 A1	
3837 B2	I801 A3	
3838 B4	I802 A2	
3839 C6	I803 A2	
3840 C10	I804 B3	
3841 C11	I806 B1	
3842 B4	I807 C3	
3843 D10	I808 B2	
3844 D10	I809 B2	
3845 D5	I810 C3	
3846 D11	I813 I11	
3847 D10	I815 A5	
3848 D3	I816 A5	
3849 D4	I817 A6	
3850 D2	I818 A6	
3851 D4	I819 A6	
3852 D1	I820 A5	
3853 D1	I821 A5	
3854 C2	I822 I9	
3855 E3	I823 A7	
3856 E7	I829 B8	
3857 F4	I830 B8	
3858 E1	I831 B9	
3859 E2	I832 B9	
3860 E6	I833 B9	
3861 G5	I835 A6	
3862 F3	I836 A5	
3863 F10	I837 A5	
3864 F10	I838 D6	
3865 E10	I839 D6	
3866 E5	I841 C10	
3867 G8	I842 C10	
3868 G9	I843 C10	
3869 G9	I844 C10	
3870 G9	I845 C10	
3871 B8	I846 C10	
3872 G5	I848 D10	
3873 G6	I849 D10	
3874 G7	I852 F10	
3875 H13	I853 F10	
3876 H3	I854 G9	
3877 H5	I855 G9	
3878 I4	I856 G9	
3879 F6	I857 G8	
3880 H8	I858 G8	
3881 I5	I859 D7	
3882 I11	I861 G8	
3883 H7	I862 D10	
3884 G3	I863 D10	
3885 G9	I864 D10	
3886 I4	I865 D10	
3887 I2	I866 D6	
3888 I1	I867 E10	
3889 D11	I870 G5	
3890 G11	I871 H4	
3891 D6	I872 H5	
3892 D6	I874 H5	
3893 D5	I875 H5	
3894 E1	I876 H5	
3895 F2	I877 I6	
3896 F6	I878 I5	
3897 G8	I880 I4	
3898 G2	I881 I4	
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3915 C13	I886 G1	

Analog Board: All in One 2



2 All In One 2

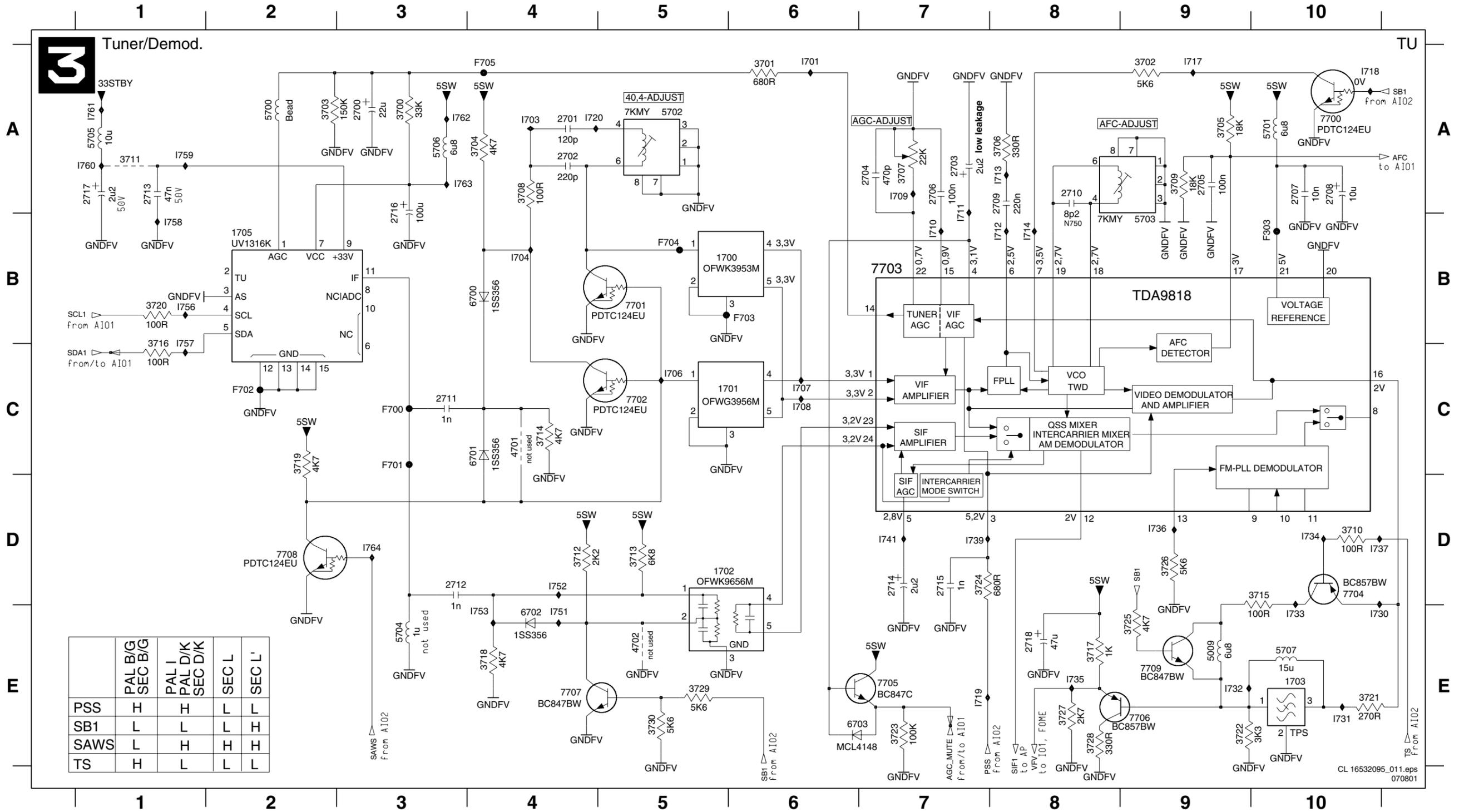
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AIO2

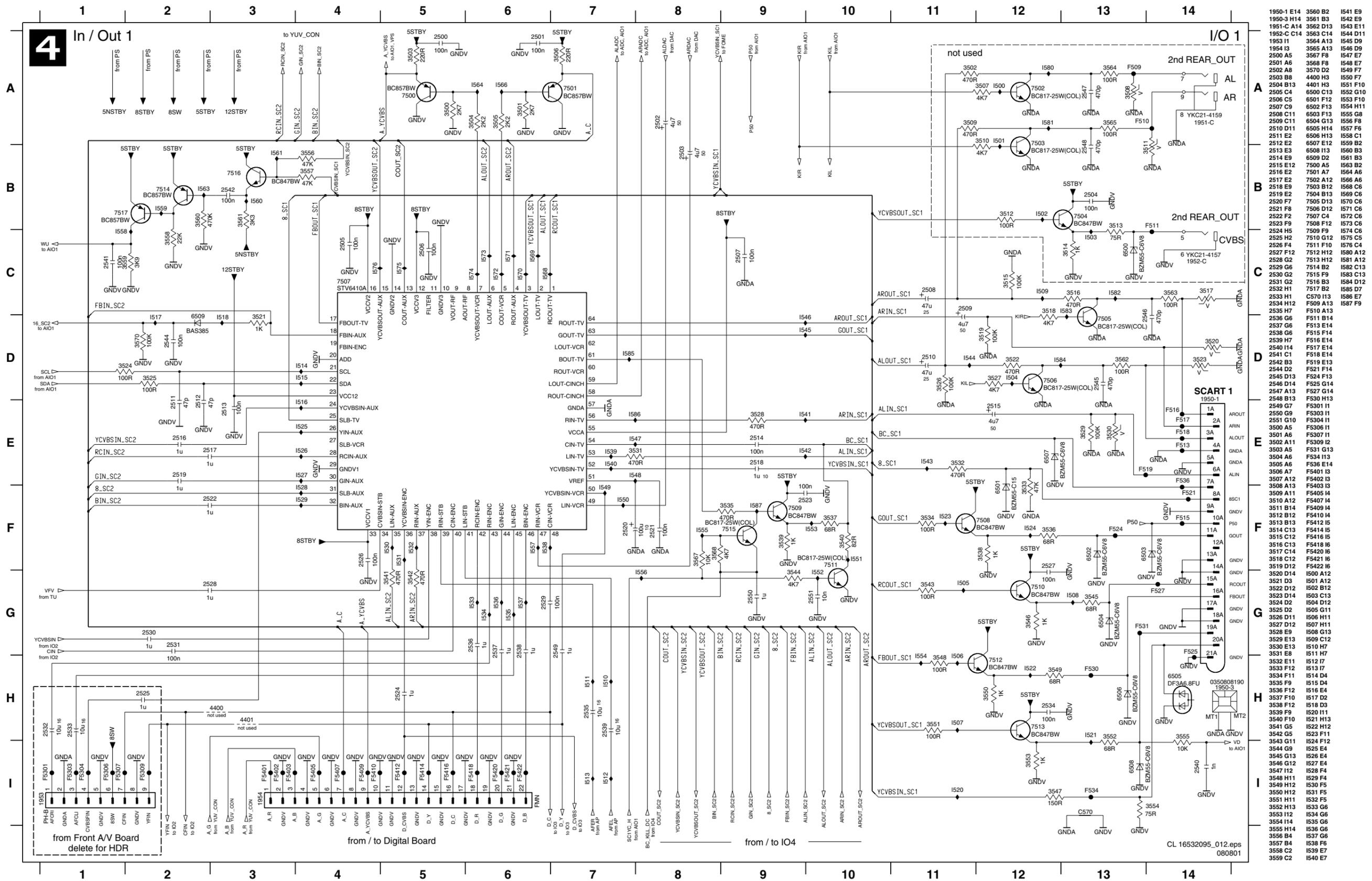
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- 2902 B13
- 2913 C7
- 2904 H14
- 2905 H14
- 2906 H14
- 2907 D14
- 2909 H6
- 2910 I3
- 2911 I3
- 2912 H12
- 2915 H13
- 2916 H13
- 2917 H13
- 2918 I6
- 3900 A13
- 3902 A3
- 3903 B4
- 3904 B5
- 3905 B5
- 3906 E9
- 3907 E1
- 3908 D11
- 3909 E1
- 3910 D1
- 3911 A12
- 3912 C13
- 3913 D13
- 3918 A6
- 3919 B8
- 3920 B3
- 3921 D11
- 3924 I7
- 3925 H3
- 4901 B3
- 4902 D10
- 4903 I8
- 4907 D1
- 5901 H14
- 5903 H13
- 5904 I8
- 7803-A F3
- 7900 A14
- 7901 C13
- 7902 C3
- 7903 D11
- 7904 I7
- 7905 H9
- 7906 H7
- 7907 H11
- 7908 B7
- 7909 C7
- C900 I14
- F900 H14
- F901 H12
- F902 C2
- F903 E4
- F904 E4
- F905 E4
- F906 F4
- F907 F4
- F908 F4
- F909 F4
- F910 F4
- F911 F4
- F912 F4
- F913 F4
- F914 G4
- F915 G4
- F916 G4
- F917 G4
- F918 G4
- F919 G4
- F920 G4
- F921 H4
- F922 H4
- F923 H4
- F924 E8
- F925 E11
- F926 C3
- F927 E1
- F928 F1
- F929 G1
- F930 G1
- F931 G1
- F932 G1
- F933 G1
- F934 H1
- F935 H1
- F936 H1
- F937 B3
- F938 D10
- F939 D11
- F940 I7
- F941 H8
- F942 C13
- F943 C12
- I847 C13
- I900 E1
- I901 E1
- I902 B2
- I904 F1
- I905 B7
- I914 I3
- I915 I3
- I934 E4
- I935 E4
- I936 E4
- I938 E4
- I942 B13
- I943 B14
- I947 H14
- I884 E1

Analog Board: Tuner / Demodulator

- | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------|---------|----------|---------|---------|---------|----------|----------|---------|----------|---------|----------|---------|----------|----------|---------|----------|---------|---------|---------|----------|----------|----------|---------|---------|
| 1700 B5 | 2700 A3 | 2705 A9 | 2710 A8 | 2715 D7 | 3701 A6 | 3706 A8 | 3711 A1 | 3716 C1 | 3721 E10 | 3726 D9 | 4701 C4 | 5702 A5 | 5707 E10 | 7700 A10 | 7705 E7 | F303 B10 | F704 B5 | I706 C5 | I711 A7 | I718 A10 | I732 E9 | I737 D10 | I753 E4 | I760 A1 |
| 1701 C5 | 2701 A4 | 2706 A7 | 2711 C3 | 2716 A3 | 3702 A9 | 3707 A7 | 3712 D4 | 3717 E8 | 3722 E9 | 3727 E8 | 4702 E5 | 5703 B9 | 6700 B4 | 7701 B5 | 7706 E9 | F700 C3 | F705 A4 | I707 C6 | I712 B8 | I719 E7 | I733 E10 | I739 D7 | I756 B1 | I761 A1 |
| 1702 D5 | 2702 A4 | 2707 A10 | 2712 D3 | 2717 A1 | 3703 A2 | 3708 A4 | 3713 D5 | 3718 E4 | 3723 E7 | 3728 E8 | 5009 E9 | 5704 E3 | 6701 C4 | 7702 C5 | 7707 E4 | F701 C3 | I701 A6 | I708 C6 | I713 A8 | I720 A4 | I734 D10 | I741 D7 | I757 B1 | I762 A3 |
| 1703 E10 | 2703 A7 | 2708 A10 | 2713 A1 | 2718 E8 | 3704 A4 | 3709 A9 | 3714 C4 | 3719 C2 | 3724 D7 | 3729 E5 | 5700 A2 | 5705 A1 | 6702 E4 | 7703 B7 | 7708 D2 | F702 C2 | I703 A4 | I709 A7 | I714 B8 | I721 E10 | I735 E8 | I742 E4 | I758 B1 | I763 A3 |
| 1705 B2 | 2704 A7 | 2709 A8 | 2714 D7 | 3700 A3 | 3705 A9 | 3710 D10 | 3715 D10 | 3720 B1 | 3725 E9 | 3730 E5 | 5701 A10 | 5706 A3 | 6703 E6 | 7704 D10 | 7709 E9 | F703 B6 | I704 B4 | I710 B7 | I717 A9 | I731 E10 | I736 D9 | I752 D4 | I759 A1 | I764 D3 |

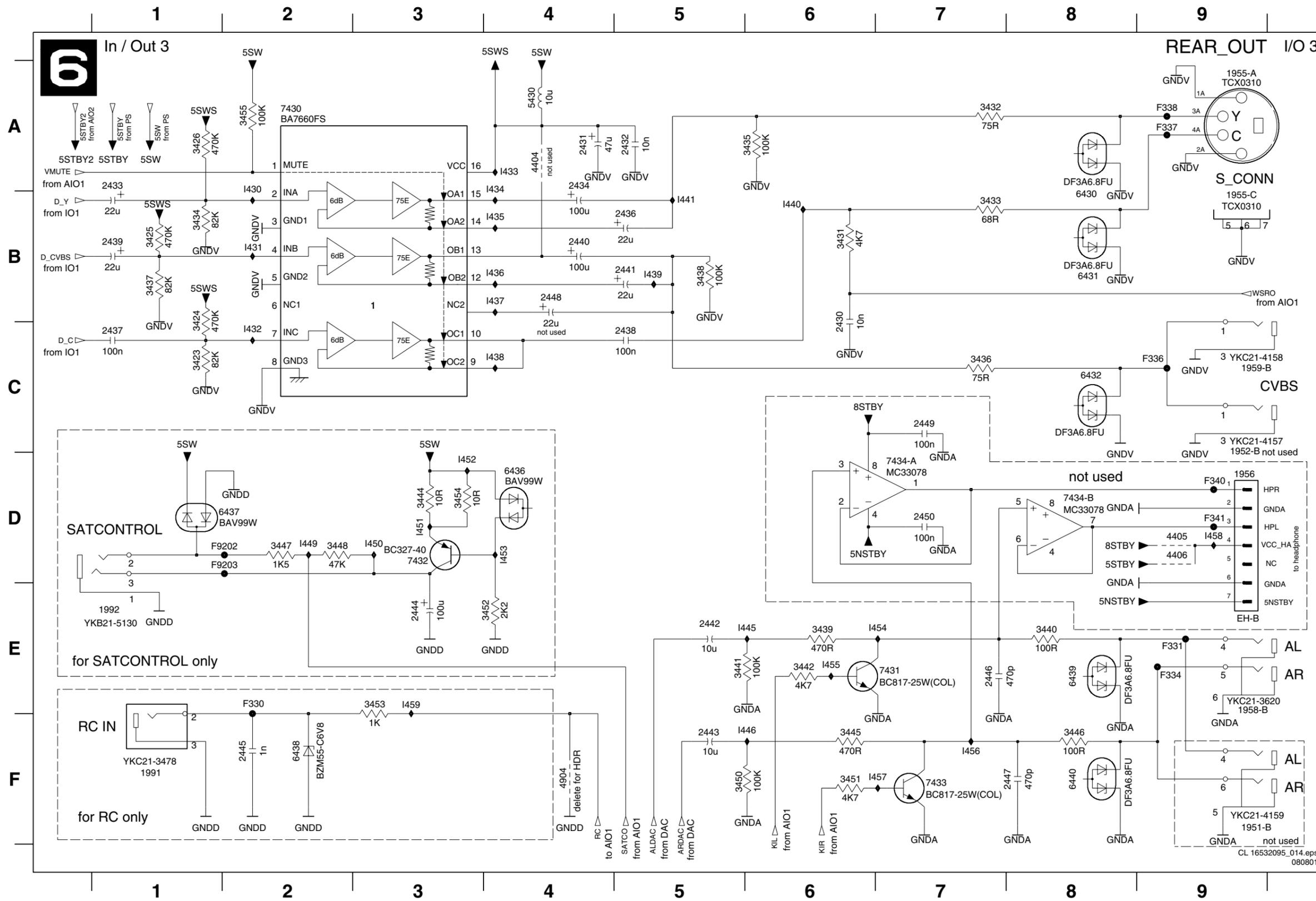


Analog Board: In / Out 1



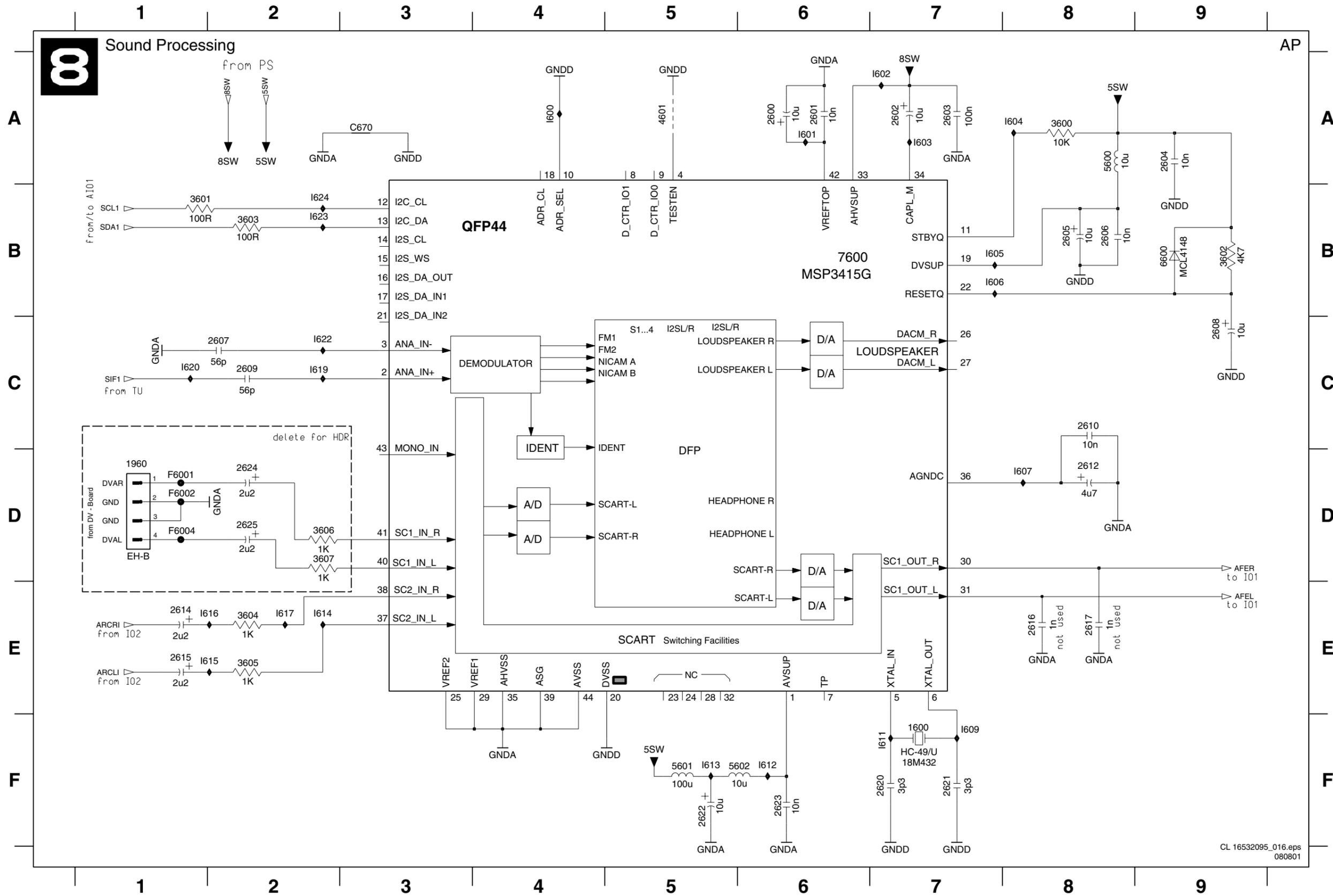
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1951-C A14	3562 D13	1543 E11
1952-C C14	3563 C14	1544 D11
1953 I1	3564 A13	1545 D9
1954 I3	3565 A13	1546 D9
2500 A5	3567 F8	1547 E7
2501 A6	3568 F8	1548 E7
2502 A8	3570 D2	1549 F7
2503 B9	4400 H3	1550 F7
2504 B13	4401 H3	1551 F10
2505 C4	6500 C13	1552 G10
2506 C5	6501 F12	1553 F10
2507 C9	6502 F13	1554 H11
2508 C11	6503 F13	1555 G8
2509 C11	6504 G13	1556 F8
2510 D11	6505 H14	1557 F6
2511 E2	6506 H13	1558 C1
2512 E2	6507 E12	1559 B2
2513 E3	6508 H13	1560 B3
2514 E9	6509 D2	1561 B3
2515 E12	7500 A5	1563 B2
2516 E2	7501 A7	1564 A6
2517 E2	7502 A12	1566 A6
2518 E9	7503 B12	1568 C6
2519 E2	7504 B13	1569 A12
2520 F7	7505 D13	1570 C6
2521 F8	7506 D12	1571 C6
2522 F2	7507 C4	1572 C6
2523 F9	7508 F12	1573 C6
2524 H5	7509 F9	1574 C6
2525 H2	7510 G12	1575 C5
2526 F4	7511 F10	1576 C4
2527 H2	7512 H12	1580 A12
2528 G2	7513 H12	1581 A12
2529 G6	7514 B2	1582 C13
2530 G2	7515 F9	1583 C13
2531 G2	7516 B3	1584 D12
2532 H1	7517 B2	1585 D7
2533 H1	C570 I13	1586 E7
2534 H12	F509 A13	1587 F9
2535 H7	F510 A13	
2536 G6	F511 B14	
2537 G6	F513 A14	
2538 G6	F515 A14	
2539 H7	F516 E14	
2540 I14	F517 E14	
2541 C1	F518 E14	
2542 B3	F519 E13	
2543 D2	F520 A13	
2544 D13	F524 F13	
2545 D13	F525 G14	
2546 D14	F527 G14	
2547 A13	F530 H13	
2548 B13	F530 H13	
2549 G7	F530 I1	
2550 G9	F530 I1	
2551 G10	F530 I1	
2552 A5	F530 I1	
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2556 A6	F536 E14	
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2688 A13	F540 I13	
2689 A11	F540 I13	
2690 A12	F540 I13	
2691 A13	F540 I13	
2692 A11	F540 I13	
2693 A12	F540 I13	
2694 A13	F540 I13	
2695 A11	F540 I13	
2696 A12	F540 I13	
2697 A13	F540 I13	
2698 A11	F540 I13	
2699 A12	F540 I13	
2700 A13	F540 I13	

Analog Board: In / Out 3



- 1951-B F9 F9203 D2
- 1952-B C9 I430 A2
- 1955-A A9 I431 B2
- 1955-C B9 I432 C2
- 1956 D9 I433 A4
- 1958-B E9 I434 A4
- 1959-B C9 I435 B4
- 1991 F1 I436 B4
- 1992 E1 I437 B4
- 2430 B6 I438 C4
- 2431 A4 I439 B5
- 2432 A5 I440 B6
- 2433 A1 I441 B5
- 2434 A4 I445 E6
- 2436 B5 I446 F6
- 2437 C1 I449 D2
- 2438 C5 I450 D3
- 2439 B1 I451 D3
- 2440 B4 I452 D3
- 2441 B5 I453 D4
- 2442 E5 I454 E7
- 2443 F5 I455 E6
- 2444 E3 I456 F7
- 2445 F2 I457 F7
- 2446 E7 I458 D9
- 2447 F8 I459 E3
- 2448 B4
- 2449 C7
- 2450 D7
- 3423 C1
- 3424 B1
- 3425 B1
- 3426 A1
- 3431 B6
- 3432 A7
- 3433 B7
- 3434 B1
- 3435 A6
- 3436 C7
- 3437 B1
- 3438 B5
- 3439 E6
- 3440 E8
- 3441 E5
- 3442 E6
- 3444 D3
- 3445 F6
- 3446 F8
- 3447 D2
- 3448 D2
- 3450 F5
- 3451 F6
- 3452 E4
- 3453 E3
- 3454 D3
- 3455 A2
- 4404 A4
- 4405 D9
- 4406 D9
- 4904 F4
- 5430 A4
- 6430 A8
- 6431 B8
- 6432 C8
- 6436 D4
- 6437 D1
- 6438 F2
- 6439 E8
- 6440 F8
- 7430 A2
- 7431 E7
- 7432 D3
- 7433 F7
- 7434-A D7
- 7434-B D8
- F330 E2
- F331 E9
- F334 E9
- F336 C9
- F337 A9
- F338 A9
- F340 D9
- F341 D9
- F9202 D2

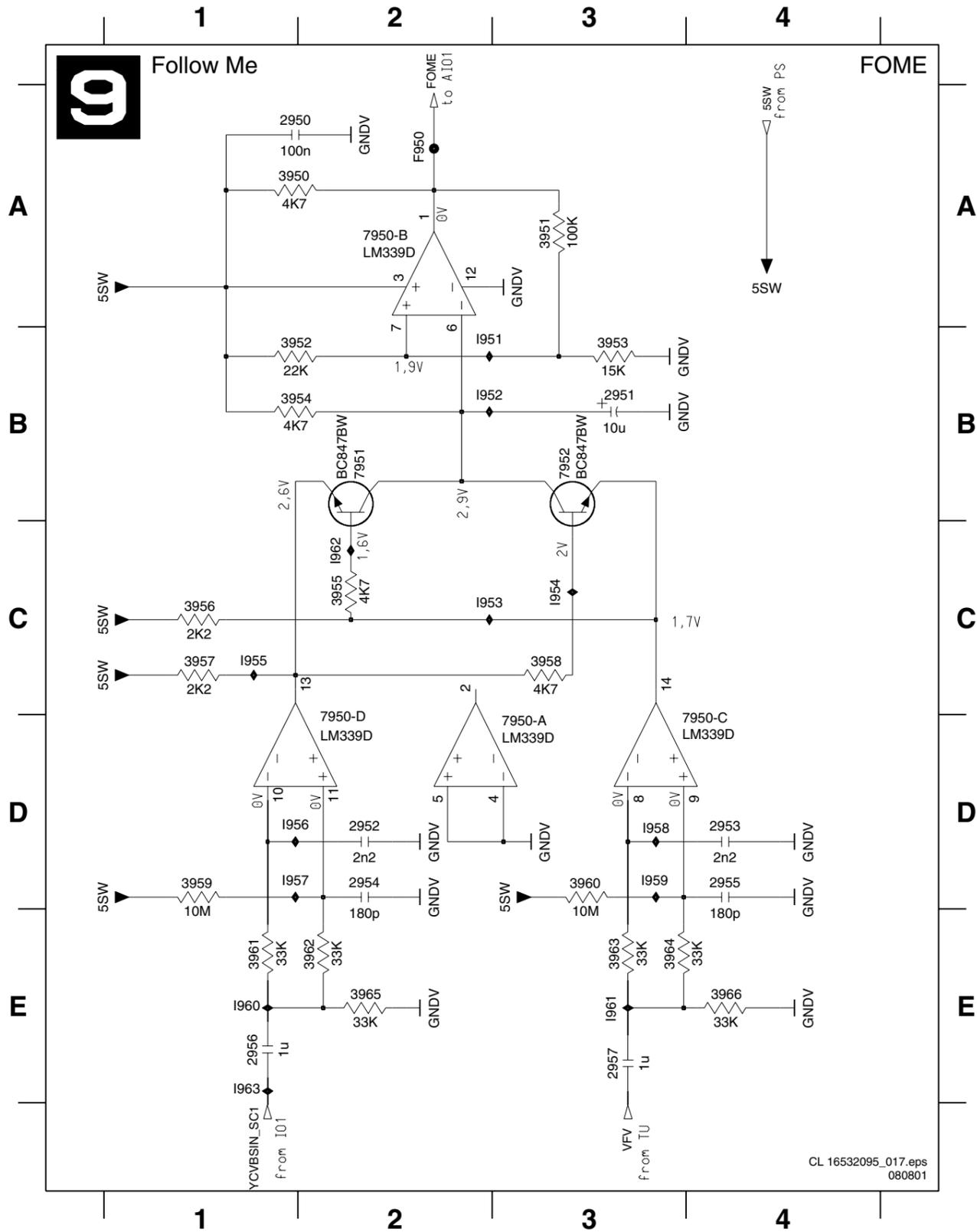
Analog Board: Sound Processing



- 1600 F7
- 1960 D1
- 2600 A6
- 2601 A6
- 2602 A7
- 2603 A7
- 2604 A9
- 2605 B8
- 2606 B8
- 2607 C2
- 2608 C9
- 2609 C2
- 2610 C8
- 2612 D8
- 2614 E1
- 2615 E1
- 2616 E8
- 2617 E8
- 2620 F7
- 2621 F7
- 2622 F5
- 2623 F6
- 2624 D2
- 2625 D2
- 3600 A8
- 3601 B1
- 3602 B9
- 3603 B2
- 3604 E2
- 3605 E2
- 3606 D2
- 3607 D2
- 4601 A5
- 5600 A8
- 5601 F5
- 5602 F6
- 6600 B9
- 7600 B6
- C670 A3
- F6001 D1
- F6002 D1
- F6004 D1
- I600 A4
- I601 A6
- I602 A7
- I603 A7
- I604 A8
- I605 B7
- I606 B7
- I607 D8
- I609 F7
- I611 F7
- I612 F6
- I613 F5
- I614 E2
- I615 E2
- I616 E2
- I617 E2
- I619 C2
- I620 C1
- I622 C2
- I623 B2
- I624 B2

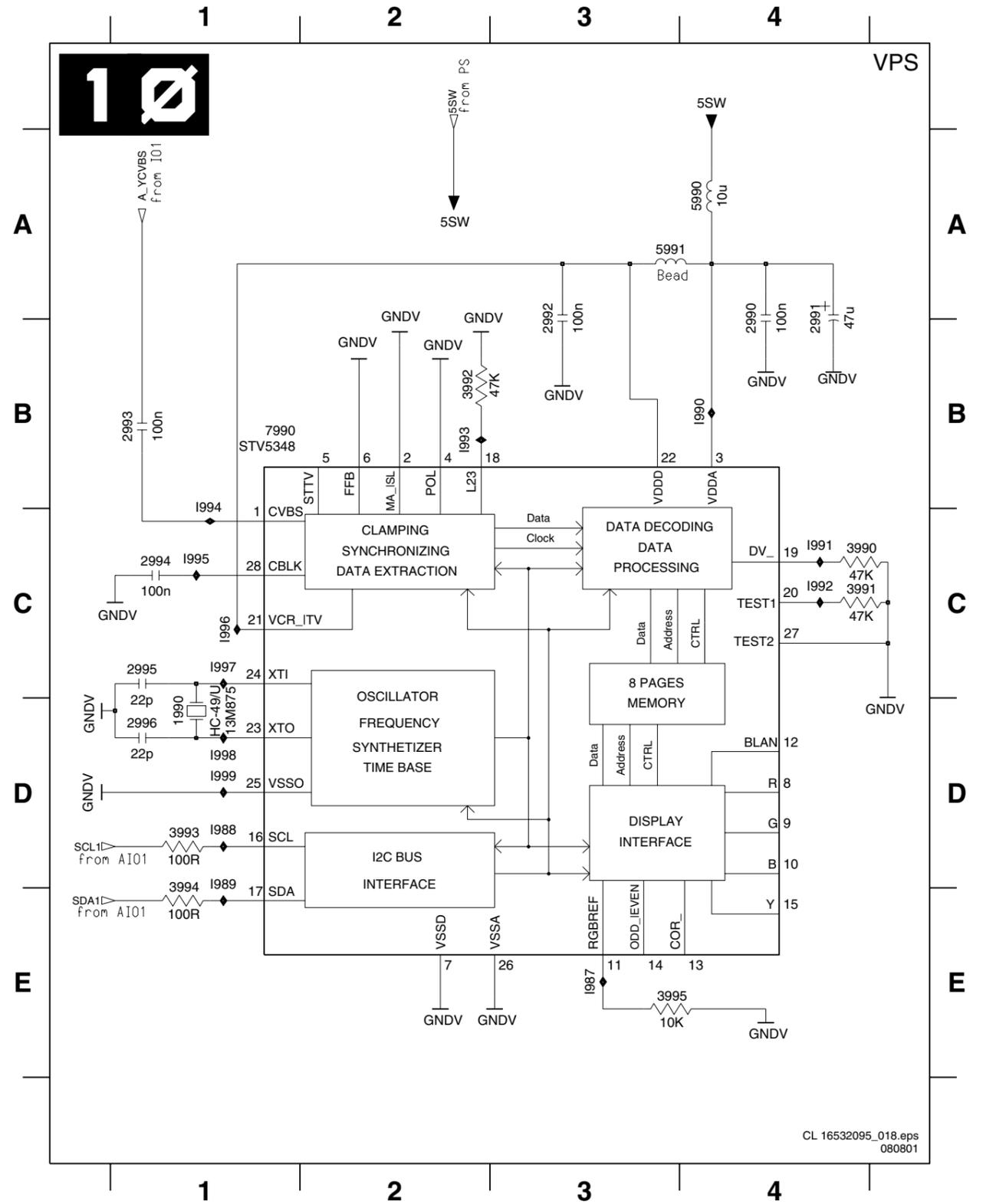
Analog Board: Follow Me

2950 A1	2954 D2	3950 A1	3954 B1	3958 C3	3962 E2	3966 E4	7950 D4	I951 B2	I955 C1	I959 D3	I963 E1
2951 B3	2955 D4	3951 A3	3955 C2	3959 D1	3963 E3	7950 A2	7951 B2	I952 B2	I956 D1	I960 E1	
2952 D2	2956 E1	3952 B1	3956 C1	3960 D3	3964 E3	7950 D2	7952 B3	I953 C2	I957 D1	I961 E3	
2953 D4	2957 E3	3953 B3	3957 C1	3961 E1	3965 E2	7950 D2	F950 A3	I954 C3	I958 D3	I962 C2	

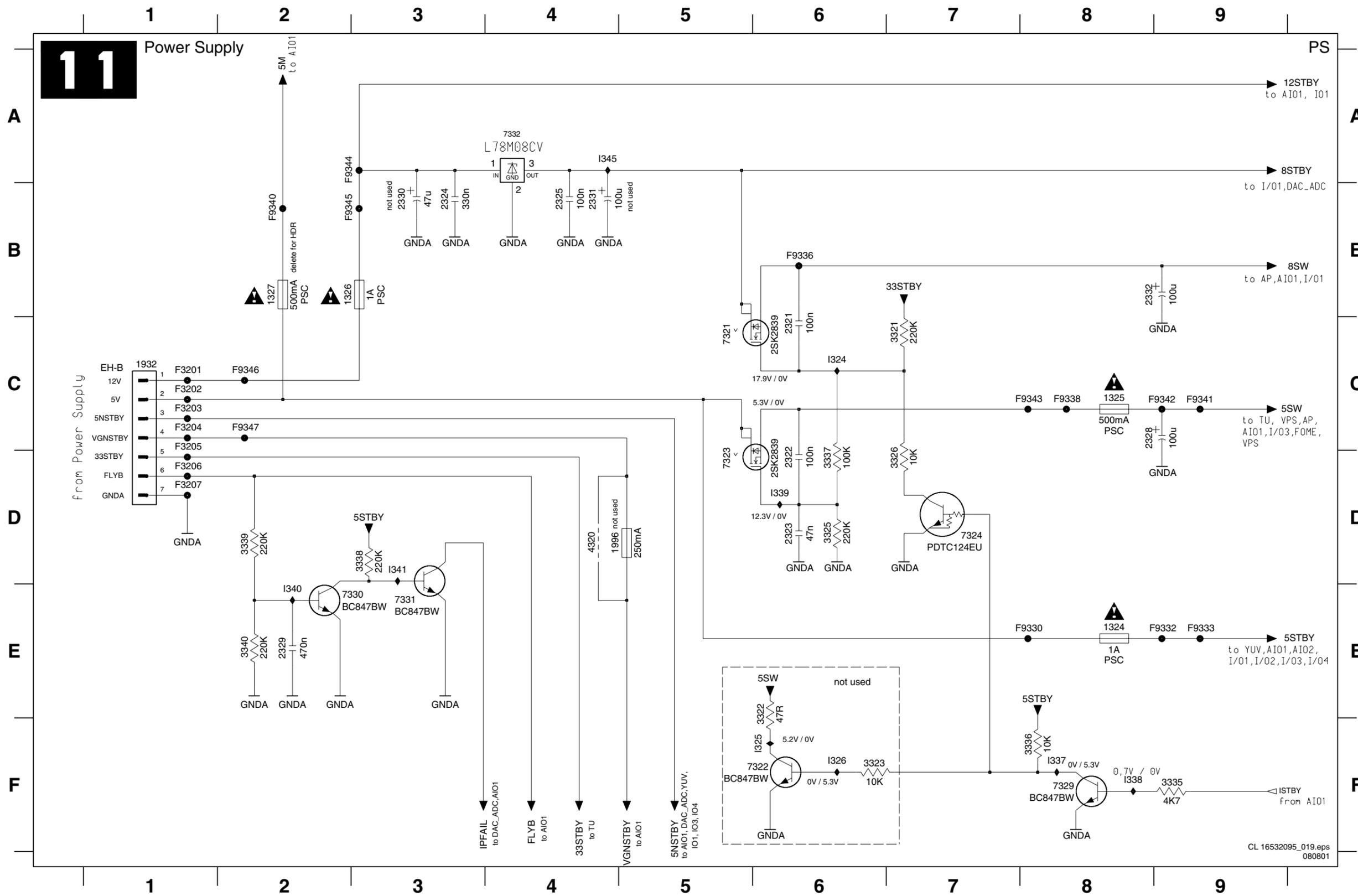


Analog Board: VPS

1990 D1	2992 A3	2995 C1	3991 C4	3994 E1	5991 A3	I988 D1	I991 C4	I994 B1	I997 C1
2990 A4	2993 B1	2996 D1	3992 B2	3995 E3	7990 B1	I989 D1	I992 C4	I995 C1	I998 D1
2991 A4	2994 C1	3990 C4	3993 D1	5990 A4	I987 E3	I990 B4	I993 B2	I996 C1	I999 D1

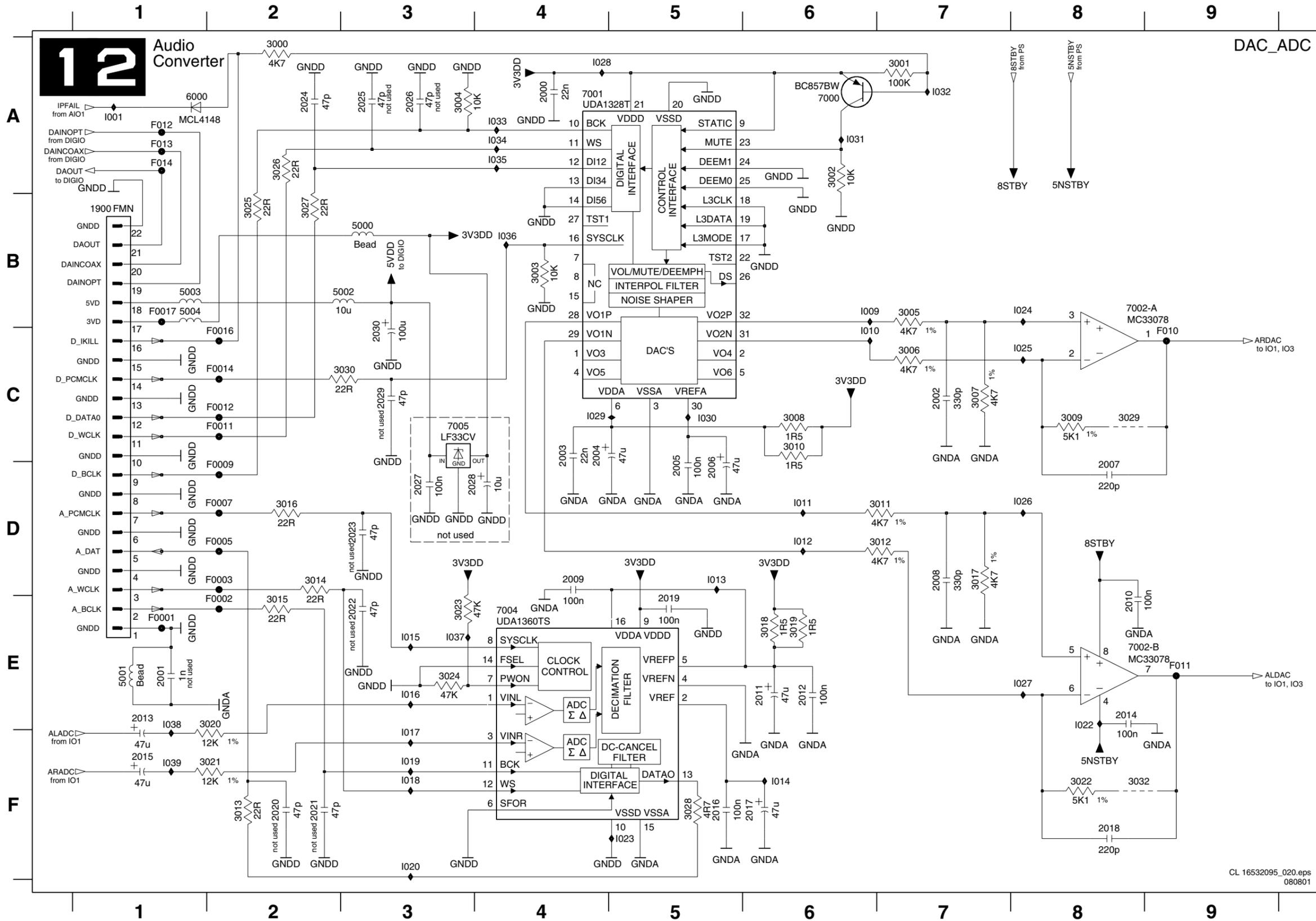


Analog Board: Power Supply



- 1324 E8
- 1325 C8
- 1326 B2
- 1327 B2
- 1932 C1
- 1996 D4
- 2321 C6
- 2322 D6
- 2323 D6
- 2324 B3
- 2325 B4
- 2328 C8
- 2329 E2
- 2330 B3
- 2331 B4
- 2332 B8
- 3321 C7
- 3322 E6
- 3323 F6
- 3325 D6
- 3326 D7
- 3335 F9
- 3336 F8
- 3337 D6
- 3338 D3
- 3339 D2
- 3340 E2
- 4320 D4
- 7321 C5
- 7322 F6
- 7323 D5
- 7324 D7
- 7329 F8
- 7330 E2
- 7331 E3
- 7332 A4
- F3201 C1
- F3202 C1
- F3203 C1
- F3204 C1
- F3205 C1
- F3206 D1
- F3207 D1
- F9330 E8
- F9332 E9
- F9333 E9
- F9336 B6
- F9338 C8
- F9340 B2
- F9341 C9
- F9342 C9
- F9343 C8
- F9344 A3
- F9345 B3
- F9346 C2
- F9347 C2
- I324 C6
- I325 F6
- I326 F6
- I337 F8
- I338 F8
- I339 D6
- I340 E2
- I341 D3
- I345 A4

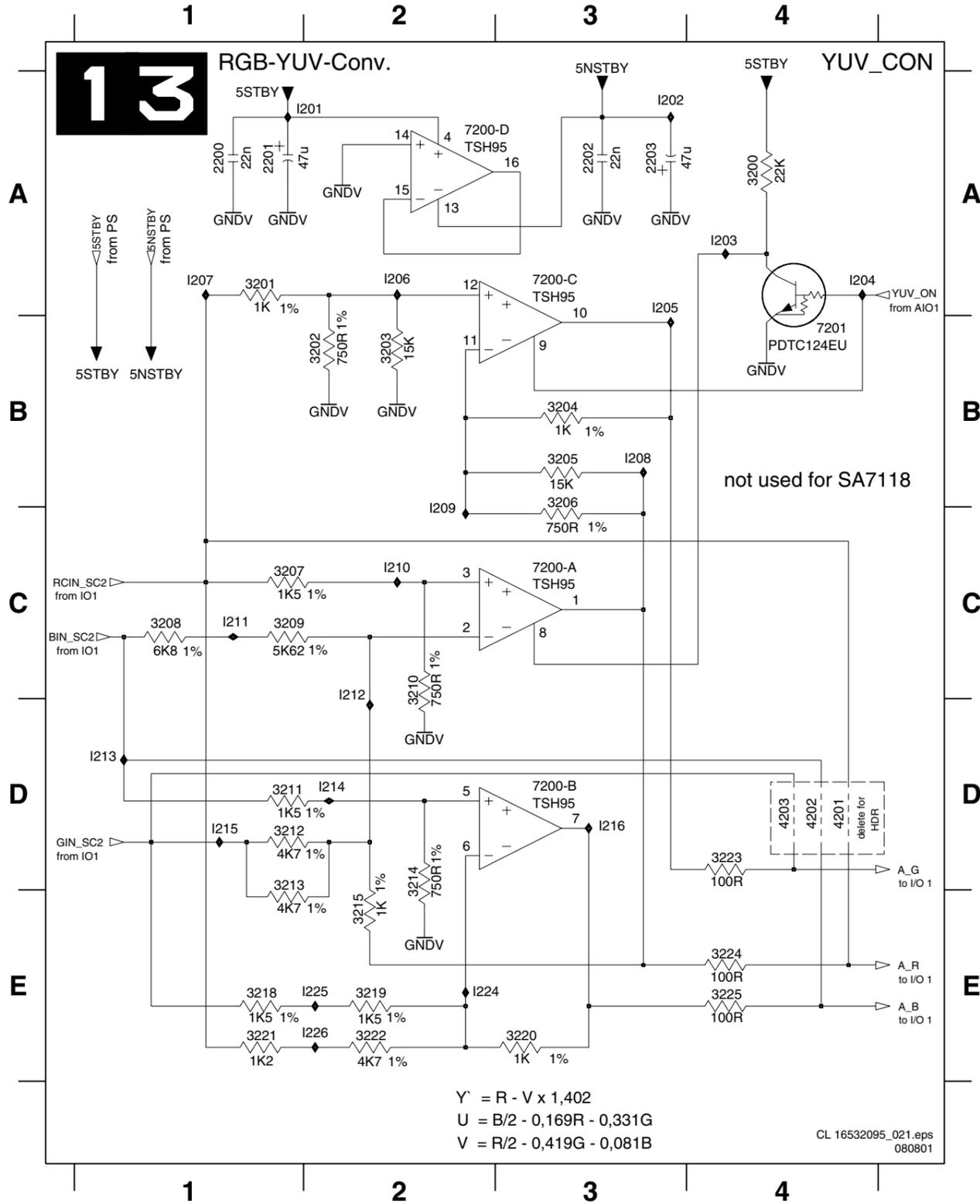
Analog Board: Audio Converter



- 1900 B1
- 2000 A4
- 2001 E1
- 2002 C7
- 2003 C4
- 2004 C4
- 2005 D5
- 2006 D5
- 2007 D8
- 2008 D7
- 2009 D4
- 2010 E8
- 2011 E6
- 2012 E6
- 2013 E1
- 2014 E8
- 2015 F1
- 2016 F5
- 2017 F6
- 2018 F8
- 2019 E5
- 2020 F2
- 2021 F2
- 2022 E3
- 2023 D3
- 2024 A2
- 2025 A3
- 2026 A3
- 2027 D3
- 2028 D4
- 2029 C3
- 2030 C3
- 3000 A2
- 3001 A7
- 3002 A6
- 3003 B4
- 3004 A3
- 3005 B7
- 3006 C7
- 3007 C7
- 3008 C6
- 3009 C8
- 3010 C6
- 3011 D7
- 3012 D7
- 3013 F2
- 3014 D2
- 3015 E2
- 3016 D2
- 3017 D7
- 3018 E6
- 3019 E6
- 3020 E2
- 3021 F2
- 3022 F8
- 3023 E3
- 3024 E3
- 3025 B2
- 3026 A2
- 3027 B2
- 3028 F5
- 3029 C8
- 3030 C3
- 3032 F8
- 5000 B3
- 5001 E1
- 5002 B3
- 5003 B1
- 5004 B1
- 6000 A1
- 7000 A6
- 7001 A4
- 7002-A B8
- 7002-B E8
- 7004 E4
- 7005 C3
- F0001 E1
- F0002 E2
- F0003 D2
- F0005 D2
- F0007 D2
- F0009 D2
- F0011 C2
- F0012 C2
- F0014 C2
- F0016 C2
- F0017 B1
- F010 C9
- F011 E9
- F012 A1
- F013 A1
- F014 A1
- I001 A1
- I009 B6
- I010 C6
- I011 D6
- I012 D6
- I013 D5
- I014 F6
- I015 E3
- I016 E3
- I017 F3
- I018 F3
- I019 F3
- I020 F3
- I022 E8
- I023 F5
- I024 B8
- I025 C8
- I026 D8
- I027 E8
- I028 A4
- I029 C4
- I030 C5
- I031 A6
- I032 A7
- I033 A4
- I034 A4
- I035 A4
- I036 B4
- I037 E3
- I038 E1
- I039 F1

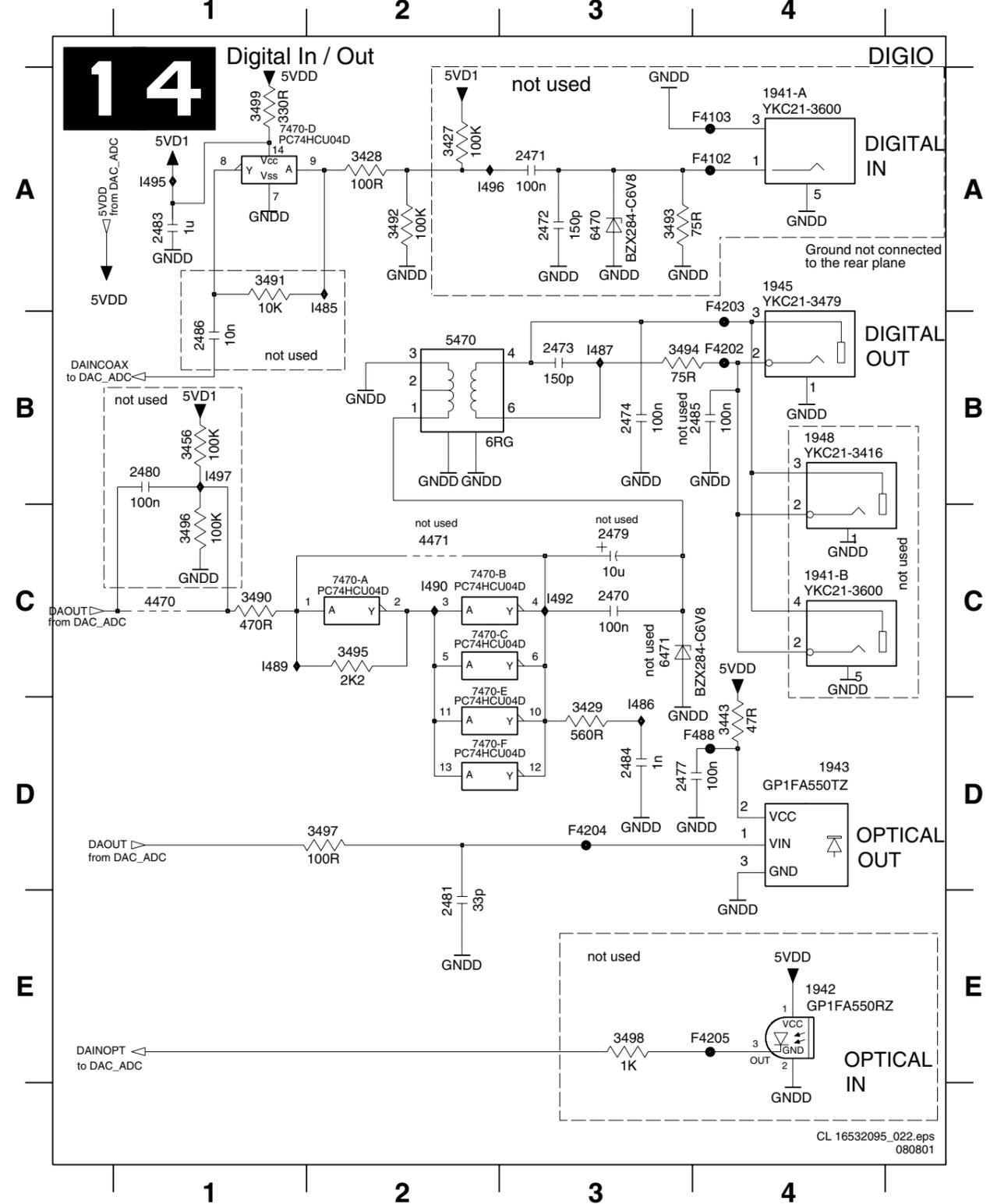
Analog Board: RGB-YUV-Converter

2200 A1	3202 B2	3208 C1	3214 D2	3222 E2	4203 D4	I201 A2	I207 A1	I213 D1	I226 E2
2201 A1	3203 B2	3209 C1	3215 E2	3223 D4	7200-A C3	I202 A3	I208 B3	I214 D2	
2202 A3	3204 B3	3210 C2	3218 E1	3224 E4	7200-B D3	I203 A4	I209 C2	I215 D1	
2203 A3	3205 B3	3211 D1	3219 E2	3225 E4	7200-C A3	I204 A4	I210 C2	I216 D3	
3200 A4	3206 B3	3212 D1	3220 E3	4201 D4	7200-D A2	I205 A3	I211 C1	I224 E2	
3201 A1	3207 C1	3213 D1	3221 E1	4202 D4	7201 B4	I206 A2	I212 C2	I225 E2	



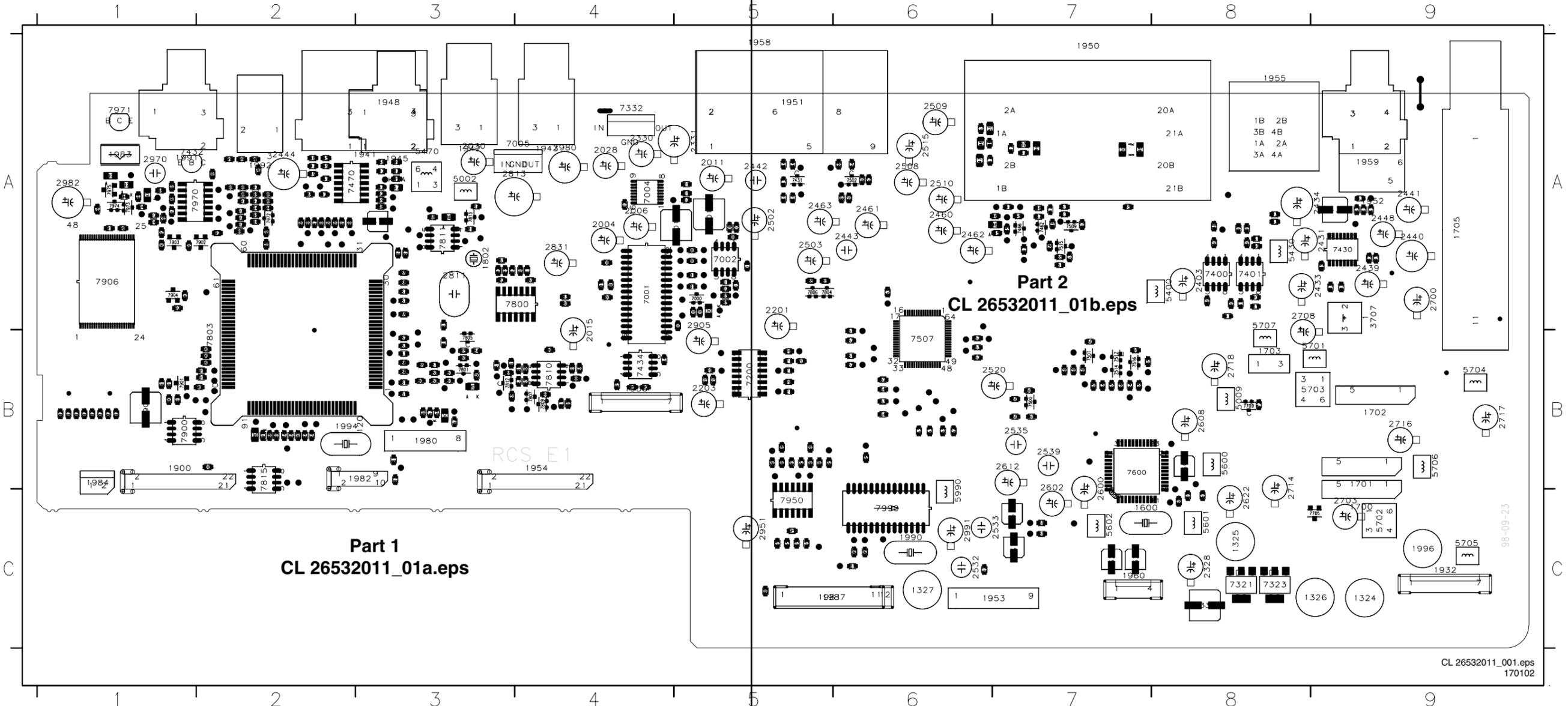
Analog Board: Digital In / Out

1941-A A4	2471 A3	2481 E2	3429 D3	3494 B3	4471 C2	7470-D A1	F4204 D3	I490 C2
1941-B C4	2472 A3	2483 A1	3443 D4	3495 C2	5470 B2	7470-E C2	F4205 E4	I492 C3
1942 E4	2473 B3	2484 D3	3456 B1	3496 C1	6470 A3	7470-F D2	F488 D4	I495 A1
1943 D4	2474 B3	2485 B4	3490 C1	3497 D2	6471 C3	F4102 A4	I485 A2	I496 A2
1945 A4	2477 D3	2486 B1	3491 A1	3498 E3	7470-A C2	F4103 A4	I486 D3	I497 B1
1948 B4	2479 C3	3427 A2	3492 A2	3499 A1	7470-B C2	F4202 B4	I487 B3	
2470 C3	2480 B1	3428 A2	3493 A3	4470 C1	7470-C C2	F4203 A4	I489 C1	

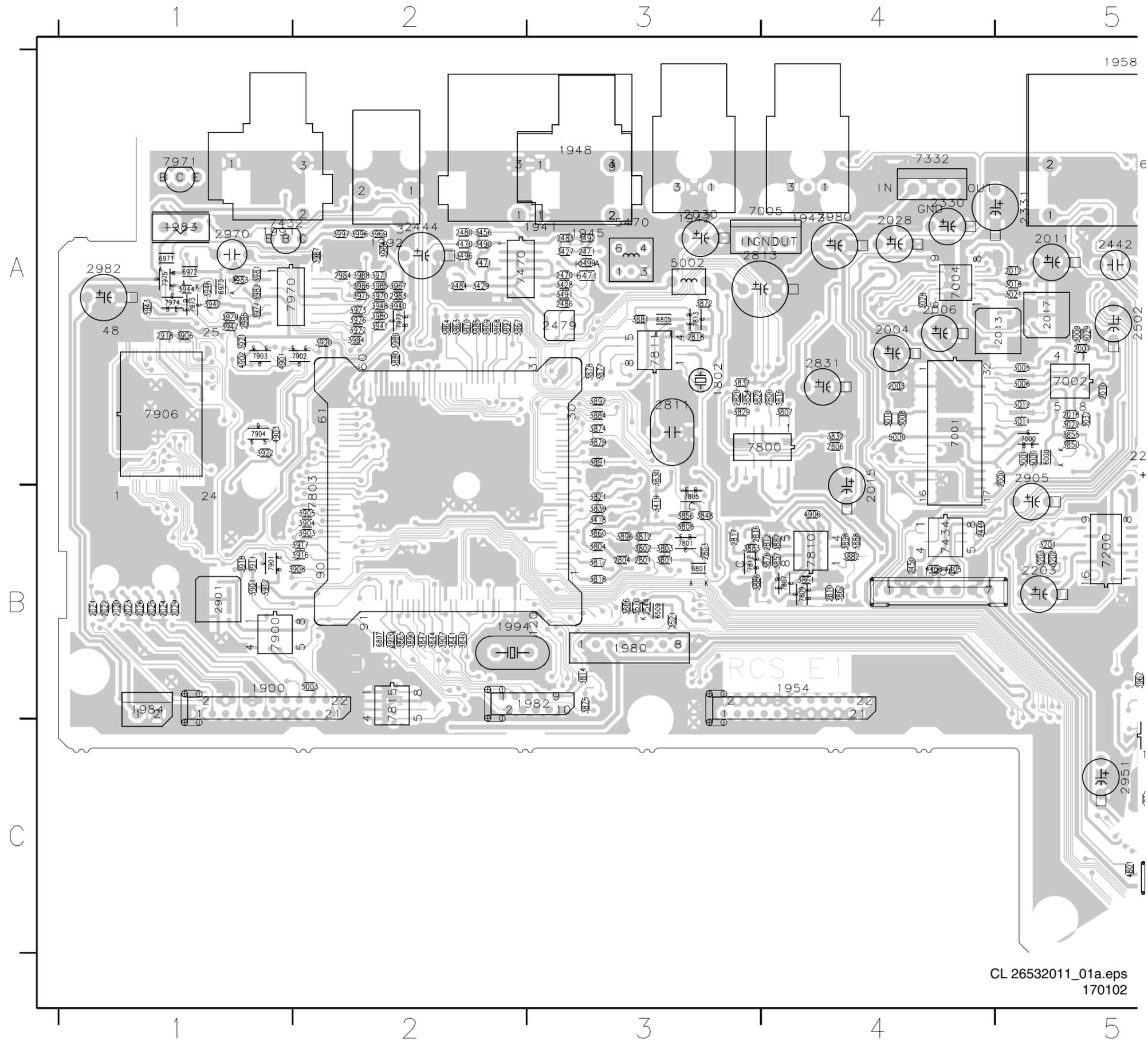


Layout Analog Board (Overview Top View)

1323 C8	1954 B4	2012 A5	2405 A8	2463 A5	2522 B6	2622 C8	2901 B1	3012 A5	3418 B3	3471 A6	3523 B6	3604 C7	3841 B2	3874 A3	3905 B2	3961 B5	3987 A2	5601 C8	7000 A5	7507 B6	7906 A1
1324 C9	1955 A8	2013 A5	2406 A8	2464 A7	2523 A7	2624 C7	2903 A3	3018 A5	3419 B3	3472 A7	3526 A6	3605 C7	3844 B2	3875 B3	3906 A1	3962 B5	3988 A2	5602 C7	7001 A4	7509 A7	7950 C5
1326 C9	1956 B4	2015 B4	2407 A8	2466 A7	2523 C6	2625 C7	2918 A1	3021 A5	3423 A9	3473 A7	3528 B6	3707 A9	3847 B2	3876 B4	3908 B2	3963 B5	3989 A2	5701 B9	7002 A5	7514 B7	7970 A1
1327 C6	1958 A5	2017 A5	2408 A8	2469 A7	2528 B6	2700 A9	2950 C5	3022 A5	3427 A3	3474 A7	3531 B6	3725 B8	3848 B3	3877 A3	3910 B2	3964 B5	3993 C6	5702 C9	7003 A4	7600 B7	7971 A1
1600 C7	1959 A9	2018 A5	2430 A9	2470 A3	2529 B6	2703 C9	2951 C5	3028 A4	3428 A3	3475 A7	3532 A6	3801 B3	3850 A5	3878 A3	3911 B1	3965 B5	3994 C6	5703 B9	7004 A4	7705 C9	7972 A2
1700 C9	1960 C7	2020 B1	2431 A9	2471 A3	2530 B6	2708 A8	2952 B5	3029 A5	3429 A2	3477 A7	3533 A6	3802 B3	3852 A5	3879 A3	3912 B1	3966 B5	3996 A2	5703 C9	7200 B5	7709 B8	7973 A1
1701 B9	1980 B3	2021 B1	2433 A9	2479 A3	2530 A7	2714 B8	2953 B5	3032 A5	3431 A9	3479 A7	3533 A7	3803 B3	3853 A6	3880 A2	3916 B2	3967 A2	3997 A2	5704 B9	7315 A7	7800 A4	7974 A1
1702 B9	1981 C5	2022 B1	2434 A9	2480 A2	2532 C6	2716 B9	2956 B6	3110 C4	3432 A8	3489 A7	3536 B7	3804 B3	3854 A3	3881 A3	3917 B2	3968 A2	4202 B3	5706 B9	7316 B7	7801 B3	7975 A1
1703 B8	1982 B3	2023 B1	2436 A9	2483 A3	2533 C7	2717 B9	2957 B5	3201 B5	3433 A9	3490 A2	3537 A7	3807 A4	3855 A5	3882 B4	3918 B1	3969 A2	4405 B4	5707 A8	7317 B7	7803 B2	7990 C6
1703 A9	1983 A1	2024 B1	2437 A9	2484 A2	2533 B7	2718 B8	2970 A1	3202 B5	3434 A9	3491 A3	3537 B7	3808 B3	3856 B3	3883 B3	3920 A2	3970 A2	4406 B4	5902 B2	7321 C8	7804 A3	
1802 A3	1984 B1	2025 B1	2438 A9	2486 A3	2537 B6	2800 A4	2980 A4	3203 B5	3435 A8	3492 A3	3538 B7	3812 B3	3857 B4	3884 A3	3921 A1	3971 A2	4470 A2	5990 C6	7323 C8	7805 B3	
1900 B1	1987 C6	2026 B1	2439 A9	2500 B7	2538 B6	2801 B3	2982 A1	3207 B5	3437 A9	3496 A2	3539 A7	3814 B3	3859 A5	3885 A2	3922 A1	3972 A2	4471 A2	6000 A5	7332 A4	7806 A5	
1910 C3	1990 C6	2028 A4	2440 A9	2501 B7	2539 B7	2803 B3	2983 A2	3208 B5	3439 A5	3499 A3	3539 B7	3815 A4	3860 B5	3886 B3	3930 C5	3973 A2	4801 C5	6304 A7	7400 A8	7807 B4	
1911 C3	1991 A1	2029 B1	2441 A9	2502 A5	2541 B7	2804 B3	2984 A2	3210 B5	3440 A5	3500 B7	3541 B6	3817 B3	3861 B4	3887 B4	3940 A2	3975 A2	4901 A1	6309 B3	7401 A8	7809 B4	
1932 C9	1992 A2	2030 A3	2442 A3	2503 A5	2542 B7	2806 A4	2985 A1	3211 B5	3441 A5	3501 B7	3542 B6	3818 B3	3862 B4	3888 B4	3941 A2	3976 A2	4902 A1	6461 A7	7430 A9	7810 B4	
1941 A3	1994 B2	2201 A5	2443 A6	2508 A6	2544 B3	2810 B4	2991 C6	3214 B5	3442 A5	3502 A6	3560 B7	3819 C6	3863 A2	3890 B2	3942 A1	3977 A1	4903 A1	6463 A7	7431 A5	7811 A3	
1942 A3	1996 C9	2203 B5	2444 A2	2509 A6	2547 A6	2811 A3	3000 A5	3402 A8	3445 A9	3503 B7	3561 B7	3821 B3	3864 A2	3891 A3	3943 A1	3979 A1	4906 B4	6468 A7	7432 A1	7812 B3	
1943 A4	2000 A3	2328 C8	2446 A5	2510 A6	2600 B7	2812 B4	3001 A5	3403 A8	3456 A2	3503 B7	3564 A6	3822 A3	3865 B2	3892 A3	3944 A1	3980 A2	5000 A4	6471 A3	7434 B4	7813 A3	
1943 A3	2003 A4	2330 A4	2448 A9	2512 B6	2602 B7	2813 A3	3005 A5	3404 A8	3457 A7	3504 B7	3568 A7	3823 A3	3866 B3	3896 B3	3946 A1	3981 A1	5002 A3	6801 B3	7462 A7	7815 B2	
1948 A3	2004 A4	2331 A5	2449 B4	2513 A6	2603 B8	2816 B3	3006 A5	3409 A8	3458 A7	3506 B7	3570 B3	3830 A3	3867 A2	3897 A2	3947 A1	3982 A1	5003 B2	6803 A3	7466 A7	7900 B1	
1950 A7	2006 A4	2332 C8	2450 B4	2514 A7	2608 B8	2817 B3	3008 A4	3412 A8	3459 A7	3507 A6	3600 C8	3832 A4	3868 A2	3898 B4	3948 A2	3983 A1	5009 B8	6807 B2	7470 A2	7901 B1	
1951 A5	2007 A5	2336 B6	2460 A6	2517 B6	2612 B7	2818 A3	3009 A5	3413 A8	3464 A6	3517 A6	3600 B8	3837 A3	3869 A2	3901 B1	3951 C5	3984 A2	5400 A8	6970 A1	7500 B7	7902 A2	
1952 A9	2010 A5	2400 A8	2461 A6	2520 B7	2614 C7	2820 A3	3010 A4	3414 A8	3465 A6	3521 B3	3601 C8	3839 B3	3870 A2	3903 B2	3952 C5	3985 A2	5430 A8	6971 A1	7501 B7	7903 A1	
1953 C7	2011 A5	2403 A8	2462 A6	2521 B6	2615 C7	2831 A4	3011 A5	3415 A8	3470 A6	3523 A7	3603 C8	3840 B2	3872 A3	3904 B2	3953 C5	3986 A2	5470 A3	6972 A1	7502 A6	7904 A1	

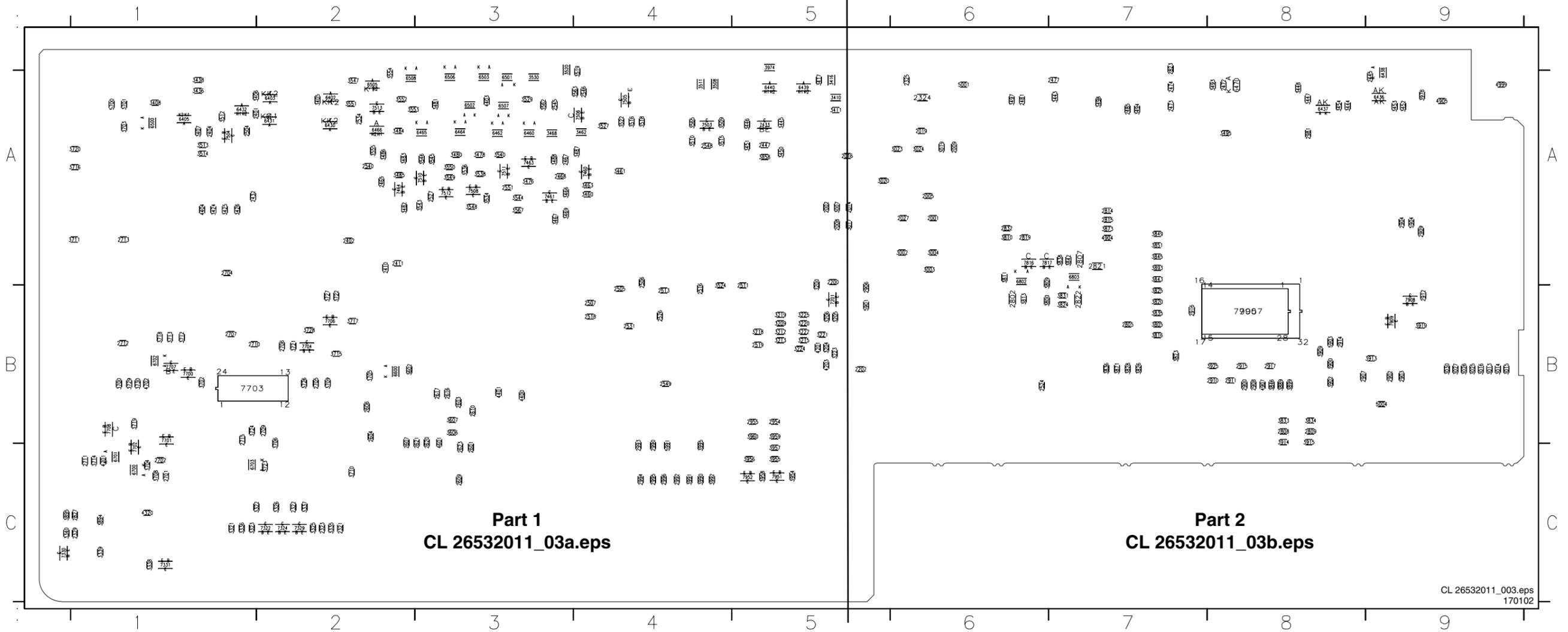


Layout Analog Board (Part 1 Top View)



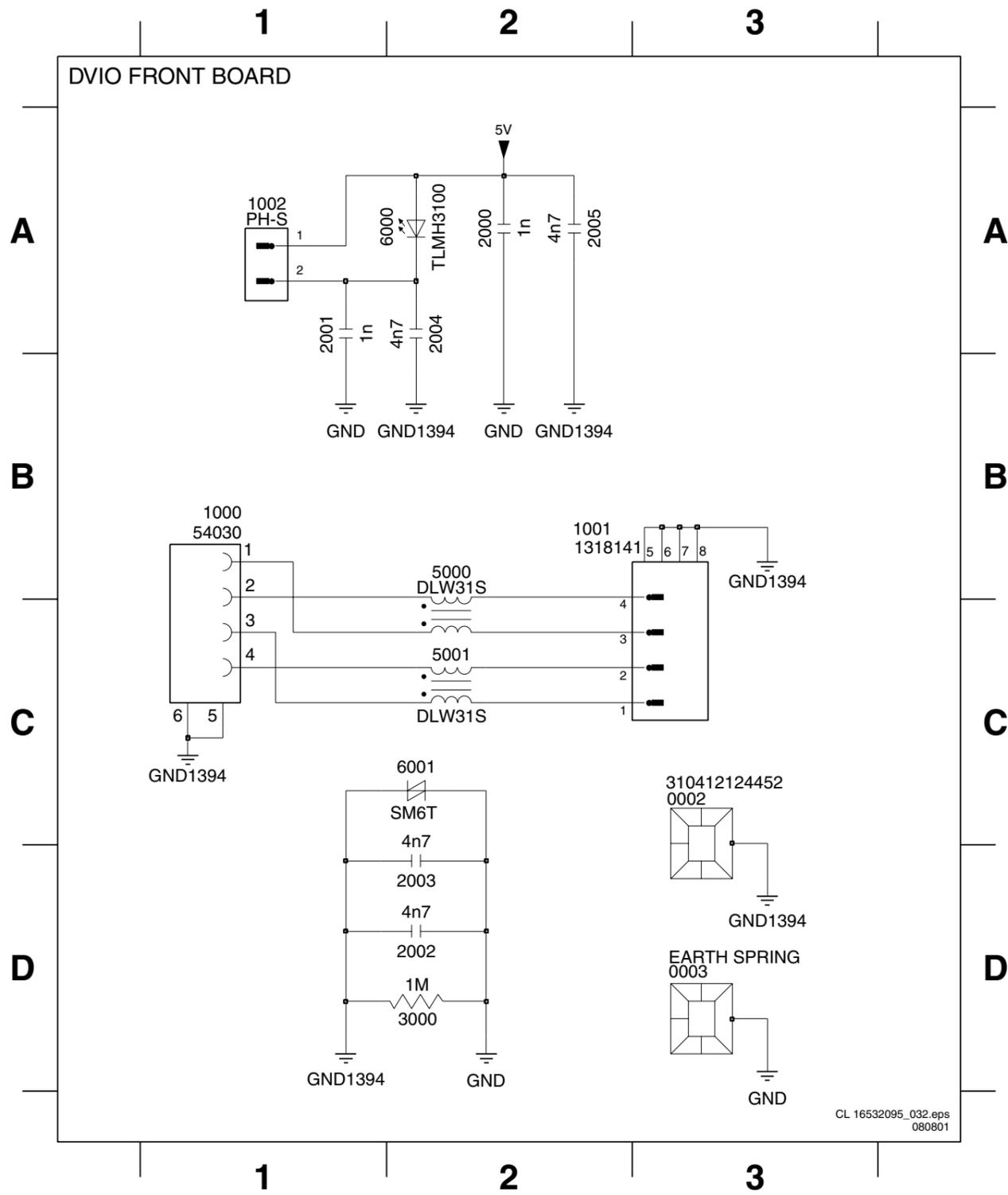
Layout Analog Board (Overview Bottom View)

2001 A6	2329 C1	2513 B4	2617 B3	2819 A6	2981 A8	3030 B9	3219 B5	3411 A5	3466 A3	3511 A4	3548 A3	3709 B2	3809 A6	3858 A5	3974 A5	5004 B9	6462 A3	7322 C2	7704 B2
2002 A5	2401 A1	2516 B4	2620 B3	2821 A7	2990 C4	3100 C7	3220 B5	3416 A5	3467 A3	3512 A1	3549 A3	3710 C2	3810 A6	3871 B7	3978 A9	5700 A1	6464 A3	7324 C2	7706 B2
2005 A6	2402 A2	2518 B4	2621 B3	2822 B7	2992 C4	3101 C7	3221 B5	3417 A5	3468 A3	3513 A1	3550 A3	3711 A1	3811 A6	3873 A7	3990 C4	5901 B5	6465 A3	7329 C2	7707 B1
2008 A5	2404 A1	2519 B5	2623 C3	2823 A7	2993 C4	3102 C7	3222 B5	3424 A1	3469 A3	3514 A1	3551 A2	3712 B1	3813 B6	3889 B8	3991 C4	5903 B8	6466 A2	7330 C1	7708 B1
2009 A6	2410 A2	2524 B6	2701 C1	2827 C1	2994 C4	3103 C7	3223 B5	3425 A1	3476 A3	3515 A4	3552 A2	3713 B1	3816 B7	3893 A7	3992 C4	5904 A9	6470 A8	7331 C1	7816 A6
2014 A5	2411 A2	2526 B4	2702 C1	2832 A6	2995 C4	3104 C7	3224 B5	3426 A1	3478 A3	3516 A4	3553 A2	3714 C1	3820 B7	3894 C1	3995 C4	5991 C4	6500 A1	7433 A5	7817 A6
2016 A5	2432 A1	2527 A3	2704 A1	2900 B8	2996 C4	3105 C7	3225 B5	3436 A1	3480 A3	3518 A4	3554 A2	3715 B2	3823 B7	3895 C1	4101 C7	6100 C7	6501 A3	7460 A4	7905 B8
2019 A6	2445 A9	2531 B4	2705 B2	2902 B9	3002 A6	3106 C7	3321 C1	3438 A1	3481 A3	3519 A4	3555 A2	3716 A1	3824 B7	3899 B8	4102 C7	6101 C7	6502 A3	7461 A3	7907 B8
2027 A6	2447 A5	2534 A2	2706 B2	2903 B9	3005 A6	3107 C7	3322 C1	3443 A7	3482 A2	3520 A3	3562 A3	3717 B2	3825 B7	3900 B8	4201 B5	6102 C6	6503 A3	7463 A3	7908 B9
2100 C7	2465 A2	2540 A2	2707 B1	2904 A9	3004 A6	3108 C7	3323 C1	3444 A8	3483 A2	3522 A4	3565 A4	3718 B1	3826 B7	3902 B8	4203 B5	6103 C6	6505 A2	7464 A2	7909 B9
2101 C7	2467 A3	2545 A3	2709 B2	2906 B5	3007 A5	3109 C6	3325 C2	3445 A5	3484 A2	3524 B4	3565 A4	3719 B1	3828 B7	3909 B8	4520 C1	6104 C6	6506 A3	7505 A4	7951 C5
2102 C7	2468 A3	2546 A4	2710 B1	2907 B8	3015 B9	3111 C6	3326 C2	3446 A5	3485 A2	3527 A4	3567 A3	3720 A1	3831 B7	3913 B9	4400 B3	6402 A2	6507 A3	7504 A1	7952 C5
2103 C7	2472 A8	2548 A4	2711 C1	2908 B8	3014 B9	3112 C6	3335 C2	3447 A8	3486 A2	3529 A3	3602 B2	3721 B2	3833 B8	3914 B8	4401 B3	6403 A2	6508 A2	7505 A4	
2104 C7	2473 A7	2549 B4	2712 B1	2909 A9	3015 B9	3113 C6	3336 C1	3448 A8	3487 A4	3530 A3	3606 B3	3722 B2	3834 B8	3915 B8	4403 A3	6405 A1	6600 B2	7506 A4	
2105 C7	2474 A7	2551 A3	2713 A1	2910 B8	3016 B9	3200 A5	3337 C2	3450 A5	3488 A3	3534 A3	3607 B3	3723 C2	3835 B7	3919 B9	4404 A1	6430 A2	6700 C1	7508 A3	
2106 C6	2477 A7	2601 C3	2715 B1	2911 B8	3017 A5	3204 B5	3338 C1	3451 A5	3493 A8	3536 A3	3700 B1	3724 B1	3836 B7	3925 B8	4601 B3	6431 A2	6701 C1	7510 A3	
2200 A5	2481 A6	2603 B3	2802 B6	2912 B9	3019 A6	3205 B5	3339 C1	3452 A9	3494 A7	3538 A3	3701 A1	3726 B2	3838 A7	3954 C5	4701 C1	6432 A1	6702 B1	7511 A3	
2202 B5	2485 A7	2604 B2	2805 B7	2914 B8	3020 A5	3206 B5	3340 C1	3453 A9	3495 A8	3540 A3	3702 B1	3727 B2	3843 A7	3955 C5	4702 B1	6436 A9	6703 C1	7512 A3	
2321 C2	2504 A1	2606 B2	2807 A7	2915 B8	3023 A6	3209 B5	3405 A2	3454 A8	3497 A6	3543 A3	3703 A1	3728 B2	3843 A7	3956 C5	4904 A7	6437 A8	6802 A6	7513 A2	
2322 C2	2505 B4	2607 B2	2808 B8	2916 B7	3024 A6	3212 B5	3406 A1	3460 A4	3498 A7	3544 A3	3704 C1	3729 B1	3845 A7	3957 C5	4905 A9	6438 A9	6803 A7	7700 B1	
2323 C2	2506 A4	2609 C3	2809 B8	2917 B8	3025 B9	3213 B5	3407 A1	3461 A4	3508 A4	3545 A3	3705 B2	3730 B1	3846 B8	3958 C5	4907 B8	6439 A5	7100 C7	7701 B1	
2324 A6	2507 B4	2610 B3	2814 A7	2954 B5	3026 B9	3215 B5	3408 A1	3462 A4	3509 A4	3546 A3	3706 B2	3800 B6	3849 A7	3959 B5	4999 A9	6440 A5	7101 C7	7702 C1	
2325 A6	2511 B5	2616 B3	2815 A7	2955 B5	3027 B9	3218 B5	3410 A5	3463 A4	3510 A4	3547 A2	3708 C1	3805 B7	3851 A7	3960 B5	5001 A6	6460 A3	7201 B5	7703 B1	

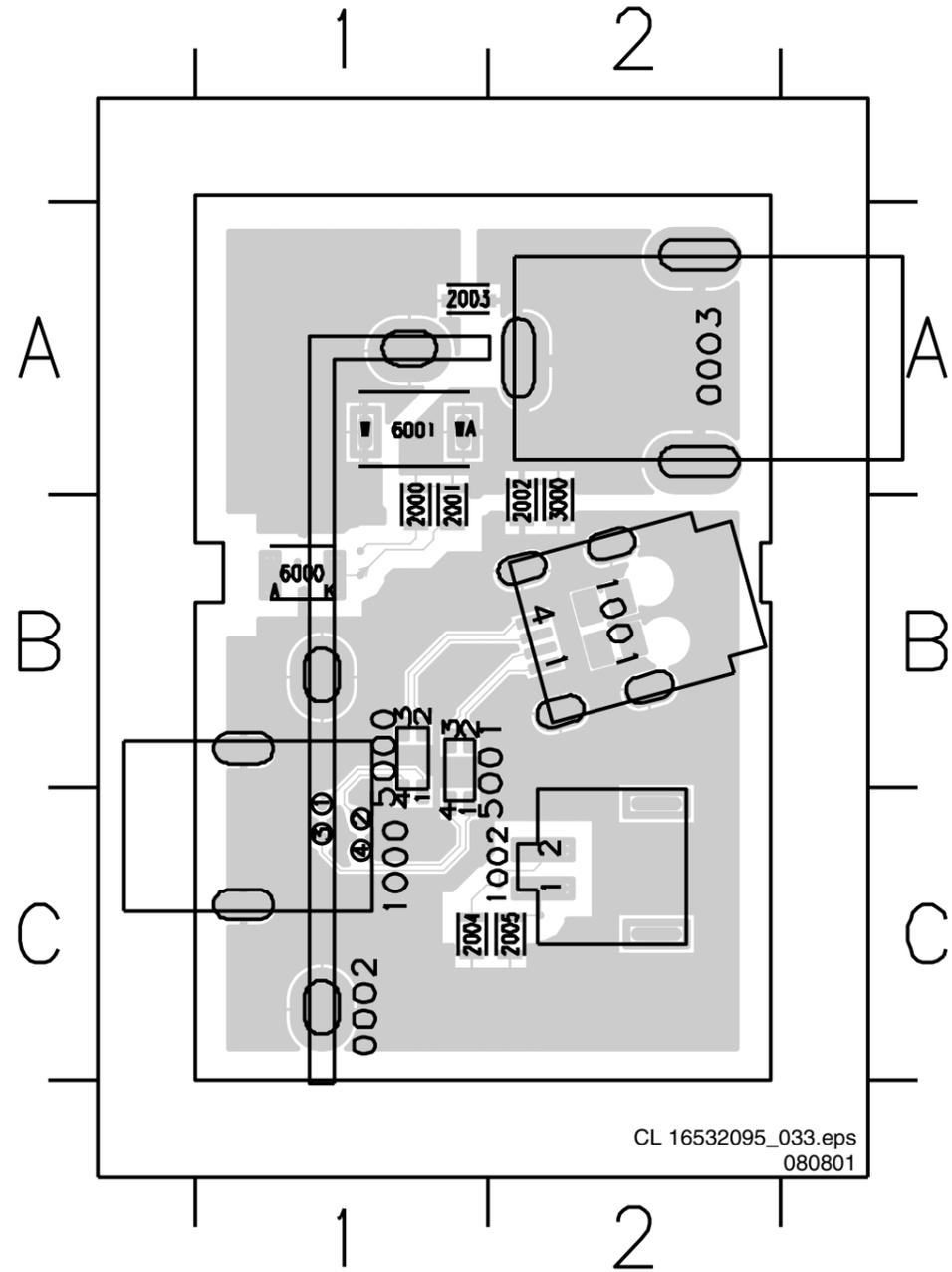


DVIO Front Board

0002 C3 1000 B1 1002 A1 2001 A1 2003 D2 5000 B2 6000 A2
 0003 D3 1001 B2 2000 A2 2002 D2 3000 D2 5001 C2 6001 C2



Layout DVIO Front Board

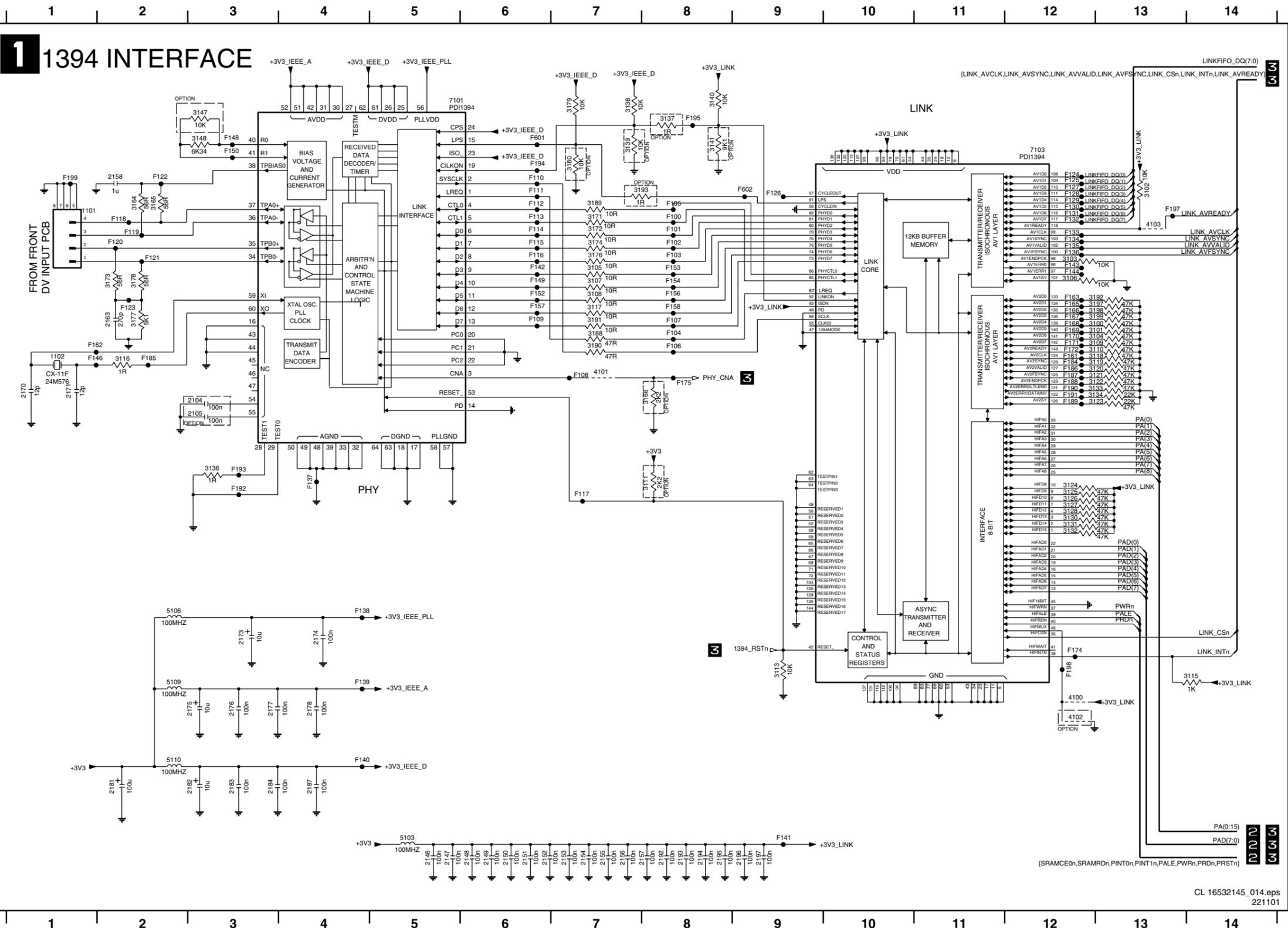


- 0002 C1
- 0003 A2
- 1000 C1
- 1001 B2
- 1002 C2
- 2000 B1
- 2001 B1
- 2002 B2
- 2003 A1
- 2004 C1
- 2005 C2
- 3000 B2
- 5000 B2
- 5001 B2
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- 6001 A1

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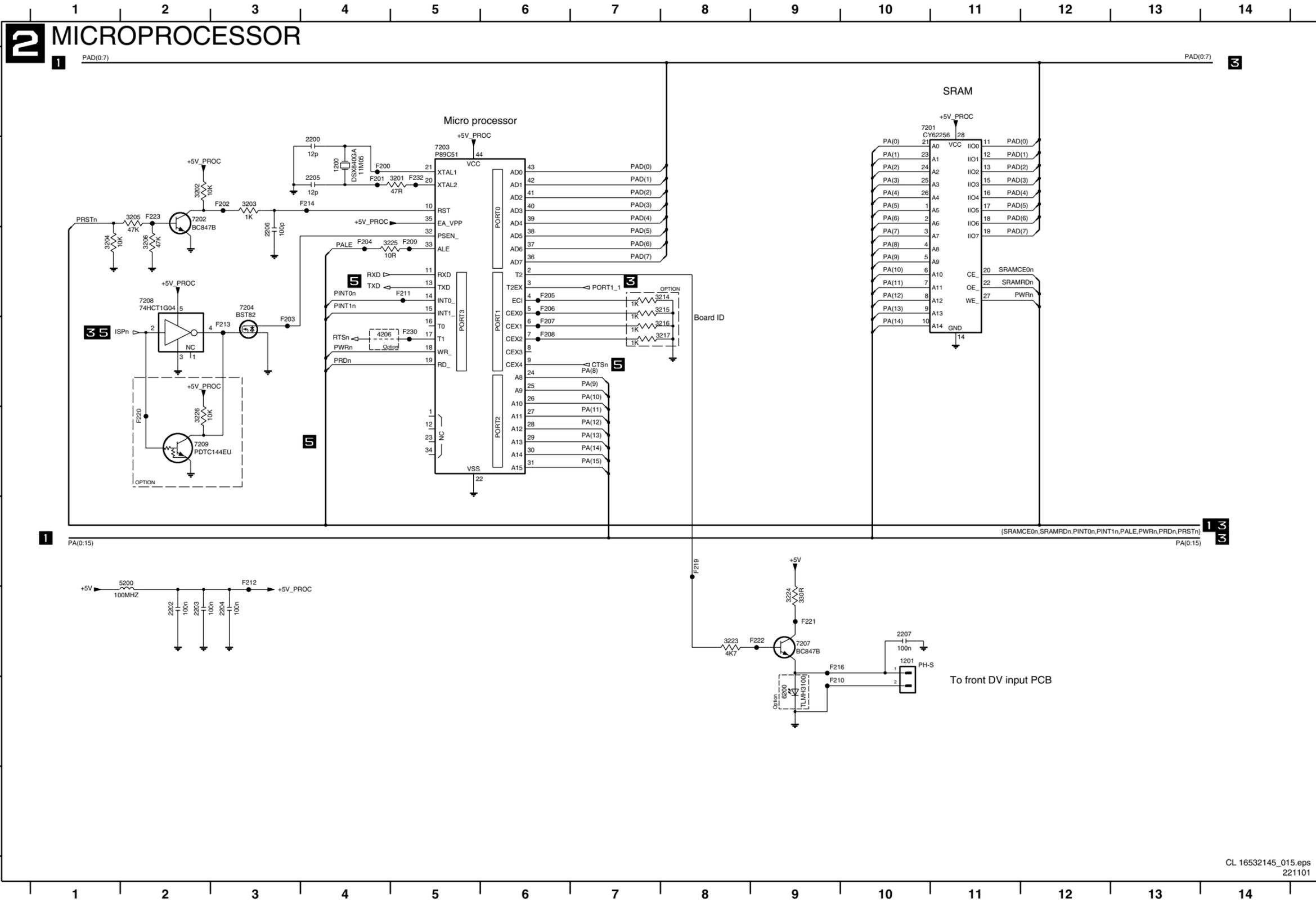
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DVIO Board: 1394 Interface



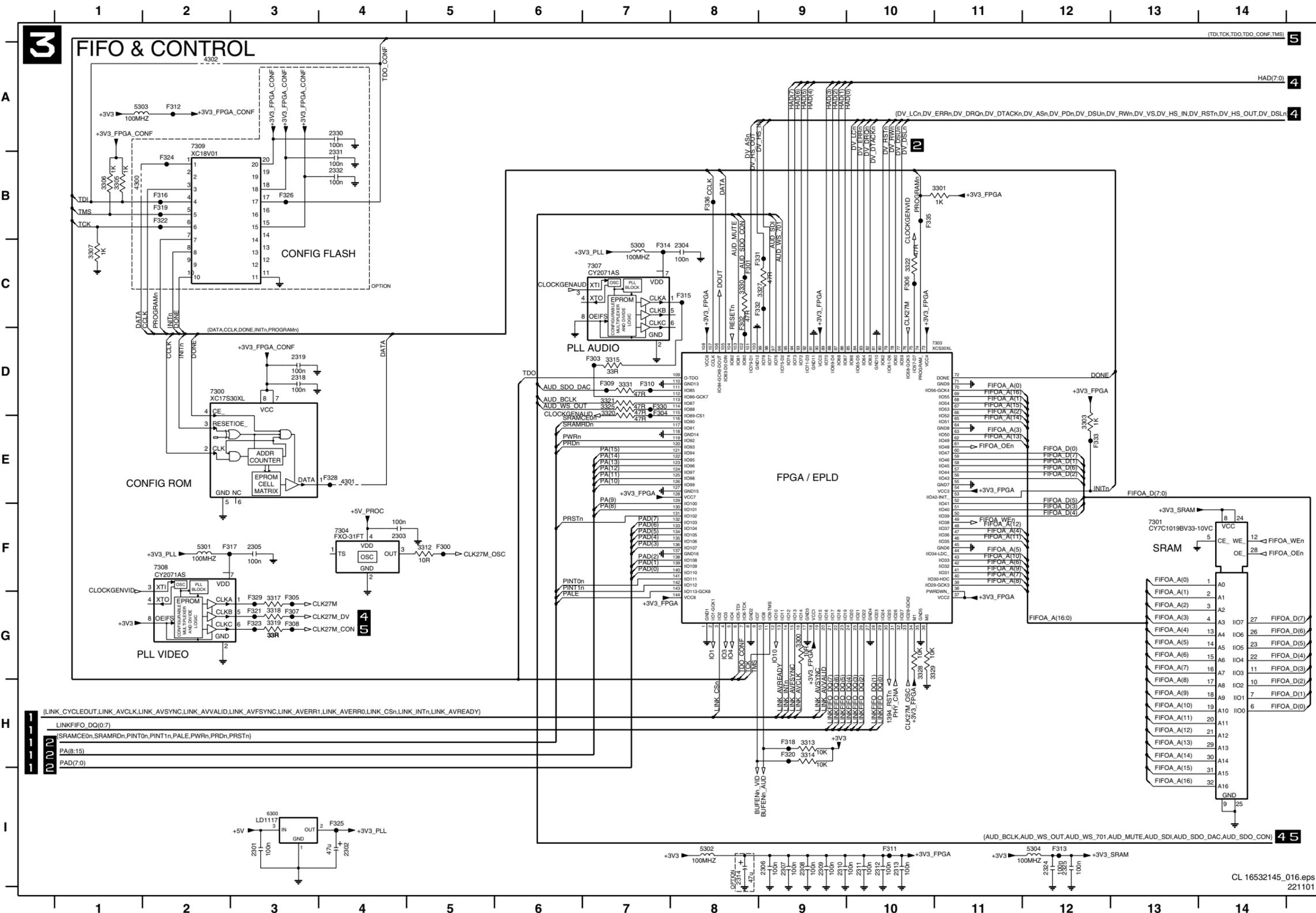
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1102	D1	3188	D7	F185	D2
2104	D3	3189	B7	F186	D12
2105	D3	3190	D7	F187	D12
2146	I5	3191	C7	F188	D12
2147	I5	3192	C13	F189	D12
2148	I6	3193	B7	F190	D12
2149	I6	3197	C13	F191	D12
2150	I6	3198	C13	F192	E3
2151	I6	3199	C13	F193	E3
2152	I6	4100	H12	F194	B6
2153	I7	4101	D7	F195	A8
2154	I7	4102	H12	F197	B13
2155	I7	4103	B13	F198	G12
2156	I7	5103	I5	F199	B1
2157	I8	5106	G2	F601	A6
2158	B2	5109	G2	F602	B9
2163	C2	5110	H2		
2170	D1	7101	A5		
2171	D1	7103	B12		
2173	G3	F100	B8		
2174	G4	F101	B8		
2175	H3	F102	C8		
2176	H3	F103	C8		
2177	H3	F104	D8		
2178	H4	F105	B8		
2181	I2	F106	D8		
2182	I3	F107	C8		
2183	I3	F108	D7		
2184	I3	F109	C6		
2187	I4	F110	B6		
2192	I8	F111	B6		
2193	I8	F112	B6		
2194	I8	F113	B6		
2195	I8	F114	B6		
2196	I9	F115	C6		
2197	I9	F116	C6		
3100	C13	F117	E7		
3101	D13	F118	B2		
3102	B13	F119	B2		
3103	C12	F120	C2		
3104	D13	F121	C2		
3105	C7	F122	B2		
3106	C12	F123	C2		
3107	C7	F124	B12		
3108	C7	F125	B12		
3109	D13	F126	B9		
3110	D13	F127	B12		
3111	E8	F128	B12		
3113	G9	F129	B12		
3115	G14	F130	B12		
3116	D2	F131	B12		
3117	C7	F132	B12		
3118	D13	F133	B12		
3119	D13	F134	C12		
3120	D13	F135	C12		
3121	D13	F136	C12		
3122	D13	F137	E4		
3123	D13	F138	G4		
3124	E12	F139	G4		
3125	E12	F140	H4		
3126	E12	F141	I9		
3127	E12	F142	C6		
3128	F12	F143	C12		
3130	F12	F144	C12		
3131	F12	F146	D1		
3132	F12	F148	A3		
3133	D13	F149	C6		
3134	D13	F150	B3		
3136	E3	F152	C6		
3137	A8	F153	C8		
3138	A7	F154	C8		
3139	A7	F156	C8		
3140	A8	F157	C6		
3141	A8	F158	C8		
3147	A3	F161	D12		
3148	A3	F162	D1		
3164	B2	F163	C12		
3165	B2	F165	C12		
3166	D8	F166	C12		
3171	B7	F167	C12		
3172	B7	F168	C12		
3173	C2	F169	D12		
3174	C7	F170	D12		
3176	C7	F171	D12		
3177	C2	F172	D12		
3178	C2	F174	G12		
3179	A7	F175	D8		

DVIO Board: Microprocessor



- 1200 B4
- 1201 G10
- 2200 B4
- 2202 G2
- 2203 G2
- 2204 G3
- 2205 B4
- 2206 C3
- 2207 G10
- 3201 B5
- 3202 B2
- 3203 B3
- 3204 C1
- 3205 B2
- 3206 C2
- 3214 C8
- 3215 C8
- 3216 D8
- 3217 D8
- 3223 G8
- 3224 G9
- 3225 C4
- 3226 E2
- 4206 D4
- 5200 F2
- 6200 H9
- 7201 A10
- 7202 B2
- 7203 B5
- 7204 C3
- 7207 G9
- 7208 C2
- 7209 E2
- F200 B4
- F201 B4
- F202 B3
- F203 D3
- F204 C4
- F205 C6
- F206 C6
- F207 D6
- F208 D6
- F209 C5
- F210 G9
- F211 C5
- F212 F3
- F213 D3
- F214 B4
- F216 G9
- F219 F8
- F220 E2
- F221 G9
- F222 G9
- F223 B2
- F230 D5
- F232 B5

DVIO Board: Fifo & Control

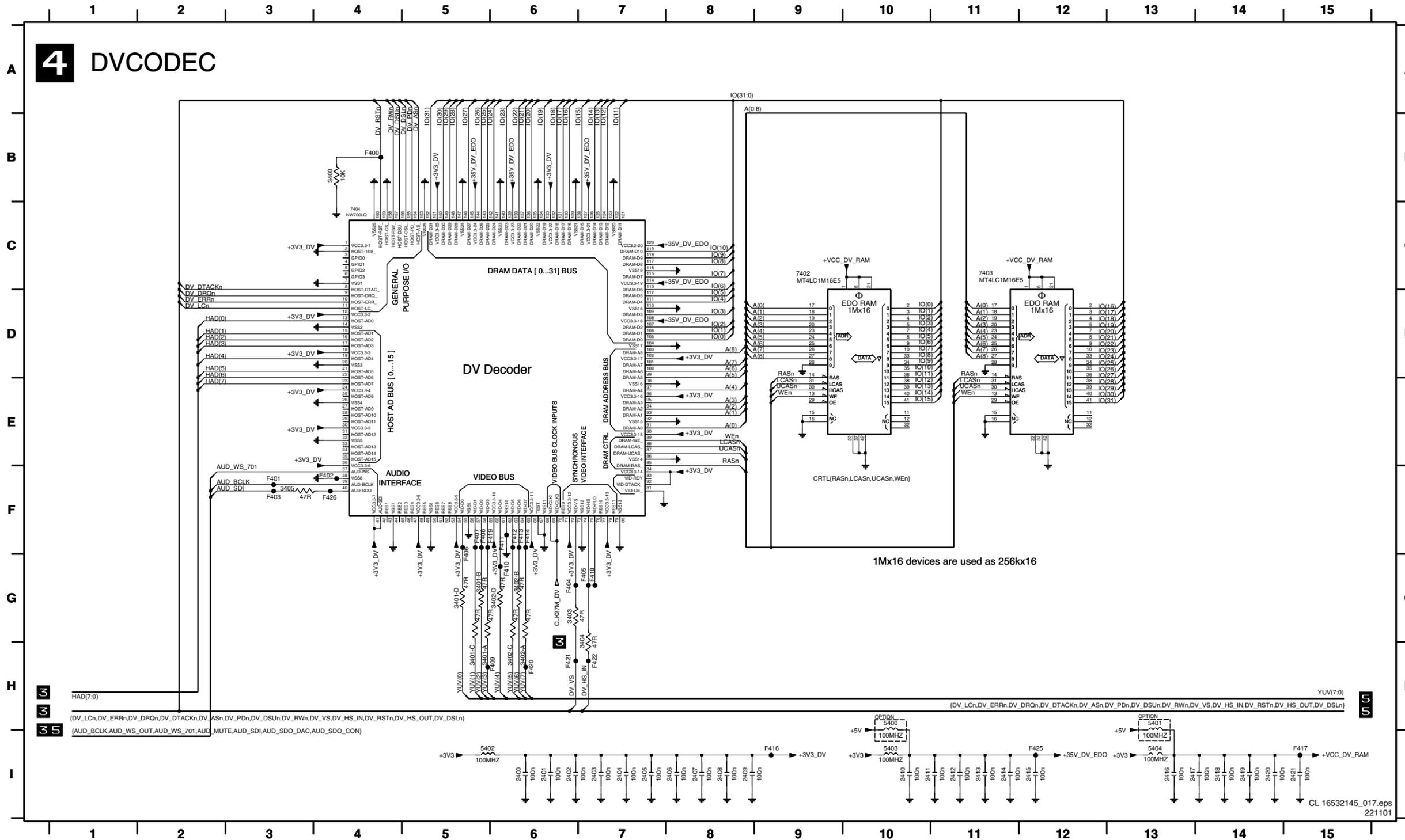


- 2301 I3
- 2302 I4
- 2303 F4
- 2304 C8
- 2305 F3
- 2306 I9
- 2307 I9
- 2308 I9
- 2309 I9
- 2310 I9
- 2311 I10
- 2312 I10
- 2313 I10
- 2314 I8
- 2318 D3
- 2319 D3
- 2324 I12
- 2330 A4
- 2331 B4
- 2332 B4
- 3300 G9
- 3301 B11
- 3303 E12
- 3305 B1
- 3306 B1
- 3307 C1
- 3312 F5
- 3313 H9
- 3314 H9
- 3315 D7
- 3317 G3
- 3318 G3
- 3319 G3
- 3320 D7
- 3321 D7
- 3322 C10
- 3325 D7
- 3327 C9
- 3328 G10
- 3329 G11
- 3330 C8
- 3331 D7
- 4300 B1
- 4301 E4
- 4302 A2
- 5300 C7
- 5301 F2
- 5302 I8
- 5303 A1
- 5304 I12
- 6300 I3
- 7300 D2
- 7301 F13
- 7303 D10
- 7304 F4
- 7307 C7
- 7308 F2
- 7309 A2
- F300 F5
- F301 C8
- F302 C8
- F303 D7
- F304 D7
- F305 G3
- F306 C10
- F307 G3
- F308 G3
- F309 D7
- F310 D7
- F311 I10
- F312 A2
- F313 I12
- F314 C7
- F315 C8
- F316 B2
- F317 F2
- F318 H9
- F319 B2
- F320 H9
- F321 G3
- F322 B2
- F323 G3
- F324 B2
- F325 I4
- F326 B3
- F328 E4
- F329 G3

- F330 D7
- F331 C8
- F332 C8
- F333 E12
- F335 B10
- F336 B8

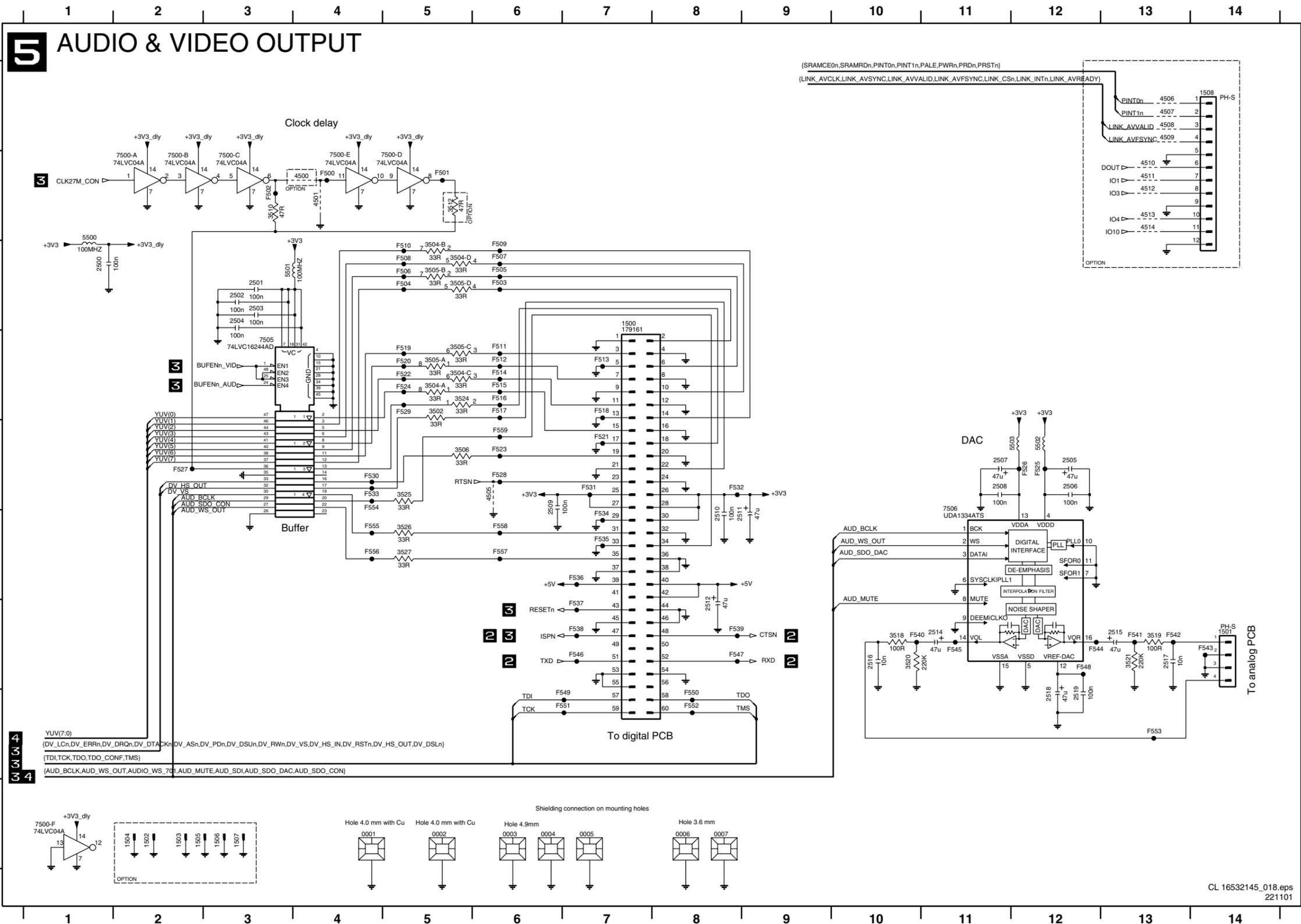
DVIO Board: DVCODEC

4 DVCODEC



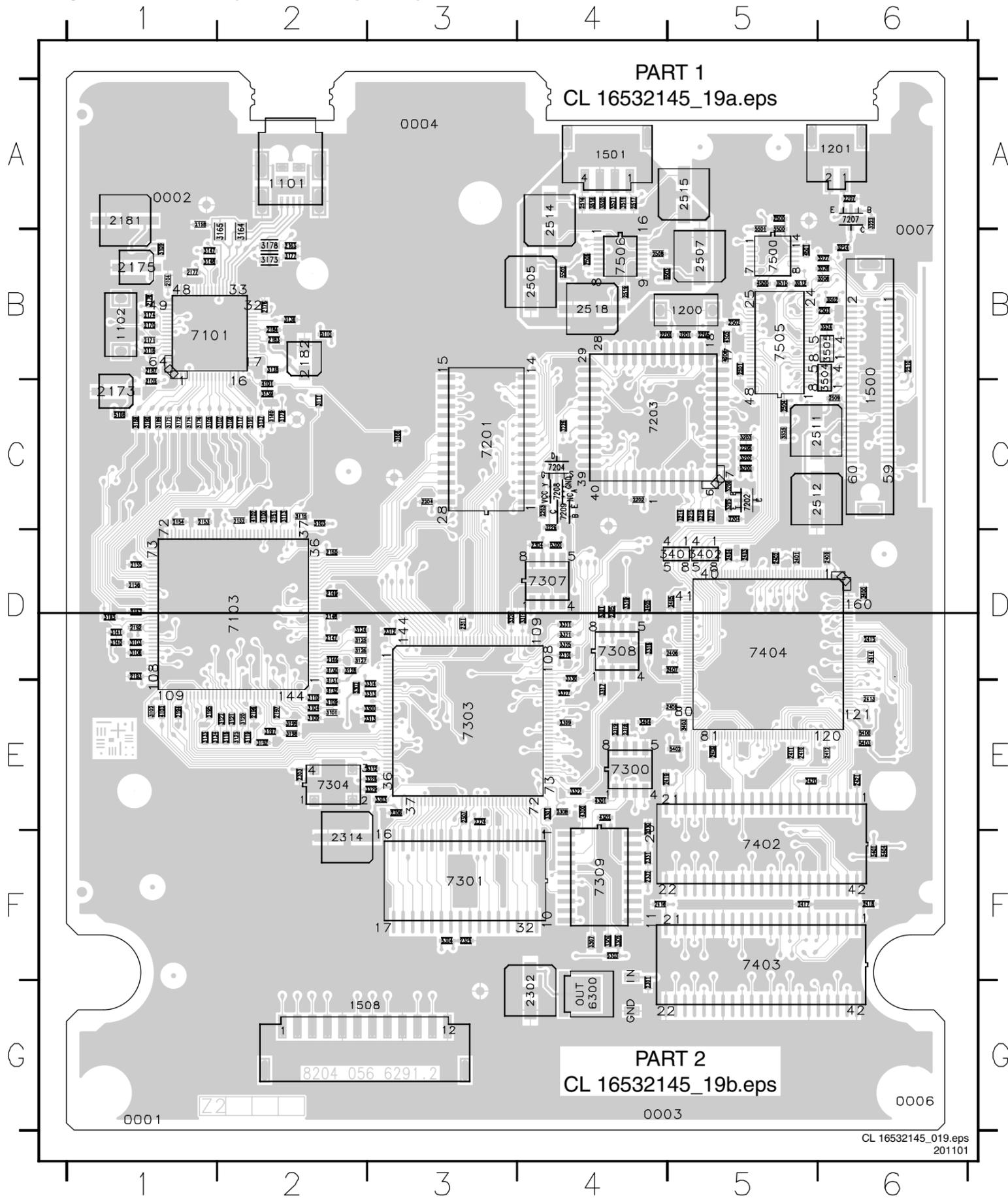
- 2400 I6
- 2401 I6
- 2402 I6
- 2403 I7
- 2404 I7
- 2405 I7
- 2406 I8
- 2407 I8
- 2408 I8
- 2409 I8
- 2410 I10
- 2411 I10
- 2412 I11
- 2413 I11
- 2414 I11
- 2415 I12
- 2416 I13
- 2417 I13
- 2418 I14
- 2419 I14
- 2420 I14
- 2421 I15
- 3400 B4
- 3401-A H5
- 3401-B G5
- 3401-C H5
- 3401-D G5
- 3402-A H6
- 3402-B G6
- 3402-C H6
- 3402-D G6
- 3403 G6
- 3404 G7
- 3405 F3
- 5400 H10
- 5401 H13
- 5402 I5
- 5403 I10
- 5404 I13
- 7402 C9
- 7403 C11
- 7404 C4
- F400 B4
- F401 F3
- F402 F4
- F403 F3
- F404 G6
- F405 G7
- F406 F5
- F407 F5
- F408 F5
- F409 H6
- F410 G6
- F411 F6
- F412 F6
- F413 F6
- F414 F6
- F415 I9
- F416 I9
- F417 I15
- F418 G7
- F419 F6
- F420 H6
- F421 H6
- F422 H7
- F425 I12
- F426 F4

DVIO Board: Audio & Video Output



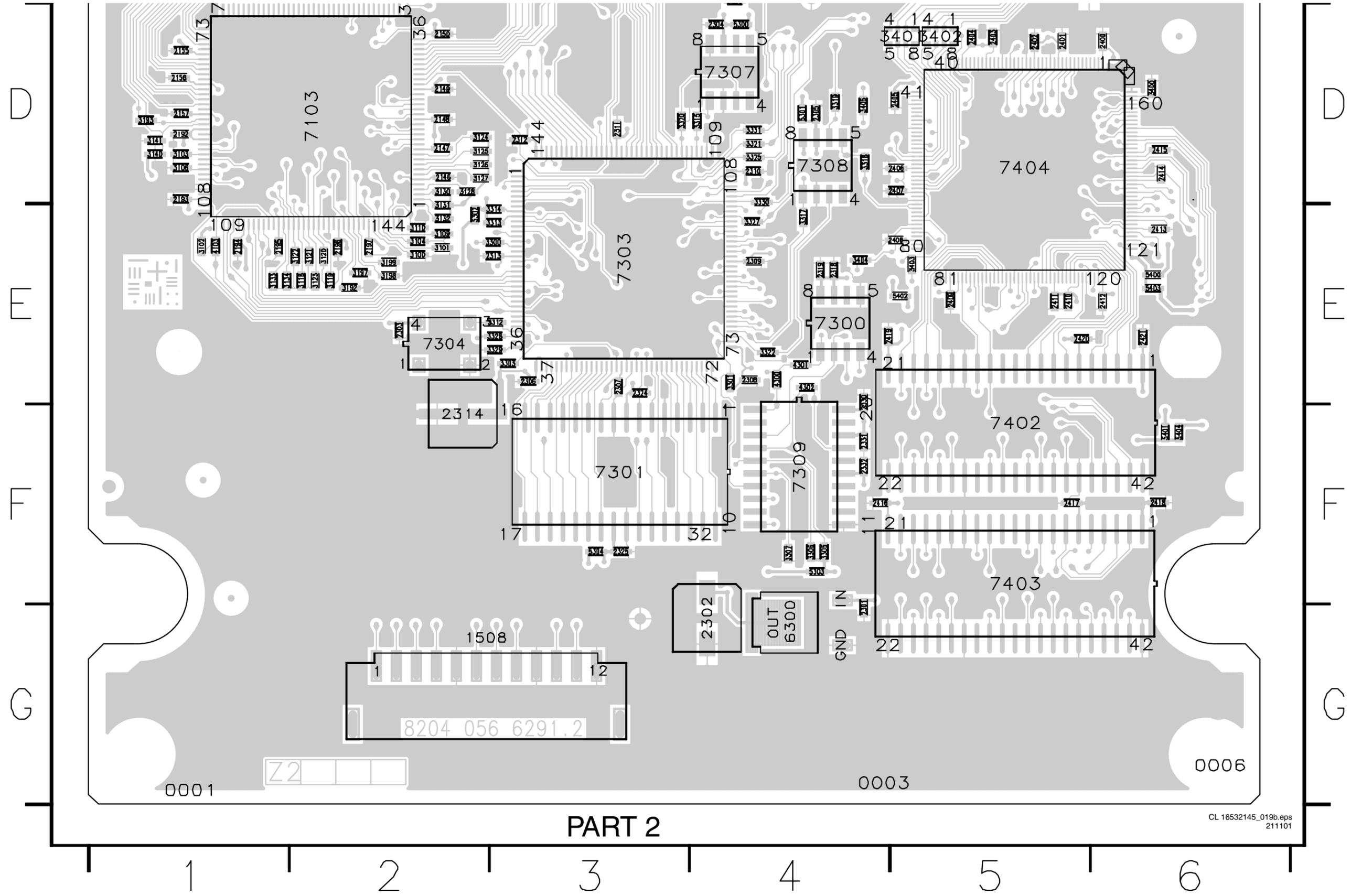
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0003	I6	F511	D6
0004	I6	F512	D6
0005	I7	F513	D7
0006	I8	F514	D6
0007	I8	F515	D6
1500	C7	F516	D6
1501	G14	F517	D6
1502	I2	F518	D7
1503	I2	F519	D5
1504	I2	F520	D5
1505	I2	F521	E7
1506	I3	F522	D5
1507	I3	F523	E6
1508	A14	F524	D5
2500	C1	F525	E12
2501	C3	F526	E12
2502	C3	F527	E2
2503	C3	F528	E6
2504	C3	F529	D5
2505	E12	F530	E4
2506	E12	F531	E7
2507	E11	F532	E8
2508	E11	F533	E4
2509	E6	F534	F7
2510	F8	F535	F7
2511	F8	F536	F7
2512	G8	F537	G7
2514	G11	F538	G7
2515	G13	F539	G8
2516	G10	F540	G10
2517	G13	F541	G13
2518	H12	F542	G13
2519	H12	F543	G14
3502	D5	F544	G12
3504-A	D5	F545	G11
3504-B	C5	F546	G7
3504-C	D5	F547	G8
3504-D	C5	F548	G12
3505-A	D5	F549	H7
3505-B	C5	F550	H8
3505-C	D5	F551	H7
3505-D	C5	F552	H8
3506	E5	F553	H13
3510	B3	F554	E4
3511	B4	F555	F4
3512	B5	F556	F6
3518	G10	F557	F4
3519	G13	F558	F6
3520	G10	F559	E6
3521	G13		
3524	D5		
3525	E5		
3526	F5		
3527	F5		
4500	B4		
4505	E6		
4506	A13		
4507	A13		
4508	A13		
4509	A13		
4510	B13		
4511	B13		
4512	B13		
4513	B13		
4514	B13		
5500	B1		
5501	C3		
5502	E12		
5503	E12		
7500-A	B2		
7500-B	B2		
7500-C	B3		
7500-D	B4		
7500-E	B4		
7500-F	I1		
7505	D3		
7506	F11		
F500	B4		
F501	B5		
F502	B3		
F503	C6		
F504	C5		
F505	C6		
F506	C5		
F507	C6		
F508	C5		

Layout DVIO Board (Overview Top View)



1101 A2	2332 F4	3130 D2	3331 D4	7403 F5
1102 B1	2400 D6	3131 E2	3400 D6	7404 D5
1200 B5	2401 D5	3132 E2	3401 D5	7500 B5
1201 A6	2402 D5	3133 E1	3402 D5	7505 B5
1500 C6	2403 D5	3134 E1	3403 E5	7506 B4
1501 A4	2404 D5	3136 B2	3404 E4	
1508 G2	2405 D5	3137 C2	3405 D4	
2104 B1	2406 D5	3138 B2	3502 B6	
2105 C1	2407 D5	3139 C2	3504 B6	
2146 D2	2408 E5	3140 D1	3505 B6	
2147 D2	2409 E5	3141 D1	3506 B6	
2148 D2	2410 E5	3147 B1	3510 B5	
2149 D2	2411 E5	3148 B1	3512 B5	
2150 D2	2412 E6	3164 B2	3518 A4	
2151 C2	2413 E6	3165 B2	3519 A4	
2152 C2	2414 D6	3166 C3	3520 A4	
2153 C1	2415 D6	3171 C1	3521 A4	
2154 C1	2416 F4	3172 C1	3524 B6	
2155 D1	2417 F5	3173 B2	3525 C5	
2156 D1	2418 F6	3174 C1	3526 B6	
2157 D1	2419 E4	3176 C1	3527 B6	
2158 A1	2420 E5	3177 B2	4100 C2	
2163 B2	2421 E6	3178 B2	4101 C2	
2170 B1	2500 A5	3179 C2	4102 C2	
2171 B1	2501 B5	3180 C2	4103 E1	
2173 C1	2502 B5	3188 C1	4206 B5	
2174 B1	2503 B6	3189 C1	4300 E4	
2175 B1	2504 C5	3190 C1	4301 E4	
2176 B1	2505 B4	3191 C2	4302 E4	
2177 B1	2506 B4	3192 E2	4500 B5	
2178 B2	2507 B5	3193 D1	4501 B5	
2181 A1	2508 B4	3197 E2	4505 B5	
2182 B2	2509 C6	3198 E2	5103 C2	
2183 B2	2510 B6	3199 E2	5106 C1	
2184 B2	2511 C5	3201 B5	5109 B1	
2187 B1	2512 C5	3202 C5	5110 B2	
2192 D1	2514 A4	3203 C5	5200 C5	
2193 D1	2515 A5	3204 C5	5300 D4	
2194 E1	2516 A4	3205 C5	5301 D4	
2195 E1	2517 A4	3206 C5	5302 E2	
2196 E2	2518 B4	3214 C5	5303 F4	
2197 E2	2519 B4	3215 C5	5304 F3	
2200 B4	3100 E2	3216 C5	5400 E6	
2202 C4	3101 E2	3217 C5	5401 F6	
2203 C4	3102 E1	3223 A6	5402 E5	
2204 C3	3103 D1	3224 B6	5403 E6	
2205 B5	3104 E2	3225 C4	5404 F6	
2206 C5	3105 C1	3226 C4	5500 A5	
2207 A6	3106 D1	3300 E3	5501 A5	
2301 G4	3107 C2	3301 E4	5502 B4	
2302 G4	3108 C2	3303 E3	5503 B4	
2303 E2	3109 E2	3305 F4	6300 G4	
2304 D4	3110 E2	3306 F4	7101 B1	
2305 D4	3111 C2	3307 F4	7103 D2	
2306 E3	3113 C2	3312 E3	7201 C3	
2307 E3	3115 C2	3313 E3	7202 C5	
2308 E4	3116 B1	3314 E3	7203 C4	
2309 E4	3117 C2	3315 D4	7204 C4	
2310 D4	3118 E2	3317 E4	7207 A6	
2311 D3	3119 E2	3318 D4	7208 C4	
2312 D3	3120 E2	3319 D4	7209 C4	
2313 E3	3121 E2	3320 D3	7300 E4	
2314 F2	3122 E2	3321 D4	7301 F3	
2318 E4	3123 E2	3322 E4	7303 E3	
2319 E4	3124 D2	3325 D4	7304 E2	
2324 E3	3125 D2	3327 E4	7307 D4	
2325 F3	3126 D2	3328 E3	7308 D4	
2330 E4	3127 D2	3329 E3	7309 F4	
2331 F4	3128 D2	3330 D4	7402 F5	

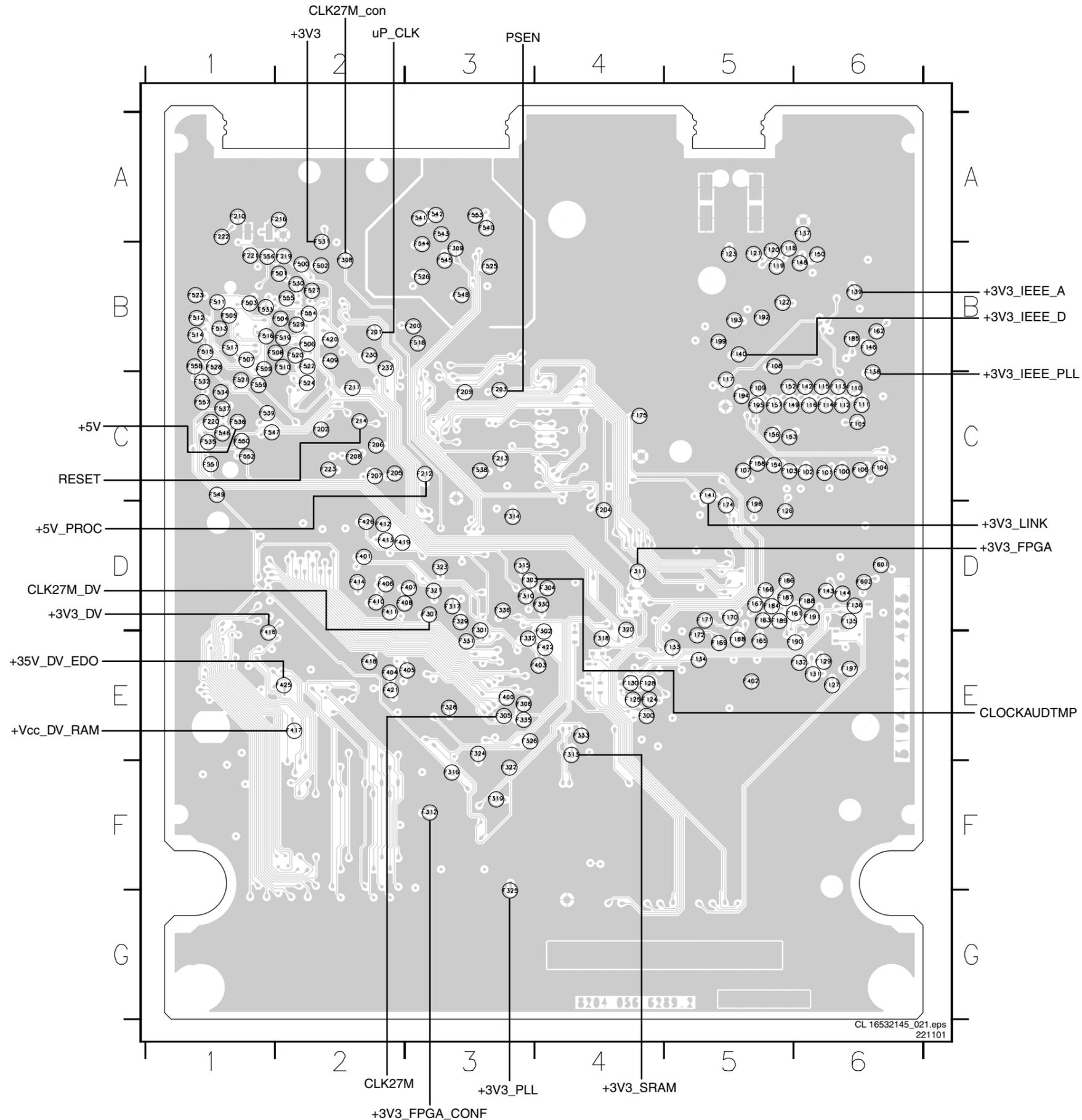
Layout DVIO Board (Part 2 Top View)



PART 2

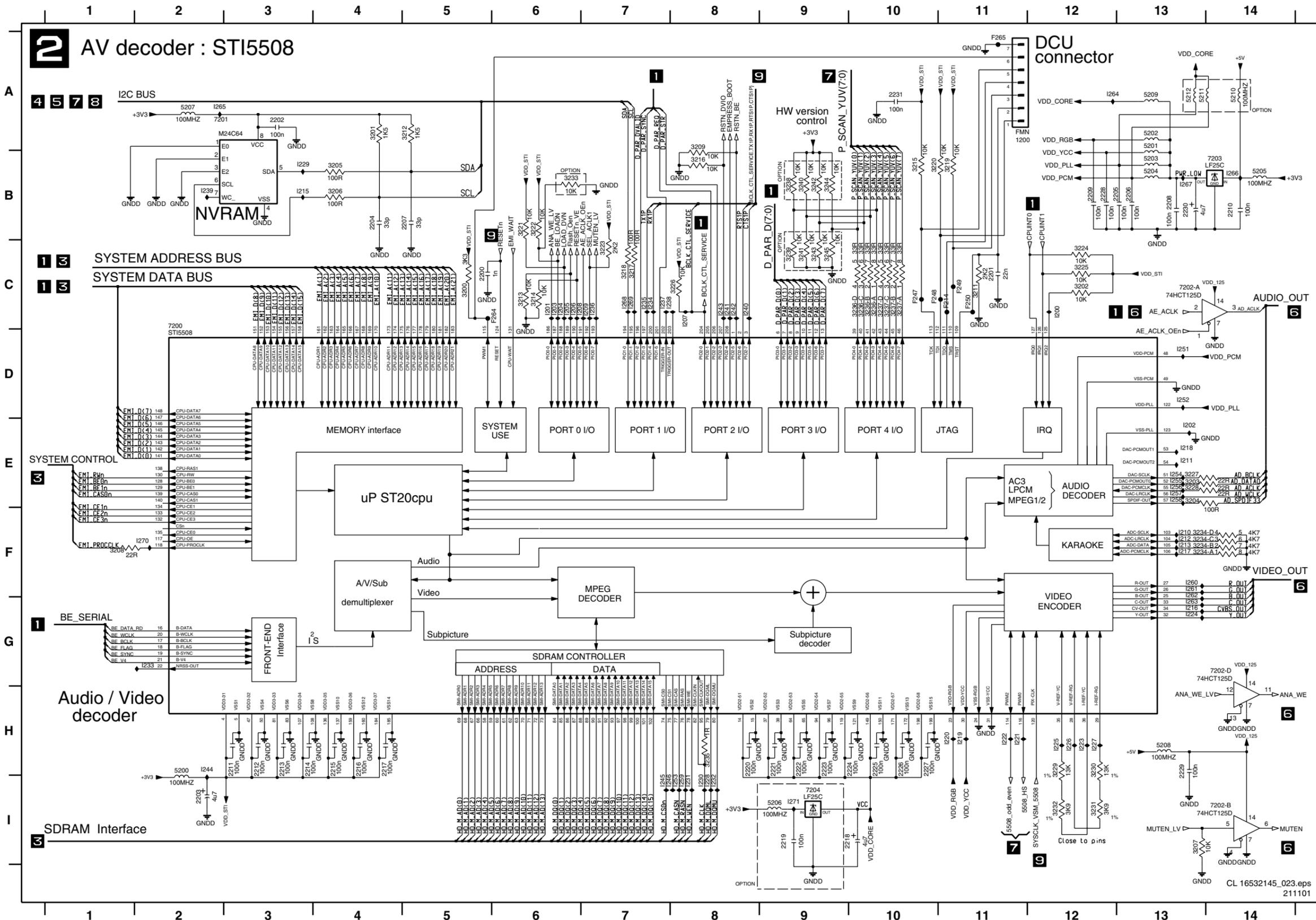
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Layout DVIO Board (Testlands Bottom View)



F100	C6	F144	D6	F206	C2	F328	E3	F513	B1
F100	C6	F146	B6	F206	C2	F329	D3	F513	B1
F101	C6	F146	B6	F207	C2	F329	D3	F514	B1
F101	C6	F148	B6	F207	C2	F330	D4	F514	B1
F102	C6	F148	B6	F208	C2	F330	D4	F515	B1
F102	C6	F149	C5	F208	C2	F331	E3	F515	B1
F103	C5	F149	C5	F209	C3	F331	E3	F516	B1
F103	C5	F150	B6	F209	C3	F332	E3	F516	B1
F104	C6	F150	B6	F210	A1	F332	E3	F517	B1
F104	C6	F152	C5	F210	A1	F333	E4	F517	B1
F105	C6	F152	C5	F211	C2	F333	E4	F518	B3
F105	C6	F153	C5	F211	C2	F335	E3	F518	B3
F106	C6	F153	C5	F212	C3	F335	E3	F519	B2
F106	C6	F154	C5	F212	C3	F336	D3	F519	B2
F107	C5	F154	C5	F213	C3	F336	D3	F520	B2
F107	C5	F156	C5	F213	C3	F400	E3	F520	B2
F108	B5	F156	C5	F214	C2	F400	E3	F521	C1
F108	B5	F157	C5	F214	C2	F401	D2	F521	C1
F109	C5	F157	C5	F216	A2	F401	D2	F522	B2
F109	C5	F158	C5	F216	A2	F402	E5	F522	B2
F109	C6	F158	C5	F219	B2	F402	E5	F523	B1
F110	C6	F161	D6	F219	B2	F403	E4	F523	B1
F111	C6	F161	D6	F220	C1	F403	E4	F524	C2
F111	C6	F162	B6	F220	C1	F404	E2	F524	C2
F112	C6	F162	B6	F221	B1	F404	E2	F525	B3
F112	C6	F163	D5	F221	B1	F405	E3	F525	B3
F113	C6	F163	D5	F222	A1	F405	E3	F526	B3
F113	C6	F165	E5	F222	A1	F406	D2	F526	B3
F114	C6	F165	E5	F223	C2	F406	D2	F527	B2
F114	C6	F166	D5	F223	C2	F407	D3	F527	B2
F115	C6	F166	D5	F230	B2	F407	D3	F528	B1
F115	C6	F167	D5	F230	B2	F408	D2	F528	B1
F116	C6	F167	D5	F232	B2	F408	D2	F529	B2
F116	C6	F168	E5	F232	B2	F409	B2	F529	B2
F117	C5	F168	E5	F300	E4	F409	B2	F530	B2
F117	C5	F169	E5	F300	E4	F410	D2	F530	B2
F118	B5	F169	E5	F301	D3	F410	D2	F531	A2
F118	B5	F170	D5	F301	D3	F411	D2	F531	B2
F119	B5	F170	D5	F302	E4	F411	D2	F532	C1
F119	B5	F171	D5	F302	E4	F412	D2	F532	C1
F120	B5	F171	D5	F303	D3	F412	D2	F533	B1
F120	B5	F172	E5	F303	D3	F413	D2	F533	B1
F121	B5	F172	E5	F304	D4	F413	D2	F534	C1
F121	B5	F174	D5	F304	D4	F414	D2	F534	C1
F122	B5	F174	D5	F305	E3	F414	D2	F535	C1
F122	B5	F175	C4	F305	E3	F416	E1	F535	C1
F123	B5	F175	C4	F306	E3	F416	E1	F536	C1
F123	B5	F184	D5	F306	E3	F417	E2	F536	C1
F124	E4	F184	D5	F307	D3	F417	E2	F537	C1
F124	E4	F185	B6	F307	D3	F418	E2	F537	C1
F125	E4	F185	B6	F308	B2	F418	E2	F538	C3
F125	E4	F186	D5	F308	B2	F419	D2	F538	C3
F126	D5	F186	D5	F309	B3	F419	D2	F539	C1
F126	D5	F187	D5	F309	B3	F420	B2	F539	C1
F127	E6	F187	D5	F310	D3	F420	B2	F540	A3
F127	E6	F188	D6	F310	D3	F421	E2	F540	A3
F128	E4	F188	D6	F311	D4	F421	E2	F541	A3
F128	E4	F189	D5	F311	D4	F422	E4	F541	A3
F129	E6	F189	D5	F312	F3	F422	E4	F542	A3
F129	E6	F190	E6	F312	F3	F425	E2	F542	A3
F130	E4	F190	E6	F313	E4	F425	E2	F543	A3
F130	E4	F191	D6	F313	E4	F426	D2	F543	A3
F131	E6	F191	D6	F314	D3	F426	D2	F544	B3
F131	E6	F192	B5	F314	D3	F500	B2	F544	B3
F132	E6	F192	B5	F315	D3	F500	B2	F545	B3
F132	E6	F193	B5	F315	D3	F501	B2	F545	B3
F133	E5	F193	B5	F316	F3	F501	B2	F546	C1
F133	E5	F194	C5	F316	F3	F502	B2	F546	C1
F134	E5	F194	C5	F317	D3	F502	B2	F547	C1
F134	E5	F195	C5	F317	D3	F503	B1	F547	C1
F135	D6	F195	C5	F318	E4	F503	B1	F548	B3
F135	D6	F197	E6	F318	E4	F504	B2	F548	B3
F136	D6	F197	E6	F319	F3	F504	B2	F549	C1
F136	D6	F198	D5	F319	F3	F505	B1	F549	C1
F137	A6	F198	D5	F320	D4	F505	B1	F550	C1
F137	A6	F199	B5	F320	D4	F506	B2	F550	C1
F138	C6	F199	B5	F321	D3	F506	B2	F551	C1
F138	C6	F200	B3	F321	D3	F507	B1	F551	C1
F139	B6	F200	B3	F322	F3	F507	B1	F552	C1
F139	B6	F201	B2	F322	F3	F508	B2	F552	C1
F140	B5	F201	B2	F323	D3	F508	B2	F553	A3
F140	B5	F202	C2	F323	D3	F509	B1	F553	A3
F141	C5	F202	C2	F324	E3	F509	B1	F554	B2
F141	C5	F203	C3	F324	E3	F510	B2	F554	B2
F142	C6	F203	C3	F325	G3	F510	B2	F555	B2
F142	C6	F204	D4	F325	G3	F511	B1	F555	B2
F143	D6	F204	D4	F326	E3	F511	B1	F556	B1
F143	D6	F205	C2	F326	E3	F512	B1	F556	B1
F144	D6	F205	C2	F328	E3	F512	B1	F557	C1

Digital Board: AV Decoder STI5508

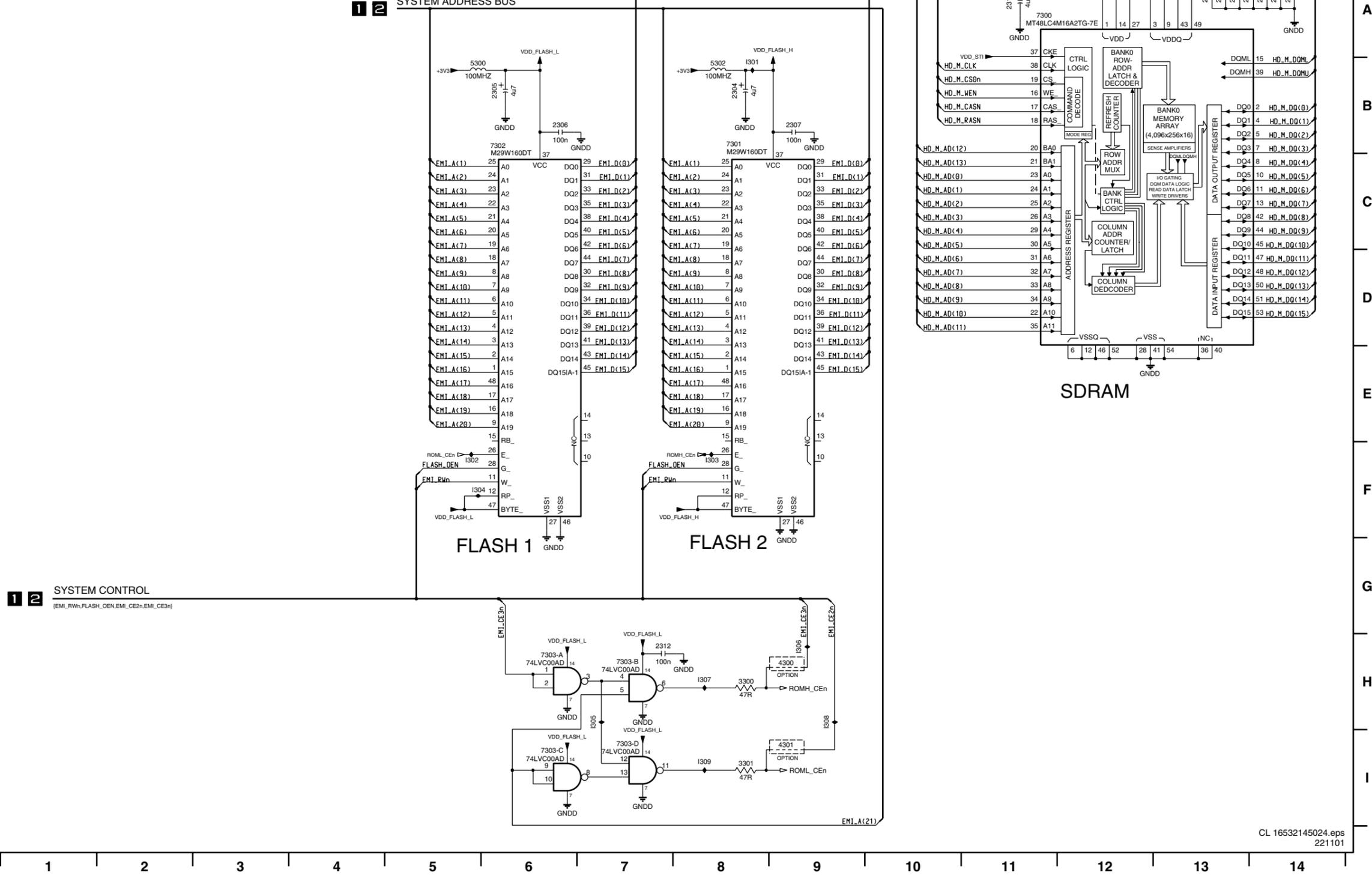


1200	A11	5207	A2
2200	C5	5208	H13
2201	C11	5209	A13
2202	A3	5210	A14
2203	I2	5211	A13
2204	B4	5212	A13
2205	B13	7200	C2
2206	B13	7201	A2
2207	B5	7202-A	C13
2208	B13	7202-B	I14
2209	B12	7202-D	G14
2210	B14	7203	B14
2211	H3	7204	I9
2212	H3	F214	C11
2213	H3	F247	C10
2214	H3	F248	C10
2215	H4	F249	C11
2216	H4	F250	C11
2217	H4	F264	C6
2218	I10	F265	A11
2219	I9		
2220	H8		
2221	H9		
2222	H9		
2223	H9		
2224	H10		
2225	H10		
2226	H10		
2227	H10		
2228	B12		
2229	H13		
2230	B13		
2231	A10		
3200	C5		
3201	A4		
3202	C12		
3203	E13		
3204	E13		
3205	B4		
3206	B4		
3207	I13		
3208	F1		
3209	A8		
3211	C11		
3212	A5		
3213	C6		
3214	C6		
3215	B10		
3216	B8		
3217	C7		
3218	C7		
3219	B11		
3220	B10		
3221	B6		
3222	B6		
3223	C7		
3224	C12		
3225	C12		
3226	C8		
3227	E13		
3228	E13		
3229	H12		
3230	H12		
3231	I12		
3232	I12		
3233	B6		
3234-A	F13		
3234-B	F13		
3234-C	F13		
3234-D	F13		
3235	H8		
3236-A	C10		
3236-B	C10		
3236-C	C10		
3236-D	C10		
3237-A	C10		
3237-B	C10		
3237-C	C10		
3237-D	C10		
3238	B9		
3239	C9		
3240	B9		
3241	C9		
3242	B9		
3243	C9		
3244	B9		
3245	C9		
5200	H2		
5201	A13		
5202	A13		
5203	B13		
5204	B13		
5205	B14		
5206	I9		

Digital Board: AV Decoder Memory

3 AV Decoder Memory

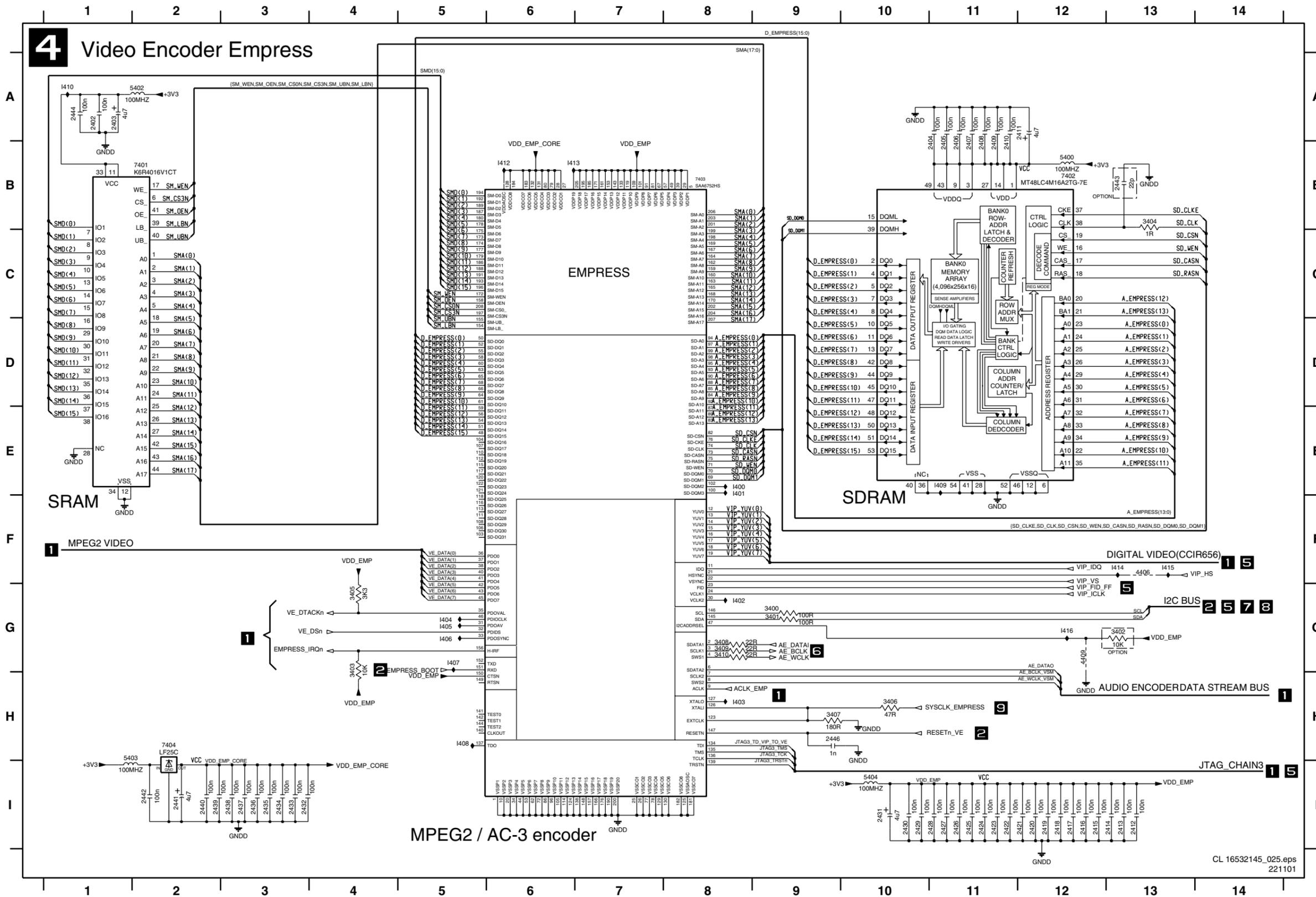
- 2** SDRAM Interface
- 1 2** SYSTEM DATA BUS
- 1 2** SYSTEM ADDRESS BUS



- 2300 A14
- 2301 A14
- 2302 A14
- 2303 A13
- 2304 B8
- 2305 B6
- 2306 B6
- 2307 B9
- 2308 A13
- 2309 A13
- 2310 A13
- 2311 A11
- 2312 H7
- 3300 H8
- 3301 I8
- 4300 H9
- 4301 I9
- 5300 B5
- 5302 B8
- 7300 A11
- 7301 B8
- 7302 B6
- 7303-A H6
- 7303-B H7
- 7303-C I6
- 7303-D I7

Digital Board: Video Encoder, Empress

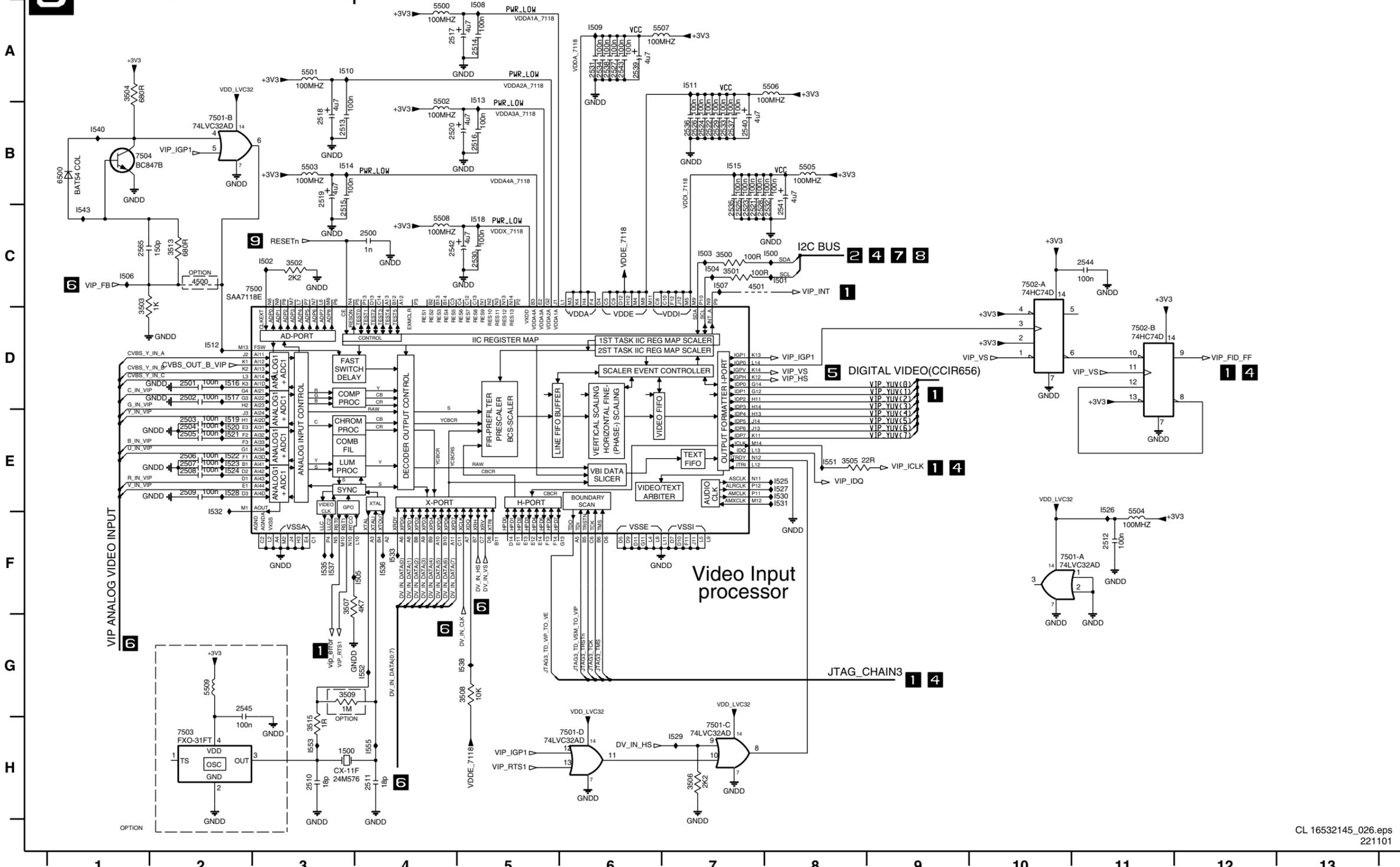
4 Video Encoder Empress



- 2402 A1
- 2403 A1
- 2404 B11
- 2405 B11
- 2406 B11
- 2407 B11
- 2408 B11
- 2409 B11
- 2410 B11
- 2411 A12
- 2412 I13
- 2413 I13
- 2414 I13
- 2415 I12
- 2416 I12
- 2417 I12
- 2418 I12
- 2419 I12
- 2420 I12
- 2421 I12
- 2422 I11
- 2423 I11
- 2424 I11
- 2425 I11
- 2426 I11
- 2427 I11
- 2428 I10
- 2429 I10
- 2430 I10
- 2431 I10
- 2432 I3
- 2433 I3
- 2434 I3
- 2435 I3
- 2436 I3
- 2437 I3
- 2438 I3
- 2439 I2
- 2440 I2
- 2441 I2
- 2442 I2
- 2443 B13
- 2444 A1
- 2446 H9
- 3400 G9
- 3401 G9
- 3402 G13
- 3403 G4
- 3404 B13
- 3405 G4
- 3406 H10
- 3407 H9
- 3408 G8
- 3409 G8
- 3410 G8
- 4406 F13
- 4409 G12
- 5400 B12
- 5402 A2
- 5403 H1
- 5404 I10
- 7401 B2
- 7402 B12
- 7403 B8
- 7404 H2

Digital Board: VIP CVBS Y/C Video Input

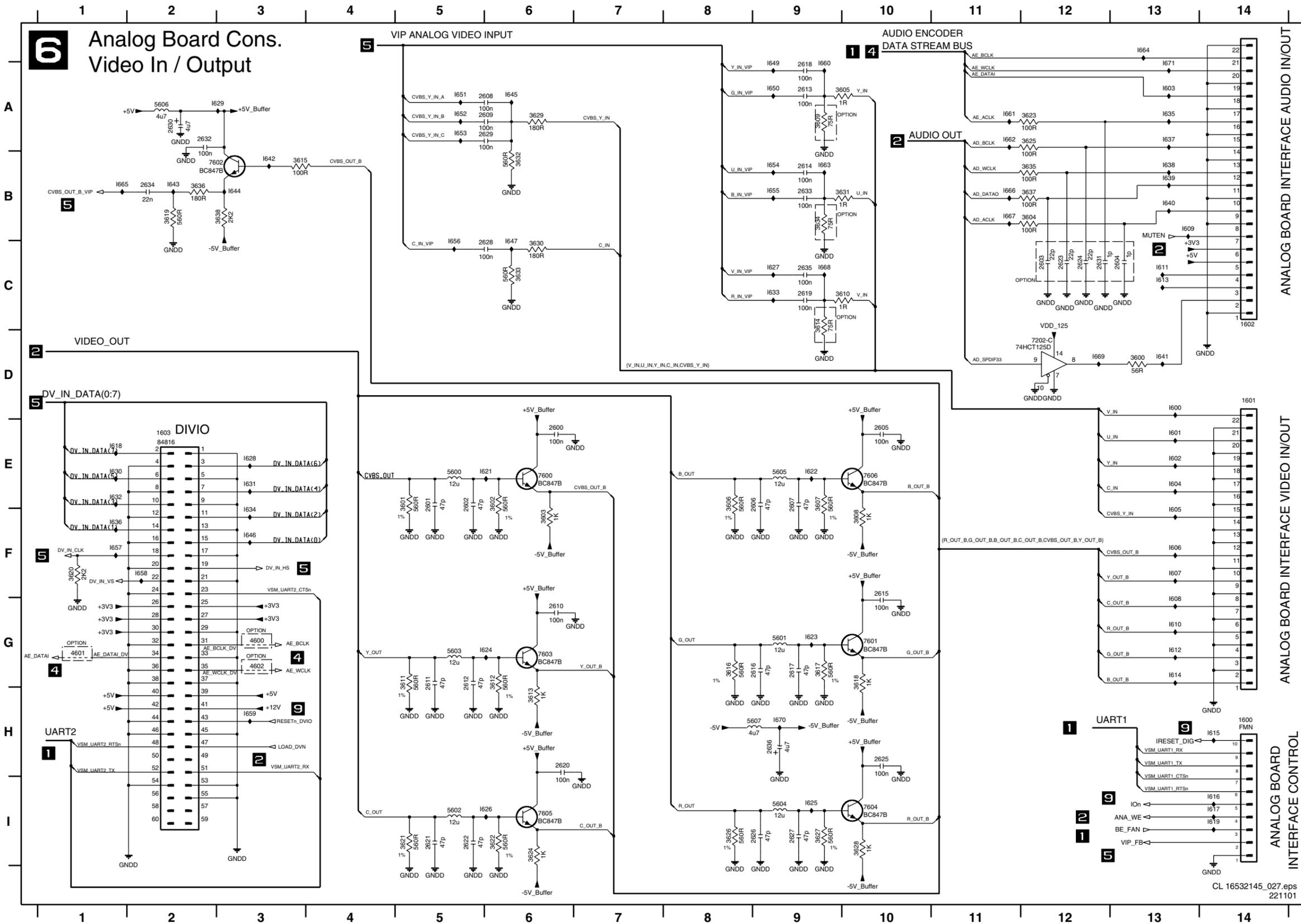
5 VIP CVBS Y/C Video Input



- 1500 H3
- 2500 C4
- 2501 D2
- 2502 D2
- 2503 E2
- 2504 E2
- 2505 E2
- 2506 E2
- 2507 E2
- 2508 E2
- 2509 E2
- 2510 H3
- 2511 H4
- 2512 F11
- 2513 B3
- 2514 A5
- 2515 C3
- 2516 B5
- 2517 A4
- 2518 B3
- 2519 B3
- 2520 B4
- 2521 C7
- 2522 B7
- 2523 C7
- 2524 B7
- 2525 C7
- 2526 B7
- 2527 A6
- 2528 C7
- 2529 B7
- 2530 C5
- 2531 A6
- 2532 C8
- 2533 B7
- 2534 A6
- 2535 C7
- 2536 B7
- 2537 B7
- 2538 A6
- 2539 A6
- 2540 B7
- 2541 B8
- 2542 C4
- 2543 A6
- 2544 C11
- 2545 G2
- 2546 C1
- 2547 C7
- 2548 C3
- 2549 C1
- 2550 E8
- 2551 H7
- 2552 F3
- 2553 H3
- 2554 C2
- 2555 C7
- 2556 A4
- 2557 A4
- 2558 B3
- 2559 E11
- 2560 B8
- 2561 A8
- 2562 A6
- 2563 C4
- 2564 G2
- 2565 G2
- 2566 B1
- 2567 C3
- 2568 F11
- 2569 B2
- 2570 C7
- 2571 H6
- 2572 C10
- 2573 D11
- 2574 H2
- 2575 B1

Digital Board: Analog Board Cons. Video In / Output

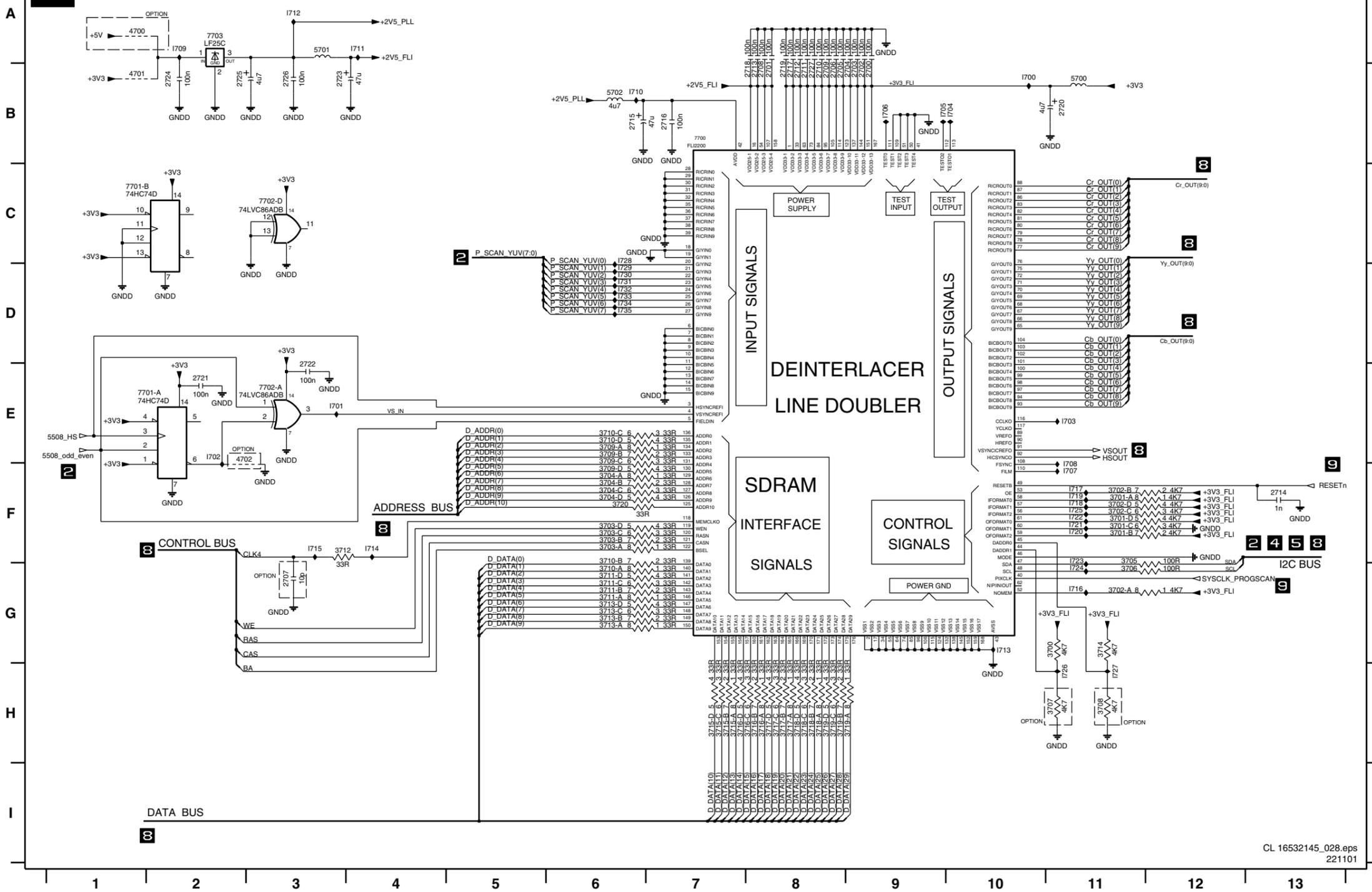
6 Analog Board Cons. Video In / Output



Pin	Signal	Component
1600	H14	7202-C D12
1601	D14	7600 E6
1602	C14	7601 G10
1603	E2	7602 B3
2600	E6	7603 G6
2601	E5	7604 I10
2602	E5	7605 I6
2603	C12	7606 E10
2604	C13	
2605	E10	
2606	E9	
2607	E9	
2608	A6	
2609	A6	
2610	G6	
2611	G5	
2612	G5	
2613	A9	
2614	B9	
2615	F10	
2616	G9	
2617	G9	
2618	A9	
2619	C9	
2620	H6	
2621	I5	
2622	I5	
2623	C12	
2624	C12	
2625	H10	
2626	I9	
2627	I9	
2628	C6	
2629	A6	
2630	A2	
2631	C12	
2632	A2	
2633	B9	
2634	B2	
2635	C9	
2636	H9	
2637	H9	
3600	D13	
3601	E5	
3602	E6	
3603	F6	
3604	B12	
3605	A10	
3606	E8	
3607	E9	
3608	F10	
3609	A9	
3610	C10	
3611	G5	
3612	G6	
3613	H6	
3614	C9	
3615	B3	
3616	G8	
3617	G9	
3618	G10	
3619	B2	
3620	F1	
3621	I5	
3622	I6	
3623	A12	
3624	I6	
3625	A12	
3626	I8	
3627	I9	
3628	I10	
3629	A6	
3630	C6	
3631	B10	
3632	B6	
3633	C6	
3634	B9	
3635	B12	
3636	B2	
3637	B12	
3638	B3	
4600	G3	
4601	G1	
4602	G3	
5600	E5	
5601	G9	
5602	I5	
5603	G5	
5604	I9	
5605	E9	
5606	A2	
5607	H9	

Digital Board: Progressive Scan

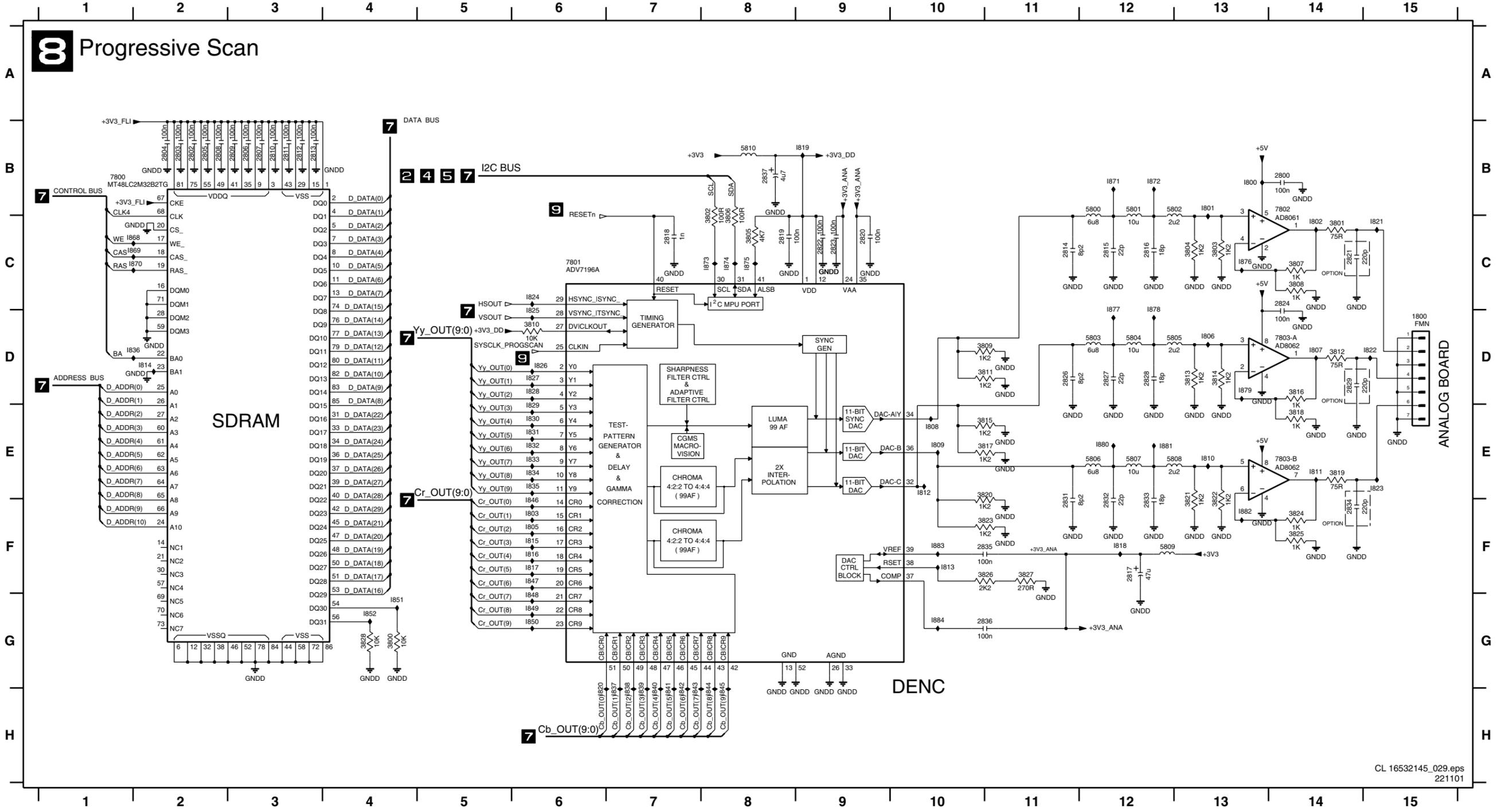
7 Progressive Scan



- 2700 B9
- 2701 B8
- 2702 B9
- 2703 B9
- 2704 B9
- 2705 B8
- 2706 B8
- 2707 G3
- 2708 B8
- 2709 B8
- 2710 B8
- 2711 B8
- 2712 B8
- 2713 B8
- 2714 F13
- 2715 B6
- 2716 B7
- 2717 B8
- 2718 B8
- 2719 B8
- 2720 B11
- 2721 E2
- 2722 E3
- 2723 B3
- 2724 B2
- 2725 B2
- 2726 B3
- 2727 B8
- 3700 G11
- 3701-A F11
- 3701-B F11
- 3701-C F11
- 3701-D F11
- 3702-A G11
- 3702-B F11
- 3702-C F11
- 3702-D F11
- 3703-A F6
- 3703-B F6
- 3703-C F6
- 3703-D F6
- 3704-A F6
- 3704-B F6
- 3704-C F6
- 3704-D F6
- 3705 G11
- 3706 G11
- 3707 H11
- 3708 H11
- 3709-A E6
- 3709-B E6
- 3709-C F6
- 3709-D F6
- 3710-A G6
- 3710-B G6
- 3710-C E6
- 3710-D E6
- 3711-A G6
- 3711-B G6
- 3711-C G6
- 3711-D G6
- 3712 F3
- 3713-A G6
- 3713-B G6
- 3713-C G6
- 3713-D G6
- 3714 G11
- 3715-A H7
- 3715-B H7
- 3715-C H7
- 3715-D H7
- 3716-A H8
- 3716-B H8
- 3716-C H8
- 3716-D H7
- 3717-A H8
- 3717-B H8
- 3717-C H8
- 3717-D H8
- 3718-A H8
- 3718-B H8
- 3718-C H8
- 3718-D H8
- 3719-A H9
- 3719-B H8
- 3719-C H8
- 3719-D H8
- 3720 F6
- 4700 A1
- 4701 B1
- 4702 E2
- 5700 B11
- 5701 A3
- 5702 B6
- 7700 B7
- 7701-A E1
- 7701-B C1
- 7702-A E3
- 7702-D C3
- 7703 A2

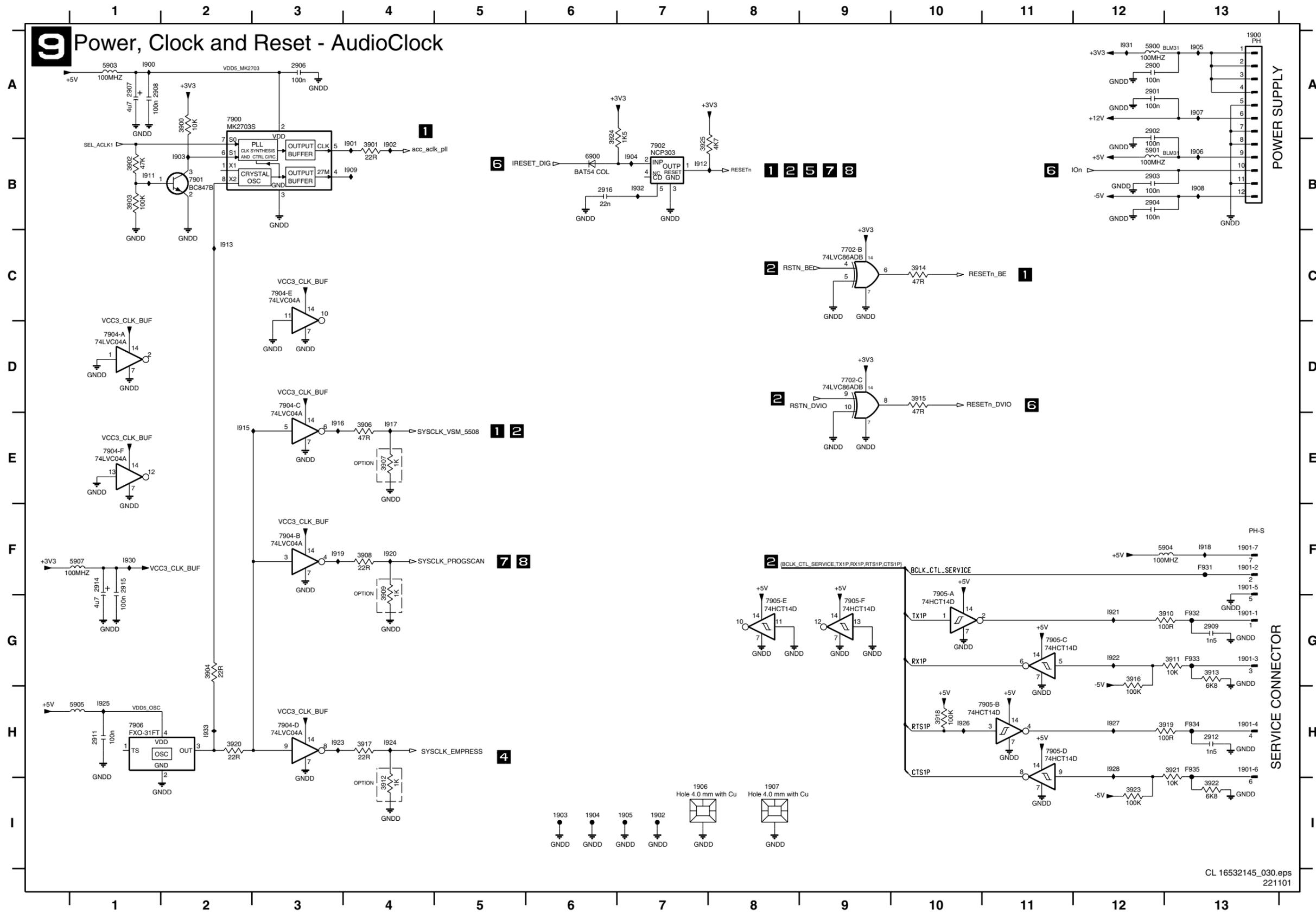
Digital Board: Progressive Scan

1800	D15	2806	B3	2812	B3	2818	C7	2824	C14	2832	E12	3800	G4	3806	B8	3812	D14	3818	E14	3824	F14	5801	B12	5807	E12	7802	B14
2800	B14	2807	B3	2813	B3	2819	C8	2826	D11	2833	E12	3801	C14	3807	C14	3813	D13	3819	E14	3825	F14	5802	B12	5808	E12	7803-A	D14
2802	B2	2808	B2	2814	C11	2820	C9	2827	D12	2834	F14	3802	B8	3808	C14	3814	D13	3820	E10	3826	F11	5803	D12	5809	F12	7803-B	E14
2803	B2	2809	B3	2815	C12	2821	C14	2828	D12	2835	F10	3803	C13	3809	D10	3815	E10	3821	E13	3827	F11	5804	D12	5810	B8		
2804	B2	2810	B3	2816	C12	2822	C9	2829	D14	2836	G10	3804	C13	3810	D6	3816	D14	3822	E13	3828	G4	5805	D12	7800	B1		
2805	B2	2811	B3	2817	F12	2823	C9	2831	E11	2837	B8	3805	C8	3811	D11	3817	E11	3823	F11	5800	B12	5806	E12	7801	C6		



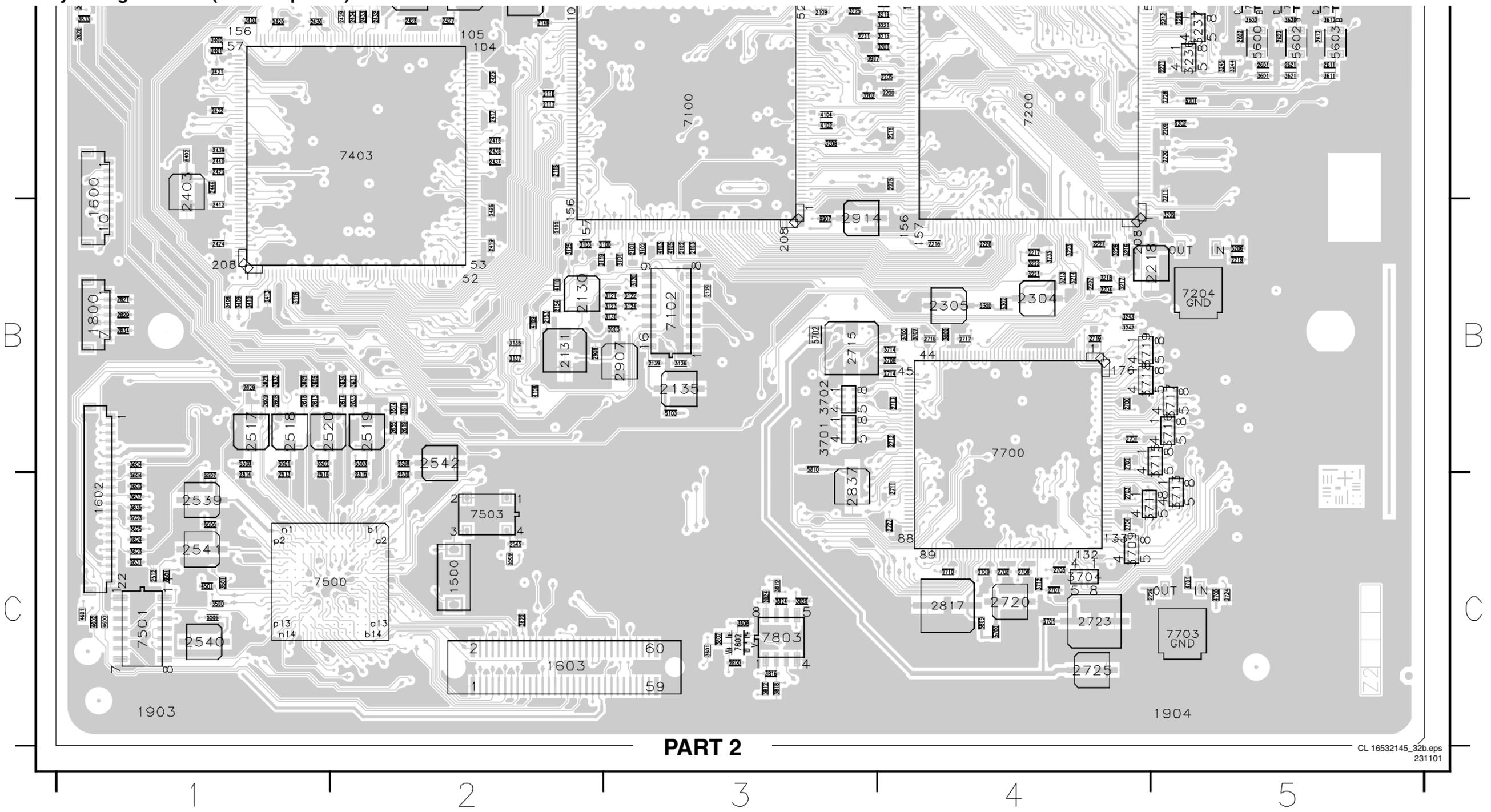
Digital Board: Power, Clock, and Reset Audio Clock

9 Power, Clock and Reset - AudioClock



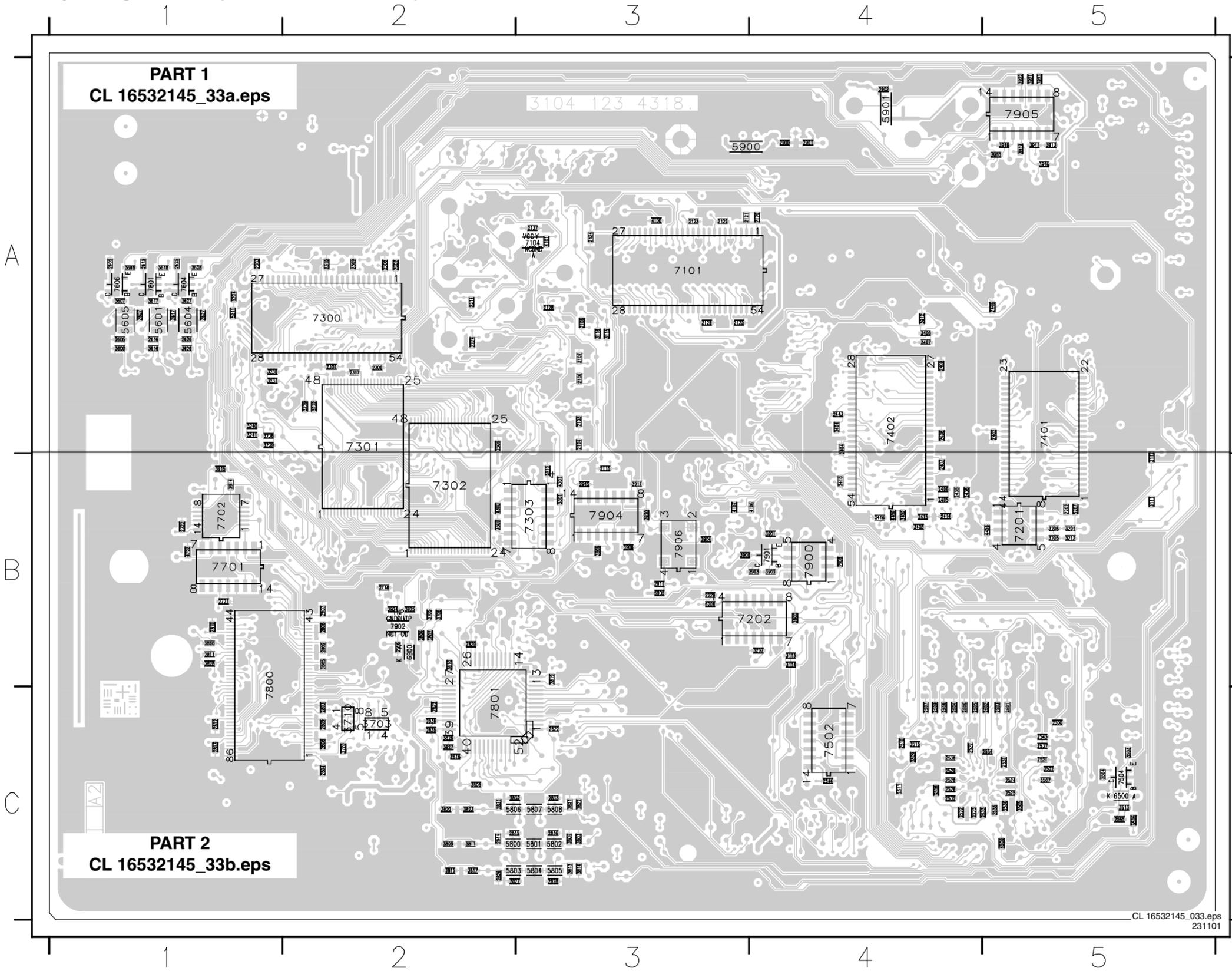
1900	A13
1901-1	G13
1901-2	F13
1901-3	G13
1901-4	H13
1901-5	F13
1901-6	H13
1901-7	F13
1902	I7
1903	I6
1904	I6
1905	I7
1906	I7
1907	I8
1908	A12
1909	A12
1910	A12
1911	B12
1912	B12
1913	B12
1914	A3
1915	A1
1916	A1
1917	G13
1918	H1
1919	H13
1920	F1
1921	F1
1922	B6
1923	A2
1924	B4
1925	B1
1926	B1
1927	G2
1928	E4
1929	E4
1930	F4
1931	F4
1932	G13
1933	G13
1934	C10
1935	D10
1936	G12
1937	H4
1938	H10
1939	H13
1940	H2
1941	H13
1942	I13
1943	I12
1944	A6
1945	B7
1946	A12
1947	B12
1948	A1
1949	F13
1950	H1
1951	H1
1952	B6
1953	C9
1954	D9
1955	A2
1956	B2
1957	B7
1958	D1
1959	F3
1960	D3
1961	H3
1962	C3
1963	E1
1964	G10
1965	H10
1966	G11
1967	H11
1968	G8
1969	G9
1970	H1
1971	F13
1972	G13
1973	G13
1974	H13
1975	H13

Layout Digital Board (Part 2 Top View)



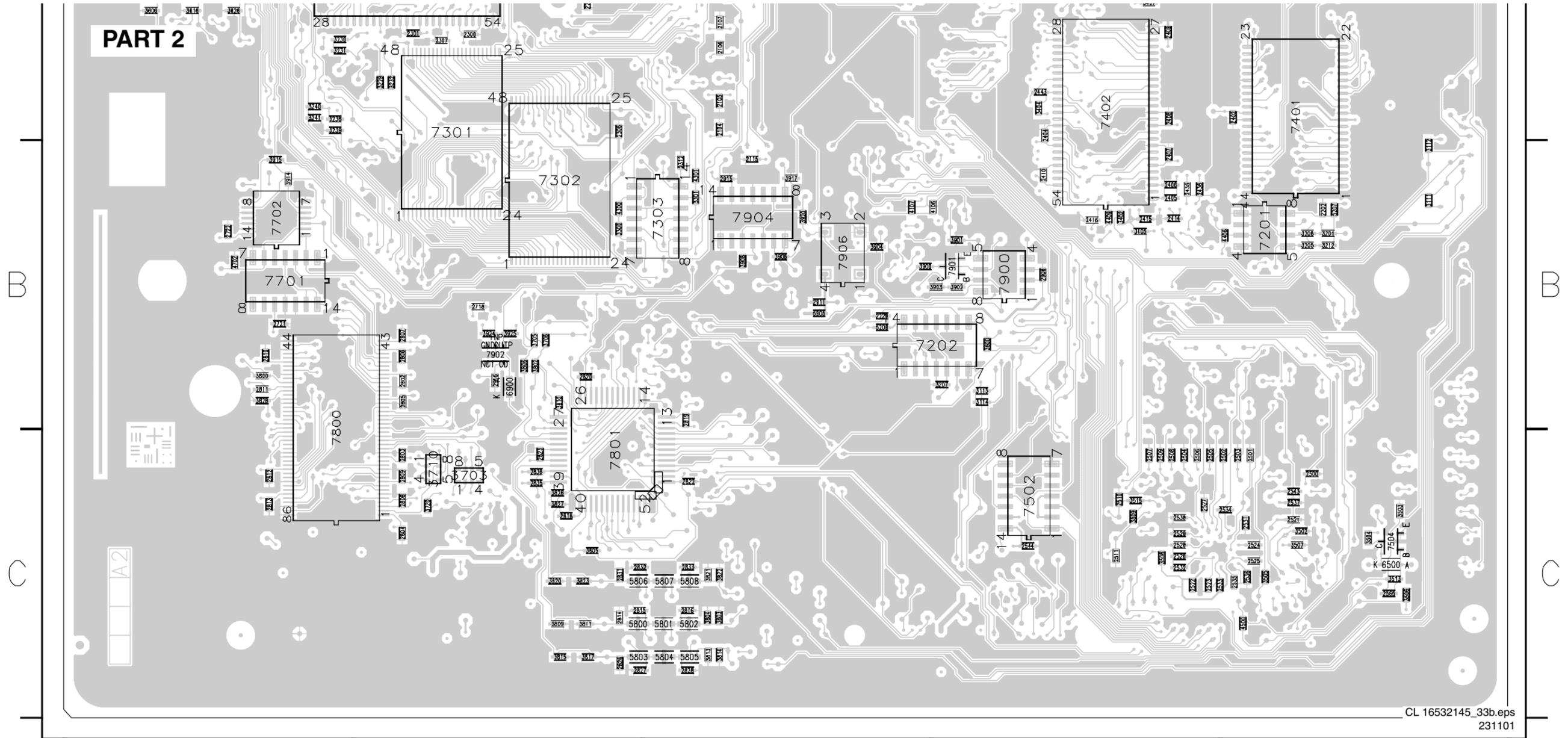
PART 2

Layout Digital Board (Overview Bottom View)

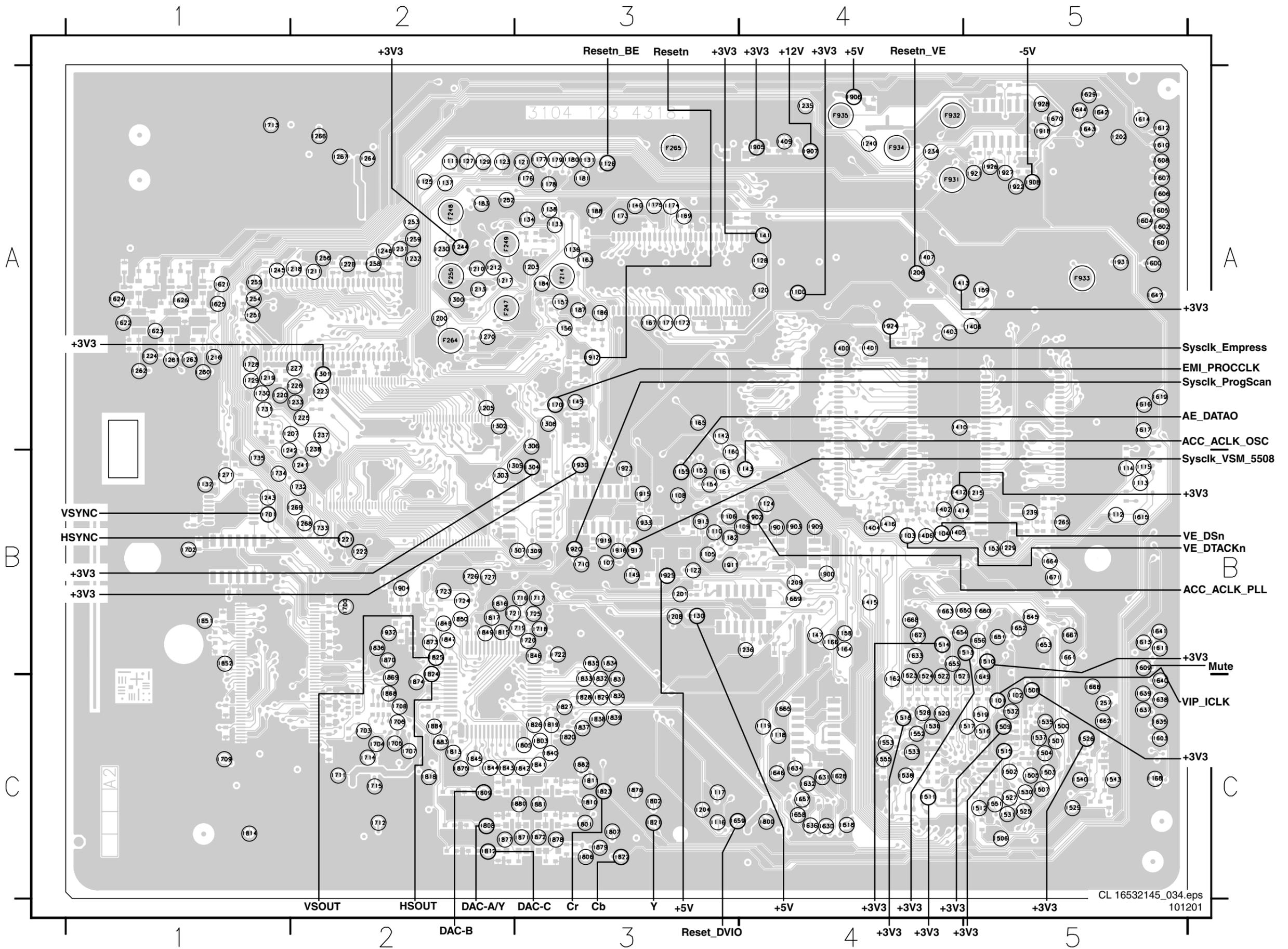


2104	A3	2802	B2	3803	C3	7702	B1
2105	A3	2803	C2	3804	C3	7800	B1
2106	A3	2804	C2	3805	C2	7801	C2
2107	A3	2805	B2	3806	B2	7900	B4
2108	A3	2806	B2	3809	C2	7901	B4
2115	B3	2807	B2	3810	B2	7902	B2
2120	A4	2808	C2	3811	C2	7904	B3
2121	A3	2809	C2	3813	C3	7905	A5
2122	A3	2810	B1	3814	C3	7906	B3
2123	A3	2811	B1	3815	C2		
2124	A3	2812	C1	3817	C2		
2125	A3	2813	C1	3820	C2		
2126	A3	2814	C2	3821	C3		
2128	A3	2815	C2	3822	C3		
2137	A3	2816	C3	3823	C2		
2202	B5	2818	C2	3826	C2		
2214	A2	2819	B3	3827	C2		
2224	A2	2820	B2	3828	B1		
2229	B3	2822	C3	3900	B3		
2300	A2	2823	C2	3901	B4		
2301	A2	2826	C2	3902	B4		
2302	A2	2827	C2	3903	B4		
2303	A1	2828	C3	3904	B3		
2306	A2	2831	C2	3906	B3		
2307	A2	2832	C2	3908	B3		
2308	A2	2833	C3	3910	A5		
2309	A2	2835	C2	3911	A5		
2310	A2	2836	C2	3912	A4		
2312	B3	2900	A4	3913	A5		
2402	A5	2901	A4	3914	B1		
2404	A4	2902	A4	3915	B1		
2405	B4	2906	B4	3916	A5		
2406	B4	2911	B3	3917	B3		
2407	B4	2915	B3	3918	A5		
2408	A4	2916	B2	3919	A5		
2409	A4	3111	B5	3920	B3		
2410	B4	3112	B5	3921	A5		
2414	B4	3113	B4	3922	A5		
2415	B4	3114	B4	3923	A5		
2416	B4	3115	A3	3924	B2		
2435	B4	3116	A3	3925	B2		
2436	B4	3201	B5	4100	A3		
2443	A4	3205	B5	4101	A3		
2446	A5	3206	B5	4106	B4		
2500	C5	3207	B4	4107	B3		
2501	C5	3212	B5	4300	B2		
2502	C5	3229	A2	4301	B3		
2503	C5	3230	A1	4406	B5		
2504	C4	3231	A1	4409	B4		
2505	C4	3232	A2	4500	C5		
2506	C4	3238	A1	4702	B1		
2507	C4	3239	A1	5204	A1		
2508	C4	3240	A1	5207	B5		
2509	C4	3241	A1	5208	B3		
2510	C4	3300	B2	5211	A1		
2511	C4	3301	B3	5601	A1		
2521	C5	3402	B4	5604	A1		
2522	C4	3404	A4	5605	A1		
2523	C4	3405	B4	5800	C2		
2524	C5	3406	A4	5801	C3		
2525	C5	3407	A4	5802	C3		
2526	C4	3502	C5	5803	C2		
2527	C4	3503	C5	5804	C3		
2528	C4	3504	C5	5805	C3		
2529	C4	3505	C5	5806	C2		
2531	C5	3506	C5	5807	C3		
2532	C4	3507	C5	5808	C3		
2533	C5	3508	C4	5900	A3		
2534	C5	3509	C4	5901	A4		
2535	C5	3513	C5	5905	B3		
2536	C5	3515	C4	6500	C5		
2537	C5	3600	B4	6900	B2		
2538	C4	3606	A1	7101	A3		
2543	C5	3607	A1	7104	A3		
2544	C4	3608	A1	7201	B5		
2565	C5	3616	A1	7202	B4		
2605	A1	3617	A1	7300	A2		
2606	A1	3618	A1	7301	A2		
2607	A1	3626	A1	7302	B2		
2615	A1	3627	A1	7303	B3		
2616	A1	3628	A1	7401	A5		
2617	A1	3703	C2	7402	A4		
2625	A1	3705	B2	7502	C4		
2626	A1	3706	B2	7504	C5		
2627	A1	3710	C2	7601	A1		
2718	B2	3720	C2	7604	A1		
2721	B1	3800	B1	7606	A1		
2722	B1	3802	B2	7701	B1		

Layout Digital Board (Part 2 Bottom View)



Layout Digital Board (Testlands Bottom View)



8. Alignments

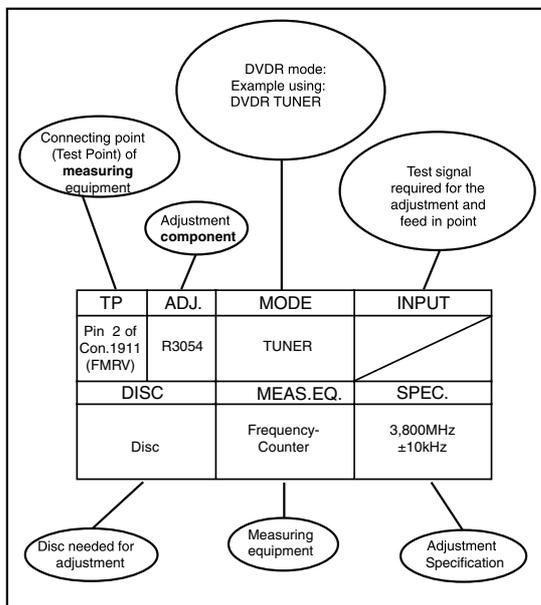
8.1 Alignment Instructions Analogue Board

Alignments Analog PCB Eur

Test equipment:

- Dual-trace oscilloscope
Voltage range : 0.001 ~ 50 V/div
Frequency : DC ~ 50 MHz
Probe : 10:1, 1:1
- DVM (Digital voltmeter)
- Frequency counter
- Sinus generator
Sinus : 0 ~ 50 MHz
- Test pattern generator

How to read the adjustment procedures:



Front End (FV)

Service tasks after replacement of IC 7703, coil L5702 and L5703:

1 AFC Adjustment:

Purpose: Correct adjustment of demodulator AFC - circuit

Symptom, if incorrectly set:

Bad or disturbed TV channel reception.

PAL - AFC adjustment [5703]:

TP	ADJ.	MODE	INPUT
IC 7703 Pin 17 (1976)	L5703	TUNER	38,9MHz 500mV _{pp} at Tuner 1705, Pin 11 (F700, IF-out)
DISC		MEAS.EQ.	SPEC.
		DC Voltmeter Frequ. Generator	2,5V ±0,1V

Storage in NVRAM via command mode interface of DSW:

After adjustment, the AFC reference value has to be stored in the NVRAM.

This reference value is 256 * measured voltage/Ucc. Ucc is 5.0V.

Store the reference value via command 732, followed by the ref. value.

Example: DD:> 732 128

2 HF - AGC adjustment [3707]:

Service tasks after replacement of IC 7703:

Purpose: Set amplifier control.

Symptom, if incorrectly set:

Picture jitter if input level is too low and picture distortion if input level is too high.

TP	ADJ.	MODE	INPUT
Tuner 1705 Pin 11 (F700, IF-out)	R3707	Set tuned to channel 25 503.25 MHz	5mV(74dBμV) on aerial input PAL white picture, audio IF on, no modulation
DISC		MEAS.EQ.	SPEC.
		Oscilloscope Video Pattern Generator	500mV _{pp} +/-0.5dB (use a 10:1 probe)

3 Attenuating the 40.4 MHz [5702]: (SECAM only)

Service tasks after replacement of coil 5702:

Purpose: To attenuate the band I carrier rests.

Symptom, if incorrectly set:

Bad picture quality when the filter attenuates the picture carrier (38.9MHz).

TP	ADJ.	MODE	INPUT
OFW 1700 Pin 1 (F704)	L5702	TUNER	40.4 MHz, 200mV _{rms} at Tuner 1705, Pin 11 (F700, IF-out)
DISC		MEAS.EQ.	SPEC.
		Oscilloscope, Sinus Generator, Counter	adjust minimum amplitude

If the adjustment is correct the signal at pin 1 of OFW [1700] must be smaller than the input signal amplitude by at least 6 dB.

8.2 Reprogramming Procedure of NVM on the Analogue PCB

The NVM, item 7815, on the Analogue board contains the following factory settings:

1. Bargraph 0dB correction factor
2. Clock correction factor
3. AFC reference value
4. Slash version

The settings 1,2 and 3 are stored in the NVM during the production of the analogue board.

The slash version is stored at the end of the production line of the set.

In case of failure, the NVM must be replaced by an empty device. By way of commands via the Diagnostic Software or via ComPair, the factory settings must be restored in the NVM.

8.2.1 Bargraph 0db Alignment

For an exact functionality of the bar graph in the display, a correction factor for the left and the right channel is stored in the NVM.

Procedure:

- Put the set in DSW command mode
- route Audio path from Audio front connectors to digital with the following command:
DD:> 713 01
- apply a sine wave of 1 kHz, 1.65 Vrms (0 dB) to the front connectors, audio left and right
- store 0 dB bar graph level with command 720
DD:>720

8.2.2 Clock Correction Adjustment

To guarantee an exact function of the real time clock, an adjustment of the clock frequency is possible and stored in the NVM.

Procedure:

- Connect a pull up resistor of 10k between pin 7 and 8 of the clock IC PCF8593T, item 7811, on the analogue PCB
- put the set in service command mode
- execute command 722 to initiate that a 1 Hz signal is available on pin 7 of the clock IC
DD:>722
- measure the frequency of the Clock Crystal with an accuracy of ± 1 (s). Normally the measured frequency must be between 999902 (s) and 1000097 (s). If the frequency is outside this range, the clock IC must be replaced.
- Execute command 721 with the measured frequency as an input parameter
example:
DD:>721 1000023

8.2.3 AFC Reference Voltage Tuner

This function stores the reference voltage for the tuner in the NVM. Before this value can be stored, the AFC adjustment, described in the adjustment instructions of the analogue board, must be carried out.

Procedure:

- Adjust AFC circuit
- Calculate the reference value
- Execute command 732 and use the calculated reference value as parameter
example:
DD:>732 128

8.2.4 Slash Version

The slash version is stored with command 715 followed by the slash version as parameter.

The slash versions used in DVDR1000 and DVDR1500 are the following:

- DVDR980/00X: 2
- DVDR980/02X: 2
- DVDR980/05X: 4
- DVDR985/00X: 5
- DVDR985/02X: 5
- DVDR985/05X: 6

Example:

DD:>715 1

Reset of Slash Version

Use command 729 to reset the analogue board to the default setting.

Procedure:

- Put the set in DSW command mode
- Execute command 729 with the following parameters:
DD:> 729 w 0xA0 3 0x07 0xD0 0x00
- Leave the DSW command mode and start up the set in application mode. No background is visible on the TV screen. The analogue board is ready to accept the appropriate slash version.

8.3 Rework Procedure IEEE Unique Number

8.3.1 Scope:

The procedure describes how to upgrade sets with a unique number after repair. This unique number is stored in the NVRAM (item 7201) of the digital board at the end of the production line.

This procedure is only valid or necessary when:

- The digital board is replaced
- NVRAM on the digital board is replaced
- NVRAM is cleared

In all other cases the repaired set retains its unique number. The procedure defines several means to re-assure the unique number depending on the possibilities of repair or the state the faulty set is in.

8.3.2 Handling:

State of Original (Defective) Board:

1. The digital board starts up in Diagnostics Mode: follow procedure A to retrieve the valid unique number
2. The digital board does NOT start up in Diagnostics Mode: follow procedure B.

8.3.3 Procedure A

1. Connect defective digital board to PC via serial cable (3122 785 90017)
2. start up hyper terminal or any other serial terminal via the correct settings (DSW command mode interface)
3. read out existing unique number via nucleus 403
example:
DD:> 403
40300: DV Unique ID = 00D7A1FC6C
Test OK @
4. note read out
5. program new digital board via nucleus 410
example: DD:> 410 00D7A1FC6C
41000:
Test OK @

The set has now the original unique number

8.3.4 Procedure B

1. Note the serial number of the set example:
AH050136130156
 - AH = production centre Hasselt. According to UAW-500: A=1 and H=8
 - 05 = change code (this is not used for this calculation)
 - 01 = YEAR
 - 36 = Production WEEK
 - 130156 = Lot and SERIAL number
2. Calculate the unique number: this number always exists out of 10 hexadecimal numbers.
3. First 5 numbers: First we calculate a decimal number according to the formula below: $35828 * \text{YEAR} + 676 * \text{WEEK} + 26 * A + H + 8788$ The figures are fixed, YEAR + WEEK + factory code (A + H) are variable
Example: $35828 * 01 + 676 * 36 + 26 * 1 + 8 + 8788 = 68986$ (decimal) Then we translate the decimal number to a hexadecimal number.
example: 68986 (decimal) = 10D7A (hex)
4. Last 5 numbers: The last 5 numbers exist out of the Lot and SERIAL number. We have to translate the decimal number to the next 5 hexadecimal numbers:
Example: 130156 (decimal) = 1FC6C (hex)
5. Program new digital board via nucleus 410 Therefore we use the 10 hexadecimal numbers we calculated above:
example:
DD:> 410 10D7A1FC6C
41000:
Test OK @

The set has now its original unique numbe

9. Circuit-, IC Descriptions and List of Abbreviations

9.1 Multi-Mode SOPS 50PS203

9.1.1 Why Multi-Mode SOPS?

Using ordinary SOPS results in a decrease of the efficiency at low output loads due to the increase of the switching frequency. The Multi-Mode SOPS will reduce the switching frequency at low loads but still preserves valley switching.

9.1.2 Block Diagram

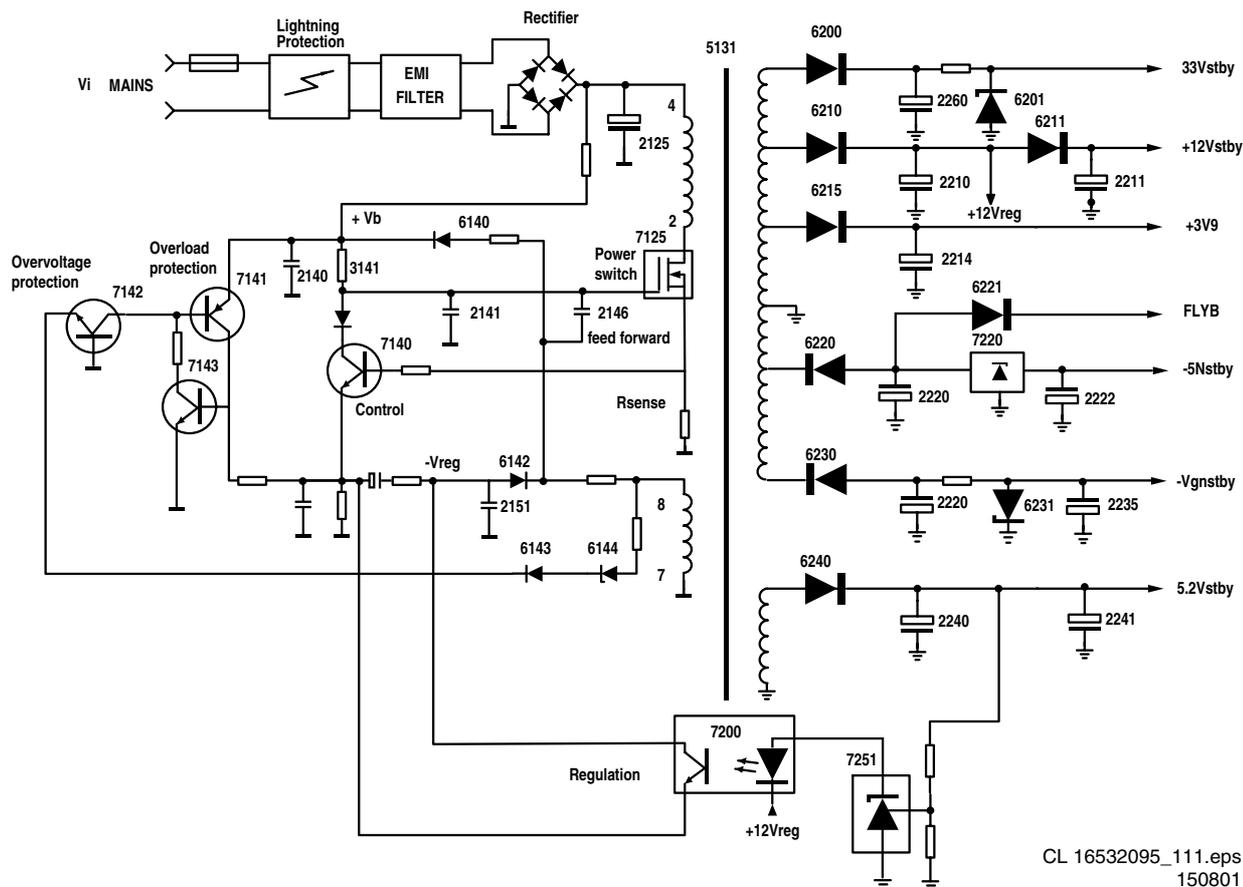


Figure 9-1

9.1.3 Circuit Description

Input Circuit

The input circuit consists of a lightning protection circuit and an EMI filter.

The lightning protection comprises R3120, sparkgaps 1124 and 1125. D6128, 6129, C2127 and R3129 are optional. L5110, L5115, C2120 and L5120 form the EMI filter. It prevents inflow of noises into the mains.

Primary Rectifier/smoothing Circuit

The AC input is rectified by diodes 6151, 6152, 6153, 6154 and smoothed into C2125. The voltage over C2125 is approximately 300V. It can vary from 200V to 390V.

Start Circuit

This circuit is formed by R3125, 3126, R3141, C2140 and R3132.

When the power plug is connected to the mains voltage, the MOSFET 7125 will start conducting as soon as the gate

voltage reaches a treshold value. A current starts to flow in primary winding 2-4. The MOSFET will be fed forward via winding 2-4, R3150 and C2146.

+Vb Supply and Negative Regulation Voltage

The positive part of the voltage over winding 7-8 will be rectified via R3150, D6140 and charged via R3140 into C2140. The voltage over C2140 has a value of +30 till +40V. This value depends on the value of the mains voltage V_i and the load. The negative part of the voltage over winding 7-8 will be rectified via R3150, D6142 and charged into C2151. The voltage over C2151 has a value of -15V and is used as regulation voltage.

Control Circuit

The control circuit exists of T7140, D6141, C2144 and 2145, C2147, R3147 and 3148.

This circuit is fed by supply voltage +Vb via R 3141. This circuit controls the conduction time and the switching frequency of the power switch circuit. It switches off the MOSFET as soon as the voltage over Rsense reaches a certain value. This value

depends on the error voltage at the emitter of T7140, which can be positive or negative (+/- 0,66V). The voltage fed back by the regulation circuit defines this error voltage.

Power Switch Circuit

This circuit comprises MOSFET 7125, Rsense formed by R3133, 3134, 3135, 3136 and 3137, R3131, R3132, D6146. Diodes 6130, 6131 and 6132 protect the control circuit in case of failure of the MOSFET.

Regulation Circuit

The regulation circuit comprises opto-coupler 7200, which isolates the base voltage of transistor 7140 at the primary side from a reference component 7251 at the secondary side. The TL431(7251) can be represented by two components:

- a very stable and accurate reference diode
- a high gain amplifier

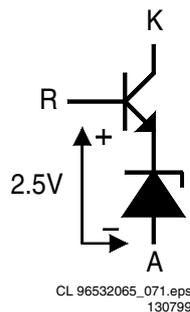


Figure 9-2

TL431 will conduct from cathode to anode when the reference is higher than the internal reference voltage of about 2.5V. If the reference voltage is lower, the cathode current is almost zero. The cathode current flows through the LED of the opto-coupler. The collector current of the opto-coupler will adjust the feedback level of the error voltage at the emitter of T7140.

Overload Protection Circuit

This circuit consists of R3145, C2143, a thyristor circuit formed by T7141 and T7143, R3143 and R3142. When the output is shortened, the thyristor circuit will start to conduct and switch off the supply voltage over C2140. This results in a switching of f of the drain current of the MOSFET 7125 and the output will be disabled. The start circuit will try to start up the power supply again. If the circuit is still shortened, the complete start and stop sequence will repeat. The power supply comes in a hiccup mode (is ticking).

Overvoltage Protection Circuit

This circuit consists of R3149, D6144, 6143, R3144, C2142 and T7142.

When the regulation circuit is interrupted due to an error in the control loop, the regulated output voltage will increase (overvoltage). This overvoltage is sensed on the primary winding 7-8.

When an overvoltage is detected, the circuit will start up the thyristor circuit T7141-7143. The power supply will come in a hiccup mode as long as the error in the control loop is present.

Secondary Rectifier/Smoothing Circuit

There are 6 rectifier/smoothing circuits on the secondary side. Each voltage depends on the number of windings of the transformer.

From these circuits a lot of voltages are derived and fed to 3 connectors. The following voltages are present at the output: Connector 209

Functional use: to Digital board + Dvio board

1. +3V3(for dig pcb + DVio)
2. +3V3(for dig pcb + DVio)
3. +3V3(for dig pcb + DVio)

4. +3V3(for dig pcb + DVio)
5. GND(for dig pcb + DVio)
6. +12V(for dig pcb + DVio)
7. GND(for dig pcb + DVio)
8. GND(for dig pcb + DVio)
9. +5V(for dig pcb + DVio)
10. STBY control(for dig pcb + DVio)
11. GND(for dig pcb + DVio)
12. -5V(for dig pcb + DVio)

The +12V is switched off by the STBY_ctrl signal.

When the +12V is switched off, also the +3V3, +5V and -5V are switched off. All these voltages are low drop regulated.

Connector 0205

Functional use: to analogue board + display board + flap motor 'STBY' indicates that the voltage will not be switched off in the standby situation.

1. +12VSTBY(= +12V Standby, for display heating, 8Vstby)
2. +5VSTBY(= +5V Standby; general use)
3. -5NSTBY(= -5V Standby; neg. voltage for drivers)
4. VGNSTBY(= -32V Standby; for display grids)
5. +33STBY(= +33V Standby; for tuner)
6. FLYB(flyback pulse for power fail + measurement)
7. GNDA(Ground for the analogue board)

Connector 0207

Functional use: to engine

1. +3V3(for engine servo board)
2. +5V(for engine servo board)
3. GND(for engine servo board)
4. +4V6E(for engine analog part)
5. GND(for engine servo board)
6. -5V(for engine servo board)
7. GND(for engine motor currents)
8. +12V(for engine motor currents)

9.2 Display Board

9.2.1 Operation Unit DC (DC Part)

The core element of the operation unit DC is the microcontroller TMP88CU77ZF [7156]. The TMP88CU77ZF is an 8 bit microcontroller fitted with 96kB ROM and 3kB RAM and is responsible for following functions:

- Integrated VFD driver
- Timer
- Evaluation of the keyboard matrix
- Decoding the remote control commands from the infra-red receiver pos. 6170
- Activation of the display
- Motor driver

The system clock is generated with the 12MHz quartz (Pos. 1153).

9.2.2 Evaluation of the Keyboard Matrix

There are 15 different keys on the display board. A resistor network is used to generate a specific direct voltage value, depending on the key pressed, via the resistors 3145, 3171, 3183 and 3194 on the analog/digital (A/D) ports (7156 Pin 17, 18, 19, 20). Pressing keys simultaneously may lead to undesired functions!

9.2.3 IR Receiver and Signal Evaluation

The IR receiver [7140] contains a selectively controlled amplifier as well as a photo-diode. The photo-diode changes the received transmission (approx. 940nm) in electrical pulses, which are then amplified and demodulated. On the output of the IR receiver [7140], a pulse sequence with TTL-level, which corresponds to the envelope curve of the received IR remote control command, can be measured. This pulse sequence is input into the controller for further signal evaluation via input IRR [7156, pin 2].

9.2.4 Motor Driver Flap

The flap-motor is controlled via the 2 Port-Pins (MD1, MD2) of the P (7156, Pin 12, Pin 100). The motor driver part is constructed as a bridged dual power operational amplifier. Between the IC outputs (7120, Pin1, Pin3) and a Boucherot circuit (2121, 3126) suppresses a spurious 3MHz oscillation from the output stage. The two ports-pins (MD1, MD2) of the P are PWM-outputs and are controlled in the following way:

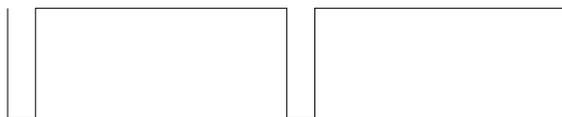
Flap Motor:

	MD1	MD2
off	H	L
open	H	PWM(H)
close	L	PWM(L)

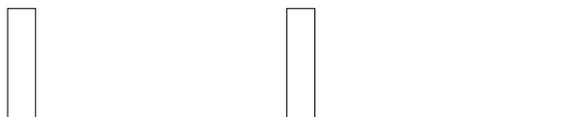
Duty Cycle 50% for OPEN and CLOSE



Duty Cycle app. 10% for CLOSE



Duty Cycle app. 10% for OPEN



CL 16532095_112.eps
150801

Figure 9-3

For the detection of the end-positions of the flap there are two switches (1178, 1179) installed and the information is evaluated from the P via the signals SW_1178 and SW_1179.

Flap Switches:

	SW1	SW2
open	L	H
closed	H	L
moving	H	H
error	L	L

9.2.5 Bi-Color LED (Standby and ON)

The STBY-LED is a red/green bi-color-LED and is controlled via the STBYLED-signal of the P (7156 Pin 10) in the following way:

Colour of STBY LED	Status of the Set
red	STBY
green	ON

9.3 Analogue Board Europe

9.3.1 Microprocessor TMP93C071F

The microcontroller „AIO“ TMP93C071F is a 16bit microcontroller with internal ROM and 8kB RAM. It includes the following functions:

- A/D converters
- composite sync input
- I²C bus interface

Following connection to the mains, a positive pulse on the reset input on the P is generated by the reset-IC TL7705 (Pos.7900). The system clock is generated with the 20MHz quartz (Pos. 1994).

9.3.2 Bus Systems

The communication between the P and the other functional groups is via the I²C-bus (SDA, SCL). The clock rate is approx. 95kHz.

Functional groups on the I²C bus:

- E²PROM ST24E16 (Pos. 7815)
- Tuner (Pos. 1705)
- Matrix-switch STV6410 (Pos. 7507)
- Audio IC / MSP (Pos. 7600)
- Display board (Pos. 1987)
- VPS-IC (Pos. 7990).

9.3.3 E²PROM

The E²PROM ST24E16 (Pos. 7815) is an electric erasable and programmable, non-volatile memory. The E²PROM stores data specific to the device, such as the AFC-reference value, clock-correction-factor, etc. The data is accessed by the P via the I²C-bus.

9.3.4 VPS, PDC, Teletext (Europe Only)

The STV5348 (Pos. 7990) is a VPS, PDC, and Teletext Decoder with an external 13,875Mhz quartz.

The following data formats are identified:

- VPS (Timer data and station name)
- PDC Format 2 (Timer data and station name)
- PDC Format 1 (station name and time)
- TXT header line (time for „time download“)

9.3.5 FOME

The FOME-circuit compares the video signal coming from the tuner and the one coming from the Scart-plug 1. If the video-signals are identical the output of the FOME-circuit is low.

9.3.6 Fan Control

The fan control circuit is necessary to control the speed of the cabinet fan (Pos. 1984) according to the requirements in temperature and noise. The temperature is measured via an NTC on the display board (Pos. 3145). When the temperature is lower than 25°C the fan-voltage is approx. 5V and will reach approx. 10V at a temperature of 40°C. It is also possible to switch off the fan via the control line ION_FAN. The circuit generates also two control-signals: TEMP goes to the P and BE_FAN is the control-line for the basic engine fan.

9.3.7 Power Supply

The 5SW and 8SW supply are switched off in case of standby from the P via the ISTBY-line. This is possible for power-save. The ISTBY-line must be low in case of STBY. There is also a „power fail“ circuit on the PS-schematic which is necessary to mute AUDIO when IPFAIL is low.

9.3.8 Front End (TU, AP Part)

The Front End Comprises the Following Parts:

- Tuner [1705]
- IF amplifier & video demodulator IC TDA 9818 [7703]
- Sound processor MSP3415G [7600]

IF Selection

The IF frequency of the video carrier is 38.9 MHz for all systems except SECAM L' (33.9 MHz).

A quasi-split audio system is used. Separate surface-wave filters (SAW) are required. [1700], [1701] for video, [1702] for audio. [1700] is switched into the signal path for DK/I-SECAM L/L' reception, if the signal SAWS is "high". In this case the switches [7701], [7702] are open and the diode [6700] is conducting. [1701] is switched into the signal path for BG reception, if the signal SAWS is "low". Then the switch [7708] is open and the diode [6701] is conducting. For DK/I-SECAM L' reception, an additional circuit for suppressing the adjacent channel audio carrier is provided, which is set using coil [5702] to maximum suppression at 40.4MHz.

IF Demodulator**TDA 9818**

The IF signal from the tuner is processed by the demodulator IC TDA 9818 [7703]. The signal PSS to pin3 switches between demodulation of positive SECAM or negative PAL modulated video carriers. A QSS-audio-IF signal SIF1 is generated for demodulation in the sound processor [7600]. The audio-IF carrier is selected in the audio SAW filter [1702]. This filter is switched for SECAM L'. If the signal SB1 is "high", the switch [7707] is closed and the diode [6702] is not conducting. For all other standards the diode [6702] is conducting and the switch [7707] is open. The output signal from this SAW filter is first processed in the TDA 9818. Audio carriers are converted from the tuner IF level into the audio IF position and further processed in the audio demodulator [7600]. The AFC coil [5703] on the TDA 9818 is adjusted so that when a frequency of 38.90 MHz is supplied to the IF output of the tuner, the AFC voltage on pin 17 of the TDA 9818 is 2.5V. The setting of the picture carrier frequency for SECAM L in the TDA 9818 is achieved by connecting pin 7 of the IC via a resistor [3702] to earth. The switch [7700] and the signal SB1 "high" do this. The HF-AGC is set using the AGC controller [3707] so that, with a sufficiently large antenna input signal (74 dBV), the voltage at the IF output of the tuner [1705] pin 11 is 500 mVpp. This setting must be carried out, when the audio carrier is switched off. The demodulated video signal appears on pin 16 [7703]. The demodulator AGC voltage at pin4 is used to determine the antenna signal strength after a buffer [7705] with the signal AGC_MUTE. In the opposite direction this line may be used to mute the demodulator to avoid cross talk in all cases, where the tuner signal is not needed. In this case a „high“ signal is sent via AGC_MUTE and the conducting diode [6703] to pin4. The video trap [1703] reduces adjacent channel video and sound carrier remainders in the video for BG standards. For all other standards the switch [7704] and signal TS "low" bypass this trap. In this cases the selectivity of the SAW filter [1700] is sufficient. A frequency response correction is achieved by the inductance [5009] for not BG standards. This correction is not preferred for SECAM L' and therefore shorts circuited by [7709], if the signal SB1 is "high". The demodulated video signal VFV is available after the buffer and limiting stage for noise peaks [7706]. The FM-PLL demodulator function of TDA 9818 is not used and deactivated by the resistor [3726].

Audio Demodulator**Sound processor MSP 3415G**

The MSP 3415G [7600] is a multistandard sound processor which can demodulate FM Mono/Stereo, NICAM and AM signals. The incoming signal is first controlled and then digitised. The digital signal is then demodulated in 2 separate channels. In the first MSP channel, FM and NICAM (B/G/I/D/K) are demodulated, whereas in the second MSP channel, FM and are demodulated again (NICAM L corresponds to NICAM B/G). These demodulated signals are selected digitally in the I/O and switched to the D/A converter on the outputs. Amplitude and bandwidth of the demodulated audio signals can be determined in the MSP using the corresponding commands via

the I2C bus. The audio signal from the tuner is available at the pins 30 AFER and 31 AFEL.

9.3.9 Input/Output Video-Routing (Europe-Version)**General Description:**

The complete Video- I/O-switching is basically realised by the I/O switch STV6410A. It is controlled via IIC-Bus-0 (SDA/SCL) by the all in one C on the analogue board. The STV 6410 has three YCVBS switches, three chroma switches and one RGB switch. All switches have 6-dB amplification on the outputs. The YCVBS inputs have bottom clamp, the chroma inputs have average clamp, and the RGB inputs have bottom clamp circuits at the inputs. The R/C inputs can be switched to average clamp for chroma signals via I2C bus.

The IC has also one slow blanking monitor and one fast blanking switch for fast RGB insertion (see detailed description in chapter 1.5). Two pre-selectors BA 7652 are additionally used: One for switching between Rear CVBS, Y- Rear and Front, the second for switching between Chroma- Rear and Front signal. Both pre-selectors are controlled via IS1 and IS2 from the analogue board C.

CVBS Signals:

There are four CVBS input connection possibilities: Front chinch (E6), Rear Chinch (E4), Scart 1 (E1) and Scart 2 (E2). Rear Chinch In is routed via the pre selector BA 7652; the other signals are connected direct to the STV 6410. The selected CVBS signal is routed to Rear Chinch Out (via BA 7660, 6dB amplification, 75 Ohm driver) and to Scart 1. Independent of the input signal quality (CVBS, S-Video or RGB) the digital board supplies also S-Video and RGB signals to the corresponding socket.

S-Video Signals:

There are also four S-Video input connection possibilities: Front In (E5), Rear In (E3), Scart 1 and Scart 2. For S-Video from Scart this option has to be switched on in the OSD menu. The pre-selectors and the STV 6410 do the signal selection (for detailed routing see overview). Also the video quality will be S-Video, the digital board supplies also CVBS to the corresponding sockets. The S-Video signal that is coming from the digital board is routed via BA 7660 (6-dB amplification and 75-Ohm driver) to the S-Video Rear Out socket.

RGB Signals:

The Scart 2 RGB input signal (Decoder socket) is connected to the RGB switch of STV 6410 and to the digital board in parallel. The RGB from Scart 2 is routed to Scart 1 in low power standby mode. The direct connection (not via STV 6410) is for loop through and REC. The RGB signal, which is coming from the digital board, is connected to the RGB encoder input of the STV 6410 and is routed to Scart 1 in all other modes.

As the Scart-connection can carry either RGB- or Y/C-signals it is necessary to define the available and selected signal-property. While Pin15 of Scart (Red or Chroma-upstream) is fully handled via STV6410A the Pin7 (Blue or Chroma-downstream) has to be extra set.

- Scart1: Pin42 of C (SC1YC_H-line):
 - Low (Blue-Out on SC1
 - High (Chroma-In on SC1
- Scart2: Pin41 of C (SC2RGB_H-line):
 - Low (Chroma-Out on SC2
 - High (Blue-In on SC2

Detection of Status-Information**Pin-8 (Slow-Blank):**

Level-detection of Pin-8 (Scart-1 and -2) is realised by using STV6410A. It can be readout via IIC-Bus by the CC-C. To obtain the status of Scart1-Pin8, Bit 0 & 1 of register 06h must be set to 0 (Input-mode). The corresponding bits for verification of Scart2-Pin8-status are set to input-mode as default.

Meaning of Read-Register-Bits:

- Bit 7 & 6: not used
- Bit 5 & 4: Status Scart-2/Pin8:
 - 0 1 Low-level
 - 1 0 Medium-level (16:9)
 - 1 1 High-level (4:3)
- Bit 3 & 2: not used
- Bit 1 & 0: Status Scart-1/Pin8:
 - 0 1 Low-level
 - 1 0 Medium-level (16:9)
 - 1 1 High-level (4:3)

Pin-16 (Fast Blank):

Only the status/level of Scart-2/Pin16 must be detected; this is realised by using PortC3/AIN14 (Pin25) of the CC-C as an Analogue-input.

- ADC-value lower or equal 24h (Pin16 low (no RGB-signals)
- ADC-value greater 24h (Pin16 high (RGB present on Scart-2)

To avoid misdetection a "software-integration" (result is first valid if it was 3-times the same) must be implemented, determination has to be done approx. every 47msec (no multiple of V-sync).

WSS on Y/C-Plug:

Picture-Ratio-Information (16:9 or 4:3) on SVHS-connections is coded via the average DC-level of the Chroma-signal-line, detection is realised by using an analogue-input-port of the CC-C.

- ADC- value lower or equal 40h (4:3-picture-ratio delivered
- ADC-value greater 40h (16:9-picture-ratio available on plug

Y/C-Rear is determined via Port40/AIN3 (Pin14) of CC (WSRI-line) and Port41/AIN4 (Pin15) is used for Y/C-Front (WSFI-line).

Generation of Status-Information

Pin-8 (Slow Blank):

Only on Scart-1 the Slow-Blank-Status (Level of Pin8) must be created, which is done via IIC-Bus-register 06h (Bits 0 & 1) of the STV6410A.

Pin-16 (Fast Blank):

Only the status/level of Pin16-Scart1 must be controlled; this is realised by using the FB-switch-capabilities of the STV6410A, which are set via IIC-Bus-register 04h (bits 4 & 5).

WSS on Y/C-Plug:

The appropriate DC-level on Chroma-signal-line for Y/C-Rear-Out is produced via Port57 (Pin10) of the CC-C (WSRO-line).

- 4:3 - Picture-ratio supported on Y/C-Plug: Port57 set to 0
- 16:9 - Picture-ratio supported on Y/C-Plug: Port57 set to 1

(OPV) the signals are delivered back to the STV 6410 and also direct to the 2nd rear out Cinch. The other outputs (Scart, Cinch) are supported by the STV 6410.

Detailed Description STV 6410:

The STV 6410 is an I²C bus controlled audio and video switch matrix, which is able to handle audio input signals up to 2 Vrms. The used outputs are equipped with internal level adjustment possibility. Low distortion and very good channel separation is a typical peculiarity of this IC. The output resistance is very low and the frequency bandwidth is up to 50 kHz.

Detailed Description UDA 1360:

The UDA 1360TS is a stereo Analog-to-Digital Converter employing bitstream conversion techniques. The UDA supports the I²S-bus data format and the MSB-justified data format with word lengths of up to 20 bits. The IC supports also 2Vrms input signals and is designed for 3V3 supply voltage. The device is able to handle system clocks of 256fs and 384fs. Typical THD+N at 0dB is -85dB and a S/N performance up to 97dB is possible.

Detailed Description UDA 1328:

The UDA1328 is a 6 channel DAC employing bitstream conversion techniques, which can be used either in L3 microcontroller mode or in static pin mode. The UDA 1328 supports the I²S-bus data format with word lengths of up to 24 bits. Digital sound features can be controlled with the L3 interface. System clock can be set to 256fs or 384fs. The Device also provides 2 high quality differential outputs. Typical THD+N at 0dB is -95dB and a S/N of up to 106dB is possible. Supply voltage is 3V3.

Detailed Description MC 33078:

The MC33078 is a dual operational amplifier for audio applications. It offers low voltage noise (4,5nV/√Hz) and high frequency performances (15MHz Gain Bandwidth product, 7V/s slew rate). In addition the MC33078 has a very low distortion (0,002%).

9.3.10 Audio Routing Analogue board (Europe / Nafta)

General Description:

The Audio- I/O switching is realised by the STV6410 I/O switch. By I²C Bus (SDA-0/SCL-0) it is possible to control all the Audio in- and outputs (for detailed Information we refer to the STV6410 routing overview).

Analog audio coming from DV-Board and second rear Cinch input is routed via MSP3415 to the STV 6410. After selecting the audio source via STV 6410, the signal must be transformed into the digital domain. For this, the UDA 1360TS (ADC) is responsible. An input-voltage of up to 2Vrms can be handled from the IC's. For further processing, the UDA 1360TS (ADC) delivers the data-in I²S format to the digital-board. After a certain delay the (processed) data come back from the digital board to the UDA 1328 (DAC). The UDA 1328 (DAC) transforms the I²S data back into the analog domain and feeds the signals direct to the MC33078 (OPV). From the MC33078

BLOCK DIAGRAM VIDEO IN/OUT EUROPE-VERSION

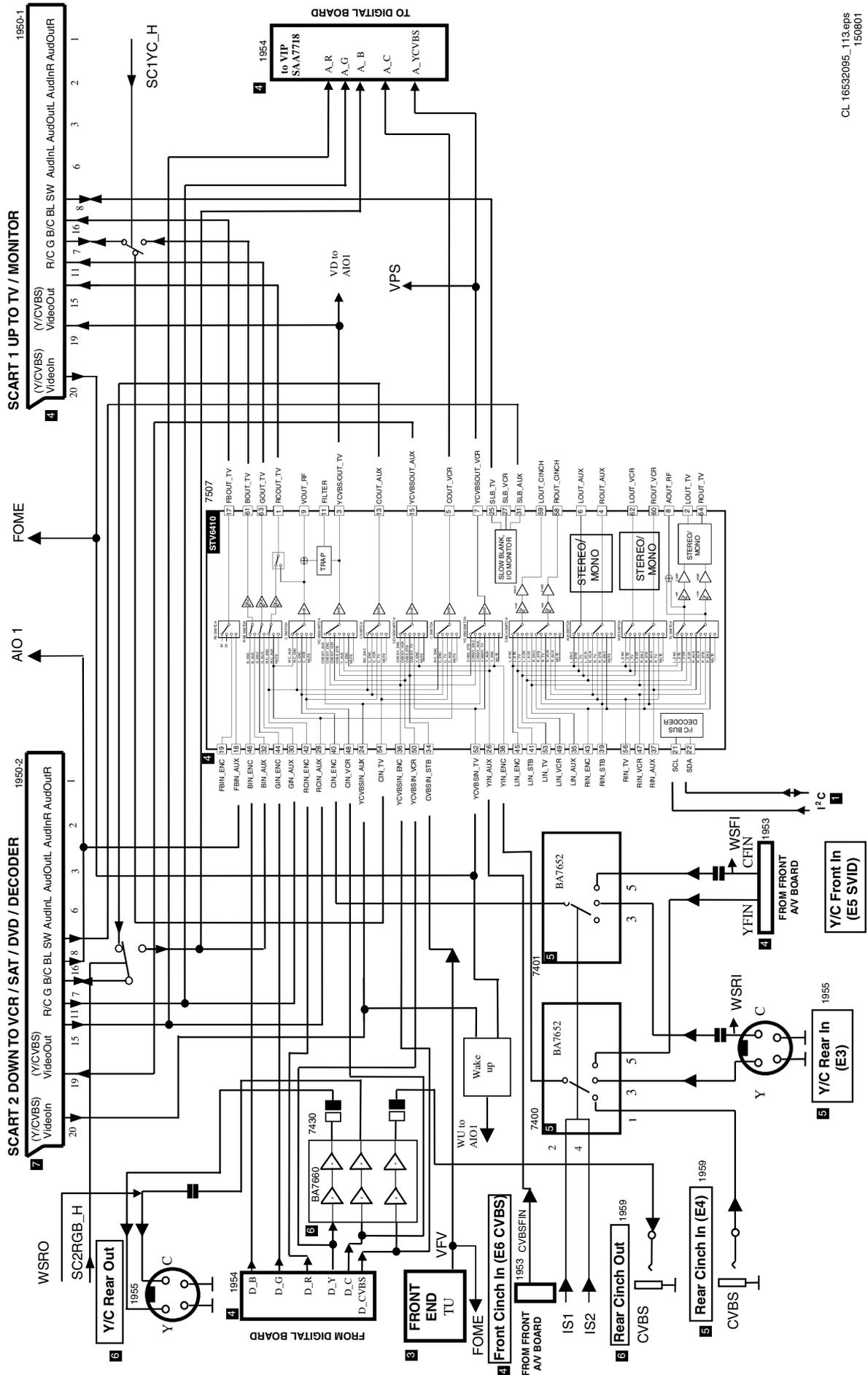


Figure 9-4

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BLOCK DIAGRAM AUDIO IN/OUT EUROPE-VERSION

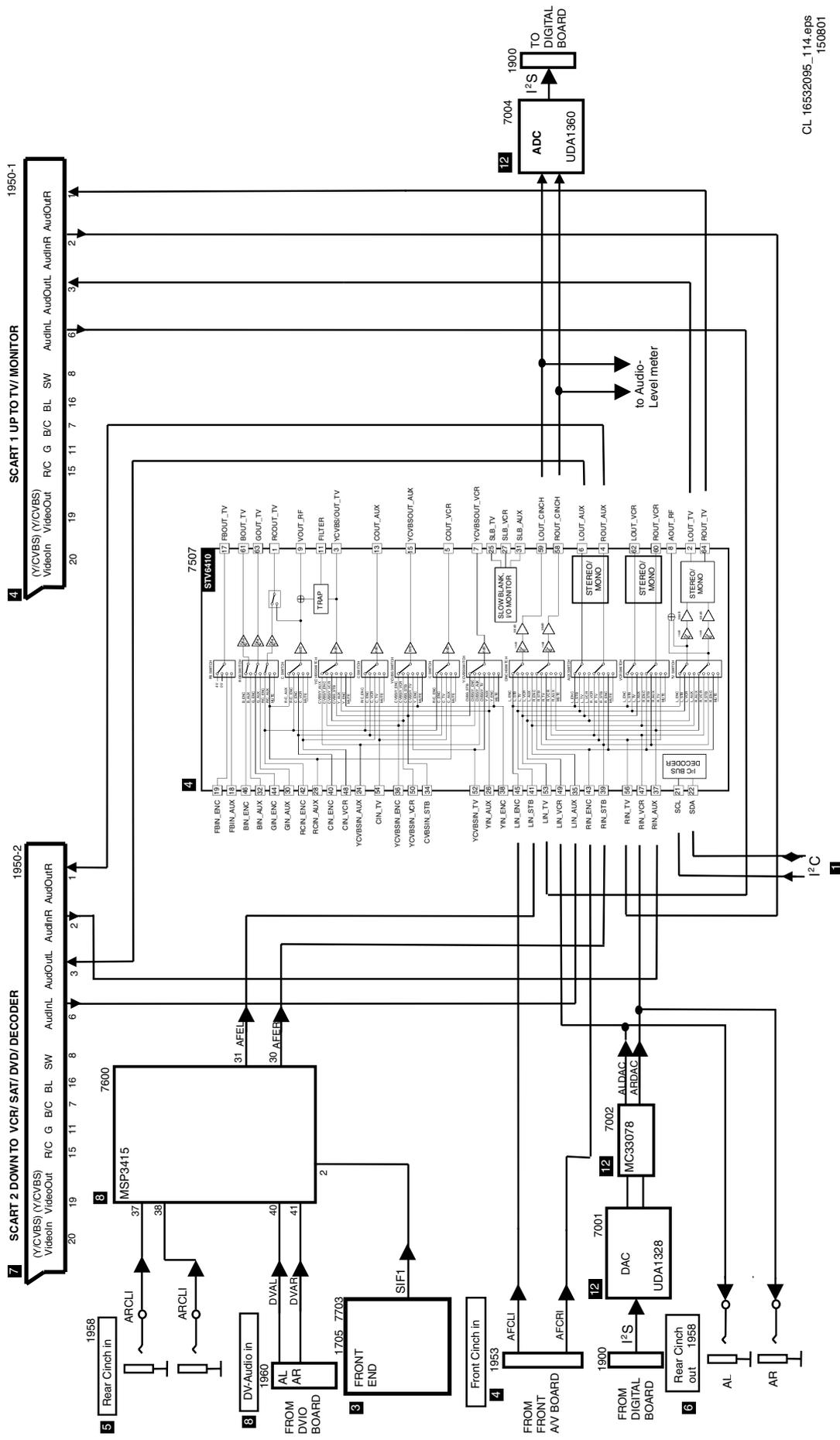


Figure 9-5

9.4 Analog Board Nafta version

9.4.1 Microprocessor TMP93C071F

The microcontroller „AIO“ TMP93C071F is a 16bit microcontroller with internal ROM and 8kB RAM. It includes the following functions:

- A/D converters
- composite sync input
- I²C bus interface

The following connection to the mains, a positive pulse on the reset input on the P is generated by the reset-IC TL7705 (Pos.7900).

The system clock is generated with the 20MHz quartz (Pos. 1994).

9.4.2 Bus Systems

The communication between the P and the other functional groups is via the I²C-bus (SDA, SCL). The clock rate is approx. 95kHz.

Functional groups on the I²C bus:

- E²PROM ST24E16 (Pos. 7815)
- Tuner (Pos. 1705)
- Matrix-switch STV6410 (Pos. 7507)
- Audio IC / MSP (Pos. 7600)
- Display board (Pos. 1987)

9.4.3 E²PROM

The E²PROM ST24E16 (Pos. 7815) is an electric erasable and writeable, non-volatile memory. The E²PROM stores data specific to the device, such as the AFC-reference value, clock-correction-factor, etc. The data is accessed by the P via the I²C-bus.

9.4.4 FOME

The FOME (Follow Me) -circuit compares the video signal coming from the tuner and the one coming from the Scart-plant 1. If the video-signals are identical the output of the FOME-circuit is low.

9.4.5 Fan Control

The fan control circuit is necessary to control the speed of the cabinet fan (Pos. 1984) according to the requirements in temperature and noise. The temperature is measured via an NTC on the display board (Pos. 3145). When the temperature is lower than 25°C the fan-voltage is approx. 5V and will reach approx. 10V at a temperature of 40°C. It is also possible to switch off the fan via the control line ION_FAN. The circuit generates also two control-signals: TEMP goes to the P and BE_FAN is the control-line for the basic engine fan.

9.4.6 Power Supply

The 5SW and 8SW supply are switched off in case of Stby from the P via the ISTBY-line. This is possible for power-save. The ISTBY-line must be low in case of STBY. There is also a „power fail“ circuit on the PS-schematic which is necessary to mute AUDIO when IPFAIL is low.

9.4.7 Front End (TU, AP Part)

The front end comprises the following parts:

- Tuner [1705]
- IF amplifier & video demodulator IC TDA 9817 [7703]
- Sound processor MSP3445G [7600]

IF Selection

The IF frequency of the video carrier is 45.75 MHz. A quasi-split audio system is used. Separate surface-wave filters (SAW) are required. [1701] for video, [1702] for audio.

IF Demodulator

TDA 9817

The IF signal from the tuner is processed by the demodulator IC TDA 9817 [7703]. A QSS-audio-IF signal SIF1 is generated for demodulation in the sound processor [7600]. Audio carriers are converted from the tuner IF level into the audio IF position and further processed in the audio demodulator [7600]. The AFC coil [5703] on the TDA 9817 is adjusted so that when a frequency of 45.75 MHz is supplied to the IF output of the tuner, the AFC voltage on pin 17 of the TDA 9817 is 2.5V. The HF-AGC is set using the AGC controller [3707] so that, with a sufficiently large antenna input signal (74 dBV) the voltage at the IF output of the tuner [1705] pin 11 is 500 mVpp. This setting must be carried out, when the audio carrier is switched off. The demodulated video signal appears on pin 16 [7703]. The demodulator AGC voltage at pin4 is used to determine the antenna signal strength after a buffer [7705] with the signal AGC_MUTE. In the opposite direction this line may be used to mute the demodulator to avoid crosstalk in all cases, where the tuner signal is not needed. In this case a „high“ signal is sent via AGC_MUTE and the conducting diode [6703] to pin4. The video trap [1703] reduces adjacent channel video and sound carrier remainders in the video. The demodulated video signal VFV is available after the buffer and limiter stage for noise peaks [7706]. The FM-PLL demodulator function of TDA 9817 is not used and deactivated by the resistor [3726].

Audio Demodulator

Sound processor MSP 3445G

The MSP 3445G [7600] is a NTSC sound processor. Amplitude and bandwidth of the demodulated audio signals can be determined in the MSP using the corresponding commands via the I2C bus. The audio signal from the tuner is available at the pins 30 AFER and 31 AFEL.

9.4.8 Video-Routing (Nafta Version)

General Description:

The complete Video- I/O-switching is basically realised by the I/O switch STV6410A, which is controlled via IIC-Bus-0 (SDA/SCL) by the all in one C on the analogue board. The STV 6410 has three YCVBS, three chroma, and one RGB switch which is not used in the Nafta I/O. All switches have 6-dB amplification on the outputs. The YCVBS inputs have bottom clamp, the chroma inputs have average clamp, and the RGB switch has bottom clamp circuits at the inputs. The R/C inputs can be switched to average clamp for chroma signals via I2C bus. Two pre-selectors BA 7652 are additionally used: One for switching between Y- Rear and Front, the second for switching between Chroma- Rear and Front signal. Both pre-selectors are controlled via IS1 and IS2 from the analogue board C.

CVBS Signals:

There are two CVBS input connection possibilities: Front chinch (E5) and Rear Chinch In (E3). Both CVBS sources are connected direct to the STV 6410 and routed to Rear Out 1 and Rear Out 2 via the 75-Ohm driver BA 7623. Both CVBS output sockets are connected to BA 7623 in parallel. Independent of the input signal quality (CVBS, S-Video or Y/UV) the digital board supplies also S-Video and Y/UV signals to the corresponding sockets.

S-Video Signals:

There are also two S-Video input connection possibilities: Front (E4) and Rear (E2) S-Video In which are connected to the pre-selector IC's BA 7652. One is used for Y, the other for Chroma

switching. The output of the pre-selector switches is connected to the STV 6410, and then the signal is routed via the 75-Ohm driver BA 7623 to the Rear Out S-Video socket.

Also the video quality will be S-Video, the digital board supplies also CVBS and Y/UV to the corresponding sockets.

Y/UV Signals:

The Y/UV In signal is routed direct to the digital board, there is no Y/UV IN -> Y/UV Out loop through in low power standby. As the digital board supplies only RGB signals, a RGB Y/UV matrix is used. This matrix consists of the operational amplifier TSH95 which generates the U and V signals according to the formulas: $2U=B-0,338R-0,661G$, $2V=R-0,838G-0,161B$. Then the signals are routed to the UV Output sockets via the 75-Ohm driver BA 7623. The corresponding Y signal is coming from the digital board via the STV 6410. The 75 Ohm Y socket is driven by the 75-Ohm driver BA 7623 and finally connected to the of the Y/UV Output.

Detection of Status-Information

WSS on Y/C-Plug:

- Picture-Ratio-Information (16:9 or 4:3) on SVHS-connections is coded via the average DC-level of the Chroma-signal-line, detection is realised by using an analogue-input-port of the CC-C.
- ADC- value lower or equal 40h (4:3-picture-ratio delivered)
- ADC-value greater 40h (16:9-picture-ratio available on plug)
- Y/C-Rear is determined via Port40/AIN3 (Pin14) of CC (WSRI-line) and Port41/AIN4 (Pin15) is used for Y/C-Front (WSFI-line).

Generation of Status-Information

WSS on Y/C-Plug:

The appropriate DC-level on Chroma-signal-line for Y/C-Rear-Out is produced via Port57 (Pin10) of the CC-C (WSRO-line).

- 4:3 - Picture-ratio supported on Y/C-Plug: Port57 set to 0
- 16:9 - Picture-ratio supported on Y/C-Plug: Port57 set to 1

9.4.9 Audio routing Analogue board (Europe / Nafta)

General Description:

The Audio- I/O switching is realised by the STV6410 I/O switch. By I²C Bus (SDA-0/SCL-0) it is possible to control all the Audio in- and outputs (for detailed Information we refer to the STV6410 routing overview).

Analog audio coming from DV-Board and second rear Cinch input is routed via MSP3415 to the STV 6410. After selecting the audio source via STV 6410, the signal must be transformed into the digital domain. For this, the UDA 1360TS (ADC) is responsible. An input-voltage of up to 2Vrms can be handled from the IC's. For further processing, the UDA 1360TS (ADC) delivers the data-in I²S format to the digital-board. After a certain delay the (processed) data come back from the digital board to the UDA 1328 (DAC). The UDA 1328 (DAC) transforms the I²S data back into the analog domain and feeds the signals direct to the MC33078 (OPV). From the MC33078 (OPV) the signals are delivered back to the STV 6410 and also direct to the 2nd rear out Cinch. The other outputs (Scart, Cinch) are supported by the STV 6410.

Detailed Description STV 6410:

The STV 6410 is an I²C bus controlled audio and video switch matrix, which is able to handle audio input signals up to 2 Vrms. The used outputs are equipped with internal level adjustment possibility. Low distortion and very good channel separation is a typical peculiarity of this IC. The output resistance is very low and the frequency bandwidth is up to 50 kHz.

Detailed Description UDA 1360:

The UDA 1360TS is a stereo Analog-to-Digital Converter employing bitstream conversion techniques.

The UDA supports the I²S-bus data format and the MSB-justified data format with word lengths of up to 20 bits. The IC supports also 2Vrms input signals and is designed for 3V3 supply voltage.

The device is able to handle system clocks of 256fs and 384fs. Typical THD+N at 0dB is -85dB and a S/N performance up to 97dB is possible.

Detailed Description UDA 1328:

The UDA1328 is a 6 channel DAC employing bitstream conversion techniques, which can be used either in L3 microcontroller mode or in static pin mode.

The UDA 1328 supports the I²S-bus data format with word lengths of up to 24 bits.

Digital sound features can be controlled with the L3 interface. System clock can be set to 256fs or 384fs.

The Device also provides 2 high quality differential outputs. Typical THD+N at 0dB is -95dB and a S/N of up to 106dB is possible.

Supply voltage is 3V3.

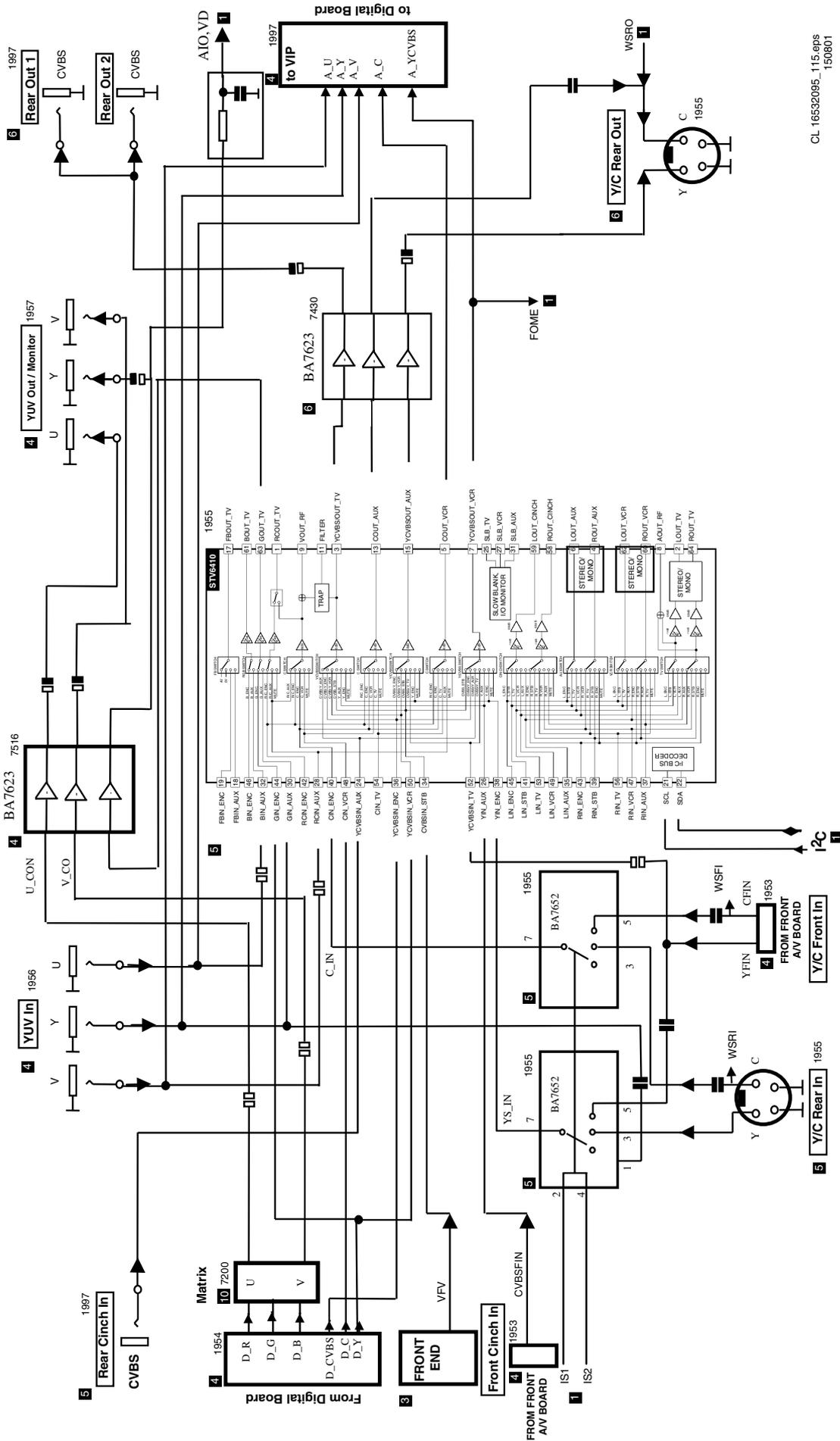
Detailed Description MC 33078:

The MC33078 is a dual operational amplifier for audio applications.

It offers low voltage noise (4,5nV/√Hz) and high frequency performances (15MHz Gain Bandwidth product, 7V/s slew rate).

In addition the MC33078 has a very low distortion (0,002%).

BLOCK DIAGRAM VIDEO IN/OUT NAFTA-VERSION



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Figure 9-6

9.5 Digital Board

9.5.1 Record Mode

Video Part

Analog Video input signals CVBS, YC and UV(RGB for EURO and YUV for USA) are routed via the analog board to connector 1601 and sent to IC7500 SAA7118 (Video Input Processor). Digital video input signals (DV_IN_DATA(7:0)) are sent from the DIVIO board through the connector 1603 and further also to IC7500.

IC7500 (VIP) encodes the analog video to digital video and processes the digital video to a digital video stream (CCIR656 format). This output stream (VIP_YUV[7:0]) goes to IC7403 SAA6752H (EMPRESS) and to IC7100 Versatile Stream Manager. The latter uses the data for VBI (vertical blanking interval) extraction.

IC7403 (EMPRESS) encodes the digital video stream into a MPEG2 video stream that is fed to IC7100 (VSM).

Audio Part

I2S audio are sent from the analog board to IC7403 EMPRESS via connector 1602. The EMPRESS compresses I2S audio data into an AC3 audio stream which is fed to IC7100 (VSM).

Front-End I2S

IC7100 (VSM) interfaces directly to the different hardware modules such as Basic Engine, EMPRESS IC7403, MPEG decoder IC7200 (Sti5508) and buffers the data streams that are coming from or going to these hardware modules.

In IC7100 (VSM), the video MPEG2 stream and the audio AC3 stream are multiplexed into a I2S packetized stream. The serial data are sent to the Basic Engine to be recorded.

Loop-Through

The multiplexed audio and video stream in the VSM is fed back via the parallel front-end interface to IC7200 (Sti5508). This IC decodes the MPEG stream into analog video and I2S audio. The video and audio signals are routed to the analog board via connectors 1601 and 1602. During recording, the recorded signal is present at the outputs of the analog board.

9.5.2 Playback Mode

During playback, the serial data from the Basic Engine is going directly to the Sti5505 via the serial front-end I2S interface. The Sti5508 is a MPEG & Audio/video decoder and has the following outputs:

- To the analog board:
 - analog video RGB, YC, CVBS
 - I2S audio (PCM format)
 - SPDIF audio (digital audio output)
- To the Progressive scan board:
 - digital video YC(7:0).

9.5.3 S2B Interface

The S2B interface between the VSM (IC7100) and the Servo processor MACE3 controls the Basic Engine during record and playback mode.

9.5.4 System Clock

System clocks(27MHz) of VSM, Sti5508, EMPRESS and Progressive Scan are generated by oscillator 7906

9.5.5 Audio Clock

During record mode, the audio clock ACC_ACLK_OSC is generated by IC7102 (PLL) because then, the audio clock must be synchronized with the incoming video (VIP_FID) from the VIP.

During playback mode, the audio clock ACC_ACLK_PLL is generated by the clock synthesizer IC7900 (MK2703S). Both ACC_ACLK_OSC(also goes to the EMPRESS as ACLK_EMP) and ACC_ACLK_PLL are fed to the VSM. This IC selects the appropriate clock to the Sti5508. The EMPRESS IC derives from the incoming ACLK_EMP the I2S audio encoder clocks AE_BCLK and AE_WCLK which are sent to the VSM.

9.5.6 On/Off

The digital board is not powered in standby mode. Control signal ION, coming from the analog board, will enable the PSU and power the digital board.

- ION = High: the digital board is in powered down standby mode
- ION = Low: the power supply to the digital board is enabled

9.5.7 Reset

Control signal IRESET_DIG, controlled by the microprocessor on the analog board is sent to the RESET LOGIC circuit.

- IRESET_DIG = Low in standby mode
- IRESET_DIG = High: the whole system is reset and the Digital board is waked up.

9.5.8 I2C Bus

Sti5508 is master of the I2C bus. The following IC's are controlled by the I2C bus:

- IC7201 NVRAM
- IC7403 EMPRESS
- IC7500 VIP
- IC7700 FLI2200 Video Deinterlacer Line Doubler
- IC7801 ADV7196 Video Denc

9.5.9 EMI Bus

The following IC's are connected to the External Memory Interface bus (EMI) which functions as system bus:

- IC7301 and 7302: Flash memories which contain the application and diagnostic software
- IC7100: VSM
- IC7200: MPEG AV Decoder

9.5.10 Progressive Scan

Description

The progressive scan part is integrated in the Digital Board and built around the SAGE Fli2200 de-interlacer / line doubler (7701). This I2C controlled de-interlacer uses a 64Mbit SDRAM (32bit x 2M) to perform high quality deinterlacing (meshing). The de-interlacer gets his digital YUV input data from the STi5508 (7200). The format of the digital YUV input to the SAGE is CCIR656 with separated Hsync, Vsync and odd/even signal running on 27Mhz.

Because the STi5508 doesn't have a Vsync output the odd/even output of this IC has to be translated to a Vsync signal. Some glue logic has been added to extract the vertical sync. The glue logic circuit consists of Flip-Flop IC 74HC74D (7701) and EXOR 74LVC86 (7702). The next diagram shows how the vertical sync is extracted.

Vertical Sync

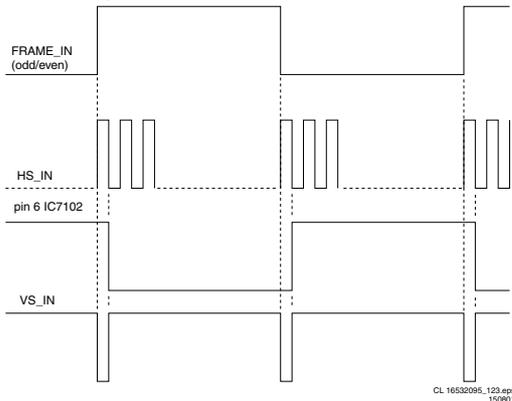


Figure 9-9

The output of the de-interlacer (4:4:4 progressive video) is fed to the Analog Devices ADV71967 MacroVision compliant DENC (7801).

The YUV current output of the DENC is fed via a low pass filter to the single supply output opamps AD8061/8062 (7802-7803). The analog video is fed via a 7 poled flex to the analog board where the YUV 2FH cinch connectors are located.

9.6 Divio Board

9.6.1 Short Description of the Module:

The DVIO Module is a decoder for DV streams. The module is intended for the Philips DVDR1000/002 en DVDR1000/172 DVD+RW recorders. Input is a stream from a DV-camcorder IEEE1394. Outputs are CCIR656 Video and Analog audio (L+R). A serial control interface is present.

The following picture shows the location of the DVIO Module inside the DVDR set.

Description DVIO Module

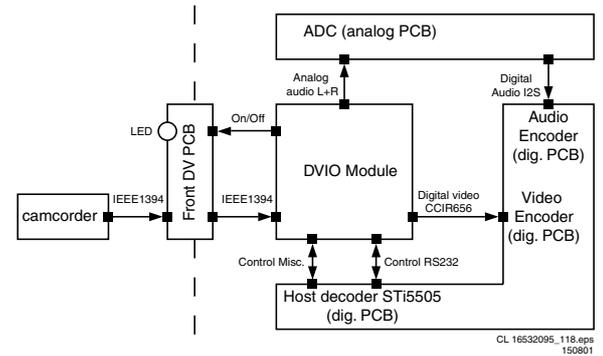
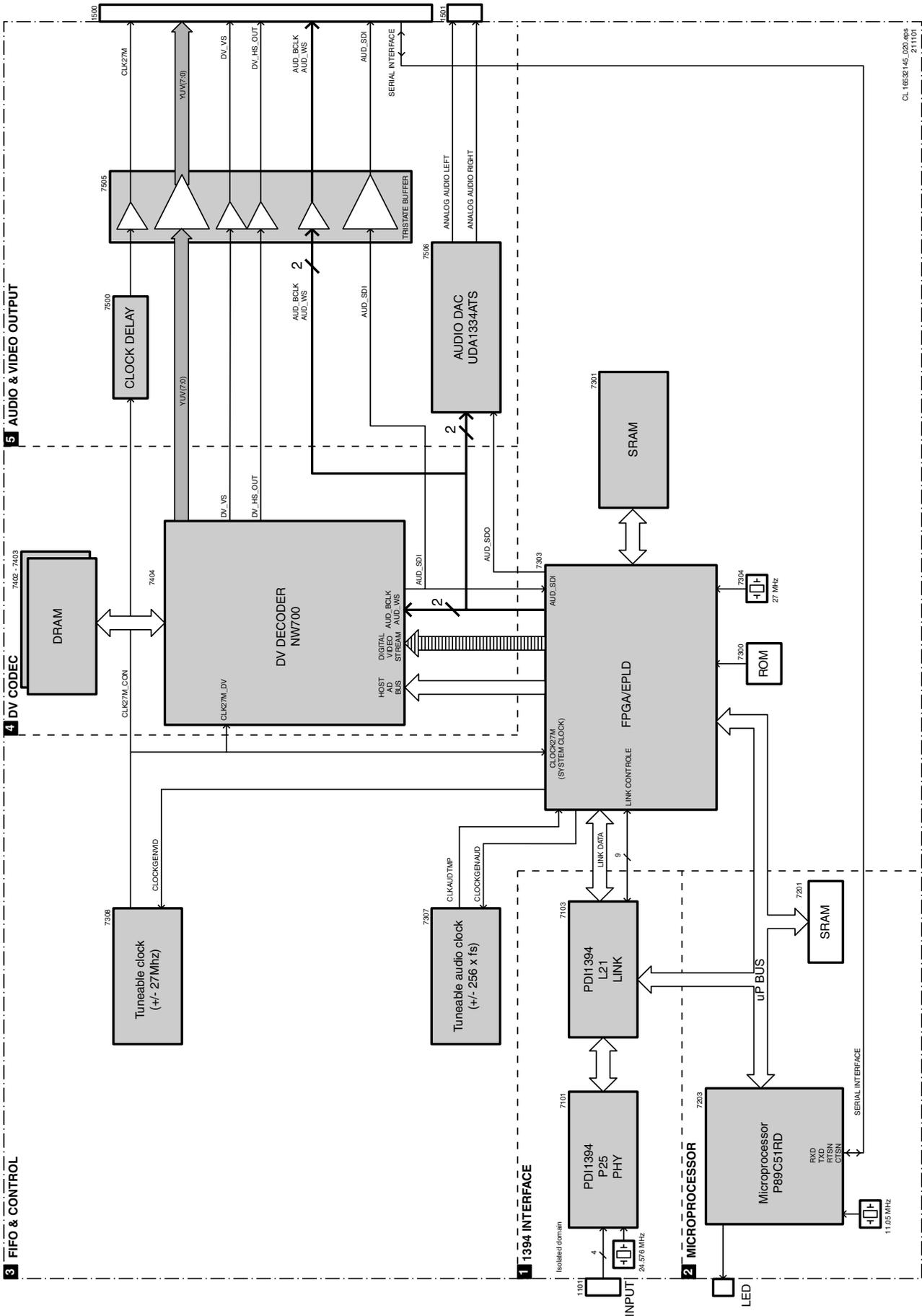


Figure 9-10

9.6.2 Block Diagram

Block Diagram DVIO



Cl. 16532145_020.eps 21110

Figure 9-11

9.6.3 Functional Description

The DVIO module consists of the following blocks (see blockdiagram):

1. IEEE1394 Interface
 - PDI1394P25(7101)
 - PDI1394L40(7103)
2. Micro-controller
 - 89C51RD2(7203)
 - 32kb SRAM(7201)
3. FIFO and Control
 - FPGA/EPLD(7303)
 - SRAM(7301)
 - Clock generation(7307, 7308)
 - Independently tuneable audio and video clock, implemented with FPGA and PLL
4. DV-Decoder
 - NW700(7404)
 - EDO DRAM(7402, 7403)
5. Audio & Video output
 - Audio DAC UDA1334ATS(7602)
 - Clock delay(7500)
 - Tristate buffer(7505)

IEEE1394 Interface

The 1394 interface consists of a PDI1394P25 physical layer and a PDI1394L40 link layer.

It has the following features:

- S200 operation (200 megabit per second)
- One i.Link port (4 pin)
- AV link port

Micro-Controller

The 89C51RD2 processor has a 8051 cpu with the following extra features:

- 64 kilobyte of flash memory as program memory
- 1 kilobyte of internal data memory
- watchdog timer
- PCA outputs
- Power control modes
- Speed allowed up to 33 MHz but used at 11.0592 MHz
- On board ISP(In Circuit Programming) functionality

ISP

By use of In Circuit Programming, it is possible to update the software of the DVIO board that is in the 89C51RD2. ISP can be made active by resetting the processor and keeping the ISPN pin low during reset. During ISP, the ISPN signal on the board has to be kept low. A programming voltage of 5V is always present at the Vpp pin. When the ISP mode is active, the new program can be sent to the microprocessor through the serial port.

Fifo and Control

In decode mode, an isochronous AV-stream is flowing through the IEEE1394 Interface into the FPGA. The FPGA stores the data in a FIFO buffer (ping-pong buffer type, i.e. 2 buffers that can hold one whole frame each).

Reset

The FPGA controls the reset signals on the board. This has the advantage that it is possible to reset the board both from software and hardware.

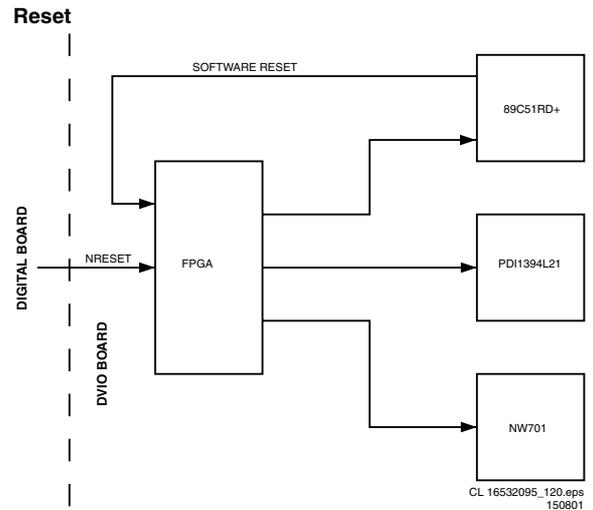


Figure 9-12

The board reset NRESET will reset the whole board, and the software reset can reset everything except the microprocessor itself. Power-on reset is implemented by adding pull-ups and pull-downs to the reset inputs of the devices. Since the FPGA will tri-state all the pins during configuration, reset is active during configuration time. After configuration of the FPGA, the reset signals are driven inactive. The NRESET signal is used to reset the DVIO board. After reset, the tri-state buffers to connector 1500 are disabled.

Clock Circuit

There are 2 clocks to consider in the system, this is the video clock and the audio clock. These two clocks do not have a relation, so these clocks must be considered independently. The video clock is approximately 27 MHz. When data is flowing from an external source that is supposed to have the same frequency, it does not have exactly the same clock. Because of this, buffers may under-run or over-run. Since the clock can not be directly recovered from the 1394 interface, there has to be another solution. This solution is a tuneable clock that is adjusted to the required frequency to process at the rate of the incoming data.

The hardware implementation of such a tuneable clock is as follows:

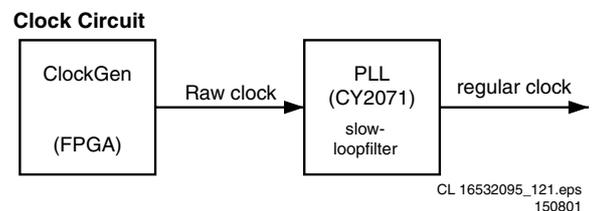


Figure 9-13

The same can be applied for the audio clock. For this clock, a frequency of 8.192 MHz, 11.2896 MHz or 12.228 MHz is required. This depends on the sample-rate frequency(32kHz, 44.1kHz or 48kHz) of the audio signal.

DV Decoder

The AV-data will go from the FIFO to the NW700. The NW700 decodes the stream into video data in 656 format and audio data in I2S format.

The microprocessor has the ability to read the status registers of the NW700 through the FPGA. By reading these registers, extra data from the DV stream, that is not decoded into audio or video, can be sent to the digital board using pin TXD of the serial interface. This data includes time stamp and some more.

Audio & Video Output

The audio I2S data are sent to audio DAC UDA1334. Analog audio left and right signals are connected to the analog board. The tristate buffer enables the digital video stream to the Video Input Processor on the digital board when the DV source is selected.

The clock delay synchronizes the AV clock with the AV data at the output.

9.7 IC's Analog Board

9.7.1 IC7001: UDA1328T

Multi-channel filter DAC

UDA1328T

1 FEATURES

1.1 General

- 2.7 to 3.6 V power supply
- 5 V tolerant TTL compatible inputs
- Selectable control via L3 microcontroller interface or via static pin control
- Multi-channel integrated digital filter plus non-inverting Digital-to-Analog Converter (DAC)
- Supports sample frequencies between 5 and 100 kHz
- Digital silence detection (output)
- Slave mode only applications
- No analog post filtering required for DAC
- Easy application.

1.2 Multiple format input interface

- I²S-bus, MSB-justified and LSB-justified format compatible (in L3 mode)
- I²S-bus and LSB-justified format compatible
- 1f_s input format data rate.

1.3 Multi-channel DAC

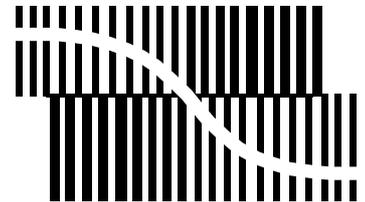
- 6-channel DAC with power on/off control
- Digital logarithmic volume control via L3; volume can be set for each of the channels individually
- Digital de-emphasis for 32, 44.1, 48 and 96 kHz f_s via L3 and, for 32, 44.1 and 48 kHz in static mode
- Soft or quick mute via L3
- Output signal polarity control via L3 microcontroller interface.

1.4 Advanced audio configuration

- 6-channel line output (under L3 volume control)
- A stereo differential output (channel 1 and channel 2) for improved performance
- High linearity, wide dynamic range, low distortion.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1328T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1



BITSTREAM CONVERSION

2 APPLICATIONS

This multi-channel DAC is eminently suitable for DVD-like applications in which 5.1 channel encoded signals are used.

3 GENERAL DESCRIPTION

The UDA1328 is a single-chip 6-channel DAC employing bitstream conversion techniques, which can be used either in L3 microcontroller mode or in static pin mode.

The UDA1328 supports the I²S-bus data format with word lengths of up to 24 bits, the MSB-justified data format with word lengths of up to 24 bits and the LSB-justified serial data format with word lengths of 16, 18, 20 and 24 bits.

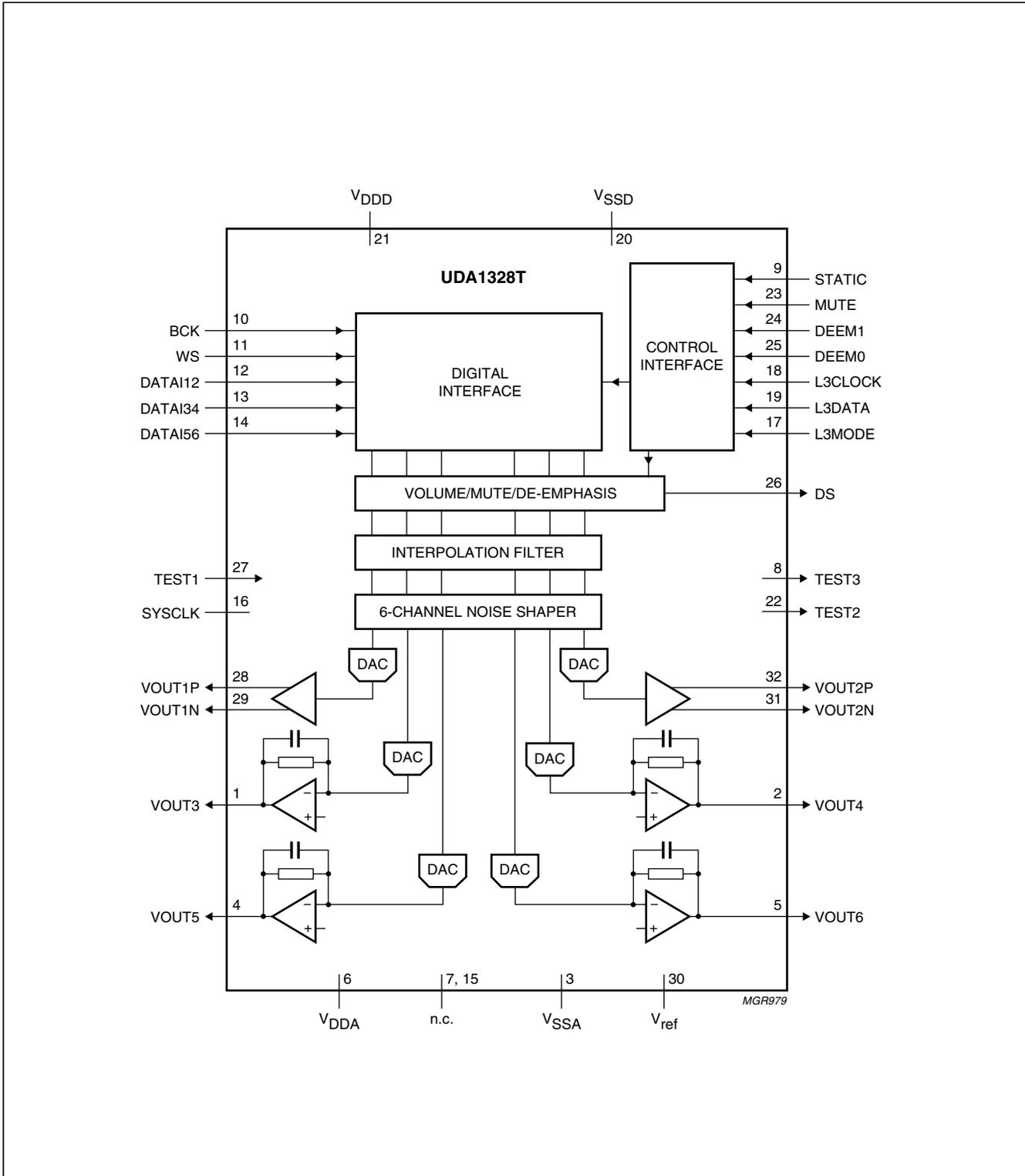
All digital sound processing features can be controlled with the L3 interface e.g. volume control, selecting digital silence type, output polarity control and mute. Also system features such as power control, digital silence detection mode and output polarity control.

Under static pin control, via static pins, the system clock can be set to either 256f_s or 384f_s support, digital de-emphasis can be set, there is digital mute and the digital input formats can also be set.

Multi-channel filter DAC

UDA1328T

6 BLOCK DIAGRAM



Multi-channel filter DAC

UDA1328T

7 PINNING

SYMBOL	PIN	DESCRIPTION
VOUT3	1	channel 3 analog output
VOUT4	2	channel 4 analog output
V _{SSA}	3	analog ground
VOUT5	4	channel 5 analog output
VOUT6	5	channel 6 analog output
V _{DDA}	6	analog supply voltage
n.c.	7	not connected (reserved)
TEST3	8	test output 3
STATIC	9	static mode/L3 mode switch input
BCK	10	bit clock input
WS	11	word select input
DATAI12	12	data input channel 1 and 2
DATAI34	13	data input channel 3 and 4
DATAI56	14	data input channel 5 and 6
n.c.	15	not connected (reserved)
SYSCLK	16	system clock: 256f _s , 384f _s , 512f _s and 768f _s
L3MODE	17	L3 mode selection input
L3CLOCK	18	L3 clock input
L3DATA	19	L3 data input
V _{SSD}	20	digital ground
V _{DDD}	21	digital supply voltage
TEST2	22	test output 2
MUTE	23	static mute control input
DEEM1	24	DEEM control 1 input (static mode)
DEEM0	25	L3 address select (L3 mode)/DEEM control 0 input (static mode)
DS	26	digital silence detect output
TEST1	27	test input 1
VOUT1P	28	channel 1 analog output P
VOUT1N	29	channel 1 analog output N
V _{ref}	30	DAC reference voltage
VOUT2N	31	channel 2 analog output N
VOUT2P	32	channel 2 analog output P

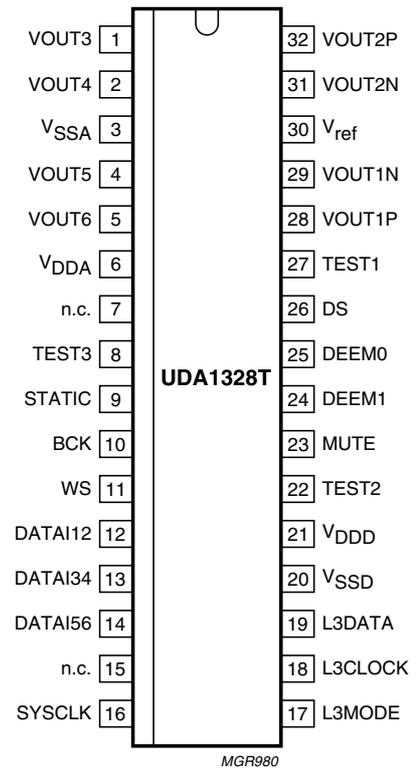


Fig.2 Pin configuration.

Multi-channel PIter DAC

UDA1328T

8 FUNCTIONAL DESCRIPTION

8.1 System clock

The UDA1328 operates in slave mode only, this means that in all applications the system must provide the system clock. The system frequency is selectable. The options are $256f_s$, $384f_s$, $512f_s$ and $768f_s$ for the L3 mode and $256f_s$ or $384f_s$ for the static mode. The system clock must be frequency-locked to the digital interface signals.

It should be noted that the UDA1328 can operate from 5 to 100 kHz sampling frequency (f_s). However in $768f_s$ mode the sampling frequency must be limited to 55 kHz.

8.2 Application modes

Operating mode can be set with the STATIC pin, either to L3 mode (STATIC = LOW) or to the static mode (STATIC = HIGH). See Table 1 for pin functions in the static mode.

Table 1 Mode selection in the static mode

PIN	L3 MODE	STATIC MODE
L3CLOCK	L3CLOCK	clock select
L3MODE	L3MODE	SF1 ⁽¹⁾
L3DATA	L3DATA	SF0 ⁽¹⁾
MUTE	X ⁽²⁾	MUTE
DEEM1	X ⁽²⁾	DEEM1
DEEM0	L3ADR	DEEM0

Notes

- SF1 and SF0 are the Serial Format inputs (2-bit).
- X means that the pin has no function in this mode and can best be connected to ground.

8.3 Interpolation PIter (DAC)

The digital filter interpolates from 1 to $128f_s$ by cascading a half-band filter and a FIR filter, see Table 2. The overall filter characteristic of the digital filters is illustrated in Fig.3, and the pass-band ripple is illustrated in Fig.4. Both figures are with a 44.1 kHz sampling frequency.

Table 2 Interpolation PIter characteristics

ITEM	CONDITION	VALUE (dB)
Pass-band ripple	0 to $0.45f_s$	± 0.02
Stop band	$>0.55f_s$	-55
Dynamic range	0 to $0.45f_s$	>114
DC gain	-	-3.5

8.4 Digital silence detection

The UDA1328 can detect digital silence conditions in channels 1 to 6, and report this via the output pin DS. This function is implemented to allow for external manipulation of the audio signal in the absence of program material, such as muting or recorder control.

An active LOW output is produced at the DS pin if the channels selected via L3 or for all channels in static mode, carries all zeroes for at least 9600 consecutive audio samples (equals 200 ms for $f_s = 48$ kHz). The DS pin is also active LOW when the output is digitally muted either via the L3 interface or via the STATIC pin.

In static mode all channels participate in the digital silence detection. In L3 mode control each channel can be set, either to participate in the digital silence detection or not.

8.5 Noise shaper

The 3rd-order noise shaper operates at $128f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a Filter Stream DAC (FSDAC).

8.6 Filter stream DAC

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. No post-filter is needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales proportionally with the power supply voltage.

8.7 Static mode

The UDA1328 is set to static mode by setting the STATIC pin HIGH. The function of 6 pins of the device now get another function as can be seen in Table 1.

8.7.1 SYSTEM CLOCK SETTING

In static mode pin 18 (L3CLOCK) is used to select the system clock setting. When pin 18 is LOW, the device is in $256f_s$ mode, when pin 18 is HIGH the device is in $384f_s$ mode.

Multi-channel filter DAC

UDA1328T

8.7.2 DE-EMPHASIS CONTROL

In static pin mode the pins DEEM0 and DEEM1 control the de-emphasis mode; see Table 3.

Table 3 De-emphasis control

DEEM MODE	DEEM1	DEEM0
No de-emphasis	0	0
32 kHz de-emphasis	0	1
44.1 kHz de-emphasis	1	0
48 kHz de-emphasis	1	1

8.7.3 DIGITAL INTERFACE FORMATS

In static pin mode the digital audio interface formats can be selected via pin 17 (SF1) and 19 (SF0). The following interface formats can be selected (see also Table 4):

- I²S-bus with data word length of up to 24 bits
- LSB-justified format with data word length of 16, 20 or 24 bits.

Table 4 Input format selection in the static mode

INPUT FORMAT	SF1	SF0
I ² S-bus	0	0
LSB-justified 16 bits	0	1
LSB-justified 20 bits	1	0
LSB-justified 24 bits	1	1

It should be noted that the digital audio interface holds that the BCK frequency can be 64 times the WS maximum frequency, or $f_{BCK} \leq 64 \times f_{WS}$

8.8 L3 mode

The device is set to L3 mode by setting the STATIC pin to LOW. The device can then be controlled via the L3 microcontroller interface (see Chapter 9).

8.8.1 DIGITAL INTERFACE FORMATS

The following interface formats can be selected in the L3 mode:

- I²S-bus with data word length of up to 24 bits
- MSB-justified with data word length of up to 24 bits
- LSB-justified format with data word length of 16, 18, 20 or 24 bits.

8.8.2 L3 ADDRESS

The UDA1328 can be addressed via the L3 microcontroller interface using one of two addresses. This is done in order to individually control the UDA1328 and other Philips DACs or CODECs via the same L3 bus.

The address can be selected using pin 25 (DEEM0) in L3 mode. When pin 25 is set LOW, the address is 000100. When pin 25 is set HIGH the address is 000101.

Low-voltage low-power stereo audio ADC

UDA1360TS

FEATURES

General

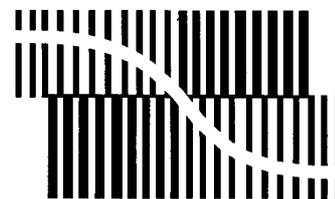
- Low power consumption
- 2.4 to 3.6 V power supply
- Supports 256 and 384f_s system clock
- Supports sampling frequency range of 5 to 55 kHz
- Small package size (SSOP16)
- Integrated high-pass filter to cancel DC offset
- Power-down mode
- Supports 2 V (RMS) input signals
- Easy application
- Non-inverting ADC plus decimation filter.

Multiple format output interface

- I²S-bus and MSB-justified format compatible
- Up to 20 significant bits serial output.

Advanced audio configuration

- Stereo single-ended input configuration
- High linearity, dynamic range and low distortion.



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The UDA1360TS is a single chip stereo Analog-to-Digital Converter (ADC) employing bitstream conversion techniques. The low power consumption and low voltage requirements make the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates recording functions.

The UDA1360TS supports the I²S-bus data format and the MSB-justified data format with word lengths of up to 20 bits.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V _{DDA}	analog supply voltage		2.4	3.0	3.6	V
V _{DDD}	digital supply voltage		2.4	3.0	3.6	V
I _{DDA}	analog supply current		–	9	–	mA
I _{DDD}	digital supply current		–	3.5	–	mA
T _{amb}	operating ambient temperature		–40	–	+85	°C
ADC						
V _{i(rms)}	input voltage (RMS value)	see Table 1	–	1.0	–	V
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB	–	–85	–80	dB
		at –60 dB; A-weighted	–	–37	–33	dB
S/N	signal-to-noise ratio	V ₁ = 0 V; A-weighted	–	97	–	dB
α _{cs}	channel separation		–	100	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1360TS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

Low-voltage low-power stereo audio ADC

UDA1360TS

BLOCK DIAGRAM

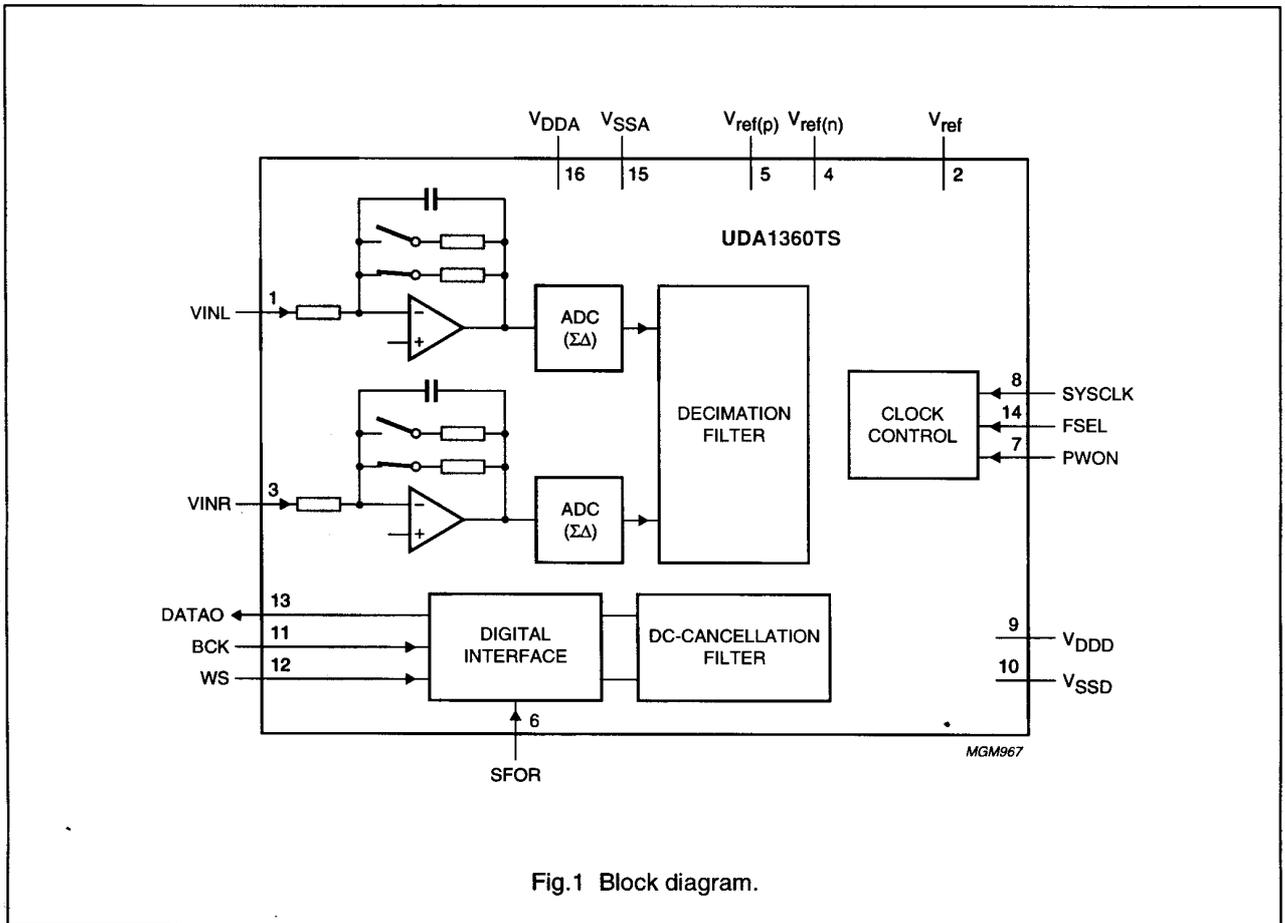


Fig.1 Block diagram.

Low-voltage low-power stereo audio ADC

UDA1360TS

PINNING

SYMBOL	PIN	DESCRIPTION
VINL	1	left channel input
V _{ref}	2	reference voltage
VINR	3	right channel input
V _{ref(n)}	4	ADC negative reference voltage
V _{ref(p)}	5	ADC positive reference voltage
SFOR	6	data format selection input
PWON	7	power control input
SYSCLK	8	system clock input 256 or 384f _s
V _{DDD}	9	digital supply voltage
V _{SSD}	10	digital ground
BCK	11	bit clock input
WS	12	word selection input
DATAO	13	data output
FSEL	14	system clock frequency select
V _{SSA}	15	analog ground
V _{DDA}	16	analog supply voltage

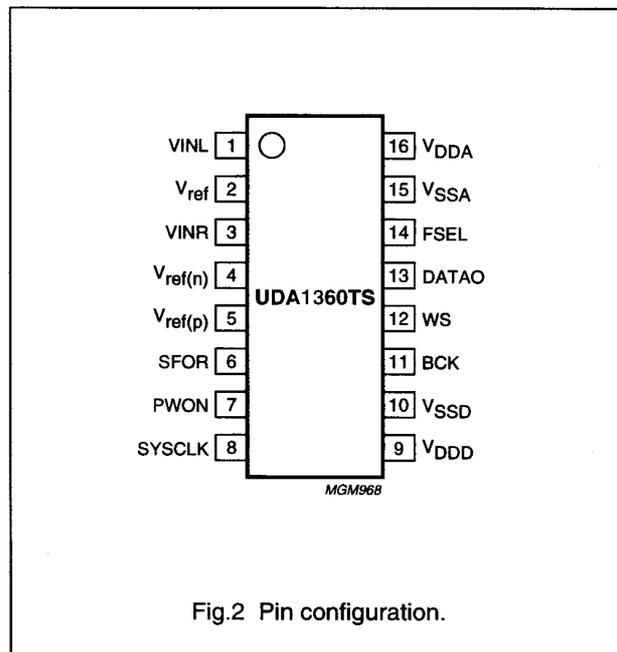


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

System clock

The UDA1360TS accommodates slave mode only, this means that in all applications the system devices must provide the system clock. The system frequency is selectable via the static FSEL pin, and the system clock must be locked in frequency to the digital interface input signals.

The options are 256f_s (FSEL = LOW) and 384f_s (FSEL = HIGH). The sampling frequency range is 5 to 55 kHz.

The BCK clock can be up to 128f_s, or in other words the BCK frequency is 128 times the Word Select (WS) frequency or less: $f_{BCK} \leq 128 \times f_{WS}$.

Notes:

1. The WS edge MUST fall on the negative edge of the BCK at all times for proper operation of the digital I/O data interface.
2. For MSB justified formats it is important to have a WS signal with 50% duty factor.

Analog-to-Digital Converter (ADC)

The stereo ADC of the UDA1360TS consists of two 3rd-order Sigma-Delta modulators. They have a modified Ritchie-coder architecture in a differential switched capacitor implementation. The over-sampling ratio is 128.

Input level

The overall system gain is proportional to V_{DDA}. The 0 dB input level is defined as that which gives a -1 dB FS digital output (relative to the full-scale swing). In addition, an input gain switch is incorporated with the above definitions.

The UDA1360TS front-end is equipped with a selectable 0 or 6 dB gain, in order to supports 2 V (RMS) input using a series resistor of 12 kΩ.

For the definition of the pin settings for 1 or 2 V (RMS) mode given in Table 1, it is assumed that this resistor is present as a default component.

If the 2 V (RMS) signal input is not needed, the external resistor should not be used.

Low-voltage low-power stereo audio ADC

UDA1360TS

Table 1 Application modes using input gain stage

RESISTOR (12 kΩ)	INPUT GAIN SWITCH	MAXIMUM INPUT VOLTAGE
Present	0 dB	2 V (RMS)
Present	6 dB	1 V (RMS)
Absent	0 dB	1 V (RMS)
Absent	6 dB	0.5 V (RMS)

Multiple format output interface

The UDA1360TS supports the following data output formats:

- I²S-bus with data word length of up to 20 bits
- MSB-justified serial format with data word length of up to 20 bits.

The output format can be set by the static SFOR pin. When SFOR is LOW, the I²S-bus is selected, when SFOR is set HIGH the MSB-justified format is selected.

The data formats are illustrated in Fig.4. Left and right data channel words are time multiplexed.

Decimation filter

The decimation from $128f_s$ is performed in two stages. The first stage realizes 3rd-order sin x/x characteristic. This filter decreases the sample rate by 16. The second stage (an FIR filter) consists of 3 half-band filters, each decimating by a factor of 2.

Table 2 DC cancellation filter characteristics

ITEM	CONDITION	VALUE (dB)
Pass-band ripple		none
Pass-band gain		0
Stop band	$>0.55f_s$	-60
Droop	at $0.00045f_s$	0.031
Attenuation at DC	at $0.00000036f_s$	>40
Dynamic range	0 to $0.45f_s$	>110

Mute

On recovery from power-down, the serial data output DATAO is held LOW until valid data is available from the decimation filter. This time tracks with the sampling frequency:

$$t = \frac{12288}{f_s} = 279 \text{ ms ; where } f_s = 44.1 \text{ kHz.}$$

Power-down mode

The PWON pin can control the power saving together with the optional gain switch for 2 V (RMS) or 1 V (RMS) input. When the PWON pin is set LOW, the ADC is set to power-down. When PWON is set to HIGH or to half the power supply, then either 6 dB gain or 0 dB gain in the analog front-end is selected.

Application modes

The UDA1360TS can be set to different modes using two 3-level pins and one 2-level pin. The selection of modes is given in Table 3.

Table 3 Mode selection summary

PIN	V _{SS}	$\frac{1}{2}V_{DD}$	V _{DD}
SFOR	I ² S-bus	test mode	MSB
PWON	power-down	0 dB gain	6 dB gain
FSEL	$256f_s$	-	$384f_s$

3-channel 75Ω driver

BA7660FS

The BA7660FS is a 75Ω driver with a 6dB amplifier and three internal circuits, and provides 75Ω drive of composite Y signals and C signals, as well as RGB signals. Each load is capable of driving two circuits, and a sag correction function reduces the capacitance of the output coupling capacitor.

The input voltage is within a range of 0V to 1.5V, enabling direct connection of ordinary D / A converter output. An internal power-saving circuit is also included which provides simultaneous muting on all three channels, and output pin shorting protection.

●Applications

DVDs, set top boxes and other digital video devices

●Features

- 1) Can be coupled directly to D / A converter output.
- 2) Operates at a low power consumption (115mW typ.).
- 3) Internal output muting circuit.
- 4) Internal power-saving circuit.
- 5) Internal output protection circuit.
- 6) An internal sag correction function makes it possible to reduce the capacitance of the output coupling capacitor.
- 7) Each load is capable of driving two circuits.
- 8) The compact 16-pin SSOP-A package is used.

●Absolute maximum ratings (Ta = 25C)

Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc	8	V
Power dissipation	Pd	650	mW
Operating temperature	Topr	- 25 ~ + 75	°C
Storage temperature	Tstg	- 55 ~ + 125	°C

●Recommended operating conditions (Ta = 25C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating power supply voltage	Vcc	4.5	5.0	5.5	V

●Pin descriptions and input / output circuits

Pin. No	Pin name	IN	OUT	Reference voltage	Equivalent circuit	Function
1	MUTE	K	—	—		<p>Muting control</p> <p>If MUTE (pin 1) is set to HIGH, muting is carried out simultaneously on all three channels.</p>
2 4 7	INA INB INC	K	—	—		<p>Signal input</p> <p>Input signals consist of composite video signals, Y signals, C signals, RGB, and others. The input level is within a range of 0 to 1.3 (min.) to 1.5 (typ.).</p>
3 5 8	GND	—	—	0V		<p>Ground</p>
14 12 9 15 13 10	OUTA2 OUTB2 OUTC2 OUTA1 OUTB1 OUTC1	—	K	0.9V 0.95V		<p>Signal output</p> <p>The signal output level is $(0.9 + 2 \times \text{input voltage [V]})$. Pins 9, 12, and 14 are the pins for sag correction. If pins 10, 13, and 15 are set to 0.2V or less, the protective circuit is triggered and the power-saving mode is accessed.</p>
16	Vcc	—	—	5.0V		<p>Power supply</p>

9.7.4 IC7507: STV6410

STV6410

AUDIO/VIDEO SWITCH MATRIX

- I²C BUS CONTROL
- STANDBY MODE

VIDEO SECTION

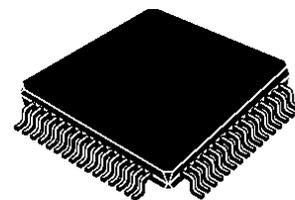
- 5 CVBS INPUTS, 4 CVBS OUTPUTS (ONE WITH SELECTABLE CHROMA TRAP FILTER)
- 5 Y/C INPUTS, 3 Y/C OUTPUTS
- 6dB GAIN ON ALL CVBS/Y AND C OUTPUTS
- 1 Y/C ADDER
- 2 RGB/FB INPUTS, 1 RGB/FB OUTPUT WITH 6dB ADJUSTABLE GAIN
- VIDEO MUTING ON ALL THE OUTPUTS
- 3 SLOW BLANKING INPUTS/OUTPUTS
- SYNC BOTTOM CLAMP ON ALL CVBS/Y AND RGB INPUTS, AVERAGE ON C INPUTS
- BANDWIDTH : 15MHz
- CROSSTALK : 60dB Typ.

AUDIO SECTION

- 5 STEREO INPUTS, 4 STEREO OUTPUTS (TWO WITH LEVEL ADJUSTMENT)
- MONO SOUND OUTPUT
- MONO SOUND CAPABILITY ON TV OUTPUTS
- AUDIO MUTING ON ALL THE OUTPUTS

DESCRIPTION

The STV6410 is a highly integrated I²C bus-controlled audio and video switch matrix, optimized for use in digital set-top box applications. It provides all the audio and video routings required in a full three scart set-top box design. It is also fully pin compatible with STV6411, the two scart version.

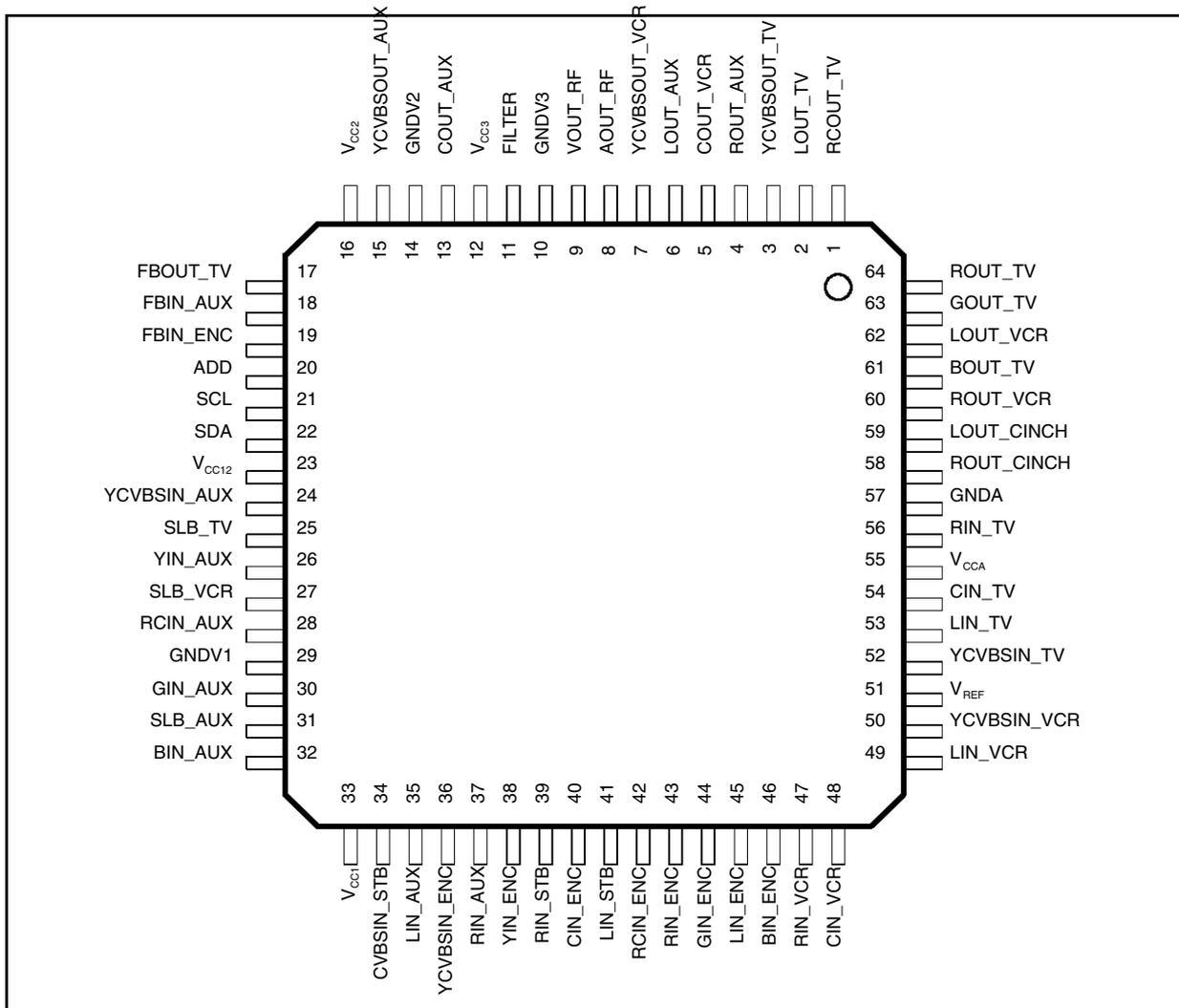


TQFP64
(Plastic Quad Flat Pack)

ORDER CODE : STV6410D

STV6410

PIN CONNECTIONS



6410-01.EPS

PIN LIST

Pin Number	Symbol	Description
1	RCOUT_TV	Red/chroma Output, to TV Scart
2	LOUT_TV	Audio Left Output, to TV Scart
3	YCVBSOUT_TV	Y/CVBS Output, to TV scart
4	ROUT_AUX	Audio Right Output, to AUX Scart
5	COUT_VCR	Chroma Output, to VCR Scart
6	LOUT_AUX	Audio Left Output, to AUX Scart
7	YCVBSOUT_VCR	Y/CVBS Output, to VCR Scart
8	AOUT_RF	Audio (L+R) Output to RF Modulator
9	VOUT_RF	Video (CVBS) Output to RF Modulator
10	GNDV3	Video Switches Ground 3
11	FILTER	Chroma Trap Filter
12	Vccv3	Video Switches Supply 3 (8V)
13	COUT_AUX	Chroma Output, to AUX Scart
14	GNDV2	Video Switches Ground 2
15	YCVBSOUT_AUX	Y/CVBS Output, to AUX Scart

6410-01.TBL

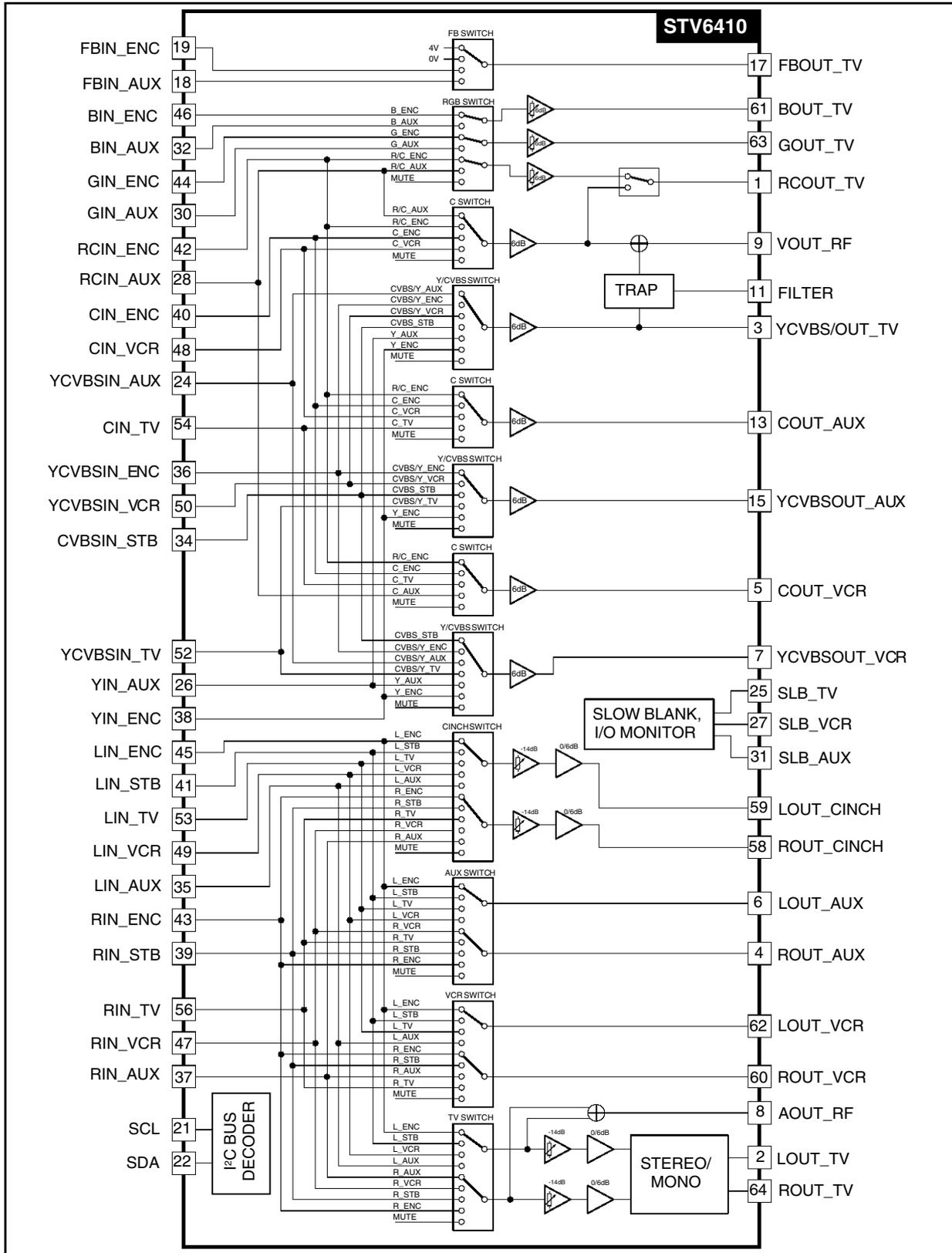
STV6410

PIN LIST (continued)

Pin Number	Symbol	Description
16	V _{CCV2}	Video Switches Supply 2 (8V)
17	FBOU _{TV}	Fast Blanking Output, to TV Scart
18	FBIN _{AUX}	Fast Blanking Input, from AUX Scart
19	FBIN _{ENC}	Fast Blanking Input, from Encoder
20	ADD	I ₂ C Bus IC Address Programming
21	SCL	I ₂ C Bus Clock
22	SDA	I ₂ C Bus Data
23	V _{CC12}	Slow Blanking Power Supply (12V)
24	YCVBSIN _{AUX}	Y/CVBS Input from AUX Scart
25	SLB _{TV}	Slow Blanking Input/Output from TV
26	YIN _{AUX}	Y Input, from AUX Scart
27	SLB _{VCR}	Slow Blanking Input/Output from VCR
28	RCIN _{AUX}	Red/Chroma Input, from AUX Scart
29	GNDV1	Video Switches Ground 1
30	GIN _{AUX}	Green Input, from AUX Scart
31	SLB _{AUX}	Slow Blanking Input/Output from AUX
32	BIN _{AUX}	Blue Input, from AUX Scart
33	V _{CCV1}	Video Switches Supply 1 (8V)
34	CVBSIN _{STB}	CVBS Input from STB
35	LIN _{AUX}	Audio Left Input, from AUX Scart
36	YCVBSIN _{ENC}	Y/CVBS Input from Encoder
37	RIN _{AUX}	Audio Right Input, from AUX Scart
38	YIN _{ENC}	Y Input, from Encoder
39	RIN _{STB}	Audio Right Input, from STB
40	CIN _{ENC}	Chroma Input, from Encoder
41	LIN _{STB}	Audio Left Input, from STB
42	RCIN _{ENC}	Red/Chroma Input, from Encoder
43	RIN _{ENC}	Audio Right Input, from Encoder
44	GIN _{ENC}	Green Input, from Encoder
45	LIN _{ENC}	Audio Left Input, from Encoder
46	BIN _{ENC}	Blue Input, from Encoder
47	RIN _{VCR}	Audio Right Input, from VCR Scart
48	CIN _{VCR}	Chroma Input, from VCR Scart
49	LIN _{VCR}	Audio Left Input, from VCR
50	YCVBSIN _{VCR}	Y/CVBS Input from VCR Scart
51	V _{REF}	Voltage Reference Decoupling
52	YCVBSIN _{TV}	Y/CVBS Input, from TV Scart
53	LIN _{TV}	Audio Left Input, from TV Scart
54	CIN _{TV}	Chroma Input, from TV Scart
55	V _{CCA}	Audio Switches Supply (8V)
56	RIN _{TV}	Audio right input, from TV Scart
57	GND _A	Audio Switches Ground
58	ROUT _{CINCH}	Audio Right Output, to CINCH
59	LOUT _{CINCH}	Audio Left Output, to CINCH
60	ROUT _{VCR}	Audio Right Output, to VCR sCart
61	BOU _{TV}	Blue Output, to TV Scart
62	LOUT _{VCR}	Audio Left Output, to VCR Scart
63	GOU _{TV}	Green Output, to TV Scart
64	ROUT _{TV}	Audio Right Output, to TV Scart

STV6410

BLOCK DIAGRAM



9.7.5 IC7600: MSP3415D

Multistandard Sound Processor Family

Release Note: Revision bars indicate significant changes to the previous edition. The hardware and software description in this document is valid for the MSP 34x5G version B8 and following versions.

1. Introduction

The MSP 34x5G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed in a single chip. Figure 1–1 shows a simplified functional block diagram of the MSP 34x5G.

These TV sound processing ICs include versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free.

Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM-Stereo-Radio standard.

Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and

EIA-J. The MSP 34x5G has optimum stereo performance without any adjustments.

All MSP 34xxG versions are pin compatible to the MSP 34xxD. Only minor modifications are necessary to adapt a MSP 34xxD controlling software to the MSP 34xxG. The MSP 34x5G further simplifies controlling software. Standard selection requires a single I²C transmission only.

Note: The MSP 34x5G version has reduced control registers and less functional pins. The remaining registers are software-compatible to the MSP 34x0G. The pinning is compatible to the MSP 34x0G.

The MSP 34x5G has built-in automatic functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/stereo/bilingual; no I²C interaction is necessary (Automatic Sound Selection).

The MSP 34x5G can handle very high FM deviations even in conjunction with NICAM processing. This is especially important for the introduction of NICAM in China.

The ICs are produced in submicron CMOS technology. The MSP 34x5G is available in the following packages: PSDIP64, PSDIP52, PMQFP44, PLQFP64, and PQFP80.

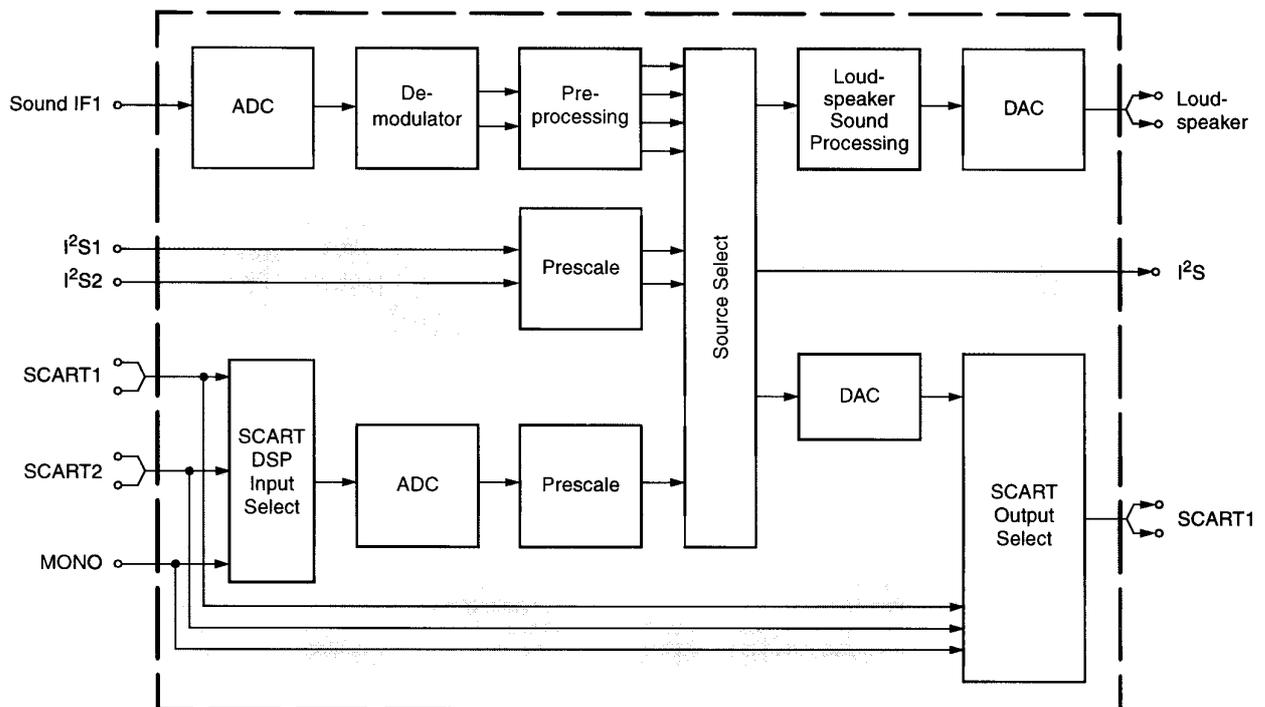


Fig. 1–1: Simplified functional block diagram of MSP 34x5G

2. Functional Description

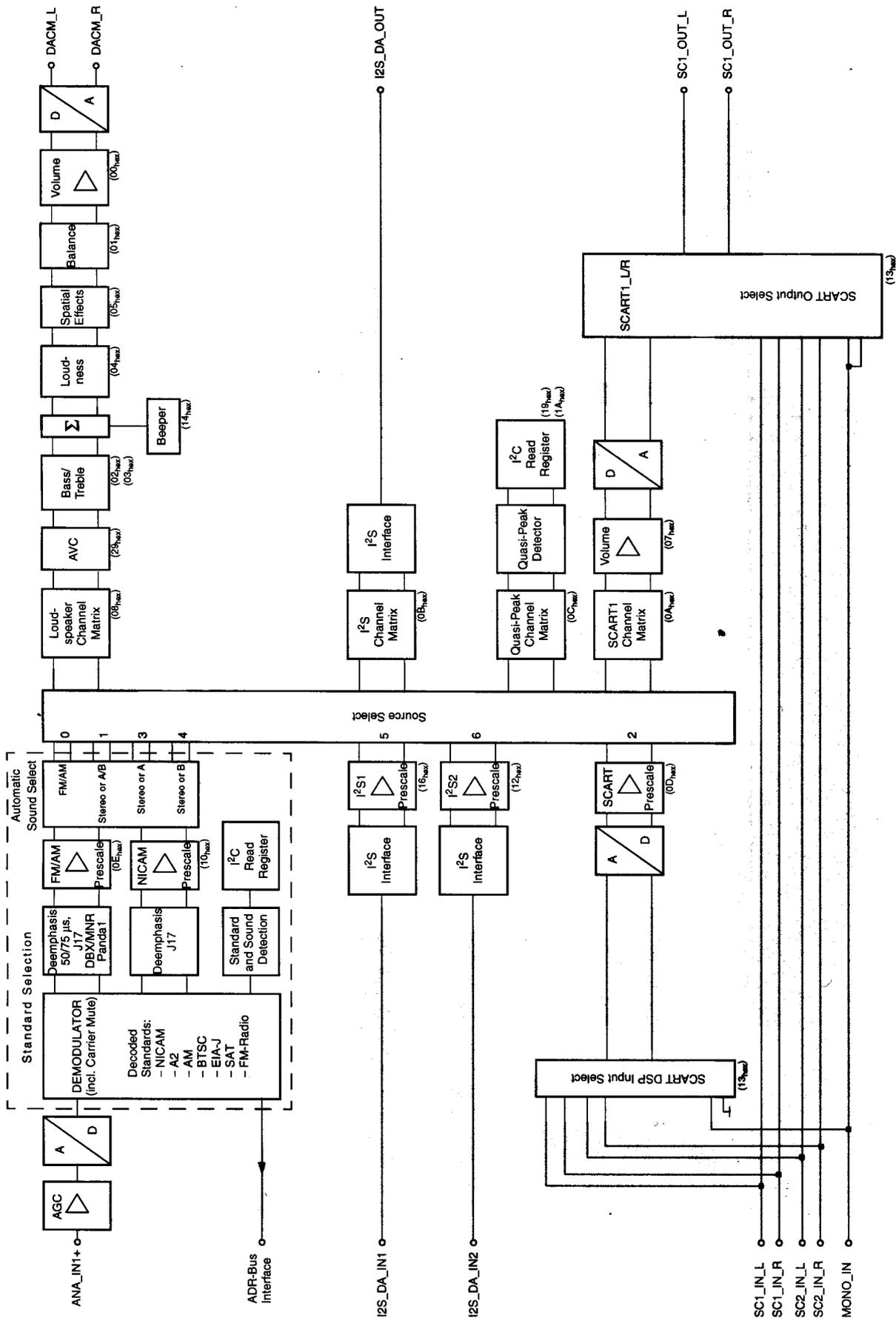


Fig. 2-1: Signal flow diagram of the MSP 34x5G (input and output names correspond to pin names).

2.1. Architecture of the MSP 34x5G Family

Fig. 2–1 on page 8 shows a simplified block diagram of the IC. The block diagram contains all features of the MSP 3455G. Other members of the MSP 34x5G family do not have the complete set of features: The demodulator handles only a subset of the standards presented in the demodulator block; NICAM processing is only possible in the MSP 3415G and MSP 3455G (see dashed block in Fig. 2–1).

2.2. Sound IF Processing

2.2.1. Analog Sound IF Input

The input pins ANA_IN1+ and ANA_IN– offer the possibility to connect sound IF (SIF) sources to the MSP 34x5G. The analog-to-digital conversion of the preselected sound IF signal is done by an A/D-converter. An analog automatic gain circuit (AGC) allows a wide range of input levels. The high-pass filter formed by the coupling capacitor at pin ANA_IN1+ (see Section 7. “Appendix D: Application Information” on page 92) is sufficient in most cases to suppress video components. Some combinations of SAW filters and sound IF mixer ICs, however, show large picture components on their outputs. In this case, further filtering is recommended.

2.2.2. Demodulator: Standards and Features

The MSP 34x5G is able to demodulate all TV sound standards worldwide including the digital NICAM system. Depending on the MSP 34x5G version, the following demodulation modes can be performed:

A2-Systems: Detection and demodulation of two separate FM carriers (FM1 and FM2), demodulation and evaluation of the identification signal of carrier FM2.

NICAM-Systems: Demodulation and decoding of the NICAM carrier, detection and demodulation of the analog (FM or AM) carrier. For D/K-NICAM, the FM carrier may have a maximum deviation of 384 kHz.

Very high deviation FM-Mono: Detection and robust demodulation of one FM carrier with a maximum deviation of 540 kHz.

BTSC-Stereo: Detection and FM demodulation of the aural carrier resulting in the MTS/MPX signal. Detection and evaluation of the pilot carrier, AM demodulation of the (L-R)-carrier and detection of the SAP sub-carrier. Processing of the DBX noise reduction or Micronas Noise Reduction (MNR).

BTSC-Mono + SAP: Detection and FM demodulation of the aural carrier resulting in the MTS/MPX signal. Detection and evaluation of the pilot carrier, detection and FM demodulation of the SAP-subcarrier. Processing of the DBX noise reduction or Micronas Noise Reduction (MNR).

Japan Stereo: Detection and FM demodulation of the aural carrier resulting in the MPX signal. Demodulation and evaluation of the identification signal and FM demodulation of the (L-R)-carrier.

FM-Satellite Sound: Demodulation of one or two FM carriers. Processing of high-deviation mono or narrow bandwidth mono, stereo, or bilingual satellite sound according to the ASTRA specification.

FM-Stereo-Radio: Detection and FM demodulation of the aural carrier resulting in the MPX signal. Detection and evaluation of the pilot carrier and AM demodulation of the (L-R)-carrier.

The demodulator blocks of all MSP 34x5G versions have identical user interfaces. Even completely different systems like the BTSC and NICAM systems are controlled the same way. Standards are selected by means of MSP Standard Codes. Automatic processes handle standard detection and identification without controller interaction. The key features of the MSP 34x5G demodulator blocks are

Standard Selection: The controlling of the demodulator is minimized: All parameters, such as tuning frequencies or filter bandwidth, are adjusted automatically by transmitting one single value to the STANDARD SELECT register. For all standards, specific MSP standard codes are defined.

Automatic Standard Detection: If the TV sound standard is unknown, the MSP 34x5G can automatically detect the actual standard, switch to that standard, and respond the actual MSP standard code.

Automatic Carrier Mute: To prevent noise effects or FM identification problems in the absence of an FM carrier, the MSP 34x5G offers a configurable carrier mute feature, which is activated automatically if the TV sound standard is selected by means of the STANDARD SELECT register. If no FM carrier is detected at one of the two MSP demodulator channels, the corresponding demodulator output is muted. This is indicated in the STATUS register.

2.2.3. Preprocessing of Demodulator Signals

The NICAM signals must be processed by a deemphasis filter and adjusted in level. The analog demodulated signals must be processed by a deemphasis filter, adjusted in level, and dematrixed. The correct deemphasis filters are already selected by setting the standard in the STANDARD SELECT register. The level adjustment has to be done by means of the FM/AM and NICAM prescale registers. The necessary dematrix function depends on the selected sound standard and the actual broadcasted sound mode (mono, stereo, or bilingual). It can be manually set by the FM Matrix Mode register or automatically by the Automatic Sound Selection.

2.2.4. Automatic Sound Select

In the Automatic Sound Select mode, the dematrix function is automatically selected based on the identification information in the STATUS register. No I²C interaction is necessary when the broadcasted sound mode changes (e.g. from mono to stereo).

The demodulator supports the identification check by switching between mono-compatible standards (standards that have the same FM-Mono carrier) automatically and non-audible. If B/G-FM or B/G-NICAM is selected, the MSP will switch between these standards. The same action is performed for the standards: D/K1-FM, D/K2-FM, and D/K-NICAM. Switching is only done in the absence of any stereo or bilingual identification. If identification is found, the MSP keeps the detected standard.

In case of high bit-error rates, the MSP 34x5G automatically falls back from digital NICAM sound to analog FM or AM mono.

Table 2-1 summarizes all actions that take place when Automatic Sound Select is switched on.

To provide more flexibility, the Automatic Sound Select block prepares four different source channels of demodulated sound (Fig. 2-2). By choosing one of the four demodulator channels, the preferred sound mode can be selected for each of the output channels (loudspeaker, headphone, etc.). This is done by means of the Source Select registers.

The following source channels of demodulated sound are defined:

- **“FM/AM” channel:** Analog mono sound, stereo if available. In case of NICAM, analog mono only (FM or AM mono).
- **“Stereo or A/B” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains both languages A (left) and B (right).

- **“Stereo or A” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains language A (on left and right).
- **“Stereo or B” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains language B (on left and right).

Fig. 2-2 and Table 2-2 show the source channel assignment of the demodulated signals in case of Automatic Sound Select mode for all sound standards.

Note: The analog primary input channel contains the signal of the mono FM/AM carrier or the L+R signal of the MPX carrier. The secondary input channel contains the signal of the 2nd FM carrier, the L-R signal of the MPX carrier, or the SAP signal.

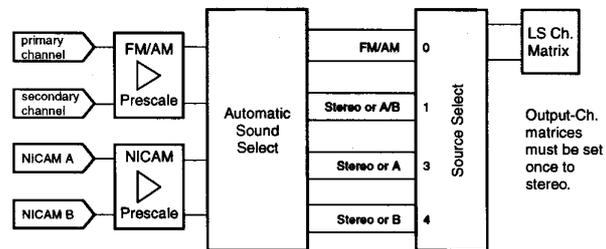


Fig. 2-2: Source channel assignment of demodulated signals in Automatic Sound Select Mode

2.2.5. Manual Mode

Fig. 2-3 shows the source channel assignment of demodulated signals in case of manual mode. If manual mode is required, more information can be found in Section 6.7. “Demodulator Source Channels in Manual Mode” on page 90.

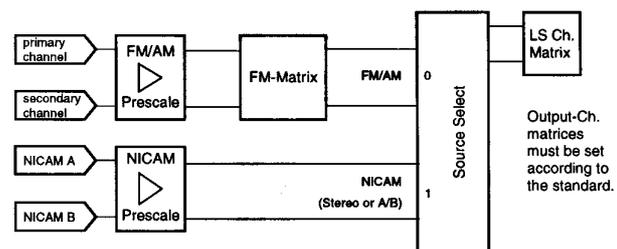


Fig. 2-3: Source channel assignment of demodulated signals in Manual Mode

2.3. Preprocessing for SCART and I²S Input Signals

The SCART and I²S inputs need only be adjusted in level by means of the SCART and I²S prescale registers.

2.4. Source Selection and Output Channel Matrix

The Source Selector makes it possible to distribute all source signals (one of the demodulator source channels or SCART) to the desired output channels (loudspeaker, etc.). All input and output signals can be processed simultaneously. Each source channel is identified by a unique source address.

For each output channel, the sound mode can be set to sound A, sound B, stereo, or mono by means of the output channel matrix.

If Automatic Sound Select is on, the output channel matrix can stay fixed to stereo (transparent) for demodulated signals.

2.5. Audio Baseband Processing

2.5.1. Automatic Volume Correction (AVC)

Different sound sources (e.g. terrestrial channels, SAT channels, or SCART) fairly often do not have the same volume level. Advertisements during movies usually have a higher volume level than the movie itself. This results in annoying volume changes. The AVC solves this problem by equalizing the volume level.

To prevent clipping, the AVC's gain decreases quickly in dynamic boost conditions. To suppress oscillation effects, the gain increases rather slowly for low level inputs. The decay time is programmable by means of the AVC register (see page 30).

For input signals ranging from -24 dB_r to 0 dB_r, the AVC maintains a fixed output level of -18 dB_r. Fig. 2-4 shows the AVC output level versus its input level. For prescale and volume registers set to 0 dB, a level of 0 dB_r corresponds to full scale input/output. This is

- SCART input/output 0 dB_r = 2.0 V_{rms}
- Loudspeaker output 0 dB_r = 1.4 V_{rms}

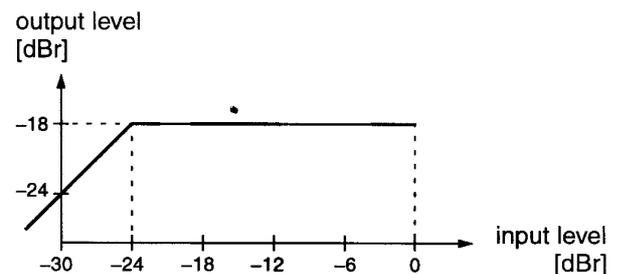


Fig. 2-4: Simplified AVC characteristics

2.5.2. Loudspeaker Outputs

The following baseband features are implemented in the loudspeaker output channels: bass/treble, loudness, balance, and volume. A square wave beeper can be added to the loudspeaker channel.

2.5.3. Quasi-Peak Detector

The quasi-peak readout register can be used to read out the quasi-peak level of any input source. The feature is based on following filter time constants:

- attack time: 1.3 ms
- decay time: 37 ms

2.6. SCART Signal Routing

2.6.1. SCART DSP In and SCART Out Select

The SCART DSP Input Select and SCART Output Select blocks include full matrix switching facilities. To design a TV set with two pairs of SCART-inputs and one pair of SCART-outputs, no external switching hardware is required. The switches are controlled by the ACB user register (see page 34).

2.6.2. Stand-by Mode

If the MSP 34x5G is switched off by first pulling STANDBYQ low and then (after >1 μ s delay) switching off DVSUP and AVSUP, but keeping AHVSUP ('Stand-by'-mode), the SCART switches maintain their position and function. This allows the copying from selected SCART-inputs to SCART-outputs in the TV set's stand-by mode.

In case of power on or starting from stand-by (switching on the DVSUP and AVSUP, RESETQ going high 2 ms later), all internal registers except the ACB register (page 34) are reset to the default configuration (see Table 3-5 on page 18). The reset position of the ACB register becomes active after the first I²C transmission into the Baseband Processing part. By transmitting the ACB register first, the reset state can be redefined.

2.7. I²S Bus Interface

The MSP 34x5G has a synchronous master/slave input/output interface running on 32 kHz.

The interface accepts two formats:

1. I²S_WS changes at the word boundary
2. I²S_WS changes one I²S-clock period before the word boundaries.

All I²S options are set by means of the MODUS and the I2S_CONFIG registers.

The I²S bus interface consists of five pins:

- I2S_DA_IN1, I2S_DA_IN2:
I²S serial data input: 16, 18...32 bits per sample
- I2S_DA_OUT:
I²S serial data output: 16, 18...32 bits per sample
- I2S_CL:
I²S serial clock
- I2S_WS:
I²S word strobe signal defines the left and right sample

If the MSP 34x5G serves as the master on the I²S interface, the clock and word strobe lines are driven by the IC. In this mode, only 16 or 32 bits per sample can be selected. In slave mode, these lines are input to the IC and the MSP clock is synchronized to 576 times the I2S_WS rate (32 kHz). NICAM operation is not possible in slave mode.

An I²S timing diagram is shown in Fig. 4-28 on page 62.

2.8. ADR Bus Interface

For the ASTRA Digital Radio System (ADR), the MSP 3405G, MSP 3415G, and MSP 3455G performs preprocessing such as carrier selection and filtering. Via the 3-line ADR-bus, the resulting signals are transferred to the DRP 3510A coprocessor, where the source decoding is performed. To be prepared for an upgrade to ADR with an additional DRP board, the following lines of MSP 34x5G should be provided on a feature connector:

- I2S_DA_IN1 or I2S_DA_IN2
- I2S_DA_OUT
- I2S_WS
- I2S_CL
- ADR_CL, ADR_WS, ADR_DA

For more details, please refer to the DRP 3510A data sheet.

2.9. Digital Control I/O Pins and Status Change Indication

The static level of the digital input/output pins D_CTR_I/O_0/1 is switchable between HIGH and LOW via the I²C-bus by means of the ACB register (see page 34). This enables the controlling of external hardware switches or other devices via I²C-bus.

The digital input/output pins can be set to high impedance by means of the MODUS register (see page 23). In this mode, the pins can be used as input. The current state can be read out of the STATUS register (see page 25).

Optionally, the pin D_CTR_I/O_1 can be used as an interrupt request signal to the controller, indicating any changes in the read register STATUS. This makes polling unnecessary; I²C-bus interactions are reduced to a minimum (see STATUS register on page 25 and MODUS register on page 23).

2.10. Clock PLL Oscillator and Crystal Specifications

The MSP 34x5G derives all internal system clocks from the 18.432 MHz oscillator. In NICAM or in I²S-Slave mode, the clock is phase-locked to the corresponding source. Therefore, it is not possible to use NICAM and I²S-Slave mode at the same time.

For proper performance, the MSP clock oscillator requires a 18.432-MHz crystal. Note, that for the phase-locked mode (NICAM, I²S slave), crystals with tighter tolerance are required.

4.2. Pin Connections and Short Descriptions

NC = not connected; leave vacant

LV = if not used, leave vacant

DVSS: if not used, connect to DVSS

X = obligatory; connect as described in circuit diagram

AHVSS: connect to AHVSS

Pin No.					Pin Name	Type	Connection (if not used)	Short Description
PQFP 80-pin	PLQFP 64-pin	PMQFP 44-pin	PSDIP 64-pin	PSDIP 52-pin				
1	64	–	8	–	NC		LV	Not connected
2	1	12	9	7	I ² C_CL	IN/OUT	X	I ² C clock
3	2	13	10	8	I ² C_DA	IN/OUT	X	I ² C data
4	3	14	11	9	I ² S_CL		LV	I ² S clock
5	4	15	12	10	I ² S_WS		LV	I ² S word strobe
6	5	16	13	11	I ² S_DA_OUT		LV	I ² S data output
7	6	17	14	12	I ² S_DA_IN1		LV	I ² S1 data input
8	7	–	15	13	ADR_DA		LV	ADR data output
9	8	–	16	14	ADR_WS		LV	ADR word strobe
10	9	18	17	15	ADR_CL		LV	ADR clock
11	–	–	–	–	DVSUP		X	Digital power supply +5 V
12	–	–	–	–	DVSUP		X	Digital power supply +5 V
13	10	19	18	16	DVSUP		X	Digital power supply +5 V
14	–	20	–	–	DVSS		X	Digital ground
15	–	–	–	–	DVSS		X	Digital ground
16	11	–	19	17	DVSS		X	Digital ground
17	12	21	20	18	I ² S_DA_IN2		LV	I ² S2-data input
18	13	–	21	19	NC		LV	Not connected
19	14	–	22	–	NC		LV	Not connected
20	15	–	23	–	NC		LV	Not connected
21	16	22	24	20	RESETQ	IN	X	Power-on-reset
22	–	–	–	–	NC		LV	Not connected
23	–	–	–	–	NC		LV	Not connected
24	17	23	25	21	NC		LV	Not connected
25	18	24	26	22	NC		LV	Not connected

	Pin No.					Pin Name	Type	Connection (if not used)	Short Description
	PQFP 80-pin	PLQFP 64-pin	PMQFP 44-pin	PSDIP 64-pin	PSDIP 52-pin				
26	19	25	27	23	VREF2		X	Reference ground 2 high-voltage part	
27	20	26	28	24	DACM_R	OUT	LV	Loudspeaker out, right	
28	21	27	29	25	DACM_L	OUT	LV	Loudspeaker out, left	
29	22	–	30	–	NC		LV	Not connected	
30	23	–	31	26	NC		LV	Not connected	
31	24	–	32	–	NC		LV	Not connected	
32	–	–	–	–	NC		LV	Not connected	
33	25	–	33	27	NC		LV	Not connected	
34	26	28	34	28	NC		LV	Not connected	
35	27	29	35	29	VREF1		X	Reference ground 1 high-voltage part	
36	28	30	36	30	SC1_OUT_R	OUT	LV	SCART 1 output, right	
37	29	31	37	31	SC1_OUT_L	OUT	LV	SCART 1 output, left	
38	30	32	38	32	NC		LV	Not connected	
39	31	33	39	33	AHVSUP		X	Analog power supply 8.0 V	
40	32	34	40	34	CAPL_M		X	Volume capacitor MAIN	
41	–	–	–	–	NC		LV	Not connected	
42	–	–	–	–	NC		LV	Not connected	
43	–	–	–	–	AHVSS		X	Analog ground	
44	33	35	41	35	AHVSS		X	Analog ground	
45	34	36	42	36	AGNDC		X	Analog reference voltage high-voltage part	
46	–	–	–	–	NC		LV	Not connected	
47	35	–	43	–	NC		LV	Not connected	
48	36	–	44	–	NC		LV	Not connected	
49	37	–	45	–	NC		LV	Not connected	
50	38	–	46	37	NC		LV	Not connected	
51	39	–	47	38	NC		LV	Not connected	
52	40	–	48	–	NC		AHVSS	Analog Shield Ground	
53	41	37	49	39	SC2_IN_L	IN	LV	SCART 2 input, left	
54	42	38	50	40	SC2_IN_R	IN	LV	SCART 2 input, right	

PQFP 80-pin	Pin No.				Pin Name	Type	Connection (if not used)	Short Description
	PLQFP 64-pin	PMQFP 44-pin	PSDIP 64-pin	PSDIP 52-pin				
55	43	39	51	–	ASG		AHVSS	Analog Shield Ground
56	44	40	52	41	SC1_IN_L	IN	LV	SCART 1 input, left
57	45	41	53	42	SC1_IN_R	IN	LV	SCART 1 input, right
58	46	42	54	43	VREFTOP		X	Reference voltage IF A/D converter
59	–	–	–	–	NC		LV	Not connected
60	47	43	55	44	MONO_IN	IN	LV	Mono input
61	–	–	–	–	AVSS		X	Analog ground
62	48	44	56	45	AVSS		X	Analog ground
63	–	–	–	–	NC		LV	Not connected
64	–	–	–	–	NC		LV	Not connected
65	–	–	–	–	AVSUP		X	Analog power supply +5 V
66	49	1	57	46	AVSUP		X	Analog power supply +5 V
67	50	2	58	47	ANA_IN1+	IN	LV	IF input 1
68	51	3	59	48	ANA_IN–	IN	LV	IF common
69	52	–	60	49	NC		LV	Not connected
70	53	4	61	50	TESTEN	IN	X	Test pin
71	54	5	62	51	XTAL_IN	IN	X	Crystal oscillator
72	55	6	63	52	XTAL_OUT	OUT	X	Crystal oscillator
73	56	7	64	1	TP		LV	Test pin
74	57	–	1	2	NC		LV	Not connected
75	58	–	2	–	NC		LV	Not connected
76	59	–	3	–	NC		LV	Not connected
77	60	8	4	3	D_CTR_I/O_1	IN/OUT	LV	D_CTR_I/O_1
78	61	9	5	4	D_CTR_I/O_0	IN/OUT	LV	D_CTR_I/O_0
79	62	10	6	5	ADR_SEL	IN	X	I ² C Bus address select
80	63	11	7	6	STANDBYQ	IN	X	Standby (low-active)

Single/multistandard VIF/SIF-PLL and FM-PLL/AM demodulators

TDA9817; TDA9818

FEATURES

- 5 V supply voltage
- Applicable for IFs (Intermediate Frequencies) of 38.9 MHz, 45.75 MHz and 58.75 MHz
- Gain controlled wide band Video IF (VIF)-amplifier (AC-coupled)
- True synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
- Robustness for over-modulation better than 105% due to gated phase detector at L/L accent standard and PLL-bandwidth control at negative modulated standards
- VCO (Voltage Controlled Oscillator) frequency switchable between L and L accent (alignment external) picture carrier frequency
- VIF AGC (Automatic Gain Control) detector for gain control, operating as peak sync detector for B/G, peak white detector for L; signal controlled reaction time for L
- Tuner AGC with adjustable TakeOver Point (TOP)
- AFC (Automatic Frequency Control) detector without extra reference circuit

- AC-coupled limiter amplifier for sound intercarrier signal
- Alignment-free FM PLL (Phase Locked Loop) demodulator with high linearity
- SIF (Sound IF) input for single reference QSS (Quasi Split Sound) mode (PLL controlled); SIF AGC detector for gain controlled SIF amplifier; single reference QSS mixer able to operate in high performance single reference QSS mode and in intercarrier mode
- AM demodulator without extra reference circuit
- Stabilizer circuit for ripple rejection and to achieve constant output signals
- ESD (Electrostatic Discharge) protection for all pins.

GENERAL DESCRIPTION

The TDA9817 is an integrated circuit for single standard vision IF signal processing and FM demodulation.

The TDA9818 is an integrated circuit for multistandard vision IF signal processing, sound AM and FM demodulation.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9817	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1
TDA9818	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1

Single/multistandard VIF/SIF-PLL and FM-PLL/AM demodulators

TDA9817; TDA9818

BLOCK DIAGRAM

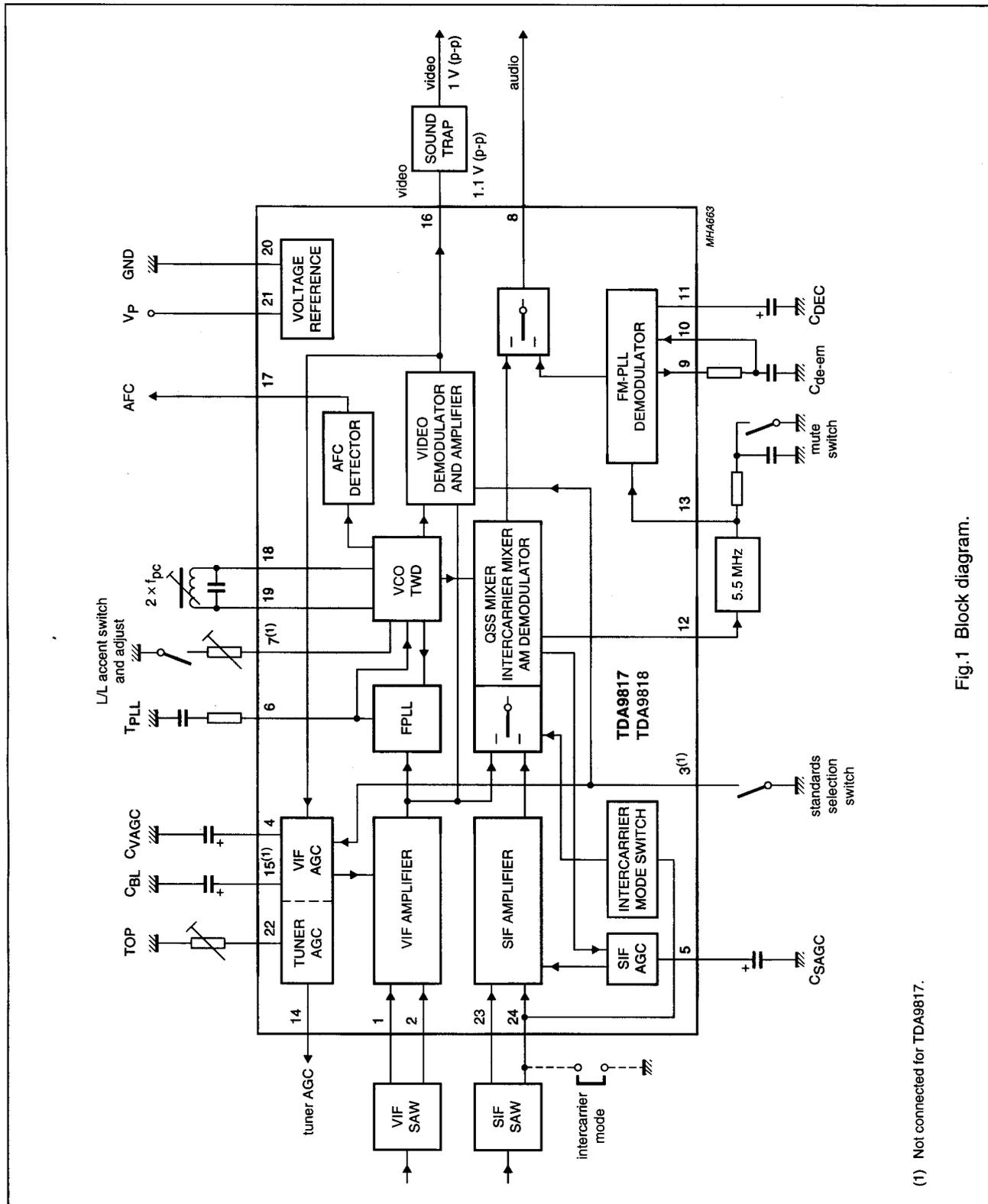


Fig.1 Block diagram.

(1) Not connected for TDA9817.

Single/multistandard VIF/SIF-PLL and FM-PLL/AM demodulators

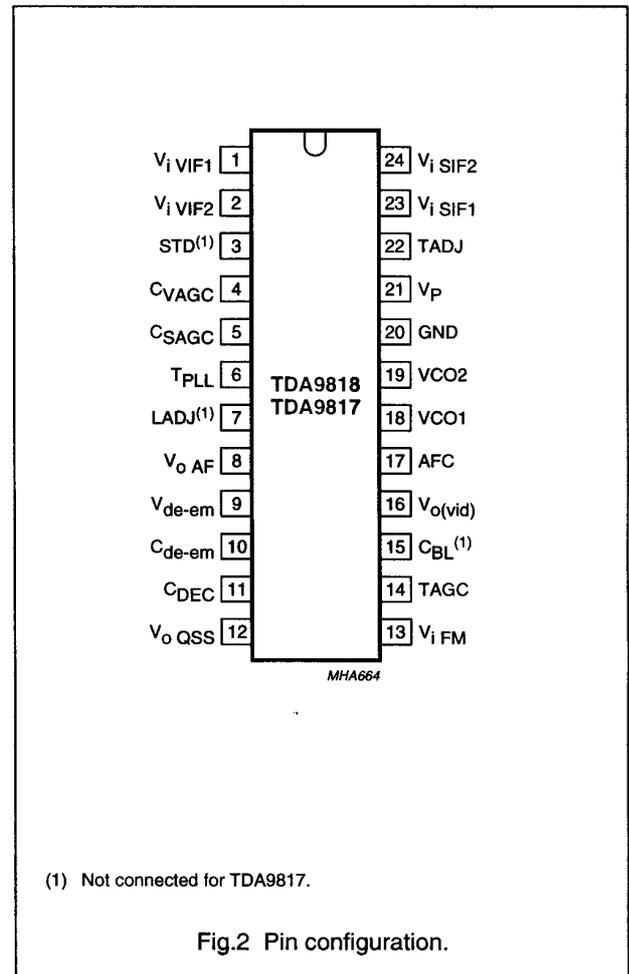
TDA9817; TDA9818

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i\ VIF1}$	1	VIF differential input signal voltage 1
$V_{i\ VIF2}$	2	VIF differential input signal voltage 2
STD ⁽¹⁾	3	standard switch
C_{VAGC}	4	VIF AGC capacitor
C_{SAGC}	5	SIF AGC capacitor
T_{PLL}	6	PLL loop filter
LADJ ⁽¹⁾	7	L/L accent switch and adjust
$V_{o\ AF}$	8	audio output
V_{de-em}	9	de-emphasis input
C_{de-em}	10	de-emphasis output
C_{DEC}	11	decoupling capacitor
$V_{o\ QSS}$	12	single reference QSS/intercarrier output voltage
$V_{i\ FM}$	13	sound intercarrier input voltage
TAGC	14	tuner AGC output
C_{BL} ⁽¹⁾	15	black level detector
$V_{o(vid)}$	16	composite video output voltage
AFC	17	AFC output
VCO1	18	VCO1 resonance circuit
VCO2	19	VCO2 resonance circuit
GND	20	ground
V_P	21	supply voltage
TADJ	22	tuner AGC takeover point adjust
$V_{i\ SIF1}$	23	SIF differential input signal voltage 1
$V_{i\ SIF2}$	24	SIF differential input signal voltage 2

Note

1. Not connected for TDA9817.



Single/multistandard VIF/SIF-PLL and FM-PLL/AM demodulators

TDA9817; TDA9818

FUNCTIONAL DESCRIPTION

The integrated circuit comprises the functional blocks as shown in Fig.1:

- Vision IF amplifier and VIF AGC detector
- Tuner AGC
- Frequency Phase Locked Loop detector (FPLL)
- VCO, Travelling Wave Divider (TWD) and AFC
- Video demodulator and amplifier
- SIF amplifier and SIF AGC
- Single reference QSS mixer
- AM demodulator
- FM-PLL demodulator
- AF (Audio Frequency) signal processing
- Internal voltage stabilizer.

Vision IF amplifier and VIF AGC detector

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Each differential stage comprises a feedback network controlled by emitter degeneration.

The AGC detector generates the required VIF gain control voltage for constant video output by charging/discharging the AGC capacitor. Therefore for negative video modulation the sync level and for positive video modulation the peak white level of the video signal is detected. In order to reduce the reaction time for positive modulation, where a very large time constant is needed, an additional level detector increases the discharging current of the AGC capacitor (fast mode) in the event of a decreasing VIF amplitude step. The additional level information is given by the black-level detector voltage.

Tuner AGC

The AGC capacitor voltage is converted to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current at pin TAGC (open-collector output). The tuner AGC takeover point can be adjusted at pin TADJ. This allows to match the tuner to the SAW filter in order to achieve the optimum IF input level.

Frequency Phase Locked Loop detector (FPLL)

The VIF-amplifier output signal is fed into a frequency detector and into a phase detector via a limiting amplifier. During acquisition the frequency detector produces a DC current proportional to the frequency difference between the input and the VCO signal. After frequency lock-in the phase detector produces a DC current proportional to the

phase difference between the VCO and the input signal. The DC current of either frequency detector or phase detector is converted into a DC voltage via the loop filter, which controls the VCO frequency. In the event of positive modulated signals the phase detector is gated by composite sync in order to avoid signal distortion for overmodulated VIF signals.

VCO, Travelling Wave Divider (TWD) and AFC

The VCO operates with a resonance circuit (with L and C in parallel) at double the PC frequency. The VCO is controlled by two integrated variable capacitors. The control voltage required to tune the VCO from its free-running frequency to actually double the PC frequency is generated by the frequency-phase detector (FPLL) and fed via the loop filter to the first variable capacitor. This control voltage is amplified and additionally converted into a current which represents the AFC output signal. At centre frequency the AFC output current is equal to zero.

For TDA9818: the VCO centre frequency can be decreased (required for L accent standard) by activating an additional internal capacitor. This is achieved by using the L accent switch. In this event the second variable capacitor can be controlled by a variable resistor at the L accent switch for setting the VCO centre frequency to the required L accent value.

The oscillator signal is divided by 2 with a TWD which generates two differential output signals with a 90 degree phase difference independent of the frequency.

Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The vision IF input signal is multiplied with the 'in phase' signal of the travelling wave divider output. In the demodulator stage the video signal polarity can be switched in accordance with the TV standard.

The demodulator output signal is fed via an integrated low-pass filter for attenuation of the carrier harmonics to the video amplifier. The video amplifier is realized by an operational amplifier with internal feedback and high bandwidth. A low-pass filter is integrated to achieve an attenuation of the carrier harmonics for B/G and L standard. The standard dependent level shift in this stage delivers the same sync level for positive and negative modulation. The video output signal at $V_{o(vid)}$ is 1.1 V (p-p) for nominal vision IF modulation, in order to achieve 1 V (p-p) at sound trap output.

Single/multistandard VIF/SIF-PLL and FM-PLL/AM demodulators

TDA9817; TDA9818

SIF amplifier and SIF AGC

The sound IF amplifier consists of two AC-coupled differential amplifier stages. Each differential stage comprises a controlled feedback network provided by emitter degeneration.

The SIF AGC detector is related to the SIF input signal (average level of AM or FM carrier) and controls the SIF amplifier to provide a constant SIF signal to the AM demodulator and single reference QSS mixer. At L standard (AM sound) the SIF AGC reaction time is set to 'slow' for nominal video conditions. But with a decreasing VIF amplitude step the SIF AGC is set to 'fast' mode controlled by the VIF AGC detector. In FM mode this reaction time is always 'fast'.

Single reference QSS mixer

The single reference QSS mixer is realized by a multiplier. The SIF amplifier output signal is fed to the single reference QSS mixer and converted to intercarrier frequency by the regenerated picture carrier (VCO). The mixer output signal is fed via a high-pass for attenuation of the video signal components to the output pin 12. With this system a high performance hi-fi stereo sound processing can be achieved.

For a simplified application without a sound IF SAW filter the single reference QSS mixer can be switched to the intercarrier mode by connecting pin 24 to ground. In this mode the sound IF passes the vision IF SAW filter and the composite IF signal is fed to the single reference QSS mixer. This IF signal is multiplied with the 90 degree TWD output signal for converting the sound IF to intercarrier frequency. This composite intercarrier signal is fed to the output pin 12, too. By using this quadrature detection, the low frequency video signals are removed.

AM demodulator

The AM demodulator is realized by a multiplier. The modulated SIF amplifier output signal is multiplied in phase with the limited (AM is removed) SIF amplifier output signal. The demodulator output signal is fed via an integrated low-pass filter for attenuation of the carrier harmonics to the AF amplifier.

FM-PLL demodulator

The FM-PLL demodulator consists of a limiter and an FM-PLL. The limiter provides the amplification and limitation of the FM sound intercarrier signal. The result is high sensitivity and AM suppression. The amplifier

consists of 7 stages which are internally AC-coupled in order to minimize the DC offset.

Furthermore the AF output signal can be muted by connecting a resistor between the limiter input pin 13 and ground.

The FM-PLL consists of an integrated relaxation oscillator, an integrated loop filter and a phase detector. The oscillator is locked to the FM intercarrier signal, output from the limiter. As a result of locking, the oscillator frequency tracks with the modulation of the input signal and the oscillator control voltage is superimposed by the AF voltage. The FM-PLL operates as an FM demodulator.

AF signal processing

The AF amplifier consists of two parts:

1. The AF pre-amplifier for FM sound is an operational amplifier with internal feedback, high gain and high common mode rejection. The AF voltage from the PLL demodulator, by principle a small output signal, is amplified by approximately 33 dB. The low-pass characteristic of the amplifier reduces the harmonics of the intercarrier signal at the sound output terminal pin 9 at which the de-emphasis network for FM sound is applied. An additional DC control circuit is implemented to keep the DC level constant, independent of process spread.
2. The AF output amplifier (10 dB) provides the required output level by a rail-to-rail output stage. This amplifier makes use of an input selector for switching to AM, FM de-emphasis or mute state, controlled by the standard switching voltage and the mute switching voltage.

Internal voltage stabilizer

The bandgap circuit internally generates a voltage of approximately 1.25 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.6 V which is used as an internal reference voltage.

9.7.7 IC7803: TMP93C071

CMOS 16-Bit Microcontroller TMP93C071F

1. Outline and Feature

TMP93C071F is a high-speed advanced 16-bit microcontroller developed for application with VCR system control, software servo motor control and timer control.

In addition to basics such as I/O ports, the TMP93C071F has high-speed/high-precision signal measuring circuit, PWM (Pulse-Width-Modulator) and high-precision real timing pulse generator.

The device characteristics are as follows:

- (1) Original 16-bit CPU (900L_CPU)
 - TLCS-90 instruction mnemonic upward compatible
 - 16 Mbyte linear address space
 - General-purpose registers and register bank system
 - 16-bit multiplication/division and bit transfer/arithmetic instructions
 - High-speed micro DMA: 4 channels (1.6 μ s / 2 byte at 20 MHz)
- (2) Minimum instruction execution time: 200 ns at 20 MHz
- (3) Internal ROM: ROMless
- (4) Internal RAM: 8 Kbyte
- (5) External memory expansion
 - Can be expanded up to 16 Mbyte (for both programs and data)
 - AM8/16 pin (select the external data bus width)
 - Can be mixed 8 and 16bit external data buses.
 - ...Dynamic data bus sizing.
- (6) 20-bit time-base-counter (TBC)
 - free running counter
 - accuracy: 100 ns (at 20 MHz)
 - overflow: 105 ms (at 20 MHz)
- (7) 8-bit timer (TC0): 1 channel
 - for CTL linear time counter
- (8) 16-bit timer (TC1-5): 5 channels
 - C-sync count, capstan FG count, general: (3 channels)
- (9) Timing pulse generator (TPG): 2 channels
 - (16-bit timing data + 6-bit-output data) with 8-stages FIFO: 1 channel
 - (16-bit timing data + 4-bit-output data): 1 channel
 - accuracy: 400 ns (at 20 MHz)
- (10) Pulse width modulation outputs (PWM)
 - 14-bit PWM: 3 channels (for controlling capstan, drum and tuner)
 - 8-bit PWM: 9 channels (for controlling volume)
 - carrier frequency: 39.1 kHz (at 20 MHz)

980910EBP1

- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.
- TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.
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- (11) 24-bit time base counter capture circuit (Capture 0)
 - (18-bit timing data + 6-bit trigger data) with 8-stages FIFO: 1 channel
 - capture input sources: Remote-control-input (RMTIN), V-sync, CTL, Drum-PG, general (1 channel)
 - accuracy: 400 ns (at 20 MHz)
- (12) 17-bit time base counter capture circuit (Capture 1/2)
 - (16-bit timing data + 1-bit trigger data): 2 channel
 - capture input sources: Drum-FG, Capstan-FG
 - accuracy: 100 ns (at 20 MHz)
- (13) VISS/VASS detection circuit (VISS/VASS)
 - CTL duty detection
 - VASS data 16-bit latch
- (14) Composite-sync-signal (C-sync) input (C-sync In)
 - Vertical-sync-signal (V-sync) separation (V-sepa)
- (15) Head Amp switch/Color Rotary control (HA/CR)
- (16) Pseudo-V/H generator (PV/PH)
- (17) 8-bit A/D converter (ADC): 16 channels
 - Conversion speed: 95states (9.5 μ s at 20 MHz)
- (18) Serial bus I/F
 - 8-bit synchronous (SIO0, 1): 2 channels
 - UART: 1 channel
 - I²CBUS: 1 channel/2 ports
 - • • • Multi - Master function/Master transfer with micro DMA.
- (19) Watch dog timer (WDT)
- (20) Interrupt controller (INTC)
 - CPU: 2 sources • • • SWI instruction, and illegal instruction
 - Internal: 20 sources  7-level priority can be set.
 - External: 5 sources 
- (21) I/O ports
 - 57 I/O ports (multiplexed functional pins)
 - 8 Input ports (P40/AIN3-P47/AIN10: These pins are used as analog input for A/D converter.)
 - 4 Output ports (P24/A20-P27/A23: These pins are also used as address bus outputs.)
- (22) Standby function: 4 halt modes (RUN, IDLE2, IDLE1, STOP)
- (23) System clock function
 - Dual clock operation 20 MHz (High-speed: normal)/32 kHz(Low-speed: slow)
 - • • • 17-bit Real Time Counter built in
- (24) Operating Voltage
 - Vcc = 2.7 to 5.5 V (at 32 kHz)
 - Vcc = 4.5 to 5.5 V (at 20 MHz)
- (25) Package
 - 120 pin QFP 28 mm \times 28 mm (Pin pitch: 0.8 mm)
 - Type name QFP120-P-2828-0.80A

Block Diagram of TMP93C071F

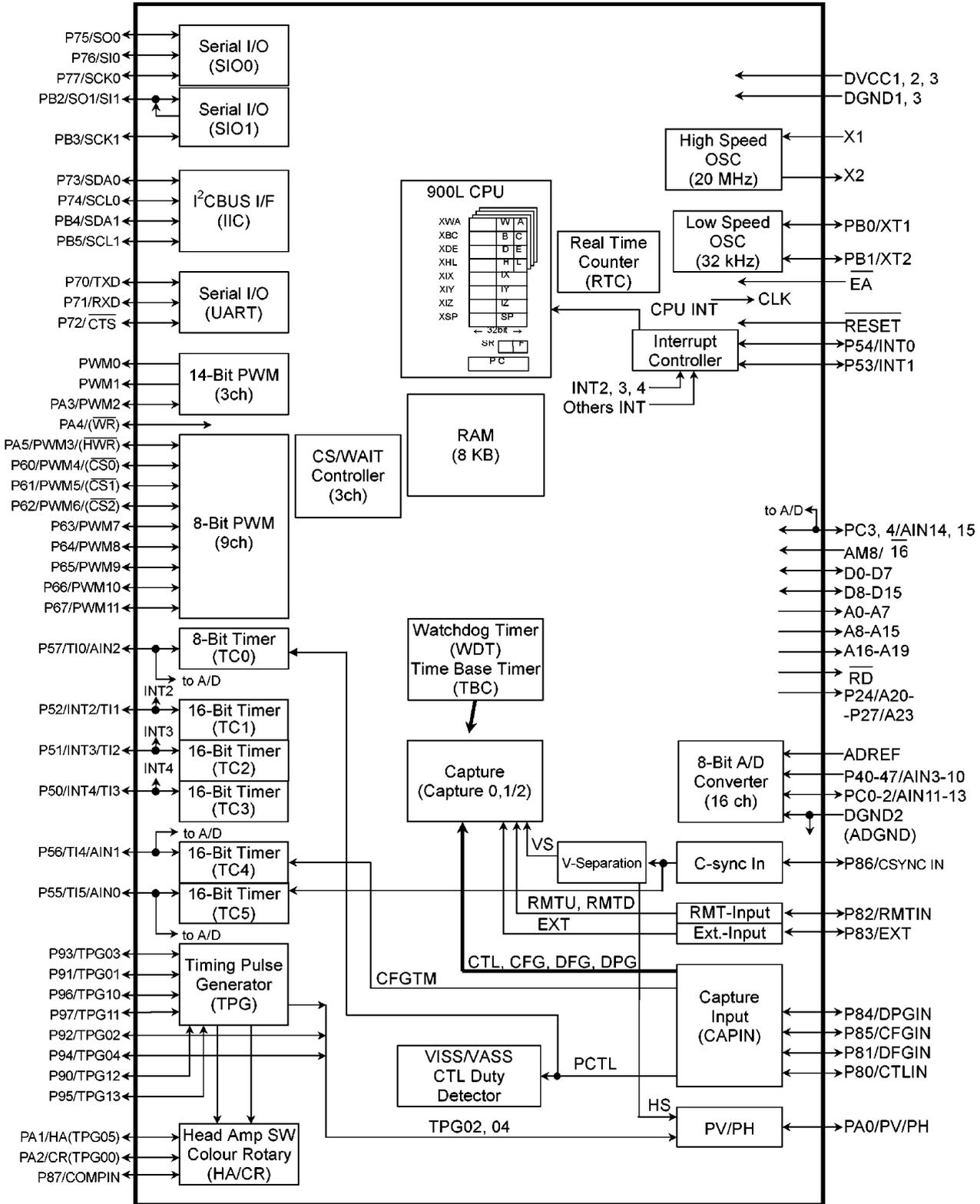


Figure 1 TMP93C071 Block Diagram

2. Pin Assignment And Functions

The assignment of input and output pins for the TMP93C071, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93C071.

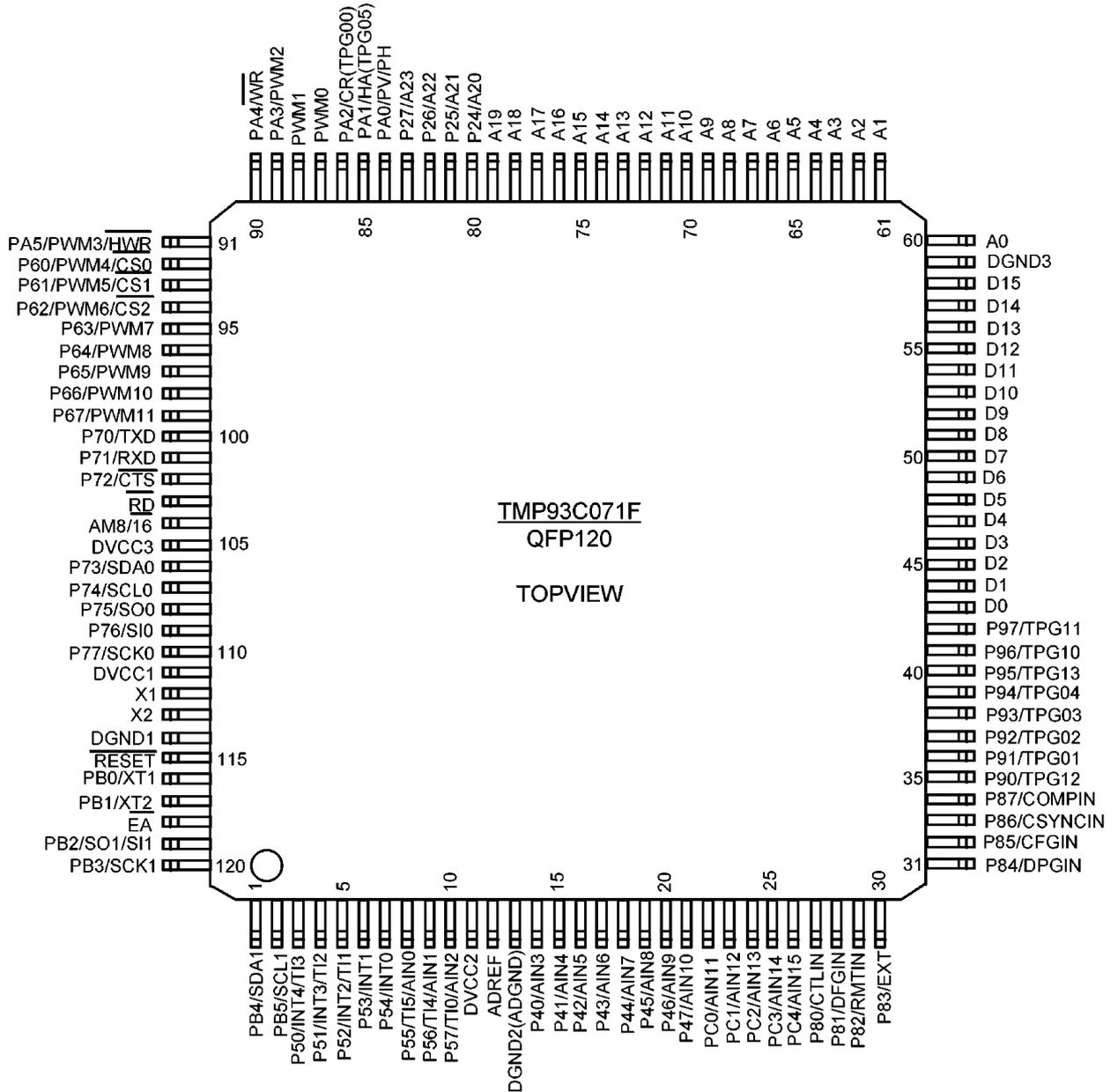


Figure 2.1.1 Pin Assignment (120-pin QFP)

2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

Table 2.2.1 Pin Names and Function (1/5)

Pin name	Number of pins	I/O	Functions
D0 to D15	16	I/O (3-state)	data: 0 to 15 for data bus
A0 to A19	20	Output	Address: 0 to 19 for address bus
A20 to A23/ P24 to P27	4	Output Output	Address: 20 to 23 for address bus Port 2: Output port
\overline{RD}	1	Output	Read: strobe signal for reading external memory
AM8/16	1	Input	data bus width select input (only 8 bit or 8 bit/16 bit)
PC3, 4/ $\overline{16}$ AIN14, 15	2	I/O Input	Port C3, 4: I/O port that allows selection of I/O on a bit basis. Analog Input: Analog input signal for A/D converter
\overline{EA}	1	Input	External access: Always set to $_0$
\overline{RESET}	1	Input	Reset: Initializes LSI.(with pull-up R)
X1/X2	2	I/O	High Frequency Oscillator connecting pins (20 MHz)
PB0/ XT1	1	I/O Input	Port B0: I/O port (Open Drain Output) Low Frequency Oscillator connecting pin (32 kHz)
PB1/ XT2	1	I/O Output	Port B1: I/O port (Open drain Output) Low Frequency Oscillator connecting pin
ADREF	1	Input	A/D reference Voltage input
P40 to P47/ AIN3 to AIN10	8	Input Input	Port 4: Input ports Analog input: Analog input signal for A/D converter
PC0 to PC2/ AIN11 to AIN13	3	I/O Input	Port C: PC0 to PC2 I/O port that allows selection of I/O on a bit basis. Analog input: Analog input signal for A/D converter
P57/ TI0/ AIN2	1	I/O Input (schmitt) Input	Port 57: I/O port 8-bit timer0 (TC0) Input 0 Analog input: Analog input signal for A/D converter
P56/ TI4/ AIN1	1	I/O Input (schmitt) Input	Port 56: I/O port 16-bit timer4 (TC4) Input 4 Analog input: Analog input signal for A/D converter
P55/ TI5/ AIN0	1	I/O Input (schmitt) Input	Port 55: I/O port 16-bit timer5 (TC5) Input 5 Analog input: Analog input signal for A/D converter
P54/ INT0	1	I/O Input (schmitt)	Port 54: I/O port External Interrupt request input 0: Rising edge/ Level selectable 
P53/ INT1	1	I/O Input (schmitt)	Port 53: I/O port External Interrupt request input 1: Rising edge/ Level selectable 
P52/ INT2/ TI1	1	I/O Input (schmitt) Input	Port 52: I/O port External Interrupt request input 2 Rising edge/Falling edge selectable  16-bit timer1(TC1) Input 1

Table 2.2.1 Pin Names and Function (2/5)

Pin name	Number of pins	I/O	Functions
P51/ INT3/ TI2	1	I/O Input Input (schmitt)	Port 51: I/O port External Interrupt request input 3 Rising edge/Falling edge selectable  16-bit timer2 (TC2) Input 2
P50/ INT4/ TI3	1	I/O Input Input (schmitt)	Port 50: I/O port External Interrupt request input 4 Rising edge/Falling edge selectable  16-bit timer3 (TC3) Input 3
PWM0	1	Output 3-state Open Drain	PWM (14 bit) output 0: PWM0 output push/pull or open drain output selectable
PWM1	1	Output 3-state Open Drain	PWM (14 bit) output 1: PWM1 output push/pull or open drain output selectable
PA3/ PWM2	1	I/O 3-state Open Drain	Port A3: I/O port PWM (14 bit) output 2: PWM2 output push/pull or open drain output selectable
PA4/ \overline{WR}	1	I/O 3-state Open Drain Output	Port A4: I/O port push/pull or open drain output selectable Write: Strobe signal for writing data on pins D0 to D7
PA5/ PWM3/ \overline{HWR}	1	I/O Output 3-state Open Drain Output	Port A5: I/O port 8-bit PWM output 3: PWM3 output push/pull or open drain output selectable High write: Strobe signal for writing data on pins D8 to D15
P60/ PWM4/ $\overline{CS0}$	1	I/O Output 3-state Open Drain Output	Port 60: I/O port 8-bit PWM output 4: PWM4 output push/pull or open drain output selectable Chip select0: Output _0_ when address is within specified address area.
P61/ PWM5/ $\overline{CS1}$	1	I/O Output 3-state Open Drain Output	Port 61: I/O port 8-bit PWM output 5: PWM5 output push/pull or open drain output selectable Chip select1: Output _0_ when address is within specified address area.
P62/ PWM6/ $\overline{CS2}$	1	I/O Output 3-state Open Drain Output	Port 62: I/O port 8-bit PWM output 6: PWM6 output push/pull or open drain output selectable Chip select2: Output _0_ when address is within specified address area.

Table 2.2.1 Pin Names and Function (3/5)

Pin name	Number of pins	I/O	Functions
P63/ PWM7	1	I/O Output 3-state Open Drain	Port 63: I/O port 8-bit PWM output7: PWM7 output push/pull or open drain output selectable
P64/ PWM8	1	I/O Output 3-state Open Drain	Port 64: I/O port 8-bit PWM output8: PWM8 output push/pull or open drain output selectable
P65/ PWM9	1	I/O Output 3-state Open Drain	Port 65: I/O port 8-bit PWM output9: PWM9 output push/pull or open drain output selectable
P66/ PWM10	1	I/O Output 3-state Open Drain	Port 66: I/O port 8-bit PWM output 10: PWM10 output push/pull or open drain output selectable
P67/ PWM11	1	I/O Output 3-state Open Drain	Port 67: I/O port 8-bit PWM output 11: PWM11 output push/pull or open drain output selectable
P73/ SDA0	1	I/O I/O (schmitt) Open Drain	Port 73: I/O port I ² CBUS SDA line 0 push/pull or open drain output selectable
P74/ SCL0	1	I/O I/O (schmitt) Open Drain	Port 74: I/O port I ² CBUS SCL line 0 push/pull or open drain output selectable
P75/ SIO0	1	I/O Output (schmitt) Open Drain	Port 75: I/O port SIO0 send data 0 push/pull or open drain output selectable
P76/ SIO	1	I/O Input (schmitt)	Port 76: I/O port SIO0 receive data 0
P77/ SCK0	1	I/O I/O (schmitt) Open Drain	Port 77: I/O port SIO0 transfer clock input/output 0 push/pull or open drain output selectable
P70/ TXD	1	I/O Output (schmitt) Open Drain	Port 70: I/O port UART send data push/pull or open drain output selectable
P71/ RXD	1	I/O Input (schmitt)	Port 71: I/O port UART receive data
P72/ CTS	1	I/O Input (schmitt)	Port 72: I/O port UART clear to send
P80/ CTLIN	1	I/O Input (schmitt)	Port 80: I/O port Capture input for Control signal (CTL)

Table 2.2.1 Pin Names and Function (4/5)

Pin Name	Number of pins	I/O	Functions
P81/ DFGIN	1	I/O Input (schmitt)	Port 81: I/O port Capture input for Drum-FG signal (DFG)
P82/ RMTIN	1	I/O Input (schmitt)	Port 82: I/O port Capture input for Remote Control Input signal
P83/ EXT	1	I/O Input (schmitt)	Port 83: I/O port External Capture input (Rising edge only)
P84/ DPGIN	1	I/O Input (schmitt)	Port 84: I/O port Capture input for Drum-PG signal (DPG)
P85/ CFGIN	1	I/O Input (schmitt)	Port 85: I/O port Capture input for Capstan-FG signal (CFG)
P86/ CSYNC IN	1	I/O Input (schmitt)	Port 86: I/O port Capture input for C-sync
P87/ COMPIN	1	I/O Input (schmitt)	Port 87: I/O port Envelope Comparator Input (to HA/CR)
P90/ TPG12	1	I/O Output Open Drain	Port 90: I/O port TPG12: TPG output 12 push/pull or open drain output selectable
P91/ TPG01	1	I/O Output Open Drain	Port 91: I/O port TPG01: TPG output 01 push/pull or open drain output selectable
P92/ TPG02	1	I/O Output Open Drain	Port 92: I/O port TPG02: TPG output 02 (Internally connected to PV/PH Logic) push/pull or open drain output selectable
P93/ TPG03	1	I/O Output Open Drain	Port 93: I/O port TPG03: TPG output 03 push/pull or open drain output selectable
P94/ TPG04	1	I/O Output Open Drain	Port 93: I/O port TPG04: TPG output 04 (Internally connected to PV/PH Logic) push/pull or open drain output selectable
P95/ TPG13	1	I/O Output Open Drain	Port 95: I/O port TPG13: TPG output 13 push/pull or open drain output selectable
P96/ TPG10	1	I/O Output Open Drain	Port 96: I/O port TPG10: TPG output 10 push/pull or open drain output selectable
P97/ TPG11	1	I/O Output Open Drain	Port 97: I/O port TPG11: TPG output 11 push/pull or open drain output selectable
PA0/ PV-PH	1	I/O Output 3-state	Port PA0: I/O Port Pseudo-Vsync/Pseudo-Hsync (PV/PH) output (controlled by TPG02/04.)
PA1/ HA (TPG05)	1	I/O Output	Port PA1: I/O Port HA: Head amp switch output (are also used as TPG05 output.)
PA2/ CR (TPG00)	1	I/O Output	Port PA2: I/O Port CR: Colour Rotary output (are also used as TPG00 output.)

Table 2.2.1 Pin Names and Function (5/5)

Pin name	Number of pins	I/O	Functions
PB2/ SO1/SI1	1	I/O I/O (schmitt) Open Drain	Port PB2: I/O Port SIO1 send data 1 and receive data 1 (Internally connected) push/pull or open drain output selectable
PB3/ SCK1	1	I/O I/O (schmitt) Open Drain	Port PB3: I/O Port SIO1 transfer clock input/output 1 push/pull or open drain output selectable
PB4/ SDA1	1	I/O I/O (schmitt) Open Drain	Port PB4: I/O Port I ² CBUS SDA line 1 push/pull or open drain output selectable
PB5/ SCL1	1	I/O I/O (schmitt) Open Drain	Port PB5: I/O Port I ² CBUS SCL line 1 push/pull or open drain output selectable
DVCC1, 2, 3	3		Power supply pins All of these pins should be connected to power source.
DGND1, DGND2 (ADGND), DGND3	3		GND pins (0 V) All of these pins should be connected to GND (0 V) line. DGND2 are also used as ADGND for A/D converter.

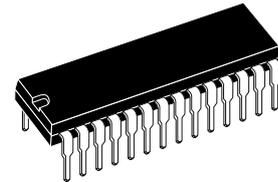
9.7.8 IC7990: STV5348

STV5348

- COMPLETE TELETEXT AND VPS DECODER INCLUDING AN 8 PAGE MEMORY ON A SINGLE CHIP
- UPWARD SOFTWARE COMPATIBLE WITH PREVIOUS SGS-THOMSON'S MULTICHIP SOLUTIONS (SAA5231, SDA5243, STV5345)
- PERFORM PDC SYSTEM A (VPS) AND PDC SYSTEM B (8/30/2) DATA STORAGE SEPARATELY
- DEDICATED "ERROR FREE" OUTPUT FOR VALID PDC DATA
- INDICATION OF LINE 23 FOR EXTERNAL USE
- SINGLE +5V SUPPLY VOLTAGE
- SINGLE 13.875MHz CRYSTAL
- REDUCED SET OF EXTERNAL COMPONENTS, NO EXTERNAL ADJUSTMENT
- OPTIMIZED NUMBER OF DIGITAL SIGNALS REDUCING EMC RADIATION
- HIGH DENSITY CMOS TECHNOLOGY
- DIGITAL DATA SLICER AND DISPLAY CLOCK PHASE LOCK LOOP
- 28 PIN DIP & SO PACKAGE

DESCRIPTION

The STV5348 decoder is a computer-controlled teletext device including an 8 page internal memory. Data slicing and capturing extracts the teletext information embedded in the composite video signal. Control is accomplished via a two wire serial I²C bus ®. Chip address is 22h. Internal ROM provides a character set suitable to display text using up to seven national languages. Hardware and software features allow selectable master/slave synchronization configurations. The STV5348 also supports facilities for reception and display of current level protocol data.



DIP28

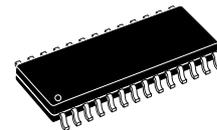
(Plastic Package)

ORDER CODE :

STV5348 West European

STV5348/H East European

STV5348/T Turkish & European



SO28

(Plastic Package)

ORDER CODE :

STV5348D West European

STV5348D/H East European

STV5348D/T Turkish & European

PIN CONNECTIONS

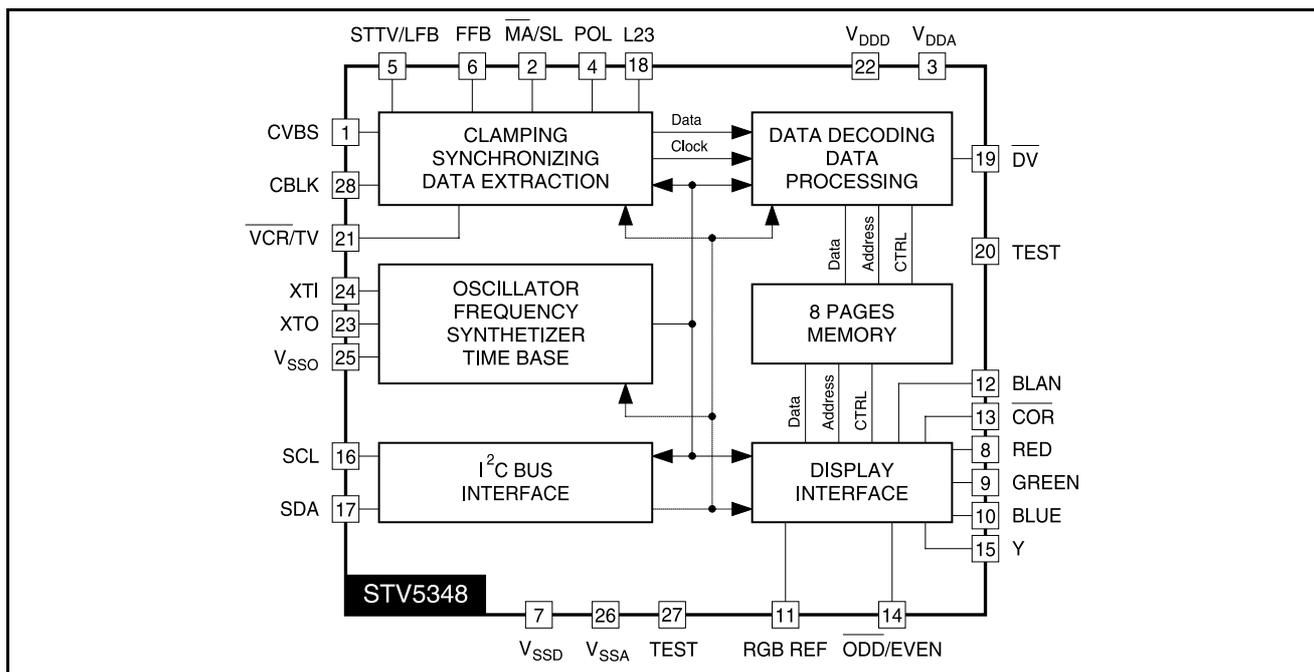
CVBS	1	28	CBLK
MA/SL	2	27	TEST
V _{DDA}	3	26	V _{SSA}
POL	4	25	V _{SSO}
STTV/LFB	5	24	XTI
FFB	6	23	XTO
V _{SSD}	7	22	V _{DDD}
R	8	21	VCR/TV
G	9	20	RESERVED
B	10	19	DV
RGB REF	11	18	L23
BLAN	12	17	SDA
COR	13	16	SCL
ODD/EVEN	14	15	Y

PIN DESCRIPTION

Pin N°	Symbol	Function	Description	Figure
1	CVBS	Input	Composite Video Signal Input through Coupling Capacitor	9
2	MA/SL	Input	Master/Slave Selection Mode	11
3	V _{DDA}	Analog Supply	+5V	-
4	POL	Input	STTV / LFB / FFB Polarity Selection	12
5	STTV/LFB	Output / Input	Composite Sync Output, Line Flyback Input	15
6	FFB	Input	Field Flyback Input	12
7	V _{SSD}	Ground	Digital Ground	-
8	R	Output	Video Red Signal	13
9	G	Output	Video Green Signal	13
10	B	Output	Video Blue Signal	13
11	RGBREF	Supply	DC Voltage to define RGB High Level	13
12	BLAN	Output	Fast Blanking Output TTL Level	15
13	COR	Output	Open Drain Contrast Reduction Output	15
14	ODD/EVEN	Output	25Hz Output Field synchronized for non-interlaced display	15
15	Y	Output	Open Drain Foreground Information Output	15
16	SCL	Input	Serial Clock Input	16
17	SDA	Input/ Output	Serial Data Input/Output	17
18	L23	Output	Line 23 Identification	15
19	DV	Output	VPS Data Valid	15
20	RESERVED	Test	To be connected to V _{SSD} through a resistor	15
21	VCR/TV	Input	PLL Time Constant Selection	15
22	V _{DDD}	Digital Supply	+5V	-
23	XTO	Crystal Output	Oscillator Output 13.875MHz	14
24	XTI	Crystal Input	Oscillator Input 13.875MHz	14
25	V _{SSO}	Ground	Oscillator Ground	-
26	V _{SSA}	Ground	Analog Ground	-
27	TEST	Test	Grounded to V _{SSA}	11
28	CBLK	Input / Output	To connect Black Level Storage Capacitor	28

5348-01.TBL

BLOCK DIAGRAM



9.7.9 Tuner1705: UV1316K

VHF/UHF television tuner**UV1336K MK3****FEATURES**

- Member of UV1300 MK3 family of small-sized UHF/VHF tuners
- Integrated with passive splitter
- Covers systems M, N
- Digitally-controlled (PLL) tuning via I²C-bus
- Fast 400kHz I²C bus protocol compatible with 3.3V and 5V micro controllers
- 181 channels coverage (Off-air and full cable)
- World standardized mechanical dimensions and pinning. Horizontal mounting is optionally available.

**DESCRIPTION**

The UV1336K MK3 splitter - tuner belongs to the UV1300 family of WSP tuners, which are designed to meet a wide range of TV applications. It is a full band tuner suitable for NTSC M, N and PAL M, N. The low IF output impedance is designed for direct drive of a wide variety of SAW filters with sufficient suppression of triple transient.

The UV1336K MK3 incorporates internal wideband-AGC with selectable TOP adjustment via I²C.

This tuner complies with the requirements of radiation, conforming with:

FCC Part 15, Subpart B

BETS 7

CISPR13

MARKING

The following items of information are printed on a sticker that is on the top cover of the tuner:

Type number

Code number

Origin letter of factory

Change code

Year and week code

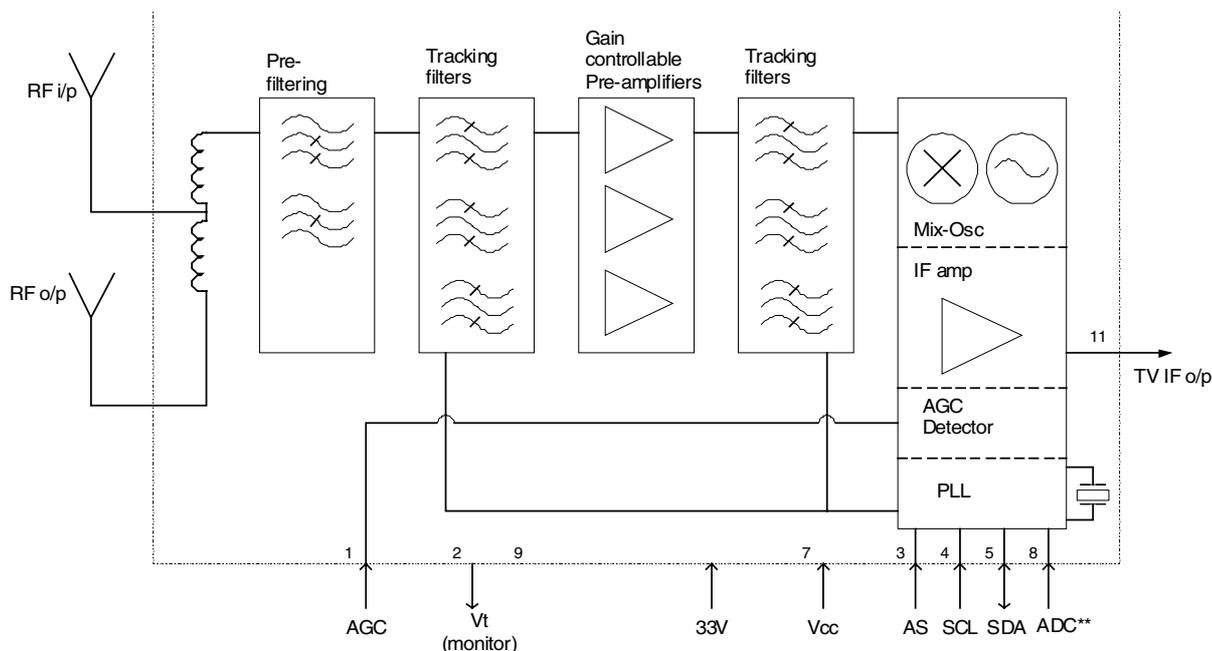
ORDERING INFORMATION

TYPE	DESCRIPTION	ORDER NUMBERS
UV1336K/A F G S-3	F connector, wideband AGC, switchable FM trap	3139 147 17011

VHF/UHF television tuner

UV1336K MK3

BLOCK DIAGRAM



** ADC option not available in NTSC versions

PINNING

SYMBOL	PIN	DESCRIPTION
AGC	1	Gain Control Voltage
TU	2	Tuning voltage
AS	3	I ² C-Bus Address Select
SCL	4	I ² C-Bus Serial Clock
SDA	5	I ² C-Bus Serial Data
n.c.	6	Not Connected
V _s	7	PLL Supply Voltage +5V
n.c.	8	Not Connected
V _{ST}	9	Fixed tuning Supply Voltage +33V
n.c.	10	Not connected
IF1	11	Asymmetrical IF Output
GND	M1,M2,M3,M4	Mounting Tags (Ground)

9.8 IC's Digital Board

9.8.1 IC7100: VSM

VERSATILE STREAM MANAGER

GENERAL DESCRIPTION

The Versatile Stream Manager (VSM) is an ASIC used in the first generation DVD Video Recorder. Main function of the VSM is to interface directly to the different hardware modules such as Basic Engine, MPEG encoders, MPEG decoders and buffering the data streams that are coming from or going to these hardware modules.

The VSM contains a memory interface to support one 4M*16 SDRAM device. A host interface allows a CPU to directly access this memory and the VSM's internal registers.

Handling of data streams is done using scatter / gather DMA's under software control. Hardware support is provided in the VSM to support software MPEG AV multiplexing.

FEATURES

The VSM features include:

- SDRAM memory interface to support one 4 banks*1M*16 (64Mbit) SDRAM device.

- Glueless Host Interface for STM's STi5505.

- Glueless MPEG Decoder interface for STM's STi5505

- Glueless interface to Philips' SAA6750 MPEG Video Encoder or SAA6752 MPEG AV Encoder.

- Glueless interface to Motorola's DSP56362 used as MPEG Audio Encoder.

- Glueless interface to Philips' HDR65 as part of Basic Engine interface including the Sector Processor as also included in the STi5505.

- Audio Clock Control providing PLL loop and clock lock detection.

- Double Extraction of VBI decoded data from extended CCIR 656 stream.

- Double UART with hardware handshake and 8 byte Rx/Tx FIFO.

- Generation of additional Host Bus to support Audio Encoder DSP56362.

- Descriptor based DMA Controllers for data stream handling.

- Hardware support for software MPEG multiplex process.

- Internal Interrupt Controller to handle internal and 4 external interrupt sources.

- Operates from single 27 MHz clock input.

- JTAG for production tests.

- 3.3V logic core.

- 3.3V / 5V toleration IO pins.

- 208 PIN LQFP Package. (CR1087)

BLOCK DIAGRAM

Figure 2.1 shows the block diagram of the VSM. The hardware blocks can be divided in to three categories:

- General modules: Host Interface, Memory Interface, Interrupt Controller.

- DMA Controllers.

- Functional Interfaces; the link between the actual external hardware interface and the DMA Controller. Some Functional Interfaces have knowledge about the stream coming through in order to perform for example MPEG stream characteristics extraction and insertion.

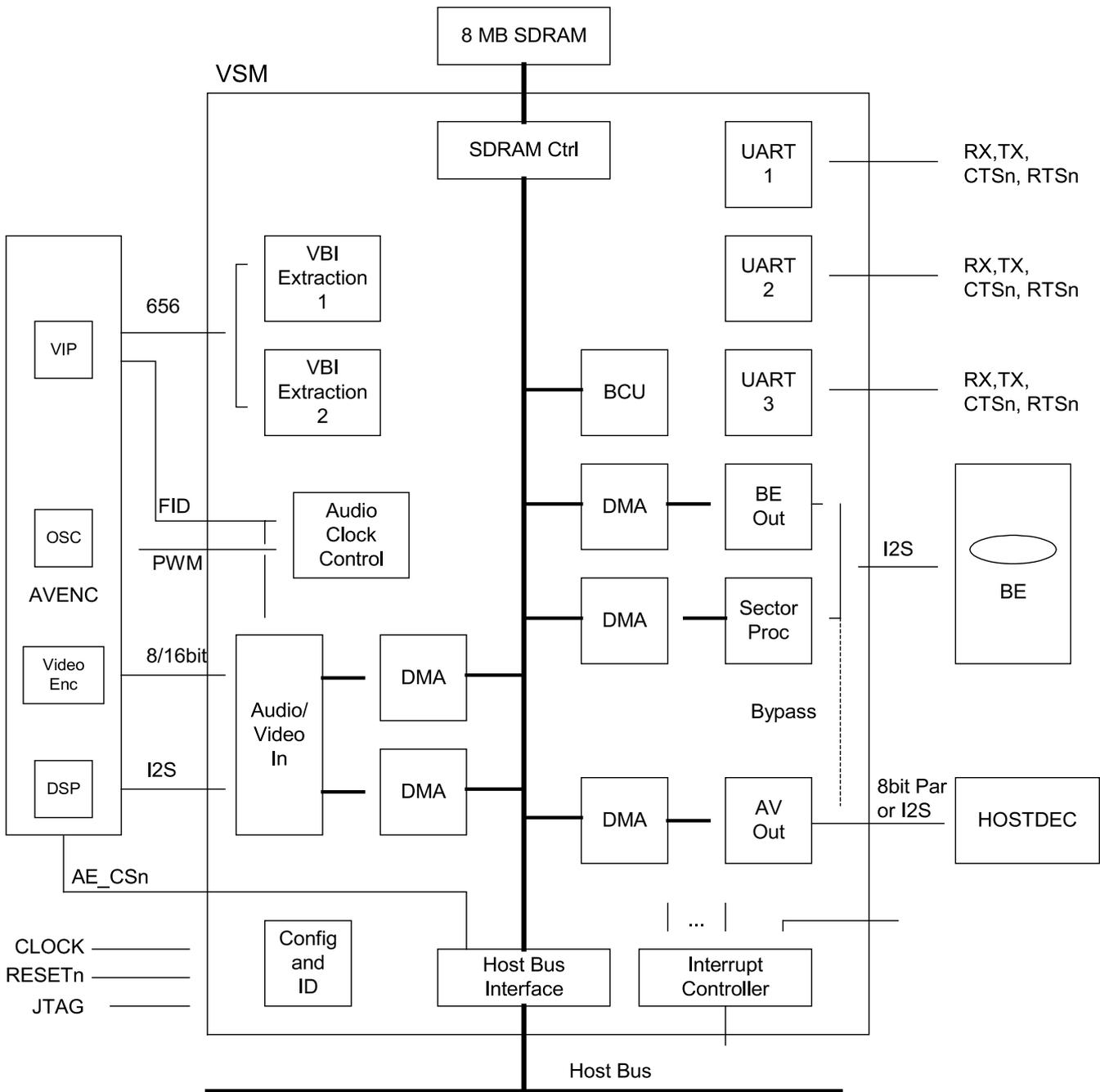


Figure 2.1: VSM Overview

PINNING

OVERVIEW

Name	Pins	Type	Function
System			
RESETn	1	In	
SYSCLK (27MHz)	1	In	
Host Interface			
HO_A(21:1)	21	In	
HO_D(15:0)	16	In/Out	
HO_BEn(1:0)	2	In	
HO_RWn	1	In	
HO_CSLn	1	In	
HO_CSHn	1	In	
HO_A22	1	In	
HO_WAIT	1	Out	
HO_PROCCLK	1	In	
Memory Interface			
M_A(13:0)	14	Out	
M_DQ(15:0)	16	In/Out	
M_RASn	1	Out	
M_CASn	1	Out	
M_WEn	1	Out	
M_LDQM	1	Out	
M_UDQM	1	Out	
M_CLKOUT	1	Out	
M_CLKEN	1	Out	
Basic Engine Interface			
BE_BCLK	1	In	
BE_DATI	1	In	
BE_WCLK	1	In	
BE_SYNC	1	In/Out	
BE_FLAG	1	In	
BE_V4	1	In	
BE_DATO	1	Out	
Video Encoder Interface			
VE_D(15:0)	16	In	
VE_DS _n	1	Out	
VE_DTACK _n	1	In	
VE_VIP_ERROR	1	In	Signal coming from SAA7114
Audio Encoder Interface			
AE_CS _n	1	Out	
AE_BCLK	1	In/Out	(CR151,CR157)
AE_WCLK	1	In/Out	(CR151,CR157)
AE_DATA	1	In	(CR157)

Decoder Interface			
D_PAR_D(7:0)	8	Out	
D_PAR_DVALID	1	Out	
D_PAR_STR	1	Out	
D_PAR_REQ	1	In	
D_PAR_SYNC	1	Out	
D_WCLK	1	Out	
D_V4	1	Out	
Audio Clock Control			
ACC_FID	1	In	(CR200)
ACC_PWM	1	Out	
ACC_ACLK_OSC	1	In	
ACC_ACLK_DAI	1	In	
ACC_ACLK_PLL	1	In	
ACC_ACLK_DEC	1	Out	
VBI Extractor			
VBI_IPD(7:0)	8	In	
VBI_ICLK	1	In	
UART 1			
UART1_RX	1	In	
UART1_TX	1	Out (OC)	
UART1_CTSn	1	In	
UART1_RTSn	1	Out (OC)	
UART 2			
UART2_RX	1	In	
UART2_TX	1	Out (OC)	
UART2_CTSn	1	In	
UART2_RTSn	1	Out (OC)	
UART 3 (VSM1B)			
UART3_RX	1	In	
UART3_TX	1	Out	
UART3_CTSn	1	In	
UART3_RTSn	1	Out	
Interrupt Controller			
EXTINT(3:0)	4	In	From: VEnc, AEnc, BE, VSync (STi5505)
CPUINT(1:0)	2	Out (OC)	
JTAG			
TCK	1	In	Boundary Scan
TDI	1	In	
TDO	1	Out/Z	
TMS	1	In	
TRSTn	1	In	
Test			
TEST0	1	In	Amsal Test
TEST1	1	In	
Power Supply			
VDD	20	Power	10% of total pins package
VSS	20	Power	10% of total pins package
Total Pins	208		

9.8.2 IC7101; IC7306: IC 7402 SDRAM

SYNCHRONOUS DRAM

MT48LC16M4A2 – 4 Meg x 4 x 4 banks
 MT48LC8M8A2 – 2 Meg x 8 x 4 banks
 MT48LC4M16A2 – 1 Meg x 16 x 4 banks

For the latest data sheet, please refer to the Micron web site: www.micronsemi.com/datasheets/sdramds.html

FEATURES

- PC66-, PC100- and PC133-compliant
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge, includes CONCURRENT AUTO PRECHARGE, and Auto Refresh Modes
- Self Refresh Modes: standard and low power
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply

OPTIONS

- Configurations

16 Meg x 4 (4 Meg x 4 x 4 banks)	16M4
8 Meg x 8 (2 Meg x 8 x 4 banks)	8M8
4 Meg x 16 (1 Meg x 16 x 4 banks)	4M16

- WRITE Recovery ('WR)
'WR' = "2 CLK"¹ A2

Plastic Package – OCPL²
 54-pin TSOP II (400 mil) TG

Timing (Cycle Time)
 10ns @ CL = 2 (PC100) -8E⁴
 7.5ns @ CL = 3 (PC133) -75
 7.5ns @ CL = 2 (PC133) -7E

- Self Refresh
 Standard None
 Low Power I.

- Operating Temperature Range
 Commercial (0°C to +70°C) None
 Extended (-40°C to +85°C) IT³

NOTE:1. Refer to Micron Technical Note TN-48-05.
 2. Off-center parting line.
 3. Consult Micron for availability.
 4. Not recommended for new designs.

Part Number Example:
MT48LC8M8A2TG-75

MARKING

PIN ASSIGNMENT (Top View)

54-Pin TSOP

x4	x8	x16			x16	x8	x4
-	-	V _{DD}	2	54	V _{SS}	-	-
NC	DQ0	DQ0	3	53	DQ15	DQ7	NC
-	-	V _{DDQ}	4	52	V _{SSQ}	-	-
NC	NC	DQ1	5	51	DQ14	NC	NC
DQ0	DQ1	DQ2	6	50	DQ13	DQ6	DQ3
-	-	V _{SSQ}	7	49	V _{DDQ}	-	-
NC	NC	DQ3	8	48	DQ12	NC	NC
NC	DQ2	DQ4	9	47	DQ11	DQ5	NC
-	-	V _{DDQ}	10	46	V _{SSQ}	-	-
NC	NC	DQ5	11	45	DQ10	NC	NC
DQ1	DQ3	DQ6	12	44	DQ9	DQ4	DQ2
-	-	V _{SSQ}	13	43	V _{DDQ}	-	-
NC	NC	DQ7	14	42	DQ8	NC	NC
-	-	V _{DD}	15	41	V _{SS}	-	-
NC	NC	DQML	16	40	NC	-	-
-	-	WE#	17	39	DQMH	DQM	DQM
-	-	CAS#	18	38	CLK	-	-
-	-	RAS#	19	37	CKE	-	-
-	-	CS#	20	36	NC	-	-
-	-	BA0	21	35	A11	-	-
-	-	BA1	22	34	A9	-	-
-	-	A10	23	33	A8	-	-
-	-	A0	24	32	A7	-	-
-	-	A1	25	31	A6	-	-
-	-	A2	26	30	A5	-	-
-	-	A3	27	29	A4	-	-
-	-	V _{DD}		28	V _{SS}	-	-

Note: The # symbol indicates signal is active LOW. A dash (-) indicates x8 and x4 pin function is same as x16 pin function.

	16 Meg x 4	8 Meg x 8	4 Meg x 16
Configuration	4 Meg x 4 x 4 banks	2 Meg x 8 x 4 banks	1 Meg x 16 x 4 banks
Refresh Count	4K	4K	4K
Row Addressing	4K (A0-A11)	4K (A0-A11)	4K (A0-A11) *
Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column Addressing	1K (A0-A9)	512 (A0-A8)	256 (A0-A7)

KEY TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME		SETUP TIME	HOLD TIME
		CL = 2*	CL = 3*		
-7E	143 MHz	-	5.4ns	1.5ns	0.8ns
-75	133 MHz	-	5.4ns	1.5ns	0.8ns
-7E	133 MHz	5.4ns	-	1.5ns	0.8ns
-8E ^{3,4}	125 MHz	-	6ns	2ns	1ns
-75	100 MHz	6ns	-	1.5ns	0.8ns
-8E ^{3,4}	100 MHz	6ns	-	2ns	1ns

* CL = CAS (READ) latency

64Mb SDRAM PART NUMBERS

PART NUMBER	ARCHITECTURE
MT48LC16M4A2TG	16 Meg x 4
MT48LC8M8A2TG	8 Meg x 8
MT48LC4M16A2TG	4 Meg x 16

GENERAL DESCRIPTION

The 64Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 67,108,864 bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x4's 16,777,216-bit banks is organized as 4,096 rows by 1,024 columns by 4 bits. Each of the x8's 16,777,216-bit banks is organized as 4,096 rows by 512 columns by 8 bits. Each of the x16's 16,777,216-bit banks is organized as 4,096 rows by 256 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11 select the row). The address bits registered coincident with the READ or WRITE

command are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 64Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the $2n$ rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

The 64Mb SDRAM is designed to operate in 3.3V memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access.

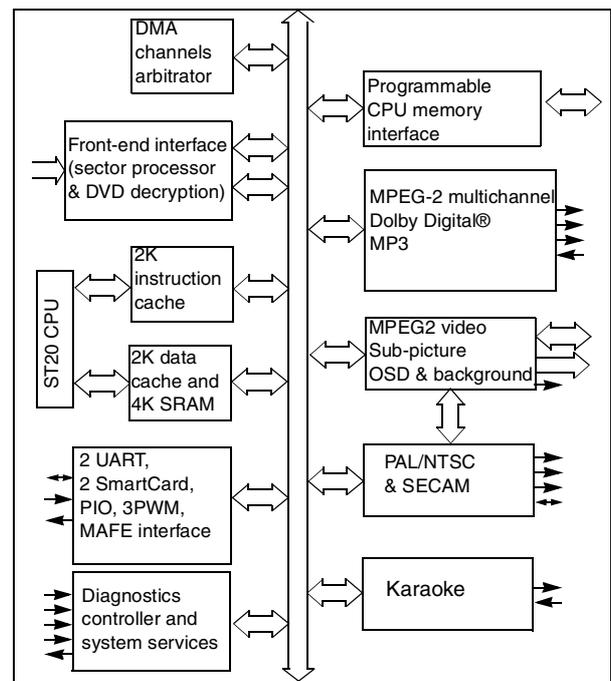
STi5508

DVD HOST PROCESSOR WITH ENHANCED AUDIO FEATURES

- **Integrated 32-bit host CPU @ 60MHz**
 - 2 Kbytes of lcache, 2 Kbytes of Dcache, and 4Kbytes of SRAM configurable as Dcache.
- **Audio decoder**
 - 5.1 channel Dolby Digital® /MPEG-2 multi-channel decoding, 3 X 2-channel PCM outputs
 - IEC60958 -IEC61937 digital output
 - SRS®/TruSurround®
 - DTS digital out and MP3 decoding
- **Karaoke processor**
 - Echo, pitch shift, microphone inputs, voice cancellation and multiple other effects
- **Video decoder**
 - Supports MPEG-2 MP@ML
 - Fully programmable zoom-in and zoom-out
 - PAL to NTSC and NTSC to PAL conversion
- **DVD and SVCD subpicture decoder**
- **High performance on-screen display**
 - 2 to 8 bits per pixel OSD options
 - Anti-flicker, anti-flutter and anti-aliasing filters
- **PAL/NTSC/SECAM encoder**
 - RGB, CVBS, Y/C and YUV outputs with 10-bit DACs
 - Macrovision® 7.01/6.1 compatible
- **Shared SDRAM memory interface**
 - Supports 1 or 2x16Mbit, or 1x64Mbit 125MHz SDRAM
- **Programmable CPU memory interface for SDRAM, ROM, peripherals...**
- **Front-end interface**
 - DVD, VCD, SVCD and CD-DA compatible
 - Serial, parallel and ATAPI interfaces
 - Hardware sector filtering
 - Integrated CSS decryption and track buffer
- **Integrated peripherals**
 - 2 UARTS, 2 SmartCards, I2C controller, 3 PWM outputs, 3 capture timers
 - Modem support
 - 38 bits of programmable I/O
- **Professional toolset support**
 - ANSI C compiler and libraries
- **208 pin PQFP package**

The STi5508 provides a highly integrated back-end solution for DVD applications. A host CPU handles both the general application (the user interface, and the DVD, CD-DA, VCD, SVCD navigation) and the drivers of the different embedded peripheral (audio/video, karaoke, sub-picture decoders, OSD, PAL/NTSC encoder...).

Because of its memory savings, increased number of internal peripherals, improved development platform and reference design, the STi5508 offers a cost-effective solution to DVD applications, with rapid time-to-market.



1 Architecture overview

1.1 Introduction

The figure below shows the architecture of the STi5508. This device has the same global architecture as the STi5505, with the addition of new features such as karaoke, a shared SDRAM memory interface and extra display planes. Because of this increased performance, the STi5508 and STi5505 are not pin compatible. This chapter gives a brief overview of each of the functional blocks of the STi5508.

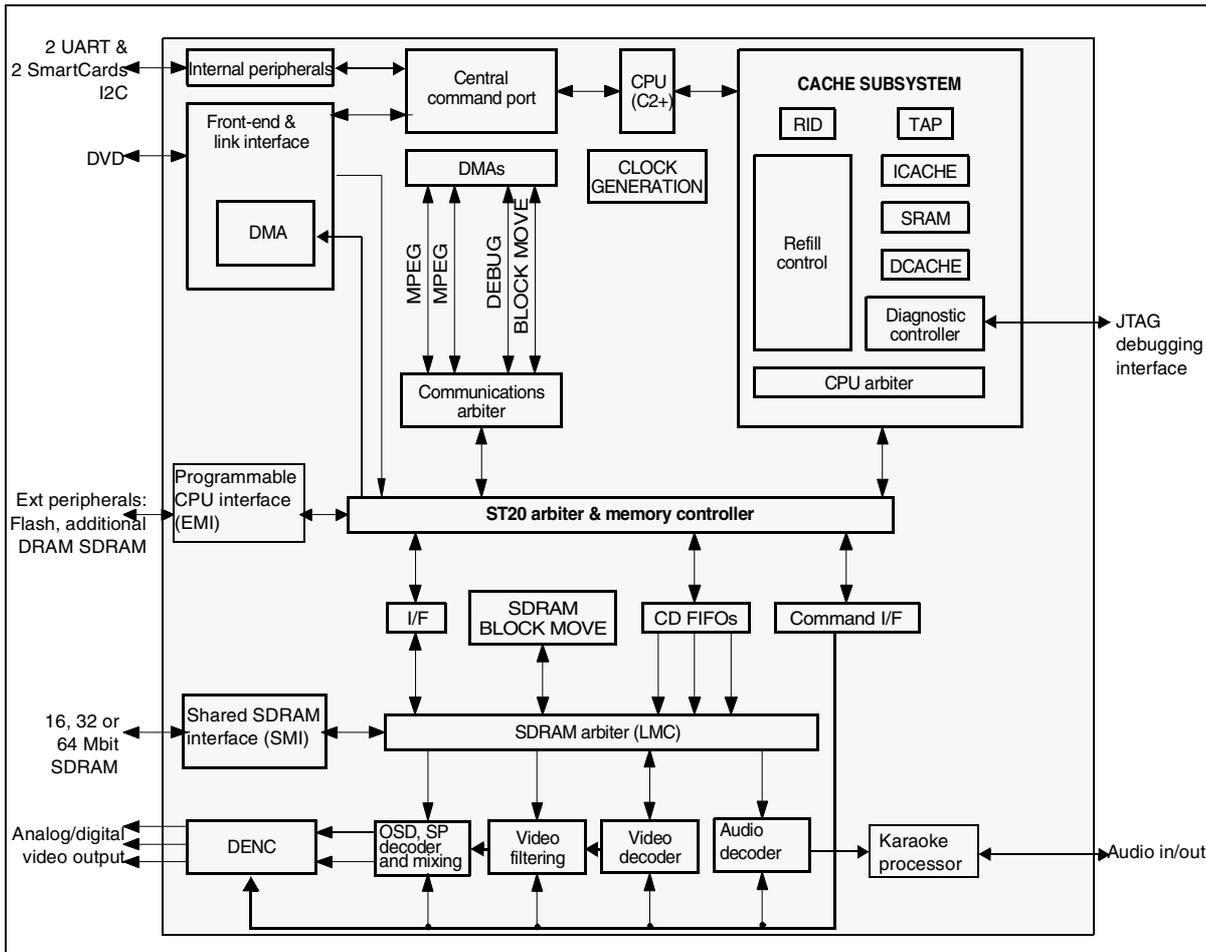


Figure 1 Functional block diagram

1 Architecture overview

STi5508

1.2 Central processor

The STi5508 Central Processing Unit is a ST20C2+ 32-bit processor core. It contains instruction processing logic, instruction and data pointers, and an operand register. It directly accesses the high-speed on-chip SRAM, which can store data or programs and uses the cache to reduce access time to off-chip program and data memory.

The processor can access memory via the Programmable CPU Interface (often referred to as the EMI) or the Shared Memory Interface (SMI), which is shared with the video, audio, sub-picture and OSD decoders.

1.3 MPEG video decoder

This is a real-time video compression processor supporting the MPEG-1 and MPEG-2 standards at video rates up to 720 x 480 x 60 Hz and 720 x 576 x 50 Hz. Picture format conversion for display is performed by vertical and horizontal filters. User-defined bitmaps can be super-imposed on the display picture by using the on-screen display function.

The display unit is part of the MPEG video decoder, it overlays the four display planes shown in the figure below. The display planes are normally overlaid in the order illustrated, with the background color at the back and the sub-picture at the front (used as a cursor plane). The sub-picture plane can alternatively be positioned between the OSD and MPEG video planes where it can be used as a second on-screen display plane.

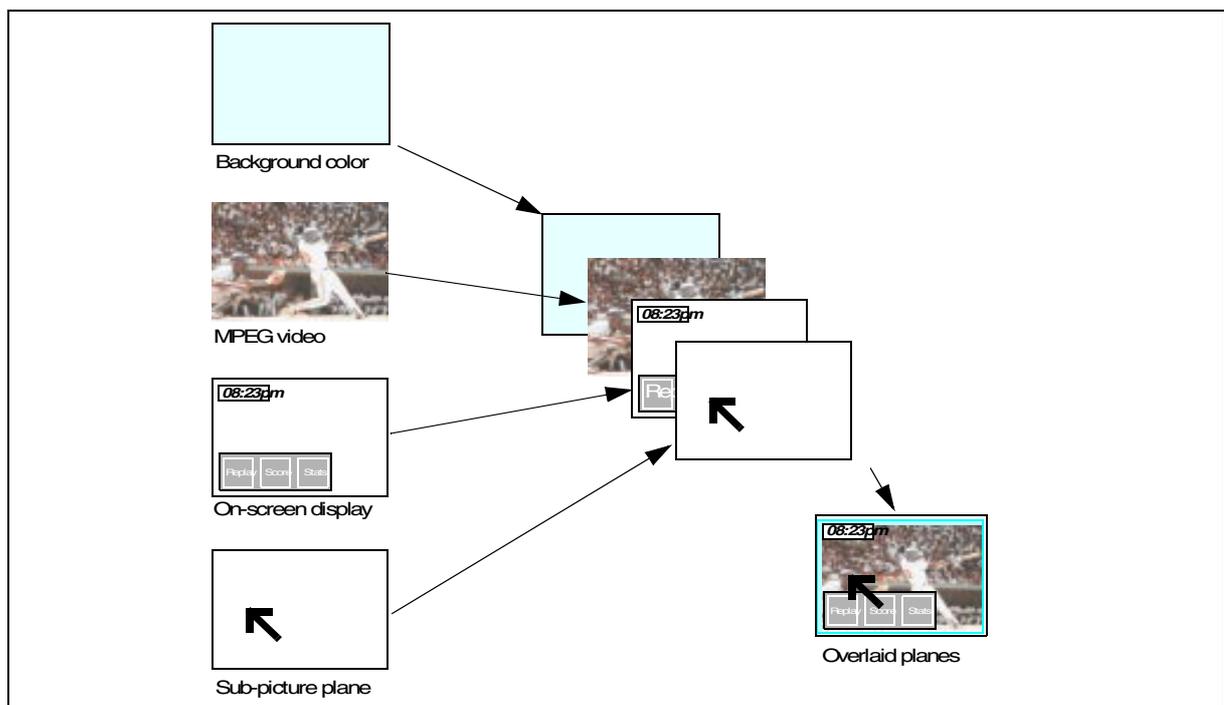


Figure 2 Display planes

STi5508**1 Architecture overview****1.4 Audio decoder**

The audio decoder accepts: Dolby Digital, MPEG-1 layers I and II, MPEG-2 layer II 6-channel, PCM, CDDA data formats; MPEG2 PES streams for MPEG-2, MPEG-1, Dolby Digital, MP3, and Linear PCM (LPCM). The audio decoder supports DTS digital out (DVD DTS and CDDA DTS).

S/PDIF input data (IEC-60958 or IEC-61937 standards) is accepted if an external circuitry extracts the PCM clock from the stream.

Skip frame, repeat blocks and soft mute frame features can be used to synchronize audio and video data. PTS audio extraction is also supported.

The device outputs up to 6 channels of PCM data and appropriate clocks for external digital-to-analog converters.

Programmable downmix enables 1,2,3 or 4 channel outputs. Data can be output in either I²S format or Sony format. The decoder can format output data according to IEC-60958 standard (for non compressed data: L/R channels, 16, 18, 20 and 24-bits) or IEC-61937 standard (for compressed data), for $F_S = 96\text{kHz}$, 48kHz, 44.1kHz or 32kHz.

Sampling frequencies of 96kHz, 48kHz, 44.1kHz, 32kHz and half sampling frequencies are supported. A downsampling filter (96kHz/48kHz) is available.

The decoder supports dual mode for MPEG and Dolby Digital. It is karaoke aware and capable in Dolby Digital and MPEG formats according to DVD specifications. It includes a Dolby surround compatible downmix and a ProLogic decoder.

A pink noise generator enables the accurate positioning of speakers for optimal surround sound setup.

In global mute mode, the decoder decodes the incoming bitstream normally but the PCM and SPDIF outputs are softmuted. This mode is used to prepare a period of decoding mode, to synchronize audio and video data without hearing the audio.

Slow-forward and fast-forward trick modes are available for compressed and non-compressed data.

The control interface of the decoder is activated via memory mapped registers in the ST20 address space.

1.5 Karaoke

The karaoke processor is a post-processing module which supports the following features: 2 micro PCM input, pitch shift, echo effect, reverberation, chorus, voice cancellation, level-sensitive vocal cancelling, vocal partnering, independant volume control on music and vocal channels.

1.6 Modem analog front-end interface

The Modem Analog Front-end interface is used to transfer transmit and receive DAC and ADC samples between the memory and an external modem analog front-end (MAFE), using a synchronous serial protocol. DMA is used to transfer the sample data between memory buffers and the MAFE interface module, with separate transmit and receive buffers and double buffering of the buffer pointers. FIFOs are used to take into account the access latency to memory, in a worst case system and to allow the use of bursts for memory bandwidth efficiency improvement. The V22 bis standard is supported.

1.7 Memory subsystem**On-chip**

The on-chip memory includes 2Kbytes of instruction cache, 2Kbytes of data cache and 4Kbytes of SRAM that can be optionally configured as data cache. The subsystem provides 240M/bytes of internal bandwidth, supporting pipelined 2-cycle internal memory access.

1 Architecture overview

STi5508

The instruction and data caches are direct-mapped, with a write-back system for the data-cache. The caches support burst accesses to the external memories for refill and write-back. Burst access increases the performance of page-mode DRAM memories.

Off-chip

There are two off-chip memory interfaces:

- The external memory interface (EMI) accessed by the ST20 is used for the transfer of data and programs between the STi5508 and external peripherals, flash and additional SDRAM and DRAM.
- Shared memory interface (SMI) controls the movement of data between the STi5508 and 16, 32 or 64 Mbits of SDRAM. This external SDRAM stores the display data generated by the MPEG decoder and CPU and the C2+ code data.

The EMI uses minimal external support logic to support memory subsystems, and accesses a 32 Mbytes of physical address space (greater if SDRAM or DRAM is used) in four general purpose memory banks of 8 or 16 bits wide, 21 or 22 address lines, and byte select. For applications requiring extra memory, the EMI supports this extra memory with zero external support logic, even for 16-bit SDRAM devices. The EMI can be configured for a wide variety of timing and decode functions by the configuration registers. The timing of each of the four memory banks can be set separately, with different device types being placed in each bank with no need for external hardware.

1.8 Serial communication

Asynchronous serial controllers

The Asynchronous Serial Controller (ASC), also referred to as the UART interface, provides serial communication between the STi5508 and other microcontrollers, microprocessors or external peripherals. The STi5508 has four ASCs, two of which are generally used by the SmartCard controllers.

Eight or nine bit data transfer, parity generation, and the number of stop bits are programmable. Parity, framing, and overrun error detection increase data transfer reliability. Transmission and reception of data can be double-buffered, or 16-deep FIFOs can be used. A mechanism to distinguish the address from the data bytes is included for multiprocessor communication. Testing is supported by a loop-back option. A 16-bit baud-rate generator provides the ASC with a separate serial clock signal.

Each ASC supports full-duplex asynchronous communication where both the transmitter and the receiver use the same data frame format and the same baud-rate. Each ASC can be set to operate in SmartCard mode for use when interfacing to a SmartCard.

Synchronous serial control

The Synchronous Serial Controller (SSC) provides a high-speed interface to a wide variety of serial memories, remote control receivers and other microcontrollers. The SSC supports all of the features of the Serial Peripheral Interface bus (SPI) and the I²C bus. The SSC can be programmed to interface to other serial bus standards. The SSC shares pins with the parallel input/output (PIO) ports, and support full-duplex and half-duplex synchronous communication when used in conjunction with the PIO configuration.

1.9 Front-end interface

The STi5508 can be connected to a front-end through the following interfaces:

- I2S interface;
- multi-format serial interface;
- multi-format parallel interface;

- ATAPI interface (for DVD-ROMs)

1.10 On-chip PLL

The on-chip PLL accepts 27 MHz input and generates all the internal high-frequency clocks needed for the CPU, MPEG and audio subsystems.

1.11 Diagnostic controller (DCU)

The ST20 Diagnostic Controller Unit (DCU) is used to boot the CPU and to control and monitor the chip systems via the standard IEEE 1194.1 Test Access Port. The DCU includes on-chip hardware with ICE (In Circuit Emulation) and LSA (Logic State Analyzer) features to facilitate verification and debugging of software running on the on-chip CPU in real time. It is an independent hardware module with a private link from the host to support real-time diagnostics.

1.12 Interrupt subsystem

The interrupt system allows an on-chip module or external interrupt pin to interrupt an active process so that an interrupt handling process can be run. An interrupt can be signalled by one of the following: a signal on an external interrupt pin, a signal from an internal peripheral or subsystem, software asserting an interrupt in the pending register.

Interrupts are implemented by an on-chip interrupt controller and an on-chip interrupt-level controller. The interrupt controller supports eight prioritized interrupts as inputs and manages the pending interrupts. This allows the nesting of pre-emptive interrupts for real-time system design. Each interrupt can be programmed to be at a lower or higher priority than the high priority process queue.

1.13 PAL/NTSC/SECAM encoder

The integrated digital encoder converts a multiplexed 4:2:2 or 4:4:4 YCbCr stream into a standard analog baseband PAL/NTSC or SECAM signal and into RGB, YUV, Yc and CVBS components. The encoder can perform closed-caption, CGMS encoding, and allows Macrovision™ 7.01/6.1 copy protection.

1.14 SmartCard interfaces

Two SmartCard interfaces support SmartCards compliant with ISO7816-3. Each interface is has a UART (ASC), a dedicated programmable clock generator, and eight bits of parallel IO port.

1.15 PWM and counter module

The PWM and counter module provides three PWM encoder outputs, three PWM decoder (capture) inputs and four programmable timers. Each capture input can be programmed to detect rising edge, falling edge, both edges or neither edge (disabled). These facilities are clocked by two independent clocks, one for PWM outputs and one for capture inputs/timers. The PWM counter is 8-bit, with 8-bit registers to set the output-high time. The capture/compare counter and the compare and capture registers are 32-bit. The module generates a single interrupt signal.

1.16 Parallel I/O module

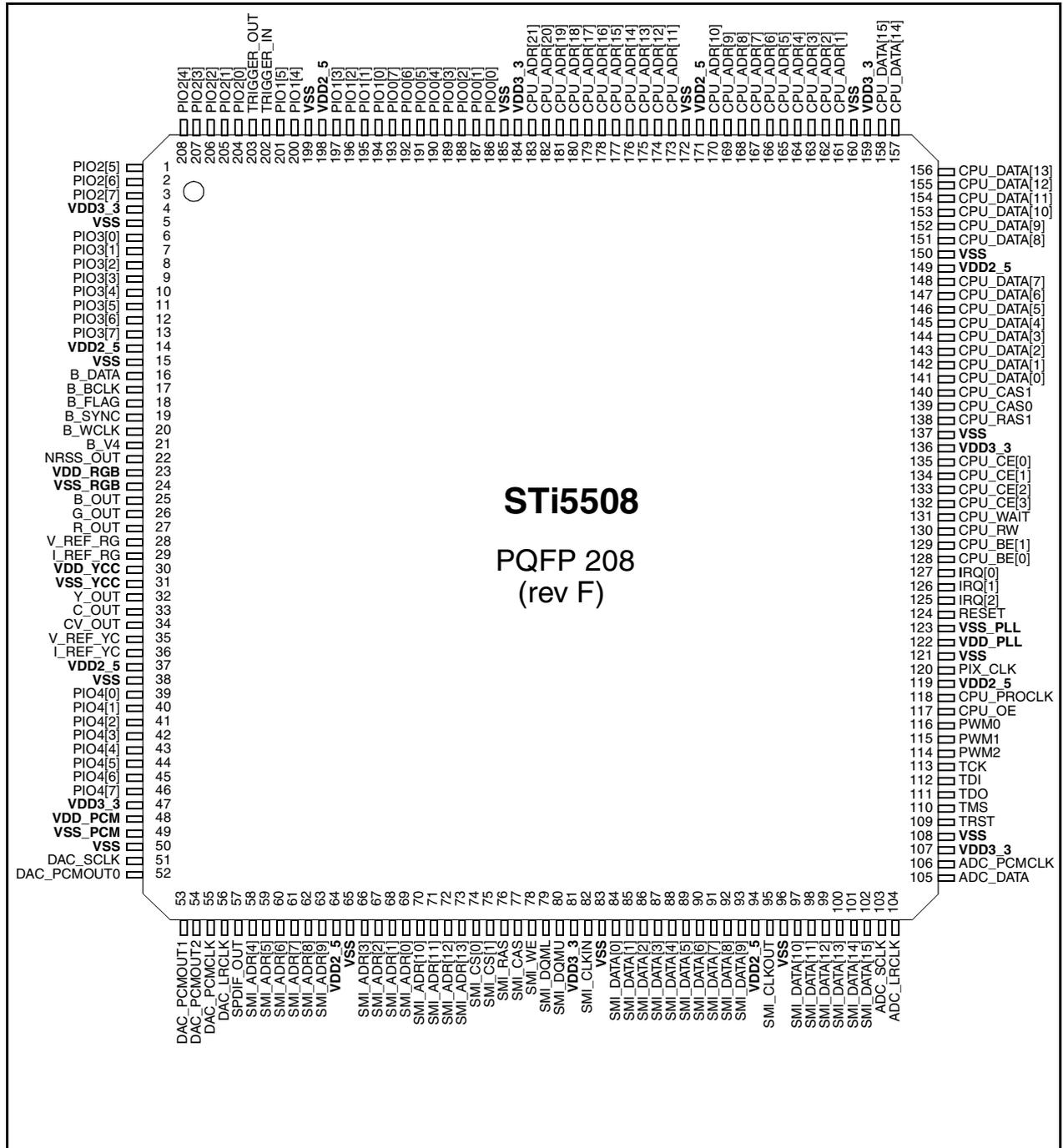
38 bits of parallel I/O are configured in 5 ports, and each bit is programmable as output or input. The output can be configured as a totem-pole or open-drain driver. The input compare logic can generate an interrupt on any change of any input bit. Many parallel IO have alternate functions and can be connected to an internal peripheral signal such as a UART or SSC.

2 Pin data

STi5508

2 Pin data

2.1 Pin out



STi5508

2 Pin data

2.2 Pin list sorted by function

Alternate functions printed in *Italic* show a suggested use of the PIO; alternate functions not printed in *Italic* are multiplexed with a specific hardware.

Pin number	Pin name	Main function	Alternate function		Type
			Input	Output	
Audio DAC					
51	DAC_SCLK	OVER SAMPLING CLK		EXT_AUD_CLK	O
52	DAC_PCMOUT0	PCM_OUT0		EXT_AUD_DATA	O
53	DAC_PCMOUT1	PCM_OUT1	EXT_AUD_REQ		I/O
54	DAC_PCMOUT2	PCM_OUT2			O
55	DAC_PCMCLK	PCM_CLOCK			I/O
56	DAC_LRCLK	LEFT/RIGHT CLK		EXT_AUD_WCLK	O
57	SPDIF_OUT	SPDIF_OUT			O
48	VDD_PCM	VDD FREQ SYNTH=2.5V			PWR 2.5V
49	VSS_PCM	VSS FREQ SYNTH=GND			PWR
Audio ADC input					
104	ADC_LRCLK	Left/Right Clock			I/O
106	ADC_PCMCLK	PCM CLOCK			I/O
105	ADC_DATA	DATA			I
103	ADC_SCLK	SAMPLING CLK			I/O
Clock & reset					
124	RESET	CHIP RESET			I
122	VDD_PLL	VDD PLL=2.5V			PWR 2.5V
123	VSS_PLL	GND PLL=GND			PWR
120	PIX_CLK	27 MHz main clock			I
PIOs and communication					
186	PIO0[0]	PIO0[0]	UART0_DATA (<i>SC0_DATA</i>)		I/O
187	PIO0[1]	PIO0[1]		ATAPI_RD	I/O
188	PIO0[2]	PIO0[2]		ATAPI_WR	I/O
189	PIO0[3]	PIO0[3]		SC0_CLOCK	I/O
190	PIO0[4]	PIO0[4]		SC0_RST	I/O
191	PIO0[5]	PIO0[5]		SC0_CMD_VCC	I/O
192	PIO0[6]	PIO0[6]		SC0_DATA_DIR	I/O
193	PIO0[7]	PIO0[7]	SC0_DETECT		I/O
194	PIO1[0]	PIO1[0]	SSC0_DATA (MTSROut/MRSTin)		I/O
195	PIO1[1]	PIO1[1]	SSC0_CLOCK		I/O
196	PIO1[2]	PIO1[2]	SC EXTERNAL CLOCK	PARA_DVALID	I/O
197	PIO1[3]	PIO1[3]		UART2_TXD	I/O
200	PIO1[4]	PIO1[4]	UART2_RXD		I/O

Table 1 Pins sorted by function

2 Pin data

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Pin number	Pin name	Main function	Alternate function		Type
			Input	Output	
201	PIO1[5]	PIO1[5]	PARA_SYNC	UART1_TXD	I/O
202	TRIGGER_IN	TRIGGER_IN for DCU			I/O
203	TRIGGER_OUT	TRIGGER_OUT for DCU			I/O
204	PIO2[0]	PIO2[0]	UART3_DATA (SC1_DATA)		I/O
205	PIO2[1]	PIO2[1]	UART1_RXD	MAFEIF_DOUT PARA_REQ	I/O
206	PIO2[2]	PIO2[2]	PARA_STROBE	MAFEIF_HC1	I/O
207	PIO2[3]	PIO2[3]		SC1_CLOCK	I/O
208	PIO2[4]	PIO2[4]		SC1_RST	I/O
1	PIO2[5]	PIO2[5]		SC1_CMD_VCC	I/O
2	PIO2[6]	PIO2[6]		SC1_DATA_DIR	I/O
3	PIO2[7]	PIO2[7]	SC1_DETECT		I/O
6	PIO3[0]	PIO3[0]	MAFEIF_SCLK PARA_DATA[0]		I/O
7	PIO3[1]	PIO3[1]	MAFEIF_DIN PARA_DATA[1]		I/O
8	PIO3[2]	PIO3[2]	MAFEIF_FSI PARA_DATA[2]		I/O
9	PIO3[3]	PIO3[3]	CAPTURE_IN0 PARA_DATA[3]		I/O
10	PIO3[4]	PIO3[4]	CAPTURE_IN1 PARA_DATA[4]		I/O
11	PIO3[5]	PIO3[5]	CAPTURE_IN2 PARA_DATA[5]		I/O
12	PIO3[6]	PIO3[6]	PARA_DATA[6]	COMP_OUT1	I/O
13	PIO3[7]	PIO3[7]	PARA_DATA[7]	COMP_OUT0	I/O
39-46	PIO4[0:7]	PIO4[0:7]	YC[0:7]		I/O
			SSC1_DATA/ NRSS_CLOCK ¹		
			SSC1_CLOCK		
			SDAV_CLK/ P1394_Clk ²		
			SDAV_DATA ²		
			SDAV_DIR / P1394_P_CLK ²		
			OSC_IN_CLK ²		
EMI Interface					
161-170	CPU_ADR[1:10]	ADR[1:10]			O
173-183	CPU_ADR[11:21]	ADR[11:21]			O
141-148	CPU_DATA[0:7]	DATA[0:7]			I/O
151-158	CPU_DATA[8:15]	DATA[8:15]			I/O
138	CPU_RAS1	DRAM RAS		NOT_SDRAM_CS1	I/O
131	CPU_WAIT	WAIT STATE			I

Table 1 Pins sorted by function

STi5508

2 Pin data

Pin number	Pin name	Main function	Alternate function		Type
			Input	Output	
130	CPU_RW	READ-NOT WRITE		NOT_SDRAM_WE	O
128	CPU_BE[0]	BYTE 0 ENABLE		DQM[0]	O
129	CPU_BE[1]	BYTE 1 ENABLE		DQM[1]	O
139	CPU_CAS0	DRAM CAS0		SDRAM_CAS/ CPU_ADR[22]	O
140	CPU_CAS1	DRAM		NOT_SDRAM_CS0	O
135	CPU_CE[0]	DRAM_RAS0		SDRAM_RAS	O
134	CPU_CE[1]	CHIP SEL. BANK 1			O
133	CPU_CE[2]	CHIP SEL. BANK 2			O
132	CPU_CE[3]	CHIP SEL. BANK 3		CS_SUB_BANK3	O
118	CPU_RAM_CLK	SDRAM CLOCK			O
117	CPU_OE	OUTPUT ENABLE			I/O
Interrupt					
127	IRQ[0]	IRQ[0] (<i>SERVO_IRQ</i>)			I
126	IRQ[1]	IRQ[1] (<i>ATAPI_IRQ</i>)			I
125	IRQ[2]	IRQ[2] (<i>MD_IRQ</i>)			I
Timers					
116	PWM0	Pulse Width Modula 0	HSYNC		O
115	PWM1	Pulse Width Modula1	BOOT FROM ROM ³		I/O
114	PWM2	Pulse Width Modula 2	VSYNC		O
JTAG					
113	TCK	TEST CLOCK			I
112	TDI	TEST DATA IN			I
111	TDO	TEST DATA OUT			O
110	TMS	TEST MODE SELECT			I
109	TRST ⁴	TEST RESET			I
Front-end					
16	B_DATA	I2S DATA	SER_DATA		I
17	B_BCLK	I2S BIT CLOCK	SER_BCLK		I
18	B_FLAG	I2S ERROR FLAG DVD	SER_VALID		I
19	B_SYNC	I2S SECTOR/ABS TIME	SER_SYNC		I
20	B_WCLK	I2S WORD CLOCK		NRSS CLOCK	I/O
21	B_V4	I2S VERSATILE INPUT PIN	NRSS_IN		I
22	NRSS_OUT	NRSS OUT			O
Video DAC					
27, 26, 25	R_OUT, G_OUT, B_OUT	R_OUT, G_OUT, B_OUT			O
32, 33, 34	Y_OUT, C_OUT, CV_OUT	Y_OUT, C_OUT, CV_OUT			O
29	I_REF_RGB	I_REF_DAC_RGB			I
28	V_REF_RGB	V_REF_DAC_RGB			I
36	I_REF_YCC	I_REF_DAC_YCC			I

Table 1 Pins sorted by function

2 Pin data

STi5508

Pin number	Pin name	Main function	Alternate function		Type
			Input	Output	
35	V_REF_YCC	V_REF_DAC_YCC			I
23	VDD_RGB	VDDA_RGB=2.5V			PWR 2.5V
24	VSS_RGB	VSSA_RGB=GND			PWR
30	VDD_YCC	VDDA_YCC=2.5V			PWR 2.5V
31	VSS_YCC	VSSA_YCC=GND			PWR
Shared memory interface					
69-66	SMI_ADR[0:3]	Address bus SDRAM			O
58-63	SMI_ADR[4:9]	Address bus SDRAM			O
70-73	SMI_ADR [10:13]	Address bus SDRAM			O
84-93, 97-102	SMI_DATA[0:15]	Data bus SDRAM			I/O
74, 75	SMI_CS[0,1]	Chip select bank 0,1			O
76	SMI_RAS	RAS SDRAM			O
77	SMI_CAS	CAS SDRAM			O
78	SMI_WE	SDRAM write enable			O
79, 80	SMI_DQML, U	DQ MASK EN LOW, UP			O
82	SMI_CLKIN	SDRAM CLOCK IN			I
95	SMI_CLKOUT	SDRAM CLOCK OUT			O
Power supply					
4, 47, 81, 107, 136, 159, 184	VDD3_3	3.3 V POWER SUPPLY			PWR
14, 37, 64, 94, 119, 149, 171, 198	VDD2_5	2.5V POWER SUPPLY			PWR
5, 15, 38, 50, 65, 83, 96, 108, 121, 137, 150, 160, 172, 185, 199	VSS	GROUND			PWR

Table 1 Pins sorted by function

1. FEI_CFG bits 8 and 9 must be programmed according to the required NRSS configuration.
2. Register LNK_SDAV_CONF bit 22 (SDE) must be set to 1 to validate the output path.
3. BOOTFROMROM is active during reset.
4. Tie low whenever JTAG is not used.

STi5508

2 Pin data

2.3 Pins sorted by pin number

Pin N°	Pin name	Main function	Alternate function		Dir func.
			Input	Output	
Left Side					
1	PIO2[5]	PIO2[5]		SC1_CMD_VCC	I/O
2	PIO2[6]	PIO2[6]		SC1_DATA_DIR	I/O
3	PIO2[7]	PIO2[7]	SC1_DETECT		I/O
4	VDD3_3	3.3 V POWER SUPPLY			POWER
5	VSS	GROUND			POWER
6	PIO3[0]	PIO3[0]	MAFEIF_SCLK PARA_DATA[0]		I/O
7	PIO3[1]	PIO3[1]	MAFEIF_DIN PARA_DATA[1]		I/O
8	PIO3[2]	PIO3[2]	MAFEIF_FSI PARA_DATA[2]		I/O
9	PIO3[3]	PIO3[3]	CAPTURE_IN0 PARA_DATA[3]		I/O
10	PIO3[4]	PIO3[4]	CAPTURE_IN1 PARA_DATA[4]		I/O
11	PIO3[5]	PIO3[5]	CAPTURE_IN2 PARA_DATA[5]		I/O
12	PIO3[6]	PIO3[6]	PARA_DATA[6]	COMP_OUT1	I/O
13	PIO3[7]	PIO3[7]	PARA_DATA[7]	COMP_OUT0	I/O
14	VDD2_5	2.5V POWER SUPPLY			POWER
15	VSS	GROUND			POWER
16	B_DATA	I2S DATA	SER_DATA		I
17	B_BCLK	I2S BIT CLOCK	SER_BCLK		I
18	B_FLAG	I2S ERROR FLAG DVD	SER_VALID		I
19	B_SYNC	I2S SECTOR/ABS TIME	SER_SYNC		I
			SSC1_DATA/ NRSS_CLOCK ¹		
			SSC1_CLOCK		
			SDAV_CLK/ P1394_CLK ²		
20	B_WCLK	I2S WORD CLOCK		NRSS CLOCK	I/O
21	B_V4	I2S VERSATILE INPUT	NRSS_IN		I
22	NRSS_OUT	NRSS OUT			O
23	VDD_RGB	VDDA_RGB=2.5V			POWER
24	VSS_RGB	VSSA_RGB=GND			POWER
25	B_OUT	B_OUT			O
26	G_OUT	G_OUT			O
27	R_OUT	R_OUT			O
28	V_REF_RGB	V_REF_DAC_RGB			I

Table 2 Pins sorted by number

2 Pin data

STi5508

Pin N°	Pin name	Main function	Alternate function		Dir func.
			Input	Output	
29	I_REF_RGB	I_REF_DAC_RGB			I
30	VDD_YCC	VDDA_YCC=2.5V			POWER
31	VSS_YCC	VSSA_YCC=GND			POWER
32	Y_OUT	Y_OUT			O
33	C_OUT	C_OUT			O
34	CV_OUT	CV_OUT			O
35	V_REF_YCC	V_REF_DAC_YCC			I
36	I_REF_YCC	I_REF_DAC_YCC			I
37	VDD2_5	2.5V POWER SUPPLY			POWER
38	VSS	GROUND			POWER
39	PIO4[0]	PIO4[0]	YC[0]		I/O
40	PIO4[1]	PIO4[1]	YC[1]		I/O
41	PIO4[2]	PIO4[2]	YC[2]		I/O
42	PIO4[3]	PIO4[3]	YC[3]		I/O
43	PIO4[4]	PIO4[4]	YC[4]		I/O
44	PIO4[5]	PIO4[5]	YC[5]		I/O
45	PIO4[6]	PIO4[6]	YC[6]		I/O
46	PIO4[7]	PIO4[7]	YC[7]		I/O
47	VDD3_3	3.3 V POWER SUPPLY			POWER
48	VDD_PCM	VDD FREQ SYNTH=2.5V			POWER
49	VSS_PCM	VSS FREQ SYNTH=GND			POWER
50	VSS	GROUND			POWER
51	DAC_SCLK	SAMPLING CLK		EXT_AUD_CLK	O
52	DAC_PCMOUT0	PCM_OUT0		EXT_AUD_DATA	O
Bottom side					
53	DAC_PCMOUT1	PCM_OUT1	EXT_AUD_REQ		I/O
54	DAC_PCMOUT2	PCM_OUT2			O
55	DAC_PCMCLK	PCM_CLOCK			I/O
56	DAC_LRCLK	LEFT/RIGHT CLK		EXT_AUD_WCLK	O
57	SPDIF_OUT	SPDIF_OUT			O
58	SMI_ADR[4]	Adress bus SDRAM			O
59	SMI_ADR[5]	Adress bus SDRAM			O
60	SMI_ADR[6]	Adress bus SDRAM			O
61	SMI_ADR[7]	Adress bus SDRAM			O
62	SMI_ADR[8]	Adress bus SDRAM			O
63	SMI_ADR[9]	Adress bus SDRAM			O
64	VDD2_5	2.5V POWER SUPPLY			POWER
65	VSS	GROUND			POWER
66	SMI_ADR[3]	Adress bus SDRAM			O
67	SMI_ADR[2]	Adress bus SDRAM			O

Table 2 Pins sorted by number

STi5508

2 Pin data

Pin N°	Pin name	Main function	Alternate function		Dir func.
			Input	Output	
68	SMI_ADR[1]	Adress bus SDRAM			O
69	SMI_ADR[0]	Adress bus SDRAM			O
70	SMI_ADR[10]	Adress bus SDRAM			O
71	SMI_ADR[11]	Adress bus SDRAM			O
72	SMI_ADR[12]	Adress bus SDRAM			O
73	SMI_ADR[13]	Adress bus SDRAM			O
74	SMI_CS[0]	Chip select bank 0			O
75	SMI_CS[1]	Chip select bank 1			O
76	SMI_RAS	RAS SDRAM			O
77	SMI_CAS	CAS SDRAM			O
78	SMI_WE	SDRAM write enable			O
79	SMI_DQML	DQ MASK EN LOW			O
80	SMI_DQMU	DQ MASK EN UP			O
81	VDD3_3	3.3 V POWER SUPPLY			POWER
82	SMI_CLKIN	SDRAM CLOCK IN			I
83	VSS	GROUND			POWER
84	SMI_DATA[0]	Data bus SDRAM			I/O
85	SMI_DATA[1]	Data bus SDRAM			I/O
86	SMI_DATA[2]	Data bus SDRAM			I/O
87	SMI_DATA[3]	Data bus SDRAM			I/O
88	SMI_DATA[4]	Data bus SDRAM			I/O
89	SMI_DATA[5]	Data bus SDRAM			I/O
90	SMI_DATA[6]	Data bus SDRAM			I/O
91	SMI_DATA[7]	Data bus SDRAM			I/O
92	SMI_DATA[8]	Data bus SDRAM			I/O
93	SMI_DATA[9]	Data bus SDRAM			I/O
94	VDD2_5	2.5V POWER SUPPLY			POWER
95	SMI_CLKOUT	SDRAM CLOCK OUT			O
96	VSS	GROUND			POWER
97	SMI_DATA[10]	Data bus SDRAM			I/O
98	SMI_DATA[11]	Data bus SDRAM			I/O
99	SMI_DATA[12]	Data bus SDRAM			I/O
100	SMI_DATA[13]	Data bus SDRAM			I/O
101	SMI_DATA[14]	Data bus SDRAM			I/O
102	SMI_DATA[15]	Data bus SDRAM			I/O
103	ADC_SCLK	SAMPLING CLK			I/O
104	ADC_LRCLK	Left/Right Clock			I/O
			SDAV_DATA ²		
			Sdav_dir / P1394_P_CLK ²		
Right side					

Table 2 Pins sorted by number

2 Pin data

STi5508

Pin N°	Pin name	Main function	Alternate function		Dir func.
			Input	Output	
105	ADC_DATA	DATA			I
106	ADC_PCMCLK	PCM CLOCK			I/O
			OSC_IN_CLK ²		
107	VDD3_3	3.3 V POWER SUPPLY			POWER
108	VSS	GROUND			POWER
109	TRST ³	TEST RESET			I
110	TMS	TEST MODE SELECT			I
111	TDO	TEST DATA OUT			O
112	TDI	TEST DATA IN			I
113	TCK	TEST CLOCK			I
114	PWM2	Pulse Width Modul 2	VSYNC		O
115	PWM1	Pulse Width Modul 1	BOOT_FROM_ROM ⁴		I/O
116	PWM0	Pulse Width Modul 0	HSYNC		O
117	CPU_OE	OUTPUT ENABLE			I/O
118	CPU_RAM_CLK	SDRAM CLOCK			O
119	VDD2_5	2.5V POWER SUPPLY			POWER
120	PIX_CLK	27 MHz main clock			I
121	VSS	GROUND			POWER
122	VDD_PLL	VDD PLL=2.5V			POWER
123	VSS_PLL	GND PLL=GND			POWER
124	RESET	CHIP RESET			I
125	IRQ[2]	IRQ[2] (<i>MD_IRQ</i>)			I
126	IRQ[1]	IRQ[1] (<i>ATAPI_IRQ</i>)			I
127	IRQ[0]	IRQ[0] (<i>SERVO_IRQ</i>)			I
128	CPU_BE[0]	BYTE 0 ENABLE		DQM[0]	O
129	CPU_BE[1]	BYTE 1 ENABLE		DQM[1]	O
130	CPU_RW	READ-NOT WRITE		NOT_SDRAM_WE	O
131	CPU_WAIT	WAIT STATE			I
132	CPU_CE[3]	CHIP SEL. BANK 3		CS_SUB_BANK3	O
133	CPU_CE[2]	CHIP SEL. BANK 2			O
134	CPU_CE[1]	CHIP SEL. BANK 1			O
135	CPU_CE[0]	DRAM_RAS0		SDRAM_RAS	O
136	VDD3_3	3.3 V POWER SUPPLY			POWER
137	VSS	GROUND			POWER
138	CPU_RAS1	DRAM RAS		NOT_SDRAM_CS1	I/O
139	CPU_CAS0	DRAM CAS0		SDRAM_CAS/ CPU_ADR[22]	O
140	CPU_CAS1	DRAM		NOT_SDRAM_CS0	O
141	CPU_DATA[0]	DATA[0]			I/O
142	CPU_DATA[1]	DATA[1]			I/O

Table 2 Pins sorted by number

STi5508

2 Pin data

Pin N°	Pin name	Main function	Alternate function		Dir func.
			Input	Output	
143	CPU_DATA[2]	DATA[2]			I/O
144	CPU_DATA[3]	DATA[3]			I/O
145	CPU_DATA[4]	DATA[4]			I/O
146	CPU_DATA[5]	DATA[5]			I/O
147	CPU_DATA[6]	DATA[6]			I/O
148	CPU_DATA[7]	DATA[7]			I/O
149	VDD2_5	2.5V POWER SUPPLY			POWER
150	VSS	GROUND			POWER
151	CPU_DATA[8]	DATA[8]			I/O
152	CPU_DATA[9]	DATA[9]			I/O
153	CPU_DATA[10]	DATA[10]			I/O
154	CPU_DATA[11]	DATA[11]			I/O
155	CPU_DATA[12]	DATA[12]			I/O
156	CPU_DATA[13]	DATA[13]			I/O
Top side					
157	CPU_DATA[14]	DATA[14]			I/O
158	CPU_DATA[15]	DATA[15]			I/O
159	VDD3_3	3.3 V POWER SUPPLY			POWER
160	VSS	GROUND			POWER
161	CPU_ADR[1]	ADR[1]			O
162	CPU_ADR[2]	ADR[2]			O
163	CPU_ADR[3]	ADR[3]			O
164	CPU_ADR[4]	ADR[4]			O
165	CPU_ADR[5]	ADR[5]			O
166	CPU_ADR[6]	ADR[6]			O
167	CPU_ADR[7]	ADR[7]			O
168	CPU_ADR[8]	ADR[8]			O
169	CPU_ADR[9]	ADR[9]			O
170	CPU_ADR[10]	ADR[10]			O
171	VDD2_5	2.5V POWER SUPPLY			POWER
172	VSS	GROUND			POWER
173	CPU_ADR[11]	ADR[11]			O
174	CPU_ADR[12]	ADR[12]			O
175	CPU_ADR[13]	ADR[13]			O
176	CPU_ADR[14]	ADR[14]			O
177	CPU_ADR[15]	ADR[15]			O
178	CPU_ADR[16]	ADR[16]			O
179	CPU_ADR[17]	ADR[17]			O
180	CPU_ADR[18]	ADR[18]			O
181	CPU_ADR[19]	ADR[19]			O

Table 2 Pins sorted by number

2 Pin data

STI5508

Pin N°	Pin name	Main function	Alternate function		Dir func.
			Input	Output	
182	CPU_ADR[20]	ADR[20]			O
183	CPU_ADR[21]	ADR[21]			O
184	VDD3_3	3.3 V POWER SUPPLY			POWER
185	VSS	GROUND			POWER
186	PIO0[0]	PIO0[0]	UART0_DATA (SC0_DATA)		I/O
187	PIO0[1]	PIO0[1]		ATAPI_RD	I/O
188	PIO0[2]	PIO0[2]		ATAPI_WR	I/O
189	PIO0[3]	PIO0[3]		SC0_CLOCK	I/O
190	PIO0[4]	PIO0[4]		SC0_RST	I/O
191	PIO0[5]	PIO0[5]		SC0_CMD_VCC	I/O
192	PIO0[6]	PIO0[6]		SC0_DATA_DIR	I/O
193	PIO0[7]	PIO0[7]	SC0_DETECT		I/O
194	PIO1[0]	PIO1[0]	SSC0_DATA		I/O
195	PIO1[1]	PIO1[1]	SSC0_CLOCK		I/O
196	PIO1[2]	PIO1[2]	SC EXTERNAL CLOCK	PARA_DVALID	I/O
197	PIO1[3]	PIO1[3]		UART2_TXD	I/O
198	VDD2_5	2.5V POWER SUPPLY			POWER
199	VSS	GROUND			POWER
200	PIO1[4]	PIO1[4]	UART2_RXD		I/O
201	PIO1[5]	PIO1[5]	PARA_SYNC	UART1_TXD	I/O
202	TRIGGER_IN	TRIGGER_IN for DCU			I/O
203	TRIGGER_OUT	TRIGGER_OUT for DCU			I/O
204	PIO2[0]	PIO2[0]	UART3_DATA (SC1_DATA)		I/O
205	PIO2[1]	PIO2[1]	UART1_RXD	MAFEIF_DOUT PARA_REQ	I/O
206	PIO2[2]	PIO2[2]	PARA_STROBE	MAFEIF_HC1	I/O
207	PIO2[3]	PIO2[3]		SC1_CLOCK	I/O
208	PIO2[4]	PIO2[4]		SC1_RST	I/O

Table 2 Pins sorted by number

1. FEI_CFG bits 8 and 9 must be programmed according to the required NRSS configuration.
2. Register LNK_SDAV_CONF bit 22 (SDE) must be set to 1 to validate the output path.
3. Tie low whenever JTAG is not used
4. BOOTFROMROM is active during reset.

M24C64 M24C32

64/32 Kbit Serial I²C Bus EEPROM

- Compatible with I²C Extended Addressing
- Two Wire I²C Serial Interface
Supports 400 kHz Protocol
- Single Supply Voltage:
 - 4.5V to 5.5V for M24Cxx
 - 2.5V to 5.5V for M24Cxx-W
 - 1.8V to 3.6V for M24Cxx-R
- Hardware Write Control
- BYTE and PAGE WRITE (up to 32 Bytes)
- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Behavior
- 1 Million Erase/Write Cycles (minimum)
- 40 Year Data Retention (minimum)

DESCRIPTION

These I²C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 8192x8 bits (M24C64) and 4096x8 bits (M24C32), and operate down to 2.5 V (for the -W version of each device), and down to 1.8 V (for the -R version of each device).

The M24C64 and M24C32 are available in Plastic Dual-in-Line, Plastic Small Outline and Thin Shrink Small Outline packages.

Table 1. Signal Names

E0, E1, E2	Chip Enable Inputs
SDA	Serial Data/Address Input/Output
SCL	Serial Clock
\overline{WC}	Write Control
V _{CC}	Supply Voltage
V _{SS}	Ground

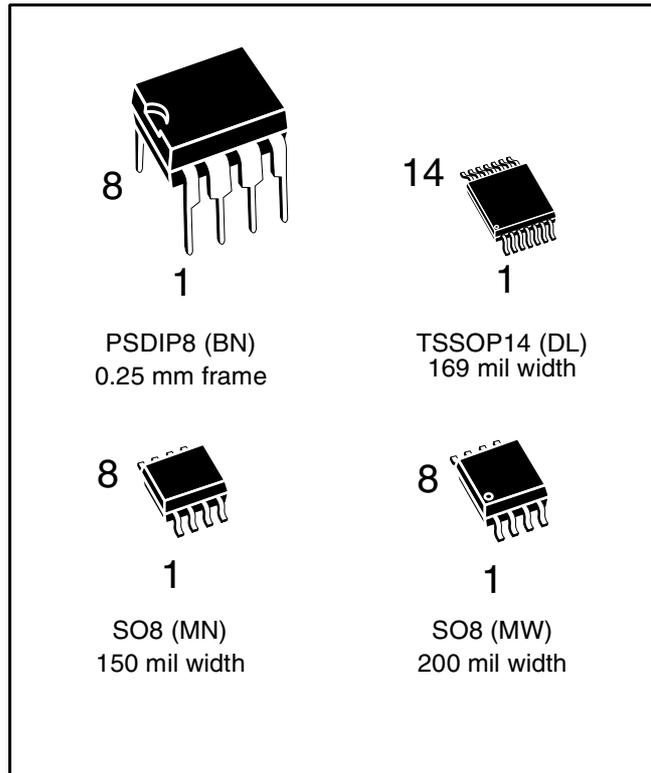
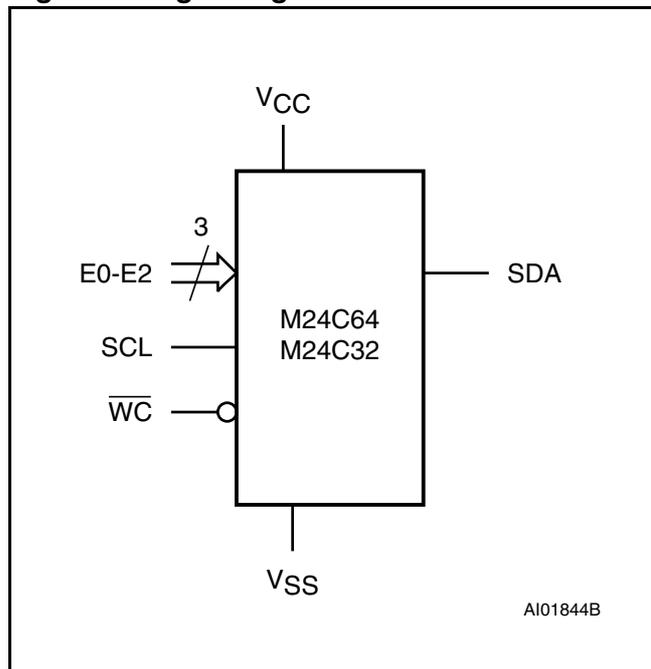


Figure 1. Logic Diagram



M24C64, M24C32

Figure 2A. DIP Connections

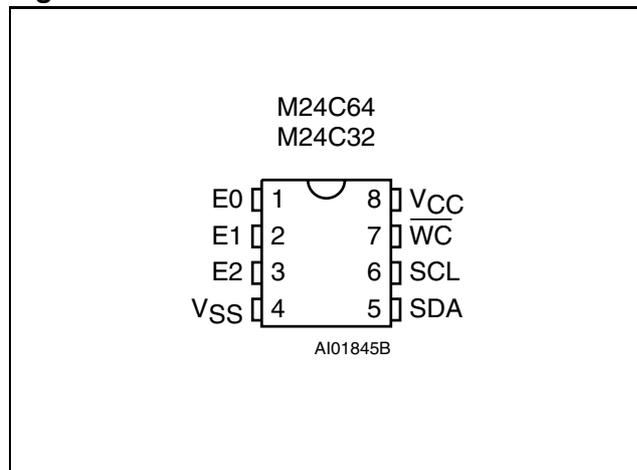
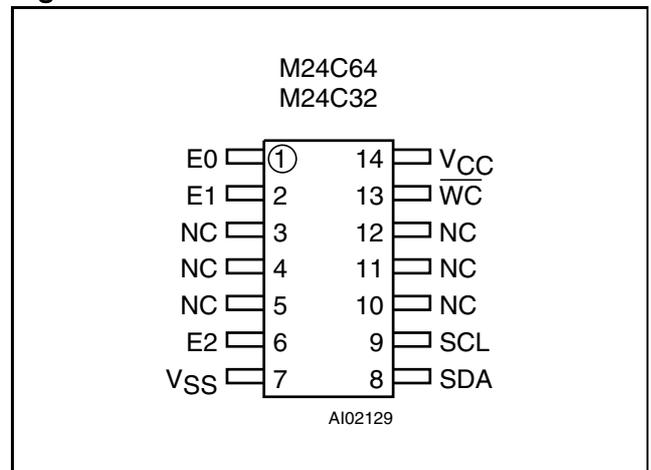
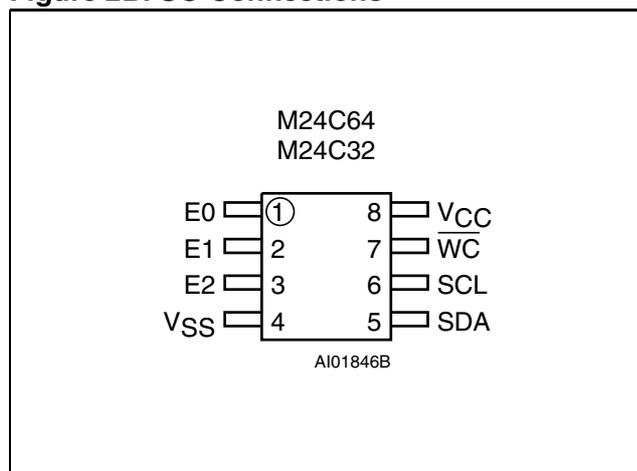


Figure 2C. TSSOP Connections



Note: 1. NC = Not Connected

Figure 2B. SO Connections



These memory devices are compatible with the I²C extended memory standard. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The memory carries a built-in 4-bit unique Device Type Identifier code (1010) in accordance with the I²C bus definition.

The memory behaves as a slave device in the I²C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a Device Select Code and RW bit (as described in Table 3), terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission.

Table 2. Absolute Maximum Ratings ¹

Symbol	Parameter	Value	Unit
T _A	Ambient Operating Temperature	-40 to 125	°C
T _{STG}	Storage Temperature	-65 to 150	°C
T _{LEAD}	Lead Temperature during Soldering	PSDIP8: 10 sec SO8: 40 sec TSSOP14: t.b.c.	260 215 t.b.c. °C
V _{IO}	Input or Output range	-0.6 to 6.5	V
V _{CC}	Supply Voltage	-0.3 to 6.5	V
V _{ESD}	Electrostatic Discharge Voltage (Human Body model) ²	4000	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.

2. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)



M29W160DT M29W160DB

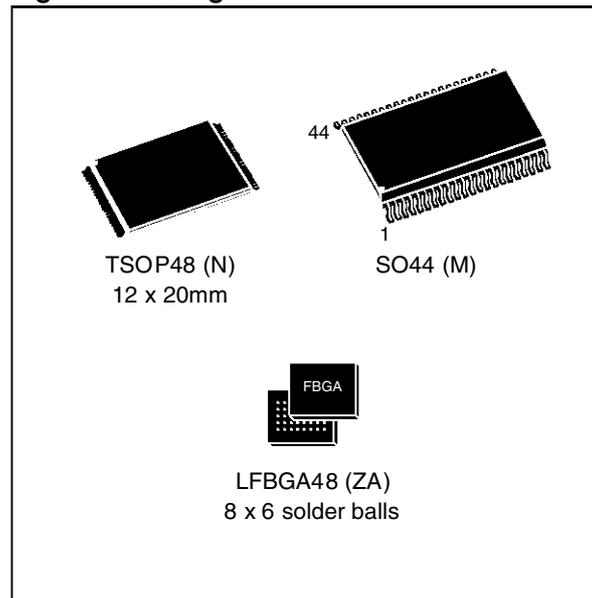
16 Mbit (2Mb x8 or 1Mb x16, Boot Block)
3V Supply Flash Memory

PRELIMINARY DATA

FEATURES SUMMARY

- SINGLE 2.7 to 3.6V SUPPLY VOLTAGE for PROGRAM, ERASE and READ OPERATIONS
- ACCESS TIME: 70ns
- PROGRAMMING TIME
 - 10µs per Byte/Word typical
- 35 MEMORY BLOCKS
 - 1 Boot Block (Top or Bottom Location)
 - 2 Parameter and 32 Main Blocks
- PROGRAM/ERASE CONTROLLER
 - Embedded Program and Erase algorithms
- ERASE SUSPEND and RESUME MODES
 - Read and Program another Block during Erase Suspend
- UNLOCK BYPASS PROGRAM COMMAND
 - Faster Production/Batch Programming
- TEMPORARY BLOCK UNPROTECTION MODE
- SECURITY MEMORY BLOCK
- LOW POWER CONSUMPTION
 - Standby and Automatic Standby
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
 - Manufacturer Code: 0020h
 - Top Device Code M29W160DT: 22C4h
 - Bottom Device Code M29W160DB: 2249h

Figure 1. Packages



M29W160DT, M29W160DB**SUMMARY DESCRIPTION**

The M29W160D is a 16 Mbit (2Mb x8 or 1Mb x16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6V) supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Each block can be protected independently to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents.

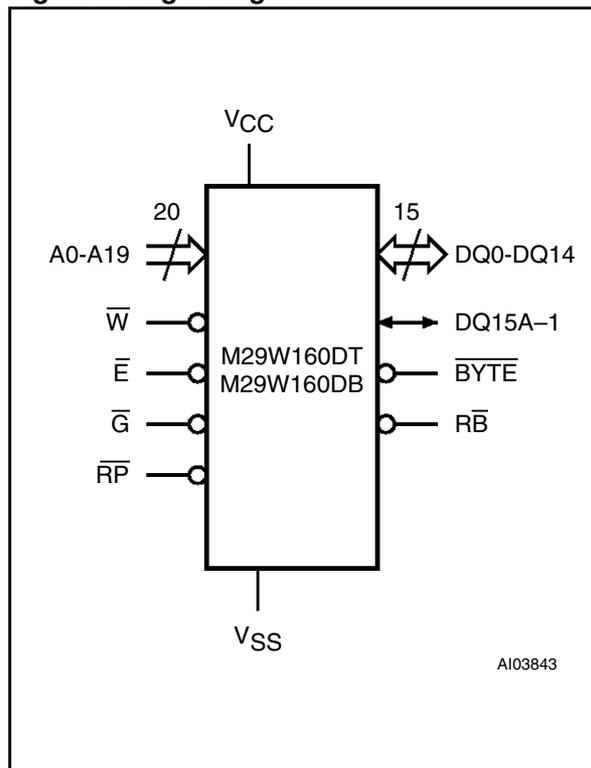
The end of a program or erase operation can be detected and any error conditions identified. The

command set required to control the memory is consistent with JEDEC standards.

The blocks in the memory are asymmetrically arranged, see Tables 2 and 3, Block Addresses. The first or last 64 Kbytes have been divided into four additional blocks. The 16 Kbyte Boot Block can be used for small initialization code to start the micro-processor, the two 8 Kbyte Parameter Blocks can be used for parameter storage and the remaining 32K is a small Main Block where the application may be stored.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered in TSOP48 (12 x 20mm), SO44 and LFBGA48 (0.8mm pitch) packages and it is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

Note: $\overline{R\overline{B}}$ not available on SO44 package.

Table 1. Signal Names

A0-A19	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
DQ8-DQ14	Data Inputs/Outputs
DQ15A-1	Data Input/Output or Address Input
\overline{E}	Chip Enable
\overline{G}	Output Enable
\overline{W}	Write Enable
$\overline{R\overline{P}}$	Reset/Block Temporary Unprotect
$\overline{R\overline{B}}$	Ready/Busy Output (Not available on SO44 package)
\overline{BYTE}	Byte/Word Organization Select
VCC	Supply Voltage
VSS	Ground
NC	Not Connected Internally
DU	Don't Use as internally connected

M29W160DT, M29W160DB

Figure 3. TSOP Connections

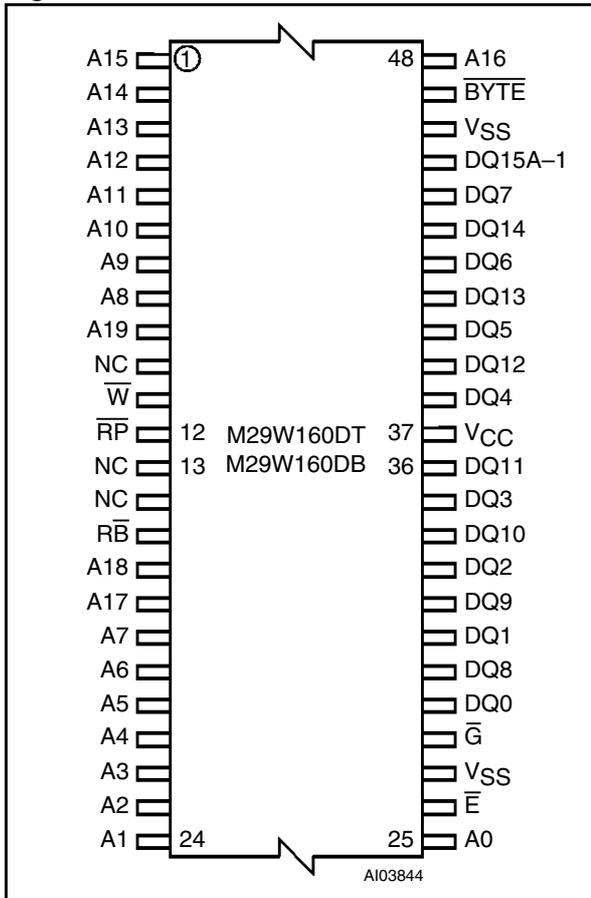
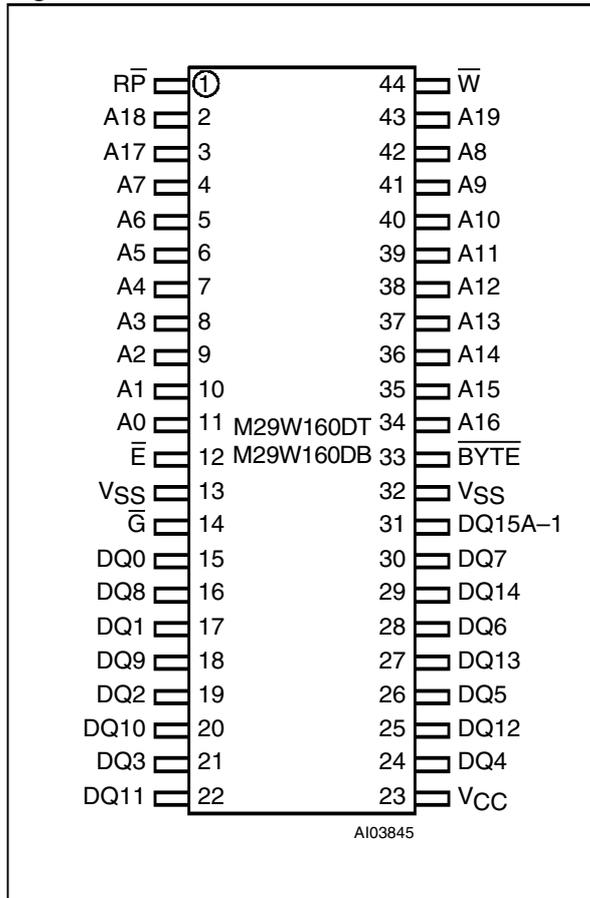


Figure 4. SO Connections



MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

1 FEATURES

1.1 Video input and preprocessing

- Digital YUV input according to "ITU-R BT.656" (8 bits at 27 MHz) and "ITU-R BT.601"
- Support of enhanced "ITU-R BT.656" input format containing decoded VBI data readable via I²C-bus; Closed Caption (CC), Wide Screen Signalling (WSS) and copyright information [Copy Generation Management System (CGMS)]
- Processing of non broadcast video signals from analog VCR according to IEC 756
- Two video clock input pins for switching two digital video sources
- "ITU-R BT.601" format conversion to 1/2D1, 2/3D1 and Standard Interchange Format (SIF)
- 4 : 2 : 2 to 4 : 2 : 0 colour format conversion
- Decimation filtering for all format conversions
- Adaptive median filter and motion compensated filter for input noise reduction.

1.2 Video compression

- Real time MPEG-2 encoding compliant to Main Profile at Main Level (MP@ML) for 625 and 525 interlaced line systems
- Supported resolutions: D1, 2/3D1, 1/2D1 and SIF
- IPB frame, IP frame and I frame only encoding supported at all modes
- Supported bit rates: up to 25 Mbit/s I-only encoding; up to 15 Mbit/s IP-only or IBP encoding.
- Variable video bit rate mode for constant picture quality and constant bit rate mode to gain optimum picture quality from a fixed channel transfer rate
- Access to bit rate control parameters whilst encoding to support external real-time control algorithms (e.g. constrained variable bit rate control)
- Programmable Group Of Pictures (GOP) structure
- Innovative motion estimation with wide search range
- Adaptive quantization
- Motion compensated noise filter.

1.3 Audio input

- Audio inputs: I²S format or EIAJ format (16, 18 or 20 bits), master or slave mode at 32, 44.1 and 48 kHz
- Two digital I²S input ports for selection between two digital audio sources



- Audio clock generation: $256/384 \times f_s$ (48 kHz) locked to video frame rate (if video is present)
- Sample rate conversion to 48 kHz (locked to video frame rate) for slave mode operation in all modes except Digital Versatile Disc (DVD) compliant bypass.

1.4 Audio compression

- Dolby[®](¹) Digital Consumer Encoding (DDCE) also known as AC-3(²) 2 channel audio encoding at 256 kbit/s or 384 kbit/s (only for SAA6752HS/01)
- MPEG-1 layer 2 audio encoding at 256 kbit/s or 384 kbit/s
- Input data bypass for Linear Pulse Code Modulation (LPCM) and compressed audio data [MPEG-1, MPEG-2, Dolby[®] Digital (DD) and Digital Theatre System (DTS)] according to IEC 61937
- Preamble Pc, Preamble Pd and bit stream information captured for identification of modes during bypass of compressed audio data for MPEG-1, MPEG-2, DD and DTS according to IEC 61937
- Audio mute via I²C-bus control for all modes except DVD-compliant bypass.

1.5 Stream multiplexer

- Multiplexing of video and audio streams according to the MPEG-2 systems standard ("ISO 13818-1")
- Generation and output of MPEG-2 Transport Streams (TS), MPEG-2 Program Streams (PS), Packetized Elementary Streams (PES) and Elementary Streams (ES) compliant to the DVD, D-VHS and DVB standards
- MPEG time stamp (PTS/DTS/SCR/PCR) generation and insertion (synchronization)
- Insertion of metadata
- Optional generation of empty time slots for subsequent insertion of application specific data packets
- Optional insertion of user data in the GOP header and in the picture header.

(1) Dolby is a registered trademark of Dolby Laboratories Licensing Corporation.

(2) AC-3 is a registered trademark of Dolby Laboratories Licensing Corporation.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

1.6 Output interface

- Parallel interface 8-bit master/slave output
- 3-state output port
- Glueless interfacing with IEEE 1394 chip sets (for example, PDI 1394 L11)
- Data Expansion Bus Interface (DEBI) interface.

1.7 Control domain

- All control done via I²C-bus
- I²C-bus slave transceiver up to 400 kHz
- I²C-bus slave address select pin
- Host interrupt flag pin.

1.8 Other features

- Single external clock or single crystal 27 MHz
- Separate 27 MHz system clock output
- Interface voltage 3.3 V
- TTL compatible digital outputs
- Power supply voltage 3.3 and 2.5 V
- Boundary Scan Test (BST) supported
- Power-down mode
- Single SDRAM system memory (16 Mbit@16 bit or 64 Mbit@16 bit).

2 GENERAL DESCRIPTION

2.1 General

Philips Semiconductors' second generation real time MPEG-2 encoder, the SAA6752HS, is a highly integrated single chip audio and video encoding solution with very flexible multiplexing functionality. With our expertise in two critical areas for consumer video encoding, noise filtering and motion estimation, we have pushed the boundaries for video quality even further, providing enhanced quality for low bit rates and enabling increased recording times for a given storage capacity. The SAA6752HS will also enable a key driver for new consumer digital recording applications; system cost reduction. By integrating all audio encoding and multiplexing functionality we will be moving from a three chip to a one chip system, with cost efficient design and process technology, thus providing a truly low cost, high quality encoding system.

The SAA6752HS/02 is intended for customers whose application does not require the DDCE function.

The SAA6752HS gives significant advantages to customers developing digital recording applications:

- **Fast time-to-market and low development resources:** By adding a simple external video input processor IC, audio analog-to-digital converter, and an external SDRAM, analog video and audio sources are compressed into high quality MPEG-2 video and MPEG-1 layer 2 or AC-3 audio streams, multiplexed into a single program or transport stream for simple connection to various storage media or broadcast media. Hence, making design effort for our customers a minimum, as well as removing the need for in-depth experience in MPEG encoding.
- **Low system host resources:** All video and audio encoding algorithms and software are run on an internal MIPS®⁽¹⁾ processor. The SAA6752HS only requires small amount of communication from system host processor to set up and control required encoding parameters via I²C-bus.

2.2 Application fields

2.2.1 DVD BASED OPTICAL DISC RECORDERS (DVD+RW, DVD-RW, DVD-RAM)

Emerging optical disc based recording systems target to replace the existing consumer recording (VCR) and playback (DVD and VCD) products. The first generation recordable DVD based products will want to maximise recording times for the 4.7 Gbyte storage capacity. For these systems the SAA6752HS is critical, with its superior noise filtering and motion estimation, in enabling high quality at low bit rates.

Playback compatibility with existing DVD decoding solutions will also be important, which is why the SAA6752HS provides Dolby® digital consumer (AC-3) audio encoding to allow playback through existing players implementing DDCE (AC-3) decoding dominant in current DVD platforms.

The DVD stream is based on MPEG Program Stream (PS). The SAA6752HS directly outputs MPEG PS compliant to the DVD standard.

(1) MIPS is a registered trademark of MIPS Technologies.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

2.2.2 HDD BASED TIME SHIFT RECORDING

Hard Disc Drive (HDD) based time-shift systems enable Personalized TV (PTV) functionality, providing consumers with new powers of control over what and when to watch broadcast content. With the audio and video content recorded digitally, identification, search and retrieval becomes a 'no brainer' task as compared to traditional VCR functionality. Combine this with electronic program guides and intelligent control, and the PTV can also analyse the viewers watching habits to search for programs likely to be of interest and automatically recorded in anticipation of the viewers preferences.

Since HDD recorders are closed systems, the recording format stream can be proprietary. SAA6752HS flexible multiplexing formats, support a number of recording stream formats for HDD including MPEG Transport Stream (TS) or MPEG Packetized Elementary Stream (PES).

2.2.3 DIGITAL VCR (DVHS) RECORDING

A DVHS player records streams based on MPEG Transport Streams (TS) packed in logical tape tracks. The SAA6752HS output streams are compliant with DVHS standard requirements.

2.2.4 VIDEO EDITING/TRANSMISSION/SURVEILLANCE/ CONFERENCING

The SAA6752HS can operate as a stand-alone device in all above applications. The SAA6752HS' full features and flexibility allows customers to tailor functionality and performance to specific application requirements. All required control settings such as GOP size and bit rate modes can be selected via I²C-bus.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DDP}	digital supply voltage (pad cells)	3.0	3.3	3.6	V
V _{DDCO}	digital supply voltage (core)	2.3	2.5	2.7	V
V _{DDA}	analog supply voltage (oscillator and PLL)	2.3	2.5	2.7	V
I _{DD(tot)}	analog + digital supply current	407	453	525	mA
P _{tot}	total power dissipation	1.2	1.4	1.9	W
f _{DCXO}	quartz frequency (digital controlled tuning)	27 × (1 – 200 × 10 ⁻⁶)	27	27 × (1 + 200 × 10 ⁻⁶)	MHz
f _{SDRAM}	SDRAM clock frequency	–	108	–	MHz
f _{SCL}	I ² C-bus input clock frequency	100	–	400	kHz
B	output bit-rate	1.5	–	25	Mbit/s
V _{IH}	HIGH-level digital input voltage	1.7	–	3.6	V
V _{IL}	LOW-level digital input voltage	–0.5	–	+0.7	V
V _{OH}	HIGH-level digital output voltage	V _{DDP} – 0.4	–	V _{DDP}	V
V _{OL}	LOW-level digital output voltage	0	–	0.4	V
T _{amb}	ambient temperature	0	–	70	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA6752HS/01 ⁽¹⁾	SQFP208	plastic shrink quad ?at package; 208 leads (lead length 1.3 mm); body 28 × 28 × 3.4 mm; high stand-off height	SOT316-1
SAA6752HS/02 ⁽²⁾			

Notes

1. MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer.
2. MPEG-2 video and MPEG-audio encoder with multiplexer, but without AC-3 audio encoder.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

5 BLOCK DIAGRAM

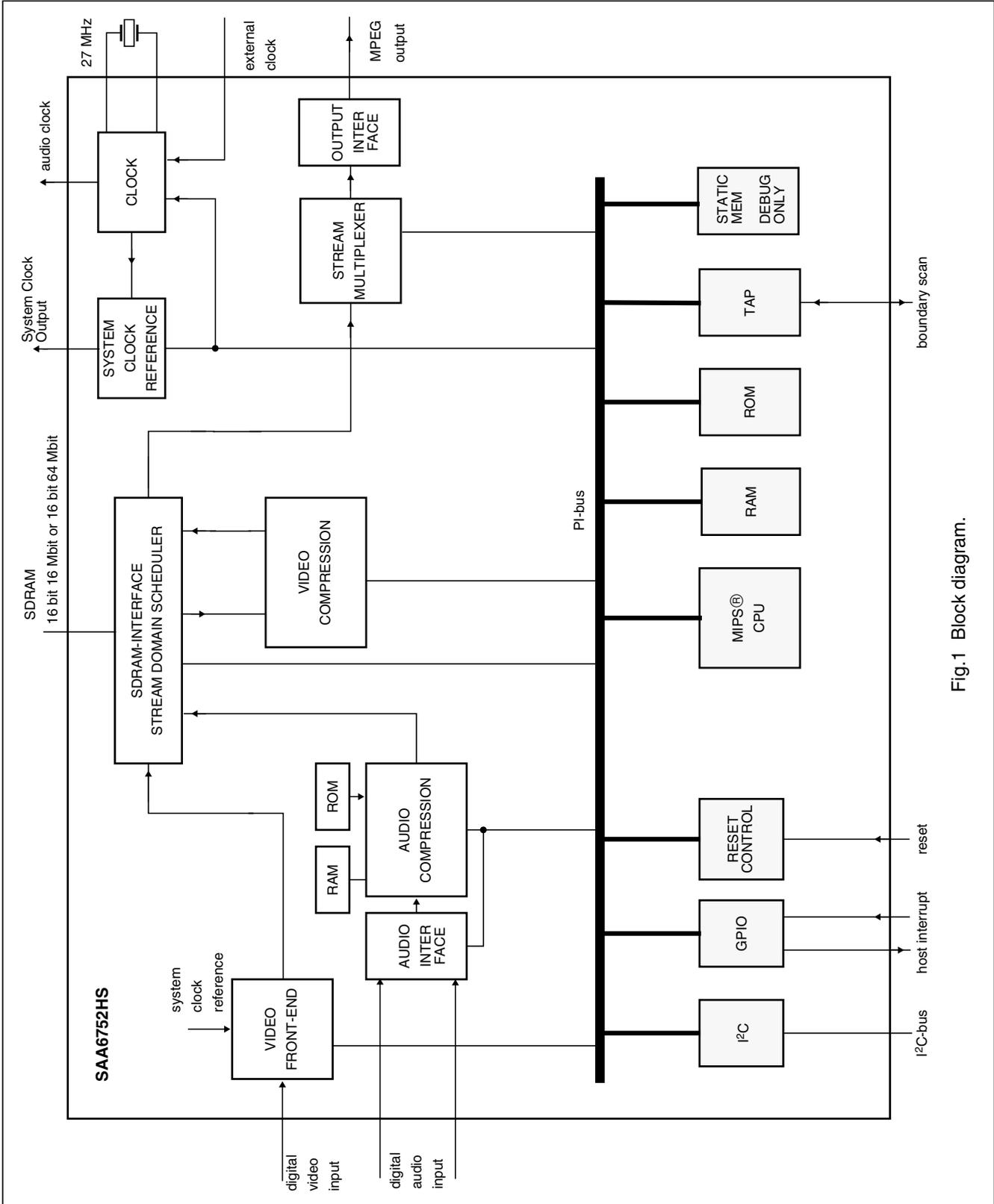


Fig.1 Block diagram.

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

6 PINNING

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
V _{SSP}	1	ground	–	pad ground
SDATA1	2	input	–	I ² S-bus serial data input port 1 with internal pull-down resistor
SCLK1	3	input/output	4	I ² S-bus serial clock port 1 with internal pull-down resistor
SWS1	4	input/output	4	I ² S-bus word select port 1 with internal pull-down resistor
V _{DDP}	5	supply	–	pad ring supply voltage (3.3 V)
SDATA2	6	input/output	4	I ² S-bus serial data port 2 with internal pull-down resistor
SCLK2	7	input/output	4	I ² S-bus serial clock port 2 with internal pull-down resistor
SWS2	8	input/output	4	I ² S-bus word select port 2 with internal pull-down resistor
ACLK	9	output	4	audio clock output (256 × f _s or 384 × f _s)
V _{SSP}	10	ground	–	pad ground
IDQ	11	input	–	reserved (recommended connect to pin V _{SSP}) with internal pull-down resistor
YUV0	12	input	–	video input signal bit 0 (LSB)
YUV1	13	input	–	video input signal bit 1
YUV2	14	input	–	video input signal bit 2
YUV3	15	input	–	video input signal bit 3
YUV4	16	input	–	video input signal bit 4
YUV5	17	input	–	video input signal bit 5
YUV6	18	input	–	video input signal bit 6
YUV7	19	input	–	video input signal bit 7 (MSB)
V _{SSP}	20	ground	–	pad ground
HSYNC	21	input	–	horizontal sync input (video) with internal pull-down resistor
VSYNC	22	input	–	vertical sync input (video) with internal pull-down resistor
FID	23	input	–	video field identification input (odd/even field) with internal pull-down resistor
VCLK1	24	input	–	video clock input 1 (27 MHz) with internal pull-down resistor
V _{SSCO}	25	ground	–	core ground
V _{SSCO}	26	ground	–	core ground
V _{DDCO}	27	supply	–	core supply voltage (2.5 V)
V _{DDCO}	28	supply	–	core supply voltage (2.5 V)
V _{DDP}	29	supply	–	pad ring supply voltage (3.3 V)
VCLK2	30	input	–	video clock input 2 (27 MHz) with internal pull-down resistor
PDOAV	31	3-state output	4	parallel stream data output for audio/video identifier
PDIDS	32	input	–	parallel stream data input for data strobe (request for packet in Data Expansion Bus Interface (DEBI) slave mode) with internal pull-up resistor
PDOSYNC	33	3-state output	4	parallel stream data output for packet sync
V _{SSP}	34	ground	–	pad ground
PDOVAL	35	3-state output	4	parallel stream data valid output with internal pull-up resistor
PDO0	36	3-state output	4	parallel stream data output bit 0 (LSB)

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
PDO1	37	3-state output	4	parallel stream data output bit 1
PDO2	38	3-state output	4	parallel stream data output bit 2
V _{DDP}	39	supply	–	pad ring supply voltage (3.3 V)
PDO3	40	3-state output	4	parallel stream data output bit 3
PDO4	41	3-state output	4	parallel stream data output bit 4
PDO5	42	3-state output	4	parallel stream data output bit 5
PDO6	43	3-state output	4	parallel stream data output bit 6
V _{SSP}	44	ground	–	pad ground
PDO7	45	3-state output	4	parallel stream data output bit 7 (MSB)
PDIOCLK	46	input/output	4	parallel stream clock input/output
I2CADDRSEL	47	input	–	I ² C-bus address select input with internal pull-up resistor
SD_DQ15	48	input/output	8	SDRAM data input/output bit 15 (MSB)
V _{DDP}	49	supply	–	pad ring supply voltage (3.3 V)
SD_DQ0	50	input/output	8	SDRAM data input/output bit 0 (LSB)
SD_DQ14	51	input/output	8	SDRAM data input/output bit 14
SD_DQ1	52	input/output	8	SDRAM data input/output bit 1
V _{SSP}	53	ground	–	pad ground
SD_DQ13	54	input/output	8	SDRAM data input/output bit 13
SD_DQ2	55	input/output	8	SDRAM data input/output bit 2
SD_DQ12	56	input/output	8	SDRAM data input/output bit 12
V _{DDP}	57	supply	–	pad ring supply voltage (3.3 V)
SD_DQ3	58	input/output	8	SDRAM data input/output bit 3
SD_DQ11	59	input/output	8	SDRAM data input/output bit 11
SD_DQ4	60	input/output	8	SDRAM data input/output bit 4
SD_DQ10	61	input/output	8	SDRAM data input/output bit 10
V _{SSP}	62	ground	–	pad ground
SD_DQ5	63	input/output	8	SDRAM data input/output bit 5
SD_DQ9	64	input/output	8	SDRAM data input/output bit 9
SD_DQ6	65	input/output	8	SDRAM data input/output bit 6
SD_DQ8	66	input/output	8	SDRAM data input/output bit 8
V _{DDP}	67	supply	–	pad ring supply voltage (3.3 V)
SD_DQ7	68	input/output	8	SDRAM data input/output bit 7
SD_DQM1	69	output	8	SDRAM data mask enable output bit 1
SD_DQM0	70	output	8	SDRAM data mask enable output bit 0 (LSB)
SD_WE	71	output	8	SDRAM write enable output (active LOW)
V _{SSP}	72	ground	–	pad ground
SD_CAS	73	output	8	SDRAM column address strobe output (active LOW)
SD_CLK	74	output	8	SDRAM clock output
SD_RAS	75	output	8	SDRAM row address strobe output (active LOW)
SD_CKE	76	output	8	SDRAM clock enable output

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
V _{SSCO}	77	ground	–	core ground
V _{SSCO}	78	ground	–	core and substrate ground
V _{DDCO}	79	supply	–	core supply voltage (2.5 V)
V _{DDCO}	80	supply	–	core supply voltage (2.5 V)
V _{DDP}	81	supply	–	pad ring supply voltage (3.3 V)
SD_CS	82	output	8	SDRAM chip select output (active LOW)
SD_A13	83	output	8	SDRAM address output bit 13 (bank selection for 64 Mbit)
SD_A9	84	output	8	SDRAM address output bit 9
SD_A8	85	output	8	SDRAM address output bit 8
V _{SSP}	86	ground	–	pad ground
SD_A11	87	output	8	SDRAM address output bit 11 (bank selection for 16 Mbit)
SD_A7	88	output	8	SDRAM address output bit 7
SD_A12	89	output	8	SDRAM address output bit 12 (bank selection for 64 Mbit)
SD_A6	90	output	8	SDRAM address output bit 6
V _{DDP}	91	supply	–	pad ring supply voltage (3.3 V)
SD_A10	92	output	8	SDRAM address output bit 10
SD_A5	93	output	8	SDRAM address output bit 5
SD_A0	94	output	8	SDRAM address output bit 0 (LSB)
SD_A4	95	output	8	SDRAM address output bit 4
V _{SSP}	96	ground	–	pad ground
SD_A1	97	output	8	SDRAM address output bit 1
SD_A3	98	output	8	SDRAM address output bit 3
SD_A2	99	output	8	SDRAM address output bit 2
SD_DQM3	100	output	8	reserved (do not connect)
V _{DDP}	101	supply	–	pad ring supply voltage (3.3 V)
SD_DQM2	102	output	8	reserved (do not connect)
SD_DQ31	103	input/output	8	reserved (do not connect)
SD_DQ16	104	input/output	8	reserved (do not connect)
V _{SSP}	105	ground	–	pad ground
SD_DQ30	106	input/output	8	reserved (do not connect)
SD_DQ17	107	input/output	8	reserved (do not connect)
SD_DQ29	108	input/output	8	reserved (do not connect)
V _{DDP}	109	supply	–	pad ring supply voltage (3.3 V)
SD_DQ18	110	input/output	8	reserved (do not connect)
SD_DQ28	111	input/output	8	reserved (do not connect)
SD_DQ19	112	input/output	8	reserved (do not connect)
SD_DQ27	113	input/output	8	reserved (do not connect)
V _{SSP}	114	ground	–	pad ground
SD_DQ20	115	input/output	8	reserved (do not connect)
SD_DQ26	116	input/output	8	reserved (do not connect)

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
V _{SSCO}	77	ground	–	core ground
V _{SSCO}	78	ground	–	core and substrate ground
V _{DDCO}	79	supply	–	core supply voltage (2.5 V)
V _{DDCO}	80	supply	–	core supply voltage (2.5 V)
V _{DDP}	81	supply	–	pad ring supply voltage (3.3 V)
SD_CS	82	output	8	SDRAM chip select output (active LOW)
SD_A13	83	output	8	SDRAM address output bit 13 (bank selection for 64 Mbit)
SD_A9	84	output	8	SDRAM address output bit 9
SD_A8	85	output	8	SDRAM address output bit 8
V _{SSP}	86	ground	–	pad ground
SD_A11	87	output	8	SDRAM address output bit 11 (bank selection for 16 Mbit)
SD_A7	88	output	8	SDRAM address output bit 7
SD_A12	89	output	8	SDRAM address output bit 12 (bank selection for 64 Mbit)
SD_A6	90	output	8	SDRAM address output bit 6
V _{DDP}	91	supply	–	pad ring supply voltage (3.3 V)
SD_A10	92	output	8	SDRAM address output bit 10
SD_A5	93	output	8	SDRAM address output bit 5
SD_A0	94	output	8	SDRAM address output bit 0 (LSB)
SD_A4	95	output	8	SDRAM address output bit 4
V _{SSP}	96	ground	–	pad ground
SD_A1	97	output	8	SDRAM address output bit 1
SD_A3	98	output	8	SDRAM address output bit 3
SD_A2	99	output	8	SDRAM address output bit 2
SD_DQM3	100	output	8	reserved (do not connect)
V _{DDP}	101	supply	–	pad ring supply voltage (3.3 V)
SD_DQM2	102	output	8	reserved (do not connect)
SD_DQ31	103	input/output	8	reserved (do not connect)
SD_DQ16	104	input/output	8	reserved (do not connect)
V _{SSP}	105	ground	–	pad ground
SD_DQ30	106	input/output	8	reserved (do not connect)
SD_DQ17	107	input/output	8	reserved (do not connect)
SD_DQ29	108	input/output	8	reserved (do not connect)
V _{DDP}	109	supply	–	pad ring supply voltage (3.3 V)
SD_DQ18	110	input/output	8	reserved (do not connect)
SD_DQ28	111	input/output	8	reserved (do not connect)
SD_DQ19	112	input/output	8	reserved (do not connect)
SD_DQ27	113	input/output	8	reserved (do not connect)
V _{SSP}	114	ground	–	pad ground
SD_DQ20	115	input/output	8	reserved (do not connect)
SD_DQ26	116	input/output	8	reserved (do not connect)

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
SD_DQ21	117	input/output	8	reserved (do not connect)
SD_DQ25	118	input/output	8	reserved (do not connect)
V _{DDP}	119	supply	–	pad ring supply voltage (3.3 V)
SD_DQ22	120	input/output	8	reserved (do not connect)
SD_DQ24	121	input/output	8	reserved (do not connect)
SD_DQ23	122	input/output	8	reserved (do not connect)
EXTCLK	123	input	–	27 MHz external clock input with internal pull-up resistor
V _{SSP}	124	ground	–	pad ground
V _{SSA}	125	ground	–	oscillator analog ground
XTALI	126	analog input	–	crystal oscillator input (27 MHz); note 2
XTALO	127	analog output	–	crystal oscillator output (27 MHz)
V _{DDA}	128	supply	–	oscillator analog supply voltage (2.5 V)
V _{SSCO}	129	ground	–	core ground
V _{SSCO}	130	ground	–	core ground
V _{DDCO}	131	supply	–	core supply voltage (2.5 V)
V _{DDCO}	132	supply	–	core supply voltage (2.5 V)
V _{DDP}	133	supply	–	pad ring supply voltage (3.3 V)
TDI	134	input	–	boundary scan test data input; pin must float or set to HIGH during normal operating; with internal pull-up resistor; note 3
TMS	135	input	–	boundary scan test mode select; pin must float or set to HIGH during normal operating; with internal pull-up resistor; note 3
TCK	136	input	–	boundary scan test clock; pin must be set to LOW during normal operating; with internal pull-up resistor; note 3
TDO	137	3-state output	4	boundary scan test data output; pin not active during normal operating; with 3-state output; note 3
V _{SSP}	138	ground	–	pad ground
TRST	139	input	–	test reset input (active LOW), for boundary scan test (with internal pull-up); notes 3 and 4
CLKOUT	140	output	4	27 MHz system clock output
TEST0	141	input/output	4	reserved (do not connect)
TEST1	142	input/output	4	reserved (do not connect)
V _{DDP}	143	supply	–	pad ring supply voltage (3.3 V)
TEST2	144	input/output	4	reserved (do not connect)
SDA	145	input/open-drain output	–	serial data input/output (I ² C-bus)
SCL	146	input/open-drain output	–	serial clock input/output (I ² C-bus)
RESET	147	input	–	reset input (active LOW); with internal pull-up resistor
V _{SSP}	148	ground	–	pad ground
RTS	149	output	4	reserved (do not connect); Universal Asynchronous Receiver/Transmitter (UART) request to send output (active LOW)

MPEG-2 video and MPEG-audio/AC-3 audio encoder with multiplexer

SAA6752HS

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
CTS	150	input	–	reserved (recommended connect to pin V _{DDP}); UART clear to send input; external static memory select input (active LOW); with internal pull-up resistor
RXD	151	input	–	reserved (recommended connect to pin V _{DDP}); UART receive data; internal boot select input; with internal pull-up resistor
TXD	152	output	4	reserved (do not connect); UART transmit data
V _{DDP}	153	supply	–	pad ring supply voltage (3.3 V)
SM_LB	154	input/output	4	reserved (do not connect)
SM_UB	155	input/output	4	reserved (do not connect)
H_IRF	156	3-state output	4	host interrupt ?ag output; with internal pull-up resistor
V _{SSP}	157	ground	–	pad ground
SM_OE	158	output	4	reserved (do not connect), static memory output enable output (active LOW)
SM_A9	159	output	4	reserved (do not connect), static memory address output bit 9
SM_A10	160	output	4	reserved (do not connect), static memory address output bit 10
V _{DDP}	161	supply	–	pad ring supply voltage (3.3 V)
SM_A8	162	output	4	reserved (do not connect), static memory address output bit 8
SM_A11	163	output	4	reserved (do not connect), static memory address output bit 11
SM_A7	164	output	4	reserved (do not connect), static memory address output bit 7
SM_A12	165	output	4	reserved (do not connect), static memory address output bit 12
V _{SSP}	166	ground	–	pad ground
SM_A6	167	output	4	reserved (do not connect), static memory address output bit 6
SM_A13	168	output	4	reserved (do not connect), static memory address output bit 13
SM_A5	169	output	4	reserved (do not connect), static memory address output bit 5
SM_A14	170	output	4	reserved (do not connect), static memory address output bit 14
V _{DDP}	171	supply	–	pad ring supply voltage (3.3 V)
SM_WE	172	output	4	reserved (do not connect), static memory write enable output (active LOW)
SM_D7	173	input/output	4	reserved (do not connect), static memory data input/output bit 7 with internal pull-down resistor
SM_D8	174	input/output	4	reserved (do not connect), static memory data input/output bit 8 with internal pull-down resistor
SM_D6	175	input/output	4	reserved (do not connect), static memory data input/output bit 6 with internal pull-down resistor
V _{SSP}	176	ground	–	pad ground
SM_D9	177	input/output	4	reserved (do not connect), static memory data input/output bit 9 with internal pull-down resistor
SM_D5	178	input/output	4	reserved (do not connect), static memory data input/output bit 5 with internal pull-down resistor
SM_D10	179	input/output	4	reserved (do not connect), static memory data input/output bit 10 with internal pull-down resistor

MPEG-2 video and MPEG-audio/AC-3 audio
encoder with multiplexer

SAA6752HS

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
SM_D4	180	input/output	4	reserved (do not connect), static memory data input/output bit 4 with internal pull-down resistor
V _{SSCO}	181	ground	–	internal pre-driver and substrate ground
V _{SSCO}	182	ground	–	core ground
V _{DDCO}	183	supply	–	core supply voltage (2.5 V)
V _{DDCO}	184	supply	–	internal pre-driver supply voltage (2.5 V)
V _{DDP}	185	supply	–	pad ring supply voltage (3.3 V)
SM_D11	186	input/output	4	reserved (do not connect), static memory data input/output bit 11 with internal pull-down resistor
SM_D3	187	input/output	4	reserved (do not connect), static memory data input/output bit 3 with internal pull-down resistor
SM_D12	188	input/output	4	reserved (do not connect), static memory data input/output bit 12 with internal pull-down resistor
SM_D2	189	input/output	4	reserved (do not connect), static memory data input/output bit 2 with internal pull-down resistor
V _{SSP}	190	ground	–	pad ground
SM_D13	191	input/output	4	reserved (do not connect), static memory data input/output bit 13 with internal pull-down resistor
SM_D1	192	input/output	4	reserved (do not connect), static memory data input/output bit 1 with internal pull-down resistor
SM_D14	193	input/output	4	reserved (do not connect), static memory data input/output bit 14 with internal pull-down resistor
SM_D0	194	input/output	4	reserved (do not connect), static memory data input/output bit 0 (LSB) with internal pull-down resistor
V _{DDP}	195	supply	–	pad ring supply voltage (3.3 V)
SM_D15	196	input/output	4	reserved (do not connect), static memory data input/output bit 15 (MSB) with internal pull-down resistor
SM_CS3	197	output	4	reserved (do not connect), static memory chip select output for external ROM or RAM (active LOW)
SM_A4	198	output	4	reserved (do not connect), static memory address output bit 4
SM_A3	199	output	4	reserved (do not connect), static memory address output bit 3
V _{SSP}	200	ground	–	pad ground
SM_A2	201	output	4	reserved (do not connect), static memory address output bit 2
SM_A15	202	output	4	reserved (do not connect), static memory address output bit 15
SM_A1	203	output	4	reserved (do not connect), static memory address output bit 1
SM_A16	204	output	4	reserved (do not connect), static memory address output bit 16
V _{DDP}	205	supply	–	pad ring supply voltage (3.3 V)
SM_A0	206	output	4	reserved (do not connect), static memory address output bit 0 (LSB)
SM_A17	207	output	4	reserved (do not connect), static memory address output bit 17 (MSB)
SM_CS0	208	output	4	reserved (do not connect)

**MPEG-2 video and MPEG-audio/AC-3 audio
encoder with multiplexer**

SAA6752HS**Notes**

1. All input pins, input/output pins (in input mode), output pins (in 3-state mode) and open-drain output pins are limited to 3.3 V.
2. If used with external clock source the input voltage has to be limited to 2.5 V.
3. In accordance with the "IEEE 1149.1" standard.
4. Special function of pin $\overline{\text{TRST}}$:
 - a) For board designs without boundary scan implementation, pin $\overline{\text{TRST}}$ must be connected to ground.
 - b) Pin $\overline{\text{TRST}}$ provides easy initialization of the internal BST circuit. By applying a LOW it can be used to force the internal Test Access Port (TAP) controller to the Test-Logic-Reset state (normal operating) at once.

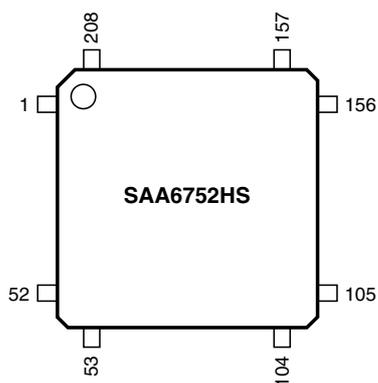


Fig.2 Pin configuration.

9.8.7 IC7500: SAA7118 (VIP)

**PAL/NTSC/SECAM Video Decoder with Adaptive Comb Filter,
Component Video Input, VBI-Data Slicer and High Performance Scaler**

SAA7118**1 FEATURES**

The SAA7118 is a video capture device for application at the image port of VGA controller, with following feature high lights:

Video Acquisition/ Clock

Up to sixteen analog CVBS, split as desired (All of the CVBS inputs optionally can be used to convert VSB signals)

Up to eight analog Y+C inputs, split as desired

Up to four analog component inputs, with embedded or separate sync, split as desired

Four on-chip anti-aliasing filters in front of the ADC's Automatic Clamp Control (ACC) for CVBS, Y and C (or VSB) and component signal

Switchable white Peak Control

Four 9 Bit Low Noise CMOS analog-to-digital converters at two-fold ITU-656 oversampling (27 MHz)

Digitized CVBS or Y+C-signals are available on the expansion port

Fully programmable static gain or automatic gain control, matching to the particular signal properties

On-Chip Line Locked Clock Generation according ITU601

Requires only one crystal (32.11 or 24.576 MHz) for all standards

Horizontal and vertical Sync Detection

Video Decoder

Digital PLL for Synchronization and Clock Generation from all Standards and Non- Standard Video Sources e.g. consumer grade VTR

Digital PLL for Synchronization and Clock Generation from all Standards and Non- Standard Video Sources e.g. consumer grade VTR

Automatic detection of any supported colour standard

Luminance and chrominance signal processing for PAL BGDHIN, Combination-PAL N, PAL M, NTSC M, NTSC-Japan, NTSC 4.43 and SECAM

Adaptive 2/4-line comb filter for two dimensional chrominance/luminance-separation, also with VTR signals

- Increased Luminance and Chrominance Bandwidth for all PAL and NTSC-standards
 - Reduced cross colour and cross luminance artefacts
- PAL delay line for correcting PAL phase errors

Brightness Contrast Saturation (BCS)- adjustment, separately for composite and baseband signals

User programmable sharpness control

Fast Blanking between component inputs and a CVBS input through a dedicated pin

Detection of copy-protected signals acc. to the Macrovision standard, indicating level of protection

Independent Gain and Offset - adjustment for raw data path

Component Video Processing

Synchronous Component Video (RGB) input via fast blanking, YCbCr input

Digital matrix

Video Scaler

Horizontal and Vertical Down-Scaling and Up-Scaling to randomly sized windows

Horizontal and Vertical Scaling range: variable zoom to 1/64 (icon)

(Note: H and V zoom are restricted by the transfer data rates)

Anti-Alias- and Accumulating Filter for Horizontal Scaling

Vertical Scaling with Linear Phase Interpolation and Accumulating Filter for Anti-Aliasing (6 bit phase accuracy)

Horizontal Phase Correct Up- and Down-Scaling for improved signal quality of scaled data, especially for compression and video phone applications, with 6 bit phase accuracy (1.2 nsec step width)

Two independent programming sets for scaler part, to define two "ranges" per field or sequences over frames

Fieldwise switching between Decoder-part and Expansion port (X-port) input

Brightness, contrast and saturation controls for scaled outputs

VBI-Data Decoder and Slicer

versatile VBI-data decoder, slicer, clock regeneration and byte synchronization

e.g. for WST, NABST, Close Caption, WSS, etc.

Audio Clock Generation

Generation of a field locked Audio Master Clock to support a constant number of audio clocks per video field

PAL/NTSC/SECAM Video Decoder with Adaptive Comb Filter, Component Video Input, VBI-Data Slicer and High Performance Scaler

SAA7118

Generation of an audio serial and left/right (channel) clock signal

Digital I/O Interfaces

Real Time signal port (R - port), incl. continuous line locked reference clock and real time status information supporting RTC level 3.1 (refer to external document "RTC Functional Specification" for details)

Bidirectional Expansion Port (X - port) with half duplex functionality (D1), 8-bit YCbCr

- output from Decoder part, real time and unscaled, or
- input to Scaler part, e.g. video from MPEG-decoder (extension to 16 bit possible)

Video Image port (I - port) configurable for 8 - bit data (extension to 16 bit possible) in Master Mode (own clock), or Slave Mode (external clock), with auxiliary timing and hand shake signals

Discontinuous data streams supported

32-word * 4 Byte FIFO register for video output data

28-word * 4 Byte FIFO register for decoded VBI output data

Scaled 4:2:2, 4:1:1, 4:2:0, 4:1:0 YCbCr output

Scaled 8-bit luminance only and raw CVBS data output sliced, decoded VBI data output

Miscellaneous

Power On Control

5 V tolerant digital inputs and I/O ports

Software controlled power saving stand-by modes supported

Programming via serial I²C-bus, full read-back ability by an external controller, bit rate up to 400 kbit/s

Boundary Scan Test circuit complies to the IEEE Std. 1149.b1 -1994

BGA156 package

2 APPLICATIONS

Multimedia

Digital Television

Image Processing

Video Phone

PC- Editing cards

PC- Tuner cards

3 GENERAL DESCRIPTION

Philips X-VIP is a new Multistandard Comb Filter Video Decoder chip with additional component processing, providing high quality, optionally scaled, video.

The SAA7118 is a combination of a four channel analog preprocessing circuit including source selection, anti-aliasing filter and A/D-converter, an automatic clamp and gain control, a Clock Generation Circuit (CGC), a Digital Multi Standard Decoder containing two-dimensional chrominance/luminance separation by an adaptive comb filter and a high performance scaler, including variable horizontal and vertical up and down scaling and a Brightness- Contrast- Saturation- Control circuit.

It is a highly integrated circuit for Desktop Video and similar applications. The decoder is based on the principle of line-locked clock decoding and is able to decode the colour of PAL, SECAM and NTSC signals into ITU-601 compatible colour component values. The SAA7118 accepts as analog inputs CVBS or S-Video (Y+C) from TV or VCR sources, including weak and distorted signals, as well as baseband component signals YCbCr or RGB. An expansion port (X-port) for digital video (bi-directional half duplex, D1 compatible) is also supported to connect to MPEG or video phone codec. At the so called image port (I-port) the 7118 supports 8 (16) bit wide output data with auxiliary reference data for interfacing to VGA controllers.

The target application for SAA7118 is to capture and optionally scale video images, to be provided as digital video stream through the image port of a VGA controller, for capture to system memory, or just to provide digital baseband video to any picture improvement processing.

SAA7118 also provides means for capturing the serially coded data in the vertical blanking interval (VBI-data). Two principal functions are available:

- to capture raw video samples, after interpolation to the required output data rate, via the scaler and
- a versatile data slicer (data recovery) unit.

SAA7118 incorporates also a field locked audio clock generation. This function ensures that there is always the same number of audio samples associated with a field, or a set of fields. This prevents the loss of synchronization between video and audio, during capture or playback.

All of the A/D- converters may be used to digitize a VSB signal for further for further decoding; a dedicated output port and a selectable VSB clock input is provided.

The circuit is controlled via I²C-bus (full write / read capability for all programming registers, bit rate up to 400 kbits/s)

PAL/NTSC/SECAM Video Decoder with Adaptive Comb Filter,
Component Video Input, VBI-Data Slicer and High Performance Scaler

SAA7118

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DDx}	digital supply voltage	3.0	3.3	3.6	V
V_{DDCx}	digital core supply voltage	3.0	3.3	3.6	V
V_{DDA}	analog supply voltage	3.1	3.3	3.5	V
T_{amb}	ambient temperature	0	-	70	°C
P_{A+D}	analog and digital power dissipation ⁽¹⁾	-	t.b.d.	-	W

Note

- Power consumption is measured in CVBS-input mode (only one ADC active) and 8 bit image port output mode, expansion port is tristated

5 ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7118	156	BGA156	Plastic	SOT 472-1(BB3)

PAL/NTSC/SECAM Video Decoder with Adaptive Comb Filter,
Component Video Input, VBI-Data Slicer and High Performance Scaler

SAA7118

6 SYSTEM BLOCK DIAGRAM

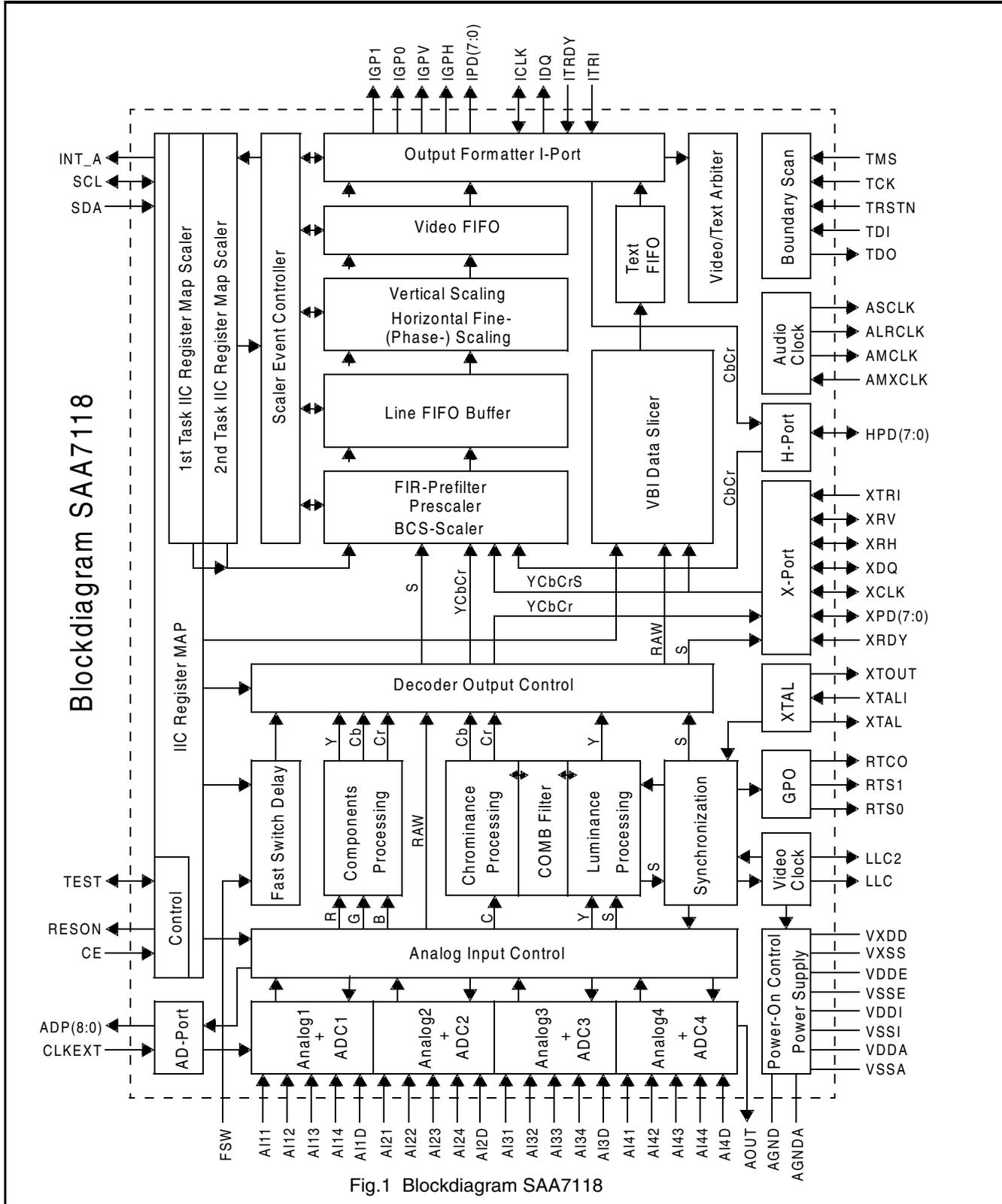
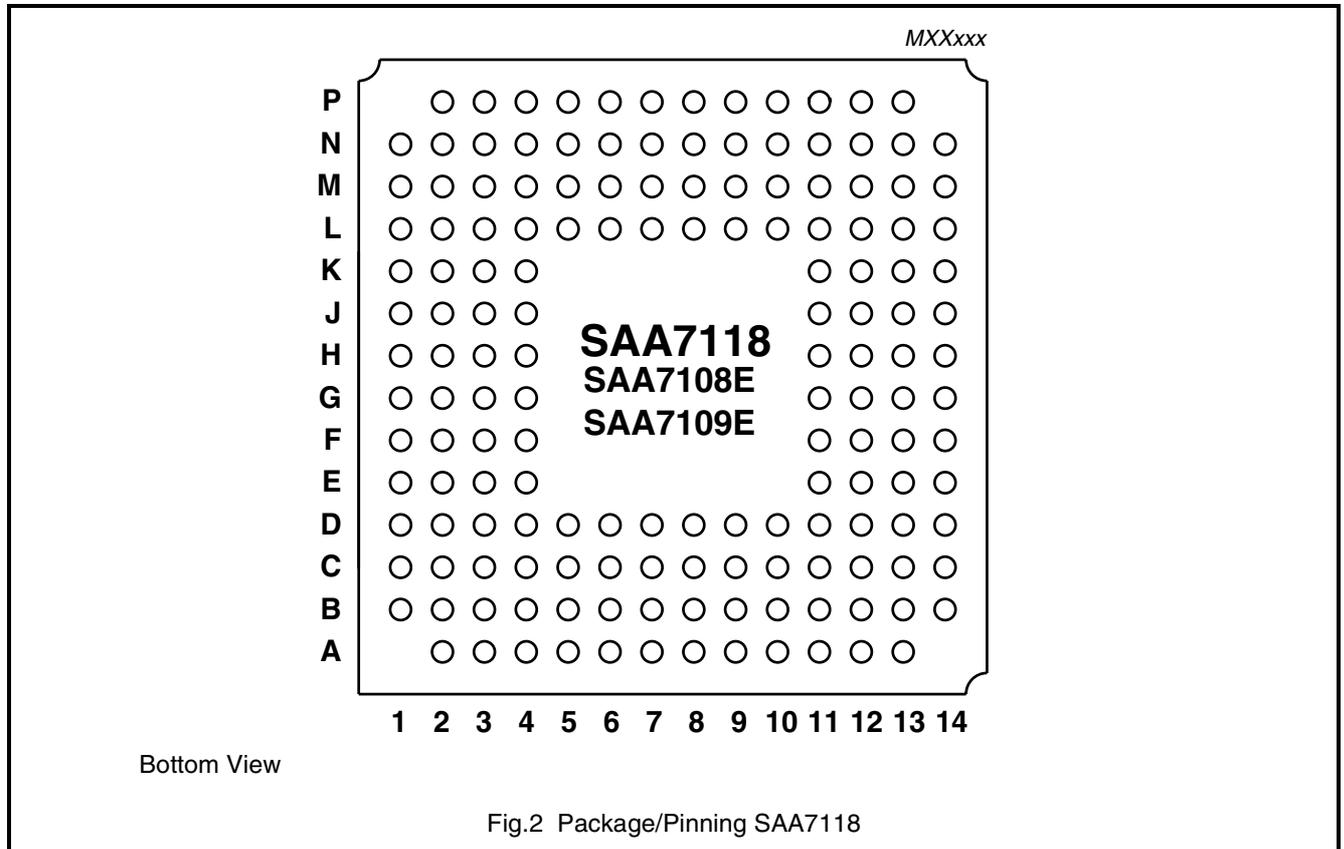


Fig.1 Blockdiagram SAA7118

PAL/NTSC/SECAM Video Decoder with Adaptive Comb Filter,
Component Video Input, VBI-Data Slicer and High Performance Scaler

SAA7118

7 PINNING AND CONFIGURATION



7.1 Pinning List

Table 1 Pinning List SAA7118

PIN	NAME	TYPE	DESCRIPTION
A02	XTOUT	O	Crystal oscillator output signal
A03	XTAL	O	Connect output pin for quartz
A04	VXSS	P	Ground for crystal oscillator
A05	TDO	O	Test Data Output for Boundary Scan Test (2)
A06	XRDY	O	Status flag or ready signal from scaler
A07	XCLK	I/O	Clock I/O expansion port
A08	XPD0	I/O	LSB of expansion port bus
A09	XPD2	I/O	MSB-5 of expansion port bus
A10	XPD4	I/O	MSB-3 of expansion port bus
A11	XPD6	I/O	MSB-1 of expansion port bus
A12	TEST5	I/pu	Scan test input; do not connect
A13	TEST3	I/pu	Scan test input; do not connect
B01	AI41	I	Analog input #41
B02	RES1	O	Reserved pin for future extensions or testing, do not connect
B03	VXDD	P	Supply for crystal oscillator

PAL/NTSC/SECAM Video Decoder with Adaptive Comb Filter,
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SAA7118

PIN	NAME	TYPE	DESCRIPTION
B04	XTALI	I	Connect input pin for quartz
B05	TDI	I/pu	Test Data Input for Boundary Scan Test (with internal pull-up) (2)
B06	TCK	I/pu	Test Clock for Boundary Scan Test (with internal pull-up) (2)
B07	XDQ	I/O	Data qualifier for expansion port
B08	XPD1	I/O	MSB-6 of expansion port bus
B09	XPD3	I/O	MSB-4 of expansion port bus
B10	XPD5	I/O	MSB-2 of expansion port bus
B11	XTRI	I	X-port output control signal; effects (XPD[7:0], XRH, XRV, XDQ and XCLK)
B12	TEST4	O	Scan test output; do not connect
B13	RES2	NC	Reserved pin for future extensions or testing, do not connect
B14	RES3	NC	Reserved pin for future extensions or testing, do not connect
C01	VSSA4	P	Ground for analog input AI4x
C02	AGND	P	Analog Signal Ground
C03	RES4	NC	Reserved pin for future extensions or testing, do not connect
C04	RES5	NC	Reserved pin for future extensions or testing, do not connect
C05	VDDE1	P	Digital supply peripheral cells
C06	TRSTN	I/pu	Test ReSeT Not for Boundary Scan Test (with internal pull-up) (1)
C07	XRH	I/O	Horizontal reference expansion-port
C08	VDDI1	P	Digital supply core
C09	VDDE2	P	Digital supply peripheral cells
C10	VDDI2	P	Digital supply core
C11	XPD7	I/O	MSB of expansion port bus
C12	RES6	NC	Reserved pin for future extensions or testing, do not connect
C13	RES7	NC	Reserved pin for future extensions or testing, do not connect
C14	TEST2	I/pu	Scan test input; do not connect
D01	AI43	I	Analog input #43
D02	AI42	I	Analog input #42
D03	AI4D	I/O	Differential input for AI4x
D04	VDDA4	P	Supply for analog input AI4x
D05	VSSE1	P	Digital ground peripheral cells
D06	TMS	I/pu	Test Mode Select for Boundary Scan Test or Scan Test (with internal pull-up) (2)
D07	VSSI1	P	Digital ground core (Substrate connection)
D08	XRV	I/O	Vertical reference for expansion-port
D09	VSSE2	P	Digital ground peripheral cells
D10	VSSI2	P	Digital ground core
D11	VSSE3	P	Digital ground peripheral cells
D12	VDDE3	P	Digital supply peripheral cells
D13	TEST1	I/pu	Scan test input; do not connect
D14	HPD0	I/O	LSB of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port
E01	AI44	I	Analog input #44

PAL/NTSC/SECAM Video Decoder with Adaptive Comb Filter,
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SAA7118

PIN	NAME	TYPE	DESCRIPTION
E02	VDDA4A	P	Supply for analog input AI4x
E03	AI31	I	Analog input #31
E04	VSSA3	P	Ground for analog input AI3x
E11	HPD1	I/O	MSB-6 of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port
E12	HPD3	I/O	MSB-4 of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port
E13	HPD2	I/O	MSB-5 of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port
E14	HPD4	I/O	MSB-3 of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port
F01	AI3D	I/O	Differential input for AI3x
F02	AI32	I	Analog input #32
F03	AI33	I	Analog input #33
F04	VDDA3	P	Supply for analog input AI3x
F11	VSSI3	P	Digital ground core
F12	VDDI3	P	Digital supply core
F13	HPD5	I/O	MSB-2 of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port
F14	HPD6	I/O	MSB-1 of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port
G01	AI34	I	Analog input #34
G02	VDDA3A	P	Supply for analog input AI3x
G03	AI22	I	Analog input #22
G04	AI21	I	Analog input #21
G11	VSSE4	P	Digital ground peripheral cells
G12	IPD1	O	MSB-6 of Image port bus
G13	HPD7	I/O	MSB of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port
G14	IPD0	O	LSB of Image port bus
H01	AI2D	I/O	Differential input for AI2x
H02	AI23	I	Analog input #23
H03	VSSA2	P	Ground for analog input AI2x
H04	VDDA2	P	Supply for analog input AI2x
H11	IPD2	O	MSB-5 of Image port bus
H12	VDDE4	P	Digital supply peripheral cells
H13	IPD4	O	MSB-3 of Image port bus
H14	IPD3	O	MSB-4 of Image port bus
J01	VDDA2A	P	Supply for analog input AI2x
J02	AI11	I	Analog input #11
J03	AI24	I	Analog input #24
J04	VSSA1	P	Ground for analog input AI1x

PAL/NTSC/SECAM Video Decoder with Adaptive Comb Filter,
Component Video Input, VBI-Data Slicer and High Performance Scaler

SAA7118

PIN	NAME	TYPE	DESCRIPTION
J11	VSSI4	P	Digital ground core
J12	VDDI4	P	Digital supply core
J13	IPD6	O	MSB-1 of Image port bus
J14	IPD5	O	MSB-2 of Image port bus
K01	AI12	I	Analog input #12
K02	AI13	I	Analog input #13
K03	AI1D	I/O	Differential input for AI1x
K04	VDDA1	P	Supply for analog input AI1x
K11	IPD7	O	MSB of Image port bus
K12	IGPH	O	Multi purpose horizontal reference signal
K13	IGP1	O	General purpose signal #1
K14	IGPV	O	Multi purpose vertical reference signal
L01	VDDA1A	P	Supply for analog input AI1x
L02	AGNDA	P	Analog signal ground connection
L03	AI14	I	Analog input #14
L04	VSSE5	P	Digital ground peripheral cells
L05	VSSI5	P	Digital ground core
L06	ADP6	O	MSB-2 of Direct A/D-converted output bus (VSB)
L07	ADP3	O	MSB-5 of Direct A/D-converted output bus (VSB)
L08	VSSE6	P	Digital ground peripheral cells
L09	VSSI6	P	Digital ground core
L10	RTCO	O/st/pd (3)	RTC output; strap to LOW (4k7) for first I ² C slave address 42h strap to HIGH (4k7) for second I ² C slave address 40h
L11	VSSE7	P	Digital ground peripheral cells
L12	ITRI	I/O	Image-port control signal, effects all Image port pins
L13	IDQ	O	Data qualifier for image port
L14	IGP0	O	General purpose signal #0
M01	AOUT	O	Analog test output (not for use in application)
M02	VSSA0	P	Ground for internal clock generator
M03	VDDA0	P	Supply for internal clock generator
M04	VDDE5	P	Digital supply peripheral cells
M05	VDDI5	P	Digital supply core
M06	ADP7	O	MSB-1 of Direct A/D-converted output bus (VSB)
M07	ADP2	O	MSB-6 of Direct A/D-converted output bus (VSB)
M08	VDDE6	P	Digital supply peripheral cells
M09	VDDI6	P	Digital supply core
M10	RTS0	O	Real time status or sync information
M11	VDDE7	P	Digital supply peripheral cells
M12	AMXCLK	I	Audio Master External clock input

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SAA7118

PIN	NAME	TYPE	DESCRIPTION
M13	FSW	I/pd	Fast Switch (Blanking), with internal pull-down, inserts component inputs into CVBS signal
M14	ICLK	I/O	Clock output signal for image-port, LCLK of LPB image port mode, or optional asynchronous backend clock input
N01	RES8	NC	Reserved pin for future extensions or testing, do not connect
N02	RES9	I/pu	Reserved pin for future extensions or testing, do not connect
N03	RES10	I/pd	Reserved pin for future extensions or testing, do not connect
N04	CE	I/pu	Chip Enable or Reset with internal pull-up
N05	LLC2	O	Line-locked clock at half frequency (13.5 MHz nominal)
N06	CLKEXT	I	External clock input intended for A/D-conversion of VSB signals (36 MHz)
N07	ADP5	O	MSB-3 of Direct A/D-converted output bus (VSB)
N08	ADP0	O	LSB of Direct A/D-converted output bus (VSB)
N09	SCL	I	I ² C Serial Clock
N10	RTS1	O	Real time status or sync information
N11	ASCLK	O	Audio serial clock
N12	ITRDY	I	Target Ready for image port bus
N13	RES11	NC	Reserved pin for future extensions or testing, do not connect
N14	RES12	NC	Reserved pin for future extensions or testing, do not connect
P02	RES13	I/O	Reserved pin for future extensions or testing, do not connect
P03	EXMCLR	I/pd	External Mode Clear, with internal pull-down
P04	LLC	O	Line-locked clock (27 MHz nominal)
P05	RESON	O	Reset Output Not signal
P06	ADP8	O	MSB of Direct A/D-converted output bus (VSB)
P07	ADP4	O	MSB-4 of Direct A/D-converted output bus (VSB)
P08	ADP1	O	MSB-7 of Direct A/D-converted output bus (VSB)
P09	INT_A	O/od	I ² C interrupt flag (Low if any enabled status bit has changed)
P10	SDA	I/O/od	I ² C Serial Data
P11	AMCLK	O	Audio Master clock, must be less than half the crystal clock frequency
P12	ALRCLK	O/st/pd	Audio left/right clock, strap to LOW (4k7) for 24.576 MHz crystal strap to HIGH (4k7) for 32.11 MHz crystal (3)
P13	TEST0	I/pu	Scan test input; do not connect

TYPE description:
I=input, O=output, P=power, NC=not connected, st=strapping, pu=pull-up, pd=pull-down, od=open drain

Notes

1. This pin provides easy initialization of BST circuitry. TRSTN can be used to force the TAP (Test Access Port) controller to the Test-Logic-Reset state (normal operation) at once
2. According to the IEEE1149.b1-1994 standard the pads TDI and TMS are input pads with a internal pull-up transistor and TDO a tri-state output pad. TCK, TRSTN are also built with internal pile-up
3. Strapping remark: If the strapping pin is unused, the internal pull-down resistor is sufficient for strap function. If pin is used in an application, an external strapping resistor (4,7k) is necessary to get a certain strap function.

FLI2200

Description

The FLI2200 is a single chip implementation of Faroudja Laboratories' award winning deinterlacing and post-processing algorithms that produce the highest quality progressive video output from a variety of interlaced video inputs including 525/60 (NTSC) or 625/50 (PAL or SECAM). It uses patented and patent pending motion-adaptive deinterlacing that selects the optimal filtering on a per-pixel basis. This includes detection and proper interleaving of 3:2 and 2:2 pull-down for film-base sources, including continuous monitoring and compensation for bad edits that occur frequently in broadcast material due to poor scene cuts or insertion of commercials. Video material is processed by a set of content-sensitive spatio-temporal filters that adapt to the appropriate direction for smoothest interpolation using the patented Faroudja DCDi™ algorithm. The FLI2200 also includes motion-adaptive cross-color suppression that removes highly objectionable coloration artifacts produced by commonly used video decoders. Its internal processing uses 10 bits per channel to maintain the highest quality. Its inputs and outputs are 10 bits/channel for best quality but also supports 8 bits/channel for more cost-sensitive applications. The FLI2200 requires 4 MB of low cost SDRAM for best quality deinterlacing, but it can also be operated in an optimized intra-field mode without memory for more cost-sensitive applications. This makes possible the use of a single design for both high-end and low-end applications.

The FLI2200 integrates a number of functions to provide maximum flexibility in a low cost configuration. This includes an on-chip clock generator, SDRAM controller, display controller, input and output color-space converters. It uses a standard 2-wire serial control interface for easy control and access to the registers.

The FLI2200 can be connected without glue logic to the FLI2000 video decoder and FLI2220 Enhancer and OSD Generator to produce the highest quality video pipeline for premium applications. It is also fully compatible with other decoders having a ITU-R BT 656 output format.

Applications

Flat panel TV – LCD, PDP
 Progressive scan TVs
 Multimedia front/rear projectors
 Home Theater
 Scan Converters
 Multimedia PCs/Workstations

DCDi™ is a Faroudja trademark

Features

Motion-adaptive cross-color suppression removes artifacts produced by improper Y/C separation in low-cost video decoders

Motion-adaptive video deinterlacing selects optimal filtering on a per-pixel basis

- Film-mode for proper handling of 3:2 and 2:2 pull-down material

- Bad-edit detection/correction compensates for poor scene cuts and insertions common in broadcast material

- Motion-weighted interpolation for video sources produces maximum resolution without introducing motion artifacts

- Directional Correlational Deinterlacing (DCDi™) minimizes jaggies on angled lines

8/10-bit Y/Cb/Cr (D1) (ITU-R BT 656), 16/20-bit Y Cb/Cr (ITU-R BT 601), 24/30-bit RGB or YCbCr/YPbPr interlaced input options

- ? Supports 525/60 (NTSC), 625/50 (PAL/SECAM)

- ? Accepts up to 1100 pixels/line

8/10-bit, 16/20-bit YUV, 24/30-bit RGB or YCbCr/YPbPr progressive output options

Supports 8- or 10-bit inputs and outputs

10-bit internal processing for highest quality

Includes color-space converters at input and output for maximum flexibility

Auto-detection of NTSC/PAL/SECAM inputs

High-order filtering produces smooth chroma output in 4:2:2 to 4:4:4 or 4:4:4 to 4:2:2 conversions

Resolution recovery maximizes output signal-to-noise ratio and dynamic range

Can be operated without glue logic with FLI2000 Video Decoder and FLI2220 Enhancer and OSD Generator ICs to produce highest quality video pipeline

Glue-less interface to most standard video decoders

Built-in display timing generator

On-chip clock generator eliminates external PLLs

On-chip SDRAM controller

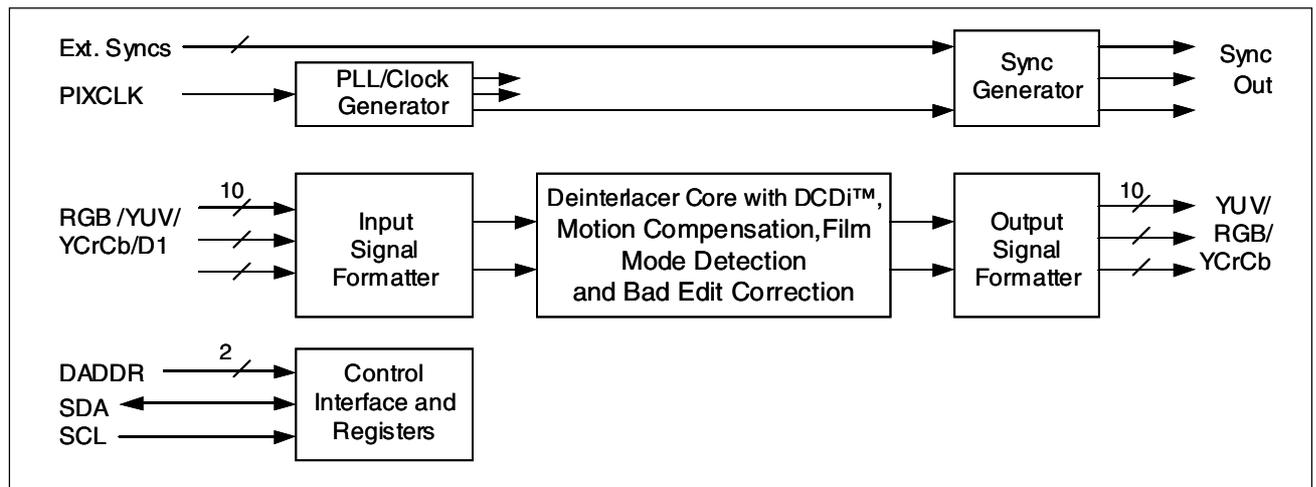
Uses low cost SDRAM as field memory – 4 MB

Optimized intra-field operation allows memory-less configuration for lowest cost applications with same design and layout as for high-end applications

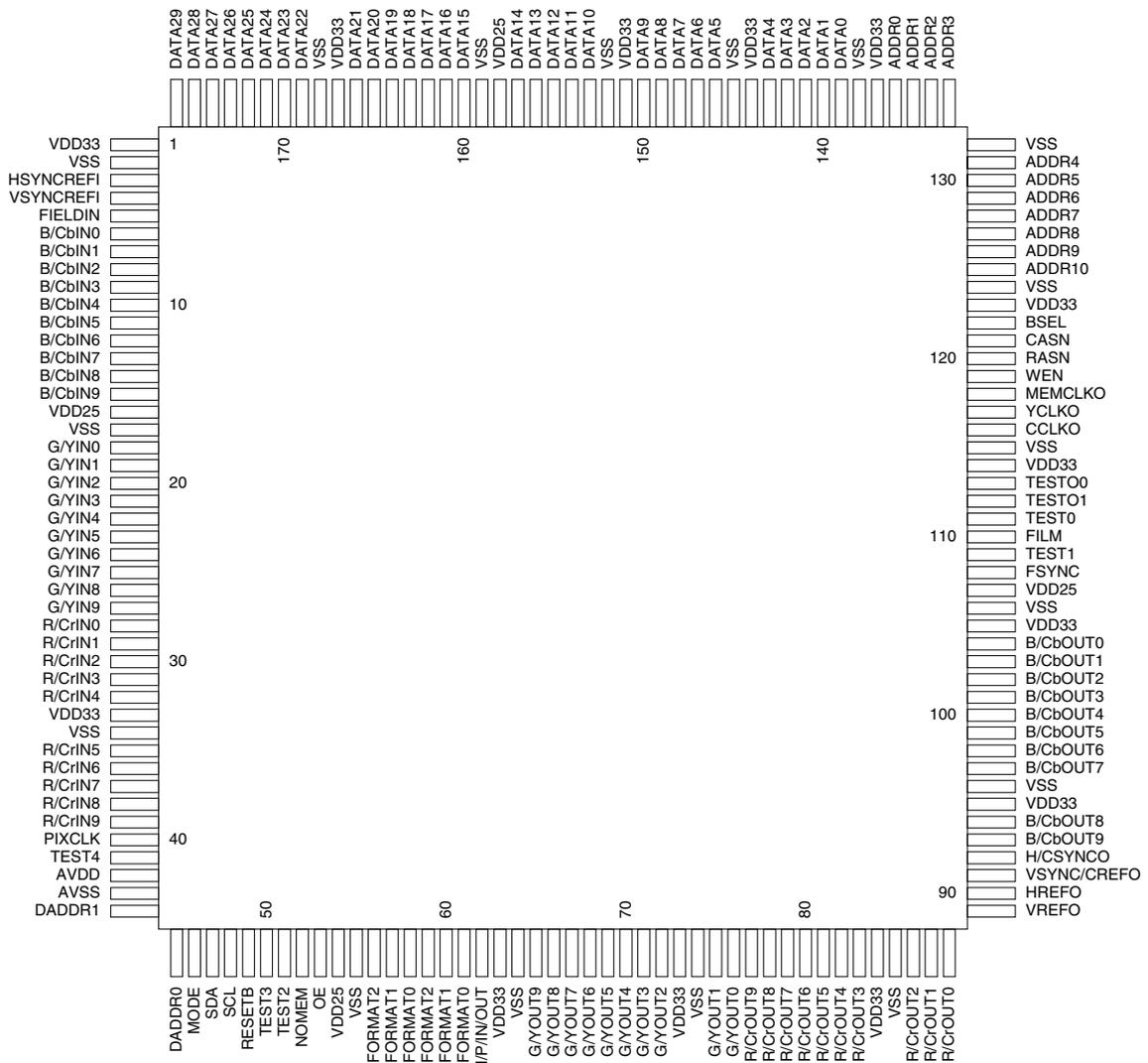
2-wire serial control interface for easy control

176-pin TQFP package

Simplified Block Diagram



Pin description



Pin Connections and Functions

Pin #	Name	Description
See list	V _{SS}	Ground connections. Connect to the digital ground plane. Pins: 2, 17, 34, 55, 64, 74, 85, 96, 106, 115, 124, 132, 138, 145, 152, 159, 168
See list	V _{DD33}	Pad Ring digital power connections. Connect to the digital 3.3 volt power supply and decouple to the digital ground plane. Pins: 1, 33, 63, 73, 84, 95, 105, 114, 123, 137, 144, 151, 167
See list	V _{DD25}	Core Logic digital power connections. Connect to the digital 2.5 volt power supply and decouple to the digital ground plane. Pins: 16, 54, 107, 158
43	AV _{SS}	Ground connection for the clock PLL circuits. Connect to the digital ground plane
42	AV _{DD}	Analog power connections for the clock PLL circuit. Connect to a separately decoupled 2.5 volt power supply and decouple directly to the AV _{SS} pin..
49	RESETB	Reset. When this input is set low it will reset all the internal registers to the default states. Refer to the section on the control registers for details of these states. The device must be reset after it is powered-up.
53	OE	When this pin is set high the outputs of the FLI2200 will be enabled; when it is set low the outputs will be set into a high-impedance state.
56-58	IFORMAT ₂₋₀	Input signal format control. The settings of these pins set the format of the input signal. This can be overridden by the IFmtOvr bit, bit 3 in register 00 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 00 _H for details.
59-61	OFORMAT ₂₋₀	Output signal format control. The settings of these pins set the format of the output signal. This can be overridden by the OFmtOvr bit, bit 3 in register 07 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 07 _H for details.
44-45	DADDR ₁₋₀	The settings of DADDR ₁₋₀ allow the device address of the control bus to be programmed to prevent conflict with the other devices connected to the bus. DADDR ₁₋₀ allow the device address to be set to any of the following values: C0/C1 _H , C2/C3 _H , E0/E1 _H , E2/E3 _H . Please refer to the section “Control Bus Operation and Protocol” for further information.
46	MODE	When this pin is set low the control bus will operate in the slave mode; allowing the device to be programmed from an external controller. When it is set high the FLI2200 will self-program from an external I ² C memory connected to the bus. Please refer to the “Control Bus Operation and Control Protocol” section for more details.
47	SDA	2-wire serial control bus data. Data can be written to the control registers via this pin when it is in the input mode and data can be read from the status registers when it is in the output mode. Refer to the section on the serial port for timing and format details and to the section on the registers for programming information.
48	SCL	2-wire serial control bus clock. When the control port operates in slave mode this pin will be an input and when it operates in the self programming mode it will be an output.
40	PIXCLK	Pixel clock input. This clock is used to drive all the circuits in the FLI2200. An internal PLL is used to upconvert this clock to provide the master clock signal and other clocks used internally. Note that when the FLI2200 is used in the D1 input mode the PIXCLK input should run at the rate of two cycles per pixel (one for luma and one for chroma).
62	N/P/IN/OUT	NTSC/PAL input or output. The default function of this pin is NTSC/PAL signal indicator output. When the input video signal is a 525 line signal this pin will be set high and when it is a 625 line signal the pin is set low. This function of this pin can be programmed to be an input according to the setting of this pin if the NPOp ₁₋₀ bits, bits 5-4 in register 03 _H , are set to 00 _H , overriding the internal line counter. i.e., it will treat the signal as a 525 line signal when it is set high and a 625 line signal when it is set low.

Pin #	Name	Description
52	NOMEM	No Memory Mode control input. This pin controls the operation of the FLI2200 as follows: When this pin is set low the device is used with external field memories and operates in the full set of deinterlacing modes, i.e., motion adaptive video deinterlacing and full frame film source deinterlacing using 3:2 pulldown detection (2:2 pulldown for 625/50 sources). When this pin is set high the FLI2200 is forced into the intra-field only deinterlacing mode, which requires no external memories, allowing the FLI2200 to be used in low-cost applications where the ultimate video quality is not a requirement. To ensure proper startup of the SDRAMs this pin should be set high during the power-up sequence. This can be overridden by the NMOvr bit, bit 1 in register 05 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 05 _H for details.
27-18	G/YIN _{9,0}	10-bit green or luminance signal input bus. The mode is set by the IFORMAT _{2,0} pins. This can be overridden by the IFmtOvr bit, bit 3 in register 00 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 00 _H for details. This signal is sampled on the rising edge of PIXCLK.
15-6	B/CbIN _{9,0}	10-bit blue or Cb chroma signal input bus. The mode is set by the IFORMAT _{2,0} pins. This can be overridden by the IFmtOvr bit, bit 3 in register 00 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 00 _H for details. Bits 6, 4 and 3 in register 08 _H specify the busses used in the multiplexed modes. In all cases the signals are sampled on the rising edges of PIXCLK. In the Y Cb Cr and Y Pb Pr modes the Cb or Pb signal is sampled on alternate rising edges of PIXCLK in 4:2:2 mode. The frequency of PIXCLK will be 27 MHz in the multiplexed Y/Cb/Cr mode and 13.5 MHz in all other modes. These pins should be tied low when not used.
39-35 32-28	R/CrIN _{9,0}	10-bit red or Cr chroma signal input bus. The mode is set by the IFORMAT _{2,0} pins. This can be overridden by the IFmtOvr bit, bit 3 in register 00 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 00 _H for details. Bits 6, 4 and 3 in register 08 _H specify the busses used in the multiplexed modes. In all cases the signals are sampled on the rising edges of PIXCLK. In the Y Cb Cr mode the Cr signal is sampled on alternate rising edges of PIXCLK in 4:2:2 mode. The frequency of PIXCLK will be 27 MHz in the multiplexed Y/Cb/Cr mode and 13.5 MHz in all other modes. These pins should be tied low when not used.
3	HSYNCREFI	Horizontal sync or reference. The horizontal sync or reference of the input signal should be connected to this pin. The function is programmed with bit 4 in register 00 _H . The polarity and position of the sync or reference pulse relative to the start of active video are both programmable within a small range. When the FLI2200 is used in the ITU-R BT 601/D1 input mode with embedded syncs (IFormat = 110) this input is not used and should be tied low; in this case all sync information will be derived from the signal.
4	VSYNCREFI	Vertical sync or reference. The vertical sync or reference of the input signal should be connected to this pin. The function is programmed with bit 4 in register 00 _H . The polarity and position of the sync or reference pulse relative to the start of active video are both programmable within a small range. When the FLI2200 is used in the ITU-R BT 601/D1 input mode with embedded syncs (IFormat = 110) this input is not used and should be tied low; in this case all sync information will be derived from the signal.
5	FLDIN	Field identifier input. The field identifier output of the source signal should be connected to this pin. A low setting signifies an even field and a high level signifies an odd field. When bit 4 in register 00 _H is set low, the input timing is based on HREF and VREF and this signal is required. When this bit is set high the input timing is based on HSYNC and VSYNC and this signal is generated internally and is not required. When bit 5 in register 06 is set high this signal is also used as the frame boundary identifier for 30 Hz film sources.

Pin #	Name	Description
65-72 75-76	G/YOUT _{9,0}	Green or luminance output bus. In the RGB mode this output is the Green signal and in the YCbCr mode it is the Y signal. The mode is set by the OFORMAT _{2,0} pins. This can be overridden by the OFmtOvr bit, bit 3 in register 07 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 07 _H for details. The signal is clocked out on the falling edge of YCLKO.
93-94 97-104	B/CbOUT _{9,0}	Blue or Cb chrominance output bus. In the RGB mode this output is the Blue signal, in the Y Cb Cr mode it is the Cb signal. The mode is set by the OFORMAT _{2,0} pins. This can be overridden by the OFmtOvr bit, bit 3 in register 07 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 07 _H for details. The busses used in the multiplexed modes are set by means of bit 5 in register 08 _H . The signal is clocked out on the falling edge of YCLKO in the RGB and YUV 4:4:4 modes, on the falling edge of YCLKO prior to the next rising edge of CCLKO in the YUV 4:2:2 mode, and on the rising edge of MEMCLKO in the multiplexed YCbCr (pseudo D1) mode.
77-83 86-88	R/CrOUT _{9,0}	Red or Cr chrominance output bus. In the RGB mode this output is the Red signal, in the YCbCr mode it is the Cr signal. The mode is set by the OFORMAT _{2,0} pins. This can be overridden by the OFmtOvr bit, bit 3 in register 07 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 07 _H for details. The busses used in the multiplexed modes are set by means of bit 5 in register 08 _H . The signal is clocked out on the falling edge of YCLKO in the RGB and YUV 4:4:4 modes, on the falling edge of YCLKO prior to the next rising edge of CCLKO in the YUV 4:2:2 mode, and on the rising edge of MEMCLKO in the multiplexed YCbCr (pseudo D1) mode.
116	CCLKO	Chroma output sampling clock. This clock is derived from PIXCLK and will be at half the frequency of YCLKO. In 30-bit 4:2:2 output mode the chroma output signals will change on the falling edge of YCLKO prior to the next rising edge this clock.
117	YCLKO	Luma output sampling clock. This clock is derived from PIXCLK and is double the frequency of PIXCLK. In 30-bit and 20-bit output modes the output signals will change on the falling edge of this clock.
89	VREFO	Start of active field or frame indicator. This signal goes high to indicate the first active line in each field or frame and goes low during the vertical blanking interval. The polarity and timing of this signal are programmable.
90	HREFO	Start of active line indicator output. This signal goes high to indicate the first active pixel in each line and goes low during the horizontal blanking interval. The polarity and timing of this signal are programmable.
91	VSYNC/ CREFO	Vertical sync output. This signal provides the vertical sync function for the outputs. Its polarity is programmable to be active high or active low. It can also be programmed to be a composite reference for applications requiring this instead of sync.
92	H/CSYNCO	Horizontal or composite sync output. This signal provides the horizontal sync function for the outputs. Its polarity is programmable to be active high or active low. This signal can also be programmed to be the composite sync output, CSYNC.
108	FSYNC	Film mode sync output. When film mode is detected this pin will toggle in sync with the 3:2 (NTSC) or 2:2 (PAL and 30 Hz film in NTSC) pulldown sequence detected in the source.
110	FILM	Film mode detector output. This pin will be set high when the FLI2200 detects that the video input was converted from 24 fps film with a teleciné machine. If film mode is not detected this pin will be set low.

Pin #	Name	Description
125-131 133-136	ADDR ₁₀₋₀	SDRAM Address bus. This signal bus is used to address the external SDRAM(s) used for field memories. It should be connected to the A ₁₀₋₀ bus of the memory chip(s). Please refer to the Applications section of this data sheet for further details.
176-169 166-160 157-153 150-146 143-139	DATA ₂₉₋₀	SDRAM Data bus. This signal bus is used to transfer the data to and from the external SDRAM(s) used for field memories. It should be connected to the DQ ₂₉₋₀ bus of the memory chip when using a 64 Mbit SDRAM. When using two 16 Mbit SDRAMs this 30-bit bus may be connected to the two 16-bit data busses of the memories in two ways: either connect 16 lines to one chip and 14 to the other, or connect 15 to both. In all cases the two unused data lines on the memory chip(s) should be connected to ground via 22 k Ω resistors. Please refer to the Applications section of this data sheet for further details.
118	MEMCLKO	SDRAM clock and 2x output sampling clock. This clock is derived from PIXCLK and will be at double the frequency of YCLKO. This active signal should be connected to the CLK pin(s) on the SDRAM(s). When the 10-bit output mode selected the output signals will also change at this clock rate and this should then be used as the output clock..
119	WEN	SDRAM Write Enable. This active low signal should be connected to the WE pin(s) on the SDRAM(s).
120	RASN	SDRAM Row Address Select. This active low signal should be connected to the RAS pin(s) on the SDRAM(s).
121	CASN	SDRAM Column Address Select. This active low signal should be connected to the CAS pin(s) on the SDRAM(s).
122	BSEL	SDRAM Bank Select. When using two 16 Mbit SDRAMs this signal should be connected to the BA (also called BS or A ₁₁) pin on both SDRAMs. When using a 64 Mbit SDRAM this signal should be connected to the BA0 (also called BS0 or A ₁₁) pin on the SDRAM and BA1/BS1 (also called BA when BA0 is referred to as A ₁₁) should be tied low.
41, 50, 51, 109, 111	TEST ₄₋₀	These pins are used for test purposes only and should always be tied low for normal operation.
112, 113	TESTO ₁₋₀	These pins are test outputs and should be left unconnected in normal operation.



64Mb: x32
SDRAM

SYNCHRONOUS DRAM

MT48LC2M32B2 - 512K x 32 x 4 banks

For the latest data sheet, please refer to the Micron Web site: www.micronsemi.com/datasheets/sdramds.html

FEATURES

- PC100 functionality
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge, includes CONCURRENT AUTO PRECHARGE, and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh (15.6µs/row)
- LVTTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply
- Supports CAS latency of 1, 2, and 3.

OPTIONS

- Configuration
2 Meg x 32 (512K x 32 x 4 banks)
- Plastic Package - OCPL¹
86-pin TSOP (400 mil)
- Timing (Cycle Time)
 - 5ns (200 MHz)
 - 5.5ns (183 MHz)
 - 6ns (166 MHz)
 - 7ns (143 MHz)
- Operating Temperature Range
Commercial (0° to +70°C)
Extended (-40°C to +85°C)

MARKING

2M32B2

TG

-5
-55
-6
-7

None
IT²

- NOTE: 1. Off-center parting line
2. Available on -7

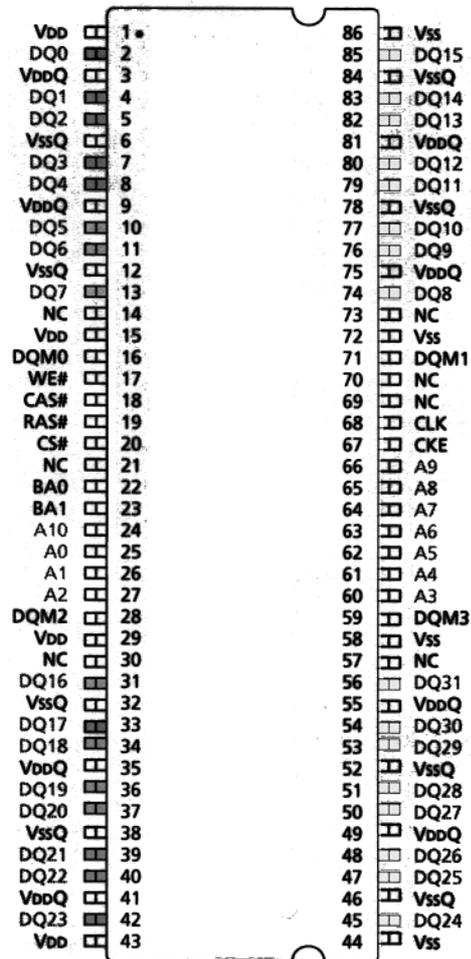
Part Number Example:
MT48LC2M32B2TG-7

KEY TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME CL = 3*	SETUP TIME	HOLD TIME
-5	200 MHz	4.5ns	1.5ns	1ns
-55	183 MHz	5ns	1.5ns	1ns
-6	166 MHz	5.5ns	1.5ns	1ns
-7	143 MHz	5.5ns	2ns	1ns

*CL = CAS (READ) latency

PIN ASSIGNMENT (TOP VIEW) 86-PIN TSOP



Note: The # symbol indicates signal is active LOW.

	2 Meg x 32
Configuration	512K x 32 x 4 banks
	4K
	2K (A0-A10)
	4 (BA0, BA1)
	256 (A0-A7)


**64Mb: x32
SDRAM**

64Mb (x32) SDRAM PART NUMBER

PART NUMBER	ARCHITECTURE
MT48LC2M32B2TG	2 Meg x 32

GENERAL DESCRIPTION

The 64Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 67,108,864-bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 16,777,216-bit banks is organized as 2,048 rows by 256 columns by 32 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A10 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 64Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the $2n$ rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

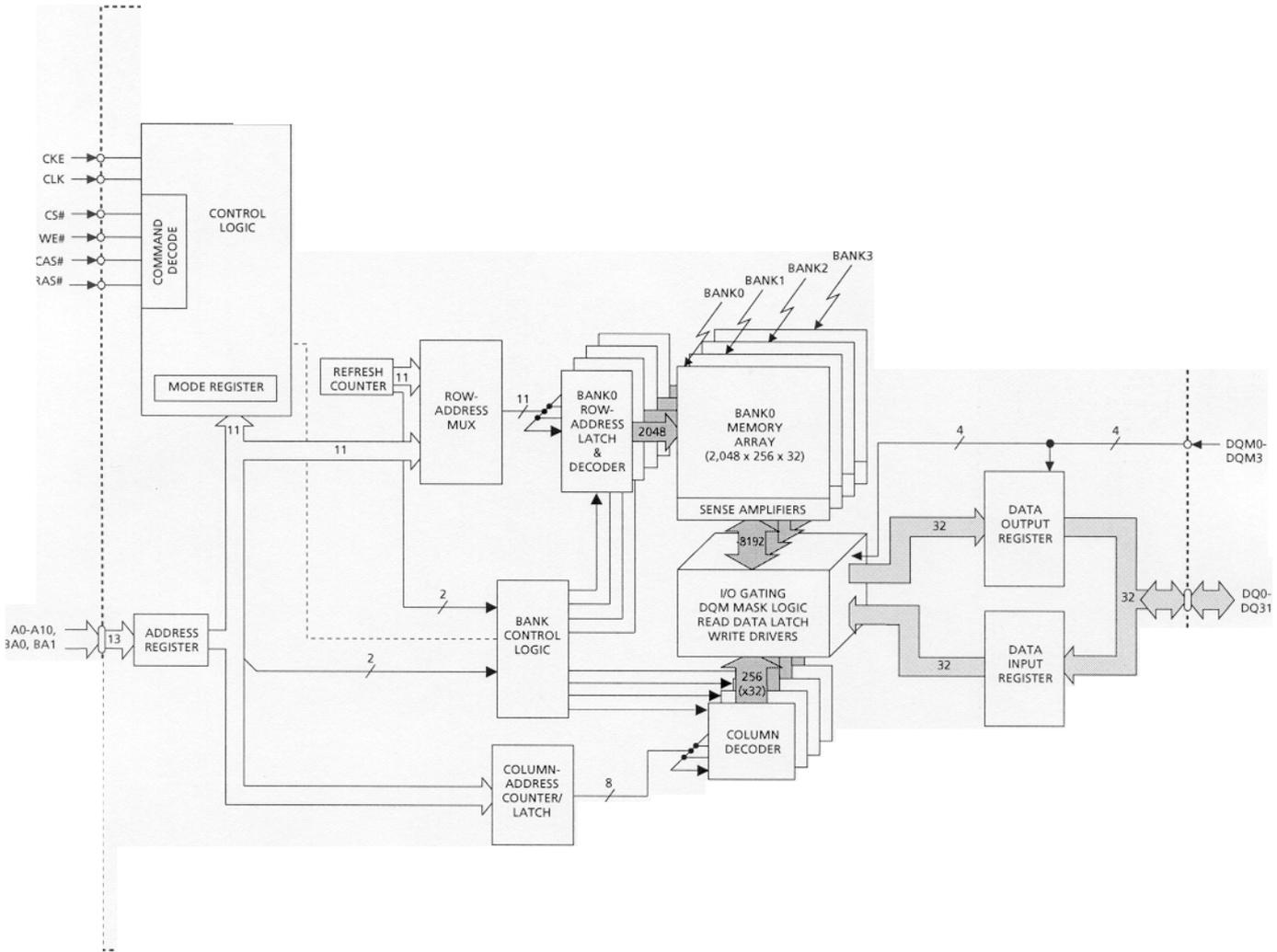
The 64Mb SDRAM is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access.



64Mb: x32
SDRAM

FUNCTIONAL BLOCK DIAGRAM
2 Meg x 32 SDRAM




**64Mb: x32
SDRAM**
PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
68	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
67	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), ACTIVE POWER-DOWN (row active in any bank) or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
20	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
17, 18, 19	WE#, CAS#, RAS#	Input	Command Inputs: WE#, CAS#, and RAS# (along with CS#) define the command being entered.
16, 71, 28, 59	DQM0-DQM3	Input	Input/Output Mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) during a READ cycle. DQM0 corresponds to DQ0-DQ7; DQM1 corresponds to DQ8-DQ15; DQM2 corresponds to DQ16-DQ23; and DQM3 corresponds to DQ24-DQ31. DQM0-DQM3 are considered same state when referenced as DQM.
22, 23	BA0, BA1	Input	Bank Address Input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
25-27, 60-66, 24	A0-A10	Input	Address Inputs: A0-A10 are sampled during the ACTIVE command (row-address A0-A10) and READ/WRITE command (column-address A0-A7 with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODEREGISTER command.
2, 4, 5, 7, 8, 10, 11, 13, 74, 76, 77, 79, 80, 82, 83, 85, 31, 33, 34, 36, 37, 39, 40, 42, 45, 47, 48, 50, 51, 53, 54, 56	DQ0-DQ31	Input/Output	Data I/Os: Data bus.
14, 21, 30, 57, 69, 70, 73	NC	-	No Connect: These pins should be left unconnected. Pin 70 is reserved for SSTL reference voltage supply.
3, 9, 35, 41, 49, 55, 75, 81	V _{DDQ}	Supply	DQ Power Supply: Isolated on the die for improved noise immunity.
6, 12, 32, 38, 46, 52, 78, 84	V _{SSQ}	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
1, 15, 29, 43	V _{DD}	Supply	Power Supply: +3.3V ±0.3V.
44, 58, 72, 86	V _{SS}	Supply	Ground.

ADV7196A

INPUT FORMATS

YCrCb in 2x10-Bit (4:2:2) or 3x10-Bit (4:4:4) format compliant to SMPTE-293M (525p), ITU-R.BT1358 (625p), SMPTE274M (1080i), SMPTE296M (720p) and any other High Definition standard using Async Timing Mode
 RGB in 3x10 Bit 4:4:4 format

OUTPUT FORMATS

YPrPb Progressive Scan (EIA-770.1, EIA-770.2)
 YPrPb HDTV (EIA 770.3)
 RGB levels compliant to RS-170 and RS-343A
 11-Bit + Sync (DAC A)
 11-Bit DACs (DAC B, DAC C)

PROGRAMMABLE FEATURES

Internal Testpattern Generator with Color Control
 Y/C delay (+/-)
 Gamma Correction
 Individual DAC on/off control
 54MHz Output (2xOversampling)
 Sharpness filter with programmable gain/attenuation

GENERAL DESCRIPTION

The ADV7196A is a triple high speed, digital-to-analog encoder on a single monolithic chip. It includes of three high speed video D/A converters with TTL compatible inputs.

The ADV7196A has three separate 10-Bit wide input ports which accept data in 4:4:4 10-Bit YCrCb or RGB or 4:2:2 10-Bit YCrCb. This data is accepted in progressive scan format at 27MHz or HDTV format at 74.25MHZ or 74.1758MHz. For any other High Definition standard but SMPTE 293M, ITU-R BT.1358, SMPTE274M or SMPTE296M the Async Timing Mode can be used to input data to the ADV7196A. For all standards, external horizontal, vertical and blanking signals or EAV/SAV codes control the insertion of appropriate synchronisation signals into the digital data stream and therefore the output signals.

The ADV7196A outputs analog YPrPb progressive scan format complying to EIA770.1, EIA 770.2 or YPrPb HDTV complying to EIA 770.3 or RGB complying to RS-170/RS 343A.

The ADV7196A requires a single 3.3V power supply, an optional external 1.235 V reference and a 27 MHz clock in Progressive Scan Mode or a 74.25MHz (or 74.1758MHz) clock in HDTV mode.

Programmable Adaptive Filter Control
 Undershoot Limiter
 VBI Open Control
 I2C Filter
 Macrovision Rev 1.0 (525p)
 CGMS-A (525p)
 2 Wire Serial MPU Interface

Single Supply +3.3 V Operation
 52-MQFP package

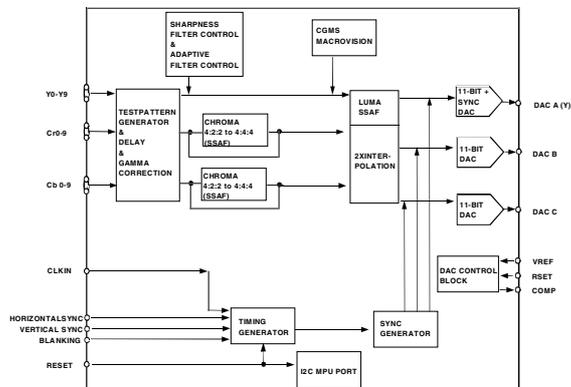
APPLICATIONS

Progressive Scan / HDTV Display Devices
 DVD Players
 Progressive Scan/HDTV Projection Systems
 MPEG2@81MHz
 Digital Video Systems
 High Resolution Color Graphics
 Image Processing/ Instrumentation
 Digital Radio Modulation/ Video Signal Reconstruction

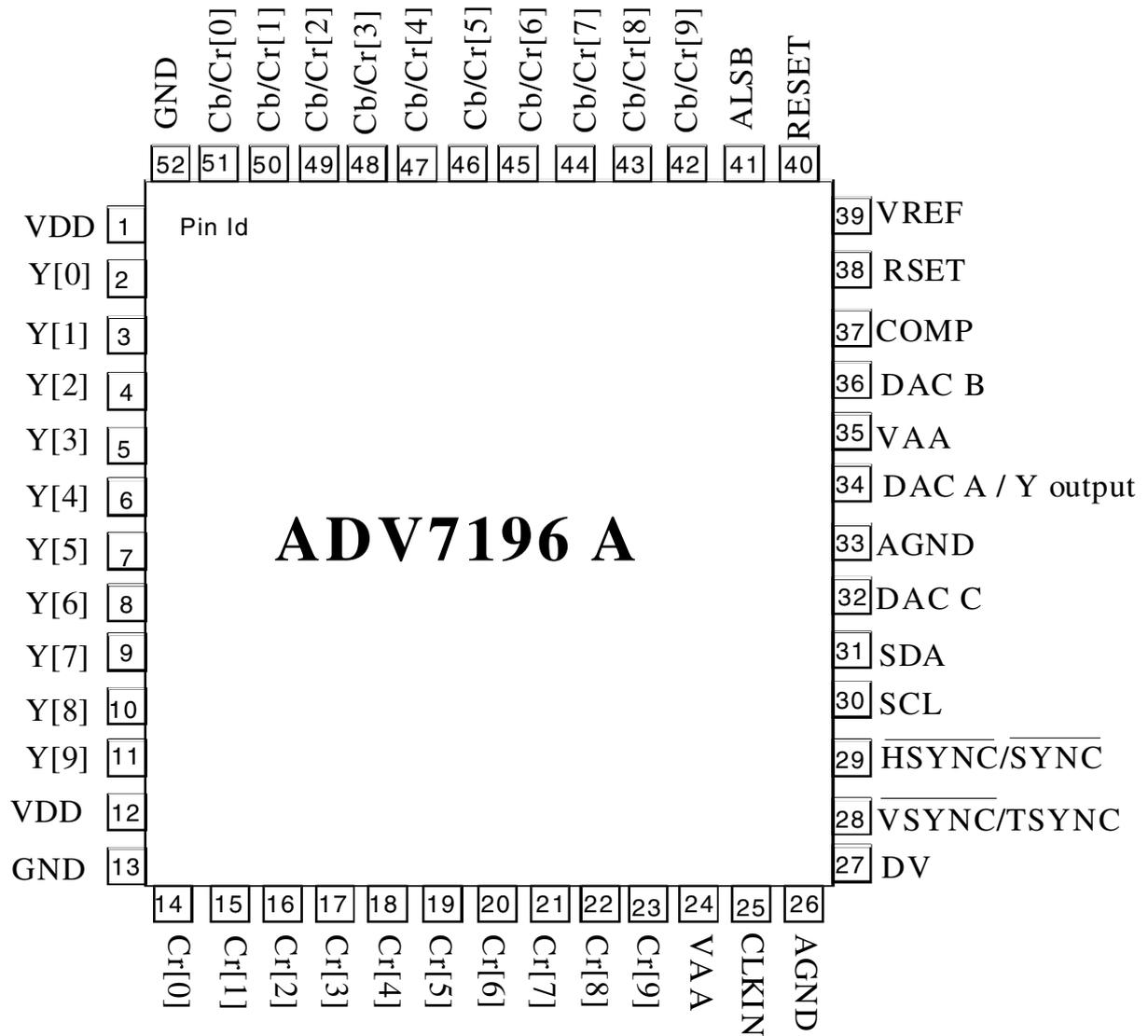
In Progressive Scan Mode, a Sharpness Filter with programmable gain allows high frequency enhancement on the luminance signal. Programmable Adaptive Filter Control which may be used, allows removal of ringing on the incoming Y data. The ADV7196A supports CGMS-A data control generation and the Macrovision Anticopy algorithm in 525p mode.

The ADV7196A is packaged in a 52-Pin MQFP package.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin	Mnemonic	Input/Output	Function
GND	G		Digital Ground
AGND	G		Analog Ground
ALSB	I		TTL Address Input. This signal sets up the LSB of the MPU address. When this pin is tied high the I2C filter is activated which reduces noise on the I2C interface. When this pin is tied low, the input bandwidth on the I2C lines is increased.
DV	I		Video Blanking Control Signal Input.
CLKIN	I		Pixel Clock Input. Requires a 27MHz reference clock for standard operation in Progressive Scan Mode or a 74.25MHz (74.1758MHz) reference clock in HDTV mode.
COMP	O		Compensation Pin for DACs. Connect 0.1 μ F Capacitor from COMP pin to V _{AA} .
DAC A	O		Y analog output.
DAC B	O		Color component analog output of input data on Cr 9-0 input pins.
DAC C	O		Color component analog output of input data on Cb/Cr 9-0 input pins.
<u>HSYNC/</u> <u>SYNC</u>	I		<u>HSYNC</u> , horizontal sync control signal input or SYNC input control signal in Async Timing Mode.
Cr 9-0	I		10-Bit Progressive scan/ HDTV input port for color data in 4:4:4 input mode. In 4:2:2 mode this input port is not used. Input port for R data when RGB data is input.
Cb/Cr 9-0	I		10-Bit Progressive scan/ HDTV input port for color data. In 4:2:2 mode the multiplexed CrCb data must be input on these pins. Input port for B data when RGB is input.
<u>RESET</u>	I		This input resets the on-chip timing generator and sets the ADV7196A into Default Register setting. Reset is an active low signal.
R _{SET}	I		A 2470 Ohms resistor (for input ranges 64-940 and 64-960, output standards EIA770.1-3) must be connected from this pin to AGND and is used to control the amplitudes of the DAC outputs. For input ranges 0 -1023 (RS-170,RS-343A) the R _{SET} value must be 2820 Ohms.
SCL	I		MPU Port Serial Interface Clock Input
SDA	I/O		MPU Port Serial Data Input/Output
<u>VSYNC/</u> <u>TSYNC</u>	I		<u>VSYNC</u> , vertical sync control signal input or TSYNC input control signal in AsyncTiming Mode.
V _{DD}	P		Digital power supply
V _{AA}	P		Analog power supply
V _{REF}	I/O		Optional External Voltage Reference Input for DACs or Voltage Reference Output (1.235V).
Y9 -Y0	I		10-Bit Progressive scan/ HDTV input port for Y data. Input for G data when RGB data is input.

9.9 IC's Divio

9.9.1 IC7101: 58PDI1394P25PHY

PDI1394P25

1.0 FEATURES

- Fully supports provisions of IEEE 1394±1995 Standard for high performance serial bus and the P1394a±2000 Standard¹
- Fully interoperable with Firewire[®] and i.LINK[™] implementations of the IEEE 1394 Standard.²
- Full P1394a support includes:
 - ± Connection debounce
 - ± Arbitrated short reset
 - ± Multispeed concatenation
 - ± Arbitration acceleration
 - ± Fly-by concatenation
 - ± Port disable/suspend/resume
- Provides one 1394a fully-compliant cable port at 100/200/400 Mbps. Can be used as a one port PHY without the use of any extra external components
- Fully compliant with Open HCI requirements
- Cable ports monitor line conditions for active connection to remote node.
- Power down features to conserve energy in battery-powered applications include:
 - ± Automatic device power down during suspend
 - ± Device power down terminal
 - ± Link interface disable via LPS
 - ± Inactive ports powered-down
- Logic performs system initialization and arbitration functions
- Encode and decode functions included for data-strobe bit level encoding
- Incoming data resynchronized to local clock
- Single 3.3 volt supply operation
- Minimum V_{DD} of 2.7 V for end-of-wire power-consuming devices
- While unpowered and connected to the bus, will not drive TPBIAS on a connected port, even if receiving incoming bias voltage on that port

- Supports extended bias-handshake time for enhanced interoperability with camcorders
- Interface to link-layer controller supports both low-cost bus-holder isolation and optional Annex J electrical isolation
- Data interface to link-layer controller through 2/4/8 parallel lines at 49.152 MHz
- Low-cost 24.576 MHz crystal provides transmit, receive data at 100/200/400 Mbps, and link-layer controller clock at 49.152 MHz
- Does not require external filter capacitors for PLL
- Interoperable with link-layer controllers using 3.3 V and 5 V supplies
- Interoperable with other Physical Layers (PHYs) using 3.3 V and 5 V supplies
- Node power class information signaling for system power management
- Cable power presence monitoring
- Separate cable bias (TPBIAS) for each port
- Register bits give software control of contender bit, power class bits, link active bit, and 1394a features
- Function and pin compatible with the Texas Instruments TSB41LV01[®] 400 Mbps Phy

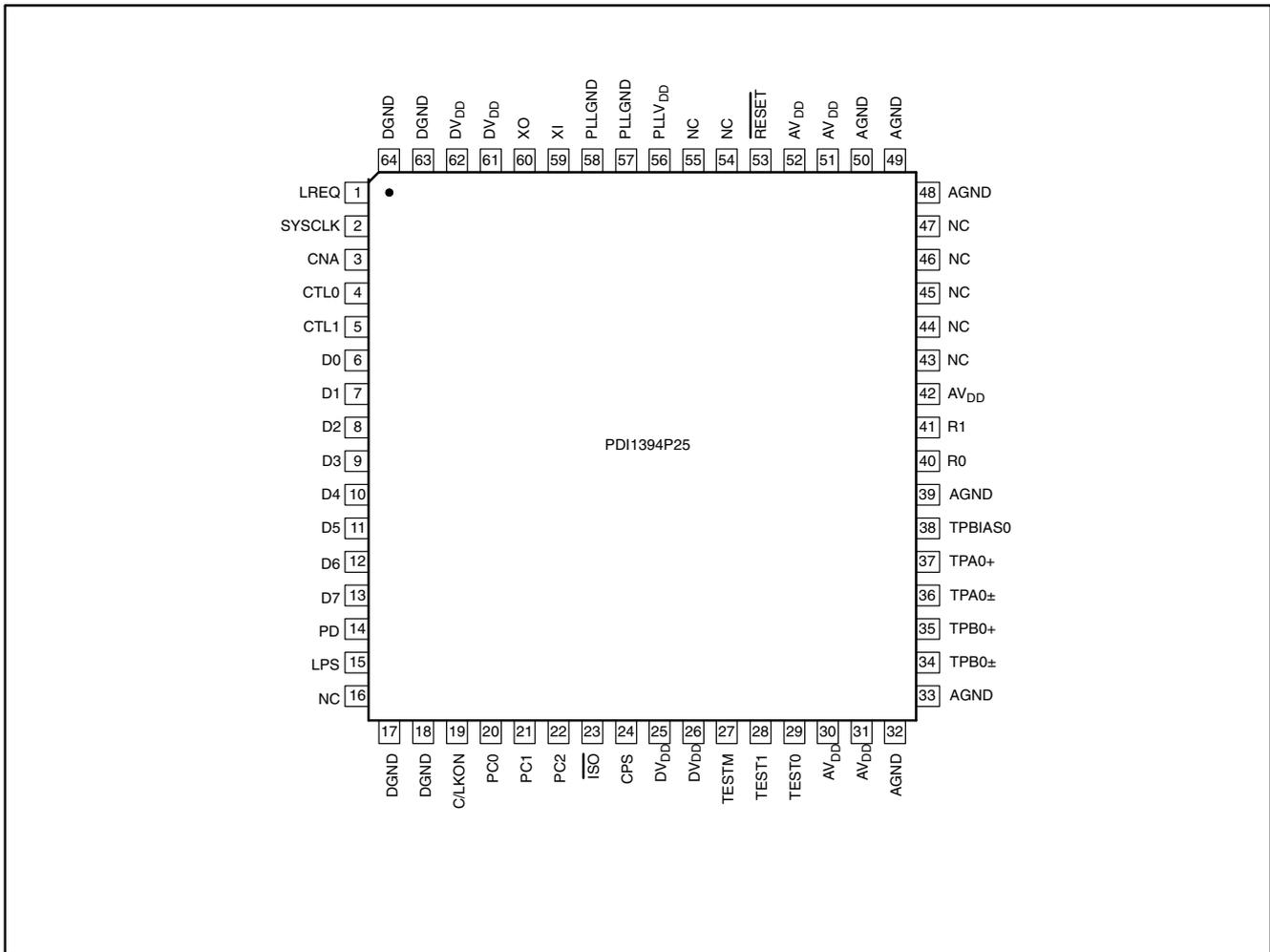
2.0 DESCRIPTION

The PDI1394P25 provides the digital and analog transceiver functions needed to implement a one port node in a cable-based IEEE 1394±1995 and/or 1394a network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The PDI1394P25 is designed to interface with a Link Layer Controller (LLC), such as the PDI1394L11 or PDI1394L21.

3.0 ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	ORDER CODE	PKG. DWG. #
64-pin plastic LQFP	0 to +70°C	PDI1394P25BD	SOT314-2

4.0 PIN CONFIGURATION



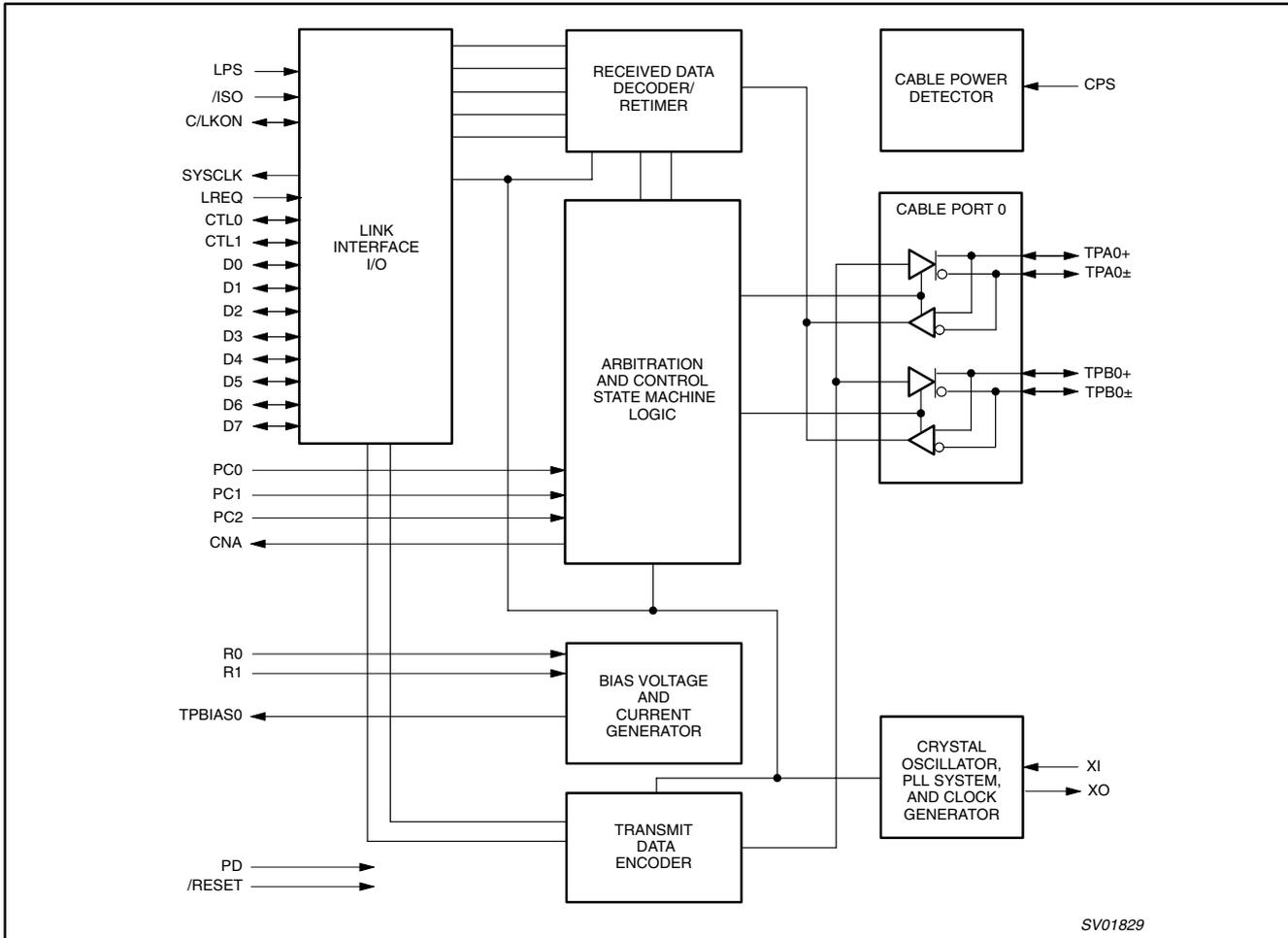
5.0 PIN DESCRIPTION

Name	Pin Type	Pin Numbers	I/O	Description
AGND	Supply	32, 33, 39, 48, 49, 50	⊘	Analog circuit ground terminals. These terminals should be tied together to the low impedance circuit board ground plane.
AV _{DD}	Supply	30, 31, 42, 51, 52	⊘	Analog circuit power terminals. A combination of high frequency decoupling capacitors on each side are suggested, such as paralleled 0.1 μF and 0.001 μF. These supply terminals are separated from PLLV _{DD} and DV _{DD} internal to the device to provide noise isolation. They should be tied at a low impedance point on the circuit board.
C/LKON	CMOS 5 V tol	19	I/O	<p>Bus Manager Contender programming input and link-on output. On hardware reset, this terminal is used to set the default value of the contender status indicated during self-ID. Programming is done by tying the terminal through a 10-kΩ resistor to a high (contender) or low (not contender). The resistor allows the link-on output to override the input.</p> <p>If this pin is connected to a LLC driver pin for setting Bus Manager/IRM contender status, then a 10-kΩ series resistor should be placed on this line between the PHY and the LLC to prevent possible contention. In this case, the pull-high or pull-low resistors mentioned in the previous paragraph should not be used. Refer to Figure 9.</p> <p>Following hardware reset, this terminal is the link-on output, which is used to notify the LLC to power-up and become active. The link-on output is a square-wave signal with a period of approximately 163 ns (8 SYCLK cycles) when active. The link-on output is otherwise driven low, except during hardware reset when it is high impedance.</p> <p>The link-on output is activated if the LLC is inactive (LPS inactive or the LCtrl bit cleared) and when:</p> <ol style="list-style-type: none"> the PHY receives a link-on PHY packet addressed to this node, the PEI (port-event interrupt) register bit is 1, or any of the CTOI (configuration-timeout interrupt), CPSI (cable-power-status interrupt), or STOI (state-timeout interrupt) register bits are 1 and the RPIE (resuming-port interrupt enable) register bit is also 1. <p>Once activated, the link-on output will continue active until the LLC becomes active (both LPS active and the LCtrl bit set). The PHY also deasserts the link-on output when a bus-reset occurs unless the link-on output would otherwise be active because one of the interrupt bits is set (i.e., the link-on output is active due solely to the reception of a link-on PHY packet).</p> <p>NOTE: If an interrupt condition exists which would otherwise cause the link-on output to be activated if the LLC were inactive, the link-on output will be activated when the LLC subsequently becomes inactive.</p>
CNA	CMOS	3	O	Cable Not Active output. This terminal is asserted high when there are no ports receiving incoming bias voltage.
CPS	CMOS	24	I	Cable Power Status input. This terminal is normally connected to cable power through a 390 kΩ resistor. This circuit drives an internal comparator that is used to detect the presence of cable power.
CTL0, CTL1	CMOS 5 V tol	4, 5	I/O	Control I/Os. These bi-directional signals control communication between the PDI1394P25 and the LLC. Bus holders are built into these terminals.
D0±D7	CMOS 5 V tol	6, 7, 8, 9, 10, 11, 12, 13	I/O	Data I/Os. These are bi-directional data signals between the PDI1394P25 and the LLC. Bus holders are built into these terminals. Unused Dn pins should be pulled to ground through 10 kΩ resistors.
DGND	Supply	17, 18, 63, 64	⊘	Digital circuit ground terminals. These terminals should be tied together to the low impedance circuit board ground plane.
DV _{DD}	Supply	25, 26, 61, 62	⊘	Digital circuit power terminals. A combination of high frequency decoupling capacitors near each side of the IC package are suggested, such as paralleled 0.1 μF and 0.001 μF. Lower frequency 10 μF filtering capacitors are also recommended. These supply terminals are separated from PLLV _{DD} and AV _{DD} internal to the device to provide noise isolation. They should be tied at a low impedance point on the circuit board.

Name	Pin Type	Pin Numbers	I/O	Description
ISO	CMOS	23	I	Link interface isolation control input. This terminal controls the operation of output differentiation logic on the CTL and D terminals. If an optional isolation barrier of the type described in Annex J of IEEE Std 1394±1395 is implemented between the PDI1394P25 and LLC, the ISO terminal should be tied low to enable the differentiation logic. If no isolation barrier is implemented (direct connection), or bus holder isolation is implemented, the ISO terminal should be tied high to disable the differentiation logic.
LPS	CMOS 5 V tol	15	I	<p>Link Power Status input. This terminal is used to monitor the active/power status of the link layer controller and to control the state of the PHY-LLC interface. This terminal should be connected to either the V_{DD} supplying the LLC through a 10 kΩ resistor, or to a pulsed output which is active when the LLC is powered. A pulsed signal should be used when an isolation barrier exists between the LLC and PHY. (See Figure 8)</p> <p>The LPS input is considered inactive if it is sampled low by the PHY for more than 2.6 μs (128 SYSCLK cycles), and is considered active otherwise (i.e., asserted steady high or an oscillating signal with a low time less than 2.6 μs). The LPS input must be high for at least 21 ns in order to be guaranteed to be observed as high by the PHY.</p> <p>When the PDI1394P25 detects that LPS is inactive, it will place the PHY-LLC interface into a low-power reset state. In the reset state, the CTL and D outputs are held in the logic zero state and the LREQ input is ignored; however, the SYSCLK output remains active. If the LPS input remains low for more than 26 μs (1280 SYSCLK cycles), the PHY-LLC interface is put into a low-power disabled state in which the SYSCLK output is also held inactive. The PHY-LLC interface is placed into the disabled state upon hardware reset.</p> <p>The LLC is considered active only if both the LPS input is active and the LCtrl register bit is set to 1, and is considered inactive if either the LPS input is inactive or the LCtrl register bit is cleared to 0.</p>
LREQ	CMOS 5 V tol	1	I	LLC Request input. The LLC uses this input to initiate a service request to the PDI1394P25. Bus holder is built into this terminal.
NC	No connect	54, 55	⌀	These pins are not internally connected and consequently are "don't cares". Other vendors' pin compatible chips may require connections and external circuitry on these pins.
NC	No connect	16, 43, 44, 45, 46, 47	⌀	No connect.
PC0, PC1, PC2	CMOS 5 V tol	20, 21, 22	I	Power Class programming inputs. On hardware reset, these inputs set the default value of the power class indicated during self-ID. Programming is done by tying the terminals high or low. Refer to Table 21 for encoding.
PD	CMOS 5 V tol	14	I	Power Down input. A logic high on this terminal turns off all internal circuitry except the cable-active monitor circuits which control the CNA output. For more information, refer to Section 17.2
PLL _{GND}	Supply	57, 58	⌀	PLL circuit ground terminals. These terminals should be tied together to the low impedance circuit board ground plane.
PLL _{V_{DD}}	Supply	56	⌀	PLL circuit power terminals. A combination of high frequency decoupling capacitors near each terminal are suggested, such as paralleled 0.1 μF and 0.001 μF. These supply terminals are separated from DV _{DD} and AV _{DD} internal to the device to provide noise isolation. They should be tied at a low impedance point on the circuit board.
RESET	CMOS 5 V tol	53	I	Logic reset input. Asserting this terminal low resets the internal logic. An internal pull-up resistor to V _{DD} is provided so only an external delay capacitor is required for proper power-up operation. For more information, refer to Section 17.2. This input is otherwise a standard Schmitt logic input, and can also be driven by an open-drain type driver.
R0, R1	Bias	40, 41	⌀	Current setting resistor pins These pins are connected to an external resistance to set the internal operating currents and cable driver output currents. A resistance of 6.34 kΩ ±1% is required to meet the IEEE 1394±1995 Std. output voltage limits.

Name	Pin Type	Pin Numbers	I/O	Description
SYSCLK	CMOS	2	O	System clock output. Provides a 49.152 MHz clock signal, synchronized with data transfers, to the LLC.
TEST0	CMOS	29	I	Test control input. This input is used in manufacturing tests of the PDI1394P25. For normal use, this terminal should be tied to GND.
TEST1	CMOS	28	I	Test control input. This input is used in manufacturing tests of the PDI1394P25. For normal use, this terminal should be tied to GND. Other vendors' pin compatible chips may require connections and external circuitry on this pin.
TESTM	CMOS	27	I	Test control input. This input is used in manufacturing tests of the PDI1394P25. For normal use, this terminal should be tied to V _{DD} .
TPA0+	Cable	37	I/O	Twisted-pair cable A differential signal terminals. Board traces from each pair of positive and negative differential signal terminals should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPA0±	Cable	36	I/O	
TPB0+	Cable	35	I/O	Twisted-pair cable B differential signal terminals. Board traces from each pair of positive and negative differential signal terminals should be kept matched and as short as possible to the external load resistors and to the cable connector.
TPB0±	Cable	34	I/O	
TPBIAS0	Cable	38	I/O	Twisted-pair bias output. This provides the 1.86 V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers, and for signaling to the remote nodes that there is an active cable connection. These terminals must be decoupled with a 0.3 μF±1 μF capacitor to ground.
XO, XI	Crystal	59, 60	⊘	Crystal oscillator inputs. These terminals connect to a 24.576 MHz parallel resonant fundamental mode crystal. The optimum values for the external shunt capacitors are dependent on the specifications of the crystal used. Can also be driven by an external clock generator (leave XO unconnected in this case and start supplying the external clock before resetting the PDI1394P25). For more information, refer to Section 17.5

6.0 BLOCK DIAGRAM



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7.0 FUNCTIONAL SPECIFICATION

The PDI1394P25 requires only an external 24.576 MHz crystal as a reference. An external clock can be connected to XI instead of a crystal. An internal oscillator drives an internal phase-locked loop (PLL), which generates the required 393.216 MHz reference signal. This reference signal is internally divided to provide the clock signals used to control transmission of the outbound encoded Strobe and Data information. A 49.152 MHz clock signal, supplied to the associated LLC for synchronization of the two chips, is used for resynchronization of the received data. The Power Down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL and disables all circuits except the cable bias detectors at the TPB terminals. The port transmitter circuitry and the receiver circuitry are also disabled when the port is disabled, suspended, or disconnected.

The PDI1394P25 supports an optional isolation barrier between itself and its LLC. When the $\overline{\text{ISO}}$ input terminal is tied high, the LLC interface outputs behave normally. When the $\overline{\text{ISO}}$ terminal is tied low, internal differentiating logic is enabled, and the outputs are driven such that they can be coupled through a capacitive or transformer galvanic isolation barrier as described in *IEEE 1394a section 5.9.4*. To operate with single capacitor (bus holder) isolation,

the $\overline{\text{ISO}}$ on the PHY terminal must be tied high. For more details on using single capacitor isolation, please refer to the Philips Isolation Application Note AN2452.

Data bits to be transmitted through the cable ports are received from the LLC on two, four or eight parallel paths (depending on the requested transmission speed). They are latched internally in the PDI1394P25 in synchronization with the 49.152 MHz system clock. These bits are combined serially, encoded, and transmitted at 98.304/196.608/392.216 Mbps (referred to as S100, S200, and S400 speed, respectively) as the outbound data-strobe information stream. During transmission, the encoded data information is transmitted differentially on the TPB cable pair(s), and the encoded strobe information is transmitted differentially on the TPA cable pair(s).

During packet reception the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair, and the encoded strobe information is received on the TPB cable pair. The received data-strobe information is decoded to recover the receive clock signal and the serial data bits. The serial

data bits are split into two-, four- or eight-bit parallel streams (depending upon the indicated receive speed), resynchronized to the local 49.152 MHz system clock and sent to the associated LLC.

Both the TPA and TPB cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during arbitration to set the speed of the next packet transmission (speed signaling). In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the remotely supplied twisted-pair bias voltage (cable bias detection).

The PDI1394P25 provides a 1.86 V nominal bias voltage at the TPBIAS terminal for port termination. The PHY contains two independent TPBIAS circuits. This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. This bias voltage source must be stabilized by an external filter capacitor of $0.3 \mu\text{F} \pm 1 \mu\text{F}$.

The line drivers in the PDI1394P25 operate in a high-impedance current mode, and are designed to work with external 112Ω line-termination resistor networks in order to match the 110Ω cable impedance. One network is provided at each end of all twisted-pair cable connections. Each network is composed of a pair of series-connected 56Ω resistors. The midpoint of the pair of resistors that is directly connected to the twisted-pair A terminals is connected to its corresponding TPBIAS voltage terminal. The midpoint of the pair of resistors that is directly connected to the twisted-pair B terminals is coupled to ground through a parallel R-C network with recommended values of $5 \text{ k}\Omega$ and 220 pF . The values of the external line termination resistors are designed to meet the standard specifications when connected in parallel with the internal receiver circuits. An external resistor connected between the R0 and R1 terminals sets the driver output current, along with other internal operating currents. This current setting resistor has a value of $6.34 \text{ k}\Omega \pm 1\%$.

When the power supply of the PDI1394P25 is removed while the twisted-pair cables are connected, the PDI1394P25 transmitter and receiver circuitry presents a high impedance to the cable in order to not load the TPBIAS voltage on the other end of the cable.

The TEST0 and TEST1 terminals are used to set up various manufacturing test conditions. For normal operation, they should be connected to ground. TEST1 can also be tied through a $1 \text{ k}\Omega$ resistor to ground to accommodate other vendors' pin compatible chips.

The TESTM terminal is used to set up various manufacturing test conditions. For normal operation it should be tied to V_{DD} .

Four package terminals, used as inputs to set the default value for four configuration status bits in the self-ID packet, should be hard-wired high or low as a function of the equipment design. The PC0 \pm PC2 terminals are used to indicate the default power-class status for the node (the need for power from the cable or the ability to supply power to the cable). See Table 21 for power class encoding. The C/LKON terminal is used as an input to indicate that the node is a contender for bus manager.

The PHY supports suspend/resume as defined in the IEEE 1394a specification. The suspend mechanism allows pairs of directly connected ports to be placed into a low power state while maintaining a port-to-port connection between 1394 bus segments. While in a low power state, a port is unable to transmit or receive data transaction packets. However, a port in a low power state is

capable of detecting connection status changes and detecting incoming TPBIAS. When the PDI1394P25's port is suspended, all circuits except the bias-detection circuits are powered down, resulting in significant power savings. The TPBIAS circuit monitors the value of incoming TPA pair common-mode voltage when local TPBIAS is inactive. Because this circuit has an internal current source and the connected node has a current sink, the monitored value indicates the cable connection status. This monitor is called connect-detect.

Both the cable bias-detect monitor and TPBIAS connect-detect monitor are used in suspend/resume signaling and cable connection detection. For additional details of suspend/resume operation, refer to the 1394a specification. The use of suspend/resume is recommended for new designs.

The port transmitter and receiver circuitry is disabled during power down (when the PD input terminal is asserted high), during reset (when the RESET input terminal is asserted low), when no active cable is connected to the port, or when controlled by the internal arbitration logic. The port twisted-pair bias voltage circuitry is disabled during power down, during reset, or when the port is disabled as commanded by the LLC.

The CNA (cable-not-active) terminal provides a high when the twisted-pair cable port is not receiving incoming bias (i.e., it is either disconnected or suspended), and can be used along with LPS to determine when to power-down the PDI1394P25. The CNA output is not debounced. When the PD terminal is asserted high, the CNA detection circuitry is enabled (regardless of the previous state of the ports) and a pull-down is activated on the RESET terminal so as to force a reset of the PDI1394P25 internal logic.

The LPS (link power status) terminal works with the C/LKON terminal to manage the power usage in the node. The LPS signal from the LLC is used in conjunction with the LCtrl bit (see Table 1 and Table 2) to indicate the active/power status of the LLC. The LPS signal is also used to reset, disable, and initialize the PHY-LLC interface (the state of the PHY-LCC interface is controlled solely by the LPS input regardless of the state of the LCtrl bit).

The LPS input is considered inactive if it remains low for more than $2.6 \mu\text{s}$ and is considered active otherwise. When the PDI1394P25 detects that LPS is inactive, it will place the PHY-LLC interface into a low-power reset state in which the CTL and D outputs are held in the logic zero state and the LREQ input is ignored; however, the SYSCLK output remains active. If the LPS input remains low for more than $26 \mu\text{s}$, the PHY-LLC interface is put into a low-power disabled state in which the SYSCLK output is also held inactive. The PHY-LLC interface is also held in the disabled state during hardware reset. The PDI1394P25 will continue the necessary repeater functions required for normal network operation regardless of the state of the PHY-LLC interface. When the interface is in the reset or disabled state and LPS is again observed active, the PHY will initialize the interface and return it to normal operation.

The PHY uses the C/LKON terminal to notify the LLC to power up and become active. When activated, the C/LKON signal is a square wave of approximately 163 ns period. The PHY activates the C/LKON output when the LLC is inactive and a wake-up event occurs. The LLC is considered inactive when either the LPS input is inactive, as described above, or the LCtrl bit is cleared to 0. A wake-up event occurs when a link-on PHY packet addressed to this node is received, or conditionally when a PHY interrupt occurs. The PHY deasserts the C/LKON output when the LLC becomes active (both LPS active and the LCtrl bit set to 1). The PHY also deasserts

1394 enhanced AV link layer controller**PDI1394L40****1.0 FEATURES**

- IEEE1394a and IEEE1394–1995 Standard Link Layer Controller
- Hardware Support for the IEC61883 International Standard of Digital Interface for Consumer Electronics
- Interface to any IEEE 1394–1995 or 1394a Physical Layer Interface
- 5 V Tolerant I/Os
- Single 3.3 V supply voltage
- Full-duplex isochronous operation
- Operates with 400/200/100 Mbps physical layer devices
- 12K byte fully programmable FIFO pool for isochronous and asynchronous data
- Supports single capacitor isolation mode and IEEE 1394–1995, Annex J. isolation
- 6-field deep SYT buffer added to enhance real-time isochronous synchronization using the AVFSYNC pin
- Generates its own AV port clocks under software control. Select one of three frequencies: 24.576, 12.288, or 6.144 MHz
- On chip timer resources
- Flexible 8/16 bit multiplexed/non-multiplexed host interface
- Parallel AV interface

3.0 QUICK REFERENCE DATAGND = 0 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V _{DD}	Functional supply voltage range		3.0	3.3	3.6	V
I _{DD}	Supply current @ V _{DD} = 3.3 V	Operating		110	200	mA
SCLK	Device clock		49.147	49.152	49.157	MHz

4.0 ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
144-pin LQFP144	0 to +70 °C	PDI1394L40BE	PDI1394L40BE	SOT486-1

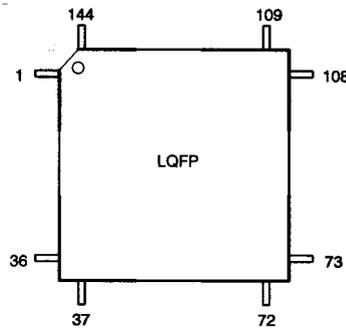
NOTE:

This datasheet is subject to change.
Please visit our internet website www.semiconductors.philips.com/1394 for latest changes.

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5.0 PIN CONFIGURATION



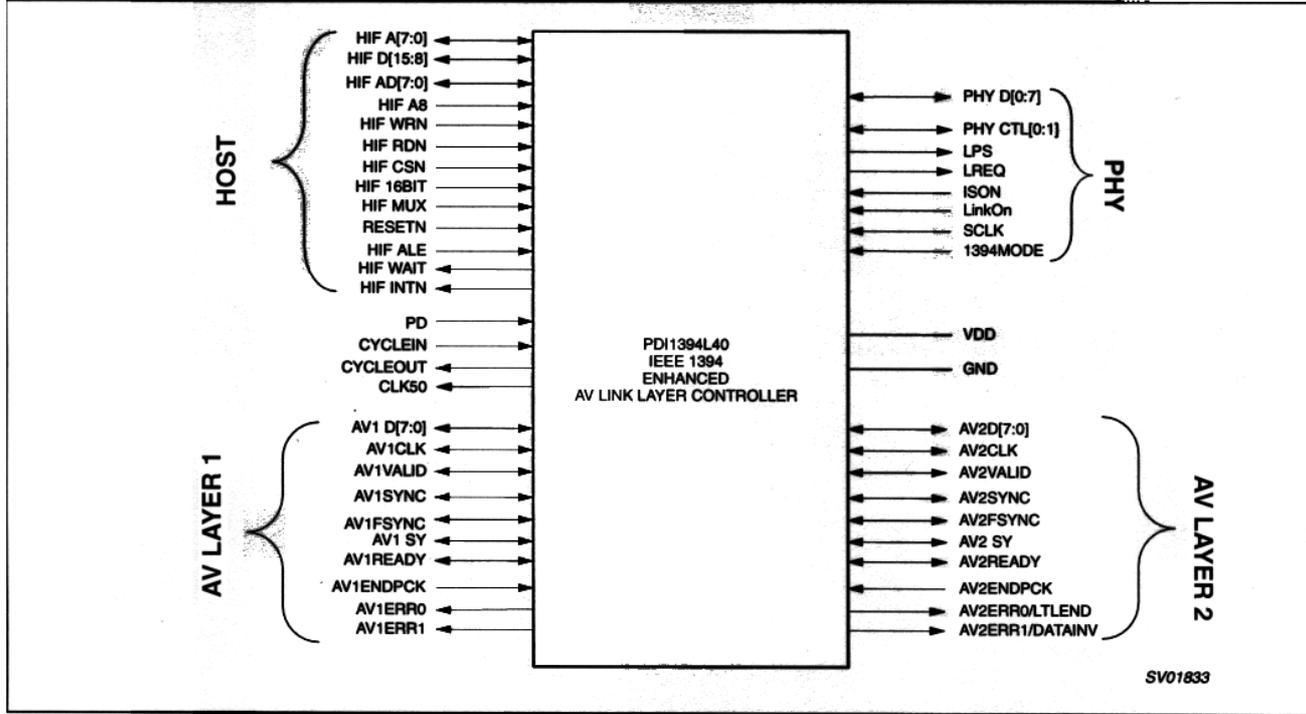
Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	HIF D15	37	HIF WRN	73	PHY D7*	109	AV1D1
2	HIF D14	38	HIF INTN	74	PHY D6*	110	AV1D2
3	HIF D13	39	HIF ALE	75	PHY D5*	111	AV1D3
4	HIF D12	40	HIF RDN	76	PHY D4*	112	GND
5	GND	41	HIF WAIT	77	GND	113	V _{DD}
6	V _{DD}	42	RESETN	78	V _{DD}	114	AV1D4
7	HIF D11	43	GND	79	PHY D3*	115	AV1D5
8	HIF D10	44	V _{DD}	80	PHY D2*	116	AV1D6
9	HIF D9	45	HIF 16BIT	81	PHY D1*	117	AV1D7
10	HIF D8	46	HIF MUX	82	PHY D0*	118	AV1READY
11	GND	47	1394 MODE	83	GND	119	GND
12	V _{DD}	48	PD	84	V _{DD}	120	V _{DD}
13	HIF AD7	49	RESERVED	85	PHY CTL1*	121	AV2ERR0/LTLEND
14	HIF AD6	50	RESERVED	86	PHY CTL0*	122	AV2ERR1/DATINV
15	HIF AD5	51	RESERVED	87	LREQ	123	AV2ENDPCK
16	HIF AD4	52	RESERVED	88	SCLK*	124	AV2CLK
17	GND	53	GND	89	GND	125	AV2FSYNC
18	V _{DD}	54	V _{DD}	90	V _{DD}	126	AV2 SY
19	HIF AD3	55	CLK50	91	LPS*	127	AV2VALID
20	HIF AD2	56	CYCLEIN	92	LINKON	128	AV2SYNC
21	HIF AD1	57	CYCLEOUT	93	ISON	129	RESERVED
22	HIF AD0	58	RESERVED	94	GND	130	RESERVED
23	GND	59	RESERVED	95	V _{DD}	131	GND
24	V _{DD}	60	GND	96	AV1ERR0	132	V _{DD}
25	HIF A8	61	V _{DD}	97	AV1ERR1	133	AV2D0
26	HIF A7	62	TESTPIN	98	AV1ENDPCK	134	AV2D1
27	HIF A6	63	TESTPIN	99	AV1CLK	135	AV2D2
28	HIF A5	64	TESTPIN	100	AV1FSYNC	136	AV2D3
29	HIF A4	65	RESERVED	101	AV1 SY	137	GND
30	HIF A3	66	RESERVED	102	AV1VALID	138	V _{DD}
31	HIF A2	67	RESERVED	103	AV1SYNC	139	AV2D4
32	HIF A1	68	RESERVED	104	RESERVED	140	AV2D5
33	HIF A0	69	GND	105	RESERVED	141	AV2D6
34	GND	70	V _{DD}	106	GND	142	AV2D7
35	V _{DD}	71	RESERVED	107	V _{DD}	143	AV2READY
36	HIF CSN	72	RESERVED	108	AV1D0	144	RESERVED

* Indicates pin equipped with internal bus hold circuit activated by the state of the ISON pin.

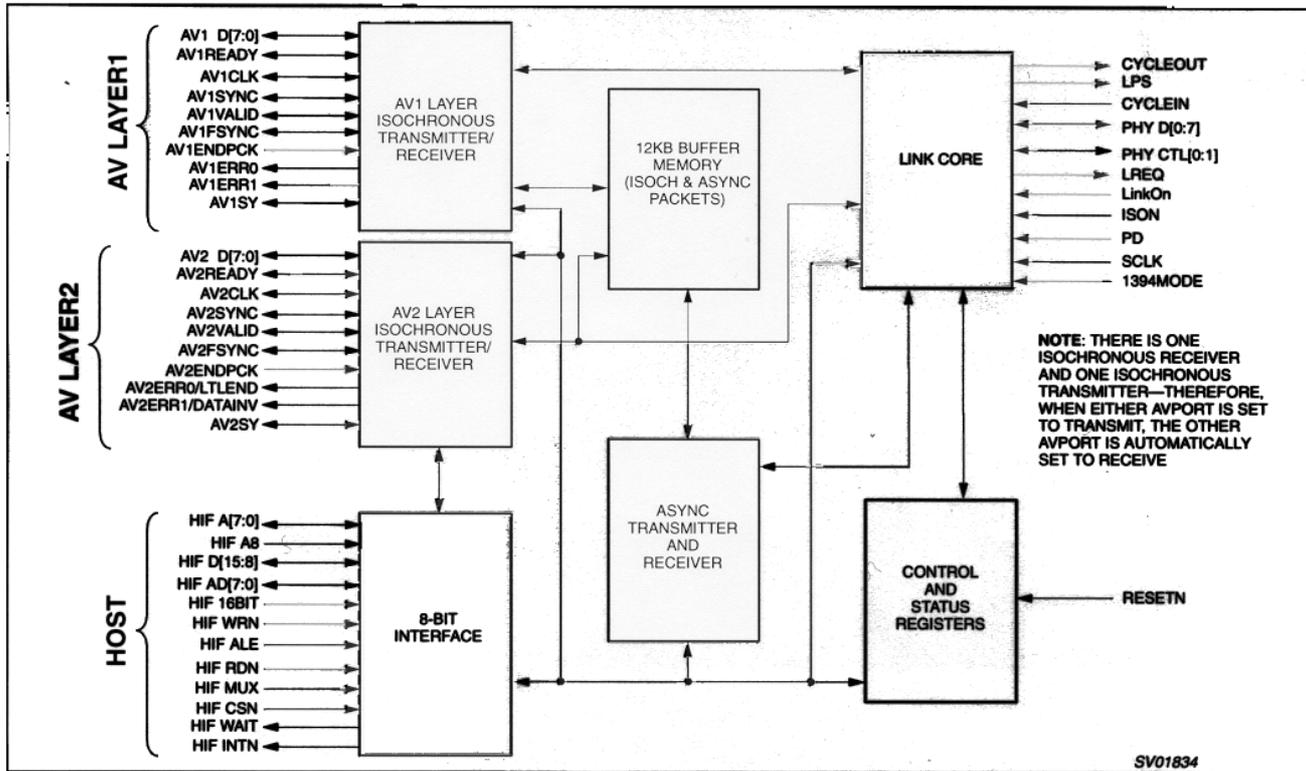
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6.0 FUNCTIONAL DIAGRAM



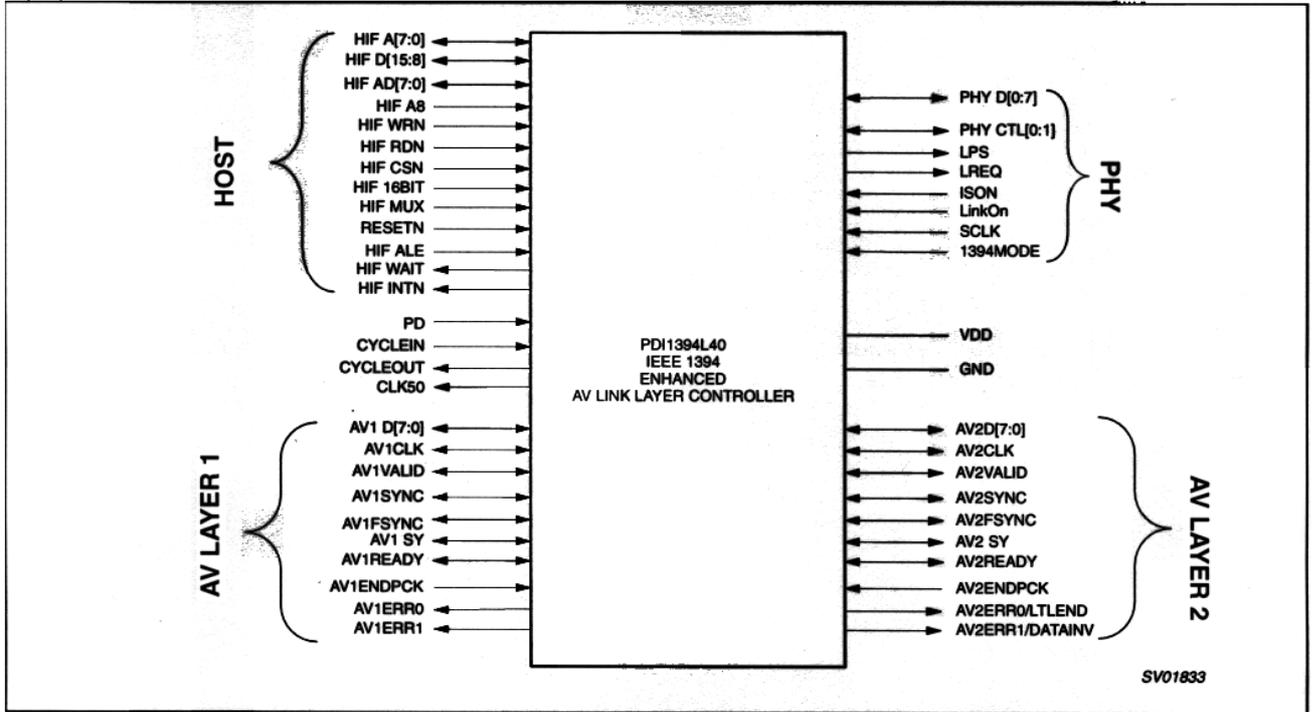
7.0 INTERNAL BLOCK DIAGRAM



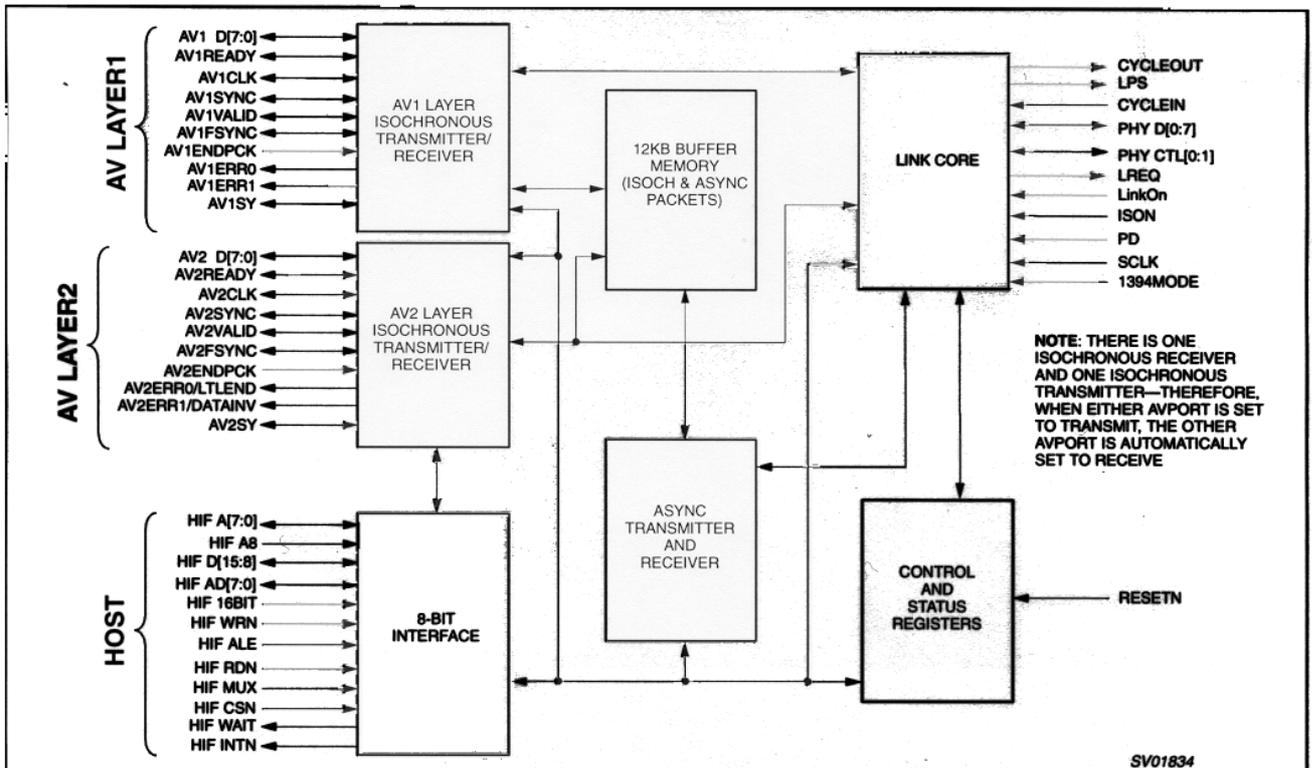
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6.0 FUNCTIONAL DIAGRAM



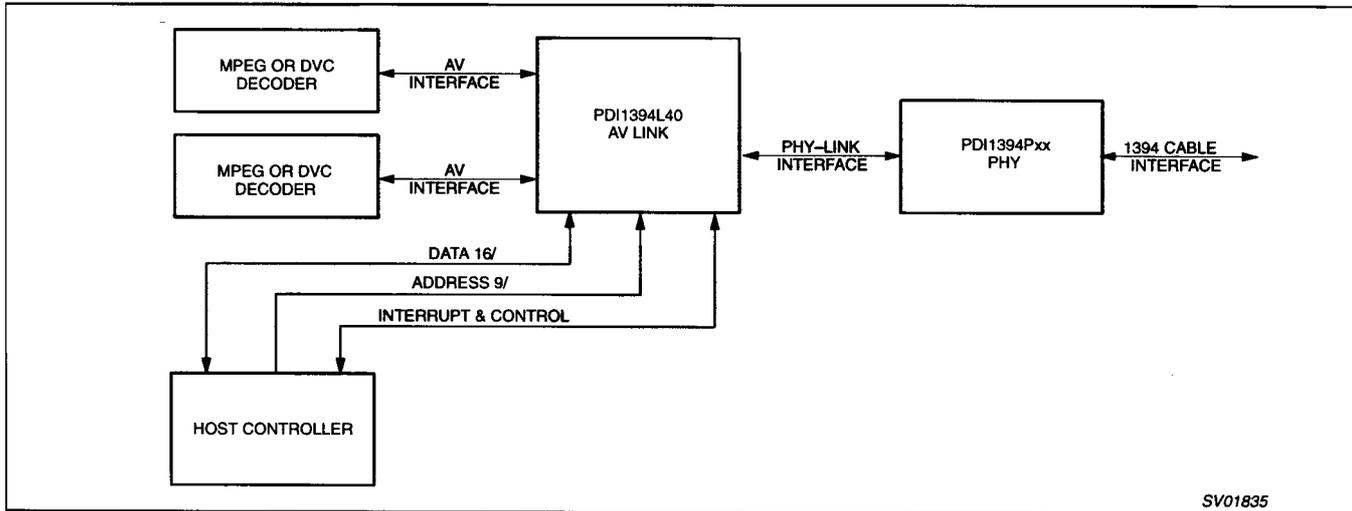
7.0 INTERNAL BLOCK DIAGRAM



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8.0 APPLICATION DIAGRAM



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9.0 PIN DESCRIPTION

9.1 Host Interface

PIN No.	PIN SYMBOL	I/O	NAME AND FUNCTION
13, 14, 15, 16, 19, 20, 21, 22	HIF AD[7:0]	I/O	Host Interface Data 7 (MSB) through 0. Byte wide data path to internal registers.
1, 2, 3, 4, 7, 8, 9, 10	HIF D[15:8]	I/O	Host Interface Data 15 (MSB) through 8. Only used in 16 bit access mode (HIF 16BIT = HIGH).
26, 27, 28, 29, 30, 31, 32, 33	HIF A[7:0]	I/O	Host Interface Address 0 through 8. Provides the host with a byte wide interface to internal registers. See description of Host Interface for addressing rules (Section 12.5).
25	HIF A8	I	Control bit used to indicate the first byte/word of a read function or the last byte/word of a write function so that the data quadlet is fetched or stored. See Section 12.5 for more information regarding the host interface.
36	HIF CSN	I	Chip Select (active LOW). Host bus control signal to enable access to the FIFO and control and status registers.
37	HIF WRN	I	Write enable. When asserted (LOW) in conjunction with HIF CSN, a write to the PDI1394L40 internal registers is requested. (NOTE: HIF WRN and HIF RDN : if these are both LOW in conjunction with HIF CSN, then a write cycle takes place. This can be used to connect CPUs, that use R/W_N line rather than separate RD_N and WR_N lines. In that case, connect the R/W_N line to the HIF WRN and tie HIF RDN LOW.)
38	HIF INTN	O	Interrupt (active LOW). Indicates a interrupt internal to the PDI1394L40. Read the General Interrupt Register for more information. This pin is open drain and requires a 1KΩ pull-up resistor.
39	HIF ALE	I	Address latch enable. Used in multiplex mode only.
40	HIF RDN	I	Read enable. When asserted (LOW) in conjunction with HIF CSN, a read of the PDI1394L40 internal registers is requested.
41	HIF WAIT	O	Wait signal. Signals Host interface in WAIT condition when HI. See Section 12.5.
42	RESETN	I	Reset (active LOW). The asynchronous master reset to the PDI1394L40.
45	HIF 16BIT	I	Host interface mode pin. When LOW HIF operates in 8 bit mode. When HIGH HIF operates in 16 bit mode.
46	HIF MUX	I	Host interface mode pin. When LOW HIF operates in non-multiplex mode, when HIGH HIF operates in multiplex mode. When HIGH, the low-order eight address bits are multiplexed with data on HIF AD[7:0], otherwise they are non-multiplexed and supplied on A[7:0].

1394 enhanced AV link layer controller

PDI1394L40

9.2 AV Interface 1

NOTE: This AV interface may be configured to transmit or receive according to the condition of "DIRAV1" bit in GLOBCSR register (0x018)—default is transmit.

PIN No.	PIN SYMBOL	I/O	NAME AND FUNCTION
96	AV1ERR0	O	CRC error. Indicates bus packet delivered on AV1 D[7:0] had a CRC error; the current AV packet is unreliable.
97	AV1ERR1	O	Sequence Error. Indicates at least one source packet was lost before the current AV1 D [7:0] data.
98	AV1ENDPCK	I	End of application packet indication from data source. Required only if input packet is not multiple of 4 bytes. It can be tied LOW for data packets that are 4*N in size.
99	AV1CLK	I/O	External application clock. Rising edge active. This pin can be programmed to be an output and the application clock. Depending on the configuration of AV Port 1 as transmitter or receiver, the output enable is located in the ITXPKCTL register (address 0x020) or IRXPKCTL register (address 0x040).
100	AV1FSYNC	I/O	Programmable frame sync, is set to input when AV interface 1 is a transmitter and to output when the interface is configured as a receiver. When the pin is an input, it is used to designate a frame of data for Digital Video (DV). The signal is time stamped and transmitted in the SYT field of ITXHQ2. When set to an output, the signal is derived from SYT field of IRXHQ2.
101	AV1 SY	I/O	SY Value. When port AV1 is configured as a transmitter, this pin is an input. When the AV port is configured to as a receiver, the pin is an output. See the description for bit 0 of the ITXCTL (0x034) and IRXCTL (0x054) registers.
102	AV1VALID	I/O	Indicates data on AV1 D [7:0] is valid.
103	AV1SYNC	I/O	Indicates that the data currently being clocked by the source under the condition of AV1VALID is the start of an application packet. If the AV interface is configured as a receiver, then it will assert AV1SYNC when an application packet becomes available and persist until the first data of the packet is clocked out. Thus, AV1VALID may last for more than one cycle, but for exactly one cycle in which AV1VALID is asserted.
117, 116, 115, 114, 111, 110, 109, 108	AV1 D[7:0]	I/O	Audio/Video Data 7 (MSB) through 1. Part of byte-wide interface to the AV layer 1.
118	AV1READY	I	When the AV port is configured as a receiver, this pin is an input. This is a flow control signal that allows the application to indicate whether it is able to accept data flowing across AV Interface 1. The AV interface responds to an inactive AV1READY by not asserting AV1VALID, and thereby withholding data from the application. The AV1READY signal is processed through one level of pipelining, which means that the AV Link will accept data on the cycle in which AV1READY is de-asserted and will not accept data on the cycle in which AV1READY is asserted.
		O	When the AV port is configured to transmit, this pin is an output. This is a flow control signal that allows the link chip to indicate whether it is able to accept data flowing across AV Interface 1. The source of data, an external entity, responds to an inactive AV1READY by not asserting AV1VALID, and thereby withholding data. The AV1READY signal should be processed by the sink through one level of pipelining, which means that the receiver must be able to accept data on the cycle in which AV1READY is de-asserted. The receiving interface does not have to accept data on the cycle in which AV1READY is asserted.

1394 enhanced AV link layer controller

PDI1394L40

9.3 AV Interface 2

NOTE: This AV interface may be configured to transmit or receive according to the condition of "DIRAV1" bit in GLOBCSR register—default is receive.

PIN No.	PIN SYMBOL	I/O	NAME AND FUNCTION
121	AV2ERR0/ LTLEND	I/O	CRC error, indicates bus packet containing AV2 D [7:0] had a CRC error, the current AV packet is unreliable. This pin is also used to input the mode of LTLEND (Little Endian) bit after a chip reset. An appropriate pull-up or pull-down resistor (22 kΩ recommended) should be connected to place the pin in the desired state during reset. Please see details related to use of the LTLEND bit in the "Host Interface" section (of the datasheet (Section 12.5)).
122	AV2ERR1/ DATINV	I/O	Sequence Error. Indicates at least one source packet was lost before the current AV2 D [7:0] data. This pin is also used to input the mode of DATINV (Data Invariant) bit after a chip reset. An appropriate pull-up or pull-down resistor (22 kΩ recommended) should be connected to place the pin in the desired state during reset. Please see details related to use of the DATINV bit in the "Host Interface" section (of the datasheet (Section 12.5)).
123	AV2ENDPCK	I	End of application packet indication from data source. Required only if input packet is not multiple of 4 bytes. It can be tied LOW for data packets that are 4*N in size.
124	AV2CLK	I/O	External application clock. Rising edge active. This pin can be programmed to be an output and the application clock. Depending on the configuration of AV Port 2 as transmitter or receiver, the output enable is located in the ITXPCTL register (address 0x020) or IRXPCTL register (address 0x040).
125	AV2FSYNC	I/O	Programmable frame sync, is set to input when AV interface 2 is a transmitter, and to output when the interface is configured as a receiver. When the pin is an input, it is used to designate a frame of data for Digital Video (DV). The signal is time stamped and transmitted in the SYT field of ITXHQ2. When set to an output, the signal is derived from SYT field of IRXHQ2.
126	AV2 SY	I/O	SY Value: When port AV2 is configured as a transmitter, this pin is an input. When the AV port is configured to as a receiver, the pin is an output. See the description for bit 0 of the ITXCTL (0x034) and IRXCTL (0x054) registers.
127	AV2VALID	I/O	Indicates data on AV2 D [7:0] is valid.
128	AV2SYNC	I/O	Indicates that the data currently being clocked by the source under the condition of AV2VALID is the start of an application packet. If the AV interface is configured as a receiver, then it will assert AV2SYNC when an application packet becomes available and persist until the first data of the packet is clocked out. Thus, AV2VALID may last for more than one cycle, but for exactly one cycle in which AV2VALID is asserted.
142, 141, 140, 139, 136, 135, 134, 133	AV2 D[7:0]	I/O	Audio/Video Data 7 (MSB) through 0. Part of byte-wide interface to the AV layer 2.
143	AV2READY	I	When the AV port is configured as a receiver, this pin is an input. This is a flow control signal that allows the application to indicate whether it is able to accept data flowing across AV Interface 2. The AV interface responds to an inactive AV2READY by not asserting AV2VALID, and thereby withholding data from the application. The AV2READY signal is processed through one level of pipelining, which means that the AV Link will accept data on the cycle in which AV2READY is de-asserted and will not accept data on the cycle in which AV2READY is asserted.
		O	When the AV port is configured to transmit, this pin is an output. This is a flow control signal that allows the link chip to indicate whether it is able to accept data flowing across AV Interface 2. The source of data, and external entity, responds to an inactive AV2READY by not asserting AV2VALID, and thereby withholding data. The AV2READY signal should be processed by the sink through one level of pipelining, which means that the receiver must be able to accept data on the cycle in which AV2READY is de-asserted. The receiving interface does not have to accept data on the cycle in which AV2READY is asserted.

1394 enhanced AV link layer controller

PDI1394L40

9.4 Phy Interface

PIN No.	PIN SYMBOL	I/O	NAME AND FUNCTION
82, 81, 80, 79, 76, 75, 74, 73	PHY D[0:7]	I/O	Data 0 (MSB) through 7 (NOTE: To preserve compatibility to the specified Link-Phy interface of the IEEE 1394–1995 standard, Annex J, bit 0 is the most significant bit). Data is expected on AV D[0:1] for 100Mb/s, AV D[0:3] for 200Mb/s, and AV D[0:7] for 400Mb/s. See IEEE 1394–1995 standard, Annex J for more information.
86, 85	PHY CTL[0:1]	I/O	Control Lines between Link and Phy. See 1394 Specification for more information.
47	1394 MODE	I	1394–1995 Annex J PHY (HIGH), or 1394a PHY (LOW)
87	LREQ	O	Link Request. Bus request to access the PHY. See IEEE 1394–1995 standard, Annex J for more information. (Used to request arbitration or read/write PHY registers).
88	SCLK	I	System clock. 49.152MHz input from the PHY (the PHY-LINK interface operates at this frequency).
91	LPS	O	Link power status. Outputs a frequency (typically 1.4 MHz) with 25% duty cycle which tells the PHY chip that the L40 is active.
92	LINKON	I	L40 generates a host interrupt when this pin receives a link on signal from the PHY. Interrupt is a request from another node for the L40 to be powered up (see PD pin).
93	ISON	I	Isolation mode. This pin is asserted (LOW) when an Annex J type isolation barrier is used. See IEEE 1394–1995 Annex J. for more information. When tied HIGH, this pin enables internal bushold circuitry on the affected PHY interface pins (see below). Active bushold circuits allow either the direct connection to PHY pins or the use of the single capacitor isolation mode.

9.5 Other Pins

PIN No.	PIN SYMBOL	I/O	NAME AND FUNCTION
5, 11, 17, 23, 34, 43, 53, 60, 69, 77, 83, 89, 94, 106, 112, 119, 131, 137	GND		Ground reference
6, 12, 18, 24, 35, 44, 54, 61, 70, 78, 84, 90, 95, 107, 113, 120, 132, 138	V _{DD}		3.3 V ± 0.3 V power supply
48	PD _{1,2,3,4}	I	Power Down. When asserted (high), the AV Link goes into a low power mode and de-asserts the LPS pin. When in this state, reads and writes to the registers are not allowed. The AV Link will resume operation when PD is de-asserted (low), all register settings and configurations are restored to their pre power down values.
49, 50, 51, 52, 58, 59, 65, 66, 67, 68, 71, 72, 104, 105, 129, 130, 144	RESERVED	NA	These pins are reserved for factory testing. For normal operation they should be connected to ground.
55	CLK50	O	Auxiliary clock, value is SCLK (usually 49.152 MHz)
56	CYCLEIN	I	Provides the capability to supply an external cycle timer signal for the beginning of 1394 bus cycles.
57	CYCLEOUT	O	Reproduces the 8kHz cycle clock of the cycle master.
62, 63, 64	TESTPIN		Test pins. These signals must be connected to ground.

NOTES:

Before asserting the RPL bit, SWPD or setting the PD pin high, the user should assure that the link chip is in the following state of operation:

1. The isochronous transmit FIFO is not receiving data for transmission
2. The isochronous transmitter is disabled
3. No asynchronous packets are being generated for transmission
4. Both the ASYNC request and response queues are empty

80C51 8-bit Flash microcontroller family 16KB/32KB/64KB ISP/IAP Flash with 512B/512B/1KB RAM

P89C51RB2/P89C51RC2/ P89C51RD2

DESCRIPTION

The P89C51RB2/RC2/RD2 device contains a non-volatile 16kB/32kB/64kB Flash program memory that is both parallel programmable and serial In-System and In-Application Programmable. In-System Programming (ISP) allows the user to download new code while the microcontroller sits in the application. In-Application Programming (IAP) means that the microcontroller fetches new program code and reprograms itself while in the system. This allows for remote programming over a modem link. A default serial loader (boot loader) program in ROM allows serial In-System programming of the Flash memory via the UART without the need for a loader in the Flash code. For In-Application Programming, the user program erases and reprograms the Flash memory by use of standard routines contained in ROM.

This device executes one machine cycle in 6 clock cycles, hence providing twice the speed of a conventional 80C51. An OTP configuration bit lets the user select conventional 12 clock timing if desired.

This device is a Single-Chip 8-Bit Microcontroller manufactured in advanced CMOS process and is a derivative of the 80C51 microcontroller family. The instruction set is 100% compatible with the 80C51 instruction set.

The device also has four 8-bit I/O ports, three 16-bit timer/event counters, a multi-source, four-priority-level, nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits.

The added features of the P89C51RB2/RC2/RD2 makes it a powerful microcontroller for applications that require pulse width modulation, high-speed I/O and up/down counting capabilities such as motor control.

FEATURES

- 80C51 Central Processing Unit
- On-chip Flash Program Memory with In-System Programming (ISP) and In-Application Programming (IAP) capability
- Boot ROM contains low level Flash programming routines for downloading via the UART
- Can be programmed by the end-user application (IAP)
- 6 clocks per machine cycle operation (standard)
- 12 clocks per machine cycle operation (optional)
- Speed up to 20 MHz with 6 clock cycles per machine cycle (40 MHz equivalent performance); up to 33 MHz with 12 clocks per machine cycle
- Fully static operation
- RAM expandable externally to 64 kB
- 4 level priority interrupt
- 7 interrupt sources
- Four 8-bit I/O ports
- Full-duplex enhanced UART
 - ± Framing error detection
 - ± Automatic address recognition
- Power control modes
 - ± Clock can be stopped and resumed
 - ± Idle mode
 - ± Power down mode
- Programmable clock out
- Second DPTR register
- Asynchronous port reset
- Low EMI (inhibit ALE)
- Programmable Counter Array (PCA)
 - ± PWM
 - ± Capture/compare

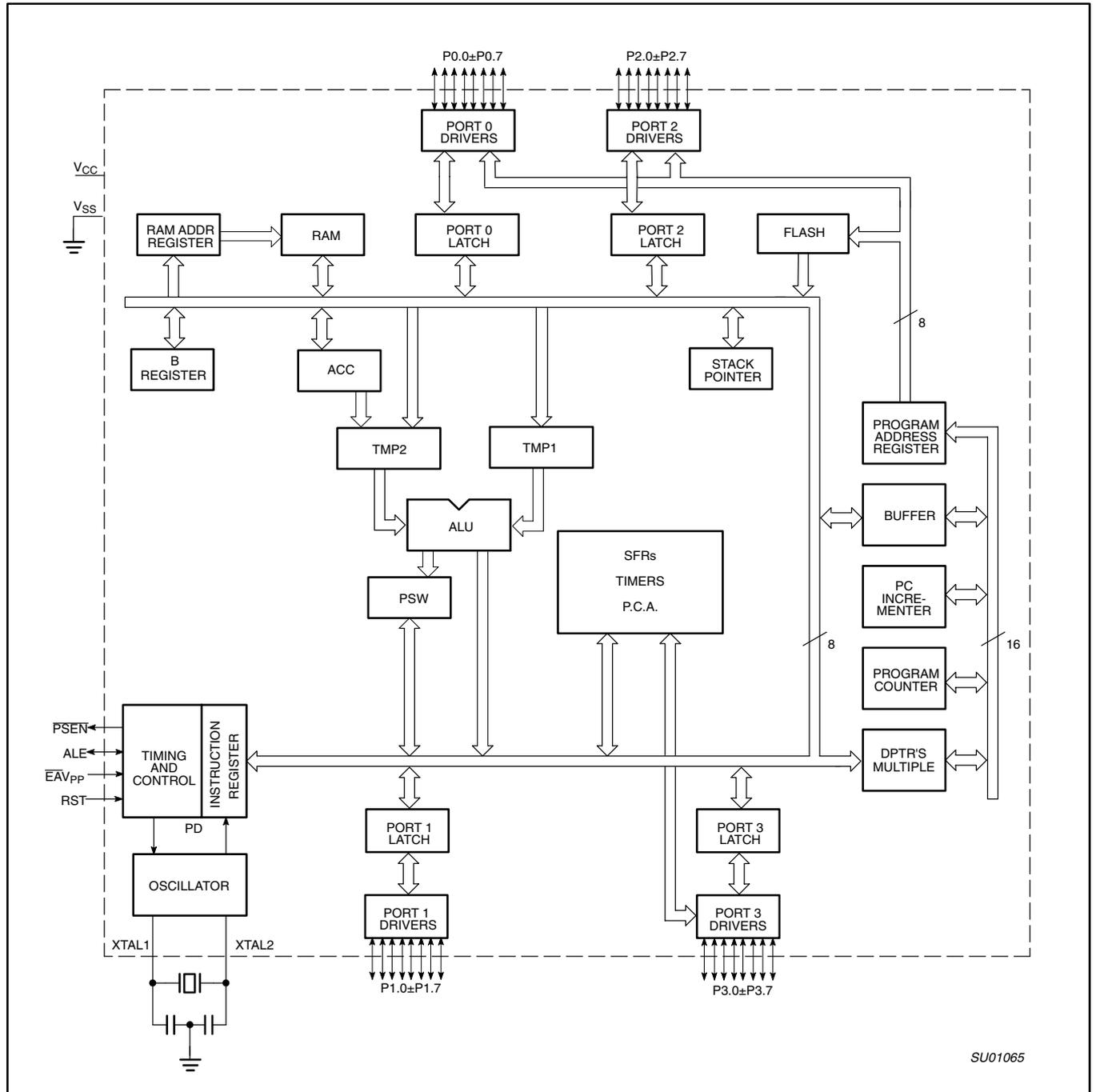
80C51 8-bit Flash microcontroller family

16KB/32KB/64KB ISP/IAP Flash with 512B/512B/1KB RAM

P89C51RB2/P89C51RC2/

P89C51RD2

BLOCK DIAGRAM

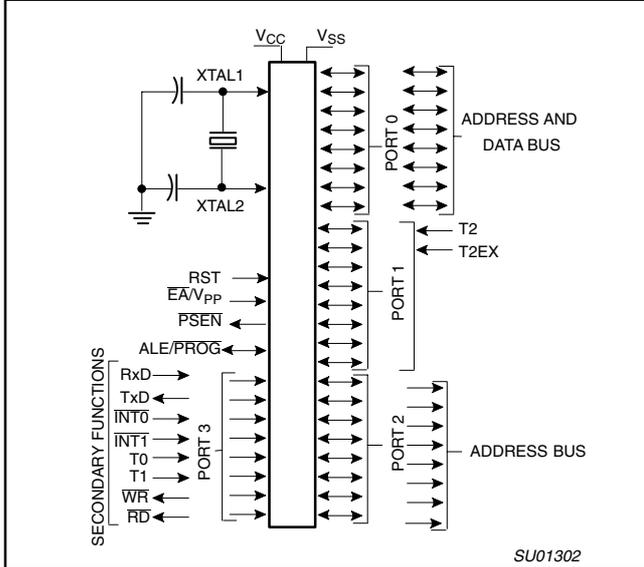


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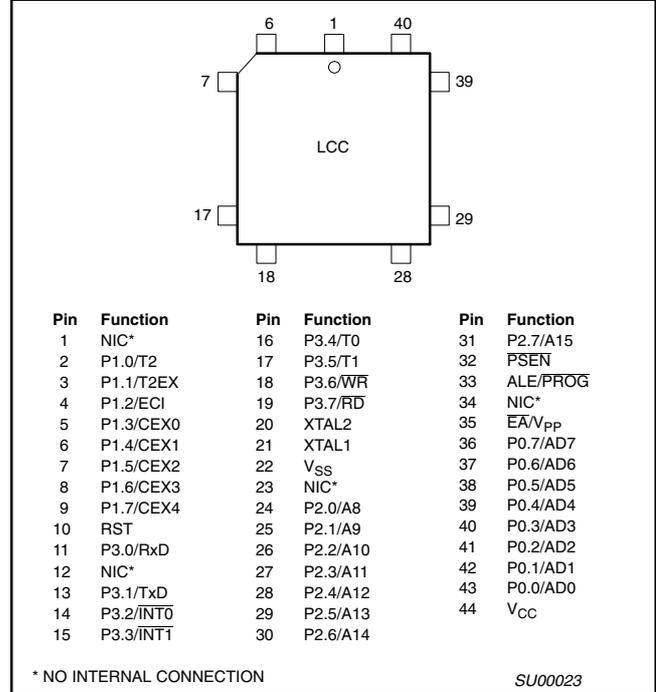
80C51 8-bit Flash microcontroller family
16KB/32KB/64KB ISP/IAP Flash with 512B/512B/1KB RAM

P89C51RB2/P89C51RC2/
P89C51RD2

LOGIC SYMBOL

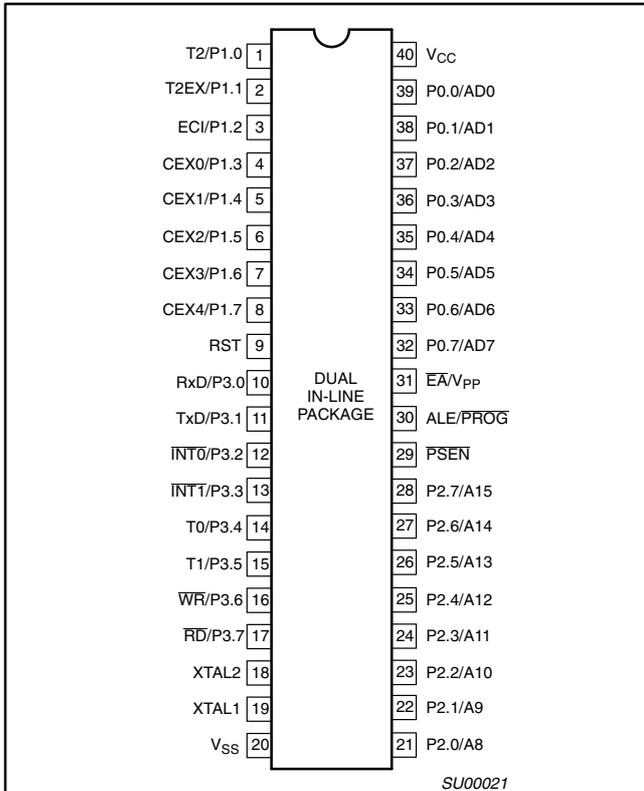


Plastic Leaded Chip Carrier

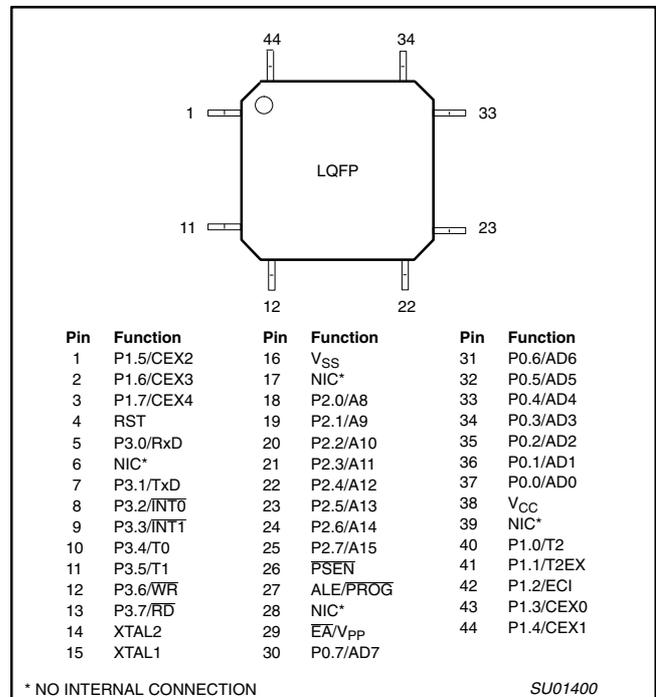


PINNING

Plastic Dual In-Line Package



Plastic Quad Flat Pack



80C51 8-bit Flash microcontroller family
16KB/32KB/64KB ISP/IAP Flash with 512B/512B/1KB RAM

P89C51RB2/P89C51RC2/
P89C51RD2

PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	PDIP	PLCC	LQFP		
V _{SS}	20	22	16	I	Ground: 0 V reference.
V _{CC}	40	44	38	I	Power Supply: This is the power supply voltage for normal, idle, and power-down operation.
P0.0±0.7	39±32	43±36	37±30	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.
P1.0±P1.7	1±8	2±9	40±44, 1±3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups on all pins except P1.6 and P1.7 which are open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}).
	1	2	40	I/O	Alternate functions for 89C51RB2/RC2/RD2 Port 1 include: T2 (P1.0): Timer/Counter 2 external count input/Clockout (see Programmable Clock-Out)
	2	3	41	I	T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction Control
	3	4	42	I	ECI (P1.2): External Clock Input to the PCA
	4	5	43	I/O	CEX0 (P1.3): Capture/Compare External I/O for PCA module 0
	5	6	44	I/O	CEX1 (P1.4): Capture/Compare External I/O for PCA module 1
	6	7	1	I/O	CEX2 (P1.5): Capture/Compare External I/O for PCA module 2
	7	8	2	I/O	CEX3 (P1.6): Capture/Compare External I/O for PCA module 3
	8	9	3	I/O	CEX4 (P1.7): Capture/Compare External I/O for PCA module 4
P2.0±P2.7	21±28	24±31	18±25	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register. P2.7 must be a ¹ to program and erase the device.
P3.0±P3.7	10±17	11, 13±19	5, 7±13	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 3 also serves the special features of the 89C51RB2/RC2/RD2, as listed below:
	10	11	5	I	RxD (P3.0): Serial input port
	11	13	7	O	TxD (P3.1): Serial output port
	12	14	8	I	INT0 (P3.2): External interrupt
	13	15	9	I	INT1 (P3.3): External interrupt
	14	16	10	I	T0 (P3.4): Timer 0 external input
	15	17	11	I	T1 (P3.5): Timer 1 external input
	16	18	12	O	WR (P3.6): External data memory write strobe
	17	19	13	O	RD (P3.7): External data memory read strobe
RST	9	10	4	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal resistor to V _{SS} permits a power-on reset using only an external capacitor to V _{CC} .
ALE	30	33	27	O	Address Latch Enable: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted twice every machine cycle, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. ALE can be disabled by setting SFR auxiliary.0. With this bit set, ALE will be active only during a MOVX instruction.

80C51 8-bit Flash microcontroller family
16KB/32KB/64KB ISP/IAP Flash with 512B/512B/1KB RAM

P89C51RB2/P89C51RC2/
P89C51RD2

MNEMONIC	PIN NUMBER			TYPE	NAME AND FUNCTION
	PDIP	PLCC	LQFP		
PSEN	29	32	26	O	Program Store Enable: The read strobe to external program memory. When executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
$\overline{\text{EA}}/V_{\text{PP}}$	31	35	29	I	External Access Enable/Programming Supply Voltage: $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations. If $\overline{\text{EA}}$ is held high, the device executes from internal program memory. The value on the $\overline{\text{EA}}$ pin is latched when RST is released and any subsequent changes have no effect. This pin also receives the programming supply voltage (V_{PP}) during Flash programming.
XTAL1	19	21	15	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	Crystal 2: Output from the inverting oscillator amplifier.

NOTE:
To avoid latch-up effect at power-on, the voltage on any pin (other than V_{PP}) must not be higher than $V_{\text{CC}} + 0.5 \text{ V}$ or less than $V_{\text{SS}} \pm 0.5 \text{ V}$.



Spartan and Spartan-XL Families Field Programmable Gate Arrays

DS060 (v1.6) September 19, 2001

Product Specification

Introduction

The Spartan™ and the Spartan-XL families are a high-volume production FPGA solution that delivers all the key requirements for ASIC replacement up to 40,000 gates. These requirements include high performance, on-chip RAM, core solutions and prices that, in high volume, approach and in many cases are equivalent to mask programmed ASIC devices.

The Spartan series is the result of more than 14 years of FPGA design experience and feedback from thousands of customers. By streamlining the Spartan series feature set, leveraging advanced process technologies and focusing on total cost management, the Spartan series delivers the key features required by ASIC and other high-volume logic users while avoiding the initial cost, long development cycles and inherent risk of conventional ASICs. The Spartan and Spartan-XL families in the Spartan series have ten members, as shown in Table 1.

Spartan and Spartan-XL Features

Note: The Spartan series devices described in this data sheet include the 5V Spartan family and the 3.3V Spartan-XL family. See the separate data sheet for the 2.5V Spartan-II family.

- First ASIC replacement FPGA for high-volume production with on-chip RAM
- Density up to 1862 logic cells or 40,000 system gates
- Streamlined feature set based on XC4000 architecture
- System performance beyond 80 MHz
- Broad set of AllianceCORE™ and LogiCORE™ predefined solutions available
- Unlimited reprogrammability
- Low cost

- System level features
 - Available in both 5V and 3.3V versions
 - On-chip SelectRAM™ memory
 - Fully PCI compliant
 - Full readback capability for program verification and internal node observability
 - Dedicated high-speed carry logic
 - Internal 3-state bus capability
 - Eight global low-skew clock or signal networks
 - IEEE 1149.1-compatible Boundary Scan logic
 - Low cost plastic packages available in all densities
 - Footprint compatibility in common packages
- Fully supported by powerful Xilinx development system
 - Foundation Series: Integrated, shrink-wrap software
 - Alliance Series: Dozens of PC and workstation third party development systems supported
 - Fully automatic mapping, placement and routing

Additional Spartan-XL Features

- 3.3V supply for low power with 5V tolerant I/Os
- Power down input
- Higher performance
- Faster carry logic
- More flexible high-speed clock network
- Latch capability in Configurable Logic Blocks
- Input fast capture latch
- Optional mux or 2-input function generator on outputs
- 12 mA or 24 mA output drive
- 5V and 3.3V PCI compliant
- Enhanced Boundary Scan
- Express Mode configuration
- Chip scale packaging

Table 1: Spartan and Spartan-XL Field Programmable Gate Arrays

Device	Logic Cells	Max System Gates	Typical Gate Range (Logic and RAM) ⁽¹⁾	CLB Matrix	Total CLBs	No. of Flip-flops	Max. Avail. User I/O	Total Distributed RAM Bits
XCS05 and XCS05XL	238	5,000	2,000-5,000	10 x 10	100	360	77	3,200
XCS10 and XCS10XL	466	10,000	3,000-10,000	14 x 14	196	616	112	6,272
XCS20 and XCS20XL	950	20,000	7,000-20,000	20 x 20	400	1,120	160	12,800
XCS30 and XCS30XL	1368	30,000	10,000-30,000	24 x 24	576	1,536	192	18,432
XCS40 and XCS40XL	1862	40,000	13,000-40,000	28 x 28	784	2,016	224	25,088

Notes:

1. Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

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Spartan and Spartan-XL Families Field Programmable Gate Arrays

General Overview

Spartan series FPGAs are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources (routing channels), and surrounded by a perimeter of programmable Input/Output Blocks (IOBs), as seen in Figure 1. They have generous routing resources to accommodate the most complex interconnect patterns.

The devices are customized by loading configuration data into internal static memory cells. Re-programming is possible an unlimited number of times. The values stored in these

memory cells determine the logic functions and interconnections implemented in the FPGA. The FPGA can either actively read its configuration data from an external serial PROM (Master Serial mode), or the configuration data can be written into the FPGA from an external device (Slave Serial mode).

Spartan series FPGAs can be used where hardware must be adapted to different user applications. FPGAs are ideal for shortening design and development cycles, and also offer a cost-effective solution for production rates well beyond 50,000 systems per month.

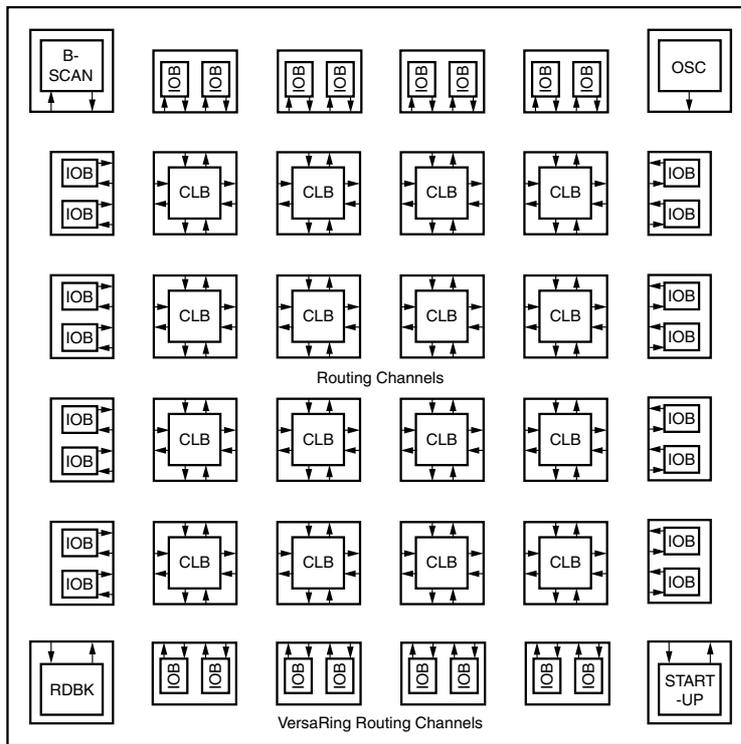


Figure 1: Basic FPGA Block Diagram

Pin Descriptions

There are three types of pins in the Spartan/XL devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated with the I/O pull-up resistor network activated. After configuration, if an IOB is unused it is configured as an input with the I/O pull-up resistor network remaining activated.

Any user I/O can be configured to drive the Global Set/Reset net GSR or the global three-state net GTS. See **Global Signals: GSR and GTS**, page 20 for more information.

Device pins for Spartan/XL devices are described in **Table 18**.

Table 18: Pin Descriptions

Pin Name	I/O During Config.	I/O After Config.	Pin Description
Permanently Dedicated Pins			
V _{CC}	X	X	Eight or more (depending on package) connections to the nominal +5V supply voltage (+3.3V for Spartan-XL devices). All must be connected, and each must be decoupled with a 0.01 –0.1 μF capacitor to Ground.
GND	X	X	Eight or more (depending on package type) connections to Ground. All must be connected.
CCLK	I or O	I	During configuration, Configuration Clock (CCLK) is an output in Master mode and is an input in Slave mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High or Low time restriction on Spartan/XL devices, except during Readback. See Violating the Maximum High and Low Time Specification for the Readback Clock , page 39 for an explanation of this exception.
DONE	I/O	O	DONE is a bidirectional signal with an optional internal pull-up resistor. As an open-drain output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs. The optional pull-up resistor is selected as an option in the program that creates the configuration bitstream. The resistor is included by default.
PROGRAM	I	I	PROGRAM is an active Low input that forces the FPGA to clear its configuration memory. It is used to initiate a configuration cycle. When PROGRAM goes High, the FPGA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases INIT. The PROGRAM pin has a permanent weak pull-up, so it need not be externally pulled up to VCC.
MODE (Spartan) M0, M1 (Spartan-XL)	I	X	The Mode input(s) are sampled after INIT goes High to determine the configuration mode to be used. During configuration, these pins have a weak pull-up resistor. For the most popular configuration mode, Slave Serial, the mode pins can be left unconnected. For Master Serial mode, connect the Mode/M0 pin directly to system ground.



Table 18: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
PWRDWN	I	I	PWRDWN is an active Low input that forces the FPGA into the Power Down state and reduces power consumption. When PWRDWN is Low, the FPGA disables all I/O and initializes all flip-flops. All inputs are interpreted as Low independent of their actual level. VCC must be maintained, and the configuration data is maintained. PWRDWN halts configuration if asserted before or during configuration, and re-starts configuration when removed. When PWRDWN returns High, the FPGA becomes operational by first enabling the inputs and flip-flops and then enabling the outputs. PWRDWN has a default internal pull-up resistor.
User I/O Pins That Can Have Special Functions			
TDO	O	O	If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed. To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used.
TDI, TCK, TMS	I	I/O or I (JTAG)	If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively. They come directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed. If the BSCAN symbol is not placed in the design, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O. In this case, they must be called out by special library elements. To use these pins, place the library components TDI, TCK, and TMS instead of the usual pad symbols. Input or output buffers must still be used.
HDC	O	I/O	High During Configuration (HDC) is driven High until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, HDC is a user-programmable I/O pin.
$\overline{\text{LDC}}$	O	I/O	Low During Configuration ($\overline{\text{LDC}}$) is driven Low until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, $\overline{\text{LDC}}$ is a user-programmable I/O pin.
$\overline{\text{INIT}}$	I/O	I/O	Before and during configuration, $\overline{\text{INIT}}$ is a bidirectional signal. A 1 k Ω to 10 k Ω external pull-up resistor is recommended. As an active Low open-drain output, $\overline{\text{INIT}}$ is held Low during the power stabilization and internal clearing of the configuration memory. As an active Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 μs after $\overline{\text{INIT}}$ has gone High. During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O go active, $\overline{\text{INIT}}$ is a user-programmable I/O pin.
PGCK1 - PGCK4 (Spartan)	Weak Pull-up	I or I/O	Four Primary Global inputs each drive a dedicated internal global net with short delay and minimal skew. If not used to drive a global buffer, any of these pins is a user-programmable I/O. The PGCK1-PGCK4 pins drive the four Primary Global Buffers. Any input pad symbol connected directly to the input of a BUFGP symbol is automatically placed on one of these pins.

Spartan and Spartan-XL Families Field Programmable Gate Arrays



Table 18: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
SGCK1 - SGCK4 (Spartan)	Weak Pull-up (except SGCK4 is DOUT)	I or I/O	Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGS symbol is automatically placed on one of these pins.
GCK1 - GCK8 (Spartan-XL)	Weak Pull-up (except GCK6 is DOUT)	I or I/O	Eight Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The GCK1-GCK8 pins provide the shortest path to the eight Global Low-Skew Buffers. Any input pad symbol connected directly to the input of a BUFGLS symbol is automatically placed on one of these pins.
CS1 (Spartan-XL)	I	I/O	During Express configuration, CS1 is used as a serial-enable signal for daisy-chaining.
D0-D7 (Spartan-XL)	I	I/O	During Express configuration, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.
DIN	I	I/O	During Slave Serial or Master Serial configuration, DIN is the serial configuration data input receiving data on the rising edge of CCLK. After configuration, DIN is a user-programmable I/O pin.
DOUT	O	I/O	During Slave Serial or Master Serial configuration, DOUT is the serial configuration data output that can drive the DIN of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input. In Spartan-XL Express mode, DOUT is the status output that can drive the CS1 of daisy-chained FPGAs, to enable and disable downstream devices. After configuration, DOUT is a user-programmable I/O pin.
Unrestricted User-Programmable I/O Pins			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor network that defines the logic level as High.

CY2071A

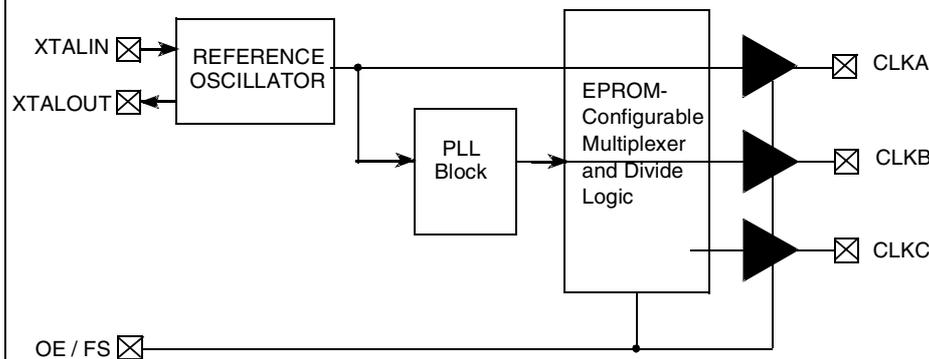
EPROM Programmable Clock Generator

Features	Benefits
Single phase-locked loop architecture	Generates a custom frequency from an external source
EPROM programmability	Easy customization and fast turnaround
Factory-programmable (CY2071A, CY2071AI) or field-programmable (CY2071AF, CY2071AFI) device options	Programming support available for all opportunities
Up to three configurable outputs	Generates three related frequencies from a single device
Low-skew, low-jitter, high-accuracy outputs	Meets critical industry standard timing requirements
Internal loop filter	Alleviates the need for external components
Power management (OE)	Supports low-power applications
Frequency select options	3 outputs with 2 user selectable frequencies
Configurable 5V or 3.3V operation	Supports industry standard design platforms
8-pin 150-mil SOIC package	Industry-standard packaging saves on board space

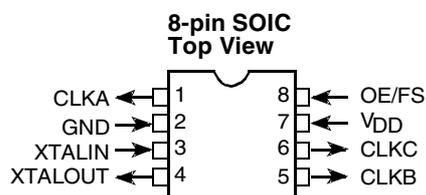
Selector Guide

Part Number	Outputs	Input Frequency Range	Output Frequency Range	Specifics
CY2071A	3	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–130 MHz (5V) 500 kHz–100 MHz (3.3V)	Factory Programmable Commercial Temperature
CY2071AI	3	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–100 MHz (5V) 500 kHz–80 MHz (3.3V)	Factory Programmable Industrial Temperature
CY2071AF	3	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–100 MHz (5V) 500 kHz–80 MHz (3.3V)	Field Programmable Commercial Temperature
CY2071AFI	3	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz–90 MHz (5V) 500 kHz–66.6 MHz (3.3V)	Field Programmable Industrial Temperature

Logic Block Diagram for CY2071A



Pin Configuration



Pin Summary

Name	Number	Description
CLKA	1	Configurable Clock Output
GND	2	Ground
XTALIN	3	Reference Crystal Input or External Reference Clock Input
XTALOUT	4	Reference Crystal Feedback
CLKB	5	Configurable Clock Output
CLKC	6	Configurable Clock Output
V _{DD}	7	Voltage Supply
OE / FS	8	Output Control Pin, either Output Enable or Frequency Select Input (Active-HIGH, internal pull-up resistor to V _{DD})

Notes:

- For best accuracy, use a parallel-resonant crystal, $C_L = 17$ pF.
- Float XTALOUT pin if XTALIN is driven by reference clock (as opposed to an external crystal).

Functional Description

The CY2071A is a general-purpose clock synthesizer designed for use in applications such as modems, disk drives, CD-ROM drives, video CD players, games, set-top boxes, and data/telecommunications. The device offers up to three configurable clock outputs in an 8-pin, 150-mil SOIC package and can operate off either a 3.3V or 5V power supply. The on-chip reference oscillator is designed for 10-MHz to 25-MHz crystals. Alternatively, an external reference clock of frequency between 1 MHz and 30 MHz can be used.

The CY2071A has one PLL and outputs three factory-EPROM configurable clocks: CLKA, CLKB, and CLKC. The output clocks can originate either from the PLL or the reference, or selected dividers thereof. Additionally, pin 8 can be configured to be an Output Enable or a Select input.

The CY2071A can replace multiple Metal Can Oscillators (MCO) in a synchronous system, providing cost and board space savings to the manufacturer. Hence, these devices are ideally suited for applications that require multiple, accurate, and stable clocks synthesized from low-cost generators in small packages. A hard-disk drive is an example of such an application. In this case, CLKA drives the PLL in the Read Controller, while CLKB and CLKC drive the MCU and associated sequencers.

CyClocks™ Software

CyClocks is an easy-to-use software application that allows you to configure any one of the EPROM-Programmable Clocks offered by Cypress. You may specify the input frequency, PLL and output frequencies, and different functional options.

Please note the output frequency ranges in this data sheet when specifying them in CyClocks to ensure that you stay within the limits. You can download a copy of CyClocks free on the Cypress Semiconductor website at www.cypress.com.

Consider using the CY2081 for applications that require unrelated output frequencies. Consider using the CY2291, CY2292, or CY2907 for applications that require more than three output clocks.

Cypress FTG Programmer

The Cypress Frequency Timing Generator (FTG) Programmer is a portable programmer designed to custom program our family of EPROM **Field** Programmable Clock Devices. The FTG programmers connect to a PC serial port and allow users of CyClocks software to quickly and easily program any of the CY2291F, CY2292F, CY2071AF, and CY2907F devices. The ordering code for the Cypress FTG Programmer is CY3670.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage.....	-0.5V to +7.0V
DC Input Voltage	-0.5V to V _{DD} +0.5V
Storage Temperature	-65°C to +150°C
Max. Soldering Temperature (10 sec)	260°C
Junction Temperature	150°C
Static Discharge Voltage	>2000V (per MIL-STD-883, Method 3015)

EDO DRAM

FEATURES

- JEDEC- and industry-standard x16 timing, functions, pinouts, and packages
- High-performance CMOS silicon-gate process
- Single power supply (+3.3V ±0.3V or 5V ±10%)
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR), HIDDEN; optional self refresh (S)
- BYTE WRITE access cycles
- 1,024-cycle refresh (10 row, 10 column addresses)
- Extended Data-Out (EDO) PAGE MODE access
- 5V-tolerant inputs and I/Os on 3.3V devices

OPTIONS

- Voltages¹
 - 3.3V
 - 5V
- Refresh Addressing
 - 1,024 (1K) rows
- Packages
 - Plastic SOJ (400 mil)
 - Plastic TSOP (400 mil)
- Timing
 - 50ns access -5
 - 60ns access -6
- Refresh Rates
 - Standard Refresh (16ms period) None
 - Self Refresh (128ms period) S²
- Operating Temperature Range
 - Commercial (0°C to +70°C) None
 - Extended (-20°C to +80°C) ET

Part Number Example:
MT4LC1M16E5TG-6

NOTE: 1. The third field distinguishes the low voltage offering: LC designates Vcc = 3.3V and C designates Vcc = 5V.
2. Available only on MT4LC1M16E5 (3.3V)

KEY TIMING PARAMETERS

SPEED	t _{RC}	t _{RAC}	t _{PC}	t _{AA}	t _{CAC}	t _{CAS}
-5	84ns	50ns	20ns	25ns	15ns	8ns
-6	104ns	60ns	25ns	30ns	17ns	10ns

MARKING

LC
C

E5

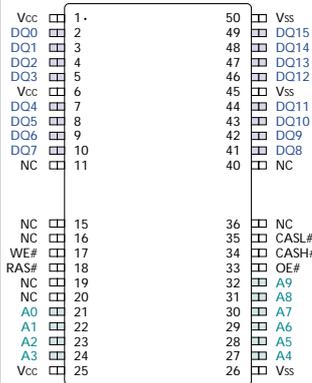
DJ
TG

None
S²

None
ET

PIN ASSIGNMENT (Top View)

44/50-Pin TSOP



GENERAL DESCRIPTION (continued)

of the two signals results in a BYTE WRITE cycle. CASL# transitioning LOW selects an access cycle for the lower byte (DQ0-DQ7), and CASH# transitioning LOW selects an access cycle for the upper byte (DQ8-DQ15).

Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) at a time. RAS# is used to latch the first 10 bits and CAS#, the latter 10 bits. The CAS# function also determines whether the cycle will be a refresh cycle (RAS# ONLY) or an active cycle (READ, WRITE or READ-WRITE) once RAS# goes LOW.

The CASL# and CASH# inputs internally generate a CAS# signal that functions like the single CAS# input on other DRAMs. The key difference is each CAS# input (CASL# and CASH#) controls its corresponding eight DQ inputs during WRITE accesses. CASL# controls DQ0-DQ7, and CASH# controls DQ8-DQ15. The two CAS# controls give the 1 Meg x 16 both BYTE READ and BYTE WRITE cycle capabilities.

A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS# (CASL# or CASH#), whichever occurs last. An EARLY WRITE occurs when WE is taken LOW prior to either CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE falls after CAS# (CASL# or CASH#) was taken LOW. During EARLY WRITE cycles, the data outputs (Q) will remain High-Z, regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no WRITE will occur, and the data outputs will drive read data from the accessed location.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by OE# and WE#.

The 1 Meg x 16 DRAM must be refreshed periodically in order to retain stored data.

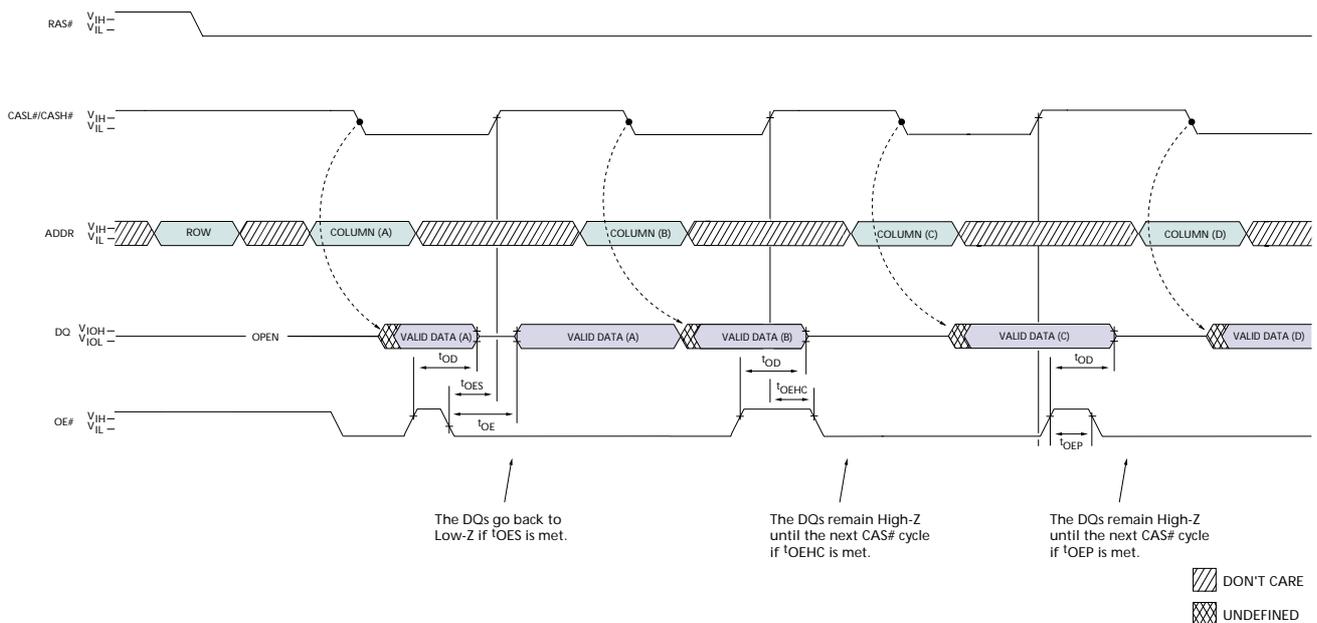
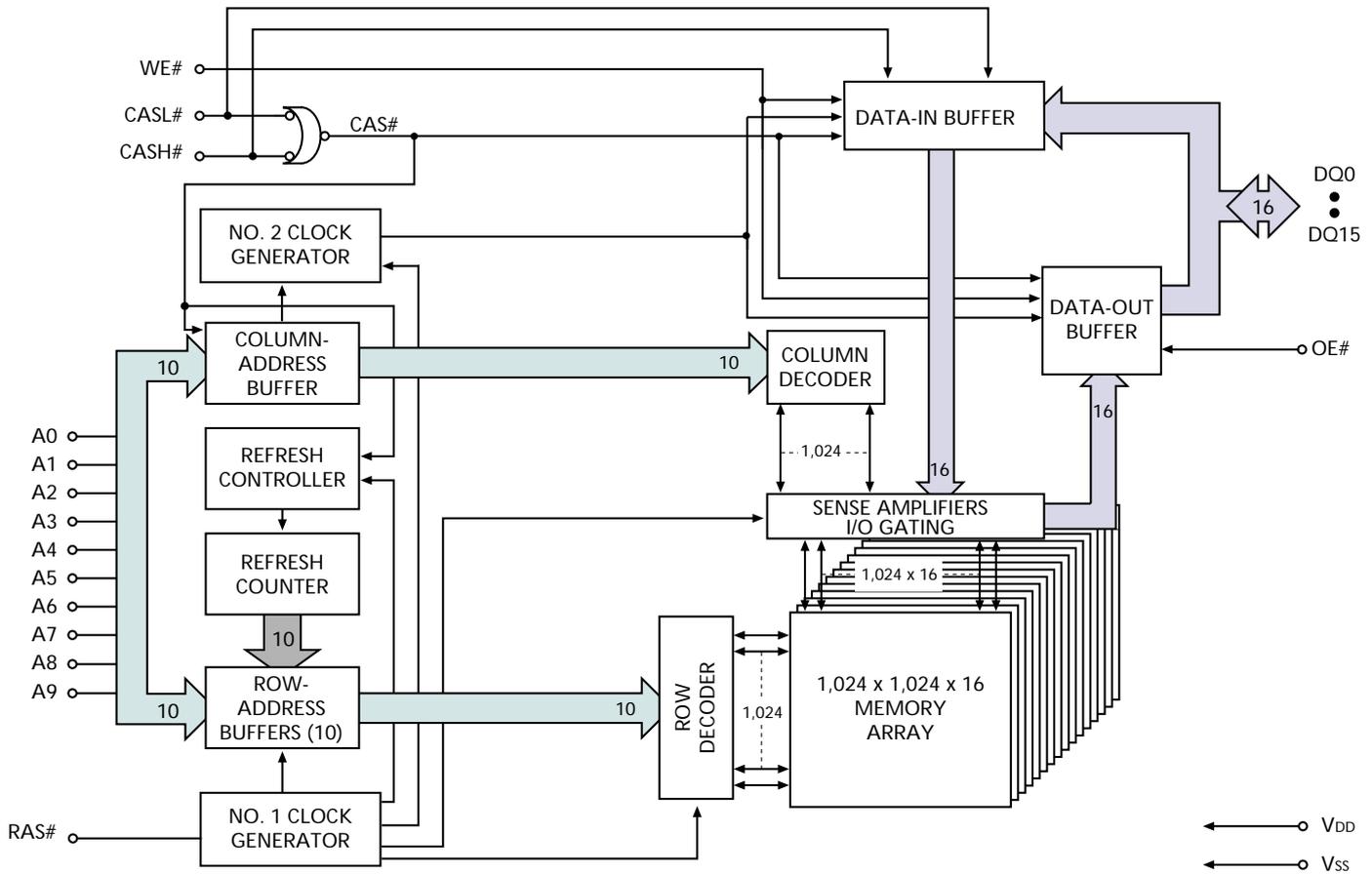


Figure 1
OE# Control of DQs

FUNCTIONAL BLOCK DIAGRAM

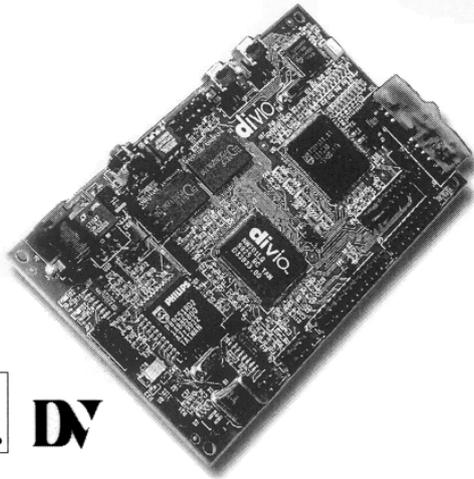


9.9.7 IC7404: NW700

divio™

NW700

DV Decoder
Daytona Beach
Reference Solution



Features and Benefits

Enhanced Feature set

- Fully DV-SD Compliant
- Automatic Audio and AUX Code Processing
- Pin compatible with NW701 (DV CODEC)

Low System Cost

- Integrated single-chip design including AV processing and video decoding
- Glue-less interface to Video Encoder (SAA7121), Audio Encoder (UDA1340), Micro-controller, and memory
- Integrated shuffle memory logic
- Requires only one 256K x 32 EDO DRAM

Real-time Performance

- High speed (33Mbytes/s throughput)
- 54MHz double clock speed for dual stream applications

Video and Audio Support

- CCIR656 Video output and I²S Audio output
- Support NTSC and PAL
- Selectable Audio channel (A/B or C/D)
- 48, 44.1, and 32KHz (12- and 16-bit) audio support

Simple Host Bus connectivity

- 8 or 16-bit asynchronous host bus interface
- built-in 512 byte DV FIFO
- Three interrupt pins for enhanced system control

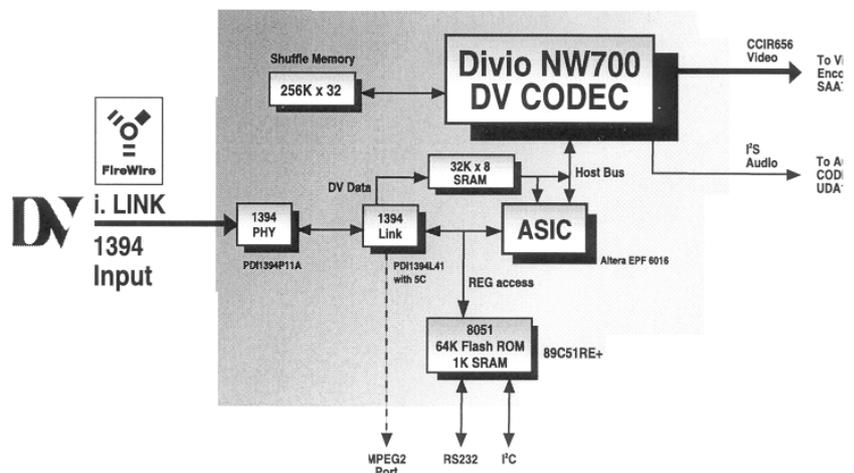
NW700 DV Decoder Daytona Beach Reference Solution

divio introduces the NW700, the world's first single-chip DV decoder. Fully DV-SD compliant and designed with divio's patented pending compression technology, the NW700 delivers unrivaled video quality, performance and compatibility. With a single-chip design and glueless interface to standard video components, divio's single chip DV decoder will replace current multi-chip solution and enable a new generation of cost-effective digital video consumer products.

divio has created the "Daytona Beach" reference solution that includes the NW700, Philips Semiconductor's PDI1394L4X audio/video 1394 LINK layer controller and PDI1394P11A 200 Mbits/sec PHY. divio provides a complete easy to integrate DV/IEEE1394 solution to OEMs to reduce time-to-market and development costs.

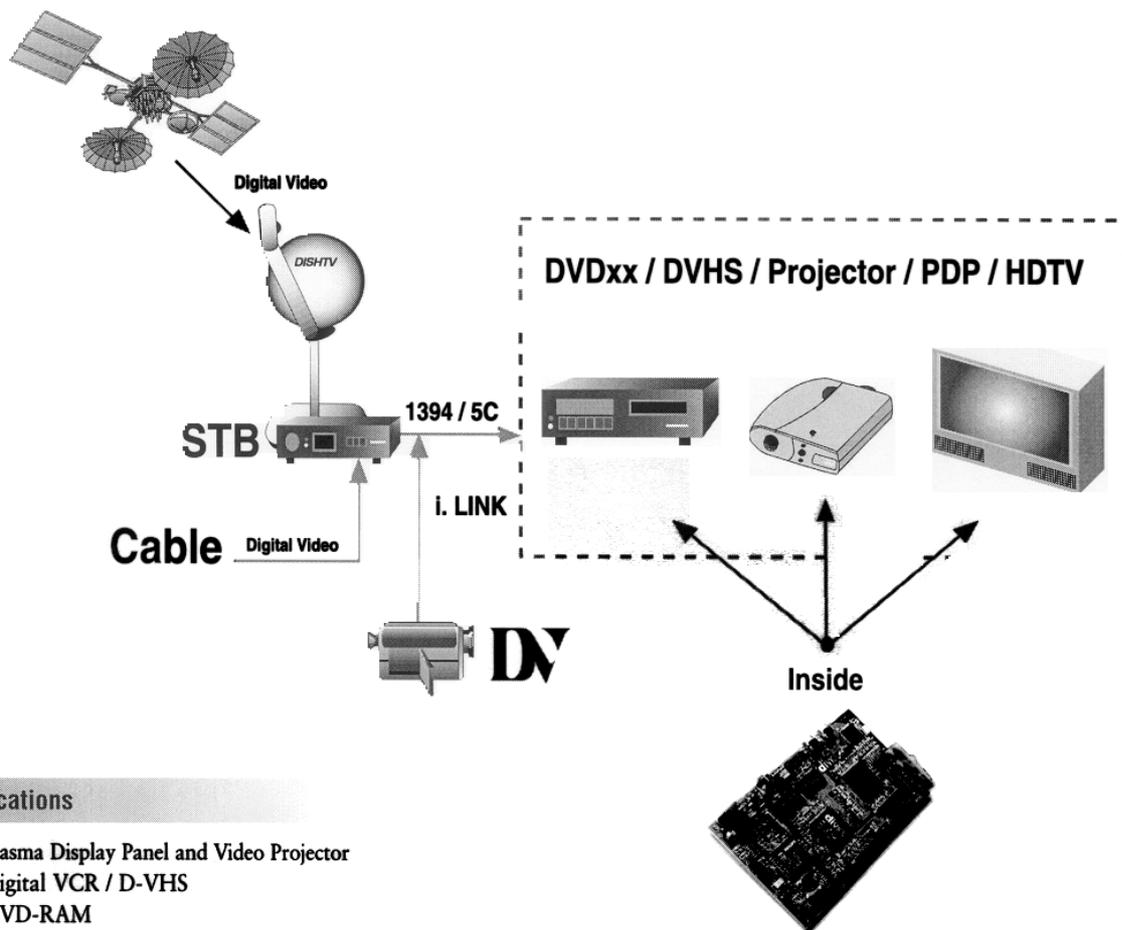
The NW700 provides an unprecedented feature-set that deliver real-time DV decoding functions to empower the next generation of consumer electronics devices.

DAYTONA BEACH DV Decode Module



NW700

DV Decoder
Daytona Beach
Reference Solution



Applications

- Plasma Display Panel and Video Projector
- Digital VCR / D-VHS
- DVD-RAM
- Digital Set-top-box
- HDTV

Daytona Beach Reference Kit

Board Components

- divio NW700 - DV Decoder
- 8051 μ C (P89C51RD2)
- 100p FPGA/32k x 8 SRAM
- IEEE1394 LINK (PDI1394L4X)
- IEEE1394 PHY (PDI1394P11A)
- 256 x 32 EDO Memory

Manufacturing Kit Contents

- Daytona Beach Reference Design
- Schematics, Gerber Files and BOM
- Technical Documents and Manuals
- FPGA and Firmware Source Code

Ordering Information

Part Number	Description
NW700LQ	DV Decoder
Daytona Beach	Manufacturing Kit



Sales Information

divio, inc.
997 East Arques Avenue
Sunnyvale, CA 94086 USA
Phone: (408) 732-1205
Fax: (408) 732-4022
E-mail: sales@divio.com
<http://www.divio.com>

Worldwide contacts:
visit <http://www.divio.com>



9.9.8 IC7506: UDA1334ATS

Low power audio DAC with PLL

UDA1334ATS

1 FEATURES**1.1 General**

- 2.4 to 3.6 V power supply voltage
- On-board PLL to generate the internal system clock:
 - Operates as an asynchronous DAC, regenerating the internal clock from the WS signal (called audio mode)
 - Generates audio related system clock (output) based on 32, 48 or 96 kHz sampling frequency (called video mode).
- Integrated digital filter plus DAC
- Supports sample frequencies from 16 to 100 kHz in asynchronous DAC mode
- No analog post filtering required for DAC
- Easy application
- SSOP16 package.

1.2 Multiple format data interface

- I²S-bus and LSB-justified format compatible
- 1f_s input data rate.

1.3 DAC digital features

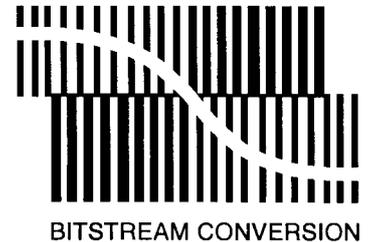
- Digital de-emphasis for 44.1 kHz sampling frequency
- Mute function.

1.4 Advanced audio configuration

- High linearity, wide dynamic range and low distortion.

1.5 PLL system clock generation

- Integrated low jitter PLL for use in applications in which there is digital audio data present but the system cannot provide an audio related system clock. This mode is called audio mode.
- The PLL can generate 256 × 48 kHz and 384 × 48 kHz from a 27 MHz input clock. This mode is called video mode.

**2 APPLICATIONS**

This audio DAC is excellently suitable for digital audio portable application, specially in applications in which an audio related system clock is not present.

3 GENERAL DESCRIPTION

The UDA1334ATS is a single chip 2 channel digital-to-analog converter employing bitstream conversion techniques, including an on-board PLL. The extremely low power consumption and low voltage requirements make the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates a playback function.

The UDA1334ATS supports the I²S-bus data format with word lengths of up to 24 bits and the LSB-justified serial data format with word lengths of 16, 20 and 24 bits.

The UDA1334ATS has basic features such as de-emphasis (44.1 kHz sampling frequency, only supported in audio mode) and mute.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1334ATS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

Low power audio DAC with PLL

UDA1334ATS

6 BLOCK DIAGRAM

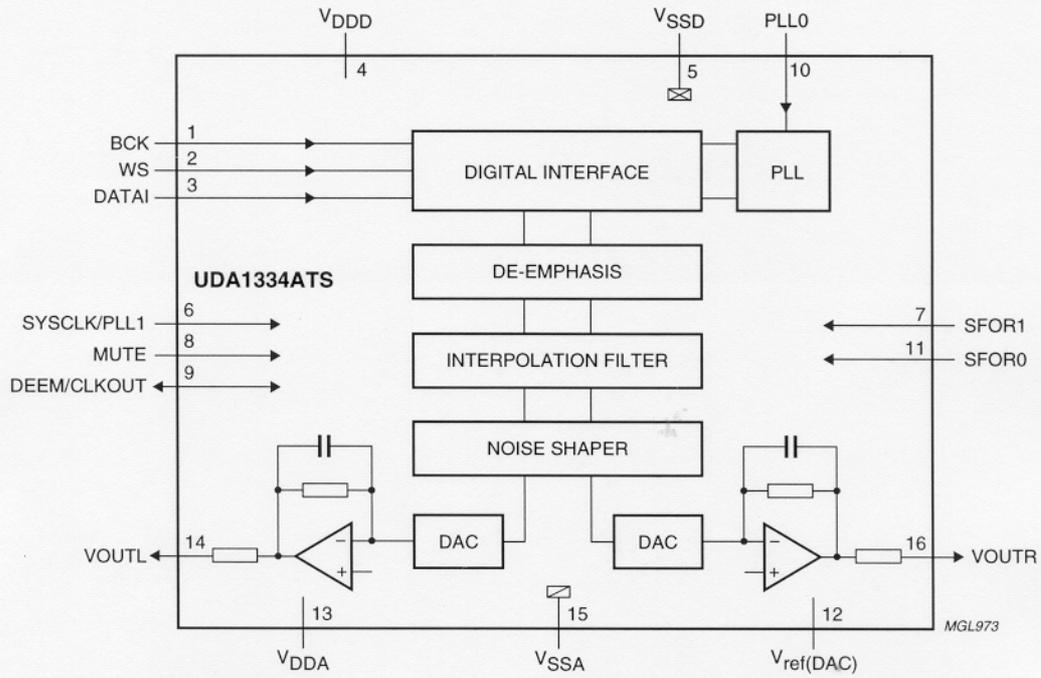


Fig.1 Block diagram.

Low power audio DAC with PLL

UDA1334ATS

7 PINNING

SYMBOL	PIN	PAD TYPE	DESCRIPTION
BCK	1	5 V tolerant digital input pad	bit clock input
WS	2	5 V tolerant digital input pad	word select input
DATAI	3	5 V tolerant digital input pad	serial data input
V _{DDD}	4	digital supply pad	digital supply voltage
V _{SSD}	5	digital ground pad	digital ground
SYSCLK/PLL1	6	5 V tolerant digital input pad	system clock input in video mode/PLL mode control 1 input in audio mode
SFOR1	7	5 V tolerant digital input pad	serial format select 1 input
MUTE	8	5 V tolerant digital input pad	mute control input
DEEM/CLKOUT	9	5 V tolerant digital input/output pad	de-emphasis control input in audio mode/clock output in video mode
PLL0	10	3-level input pad; note 1	PLL mode control 0 input
SFOR0	11	digital input pad; note 1	serial format select 0 input
V _{ref(DAC)}	12	analog pad	DAC reference voltage
V _{DDA}	13	analog supply pad	DAC analog supply voltage
VOUTL	14	analog output pad	DAC output left
V _{SSA}	15	analog ground pad	DAC analog ground
VOUTR	16	analog output pad	DAC output right

Note

1. Because of test issues these pads are not 5 V tolerant and both pads should be at power supply voltage level or at a maximum of 0.5 V above that level.

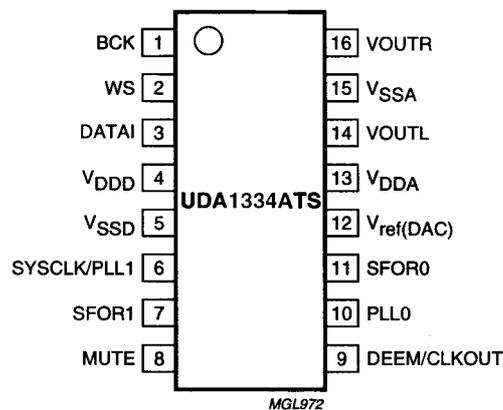


Fig.2 Pin configuration.

Low power audio DAC with PLL

UDA1334ATS

8 FUNCTIONAL DESCRIPTION

8.1 System clock

The UDA1334ATS incorporates a PLL capable of generating the system clock. The UDA1334ATS can operate in 2 modes:

- It operates as an asynchronous DAC, which means the device regenerates the internal clocks using a PLL from the incoming WS signal. This mode is called audio mode.
- It generates the internal clocks from a 27 MHz clock input, based on 32, 48 and 96 kHz sampling frequencies. This mode is called video mode.

In video mode, the digital audio input is slave, which means that the system must generate the BCK and WS signals from the output clock available at pin CLKOUT of the UDA1334ATS. The digital audio signals should be frequency locked to the CLKOUT signal.

Remarks:

1. The WS edge MUST fall on the negative edge of the BCK at all times for proper operation of the digital I/O data interface
2. For LSB-justified formats it is important to have a WS signal with a duty factor of 50%.

8.1.1 AUDIO MODE

Audio mode is enabled by setting pin PLL0 to LOW. De-emphasis can be activated via pin DEEM/CLKOUT according to Table 5.

In audio mode, pin SYSCLK/PLL1 is used to set the sampling frequency range as given in Table 1.

Table 1 Sampling frequency range in audio mode

SYSClk/PLL1	SELECTION
LOW	$f_s = 16$ to 50 kHz
HIGH	$f_s = 50$ to 100 kHz

8.1.2 VIDEO MODE

In video mode, the master clock is a 27 MHz external clock (as is available in video environment). A clock-out signal is generated at pin DEEM/CLKOUT. The output frequency can be selected using pin PLL0. The output frequency is either 12.228 MHz (256×48 kHz) with pin PLL0 being at MID level or 18.432 MHz (384×48 kHz) with pin PLL0 being HIGH, as given in Table 2.

Table 2 Clock output selection in video mode

PLL0	SELECTION
MID	12.228 MHz clock; note 1
HIGH	18.432 MHz clock; note 2
LOW	audio mode

Notes

1. The supported sampling frequencies are: 96, 48 and 24 kHz or 64, 32 and 16 kHz.
2. The supported sampling frequencies are: 96, 48 and 24 kHz; 72 and 36 kHz or 32 kHz.

8.2 Interpolation filter

The interpolation digital filter interpolates from $1f_s$ to $64f_s$ by cascading FIR filters (see Table 3).

Table 3 Interpolation filter characteristics

ITEM	CONDITION	VALUE (dB)
Pass-band ripple	$0f_s$ to $0.45f_s$	± 0.02
Stop band	$>0.55f_s$	-50
Dynamic range	$0f_s$ to $0.45f_s$	>114

8.3 Noise shaper

The 5th-order noise shaper operates at $64f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a Filter Stream DAC (FSDAC).

Low power audio DAC with PLL

UDA1334ATS

8.4 Filter stream DAC

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. No post filter is needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

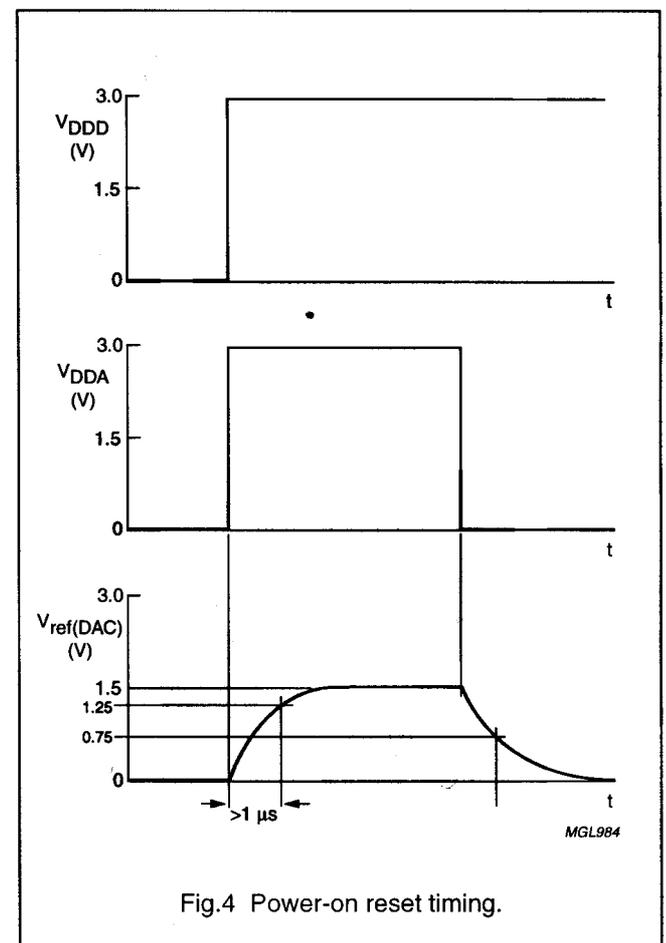
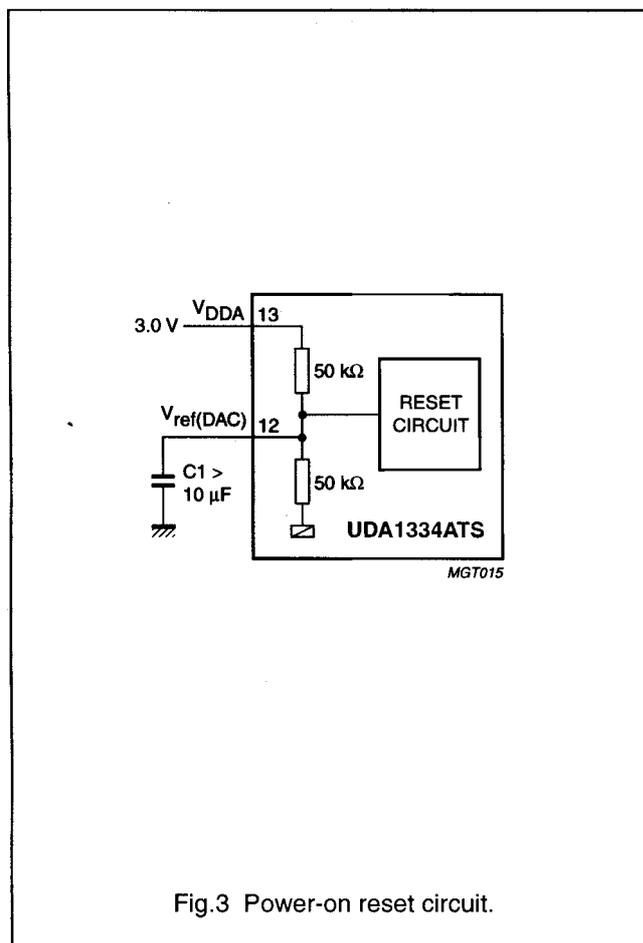
The output voltage of the FSDAC scales proportionally to the power supply voltage.

8.5 Power-on reset

The UDA1334ATS has an internal Power-on reset circuit (see Fig.3) which resets the test control block.

The reset time (see Fig.4) is determined by an external capacitor which is connected between pin $V_{ref(DAC)}$ and ground. The reset time should be at least $1 \mu\text{s}$ for $V_{ref(DAC)} < 1.25 \text{ V}$. When V_{DDA} is switched off, the device will be reset again for $V_{ref(DAC)} < 0.75 \text{ V}$.

During the reset time the system clock should be running.



Low power audio DAC with PLL

UDA1334ATS

8.6 Feature settings

8.6.1 DIGITAL INTERFACE FORMAT SELECT

The digital audio interface formats (see Fig.5) can be selected via pins SFOR1 and SFOR0 as shown in Table 4.

For the digital audio interface holds that the BCK frequency can be maximum 64 times WS frequency.

The WS signal must change at the negative edge of the BCK signal for all digital audio formats.

Table 4 Data format selection

SFOR1	SFOR0	INPUT FORMAT
LOW	LOW	I ² S-bus input
LOW	HIGH	LSB-justified 16 bits input
HIGH	LOW	LSB-justified 20 bits input
HIGH	HIGH	LSB-justified 24 bits input

8.6.2 DE-EMPHASIS CONTROL

This function is only available in audio mode. In that case, pin DEEM/CLKOUT can be used to activate the digital de-emphasis for 44.1 kHz as given in Table 5.

Table 5 De-emphasis control (audio mode)

DEEM/CLKOUT	FUNCTION
LOW	de-emphasis off
HIGH	de-emphasis on

8.6.3 MUTE CONTROL

The output signal can be soft muted by setting pin MUTE to HIGH as given in Table 6.

Table 6 Mute control

MUTE	FUNCTION
LOW	mute off
HIGH	mute on

Low power audio DAC with PLL

UDA1334ATS

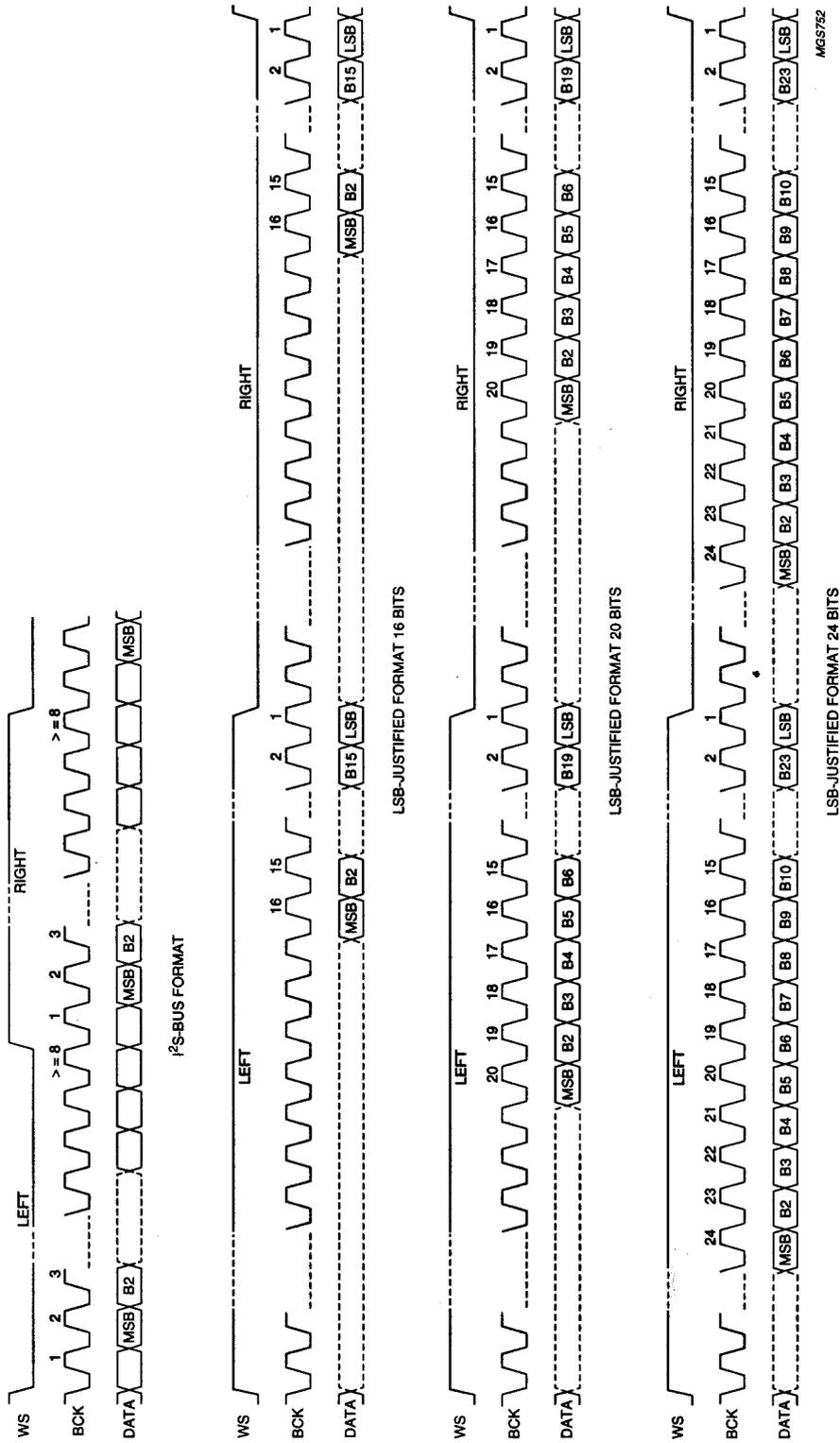


Fig.5 Digital audio formats.

9.10 List of Abbreviations

Digital Board	B_IN_VIP
+12V	Video blue input to Video Input Processor
+12V Power Supply	B_OUT
+2V5_FLI	Video blue output from Host Decoder
+2V5 Power Supply for FLI	B_OUT_B
+2V5_PLL	Filtered blue video output
+2V5 Power Supply for PLL	BA
+3V3	Bank Address
+3V3 Power Supply	BCLK_CTL_SERVICE
+3V3_ANA	Bitclock control Service Interface
+3V3 Power Supply Analogue	BE_BCLK
+3V3_DD	Basic Engine I2S bit clock
+3V3 Power Supply Digital	BE_BCLK_VSM
+3V3_FLI	Basic Engine I2S bit clock to VSM
+3V3 Power Supply for FLI	BE_CPR
+5V	Basic Engine Control Processor ready to accept data
+5V Power Supply	BE_DATA_RD
+5V_BUFFER	Basic Engine Data read
+5V Power Supply for Video Filters	BE_DATA_WR
5508_HS	Basic Engine Data write
Horizontal Synchronisation from Host Decoder to Progressive Scan	BE_FAN
5508_ODD_EVEN	Basic Engine FAN
Odd - Even control from Host Decoder to Progressive Scan	BE_FLAG
-5V	Basic Engine error flag
-5V Power Supply	BE_IRQN
-5V_BUFFER	Basic Engine interrupt request
-5V Power Supply for Video Filters	BE_LOADN
A_EMPRESS(13:0)	Basic Engine LOAD(LOW active)
EMPRESS address output to SDRAM	BE_RXD
ACC_ACLK_OSC	Basic Engine S2B received data
Audio Clock PLL output sync with incoming video for record	BE_SUR
ACC_ACLK_PLL	Basic Engine servo unit ready to accept data (S2B)
Audio Clock PLL output for play back	BE_SYNC
ACLK_EMP	Basic Engine sector/abs time sync
EMPRESS audio clock output	BE_TXD
AD_ACLK	Basic Engine S2B transmitted data
Audio Decoder Clock	BE_V4
AD_BCLK	Basic Engine versatile input pin
Audio Decoder I2S bit clock	BE_WCLK
AD_DATAO	Basic Engine I2S word clock
Audio Decoder Output data (PCM)	C_IN
AD_SPDIF33	Video Chrominance input
Audio digital output to the analog board	C_IN_VIP
AD_WCLK	Chrominance input to Video Input Processor
Audio Decoder I2S word clock	C_OUT
AE_ACLK	Chrominance output from Host Decoder
Audio Encoder Clock	C_OUT_B
AE_ACLK_OEN	Filtered Chrominance output
Audio Encoder Clock Output Enable	CAS
AE_BCLK	Column Address strobe
Audio Encoder I2S bit clock	CB_OUT(9:0)
AE_BCLK_DV	Chrominance Blue out
Audio Encoder I2S bit clock to DVIO	CLK4
AE_BCLK_VSM	SDRAM clock
Audio Encoder I2S bit clock to VSM	CPUINT0
AE_DATAI	Control processor unit interrupt
Audio Encoder Input data (PCM)	CPUINT1
AE_DATAI_DV	Control processor unit interrupt
Audio Encoder Input data (PCM) from DVIO	CR_OUT(9:0)
AE_DATAO	Chrominance Red out
Audio Encoder Output data (PCM)	CTS1P
AE_WCLK	Clear to send (Service Interface)
Audio Encoder I2S word clock	CVBS_OUT
AE_WCLK_DV	Composite video output out of the Host Decoder
Audio Encoder I2S word clock to DVIO	CVBS_OUT_B
AE_WCLK_VSM	Filtered Composite video output
Audio Encoder I2S word clock to VSM	CVBS_OUT_B_VIP
ANA_WE	Composite video output to Video Input Processor(digital board video loop)
Analogue write enable	CVBS_Y_IN
ANA_WE_LV	Composite video/Luminance input
Analogue write enable Low Voltage	CVBS_Y_IN_A
	Composite video/Luminance input to Video Input Processor
	CVBS_Y_IN_B
	Composite video/Luminance input to Video Input Processor

CVBS_Y_IN_C	Host Decoder SDRAM data mask enable(Lower)
Composite video/Luminance input to Video Input Processor	HD_M_DQMU
D_ADDR(10:0)	Host Decoder SDRAM data mask enable(Upper)
Address bus	HD_M_RASN
D_DATA(29:0)	Host Decoder SDRAM row address strobe
Data bus	HD_M_WEN
D_EMPRESS(15:0)	Host Decoder SDRAM write enable
SDRAM data input/output of EMPRESS	HSOUT
D_PAR_D(7:0)	Horizontal synchronisation OUT
Front-end parallel interface data (record)	ION
D_PAR_DVALID	Inverted ON: Enable the power supply for the digital board when LOW
Front-end parallel interface data valid	IRESET_DIG
D_PAR_REQ	Initialisation of the digital board, HIGH when power ON
Front-end parallel interface request	JTAG3_TCK
D_PAR_STR	JTAG Test Clock
Front-end parallel interface strobe	JTAG3_TD_VIP_TO_VE
D_PAR_SYNC	JTAG Transmitted Data Video Input Processor to Video Encoder
Front-end parallel interface sync	JTAG3_TD_VSM_TO_VIP
DV_IN_CLK	JTAG Transmitted Data Versatile Stream Manager to Video Input Processor
Digital Video in clock from DVIO board	JTAG3_TMS
DV_IN_DATA(7:0)	JTAG Test Mode Select
Digital Video in data bus from DVIO board	JTAG3_TRSTN
DV_IN_HS	JTAG Test part ResetN
Digital Video in horizontal synchronisation from DVIO board	LOAD_DVN
DV_IN_VS	LOAD Digital Video(LOW active)
Digital Video in vertical synchronisation from DVIO board	MUTEN
EMI_A(21:1)	Mute enable
External Memory Interface Address Bus(Host Decoder)	MUTEN_LV
EMI_BE0N	Mute enable Low Voltage
External Memory Interface Lower byte enable(Host Decoder)	P_SCAN_YUV(7:0)
EMI_BE1N	Progressive Scan digital video bus
External Memory Interface Upper byte enable(Host Decoder)	R_IN_VIP
EMI_CAS0N	Video Red input to Video Input Processor
External Memory Interface SDRAM column address strobe(Host Decoder)	R_OUT
EMI_CE1N	Video Red output from Host Decoder
External Memory Interface VSM Lower bank enable	R_OUT_B
EMI_CE2N	Filtered Red Video output from Host Decoder
External Memory Interface VSM Higher bank enable	RAS
EMI_CE3N	Row Address Strobe
External Memory Interface flash IC's enable	RESETN
EMI_D(15:0)	Reset Host Decoder
External Memory Interface Data Bus(Host Decoder)	RESETN_BE
EMI_PROCCLK	System reset basic engine (buffered)
External Memory Interface Processor Clock(Host Decoder)	RESETN_DVIO
EMI_RWN	System reset Digital Video Input Output (buffered)
External Memory Interface Read/Write control signal(Host Decoder)	RESETN_VE
EMI_WAIT	System reset Video Encoder
External Memory Interface Wait state request(Host Decoder)	ROMH_CEN
EMPRESS_BOOT	Flash 2 chip enable
EMPRESS BOOT select input	ROML_CEN
EMPRESS_IRQN	Flash 1 chip enable
EMPRESS Interrupt request output	RSTN_BE
FLASH_OEN	Reset control of basic engine
FLASH output enable control signal	RSTN_DVIO
G_IN_VIP	Reset control of DVIO
Video green input to Video Input Processor	RTS1P
G_OUT	Ready To Send data to service serial interface
Video green output from Host Decoder	RX1P
G_OUT_B	Receive data from service serial interface
Filtered green video output from Host Decoder	SCL
GNDD	I2C bus clock
Digital Ground	SD_CASN
HD_M_AD(13:0)	SDRAM Column Address strobe output (active LOW)
Host Decoder SDRAM address bus	SD_CLK
HD_M_CASN	SDRAM clock output
Host Decoder SDRAM column address strobe	SD_CLKE
HD_M_CLK	SDRAM clock enable output
Host Decoder SDRAM clock	SD_CSN
HD_M_CS0N	SDRAM
Host Decoder SDRAM chip select	SD_DQM(1:0)
HD_M_DQ(15:0)	SDRAM data mask enable output
Host Decoder SDRAM data bus	SD_RASN
HD_M_DQML	

SDRAM row address strobe output	VDDA2A_7118
SD_WEN	Power supply for analog input of VIP
SDRAM write enable output	VDDA3A_7118
SDA	Power supply for analog input of VIP
I2C bus data	VDDA4A_7118
SEL_ACLK1	Power supply for analog input of VIP
Select audio clock(playback)	VDDE_7118
SM_CS3N	Power supply digital for peripheral cells of VIP
SRAM chip select	VDDI_7118
SM_LBN	Power supply digital for core of VIP
SRAM lower bank	VDDX_7118
SM_OEN	Power supply for crystal oscillator of VIP
SRAM output enable	VE_DATA(7:0)
SM_UBN	Video Encoder data Bus
SRAM upper bank	VE_DSN
SM_WEN	Video Encoder Data Strobe
SRAM write enable	VE_DTACKN
SMA(17:0)	Video Encoder Data Transfer acknowledge
SRAM address output	VIP_ERROR
SMD(15:0)	Video Input Processor error
SRAM data input/output	VIP_FB
SYSCLK_EMPRESS	Video Input Processor Fast Blanking
System clock EMPRESS	VIP_FID_FF
SYSCLK_PROGSCAN	Video Input Processor field identifier to Flip Flop
System clock Progressive Scan	VIP_HS
SYSCLK_VSM_5508	Video Input Processor horizontal synchronisation
System clock VSM and Host decoder	VIP_ICLK
TX1P	Video Input Processor input Clock
Transmit data to service serial interface	VIP_IDQ
U_IN	Video Input Processor output data qualifier
Video U input	VIP_IGP1
U_IN_VIP	Video Input Processor input general purpose 1
Video U input to Video Input Processor	VIP_INT
V_IN	Video Input Processor interrupt
Video V input	VIP_RTS1
V_IN_VIP	Video Input Processor ready to send
Video V input to Video Input Processor	VIP_VS
VCC3_CLK_BUF	Video Input Processor vertical synchronisation
Power supply 3V3 clock buffer	VIP_YUV(7:0)
VCC3_VSM	Video Input Processor digital video(CCIR 656)
Power supply 3V3 Versatile Stream Manager	VS_IN
VCC3_VSM_MEM	Vertical synchronisation IN
Power supply 3V3 Versatile Stream Manager Memory	VSM_M_A(13:0)
VCC5_4046	Versatile Stream Manager SDRAM address bus
Power supply 5V to PLL IC	VSM_M_CASN
VDD_125	Versatile Stream Manager SDRAM column address strobe
Power supply 5V to buffer 7202	VSM_M_CLKEN
VDD_CORE	Versatile Stream Manager SDRAM clock enable
Sti5508 Core supply voltage 2.5V	VSM_M_CLKOUT
VDD_EMP	Versatile Stream Manager SDRAM clock out
Empress supply voltage 3.3V	VSM_M_D(15:0)
VDD_EMP_CORE	Versatile Stream Manager SDRAM data bus
Empress Core supply voltage 2.5V	VSM_M_LDQM
VDD_FLASH_H	Versatile Stream Manager SDRAM lower data mask enable
Flash 7301 supply voltage	VSM_M_RASN
VDD_FLASH_L	Versatile Stream Manager SDRAM row address strobe
Flash 7302 supply voltage	VSM_M_UDQM
VDD_LVC32	Versatile Stream Manager SDRAM upper data mask enable
Power supply LVC32	VSM_M_WEN
VDD_PCM	Versatile Stream Manager SDRAM write enable
Power supply Audio decoder of Sti5508	VSM_UART1_CTSN
VDD_PLL	Versatile Stream Manager UART1 clear to send to analog board (UART1 is gateway to analog board)
Power supply PLL audio decoder of Sti5508	VSM_UART1_RTSN
VDD_RGB	Versatile Stream Manager UART2 clear to send to DVIO board (UART2 is gateway to DVIO board)
Power supply video encoder of Sti5508	VSM_UART1_RX
VDD_STI	Versatile Stream Manager UART1 ready to send to analog board
Power supply of Sti5508	VSM_UART1_TX
VDD_YCC	Versatile Stream Manager UART2 ready to send to DVIO board
Power supply video encoder of Sti5508	VSM_UART2_CTSN
VDD5_MK2703	Versatile Stream Manager UART1 received data to analog board
Power supply MK2703	
VDD5_OSC	
Power supply Oscillator	
VDDA1A_7118	
Power supply for analog input of VIP	

VSM_UART2_RTSN	Configuration Clock
Versatile Stream Manager UART2 received data to DVIO board	CLK27M
VSM_UART2_RX	27MHz Clock
Versatile Stream Manager UART1 transmitted data to analog board	CLK27M_CON
VSM_UART2_TX	27MHz Clock to Digital Board
Versatile Stream Manager UART2 transmitted data to DVIO board	CLK27M_DV
VSOUT	27MHz Clock Digital Video Codec
Vertical synchronisation OUT	CLK27M_OSC
WE	27MHz Clock IC7304
Write Enable	CLOCKGENAUD
Y_IN	Clock generator Audio
Luminance input from analog board	CLOCKGENVID
Y_OUT	Clock generator Video
Luminance output from Host Decoder	CTSN
Y_OUT_B	Clear to Send
Filtered luminance output	DATA
YY_OUT(9:0)	Data from config ROM
Luminance output from FLI	DONE
Divio Board	Indication of the completion of the configuration process
+35V_DV_EDO	DOUT
+3V3 Power supply EDO Bus IC7404	Serial configuration data output
+3V3	DV_ASN
+3V3 Power supply	DVCODEC Address Strobe
+3V3_DLY	DV_DRQN
+3V3 Power supply for IC7500	DVCODEC Data Request Interrupt
+3V3_DV	DV_DSLN
+3V3 Power supply for IC7404	DVCODEC Data Strobe Lower 8 bits
+3V3_FPGA	DV_DSUN
+3V3 Internal Power supply for IC7303	DVCODEC Data Strobe Upper 8 Bits
+3V3_FPGA_CONF	DV_DTACKN
+3V3 Power supply for IC 7300	DVCODEC Data Transfer Acknowledge
+3V3_IIEEE_A	DV_ERRN
+3V3 Analogue Power supply for PHY IC 7101	DVCODEC Error Interrupt
+3V3_IIEEE_D	DV_HS_IN
+3V3 Digital Power supply for PHY IC 7101	DVCODEC Horizontal synchronisation In
+3V3_IIEEE_PLL	DV_HS_OUT
+3V3 PLL Power supply for PHY IC 7101	DVCODEC Horizontal synchronisation Out
+3V3_LINK	DV_LCN
+3V3 Power supply IC7103	DVCODEC Last Code Interrupt
+3V3_PLL	DV_PDN
+3V3 Power supply IC7307 & IC7308	DVCODEC Power Down
+3V3_SRAM	DV_RSTN
+3V3 Power supply IC7301, IC7302, IC7305 & IC7306	DVCODEC System Reset for NW701
+5V	DV_RWN
+5V Power supply	DVCODEC Read/Write control signal
+5V_PROC	DV_VS
+5V Power supply IC7200, IC7201, IC7203 & IC7208	DVCODEC Vertical synchronisation
+VCC_DV_RAM	FIFOA_A(0:15)
+3V3 Power supply for DV_RAM (IC7400--> IC7404)	FIFO buffer A Address bus
1394_RSTN	FIFOA_OEN
Reset of LINK IC (7103) and PHY IC (7101)	FIFO buffer A Output enable
A(0:8)	FIFOA_WEN
Address lines	FIFO buffer A Write enable
AUD_BCLK	HAD(0:7)
Audio Bit Clock	Host Address/Data bus for register settings of IC7404
AUD_MUTE	INITN
Audio Mute	Initiate Configuration
AUD_SDI	IO(0:30)
Audio Serial Data Input	Data bus of IC7404
AUD_SDO_CON	ISPN
Audio Serial Data Output to buffer IC 7505	In System Program Line (used for programming IC7203)
AUD_SDO_DAC	LCASN
Audio Serial Data Output to DAC IC 7506	Lower Column Address strobe for IC7404 DRAMS
AUD_WS_701	LINK_AVCLK
Audio Word Select to DV CODEC IC 7404	LINK IC Audio/Video Interface Clock
AUD_WS_OUT	LINK_AVFSYNC
Audio Word Select to buffer IC 7505	LINK IC Audio/Video frame sync
BUFENN_AUD	LINK_AVREADY
Buffer Enable Audio	LINK IC Audio/Video data ready to send
BUFENN_VID	LINK_AVSYNC
Buffer Enable Video	LINK IC Audio/Video packet sync
CCLK	LINK_AVVALID
	LINK IC Audio/Video data valid
	LINK_CSN
	LINK IC chip select

LINK_INTN
LINK IC interrupt
LINKFIFO_DQ(0:7)
Audio Video data interface
PA(0:15)
SRAM processor address
PAD(0:7)
SRAM processor data
PALE
Processor Address Latch Enable
PHY_CNA
PHY 1394 cable not active
PHY_LPS
LINK IC power status
PINT0N
Processor interrupt 0
PINT1N
Processor interrupt 1
PRDN
Processor read
PROGRAMN
Low active input to initiate a configuration cycle
PRSTN
Processor reset
PWRN
Processor write
RASN
Row address strobe
RESETN
DVIO board reset
RTSN
System Reset
RXD
Receive Data
SRAMCE0N
SRAM processor chip enable 0
SRAMRDN
SRAM processor output enable
TCK
Boundary scan Test Clock
TDI
Boundary scan Test Data Input
TDO
Boundary scan Test Data Output
TDO_CONF
Boundary scan Test Data Output from IC 7309
TMS
Boundary scan Test Mode Select
TXD
Transmitted Data
UCASN
Upper column address strobe
WEN
Write Enable control signal to SRAM
YUV(0:7)
Digital Video

10. Spare Parts List

Mechanical DVDR980 /001 /021

Various

0060	3104 127 13280	CONNECTOR FRONT ASSY (EU)
0065	3104 127 13450	TRAY FRONT ASSY COMPLETE
0081		VAE8010/02
0081		VAE8015/01
0151	3104 127 13320	COVER ASSY
0191	3104 124 07455	FILTER AIR INLED BOTTOM
0197	3104 123 30002	DUST FILTER
0198	3104 124 07733	FILTER AIR INLET COVER
0199	3104 128 93031	DC BRUSHLESS FAN
0251	3104 127 10740	FOOT SILVER ASSY
0252	3104 127 10740	FOOT SILVER ASSY
0253	3104 127 10740	FOOT SILVER ASSY
0254	3104 127 10740	FOOT SILVER ASSY
0309▲	3104 125 24250	USER MANUAL DVDR980/ EUR
0370	9307 002 60006	DVDRW/006 PHILIPS DISC EUROPE
1001▲	3104 128 07750	DVDR DIG. BOARD 1.5 EMPRESS/EU
1002▲	3122 427 22711	PSU DVDR1000-2 EURO 50PS203
1003▲	3103 608 50290	DVDR ANALOG BOARD EUR GEN 1.5
8001	3104 157 11641	CWAS FLEX DVD 22 70 32S
8002	3104 157 11641	CWAS FLEX DVD 22 70 32S
8003	3104 157 11790	CWAS SPLIT FLEX 30 100 32S
8004	3104 157 11531	CWAS FLEX DVD 10 110 32S

Mechanical DVDR980 /051

Various

0060	3104 127 13420	CONNECTOR FRONT ASSY (UK)
0065	3104 127 13450	TRAY FRONT ASSY COMPLETE
0081		VAE8010/02
0081		VAE8015/01
0151	3104 127 13320	COVER ASSY
0191	3104 124 07455	FILTER AIR INLED BOTTOM
0197	3104 123 30002	DUST FILTER
0198	3104 124 07733	FILTER AIR INLET COVER
0199	3104 128 93031	DC BRUSHLESS FAN
0251	3104 127 10740	FOOT SILVER ASSY
0252	3104 127 10740	FOOT SILVER ASSY
0253	3104 127 10740	FOOT SILVER ASSY
0254	3104 127 10740	FOOT SILVER ASSY
0309▲	3104 125 24270	USER MANUAL DVDR980 UK
0370	9307 002 60006	DVDRW/006 PHILIPS DISC EUROPE
1001▲	3104 128 07750	DVDR DIG. BOARD 1.5 EMPRESS/EU
1002▲	3122 427 22711	PSU DVDR1000-2 EURO 50PS203
1003▲	3103 608 50290	DVDR ANALOG BOARD EUR GEN 1.5
8001	3104 157 11641	CWAS FLEX DVD 22 70 32S
8002	3104 157 11641	CWAS FLEX DVD 22 70 32S
8003	3104 157 11790	CWAS SPLIT FLEX 30 100 32S
8004	3104 157 11531	CWAS FLEX DVD 10 110 32S

Mechanical DVD985 /001 /021

Various

0060	3104 127 13600	CONNECTOR FRONT ASSY 985/EUR
0065	3104 127 13450	TRAY FRONT ASSY COMPLETE
0081		VAE8015/01
0151	3104 127 13320	COVER ASSY
0191	3104 124 07455	FILTER AIR INLED BOTTOM

0197	3104 123 30002	DUST FILTER
0198	3104 124 07733	FILTER AIR INLET COVER
0199	3104 128 93031	DC BRUSHLESS FAN
0251	3104 127 10740	FOOT SILVER ASSY
0252	3104 127 10740	FOOT SILVER ASSY
0253	3104 127 10740	FOOT SILVER ASSY
0254	3104 127 10740	FOOT SILVER ASSY
0309▲	4822 736 16493	EN-FR-ES-BR.PORT-TRAD.CHIN
0370	9307 002 60006	DVDRW/006 PHILIPS DISC EUROPE
1001▲	3104 128 07750	DVDR DIG. BOARD 1.5 EMPRESS/EU
1002▲	3122 427 22711	PSU DVDR1000-2 EURO 50PS203
1003▲	3103 608 50290	DVDR ANALOG BOARD EUR GEN 1.5
1005	3104 128 07900	PB DVDR1000 DVIO GEN.1.5 ASSY
8001	3104 157 11641	CWAS FLEX DVD 22 70 32S
8002	3104 157 11641	CWAS FLEX DVD 22 70 32S
8003	3104 157 11790	CWAS SPLIT FLEX 30 100 32S
8004	3104 157 11531	CWAS FLEX DVD 10 110 32S
8013	3104 128 92921	CABLE IEEE-1394 4P AMP
8015	3104 157 12191	CWAS FLEX DVDR 7 360 32S

Accessorieskit DVDR980 /001 /021

Various

0318	3128 147 13670	RC2056/01 IRT PROD ASSY
0320	4822 321 22611	
0321	3104 128 92490	VIDEO CORD SET GOLD PLATED
0322▲	2422 070 98133	MAINSCORD EUR 1M5 BK B
0323	4822 321 61847	SCART
0324	3111 170 21592	CORDON ANT. L.1,50M
0370	3104 128 93041	S-VHS CABLE 1.5M
0371	9307 002 60006	DVDRW/006 PHILIPS DISC EUROPE

Accessories DVDR980 /051

Various

0318	3128 147 13670	RC2056/01 IRT PROD ASSY
0320	4822 321 22611	
0321	3104 128 92490	VIDEO CORD SET GOLD PLATED
0322▲	4622 001 60590	CORDSET UK (WITH COIL)
0323	4822 321 61847	SCART
0324	3111 170 21592	CORDON ANT. L.1,50M
0370	3104 128 93041	S-VHS CABLE 1.5M
0371	9307 002 60006	DVDRW/006 PHILIPS DISC EUROPE

Accessories DVDR985 /051

Various

0318	3128 147 13670	RC2056/01 IRT PROD ASSY
0320	4822 321 22611	
0321	3104 128 92490	VIDEO CORD SET GOLD PLATED
0322▲	4622 001 60590	CORDSET UK (WITH COIL)
0323	4822 321 61847	SCART
0324	3111 170 21592	CORDON ANT. L.1,50M
0370	3104 128 93041	S-VHS CABLE 1.5M
0371	9307 002 60006	DVDRW/006 PHILIPS DISC EUROPE

Front complete

Various

0001	3104 127 13470	FRONT ASSY
0002	3104 127 13220	SIDE PLATE LEFT ASSY
0003	3104 127 13230	SIDE PLATE RIGHT ASSY
0004	3104 124 08470	WINDOW

0005	3139 244 00761	LIGHT GUIDE DVD STEP 2K
0011	3104 127 13240	BUTTON STANDBY ASSY
0012	3104 127 13250	BUTTON PLAY/STOP/RECORD ASSY
0013	3104 127 13260	BUTTON OPENCLOSE/RECVOLUM ASSY
0014	3104 127 13270	BUTTON DISPLAY ASSY
0015	3104 127 13530	IR LENS ASSY
1001	3104 128 08270	DISPLAYPANEL 4330 ASSY DVDR980

Front assy DVD985 /001 /021

Various

0001	3104 127 13580	FRONT ASSY
0002	3104 127 13220	SIDE PLATE LEFT ASSY
0003	3104 127 13230	SIDE PLATE RIGHT ASSY
0004	3104 124 08470	WINDOW
0005	3139 244 00761	LIGHT GUIDE DVD STEP 2K
0011	3104 127 13240	BUTTON STANDBY ASSY
0012	3104 127 13250	BUTTON PLAY/STOP/RECORD ASSY
0013	3104 127 13260	BUTTON OPENCLOSE/RECVOLUM ASSY
0014	3104 127 13270	BUTTON DISPLAY ASSY
0015	3104 127 13530	IR LENS ASSY
1001	3104 128 08270	DISPLAYPANEL 4330 ASSY DVDR980
1006	3104 128 07610	PCB ASSY 4319 DVIO-FRONT

Display PWB

Various

1140	4822 276 13732	SWITCH TACT PUSH
1150	2422 086 10947	PROT DEV 65V 250MA PSC A
1153	5322 242 73686	CST12,00MTW-TF01
1156	2422 527 00513	BUZZER PIEZO CB13PA-X5
1159	4822 276 13732	SWITCH TACT PUSH
1160	4822 276 13732	SWITCH TACT PUSH
1162	4822 276 13732	SWITCH TACT PUSH
1163	4822 276 13732	SWITCH TACT PUSH
1167	4822 276 13732	SWITCH TACT PUSH
1168	4822 276 13732	SWITCH TACT PUSH
1169	4822 276 13732	SWITCH TACT PUSH
1170	4822 276 13732	SWITCH TACT PUSH
1171	4822 276 13732	SWITCH TACT PUSH
1174	4822 276 13732	SWITCH TACT PUSH

-II-

2140	4822 124 11946	22µF 20% 16V
2150	4822 124 80231	47µF 20% 16V
2151	4822 126 14305	100nF 10% 16V 0603
2152	4822 121 43526	47nF 5% 250V
2154	4822 124 40849	330µF 20% 16V
2155	4822 126 14305	100nF 10% 16V 0603
2156	2238 586 59812	0603 50V 100NP80M
2157	5322 126 11583	10nF 10% 50V 0603
2158	4822 126 14305	100nF 10% 16V 0603
2159	2238 586 59812	0603 50V 100NP80M
2160	4822 126 14305	100nF 10% 16V 0603
2161	4822 126 14305	100nF 10% 16V 0603
2165	5322 126 11583	10nF 10% 50V 0603
2167	4822 126 13881	470pF 5% 50V
2168	4822 122 31765	100pF 2% 63V 1206
2169	5322 126 11583	10nF 10% 50V 0603
2170	5322 126 11583	10nF 10% 50V 0603
2171	4822 126 13879	220nF 20% 16V
2173	5322 126 11583	10nF 10% 50V 0603
2174	4822 126 14305	100nF 10% 16V 0603
2175	3198 017 41050	0603 10V 1µF COL R
2177	5322 126 11583	10nF 10% 50V 0603
2179	5322 126 11583	10nF 10% 50V 0603
2180	4822 126 14305	100nF 10% 16V 0603

-III-

3135	4822 117 12063	NTC DC 5W 10k 5%
3136	4822 051 30472	4k7 5% 0.062W
3137	4822 051 30472	4k7 5% 0.062W
3138	4822 051 30103	10k 5% 0.062W

3139	4822 051 30391	390Ω 5% 0.062W
3140	4822 051 30221	220Ω 5% 0.062W
3141	4822 051 30472	4k7 5% 0.062W
3142	4822 117 12925	47k 1% 0.063W 0603
3143	4822 051 30103	10k 5% 0.062W
3144	4822 051 30391	390Ω 5% 0.062W
3145	4822 051 30103	10k 5% 0.062W
3146	4822 051 30103	10k 5% 0.062W
3147	4822 051 30103	10k 5% 0.062W
3148	4822 051 30222	2k2 5% 0.062W
3149	4822 051 30472	4k7 5% 0.062W
3150	4822 051 30562	5k6 5% 0.063W 0603 RC21 RST SM
3151	4822 051 30102	1k 5% 0.062W
3152	4822 116 52257	22k 5% 0.5W
3153	2322 704 65608	RST SM 603 RC22H 5Ω6 PM1
3154	4822 050 21003	10k 1% 0.6W
3155	4822 051 30222	2k2 5% 0.062W
3156	4822 050 21003	10k 1% 0.6W
3157	4822 116 83884	47k 5% 0.5W
3158	4822 051 30223	2k2 5% 0.062W
3159	4822 051 30562	5k6 5% 0.063W 0603 RC21 RST SM
3160	2322 704 65608	RST SM 603 RC22H 5Ω6 PM1
3161	4822 051 30683	68k 5% 0.062W
3162	4822 051 30683	68k 5% 0.062W
3163	4822 051 30103	10k 5% 0.062W
3164	4822 050 21003	10k 1% 0.6W
3165	4822 051 30222	2k2 5% 0.062W
3166	4822 116 83876	270Ω 5% 0.5W
3167	4822 116 83876	270Ω 5% 0.5W
3168	4822 116 52175	100Ω 5% 0.5W
3169	4822 051 30103	10k 5% 0.062W
3171	4822 051 30222	2k2 5% 0.062W
3172	4822 051 30472	4k7 5% 0.062W
3173	4822 051 30103	10k 5% 0.062W
3174	4822 051 30475	4M7 5% 0.062W
3177	4822 051 30102	1k 5% 0.062W
3178	4822 051 30222	2k2 5% 0.062W
3180	4822 051 30103	10k 5% 0.062W
3182	4822 051 30152	1k5 5% 0.062W
3183	4822 051 30222	2k2 5% 0.062W
3186	4822 051 30102	1k 5% 0.062W
3187	4822 051 30222	2k2 5% 0.062W
3188	4822 051 30472	4k7 5% 0.062W
3189	4822 051 30103	10k 5% 0.062W
3190	4822 117 12925	47k 1% 0.063W 0603
3192	4822 051 30102	1k 5% 0.062W
3193	4822 051 30103	10k 5% 0.062W
3194	4822 051 30222	2k2 5% 0.062W
3197	4822 051 30472	4k7 5% 0.062W
3999	4822 117 12842	

5150	4822 157 51462	10μH 10% 4X9.8MM LAL04T100K
5151	4822 157 51462	10μH 10% 4X9.8MM LAL04T100K
5153	2422 531 02423	TRANSFORMER HEATER



6140	9322 140 17676	LED VS LTL-14CHJ(LITO)A
6150	9322 129 38685	DIO REG SM BZM55-C6V8 (TEGO)

6151	4822 130 83757	MCL4148
6152	9340 260 20115	DIO SIG SM BAW56W(PHSE) R
6154	9322 102 64685	DIO REG SM UDZ2.7B (RHM0) R
6155	9340 260 20115	DIO SIG SM BAW56W(PHSE) R

6156	4822 130 83757	MCL4148
6157	4822 130 30621	1N4148
6158	4822 130 30621	1N4148
6159	4822 130 30621	1N4148
6160	9340 260 20115	DIO SIG SM BAW56W(PHSE) R
6161	9340 260 20115	DIO SIG SM BAW56W(PHSE) R

6164	4822 130 30621	1N4148
6165	4822 130 30621	1N4148
6166	4822 130 30621	1N4148
6167	4822 130 30621	1N4148
6168	9340 260 20115	DIO SIG SM BAW56W(PHSE) R

6169	9340 260 20115	DIO SIG SM BAW56W(PHSE) R
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6170	9340 260 20115	DIO SIG SM BAW56W(PHSE) R
6171	9340 260 20115	DIO SIG SM BAW56W(PHSE) R
6172	9340 260 20115	DIO SIG SM BAW56W(PHSE) R
6173	9340 260 20115	DIO SIG SM BAW56W(PHSE) R
6174	9340 260 20115	DIO SIG SM BAW56W(PHSE) R
6175	4822 130 30621	1N4148
6176	4822 130 30621	1N4148
6177	4822 130 30621	1N4148
6178	4822 130 30621	1N4148
6179	4822 130 30621	1N4148
6180	4822 130 30621	1N4148
6181	4822 130 30621	1N4148
6182	4822 130 30621	1N4148
6183	4822 130 30621	1N4148
6184	4822 130 30621	1N4148
6185	4822 130 30621	1N4148
6186	4822 130 30621	1N4148
6187	4822 130 30621	1N4148
6188	4822 130 30621	1N4148
6189	4822 130 30621	1N4148
6190	4822 130 30621	1N4148
6191	4822 130 30621	1N4148
6192	4822 130 30621	1N4148
6193	4822 130 30621	1N4148
6194	4822 130 30621	1N4148
6195	4822 130 30621	1N4148
6196	4822 130 30621	1N4148
6197	4822 130 30621	1N4148
6198	4822 130 83757	MCL4148



7140	9322 155 22667	REMOTE RECEIVER TSOP2236ZC1
7141	4822 130 61553	DTC124EU
7142	9340 217 70115	TRA SIG SM BC847BW (PHSE) R
7143	9340 218 50115	TRA SIG SM BC857BW (PHSE) R
7144	9340 218 50115	TRA SIG SM BC857BW (PHSE) R
7145	9340 217 70115	TRA SIG SM BC847BW (PHSE) R
7150	2722 171 07721	VFD BJ-801GNK 120X32
7151	9340 217 70115	TRA SIG SM BC847BW (PHSE) R
7152	9322 148 79668	FET POW SM STN3NE06(ST00)
7153	9340 217 70115	TRA SIG SM BC847BW (PHSE) R
7155	9340 217 70115	TRA SIG SM BC847BW (PHSE) R
7156	3103 178 56451	OTPROM ASSY DDCP1-1U
7157	9340 217 70115	TRA SIG SM BC847BW (PHSE) R
7160	5322 209 11147	HEF4093BT
7164	9340 217 70115	TRA SIG SM BC847BW (PHSE) R
7165	4822 130 61553	DTC124EU
7166	9340 217 70115	TRA SIG SM BC847BW (PHSE) R

Front con PWB

Various

1910	2422 033 00355	YKC22-0489
1911	2422 025 10185	CON BM H 9P M 2.00 PH B



2102	4822 126 14241	0603 50V 330P COL R
2105	4822 126 14241	0603 50V 330P COL R
2106	4822 126 14305	100nF 10% 16V 0603



3101	4822 051 30102	1k 5% 0.062W
3102	4822 051 30105	1M 5% 0.062W
3106	4822 051 30102	1k 5% 0.062W
3107	4822 051 30105	1M 5% 0.062W
3110	4822 051 30151	150Ω 5% 0.062W
3111	4822 051 30759	75Ω 5% 0.062W
3112	4822 051 30759	75Ω 5% 0.062W
3113	4822 051 30759	75Ω 5% 0.062W



6100	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6101	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6102	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6103	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ
6104	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ

Analog PWB

Various

1324▲	2422 086 10954	PROT DEV 65V 1A PSC
1325▲	2422 086 10951	PROT DEV 65V 500MA PSC
1326▲	2422 086 10954	PROT DEV 65V 1A PSC
1327▲	2422 086 10951	PROT DEV 65V 500MA PSC
1600	4822 242 10434	L1101-95263- 0E1(18,432MHz) OFWK3953M
1700	4822 242 81436	OFWK3953M
1701	4822 242 10307	OFWK3956M
1702	2422 549 44341	FIL SAW 38MHz 9 OFWK9656M
1703	4822 242 72586	TPS5_5MB-TF20
1705	3139 147 17001	TUNER UV1316MK3(NON EURO)
1802	4822 242 70938	TA252E00 (32,768KHZ)
1900	4822 265 11154	52030-2210 (22P)
1910	2422 033 00355	YKC22-0489
1911	2422 025 10185	CON BM H 9P M 2.00 PH B
1932	2422 025 11244	CON BM V 07P M 2.50 EH B
1943	9322 155 28667	OPT FIB CON GP1FA550TZ (SRP)JL
1945	2422 026 05197	CON BM CINCH H 1P F BK B
1950	2422 033 00334	CON BM EURO H 42P F BK GRND-L
1953	2422 025 10769	CON BMT 9P VERT PH-B
1954	4822 265 11154	52030-2210 (22P)
1955	2422 026 05046	CON BM MDIN 8P F TCX0310B
1958	2422 026 05093	CON BM CINCH 4P F 2*WHRD
1959	2422 026 05096	CON BM CINCH H 2P F YEYE
1960	4822 267 10565	4P
1982	4822 267 11031	10P. FEM. V
1983▲	2422 086 10919	PROT DEV 65V 125MA MP13
1984	2412 020 00724	CON BM V 2P M 2.50 EH B
1987	2422 025 10772	CON BM V 12P M 2.00 PH B
1990	4822 242 73552	13,875 000 MHz
1994	4822 242 10956	20MHz 20P AT-49



2000	4822 126 14494	22nF 10% 25V 0603
2002	4822 126 14241	0603 50V 330P COL R
2003	4822 126 14494	22nF 10% 25V 0603
2004	4822 124 40433	47μF 20% 25V
2005	4822 126 14305	100nF 10% 16V 0603
2006	4822 124 40433	47μF 20% 25V
2007	4822 126 13883	220pF 5% 50V
2008	4822 126 14241	0603 50V 330P COL R
2009	4822 126 14305	100nF 10% 16V 0603
2010	4822 126 14305	100nF 10% 16V 0603
2011	4822 124 40433	47μF 20% 25V
2012	4822 126 14305	100nF 10% 16V 0603
2013	4822 124 80151	47μF 16V
2014	4822 126 14305	100nF 10% 16V 0603
2015	4822 124 40433	47μF 20% 25V
2016	4822 126 14305	100nF 10% 16V 0603
2017	4822 124 80151	47μF 16V
2018	4822 126 13883	220pF 5% 50V
2019	4822 126 14305	100nF 10% 16V 0603
2024	4822 122 33777	47pF 5% 63V
2030	4822 124 41584	100μF 20% 10V
2102	4822 126 14241	0603 50V 330P COL R
2105	4822 126 14241	0603 50V 330P COL R
2106	4822 126 14305	100nF 10% 16V 0603
2321	4822 126 14305	100nF 10% 16V 0603
2322	4822 126 14305	100nF 10% 16V 0603
2323	3198 017 34730	0603 16V 47nF COL
2324	2020 552 96327	16V 330nF PM10
2325	4822 126 14305	100nF 10% 16V 0603
2328	4822 124 41584	100μF 20% 10V
2329	3198 017 44740	0603 10V 470nF COL

2331	4822 124 40196	220µF 20% 16V	2601	5322 126 11583	10nF 10% 50V 0603	2991	4822 124 40433	47µF 20% 25V
2332	4822 124 12095	100µF 20% 16V	2602	4822 124 40248	10µF 20% 63V	2992	4822 126 14305	100nF 10% 16V 0603
2400	5322 126 11583	10nF 10% 50V 0603	2603	4822 126 14305	100nF 10% 16V 0603	2993	4822 126 14305	100nF 10% 16V 0603
2401	4822 126 14305	100nF 10% 16V 0603	2604	5322 126 11583	10nF 10% 50V 0603	2994	4822 126 14305	100nF 10% 16V 0603
2402	4822 126 14305	100nF 10% 16V 0603	2605	4822 124 23002	10µF 16V	2995	4822 122 33761	22pF 5% 50V
2403	4822 124 40433	47µF 20% 25V	2606	5322 126 11583	10nF 10% 50V 0603	2996	4822 122 33761	22pF 5% 50V
2404	5322 126 11583	10nF 10% 50V 0603	2607	4822 126 14225	56pF 5% 50V 0603			
2405	5322 126 11583	10nF 10% 50V 0603	2608	4822 124 40248	10µF 20% 63V			
2406	5322 126 11578	1nF 10% 50V 0603	2609	4822 126 14225	56pF 5% 50V 0603			
2407	4822 126 14305	100nF 10% 16V 0603	2610	5322 126 11583	10nF 10% 50V 0603			
2408	5322 126 11578	1nF 10% 50V 0603	2612	4822 124 40769	4.7µF 20% 100V			
2410	5322 126 11583	10nF 10% 50V 0603	2614	3198 030 82280	EL SM 50V 2U2 PM20 COL R			
2411	5322 126 11583	10nF 10% 50V 0603						
2430	5322 126 11583	10nF 10% 50V 0603	2615	3198 030 82280	EL SM 50V 2U2 PM20 COL R			
2431	4822 124 40433	47µF 20% 25V						
2432	5322 126 11583	10nF 10% 50V 0603	2620	3198 016 33380	0603 50V 3P3 COL			
2433	4822 124 81151	22µF 50V	2621	3198 016 33380	0603 50V 3P3 COL			
2434	4822 124 40207	100µF 20% 25V	2622	4822 124 40248	10µF 20% 63V			
2436	5322 124 41945	22µF 20% 35V	2623	5322 126 11583	10nF 10% 50V 0603			
2437	4822 126 14305	100nF 10% 16V 0603	2624	3198 030 82280	EL SM 50V 2U2 PM20 COL R			
2438	4822 126 14305	100nF 10% 16V 0603						
2439	4822 124 81151	22µF 50V	2625	3198 030 82280	EL SM 50V 2U2 PM20 COL R			
2440	4822 124 40207	100µF 20% 25V						
2441	4822 124 81151	22µF 50V	2700	4822 124 81151	22µF 50V			
2442	4822 124 11947	10µF 20% 16V	2701	5322 122 33861	120pF 10% 50V			
2443	4822 124 11947	10µF 20% 16V	2702	4822 126 13883	220pF 5% 50V			
2446	4822 126 13881	470pF 5% 50V	2703	5322 124 41379	2.2µF 20% 50V			
2447	4822 126 13881	470pF 5% 50V	2704	4822 126 13881	470pF 5% 50V			
2460	4822 124 40433	47µF 20% 25V	2705	4822 126 14305	100nF 10% 16V 0603			
2461	4822 124 40769	4.7µF 20% 100V	2706	4822 126 14305	100nF 10% 16V 0603			
2462	4822 124 40433	47µF 20% 25V	2707	5322 126 11583	10nF 10% 50V 0603			
2463	4822 124 40769	4.7µF 20% 100V	2708	4822 124 40248	10µF 20% 63V			
2464	4822 126 14305	100nF 10% 16V 0603	2709	4822 126 13879	220nF 20% 16V			
2465	4822 126 14305	100nF 10% 16V 0603	2710	2020 552 94523	0603 50V 8P2 PM0P5			
2466	5322 126 11583	10nF 10% 50V 0603	2711	5322 126 11578	1nF 10% 50V 0603			
2467	4822 126 13881	470pF 5% 50V	2712	5322 126 11578	1nF 10% 50V 0603			
2468	4822 126 13881	470pF 5% 50V	2713	3198 024 44730	47nF 50V 0603			
2469	3198 017 41050	0603 10V 1µF COL R	2714	4822 124 22652	2.2µF 20% 50V			
2470	4822 126 14305	100nF 10% 16V 0603	2715	5322 126 11578	1nF 10% 50V 0603			
2473	4822 122 33753	150pF 5% 50V	2716	4822 124 41584	100µF 20% 10V			
2474	4822 126 14305	100nF 10% 16V 0603	2717	4822 124 22652	2.2µF 20% 50V			
2477	4822 126 14305	100nF 10% 16V 0603	2718	4822 124 40433	47µF 20% 25V			
2481	2222 867 15339	0603 50V 33P PM5	2800	3198 017 44740	0603 10V 470nF COL			
2483	3198 017 41050	0603 10V 1µF COL R	2801	4822 126 14238	0603 50V 2N2 COL R			
2484	5322 126 11578	1nF 10% 50V 0603	2802	4822 126 13482	470nF 80/20% 16V			
2500	4822 126 14305	100nF 10% 16V 0603	2803	4822 126 13883	220pF 5% 50V			
2501	4822 126 14305	100nF 10% 16V 0603	2806	3198 017 44740	0603 10V 470nF COL			
2502	4822 124 40769	4.7µF 20% 100V	2807	4822 126 13482	470nF 80/20% 16V			
2503	4822 124 40769	4.7µF 20% 100V	2810	5322 126 11578	1nF 10% 50V 0603			
2505	4822 126 14305	100nF 10% 16V 0603	2811	4822 124 11968	220mF 20% 5.5V			
2506	4822 126 14305	100nF 10% 16V 0603	2812	4822 126 14305	100nF 10% 16V 0603			
2507	4822 126 14305	100nF 10% 16V 0603	2814	5322 126 11583	10nF 10% 50V 0603			
2508	4822 124 40433	47µF 20% 25V	2815	4822 126 14507	18pF 5% 50V 0603			
2509	4822 124 40769	4.7µF 20% 100V	2816	3198 017 41050	0603 10V 1µF COL R			
2510	4822 124 40433	47µF 20% 25V	2817	5322 126 11578	1nF 10% 50V 0603			
2511	4822 122 33777	47pF 5% 63V	2818	5322 126 11583	10nF 10% 50V 0603			
2512	4822 122 33777	47pF 5% 63V	2819	3198 017 44740	0603 10V 470nF COL			
2513	4822 126 14305	100nF 10% 16V 0603	2820	3198 017 44740	0603 10V 470nF COL			
2514	4822 126 14305	100nF 10% 16V 0603	2821	2020 552 96305	4U7 20% 10V			
2515	4822 124 40769	4.7µF 20% 100V	2822	2020 552 96305	4U7 20% 10V			
2516	3198 017 41050	0603 10V 1µF COL R	2823	4822 126 14305	100nF 10% 16V 0603			
2517	3198 017 41050	0603 10V 1µF COL R	2831	4822 124 40433	47µF 20% 25V			
2518	3198 017 41050	0603 10V 1µF COL R	2832	4822 126 14305	100nF 10% 16V 0603			
2519	3198 017 41050	0603 10V 1µF COL R	2900	5322 126 11583	10nF 10% 50V 0603			
2520	4822 124 41584	100µF 20% 10V	2901	4822 124 80151	47µF 16V			
2521	4822 126 14305	100nF 10% 16V 0603	2902	4822 126 14305	100nF 10% 16V 0603			
2522	3198 017 41050	0603 10V 1µF COL R	2903	4822 126 13879	220nF 20% 16V			
2523	4822 126 14305	100nF 10% 16V 0603	2904	3198 017 41050	0603 10V 1µF COL R			
2524	3198 017 41050	0603 10V 1µF COL R	2905	4822 124 40433	47µF 20% 25V			
2525	3198 017 41050	0603 10V 1µF COL R	2906	4822 126 14305	100nF 10% 16V 0603			
2526	4822 126 14305	100nF 10% 16V 0603	2907	5322 126 11583	10nF 10% 50V 0603			
2527	4822 126 14305	100nF 10% 16V 0603	2909	4822 126 14305	100nF 10% 16V 0603			
2528	3198 017 41050	0603 10V 1µF COL R	2910	4822 126 11669	27pF			
2529	4822 126 14305	100nF 10% 16V 0603	2911	2222 867 15339	0603 50V 33P PM5			
2530	3198 017 41050	0603 10V 1µF COL R	2914	4822 126 14305	100nF 10% 16V 0603			
2531	4822 126 14305	100nF 10% 16V 0603	2915	4822 126 14305	100nF 10% 16V 0603			
2532	4822 124 11947	10µF 20% 16V	2916	4822 126 14305	100nF 10% 16V 0603			
2533	4822 124 11947	10µF 20% 16V	2917	4822 126 14305	100nF 10% 16V 0603			
2534	4822 126 14305	100nF 10% 16V 0603	2918	4822 126 14305	100nF 10% 16V 0603			
2535	4822 124 11947	10µF 20% 16V	2950	4822 126 14305	100nF 10% 16V 0603			
2536	3198 017 41050	0603 10V 1µF COL R	2951	4822 124 40248	10µF 20% 63V			
2537	3198 017 41050	0603 10V 1µF COL R	2952	4822 126 14238	0603 50V 2N2 COL R			
2538	3198 017 41050	0603 10V 1µF COL R	2953	4822 126 14238	0603 50V 2N2 COL R			
2539	4822 124 11947	10µF 20% 16V	2954	4822 126 14508	180pF 5% 50V 0603			
2540	5322 126 11578	1nF 10% 50V 0603	2955	4822 126 14508	180pF 5% 50V 0603			
2541	4822 126 14305	100nF 10% 16V 0603	2956	3198 017 41050	0603 10V 1µF COL R			
2542	4822 126 13879	220nF 20% 16V	2957	3198 017 41050	0603 10V 1µF COL R			
2544	4822 126 14305	100nF 10% 16V 0603	2970	4822 124 11947	10µF 20% 16V			
2545	4822 126 13881	470pF 5% 50V	2980	4822 124 40207	100µF 20% 25V			
2546	4822 126 13881	470pF 5% 50V	2981	4822 126 14305	100nF 10% 16V 0603			
2549	3198 017 41050	0603 10V 1µF COL R	2982	4822 124 40207	100µF 20% 25V			
2550	3198 017 41050	0603 10V 1µF COL R	2983	5322 126 11583	10nF 10% 50V 0603			
2551	5322 126 11583	10nF 10% 50V 0603	2984	3198 016 31020	0603 25V 1nF			
2600	4822 124 40248	10µF 20% 63V	2990	4822 126 14305	100nF 10% 16V 0603			

3433	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM	3536	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM	3816	4822 051 30101	100Ω 5% 0.062W
3434	4822 117 12864	82k 5% 0.6W	3537	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM	3817	4822 051 30102	1k 5% 0.062W
3435	4822 117 13632	100k 1% 0603 0.62W	3538	4822 051 30102	1k 5% 0.062W	3818	4822 051 30101	100Ω 5% 0.062W
3436	4822 051 30759	75Ω 5% 0.062W	3539	4822 051 30102	1k 5% 0.062W	3819	4822 051 30101	100Ω 5% 0.062W
3437	4822 117 12864	82k 5% 0.6W	3540	5322 117 13068	82Ω 1% 0.063W 0603 RC22H	3820	4822 051 30472	4k7 5% 0.062W
3438	4822 117 13632	100k 1% 0603 0.62W	3541	4822 051 30471	470Ω 5% 0.062W	3821	4822 051 30103	10k 5% 0.062W
3439	4822 051 30471	470Ω 5% 0.062W	3542	4822 051 30151	150Ω 5% 0.062W	3822	4822 117 13632	100k 1% 0603 0.62W
3440	4822 051 30101	100Ω 5% 0.062W	3543	4822 051 30101	100Ω 5% 0.062W	3823	4822 051 30103	10k 5% 0.062W
3441	4822 117 13632	100k 1% 0603 0.62W	3544	4822 051 30472	4k7 5% 0.062W	3824	4822 051 30103	10k 5% 0.062W
3442	4822 051 30472	4k7 5% 0.062W	3545	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM	3825	4822 051 30103	10k 5% 0.062W
3443	4822 051 30479	47Ω 5% 0.062W	3546	4822 051 30102	1k 5% 0.062W	3829	4822 051 30008	0Ω jumper
3445	4822 051 30471	470Ω 5% 0.062W	3547	4822 051 30151	150Ω 5% 0.062W	3830	4822 051 30472	4k7 5% 0.062W
3446	4822 051 30101	100Ω 5% 0.062W	3548	4822 051 30101	100Ω 5% 0.062W	3831	4822 051 30103	10k 5% 0.062W
3450	4822 117 13632	100k 1% 0603 0.62W	3549	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM	3832	4822 117 13632	100k 1% 0603 0.62W
3451	4822 051 30472	4k7 5% 0.062W	3553	4822 051 30102	1k 5% 0.062W	3833	4822 051 30222	2k2 5% 0.062W
3455	4822 117 13632	100k 1% 0603 0.62W	3554	4822 051 30759	75Ω 5% 0.062W	3834	4822 051 30222	2k2 5% 0.062W
3458	4822 051 30152	1k5 5% 0.062W	3555	4822 051 30103	10k 5% 0.062W	3835	4822 051 30103	10k 5% 0.062W
3459	4822 051 30472	4k7 5% 0.062W	3556	4822 117 12925	47k 1% 0.063W 0603	3837	4822 117 13632	100k 1% 0603 0.62W
3460	4822 051 30471	470Ω 5% 0.062W	3557	4822 117 12925	47k 1% 0.063W 0603	3838	4822 051 30472	4k7 5% 0.062W
3461	4822 051 30472	4k7 5% 0.062W	3558	4822 051 30223	22k 5% 0.062W	3839	4822 051 30103	10k 5% 0.062W
3462	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR	3559	4822 051 30392	3k9 5% 0.063W 0603	3840	4822 051 30101	100Ω 5% 0.062W
3463	4822 117 13632	100k 1% 0603 0.62W	3560	4822 117 12891	220k 1% ERJ3Ω	3841	4822 051 30101	100Ω 5% 0.062W
3464	4822 117 13632	100k 1% 0603 0.62W	3561	4822 051 30332	3k3 5% 0.062W	3842	4822 051 30684	680k 5% 0.062W
3465	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR	3562	4822 051 30101	100Ω 5% 0.062W	3843	4822 051 30103	10k 5% 0.062W
3466	4822 051 30471	470Ω 5% 0.062W	3563	4822 051 30101	100Ω 5% 0.062W	3844	4822 051 30102	1k 5% 0.062W
3467	4822 051 30472	4k7 5% 0.062W	3567	4822 051 30103	10k 5% 0.062W	3845	4822 051 30472	4k7 5% 0.062W
3468	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR	3568	4822 051 30472	4k7 5% 0.062W	3846	4822 051 30102	1k 5% 0.062W
3469	4822 117 13632	100k 1% 0603 0.62W	3570	4822 117 13632	100k 1% 0603 0.62W	3847	4822 051 30332	3k3 5% 0.062W
3470	4822 117 13632	100k 1% 0603 0.62W	3600	4822 051 30103	10k 5% 0.062W	3848	4822 117 12925	47k 1% 0.063W 0603
3471	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR	3601	4822 051 30101	100Ω 5% 0.062W	3849	4822 051 30103	10k 5% 0.062W
3472	4822 051 30471	470Ω 5% 0.062W	3602	4822 051 30472	4k7 5% 0.062W	3850	4822 051 30472	4k7 5% 0.062W
3473	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM	3603	4822 051 30101	100Ω 5% 0.062W	3851	4822 051 30103	10k 5% 0.062W
3474	4822 051 30471	470Ω 5% 0.062W	3604	4822 051 30102	1k 5% 0.062W	3852	4822 051 30223	22k 5% 0.062W
3475	4822 051 30102	1k 5% 0.062W	3605	4822 051 30102	1k 5% 0.062W	3853	4822 117 13632	100k 1% 0603 0.62W
3476	5322 117 13068	82Ω 1% 0.063W 0603 RC22H	3606	4822 051 30102	1k 5% 0.062W	3854	5322 117 13018	1k0 1% 0.063W 0603 RC22H
3477	4822 117 12925	47k 1% 0.063W 0603	3607	4822 051 30102	1k 5% 0.062W	3855	4822 051 30472	4k7 5% 0.062W
3478	4822 051 30759	75Ω 5% 0.062W	3700	4822 051 30333	33k 5% 0.062W	3856	4822 117 13632	100k 1% 0603 0.62W
3479	4822 051 30472	4k7 5% 0.062W	3701	4822 051 30681	680Ω 5% 0.062W	3857	4822 051 30222	2k2 5% 0.062W
3480	4822 051 30759	75Ω 5% 0.062W	3702	4822 051 30562	5k6 5% 0.063W 0603 RC21 RST SM	3858	4822 117 13632	100k 1% 0603 0.62W
3481	4822 051 30759	75Ω 5% 0.062W	3703	4822 051 30154	150k 5% 0.062W	3859	4822 051 30223	22k 5% 0.062W
3482	4822 051 30101	100Ω 5% 0.062W	3704	4822 051 30472	4k7 5% 0.062W	3860	4822 051 30682	6k8 5% 0.062W
3483	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM	3705	4822 051 30183	18k 5% 0.062W	3861	4822 051 30103	10k 5% 0.062W
3484	4822 051 30759	75Ω 5% 0.062W	3706	4822 051 30331	330Ω 5% 0.062W	3862	4822 051 30223	22k 5% 0.062W
3485	4822 051 30102	1k 5% 0.062W	3707	4822 100 12158	22k 30%	3863	4822 051 30101	100Ω 5% 0.062W
3486	4822 051 30151	150Ω 5% 0.062W	3708	4822 051 30101	100Ω 5% 0.062W	3864	4822 051 30101	100Ω 5% 0.062W
3487	4822 051 30101	100Ω 5% 0.062W	3709	4822 051 30183	18k 5% 0.062W	3865	4822 051 30101	100Ω 5% 0.062W
3488	4822 051 30101	100Ω 5% 0.062W	3710	4822 051 30101	100Ω 5% 0.062W	3866	4822 117 12925	47k 1% 0.063W 0603
3489	4822 051 30103	10k 5% 0.062W	3711	4822 051 30008	0Ω jumper	3867	4822 051 30101	100Ω 5% 0.062W
3490	4822 051 30471	470Ω 5% 0.062W	3712	4822 051 30222	2k2 5% 0.062W	3868	4822 051 30103	10k 5% 0.062W
3492	4822 117 13632	100k 1% 0603 0.62W	3713	4822 051 30682	6k8 5% 0.062W	3869	4822 051 30332	3k3 5% 0.062W
3494	4822 051 30759	75Ω 5% 0.062W	3714	4822 051 30472	4k7 5% 0.062W	3870	4822 051 30101	100Ω 5% 0.062W
3495	4822 051 30222	2k2 5% 0.062W	3715	4822 051 30101	100Ω 5% 0.062W	3872	4822 051 30103	10k 5% 0.062W
3497	4822 051 30101	100Ω 5% 0.062W	3716	4822 051 30101	100Ω 5% 0.062W	3873	4822 051 30103	10k 5% 0.062W
3499	4822 051 30331	330Ω 5% 0.062W	3717	4822 051 30102	1k 5% 0.062W	3874	4822 051 30123	12k 5% 0.062W
3500	4822 051 30272	2k7 5% 0.062W	3718	4822 051 30472	4k7 5% 0.062W	3875	4822 051 30102	1k 5% 0.062W
3501	4822 051 30272	2k7 5% 0.062W	3719	4822 051 30472	4k7 5% 0.062W	3876	4822 051 30331	330Ω 5% 0.062W
3503	4822 051 30221	220Ω 5% 0.062W	3720	4822 051 30101	100Ω 5% 0.062W	3877	4822 051 30101	100Ω 5% 0.062W
3504	4822 051 30222	2k2 5% 0.062W	3721	4822 051 30271	270Ω 5% 0.062W	3878	4822 051 30101	100Ω 5% 0.062W
3505	4822 051 30222	2k2 5% 0.062W	3722	4822 051 30332	3k3 5% 0.062W	3879	4822 051 30103	10k 5% 0.062W
3506	4822 051 30221	220Ω 5% 0.062W	3723	4822 117 13632	100k 1% 0603 0.62W	3880	4822 051 30103	10k 5% 0.062W
3515	4822 117 13632	100k 1% 0603 0.62W	3724	4822 051 30681	680Ω 5% 0.062W	3881	4822 051 30103	10k 5% 0.062W
3516	4822 051 30471	470Ω 5% 0.062W	3725	4822 051 30472	4k7 5% 0.062W	3882	4822 117 13632	100k 1% 0603 0.62W
3517	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR	3726	4822 051 30562	5k6 5% 0.063W 0603 RC21 RST SM	3883	4822 051 30331	330Ω 5% 0.062W
3518	4822 051 30472	4k7 5% 0.062W	3727	4822 051 30272	2k7 5% 0.062W	3885	4822 051 30222	2k2 5% 0.062W
3519	4822 117 13632	100k 1% 0603 0.62W	3728	4822 051 30331	330Ω 5% 0.062W	3886	4822 051 30479	47Ω 5% 0.062W
3520	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR	3729	4822 051 30562	5k6 5% 0.063W 0603 RC21 RST SM	3887	4822 051 30474	470k 5% 0.062W
3521	4822 051 30102	1k 5% 0.062W	3730	4822 051 30562	5k6 5% 0.063W 0603 RC21 RST SM	3888	4822 051 30223	22k 5% 0.062W
3522	4822 051 30471	470Ω 5% 0.062W	3800	4822 051 30103	10k 5% 0.062W	3889	4822 051 30102	1k 5% 0.062W
3523	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR	3801	4822 051 30273	27k 5% 0.062W	3890	4822 051 30101	100Ω 5% 0.062W
3524	4822 051 30101	100Ω 5% 0.062W	3803	4822 051 30682	6k8 5% 0.062W	3892	4822 051 30103	10k 5% 0.062W
3525	4822 051 30101	100Ω 5% 0.062W	3804	4822 051 30222	2k2 5% 0.062W	3893	4822 051 30103	10k 5% 0.062W
3526	4822 117 13632	100k 1% 0603 0.62W	3805	4822 051 30222	2k2 5% 0.062W	3896	4822 051 30103	10k 5% 0.062W
3527	4822 051 30472	4k7 5% 0.062W	3807	4822 051 30008	0Ω jumper	3898	4822 051 30103	10k 5% 0.062W
3528	4822 051 30471	470Ω 5% 0.062W	3808	4822 051 30333	33k 5% 0.062W	3899	4822 051 30103	10k 5% 0.062W
3529	4822 117 13632	100k 1% 0603 0.62W	3809	4822 051 30103	10k 5% 0.062W	3900	4822 051 30103	10k 5% 0.062W
3530	2322 574 10402	VDR 0805 1M A/6V4 MAX 21VR	3810	4822 117 13632	100k 1% 0603 0.62W	3901	4822 117 12925	47k 1% 0.063W 0603
3531	4822 051 30471	470Ω 5% 0.062W	3811	4822 051 30472	4k7 5% 0.062W	3902	4822 051 30472	4k7 5% 0.062W
3532	4822 051 30471	470Ω						

0040	4822 492 63066	
0060	4822 492 63066	
0090	4822 492 63066	
0101▲	4822 265 31015	
0120▲	4822 265 11253	FUSE HOLDER 2P
1120▲	4822 253 30383	19181 (2,5A)
1520▲	4822 252 11144	19398E1(3,150A)

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2119▲	2020 554 90186	CERSAF KX 250V S 1nF PM20 A
2120▲	4822 121 10697	220nF 20% 275V
2125	2222 580 15649	EL 151 400V S 68µF PM20
2129	4822 121 70162	10nF 5% 400V
2130	4822 126 14525	47pF 5% 1KV
2131▲	2020 554 90186	CERSAF KX 250V S 1nF PM20 A
2136	4822 126 12263	220pF 10% 1KV
2139	2222 580 15649	100nF 10% 50V
2140	2222 580 15649	100nF 10% 50V
2141	4822 126 13881	470pF 5% 50V
2142	4822 122 33575	220pF 5% 63V CASE
2143	4822 126 14305	100nF 10% 16V 0603
2144	4822 126 14583	470nF 10% 16V XTR
2145	4822 126 14583	470nF 10% 16V XTR
2146	5322 122 34099	470pF 10% 63V
2147	4822 124 40248	10µF 20% 63V
2151	2222 580 15649	100nF 10% 50V
2152	4822 126 14241	0603 50V 330P COL R
2153	4822 126 13694	68pF 1% 63V
2200	4822 124 11566	47µF 20% 50V
2201	2222 580 15649	100nF 10% 50V
2210	2020 021 91657	EL YXG 16V S 680µF PM20 B
2211	4822 124 40255	100µF 20% 63V
2214	4822 124 12285	2200µF 20% 16V YXG EL
2220	4822 124 80144	220µF 20% 25V
2221	4822 124 40255	100µF 20% 63V
2223	2222 580 15649	100nF 10% 50V
2230	4822 124 40255	100µF 20% 63V
2235	2020 012 93762	EL YK 50V S 330µF PM20 B
2240	2020 021 91664	EL YXG 16V S 1000µF PM20 B
2241	4822 124 40255	100µF 20% 63V
2251	4822 126 14494	22nF 10% 25V 0603
2501	4822 126 14494	22nF 10% 25V 0603
2502	4822 124 40255	100µF 20% 63V
2506	4822 124 40255	100µF 20% 63V
2511	4822 126 14305	100nF 10% 16V 0603
2512	4822 124 40255	100µF 20% 63V
2513	2222 580 15649	100nF 10% 50V
2515	4822 124 40255	100µF 20% 63V
2520	4822 126 14494	22nF 10% 25V 0603
2521	4822 124 40255	100µF 20% 63V

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3120▲	2122 550 00147	VDR DC 1M A/423V S MAX 775V B
3122▲	4822 053 21684	680k 5% 0.5W
3125	4822 116 83866	1M 5% 0.5W
3126	4822 116 83866	1M 5% 0.5W
3127	4822 116 83874	220k 5% 0.5W
3128	4822 116 83874	220k 5% 0.5W
3131	4822 116 52195	47Ω 5% 0.5W
3132	4822 116 52195	47Ω 5% 0.5W
3133	4822 116 80676	1Ω5 5% 0.5W
3134	4822 116 80676	1Ω5 5% 0.5W
3135	4822 116 80676	1Ω5 5% 0.5W
3139	4822 117 13632	100k 1% 0603 0.62W
3140	4822 051 30272	2k7 5% 0.062W
3141	4822 116 52257	22k 5% 0.5W
3142	4822 051 30221	220Ω 5% 0.062W
3143	4822 051 30102	1k 5% 0.062W
3144	4822 051 30102	1k 5% 0.062W
3145	4822 051 20223	22k 5% 0.1W
3146	4822 116 52175	100Ω 5% 0.5W
3147	4822 051 30222	2k2 5% 0.062W
3148	4822 116 52256	2k2 5% 0.5W
3149	4822 116 52256	2k2 5% 0.5W
3150	4822 053 10689	68Ω 5% 1W
3151	4822 117 13632	100k 1% 0603 0.62W
3152	4822 116 52261	24k 5% 0.5W
3200	4822 116 52263	2k7 5% 0.5W
3201	4822 051 20333	33k 5% 0.1W
3220	4822 051 30222	2k2 5% 0.062W
3221	4822 051 30223	22k 5% 0.062W
3222	4822 051 30472	4k7 5% 0.062W
3223	4822 116 52283	4k7 5% 0.5W
3230▲	4822 052 10479	47Ω 5% 0.33W
3233	4822 117 10833	10k 1% 0.1W

3234	4822 117 10833	10k 1% 0.1W
3250	4822 116 83883	470Ω 5% 0.5W
3253	4822 117 12925	47k 1% 0.063W 0603
3254	4822 116 83883	470Ω 5% 0.5W
3255	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3256	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3501	4822 116 52256	2k2 5% 0.5W
3502	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3503	4822 051 30681	680Ω 5% 0.062W
3504	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3511	4822 051 30103	10k 5% 0.062W
3512	4822 051 20472	4k7 5% 0.1W
3513	4822 117 12925	47k 1% 0.063W 0603
3514	4822 050 21003	10k 1% 0.6W
3515	4822 117 10833	10k 1% 0.1W
3516	4822 051 30103	10k 5% 0.062W
3520	4822 051 20511	510Ω 5% 0.1W
3521	4822 051 30102	1k 5% 0.062W
3522	4822 117 11449	2k2 5% 0.1W 0805
3523	4822 051 30681	680Ω 5% 0.062W
3524	4822 051 20332	3k3 5% 0.1W
3525	5322 117 13036	1k2 1% 0.063W 0603 RC22H

5110	2422 535 94634	IND FXD LHL08 S 2U2 PM20 A
5115	2422 535 94634	IND FXD LHL08 S 2U2 PM20 A
5120▲	4822 157 11846	
5125	4822 157 70826	2.4µH
5131▲	4822 146 10402	TRAFO CT395FANF/PVF
5210	2422 535 94639	IND FXD LHL08 S 10U PM20
5240	2422 535 94632	IND FXD LHL08 S 1U PM30 A
5501	2422 535 94634	IND FXD LHL08 S 2U2 PM20 A
5505	2422 535 94639	IND FXD LHL08 S 10U PM20
5511	2422 535 94639	IND FXD LHL08 S 10U PM20
5515	2422 535 94639	IND FXD LHL08 S 10U PM20
5520	2422 535 94634	IND FXD LHL08 S 2U2 PM20 A

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6125	4822 130 42606	BYD33J
6130	5322 130 34574	1N4004G
6131	5322 130 34574	1N4004G
6132	5322 130 34574	1N4004G
6140	4822 130 30842	BAV21
6141	4822 130 83757	MCL4148
6142	4822 130 30842	BAV21
6143	4822 130 30842	BAV21
6144	9340 387 30115	DIO REG SM BZX284-C16 (PHSE) R
6145	4822 130 83757	MCL4148
6146	4822 130 83757	MCL4148
6151	4822 130 31603	1N4006
6152	4822 130 31603	1N4006
6153	4822 130 31603	1N4006
6154	4822 130 31603	1N4006
6200	4822 130 42606	BYD33J
6201	4822 130 34142	BZX79-B33
6210	4822 130 11596	BYW29EX-200
6211	5322 130 34574	1N4004G
6215	9322 161 46687	DIO REC STPS745FP (ST00) L
6220	5322 130 31938	BYV27-200
6221	4822 130 30842	BAV21
6230	4822 130 42606	BYD33J
6231	4822 130 34142	BZX79-B33
6240	4822 130 11596	BYW29EX-200
6505	4822 130 32245	BYV10-40
6511	4822 130 11666	BZX284-C8V2
6512	5322 130 34574	1N4004G
6515	4822 130 34278	BZX79-B6V8
6520	4822 130 83757	MCL4148



7125	9322 126 65687	STP5NB60FP
7140	5322 130 60159	BC846B
7141	4822 130 60373	BC856B
7142	5322 130 60159	BC846B
7143	5322 130 60159	BC846B
7200▲	9322 149 04682	OPT CP TCET1102(G) (VISH) L
7220	4822 209 72684	L7905CV
7241	4822 130 60373	BC856B
7251	4822 209 81397	TL431CLPST
7501	9322 163 53685	FET POW SM IRLML2502 (INR0) R

7502	4822 209 81397	TL431CLPST
7511	9322 163 53685	FET POW SM IRLML2502 (INR0) R
7512	5322 130 60159	BC846B
7515	9322 163 53685	FET POW SM IRLML2502 (INR0) R
7520	4822 130 11336	STP16NE06FP
7521	4822 209 81397	TL431CLPST

Dig 1.5 PWB

Various

1100	2422 025 17018	CON BM V 15P F 1.00 FFC 0.3 R
1101	2422 025 17018	CON BM V 15P F 1.00 FFC 0.3 R
1200	2422 025 16794	CON BM V 7P F 1.00 FFC 0.3 R
1500	2422 543 01115	RES XTL SM 24M576 12P CX-11F R
1600	2422 025 16729	CON BM V 10P F 1.00 FFC 0.3 R
1601	2422 025 16389	CON BM V 22P F 1.00 FFC 0.3 R
1602	2422 025 16389	CON BM V 22P F 1.00 FFC 0.3 R
1603	2422 025 16939	CON BM V 60P F 0.80 84616 R

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2100	4822 126 14305	100nF 10% 16V 0603
2101	4822 126 14305	100nF 10% 16V 0603
2102	4822 126 14305	100nF 10% 16V 0603
2103	4822 126 14305	100nF 10% 16V 0603
2104	4822 126 14305	100nF 10% 16V 0603
2105	4822 126 14305	100nF 10% 16V 0603
2106	4822 126 14305	100nF 10% 16V 0603
2107	4822 126 14305	100nF 10% 16V 0603
2108	4822 126 14305	100nF 10% 16V 0603
2109	4822 126 14305	100nF 10% 16V 0603
2110	4822 126 14305	100nF 10% 16V 0603
2111	4822 126 14305	100nF 10% 16V 0603
2112	4822 126 14305	100nF 10% 16V 0603
2113	4822 126 14305	100nF 10% 16V 0603
2114	4822 126 14305	100nF 10% 16V 0603
2115	4822 126 14305	100nF 10% 16V 0603
2116	4822 126 14305	100nF 10% 16V 0603
2117	4822 126 14305	100nF 10% 16V 0603
2118	4822 126 14305	100nF 10% 16V 0603
2119	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2120	4822 126 14305	100nF 10% 16V 0603
2121	4822 126 14305	100nF 10% 16V 0603
2122	4822 126 14305	100nF 10% 16V 0603
2123	4822 126 14305	100nF 10% 16V 0603
2124	4822 126 14305	100nF 10% 16V 0603
2125	4822 126 14305	100nF 10% 16V 0603
2126	4822 126 14305	100nF 10% 16V 0603
2127	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2128	3198 016 31020	0603 25V 1nF
2129	4822 126 13956	68pF 5% 63V CASE 0603
2130	3198 030 82280	EL SM 50V 2U2 PM20 COL R
2131	5322 124 41945	22µF 20% 35V
2132	4822 126 14305	100nF 10% 16V 0603
2135	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2136	4822 122 33777	47pF 5% 63V
2137	4822 126 14305	100nF 10% 16V 0603
2139	4822 126 14305	100nF 10% 16V 0603
2141	4822 122 33777	47pF 5% 63V
2146	4822 126 14305	100nF 10% 16V 0603
2200	3198 016 31020	0603 25V 1nF
2201	4822 126 14494	22nF 10% 25V 0603
2202	4822 126 14305	100nF 10% 16V 0603
2203	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2204	2222 867 15339	0603 50V 33P PM5
2205	4822 126 14305	100nF 10% 16V 0603
2206	4822 126 14305	100nF 10% 16V 0603
2207	2222 867 15339	0603 50V 33P PM5
2208	4822 126 14305	100nF 10% 16V 0603
2209	4822 126 14305	100nF 10% 16V 0603
2210	4822 126 14305	100nF 10% 16V 0603
2211	4822 126 14305	100nF 10% 16V 0603
2212	4822 126 14305	100nF 10% 16V 0603
2213	4822 126 14305	100nF 10% 16V 0603
2214	4822 126 14305	100nF 10% 16V 0603

3408	4822 117 12139	22Ω 5% 0.062W
3409	4822 117 12139	22Ω 5% 0.062W
3410	4822 117 12139	22Ω 5% 0.062W
3500	4822 051 30101	100Ω 5% 0.062W
3501	4822 051 30101	100Ω 5% 0.062W
3502	4822 051 30222	2k2 5% 0.062W
3503	4822 051 30102	1k 5% 0.062W
3503	4822 051 30759	75Ω 5% 0.062W
3504	4822 051 30681	680Ω 5% 0.062W
3505	4822 117 12139	22Ω 5% 0.062W
3506	4822 051 30222	2k2 5% 0.062W
3507	4822 051 30472	4k7 5% 0.062W
3508	4822 051 30103	10k 5% 0.062W
3513	4822 051 30681	680Ω 5% 0.062W
3515	4822 117 12917	1Ω 5% 0.062W CASE0603
3600	2322 704 65609	RST SM 0603 RC22H 56Ω PM1 R
3601	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3602	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3603	4822 051 30102	1k 5% 0.062W
3604	4822 051 30101	100Ω 5% 0.062W
3604	4822 117 12139	22Ω 5% 0.062W
3605	4822 117 12917	1Ω 5% 0.062W CASE0603
3606	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3607	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3608	4822 051 30102	1k 5% 0.062W
3610	4822 117 12917	1Ω 5% 0.062W CASE0603
3611	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3612	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3613	4822 051 30102	1k 5% 0.062W
3615	4822 051 30101	100Ω 5% 0.062W
3616	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3617	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3618	4822 051 30102	1k 5% 0.062W
3619	4822 051 30561	560Ω 5% 0.062W
3620	4822 051 30222	2k2 5% 0.062W
3621	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3622	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3623	4822 051 30101	100Ω 5% 0.062W
3623	4822 117 12139	22Ω 5% 0.062W
3624	4822 051 30102	1k 5% 0.062W
3625	4822 051 30101	100Ω 5% 0.062W
3625	4822 117 12139	22Ω 5% 0.062W
3626	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3627	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3628	4822 051 30102	1k 5% 0.062W
3629	4822 051 30181	180Ω 5% 0.062W
3630	4822 051 30181	180Ω 5% 0.062W
3631	4822 117 12917	1Ω 5% 0.062W CASE0603
3632	4822 051 30561	560Ω 5% 0.062W
3633	4822 051 30561	560Ω 5% 0.062W
3635	4822 051 30101	100Ω 5% 0.062W
3635	4822 117 12139	22Ω 5% 0.062W
3636	4822 051 30181	180Ω 5% 0.062W
3637	4822 051 30101	100Ω 5% 0.062W
3637	4822 117 12139	22Ω 5% 0.062W
3638	4822 051 30222	2k2 5% 0.062W
3900	4822 051 30103	10k 5% 0.062W
3901	4822 117 12139	22Ω 5% 0.062W
3902	4822 117 12925	47k 1% 0.063W 0603
3903	4822 117 13632	100k 1% 0603 0.62W
3904	4822 117 12139	22Ω 5% 0.062W
3906	4822 051 30479	47Ω 5% 0.062W
3908	4822 117 12139	22Ω 5% 0.062W
3910	4822 051 30101	100Ω 5% 0.062W
3911	4822 051 30103	10k 5% 0.062W
3913	4822 051 30682	6k8 5% 0.062W
3914	4822 051 30479	47Ω 5% 0.062W
3915	4822 051 30479	47Ω 5% 0.062W
3916	4822 117 13632	100k 1% 0603 0.62W
3917	4822 117 12139	22Ω 5% 0.062W
3918	4822 117 13632	100k 1% 0603 0.62W
3919	4822 051 30101	100Ω 5% 0.062W
3920	4822 117 12139	22Ω 5% 0.062W
3921	4822 051 30103	10k 5% 0.062W
3922	4822 051 30682	6k8 5% 0.062W
3923	4822 117 13632	100k 1% 0603 0.62W
3924	4822 051 30152	1k5 5% 0.062W
3925	4822 051 30472	4k7 5% 0.062W

5100	4822 157 11717	BLM31P500SPT
5101	4822 157 11717	BLM31P500SPT
5102	4822 157 11499	BLM11P600SPT
5103	4822 157 11499	BLM11P600SPT
5200	4822 157 11499	BLM11P600SPT
5201	4822 157 11499	BLM11P600SPT
5202	4822 157 11499	BLM11P600SPT
5203	4822 157 11499	BLM11P600SPT
5204	4822 157 11499	BLM11P600SPT
5205	4822 157 11499	BLM11P600SPT
5207	4822 157 11499	BLM11P600SPT
5208	4822 157 11499	BLM11P600SPT
5209	4822 157 11499	BLM11P600SPT
5300	4822 157 11499	BLM11P600SPT
5302	4822 157 11499	BLM11P600SPT
5400	4822 157 11499	BLM11P600SPT
5402	4822 157 11499	BLM11P600SPT
5403	4822 157 11499	BLM11P600SPT
5404	4822 157 11499	BLM11P600SPT
5500	4822 157 11499	BLM11P600SPT
5501	4822 157 11499	BLM11P600SPT
5502	4822 157 11499	BLM11P600SPT
5503	4822 157 11499	BLM11P600SPT
5504	4822 157 11499	BLM11P600SPT
5505	4822 157 11499	BLM11P600SPT
5506	4822 157 11499	BLM11P600SPT
5507	4822 157 11499	BLM11P600SPT
5508	4822 157 11499	BLM11P600SPT
5600	4822 157 70651	12μH (NL322522T-120J)
5601	4822 157 70651	12μH (NL322522T-120J)
5602	4822 157 70651	12μH (NL322522T-120J)
5603	4822 157 70651	12μH (NL322522T-120J)
5604	4822 157 70651	12μH (NL322522T-120J)
5605	4822 157 70651	12μH (NL322522T-120J)
5606	4822 157 70649	4.7μH (NL322522T-4R7J)
5607	4822 157 70649	4.7μH (NL322522T-4R7J)
5900	4822 157 11717	BLM31P500SPT
5901	4822 157 11717	BLM31P500SPT
5903	4822 157 11499	BLM11P600SPT
5904	4822 157 11717	BLM31P500SPT
5905	4822 157 11499	BLM11P600SPT
5907	4822 157 11499	BLM11P600SPT

6500	4822 130 11528	1PS76SB10
6500	4822 130 80622	BAT54
6900	4822 130 11528	1PS76SB10
6900	4822 130 80622	BAT54

7100	9352 692 48557	IC SM SAA7333HL/M1 (PHSE) Y
7101	9322 166 67668	IC SM MT48LC4M16A2TG-7E(MRNO)R
7102	5322 209 16384	PC74HCT9046AD
7103	9322 170 16685	IC SM NC7SZ58 (FSC0) R
7104	9352 456 50115	HC1G04
7200	9322 169 81671	IC SM STI5508EVB (ST00) Y
7201	9322 130 41668	IC SM M24C64-WMN6 (ST00) R
7202	4822 209 30212	PC74HCT125T
7203	9322 142 88668	IC SM LF25CDT (ST00) R
7300	9322 166 67668	IC SM MT48LC4M16A2TG-7E(MRNO)R
7303	9352 499 60118	IC SM 74LVC00AD (PHSE) R
7402	9322 166 67668	IC SM MT48LC4M16A2TG-7E(MRNO)R
7403	9352 701 80557	IC SM SAA6752HS/V101 (PHSE) Y
7404	9322 142 88668	IC SM LF25CDT (ST00) R
7500	9352 673 95518	IC SM SAA7118E/V1 (PHSE) R
7501	9352 500 60118	IC SM 74LVC32AD (PHSE) R
7502	5322 209 71589	74HC74D
7504	4822 130 60511	BC847B
7600	4822 130 60511	BC847B
7601	4822 130 60511	BC847B
7602	4822 130 60511	BC847B
7603	4822 130 60511	BC847B
7604	4822 130 60511	BC847B
7605	4822 130 60511	BC847B
7606	4822 130 60511	BC847B
7702	9352 501 00118	IC SM 74LVC86ADB (PHSE) R
7900	9322 151 71668	IC SM MK2703STR (MICL) R

7901	4822 130 60511	BC847B
7902	9322 165 15685	IC SM NCP303LSN30 (ONSE) R
7904	4822 209 16399	74LVC04AD
7905	5322 209 71568	PC74HCT14T
7906	4822 242 10838	27MHZ 120P FX0-31FT

DIVIO front DVD985 /001 /021

Various

1000	2422 033 00363	CON BM H 4P F 0.8 B
1001	2422 025 17106	CON BM H 4P F 0.8 IEEE R

-II-

2000	5322 126 10511	1nF 5% 50V
2001	5322 126 10511	1nF 5% 50V
2002	2020 557 90732	250V 4N7 PM10 R
2002	2222 580 19815	50V 330nF P8020 R
2003	2020 557 90732	250V 4N7 PM10 R
2003	2222 580 19815	50V 330nF P8020 R
2004	2020 557 90732	250V 4N7 PM10 R
2005	2020 557 90732	250V 4N7 PM10 R
2204	2222 867 15339	0603 50V 33P PM5
2205	2222 867 15339	0603 50V 33P PM5

□

3000	4822 051 20105	1M 5% 0.1W
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5000	2422 549 44768	IND FXD SM EMI 100mH z 90R R
5001	2422 549 44768	IND FXD SM EMI 100mH z 90R R

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6000	4822 130 11395	TLMH3100
6001	9322 172 97668	DIO SUP SM6T39CA (ST00) R

DIVIO PWB DVD985 /001 /021

Various

1101	2422 025 17106	CON BM H 4P F 0.8 IEEE R
1102	2422 543 01115	RES XTL SM 24M576 12P CX-11F R
1200	2422 543 01159	RES XTL SM 11M0592 20P DSX840
1500	2422 025 17084	CON BM V 60P F 0.80 179161 R

-II-

2146	4822 126 14305	100nF 10% 16V 0603
2147	4822 126 14305	100nF 10% 16V 0603
2148	4822 126 14305	100nF 10% 16V 0603
2149	4822 126 14305	100nF 10% 16V 0603
2150	4822 126 14305	100nF 10% 16V 0603
2151	4822 126 14305	100nF 10% 16V 0603
2152	4822 126 14305	100nF 10% 16V 0603
2153	4822 126 14305	100nF 10% 16V 0603
2154	4822 126 14305	100nF 10% 16V 0603
2155	4822 126 14305	100nF 10% 16V 0603
2156	4822 126 14305	100nF 10% 16V 0603
2157	4822 126 14305	100nF 10% 16V 0603
2158	3198 017 41050	0603 10V 1μF COL R
2163	4822 126 14506	270pF 5% 50V 0603
2170	4822 126 11663	12pF
2171	4822 126 11663	12pF
2173	4822 124 23002	10μF 16V
2174	4822 126 14305	100nF 10% 16V 0603
2175	4822 124 23002	10μF 16V
2176	4822 126 14305	100nF 10% 16V 0603
2177	4822 126 14305	100nF 10% 16V 0603
2178	4822 126 14305	100nF 10% 16V 0603
2181	4822 124 12095	100μF 20% 16V
2182	4822 124 23002	10μF 16V
2183	4822 126 14305	100nF 10% 16V 0603
2184	4822 126 14305	100nF 10% 16V 0603
2187	4822 126 14305	100nF 10% 16V 0603
2192	4822 126 14305	100nF 10% 16V 0603
2193	4822 126 14305	100nF 10% 16V 0603
2194	4822 126 14305	100nF 10% 16V 0603

2195	4822 126 14305	100nF 10% 16V 0603
2196	4822 126 14305	100nF 10% 16V 0603
2197	4822 126 14305	100nF 10% 16V 0603
2200	4822 126 11663	12pF
2202	4822 126 14305	100nF 10% 16V 0603
2203	4822 126 14305	100nF 10% 16V 0603
2204	4822 126 14305	100nF 10% 16V 0603
2205	4822 126 11663	12pF
2206	4822 122 31765	100pF 2% 63V 1206
2207	4822 126 14305	100nF 10% 16V 0603
2301	4822 126 14305	100nF 10% 16V 0603
2302	4822 124 80151	47µF 16V
2303	4822 126 14305	100nF 10% 16V 0603
2304	4822 126 14305	100nF 10% 16V 0603
2305	4822 126 14305	100nF 10% 16V 0603
2306	4822 126 14305	100nF 10% 16V 0603
2307	4822 126 14305	100nF 10% 16V 0603
2308	4822 126 14305	100nF 10% 16V 0603
2309	4822 126 14305	100nF 10% 16V 0603
2310	4822 126 14305	100nF 10% 16V 0603
2311	4822 126 14305	100nF 10% 16V 0603
2312	4822 126 14305	100nF 10% 16V 0603
2313	4822 126 14305	100nF 10% 16V 0603
2314	4822 124 80151	47µF 16V
2318	4822 126 14305	100nF 10% 16V 0603
2319	4822 126 14305	100nF 10% 16V 0603
2324	4822 126 14305	100nF 10% 16V 0603
2325	4822 126 14305	100nF 10% 16V 0603
2330	4822 126 14305	100nF 10% 16V 0603
2331	4822 126 14305	100nF 10% 16V 0603
2332	4822 126 14305	100nF 10% 16V 0603
2400	4822 126 14305	100nF 10% 16V 0603
2401	4822 126 14305	100nF 10% 16V 0603
2402	4822 126 14305	100nF 10% 16V 0603
2403	4822 126 14305	100nF 10% 16V 0603
2404	4822 126 14305	100nF 10% 16V 0603
2405	4822 126 14305	100nF 10% 16V 0603
2406	4822 126 14305	100nF 10% 16V 0603
2407	4822 126 14305	100nF 10% 16V 0603
2408	4822 126 14305	100nF 10% 16V 0603
2409	4822 126 14305	100nF 10% 16V 0603
2410	4822 126 14305	100nF 10% 16V 0603
2411	4822 126 14305	100nF 10% 16V 0603
2412	4822 126 14305	100nF 10% 16V 0603
2413	4822 126 14305	100nF 10% 16V 0603
2414	4822 126 14305	100nF 10% 16V 0603
2415	4822 126 14305	100nF 10% 16V 0603
2416	4822 126 14305	100nF 10% 16V 0603
2417	4822 126 14305	100nF 10% 16V 0603
2418	4822 126 14305	100nF 10% 16V 0603
2419	4822 126 14305	100nF 10% 16V 0603
2420	4822 126 14305	100nF 10% 16V 0603
2421	4822 126 14305	100nF 10% 16V 0603
2500	4822 126 14305	100nF 10% 16V 0603
2501	4822 126 14305	100nF 10% 16V 0603
2502	4822 126 14305	100nF 10% 16V 0603
2503	4822 126 14305	100nF 10% 16V 0603
2504	4822 126 14305	100nF 10% 16V 0603
2505	4822 124 80151	47µF 16V
2506	4822 126 14305	100nF 10% 16V 0603
2507	4822 124 80151	47µF 16V
2508	4822 126 14305	100nF 10% 16V 0603
2509	4822 126 14305	100nF 10% 16V 0603
2510	4822 126 14305	100nF 10% 16V 0603
2511	4822 124 80151	47µF 16V
2512	4822 124 80151	47µF 16V
2514	4822 124 80151	47µF 16V
2515	4822 124 80151	47µF 16V
2516	5322 126 11583	10nF 10% 50V 0603
2517	5322 126 11583	10nF 10% 50V 0603
2518	4822 124 80151	47µF 16V
2519	4822 126 14305	100nF 10% 16V 0603



3100	4822 117 12925	47k 1% 0.063W 0603
3101	4822 117 12925	47k 1% 0.063W 0603
3102	4822 051 30103	10k 5% 0.062W
3103	4822 051 30103	10k 5% 0.062W
3104	4822 117 12925	47k 1% 0.063W 0603
3105	4822 051 30109	10Ω 5% 0.062W
3106	4822 051 30103	10k 5% 0.062W
3107	4822 051 30109	10Ω 5% 0.062W
3108	4822 051 30109	10Ω 5% 0.062W
3109	4822 117 12925	47k 1% 0.063W 0603
3110	4822 117 12925	47k 1% 0.063W 0603
3113	4822 051 30103	10k 5% 0.062W
3115	4822 051 30102	1k 5% 0.062W
3116	4822 117 12917	1Ω 5% 0.062W CASE0603
3117	4822 051 30109	10Ω 5% 0.062W
3118	4822 117 12925	47k 1% 0.063W 0603
3119	4822 117 12925	47k 1% 0.063W 0603
3120	4822 117 12925	47k 1% 0.063W 0603

3121	4822 117 12925	47k 1% 0.063W 0603
3122	4822 117 12925	47k 1% 0.063W 0603
3123	4822 117 12925	47k 1% 0.063W 0603
3124	4822 117 12925	47k 1% 0.063W 0603
3125	4822 117 12925	47k 1% 0.063W 0603
3126	4822 117 12925	47k 1% 0.063W 0603
3127	4822 117 12925	47k 1% 0.063W 0603
3128	4822 117 12925	47k 1% 0.063W 0603
3130	4822 117 12925	47k 1% 0.063W 0603
3131	4822 117 12925	47k 1% 0.063W 0603
3132	4822 117 12925	47k 1% 0.063W 0603
3133	4822 051 30223	22k 5% 0.062W
3134	4822 051 30223	22k 5% 0.062W
3136	4822 117 12917	1Ω 5% 0.062W CASE0603
3138	4822 051 30103	10k 5% 0.062W
3140	4822 051 30103	10k 5% 0.062W
3148	2322 704 66342	RST SM 0603 RC22H 6k34 PM1 R
3163	4822 051 30008	0Ω jumper
3164	2322 734 65609	RST SM 0805 RC12H 56Ω PM1 R
3165	2322 734 65609	RST SM 0805 RC12H 56Ω PM1 R
3171	4822 051 30109	10Ω 5% 0.062W
3172	4822 051 30109	10Ω 5% 0.062W
3173	2322 734 65609	RST SM 0805 RC12H 56Ω PM1 R
3174	4822 051 30109	10Ω 5% 0.062W
3176	4822 051 30109	10Ω 5% 0.062W
3177	2322 704 65102	RST SM 0603 RC22H 5k1 PM1
3178	2322 734 65609	RST SM 0805 RC12H 56Ω PM1 R
3179	4822 051 30103	10k 5% 0.062W
3188	4822 051 30479	47Ω 5% 0.062W
3189	4822 051 30109	10Ω 5% 0.062W
3190	4822 051 30479	47Ω 5% 0.062W
3191	4822 051 30109	10Ω 5% 0.062W
3192	4822 117 12925	47k 1% 0.063W 0603
3197	4822 117 12925	47k 1% 0.063W 0603
3198	4822 117 12925	47k 1% 0.063W 0603
3199	4822 117 12925	47k 1% 0.063W 0603
3201	4822 051 30479	47Ω 5% 0.062W
3202	4822 051 30103	10k 5% 0.062W
3203	4822 051 30102	1k 5% 0.062W
3204	4822 051 30103	10k 5% 0.062W
3205	4822 117 12925	47k 1% 0.063W 0603
3206	4822 117 12925	47k 1% 0.063W 0603
3223	4822 051 30472	4k7 5% 0.062W
3224	4822 051 30331	330Ω 5% 0.062W
3225	4822 051 30109	10Ω 5% 0.062W
3300	4822 051 30109	10Ω 5% 0.062W
3301	4822 051 30102	1k 5% 0.062W
3303	4822 051 30102	1k 5% 0.062W
3305	4822 051 30102	1k 5% 0.062W
3306	4822 051 30102	1k 5% 0.062W
3307	4822 051 30102	1k 5% 0.062W
3312	4822 051 30109	10Ω 5% 0.062W
3313	4822 051 30103	10k 5% 0.062W
3314	4822 051 30103	10k 5% 0.062W
3315	4822 051 30339	33Ω 5% 0.062W
3317	4822 051 30339	33Ω 5% 0.062W
3318	4822 051 30339	33Ω 5% 0.062W
3319	4822 051 30339	33Ω 5% 0.062W
3320	4822 051 30479	47Ω 5% 0.062W
3321	4822 051 30479	47Ω 5% 0.062W
3322	4822 051 30479	47Ω 5% 0.062W
3325	4822 051 30479	47Ω 5% 0.062W
3327	4822 051 30479	47Ω 5% 0.062W
3328	4822 051 30103	10k 5% 0.062W
3329	4822 051 30103	10k 5% 0.062W
3330	4822 051 30479	47Ω 5% 0.062W
3331	4822 051 30479	47Ω 5% 0.062W
3400	4822 051 30103	10k 5% 0.062W
3401	4822 117 13573	NETW 4 X 47Ω 5% MNR14
3402	4822 117 13573	NETW 4 X 47Ω 5% MNR14
3403	4822 051 30479	47Ω 5% 0.062W
3404	4822 051 30479	47Ω 5% 0.062W
3405	4822 051 30479	47Ω 5% 0.062W
3502	4822 051 30339	33Ω 5% 0.062W
3504	4822 117 13576	NETW 4 X 33Ω 5% 1206
3505	4822 117 13576	NETW 4 X 33Ω 5% 1206
3506	4822 051 30339	33Ω 5% 0.062W
3510	4822 051 30479	47Ω 5% 0.062W
3511	4822 051 30008	0Ω jumper
3518	4822 051 30101	100Ω 5% 0.062W
3519	4822 051 30101	100Ω 5% 0.062W
3520	4822 117 12891	220k 1% ERJ3Ω
3521	4822 117 12891	220k 1% ERJ3Ω
3524	4822 051 30339	33Ω 5% 0.062W
3525	4822 051 30339	33Ω 5% 0.062W
3526	4822 051 30339	33Ω 5% 0.062W
3527	4822 051 30339	33Ω 5% 0.062W



5103	4822 157 11499	BLM11P600SPT
5106	4822 157 11499	BLM11P600SPT
5109	4822 157 11499	BLM11P600SPT
5110	4822 157 11499	BLM11P600SPT
5200	4822 157 11499	BLM11P600SPT
5300	4822 157 11499	BLM11P600SPT
5301	4822 157 11499	BLM11P600SPT
5302	4822 157 11499	BLM11P600SPT
5303	4822 157 11499	BLM11P600SPT
5304	4822 157 11499	BLM11P600SPT
5402	4822 157 11499	BLM11P600SPT
5403	4822 157 11499	BLM11P600SPT
5404	4822 157 11499	BLM11P600SPT
5500	4822 157 11499	BLM11P600SPT
5501	4822 157 11499	BLM11P600SPT
5502	4822 157 11499	BLM11P600SPT
5503	4822 157 11499	BLM11P600SPT



6300	4822 209 17398	LD1117DT33
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7101	9352 683 02157	IC SM PDI1394P25BD (PHSE) Y
7103	9352 682 52557	IC SM PDI1394L40 (PHSE) Y
7201	4822 209 91023	UM62256EM-70LL
7202	4822 130 60511	BC847B
7204	9337 331 10215	FET SIG SM BST82 (PHSE) R
7207	4822 130 60511	BC847B
7208	9352 456 40115	IC SM 74HCT1G04GW (PHSE) R
7300	3104 123 96640	IC ROM XC17S30XL DVIO 1.5
7301	9322 166 64668	IC SM CY7C1019BV33-10VC(CYPR)
7303	9322 169 90671	IC SM XC530XL-4TQ144C (XLI) Y
7304	4822 242 10838	27MHZ 120P FX0-31FT
7307	3104 123 96620	IC FLASH PLL CY2071A DVIO 1.5
7308	3104 123 96620	IC FLASH PLL CY2071A DVIO 1.5
7309	3104 123 96630	IC FLASH XC18V01 DVIO 1.5
7402	8204 056 07210	IC SM MT4LC1M16E5DJ-6
7402	9322 178 74668	MT4LC1M16E5DJ-6
7403	8204 056 07210	IC SM MT4LC1M16E5DJ-6
7403	9322 178 74668	MT4LC1M16E5DJ-6
7404	8204 056 07160	IC SM NW700LQ TQFP160
7404	9322 179 31671	IC SM NW700L
7500	9352 424 20118	IC SM 74LVC04APW (PHSE) R
7505	9352 351 50118	IC SM 74LVC16244ADGG (PHSE) R
7506	9352 668 39118	IC SM UDA1334ATS/N2 (PHSE) R