digital

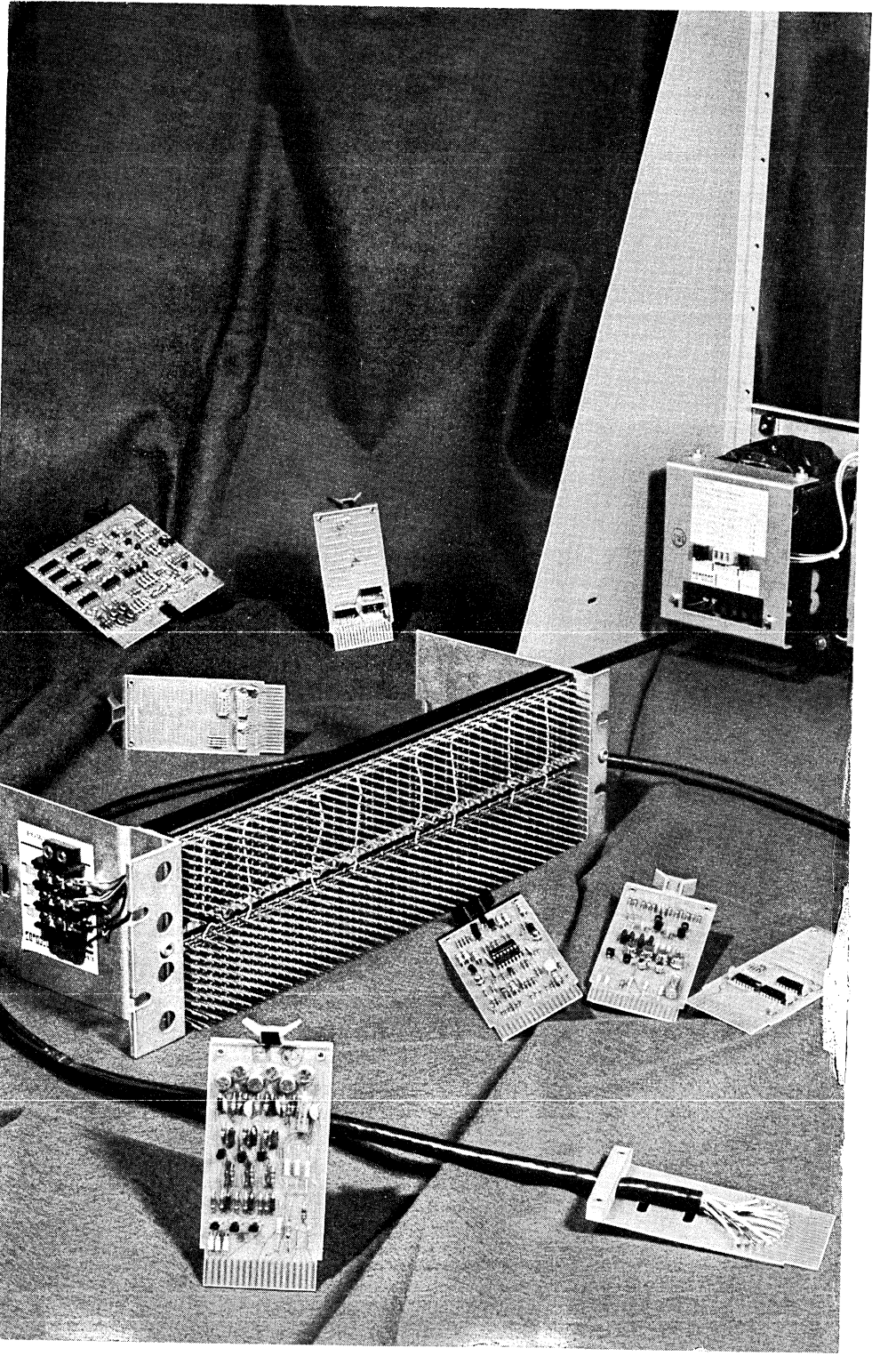
LOGIC HANDBOOK

Modules

Hardware

Applications

Positive Logic Edition



THE

LOGIC HANDBOOK
FLIP CHIP™ MODULES
1969 EDITION

POSITIVE LOGIC EDITION

FOREWORD

This fifth edition of the Logic Handbook is your guide to the most extensive array of logic capabilities, hardware and applications information ever offered by Digital Equipment Corporation. Here you will find a wealth of useful information on the latest techniques and products available for implementing your electronic logic designs for instrumentation computer interfacing, data gathering, or control. The handbook is a basic reference for anyone involved in specifying, designing, manufacturing or using solid state logic.

The Products

Two of our major module lines are featured in this edition: M Series TTL integrated circuit modules and K Series low-speed noise-immune logic. The M Series line has now been expanded to over 60 modules. In addition to a comprehensive array of basic logic and functional modules, the general-purpose M Series line now offers seven new computer interfacing modules to augment its already broad interfacing capabilities. The K Series product offering has also been expanded, and now comprises nearly 60 modules, all compatible with M Series. Complementing its basic logic, expanded K Series offers specialized functional modules such as sensor converters, communications interfaces, 120 V ac interfaces, drivers for solenoids and motors, and logic level converters for tying either high-speed or noise-sensitive logic to other devices.

Fifteen A Series analog/digital modules are also described, including seven functionally complete digital-to-analog converter modules.

As the cost of the logic itself decreases, it becomes increasingly important that efficient, reliable and inexpensive hardware be available to keep total system costs down. DIGITAL provides this hardware. Now, from a few to thousands of modules can be connected, wired, mounted, power and enclosed efficiently with the lowest cost per function in the industry.

DIGITAL's complete line of power and hardware accessories provides everything needed to put your designs into action, from connector blocks to mounting cabinets. Seven power supplies, six connector block variations, ten mounting panels, twelve blank module configurations and five types of connector cards are among the well over 100 different hardware and accessory items described in this edition of the Logic Handbook.

Over 35 applications notes and dozens of useful design notes have been included to help you easily design custom systems, making this one of the most informative electronic handbooks available. The application information is accessible through subject index in the back or by using the thumb index on page iii.

The Company

In a little over ten years, Digital has become a major force in the electronics industry. The company has grown from three employees and 8,500 square feet of production floor space in a converted woolen mill in Maynard, Massachusetts, to an international corporation employing more than 3,000 people with over one million square feet of floor space in a dozen buildings around the world. From its beginnings as a manufacturer of digital modules, the company has now grown to the point where it is the world's largest manufacturing supplier of logic modules and the fourth largest computer manufacturer in the industry.

DIGITAL's rise as a leader in the electronics industry began in 1957 with the introduction of the company's line of electronic circuit modules. These solid state modules were used to build and test other manufacturers' computers. A year later, DIGITAL introduced its first computer, the PDP-1. The PDP-1 heralded a new concept for the industry—the small, on-line computer. And the PDP-1 was inexpensive—it sold for $120,000 while competitive machines with similar capabilities were selling at over $1 million. But the PDP-1 was more than a data processor; more than just a tool to manipulate data. It was a system that could be connected to all types of instrumentation and equipment for on-line, real-time monitoring, control and analysis. It was a system with which people and machines could interact.

Also, in 1958, DIGITAL introduced the Systems Module, a high-quality, low cost solid state digital logic circuit on a single printed circuit card. Today, electronic modules, like the ones DIGITAL introduced, are used in most electronic equipment, from computers to television sets.

In 1965, DIGITAL announced the first of the FLIP CHIP modules lines. These highly reliable modules include cards for internal computer logic, interfacing, control and analog-to-digital conversion.

About a year ago, DIGITAL announced the newest additions to the FLIP-CHIP family: M Series high-speed integrated circuit modules and K Series noise-immune modules.

This year, DIGITAL introduced the PDP-1's grandson, the PDP-8/L. It is a small computer with far greater capabilities than the PDP-1 and a price tag of only $8,500.

DIGITAL produces almost two million modules a year, making it the world's largest manufacturing supplier of logic modules. DIGITAL sales engineers in over 50 offices around the world and our applications engineering staff at the home office are ready to help you with your more difficult or complex applications. They are all listed on the inside back cover. Give us a call.

March, 1969

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PART IV

WARRANTY

WARRANTY 1. B, R, W, M, K, AND A MODULES — All B, R, W, M, K, and A modules shown in Catalogs C-105, or C-110 as revised from time to time, are warranted against defects in workmanship and material under normal use and service for a period of ten years from date of shipment providing parts are available. DEC will repair or replace any B, R, W, M, K, or A modules found to be defective in workmanship or material within ten years of shipment for a handling charge of $5.00 or 10% of list price per unit, whichever is higher. Handling charges will be applicable from one year after delivery.

WARRANTY 2. SYSTEM MODULES, LABORATORY MODULES, HIGH CURRENT PULSE EQUIPMENT, G, S, H, NON-CATALOG FLIP-CHIP MODULES AND ACCESSORIES — All items referenced are warranted against defects in workmanship and material under normal use service for a period of one year from date of shipment. DEC will repair or replace any of the above items found to be defective in workmanship or material within one year of shipment. Handling charges will be applicable from one year after delivery with handling charges varying depending on the complexity of the circuit.

The Module Warranty outside the continental U.S.A. is limited to repair of the module and excludes shipping, customer's clearance or any other charges.

Modules must be returned prepaid to DEC. Transportation charges covering the return of the repaired modules shall be paid by DEC. DEC will select the carrier, but by so doing will not thereby assume any liability in connection with the shipment nor shall the carrier be in any way construed to be the agent of DEC. Please ship all units to:

Digital Equipment Corporation
Module Marketing Services
Repair Division
146 Main Street
Maynard, Mass. 01754

No module will be accepted for credit or exchange without the prior written approval of DEC, plus proper Return Authorization Number (RA#).

All shipments are F.O.B. Maynard, Massachusetts, and prices do not include state or local taxes.
Prices and specifications are subect to change without notice.

QUANTITY DISCOUNTS

$5,000 — 3%; $10,000 — 5%; $20,000 — 10%; $40,000 — 15%;
$70,000 — 18%; $100,000 — 20%; $250,000 — 22%; $500,000 — 25%

Discounts apply to any combination of FLIP CHIP Modules

PART I

M SERIES

INTRODUCTION

The development of monolithic integrated circuits has had an impact on the design of digital module systems. Advantages of small size and high operating speeds made these circuits initially attractive. However, a lower price/performance ratio compared to hybrid or discrete component modules offset the advantages. Recently, significant price reductions in both TTL (transistor-transistor logic) and DTL (diode-transistor logic) integrated circuits indicated a re-evaluation was needed.

DIGITAL EQUIPMENT CORPORATION undertook a study of both types of logic, their performance in large and small systems, and their ease of use in system design. The result of this study is the M Series Integrated Circuit FLIP CHIP™ Module.

M Series modules contain high speed TTL logic in both general purpose and functional logic arrays. TTL was chosen for its high speed, capacitance drive capability, high noise immunity and choice of logical elements. High performance integrated circuit modules are now available at approximately one half the price of their discrete or hybrid counterparts.

In addition to the reduced cost of integrated circuits, Digital's advanced manufacturing methods and computer controlled module testing have resulted in considerable production cost savings, reflected in the low price of all M Series Modules.

GENERAL CHARACTERISTICS

M Series high-speed, monolithic integrated circuit logic modules employ TTL (transistor-transistor logic) integrated circuits which provide high speed, high fan out, large capacitance drive capability and excellent noise margins. The M Series includes a full digital system complement of basic modules which are designed with sufficient margin for reliable system operation at frequencies up to 6 MHz. Specific modules may be operated at frequencies up to 10 MHz. The integrated circuits are dual in-line packages.

The M Series printed circuit boards are identical in size to the standard FLIP CHIP™ modules. The printed circuit board material is double-sided providing 36-pins in a single height module. Mounting panels (H910 and H911) and 36-pin sockets (H803 and H808) are available for use with M Series modules. Additional information concerning applicable hardware may be found in the Power Supply & Hardware and Accessories section of this handbook.

M Series modules are compatible with Digital's K Series and, through the use of level converters, are compatible with all of Digital's other standard negative voltage logic FLIP CHIP™ modules.

OPERATING CHARACTERISTICS

Power Supply Voltage: 5 volts ± 5%

Operating Temperature Range: 0° to 70°C

Speed: M Series integrated circuit modules are rated for operation in a system environment at frequencies up to 6 MHz. Specific modules may be operated at higher frequencies as indicated by the individual module specifications.

Noise Immunity: Typical DC noise margin is 1 volt at either the logic 1 or the logic 0 level. Worst case noise margin is 400 millivolts at either level when full fan-out is employed. Reduced fanout will generally enhance the noise margin.

Logic Levels: Logic levels, unless otherwise specified, are as follows:

	Outputs	Inputs
Logic 1 or High (H)	> +2.4 volts	< +2.0 volts
Logic 0 or Low (L)	< +0.4 volts	> +0.8 volts

The above is consistent with the loading specifications for M Series modules.

Input and Output Loading: The input loading and output drive capability of M Series modules are specified in terms of a specific number of unit loads. Typically the input loading is one unit, however certain modules may contain inputs which will present greater than one unit load. The typical M Series module output will supply 10 unit loads of input loading. However, certain module outputs will deviate from a 10 unit load capability and provide more or less drive. Always refer to the individual module specifications to ascertain actual loading figures.

Unit Load: In the logic 0 state, one unit load requires that the driver be able to sink 1.6 milliamps (maximum) from the load's input circuit while maintaining an output voltage of equal to or less than +0.4 volts. In the logic 1

state, one unit load requires that the driver supply a leakage current 40 microamps (maximum) while maintaining an output voltage of equal to or greater than +2.4 volts.

TIMING: M Series pulse sources provide sufficient pulse duration to trigger any M Series flip-flop operating within maximum propagation delay specifications. Detailed timing information appears later in this section and in the module specifications.

TTL NAND GATE

The basic gate of the M Series is a TTL NAND gate. Operation of the TTL gate is similar in many respects to the familiar DTL (diode-transistor logic) NAND gate. The two circuits are compared in Figure 1.

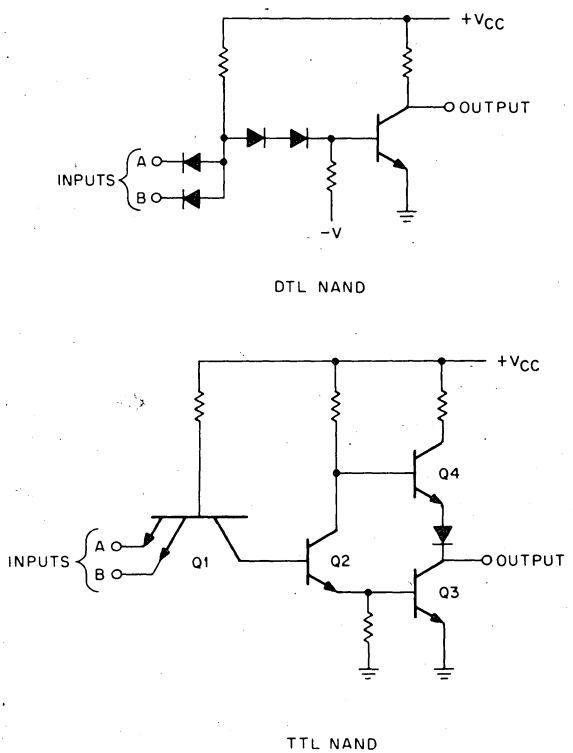


Figure 1. Schematic Comparison of DTL and TTL NAND gates

Both approaches provide the NAND function, in which the output, C, is low when both inputs (A and B) are high.

Logic Levels: Operating from a power supply voltage of +5 vdc ±5%, the TTL NAND gate develops the following nominal logic levels at the loading extremes:

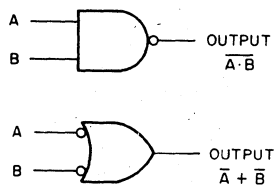
Logic Level	Voltage, No Load	Voltage, Full Load
1 (High) (H)	+3.6	+2.4
0 (Low) (L)	0.1	+0.4

Circuit Operation: The input element of the TTL gate is a multiple-emitter transistor which performs the same basic function as the input diodes of the DTL gate. When both inputs are high, the collector of transistor Q1 is high, turning on the phase-splitter, Q2. The phase-splitter turns on output switching transistor Q3, which permits the flow of load current. During the power driving state, the output is clamped near ground potential. Transistor Q4 is turned off during this state and is effectively out of the circuit.

When either of the inputs returns to the low level, the collector of the input transistor goes low, turning off the phase-splitter. The output transistor Q3, is turned off, ending the load current drain, and transistor Q4 is turned on to return the output line rapidly toward Vcc. Leakage current through the emitter of the driven gate is supplied by Q4 during the off state.

Output recovery time is speeded by the "totem pole" output circuit, which provides a practical output impedance of about 100 ohms compared to the typical DTL "pullup" resistor of 4 to 6 K ohms. This feature significantly reduces noise pickup through capacitive or inductive coupling.

NAND Logic Symbol: Logic symbology used to describe M Series modules is based on widely accepted standards. Logic symbols and a truth table for the NAND gate are shown in Figure 2.



A	B	OUTPUT
L	L	H
L	H	H
H	L	H
H	H	L

Figure 2. NAND Gate Logic Symbol and Truth Table

The first symbol is visually more effective in applications where two high inputs are ANDed to produce a low output. The second symbol better represents an application where low inputs are ORed to produce a high output.

TTL AND/NOR GATE

With a few modifications, the basic TTL NAND gate can perform an AND/NOR function useful in exclusive OR, coincidence, line selection and NOR gating operations. The modified circuit is shown in simplified form in Figure 3.

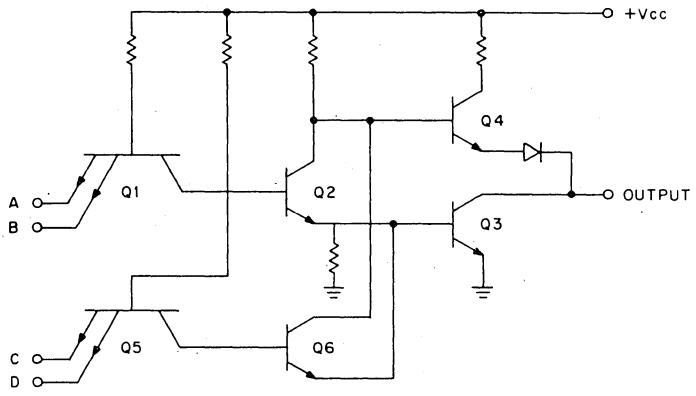
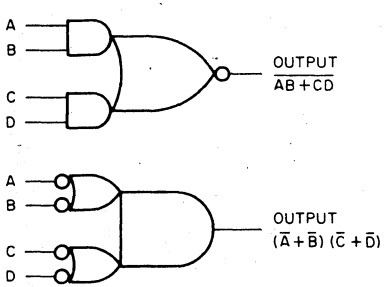


Figure 3. TTL AND/NOR Gate Simplified Schematic

Circuit Operation: The basic elements of the TTL NAND gate are used without modification. The phase-splitter (Q2) is paralleled with an identical transistor (Q6), also controlled by multiple-emitter input transistor which receives two additional inputs, C and D. When either of the input pairs are high, the phase inverter operates to switch the output voltage low. Circuit performance is essentially identical to the TTL NAND circuit.

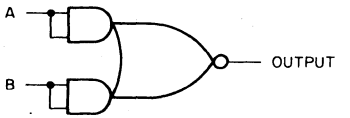
AND/NOR Logic Symbol: The logic symbols for the AND/NOR gate are shown and defined in Figure 4.



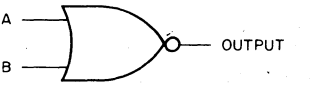
A	B	C	D	OUTPUT
H	H	ANY		L
ANY		H	H	
L	H	L	H	H
L	H	H	L	
H	L	H	L	
H	L	L	H	

Figure 4. AND/NOR Gate Logic Symbols and Truth Table

NOR Configuration: The AND/NOR gate can perform a straight NOR function if the AND gate inputs are tied together as shown in Figure 5:



AND/NOR INPUTS TIED

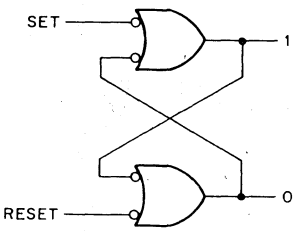


RESULTING NOR SYMBOL

Figure 5. NOR Connection of AND/NOR Gate

NAND GATE FLIP-FLOPS

RS Flip-Flop: A basic Reset/Set flip-flop can be constructed by connecting two NAND gates as shown in Figure 6.



PREVIOUS STATE		INPUT CONDITION		RESULT	
1	0	SET	RESET	1	0
L	H	L	H	H	L
H	L	H	L	L	H
L	H	H	H	NO CHANGE	
H	L	H	H	NO CHANGE	
H	L	L	H	NO CHANGE	
L	H	H	L	NO CHANGE	
L	H	L	L	H	H*
H	L	L	L	H	H*

Ambiguous state: In practice the input that stays low longest will assume control.

Figure 6. RESET/SET NAND Gate Flip-Flop

CLOCKED NAND GATE FLIP-FLOPS

The Reset-Set flip-flop can be clock-synchronized by the addition of a two-input NAND gate to both the set and the reset inputs. (See Figure 7.) One of the inputs of each NAND is tied to a common clock or trigger line.

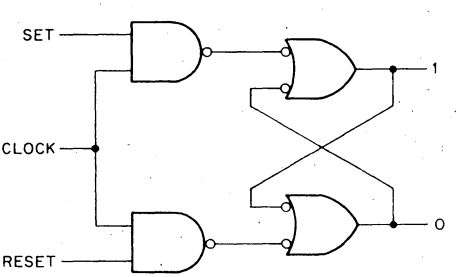


Figure 7. Clocked NAND Gate Flip-Flop

A change of state is inhibited until a positive clock pulse is applied. The ambiguous case will result if both the set and reset inputs are high when the clock pulse occurs.

M SERIES GENERAL-PURPOSE FLIP-FLOPS

Two types of general-purpose flip-flops are available in the M Series, both of which have built-in protection against the ambiguous state characteristic of NAND gate flip-flops.

FLIP-FLOP CLOCK INPUT SYMBOLS

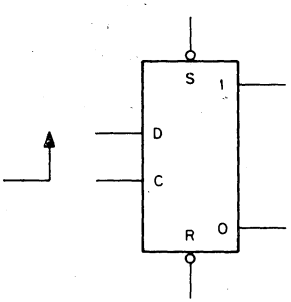
The D type flip-flop is a true leading (positive going voltage) edge triggered flip-flop and the D input is locked out until the clock input returns to low. The symbol to indicate this function will be as follows;.

D TYPE FLIP FLOP CLOCK

The operation of the J-K type flip-flop is to transfer the information present at the J and K inputs just prior to and during the clock pulse to the master flip-flop when the threshold is passed on the leading (positive going voltage) edge of the clock pulse. The information stored in the master flip-flop is transfered to the slave flip-flop, and consequentially to the outputs, when the threshold is passed on the trailing (negative going voltage) edge of the clock pulse. The symbol to indicate this function will be as follows;

J K TYPE FLIP FLOP CLOCK

D Type Flip-Flop: The first of these is the D type flip-flop shown in Figure 8. In this element, a single-ended data input (D) is connected directly to the set gate input. An inverter is provided between the input line (D) and the reset input. This ensures that the set and reset levels cannot be high at the same time.



LOGIC SYMBOL

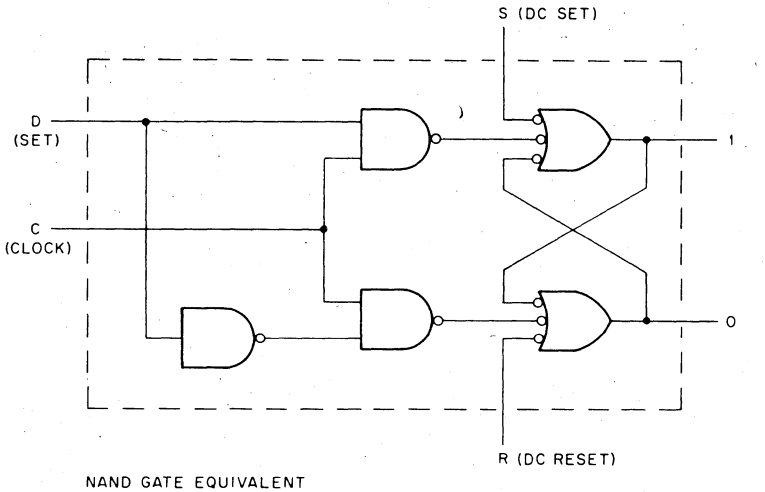


Figure 8. D Type General Purpose Flip-Flop

The flip-flop proper employs three-input NAND gates to provide for dc set and reset inputs.

D type flip-flops are especially suited to buffer register, shift register and binary ripple counter applications. Note that D type devices trigger on the leading (or positive going) edge of the clock pulse. Once the clock has passed threshold, changes on the D input will not affect the state of the flip-flop due to a lockout circuit (not shown).

A characteristic of the D type flip-flop which is not illustrated in the NAND gate equivalent circuit is the fact that the D input is locked out after the clock input threshold voltage on the leading (positive going voltage) edge of the clock has been passed. The D input is not unlocked until the clock input threshold voltage of the trailing (negative going voltage) edge has been passed.

"MASTER-SLAVE J-K FLIP-FLOP"

The two unique features of a J-K flip-flop are: A) a clock pulse will not cause any transition in the flip-flop if neither the J nor the K inputs are enabled during the clock pulse, and B) if both the J and the K inputs are enabled during the clock pulse, the flip-flop will complement (change states). There is no indeterminate condition in the operation of a J-K flip-flop.

A word of caution is in order concerning the clock input. The J and K inputs must not be allowed to change states when the clock line is high, the output will complement on the negative going voltage transition of the clock. It is for this reason that the clock line must be kept low until it is desired to transfer information into the flip-flop and no change in the states of the J and K inputs should be allowed when the clock line is high.

The J-K flip-flops used are master-slave devices which transfer information to the outputs on the trailing (negative going voltage) edge of the clock pulse. The J-K flip-flop consists of two flip-flop circuits, a master flip-flop and a slave flip-flop. The information which is present at the J and K inputs when the leading edge threshold is passed and during the clock high will be passed to the master flip-flop (The J and K inputs must not change after the leading edge threshold has been passed). At the end of the clock pulse when the threshold of the clock is passed during the trailing (negative going voltage) edge, the information present in the master flip-flop is passed to the slave flip-flop. If the J input is enabled and the K input is disabled prior to and during the clock pulse, the flip-flop will go to the "1" condition when the trailing edge of the clock occurs. If the K input is enabled and the J input is disabled prior to and during the clock pulse, the flip-flop will go to the "0" condition when the trailing edge of the clock pulse occurs. If both the J and K inputs are enabled prior to and during the clock pulse, the flip-flop will complement when the trailing edge of the clock pulse occurs. If both the J and K inputs are disabled prior to and during the clock pulse, the flip-flop will remain in whatever condition existed prior to the clock pulse when the trailing edge of the clock pulse occurs.

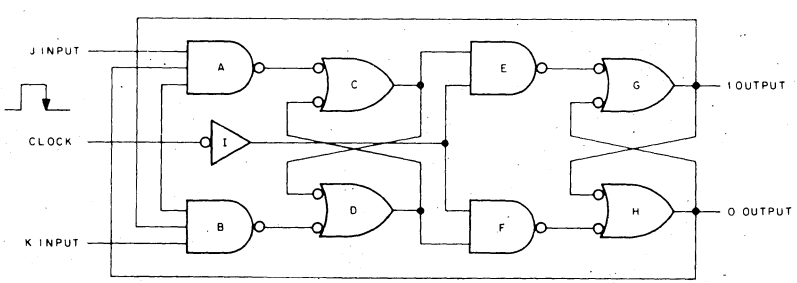


Figure 9. Master-Slave J-K Flip-Flop

Figure 10 shows a functional block diagram of a master slave J-K flip-flop using NAND gates. Gates C and D are the master flip-flop. Gates G and H are the slave flip-flop. Gates A and B are the steering network of the master flip-flop and the steering network for the slave flip-flop is comprised of gates E, F, and 1. The 1 output of the master flip-flop is point X. The operation of the flip-flop will be studied by examining the "1" to "0" transition of the flip-flops, with both the J and the K inputs enabled with a HI level before the clock pulse. When the leading edge of a HI clock pulse occurs, gate B will be enabled with three HI inputs. This will provide a RESET signal for the master flip-flop which will then go to the "0" condition. The slave flip-flop remains in the "1" condition while the clock pulse is HI because gate I is providing a LO signal to both gates E and F, thereby blocking inputs to the slave flip-flop. When the trailing edge of the clock pulse occurs, gate F will be enabled with a HI level at both its inputs and a RESET signal will be provided to the slave flip-flop, which will then go to the "0" condition. The next clock pulse, with both the J and K enabled, would cause the master flip-flop to go to the "1" condition on the leading edge of the clock pulse and cause the slave flip-flop to go to the "1" condition on the trailing edge of the pulse. Figure 10 is a truth table for the J-K flip-flop showing all eight possible initial conditions.

INITIAL CONDITIONS OUTPUTS		INPUTS		FINAL CONDITIONS OUTPUTS	
1	0	J	K	1	0
LO	HI	LO	LO	LO	HI
LO	HI	LO	HI	LO	HI
LO	HI	HI	LO	HI	LO
LO	HI	HI	HI		
HI	LO	LO	LO		
HI	LO	LO	HI		
HI	LO	HI	LO		
HI	LO	HI	HI		

Figure 10. Master-Slave J-K Flip-Flop Truth Table

UNUSED INPUTS (GATES AND FLIP-FLOPS)

Since the input of a TTL device is an emitter of a multiple-emitter transistor, care must be exercised when an input is not to be used for logic signals. These emitters provide excellent coupling into the driving portions of the circuit when left unconnected. To insure maximum noise immunity, it is necessary to connect these inputs to a source of Logic 1 (High). Two methods are recommended to accomplish this:

1. Connect these inputs to a well filtered and regulated source of +3 volts. Pins U1 and V1 are provided on the M113, M117, M119, M121, M617, and M627 for this purpose.

2. Connect these inputs to one of the active inputs on the same gate. This results in a higher leakage current due to the parallel emitters and should be considered as an additional unit load when calculating the loading of the driving gate.

Connection of unused inputs to the supply voltage, Vcc, is not advisable, since power supplies are subject to transients and voltage excursions which could damage the input transistor.

TIMING CONSIDERATIONS

Standard Timing Pulse: In digital system design, a reference for system timing is usually required. The M Series modules M401 or M405 produces a standard pulse which provides such a reference. The standard pulse derived from each of these two modules is shown in Figure 11.

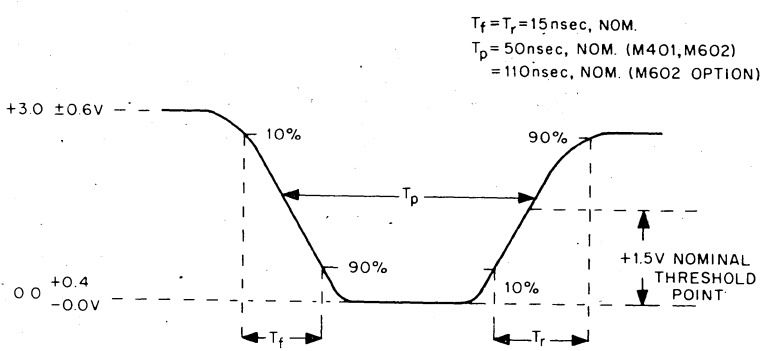


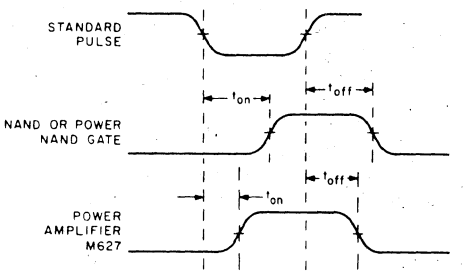
Figure 11. Standard Pulse

NAND Gate and Power Amplifier Propagation Delays: The standard pulse (Figure 11) is distributed throughout a system in negative form to maintain the leading edge integrity. (Since the TTL gate drives current in the logic 0 state, the falling edge is more predictable for timing purposes.) However, the standard pulse is of the wrong polarity for use as a clocking input to the type D and J-K flip-flops, requiring the use of a local inverter. Ordinarily, a NAND inverter is adequate. Where high fan-out is necessary, a M617 Power NAND is preferred.

For applications requiring both high fan-out and critical timing the M627 Power Amplifier is available. This module contains extremely high-speed gates which exhibit turn-on times differing by only a few nanoseconds.

Simultaneity is desirable in clock or shift pulses distributed to extended shift registers or synchronous counters.

Delays introduced by inverting gates and power amplifiers are illustrated in Figure 12. (Delays are measured between threshold points.)



DELAY (NANOSECONDS)			
t_{on}		t_{off}	
TYP	MAX	TYP	MAX
18	29	8	15
7	—	5	—

Figure 12. NAND Gate and Power Amplifier Delays

Flip-Flop Propagation Delays: D type flip-flops trigger on the leading or rising edge of a positive clock pulse; the propagation delay is measured from the threshold point of this edge. The set-up time of the D flop is also measured from this threshold point. Data on the D input must be settled at least 20 nanoseconds prior to the clock transition. The advantage of the D-flip-flop, however, is that the leading edge triggering allows the flip-flop AND gates to propagate while the clock pulse is still high. Figure 13 illustrates this situation.

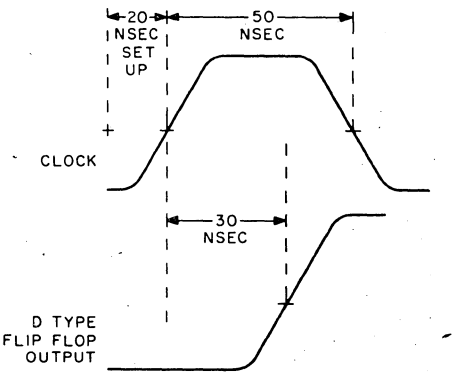


Figure 13. D Type Flip-Flop Timing

JK type flip-flops are, in effect, trailing edge triggering devices as explained previously. The only restriction on the J and K inputs is that they must be settled by the time that the rising edge occurs. Timing is shown in Figure 14.

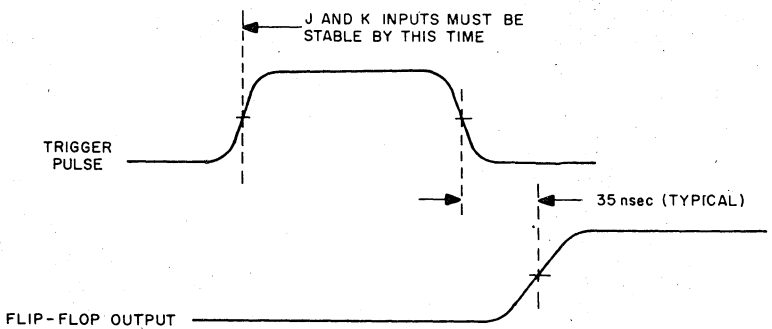


Figure 14. J-K Flip-Flop Timing

When using the dc Set or Reset inputs of either flip-flop type, propagation delays are referenced to the falling edge of the pulse. This is due to the inverted sense of these inputs. When resetting ripple type counters (where the output of one flip-flop is used as the trigger input to the next stage) the reset pulse must be longer than the maximum propagation delay of a single stage. This will ensure that a slow flip-flop does not introduce a false transition, which could ripple through and result in an erroneous count.

One-Shot Delay: Calibrated time delays of adjustable duration are generated by the M302 Delay Multivibrator. When triggered by a level change from a logical one to a logical zero, this module produces a positive output pulse that is adjustable in duration from 50 to 750 nsec with no added capacitance. Delays up to 7.5 milliseconds are possible without external capacitance. (See M302 specification.) Basic timing and the logic symbol are shown in Figure 15. The 100 picofarad internal capacitance produces a recovery time of 30 nsec. Recovery time with additional capacitance can be calculated using the formula;

$$t_r \text{ Nanoseconds} = 30 \frac{\text{C Total (Picofarads)}}{100}$$

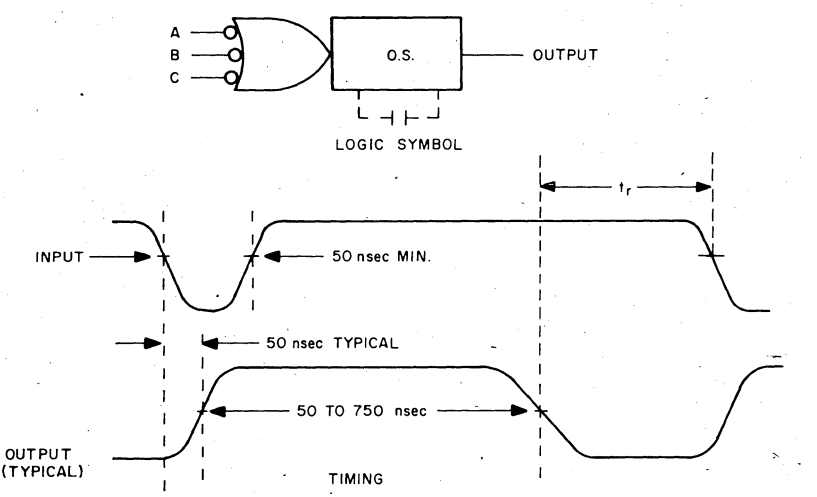


Figure 15. One-Shot Delay Timing and Logic Symbol

SYSTEM OPERATING FREQUENCY

Although individual propagation delays are significant in the design of digital logic, even more important is the maximum operating frequency of a system which is composed of these individual modules. Specifically designed systems may be operated at 10 MHz, but a more conservative design may result in a somewhat lower operating speed. M Series modules can be designed into a system with a 6 MHz clock rate with relative ease. This system frequency is derived by summing the delays in a simple logic chain:

1. A standard clock pulse width of 50 nsec is assumed. This period is measured from the threshold point of the leading edge to the threshold point of the trailing edge.

2. One flip-flop propagation delay of 35 nsec from the trailing edge of the clock pulse to the threshold point of the final state of the flip-flop is allowed.

3. Two gate-pair delays of 30 nsec each are assumed. (A gate-pair consists of two inverting gates in series.) Two gate-pair delays are usually required to perform a significant logic function with a minimum of parallel operations. The two gate-pair delays total 60 nsec.

The time necessary to perform these operations before the next occurrence of the clock pulse is the sum of the delays; 50 + 35 + 60, or 145 nsec. Allowing 20 nsec for variations within the system, the resulting period is 165 nsec, corresponding to a 6 MHz clock rate. This timing is demonstrated in Figure 16.

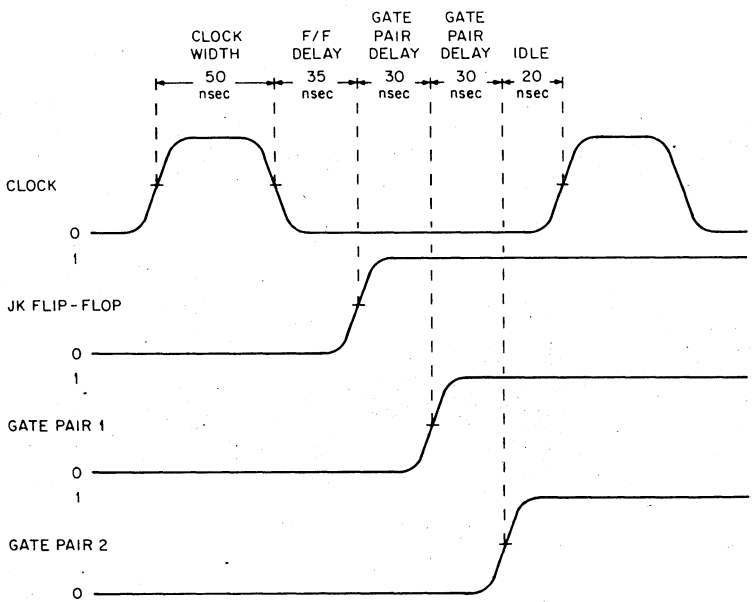
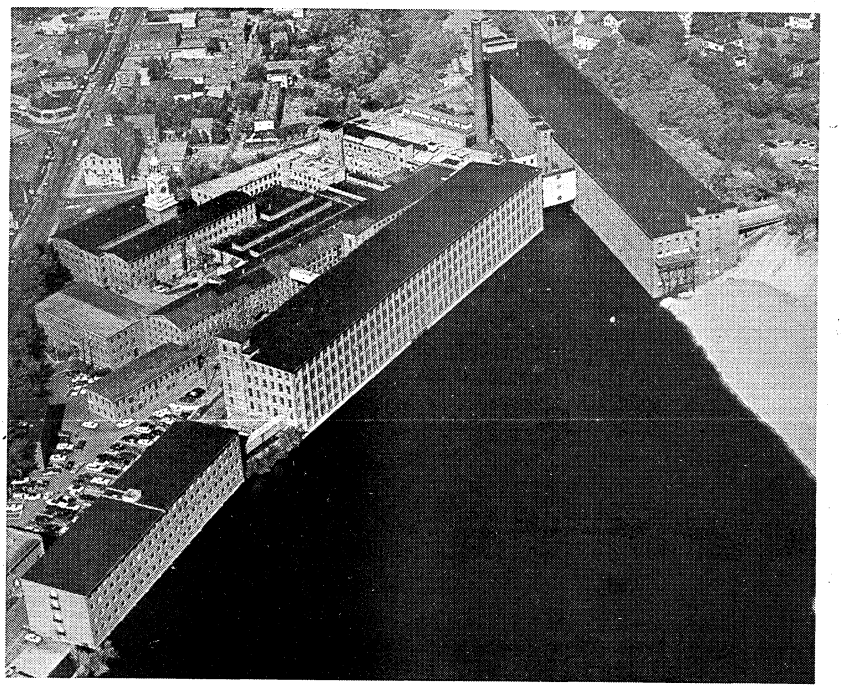


Figure 16. Delays Determining System Operating Frequency

Substitution of a D type flip-flop results in a similar timing situation. In a system using both D and J-K flip-flops, note that the D flip-flop triggers on the leading edge of the clock pulse and the J-K flip-flop triggers on the trailing edge. When calculating system timing using D flip-flops, remember that the flip-flop inputs must be settled at least 20 nsec prior to the occurrence of the clock pulse.

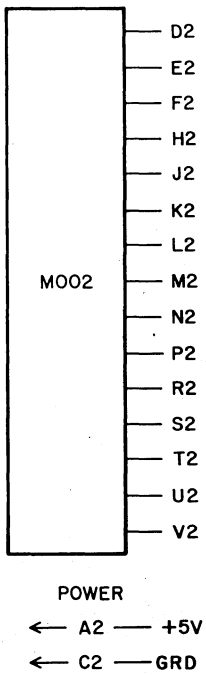
Preparation of a timing diagram that considers delays introduced by all logic elements will aid the designer in achieving predictable system performance.



DIGITAL's home office and main manufacturing facilities are located in this former woolen mill complex in Maynard, Massachusetts. We have 900,000 square feet here, about 100 times more than when the company started producing digital modules eleven years ago. We also manufacture at three other locations.

LOGIC 1 SOURCE
M002

M
SERIES



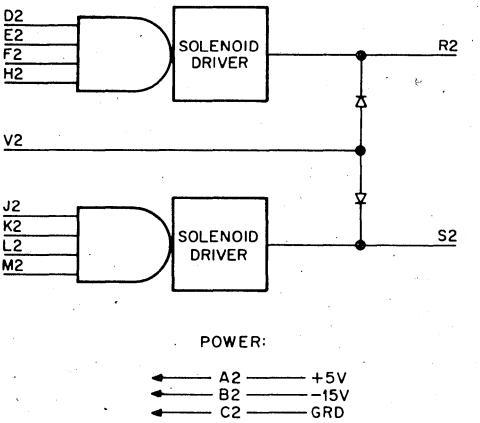
To hold unused M-Series TTL gate inputs high, the M002 provides 15 outputs at +3 volts (Logic 1), on pins D2 through V2. Up to 10 unused M-Series gate inputs may be connected to any one output. If a M002 circuit is driven by a gate, it appears as two TTL unit loads or 3.2 ma. at ground.

Power: +5 v at 16 ma. (max.)

M002 — $10

SOLENOID DRIVER
M040

M SERIES



M040 Solenoid Driver

These high current drivers can drive relays, solenoids, stepping motor windings, or other similar loads. The output levels are —2 volts and a more negative voltage determined by an external power supply. One terminal of the load device should be connected to the external power source, the other to the driver output. There are two drivers per module.

Pin V of the driver module must be connected to the external supply so that the drivers will be protected from the back voltage generated by inductive loads. If the wire to the power supply is more than 3 feet long it may have to be by-passed at the module with an electrolytic capacitor to reduce the short over-shoot caused by the inductance of the wire. If pin V is connected to the supply through a resistor, the recovery time of inductive loads can be decreased at a sacrifice in maximum drive voltage capability. Maximum rated supply voltage less actual supply voltage should be divided by load current to find the maximum safe resistance. When both circuits on a module are used, the load current for the above calculation is the sum of the currents.

Inputs: Each input presents one unit load.

Outputs: The M040 has maximum ratings of —70 volts and 0.6 amp. Typical delay for the circuit is 5 μsec. No more than two circuits should be paralleled to drive loads beyond the current capabilities of single circuits.

Grounding: High current loads should be grounded at pin C2 of the M040. —15 volt at 9 ma. (max.)

Power: +5 volt at 47 ma. (max.)

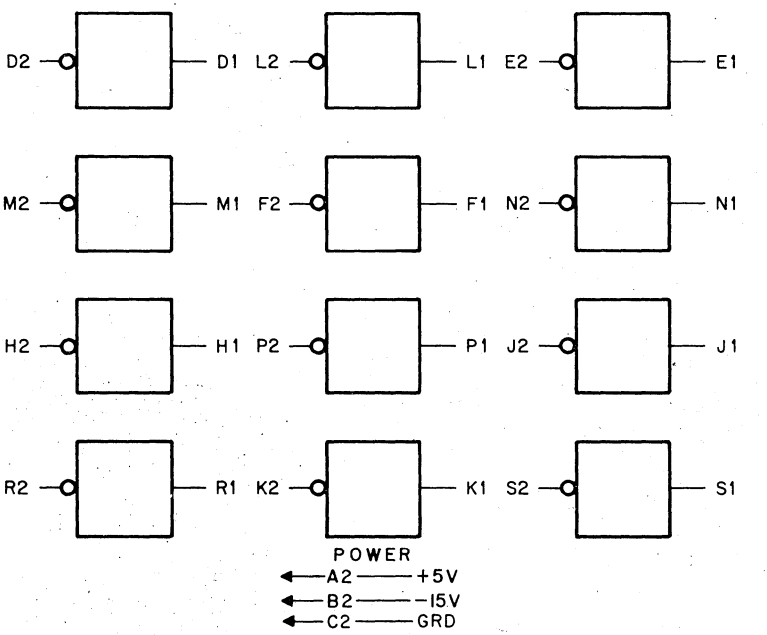
The external voltage supply must provide the output current of the two drivers. (1.2 amps. max.)

Note:
Refer to K Series driver modules for increased current drive, increased voltage breakdown or AC current drive capability.

M040 — $39

50 MA. INDICATOR DRIVER
M050

M SERIES



M050 INDICATOR DRIVER

The M050 contains twelve transistor inverters that can drive miniature incandescent bulbs such as those on an indicator panel. It is used to provide drive current for a remote indicator, such as Drake 11-504, Dialco 39-28-375, or Digital Indicator type 4908, or level conversion to drive 4917 and 4918 indicator boards (See the Hardware Section.) A low level on the input of the driver causes current to flow in the output.

Inputs: Each input presents two unit loads.

Outputs: Each output is capable of driving 50 ma. into an external load connected to any voltage between ground and −20 volts.

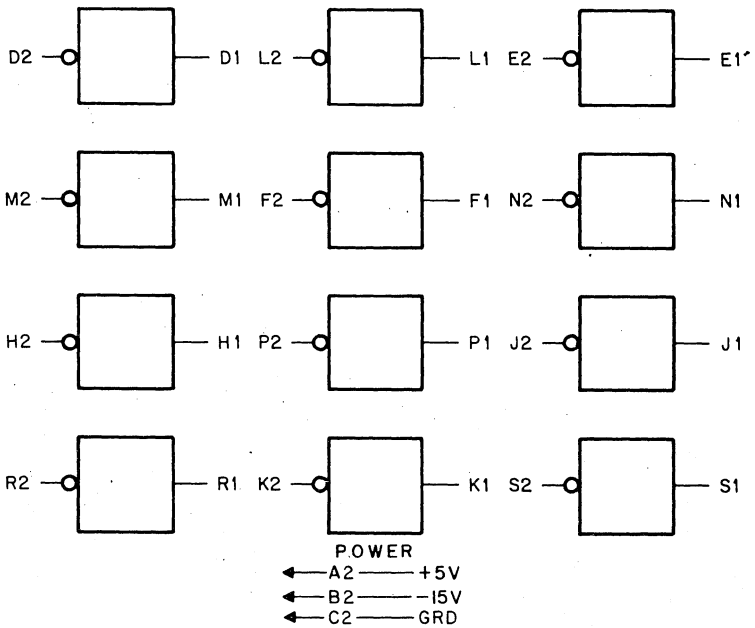
Power: +5 volt at 47 ma. (max.)
−15 volt at 16 ma. (max.)

Note: For those applications requiring the sinking of current, refer to K Series.

M050—$31

LEVEL CONVERTER
M051

M SERIES



The M051 contains twelve level converters that can be used to shift M and K Series logic levels to negative logic levels of ground and —3 volts. A grounded input on the driver generates a grounded output.

Inputs: Each input presents two TTL unit loads.

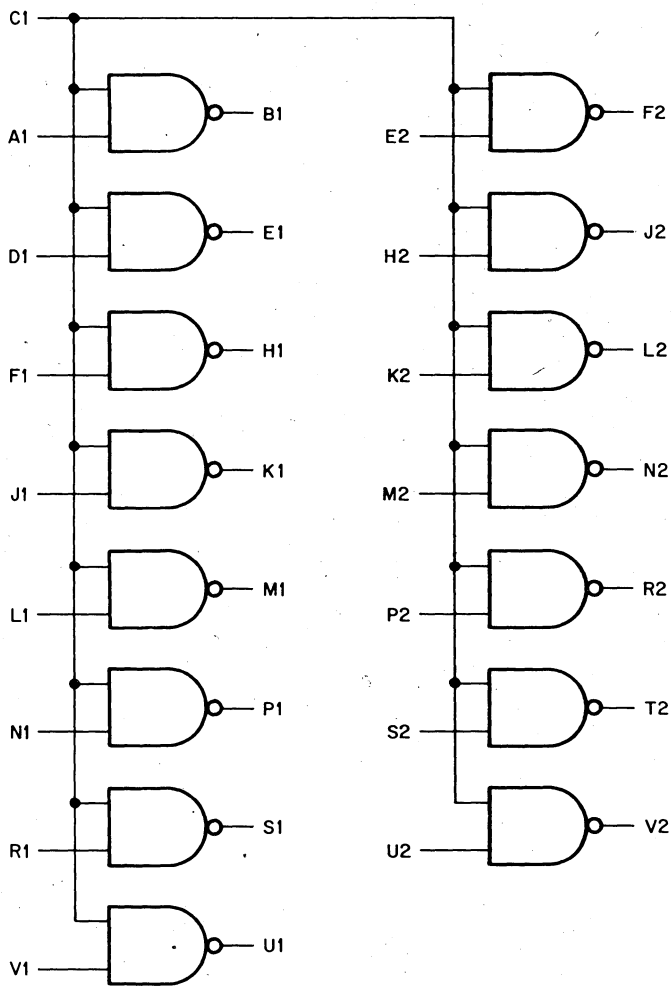
Outputs: The output consists of an open collector PNP transistor and can drive 20 ma. to ground —6V maximum may be applied to the output.

Power: +5V at 47 ma. (max.); —15V at 16 ma. (max.)

M051—$31

BUS DATA INTERFACE
M101

M SERIES



POWER

← A2 — +5V

← C2, T1 — GRD

The M101 contains fifteen, two-input NAND gates arranged for convenient data strobing off of the PDP8/I or PDP8/L positive bus. One input of each gate is tied to a common line so that all data signals on the second input of each gate can be enabled simultaneously. The M101 can also be used as inverters or a data multiplexer. All data inputs are protected from a negative of more than —0.8 volts.

Inputs: Each data signal input presents one TTL unit load. The common line input presents fifteen unit loads.

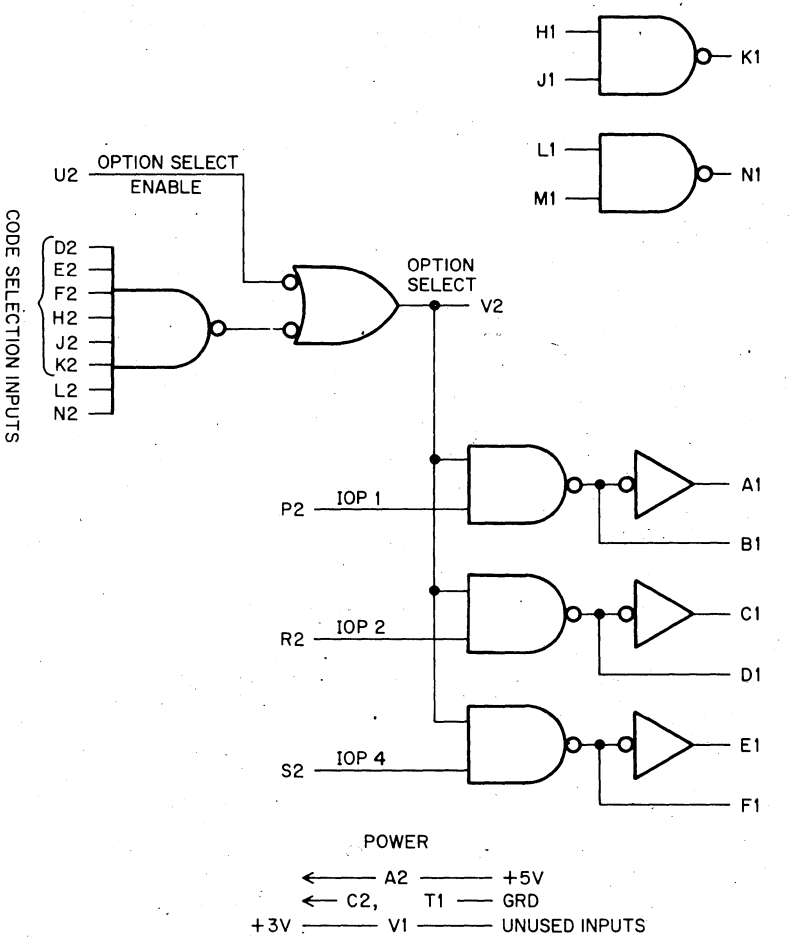
Outputs: Each output can drive ten unit loads.

Power: +5V at 82 ma. (max.)

M101—$24

DEVICE SELECTOR
M103

M SERIES



The M103 is used to decode the six device bits transmitted in complement pairs on the positive bus of the PDP8/I and PDP8/L. Selection codes are obtained by selective wiring of the bus signals to the code select inputs D2, E2, F2, H2, J2, and K2. This module also includes pulse buffering gates for the IOP signals found on the positive bus of the above computers. Two two-input NAND gates are also provided for any additional buffering that is required.

Inputs: All inputs which receive positive bus signals are protected from negative voltage undershoot of more than —0.8V.

The following inputs each present one TTL unit load D2, E2, F2, H2, J2, K2 H1, J1, L1, and M1. Inputs P2, R2, and S2 present 2.5 TTL unit loads. Inputs U2, L2 and N2 each present 1.25 unit loads. These inputs need not be tied to a source of logic 1 when not used.

Outputs: Gate outputs K1 and N1 can each drive ten TTL unit loads.

Pulse buffering outputs A1, B1, C1, D1, E1 and F1 can each drive 37 TTL unit loads.

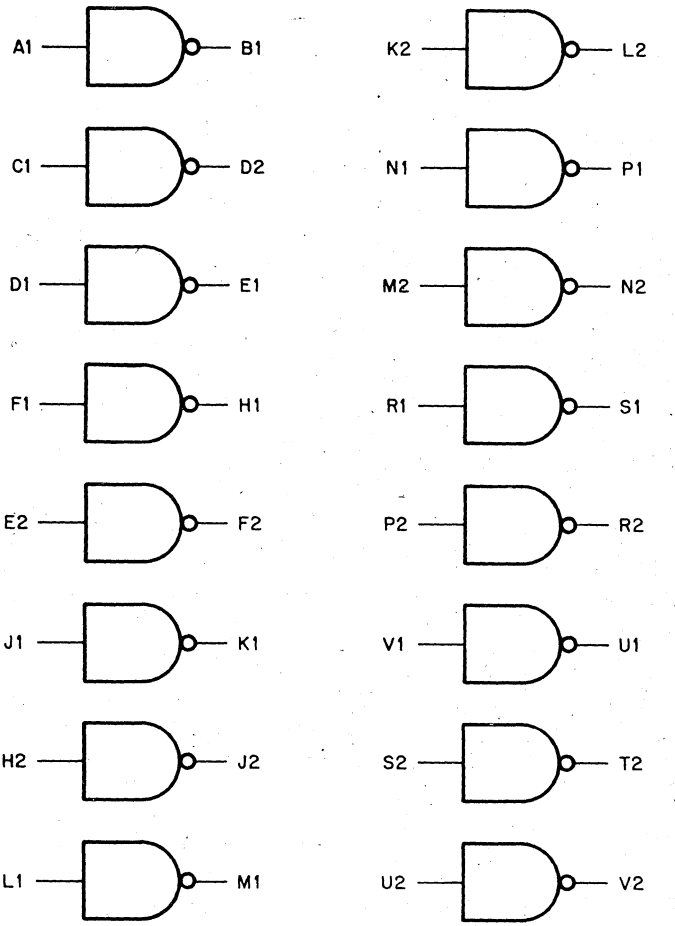
The Option Select output can drive 16 TTL unit loads.

Power: +5 volts at 110 ma. (max.)

M103—$50

INVERTER
M111

M SERIES



Sixteen Inverters with input/output connections as shown.

Input: Each input presents one unit load.

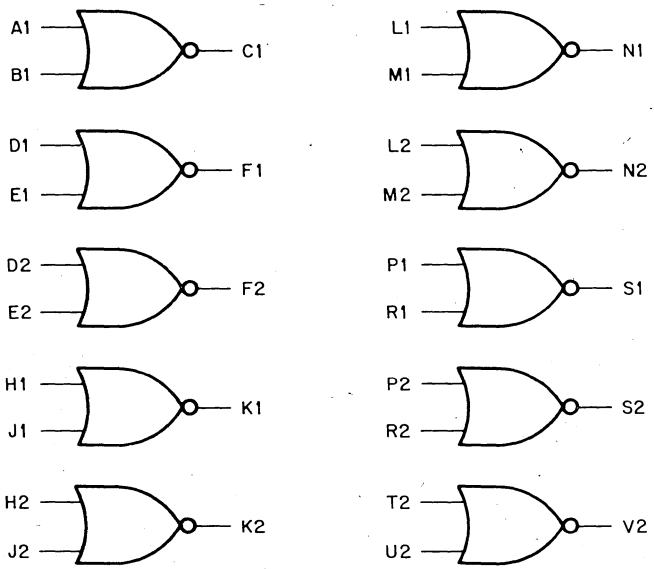
Output: Each output can drive up to ten unit loads.

Power: +5 volts, 87 ma. (max.)

M111—$24

NOR GATE
M112

M SERIES



The M112 contains ten positive NOR gates, each performing the function A + B. Pins U1 and V1 provide +3 volts, each capable of holding High (Logic 1) up to 40 unused M-Series inputs.

Input: Each input presents one unit load.

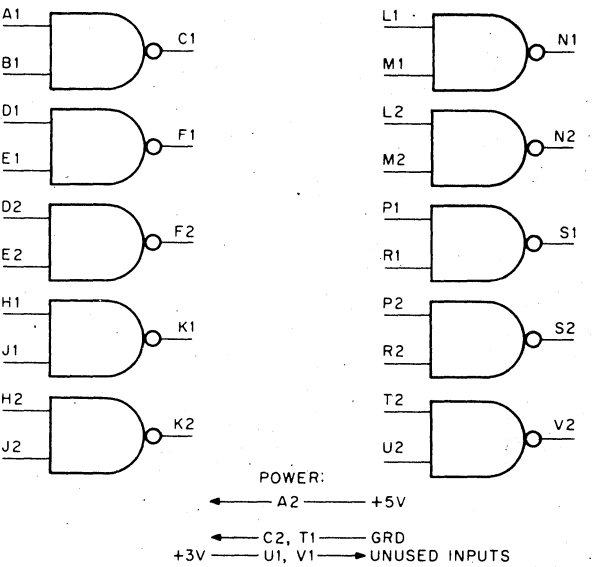
Output: Each output can drive up to ten unit loads.

Power: +5V at 50 ma. (max.)

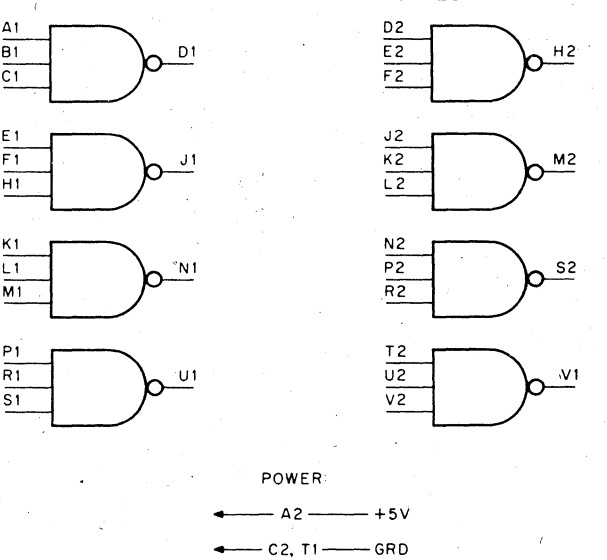
M112—$37

NAND GATES
M113, M115, M117, M119

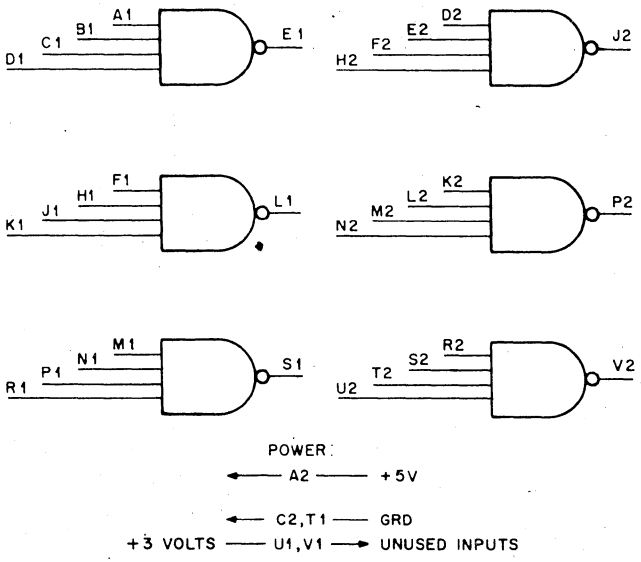
M SERIES



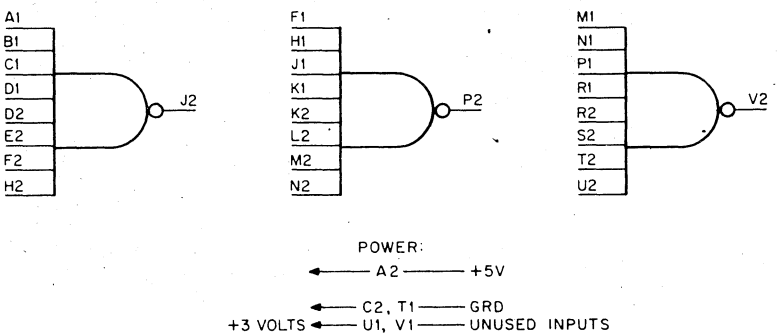
M113 2-INPUT NAND GATES



M115 3-INPUT NAND GATES



M117 4-INPUT NAND GATES



M119 8-INPUT NAND GATES

These modules provide general-purpose gating for the M Series, and are most commonly used for decoding, comparison, and control. Each module performs the NAND function A • B - - - - - - - - - N, depending upon the number of inputs.

M113—Ten, two-input NAND gates that also may be used as inverters.

M115—Eight, three-input NAND gates.
M117—Six, four-input NAND gates.
M119—Three, eight-input NAND gates.

Unused inputs on any gate must be returned to a source of logic 1, for maximum noise immunity. In the M113, M117, M119, M121, M617 and M627 modules, two pins are provided (U1 and V1) as source of +3 volts for this purpose. Each pin can supply up to 40 unit loads.

M103, M111 and M002 provide additional sources of logic 1 level.

Typical propagation delay of M Series gates is 15 nsec.

Inputs: Each input presents one unit load.

Outputs: Each output is capable of supplying 10 unit loads.

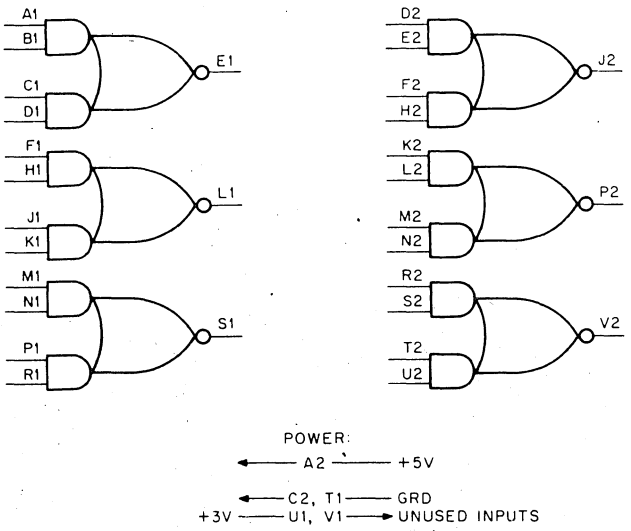
Power:

M113:	71 ma.	} +Max. current at 5 volts.
M115:	41 ma.	
M117:	41 ma.	
M119:	9 ma.	

M113—$20
M115—$20
M117—$21
M119—$20

AND/NOR GATE
M121

M SERIES



M121 AND/NOR GATES

The M121 module contains six AND/NOR gates which perform the function AB + CD. By proper connection of signals to the AND inputs, the exclusive OR, coincidence, and NOR functions can be performed.

Typical propagation delay of an M121 gate is 15 nsec.

Inputs: Each input presents one unit load to the driving module.

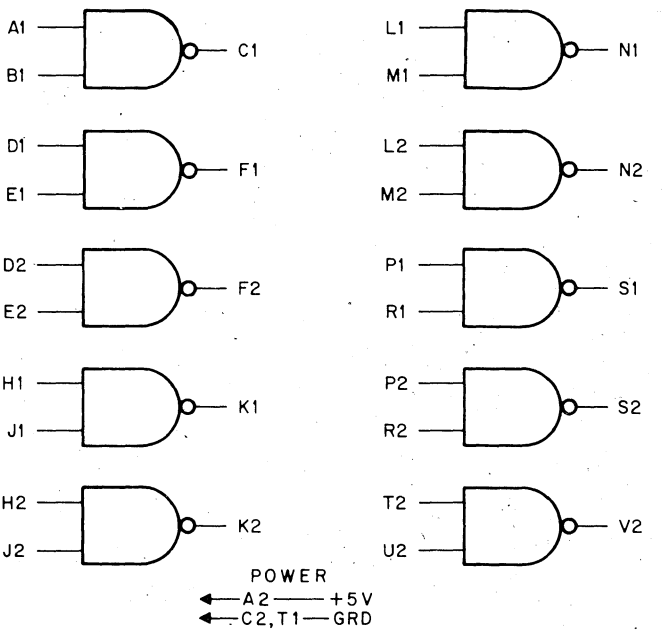
Outputs: Each output is capable of driving up to 10 unit loads.

Power: +5volt at 50 ma. (max.)

M121—$25

INPUT NAND GATES
M133

M SERIES



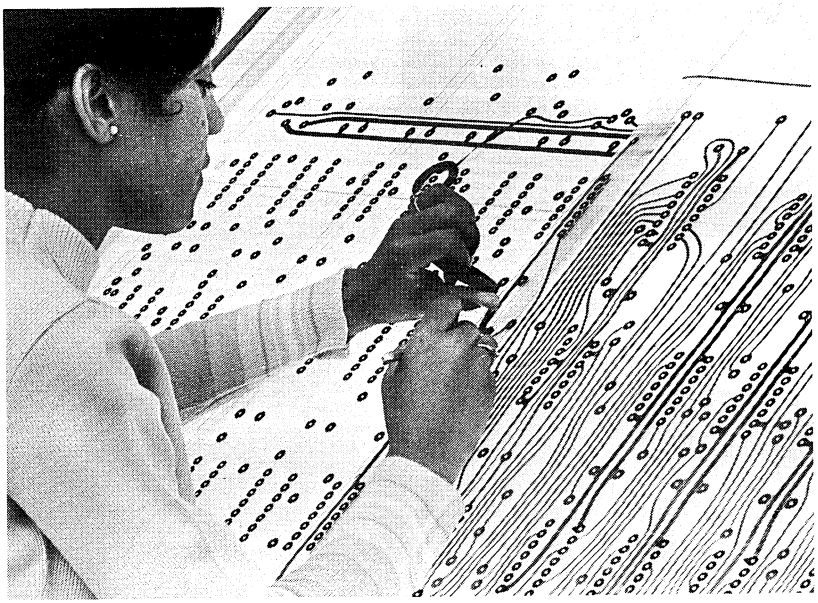
This module provides general purpose high speed gating for the M-Series. Maximum output propagation delay to a logic 1 or 0 is 10 nsec. The high speed characteristic of these gates frequently will solve tight timing problems in complex systems. Unused inputs on any gate must be returned to a source of logic 1 for maximum speed and noise immunity.

Inputs: Each input presents 1.25 unit loads.

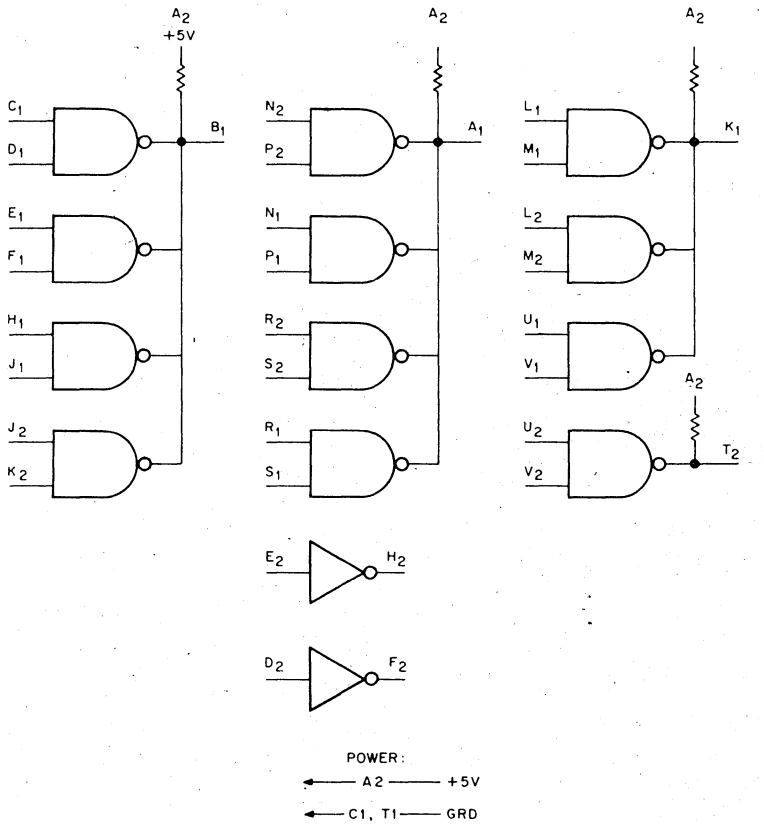
Outputs: Each output is capable of driving 12.5 unit loads.

Power: +5V at 160 ma. (max.)

M133—$29



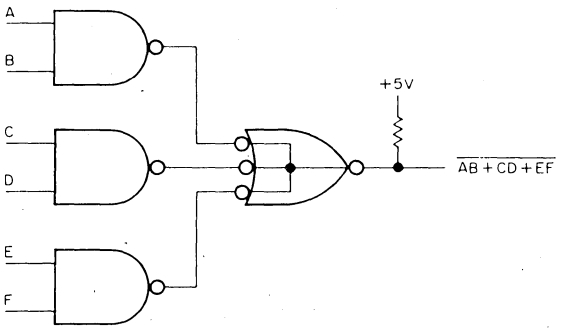
The printed circuit board layout is a crucial step in module production. Tolerances are checked to within 1/5000 of an inch.



M141 NAND/OR GATE

The M141 NAND/OR gate performs two levels of logic. The first is the NAND function which is identical to the M113 NAND gate. The second level is that of a wired OR for low logic levels. The two input NAND gate which is used in the M141 does not have the standard TTL output circuit, but only the lower half of the totem pole output. This allows the outputs of these gates to be connected together and to share a common pull-up resistor. Propagation delay through these gates is a maximum of 70 nsec.

The NAND/OR gates are arranged in four groups consisting of 4, 4, 3, and 1 two input NAND gates respectively. The outputs in each group are connected together which provide a wired OR for low levels. The function of these gates can be shown as:



By using one of the two inverters provided, a true AND/OR function can be realized. A maximum of four groups of gates can be connected together. Connection is made by merely connecting output pins together.

Inputs: Each input presents one unit load.

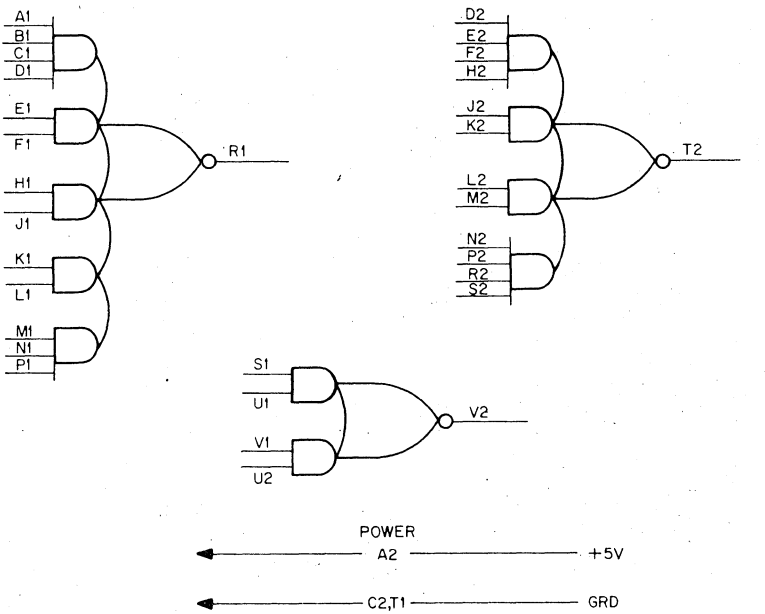
Outputs: Four gate outputs, each capable of driving 7 unit loads. The load resistor of each output presents 2 unit loads when connected to another output. For example, four groups are connected together, therefore 3 groups present two unit loads each to the fourth group, totalling 6 unit loads. This leaves 1 unit load capability. Each inverter output is capable of driving up to 10 unit loads.

Power: +5 volts at 117 ma. (max.)

M141—$30

AND/NOR GATE
M160

M SERIES



M160 AND/NOR GATES

The M160 module contains three general purpose AND/NOR gates which perform functions similar to the M121. By connecting signals to the AND inputs, these gates can be used to select and place on a single output any of several input signals.

Typical propagation delay of an M160 gate is 20 nsec.

Inputs: Each input presents one unit load

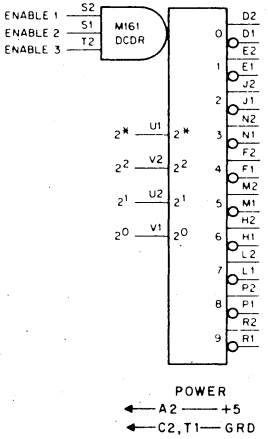
Outputs: Each output is capable of driving 10 unit loads

Power: 5 volt at 30 ma. (max.)

M160—$35

BINARY TO OCTAL/DECIMAL DECODER
M161

M SERIES



M161 BINARY TO OCTAL/DECIMAL DECODER

The M161 is a functional decoding module which can be used as a binary-to-octal or binary-coded decimal (8421 or 2421 codes) to decimal decoder. In the binary-to-octal configuration, up to eight M161's can be linked together to provide decoding of up to six bits. Three ENABLE inputs are provided for selective enabling of modules in decoders of more than one digit. In the octal mode, the bit 2* input is connected to ground, which automatically inhibits the 8 and 9 outputs. Connections for a 5-bit binary/octal decoder (4 modules) are shown below. The figure assumes that the inputs to the decoder are the outputs of flip-flops such as FF2° (1), 1 output side; and FF2° (0), 0 output side.

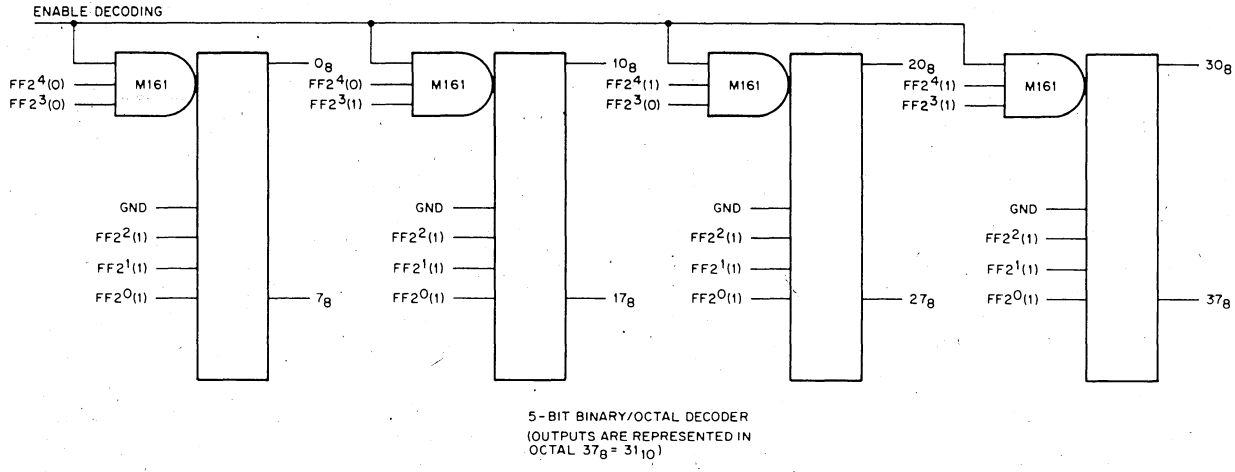
The 2* input may be of decimal value 2, 4, 6, 8 as long as illegal combinations are inhibited before connections to the inputs, and the 4-2-1 part of the code is in binary.

The propagation delay through the decoder is typically 55 nsec in the binary-to-octal mode, and 75 nsec in the BCD-to-decimal mode. The maximum delay in the BCD-to-decimal mode is 120 nsec, frequency-limiting this module to 8HMz when used in this fashion. The enable inputs can be used to strobe output data providing inputs 2° — 2* have settled at least 50 nsec prior to the input pulse.

Inputs: 2° through 2*, 1 unit load each; ENABLE 1 through ENABLE 3, 2 unit loads each.

Outputs: Each positive output is capable of driving 10 unit loads, and each negative output, 9 unit loads.

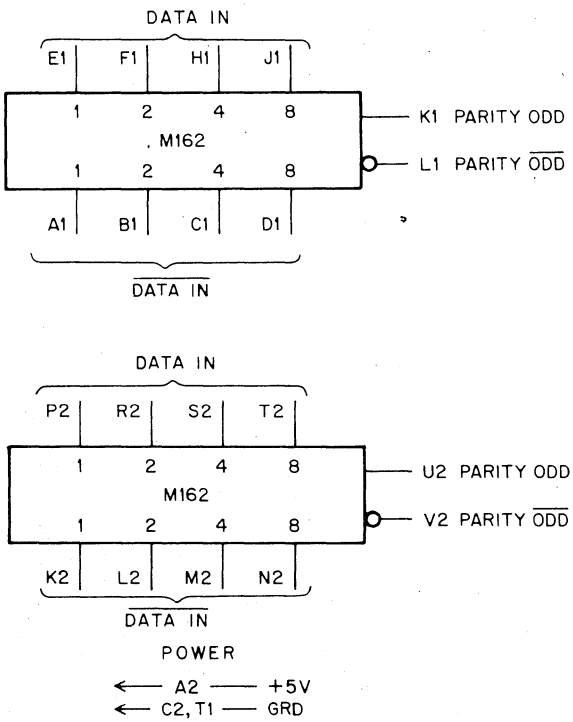
Power: 5 volts at 120 ma. (max.)



5-BIT BINARY/OCTAL DECODER

PARITY CIRCUIT
M162

M SERIES



The M162 is a parity detector and contains two Parity Circuits. Each circuit indicates whether the Binary Data presented to it contains an ODD or EVEN number of ONES. The DATA and its complement are required as shown.

Indication of ODD PARITY is given by a High level of pins K1 and U2 respectively. Pins L1 and V2, when High, indicate EVEN PARITY or no input.

Input: Each input presents four unit loads.

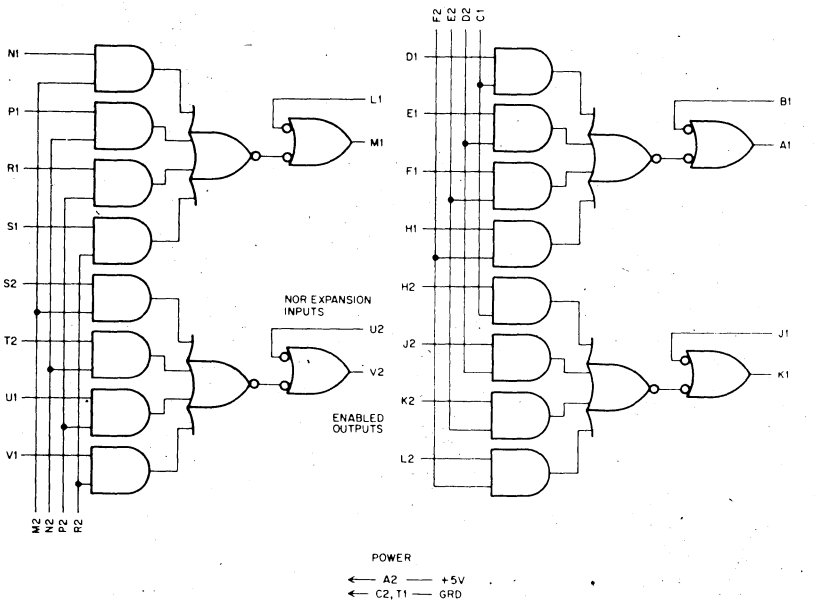
Output: Pins L1 and V2 can each supply up to ten unit loads. Pin K1 and U2 can each supply up to six unit loads.

Power: +5 volts at 102 ma. (max.)

M162 — $68

GATING MODULE
M169

M SERIES



M169 GATING MODULE

The M169 provides a general gating function, and may be used as a four-output multiplexer. Raising High a DATA INPUT and selecting a corresponding INPUT ENABLE line, generates a High at the appropriate ENABLED OUTPUT, A1, K1, M1 or V2. Any of the ENABLED OUTPUTS may be enabled directly through an M121 or M160 AND/NOR gate, used as an NOR Expander. Maximum input to output propagation delay for any circuit is 45 nsec.

Inputs: Each DATA INPUT pin and EXPANSION INPUT pin presents one unit load. Each INPUT ENABLE pin presents two unit loads.

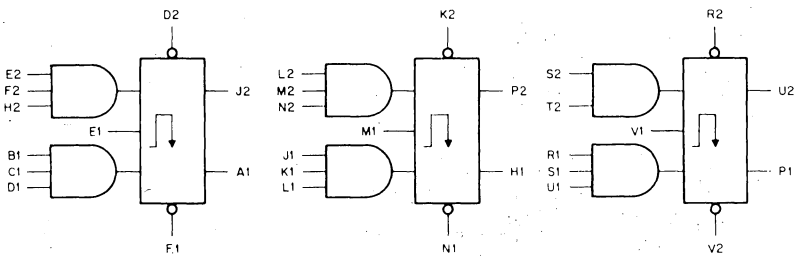
Outputs: Each output can drive up to ten unit loads.

Power: +5 volts at 50 ma. (max.)

M169 — $35

TRIPLE J-K FLIP-FLOP
M202

M SERIES



A2, +5V
C2, T1, GROUND
B2, NOT USED

The M202 contains three J-K flip-flops augmented by multiple-input and gates. For general use as gated control flip flops or buffers.

Logical operation of the J-K flip flops used in this module is identical to those flip-flops used in the M207 (described in detail) except clock, J-K inputs, inputs, direct clear, direct set and both output lines for each flip-flop are independent.

Inputs: All gate inputs represent 1 unit load. The dc set and clear input each represent two unit loads. Clock inputs represent two unit loads.

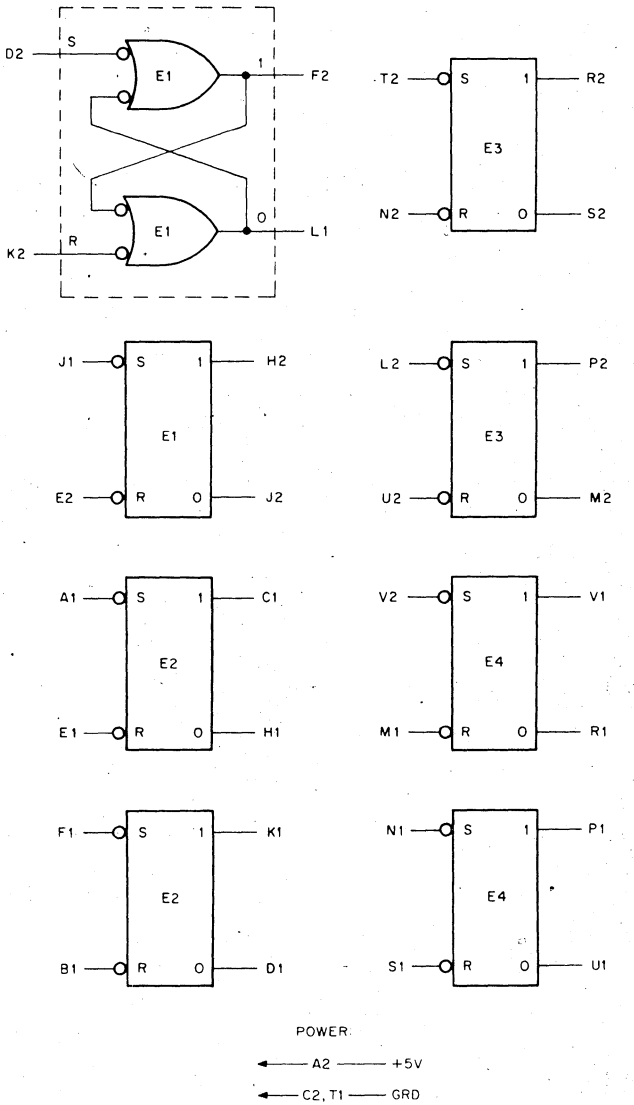
Outputs: Each output will drive 10 unit loads.

Power: +5 v at 57 ma. (max.)

M202 — $30

8-R/S FLIP-FLOPS
M203

M SERIES



M203 8-R/S FLIP-FLOPS

The M203 is made up of 8 R/S type flip-flops. Each flip-flop is made up of two 2-input NAND gates whose outputs are cross coupled. R/S flip-flops provide an inexpensive method of storage but care must be taken to inhibit placing the Set and Reset inputs low at the same time. In this case, the last of the inputs to be removed will control the final state of the flip-flop.

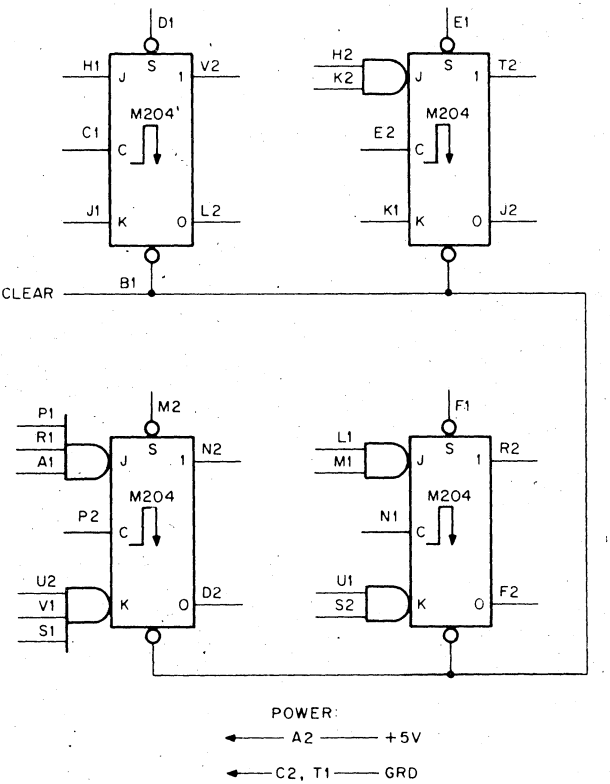
The propagation delay of the M203 is approximately 30 nsec.

Inputs: All inputs present 1 unit load.

Outputs: All outputs are capable of driving 9 unit loads.

Power: +5 volts, 55 ma. (max.)

M203 — $28



M204 GENERAL-PURPOSE BUFFER AND COUNTER

The M204 contains four J-K type flip-flops, augmented by multiple-input AND gates, for general use as gated control flip-flops or buffers. The gating scheme permits the formation of counters of most moduli up to 16, by simple connector wiring. Clock, trigger and input lines for each flip-flop are independent. A common CLEAR input is provided.

Input information is transferred to the outputs when the threshold point is reached on the trailing (negative going voltage) edge of the clock pulse.

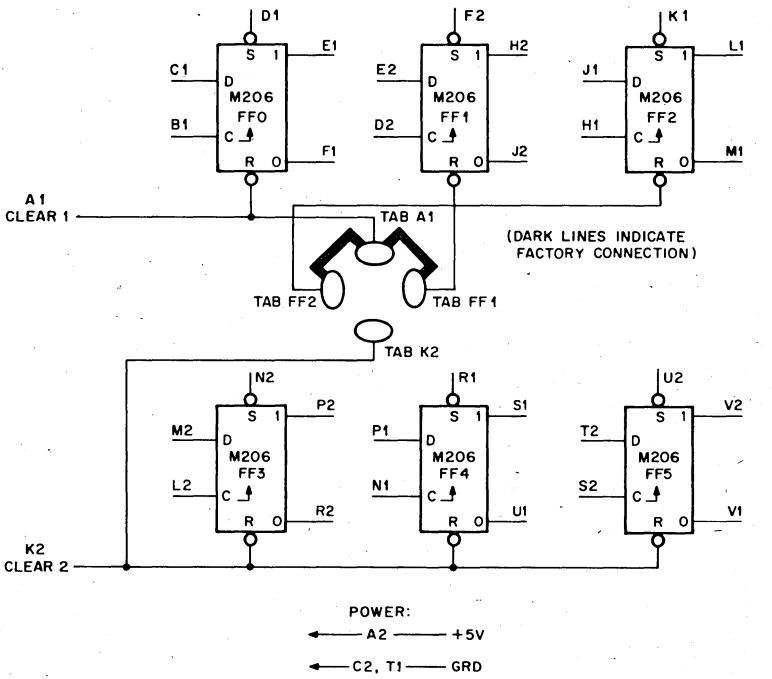
Logical operation of the J-K flip-flops used in this module is identical to the M207 (described in detail) except for the addition of dc set inputs.

Inputs: The "C" inputs present two unit loads each to the source. The dc set ("S") inputs present two unit loads each. The common CLEAR line presents 8 unit loads. All other inputs present one unit load to the source.

Outputs: Each output, before interconnection as a counter, is capable of driving 10 unit loads.

Power: +5 volts, 74 ma. (max.)

M204 — $36



M206 D TYPE FLIP-FLOPS

The M206 contains six separate D-Type flip-flops. Each flip-flop has inde pendent gated data, clock, and dc set inputs.

Provision is made on the printed circuit board for changing the configuration of the two CLEAR lines to the flip-flops. All M206 modules are supplied with the 3-3 configuration, but the grouping can be changed as follows:

CONFIGURATION	CLEAR 1 (A1)	CLEAR 2 (K2)	DELETE JUMPER	ADD JUMPER
3-3	FF0, 1, & 2	FF3, 4, & 5		
4-2	FF0 & 1	FF2, 3, 4, & 5	A1 to FF2	K2 to FF2
5-1	FF0	FF1, 2, 3, 4, & 5	A1 to FF2 A1 to FF1	K2 to FF2 K2 to FF1

Information must be present on the D input 20 nsec (max) prior to a standard clock pulse and should remain at the input at least 5 nsec (max) after the clock pulse leading edge has passed the threshold voltage. Data transferred into the flip-flop will be stable at the output within 50 nsec, maximum. Typical width requirement for the clock, dc reset and dc set pulses is 30 nsec each.

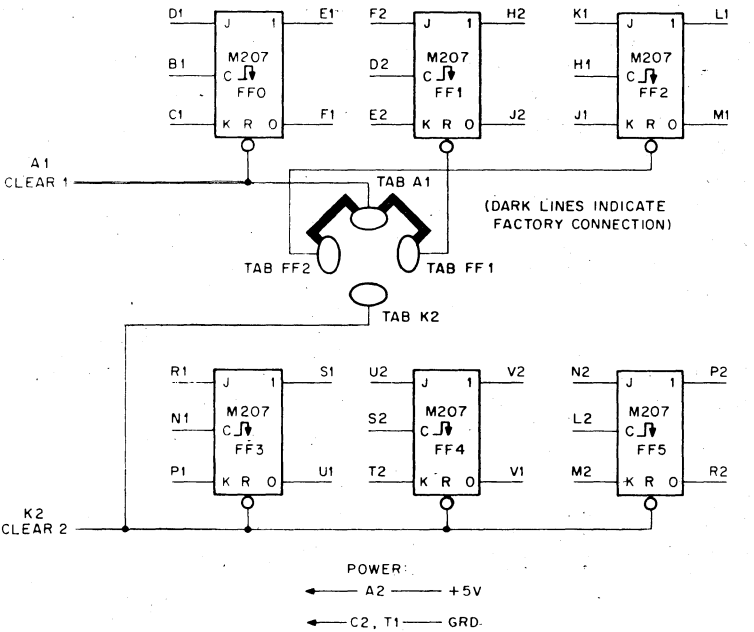
Information present on the D input is transferred to the output when the threshold is reached on the leading (positive going voltage) edge of the clock pulse.

Inputs: D inputs present 1 unit load each. C inputs present 2 unit loads each. CLEAR lines present 3 unit loads per connected flip-flop. S inputs present 2 unit loads each.

Outputs: Each output is capable of driving 10 unit loads.
Power: +5 volts, 87 ma. (max.)

A common clear for all six flip-flops can be obtained by wiring pins A1 and K2 together externally. **CAUTION:** The loading of each clear line is calculated on the basis of 3 unit loads per flip-flop. For example, the 4-2 configuration results in 12 unit loads at input K2 and 6 unit loads at input A1.

M206 — $36



M207 J-K FLIP FLOPS

The M207 contains six J-K type flip-flops which can be used as buffers, control flip-flops, shift registers, and counters. A truth table for clocked set and reset conditions appears below. Note that when the J and K inputs are both high, the flip-flop complements on each clock pulse.

STARTING CONDITION (OUTPUT)		INPUT CONDITION		RESULT AT END OF STANDARD CLOCK PULSE (OUTPUT)	
1	0	J	K	1	0
L	H	L	L	No change	
		L	H	No change	
		H	L	H	L
		H	H	H	L
H	L	L	L	No change	
		L	H	L	H
		H	L	No change	
		H	H	L	H

Application of a low level to an R input for at least 25 nsec resets the flip-flop unconditionally. Two CLEAR inputs are provided, with jumper terminals for optional clearing in groups of 3 and 3 (standard), 4 and 2, 5 and 1, or 6 and 0.

J and K inputs must be stable during the leading-edge threshold of a standard clock input and must remain stable during the positive state of the clock. Data transferred into the flip-flop will be stable at the output within 30 nsec (typical) of the clock pulse trailing edge threshold (negative going voltage).

Provision is made on the printed circuit board for changing the configuration of the two CLEAR lines to the flip-flop. All M207 modules are supplied with the 3-3 configuration, but the grouping can be changed as follows:

CONFIGURATION	CLEAR 1 (A1)	CLEAR 2 (K2)	DELETE JUMPER	ADD JUMPER
3-3	FF0, 1, & 2	FF3, 4, & 5		
4-2	FF0 & 1	FF2, 3, 4, & 5	A1 to FF2	K2 to FF2
5-1	FF0	FF1, 2, 3, 4, & 5	A1 to FF2	K2 to FF2
			A1 to FF1	K2 to FF1

Inputs: J or K inputs present 1 unit load each. C inputs present 2 unit loads each. CLEAR lines present 2 unit loads per connected flip-flop.

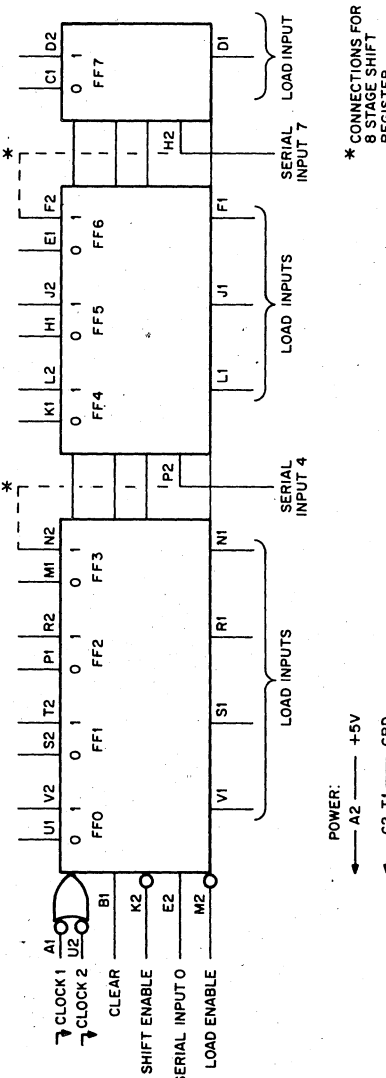
Outputs: Each output is capable of driving 10 unit loads.

Power: +5 volts, 96 ma. (max.)

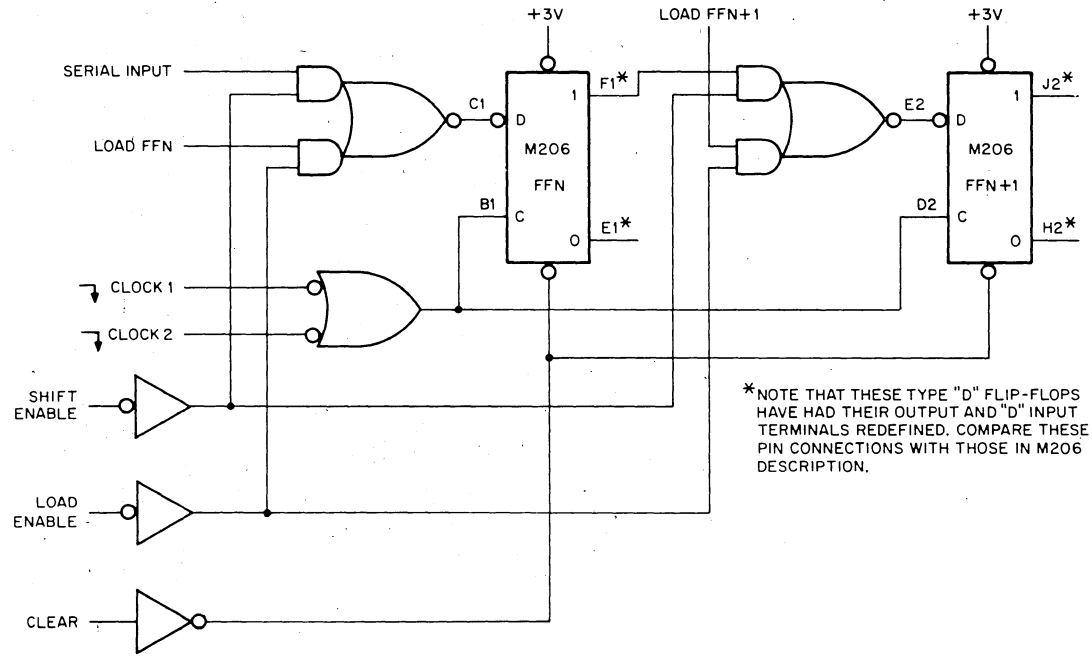
M207 — $36

8-BIT BUFFER/SHIFT REGISTER
M208

M SERIES



M208 8-BIT BUFFER/SHIFT REGISTER



TWO REPRESENTATIVE STAGES

The M208 is an internally connected 8-bit buffer/shift register. Provisions are made for gated single-ended parallel load, bipolar parellel output, and serial input. The shift register is divided into three segments:

Bits 0 through 3: Serial input to bit 0, bipolar outputs from bits 0 through 3.

Bits 4 through 6: Serial input to bit 4, bipolar outputs from bits 4 through 6.

Bit 7: Serial input to 7, bipolar outputs from bit 7.

Each of these groups shares a common shift line (the ORed CLOCK 1 and CLOCK 2 inputs) and a common parallel load line (LOAD ENABLE). To form a 6-bit shift register, for example, the true output of bit 3 is connected to the serial input of stage 4. A shift register of 8 bits may be constructed from a single module. Modules may be cascaded to form shift registers of any desired length. A few additional stages may be formed more economically from NAND and AND/NOR gates plus a D-type flip-flop. A representative stage of this type is illustrated.

Two clock inputs are provided so that individual Load and Shift clock sources may be used. Care must be taken that the clock inputs remain in the high state in the off condition because either input going to the low state will produce a positive edge at the output of the NAND gate and trigger the D type flip-flop. Data shifted or parallel loaded into the M208 will appear on the outputs within 55 nsec (max) of the clock pulse leading edge threshold. Load of Shift Enable levels and parallel data must be present at least 50 nsec prior to a clock pulse. Propagation delay from the leading edge of a CLEAR pulse to the outputs is 40 nsec max.

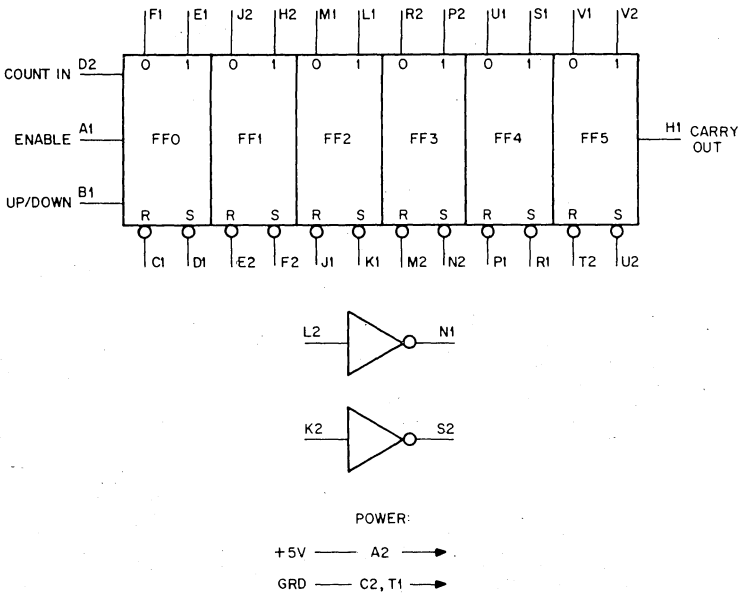
Inputs: Serial data, dc set, and enable inputs present one unit load each to the source module. Each clock input presents 2½ unit loads. The CLEAR input presents two unit loads.

Outputs: Parallel outputs are capable of driving 10 unit loads each.

Power: +5 volts, 184 ma. (max.)

BINARY UP/DOWN COUNTER
M211

M SERIES



M211 BINARY UP/DOWN COUNTER

The M211 is a 6 bit binary UP/DOWN counter. It can switch counting mode (UP or DOWN) without disturbing the contents of the counter. Maximum count rate is 10 MHz. SET/RESET inputs are available for each bit. Maximum carry propagation time is 80 ns per bit.

Enable Line: The Enable input must be negated 100 nsec. prior to an UP/DOWN level command.

The Enable input must **not** be negated earlier than 500 nsec. after the leading edge (positive going voltage) of the clock pulse.

The Enable input must be asserted at least 60 nsec. prior to the first count.

UP/DOWN Control Line: A logical 1 on this line will yield an up count.

A logical 0 on this line will yield a down count.

Carry Out: The Carry Out will yield a positive level change whenever a carry or borrow occurs.

Inputs: Count In—positive transition or pulse with less than 400 nsec rise-time. Count In presents 2 unit loads. Reset—Each reset input presents 3 unit loads. Set—Each set input presents 2 units loads. All other inputs present 1 unit load.

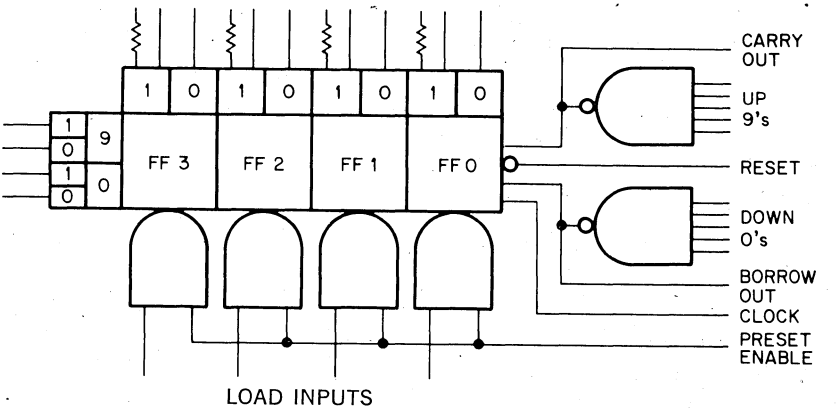
Outputs: Each flip flop output (1 or 0) can drive 8 unit loads. Carry Out can drive 10 unit loads. Each inverter output can drive 30 unit loads.

Power: +5.0 volts, 217 ma. (max.)

M211 — $75.00

BCD UP/DOWN COUNTER
M213

M SERIES



PIN	A CONNECTOR		B CONNECTOR	
	SIDE (1)	SIDE (2)	SIDE (1)	SIDE (2)
A	—	+5	—	+5
B	—	—	—	—
C	—	Ground	—	Ground
D	9 (0) Out	9 (1) Out	0 (0) Out	0 (1) Out
E	9 In	Up	0 In	Down
F	9 In	9 In	0 In	0 In
H	Carry Out	9 In	Borrow Out	0 In
J	Test Point	9 In	—	0 In
K	—	9 In	—	0 In
L	—	9 In	—	0 In
M	Test Point	Preset Enable	—	
N	—	Clock	Test Point	Reset
P	Test Point	Load FF 0	Test Point	Load FF 2
R	Test Point	Load FF 1	Test Point	Load FF 3
S	FF 0 (0)	FF 0 (1)	FF 2 (0)	FF 2 (1)
T	Ground	FF 0 (1)	Ground	FF 2 (1)
U	FF 1 (0)	FF 1 (1)	FF 3 (0)	FF 3 (1)
V	—	FF 1 (1)	—	FF 3 (1)

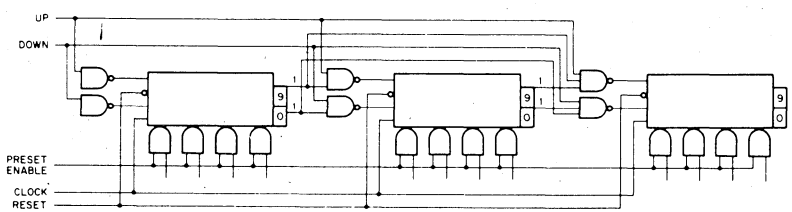
The M213 can be used to construct multi-digit synchronous counters for up/down counting in binary coded decimal. The maximum counting rate is 5 MHz. The counting direction is controlled by enabling the up or down control gate inputs. For maximum noise immunity, the up and down control lines should be kept low until counting is desired. Clock pulses that occur while the up and down lines are both low will not change the contents of the counter. Unpredictable operation will result if both the up and down lines are high at the same time. Positive clock pulses should not occur sooner than 50 ns after any change in the up or down control lines.

The "1" side of each flip-flop output is available directly for controlling nearby logic or through an isolation resistor when decoding displays are being driven at the end of long lines.

The counter may be preset by first resetting the counters and enabling the preset line. The clock input should then be pulsed once with a positive pulse to transfer data from the load inputs into the flip-flops. The up and down control lines must both be low for correct preset operation.

Counter Construction: The up and down input gate wiring for cascading M213 modules makes it possible to construct the hardware for fixed decimal point counters so that additional digits to the left or right of the decimal point can be added later as options. If the sockets are wired initially for a larger counter than is thought to be required, the unused high order digits may be left blank. Unused low order digit sockets should have pins AD2 and BD2 connected to +3 volts. When it is found that additional counter capacity or accuracy is needed, M213 modules can be plugged into the blank sockets on either side of the decimal point as required.

The diagram below shows how to connect three M213 counters for up/down counting. Notice that all the counters are clocked at the same time, but that a counter will not count unless the counters of lower significant digits all contain 9's for up counting or 0's for down counting. All unused module inputs should be connected to +3 volts.



Inputs: The input loads presented are:

CLOCK	— Eight unit loads
RESET	— Eight unit loads
PRESET ENABLE	— Four unit loads
All other inputs	— One unit load

Pulse widths required:

CLOCK	POSITIVE	> 20 nsec
RESET	NEGATIVE	> 25 nsec

Outputs: Output drive ability:

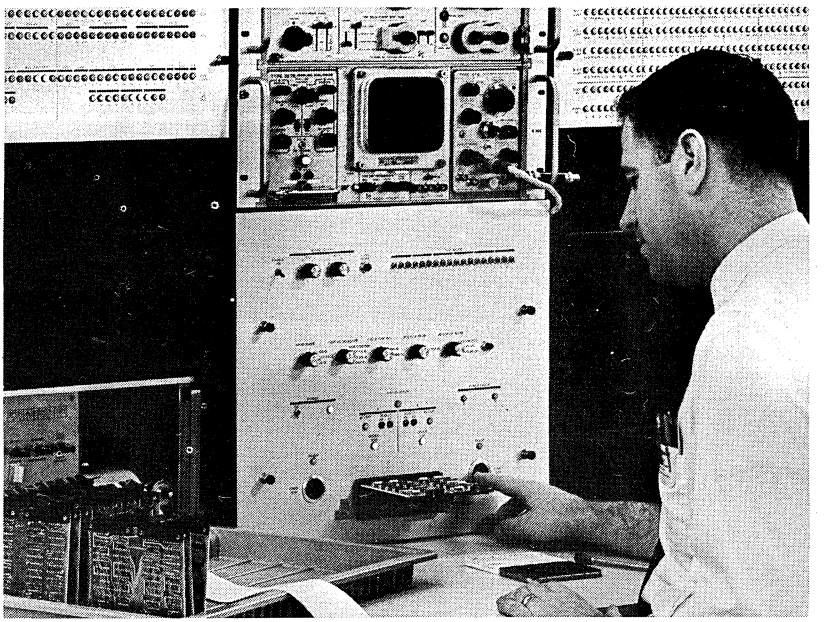
FLIP-FLOP 1 or 0	— Seven unit loads
FLIP-FLOP 1 (Resistor)	— Five unit loads
(Total load on a 1 output is 7 unit loads.)	
CARRY OUT	— Eight unit loads
BORROW OUT	— Eight unit loads

Cascade Outputs:

9 (1), 9 (0)	
0 (1), 0 (0)	Ten unit loads

Power: +5 volts at 160 ma. (max.)

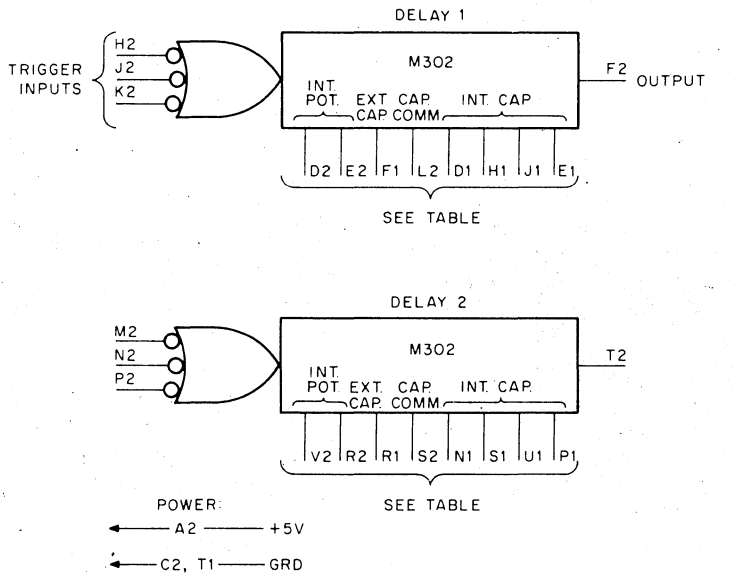
M213 — $86



DEC thoroughly tests all finished modules, performing 100 ac and dc tests in less than 5 seconds. Most testing is done automatically on one of three computer-operated test stations like this one.

DUAL DELAY MULTIVIBRATOR
M302

M SERIES



The M302 contains two delays (one-shot multivibrators) which are triggered by a level change from high to low or a pulse to low whose duration is equal to or greater than 50 nanoseconds. When the input is triggered, the output changes from low to high for a predetermined length of time and then returns to low. The basic DELAY RANGE is determined by an internal capacitor. The delay range may be increased by selection of additional capacitance which is available by connecting various module pins or by the addition of external capacitance. An internal potentiometer can be connected for fine delay adjustments within each range or an external resistance may be used. If an external resistance is used, the combined resistance of the internal potentiometer and the external resistance should be limited of 10,000 ohms.

The fall time of the input trigger should be less than 400 nonoseconds.

The delay time is adjustable from 50 nanoseconds to 7.5 milliseconds using the internal capacitors and can be extended by adding an external capacitor.

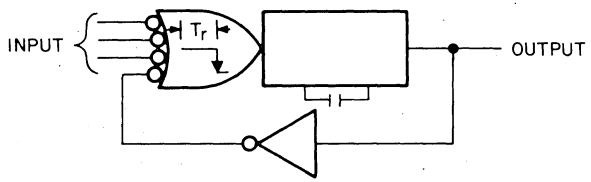
Care should be exercised in the selection of external capacitors to assure low leakage as leakage will affect the time delay.

Recovery time is determined by the size of the capacitance used. The minimum recovery time of this module is 30 nanoseconds when not using any additional capacitance. Recovery time with additional capacitance can be calculated using the formula:

$$T_r = 300\ C$$

Where T_r is in seconds
C is in farads

Recovery time is defined for this module as follows: Recovery time, T_r, is the minimum time interval which must exist before each trigger with all inputs high and the output low. The figure shown below illustrates these conditions:



Delay Range	Capacitor Value	Interconnections Required	
		Delay 1	Delay 2
50 nsec — 750 nsec	100 pf (internal)	None	None
500 nsec — 7.5 usec	1000 pf (internal)	D1 — L2	N1 — S2
5 usec — 75 usec	0.01 uf (internal)	H1 — L2	S1 — S2
50 usec — 750 usec	0.10 uf (internal)	J1 — L2	U1 — S2
500 usec — 7.5 msec	1.0 uf (internal)	E1 — L2	P1 — S2
Above 7.5 msec	Add external capacitors between specified pins	F1 — L2	R1 — S2
Adjustable Delays: connect pins to add internal adjustment potentiometer. Without a potentiometer, the delay will not recover. An external potentiometer of less than 10KΩ can be used by connecting it between E2 or R2 and ground pin C2. Use of an external adjustment resistor will cause some increase in jitter. It is recommended that leads to an external potentiometer be twisted pairs and as short as possible.		D2 — E2	V2 — R2

Inputs: Each input presents 2½ unit loads.

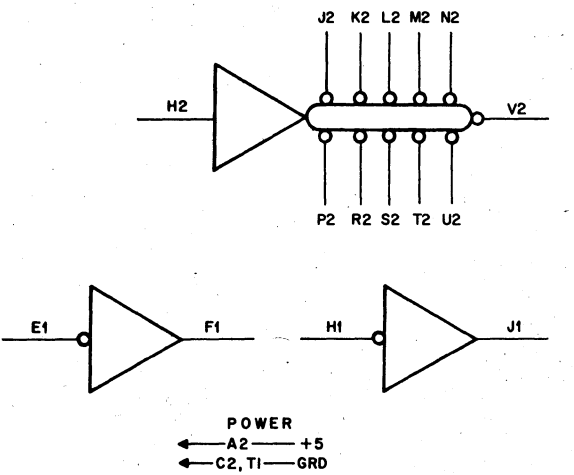
Outputs: Each output is capable of driving 25 unit loads.

Power: +5 volts, 166 ma. (max.)

M302 — $46

DELAY LINE
M310

M SERIES



The M310 consists of a tapped delay line with associated circuitry and two pulse amplifiers. The total delay is 500 nanoseconds with taps available at 50 nanosecond intervals.

The time delay is increased when the amplifier is connected to the delay line taps in ascending order as follows: J2, K2, L2, M2, N2, P2, R2, S2, T2, U2, and V2. The tap J2 yielding the minimum delay and the tap V2 yielding the maximum delay.

The pulse amplifiers are intended to be used to standardize the outputs of the delay line. The output of the pulse amplifier is a positive pulse whose duration is typically 50 to 200 nanoseconds. These amplifiers are not intended to be driven by TTL IC logic.

Inputs: Pin H2 represents four unit load.

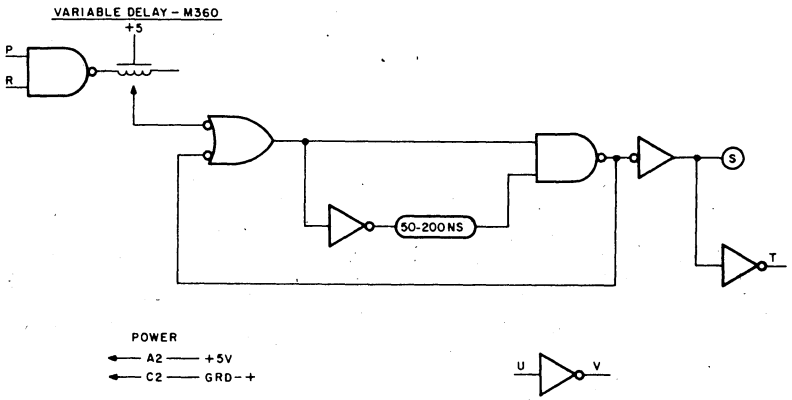
Outputs: Pin F1 and J1 outputs can drive 30 unit loads.

Power: +5 volts at 89 ma. (max.)

M310 — $58

VARIABLE DELAY
M360

M SERIES



The M360 contains an adjustable delay line with a standardizing amplifier. The delay is adjustable between the limits of 50 nanoseconds to 300 nanoseconds by means of a slotted screw which is accessible from the handle end of the module. The resolution of the delay adjustment is approximately 1 nanosecond. The output consists of a positive pulse whose width is nominally 50 to 200 nanoseconds and the leading (positive going voltage) edge of which, is delayed with respect to the leading (positive going voltage) edge of the input by a length of time as determined by the setting of the delay line adjustment.

Inputs: Pins P and R represent one TTL unit load. Pin U represents two TTL unit loads.

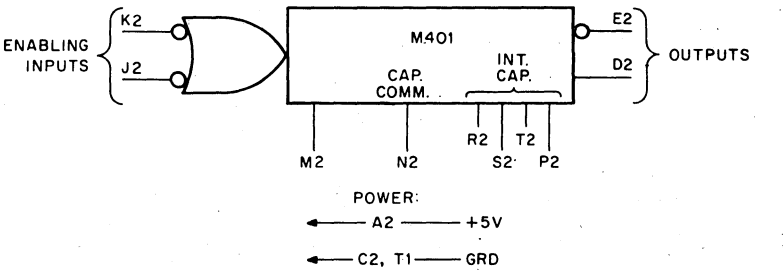
Outputs: Pin S can drive 27 TTL unit loads. Pins T and V are outputs consisting of open collector NPN transistors and can sink 30 milliamperes to ground. Voltage applied to Pins T and V must **not** exceed +20 volts.

Power: +5 volts, 50 ma. (max.)

M360 — $68

VARIABLE CLOCK
M401

M SERIES



M401 VARIABLE CLOCK

The M401 Variable Clock is a stable RC-coupled multivibrator which produces standard timing pulses at adjustable repetition rates.

The module is intended for use as the primary source of timing signals in a digital system. Repetition rate is adjustable from 175 HZ to 10 MHz in five ranges. Internal capacitors, selected by jumper pin connections, provide coarse frequency control. An internal potentiometer provides continuously variable adjustment within each range.

A two-input OR gating input is provided for start-stop control of the pulse train. A level change from high to low with fall time less than 400 nsec is required to enable the clock.

If the input is derived from the output of TTL logic and propagation time is 50 nanoseconds, as measured from the +1.5 volt point of the negative going voltage edge of the input to the +1.5 volt point of the negative going edge of the output at pin E2.

Frequency Range	Interconnections Required	
1.5 MHz to 10 MHz	(100 pf)	NONE
175 KHz to 1.75 MHz	(1000 pf)	N2 — R2
17.5 KHz to 175 KHz	(.01 μfd)	N2 — S2
1.75 KHz to 17.5 KHz	(0.1 μfd)	N2 — T2
175 Hz to 1.75 KHz	(1.0 μfd)	N2 — P2

Fine Frequency Adjustment:
Controlled by an internal potentiometer. No provision is made for any external connections.

External capacitor may be added by connection between pin N2 and ground.

The M401 may also be voltage controlled by applying a control voltage to pin M. This feature is available only in M401 modules using printed circuit board revision "E" or later. The voltage applied to Pin M should be limited to the range of 0 volts to +10.0 volts. This voltage swing will allow the frequency to be shifted by approximately 30 percent in the frequency range using the internal capacitors of 1.0, 0.1, 0.01 and 0.001 ufd. If the voltage applied to Pin M is D.C. or low frequency (below 1 KHz), Pin M will appear approximately as a +1.0 volt source with a Thevenin resistance of 800 ohms. Modulating the M401 with a 10V P-P signal about a center frequency, as derived by the application of a mean voltage of +5 volts to Pin M, will yield a typical frequency excursion of —0 in excess of ±15% about the center frequency. Typical frequency excursions which may be obtained are shown below:

Voltage applied to Pin M	CAPACITOR			
	1.0 ufd.	0.1 ufd.	0.01 ufd.	.001 ufd.
0	1.000	10.00	100.0	1000
+1	1.054	10.49	104.6	1036
+2	1.101	10.94	109.2	1071
+3	1.147	11.39	113.6	1108
+4	1.193	11.83	118.0	1142
+5	1.238	12.26	122.2	1181
+6	1.282	12.69	126.4	1271
+7	1.325	13.10	130.4	1295
+8	1.368	13.50	134.2	1312
+9	1.408	13.87	137.7	1322
+10	1.443	14.20	140.9	1323
				Output frequency in KHz

Inputs: Each enable input represents 1 unit load. Pin M, refer to text above.

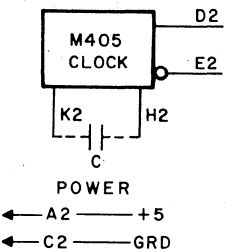
Outputs: The positive output can drive 10 unit loads; the negated output, 9 unit loads.

Power: +5 volts, 80 ma. (max.).

M401 — $55

CRYSTAL CLOCK
M405

M SERIES



The M405 clock employs a series resonant crystal oscillator to obtain a frequency stability of .01% of specified value between 0°C and +55°C. The clock frequency may be specified anywhere in the range of 5 KHz to 10 MHz by the customer.

Outputs: Outputs at pins D2 and E2 are respectively positive and negative going 0-+3 volt 50 nsec pulses. Pin D2 can drive 10 unit loads while E2 can drive only 9 unit loads. Pulses at pins D2 and E2 are time shifted by one gate delay with negative pulse at pin E2 leading the positive pulse at D2 by a maximum of 20 nsec. The output pulse width can be modified by the addition of an external capacitor between pins K2 and H2. This capacitor will increase the output pulse width by approximately 1 nsec per 2.5 mmfd of additional capacitance. Output pulse width should not exceed 100 nsec between MHz and 10 MHz and 10% of the period at any other frequency.

Power: +5 volts, 50 ma. (maximum)

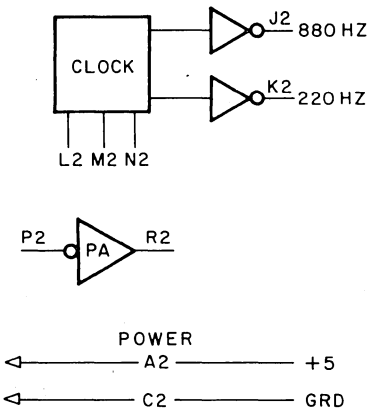
Ordering Information: When ordering the M405 always specify frequency. Allow six weeks for delivery.

Standard Stock Frequencies: 1.333 MHz, 2.000 MHz, 5.000 MHz.

M405 — $100

VARIABLE CLOCK
M452

M SERIES



The M452 is a free running clock which generates the necessary timing signals for the PDP 8/I teletype control. Frequency adjustment of this module is limited to less than 5% and the overall clock stability with respect to supply voltage and temperature variations is about 1%. The available output frequencies are 880Hz, and 220Hz. A pulse amplifier is provided for the generation of nominal 150 nsec pulses.

Inputs: The pulse amplifier input presents one unit load.

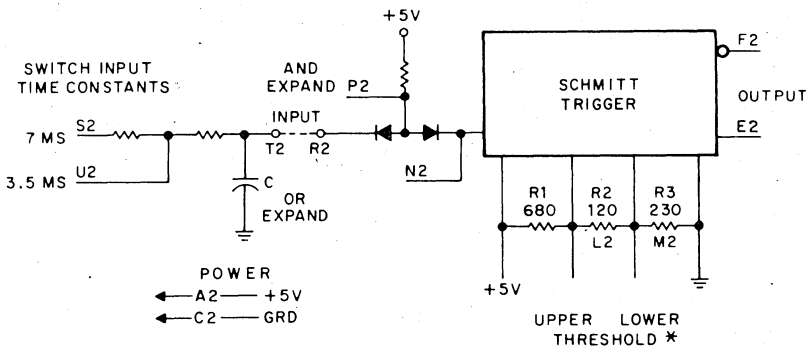
Outputs: Pin J2 drives 30 unit loads at 880Hz. Pins N2 and M2 drive 9 unit loads at 330Hz. Pin L2 drives 9 unit loads at 220Hz. Pin K2 drives 30 unit loads at 220Hz. Pin R2 drives 10 unit loads with a nominal 150 nsec positive output pulse. Under normal operating conditions, pins L2, M2, N2, are used as test points.

Power: +5 volts, 77 ma. (max.)

M452 — $40

SCHMITT TRIGGER
M501

M SERIES

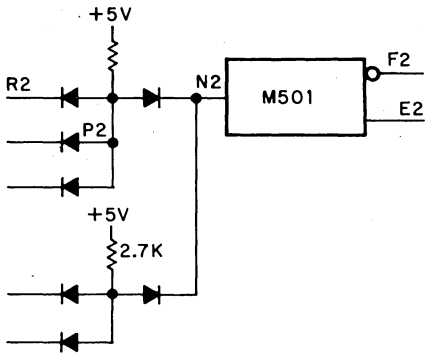


Basically a Schmitt Trigger with variable thresholds, the M501 is used as a Switch Filter, Pulse Shaper and Threshold Detector. Complementary positive logic levels are provided as outputs.

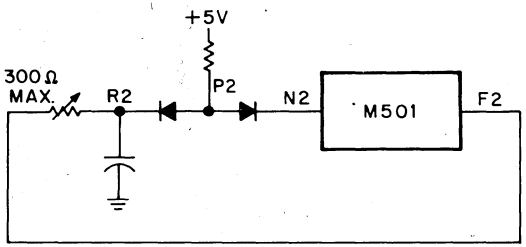
The INPUT on PIN R2 is compared with the thresholds set on PINS L2 and M2, Upper and Lower respectively. AND and OR EXPANSION may be performed on PINS P2 and N2. Module R001 and R002 provide the diodes required. An integrator is provided on the input, allowing SWITCHES to be connected to the Schmitt Trigger with contact bounce effects eliminated. Two switch TIME CONSTANTS are provided. Inputs to PIN S2 result in a 7 m sec TIME CONSTANT, to PIN U2, 3.5 m sec.

The Upper and Lower threshold are preset at 1.7 volts and 1.1 volts. They may be modified by the addition of resistor combination in parallel with the internal network. However, the upper threshold must not exceed 2.0 volts or the lower threshold fall below 0.8 v.

R_X	PARALLEL	R2	—	THRESHOLD CLOSER
R_X	PARALLEL	R1	—	UPPER RISES
R_X	PARALLEL	R3	—	LOWER FALLS



Connecting a resistor from OUTPUT PIN F TO INPUT PIN R with PIN T tied to PIN R forms an oscillator.



Inputs: Input signal swing on PIN R2 is limited to ±20 volts.

Input Pin R2: 2.7 KΩ to +5 volts or 1.8 ma. at ground.

Pin P2—AND EXPAND input
Pin N2—OR EXPAND input
Pin S2—RC SWITCH INPUT Filter 7 msec
Pin U2—RC SWITCH INPUT Filter 3.5 msec
Pin L2, M2—Available for threshold modification.

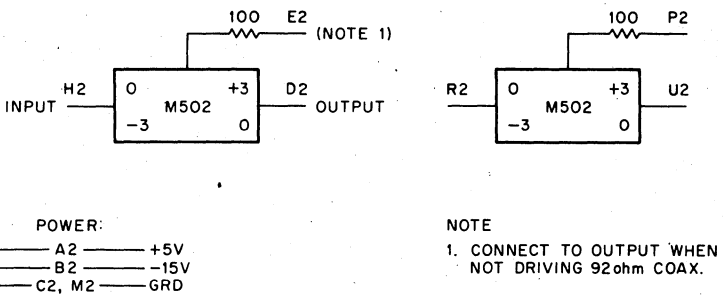
Outputs: PIN F2 goes to GROUND when the input on PIN R2 rises above the UPPER threshold, having been below the lower threshold.
PIN F2 rises to +3 volts when the input on PIN R2 falls below the LOWER threshold, having been above the upper threshold.
PIN E2 is the complement of the PIN F2.
PIN E2 can drive ten unit loads.
PIN F2 can drive eight unit loads.

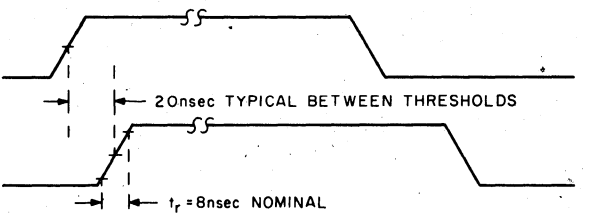
Power: +5 volts at 31 ma. (max.)

M501 — $25

NEGATIVE INPUT CONVERTER
M502

M SERIES





M502 NEGATIVE INPUT CONVERTER

INPUT	OUTPUT
0v	+3v
−3v	0v

The M502 contains two non-inverting high-speed signal converters which interface standard negative (−3v and ground) DIGITAL logic levels or pulses with M and K Series positive logic mocules. These converters provide sufficient current drive at a low output impedance for system interconnections by means of terminated 92-ohm coaxial cable. The converters operate at frequencies up to 10 MHz, with typical output rise and fall times of 8 nsec. Propagation times for output rise and fall are typically 20 nsec.

Inputs: Input loading is equivalent to a 3 ma. clamped load.

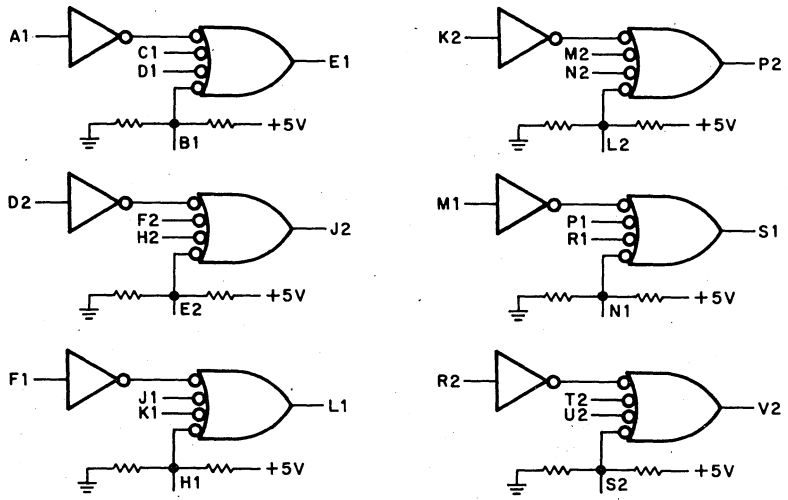
Outputs: Each output can drive terminated 92-ohm coaxial cable, and supply an additional 30 ma. at +3 volts or sink an additional 30 ma. at ground. Output rise and fall times depend on the length of coaxial cable driven. When coaxial cable is not driven, switching speeds are increased by connecting the 100 ohm resistor to the output.

Power: +5 volts, 49 ma. (max.); −15 volts, 92 ma. (max.). Add 44 ma. for each 100 ohm resistor connected to outputs.

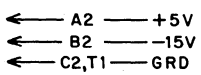
M502 — $26

NEGATIVE INPUT CONVERTER
M506

M SERIES



POWER



−3 in => 0 OUT
0 in => +3 OUT

The M506 contains three non-inverting signal converters which can be used to interface the negative logic levels or pulses of duration greater than 100 nsec to M and K Series positive logic levels of +3 volts and ground. These converters operate at frequencies up to 2 MHz with typical rise and fall propagation time of respectively 70 nsec and 40 nsec.

In addition, to the negative level inputs, each converter circuit has three additional NOR inputs for positive logic levels of +3 volts and ground. One of these inputs is tied to +3 volts so that unused inputs can be tied to a source of logic 1.

Inputs: All negative level inputs (A1, D2, . . . R2) present a 10 ma. at ground load.

Inputs B1, E2, . . . S2 present five TTL unit loads and can drive seven TTL unit loads at logic 1 if not used as an input.
All other inputs present 1 unit load.

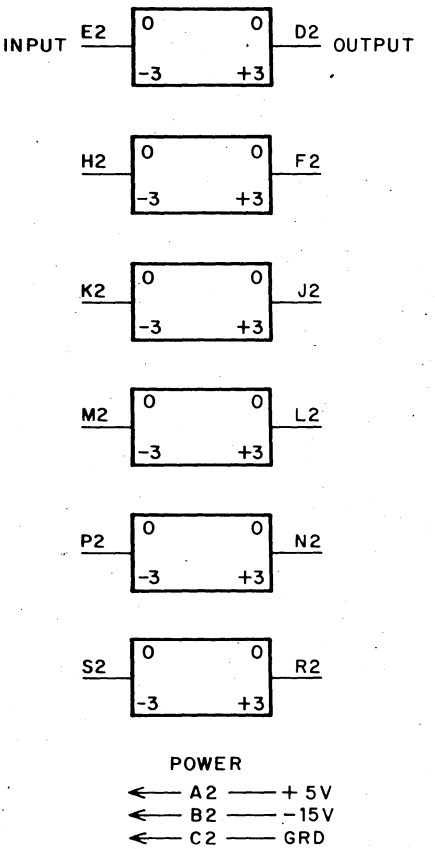
Outputs: Each output can drive 10 TTL unit loads.

Power: +5 v at 81 ma. (max.); −15v at 115 ma. (max.).

M506 — $53

BUS CONVERTER
M507

M SERIES



INPUT	OUTPUT
GRD	GRD
—3V	+3V

The M507 contains six inverting level shifters which will accept —3 volts and GRD as inputs. The input to each level shifter consists of a 10 ma. clamped load and is diode protected against positive voltage excursions.

The output consists of an open collector NPN transistor. The output of each level shifter will sink 100 ma. to GRD. The maximum voltage which may be applied to the output is +20 volts. The output transistor is protected against negative voltage excursions by a diode connected between the collector and GRD. The output rise is delayed by 100 nsec. for pulse spreading.

The principle use of this module is to convert negative voltage logic levels or pulses of duration greater than 100 nsec.

Inputs: Input loading is equivalent to a 3 ma. clamped load.

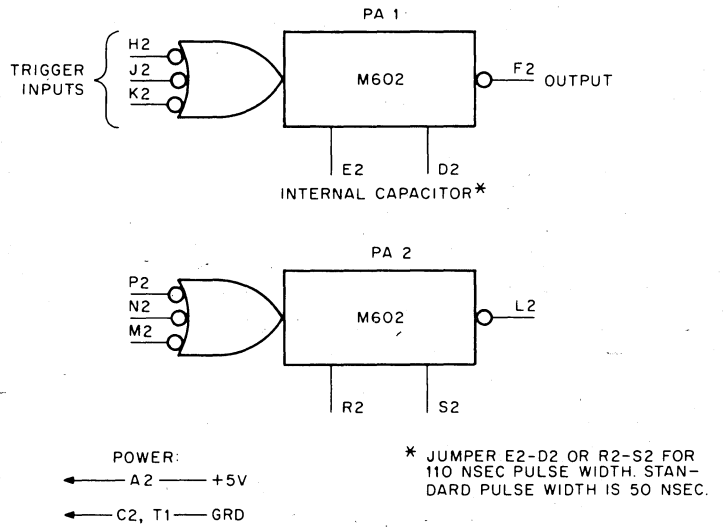
Outputs: Each output can sink 100 ma. to GRD. Maximum voltage applied to any output is +20 volts.

Power: +5 volts, 42 ma. (max.); —15 volts, 115 ma. (max.).

M507 — $45

PULSE AMPLIFIER
M602

M SERIES



The M602 contains two pulse amplifiers which provide power amplification, standardize pulses in amplitude and width, and transform level changes into a standard pulse. A negative pulse output is produced when the input is triggered by a transition from high to low. Propagation time between input and output thresholds is 30 nsec maximum. An internal capacitor is brought out to pin connections to permit the standard 50 nsec output pulse to be increased to 110 nsec (nominal). Recovery time is equal to that of the output pulse width. The input must have a fall time (10% to 90% points) of less than 400 nsec and must remain below 0.8 volts for at least 30 nanoseconds. Maximum PRF is 10 MHz.

Inputs: Each input presents 2½ unit loads.

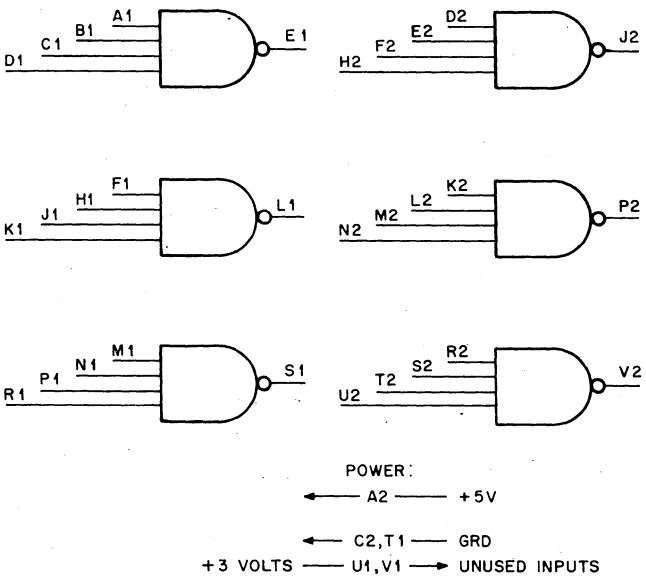
Outputs: Each output is capable of driving 30 unit loads.

Power: +5 volts, 213 ma. (max.)

M602 — $28

FOUR-INPUT POWER NAND GATE
M617

M SERIES



M617 POWER NAND GATE

The M617 contains 6 four-input NAND gates each capable of driving up to 30 unit loads. Typical gate propagation delay is 15 nsec. Physical configuration and logical operation are identical to the M117.

Inputs: Each input presents 1 unit load.

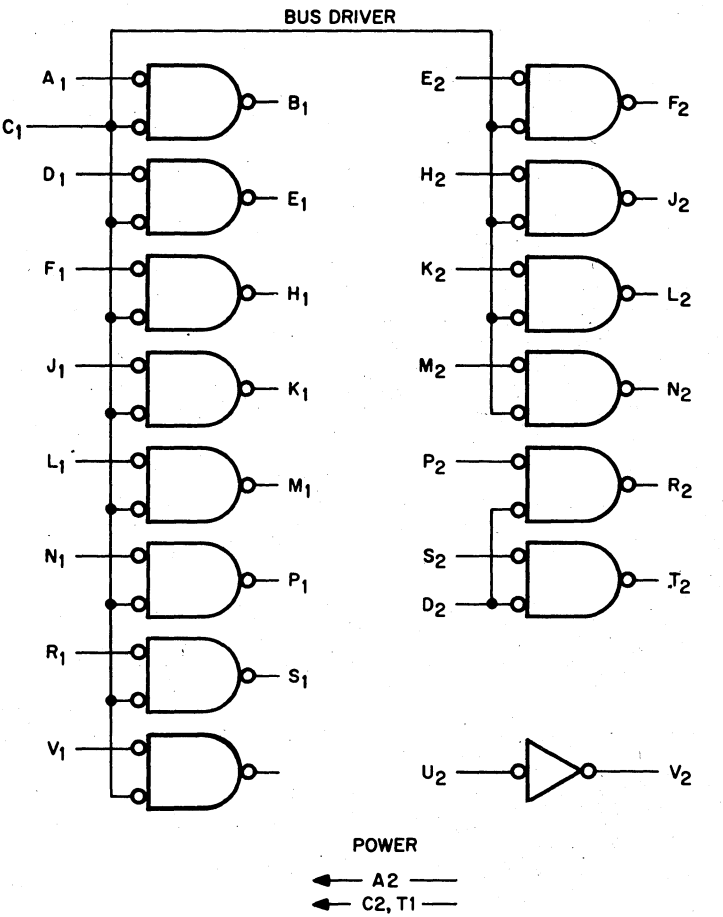
Outputs: Each output is capable of driving 30 unit loads.

Power: +5 volts, 97 ma. (max.).

M617 — $27

BUS DRIVER
M624

M SERIES



The M624 contains fifteen bus drivers intended for convenient driving of the positive input bus of either the PDP-8I or PDP-8L. Twelve of the drivers have a common gate line and would be used for DATA. There are three additional drivers, two of which share a common gate line and the third without a gate line. These three additional drivers were intended to accommodate the functions of "Program Interrupt", "IO Skip" and "Clear AC".

Inputs: Pin C1 presents 12 TTL unit loads.
Pin D2 and U2 present two unit loads.
All other input pins present one unit load.

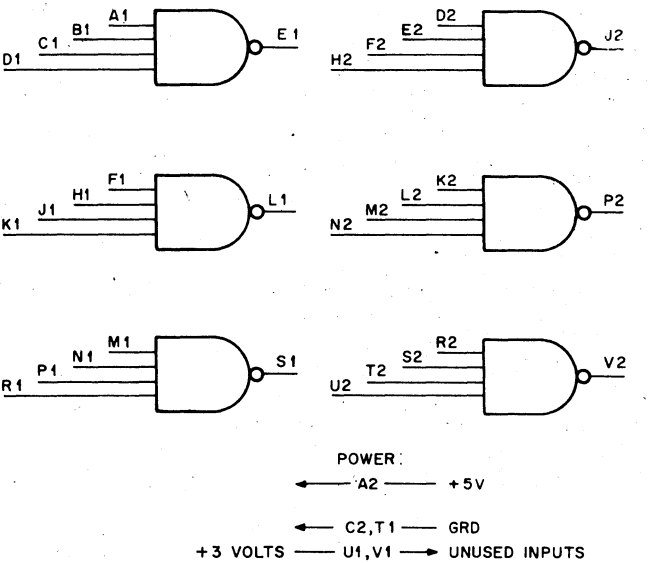
Outputs: All outputs can sink 100 ma. to ground. Voltage applied to the output should be equal to or less than +20 volts. The output consists of an open collector NPN transistor. Output rise and fall TTT are typically 30 nanoseconds when a 100 ma. resistive load to +5.0 volts is connected to a driver output.

Power: +5 volts, 89 ma. (max.). (Driver outputs not connected).

M624 — $45

NAND POWER AMPLIFIER
M627

M SERIES



M627 NAND POWER AMPLIFIER

The M627 combines power amplification with high-speed gating, specifically for high fan-out of clock or shift pulses to expanded counters and shift registers. Propagation time between input and output transitions is typically 6 nsec. To utilize the timing accuracy of this module, wire runs of minimum length are recommended.

The module may also be used as a four-input NAND gate. In the pulse amplifier application, unused inputs should be connected to the +3 volt pins provided.

Inputs: Each input presents 2½ unit loads.

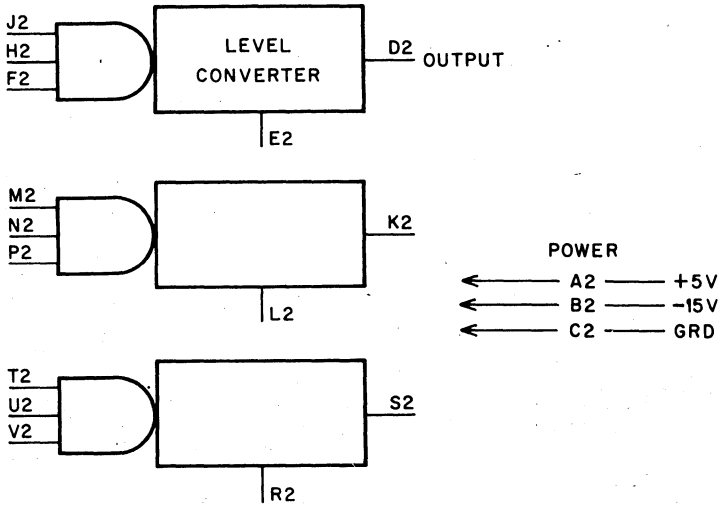
Outputs: Each output is capable of driving 40 unit loads.

Power: +5 volts, 136 ma. (max.)

M627 — $32

NEGATIVE OUTPUT CONVERTER
M650

M SERIES



NEGATIVE OUTPUT CONVERTER

0 IN => −3V
+3 IN => 0 OUT

The M650 contains three non-inverting signal converters which can be used to interface the positive logic levels or pulses (of duration greater than 100 nsec) of K and M series to DIGITAL negative logic levels of −3 volts and ground. These converters provide current drive at a low output impedance so that unterminated cables or wires can be driven with a minimum of ringing and reflections.

The converters operate at frequencies up to 2 Mc with maximum rise and fall total transition of respectively 75 nsec and 115 nsec. By grounding pin E2 (L2 or R2) the rise and fall total transition times can be increased to avoid ringing on exceptionally long lines. The converter then operates at frequencies up to 500 KHz with typical rise and fall total transition times of 500 nsec.

A positive AND condition at the input gate produces a ground output. If any input is at ground the converter output is at −3 volts.

Inputs: Each input presents 1 unit load.

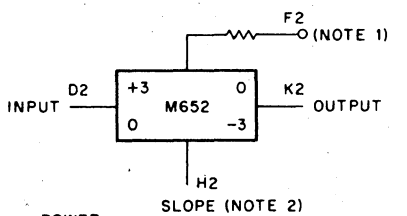
Outputs: Each output is capable of driving ma. at ground and at −3 volts.

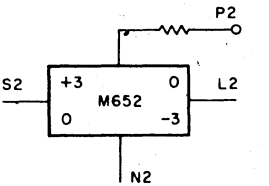
Power: +5 volts, 37 ma. (max.); −15 volts, 29 ma. (max.)

M650 — $25

NEGATIVE OUTPUT CONVERTER
M652

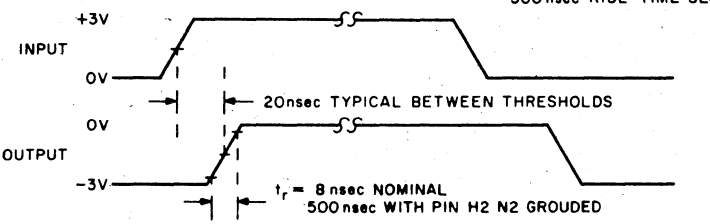
M SERIES





POWER:
A2 — +5V
B2 — -15V
C2, M2 — GRD

NOTES:
1. CONNECT TO OUTPUT WHEN NOT DRIVING 92ohm COAX.
2. CONNECT TO GROUND PIN FOR 500nsec RISE TIME SLOPE.



INPUT	OUTPUT
0v	—3v
+3v	0v

The M652 contains two non-inverting high-speed signal converters which can be used to interface the positive logic levels or pulses of the K and M Series to DIGITAL negative logic levels of —3 volts and ground. These converters provide current drive at a low output impedance so that system interconnections can be made using terminated 92-ohm coaxial cable. The conerters operate at frequencies up to 10 MHz with typical output rise and fall times of 8 nsec. Propagation times for output rise and fall are typically 20 nsec. The slope of the output transition can be decreased by grounding an internal RC network, to avoid ringing on exceptionally long lines. The converter then operates at frequencies up to 1 MHz.

Inputs: Positive logic levels of 0 and +3 volts (nominal). Input loading is 2 unit loads. Input signals more positive than +6 volts will damage the circuit.

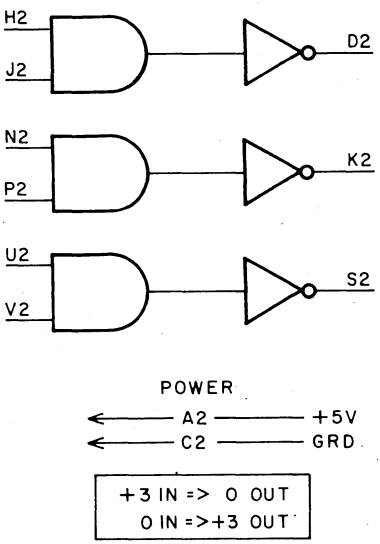
Outputs: Each output can drive terminated 92 ohm coaxial cable and supply an additional 20 ma. at ground or sink an additional 20 ma. at —3 volts. Output rise and fall times are dependent on the length of coaxial cable driven. When coaxial cable is not driven, switching speeds will be increased by connecting the 100-ohm resistor to the output.

Power: +5 volts, 122 ma. (max.); —15 volts, 202 ma. (max.)

M652 — $26

POSITIVE LEVEL DRIVER
M660

M SERIES



The M660 Cable Driver consists of three circuits each of which will drive 100 ohm terminated cable with M Series levels or pulses whose duration is greater than 100 nsec.

Inputs: Each input represents 1 unit load.

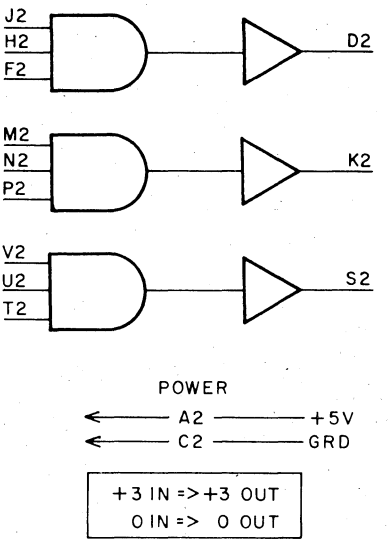
Outputs: M Series logic levels with 50 ma. drive current at logic "1" or "0".

Power: +5v, 71 ma. (max.)

M660 — $25

POSITIVE LEVEL DRIVER
M661

M SERIES



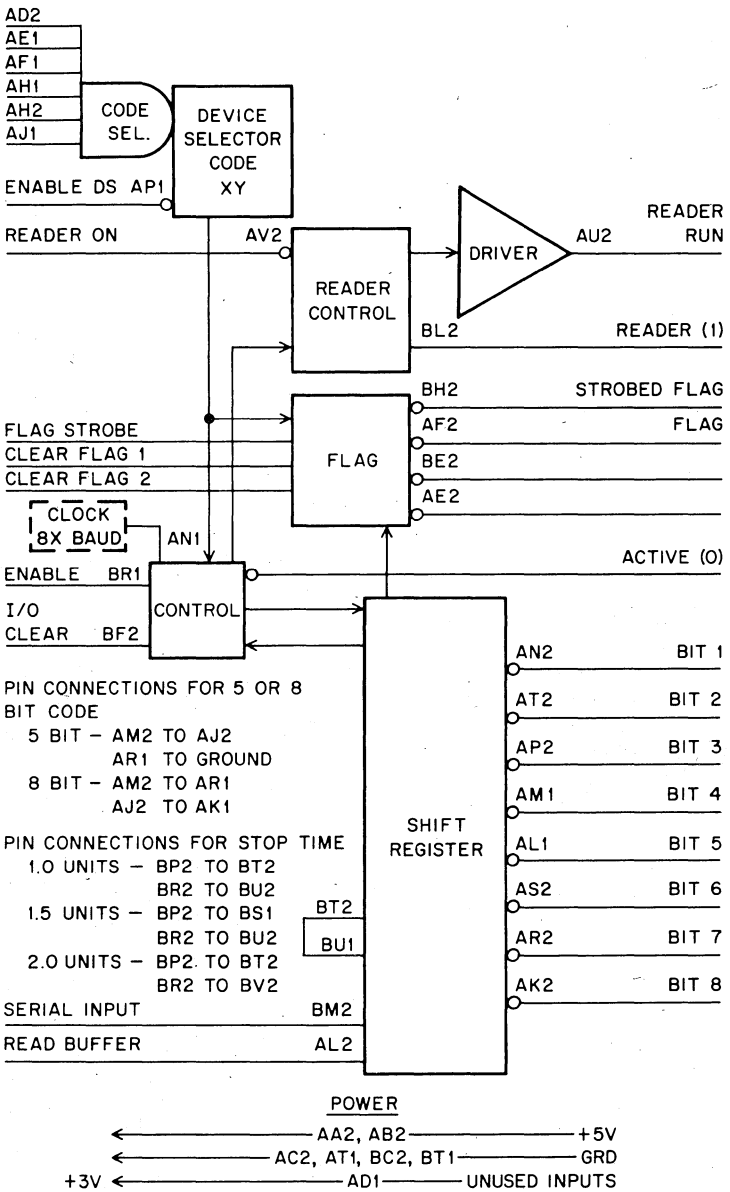
The M661 contains three circuits which may be used to drive low impedance unterminated cable with M Series logic levels or pulses whose duration is 100 nsec or greater.

Inputs: Each input represents 1 unit load.

Outputs: M Series logic "1" at 5 ma.
M Series logic "0" at 20 ma.

Power: +5v, 111 ma. (max.)

M661 — $15


AD2
AE1
AF1
AH1
AH2
AJ1
CODE SEL.
DEVICE SELECTOR CODE XY
ENABLE DS AP1
READER ON
AV2
READER CONTROL
DRIVER
AU2
READER RUN
BL2
READER (1)
BH2
STROBED FLAG
AF2
FLAG
BE2
AE2
FLAG STROBE
CLEAR FLAG 1
CLEAR FLAG 2
FLAG
CLOCK 8X BAUD
AN1
ENABLE BR1
I/O CLEAR BF2
CONTROL
ACTIVE (0)
PIN CONNECTIONS FOR 5 OR 8 BIT CODE
5 BIT – AM2 TO AJ2
AR1 TO GROUND
8 BIT – AM2 TO AR1
AJ2 TO AK1
PIN CONNECTIONS FOR STOP TIME
1.0 UNITS – BP2 TO BT2
BR2 TO BU2
1.5 UNITS – BP2 TO BS1
BR2 TO BU2
2.0 UNITS – BP2 TO BT2
BR2 TO BV2
BT2
BU1
SERIAL INPUT
BM2
READ BUFFER
AL2
SHIFT REGISTER
AN2
BIT 1
AT2
BIT 2
AP2
BIT 3
AM1
BIT 4
AL1
BIT 5
AS2
BIT 6
AR2
BIT 7
AK2
BIT 8
POWER
AA2, AB2
+5V
AC2, AT1, BC2, BT1
GRD
+3V
AD1
UNUSED INPUTS

The M706 Teletype Receiver is a serial-to-parallel teletype code converter self contained on a double height module. This module includes all of the serial-to-parallel conversion, buffering, gating, and timing (excluding only an external clock necessary to transfer information in an asynchronous manner between a serial data line or teletype device and a parallel binary device). Either a 5-bit serial character consisting of 7.0, 7.5, or 8.0 units or an 8-bit serial character of 10.0, 10.5, or 11.0 units can be assembled into parallel form by the M706 through the use of different pin connections on the module. When conversion is complete, the start and stop bits accompanying the serial character are removed. The serial character is expected to be received with the start bit first, followed by bits 1 through 8 in that order, and completed by the stop bits. Coincident with reception of the center of bit eight, the Flag output goes low indicating that a new character is ready for transmission into the parallel device. The parallel data is available at the Bit 1 through Bit 8 outputs until the beginning of the start bit of a new serial character as received on the serial input. See the timing diagram of Figure 1 for additional information.

In addition to the above listed features, the M706 includes the necessary logic to provide rejection of spurious start bits less than one-half unit long, and half-duplex system operation in conjunction with the M707. Device selector gating is also provided so that this module can be used on the positive I/O bus of either the PDP8/I or the PDP8/L. To obtain additional applications information on the M706, write for Applications Note AP-M-013.

Inputs: All inputs present one TTL unit load except where noted. When input pulses are required, they must have a width of 50 nsec or greater.

Clock: The clock frequency must be eight times the serial input bit rate (baud rate). This input can be either pulses or a square wave. Input loading on the clock line is three unit loads.

Enable: This input when brought to ground will inhibit reception of new characters. It can be grounded any time during character reception, but returned high only between the time the Flag output goes to ground and a new character start bit is received at the serial input. When not used this input should be tied to a source of +3 volts.

I/O Clear: A high level or positive pulse at this input clears the Flag and initializes the state of the control. When not used, or during reception, this input should be at ground.

Code Select Inputs: When a positive AND condition occurs at these inputs the following signals can assume their normal control functions—Flag Strobe, Read Buffer, and Clear Flag 1. Frequently these inputs might be used to multiplex receiver modules when a signal like Read Buffer is common to many modules. The inputs can also be used for device Selector inputs when the M706 is used on the positive I/O bus of the PDP8/I or PDP8/L. The code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If it is desired to bypass the code select inputs, they can be left open and the Enable D.S. line tied to ground.

Clear Flag 1: A high level or positive pulse at this input while the code select inputs are all high, will clear the Flag. When not used, this line should be grounded. Propagation delay from input rise until the Flag is cleared is a maximum of 100 nsec. The Flag cannot be set if this input is held high.

Clear Flag 2: A high level or positive pulse at this input, independent of the state of the code select inputs, will clear the Flag. All other characteristics are identical to those of Clear Flag 1.

Flag Strobe: If the Flag is set, and the code select inputs are all high, a positive pulse at this input will generate a negative going pulse at the Strobed Flag output. Propagation delay from the strobe to output is a maximum of 30 nsec.

Read Buffer: A high level or positive pulse at this input while the code select inputs are all high will transfer the state of the shift register to outputs Bit 1 through Bit 8. Final parallel character data can be read by this input as soon as the Flag output goes to ground. Output data will be available a maximum of 100 nsec after the rising edge of this input. See the timing diagram of Figure 1 for additional information.

Reader On: A low level or ground at this input will turn the internal reader flip-flop on. This element is turned off at the beginning of a received character start bit. This input can also be pulsed by tying it to one of the signals derived at output pins AE2 or BE2.

Serial Input: Serial data received on this input is expected to have a logical zero (space) equal to +3 volts and a logical 1 (mark) of ground. The input receiver on the M706 is a schmitt trigger with hysterisis thresholds of nominally 1.0 and 1.7 volts so that serial input data can be filtered up to 10% of bit width on each transition to remove noise. This input is diode protected from voltage overshoot above +5.9 volts and undershoot below —0.9 volts. Input loading is four unit loads.

Outputs: All outputs can drive ten unit loads unless otherwise specified.

Bits 1 through 8: A read Buffer input signal will transfer the present shift register contents to these outputs with a received logical 1 appearing as a ground output. If the Read Buffer input is not present, all outputs are at logical 1. When the M706 is used for reception of 5-bit character codes, the ouput data will appear on output lines Bit 1 through 5 and bits 6, 7, 8 will have received logical zeros.

Active (0): This output goes low at the beginning of the start bit of each received character and returns high at the completion of reception of bit 8 for an 8-bit character or of bit 5 for a 5-bit character. Since this signal uses from ground to +3 volts one-half bit time after the Flag output goes to ground, it can be used to clear the flag through Clear Flag 2 input while the Flag Output after being inverted can strobe parallel data out when connected to Read Buffer.

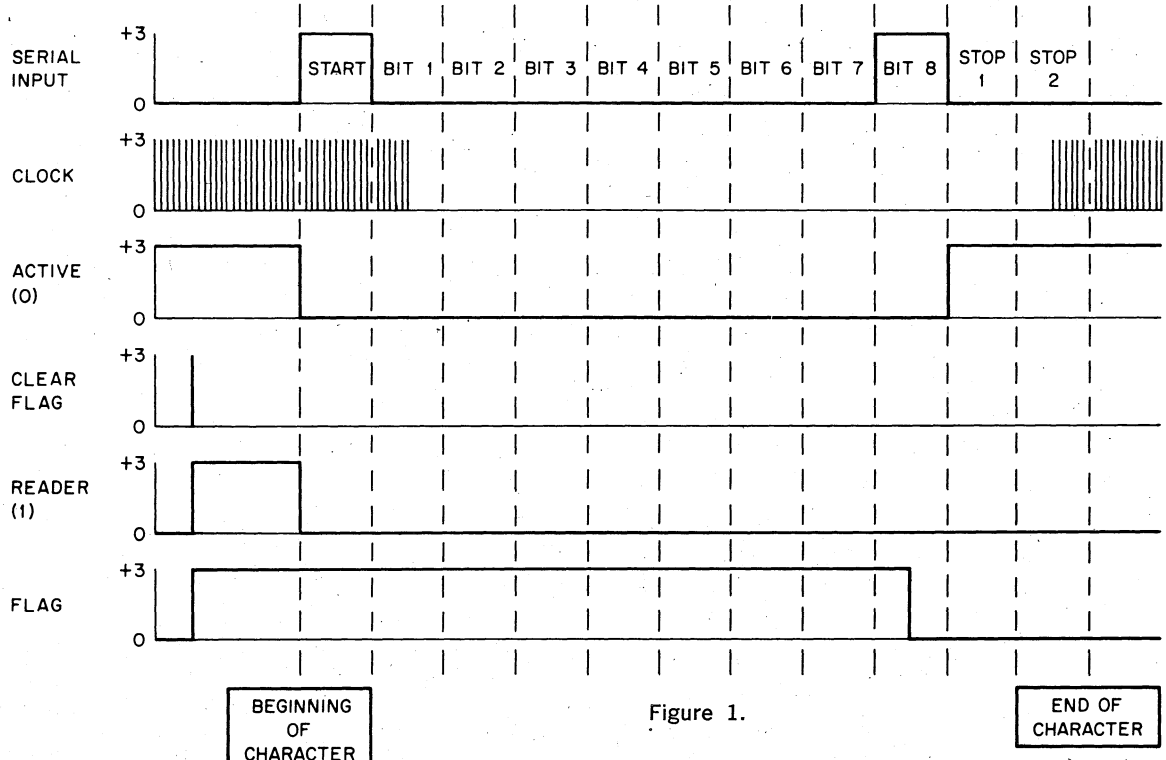


Figure 1.

TYPICAL TIMING DIAGRAM
Serial Input-Parallel Output 8-Bit (01, 111, 111)-2 Unit Stop Time

If an M706 and M707 are to be used in half duplex mode, this output should be tied to the Wait input of the M707 to inhibit M707 transmission during M706 reception. Output drive is eight unit loads.

Flag: This output falls from +3 volts to ground when the serial character data has been fully converted to parallel form. Relative to serial bit positions, this time occurs during the center of either bit 8 or bit 5 depending respectively on the character length. If the M706 is receiving at a maximum character rate, i.e. one character immediately follows another; the parallel output data is available for transfer from the time the Flag output falls to ground until the beginning of a new start bit. This is Stop bit time plus one-half bit time.

Strobed Flag: This output is the NAND realization of the inverted Flag output and Flag Strobe.

Reader (1): Whenever the internal reader flip-flop is set by the Reader ON input, this output rises to +3 volts. It is cleared whenever a start bit of a new character received on the serial input.

Reader Run: For use with Digital modified ASR33 and ASR35 teletypes which have relay controlled paper tape readers. This output can drive a 20 ma at +0.7 volts load. The common end of the load can be returned to any negative voltage not exceeding —20 volts.

Pin AE2: This output is the logical realization of NOT (Clear Flag 1 or Clear Flag 2 or I/O Clear) and is a +3 volts to ground output level or pulse depending on the input. This signal can be used to pulse Reader On for control of Reader Run as used in DEC PDP8/I or PDP8/L computers.

Pin BE2: This output is brought from +3 volts to ground by an enabled Clear Flag 1 input. It can be connected to Reader On for a different form of control of Reader Run.

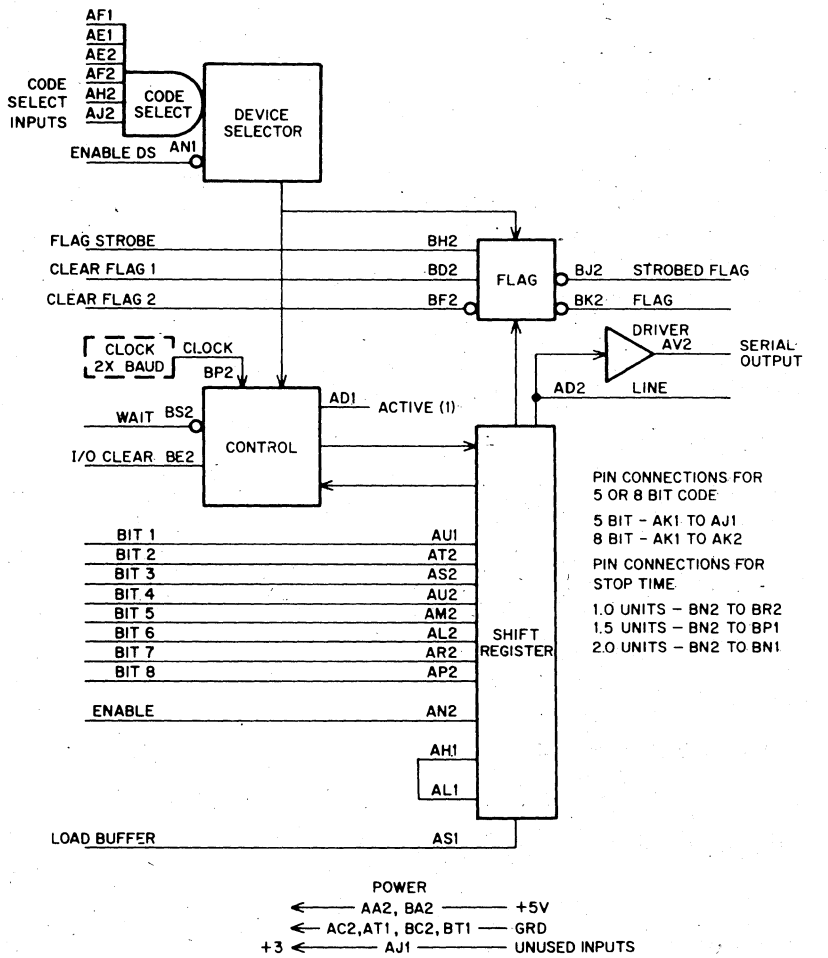
+3 Volts: Pin AD1 can drive ten unit loads at a +3 volt level.

Power: +5 volts at 400 ma. (max.).

M706 — $175

TELETYPE TRANSMITTER
M707

M SERIES



The M707 Teletype Transmitter is a parallel-to-serial teletype code converter self contained on a double height module. This module includes all of the parallel-to-serial conversion, buffering, gating, and timing (excluding only an external clock) necessary tot ransfer information in an asynchronous manner between a parallel binary device and a serial data line or teletype device. Either a 5-bit or an 8-bit parallel character can be assembled into a 7.0, 7.5, or 8.0 unit serial character or a 10.0, 10.5, or 11.0 unit serial character by the M707 through the use of different pin connections on the module. When conversion is complete, the necessary start bit and selected stop bits (1.0, 1.5, or 2.0 units) have been added to the original parallel character and transmitted over the serial line. The serial character is transmitted with the start bit first, followed by bits 1 through 8 in that order, and completed by the stop bits. Coincident with the stop bit being put on the serial line, the Flag output goes low indicating that the previous character has been transmitted and a new parallel character can be loaded into the M707. Transmission of this new character will not occur until the stop bits from the previous character are completed. See the timing diagram of Figure 1 for additional information.

In addition to the above listed features, the M707 includes the necessary gating so that it can be used in a half-duplex system with the M706. Device selector gating is also provided so that this module can be used on the positive bus of either the PDP8/I or the PDP8/L. To obtain additional applications information on the M707 write for Applications Note AP-M-013.

Inputs: All inputs present one TTL unit load with the exception of the Clock input which presents ten unit loads. Where the use of input pulses is required, they must have width of 50 nsec or greater.

Clock: The clock frequency must be twice the serial output bit rate. This input can be either pulses or a square wave.

Bits 1 through 8: A high level at these inputs is reflected as a logic 1 or mark in the serial output. When a 5-bit code is used, bit inputs 1 through 5 should contain the parallel data, bit 6 should be considered as an Enable, and bits 7, 8 and Enable should be grounded.

Enable: This input provides the control flexibility necessary for transmitter multiplexing. When grounded during a Load Buffer pulse, this input prevents transmission of a character. It can be driven from the output of an M161 for scanning purposes or in the case of a single transmitter, simply tied to +3 volts.

Wait: If this input is grounded prior to the stop bits of a transmitted character, it will hold transmission of a succeeding character until it is brought to a high level. A ground on this line will not prevent a new character from being loaded into the shift register. This line is normally connected to Active (0) on a M706 in half duplex two wire systems. When not used, this line should be tied to +3 volts.

Code Select Inputs: When a positive AND condition occurs at these inputs the following signals can assume their normal control functions—Flag Strobe, Load Buffer, and Clear Flag 1. Frequently these inputs might be used to multiplex transmitter modules when signals like Load Buffer are common to many modules. These inputs can also be used for device selector inputs when the M707 is used on the positive bus of the PDP8/I or PDP8/L. The

code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If it is desired to by-pass the code select inputs, they can be left open and the Enable DS line tied to ground.

Clear Flag 1: A high level or positive pulse at this input while the code select inputs are all high, will clear the Flag. When not used, this line should be grounded. Propagation delay from input rise until the Flag is cleared at the Flag output is a maximum of 100 nsec. The Flag cannot be set if this input is held at logic 1.

Clear Flag 2: A low level or negative pulse at this input will clear the Flag. When not used this input should be tied to +3 volts. The Flag will remain cleared if this input is grounded. Propagation from input fall to Flag output rise is a maximum of 80 nsec. If it is desired to clear the flag on a load buffer pulse, Clear Flag 2 can be tied to pin AR1 of the module.

Flag Strobe: If the Flag is set, and the code select inputs are all high, a positive pulse at this input will generate a negative going pulse at the Strobed Flag output. Propagation delay from the strobe to output is a maximum of 30 nsec.

I/O Clear: A high level or positive pulse at this input clears the Flag, clears the shift register and initializes the state of the control. This signal is not necessary if the first serial character transmitted after power turn-on need not be correct. When not used, or during transmission, this input should be at ground.

Load Buffer: A high level or positive pulse at this input while the code select inputs are all high will load the shift register buffer with the character to be transmitted. If the Enable input is high when this input occurs, transmission will begin as soon as the stop bits from the previous character are counted out. If a level is used, it must be returned to ground within one bit time (twice the period of the clock).

Outputs: All outputs present TTL logic levels except the serial output driver which is an open collector PNP transistor with emitter returned to +5 volts.

Serial Output: This open collector PNP transistor output can drive 20 ma into any load returned to a voltage between +4 volts and −15 volts. A logical output or mark is +5 volts and a logical 0 or space is an open circuit. If inductive loads are driven by this output, diode protection must be provided by connecting the cathode of a high speed silicon diode to the output and the diode anode to the coil supply voltage.

Line: This output can drive ten TTL unit loads and presents the serial output signal with a logical 1 as +3 volts and logical 0 as ground.

Active: During the time period from the occurrence of the serial start bit and the beginning of the stop bits, this output is high. This signal is often used in half duplex systems to obtain special control signals. Output drive is eight TTL unit loads.

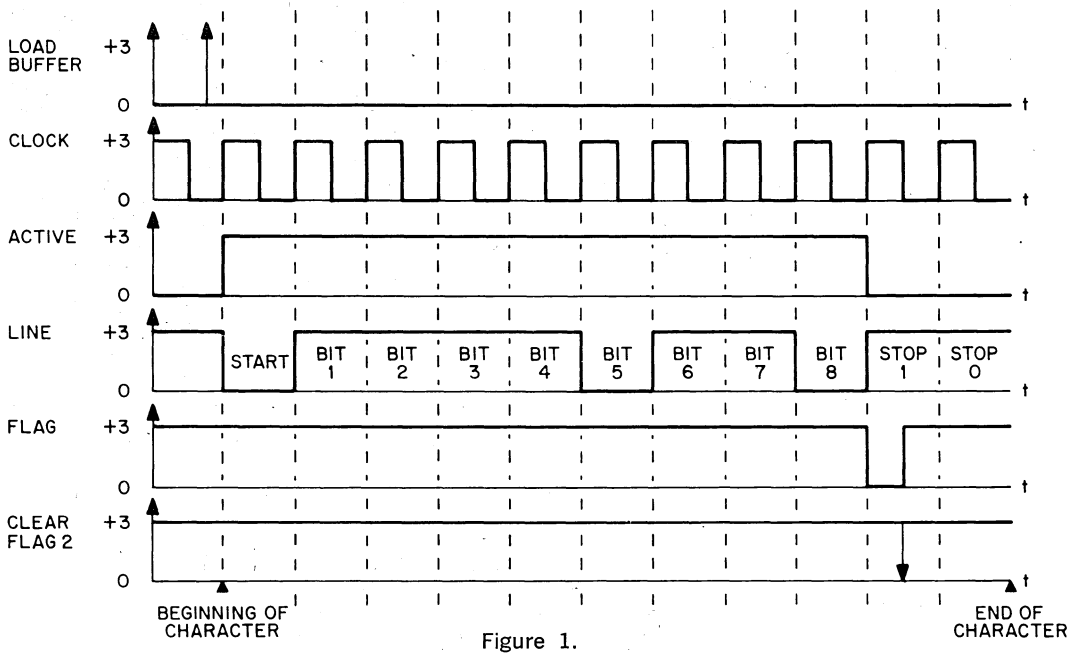


Figure 1.

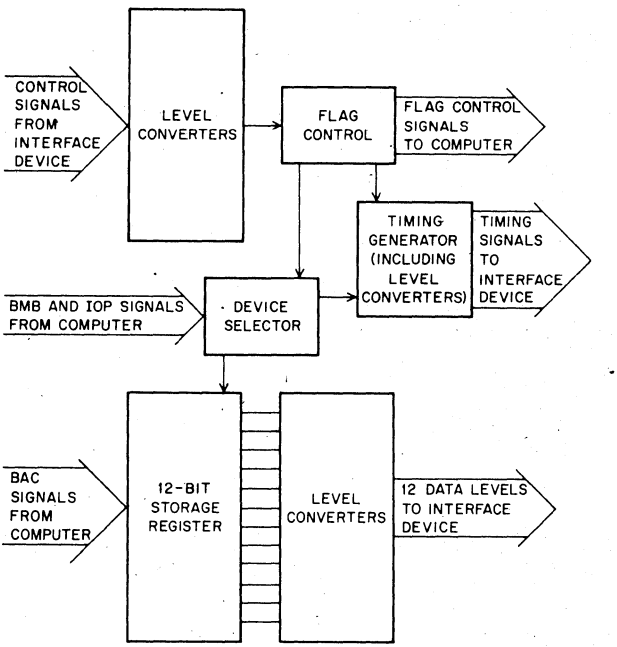
Typical Timing Diagram, Parallel input, 8-Bit Character (11, 110, 110) With two bit Stop time.

Flag: This output falls from +3 volts to ground at the beginning of the stop bits driving a character transmission. The M707 can now be reloaded and the Flag cleared (set to +3 volts). This output can drive ten TTL unit loads.

Strobed Flag: This output is the NAND realization of the inverted Flag output and Flag Strobe. Output drive is ten TTL unit loads.
+3 volts: Pin BJ1 can drive ten TTL unit loads at a +3 volt level.

Power: +5 volts at 375 ma. (max.)

These pantograph-controlled insertion machines position and crimp pre-tested components onto four module boards at a time. A press will cut the modules apart after assembly is completed, minimizing handling up to that point.



The M730 and M731 interface modules provide extremely flexible interface control logic to connect devices, systems, and instruments to the output half of the programmed I/O transfer bus of either a PDP8/I or a PDP8/L positive bus computer. Peripheral equipment which operates either asynchronously or synchronously to a computer and expects to receive data from that computer, can to a large degree be interfaced by either the M730 or M731. Basic restrictions on the device or system to be interfaced are simply that it receive data in parallel, provide one or more control lines, and operate at a data transfer rate of less than 20 KHz. Complete interfaces to such peripheral gear as card punches and other repetitive devices is possible using the M730 and M731; however part of the controlling functions, such as counting etc. must be performed by computer software.

Functionally, these modules contain five distinct sections which are as follows:

1. Device Selector—This logic network converts the buffered memory buffer (BMB) signals and IOP timing pulses from the computer into internal module control pulses.

2. Timing Generator—Through the use of device selector signals, control signals from the interfaced device, and module jumpers, this unit can supply variable width pulses or synchronous control levels at amplitudes specified in section 5 below.

3. Storage Register—This 12-bit flip-flop buffer register provides output data storage for information to be transmitted to the interfaced device.

4. Flag Control—Provisions for generation of I/O Skip and Program Interrupt signals for the computer are made in this area.

5. Level Converters—All level converters from the storage register or timing generator are open—collector transistor types which can drive 30 ma at ground. The M730 has npn drivers and can interface loads returned to a maximum positive supply of +20 volts and the M731 has pnp drivers which can interface loads returned to a maximum negative supply of −20 volts. Level converters which input control signals to the Flag control can receive signals of the same polarity and magnitude as the output drivers can sustain.

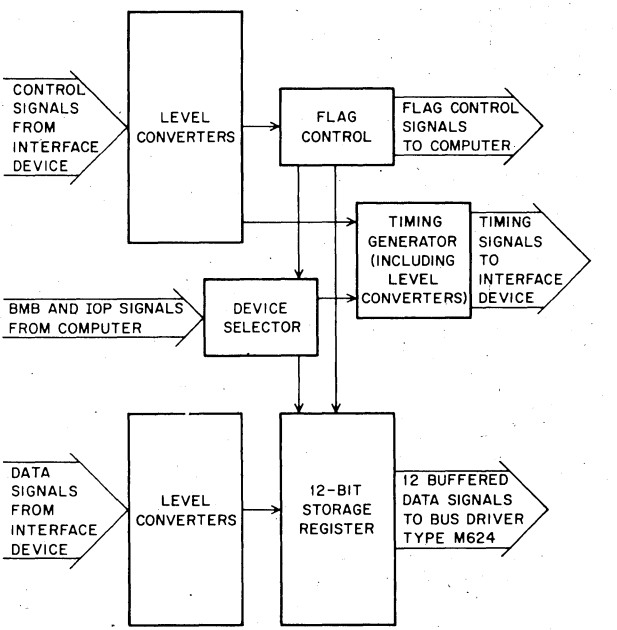
Thresholds on the input converters are +1.5 volts and −1.5 volts for the M730 and M731 respectively. All positive voltage levels are compatible with K and M series and all negative voltage signals are compatible with R, B and W Series.

For additional information, technical specifications and applications assistance, a Digital module specialist can be contacted at any Digital Sales office. Application Note AP-M-017 contains useful information concerning the use of the M730 and M731.

M730 — $185
M731 — $185

BUS INTERFACE
TYPES M732 & M733

M SERIES



The M732 and M733 interface modules provide extremely flexible interface control logic to connect devices, systems, and instruments to the input half of the programmed I/O transfer bus of either a positive bus PDP8/I or PDP8/L computer. Peripheral equipment which operates either asynchronously or synchronously to a computer and expects to transmit data to that computer, can to a large degree be interfaced by either the M732 or M733. Basic restrictions on the device or system to be interfaced are simply that it transmit data in parallel, provide one or more control lines, and operate at a data transfer rate of less than 20KHZ. Complete interfaces to such peripheral gear as card readers and other repetitive devices is possible using the M732 and M733; however, part of the controlling functions such as counting, etc., must be performed by computer software.

Functionally, these modules contain five distinct sections which are as follows:

1. Device Selector—This logic network converts the buffered memory buffer (BMB) signals and IOP timing pulses from the computer into internal module control pulses.

2. Timing Generator—Through the use of device selector signals, control signals from the interfaced device, and module jumpers, this unit can supply variable width pulses or synchronous control levels at amplitudes specified in section 5 below.

3. Storage Register—This 12-bit flip-flop buffer register provides input data storage of information received from the interfaced device. Information is loaded into this register by a control line from the peripheral.

4. Flag Control—Provisions for generation of I/O Skip and Program Interrupt signals for the computer are made in this area.

5. Level Converters—All level converters from the timing generator are open collector transistor types which can drive 30 ma at ground. The M732 has npn drivers and can interface loads returned to a maximum positive supply of +20 volts and the M733 has pnp drivers which can interface to a maximum negative supply of −20 volts. Level converters which input control and data signals to these modules can receive signals of the same polarity and magnitude as the output drivers can sustain. Thresholds on the input converters are +1.5 volts and −1.5 volts for the M732 and M733 respectively.

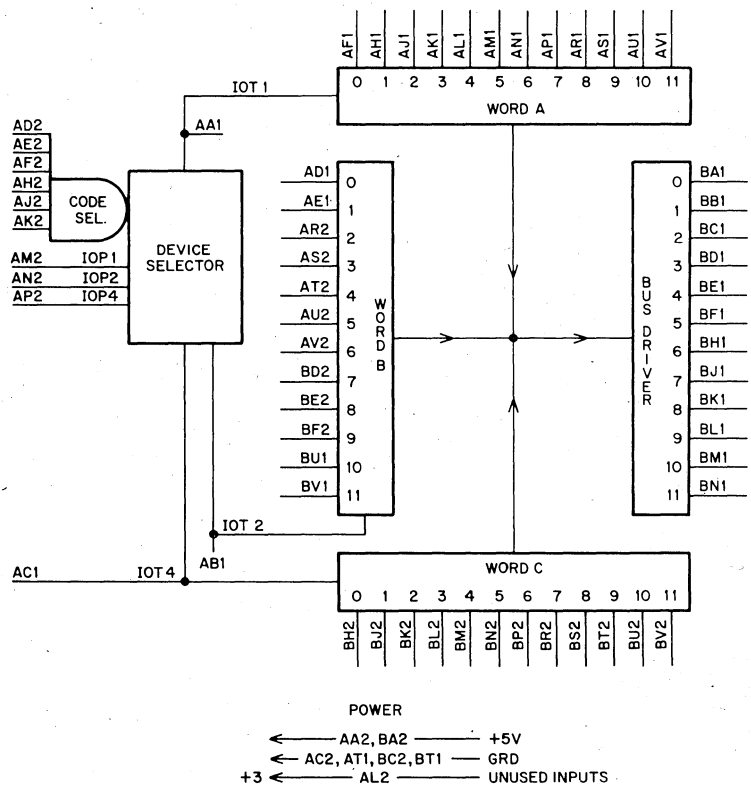
   All positive voltage levels are compatible with K and M Series and all voltage signals are compatible with R, B, and W Series.

For additional information, technical specifications and applications assistance, a Digital module specialist can be contacted at any Digital Sales Office. Application Note AP-M-018 contains useful information concerning the use of the M732 and M733.

M732 — $185.00
M733 — $190.00

I/O BUS INPUT MULTIPLEXER
M734

M SERIES



The M734 is a double height, single width module and is a three word multiplexer used for strobing twelve-bit words on the positive voltage input bus; usually the input of the PDP8/I or the PDP8/L. Device selector gating is provided. The data outputs of the M734 Multiplexer consist of open collector npn transistors which allow these outputs to be directly connected to the bus. All inputs present one TTL unit load and function as follows:

Code select Inputs: When a positive AND condition occurs at these inputs, the pulse inputs IOP1, IOP2, and IOP4 are enabled for use in strobing input data. The code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If all select inputs are not required, unused inputs must be tied to a source of +3 volts (Pin AL2). These inputs are all clamped so that no input can go more negative than —0.9 volts.

IOP1, 2, 4: These three 50 nsec or longer positive pulse inputs strobe respectively 12-bit words A, B, and C into the bus driver. All three lines are clamped so that no input can go more negative than —0.9 volts.

Data inputs: Bit 0-11 on words A, B, and C are strobed in 12-bit words as above. Bus driver output lines correspond numerically (0-11) to the selected word input lines (0-11). A high data input will force a bus driver output to ground during a data strobe. Inputs must be present at least 30 nsec prior to issuance of IOP 1, 2, or 4.

Bus driver: These open collector npn transistor bus driver outputs can sink 30 ma at ground. The maximum output voltage must not exceed +20 volts. Each driver output is protected from negative undershoot by a diode clamp. When this module is used with the PDP8/I or PDP8/L, these outputs would be connected to the accumulator input lines of the I/O bus. Typical rise and fall TTT at these outputs with a 30 ma resistive load are 100 nsec.

Data Strobes: Pins AA1, AB1, and AC1 can each drive 18 TTL unit loads. These outputs appear coincident with IOP1, IOP2, and IOP4 respectively only if the code select inputs are all high.

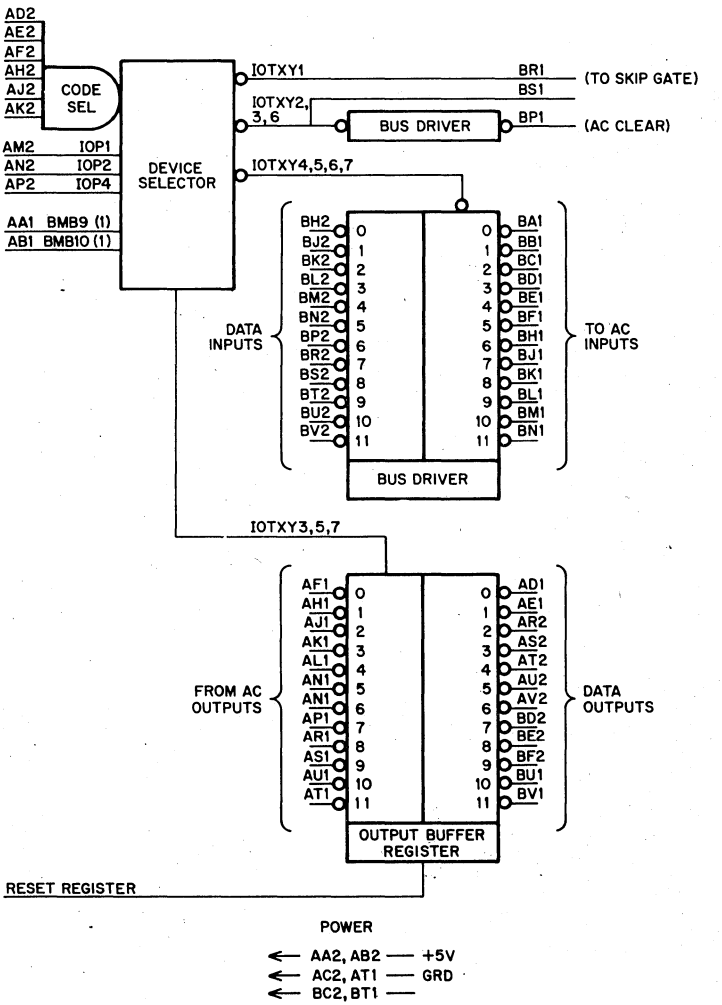
+3V—Pin AL2 can drive 19 inputs at a high logic level.

Power: +5 volts at 290 ma. (max.).

M734 — $110.00

I/O BUS TRANSFER REGISTER
M735

M SERIES



The M735 provides one 12-bit input bus driver and one 12-bit output buffer register for input and output data transfers on the positive I/O bus of either a PDP8/I or a PDP8/L. Device selector gating plus additional signal lines provide the flexibility necessary for a complete interface with the exception of flag sense signals. Use of the M735 is not restricted to a computer, as it can be used in many systems to provide reception and transmission of data over cables.

Inputs:
All inputs present one TTL unit load with few exceptions as noted in the functional descriptions below:

Code Select Inputs: When a positive AND condition occurs at these inputs, the pulse input gates for IOP1, IOP2, and IOP4 are enabled for use as detailed below. The code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If all select inputs are not required, unused inputs must be tied to a source of +3 volts. These inputs are all clamped so that no input can go more negative than —0.9 volts. When this module is used with the PDP8/I or PDP8/L these inputs would be connected to BMB outputs 3-8 to generate a device code. Where required in discussions below, this 6-bit device code will be referred to as code XY.

IOP1, 2, 4, BMB9(1) and BMB10(1): These three IOP's 50 nsec or longer positive pulse inputs, in conjunction with control level inputs BMB9(1) (Pin AA) and BMB10(1) (Pin AB1) provide all of the necessary signals for operation of this module. Table 1 below indicates the recommended use of these pulses and levels. A"1" or "0" in this table indicates the presence or absence respectively of a pulse (an IOP) or the logic level at pins AA1 or AB1.

The M735 module operation as associated with the various mnemonic IOT codes is quite explicit with the exception of IOTXY5. This code (IOTXY5) would be used to load zeros into the M735 with IOTXY1 and then to load into the AC the data present at the data inputs of the bus driver when IOTXY4 occurs. In this particular operation the AC has been effectively cleared as the content of the AC was zero during IOTXY1 thereby allowing the transfer of data into the AC without the use of the AC clear command usually generated by IOT2.

IOP 4	IOP 2	IOP 1	BMB 9(1)	BMB 10(1)	PDP/8 Mnemonic	Module Operation
0	0	1	0	0	IOTXY1	+3V → OV output pulse on pin BR1 used for skip function.
0	1	0	0	1	IOTXY2	+3V → OV output pulse on pin BS1, bus driver output on BP1 pulsed to ground and is used for the AC clear function.
0	1	1	0	1	IOTXY3	Load output register from accumulator outputs on IOP1 execute IOTXY2.
1	0	0	1	0	IOTXY4	Data inputs strobed onto accumulator inputs.
1	0	1	1	0	IOTXY5	Load output register on IOP1, Execute IOTXY4.
1	1	0	1	1	IOTXY6	Execute IOTXY2, and IOTXY4.
1	1	1	1	1	IOTXY7	Execute IOTXY3, and IOTXY4.

Although it is not implicit from Table 1, BMB9(1) and BMB10(1) inputs are gated in a positive OR circuit, so that when the M735 is not used on a PDP8/I or PDP8/L I/O bus one of these inputs can be grounded and the other used for control. They must appear at least 50 nsec prior to an IOP pulse. If the M735 is used with one of the above computers, these inputs must be tied to the corresponding I/O bus lines. The input load on IOP1 is two TTL unit loads. All five inputs are clamped so that no input can go more negative than —0.9 volts.

Data Inputs: Each data input when at ground, enables the corresponding bus driver output to be pulsed to ground during IOTXY4. A high input will inhibit the bus driver from being strobed. Since each input is ANDed with IOTXY4, any change of data after this strobe begins will change the bus driver output.

Accumulator Inputs: The input level presented to these inputs will be the same as that assumed by the buffer outputs after executing inputs strobes IOTXY , 5, or 7. Input data must be present at least 50 nsec prior to an IOP. Each input is protected from negative undershoot by a diode clamp.

Reset Register Pin AL2: A positive pulse of 50 nsec or longer at this input sets all buffer outputs to ground. When high, this input overrides any data loading from the accumulator inputs. The output register will be cleared within 70 nsec from the rising edge of this input. Diode input clamping is provided to limit negative undershoot to —0.9 volts.

Outputs:
Pin BR1: This output can drive ten TTL unit loads and has a propogation delay of less than 20 nsec. See Table 1.

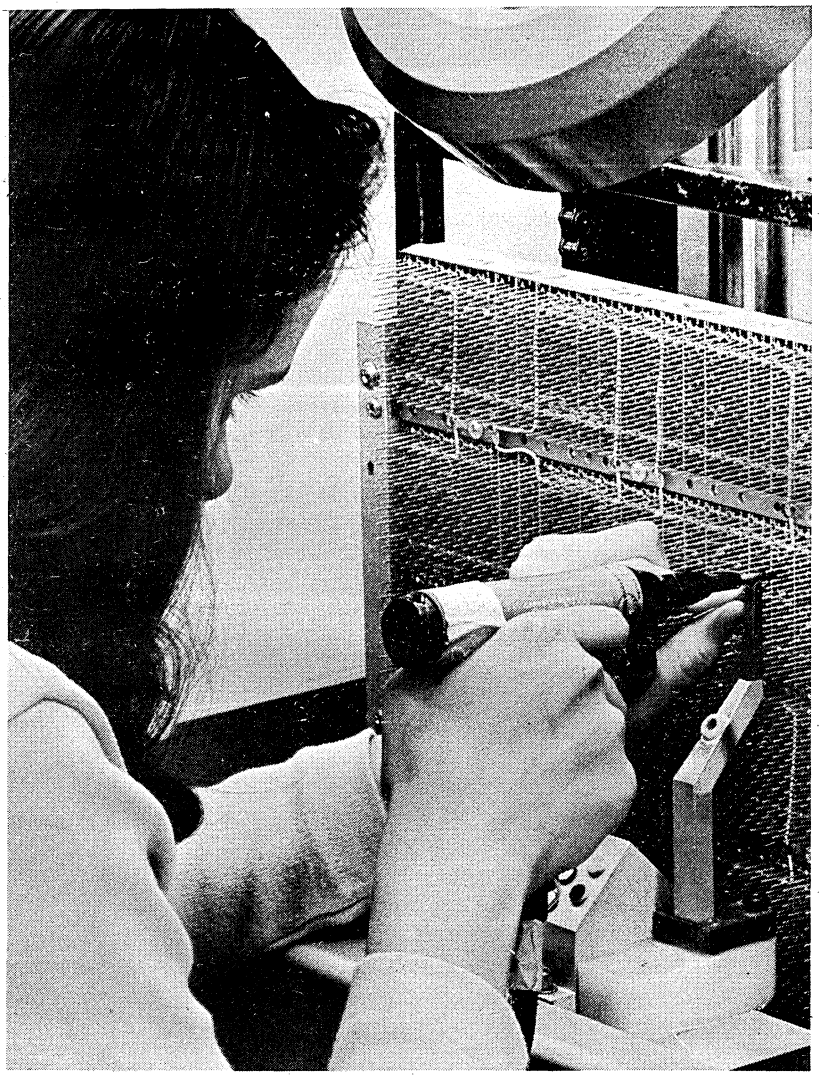
Bus Driver: These open collector npn transistor bus driver outputs, including pin BP1, can sink 30 ma. at ground. The maximum output voltage cannot exceed +20 volts and each driver output is protected from negative undershoot by a diode clamp. When this module is used with the PDP8/I or PDP8/L,

output pins BA1—BN1 would be connected to the accumulator input lines and pin BP1 to the clear accumulator line of the I/O bus. Typical rise and fall TTT of these outputs with a 30ma resistive load are 100 nsec.

Buffer Outputs: Each output can drive ten TTL unit loads.

Power: +5 volts at 385 ma. (max.)

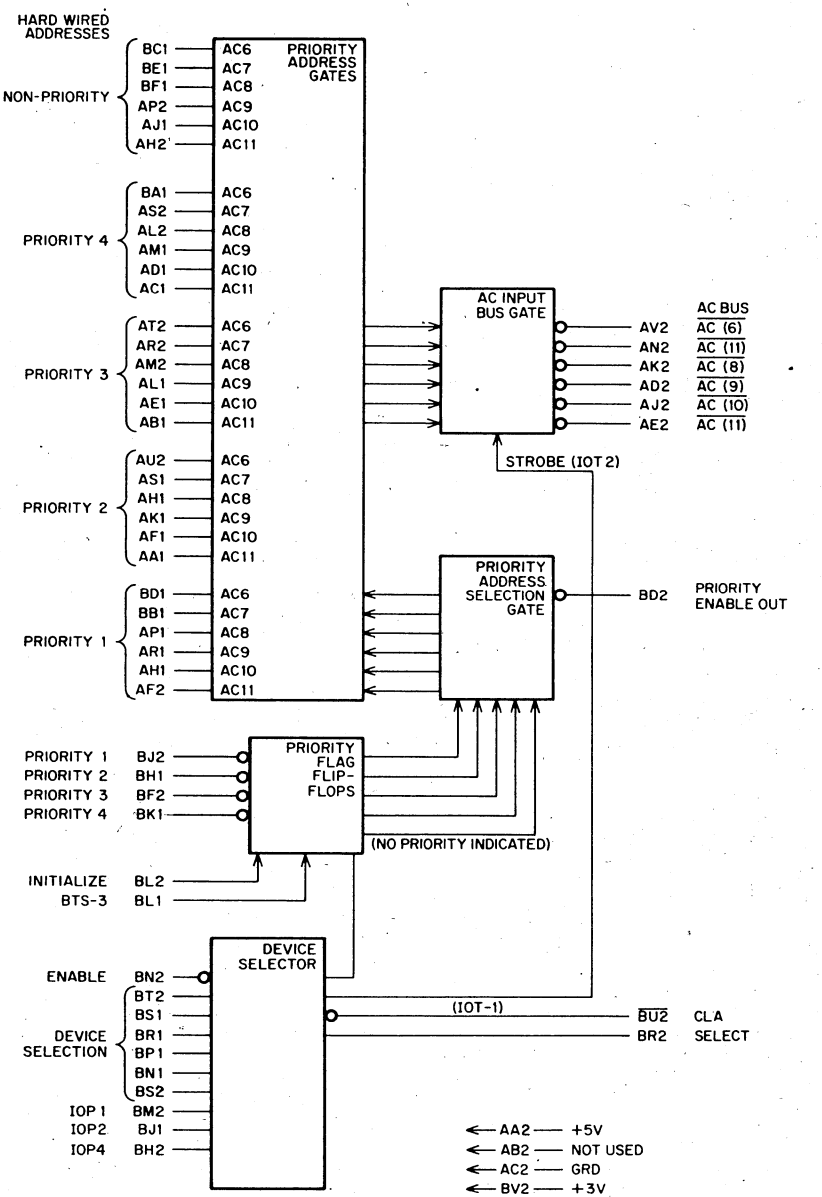
M735 — $140



The computer-controlled, semi-automatic wire wrap automatically locates the correct pin and helps position the wire wrap tool for complex back panel wiring. This operation makes it possible for DEC to wire wrap all of its systems with great speed and accuracy and pass on a substantial savings to its customers.

PRIORITY INTERRUPT MODULE
M736

M SERIES



PRIORITY INTERRUPT MODULE
M736

M SERIES

The M736 is used in conjunction with the PDP8/I or 8/L to provide the capability of assigning priorities to various I/O devices connected to the I/O bus of the computer. The M736 can be used to assign priorities for one thru four external devices. Priority assignment may be provided for more than four devices by using additional M736 modules for each additional group of four devices. All M736's in a particular priority system would utilize the same device code.

THEORY OF OPERATION

Basically the M736 module consists of the following:

1. The M103 device selector function.
2. A Bit Time State-3 (BTS-3) input.
3. Four priority input lines.
4. Priority enable line, input and output.
5. Five groups of six gates, each of which is capable of being hard wired to provide address information to locate subroutings to service the various devices associated with the priority interrupt system. The output of each of these gates is strobed onto the accumulator input bus on lines AC(6) thru AC(11).

SEQUENCE OF OPERATION

The external device activates its skip and/or interrupt FLAG flip-flop. The activation of the FLAG causes two things to happen; (a) The computer's interrupt request line is pulled to ground. This tells the computer that an external devices requires service and requests the computer to jump to an I/O priority interrupt service subroutine as soon as the computer completes its present cycle. (b) The external device FLAG pulls to ground the appropriate hard wired priority line connected to a "D" flip-flop in the M736.

A Bit Time State-3 (BTS-3) pulse from the computer is applied to the clock input of the "D" flip-flop to which the activating device flag is connected, as mentioned in section 1b above, and causes this flip-flop in the M736 to set. If more than one priority devices called to be serviced at the same time, all of the associated priority "D" flip-flops in the M736 would be set at this time. The outputs of the priority flip-flops in the M736 are connected to a priority gate structure which is arranged in such a manner that only one output line will be activated and that line will be associated with the external device with the highest priority.

This activated output of the priority gate structure is applied to one group of six two-input gates which make up the address gate. The other input of each of the six two-input gates of the address gate is hard wired to provide a discrete address which will correspond to the starting location of the particular

subroutine associated with that priority request. Each of the six output lines of the activated address gates is applied to one input of a two-input gate of the AC input strobe gate.

The computer now has had time to jump to the priority interrupt service routine and now issues a device selection code corresponding to the hard wired device selection code assigned to the M736 priority interrupt modules. This device selection code will pre-enable the IOP gates of the M736 of M736's.

The computer now issues an IOP-1 pulse to the IOP-1 gate of the M736 module. The output of the IOP-1 gate now produces an IOT-1 pulse which causes the "Clear the AC" line of the I/O bus to be pulled to ground, and thereby clears the AC.

The computer issues an IOP-2 pulse to the IOP-2 gate of the M736 module. The output of the IOP-2 gate produces an IOT-2 pulse which is applied to the strobe inputs of the AC input bus gate. As the other inputs of the AC input bus gate are connected to the outputs of the address gate, appropriate lines of the AC input bus (AC 6 thru AC 11) will be pulled to ground thereby loading into the AC the starting address of the subroutine associated with the particular priority I/O device to be serviced.

The computer now refuses to accept any further interrupt requests and jumps to the subroutine with the particular starting address which was loaded into the AC. The service routine of the particular priority device contains an instruction to clear the interrupt flag flip-flop of the particular I/O device and at the end of the subroutine issues the M736 device selector code with an IOP-4 which clears the priority flag flip-flops of the M736. The computer now turns on the priority interrupt system capability which allows the computer to service any future interrupt requests.

USING THE M736 PRIORITY INTERRUPT MODULES

1. Assign a device selection code to the M736 priority system and connect the device selection inputs of the M736 to the proper device selection lines to assure decoding for that code. If more than one M736 is used connect the device selection lines for each M736 in exactly the same manner. Each M736 will use the same device selection code.
   These inputs are: BT2, BS1, BR1, BP1, BN1 and BS2.
2. Connect the enable input, BN2, of each M736 to GRD.
3. Connect the IOP-1 input, BM2, to the IOP-1 bus line.
4. Connect the IOP-2 input, BJ1, to the IOP-2 bus line.
5. Connect the IOP-4 input, BL2, to the IOP-4 bus line.
6. Connect the BTS-3 input, BL1, to the BTS-3 bus line.
7. Connect the outputs of the external I/O device flag flip-flops to the priority

NOTE: In normal operation, IOP-4, is not required as the flag flip-flop in the external priority I/O device is cleared by the subroutine servicing that device. When the flag in the I/O device is cleared, the next BTSO3 pulse will load the disabled flag outpu tinto its respective priority flag flip-flop in the M736 effectively clearing the priority flag flip-flop. flip-flop.

inputs in such a manner as to pull the corresponding priority input line of the M736 to GRD when the device flag is activated. These inputs are as follows:

1st priority	BH1	"	"	"
2nd priority	BF2	"	"	"
3rd priority	BK1	2nd	"	"
4th priority	BJ2	"	"	"
5th priority	BH1	"	"	"
6th priority	BJ2	1st	M736	module

etc. carry on for additional priority interrupt devices.

8. Assign starting address to the subroutines which will service each priority interrupt device attached to the priority interrupt system. Also assign a starting address for the subroutine to service non-priority devices. Hard-wire the various starting address of the service routines as follows:

	AC(6)	AC(7)	AC(8)	AC(9)	AC(10)	AC(11)
Priority 1	BD1	BB1	AP1	AR1	AH1	AF2
Priority 2	AU2	AS1	AN1	AK1	AF1	AA1
Priority 3	AT2	AR2	AM2	AL2	AE1	AB1
Priority 4	BA1	AS2	AL2	AM1	AD1	AC1
NON-Priority	BC1	BE1	BF1	AP2	AJ1	AH2

NOTE: If more than four external I/O devices require priority assignments, the NON-priority address inputs BC1, BE1, BF1, AP2, AJ1 and AH2 of the M736 module used for the first four highest priorities, *must* be connected to GRD. If more than two M736 modules are required all of the NON-priority address lines of each module except the last M736 containing the lowest priorities, must be connected to GRD. The NON-Priority address is hardwired to the NON-Priority address inputs of only the lowest priority M736 module. All un-used priority address inputs must be grounded. Logic 1 level for address may be obtained from module pin BV2 of each M736 module. Lower priority addresses would be hardwired on succeeding M736 modules in the same order hard wired to the second M736 module as follows:

	AC(6)	AC(7)	AC(8)	AC(9)	AC(10)	AC(11)
Priority 5	BD1	BB1	AP1	AR1	AH1	AF2
Priority 6	AU2	AH2	AK2	AD2	AJ2	AE2

9. Connect the AC input bus gate outputs to the AC bus as follows:

	AC(6)	AC(7)	AC(8)	AC(9)	AC(10)	AC(11)
Module Pins	AV2	AH2	AK2	AD2	AJ2	AE2

10. Connect the Priority Enable input line BE2, of the M736 with the highest priorities, or the only priorities, to ground.

11. If lower priorities of 5 or more are assigned, connect the Priority output of the module with the higher priorities, Pin BD2, to the next M736 module (with the next following four lesser priorities) Priority enable input pin BE2.

12. Last, but not least, connect the INITIALIZE input, BL2 to the Initialize line of the computer I/O bus.

M736 — $130

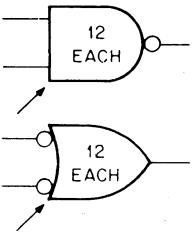
LOGIC APPLIQUES

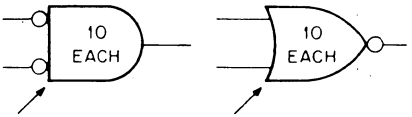
M SERIES

For convenient drawing of neat block diagrams, to supplement the DEC drawing template, self sticking matte-surface appliques lift from backing with a sharp knife.

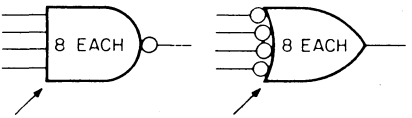
DIAGRAMS	MODULES	APPLIQUE TYPE
12 2-input NOR, 12 2-input NAND	M101, M113 K113, M141	DRT-1-47
10 2-input NAND, 10 2-input NOR	M112	DRT-1-03
8 4-input NOR, 8 4-input NAND	M117, M617, M627	DRT-1-35
10 8-input NOR, 10 8-input NAND	M119	DRT-1-51
9 4-input AND/NOR 9 4-input NOR/AND	M121, M160	DRT-1-25
3 Binary to Octal/Decimal Decoder	M161	DRT-1-20
24 JK Flip-flops	M203, M206, M207	DRT-1-23
16 JK Flip-flops with gates	M204	DRT-1-22
3 8-bit Buffer/Shift Register	M208	DRT-1-41
18 Level Converters	M502, M652	DRT-1-39
10 NOR Level Converters 10 NAND Level Converters	M506	DRT-1-52
7 NOR Pulse Amplifiers 7 AND Pulse Amplifiers	M602, M650	DRT-1-34
2 12-input AND/NOR 2 12-input NOR/AND 2 Timers, 2 clocks	M160, M302 M401	DRT-1-21

PRICE: $1.50/sheet

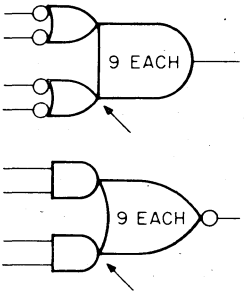




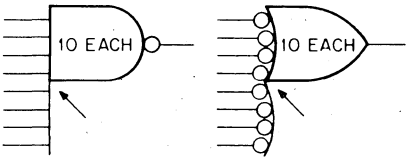
M117, M617, M627



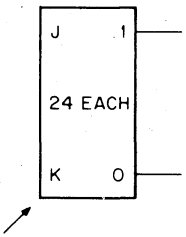
M121, M160



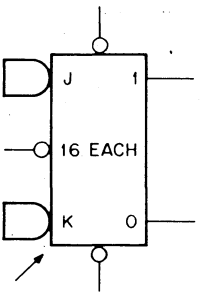
M119

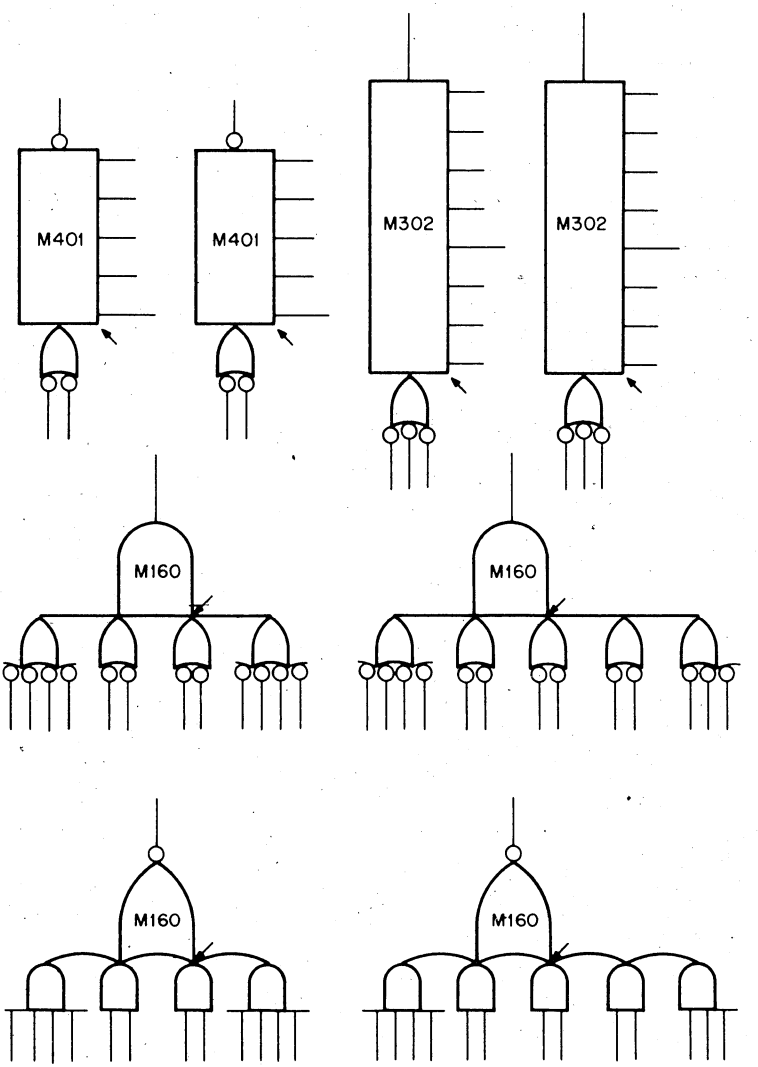


M203, M206, M207

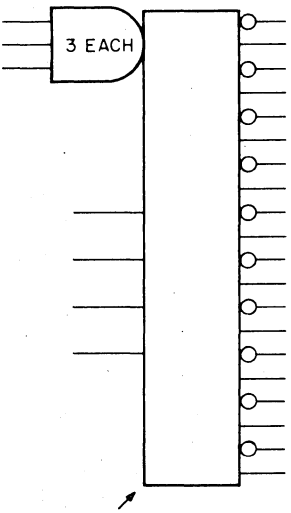


M204

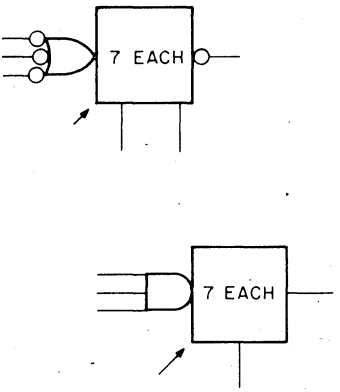



M401
M401
M302
M302
M160
M160
M160
M160

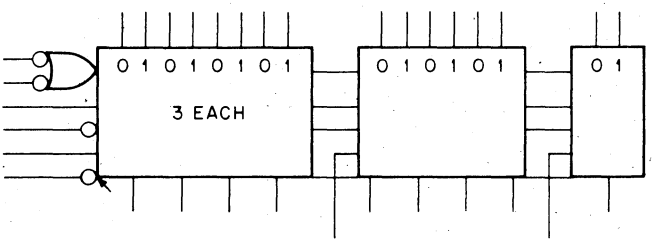
M161



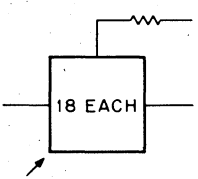
M602, M650



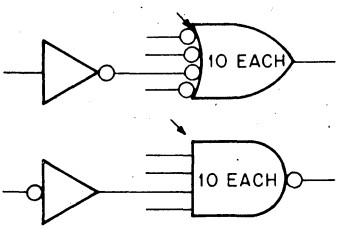
M208



M502, M652

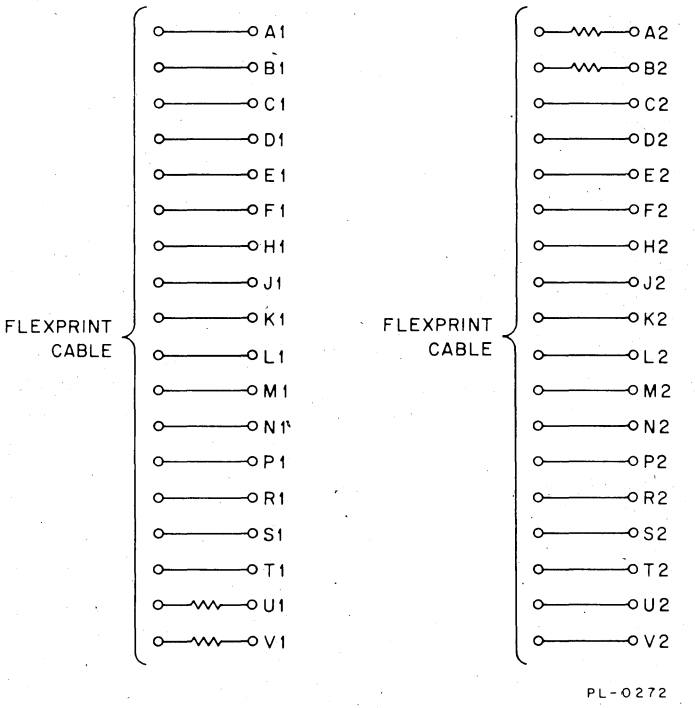


M506



FLEXPRINT CABLE CONNECTOR
M901

M SERIES



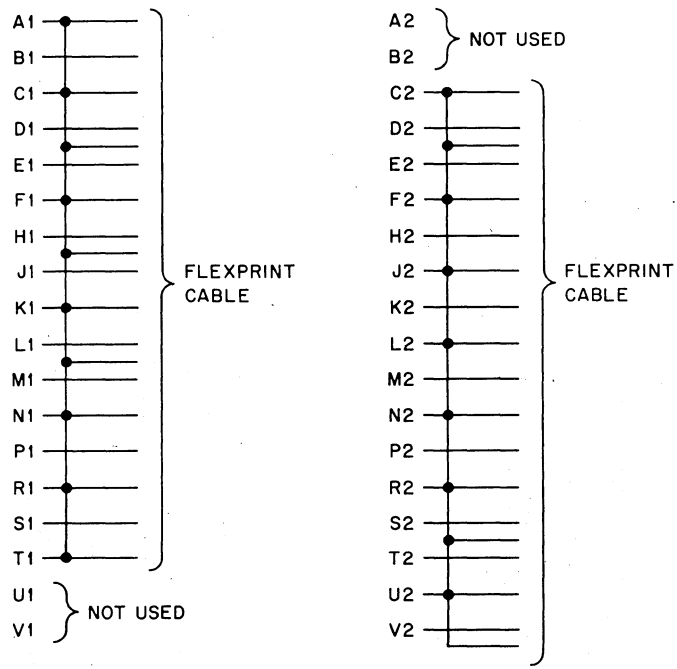
This module allows 36 lines to be used as signals and/or grounds. The 100 ohm resistors connected in series with the modules pins A2, B2, U1 and V1 are provided to afford some measure of protection in the event that these pins are inadvertently connected to a source of supply voltage.

Input: Recommended current per line is 100 ma. maximum.

M901 — $16

FLEXPRINT CONNECTOR
M903

M
SERIES



The M903 connector is a single sized, double sided board.

This connector provides high density cable connections using two single flexprint cables. Eighteen signal leads and grounds are used as listed below.

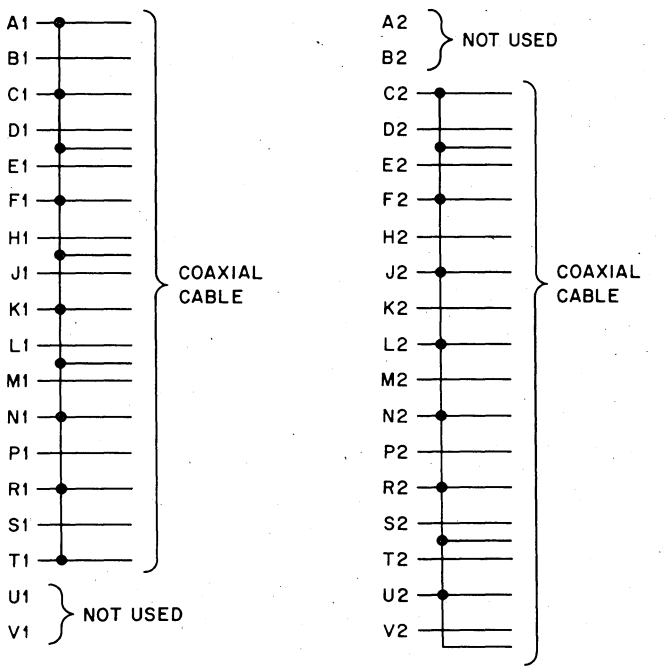
Signal: B1, D1, E1, H1, J1, L1, M1, P1, S1
D2, E2, H2, K2, M2, P2, S2, T2, V2

Common Ground: A1, C1, F1, K1, N1, R1, T1
C2, F2, J2, L2, N2, R2, U2

M903 — $12.50

COAXIAL CABLE CONNECTOR
M904

M SERIES



The M904 connector is a single sized, double sided board.

This connector provides high density cable connections using coaxial cable. Provisions are made for connection of two nine-conductor coaxial cables to this connector. Eighteen signal leads and grounds are used.

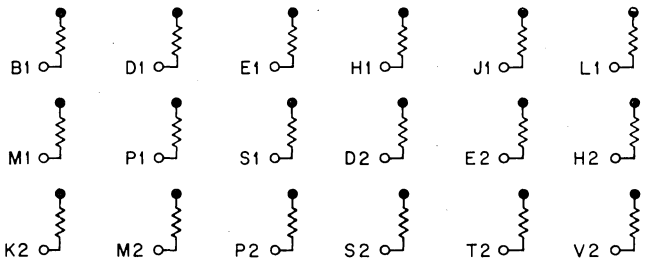
Signal: B1, D1, E1, H1, J1, L1, M1, P1, S1
D2, E2, H2, K2, M2, P2, S2, T2, V2

Common (ground): A1, C1, F1, K1, N1, R1, T1
C2, F2, J2, L2, N2, R2, U2

M904 — $14

CABLE TERMINATOR
M906

M SERIES



The M906 cable terminator module contains 18 load resistors which are clamped to prevent excursions beyond +3V and ground. It may be used in conjunction with M623 to provide cable driving ability similar to M661 using fewer module slots.

The M906 may be used to terminate inputs. In this configuration, M906 and M111 are a good combination.

Inputs:
This module is normally used standard M-Series levels of 0 and +3V to partially terminate 100 ohm cable. It presents a load of 22.5 ma or 14 TTL unit loads at ground, and therefore, must be driven from at least an M617 type circuit, or preferably a cable driver.

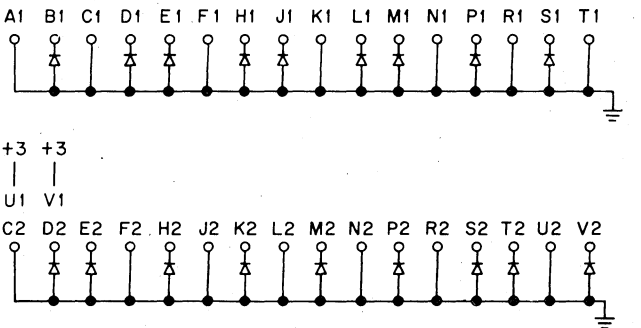
The following pins MUST be grounded: A1, C1, F1, K1, N1, R1, T1
C2, F2, J2, L2, N2, R2, U2

Power: +5V @ 440 ma. (max.) (all lines grounded).

M906 — $20

DIODE CLAMP CONNECTOR
M907

M SERIES



The M907 is used to provide proper undershoot ground clamps for PDP8/I positive bus signals not using M103 or M101 inputs.

The M907 also provides +3V for clamping 25 unused inputs. Diode clamps appear on signal leads used in double-sided alternate ground I/O cables.

Diode clamp: B1, D1, E1, H1, J1, L1, M1, P1, S1,
D2, E2, H2, K2, M2, P2, S2, T2, V2

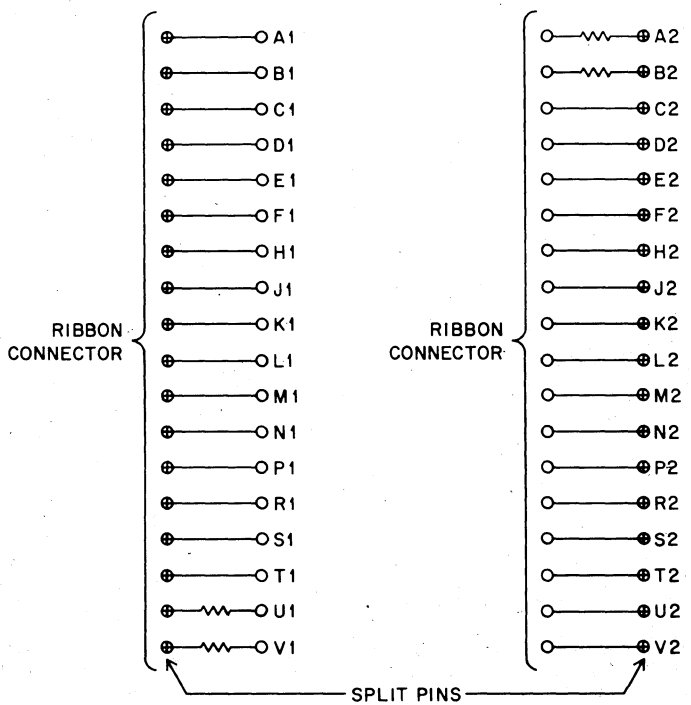
Ground: A1, C1, F1, K1, N1, R1, T1,
C2, F2, J2, L2, N2, R2, U2

Power: +5v at 10.2 ma. (max.)

M907 — $16

RIBBON CONNECTOR
M908

M
SERIES



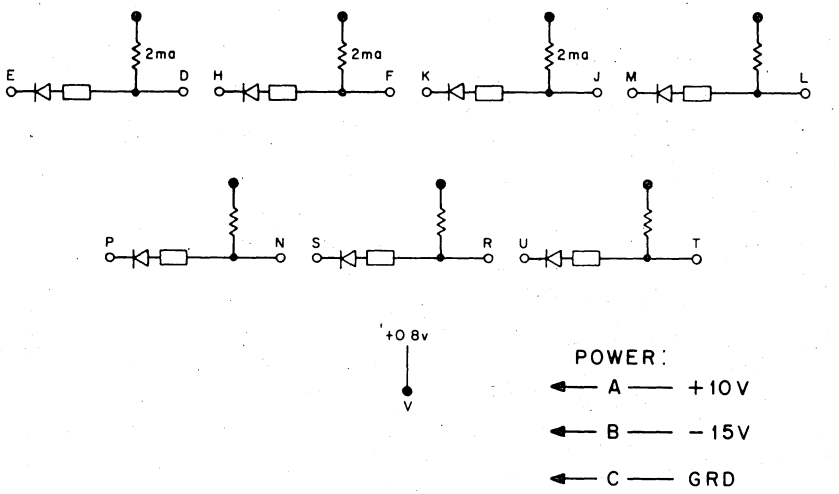
The M908 cable connector consists of a single sized, double sided board which contains thirty-six split pins which allows the connection of thirty-six separate wires. All connections are made on the component side of the module. The 10 ohm, 1/4 watt resistors connected in series with module pins A2, B2, U1 and V1 are provided to afford some measure of protection in the event that these pins are inadvertently connected to a source of supply voltage.

The M908 is primarily intended for use with ribbon cable and is normally supplied with a ribbon cable clamp unless otherwise specified.

M908 — $18

POSITIVE LEVEL CONVERTER
W512

W SERIES



INPUT	OUTPUT
+	−3V
GRD	GRD

W512 POSITIVE LEVEL CONVERTER

Positive logic systems, such as those using monolithic integrated circuits, can use the W512 to make available standard DEC levels of −3V and ground to accessory modules in the W and A series.

Input threshold voltage to each converter is normally 1.6 volts for compatibility with DTL and TTL levels. This threshold can be set at 0.8 volts by grounding pin V for RTL level conversion.

Inputs: Input current 1 ma or less for input voltages between 0.3 volts and the threshold. 100 μa for inputs above the threshold. Input voltages must not exceed 6.0 volts with pin V open, or 5.3 volts with pin V grounded. Inputs must exceed nominal thresholds by at least 0.4 volts for full switching with minimum noise rejection.

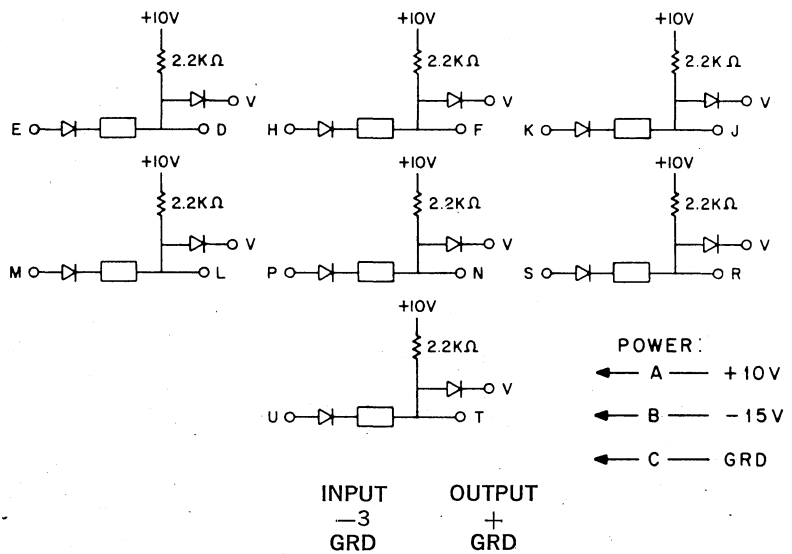
Outputs: Each output can supply up to 8 ma at ground. Grounded inputs provide grounded outputs and positive inputs provide negative outputs. Output rise and fall TTT are less than respectively 70 and 200 nsec.

Power: 10v (A)/104 ma: 15 v (B)/30 ma.

W512 — $25

POSITIVE LEVEL AMPLIFIER
W603

W SERIES



W603 POSITIVE LEVEL AMPLIFIER

Positive logic systems such as those using RTL, DTL, or TTL monolithic integrated circuits can be driven from FLIP CHIP systems through the W603. Clamped load resistors at the output of each circuit permit output levels to be adjusted to the type of circuit being driven. This clamp voltage is common to all seven converters on the module.

Inputs: 1 ma at ground.

Outputs: Each output can supply up to 5 ma at ground. Drive capability at the positive output voltage is provided by internal 2200-ohm resistors returned to +10 volts. The upper positive level will be no more than 0.8 volts above the clamp voltage.

Grounded inputs provide grounded outputs; negative inputs produce positive outputs. Output rise and fall TTT are less than respectively 100 and 150 nsec.

Power: +10(A)/35 ma. — 15(B)/7 ma.

When the W603 is used to drive M or K series modules, the module pins V and A may be tied to the +5 volt logic power supply. The following drive capability will result:

Each output will supply one M series unit load, or two K series unit loads.

W603 — $23

K SERIES

INTRODUCTION

Control system complexity and demands on reliability are rising with ever-increasing automation. More and more, control system designers are looking to solid state electronics for new answers to the old problems of reliability, complexity, and economy. Some of the answers are provided by solid-state digital logic designed for the industrial environment, and solid state analog-digital conversion to link analog sensors and actuators to digital control.

Why Solid State?

The time-honored way to do control logic is with the deceptively simple-looking relay. The metal-to-metal contact area sees physical and chemical actions of remarkable complexity. Even the mechanical-magnetic interactions are involved enough to cause problems now and then. Still, relays sometimes respond beautifully to simple maintenance. If the contacts stick, force them apart; if they are dirty, clean them.

Railway signaling relays, operating perhaps a hundred times a day, accumulate 25 years and a million operations without failure. And modern sealed-contact relays can do 10 billion operations under the right conditions without wearing out. So why abandon well-proven, reliable components? Only because it is necessary. And it is necessary in a growing number of applications.

Reliability

As profit margins grow tighter, and maximum process efficiency becomes a necessity rather than an ideal, control system reliability assumes greater importance. Faulty operation and machine downtime can swiftly and disastrously cut into the profit picture. With a highly complex control system, check-out can easily become a very costly and time consuming operation. Many factors affect the reliability of a control system. A major consideration is the speed at which the logic control elements must operate. At 1KHz, near the maximum rate for dry reed relays, 100 million operations accumulate in about 30 hours. Longer-lived mercury-wetted contacts operating 100 times per second, accumulate 10 billion operations in about four years. Even if a four year component life is enough, there are applications where 100 operations per second are not. Solid state logic, with nothing to wear out, stick, or corrode, can operate almost indefinitely at 100,000 operations per second.

Complexity is another factor. Demands for more automation, more efficiency, more safety, more accuracy all result in increased control system complexity. As a result, the sheer numbers of logical decisions demand component reliability far greater than that acceptable in a small system. Solid state logic provides the degree of reliability needed in a large system, at reasonable cost.

Size

Even the tiniest-contact reed relay coil is enormous alongside a transistor, or a complete integrated circuit. And most small control systems are not built with reed relays: to get the advantage of ruggedness or standardization, usually all the relays used are built to 300 volt or even 600 volt specifications whether they drive external loads or just relay coils. But a single small printed circuit board can easily accommodate a half dozen or more relay equivalents in logic capability, in a small fraction of the space of one 300 volt relay.

Computer Tie-In

There are several levels of computer involvement possible, extending from incorporation of a computer as a part of an individual control system to the use of a central computer to monitor the performance of many independent control systems. Regardless of the level at which the computer interacts, its presence demands an interface between solid-state circuitry and the controlled machine or process. If such an interface is forced into existence by the present or projected future use of a computer, why not put solid state control logic behind it and gain the benefits of solid state speed, compactness, and reliability through the entire system?

Also solid-state logic can communicate with existing analog sensors and actuators through solid-state analog-to-digital (A/D) and digital-to-analog (D/A) converters.

All of these factors tend to make solid state control systems increasingly attractive, particularly as their costs come down.

Who Should Be Designing For Solid State Controls?

Broadly speaking, the decision between conventional relay controls and the new solid state controls, like most engineering decisions, hinges on comparative overall costs. Where three or four or a half dozen relays can do the whole job, the cost of a solid-state interface will seldom be justified unless high speeds are required. Very large or computer-oriented systems leave little justification for the use of relays.

For intermediate systems, the comparison is more complicated. The tabulation below can serve as a framework for a systematic review of factors you should consider before you specify your next control system.

Considerations	Factors Suggesting Relays	Factors Suggesting Solid State
Reliability	Control system failure causes no panic. Temporary manual control acceptable. Simple system, easy to trouble shoot.	Downtime cuts quickly into process profitability. Quick check-out of entire system in case of trouble desirable, instead of on-the-spot checking. Lives and property might be endangered by failure.
Cost	Low cost relays acceptable. Maintenance costs need not be considered. Personnel training costs important. System failures will not cause significant secondary costs.	High quality relays used for comparison. Costs of failure high. Installation space costly. Cost of future modifications must be considered. Maintenance costs over life could be important.
Complexity	Small systems, perhaps a half dozen relays or fewer.	Complicated systems, which would require fifteen or more relays to implement.
Sophistication	Traditional performance still acceptable.	New levels of performance are needed, calling for increased control system complexity to remain competitive.

Considerations	Factors Suggesting Relays	Factors Suggesting Solid State
Familiarity	Controls that must be serviced by electricians who can not be retrained.	Environments already include other solid-state components or they will soon be added. Also, multi-system installations where a few controls technicians will cover a lot of equipment.
Growth	No foreseeable use of computers. Little likelihood of important modifications.	Added performance or safety features may be wanted later without tearing the system down. Computer tie-in might become desirable or is planned already.
Size	Plenty of space available.	Relay equipment might require separate balconies, restrict maintenance of machinery, or block aisles. Features added later must fit original enclosure.
Speed	Control system delays of tens of milliseconds acceptable. Operating rate is low, relay wearout no problem.	Compatibility with pulse tachometers, photoelectric pickups, electronic instruments required. Closed-loop stability demands quick response. High repetition rate that would cause wearout of moving parts.

Why Digital?

Relays, solenoids, switches, fuses, locks, counters, annunciators, panel lights and panic buttons all have one thing in common: they are digital. All these devices (when working properly) are up, down, on, off, in, out; but never in-between. Strictly speaking, of course, you cannot get from on to off without passing through in-between. But digital devices pass through in-between at maximum speed, and without waiting around for doubt to creep in.

Non-digital devices like panel meters, potentiometers, and slide rules work in the "in-between" area, producing outputs that are proportional to the input. The angular position of a panel meter pointer is the analog of the magnitude of the electrical input. A potentiometer's voltage output is the analog of mechanical shaft position. In a slide rule, position is the analog of magnitude.

In a slide rule, accuracy is limited by the thickness of the calibrating marks and the difficulty of estimating values between them. Each space is an area of uncertainty. The same kind of uncertainty exists in every proportional electrical system, in the form of noise. In all but the most expensive analog equipment, the amount of noise, like slide rule error, limits accuracy to two or three significant figures.

Noise taken in this broad sense affects every proportional device. Noise is a major reason for the dominance of digital computers over analog computers where complex calculations are required. Small amounts of noise contributed by each analog input or computing element add up to degrade the accuracy of the answer. In digital circuits, the noise can be disregarded as long as it is below an "off" or "on" threshold level.

Analog controllers and servo systems, chart recorders, panel meters, and small analog computers are often simpler and cheaper than their digital equivalents, and should be used wherever they can do the job. But since so many commonly used control devices (from relays to panic buttons) are digital anyway, all-digital control is convenient. For complex control situations, digital methods can deliver accuracy and perform types of control beyond the ability of an analog system at any cost. And using solid state digital control, analog and digital devices can work together through A/D and D/A conversion. Better still, noise-free direct digital sensors and actuators can be used in the design of new process equipment.

Noise Immune Control Modules

Because of their high sensitivity and speed, solid state components can respond to noise that relays would safely ignore. To use solid state logic with freedom from noise problems in the neighborhood of arcing contacts, brushes, welders, etc. requires special design considerations.

Unlike analog devices, digital circuits have a noise "threshold" above which a noise or signal must rise to cause any change in the output of the circuit. It is this threshold that accounts for the superiority of digital circuits in processing information through complex manipulations without loss of accuracy. In the design of sold state logic for industrial use, this basic threshold feature of digital circuits can be exploited. By adding external capacitance, the speed, and thus the sensitivity, of the circuit can be lowered.

Noise

Suppose that on the basis of the above, you find you should be using solid-state digital logic. But will the system "drop bits," or otherwise go haywire in your environment? How well can noise trouble be anticipated, and what measures should be taken? How can you compare the noise immunity of competing manufacturers' circuits? These questions need some kind of answer before you can feel confidence in taking the step.

A logical starting point is the noise itself. What is its amplitude? Its frequency distribution? How does it vary with time? With temperature? How many picofarads of coupling capacitance between the noise sources and the logic wiring? How many nanohenries of shared inductance in the logic and noise ground return paths?

Right away you suspect these questions are going to be difficult to answer. You may be able to say that typical noise source voltages are "measured in

kilovolts" and are "strongest in the Megahertz frequencies." But going beyond such hazy estimates will require detailed knowledge of the physical conditions that interact to produce electrical noise. You'll need to know the materials used in all metal-to-metal contacts, and the condition of the contact surfaces. You'll need the inductance and capacitance of the wires connecting them. And the inductance and capacitance of the loads they drive. And the gases in the atmosphere surrounding the contacts. Even the exact routing of the wires will have to be examined.

Is solid-state out of the question after all, because analysing the noise environment is impractical? No, solid-state is not impractical: provided you use circuits designed specifically for noisy environments, where the focus is on qualitative rather than quantitative factors.

Engineering For the Unknown

Engineers prefer to deal in quantities: "how big," "how many," and "how much." Success in dealing with noise requires a different approach because very few if any accurate numbers about noise will be forthcoming. Qualitative considerations, those that affect the overall character of circuit behavior rather than specific numerical details, are central to this approach.

We can group the qualitative tools available for dealing with electrical noise into two groups: those that keep noise out of the solid-state logic, and those that minimize the influence of noise that gets in. Keeping noise out is cheaper than electrically rejecting it, since primarily mechanical and packaging considerations rather than electronic aspects are involved. Here are some of the ways you can keep noise out:

1. Segregate logic wiring from field wiring. Don't design input converters and output drivers so field wiring goes through the same connectors used to carry logic signals. Arrange to use opposite ends of printed boards for logic and field wiring connections, and never allow the two kinds of wiring to lie side-by-side or be bundled together.

2. Don't mix logic ground with field ground. This doesn't mean logic ground should float; on the contrary. But heavy currents should not pass through the logic ground system on their way back to a power supply. An excellent scheme is to switch the AC line with isolated triacs. DC solenoid drivers might seem difficult to isolate, but judicious use of ground isolating resistors and auxiliary chassis tiepoints can force most of the load current outside of the logic ground system.

3. Use high-density packaging. Computer type modular construction minimizes lead lengths in the logic, minimizing the capacitive coupling between logic wiring and nearby field wiring. Dense packing also cuts resistance and inductance in the logic grounding system, minimizing interference from any residual noise currents that may flow there.

4. Where logic and power circuits must be adjacent, use shielding. For example, a group of printed boards carrying field circuits can be shielded from general purpose logic modules simply by inserting un-etched copper clad boards in the sockets that separate the two groups. (Logic power must skip these sockets to avoid shorting the supply.) A single ground connection to the shield board is perfectly adequate, since the noise currents it carries will be limited by the small capacitance involved.

5. Filter the line voltage where it enters the logic power supply, or at supply output terminals. Supplies for panel lamps should also be filtered, if their wiring approaches logic wiring. Do not use logic power for any other function or carry supply output wires into the field for any reason.

The above five measures may suffice to allow even fast, computer-speed logic to be used in the vicinity of severe noise. Often, however, some forgotten loophole in the noise exclusion plan will spoil the dependability of an otherwise noise-tight system. All it takes is one such leak to cause real headaches if the logic itself is sensitive to noise. A good belt-and-braces approach will include not only these noise isolation qualities, but several noise desensitizing qualities as well:

1. Slow speed of response. Noise is usually most intense at high frequencies (in the Megahertz). Metal-to-metal contacts are nearly ideal step generators, and wiring resonances often dictate high-frequency noise peaks. A circuit that can't be switched for five microseconds is deaf to all but the biggest and slowest of noises, and usually will be entirely undisturbed. But be careful to use discrete capacitors, not sluggish semiconductors to obtain circuit slowdown. Semiconductor manufacturers "improve" their products regularly, often by increasing their speed.

2. Good current threshold and voltage thresholds. By "good" is meant "measured in milliamperes and volts." The bigger the better, but guard against falling in love with numbers. A factor of two in voltage threshold means little if you can't predict noise amplitudes to the nearest order of magnitude.

3. Risetime independence. Circuits that don't care what risetime you feed them give you an important insurance policy. If all else fails, you can hang a capacitor to ground at any troublesome point, without worrying about the effect this has on risetime. Even more than the other qualities, risetime independence is a prime example of engineering for the unknown.

4. Special care in timer and flip-flop design. These are the circuits that stretch a noise spike to damaging length. A system that has noise-immune, risetime-independent flip-flops and timers will for most purposes be as noise immune with ultra-fast gates as with slow gates.

Looking Ahead

Many of the factors listed above cost nothing more than forethought. All are applicable regardless of choices between discrete components, integrated circuits, or a combination. As the qualitative approach to noise avoidance is more widely understood and applied, solid-state logic will become more accepted, more universal. Fears will disappear. Should your next control system be solid-state?

K SERIES
CONTROL MODULES

Computer-oriented logic, by its very nature, is high speed (1 MHz and above), and provides noise immunity far below that required in a process control environment. The upper frequency range of the K-Series modules is 100 KHz, with provision for reduction to 5 KHz for maximum noise immunity. These modules incorporate all silicon diodes, transistors, and integrated circuits, deliberately slowed.

Either English (non-inverting) logic or NAND/NOR logic is compatible with K Series. The hardware for this series is specifically designed for standard NEMA enclosures. FLIP CHIP™ mounting hardware can likewise be used for rack-mounting, inasmuch as K-Series modules fit standard DEC sockets.

Proven FLIP CHIP™ connectors, used for years in applications from steel mills to lathe controls, provide modularity. Even the connection between terminal strips and electronics can be plugged for installing the logic after field wiring is complete, and removing it quickly for modifications or additions.

Checkout and trouble shooting is easy with K-Series logic. Every system input and output has an indicator light at its screw terminal. A special test probe provides its own local illumination and built-in indication of transients, as well as steady states. Every point in the system is a test point, and consistent pin assignments reduce the need to consult prints.

Construction materials and methods are the same as for other high-production FLIP CHIP™ modules, including a computer-controlled operating test of each complete module. K-Series modules further offer the size reduction, reliability, flexibility, and low cost of solid state logic, with an added bonus of easy interconnection. FLIP CHIP™ industrial modules are ideal for interfacing high speed M-series or computer-systems to machinery and processes. Sensing and output circuits operate at 120 vac for full electromechanical capability. Inputs from contact devices see a moderate reactive load to assure normal contact life. Solid state ac switches are fully protected against false triggering. Voltages from the external environment are excluded from the wire-wrap connections within the logic.

K SERIES SPECIFICATIONS

SUMMARY

Frequency range: DC to 100 KHz. Control points on each module allow reduction to 5 KHz for maximum noise immunity for critical functions.

Signal levels: Ov and +5v, regardless of fanout used.

Fan-out: 15 ma available from all outputs; typical inputs 1-3 ma.

Waveforms: Trapezoidal. No fast transients to cause cross talk. External capacitive loading affects speed only; no risetime dependence.

Temperature range: −20°C to +65°C, using all-silicon diodes, transistors, and monolithic integrated circuits (0° to 150°F). Limited to 0°C on four module types.

Noise immunity: False "1":20 ma at 1.6v for 1.5 μsec typical. False "0":3 ma at 3v for 1.5 μsec typical. Time thresholds can be increased by a factor of 20 for critical points by wiring the slowdown control pins.

Simple power requirements: Single voltage supply, +5v ±10%. Dissipation typically 120 mw per counting or shifting flip-flop, 30 mw per control flip-flop, 25 mw per two-stage diode gate.

Control system voltage: 120 VAC, 50 or 60 hertz.

Mounting provisions: Standard NEMA industrial enclosures. May also be used in 19" electronics cabinets.

GENERAL SPECIFICATIONS

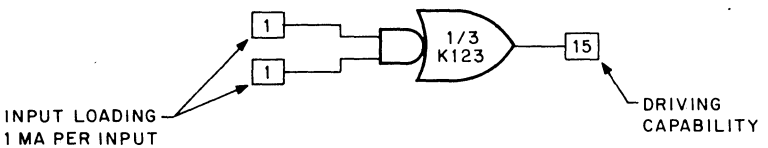
Construction Features
K-Series modules include the quality features of older lines of FLIP CHIP modules: flame-resistant epoxy-glass laminates, all-silicon semiconductors, gold plated fingers and solid gold connector contacts. Thorough testing of each module is by computer operated automatic tester for most modules, or by specialized equipment for those which are not amenable to automatic test. A test specification sheet or data sheet is packaged with each module, including a circuit schematic for that type. Monolithic or hybrid integrated circuits are included wherever they can improve the performance-cost ratio. Versatile mounting hardware imposes as few physical constraints as practicable.

Logic Signals
There are no ultra-fast transients at any K Series output. Logic signal "1" and "0" levels are essentially independent of fanout. Rise and fall transitions have controlled slopes which are not strongly influenced by normal changes in fanout, lead length, temperature, or repetition rate. The fastest K Series trapezoidal logic signal can be fully analyzed with a 500KC oscilloscope. Logic "1" or "true" is +5 volts and logic "0" or "false" is zero volts except where redefined by logic designs. Counters and shift registers advance on the "1" to "0" transition and are cleared by a "0" level. Any unused input may be left open relative to noise considerations.

M Series Compatibility
M Series outputs can drive K Series logic gates and output converters K604 and K644 directly, and any K Series input after passing through a K Series gate, provided they meet timing requirements. See Applications Notes.

Fanout and Fanin
K Series fanout capabilities are sufficient to relegate fanout calculations to the final checking phases of logic design. Logic outputs from any module type can drive up to 15 milliamperes. Logic gate inputs consume 1 milliampere

per input. Other loadings range from 1 to 4 milliamperes as indicated by the loading numbers enclosed in squares on each specification diagram.



FANIN AND FANOUT

Expandable gates give K Series a fanin capability well beyond typical logic requirements. The most restrictive fanin limitation in K Series logic concerns the wired AND configuration, for which several logic outputs are simply wired in common: the wired AND fanout capability is reduced to three milliamperes when the maximum of 5 outputs are tied together. The second level of logic (the OR node) within K113 and K123 gates is limited to less than 10 OR inputs to preserve output falltime control. The input AND gates of K113 or K123 modules may be extended with K003 expanders up to a maximum of 100 inputs, well beyond any practical requirement.

Operating Temperature
K-Series modules are designed for operation in free-air ambient temperatures between −20°C and +65°C (0°F to 150°F) except the following types which are restricted to 0°C (32°F) minimum: K202, K220, K230.

Speed
Many applications for K Series modules involve operation at rates lower than relay speeds. Even at speeds many times faster than relay capabilities, timing need not be considered unless the logic includes a "loop". A flip-flop constructed of logic gates is such a loop, in which the output at a given point feeds back to influence itself, thus demanding input durations longer than total loop delay. Proper operation of such loops should be verified by calculation using the specifications below. For a complex loop an experiment should be made if possible to look for flaws in the calculations.

When anticipated repetition rates will be of the same order of magnitude as rated logic frequency, more care is required in timing design. K Series circuits are intentionally slowed to the maximum extent practicable for 100 KHz operation, and the resulting propagation delays can limit complex logic systems to 50 KHz or even 30 KHz repetition rates. In addition, timing loops must be examined just as carefully in fast logic as in slow. If K Series speed appears marginal or insufficient for the job at hand, use M Series high speed logic modules.

Timing Characteristics for K113, K123, K202, K210, K220, K230	Time (μsec)		
	Min.	Typ.	Max.
Logic Gate Propagation Delay, Output Rise (0V to +5V)	0.5	2.0	3.0
Output D only, when connected to pin B	7.5	40	180
Logic Gate Propagation Delay, Output Fall (+5V to 0V)	0.3	1.0	6.0
Output D only, when connected to pin B	4.5	20	180
Count/Shift Input Propagation Delay, Output Rise	2.0	5.0	9.0
As above, but pin B grounded to pin C	10	30	100
Count/Shift Input Propagation Delay, Output Fall	1.0	4.0	9.0
As above, but pin B grounded to Pin C	10	30	100
Rise time, all unslowed outputs	2.0	5.0	9.0
Pin D outputs only, when connected to pin B	30	100	240
Fall time, all unslowed outputs	0.5	1.0	4.0
Pin D outputs only, when connected to pin B	7.5	20	120
Minimum time between successive input transitions on any module which has one or more Count/Shift inputs	4		
As above, put pin B grounded to pin C	10		

Exceptions:
Input transitions at pins J and K may follow other input transitions with delays down to zero; For characteristics not listed above, see timing information on individual data pages.

NOTE: Count Shift inputs are included in types K202, K210, K220 and K230

Noise Immunity

Two properties of electrical interference often overlooked in evaluating logic noise immunity are its source impedance and its frequency distribution. Unless the digital logic is spread over several feet or yards so that high potentials can be induced in the ground system, most noise will be injected via very small stray capacitances and hence will have a high source impedance. The voltages at the noise source itself are usually measured in thousands of volts. Consequently, voltage thresholds alone cannot provide adequate noise rejection. The noise appears to come from a current source, so that logic circuit current thresholds are also an important measure of noise immunity.

Capacitance-coupled interference is strongest at the highest frequencies. Logic circuits which respond slowly can reject high frequency interference peaks that exceed dc current and voltage thresholds. K Series modules get their outstanding noise immunity from a balanced combination of current voltage, and time thresholds.

Important as good noise thresholds are, practical noise environments are only vaguely predictable, so that the following design features are probably still more important:

1. All field wiring is isolated from K Series logic wiring pins.

2. Logic power is not transmitted outside the logic environment for contact sensing, etc.

3. W994 electrostatic shields may be plugged in to further isolate pilot circuit noise: see Construction Recommendations (Applications Note)

4. Plug-in module compactness keeps logic wiring short, to reduce noise injection capacitance, and confines the ground mesh for reduced ground noise.

5. Every third logic gate has optional slowdown control, ample for slowdown of all control flip-flops.

6. If all else fails, lack of risetime dependence permits any K Series output to be loaded with 0.01 mfd to ground to further reduce impedance and speed of response. Each K003 diode expander has such a capacitor available at pin B.

K Series Typical Noise Thresholds

To be falsely interpreted as a high level, a low (zero volts) K Series logic level would have to be raised 1.6 volts and held there for 1.5 microseconds; to do this would require 20 milliamperes to be supplied somehow from the noise source to the K Series output in question for this period of time. To be falsely interpreted as a low level, a high (+5V) K Series logic level would have to be reduced 3 volts and held there for 1.5 microseconds; to do this would require 3 milliamperes to be supplied somehow from the noise source to the K Series output in question for this period of time.

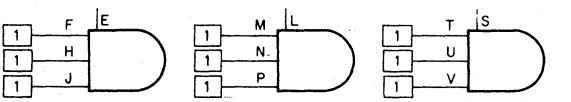
Power Requirements

A simple 5 volt supply operates any K Series system. Tolerance at room temperature: ±10%. K Series regulators K731 and K732 have a built-in temperature coefficient of approximately minus 1% for 3°C(5°F) to obtain full logic fanout over a wide temperature range and to minimize the temperature coefficient of K303 timers. Both regulators run from a nominal 12.6 volt center-tapped transformer secondary, with hash removed. See Construction Recommendations for information about alternate sources of logic power. Logic power is not used for contact sensing; 120 VAC is specified to provide full compatibility with silver contacts and noisy environments.

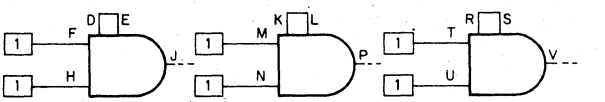
GATE EXPANDERS
K003, K012, K026, K028

K SERIES

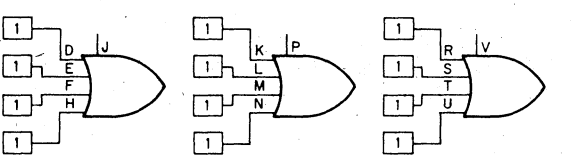
K003
AS EXPANDERS FOR
INPUT AND GATES OF
K113 OR K123 OR K134



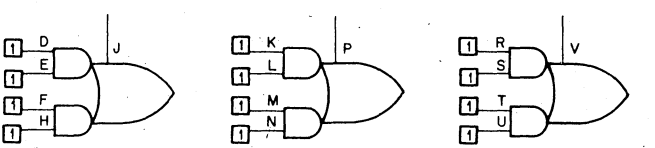
K003
AS INDEPENDENT GATES
FOR AND/OR EXPANSION
OF K113 OR K123



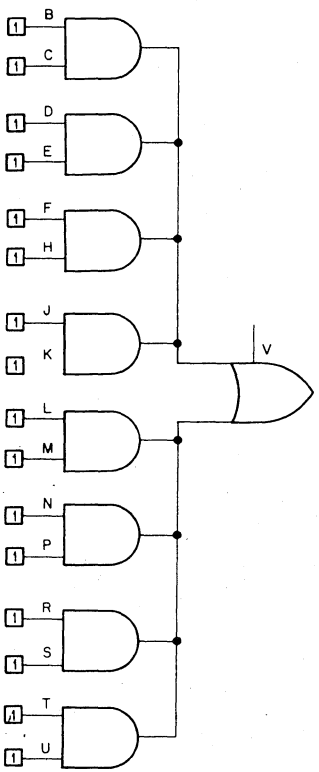
K012
AS EXPANDERS FOR
OR GATING IN K113
OR K123



K026 AS INDEPENDENT
GATES FOR AND/OR
EXPANSION OF
K113 OR K123



K028 AS EXPANDER
FOR K113 OR K123

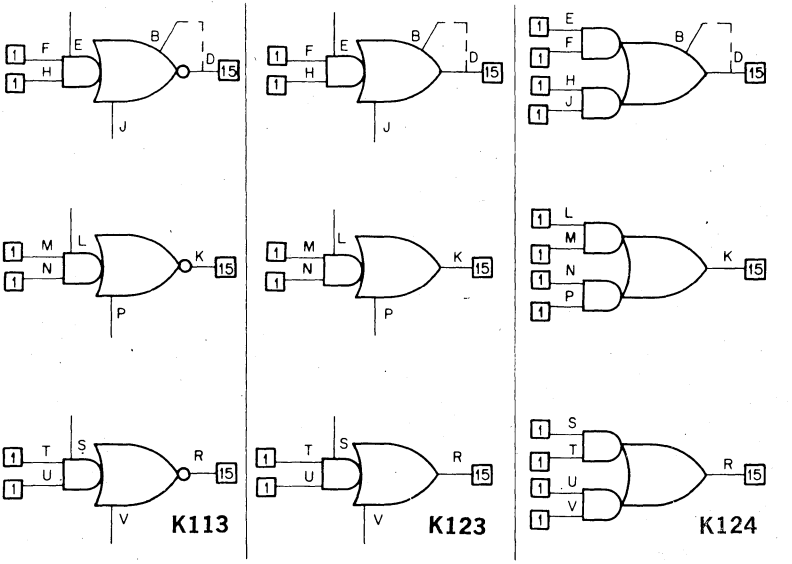


These inexpensive gate expanders offer great logic flexibility and versatility without a proliferation of module types. Logic functions performed by expanders are illustrated in combination with the K113 and K123 gates in several pages that follow the data sheet for the gates themselves.

K003 — $4
K012 — $7
K026 — $6
K028 — $7

LOGIC GATES
K113, K123, K124

K SERIES



Together with the K003, K012, K026 or K028 expanders, these gates perform any desired logic function, including AND, OR, AND/OR, NAND, NOR, exclusive OR, and wired AND.

Logic gate type K123 is an AND/OR non-inverting gate subject to expansion at either the AND or the OR node. Logic symbols and equivalent schematics are compared in the following illustrations. Typical pin connections are shown.

The AND input can be expanded up to 100 inputs total. The OR input can be expanded by any of the expanders, up to 9 inputs total. More OR inputs can be added if faster fall times are acceptable.

Expansion of the K113 inverting gate is identical. The equivalent circuit is the same except for inversion in the output amplifier.

The K124 provides a convenient way to implement non-inverting gate control flip-flops, exclusive ORs, and two term OR logic equations without the need for expanders. The module is electrically the same as a K123 gate with a K003 expander.

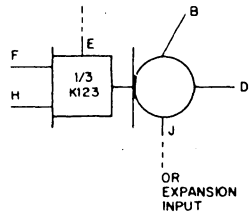
All three gate types include a slowdown capacitor that can be connected to the output of one circuit to increase its noise rejection when gates are interconnected to make control flip-flops. Use of this capacitor increases rise and fall time by approximately a factor of 20.

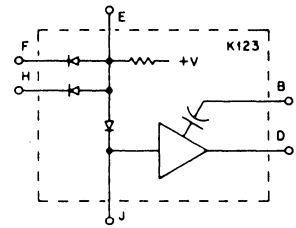
K113	$11
K123	$12
K124	$14

LOGIC SYMBOL

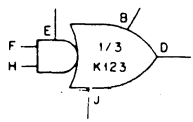
SIMPLIFIED SCHEMATIC

NEMA



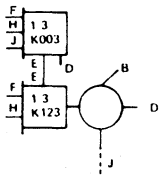


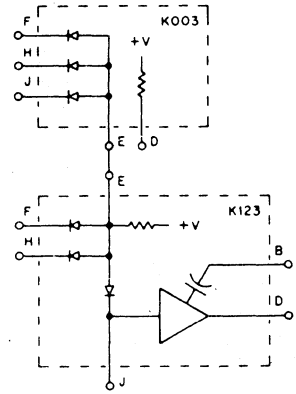
MIL



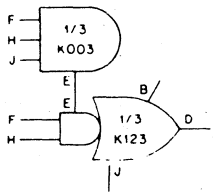
BASIC GATE

NEMA



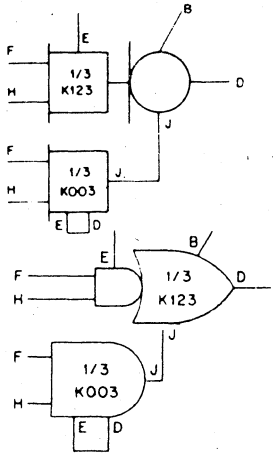


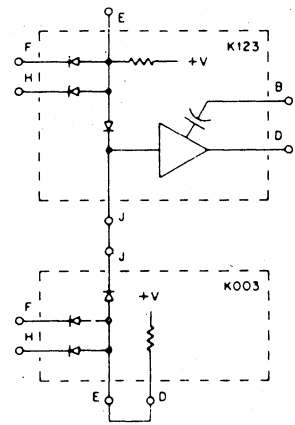
MIL



K003 AND EXPANSION

NEMA





MIL

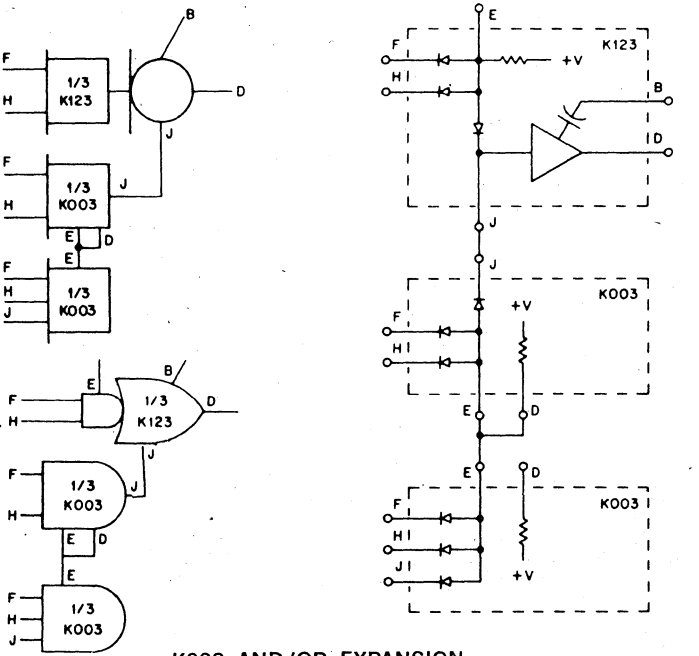
K003 OR EXPANSION

LOGIC SYMBOL

SIMPLIFIED SCHEMATIC

NEMA

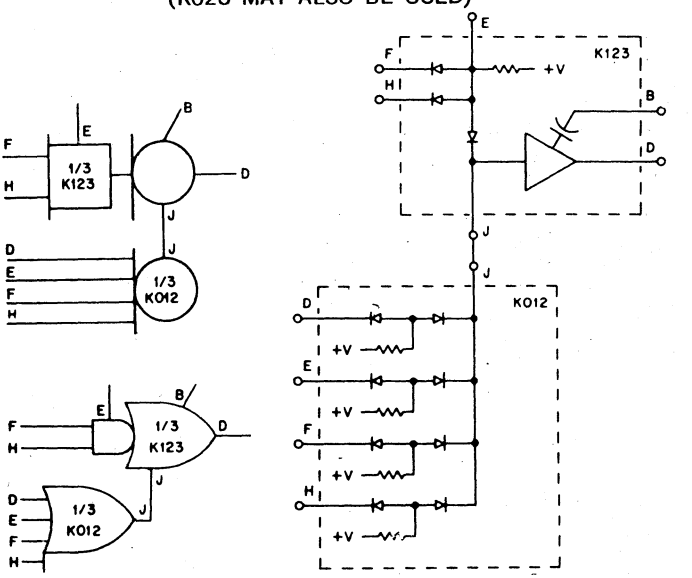
MIL



K003 AND/OR EXPANSION
(K026 MAY ALSO BE USED)

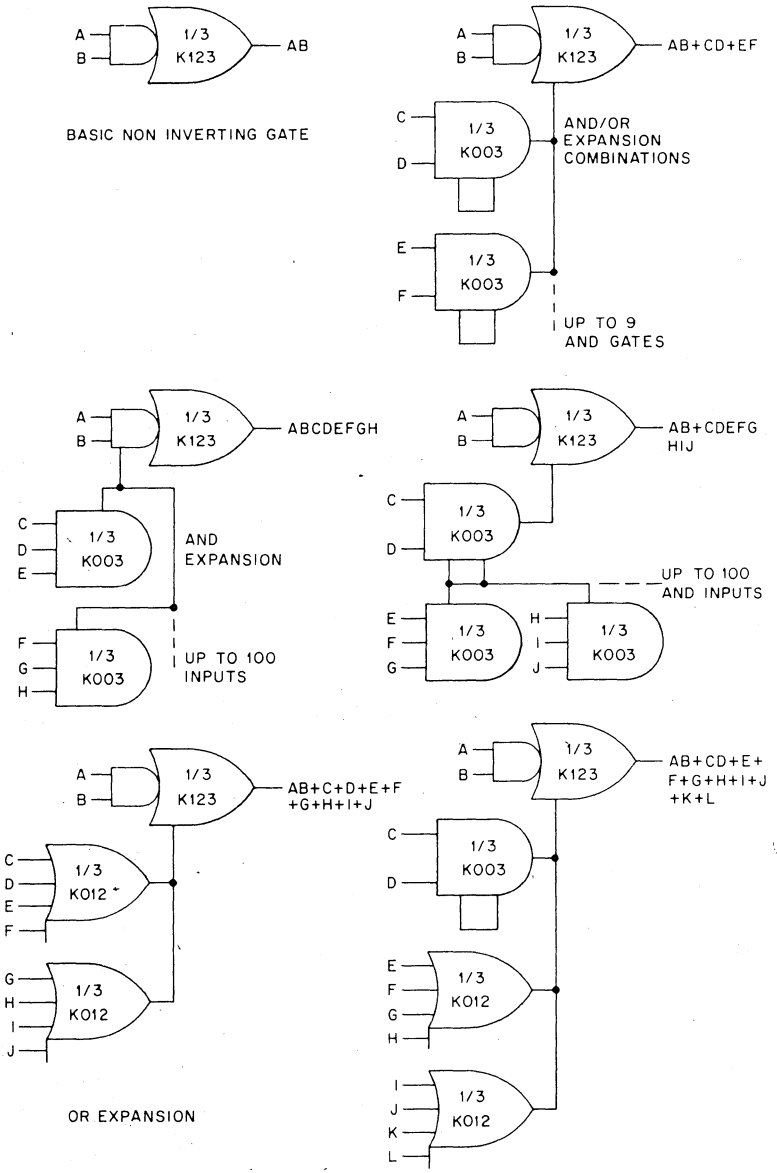
NEMA

MIL



K012 OR EXPANSION

The basic types of logic function obtainable by expansion are shown below for the K123 non-inverting gate. Logic functions for the expanded K113 inverting gate are identical except for inversion of the output. Letters refer to logic signal names rather than module pin numbers.

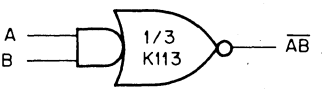


LOGIC FUNCTIONS WITH GATE EXPANSION

NAND, NOR, EXCLUSIVE OR

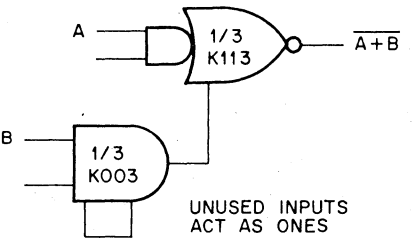
The K113 inverting gate performs the NAND function directly, and performs the NOR function when combined with a K003 expander.

With proper input connections, the K124 non-inverting gate performs the exclusive OR function.



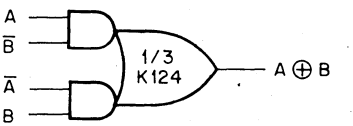
A	B	$\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

NAND FUNCTION OF BASIC INVERTING GATE



A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

NOR FUNCTION OF BASIC INVERTING GATE
WITH EXPANDER

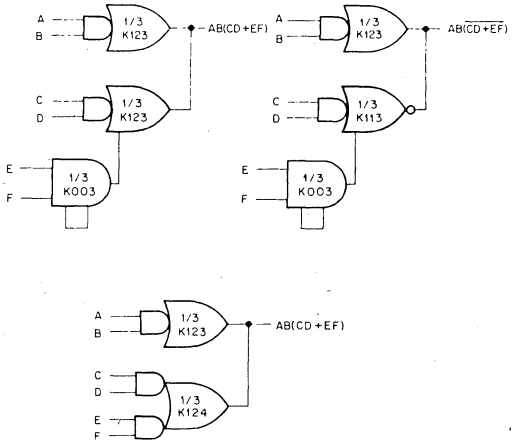


A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

EXCLUSIVE OR USING THE K124 GATE

WIRED AND

Wired AND functions can be obtained by connecting K123 outputs to other K124, K123 or K113 outputs as shown below.



WIRED AND EXAMPLES

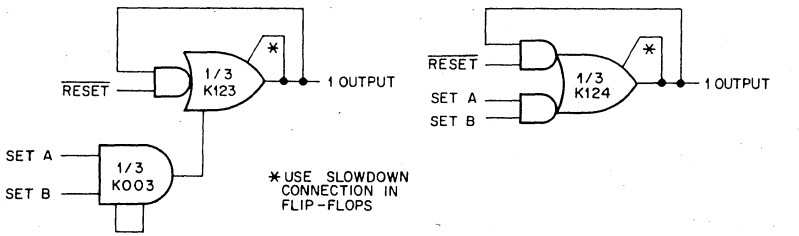
SUMMARY OF GATE-EXPANDER LOGIC COMBINATIONS

FOR ZERO VOLTS DEFINED AS LOGIC ZERO standard definition			
Logic Function	No. of Inputs	Expanders	Gates
AND	2	none	1/3 K123
	3-5	1/3 K003	1/3 K123
	6-8	2/3 K003	1/3 K123
OR	2	1/3 K003 or 1/3 K012	1/3 K123
	3-5	1/3 K012	1/3 K123
	6-9	2/3 K012	1/3 K123
NAND	2	none	1/3 K113
	3-5	1/3 K003	1/3 K113
	6-8	2/3 K003	1/3 K113
NOR	2	1/3 K003 or 1/3 K012	1/3 K113
	3-5	1/3 K012	1/3 K113
	6-9	2/3 K012	1/3 K113

FOR ZERO VOLTS DEFINED AS LOGIC ONE (inverted definition)			
Logic Function	No. of Inputs	Expanders	Gates
AND	2	1/3 K003 or 1/3 K012	1/3 K123
	3-5	1/3 K012	1/3 K123
	6-9	2/3 K012	1/3 K123
OR	2	none	1/3 K123
	3-5	1/3 K003	1/3 K123
	6-8	2/3 K003	1/3 K123
NAND	2	1/3 K003 or 1/3 K012	1/3 K113
	3-5	1/3 K012	1/3 K113
	6-9	2/3 K012	1/3 K113
NOR	2	none	1/3 K113
	3-5	1/3 K003	1/3 K113
	6-8	2/3 K003	1/3 K113

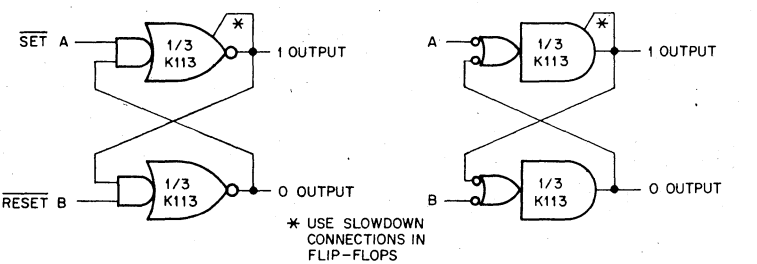
CONTROL FLIP-FLOPS FROM GATES

Control flip-flops can be formed by interconnection of gates as shown below.



NON-INVERTING GATE CONTROL FLIP-FLOP

The output of the flip-flop above is set to a ONE when the two SET inputs are both ONEs. A ZERO at the RESET input returns the output to ZERO, provided at least one of the SET inputs is also ZERO.

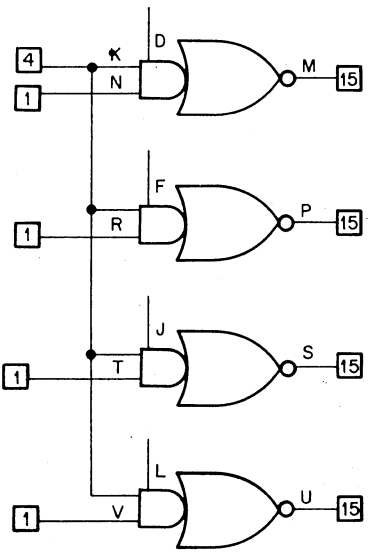


INVERTING GATE CONTROL FLIP-FLOP

The flip-flop above, made from two inverting gates, provides complementary 1 and 0 outputs. A truth table is shown below.

TRUTH TABLE

$\overline{SET}$	$\overline{RESET}$	1 OUTPUT	0-OUTPUT
0	0	1	1
0	1	1	0
1	0	0	1
1	1	NO CHANGE	

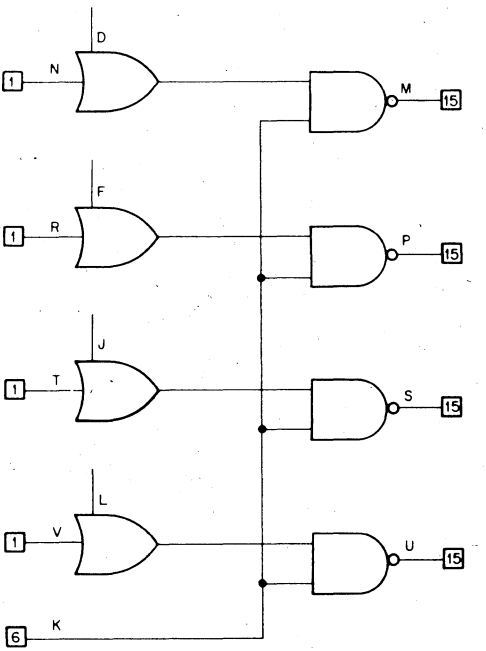


K134 INVERTERS

Four flip-flop functional modules such as K210, K220, K230 can conveniently be augmented by a K134 to get "0" as well as "1" outputs. The K134 is also provided with expansion and inhibit inputs for use as the readout element of ready-only memories using K281 diode memories (See Applications Notes). A common input at pin K can force all four outputs high, a helpful feature for building large K281 memories or very large K161 decoders.

K134 inverters may also be AND expanded by K003 gate expanders, providing an efficient way to obtain 4-input NAND or inverted NOR gates.

K134 — $13



K135 INVERTERS

The K135 module was designed primarily for the K725 I/O box, but it may be used in applications that require inverters with "OR" expandability. A common input at pin K can force all four outputs high regardless of the "OR" gate inputs. This feature is useful if a K161 decoder is used for multiplexing K135 modules, since all outputs for the same bit can be wire "AND"ed together.

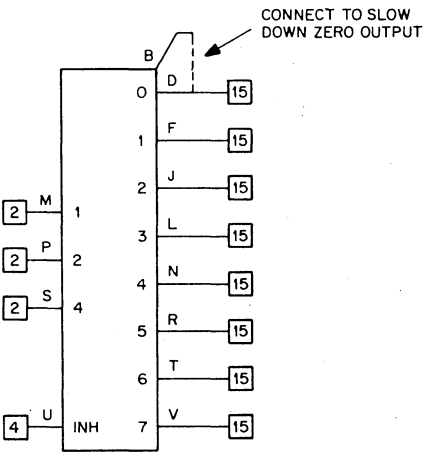
The loading on pin K is initially 6 with no "OR" expansions and increases by "1" unit load for each "OR" input that is added to the module. For example, if a K012 expander was added to each of the four inverters, the total pin K load would be 22 unit loads.

K003 expanders can be used for AND/OR expandability. The number of AND inputs on a given OR input does not affect the loading of pin K.

K135 — $13

BINARY TO OCTAL DECODER
K161

K SERIES



K161 DECODER

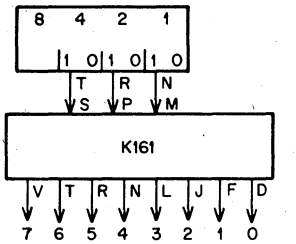
Three-bit binary numbers at the input to the K161 will be decoded into eight one-at-a-time outputs. Both inputs and outputs are high for assertion. The inhibit input allows BCD to ten line decoders to be built, or permits several decoders to be interconnected for sixteen, twenty-four, thirty-two outputs, etc. Inhibit input may be left open if unused, even though high is the inhibit state. When the K161 is being used with M series, all input signals must be buffered with K series gates. This is necessary due to the 3 volt thresholds in the K161.

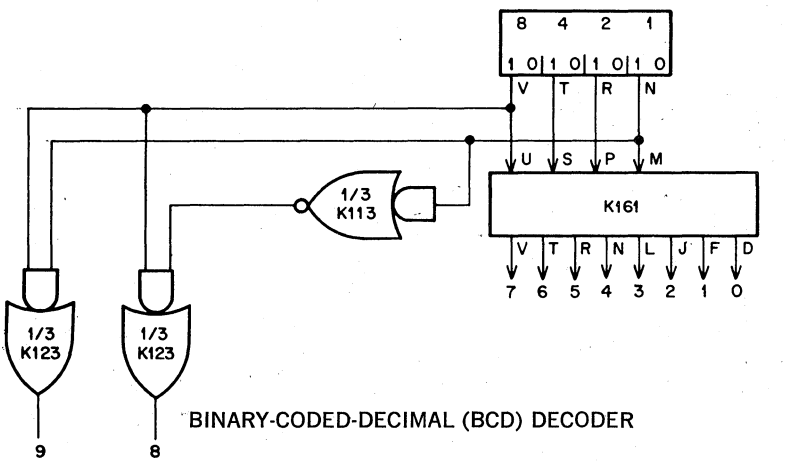
Standard K Series slowdown circuits on each output minimize and for most purposes nullify the splinter pulses that all decoders emit during input transitions. Additional slowdown available on the zero output can usually suppress the larger splinter that may occur there. But since splinter size is ultimately determined by input timing tolerances, it is cleanest to avoid logic designs in which a decoder output is used as a source of pulses.

The diagrams below show how to connect decoders for 8, 10, 16 and 32 outputs. Much larger decoders are possible, and in fact up to 256 outputs or even more can be obtained by inhibiting all but one of several decoders.

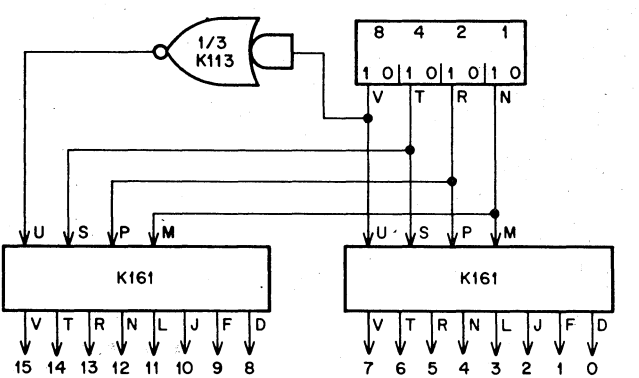
K161 — $25

8 STATE DECODER

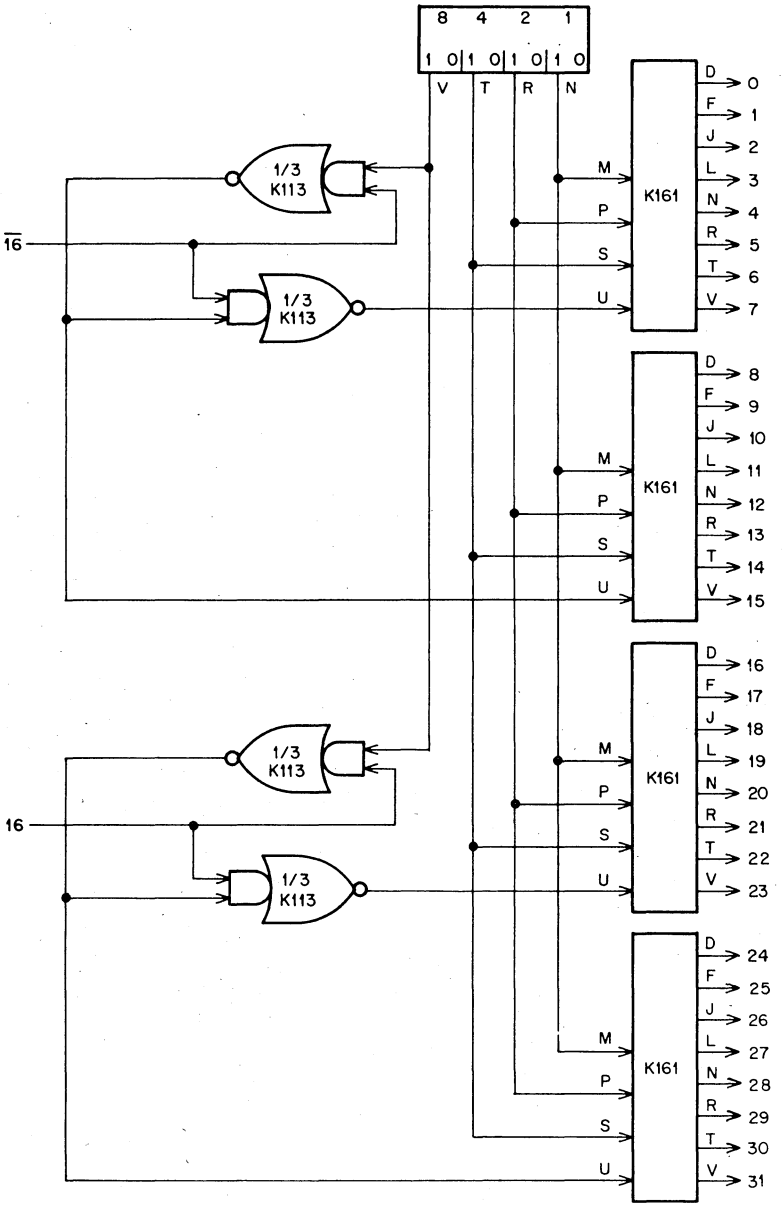




BINARY-CODED-DECIMAL (BCD) DECODER



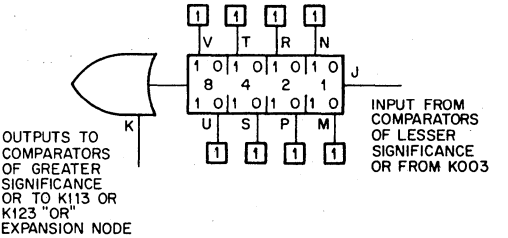
16 STATE DECODER



32 STATE DECODER

DIGITAL COMPARATOR
K174

K SERIES



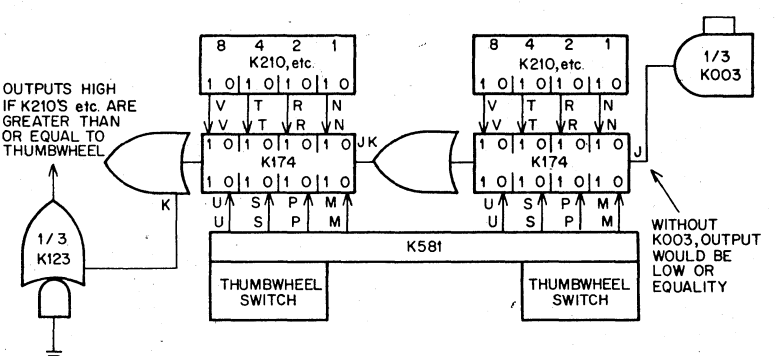
K174 DIGITAL COMPARATOR

Numerical comparisons such as those required in digital positioning controls are facilitated by the K174. Performing the same function as the comparator is closed-loop analog systems, the K174 tells which of two quantities is larger.

Fundamentally, the K174 performs a subtraction to determine whether a "borrow" would be needed to obtain a positive result. The magnitude of the difference is not available; only the sign.

Note in the example below that the output on pin K will be low only if the magnitude of the number in the K210's is less than the thumbwheels.

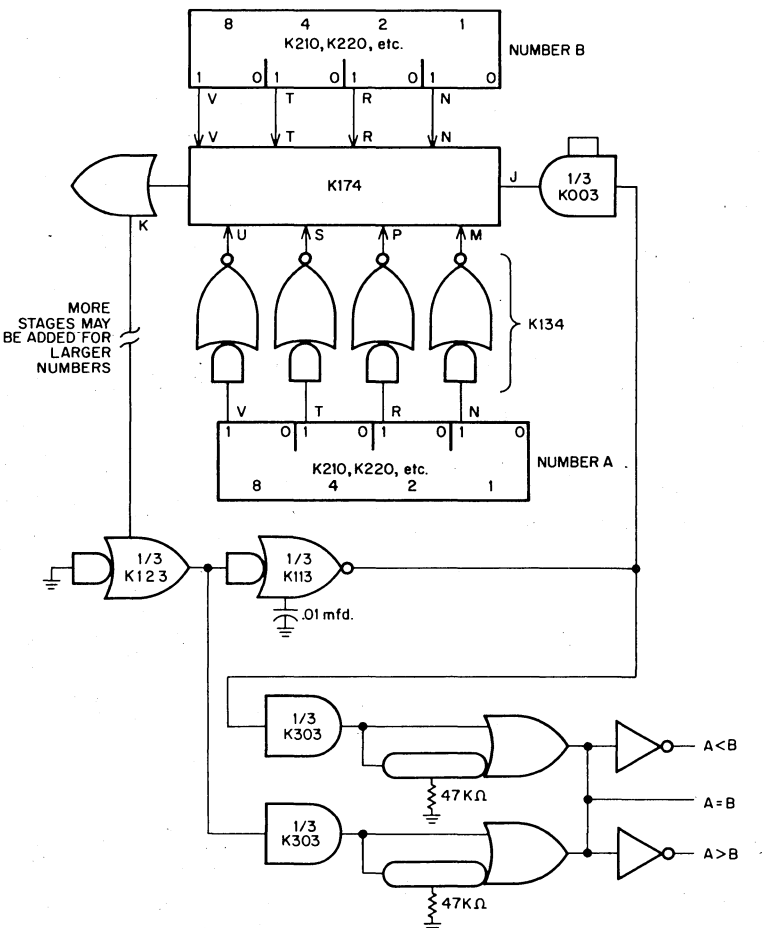
If more than four bits are to be compared, several comparators may be cascaded as shown below. Note use of K003 as if expanding an "OR" to control the state of the output for the case of equal input numbers.



TWO DIGIT COMPARISON OF THUMBWHEELS AGAINST K210, ETC.

If the numbers being compared are not multiples of 4 bits then one of the inputs on each unused comparitor position must be connected to +5 and the other one to ground.

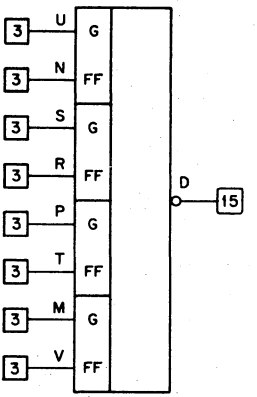
The K174 can also be used to obtain three independent outputs for full-greater-than, equal-to, less-than capability. The application below takes advantage of the fact that if A is equal to B, K will go high if J goes high and K will go low if J goes low. By inverting the output at pin K and feeding it back to pin J, the K174 will oscillate if A = B. If the timers are adjusted for a delay longer than the period of oscillation, the three possible output states can be obtained (High for assertion). With the values shown, the frequency will be approximately 50 KHz. Outputs respond to new conditions in 100 μsec.



K174 — $18

RATE MULTIPLIER
K184

K SERIES



If the four outputs of K210 counter are wired to K184 "F" inputs, and a four-bit binary fraction presented in reverse order to the corresponding "G" inputs, a pulse train is emitted at an average rate equal to the product of the K210 input rate and the binary fraction. Each transition from "0" to "1" at an FF input produces a 5 μsec output pulse to ground, if the corresponding "G" input has been high for 5 microseconds or more. Inputs are not rise-time sensitive. Outputs from several rate multipliers may be combined to give any desired precision.

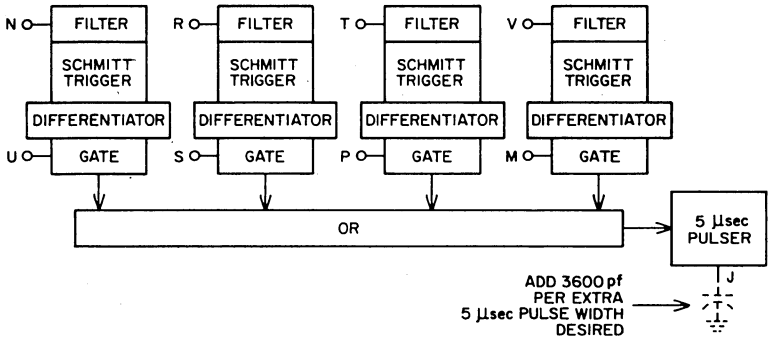
Rate multipliers are primarily useful in numerical control applications, such as those described in the following magazine articles:

"Linear Interpolation" *Control Engineering*, June '64, p. 79.

"Curvilinear Interpolation" *Control Engineering*, April '68, p. 81.

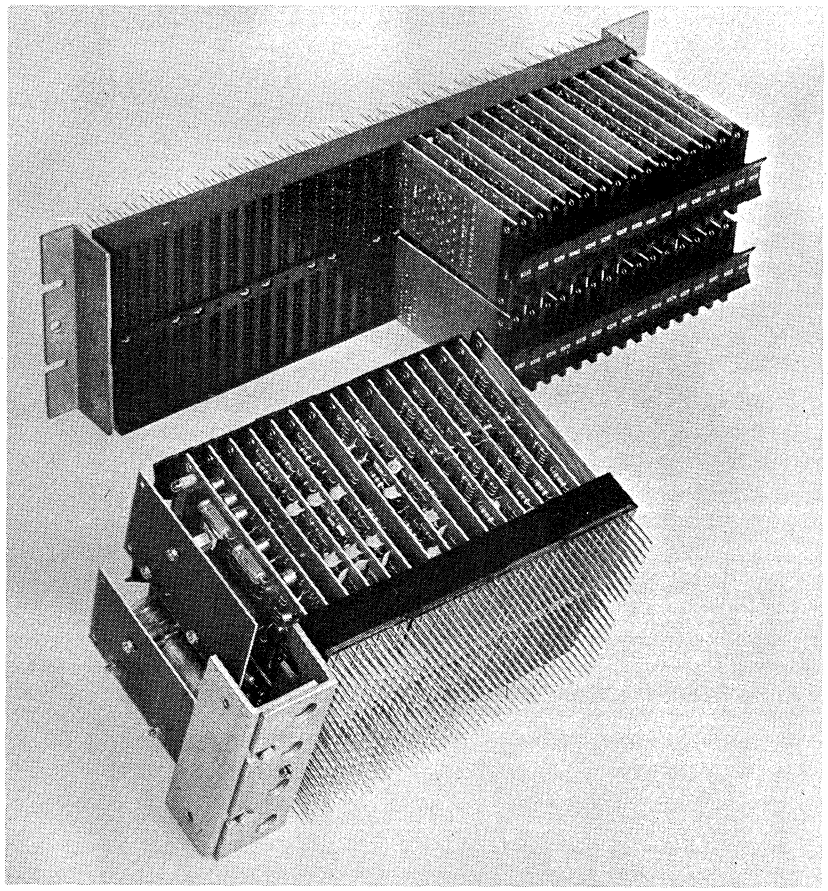
"Many Digital Functions Can Be Generated With A Rate Multiplier" *Electronic Design*, Feb. 1, '68, p. 82.

In addition, the K184 can provide several other useful functions that take advantage of its internal complexities.



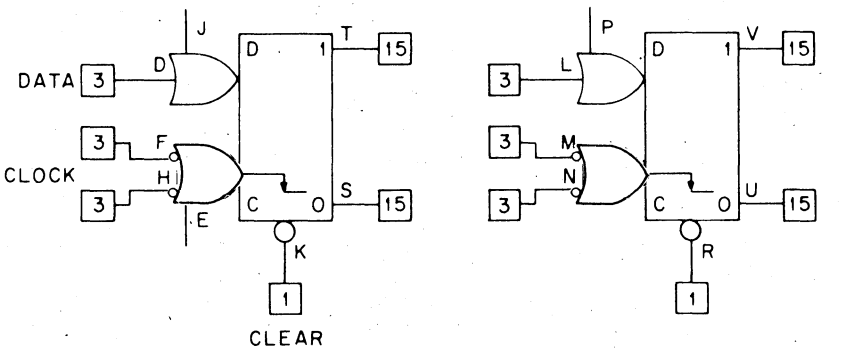
LOGICAL EQUIVALENT OF K184 RATE MULTIPLIER

K184 — $18



FLIP-FLOP
K202

K SERIES



K202 flip-flops do shifting, complementing, counting, and other functions beyond the capabilities of simple set-reset flip-flops built up from logic gates. They also may be used to extend K210 counters or K230 shift registers.

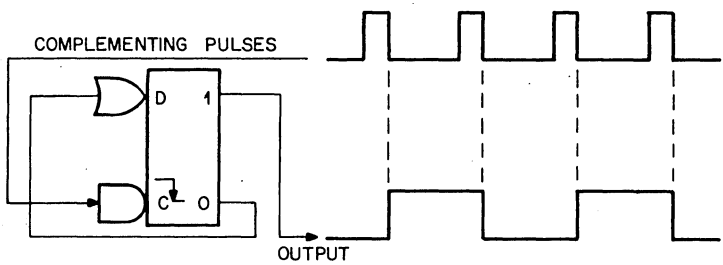
When the output of the clock gate falls from high to low, the information at the OR input (pins D-J, L-P) is transferred into the flip-flop. Pin J (or P) is ORed with the pin D (or L) input. Like pins J and P of a logic gate, these pins can be driven only from a K003, K012 or K026 expander.

Time is required for flip-flops and delayed inputs to adjust to new signals. The clock gate output must not fall to zero sooner than 4 μsec after its own rise, the end of a clear signal, or a change on associated data input pins.

A K202 flip-flop is cleared by grounding the clear input pin. The flip-flop is held in the zero state as long as the clear input is zero volts, regardless of other inputs.

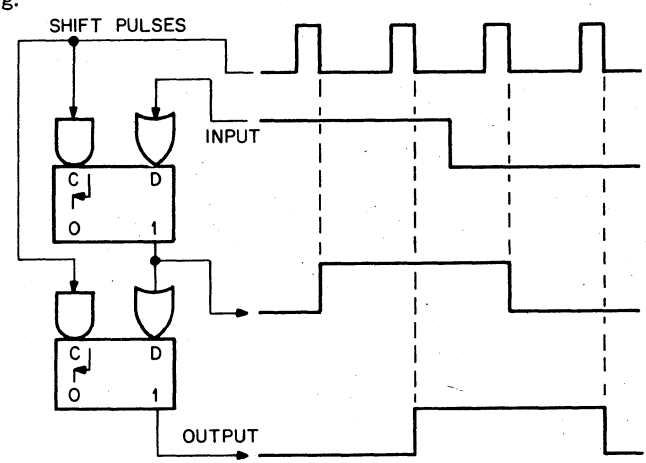
When using a K202 flip-flop to extend the length of a K230 shift register, pins B on both modules must be left open (unslowed). Pin B slows the clock inputs of the K202 for complementing correctly at slow speeds in very noisy surroundings; but the data inputs are not affected by pin B.

Complementing: Below is shown a complementing application. Here the information stored at the data input is the opposite of the flip-flop's present state. Each time the clock gate output changes from "1" to "0", the opposite of the current state is read in.



K202 COMPLEMENTING

Shift Register: The diagram below shows two flip-flops connected as a two-stage shift register. At each step the incoming signal, whether high or low, is set into the first stage of the register, and the original content of the first stage is set into the second stage. The input to each flip-flop must be stable for at least 4 microseconds before another shift pulse occurs, for reliable shifting.



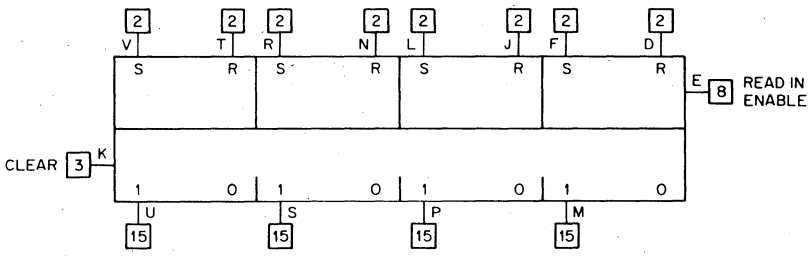
K202 2-STAGE SHIFT REGISTER

Note: In older systems of logic, most flip-flop functions had to be performed by general-purpose flip-flops like the K202. The K Series, however, includes functional types K210, K220, and K230 which are both less expensive and easier to use than the K202 for most applications. Think of the K202 primarily as a complementing control flip-flop and register extender.

K202 — $27

FLIP-FLOP REGISTER
K206

K SERIES



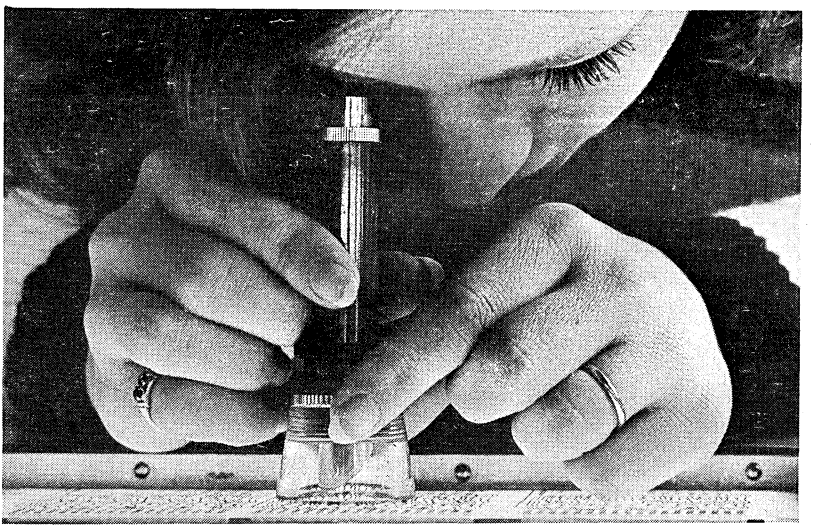
K206 FLIP-FLOP REGISTER

The four set-reset flip-flops in the K206 are arranged for convenient addressing from the outputs of a K161 Binary to Octal Decoder. The flip-flop outputs can then be wired to control and maintain the state of corresponding output drivers, providing addressable output conditioning from teletypes, computers, or fixed-memory sequence controllers.

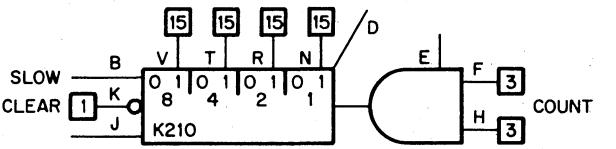
In addition, the same decoder may be used to address a particular K578 input sampler by grounding the K206 enable input when flip-flop changes are not desired. Pin E enable fanin on the K206 is reduced to 2 milliamperes when K161 addressing is used.

Since most control systems have about half as many digital outputs as inputs, it is convenient to use the least significant bit of the K161 address to determine which flip-flop state is wanted. Odd addresses allow for setting; even addresses, resetting. All flip-flops may be reset together by grounding the clear input, pin K.

K206 — $20



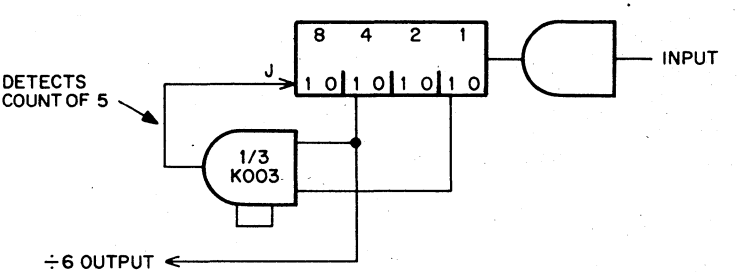
All DEC modules are exhaustively inspected and tested, both visually and electronically. A typical module undergoes a printed circuit board inspection procedure that consists of over 70 individual steps.



The K210 is a binary or BCD counter that can be wired to return to zero after any number of input cycles from 2 to 16. Count-up occurs when the COUNT gate output steps to zero. Decimal counting logic is built in; when pin D is unused, the counter resets to zero on the next count after nine. When pin D is grounded, the counter overflows to zero, after a count of 15. (Pin D is not intended for dynamic switching between binary and BCD counting.)

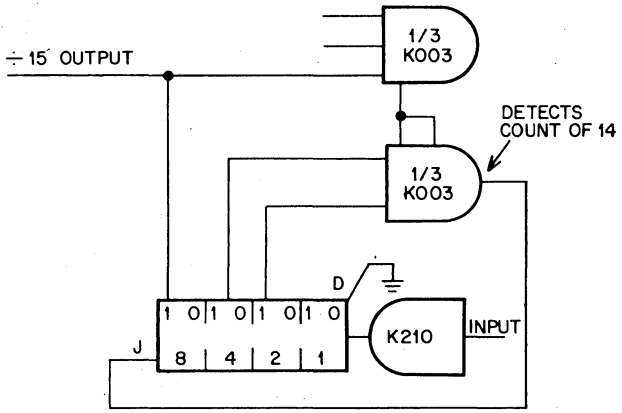
The counter is reset by grounding the clear input for 4 microseconds or more. A positive level at the J input from a K003 expander also resets the counter on the next high to low transition of the COUNT gate output for counts other than 10 or 16.

Wire the K003 as a decoder to detect one count less than the desired modulus. (Detect 5 for a count-of-6 counter, etc.)



K210 CONNECTED FOR COUNT OF 6

For counts above 10, ground pin D. Combine two K003 expanders as shown below, where three counter outputs must be sensed (to divide by 12, 14, or 15).

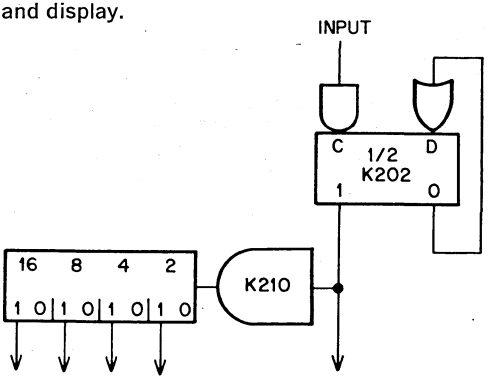


K210 CONNECTED FOR COUNT OF 15

Time is required for flip-flops and pin J reset logic to adjust to new inputs. The count gate output must not step to zero sooner than 4.0 μsec after its own rise, a change at pin J, or the end of a clearing signal at pin K. **When pin B is grounded for slowdown, allow 50 μsec.**
Larger counters are obtained by cascading K210's or adding K202 flip-flops. To cascade K210 modules, wire the most significant output of one counter to the input gate of the next. Inputs to the least significant stage can be either pulses or logic transitions to ground; risetime is not important.

Any transducer such as a switch, photocell, pulse tachometer, thermistor probe, or others compatible with K508 or K524 input converters can generate the signal which is to be counted. The lack of input risetime restrictions may allow transducer outputs to drive K210 counters directly if damaging transients can be avoided, as when the transducer shares the logic system environment.

For visual readout of binary-coded decimal counters, the four outputs from each K210 may be connected to corresponding input pins on a K671 decoding driver and display.

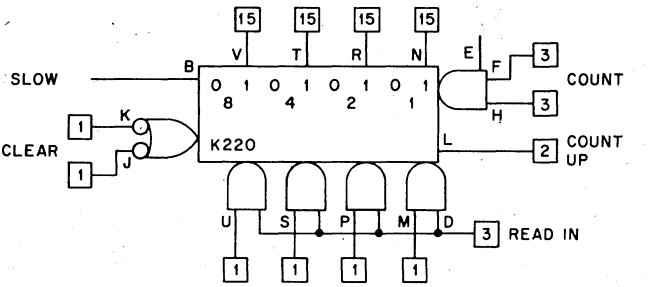


K210 AUGMENTED WITH K202 FOR COUNT OF 32

K210 — $27

UP/DOWN COUNTER
K220

K SERIES

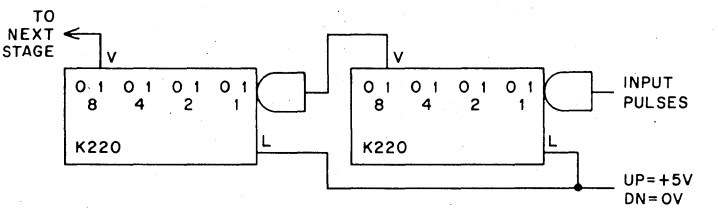


(DOUBLE-SIZE BOARD)

Four flip-flops and all the gates needed for binary-coded decimal up counting, down counting, presetting, and clearing are built into the K220. Up-down counters are useful for many digital position readout and feedback applications.

The direction of counting is established by the signal at pin L, high for up counting and low for down counting. Pin L count direction changes should finish no later than 4.0 μsec before next count input.

When K220 counters are cascaded, a single connection from the "8" output of one K220 to the count input gate of the next establishes both carry and borrow propagation.



CASCADED K220 COUNTER

K220 — $52

Up-counts occur when input makes the transition from high to low (+5 v to 0 v), as in K210 and K230. Down-counts, however, take place on the transition from low to high (0 v to +5 v). Thus both carry and borrow signals propagate via the simple connection from 8-weight output to 10-weight input.

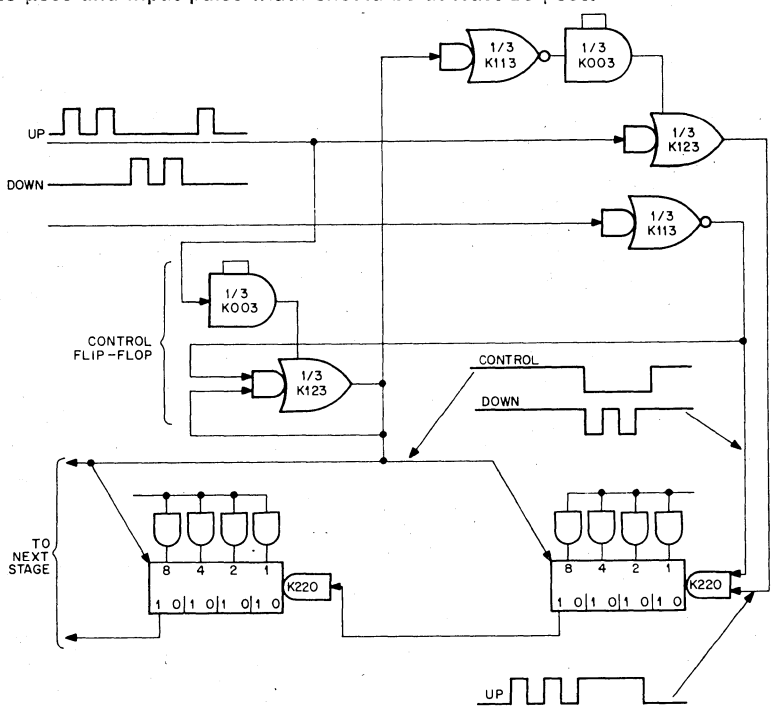
ONEs present at readin gate pins U,S,P, or M are read into the respective flip-flops when pin D makes the transitions from low to high. The transition at pin D should finish not later than 4.0 μsec before next count input. Transition from low to high at pin D should also begin no sooner than 4.0 μsec after any previous transition at pins D,M,P,S, or U. Ground any unused readin gate inputs to prevent readin of undesired ONEs.

Grounding pin J or K forces all flip-flops to zero for as long as either clear input remains low.

Time is required for flip-flops, counting logic, or readin gates to adjust to new inputs. Except clear inputs, no counter input may be changed within 4 μsec of a transition at any other input (Refers to logical output of count gate). When pin B is grounded for slowdown, allow 50 μsec.

All connections are made on the upper connector, except two: binary Up/Down counting may be obtained by grounding pins D and E on lower connector.

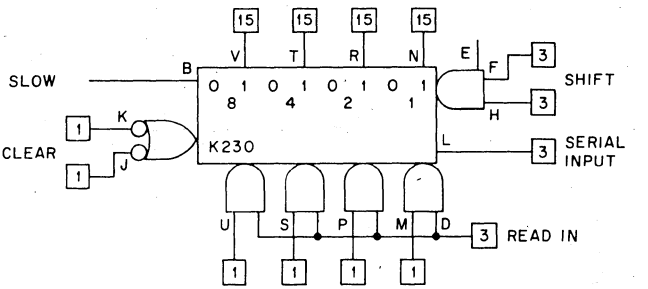
Below is shown a means for accepting up and down pulse-trains from two separate sources. For this application input pulse spacing should be at least 20 μsec and input pulse width should be at least 10 μsec.



UP/DOWN COUNTER
FOR SEPARATE PULSE SOURCES TO 50Kc

SHIFT REGISTER
K230

K SERIES



(DOUBLE-HEIGHT BOARD, ALL CONNECTIONS ARE TO UPPER SOCKET)

Information presented to pin L of this four stage flip-flop register is shifted toward pin V with each transition from "1" to "0" at the shift input gate.

ONEs present at readin gate input pins M,P,S, or U are read into the respective flip-flops when pin D makes the transition from low to high. The pin D transition should finish no later than 4.0 μsec before the next count input. Transition from low to high at pin D should also begin no sooner than 4.0 μsec after any previous transition at pins D,M,P,S, or U. Ground any unused readin gate inputs to prevent readin of undesired ONEs.

Grounding pin J or K forces all flip-flops to zero for as long as either clear input remains low.

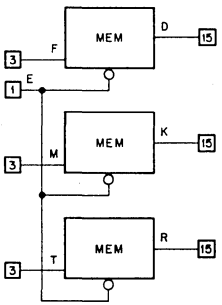
Shift registers of any length can be formed by tying pin V of one K230 to pin L of the next, and operating all shift gates together. Supply all shift pulses from the same device to maintain synchronism. The propagation delay of even one gate is too large a difference between two shift inputs on the same register. For every 20 bits that are required, duplicate the last stage of the shift-generating logic and tie the outputs in parallel to all K230 shift gate inputs.

Time is required for flip-flops, shifting logic or readin gates to adjust to new inputs. Except clear inputs, no register input may be changed within 4 μsec after a transition at any other input. (Refers to logical output of shift gate). When pin B is grounded for slowdown, allow 50 μsec.

K230 — $36

RETENTIVE MEMORY
K273

K SERIES



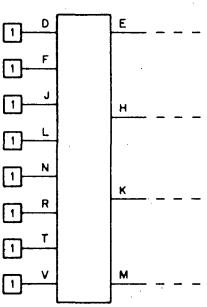
(DOUBLE THICKNESS MODULE)

Three magnetically latched mercury wetted contact relays in the K273 follow logic-level input information at rates up to 100 Hz, when pin E is grounded. Normally the OK Level output from a K731 source module drives pin E. When a line voltage failure is detected, pin E rises and each relay mechanically stores the last valid input data until full power returns.

K273 — $72

FIXED MEMORY
K281

K SERIES



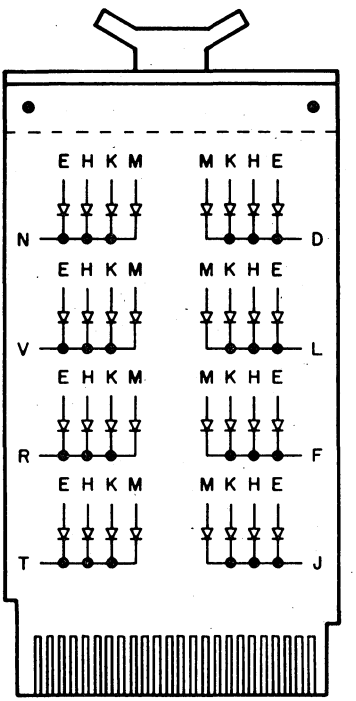
K281 FIXED MEMORY

The K281 is designed to be used with the K161 (Binary to Octal Decoder), the K681 (8-30 ma drivers) and the K134 (4 inverters), to build a read-only memory. Each K281 initially contains eight four-bit words consisting of only "1's". The user selects the codes he desires by cutting out diodes in the bit positions that are to be "0's". Additional K281 and K134 modules may be added to the system to generate more words and longer words. See Applications Notes for diagram of memory configuration.

K281 — $8

CODING THE K281 DIODE MEMORY

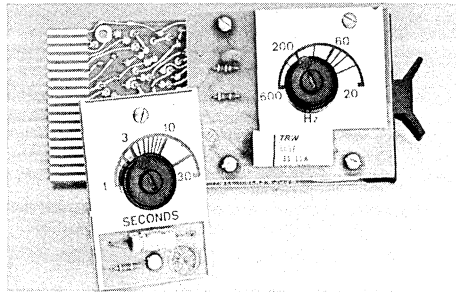
When the K281 is used to build a K-Series Read Only Memory, the codes are stored by cutting out diodes where zeros are desired. The diode map below shows the physical location of the diodes on the K281 and how they are connected to the module pins.



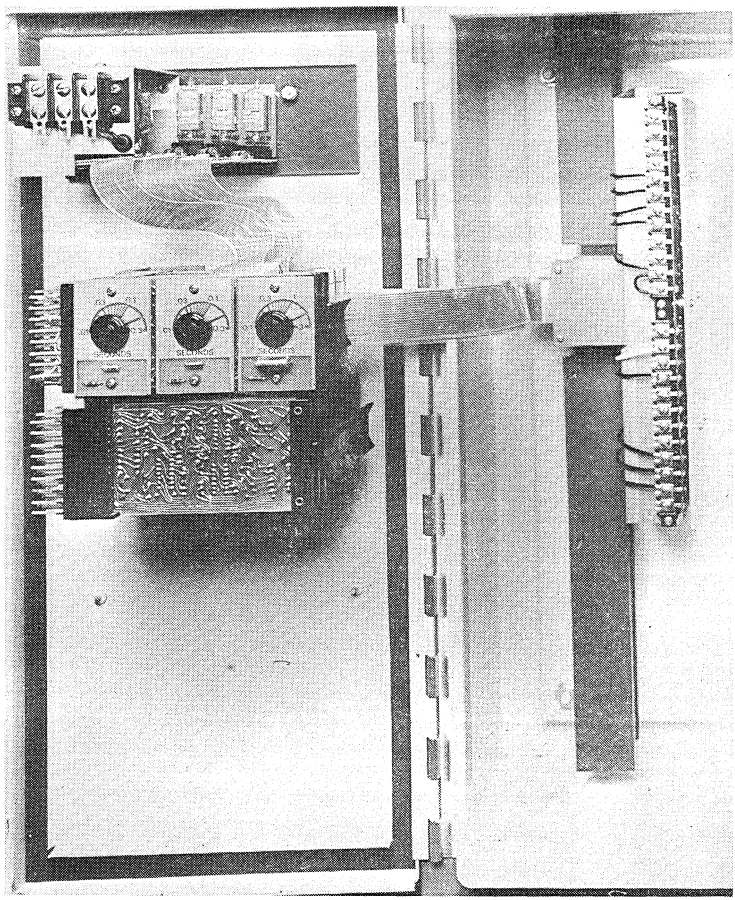
E, H, K, M are the four output pins.

D, F, J, L, N, R, T, V are the eight drive lines.

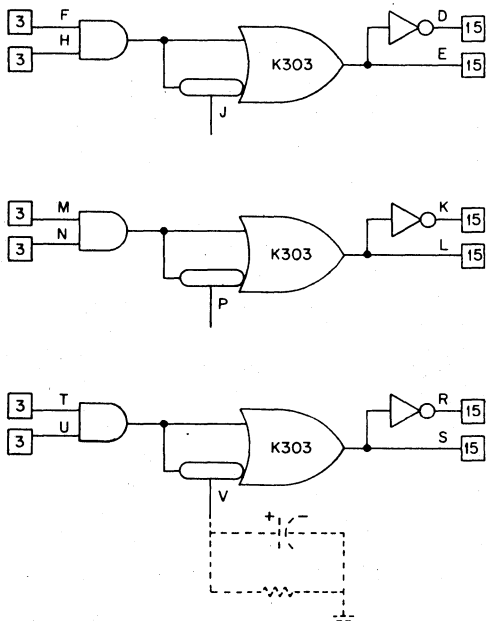
Component side up



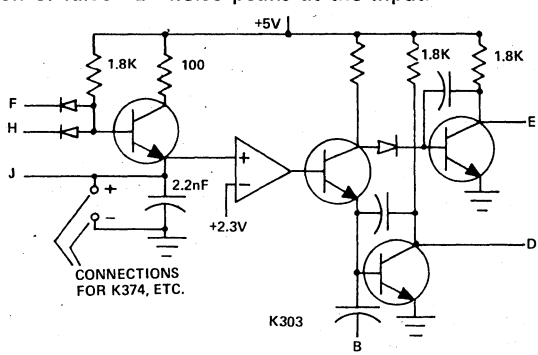
K303 WITH K373 AND K378



SMALL K-SERIES CONTROL INSTALLED IN NEMA 12 ENCLOSURE

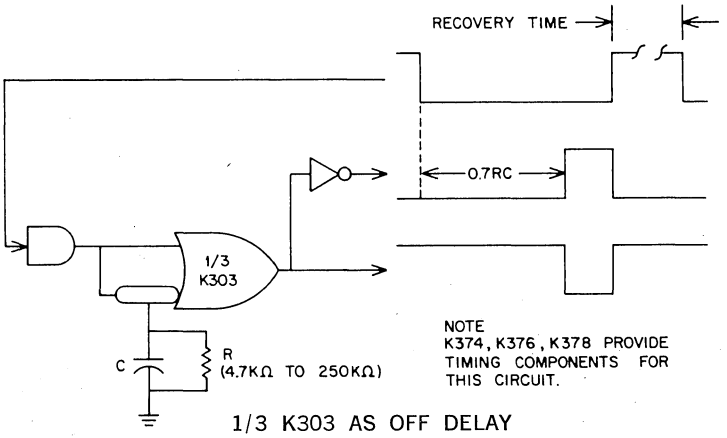


K303 timers provide time delays from 10 microseconds to 30 seconds and can be interconnected to form clocks with periods covering the same intervals. Fixed or adjustable delays and frequencies are obtainable. Calibrated controls are available (K371 through K378) for mounting directly on the K303. Remote controls can be added, if desired. A simplified schematic of the K303 is shown below. Note that the comparator has hysteresis, increasing the rejection of false "1" noise peaks at the input.



K303 TIMER SIMPLIFIED SCHEMATIC

When a K303 input gate steps to zero, the uninverted output falls after a controlled interval, while the inverted output rises. The interval can be as little as 10 μsec or as long as 30 seconds, depending on the size of the R and C connected to pin J,P, or V. Recovery begins when the input gate rises to 1. Allow recovery time of at least 0.3% of the maximum delay obtainable from the capacitor, in order to guarantee 95% repeat accuracy in the delay.



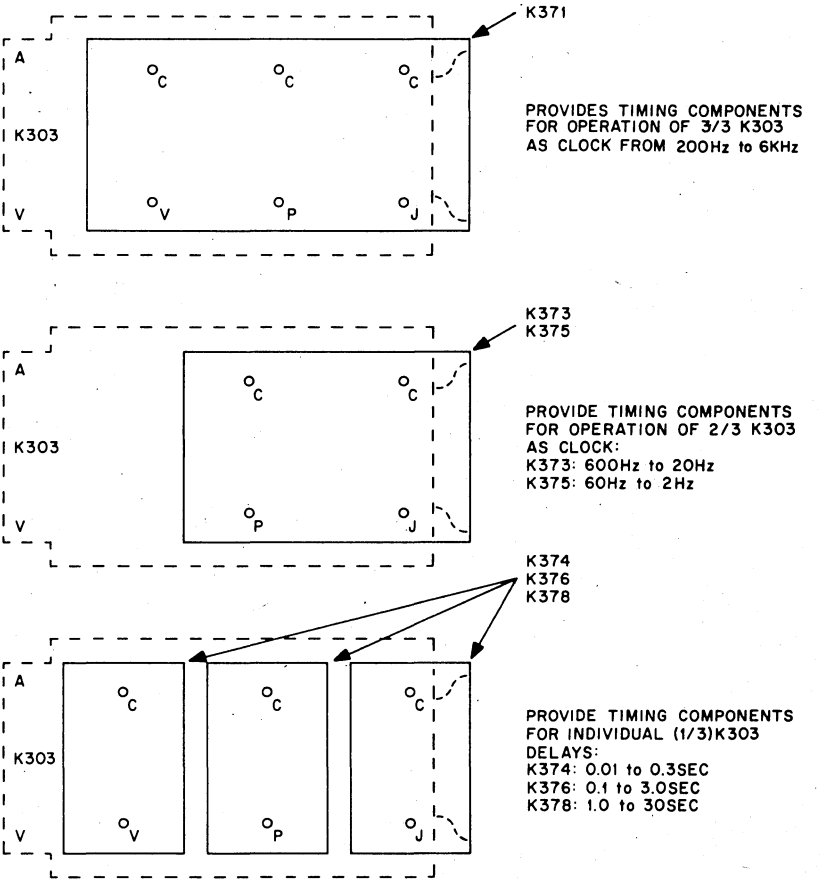
1/3 K303 AS OFF DELAY

A positive step at the input gate resets the K303 timer outputs. If the step occurs before a timeout is complete, the timeout is terminated and no change appears at the outputs. This property is sometimes convenient for establishing a pulse repetition rate threshold (Frequency Setpoint).

A built-in 2.2 nanofarad timing capacitor assures adequate noise rejection when external capacitors are mounted several inches from the timer. Time threshold for resetting is always several percent of rated recovery time, so that noise rejection time increases in proportion to the size of the timing capacitor. Remote rheostats and timing capacitors may be used, but noise rejection will be degraded. If several timing capacitors will be switch selected, wire in the smallest near the module and switch the others in parallel with it.

Variable or fixed timing resistors used with K303 timers may be any carbon composition, film, or wirewound rheostat or potentiometer. Delay time is linearly proportioned to resistance from 250KΩ down to a few thousand ohms, falling to zero (reset inhibited) below a few hundred ohms. Momentary shorting to ground of control pins will not cause damage, but a padding resistor of at least 300Ω in series with variable controls is advisable both to prevent continuous grounding and to avoid confusion which may arise if resetting is inhibited.

Timing capacitors may be any ordinary mica, paper, ceramic, or low leakage electrolytic type. For delays above a few seconds, wet slug tantalum electrolytic capacitors are advisable to avoid leakage-induced drift at high temperatures. Temperature coefficient of delay has been optimized for the carbon composition potentiometers and tantalum electrolytic capacitors used in the controls described below, and is typically less than ±1% in 5°C (9°F) using K731 and K732 regulators for power.

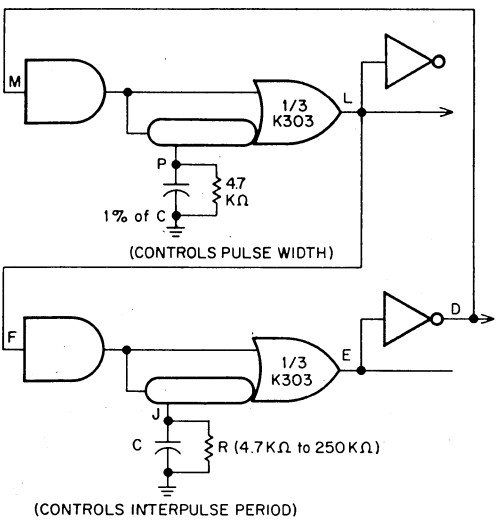


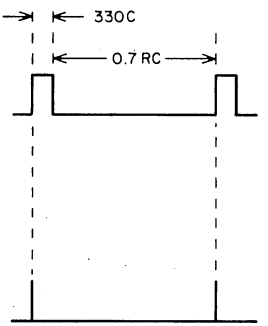
Calibrated controls for timers and clocks are available in several ranges. They mount to the K303 module by two screws per circuit, providing both mechanical and electrical connections. Each control includes a logarithmic potentiometer for easy settling over the full 30:1 calibrated range. Calibrations are approximate, meant for quick setup and easy control identification. Accurate time settings require the use of an oscilloscope, stopwatch, or other reliable time standard. These controls are intended for use at the end of K941 mounting bars.

Note: Time delay jitter is proportional to supply voltage ripple if times of the order of 1 msec are selected. For critical applications, use light loading on separate K731 or use H710 supply.

TIMER K303

Two K303 sections can be interconnected to make a free-running oscillator if one of the timing capacitors is about 100 times smaller than the other. The circuit with the larger capacitor will predominantly control the frequency. The diagram below shows the interconnections.





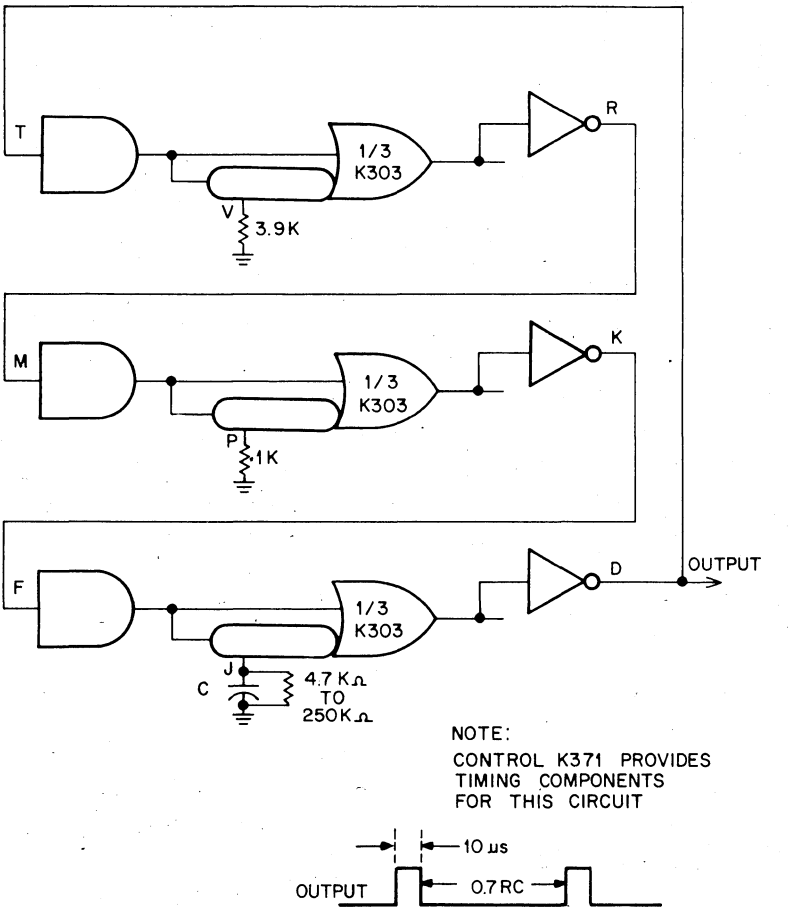
NOTE:
K373, K375 PROVIDE TIMING COMPONENTS FOR THIS CIRCUIT

$18.00
Plus: 2 resistors
2 capacitors

2/3 K303 AS CLOCK BELOW 1 KHz

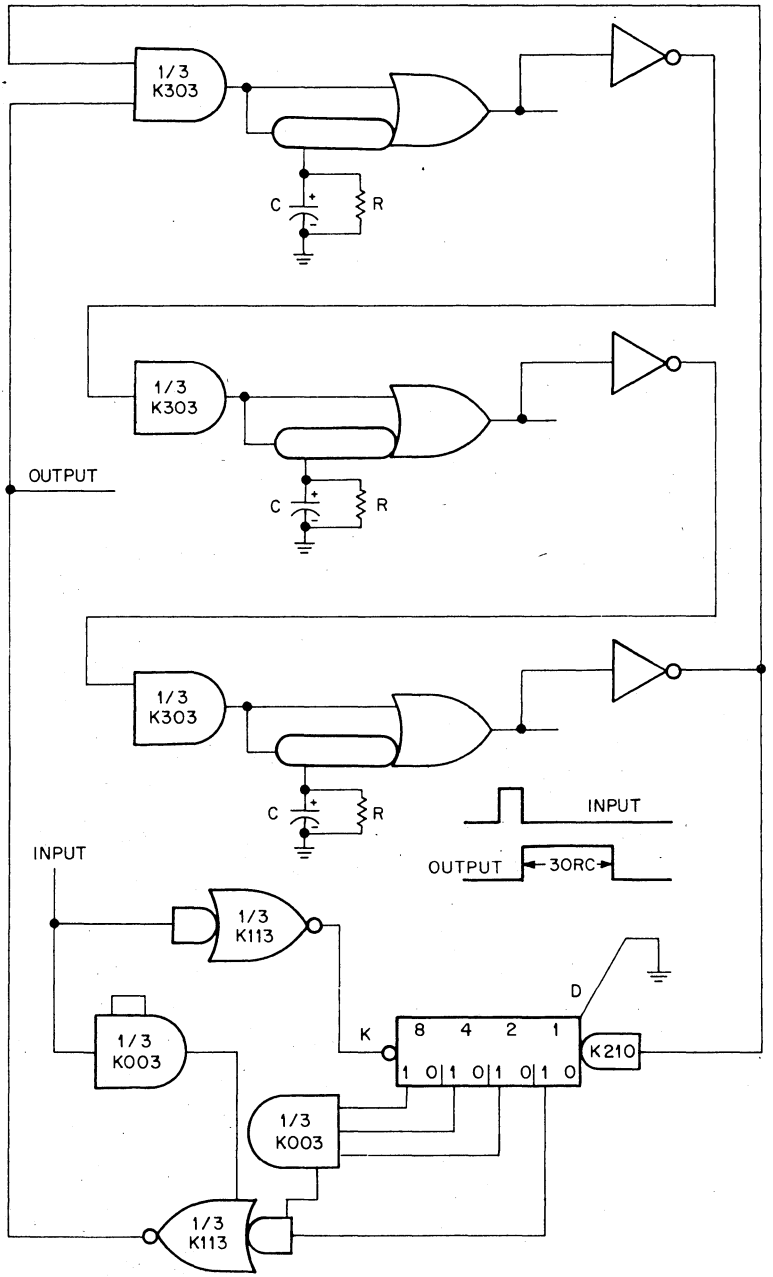
The 100 to 1 ratio of timing capacitors required limits this method to frequencies to 1 KHz or less, due to the 2.2 nanofarad capacitor built into each circuit. Three K303 circuits may be connected together for higher frequencies, as shown on next page.

K303 — $27
K371 — $8
K373 — $8
K374 — $7
K375 — $8
K376 — $7
K378 — $9

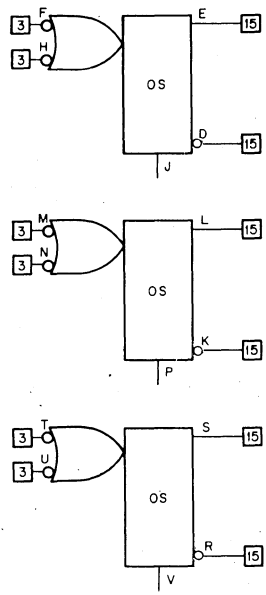


3/3 K303 AS CLOCK ABOVE 500 Hz

Longer delays than 30 seconds using large electrolytic capacitors would suffer from increased drift due to capacitor leakage. Moreover, there are some applications in which moisture and contamination cannot reliably be excluded from the electronics environment, making 250KΩ timing resistance impractical due to leakage along board surfaces. For either situation, two techniques are available: either cascade several timer circuits, or combine a clock-connected K303 with one or more K210 counters. The clock may be gated off at an unused input to avoid synchronizing errors. The diagram below shows both techniques combined, using one K210 and all three sections of a K303 to obtain a 22-minute delay.



TIMER FOR UP TO 22 MINUTES



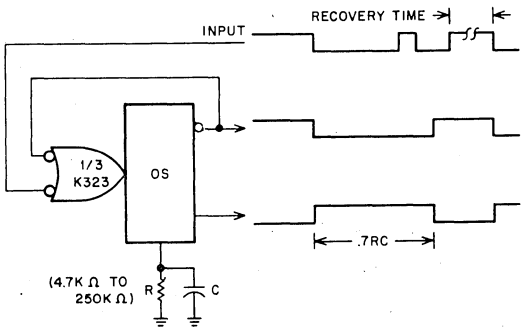
K323 one shots provide output pulse widths from 10 microseconds to 30 seconds with either fixed or adjustable delays. Calibrated controls are available (K374, K376 and K378) for mounting directly on the K323. Remote controls can be added, if desired.

When the K323 input gate steps to zero, the uninverted output rises and stays positive for the controlled interval time. The pulse width is controlled by the value of R and C connected to pin J, P, or V. The one shot recovery begins when the input gate rises to 1. Allow a recovery time of at least 0.3% of the maximum delay obtainable from the capacitor, in order to guarantee 95% repeat accuracy in pulse width.

K323 — $35

A positive step at the input gate forces the uninverted output low. If the step occurs before a time out is complete, the timeout is terminated and the pulse width will be unknown. This premature resetting can be eliminated by connecting the inverted output of the one shot to one of its AND inputs. This will make the one shot insensitive to input transitions during the time out period.

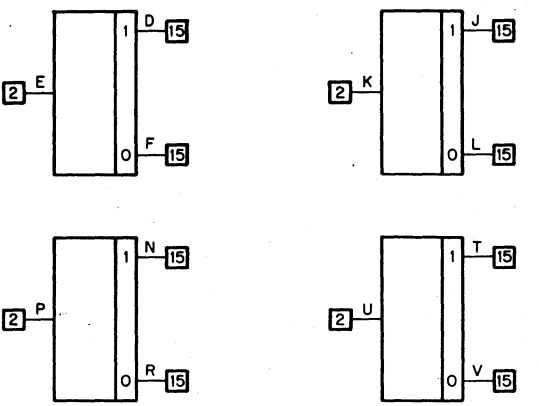
A positive pulse does not terminate the timeout



The K323 circuit is similar to the K303 Timer and uses the same techniques of noise rejection. For further information on resistors, capacitors and construction recommendations for external pulse width controls, please refer to the K303 module.

SCHMITT TRIGGERS
K501

K SERIES



The K501 can be used with the K580, K581, or K578 to provide simultaneous true and complement signals with full K series drive. Built in hysteresis and slowed outputs insure reliable operation in noisy signal environments.

Schmitt Triggers can also be used to speed up signals with very slow rise or fall times for input into pulse formers or logic circuits where timing considerations are critical.

The K501 is not designed to be connected directly to unfiltered contacts or other noisy signal sources.

K501 — $20

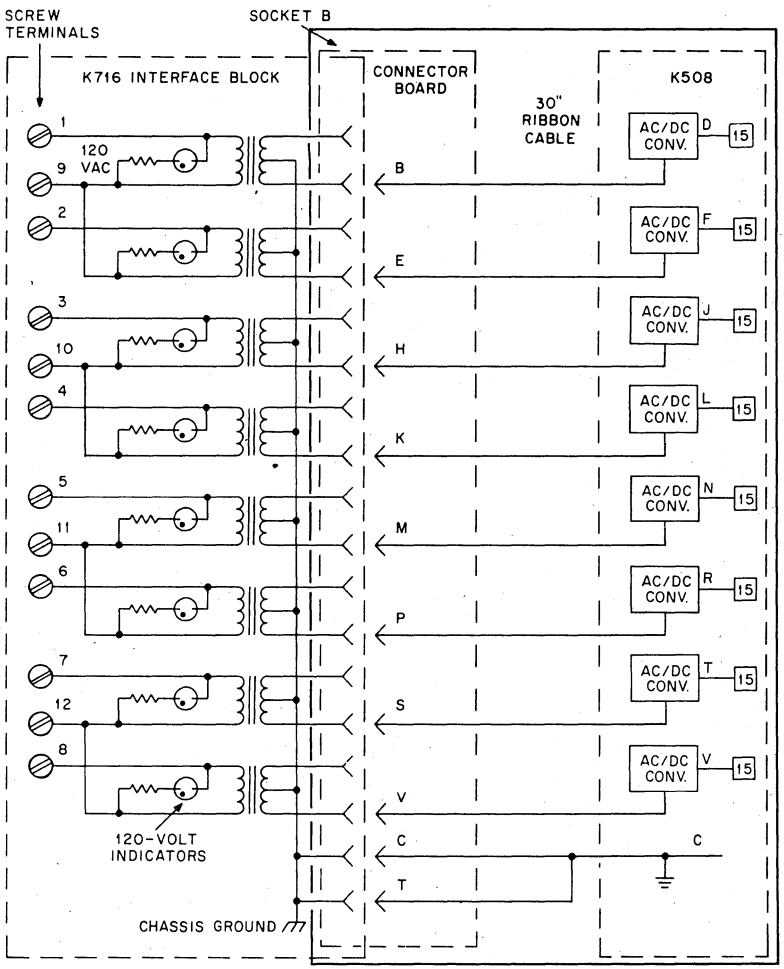
ACCESSORIES CONTAINING ELECTRONICS

On the following pages is a broad selection of interface modules. To help you get acquainted with the range of capabilities they offer, here is a summary table. Grouping by type of use to aid selection is not rigid. Maximum compatibility has been preserved to permit any combination of modules to be put together in the same system.

		Compatible Accessories			
Logic-to-Interface Connection and Type of Use	Module Type	K716 Interface Block	K724 K725 Shells	K782 Thru Terminal	K784 Diode Terminal
Integral 30" Flat cable connector. For small controls with heavy-duty field wiring	120 VAC input: K508	X			
	120/240 VAC output: K604	X		X	
	Transducer input: K524	X		X	
	2.5 Ampere DC Driver: K644	X		X	
Integral Terminals for larger systems	120 VAC input: K578		X		
	120/240 VAC output: K614		X		
	250 Volt DC Driver: K656		X		
	4 Amp Driver: K658		X		
Solder Lugs with strain relief. For indicators, control panels, and nearby transducers	Transducer Input: K522			X	
	Dry circuit switch filter: K580			X	
	Inverted switch filter: K581			X	
	Low power indicator driver: K681				X
	Indicator/Relay driver: K683				X
Integral 12" flat cable with NIXIE® tubes	Decimal Display: K671				

AC INPUT CONVERTER
TYPE K508

K SERIES



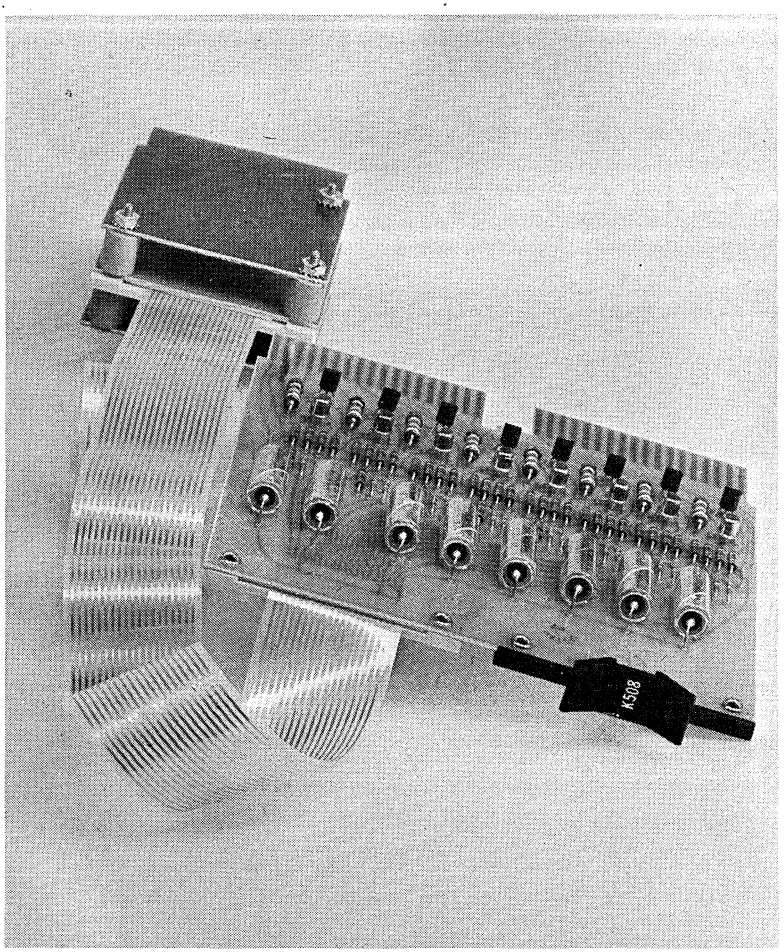
(DOUBLE-SIZE BOARD)

K508 — $44

The K508 AC input converter, operating through the K716 interface block, is designed for use with ordinary silver contacts in limit switches, pressure switches, pushbuttons and the like. Each input terminal presents a reactive load of 1 volt-ampere, which together with an external 120 volt AC pilot circuit voltage inhibits contamination buildup at the contact surface.

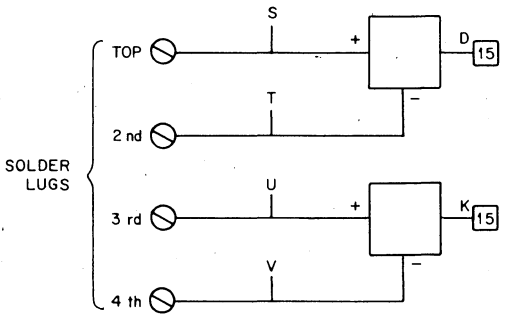
Electrical noise riding on pilot circuit wiring is attenuated in the input transformers and by hash filters at the K508 module. Contact bounce filtering is designed to respond to the first signal, and to leave the logic output in the "1" state in spite of skips lasting up to 100 milliseconds.

K508 output circuits have hysteresis, so that no intermediate output state can result from an ill-defined input condition. No separate Schmitt-triggers are required. Outputs are at ground for no input, at +5 volts when energized. All connections use upper connector.



SENSOR CONVERTER
K522

K SERIES



K522 SENSOR CONVERTER

The K522 Sensor Converter can take signals from photocells, thermistors, and other variable-resistance sensors and convert them to logic levels. Its built-in +1.8 volt reference, programmable hysteresis, and noise cancelling ability make it simple to use. The K522 does not, however, provide the tolerance to high level noise or accidental application of line voltage which is obtainable from the K524. The table below should help in deciding between the two types.

CHARACTERISTICS	K522	K524
Number of circuits	2	4
Module size	single	double
Input connections	solder lugs	cable connector
Inputs accessible at module connector	yes	no
DC differential mode possible	no	yes
Provision for adding transducer biasing trimpots in predrilled holes on board	yes	yes
Noise cancellation range (common mode)	±1 volt	±7.5 volts
Maximum + input range for correct output	0 to +5V	±30V
Tolerance to overvoltage (no damage)	±3 volts	140 VAC
Minimum hysteresis (deadband)	10mv	10mv
Maximum hysteresis	160mv	10mv
Maximum switching rate	50KHz	25KHz

K522 — $22

Minimum transducer resistance (at threshold)	400Ω	400Ω
Maximum transducer resistance (at threshold)	20KΩ	100KΩ
Noise Cancellation ratio at Line Frequency (CMR)	10:1	10:1
Noise Cancellation ratio at 1 KHz	20:1	20:1
Temperature Coefficient of Threshold (typical)	±1mv/°C (0.1%)	±1mv/°C (0.1%)

Note: Outputs are high when + input is high.

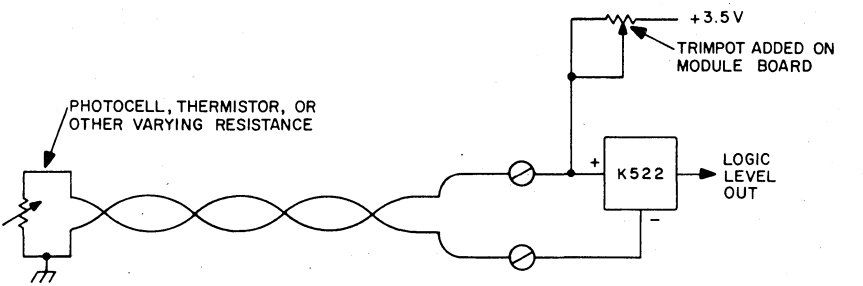
In general, the K522 is suited to laboratory and light machinery use where transducers are nearby and there is little danger of high voltage being applied to them accidentally. This is especially important when low resistance transducers are used with board mounted trimpots, since the trimpot provides a path from the transducer leads back to the logic supply. (If high voltage such as 120 VAC) were to get to the logic supply, all modules in the system would be destroyed.

The hysteresis of each K522 circuit can easily be selected in increments of 10 mv from a minimum of 10 mv (no connection) to a maximum of 160 mv by connecting one or more programming pins to the output.

Below is a table of pin connections for programming the hysteresis of each circuit.

Value when wired to converter output	10mv	20mv	40mv	80mv
Circuit 1 (Pin D)	E	F	H	J
Circuit 2 (Pin K)	L	M	N	P
Table of Hysteresis Programming Pins				

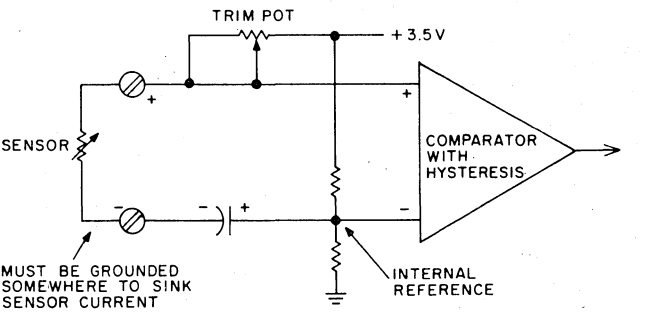
Example: To add 30 mv hysteresis to the basic 10 mv hysteresis for a total of 40 mv hysteresis, connect pins E and F or L and M to the circuit outputs.



K522 WITH NEARBY SENSOR

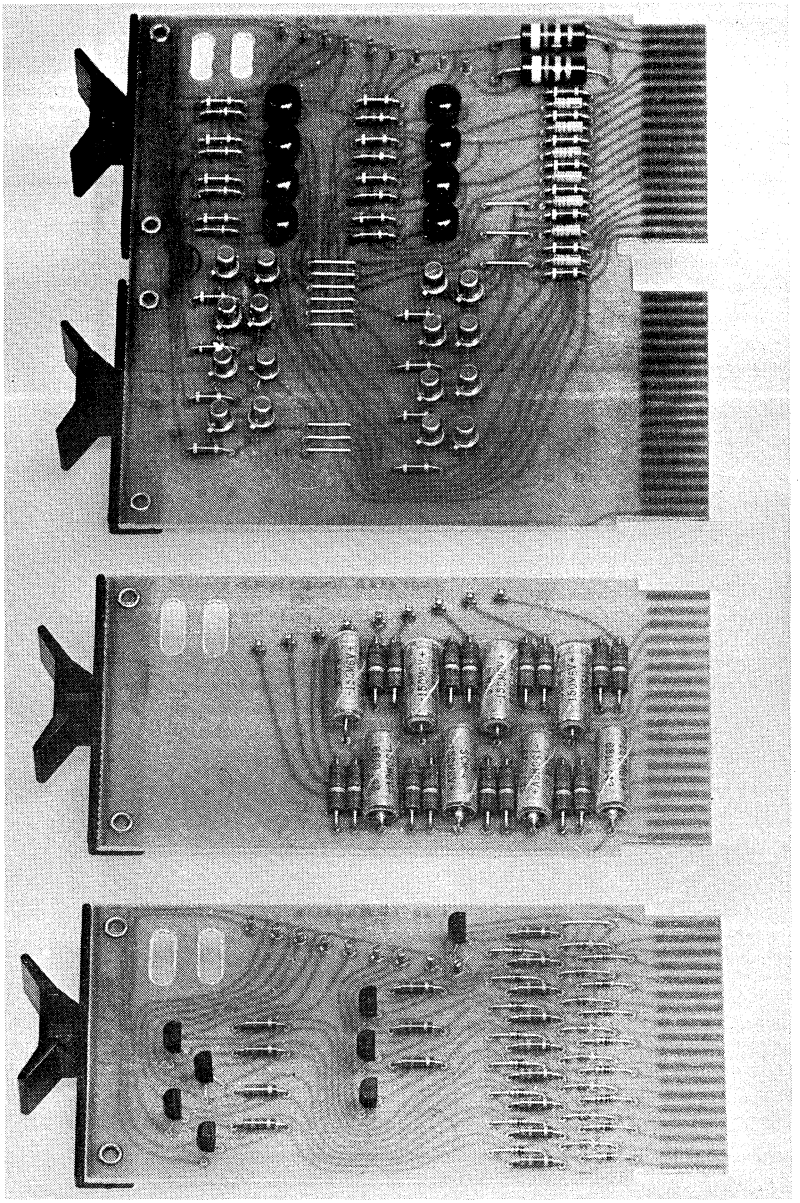
The diagram above shows how a sensor located a few feet from a K522 can be connected by a simple twisted pair of wires if the environmental noise is not too severe. Differences in potential between logic ground and chassis ground at the sensor are not likely to exceed ±1 volt in such a case, so the noise cancellation ability of the K522 circuit would be adequate to maintain a consistent threshold. Since the built-in reference in the K522 is half the voltage on the trimpot, and the switching threshold is half the voltage on the trimpot; the switching threshold will be near the point where the sensor and trimming resistances are equal, if 3.5v is used for bias.

If the sensor is ungrounded, a ground return must be provided at the module by tying pin T and/or pin V to ground. The simplified equivalent circuit below shows the AC coupling capacitor which makes this necessary.



K522 EQUIVALENT CIRCUIT

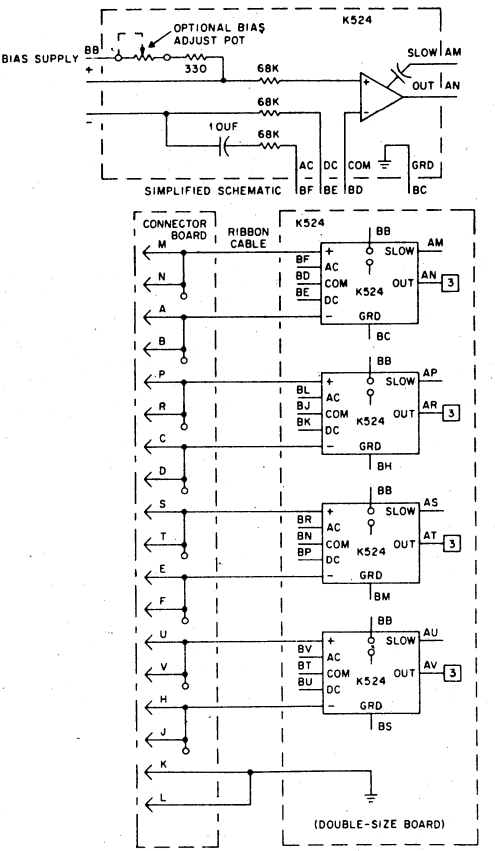
The K522 can also be used with a self-generating sensor such as a tachometer pickup, just as the K524 can.



OTHER MODULES HAVING SOLDER LUGS AND STRAIN RELIEF HOLES LIKE THE K522. SHOWN ARE K681, K580, AND K683.

SENSOR CONVERTER
K524

K SERIES



Basically a noise-rejecting, threshold sensing differential voltage amplifier the K524 is readily adapted to sensing threshold points in DC analog signals, AC signals, and pulses. It can also be biased to sense resistance thresholds. The differential amplifying technique permits flexible grounding and shielding methods to accommodate floating signal generators and minimize noise.

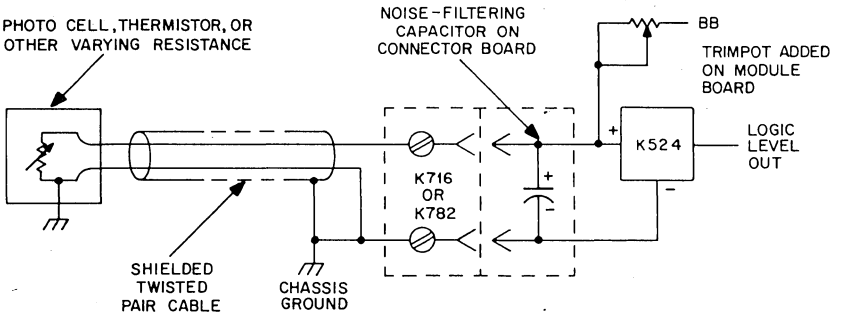
The K524 Sensor Converter senses voltage transitions or resistance thresholds by noise-rejecting differential amplification. A choice of AC or DC coupling is provided.

Output transitions occur when input voltage differentials are within 0.3 volts or less. When the "+" input is more positive, the output is a ONE. When the "+" input is more negative, the output is a ZERO.

K524 — $98

K524 APPLICATIONS

Below is shown a K524 circuit used in the same application as the K522 above, but where longer sensor leads and hence more noise is expected.

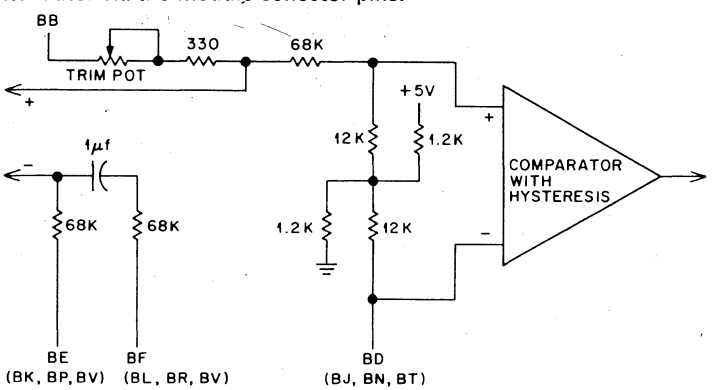


K524 WITH DISTANT SENSOR

Switching occurs at equality between sensor and biasing resistance when +5 volts is used for bias. Pin BB (pin B on lower connector) must be connected to an independent bias supply, such as a separate K731 operated from a separate transformer, to insure against damaging currents through the bias circuits to the logic in case of accidental high voltages at K524 inputs. This precaution is most essential in systems containing K604 or K644 output converters, since inadvertent use of the wrong K716 socket is possible. This problem does not arise with self-generating sensors or where bias is supplied externally to variable-resistance sensors.

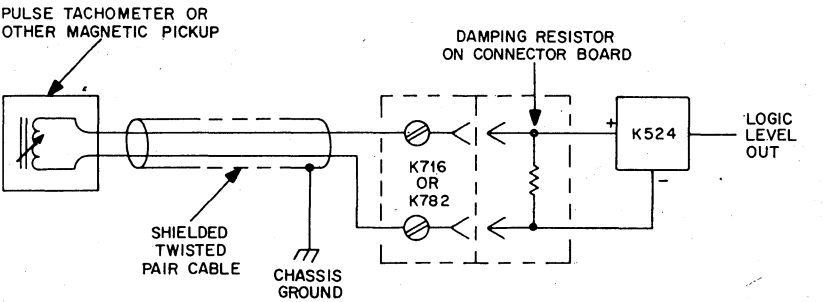
Since low-frequency noise injected by the chassis ground connection goes directly to the — input but is attenuated by the bias network at the + input, some loss of noise rejection will result. One way to restore full rejection would be to return the bias supply itself to the same noise source. If a K731 is used, this means both its transformer winding centertap and its pin C connections must be connected to ground only at the point where the cable is grounded.

Because of the more complex input network in the K524, allowing true DC differential operation if desired, one additional connection is required. The simplified schematic below shows that the inverting input to the internal comparator must be connected either to the DC-coupled or to the AC-coupled input attenuator via the module conector pins.



K524 EQUIVALENT CIRCUIT

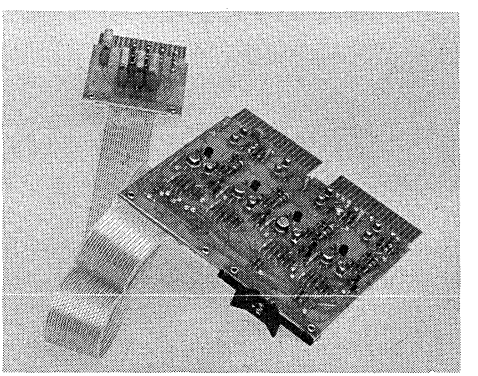
Below is shown another way to use the K524, this time with a self-generating transducer.



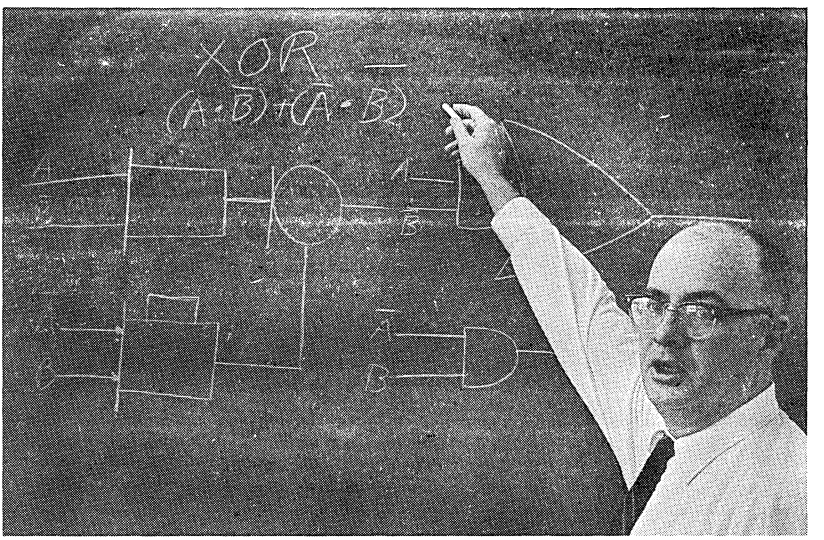
Here is a table showing the auxiliary pin connections on the lower module connector for the various applications of the K524.

APPLICATIONS	COUPLING	PIN CONNECTIONS
As low performance analog comparator, for comparing two photocells etc., or wherever reference is supplied externally.	DC (K524 only)	BD to BE, BJ to BK, BN to BP, BT to BV
Photocells, thermistors, pulse tachometers, pressure transducers or wherever it is convenient to use the internal 2.5 volt reference.	AC (see also K522)	BD to BF, BJ to BL, BN to BR, BT to BV

Signals up to 25 KHz, suitable for counting by K210 or K220 counters, can be obtained with symmetrical input signals having at least 1 volt excursions past the switching point. Maximum output rates can be limited to approximately 5KHz by tying together pins AM and AN, AP and AR, etc.



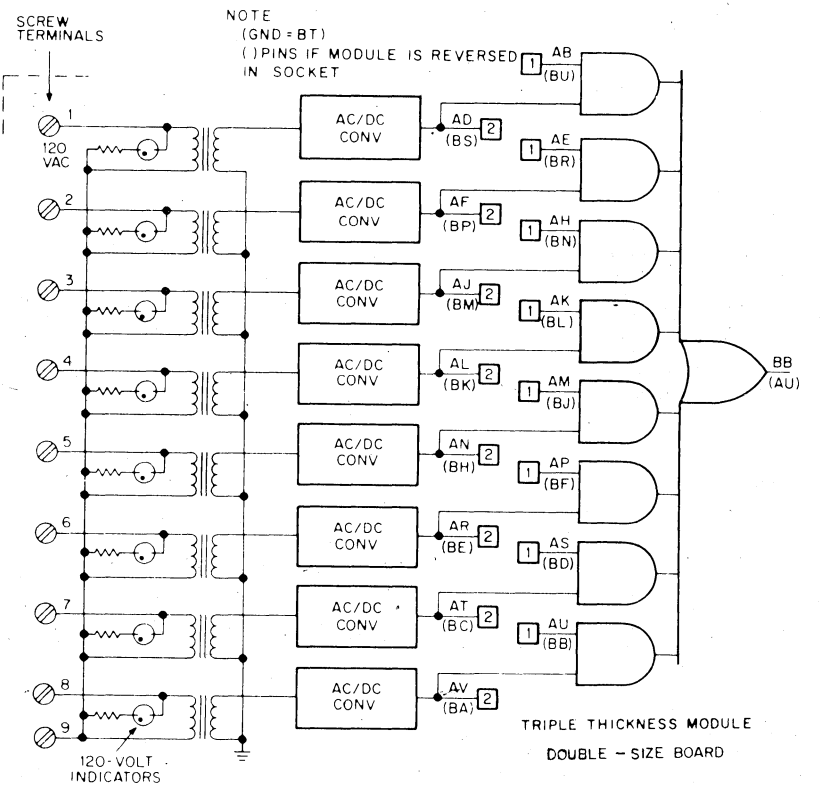
K524 SENSOR CONVERTER



DEC provides a series of seminars to educate its customers on DEC's module products. Here, William G. McNamara, Module Marketing Manager, is explaining digital logic.

120 VAC INPUT CONVERTER
K578

K SERIES



K578 AC INPUT CONVERTER

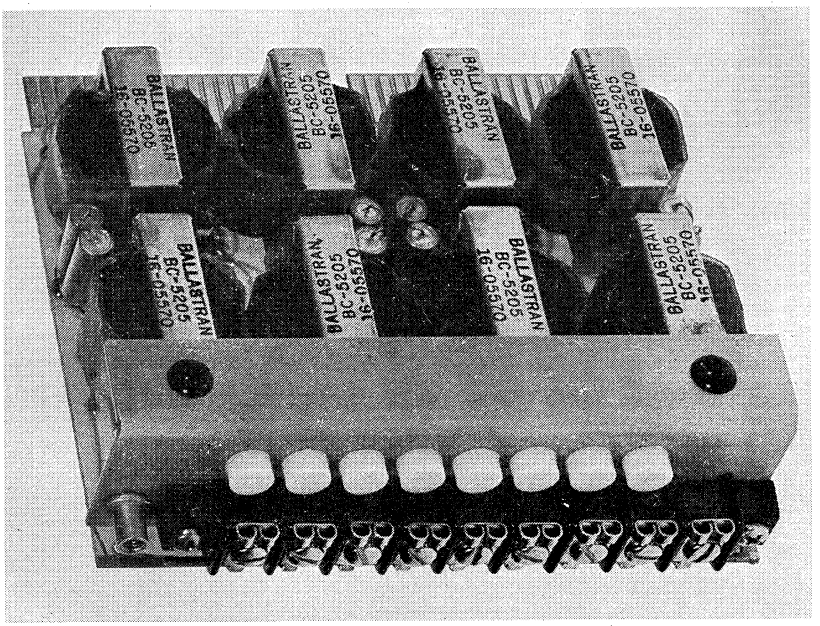
K578 — $80

The K578 input converter, when mounted in a K724 or K725 interface shell, provides logic levels from 120 VAC signals from limit switches, relays etc. The 1VA reactive load provided by the K578 isolation transformers insures sparking at pilot contacts. Together with the ample circuit voltage used, this reactive load assures maximum contact reliability.

Electrical noise riding on pilot circuit wiring is attenuated both by the input transformer and by RC filtering. Bounce filtering is designed to pick up by the end of the first full cycle of contact, and to drop out (return to "zero" output state) by the end of three full cycles after the input is removed. (About 50 milliseconds.) This speed of response is desirable in large sequential scanning-type control systems, even though occasionally a heavy contact may be observed to produce more than one output transition due to very long bounce duration. If necessary, response speed may be cut in half by tying 150 mfd from the offending logic output to ground. However since no Schmitt triggers are included in the K578 (unlike the K508), a K184 or K501 must be used as described in the applications notes if it is important to know exactly how many contact closures have occurred in a given period.

Gating circuits equivalent to four K026 sections are included for contact scanning applications using the K161, or to facilitate forming the logical OR of many inputs. Direct outputs are from circuits similar to the K580, and may not be wired together.

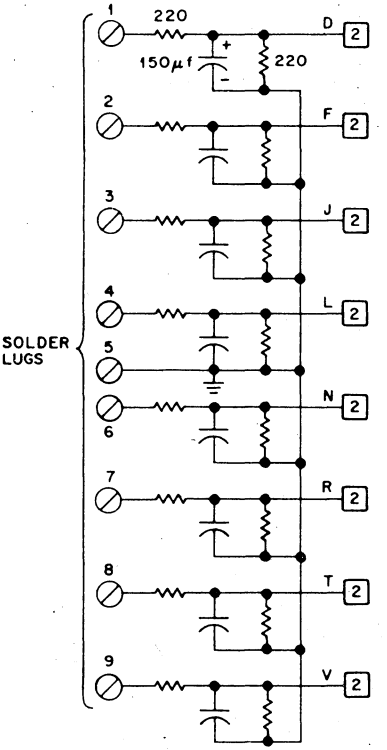
Clamp-type terminals on the K578 take two wires up to size 14. Neon indicators are included. The K578 can also be used in the K943 mounting panel, however some mechanical means of support must be provided tc hold the K578 in its socket if vibration is a consideration.



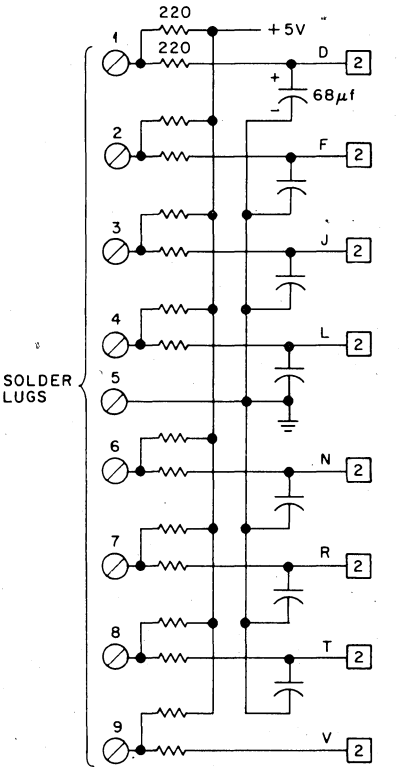
K578 TERMINAL STRIP CONNECTIONS FROM LEFT TO RIGHT ARE NUMBERS 1 TO 9

DRY CONTACT FILTERS
K580, K581

K SERIES



K580



K581

K580	$20
K581	$20

These filters convert signals from dry circuit or wiping contacts to logic levels. Primarily they are used with gold contacts such as the new encapsulated reed limit switches, thumbwheel switches, and the like. Those pushbuttons or slide switches that provide good wiping action will also operate reliably with these filters, but silver contacts designed for long life on heavy duty loads are likely to give trouble. For them, use interfaces designed for such application like K508-K716 or K578, or at least switch a high voltage. (see K580 voltage table.)

Access to K580 and K581 inputs is by solder lugs only. Strain relief holes are provided in board (near handle) for a 9-wire cable. The avoidance of contact connections on the logic wiring panel combined with heavy filtering guarantees noise isolation and protects modules by preventing accidental short circuits. Below is a summary of other characteristics.

	Contact Current	Contact Voltage	Output for Contact Closed	Time Delay on Closure	Time Delay on Opening
K580	22ma	See Table	high	10msec	30msec
K581	22ma	5V	low	20msec	20msec

(Time delay figures above are nominal, and assume connection to the input of a standard gate such as K113 or K123.)

The contact current for the K581 comes from the logic supply, making it very important to assure freedom from accidental high voltages on K581 inputs, which could damage many logic modules by getting through to the system power supply. This hazard is not present with the K580, which uses an external source of +10 volts or more. The table belows shows how external dropping resistors may be added to provide higher voltage operation.

TABLE OF K580 VOLTAGE DROPPING RESISTANCES

CONTACT SUPPLY VOLTAGE	10	12	15	24	28	48	90	100	120
Dropping Resistance	0	82Ω	220Ω	620Ω	820Ω	1.8KΩ	3.6KΩ	3.9KΩ	4.7KΩ
Dissipation	—	0.05W	0.11W	0.3W	0.4W	0.85W	1.8W	2.0W	2.5W

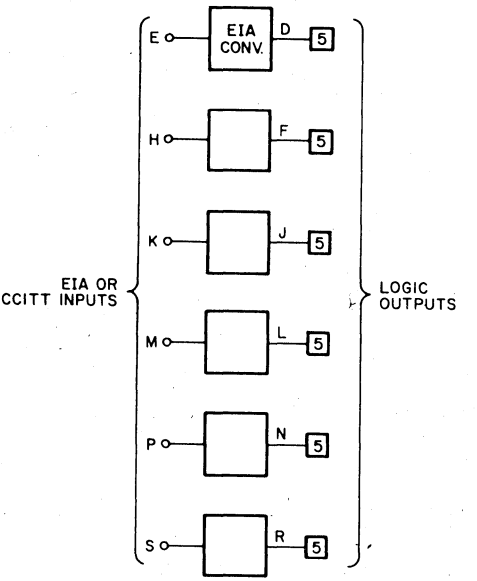
When using dropping resistors and higher voltage supplies, total tolerance of resistors and supply should be ±10% to insure high levels between +4V and +6V at the logic. Also observe that a handful of droping resistors in 90V or 120V systems may dissipate more power than the entire logic system, and must be located so as not to cause excessive temperature rise in the K series environment.

Note that these circuits may not be paralleled to obtain the wired OR or wired AND function, and that fanout is limited to 2 milliamperes in order to maintain the low (zero) output voltage within normal K-Series specifications. Fanout to ordinary logic gates and diode expanders may be raised to 4 milliamperes if some noise and contact bounce rejection can be traded off; but hysteresis inputs such as those at counter inputs, rate multiplier, etc., may not switch properly if the logic zero is allowed to rise much above +0.5V.

See application note for thumbwheel register multiplexing using K581.

EIA INPUT CONVERTER
K596

K SERIES



Any bipolar input signals with amplitudes between ±3 volts and ±25 volts will be transformed by this non-inverting converter into standard K-Series or M-Series logic signals with driving capabilities of 5 ma or 3 unit loads, respectively. Load for paralleling (wired OR): 1 milliampere. Input impedence stays between 3KΩ and 6KΩ for full capability with both the American EIA and the European CCITT standards for data transmission. Built-in noise filtering causes transition delays of several microseconds, limiting the maximum baud rate that can be handled.

Open-circuit inputs will produce low (zero-volts) outputs on the lower three circuits. The output stage of the first three circuits if inputs are open is controlled by pin B, which must be grounded for outputs low or connected to pin A (+ 5 volts) for outputs high. This last provision allows type 33 or type 35 current switching teletypes to be converted and wired ORed with modem interfaces. Pin B must be connected either to pin A or pin C: if it is left open, there may be crosstalk between circuits.

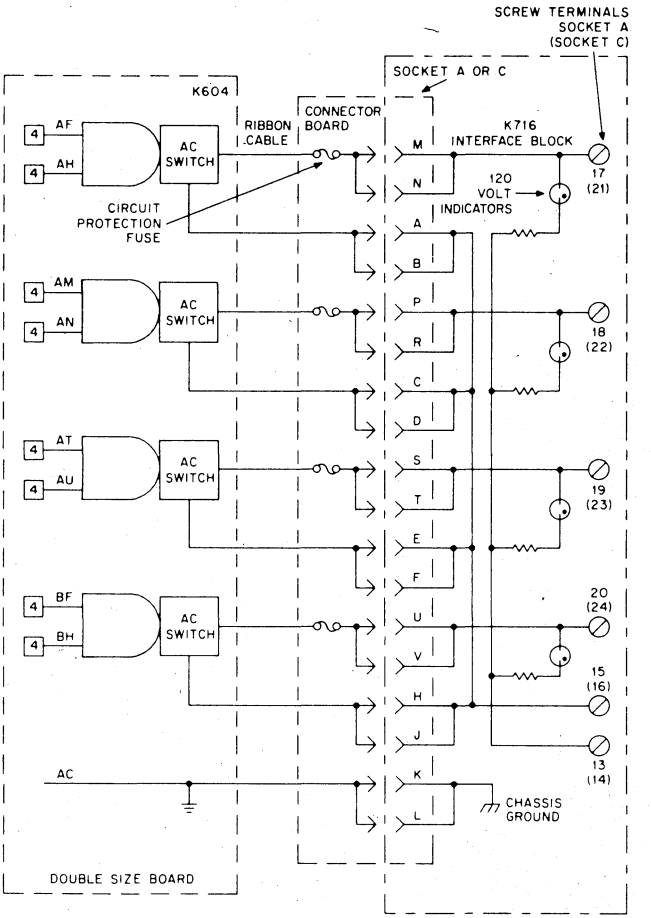
Please observe that noise and interference can enter a digital system through any wires that pass through a noise field. K596 modules should be located at the edge of the system, and communications wiring should not be allowed to lie close to logic wiring for more than a few inches.

K596 — $16

After the modules are flow-soldered, they undergo a visual inspection to insure that all solder points and runs are properly made. If needed, additional solder is added.

ISOLATED AC SWITCH
K604

K SERIES



Operating in conjunction with the K716 Interface Block, the K604 permits AC operated valves, solenoids, small motors, motor starters and the like to be controlled directly from K Series logic. Each circuit can handle up to 250 volt-amperes continuously. Total for any module, however, should not exceed 500 volt-amperes averaged over one minute. Ratings below include maximum horsepower based on use of Allen-Bradley type K_R motor starters. Less sensitive starters or relays may have significantly reduced capacity.

K604 — $82

Maximum Capacity, each K604 circuit (120 v AC lines)						
Condition	Continuous V.A.	Inrush V.A.	Motor Direct	Type K Starter	208/220 Max. H.P.	480/600 Max. H.P.
With Fuse	250	600	1/20 H.P.	Size 3	30	50
No Fuse	250	1800	1/10 H.P.	Size 4	50	100

Littelfuze® type 275005 fuses provide fault protection for the triac output circuits. The fuses are mounted by clips on the connector board for easy replacement. Without the fuses, short circuits will destroy the module. The no-fuse information above is for reference only, and operation without fuse protection cannot be recommended. Circuits cannot be paralleled to increase ratings.

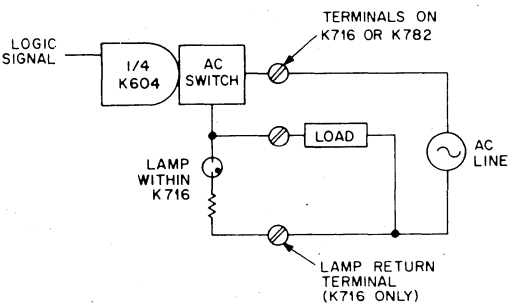
AC switch turnon takes place within 500 microseconds after input logic gate goes high. Turnoff takes place at zero crossings of the current. Maximum "off" leakage: 10 ma RMS at 140 VAC. Line voltage rating: 100 to 140 VAC, 50 to 60 Hz. Each triac output circuit has 400-volt breakdown rating. Shunt capacitor and shunt clipping devices inhibit false triggering on line transients.

Where very small devices such as pilot lamps, light duty relays, or AC input converters constitute the sole load, an auxiliary load such as a 12KΩ 2 watt resistor may be required to absorb sufficient holding current for full voltage output.

Two special precautions are made necessary by the presence of AC line voltages on the K604 module. First, always disconnect the ribbon cable connector before inserting or removing a K604 or an adjacent module, to avoid shocks or component damage. Second, W993 copper-clad boards ($4 each) should be installed between K604 modules and all other types except K508 or K644. **With the pin A connection cut away,** on either the board or the socket, the W993 copper clad board acts as an electrostatic shield. If this added interface protection is later found to be unnecessary, the sockets reserved for shield boards can be used to add logic features, modifications, etc. Refer to Construction Recommendations.

If desired, a K782 terminal board instead of the K716 may be used to obtain connections to field wiring. No indicators are provided by the K782, however.

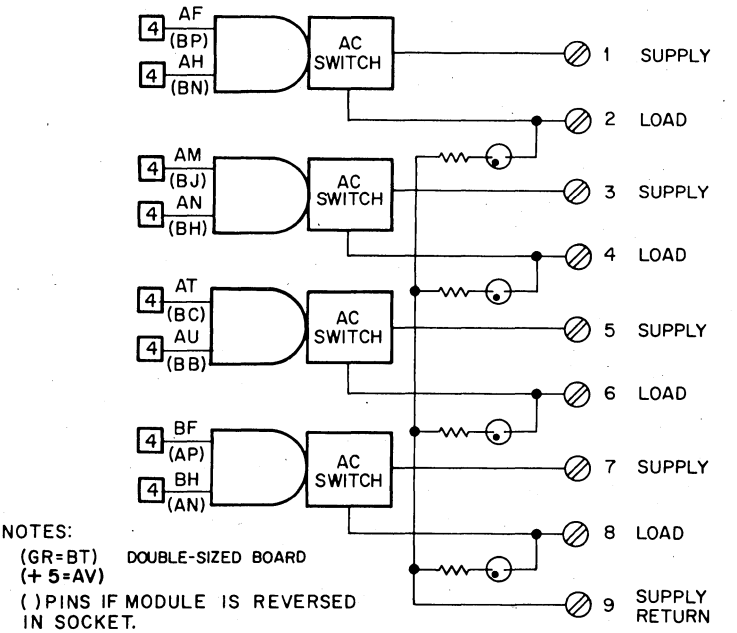
For 240 volt operation, refer to the application note on this topic.



K604 CIRCUIT IN USE

ISOLATED SWITCH
K614

K SERIES

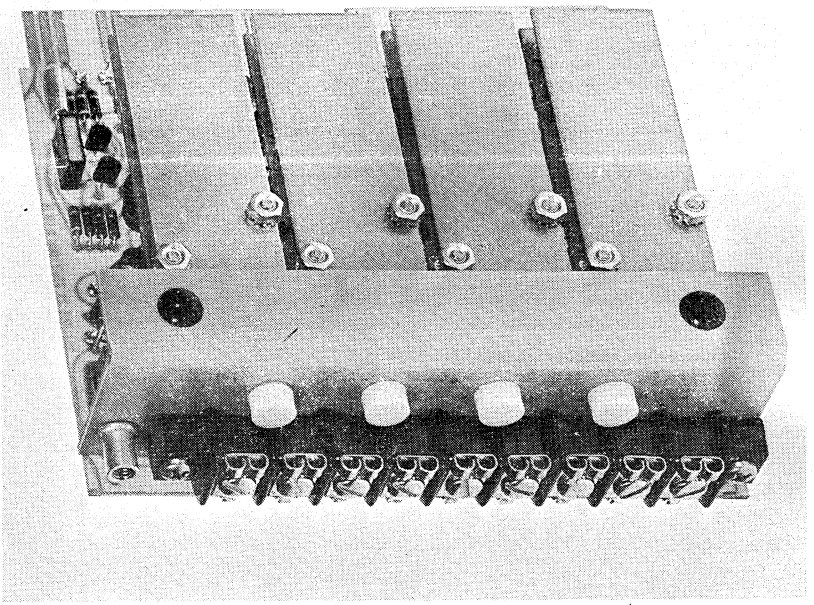


K614 AC SWITCH

This module uses the K604 circuit and behaves in most respects the same. However, the K614 is designed to fit a K724 or K725 interface shell. Accordingly the K614 has built-in clamp-type terminals for wires to size 14, Neon indicators, and output ratings boosted to 500 VA per circuit by the larger heat sink area available in this configuration. However, total for any module must not exceed 750 volt-amperes averaged over any one minute.

See Applications Notes for information on 240 volt operation.

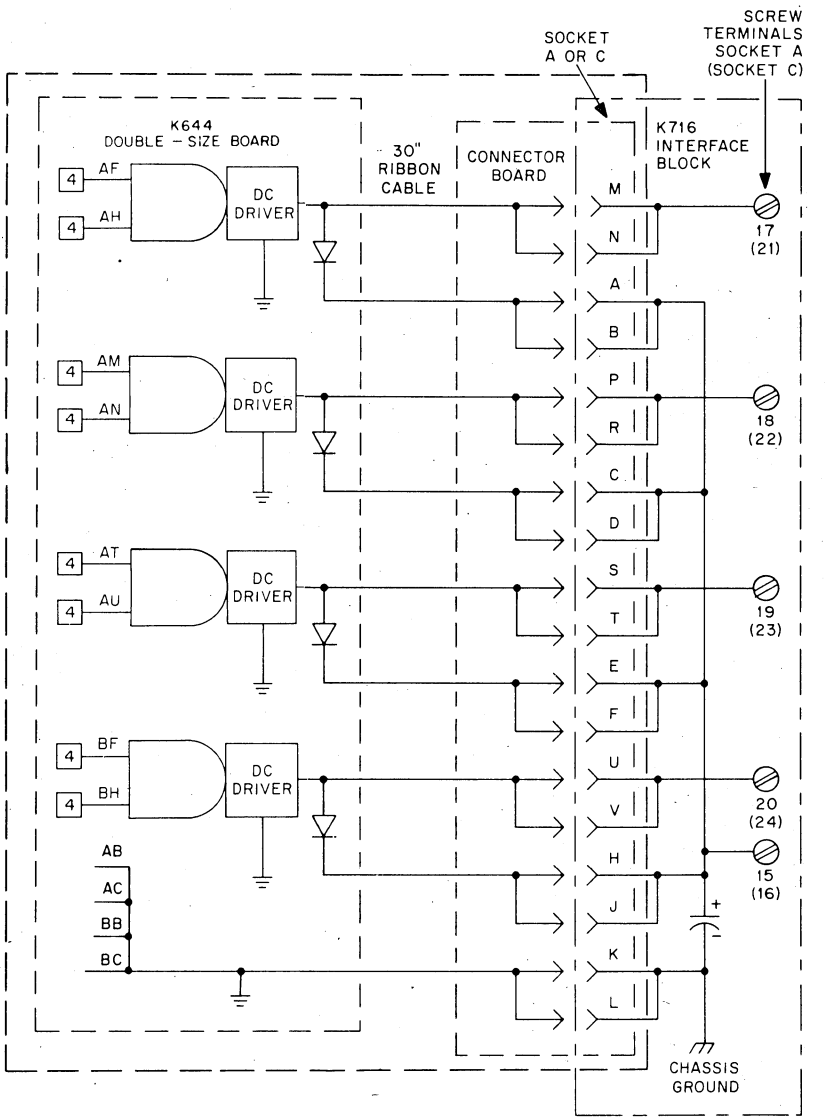
K614 — $88



K614 TERMINALS AS VIEWED LEFT TO RIGHT ARE NUMBERS 1 THROUGH 9

DC DRIVER
K644

K SERIES



K644 — $66

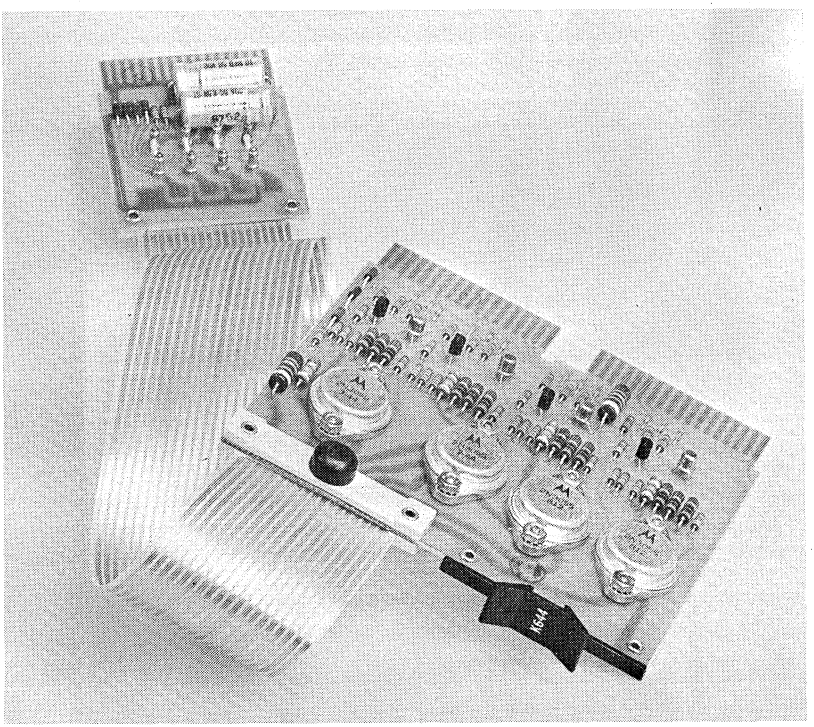
Operating through the K716 Interface Block, the K644 DC Driver permits stepping motors, dc solenoids, and similar devices rated up to 2.5 amperes at 48 volts to be driven directly from K series logic. Built-in clamping diodes protect switching transistors from transient over-voltage.

Total output circuit current for the K644 module must not exceed 4 amperes averaged over any 1 minute period. The ribbon connector should be unplugged before inserting or removing a K644 module.

Moving the parts of a magnetic device changes the winding inductance. To equalize magnetic field turnoff and turnon times, the ratio of inductance to total circuit resistance must be held constant. This demands more resistance in the circuit during turnoff, when the inductance is higher. Resistance may be inserted between K716 terminal 15 (or 16) and the load supply to achieve this, provided the K644 output voltage will not exceed 55 volts. Whether resistance is added or not, these clamp return terminals must be connected to the load supply to protect the module from overvoltage during turnoff.

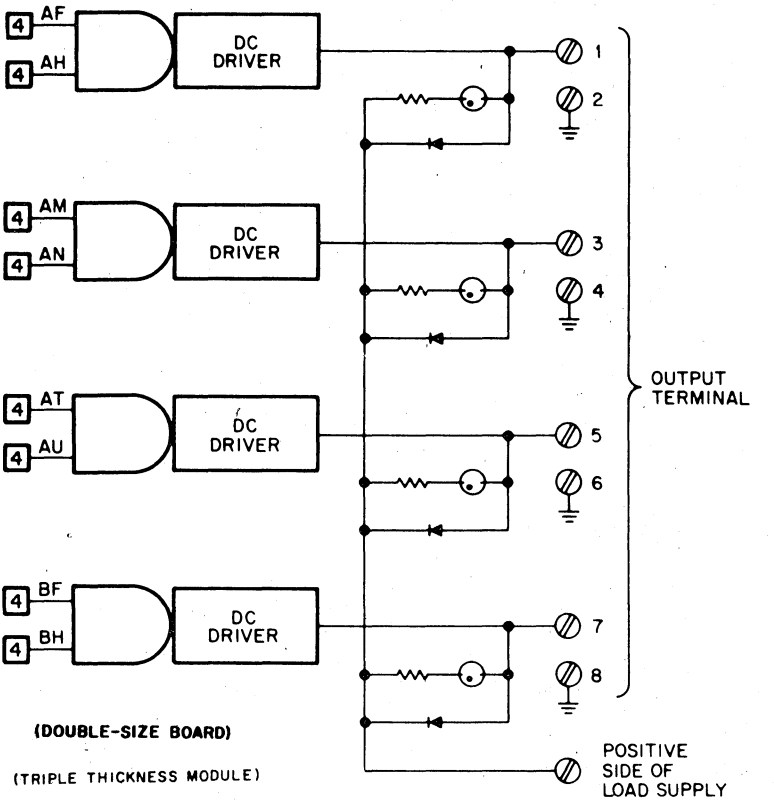
The K644 may be used with a K782 instead of a K716 to obtain the screw terminals needed for connecting heavy duty field wiring.

See applications section for logic diagrams of several stepping-motor applications.



DC DRIVER
K656

K SERIES



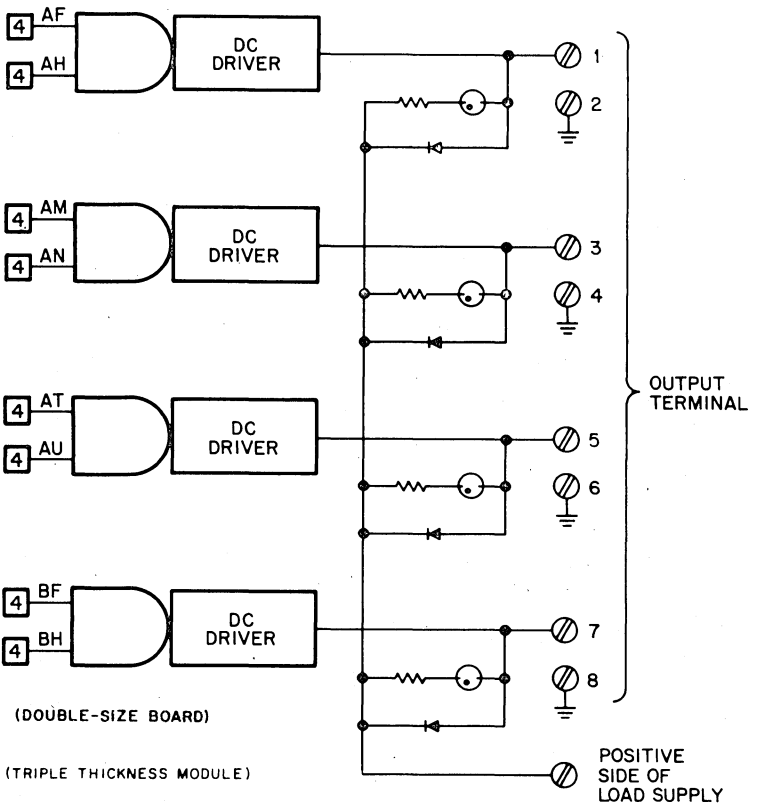
K656 250 VOLT DRIVER

Each circuit of this versatile driver can deliver up to 1 ampere at up to 250 volts, making it ideal for driving heavy-duty brakes and clutches or for high speed operation of other inductive loads. Like the K578 and K614, this module has integral clamp-type terminals and neon indicator lamps. (Lamps are effective only at 90 volts and above.) This driver module is designed to be used with K724 or K725 interface shells. Positive side of load supply must be connected to protect output transistors from damage during turnoff transient.

K656 — $80

DC DRIVER
K658

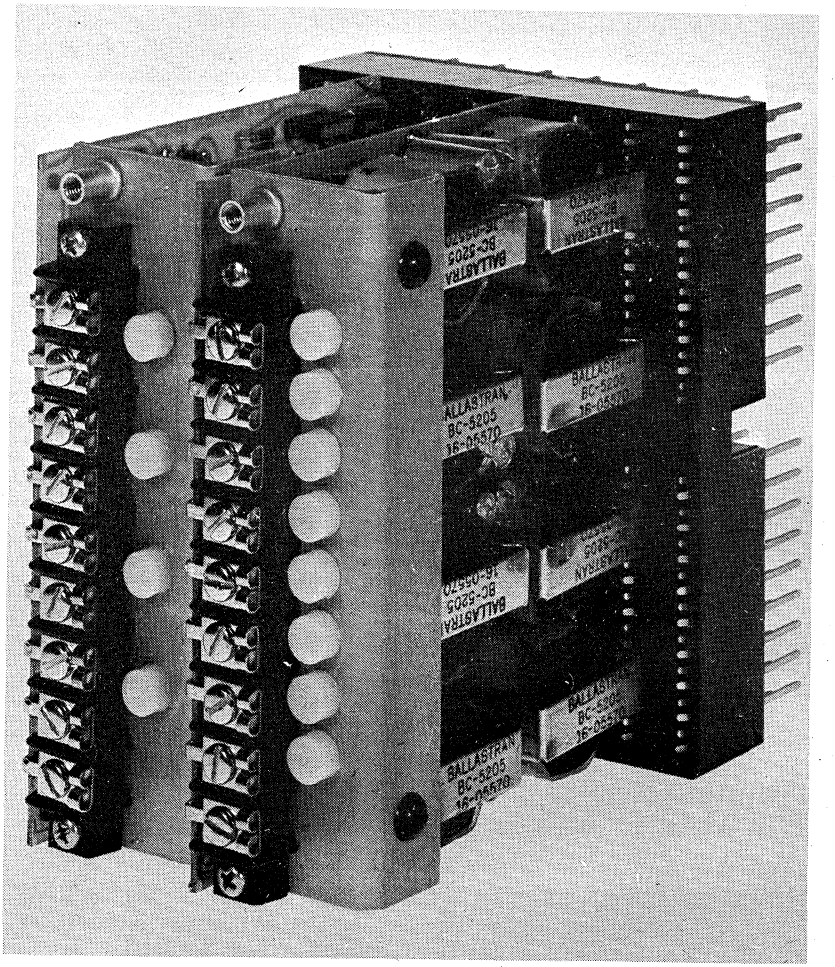
K SERIES



K658 4 AMP DRIVER

Each circuit of this versatile driver can deliver up to 4 amperes at up to 125 volts. Like the K578, K656 and K614, this module has integral clamp-type terminals and neon indicator lamps. (Lamps are effective only at 90 volts and above.) This driver module is designed to be used with K724 or K725 interface shells. Positive side of load supply must be connected to protect output transistors from damage during turnoff transient.

K658 — $128

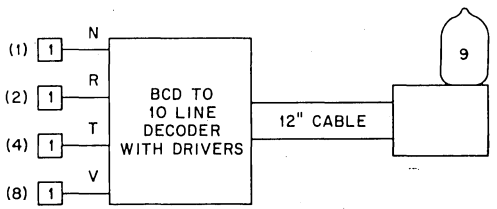


K656 AND K578

Modules with terminal strip output connections may be used in the K724 and K725 interface shells or they can be used in the K943 mounting panels. K578, K614, K656, and K658 are all triple thickness modules.

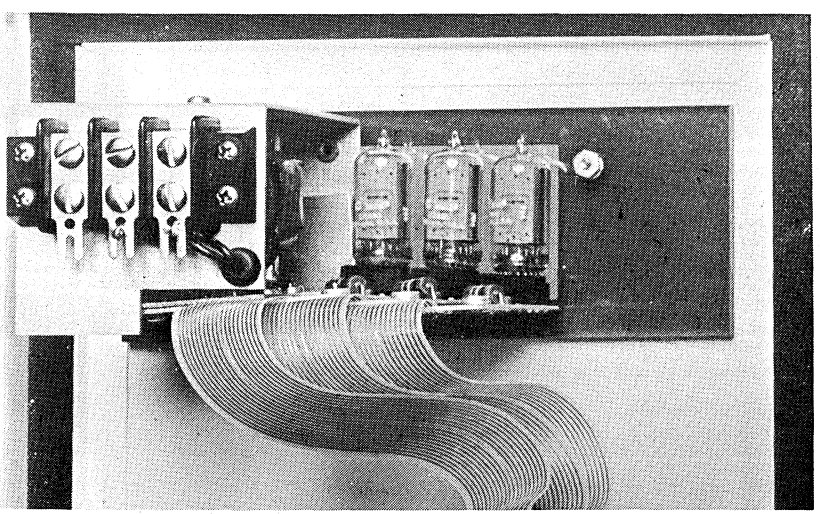
DECIMAL DECODER AND NIXIE DISPLAY
K671

K
SERIES



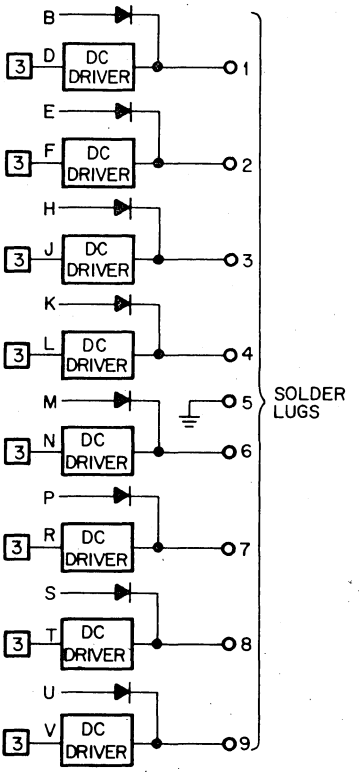
This module has two parts separated by a 1-foot ribbon cable. One part plugs into any module socket, the other contains a side-viewing Burroughs type B-5440 long life NIXIE glow tube on a mounting board. Four connections to corresponding module socket pins of a K210 or K220 binary-coded decimal counter completes the input wiring. The display tube board attaches with two screws to a K771 supply for both mechanical mounting and power supply electrical connections. Displays up to 6 digits long can be stacked on each K771 supply. Stacked digits have 0.8" mounting centers. See Construction Recommendations before assigning module locations.

K671 — $43

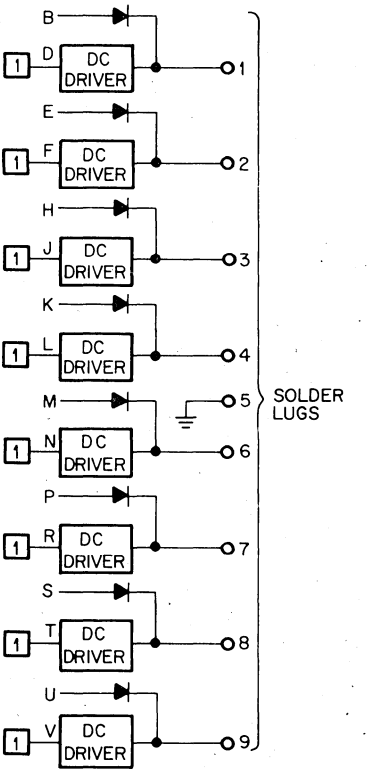


LAMP DRIVERS
K681, K683

K SERIES



K681 LAMP DRIVER



K683 LAMP DRIVER
(DOUBLE-SIZE BOARD)

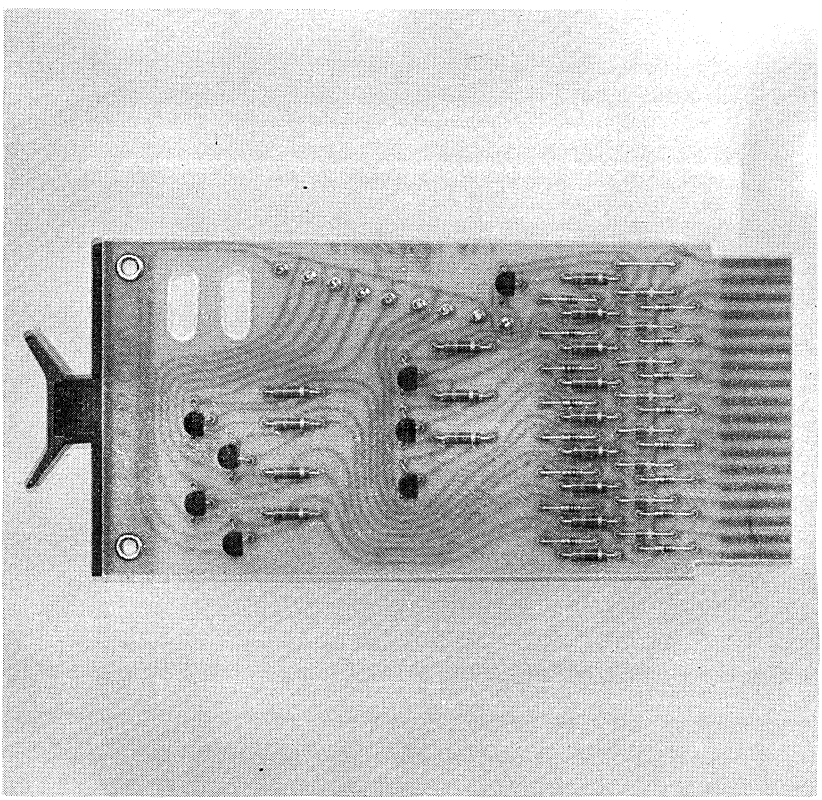
These eight-circuit modules drive external loads through 9-conductor cable soldered to split lugs at handle end by user. Strain relief holes, prepunched in board. Ground input to turn off, +5V to turn on.

Pin connections via diodes to outputs facilitate production automatic module testing while isolating system wiring from high voltages. Circuits are not slowed, and these connections are not recommended as output tiepoints unless exceptional care is taken to prevent noise and damaging voltages from degrading system reliability. (See Fixed Memory application note.)

K681 — $15
K683 — $30

MODULE TYPE	OUTPUT RATINGS		
	RESISTIVE	INDUCTIVE	INCANDESCENT LAMPS
K681	18V, 30ma	18V, 30ma with suppression diodes (K784)	Lamps rated 18V, 40ma operated at 12V to reduce current to 30 milliamperes.
K683	55V, 250ma	55V, 250ma with added suppression diodes (K784)	Lamps rated 40ma, to 48V; Lamps rated 60ma, to 28V; Lamps rated 80ma, to 18V; Lamps rated 100ma, to 12V

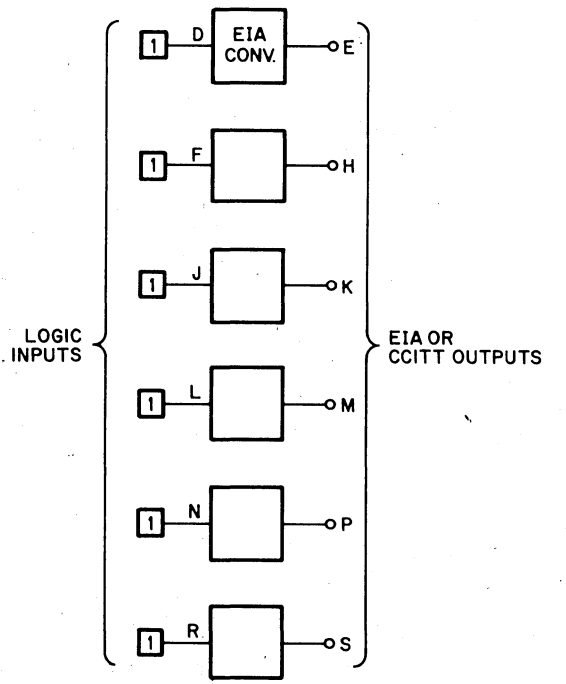
Note greatly reduced ratings on tungsten loads. Lamp filaments draw typically ten times more current at turnon than when hot, resulting in very high transistor dissipation if supply voltage is high. Series current limiting resistors or shunt preheat resistors could be used to limit surge in certain cases, but ratings above assume this would be awkward or impractical.



K681 MODULE

EIA OUTPUT CONVERTER
K696

K SERIES



EIA OUTPUT CONVERTER K696

This bipolar non-inverting driver converts standard logic levels to either the American EIA or the European CCITT standard signals for data transmission. Power can either be 6.3 VAC±10% 60Hz on pin B for EIA levels (at least ±5 volts) or 9.0 VAC±10% 50Hz on pin B for CCITT levels (at least ±6 volts). Limited output current capability results in risetimes of several microseconds for capacitive loads of a few thousand picofarads, limiting the maximum baud rate to 5K baud. One ampere of AC can supply up to 32 K696 modules. Keep AC leads short to maintain voltage.

Please observe that noise and interference can enter a digital system through any wires that pass through a noise field. K696 modules should be located at the edge of the system, and communications wiring should not be allowed to lie close to logic wiring for more than a few inches. A high impedance probe may be used to monitor the half-wave rectified and filtered negative internal supply at pin T (5 KΩ series resistance).

K696 — $44

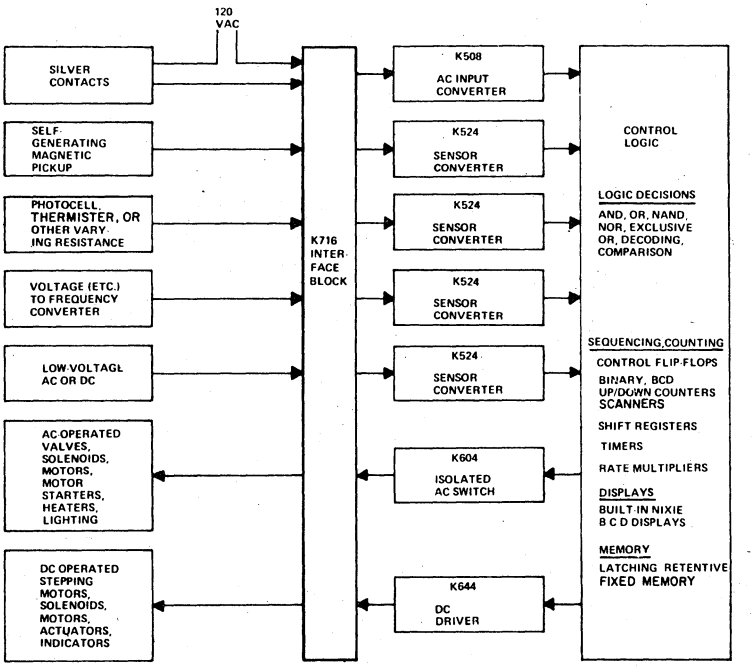
In addition to being a set of noise-immune logic, the DIGITAL K Series offers a versatile system of modular instrumentation and control hardware. On the following pages you will find a variety of equipment for mounting, wiring, powering, etc. The table below may help you get acquainted.

FUNCTION	PRODUCT	
Accessories for Interface Modules (K5XX, K6XX)	K716	Interface Block
	K724	Interface Shell, Power wiring only
	K725	Interface Shell, Prewired for scanning
	K782	8 Terminals
	K784	8 Terminals with Diodes
Power	K731	1 Amp Regulator
	K732	2 Amp Slave Regulator
	K741	2 Amp Transformer
	K743	3 Amp Transformer with Auxiliary Winding
	K771	NIXIE Supply
Mounting Hardware and Connectors	K940	Mounting Foot for K941
	K941	Mounting Bar
	K943	64 Module 19" X 5¼" Mounting Panel
	K980	End Brackets
	1907	Hold-Down and Cover
	H001	Cover Supports
	H800	8-Connector Block
	H802	Single Connector

INTERFACE BLOCK
K716

K SERIES

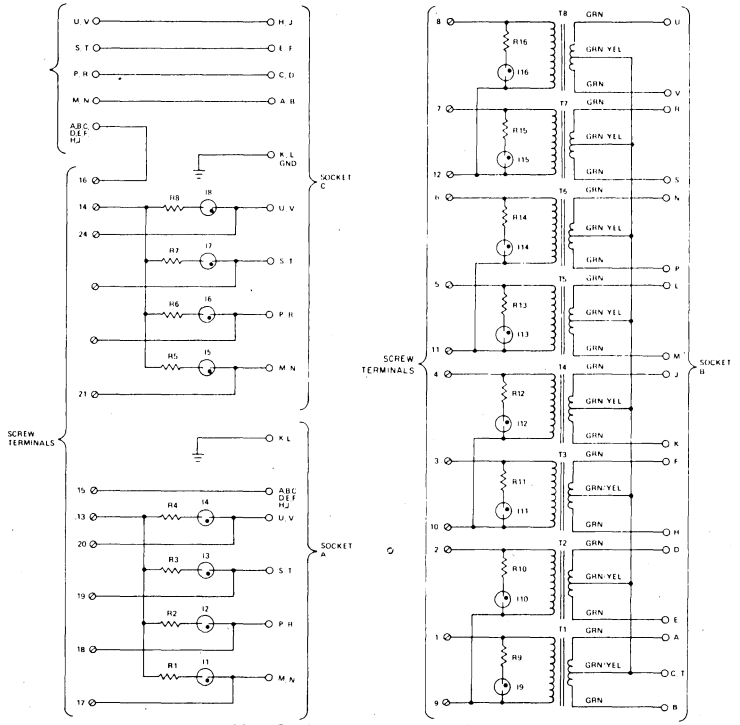
An important hardware feature of the K Series system is the K716 Interface Block, which permits field wiring to be installed at ordinary screw terminals by electricians. The logic modules interconnect to the K716 by plug-in ribbon cables.



TYPICAL CONTROL APPLICATIONS FOR K SERIES MODULES INTERFACED BY K716

Contacts: Ordinary silver contacts of the kind found in limit switches, pressure switches, and pushbuttons work best when operated with healthy levels of both line voltage and load current. The sparking that results prevents buildup of contact surface contamination. To assure reliable switching, isolation transformers in the K716 provide a reactive load for switched 120 vac pilot voltages. The K508 AC Input Converter ignores contact bounce. Hash filters in the module, and attenuation in the isolation transformer built into the K716, reduce electrical noise. Built-in indicators permit quick maintenance checks.

The K716 Interface Block serves as an interconnection interface for those K Series modules that communicate with external equipment. External field wiring terminates at a 24-terminal screw connection block that accepts plain stripped wire up to 14 gauge. No separate crimped or soldered terminals are required.



K716 INTERFACE BLOCK SCHEMATIC

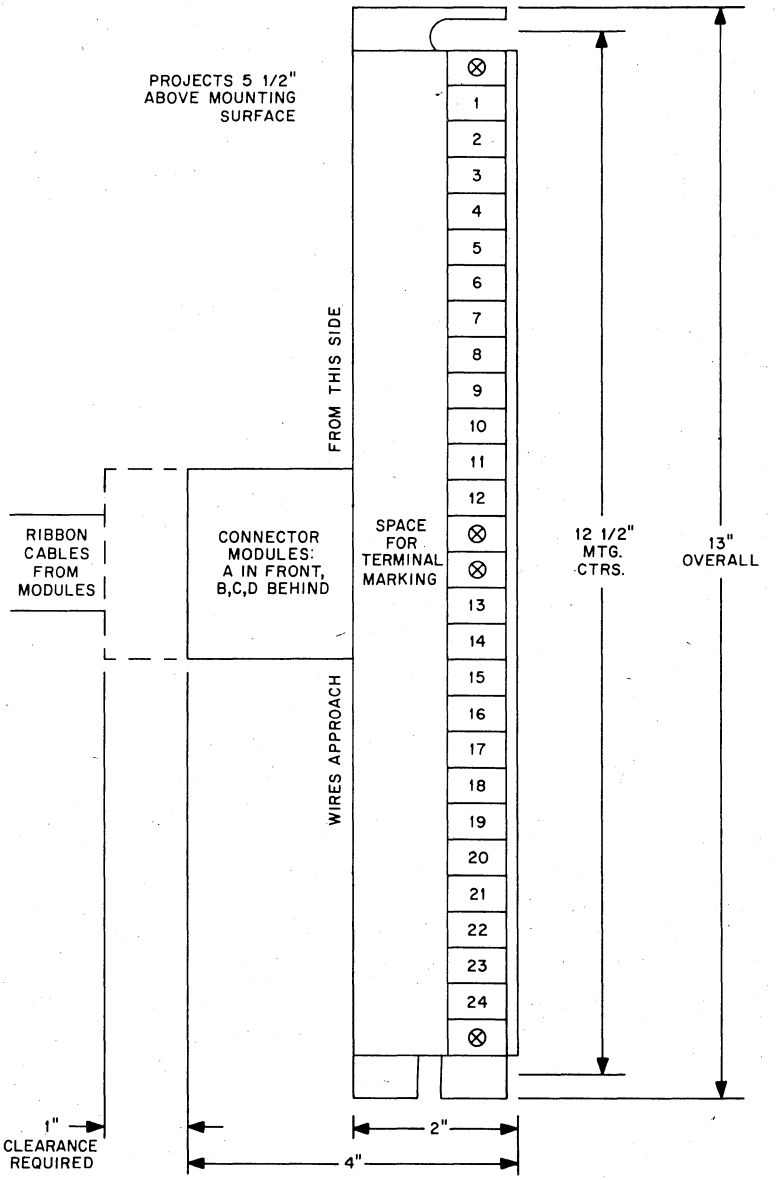
Ribbon cables from the K Series interface modules connect to printed circuit board sockets on the K716. This allows the K716 terminal block to mount on the rear panel of a NEMA enclosure for the convenience of electricians, while the digital system itself mounts on the door for easy access to both modules and logic wiring. The ribbon cable makes neat, simple wiring layouts and easy flexing at the hinge.

The three sockets in the K716 terminal block contain the same module connector system used for the modules themselves, permitting quick disconnect of the entire logic system without affecting reliability. This arrangement, together with the K940-K941 mounting hardware, allows initial checkout of control systems away from the site, as well as minimizing downtime in case of failure. (See Construction Recommendations.) The cable sockets have the same reliable gold contacts as K Series module sockets.

Socket B, for use with the K508 AC input converter, is fed by eight isolation, stepdown and contact loading transformers contained within the aluminum shell of the K716. The transformer primaries receive 120-volt pilot signals from external contact closures. Each input is monitored by a neon indicator.

Sockets A and C are for use with K524, K604, and K644. Neon indicators are provided to monitor the outputs of the K604 Isolated AC Switch module.

K716 — $90



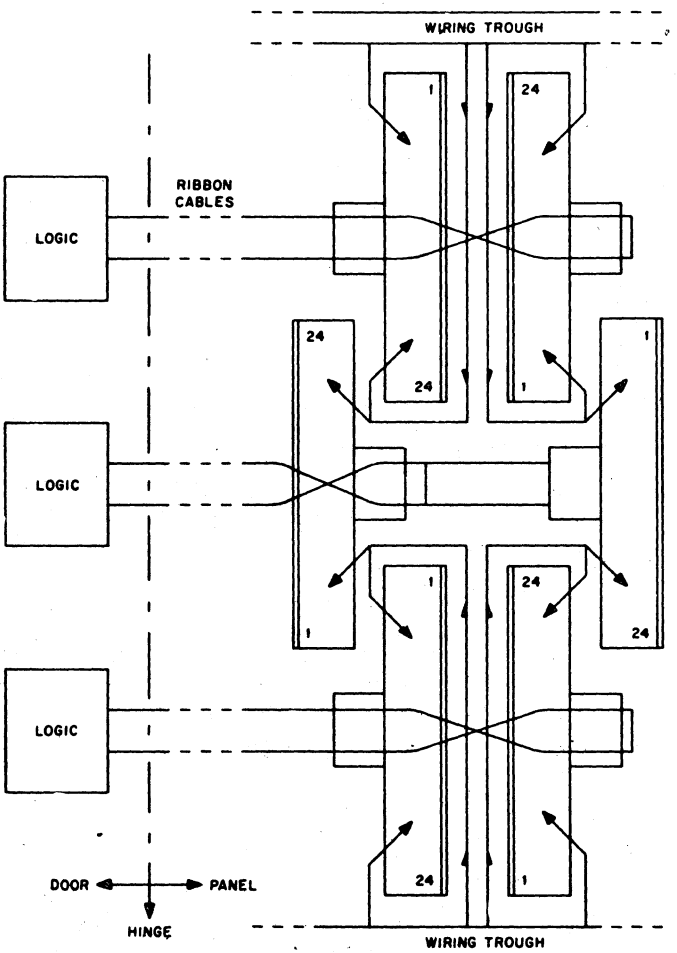
K716 INTERFACE BLOCK
FRONT VIEW

The drawing above shows approximate dimensions of the K716. Mounting slots clear no. 10 screws and allow compensation for mounting screw location tolerances. See first Application Note "Construction Recommendations."

All neon indicators are located within the K716 shell, visible at the rear of associated screw terminals.

Socket D, normally terminated by a shorting plug runs all return lines from connector C to a common point. If the shorting plug is removed, independent wiring of connector C return leads for K524 or K604 modules is possible. A W033-06F-W033 cable connector ($15) must be installed between socket D and socket A. An extra 2-inch clearance is required by this connector board. Independent wiring provides connections for four two-wire circuits instead of 8 circuits with bussed returns.

Below is a recommended mounting pattern for combining many interface blocks. This pattern can be extended provided the 30" reach of ribbon is not exceeded.



K716'S IN INDUSTRIAL ENCLOSURE

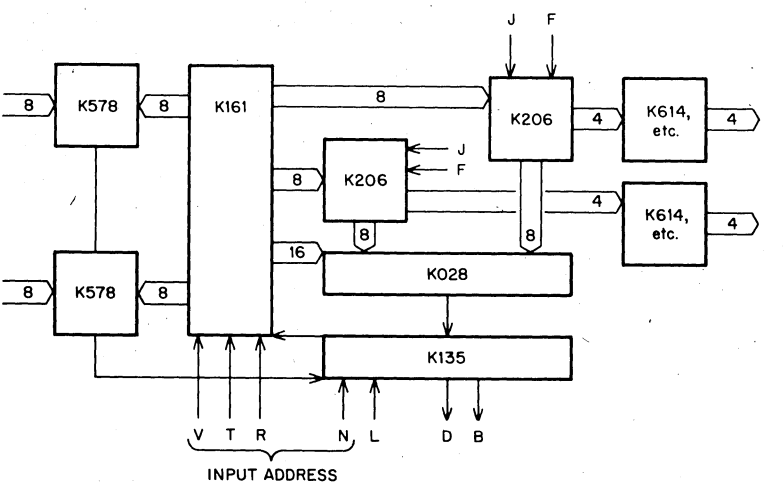
INTERFACE SHELLS
K724, K725

K SERIES

Unlike the K716 interface block pictured on the next page, these shells do not contain any electronic components. Instead, they provide the connectors and the mechanical support for self-contained interface modules K578, K614, K656, and K658. Up to four such modules may be installed, with eight module sockets remaining between them for simple logic functions. Convenient wiring channels are obtained between units if they are mounted on 12" centers vertically and 6" centers horizontally. This way a total of up to 32 input converters and 16 output converters fits in one square foot of panel space, along with up to 16 logic modules.

The K724 provides only logic power connections between sockets. It is primarily intended for very simple logic systems or for large systems where all input and output logic levels are connected to a separate logic unit by connector cables.

The K725 uses a printed backplane to make most of the connections required in a remotely scanned system. In this type of system, a few address lines transmitted to the interface shell on a single connector cable are decoded by a K161 decoder within the shell either to sample one particular K578 input, or else to set or clear a K206 flip-flop which in turn controls the state of one of the output converters. This type of system is convenient to use with a computer, and also lends itself to situations requiring remote contact sensing and switching at several scattered locations.



K725 Signal Flow

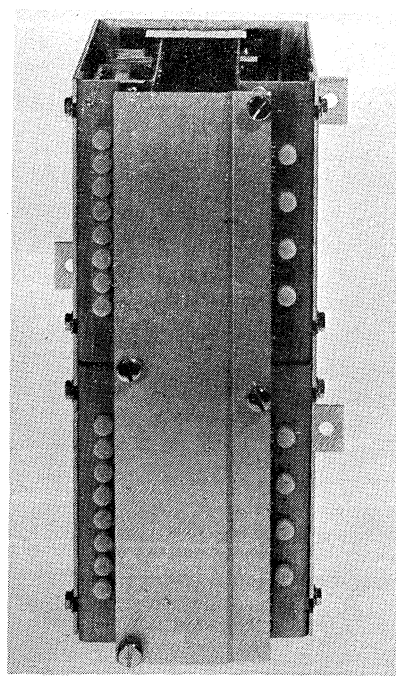
K724 — $55
K725 — $82

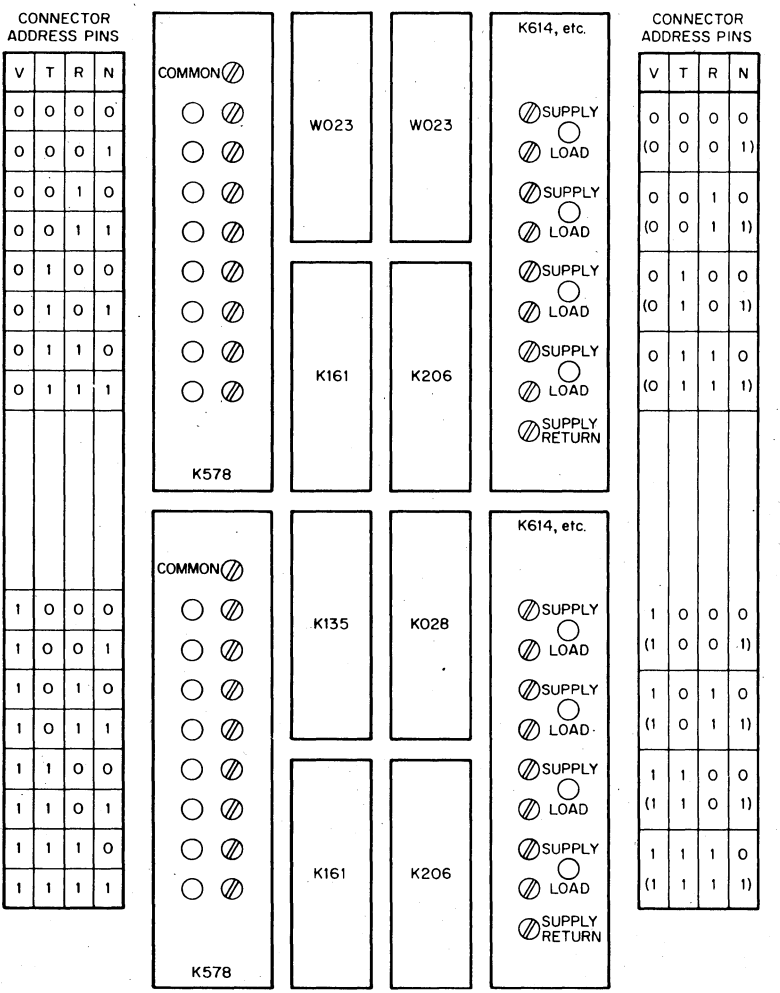
K725 CONNECTIONS

AT W023 SOCKETS

K206 Returns:	Low if addressed output flip-flop holds a "1."
K578 Returns:	Low if addressed input has 120VAC applied.
K206 Enable:	If high, clears addressed output flip-flop or, if pin N is high, sets the flip-flop.
K206 Clear:	If low, clears all output FFs.
K135 Enable:	If low, forces both K206 return and K578 return high to allow wired OR of returns from up to sixteen K725 assemblies.
Address, Pin N:	Least significant bit of input address; if K206 Enable is high, selected flip-flop forced to the state of pin N. For sampling the K206 state, pin N must be low because there are only 8 flip-flops.

A	+5V power
B	K206 returns
C	Ground
D	K578 returns
E	spare
F	K206 enable
H	spare
J	K206 clear
K	spare
L	K135 enable
M	spare
N	Address, LSB
P	spare
R	Address
S	spare
T	Address
U	spare
V	Address, MSB



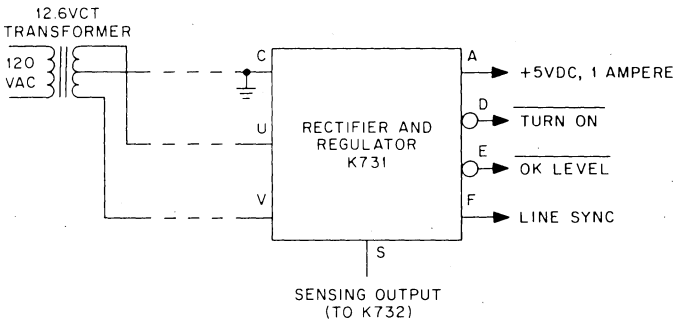


K725

INTERFACE SHELL

SOURCE MODULE
K731

K
SERIES



(TRIPLE THICKNESS MODULE)

The K731 supplies +5 volt dc power to pin A of all K Series modules and provides several specialized once-per-system control functions. Any source of center-tapped 12.6 v (50 or 60 Hz) allows the K731 to deliver up to 1 amp dc, which is sufficient to operate most typical control systems of up to 32 modules. The K731 is short-circuit proof.

This module is normally plugged into one of the innermost sockets on a K941 mounting bar, where its large components occupy space otherwise unused.

The turn-on output goes to ground during the power-up transient, and remains at ground until after the supply voltage has fully reached its quiescent value. It may be used to initialize flip-flops to a known starting condition.

The OK level output goes to ground when the supply voltage reaches 90% of its final value, and returns positive when less than 90% of full voltage is available. It is normally used as an enabling input to the K273 Retentive Memory module.

The line sync output allows a K113 or K123 gate to switch in synchronism with ac supply zero-crossings. This permits the line frequency to drive a real-time clock, or serve as the standard in a phase-locked loop with K303 timers, where higher frequencies must be synchronized with the line. Line sync fan-out is limited to 1 ma (for high fanout, use K113 or K123 for distribution). None of the K731 logic outputs may be used to obtain the OR function, and they may not be wired to any other output.

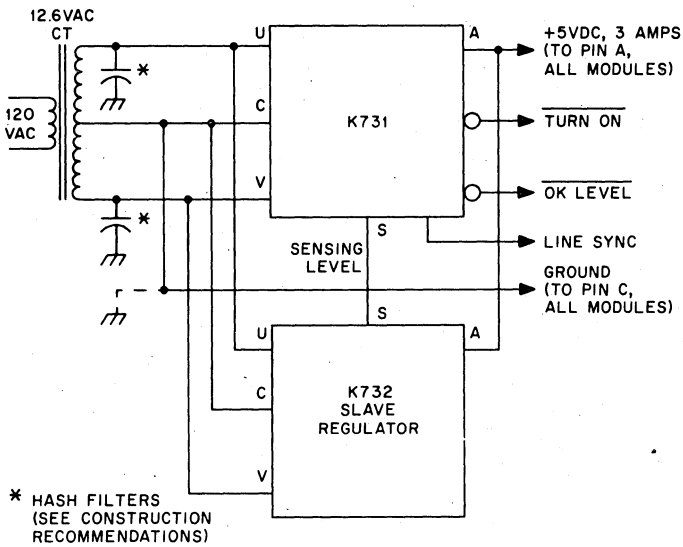
K731 delivers up to 1 ampere when used with a 12.6 volt transformer rated for 105-130 volt line. For 5% input voltage reduction (12.0 V transformer or 100 volt line) the output current capability decreases 10%. Output voltage temperature coefficient is typically minus 0.1%/°C. See summary of module current consumption following K732 data, and K741-K743 transformers on following pages.

See power supply section for photos.

K731 — $24

SLAVE REGULATOR
K732

K SERIES



(FOUR MODULES THICK)

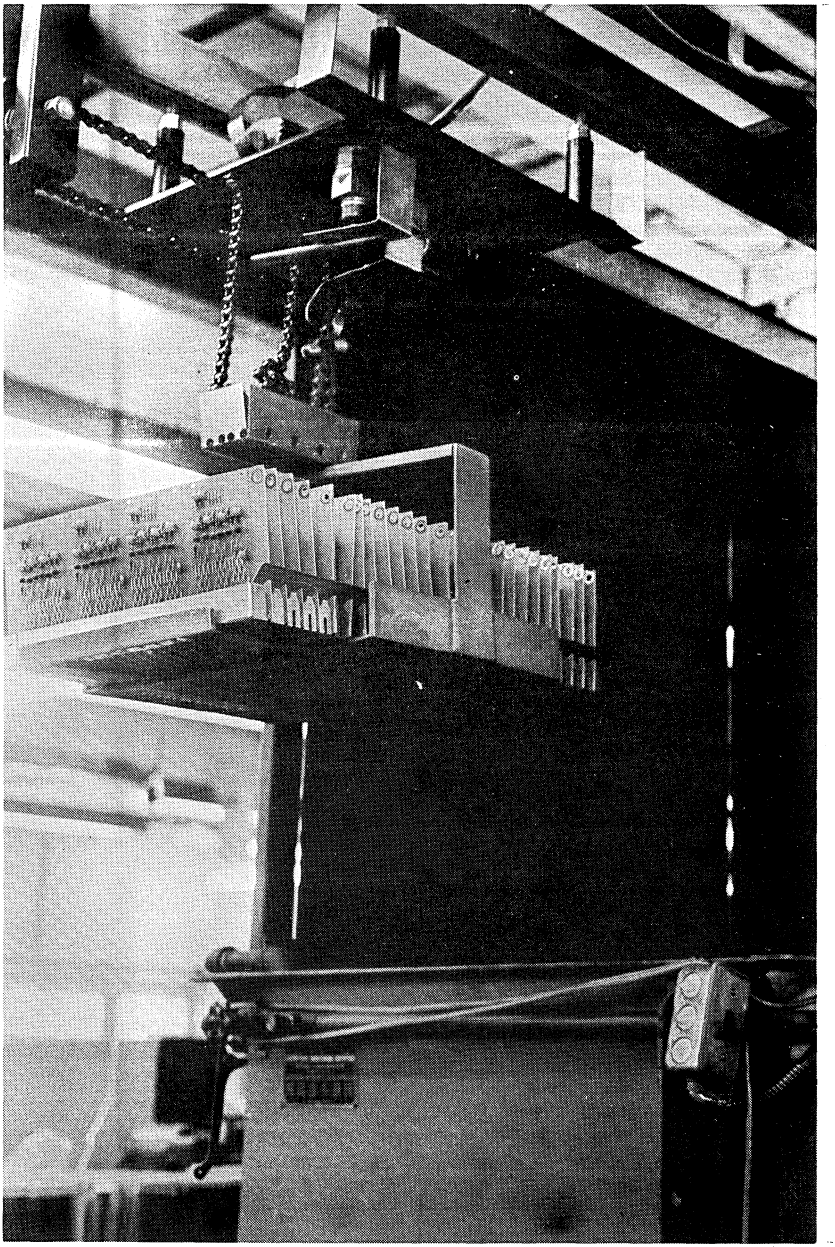
This module is normally tied to corresponding pins A,C,S,U, and V of a K731 Source. For each unit of current emitted by the K731, the K732 emits two. Up to three K732 slaves can be controlled by a single K731 for a total system current of 7 amperes.

In high-current systems, use short heavy wires for transformer secondary connections. Loss of 5% of secondary voltage in either ground return or transformer output leads will reduce regulator current ratings more than 10%. Tabs near the handle end of the K732 may be connected to K741 or K743 transformers by using convenient 914 Power Jumpers. Then by wiring pins U and V to corresponding pins on K731, AC connections are provided through the K732 to the source module. To avoid loss of regulation, do not connect a K732 until enough modules have been plugged in to draw a reasonable current (several hundred milliamperes).

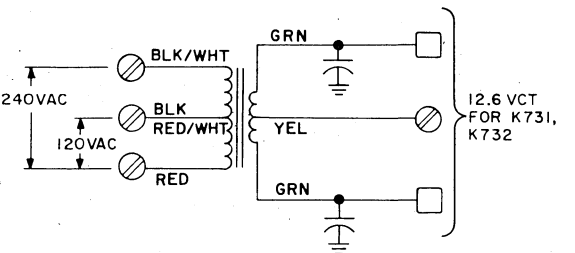
For self contained low-ripple supplies see H710 and H716.

CAUTION:
These modules lack overvoltage protection, and may damage M-Series modules in case of a supply failure. Not recommended for use with M series modules.

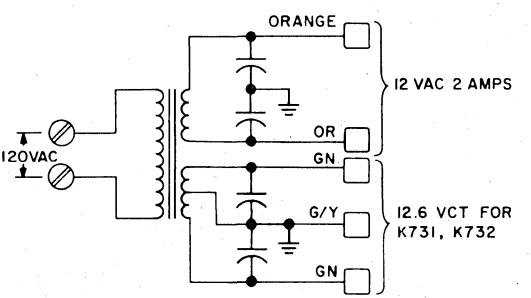
K732 — $27



After all the components have been attached to the board, the module is degreased to remove contaminants in preparation for flow soldering.



K741 TRANSFORMER WITH FILTER



K743 TRANSFORMER WITH FILTER

These hash-filtered, 50/60 Hz transformers supply K731 Source and K732 Slave Regulator modules. The K743 also provides an auxiliary winding for use with K580 Dry Contact Filters and K681 or K683 Lamp Drivers (requires additional bridge rectifier). Type 914 Power Jumpers are convenient for connecting to tab terminals on these transformers and on the K732 and K943. Both transformers have holes at the corners of the chassis plate for mounting on K980 endplates:

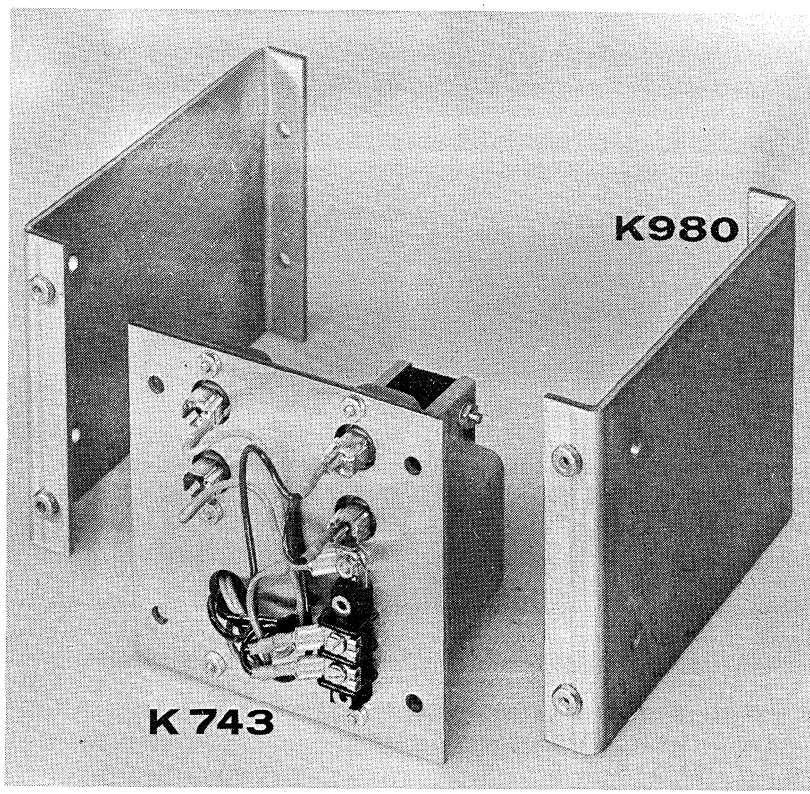
	PLATE DIMENSIONS	HOLE CENTERS	MATCHING K980 Ctrs.
K741	3½" x 5"	2½" x 3⅜"	2½"
K743	5" x 5"	4" x 3⅜"	4"

The K741 is sufficiently light in weight to be mounted on one side only, as at the end of a K943 mounting panel.

The table below shows how to obtain various currents. Line voltages within ±10% from nominal and short, heavy secondary wires are assumed. One K731 is required in each case.

60 Hz	50 Hz	K732	TRANSFORMER
0.1-1A	0.1-0.8A	0	K741 or K743
0.5-2A	0.4-1.6A	1	K741 or K743
1-3A	0.8-2.4A	1	2 K741s or K743
2-4A	1.6-3.2A	2	2 K741s or 2 K743s
3-5A	2.4- 4A	2	3 K741s or 2 K743s
4-6A	3.2-4.8A	3	3 K741s or 2 K743s
5-7A	4-5.6A	3	4 K741s or 3 K743s

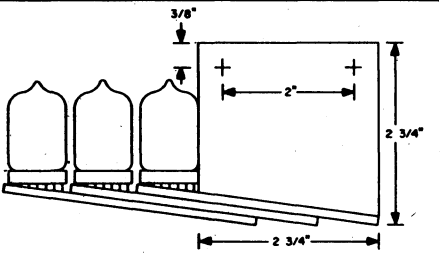
K741 — $22
K743 — $38



K743 WITH K980

DISPLAY SUPPLY
K771

K SERIES



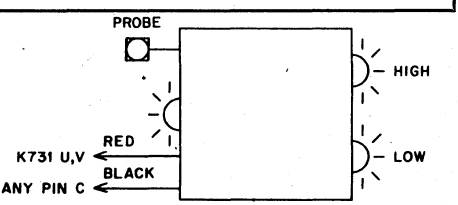
(SHOWN WITH 3 K671'S)

Shown above from the viewing side, the K771 supplies power and a convenient two-screw mounting for up to 6 K761 display tubes. Display tubes are stacked to the left, the first tube board being attached to the K771. The second tube board attaches to the first, and so on. Board mounting screws provide both mechanical mounting and electrical power connections. The two panel mounting screw locations dimensioned above have no. 6 steel threaded inserts. Several 1" holes using a standard chassis punch may be cut on 0.8" centers for viewing display tubes. To seal opening against dust, a 3" by 3-6" piece of Lucite® or Plexiglas® may be assembled between display and mounting surface. Power 120 VAC enters the supply from a terminal strip at the rear. Total depth behind mounting surface: 4".

K771 — $26

TEST PROBE
K791

K SERIES



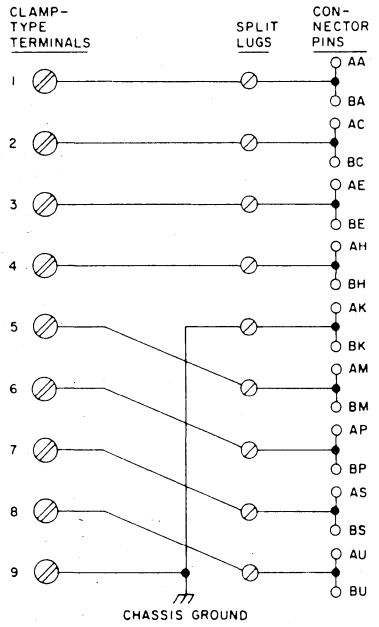
K791 TEST PROBE

This pocket test probe contains two pulse-stretching lamp drivers for visual indication of both transient and steady-state conditions. Neither indicator lights on an open circuit. A built-in test point illuminator adds convenience. The probe introduces negligible loading of the point under observation. The black wire connects to any pin C. The red wire gets ac power from the system supply transformer, pin U or V of K731. Probe is hollow and fits unwrapped end of H800W pins for hands-off use if desired.

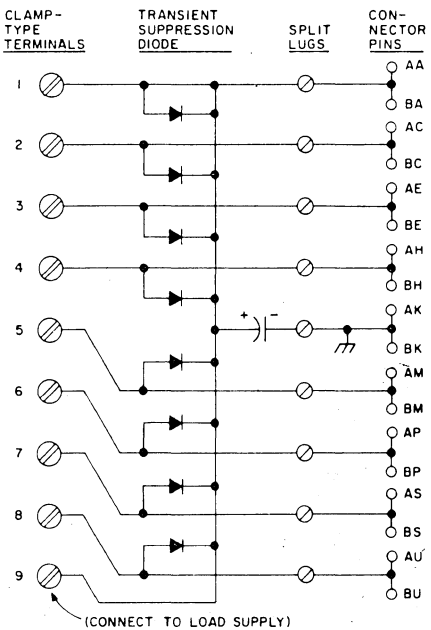
K791 — $27

TERMINALS
K782, K784

K SERIES



K782



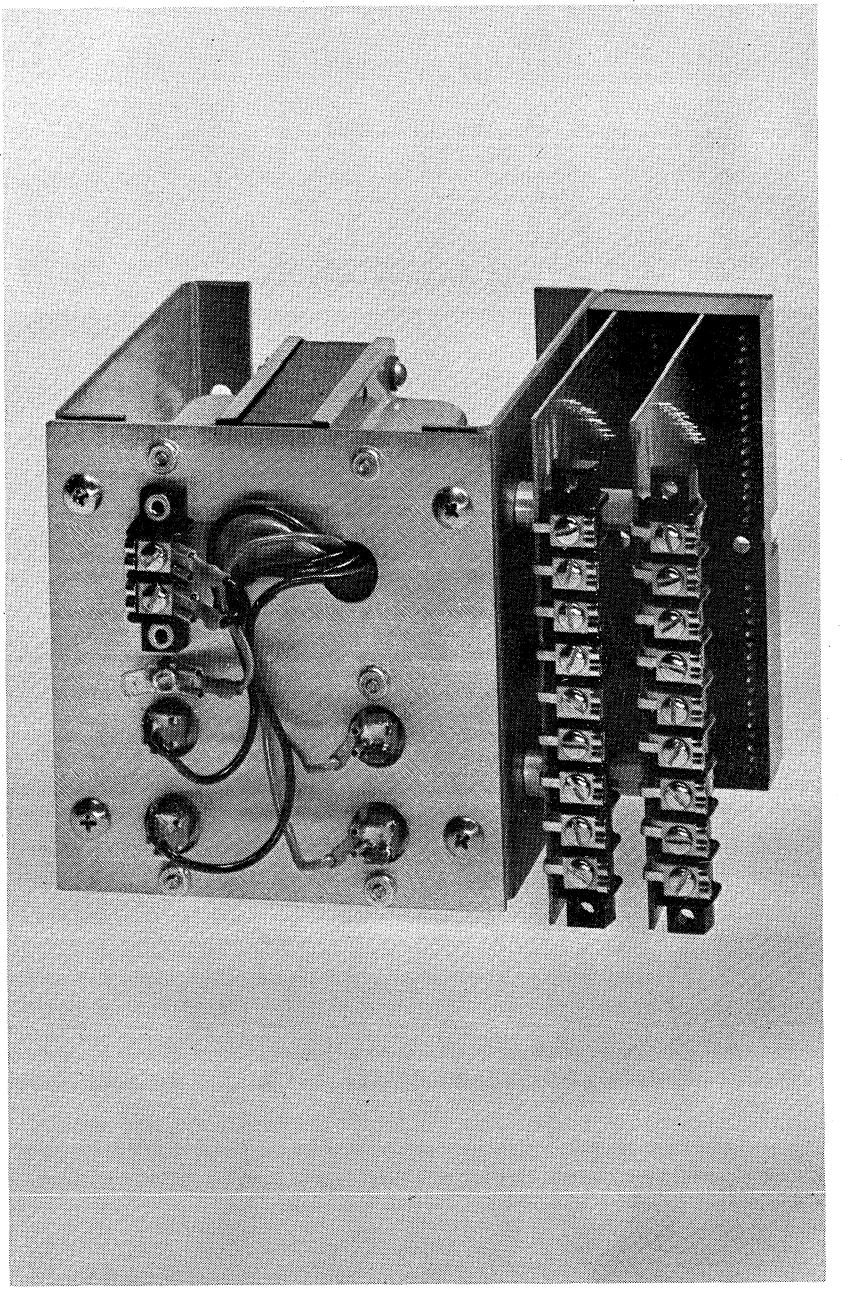
K784

These two double size modules offer an alternative to the K176 for obtaining field wiring connections in K series systems. The K782 has straight-through connections for use with K524, K580, K604, or K644 modules. The K784 includes 60 v clamp diodes for protection of K681 or K683 modules driving inductive loads. Strain relief holes and split lugs on both boards adapt them for such modules as K580 and K683 where 9-conductor ribbon or individual wires will be used.

Connector pins are also provided, so the connector board of types like K524 or K604 can be plugged into a shared H800-F block and bussed connections used.

The photo at right shows one way that these modules may be mounted, by bolting through the holes provided and mounting on K980 brackets. The attachment of a K743 transformer to the K980 is also shown here.

K782 — $12
K784 — $17

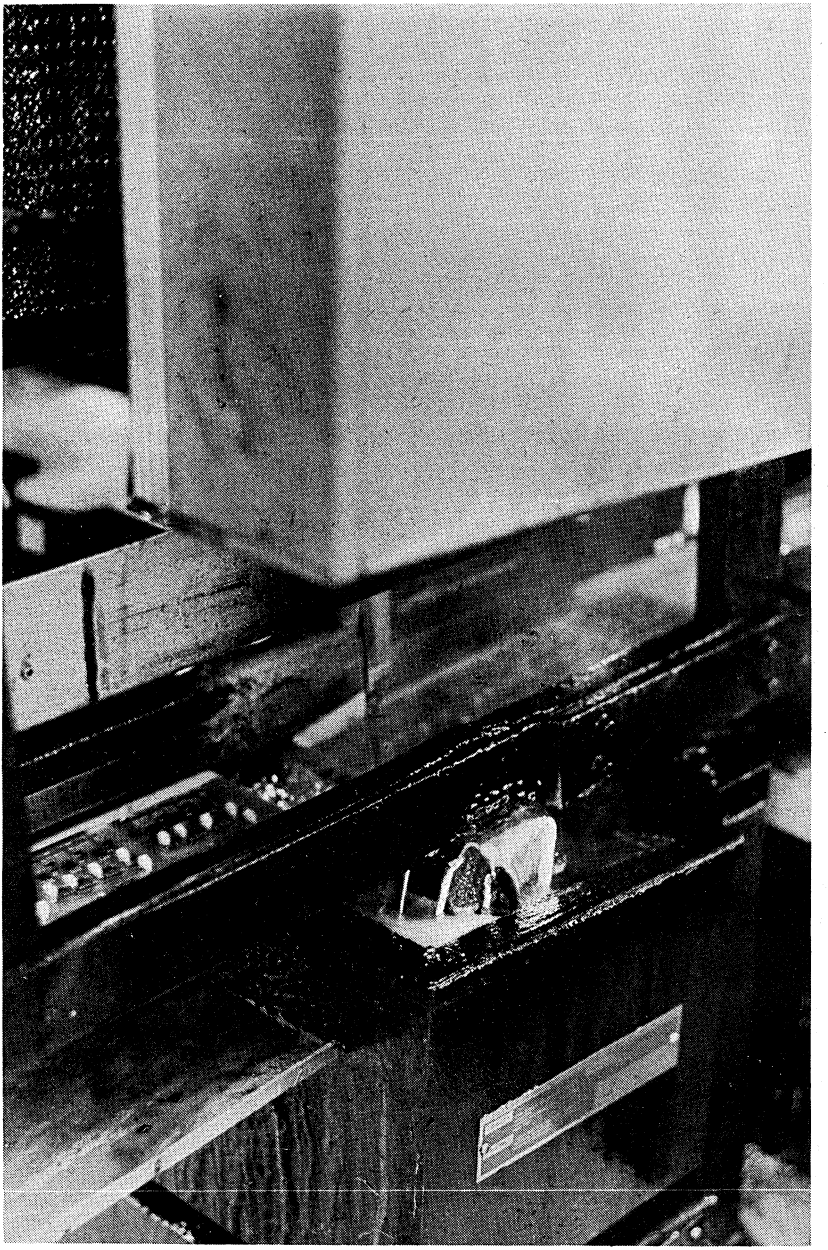


K782 TERMINALS WITH
K743 AND K980

SUMMARY OF MODULE CURRENT REQUIREMENTS

K SERIES

LOGIC MODULES		OTHER MODULES		
K003	3 ma	K508		65 ma
K012	12 ma	K522	Transducer bias plus	25 ma
K026	6 ma	K524	Transducer bias plus	35 ma
K028	8 ma	K578		0
K113	17 ma	K580	(Uses separate supply)	
K123	18 ma	K581	Per contact closed	22 ma
K124	21 ma	K596		30 ma
K134	23 ma	K604	All circuits off	40 ma
K135	22 ma		additional per circuit on	20 ma
K161	45 ma			
K174	12 ma	K614	All circuits off	40 ma
K184	56 ma		additional per circuit on	20 ma
K202	120 ma	K644	All circuits off	10 ma
K206	50 ma		additional per circuit on	160 ma
K210	150 ma	K656	All circuits off	10 ma
K220	220 ma		additional per circuit on	160 ma
K230	150 ma	K658	All circuits off	10 ma
K273	50 ma		additional per circuit on	350 ma
K281	0	K671		13 ma
K303	30 ma	K681		16 ma
K323	35 ma	K683		160 ma
K501	45 ma	K696	(Also requires 6.3vac 60 Hz or 9.0 vac 50 Hz)	7 ma



This flow-soldering machine solders all component leads to the board and makes all solder runs in one fast, exceedingly reliable, operation.

A SERIES

NOTES ON OPERATIONAL AMPLIFIERS

I. INTRODUCTION

This article describes some of the basic characteristics and uses of operational amplifiers. It is written especially for people with a digital background, but with a limited exposure to analog technology. The equations presented are not exact, but are good engineering approximations, which are accurate enough for most applications. It is hoped that this simplified discussion will provide more insight into the uses and limitations of operational amplifiers than a more rigorous approach.

The operational amplifier is a basic building block in analog work, much the same way as a NAND gate can be a basic building block in a digital computer. An operational amplifier (op amp) together with other components such as resistors and capacitors, can be used to perform addition, subtraction, integration, and many other functions. Op amps can be used to make oscillators, active filters, and even digital circuits such as Schmitt triggers, gates, and flip-flops. When used with A/D and D/A converters in data processing work, op amps perform such functions as scale changing, offsetting, and isolation between source and load.

II. GENERAL CHARACTERISTICS

An operational amplifier can be considered a 3 terminal device, plus a common or ground return, see Fig. 1. Chopper-stabilized op amps, which will not be considered here, have the Plus Input permanently tied to ground. The op amp is really a difference amplifier, in that it amplifies only the difference between the two inputs, and tries to reject any DC or AC signal that is common to both inputs.

Op amps are characterized by high DC gain, high input impedance, low output impedance, and a gain that decreases with increasing frequency. Op amps used without feedback would be operating open loop, a rare situation; but with feedback the operation would be closed loop. The use of properly applied negative feedback stabilizes the operation of the composite circuit against changes in the amplifier, and provides its versatility and usefullness.

When an op amp is working in the linear region, two approximations can be made to help in the analysis of the circuit configuration. First, the voltages of the two inputs are the same; and second, no current flows into or out of the input terminals. Fig. 2 shows a simple inverting amplifier. Assume the Minus Input is 0 volts, the same as the Plus Input, and that no current flows into the Minus Input, called the summing junction. Then $i_I = i_F$, and some simple manipulations show that the gain is equal to $-R_F/R_I$. Similar reasoning applied to the non-inverting amplifier of Fig. 3 shows that the gain is equal to $+\frac{R_1 + R_2}{R_1}$. An easy way to remember this is to think of the two resistors as forming a tapped divider network.

III. SPECIFICATIONS

Specifications are usually given for open loop performance, so that the user has to interpret and calculate how this will affect his particular closed loop circuit. The following section will give some brief descriptions of what some of the specifications mean.

Settling time. This is the time it takes the output to get within and stay within a certain amount of is final value, after the input has received a step input, see Fig. 4. This parameter is important when an amplifier is used in front of an A/D converter, since the A/D should not begin its conversion until the amplifier has settled.

Overload recovery. It takes an overload recovery time for the output to first assume its proper value after an overdriving input signal has been removed. However, the output still has not settled, and this extra time must be waited before the output is valid.

Slew rate. This term is comparable to rise or fall time in a digital circuit. It is a measure of how fast the output can change. If an amplifier output could go from 0 volts to 10 volts in 2 μsec, it would have a slew rate of 5 volts/μsec.

Frequency for full output. This is the maximum frequency at which a full scale sine wave (such as +10 to −10 volts) can be assured at the output, without noticeable distortion. In many ways this is real frequency limitation of an op amp, since up to this frequency there are no other restrictions on the amplitude of the input signal.

Frequency for unity gain. The open loop gain of an amplifier is equal to one at this frequency. But the input signal must be restricted in amplitude such that the maximum rate of change of output (slew rate) is not exceeded. Usually only millivolt signals may be processed at this frequency, therefore the full amplifier bandwidth is not usable for normal data processing systems.

Impedance. The input impedance is simply the resistance between the two inputs. The common mode impedance is the highest resistance attainable with feedback.

Common mode rejection. This is a measure of how well an amplifier will not respond to a signal common to both inputs. If used as a voltage follower, an op amp with a common mode rejection ratio (CMRR) of 10,000 could have error of 1 mv if the input were 10 v. (10/10,000 volts).

Voltage offset. The inability to achieve perfect balance in the input circuit causes the output to respond to an apparent signal when the inputs are tied to ground. For an inverting amplifier, the output error due to the input voltage offset is equal to the offset times the closed loop gain plus one. With an input offset of 3 mv, and a gain of 1, the output error would be 6 mv. Fortunately, initial voltage offset can be trimmed with a potentiometer at the right place in the circuit.

Current offset. Current offset (or bias current) multiplied by the feedback resistor (Fig. 2) produces an output error. This effect can be minimized by using the differential offset (the difference in offset currents for the two inputs) when the resistance seen from both inputs to ground are equal. For Fig. 2, the Plus Input should than be returned to ground through a resistor equal to the parallel combination of R_I and R_F.

Output ratings. The output voltage and current ratings imply a minimum value for the load resistor. 10 volts and 5 ma would correspond to a load resistor of 2 K. In an inverting amplifier, the feedback resistor is a load for the output, and the current through this resistor must be subtracted from

the amount of current still available at the output. All really useful operational amplifiers can be shorted to ground without damage, but shorting to a voltage will usually destroy some of the circuitry.

IV. APPLICATIONS

Some common configurations for operational amplifiers are shown in Figs. 5 through 10. The pin letter assignments correspond to the op amps sold by Digital Equipment Corp. If these op amps are used, the jumper between Pin S and the Minus inpunt should be removed.

The voltage follower, Fig. 5, features high input impedance, but will have an error depending on the CMRR. Large voltages cannot be handled, since common mode voltage ratings should not be exceeded. The inverter configuration, Fig. 7, is very versatile and does not have a common mode voltage problem, since both inputs are near ground. Large input voltages can be handled if the input resistor is made appropriately large. One disadvantage of the inverting configuration is that the input impedance is relatively low, essentially equal to the input resistor. When a gain trim potentiometer is used, the gain accuracy by itself becomes irrelevant. What is important is gain resolution (mostly determined by the potentiometer), and the gain stability (mostly determined by the temperature coefficients of the input and feedback resistors). The ratio of the closed loop gain to the open loop gain gives the suitability of an amplifier as far as static accuracy is concerned. With a closed loop gain of 5, and an open loop gain of 10,000, an amplifier could be used in a system with an allowable error of 1 part in 2,000.

The possibility of oscillation must always be considered when feedback amplifiers are used. Usually the more feedback used, the greater is the tendency to oscillate. Oscillations can always be attributed to phase shift. Therefore, stabilization of operational amplifiers involves phase shifting to oppose oscillation. In Fig. 7, the feedback capacitor allows high frequency signals to be fed back to the inverting input (degenerative feedback) with a phase lead. In the inverting configuration, the output will be 180° out of phase with the input at low frequencies, and the feedback signal will oppose the input signal. At high frequencies, these are additional phase lags in the amplifier and feedback circuitry. If the feedback signal has a total phase shift (lag) of 360° with a gain through the amplifier and feedback network of greater than 1, the amplifier will oscillate, since the input and output are in phase.

V. REFERENCES

1. "An Operational Amplifier Application Manual"
   Analog Devices, Inc., Cambridge, Mass.
2. "Handbook of Operational Amplifier Applications"
   Burr-Brown Research Corp., Tucson, Arizona
3. "Linear Integrated Circuits Applications Handbook"
   Fairchild Semiconductor, Mountain View, California
4. "Applications Manual for Operational Amplifiers"
   Philbrick/Nexus Research, Dedham, Mass.

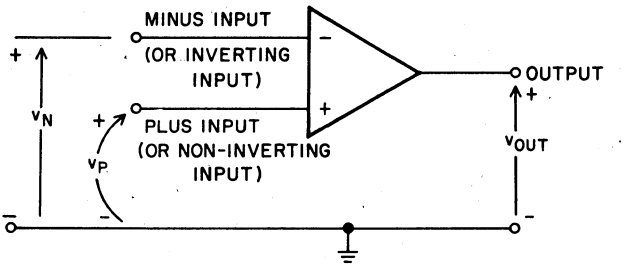
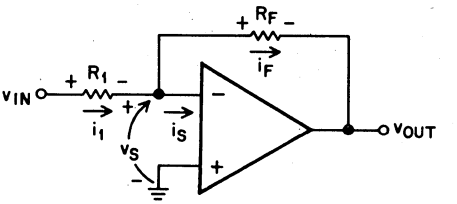


Fig. 1, Basic Operational Amplifier Symbol

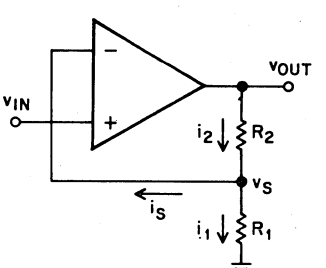


ASSUME: $v_S = 0$ THEN $i_1 = i_F$
$i_S = 0$

$$\frac{v_{IN}}{R_1} = -\frac{v_{OUT}}{R_F}$$

$$\frac{v_{OUT}}{v_{IN}} = -\frac{R_F}{R_1}$$

Fig. 2, Inverting Amplifier



ASSUME: $v_S = v_{IN}$
$i_S = 0$
THEN $i_1 = i_2$

$$\frac{v_S}{R_1} = \frac{v_{OUT} - v_S}{R_2}$$

$$\frac{v_{IN}}{R_1} = \frac{v_{OUT} - v_{IN}}{R_2}$$

$$v_{IN}\,R_2 = v_{OUT}\,R_1 - v_{IN}\,R_1$$

$$\frac{v_{OUT}}{v_{IN}} = +\frac{R_2 + R_1}{R_1}$$

Fig. 3, Non-Inverting Amplifier

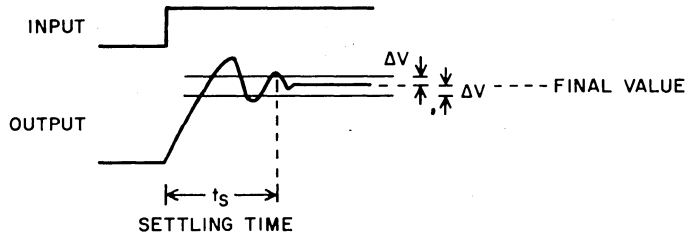


Fig. 4, Setting Time

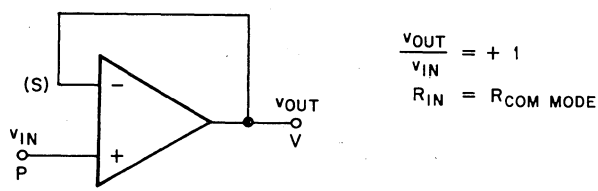


Fig. 5, Voltage Follower

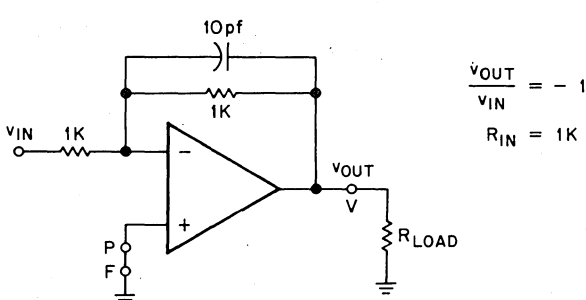
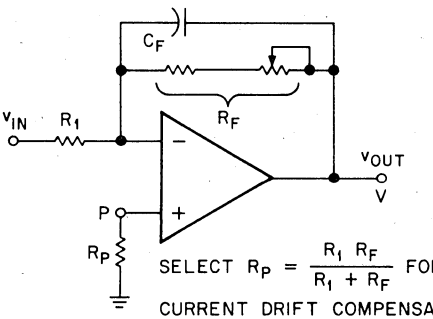


Fig. 6, Inverter



$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_1}$$

$R_{IN} = R_1$

GAIN STABILITY DEPENDS ON THE INPUT AND FEEDBACK RESISTOR, AND GAIN TRIM POTENTIOMETER.

TYP VALUES

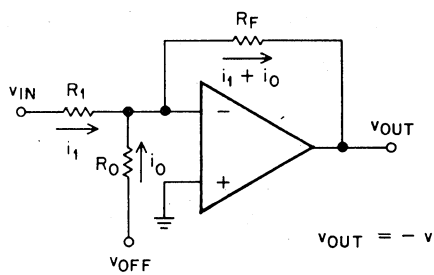
R_1 1K TO 10K

R_F 1K TO 100K

R_P 500Ω TO 5K

THE USE OF C_F REDUCES THE TENDENCY OF THE OP AMP TO OSCILLATE

Fig. 7, Adjustable Gain and Current Compensation



$$V_{OUT} = -V_{IN}\left(\frac{R_F}{R_1}\right) + \underbrace{\left[-V_{OFF}\left(\frac{R_F}{R_O}\right)\right]}_{\text{OFFSET}}$$

Fig. 8, Offsetting

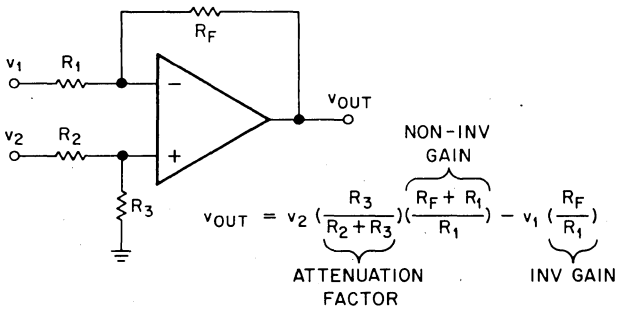
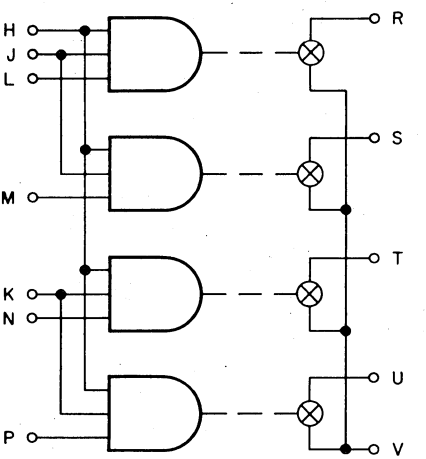


Fig. 9, Differential Gain

POSITIVE LOGIC MULTIPLEXER
TYPE A123

A SERIES



INPUT	OUTPUT TERMINALS
+3V	CONNECTED
0V	OPEN

The A123 Multiplexer provides 4 gated analog switches that are controlled by logic levels of 0v and +3v. The module is equivalent to a single-pole, 4-position switch, since one output terminal of each MOS FET switch is tied together. If all three digital inputs of a circuit are at +3v (or not connected) the two output terminals are connected together. If any digital input is at 0v, the switch terminals are disconnected. Two switches should not be on at the same time. The analog switch can handle signals between +10v and −10v, with currents up to 1 ma.

The positive power supply must be between +5v and +15v, and at least equal to or greater than the most positive excursion of the analog signal. The negative power supply must be between −5 and −20v, and at least 10 volts more negative than the most negative excursion of the analog signal. The voltage difference between the two supplies must not be more than 30v.

SPECIFICATIONS

Digital Inputs

Logic ONE:	+2.4v to +5.0v
Logic ZERO:	0.0v to +0.8v
Input loading:	0.5 ma at 0 volts

Analog Signal

Voltage range:	+10v to −10v
Current (max.):	1 ma

Output Switch

On resistance, max.:	1000 ohms
On offset:	0 volts
Off leakage, capacitance:	10 na, 10 pf
Turn on delay, max.:	0.2 μsec
Turn off delay, max.:	0.5 μsec

Power

+5v (pin A):	45 ma
+v (pin D):	18 ma (for +10v)
−v (pin E):	50 ma (for −20v)

A123—$58

OPERATIONAL AMPLIFIER
TYPE A200

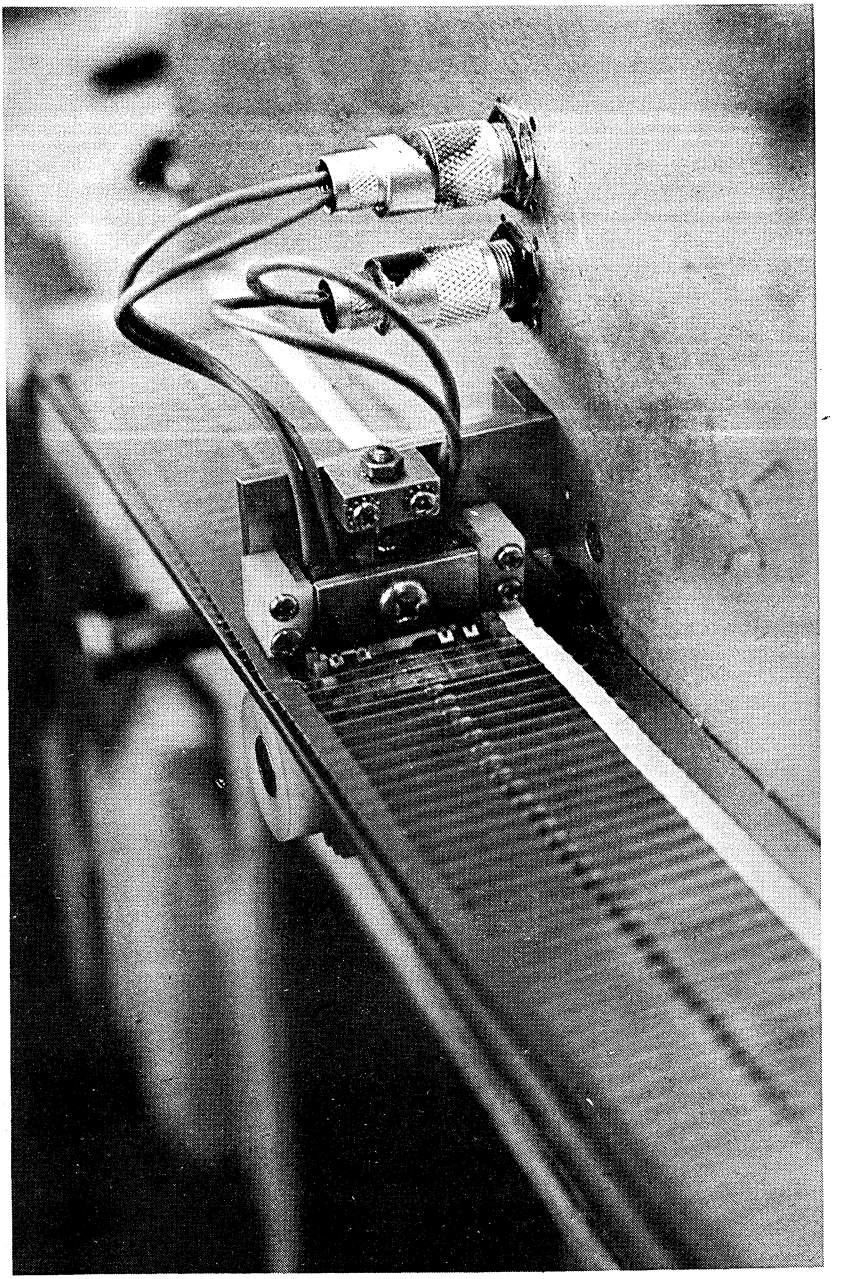
A SERIES

The A200 is an operational amplifier mounted on an A990 amplifier board. Provisions are made on the board for the mounting of potentiometers for gain trim and balance. Mounting holes are also provided for input and feedback networks, and rolloff capacitor. The module is a double width board.

OPEN LOOP GAIN:	$2x10^6$
RATED OUTPUT	
Voltage:	±11v
Current:	20 ma
FREQUENCY RESPONSE	
Unity gain, small signal:	10 MHz
Full output voltage:	300 kHz
Slewing rate:	30v/μsec
Overload recovery:	200 μsec
INPUT VOLTAGE OFFSET (Adjustable to Zero)	
Average vs. Temperature:	20 μv/°C
Average vs. Supply voltage:	15 μv/%
Average vs. Time:	10 μv/day
INPUT CURRENT OFFSET:	±2 na
Average vs. Temperature:	0.4 na/°C
Average vs. Supply voltage:	0.15 na/%
INPUT IMPEDANCE	
Between inputs:	6 megohm
Common mode:	500 megohm
INPUT VOLTAGE	
Maximum:	±15 volts
Maximum common mode:	±10 volts
Common mode rejection:	20,000
POWER	
Voltage:	±15 volts
Current at rated load:	35 ma

*REFER TO A990 FOR CONNECTIONS

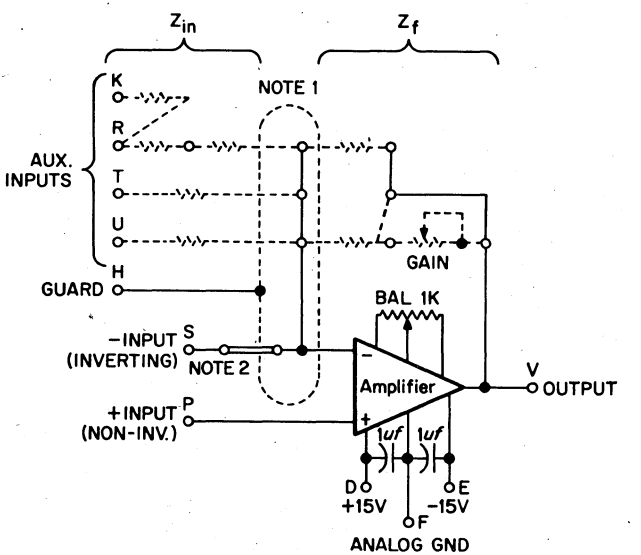
A200 — $130



All incoming components are 100% tested. Here, diodes are being tested automatically.

OPERATIONAL AMPLIFIER
A206

A SERIES



NOTE 1. Mounting holes are provided on the module so that input and feedback components can be added. Components shown with dashed lines are not included with the module.

NOTE 2. This jumper comes with the module. It may be removed to suit circuit requirements.

The A206 Operational Amplifier features extremely fast settling time (2 μs to within 1 mv), making it especially suited for use with Analog-to-Digital Converters. FET's are used in the input stage to provide high input impedance. The A206 can be used for buffering, scale-changing, offsetting, and other data-conditioning functions required with A/D converters. All other normal operational amplifier configurations can be achieved with the A206.

The A206 is supplied with a zero balance potentiometer. Provisions are made on the board for the mounting of input and feedback components, including a gain trim potentiometer. The A206 is pin-compatible with the A200 Operational Amplifier.

SPECIFICATIONS—At 25°C, unless noted otherwise.

Settling Time*	
Within 1 mv, 10v step input, typ:	1.5 μsec
Within 1 mv, 10v step input, max:	2.0 μsec
Frequency Response	
DC open loop gain, 670 ohm load, min:	100,000
Unity gain, small signal, min:	10 MHz
Full output voltage, min:	1 MHz
Slewing rate, min:	100v/μsec
Overload recovery, max:	0.5 μsec
Output	
Voltage, max:	±10v
Current, max:	±15 ma
Input Voltage	
Input voltage range, max:	±10v
Differential voltage, max:	±15v
Common mode rejection, min:	7,000
Input Impedance	
Between inputs, min:	10^{10} ohms
Common mode, min:	10^{10} ohms
Input Offset	
Avg. voltage drift vs. temp., max:	±30 μv/°C
Avg. volt. drift vs. supply volt., max:	±20 μv/%
Initial differential current offset, max:	0.03 na
Avg. dif. cur. drift vs. temp., max:	±0.003 na/°C
Temperature Range	0°C to +60°C
Power	
+15v (pin D), quiescent:	15 ma
−15v (pin E), quiescent:	15 ma

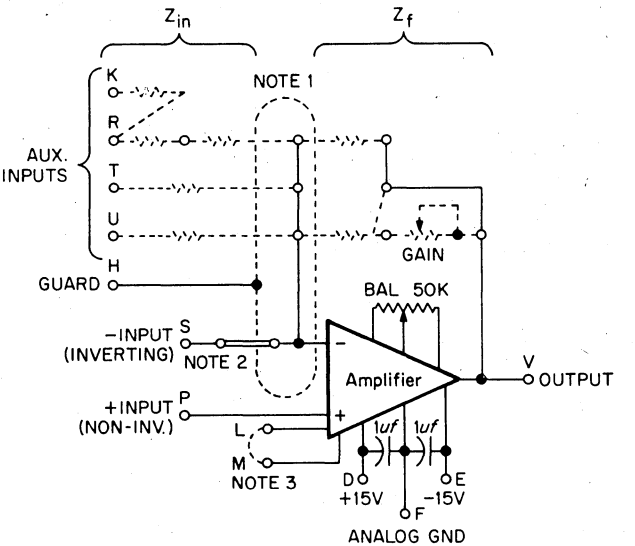
If the Output is accidentally shorted to ground, the amplifier will not be damaged.

*Gain of 1, inverting or non-inverting configuration.

A206 — $190

OPERATIONAL AMPLIFIER
A207

A SERIES



NOTE 1. Mounting holes are provided on the module so that input and feedback components can be added. Components shown with dashed lines are not included with the module.

NOTE 2. This jumper comes with the module. It may be removed to suit circuit requirements.

NOTE 3. Pins L & M can be connected together to improve settling time, but parameters such as drift and open loop gain are degraded.

The A207 is an economical Operational Amplifier featuring fast settling time (5 μs to within 10 mv), making it especially suited for use with Analog-to-Digital Converters. The A207 can be used for buffering, scale-changing, offsetting, and other data-conditioning functions required with A/D Converters. All other normal operational amplifier configurations can be achieved with the A207.

The A207 is supplied with a zero balance potentiometer. Provisions are made on the board for the mounting of input and feedback components, including a gain trim potentiometer. The A207 is pin-compatible with the A200 Operational Amplifier.

SPECIFICATIONS—At 25°C, unless noted otherwise.

	Pins L & M Connected	Differences with Pins L & M Not Connected
Settling Time*		
Within 10 mv, 10v step input, typ:	3 μsec	6 μsec
Within 10 mv, 10v step input, max:	5 μsec	8 μsec
Within 1 mv, 10v step input, max:	7 μsec	10 μsec
Frequency Response		
DC open loop gain, 670 ohm load, min:	15,000	100,000
Unity gain, small signal, min:	3 MHz	
Full output voltage, min:	50 KHz	
Slewing rate, min:	3.5v/μsec	
Overload recovery, max:	8 μsec	
Output		
Voltage, max:	±10v	
Current, max:	±15 ma	
Input Voltage		
Input voltage range, max:	±10v	
Differential voltage, max:	±10v	
Common mode rejection, min:	10,000	
Input Impedance		
Between inputs, min:	100 K ohms	
Common mode, min:	5 M ohms	
Input Offset		
Avg. voltage drift vs. temp, max:	60 μv/°C	30 μv/°C
Initial current offset, max:	0.5 μa	
Avg. current drift vs. temp, max:	5 na/°C	
Temperature Range	0°C to +60°C	
Power		
+15v (pin D), quiescent:	6 ma	
−15v (pin E), quiescent:	10 ma	

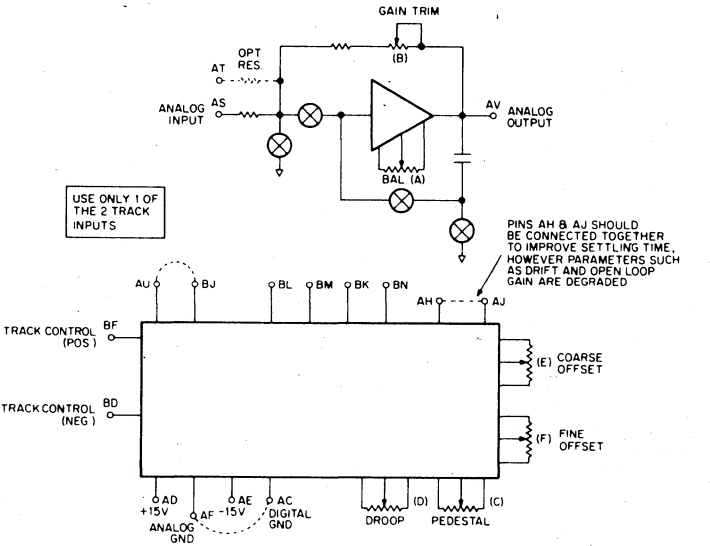
If the Output is accidentally shorted to ground, the amplifier will not be damaged.

*Gain of 1, inverting or non-inverting configuration.

A207 — $45

SAMPLE AND HOLD
A404

A SERIES



JUMPER CONNECTIONS TO OFFSET OUTPUT

	MODE	
PIN	TRACK (sample)	HOLD
BF (pos)	+3v or open	0v
BD (neg)	−3v or open	0v

Positive	Negative
AU to BJ	AU to BJ
	BL to AD
BM to AE	
BK to AF	BN to AF

Analog gnd (pin AF) and digital gnd (pin AC) must be connected together at one point in the system.

The A404 Sample & Hold has an acquisition time of 6 μsec for a 10 volt signal to within 10 mv (0.1%). The circuit inverts the input signal, and has an input impedance of 10 K. Features of the circuit include potentiometers to control the pedestal and the droop of the output signal.

Two digital Track Control (sample) inputs are provided: one for negative logic (0v & −3v), and the other for positive logic (0v & +3v). Either input by itself will perform the necessary control, and the inadvertent application of both digital signals will cause no damage to the circuit.

Potentiometers are also provided for zero balancing, gain trim, and offset adjustment (up to ±10v). If offsetting is desired, connections should be made according to the table shown with the diagram. The A404 is pin-compatible with the A400 Sample & Hold.

SPECIFICATIONS—At 25°C, unless noted otherwise. Pins AH & AJ are connected together.

Acquisition Time

Within 10 mv, 10v step input, typ:	4 μsec
Within 10 mv, 10v step input, max:	6 μsec
Within 2.5 mv, 10v step input, max:	11 μsec

Aperture Time, max: 0.2 μsec

Gain —1.000 (adjustable ±0.2%)

Input

Voltage range, max:	±10v
Impedance:	10 K ohms

Output

Voltage range, max:	±10v
Current, max:	10 ma

Pedestal*

Initial pedestal:	Adjustable to less than 1 mv
Pedestal variation vs. temp, max:	0.2 mv/°C

Droop

Initial droop:	Adjustable to less than 5 mv/ms
Droop variation vs. temp, max:	2 mv/ms/°C

Track Control

Pos. (pin BF)	+3v, Track 0v at 2 ma, Hold
Neg. (pin BD)	−3v, Track 0v at 1 ma, Hold

Board Size 1 double height board, single module width

Temperature Range 0°C to +50°C

Power

+15v (pin AD), quiescent:	22 ma
−15v (pin AE), quiescent:	35 ma

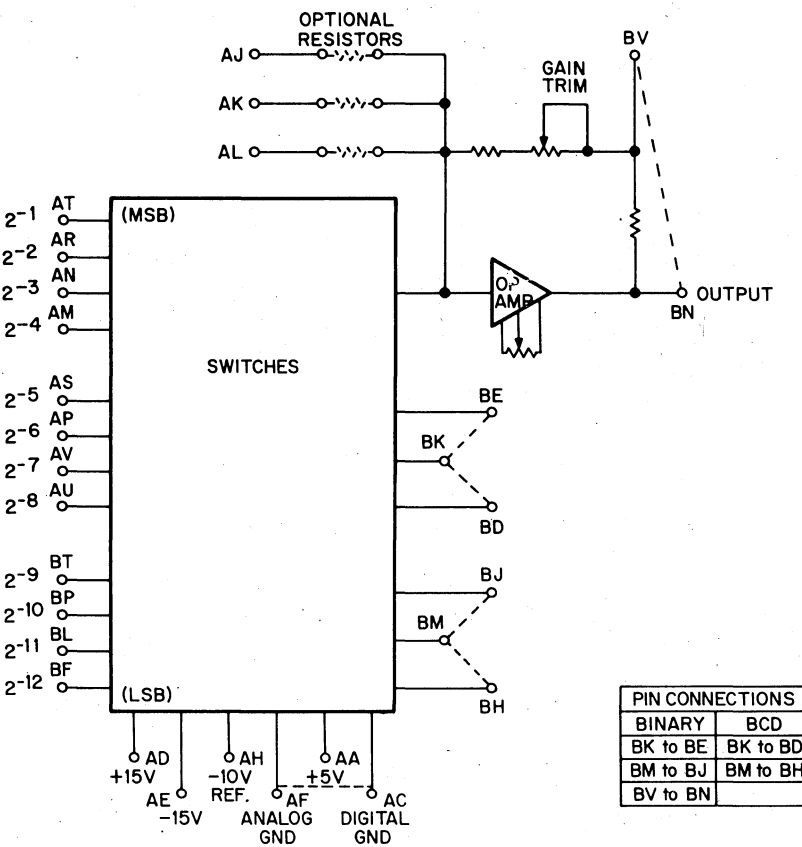
If the Output is accidentally shorted to Ground, the circuit will not be damaged.

*Difference in output voltage when changing from Track to Hold mode.

A404 — $130

12-BIT DAC
A613

A SERIES



PIN CONNECTIONS	
BINARY	BCD
BK to BE	BK to BD
BM to BJ	BM to BH
BV to BN	

BINARY INPUTS		OUTPUT
2^{-1}	ALL OTHERS	
0V	0V	+0.000V
+3	0	+5.000
+3	+3	+9.9975

ANALOG GND (PIN AF) & DIGITAL GND (PIN AC) MUST BE CONNECTED TOGETHER AT ONE POINT IN THE SYSTEM.

The A613 is a 12-bit Digital-to-Analog Converter for moderate speed applications. The module is controlled by standard positive logic levels, has an output between 0v and +10v, and will settle within 50 μsec for a full scale input change. The input coding can be either straight binary or 3 decades of 8421 BCD with only simple connector jumpers required to take care of the change.

The A613 requires a —10.0v reference that can supply negative current, such as an A704. Provisions are made for adding up to 3 extra resistors to implement offsetting functions. Potentiometers are provided for zero balancing, and gain trim. The A613 is a double height board.

An input of all Logic 0's produces zero volts out; all Logic 1's produces close to +10v out. The operational amplifier output can be shorted to Ground without damaging the circuit.

SPECIFICATIONS

Inputs

Logic ONE:	+2.0v to +5.0v
Logic ZERO:	0.0v to +0.8v
Input loading:	1 ma (max.) at 0 volts

Output

Standard:	0v to +10v
Optional, (requires Positive REF)	10v range between —10v and +10v
Settling time, (10v step):	50 μsec
Output current:	10 ma
Capacitive loading:	0.1 μf (without oscillation)

Binary Dig. In.	Analog Out	BCD (8421)	Analog Out
000 — 00	0.0000v	000	0.000v
000 — 01	+0.0025	001	+0.010
100 — 00	+5.0000	050	+0.500
111 — 11	+9.9975	500	+5.000
		999	+9.990

Accuracy

	Binary	BCD
At +25°C:	±0.015% of full scale	±0.05% of full scale
Temp. coef:	±0.001%/°C (plus drift of REF)	±0.002%/°C (plus drift of REF)

Board Size

1 double height board, single module width

Temperature Range

+10°C to +50°C

Power

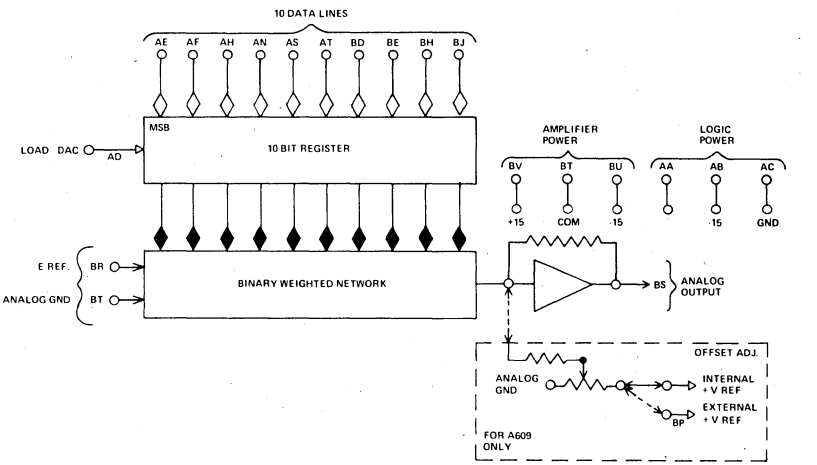
+15v at 35 ma
—15v at 60 ma } at max. load
+ 5v at 60 ma
—10.0v REF at —7 ma (reverse current)

If the Output is accidentally shorted to Ground, the output amplifier will not be damaged.

A613 — $250

10-BIT D/A CONVERTER SINGLE BUFFERED
TYPES A618 and A619

A SERIES



The A618 and the A619 Digital to Analog Converters (DAC) are contained on one DEC double Flip-Chip™ Module. These modules are also double width in the lower (B section) half. The converters are complete with a 10-bit buffer registers, level converters, a precision divider network, and a current summing amplifier capable of driving external loads up to 10 ma. The reference voltage is externally supplied for greatest efficiency and optimum scale factor matching in multi-channel applications.

The A609 DAC output voltage is bi-polar while the A618 DAC output voltage is uni-polar.

Binary numbers are represented as shown (right justified) in Table 1:

TABLE 1

Binary Input	Analog Output (Standard)	
	A618	A619
0000_8	0v	−10v or −5v
0400_8	+2.5v	−5v or −2.5v
1000_8	+5.0v	0 volts
1400_8	+7.5v	+5v or +2.5v
1777_8	+10.0v	+10v or +5v

OUTPUT:

Voltage: (A618 — Standard)	0 to +10 volts
Voltage: (A619 — Standard)	±5 or ±10 volts
Current:	10 ma MAX.
Impedance:	<0.1 ohm
Settling Time:	
(Full scale step, resistive load)	<5.0 μsec
(Full scale step, 1000 pf)	<10.0 μsec
Resolution:	1 part in 1024
Linearity:	±0.05% of full scale
Zero Offset:	±5 mv MAX.
Temperature Coefficient:	<0.2 mv/°C
Temperature Range:	0 to 50°C

INPUT:

Level: 1 TTL Unit load.

Pulse: (positive)	
Input loading: 20 TTL Unit load	
Rise and Fall Time:	20 to 100 nsec
Width:	> 50 nsec
Rate:	10^6 Hz max.

Timing:

Data lines must be settled 40 nsec before the "LOAD DAC" pulse (transition) occurs.

POWER REQUIREMENTS:

Reference Power:	—10.06 volts, 60 ma
Amplifier Power:	±15 volts, 25 ma (plus output loading)
Logic Power:	+5volts, 135 ma
	—15 volts, 60 ma

NOTES:

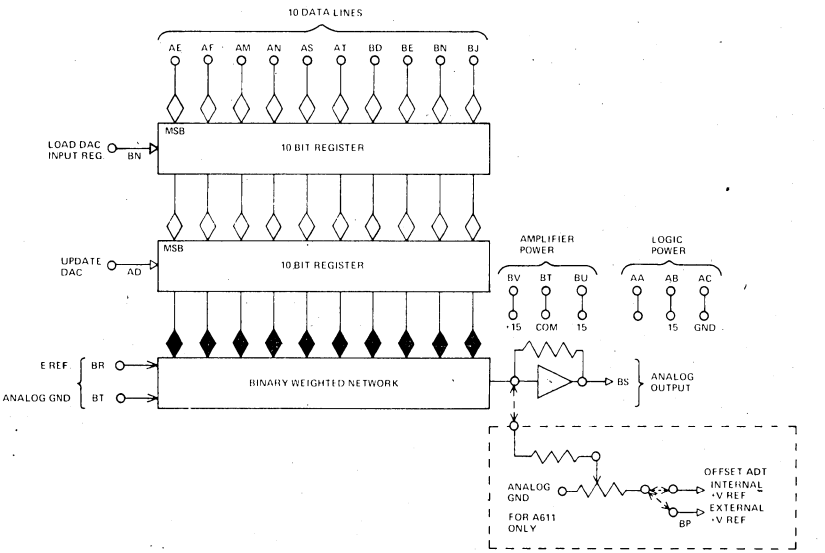
*Voltage — A619: Full scale voltage (±5 or ±10) must be specified at time of purchase.

Price: Price stated is for standard output voltage and current. Other output characteristics are available on request.

A618 — $350
A619 — $375

10-BIT D/A CONVERTER DOUBLE BUFFERED
TYPES A620 and A621

A SERIES



The A620 and the A621 Digital-to-Analog Converters (DAC) are contained on one DEC double Flip-Chip Module. These modules are also double-width in the lower (B section) half. The converters are complete with two 10-bit buffer registers, level converters, a precision divider network, and a current summing amplifier, capable of driving external loads up to 10 ma. The reference voltage is externally supplied for greatest efficiency and optimum scale-factor matching in multi-channel-application.

The A621 DAC output voltage is bi-polar while the A620 DAC output voltage is uni-polar.

The double-buffered DAC's are offered to satisfy those applications where it is imperative to update several analog output simultaneously. When DAC's deliver input to a multi-channel analog tape system or update the constants of an analog computer, the double-buffer feature may be necessary to prevent skew in the analog data.

Binary numbers are represented as shown (right justified) in Table 1:

TABLE 1

Binary Input	Analog Output (Standard)	
	A620	A621
0000_8	0v	−10v or −5v
0500_8	+2.5v	−5v or −2.5v
1000_8	+5.0v	−0 volts
1500_8	+7.5v	+5v or +2.5v
1777_8	+10.0v	+10v or +5v

OUTPUT:

Voltage: (A620 — Standard)	0 to 10 volts
Voltage: (A621 — Standard*)	±5 or ±10 volts
Current:	10 ma MAX.
Impedance:	<0.1 ohms
Settling Time:	
(Full scale step, resistive Load)	<5.0 μsec
(Full scale step, 1000 pf)	<10 μsec
Resolution:	1 part in 1024
Linearity:	±0.05% of full scale
Zero Offset:	±5 mv MAX.
Temperature Coefficient:	<0.2 mv/°C
Temperature Range:	0 to 50°C

INPUT:

Level: 1 TTL Unit load

Pulse: (positive)

Input loading:	20 TTL Unit load
Rise and Fall Time:	20 to 100 nsec
Width:	> 50 nsec
Rate:	10^6 Hz MAX.

Timing:

1. Data lines must be settled 40 nsec before the "LOAD DAC" pulse (transition) occurs.
2. The "Update DAC" pulse must occur more than 100 nsec after the "LOAD DAC" pulse.

POWER REQUIREMENTS:

Reference Power:	−10.6 volts, 60 ma
Amplifier Power:	±15 volts, 25 ma (plus output loading)
Logic Power:	+ 5 volts, 190 ma
	−15 volts, 60 ma

Notes:

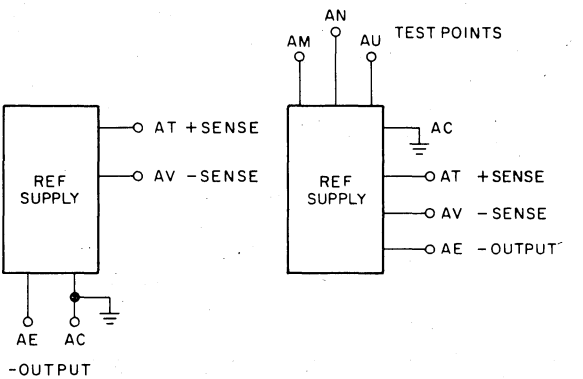
*Voltage — A621: Full scale voltage (±5 or ±10) must be specified at time of purchase.

Price: Price stated is for standard output voltage and current. Other output characteristics are available on request.

A620 — $400
A621 — $425

REFERENCE SUPPLIES
TYPES A702, A704
(DOUBLE HEIGHT)

A SERIES



Module Type	Output	Current	Temperature Coefficient	Regulation	Ripple Peak to Peak
A702	−10 v	±60 ma	1mv/°C	30 mv, no load to full load	10 mv
A704	−10 v	−90 to +40 ma	1 mv/8 hrs 1 mv/15° to 35°C 4 mv/0° to 50°C	0.1 mv. no load to full load	0.1 mv

Module Type	Adjustment Resolution	Input Power	Use	Output Impedance
A702	5 mv	−15 v/100 ma +10 v (B)/10 ma	Load with 500 μf at load. May also be preloaded if desired	0.5 ohms
A704	0.01 mv	−15 ±2 v/250 ma	See below for sensing and preloading	0.0025 ohms

Remote Sensing: The input to the regulating circuits of the A704 is connected at sense terminals AT (+) and AV (−). Connection from these points to the load voltage at the most critical location provides maximum regulation at a selected point in a distributed or remote load. When the sense terminals are connected to the load at a relatively distant location, a capacitor of approximately 100 μf should be connected across the load at the sensing point.

Preloading: The supplies may be preloaded to ground or —15v to change the amount of current available in either direction. For driving DEC Digital-Analog Converter modules, —125 ma maximum can be obtained by connecting a 270Ω±5% 1 watt resistor from the —10v pin AE reference output to pin AC ground (A704 only).

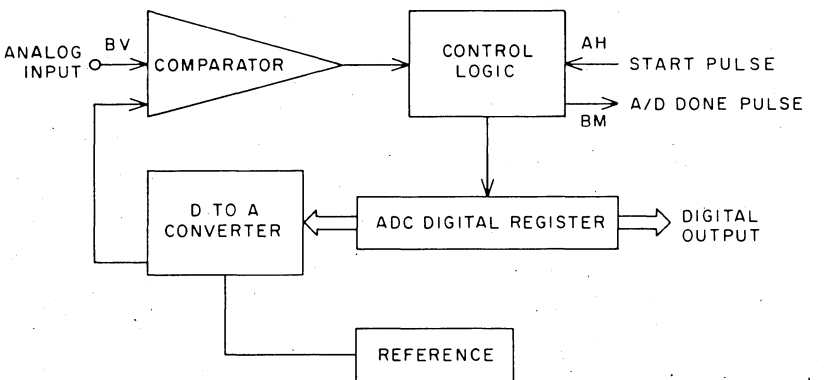
Pin Connections: The A704 is a double-sized module. The top pin letters are prefixed A.

Wiring: Digital-analog and analog-digital converters perform best when module locations and wiring are optimized. All Digital-Analog Converter modules should be side-by-side, with Type 932 bus strip used to bus pins E and pins F together on all converter modules. In an analog-digital converter, the comparator should be mounted next to the converter module for the bits of most significance. The reference supply modules should be mounted nearby, and if the A704 is used, its sense terminals should be wired to pins E and F of the most-significant-bits converter module. The high quality ground must be connected to the common ground only at pin AC of the reference supply module, and this point should also be the common ground for analog inputs to analog-digital converters. Do not mount A-series modules closer than necessary to power supply transformers or other sources of fluctuating electric or magnetic fields.

A702 — $ 58
A704 — $184

10 BIT A/D CONVERTER
A811

A SERIES



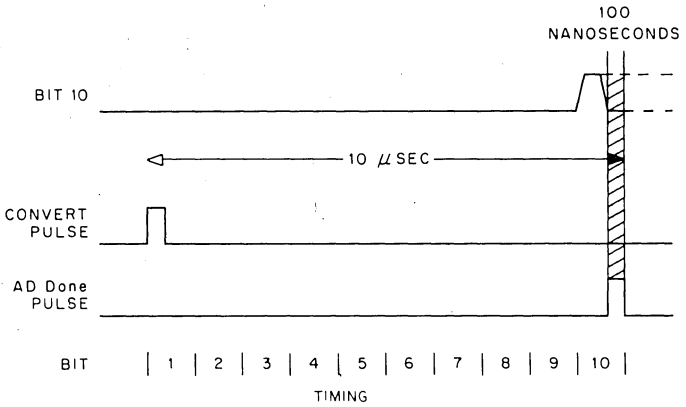
A811 10-BIT ANALOG-TO-DIGITAL CONVERTER

BIT 1 (MSB)	AE
2	AD
3	AN
4	AM
5	BL
6	BR
7	BK
8	BP
9	BS
10 (LSB)	BT

A811 10-BIT ANALOG-TO-DIGITAL CONVERTER

The A-811 is a complete, 10-bit successive approximation, analog to digital converter with a built in reference supply. The complete converter is contained on one DEC double FLIP CHIP™ logic module. Conversion is initiated by raising the Convert input to logic 1 (+4 volts). The digital result is available at the output within 10 microseconds. An A/D Done Pulse is generated when the result is valid. The A-811 uses monolithic integrated circuits for control logic, output register, and comparator.

The A811 requires 2 vertical connectors and the top section (connector A) requires 2 connector widths.



SPECIFICATIONS:

	Max.	Min.
Convert Pulse Input:		
Input loading	10 TTL unit load	
Pulse Width	500 nsec	100 nsec
Pulse Rise Time	250 nsec	—
A/D Done Pulse Output:		
Pulse Width	300 nsec	100 nsec
Digital Output:		
Logical "0"	+0.4v	0v
Logical "1"	+3.6v	+2.4v
Output Current "0"	16 ma	
Output Current "1"	—0.4 ma	
Input:		
Input Voltage	0 to +10v	
Input Impedance	1000 ohms	
Resolution:	10 bits	
Accuracy:	0.1% of full scale	
Temperature Coefficient:	0.5 mv/°C	
Operating Temperature:	0°C to 50°C	
Conversion Rate:	100 KHz MAX.	
Output Format:	Parallel Binary Uni-polar	

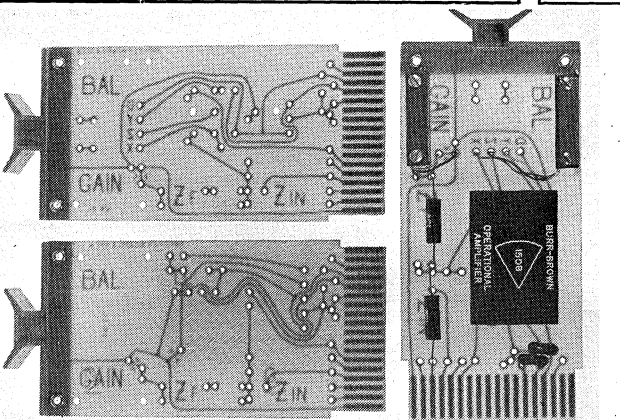
Power:
+15 volts ±1% 20 ma (pin BU)
—15 volts ±1% 160 ma (pin AV)
+ 5 volts ±1% 300 ma (pin AA)

Options:
The Input impedance of the A/D converter can be raised to greater than 100 megohms by adding an input amplifier module. A sample and hold amplifier module may also be included. The impedance of the converter with sample and hold is 10,000 ohms. Both options may be included simultaneously if high impedance and narrow aperture are both required.

A811 — $450

AMPLIFIER BOARDS
TYPES A990, A992

A SERIES



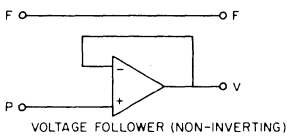
Many types of commercially available operational amplifiers can be mounted in the holes provided on these predrilled etched boards. Mounting holes and printed wires provide for balance trim, gain trim, and feedback networks required to build such common operational devices as voltage followers, inverting or non-inverting amplifiers, integrators, differentiators, summers and subtractors. Most amplifiers listed in the table below require ±15v regulated supplies which are readily available from the amplifier manufacturers. Notable exceptions are Analog Devices' Models 101, 103, and 104 which may be used with standard DEC +10v, −15v supplies at some sacrifice in voltage range (+5, −10v) and noise.

Power: Positive at pin D, negative at pin E, common at pin F for all types. Space is provided for mounting bypass capacitors used with some high frequency amplifiers.

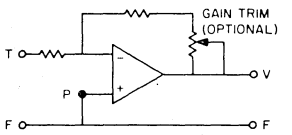
Trimming: Mounting holes on 1" centers at the handle end accept wirewound potentiometers for balance and feedback (gain) trimming. Gain rheostat may be connected in series with feedback components to allow precise adjustment of gain using inexpensive 1% feedback resistors. Board is etched to allow for use without gain trimming, and one pointed conductor must be cut at caret marks to put a rheostat in the circuit. Gain rheostat stray capacitance to ground is driven by amplifier output.

Amplifier Supplier	Types accepted by A990	Types accepted by A992 (boosters too)
Analog Devices	101, 102, 104, etc.	103, 106, 107, etc.
Burr-Brown*	1500-46, 1500-68	—
Data Device Corp.	—	most types, except boosters
Nexus	Case K or Case L	Case Q
Philbrick	—	Case PP
Union Carbide	—	most types
Zeltex	—	Case A

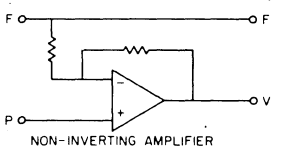
*Except Burr-Brown differential output and chopper stabilized types: Perforated board W994 or other blank module may be used to mount non-standard configurations.



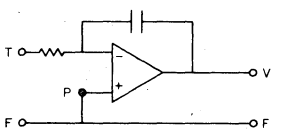
VOLTAGE FOLLOWER (NON-INVERTING)



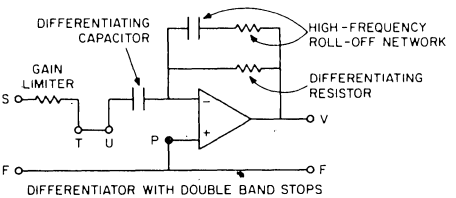
INVERTING AMPLIFIER



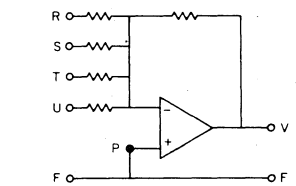
NON-INVERTING AMPLIFIER



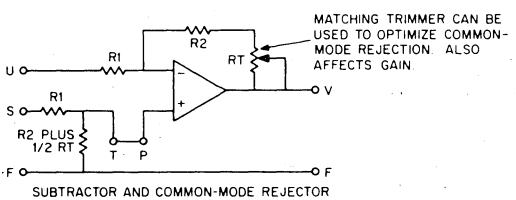
INTEGRATOR



DIFFERENTIATOR WITH DOUBLE BAND STOPS

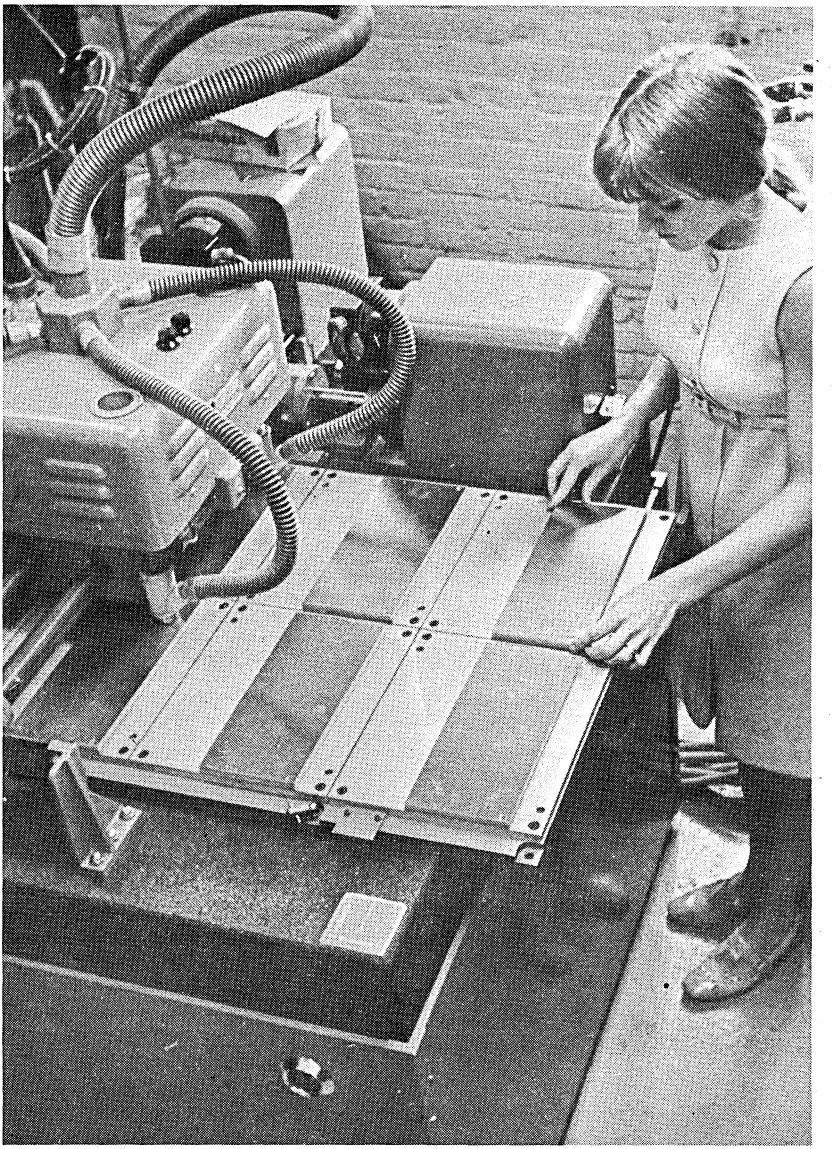


FOUR-INPUT SUMMER



SUBTRACTOR AND COMMON-MODE REJECTOR

A990 — $4
A992 — $4



Twenty module boards are drilled simultaneously from a computer-generated coordinate tape. Other pantograph-controlled machines drill up to 200 boards simultaneously from a computer-generated template.

PART II
HARDWARE, POWER SUPPLIES AND ACCESSORIES

INTRODUCTION

Digital manufactures a complete line of hardware accessories in support of its module series. Module connectors are available for as few as one module and as many as 64. A complete line of cabinets is available to house the modules and their connector blocks, as well as providing a convenient means for system expansion. Power supplies for both large and small systems and reference supplies are also available.

Coupled with the recent additions to the hardware line, Digital has made every effort to maintain or improve the high standards of reliability and performance of its present line. Through the availability of a wide range of basic accessories. DEC feels that it is offering the logic designer the necessary building blocks which he requires for complete system design.

50-CYCLE POWER

Because of the demand for Digitals products in areas where 115-v, 60-cps power is not available, each of the power supplies with a frequency-sensitive regulating transformer is also available in a multi-voltage 50-cps version. All 50-cps supplies have the same input connections. The line input is on pins 3 and 4. Jumpers should be connected depending on the input voltage. These connections are shown below along with a schematic.

WIRING HINTS

These suggestions may help reduce mounting panel wiring time. They are not intended to replace any special wiring instructions given on individual module data sheets or in application notes. For fastest and neatest wiring, the following order is recommended.

(1) All power & ground wiring and any horizontally bussed signal wiring. Use Horizontal Bussing Strips Type 932 or Type 933.

(2) Vertical grounding wires interconnecting each chassis ground with pin C grounds. Start these wires at the uppermost mounting panel and continue to the bottom panel. Space the wires 2 inches apart, so each of the chassis-ground pins is in line with one of them. Each vertical wire makes three connections at each mounting panel.

(3) All other ground wires. Always use the nearest pin C above the pin to be grounded, unless a special grounding pin has been provided in the module.

(4) All signal wires in any convenient order. Point-to-point wiring produces the shortest wire lengths, goes in the fastest, is easiest to trace and change, and generally results in better appearance and performance than cabled wiring. Point-to-point wiring is strongly urged.

The recommended wire size for use with the H800 mounting blocks and 1943 mounting panel is 24 for wire wrap, and 22 for soldering. The recommended size for use with H803 block and H911 mounting panel is #30 wire. Larger or smaller wire may be used depending on the number of connections to be made to each lug. Solid wire and a heat resistant spaghetti (Teflon) are easiest to use when soldering.

Adequate grounding is essential. In addition to the connection between mounting panels mentioned above, there must be continuity of grounds between

cabinets and between the logic assembly and any equipment with which the logic communicates.

When soldering is done on a mounting panel containing modules, a 6-v (transformer) soldering iron should be used. A 110-v soldering iron may damage the modules.

When wire wrapping is done on a mounting panel containing modules, steps must be taken to avoid voltage transients that can burn out transistors. A battery- or air-operated tool is preferred, but the filter built into some line-operated tools affords some protection.

Even with completely isolated tools, such as those operated by batteries or compressed air, a static charge can often build up and burn out semiconductors. In order to prevent damage, the wire wrap tool should be grounded except when all modules are removed from the mounting panel during wire wrapping.

AUTOMATIC WIRING

Significant cost savings can be realized in quantity production if the newest automatic wiring techniques are utilized. Every user of FLIP CHIP modules benefits from the extensive investment in high-production machinery at Digital, but some can go a step further by taking advantage of programmed wiring for their FLIP CHIP digital systems.

While the break-even point for hand wiring versus programmed wiring depends upon many factors that are difficult to predict precisely, there are a few indications:

1. One-of-a-kind systems will probably not be economical with automatic wiring, even when the size is fairly large; programming and administrative costs are likely to outweigh savings due to lower costs in the wiring itself.

2. At the other end of the spectrum, production of 50 or 100 identical systems of almost any size would be worth automating, not only to lower the cost of the wiring itself but also to reduce human error. At this level of volume, machine-wired costs can be expected to be less than the cost of hand wiring.

3. For two to five systems of several thousand wires each, a decision on the basis of secondary factors will probably be necessary: ease of making changes, wiring lead time, reliability predictions, and availability of relevant skills are factors to consider.

The Gardner-Denver Corporation, and Digital can supply further information to those interested in programmed wiring techniques. At Digital, contact the Module Sales Manager, Sales Department.

COOLING OF FLIP CHIP MODULES

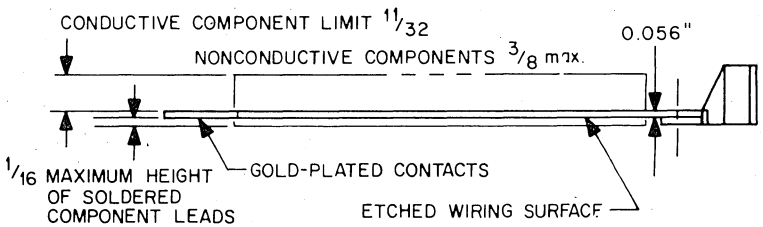
The low power consumption of K and M series modules results in a total of only about 25 watts dissipation in a typical 1943 Mounting Panel with 64 modules. This allows up to six panels of modules to be mounted together and cooled by convection alone, if air is allowed to circulate freely. In higher-dissipation systems using modules in significant quantities from the A series,

the number of mounting panels stacked together must be reduced without forced-air cooling. In general, total dissipation from all modules in a convection-cooled system should be 150 watts or less.

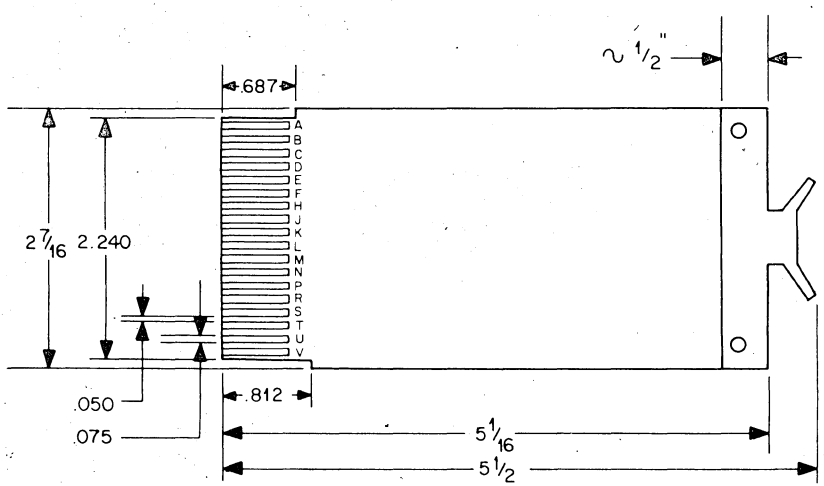
The regulating transformers used in most DEC power supplies have nearly constant heat dissipation for any loading within the ratings of the supply. Power dissipated within each supply will be roughly equal to half its maximum rated output power. If power supplies are mounted below any of the modules in a convection-cooled system, this dissipation must be included when checking against the 150 watt limit.

STANDARD MODULE SIZES

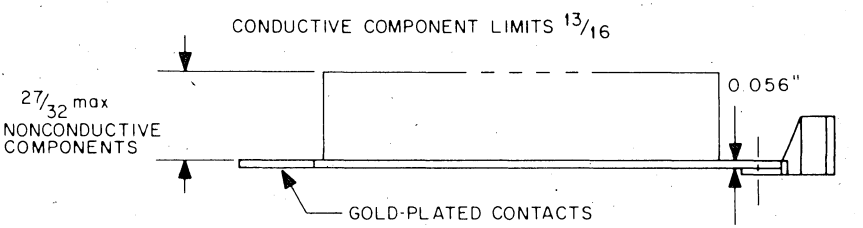
SINGLE-WIDTH FLIP CHIP MODULE



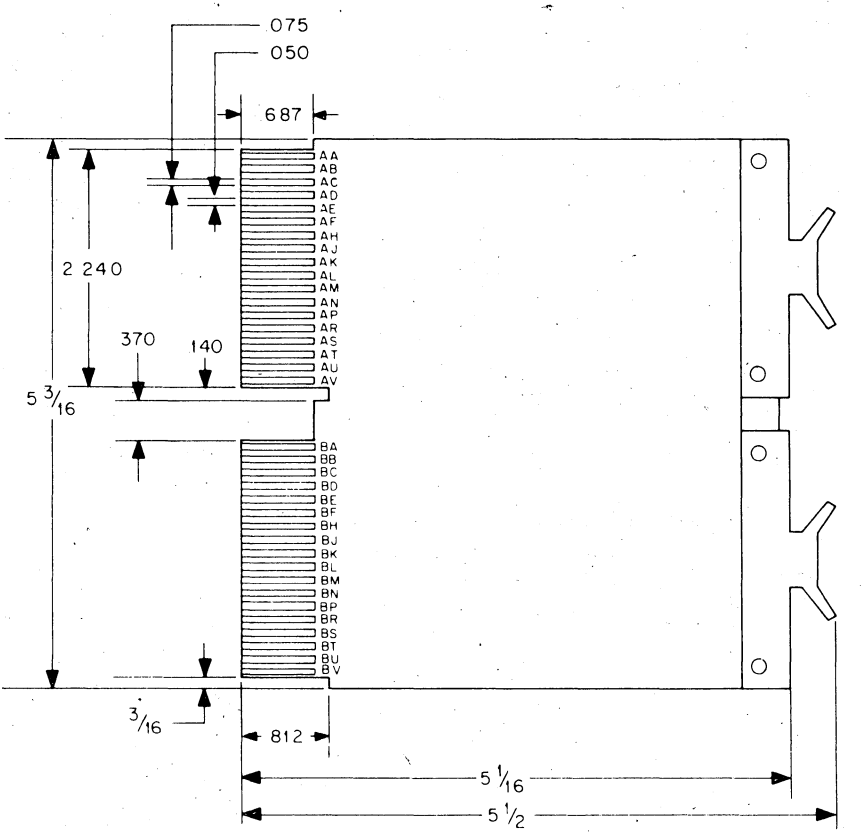
SINGLE-HEIGHT FLIP CHIP MODULE



DOUBLE-WIDTH FLIP CHIP MODULE



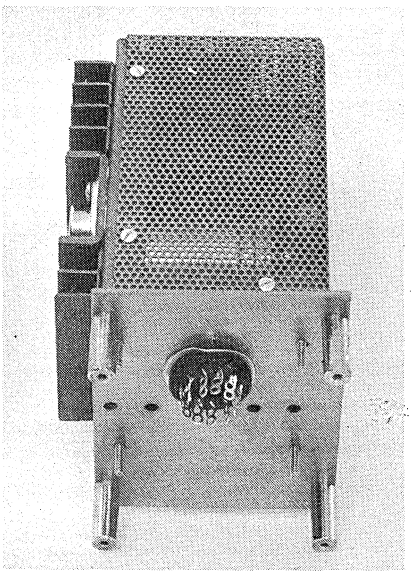
DOUBLE-HEIGHT FLIP CHIP MODULE



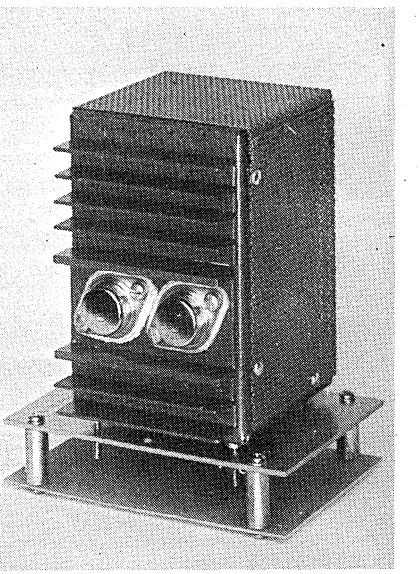
All incoming integrated circuits undergo computer controlled testing, with 40 dc and 16 ac tests performed in 1.1 seconds. This 100% inspection speeds production by minimizing the diagnosis of component failures in module test.

DUAL POWER SUPPLY
H704, H707
±15 Volts

POWER SUPPLY



H704



H704

These supplies differ only in dimensions and output current capabilities: 400 ma and 1.5 Amperes respectively for the H704 and H707. May be mounted on the bars in an H920 drawer, taking the space of two connector blocks.

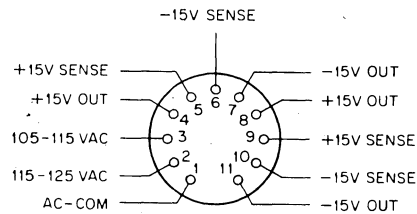
MECHANICAL CHARACTERISTICS

DIMENSIONS: 3¼ x 3⅜ x 5 in. height (H704)
DIMENSIONS: 4" x 5" x 5½" height (H707)
CONNECTIONS: All input-output wires must be soldered to octal socket at the base of the power supply.
OPERATING TEMPERATURE: —20 to +71°C ambient

H704 — $200
H707 — $400

ELECTRICAL CHARACTERISTICS

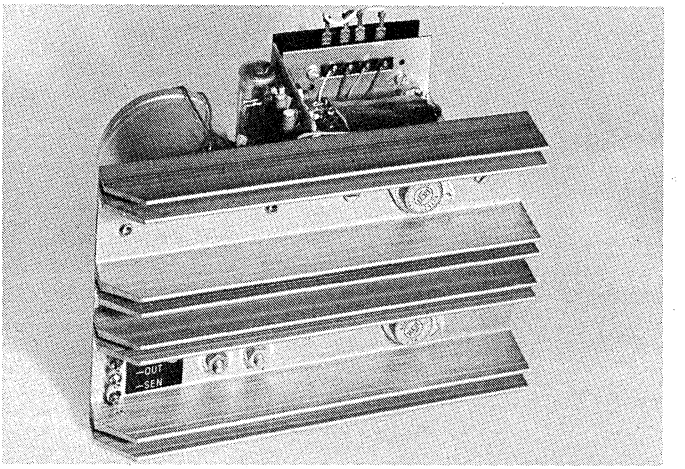
INPUT VOLTAGE: 105 to 125 vac; 47-420 cps.
OUTPUT VOLTAGE: floating ±15v
OUTPUT VOLTAGE ADJUSTMENT: ±1v each output
REGULATION: 0.05% line, 0.1% load for both voltages
RIPPLE: 1 mv rms max for both outputs
OVERLOAD PROTECTION: The power supply is capable of withstanding output short circuits indefinitely without being damaged.
IF REMOTE SENSING IS NOT USED, CONNECT: 5 TO 4
6 TO 7



IF REMOTE SENSING IS NOT USED CONNECT: 5 TO 4
6 TO 7
8 TO 9
10 TO 11

WIRING: Digital/analog and analog/digital converters perform best when module locations and wiring are optimized. All Digital-Analog Converter modules should be side-by-side, with Type 932 bus strip used to bus pins E and pins F on all converter modules. In an analog-digital converter, the comparator should be mounted next to the converter module for the bits of most significance. The reference supply module should be mounted nearby, and if the A704 is used, its sense terminals should be wired to pins E and F of the most-significant-bits converter module. The high quality ground must be connected to the common ground only at pin AC of the reference supply module, and this point should also be the common ground for analog inputs to analog-digital converters. Do not mount A-series modules closer than necessary to power supply transformers or other sources of fluctuating electric or magnetic fields.

POWER SUPPLY
H710



The H710 power supply is ruggedly built, low cost, regulated, floating output, five volt power supply that can be mounted in an H920 chassis drawer or used as a free standing unit. Remote sensing to correct for loss due to long lines is provided. When shipped from the factory, the remote sensing inputs are jumpered to their respective outputs. Especially useful in systems that require maximum repeatability from K303 timers in the millisecond region.

INPUT VOLTAGE: 105-125 VAC or 210-250 VAC 47-63 HZ

OUTPUT VOLTAGE: 5 vdc.

P-P RIPPLE: Less than 20 mv.

OUTPUT CURRENT:
0-5 amps. shirt-circuit protected for parallel supply operation.

LINE AND LOAD REGULATION:
The output voltage will not vary more than 50 mv over the full range of load current and line voltage.

OVERVOLTAGE PROTECTION:
The output is protected from transients which exceed 6.9 Volts for more than 10 nsec. However, the output is not protected against long shorts to voltages above 6.9 Volts.

POWER CONNECTIONS:
Input power connections are made via tab terminals which fit the AMP "Faston" receptacle series. Output power is supplied to solder lugs. All required mounting hardware is supplied with this unit. See 914 power jumpers.

Length: 8"
Width: 5"
Height: 6"
Finish: Chromicoat

H710 — $200

POWER SUPPLY
H716

POWER SUPPLY

Type H716 provides +5 volts at 4 amperes and —15 volts at 1.5 amperes with over voltage protection for +5 volts. This dual voltage power supply is designed to be mounted at the right end of any mounting panel which incorporates the Type H021 mounting frame. The supply is mounted by using the four holes in the Type H021, therefore the right end plate cannot be used when a Type H716 supply is mounted. The supply takes 2 connector blocks of Type H800, H803, or H808. This provides 48 module slots with Types H800 and H803, 24 slots with Types H800 and H803 and 24 slots when Type 808 is used.

MECHANICAL CHARACTERISTICS

Maximum Dimensions 5¼ x 4⅛ x 12 deep

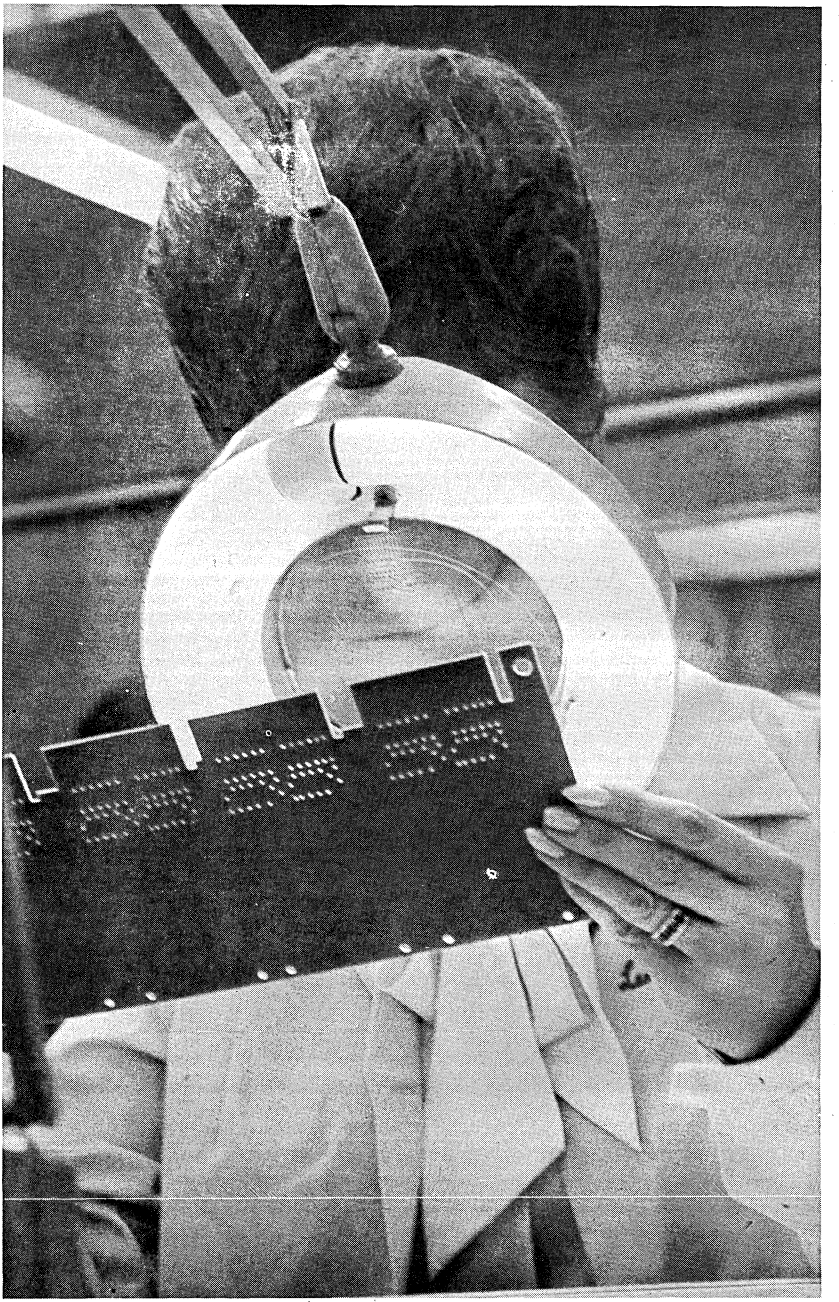
Power input via Amphenol 160-5 or equivalent connector with an Amphenol 160-5 or equivalent, in parallel.

Low voltage connections are by slip on terminals.

ELECTRICAL SPECIFICATIONS

Input:	120/240 vac ± 10%, 47-63 HZ. Normally supplied wired for 120v. For 240 volts change transformer tap connections.
Output 1:	+5v, adjustable from 4.5 to 5.5 volts at 4 amperes maximum. Line-Load-Ripple total regulation ±3%.
Output 2:	—15v ±5% at 1.5 amperes, maximum. Line-Load-Ripple total regulation ±5%.
Temp. Range:	Above specifications are over a range of 0-50°C.

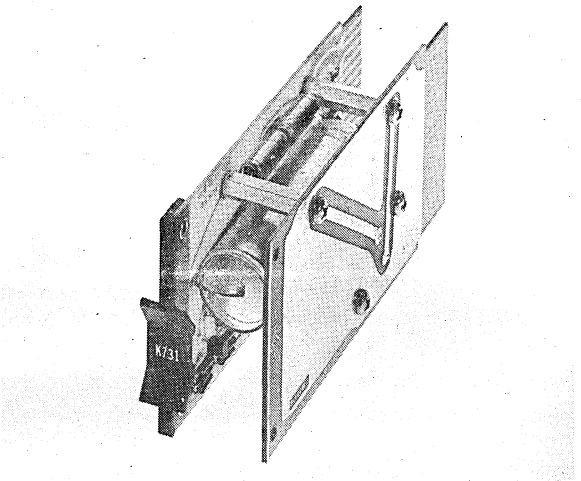
H716 — $130

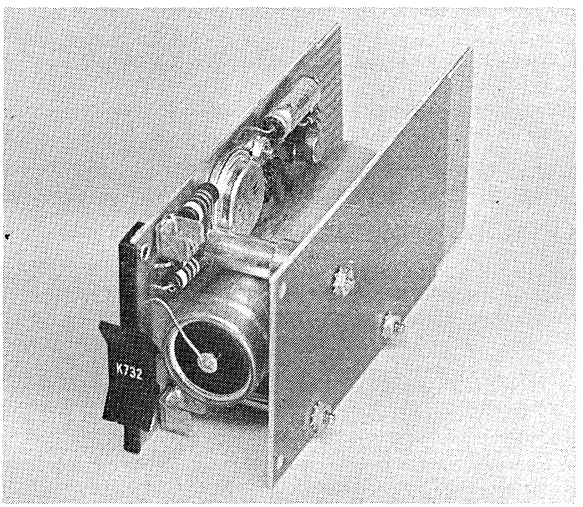


Quality of plated-thru holes is checked in our new electrochemical facility before boards go to the module assembly area.

POWER SOURCE MODULE
K731
SLAVE REGULATOR
K732

HARDWARE



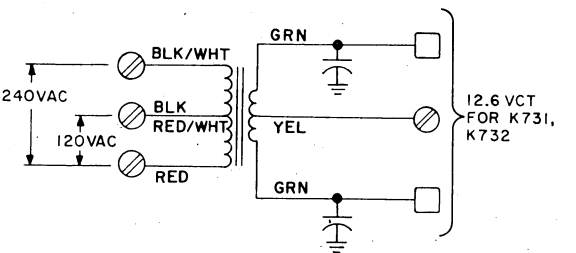


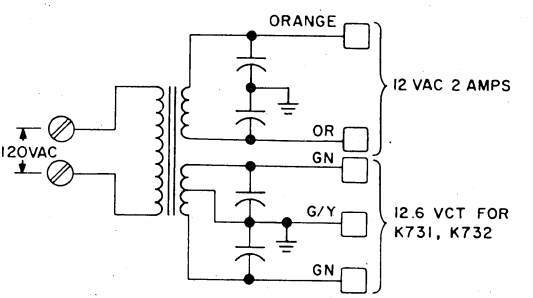
One K731 plus up to 3 K732 can provide from 1 to 7 amperes at +5v. Consult K Series text for additional characteristics and hook up information.

K731 — $24
K732 — $27

POWER TRANSFORMERS
K741, K743

POWER SUPPLY



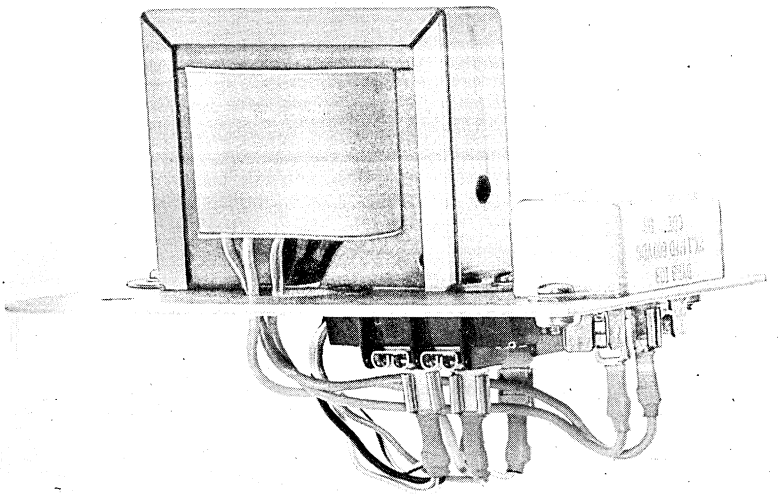


These hash-filtered, 50/60 Hz transformers supply K731 Source and K732 Slave Regulator modules. The K743 also provides an auxiliary winding for use with K580 Dry Contact Filters and K681 or K683 Lamp Drivers (requires additional bridge rectifier). Type 914 Power Jumpers are convenient for connecting to tab terminals on these transformers and on the K732 and K943. Both transformers have holes at the corners of the chassis plate for mounting on K980 endplates:

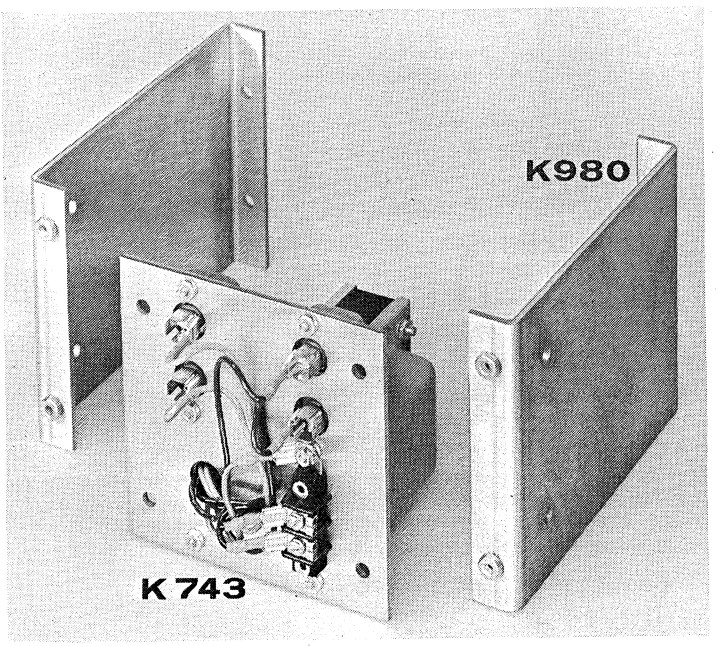
	PLATE DIMENSIONS	HOLE CENTERS MATCHING K980	Ctrs.
K741	3½" x 5"	2½" x 3⅜"	2½"
K743	5" x 5"	4" x 3⅜"	4"

The K741 is sufficiently light in weight to be mounted on one side only, as at the end of a K943 mounting panel.

K741 — $22
K743 — $38



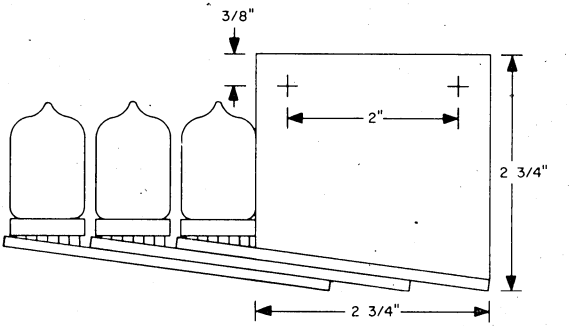
K741



K743

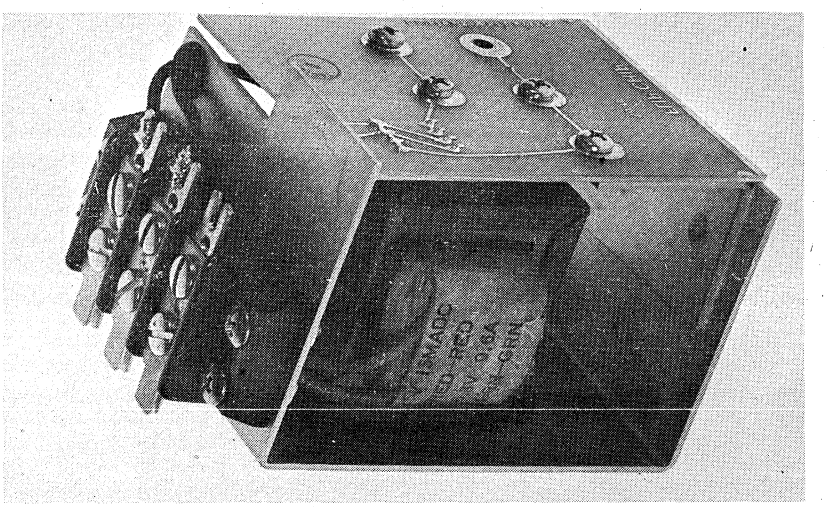
DISPLAY SUPPLY
K771

POWER SUPPLY



(SHOWN WITH 3 K671'S)

Shown above from the viewing side, the K771 supplies power and a convenient two-screw mounting for up to 6 K761 display tubes. Display tubes are stacked to the left, the first tube board being attached to the K771. The second tube board attaches to the first, and so on. Board mouning screws provide both mechanical mounting and electrical power connections. The two panel mounting screw locations dimensioned above have no. 6 steel threaded inserts. Several 1" holes using a standard chassis punch may be cut on 0.8" centers for viewing display tubes. To seal opening against dust, a 3" by 3-6" piece of Lucite® or Plexiglas® may be assembled between display and mounting surface. Power 120 VAC enters the supply from a terminal strip at the rear. Total depth behind mounting surface: 4".

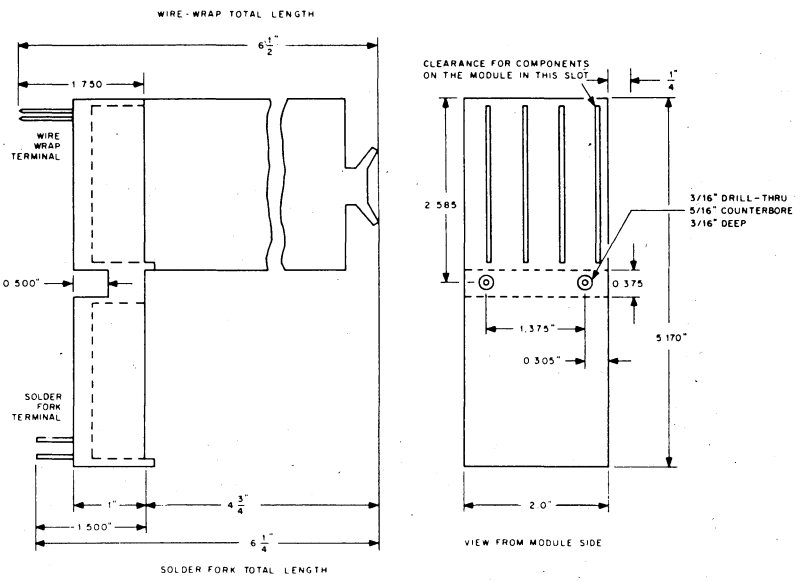


K771 — $26

CONNECTOR BLOCKS
H800-W, H800-F

HARDWARE

This is the 8-module molded socket assembly used in FLIP CHIP mounting panels. Aside from its function as a replacement part, there may be times when a special mounting fixture with one or more H800 blocks must be made by a manufacturer who wishes to fit a few modules into a confined or irregular space. The drawings below show the pertinent dimensions.



REPLACEMENT CONTACTS TYPES H801-W, H801-F

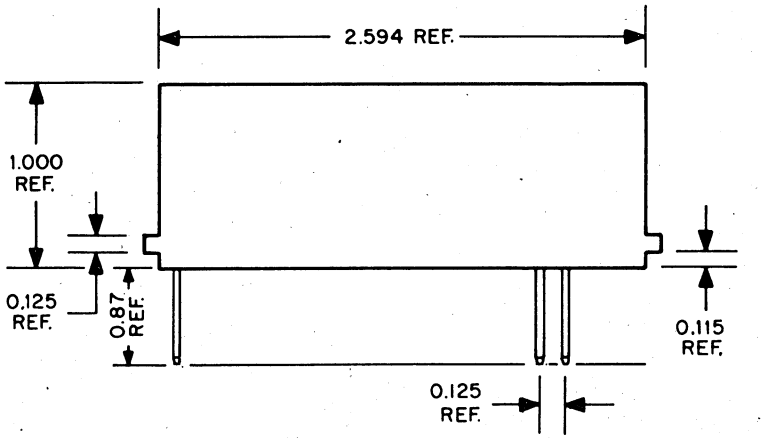
These contacts are offered in packages of 18 for replacement purposes. In each package, nine straight and nine offset contacts are included, enough to replace all contacts in one socket.

H801-W is for wire-wrap connectors; H801-F is for solder-fork connectors.

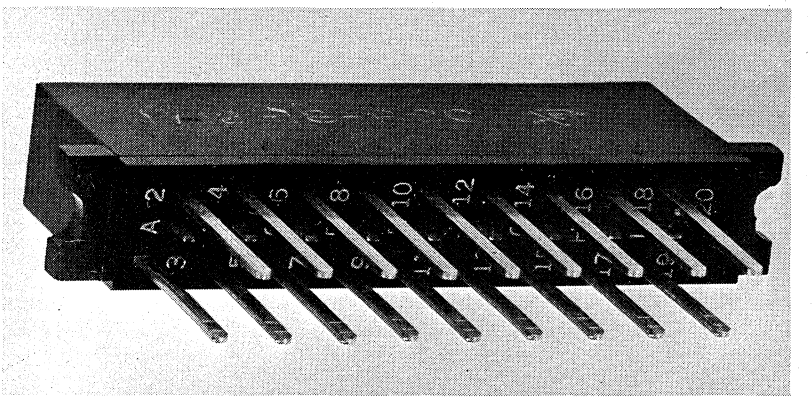
H800F — $8
H800W — $8
H801F — $2
H801W — $2

CONNECTOR BLOCK
H802

HARDWARE

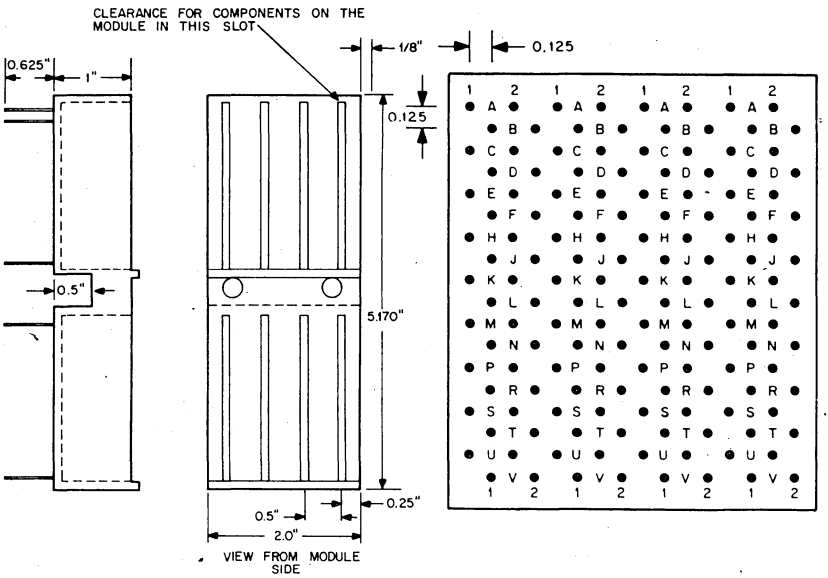


This is an 18 pin connector block for a single flip-chip module. The H802 can be used to fit a single module in a confined or irregular space. Often the H802 is used as a connector for a cable at some remote location. The H802 is only available with wire wrap pins.



H802 — $4

CONNECTOR BLOCK
H803, AND H805 PINS



The H803 is the 8-module molded Jacket Assembly used in the H910 and H911 mounting panels. For each of the eight modules, it provides a 36-pin connector with the wirewrap pins forming a 0.125-inch staggered grid as shown above. This connector is designed to be used with M Series modules; however, it can also be used with all other series listed in this handbook.

The blocks have the same physical dimensions as the H800 with the exception of pin length. These blocks are only available with wire wrap pins which are designed to be wrapped with number 30 wire. Pin dimensions are 0.025 inches square. W&K Series 18 pin modules will make contact with only the 2-side pins (A2, B2, etc.).

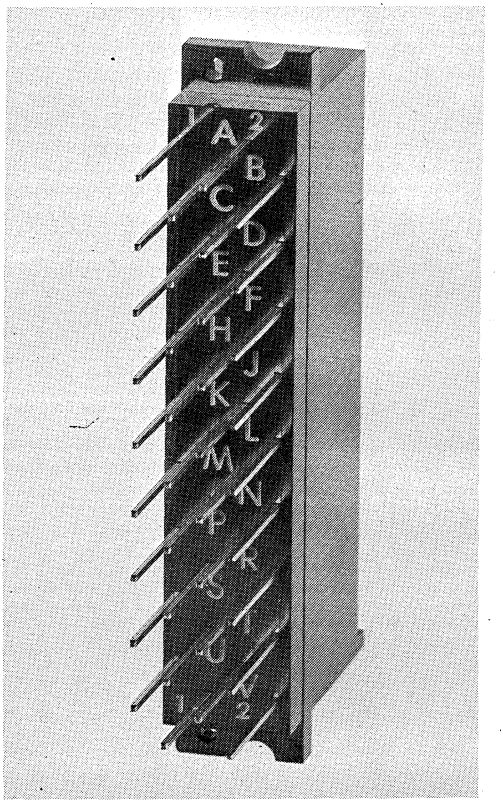
H805 is a package of 36 pins (18 left and 18 right) to be used as replacements in H803 blocks. Three types are available depending on the manufacturer of Type H803 whose name or symbol is found on the connector mounting block. For ordering purposes specify letter code as shown below: H805

A—Amphenel
C—Cinch
S—Sylvania

H803 — $13
H805 — $4

CONNECTOR BLOCK
H807

HARDWARE

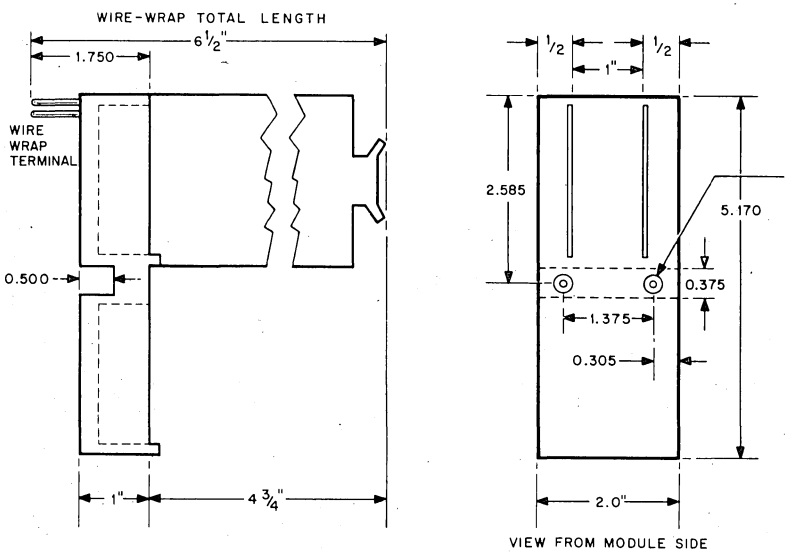


This is a 36 pin single slot connector. It is provided for M-Series modules but can be used with modules or connector boards in the K and W Series. Uses include mounting in confined or irregular spaces. Often the H807 is used to terminate a connector board at a remote location. The H807 is available only with wire wrap pins.

H807 — $5

CONNECTOR BLOCK
H808, H809 PINS

HARDWARE



The H808 is a relatively low density connector block for use with all modules in the catalog. This includes A, K, M, and W Series modules. The connector provides 4 module slots each having 36 pins. On A,K and W Series modules only the 2 side pins, (A2, B2, etc.) will make contact. This connector adds a measure of convenience and versatility to the many uses to which these catalog modules can be applied. Hand wiring of connector pins is more easily accomplished for M Series prototype work. H800 and H808 connector blocks can be mixed for M and A, K, W module mixing purposes. Wire wrapping patterns can be maintained even though module letter series are mixed because H800 & H808 pin layout is identical. H809 is a package of 36 replacement pins, 18 left and 18 right.

H808—$10
H809—$ 4

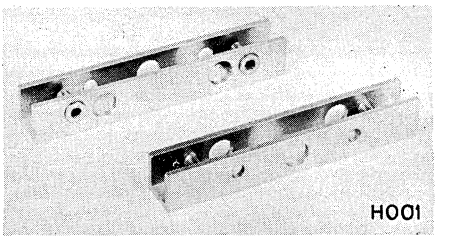
MOUNTING PANEL HARDWARE
H001, H002, H020, H021, H022

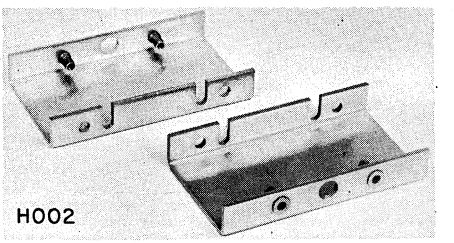
Pairs of brackets. H001 provides ¾" standoff to mount 1907 over K943 wiring. H002 provides a 2" setback so a control panel with switches, lamps, etc. can be mounted flush with mounting rack or cabinet in front of logic wiring.

The H020 consists of a mounting frame casting. Components which can be mounted on this frame include, H800, H803, H808 connector blocks, power supplies such as H710 and others or customer components that are adapted to the frame mounting requirements.

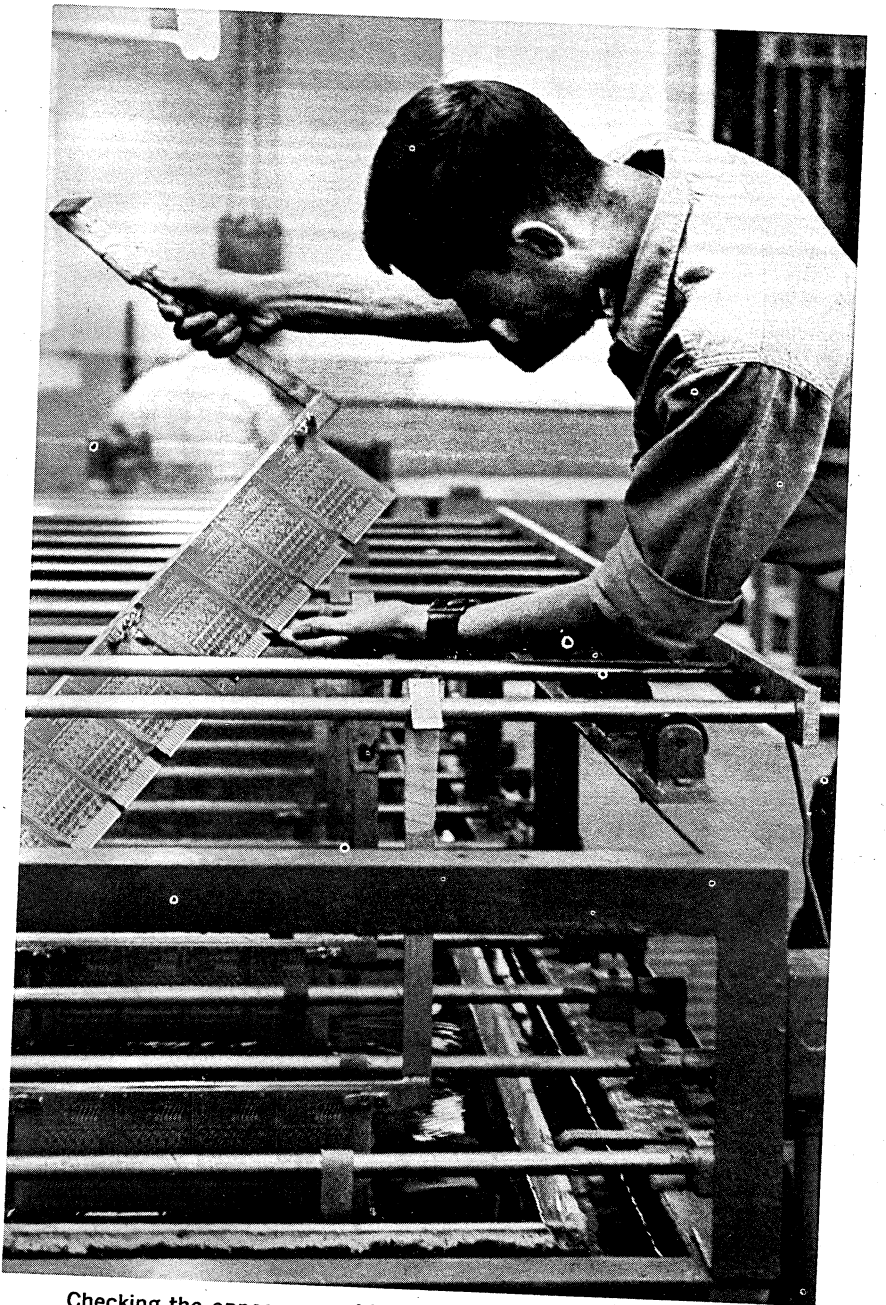
The H021 consists of a pair of offset end plates which mount to the H020.

These end plates provide a mount for the 1945-19 hold down bar, if required. H022 consists of a pair of end plates similar to H021 but provide a terminal block assembly for ease of parallel power wiring of adjacent panels.


H001


H002

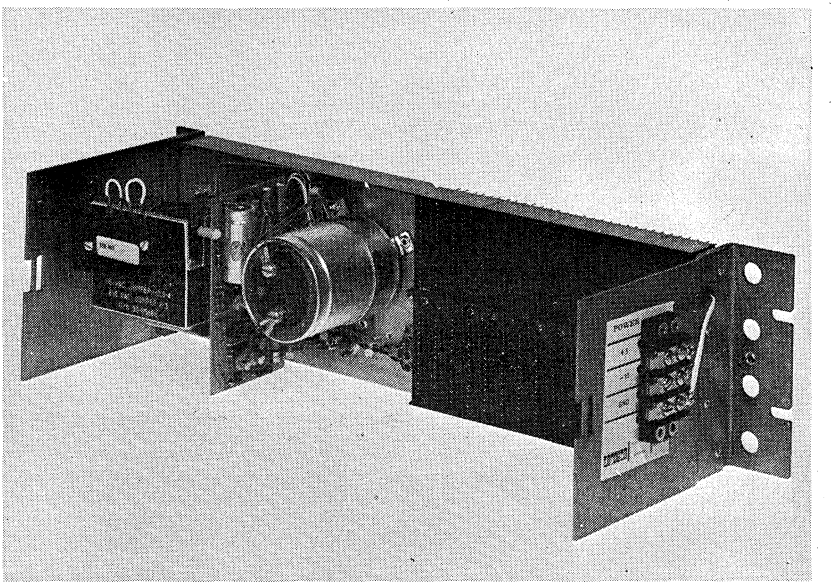
H001-PR — $8
H002-PR — $8
H020 — $15
H021 — $7
H022 — $20

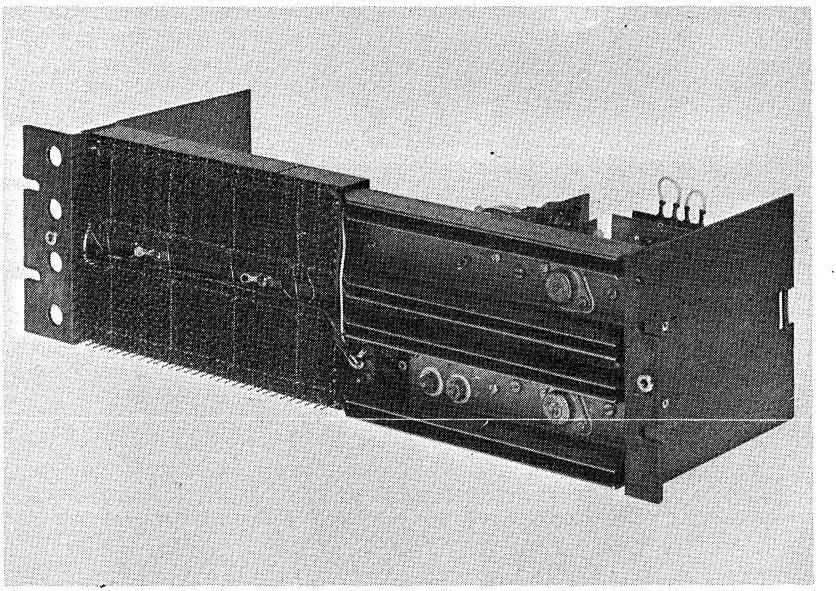


Checking the appearance of board contacts being gold-plated. Our 100 micro-inch plating is verified by periodic checking on a radiation gauge.

MOUNTING PANEL
H910

HARDWARE





This dual function mounting panel offers a way to build complete digital systems of up to 32 FLIP CHIP modules into only 5¼ in. of rack space. More power is available than is ever likely to be consumed in a 32 module system. Power in excess of that required for 32 modules can be obtained at the terminal block which si convenient to the input terminal block on any adjacent H911 or 1943 mounting panel.

The H910 panels are built from four H803 connector blocks and a 5 volt regulated supply. Wire wrap connectors for 30 awg wire only are present on the H910. The panel will hold 32, 36 pin modules. In addition, the panel is bussed with 933 bus strips on pins A2, C2, and T1 and all power wiring to the supply is connected. Power in excess of that required for the 32 modules can be obtained at the terminal block which is convenient to the input terminal block on any adjacent H911 mounting panel, generally used for M series modules.

ELECTRICAL CHARACTERISTICS

INPUT VOLTAGE:
105-125 VAC or 210-250 VAC
47-63 HZ
OUTPUT VOLTAGE:
5vdc

OUTPUT CURRENT:
0-5 amps. short-circuit protected for parallel supply operation

OVERVOLTAGE PROTECTION:
The output is protected from transients which exceed 6.9 volts for more than 10 nsec. However, the output is not protected against long shorts to voltages above 6.9 volts.

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19 in.
PANEL HEIGHT: 5$\frac{3}{16}$ in.
DEPTH: 16¾ in.
FINISH: Chromicoat
POWER INPUT CONNECTIONS:
Screw terminals

vided on transformer
MODULES ACCOMMODATED: 32
POWER OUTPUT CONNECTIONS:
Barrier strip with screw terminals and tabs which fit AMP "Faston" receptacle series 250, part no. 41774 or Type 914 power jumpers.

1945-19 HOLD DOWN BAR: Reduces vibration and keeps modules securely mounted when panel or system is moved. Adds ½ in. to depth of mounting panel.

Consult following table for option and ordering information.

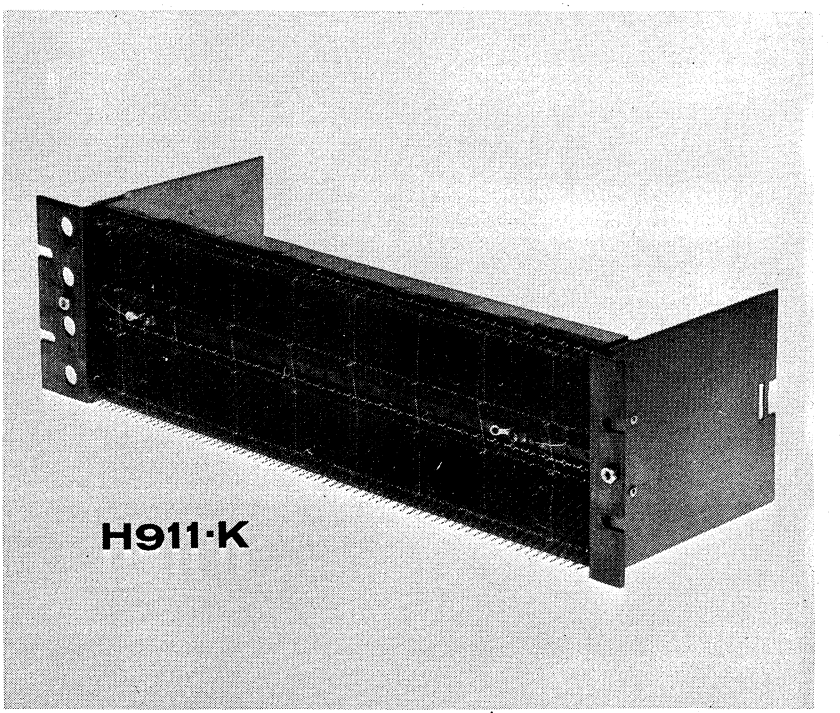
MOUNTING PANEL
H911 J, H911-K

HARDWARE

The H911 mounting panel uses eight H803 connector blocks and houses sixty four, 36 pin connectors. Mechanical dimensions are identical to those of the H910. The H911 is available with wire wrap pins only. Power wiring options are available on the H911. Generally used for M series modules.

933 BUS STRIP—For H911 mounting panel, makes wiring power and register pulse busses easy.

Consult following table for option and ordering information.



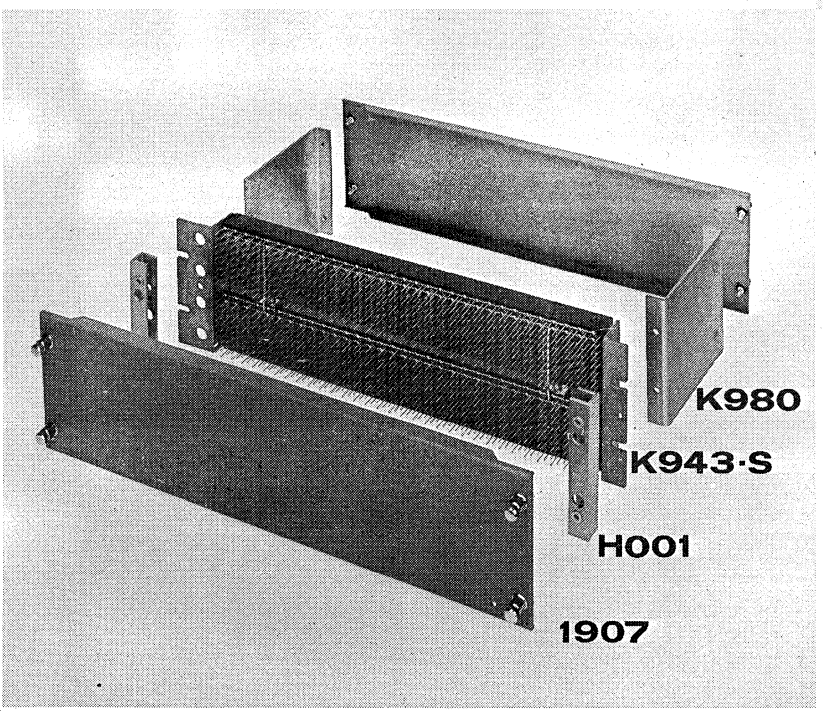
H911J—$151
H911K—$161

19" MOUNTING PANEL
K943-R, K943-S

HARDWARE

These low cost, 19" panels have 64 sockets with either wire-wrap (W) or solder fork (F) contact pins. Shipped with connector blocks installed and pins A and C bussed.

No terminal strips are included in the K943, since power regulators K731 and K732 will normally be plugged in to make power connections. If hold-down is required to prevent modules from backing out under vibration, order a pair of end plates K980. These assemble by means of added nuts on the rear of the rack mount screws. They accept the painted 1907 cover plate, making a hold-down system that contacts the module handles and can allow flexprint cables to be threaded neatly out the end. Rack space: 5¼". See photos showing K943-S, K980, 1907, and H001.



K943R—$96
K943S—$96

MOUNTING PANEL
H913, H914, H916 & H917

HARDWARE

This panel houses a 5v regulated supply and four low density H808 connector blocks. This allows 16 of either A,K,M, or W series modules to be used. Electrical and mechanical characteristics are like those of type H910.

This panel houses 8 low density H808 connector blocks. The panel will hold 32 of either A,K,M, or W series modules. It can be used for expanding slot capacity in conjunction with H913 or alone using other options of voltage supply, e.g. K731 K732 combinations. Mechanical characteristics are like those of H911.

This panel incorporates an H020 frame on which is mounted an H716 power supply and 6 H803 (green) connector blocks. This provides 48 36 pin module slots. Although generally used for mixes of M and A series modules K and W series modules can also be accommodated.

This panel is similar to H916 except 6 low density H808 connector blocks are supplied. With this connector block 24 module slots are available allowing the use of either of the module series. Electrical and mechanical characteristics are similar to those of Type H916 with the exception of the connector block pins.

H913—$270
H914—$125
H916—$270
H917—$260

TABLE OF MOUNTING PANELS WITH & WITHOUT POWER SUPPLY

NA = Not Available.

ORDER NO.			AVAILABLE VARIATIONS				PRICE
Panel	Order Letter	Power Option	F	W	B	P	
H910	K	V	NA	X	X	X	$280
H911	J	X	NA	X	X		$151
H911	K	X	NA	X	X	X	$161
H913	L	V	NA	X	X	X	$270
H914	L	X	NA	X	X		$125
H916	M	V	NA	X	X	X	$270
H917	N	V	NA	X	X	X	$260
K943	R	X	X			X	$ 96
K943	S	X		X		X	$ 96

X = NO POWER

V = 105-125 VAC
OR 210-250 VAC
47-63 Hz.

PREWIRED POWER
(extra cost option)
Omit P if not desired.

CONNECTOR
W—for wire-wrap
F—for forked solder connectors

POWER CONNECTION
B—Power input via terminal block. Both conventional screw connections and taper tabs can be used.

Example Order: H911KX
This describes a Type H020 casting with 8 Type H803 wrie wrap connectors and ground wired to a terminal block incorporated into the end plate assembly.

END PLATES
K980

HARDWARE

Pair of plates for supporting 1907 cover to hold modules in K943 panel under shock and vibration. (Note: If vibration is anticipated, care must be taken not to nick logic wires. Use a quality wire stripping device.) Also used for mounting K741, K743, K782, K784.

K980—$6

COVER
1907

HARDWARE

Blue painted or brown tweed painted aluminum cover with captive screws to mate threaded bushings in K980 and H001. Adds to appearance while protecting system against vibration and tampering.

1907 — $9

MODULE DRAWER AND ACCESSORIES
H920, H921, H923

The H920 Module Drawer provides a convenient mounting arrangement for a complete digital logic system. The drawer has sufficient room to house up to 20 mounting blocks in addition to the H710 power supply. The power supplies not included in the H920 but must be ordered separately. When used without the power supply, there is room for up to 24 mounting blocks. The drawer accepts both H800 and H803 mounting blocks and fits a standard 19" relay rack and all DEC cabinets. Width of the module drawer is 16¾" and depth is 19". When used with the H921 Panel, the height is 6¾". The module drawer comes equipped with a power bracket for distribution of power within the drawer, to other drawers or to mounting panels. The H920 comes with convenient mounting arrangements for both the H921 front panel and the H923 slide tracks. The H921 is a front panel designed to be used primarily with the H920 Module Drawer. It provides convenient mounting arrangements for switches, indicators, and other accessories which may be required in a logic system. The H921 comes pre-drilled and ready to mount to the H920. Height of the panel is 6¾" and width is 19".

The H923 chassis slides are designed to be used with the H920 Mounting Drawer. These slides allow the user to slide the drawer out of the cabinet or rack and tilt the drawer to any angle. H923 tracks may also be ordered directly from Chassis Trak, Inc., Indianapolis, Indiana, part number CTD 120.

H920 — $170.00
H921 — $ 5.00
H923 — $ 75.00

MODULE DRAWER
H925

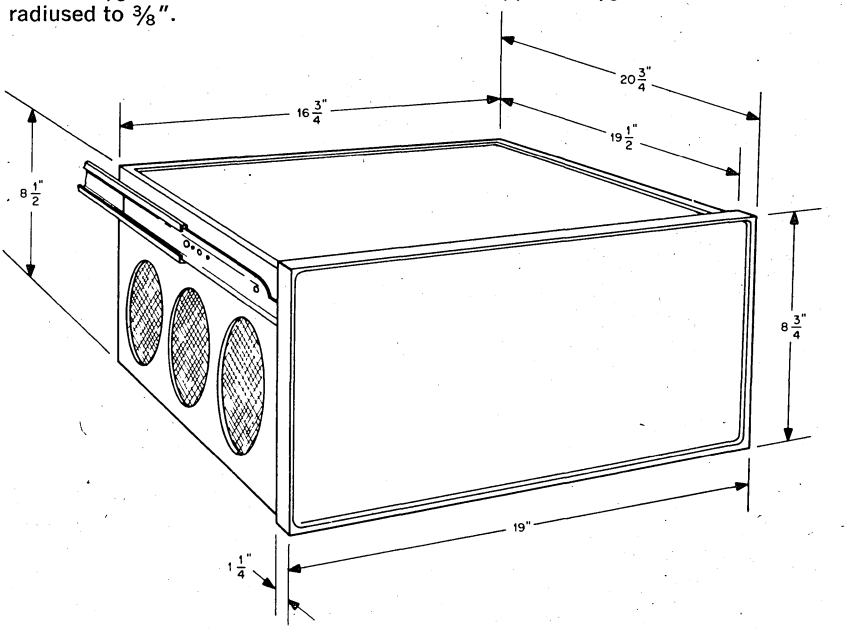
HARDWARE

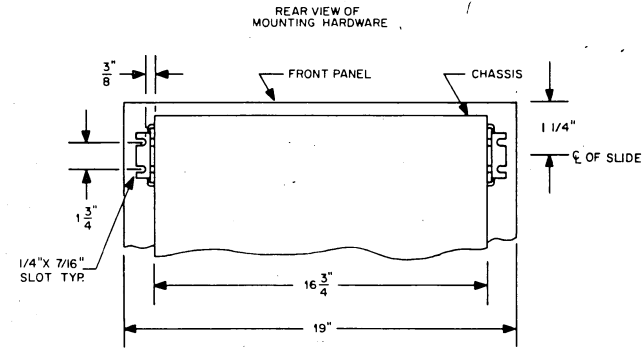
This enclosure provides mounting space for up to 18 H800 or H803 connector blocks accommodating as many as 144 M or K series modules. The H808 one-half density connector may also be used for an accommodation of 72 M series modules. The connector blocks mount pins-upward for easy access during system checkout.

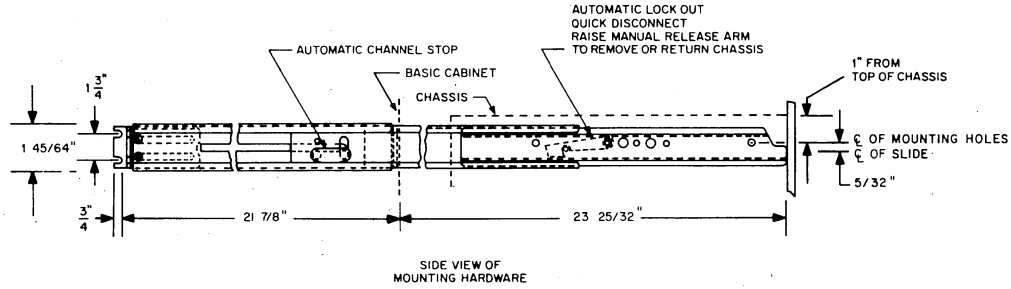
Three axial flow fans are provided and are mounted internally on the right side of the enclosure to provide cooling air flow across mounted modules and through the power supply area.

A 3¾" wide, 7¾" high, 18¾" deep space is provided in the left side portion of the enclosure for power supply mounting or other purposes. Any assembly mounted in this space should be designed in such a manner as to not obstruct the air flow from passing on through the three screened openings in the left side of the enclosure. Two non-tilting slides, similar to Grant type SS-168-NT are provided for mounting the H925. Mounting height should allow for possible servicing of the enclosure using bottom access.

Cover plates are provided for the top and bottom of the enclosure. The enclosure also includes an attractive bezel and front sub-panel. The sub-panel is manufactured of 16 gage material and is intended for the mounting of front panel controls and other accessories. The bezel allows for the installation of customer supplied dress panel. The dress panel should be manufactured of ⅛" thick material which measures 8¼" x 18⅜" with the corners radiused to ⅜".




REAR VIEW OF
MOUNTING HARDWARE
3/8"
FRONT PANEL
CHASSIS
1 1/4"
℄ OF SLIDE
1 3/4"
1/4"X 7/16"
SLOT TYP.
16 3/4"
19"


AUTOMATIC LOCK OUT
QUICK DISCONNECT
RAISE MANUAL RELEASE ARM
TO REMOVE OR RETURN CHASSIS
AUTOMATIC CHANNEL STOP
BASIC CABINET
CHASSIS
1" FROM
TOP OF CHASSIS
1 3/4"
1 45/64"
℄ OF MOUNTING HOLES
℄ OF SLIDE
5/32"
3/4"
21 7/8"
23 25/32"
SIDE VIEW OF
MOUNTING HARDWARE

H925 — $325

WIRING ACCESSORIES

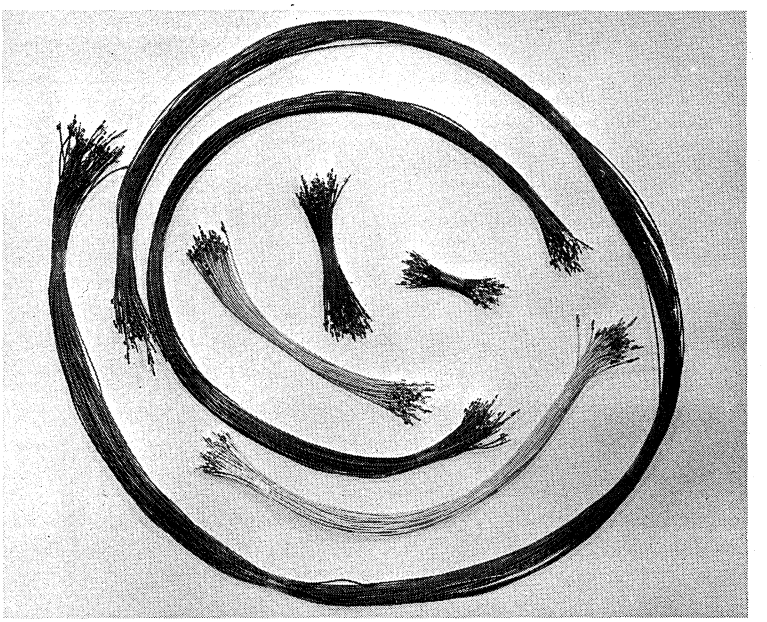
913, 914, 915, 917
H820, H821, H825, H826

913 AND 915 PATCHCORDS

These patchcords provide slip-on connections for FLIP CHIP mounting panels and are available in color-coded lengths of 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, and 64 inches. All cords are shipped in quantities of 100 in handy polystyrene boxes. Type 913 patchcords are for 24 gauge wirewrap and use AMP Terminal Type #60530-1. Type 915 patchcords are for 30 gauge wirewrap and use AMP Terminal Type #85952-3.

H820 AND H821 GRIP CLIPS FOR SHIP-ON PATCHCORDS

The type H820 and H821 GRIP CLIPS are identical to slip-on connectors used in respectively the 913 and 915 patchcords. These connectors are shipped in packages of 1000 and permit fabrication of patchcords to any desired length. H820 GRIP CLIPS will take size 24-20 awg. wire and may be purchased from AMP, Inc. as AMP part #60477-2. H821 GRIP CLIPS will take size 30-24 awg. wire and are AMP part #85952-3.

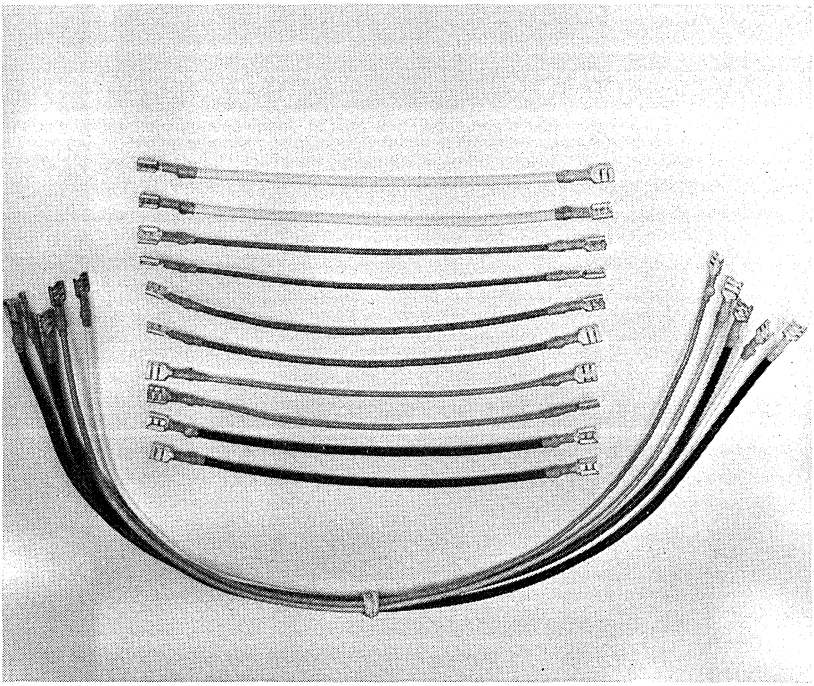


H825 HAND CRIMPING TOOL

Type H825 hand crimping tool may be used to crimp the type H820 GRIP CLIP connectors. Use of this tool insures a good electrical connection. This tool may also be obtained from AMP, Inc. as AMP part #90084.

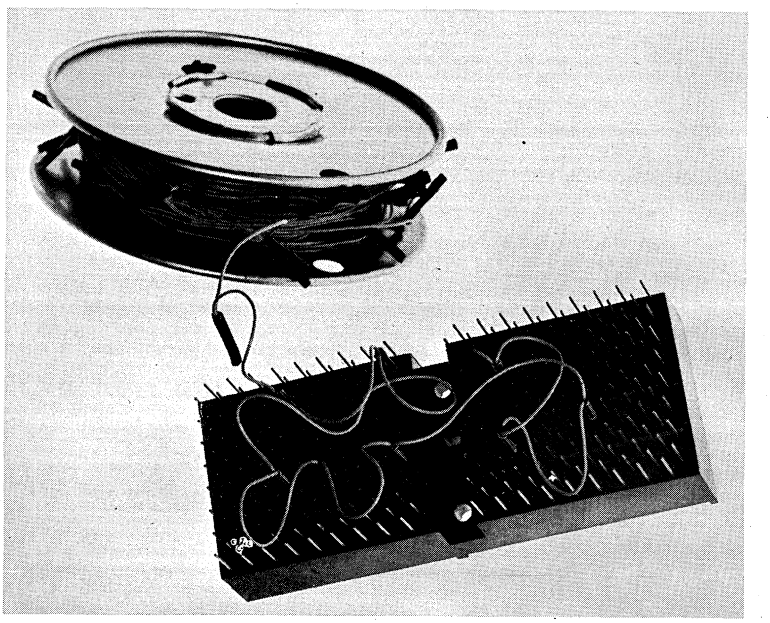
H826 HAND CRIMPING TOOL

Type H826 hand crimping tool may be used to crimp the type H821 GRIP CLIP connectors. This tool is identical to AMP part #9019-1.



914 POWER JUMPERS

For interconnections between power supplies, mounting panels, and logic lab panels, these jumpers use AMP "Faston" receptacles series 250. Specify 914-7 for interconnecting adjacent mounting panels, or 914-19 for other runs of up to 19 inches. 914-7 contains 10 jumpers per package; 914-19 contains 10 jumpers per package.



917 DAISY CHAIN

Type 917 is a continuous length of unbroken #25 AWG stranded wire. 250 gold plated and insulated terminals are crimped at predetermined intervals on each reel. In conjunction with type H803 or type H807 connector blocks and M Series modules, hand patch wiring of prototype systems is easily and quickly accomplished. All that is required is a reel of type 917 Daisy Chain and wire cutters. These dependable push on connections are also easily removeable making this wiring technique ideal in cases where wiring and unwiring for changing systems needs is required. If ever a third lead is necessary a type 915 patchcord can be used if placed on the pin before the Type 917 termination. Two contact spacings available at 2½" or 5".

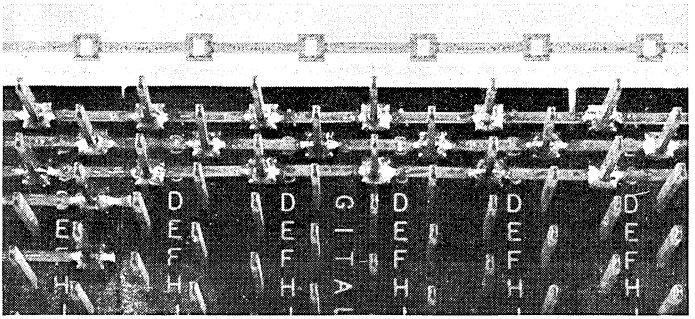
917 — 2.5 — blue
917 — 5 — white

Also available from:
Berg Electronics
New Cumberland, Pa. 17070
Tel. (717) 938-6711

913 — $18.00/pkg. of 100
914-7 — $4/pkg.
914-19 — $4/pkg.
915 — $33.00/pkg. of 100
H820 — $48.00/pkg. of 1000
H821 — $75.00/pkg. of 1000
H825 — $146.00
H826 — $210.00

WIRING ACCESSORIES

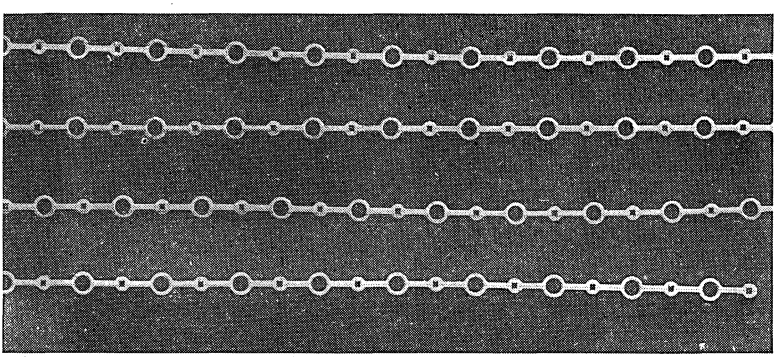
932, 933, 934, 935, 936
H810, H811, H812, H813, H814



932 BUS STRIP

Simplifies wiring of register pulse busses, power, and grounds. Same as used in K943.

932 — $0.60



933 BUS STRIP

Simplifies wiring of power, ground and signal busses on mounting panels using H803 connectors.

933 — $1

934 WIRE-WRAPPING WIRE

1000 ft. roll of 24 gauge solid wire with tough, cut-resistant insulation. (Use Teflon insulated wire instead for soldering.)
For use with H800 connectors.

934 — $50

935 WIRE-WRAPPING WIRE

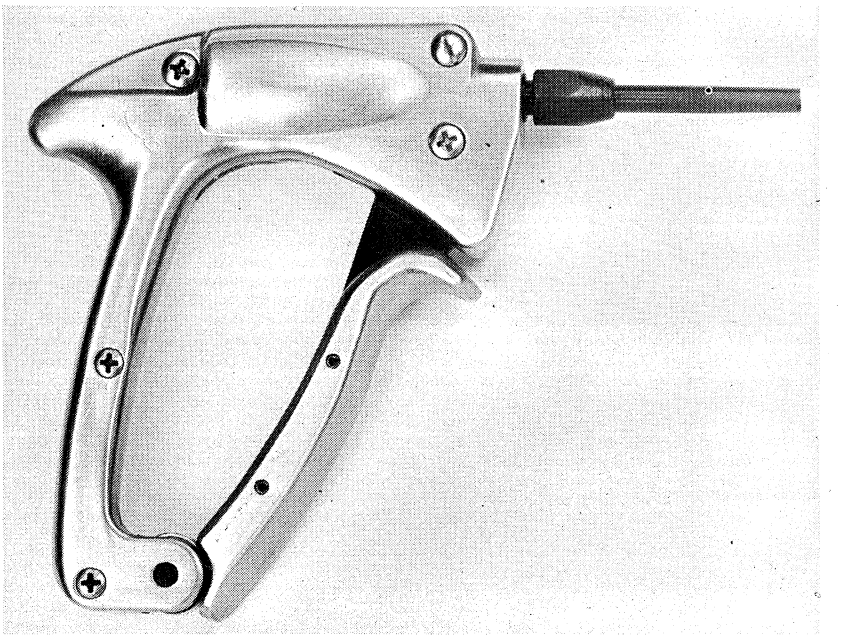
1000 foot roll or 30 gauge insulated solid wire for use with H803 connectors.

935 — $60

936 19 CONDUCTOR RIBBON CABLE

Use on W Series connector modules or split into 9-conductor cables for use with K580, K681, K683, etc.

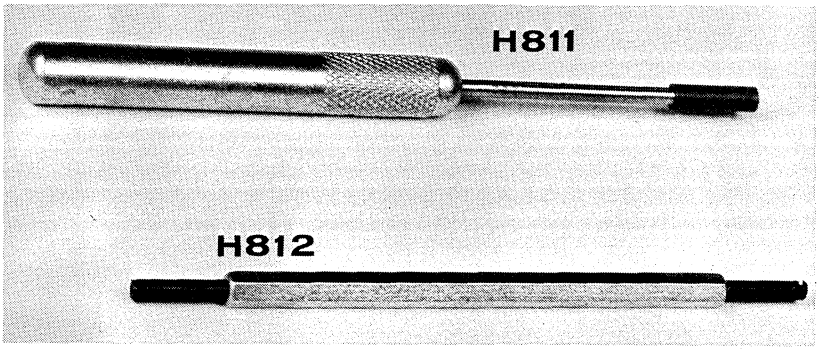
936 — $0.60



H810 PISTOL GRIP HAND WIRE WRAPPING TOOL

The type H810 Wire Wrapping Tool is designed for wrapping #24 or #30 solid wire on Digital-type connector pins. The H810 Kit includes the proper sleeves and bits. It is recommended that five turns of bare wire be wrapped on these pins. This tool may also be purchased from Gardner-Denver Co. (Gardner-Denver part No. 14H-1C) with No. 26263 bit and No. 18840 sleeve for wrapping #24 wire. Specify bit #504221 and sleeve #500350 for wrapping #30 wire. When ordering from Digital specify the sleeve and bit size desired for #24 and #30 wire.

H810(24) — $ 99
H810A — $ 99
H810B — $150



The Type H811 Hand Wrapping tool is useful for service or repair applications. It is designed for wrapping #24 solid wire on DEC Type H800-W connector pins. This tool may also be purchased from Gardner-Denver Co. as Gardner-Denver Part #A20557-12.

Wire wrapped connections may be removed with the Type H812 Hand Unwrapping tool. This tool may also be purchased from Gardner-Denver Co. as Gardner-Denver Part #500130.

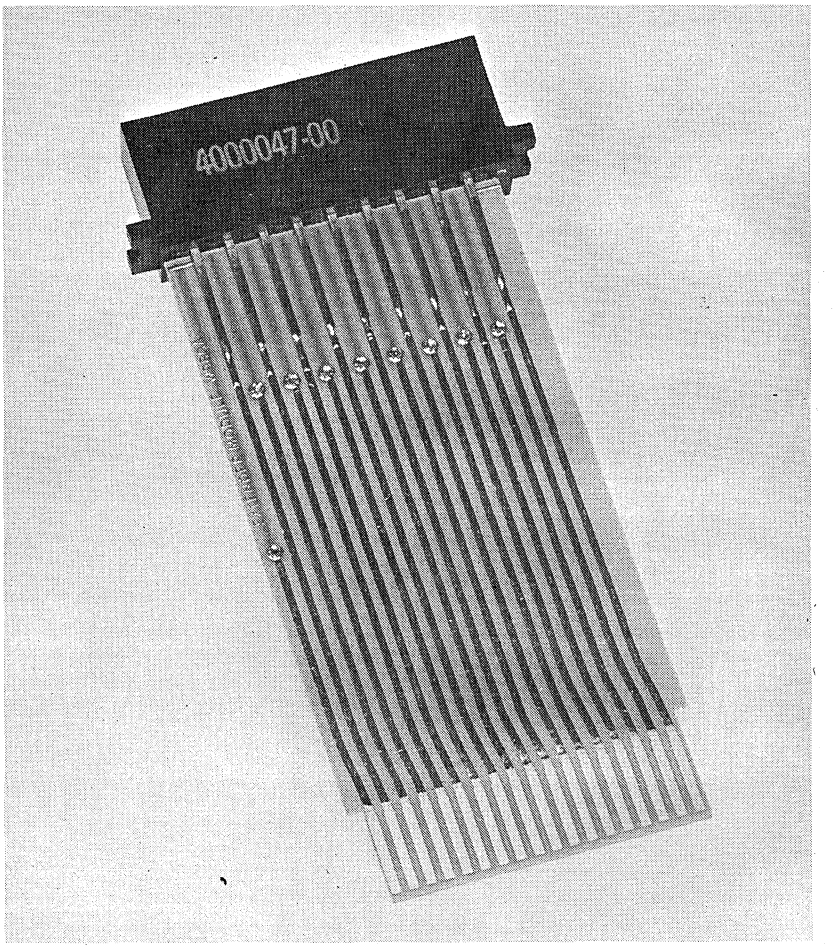
The H811A and H12A are equivalent to the H811 and the H812 except that the A versions are designed for #30 wire. Both tools may be purchased from Gardner-Denver directly under the following part numbers: H811A A-20557-29; H812A 505 244-475. The H813 is a #24 bit; H813A, a #30 bit. The H814 is a #24 sleeve; H814A, a #30 sleeve.

None of the Wire Wrapping Tools will be accepted for credit under any circumstances.

H811(24)	— $21.50
H811A(30)	— $21.50
H812(24)	— $10.50
H812A(30)	— $10.50
H813(24)	— $30
H813A(30)	— $30
H814(24)	— $21
H814A(30)	— $21

MODULE EXTENDER
W980,

HARDWARE



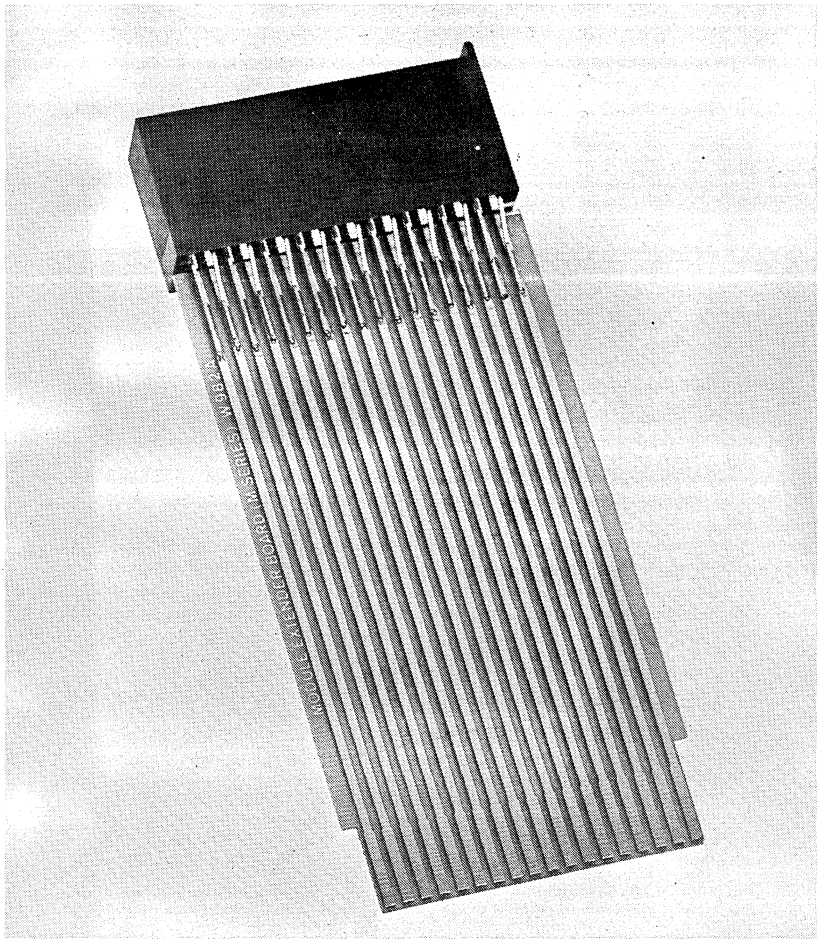
The W980 Module Extender allows access to the module circuits without breaking connections between the module and mounting panel wiring.

For double size flip-chip modules use two W980 extenders side by side. The W980 is for use with A, K and W Series 18 pin modules.

W980 — $14

MODULE EXTENDER
W982,

HARDWARE



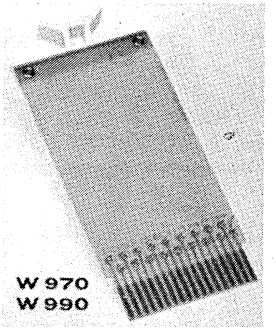
The W982 serves a function similar to the W980 except it contains 36 pins for use with M series modules. The W982 can be used with all modules in this catalog. A, K, and W series modules will make contact with only 2 side pins. A2, B2, etc.

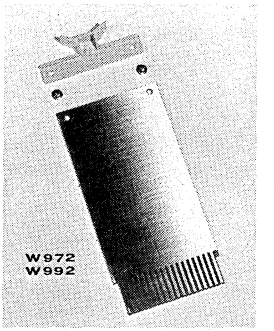
For double size M Series modules use two W982 extenders side by side.

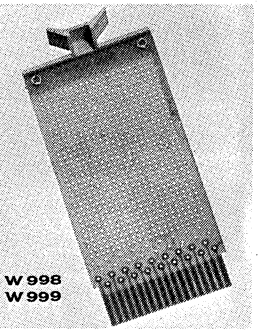
W982 — $18

BLANK MODULES
W970-W975, W990-W999

HARDWARE





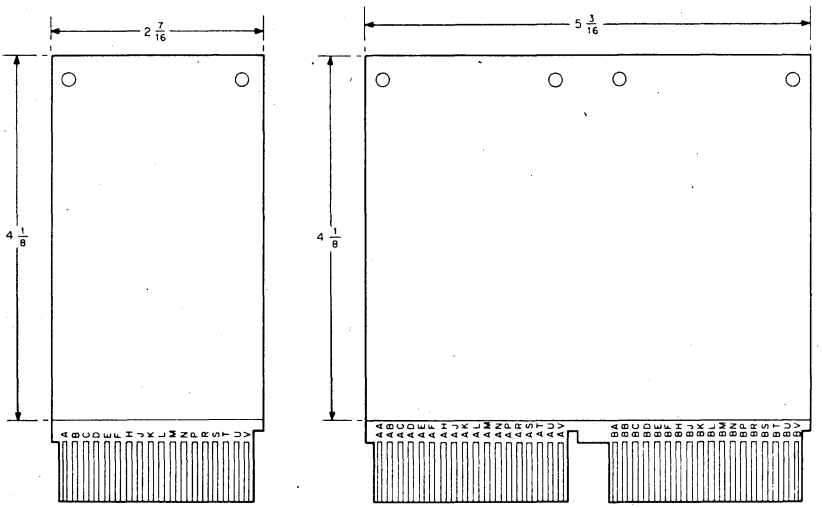


These 10 blank modules offer convenient means of integrating special circuits and even small mechanical components into a FLIP CHIP system, without loss of modularity. Both single- and double-size boards are supplied with contact area etched and gold plated. The W990 Series modules provide connector pins on only one module side for use with H800 connector blocks. W970 series modules have etched contacts on both sides of the module for use with double density connectors Type H803, and low density Type H808.

Type	Pins	Description	Handle	Price
W990	18	Bare board, split-lug terminals	attached	$ 2.50
W991	36	Bare board, split-lug terminals	attached	$ 5.00
W992	18	Copper clad, to be etched by user	separate	$ 2.00
W993	36	Copper clad, to be etched by user	separate	$ 4.00
W998	18	Perforated, 0.052" holes, 18 with etched lands. The holes are on 0.1" centers, both horizontally and vertically.	attached	$ 4.50
W999	36	Perforated, 0.052" holes, 36 with etched lands. The holes are on 0.1" centers, both horizontally and vertically.	attached	$ 9.00
W970	36	Bare board, no split lugs, similar to W990, contact both sides	attached	$ 4.00
W971	72	Bare board, no split lugs, similar to W991, contact both sides	attached	$ 8.00
W972	36	Copper clad, similar to W992	separate	$ 4.00
W973	72	Copper clad, similar to W993	separate	$ 6.00
W974	36	same as W998, contact both sides	attached	$ 9.00
W975	72	same as W999, contact both sides	attached	$18.00

BLANK COPPER CLAD MODULES
W992, W993, W972, W973

HARDWARE



W992 W993

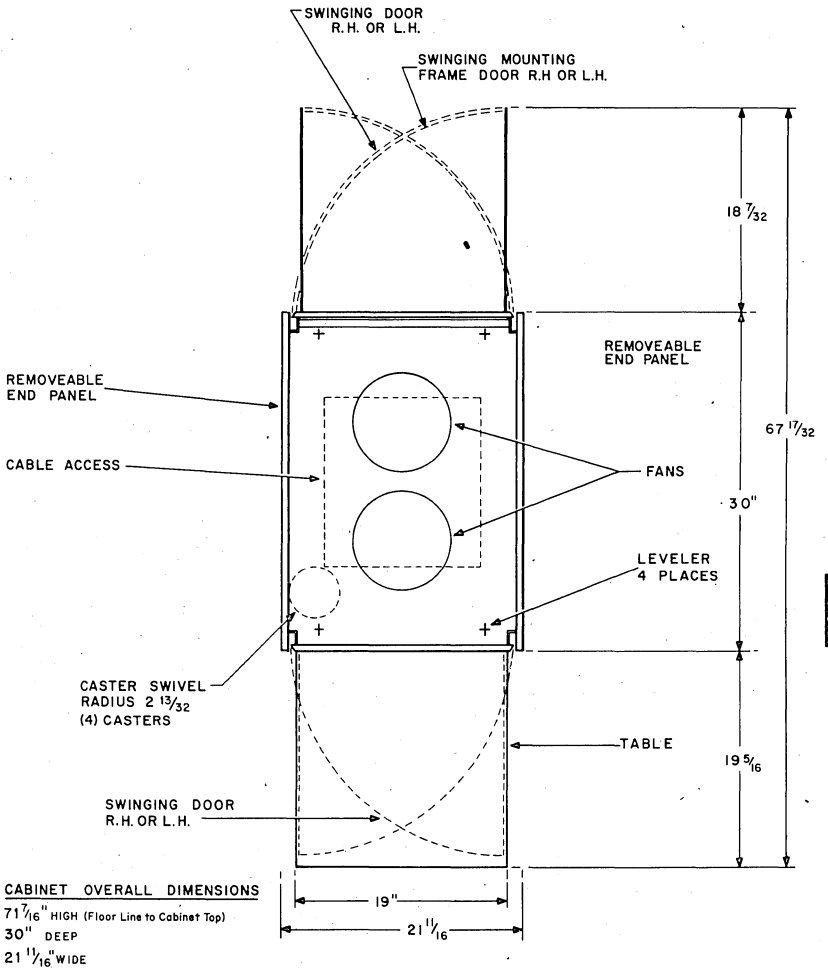
Type W992 and W993 are single side copper clad boards. The diagrams above indicate the copper clad area that is usable for etching purposes. The identifying numbers are etched from the clad using a minimum of etchable area. Type W972 and W973 are equivalent to the above types but have copper clad on both sides.

W972—$4
W973—$6
W992—$2
W993—$4

CABINET
H950

HARDWARE

	DEC Standard	
	71-7/16" Overall Height	Prices
	63" Mounting Panel Height	
Frame 19" Cabinet, 63" Mtg. Panel Height	H950-AA	$120.00
Full Door (RH)	H950-BA	35.00
Full Door (LH)	H950-CA	35.00
Mounting Panel Door (RH)	H950-DA	35.00
Mounting Panel Door (LH)	H950-EA	35.00
Mounting Panel Door—Skin	H950-FA	20.00
Short Door (covers 21" Mounting Height)	H950-HA	30.00
Short Door (covers 22¾" Mounting Height)	H950-HB	30.00
Short Door (covers 26¼" Mounting Height)	H950-HC	30.00
Short Door (covers 31½" Mounting Height)	H950-HD	30.00
Short Door (covers 36¾" Mounting Height)	H950-HE	30.00
Short Door (covers 42" Mounting Height)	H950-HF	30.00
Short Door (covers 47¼" Mounting Height)	H950-HG	30.00
Short Door (covers 52½" Mounting Height)	H950-HH	30.00
Short Door (covers 57¾" Mounting Height)	H950-HJ	30.00
5¼" Cover Panel (Snap On)	H950-PA	10.00
10½" Cover Panel (Snap On)	H950-QA	15.00
Filter	H950-SA	2.00
End Panel	H952-AA	35.00
Stabilizer Ft. (Pair)	H952-BA	45.00
Fan Assembly	H952-CA	45.00
Caster Set (4)	H952-EA	13.00
Leveler Set (4)	H952-FA	10.00



CABINET
H950

ORDERING INFORMATION FOR PREASSEMBLED CABLE

Standard lengths for preassembled cable are: 3, 5, 7, 10, 15 and 25 feet.

Cable price per foot is as follows:

19 conductor Ribbon cable	$0.60
9 conductor Flat Coaxial cable	$1.00
19 conductor 1¼" Mylar cable (BC08 only)	$0.75

Standard charges for connection of cable to each connector is as follows:

Ribbon	$ 9.00 per connector side
Coaxial	$18.00 per connector side
Mylar	$ 3.00 per connector side

STANDARD PREASSEMBLED CABLES

RIBBON

Type	CONNECTORS	Basic Price
BC02F-XX	W018-W023	31.00
BC02L-XX	W021-W021	26.00
BC02M-XX	W021-W021	27.00
BC02P-XX	W022-W022	28.00
BC02S-XX	W023-W023	26.00
BC02W-XX	W028-W028	28.00

COAXIAL

Type	CONNECTORS	Basic Price
BC03C-XX	W021-W021	44.00
BC03D-XX	W021-W021	45.00

To the above prices, add price of cable:

Example: BC02L-7 $30.20

1—BC02L-XX	$26.00
7 feet ribbon cable @ $0.60/ft.	4.20
	$30.20

A $5.00 service charge will be applicable to all cable lengths other than 3, 5, 7, 10, 15 and 25 feet.

Example: BC02L-9 $36.40

1—BC02L-XX	$26.00
9 feet ribbon cable @ $0.60/ft.	5.40
non standard length service charge	5.00
	$36.40

ORDERING INFORMATION FOR PREASSEMBLED CABLE

Standard preassembled cables; X shall equal 3, 5, 7, 10, 15 or 25 feet.

STANDARD M SERIES CABLES

M903-M903 1¼" Mylar Cable	
BCO8A-3	$41.50
BCO8A-5	44.50
BCO8A-7	47.50
BCO8A-10	52.00

M904-M904 Flat Coax. Cable	
BCO8B-3	$106.00
BCO8B-5	110.00
BCO8B-7	114.00
BCO8B-10	120.00

M903-2 W031 1¼" Mylar Cable	
BCO8C-3	$34.00
BCO8C-5	37.00
BCO8C-7	40.00
BCO8C-10	44.50

M904-2 W011 Flat Coax. Cable	
BCO8D-3	$101.60
BCO8D-5	105.60
BCO8D-7	109.60
BCO8D-10	115.60

CABLE CONNECTORS FOR INDICATOR AMPLIFIERS

TYPES W018, W023

W SERIES

The W018 and W023 provide 18 line ribbon cable connections to FLIP CHIP mounting panels. In the W018 connection to each pin is through a series low leakage silicon diode. The W023 provides unbroken signal lines from the cable to the connector pin.

When these cables are used with 4917 or 4918 indicators, the W018 must be located at the FLIP CHIP panel and the W023 inserted in the indicator socket connector. Cables may be ordered with connector modules on both ends or on one end only. Cable length may be specified in increments of 1 inch.

For ordering information, see W021, W022, and W028 on next page.

Care should be taken when using the W023 for other purposes, since the Power Pins (A, B) are unprotected.

Type	Price without Cable
W018	$9.00
W023	$4.00

CABLE CONNECTORS FOR LEVELS AND PULSES

TYPES W021, W022, W028

W SERIES

The W021, W022, and W028 provide cable connections to the FLIP CHIP mounting panel. The cable is a 19-conductor ribbon with nine signal leads and ten shields. The signal leads are connected to pins D, E, H, K, M, P, S, T and V. The shields are internally connected together and to pins C, F, J, L, N, R, and U.

In the W021, the signal leads are connected directly to the signal pins. In the W028, jumpers are available for series or shunt terminators. The Type W022 has a 100-ohm shunt terminator from each signal wire to the shield.

W021 — $4.00
W022 — $5.00
W028 — $5.00

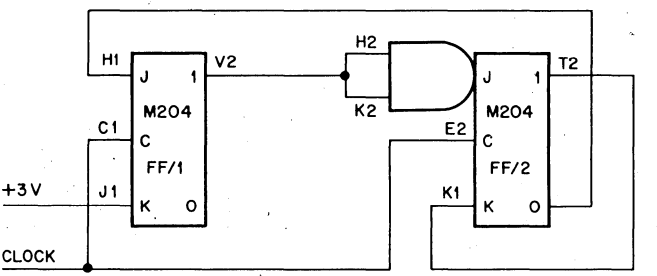
PART III
APPLICATIONS

COUNTER APPLICATIONS
TYPE M204

The arrangement of the J-K flip-flops on the M204 was designed to allow its use as a general purpose clocked counter with a minimum of external gating. This note describes configurations up to modulus 10 (binary coded decimal). In this range only modulus 7 requires additional hardware. The basic design principle used in these counters is to detect the present state of the counter and decide whether or not to complement the flip-flops on the next clock pulse.

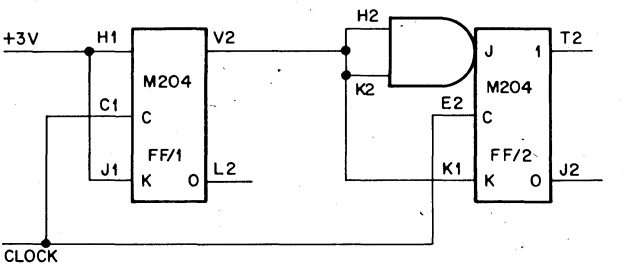
Other techniques exist for making counters of this type making use of pulse amplifiers etc., but these usually represent a significant increase in price.

It must be noted that the line defined as "Clock" requires a positive pulse which is the logical inversion of the standard pulse. One gate of an M117 can be used to perform this inversion. Since each clock input presents two unit loads to the source, more than 5 stages of counting requires the use of one gate of an M627. (Refer to the "Timing Considerations" section of the Logic Handbook.)



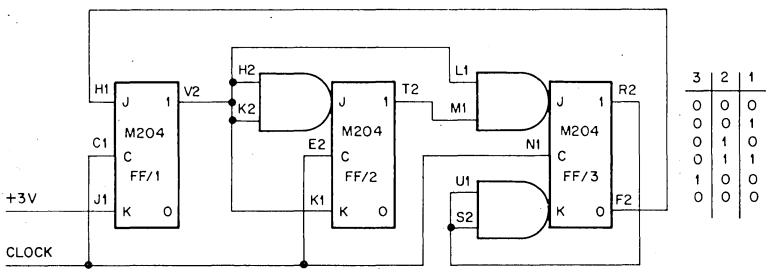
2	1
0	0
0	1
1	0
0	0

MODULUS 3



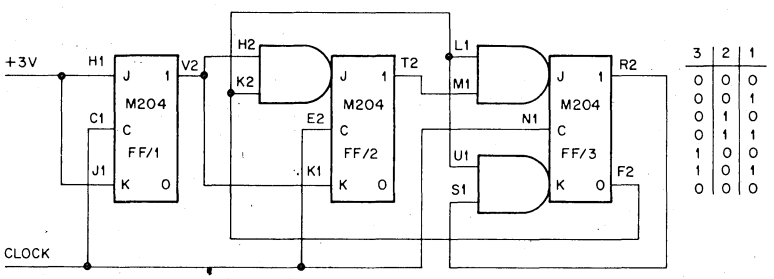
2	1
0	0
0	1
1	0
1	1
0	0

MODULUS 4



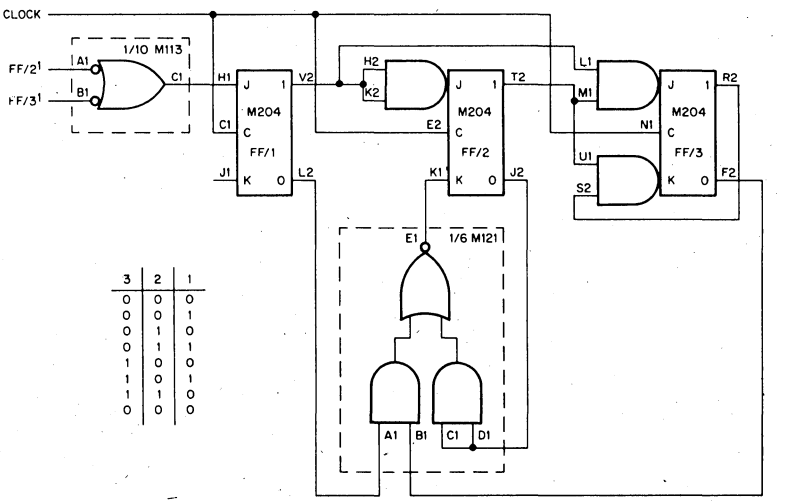
3	2	1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
0	0	0

MODULUS 5



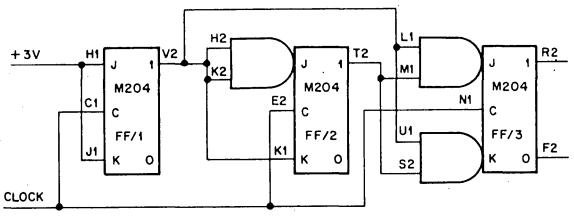
3	2	1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
0	0	0

MODULUS 6



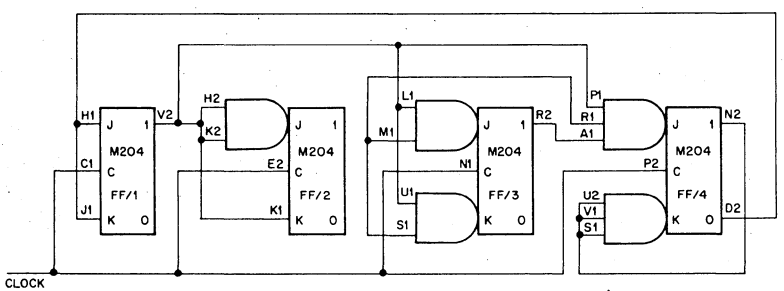
MODULUS 7

The modulus 7 counter requires external gating and cannot be implemented with the M204 alone.



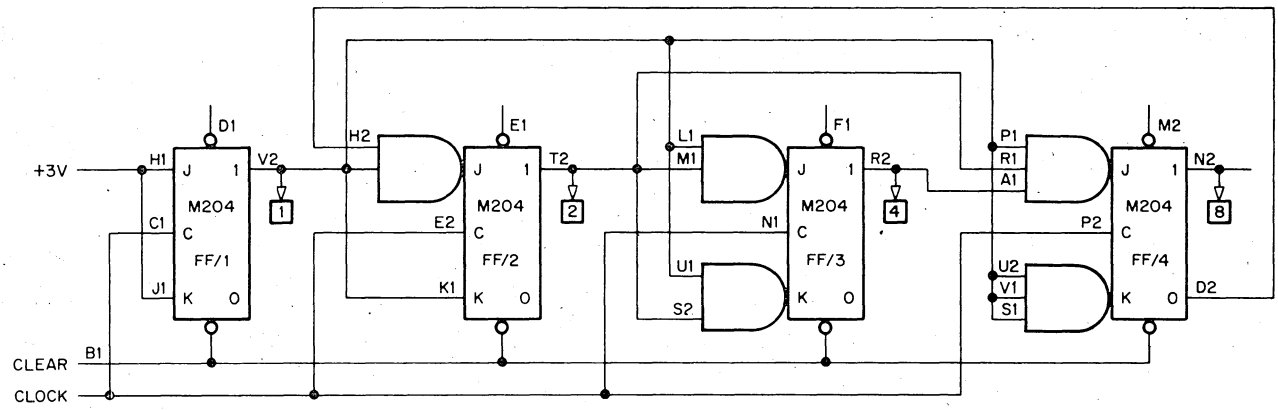
3	2	1
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1
-	-	-
0	0	0

MODULUS 8



MODULUS 9

4	3	2	1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
0	0	0	0



8 FF/4	4 FF/3	2 FF/2	1 FF/1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
0	0	0	0

MODULUS 10 (BCD 8421)

Discrete components for DIGITAL Modules are positioned and crimped in place at rates up to 2,200 per hour on pantograph controlled inserting machines. Board layouts put like parts in rows, minimizing the effort required to follow the template. Several templates for each module type are generated by numerically controlled milling machines.

EQUALITY AND RELATIVE MAGNITUDE DETECTION

APPLICATIONS

INTRODUCTION

This application describes one method of comparing two binary numbers for equality (A = B) and relative magnitude (A > B). Figure 1 shows 2 bits of a detector using M113, M117 and M121 modules. A 4-bit section requires sixteen two input NAND gates (1 3/5 M113), five — four input NAND gates (5/6 M117), and four AND/NOR gates (2/3 M121).

Each bit of the comparator functions with two independent circuit sections; the equality detector and the magnitude detector.

THE EQUALITY DETECTOR

Figure 2 shows just the equality detector used in each bit. The two AND gates in the AND/NOR gate actual detect $A_N \oplus B_N$ ($\oplus$ is exclusive OR) but since the output section of the AND/NOR gate also performs an inversion, the result is $\overline{A_N \oplus B_N}$ or equivalently $A_N = B_N$. This result can be verified in the truth table in Figure 3. If only equality detection is required, the output from a group of these detectors can be NANDed together with one gate of an M117 to give an "$\overline{A = B}$" signal at the output. For expansion to 16 bits, the "$\overline{A = B}$" signal from four 4-bit sections can be fed into a negative input OR gate (ie. another gate of an M113) to give an "A = B" signal from each 4 bits and then NANDed again with an M117 to provide up to 16 bit equality detection.

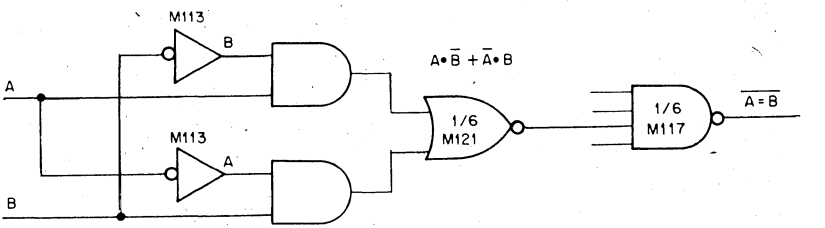


Figure 2.

A_N	B_N	$A \cdot \overline{B_N}$	$\overline{A} \cdot B_N$	$(A_N \cdot \overline{B_N})\ A\ (\overline{A_N} \cdot B_N)$	$A_N = B_N$
0	0	0	0	0	1
0	1	0	1	1	0
1	0	1	0	1	0
1	1	0	0	0	1

Figure 3.

NOTE: $\overline{(A_N \quad B_N) + (A_N \cdot B_N)} \Leftrightarrow A_N = B_N$
ALSO: "0" = Low
"1" = High

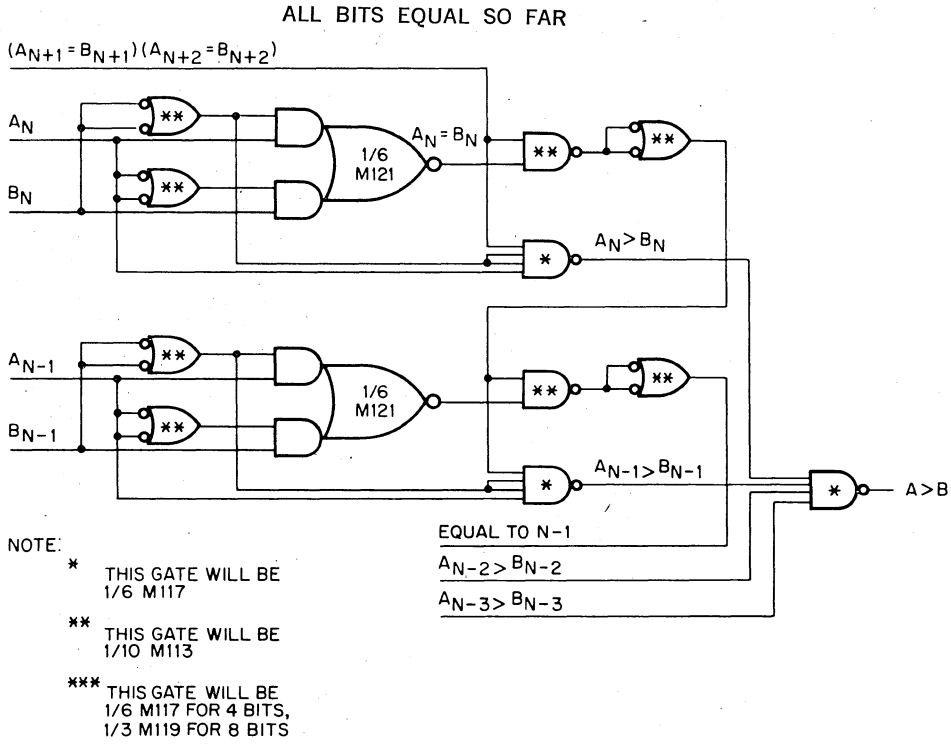


FIGURE 1. EQUALITY AND MAGNITUDE DETECTOR

THE RELATIVE MAGNITUDE DETECTOR

The relative magnitude detector at bit "N"

— receives "A_N", "$\overline{B_N}$", and "$(A_N = B_N)$" signals from the equality section,

— receives an "Equal so far" signal from "N + 1"

— generates output signals "Equal so far" and "$\overline{A_N > B_N}$".

The input signal "Equal so far" from bit "N + 1" indicates that all bits more significant than N are equal if HIGH (ie. +3 volts). Conversely, if LOW (ground) it indicates that at least one of the more significant bits is not equal. The output "Equal so far" from bit "N" being HIGH indicates that all bits up to and including bit N are equal. A LOW indicates an inequality at or before bit N. The "$\overline{A_N > B_N}$" signal will be LOW if $A_N = 1$ and $B_N = 0$ and all more significant bits are equal. By conditioning the "$\overline{A_N > B_N}$" signal with equality information from more significant bits, it is insured that if $B_N = 1$ and $A_N = 0$, an "$\overline{A_{N-X} > B_{N-X}}$" signal cannot be enabled to give a false A > B signal at the output (bit "N-X" is simply some bit less significant than bit "N"). Thus only the most significant level of inequality is considered if two numbers are unequal. In addition to the bit schematic of Figure 4, Figure 5 shows the truth table for the relative magnitude detector part of each bit.

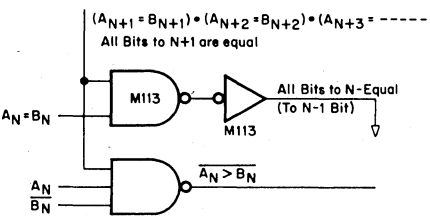


Figure 4.

INPUTS TO BIT N			OUTPUTS FROM BIT N	
Equal to Bit N + 1	A_N	B_N	"Equal to Bit N"	$A_N > B_N$
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

Figure 5.

A true XOR gate may be implemented using four-tenths of an M113, economizing by one (1) gate over the XOR in figure 3.

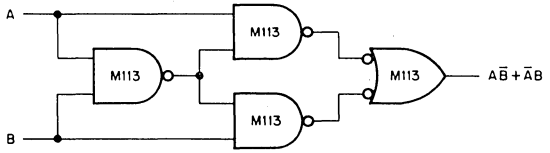


Figure 6.

USING THE EQUALITY AND RELATIVE MAGNITUDE DETECTOR

Figure 1 shows the construction of a two bit section of the detector. There are two outputs "A > B" and "Equal to bit N-1". The "A = B" output from the detector will always come from the least significant bit regardless of the number of bits in the detector. Figure 7 summarizes the meanings of the various possible output signals.

As in the case of the equality detector, the relative magnitude detector can be expanded to 16 bits by the method shown in Figure 8. It can be expanded further to as many bits as necessary by using "A > B" outputs from 16 bit sections to feed an extender such as that in Figure 8.

Since equality information must propagate from the most significant bit to the least significant bit, the propagation delay should be considered in each application. Each bit has a 30 nanosecond delay and if the extension in Figure 8 is used there is an extra 30 nanosecond delay for the total detector. Thus a 16 bit equality and magnitude detector would have a propagation delay of (16) (30 nsec) + 30 ns = 520 nanoseconds.

DETECTOR OUTPUT SUMMARY

A > B	A = B (at least significant bit)	Output Indication
0 (low))	0 (low)	B > A
0 (low)	1 (high)	A = B
1 (high)	0 (low)	A > B
1 (high)	1 (high)	impossible

Figure 7

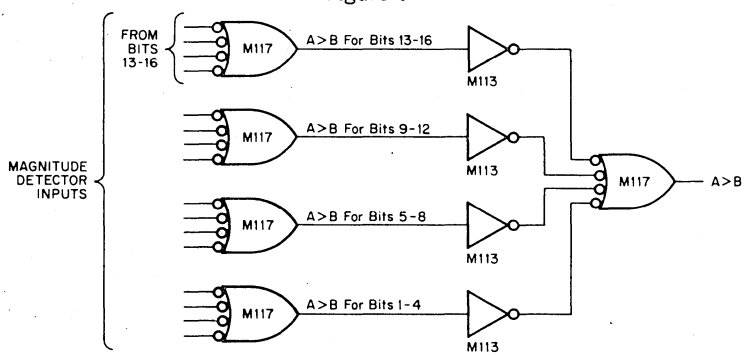


Figure 8

Table 1 gives the modules and pro-rated cost of a four bit equality detector.

Table 2 gives the modules necessary and the cost of a 4 bit equality and relative magnitude detector pro-rated according to module range. The gates required to extend the A > B output for more than four bits (see figure 8) are available as spare gates on the modules mentioned for each 4 bit section.

TABLE 1

DESCRIPTION	MODULE	QUANTITY	TOTAL PRICE
2 Input NAND gates	M113	4/5	$16.00
4 Input NAND gates	M117	1/6	3.50
AND/NOR gates	M121	2/3	16.60
			$36.16

TABLE 2

DESCRIPTION	MODULE	QUANTITY	TOTAL PRICE
2 Input NAND gates	M113	1 3/5	$32.00
4 Input NAND gates	M117	5/6	17.50
AND/NOR gates	M121	2/3	16.66
			$66.16

VOLTAGE CONTROL OF THE M401 VARIABLE CLOCK

The pulse repetition frequency of the M401 may be controlled or modulated by applying a variable voltage to the base of Q1. This may be accomplished as follows:

1. Open the connection between the base of Q1 and the junction of the resistor R1 & R2.
2. Insert a 750Ω, ±5%, ¼ watt resistor between the base of Q1 and one of the unused module terminals, F, H, L or M.
3. If the rate at which the frequency is to be changed or controlled is not excessive, add a .01 μfd. disc capacitor between the base of Q1 and ground for noise filtering.

The voltage swing applied to the resistor connected to the base of Q1 should be limited to ±0.25 volts about a center voltage of +1.5 volts. Table 1 shows the frequency excursions which one might expect when the frequency adjust potentiometer is adjusted to its full counterclockwise and full clockwise positions.

CAPACITOR	Freq. Adj. Pot.	+1.25V	+1.50V	+1.75V
No Ext. Cap.	CW	12.9Mhz.	13.1Mhz.	13.2Mhz.
	CCW	1.02Mhz.	1.32Mhz.	1.81Mhz.
.001 mfd.	CW	2.70Mhz.	3.37Mhz.	4.14Mhz.
	CCW	72.8Khz.	97.4Khz.	142.9Khz.
.01 mfd.	CW	382.6Khz.	504.5Khz.	720.4Khz.
	CCW	8.19Khz.	11.04Khz.	16.42Khz.
0.1 mfd.	CW	34.46Khz.	46.54Khz.	68.93Khz.
	CCW	722hz.	972hz.	1444hz.
1.0 mfd.	CW	3.622Khz.	5.144Khz.	8.052Khz.
	CCW	83hz.	112hz.	167hz.

PARITY GENERATION USING THE M162

APPLICATIONS

The M162 consists of two complete parity circuits, each of which will accommodate four lines.

4 LINE ODD PARITY GENERATION

The following condition must exist with four line odd parity generation:

$$A \oplus B \oplus C \oplus D \quad => \quad P$$

where $\oplus$ = the modulo 2 sum.

Also, in general, the following is usually desired:

$$\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \quad => \quad P$$

or

$$(A \oplus B \oplus C \oplus D) \; + (\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}) \quad => \quad P$$

The M162 connected as illustrated in figure 1 will satisfy the odd parity generation as per the following truth table:

	A	B	C	D	P
0	0	0	0	0	1
1	1	0	0	0	0
2	0	1	0	0	0
3	1	1	0	0	1
4	0	0	1	0	0
5	1	0	1	0	1
6	0	1	1	0	1
7	1	1	1	0	0
8	0	0	0	1	0
9	1	0	0	1	1
		↓ etc.			

It will be noted that the modulo 2 sum of the five bits (4 bits + parity) always yields 0 (an odd number of bits).

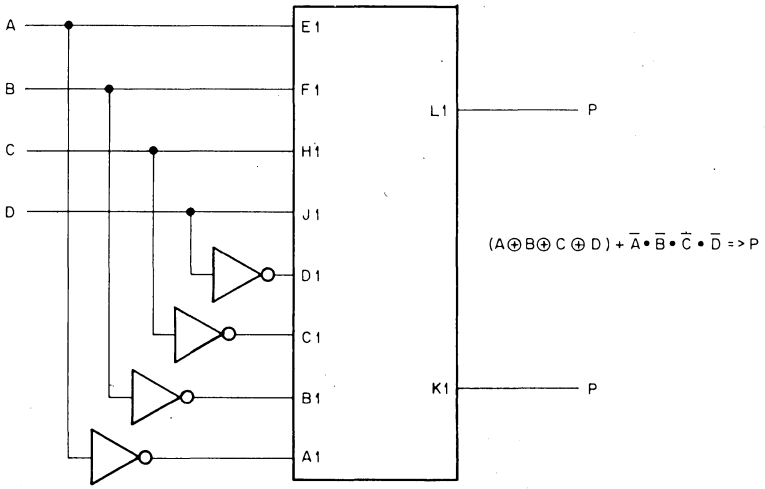


Figure 1.

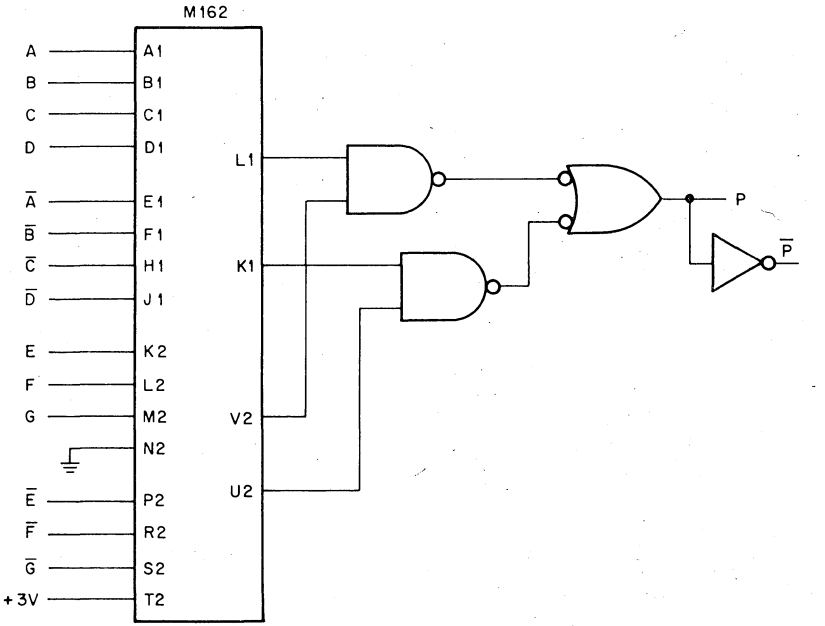
The odd parity generation with the condition $\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \Rightarrow P$ will always yield an odd number of bits in the resulting character.

7 LINE ODD PARITY GENERATION

In this case the following would be desired:

$$(A \oplus B \oplus C \oplus D \oplus E \oplus F \oplus G) + (\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E} \cdot \overline{F} \cdot \overline{G}) \Rightarrow P$$

This result may be obtained by connecting the M162 as shown in figure 2.



$$P = (A \oplus B \oplus C \oplus D \oplus E \oplus F \oplus G) + \overline{(A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G)}$$

Figure 2

ODD PARITY RECOGNITION

Figure 3 illustrates the connections for odd parity recognition and the following equation would be valid.

$$ODD = 1 = \overline{(A \oplus B \oplus C \oplus D \oplus E \oplus F \oplus G \oplus P)}$$

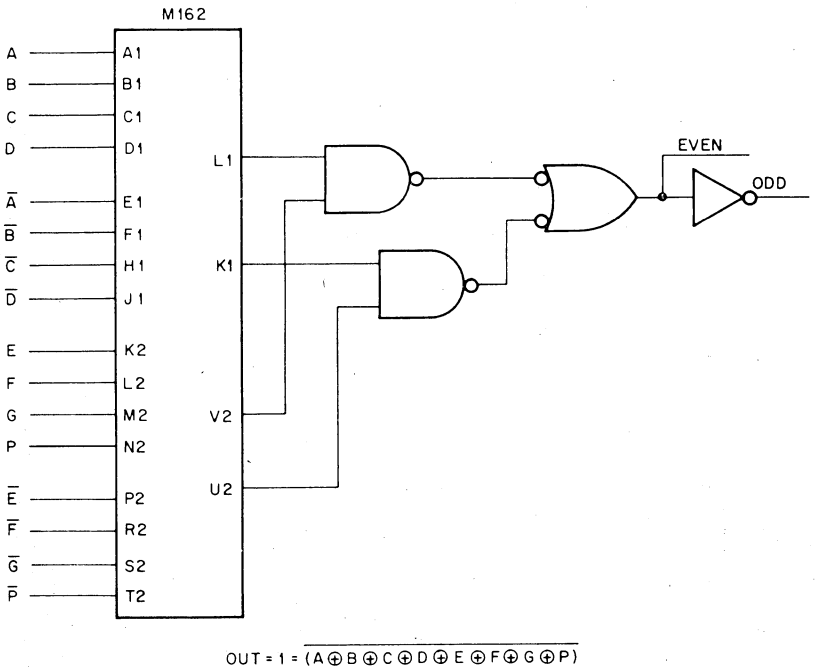


Figure 3

Odd parity generation for a larger number of bits may be accomplished by using the P and P outputs as if they were the L, and K, outputs of the M162 shown in figure 2. Figure 4 illustrates this expansion.

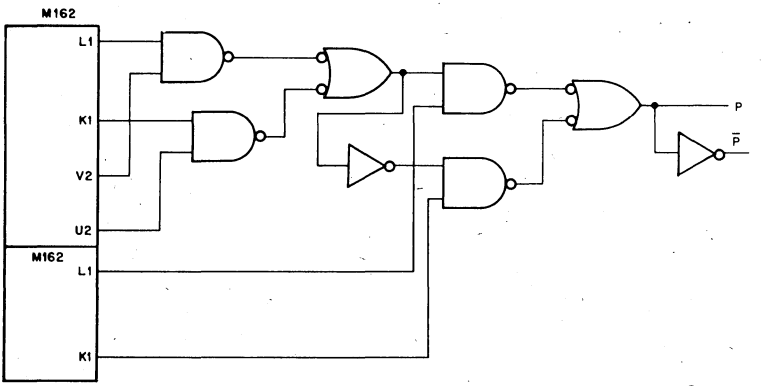


Figure 4

Decoding for the larger number of bits would be accomplished in exactly the same manner illustrated in figure 4 with the P output indicating a logic 1 for odd parity. However, remember that all unused direct inputs must be grounded and all NOTed unused inputs must be connected to +3 volts.

PROBABILITY GENERATOR

APPLICATIONS

This application note deals with the generation of pulses which have a set probability of occurring with respect to an input function. It is sometimes desirable to utilize a device which will emanate a pulse which has a definite probability relationship with respect to an input. That is to say if an input pulse is applied to the device there exists a definite set probability that an output will occur. Figure 1 illustrates one method in which this might be accomplished utilizing "M" series logic modules.

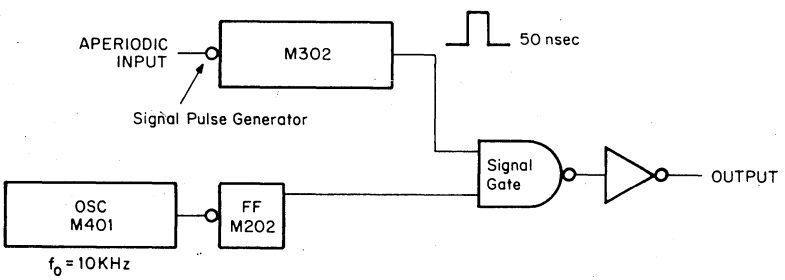
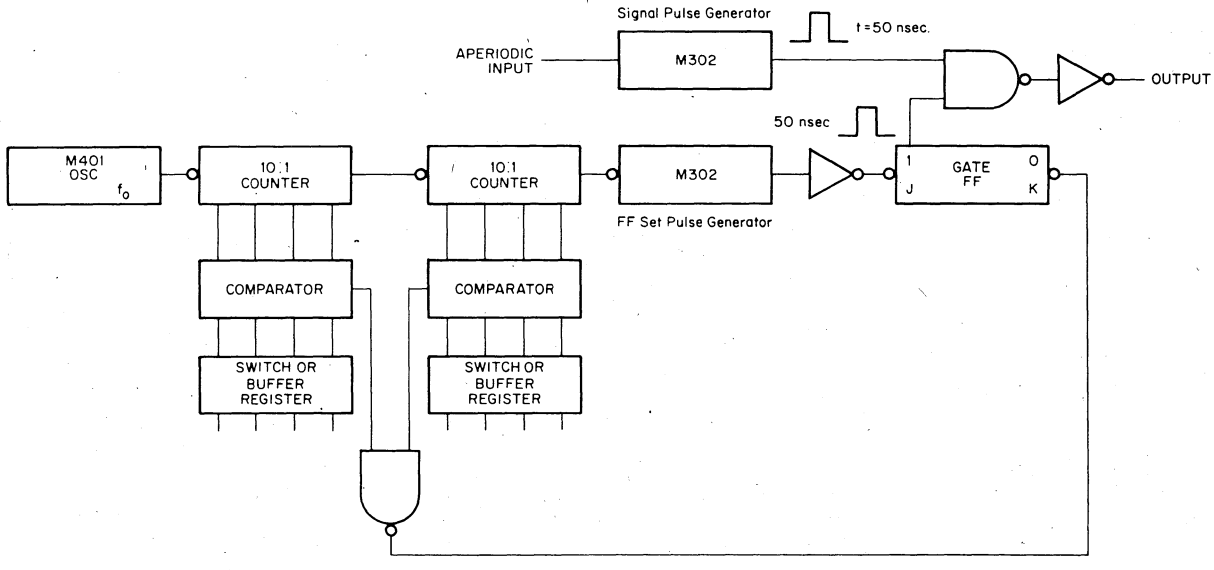


Figure 1

The circuit of figure 1 yields a 50% probability that an output will occur when an input is applied to the circuit. Two conditions must be met to assure the set probability.

1. The pulse width output of the flip-flop going to the signal gate must be very much greater than the 50 nsec pulse width output of the signal pulse generator.

2. The input must be aperiodic. (Usually obtained from animal response.) It is sometimes desired that the percentage probability be altered during the course of the experiment. Figure 2 illustrates the generation of a variable percentage probability.



APPL. 18

VARIABLE PERCENTAGE PROBABILITY GENERATION

Figure 2

The two counters represent a complete counter with a modulus of 100 with a radix of 10. Using a counter with a modulus of 100 will yield a percentage resolution of 1%. A counter with a modulus of 1000 would yield a resolution of 0.1% probability. The input is usually derived from an animal response, either human or otherwise, and the minimum time between inputs would be approximately five to twenty milliseconds. The minimum time between inputs determines the minimum frequency of the oscillator. A probability resolution of 1.0% could be easily accomplished if the oscillator frequency is approximately 10 KHz. The stability of absolute frequency is unimportant. The output of the counter is passed to a M302 "FF set pulse generator" and then to an inverter as the unconditional set terminals of the flip-flop requires a logical 0 to set the flip-flop. The flip-flop is reset by the output of the comparator circuit which emanates a pulse only when the counter flip-flops match the conditions indicated by the switch decades or buffer register. The buffer register would be used if it were desired to change the probability by the use of a computer. The signal gate flip-flop will now have a duty cycle represented by the set probability and would be expressed in percent.

Application

In behavioral research, probability generated pulses may be used to change or not change certain stimuli or to reinforce or not reinforce a subject on a random basis with a set probability.

ELIMINATING THE EFFECTS OF SWITCH CONTACT BOUNCE USING M203*

APPLICATIONS

The circuit of Figure 1 below illustrates one approach to the elimination of switch contact bounce. It is a circuit which is commonly used for this purpose. However this circuit has two inherent disadvantages. In the first case the current which the switch contacts make or break is limited to a maximum of 1.6 ma. which is in many cases not sufficient to maintain a low resistance switch contact surface. The second disadvantage is that one of the gate inputs is open at all times. As the input resistance of the typical TTL gate is of the order of several thousand ohms, the inherent noise rejection is minimal.

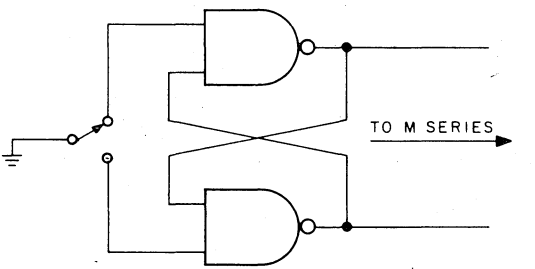


Figure 1

The circuit of Figure 2 provides better noise immunity as the typical resistance of the output of a TTL gate in the logic 1 state is of the order of 70 ohms. The instantaneous contact current of the switch will be between 18 and 55 ma.

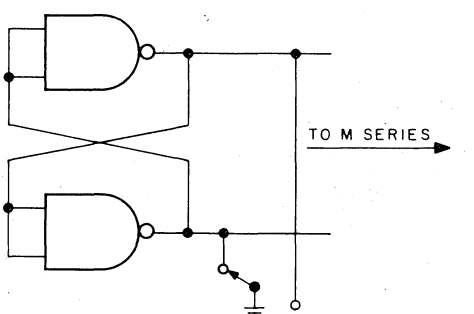


Figure 2

The M908 could be used for interconnection between the switches and flip-flops; up to 18 switches could be accommodated for each M908 used.

* This application note is of concern to only those persons not requiring the high noise immunity afforded by "K" Series.

INTERFACING K AND M SERIES LOGIC TO NEGATIVE VOLTAGE LOGIC

APPLICATIONS

NEGATIVE VOLTAGE TO K SERIES

It is recommended that an output of negative voltage logic be interfaced to K Series logic via the diode inputs of the K134 inverter module. Figure 1 illustrates one method of interfacing the output of negative voltage logic to the input of the K Series modules. The K134 will appear to the negative voltage logic as two unit loads. The W994 perforated blank module could be used to mount these resistors.

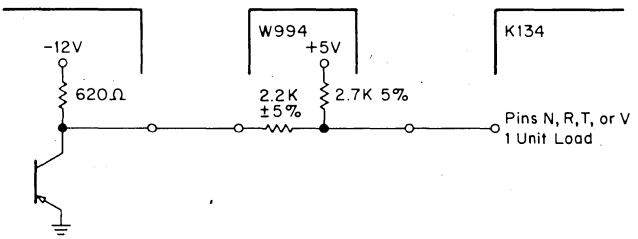


Figure 1

K SERIES TO NEGATIVE VOLTAGE

The output of the K Series may be interfaced to the negative voltage logic by the use of the M050 module. The M050 has no pull-up resistors and resistors must be supplied and connected to a source of —12 volts. The resistors used as pull-up should have a value of 620 ohms with a tolerance of 5%. The W994 perforated blank would provide a convenient means for mounting these resistors. This arrangement will provide five unit loads of drive into negative voltage logic.

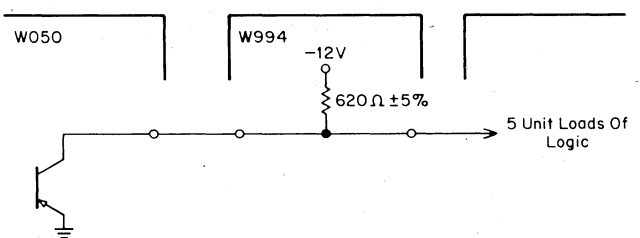


Figure 2

NEGATIVE VOLTAGE TO M SERIES

Interfacing the negative voltage logic to M Series would be accomplished using the circuit shown below in Figure 3. The output of the network should be passed through two M Series inverters to assure proper rise time required in M Series logic. The M111 would provide sufficient inverters to convert eight lines of negative voltage logic. This interface would represent 2 unit loads to the negative voltage logic.

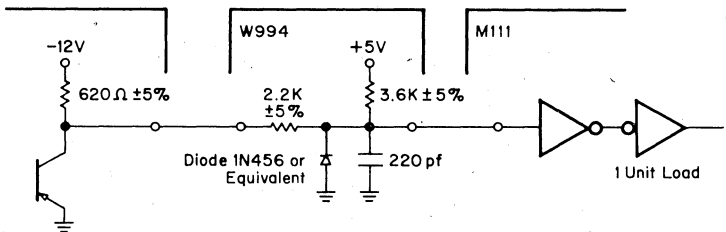


Figure 3

M SERIES TO NEGATIVE VOLTAGE

This conversion would be accomplished in exactly the same manner as illustrated in figure 2.

K-SERIES CONSTRUCTION RECOMMENDATIONS

A high percentage of all failures in electronic systems result directly from hasty planning of nonelectronic aspects. Much time and trouble can be saved by planning mechanical assembly before construction begins. Wiring methods and lead dress, heat distribution and temperature control, power supply reliability and line fault contingencies, and the attitudes and habits of people working near the system all merit forethought. Important opportunities for reliability, maintainability, and convenience will be lost if early and consistent attention is not given the topics below.

Environment

a. Temperature

Module temperature ratings are −20°C to 65°C (0°F to 150°F) except K202, K210, K220, and K230 which are limited to 0°C (36°F) minimum. These ratings are for average air temperature at the printed board, and take local heating by high dissipation components into account. Free, unobstructed air convection is required for reliable operation; the plane of each module must be essentially vertical for this reason.

Convection is required not only to remove heat but also to distribute it, and movable louvres or baffles used to obtain self-heating under frigid conditions must not interfere with air movement within and around modules.

b. Motion

Transport or use in trucks or aboard ships can vibrate modules sufficiently to work them out of their sockets. K273, K604, K644, K731, K732, and K303 modules with K374 or similar controls attached are most subject to disturbance.

If modules are mounted in a K943 19-inch panel, use K980 endplates and a 1907 cover.

If modules are mounted on the ninged door of an enclosure, position the K941 so a support bolted to the side of the enclosure will contact the modules when the door is closed, taking care not to let the support interfere with ribbon cable on K508, K524, K604, and K644.

Mercury contact relays in K273 modules should be maintained within 30° of vertical while operating to insure correct logic output.

Controls such as K374, etc. will hold their setting in vibration, but are easily disturbed by repeated contact with loose wiring, etc.

Finally, take pains not to nick logic wires if vibration is likely to be encountered. Use a quality wire stripper. One of the new motor driven rotary types could easily pay for itself by reducing wiring time and avoiding vibration induced wire breakage.

c. Contaminants

Sulphurous fumes will attack exposed copper or silver; their presence demands the coating of ribbon connections and K731 heatsink cladding with suitable insulating varnish or plastic. A combination of high humidity and

contaminated atmospheres requires such treatment on all printed wiring of K303 timers and controls, since at maximum settings even a few microamperes of leakage will affect their timing. Varnish or coatings are neither required nor recommended in less hostile conditions, and in any case it is desirable to exclude contaminants.

d. Convenience

Adjustments should be mounted so the least critical are easiest to reach. Calibrated controls such as K374, etc. should be positioned in a logical pattern before K303 sockets are wired. Ruggedness and feel should govern the selection of remote timer controls likely to be operated in moments of preoccupation or alarm.

Pluggable connections to K716, K724-K725, and (optionally) to K782-K784 allow electricians to complete their work while the logic itself is being built or checked elsewhere. Plan cable routing to simplify installation of electronics last. Take advantage of the ease with which a K941 mounting bar can be fastened to a pre-installed K940 foot.

Logic Wiring

a. General Information

Wire wrapping is the most suitable technique for the sockets used with K series modules. Some prefer AMP Termi-Point (trademark) but neither AMP nor DEC can guarantee full compatibility for this system. Solder fork connectors are optional; wrapped connections may also be soldered. For large volume repetitive systems using K943 mounting panels, DEC offers a machine-wrapping service.

Never solder or wire wrap with any tool if there are modules installed, unless the tool is grounded to the frame to drain static charges, and unless AC operated devices work from isolation transformers. It is safest to avoid AC operated wire wrap tools together. Hand-operated pistol-grip wire wrapping tools are surprisingly efficient and easy to use. If automatic machine wrapping is contemplated, plan for only two wraps per pin.

b. Wire Types

Teflon (trademark) insulation over size 22 tinned solid copper wire is best for soldering. Size 24 tinned solid copper wire must be used for wrapping H800 and K943 pins. Teflon (trademark) insulation may be used, but some prefer to sacrifice high temperature performance by using Kynar (trademark), to get greater resistance to cut-through where soldering is not involved.

Type 932 bussing strip allows module power and ground pins A and C to be connected conveniently, and is also helpful if several modules have common pin connections.

c. Procedures

First solder in all bussing strips. Next tie all grounds and grounded pins together. Finally point-to-point wire all other connections.

Run all wires diagonally or vertically. Do not run wires horizontally except to adjacent pins or along mounting bar between modules. Horizontal zig-zag wiring interferes with checking and is prone to insulation cut-through. Leave wires a bit slack so they can be pushed aside for probing. Cabling is definitely not recommended. Wires should be more or less evenly distributed over the wiring area.

When wrapping, avoid chains of top-wrap-to-bottom-wrap sequences which entail numerous unwrappings if changes must be made. Properly sequenced wraps require no more than three wires to be replaced for any one change in two-wraps-per-pin systems. Never re-wrap any wire. For best reliability, do not bend or stress wrapped pins, for this may break some of the cold welds. Follow tool supplier's recommendations on tool gauging and maintenance etc. As a convenience, DEC stocks three Gardener-Denver tools under numbers H810, H811, and H812. See specifications pages.

Field Wiring

a. AC Pilot Circuits

All screw terminals used in the K-Series have clamps so that wires do not need any further treatment after insulation is stripped. All terminals can take either one or two wires up to 14 gauge.

K716 terminals have been arranged so AC inputs all go to one end of the interface block, and AC outputs all go to the other end. The eight terminals nearest the center are typically connected only to each other and to a few return and AC supply wires. Input and output leads should be segregated so they do not block entry to the ribbon connector sockets. If sockets face to the left, AC inputs will be above and all other connections below. Wires should be routed down the connector side of K716 blocks to cable clamps or wiring ducts placed parallel with K716s. (See diagrams on K716 data page.)

Plan the logical arrangement of field wiring terminals and indicators before module locations are selected to avoid excessive folding or twisting of ribbon cables. (See recommendations on module locations below.)

b. DC and Transducer circuits

DC outputs from K644, K656, K681, and K683 and AC outputs from K604 and K614 are high level; wiring is noncritical. Low level inputs, however, may require special treatment to avoid false indications. Low level signals should at least be isolated from AC line and DC output signals throughout the field wiring system, and, as a minimum, individual twisted pairs should be used for signals and return connections.

For lower signal levels or longer wiring runs, shielded pairs may be required, with the shield grounded only at one point, preferably at the logic system end unless one side of the transducer is unavoidably grounded. Conduit which may be grounded indiscriminately is not an effective substitute for shielded, insulated wiring.

All signals except line voltage AC inputs use the straight-through connections of K716 terminals 15 through 24. Within the K716, leads are shortest to terminals 15, 17, 18, 19, and 20; use these terminals for minimum noise on K524 low level signals.

Module Locations

a. End Sockets (K941)

The first sockets to assign are those for K731 and K732 regulators, and for K303 timers. If possible, mount regulators nearest the foot of a K941 mounting bar, so their extra bulk projects into the space between the mounting surface and the first H800 block on the bar. Controls mounted on the same mounting surface opposite K731 source modules may be as much as 5/8" deep without touching modules.

Sockets at the outer end of K941 mounting bars are the only locations where K303 timers can have integral controls mounted. Even where the use of K370-group controls is not initially planned, assignment of K303 modules to these outer locations is recommended. Also, these sockets should be the first reserved as spares if any unused locations are available. This way maximum flexibility will be preserved for possible design changes or additions.

b. Interface Modules

AC and DC interface modules such as K508, K524, K604, and K644 should be assigned locations that simplify cabling. Ribbon cables can be twisted by a succession of 45° folds, but a neat installation should be planned. Assign the location and position of K716 interface blocks first. Consider such features as logical arrangement of indicator lights for trouble shooting, ease of routing and tracing field wiring, and directness and length of ribbon cable runs back to the logic modules.

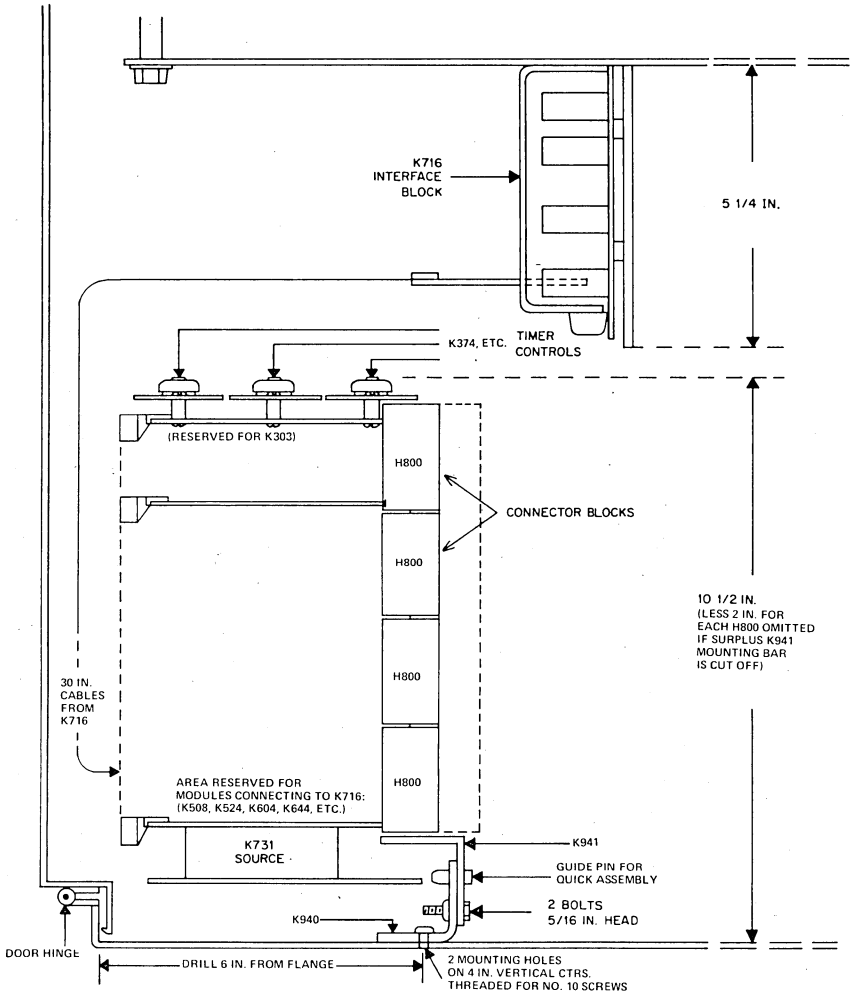
After K716 locations and assignments have been selected, assign socket positions for interface modules (K508, etc.). The order should be coordinated so the combined ribbon cables will lie flat together. Excess ribbon cable can be easily and neatly folded away. Lengths other than 30" are not available since these modules cannot be tested and stocked until cables are cut and soldered. This should cause no difficulty if module locations are assigned thoughtfully.

c. Display Modules

If K671 decade displays are required, select their locations after regulator and interface modules have been assigned sockets. The 12" cables on these modules are oriented for convenient assembly of displays above logic modules, to be viewed from outside the door or enclosure in which K940 and K941 hardware is mounted. Used this way, the digits of lower significance have cables below those of more significant digits.

For neatest cabling and quickest module wiring, counter and display modules should be arranged so the counter input will be nearest the K940 mounting surface. Notice that pin connections on K671, K210, and K220, and K230 modules are coordinated, so that a side-by-side pairing of flip-flop and associated K671 modules will result in short, neat, easy wiring. Ribbon cable passes easily between modules, so it is not necessary to restrict K671 modules to the topmost row. However, the limited cable length will usually restrict them to the top mounting bar in systems using more than one K941.

Do not fold or arrange ribbon cables so that they lie flat on the upper edges of modules, as this will restrict the flow of cooling air.

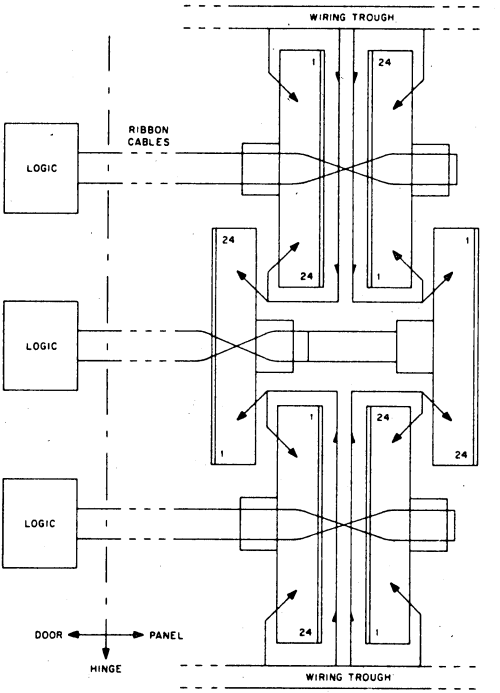


K-SERIES LOGIC IN A NEMA-12 ENCLOSURE,
16 IN. DEEP
TOP VIEW

System Power

a. Supply Transformer

Any filament or "control" transformer rated at 12 v or 12.6 v RMS on nominal 120 v line voltage may be used to supply power to K series logic. However, use of a 12 v instead of a 12.6 v transformer reduces maximum current ratings from K731 and K732 by 15%, as does a 5% voltage drop from any other cause such as resistance in secondary wiring or line voltage below the nominal 10% tolerance.



K716S IN INDUSTRIAL ENCLOSURE

Transformer current rating should be for capacitor-input filter, about 50% higher than the rating required for resistive loads. Thus a single K731 1 amp regulator requires a center-tapped transformer with ¾ ampere rating on resistive loads at 12.6v, or with two 6.3v windings rated ¾ ampere each.

These transformer selection considerations can of course be eliminated by using K741 or K743 transformers with noise filtering built-in.

b. Noise Filtering

Hash filter capacitors of 0.1 mf each are recommended from each side of the power transformer secondary to chassis ground. In environments where the AC line may carry unusually large amounts of noise, line filters such as Sprague Filterols (trademark) are advisable. K series systems must not share 12 volt power with any electromechanical device, since the transformer itself is the primary filter for medium-frequency line noise rejection.

c. Power Wiring

In systems not requiring full use of the quick-change features of the K716 and K940, transformer secondaries can be wired directly to pins U and V of regulator modules. If power connections are to be removed with maximum speed, a W021 connector board may be used to bring 12 VAC power into the system. It is best to limit current through any pin to about 2 amperes, so in large systems several W021 pins are needed for each side of the secondary.

d. Alternate Power Supplies

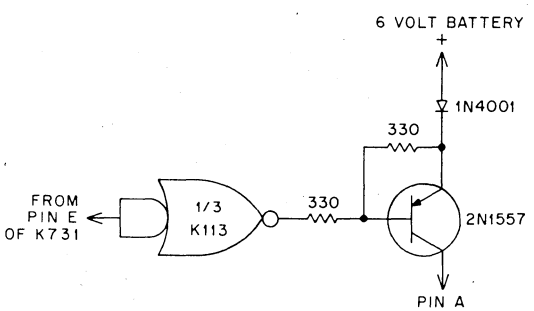
Any source of 5 VDC ± 10% may be used for K series systems at ordinary room temperatures, provided noise, hash, spikes, turnon-overshoot, etc. are reasonably well controlled. K series modules are far less sensitive to noise on power lines than computer-speed circuits, but it is still possible to cause malfunction or damage if extreme noise is present.

Temperature coefficient of the K731 regulator is selected to compensate for that of timers and other circuits, so operation over temperature extremes with constant-voltage supplies involves a sacrifice in timing consistency. Output fanouts are also degraded if constant voltage supplies are used at extreme low temperatures. Derate linearly from 15 ma at room temperature to 12 ma at −20°C (0°F) for constant-voltage power supplies.

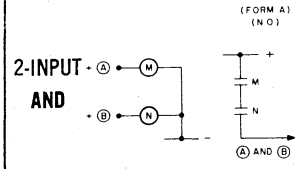
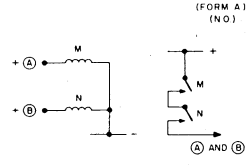
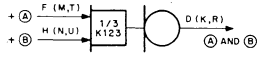
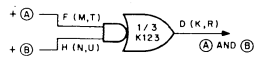
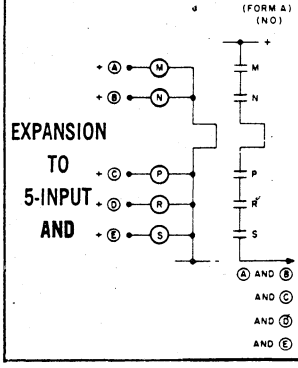
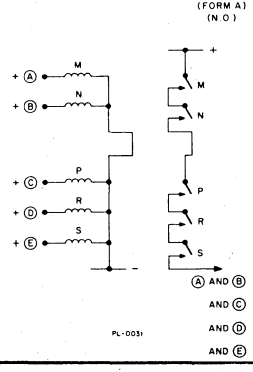
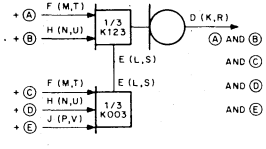
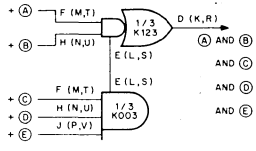
e. Line Failure

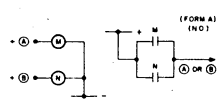
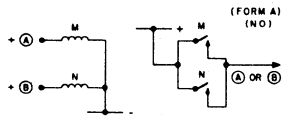
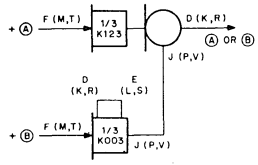
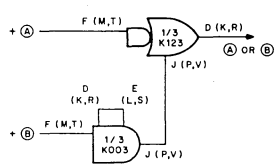
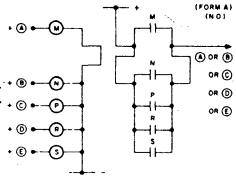
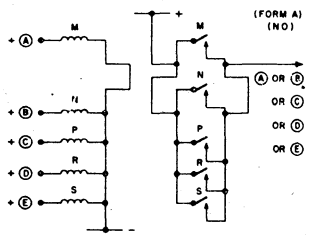
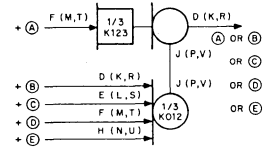
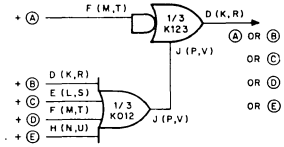
When unscheduled shutdown of a K-series system cannot be tolerated in spite of AC power failure, some form of local energy storage is required. To withstand short-term failures it is possible to add extra capacitance from pin A to pin C. However, manual grounding of pin D (turnon level) may be required to start the system, since the external capacitance will appear to the regulator as a short and output current will be limited to a low value. For each ampere millisecond of dc power storage beyond the rise of K731 OK level, 10,000 mfd is required. The supply itself provides one half ampere-millisecond internally. K732 slave regulators each provide one ampere-millisecond internally. However, these survival times are only available when regulators are operating at or below 75% of their nominal ratings.

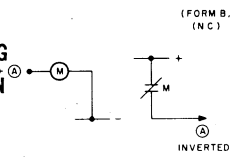
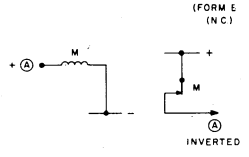
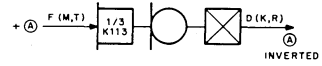
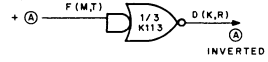
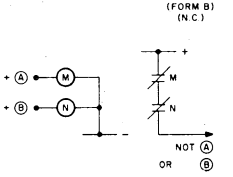
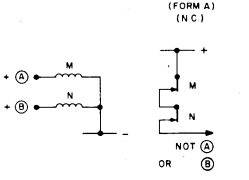
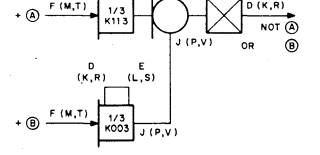
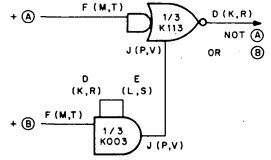
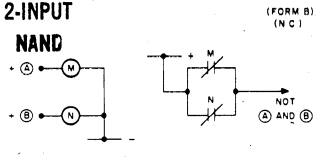
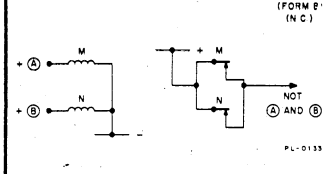
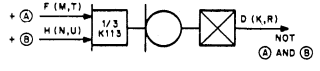
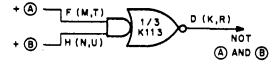
A 5 volt battery, or a 6 volt battery with series diode(s) to drop the voltage to 5 volts, may be used as an alternate source of power in case of line voltage failure. In very small systems (with some types of batteries) it may be practical to use the battery itself as a shunt regulator, charging it through a simple full-wave rectifier and dropping resistor circuit from the same kind of transformer used with K-series regulators. Unless the current is very low with respect to battery size, however, some means of switching the battery connection will be required. Below is shown a circuit which can be used for current requirements to 1 ampere. The same principle can be extended to larger systems with slightly more complex circuitry.

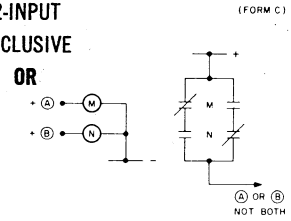
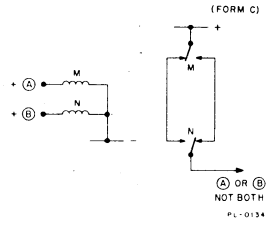
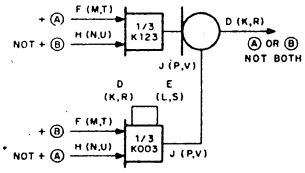
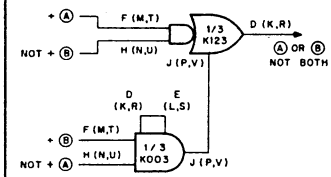
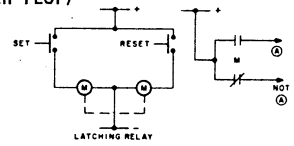
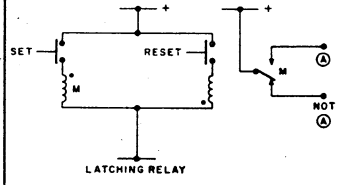
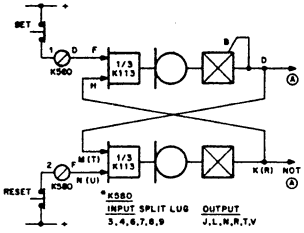
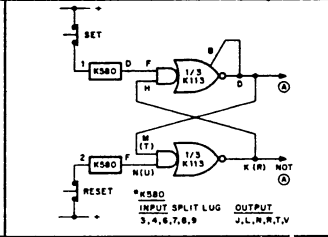
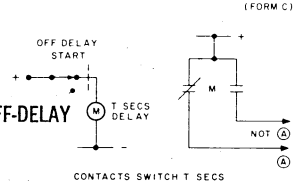
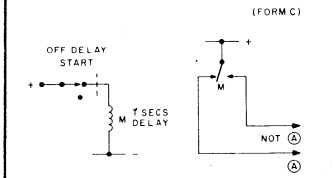
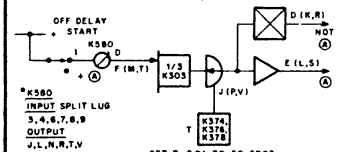
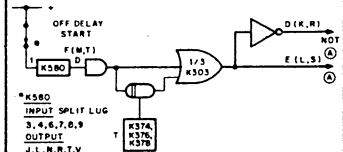


POWER FAILURE SWITCH FOR EMERGENCY BATTERY

ELECTRO-MECHANICAL		K SERIES	
J.I.C.	GENERAL	N.E.M.A.	MIL.
2-INPUT AND 			
EXPANSION TO 5-INPUT AND 			

ELECTRO-MECHANICAL		K SERIES	
J.I.C.	GENERAL	N.E.M.A.	MIL.
2-INPUT INCLUSIVE OR 			
5-INPUT INCLUSIVE OR 			

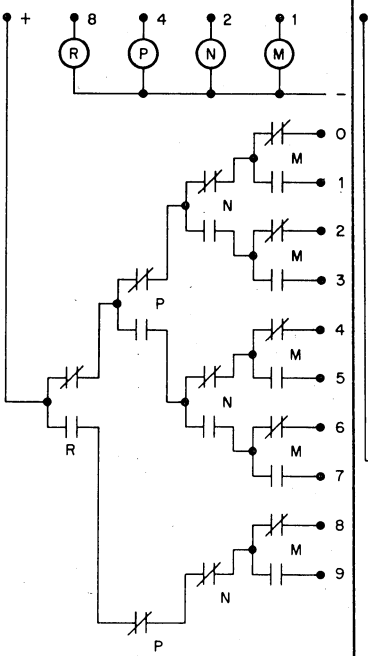
ELECTRO-MECHANICAL		K SERIES	
J.I.C.	GENERAL	N.E.M.A.	MIL.
INVERTING FUNCTION 			
2-INPUT NOR 			
2-INPUT NAND 			

ELECTRO-MECHANICAL		K SERIES	
J.I.C.	GENERAL	N.E.M.A.	MIL.
2-INPUT EXCLUSIVE OR 			
BISTABLE (FLIP-FLOP) 			
 OFF-DELAY			

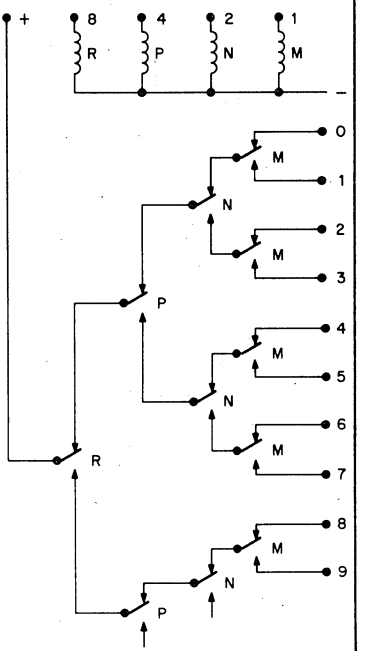
ELECTRO-MECHANICAL

DECODER:
BCD TO
10 LINE

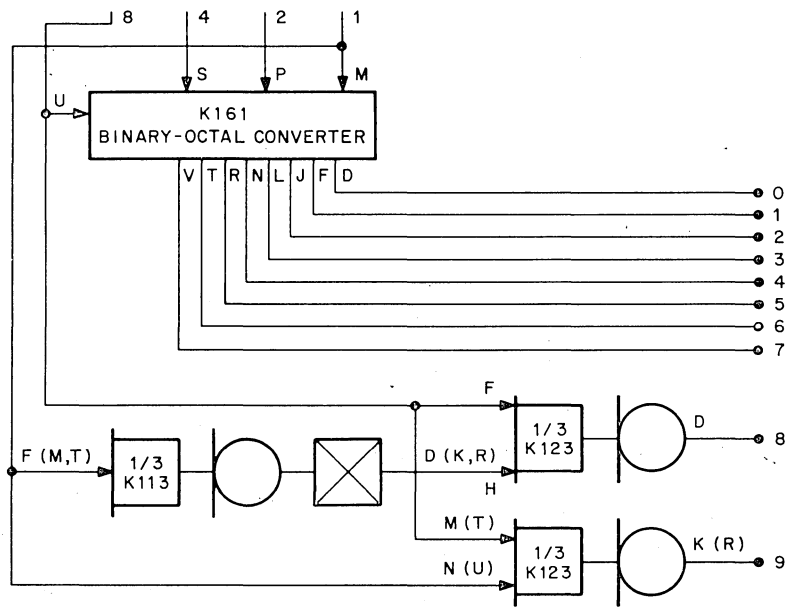
J.I.C.



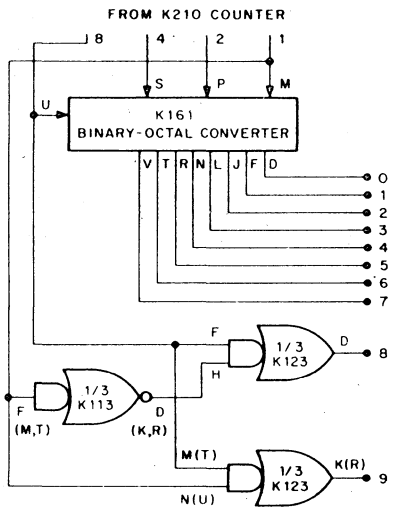
GENERAL



N.E.M.A.


FROM K210 COUNTER
8
4
2
1
S
P
M
U
K161
BINARY-OCTAL CONVERTER
V T R N L J F D
0
1
2
3
4
5
6
7
F
1/3
K123
D
8
F (M,T)
1/3
K113
D (K,R)
H
M (T)
1/3
K123
K (R)
9
N (U)

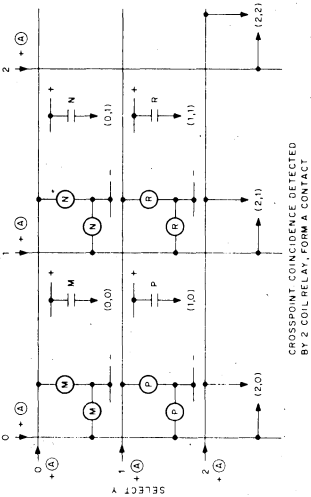
MIL.


FROM K210 COUNTER
8
4
2
1
S
P
M
U
K161
BINARY-OCTAL CONVERTER
V T R N L J F D
0
1
2
3
4
5
6
7
F
1/3
K123
D
8
H
1/3
K113
F
(M,T)
D
(K,R)
M(T)
1/3
K123
K(R)
9
N(U)

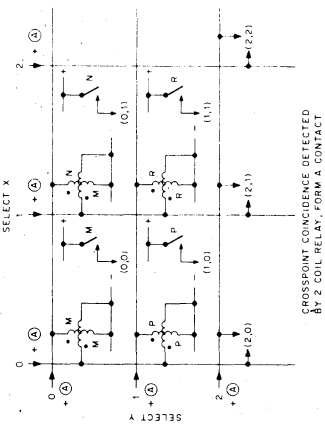
ELECTRO-MECHANICAL

CROSSBAR SELECTOR

J.I.C.

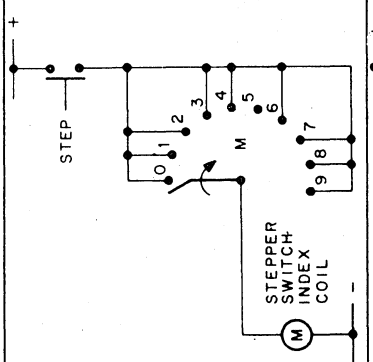


GENERAL

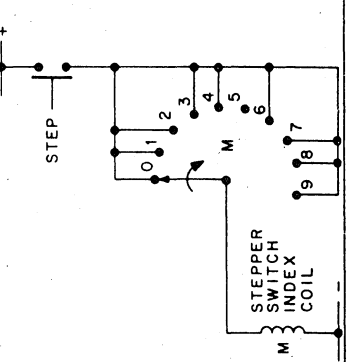


HOME-TO-5

J.I.C.



GENERAL



K SERIES

N.E.M.A.

MIL.

K SERIES SEQUENCERS — GENERAL

A fundamental part of many K Series systems is a sequencer that controls the progression from one state or operation to the next state or operation. Four logic elements are available to define the state or operation currently in effect, and there are also several choices of method for moving from each state to the next, and for deriving output signals that include any arbitrary set of states. This note considers each sequencer in a general way, so that their overall merits can be compared before starting detailed design with the 1 or 2 most appropriate. The simplest sequencer of all, consisting of logic gates alone, is not mentioned here; but of course if AND and OR functions by themselves can do the job, splendid.

1. TIMER SEQUENCER

Several independent K303 timers connected in cascade form a very flexible, completely adaptable sequencer. If each timer input is driven by the direct (non-inverted) output of the previous timer, removing logic "1" from the first will cause all the outputs to fall like hesitant dominoes. A pushbutton, limit switch, etc. can then reset all timers by restoring "1" at the first until the next cycle is wanted. Or by connecting the timers in a loop with an odd number of inversions a self-recycling sequencer can be obtained.

The complete adjustability of timer sequencers can be a disadvantage in some applications. When more than 3 or 4 steps are needed, the sheer number of knobs to twiddle begins to lead toward possible confusion and perhaps "provocative maintenance."

2. COUNTER SEQUENCER

One K210 counter provides up to 16 sequence states, and many more are obtainable by cascading. The counter may be stepped along by a fixed-frequency source such as the line frequency, or by a K303 clock. It is also possible to generate stepping pulses by completion signals from the processes being sequenced. K184 rate multipliers can be conveniently used to produce such pulses. Counter sequencers recycle without external aids at 9 or 15 (BCD or binary connections) and may be set to recycle at other steps as shown in K210 specifications.

Counter sequencers offer the most discrete states for the money, and the entire sequence can be scaled up or down in time simply by adjusting the input stepping rate. However, if many different output signals are to be derived from a counter sequencer, the gating can become complex unless the signals required happen to fit those available from K161 octal decoders or from the counter directly.

3. SHIFT SEQUENCERS

K230 shift registers can be connected as ordinary ring counters or as switch-tail ring counters. Specialized shift sequencers such as Barker

code (pseudo-random) sequencers are also possible. The most generally useful type is the switch-tail (Johnson code) ring counter, in which the last stage is fed back inverted into the first. This provides two states for every flip-flop, or 8 states if all four flip-flops in a K230 are utilized. The pattern achieved is the same falling-domino behavior obtained with the non-recirculating timer sequencer, except that the "dominoes" fall up one-by-one after they have finished falling down. Either fixed frequency or event-completion signals can be used to step a shift sequencer, just as for counter sequencers.

Shift sequencers cost more per state than counter sequencers. Their only advantage lies in the fact that any state or any collection of contiguous states can be detected by a simple 2-input gate. Not only does this feature simplify the derivation of many overlapping output signals, but it also offers excellent flexibility for modifications after construction. The need for only two connections to generate any once-per-sequence signal to start and end at any arbitrary state even permits practical patch-panel programming of output signals.

4. POLYFLOP SEQUENCERS

If the state or operation in progress is to be determined in many cases by a combination of external factors, instead of primarily by the sequencer itself, a polyflop may be the best solution. A polyflop is simply a multi-state circuit which will remember the last state into which it was forced until the next input comes along. Polyflops can have any number of states, though the practical limit is probably 8 or fewer. Set-reset flip-flops are a very common special case of the polyflop, having 2 states. If you want a name for the next six types you could call them tripflop, quadraflop, pentaflop, hexaflop, septaflop, and octaflop.

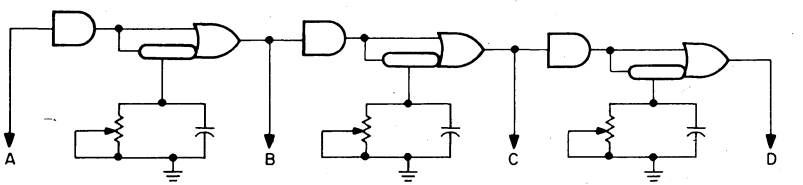
The general polyflop is built from as many K113 inverting gates as there are states required, each with input AND expansion sufficient to gate together all outputs by the one that gate controls. Thus any one low output will force all other outputs high. Polyflops do not establish any fixed order through the possible steps as the other three sequencers do, and so perhaps should be called state memories rather than state sequencers. However, there are some situations in which a polyflop is found to be a superior replacement for one of the ordered sequencers, such as where several different outside signals must be able to force the control into corresponding specific states immediately without passing through the normal sequence.

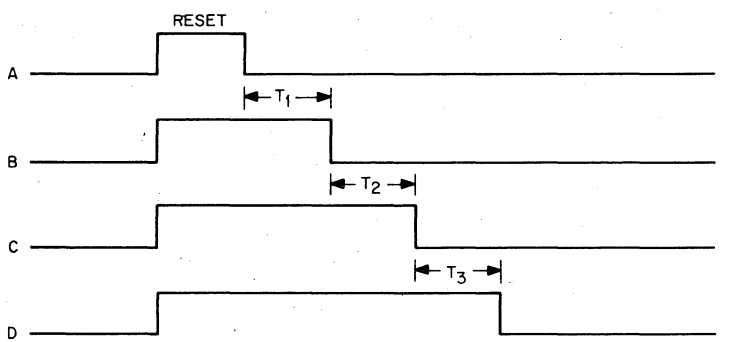
SUMMARY

Sequencer Type	Relative Cost per State	Modification Flexibility	Other Features
Timer	highest	easiest	Can be self-stepping
Counter	low-med	fair	Best for many states, few outputs
Shifter	medium	good	Suitable for patch panel setup
Polyflop	medium	fair	States may be forced in any order

TIMER SEQUENCERS

The simplest and most obvious way to sequence operations or states on a machine or in a control system is to use several timers in cascade. Below is shown a simple three-state timers sequencer.





A pushbutton, clock, or another sequencer can provide signal A that resets all timers and begins the sequence. Any number of timers may be cascaded, but if many steps are needed one of the less flexible sequencers should be considered as a means of reducing the number of adjustments and the cost.

Outputs other than those available directly from the timers can be obtained by a two-input gate connected to appropriate direct or inverter timer outputs. For example, a signal true during both T_2 and T_3 can be obtained by ANDing output D with the inversion of output B. The possibility of deriving any once-per-cycle output from this type of sequencer with two-input gates only is a virtue shared with switch-tail shifting sequencers.

The inverted output from the last timer in the chain may be used to provide the initiate signal resulting in self-recycling. However, sufficiently large timing capacitors must be in use to allow the initiate signal to rise all the way to +5 V if normal relations between timing RC and time delays are to be maintained.

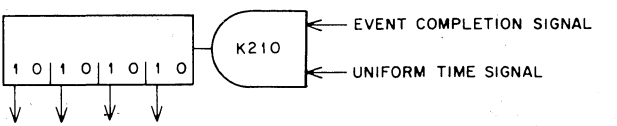
Three inversions, or any odd number of inversions must be contained within a self-recycling loop.

Many variations are possible by combining timer sequencers with other types of sequencers, branching to auxiliary sequencer chains, gating timer inputs from external devices, etc.

COUNTER SEQUENCERS

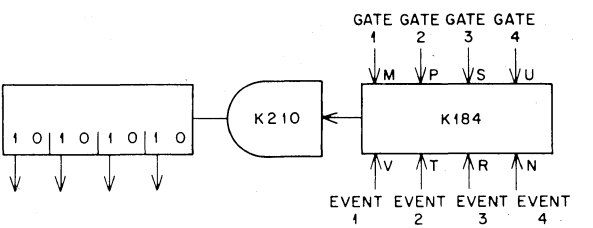
Counter sequencers offer the largest number of discrete steps for the money, since for N flip-flops up to 2^N states are obtainable. A single K210 counter, for example, offers up to 16 states for $27.

A source of timing signals, such as the "line sync" output from the K731 or a K303 clock may be used to advance a counter sequencer at uniform increments of time. In addition, event completion signals may be used to gate, augment, or substitute for the uniform time signal. One way to sub-



Event completion signal gates the time signal if the latter is a normally low, relatively higher frequency signal. Event completion signal augments the time signal if the latter is a normally high, relatively lower frequency signal.

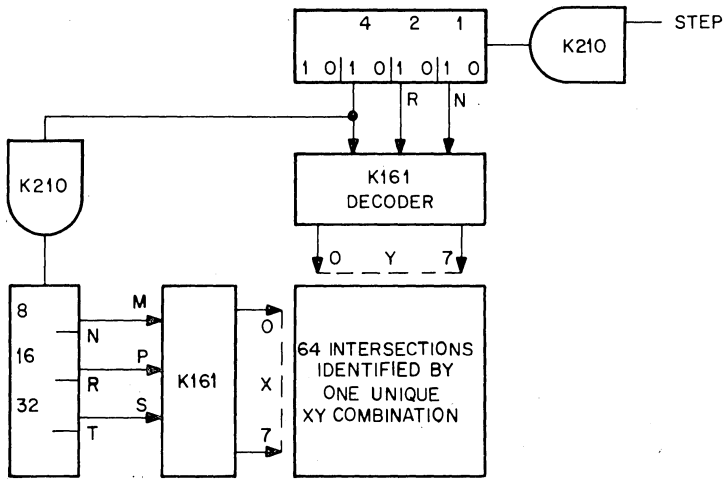
stitute for time signals is to use a K184 Rate Multiplier as if it were four separate differentiating pulse generators with ORed outputs.



USING K184 TO GENERATE EVENT COMPLETION PULSES

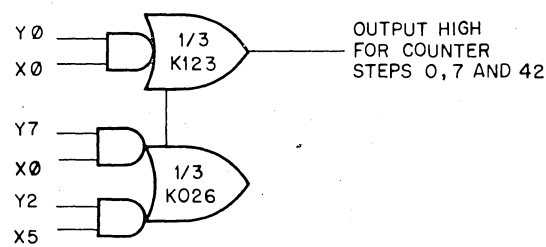
The principal disadvantage of counter sequencers is gating complexity, if many outputs must be derived which are not simply the flip-flop outputs themselves. Counter sequencers are most suitable for high-resolution sequencing of relatively few outputs whose relationship to sequencer states is unlikely to be modified after construction.

A crosspoint matrix offers reasonably low cost and good flexibility for developing counter sequencers with large numbers of states. For example, the 64 state sequencer shown here costs about $100 before any 2-input state detectors are added.



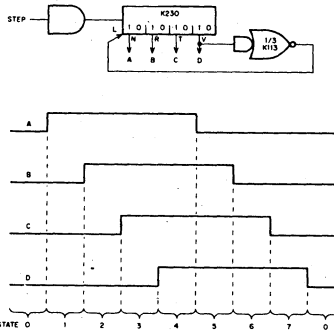
64 STATE CROSSPOINT SEQUENCER

The desired states may be detected one-by-one using any two-input AND gate such as those of gates K113, K123, or K134, or two-input gates on other modules like K210 counters, K230 shift registers, K303 timers, K604 or K614 AC switches, K644 or K656 DC drivers, etc. Or several states may be combined by ORing the outputs of several two-input AND gates as shown below.



SHIFTER SEQUENCERS

An alternate to the Counter Sequencer for generating many outputs, especially where some of the output sequences may be revised after construction, is the switch-tail shift ring.



Any one state can be detected by a single 2 input gate. For example, state 2 is true if B is high and C is low; state 4 is true if A and D are both high, etc. Moreover, any contiguous array of states may be detected by a gate of only two inputs. For example, state 2, 3, and 4 can be combined by a two-input gate that looks for A and B both high. This convenient characteristic not only reduces the cost and complexity of output gating, but also makes last minute changes easy since no new gates have to be added to modify the steps to which a given output gate responds, so long as they are contiguous. Also, notice that state 0 is on an equal footing with the others so that "contiguous" states may include or span the zero or home state.

The two input gating rule could be exploited to permit patch-panel coding of a general-purpose sequencer. One possible arrangement for such a panel is shown here, for a four flip-flop sequencer. In use, one would simply AND start and finish signals that span the desired state or states.

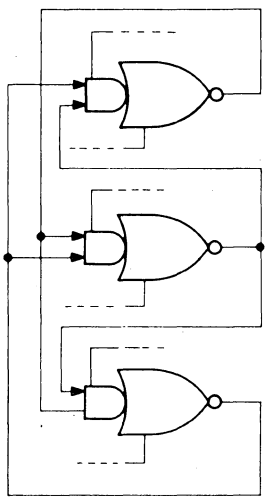
START	A ⊙	B ⊙	C ⊙	D ⊙	$\bar{A}$ ⊙	$\bar{B}$ ⊙	$\bar{C}$ ⊙	$\bar{D}$ ⊙
FINISH	$\bar{A}$ ⊙	$\bar{B}$ ⊙	$\bar{C}$ ⊙	$\bar{D}$ ⊙	A ⊙	B ⊙	C ⊙	D ⊙
STATE	1	2	3	4	5	6	7	0

For the special case of four states to be spanned, only one connection is required. Observe that to span more than half the available states, it is necessary to detect their complement and invert.

Switch-tail shift rings can be driven from all of the same sources as counter sequencers, and may be extended to as many states as desired. If N is the number of shift register flip-flops, 2 N states will be obtained in the sequencer.

POLYFLOP SEQUENCERS

Just as a flip-flop can be set to one of two states and remember it, a logic circuit that has three, four, or more states will remember the last of its several states to which it has been set.



The fundamental principle of the polyflop is that each inverting AND gate must have an input from all other outputs but its own.

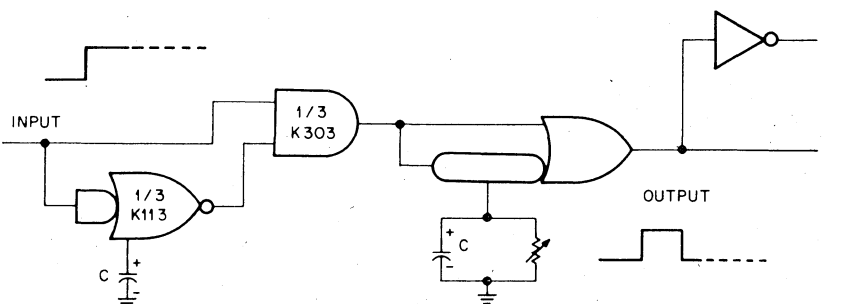
POLYFLOP	K113	K003	MODULE COST
TRIFLOP	1	0	$11.00
QUADRAFLOP	1-1/3	1-1/3	$20.00
PENTAFLOP	1-2/3	1-2/3	$25.00
HEXAFLOP	2	2	$30.00
SEPTAFLOP	2-1/3	4-2/3	$44.33
OCTAFLOP	2-2/3	5-1/3	$51.00
NONAFLOP	3	6	$57.00

The table above shows the components needed to build polyflops in the practical range of sizes. Module cost figures refer only to module sections actually used, and there is a significant amount of wiring required for the larger polyflops. Nevertheless, there will be circumstances in which a polyflop is more efficient than either a more conventional sequencer or a collection of ordinary set-reset flip-flops. Through the OR-expansion capability of K113 gates, external signals can be readily gated into a polyflop using low cost gate expanders. Selected output is low; all others high.

USING K303 TIMERS AS ONE-SHOTS

By itself, a K303 timer goes to the one state when its input goes high and waits there, not starting to time-out until the input returns low. Sometimes, however, it is convenient to start the entire cycle on an input change from low to high, without waiting for the input to return low. This behavior is that of the "one-shot" (also called single-shot or monostable multivibrator).

A K113 gate with a capacitor tied from its OR expansion node to ground can be used to obtain the necessary differentiating action. This capacitor should be the same size as the timing capacitor being used on the associated K303 circuit.



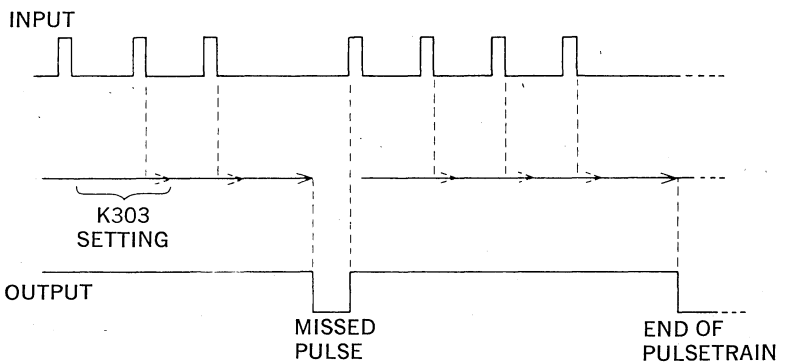
K303 AS ONE-SHOT

The K113 delay is about 3% of the maximum delay obtainable when using the same capacitor with a 250 KΩ timing resistor on the K303. The delay of the K113 is fixed, so the minimum K303 delay obtainable in this use is larger than normal.

The input must remain high for this same 3% interval, and should dwell in the low state at least twice this long for good repeatability.

USING K303 TIMERS FOR FREQUENCY SETPOINT

A K303 timer will reset to the start of its timing cycle when its inputs become high regardless of its previous state. This feature can be exploited to distinguish two pulse repetition rates, to detect a missing pulse in an otherwise continuous pulsetrain, or to close a frequency-regulating feedback loop. (Note: Where critical requirements are placed on K303 timing consistency in the millisecond range, consider the use of a low-ripple supply such as H710 to minimize modulation of the timing period at the ripple frequency.



Input signal can be a square wave or pulses of any width down to 0.3% of the maximum delay available with the timing capacitor used. (Pulsewidths down to 0.1% or less may be used if timing consistency can be sacrificed.) Timer delay would normally be set 30% to 50% longer than the nominal pulse repetition rate to detect missed pulses in a train, or at the geometric mean between two pulse periods which are to be distinguished.

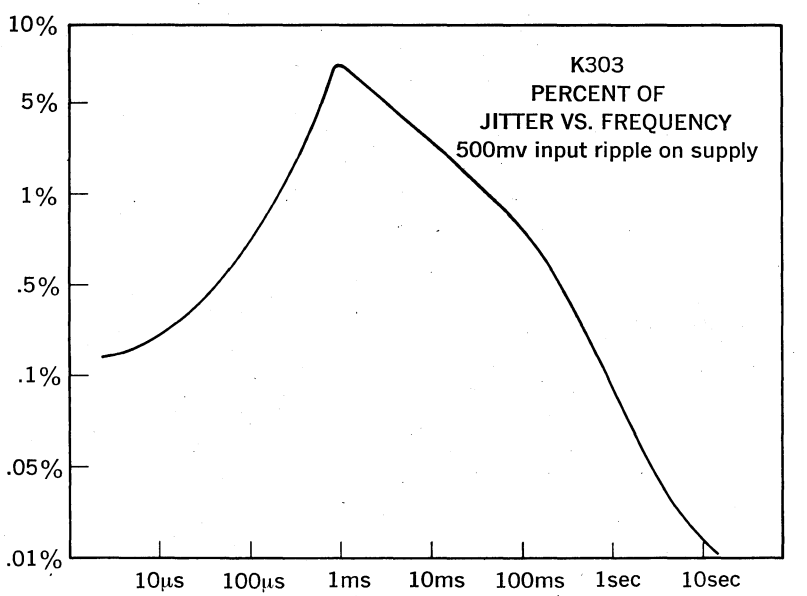
By cascading timers, pulses as short as 300 nanoseconds may be stretched to any length needed. However, pulses less than several microseconds in length do not produce consistent or predictable time delays from the K303, and are only recommended for pulse-stretching (using built-in 0.002 mf timing capacitor).

ESTIMATING K303 TIME JITTER

Repeat accuracy in the K303 can deviate as much as 8% of base time or frequency or even more if sufficient ripple is present on voltage supply line. Jitter is related to frequency or time setting and may be estimated by the graph showing maximum jitter from a K731 power supply at 75% of its maximum output. (i.e. 1 ms. period @ 500 mv. supply ripple yields 8% jitter.) Jitter at a given frequency is also proportional to supply ripple.

Reduction of ripple in applications requiring high accuracy may be accomplished by using a separate, lightly loaded K731 or by using the H716 or H710 Power Supply. Recovery times less than .3% will be additive to supply jitter. When used as a clock the timer controls K371, K373, or K375 will provide the proper recovery times.

If peak-to-peak ripple is held to 100 mv, 95% repeat accuracy may be expected from the K303 at all the settings.



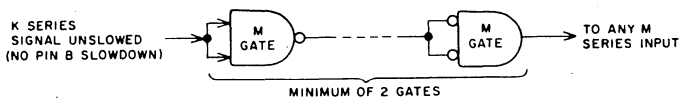
COMBINING K WITH M-SERIES MODULES

There are several types of applications in which a combination of M and K Series modules is better than either one alone, such as interfacing a K Series system to a computer or interfacing an M Series system to electro-mechanical devices. Here are the things to consider and recommended designs for both pulses and levels in each direction.

TIMING

Timing considerations are important, but unfortunately are not reducible to simple rules: as in any other logic design task, interfacing K with M Series modules requires adherence to all timing constraints of the output device, the input device, and the logic loops (if any) as a whole. As a minimum, M Series signal driving K Series circuits must last long enough (at least 4 microseconds even if no propagation within the K Series is required) so that the K Series will not reject it as if it were noise; and as a minimum, K Series signals driving M Series circuits must be received by M Series inputs that will not be confused by ultra-slow risetimes.

K TO M SERIES LEVELS



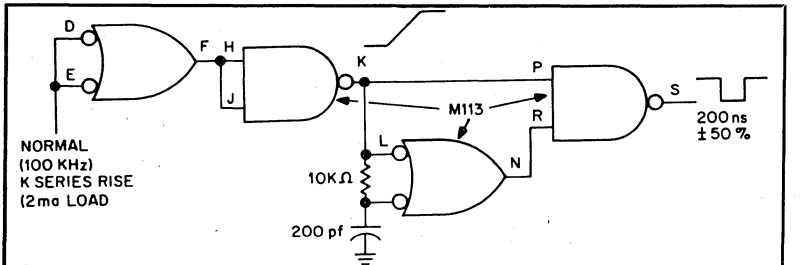
K TO M-SERIES LEVEL CONVERTER

Note: Total lead length connected to input of first M Series gate should be less than 6 inches, to minimize any tendency toward oscillation while active region is being traversed. Do not use slowed K Series levels. If noise still gets through, a .001 capacitor from M Series input pin to ground can be added.

M TO K SERIES LEVELS

1. Diode gate inputs (K113, K123, etc.) and drivers with flexprint cables (K604, K644, K671) may be paralleled freely with M Series inputs.
2. M Series outputs should not be paralleled (wired AND) with K Series outputs.
3. K303 inputs, K220, K230 readin gate inputs, and K135 and K161 inhibit inputs require the full 5 volt K Series swing, and normally should not be paralleled with M Series inputs. Also in this category are clear inputs to K202, K210, K220, and K230. M Series gate outputs will rise all the way to +5V if no M Series inputs are paralleled with these points, except the K161 inhibit input.
4. Other K Series inputs generally may be driven directly, but in some cases heavy capacitive loading will slow the transitions.

K TO M SERIES PULSES



Note: Same input restrictions as K to M Series level converter. M113 may be replaced by M602 circuit if desired.

M TO K SERIES PULSES

Use a type M302 delay multivibrator set for at least 5 μsec (capacitor pins H1-L2 or S1-S2). Observe same restrictions on K Series inputs to be driven as listed above under "M to K Series levels."

Loading

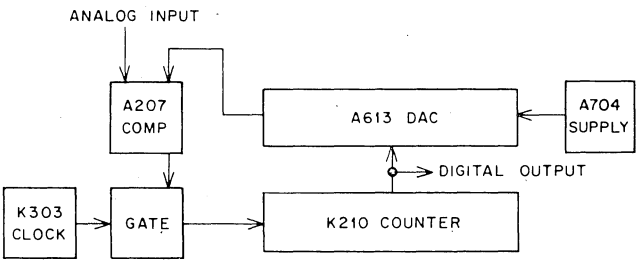
Driving M from K Series modules, each risetime-insensitive input should be regarded as a 2ma K Series load, and K Series inputs may be freely mixed with M Series inputs up to the total K Series fanout of 15 milliamperes. M Series inputs could be regarded as 1.6ma each if more complicated rules and qualifications concerning use with K303 timers and reduction in low-output noise rejection were established, but the 2 ma equivalence is simpler and safer.

Driving K from M Series, each milliampere of K Series load should be regarded as one M Series unit load.

For computer interfacing and other M-Series applications where K Series is used as a buffer to keep noise in the external environment from reaching high-speed logic, beware of long wires between the M and K Series portions. For full noise protection, all signal leads penetrating the noisy environment normally must have K-series modules at *both* ends. EIA converters (K596, K696) or lamp drivers may offer a helpful increase in signal amplitude or decrease in allowable line impedance for long data links. In any case, use all the slowdown connections or slant capacitors that the required data rates permit.

COMBINING K WITH A SERIES MODULES

The voltage breakdown ratings of K series gate module inputs (K113, K123, K134) is high enough to withstand the ±10 volt output swing of an amplifier such as A207, with correct gate output levels. This fact allows the A207 to be used not only as operational amplifier, but also as a comparator. A 12 bit slow speed analog-to-digital counter-type converter is made possible by using the A207 output directly as a logic signal.



BASIC COUNTER CONVERTER FEEDBACK LOOP

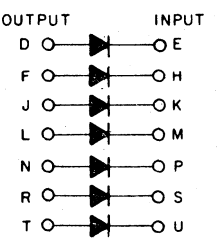
In operation, the counter starts at zero and counts up until the D to A converter output just exceeds the analog input. As the comparator inputs reverse their polarity relationship, the comparator output switches and inhibits the clock. The counter is left holding a number representing the analog input voltage.

The 20 microsecond recovery time of the A207 used as a comparator restricts operation to below 50 KHz. In the system shown here, the comparator "done" signal forces the clock output to the high state. Operation is re-started by clearing the counter or by an increase in the analog voltage. If a control flip-flop were added between the comparator and the gate, action could be halted regardless of input voltage change until a new "start" signal. Maximum conversion time is 4095 times 30 microseconds, or about 120 milliseconds. (The extra 10 microseconds allows for counter carry propagation time and the time required for the A613 output to change one small step).

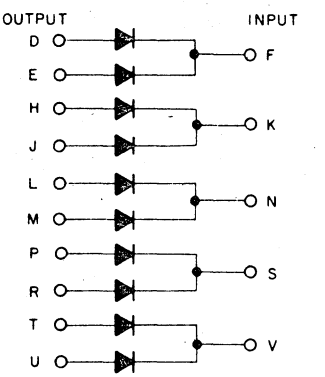
COMBINING K WITH R SERIES MODULES

For conversion from R series or other zero-and-minus levels to K series levels, the W603 (seven circuits, $23) may be used. When driving gate module or timer inputs, and most other K series inputs as well, pins B and V may be left open if desired (no +10 V supply). For conversion from K series to R series levels, use W512 (seven circuits, $25). For a more complete description of these FLIP CHIP modules, ask for the DIGITAL LOGIC HANDBOOK C-105.

There are two modules in the R series which can be used directly in the K series: The R001 and R002 gate expanders. The R001 is convenient for adding one extra input to a K-Series expandable AND gate, while the R002 can facilitate multiple inputs to several expandable AND gates from the same logic signal.



R001 DIODE NETWORK

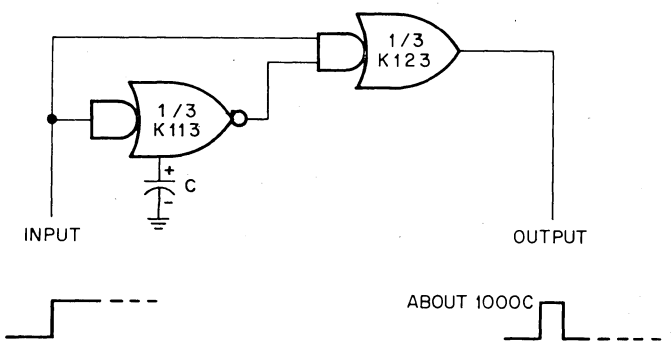


R002 DIODE NETWORK

R001 — $4
R002 — $5

PULSE GENERATOR

An effective pulse generator is formed by adding a capacitor to the OR node of a K113 inverting gate, as shown below. The circuit converts positive level transitions to pulses for clearing flip-flops, etc. Pulse width is slightly greater than 1000 C: 1.0 microfarad produces 1.0 to 1.5 millisecond pulses, 0.01 microfarad produces 10 to 15 microsecond pulses. The input must remain low for several times the pulse width for reasonable pulse width consistency.



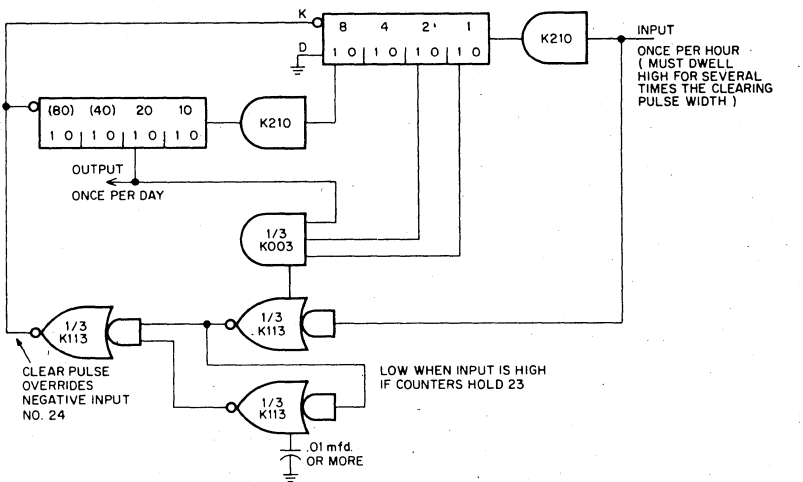
PULSE GENERATOR

Each K003 gate expander module includes a 0.01 mf capacitor from pin B to ground, suitable for use in this circuit to obtain pulses approximately ten microseconds wide. This is essentially the same scheme used to obtain one-shot behavior with K303 timers.

Inverted output pulses for clearing flip-flop registers, etc. may be obtained by substituting a K113 for the K123 gate shown.

USING K210s FOR LONG ODD-MODULUS COUNTERS

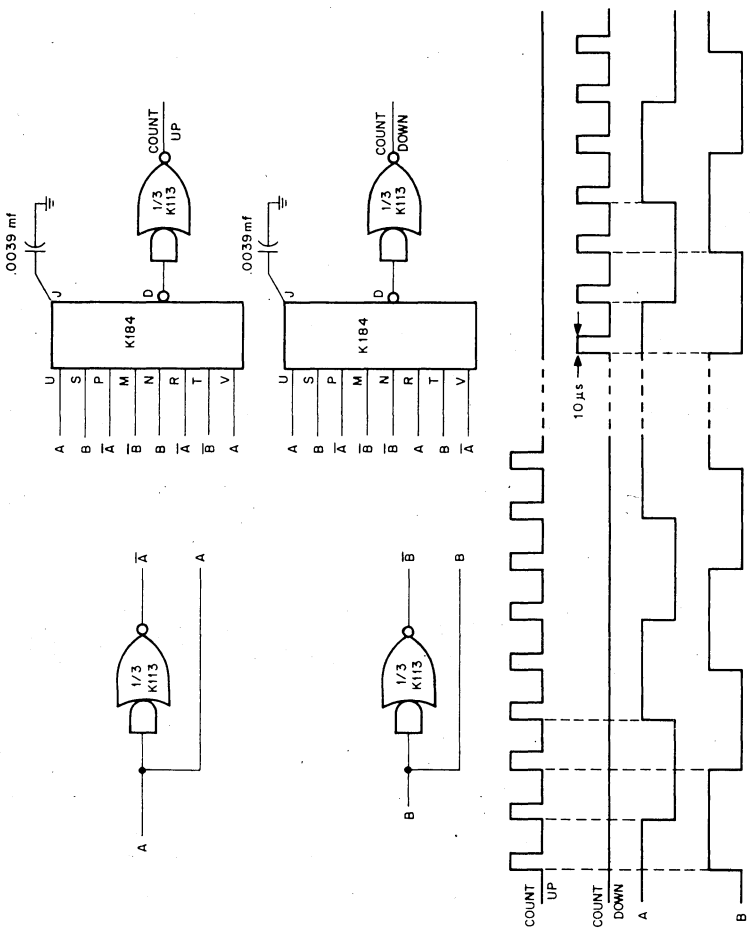
The pulse generator shown on the previous page can be incorporated with K210 counters to obtain counts at non-binary moduli above 16, the limit for a single K210. Below is shown a modulus 24 counter, as would be required for a digital clock.



The basic principle involved is to detect the largest number to be permitted, and to generate a clear pulse when it disappears due to the reception of one more count. The same method may be extended to counters of any length, provided the clear pulsewidth is wide enough to override any possible carry propagation.

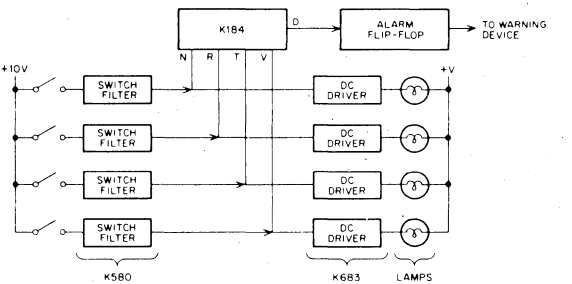
Shaft Angle Pickup Quadrature to Pulse Converter

Photoelectric shaft-angle transducers generate signals A and B in quadrature. Where maximum resolution and/or two-way counting is desired, the scheme below can be used to interface the amplified transducer outputs to the counter control shown on K220 data pages.



ANNUNCIATORS

In the simplest type of annunciator, a single alarm device is triggered by any abnormal occurrence, and a lamp is lighted by the occurrence to identify it. An inexpensive annunciator of this type can be built by taking advantage of the four Schmitt triggers and differentiators in the K184 module as indicated below. If silver contacts are to be sensed, auxiliary load and higher voltage must be used, preferably 120 VAC with K604-K716 or K614. Any number of inputs may be handled by ORing K184 outputs (wired OR possible for up to 5 K184s). The normal 5 μsec K184 pulsewidth should be stretched to 140 μsec for use with a slowed-down alarm flip-flop by putting a 0.1 mf capacitor from each K184 pin J to ground.



SIMPLE ANNUNCIATOR FOR FOUR DRY CONTACTS

In larger systems or where an abnormal occurrence may be too brief to be identified from a simple direct driven indicator, flip-flop memory must be added to each line to set up this sequence of operations:

ALARM STATUS	ANNUNCIATOR LAMP STATUS
1. No Alarm	Off
2. Alarm — Unacknowledged	Flashing (2Hz)
3. Alarm — Acknowledged	Steady
1. No Alarm — Memory Cancelled	Off

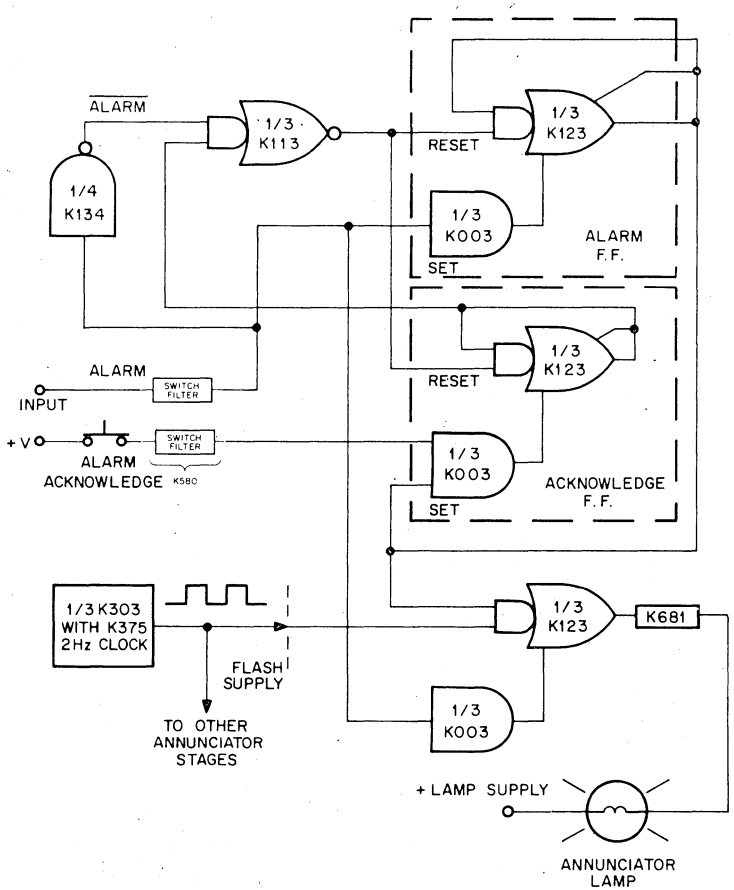
The Flash Supply is generated at a suitably low frequency by a K303 Clock with K375 Timer Control. This supply is available for distribution to other similar stages in a system.

The Alarm F.F. is set with an Alarm Input at Logic 1, the K580 controls the Alarm 0 to 1 response time. (See K580 data sheet) This allows the Lamp to flash. The Alarm F.F. is not cancelled, should the Alarm Input return to Logic 0. The initial Alarm must first be acknowledged manually before the Alarm F.F. is reset. Acknowledging the Alarm changes the Lamp from Flashing to Steady, and prepares the Alarm F.F. for Reset by the Alarm Input returning to Logic 0.

K Series Modules per Annunciator

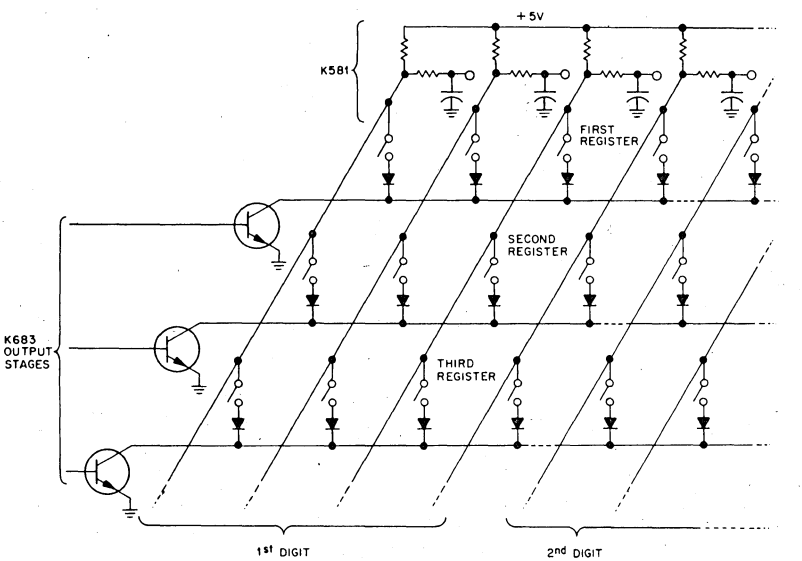
MODULE TYPE	NUMBER REQUIRED	NUMBERS OF CIRCUITS USED	COST PER LINE
K003	1 @ $ 4.00	3 of 3	$ 4.00
K113	1 @ $11.00	1 of 3	$ 3.60
K123	1 @ $12.00	3 of 3	$12.00
K134	1 @ $13.00	1 of 4	$ 4.33
K580	1 @ $20.00	1 of 8	$ 2.50
K681	1 @ $15.00	1 of 8	$ 1.80
		TOTAL	$28.23

The cost of common items, K303, K375, Power supplies etc., must be spread equally over the number of Annunciators in a system to get the true cost per stage.



Where more than one or two thumbwheel registers are needed it may be economic to multiplex several digits through the same K581 circuits as shown below. This scheme requires diodes to be mounted on the switches, as provided for by all of the types listed above. IN4001 diodes may be used.

Digitran part number 8788 offers two 8000 series switches with diodes mounted on a printed circuit board like a single-height FLIP CHIP module, and several of these may be connected to provide multiplexed registers as shown. Each such Digitran 8788 takes one module slot, but one extra socket per register pair is required to accept the extra thickness of the most significant digits.



To sequence through the registers, it is necessary to turn on one K683 circuit at a time; this can be done by a K161 binary to octal decoder. Since no BCD decade can draw more than 60 milliamperes, as many as four decades can be handled on any one K683 switch. Circuits may be paralleled for larger registers.

Notice that K581 outputs will be one diode drop above ground in the "low" state: This restricts multiplexing to use with K220 or K230 readin gates, or to K113, K123, or K134 inputs at 1 milliampere only. If the diode outputs (connector) on K683 are used, noise rejection will be reduced to levels that would normally be unacceptable. Direct (solder lug) connections are definitely recommended.

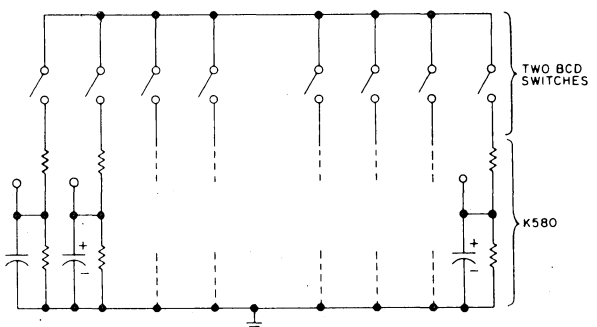
THUMBWHEELS AND MULTIPLEXING THEM WITH K581

Binary-coded decimal thumbwheel switches of many sizes and types are available to provide convenient manual data entry into K220 and K230 readin gates via K580 switch filters. Below are listed some of the many types that can be used this way:

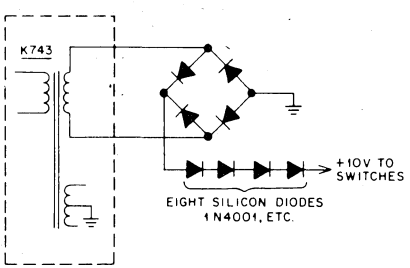
MANUFACTURER'S TYPE	PANEL CUTOUT HEIGHT	WIDTH PER DIGIT*
Digitran 315	1.380"	0.500"
Digitran 13015	2.000"	0.500"
Digitran 715	0.980"	0.500"
Digitran 8015	0.980"	0.500"
Digitran 9015	1.375"	0.600"
EECo 5305	0.960"	0.500"

*Note: Additional "zero digits" width generally required in panel cutout.

The simplest hookup uses one K580 for every two decimal digits as shown here.

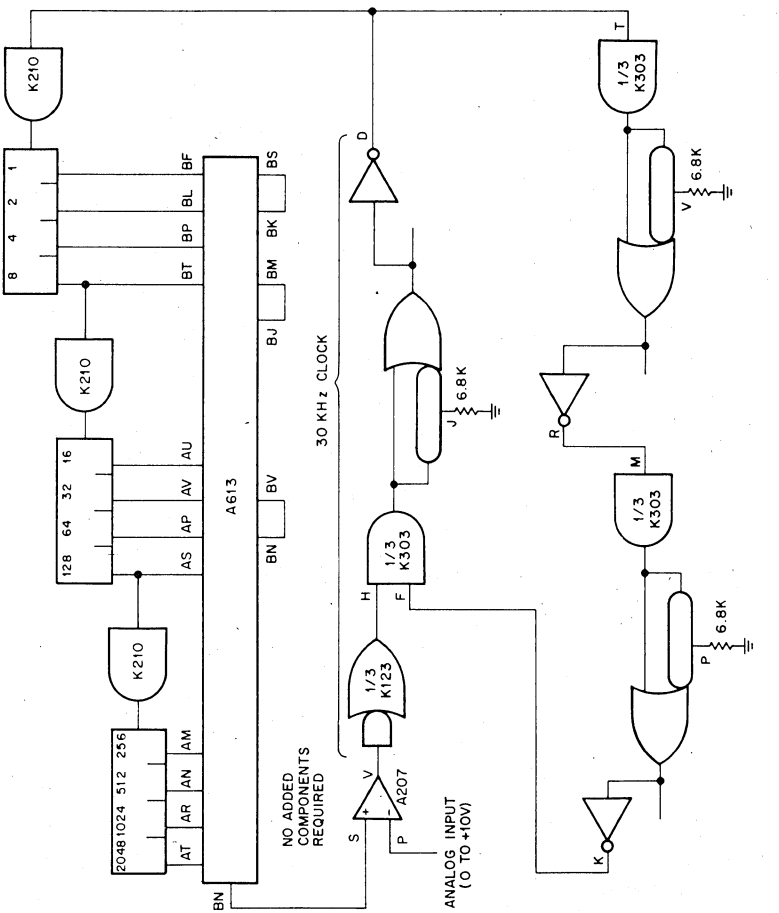


Power for the unmultiplexed system can be obtained from a 10 volt DC power supply or by using the circuit shown here with the auxiliary 12.6v winding on the K743 transformer.



OBTAINING +10V FROM K743

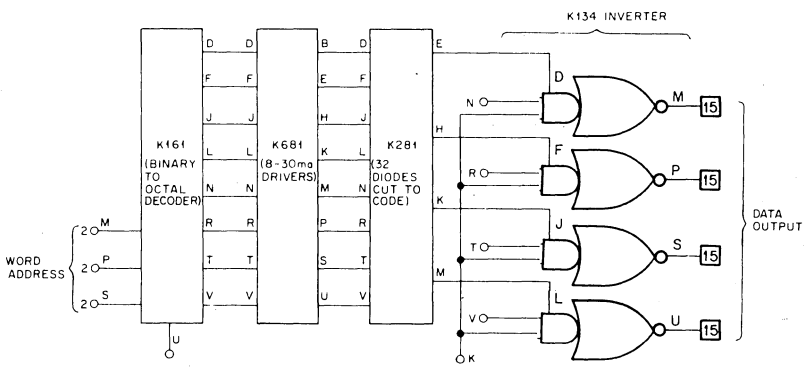
A faster converter may also be built using up/down counters or by building a successive-approximation type of converter.



12 BIT ANALOG TO DIGITAL CONVERTER

FIXED MEMORY USING K281

Switch registers such as those shown on the preceding page may be considered as memory devices. Very often a system that needs thumbwheel memory (or flip-flop memory) can also benefit from memory that is not readily changed. By using a K281 board with diodes cut out where "zero" is to be recorded, many types of sequence or character (symbol) codes may be permanently stored in a digital system.



Variations

More 4-bit words:

a) Use pin K inhibit on K134s to select 8 words
b) Duplicate K281 and K134, tying K134 outputs together
c) Use same K161 and K681
d) Up to 40 4-bit words may be obtained (fanout down to 3)
For more 4-bit words use longer words and gate outputs

Longer Words:

a) Use same K161 and K681
b) Duplicate K281 and K134; two for 8 bits, three for 12 bits, etc.
c) Single K681 capable of word lengths to 28 bits
d) Get more than 8 words as in getting more 4-bit words

Serial Scanout:

a) Connect word address lines to scanning counter
b) Tie together K134 outputs
c) Select word at K134 pins N, R. T, V.
d) Second K161 can select word at K134 inputs
e) Scanning and word-address K161s may be swapped
f) This system is expandable in two dimensions also

Note: The K681 Lamp Driver lacks the noise immunity and output slowdown designed into all of the general-purpose K-Series logic modules. For this reason it is important to take advantage of congruent pin assignments by assigning adjacent module slots to K161, K681, K281, and K134 modules used in memory applications.

PARALLEL COUNTERS

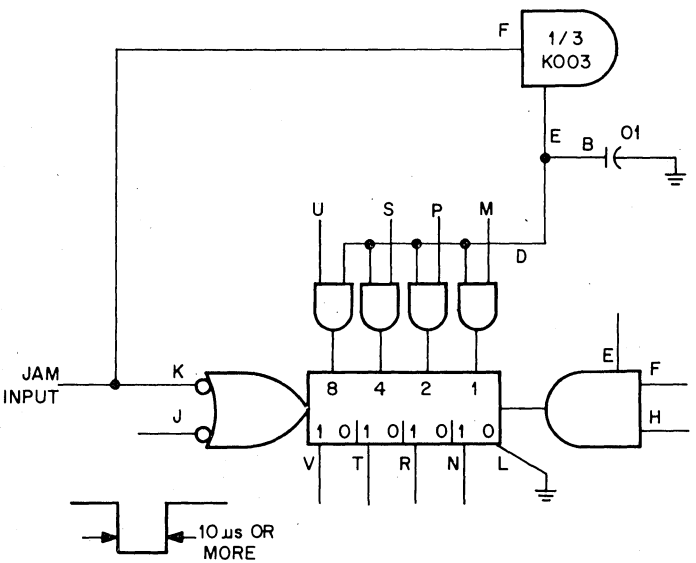
The counters shown elsewhere in this handbook are "serial" counters: that is, the input to a counter module of high significance is the simple output of the next less significant flip-flop, resulting in a time difference between groups of outputs (within a given K210, K220, or K230 module all outputs switch essentially simultaneously).

If a long counter is driving a large decoder, or if flip-flop outputs from different parts of the counter are being gated together for any purpose, carry propagation time down a serial counter can give rise to false transients lasting several microseconds from the decoder or gating. In effect, the carry propagation time causes the counter to pass through one or more wrong counts on the way to the correct state.

The solution is to feed count pulses in parallel to all modules simultaneously, but gating the pulses to modules of high significance with the "1" outputs from all bits of lesser significance. Observe that modules of higher significance would need input gates expanded to 9, 13, or 17 inputs for 12, 16, and 20 flip-flop counters respectively.

JAMMING DATA INTO K220, K230

The "clear" and "read ones" inputs on these modules may be combined to obtain the effect of a "jam." That is, completely new data may be stored in a single operation regardless of previous flip-flop states. However, the "read ones" (pin D) input must wait to rise at least 4 microseconds after the clear input rises, to give the clearing action time to die away. A simple way to accomplish this delay is shown below.



DIODE AND CAPACITOR IN K003 AS RISE DELAY

This circuit gives about 10 microseconds of rise delay. The K003 capacitor discharges on jam input fall through the K003 diode, but the diode opens to force the pin D load current alone to recharge the capacitor, which takes time. The delay may be reduced if desired to about 5 microseconds by connecting another one milliampere pull-up (pin D to pin E on the K003 shown above).

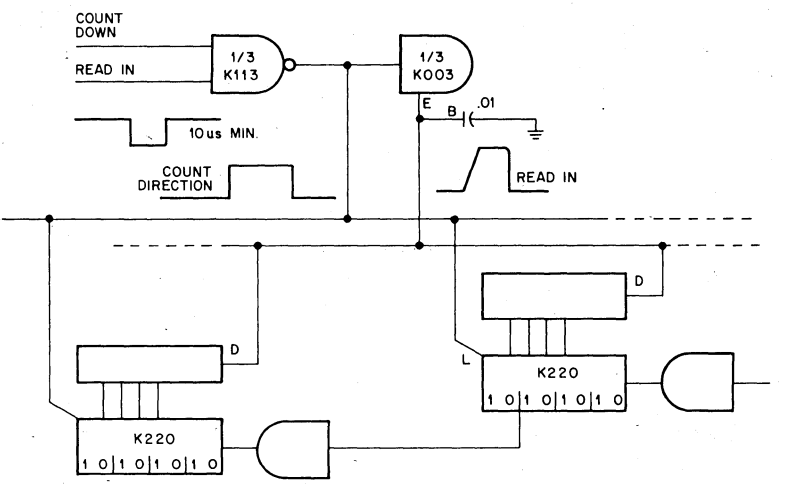
Several "read ones" inputs may be driven from a single K003 section, provided the capacitance is multiplied by the same number. However, the heavy capacitive loading may cause slow falltimes on the jam input line. Pin D inputs on K220 and K230 may be regarded as 1 milliampere loads in this application.

K220 READIN ON DOWN-COUNT

Because of the simple one-wire cascading feature built into the K220 up/down counter, a restriction is placed on the readin capability to prevent "borrow" from propagating erroneously.

If a "1" is read into the most significant *flip-flop* of one K220, the next more significant K220 *module* will receive a low-to-high transition at its count input. If this module has zero volts at its pin L, it will regard this low-to-high transition as a borrow signal and will accordingly count down one step.

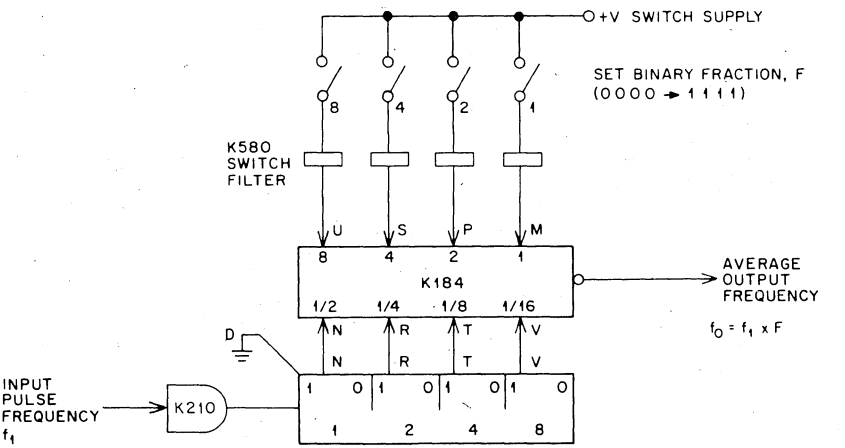
To prevent such erroneous down-counts, it is necessary to raise the count direction line to a logic "1" (count *up*) for at least 4 μsec before and 4 μsec after the low-to-high transition at the readin gate, pin D. The diagram below shows how this may be accomplished, using the same delay technique shown on the preceding page.



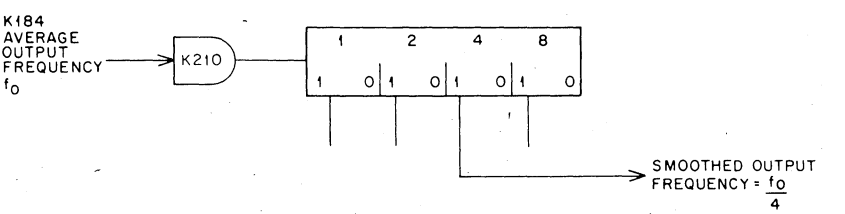
DEC Module assembly lines combine automated manufacturing steps with visual inspection and computer controlled testing.

K184 RATE MULTIPLIER

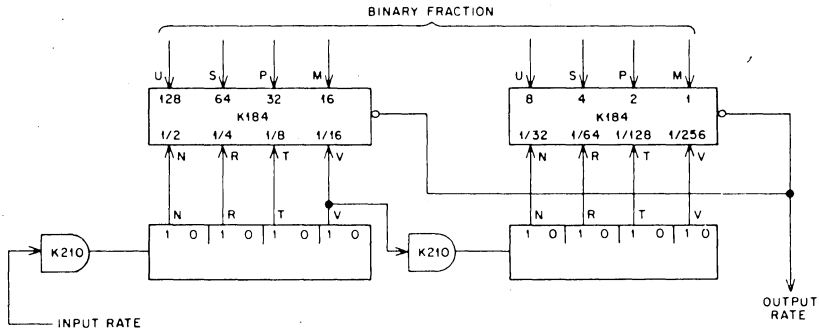
The K184 Rate Multiplier accepts an input pulse frequency f_1, via a Binary Counter, multiplies this by a Binary Fraction F, and emits a pulse train, with average frequency $f_0 = f_1 \times F$. Note that f_0 is always less than f_1, also that the Counter and Fraction are Binary; the Fraction being presented in reverse order to the K184. FIG 1a shows how a K184 with the Binary Fraction preset on switches, generates the product frequency f_0.



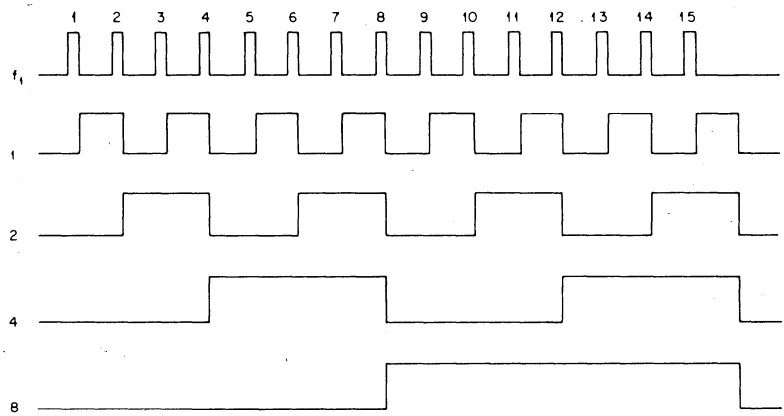
Since this frequency is average, and not periodic, some digital smoothing may be added; f_1 can then be preselected, to control Hydraulic or Pneumatic Valve opening and closing rates, Stepping Motor velocities etc.



The resolution of the system is increased by cascading K184 modules and Counters. The K184 outputs, f_0, are simply commoned in this case.



8 BIT RATE MULTIPLIER



BINARY-CLOCK COUNTER OUTPUTS GENERATED BY f_1

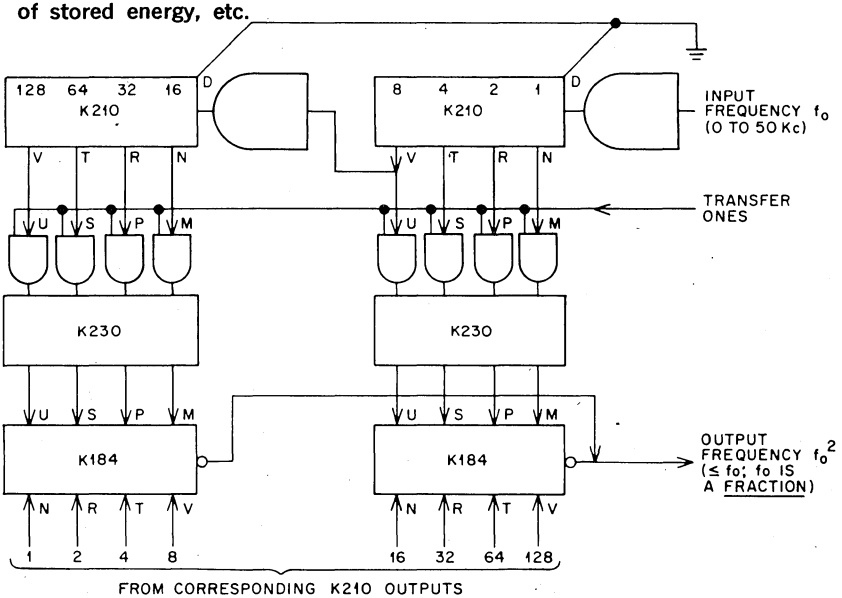
PRINCIPLE OF K184 OPERATION

As shown above, the input clock frequency f_1 generates a binary sequence in the Clock Counter. The 1, 2, 4, and 8 Counter outputs, when connected to the K184 Clock inputs, generate pulses in the K184 on 0→1 transitions. Note that no two 0→1 transitions are ever in coincidence. Also notice that of all possible pulses, all but one are obtainable if each 0→1 transition is allowed through; but when all bits simultaneously return to the zero state, no pulse is available. Thus the maximum output rates for 4, 8, and 12 bit rate multipliers are 15/16, 255/256, and 4095/4096 of the input rates.

2. Uncritical loads, where spurious conduction for several milliseconds could not be damaging or hazardous. Since the other components are rated for 240 volt service already, simply remove the transient-clipping varistors. These are axial-lead-devices with a black body and metal end-caps, about 2 cm long and 8 mm diameter. Lamp return voltage may be supplied from the load common (240 volts) if a rectifier diode is provided to obtain half-wave operation. In a system containing both modified and unmodified circuits segregate and mark them. Use of unmodified units with 240 volts directly will destroy them by grossly overheating the varistors.

RATE SQUARER

This circuit shows one of the many fascinating and useful tricks possible with rate multipliers. Here the output rate varies as the square of the input rate, so that, for example, a flywheel rotation rate could be read out in units of stored energy, etc.



SEQUENCE OF OPERATION

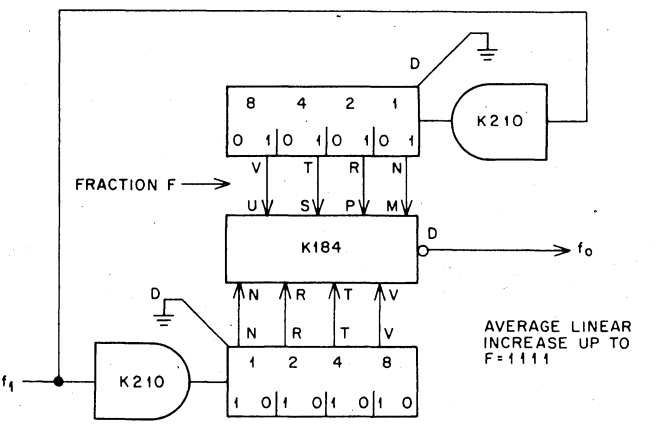
0. K230 holds previous rate number; K210s cleared
1. Gate f_o to K210 counter for fixed period
2. Stop counter at end of internal; clear K230s and read in
3. Clear K210 and return to step 1.

MODULE COST	
2 K210 @ $27.	$ 54.00
2 K230 @ 36.	$ 72.00
2 K184 @ 18.	$ 36.00
TOTAL excluding control	$162.00

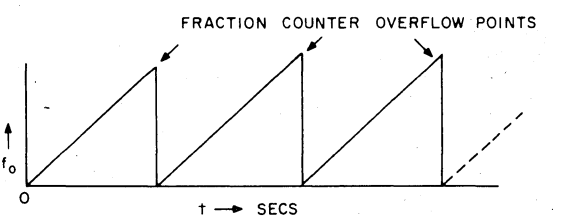
NOTE: f_o is regarded as a fraction, where 1.0 is that frequency which just fills the counter during the count interval. Average output rate is the product of current count rate times the average rate in the previous interval.

K184 AS A DIGITAL INTEGRATOR

If the fraction F, to a K184 is derived from a Counter also incremented by the input frequency f_1, f_0 increases, on average, in a linear fashion.

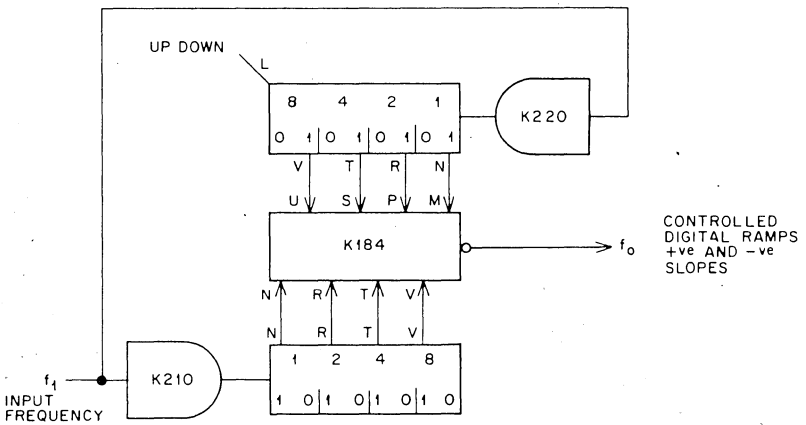


As shown below, if the FRACTION K210 overflows from 1111 to 0000, f_0 will fall to zero and begin again to increment as before. The result is a Digital Sawtooth generator. f_0 against time t is shown here.

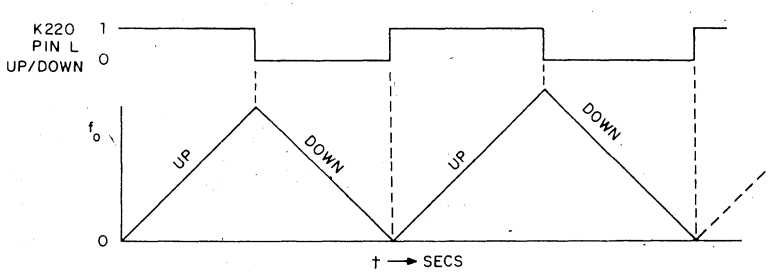


Resolution can be increased by module cascading. If the Fraction Counter is a K220 UP/DOWN Counter connected for Binary operation,* then the slope of f_0 can be reversed and controlled symmetrically.

*(Pins BD, BE grounded)



The output of the K184 shown above, is on average, a linearly increasing frequency when the K220 counts UP, and a linearly decreasing frequency on K220 count DOWN. This facility is of use in controlling Stepping Motor Acceleration on K220 UP counts, and Deceleration on DOWN counts. The Fraction Counter must not be allowed to overflow.



The response of f_o shown above is average and must be smoothed digitally to remove unacceptably large variations in pulse spacing; which would cause for example a Stepping Motor to change velocity instantaneously during the Acceleration period.

For more on rate multipliers, see references on K184 data page.

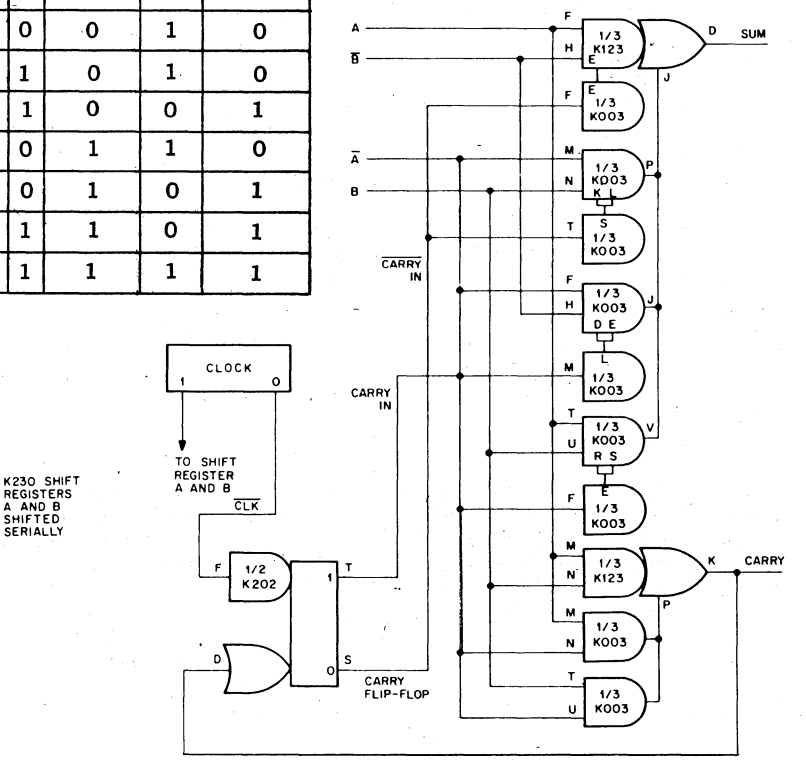
SERIAL ADDER

When speed is not paramount, one can sum the contents of two K230 shift registers bit-by-bit at low cost. The result can go back into one of the source registers.

Clock output CLK, 1 to 0 transitions, shift serially the addend and augend contained in K230 Shift Registers, A and B. The contents of the Registers are serially summed with the Carry In bits from the Carry flip-flop.

Carry Out signals, and CLK signal 1 to 0 transitions, cause the Carry Out flip-flop to be Set or Reset, ie Carry or No-Carry.

A	B	carry in	sum	carry out
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1



STEPPING MOTORS

INTRODUCTION

There are two fundamental parts to the design of any stepping motor drive system: Designing the logic for correct sequencing, and electromechanical design. Several logic designs are shown on the next few pages; here first is a brief discussion of electromechanical aspects.

Much of the emphasis in stepping motor system design is on maximizing stepping rates. There are two components in maximizing stepper speed: Maximizing the rate of motor current rise and delay, and operating within the motor's limitations of torque, friction and stiffness during the critical acceleration — deceleration phase. Successful design results in accurate stepping with no missed or gratuitous steps.

To optimize the response speed of any magnetically operated device, a minimum requirement is that the ratio of circuit inductance to circuit resistance be less than the desired response time. Thus if response of 1 millisecond is required in a one henry winding, the total of winding resistance and series padding resistance should be greater than 1000 ohms. If this ratio (L/R or henries-divided-by-ohms) equals or exceeds the desired response time in seconds, electrical effects tend to be the dominant limitation on speed and override mechanical factors.

The design problem is complicated by the increase in winding inductance as motion is accomplished. The inductance at turnoff may be many times the inductance at turnon in efficient devices such as solenoids. However, many types of stepping motors are designed to achieve maximum performance at the expense of efficiency, and the inductance of these motors may vary only a negligible amount (less than 10%) as rotor position changes. Since inductance ratios are generally unpublished, the best approach may be to start with equal resistance and then measure the actual current rise and fall times, increasing the turnoff resistance if necessary later. (In all of this, the driving transistors are assumed to switch in zero time, as they respond in microseconds whereas L/R ratios are generally in the millisecond range.)

Notice that during turnoff the switching transistor experiences a voltage equal to the supply voltage for the equal case, but larger than the supply voltage if additional turnoff resistance Rpp is added. Since the voltage rating of the driver is the limiting factor on the minimum L/R that can be achieved with a given inductance, the ratio of drive transistor voltage rating to supply voltage should be adjusted as indicated below for optimum electrical response:

$$\frac{V_T}{V_S} = \frac{L_{Off}}{L_{On}} = \frac{R_L + R_P + R_{PP}}{R_L + R_P}$$

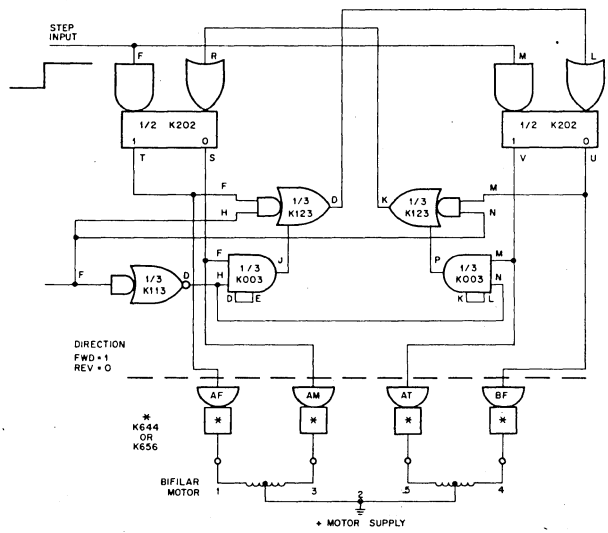
Operating within the stepper's limitations of torque, friction, and stiffness during acceleration and decelelration is trickier than it looks, especially since some crucial constant may be omitted from published specifications for the device. There is often the wish to avoid abrupt (full frequency) starts and stops to achieve maximum stepping rates. Often only one or two steps need to be slowed to achieve maximum acceleration error-free. Too gradual change in stepping rate can actually encourage errors if inertia is moderate and friction low, caused by an actual resonant reversal of rotation at some particular step.

All of the logic circuits shown on the next pages can be used with any clock rate profile. It is best, however, to use an abrupt start-stop system unless the need for ultimate performance warrants a full study of system dynamics, including the use of a tachometer on the stepper shaft to observe the effect of proposed frequency profiling.

SLO-SYN* STEPPER SEQUENCER

A K202 flip-flop module, connected as shown, forms a reversible switch-tail ring counter. With the "direction" input logic 1, 1 to 0 transitions on the "step input" index a bifilar stepping motor forward. With logic 0 on the direction input, the direction is reversed.

A d.c. driver controlled by the switch-tail counter provides power for the stepping motor.

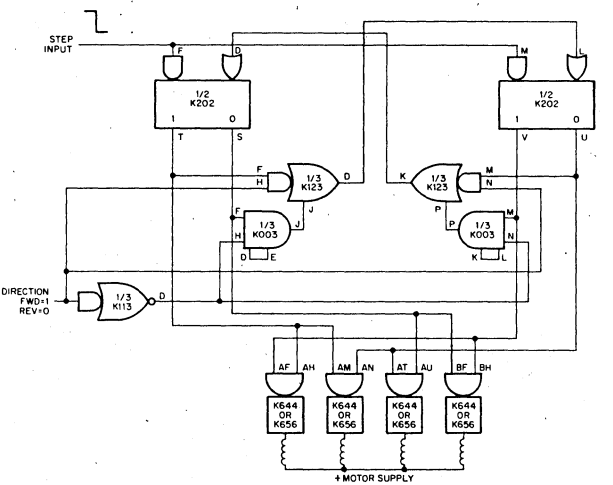


*SLO-SYN is a trademark of Superior Electric Co.

RESPONSYN* STEPPER SEQUENCER

This sequencer uses the same two bit shift register with inverted feedback as the SLO-SYN sequencer, but the outputs are gated to obtain the different drive pattern required by these motors.

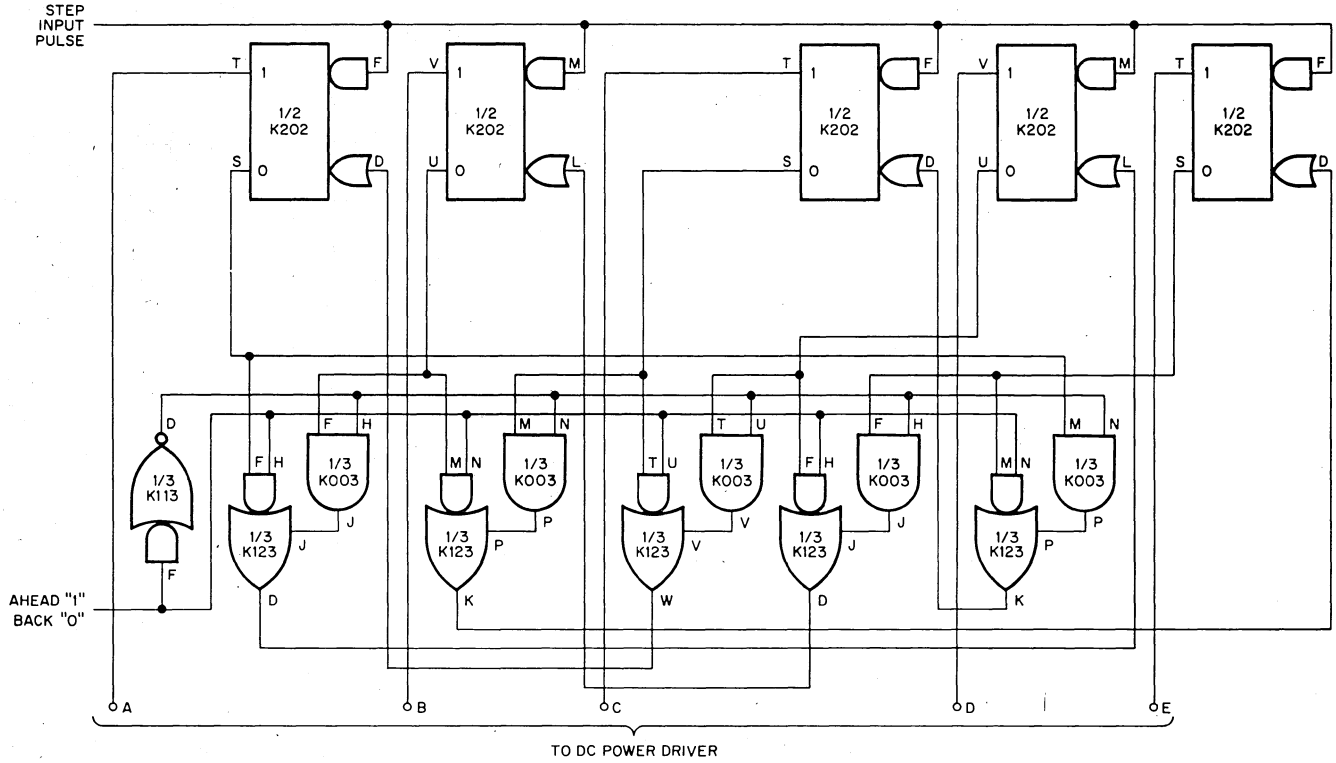
*RESPONSYN is a trademark of United Shoe Machinery Corp.



FUJITSU STEPPER SEQUENCER

FUJITSU Stepper motors can be driven forward and reverse, with the module arrangement shown. The table describes the stepping sequence required by a FUJITSU 5 torquer motor (with or without hydraulic servo amplifier).

STEP	A	B	C	D	F
0	X	X			
1	X	X	X		
2		X	X		
3		X	X	X	
4			X	X	
5			X	X	X
6				X	X
7	X			X	X
8	X				X
9	X	X			X



FUJITSU STEPPER MOTOR SEQUENCE.

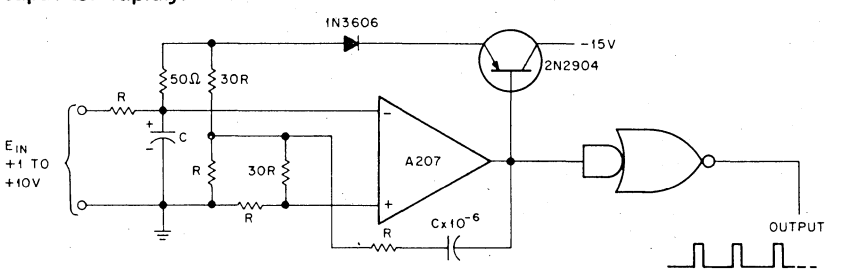
ANALOG-TO-FREQUENCY CONVERTERS

When a relatively slow-varying or constant analog signal must be transmitted some distance through noise, some form of current-to-frequency or voltage-to-frequency conversion is appropriate. There are really two distinct sets of benefits to be gained:

1. Analog noise will be averaged, and may be almost entirely nullified even if it is comparable to the signal in amplitude. Normally the frequency is sampled for an exact internal number of line-frequency cycles to average power frequency coupling to zero. High noise frequencies are mostly averaged out by the conversion device itself.
2. Digital noise will be averaged also, since one or two extra pulses or missed pulses represent a small fraction of the total number. In addition, the digital form of the measured quantity is inherently noise resistant since noise less than the switching threshold at the receiver has truly no influence whatever.

The improved transmissibility of analog data both before and after the conversion to an equivalent frequency has to be paid for in reduced speed of response to changes. (From the viewpoint of an information theorist, such a transmission mode would be said to deliver high redundancy and low information rate.) But many sensors on slowly varying processes which are distant from an associated digital system are ideally suited for this treatment.

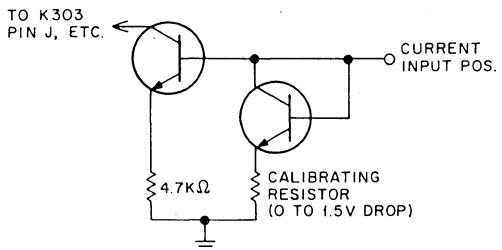
The diagram below shows how an operational amplifier may be utilized to provide direct conversion from an analog voltage to an equivalent frequency with errors in the tens of millivolts. This scheme measures how long current in the input resistor R takes to charge the capacitor C ten millivolts. Each time this occurs, the output switches to the other state and discharges the capacitor rapidly.



VOLTAGE-TO-FREQUENCY CONVERTER

Resistance R should be about 1000 to 10,000 ohms to achieve a balance between error due to wide pulsewidth at high frequency and error due to the biasing effect of amplifier input current. To minimize the effect of amplifier switching time, capacitor C should be large enough (100 mfd with R=1000Ω, for example) to limit maximum full-scale frequency to around one kiloHertz. Nearly any quality silicon diode and PNP transistor with at least 30 volt ratings could be used, and the small capacitor with its associated current limiting resistor is not critical either. Other components should be selected carefully to minimize drift and temperature coefficient.

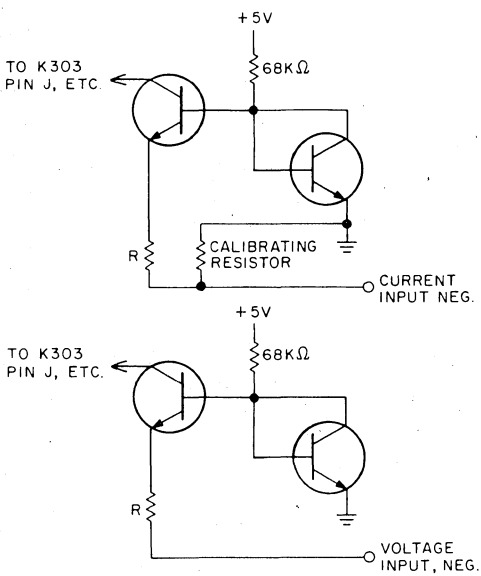
K303 clock circuits can be modified by the additional parts shown below to achieve lower performance conversion at a saving. Basically, a current source controlled by the input signal being converted replaces the action of the timing resistor R shown in the Handbook diagrams. Transistors can be any high gain Silicon NPN type such as 2N2219.



NOTE:
THE SMALL VOLTAGE DROP (1.5V MAX) AVAILABLE LIMITS LINEARITY TO ±5% OR SO FOR THIS CIRCUIT.

FOR POSITIVE INPUTS

If output frequencies are counted for an integral number of power-frequency cycles, clock filler will be compensated along with line frequency pickup on the analog leads.



NOTE:
USE LARGEST PRACTICABLE VOLTAGE SWING. RESISTOR R SHOULD BE APPROXIMATELY 3KΩ FOR EACH VOLT OF FULL-SCALE INPUT SWING. LINEARITY CAN BE IMPROVED TO ABOUT ±1% OF FULL SCALE BY USING INPUT VOLTAGE SWINGS UPWARDS OF 10 VOLTS.

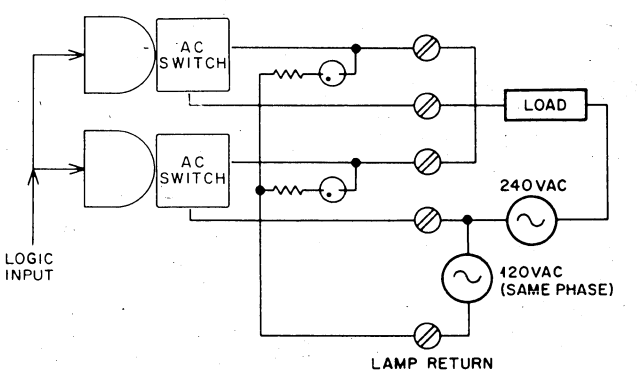
FOR NEGATIVE INPUTS

USING K604, K614 WITH 240 VOLTS

These isolated AC switches have semiconductors and other components rated for 240 volt service. However, the Triac switches used were rated primarily for phase control applications. The difference is that some switching applications require an "off" switch to remain substantially off in the presence of transients and noise, without conducting for even one half of one cycle. Since a transient voltage, larger than the breakdown voltage of these devices (400 volts) can cause them to start and remain conducting until several milliseconds later when the load current returns to zero, the K604 and K614 contain transient-clipping devices across each circuit which go into conduction between the peak voltage of a 120 volt line (200 volts) and the Triac breakover voltage (400 volts).

Triac switches are not readily available at present with breakdown ratings above 400 volts. However, K604 and K614 switches can successfully be used in 240 volt service if two types of application are distinguished:

1. Critical loads: For example, a hydraulic solenoid valve controlling the liquid metal on a die-casting machine, an ignition transformer on a process boiler, a trip solenoid on a punch press; any use involving both fast response and a potential safety hazard. For such applications, two circuits should be connected in series, so that any undesired conduction will be limited to the actual duration (usually microseconds) of a transient or noise spike. Wiring K614 outputs in series is simple because two terminals are provided on each circuit. To put K604 outputs in series, use K782 terminals or see K716 data page for connector cable information. Note indicator lamp connections in diagram below.



SERIES CONNECTED AC SWITCHES

DEC PRODUCT SUMMARY

DIGITAL manufactures a broad line of general purpose computers and offers a unique line of peripheral equipment and options. PDP-10 is the largest DIGITAL PDP (Programmed Data Processor) computer. PDP-10 is an industry leader in multi-program time-sharing with over one million user hours already logged and proven software. The 36-bit PDP-10 will time-share, batch process, and run hybrid-simulation all simultaneously at an amazingly low price. The 18-bit PDP-9/I and 9/L are medium sized DIGITAL computers at small computer prices. PDP-9/I offers extensive processing power, background/foreground programming, and many real-time capabilities. And the 12-bit PDP-8 family has made DIGITAL the world's leading manufacturer of small computers. PDP-8, the all time winner, was the first computer to break the $20,000 price barrier and then the PDP-8/S broke the $10,000 barrier. Now, their faster, more economical and more compact successors PDP-8/I and PDP-8/L offer TTL integrated circuit module construction. Many manufacturers have found PDP-8 family computers ideal to build into an integrated system. DIGITAL, for example, builds PDP-8 family computers into an expanding group of systems called Computerpacks. These are integrated hardware and software packages for turnkey use in a number of computer applications. DIGITAL has several Computerpacks for the laboratory, others for typesetting, navigation, education, industrial control and outer acq. and small computer time-sharing. Many original equipment manufacturers use PDP-8 family computers as the central processor for their systems.

PDP-8/I and PDP-8/L

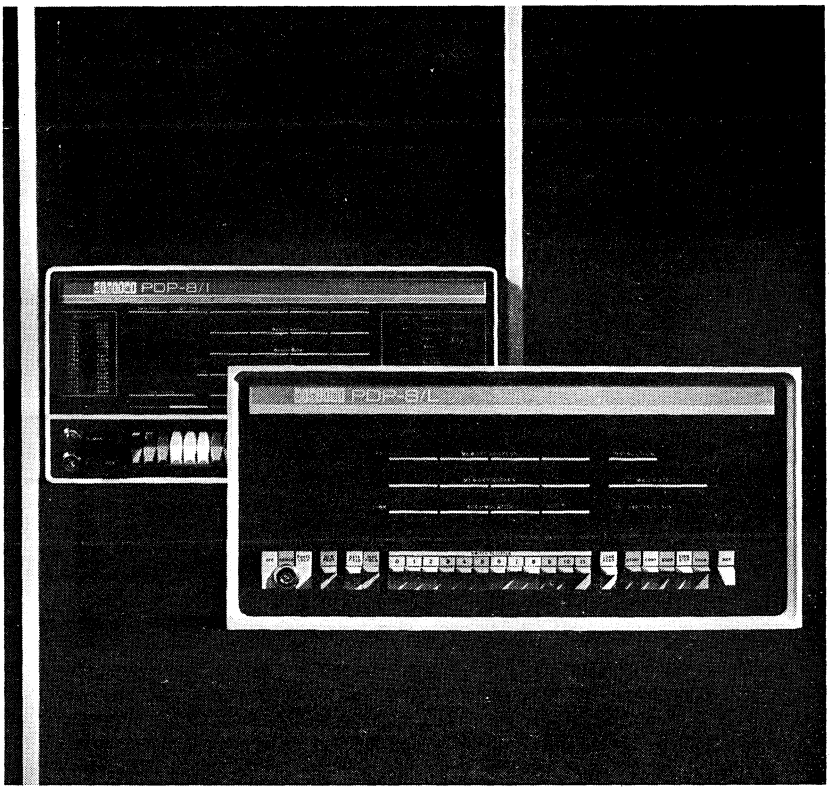
PDP-8/I and PDP-8/L are the latest members of the PDP-8 Family of general purpose computers. They are the faster, smaller and more economical successors to the over 3,000 PDP-8 Family computers installed all over the world.

Both PDP-8/I and PDP-8/L are built around the same 4,096-word, 12-bit core memory and fully parallel central processor. Both have TTL integrated circuits throughout. Both come with a big software package that is compatible throughout the PDP-8 Family. And PDP-8/I and PDP-8/L inherit a world-wide service organization renowned for its speed and dependability. PDP-8/L is the lowest cost full scale digital computer available. It comes in a very neat, small package with a very neat, small price. Just right for plugging into anybody's integrated system. PDP-8/I has the same basic capability plus an internal peripheral control and data break panel for plug-in expansion. The PDP-8/I is faster, slightly more expensive, and more flexible than the PDP-8/L. That's because the 8/I is designed for those who need plug-in expansion and the 8/L is designed for those who don't.

Both machines are built in the Digital tradition. They are tested and retested by skilled engineers and sophisticated computerized test equipment.

8/I Specifications:
Word Length: 12 bits
Memory: 4096 to 32,768 words; cycle time 1.5 microseconds
Add Time: 3.0 microseconds
In-Out Transfer Rates: 7,992,000 bits per second
Standard I/O Device: ASR-33 Teletypewriter with paper tape reader and punch

8/L Specifications:
Word Length: 12 bits
Memory: 4096 to 8196 words; cycle time 1.6 μsec
Add Time: 3.2 microseconds
In-Out Transfer Rates: 7,500,000 bits per second
Standard I/O Device: ASR-33 Teletypewriter with paper tape reader and punch


DIGITAL PDP-8/L
DIGITAL PDP-8/L

PDP-9 and 9/L

The PDP-9 is a general-purpose computer designed to handle a variety of on-line, real-time scientific applications calling for more power and flexibility than offered by the PDP-8. The basic PDP-9 features 8,192 words of 18 bit core memory; a real-time clock; a 300-character-per-second paper tape reader; a 50-character-per-second tape punch; and input-output teleprinter (KSR-33). Input/Output an be via programmed transfers, data channel transfers, or direct memory access.

Single address instructions are used, with auto-indexing and one level of indirect addressing permitted. A single memory reference instruction can directly address any location in a block of 8,192 words of memory. PDP-9 has a Direct Memory Access channel plus four built-in Data Channels.

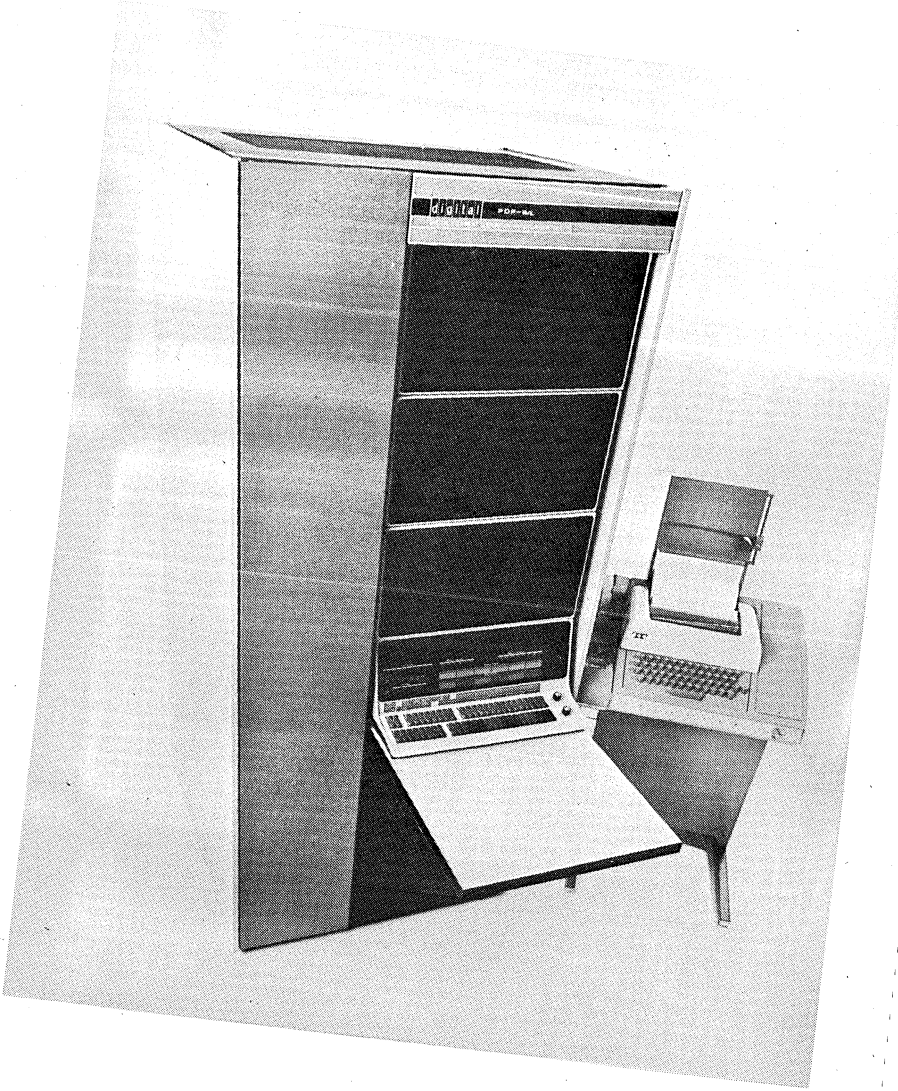
A comprehensive software package including FORTRAN IV, MACRO Assembler, a monitor system, and diagnostic routines is provided with the basic machine. With the modular software package, PDP-9 users can program in a device-independent environment to take full advantage of configurations with mass storage devices and central processor options. And with the PDP-9 background/foreground monitor, new software can be tested concurrently with on-line system functions.

The $19,900 PDP-9/L, a smaller version of the PDP-9, is available at a 4096-word level that fits easily into a dedicated systems environment. Its basic software includes COMPACT, a complete programming system for the 4K PDP-9/L, with Assembler, Editor, Math Package, debugging programs (ODT, Trace), and utility programs, all with complete upward compatibility. Expanded, the PDP-9/L can take full advantage of the Advanced Software System developed for the PDP-9.

Specifications:

- 4096 18-bit words of core memory, expandable to 32,768 words
- 1.0 microsecond cycle time (1.5 microseconds on 9/L systems)
- 8 data channels
- Up to 256 input/output devices
- COMPACT, a complete software system for the 4K PDP-9/L
- Advanced Software System for larger machines, including FORTRAN IV and background/foreground monitor

Options: DECtape, IBM-compatible magnetic tape, displays, A/D converters, line printers, card readers, plotters, etc.


digital
PDP-8/L

PDP-10

PDP-10 is an expandable, 36-bit computer system. All PDP-10 systems begin with two basic hardware elements: central processor and core memory. The same central processor is used in every PDP-10 configuration, but core memory can be composed of any mix of several modules. The modules vary in size, speed, and cost.

The PDP-10 includes an extremely powerful processor with 15 index registers, 16 accumulators, and from 8,192 to 262,144 words of 36-bit core memory, a 300-character-per-second paper tape reader, a 50-character-per-second paper tape punch, a console teleprint, and a seven-level priority interrupt subsystem. The PDP-10 features an I/O bus which provides 200K word/sec transfer rate; interfaces up to 128 devices with processor. It has 366 instructions, all different and logically complete.

The PDP-10 is designed for on-line and real-time, time-sharing, batch processing, and hybrid simulation applications such as physics and biomedical research, process control, as a departmental computation facility, in simulation and aerospace, chemical instrumentation, display processing and as a science teaching aid.

The software package includes real-time FORTRAN IV, BASIC, a control monitor, a macro assembler, a context editor, a symbolic debugging program, an I/O controller, a peripheral interchange program, a desk calculator and library programs. All software systems assure upward compatibility from the standard 8,192 words of memory through the multiprogramming and swapping systems at both the symbolic and relocatable binary level.

PDP-10 features a 1-microsecond cycle time, a 2.1-microsecond add time, I/O transfer rates up to 7,200,000 bits per second and a modular, proven software package that expands to make full use of all hardware configurations. Memory can be expanded in 8,192 word increments to the maximum directly addressable 262,144 words.

PDP-12

Digital's PDP-12 is a general-purpose computer system. It is designed as a simple to operate, yet uniquely flexible tool for a wide variety of research and real-time data handling applications.

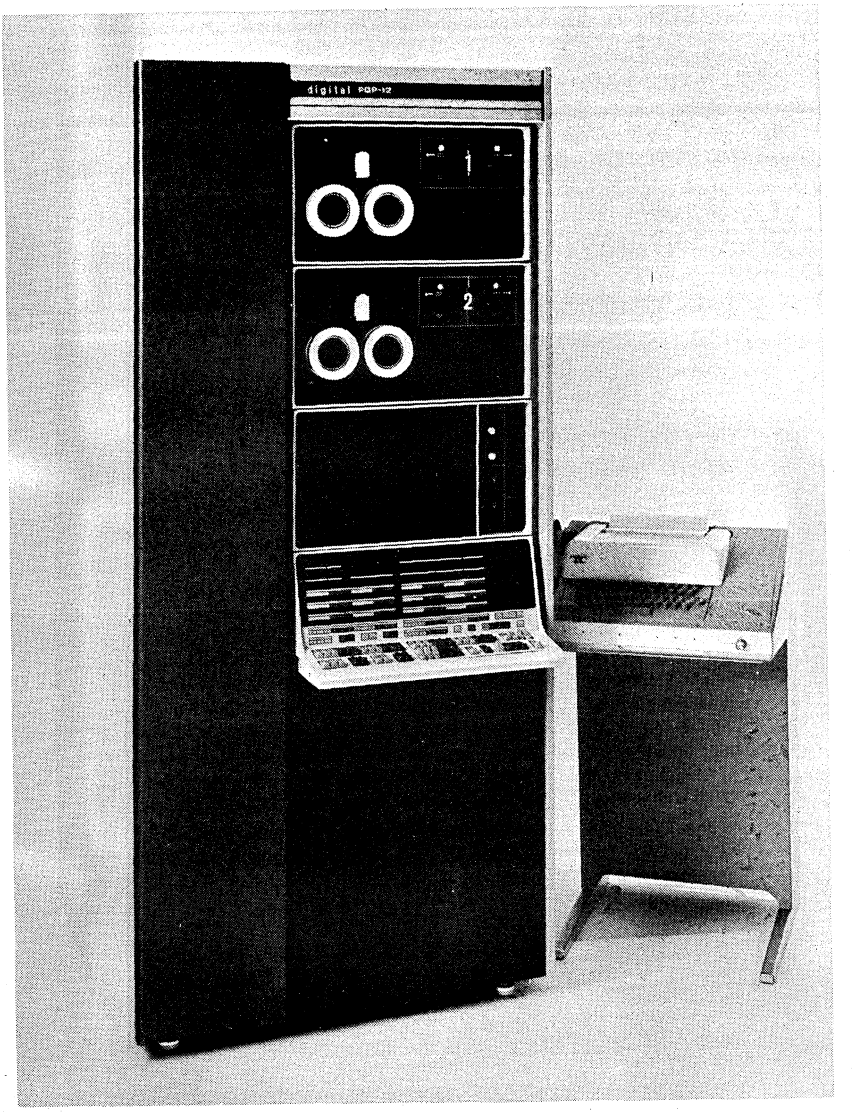
Performance characteristics of the PDP-12 have been optimized around a complete hardware/software system, rather than an expandable minimum configuration. The PDP-12 systems concept works to the advantage of users at all levels of programming sophistication. By simplifying programming tasks, the PDP-12 frees users from the mere mechanics of program preparation to concentrate on the more creative aspects of their work.

The following is a brief list of some of the PDP-12's outstanding features:

- All-new, unified display-based programming system
- Automatic program loading from magnetic tape
- Built-in program debugging hardware
- 7"x9" CRT display with graphic and alphanumeric capabilities
- Large existing library of applications programs
- TTL integrated-circuit modules throughout
- LINCtape-addressable, bi-directional program and data storage
- Free-standing cabinet and console table

Specifications:

- 4,096 12-bit words of core memory, expandable to 32,768 words
- 1.5 microsecond cycle time
- 43 basic instructions including 29 memory reference instructions
- 15 auto-index registers
- 6 programmable SPDT relays
- 6 sense switches
- 12 external sense lines
- Peripherals including 16-channel A/D converter, DECtape units, and new 7" x 9" display, all fully buffered
- Software: new unified display-based system; FORTRAN, FOCAL, BASIC, mathematical, maintenance, and utility routines


digital PDP-12
1
2

COMPUTER LAB

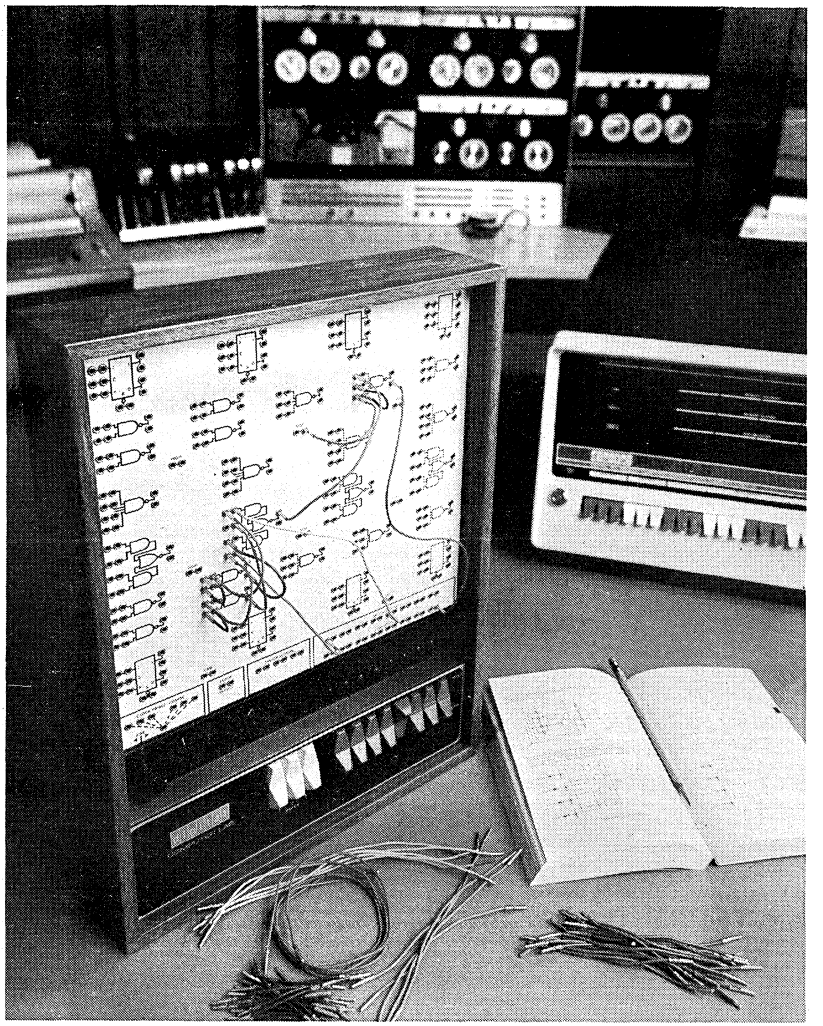
The COMPUTER LAB is a new high performance low-cost digital logic trainer. The COMPUTER LAB uses the same monolithic integrated transistor-transistor logic circuitry used in DIGITAL's latest PDP computers.

The digital logic fundamentals presented by the COMPUTER LAB constitute the basic knowledge required to pursue a career in computer technology as computer technician, engineer, programmer or operator. The COMPUTER LAB will also help the math-oriented student to understand "New Math" concepts because computer logic operates with binary numbers according to Boolean algebraic laws.

Wiring is easy because of the standard logic symbology used on the front panel and the color coded Patchcords which are easily inserted and removed. An improper circuit will not damage the COMPUTER LAB. The faulty circuit merely "waits" for correction.

Features:

- Transistor—Transistor logic circuitry as used in DIGITAL's PDP computers
- Teaches modern computer logic
- Easy to use: MIL-STD 806 logic symbology on front panel
- Portable: Dimensions of 12½" x 17" x 3¼", weighing only 11 lbs.
- Comprehensive Workbook provides:
  - —Ten detailed chapters
  - —More than 30 experiments
  - —Over 200 hours of laboratory study
  - —Dozens of tables and diagrams
  - —An extensive appendix of supplementary information
- Teacher's Guide with answers, additional text, extra problems, and course plans.
- Low cost: COMPUTER LAB, Workbook and Patchcord set, ready to use $445.00



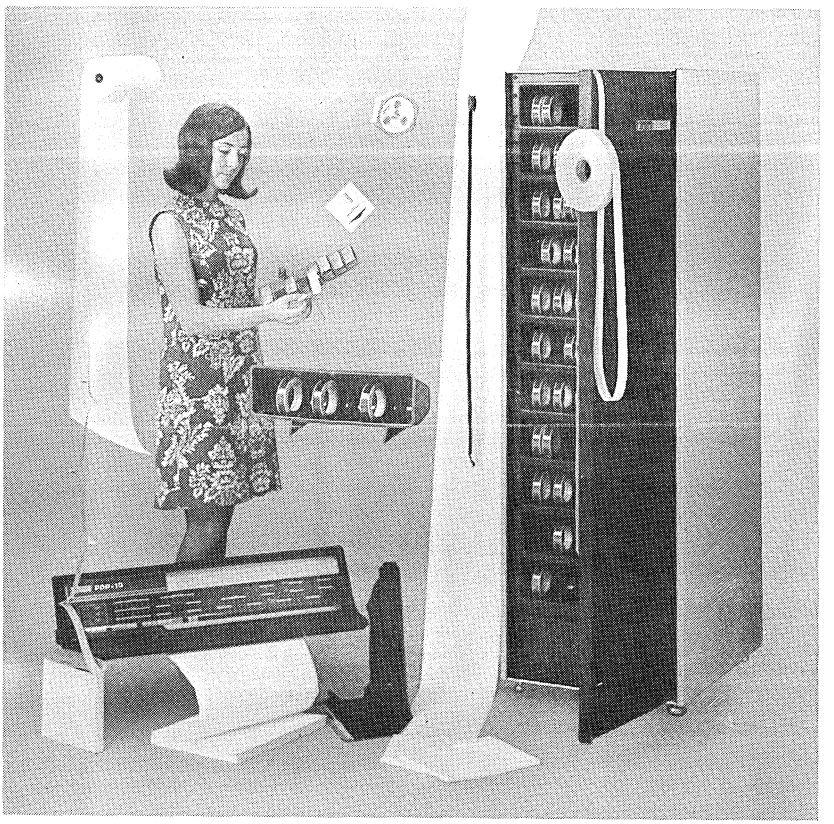
DEC SUPPLIES

Digital Equipment Corporation offers a complete line of computer operating supplies. These supplies are guaranteed to work with all PDP computers. In fact, DEC equipment performs best when used with DEC supplies! The DEC Field Service personnel are trained to make adjustments in accordance with the specifications of DEC-sold supplies. These adjustments differ for supplies provided from other vendors.

The most important reason for using DEC supplies is their low cost. DEC supplies are, in some cases, 50% lower in price than those offered by other major suppliers. This is of particular significance when you realize how many of these items you purchase during the year.

DEC now provides fast delivery on all operating supplies because many are stocked locally at regional offices. All orders will be shipped within 48 hours to assure you the fastest delivery possible.

Part No.	Description	Price
74-3860	DECtape	$ 7.00 ea.
74-3860-1	LINC Tape	7.00 ea.
36-05363	Fanfold Paper Tape (1" wide)	45.00 case
36-05360	Oil rolled tape	36.00 case
36-05364	Paper Tape Trays (9¼" x 12")	3.30 ea.
18-09128	Empty DECtape Reels	.50 ea.
18-0932-01	DECtape Storage Racks (Cabinets)	9.00 ea.
18-09232-02	DECtape Storage Racks (Desk)	7.50 ea.
18-09139N	Printer Ribbons for DEC Line Printers	15.00 ea.
18-09137	Teletype Ribbon	20.00 box
36-05361	Printer Paper	15.00 box
18-09211	Paper Tape Gauge	8.40 ea.
18-09138	Roll Paper Tape Winders	3.50 ea.
18-09157	PDP-10 Console Cover	75.00 ea.



WIRE WRAP SERVICE POLICY AND PRICES

Wire Wrap Service Policy and Prices
As a service to those customers who are building multiple units, we will provide an automatic wire wrap service. This service will be available to anyone who has at least five like systems to be wired.

Inputs:
The customers should provide us with a deck of IBM cards for input to the wire list program. The deck must be prepared in accordance with the Standard DEC format and procedures.

Key Punching:
If a customer does not have a key punching facility available, we can provide punching services at the rate of $0.05 per card when cards have been listed on our forms DR-22.

One Time Charges:

24 Gauge Wire Wrap:
$320 minimum charge for up to four panels (1943, or equivalent in any other mounting arrangement) $25 for each additional panel.

30 Gauge Wire Wrap:
$200 minimum charge for up to two panels (H911 or equivalent in any other mounting arrangement) and $50 for each additional panel.
One time charges are not discountable.

File Maintenance Service:
If desired, DEC will maintain on file a magnetic tape record of the original source information for a period of two years. A service charge of $50, not discountable is assessed for this service.

In many cases the customer will want to maintain the magnetic tape in his own EDP center and DEC will provide him a tape in card image for $35.00/reel.

Purchase Orders:
A separate P.O. # must be issued to DEC for any Wire Wrap service. This is necessary for the following reasons.

1. Pricing of the wire wrap job cannot take place until the actual processing of the source deck has been completed (to determine wire count and charges for correction and re-run).
2. The module and mounting panels on the same order would be unnecessarily delayed by the above because the order could not be entered without complete price information. This could mean several weeks delay to the customer.

Errors/Corrections:
No ECO work will be performed on wired panels. This means DEC will not up-date wired frames to incorporate changes that may come into the house before shipment of the panel.

In addition, in those cases where errors have been found in a customer supplied card deck, the customer will be contacted to establish corrections. The customer will be charged a flat fee of $50.00. Correction charges are not applicable to discount.

Bussing:
Special bussing will be performed by DEC should it be required. The customer will be charged at the rate of $0.10 per point for special bussing not including the cost of the bus strip. For a charge of $5.00 DEC will provide to the customer a vellum of the appropriate mounting panel. Bussing will be done according to an appropriate marked up DEC drawing only. Special bussing will add at least two weeks to the normal delivery time.

Delivery:
The normal delivery for wire wrap panels is 4 to 6 weeks after receipt of both the purchase order and an accurate card deck. Additional time should be allowed for delivery if key punching and/or special bussing is required.

Prices:
The cost per wire for wrapping #24 wire is 33¢ and for #30 wire is 45¢.

Both applicable to standard module discount agreements.

Wiring Verification:
At no extra charge to the customer the wire wrapped panel will be verified. The only restriction being that the size of the panel be limited to 4 connector blocks high by 10 connector blocks wide. No price reduction will be allowed for elimination of the verification service.

Customer Receives:
The customer receives one copy each of the Name Sort, Pin Sort, To-From and Z level list. Additional copies will be provided at a cost of $10.00 each. The card deck and Gardner-Denver deck are the property of the customer and will be shipped to him upon completion of the job.

PRICE LIST AND NUMERICAL INDEX

		Price	Page
A123	Positive Logic Multiplexer	$ 58.00	230
A200	Operational Amplifier	130.00	232
A206	Operational Amplifier	190.00	234
A207	Operational Amplifier	45.00	236
A404	Sample & Hold	130.00	238
A613	12-Bit D/A Converter	250.00	240
A618	10-Bit D/A Converter, Single Buffered	350.00	242
A619	10-Bit D/A Converter, Single Buffered	375.00	242
A620	10-Bit D/A Converter, Double Buffered	400.00	244
A621	10-Bit D/A Converter, Double Buffered	425.00	244
A702	Reference Supplies	58.00	246
A704	Reference Supplies	184.00	246
A811	10-Bit A/D Converter	450.00	248
A990	Amplifier Board	4.00	250
A992	Amplifier Board	4.00	250
H001	Bracket	8.00	274
H002	Bracket	8.00	274
H020	Frame Casting	15.00	274
H021	End Plates	7.00	274
H022	End Plate Assembly	20.00	274
H704	Dual Power Supply	200.00	260
H707	Dual Power Supply	400.00	260
H710	Power Supply	200.00	262
H716	Power Supply	130.00	263
H800	Connector Block	8.00	269
H801	Replacement Contacts	2.00	269
H802	Connector Block	4.00	270
H803	Connector Block	13.00	271
H805	Replacement Contacts	4.00	271
H807	Connector Block	5.00	272
H808	Connector Block	10.00	273
H809	Replacement Contacts	4.00	273
H810	Pistol Grip Wire-wrapping Tool	99.00	290
H811	Hand Wrapping Tool	21.50	291
H812	Hand Unwrapping Tool	10.50	291
H813	Hand Unwrapping Tool	30.00	291
H814	Hand Unwrapping Tool	21.00	291
H820	Grip Clip	48.00	286
H821	Grip Clip	75.00	286
H825	Hand Crimping Tool	146.00	286
H826	Hand Crimping Tool	210.00	286
H910	Mounting Panel	280.00	276
H911J	Mounting Panel	151.00	278
H913	Mounting Panel	270.00	280
H914	Mounting Panel	125.00	280
H916	Mounting Panel	270.00	280
H917	Mounting Panel	260.00	280
H920	Module Drawer	170.00	283

		Price	Page
H921	Front Panel	5.00	283
H923	Slide Tracks	75.00	283
H925	Module Drawer	325.00	284
H950-AA	Cabinet	120.00	296
K003	Gate Expander	4.00	134
K012	Gate Expander	7.00	134
K026	Gate Expander	6.00	134
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HARDWARE

Comprises over 100 separate hardware and accessory items including power supplies, connector blocks, mounting panels, blank modules, and connector cards.

APPLICATIONS

Contains thirty-five applications notes and dozens of useful design notes that make this Handbook one of the most informative digital electronics handbooks available.

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