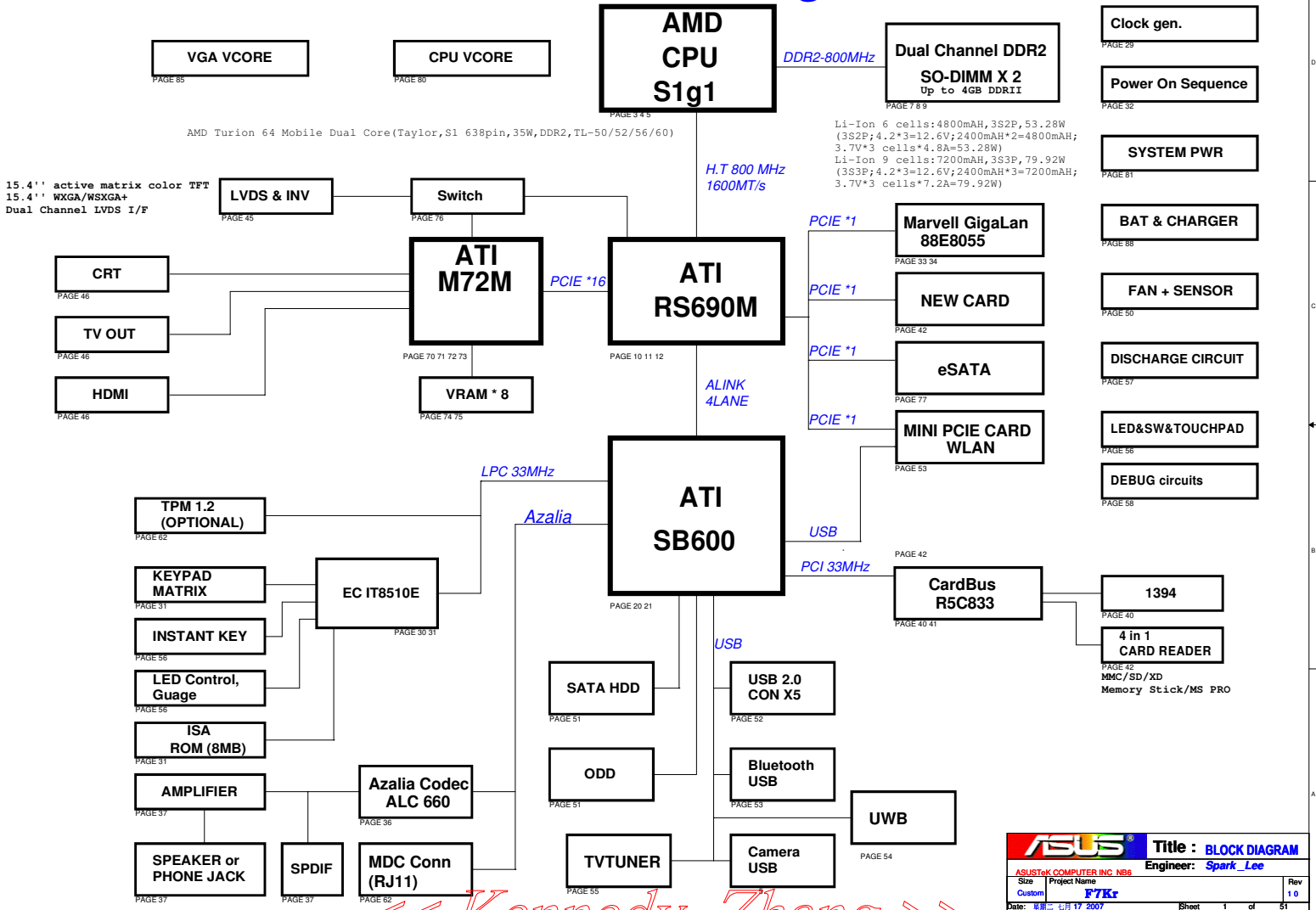
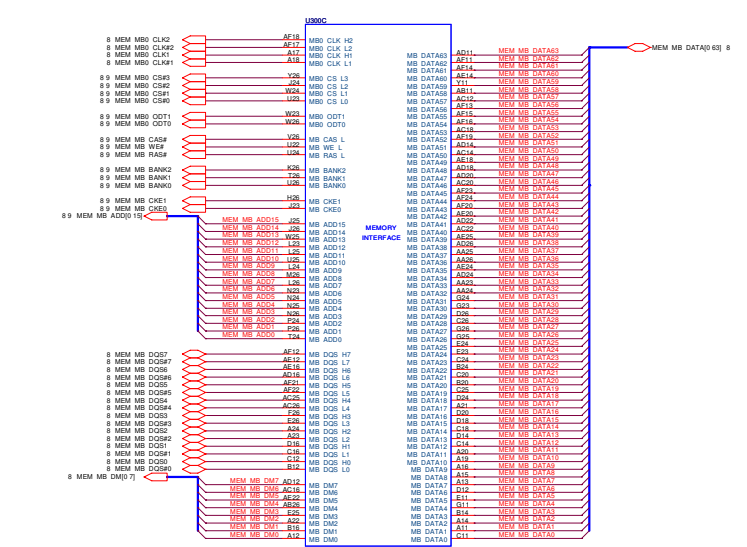
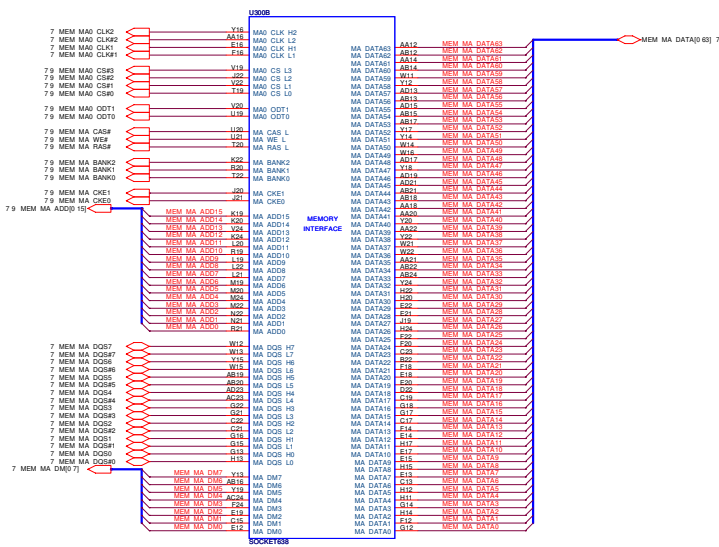


F7K Block Diagram



ASUS		Title : BLOCK DIAGRAM	
ASUSTeK COMPUTER INC. NBS		Engineer: Spark_Lee	
Site	Project Name		Rev
Custom	F7K		1.0
Date: 08-11-17 2007		Sheet	1 of 51



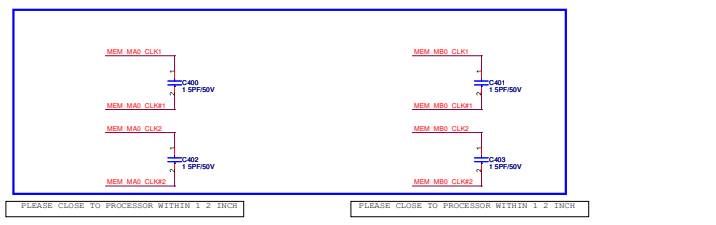
U000

7400	TPC28T	1	CPU RSVD MAO CLK#3	P20	RSVD MAO CLK H3	RSVD MA RESET L	H16	CPU RSVD MA RESET L	7401	TPC28T
7403	TPC28T	1	CPU RSVD MAO CLK#2	P22	RSVD MAO CLK L3	RSVD MA RESET L	H18	CPU RSVD MAO CLK#1	7403	TPC28T
7404	TPC28T	1	CPU RSVD MAO CLK#1	P24	RSVD MAO CLK L0	RSVD V DSTRB#	S3	CPU RSVD V DSTRB#	7405	TPC28T
7406	TPC28T	1	CPU RSVD MAO CLK#0	P26	RSVD MAO CLK L0	RSVD V DSTRB#	C1	CPU RSVD V DSTRB#	7407	TPC28T
							H6	CPU RSVD V DSTRB#	7408	TPC28T
							D5	CPU RSVD CORE TYPE	7410	TPC28T

MISC

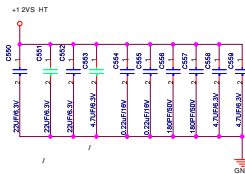
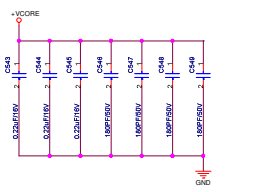
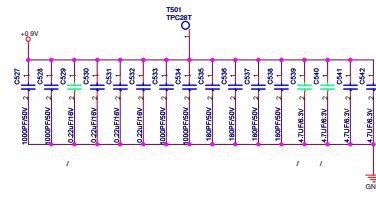
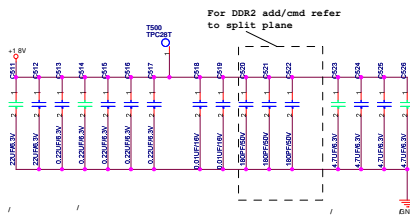
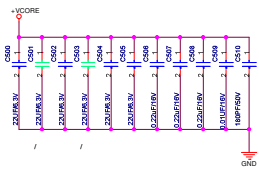
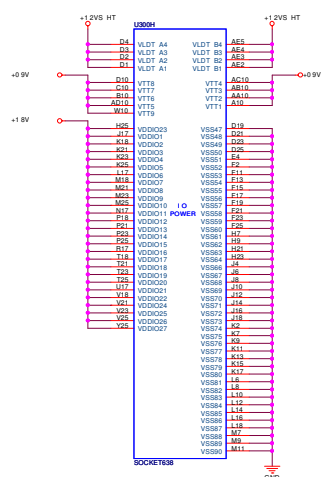
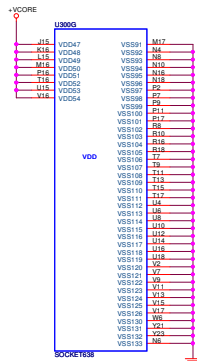
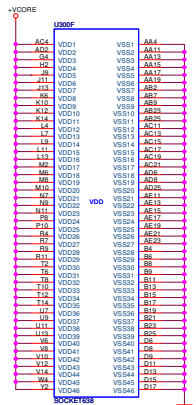
7411	TPC28T	1	CPU RSVD MB CLK#3	P30	RSVD MB CLK H3	FREE	B24	FREE
7412	TPC28T	1	CPU RSVD MB CLK#2	P32	RSVD MB CLK L3	FREE	B22	FREE
7413	TPC28T	1	CPU RSVD MB CLK#1	P34	RSVD MB CLK L0	FREE	H16	FREE
7414	TPC28T	1	CPU RSVD MB CLK#0	P36	RSVD MB CLK L0	FREE	H14	FREE

SOCKET#88



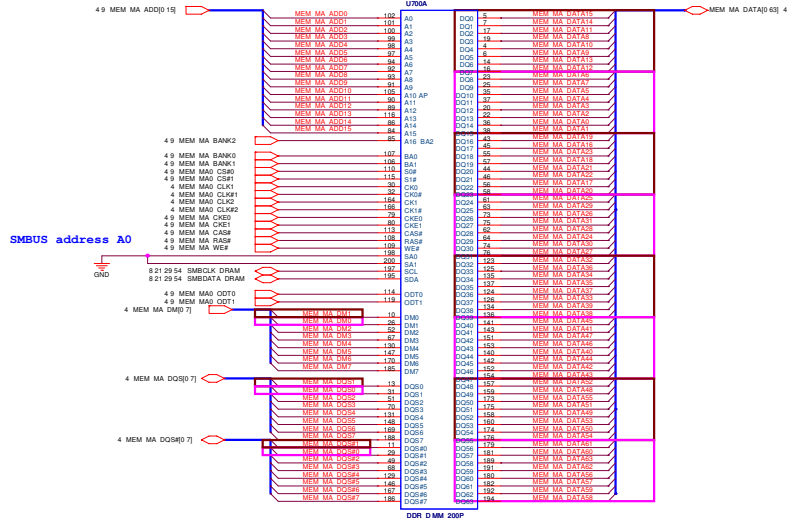
ASUS **Intel®** **AMD S1 CPU-DDR2**
 SOLVING COMPUTERS AND MORE
 828 Project Name: **Spark_Leo** Engineer:
 Date: **08-13-11** Rev: **1.0**
 Drawn: **FJK** Sheet: **4** of **51**

« Kennedy_Zhang »

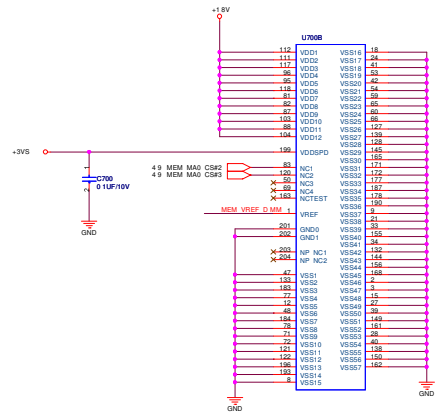
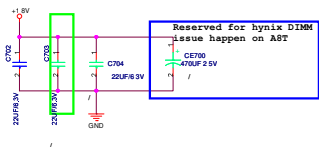


<< Kennedy_Zhang >>

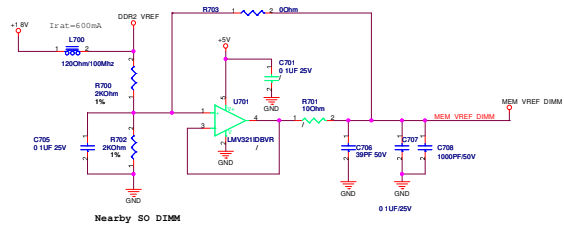
REV . TYPE



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main source is 12G025122006 (TYCO)



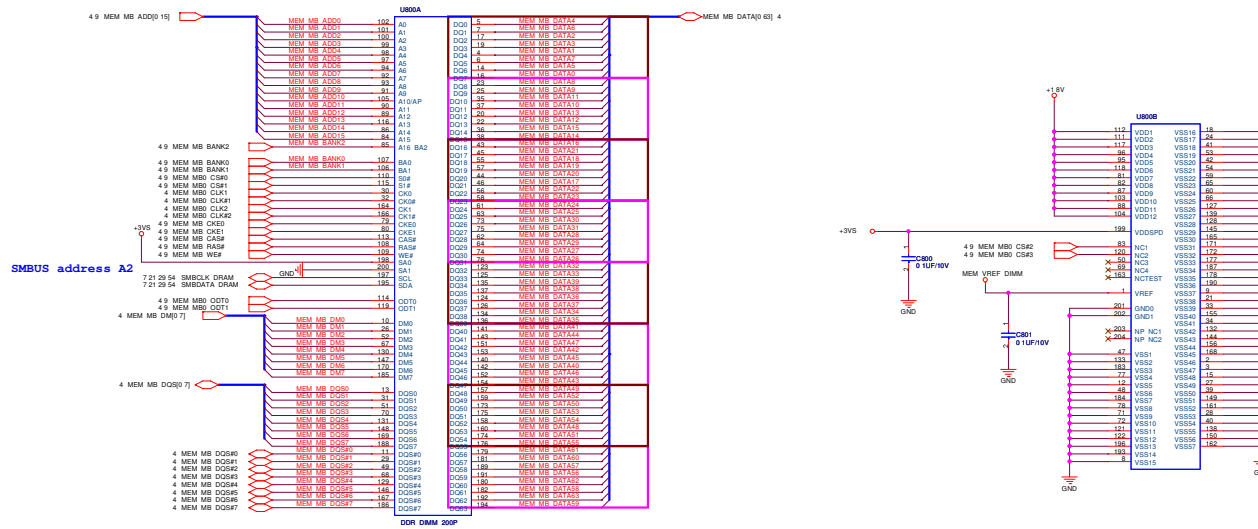
DOR DIMM 200P



Nearby SO DIMM

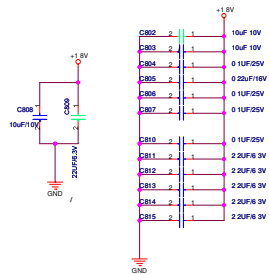
« Kennedy_Zhang »

STD. TYPE

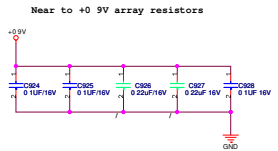
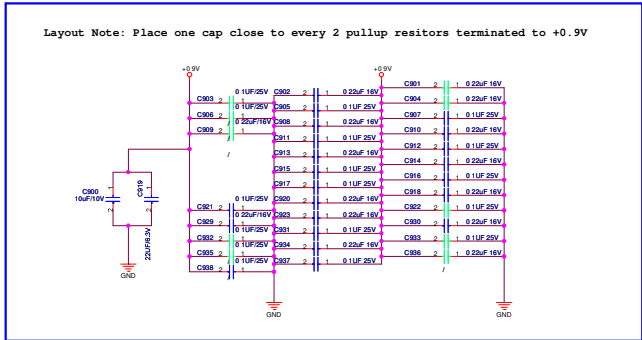
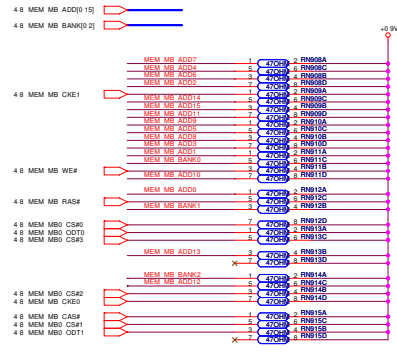
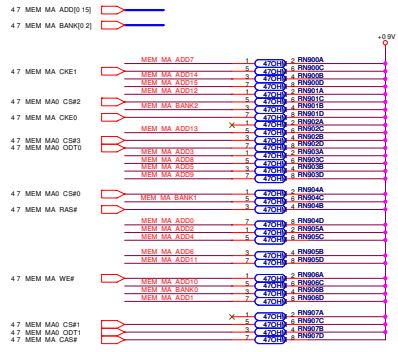


Second source is 12G025122000 (FOXCONN)
Main source is 12G025122007 (TYCO)

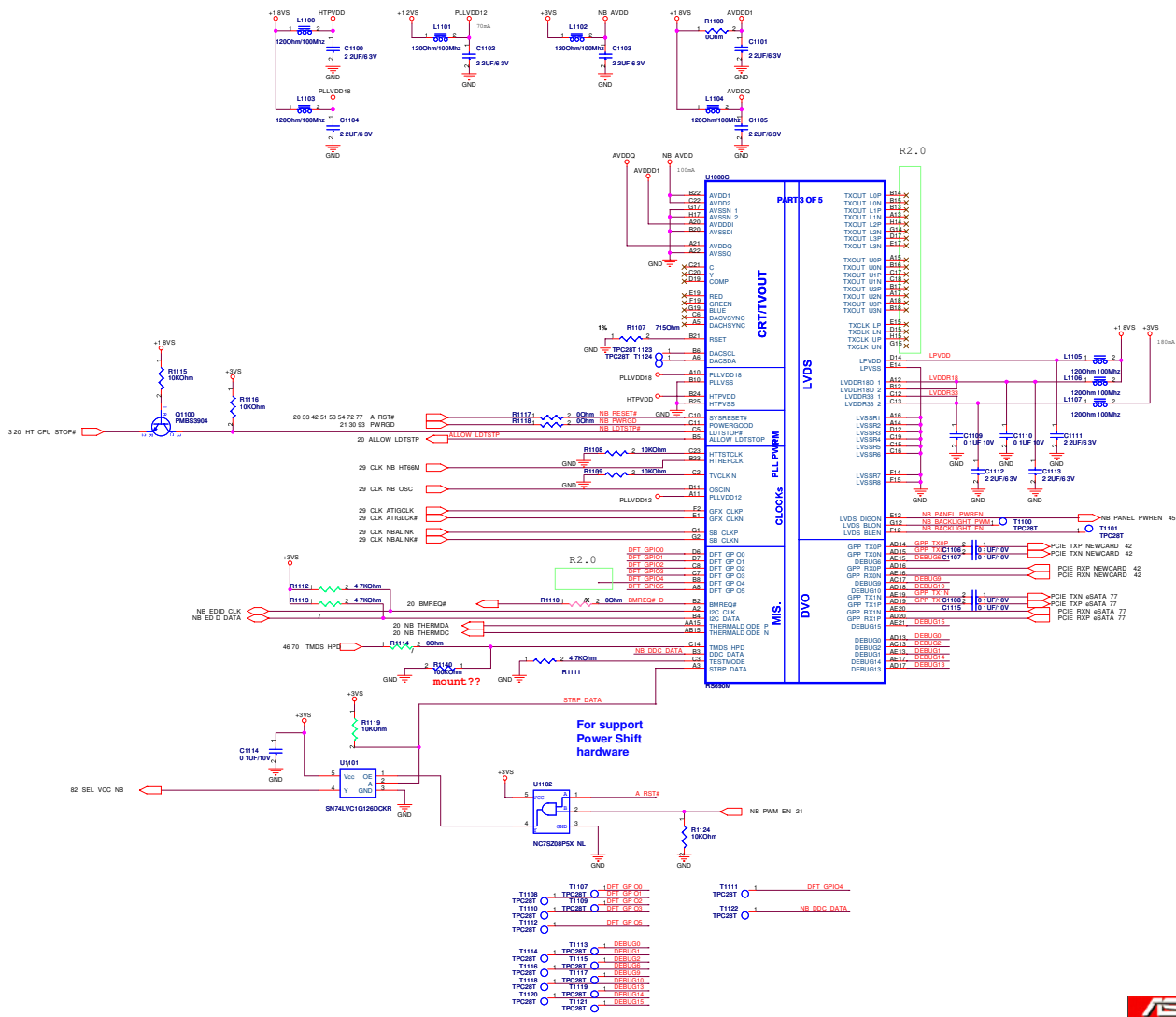
DDR DIMM 20P



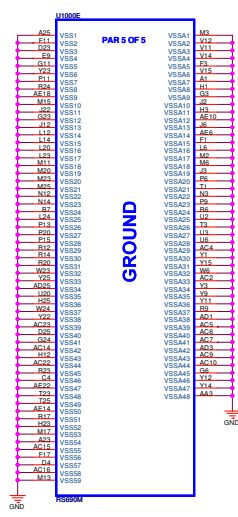
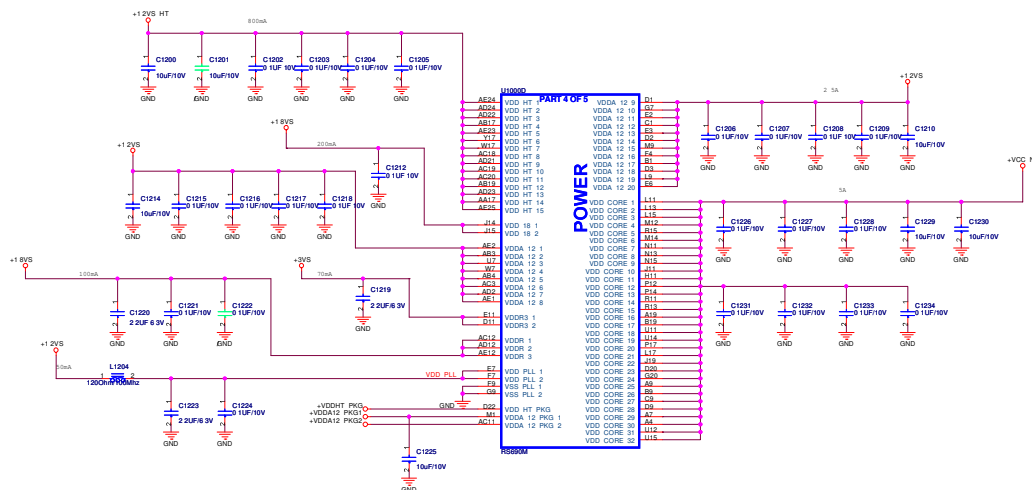
« Kennedy_Zhang »



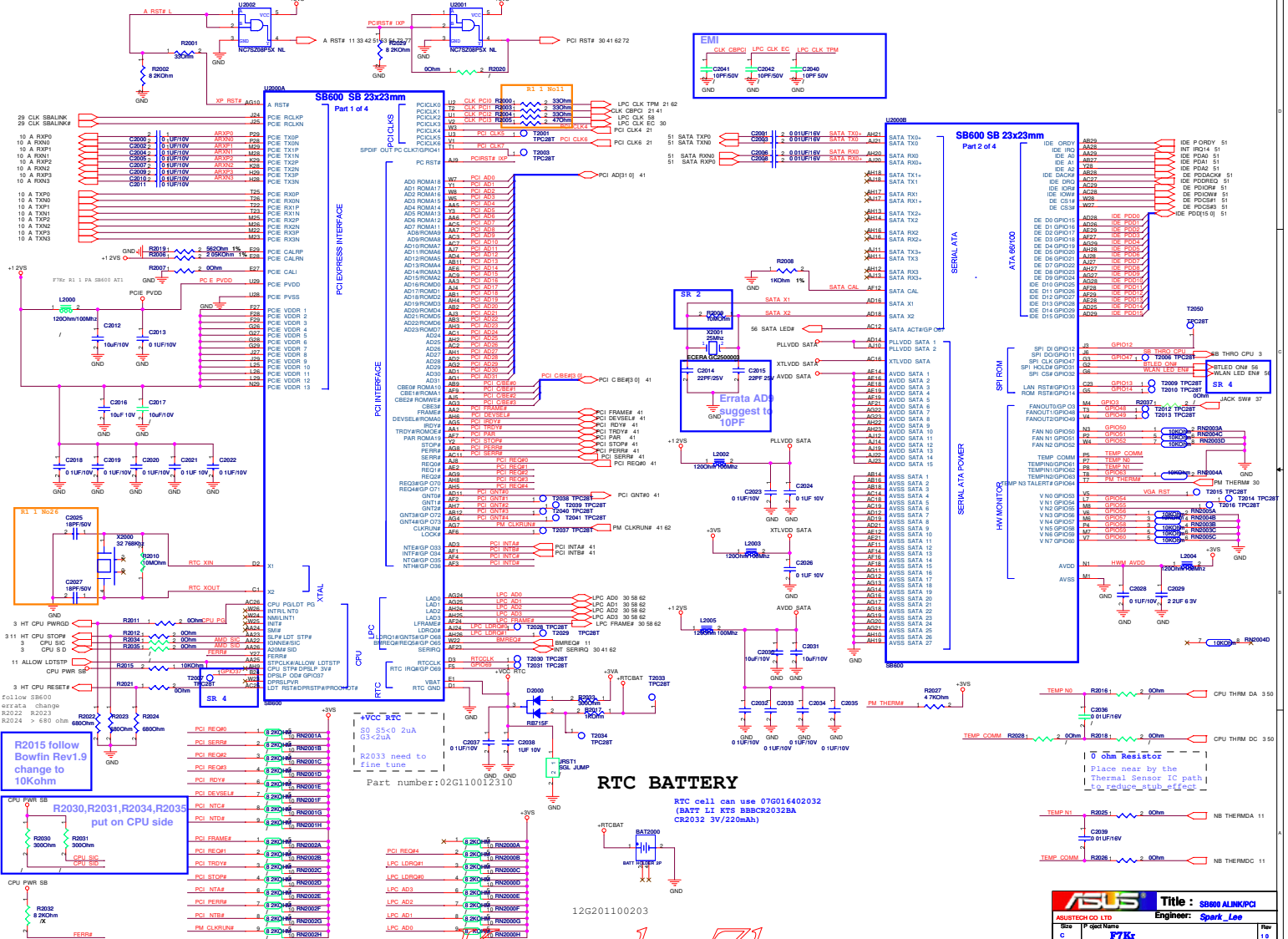
« Kennedy_Zhang »



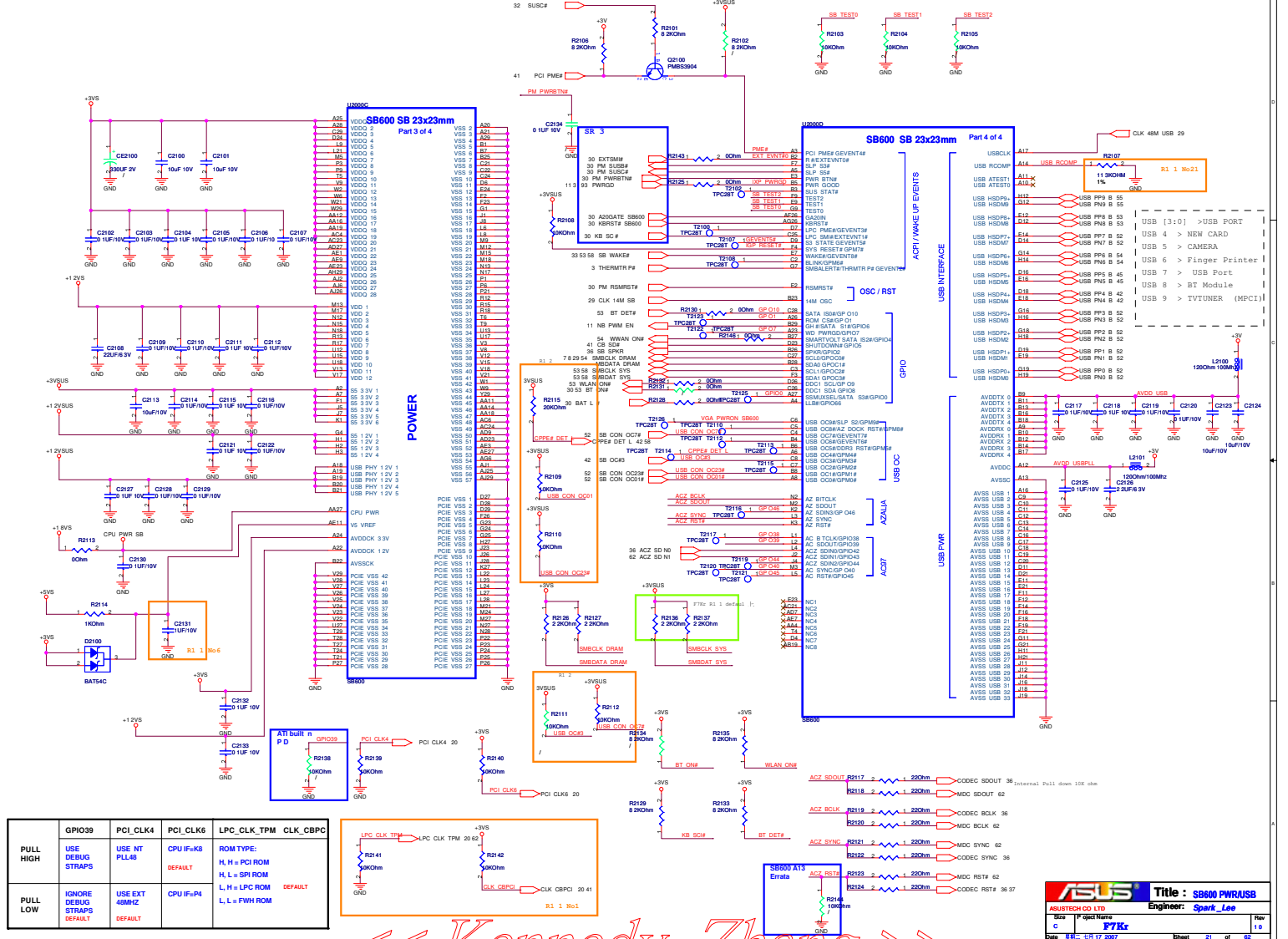
« Kennedy_Zhang »



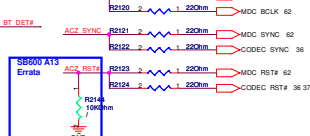
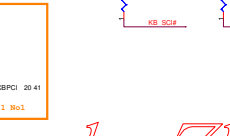
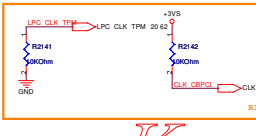
« Kennedy_Zhang »



Kennedy_Zhang



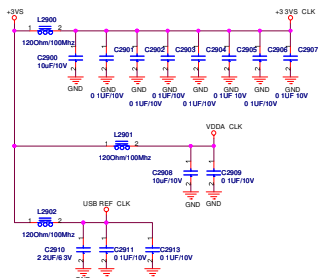
	GPIO39	PCI_CLK4	PCI_CLK6	LPC_CLK_TPM	CLK_CBPC
PULL HIGH	USE DEBUG STRAPS	USE NT PULL	CPU IF:K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, L = LPC ROM L, L = FW ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT 48MHZ DEFAULT	CPU IF:P4 DEFAULT		



ASUSTeCH CO LTD
Title: SB600 PWR/USB
Engineer: Spark_Lee

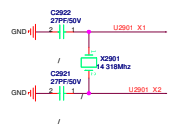
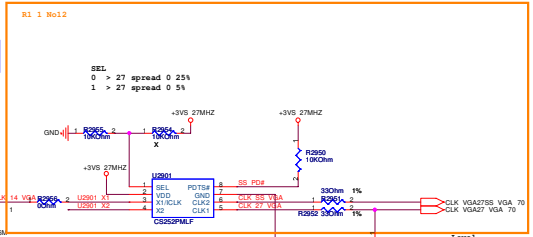
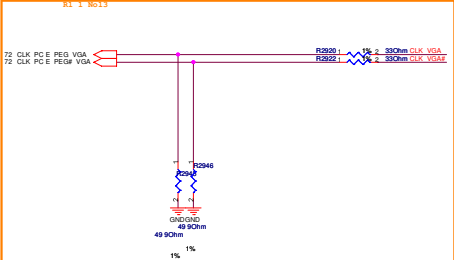
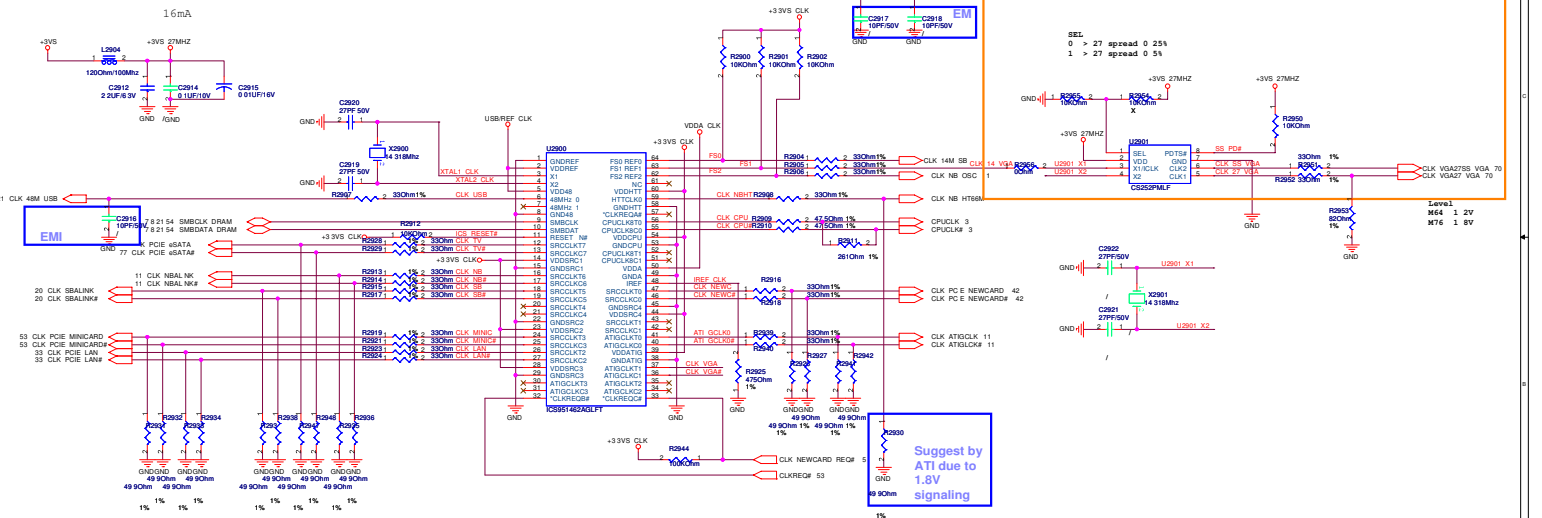
Ver	1.0	Rev	1.0
Date	2007-07-17	Sheet	11 of 16

Kennedy_Zhang



EXT CLK FREQUENCY SELECT TABLE (MHZ)

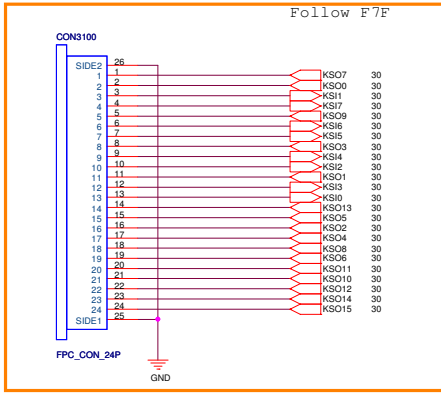
FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	HI Z	100 00	HI Z	HI Z	48 00	Reserved
0	0	1	X	100 00	X/3	X/6	48 00	Reserved
0	1	0	180 00	100 00	60 00	30 00	48 00	Reserved
0	1	1	220 00	100 00	36 56	73 12	48 00	Reserved
1	0	0	100 00	100 00	66 66	33 33	48 00	Reserved
1	0	1	133 33	100 00	66 66	33 33	48 00	Reserved
1	1	1	200 00	100 00	66 66	33 33	48 00	Normal ATHLON64 operation



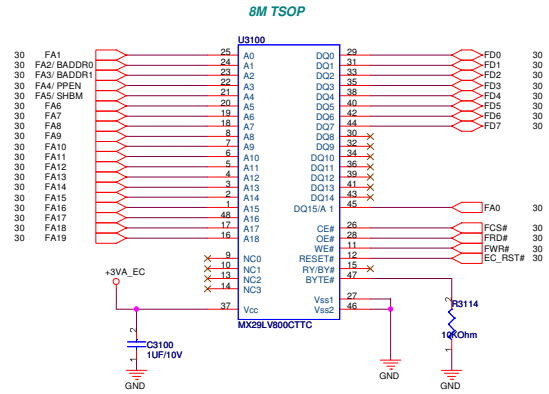
« Kennedy_Zhang »

KBC connector

Follow F7F

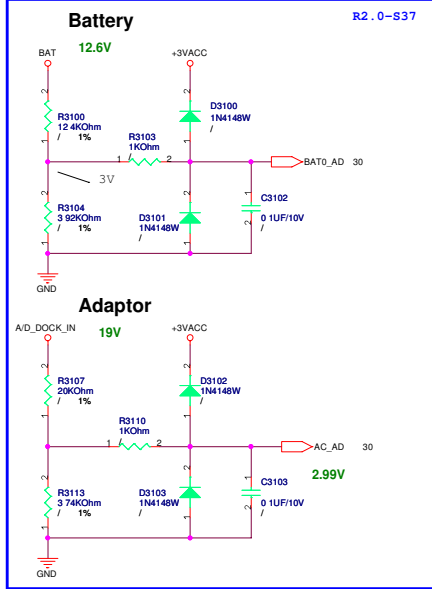


12G182402405

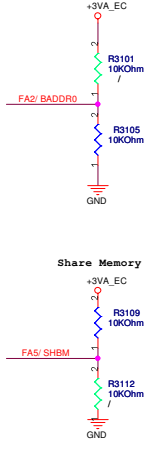


EC ADC

R2.0-S37



EC Hardware Strap



PNPCFG base address set by SWCBAR/SWCBALR

Share Memory

SHEM
No pull up:
disable shared memory with host BIOS
Ext 10K up:
enable shared memory with host BIOS

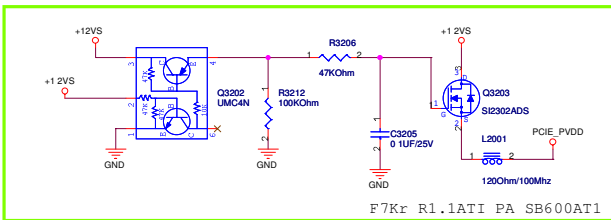
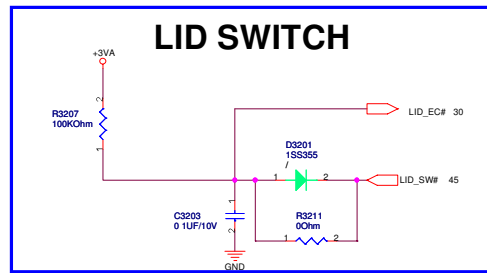
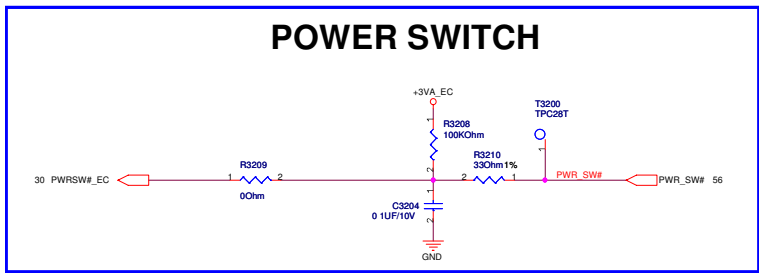
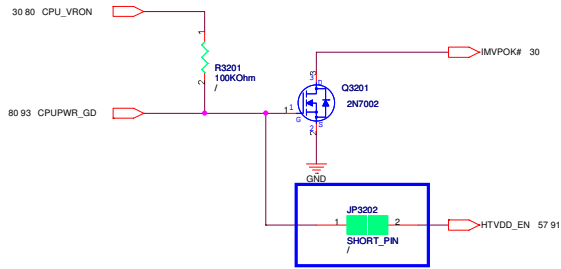
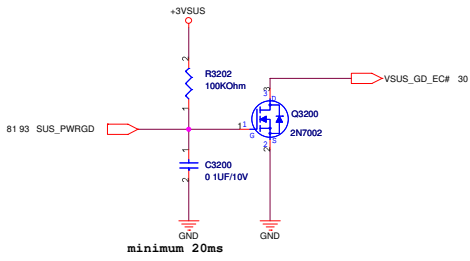
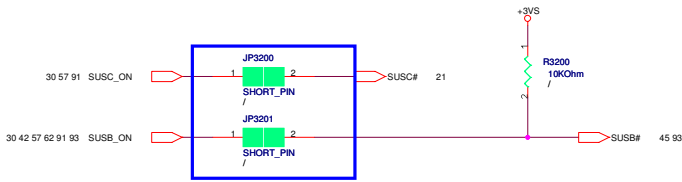
strap value sampled after VSTBY power up reset

BADDR[1:0]
No pull up:
The register pair to access PNPCFG is 002Eh and 002Fh.
Ext 10K up on BADDR0:
The register pair to access PNPCFG is 004Eh and 004Fh.
Ext 10K up on BADDR1:
The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBARR.

PPEN
No pull up:
Normal
Ext 10K up:
KBS interface pins are switched to parallel port interface for in-system programming.

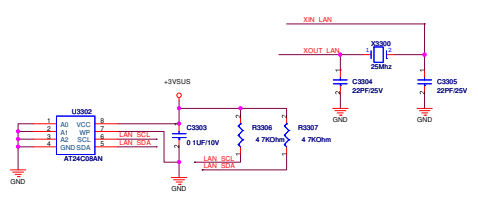
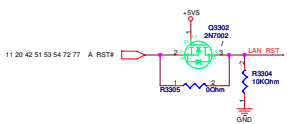
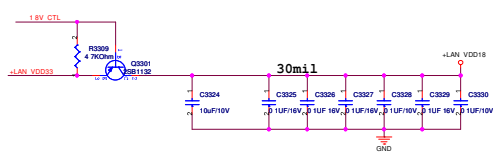
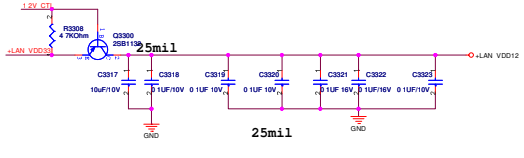
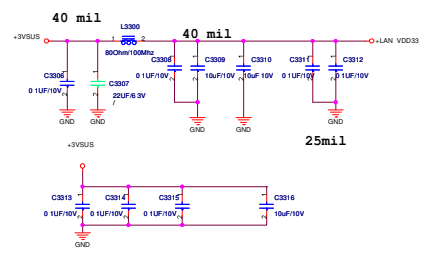
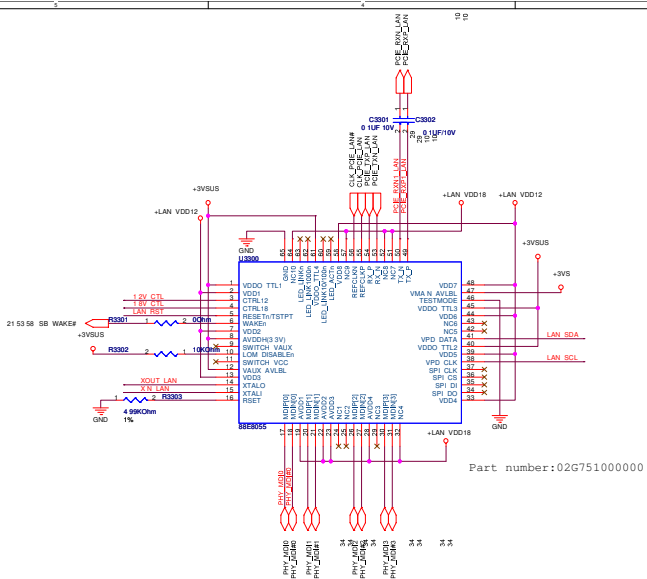
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ASUSTeK COMPUTER INC. NBS		Engineer: Spark_Lee	
Size	Project Name		Rev
Custom	FTK		1.0
Date: 08-11-17 2007		Sheet	31 of 62

« Kennedy_Zhang »



ASUS		Title : POWER-ON SEQUENCE	
ASUSTek COMPUTER INC		Engineer: <i>Spark_Lee</i>	
Site	Project Name	Rev	1.0
Custom	F7Kr		
Date: 03/11/2007		Sheet	32 of 62

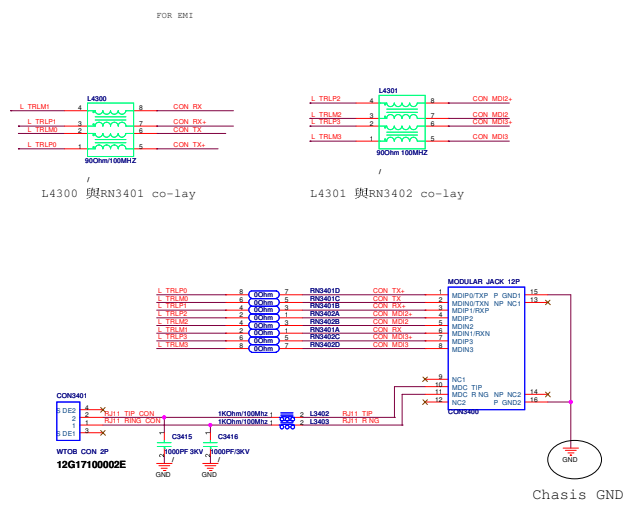
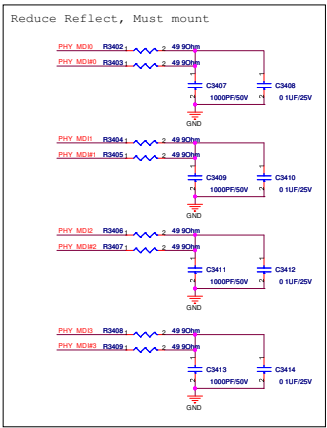
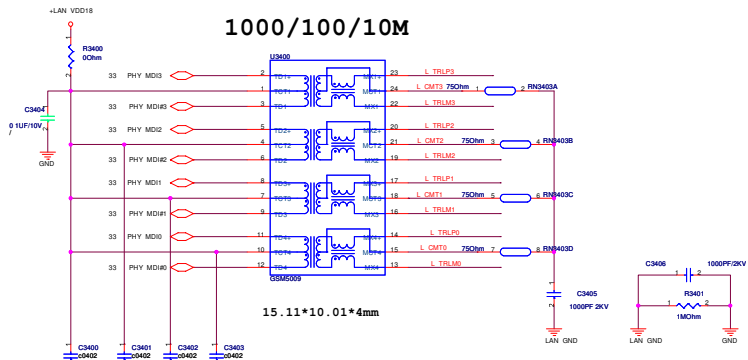
« Kennedy_Zhang »



ASUS		Title : LAN RTL8111B	
ASUSTEK COMPUTER INC.		Engineer: Spark_Lee	
Doc	P: gpc/hzhs	Rev	1.0
C	P7Kc		
Doc	118 - 03-17-2007	Sheet	33 of 32

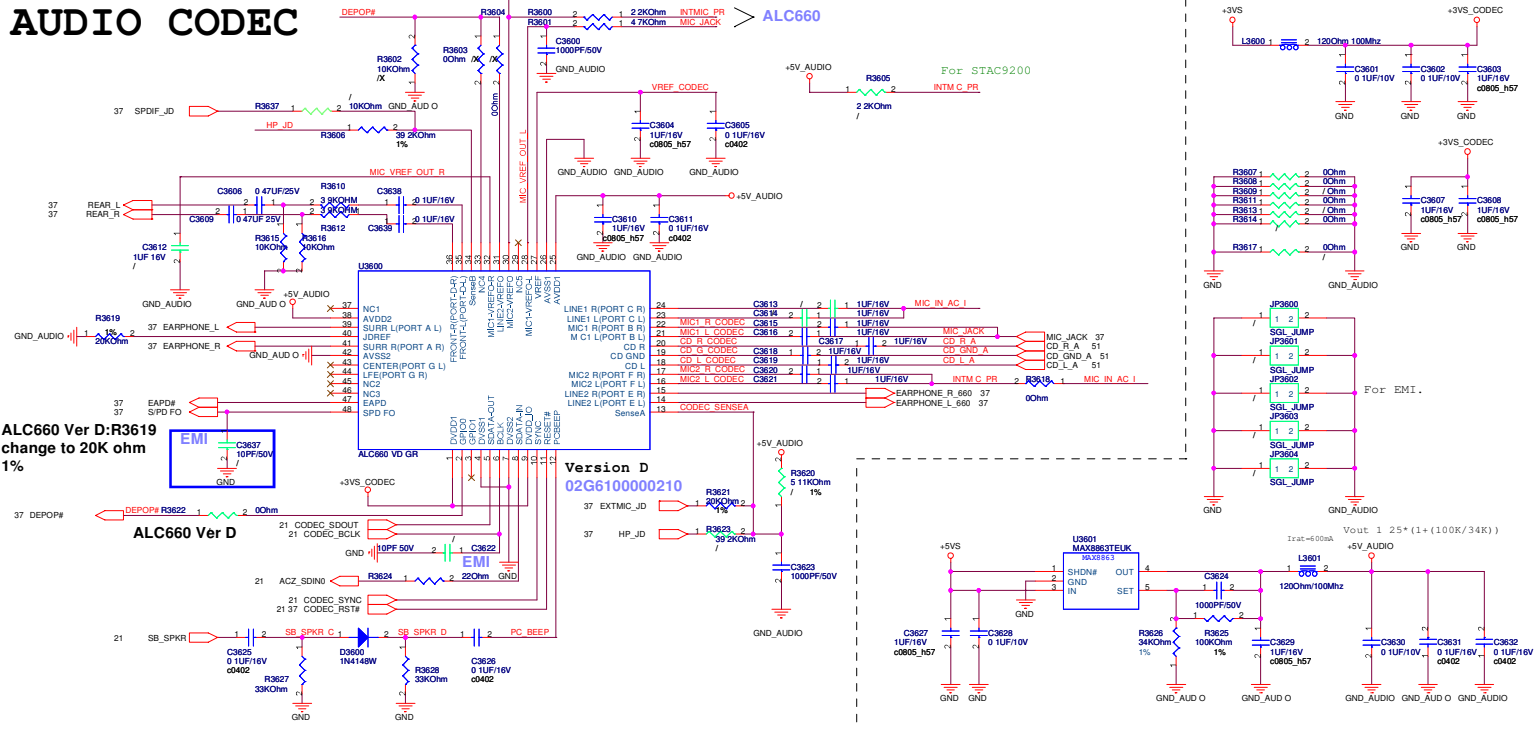
<< Kennedy_Zhang >>

LAN PORT



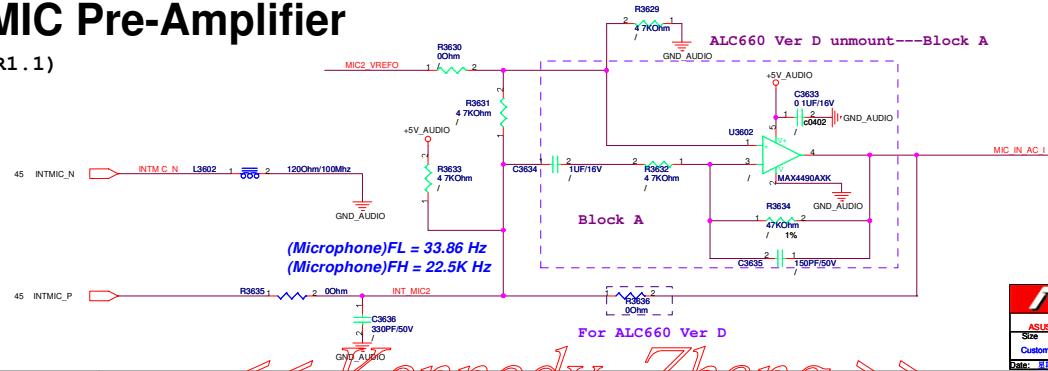
« Kennedy_Zhang »

AUDIO CODEC



Internal MIC Pre-Amplifier

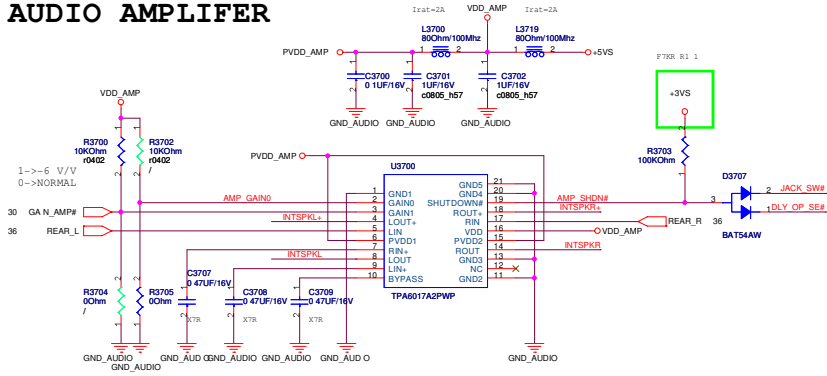
(Follow F2J R1.1)



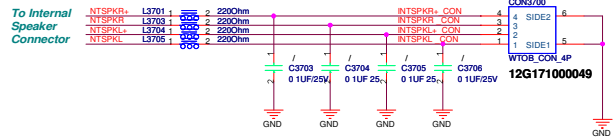
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ASUSTeK COMPUTER INC		Engineer: Spark_Lee	
Size	Project Name	Date	Rev
Custom	F7Kz	8/8 14:17:2007	1.0
		Sheet	36 of 82

« Kennedy_Zhang »

AUDIO AMPLIFIER

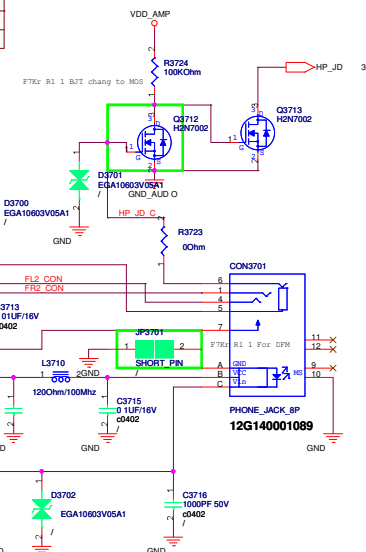


SPEAKER

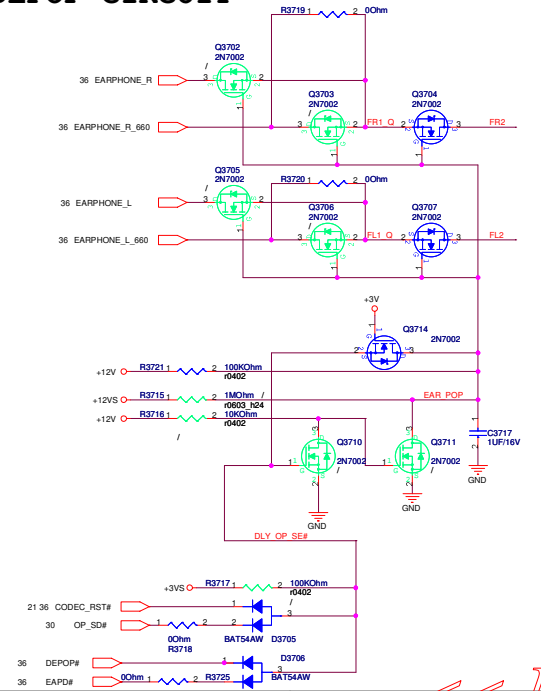


HeadPhone&SPDIF

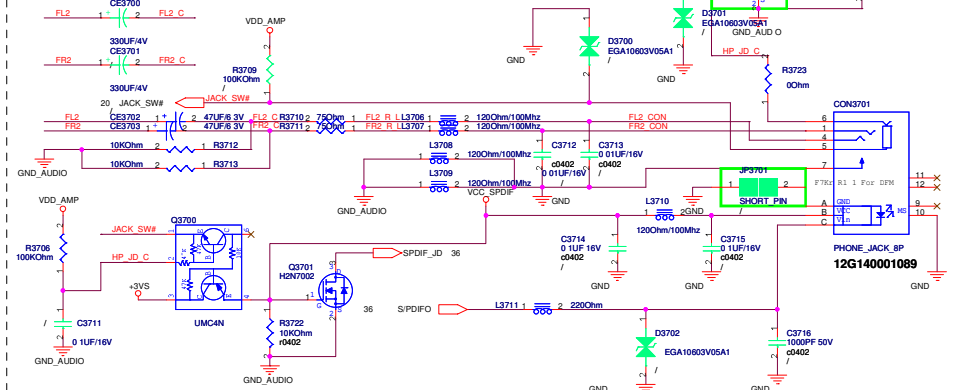
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HP_JD	L	H	H
JACK_SW#	L	L	H



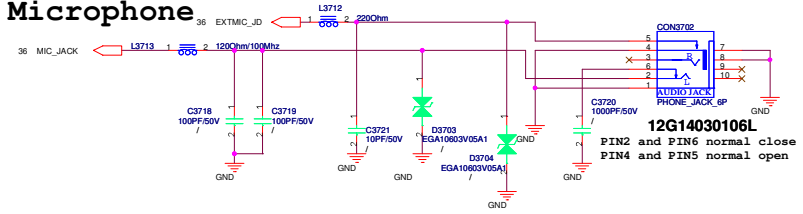
DEPOP CIRCUIT



Co-Layout with CE3702/CE3703

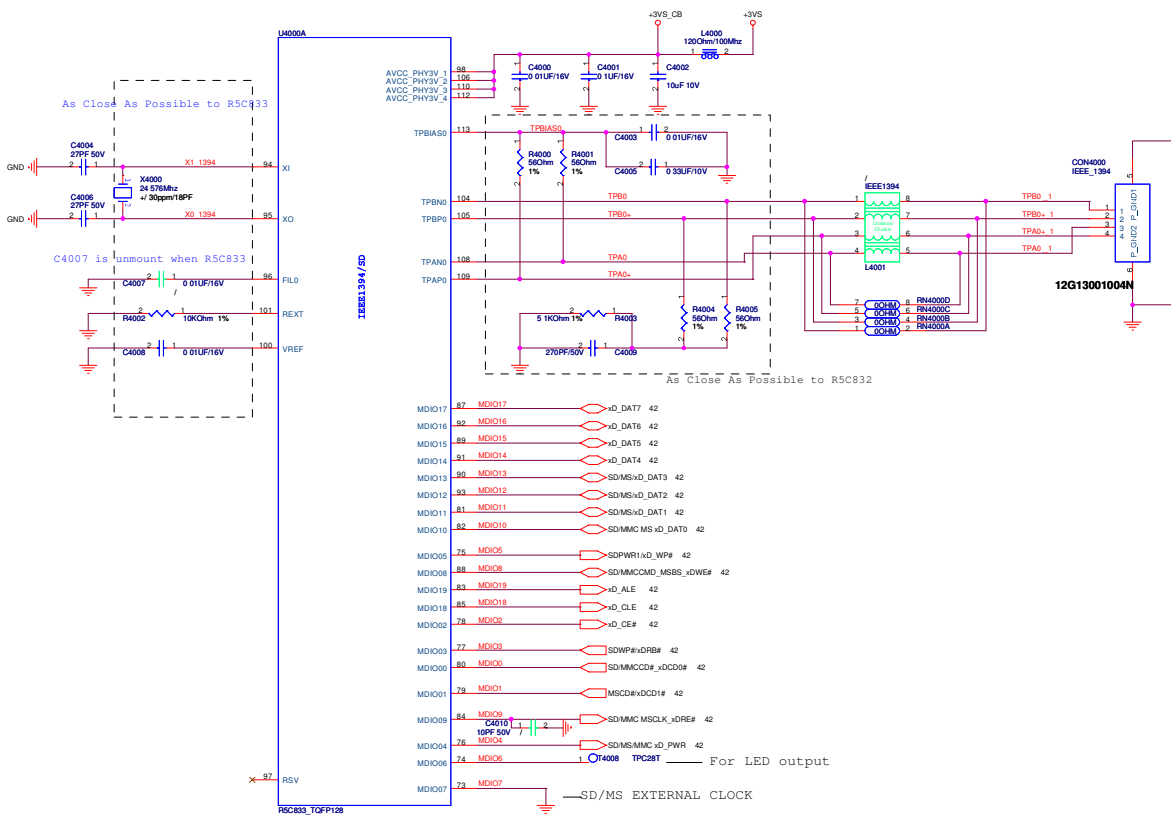


External Microphone



ASUS Title : AUDIO AMP & JACK
 ASUSTeK COMPUTER INC Engineer: Spark_Lee
 Site: Project Name: FTKr
 Date: 11/17/2007 Sheet: 37 of 82

« Kennedy_Zhang »



MDIO02	> xDCE#
MDIO05	> xD Power Control 1 / xDNP
MDIO04	> xD/MS/SD LED Control
MDIO14	> xD Data
MDIO15	> xD Data
MDIO16	> xD Data
MDIO17	> xD Data
MDIO18	> xD CLE
MDIO19	> xD ALE

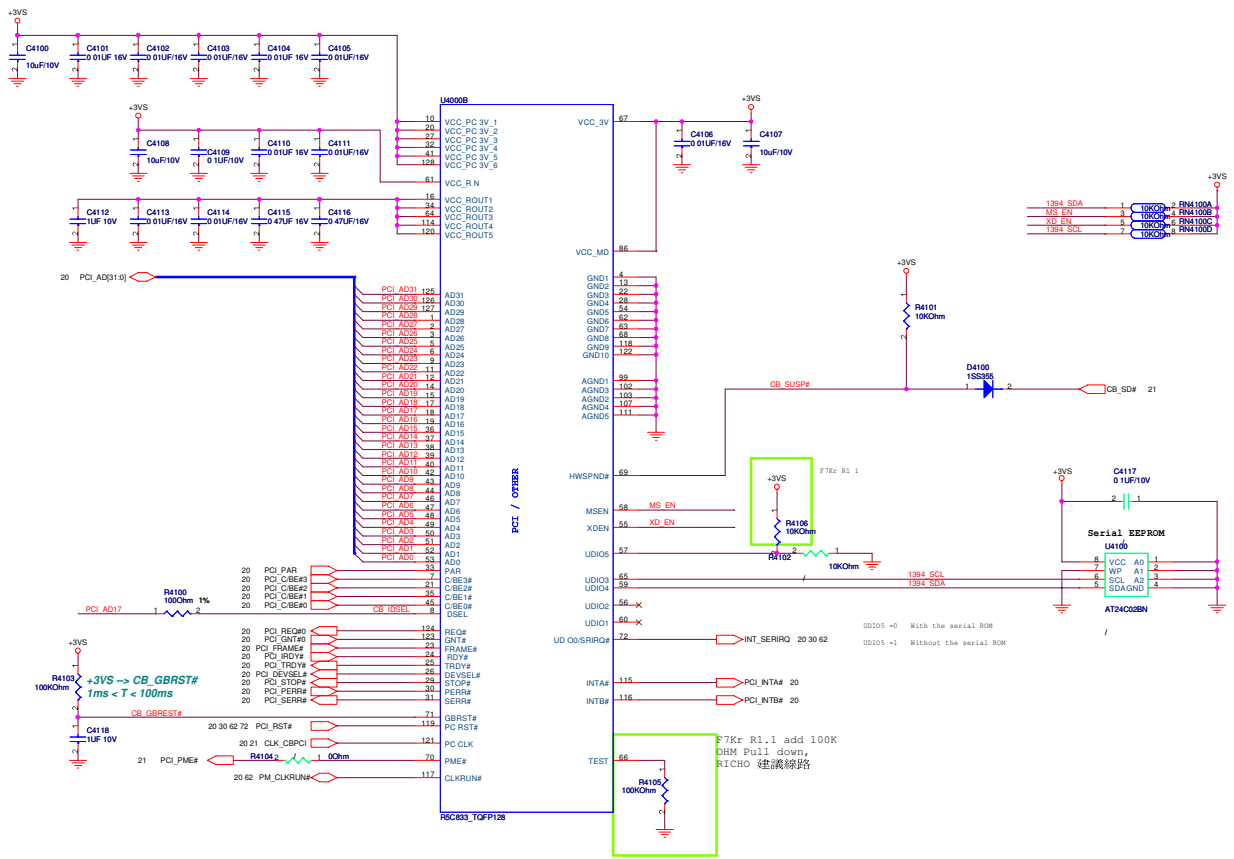
MDIO01	> MS Card Detect
MDIO03	> SD Write Protect
MDIO04	> SD Card Power0 Control/MS Power Control
MDIO07	> SD External Clock/MS External Clock
MDIO09	> SD Command/MS Bus State
MDIO08	> SD Clock/MS Clock
MDIO10	> SD Data 0/MS Data 0
MDIO11	> SD Data 1/MS Data 1
MDIO12	> SD Data 2/MS Data 2
MDIO13	> SD Data 3/MS Data 3

MDIO00	> SD Card Detect
MDIO01	> MS Card Detect
MDIO03	> SD Write Protect
MDIO04	> SD Card Power0 Control/MS Power Control
MDIO08	> SD Command/MS Bus State
MDIO09	> SD Clock/MS Clock
MDIO10	> SD Data 0/MS Data 0
MDIO11	> SD Data 1/MS Data 1
MDIO12	> SD Data 2/MS Data 2
MDIO13	> SD Data 3/MS Data 3

ASUS Title: RICH 5C832-CARD&1394
 Engineer: Spark_Lee

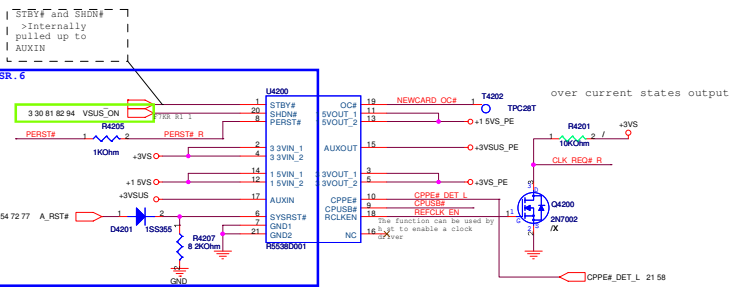
Size	Project Name	Rev
Custom	F7K7	1.0
Date: 01/12/2007	Sheet	20 of 25

<< Kennedy_Zhang >>

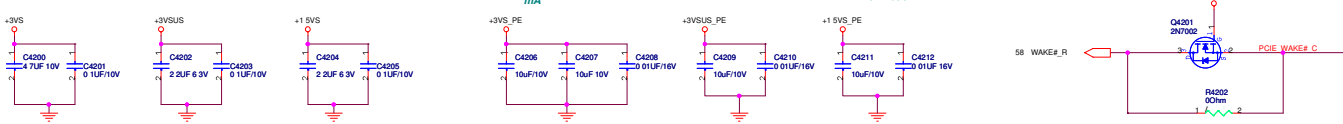
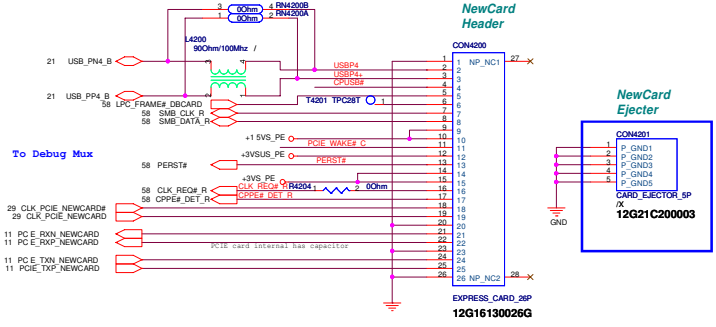


<< Kennedy_Zhang >>

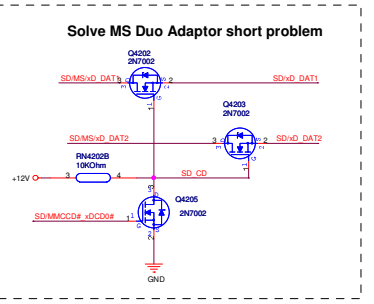
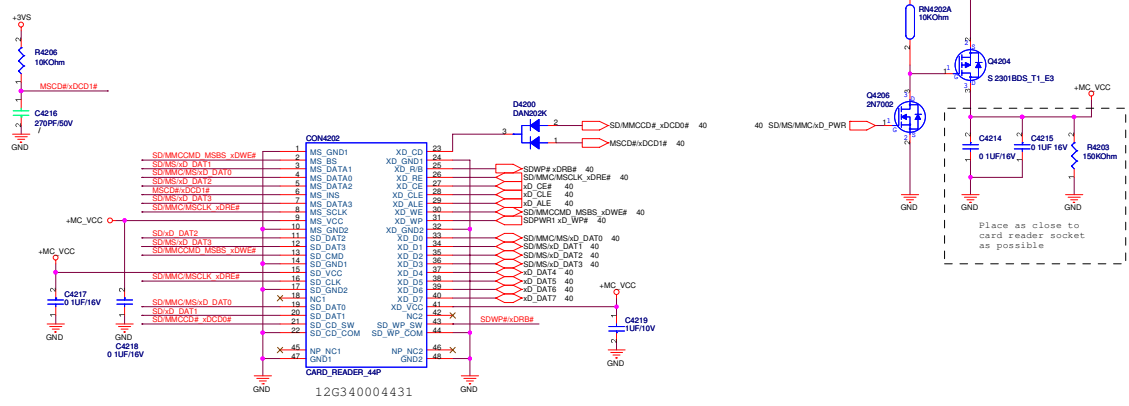
NEW CARD SOCKET



!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V



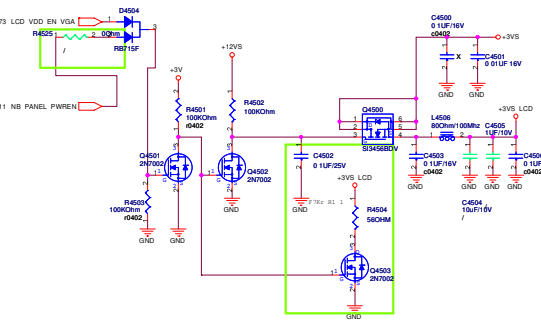
4 IN 1 CARD READER SOCKET



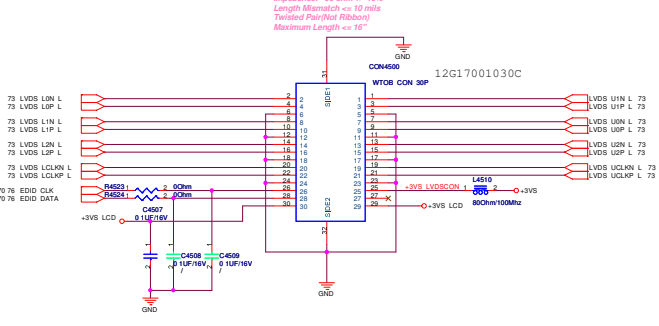
ASUS Title : Express Card & Card Reader
 ASUSTek COMPUTER INC. NBS Engineer: Spark_Lee
 Size Project Name Rev
 Custom FTK
 Date: 10/11/2007 Sheet 42 of 48

<< Kennedy_Zhang >>

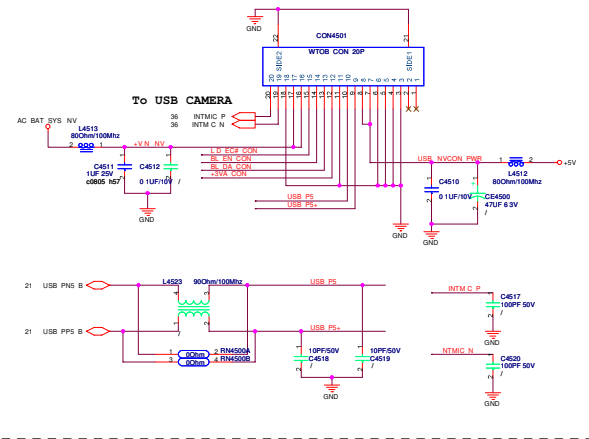
LCD Power



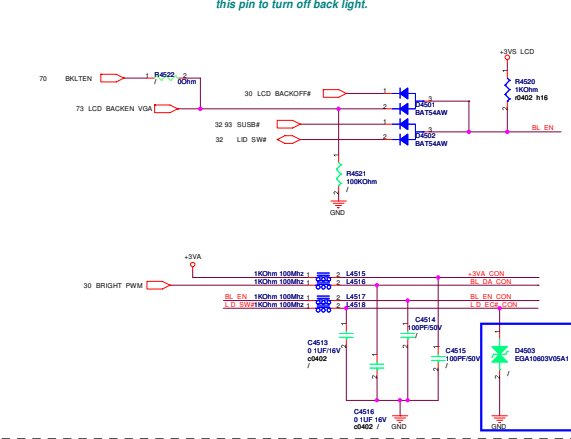
LCD LVDS Interface



INVERTER Interface



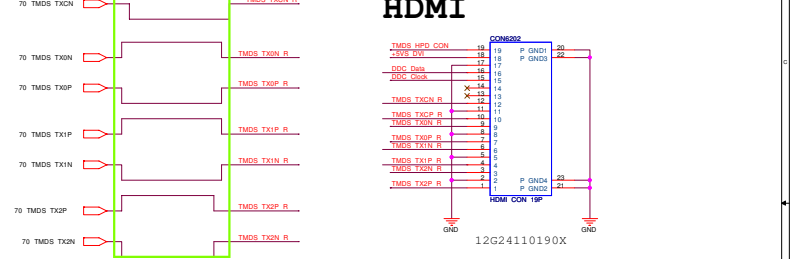
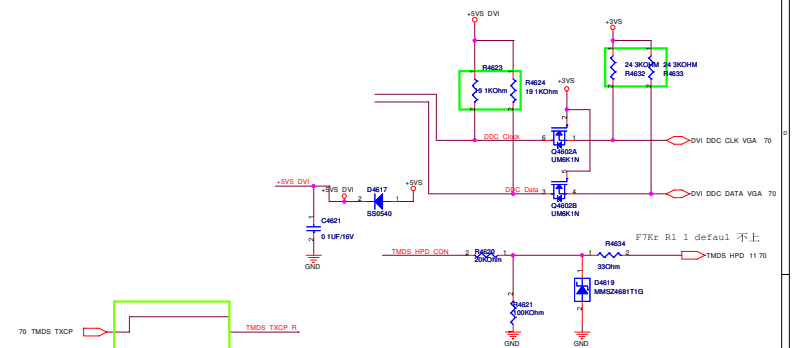
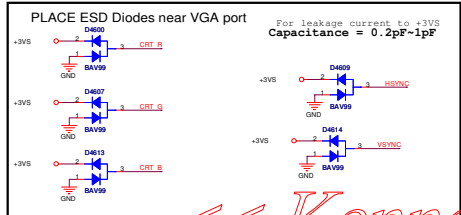
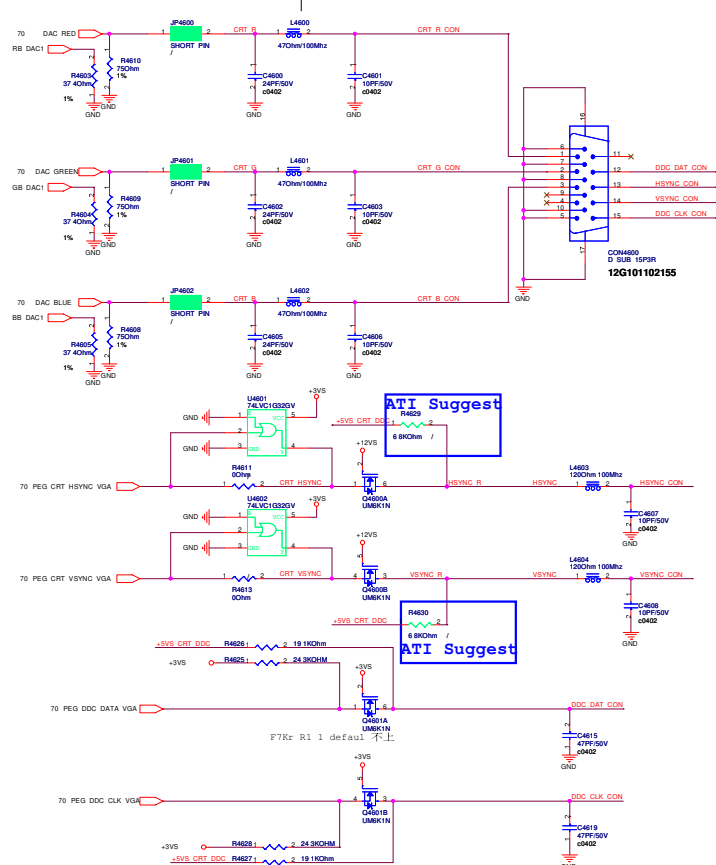
Backlight Enable



« Kennedy_Zhang »

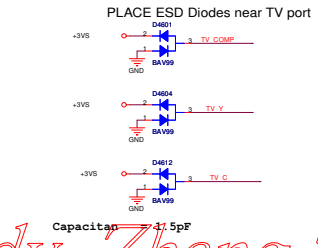
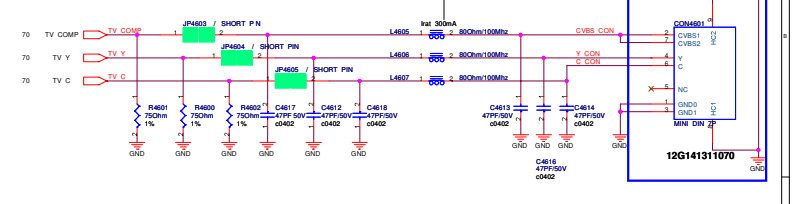
VGA OUT

Reference Schematics L=47nH



TV OUT

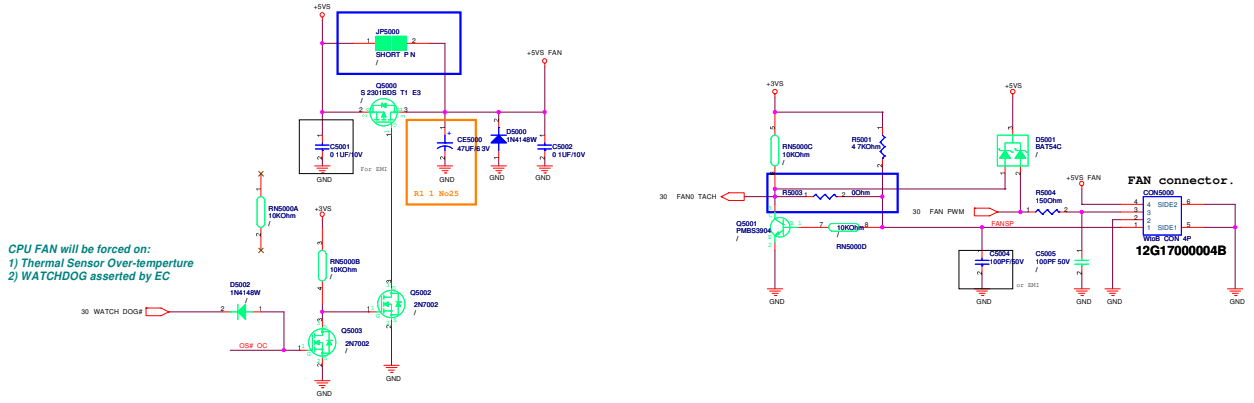
Reference Schematics L=470nH



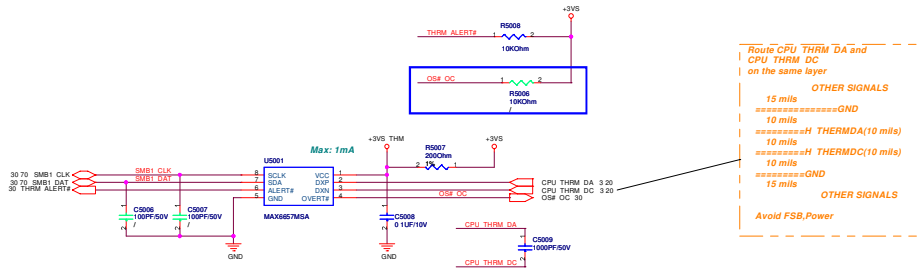
ASUS		Title : TV&CRT CONNECTOR	
Rev	0	Enginer	Spark_Lee
Date	11-17-2007	Sheet	45 of 45

« Kennedy_Zhang »

DC FAN control



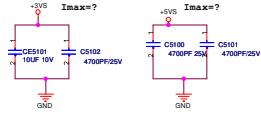
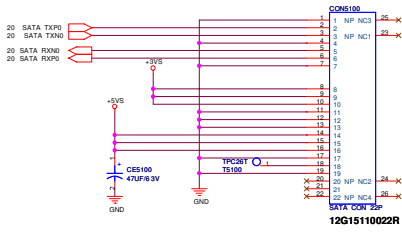
Thermal Sensor



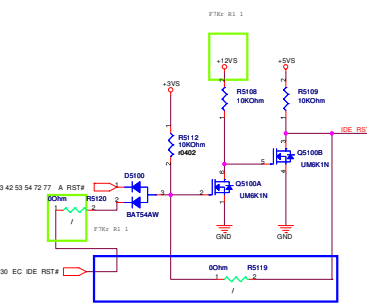
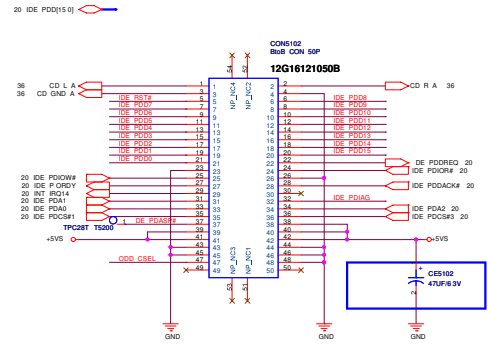
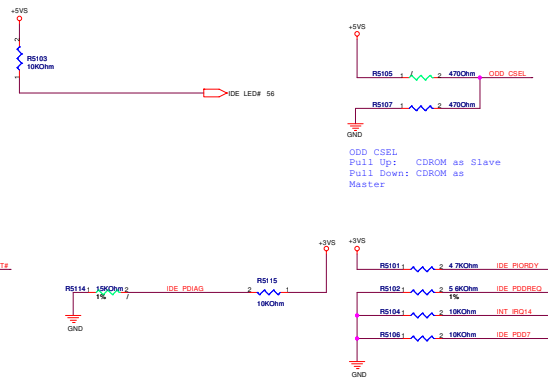
<< Kennedy_Zhang >>

		Title : THERMAL & FAN CONTROL	
ASUSTek COMPUTER INC. HKS		Engineer: Spark_Lee	
Doc No:	Doc Name:	Rev:	1.0
Date: 11-18-17 20:07		Sheet: 50 of 55	

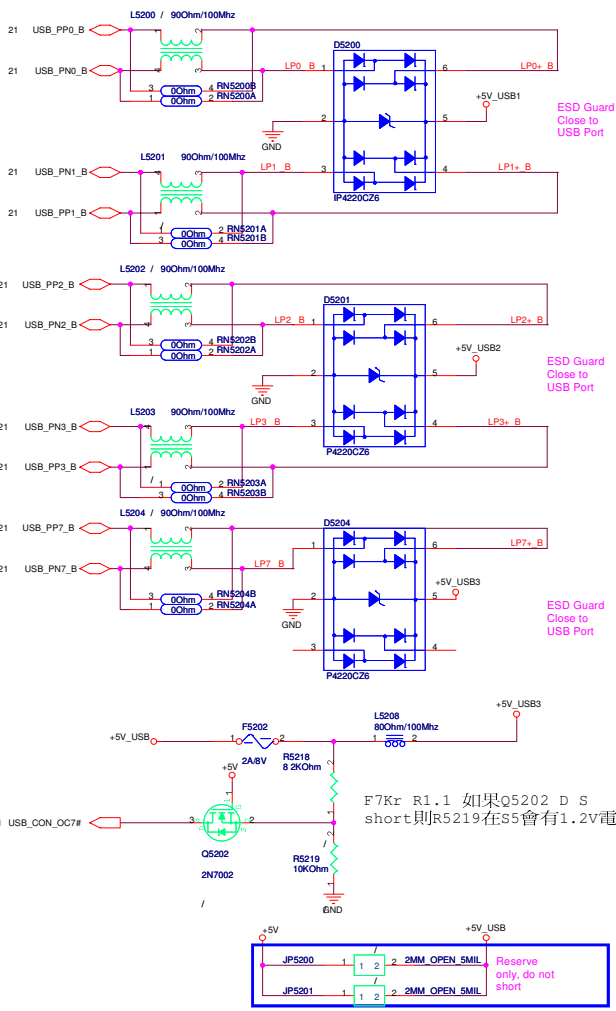
SATA_HDD(Default)



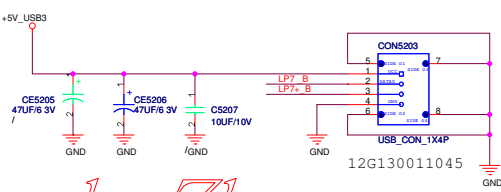
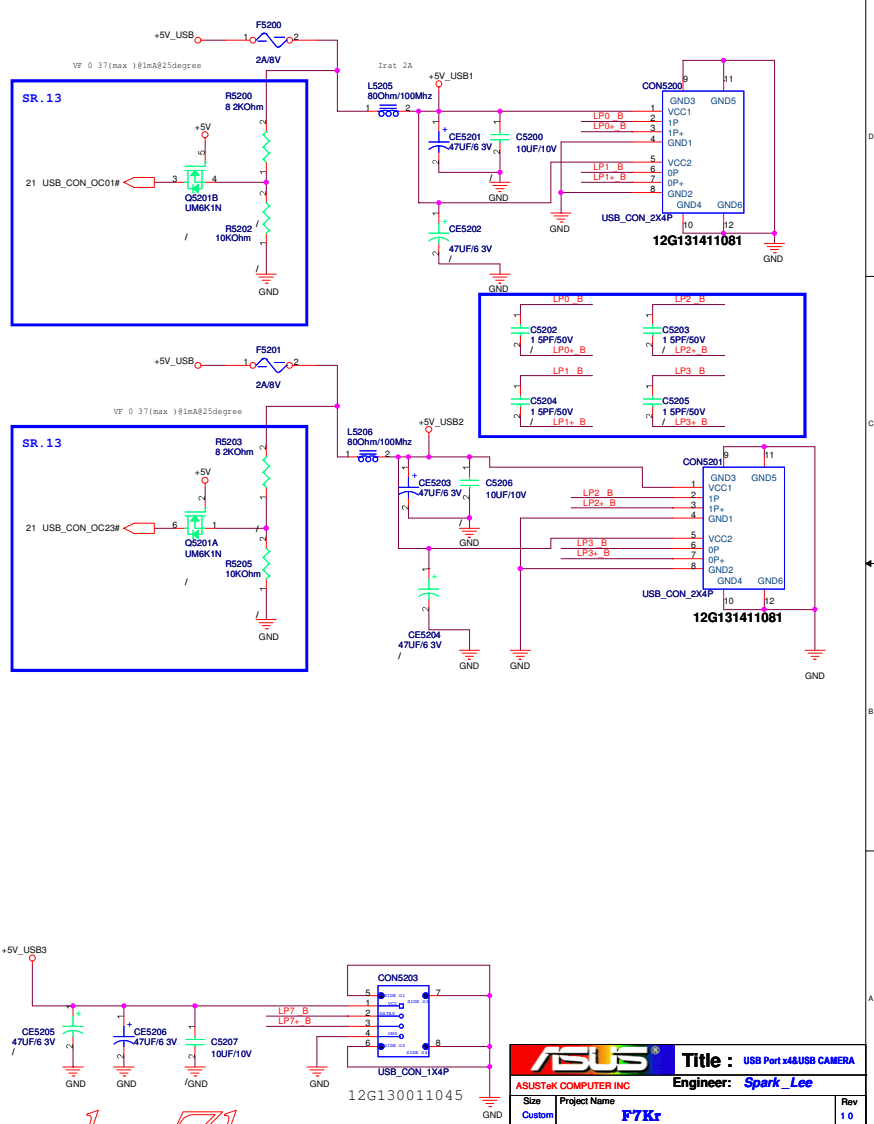
CD-ROM



« Kennedy_Zhang »



F7Kr R1.1 如果Q5202 D S short則R5219在S5會有1.2V電



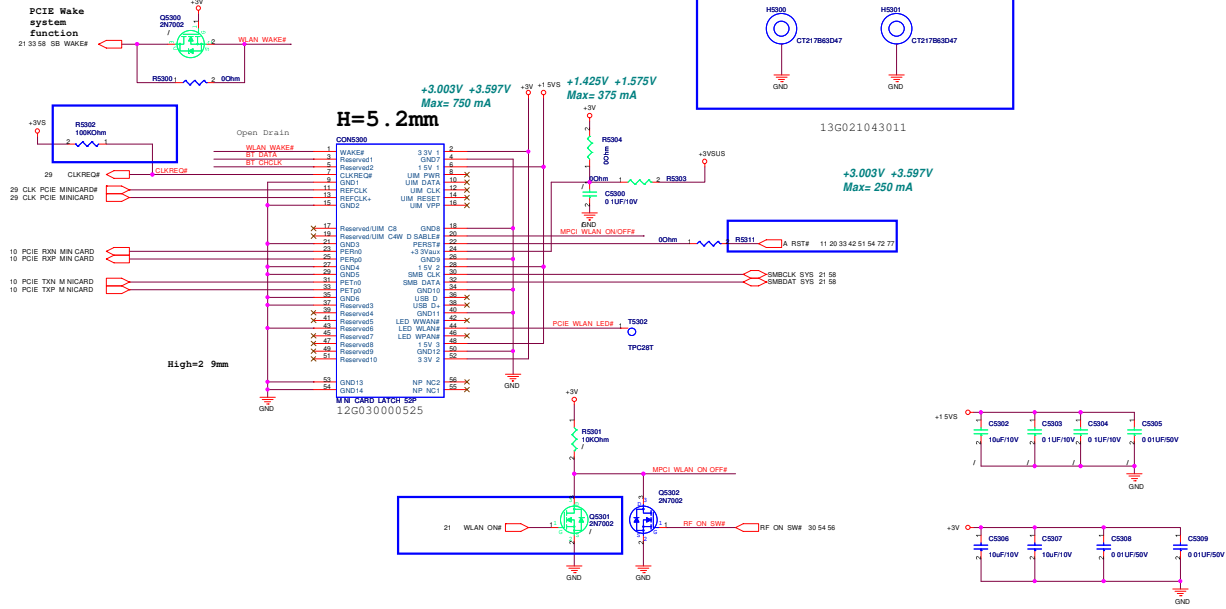
ASUS		Title : USB Port x4&USB CAMERA	
ASUSTek COMPUTER INC		Engineer: Spark_Lee	
Site	Project Name	Date	Rev
Custom	F7Kr	11/17/2007	1.0
Date: 11/17/2007		Sheet	52 of 62

<< Kennedy_Zhang >>

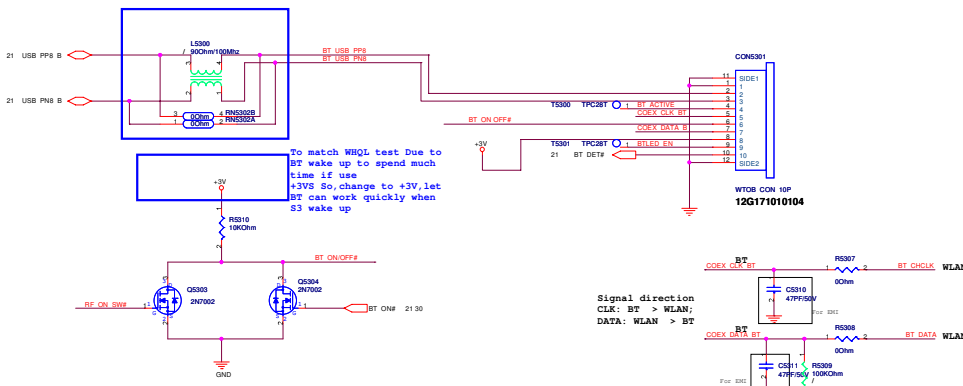
WLAN

MINI PCIEX CONNECTOR

Instead of Mini-PCIEX latch connector. For cost down.



BLUETOOTH CONNECTOR

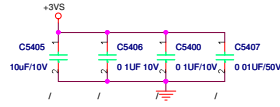
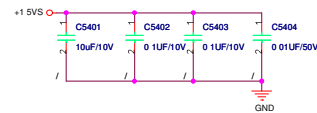


<< Kennedy_Zhang >>

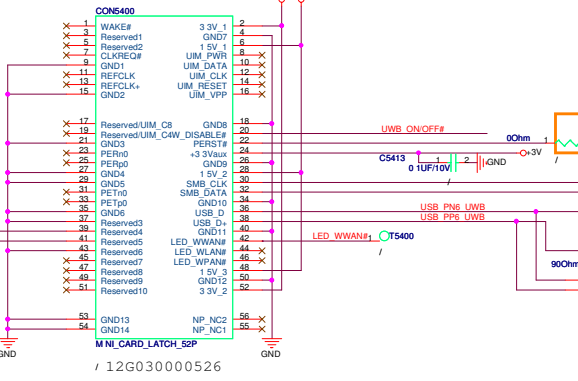
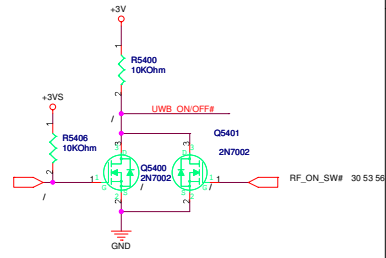
UWB

H=4.0mm

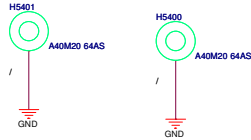
+3.003V~+3.597V
Peak = 2.75A,
Notch at 2.5V-1A, 575V
Max= 375 mA



+3.003V~+3.597V
Max= 250 mA

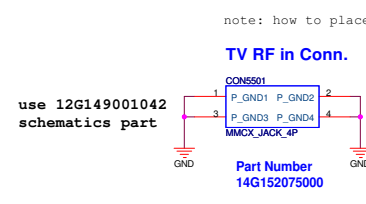
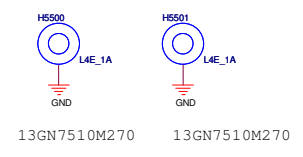
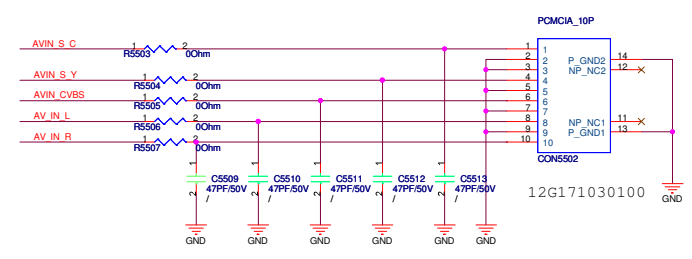
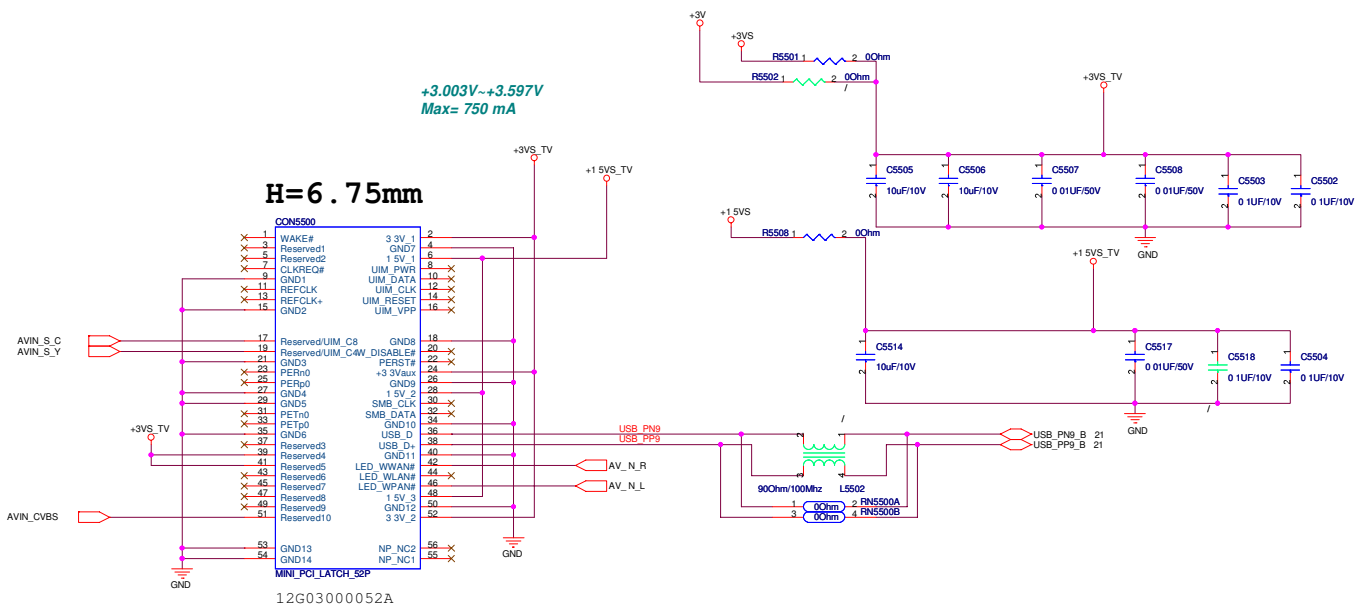


Height issue.
change to
220uF/6.3V



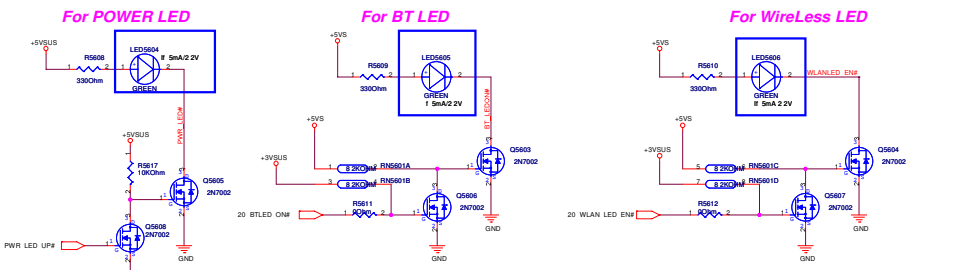
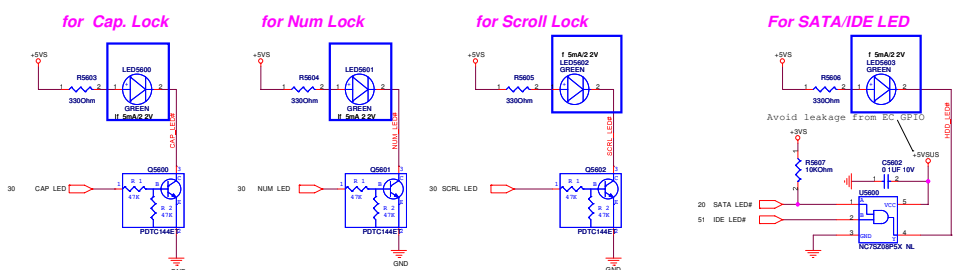
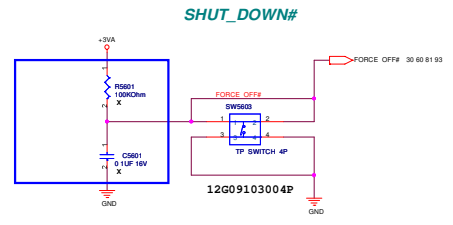
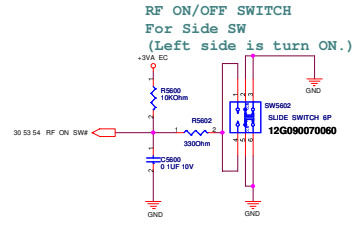
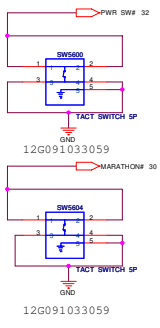
ASUS		Title : MINI Card-Windigo	
ASUSTek Computer INC		Engineer: Spark_Lee	
Size	Project Name		Rev
B	FTKr		1.0
Date: 11/17/2007		Sheet 54	of 62

<< Kennedy_Zhang >>

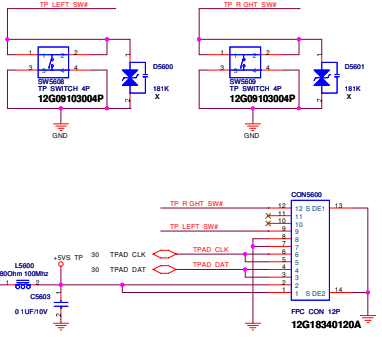


ASUS		Title: TV TUNER CONN	
ASUSTek COMPUTER INC		Engineer: Spark_Lee	
Size B	Project Name F7Kr	Rev 1.0	Rev 1.0
Date: 2007-11-17, 2007		Sheet 55	of 82

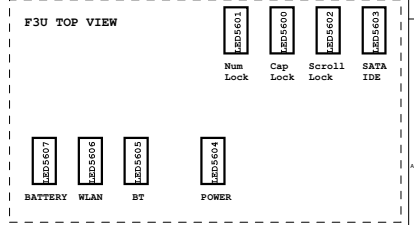
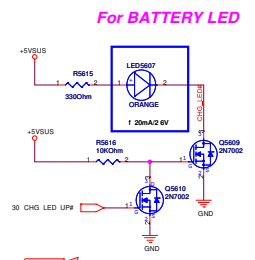
<< Kennedy_Zhang >>



TOUCH PAD SWITCH



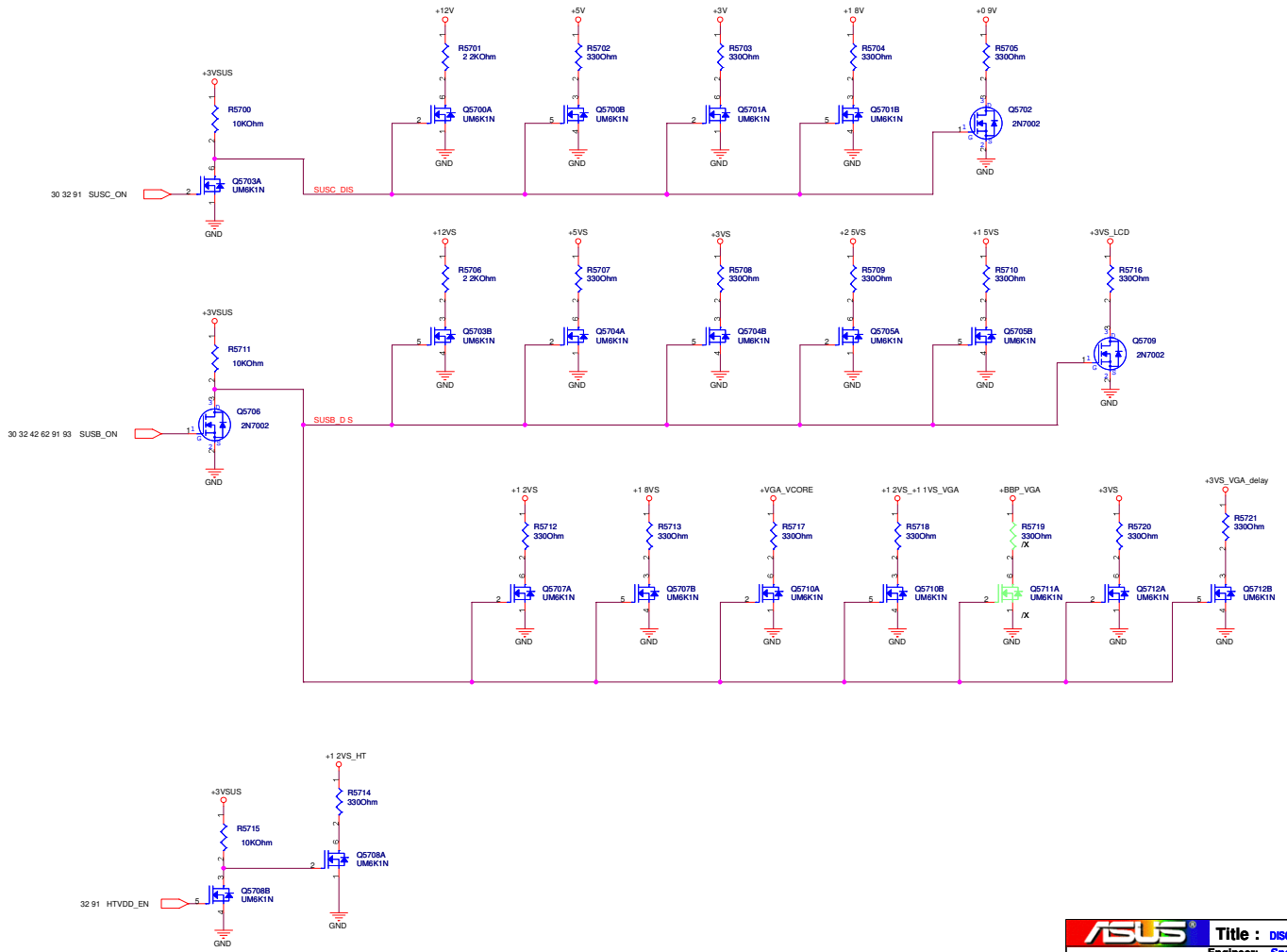
Green: 07G015700341
Orange: 07G015700064



ASUS		Title: LED&SWTOUCHPAD	
ASUSTEK COMPUTER INC.		Engineer: Spark_Lee	
BSA	P: oped Name	Rev	1.0
C	FR	Sheet	56 of 66
Date: 11-18-11			

« Kennedy_Zhang »

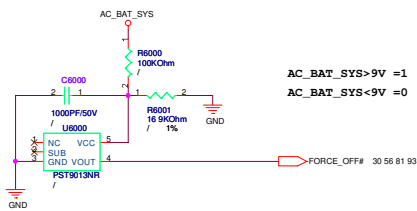
DISCHARGE CIRCUIT



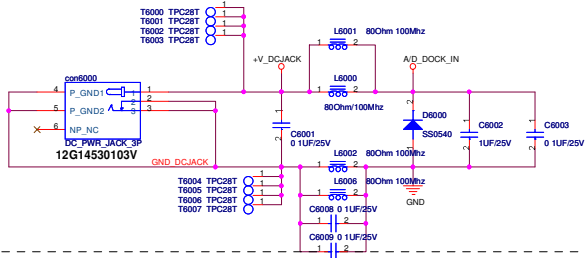
« Kennedy_Zhang »

ASUS		Title : DISCHARGE CIRCUIT	
ASUSTEK COMPUTER INC		Engineer: Spark_Lee	
Site:	Project Name:	Rev:	1.0
Cus on:	PTK	Date:	11/17/2007
Sheet 57 of 82			

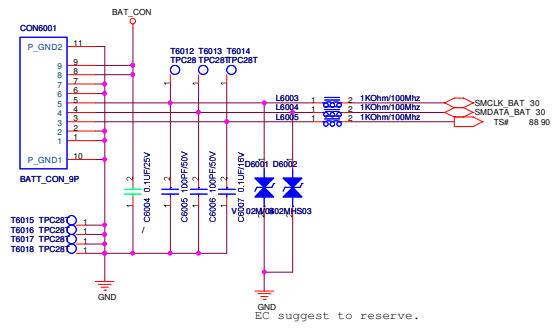
Without Battery & Pull out Adapter



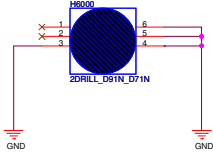
DC Power Jack



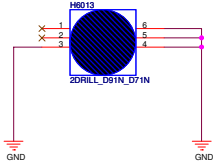
Battery Connector



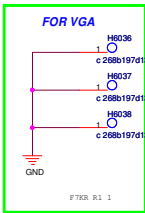
FOR LEFT UNDER



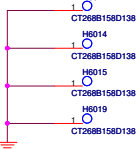
FOR RIGHT UP



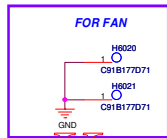
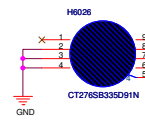
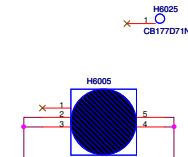
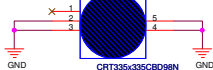
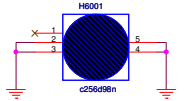
FOR VGA



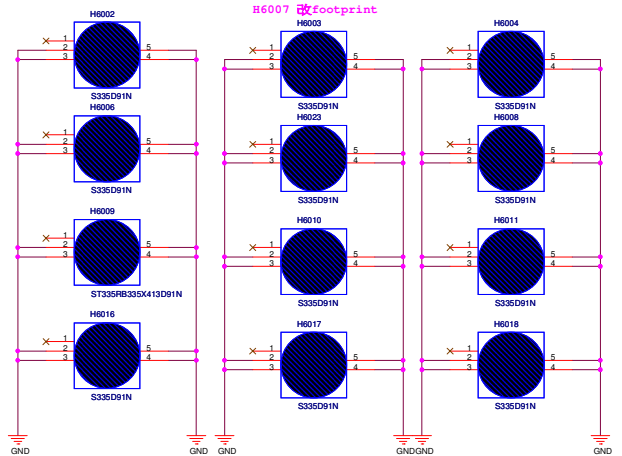
FOR CPU



FOR FAN



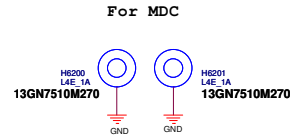
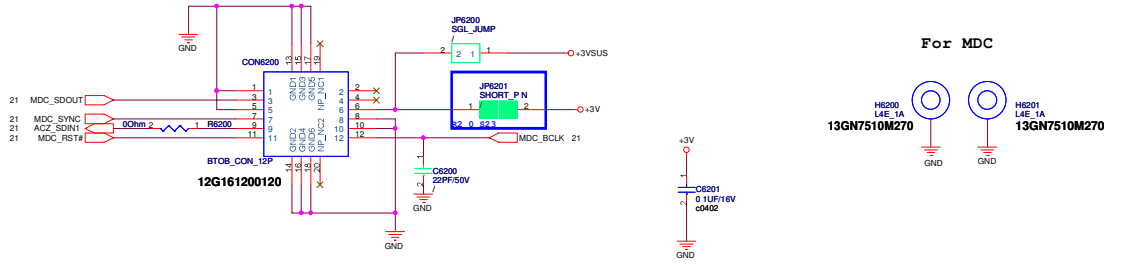
FOR SCREW HOLE



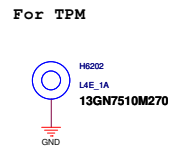
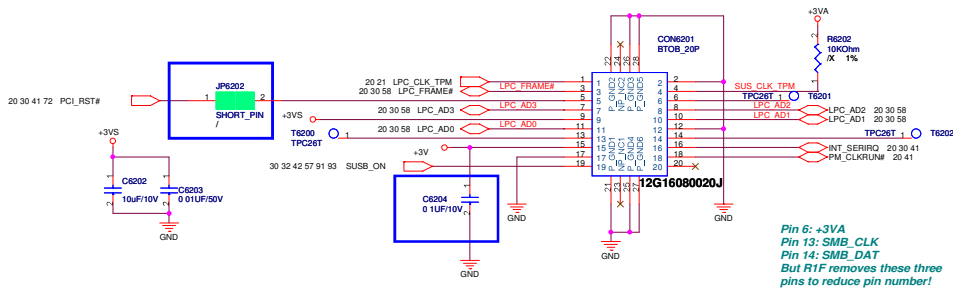
ASUS		Title : DC IN & SCREW HOLE	
ASUSTeK COMPUTER INC		Engineer: Spark_Lee	
Size	Project Name	Date:	Rev
Cus on	FTK	14/17/2007	1.0
Date: 14/17/2007		Sheet: 80 of 82	

« Kennedy_Zhang »

MDC CONN.



TPM CONN.

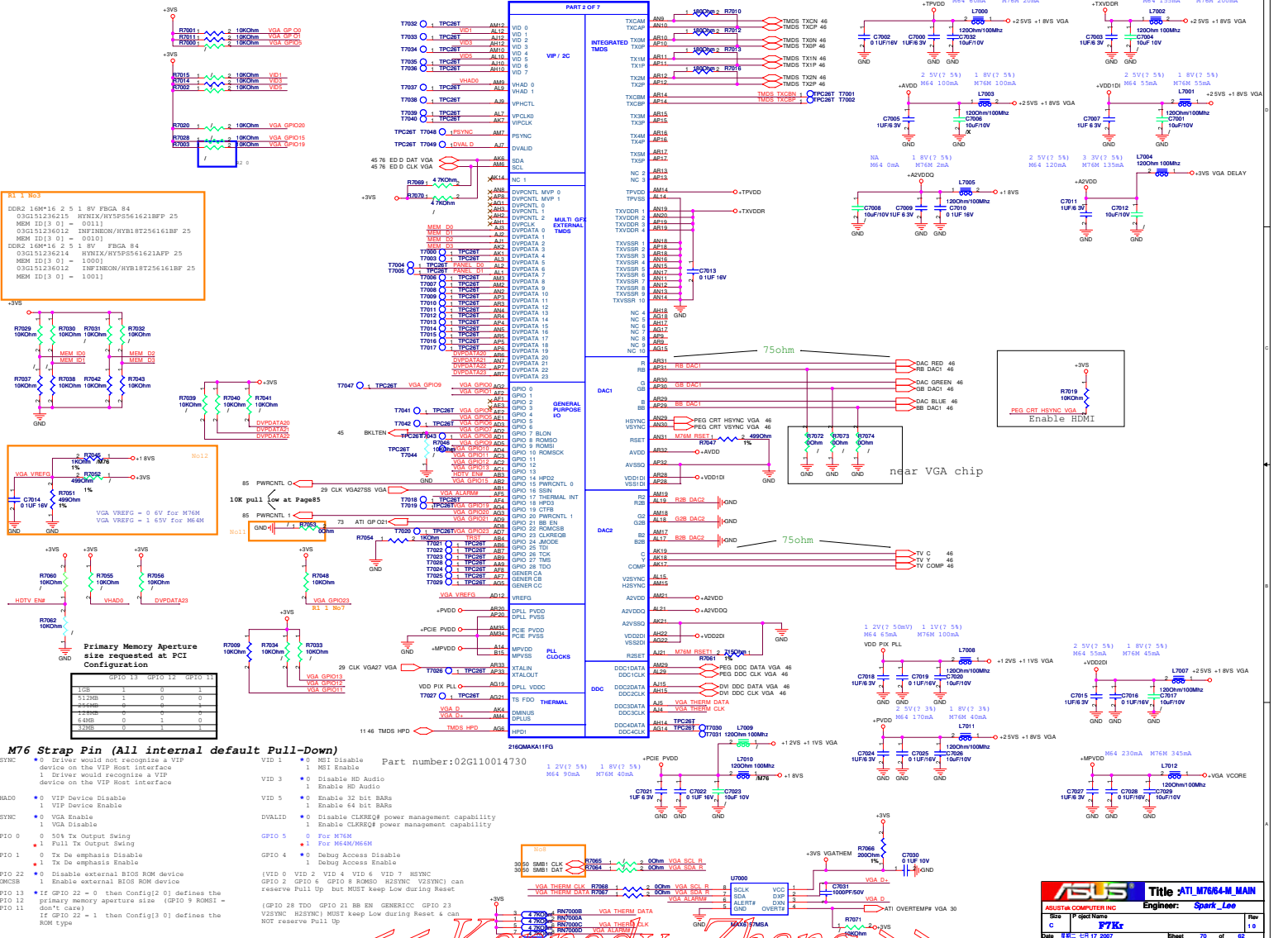


ASUS		Title : TPM&MDC CONNECTOR	
ASUSTEK COMPUTER INC		Engineer: Spark_Lee	
Site	Project Name	Rev	
Cus on	FTK	1.0	
Date: 8/8	14/17/2007	Sheet	62 of 62

« Kennedy_Zhang »

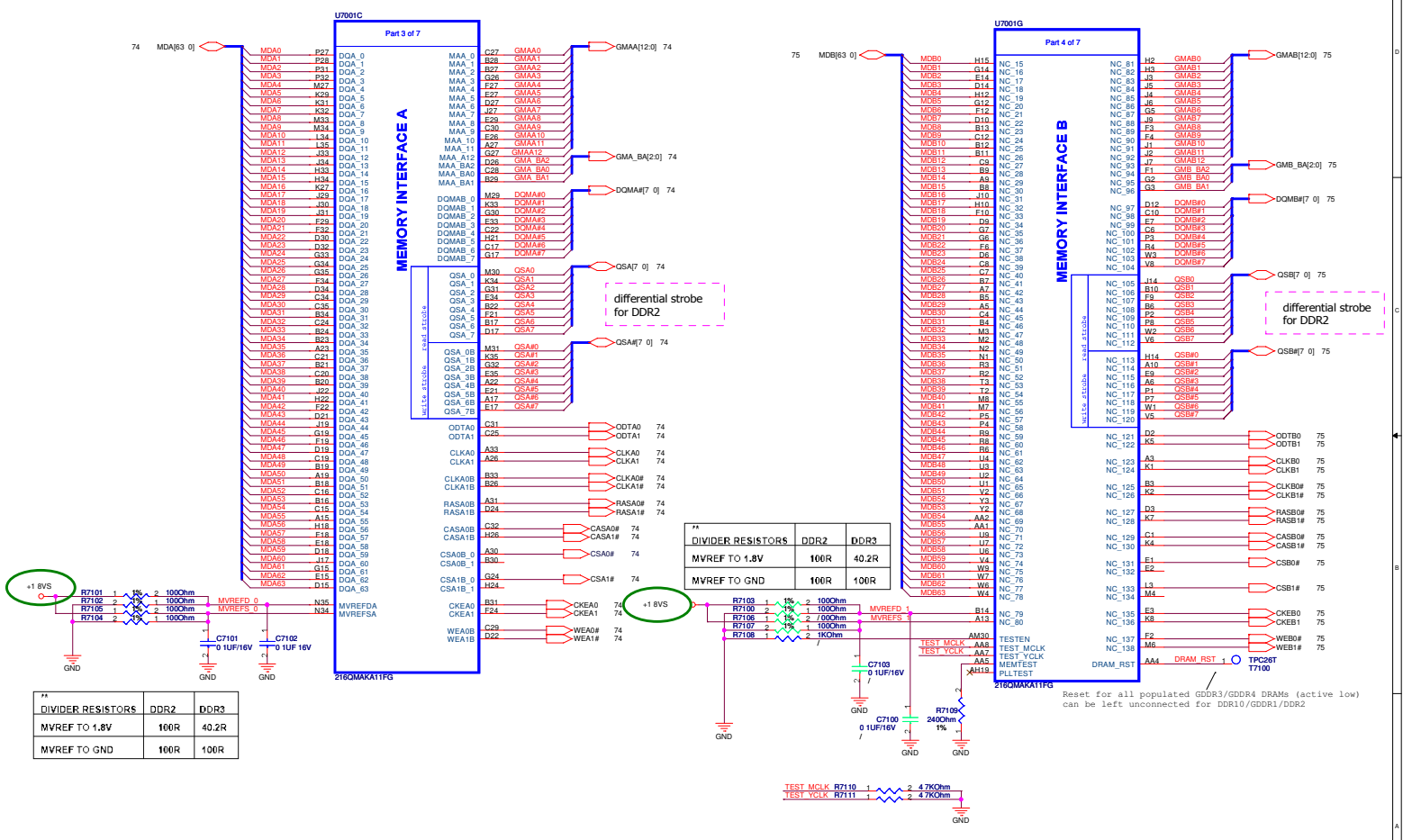
		Title : Finger Printer
ASUSTek Computer INC		Engineer: Spark_Lee
Size	Project Name	Rev
B	F7K	1.0
Date: 2007.11.17		Sheet 63 of 62

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ASUS		Title: ATI_M7684-M_MAIN	
ASUSTAR COMPUTER INC.		Engineer: Spark_Lee	
Ver:	P: Qcd Name:	Rev:	
C:	PTX:	1.0	1.0
Rev:	Rev:	Rev:	Rev:



** DIVIDER RESISTORS			
	DDR2	DDR3	
MVREF TO 1.8V	100R	40.2R	
MVREF TO GND	100R	100R	

** DIVIDER RESISTORS			
	DDR2	DDR3	
MVREF TO 1.8V	100R	40.2R	
MVREF TO GND	100R	100R	

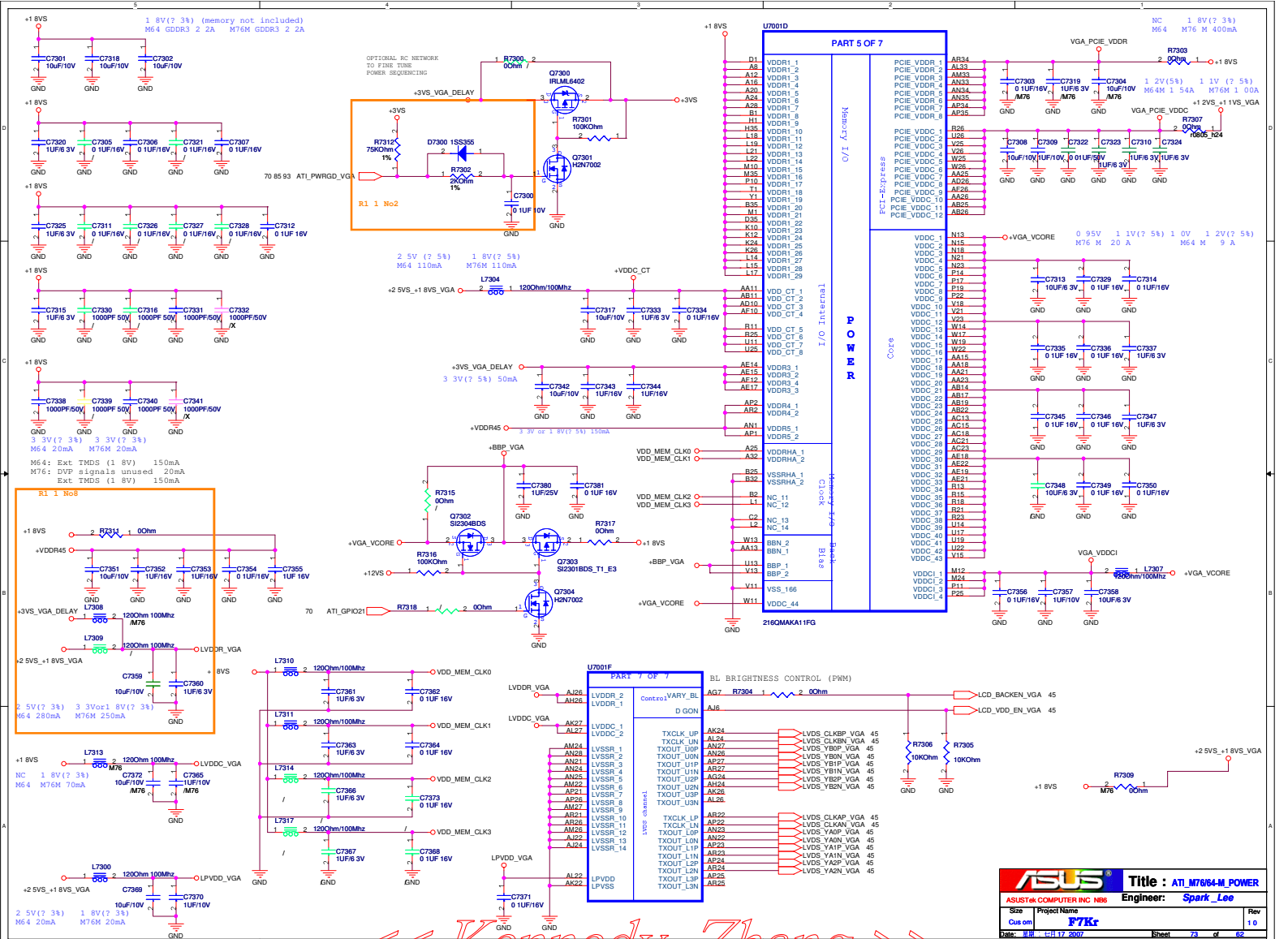
Reset for all populated GDDR3/GDDR4 DRAMs (active low) can be left unconnected for DDR10/GDDR1/DDR2

ASUS Title : AT1_M7684-M_Memory
 ASUSTek COMPUTER INC. NBE Engineer: Spark_Lee
 Size Project Name: Cus on FTKr
 Date: 8/8 14:17:2007 Sheet 71 of 82

« Kennedy_Zhang »

U7001E

Pin	Signal	Signal	Pin	Signal	Signal
P33	PCIE VSS 1	VSS 95	L33	PCIE ENB RANK0	C7261.2
P34	PCIE VSS 2	VSS 96	L34	PCIE ENB RANK1	C7262.2
P35	PCIE VSS 3	VSS 97	L35	PCIE ENB RANK2	C7263.2
P36	PCIE VSS 4	VSS 98	L36	PCIE ENB RANK3	C7264.2
P37	PCIE VSS 5	VSS 99	L37	PCIE ENB RANK4	C7265.2
P38	PCIE VSS 6	VSS 100	L38	PCIE ENB RANK5	C7266.2
P39	PCIE VSS 7	VSS 101	L39	PCIE ENB RANK6	C7267.2
P40	PCIE VSS 8	VSS 102	L40	PCIE ENB RANK7	C7268.2
P41	PCIE VSS 9	VSS 103	L41	PCIE ENB RANK8	C7269.2
P42	PCIE VSS 10	VSS 104	L42	PCIE ENB RANK9	C7270.2
P43	PCIE VSS 11	VSS 105	L43	PCIE ENB RANK10	C7271.2
P44	PCIE VSS 12	VSS 106	L44	PCIE ENB RANK11	C7272.2
P45	PCIE VSS 13	VSS 107	L45	PCIE ENB RANK12	C7273.2
P46	PCIE VSS 14	VSS 108	L46	PCIE ENB RANK13	C7274.2
P47	PCIE VSS 15	VSS 109	L47	PCIE ENB RANK14	C7275.2
P48	PCIE VSS 16	VSS 110	L48	PCIE ENB RANK15	C7276.2
P49	PCIE VSS 17	VSS 111	L49	PCIE ENB RANK16	C7277.2
P50	PCIE VSS 18	VSS 112	L50	PCIE ENB RANK17	C7278.2
P51	PCIE VSS 19	VSS 113	L51	PCIE ENB RANK18	C7279.2
P52	PCIE VSS 20	VSS 114	L52	PCIE ENB RANK19	C7280.2
P53	PCIE VSS 21	VSS 115	L53	PCIE ENB RANK20	C7281.2
P54	PCIE VSS 22	VSS 116	L54	PCIE ENB RANK21	C7282.2
P55	PCIE VSS 23	VSS 117	L55	PCIE ENB RANK22	C7283.2
P56	PCIE VSS 24	VSS 118	L56	PCIE ENB RANK23	C7284.2
P57	PCIE VSS 25	VSS 119	L57	PCIE ENB RANK24	C7285.2
P58	PCIE VSS 26	VSS 120	L58	PCIE ENB RANK25	C7286.2
P59	PCIE VSS 27	VSS 121	L59	PCIE ENB RANK26	C7287.2
P60	PCIE VSS 28	VSS 122	L60	PCIE ENB RANK27	C7288.2
P61	PCIE VSS 29	VSS 123	L61	PCIE ENB RANK28	C7289.2
P62	PCIE VSS 30	VSS 124	L62	PCIE ENB RANK29	C7290.2
P63	PCIE VSS 31	VSS 125	L63	PCIE ENB RANK30	C7291.2
P64	PCIE VSS 32	VSS 126	L64	PCIE ENB RANK31	C7292.2
P65	PCIE VSS 33	VSS 127	L65	PCIE ENB RANK32	C7293.2
P66	PCIE VSS 34	VSS 128	L66	PCIE ENB RANK33	C7294.2
P67	PCIE VSS 35	VSS 129	L67	PCIE ENB RANK34	C7295.2
P68	PCIE VSS 36	VSS 130	L68	PCIE ENB RANK35	C7296.2
P69	PCIE VSS 37	VSS 131	L69	PCIE ENB RANK36	C7297.2
P70	PCIE VSS 38	VSS 132	L70	PCIE ENB RANK37	C7298.2
P71	PCIE VSS 39	VSS 133	L71	PCIE ENB RANK38	C7299.2
P72	PCIE VSS 40	VSS 134	L72	PCIE ENB RANK39	C7300.2
P73	PCIE VSS 41	VSS 135	L73	PCIE ENB RANK40	C7301.2
P74	PCIE VSS 42	VSS 136	L74	PCIE ENB RANK41	C7302.2
P75	PCIE VSS 43	VSS 137	L75	PCIE ENB RANK42	C7303.2
P76	PCIE VSS 44	VSS 138	L76	PCIE ENB RANK43	C7304.2
P77	PCIE VSS 45	VSS 139	L77	PCIE ENB RANK44	C7305.2
P78	PCIE VSS 46	VSS 140	L78	PCIE ENB RANK45	C7306.2
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P82	PCIE VSS 50	VSS 144	L82	PCIE ENB RANK49	C7310.2
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P84	PCIE VSS 52	VSS 146	L84	PCIE ENB RANK51	C7312.2
P85	PCIE VSS 53	VSS 147	L85	PCIE ENB RANK52	C7313.2
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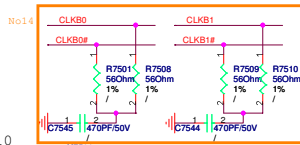


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ASUSTeK COMPUTER INC. <small>NEB</small>		Engineer: Spark_Lee	
Site		Project Name	
Cut on		Date: 8/8 14:17 2007	
Rev		Sheet 73 of 82	

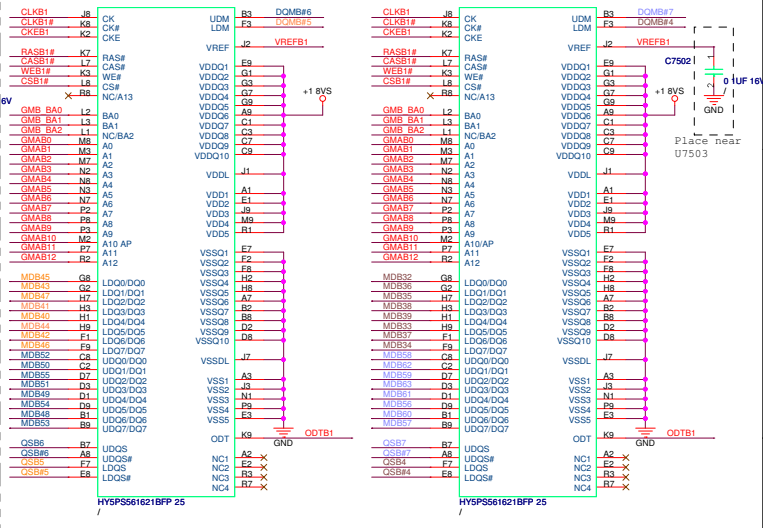
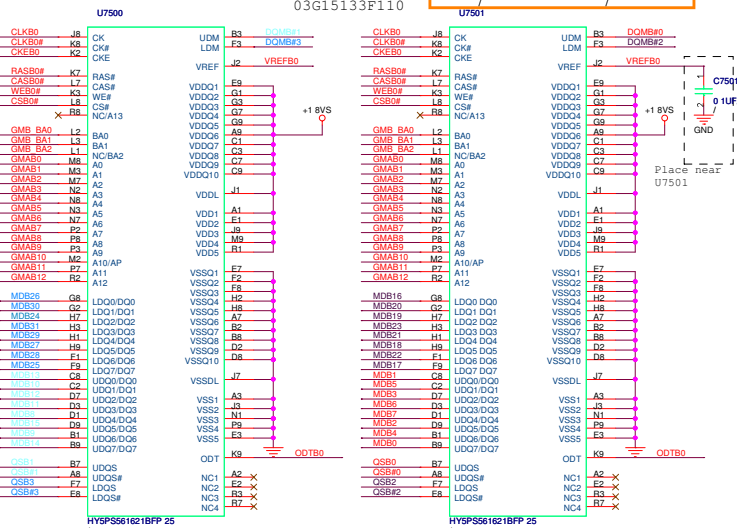
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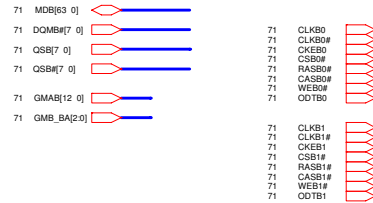
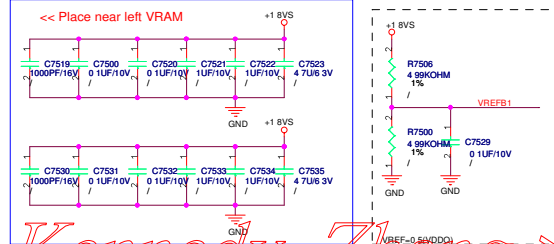
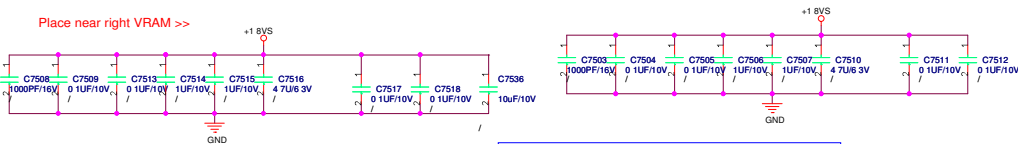
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B1



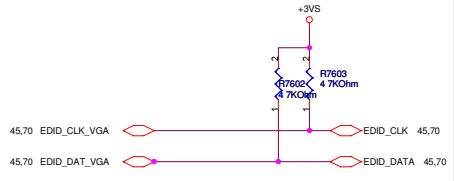
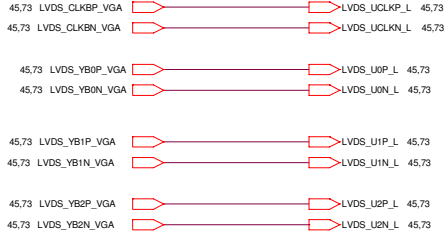
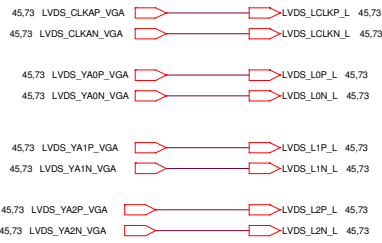
VDD/VDDQ = 1.8V

Place near right VRAM >>



« Kennedy_Zhang »

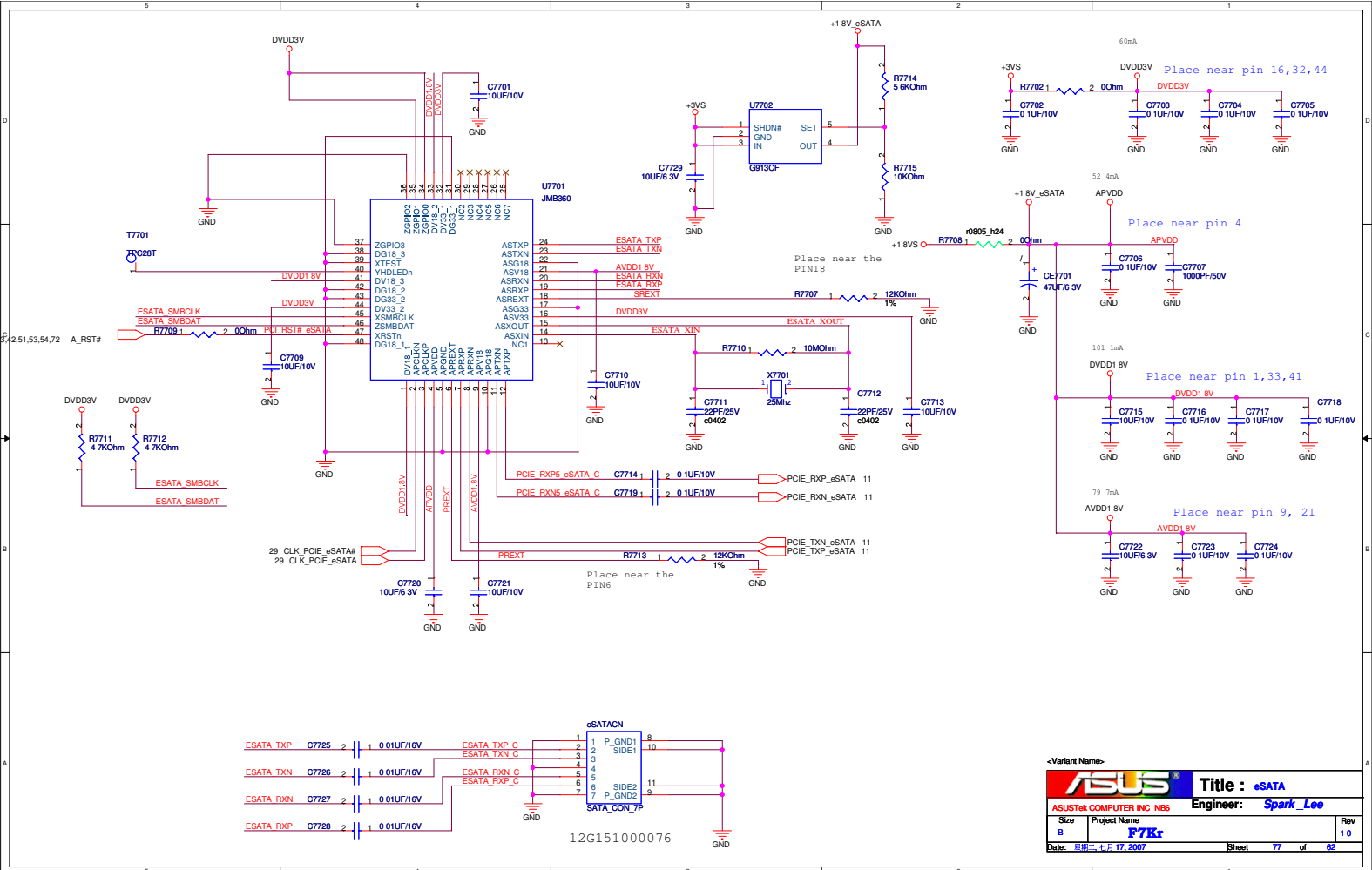
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 Size: Custom Project Name: FTKr Rev: 1.0
 Date: 2007-11-17 12:07:00 Sheet: 75 of 82



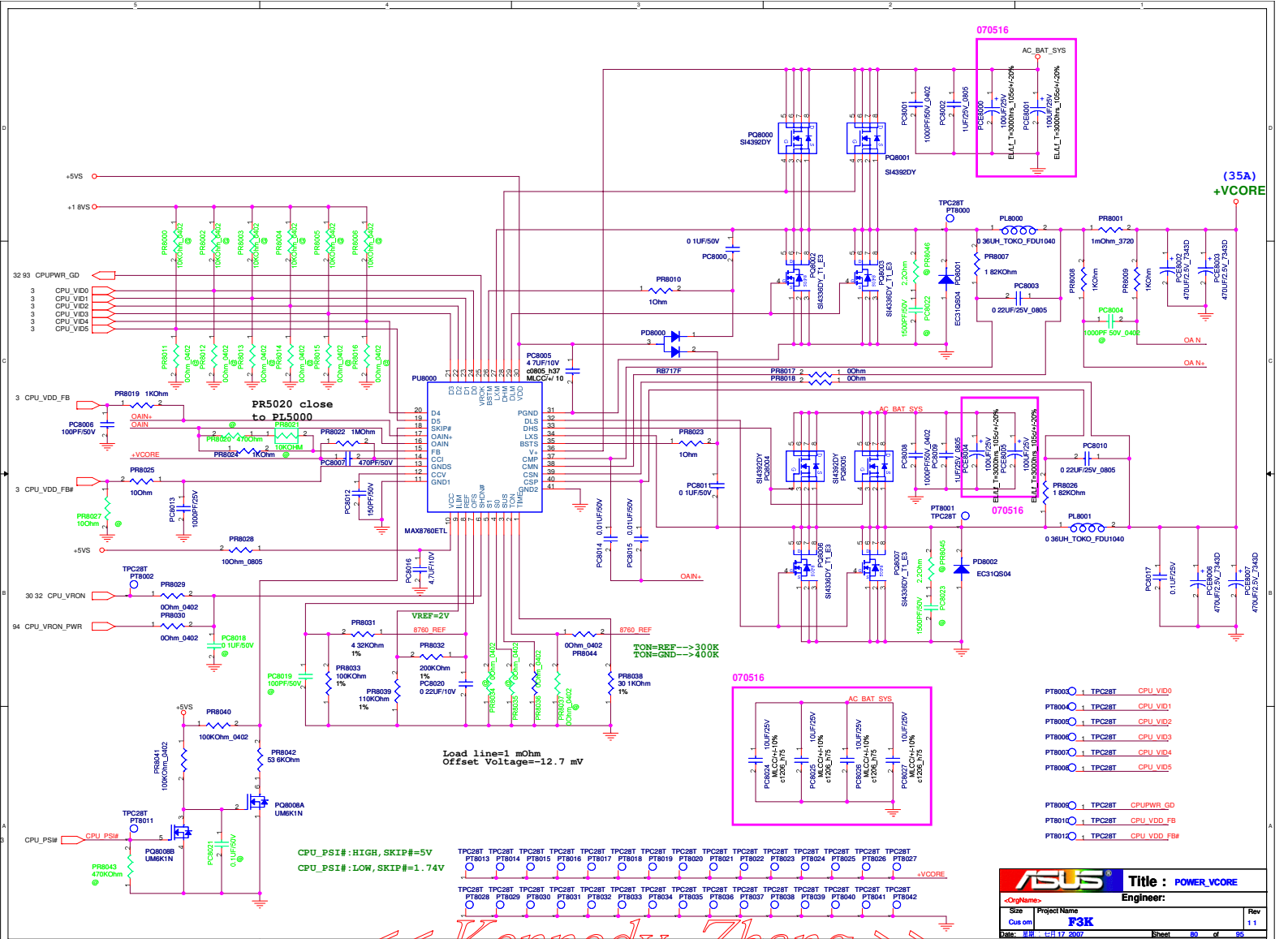
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ASUS		Title : LVDS SWITCH
ASUSTek COMPUTER INC NBS		Engineer: Sean Chou
Size B	Project Name F3Ka / F3Ke	Rev 1.1
Date: 2007-11-17		Sheet 76 of 82

<< Kennedy_Zhang >>

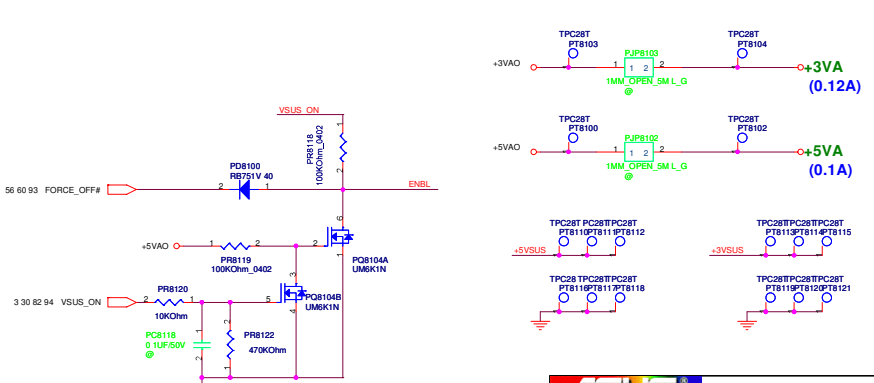
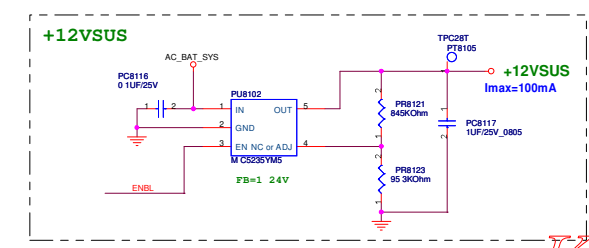
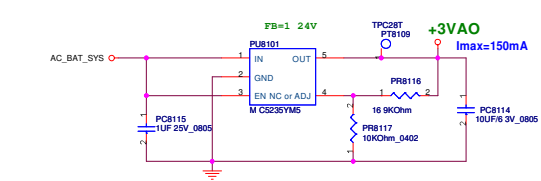
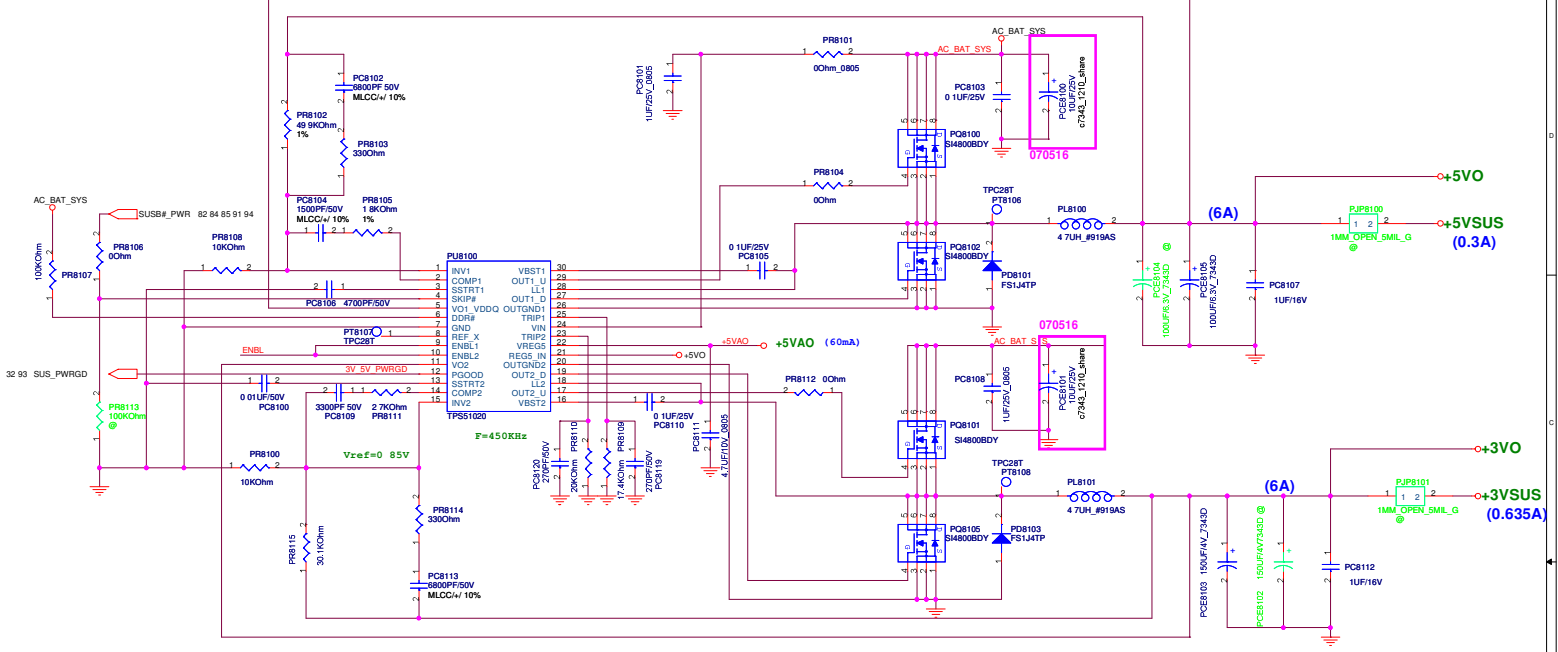


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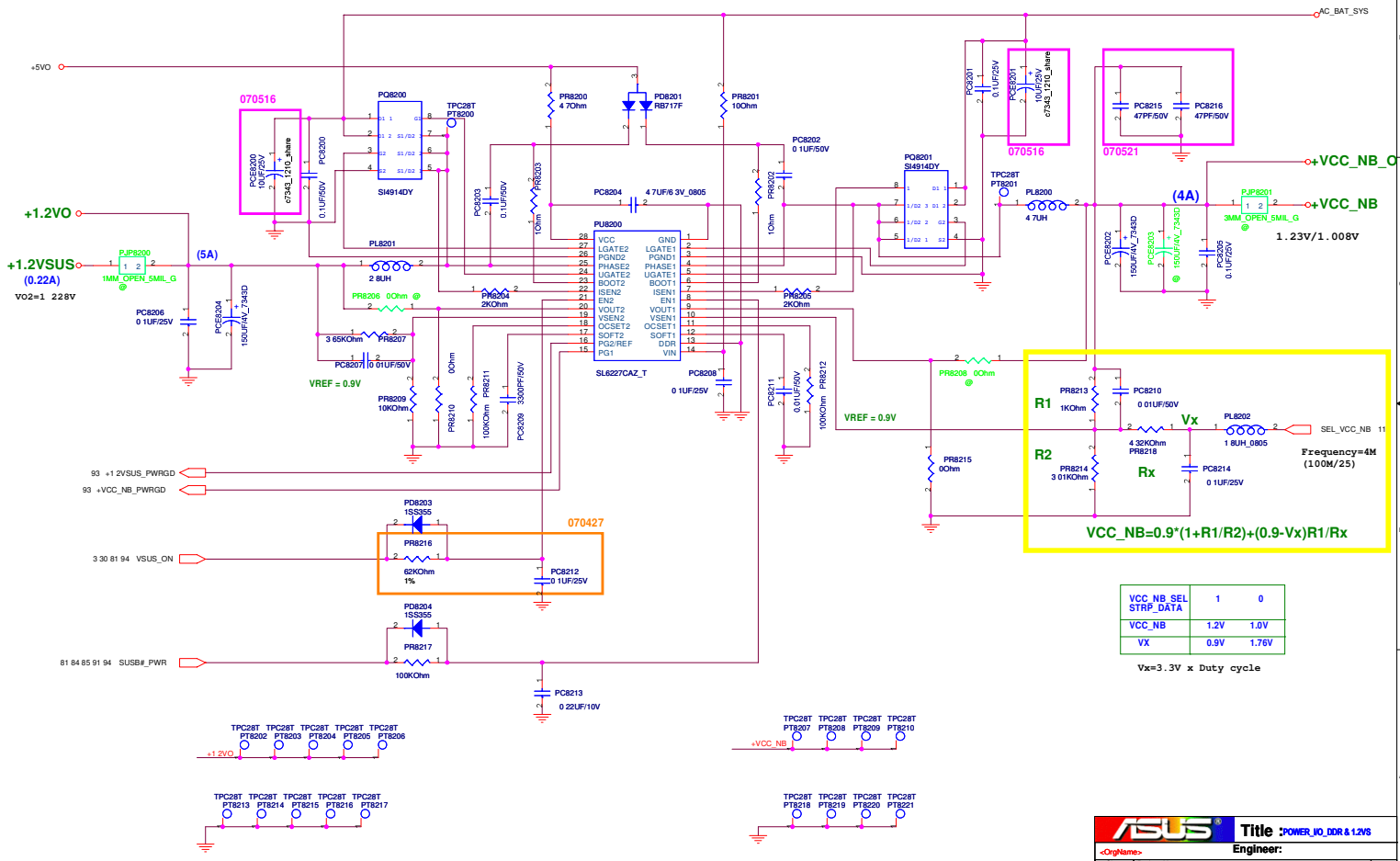
« Kennedy_Zhang »

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-<OrigName>		Engineer:	
Site	Project Name	Rev	
China	F3K	1.1	
Date: 8/8	14/17/2007	Sheet	80 of 85



ASUS		Title : POWER_SYSTEM
Engineer:		
Site:	Project Name	
Use on:	F3K	
Date:	14-17-2007	Sheet 81 of 85

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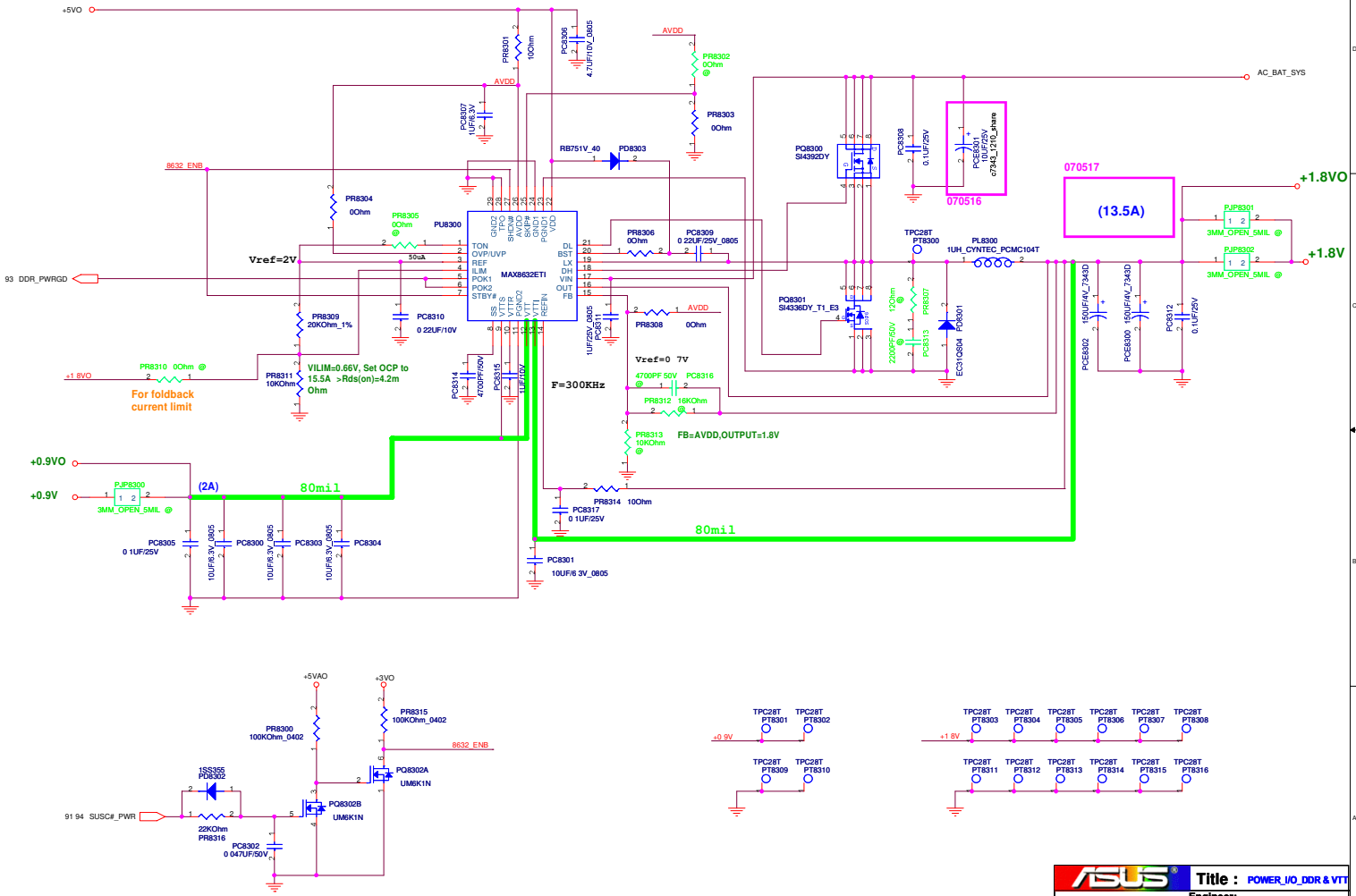


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VCC_NB	1.2V	1.0V
Vx	0.9V	1.76V

Vx=3.3V x Duty cycle

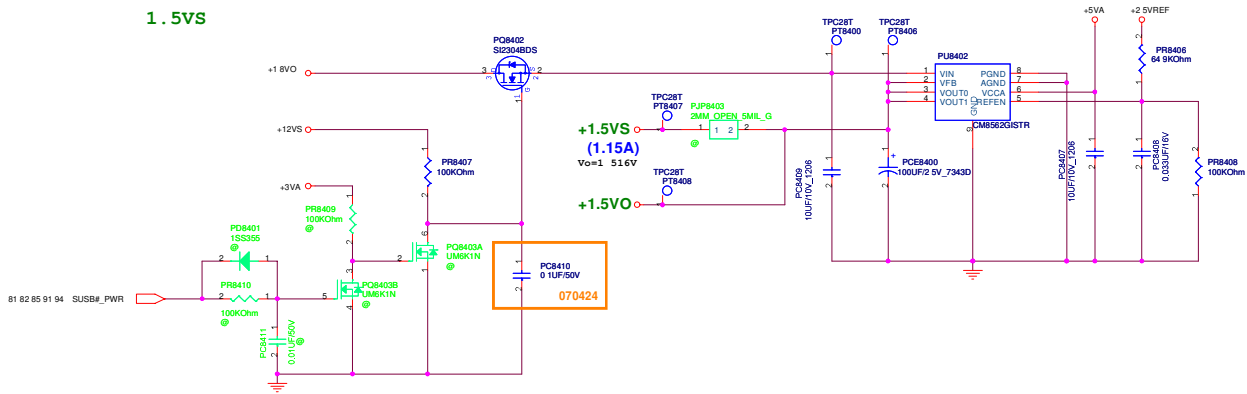
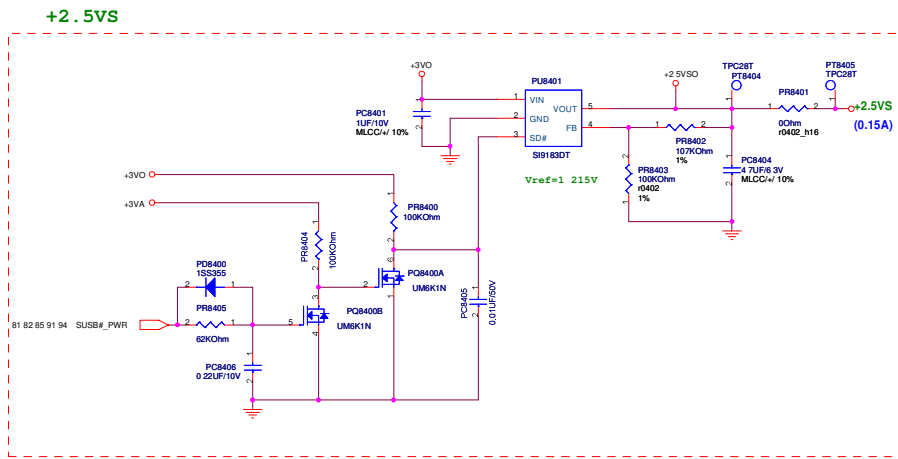
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-<OrigName>		Engineer:	
Size	Project Name	Rev	
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Cus om	FSK		
Date: 2007-04-17 20:07	Sheet	82	of 85

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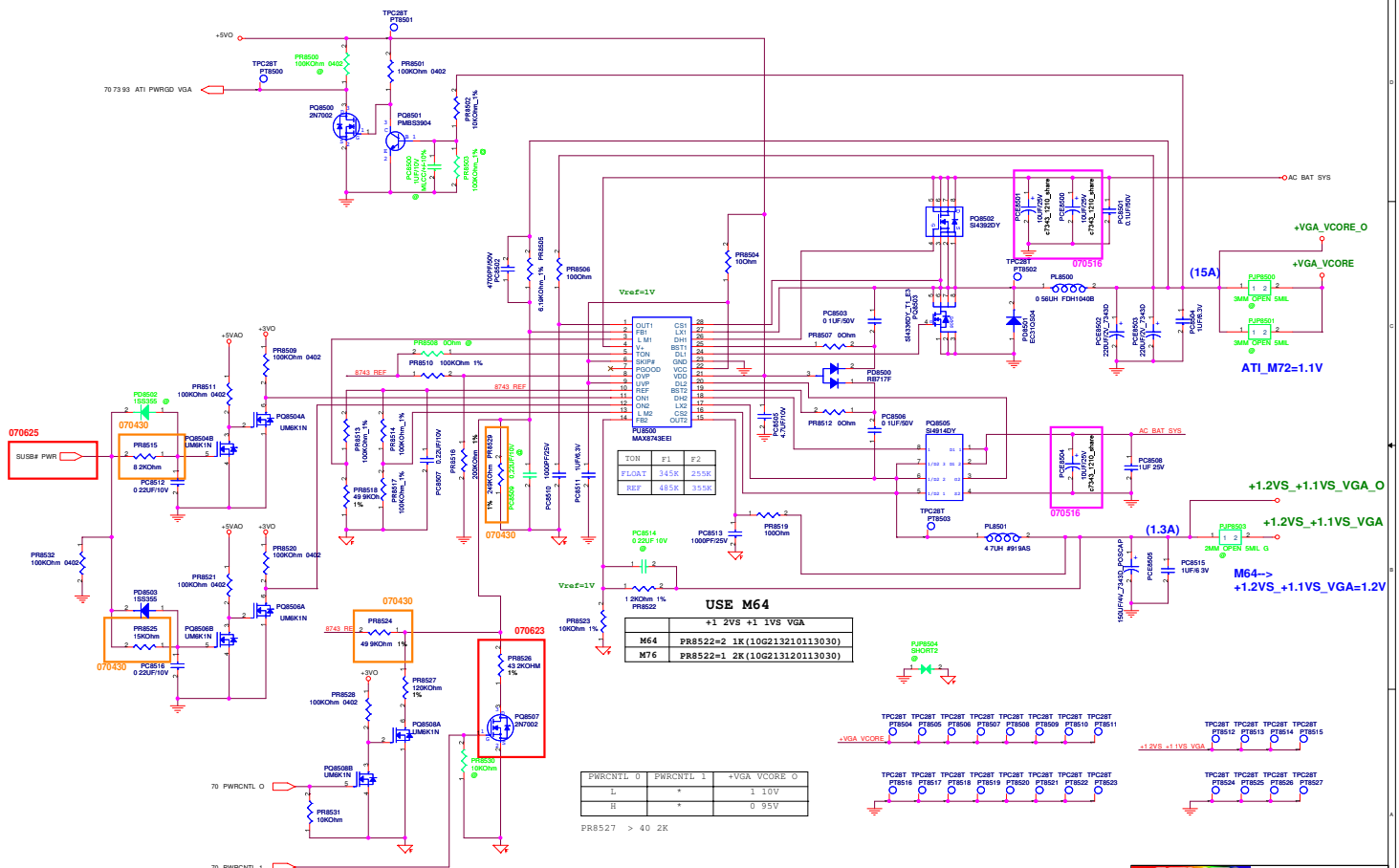
« Kennedy_Zhang »

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-<OrigName>		Engineer:	
Sz	Project Name		
Custom	F3K	Rev	1.1
Date: 11/17/2007		Sheet	83 of 98



ASUS		Title POWER_2.5VS& 1.5VS & 2.5VS	
S2a		Project Name	
Custom		F3K	
Date: 11/17/2007		Sheet 84 of 95	
Engineer:		Rev 1.1	

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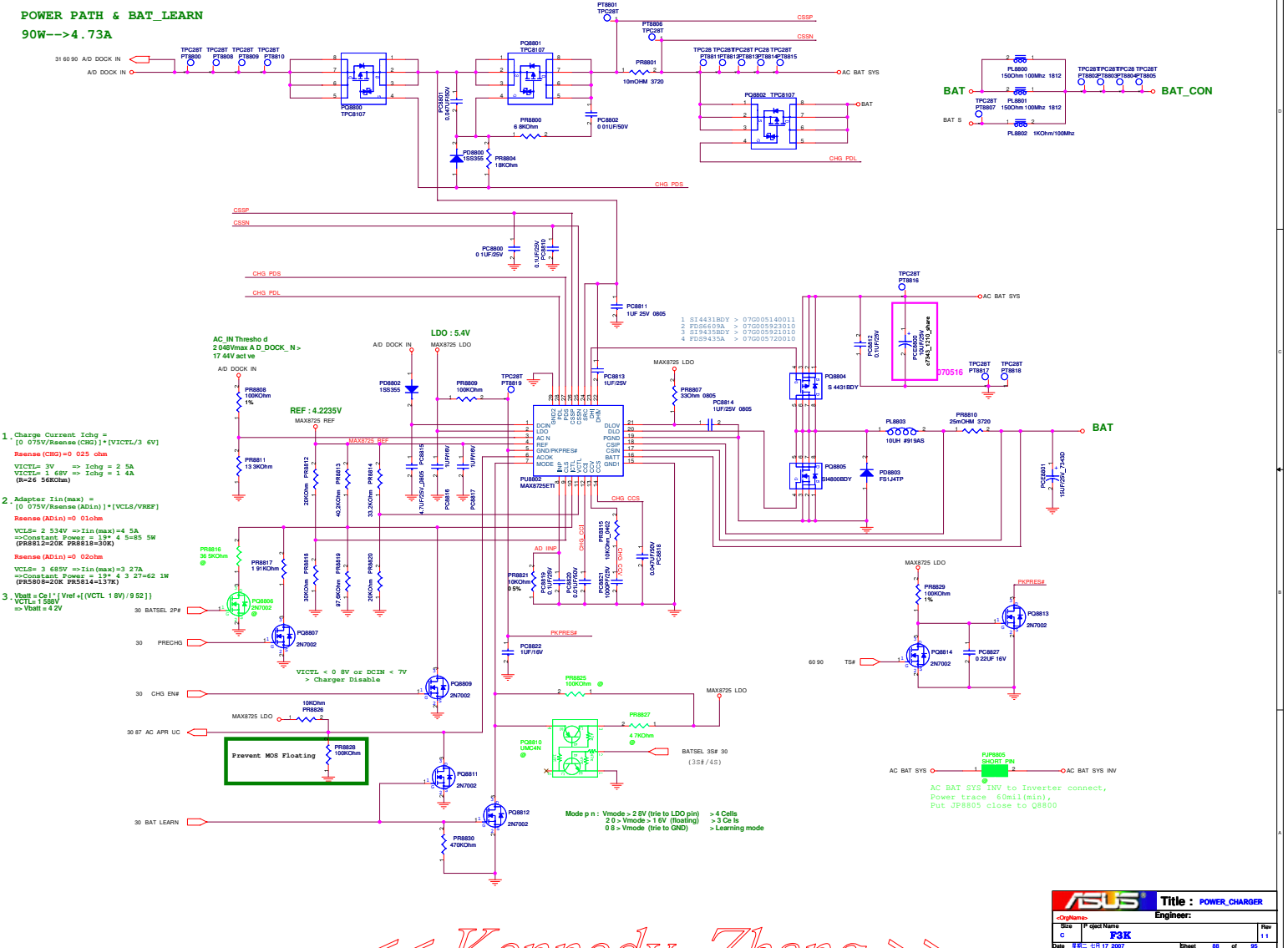
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Size	Project Name	Rev	
B	F3K	1.1	
Date: 2007-11-17	Sheet 86		of 95

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		Title : POWER_SHUTDOWN#	
<OrgName>		Engineer:	
Size	Project Name	Rev	
B	F3K	1.1	
Date: 2007.11.17	Sheet 87 of 95		

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POWER PATH & BAT_LEARN
90W-->4.73A



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ASUS		Title : POWER_CHARGER	
DocName:	Project Name:	Rev:	
Doc: 11-12-17-2007	Project Name: F3R	Rev: 11	
Sheet: 51	of: 51	of: 51	

D

D

C


C

B

B

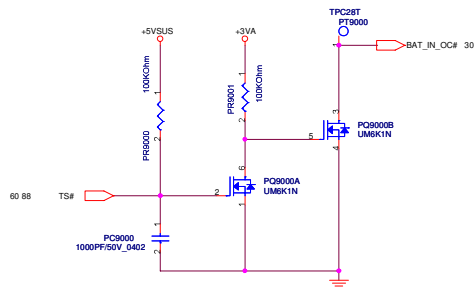
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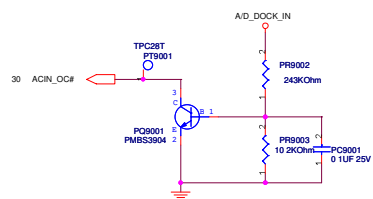
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Size	Project Name		Rev
A	F3K		1.1
Date: 星期二, 七月 17, 2007		Sheet	89 of 95

« Kennedy_Zhang »

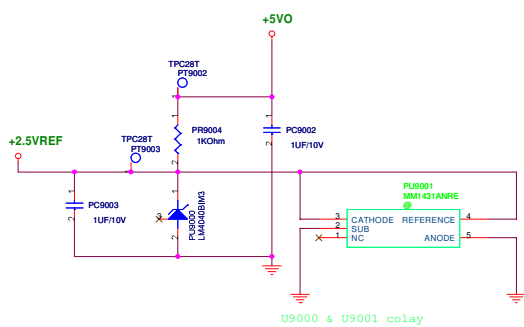
BATTERY IN DETECT



ADAPTER IN DETECT



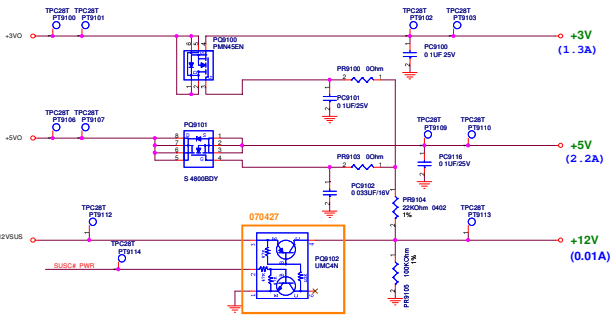
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-<OrigName>		Engineer:	
Site	Project Name	Rev	
Bus on	F3K	1.1	
Date: 8/8	14/17/2007	Sheet	80 of 88

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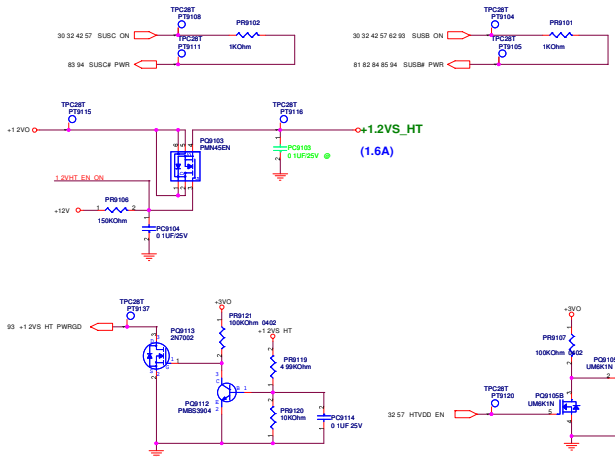
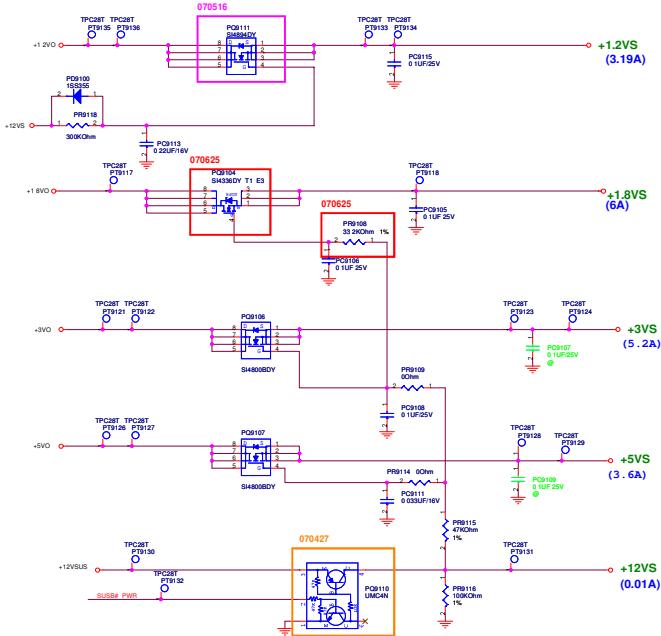
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070625

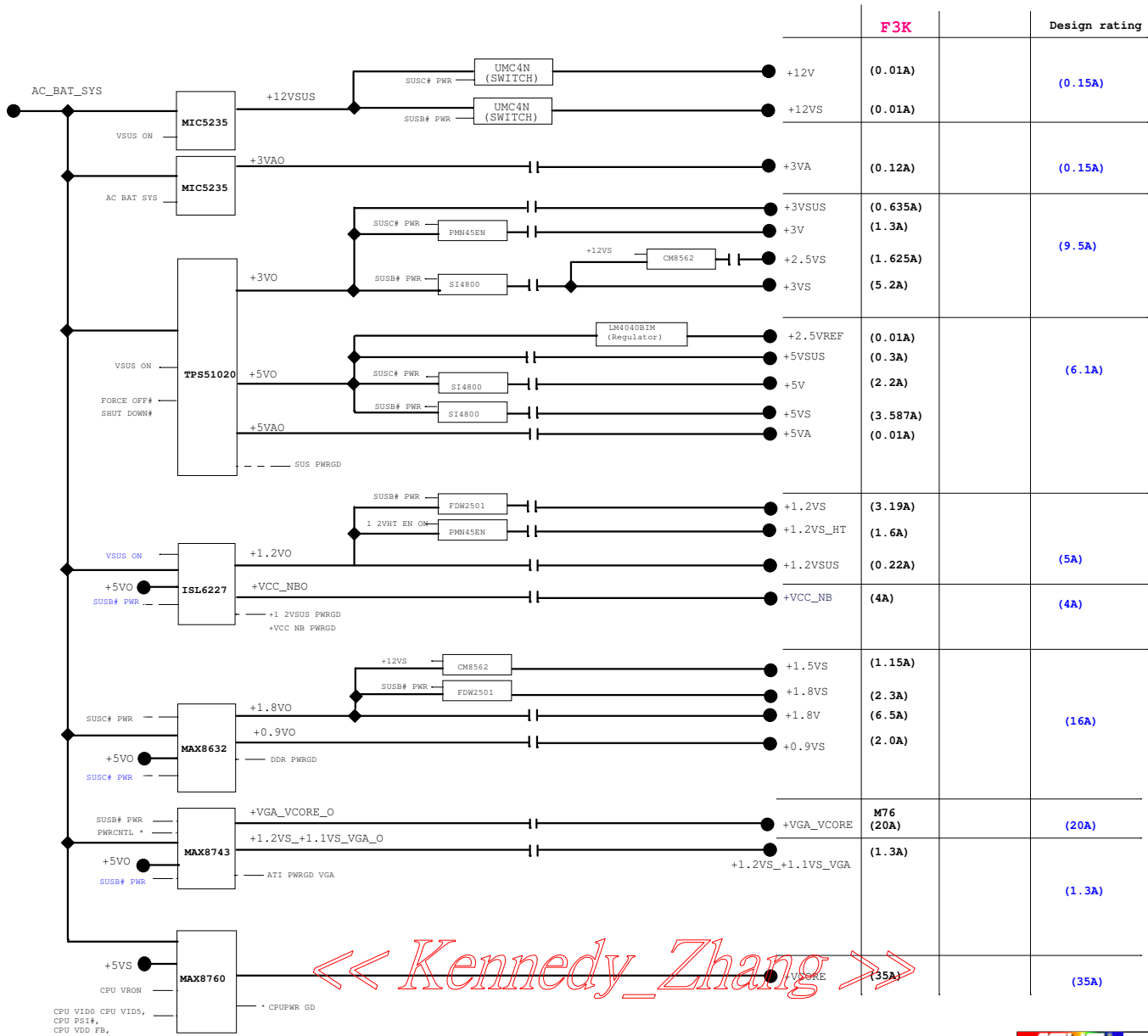


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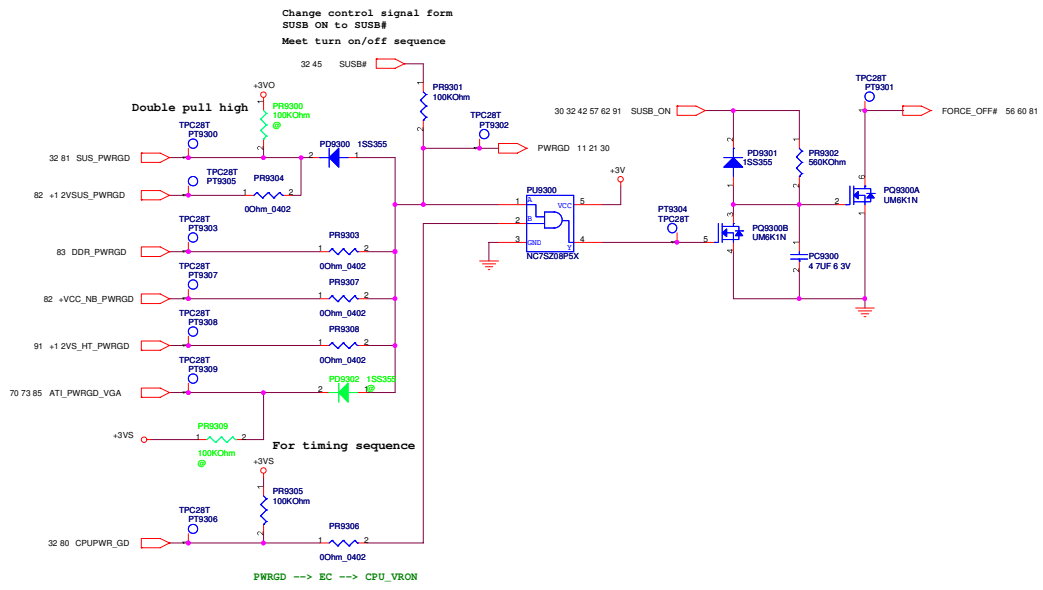
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Engineer:			
Task	Project Name	Rev	
Customer	FGK	11	
Date	08-17-2007	Page	11 of 25

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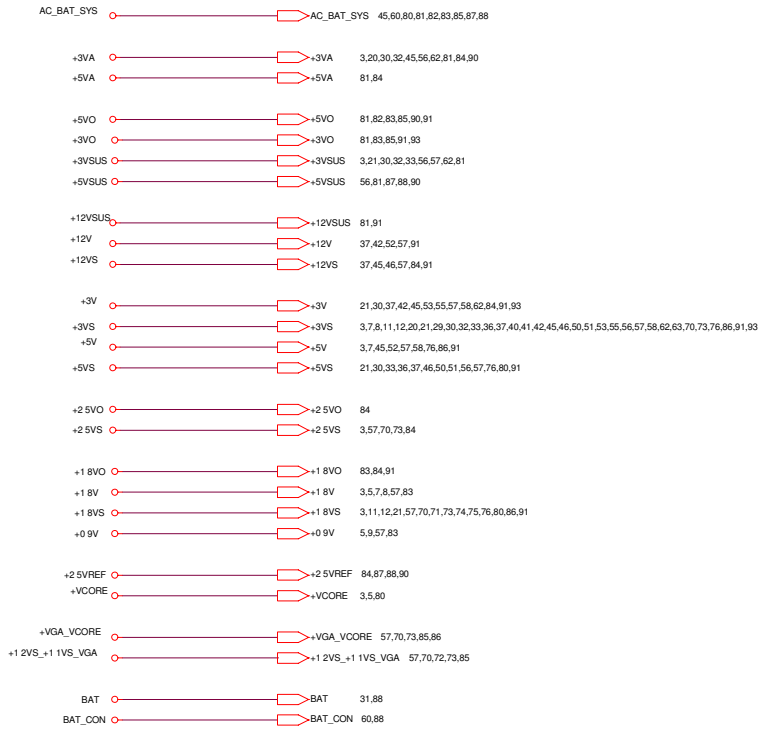
« Kennedy_Zhang »

POWER GOOD DETECTOR

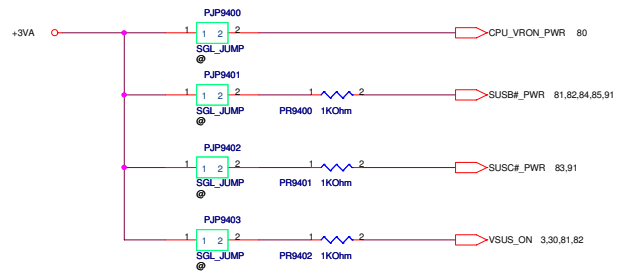


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ASUS		Title : POWER_PROTECT	
-<OrigName>		Engineer:	
Site	Project Name	Rev	
Site on	F3K	1.1	
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FOR POWER TEST



ASUS		Title : POWER_SIGNAL
<OrgName>		Engineer:
Size	Project Name	Rev
B	F3K	1.1
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3/2 Amp change to TPA6017

D

D

C


C

B

B

A

A

		Title : History
ASUSTek Computer INC. NB1		Engineer:
Size	Project Name	Rev
A	F3K	1.1
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12/08
13 RGB circuits modify
14 p53,54 add common choke
15 CE5200, CE5203 change package, USB add power name
16 New card change +3V PP
17 delete 0 ohm on P76 switch
18 net name USB_FAN# > test point; TVTUNER_ON# pull high to P55; VGNND change to GND
19 change P1205, C11201, L1202 and relative power name
20 unmount R2012, R2144, change AVDD_SATA# read to ZA
21 (SB) FANIN[2:0] & F56#IN2 & VGNND & VGNND & VGNND[2:7] use 10K to GND
12/12
13 power name +3VS VGATHEM
14 change R5C833 and unmount C4007
12/13
14 add add power name +3VS CB & +3VS FP, UIM FWR CON
15 swap VRAM
17/14
16 swap DDR, VRAM again
17 follow F5U; Delete R1120, R1121, R1122, R1123, D1100, Q1101, Change U1101 to 74126 to reduce cost
12/15
16 swap DDR
17 Change C2038 to mounting component to meet ATI's requirement
12/16
19 change P11 AVDD to NB AVDD to prevent short with P83
20 change package: U101, U701, P8R09, X3300, XZ011, P00300, U3602
21 delete 3 unknown line at P74: N17626888, N17631382, N17635879, and 1 power line: N62696617
22 delete another WMAW_MIC / WMAW_MIC port at P36
23 change C1100, C1100, C1100 package to C55000, C1100, C1100 for coincidence
12/20
21 change USB power plane
12/21
22 USB common choke swap (LP3, 1394) & swap USB 5,6,8
23 follow F3U, Change D5206, D5207, D5208, D5209 to mounting component to Protect the SB USB ports
12/25
26 add C4010 for EMI
12/26
27 swap LPC A03, LPC LDRQ#1 to termination, CLK CBPC1, LPC CLK, LPC CLK IFM, LPC CLK EC to RC
12/27
28 R3701, R3626, C3629 connect to GND AUDIO
12/30
31 add JP for RGB layout
1/3
2 D4200, R7200 change part
1/5
3 U4100, U5501 change part
3/4
4 C400 C403 mount
17/12
35 follow SB 600 errata, change R2022, R2023, R2024 to 680 ohm
36 C3613, C3614 unmount mistake, change to mount part
37 change power circuits

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R1 1 2007/01/23
N01: Page37, Strap correction
N02: Page37, add pull high add change RC value for sequence and C7300 change X7R
N03: Page70, M64 ID from 0x1 to 0x0
N04: Page70, R7009 change to /M76 because of M76:256MB, M64:128MB
N05: Page37, KB connector inversion
N06: Page37, follow demo circuits change to 1uF
N07: Page70, VGR GPIO23 pull high
N08: Page73, follow ref131 5, delete VDDR45 3 3V path & 1VDDR 3 3V for M76M, 2 5V for M64M
N09: Page54, unmount R5405 (for RST of WMAW) for SR function
N10: Page45, C4502 change to 0 1uF for fixing white screen from CMOS setup change to 0 22uF
N11: Page20, modify PC# CLK[0] damping R
N12: Page29, SS clock gen will be changed to ICS252 R2949 3 92ohm for M64, R2953 82ohm for M76
N13: Page29, CLK for PCIe VGA is changed from SR04 to AT01
N14: Page55, unmount R5501 for not supporting TV wake function
N15: Page21, A SATA (for optional) use for WMAW & WMAW USB for TVTUNER
N16: Page33, A SATA to LAN use MOS for leakage issue
N17: Page21, A SATA (for optional) add inverter 2: USB# use for inverter 1 and inverter 2 and CE4501 change to H 1 1
N18: Page52, USB ESD diode need mount
N19: Page42, A SATA to NW C400, add diode for leakage issue
N20: Page46, change R4626 & R4627 to 2 7K ohm for CR1 detect issue, R4623 & R4624 for DVI function
N21: Page21, change R4102 to 1 1K for USB eye diagram
N22: Page55, change TV TUNER connector and mtb lower for thermal issue
N23: Page71, R5572, R4530, R4505, R4500 swap
N24: Page71, delete R4210; because R4210 does the same function, change branch to page 45
N25: Page51, R5500 change part for height issue
N26, Page20, modify RTC capacitor 18pF

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		Title : Modified list	
ASUSTek Computer, Inc.		Engineer: Sean1.Chou	
C	F3Ra / F3Ke	Rev	11
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