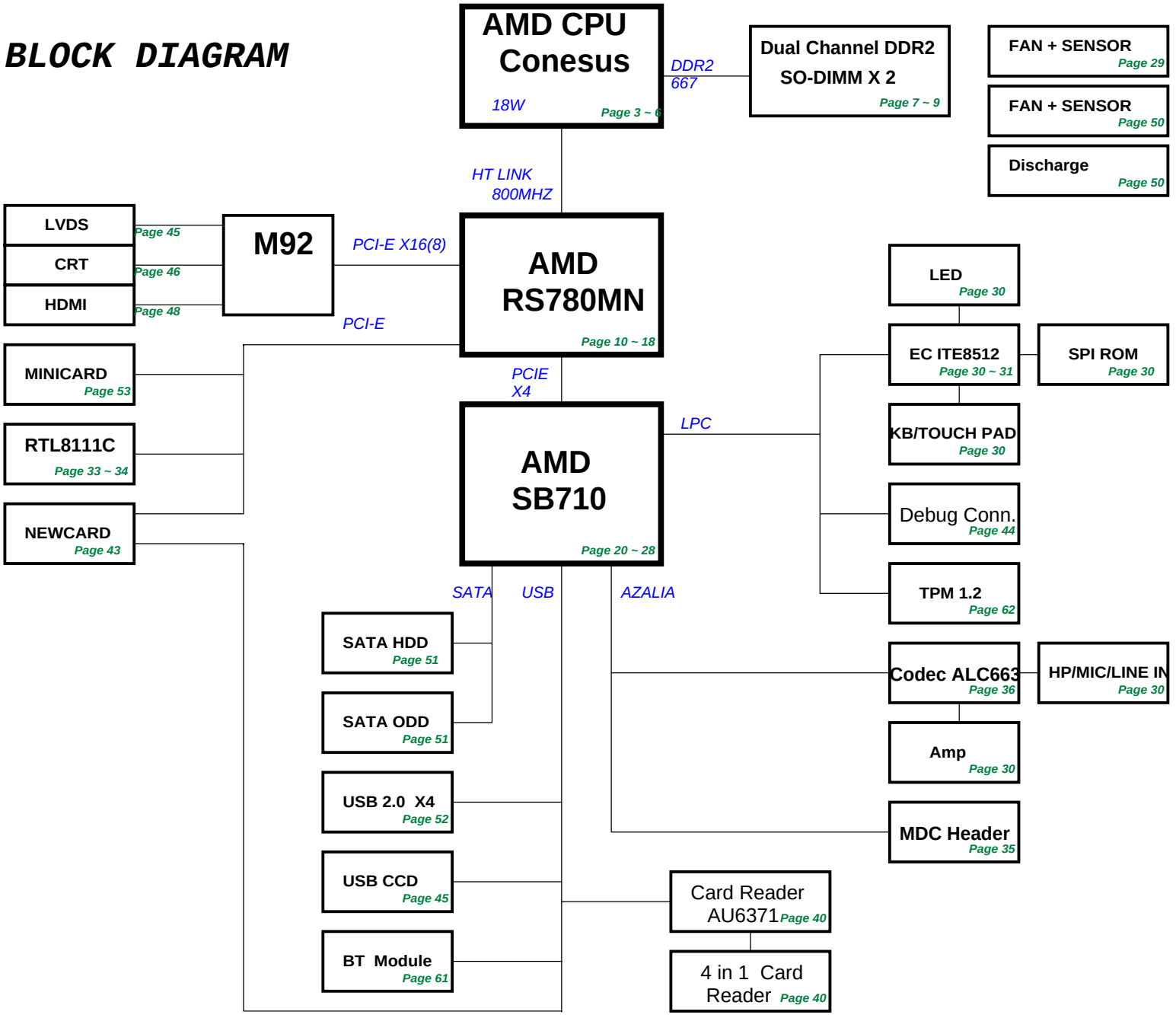
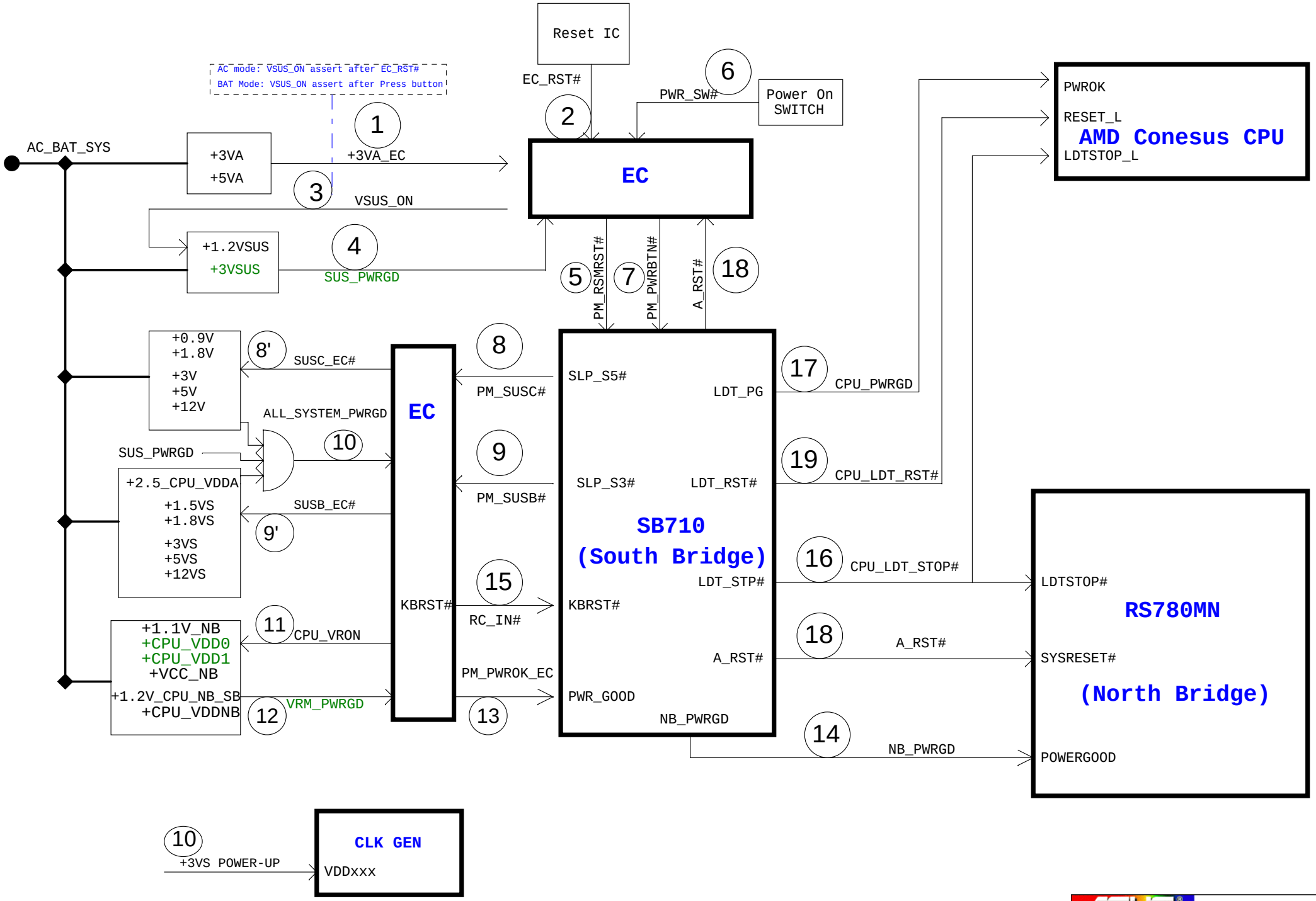
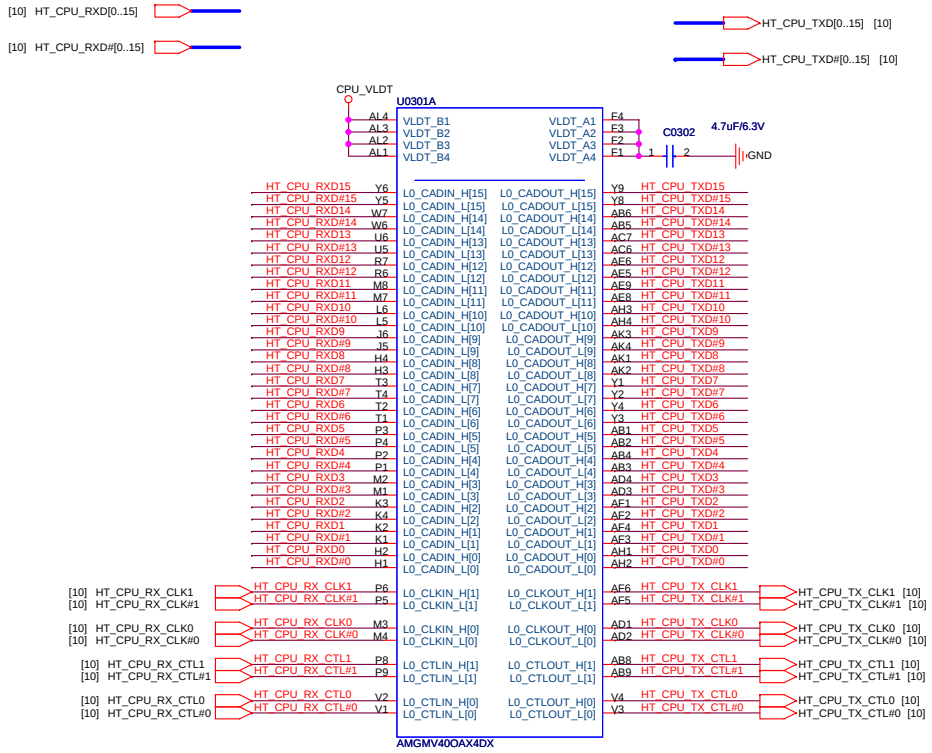
BLOCK DIAGRAM



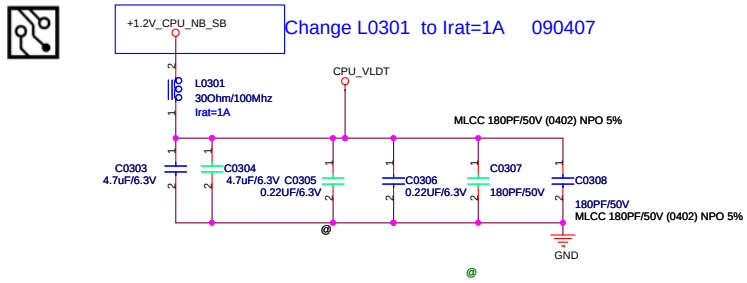
ASUSTeK Computer INC	Title : Block Diagram	
	Engineer: Ice_wang	
Size: Custom	Project Name: F83T	Rev: 1.0
Date: Tuesday, May 26, 2009	Sheet 1 of 91	



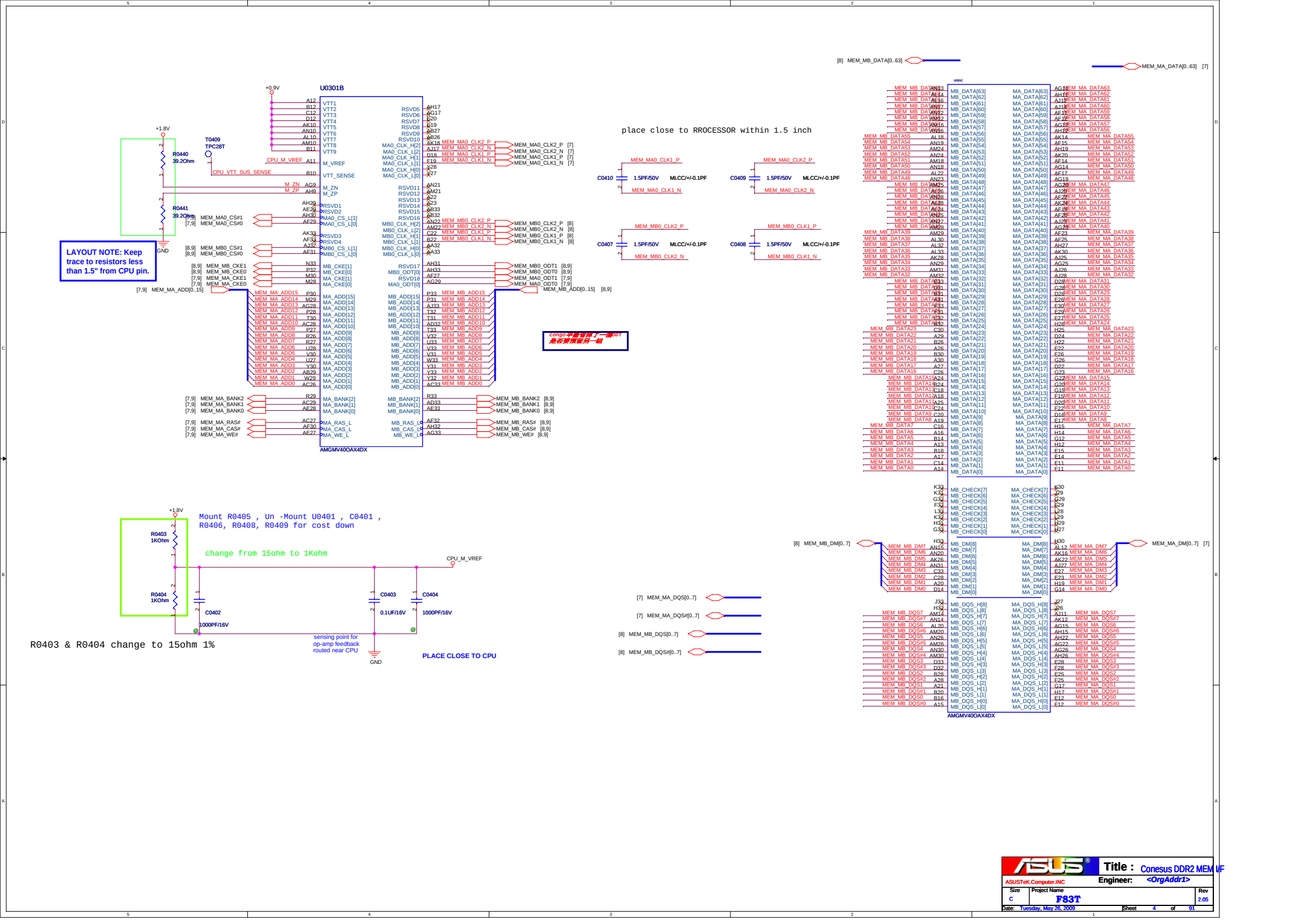
Title :	Power sequence
ASUSTeK.Computer.INC	Engineer: <OrgAddr1>
Size: Custom	Project Name: F83T
Rev: 2.05	
Date: Tuesday, May 26, 2009	Sheet 2 of 91



DESIGN NOTE:
VLDT must be routed as a pour or a trace at least 200 mils wide.
VLDT may be routed from the source to either ALx balls or Fx balls.
Choose whichever makes routing simpler.
These six capacitors must be placed very near the selected balls.
The "other" set of balls must be decoupled with a 4.7uF cap.



ASUSTeK.Computer.INC	Title : Conesus HT I/F		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: F83T		Rev: 2.05
Date: Friday, May 29, 2009	Sheet 3 of 91		


U0301B
AMGMV40OAX4DX
LAYOUT NOTE: Keep trace to resistors less than 1.5" from CPU pin.
place close to RROCESSOR within 1.5 inch
compo中是省掉了一個ODT 是否要預留另一組
Mount R0405 , Un -Mount U0401 , C0401 , R0406, R0408, R0409 for cost down
change from 15ohm to 1Kohm
R0403 & R0404 change to 15ohm 1%
sensing point for op-amp feedback routed near CPU
PLACE CLOSE TO CPU
Title : Conesus DDR2 MEM I/F
ASUSTeK.Computer.INC
Engineer: <OrgAddr1>
Size C
Project Name F83T
Rev 2.05
Date: Tuesday, May 26, 2009
Sheet 4 of 91

NOTICE

If PWROK,RESET_L,LDTSTOP_L are driven by open-drain driver, a 300 ohm pull up to VDDIO.

mount cap C0503 (AMD要求)
power LDO 部分輸出是否可以省掉一個10uf cap

for warm reset

PROCHOT

EC to CPU/PWR

THRNTRIP

NOTICE r0541

HDT

Debug 預留 090405

VID5 is optional

PSI_L is a Power Status Indicator signal.

Change 300 ohm to 4R8P 090405

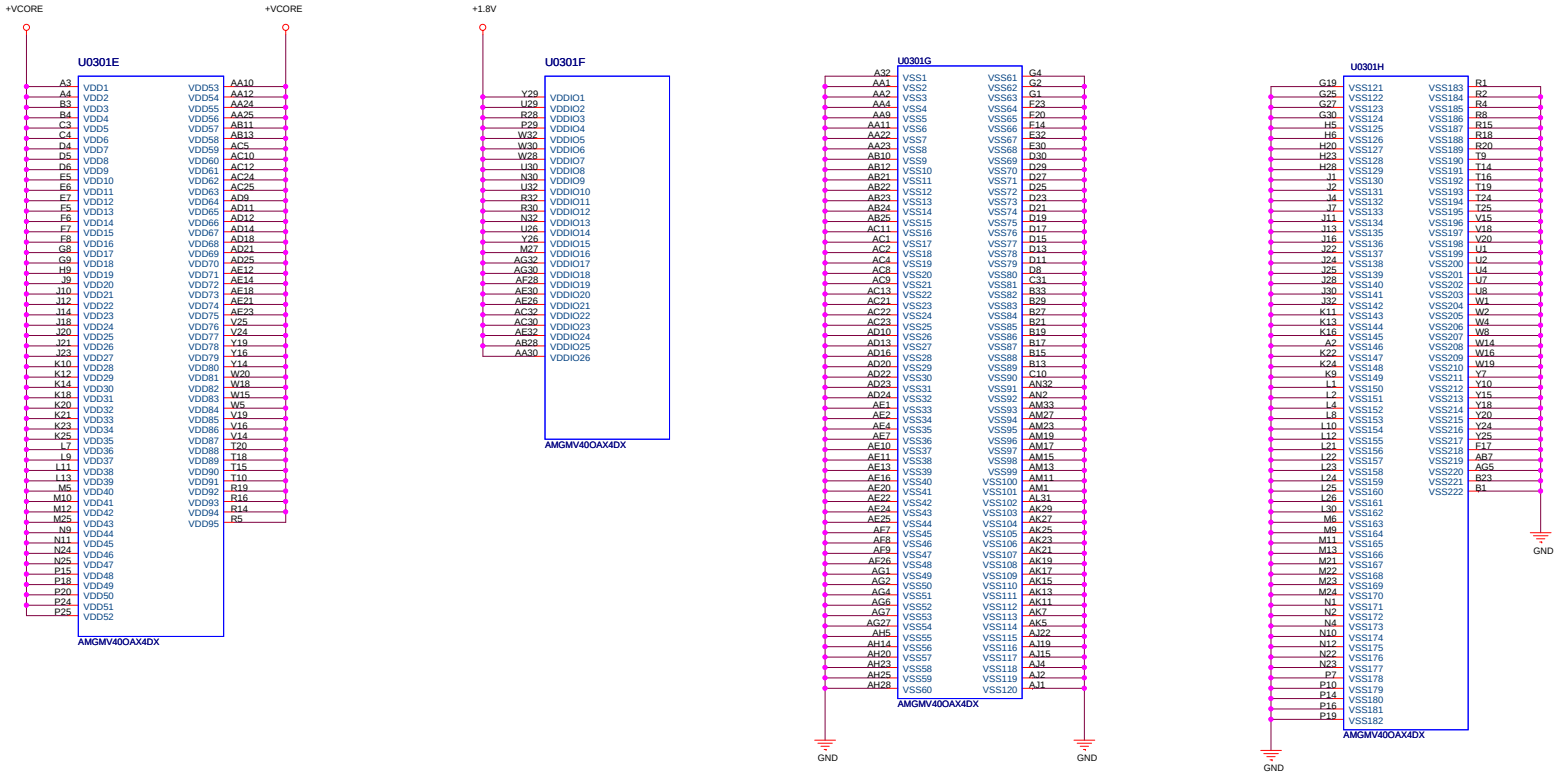
U0301D

AMGMV40OAX4DX

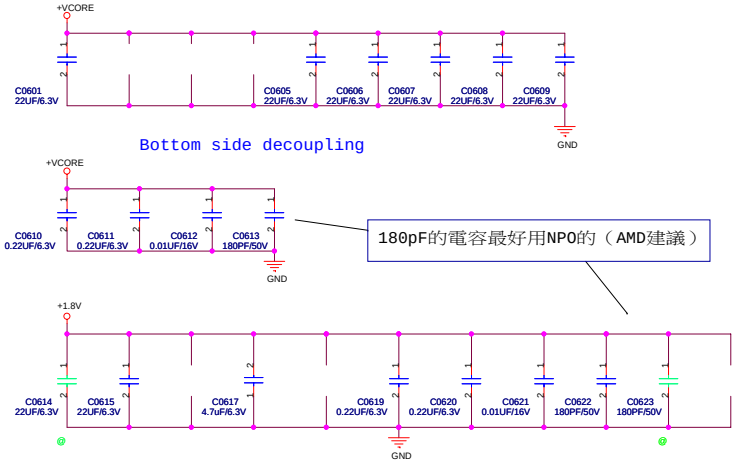
J0500

ASP_68200_07_K25
/X

ASUSTeK.Computer.INC		Title: Genesus CNT/DBG/THERM	
		Engineer: <OrgAddr1>	
Size: C	Project Name: F83		Rev: 2.05
Date: Tuesday, May 26, 2009		Sheet 5 of 91	

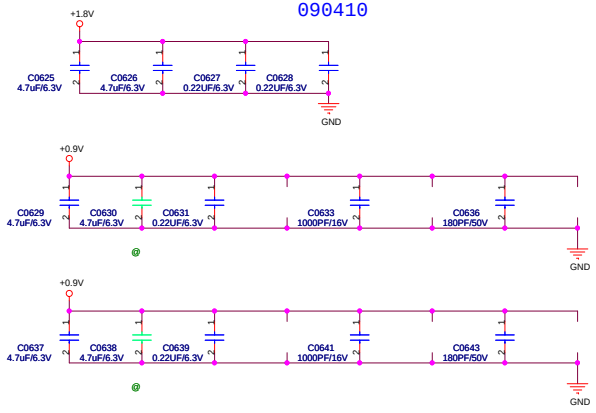


Remove C0602, C0603, C0604 090406

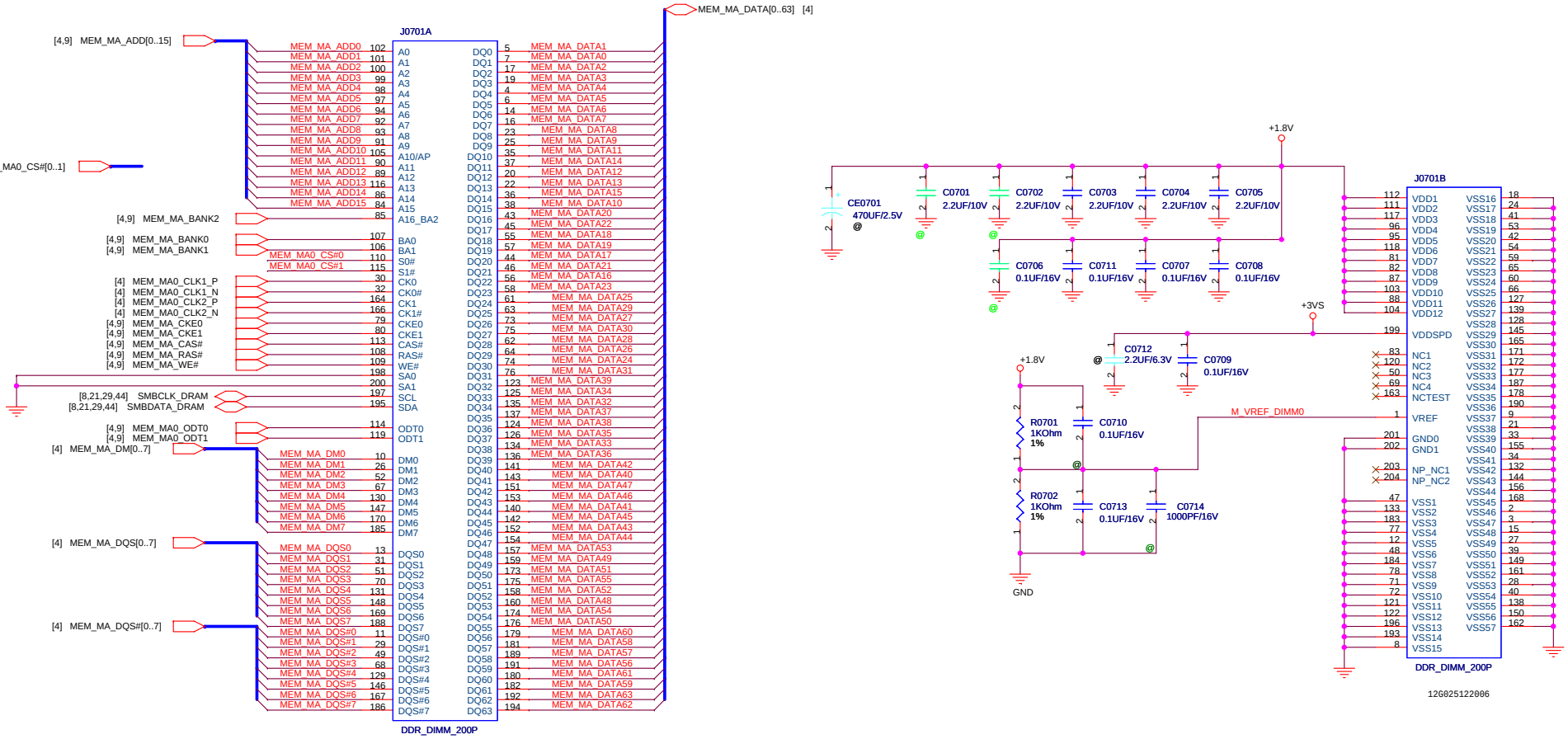


LAYOUT NOTE: Decoupling between CPU and DIMMs,
Place close to CPU as possible

NOTICE 1,8v cap placement
090410



ASUSTeK.Computer.INC	Title : Conesus Power	
	Engineer: <OrgAddr1>	
Size: C	Project Name: F83	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 6 of 91	



P/N:12G025122006

<Variant Name>

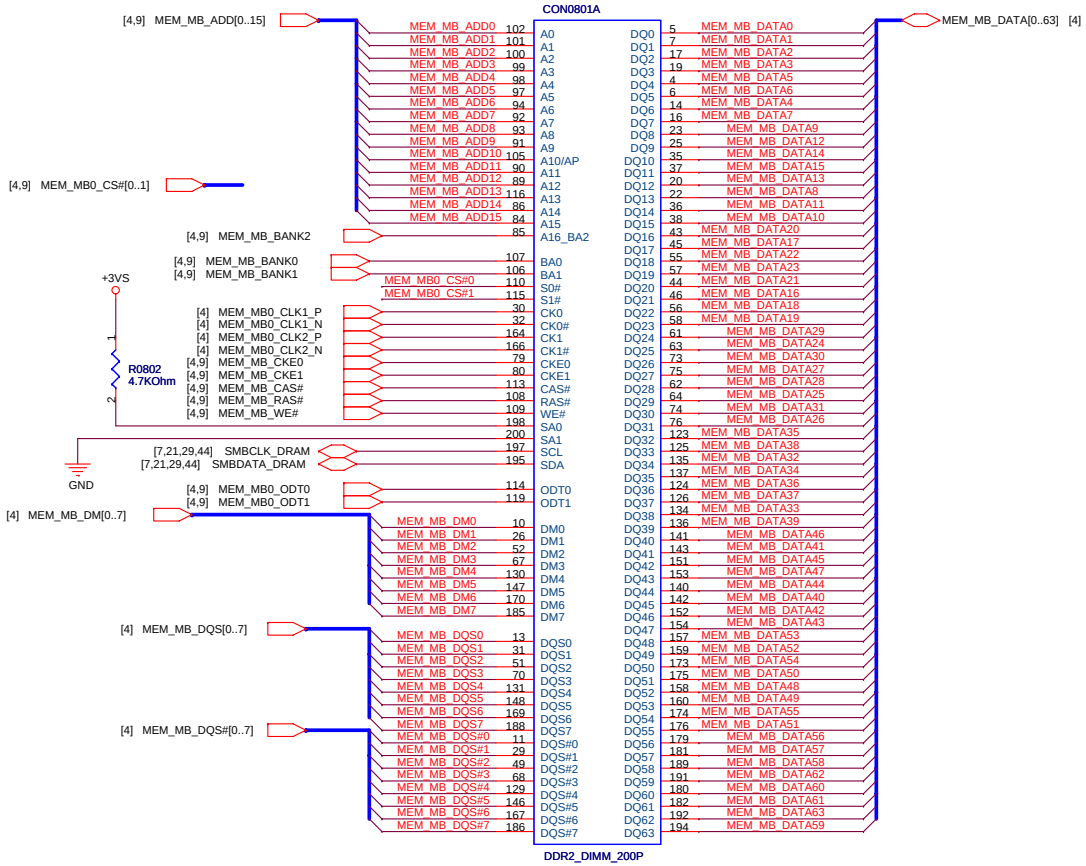
ASUSTeK COMPUTER INC

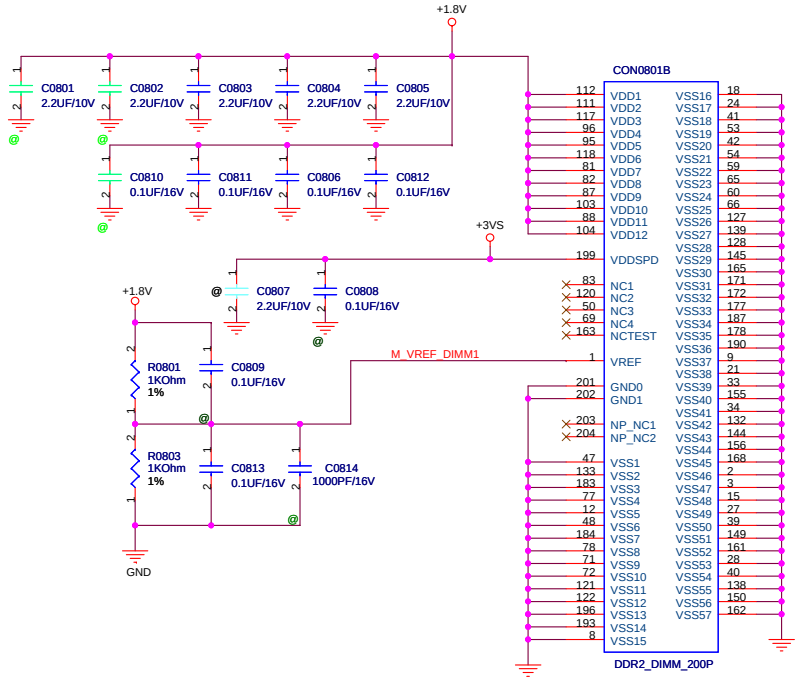
Title : DDR2 SO-DIMM0

Engineer:

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 7 of 91





PN:12G025C22003
REV.

ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM1		
	Engineer:		
Size: Custom	Project Name: F83T		Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 8 of 91		

change to 8R16P 090405

[4,7] MEM_MA_ADD[0..15]

071219
Del Bank2 to Bus

MEM_MA_ADD1 — 47OHM — RN0901C
MEM_MA_ADD3 — 47OHM — RN0901B
MEM_MA_ADD5 — 47OHM — RN0901A
MEM_MA_ADD8 — 47OHM — RN0903H
MEM_MA0_CS#1 — 47OHM — RN0901G
MEM_MA_CAS# — 47OHM — RN0901H
MEM_MA_WE# — 47OHM — RN0901E
MEM_MA_ADD9 — 47OHM — RN0903C
MEM_MA_ADD12 — 47OHM — RN0903D
MEM_MA_BANK2 — 47OHM — RN0903E
MEM_MA_CKE0 — 47OHM — RN0903B
MEM_MA_ADD7 — 47OHM — RN0901D
MEM_MA_ADD14 — 47OHM — RN0903G
MEM_MA_ADD15 — 47OHM — RN0903F
MEM_MA_CKE1 — 47OHM — RN0903A
MEM_MA_RAS# — 47OHM — RN0901F
MEM_MA_BANK1 — 47OHM — RN0905D
MEM_MA_ADD4 — 47OHM — RN0905H
MEM_MA0_ODT0 — 47OHM — RN0905C
MEM_MA_ADD13 — 47OHM — RN0905A
MEM_MA0_CS#0 — 47OHM — RN0905B
MEM_MA_ADD2 — 47OHM — RN0905F
MEM_MA_ADD6 — 47OHM — RN0905G
MEM_MA_ADD0 — 47OHM — RN0905E
MEM_MA_ADD11 — 47Ohm — RN0909C
MEM_MA0_ODT1 — 47Ohm — RN0909D
MEM_MA_BANK0 — 47Ohm — RN0909A
MEM_MA_ADD10 — 47Ohm — RN0909B

+0.9V

C0901 0.1UF/16V +1.8V
C0902 0.1UF/16V +1.8V
C0903 0.1UF/16V +1.8V
C0912 0.1UF/16V +1.8V
C0913 0.1UF/16V +1.8V
C0914 0.1UF/16V +1.8V
C0915 0.1UF/16V +1.8V
C0916 0.1UF/16V +1.8V

是否用排容？
090330

Remove1.8V C0910,C0911 0.1uF 090405

+0.9V
C0904 0.1UF/16V
C0905 0.1UF/16V
C0906 0.1UF/16V
C0907 0.1UF/16V
C0908 0.1UF/16V
C0909 0.1UF/16V
GND

071207

[4,7] MEM_MA_BANK2 — MEM_MA_BANK2
[4,7] MEM_MA_BANK1 — MEM_MA_BANK1
[4,7] MEM_MA_BANK0 — MEM_MA_BANK0
[4,7] MEM_MA0_ODT0 — MEM_MA0_ODT0
[4,7] MEM_MA0_ODT1 — MEM_MA0_ODT1
[4,7] MEM_MA_CKE0 — MEM_MA_CKE0
[4,7] MEM_MA_CKE1 — MEM_MA_CKE1
[4,7] MEM_MA_RAS# — MEM_MA_RAS#
[4,7] MEM_MA_CAS# — MEM_MA_CAS#
[4,7] MEM_MA_WE# — MEM_MA_WE#
[4,7] MEM_MA0_CS#0 — MEM_MA0_CS#0
[4,7] MEM_MA0_CS#1 — MEM_MA0_CS#1

add MA0_ODT1省MB0_ODT1
090417

change to 8R16P 090405

[4,8] MEM_MB_ADD[0..15]

MEM_MB_ADD14 — 47OHM — RN0912F
MEM_MB_ADD7 — 47OHM — RN0912A
MEM_MB_ADD11 — 47OHM — RN0912E
MEM_MB_ADD12 — 47OHM — RN0912B
MEM_MB_ADD10 — 47OHM — RN0910E
MEM_MB_ADD0 — 47OHM — RN0910G
MEM_MB0_ODT0 — 47OHM — RN0910A
MEM_MB_ADD13 — 47OHM — RN0910B
MEM_MB_RAS# — 47OHM — RN0910D
MEM_MB0_CS#0 — 47OHM — RN0910C
MEM_MB_ADD1 — 47OHM — RN0912E
MEM_MB_ADD2 — 47OHM — RN0910H
MEM_MB_ADD15 — 47OHM — RN0912G
MEM_MB_CKE1 — 47OHM — RN0912H
MEM_MB_BANK2 — 47OHM — RN0912C
MEM_MB_CKE0 — 47OHM — RN0912D
MEM_MB0_CS#1 — 47OHM — RN0914H
MEM_MB_CAS# — 47OHM — RN0914G
MEM_MB_ADD8 — 47OHM — RN0914A
MEM_MB_ADD3 — 47OHM — RN0914D
MEM_MB_ADD6 — 47OHM — RN0914C
MEM_MB_WE# — 47OHM — RN0914F
MEM_MB_BANK0 — 47OHM — RN0910F
MEM_MB_ADD4 — 47OHM — RN0914B
MEM_MB_ADD9 — 47Ohm — RN0916D
MEM_MB0_ODT1 — 47Ohm — RN0916B
MEM_MB_ADD5 — 47Ohm — RN0916C
MEM_MB_BANK1 — 47Ohm — RN0916A

+0.9V

C0917 0.1UF/16V +1.8V
C0918 0.1UF/16V +1.8V
C0919 0.1UF/16V +1.8V
C0927 0.1UF/16V +1.8V
C0929 0.1UF/16V +1.8V
C0930 0.1UF/16V +1.8V
C0931 0.1UF/16V +1.8V
C0932 0.1UF/16V +1.8V

Remove1.8V C0926,C0928 0.1uF 090405

+0.9V
C0920 0.1UF/16V
C0921 0.1UF/16V
C0922 0.1UF/16V
C0923 0.1UF/16V
C0924 0.1UF/16V
C0925 0.1UF/16V
GND

071211

[4,8] MEM_MB_BANK2 — MEM_MB_BANK2
[4,8] MEM_MB_BANK1 — MEM_MB_BANK1
[4,8] MEM_MB_BANK0 — MEM_MB_BANK0
[4,8] MEM_MB0_ODT0 — MEM_MB0_ODT0
[4,8] MEM_MB0_ODT1 — MEM_MB0_ODT1
[4,8] MEM_MB_CKE0 — MEM_MB_CKE0
[4,8] MEM_MB_CKE1 — MEM_MB_CKE1
[4,8] MEM_MB_RAS# — MEM_MB_RAS#
[4,8] MEM_MB_CAS# — MEM_MB_CAS#
[4,8] MEM_MB_WE# — MEM_MB_WE#
[4,8] MEM_MB0_CS#0 — MEM_MB0_CS#0
[4,8] MEM_MB0_CS#1 — MEM_MB0_CS#1

add MA0_ODT1省MB0_ODT1
090417

+1.8V
C0933 0.1UF/16V
C0934 0.1UF/16V
C0935 0.1UF/16V
C0936 0.1UF/16V
C0937 0.1UF/16V
C0938 0.1UF/16V
GND

PLACE CLOSE TO SOCKET(PER EMI/EMC)

ASUSTeK COMPUTER INC

Title : DDR2_TERMINATIONS

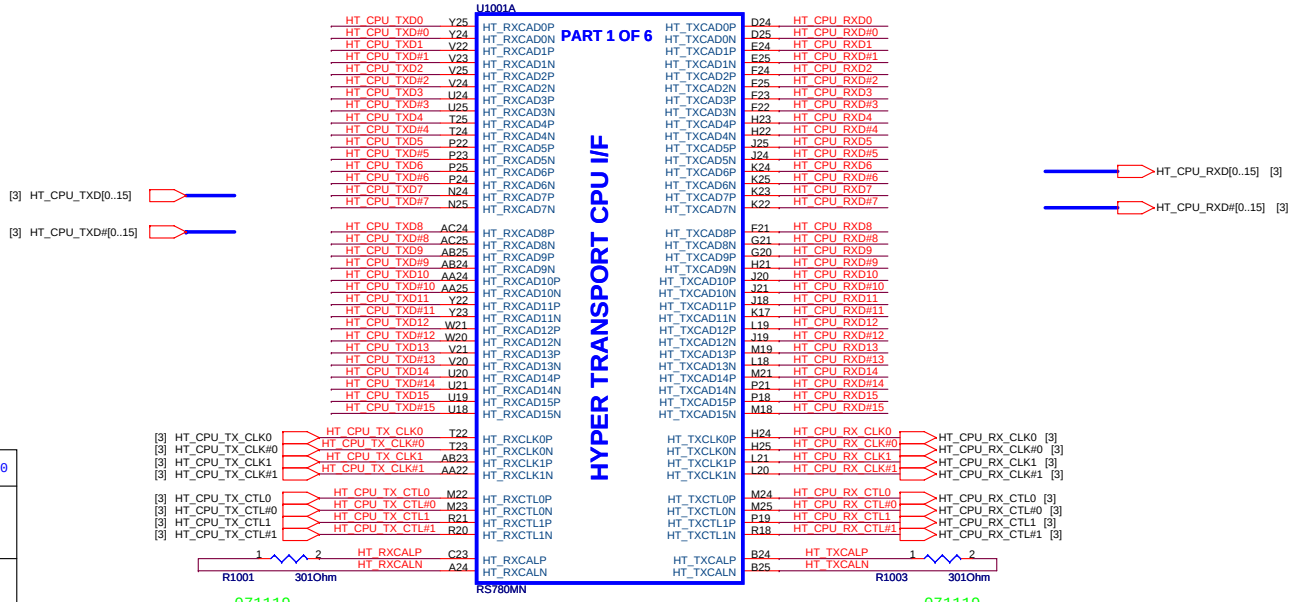
Engineer:

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 9 of 91

R1.11 080319

Change the NB Part number to RS780 (A13)



Signal	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP HT_TXCALN	100R	1.21K	301R

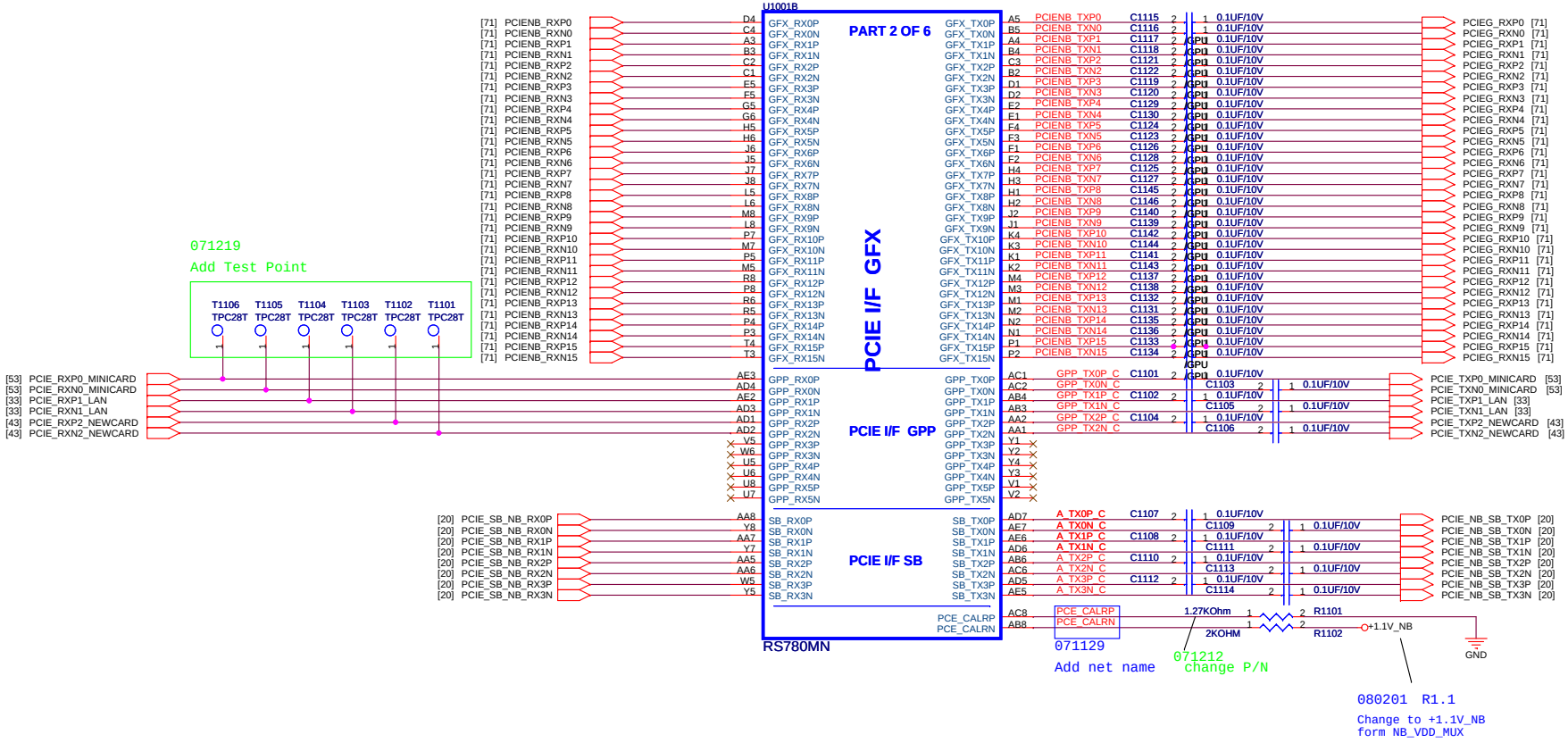
071119
change R1001 value

071119
change R1003 value

ASUSTeK.COMPUTER.INC	Title : RS780M-HT LINK I/F		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: F5Z		Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 10 of 91		

R1.11 080319

Change the NB Part number to RS780 (A13)



ASUSTeK.Computer.INC	Title : RS780M-PCIE LINK I/F	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: F5Z	Rev: 2.05
Date: Friday, May 29, 2009	Sheet 11 of 91	

notice L1201 L1204 change SL?
090411

U1001C
PART 3 OF 6
RS780MN

CRT/TVOUT
PLL PWR
LVTM
PM
CLOCKs
MIS.

080201 R1.1
Change to +1.1V_NB
form NB_VDD_MUX

071219
For Layout impdance setting

090407

R1.11
080310

R2.0080401
Change NB_ALLOW_LDTSTOP to ALLOW_LDTSTOP

STRP_DATA	0	1
VCC_NB	1.0V	1.1V

Notice RN1215 remove ?
090411

071115

090316
change backlight control by M92

071207

remove D1201 circuit
090410

071116

R1.11
080319
Change the NB Part number to RS780 (A13)

080325
R2.0 Remove Q1201A and R1219

071218
for measurement near U1001

071204
DEL serial R

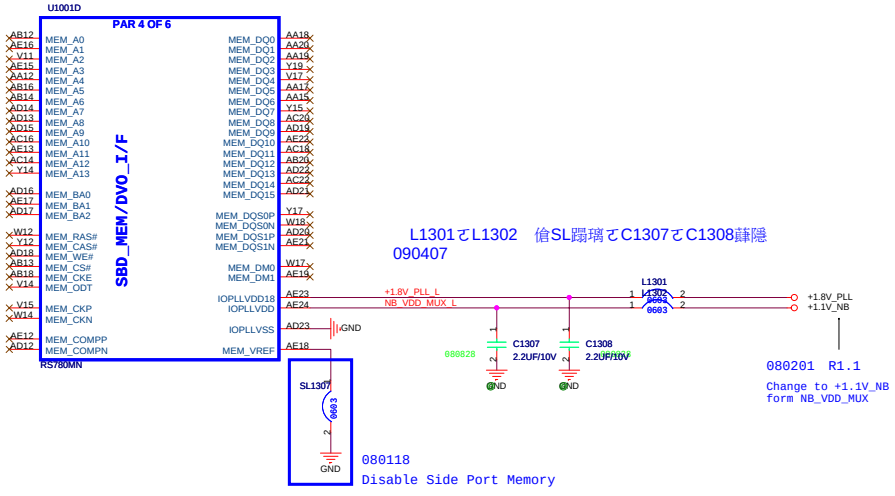
?? for external graphic

have via for measurement

Title :	RS780M-SYS I/F
ASUSTeK.Computer.INC	Engineer: <OrgAddr1>
Size: C	Project Name: F5Z
Rev: 2.05	
Date: Tuesday, May 26, 2009	Sheet 12 of 91

R1.11 080319

Change the NB Part number to RS780 (A13)



L1301ぞL1302　倍SL蹋璃ぞC1307ぞC1308蘚隠

090407

080201 R1.1

Change to +1.1V_NB form NB_VDD_MUX

080118

Disable Side Port Memory

R1.1

DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS780:SUS_STAT
```

STRAP_DEBUG_BUS_PCIE_ENABLE

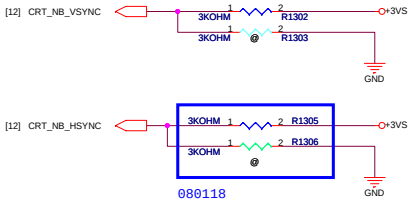
```
Enables the Test Debug Bus using PCIE bus:
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable


RS780: configurable thru register setting only
```

RS740/RS780: Enables Side port memory

```
RS780:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]
```

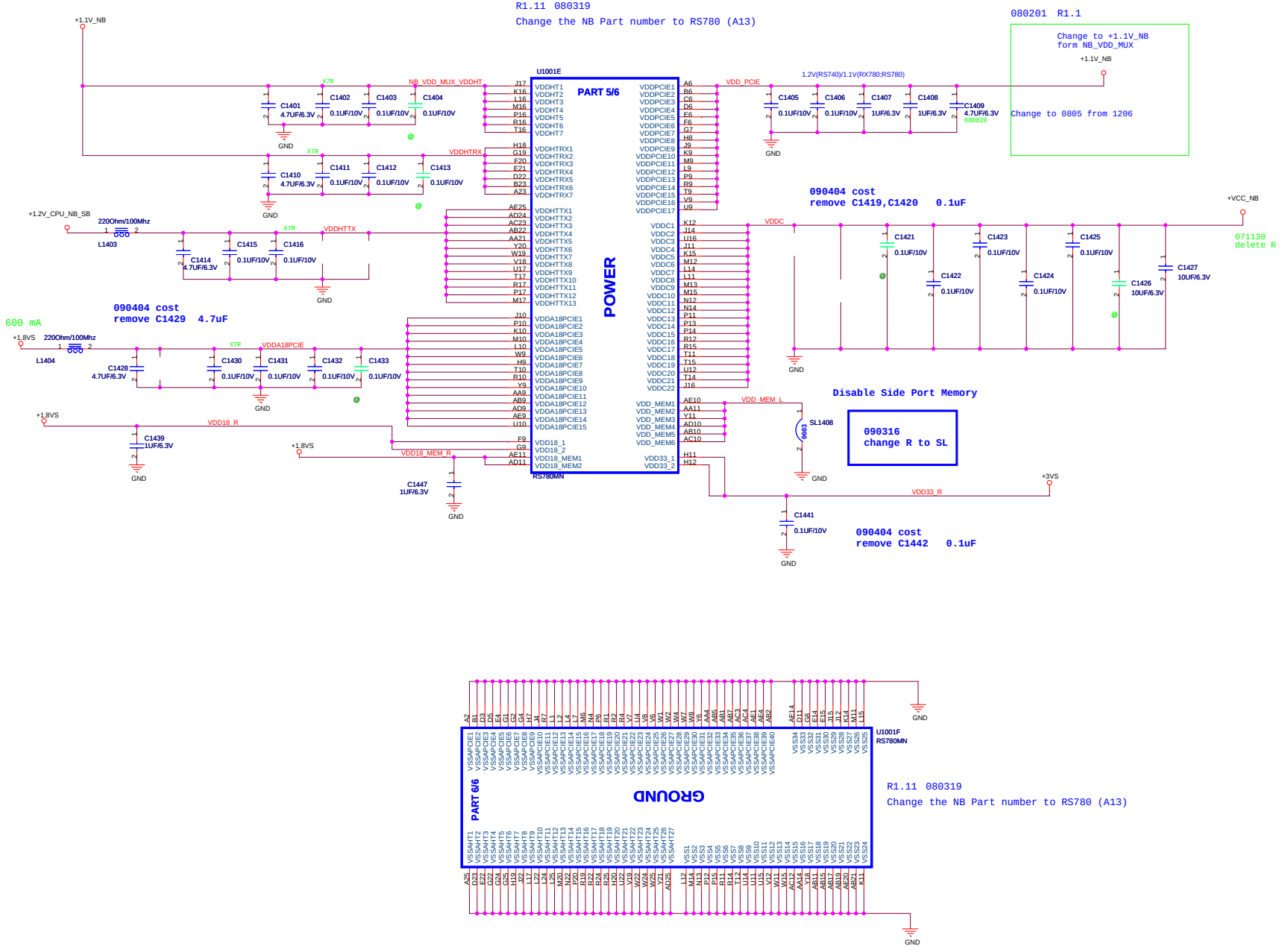


080118

Disable Side Port Memory

R1.1

ASUSTeK.Computer.INC	Title : RS780M-SPMEM/STRAP	
	Engineer: <OrgAddr1>	
Size: C	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 13 of 91	


R1.11 080319
Change the NB Part number to RS780 (A13)
080201 R1.1
Change to +1.1V_NB form NB_VDD_MUX
Change to 0805 from 1206
090404 cost remove C1419,C1420 0.1uF
090404 cost remove C1429 4.7uF
600 mA
Disable Side Port Memory
090316 change R to SL
090404 cost remove C1442 0.1uF
071130 delete R
U1001E
PART 5/6
POWER
RS780MN
U1001F
PART 6/6
GROUND
RS780MN
R1.11 080319
Change the NB Part number to RS780 (A13)
Title : RS780M-POWER
ASUSTeK.Computer.INC
Engineer: <OrgAddr1>
Size C
Project Name F5Z
Rev 2.05
Date: Tuesday, May 26, 2009
Sheet 14 of 91

ASUSTeK COMPUTER INC. NB1	Title : Engineer: <OrgAddr1>	
Size: A	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 15 of 91	

ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: <OrgAddr1>	
Size: A	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 16 of 91	

ASUSTeK COMPUTER INC. NB1	Title : Engineer: <OrgAddr1>	
Size: A	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 17 of 91	

ASUSTeK COMPUTER INC. NB1	Title :		
	Engineer: <OrgAddr1>		
Size: A	Project Name: F5Z		Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 18 of 91		

ASUSTeK COMPUTER INC. NB1	Title : Engineer: <OrgAddr1>	
Size: A	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 19 of 91	

R2.0 080327
Add test point for factory
ICT test

R1.11 080319
Change the SB Part number to SB700 (A12)

071120
add net name

071204
AMD review

080130 R1.1
Change TPM CLK

SB700
Part 1 of 5

PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC

071212
change P/N

090403
Correct to R1.1

071121

080212
R1.1
Del T2052~T2074 for
GND Via improvement

080212
R1.1
Del T2017~T2033 for
GND Via improvement

080218 R1.1
Add Test Point

Reserved Via

internal Pull Up 15K

internal Pull Up 8.2K

標注

071218
for measurement
near U2001
del R2007,R2011

Add net SB_OSC
090326

071207
AMD
review

071119
STRAP

EMI
090414

R2.0 080327
Add test point for factory
ICT test

change C2015,C2016 to 22pF 090407

做BOM時要更換成SB710的料號:02G050003001
090406

R2.02 080519
Un-Mount D2001 and Mount R2035.
080526
Change R2035 P/N form 10G212000004030 to 10G212000004070 for ECN requirement

R1.11
Change the P/N of BAT2001 from
12G201100203 to 12G201100208

change ctystal (SB710) 07G010413277
090331

Title :	SB700_CPU/PCIE/LPC/CLK
ASUSTeK.COMputer.INC	Engineer: <OrgAddr1>
Size: C	Project Name: F5Z
Rev: 2.05	
Date: Tuesday, May 26, 2009	Sheet 20 of 91

R1.11 080319
Change the SB Part number to SB700 (A12)

071129
Add net name

USB [3:0] ->USB PORT
USB 4 -> NEW CARD
USB 6 -> CAMERA
USB 10 -> CARDREADER
USB 12 -> BT Module

SB700 Part 4 of 5

Fingerprint
Bluetooth
AU6433
CCD
NewCard
USB CONN

071207
RS780 POWERGOOD
is 1.8VS rail

071203
AMD review

S0 power

090404 cost

R2.0 080401
Add R2108 and R2113 for SMBCLK_NEWCARD and SMBDATA_NEWCARD.

080212 R1.1
Del T2115 and T2116 for GND Via improvement (GPIO44 and 46)

080218 R1.1
Add Test Point

internal P/U 8.2k

R2.01 080411
Change P/N to 10G212472004010

080215 R1.1
change 4.7K P/N from 10G212472004040 to 10G212472004010

R2.0 080402
Mount R2117 and un-monent R2118 for PCB ID

071120
res. value 10k -> 4.7k to get LOW level < Vih(1.8V)

071204 AMD review

PUT AT SB700 SIDE

Change 33ohm to 4R8P 090405

for strap

SB700A11 EC enable Strap Workaround

need to modify topology??

Title :	SB700_GPIO/USB/HD/ACPI
Engineer:	<OrgAddr1>
ASUSTeK.Computer.INC	
Size: C	Project Name: F5Z
Rev: 2.05	
Date: Tuesday, May 26, 2009	Sheet 21 of 91

R2.0 080331

Change the R2208, R2209 to C2218 and C2219.

Change the R2210, R2211 to C2220 and C2221.

071121 change add net name

R1.11 080319

Change the SB Part number to SB700 (A12)

U2001B

SB700

Part 2 of 5

SERIAL ATA

ATA 66/100/133

SPI ROM

HW MONITOR

SATA PWR

SB700

071119 add TP

remove tp 090416

GPIO54,GPIO57 可設成output low，R2204 & R2207可以Costdown 090405

071203

Place SATA_CAL RES very close to ball of SB700

071119 change P/N

071120 modify net name

071114

M51/X71 NO USE

071204

071127

080218 R1.1 Add Test Point

090404 cost

090403

Notice GPIO 54 090410

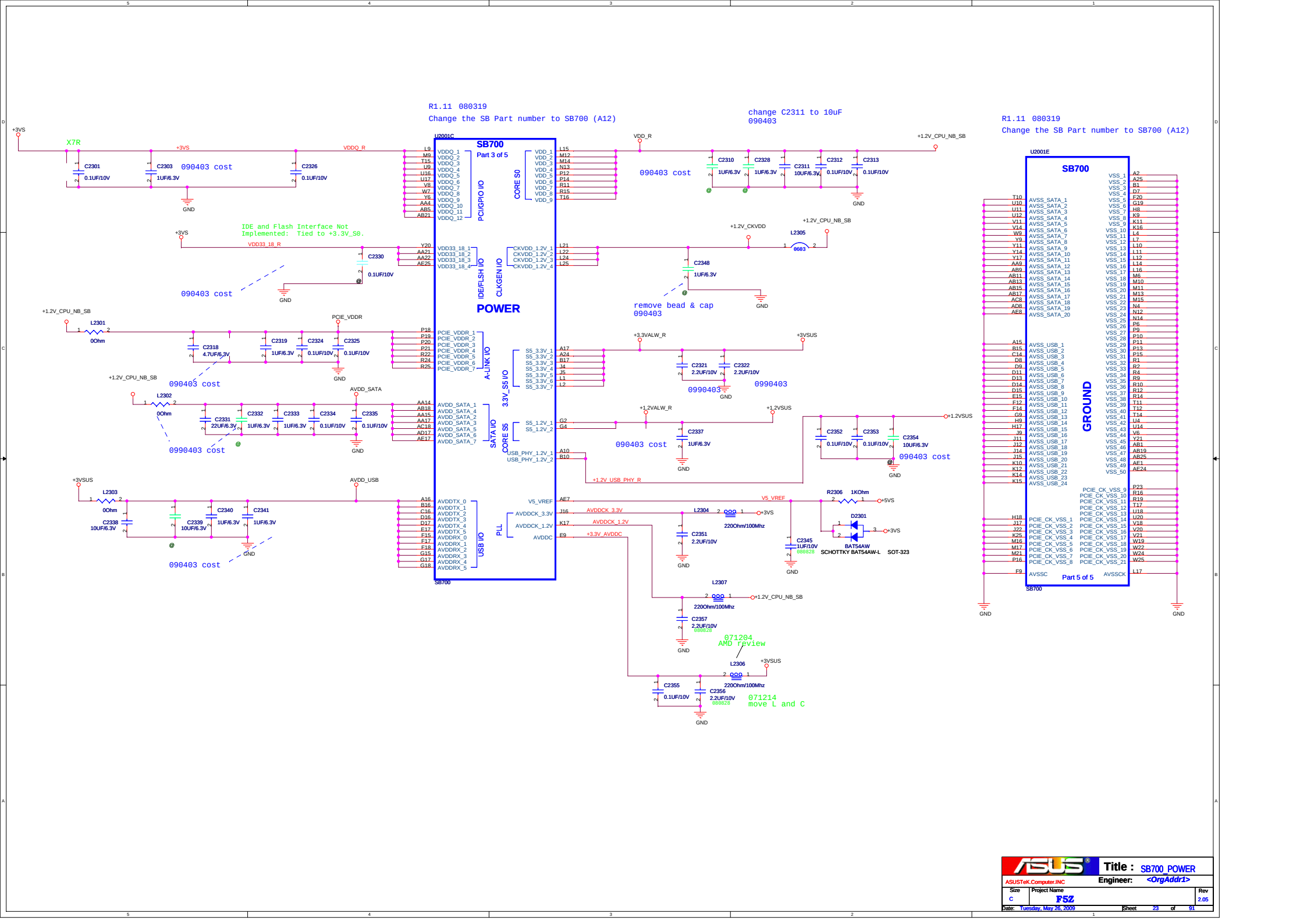
HWM not Implemented: Decoupling caps not used.

071119

GND trace at least 10mil wide

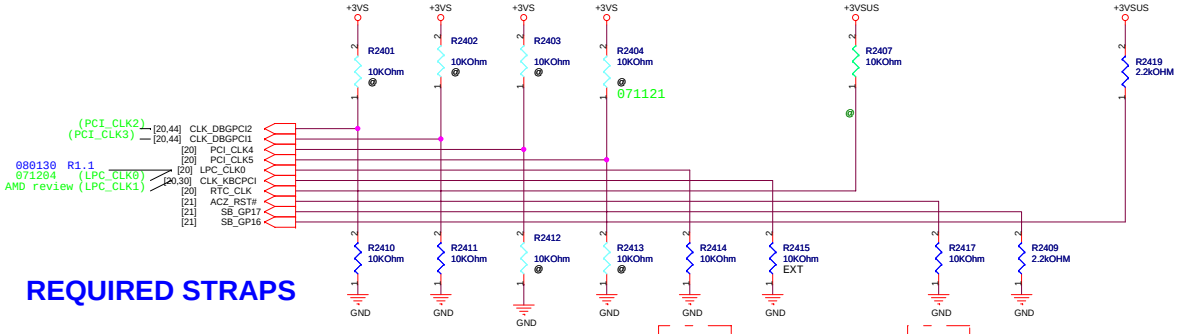
REMOVE C2216 090403

Title : SB700_PATA/SATA			
ASUSTeK.Computer.INC	Engineer: <OrgAddr1>		
Size: C	Project Name: F5Z		Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 22 of 91		


R1.11 080319
Change the SB Part number to SB700 (A12)
change C2311 to 10uF
090403
R1.11 080319
Change the SB Part number to SB700 (A12)
SB700
Part 3 of 5
POWER
GROUND
Part 5 of 5
IDE and Flash Interface Not Implemented: Tied to +3.3V_S0.
090403 cost
remove bead & cap
090403
0990403
071204
AMD review
071214
move L and C
Title : SB700_POWER
ASUSTeK.Computer.INC
Engineer: <OrgAddr1>
Project Name F5Z
Rev 2.05
Date: Tuesday, May 26, 2009
Sheet 23 of 91

Remove R2405, R2406,R2416
R2408, R2418, R2420, R2418 090405

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



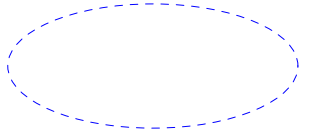
REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI MEM BOOT	H,H = Reserved H,L = SPI ROM L,H = LPC ROM (Default) L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT DEFAULT	

For SB700 A12 and later version

080204 R1.1
Change the Text Comment

Remove EEPROM 090405



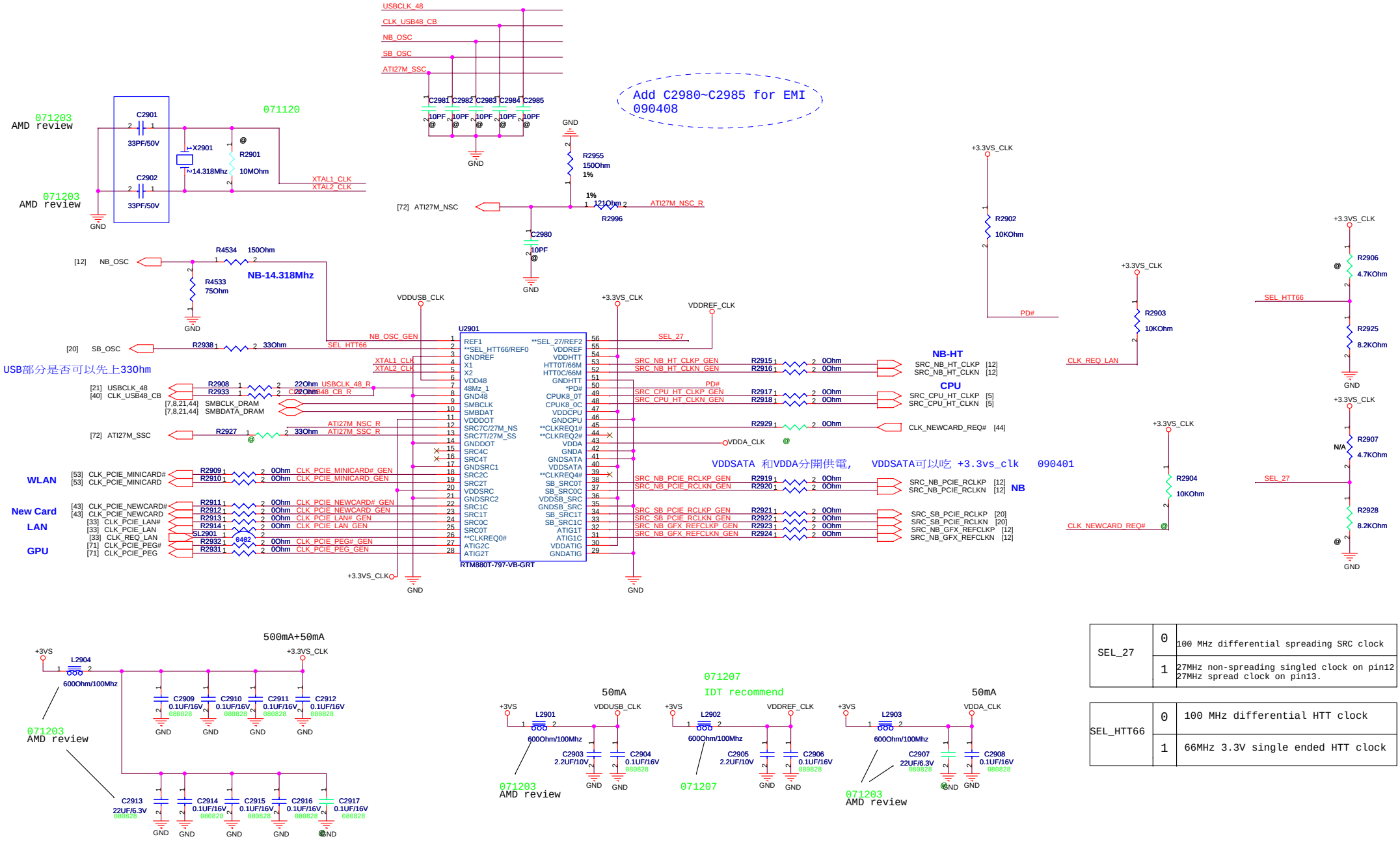
ASUSTeK.Computer.INC	Title : SB700_STRAP		
	Engineer: <OrgAddr1>		
Size: C	Project Name: F5Z		Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 24 of 91		

ASUSTeK COMPUTER INC. NB1	Title :
	Engineer: <OrgAddr1>
Size: A	Project Name: F5Z
Rev: 2.05	
Date: Tuesday, May 26, 2009	Sheet 25 of 91

ASUSTeK COMPUTER INC. NB1	Title : Engineer: <OrgAddr1>	
Size: A	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 26 of 91	

ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: <OrgAddr1>	
Size: A	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 27 of 91	

Title :	
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>
Size: A	Project Name: F5Z
Rev: 2.05	
Date: Tuesday, May 26, 2009	Sheet 28 of 91



SEL_27	0	100 MHz differential spreading SRC clock
	1	27MHz non-spreading singled clock on pin12 27MHz spread clock on pin13.

SEL_HTT66	0	100 MHz differential HTT clock
	1	66MHz 3.3V single ended HTT clock

<Variant Name>

ASUSTeK COMPUTER INC

Title : RTM880T-797-VB-GRT

Engineer: xinghua_chen

Size	Project Name	Rev
Custom	F83T	2.05

Date: Tuesday, May 26, 2009 Sheet 29 of 91

Notice EC FW 202
090410

change to 0 Ohm 090406

EC set those pins as OD type. Please check SB spec. wether it need 10K ohm pull-up resistor to +3VSUS or not.

For FW201 VOL_SEL is on GPB0 , For FW202 VOL_SEL is on GPG0.

1st : BLUETOOTH# (I) (GPF0)(10K ohm PU +3VS)
2nd : EMAIL# (I) (GPF0) (10K ohm PU +3VS)

1st : INTERNET# (I) (GPF1) (10K ohm PU +3VS)
2nd : WLAN# (I) (GPF1) (10K ohm PU +3VS)

ORIGINAL NAME : MARATHON#
If there is PWR4GEAR# button without optional EXP_GATE# function, please pull high it to +3VS. If there is the button combined the PWR4GEAR# and EXP_GATE# function, please pull high it to +3VA

Thermal sensor

If you use the IT8512JX (IT8502JX) and later version, please mount C3021 and un-mount R3052.Otherwise, please mount R3052 and un-mount C3021.

2nd: FAN1_PWM (Alt) (GPA2)
2nd : TP_LED (O) (GPA4)
2nd : KB_LED_PWM (O) (GPA6)
2nd : TP_LED_PWM (O) (GPA7)
For FW201 GPB0 is VOL_SEL. For FW202 GPB0 is BATSEL_0 and VOL_SEL is change to GPG0
2nd :SPLENDID# (I) (GPB2) (10K ohm PU +3VS)
ORIGINAL NAME :RFON_SW#
Please check RF_SW# that there is 10k ohm pull-up resistor to +3VA on p.p. 61 (BT & Side Switch)
Please check FAN0_TACH that there is 4.7k ohm pull-up resistor to +3VS on p.p. 50 (Thermal Sensor & FAN)
ORIGINAL NAME : COLOREN# (I) (GPE7) (10K ohm PU +3VS)
2nd : SD_CD_EC# (OD) (GPD7)
3rd : FAN1_TACH (Alt) (GPD7) (4.7K ohm PU +3VS)
EC set this pin as OD type. Please check SB spec. wether it need 10K ohm pull-up resistor to +3VS or not.
2nd : CRX1 (Alt) (GPH1)
For FW201 GPH2 is CTX1. For FW202 GPH2 is CHG_EN
It's used for NVidia Graphic IC thermal protection (internal thermal sensor)
Please check PM_PWROK that there are 10k ohm series resistor and pull-down on p.p.20~28 (SB_)
2nd : TP_LED (O) (GPJ4)
3rd : DRAM_THROTTLE# (O) (GPJ4)
2nd :WLAN_RST# (O) (GPJ5)

Backup PU or PD resistor

Note: If the PU or PD circuits have existed on the other page, please remove the PU or PD circuit here.

Fix for "Auto Power on" and "Data time error" Issue in Intel Platform

Note: If the schematic below has existed on pp.20~28 (SB_), please remove the circuit here.

To SB

For IT8512 Power

For PU / PD

Depend on SB required or not.

Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH8 GPIO.

For EC Reset

Note:
close to the WRST# (IT8512E pin14)

from Reset SW

For Instant Key

Note: Close to EC

Please check there are de-bounce cap near the switch, then un-mount the cap here.

If there is PWR4GEAR# button without optional EXP_GATE# function, please pull high it to +3VS.

For X'tal

Add 2nd source
07G010N23276
090331

Note:
Cload place close to EC
Cload can be fine tune , and EC need X'tal to within typical +/- 100 ppm

For EC Hardware Strap

I/O Base Address
Note: It can be programmable by EC fireware
Share Memory
Note: It can be programmable by EC fireware.
PP Enable
Note: Default Int. Pull-Low

(8Mb)

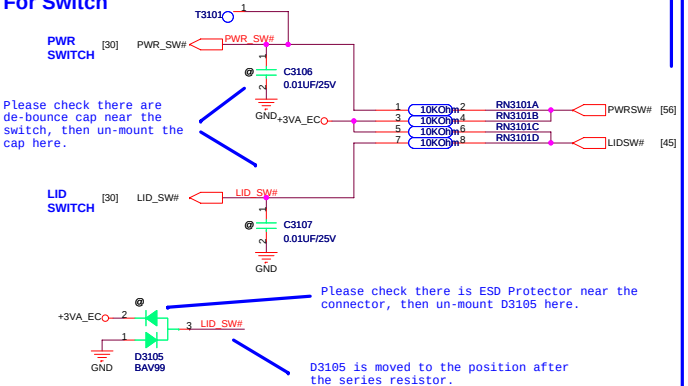
Title :	EC_IT8512 (1/2)		
ASUSTeK COMPUTER INC. NB1	Engineer:	<OrgAddr1>	
Size: Custom	Project Name: P5Z		Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 30 of 91		

For Battery

Note: If there is the same circuit on pp.60 (DC & BAT IN), please delete the circuit here

Remove D3101 part circuit
090409

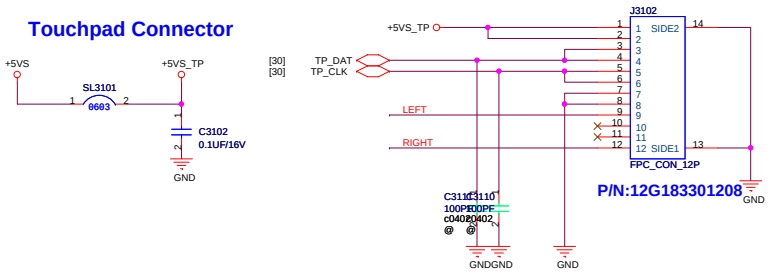
For Switch

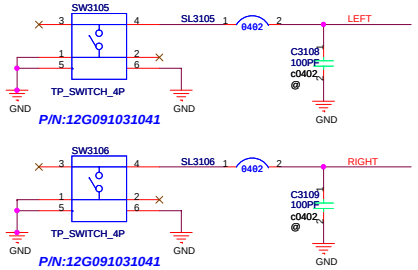


For Thermal Control Method

Note: Please follow the Thermal-Trip circuit on pp.3~6 (CPU_)

Touchpad Connector

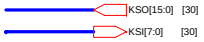




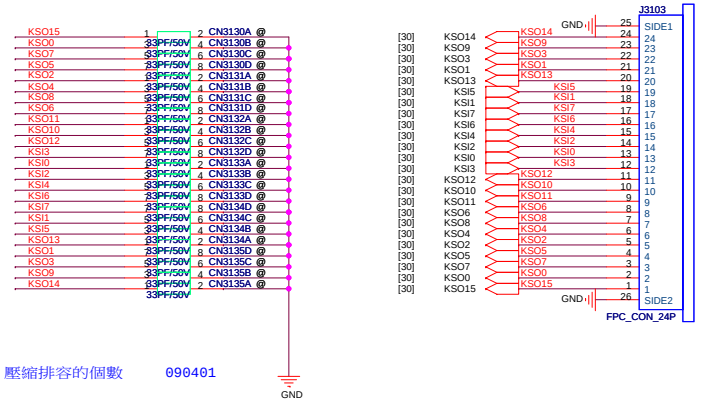
Notice switch P/N
090410

Keyboard Connector

Schematic below is noly the example in the previos project. It will be different between the different connector used in the Project.



Please follow the ASUS Keyboard Matrix Spec
Please Design based on your project.



壓縮排容的個數 090401

Remove all RST SCH and Change SW to other page

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F5Z	2.05

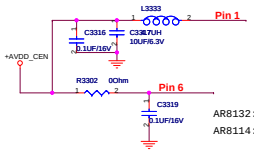
Date: Tuesday, May 26, 2009 Sheet 32 of 91

AR8132:Remove R3301,C3318
AR8114:Remove L3302,C3317,R3302

Pin 1 pin 6 1.7V

P/N:09G02X473Z05

C3318 close to Pin 1



AR8132:C3319=0.1uF

AR8114:C3319=1uF

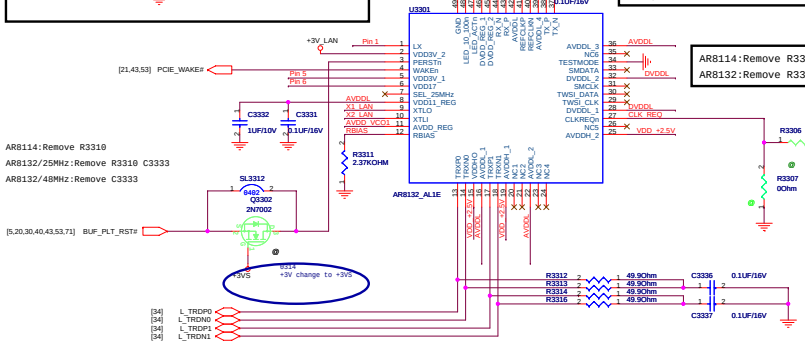
AR8132 with overclock: Remove R3315

AR8114:Remove R3315

Ground pad要打散熱孔

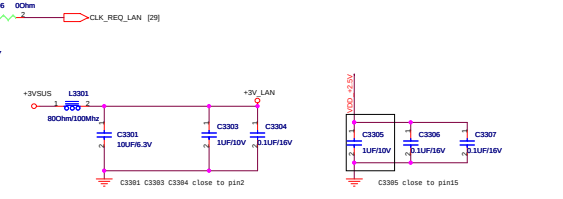
PCIE Tx,Rx方向是以南橋為觀點

LAN pin Tx,Rx是以LAN為觀點



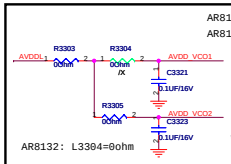
AR8114:Remove R3313

AR8132:Remove R3314



AR8132:Remove L3303

AR8132: C3321=0.1uF, Remove C3322



AR8132: L3304=0ohm

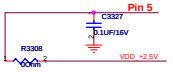
With overclock:Remove R3303

Not overclock:Remove R3304

For AR8132: Remove R3305,R3306,C3324,C3325,C3326,Q3301

For AR8114: Remove C3327 R3308

Q3301 close to Pin8

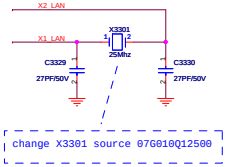


AR8114:Remove R3310

AR8132/25MHz:Remove R3310 C3333

AR8132/48MHz:Remove C3333

For AR8132 : Remove R3309

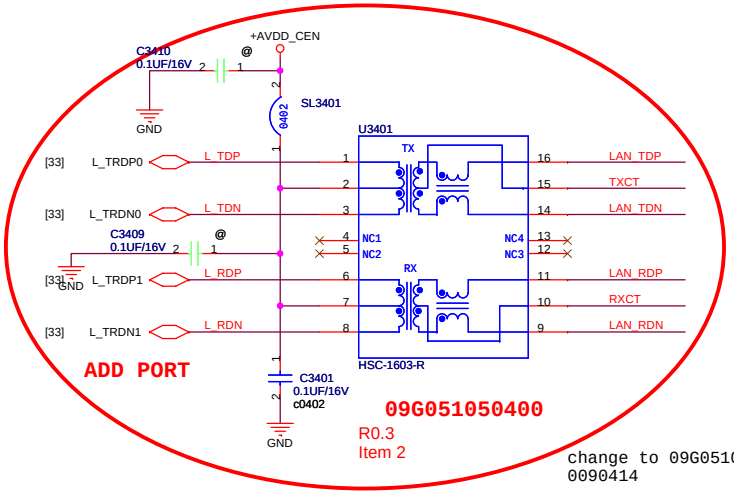


change X3301 source 07G010Q12500

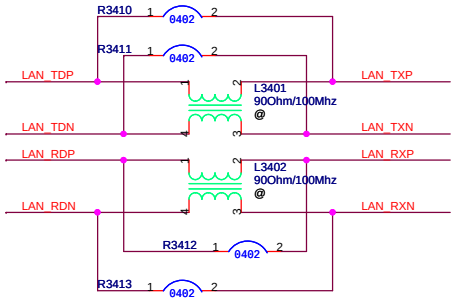
AR8114:Remove C3328

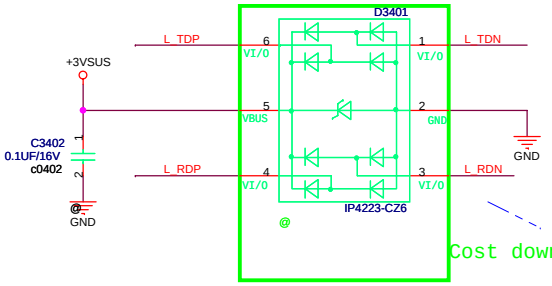
AR8132/25MHz: Remove C3328

AR8132/48MHz: Remove C3329 C3330 X3301



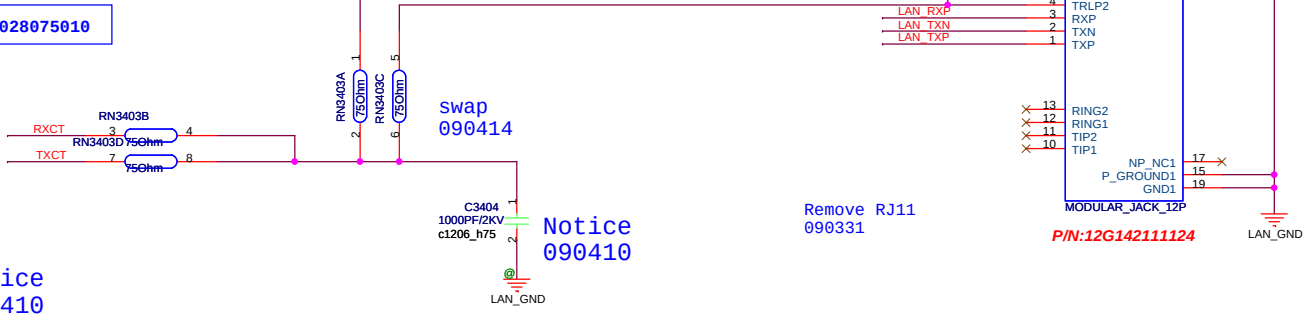
change to 09G0510010F9
0090414





Cost down
07G028075010

For RJ-45/RJ-11

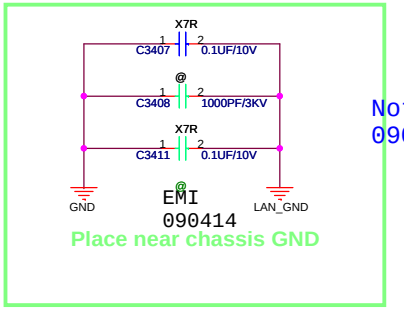


swap
090414

Notice
090410

Remove RJ11
090331

P/N:12G142111124



Notice
090410

<Variant Name>

Title : LAN-RJ45

ASUSTeK COMPUTER INC

Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Monday, June 01, 2009 Sheet 34 of 91

<Variant Name>

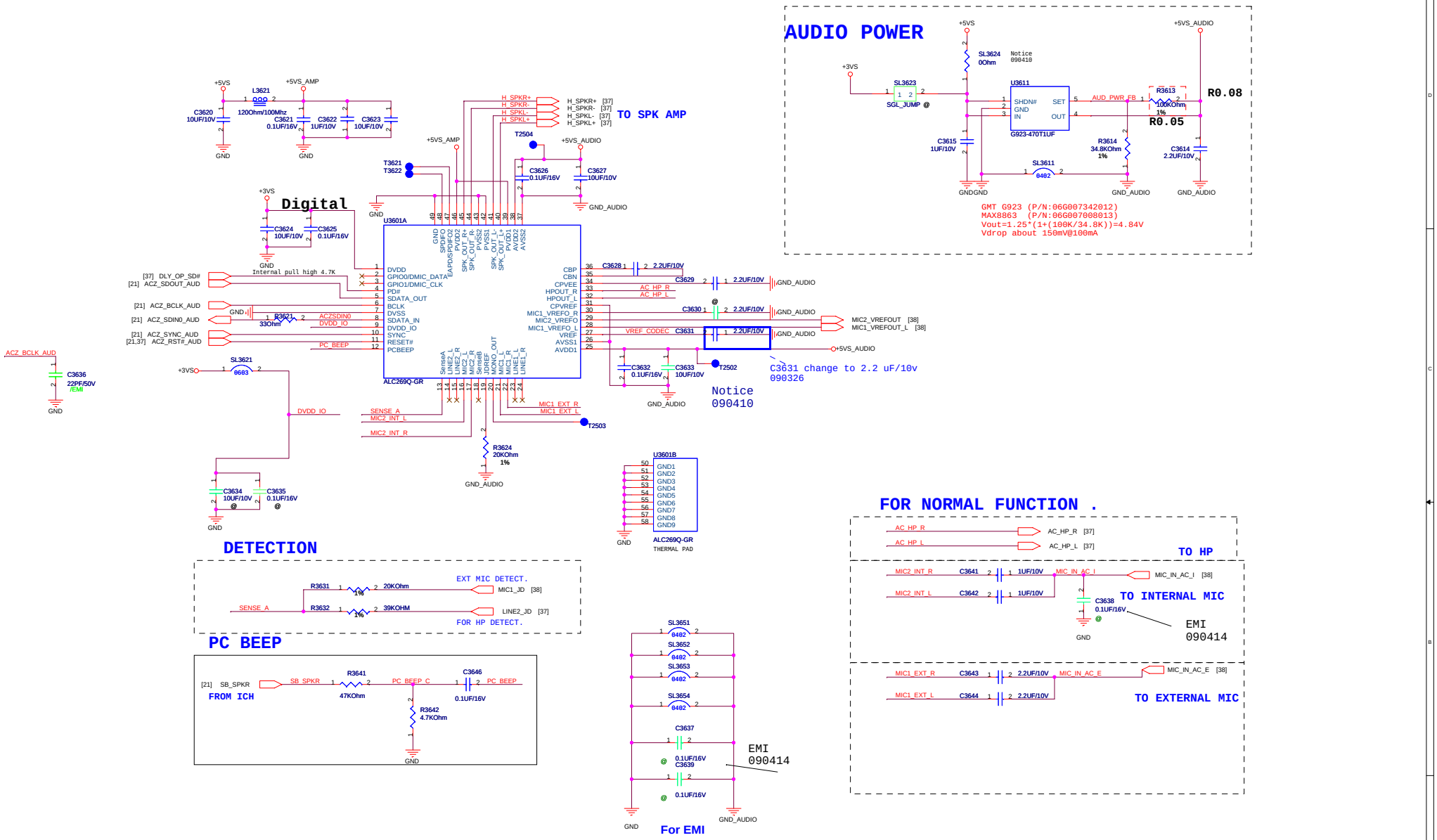
Title : LAN-MDC

ASUSTeK COMPUTER INC

Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 35 of 91



<Variant Name>

ASUSTeK COMPUTER INC.

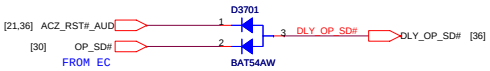
Title : CODEC-ALC662

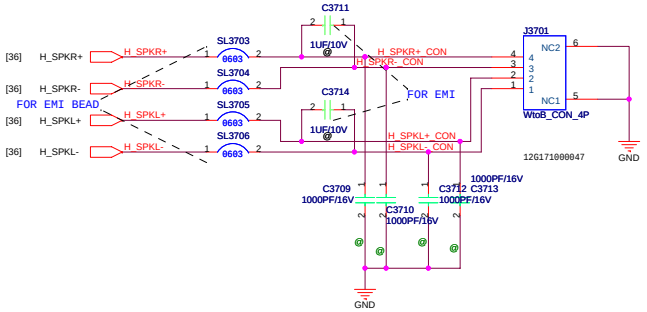
Engineer: Richard_Lu

Size	Project Name	Rev
C	F5Z	2.05

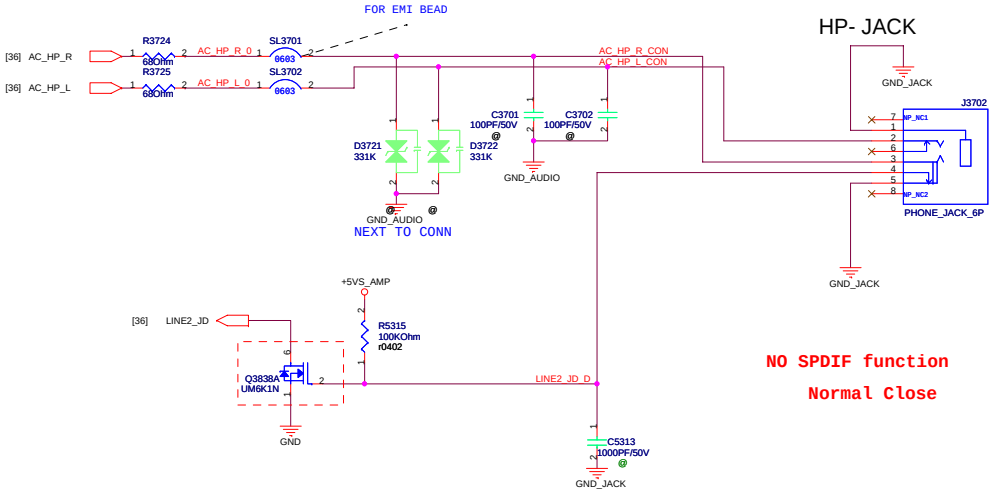
Date: Tuesday, May 26, 2009 Sheet 36 of 91

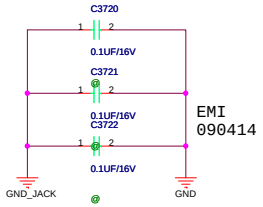
MUTE CONTROL





JACK_IN# or LINE2_JD depend on JACK's structure.
Suppose the fisrt pin should be contacted to GND while HP is plugged in.





EMI
090414

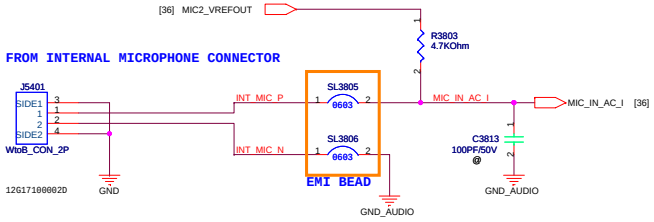
NO SPDIF function

Normal Close

<Variant Name>

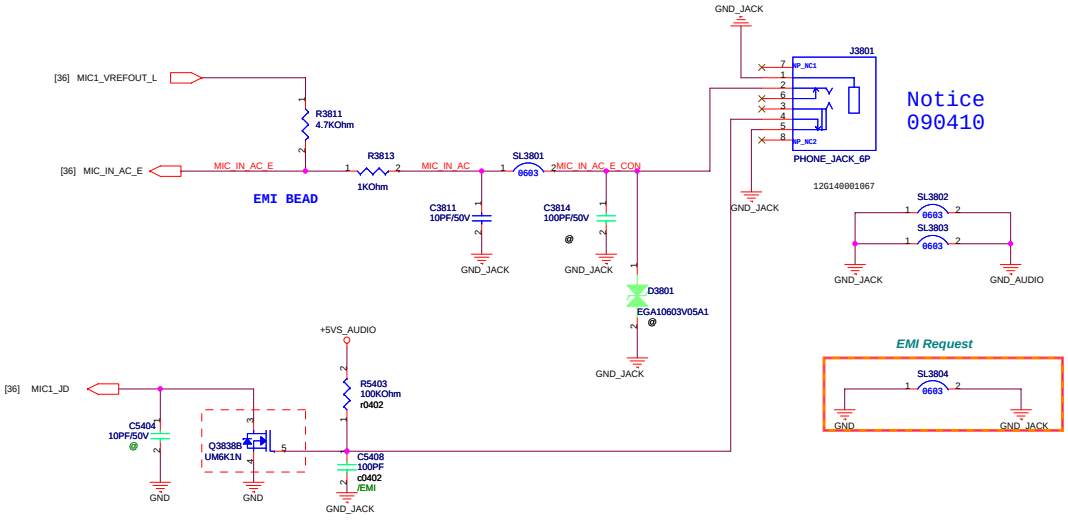
ASUSTeK COMPUTER INC	Title : AMP-GMT1431	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 37 of 91	

INTERNAL MICROPHONE



EXTERNAL MICROPHONE

Microphone In Jack



<Variant Name>

ASUSTeK COMPUTER INC.	Title : MIC-IN Jack	
	Engineer: Richard_Lu	
Size: C	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 38 of 91	

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard Lu

Size	Project Name	Rev
B	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 39 of 91

Add +3vs 081228

+3V +3VS +3V_CR R4018 0Ohm SL4001 0402 C4001 2.2UF/6.3V C4002 0.1UF/16V

AU6433-GLF:02G630001530
AU6433-GEF:02G630001521.
現在要求使用AU6433-GLF:02G630001530，
做bom以及線路要注意

Pin2 has internal pu 75K to +3V.

[5,20,30,33,43,53,71] BUF_PLT_RST# R4001 0Ohm C4019 0.1UF/16V +3V_CR R4003 0Ohm C4026 0.47UF/16V

[29] CLK_USB48_CB SL4004 0402 **Close to chip** R4005 33OOhm CR_REXT USB_PP10_DP USB_PN10_DM C4007 0.1UF/16V +1.8V_CR C4008 2.2UF/6.3V +3V_CARD C4010 2.2UF/6.3V +3V_CR CTRL4/XDRE/MSINS CTRL5/XDCD# CTRL6/XDCE# XDCIS/GLF_SDDAT2

U4001 AU6433D53-GLF-GR

1	EXT48IN	GND	29
2	CHIPRESETN	SDDATA1	28
3	REXT	CTRL1	27
4	VD33P	CTRL3	26
5	DP	DATA1	25
6	DM	DATA0	24
7	VS33P	DATA7	23
8	VDDU	DATA6	22
9	CF_V33	DATA5	21
10	V33	CTRL2	20
11	CTRL4	DATA4	19
12	XDCDN	DATA3	18
13	XDCEN	DATA2	17
14	SDDATA2	XDWPN	16
			15

CTRL1/SDWP/XDCLE/MSCLK CTRL3/SDCD#/XDWE# CR_DATA1 CR_DATA0 CR_DATA7 CR_DATA6 CTRL0/SDCLK/XDALE/MSBS CR_DATA5 CTRL2/SDCMD/XDR/B CR_DATA4 CR_DATA3 CR_DATA2 CTRL7/XDWP#

SD_DATA1_CON R4007 0Ohm R4006 0Ohm SD_CD#_EC [30] C4006 10PF/50V C4009 10PF/50V GND

CTRL0/SDCLK/XDALE/MSBS
CTRL1/SDWP/XDCLE/MSCLK
CTRL2/SDCMD/XDR/B
CTRL3/SDCD#/XDWE#
CTRL4/XDRE/MSINS
CTRL5/XDCD#
CTRL6/XDCE#
CTRL7/XDWP#

SL4003 0402 [21] USB_PP10 USB_PP10_DP
[21] USB_PN10 USB_PN10_DM
Remove Chock 2009/05/25
SL4002 0402

For AU6433 GLF : Stuff R4019(SL4008), Remove R4012,R4013

SD_DATA2_CON SL4008 0402 +3V_CR R4012 0Ohm XDCIS/GLF_SDDAT2 R4013 0Ohm GND

1:For check
0:For no check (Default)

P/N:12G340003814

C4021 0.1UF/10V +3V_CARD SL4007 0402 CTRL1/SDWP/XDCLE/MSCLK MS_CLK C4011 10PF/50V CR_DATA3 CTRL4/XDRE/MSINS CR_DATA2 CR_DATA0 CR_DATA1

+3V_CARD CTRL0/SDCLK/XDALE/MSBS SL4006 0402 CTRL0/SDCLK/XDALE/MSBS SD_CLK C4012 10PF/50V CR_DATA0 SD_DATA1_CON C4018 10PF/50V C4020 0.1UF/10V

J4001 CARD_READER_4SP

1	NP_NC2			dummy3	8
		dummy1	10		
		dummy2	9		
S9	DAT2			GND1	X1
S1	CD/DAT3			CD	X0
S2	CMD			R/-B	X2
S3	VSS1			-RE	X3
M10	VSS2			-CE	X4
M9	VCC1			CLE	X5
M8	SCLK			ALE	X6
M7	Reserved1			-WE	X7
M6	INS			-WP	X8
M5	Reserved2			GND2	X9
M4	SDIO			D0	X10
M3	VCC2			D1	X11
M2	BS			D2	X12
M1	VSS3			D3	X13
S4	VDD			D4	X14
S5	CLK			D5	X15
S6	VSS4			D6	X16
S7	DAT0	CD_SW	4	D7	X17
S8	DAT1	COMMON	5	VCC3	X18
		WP_SW	6		
2	NP_NC1	GND3	7	dummy4	

SD_DATA2_CON CR_DATA3 CTRL2/SDCMD/XDR/B CR_DATA0 CR_DATA1 CR_DATA2 CR_DATA3 CR_DATA4 CR_DATA5 CR_DATA6 CR_DATA7 CTRL5/XDCD# CTRL2/SDCMD/XDR/B CTRL4/XDRE/MSINS CTRL6/XDCE# CTRL1/SDWP/XDCLE/MSCLK CTRL0/SDCLK/XDALE/MSBS CTRL3/SDCD#/XDWE# CTRL7/XDWP#

C4013 1UF/10V GND +3V_CARD C4014 2.2UF/6.3V C4015 1UF/10V GND C4016 1UF/10V GND CTRL3/SDCD#/XDWE# CTRL1/SDWP/XDCLE/MSCLK C4017 1UF/10V GND

Fix MS Duo Adaptor short issue.
(SD_DAT1,SD_DAT2,XD_GND short,XD_CD# may be possible short)

For AU6433-GLF: No stuff All
For AU6433-GEF: Stuff Q4004,Q4005,Q4007,R4066.

R4016 0Ohm 2N7002K_T1_E3 Q4004 CR_DATA2 SD_DATA2_CON

IC side **CON side**

R4017 0Ohm 2N7002K_T1_E3 Q4005 CR_DATA1 SD_DATA1_CON

+12V R4066 100KOhm Q4007 2N7002K_T1_E3 CTRL3/SDCD#/XDWE# GND

<Variant Name>

ASUSTeK COMPUTER INC.

Title : CB_AU-6371_JEL

Engineer: Richard_Lu

Size	Project Name	Rev
C	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 40 of 91

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard Lu

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 41 of 91

<Variant Name>

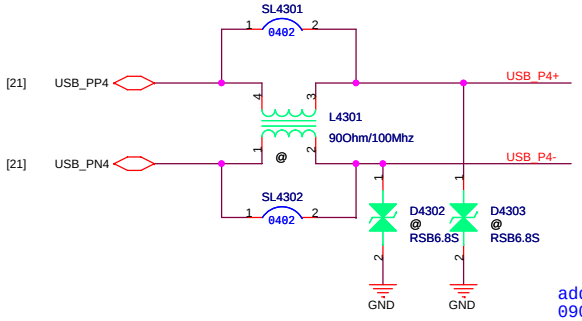
Title : *

ASUSTeK COMPUTER INC

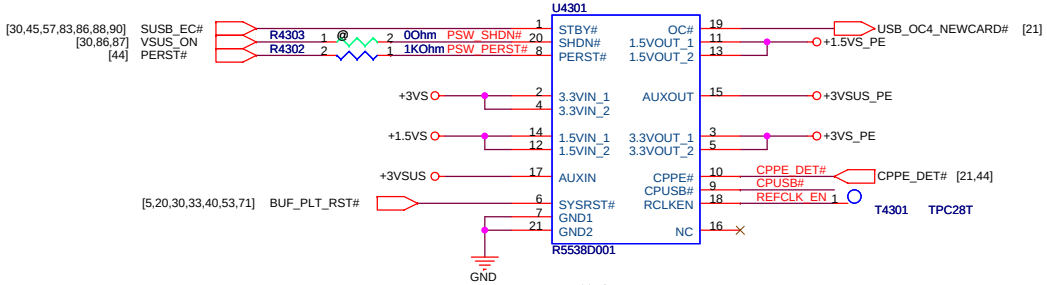
Engineer: Richard Lu

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 42 of 91



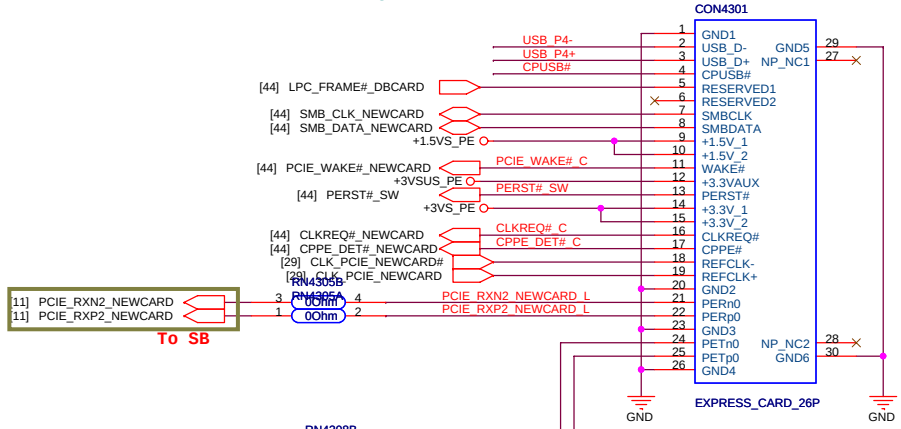
add RN4301, 預留L4301,
090331



換料

!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

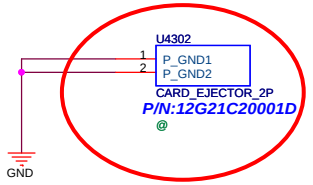
NewCard Header



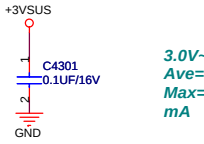
PN:12G161300261

R2.0 080402
Un-mount U4302 (Since it is not SMT component)

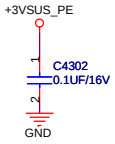
080216 R1.1
Add Resistor

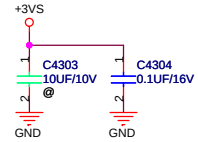


Remove U4302.
090406

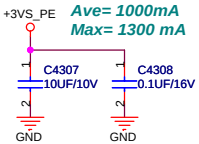


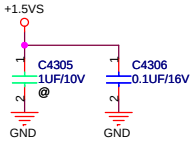
3.0V~3.6V
Ave= 200mA
Max= 275 mA



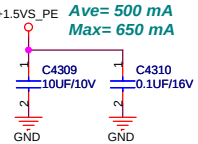


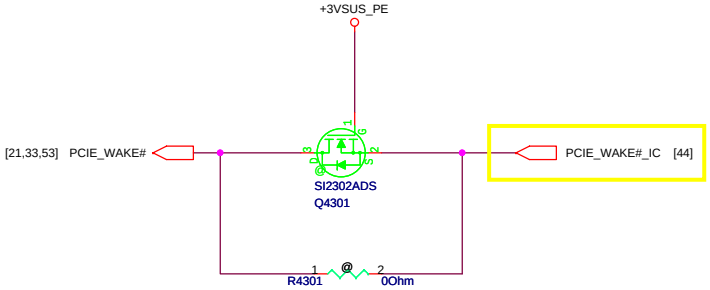
3.0V~3.6V
Ave= 1000mA
Max= 1300 mA





1.35V~1.65V
Ave= 500 mA
Max= 650 mA



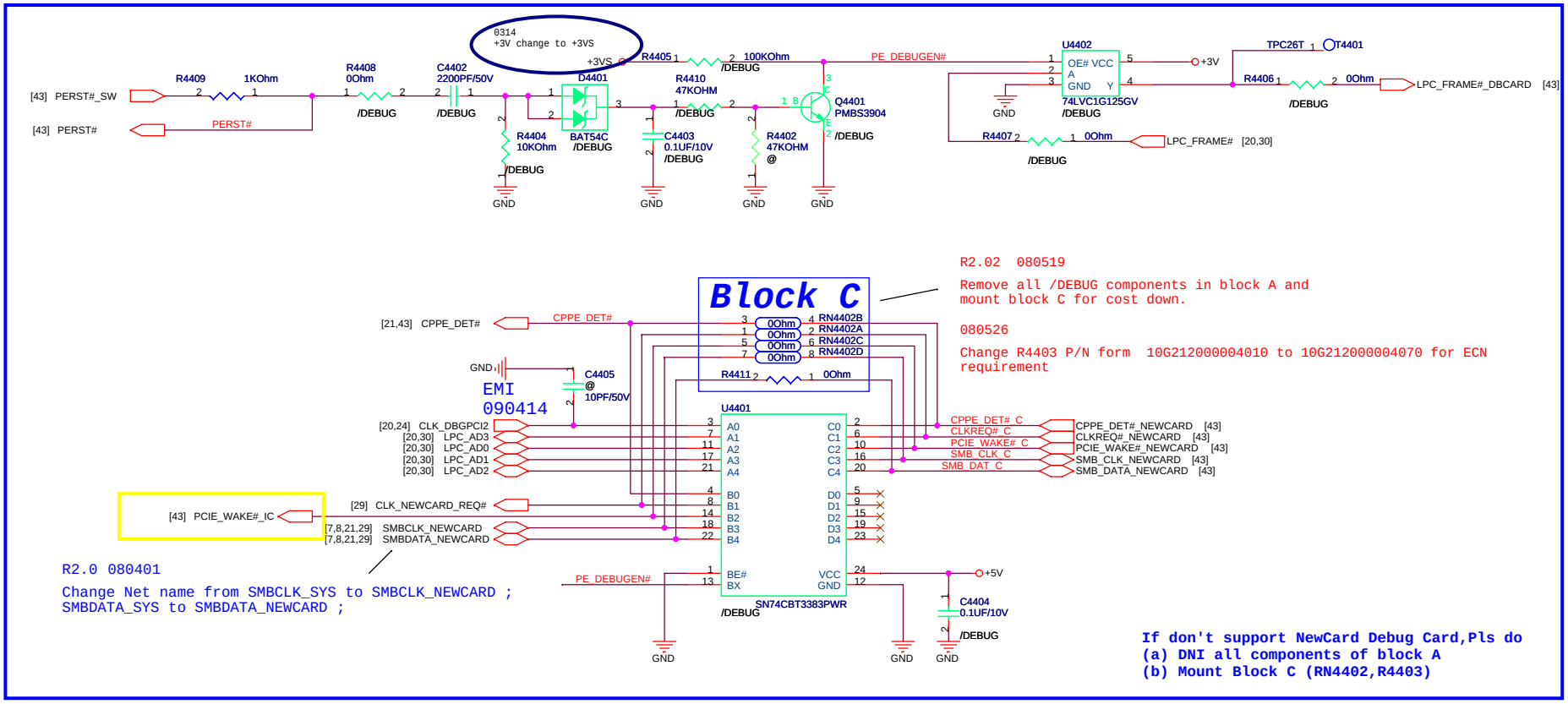


RemoveNew Card REFCLK_EN control part
090331

<Variant Name>

ASUSTeK COMPUTER INC	Title : NEWCARD	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 43 of 91	

Block A



R2.02 080519

Remove all /DEBUG components in block A and mount block C for cost down.

080526

Change R4403 P/N form 10G212000004010 to 10G212000004070 for ECN requirement

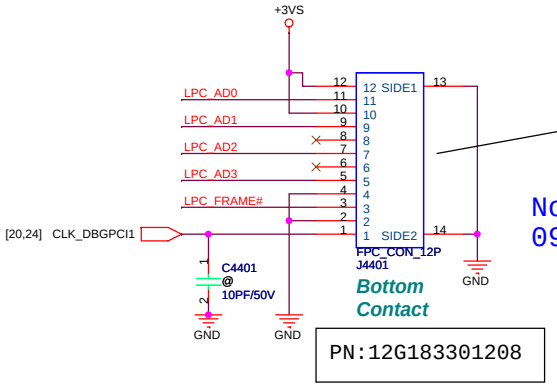
R2.0 080401

Change Net name from SMBCLK_SYS to SMBCLK_NEWCARD ; SMBDATA_SYS to SMBDATA_NEWCARD ;

If don't support NewCard Debug Card,Pls do
(a) DNI all components of block A
(b) Mount Block C (RN4402,R4403)

For PCMCIA Debug Card

If support NewCard Debug Card, Pls don't mount all components.



R2.04

Un-mount J4401 for cost down

Notice
090410

R2.05

Change RN4401 from 100ohm to 100pF capacitance. The capacitance with modification of RNX3001 is used to fix the LAD and SERIRQ signals coupling issue. However, the LPC debug board EEROM over-write function is not support now.

<Variant Name>

ASUSTeK COMPUTER INC

Title : DEBUG

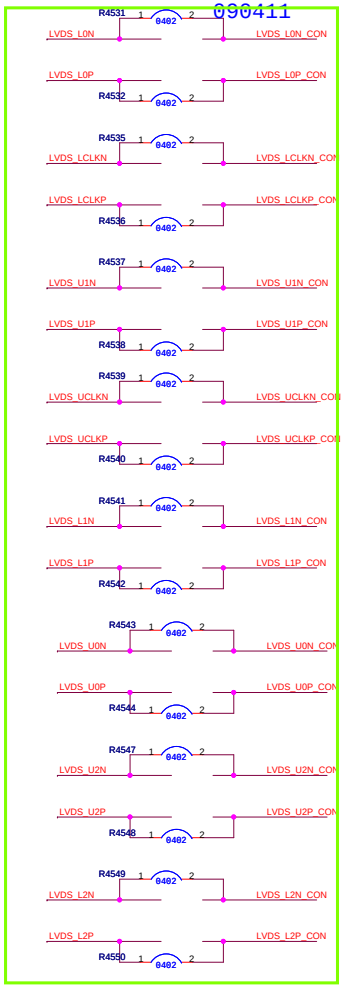
Engineer: Richard_Lu

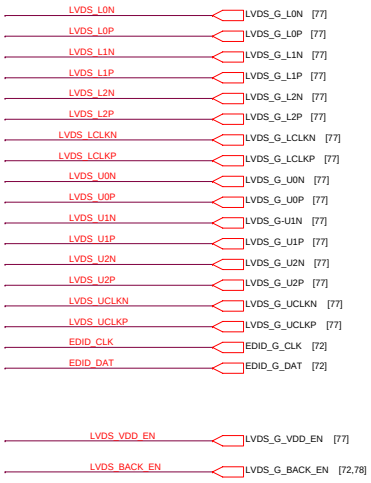
Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 44 of 91

layoutguide notic those SL colay with chock
090411

M92-M2

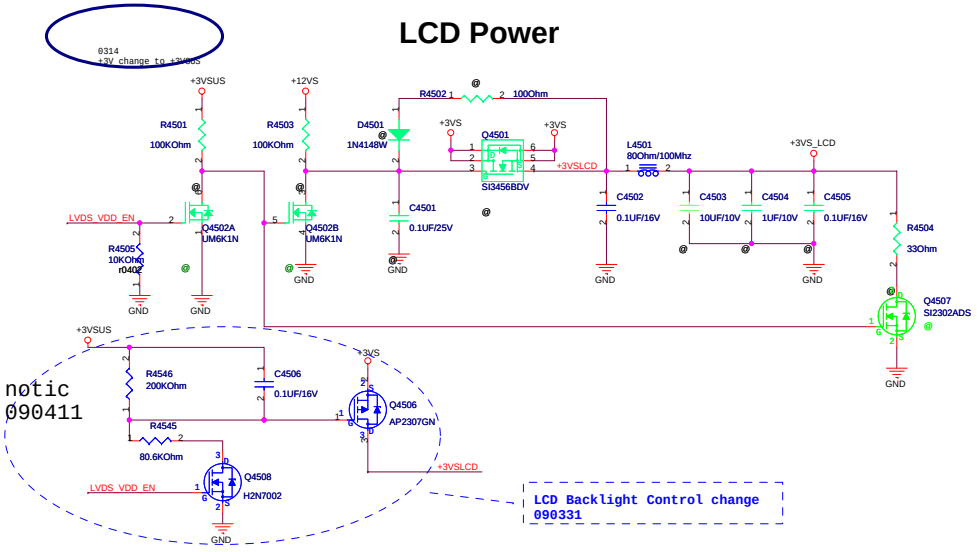




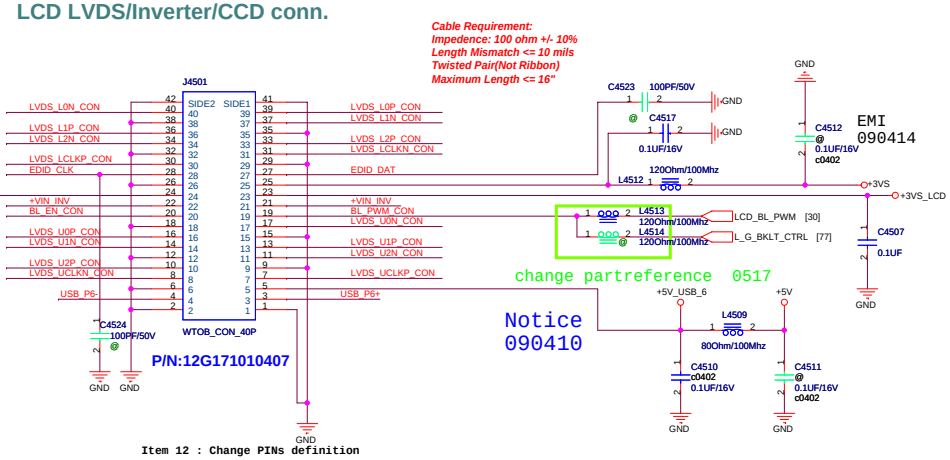
Remove Bead 2005/05/25

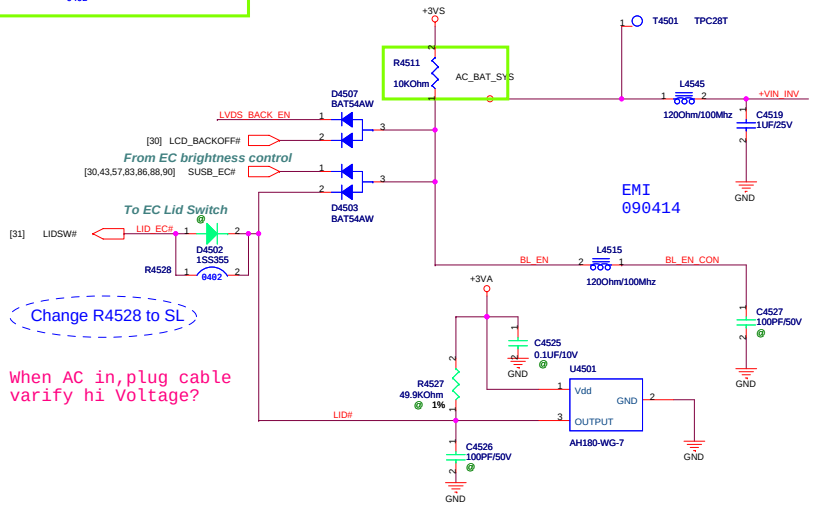
LCD Backlight Control

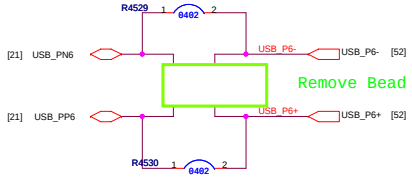
LCD Power



LCD LVDS/Inverter/CCD conn.







Remove Bead 2005/05/25

change SL
090411

<Variant Name>

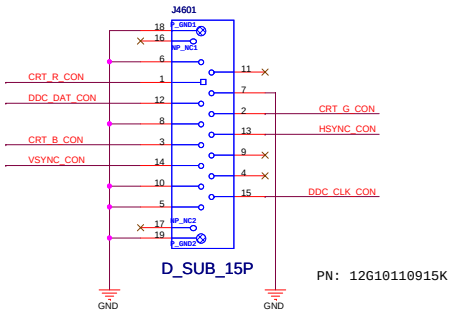
ASUSTeK COMPUTER INC.

Title : LVDS & INVERTER

Engineer: Richard_Lu

Size	Project Name	Rev
C	F5Z	2.05

Date: Friday, May 29, 2009 Sheet 45 of 91



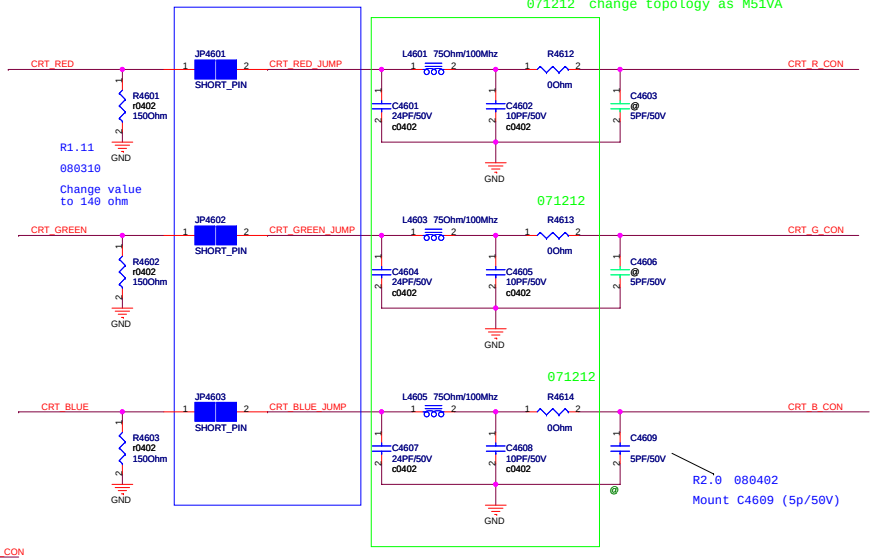
PN: 12G10110915K

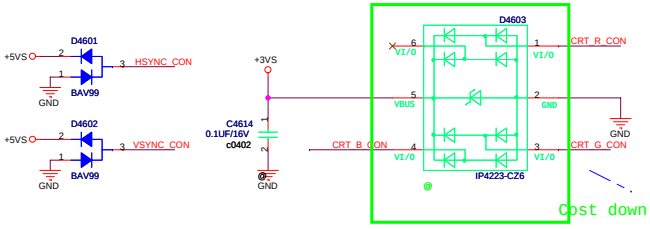
PLACE ESD Diodes near
VGA port

071204 Add Jump

071113

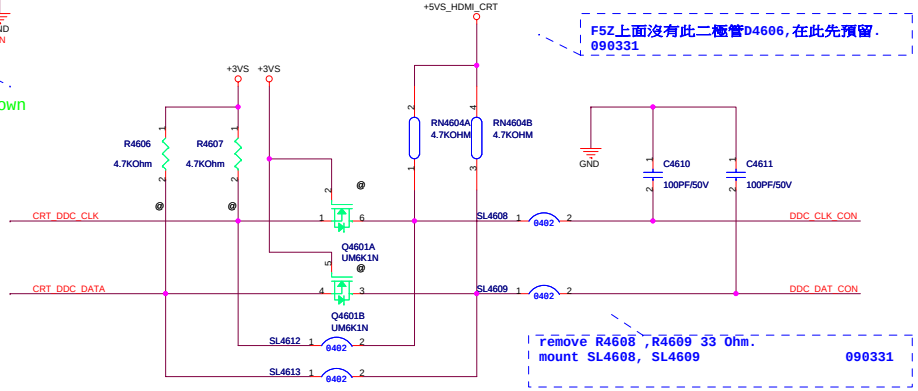
071212 change topology as M51VA





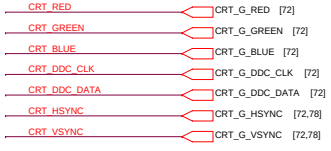
Cost down

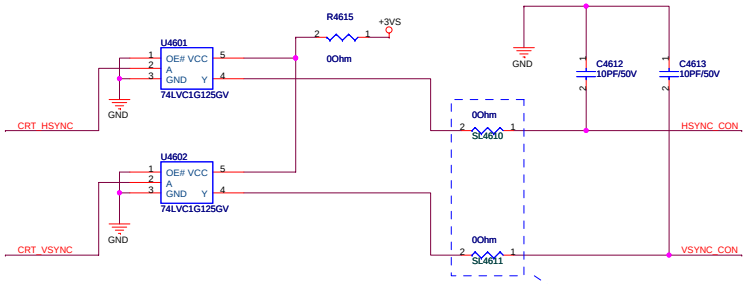
Notice change P/N
090410



F5Z上面沒有此二極管D4606,在此先預留.
090331

remove R4608 ,R4609 33 Ohm.
mount SL4608, SL4609 090331





remove R4610 ,R4611 27 Ohm.
mount SL4610, SL4611 090331

THE COST

<Variant Name>

Title : CRT

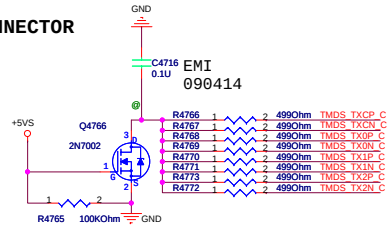
ASUSTeK COMPUTER INC

Engineer: Xinghua_chen

Size	Project Name	Rev
C	F83T	2.0

Date: Friday, May 29, 2009 Sheet 46 of 91

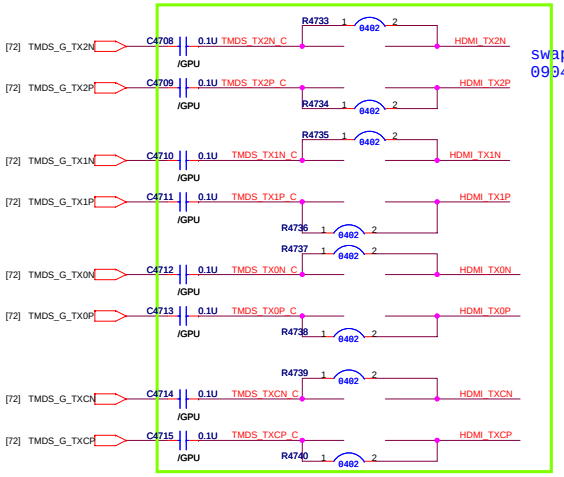
Close to CONNECTOR



不建議換成排阻.
090406

Close to CONNECTOR

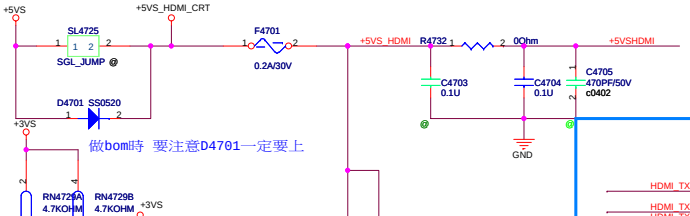
Notice
090410

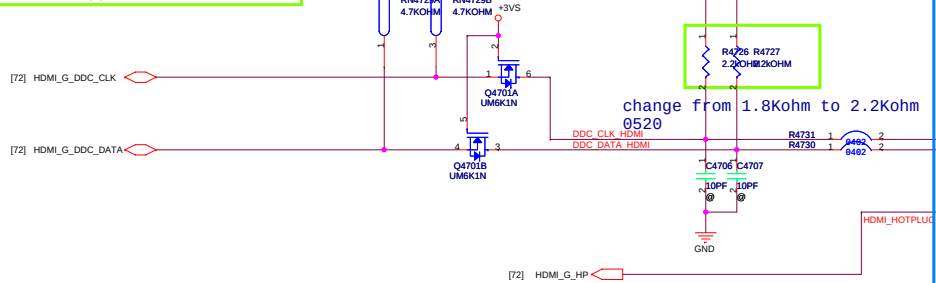


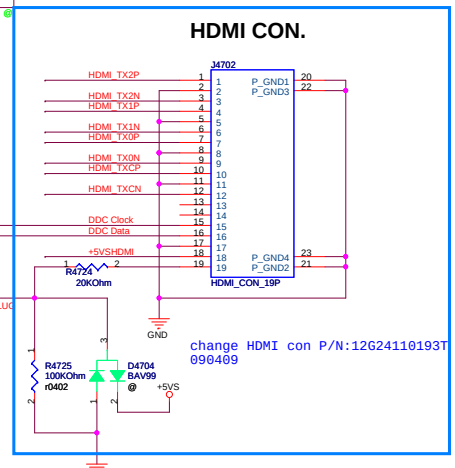
swap
090414

Remove Bead

Notice
090410







change HDMI con P/N:12G24110193T
090409

Note: 1. R1930,R1931,R1932: For EMI.(defult=0 ohm)
2. HDMI_DDC_CLK,HDMI_DDC_DATA: +3V tolerant

Notice
090410

ASUSTeK COMPUTER INC.	Title : HDMI	
	Engineer: Kuten Hsu	
Size: C	Project Name: F5Z	Rev: 2.05
Date: Wednesday, May 27, 2009	Sheet 47 of 91	

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard_Lu

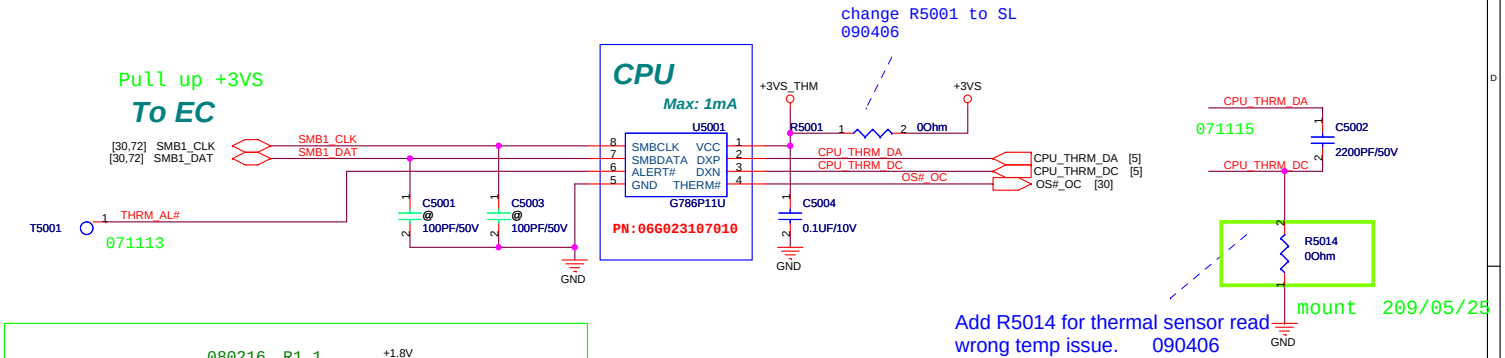
Size	Project Name	Rev
Custom	F5Z	2.05

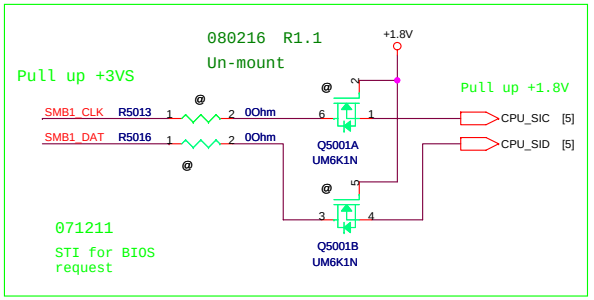
Date: Tuesday, May 26, 2009 Sheet 48 of 91

<Variant Name>

ASUSTeK COMPUTER INC	Title : *	
	Engineer: Richard Lu	
Size: A	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 49 of 91	

Thermal Sensor



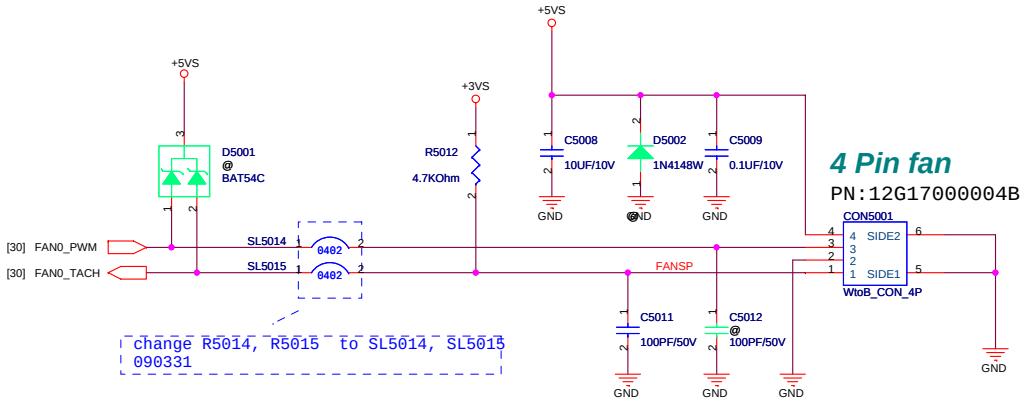


Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
15 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
========H_THERMDC(10 mils)
10 mils
=========GND
15 mils
----------OTHER SIGNALS

Avoid FSB,Power

DC FAN Control



<Variant Name>

Title : THER SENSOR & FAN

ASUSTeK COMPUTER INC

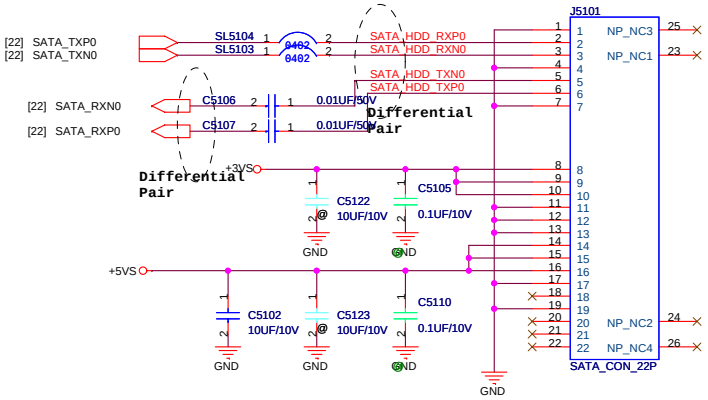
Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Friday, May 29, 2009 Sheet 50 of 91

SATA HDD

SATA HDD CON

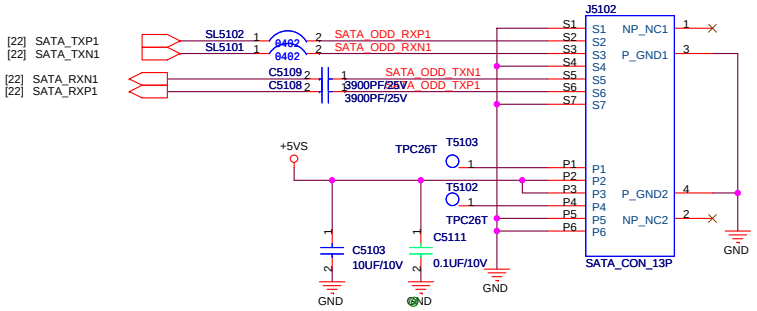


P/N:12G15200022G

MLCC 4700PF/25V (0402)X7R 10%
11G232147212360 Design IP

MLCC 0.1UF/10V (0402) X7R 10%
11G232110416360
比較一下價格

ODD



P/N:12G15100013J

<Variant Name>

ASUSTeK COMPUTER INC	Title : HDD & CD-ROM	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 51 of 91	

071119 change common choke and R P/N

080213 R1.1

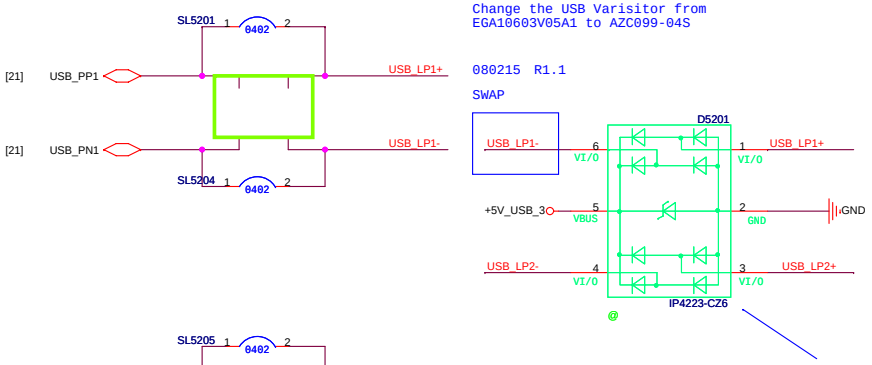
Change D5201 , D5204 , D5206 , D5208 footprint

080125 R1.1

Change the USB Varisitor from EGA10603V05A1 to AZC099-04S

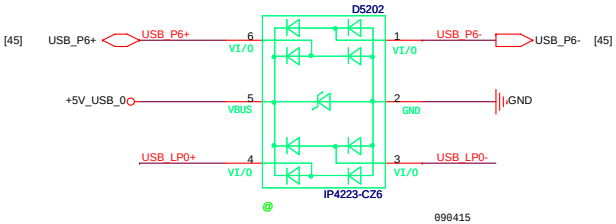
080215 R1.1

SWAP



07G028075010為建議用料
已經更換. 090331

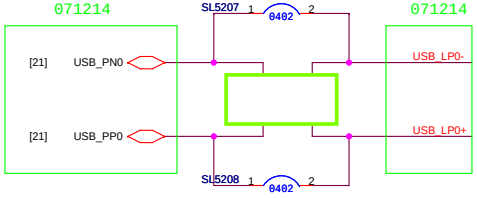
Remove Bead 2005/05/25



090415

swap 071214

swap 071214



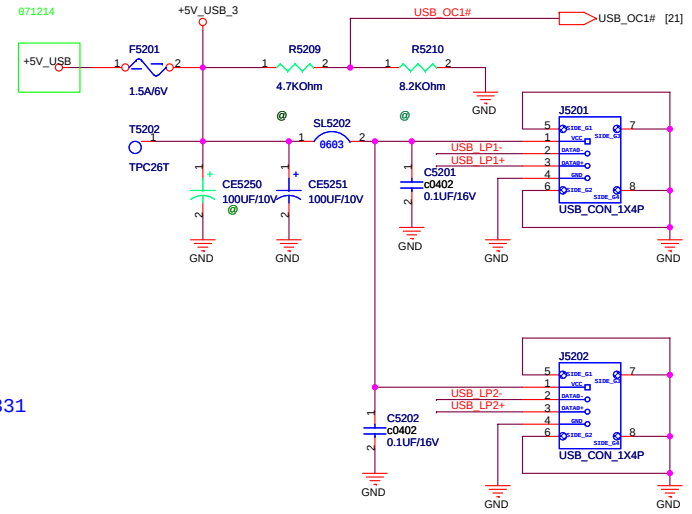
SWAP
090417

R1.1

080218

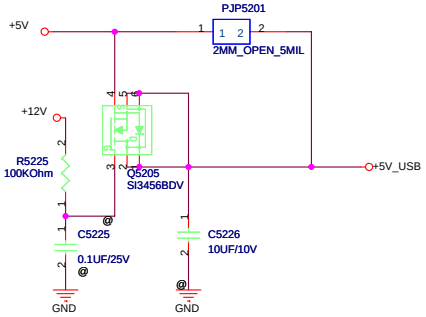
Change PN From
07G014075600 to
07G014075310

Change all MOS with ESD part

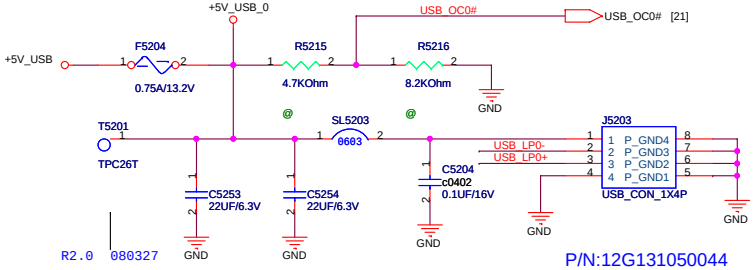


P/N:12G130011045

old:usb_1x4p_4hold_sun_lf3
new:nb_usb_1x4p_4hold_su_lf2



預留USB OC function 090406



R2.0 080327

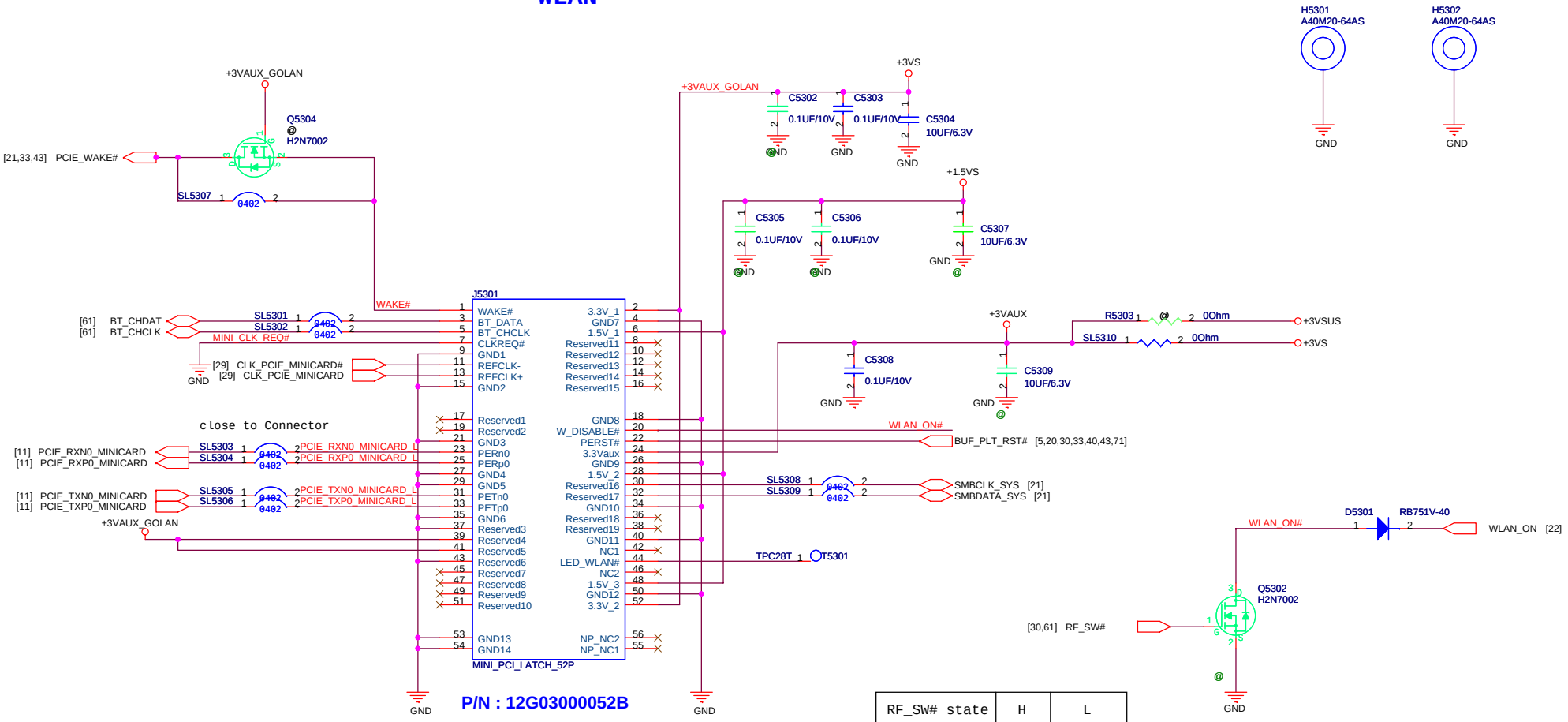
Add test point for factory ICT test

P/N:12G131050044

<Variant Name>

ASUSTeK COMPUTER INC	Title : USB CONN	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 52 of 91	

WLAN



P/N : 12G03000052B

RF_SW# state	H	L
WLAN state	Off	On

<Variant Name>

Title : MINICARD

ASUSTeK COMPUTER INC

Engineer: Xinghua_chen

Size	Project Name	Rev
Custom	F83T	2.0

Date: Friday, May 29, 2009 Sheet 53 of 91

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard Lu

Size	Project Name	Rev
A	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 54 of 91

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard Lu

Size	Project Name	Rev
A	F5Z	2.05

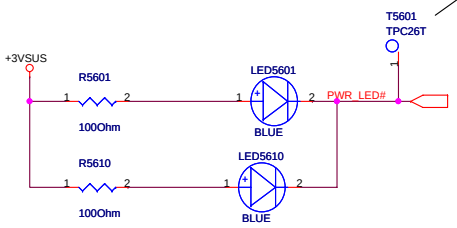
Date: Tuesday, May 26, 2009 Sheet 55 of 91

LED

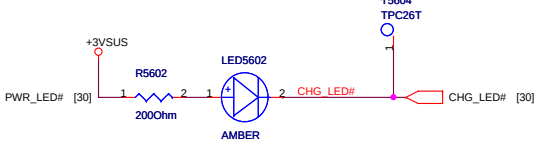
R2.0 080327

Add test point for factory ICT test

For POWER LED

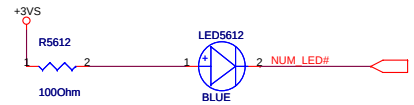


BATTERY LED



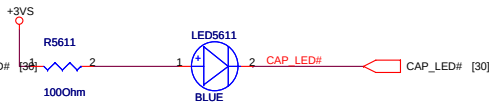
Num Lock

071122



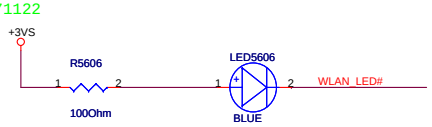
Cap Lock

071122



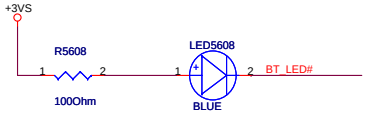
WireLess LED

071122



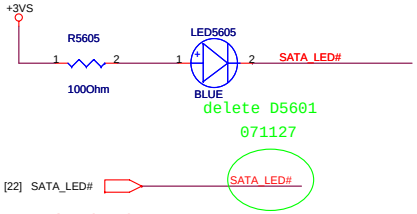
BT LED

071122

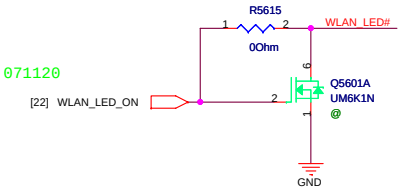


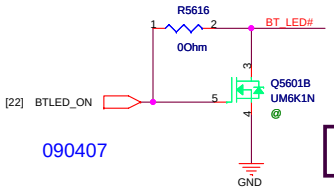
SATA/IDE LED

071122 071127



From SB GPIO





090407

Change all LED for 5mA

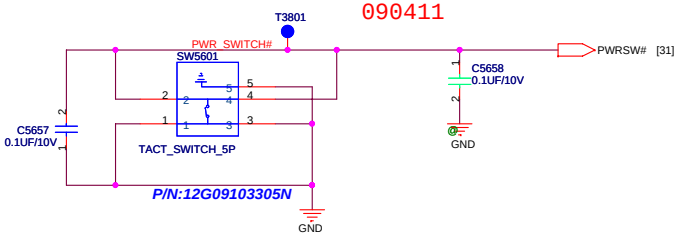
Change all MOS with ESD part

F5Z SWITCH CIRCUIT

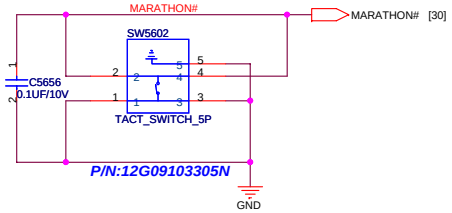
Move SW from P32 to P56

Power SW.

Remove R5656
090411

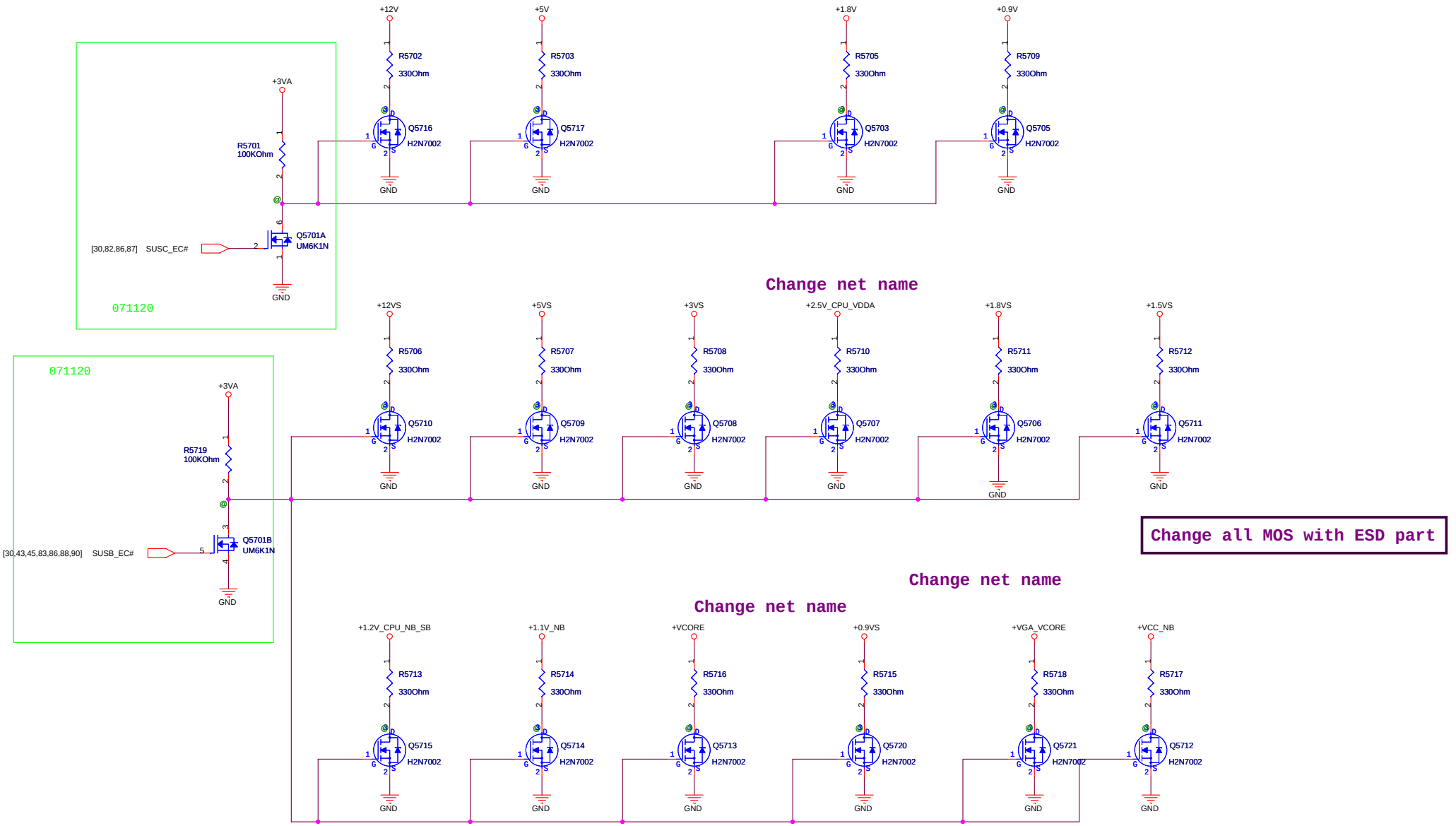


MARATHON#



<Variant Name>

ASUSTeK COMPUTER INC	Title : LED/PWR SWICH	
	Engineer: Xinghua_chen	
Size: Custom	Project Name: F83T	Rev: 2.0
Date: Wednesday, May 27, 2009	Sheet 56 of 91	



<Variant Name>

ASUSTeK COMPUTER INC

Title : DISCHARGE CKT

Engineer: Xinghua_chen

Size	Project Name	Rev
Custom	F83T	2.0

Date: Wednesday, May 27, 2009 Sheet 57 of 91

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 58 of 91

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard Lu

Size	Project Name	Rev
A	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 59 of 91

BATTERY

cahnge PL->L,PT->T,PC->C

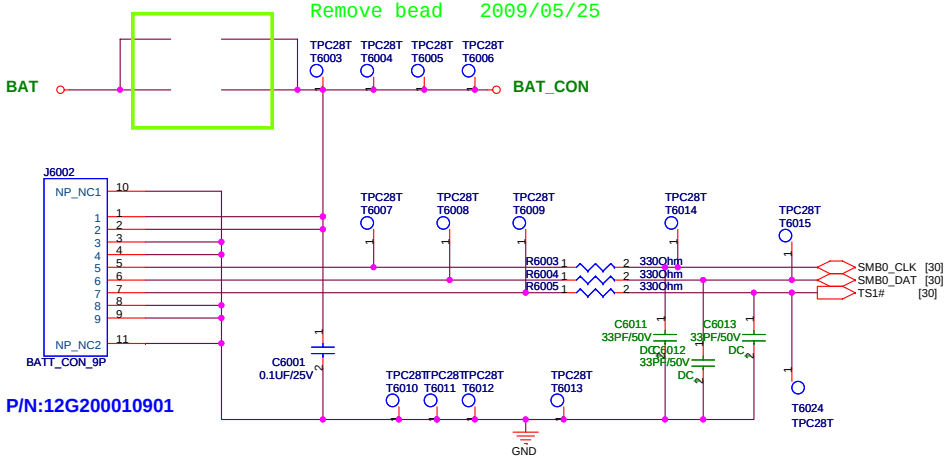
071120

Removen JP

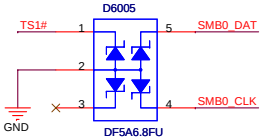
Remove bead 2009/05/25

change footprint

071203



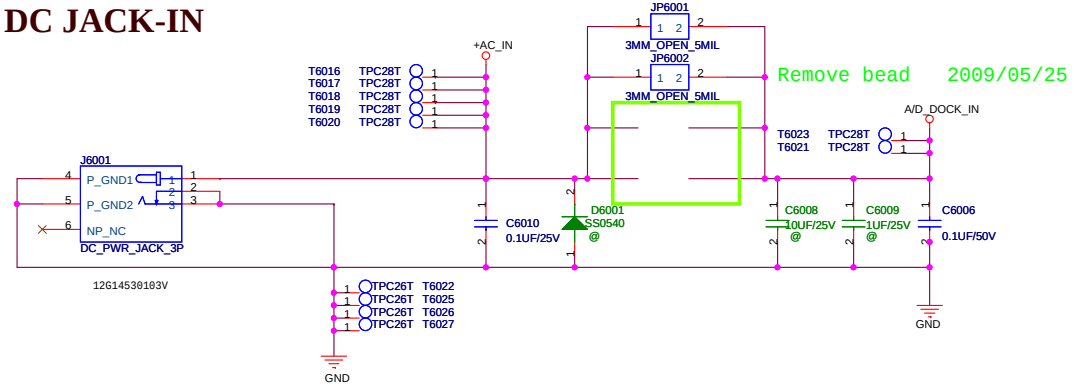
P/N:12G200010901



Add for AC Adapter protect

Adaptor IN

DC JACK-IN



<Variant Name>

ASUSTeK COMPUTER INC

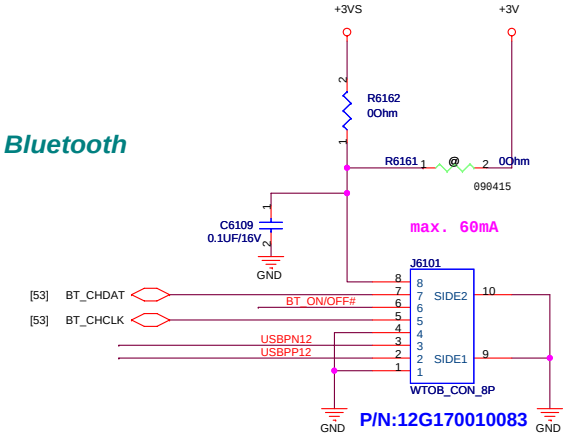
Title : DC_Jack & BAT Con

Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F5Z	2.05

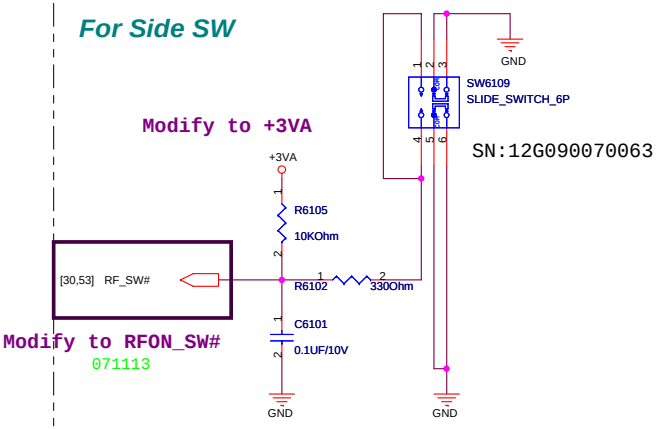
Date: Tuesday, May 26, 2009 Sheet 60 of 91

For Bluetooth



P/N:12G170010083

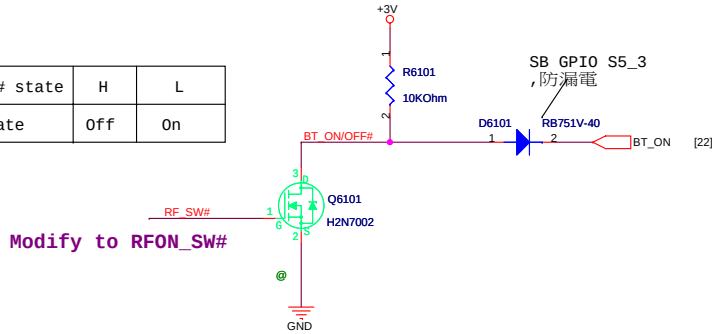
For Side SW



Modify to RFON_SW#

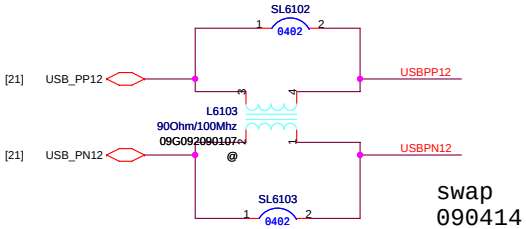
071113

RF_SW# state	H	L
BT state	Off	On



RN swap

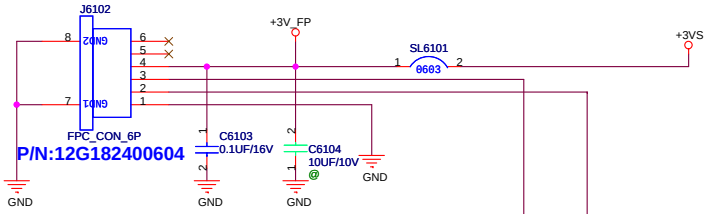
071214



swap
090414

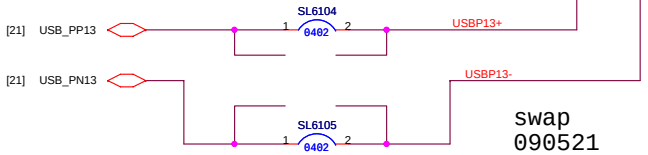
071120 change common choke and R P/N

Fingerprint Conn.



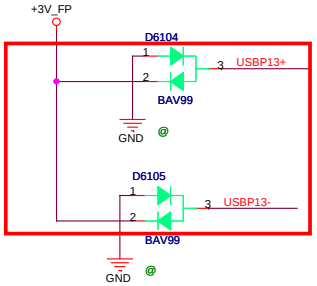
Co-layout for EMI

Cost down



swap
090521

optional，先上測試功能



<Variant Name>

Title : BT & Slide SW

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F83T	2.05

Date: Friday, May 29, 2009 Sheet 61 of 91

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard Lu

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 62 of 91

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 63 of 91

<Variant Name>

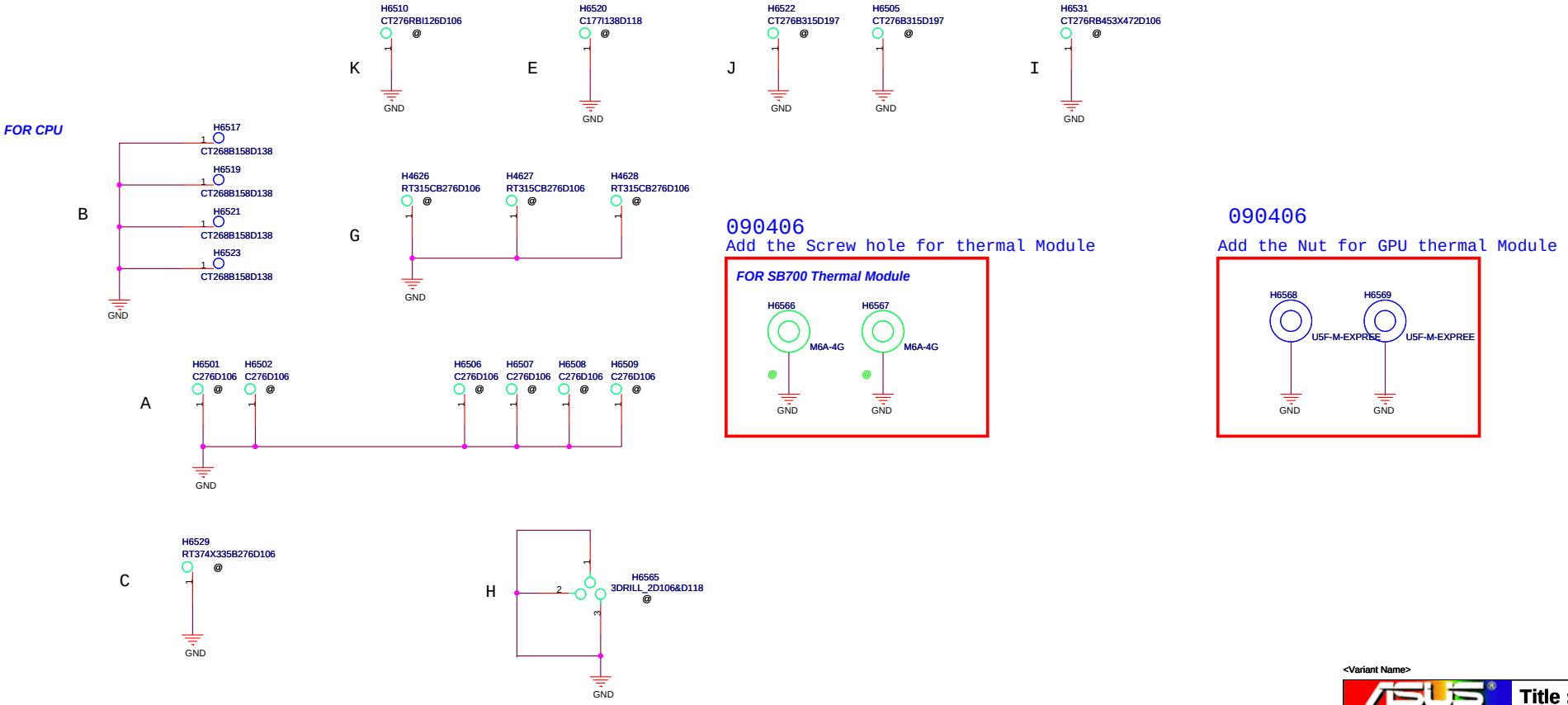
Title : TUN

ASUSTeK COMPUTER INC

Engineer: Richard Lu

Size	Project Name	Rev
B	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 64 of 91



change to P/N:13GN9980M090-1 for high limit

<Variant Name>

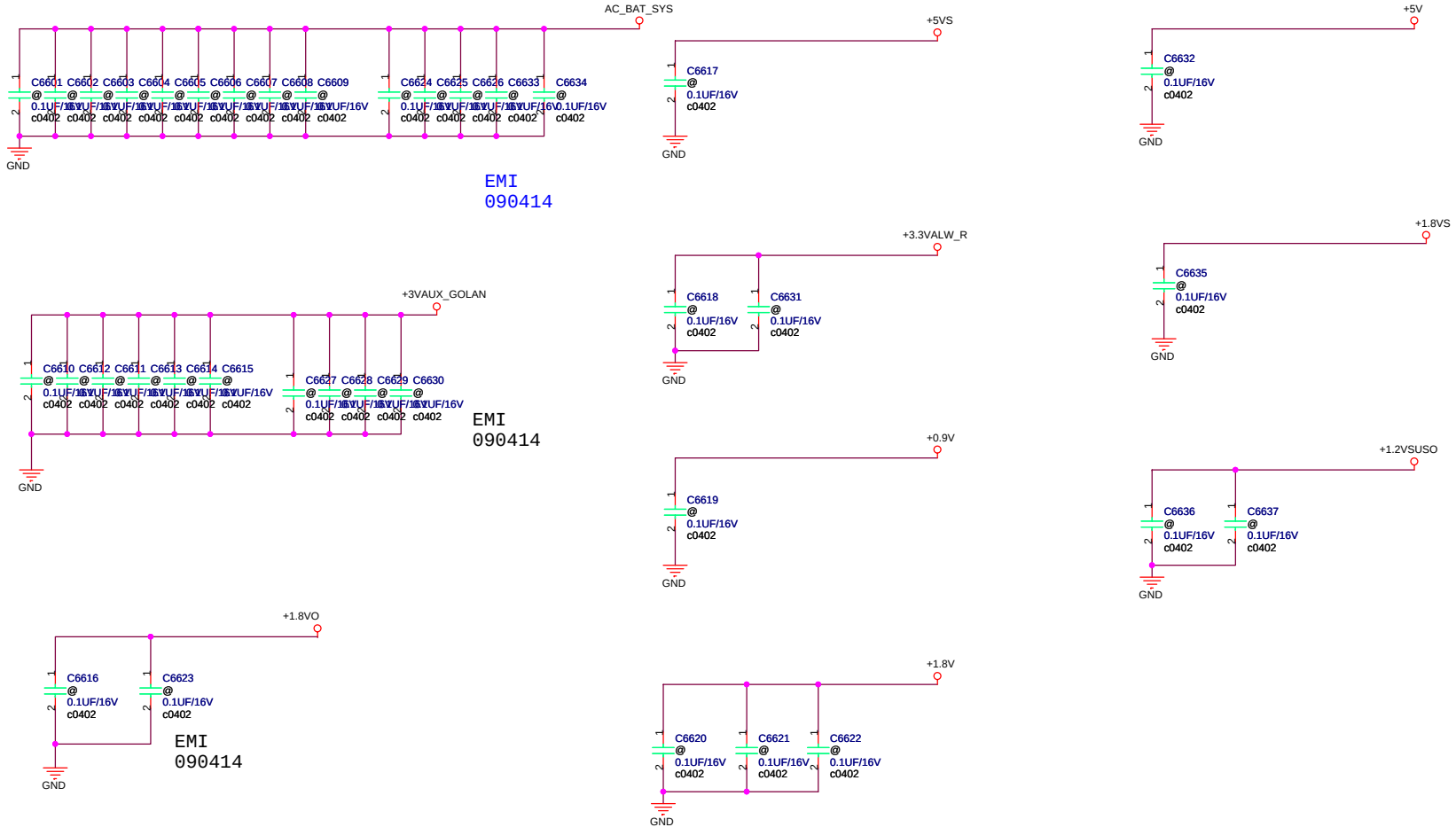
ASUSTeK COMPUTER INC

Title : Screw Hole

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Friday, May 29, 2009 Sheet 65 of 91



<Variant Name>

ASUSTeK COMPUTER INC

Title : EMI

Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 66 of 91

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard Lu

Size	Project Name	Rev
B	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 67 of 91

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 68 of 91

1,Vram data swap. 090327

2,修改VGA_CORE 電壓，Boot 電壓為1.2V. 090327

3, Page72 add a resister which connect between
XTALIN and XTALOUT when a 27MHz crystal is used. 090329

4, SWAP VRAM data Group4 and Group5 090330

5,Audio AVDD 預留 +3VS 090330

6, Add RN4301, 預留L4301. 090331

7,remove R4610 ,R4611 27 Ohm.(EMI), remove R4608 ,R4609 33 Ohm.
mount SL4608, SL4609 ,mount SL4610, SL4611 090331

8,LCD Backlight Control change 090331

9,Remove RJ11 090331

11,SB710 的晶振換成F80系列的32.768KHz的晶振.
網卡的25MHz的晶振換成料號為07G010Q12500. 090331

12, U4301 pin 18 REFCLKEN NC, remove part 090331

13,Change the ClkGen to RTM880T-797 090331

14, AU6433-GLF mount R4007 090331

15,CLK_REQ_LAN is OD ,add R2003 pull high. 090401

17,change power cap PCE8701 & PCE8702 090401

18,change the Screw Hole,Add the Nut for GPU thermal Module 090406

19,Modify the NB & SB power cap 090406

20,Swap the cap pack in page31 090406

21,changeR4726,R4727 from 1.8Kohm to 2.2Kohm 090520

22.Add buffer U4601,U4602 090520

24.Change R4511 to 10Kohm,R7870 to 2.2Kohm 090520

25.Add R2037 for safety 090520

28.Remove L6003,L6004,L6005,L6006 090525

29. Add 10uF cap C7549 090525

30.Remove L4001, L4502, L4506, L4508, L4511, L4503, L4507, L4510, L4504,
L4505, L6104, L5201, L5202, L5204, L4704, L4705, L4706, L4707 090525

31.Mount R5014, R7207 090525

32.預留 X7201, C7220, C7219, R7214, R7257 090525

33.Remove NUT for SB 090525

34.Change X2201 P/N:07G010Q12500 090525

35.Change R0403, R0404 from 15ohm to 1Kohm 090525

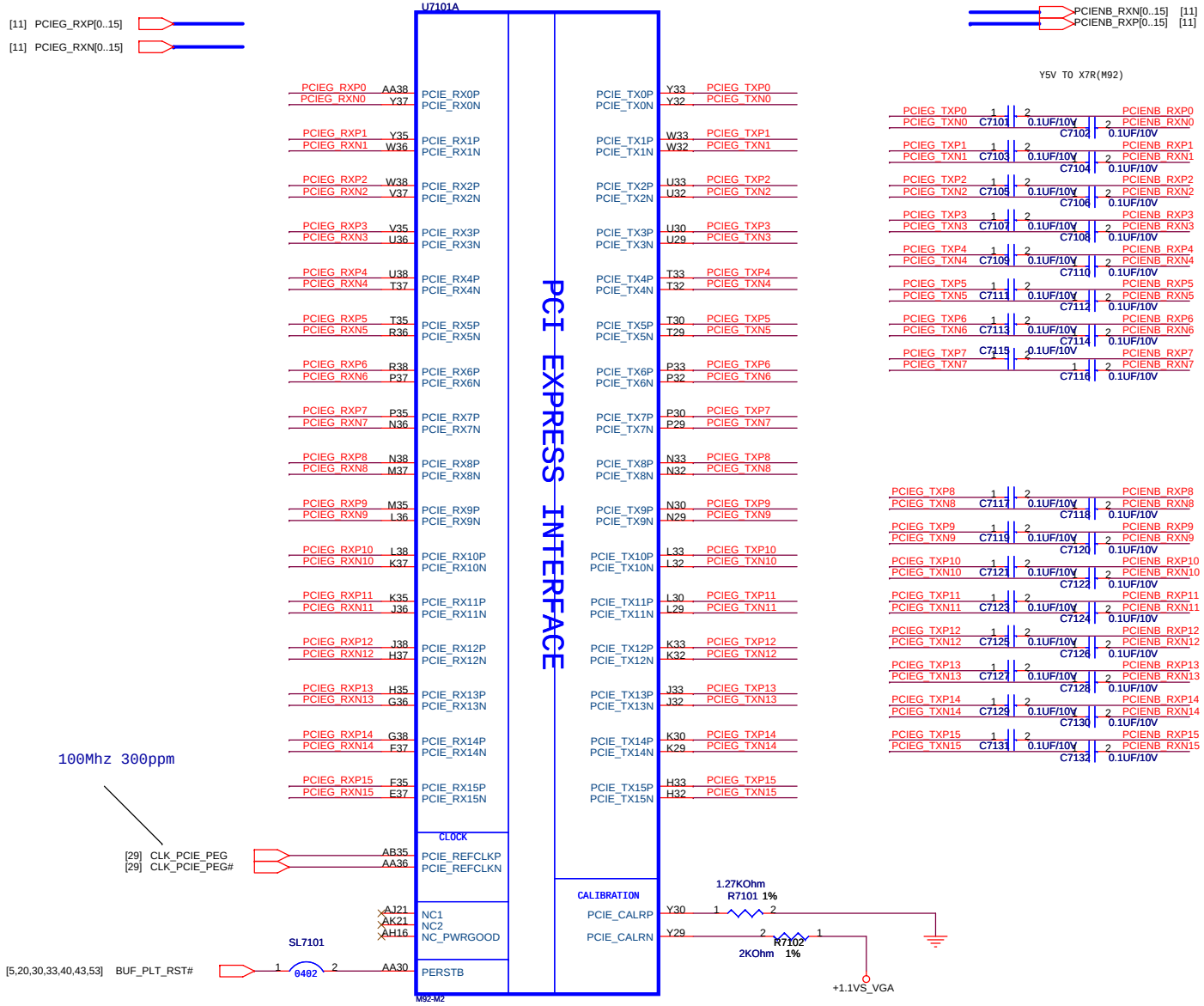
36. Add C4019 for EMI 090525

37. Change SL4610,SL4610 to 0ohm 090526

ASUSTeK COMPUTER INC. NB1		Title : HISTORY	
		Engineer: <OrgAddr1>	
Size: Custom	Project Name: F5Z		Rev: 2.05
Date: Friday, May 29, 2009		Sheet 69 of 91	

Title : <Title>		
<OrgName>	Engineer: <OrgAddr1>	
Size: A	Project Name: <Doc>	Rev: <RevCode>
Date: Tuesday, May 26, 2009	Sheet 70 of 91	

notice the net name.RX&TX



<Variant Name>

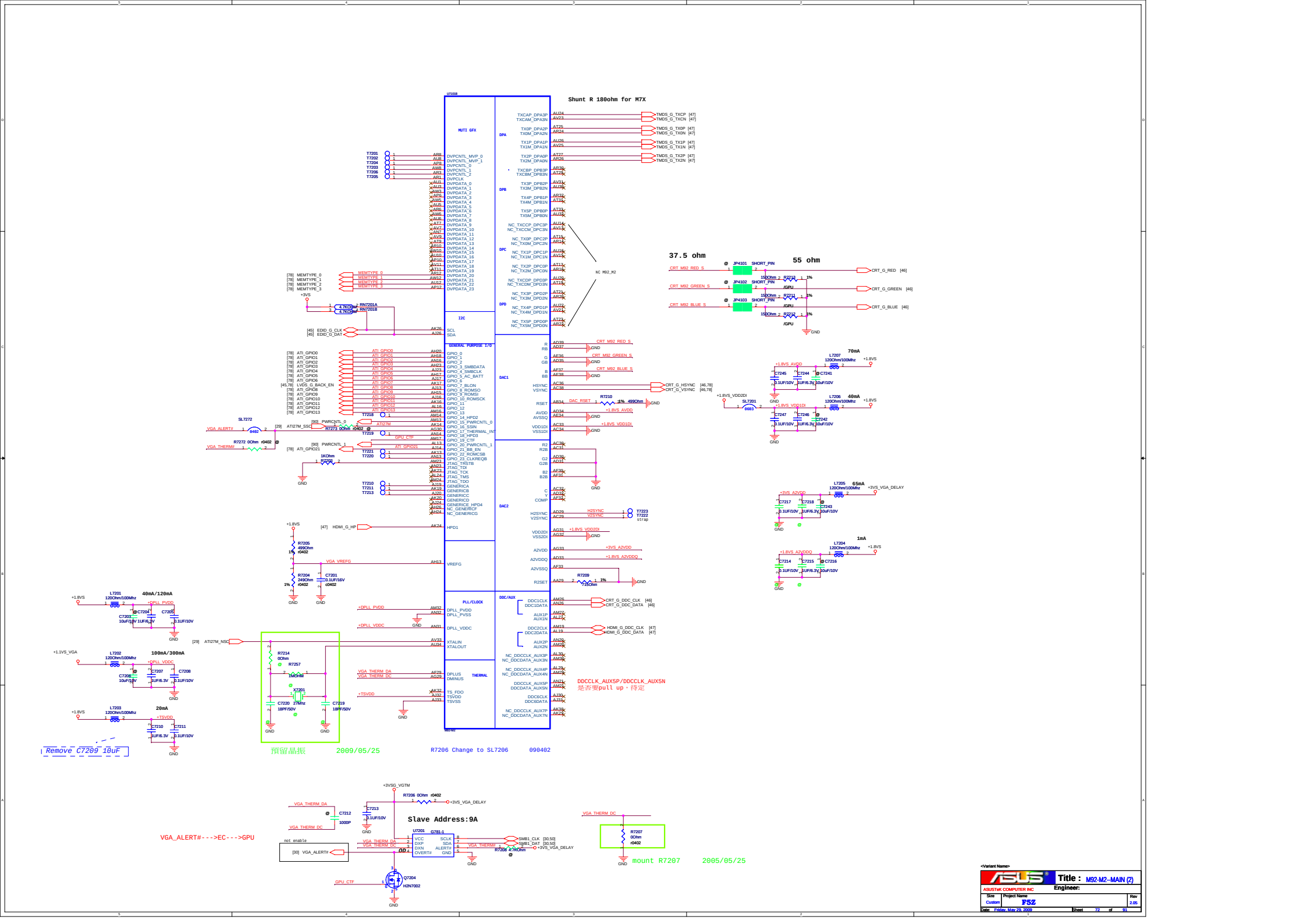
Title : M92-M2--PCIE (1)

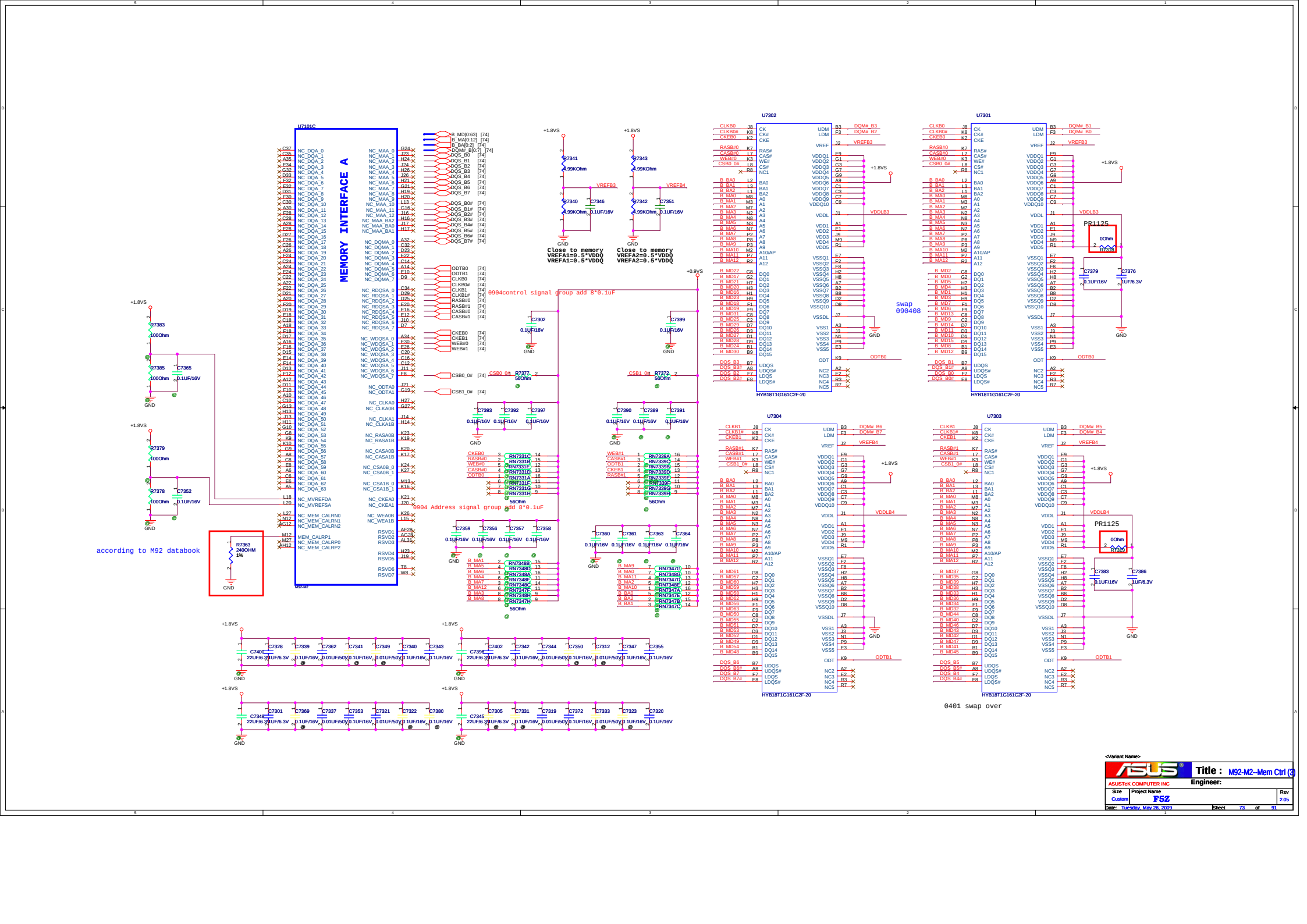
ASUSTeK COMPUTER INC

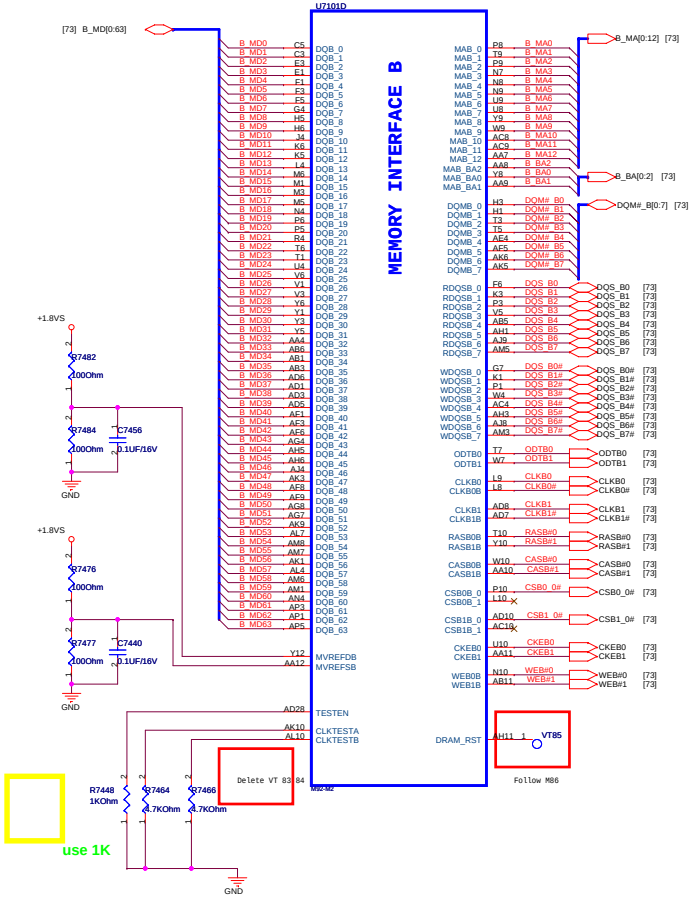
Engineer:

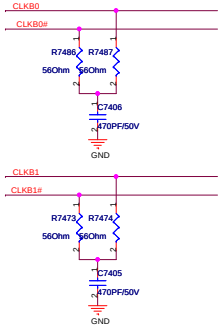
Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 71 of 91


Shunt R 180ohm for M7X
37.5 ohm
55 ohm
MUTI GFX
I2C
GENERAL PURPOSE I/O
PLL/CLOCK
DDC/AUX
THERMAL
DPA
DPB
DPC
DPD
DAC1
DAC2
NC M92_M2
DDCCLK_AUX5P/DDCCLK_AUX5N
是否要pull up，待定
Remove C7209 10uF
預留晶振 2009/05/25
R7206 Change to SL7206 090402
Slave Address:9A
VGA_ALERT#--->EC--->GPU
mount R7207 2005/05/25
Title : M92-M2--MAIN (2)
ASUSTeK COMPUTER INC
Engineer:
Size: Custom
Project Name: F5Z
Rev: 2.05
Date: Friday, May 29, 2009
Sheet 72 of 91


MEMORY INTERFACE A
U7101C
M92-M2
B_MD[0:63] [74]
B_MA[0:12] [74]
B_BA[0:2] [74]
DQM#_B[0:7] [74]
DQS_B0 [74]
DQS_B1 [74]
DQS_B2 [74]
DQS_B3 [74]
DQS_B4 [74]
DQS_B5 [74]
DQS_B6 [74]
DQS_B7 [74]
DQS_B0# [74]
DQS_B1# [74]
DQS_B2# [74]
DQS_B3# [74]
DQS_B4# [74]
DQS_B5# [74]
DQS_B6# [74]
DQS_B7# [74]
ODTB0 [74]
ODTB1 [74]
CLKB0 [74]
CLKB0# [74]
CLKB1 [74]
CLKB1# [74]
RASB#0 [74]
RASB#1 [74]
CASB#0 [74]
CASB#1 [74]
CKEB0 [74]
CKEB1 [74]
WEB#0 [74]
WEB#1 [74]
CSB0_0# [74]
CSB1_0# [74]
+1.8VS
+0.9VS
R7341 4.99KOhm
R7343 4.99KOhm
R7340 4.99KOhm
R7342 4.99KOhm
C7346 0.1UF/16V
C7351 0.1UF/16V
VREFB3
VREFB4
Close to memory
VREFA1=0.5*VDDQ
Close to memory
VREFA2=0.5*VDDQ
0904control signal group add 8*0.1uF
0904 Address signal group add 8*0.1uF
R7377 56Ohm
R7372 56Ohm
R7383 100Ohm
R7385 100Ohm
C7365 0.1UF/16V
R7379 100Ohm
R7378 100Ohm
C7352 0.1UF/16V
R7363 240OHM 1%
according to M92 databook
U7302
U7301
U7304
U7303
HYB18T1G161C2F-20
swap 090408
PR1125
0Ohm
C7379 0.1UF/16V
C7376 1UF/6.3V
C7383 0.1UF/16V
C7386 1UF/6.3V
0401 swap over
<Variant Name>
Title : M92-M2--Mem Ctrl (3)
Engineer:
ASUSTeK COMPUTER INC
Size Custom
Project Name F5Z
Rev 2.05
Date: Tuesday, May 26, 2009
Sheet 73 of 91





Del 4 Vram
090323

<Variant Name>

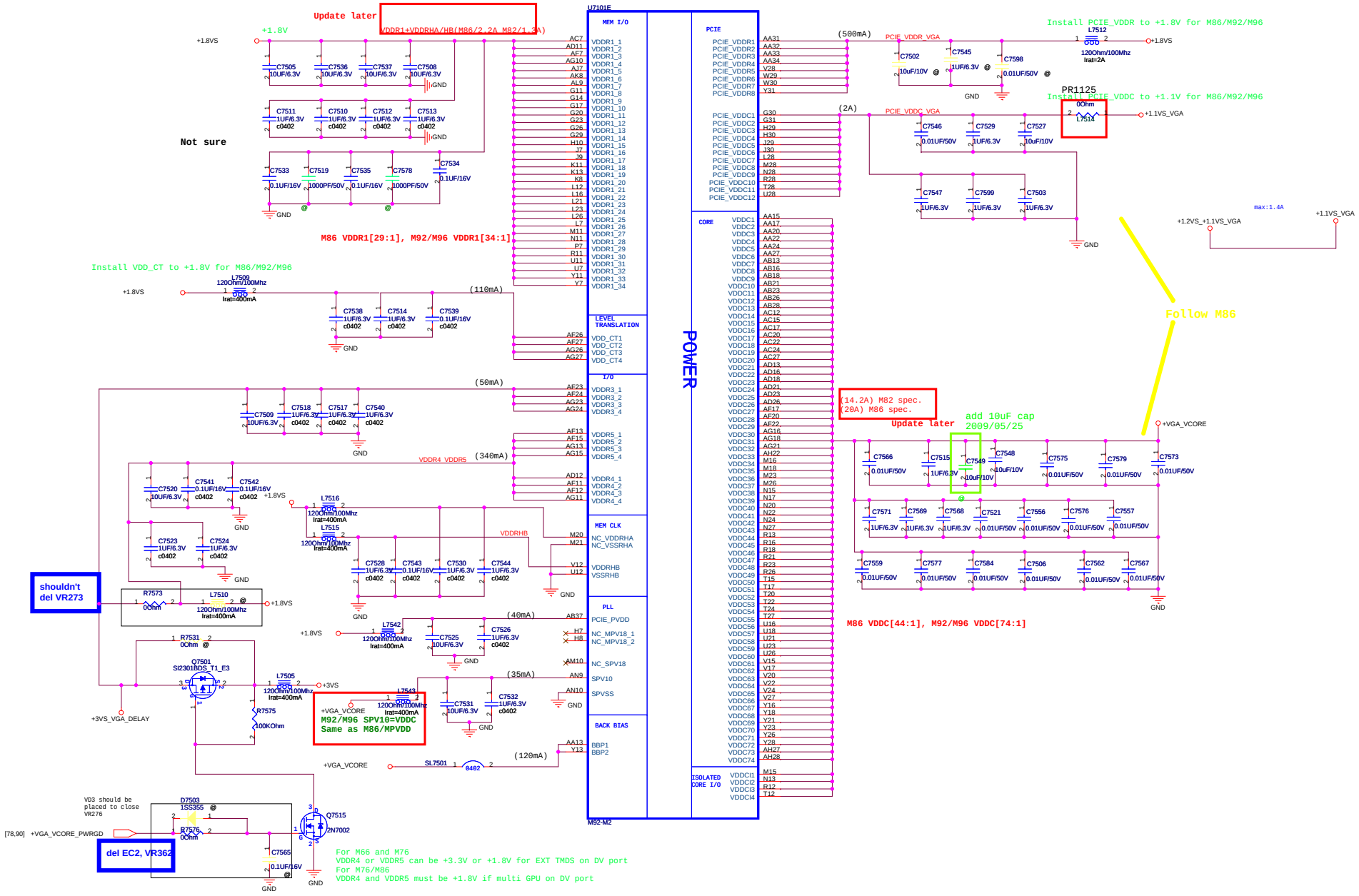
ASUSTeK COMPUTER INC

Title : M92S2-MEM VRAM(4)

Engineer:

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 74 of 91



<variant_name>

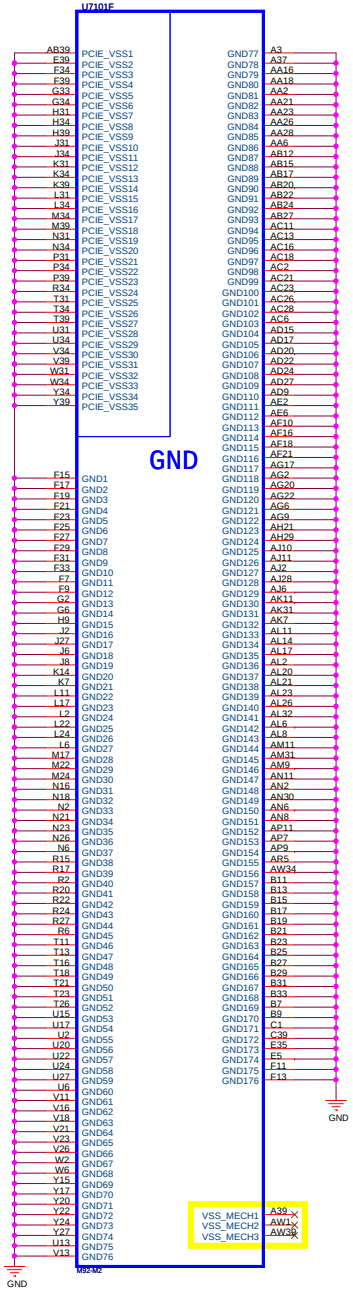
ASUSTeK COMPUTER INC.

Title : M92S2-PWR (5)

Engineer:

Size	Project Name	Rev
C	F5Z	2.05

Date: Friday, May 29, 2009 Sheet 75 of 91



<Variant Name>

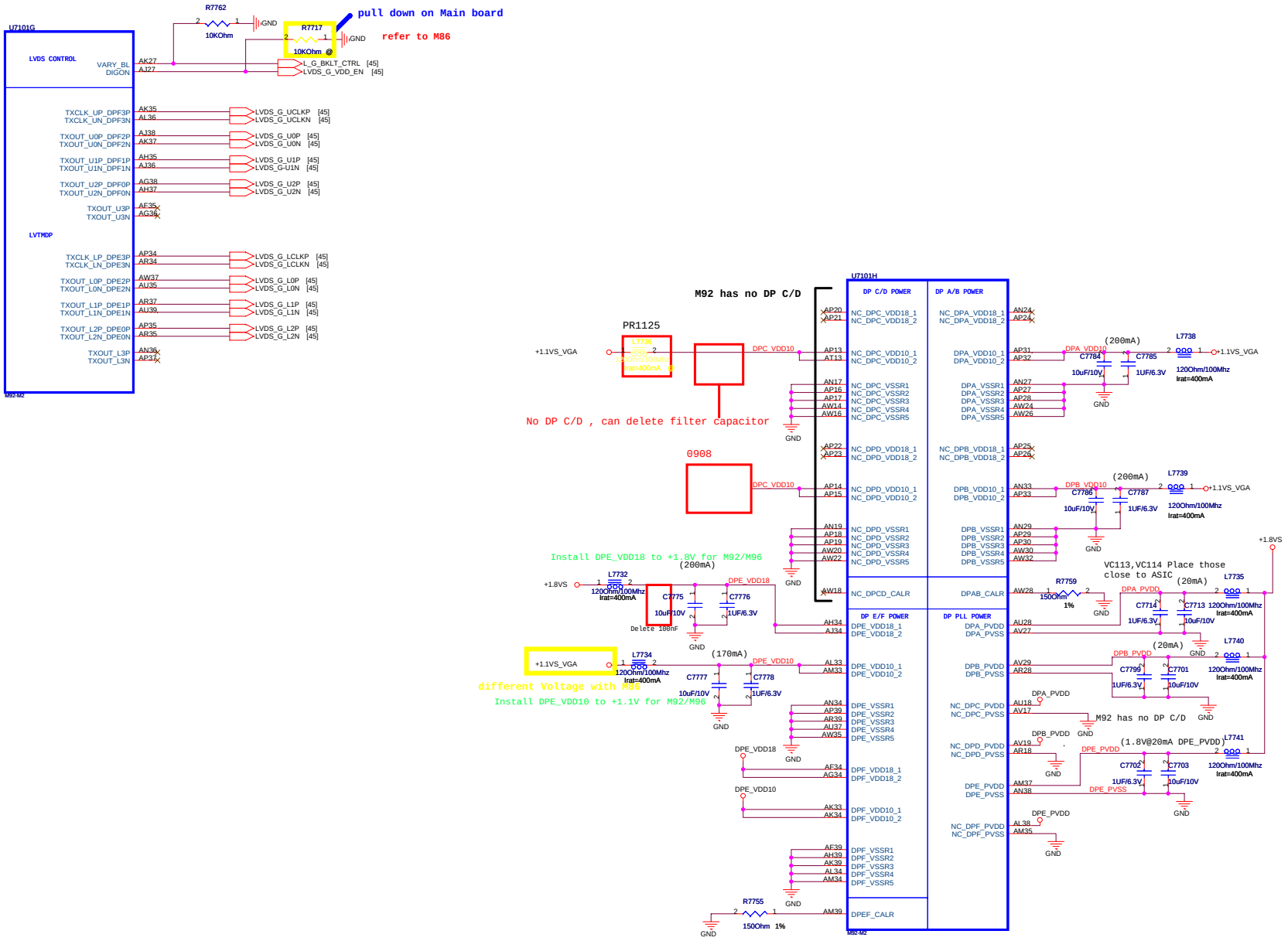
ASUSTeK COMPUTER INC.

Title : *

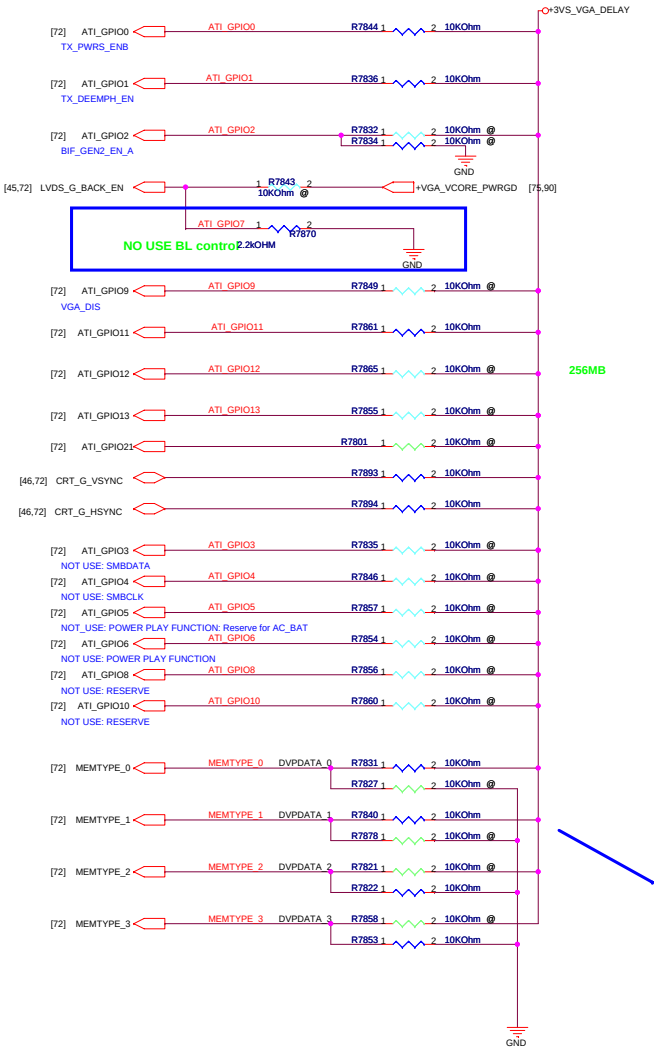
Engineer:

Size	Project Name	Rev
C	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 76 of 91


U7101G
LVDS CONTROL
VARY_BL
DIGON
R7762
10KOhm
R7717
10KOhm @
pull down on Main board
refer to M86
L_G_BKLT_CTRL [45]
LVDS_G_VDD_EN [45]
TXCLK_UP_DPF3P
TXCLK_UN_DPF3N
TXOUT_U0P_DPF2P
TXOUT_U0N_DPF2N
TXOUT_U1P_DPF1P
TXOUT_U1N_DPF1N
TXOUT_U2P_DPF0P
TXOUT_U2N_DPF0N
TXOUT_U3P
TXOUT_U3N
LVTMDP
TXCLK_LP_DPE3P
TXCLK_LN_DPE3N
TXOUT_L0P_DPE2P
TXOUT_L0N_DPE2N
TXOUT_L1P_DPE1P
TXOUT_L1N_DPE1N
TXOUT_L2P_DPE0P
TXOUT_L2N_DPE0N
TXOUT_L3P
TXOUT_L3N
M92-M2
U7101H
M92 has no DP C/D
PR1125
No DP C/D , can delete filter capacitor
0908
Install DPE_VDD18 to +1.8V for M92/M96
different Voltage with M86
Install DPE_VDD10 to +1.1V for M92/M96
Delete 100nF
VC113,VC114 Place those close to ASIC
M92 has no DP C/D
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
M92-M2
Title : M92S2-LVDS (6)
ASUSTeK COMPUTER INC
Engineer:
Size C
Project Name F5Z
Rev 2.05
Date: Tuesday, May 26, 2009
Sheet 77 of 91

OPTION STRAPS



M92 Straps

	STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
	VIP_DEVICE_STRAP_EN	V2SYNC	0 - Ignore VIP device straps (DVPDATA_20) 1 - Use VIP device straps (DVPDATA_20)	0 (internal pull-down)
OK	TX_PWRS_ENB	GPIO0	Tansmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing This setting can only be used if the PCIE bus design meets the "Low Loss interconnect" requirements.	0 (internal pull-down)
OK	TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled MXM and add-in boards	0 (internal pull-down)
OK	BIF_GEN2_EN_A	GPIO2	1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on 0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on	0
OK	VGA_DIS	GPIO9	0 - VGA Controller capacity enabled 1 - The device will not be recognized as the system's VGA controller	0 (internal pull-down)
OK	ROMIDCFG(2:0)	GPIO(13:11)	If BIOS_ROM_EN=1,then Config[2:0]defines the ROM type. If BIOS_ROM_EN=0,then Config[2:0]deifnes the primary memoru apeture size. 128MB---x000 32MB---Not Support 2GB---Not Support 256MB---x001 512MB--Not Support 4GB---Not Support 64MB---x010 1GB------Not Support	0000 (internal pull-down)
OK	BIOS_ROM_EN	GPIO22_ROMCSB	Enable external BIOS ROM device 0-Disable external BIOS ROM device 1-Enable external BIOS ROM device	0 (internal pull-down)
OK	AUD[1] AUD[0]	PEG_CRT_HSYNC_VGA PEG_CRT_VSYNC_VGA	AUD[1:0]: 00: No audio function; 01: Audio for DisplayPort and HDMI if adapter is detected; 10: Audio for DisplayPort only; 11: Audio for both DisplayPort and HDMI.	0 (internal pull-down)
OK OK	Reserved	H2SYNC GPIO_21_BB_EN GENERICC	ATI internal use only . THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET.	0 (internal pull-down)

AUDIO_EN	VIP_3	Enable HD Audio function in the PCI configuration space 0 - Disable HD Audio 1 - Enable HD Audio	0 (internal pull-down)
64BAR_EN_A	VIP_5	Enable 64-bit BARs Most commonly this strap is left at the default (32-bit BARs)	0 (internal pull-down)
MSI_DIS	VIP_1	Disable Message Signaled Interrupt is both a ROM strap and a pin strap. The pin strap is only applicable if a BIOS ROM is not present	0 (internal pull-down)
VIP_DEVICE	VHAD_0	VIP_DEVICE_STRAP_EN is set 0 =>not used VIP Host interface VIP_DEVICE_STRAP_EN is set 1 =>used VIP Host interface	0 (internal pull-down)
DEBUG ACCESS	GPIO4	Debug_access strap 3.3V ---ON 0V------OFF	0 (internal pull-down)
DEBUG_I2C_ENABLE	GPIO6	ATI internal use only . Other logic must not affect this signal during RESET Reconnended to 0	0 (internal pull-down)

0010-DDR2 Qimonda(64MX16) 512MB
Mount: VR27, VR40, VR22, VR353
Unmount: VR31, VR41, VR21, VR352

0011-DDR2 Qimonda(64MX16) 1G
Mount: VR31, VR40, VR22, VR353
Unmount: VR27, VR41, VR21, VR352

0100-DDR2 Samsung(64MX16) 512MB
Mount: VR27, VR41, VR21, VR353
Unmount: VR31, VR40, VR22, VR352

0101-DDR2 Samsung(64MX16) 1G
Mount: VR31, VR41, VR21, VR353
Unmount: VR27, VR40, VR22, VR352

Memory ID Board Straps

Vendor	DVPDATA(23,22,21,20)	ID	DDR2 Memory Type	Channel Size
Qimonda	**0000**	**0**	**32M*16 (256M)**	B channel
	0001	**1**	**32M*16 (512M)**	B channel dual-link
	0010	2	**64M*16 (512M)**	B channel
	0011 M92-M2	3	**64M*16 (1G)**	B channel dual-link
Samsung	**0100**	**4**	**64M*16 (512MB)**	B channel
	0101 M92-M2	**5**	**64M*16 (1G)**	B channel dual-link
	0110	6	**32M*16 (256MB)**	B channel M92-M2 only support B channel
	0111	7	**32M*16 (512MB)**	B channel dual-link
Hynix	1000	8	**32M*16 (256M)**	B channel
	1001	9	**32M*16 (512M)**	B channel dual-link
	1010	10	**64M*16 (512M)**	B channel
	1011 M92-M2	11	**64M*16 (1G)**	B channel dual-link
	1100	12		
	1101	13	**TBD**	
	1110	14		
Micron	1111	15	64M*16 (1G)	B channel dual-link

<Variant Name>

ASUSTeK COMPUTER INC.

Title : *

Engineer:

Size	Project Name	Rev
C	F5Z	2.05

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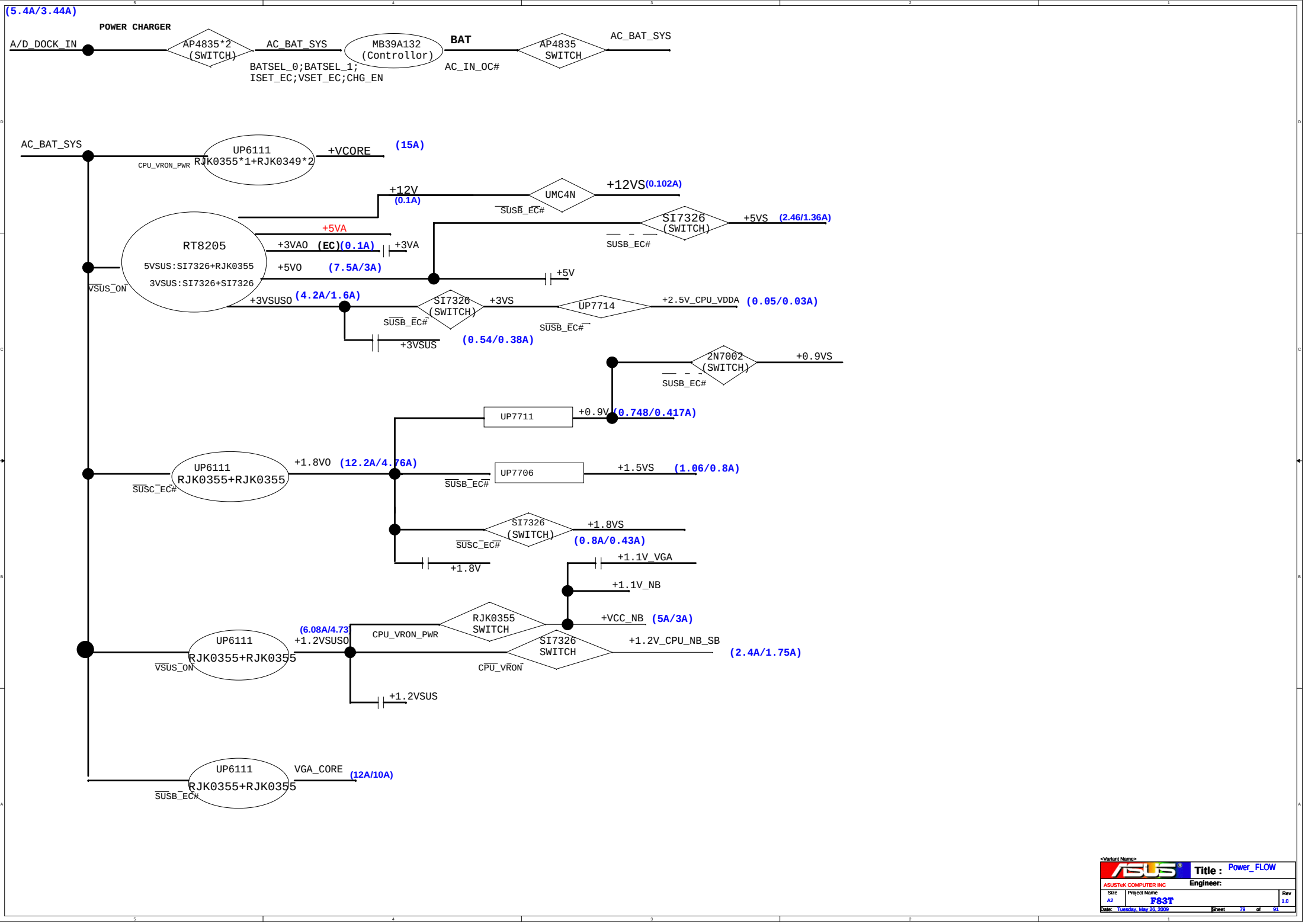
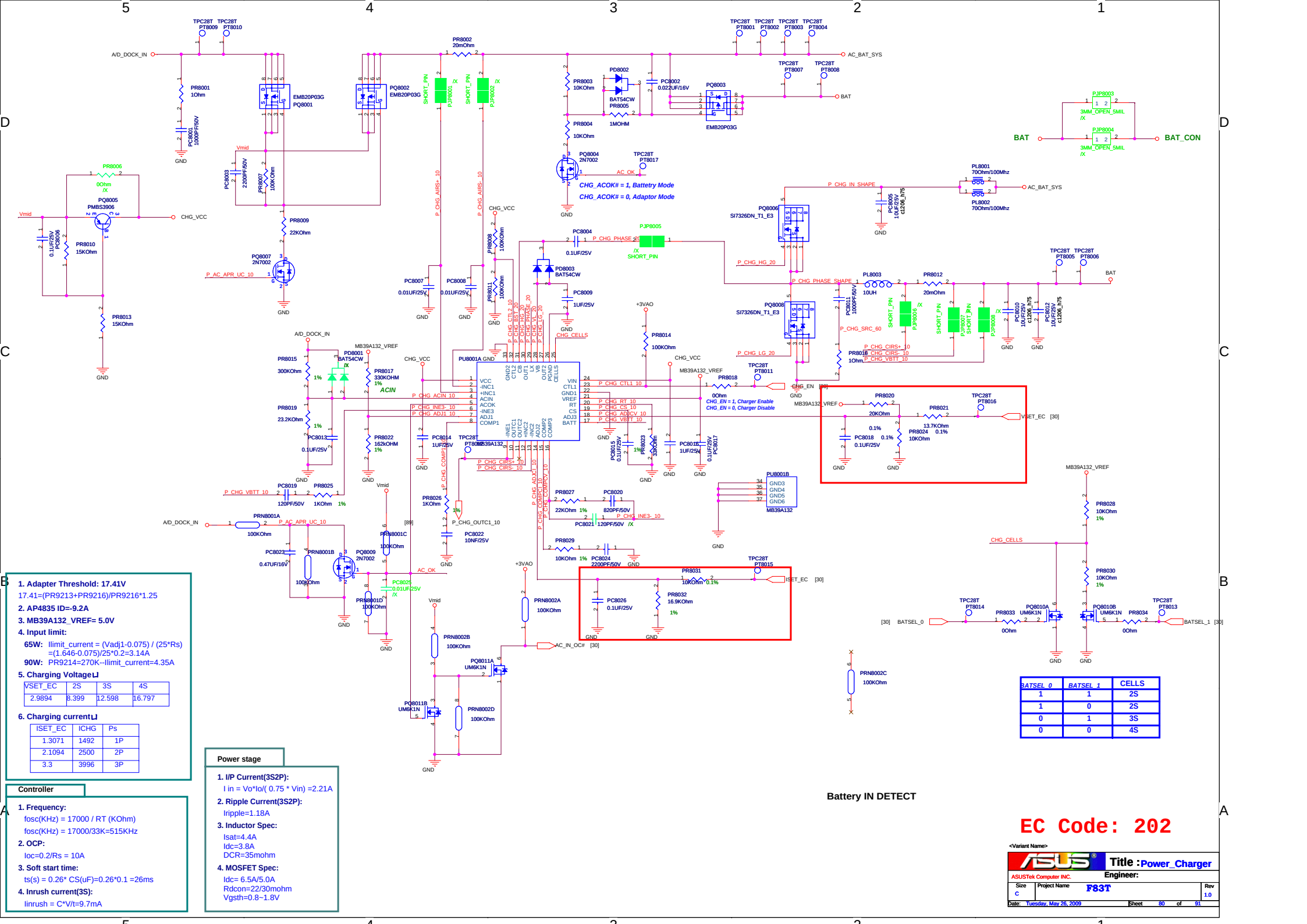

(5.4A/3.44A)
POWER CHARGER
A/D_DOCK_IN
AP4835*2 (SWITCH)
AC_BAT_SYS
MB39A132 (Controllor)
BAT
AP4835 SWITCH
AC_BAT_SYS
BATSEL_0;BATSEL_1;
ISET_EC;VSET_EC;CHG_EN
AC_IN_OC#
AC_BAT_SYS
UP6111 RJK0355*1+RJK0349*2
CPU_VRON_PWR
+VCORE
(15A)
+12V
(0.1A)
UMC4N
SUSB_EC#
+12VS(0.102A)
SI7326 (SWITCH)
SUSB_EC#
+5VS (2.46/1.36A)
+5VA
RT8205
5VSUS:SI7326+RJK0355
3VSUS:SI7326+SI7326
+3VAO (EC)(0.1A)
+3VA
+5VO (7.5A/3A)
+5V
VSUS_ON
+3VSUSO (4.2A/1.6A)
SI7326 (SWITCH)
SUSB_EC#
+3VS
UP7714
SUSB_EC#
+2.5V_CPU_VDDA (0.05/0.03A)
+3VSUS
(0.54/0.38A)
2N7002 (SWITCH)
SUSB_EC#
+0.9VS
UP7711
+0.9V (0.748/0.417A)
UP6111 RJK0355+RJK0355
SUSC_EC#
+1.8VO (12.2A/4.76A)
UP7706
SUSB_EC#
+1.5VS (1.06/0.8A)
SI7326 (SWITCH)
SUSC_EC#
+1.8VS
(0.8A/0.43A)
+1.8V
+1.1V_VGA
+1.1V_NB
RJK0355 SWITCH
+VCC_NB (5A/3A)
(6.08A/4.73)
+1.2VSUSO
CPU_VRON_PWR
UP6111 RJK0355+RJK0355
VSUS_ON
SI7326 SWITCH
CPU_VRON
+1.2V_CPU_NB_SB
(2.4A/1.75A)
+1.2VSUS
UP6111 RJK0355+RJK0355
SUSB_EC#
VGA_CORE
(12A/10A)



1. Adapter Threshold: 17.41V

17.41=(PR9213+PR9216)/PR9216*1.25

2. AP4835 ID=-9.2A

3. MB39A132_VREF= 5.0V

4. Input limit:

65W: Ilimit_current = (Vadj1-0.075) / (25*Rs)
=(1.646-0.075)/25*0.2=3.14A

90W: PR9214=270K--Ilimit_current=4.35A

5. Charging Voltage

VSET_EC	2S	3S	4S
2.9894	8.399	12.598	16.797

6. Charging current

ISET_EC	ICHG	Ps
1.3071	1492	1P
2.1094	2500	2P
3.3	3996	3P

Controller

1. Frequency:

fosc(KHz) = 17000 / RT (KOhm)

fosc(KHz) = 17000/33K=515KHz

2. OCP:

Ioc=0.2/Rs = 10A

3. Soft start time:

ts(s) = 0.26* CS(uF)=0.26*0.1 =26ms

4. Inrush current(3S):

Iinrush = C*V/t=9.7mA

Power stage

1. I/P Current(3S2P):

I in = Vo*Io/(0.75 * Vin) =2.21A

2. Ripple Current(3S2P):

Iripple=1.18A

3. Inductor Spec:

Isat=4.4A
Idc=3.8A
DCR=35mohm

4. MOSFET Spec:

Idc= 6.5A/5.0A
Rdcon=22/30mohm
Vgsth=0.8~1.8V

BATSEL_0	BATSEL_1	CELLS
1	1	2S
1	0	2S
0	1	3S
0	0	4S

Battery IN DETECT

EC Code: 202

<Variant Name>

Title : Power_Charger

ASUSTek Computer INC. Engineer:

Size	Project Name	Rev
C	F83T	1.0

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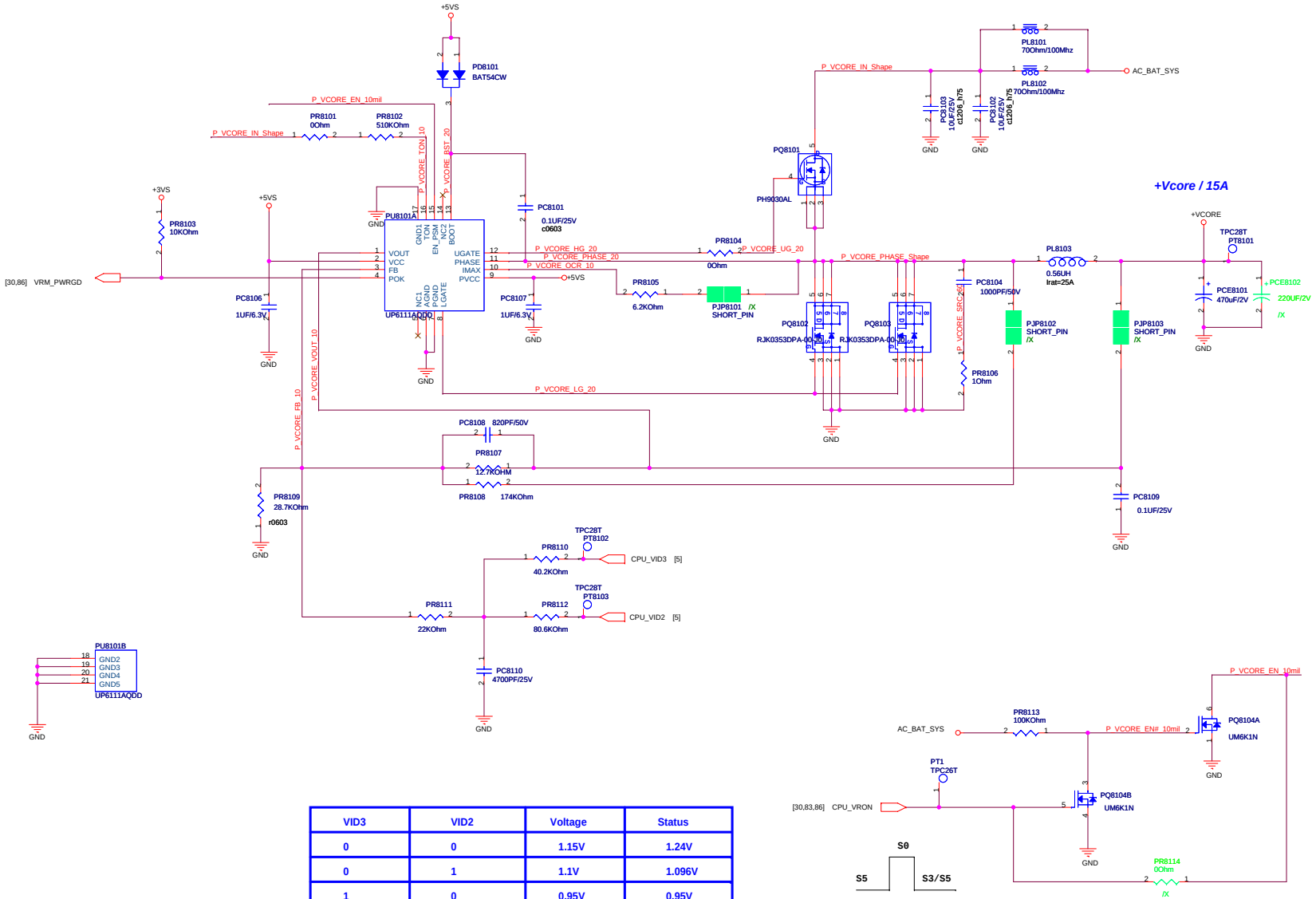


VID3	VID2	Voltage	Status
0	0	1.15V	1.24V
0	1	1.1V	1.096V
1	0	0.95V	0.95V
1	1	0.8V	0.805V

Controller

1. Voltage & Current:

   VCORE: 15A

2. Frequency:

   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ

3. OCP:

   SetPR8105=12K
   Iocp=Rocp*20/Rds(on)=12*20/7.6=31.6A

4. Soft start time:

   Soft-Star duration is 1.35ms

5. Inrush Current:

   C total =470UF
   I inrush=0.38A

Power stage

1. I/P Current:

   I in = Vo*Io/(0.75 * Vin) =1.16A

2. Ripple Current:

   Iripple=3.5A

3. Dynamic:

   Ipeak=15A
   ESR=9mohm
   V=122mV

4. Inductor Spec:

   Isat=40A
   Idc=25A
   DCR=1.6mohm

5. MOSFET Spec:

   L-side MOSFET:
   Rds(on)max=7.6mOhm
   (Vgs=4.5V)
   Icont=35A (T=25)
   Ipeak=140A (Pause<10us)

<Variant Name>

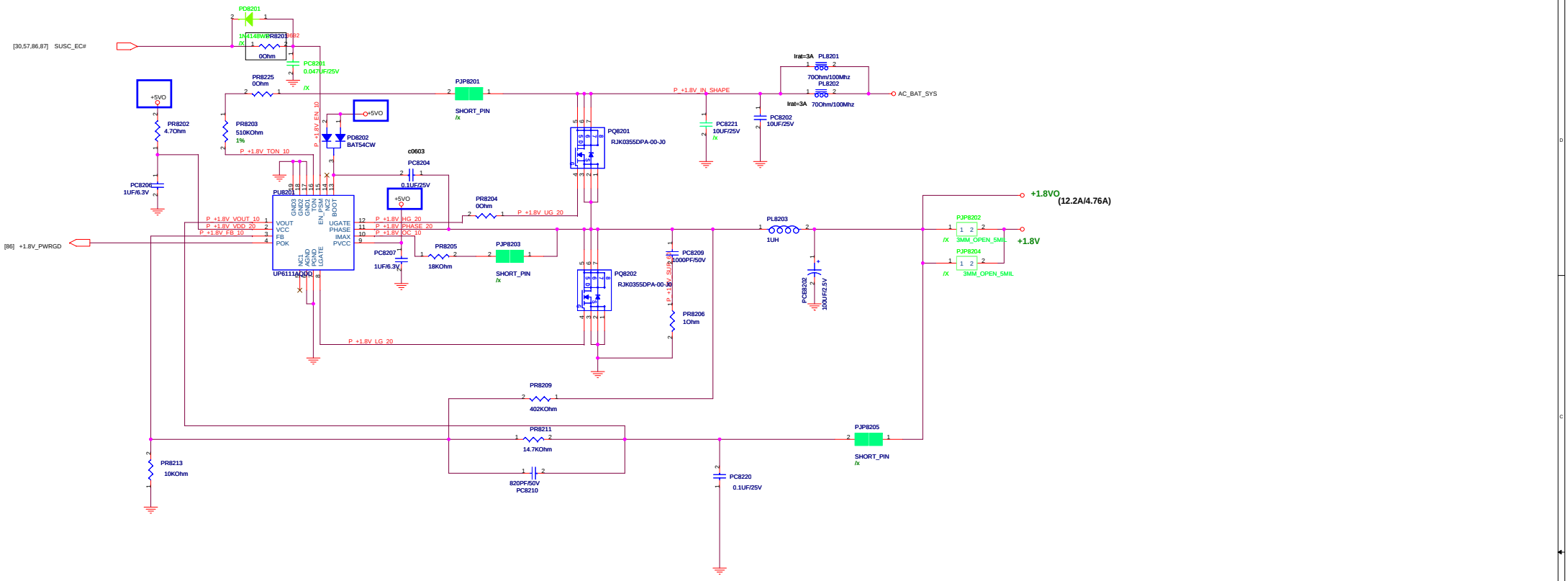
ASUSTeK COMPUTER INC

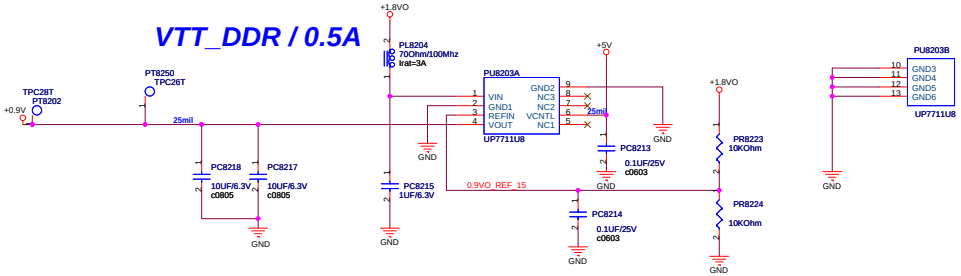
Title : Power_VCORE

Engineer:

Size	Project Name	Rev
C	F83T	1.0

Date: Tuesday, May 26, 2009 Sheet 81 of 91





Controller

1. Voltage & Current:
   +1.8V:+1.8V&8A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR7343=18kohm
   Iocp=Rocp*20/Rds(on)
   =20*18/16.5=21.8A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =100uF
   I
   inrush=0.133A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =0.947A
2. Ripple Current:
   Iripple=2.342A
3. Ripple Voltage:
   Ipeak=(vin-vo)*D/(L*Fsw)=3.25A
   ESR=18mohm
   V=58.5mV
4. Inductor Spec:
   Isat=22A
   Idc=11A
   DCR=9mohm
5. MOSFET Spec:
   H-side and L-side MOSFET:
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

<Variant Name>

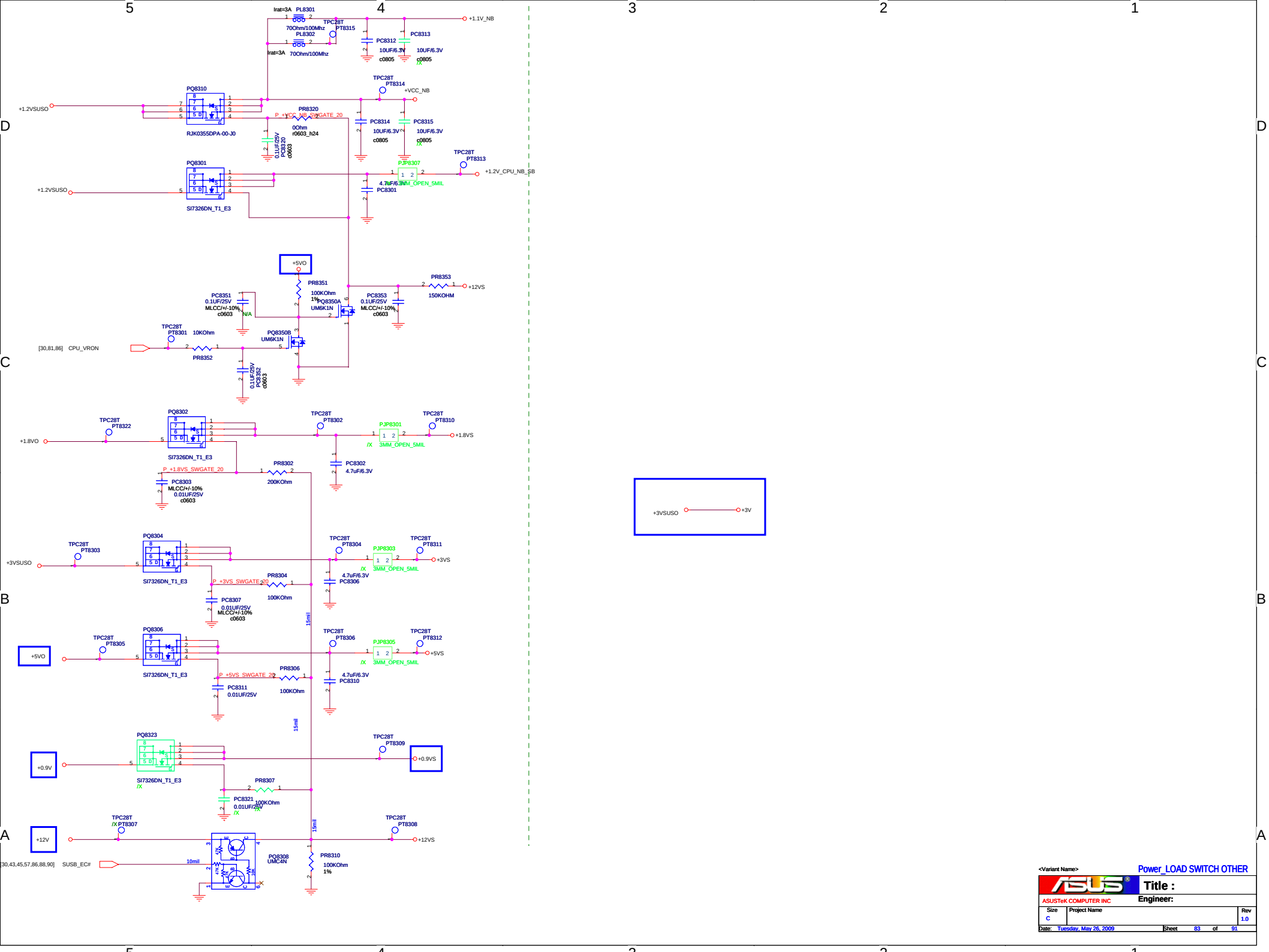
ASUSTeK COMPUTER INC

Title : Power_+1.8V&+0.9V

Engineer:

Size	Project Name	Rev
A2		1.0

Date: Tuesday, May 26, 2009 Sheet 82 of 91


+1.1V_NB
+VCC_NB
+1.2VSUSO
+1.2V_CPU_NB_SB
+5VO
+12VS
+1.8VO
+1.8VS
+3VSUSO
+3V
+3VS
+5VS
+0.9V
+0.9VS
+12V
[30,81,86] CPU_VRON
[30,43,45,57,86,88,90] SUSB_EC#
PL8301
PL8302
70Ohm/100Mhz
Irat=3A
TPC28T PT8315
PC8312
PC8313
10UF/6.3V
c0805
PQ8310
RJK0355DPA-00-J0
PR8320
0Ohm
r0603_h24
P_+VCC_NB_SWGATE_20
PC8314
PC8315
PQ8301
SI7326DN_T1_E3
PJP8307
3MM_OPEN_5MIL
PC8301
4.7uF/6.3V
PR8351
100KOhm
1%
PQ8350A
UM6K1N
PQ8350B
PC8351
0.1UF/25V
MLCC/+/-10%
N/A
PC8353
PR8353
150KOHM
PR8352
10KOhm
PQ8302
PJP8301
PC8302
PR8302
200KOhm
P_+1.8VS_SWGATE_20
PC8303
0.01UF/25V
PQ8304
PJP8303
PR8304
100KOhm
P_+3VS_SWGATE_20
PC8307
PC8306
PQ8306
PJP8305
PR8306
P_+5VS_SWGATE_20
PC8311
PC8310
PQ8323
PR8307
PC8321
PR8310
PQ8308
UMC4N
10mil
15mil
TPC28T PT8322
TPC28T PT8302
TPC28T PT8310
TPC28T PT8303
TPC28T PT8304
TPC28T PT8311
TPC28T PT8305
TPC28T PT8306
TPC28T PT8312
TPC28T PT8309
TPC28T PT8307
TPC28T PT8308
TPC28T PT8313
TPC28T PT8314

<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
A		1.0

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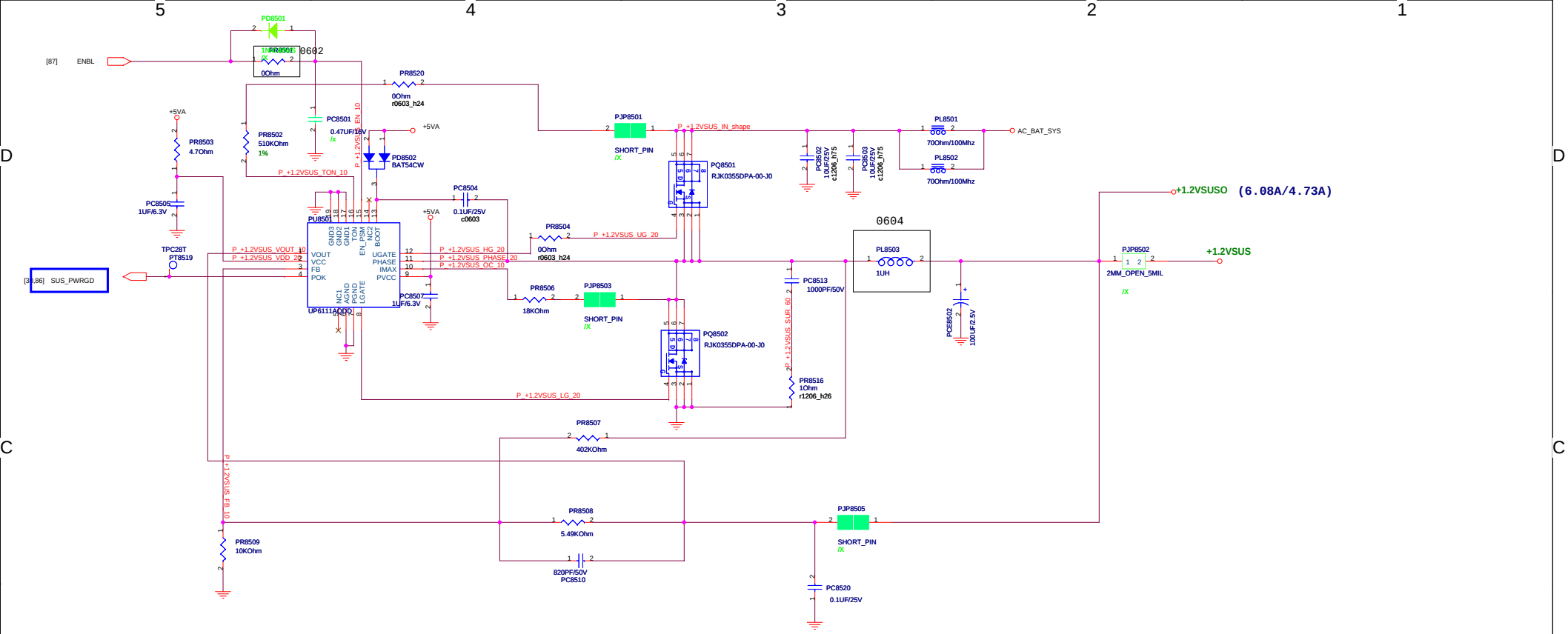


Controller

1. Voltage & Current:

   +1.2VSUS:1.16V&12A

2. Frequency:

   Ton=3.85p*Rt(on)*Vo/Vin-05
   Frequency=Vout/(Vin*Ton)
   =500KHZ

3. OCP:

   Set PR7343=18Kohm
   Iocp=Rocp*20/Rds(on)=21.9A

4. Soft start time:

   Soft-Star duration is 1.35ms

5. Inrush Current:

   C total =100uF
   I inrush=0.133A

Power stage

1. I/P Current:

   I in = Vo*Io/(0.8 * Vin) =0.915A

2. Ripple Current:

   Iripple=2.915A

3. Ripple Voltage:

   Ipeak=(Vin-Vo)*D/(L*Fsw)=2.24A
   ESR=18mohm
   V=40.32mV

4. Inductor Spec:

   Isat=22A
   Idc=11A
   DCR=9mohm

5. MOSFET Spec:

   H-side and L-side MOSFET:
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

<Variant Name>

ASUSTeK COMPUTER INC

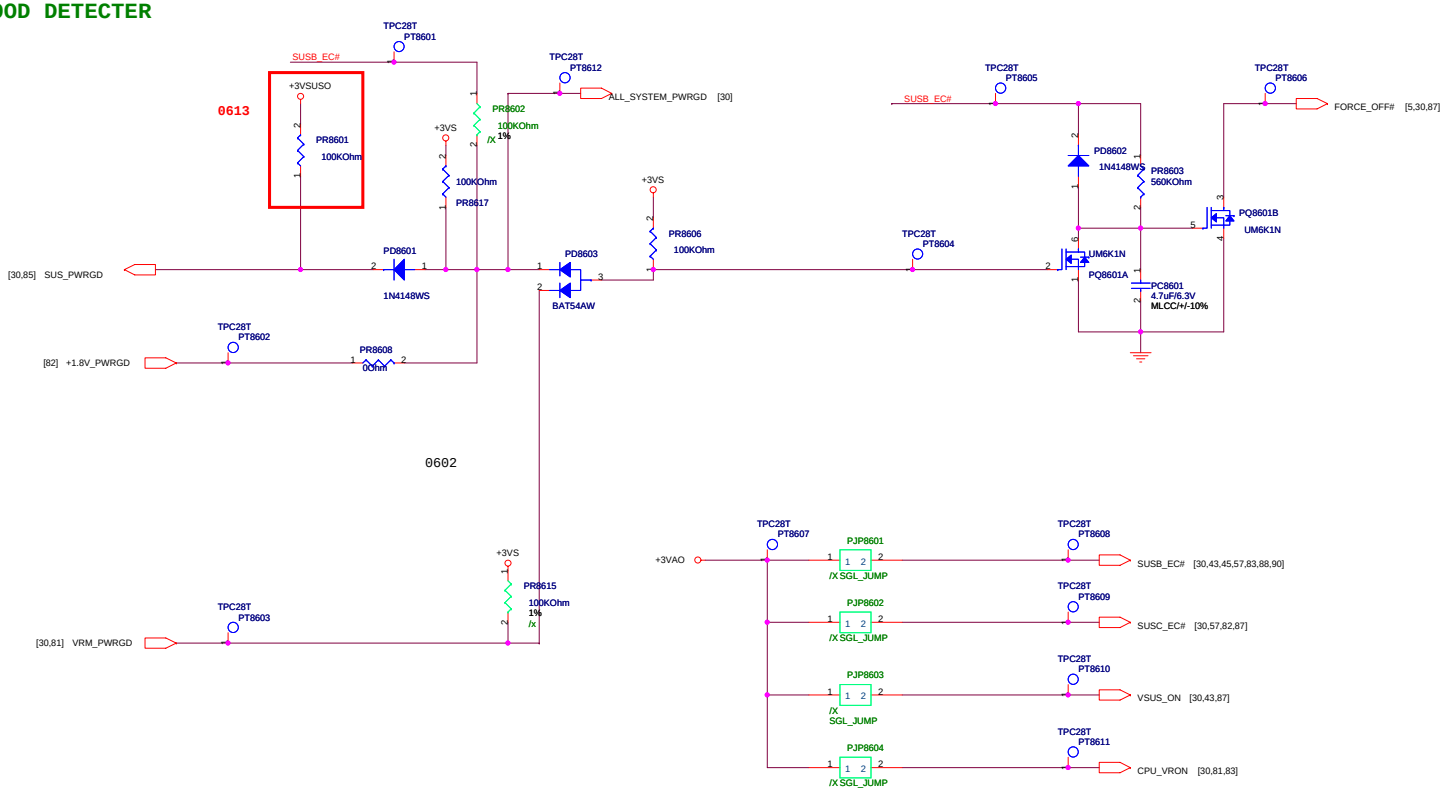
Title : Power_1.2VSUS

Engineer:

Size	Project Name	Rev
C		1.0

Date: Tuesday, May 26, 2009 Sheet 85 of 91

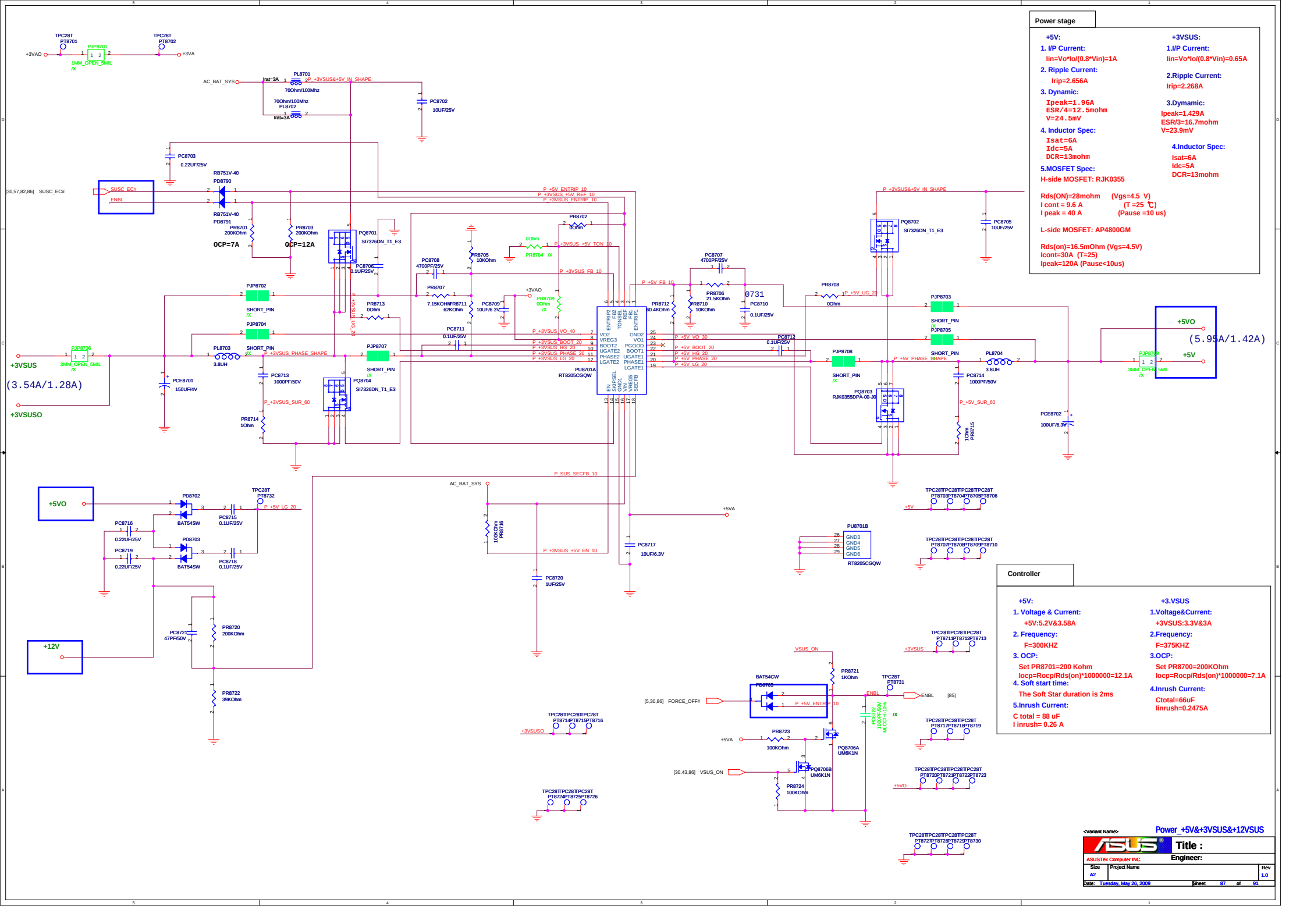
POWER GOOD DETECTER

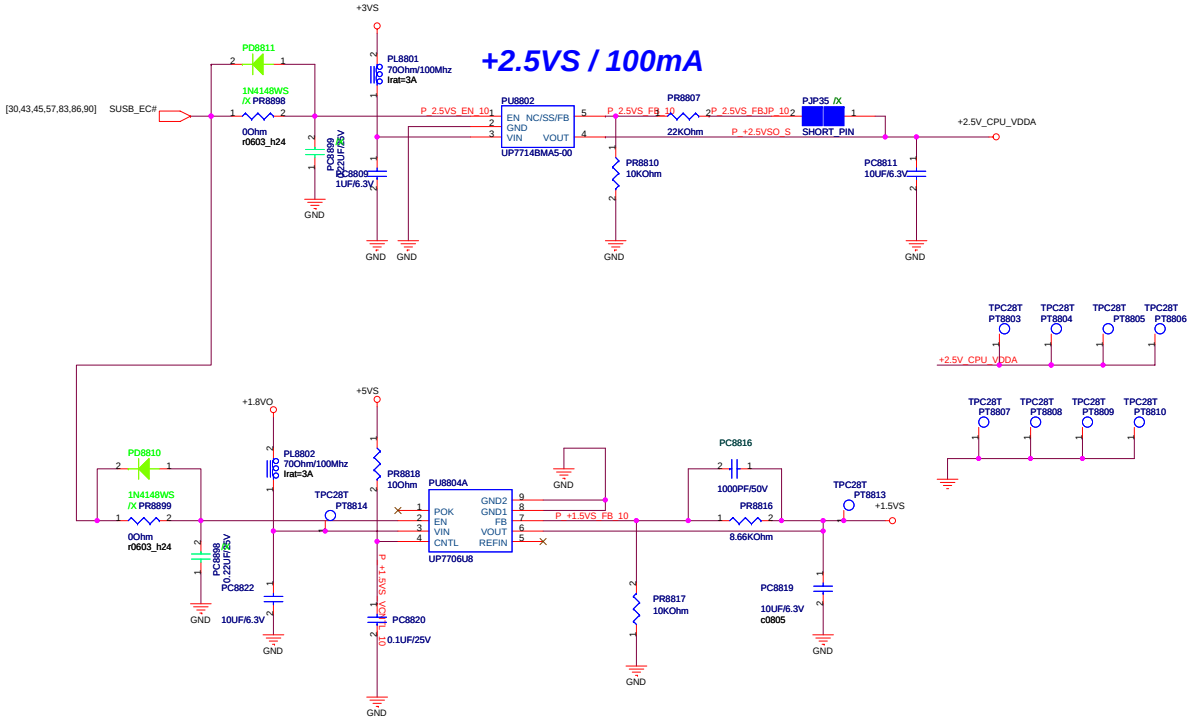


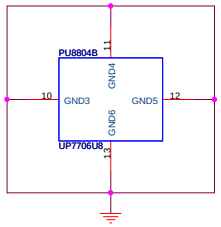
<Variant Name>

Power_GOOD_DETECTER

ASUSTeK COMPUTER INC	Title :	
	Engineer:	
Size: C	Project Name: F83T	Rev: 1.0
Date: Tuesday, May 26, 2009	Sheet 86 of 91	


Power stage
+5V:
1. I/P Current:
Iin=Vo*Io/(0.8*Vin)=1A
2. Ripple Current:
Irip=2.656A
3. Dynamic:
Ipeak=1.96A
ESR/4=12.5mohm
V=24.5mV
4. Inductor Spec:
Isat=6A
Idc=5A
DCR=13mohm
5.MOSFET Spec:
H-side MOSFET: RJK0355
Rds(ON)=28mohm (Vgs=4.5 V)
I cont = 9.6 A (T =25 ℃)
I peak = 40 A (Pause =10 us)
L-side MOSFET: AP4800GM
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)
+3VSUS:
1.I/P Current:
Iin=Vo*Io/(0.8*Vin)=0.65A
2.Ripple Current:
Irip=2.268A
3.Dymamic:
Ipeak=1.429A
ESR/3=16.7mohm
V=23.9mV
4.Inductor Spec:
Isat=6A
Idc=5A
DCR=13mohm
Controller
+5V:
1. Voltage & Current:
+5V:5.2V&3.58A
2. Frequency:
F=300KHZ
3. OCP:
Set PR8701=200 Kohm
Iocp=Rocp/Rds(on)*1000000=12.1A
4. Soft start time:
The Soft Star duration is 2ms
5.Inrush Current:
C total = 88 uF
I inrush= 0.26 A
+3.VSUS
1.Voltage&Current:
+3VSUS:3.3V&3A
2.Frequency:
F=375KHZ
3.OCP:
Set PR8700=200KOhm
Iocp=Rocp/Rds(on)*1000000=7.1A
4.Inrush Current:
Ctotal=66uF
Iinrush=0.2475A
+3VSUS
(3.54A/1.28A)
+5VO
(5.95A/1.42A)
+5V
+12V
OCP=7A
OCP=12A
SUSC_EC#
ENBL
FORCE_OFF#
VSUS_ON
AC_BAT_SYS
Power_+5V&+3VSUS&+12VSUS
ASUSTek Computer INC.
Engineer:
Project Name
Tuesday, May 26, 2009





2.5V @ 0.1A

1. Dropout Voltage:

△V = 0.21V (Io =0.3A)

2. Current Limit:

I limit =320mA

3. Continue Current:

I cont =
300mA

4. Power Dissipation:

Rthjc = 250℃/W
Pd = 0.4W

5. EN Voltage:

V rising = 2V
V falling =
0.8V

6. Supply Voltage:

Vcc =3V

7. Inrush current:

T ss = 400us
C total =10uF
I inrush =
0.063A

<Variant Name>

Power +2.5V&+1.5VS&+1.1V_NB

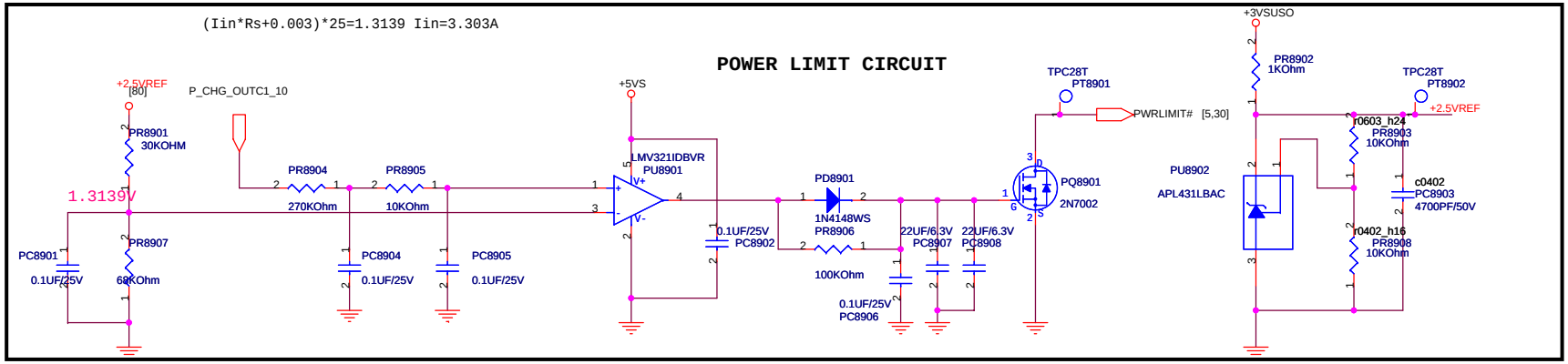
ASUSTek Computer INC.

Title :

Engineer:

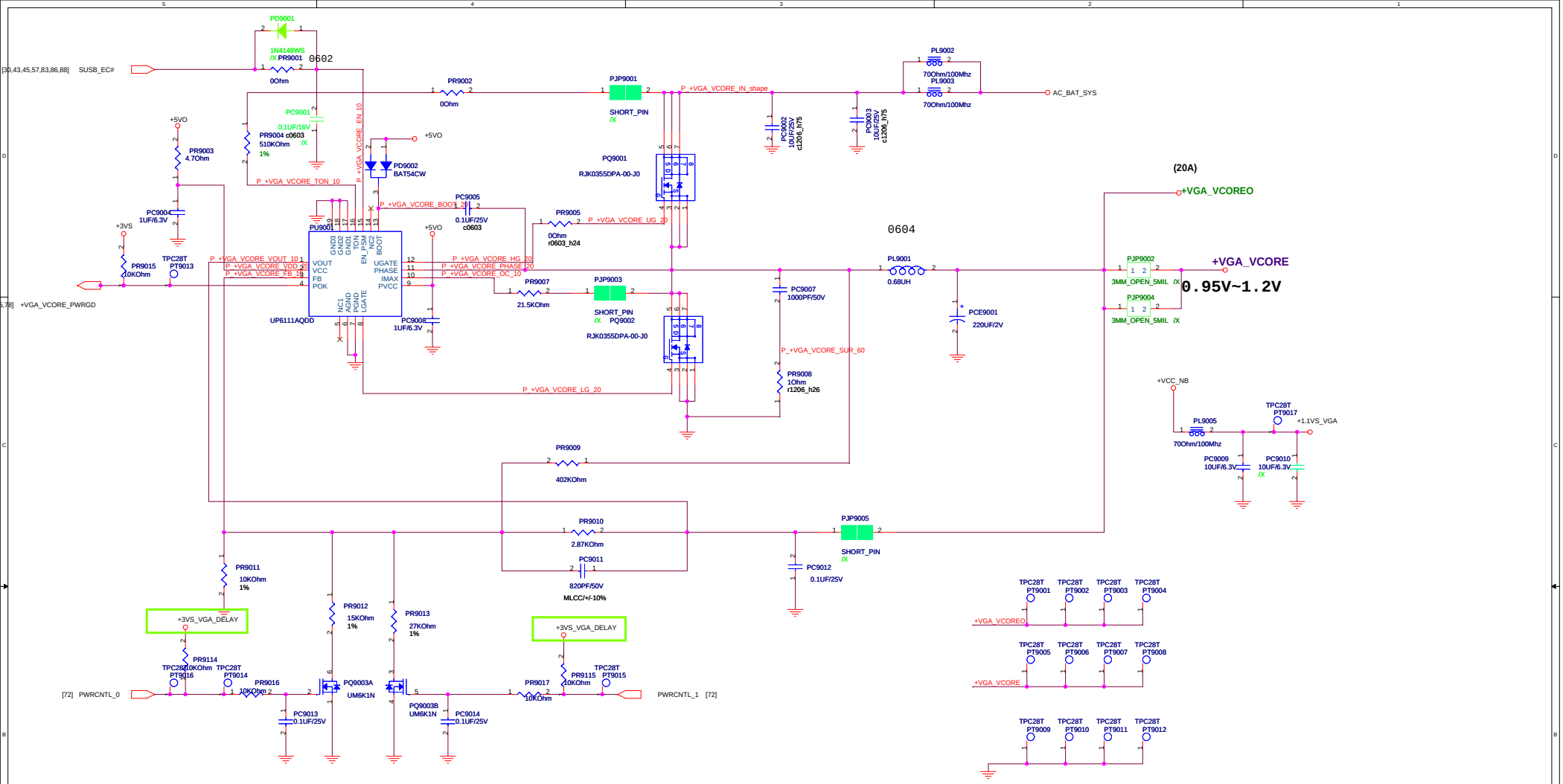
Size	Project Name	Rev
C	F83T	1.0

Date: Tuesday, May 26, 2009 Sheet 88 of 91



<Variant Name>

ASUSTek Computer INC.	Title : Power_Charger	
	Engineer: Limy_li	
Size: A3	Project Name: F83T	Rev: 2.1G
Date: Tuesday, May 26, 2009	Sheet 89 of 91	



PWRCNTL_0	PWRCNTL_1	VGA_VCORE	
0	0	0.964	-5%
0	1	1.043	Normal
1	0	1.106	+5%
1	1	1.185	+10%

Controller

1. Voltage & Current:

   +1.2VSUS: 16A

2. Frequency:

Ton=3.85p*Rt(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)
=500KHZ

3. OCP:

   Set PR8506=21.5kohm
   Iocp=Rocp*20/Rds(on)=26A

4. Soft start time:

   Soft-Star duration is 1.35ms

5.Inrush Current:

   C total =220uF
   I
   inrush=0.163A

Power stage

1. I/P Current:

   I in = Vo*Io/(0.75 * Vin) =0.85A

2. Ripple Current:

   Iripple=3.74A

3. Dynamic:

   Ipeak=6.1A
   ESR/2=4.5mohm
   V=27.5mohm

4. Inductor Spec:

   Isat=25A
   Idc=15.5A
   DCR=5.5mohm

5. MOSFET Spec:

H-side and L-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_+VGA_VCORE

Engineer:

Size	Project Name	Rev
C		1.0

Date: Tuesday, May 26, 2009 Sheet 90 of 91

Date:05/19/09

1.Del PQ8012&PR8035&PC8027 in 80_Powe_charge

Date:05/21/09

1.Chagne VCORE H-S MOS PQ8101 to PH9030AL

<Variant Name>

ASUSTeK COMPUTER INC	Title : Power_History	
	Engineer:	
Size: A	Project Name	Rev: 1.0
Date: Tuesday, May 26, 2009	Sheet 91 of 91	