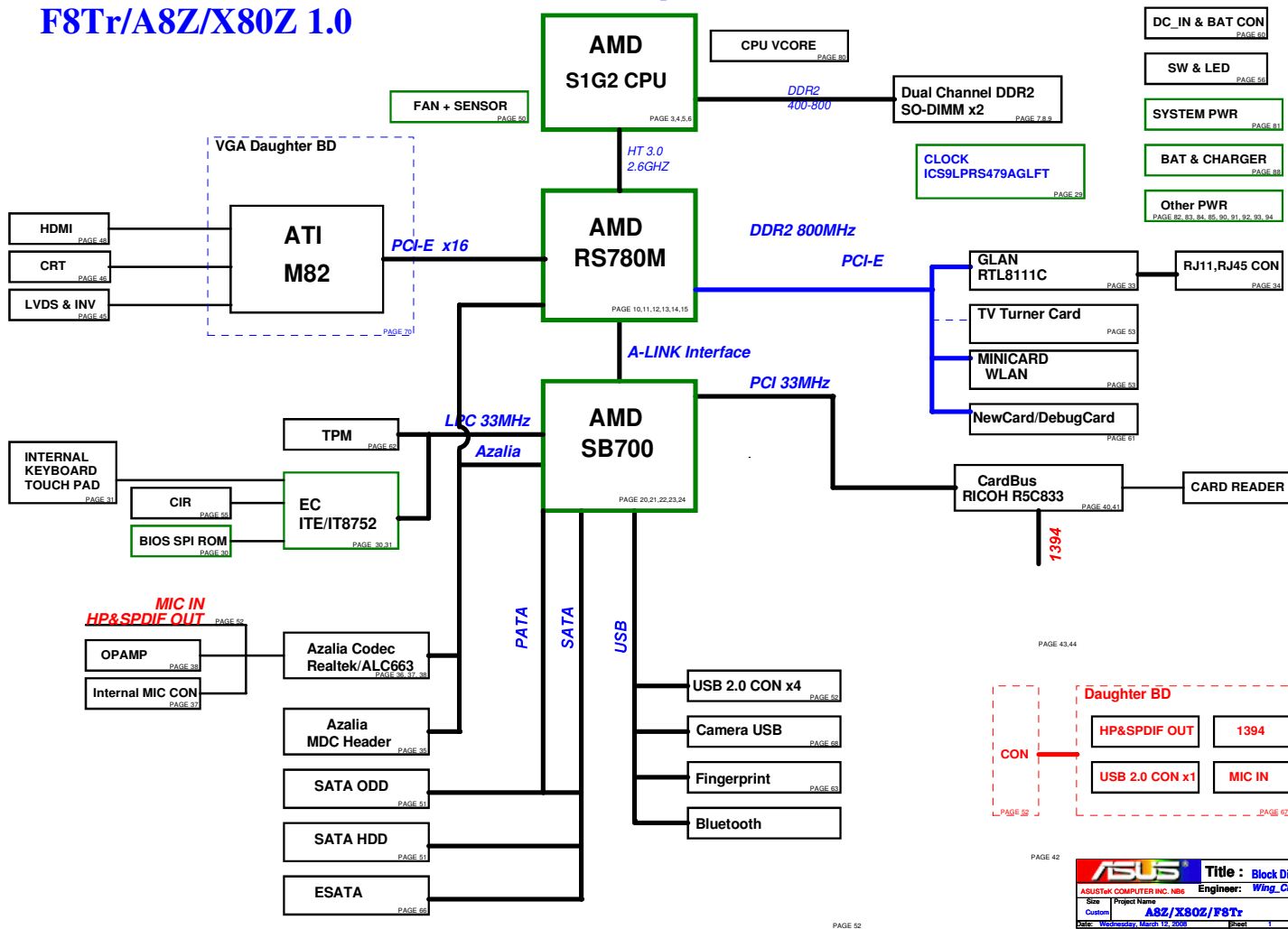


Block Diagram

F8Tr/A8Z/X80Z 1.0



ASUS		Title : Block Diagram	
ASUSTek COMPUTER INC. H86		Engineer: Wing_Cheng	
Size	Project Name	Rev	
Custom	ASZ/X80Z/F8Tr	0.1	
Date: Wednesday, March 18, 2009	Sheet	1	of 8

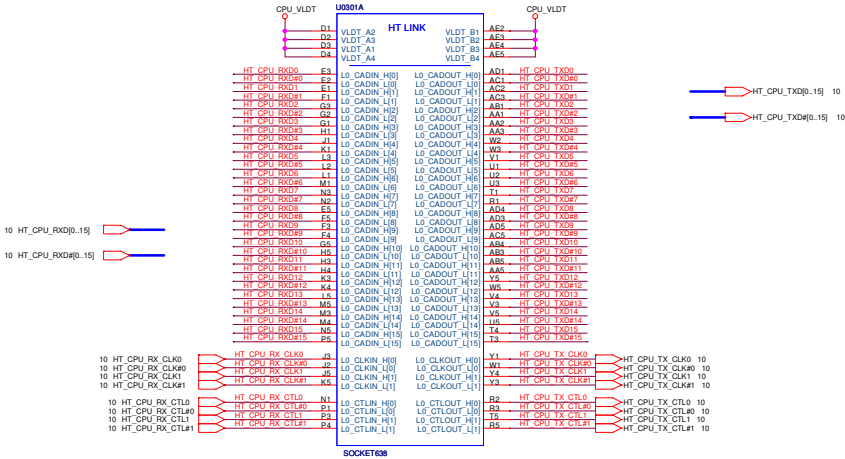
<< MaryL_Liu >>

81124	REMOVE R6054 to 6441
81125	add ahead4 make4 signal pull up p44
	change enable to 100K
	change P2P310 because 120K is not meet
	change P4 led circuit p44
	del R0M data signal ESD protect, add
	del R0M chip
	del ESD protection link to connect
	rearrange R0M resistor between
	P24-02 add by_0V2R4 P22
	remove P2834 P2832
81128	remove 100 ohm inductor capacitors C6300 C6301
	add C6C120R1P1V_1.0V P6
	del P2B_P2B_P_ESD protect P20
	rearrange C6C120R1P1V to 3R10
81129	change trace to serial resistor from 4.99k to 4.9k
	add 4990 GP10 PD P6
	change value
	add PD cap for 20
81132	add C6C120R1V100V ESD protect
	change CR POWER from R0M
	connect power to VCC on R0M1
	add delay 66F and 66F
81133	change CR power connection
81134	add R4801
	add netname+V505 R2010,V505 R2010,RP 10M1
	change net+V505R2010
	change connector pin1 and from 2 to 3
	change R2010 P76
81105	del R-5018 pin1,pin11 link to GND
	add R4201,R4203
	del ADD R3719,Q3718
	del ADD R3121,2115,2111,2111 FOR SMOUA
	del change c4011 to 1uF
	del ADD Q1401,R1205,R1209
	del change R2008 to 22 ohm
	del change fingerprint to usb11
	del change R2010 on camera and P4_PNB06 sequence
	del add EMI cap on page 20 and page 29 for pci and 14M/48M clk
	del add receiver for R-DATA
	del ADD C4208* FOR EMI
	del ADD R2025 FOR EMI
	del RESERVE P3118
	del change R1201,R1202,R1205
	del add c5210
	del add R2002 for netnew
81103	del R-4 to 10 ohm
	change W2118 to G1008 add R5104
	change C2102 100K to 10K
	del R1201 R1204 R1205
	del R4610 R4619 R4611 from 4700M/100M to 470K
	del R4611 R4612 R4613 470F
	del R4621 R4622 R4623 50F
	del C4618 C4619 C4620 from 47pF to 5pF and option change to /X
	del R4602 R4601 from 3300M to 2700M
	del R4602 from 1000M to 1400M for R3780 A13
	del C4602 C4603 C4604 from 47pF to 5pF
	del R4604 R4601 R4602 R4603
	del R4605
	del R4610 R4614 C4621 C4622 C4623 C4624 option change to N/X
	del R4605 R4606 R4607 R4608
	del R4610 20000M
	del C46017 C46018 330pF and C4619 C46200.01uF
	del R2201 R2202 R2211 R2212 R2213 from 4.9500M to 500M
	del R2201 R2212 optional change to /X, R2213 change to N/A
	del R2204 optional change to /X
	del R2206 optional change to N/A
	del R2207 optional change to /X
	del R2208 optional change to /X
	del R2209 optional change to /X
81104	change part number from 1201110000033 to 1201100000038
	del C501 optional to /X
	del R518 R519 optional to /X
81105	del C522 optional to /X
81106	del R10 P2P
	del R20P R21P R22P P6 to 100M/2000000110
	del R20P
	del R10-SM11 and P2P
	del 100000018 and GND
	del R4 PM to 450M/200011
	del R2 PM to 100M/10101110
	del 25503 optional to /X
81110	del R20M C201
	R1222 optional to N/A
	R1209, R1208, R1210, R1211, R1212, R1215,
	R1214, R1215 change to 4500M
	C2014 C2019 C2020 C2017 C2018 C2022
	change to 550 optional to N/A
	del C2025 optional to /X
81112	del R20M C2021 optional to /X
	del C2027 C2028 optional to /X

		Title :	
ASUSTeK COMPUTER INC. (NBI)		Engineer: <OrgAddrs>	
Doc	Project Name	Rev	
Custom	ASZ/X80Z/F8Ty	1.1	
Date	Wednesday, March 16, 2005	Sheet	2 of 22

<< MaryL_Liu >>

1. 5A

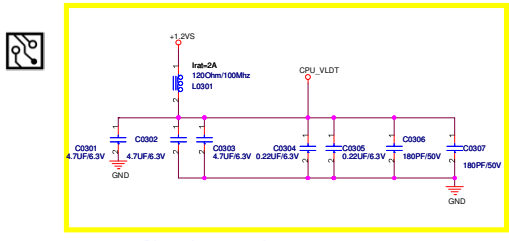


10 HT_CPU_RXD[0..15]
10 HT_CPU_RXD[0..15]

HT_CPU_TXD[0..15] 10
HT_CPU_TXD[0..15] 10

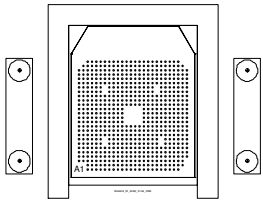
12G011306384 071113

Do not cross plane.



Place close to socket

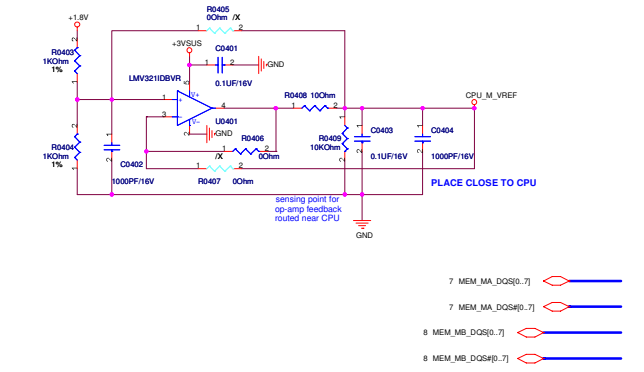
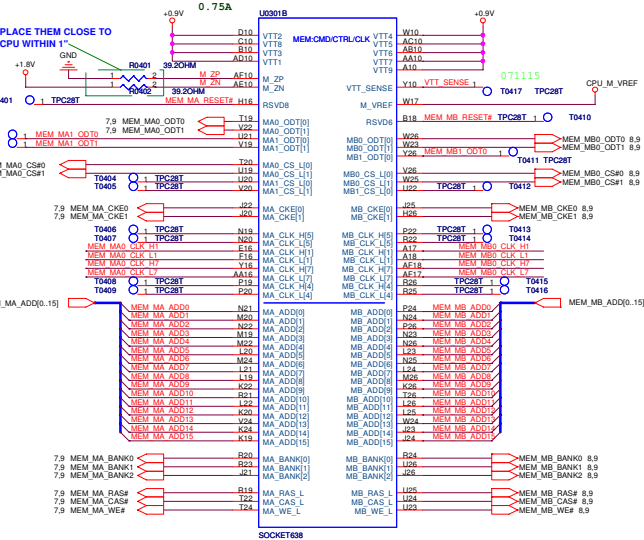
* If VLDT is connected only on one side, one 4.7UF cap should be added to the other side



ASUS		Title : Griffin HT I/F	
ASUSTek Computer INC		Engineer: <OrgAddri>	
Size	Project Name	Rev	
Custom	ABZ/X80Z/F8Tt	0.1	
Date: Wednesday, March 19, 2008	Sheet	3	of 08

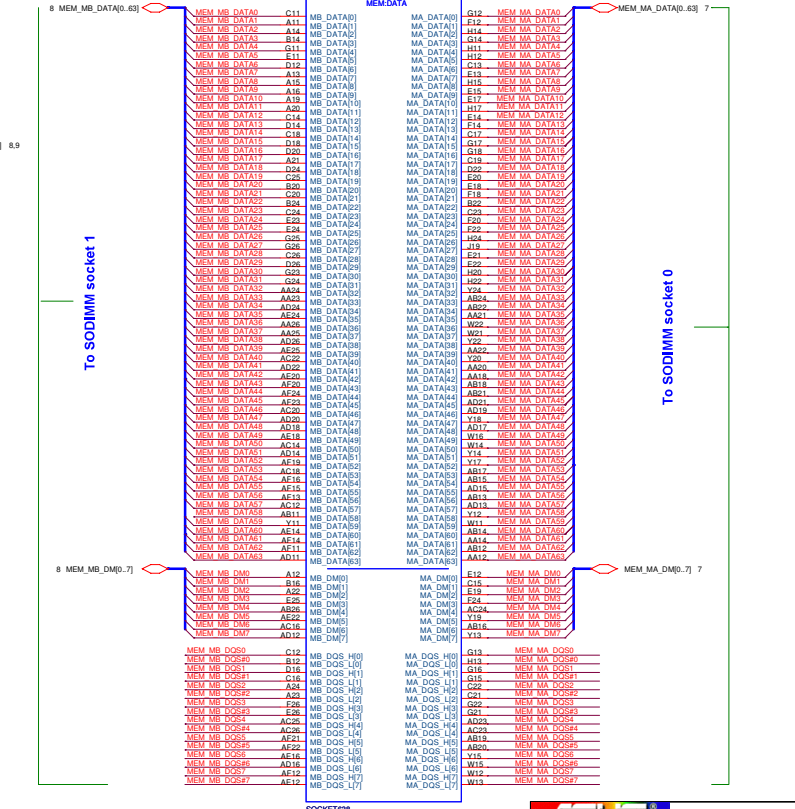
<< MaryL_Liu >>

place close to PROCESSOR within 1.5 inch



- 7 MEM_MA_DQS#0..7
- 7 MEM_MA_DQS#1..7
- 8 MEM_MB_DQS#0..7
- 8 MEM_MB_DQS#1..7

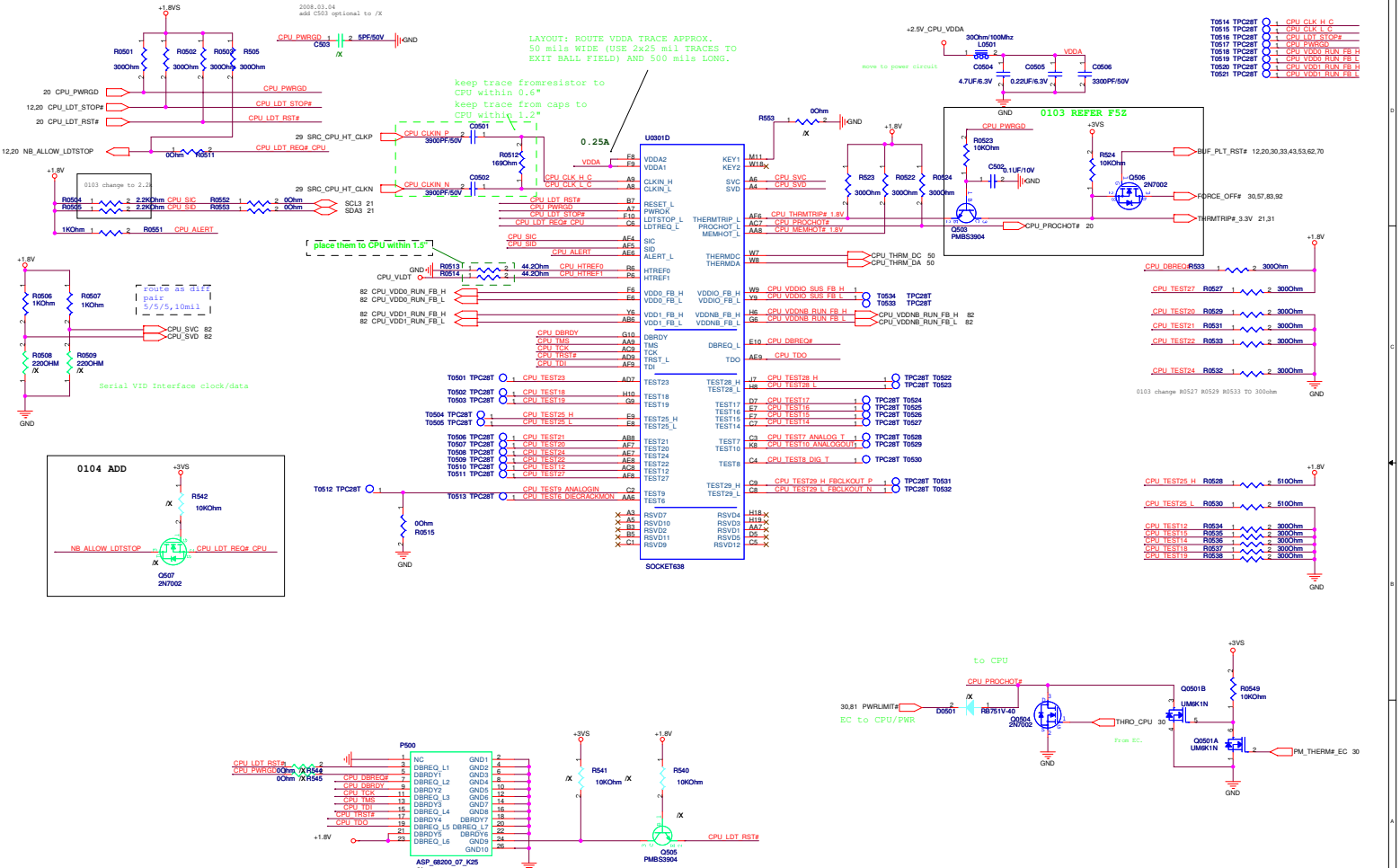
Processor Memory Interface



- 7 MEM_MA_DQS#0..7
- 7 MEM_MA_DQS#1..7
- 8 MEM_MB_DQS#0..7
- 8 MEM_MB_DQS#1..7

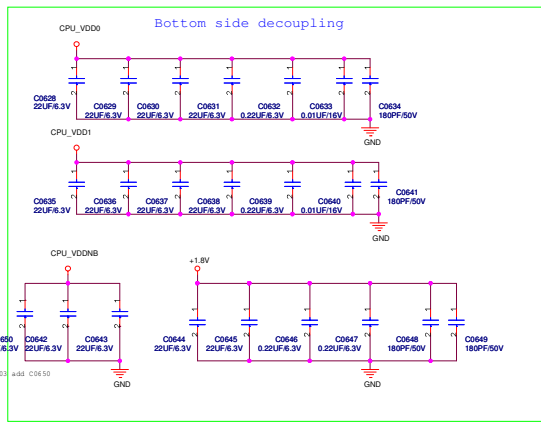
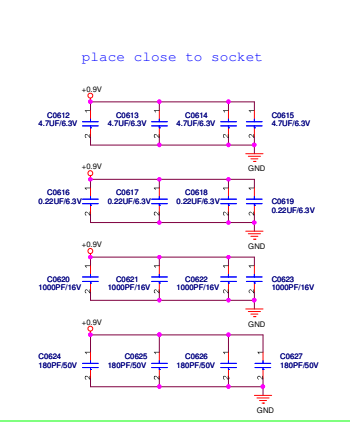
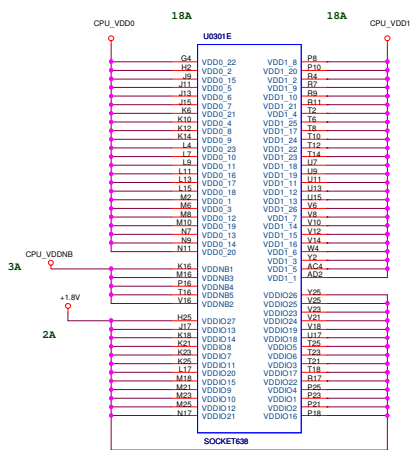
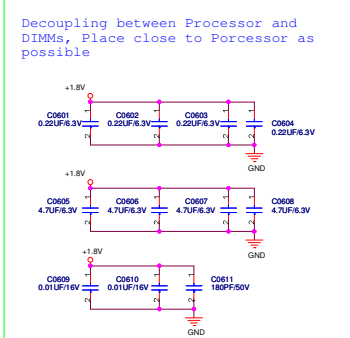
ASUS Title: Griffin DDR2 MEM I/F
 ASUSTek Computer, Inc. Engineer: <OrgAdrr1>
 Size Project Name: ABZ / X80Z / F8T Rev: 0.1
 Date: Wednesday, March 19, 2008 Sheet 4 of 8

<< MaryL_Liu >>

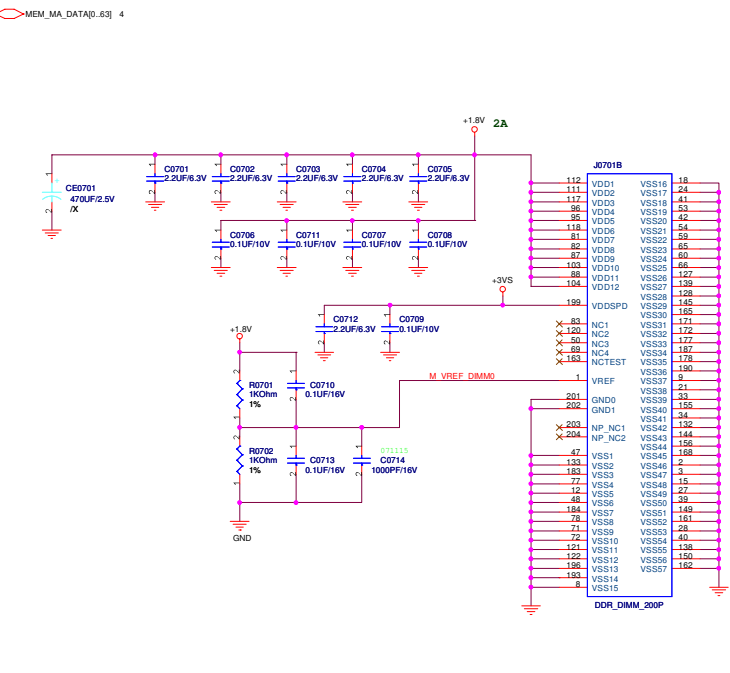
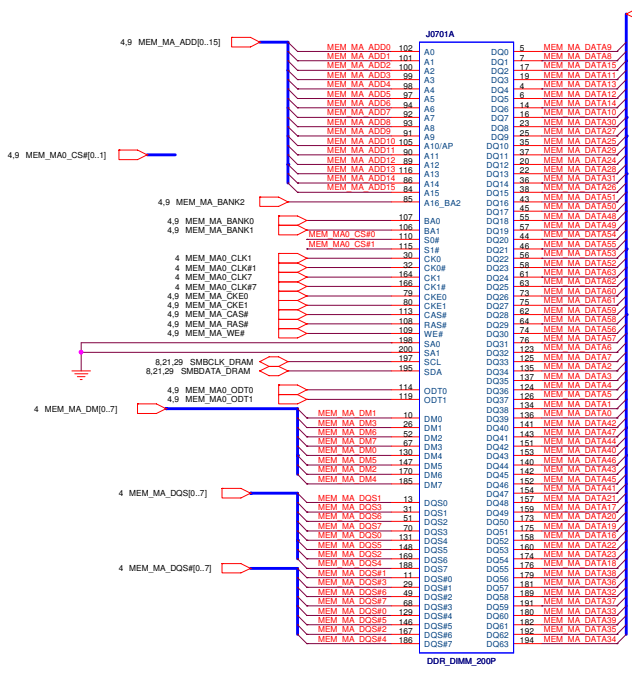


<< MaryL_Liu >>

U0301F	
AA4	VSS49
AA11	VSS128
AA15	VSS116
AA16	VSS115
AA17	VSS75
AA18	VSS26
AA19	VSS44
AA20	VSS79
AA21	VSS28
AA22	VSS46
AA23	VSS39
AA24	VSS38
AA25	VSS99
AA26	VSS35
AA27	VSS21
AA28	VSS29
AA29	VSS32
AA30	VSS33
AA31	VSS86
AA32	VSS85
AA33	VSS34
AA34	VSS83
AA35	VSS82
AA36	VSS74
AA37	VSS97
AA38	VSS91
AA39	VSS100
AA40	VSS101
AA41	VSS73
AA42	VSS36
AA43	VSS37
AA44	VSS84
AA45	VSS84
AA46	VSS88
AA47	VSS81
AA48	VSS80
AA49	VSS76
AA50	VSS122
AA51	VSS103
AA52	VSS104
AA53	VSS124
AA54	VSS72
AA55	VSS119
AA56	VSS53
AA57	VSS52
AA58	VSS105
AA59	VSS106
AA60	VSS23
AA61	VSS17
AA62	VSS107
AA63	VSS108
AA64	VSS109
AA65	VSS107
AA66	VSS108
AA67	VSS109
AA68	VSS107
AA69	VSS108
AA70	VSS109
AA71	VSS107
AA72	VSS108
AA73	VSS109
AA74	VSS107
AA75	VSS108
AA76	VSS109
AA77	VSS107
AA78	VSS108
AA79	VSS109
AA80	VSS107
AA81	VSS108
AA82	VSS109
AA83	VSS107
AA84	VSS108
AA85	VSS109
AA86	VSS107
AA87	VSS108
AA88	VSS109
AA89	VSS107
AA90	VSS108
AA91	VSS109
AA92	VSS107
AA93	VSS108
AA94	VSS109
AA95	VSS107
AA96	VSS108
AA97	VSS109
AA98	VSS107
AA99	VSS108
AA100	VSS109



<< MaryL_Liu >>



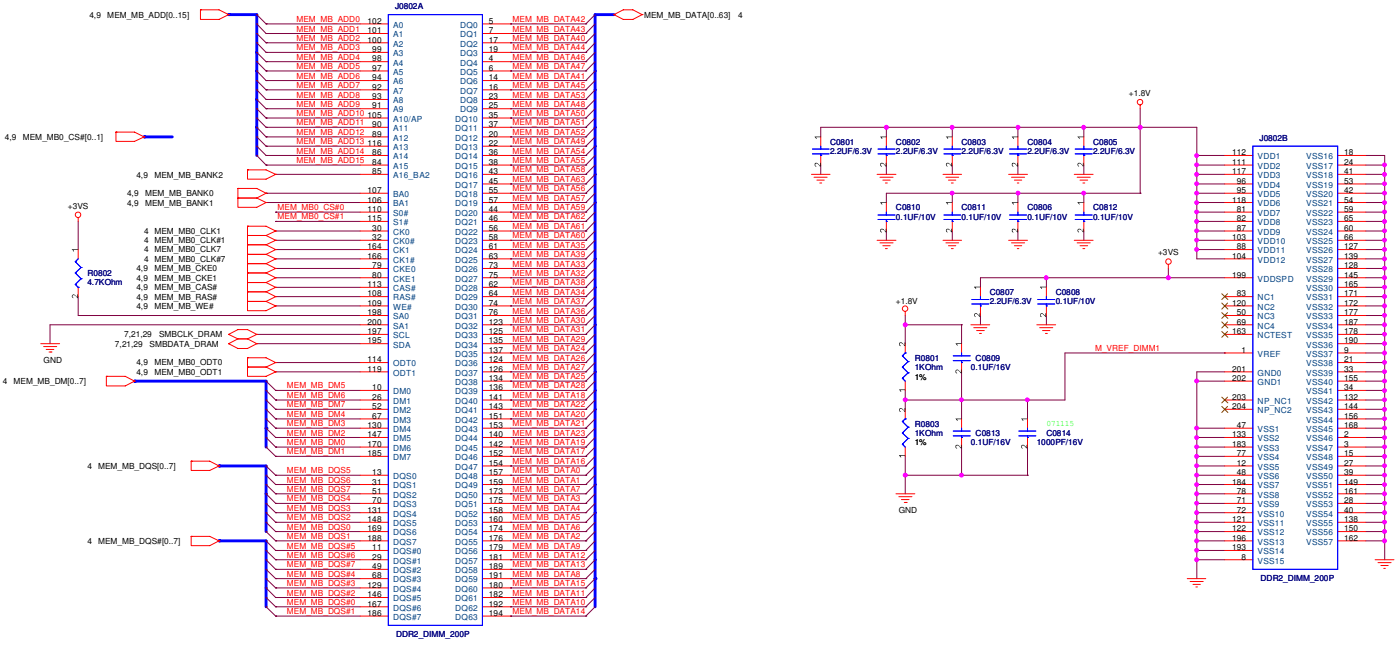
High

ASUS Title: DDR2 SO-DIMMO

ASUSTEK COMPUTER INC. Project Name: Custom ABZ/X80Z/F8T- Engineer: [Blank]

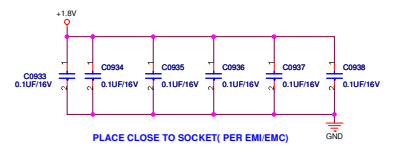
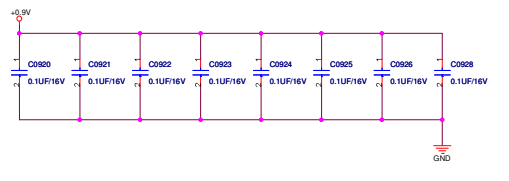
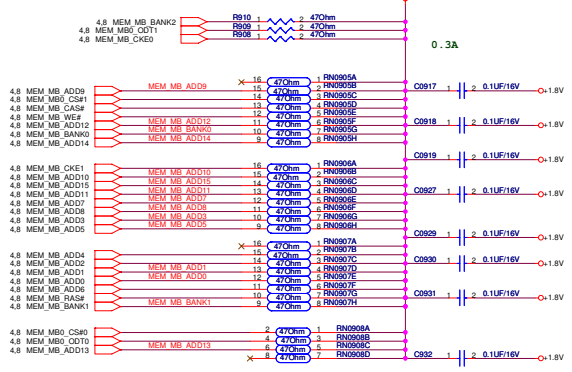
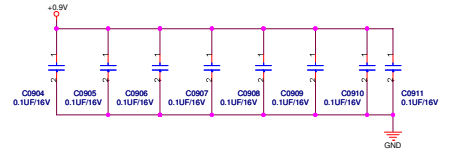
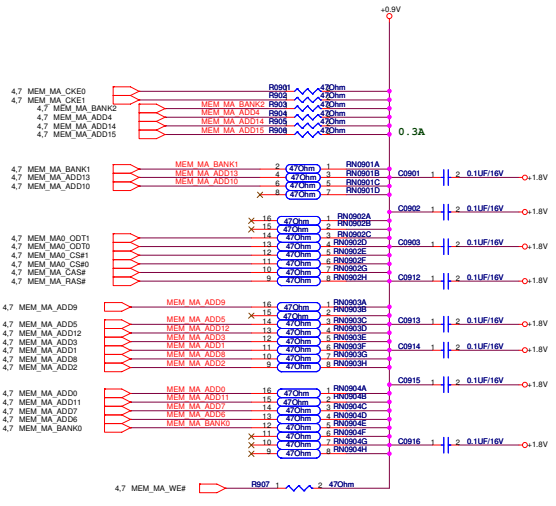
Date: Wednesday, March 12 2008 Sheet: 7 of 92

<< MaryL_Liu >>



ASUS		Title : DDR2 SO-DIMM1	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Date	Rev
Custom	ABZ/XB02/F8T	Date: Wednesday, March 12, 2008	Sheet 8 of 92

« MaryL_Liu »



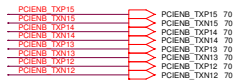
<< MaryL_Liu >>

HYPER TRANSPORT CPU I/F



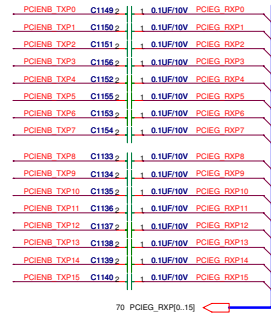
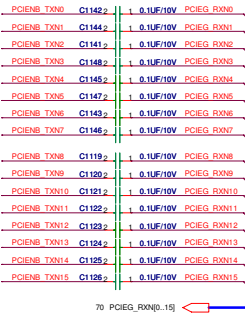
		Title: RS780M-HT LINK I/F	
		ASUSTek Computer INC	
Size	Project Name	Engineer:	Rev
Custom	ABZ / X80Z / F8T	<OrgAddr>	0.1
Date:	Wednesday, March 15, 2006	Sheet	10 of 25

<< MaryL_Liu >>

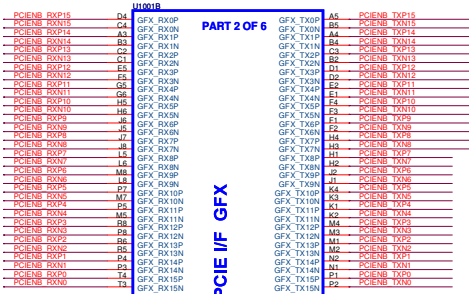
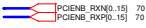


PCI-E:
0-3 HDMI@ RS780M
4-7 NC
8-15 VGABx

Refer to RS780M datasheet Table 3-10



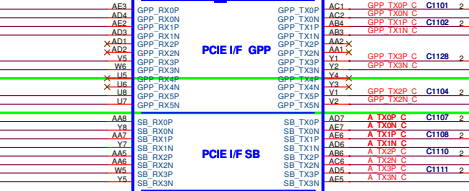
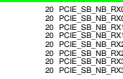
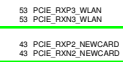
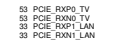
Caps on VGA card



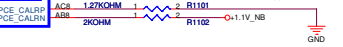
PCI-E I/F GFX

PCI-E I/F GPP

PCI-E I/F SB

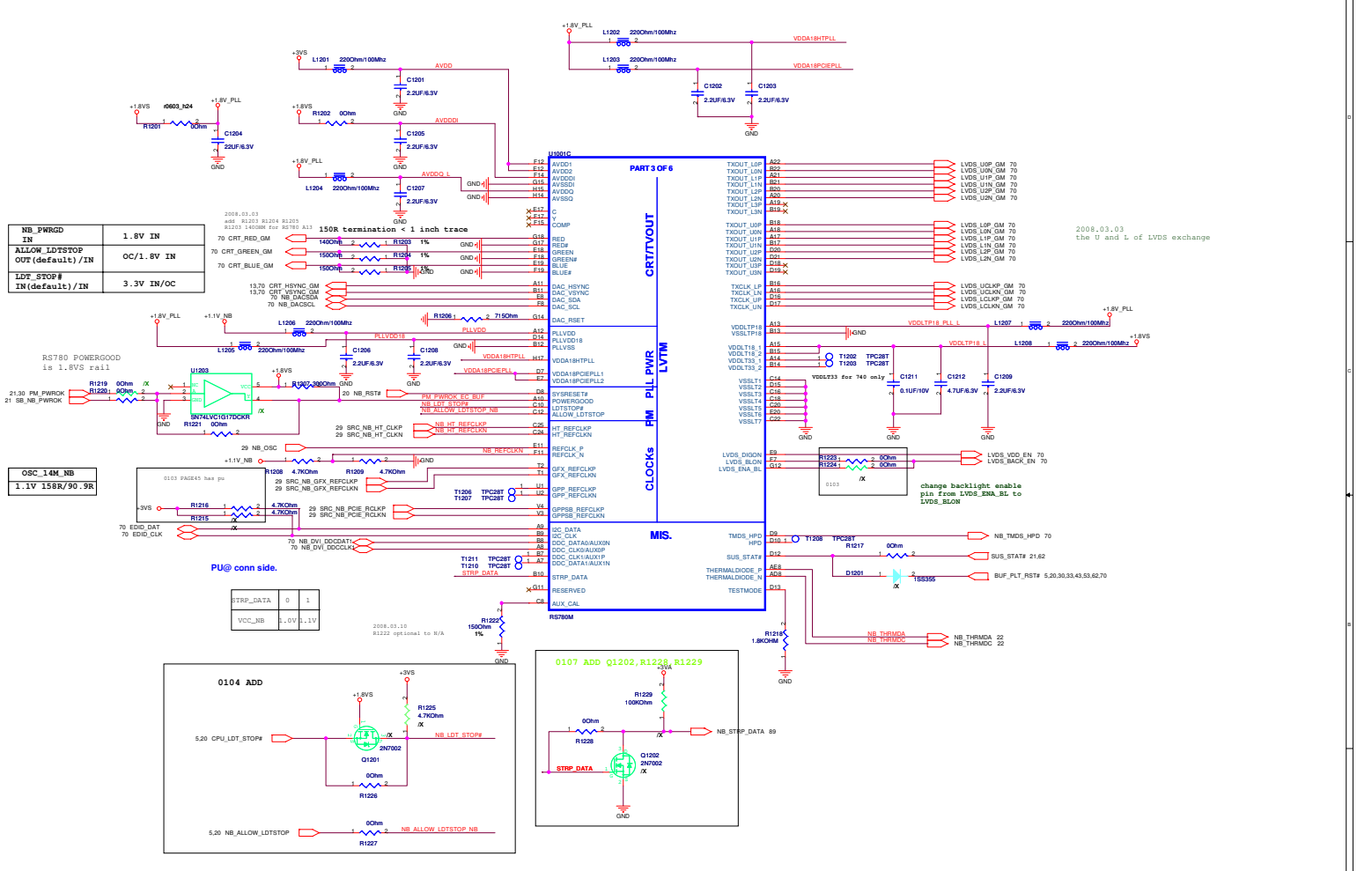


RS780M



ASUS		Title: RS780M-PCI-E LINK I/F	
ASUSTek Computer INC		Engineer: <OrgAddrt>	
Size	Project Name	Rev	
Custom	ABZ/X80Z/F8Tt	0.1	
Date: Wednesday, March 19, 2008	Sheet	11	of 28

<< MaryL_Liu >>

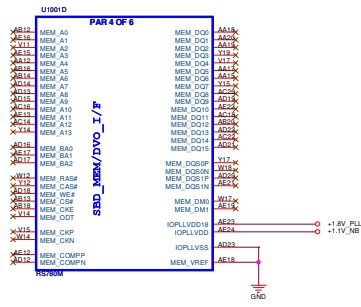


2008.03.03
the U and L of LVDS exchange

?? for external graphic

<< MaryL_Liu >>

ASUS		Title : RS780M-SYS IF	
ASUSTek Computer INC		Engineer: <OrgAdapt>	
Ver	Project Name	Rev	
C	AS2/X80Z/P8T	0.1	
Date: Wednesday, March 12, 2008		Sheet: 15 of 25	



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EEPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Value
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
 RS780:SUS_STAT

STRAP_DEBUG_BUS_PCIE_ENABLE

Enables the Test Debug Bus using PCIE bus:

1 : Disable (Can still be enabled using nbcfg register access)
 0 : Enable

RS780: configurable thru register setting only

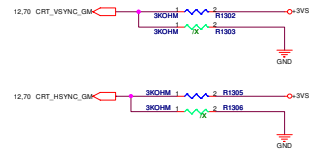
RS740 RS780: Enables Side port memory

RS780:HSYNCF

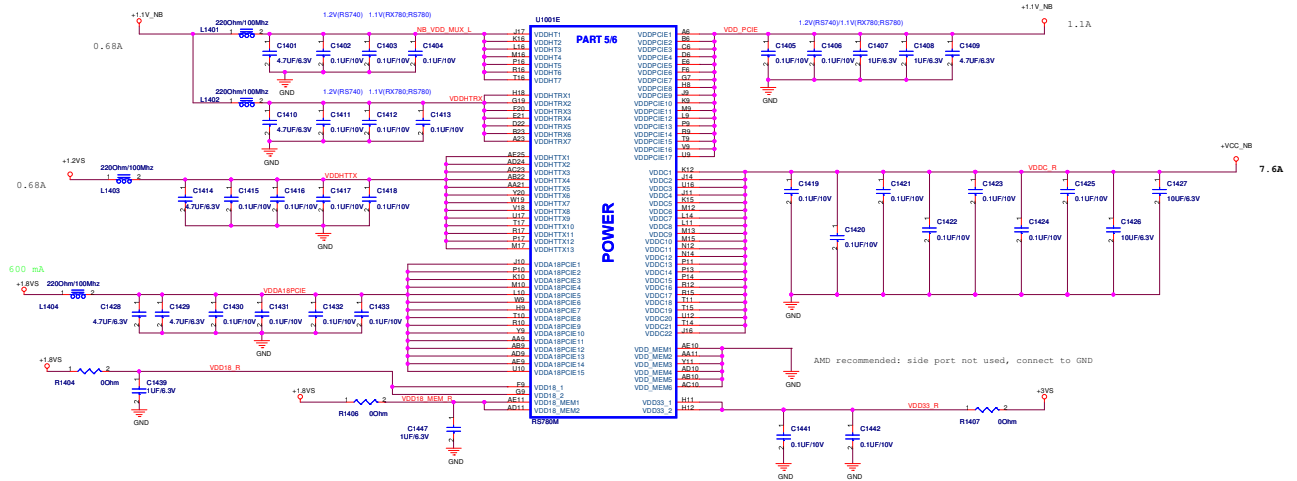
Selects if Memory SIDE PORT is available or not

1 = Memory Side port Not available
 0 = Memory Side port available

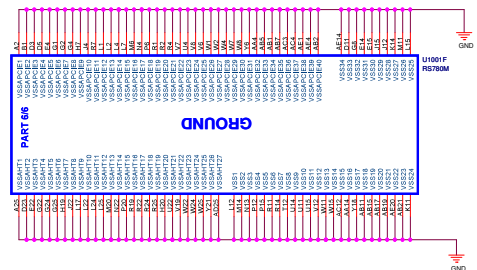
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]




<< MaryL_Liu >>




3.3V rails ramp high relative to 1.8V
Display and PLL rails. max 2.1V



<< MaryL_Liu >>

		Title :
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>
Size	Project Name	Rev
A	ABZ/X80Z/F8Tr	0.1
Date: Wednesday, March 12, 2008		Sheet 15 of 92

<< MaryL_Liu >>

		Title : BLANK
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	Rev
A	ASZ/X80Z/F8Tr	0.1
Date: Wednesday, March 12, 2008		Sheet 16 of 92

<< MaryL_Liu >>

D

D

C


C

B


B

A


A

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name ASZ/X80Z/F8Tr	Rev 0.1	
Date: Wednesday, March 12, 2008		Sheet 17 of 92	

<< MaryL_Liu >>

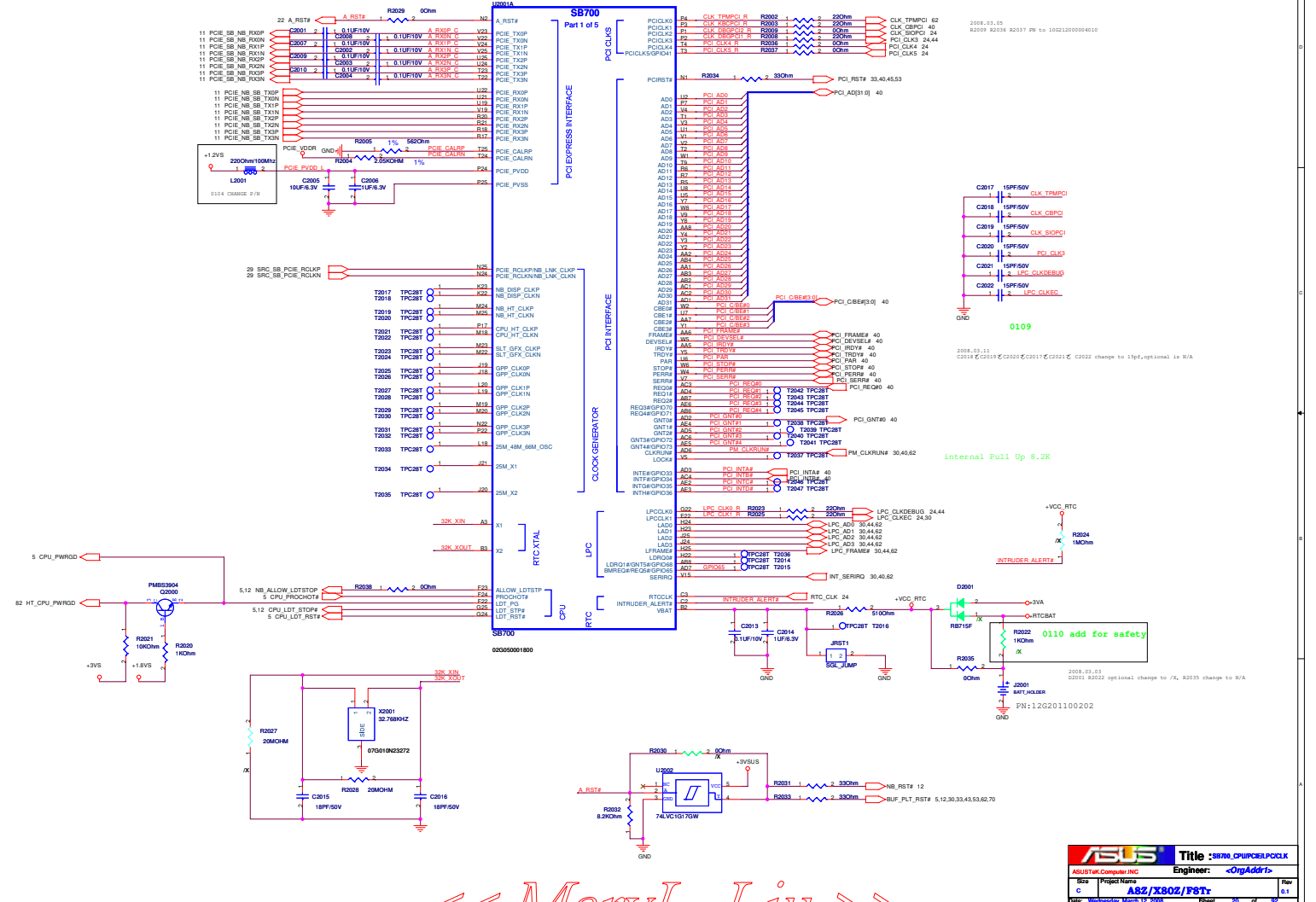
		Title : BLANK
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	Rev
A	A8Z/X80Z/F8Tr	0.1
Date: Wednesday, March 12, 2008		Sheet 18 of 92

<< MaryL_Liu >>

		Title : BLANK
ASUSTeK COMPUTER INC		Engineer:
Size A	Project Name ASZ/X80Z/F8Tr	Rev 0.1
Date: Wednesday, March 12, 2008		Sheet 19 of 92

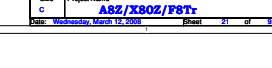
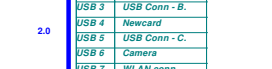
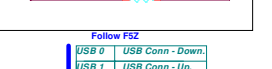
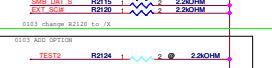
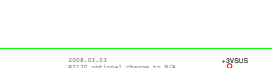
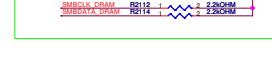
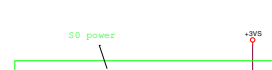
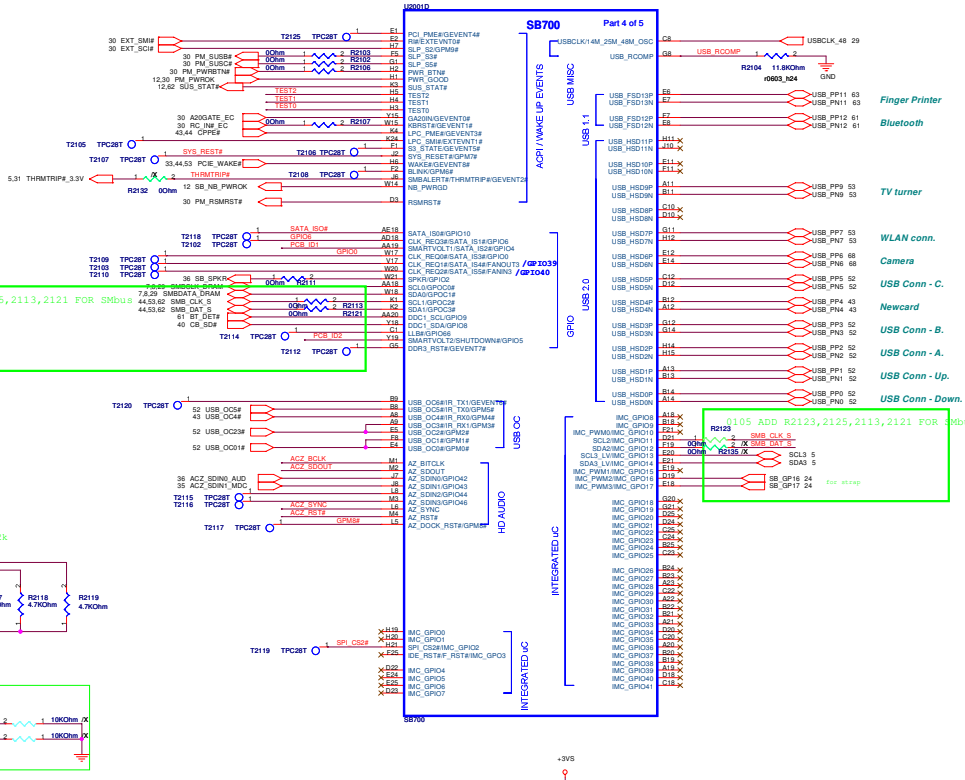
<< MaryL_Liu >>

0108 change R2008 TO 22 ohm



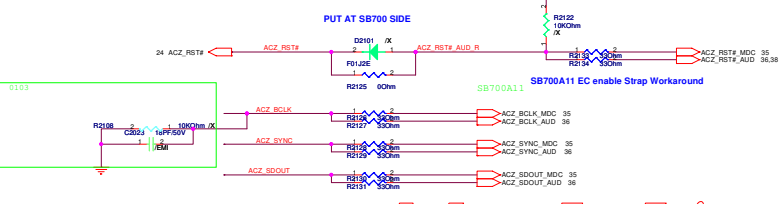
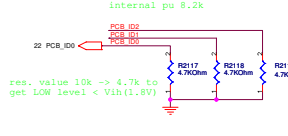
<< MaryL_Liu >>

ASUS		Title : SB700_CPU_PCIE_POOL	
ASUSTek Computer INC		Engineer: <OrgAdm>	
Size	Project Name	Rev	
C	AS2/ X302/ P8Tr	0.1	
Date: Wednesday, March 12, 2008 10:08 AM			



0105 ADD R2123,2125,2113,2121 FOR SMDs

0105 ADD R2123,2125,2113,2121 FOR SMDs



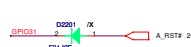
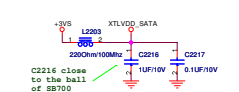
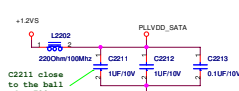
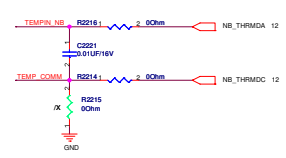
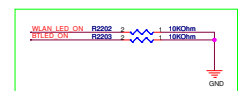
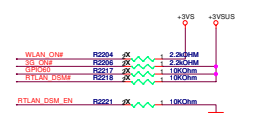
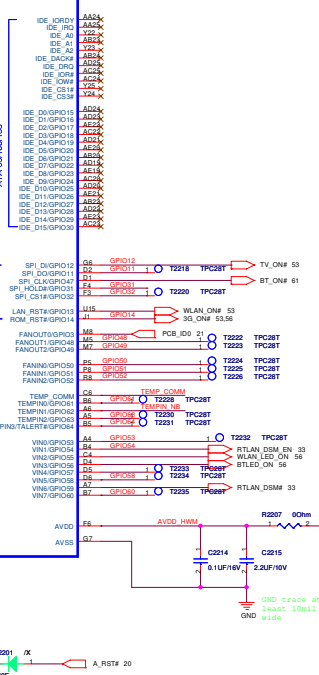
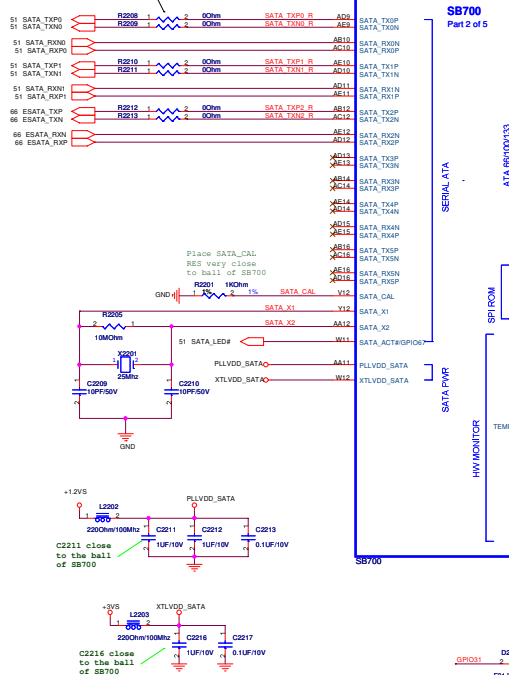
Follow FS2	
USB 0	USB Conn. - Down.
USB 1	USB Conn. - Up.
USB 2	USB Conn. - A.
USB 3	USB Conn. - B.
USB 4	Newcard
USB 5	USB Conn. - C.
USB 6	Camera
USB 7	WLAN conn.
USB 8	NC
USB 9	TV tuner
USB 10	NC
USB 11	Finger Printer
USB 12	Bluetooth
USB 13	NC

<< MaryL_Liu >>

ASUS ASUSTek Computer Inc. Title: SB700_GPIOUSBHMACR
 Sca Project Name: A82/X80Z/P81r Rev: 0.1
 C Author: <OrgAddt> Date: Wednesday, March 12, 2008 Sheet: 21 of 25

for sata II close sb in 0.5"

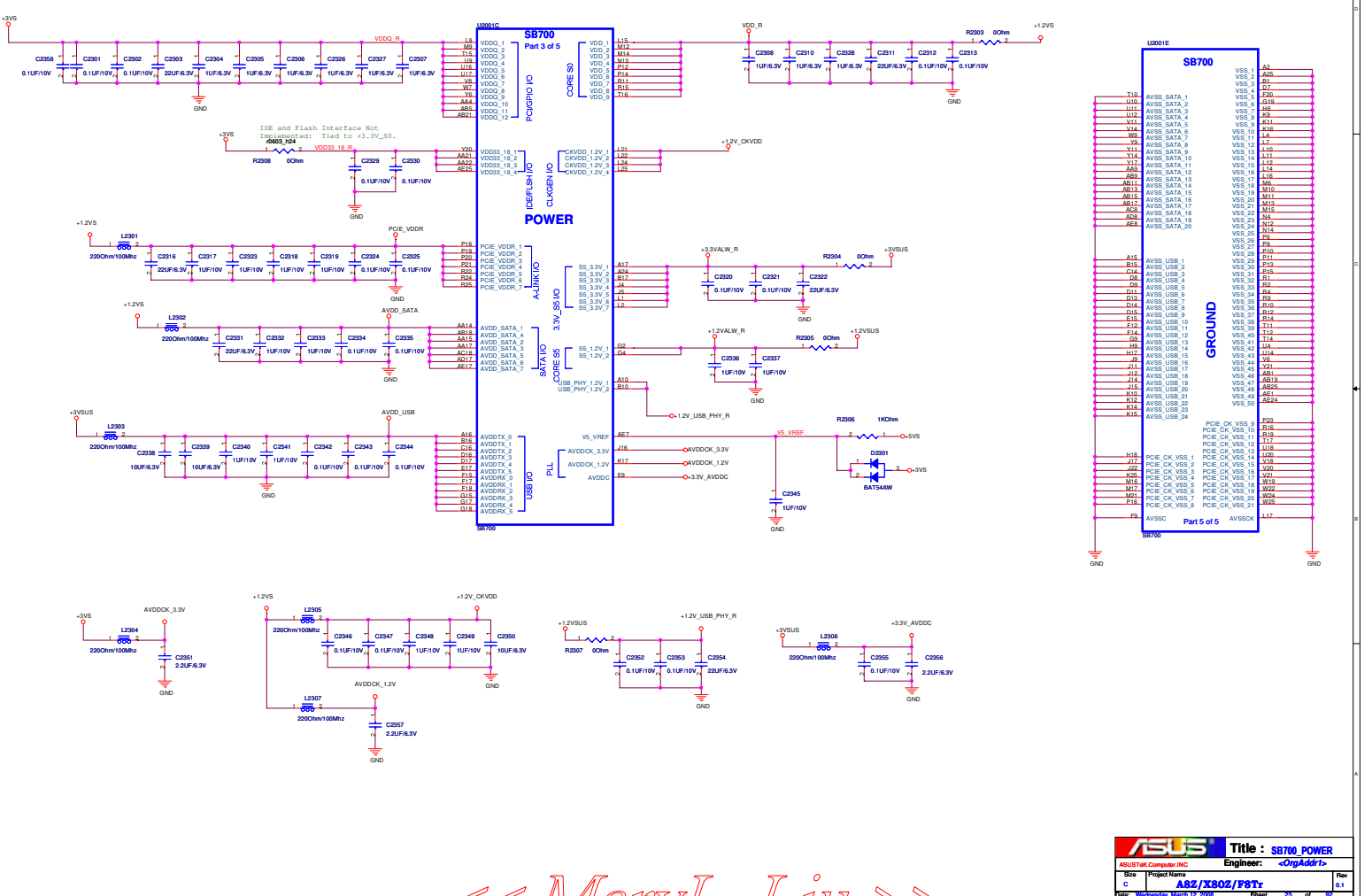
for SATA HDD
for SATA ODD
for E-SATA



2008_03_05
add R2201 optional to FX

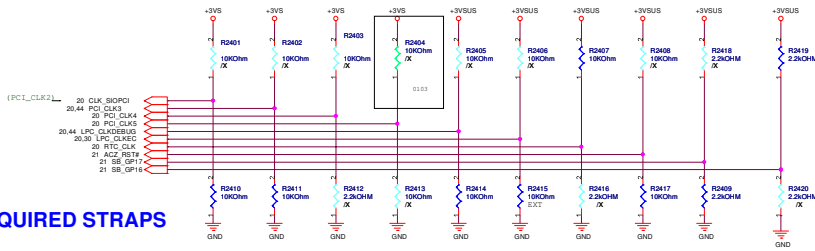
ASUS		Title : SB700_PATA/SATA	
ASUSTek Computer INC.		Engineer: <OrgAdit>	
Size	Project Name	Rev	
C	A82/X302/P8T	0.1	
Date:	Wednesday, March 12, 2008	Sheet:	25 of 25

<< MaryL_Liu >>



« MaryL_Liu »

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK




REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLKDEB	LPC_CLKEC	RTC_CLK	ACZ_RST#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC	EC ENABLED	H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PC) on XT, apply 32KHz to RTC_CLK	EC DISABLED DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM	

WITH A12 SB700, STRAP PIN FOR MEM BOOT AND EC ENABLE SWAPED.
I.E. LPC_CLK0 FOR EC ENABLE, AZ_RST# FOR MEM BOOT ENABLE.

ASUS		Title : SB700_STRAP	
ASUSTeK Computer INC.		Engineer: <OrgAdd>	
Size	Project Name	Rev	
C	A82/X802/P8Tr	0.1	
Date: Wednesday, March 17, 2009	Sheet: 24	of	25

<< MaryL_Liu >>

		Title :
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>
Size	Project Name	Rev
A	ABZ/X80Z/F8Tr	0.1
Date: Wednesday, March 12, 2008		Sheet 25 of 92

<< MaryL_Liu >>

		Title : BLANK
ASUSTeK COMPUTER INC		Engineer:
Size A	Project Name A8Z/X80Z/F8Tr	Rev 0.1
Date: Wednesday, March 12, 2008		Sheet 26 of 92


<< MaryL_Liu >>

D

D

C

C

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
A	A8Z/X80Z/F8Tr	0.1	
Date: Wednesday, March 12, 2008		Sheet 27 of 92	

B

B

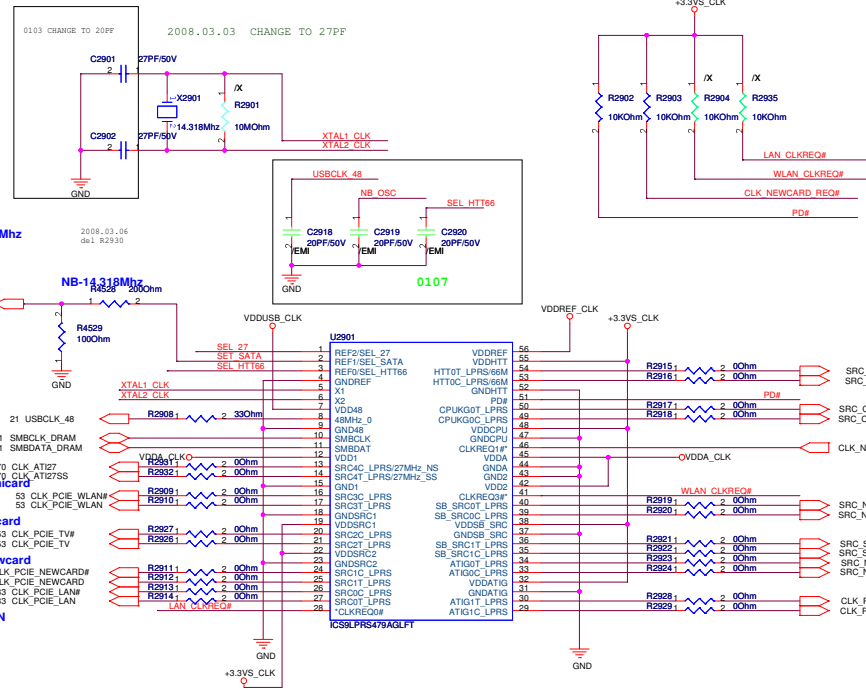
A

A

<< MaryL_Liu >>

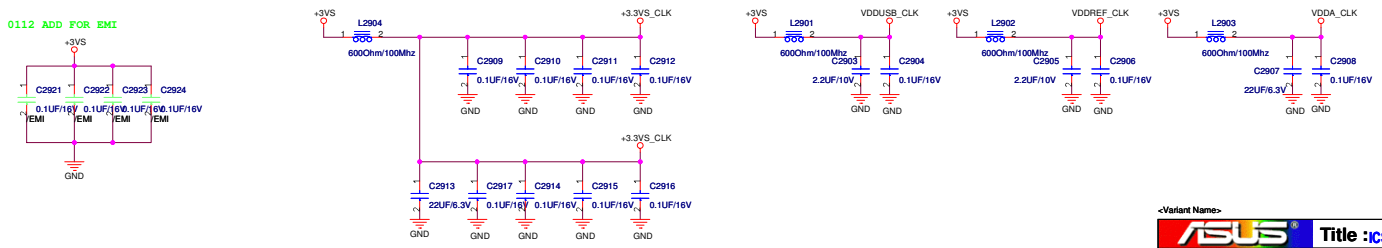
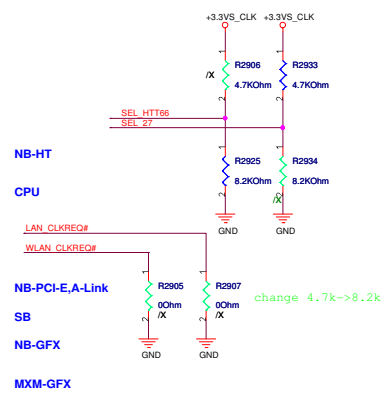
		Title : BLANK
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	Rev
A	A8Z/X80Z/F8Tr	0.1
Date: Wednesday, March 12, 2008		Sheet 28 of 92

<< MaryL_Liu >>



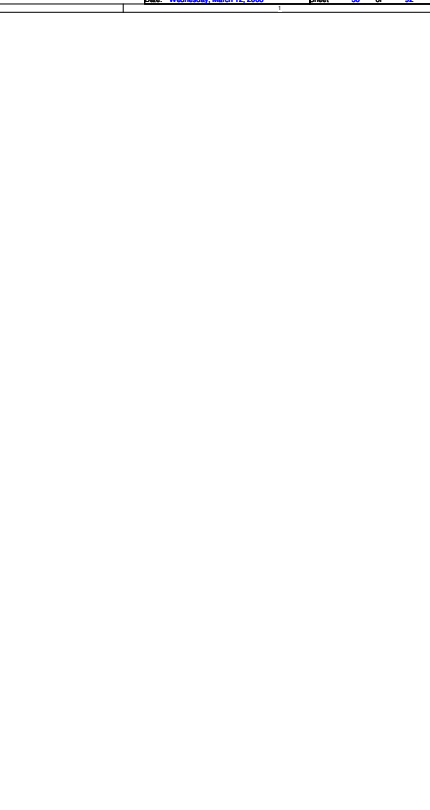
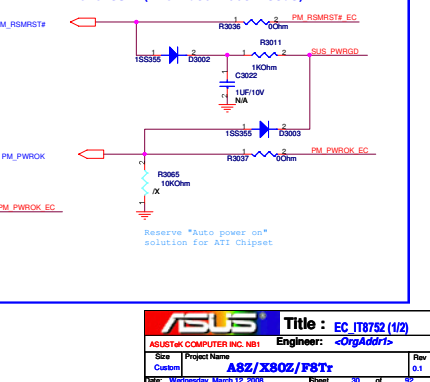
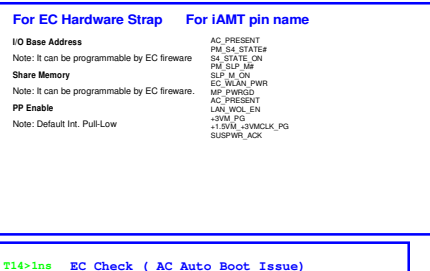
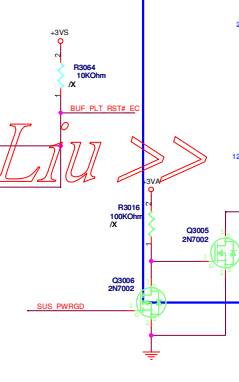
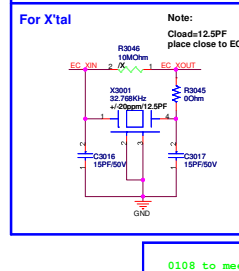
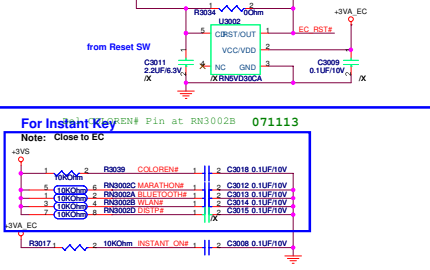
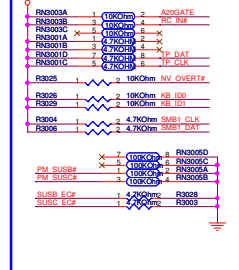
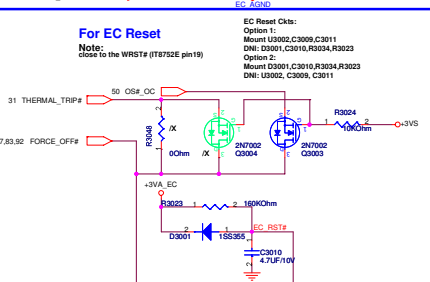
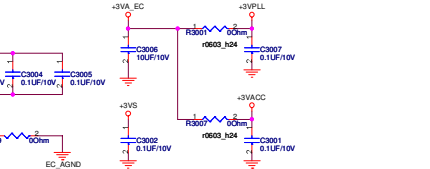
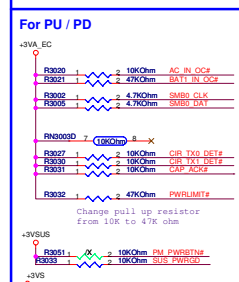
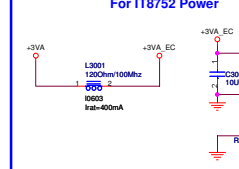
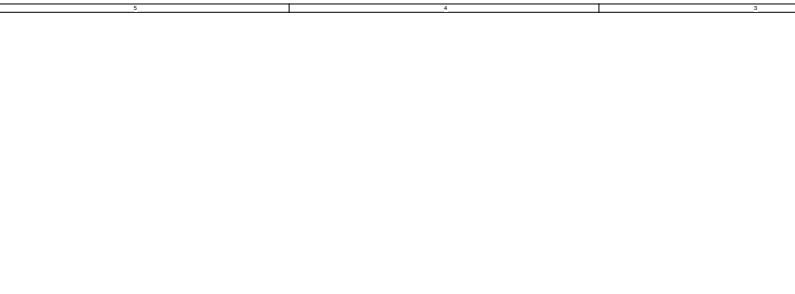
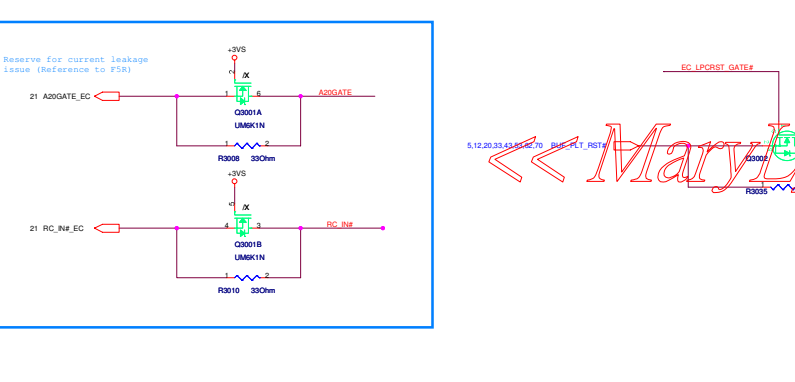
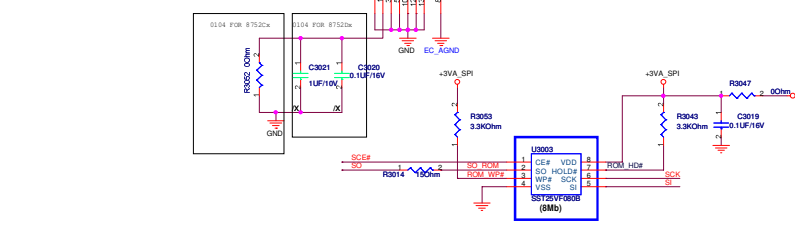
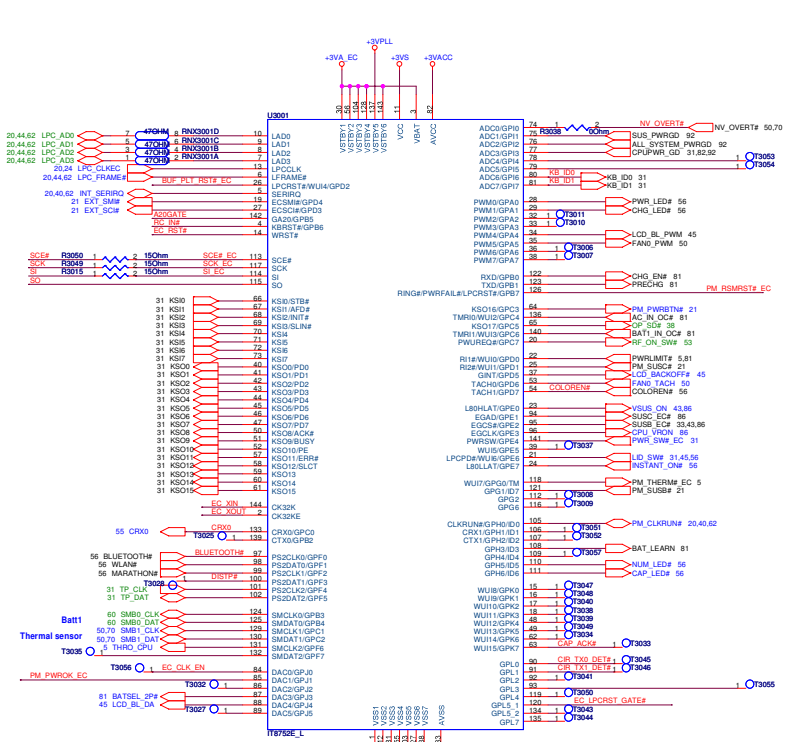
SEL_27	0	100 MHz differential Spread SRC clock
	1	27MHz 3.3V 27MHz spread clock
SEL_HTT66	0	100 MHz differential HTT clock
	1	66MHz 3.3V single ended HTT clock

- SIO-14.318Mhz
- NB-14.318Mhz
- PCIE P0: Minicard
- PCIE P3: Minicard
- PCIE P2: Newcard
- PCIE P1: LAN

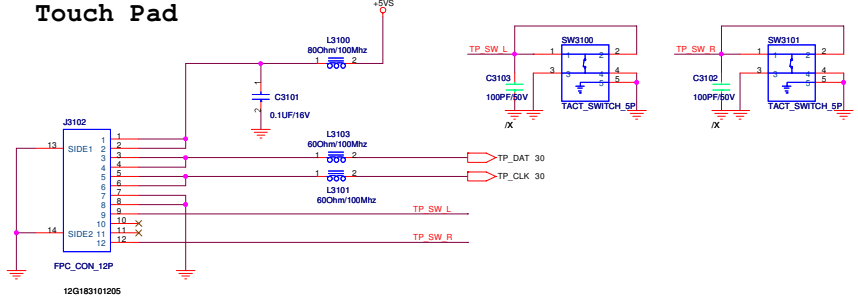


ASUS		Title : ICS9LPRS479AGLFT	
ASUSTeK COMPUTER INC		Engineer: Richard Lu	
Size	Project Name	Rev	
Custom	A8Z/X80Z/F8Tr	0.1	
Date: Wednesday, March 12, 2008	Sheet	29	of 92

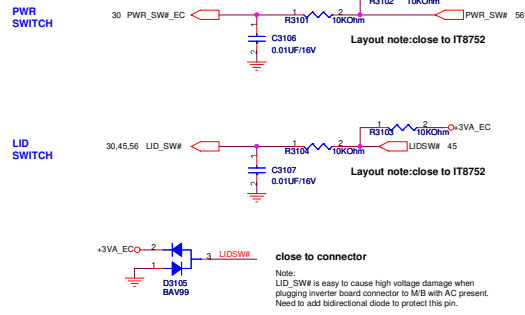
« Maryl Liu »



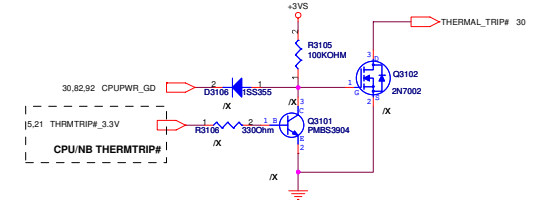
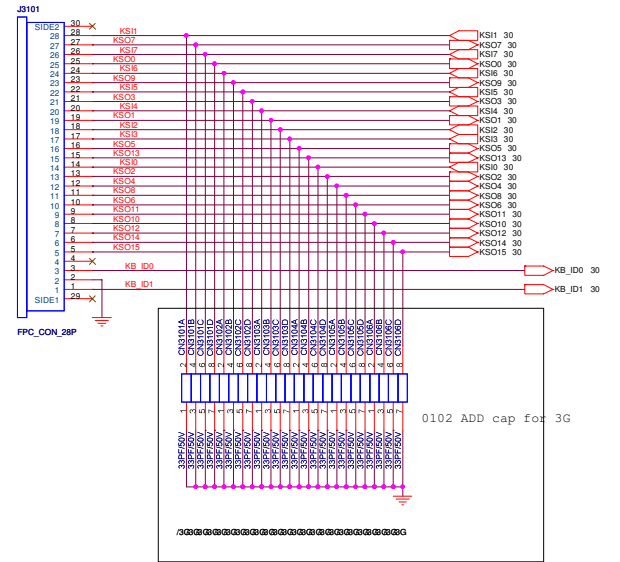
Touch Pad



For Switch




KBDDT1	KBDDT0	Matrix
1	1	US
1	0	UK
0	1	JP

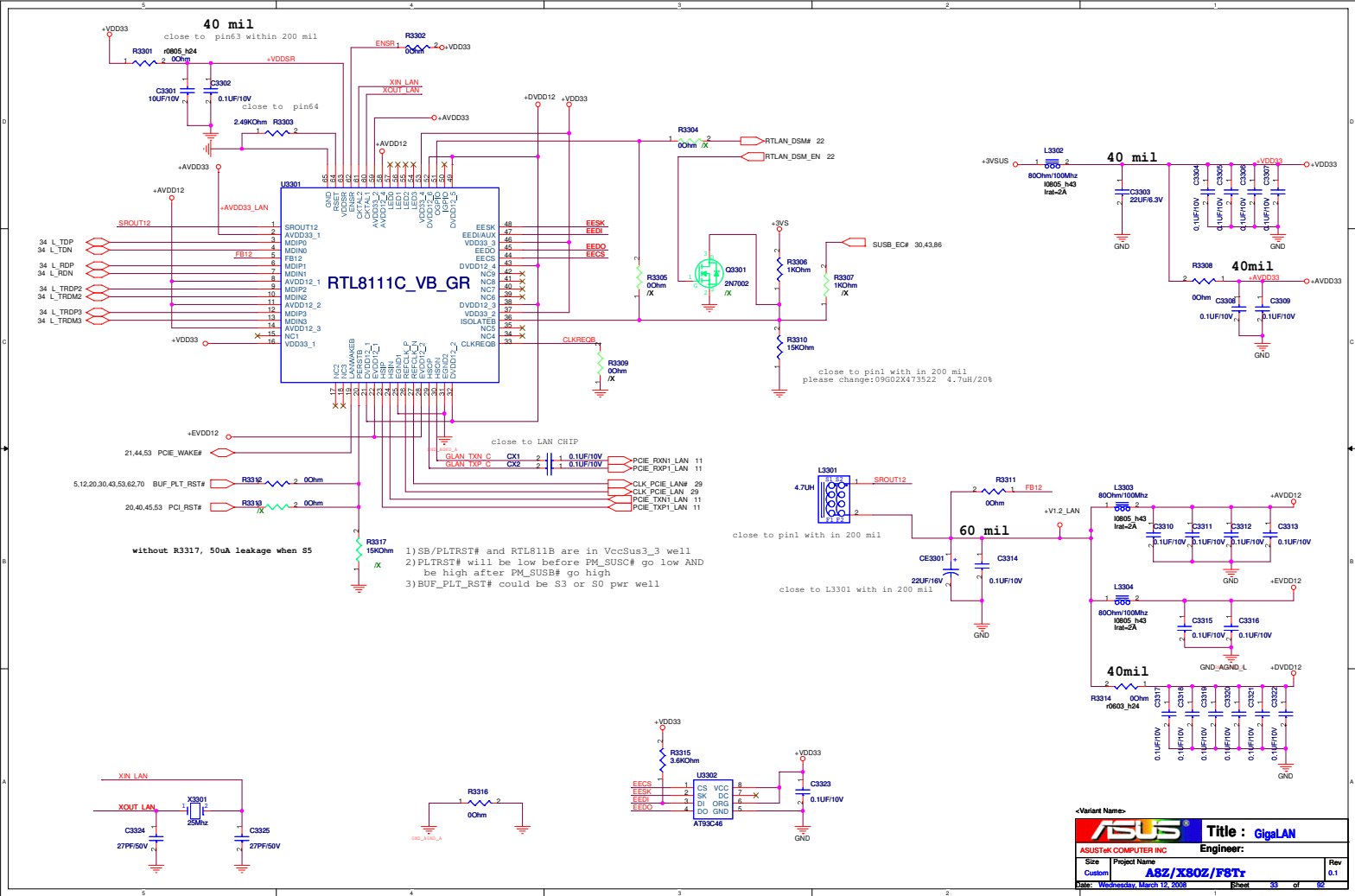


ASUS Title : EC_IT8511 (2/2)
 ASUSTeK COMPUTER INC. (NBI) Engineer: <OrgAddr>
 Size Project Name
 Custom ARZ/X80Z/F8T Rev
 Date: Wednesday, March 12, 2008 Sheet 31 of 92

<< MaryL_Liu >>

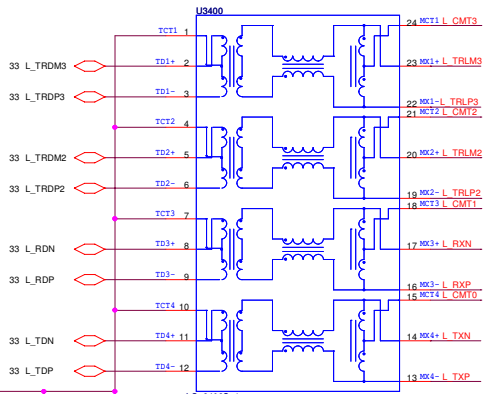
		Title : BLANK
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	Rev
A	ASZ/X80Z/F8Tr	0.1
Date: <u>Wednesday, March 12, 2008</u>		Sheet <u>32</u> of <u>92</u>

<< MaryL_Liu >>

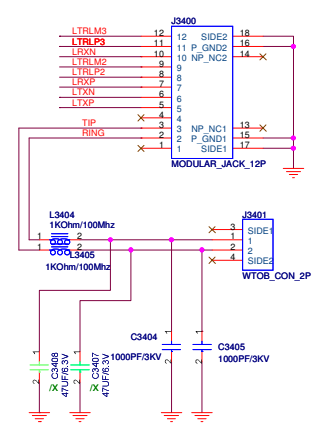
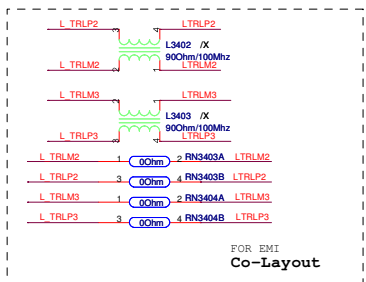
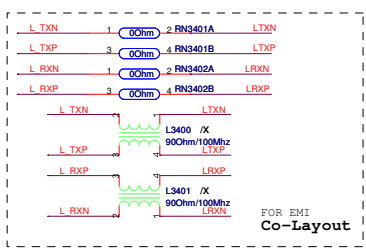
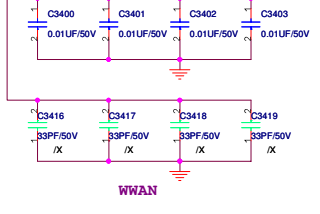
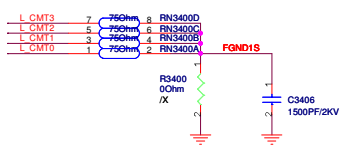


<< MaryL_Liu >>

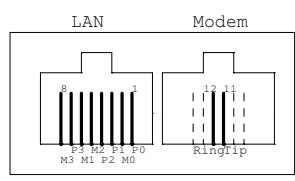
2402S have issue after IR reflow,
 alternative part:LG-2410S-1



Transformer close CON4



2008.03.12
 add C3407 C3408 optional is /X



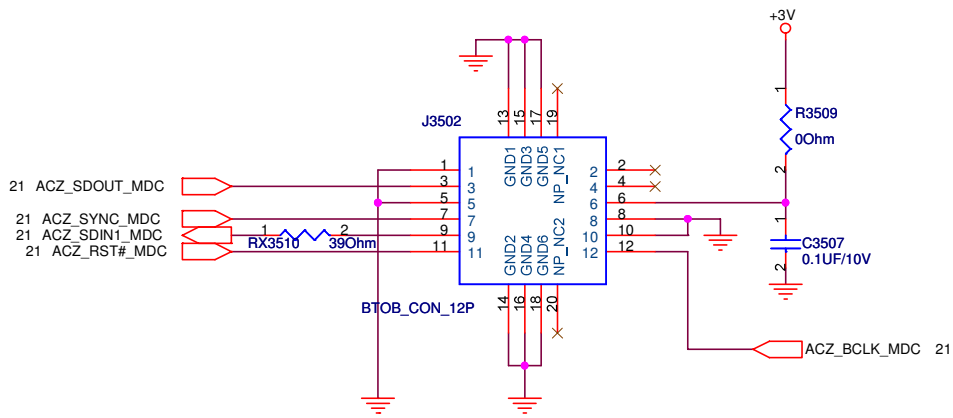
<Variant Name>

ASUS		Title : RJ11+45
ASUSTeK COMPUTER INC		Engineer:
Site:	Project Name:	
Custom	A8Z/X80Z/F8T	
Date: Wednesday, March 12, 2008	Sheet	34 of 92

Rev 0.1

<< MaryL_Liu >>

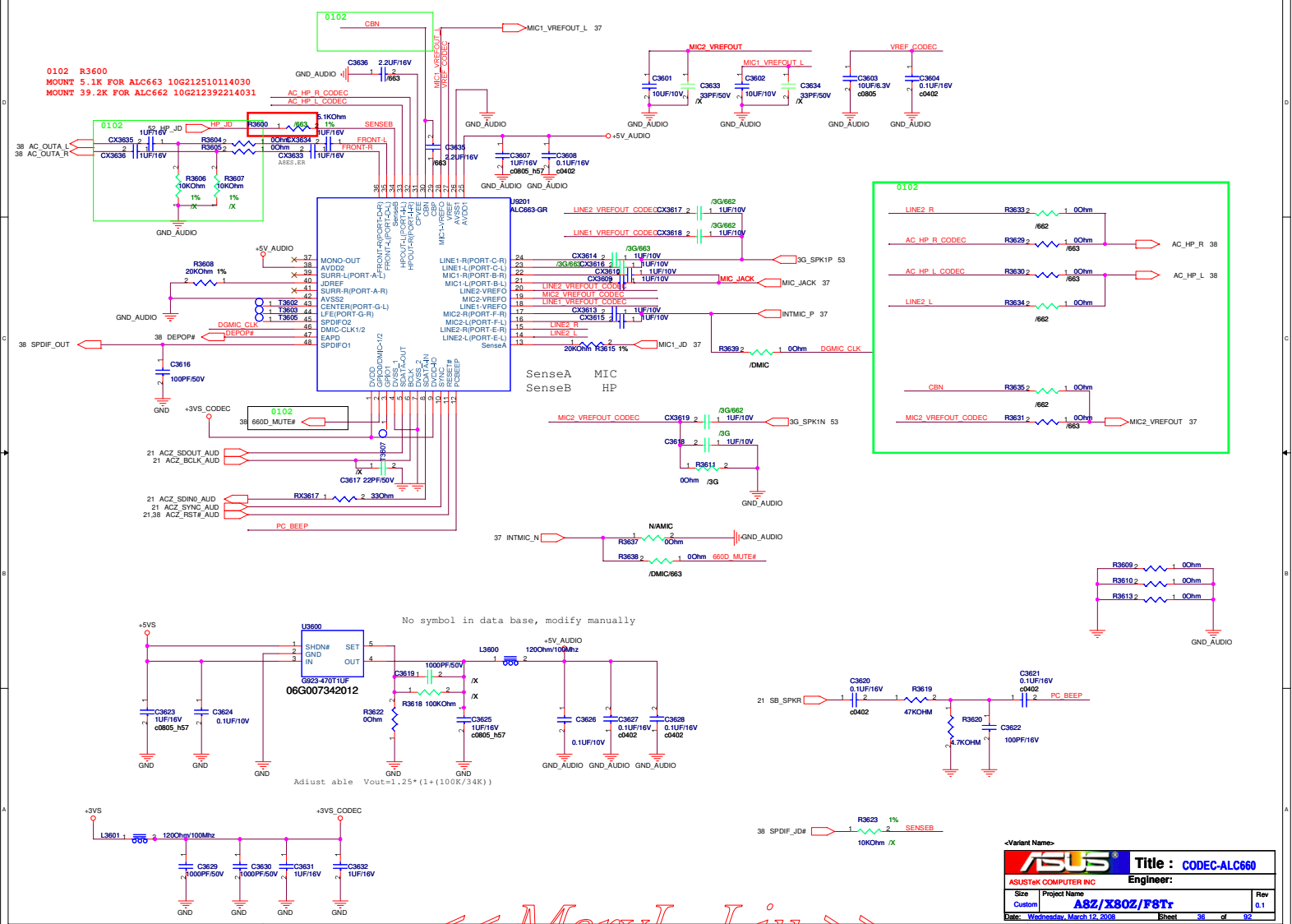
AZALIA MDC Connector



ASUS		Title : MDC
ASUSTeK COMPUTER INC		Engineer:
Size A	Project Name A8Z/X80Z/F8Tr	Rev 0.1
Date: Wednesday, March 12, 2008	Sheet 35	of 92

« MaryL_Liu »

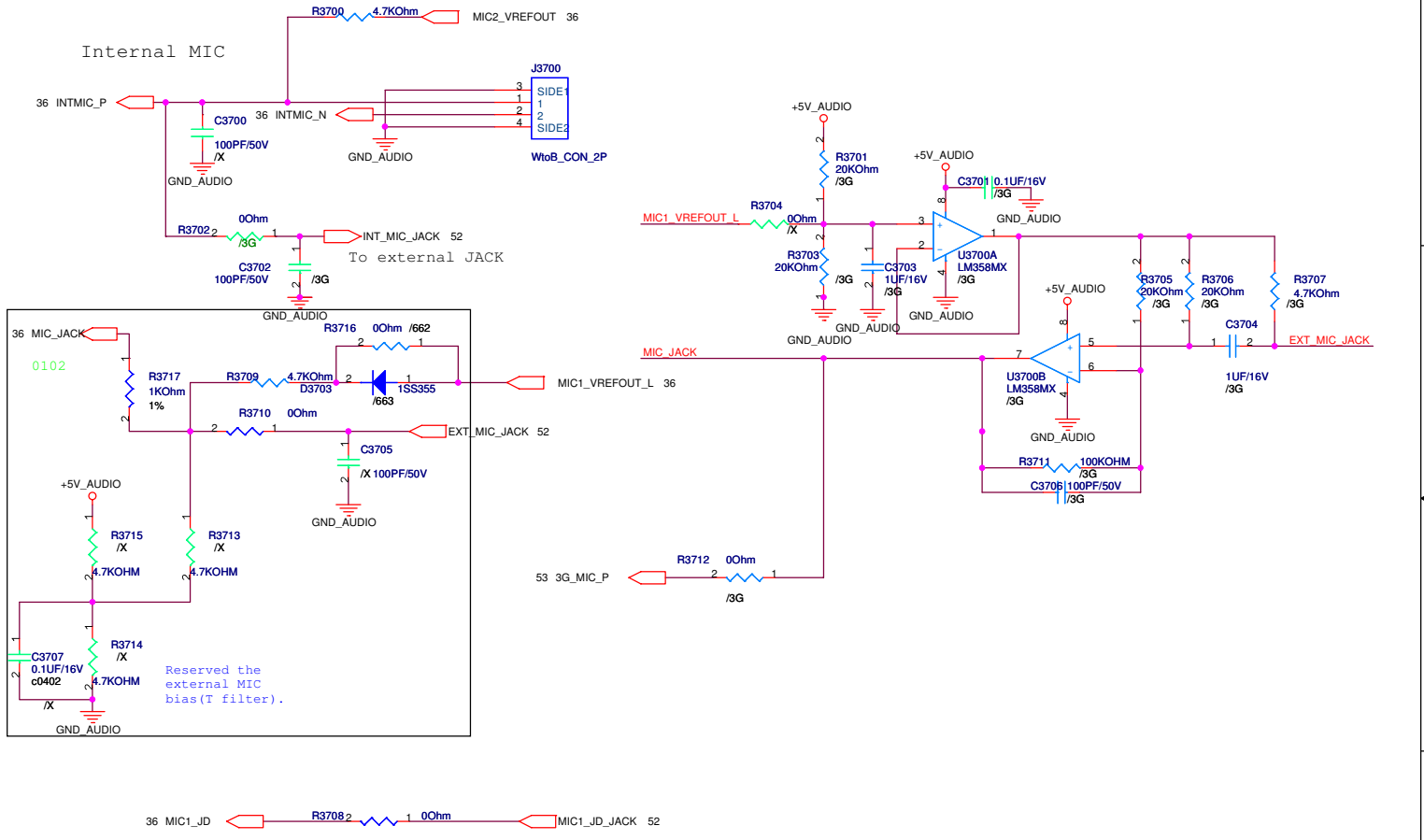
0102 R3600
 MOUNT 5.1K FOR ALC663 10G212510114030
 MOUNT 39.2K FOR ALC662 10G212392214031



<Variant Name>

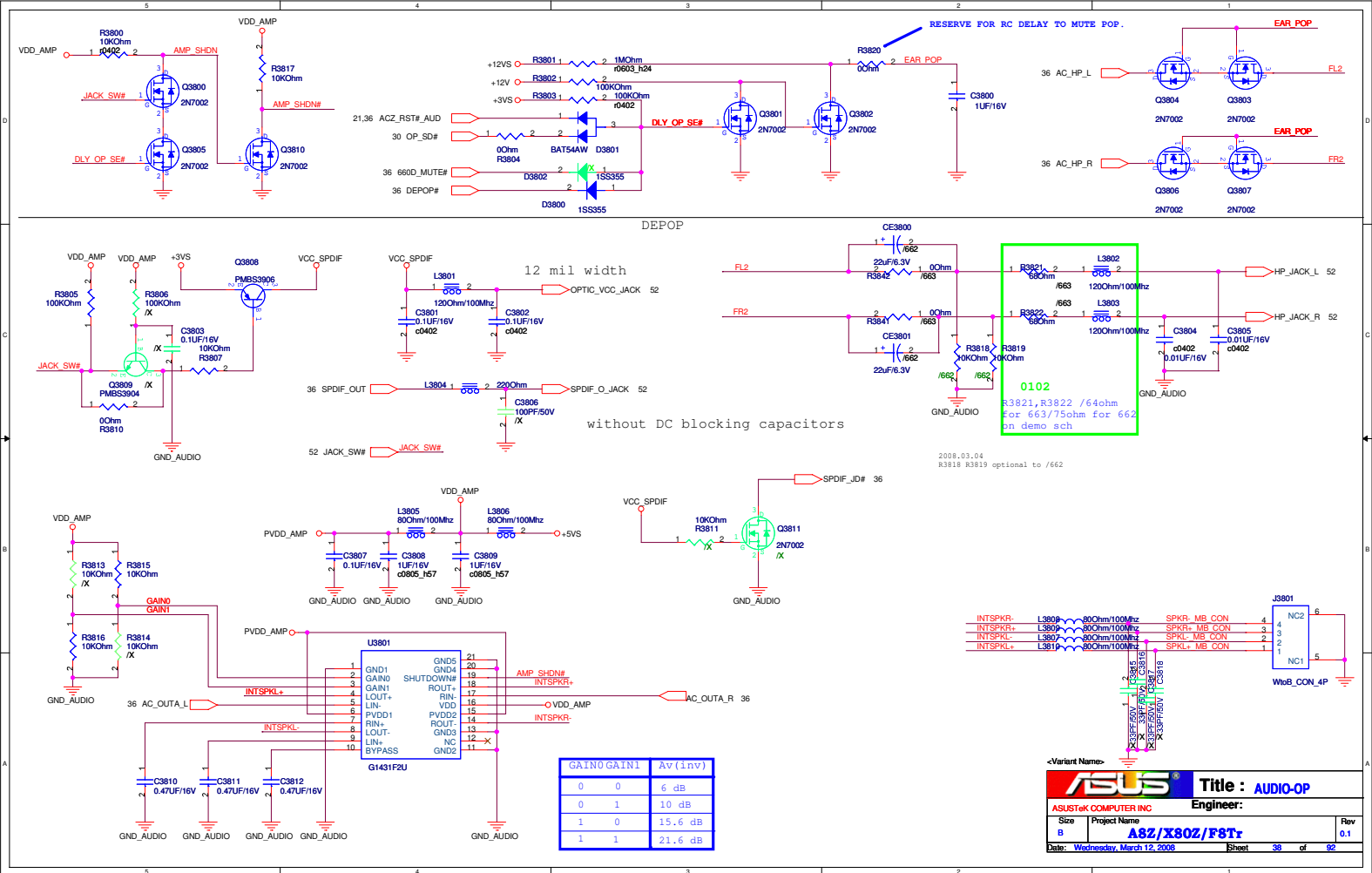
ASUS		Title : CODEC-ALC660	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	ABZ/X80Z/F8Tr	0.1	
Date: Wednesday, March 12, 2008	Sheet	38	of 82

« MaryL_Liu »



ASUS		Title : AUDIO-MIC	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	A8Z/X80Z/F8Tr		0.1
Date: Wednesday, March 12, 2008		Sheet 37 of 92	

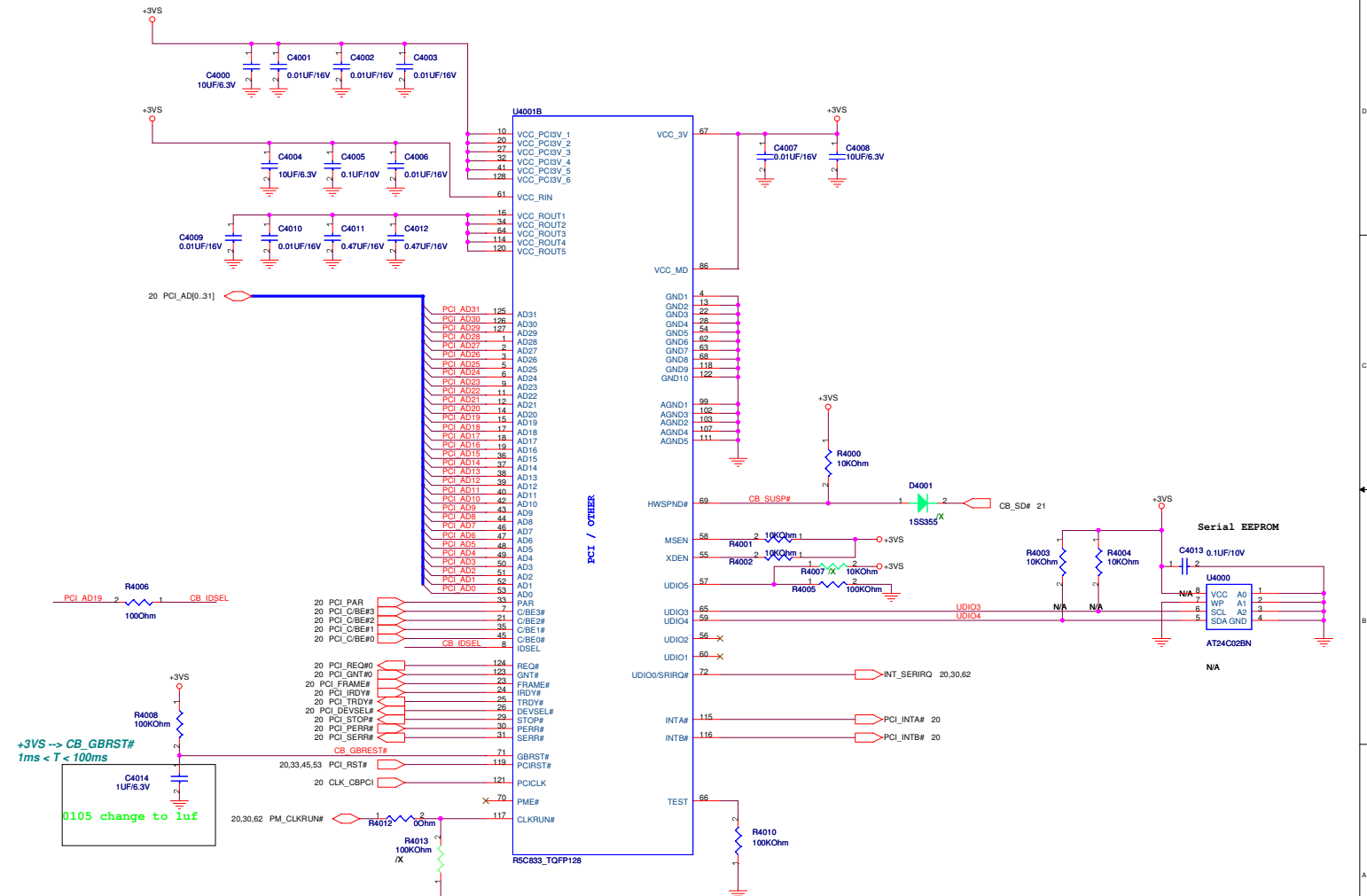
<< MaryL_Liu >>



<< MaryL_Liu >>

		Title : BLANK
ASUSTeK COMPUTER INC		Engineer:
Size A	Project Name A8Z/X80Z/F8Tr	Rev 0.1
Date: Wednesday, March 12, 2008		Sheet 39 of 92

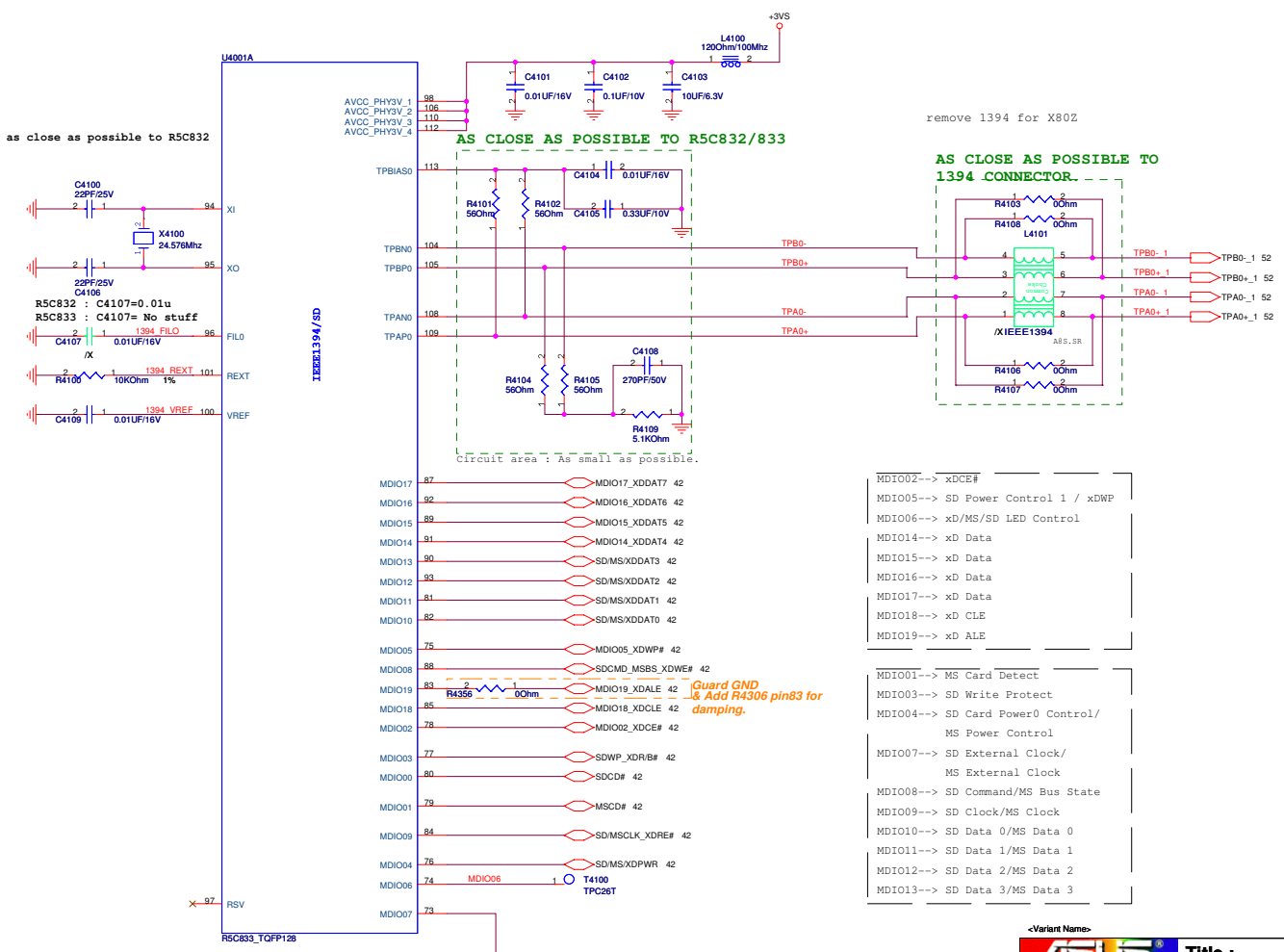
<< MaryL_Liu >>



<Variant Name>

ASUS		Title : RICOH R5C832/PCI B	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	A8Z/X80Z/F8Tr		0.1
Date: Wednesday, March 12, 2008	Sheet	40	of 92

<< MaryL_Liu >>



- MDIO17 --> MDIO17_XDDAT7 42
- MDIO16 --> MDIO16_XDDAT6 42
- MDIO15 --> MDIO15_XDDAT5 42
- MDIO14 --> MDIO14_XDDAT4 42
- MDIO13 --> SDMS_XDDAT3 42
- MDIO12 --> SDMS_XDDAT2 42
- MDIO11 --> SDMS_XDDAT1 42
- MDIO10 --> SDMS_XDDAT0 42
- MDIO05 --> MDIO05_XDWP# 42
- MDIO08 --> SDCMD_MSBS_XDWE# 42
- MDIO19 --> MDIO19_XDALE 42
- MDIO18 --> MDIO18_XDCLE 42
- MDIO02 --> MDIO02_XDCE# 42
- MDIO03 --> SDWP_XDR/B# 42
- MDIO00 --> SDCD# 42
- MDIO01 --> MSCD# 42
- MDIO09 --> SDMSCLK_XDRE# 42
- MDIO04 --> SDMS_XDPWR 42
- MDIO06 --> T4100 TPC26T
- MDIO07 --> RSV

- MDIO02--> xDCE#
- MDIO05--> SD Power Control 1 / xDWP
- MDIO06--> xD/MS/SD LED Control
- MDIO14--> xD Data
- MDIO15--> xD Data
- MDIO16--> xD Data
- MDIO17--> xD Data
- MDIO18--> xD CLE
- MDIO19--> xD ALE
- MDIO01--> MS Card Detect
- MDIO03--> SD Write Protect
- MDIO04--> SD Card Power0 Control/
MS Power Control
- MDIO07--> SD External Clock/
MS External Clock
- MDIO08--> SD Command/MS Bus State
- MDIO09--> SD Clock/MS Clock
- MDIO10--> SD Data 0/MS Data 0
- MDIO11--> SD Data 1/MS Data 1
- MDIO12--> SD Data 2/MS Data 2
- MDIO13--> SD Data 3/MS Data 3

<Variant Name>

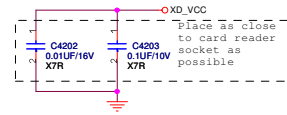
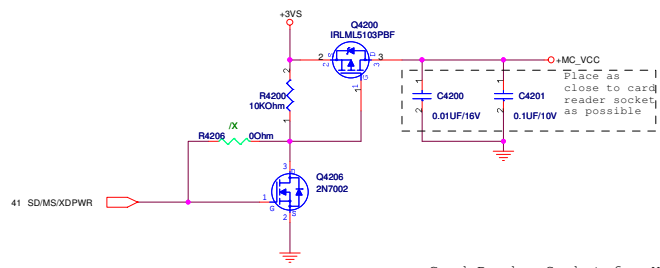
ASUS Title : RICOH R5C832/PCI A

ASUSTek COMPUTER INC Engineer:

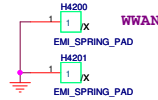
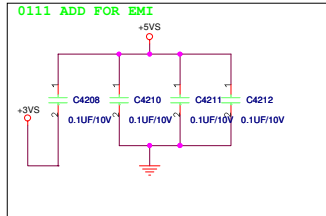
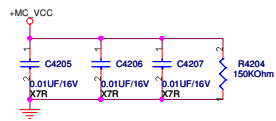
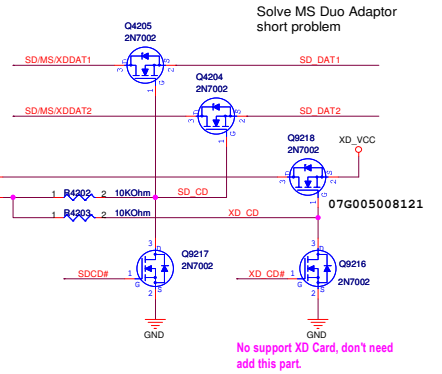
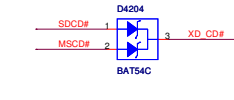
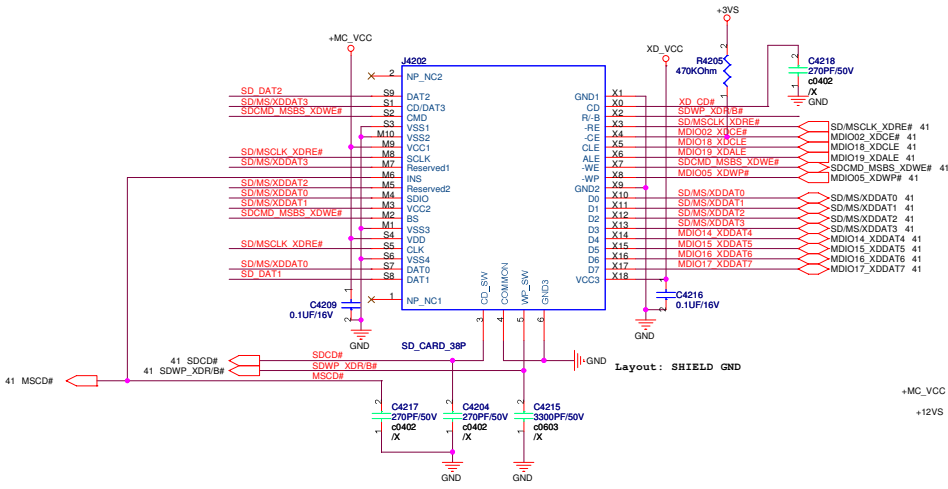
Size	Project Name	Rev
Custom	A8Z/X80Z/F8Tr	0.1
Date: Wednesday, March 12, 2008	Sheet 41 of 92	

<< MaryL_Liu >>

To correct the problem when MS Duo adaptor is in use.



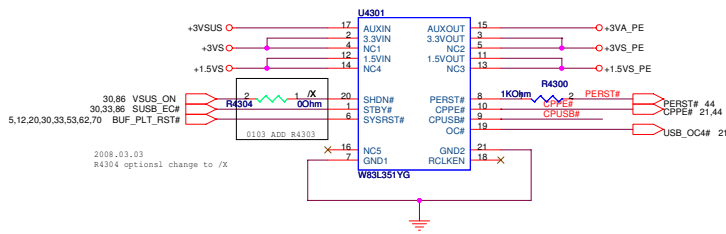
remove Card Reader Socket for X80Z



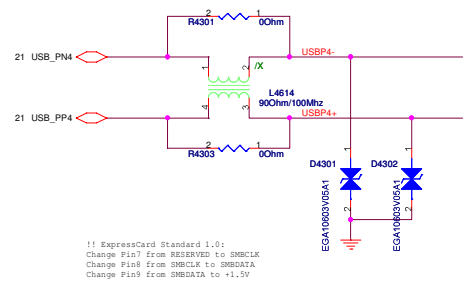
-Variant Name-		Title : CardReader	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	ASZ/X80Z/F8T	0.1	
Date: Wednesday, March 12, 2008	Sheet	42	of 92

<< MaryL_Liu >>

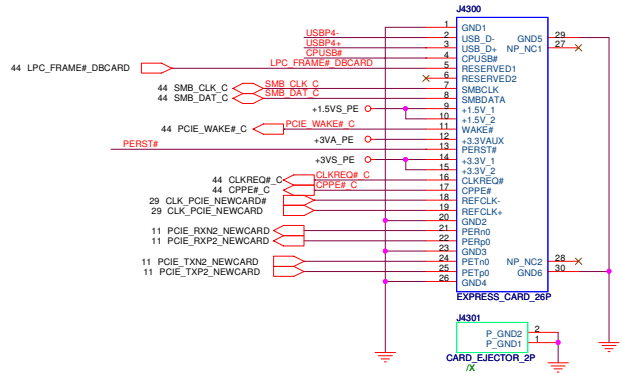
Change RICOH R5538 as 2nd source and Winbond W83L351YG (06G030091010) put on 1st source.



2008.03.03
R4304 optional change to /X



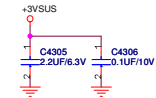
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V



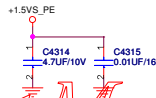
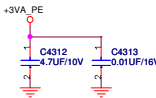
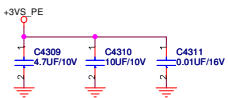
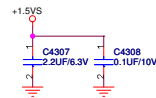
3.0V-3.6V
Ave= 1000mA
Max= 1300 mA



3.0V-3.6V
Ave= 200mA
Max= 275 mA

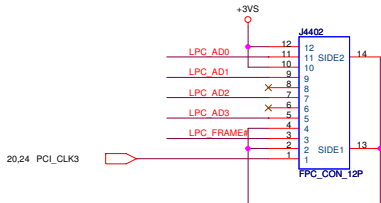
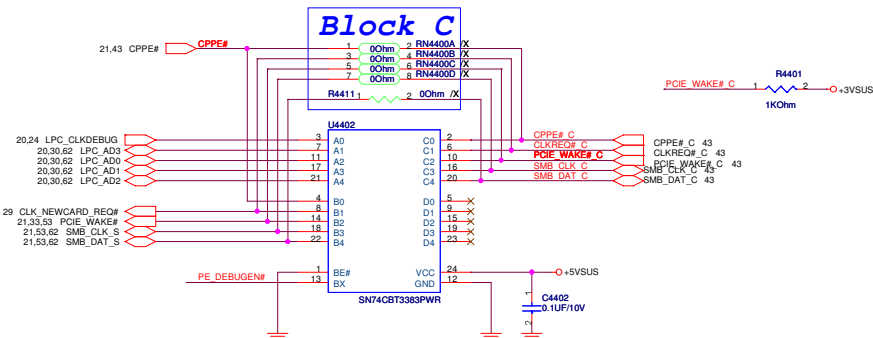
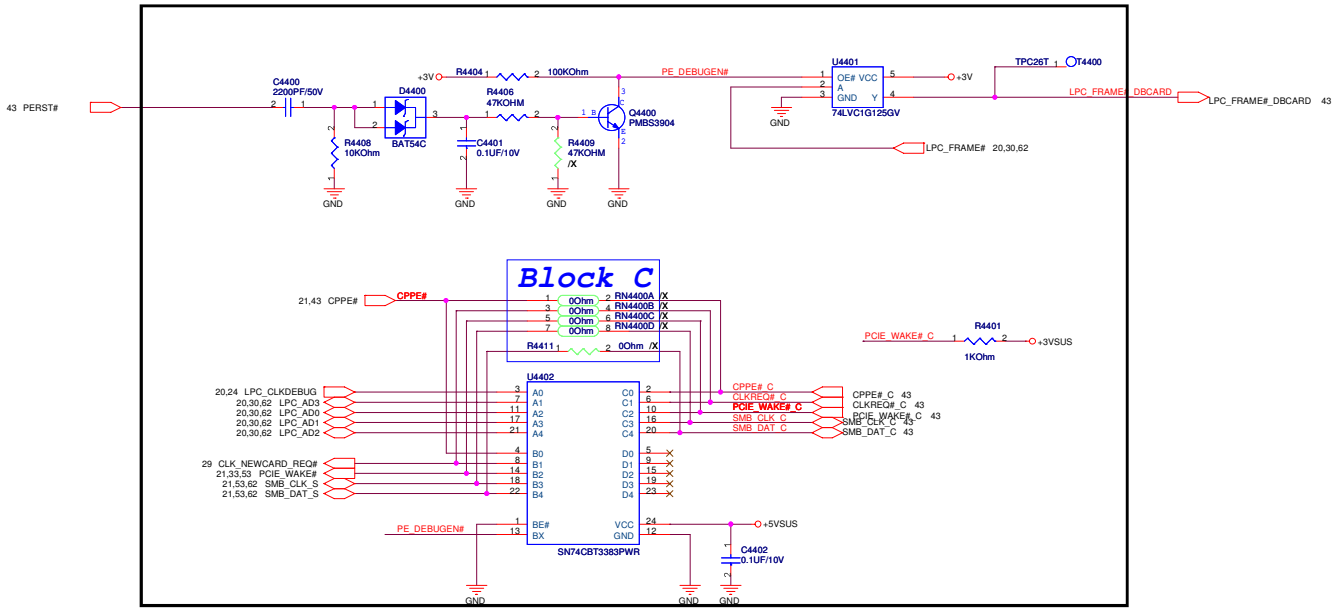


1.35V-1.65V
Ave= 500 mA
Max= 650 mA



ASUS		Title : Express Card	
ASUSTeK COMPUTER INC		Engineer:	
Site	Project Name	Rev	0.1
Custom	A82/X80Z/F8T	Date	Wednesday, March 12, 2008
Date: Wednesday, March 12, 2008		Sheet	43 of 92

<< MaryL_Liu >>

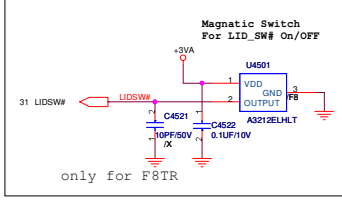
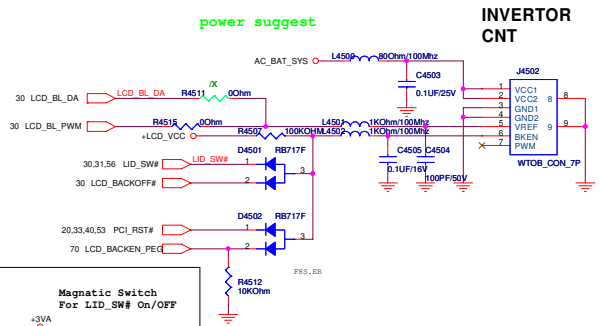
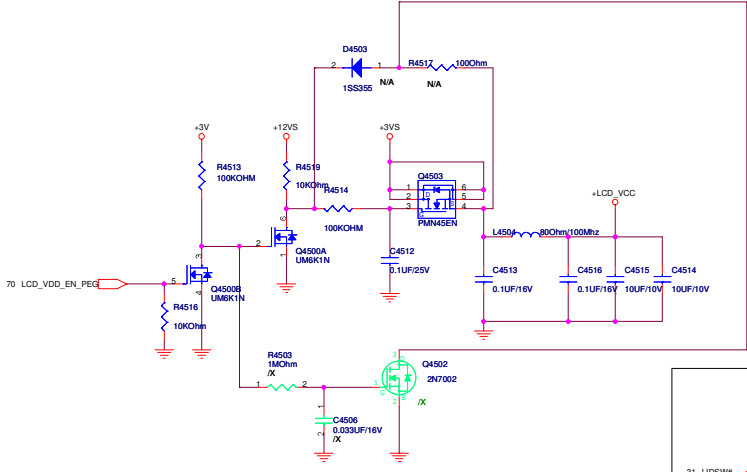
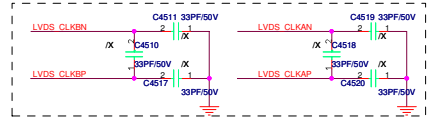
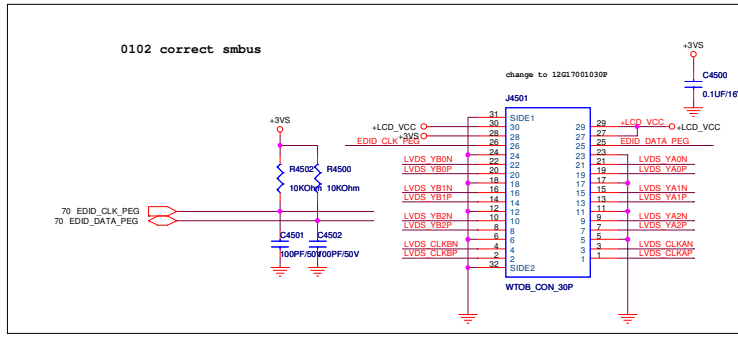
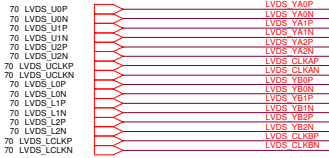


<Variant Name>

ASUS		Title : Express Card	
ASUSTeK COMPUTER INC		Engineer:	
Site:	Project Name:	Rev:	0.1
Custom:	ASZ/X80Z/F8T	Date:	Wednesday, March 12, 2008
Date: Wednesday, March 12, 2008		Sheet:	44 of 92

<< MaryL_Liu >>

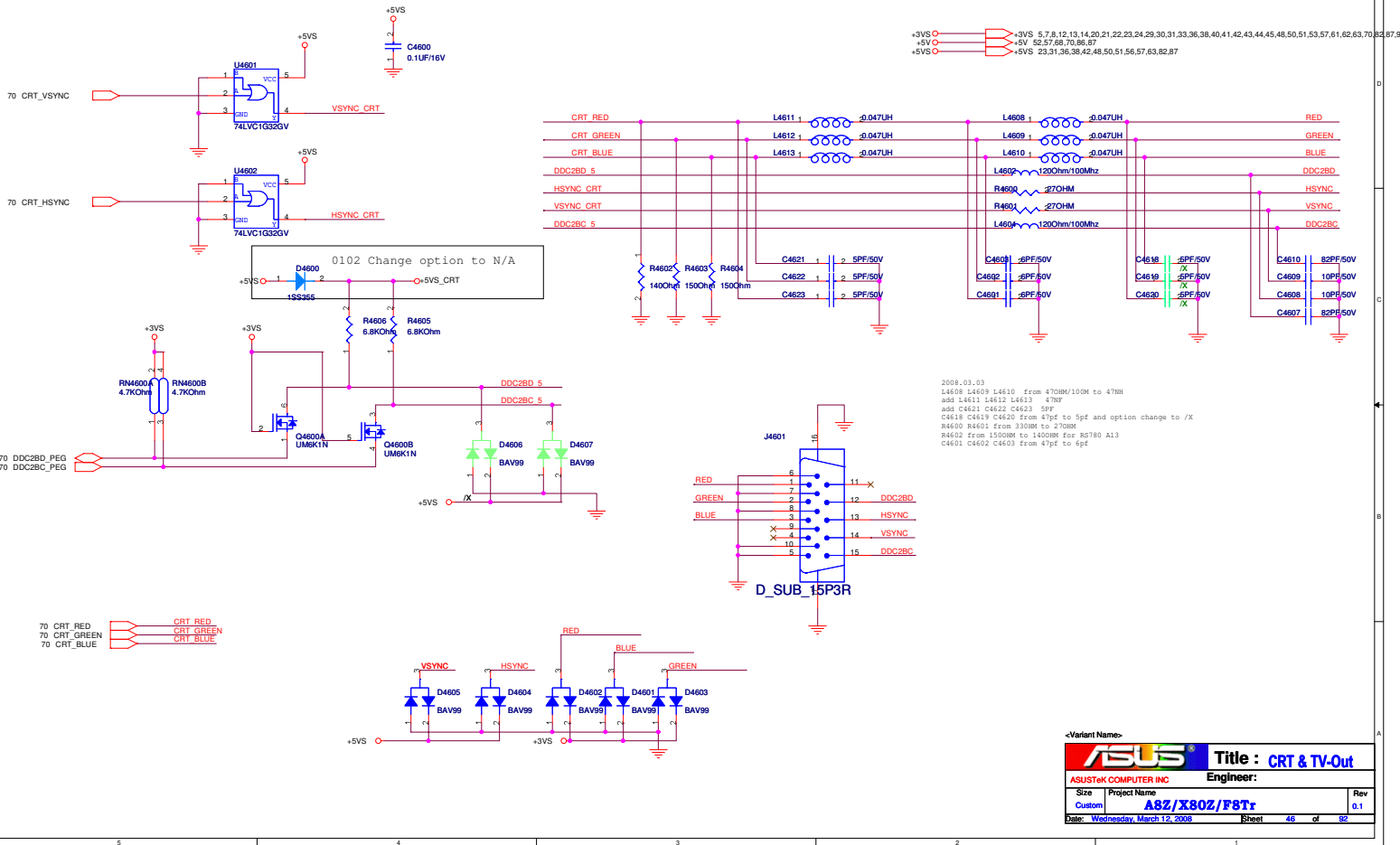
+3VS 5,7,8,12,13,14,20,21,22,23,24,29,30,31,33,36,38,40,41,42,43,44,46,48,50,51,53,57,61,62,63,70,82,83
 +3VSUS 4,20,21,22,23,24,30,33,43,44,53,83
 +12VS 36,42,57,70,87,91



<Variant Name>


ASUS		Title : LVDS & Inverter	
ASUSTEK COMPUTER INC		Engineer:	
Site	Project Name	Rev	
Custom	ABZ/X80/F8Tr	0.1	
Date: Wednesday, March 12, 2008	Sheet	45	of 82

<< MaryL_Liu >>

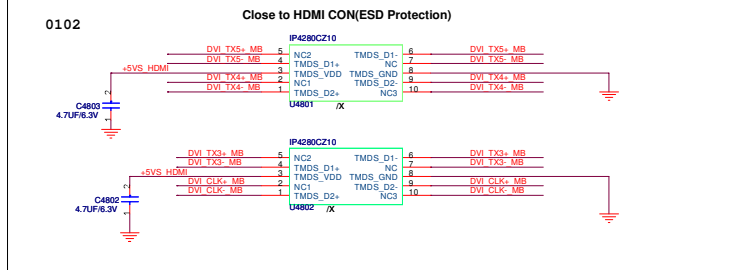


ASUS		Title : CRT & TV-Out	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	ABZ/X80Z/F8Tr	0.1	
Date: Wednesday, March 12, 2008	Sheet	46	of 92

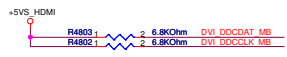
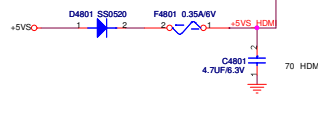
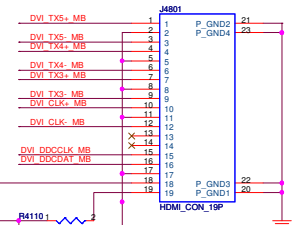
<< MaryL_Liu >>

<Variant Name>		
		Title : DVL*****
ASUSTeK COMPUTER INC		Engineer:
Size B	Project Name A8Z/X80Z/F8Tr	Rev 0.1
Date: Wednesday, March 12, 2008		Sheet 47 of 92

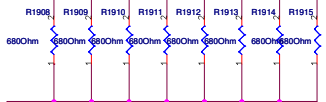
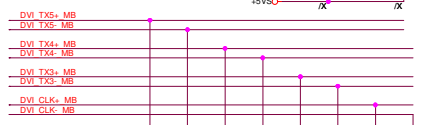
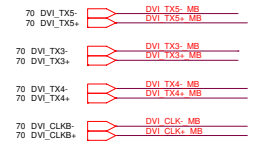
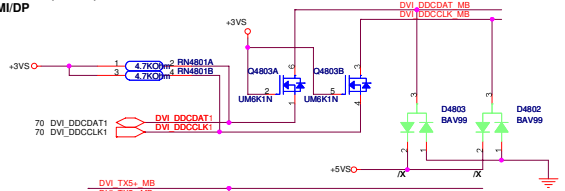
<< MaryL_Liu >>



HDMI CON



DDPC_CTRLDATA Strapping:(Port C)
Low = No HDMI/DP (default)
High = HDMI/DP




2008_03_10
R1908, R1909, R1910, R1911, R1912, R1913, R1914, R1915 change to 680Ohm



only for A8Z and X80Z

ASUS		Title : HDMI	
ASUSTAY COMPUTER INC. HKS		Engineer: Wing Cheng	
Size	Project Name	Rev	
Custom	A8Z/X80Z/F8T	0.1	
Date: Wednesday, March 12 2008		Sheet	48 of 92

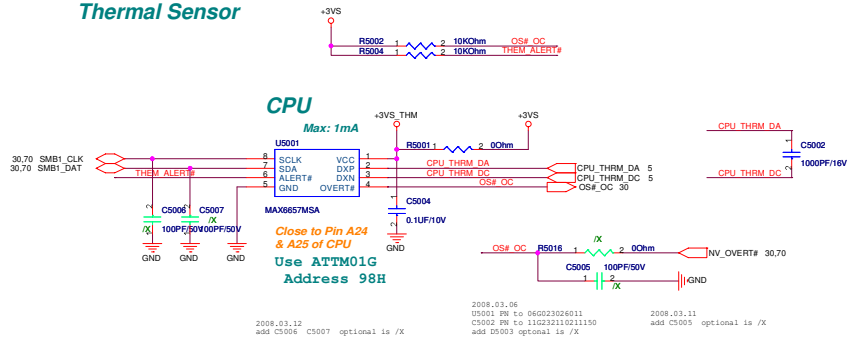
<< MaryL_Liu >>

		Title :
ASUSTeK COMPUTER INC. NB6		Engineer: <i>Wing Cheng</i>
Size	Project Name	Rev
A	ASZ/X80Z/F8Tr	0.1
Date: <u>Wednesday, March 12, 2008</u>		Sheet <u>49</u> of <u>92</u>

<< MaryL_Liu >>

Thermal Sensor

To EC

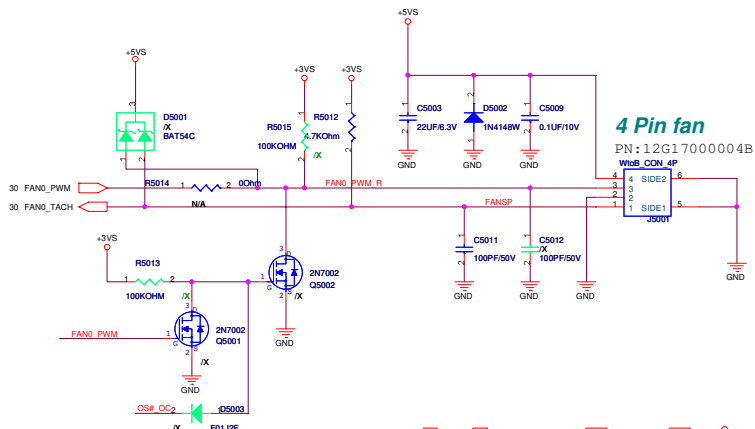


Route H_THERMDA and H_THERMDC on the same layer

-----OTHER SIGNALS
15 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
15 mils
-----OTHER SIGNALS

Avoid FSB_Power

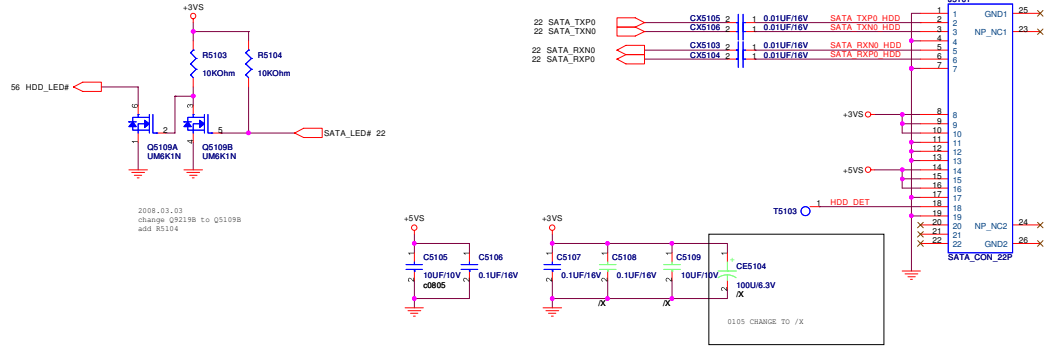
DC FAN Control



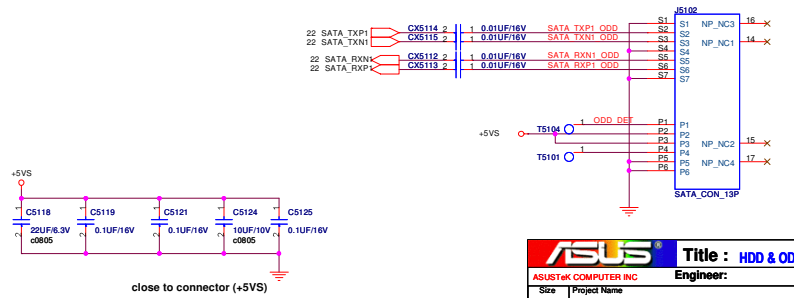
ASUS		Title : THER SENSOR & FAN	
ASUSTek COMPUTER INC		Engineer: Richard Lu	
Size	Project Name	Rev	
Custom	ASZ/X80Z/F8T	0.1	
Date: Wednesday, March 12, 2008	Sheet	50	of 92

<< MaryL_Liu >>

SATA HDD CON



SATA ODD CON



ASUS		Title : HDD & ODD	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	ABZ/X80Z/F8T	01	
Date: Wednesday, March 15, 2006	Sheet	61	of 82

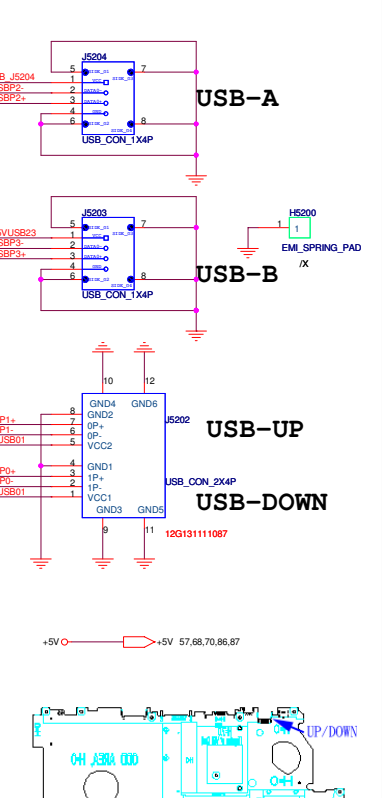
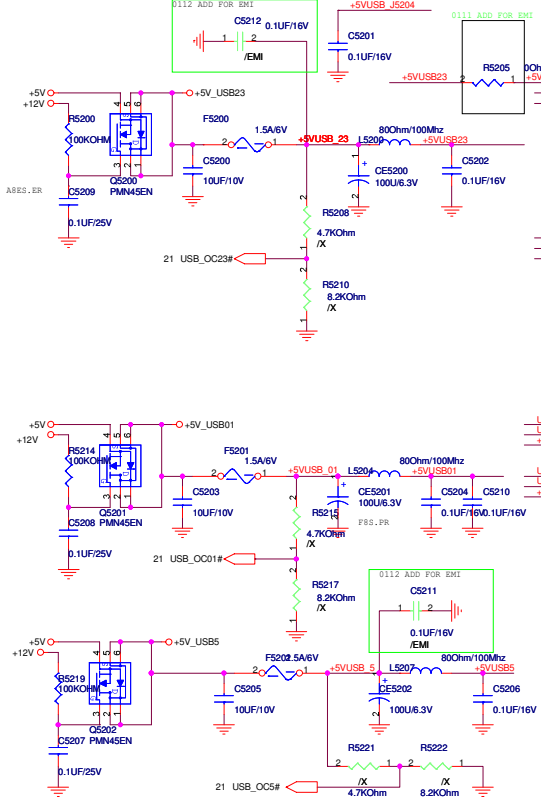
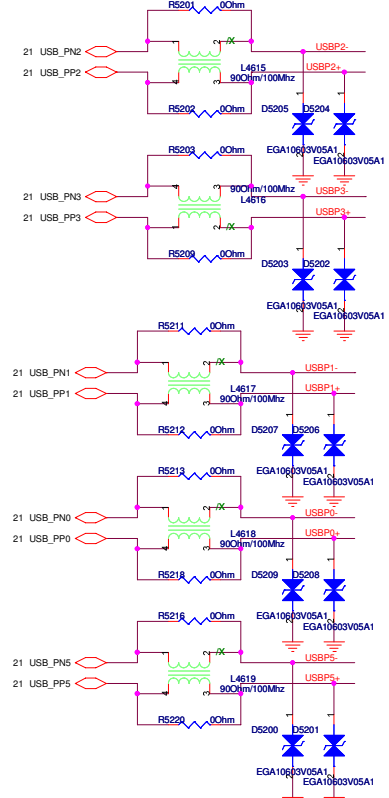
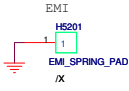
+3VS 5,7,12,13,14,20,21,22,23,24,29,30,31,33,36,38,40,41,42,43,44,45,46,48,50,53,57,61,62,63,70,82,87,91,92

+5VS 23,31,36,38,42,46,48,50,56,57,63,62,87

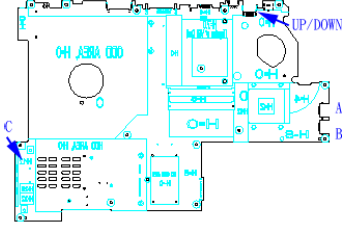
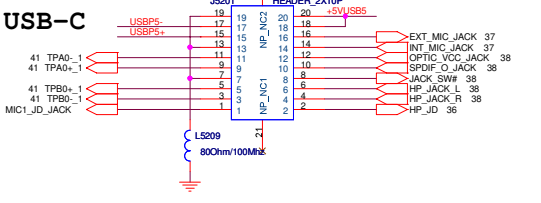
+5V 52,57,68,70,86,87

<< MaryL_Liu >>

ABES.PR
USB
common
choke
co-layer



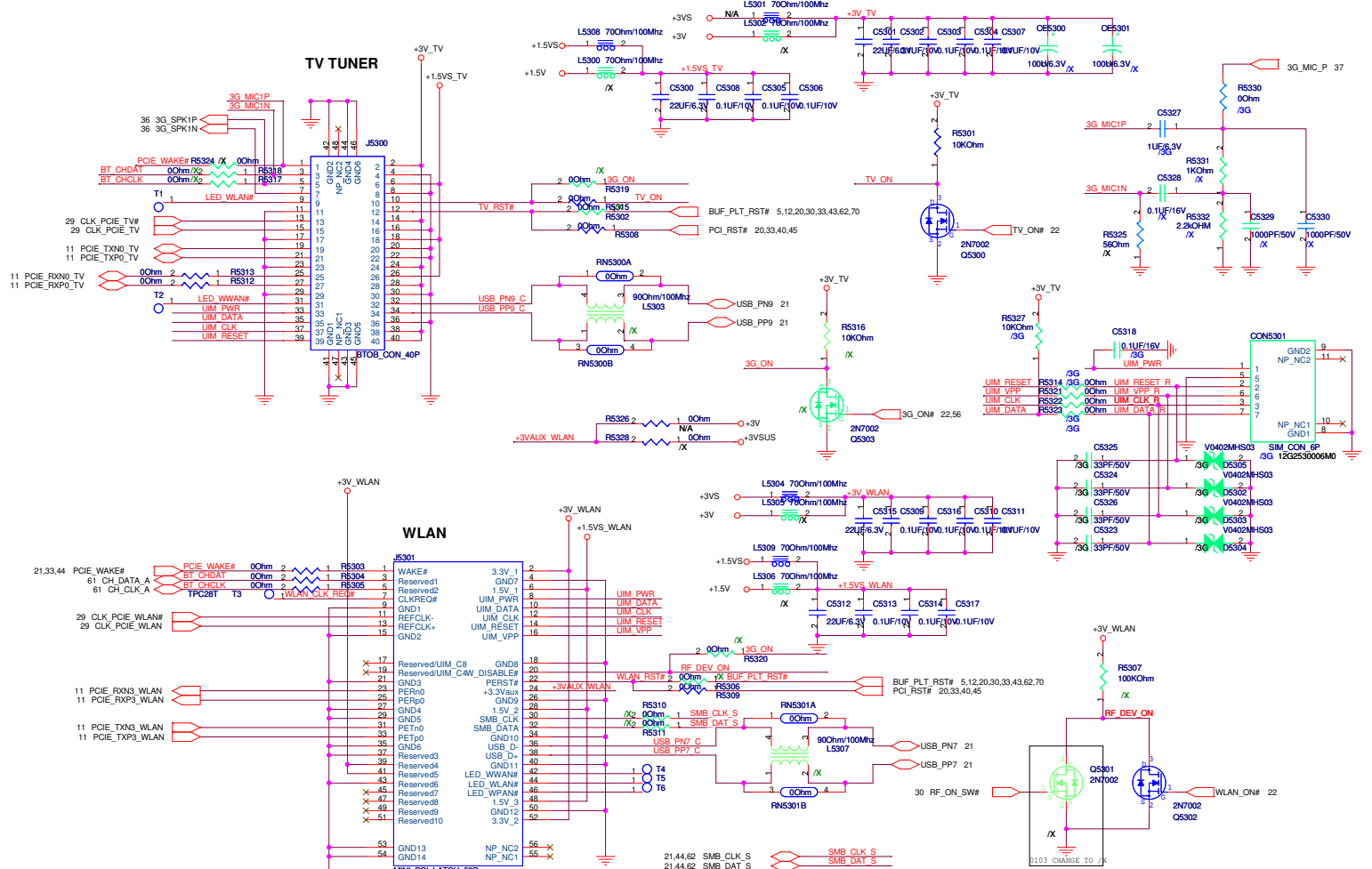
SUB-PCB: USB/1394/MIC/EARPHONE



<Variant Name>

ASUS		Title : USB/SUB PCB
ASUSTek COMPUTER INC		Engineer:
Size	Project Name	Rev
Custom	ABZ/X80Z/F8T	01
Date: Wednesday, March 12, 2008	Sheet	02 of 02

<< MaryL_Liu >>

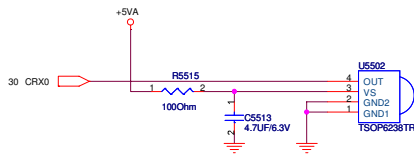


<< MaryL_Liu >>

		Title : BLANK	
ASUSTEK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	ASZ/X80Z/FSTr	0.1	
Date: Wednesday, March 12, 2008		Sheet	54 of 92

<< MaryL_Liu >>

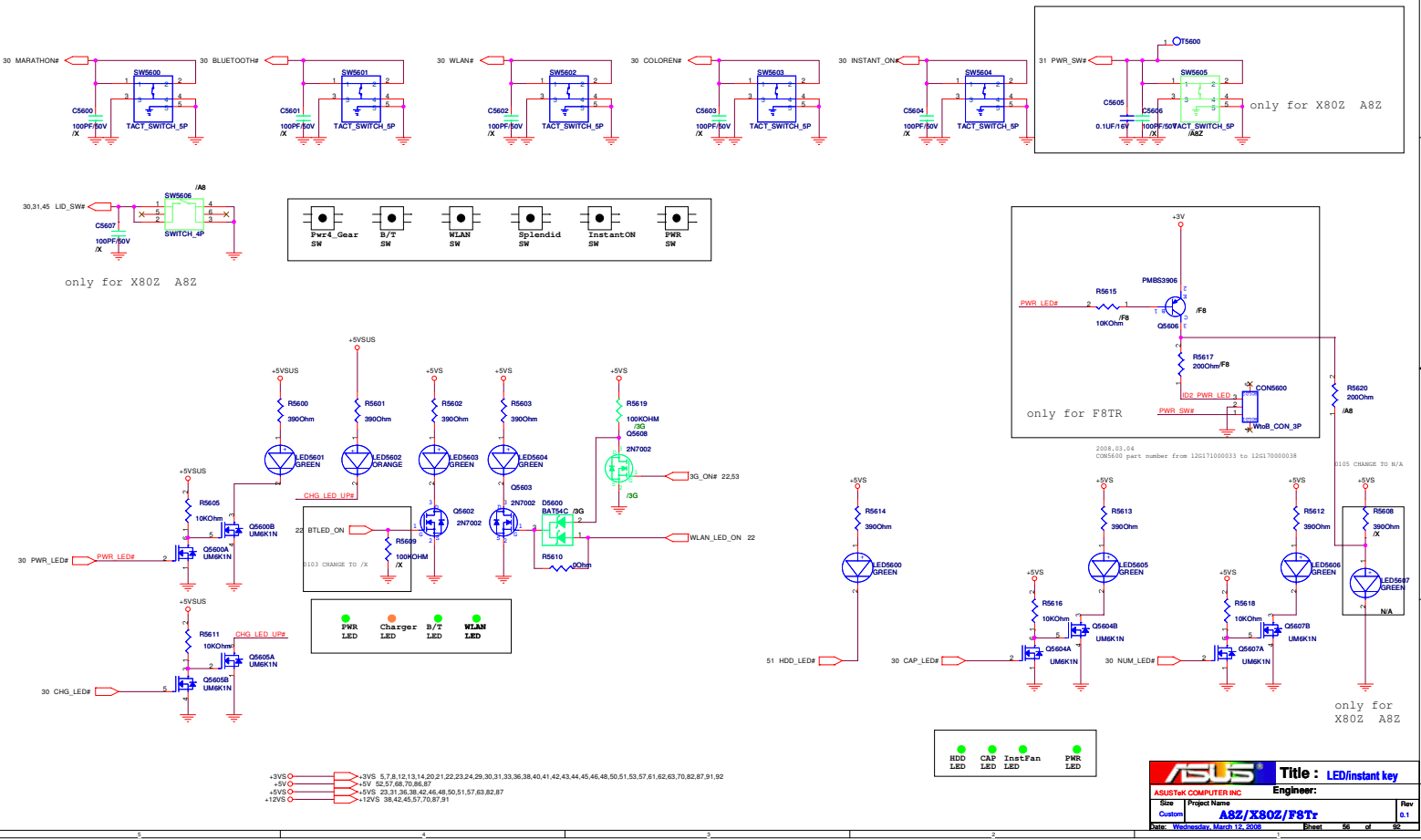
CIR
040231020500
TSOP6238TR



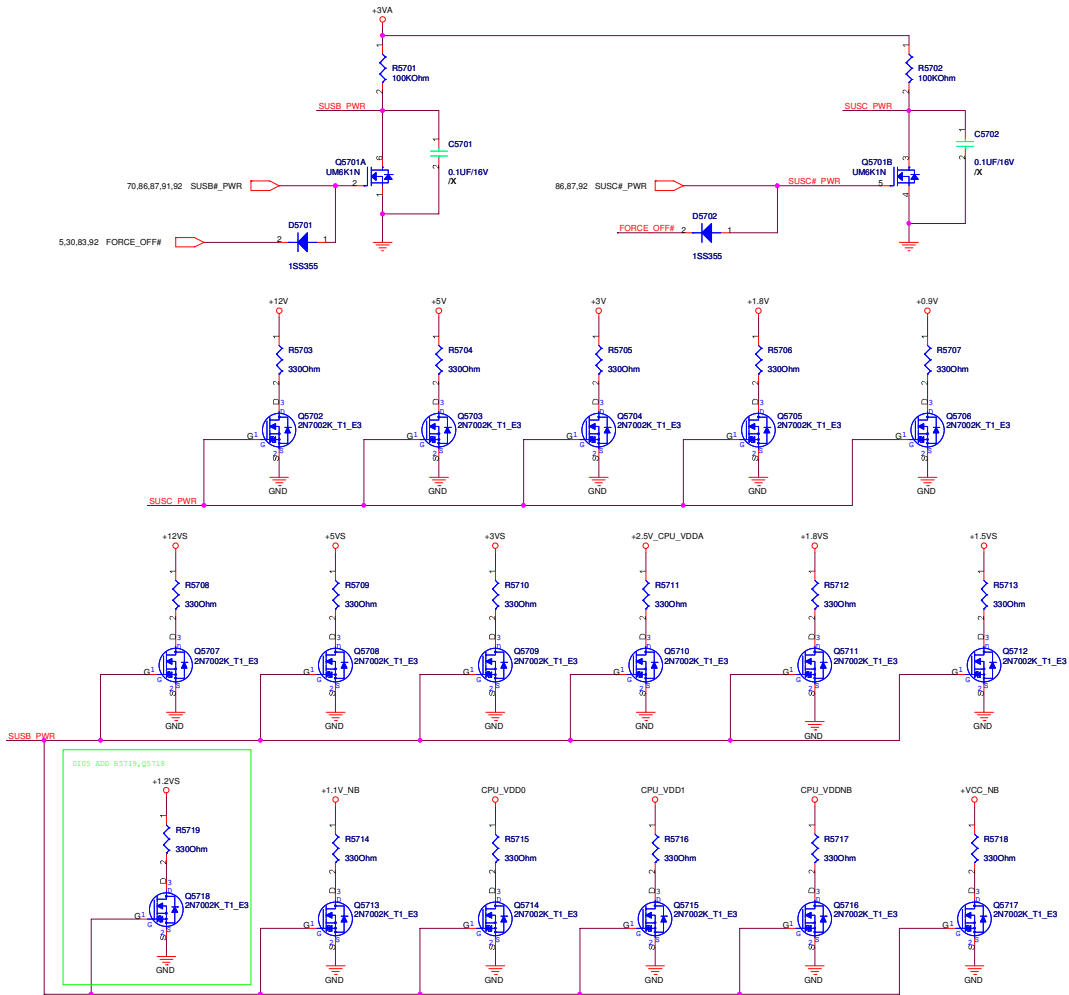
CIR for F8TR only

		Title : IrDA	
ASUSTeK COMPUTER INC		Engineer :	
Size	Project Name		Rev
B	A82/X80Z/F8Tr		0.1
Date: Wednesday, March 12, 2008		Sheet	55 of 82

<< MaryL_Liu >>




<< MaryL_Liu >>



ASUS		Title : DISCHARGE	
ASUSTEK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
A3	F6S	2.0	
Date: Wednesday, March 12, 2008		Sheet 57 of 92	

<< MaryL_Liu >>

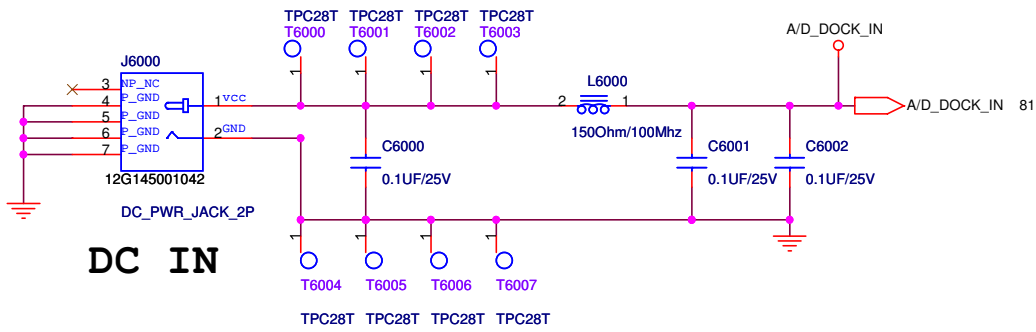
<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	Rev
A	ASZ/X80Z/F8Tr	0.1
Date: <u>Wednesday, March 12, 2008</u>		Sheet of 92

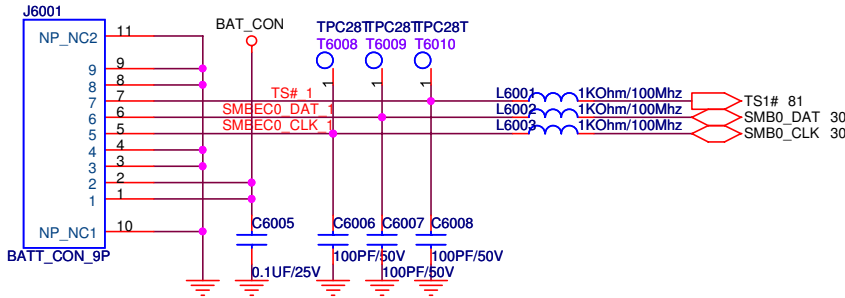
<< MaryL_Liu >>

Title		
<Title>		
Size	Document Number	Rev
A	A8Z/X80Z/F8Tr	0.1
Date:	Wednesday, March 12, 2008	Sheet 59 of 92

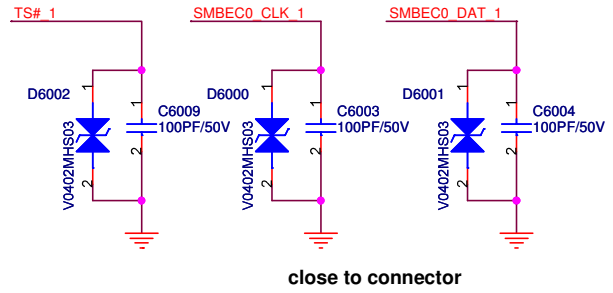
<< MaryL_Liu >>



DC IN



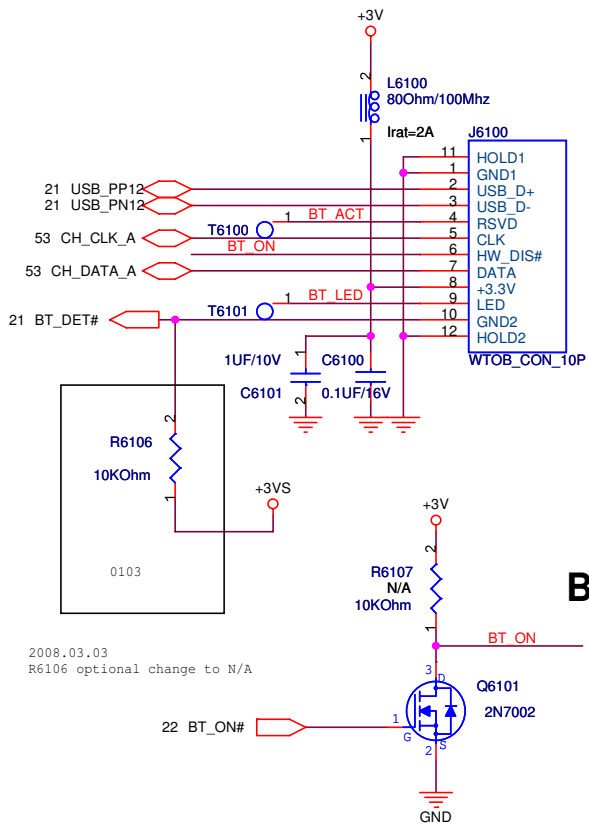
Battery Connector



<Variant Name>

ASUS		Title : DC IN / BAT	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8Z/X80Z/F8Tr		Rev 0.1
Date: Wednesday, March 12, 2008		Sheet 60 of 92	

<< MaryL_Liu >>



remove bluetooth for X80Z

Bluetooth Module CON

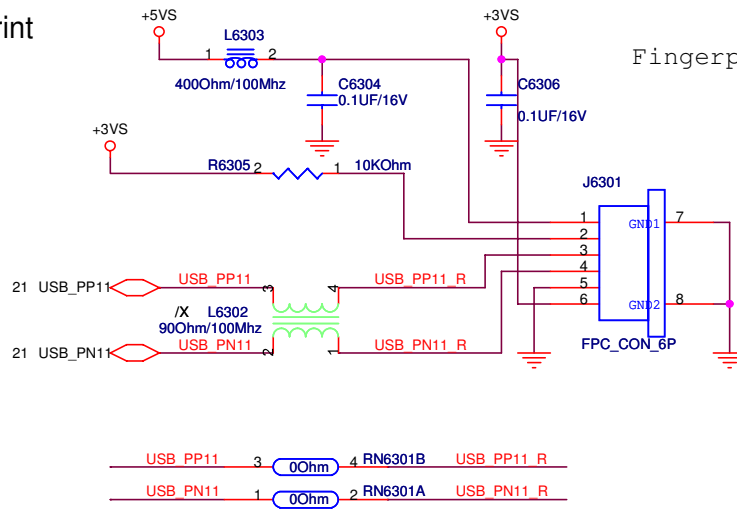
2008.03.03
R6106 optional change to N/A

ASUS		Title : BT/CAMERA	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name ASZ/X80Z/F8Tr		Rev 0.1
Date: Wednesday, March 12, 2008		Sheet	61 of 92

<< MaryL_Liu >>

Finger Print

Fingerprint for F8TR only



<Variant Name>

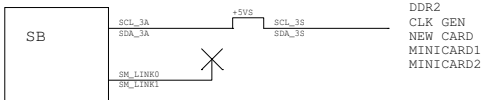
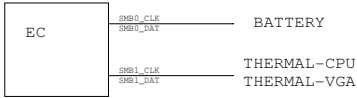
		Title :FingerPrinter
ASUSTeK COMPUTER INC		Engineer:
Size A	Project Name A8Z/X80Z/F8Tr	Rev 0.1
Date: Wednesday, March 12, 2008	Sheet 63 of 92	

«Maryl_Liu»

PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 (Internal)		
CARDBUS	AD19	0	F,E

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0 (low)	
SPD/TS	A0/30
SO-DIMM 1(high)	
SPD/TS	A4/34
G781-1	9A
G781(VGA board)	98

Thermal Sensor (CPU)
SM-Bus Mapping 1001100



BOM option

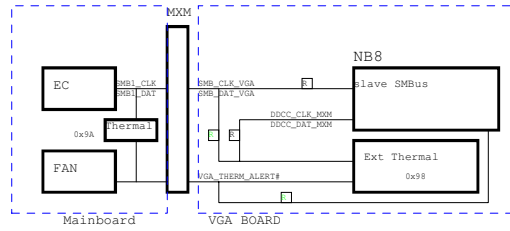
nGM:yellow
nPM:light red
=====

@ : no stuff for all
nGM :no stuff for A8E
nPM :no stuff for A8S
nGM1:no stuff for A8E, A8E/SR mount for debugging A8S in advance
3G :for Windigo,SIERRA MC8775V
nA8E :no stuff Irda for A8E

Support ID2:

Support ID2:
page 68,Finger print
page 55,IR
Page 56,pwr switch and LED

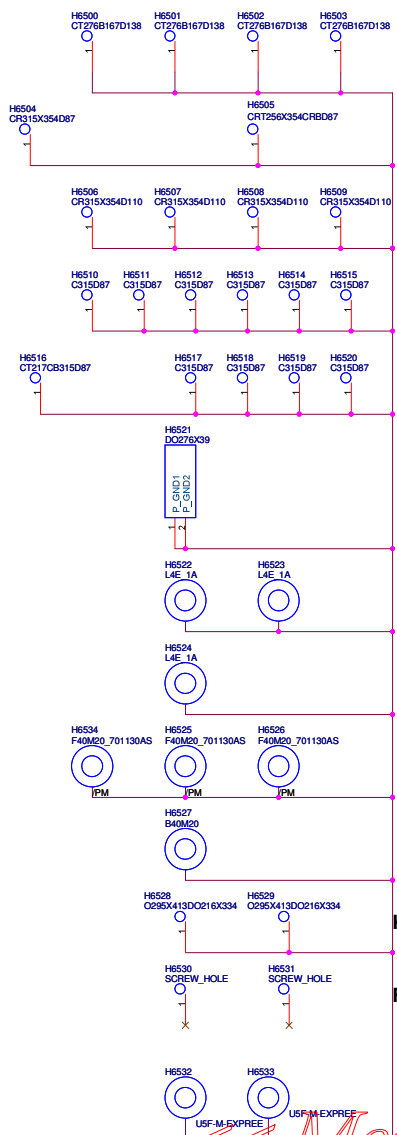
Thermal block diagram



<Variant Name>

ASUS		Title :
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	Rev
B	A8Z/X80Z/F8Tr	0.1
Date: Wednesday, March 12, 2008	Sheet	64 of 92

<< MaryL_Liu >>

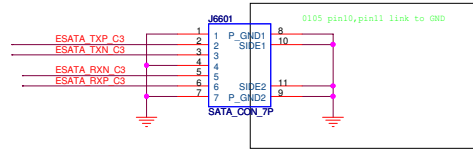


CPU
SCREW
U HOLE
SCREW
IO Board
MDC_NUT
TPM_NUT
VGA_NUT
KB_NUT
KEYBOARD
FIXED HOLE

←← MaryL_Liu →→
miniCard

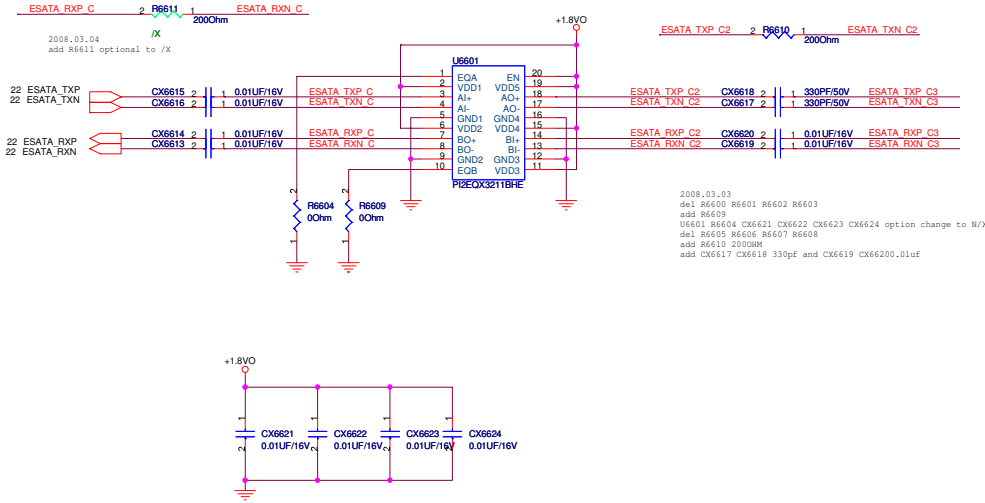
Title		Rev	
Document Number		0.1	
Customer: A8Z/X90Z/F8T			
Date: Wednesday, March 12, 2008	Sheet	65	of 92

PIN	FUNCTION
1	Gnd
2	A+
3	A-
4	Gnd
5	B-
6	B+
7	Gnd



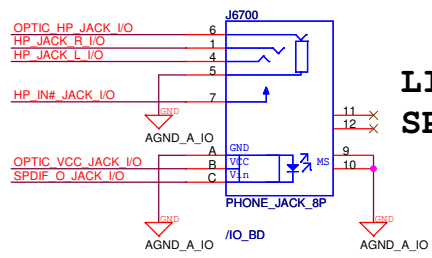
remove E-SATA for X80Z

0109 add re-driver

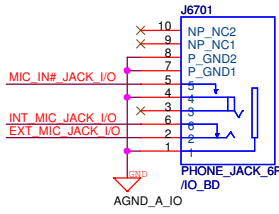


ASUS		Title : E-SATA
ASUSTek COMPUTER INC		Engineer:
Size	Project Name	Rev
B	A8Z/X80Z/F8Tr	0.1
Date: Wednesday, March 12, 2008		Sheet 66 of 92

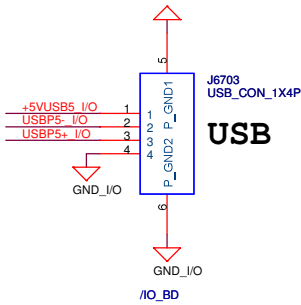
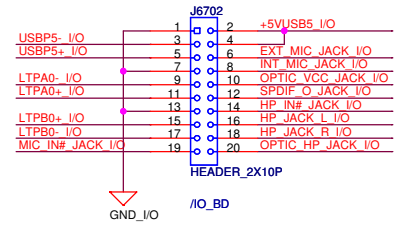
<< MaryL_Liu >>



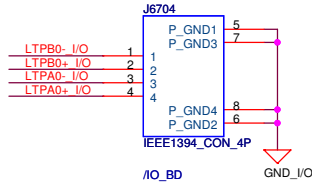
**LINE_OUT
SPDIF**



MIC

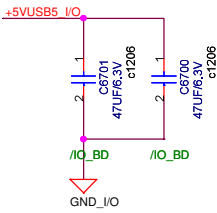


USB

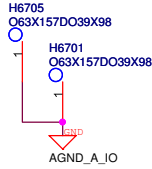
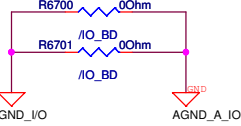


1394A

remove 1394 for X80Z



2008.03.10
add C6700 C6701

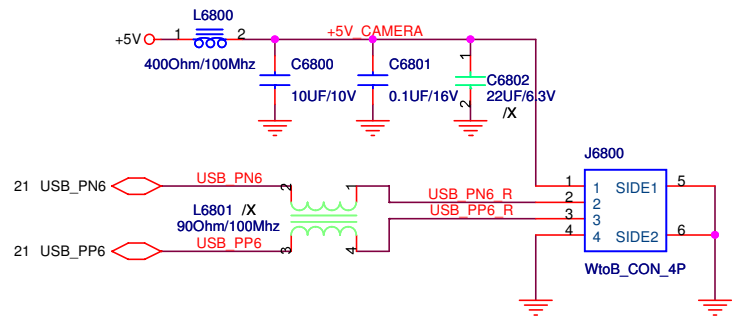


<Variant Name>

ASUS		Title :SUB_PCB	
ASUSTeK COMPUTER INC		Engineer:	
Size A4	Project Name A8Z/X80Z/F8Tr	Date: Wednesday, March 12, 2008	Rev 0.1
		Sheet 67	of 92

<< MaryL_Liu >>


Camera



<Variant Name>

		Title :CAMERA
ASUSTeK COMPUTER INC		Engineer:
Size A	Project Name A8Z/X80Z/F8Tr	Rev 0.1
Date: Wednesday, March 12, 2008	Sheet 60	of 92

<< MaryL_Liu >>

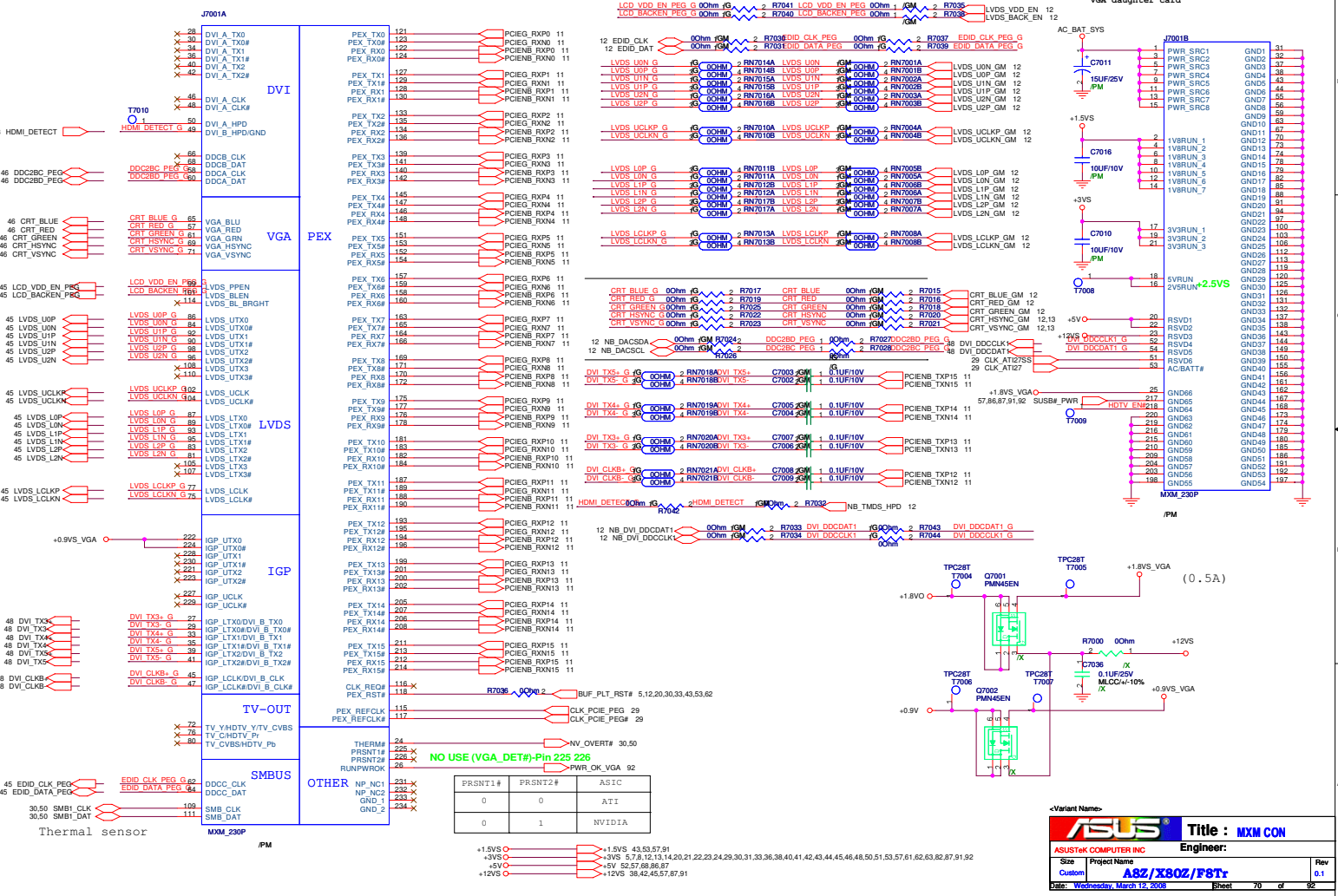
		Title : Other
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	Rev
A	ASZ/X80Z/F8Tr	0.1
Date: Wednesday, March 12, 2008		Sheet 69 of 92

<< MaryL_Liu >>

only for F8TR

RESISTORS CLOSE TO MXM

+2.5VS design always on VGA daughter card



ASUS Title: MXM CON

ASUSTEK COMPUTER INC Engineer:

Size Project Name: A8Z/X80Z/F8TR Rev: 0.1

Custom Date: Wednesday, March 12, 2008 Sheet: 70 of 82

<< MaryL_Liu >>

D

D

C

C

B

B

A

A

<< *MaryL_Liu* >>

Title		
TITLE		
Size	Document Number	Rev
A3	AB22802/F&T	0.1
Date:	Wednesday, March 12, 2008	Sheet 71 of 82

D

D

C

C

B

B

A

A

<< *MaryL_Liu* >>

Title		
TITLE		
Size	Document Number	Rev
A3	AB22802/F&T	0.1
Date:	Wednesday, March 12, 2008	Sheet 72 of 82

5

4

3

2

1

D

D

C

C

B

B

A

A

5

4

3

2

1

<< *MaryL_Liu* >>

Title		
TITLE		
Size	Document Number	Rev
A3	AB22802/F6T1	0.1
Date:	Wednesday, March 12, 2008	Sheet 73 of 82

D

D

C

C

B

B

A

A

<< *MaryL_Liu* >>

Title		
TITLE		
Size	Document Number	Rev
A3	AB22802/F6T1	0.1
Date:	Wednesday, March 12, 2008	Sheet 74 of 82

D

D

C

C

B

B

A

A

<< *MaryL_Liu* >>

Title		
TITLE		
Size	Document Number	Rev
A3	AB22802/F&T	0.1
Date:	Wednesday, March 12, 2008	Sheet 75 of 82

5

4

3

2

1

D

D

C

C

B

B

A

A

5

4

3

2

1

<< *MaryL_Liu* >>

Title		
TITLE		
Size	Document Number	Rev
A3	AB22802/F&T	0.1
Date:	Wednesday, March 12, 2008	Sheet 78 of 82

5

4

3

2

1

D

D

C

C

B

B

A

A

5

4

3

2

1

<< *MaryL_Liu* >>

Title		
TITLE		
Size	Document Number	Rev
A3	AB22802/F&T	0.1
Date:	Wednesday, March 12, 2008	Sheet 77 of 82

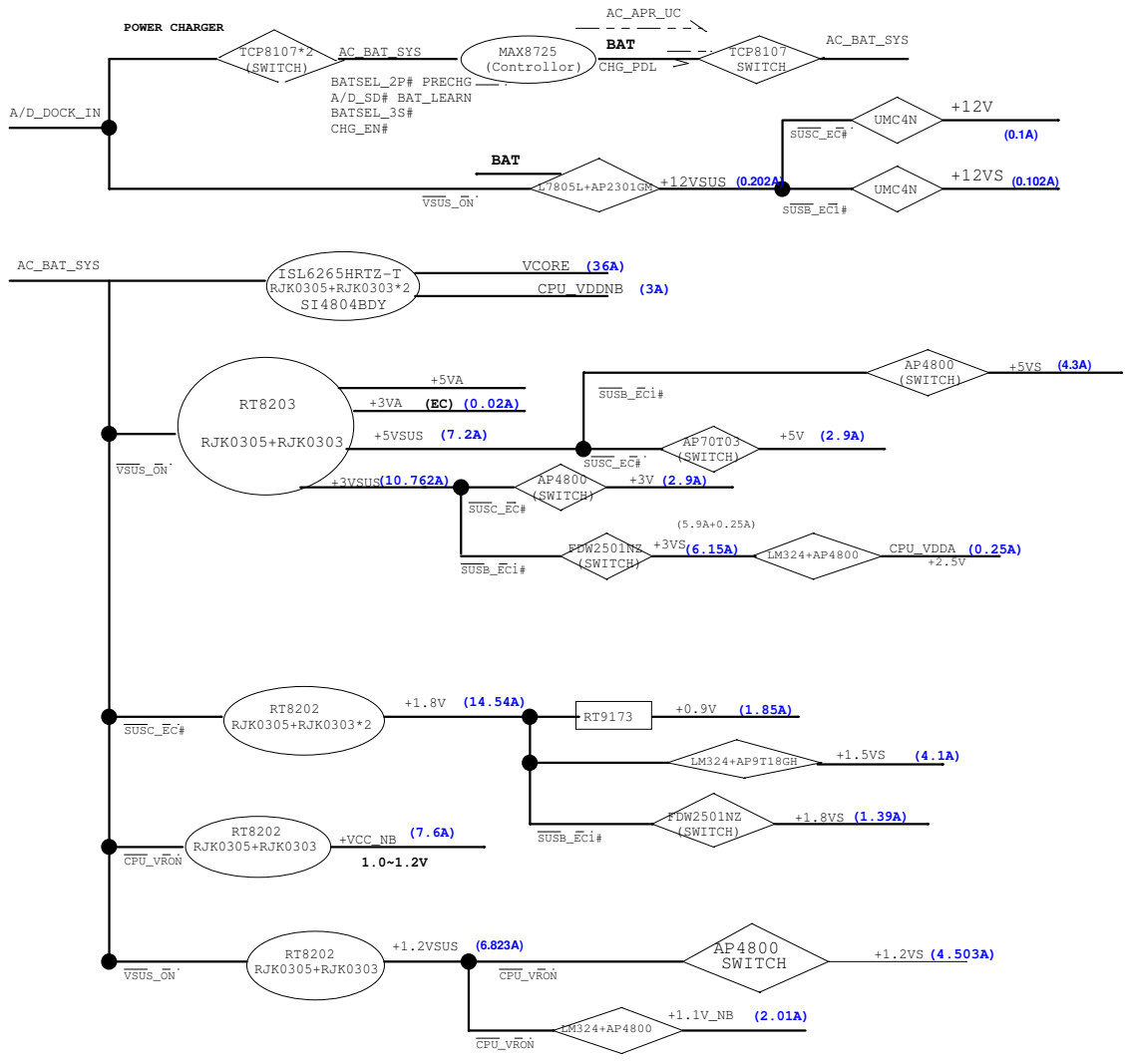
		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
B	A8Z/X80Z/F8Tr	0.1	
Date: Wednesday, March 12, 2008		Sheet	78 of 92

<< MaryL_Liu >>

REVISION LIST

		TIME : History
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	Rev
AS2	AS2/ X302/ FSTy	1.0
Date: 2008/05/14 10:00:00		Page 2 of 2

<< MaryL_Liu >>



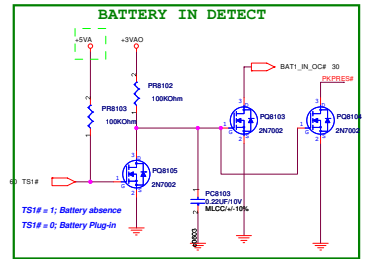
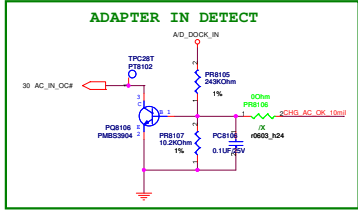
Variant Name:

ASUS		Title : POWER FLOW	
ASUSTEK COMPUTER INC		Engineer: N/A	
Size:	Project Name:	Rev:	1.0
P: P&TR		Date: Wednesday, March 12, 2008	Sheet: 80 of 82

<< MaryL_Liu >>

POWER PATH & BAT_LEARN

AC_IN Threshold 2.049Vmax AD_DOCK_IN > 1.570V active
 Adapter Inhibit = $(0.075V/Rsense(ADIN)) \times (VCLL5/VREF)$
 Resense(ADIN) = 0.15 Ohm
 VCLL5 = 3.301V
 VREF = 1.025V
 => Constant Power = $19 \times 4.5 = 85.5W$
 => P IM = 15.15W/PR5100-100V
 Charge Current Ichg = $(0.075V/Rsense(CHG)) \times (VCTL3/V4)$
 Resense(CHG) = 15m Ohm
 VCTL3 = 1.850V => Ichg = 2.63A
 VCTL4 = 1.810V => Ichg = 1.401A
 Vref = Cell 1 Vref = $(VCTL - 1.8V) / 1.95[1]$
 VCTL = 1.558V
 => Vref = 4.2V
 VCTL = 0.8V or DCIN < 7V => Charger Disable



MODE (Pin7) Battery
 High (>2.8V) 4-Cell
 Low (<0.8V) 3-Cell
 High Impedance Battery Learn
 (1.6V - Vmoco = 2V)

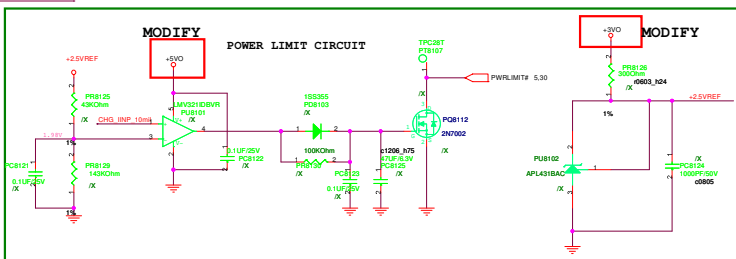
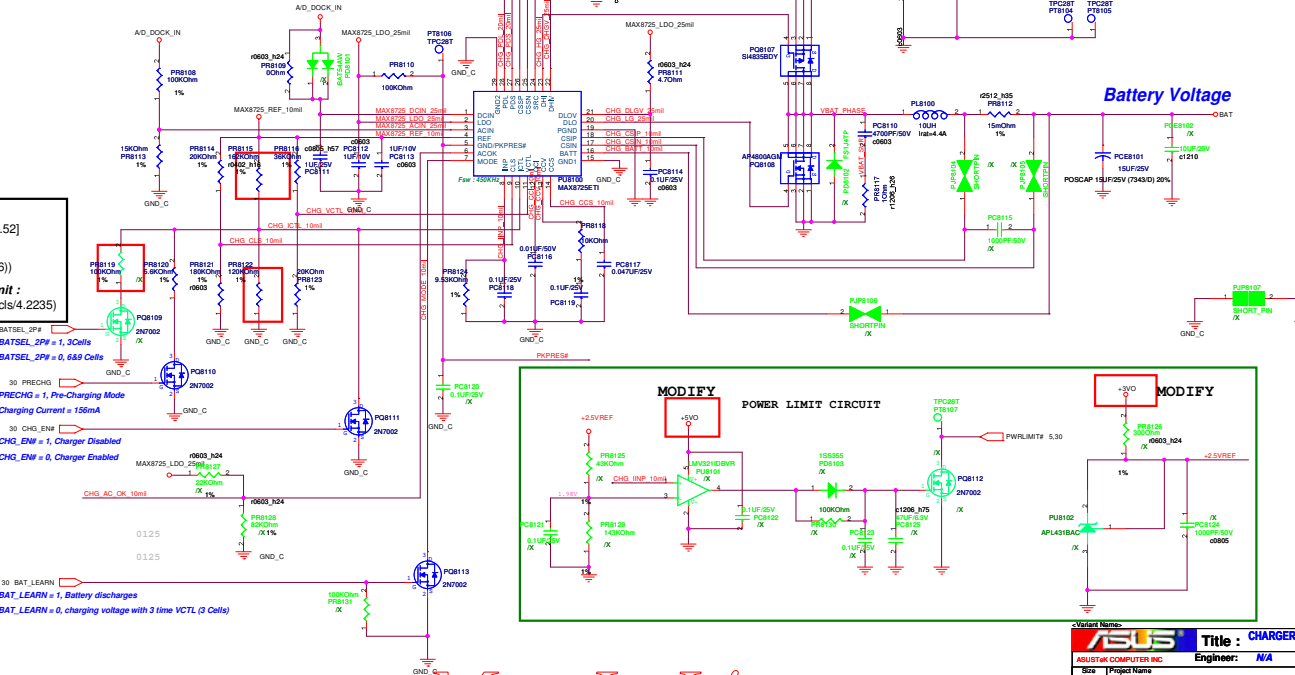
Battery Charging Voltage :
 $+V_BAT = 4 \times [4.2235 + (Vctl - 1.8) / 9.52]$
Battery Charging Current :
 $I_{charge} = (0.075 / PR5706) \times (Vctl / 3.6)$
Input Adaptor Max. Current Limit :
 $I_{limit_current} = (0.075 / PR5701) \times (Vds / 4.2235)$

Pre-Charging Mode :
 Precharging current = 190.5mA
 $V_{ctl} = 0.137V$

Battery Cell Selection :
 BATSSEL_2P# = 1, 3 Cells; Vctl = 1.058V
 Charging Current = 156mA
 $\Rightarrow I_{charge} = 1.469A$
 BATSSEL_2P# = 0, 6 Cells; Vctl = 1.836V
 $\Rightarrow I_{charge} = 2.55A$

A/D_SDI# = 1, Enable charger
 A/D_SDI# = 0, Disable charger

30 BAT_LEARN = 1, Battery discharges
 BAT_LEARN = 0, charging voltage with 3 time VCTL (3 Cells)



ASUS		Title: CHARGER	
ASUSTEK COMPUTER INC.		Engineer: N/A	
Size	Project Name	Rev	1/8
C	P6TR		
Date: Wednesday, March 12, 2008		Sheet	81 of 85

<< MaryL_Liu >>

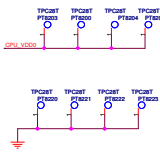
ISL6245 Pin#	QFS	VFIXEN
1.2V	V	X
3.3V	X	V
5V	X	X
Pre_Metal	X	X

Design Current : 2.1A
Maximum current : 3A
OCP point Typ. : 6A

CPU_VDDNB

5 CPU_VDDNB_RUN_FB_L
5 CPU_VDDNB_RUN_FB_H
CPU_VDDNB

SVC	SVID	Output	Pre_Metal
0	0	1.8	1.8
0	1	1.2	1.0
1	0	1.0	0.9
1	1	0.8	0.8

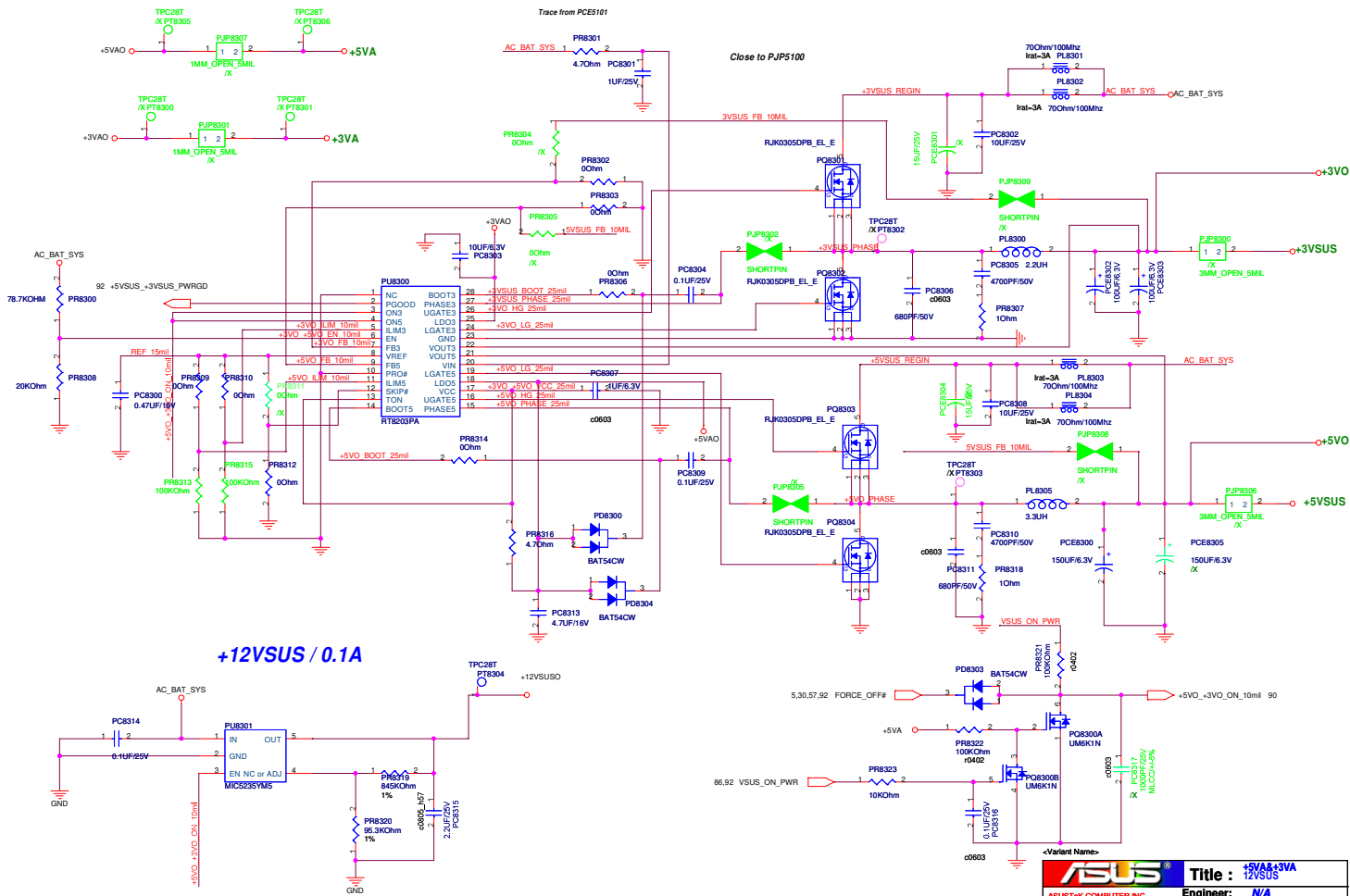


Design Current : 14.4A
Maximum current : 18A
OCP point Typ. : 30A

Design Current : 14.4A
Maximum current : 18A
OCP point Typ. : 30A

ASUS TITLE : VCORE
ASUSTeK COMPUTER INC. Engineer: NFA
Rev: 1.0
Date: 2008.03.10
PSTR

<< MaryL_Liu >>



+12VSUS / 0.1A

ASUS		Title : +5VAO/+3VA 12VSUS
ASUSTeK COMPUTER INC		Engineer : N/A
Size	Project Name	Rev
Custom	F6TR	1.0
Date: Wednesday, March 12, 2008	Sheet	83 of 92

« MaryL_Liu »

5

4

3

2

1

D

D

C

C

B

B

A

A

5

4

3

2

1

<< MaryL_Liu >>

		Title : <Title>	
<OrigName>		Engineer: <i>chang-sheng liu</i>	
Size	Project Name	Rev	
A3	<Doc>	1.00	
Date: <i>Wednesday, March 12, 2008</i>		Sheet <i>84</i> of <i>92</i>	

5

4

3

2

1

D

D

C

C

B

B

A

A

5

4

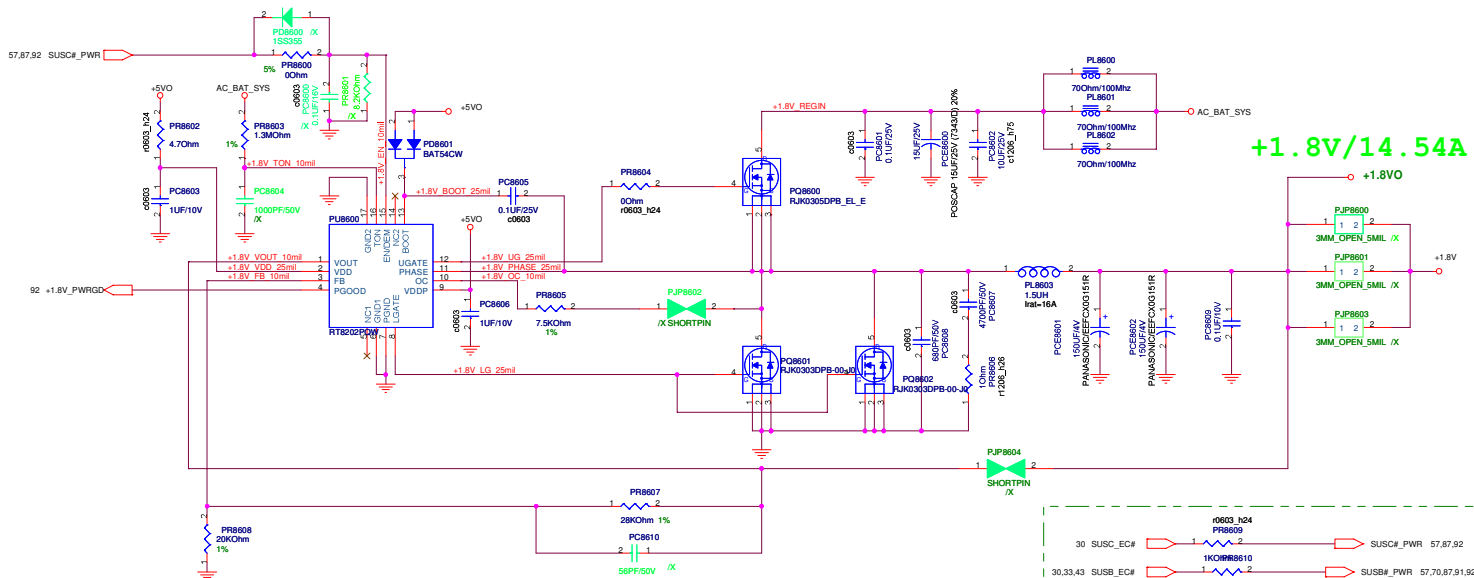
3

2

1

		Title : <Title>	
-<CryName>		Engineer: <i>chang-sheng_liu</i>	
Size	Project Name	Rev	
A3	<Doc>	1.00	
Date: <i>Wednesday, March 19, 2008</i>		Sheet	85 of 92

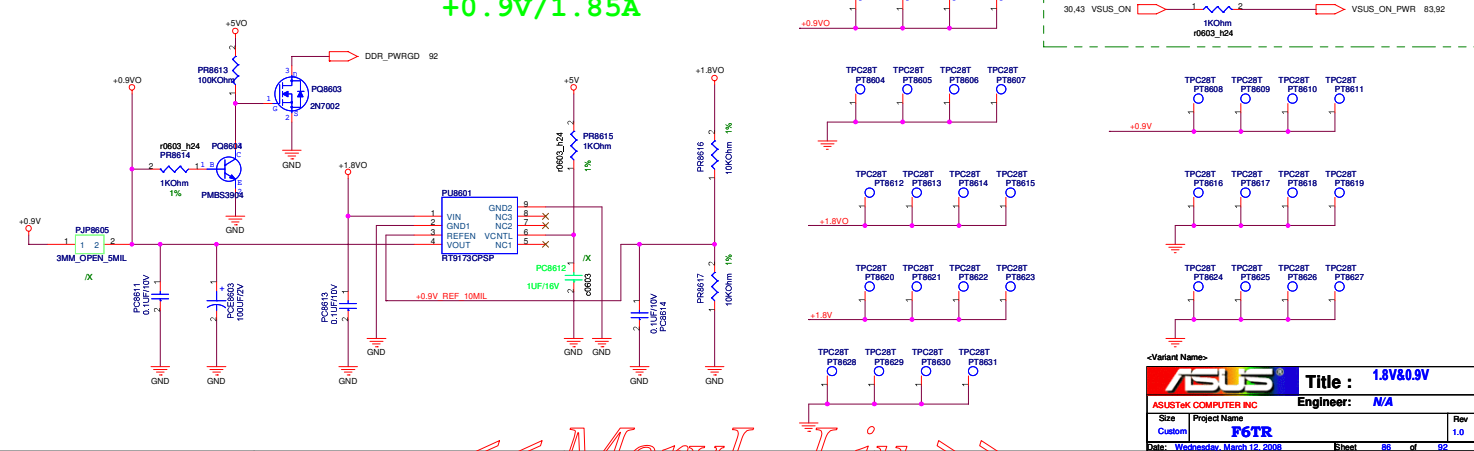
<< *MaryL_Liu* >>



+1.8V/14.54A

+1.8V0

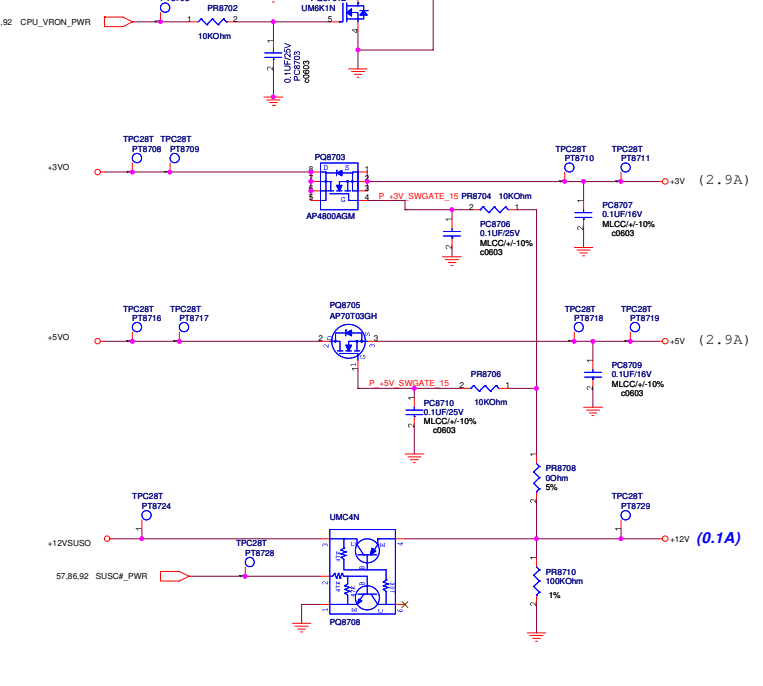
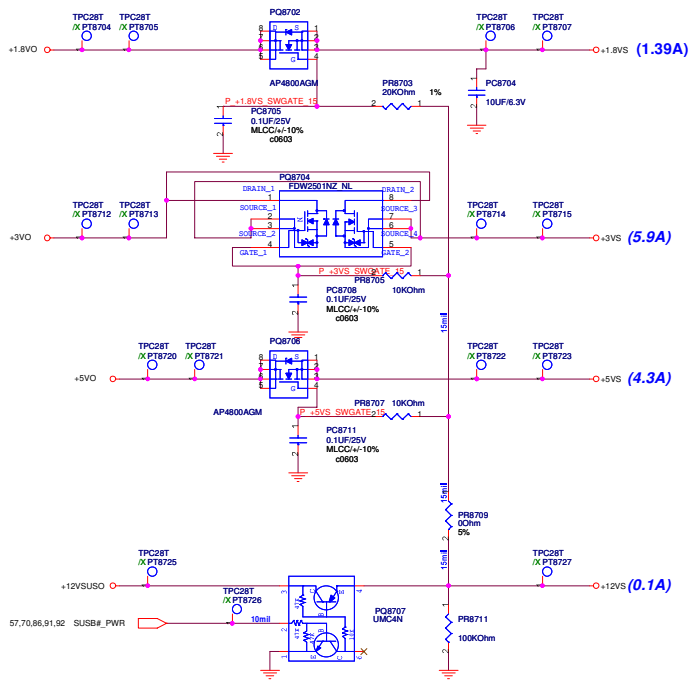
+0.9V/1.85A



<Variant Name>

ASUS		Title : 1.8V&0.9V	
ASUSTeK COMPUTER INC		Engineer : N/A	
Size	Project Name	Rev	
Custom	F6TR	1.0	
Date : Wednesday, March 12, 2008	Sheet	86	of 92

<< MaryL_Liu >>



<Variant Name>

ASUS		Title : LOAD SWITCH	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
A3	P6TR		1.0
Date: Wednesday, March 12, 2008		Sheet	87 of 92

<< MaryL_Liu >>

5

4

3

2

1

D

D

C

C

B

B

A

A

5

4

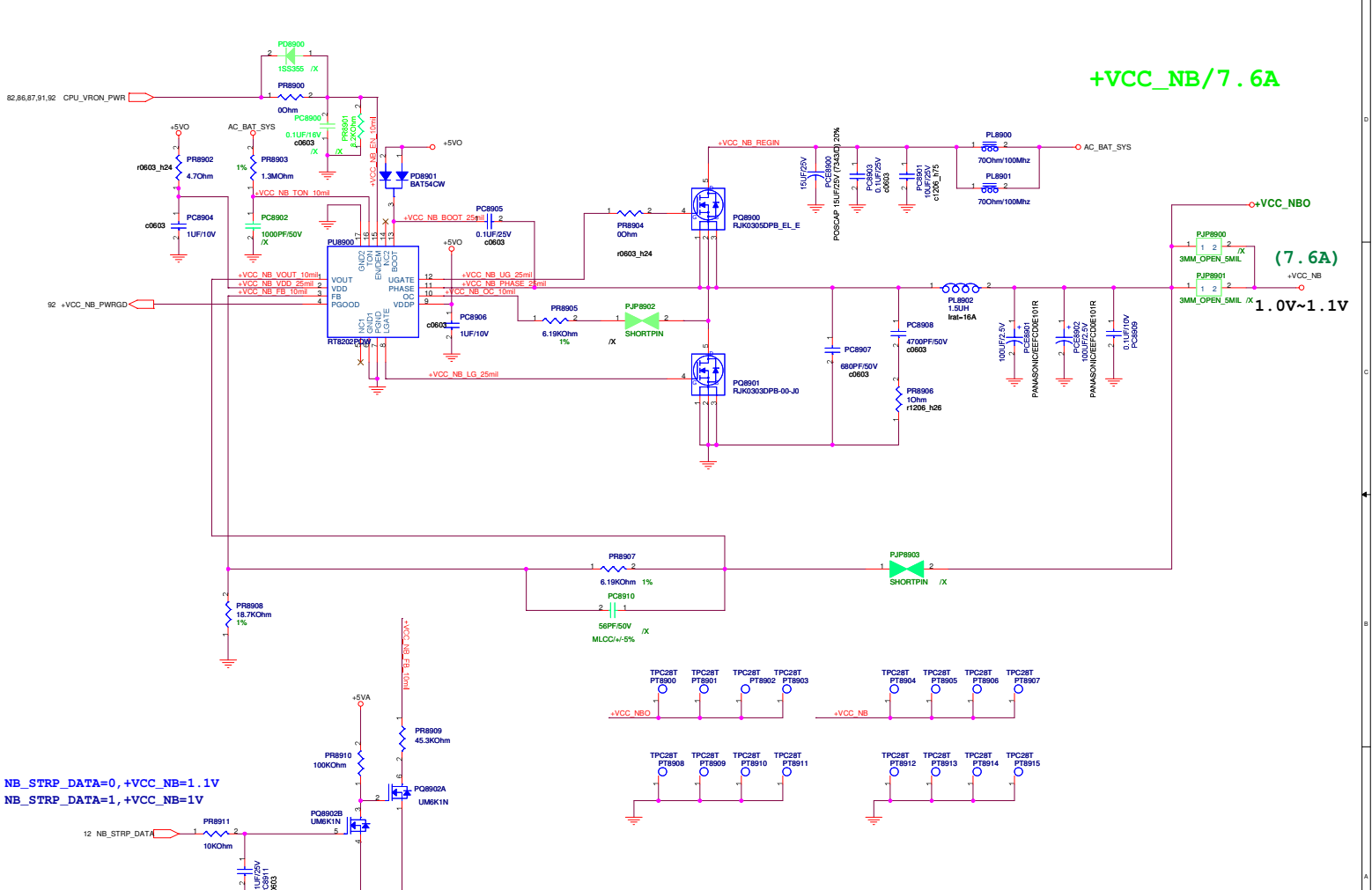
3

2

1

<< MaryL_Liu >>

		Title : <Title>	
<OrigName>		Engineer: <i>chang-sheng_lu</i>	
Size	Project Name		Rev
A3	<Doc>		1.00
Date: Wednesday, March 12, 2008		Sheet	88 of 82



+VCC_NB/7.6A

(7.6A)

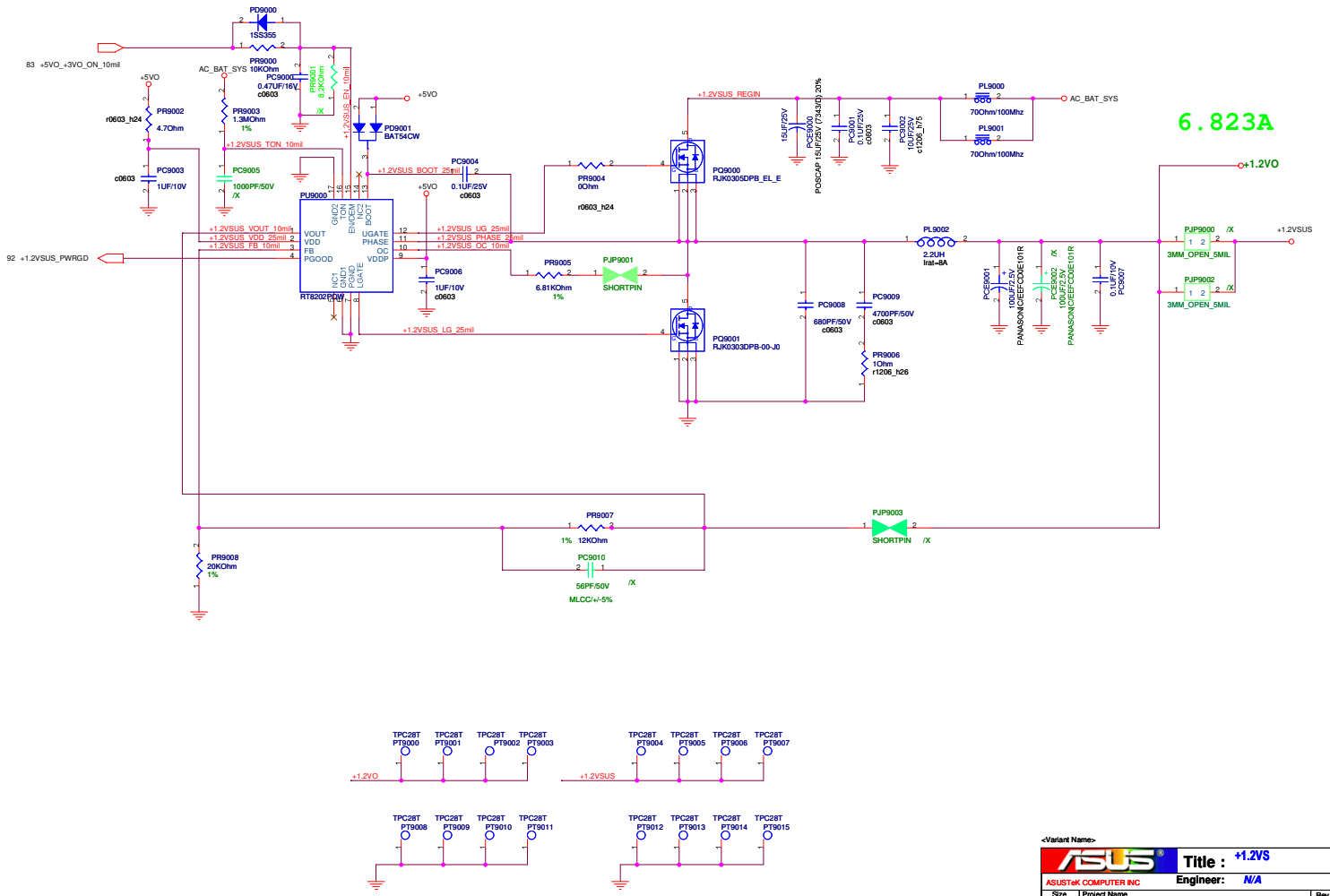
1.0V~1.1V

NB_STRP_DATA=0, +VCC_NB=1.1V
 NB_STRP_DATA=1, +VCC_NB=1V

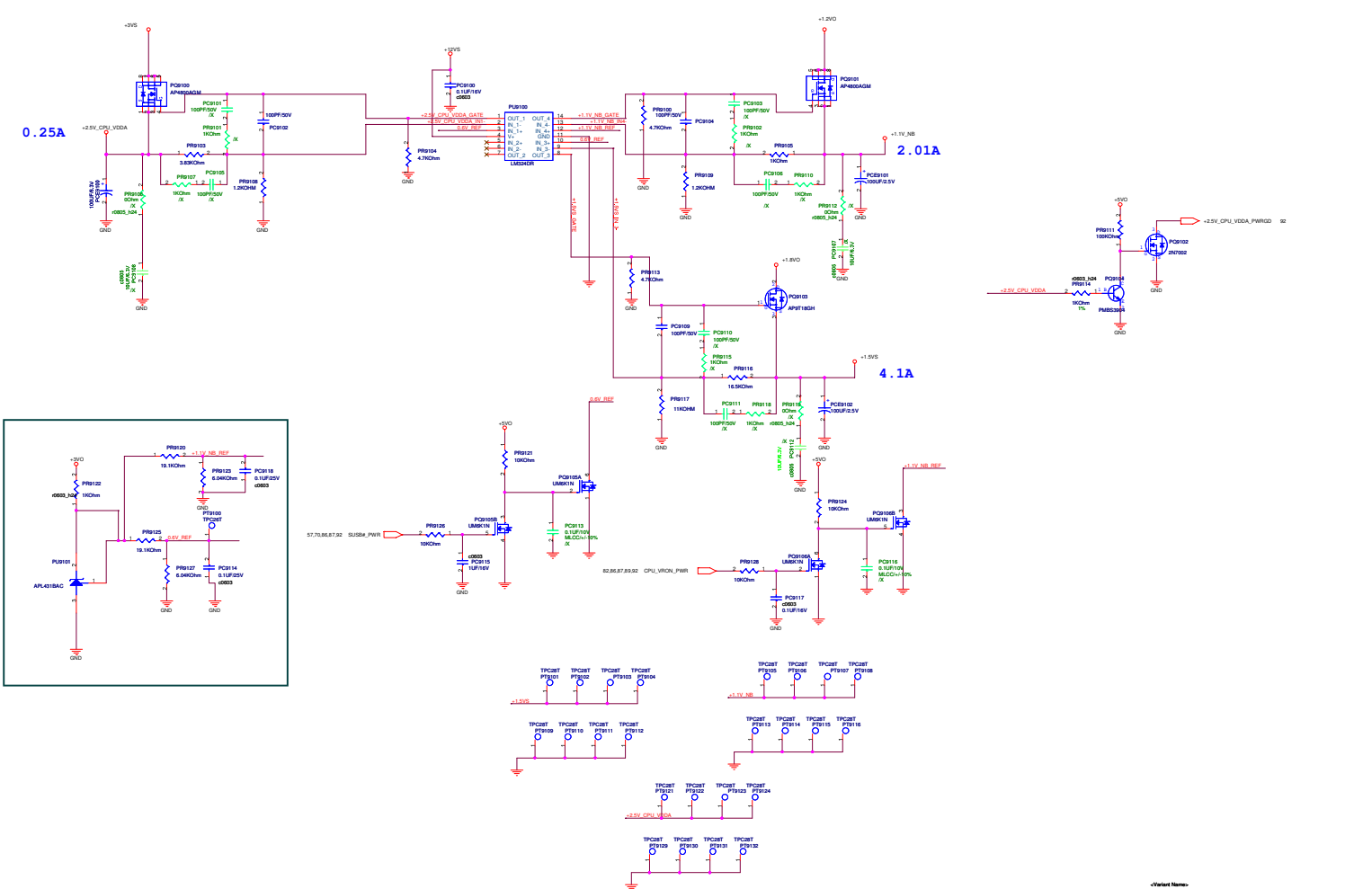
<Variant Name>

ASUS		Title : +VCC_NB	
ASUSTEK COMPUTER INC	Project Name:	Engineer:	N/A
Size:	Project Name:		
Custom:	FSTR		
Date: Wednesday, March 12, 2008	Sheet:	89	of 92

<< MaryL_Liu >>



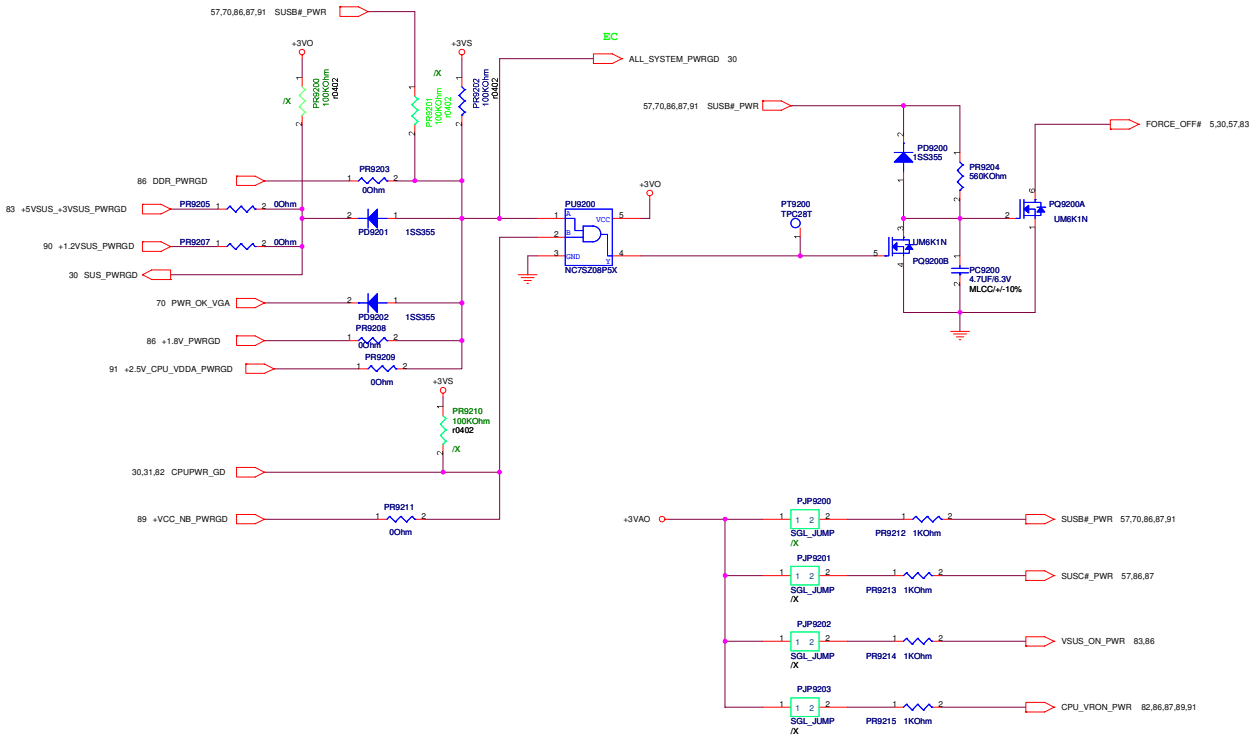
<< MaryL_Liu >>



ASUS		Title : OP+MGS
Asustek Computer Inc		Engineer : N/A
Size : []	Project Name :	Part :
Alt :	PCTR	1.0
Date : Wednesday, March 12, 2008		Sheet : 11 of 31

<< MaryL_Liu >>

POWER GOOD DETECTOR



<Variant Name>

		Title : POWER_GOOD_DETECTOR	
ASUSTEK COMPUTER INC		Engineer: N/A	
Site: Custom	Project Name: FSTR		Rev: 1.0
Date: Wednesday, March 12, 2008		Sheet: 92 of 92	

<< MaryL_Liu >>