9000A-80286
Quick Reference Card

FLUKE

Status Lines

BIT	STATUS LINE	SPECIAL CHARACTERISTICS
0	READY	e, f
1	HOLD	e, f
2	NMI	i
3	INTR	i
4	RESET	f
5	PEREQ	f
6	BUSY	f
7	ERROR	f
8	CAP FAIL	p, f, m*
9	INT VECT	p
10	PWR FAIL 30	p, m
11	PWR FAIL 62	p, m
12	GND FAIL 35	p, m
13	GND FAIL 9	p, m
14	(not used)	
15	(not used)	

Special Characteristics Definitions

- e - an enableable line
- f - a forcing line
- i - an interrupt
- m - miscellaneous line
- p - a pseudo-status line. Does not reflect actual physical line condition of a line, but indicates a condition of the Pod that is important to the user.

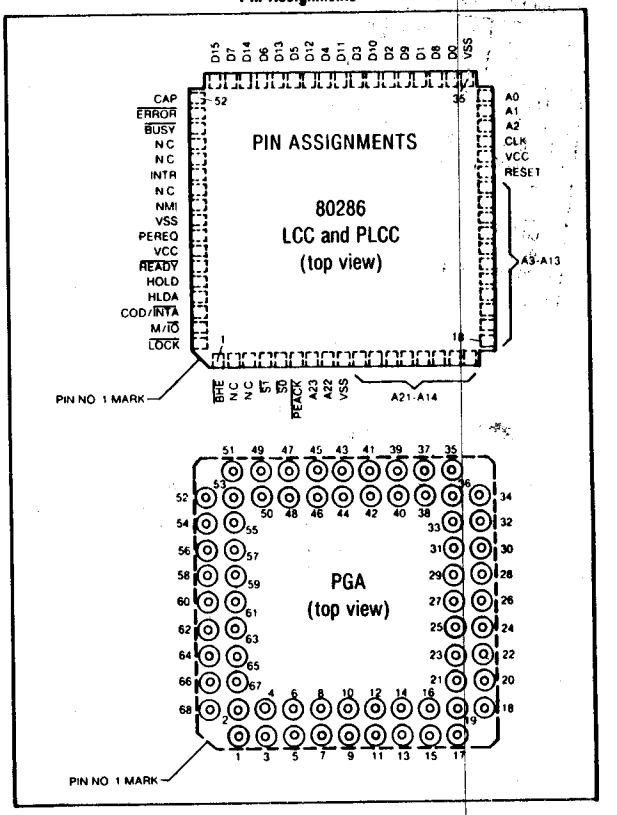
*CAP FAIL is a forcing line for the 9000-Series Mainframe and a miscellaneous line for the 9100-Series Mainframe.

Control Lines

BIT	CONTROL LINE	SPECIAL CHARACTERISTICS
0	LOCK	w
1	HLDA	w
2	PEACK	w
3	BHE	
4	S1	
5	S0	
6	M/IO	
7	COD/INTA	
8	(not used)	
9	(not used)	
10	(not used)	
11	(not used)	
12	(not used)	
13	(not used)	
14	(not used)	
15	(not used)	

w - writable control line

Pin Assignments



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Quick RAM Test

ACTION	MEANING
WRITE @ 2SXX XXXX = 0	SXX XXXX = starting address
WRITE @ 2SYY YYYY = ZZZW	S = address space 0 = memory word 1 = I/O word 2 = memory byte 3 = I/O byte YY YYYY = ending address ZZZ = increment 1 = byte addresses 0, 2 = word addresses W = function type 1 = RAM test 2 = Pattern Verify
READ @ ENTER	Returns status as follows:

CODE	MEANING
0000	No test requested
00A0	Aborted, new command entered
00A1	Aborted, illegal data in cmd
00A2	Aborted, illegal adr in cmd
00A3	Aborted, Pod timeout occurred
00B0	Busy, performing rd/wr check
00B1	Busy, performing adr dcd check
00B2	Busy, performing pattern verify
00C0	Complete, no errors
00F0	Failed, read/write error
00F1	Failed, address decoding error
00F2	Failed, pattern verify error

READ @ F000 2000	Low word of starting address
READ @ F000 2002	High word of starting address
READ @ F000 2004	Low word of ending address
READ @ F000 2006	High word of ending address
READ @ F000 2008	Low word of error address
READ @ F000 200A	High word of error address
READ @ F000 200C	Data expected at error address
READ @ F000 200E	Actual data returned from error adr
READ @ F000 2010	Returns most recent code returned
READ @ F000 2012	Hex mask of error bits
READ @ F000 2014	Returns increment and function type

Quick ROM Test

ACTION	MEANING
WRITE @ 3SXX XXXX = 0	SXX XXXX = starting address
WRITE @ 3SYY YYYY = ZZZ1	S = address space 0 = memory word 1 = I/O word 2 = memory byte 3 = I/O byte 4 = instruction word YY YYYY = ending address ZZZ = increment 1 = byte addresses 0, 2 = word addresses
READ @ ENTER	Returns status as follows:

CODE	MEANING
0000	No test requested
00A0	Aborted, new command entered
00A1	Aborted, illegal data in cmd
00A2	Aborted, illegal adr in cmd
00A3	Aborted, Pod timeout occurred
00B0	Busy, test in progress
00C0	Complete, no errors
00C1	Complete, inactive bits detected

READ @ F000 3000	Low word of starting address
READ @ F000 3002	High word of starting address
READ @ F000 3004	Low word of ending address
READ @ F000 3006	High word of ending address
READ @ F000 300C	Signature
READ @ F000 300E	Hex mask of bits detected as inactive
READ @ F000 3010	Returns most recent code
READ @ F000 3014	Returns address increment and function

Quick Fill and Verify Function

ACTION	MEANING
WRITE @ 4SXX XXXX = 0	SXX XXXX = starting address.
WRITE @ 4SYY YYYY = ZZZW	S = address space 0 = memory word 1 = I/O word 2 = memory byte 3 = I/O byte YY YYYY = ending address ZZZ = increment 1 = byte addresses 0, 2 = word addresses W = function type 1 = Fill 2 = Verify 3 = Fill then Verify
READ @ ENTER	Returns status as follows:

CODE	MEANING
0000	No test requested
00A0	Aborted, new command entered
00A1	Aborted, illegal data in cmd
00A2	Aborted, illegal adr in cmd
00A3	Aborted, Pod timeout occurred
00B0	Busy, performing fill
00B1	Busy, performing verify
00C0	Complete, no errors
00F0	Error, data does not match

READ @ F000 4000	Low word of starting address
READ @ F000 4002	High word of starting address
READ @ F000 4004	Low word of ending address
READ @ F000 4006	High word of ending address
READ @ F000 4008	Low word of error address
READ @ F000 400A	High word of error address
READ @ F000 400C	Data written by fill
READ @ F000 400E	Actual data returned from error address
READ @ F000 4010	Returns most recent code
READ @ F000 4012	Hex mask of error bits
READ @ F000 4014	Returns increment and function type

Quick Ramp Function

ACTION	MEANING
WRITE @ 5SXX XXXX = ZZZZ	S = address space 0 = memory word 1 = I/O word XX XXXX = Ramp address ZZZZ = any data
READ @ ENTER	Returns status as follows:

CODE	MEANING
0000	No test requested
00A0	Aborted, new command entered
00A2	Aborted, illegal adr in cmd
00A3	Aborted, Pod timeout occurred
00B0	Busy, performing ramp
00C0	Complete

READ @ F000 5000	Low word of address
READ @ F000 5002	High word of address
READ @ F000 5010	Returns most recent code

Interrupt Handling

ADDRESS	DESCRIPTION
F000 0080	Enable Interrupt Acknowledge Cycle
F000 0082	Read Interrupt Type and Re-enable
F000 0084	Read Interrupt Type and do not Re-enable
F000 0086	Force Interrupt Acknowledge Bus Cycle
F000 0088	Force Interrupt Acknowledge Bus Cycle and Loop
F000 008C	Read Cascade Address (lower word)
F000 008E	Cascade Address (most significant byte)

Address Mapping

NAME	WORD ADDRESSES	BYTE ADDRESSES
MEMORY	0 - FF FFFE	200 0000 - 2FF FFFF
I/O	100 0000 - 100 FFFE	300 0000 - 300 FFFF
INSTRUCTION	400 0000 - 4FF FFFE	—

Pod Function Addresses

ADDRESS	DESCRIPTION	
Pod Control Addresses		
F000 0000	Self-Test Result Code	(Read/Write)
F000 0002	Standby Address	(Read/Write)
F000 0006	Standby Read Enable	(Read/Write)
F000 0012	Software Revision Level	(Read Only)
Error Reporting Addresses		
F000 0040	Last Error Summary	(Read Only)
F000 0042	Last Control Errors	(Read Only)
F000 0044	Last Active Forcing Line and Active Interrupts	(Read Only)
F000 0048	Last High Address Drivability Errors	(Read Only)
F000 004A	Last Low Address Drivability Errors	(Read Only)
F000 004C	Last Data Drivability Errors	(Read Only)
F000 0052	Last Status	(Read Only)
Error Masks		
F000 0060	Error Summary Mask	(Read/Write)
F000 0062	Control Drivability Error Mask	(Read/Write)
F000 0064	Forcing Line and Interrupt Error Mask	(Read/Write)
F000 0068	High Address Drivability Error Mask	(Read/Write)
F000 006A	Low Address Drivability Error Mask	(Read/Write)
F000 006C	Data Drivability Error Mask	(Read/Write)
F000 006E	Miscellaneous Error Mask	(Read/Write)
Interrupt Vector and Configuration Addresses		
F000 0080	Enable Interrupt Acknowledge Cycle	(Read/Write)
F000 0082	Read Interrupt Vector and Re-enable	(Read Only)
F000 0084	Read Interrupt Vector and do not Re-enable	(Read Only)
F000 0086	Force Interrupt Acknowledge Bus Cycle	(Read Only)
F000 0088	Quick Loop on Force INTA	(Read Only)
F000 008C	Read Cascade Address (low word)	(Read Only)
F000 008E	Cascade Address (high byte)	(Read Only)
Overlay RAM Addresses		
F000 00A0	Enable Overlay RAM	(Read/Write)
F000 00A2	Overlay RAM Base Address	(Read/Write)
F000 00A4	Enable READY from the UUT to Overlay RAM	(Read/Write)
Breakpoint Addresses		
F000 00B0	Enable Breakpoint	(Read/Write)
F000 00B2	Breakpoint Address (low word)	(Read/Write)
F000 00B4	Breakpoint Address (high byte)	(Read/Write)
F000 00B6	Break confirmation	(Read Only)
Segment Register Contents for RUN UUT		
F000 0130	CS Register Contents	(Read/Write)
F000 0132	DS Register Contents	(Read/Write)
F000 0134	SS Register Contents	(Read/Write)
F000 0136	ES Register Contents	(Read/Write)

9000-Series RUN UUT Control Addresses

FUNCTION	ADDRESS	DESCRIPTION
RUN UUT Type 1 (Using the Default Execution Address)	FF FFF0	This is the RUN UUT default address that the Pod supplies if the operator does not specify an execution address. RUN UUT execution at FF FFF0 sets all segment registers to their reset values (0000 for ES, SS, and DS, and F000 for CS) and sets the offset (IP register) to FFF0.
RUN UUT Type 2 (Specifying the Execution Address — bottom 1M bytes)	Y XXXX	The RUN UUT execution address may be specified by entering the address from the Mainframe setup function as Y XXXX, where the CS register equals Y000, and the offset (IP register) is XXXX. This allows you to begin operation anywhere in the bottom 1M byte of UUT memory.
RUN UUT Type 3 (Specifying the Execution Address — top 64k bytes)	FF XXXX	The RUN UUT execution address may be specified by entering the address from the Mainframe setup function as FF XXXX, where the upper four address bits are set to F, the CS register equals F000, and the offset (IP register) is XXXX. This allows you to begin operation anywhere in the upper 64k bytes of UUT memory.
RUN UUT Type 4 (Specifying the Special Function Address)	F000 XXXX	Explicitly load the CS register using special address F000 0130 and then RUN UUT @ F000 XXXX, where the resulting address is the CS register shifted left 4 bits and the offset (IP register) is XXXX.

NOTE

The Segment Registers may be defined prior to a Type 4 RUN UUT by writing the data to the following Pod Function addresses:

F000 0130 = CS register
F000 0132 = DS register
F000 0134 = SS register
F000 0136 = ES register

After the desired values are written to the above addresses, execute RUN UUT at the address F000 XXXX, where XXXX is the desired offset address. The specified contents are loaded into the segment registers. The RUN UUT execution addresses are formed using the CS register: CS register contents are shifted left four bits, then added to the offset for the execution address.

Address Mapping

NAME	WORD ADDRESSES	BYTE ADDRESSES
MEMORY	0 - FF FFFE	200 0000 - 2FF FFFF
I/O	100 0000 - 100 FFFE	300 0000 - 300 FFFF
INSTRUCTION	400 0000 - 4FF FFFE	—