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Full-Wave Signal Rectifier Uses Just One Transistor

My favorite Ideas for Design are the timeless ideas that start with some well-known idiosyncrasy of a common component and develop it into a clever use in an application. The trick in this IFD is that the transistor is biased so that at the crossover point of the input signal, collector and emitter essentially switch roles, and the original common-emitter circuit effectively becomes an emitter-follower. The result is full-wave rectification at the output. For skeptics, Albean provides some notes on Spice analysis and empirical results. ***Don Tuite***

The simple circuit shown accomplish-es full-wave signal rectification with only one transistor *(Fig. 1)*. This is done by exploiting the "gain reversal" phenomenon exhibited by a saturated bipolar transistor. This circuit will find applications as a signal-level detector (AGC detector), rectifier, or signal-presence detector.

To understand the operation of this circuit, first assume that the transistor is biased in saturation. The bias conditions are established by R_{B1} and R_{B2}. R_L and R_E are chosen for the desired gain/dc offset at the output. This circuit configuration is simply a saturated common-emitter (CE) amplifier.

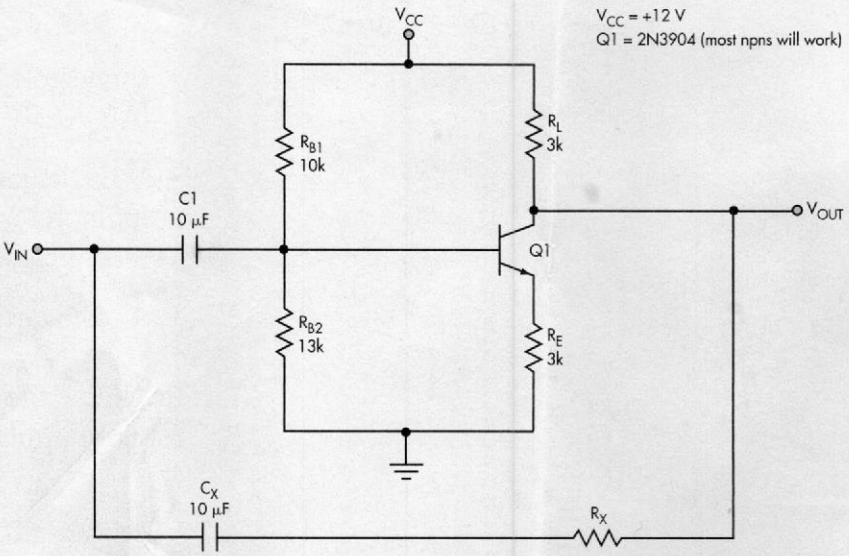
For the following analysis, the component values given are used. Consider a sinusoidal input signal. For a negative-going V_{IN}, V_{OUT} can swing positive. The gain experienced by the signal is about: $-((R_L \| R_X)/R_E) + (R_L/(R_L + R_X))$ (normal operation of a CE stage). However, for a positive-going input signal, the collector-base junction becomes forward-biased (the transistor is saturated) and the transistor operates as an emitter-follower.

At this point, the collector is acting as the emitter usually does under forward bias. The gain expression then becomes: $1 + (R_L/(R_L + R_X))$. Full-wave rectifier action requires the gain for positive and negative signals be equal in magnitude, but opposite in sign. For a gain of 1, set R_X to infinity; this reduces the above equations to: $(R_L/R_E) = 1$.

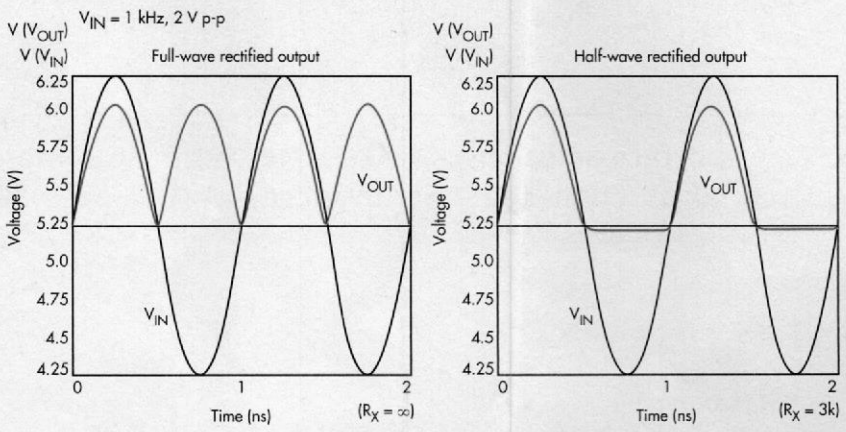
An npn transistor is used to get a positive-rectified output. Using a pnp transistor (and reversing connections as appropriate) will produce a negative-rectified output. To choose element values, start with the following (for C1, C_X coupling capacitors, use as large a value as necessary for the frequency range of interest):

1. Ensure saturation: $V_{CC} - I_C(R_L + R_E) < V_{cesat}$
2. Choose I_C
3. Choose R_L, R_E for desired gain
4. Choose the R_{B1}, R_{B2} divider consistent with above

Design for a gain of 1 (R_X = infinity) and I_C = 2 mA yields: R_{B1} = 10k; R_{B2} = 13k; $R_L = R_E$ = 3k. Gains between 1x and



1. By taking advantage of a saturated bipolar transistor's "gain reversal" phenomenon, this circuit can perform full-wave signal rectification using only one transistor.



2. A full-wave rectifier is realized by setting $R_X = \infty$ (a). Half-wave rectification is predicted at R_X = 3k.

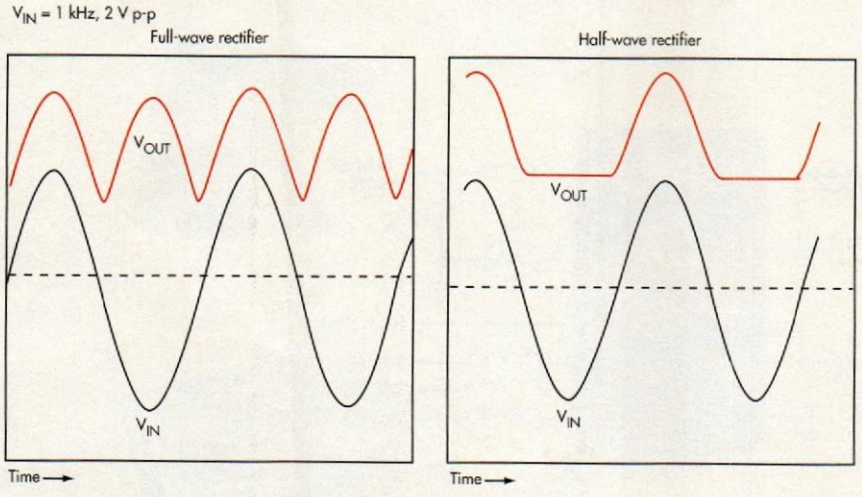
2x can be achieved, but R_X must be included as indicated in the more complex design equations.

Start with these equations. Iterate with Spice to get optimal values *(Fig. 2)*. This circuit is difficult to simulate accurately due to its inherent nonlinear operation. Thus, performing transient analyses in Spice will produce the best results *(Fig. 3)*.

It's important to have a good transistor model to accurately predict the circuit's behavior in saturation. Also, including BR (reverse beta) in the Spice models is important because the circuit's operation relies on reverse operation of the transistor. Check this circuit at higher operating frequencies using Spice transient analyses as well.

A couple of notes to consider:

1. Gain is limited to a minimum of 1. Gain scaling and dc offset can be accomplished with a subsequent stage.
2. Use R_X as a "symmetry" trim. This will give the rectifier a gain closer to +1 for a positive input. A half-wave rectifier can be made by choosing values that result in $(R_L \,||\, R_X)/(R_E) = (R_L)/(R_L + R_X)$. This equality will exactly cancel the positive and negative gains for negative-going half cycles, resulting in half-wave rectification. (The transistor will act as an emitter follower only for positive inputs.) For the example, R_X = 3k will produce a half-wave rectifier.



3. Measured waveforms verify the full-wave (a) and half-wave (b) performance predicted by the Spice analysis.

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