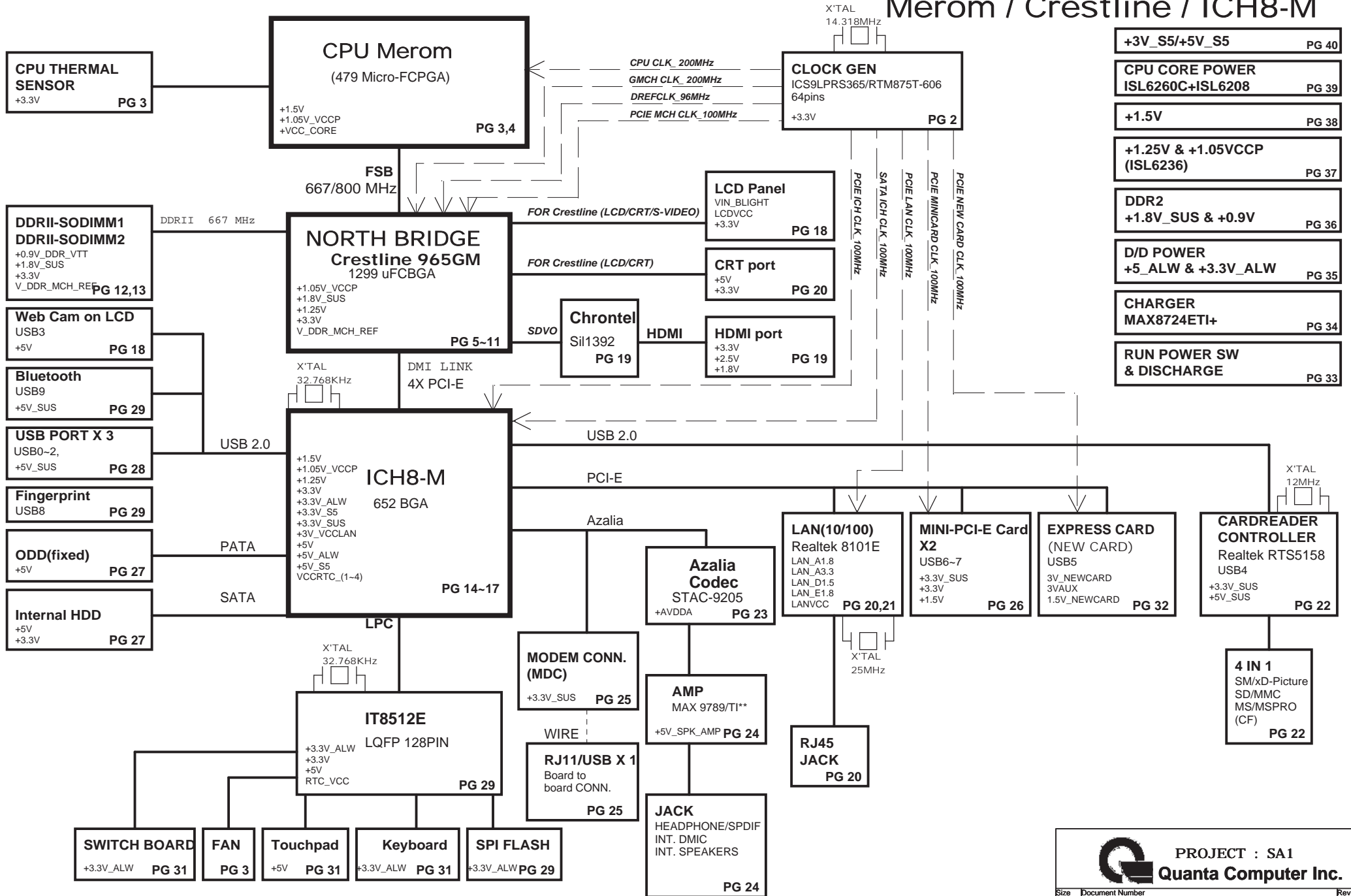


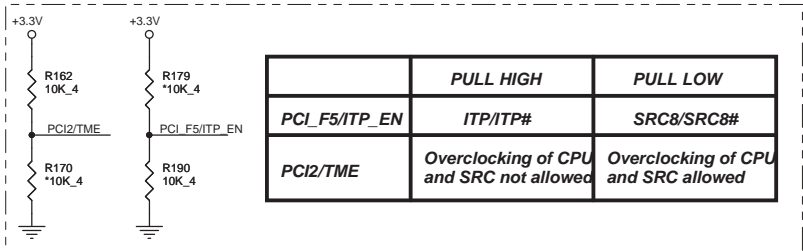
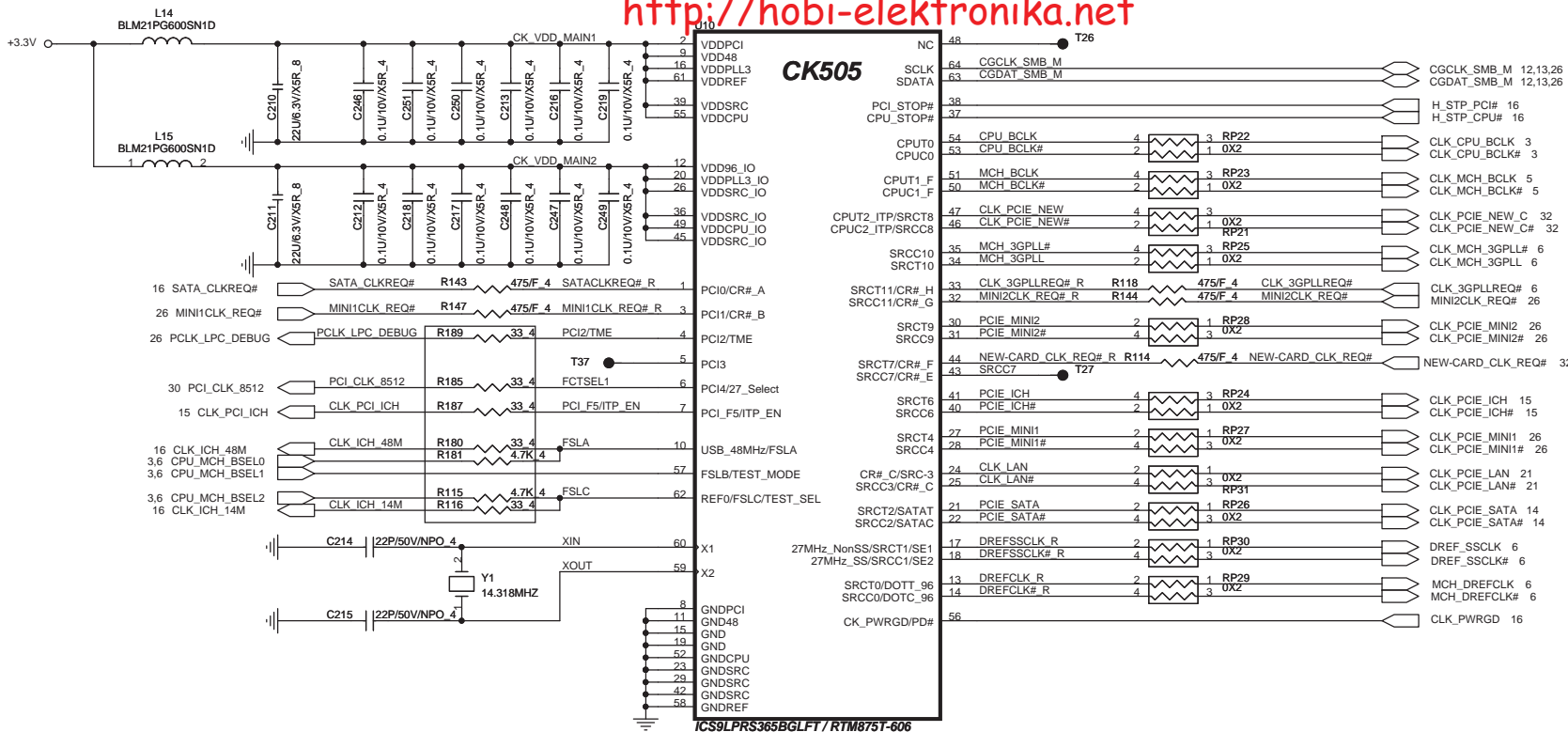
SA1 BLOCK DIAGRAM

Merom / Crestline / ICH8-M



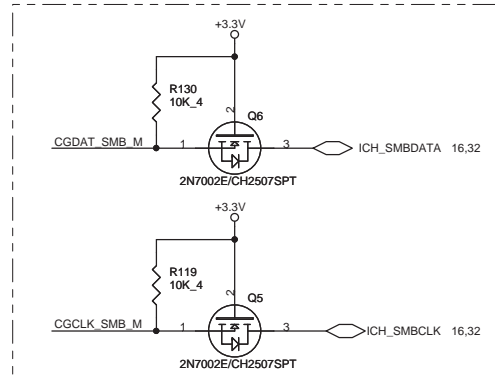
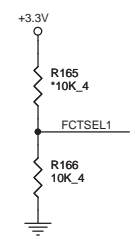
PROJECT : SA1
Quanta Computer Inc.

Size Custom	Document Number	Rev 4A
BLOCK DIAGRAM		
Date: Friday, July 20, 2007	Sheet 1	of 43



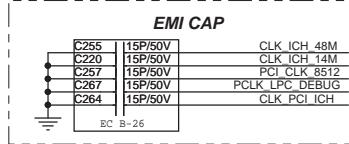
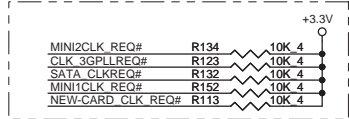
GCLK_SEL = FCTSEL1

FCTSEL1 (PIN6)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96	DOT96#	SRC-1/LCDT_100	SRC-1#/LCDT_100
1 = External VGA	SRC-0	SRC-0#	27Mout-NSS	27Mout-SS



CPU Clock select

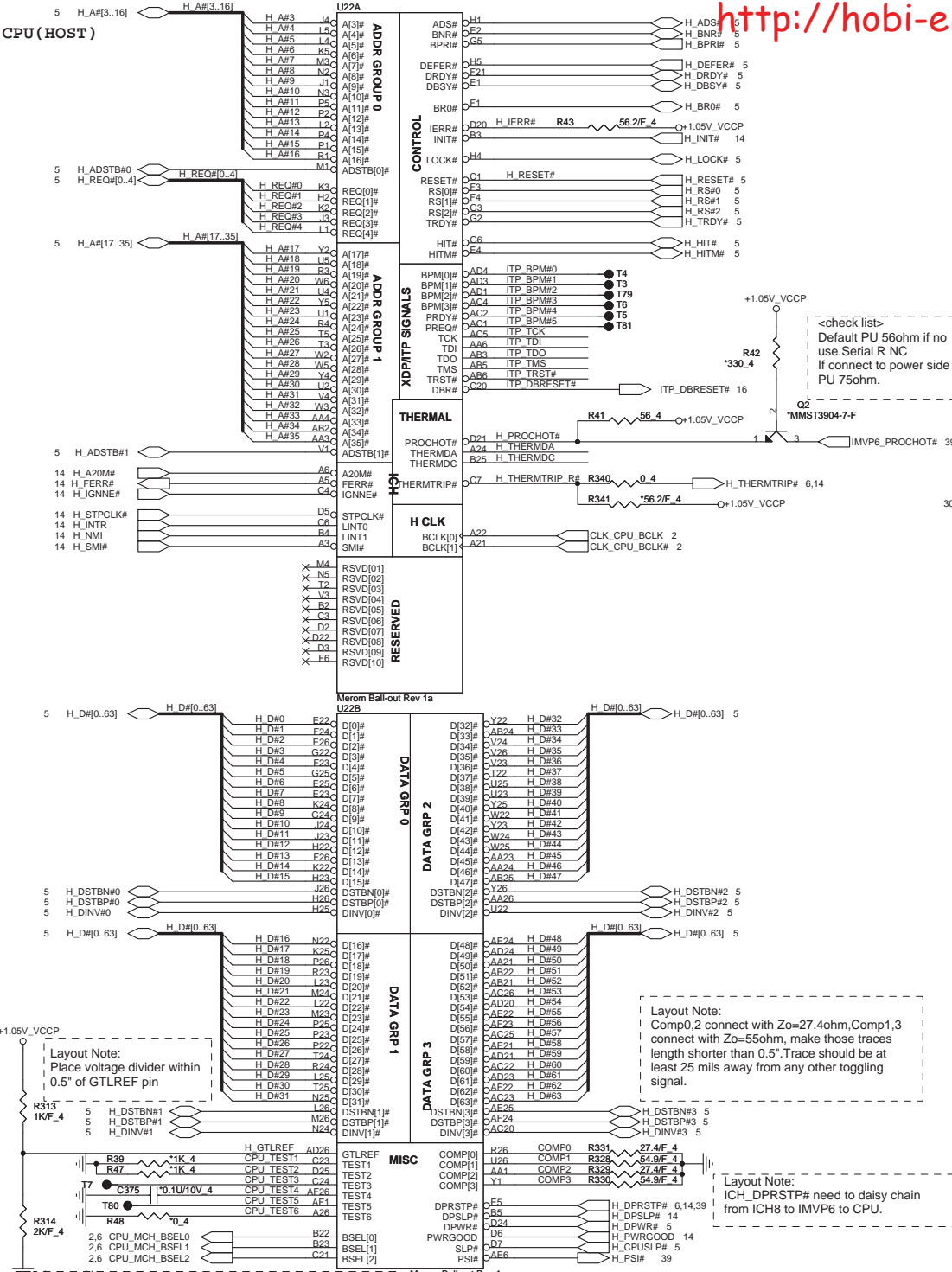
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100.00	100	33
0	0	1	133.33	100	33
0	1	1	166.66	100	33
0	1	0	200.00	100	33
0	0	0	266.66	100	33
1	0	0	333.33	100	33
1	1	0	400.00	100	33
1	1	1	200.00	100	33

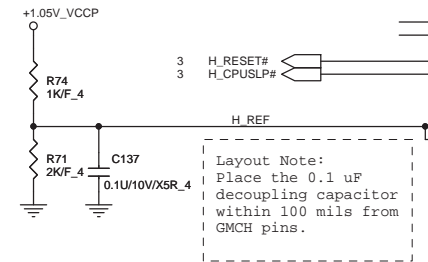
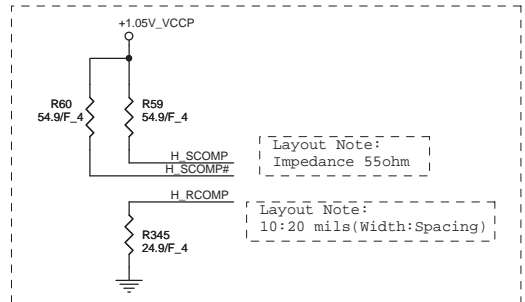
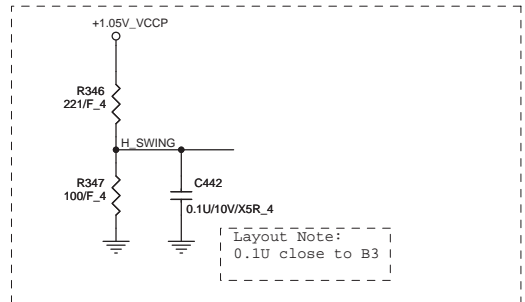
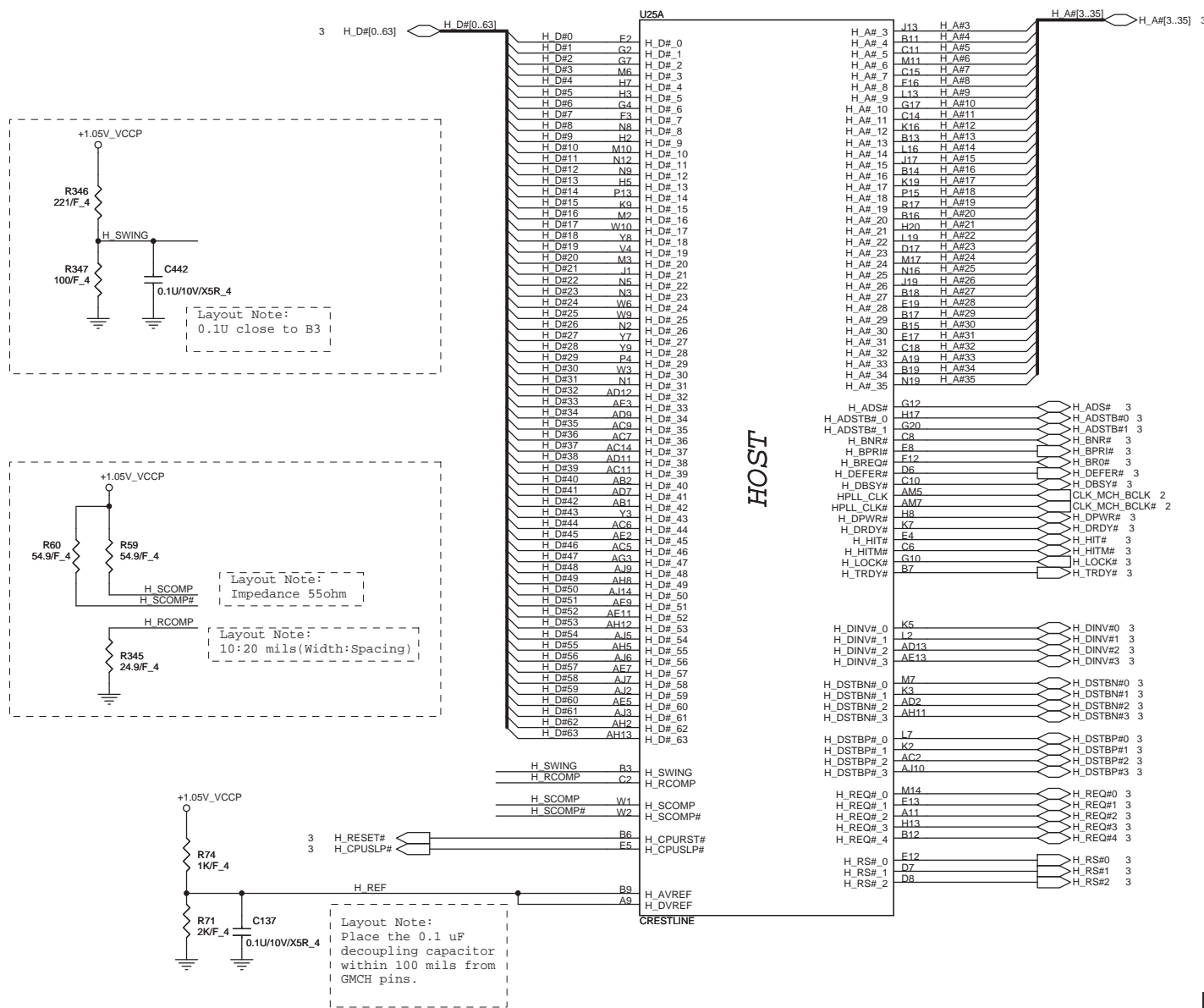


PROJECT : SA1
Quanta Computer Inc.

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 Date: Thursday, July 26, 2007 Sheet 2 of 43

CPU Thermal monitor



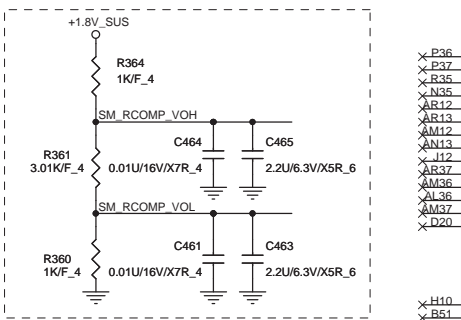


PROJECT : SA1
Quanta Computer Inc.

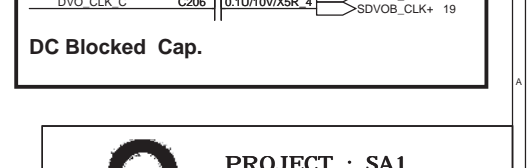
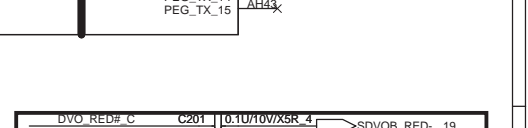
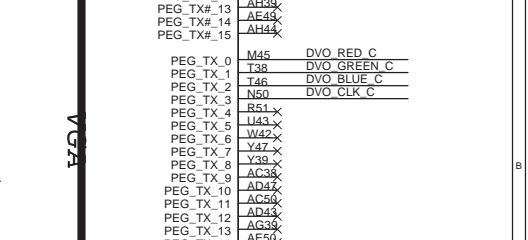
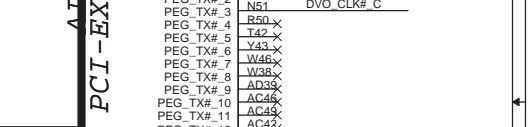
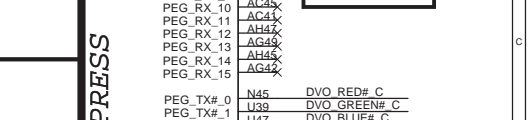
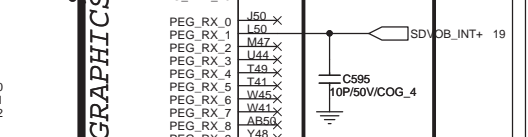
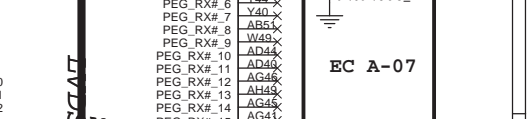
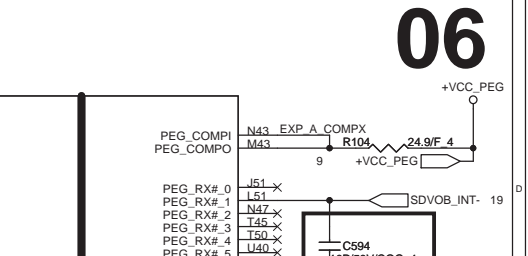
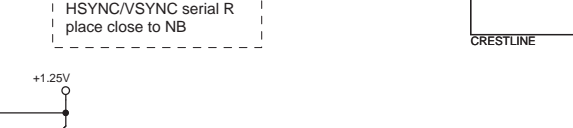
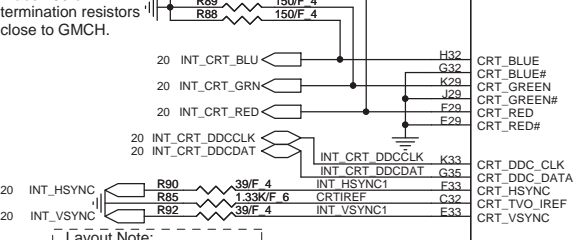
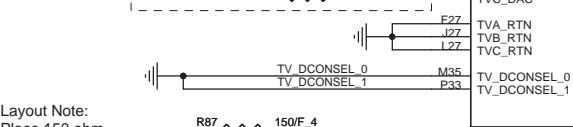
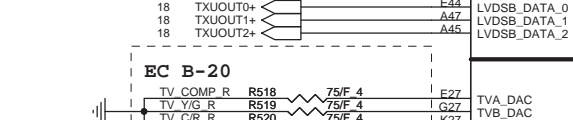
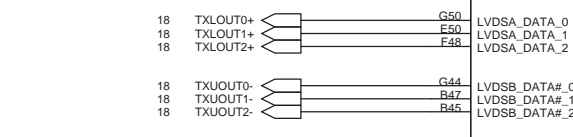
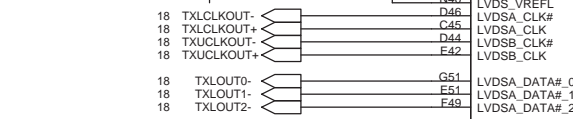
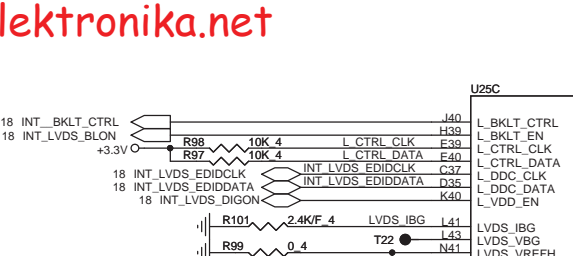
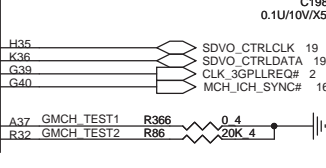
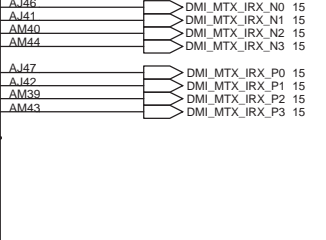
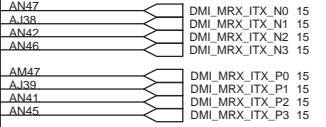
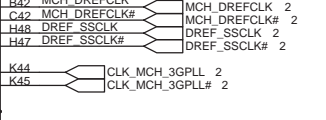
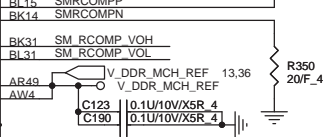
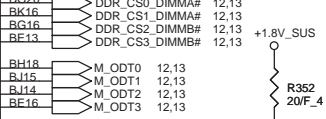
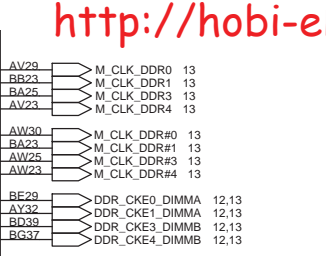
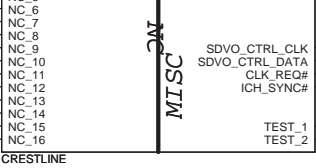
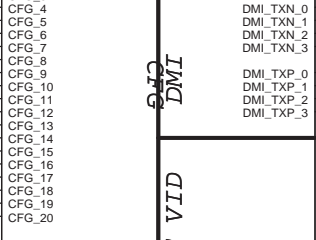
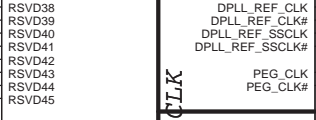
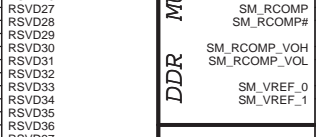
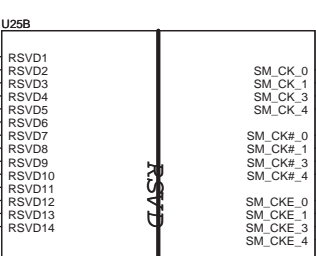
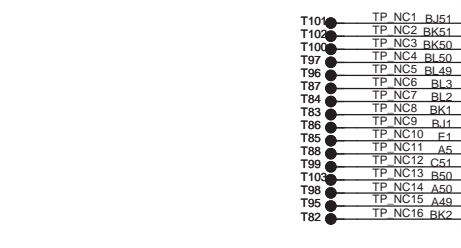
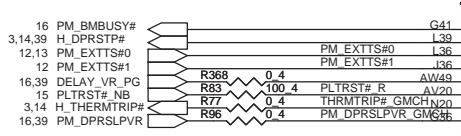
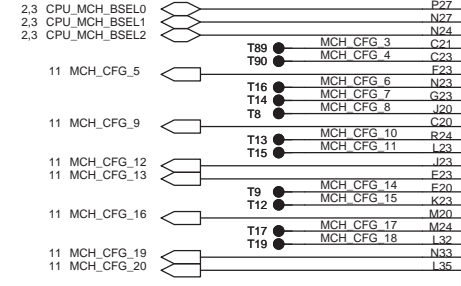
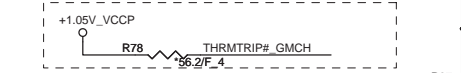
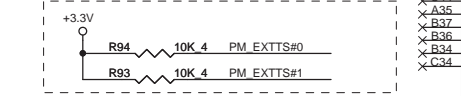
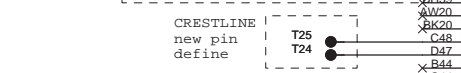
Size: Document Number
 Custom: **GMCH HOST(1 of 6)**

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Rev 1A



Santa Rosa Platform MOW Ww15
 For 4GB DRAM support,
 change Pin-BJ29 to DDR_A_Ma14,
 change Pin-BE24 to DDR_B_Ma14.



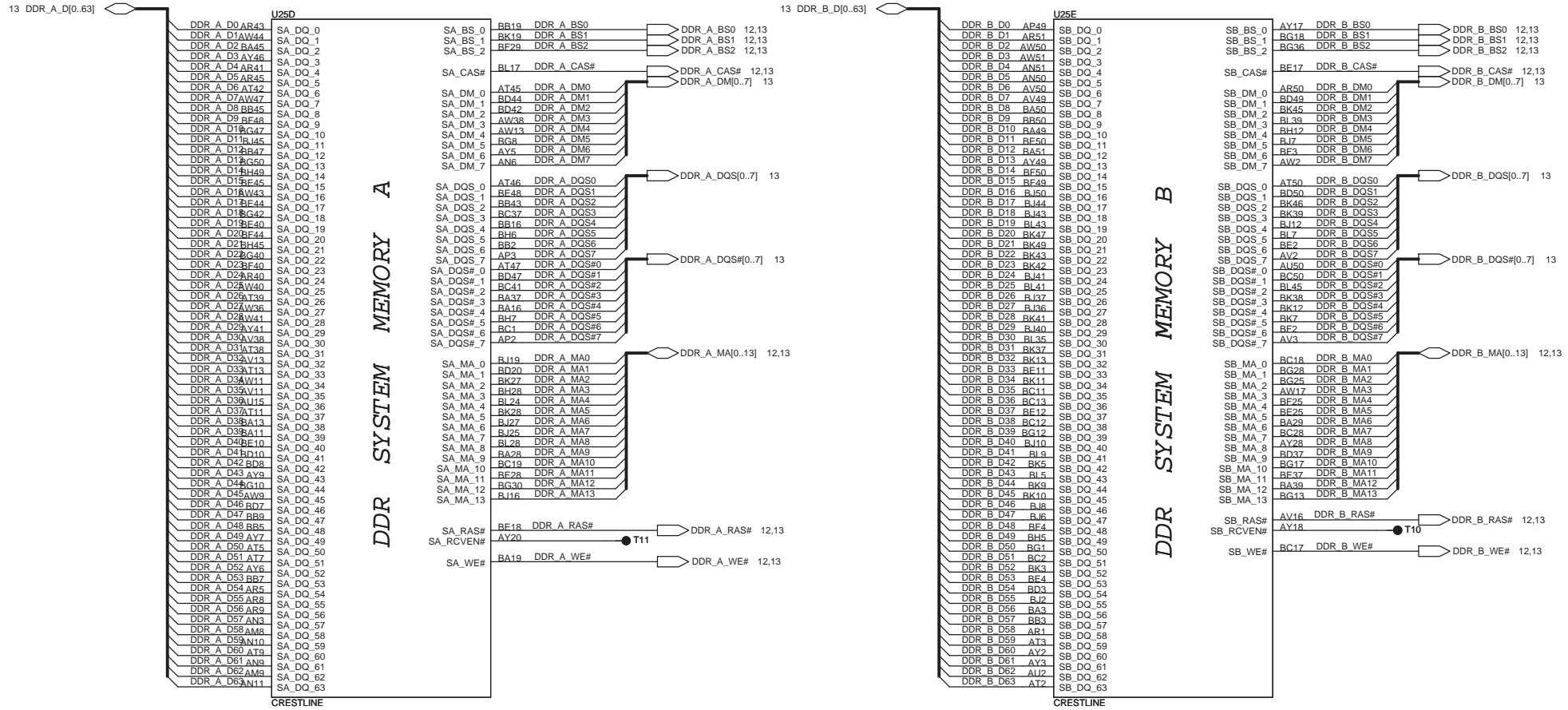
PROJECT : SA1
 Quanta Computer Inc.
 Size Document Number
 Custom GMCH DMI/VIDEO(2 of 6) Rev 1A
 Date: Friday, July 20, 2007 Sheet 6 of 43

PCI-EXPRESS GRAPHICS

Layout Note:
 Place 150 ohm
 termination resistors
 close to GMCH.

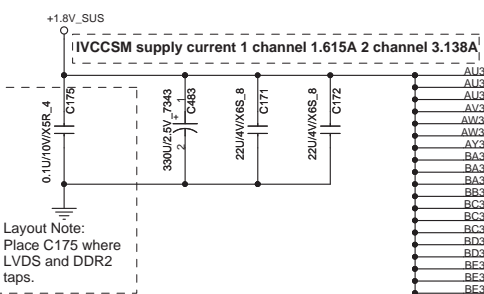
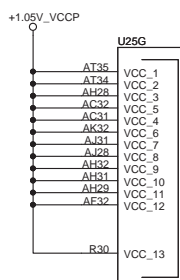
Layout Note:
 HSYNC/VSYNC serial R
 place close to NB

DC Blocked Cap.

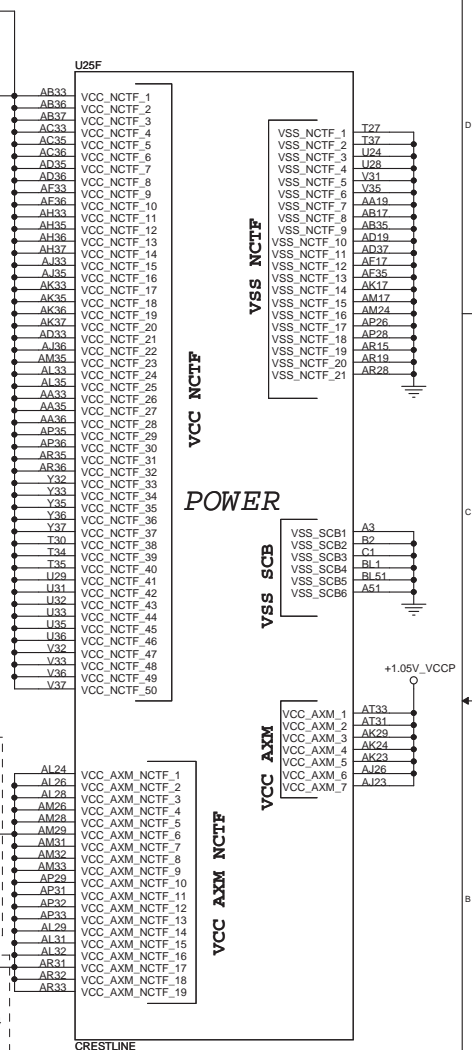
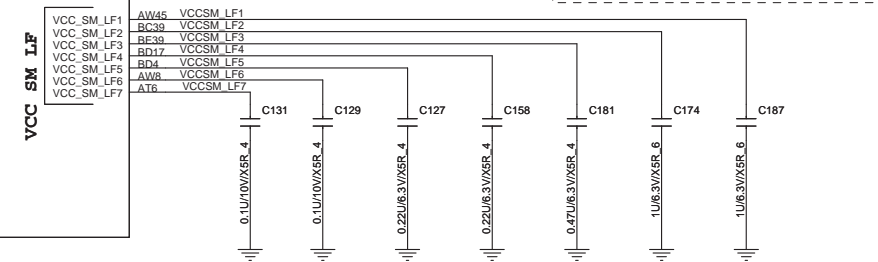
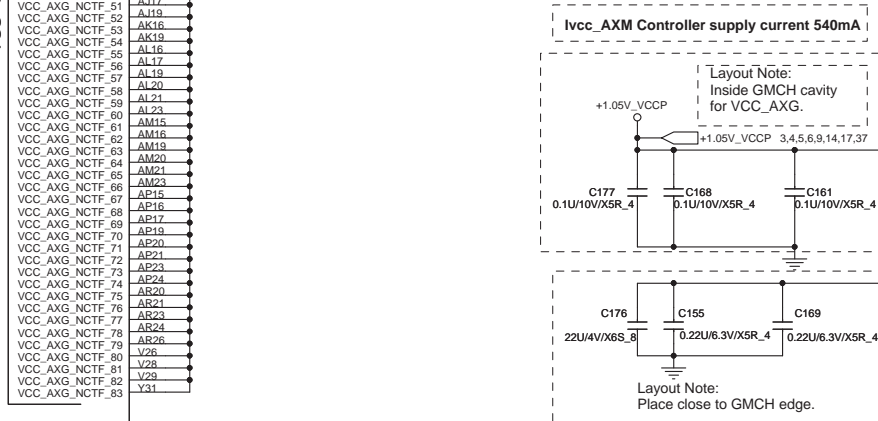
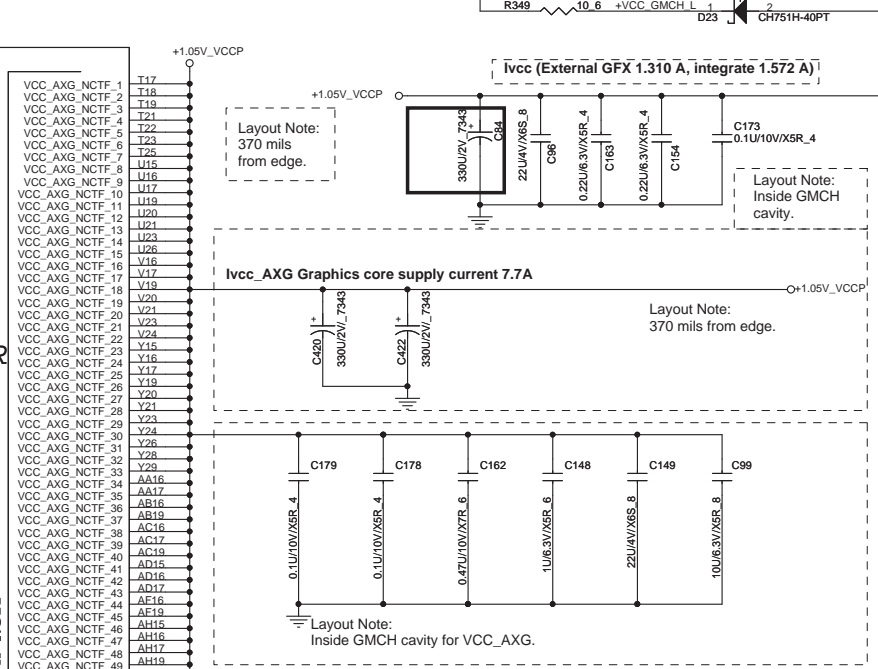
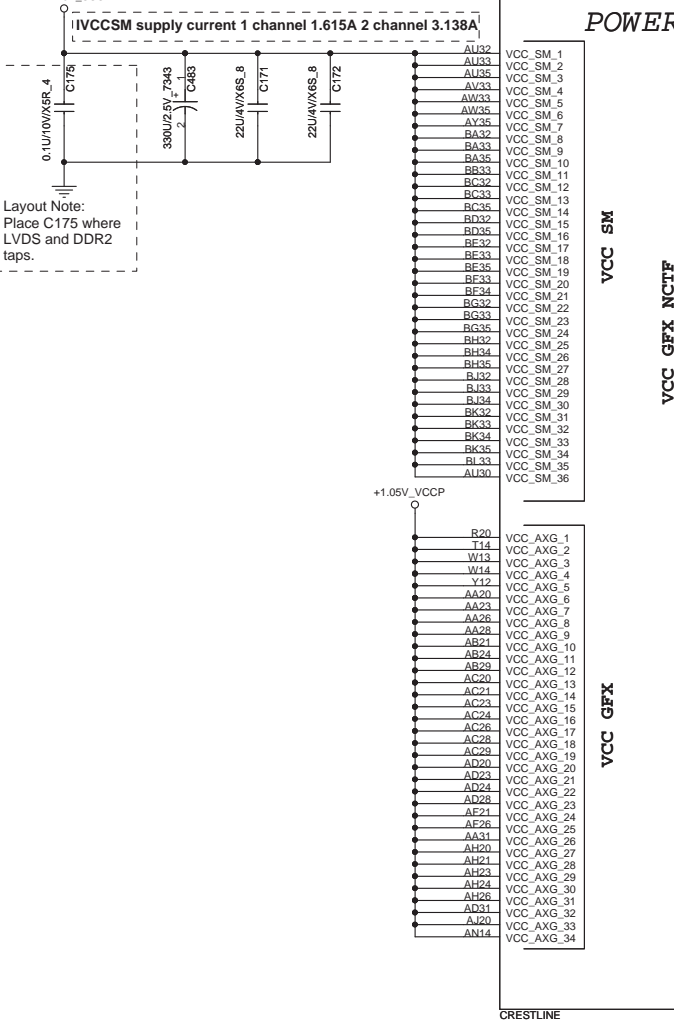


PROJECT : SA1
 Quanta Computer Inc.
 Size Document Number
 Custom GMCH DDR/Strap(3 of 6) Rev
 Date: Friday, July 20, 2007 Sheet 7 of 43

GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	12.313	

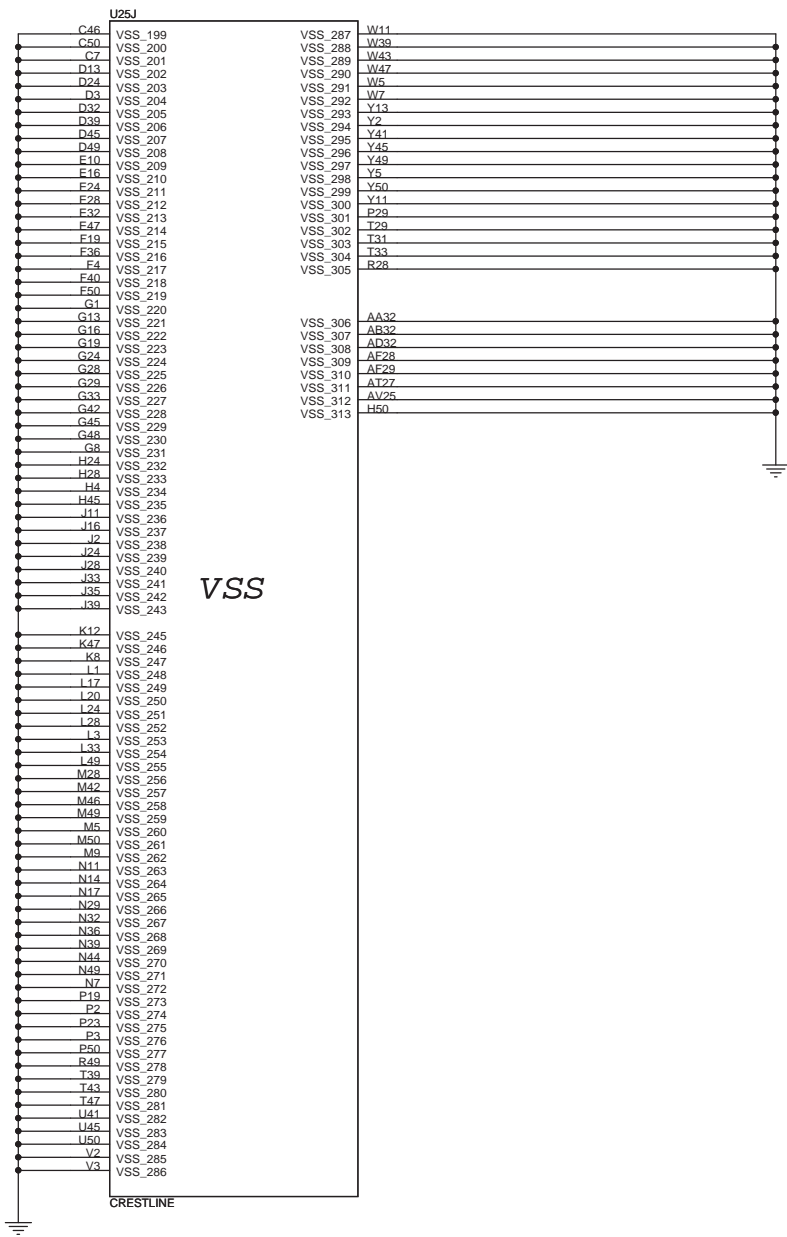
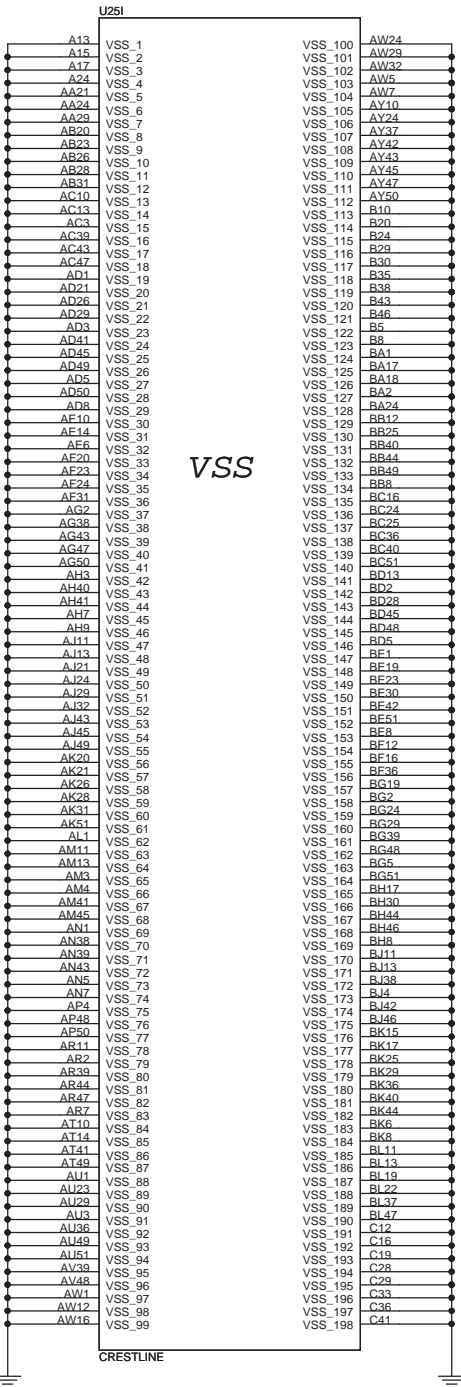


Layout Note:
Place C175 where LVDS and DDR2 taps.



CRESTLINE

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PROJECT : SA1
Quanta Computer Inc.

Size: Document Number
 Custom: **GMCH Power-3(6 of 6)** Rev 1A

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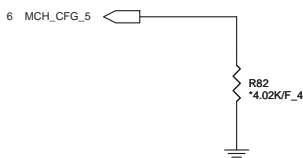
Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal.
 CFG[17:3] Have internal Pull-up
 CFG[18:19] Have internal Pull-down
 Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	IntelR Management Engine Crypto strap	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. 1= Intel Management Engine Crypto TLS cipher suite with confidentiality (default).
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

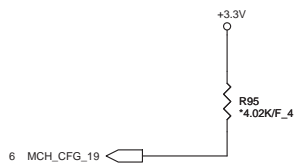
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)
-----------	---------------------------------------



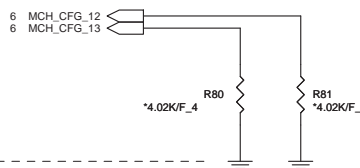
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
------------	--



XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
-----------	--

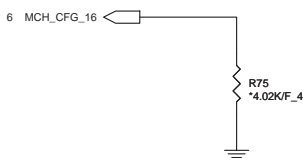


SDVO Present

Strap define at External DVI control page

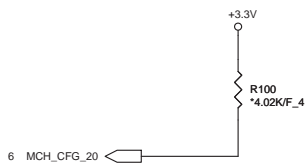
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
------------	---



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port
------------	--



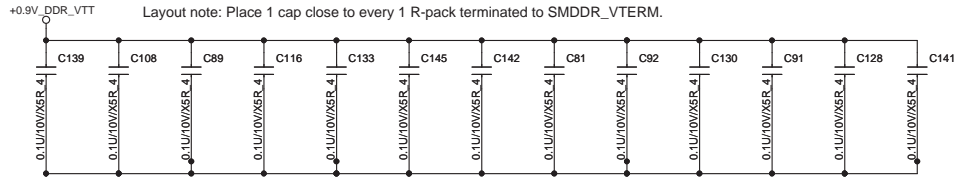
Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minimize stub.

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Quanta Computer Inc.

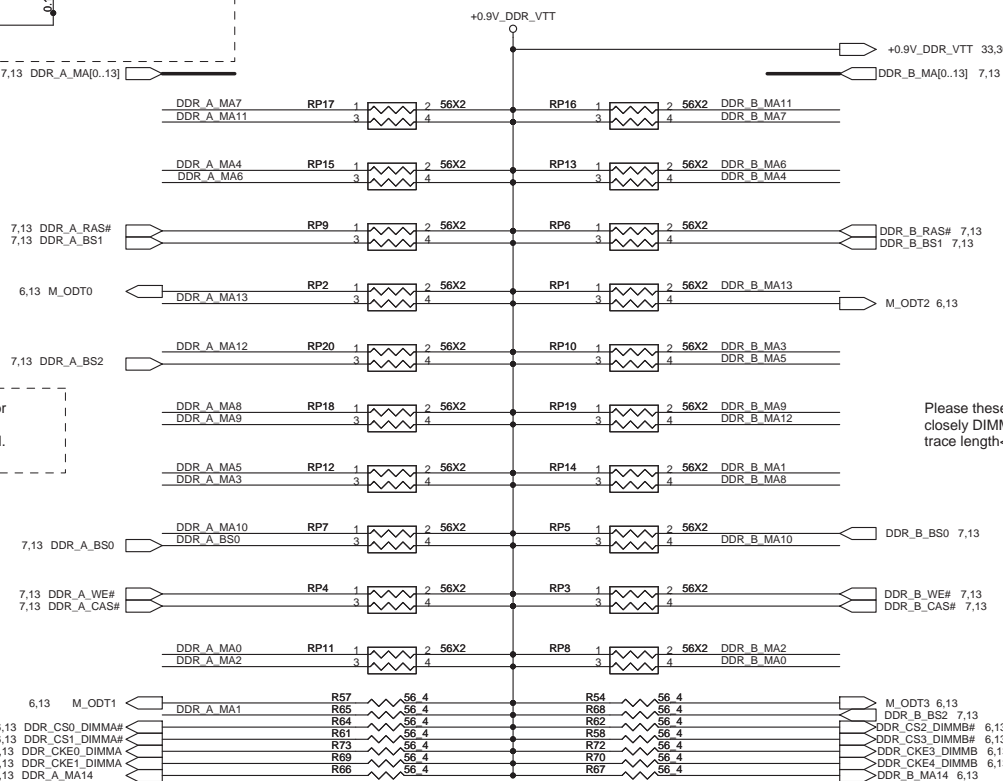
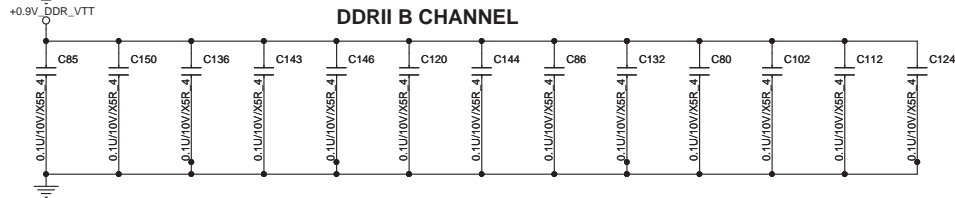
Size	Document Number	Rev
Custom	GMCH Strap Table	1A
Date:	Friday, July 20, 2007	Sheet 11 of 43

DDRII A CHANNEL

Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.



DDRII B CHANNEL

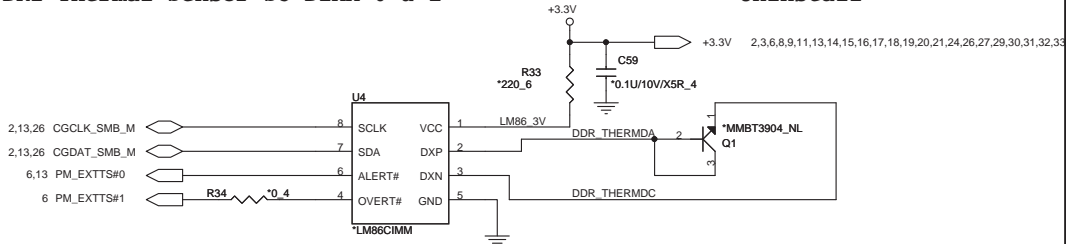


Please these resistor closely DIMMA, all trace length < 750 mil.

Please these resistor closely DIMMB, all trace length < 750 mil.

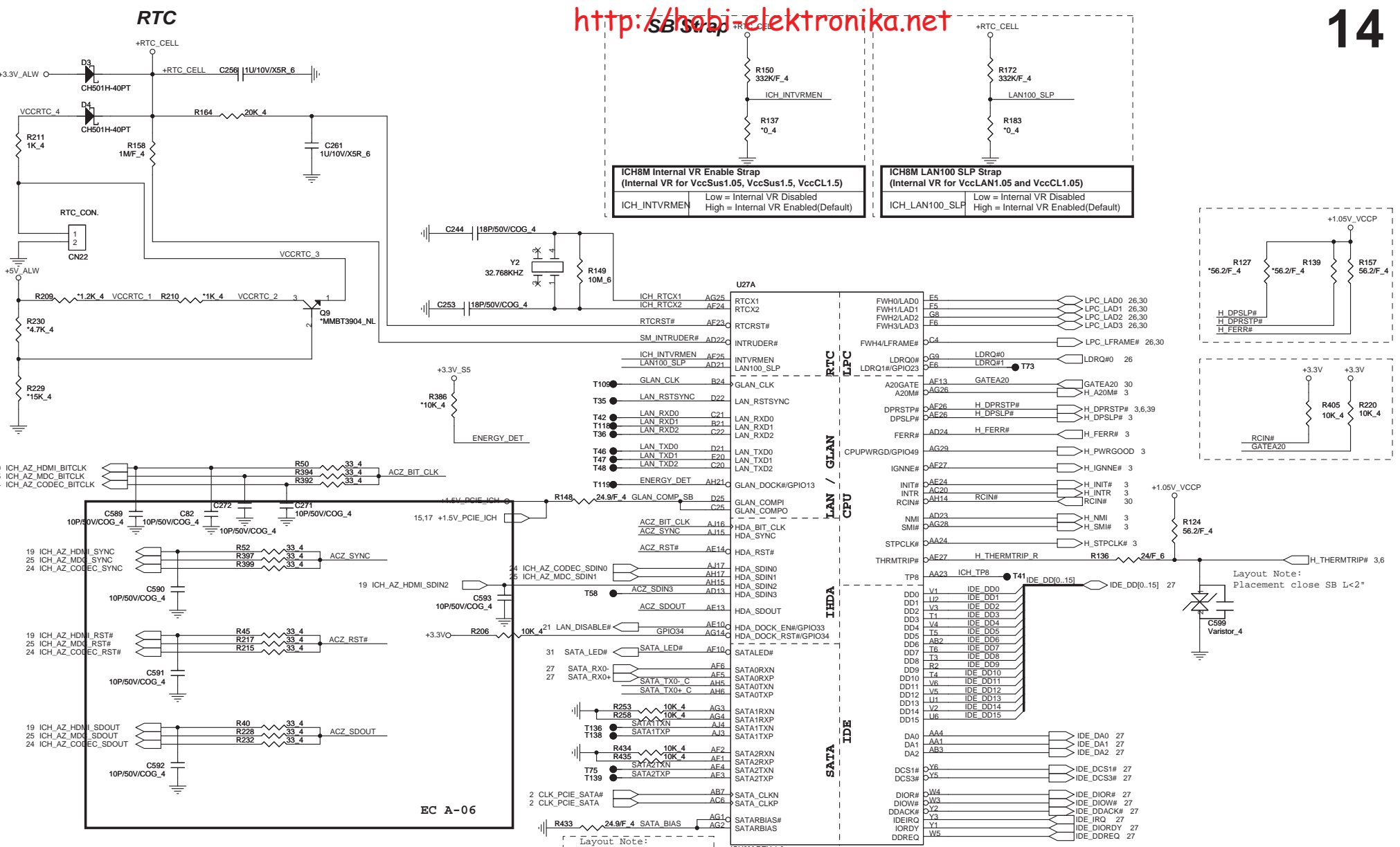
DDR2 Thermal Sensor SO-DIMM 0 & 1

Uninstall



PROJECT : SA1
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Size: Custom | Document Number: **DDR RES. ARRAY** | Rev: 1A
 Date: Friday, July 20, 2007 | Sheet 12 of 43

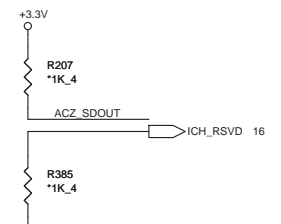


27 SATA_TX0- C294 3900P/25V/X7R 4 SATA_TX0- C
27 SATA_TX0+ C293 3900P/25V/X7R 4 SATA_TX0+ C

Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-8 M and cap on the "N" signal for same pair.

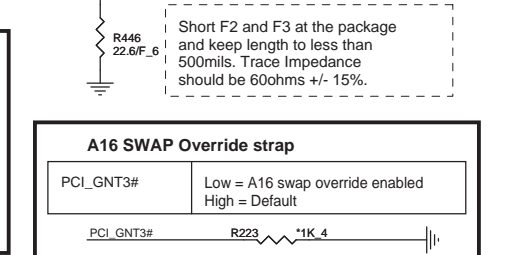
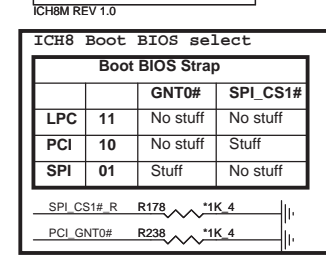
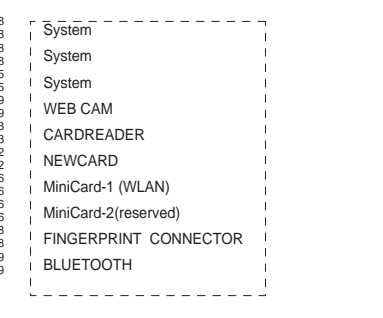
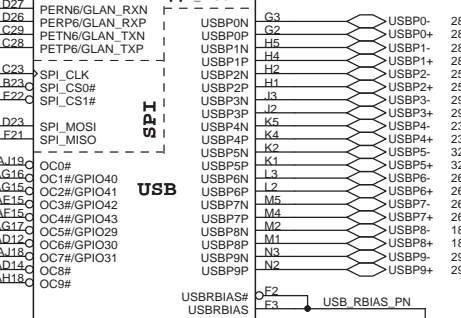
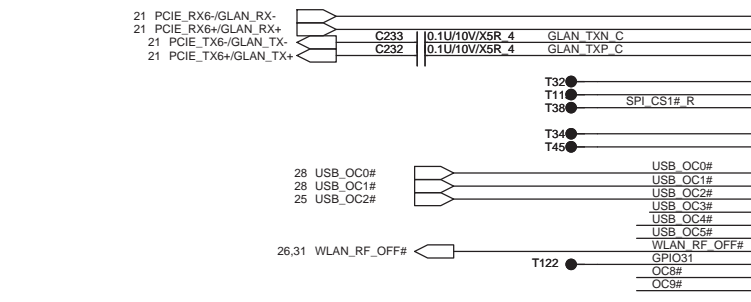
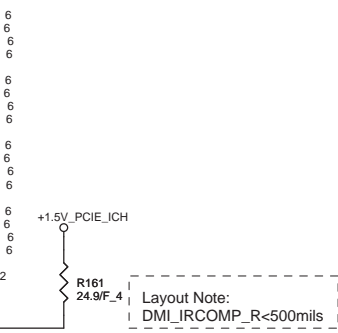
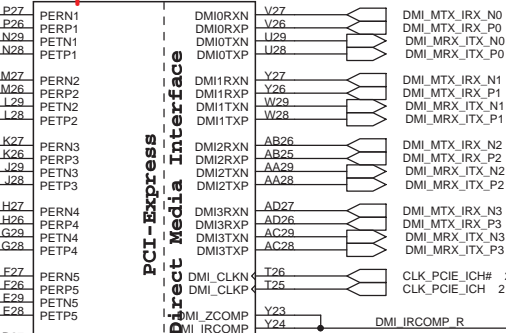
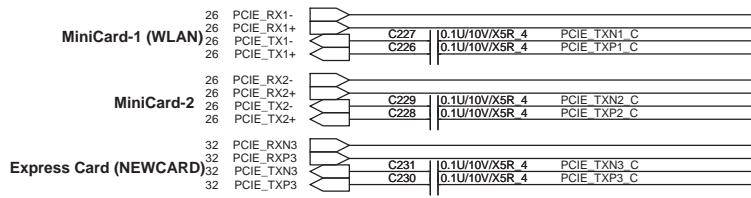
XOR Chain Entrance Strap

ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIE port config bit 1

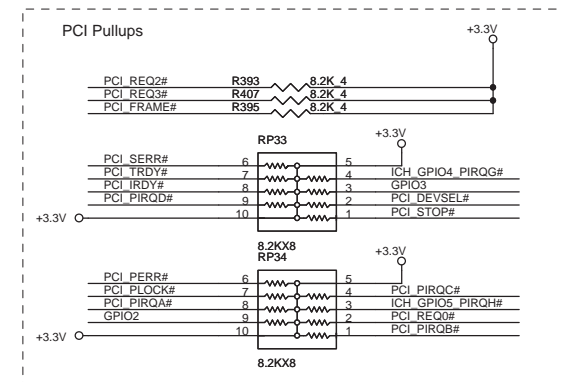
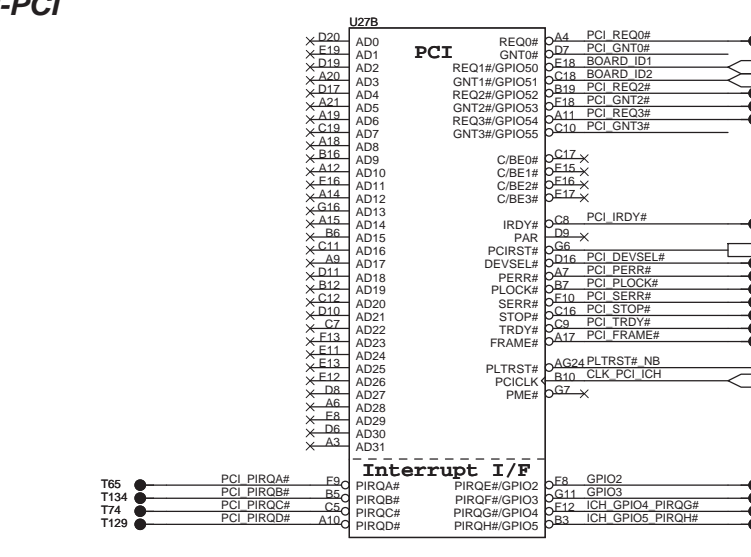
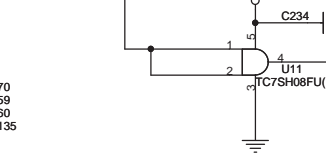
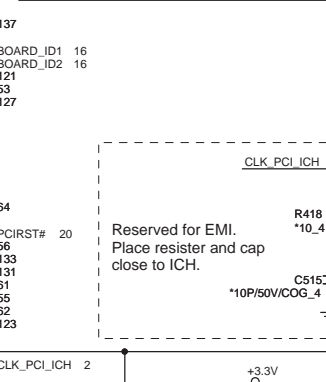
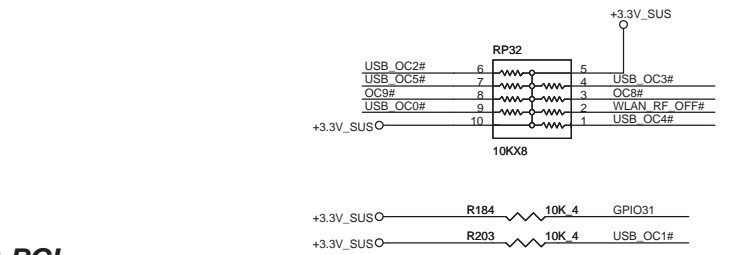


PROJECT : SA1
Quanta Computer Inc.

Size Custom Document Number **ICH8M HOST(1 of 4)** Rev 1A
Date: Friday, July 20, 2007 Sheet 14 of 43



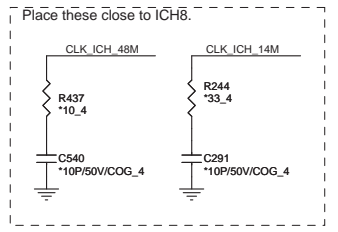
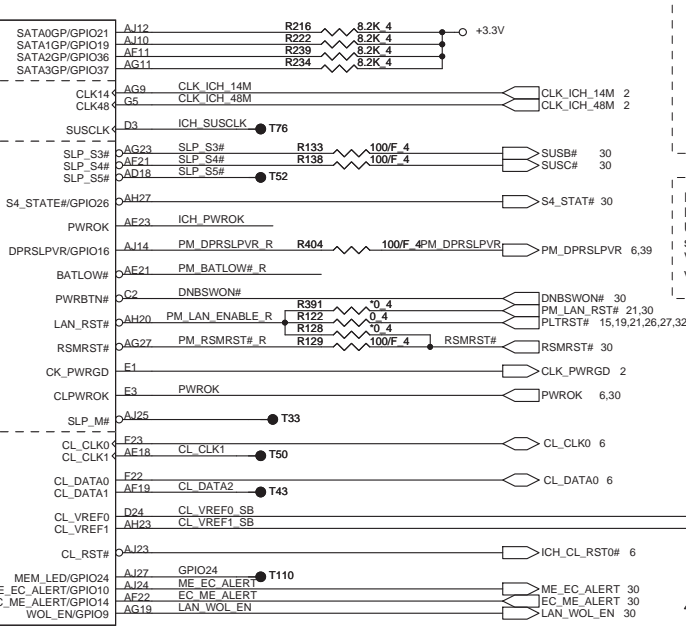
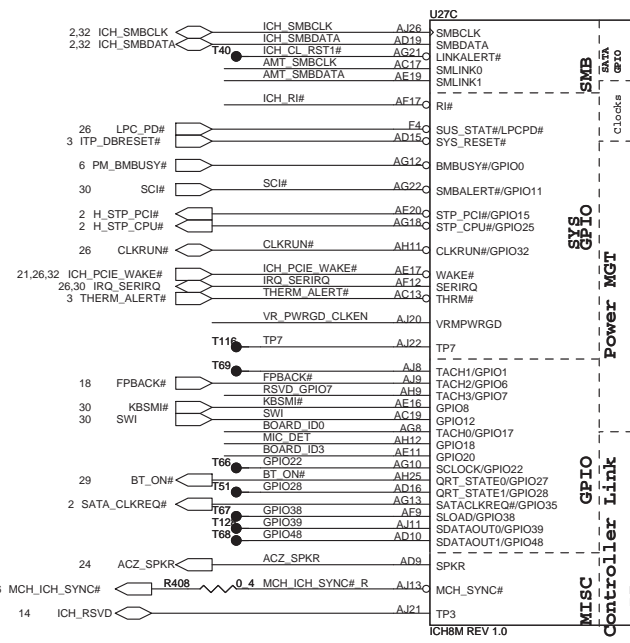
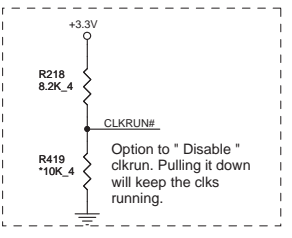
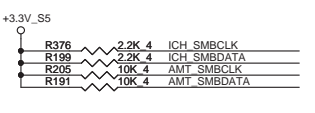
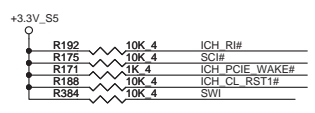
SB-PCI



PROJECT : SA1
Quanta Computer Inc.

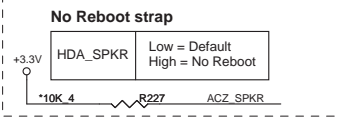
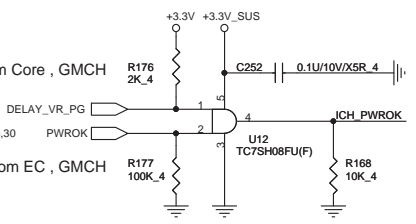
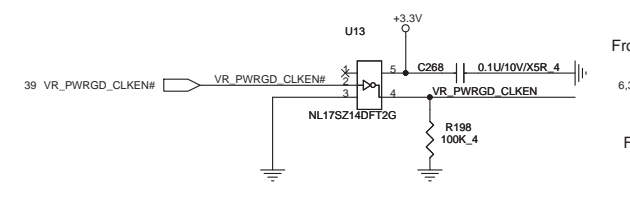
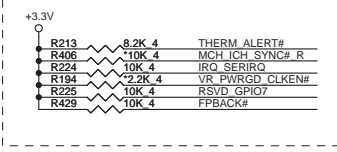
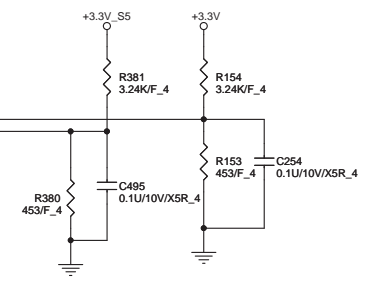
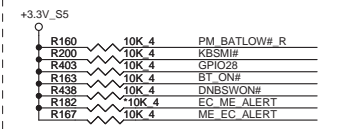
Size Document Number
 Custom ICH8M PCIE(2 of 4) Rev 1A

Date: Friday, July 20, 2007 Sheet 15 of 43

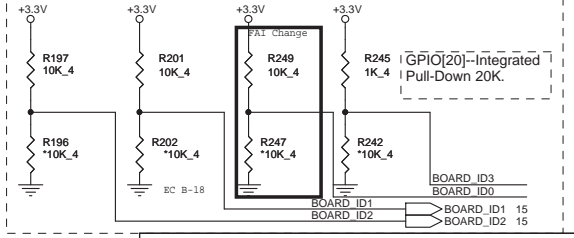
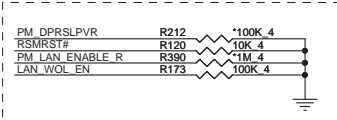


Place these close to ICH8.

If no use internal LAN MAC connect LAN_RST# to PLTRST#
Use internal LAN MAC connect LAN_RST# to RSMRST# should go high no sooner than 10 ms after both VccLAN3_3 and VccLAN1_5 have reached their nominal I voltages.



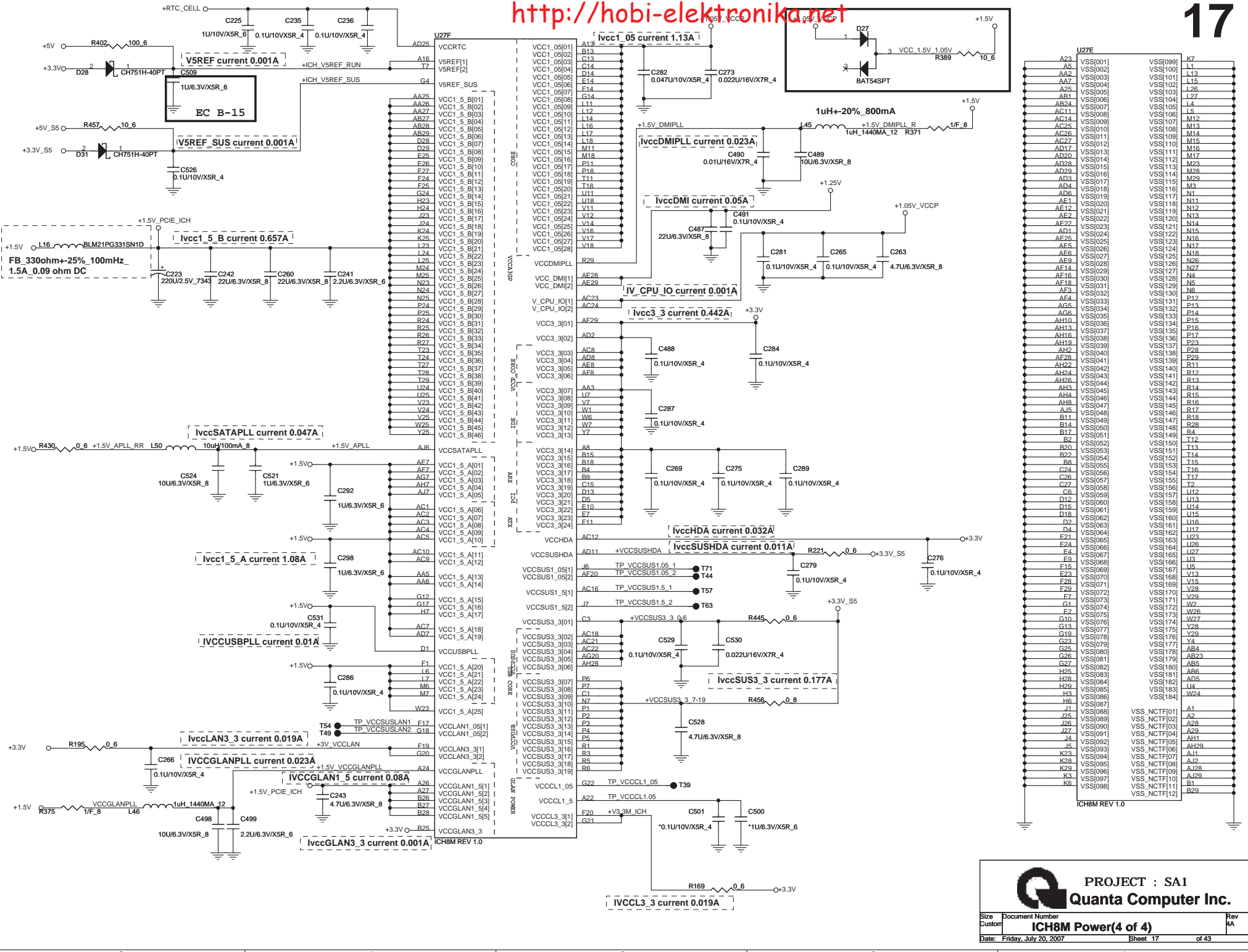
Board ID	ID3	ID2	ID1	ID0
965/HDMI(Rev:A or B M/B)	1	1	1	1
965/HDMI(Rev:C M/B)	1	1	1	1
960/non-HDMI(Rev:C M/B)	1	0	0	1



PROJECT : SA1
Quanta Computer Inc.

Size Custom Document Number **ICH8M GPIO(3 of 4)** Rev 1A

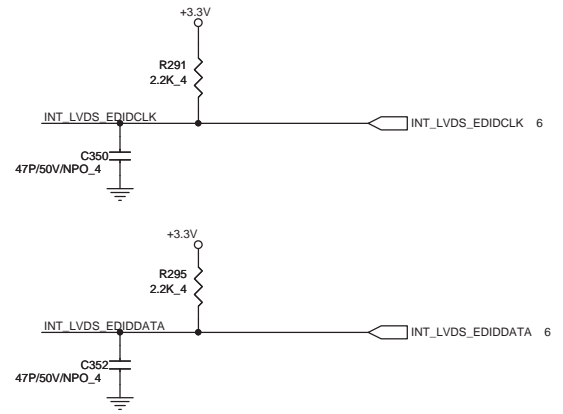
Date: Tuesday, July 24, 2007 Sheet 16 of 43



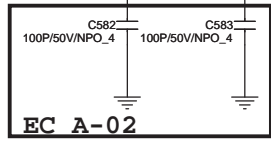
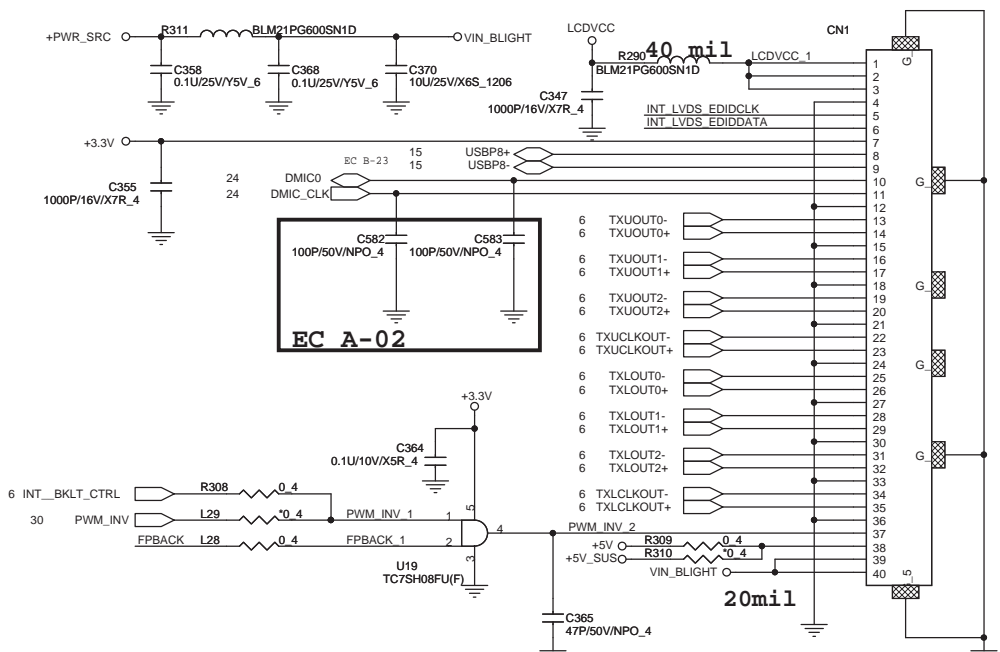
PROJECT : SA1
Quanta Computer Inc.

Size Document Number
 Custom ICH8M Power(4 of 4) Rev 1A

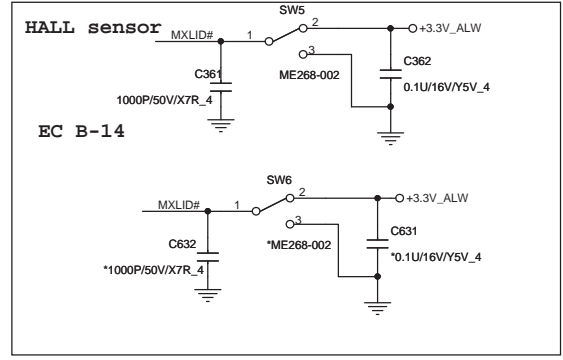
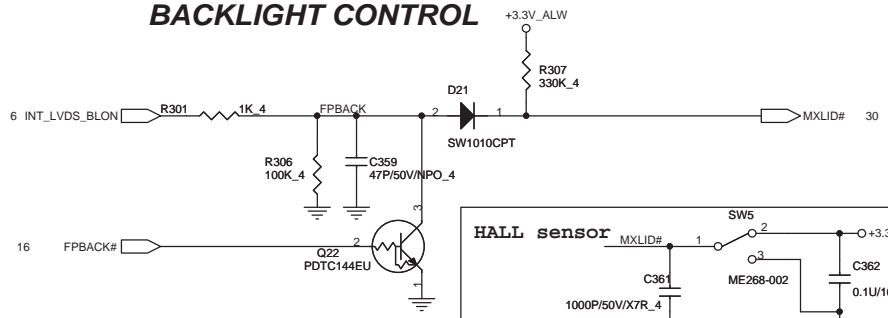
Date: Friday, July 20, 2007 Sheet 17 of 43



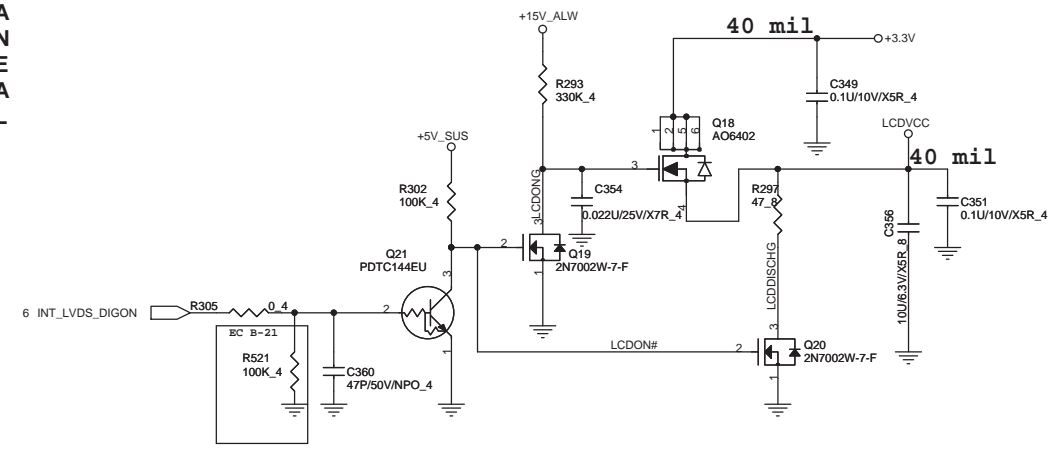
LCD CONNECTOR(Include WEB CAM function)



BACKLIGHT CONTROL



PANEL VCC CONTROL



TOP PANEL

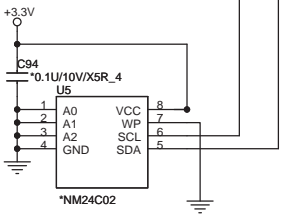
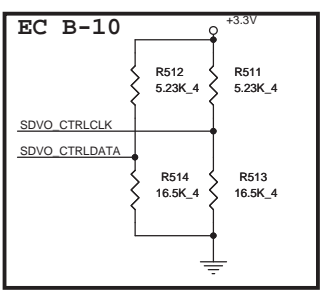
PROJECT : SA1
Quanta Computer Inc.

Size: Custom Document Number: LVDS/LCD CONN/LID/WEB CAM Rev: A
 Date: Friday, July 20, 2007 Sheet 18 of 43

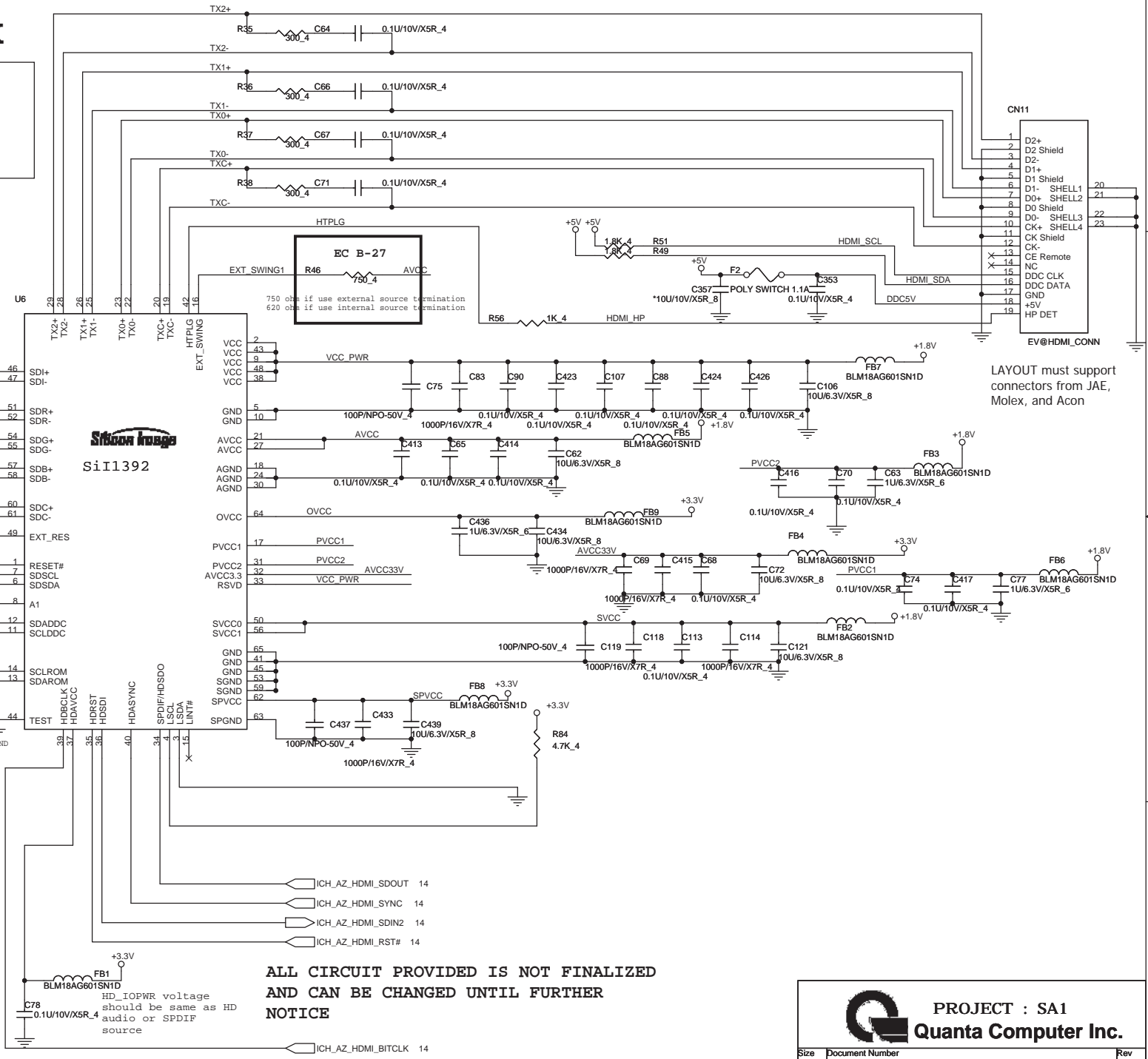
SiI1392 HDMI TX

LAYOUT RULES:

Route traces with 100 Ohm Differential Impedance
 Avoid placing GND Copper or traces adjacent to TMDS Trace
 Put these 4 resistors and 4 capacitors as close as possible to the TMDS output pins of the SiI1392



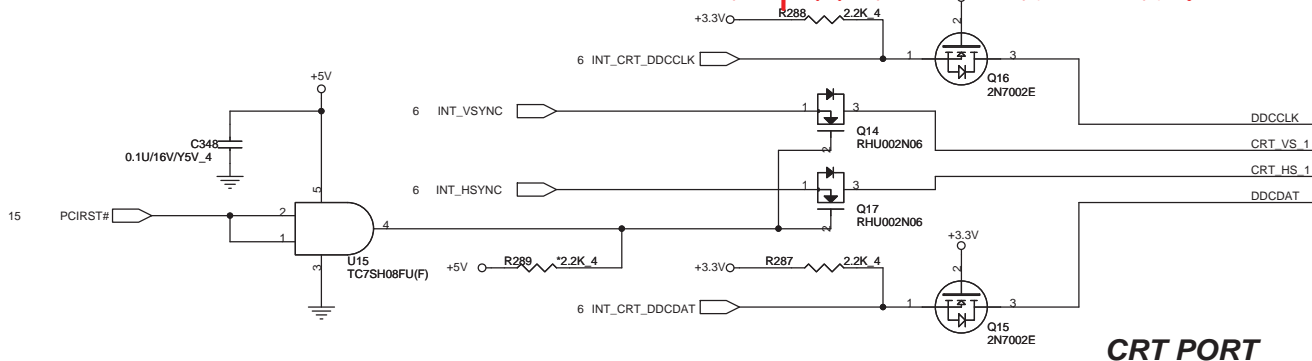
LANCELOT



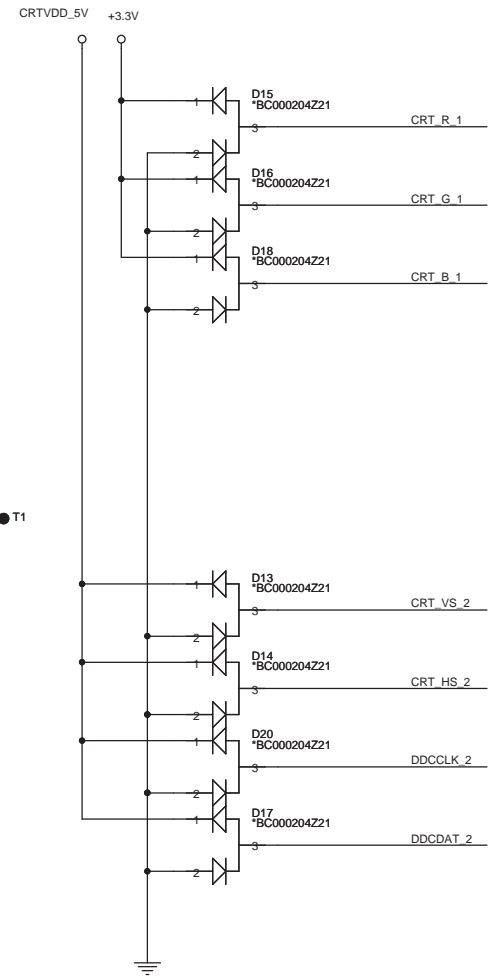
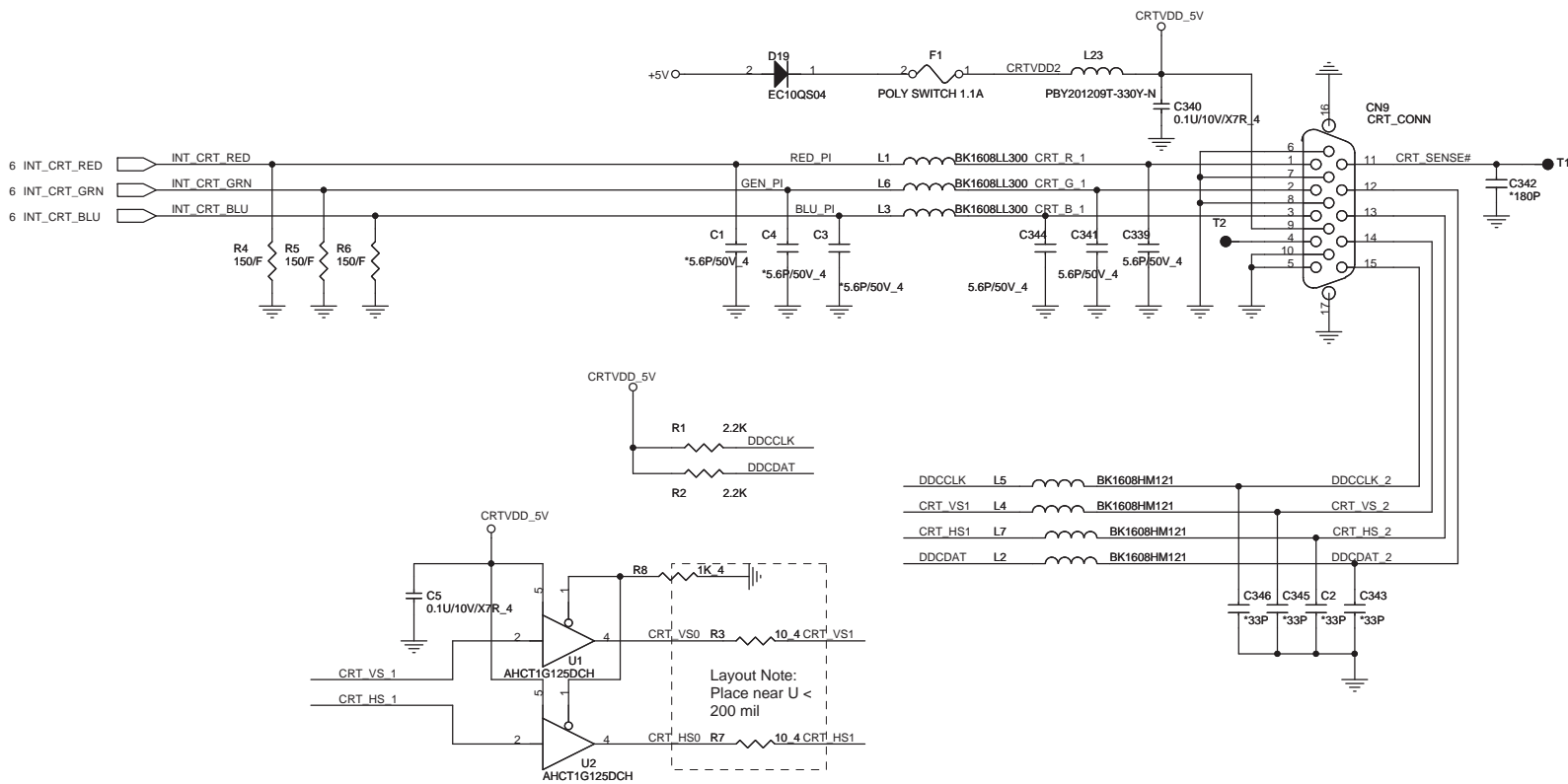
**ALL CIRCUIT PROVIDED IS NOT FINALIZED
 AND CAN BE CHANGED UNTIL FURTHER
 NOTICE**

PROJECT : SA1
Quanta Computer Inc.

Size: Custom Document Number: **HDMI** Rev: 1A
 Date: Monday, July 23, 2007 Sheet: 19 of 43

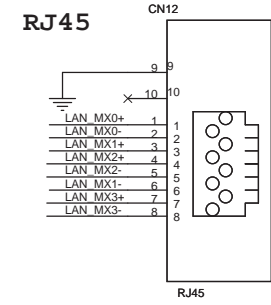
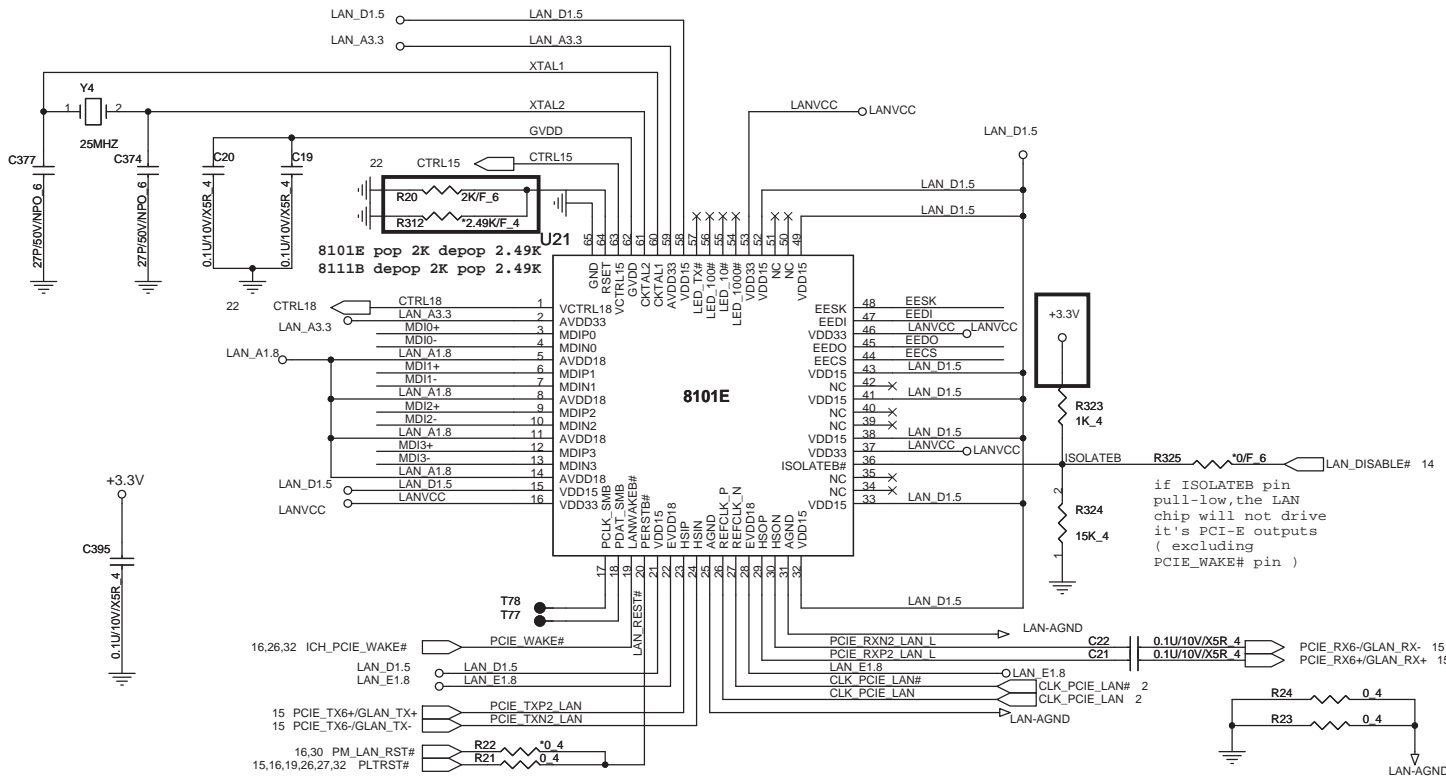


CRT PORT

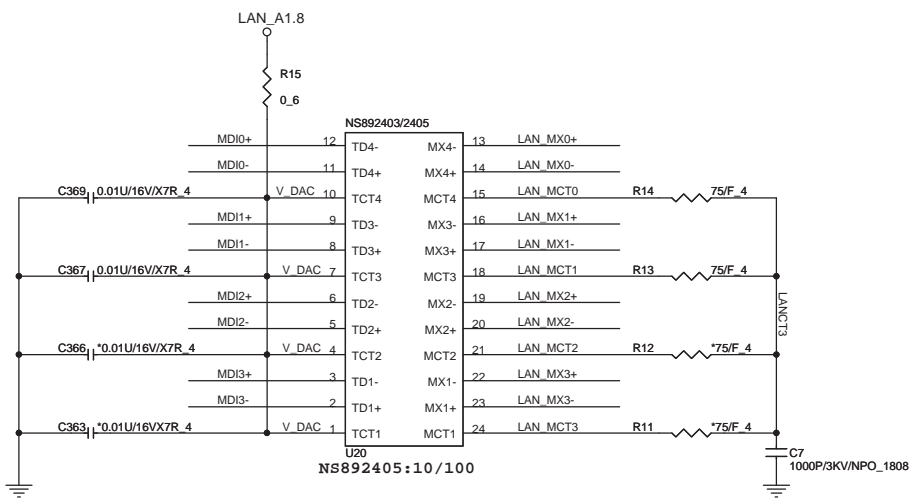
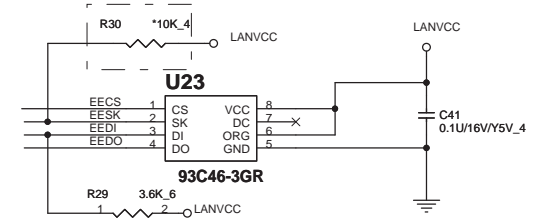


PROJECT : SA1
Quanta Computer Inc.

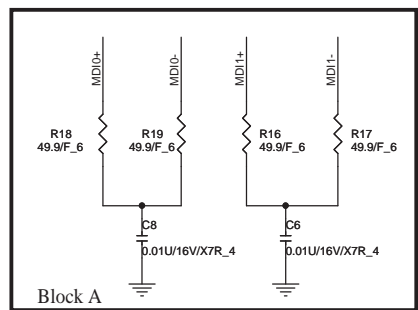
Size Custom	Document Number CRT PORT	Rev 4A
Date: Monday, July 23, 2007	Sheet 20	of 43



for 93C56 used. NC if 93C46 is used.



BLOCK A is only for RTL8101E application.

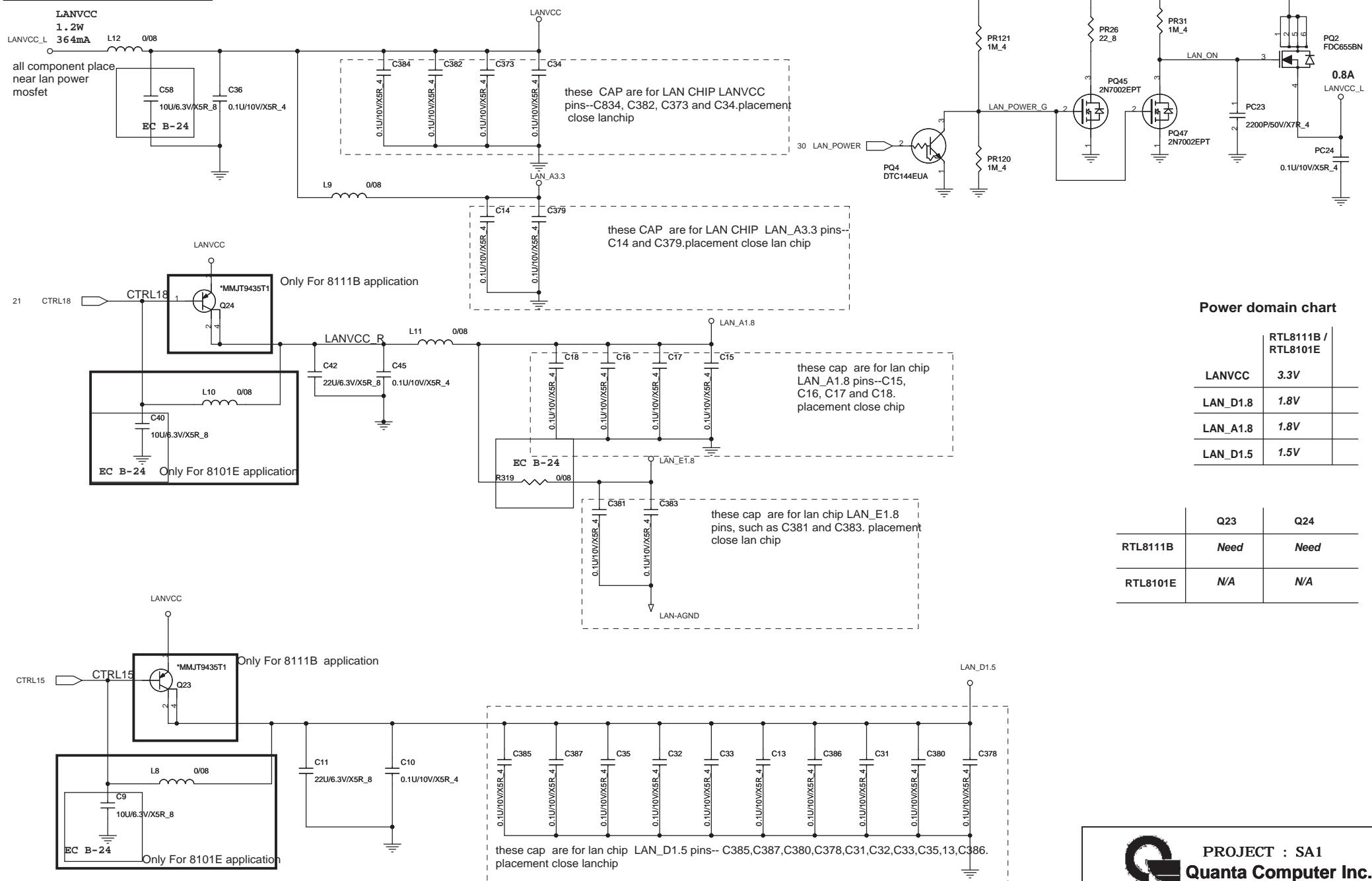


	10/100M	1G
R14 R15 R16 R17	ASM	NoASM

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Quanta Computer Inc.
 Size Document Number
 Customr LAN-REALTEK 8101E Rev 1A
 Date: Monday, July 23, 2007 Sheet 21 of 43

T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)



Power domain chart

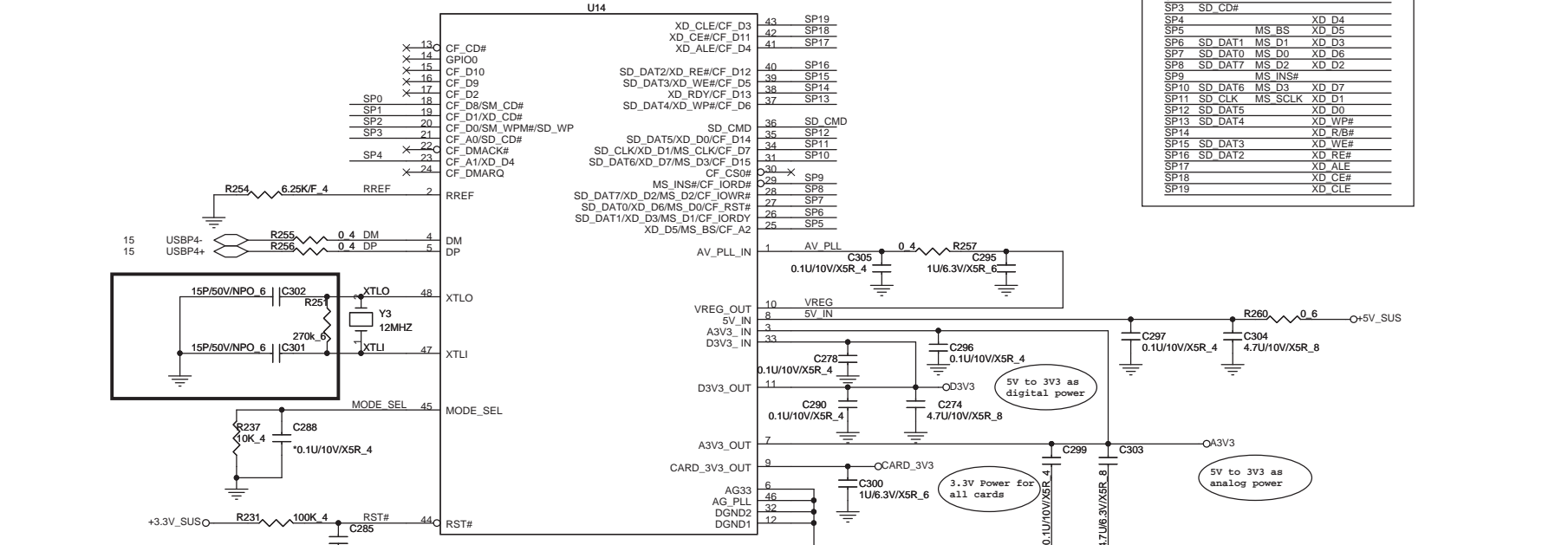
	RTL8111B / RTL8101E
LANVCC	3.3V
LAN_D1.8	1.8V
LAN_A1.8	1.8V
LAN_D1.5	1.5V

	Q23	Q24
RTL8111B	Need	Need
RTL8101E	N/A	N/A

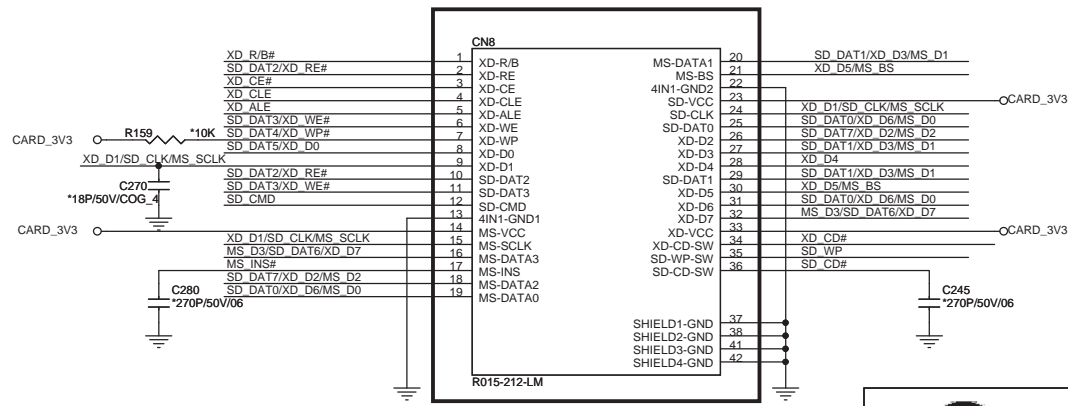
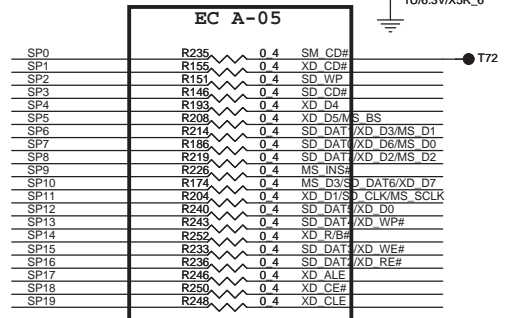
PROJECT : SA1
Quanta Computer Inc.
 Size Document Number
 Custom LAN POWER Rev 1A
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Note:

SP0	SD/MMC	MS	XD
SP1	SD_WP		XD_CD#
SP2			
SP3	SD_CD#		
SP4		MS_BS	XD_D4
SP5			XD_D5
SP6	SD_DAT1	MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

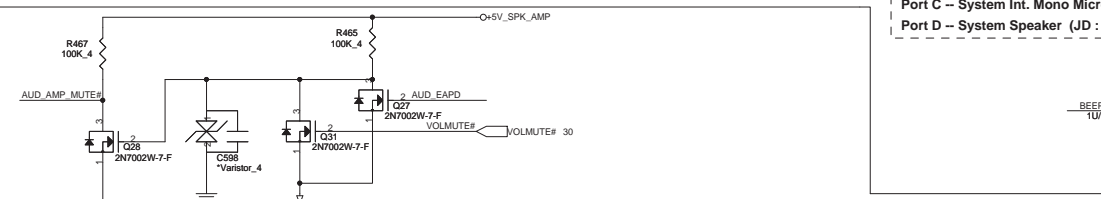
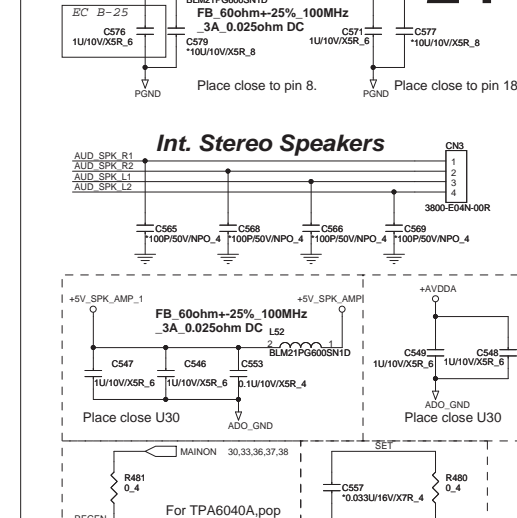
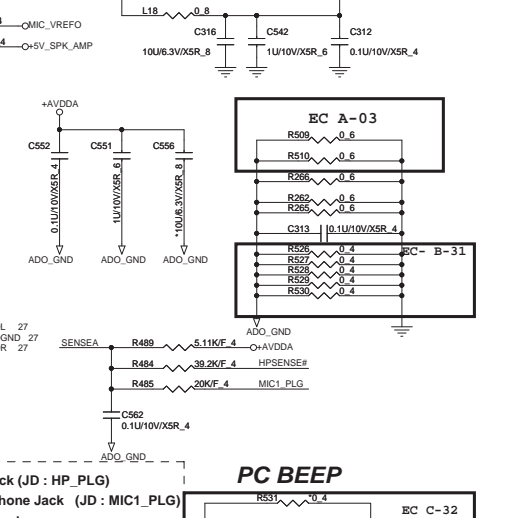
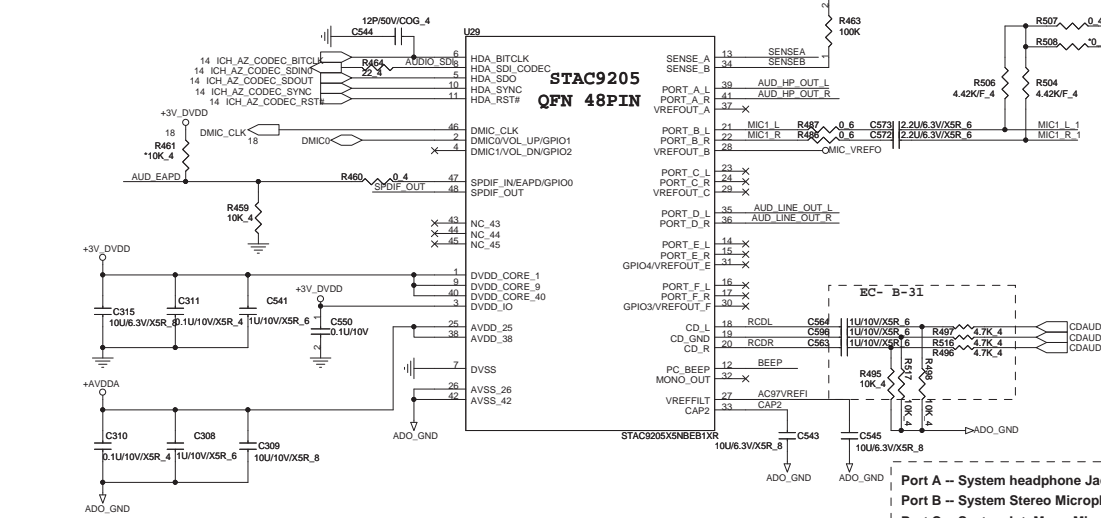


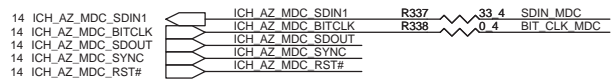
7 IN 1 CARD-READER (PUSH-PUSH)
Support SD/MS/xD/SM/RS-MMC/MMC/miniSD Cards



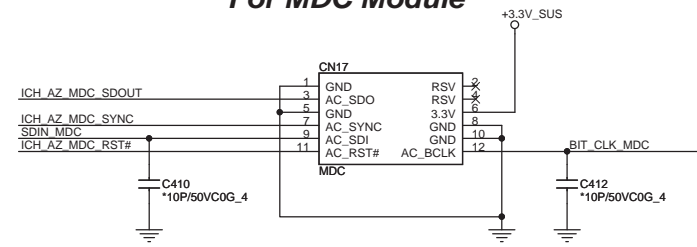
PROJECT : SA1
Quanta Computer Inc.

Size: Document Number: **RTS5158 CONTROLLER** Rev: IA
 Custom: Date: Friday, July 20, 2007 Sheet: 23 of 43

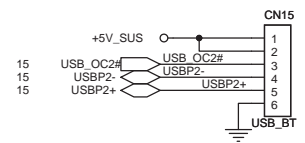




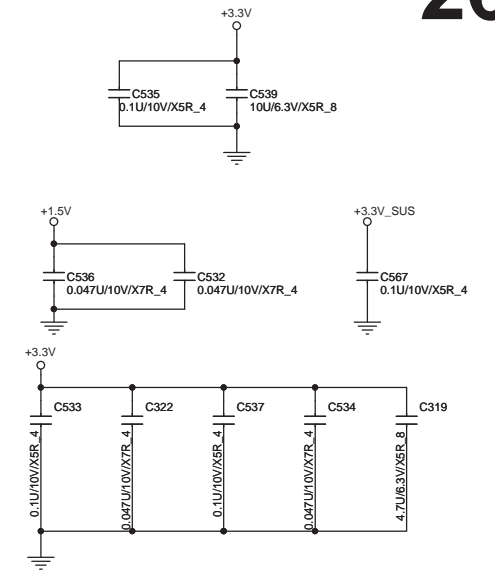
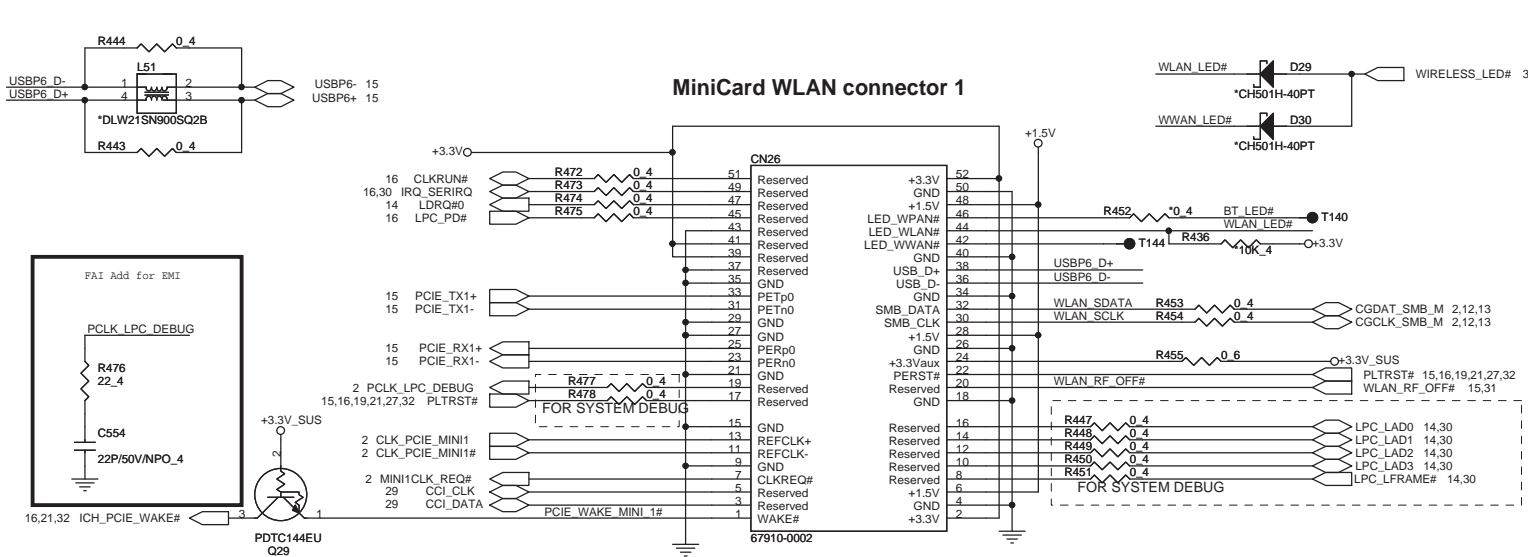
For MDC Module



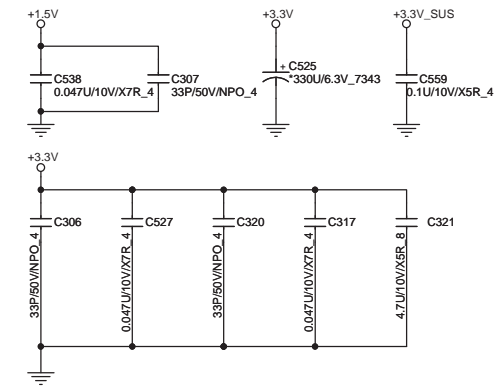
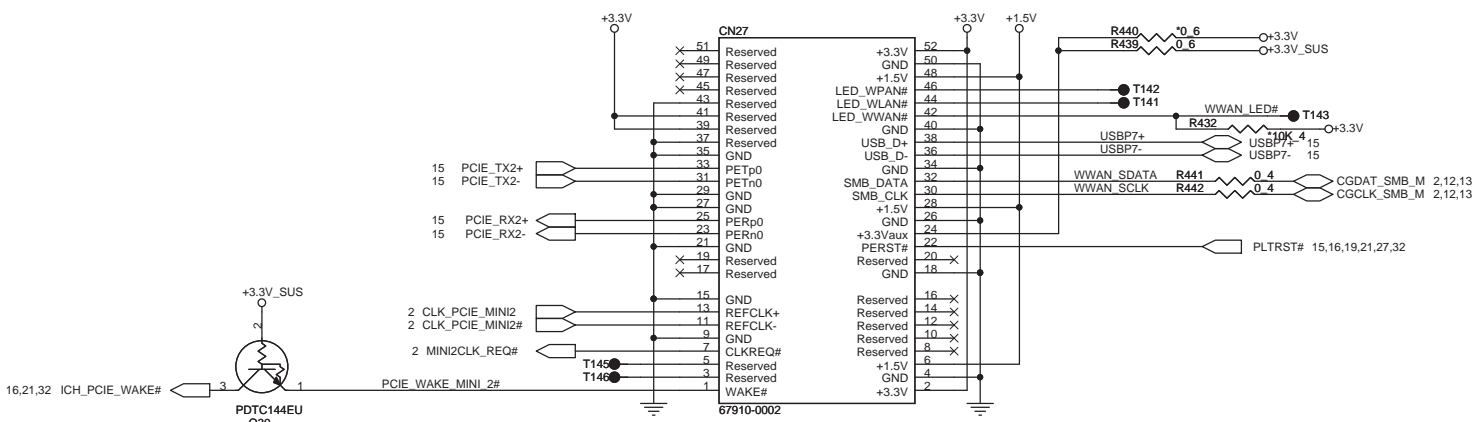
TO RJ11/USB PORT



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 Quanta Computer Inc.
 MODEM(MDC)
 Date: Friday, July 20, 2007 Sheet 25 of 43
 Rev 1A



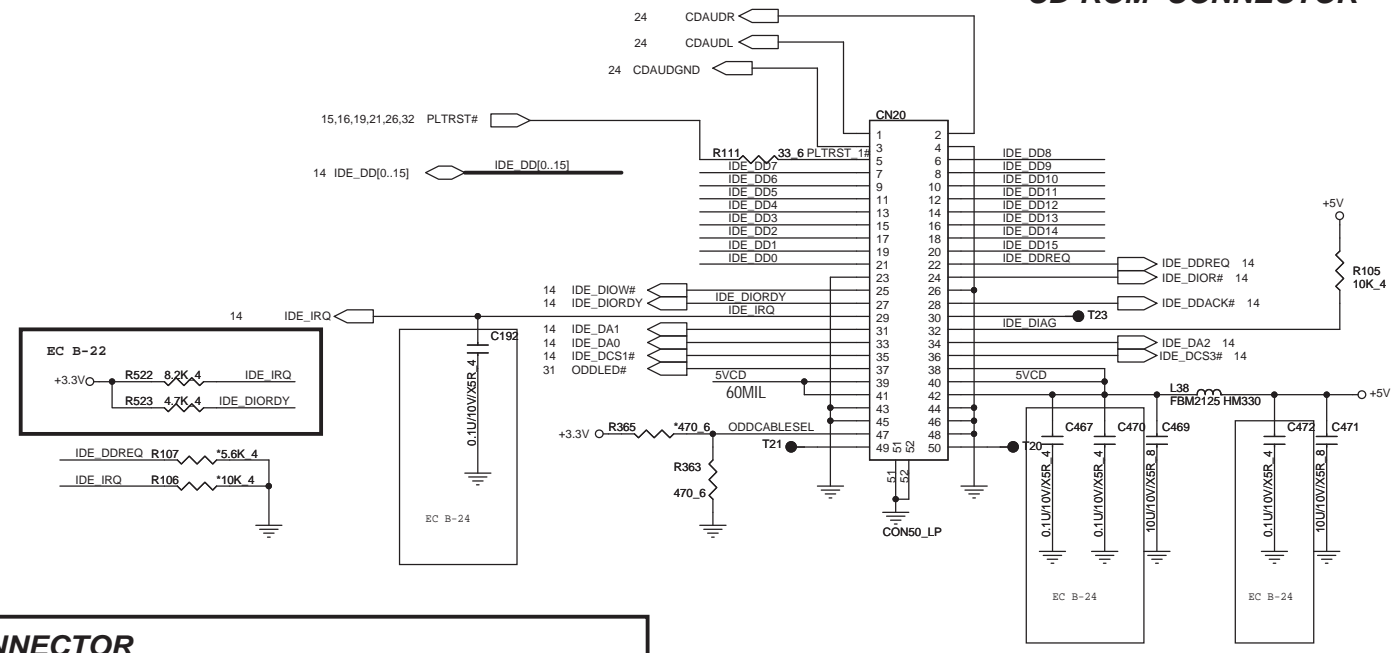
MiniCard connector 2



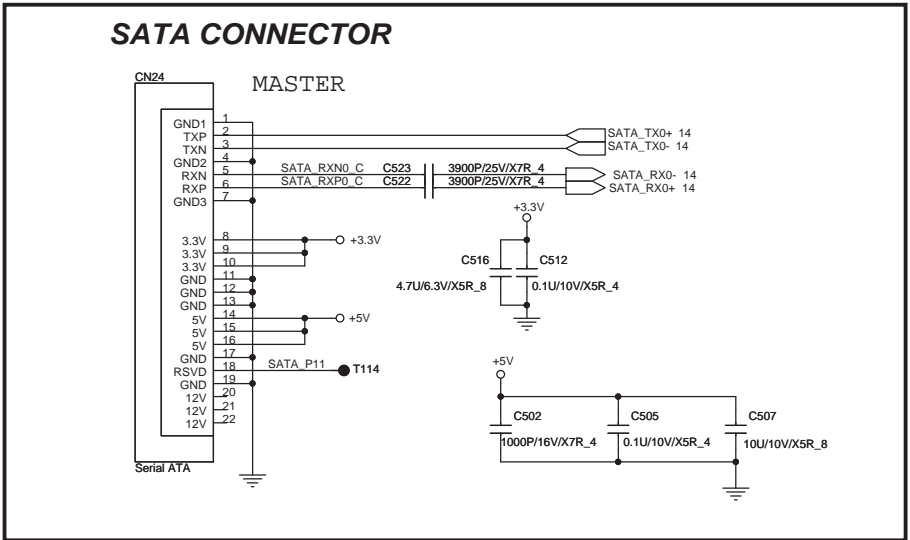
PROJECT : SA1
Quanta Computer Inc.

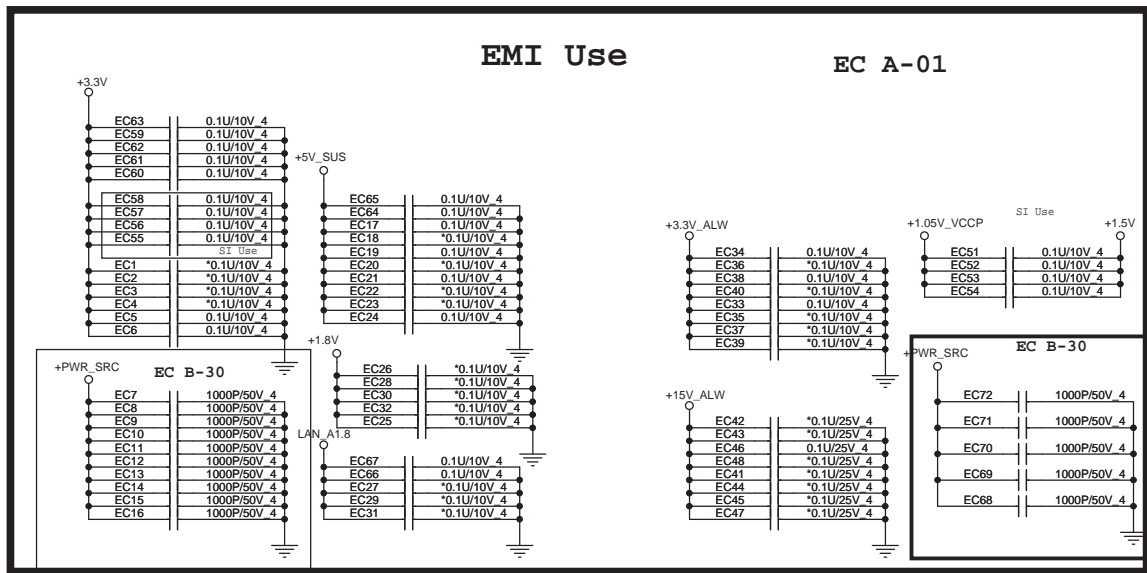
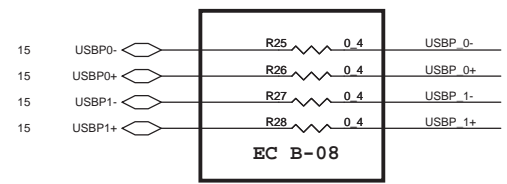
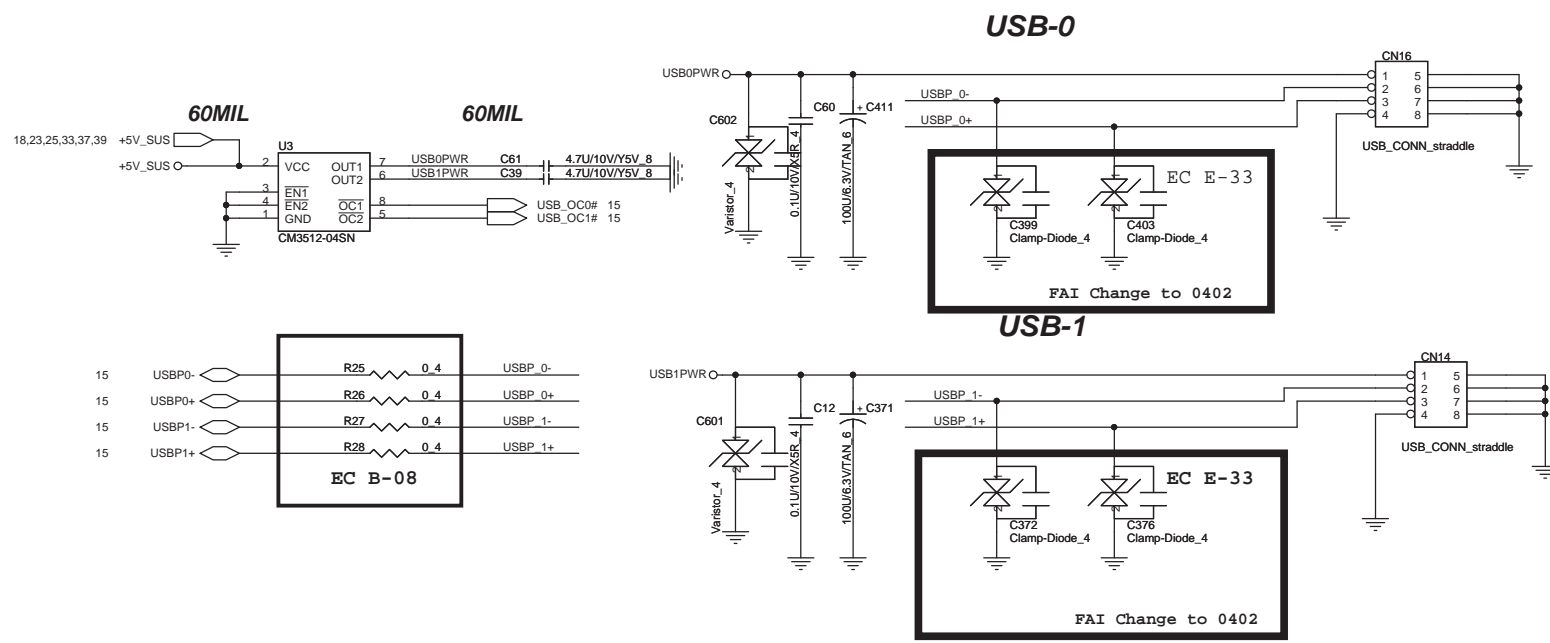
Size: Custom Document Number: MiniCard connector Rev: 1A
Date: Monday, July 23, 2007 Sheet 26 of 43


For fix ODD CD-ROM CONNECTOR



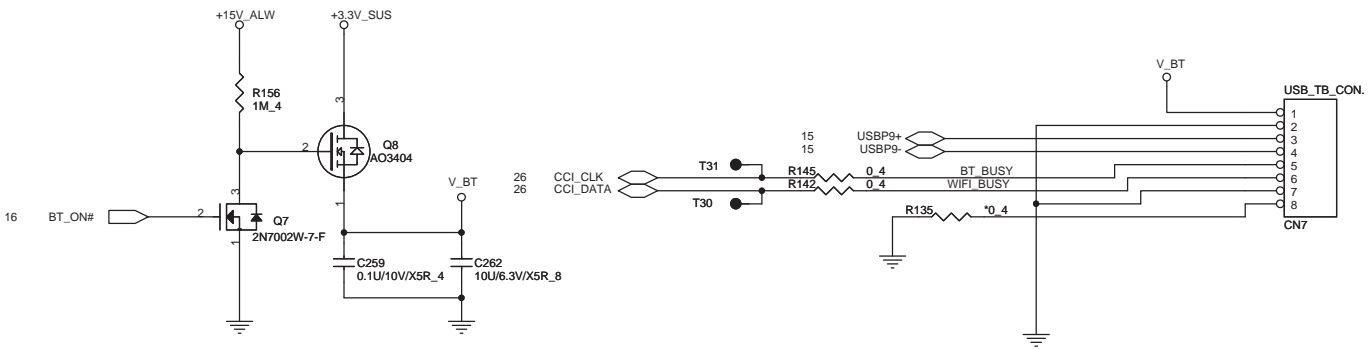
SATA CONNECTOR



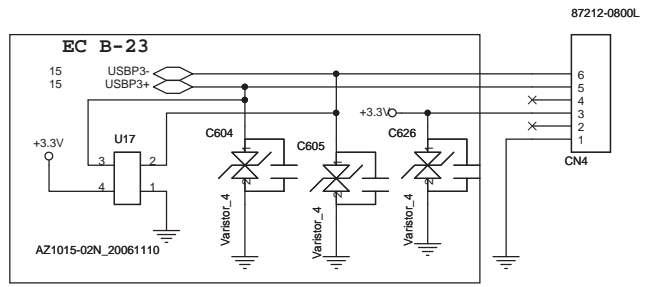


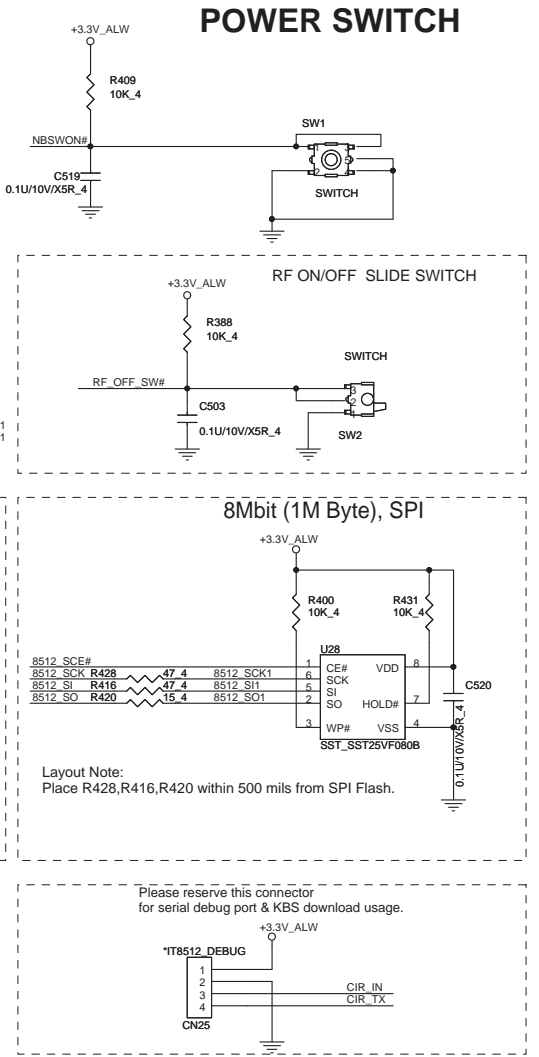
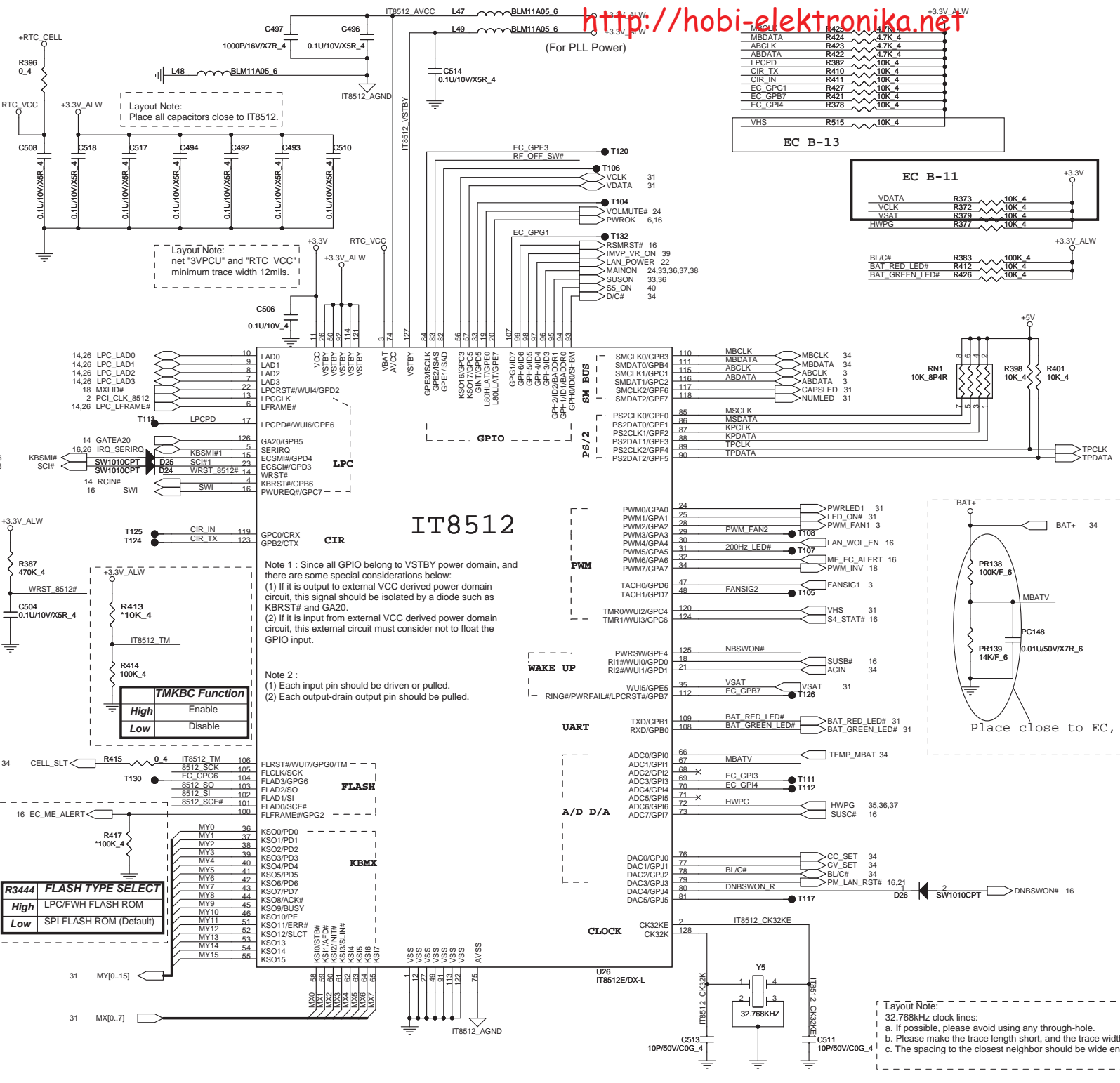

PROJECT : SA1
Quanta Computer Inc.

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Custom	USB PORT	IA
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FINGERPRINT CONNECTOR





IT8512

Note 1 : Since all GPIO belong to VSTBY power domain, there are some special considerations below:
 (1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
 (2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
 (1) Each input pin should be driven or pulled.
 (2) Each output-drain output pin should be pulled.

TMKBC Function

	High	Low
Enable	Enable	Disable
Disable	Disable	Enable

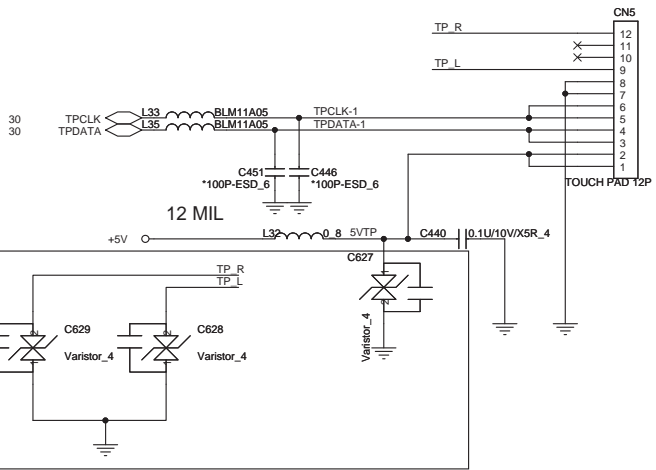
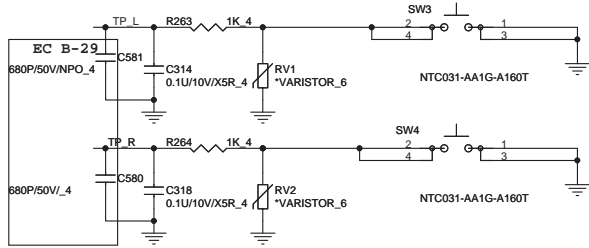
R3444 FLASH TYPE SELECT

	High	Low
LPC/FWH FLASH ROM	High	Low
SPI FLASH ROM (Default)	Low	High

PROJECT : SA1
Quanta Computer Inc.

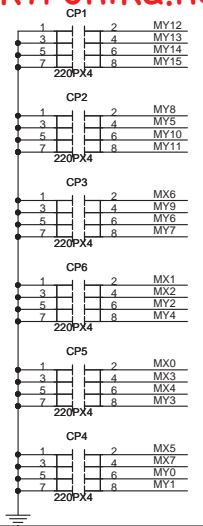
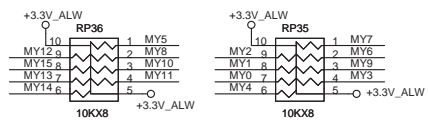
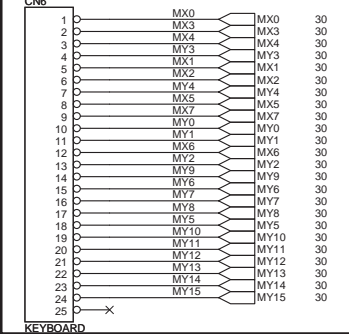
Size Custom Document Number KBC-IT8512 Rev 4A
 Date: Monday, July 23, 2007 Sheet 30 of 43

TOUCHPAD SWITCH CONN

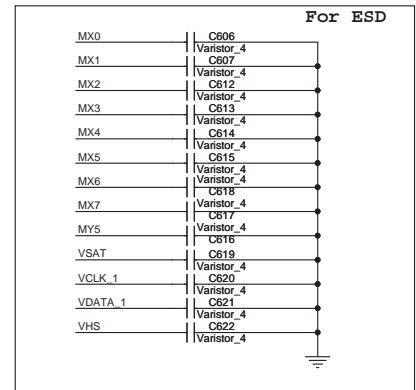
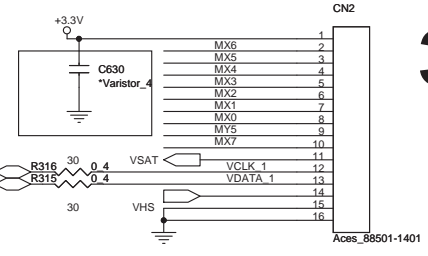
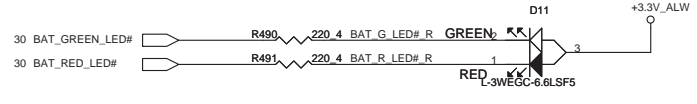
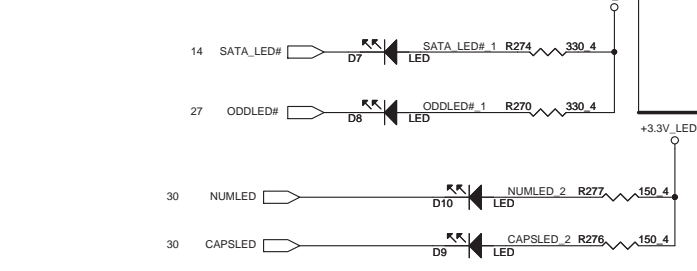


<http://hobi-elektronika.net>

KEYBOARD

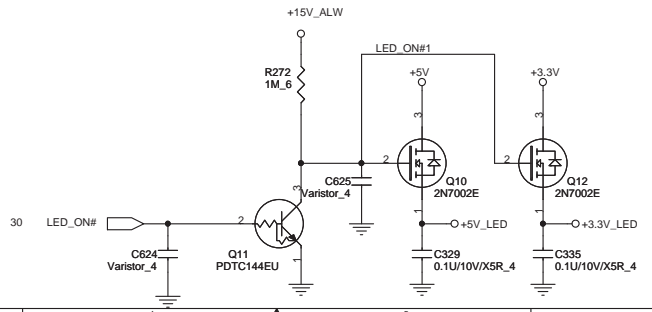
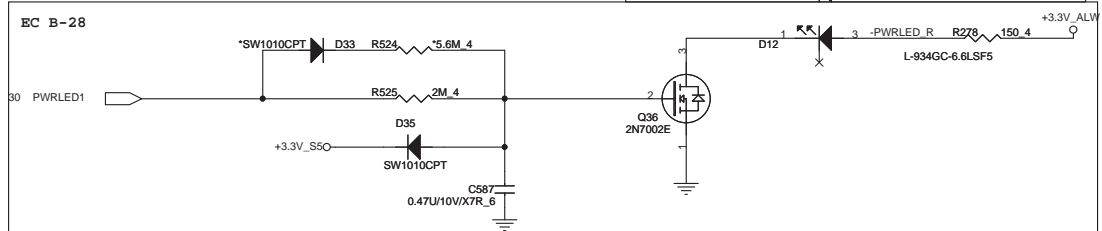
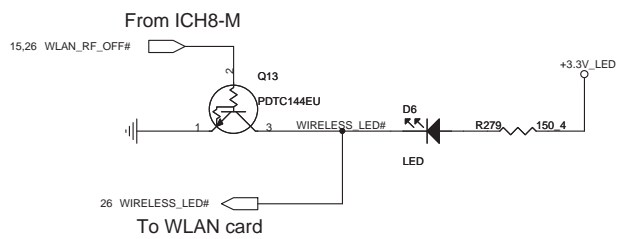


LED INDICATOR

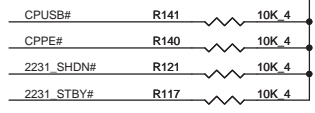
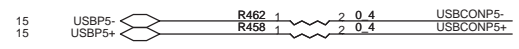


SWITCH/Volume cintral BOARD

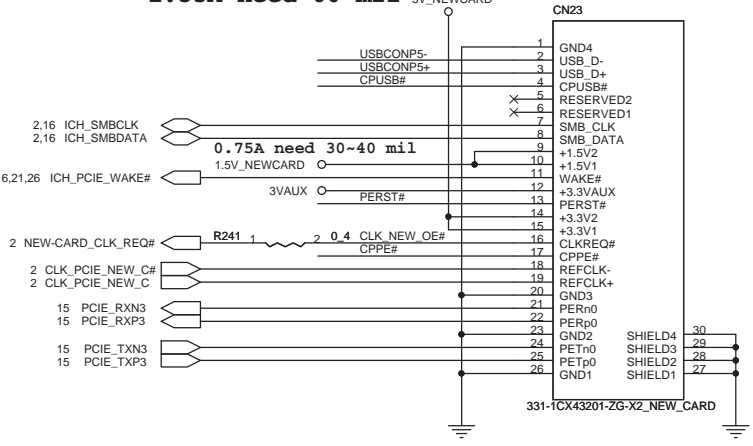
WIRELESS LED



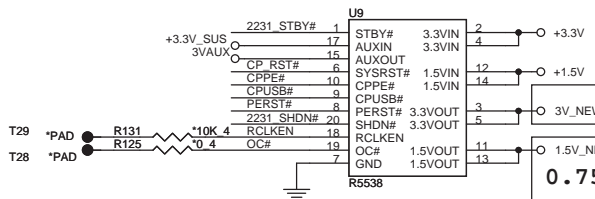
NEWCARD



1.35A need 60 mil

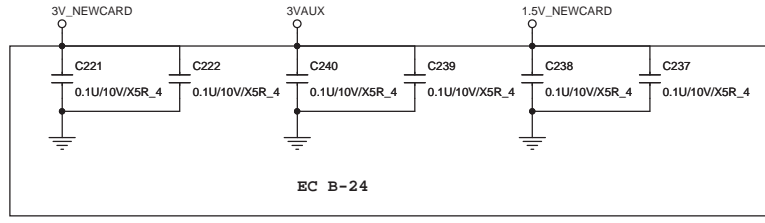
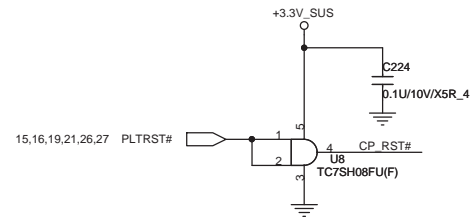


0.75A need 30~40 mil

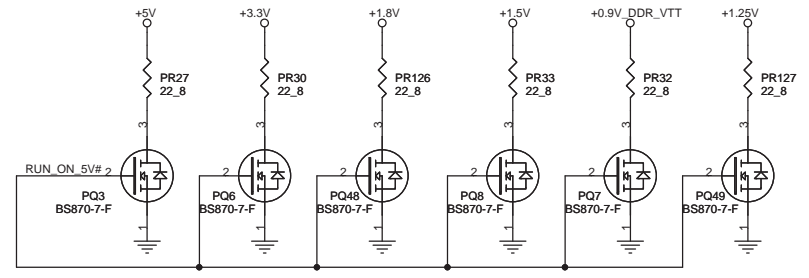
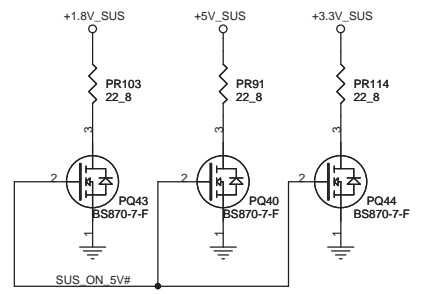
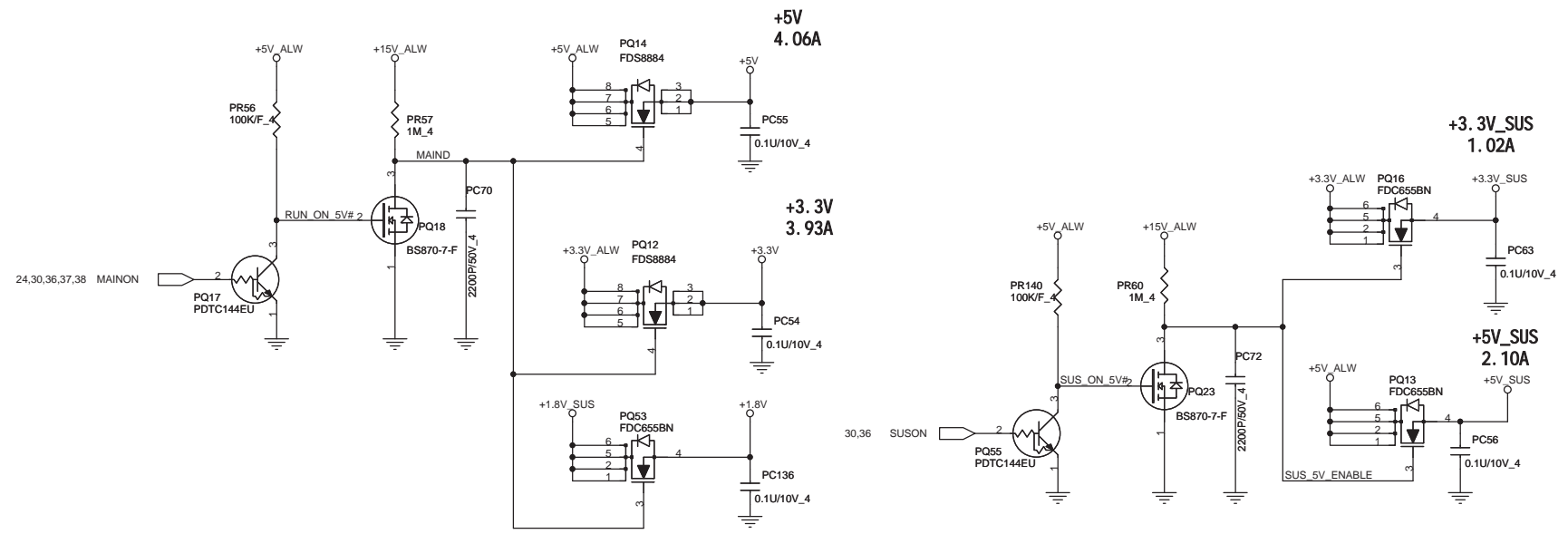


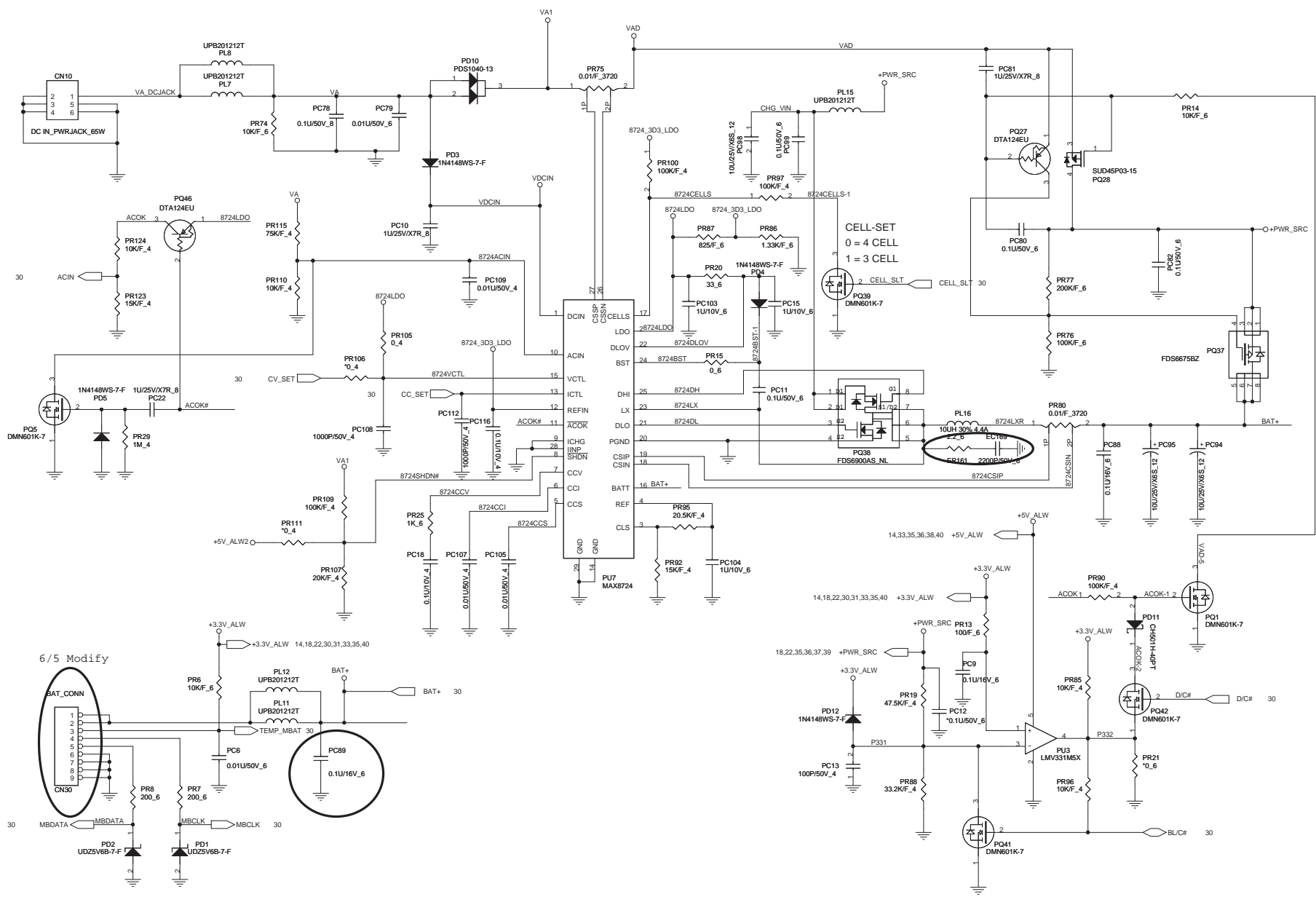
1.35A need 60 mil

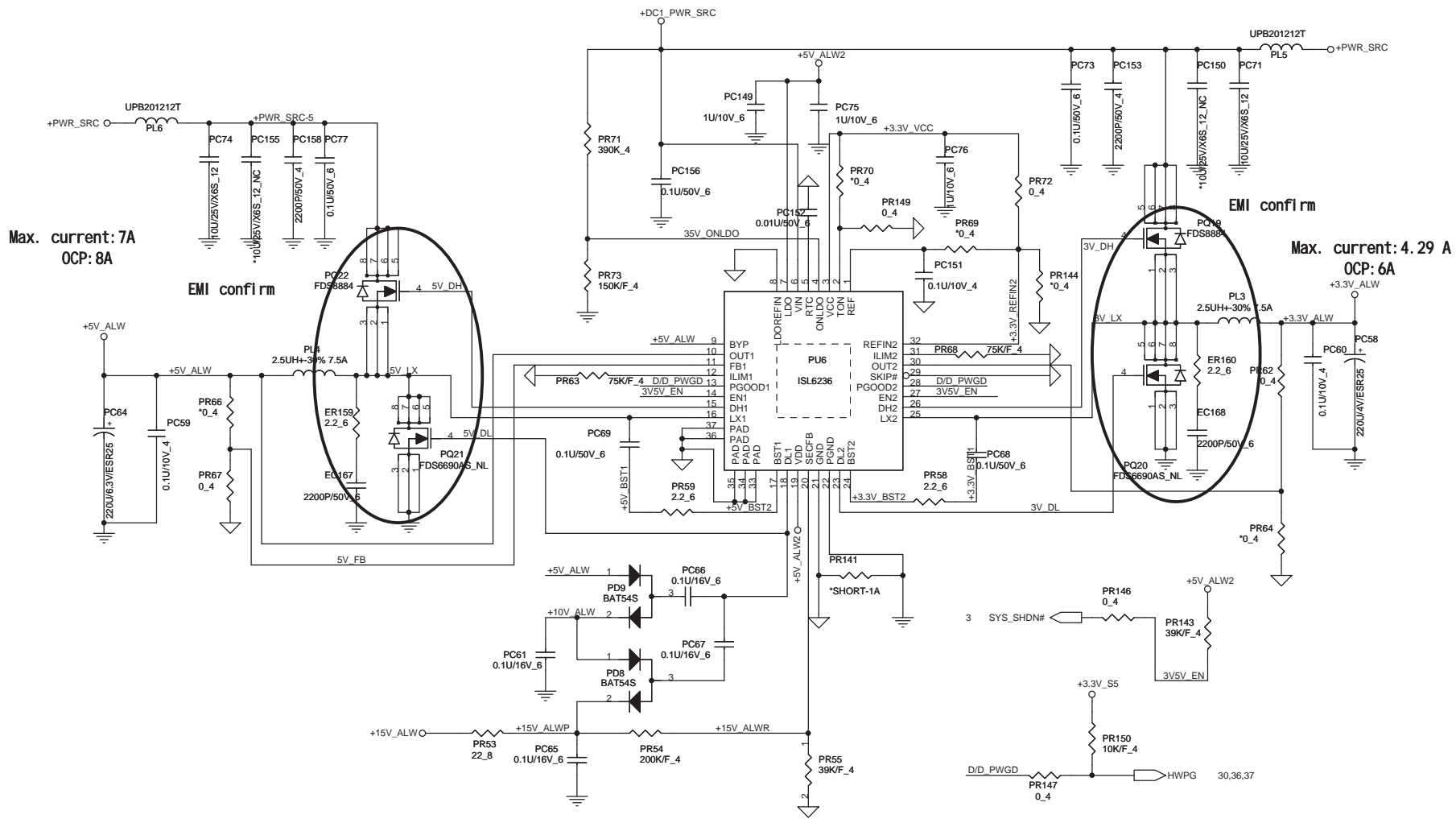
0.75A need 30~40 mil



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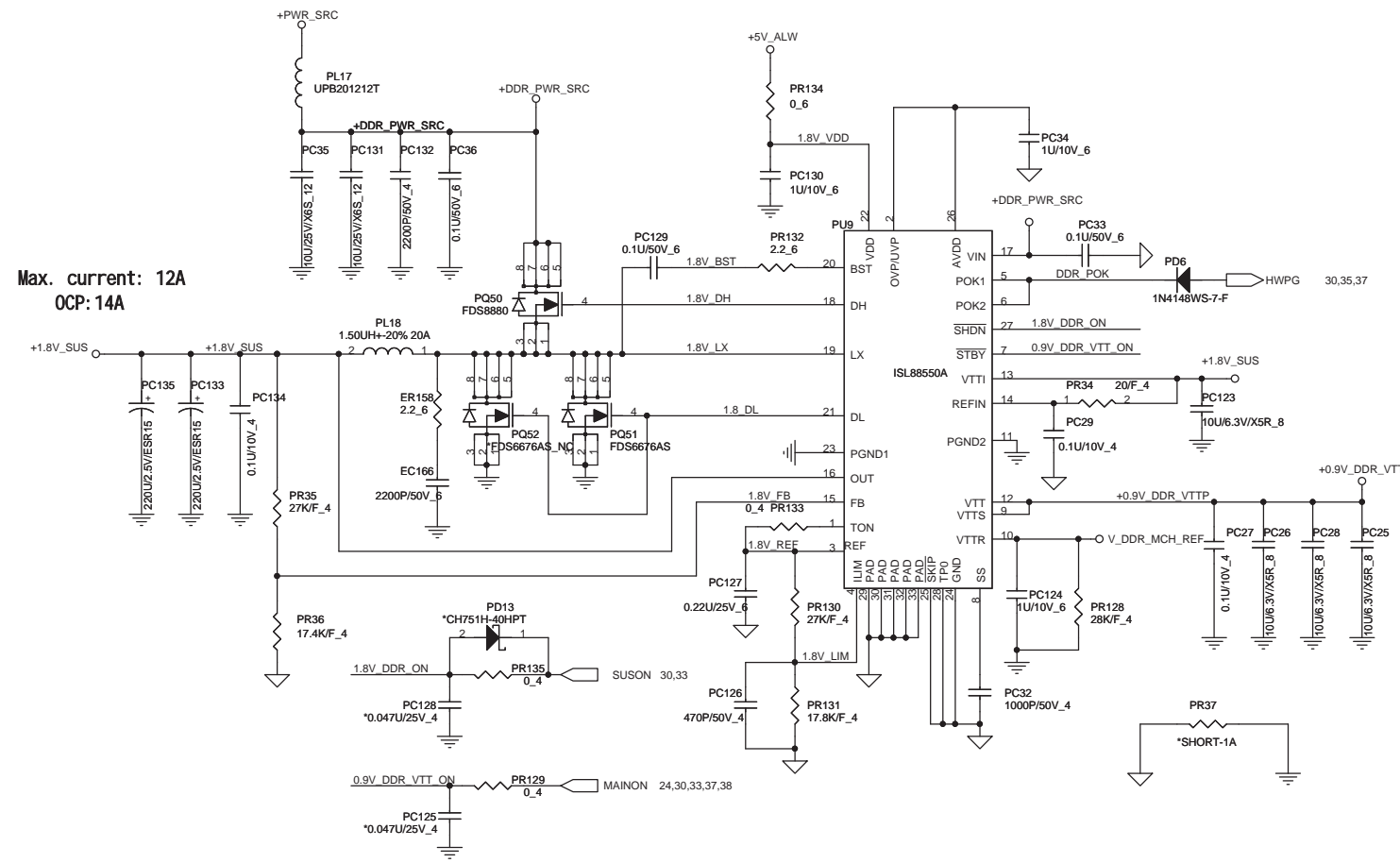







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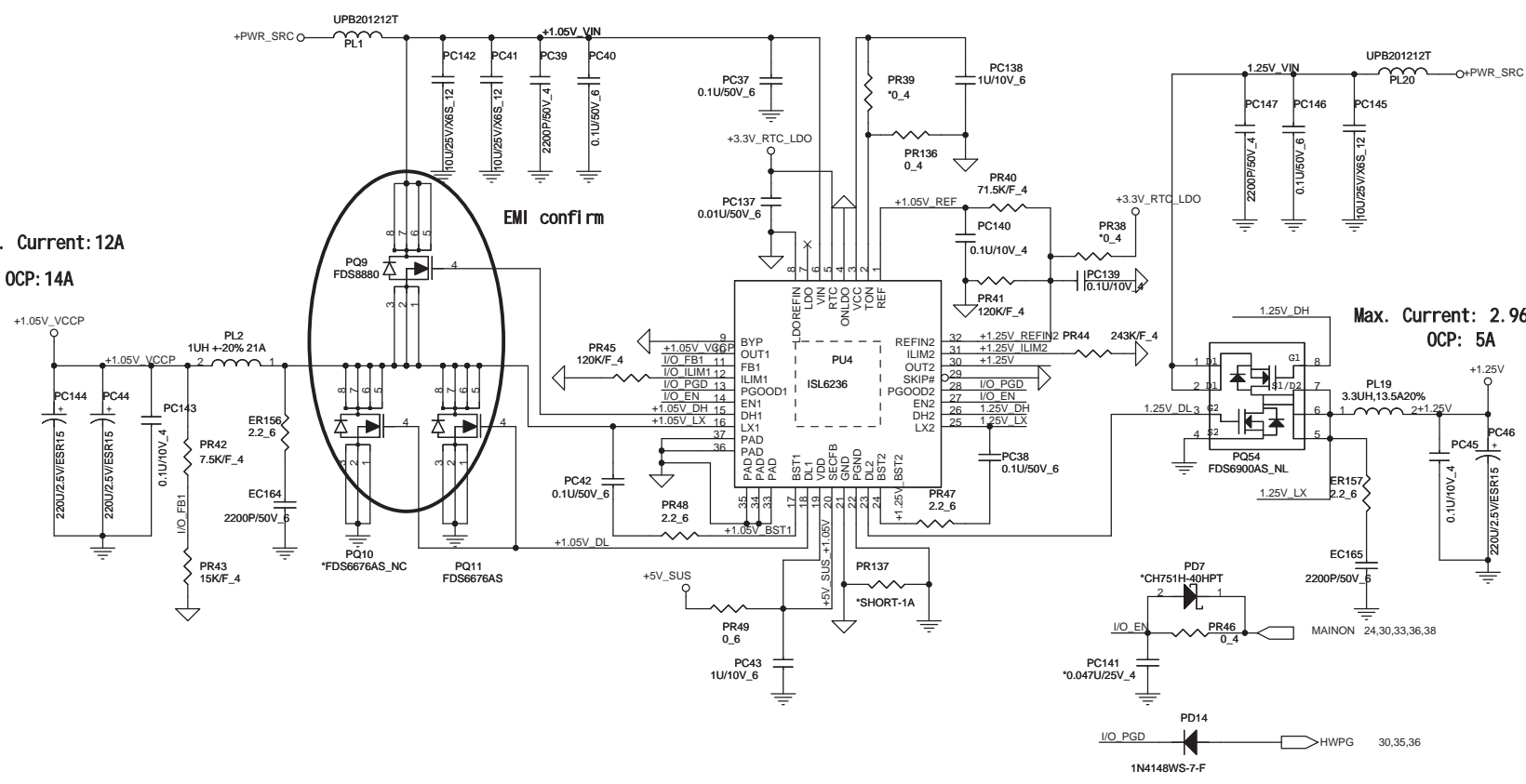


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		Quanta Computer Inc.	
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Custom			
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		Rev	1A

Max. Current: 12A
OCP: 14A

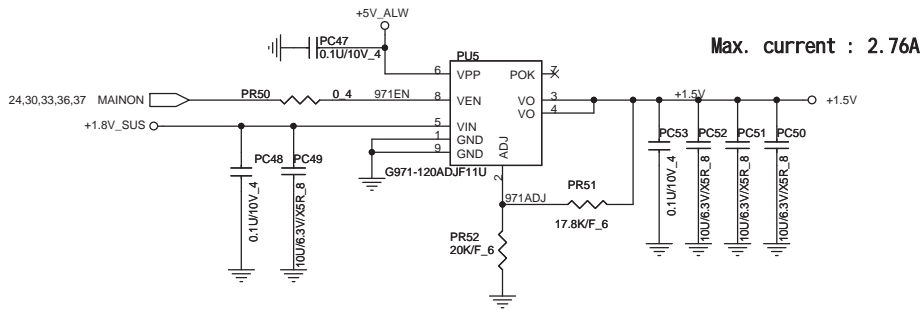
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OCP: 5A

EMI confi rm




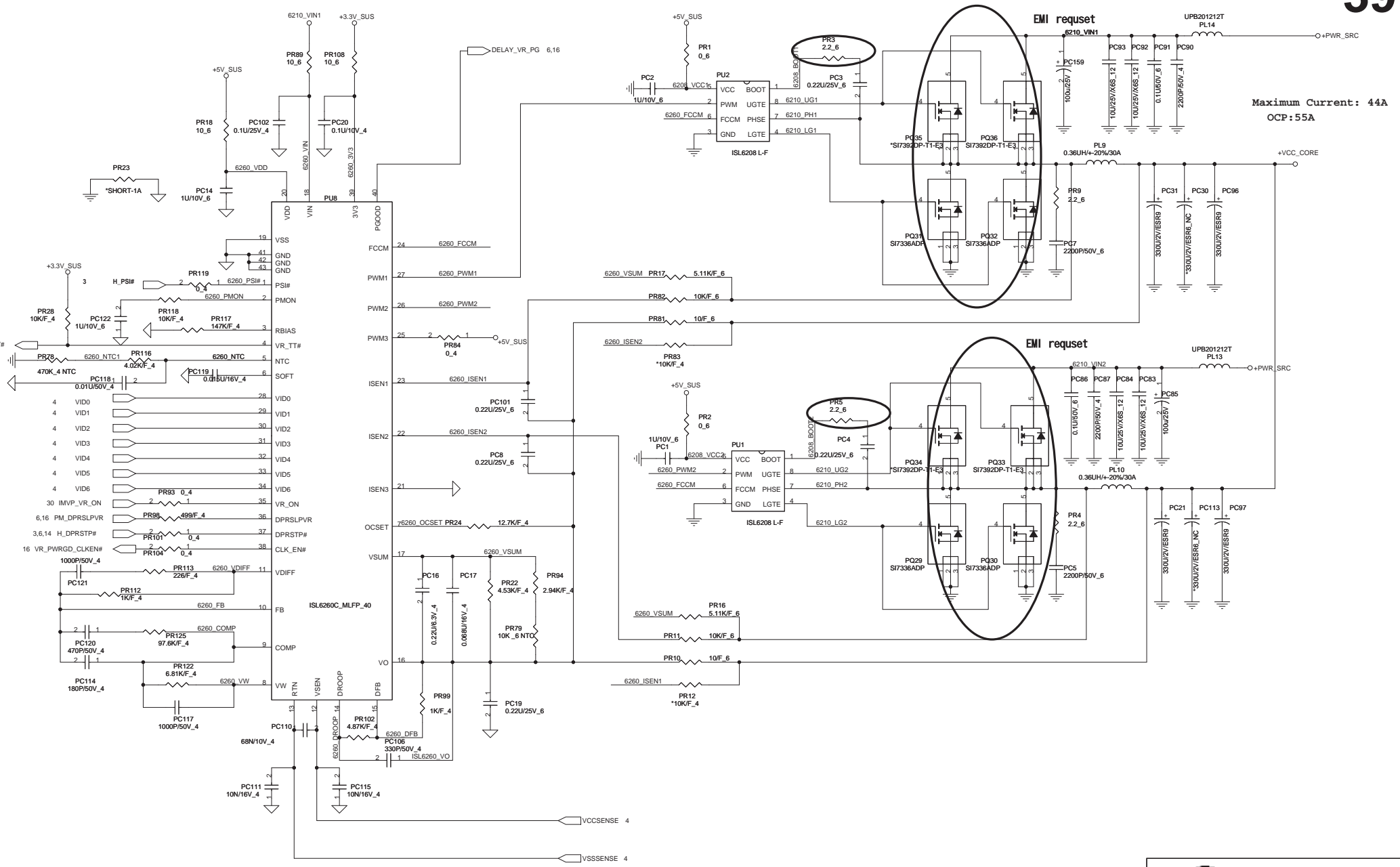
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Quanta Computer Inc.

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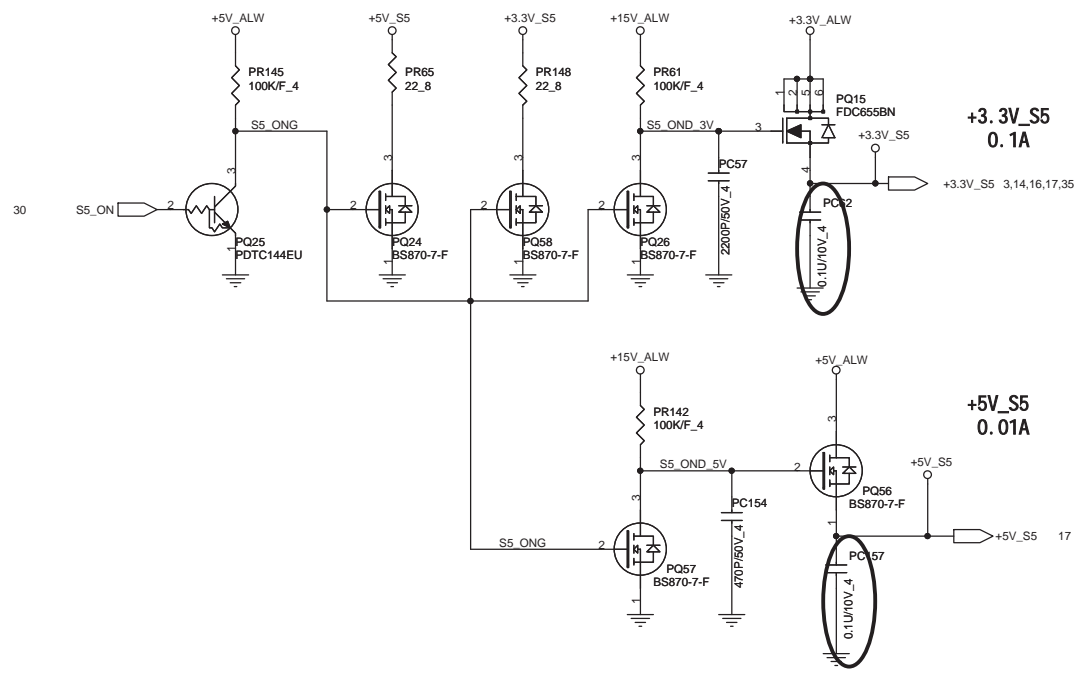
$$V_{out} = 0.8(1 + R1/R2) = 0.8(1 + 17.8K/20K) = 1.512V$$

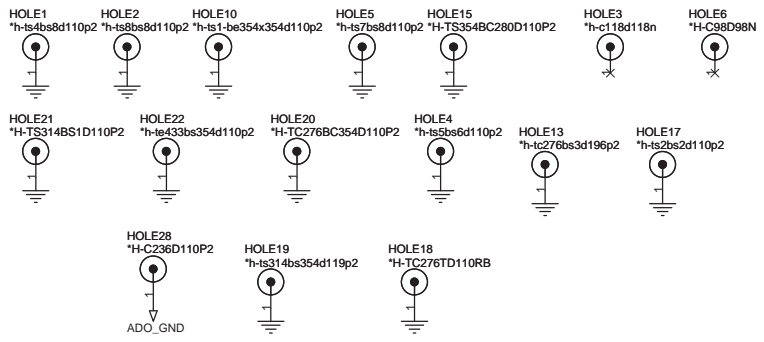
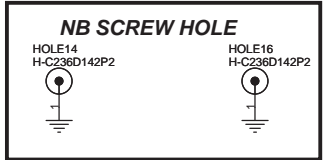
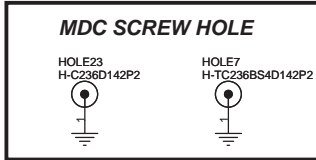
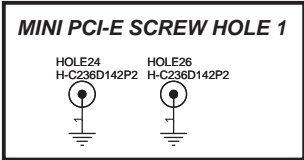
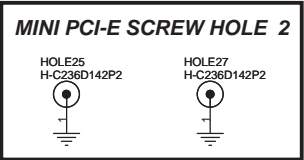
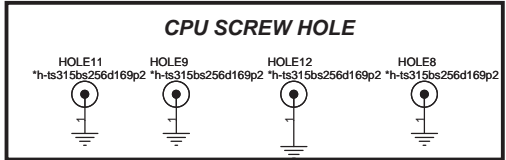
		PROJECT : SA1	
		Quanta Computer Inc.	
Size	Document Number	Rev	
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EC A-01 /28 Add EMI EC1~EC52 for EMI use
EC A-02 /18 Add EMI EC49, EC50,C582,C583 for EMI use.
EC A-03 /24 Add EMI R509,R510 for EMI use.
EC A-04 /21 CN12 Pin9 and Pin10 connect to GND
EC A-05 /23 Change All SP0~SP19 0 ohm to 33 Ohm
EC A-06 /14 Add EMI request C589~C593
EC A-07 /6 Add EMI request C594~C595
EC A-08 /24 Add R374 0 Ohm for Audio SPDIF Detec.
EC B-09 /28 Remove EB2 for EMI.
EC B-10 /19 Add R511~R514 for Fix SDVO issue
EC B-11 /30 Mount R372 R373 R379 for Volume Contral.
EC B-12 /31 Cgange D1 and D2 connect to +3.3V_LED for S3 S4 off.
EC B-13 /30 Add VHS 10K Pull-high for Wake up.
EC B-14 /18 Chnage to HALL sensor SW5, Del SW6 C588 C587.
EC B-15 /17 Change C509 from 0.1U to 1U for Loss of ODD on Vista.
EC B-16 /24 Change L20 L22 some L19 BK1608HM241-T.
EC B-17 /24 Change R503 connect to +AVDDA
EC B-18 /16 M/B ID change to 1101.
EC B-19 /24 Add R516 R517 C596 for IDT request.
EC B-20 /6 Add R518 R519 R520 to meet Intel Check list.
EC B-21 /18 Add R521 100K for meet Intel checklist.
EC B-22 /27 Add R522 R523 for ODD Pull-high
EC B-23 /18/29 Change USB3 and USB8 for S3 as mouse attach usb port near by RJ11 with FPR.
EC B-24 change C467,C470,C472,C192,C221,C222,C237,C238,C239,C240 from 0603 to 0402, and C9 C40 C58 to 10U.
EC B-25 /24 Add C576 for THD+ pass.
EC B-26 /2 Change C257,C264,C267 to 15P for meet Clock test Pass.
EC B-27 /19 Change R42 to 750 for meet HDMI .
EC B-28 /31 LED schematic follow MA8
EC B-29 /19 EMI request from 100P to 680P.
EC B-30 /23 change C301 C302 to 15P.
EC B-31 /24 EMI request Add C608~C611 R526~R530.
EC C-32 /24 Add U16 for Audio noise and SPDF issue.
EC E-33 Chnage USB C399,C403,C372,C376 Varistor to 0402 for Cost down.



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