COBHAM

GRLIB IP Core User's Manual

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1 Introduction

1.1 Scope

This document describes specific IP cores provided with the GRLIB IP library. When applicable, the cores use the GRLIP plug&play configuration method as described in the 'GRLIB User's Manual'.

1.2 Other resources

There are several documents that together describe the GRLIB IP Library and Cobham Gaisler's IP cores:

- GRLIB IP Library User's Manual (grlib.pdf) - Main GRLIB document that describes the library infrastructure, organization, tool support and on-chip bus.
- GRLIB-FT User's Manual (grlib-ft.pdf) - Describes the FT and FT-FPGA versions of the GRLIB IP library. The document is an addendum to the GRLIB IP Library User's Manual. This document is only available in the FT and FT-FPGA distributions of GRLIB.
- GRLIB FT-FPGA Xilinx Add-on User's Manual (grlib-ft-fpga-xilinx.pdf) - Describes functionality of the Virtex5-QV and Xilinx TMRTool add-on package to the FT-FPGA version of the GRLIP IP library. The document should be read as an addendum to the 'GRLIB IP Library User's Manual' and to the GRLIB FT-FPGA User's Manual. This document is only available as part of the add-on package for FT-FPGA.
- LEON/GRLIB Configuration and Development Guide (guide.pdf) - This configuration and development guide is intended to aid designers when developing systems based on LEON/GRLIB. The guide complements the GRLIB IP Library User's Manual and the GRLIB IP Core User's Manual. While the IP Library user's manual is suited for RTL designs and the IP Core user's manual is suited for instantiation and usage of specific cores, this guide aims to help designers make decisions in the specification stage.

1.3 Reference documents

[AMBA] AMBA™ Specification, Rev 2.0, ARM IHI 0011A, 1999, Issue A, ARM Limited

[GRLIB] GRLIB IP Library User's Manual, Cobham Gaisler, www.gaisler.com

[AS1553] AS15531 - Digital Time Division Command/Response Multiplex Data Bus, SAE International, November 1995

[MIL1553] MIL-STD-1553B, Digital Time Division Command/Response Multiplex Data Bus, US Department of Defence, September 1978

[MIL1553N2] MIL-STD-1553B Notice 2, US Department of Defence, September 1986

[ECSS1553] Interface and Communication Protocol for MIL-STD-1553B Data Bus Onboard Spacecraft, ECSS-E-ST-50-13C. November 2008

1.4 IP core overview

The tables below lists the provided IP cores and their AMBA plug&play device ID. The columns on the right indicate in which GRLIB distributions a core is available. GPL is the GRLIB GNU GPL (free) distribution, COM is the commercial distribution, FT the full fault-tolerant distribution and FT-FPGA is the GRLIB release targeted for raditation-tolerant programmable devices. Distributions prefixed with L4- contain the LEON4 processor. Some cores can only be licensed separately or as additions to existing releases, this is marked in the *Notes* column. Contact Cobham Gaisler for licensing details.

Note: The open-source version of GRLIB includes only cores marked with "Yes" in the GPL column.

Note: IP core FT features are only supported in FT or FT-FPGA distributions. This includes protection of Level-1 cache and register files for the LEON3 and LEON4 processors and fault-tolerance features for other IP cores such as the PCI, Ethernet and SpaceWire controllers.

Note: For encrypted RTL, contact Cobham Gaisler to ensure that your EDA tool is supported by GRLIB for encrypted RTL. Supported tools are listed in the GRLIB IP Library user's manual.

Table 1. Processors and support functions

Name	Function	Vendor:Device	GPL	COM	FT	FT-FPGA	L4-COM	L4-FT	Notes
LEON3	SPARC V8 32-bit processor	0x01 : 0x003	Yes	Yes	Yes	Yes	No	No	5)
LEON3FT	Fault-tolerant SPARC V8 32-bit Processor	0x01 : 0x053	No	No	Yes	Yes	No	No	2), 5)
DSU3	Multi-processor Debug support unit (LEON3)	0x01 : 0x004	Yes	Yes	Yes	Yes	No	No	
L3STAT	LEON3 statistics unit	0x01 : 0x098	Yes	Yes	Yes	Yes	No	No	
LEON4	SPARC V8 32-bit processor	0x01 : 0x048	No	No	No	No	Yes	No	1, 4), 5)
LEON4FT	Fault-tolerant SPARC V8 32-bit Processor	0x01 : 0x048	No	No	No	No	No	Yes	1, 4), 5)
L4STAT	LEON4 statistics unit	0x01 : 0x047	No	No	No	No	Yes	Yes	1)
DSU4	Multi-processor Debug support unit (LEON4)	0x01 : 0x049	No	No	No	No	Yes	Yes	1)
LEON3/4 CLK2x	LEON processor double clocking (includes special LEON entity, interrupt controller and qualifier unit)	-	No	Yes	Yes	Yes	Yes	Yes	
CLKGEN	Clock generation	-	Yes	Yes	Yes	Yes	Yes	Yes	
DIV32	Divider module	-	Yes	Yes	Yes	Yes	Yes	Yes	
GPTIMER	General purpose timer unit	0x01 : 0x011	Yes	Yes	Yes	Yes	Yes	Yes	
GRCLKGATE	Clock gate unit	0x01 : 0x02C	No	Yes	Yes	Yes	Yes	Yes	
GRDMAC	DMA controller with AHB/APB bridge	0x01 : 0x095	Yes	Yes	Yes	Yes	Yes	Yes	
GRTIMER	General purpose timer unit	0x01 : 0x038	No	Yes	Yes	Yes	Yes	Yes	
GRFPU / GRFPC	High-performance IEEE-754 Floating-point unit with floating-point controller to interface LEON	-	No	No	No	No	No	No	1), 2)
GRFPU-Lite / GRFPC-lite	Low-area IEEE-754 Floating-point unit with floating point controller to interface LEON	-	No	No	No	No	No	No	1), 2)
IRQMP	Multi-processor Interrupt controller	0x01 : 0x00D	Yes	Yes	Yes	Yes	Yes	Yes	
IRQ(A)MP	Multi-processor Interrupt controller	0x01 : 0x00D	Yes	Yes	Yes	Yes	Yes	Yes	
MUL32	32x32 multiplier module	-	Yes	Yes	Yes	Yes	Yes	Yes	
MULTLIB	High-performance multipliers	-	Yes	Yes	Yes	Yes	Yes	Yes	

1) Available as separate package or as addition to existing releases.
2) Delivered as encrypted RTL or in netlist format
3) Requires PHY for selected target technology. Please see IP core documentation for supported technologies.
4) Fault-tolerance (LEON4-FT functionality) is only supported in GRLIB-FT distributions.
5) The LEON3 and LEON3FT cores are functionally equivalent with the addition that fault-tolerance features can be enabled for the LEON3FT core. The functional behaviour of the LEON4 core is the same in all distributions wiht the addition that fault-tolerance features for the LEON4 core can be enabled in GRLIB FT distributions.

Table 2. Memory controllers and supporting cores

Name	Function	Vendor:Device	GPL	COM	FT	FT-FPGA	L4-COM	L4-FT	Note
DDRSPA	Single-port 16/32/64 bit DDR controller	0x01 : 0x025	Yes	Yes	Yes	Yes	Yes	Yes	3)
DDR2SPA	Single-port 16/32/64-bit DDR2 controller	0x01 : 0x02E	Yes	Yes	Yes	Yes	Yes	Yes	3)
MCTRL	8/16/32-bit PROM/SRAM/SDRAM controller	0x04 : 0x00F	Yes	Yes	Yes	Yes	Yes	Yes	
SDCTRL	32-bit PC133 SDRAM controller	0x01 : 0x009	Yes	Yes	Yes	Yes	Yes	Yes	
SRCTRL	8/32-bit PROM/SRAM controller	0x01 : 0x008	Yes	Yes	Yes	Yes	Yes	Yes	
SSRCTRL	32-bit Synchronous SRAM (SSRAM) controller	0x01 : 0x00A	No	Yes	Yes	Yes	Yes	Yes	
FTMCTRL	8//32-bit PROM/SRAM/SDRAM controller w. RS/BCH EDAC	0x01 : 0x054	No	No	Yes	Yes	No	Yes	
FTSDCTRL	32/64-bit PC133 SDRAM Controller with EDAC	0x01 : 0x055	No	No	Yes	Yes	No	Yes	
FTSDCTRL64	64-bit PC133 SDRAM controller with EDAC	0x01 : 0x058	No	No	No	No	No	No	4)
FTSRCTRL	8/32-bit PROM/SRAM/IO Controller w. BCH EDAC	0x01 : 0x051	No	No	Yes	Yes	No	Yes	
FTSRCTRL8	8-bit SRAM / 16-bit IO Memory Controller with EDAC	0x01 : 0x056	No	No	Yes	Yes	No	Yes	
NANDFCTRL	NAND Flash memory controller	0x01 : 0x059	No	Yes	Yes	Yes	Yes	Yes	
SPIMCTRL	SPI Memory controller	0x01 : 0x045	Yes	Yes	Yes	Yes	Yes	Yes	
AHBSTAT	AHB status register	0x01 : 0x052	Yes	Yes	Yes	Yes	Yes	Yes	
MEMSCRUB	Memory scrubber	0x01 : 0x057	No	No	Yes	Yes	No	Yes	

1) Available as separate package or as addition to existing releases.
2) Delivered as encrypted RTL or in netlist format
3) Requires PHY for selected target technology. Please see IP core documentation for supported technologies.
4) Deprecated

Table 3. AMBA Bus control

Name	Function	Vendor:Device	GPL	COM	FT	FT-FPGA	L4-COM	L4-FT	Note
AHB2AHB	Uni-directional AHB/AHB Bridge	0x01 : 0x020	No	Yes	Yes	Yes	Yes	Yes	
AHB2AVLA	Asynchronous AHB to Avalon Bridge	0x01 : 0x096	Yes	Yes	No	No	Yes	No	
AHB2AXI	AHB to AXI bridge	0x01 : 0x09F	Yes	Yes	Yes	Yes	Yes	Yes	
AHBBRIDGE	Bi-directional AHB/AHB Bridge	0x01 : 0x020	No	Yes	Yes	Yes	Yes	Yes	
AHBCTRL	AMBA AHB bus controller with plug&play	-	Yes	Yes	Yes	Yes	Yes	Yes	
APBCTRL	AMBA APB Bridge with plug&play	0x01 : 0x006	Yes	Yes	Yes	Yes	Yes	Yes	
AHBTRACE	AMBA AHB Trace buffer	0x01 : 0x017	Yes	Yes	Yes	Yes	Yes	Yes	
GRIOMMU	I/O Memory management unit	0x01 : 0x04F	No	No	No	No	Yes	Yes	1)

1) Available as separate package or as addition to existing releases.

Table 4. PCI interface

Name	Function	Vendor:Device	GPL	COM	FT	FT-FPGA	L4-COM	L4-FT	Note
GRPCI2	Advanced 32-bit PCI bridge	0x01 : 0x07C	Yes	Yes	Yes	Yes	Yes	Yes	
PCITARGET	32-bit target-only PCI interface (deprecated)	0x01 : 0x012	No	No	No	No	No	No	
PCIMTF/GRPCI	32-bit PCI master/target interface with FIFO (deprecated)	0x01 : 0x014	No	No	No	No	No	No	
PCITRACE	32-bit PCI trace buffer (deprecated)	0x01 : 0x015	No	No	No	No	No	No	
PCIDMA	DMA controller for PCIMTF (deprecated)	0x01 : 0x016	No	No	No	No	No	No	
PCIARB	PCI Bus arbiter	0x04 : 0x010	Yes	Yes	Yes	Yes	Yes	Yes	

Table 5. On-chip memory functions

Name	Function	Vendor:Device	GPL	COM	FT	FT-FPGA	L4-COM	L4-FT	Note
AHBRAM	Single-port RAM with AHB interface	0x01 : 0x00E	Yes	Yes	Yes	Yes	Yes	Yes	
AHBDPRAM	Dual-port RAM with AHB and user back-end interface	0x01 : 0x00F	Yes	Yes	Yes	Yes	Yes	Yes	
AHBROM	ROM generator with AHB interface	0x01 : 0x01B	Yes	Yes	Yes	Yes	Yes	Yes	
FTAHBRAM	RAM with AHB interface and EDAC protection	0x01 : 0x050	No	No	Yes	Yes	No	Yes	
L2CACHE	Level-2 cache controller	0x01 : 0x04B	No	No	No	No	Yes	Yes	1)
REGFILE_3P	Parametrizable 3-port register file	-	Yes	Yes	Yes	Yes	Yes	Yes	
SYNCRAM	Parametrizable 1-port RAM	-	Yes	Yes	Yes	Yes	Yes	Yes	
SYNCRAM_2P	Parametrizable 2-port RAM	-	Yes	Yes	Yes	Yes	Yes	Yes	
SYNCRAM_DP	Parametrizable dual-port RAM	-	Yes	Yes	Yes	Yes	Yes	Yes	

1) Available as separate package or as addition to existing releases.

Table 6. Serial communication

Name	Function	Vendor:Device	GPL	COM	FT	FT-FPGA	L4-COM	L4-FT	Note
AHBUART	Serial/AHB debug interface	0x01 : 0x007	Yes	Yes	Yes	Yes	Yes	Yes	
AHBJTAG	JTAG/AHB debug interface	0x01 : 0x01C	Yes	Yes	Yes	Yes	Yes	Yes	
APBPS2	PS/2 host controller with APB interface	0x01 : 0x060	Yes	Yes	Yes	Yes	Yes	Yes	
APBUART	Programmable UART with APB interface	0x01 : 0x00C	Yes	Yes	Yes	Yes	Yes	Yes	
CAN_OC	Opencores CAN 2.0 MAC with AHB interface	0x01 : 0x019	Yes	Yes	Yes	Yes	Yes	Yes	
GRCAN	CAN 2.0 Controller with DMA	0x01 : 0x03D	No	Yes	Yes	Yes	Yes	Yes	
GRSPW	SpaceWire link with RMAP and AHB interface	0x01 : 0x01F	No	No	No	No	No	No	1), 2)
GRSPW2	SpaceWire link with RMAP and AHB interface	0x01 : 0x029	No	No	No	No	No	No	1), 2)
GRSPW_CODEC	SpaceWire Codec	N/A	No	No	No	No	No	No	1), 2)
GRSPW_PHY	Receiver Physical layer for GRSPW	N/A	No	No	No	No	No	No	1), 2)
GRSPW2_PHY	Receiver Physical layer	N/A	No	No	No	No	No	No	1), 2)
GRSPWROUTER	SpaceWire routing switch	0x01 : 0x03E	No	No	No	No	No	No	1), 2), 3)
GRSPWTDP	SpaceWire - Time Distribution Protocol	0x01 : 0x097	No	No	No	No	No	No	1)
GRSRIO	Serial Rapid IO	0x01 : 0x0A8	No	No	No	No	No	No	1)
GRSPFI_CODEC	SpaceFibre Codec	N/A	No	No	No	No	No	No	1)
I2C2AHB	I2C (slave) to AHB bridge	0x01 : 0x00B	Yes	Yes	Yes	Yes	Yes	Yes	
I2CMST	I2C Master with APB interface	0x01 : 0x028	Yes	Yes	Yes	Yes	Yes	Yes	
I2CSLV	I2C Slave with APB interface	0x01 : 0x03E	Yes	Yes	Yes	Yes	Yes	Yes	
SPI2AHB	SPI (slave) to AHB bridge	0x01 : 0x05C	Yes	Yes	Yes	Yes	Yes	Yes	
SPICTRL	SPI Controller with APB interface	0x01 : 0x02D	Yes	Yes	Yes	Yes	Yes	Yes	
SPIMASTER	SPI master device	0x01 : 0x0A6	No	No	No	No	No	No	1)
SPISLAVE	Dual port SPI slave	0x01 : 0x0A7	No	No	No	No	No	No	1)
TAP	JTAG TAP controller	-	No	Yes	Yes	Yes	Yes	Yes	

1) Available as separate package or as addition to existing releases.
2) Delivered as encrypted RTL or in netlist format
3) The GRSPWROUTER is only licensed together with a complete LEON system.

Table 7. Ethernet interface

Name	Function	Vendor:Device	GPL	COM	FT	FT-FPGA	L4-COM	L4-FT	Note
GRETH	Cobham Gaisler 10/100 Mbit Ethernet MAC with AHB I/F	0x01 : 0x01D	Yes	Yes	Yes	Yes	Yes	Yes	
GRETH_GBIT	Cobham Gaisler 10/100/1000 Mbit Ethernet MAC with AHB	0x01 : 0x01D	No	Yes	Yes	Yes	Yes	Yes	
RGMII	Cobham Gaisler RGMII<-> GMII adapter	0x01 : 0x093	Yes	Yes	Yes	Yes	Yes	Yes	

Table 8. USB interface

Name	Function	Vendor:Device	GPL	COM	FT	FT-FPGA	L4-COM	L4-FT	Note
GRUSBHC	USB-2.0 Host controller (UHCI/EHCI) with AHB I/F	0x01 : 0x027	No	No	No	No	No	No	1)
GRUSBDC / GRUSB_DCL	USB-2.0 device controller / AHB debug communication link	0x01 : 0x022	No	No	No	No	No	No	1)

1) Available as separate package or as addition to existing releases.

Table 9. MIL-STD-1553 Bus interface

Name	Function	Device ID	GPL	COM	FT	FT-FPGA	L4-COM	L4-FT	Note
GR1553B	Advanced MIL-ST-1553B / AS15551 Interface	0x01 : 0x04D	No	No	No	No	No	No	1), 2), 3)
GRRT	MIL-STD-1553B / AS15531 Remote Terminal Back-End	-	No	No	No	No	No	No	1), 2), 3)

1) Available as separate package or as addition to existing releases.
2) Delivered as encrypted RTL or in netlist format.
3) Both BR1553B and GRRT are covered by the same IP core license and are delivered in the same package.

Table 10. Encryption

Name	Function	Vendor:Device	GPL	COM	FT	FT-FPGA	L4-COM	L4-FT	Note
GRAES	128-bit AES Encryption/Decryption Core	0x01 : 0x073	No	No	No	No	No	No	1)
GRAES_DMA	Advanced Encryption Standard with DMA	0x01 : 0x07B	No	No	No	No	No	No	1)
GRECC	Elliptic Curve Cryptography Core	0x01 : 0x074	No	No	No	No	No	No	1)

1) Available as separate package or as addition to existing releases.

Table 11. Simulation and debugging

Name	Function	Vendor:Device	GPL	COM	FT	FT-FPGA	L4-COM	L4-FT	Note
SRAM	SRAM simulation model with srecord pre-load	-	Yes	Yes	Yes	Yes	Yes	Yes	
MT48LC16M16	Micron SDRAM model with srecord pre-load	-	Yes	Yes	Yes	Yes	Yes	Yes	
MT46V16M16	Micron DDR model	-	Yes	Yes	Yes	Yes	Yes	Yes	
CY7C1354B	Cypress ZBT SSRAM model with srecord pre-load	-	Yes	Yes	Yes	Yes	Yes	Yes	
AHBMSTEM	AHB master simulation model with scripting (deprecated)	0x01 : 0x040	Yes	Yes	Yes	Yes	Yes	Yes	
AHBSLVEM	AHB slave simulation model with scripting (deprecated)	0x01 : 0x041	Yes	Yes	Yes	Yes	Yes	Yes	
AMBAMON	AHB and APB protocol monitor	-	No	Yes	Yes	Yes	Yes	Yes	
ATF	AMBA test framework consisting of master, slave and arbiter.	0x01 : 0x068 - 0x06A	No	Yes	Yes	Yes	Yes	Yes	
LOGAN	On-chip Logic Analyzer	0x01 : 0x062	Yes	Yes	Yes	Yes	Yes	Yes	

Table 12. Graphics functions

Name	Function	Vendor:Device	GPL	COM	FT	FT-FPGA	L4-COM	L4-FT	Note
APBVGA	VGA controller with APB interface	0x01 : 0x061	Yes	Yes	Yes	Yes	Yes	Yes	
SVGACTRL	VGA controller core with DMA	0x01 : 0x063	Yes	Yes	Yes	Yes	Yes	Yes	

Table 13. Auxiliary functions

Name	Function	Vendor:Device	GPL	COM	FT	FT-FPGA	L4-COM	L4-FT	Note
GRACECTRL	AMBA SystemACE interface controller	0x01 : 0x067	Yes	Yes	Yes	Yes	Yes	Yes	
GRADCDAC	Combined ADC / DAC Interface	0x01 : 0x036	No	Yes	Yes	Yes	Yes	Yes	
GRFIFO	External FIFO Interface with DMA	0x01 : 0x035	No	Yes	Yes	Yes	Yes	Yes	
GRGPIO	General purpose I/O port	0x01 : 0x01A	Yes	Yes	Yes	Yes	Yes	Yes	
GRGPREG	General purpose Register	0x01 : 0x087	Yes	Yes	Yes	Yes	Yes	Yes	
GRPULSE	General purpose I/O with pulses	0x01 : 0x037	No	Yes	Yes	Yes	Yes	Yes	
GRPWM	PWM generator	0x01 : 0x04A	No	Yes	Yes	Yes	Yes	Yes	
GRSYSMON	AMBA Wrapper for Xilinx System Monitor	0x01 : 0x066	Yes	Yes	Yes	Yes	Yes	Yes	
GRVERSION	Version and revision register	0x01 : 0x03A	Yes	Yes	Yes	Yes	Yes	Yes	

Table 14. Error detection and correction functions

Name	Function	GPL	COM	FT	FT-FPGA	L4-COM	L4-FT	Note
RS(24, 16, 8, E=1)	16 bit data, 8 check bits, corrects 4-bit error in 1 nibble	No	No	Yes	Yes	No	Yes	
RS(40, 32, 8, E=1)	32 bit data, 8 check bits, corrects 4-bit error in 1 nibble	No	No	Yes	Yes	No	Yes	
RS(48, 32, 16, E=1+1)	32 bit data, 16 check bits, corrects 4-bit error in 2 nibbles	No	No	Yes	Yes	No	Yes	
RS(48, 32, 16, E=2)	32 bit data, 16 check bits, corrects 4-bit error in 2 nibbles	No	No	Yes	Yes	No	Yes	
GR(2^4)(68, 60, 8, T=1)	QEC/QED error correction code encoder/decoder	No	No	Yes	Yes	No	Yes	

Table 15. Test functions

Name	Function	GPL	COM	FT	FT-FPGA	L4-COM	L4-FT	Note
SYNCIOTEST	Test block for synchronous I/O interfaces	Yes	Yes	Yes	Yes	Yes	Yes	

1.5 Spacecraft data handling IP cores

The Spacecraft Data Handling IP cores represent a collection of cores that have been developed specifically for the space sector.

These IP cores implement functions commonly used in spacecraft data handling and management systems. They implement international standards from organizations such as Consultative Committee for Space Data Systems (CCSDS), European Cooperation on Space Standardization (ECSS), and the former Procedures, Standards and Specifications (PSS) from the European Space Agency (ESA).

The table below lists the existing CCSDS/ECSS IP cores and AMBA plug&play device identifiers.

The columns on the right indicate in which GRLIB distributions a core is available. GPL is the GRLIB GNU GPL (free) distribution, COM is the commercial distribution, FT the full fault-tolerant distribution and FT-FPGA is the GRLIB release targeted for radiation-tolerant programmable devices. Distributions prefixed with L4- contain the LEON4 processor.

The TMTC license covers IP cores, with the upper TM and TC layers implemented in software, hardware and also cores for implementing TM and TC test equipment. It can be provided as a separate package or as an add-on to other GRLIB distributions.

Table 16. Spacecraft data handling functions

Name	Function	Vendor : Device	GPL	COM	FT	FT-FPGA	L4-COM	L4.FT	TMTC	Note
GRTM	CCSDS Telemetry Encoder	0x01 : 0x030	No	No	No	No	No	No	**Yes**	
GRTM_DESC	CCSDS Telemetry Encoder - Descriptor	0x01 : 0x084	No	No	No	No	No	No	**Yes**	
GRTM_VC	CCSDS Telemetry Encoder - Virtual Channel Generation	0x01 : 0x085	No	No	No	No	No	No	**Yes**	
GRTM_PAHB	CCSDS Telemetry Encoder - VC Generation Input - AMBA	0x01 : 0x088	No	No	No	No	No	No	**Yes**	
GRTM_PW	CCSDS Telemetry Encoder - VC Generation Input - PacketWire	N/A	No	No	No	No	No	No	**Yes**	
GRTM_UART	CCSDS Telemetry Encoder - VC Generation Input - UART	N/A	No	No	No	No	No	No	**Yes**	
GRTM_CLCWRX	CCSDS Telemetry Encoder - CLCW Receiver	N/A	No	No	No	No	No	No	**Yes**	2)
GRTM_CLCWMUX	CCSDS Telemetry Encoder - CLCW Multiplexer	N/A	No	No	No	No	No	No	**Yes**	2)
GRGEFFE	CCSDS Telemetry Encoder - Geffe Generator	0x01 : 0x086	No	No	No	No	No	No	**Yes**	
GRCE/GRCD	CCSDS Convolutional Encoder and Quicklook Decoder	N/A	No	No	No	No	No	No	**Yes**	
GRTMRX	CCSDS Telemetry Receiver	0x01 : 0x082	No	No	No	No	No	No	**Yes**	
GRTC	CCSDS Telecommand Decoder - Coding Layer	0x01 : 0x031	No	No	No	No	No	No	**Yes**	
TCAU	ESA PSS Telecommand Decoder Authentication Unit	N/A	No	No	No	No	No	No	**Yes**	
GRTC_HW	CCSDS Telecommand Decoder - Hardware Commands	N/A	No	No	No	No	No	No	**Yes**	
GRTC_UART	CCSDS Telecommand Decoder - UART	N/A	No	No	No	No	No	No	**Yes**	
GRTC_CLCWTX	CCSDS Telecommand Decoder - CLCW Transmitter	N/A	No	No	No	No	No	No	**Yes**	2)
GRTCTX	CCSDS Telecommand Transmitter	0x01 : 0x083	No	No	No	No	No	No	**Yes**	
GRCTM	CCSDS Time manager	0x01 : 0x033	No	No	No	No	No	No	**Yes**	
SPWCUC	SpaceWire - CCSDS Unsegmented Code Transfer Protocol	0x01 : 0x089	No	No	No	No	No	No	**Yes**	
GRPW	PacketWire receiver with AHB interface	0x01 : 0x032	No	No	No	No	No	No	**Yes**	
GRPWRX	PacketWire Receiver (rev 1)	0x01 : 0x03C	No	No	No	No	No	No	**Yes**	
GRPWTX	PacketWire Transmitter (rev 1)	0x01 : 0x03B	No	No	No	No	No	No	**Yes**	
APB2PW	PacketWire Transmitter Interface (rev 0)	0x01 : 0x03B	No	No	No	No	No	No	**Yes**	
PW2APB	PacketWire Receiver Interface (rev 0)	0x01 : 0x03C	No	No	No	No	No	No	**Yes**	
AHB2PP	Packet Parallel Interface	0x01 : 0x039	No	No	No	No	No	No	**Yes**	
GRRM	Reconfiguration Module	0x01 : 0x09A	No	No	No	No	No	No	No	1)

Note 1) Available as separate package or as addition to existing releases.

Note 2) There is no user manual for these simple cores.

1.6 Supported technologies

Technology support and instructions for extending GRLIB with support for additional technologies is documented in the 'GRLIB User's Manual'. The table below shows the technology maps available from Cobham Gaisler for GRLIB and in which GRLIB distributions these technology maps are included.

Vendor	Technology	GPL	COM	FT	FT-	Comment
Actel / Microsemi	ProASIC3, ProASIC3e, ProASIC3l, Axcelerator, Axcelerator DSP, Fusion, IGLOO2	No	Yes	Yes	Yes	
Actel / Microsemi	RTG4	No	No	*	*	RTG4 support is distributed as a separate add-on package.
Altera	Cyclone2 - 4, Stratix - StratixV	Yes	Yes	Yes	Yes	Note that several parts of the FT and FT-FPGA versions are distributed as encrypted RTL. Encrypted RTL is not provided for the Quartus II tool.
Lattice	-	Yes	Yes	No	No	
Xilinx	Unisim (Virtex2 - 7-series)	Yes	Yes	Yes	Yes	Xilinx Sirf (Virtex-5QV) and TMR-Tool support is distributed as a separate add-on package.
Other ASIC	-	No	-	-	No	Contact Cobham Gaisler for details. See also *GRLIB IP Library User's Manual*.

1.7 Implementation characteristics

Implementation characteristics are available in the GRLIB area spreadsheet:

http://www.gaisler.com/products/grlib/grlib_area.xls

The spreadsheet is also included in GRLIB packages together with this document.

1.8 Definitions

This section and the following subsections define the typographic and naming conventions used throughout this document.

1.8.1 Bit numbering

The following conventions are used for bit numbering:

- The most significant bit (MSb) of a data type has the leftmost position
- The least significant bit of a data type has the rightmost position
- Unless otherwise indicated, the MSb of a data type has the highest bit number and the LSb the lowest bit number

1.8.2 Radix

The following conventions is used for writing numbers:

- Binary numbers are indicated by the prefix "0b", e.g. 0b1010.
- Hexadecimal numbers are indicated by the prefix "0x", e.g. 0xF00F
- Unless a radix is explicitly declared, the number should be considered a decimal.

1.8.3 Data types

Byte (BYTE)	8 bits of data
Halfword (HWORD)	16 bits of data
Word (WORD)	32 bits of data
Double word (DWORD)	64 bits of data
Quad word (4WORD)	128-bits of data

1.9 Register descriptions

An example register, showing the register layout used throughout this document, can be seen in table 17. The values used for the reset value fields are described in table 18, and the values used for the field type fields are described in table 19. Fields that are named RESERVED, RES, or R are read-only fields. These fields can be written with zero or with the value read from the same register field.

Table 17. <Address> - <Register acronym> - <Register name>

31 24	23 16	15 8	7 0
EF3	EF2	EF1	EF0
<Reset value for EF3>	<Reset value for EF2>	<Reset value for EF1>	<Reset value for EF0>
<Field type for EF3>	<Field type for EF2>	<Field type for EF1>	<Field type for EF0>

31: 24 Example field 3 (EF3) - <Field description>
23: 16 Example field 2 (EF2) - <Field description>
15: 8 Example field 1 (EF1) - <Field description>
7: 0 Example field 0 (EF0) - <Field description>

Table 18. Reset value definitions

Value	Description
0	Reset value 0.
1	Reset value 1. Used for single-bit fields.
0xNN	Hexadecimal representation of reset value. Used for multi-bit fields.
0bNN	Binary representation of reset value. Used for multi-bit fields.
NR	Field not reset. Fields marked with NR will be reset to 0 if full reset of all registers have been enabled in the global GRLIB configuration options (see GRLIB user manual for more information).
*	Special reset condition, described in textual description of the field. Used for example when reset value is taken from a pin.
-	Don't care / Not applicable

Table 19. Field type definitions

Value	Description
r	Read-only. Writes have no effect.
w	Write-only. Used for a writable field in a register where the field's read-value has no meaning.
rw	Readable and writable.
rw*	Readable and writable. Special condition for write, described in textual description of field.
wc	Write-clear. Readable, and cleared when written with a 1
cas	Readable, and writable through compare-and-swap. Only applies to SpaceWire Plug-and-Play registers.

2 AHB2AHB - Uni-directional AHB/AHB bridge

2.1 Overview

The uni-directional AHB/AHB bridge is used to connect two AMBA AHB buses clocked by synchronous clocks with any frequency ratio. The bridge is connected through a pair consisting of an AHB slave and an AHB master interface. AHB transfer forwarding is performed in one direction, where AHB transfers to the slave interface are forwarded to the master interface. Applications of the uni-directional bridge include system partitioning, clock domain partitioning and system expansion.

Features offered by the uni-directional AHB to AHB bridge are:

- Single and burst AHB transfers
- Data buffering in internal FIFOs
- Efficient bus utilization through (optional) use of SPLIT response and data prefetching. **NOTE:** SPLIT responses require an AHB arbiter that allows assertion of HSPLIT during second cycle of SPLIT response. This is supported by GRLIB's AHBCTRL IP core.
- Posted writes
- Read and write combining, improves bus utilization and allows connecting cores with differing AMBA access size restrictions.
- Deadlock detection logic enables use of two uni-directional bridges to build a bi-directional bridge (one example is the bi-directional AHB/AHB bridge core (AHBBRIDGE))

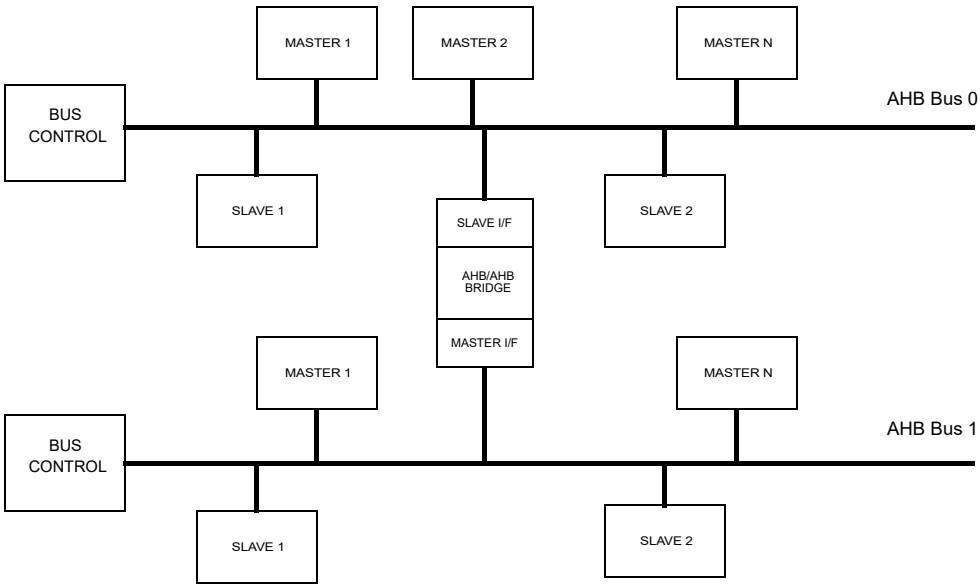


Figure 1. Two AHB buses connected with (uni-directional) AHB/AHB bridge

2.2 Operation

2.2.1 General

The address space occupied by the AHB/AHB bridge on the slave bus is configurable and determined by Bank Address Registers in the slave interface's AHB Plug&Play configuration record.

The bridge is capable of handling single and burst transfers of all burst types. Supported transfer sizes (HSIZE) are BYTE, HALF-WORD, WORD, DWORD, 4WORD and 8WORD.

For AHB write transfers write data is always buffered in an internal FIFO implementing posted writes. For AHB read transfers the bridge uses GRLIB's AMBA Plug&Play information to determine whether the read data will be prefetched and buffered in an internal FIFO. If the target address for an AHB read burst transfer is a prefetchable location the read data will be prefetched and buffered.

The bridge can be implemented to use SPLIT responses or to insert wait states when handling an access. With SPLIT responses enabled, an AHB master initiating a read transfer to the bridge is always splitted on the first transfer attempt to allow other masters to use the slave bus while the bridge performs read transfer on the master bus.The descriptions of operation in the sections below assume that the bridge has been implemented with support for AMBA SPLIT responses. The effects of disabling support for AMBA SPLIT responses are described in section 2.2.11.

If interrupt forwarding is enabled the interrupts on the slave bus interrupt lines will be forwarded to the master bus and vice versa.

2.2.2 AHB read transfers

When a read transfer is registered on the slave interface the bridge gives a SPLIT response. The master that initiated the transfer will be de-granted allowing other bus masters to use the slave bus while the bridge performs a read transfer on the master side. The master interface then requests the bus and starts the read transfer on the master side. Single transfers on the slave side are normally translated to single transfers with the same AHB address and control signals on the master side, however read combining can translate one access into several smaller accesses. Translation of burst transfers from the slave to the master side depends on the burst type, burst length, access size and the AHB/AHB bridge configuration.

If the read FIFO is enabled and the transfer is a burst transfer to a prefetchable location, the master interface will prefetch data in the internal read FIFO. If the splitted burst on the slave side was an incremental burst of unspecified length (INCR), the length of the burst is unknown. In this case the master interface performs an incremental burst up to a specified address boundary (determined by the VHDL generic *rburst)*. The bridge can be configured to recognize an INCR read burst marked as instruction fetch (indicated on HPROT signal). In this case the prefetching on the master side is completed at the end of a cache line (the cache line size is configurable through the VHDL generic *iburst*). When the burst transfer is completed on the master side, the splitted master that initiated the transfer (on the slave side) is allowed in bus arbitration by asserting the appropriate HSPLIT signal to the AHB controller. The splitted master re-attempts the transfer and the bridge will return data with zero wait states.

If the read FIFO is disabled, or the burst is to non-prefetchable area, the burst transfer on the master side is performed using sequence of NONSEQ, BUSY and SEQ transfers. The first access in the burst on the master side is of NONSEQ type. Since the master interface can not decide whether the splitted burst will continue on the slave side or not, the master bus is held by performing BUSY transfers. On the slave side the splitted master that initiated the transfer is allowed in bus arbitration by asserting the HSPLIT signal to the AHB controller. The first access in the transfer is completed by returning read data. The next access in the transfer on the slave side is extended by asserting HREADY low. On the master side the next access is started by performing a SEQ transfer (and then holding the bus using BUSY transfers). This sequence is repeated until the transfer is ended on the slave side.

In case of an ERROR response on the master side the ERROR response will be given for the same access (address) on the slave side. SPLIT and RETRY responses on the master side are re-attempted until an OKAY or ERROR response is received.

2.2.3 AHB write transfers

The AHB/AHB bridge implements posted writes. During the AHB write transfer on the slave side the data is buffered in the internal write FIFO and the transfer is completed on the slave side by always giving an OKAY response. The master interface requests the bus and performs the write transfer when the master bus is granted. If the burst transfer crosses the write burst boundary (defined by VHDL

generic *wburst*), a SPLIT response is given. When the bridge has written the contents of the FIFO out on the master side, the bridge will allow the master on the slave side to perform the remaining accesses of the write burst transfer.

Writes are accepted with zero wait states if the bridge is idle and the incoming access is not locked. If the incoming access is locked, each access will have one wait state. If write combining is disabled a non-locked BUSY cycle will lead to a flush of the write FIFO. If write combining is enabled or if the incoming access is locked, the bridge will not flush the write FIFO during the BUSY cycle.

2.2.4 Deadlock conditions

When two bridges are used to form a bi-drectional bridge, a deadlock situation can occur if the bridges are simultaneously accessed from both buses. The bridge that has been configured as a slave contains deadlock detection logic which will resolve a deadlock condition by giving a RETRY response, or by issuing SPLIT complete followed by a new SPLIT response. When the core resolves a deadlock while prefetching data, any data in the prefetch buffer will be dropped when the core's slave interface issues the AMBA RETRY response. When the access is retried it may lead to the same memory locations being read twice.

Deadlock detection logic for bi-directional configurations may lead to deadlocks in other parts of the system. Consider the case where a processor on bus A on one side of the bidirectional bridge needs to perform an instruction fetch over the bridge before it can release a semaphore located in memory on bus A. Another processor on bus B, on the other side of the bridge, may spin on the semaphore wating for its release. In this scenario, the accesses from the processor on bus B could, depending on system configuration, continuously trigger a deadlock condition where the core will drop data in, or be prevented from initiating, the instruction fetch for the processor on bus A. Due to scenarios of this kind the bridge should not be used in bi-directional configurations where dependencies as the one described above exist between the buses connected by the bridge.

Other deadlock conditions exist with locked transfers, see section 2.2.5.

2.2.5 Locked transfers

The AHB/AHB bridge supports locked transfers. The master bus will be locked when the bus is granted and remain locked until the transfer completes on the slave side. Locked transfers can lead to deadlock conditions, the core's VHDL generic *lckdac* determines if and how the deadlock conditions are resolved.

With the VHDL generic *lckdac* set to 0, locked transfers may *not* be made after another read access which received SPLIT until the first read access has received split complete. This is because the bridge will return split complete for the first access first and wait for the first master to return. This will cause deadlock since the arbiter is not allowed to change master until a locked transfer has been completed. The AMBA specification requires that the locked transfer is handled before the previous transfer, which received a SPLIT response, is completed.

With *lckdac* set to 1, the core will respond with an AMBA ERROR response to locked access that is made while an ongoing read access has received a SPLIT response. With *lckdac* set to 2 the bridge will save state for the read access that received a SPLIT response, allow the locked access to complete, and then complete the first access. All non-locked accesses from other masters will receive SPLIT responses until the saved data has been read out.

If the core is used to create a bi-directional bridge there is one more deadlock condition that may arise when locked accesses are made simultaneously in both directions. If the VHDL generic *lckdac* is set to 0 the core will deadlock. If *lckdac* is set to a non-zero value the slave bridge will resolve the deadlock condition by issuing an AMBA ERROR response to the incoming locked access.

2.2.6 Read and write combining

Read and write combining allows the bridge to assemble or split AMBA accesses on the bridge's slave interface into one or several accesses on the master interface. This functionality can improve bus utilization and also allows cores that have differing AMBA access size restrictions to communicate with each other. The functionality attained by read and write combining depends on the VHDL generics *rdcomb* (defines type of read combining), *wrcomb* (defines type of write combining), *slvmstaccsz* (defines maximum AHB access size supported by the bridge's slave interface) and *mstmaccsz* (defines maximum AHB access size that can be used by bridge's master interface). These VHDL generics are described in section 2.6. The table below shows the effect of different settings. BYTE and HALF-WORD accesses are special cases. The table does not list illegal combinations, for instance *mstmaccsz* /= *slvmaccsz* requires that *wrcomb* /= 0 and *rdcomb* /= 0.

Table 20. Read and write combining

Access on slave interface	Access size	wrcomb	rdcomb	Resulting access(es) on master interface
BYTE or HALF-WORD single read access to any area	-	-	-	Single access of same size
BYTE or HALF-WORD read burst to prefetchable area	-	-	-	Incremental read burst of same access size as on slave interface, the length is the same as the number of 32-bit words in the read buffer, but will not cross the read burst boundary.
BYTE or HALF-WORD read burst to non-prefetchable area	-	-	-	Incremental read burst of same access size as on slave interface, the length is the same as the length of the incoming burst. The master interface will insert BUSY cycles between the sequential accesses.
BYTE or HALF-WORD single write	-	-	-	Single access of same size
BYTE or HALF-WORD write burst	-	-	-	Incremental write burst of same size and length, the maximum length is the number of 32-bit words in the write FIFO.
Single read access to any area	Access size <= mstmaccsz	-	-	Single access of same size
Single read access to any area	Access size > mstmaccsz	-	1	Sequence of single accesses of mstmaccsz. Number of accesses: (access size)/mstmaccsz
Single read access to any area	Access size > mstmaccsz	-	2	Burst of accesses of size mstmaccsz. Length of burst: (access size)/mstmaccsz
Read burst to prefetchable area	-	-	0	Burst of accesses of incoming access size up to address boundary defined by rburst.
Read burst to prefetchable area	-	-	1 or 2	Burst of accesses of size mstmaccsz up to address boundary defined by rburst.
Read burst to non-prefetchable area	Access size <= mstmaccsz	-	-	Incremental read burst of same access size as on slave interface, the length is the same as the length of the incoming burst. The master interface will insert BUSY cycles between the sequential accesses.
Read burst to non-prefetchable area	Access size > mstmaccsz	-	1 or 2	Burst of accesses of size mstmaccsz. Length of burst: (incoming burst length)*(access size)/mstmaccsz
Single write	Access size <= mstmaccsz	-	-	Single write access of same size
Single write	Access size > mstmaccsz	1	-	Sequence of single access of mstmaccsz. Number of accesses: (access size)/mstmaccsz.
Single write	Access size > mstmaccsz	2	-	Burst of accesses of mstmaccsz. Length of burst: (access size)/mstmaccsz.

Table 20. Read and write combining

Access on slave interface	Access size	wrcomb	rdcomb	Resulting access(es) on master interface
Write burst	-	0	-	Burst of same size as incoming burst, up to address boundary defined by VHDL generic wburst.
Write burst	-	1 or 2	-	Burst write of maximum possible size. The bridge will use the maximum size (up to mst-maccsz) that it can use to empty the writebuffer.

Read and write combining prevents the bridge from propagating fixed length bursts and wrapping bursts. See section 2.2.7 for a discussion on burst operation.

Read and write combining with VHDL generics *wrcomb/rdcomb* set to 1 cause the bridge to use single accesses when divding an incoming access into several smaller accesses. This means that another master on the bus may write or read parts of the memory area to be accessed by the bridge before the bridge has read or written all the data. In bi-directional configurations, an incoming access on the master bridge may cause a collision that aborts the operation on the slave bridge. This may cause the bridge to read the same memory locations twice. This is normally not a problem when accessing memory areas. The same issues apply when using an AHB arbiter that performs early burst termination. The standard GRLIB AHBCTRL core does not perform early burst termination.

To ensure that the bridge does not re-read an address, and that all data in an access from the bridge's slave interface is propagated out on the master interface without interruption the VHDL generics *rdcomb* and *wrcomb* should both be set to 0 or 2. In addition to this, the AHB arbiter may not perform early burst termination (early burst termination is not performed by the GRLIB AHBCTRL arbiter).

Read and write combining can be limited to specified address ranges. See description of the *combmask* VHDL generic for more information. Note that if the core is implemented with support for prefetch and read combining, it will not obey combmask for prefetch operations (burst read to prefetchable areas). Prefetch operations will always be performed with the maximum allowed size on the master interface.

2.2.7 Burst operation

The core can be configured to support all AMBA 2.0 burst types (single access, incrementing burst of unspecified length, fixed length incrementing bursts and wrapping bursts). Single accesses and incrementing bursts of unspecified length have previously been discussed in this document. An incoming single access will lead to one access, or multiple accesses for some cases with read/write combining, on the other side of the bridge. An incoming incrementing burst of unspecified length to a prefetchable area will lead to the prefetch buffer (if available) being filled using the same access size, or the maximum allowed access size if read/write combining is enabled, on the master interface.

If the core is used in a system where no fixed length bursts or incremental bursts will be used in accesses to the bridge, then set the *allbrst* generic to 0 and skip the remainder of this section.

The VHDL generic *allbrst* controls if the core will support fixed length and wrapping burst accesses. If *allbrst* is set to 0, the core will treat all burst accesses as incrementing of unspecified length. For fixed length and wrapping bursts this can lead to performance penalties and malfunctions. Support for fixed length and wrapping bursts is enabled by setting *allbrst* to 1 or 2. Table 21 describes how the core will handle different burst types depending on the setting of *allbrst*.

Table 21. Burst handling

Value of allbrst generic	Access type*	Undefined length incrementing burst INCR	Fixed length incrementing burst INCR{4,8,16}	Wrapping burst WRAP{4,8,16}
0	Reads to non-prefetchable area	Incrementing burst with BUSY cycles inserted. Same behaviour with read and write combining.	Fixed length burst with BUSY cycles inserted. If the burst is short then the burst may end with a BUSY cycle. If access combining is used the HBURST signal will get incorrect values.	Malfunction. Not supported
	Reads to prefetchable area	Incrementing burst of maximum allowed size, filling prefetch buffer, starting at address boundary defined by prefetch buffer.		Malfunction. Not supported
	Write burst	Incrementing burst	Incrementing burst, if write combining is enabled, and triggered, the burst will be translated to an incrementing burst of undefined length. VHDL generic *wrcomb* should not be set to 1 (but to 0 or 2) in this case	Write combining is not supported. Same access size will be used on both sides of the bridge.
1	Reads to non-prefetchable area	Incrementing burst with BUSY cycles inserted. Same behaviour with read and write combining.	Same burst type with BUSY cycles inserted. If read combining is enabled, and triggered by the incoming access size, an incremental burst of unspecified length will be used. If the burst is short then the burst may end with a BUSY cycle.	Same burst type with BUSY cycles inserted. If read combining is enabled, and triggered by the incoming access size, an incremental burst of unspecified length will be used. This will cause AMBA violations if the wrapping burst does not start from offset 0.
	Reads to prefetchable area	Incrementing burst of maximum allowed size, filling prefetch buffer.	For reads, the core will perform full (or part that fits in prefetch buffer) fixed/wrapping burst on master interface and then respond with data. No BUSY cycles are inserted. If the access made to the slave interface is larger than the maximum supported access size on the master interface then a incrementing burst of unspecified length will be used to fill the prefetch buffer. This (read combining) is not supported for wrapping bursts.	
	Write burst	Same as for allbrst = 0		
2	Reads to non-prefetchable area	Incrementing burst with BUSY cycles inserted. Same behaviour with read and write combining.	Reads are treated as a prefetchable burst. See below.	
	Reads to prefetchable area	Incrementing burst of maximum allowed size, filling prefetch buffer, starting at address boundary defined by prefetch buffer.	Core will perform full (or part that fits in prefetch buffer) fixed/wrapping burst on master interface and then respond with data. No BUSY cycles are inserted. If the access made to the slave interface is larger than the maximum supported access size on the master interface then a incrementing burst of unspecified length will be used to fill the prefetch buffer. This (read combining) is not supported for wrapping bursts.	
	Write burst	Same as for allbrst = 0		

* Access to prefetchable area where the core's prefetch buffer is ised (VHDL generic pfen /= 0).

2.2.8 Transaction ordering, starvation and AMBA arbitration schemes

The bridge is configured at implementation to use one of two available schemes to handle incoming accesses. The bridge will issue SPLIT responses when it is busy and on incoming read accesses. If the bridge has been configured to use first-come, first-served ordering it will keep track of the order of incoming accesses and serve the requests in the same order. If first-come, first-served ordering is disabled the bridge will give some advantage to the master it has a response for and then allow all masters in to arbitration simultaneously, moving the decision on which master that should be allowed to access the bridge to the bus arbitration.

When designing a system containing a bridge the expected traffic patterns should be analyzed. The designer must be aware how SPLIT responses affect arbitration and how the selected transaction ordering in the bridge will affect the system. The two different schemes are further described in sections 2.2.9 and 2.2.10.

2.2.9 First-come, first-served ordering

First-come, first served ordering is used when the VHDL generic *fcfs* is non-zero.

With first-come, first-served ordering the bridge will keep track of the order of incoming accesses. The accesses will then be served in the same order. For instance, if master 0 initiates an access to the bridge, followed by master 3 and then master 5, the bridge will propagate the access from master 0 (and respond with SPLIT on a read access) and then respond with SPLIT to the other masters. When the bridge has a response for master 0, this master will be allowed in arbitration again by the bridge asserting HSPLIT. When the bridge has finished serving master 0 it will allow the next queued master in arbitration, in this case master 3. Other incoming masters will receive SPLIT responses and will not be allowed in arbitration until all previous masters have been served.

An incoming locked access will always be given precedence over any other masters in the queue.

A burst that has initiated a pre-fetch operation will receive SPLIT and be inserted last in the master queue if the burst is longer than the maximum burst length that the bridge has been configured for.

It should be noted that first-come, first-served ordering may not work well in systems where an AHB master needs to have higher priority compared to the other masters. The bridge will not prioritize any master, except for masters performing locked accesses.

2.2.10 Bus arbiter ordering

Bus arbiter ordering is used when VHDL generic *fcfs* is set to zero.

When several masters have received SPLIT and the bridge has a response for one of these masters, the master with the queued response will be allowed in to bus arbitration by the bridge asserting the corresponding HSPLIT signal. In the following clock cycle, all other masters that have received SPLIT responses will also be allowed in bus arbitration as the bridge asserts their HSPLIT signals simultaneously. By doing this the bridge defers the decision on the master to be granted next to the AHB arbiter. The bridge does not show any preference based on the order in which it issued SPLIT responses to masters, except to the master that initially started a read or write operation. Care has been taken so that the bridge shows a consistent behavior when issuing SPLIT responses. For instance, the bridge could be simplified if it could issue a SPLIT response just to be able to change state, and not initiate a new operation, to an access coming after an access that read out prefetched data. When the bridge entered its idle state it could then allow all masters in bus arbitration and resume normal operation. That solution could lead to starvation issues such as:

T0: Master 1 and Master 2 have received SPLIT responses, the bridge is prefetching data for Master 1

T1: Master 1 is allowed in bus arbitration by setting the corresponding HSPLIT

T2: Master 1 reads out prefetch data, Master 2 HSPLIT is asserted to let Master 2 in to bus arbitration

T3: Master 2 performs an access, receives SPLIT, however the bridge does not initiate an access, it just stalls in order to enter its idle state.

T4: Master 2 is allowed in to bus arbitration, Master 1 initiates an access that leads to a prefetch and Master 1 receives a SPLIT response

T5: Master 2 performs an access, receives SPLIT since the bridge is prefetching data for master 1

T6: Go back to T0

This pattern will repeat until Master 1 backs away from the bus and Master 2 is able to make an access that starts an operation over the bridge. In most systems it is unlikely that this behavior would introduce a bus lock. However, the case above could lead to an unexpectedly long time for Master 2 to complete its access. Please note that the example above is illustrative and the problem does not exist in the core as the core does not issue SPLIT responses to (non-locked) accesses in order to just change state but a similar pattern could appear as a result of decisions taken by the AHB arbiter if Master 1 is given higher priority than Master 2.

In the case of write operations the scenario is slightly different. The bridge will accept a write immediately and will not issue a SPLIT response. While the bridge is busy performing the write on the master side it will issue SPLIT responses to all incoming accesses. When the bridge has completed the write operation on the master side it will continue to issue SPLIT responses to any incoming access until there is a cycle where the bridge does not receive an access. In this cycle the bridge will assert HSPLIT for all masters that have received a SPLIT response and return to its idle state. The first master to access the bridge in the idle state will be able to start a new operation. This can lead to the following behavior:

T0: Master 1 performs a write operation, does NOT receive a SPLIT response

T1: Master 2 accesses the bridge and receives a SPLIT response

T2: The bridge now switches state to idle since the write completed and asserts HSPLIT for Master 2.

T3: Master 1 is before Master 2 in the arbitration order and we are back at T0.

In order to avoid this last pattern the bridge would have to keep track of the order in which it has issued SPLIT responses and then assert HSPLIT in the same order. This is done with first-come, first-served ordering described in section 2.2.9.

2.2.11 AMBA SPLIT support

Support for AMBA SPLIT responses is enabled/disabled through the VHDL generic *split*. SPLIT support should be enabled in most systems. The benefits of using SPLIT responses is that the bus on the bridge's slave interface side can be free while the bridge is performing an operation on the master side. This will allow other masters to access the bus and generally improve system performance. The use of SPLIT responses also allows First-come, first-served transaction ordering.

For configurations where the bridge is the only slave interface on a bus, it can be beneficial to implement the bridge without support for AMBA SPLIT responses. Removing support for SPLIT responses reduces the area used by the bridge and may also reduce the time required to perform accesses that traverse the bridge. It should be noted that building a bi-directional bridge without support for SPLIT responses will increase the risk of access collisions.

If SPLIT support is disabled the bridge will insert wait states where it would otherwise issue a SPLIT response to a master initiating an access. This means that the arbitration ordering will be left to the bus arbiter and the bridge cannot be implemented with the First-come, first-served transaction ordering scheme. The bridge will still issue RETRY responses to resolve dead lock conditions, to split up long burst and also when the bridge is busy emptying it's write buffer on the master side.

2.2.12 Core latency

The delay incurred when performing an access over the core depends on several parameters such as core configuration, the operating frequency of the AMBA buses, AMBA bus widths and memory access patterns. Table 22 below shows core behavior in a system where both AMBA buses are running at the same frequency and the core has been configured to use AMBA SPLIT responses. Table 23 further down shows core behavior in the same system without support for SPLIT responses.

Table 22. Example of single read with FFACT = 1, and SPLIT support

Clock cycle	Core slave side activity	Core master side activity
0	Discovers access and transitions from idle state	Idle
1	Slave side waits for master side, SPLIT response is given to incoming access, any new incoming accesses also receive SPLIT responses.	Discovers slave side transition. Master interface output signals are assigned.
2		If bus access is granted, perform address phase. Otherwise wait for bus grant.
3		Register read data and transition to data ready state.
4	Discovers that read data is ready, assign read data output and assign SPLIT complete	Idle
5	SPLIT complete output is HIGH	
6	Typically a wait cycle for the SPLIT:ed master to be allowed into arbitration. Core waits for master to return. Other masters receive SPLIT responses.	
7	Master has been allowed into arbitration and performs address phase. Core keeps HREADY high	
8	Access data phase. Core has returned to idle state.	

Table 23. Example of single read with FFACT = 1, without SPLIT support

Clock cycle	Core slave side activity	Core master side activity
0	Discovers access and transitions from idle state	Idle
1	Slave side waits for master side, wait states are inserted on the AMBA bus.	Discovers slave side transition. Master interface output signals are assigned.
2		Bus access is granted, perform address phase.
3		Register read data and transition to data ready state.
4	Discovers that read data is ready, assign HREADY output register and data output register.	Idle
5	HREADY is driven on AMBA bus. Core has returned to idle state	

While the transitions shown in tables 22 and 23 are simplified they give an accurate view of the core delay. If the master interface needs to wait for a bus grant or if the read operation receives wait states, these cycles must be added to to the cycle count in the tables. The behavior of the core with a fre-

quency factor of two between the buses is shown in tables 24 and 25 (best case, delay may be larger depending on on which slave clock cycle an access is made to the core).

Table 24. Example of single read with FFACT = 2, Master freq. > Slave freq, without SPLIT support

Slave side clock cycle	Core slave side activity	Master side clock cycle	Core master side activity
0	Discovers access and transitions from idle state	0	Discovers slave side transition. Master interface output signals are assigned.
1	Slave side waits for master side, wait states are inserted on the AMBA bus.		
2		1	Bus access is granted, perform address phase.
3			
4		2	Register read data and transition to data ready state.
5			
6	Discovers that read data is ready, assign HREADY output register and data output register.	3	Idle
7	HREADY is driven on AMBA bus. Core has returned to idle state		

Table 25. Example of single read with FFACT = 2, Master freq. > Slave freq, without SPLIT support

Slave side clock cycle	Core slave side activity	Master side clock cycle	Core master side activity
0	Discovers access and transitions from idle state	0	Idle
		1	
1	Slave side waits for master side, wait states are inserted on the AMBA bus.	2	Discovers slave side transition. Master interface output signals are assigned.
		3	Bus access is granted, perform address phase.
2	Discovers that read data is ready, assign HREADY output register and data output register.	4	Register read data and transition to data ready state.
		5	Idle
3	HREADY is driven on AMBA bus. Core has returned to idle state	6	
		7	

Table 26 below lists the delays incurred for single operations that traverse the bridge while the bridge is in its idle state. The second column shows the number of cycles it takes the master side to perform the requested access, this column assumes that the master slave gets access to the bus immediately and that each access is completed with zero wait states. The table only includes the delay incurred by traversing the core. For instance, when the access initiating master reads the core's prefetch buffer, each additional read will consume one clock cycle. However, this delay would also have been present if the master accessed any other slave.

Write accesses are accepted with zero wait states if the bridge is idle, this means that performing a write to the idle core does not incur any extra latency. However, the core must complete the write operation on the master side before it can handle a new access on the slave side. If the core has not transitioned into its idle state, pending the completion of an earlier access, the delay suffered by an access be longer than what is shown in the tables in this section. Accesses may also suffer increased delays during collisions when the core has been instantiated to form a bi-directional bridge. Locked accesses that abort on-going read operations will also mean additional delays.

If the core has been implemented to use AMBA SPLIT responses there will be an additional delay where, typically, one cycle is required for the arbiter to react to the assertion of HSPLIT and one clock cycle for the repetition of the address phase.

Note that if the core has support for read and/or write combining, the number of cycles required for the master will change depending on the access size and length of the incoming burst access. For instance, in a system where the bus in the core's master side is wider than the bus on the slave side, write combining will allow the core to accept writes with zero wait states and then combine several accesses into one or several larger access. Depending on memory controller implementation this could reduce the time required to move data to external memory, and will reduce the load on the master side bus.

Table 26. Access latencies

Access	Master acc. cycles	Slave cycles	Delay incurred by performing access over core
Single read	3	1	1 * clk_{slv} + 3 * clk_{mst}
Burst read with prefetch	2 + (burst length)[x]	2	2 * clk_{slv} + (2 + burst length)* clk_{mst}
Single write[xx]	(2)	0	0
Burst write[xx]	(2 + (burst length))	0	0

[x] A prefetch operation ends at the address boundary defined by the prefetch buffer's size

[xx] The core implements posted writes, the number of cycles taken by the master side can only affect the next access.

2.2.13 Endianness

The core is designed for big-endian systems.

2.3 Registers

The core does not implement any registers.

2.4 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x020. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

2.5 Implementation

2.5.1 Technology mapping

The uni-directional AHB to AHB bridge has two technology mapping generics *memtech* and fcfsmtech. *memtech* selects which memory technology that will be used to implement the FIFO memories. *fcfsmtech* selects the memory technology to be used to implement the First-come, first-served buffer, if FCFS is enaled.

2.5.2 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support *grlib_async_reset_enable*. All registers that react on the reset signal will have a synchronous reset.

2.5.3 RAM usage

The uni-directional AHB to AHB bridge instantiates one or several *syncram_2p* blocks from the technology mapping library (TECHMAP). If prefetching is enabled max(*mstmaccsz*, *slvaccsz*)/32 *syncram_2p* block(s) with organization (max*(rburst,iburst*)-max(*mstmaccsz*, *slvaccsz*)/32) x 32 is used to implement read FIFO (max*(rburst,iburst*) is the size of the read FIFO in 32-bit words). max(*mstmaccsz*, *slvaccsz*)/32 *syncram_2p* block(s) with organization *(wburst* - max(*mstmaccsz*, *slvaccsz*)/32) x 32, is always used to implement the write FIFO (where *wburst* is the size of the write FIFO in 32-bit words).

If the core has support for first-come, first-served ordering then one *fcfs* x 4 *syncram_2p* block will be instantiated, using the technology specified by the VHDL generic *fcfsmtech*.

2.6 Configuration options

Table 27 shows the configuration options of the core (VHDL generics).

Table 27. Configuration options (VHDL generics)

Generic	Function	Allowed range	Default
memtech	Memory technology		
hsindex	Slave I/F AHB index	0 to NAHBMAX-1	0
hmindex	Master I/F AHB index	0 to NAHBMAX-1	0
dir	0 - clock frequency on the master bus is lower than or equal to the frequency on the slave bus 1 - clock frequency on the master bus is higher than or equal to the frequency on the slave bus (for VHDL generic *ffact* = 1 the value of dir does not matter)	0 - 1	0
ffact	Frequency scaling factor between AHB clocks on master and slave buses.	1 - 15	2
slv	Slave bridge. Used in bi-directional bridge configuration where *slv* is set to 0 for master bridge and 1 for slave bridge. When a deadlock condition is detected slave bridge (*slv*=1) will give RETRY response to current access, effectively resolving the deadlock situation. This generic must only be set to 1 for a bridge where the frequency of the bus connecting the master interface is higher or equal to the frequency of the AHB bus connecting to the bridge's slave interface. Otherwise a race condition during access collisions may cause the bridge to deadlock.	0 - 1	0
pfen	Prefetch enable. Enables read FIFO.	0 - 1	0
irqsync	Interrupt forwarding. Forward interrupts from slave interface to master interface and vice versa. 0 - no interrupt forwarding, 1 - forward interrupts 1 - 15, 2 - forward interrupts 0 - 31. 3 - forward interrupts 0 - 31. Since interrupts are forwarded in both directions, interrupt forwarding should be enabled for one bridge only in a bi-directional AHB/AHB bridge.	0 - 3	0
wburst	Length of write bursts in 32-bit words. Determines write FIFO size and write burst address boundary. If the wburst generic is set to 2 the bridge will not perform write bursts over a 2x4=8 byte boundary. This generic must be set so that the buffer can contain two of the maximum sized accesses that the bridge can handle.	2 - 32	8

Table 27. Configuration options (VHDL generics)

Generic	Function	Allowed range	Default
iburst	Instruction fetch burst length. This value is only used if the generic *ibrsten* is set to 1. Determines the length of prefetching instruction read bursts on the master side. The maximum of (iburst,rburst) determines the size of the core's read buffer FIFO.	4 - 8	8
rburst	Incremental read burst length. Determines the maximum length of incremental read burst of unspecified length (INCR) on the master interface. The maximum of *rburst* and *iburst* determine the read burst boundary. As an example, if the maximum value of these generics is 8 the bridge will not perform read bursts over a 8x4=32 byte boundary. This generic must be set so that the buffer can contain two of the maximum sized accesses that the bridge can handle. For systems where AHB masters perform fixed length burst (INCRx , WRAPx) *rburst* should not be less than the length of the longest fixed length burst.	4 - 32	8
bar0	Address area 0 decoded by the bridge's slave interface. Appears as memory address register (BAR0) on the slave interface. The generic has the same bit layout as bank address registers with bits [19:18] suppressed (use functions ahb2ahb_membar and ahb2ahb_iobar in gaisler.misc package to generate this generic).	0 - 1073741823	0
bar1	Address area 1 (BAR1)	0 - 1073741823	0
bar2	Address area 2 (BAR2)	0 - 1073741823	0
bar3	Address area 3 (BAR2)	0 - 1073741823	0
sbus	The number of the AHB bus to which the slave interface is connected. The value appears in bits [1:0] of the user-defined register 0 in the slave interface configuration record and master configuration record.	0-3	0
mbus	The number of the AHB bus to which the master interface is connected. The value appears in bits [3:2] of the user-defined register 0 in the slave interface configuration record and master configuration record.	0-3	0
ioarea	Address of the I/O area containing the configuration area for AHB bus connected to the bridge's master interface. This address appears in the bridge's slave interface user-defined register 1. In order for a master on the slave interface's bus to access the configuration area on the bus connected to the bridge's master interface, the I/O area must be mapped on one of the bridge's BARs. If this generic is set to 0, some tools, such as Cobham Gaisler's GRMON debug monitor, will not perform Plug'n'Play scanning over the bridge.	0 - 16#FFF#	0
ibrsten	Instruction fetch burst enable. If set, the bridge will perform bursts of *iburst* length for opcode access (HPROT[0] = '0'), otherwise bursts of *rburst* length will be used for both data and opcode accesses.	0 - 1	0

Table 27. Configuration options (VHDL generics)

Generic	Function	Allowed range	Default
lckdac	Locked access error detection and correction. Locked accesses may lead to deadlock if a locked access is made while an ongoing read access has received a SPLIT response. The value of *lckdac* determines how the core handles this scenario: 0: Core will deadlock 1: Core will issue an AMBA ERROR response to the locked access 2: Core will allow both accesses to complete. If the core is used to create a bidirectional bridge, a deadlock condition may arise when locked accesses are made simultaneously in both directions. With *lckdac* set to 0 the core will deadlock. With *lckdac* set to a non-zero value the slave bridge will issue an ERROR response to the incoming locked access.	0 - 2	0
slvmaccsz	The maximum size of accesses that will be made to the bridge's slave interface. This value must equal *mstmaccsz* unless *rdcomb* /= 0 and *wrcomb* /= 0.	32 - 256	32
mstmaccsz	The maximum size of accesses that will be performed by the bridge's master interface. This value must equal *mstmaccsz* unless *rdcomb* /= 0 and *wrcomb* /= 0.	32 - 256	32
rdcomb	Read combining. If this generic is set to a non-zero value the core will use the master interface's maximum AHB access size when prefetching data and allow data to be read out using any other access size supported by the slave interface. If slvmaccsz > 32 and mstmaccsz > 32 and an incoming single access, or access to a non-prefetchable area, is larger than the size supported by the master interface the bridge will perform a series of small accesses in order to fetch all the data. If this generic is set to 2 the core will use a burst of small fetches. If this generic is set to 1 the bridge will not use a burst unless the incoming access was a burst. Read combining is only supported for single accesses and incremental bursts of unspecified length.	0 - 2	0
wrcomb	Write combining. If this generic is set to a non-zero value the core may assemble several small write accesses (that are part of a burst) into one or more larger accesses or assemble one or more accesses into several smaller accesses. The settings are as follows: 0: No write combining 1: Combine if burst can be preserved 2: Combine if burst can be preserved and allow single accesses to be converted to bursts (only applicable if slvmaccsz > 32) Only supported for single accesses and incremental bursts of unspecified length	0 - 2	0

Table 27. Configuration options (VHDL generics)

Generic	Function	Allowed range	Default
combmask	Read/write combining mask. This generic determines which ranges that the core can perform read/write combining to (only available when rdcomb respectively wrcomb are non-zero). The value given for combmask is treated as a 16-bit vector with LSB bit (right-most) indicating address 0x0 - 0x10000000. Making an access to an address in an area marked as '0' in combmask is equivalent to making an access over a bridge with rdcomb = 0 and wrcomb = 0. However, combmask is not taken into account when the core performs a prefetch operation (see pfen generic). When a prefetch operation is initiated, the core will always use the maximum supported access size (when rdcomb /= 0).	0 - 16#FFFF#	16#FFFF#
allbrst	Support all burst types 2: Support all types of burst and always prefetch for wrapping and fixed length bursts. 1: Support all types of bursts 0: Only support incremental bursts of unspecified length See section 2.2.7 for more information. When allbrst is enabled, the core's read buffer (size set via rburst/iburst generics) must have at least 16 slots.	0 - 2	0
ifctrlen	Interface control enable. When this generic is set to 1 the input signals *ifctrl.mstifen* and *ifctrl.slvifen* can be used to force the AMBA slave respectively master interface into an idle state. This functionality is intended to be used when the clock of one interface has been gated-off and any stimuli on one side of the bridge should not be propagated to the interface on the other side of the bridge. When this generic is set to 0, the ifctrl.* input signals are unused.	0 - 1	0
fcfs	First-come, first-served operation. When this generic is set to a non-zero value, the core will keep track of the order of incoming accesses and handle the requests in the same order. If this generic is set to zero the bridge will not preserve the order and leave this up to bus arbitration. If FCFS is enabled the value of this generic must be higher or equal to the number of masters that may perform accesses over the bridge.	0 - NAHBMST	0
fcfsmtech	Memory technology to use for FCFS buffer. When VHDL generic *fcfs* is set to a non-zero value, the core will instantiate a 4 bit x *fcfs* buffer to keep track of the incoming master indexes. This generic decides the memory technology to use for the buffer.	0 - NTECH	0 (inferred)
scantest	Enable scan support	0 - 1	0
split	Use AMBA SPLIT responses. When this generic is set to 1 the core will issue AMBA SPLIT responses. When this generic is set to 0 the core will insert waitstates instead and may also issue AMBA RETRY responses. If this generic is set to 0, the *fcfs* generic must also be set to 0, otherwise a simulation failure will be asserted.	0 - 1	1

Table 27. Configuration options (VHDL generics)

Generic	Function	Allowed range	Default
pipe	This setting controls the insertion of pipeline registers between the master and slave side of the bridge. *pipe* set to 0 does not include any extra pipeline registers and the incurred delays for accesses over the bridge is as described in this documentation. *pipe* set to 1 includes extra registers on all signals between the master and slave side. *pipe* set to 2 includes pipeline registers on all signals going from the slave interface to the master interface and does NOT insert extra registers on signals going from the master interface to the slave interface. *pipe* set to 3 includes pipeline registers on all signals going from the master interface to the slave interface and does NOT insert extra registers on signals going from the slave interface to the master interface. *pipe* set to 128 includes signals on a subset of the signals to prevent direct paths from the slave clock to the master side bus and from the master clock to the slave side bus.	0, 1, 128	

2.7 Signal descriptions

Table 28 shows the interface signals of the core (VHDL ports).

Table 28. Signal descriptions (VHDL ports)

Signal name	Field	Type	Function	Active
RST		Input	Reset	Low
HCLKM		Input	AHB master bus clock	-
HCLKS		Input	AHB slave bus clock	-
AHBSI	*	Input	AHB slave input signals	-
AHBSO	*	Output	AHB slave output signals	-
AHBMI	*	Input	AHB master input signals	-
AHBMO	*	Output	AHB master output signals	-
AHBSO2	*	Input	AHB slave input vector signals (on master i/f side). Used to decode cachability and prefetch-ability Plug&Play information on bus connected to the bridge's master interface.	-
LCKI	slck blck mlck	Input	Used in systems with multiple AHB/AHB bridges (e.g. bi-directional AHB/AHB bridge) to detect deadlock conditions. Tie to "000" in systems with only uni-directional AHB/AHB bus.	High
LCKO	slck blck mlck	Output	Indicates possible deadlock condition	High
IFCTRL	mstifen	Input	Enable master interface. This input signal is unused if the VHDL generic *ifctrlen* is 0. If VHDL generic *ifctrlen* is 1 this signal must be set to '1' in order to enable the core's AMBA master interface, otherwise the master interface will always be idle and will not respond to stimuli on the core's AMBA slave interface. This signal is intended to be used to keep the core's master interface in a good state when the core's slave interface clock has been gated off. Care should be taken to ensure that the bridge is idle when the master interface is disabled.	High
	slvifen	Input	Enable slave interface. This input signal is unused if the VHDL generic *ifctrlen* is 0. If VHDL generic *ifctrlen* is 1 this signal must be set to '1' in order to enable the core's AMBA slave interface, otherwise the interface will always be ready and the bridge will not propagate stimuli on the core's AMBA slave interface to the core's AMBA master interface. This signal is intended to be used to keep the slave interface in a good state when the core's master interface clock has been gated off. Care should be taken to ensure that the bridge is idle when the slave interface is disabled.	High

* see GRLIB IP Library User's Manual

2.8 Library dependencies

Table 29 shows the libraries used when instantiating the core (VHDL libraries).

Table 29. Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	MISC	Component	Component declaration

2.9 Instantiation

GRLIB contains two example designs with AHB2AHB and LEON processors: *designs/leon3-ahb2ahb* (only available in commercial distributions) and *designs/leon4-ahb2ahb* (only in distributions that include LEON4 processor). The LEON/GRLIB Configuration and Development Guide contains more information on how to use the bridge to create multi-bus systems.

3 AHBM2AXI - AHB Master to AXI Adapter

3.1 Overview

The AHBM2AXI adapter allows a single AHB master to be used as an AXI3 or AXI4 master. The adapter has an AHB slave interface on the AHB side and AXI3 or AXI4 master interface on the AXI side (see Fig. 2). The adapter has optional read prefetching and write buffering features in order to improve the latency of burst operations. The adapter is not compatible with AHB2AHB and GRD-MAC components which is a part of GRLIB IP library.

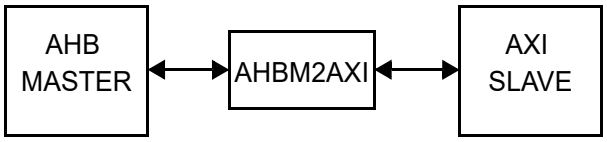


Figure 2. A standalone AHB master is connected to an AXI slave through AHBM2AXI adapter

3.1.1 AHB support

The AHBM2AXI adapter currently supports the following features of the AHB protocol:

Transfer Type: IDLE, NONSEQ, SEQ

Burst Operation: SINGLE, INCR, INCR4, INCR8, INCR16

Data-width: 32-bit, 64-bit, 128-bit, 256-bit

Transfer Size: All possible transfer sizes up to the selected data-width are supported.

Response: AXI read and write error responses are translated to AHB read and write errors.

Unsupported AHB Features:

The following features of AHB protocol are not supported by the AHBM2AXI adapter.

- BUSY transfer type : Behavior of the AHBM2AXI adapter is unpredictable when a BUSY transaction is received hence the AHBM2AXI adapter can not be used with the AHB2AHB bridge which is a part of GRLIB IP library.
- Locked transfers : Locked transfers are ignored by the AHBM2AXI adapter.

Unused AHB Features:

- RETRY and SPLIT responses : The adapter does not generate these response types.

3.2 Special Considerations

There is a combinatorial path between the incoming HTRANS signal and outgoing HREADY signal on the AHB side of the adapter, in order to allow write-buffering and write response propagation at the same time. As a result, this component is only intended to connect to a single IP core with an AHB master interface in which HTRANS output does not depend on the incoming HREADY signal combinatorially. Propagating the write response correctly is important to make sure that the intended transaction ordering has been met, meaning the AHB master that is connected to the adapter receives the acknowledgment for the last write beat in the burst when the write response has been received on the

AXI side. Being able to propagate correct write response can also simplify the software development. The AHBM2AXI adapter can not be used with the GRDMAC IP core which is a part of GRLIB IP library.

3.3 Operation

3.3.1 Read Prefetching and Write Buffering

The adapter has the feature of read prefetching and write buffering for the AHB bursts in which the transfer size (HSIZE) is equal to the selected data-width. For the transfer sizes that are narrower than the data-width each beat in the burst treated as a single transaction on the AXI side. Read prefetching and write buffering reduces the latency of undefined length burst operations since otherwise each beat in an undefined length burst has to be treated as an independent AXI transaction with a length of one.

3.3.2 Read Prefetching

Read prefetch number that is set through *rprefetch_num* generic determines the length of the AXI transaction(s) that is generated when an undefined length AHB read burst is encountered. When an undefined length AHB read burst is encountered, an AXI transaction is generated with a length of *rprefetch_num*. If the AHB read burst has less beats than *rprefetch_num* then dummy reads are generated on the AXI side to complete the AXI transaction. If the AHB read burst has more beats than *rprefetch_num* then a new AXI transaction is generated with a number of beats equal to *rprefetch_num* and this scheme continuous until the AHB burst ends. If the start address of a burst is not aligned to the prefetch boundary then the initial prefetch has less number of beats in order to align the upcoming prefetches. For example given a 32-bit (4 Byte) data-width and a *rprefetch_num* of 16 (16*4=64 Bytes) if the least significant bits of the initial burst address corresponds to byte 48, then the initial prefetch length is 4 ((64-48)/4). This way the upcoming prefetches are always aligned to 64 Byte boundary. If a new AHB burst is encountered during dummy read operations on the AXI side, the AHB burst is stalled until the current AXI transaction ends.

The maximum read prefetch number depends on the AXI protocol. For AXI3 the maximum number is 16, and for AXI4 it can be up to 256 depending on the selected data-width. Prefetch length can only be a power of two and if it is not set to be a power of two then the number is floored to the closest power of two automatically. For fixed length AHB bursts (single, INCR4, INCR8, INCR16) the length of the AXI burst is equal to the AHB burst length since in those cases the burst length is known at the beginning of the burst. The adapter will not issue a new AXI transaction while dummy cycles are inserted hence there is a trade-off for performance when selecting the read prefetch number.

3.3.3 Write Buffering

Write buffering gathers a number of consecutive beats in a AHB write burst and initiates an AXI transaction. A generic called *wbuffer_num* determines the maximum number of AHB write burst beats that will be gathered before an AXI write burst transaction is generated. If the number of beats in the AHB write burst is less than *wbuffer_num* then the AXI write transaction starts after detecting the last beat in the burst (transition from SEQ to IDLE). If the number of beats are higher than *wbuffer_num* then the first AXI transaction is generated once *wbuffer_num* number of beats are buffered. It should be noted that once an AXI write transaction is generated and AHB burst still continues then AXI transaction and buffering for the next write batch happens in parallel to minimize the latency. This scheme continuous until the AHB burst is ended. When the last data beat of the burst is reached the HREADY on the AHB side is asserted once the write response is received from the AXI side. The write buffering feature is used for the fixed size burst also in the same way as undefined length bursts.

Write buffer length can only be a power of two, and if it is not set to be a power of two then the number is floored to the closest power of two automatically. The maximum number has the same constraints as the read prefetch number. A synchronous memory width one read and write port is generated for write buffering. The size of the memory is determined by the write buffer length. The type of the memory can be configured with a generic also. The first AXI write transaction will not start until the buffer is filled or the AHB transaction has written the last beat in the burst. As a result there is a trade-off for performance while selecting the write buffer length which depends on the AXI slave behavior.

3.3.4 Endianness

The AHB side of the AHB2AXIB bridge is always assumed to be big-endian. The endianness on the AXI side is configurable through the *endianness_mode* generic.

When *endianness_mode* generic is set to zero a byte-invariant big-endian endianness mode is used on the AXI side. In order to translate big-endian AHB to byte-invariant big-endian AXI the byte order is reversed (see Fig. 3). No address translation occurs inside the adapter in this mode.

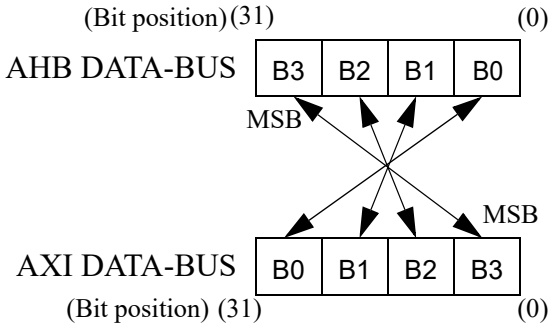


Figure 3. Big-endian AHB to byte-invariant Big-endian AXI translation (32-bit data-width)

When *endianness_mode* generic is set to one then big-endian AHB is translated to little-endian AXI. In order to achieve this the byte order is preserved but the address is translated from big-endian representation to little-endian representation when a narrow sized transaction is encountered (See Fig. 4 for an example with 32-bit data-bus width.).

The address translation formula for 32-bit, 64-bit, 128-bit and 256-bit data-bus widths are following:

32-bit data bus width:

if *HSIZE* < “010” :

axi_address(1:0) = (“100” - “1”<<“*HSIZE*” - ahb_address(1:0))(1:0)

otherwise:

axi_address(1:0) = ahb_address(1:0)

64-bit data bus width:

if *HSIZE* < “011” :

axi_address(2:0) = (“1000” - “1”<<“*HSIZE*” - ahb_address(2:0))(2:0)

otherwise:

axi_address(2:0) = ahb_address(2:0)

128-bit data bus width:

if *HSIZE* < “100” :

axi_address(3:0) = (“10000” - “1”<<“*HSIZE*” - ahb_address(3:0))(3:0)

otherwise:

axi_address(3:0) = ahb_address(3:0)

256-bit data bus width:

if *HSIZE* < “101” :

axi_address(4:0) = (“100000” - “1”<<“*HSIZE*” - ahb_address(4:0))(4:0)

otherwise:

axi_address(4:0) = ahb_address(4:0)

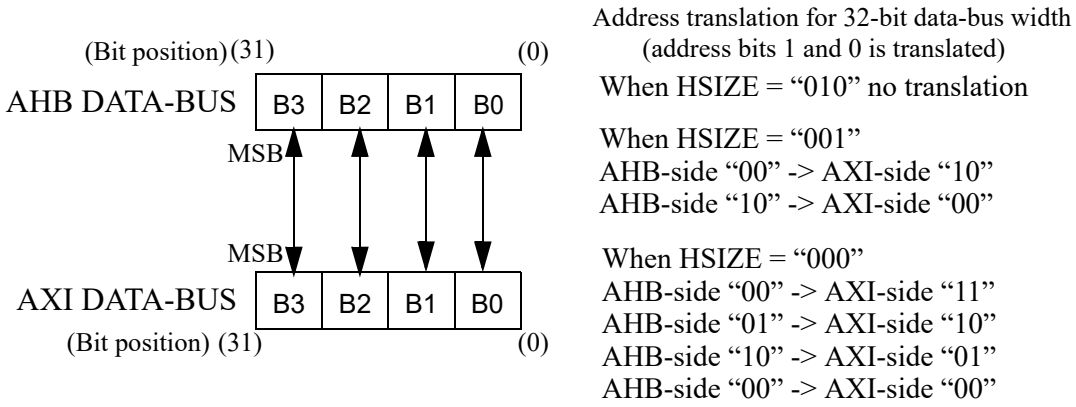


Figure 4. Big-endian AHB to little-endian AXI through address translation (32-bit data-width)

3.4 AXI AxPROT and AxCACHE Translations

The AxPROT and AxCACHE signals are translated partly according to the HPROT signal of AHB transactions. The full list of translation can be seen from Table 30.

Table 30. AxPROT and AxCACHE translations

AXI signal	Assignment
AxCACHE[3]	always logic ‘0’
AxCACHE[2]	always logic ‘0’
AxCACHE[1]	HPROT[3]
AxCACHE[0]	HPROT[2]
AxPROT[2]	not (HPROT[0])
AxPROT[1]	See configuration options (Table. 31)
AxPROT[0]	HPROT[1]

3.5 Configuration Options

Table 31. Configuration options (both AHBM2AXI3 and AHBM2AXI4)

Generic	Function	Allowed range	Default
memtech	Memory technology		
aximid	AXI master ID used for Read and Write transactions	0 - 15	0
always_secure	When set to 1 the AxPROT[1] bit is tied to logic '0' (always secure access), when set to 0 the AxPROT[1] bit is tied to logic '1' (always unsecure access).	0-1	1
endianness_mode	Determines the endianness mode (see section 3.3.4 for more detail) 0 -> Big-endian AHB to byte-invariant big-endian AXI 1 -> Big-endian AHB to little-endian AXI	0-1	0

Table 32. Configuration options specific for AXI3 (AHBM2AXI3)

Generic	Function	Allowed range	Default
wbuffer_num	Write-buffer length which determines the memory size also.	1-16	8
rprefetch_num	Read prefetch length.	1-16	8

Table 33. Configuration options specific for AXI4 (AHBM2AXI4)

Generic	Function	Allowed range	Default
wbuffer_num	Write-buffer length which determines the memory size also.	1-256 for data-width of 32-bit, 1-128 for data-width of 64-bit 1-64 for data-width of 128-bit 1-32 for data-width of 256-bit	8
rprefetch_num	Read prefetch length.	1-256 for data-width of 32-bit, 1-128 for data-width of 64-bit 1-64 for data-width of 128-bit 1-32 for data-width of 256-bit	8

3.6 Signal descriptions

Table 34 shows the interface signals of the core (VHDL ports).

Table 34. Signal descriptions (VHDL ports)

Signal name	Field	Type	Function	Active
RST		Input	Reset	Low
CLK		Input	AHB & AXI bus clock	-
AHBSI	*	Input	AHB slave input signals	-
AHBSO	*	Output	AHB slave output signals	-
AXIMI	*	Input	AXI3/4 master input signals	-
AXIMO	*	Output	AXI3/4 master output signals	-

* see GRLIB IP Library User's Manual

3.7 Library dependencies

Table 35 shows the libraries used when instantiating the core (VHDL libraries).

Table 35. Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA & AXI signal definitions
GAISLER	AXI	Component	Component declaration

3.8 Instantiation

The instantiation of the AHBM2AXI adapter depends on the AXI protocol type. There are two components called AHBM2AXI3 which is built for AXI3 protocl and AHBM2AXI4 which is built for AXI4 protocol. The difference between these two components are the AXI master output signals and the maximum values that can be set for read prefetching and write buffering.

Since AHBM2AXI adapter is intended to be used for only a single core, a transaction is sampled and evaluated directly on the rising edge of the clock, the "*hsel*" and "*hready*" inputs are ignored by the AHBM2AXI adapter. The grant signal for the AHB master that is connected to the adapter should be hardwired to logic 1.

Following is an example in which a component with an ahb master interface called "*ahbm_ex*" is connected to the AHBM2AXI4 adapter which can act as an master for AXI4 protocol.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.axi.all;


entity ahbm2axi4_ex is
  port (
    rstn  : in  std_logic;
```

```
    clk   : in  std_logic;
    aximi : in  axi_somi_type;
    aximo : out axi4_mosi_type
  );
end;


architecture rtl of ahbm2axi4_ex is


signal  ahbsi : in  ahb_slave_in_type;
signal  ahbso : out ahb_slave_out_type;
signal  ahbmi : in  ahb_mst_in_type;
signal  ahbmo : out ahb_mst_out_type;

component ahbm_ex is
 port (
 signal rstn   : in std_logic;
 signal clk    : in std_logic;
 signal ahbmi  : in ahb_mst_in_type;
 signal ahbmo  : out ahb_mst_out_type);
end component;


begin

adapter:ahbm2axi4
generic map (
 memtech => 0,
 aximid => 0,
 wbuffer_num => 16,
 rprefetch_num=> 16,
 always_secure => 1
)
port map (
 rstn => rstn,
 clk => clk,
 ahbsi => ahbsi,
 ahbso => ahbso,
 aximi => aximi,
 aximo => aximo);

ahbmaster:ahbm_ex
port map (
 rstn => rstn,
 clk => clk,
 ahbmi => ahbmi,
 ahbmo => ahbmo);


ahbsi.haddr  <= ahbmo.hadddr;
ahbsi.hwrite <= ahbmo.hwrite;
ahbsi.htrans <= ahbmo.htrans;
ahbsi.hsize  <= ahbmo.hsize;
ahbsi.hburst <= ahbmo.hburst;
ahbsi.hwdata <= ahbmo.hwdata;
ahbsi.hprot  <= ahbmo.hprot;

ahbmi.hgrant <= (others=> '1');
ahbmi.hready <= ahbso.hready;
ahbmi.hresp <= ahbso.hresp;
ahbmi.hrdata <= ahbso.hrdata;
--Remaining ahb master inputs are implementation dependent
```

4 AHB2AXIB - AHB to AXI Bridge

4.1 Overview

The AHB2AXIB bridge allows to access an AXI3 or AXI4 slave from an AHB bus through an AHB slave interface (see Fig. 5). It can also be used to connect a standalone AHB master to an AXI slave (see Fig. 6). The bridge has an AHB slave interface on the AHB side and AXI3 or AXI4 master interface on the AXI side. The bridge has optional read prefetching and write buffering features in order to improve the latency of burst operations. The AHB2AXIB bridge is not compatible with the AHB2AHB bridge which is a part of GRLIB IP library.

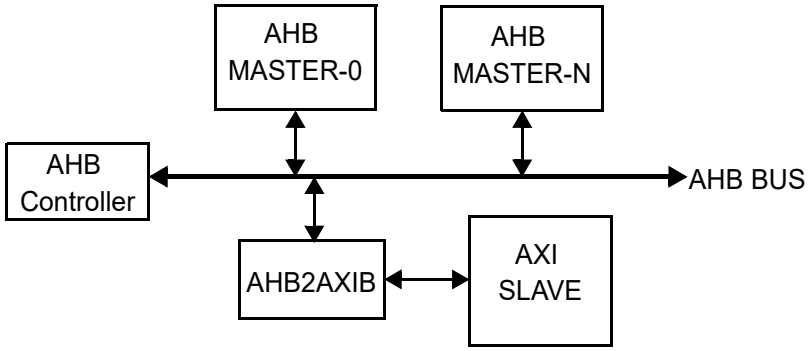


Figure 5. An AXI slave connected to the AHB bus through AHB2AXIB bridge

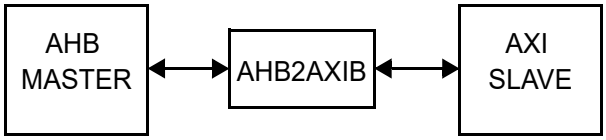


Figure 6. A standalone AHB master is connected to an AXI slave through AHB2AXIB bridge

4.1.1 AHB support

The AHB2AXIB bridge currently supports the following features of the AHB protocol:

Transfer Type: IDLE, NONSEQ, SEQ

Burst Operation: SINGLE, INCR, INCR4, INCR8, INCR16

Data-width: 32-bit, 64-bit, 128-bit, 256-bit

Transfer Size: All possible transfer sizes up to the selected data-width are supported.

Response: AXI read error response is translated to AHB read error.

Unsupported AHB Features:

The following features of AHB protocol are not supported by the AHB2AXIB bridge.

- BUSY transfer type : Behavior of the AHB2AXIB bridge is unpredictable when a BUSY transaction is received hence the AHB2AXIB bridge can not be used with the AHB2AHB bridge which is a part of GRLIB IP library.
- Locked transfers : Locked transfers are ignored by the AHB2AXIB bridge.

Unused AHB Features:

- RETRY and SPLIT responses ; AHB2AXIB bridge does not generate these response types.
- Write error response : Due to the difference between the write error handling of AXI and AHB protocol the write errors received from the AXI side is not propagated.

4.2 Operation

4.2.1 Read Prefetching and Write Buffering and Postponed Writes

The bridge has the feature of read prefetching and write buffering for the AHB bursts in which the transfer size (HSIZE) is equal to the selected data-width. For the transfer sizes that are narrower than the data-width it can still support read prefetching and write buffering if byte invariant big endian mode is used. Otherwise each beat in the burst treated as a single transaction on the AXI side. Read prefetching and write buffering reduces the latency of undefined length burst operations since otherwise each beat in an undefined length burst has to be treated as an independent AXI transaction with a length of one.

4.2.2 Read Prefetching

Read prefetch number that is set through *rprefetch_num* generic determines the length of the AXI transaction(s) that is generated when an undefined length AHB read burst is encountered. When an undefined length AHB read burst is encountered, an AXI transaction is generated with a length of *rprefetch_num*. If the AHB read burst has less beats than *rprefetch_num* then dummy reads are generated on the AXI side to complete the AXI transaction. If the AHB read burst has more beats than *rprefetch_num* then a new AXI transaction is generated with a number of beats equal to *rprefetch_num* and this scheme continuous until the AHB burst ends. If the start address of a burst is not aligned to the prefetch boundary then the initial prefetch has less number of beats in order to align the upcoming prefetches. For example given a 32-bit (4 Byte) data-width and a *rprefetch_num* of 16 (16*4=64 Bytes) if the least significant bits of the initial burst address corresponds to byte 48, then the initial prefetch length is 4 ((64-48)/4). This way the upcoming prefetches are always aligned to 64 Byte boundary. If a new AHB burst is encountered during dummy read operations on the AXI side, the AHB burst is stalled until the current AXI transaction ends.

The maximum read prefetch number depends on the AXI protocol. For AXI3 the maximum number is 16, and for AXI4 it can be up to 256 depending on the selected data-width. Prefetch length can only be a power of two and if it is not set to be a power of two then the number is floored to the closest power of two automatically. For fixed length AHB bursts (single, INCR4, INCR8, INCR16) the length of the AXI burst is equal to the AHB burst length since in those cases the burst length is known at the beginning of the burst. The bridge will not issue a new AXI transaction while dummy cycles are inserted hence there is a trade-off for performance when selecting the read prefetch number.

4.2.3 Write Buffering

Write buffering gathers a number of consecutive beats in a AHB write burst and initiates an AXI transaction. A generic called *wbuffer_num* determines the maximum number of AHB write burst beats that will be gathered before an AXI write burst transaction is generated. If the number of beats

in the AHB write burst is less than *wbuffer_num* then the AXI write transaction starts after detecting the last beat in the burst (transition from SEQ to IDLE). If the number of beats are higher than *wbuffer_num* then the first AXI transaction is generated once *wbuffer_num* number of beats are buffered. It should be noted that once an AXI write transaction is generated and AHB write burst still continues then AXI transaction and buffering of the next write batch happens in parallel to improve the latency. This scheme continuous until the AHB burst is ended. The last data beat in the burst is always acknowledged with OKAY response immediately when it is buffered in the bridge. See section 4.2.5 for more detailed information.

Write buffer length can only be a power of two, and if it is not set to be a power of two then the number is floored to the closest power of two automatically. The maximum number has the same constraints as the read prefetch number. A synchronous memory width one read and write port is generated for write buffering. The size of the memory is determined by the write buffer length. The type of the memory can be configured with a generic also. The first AXI write transaction will not start until the buffer is filled or the AHB transaction has written the last beat in the burst. As a result there is a trade-off for performance while selecting the write buffer length which depends on the AXI slave behavior.

4.2.4 Narrow Sized Transactions

When an AHB transaction is encountered which has a narrower size (HSIZE) than the data-width of the AHB2AXIB bridge, the behavior is configurable through the generics depending on the selected endianness on the AXI side. When the endianness mode on the AXI side is set as little-endian than each beat in the narrow sized AXI transaction is treated as single transaction on the AXI side. When the endinness mode on the AXI side is set as byte invariant big-endian than the *narrow_acc_mode* generic determines the behaviour. If the *narrow_acc_mode* generic is set as zero than each beat in the narrow sized AXI transaction is treated as single transaction on the AXI side. If it is set to 1 then a corresponding narrow sized AXI burst is generated with read prefetching and write buffering. But it should be noted that the length of the narrow sized burst will be determined by *rprefetch_num* and *wbuffer_num* generics and it is same as for all access sizes. When the endianness on the AXI side is set ass little-endian then *narrow_acc_mode* generic must be set to zero. See sec. 4.2.6 for more detailed information about endianness modes.

4.2.5 Postponed Writes

Since the write response from AXI is not propagated to AHB side the last beat in the AHB write transaction is acknowledged immediately when it is buffered in the bridge. Hence the corresponding AXI write transaction will finish after the AHB write transaction is completed. The transaction order on the AHB bus side will be preserved because the bridge will block an AHB read, if there is an AXI write transaction is ongoing, until the AXI write response is received. But if a transaction order has to be preserved between the AHB side of a AHB2AXIB bridge and an independent AXI master that accesses to the same AXI slave then special considerations in software might be needed. If the AHB2AXIB bridge is intended to be used for a single AHB master without an AHB bus then it is possible to use the AHBM2AXI adapter that is a part of GRLIB IP library if the AHB master is compatible. The AHBM2AXI adapter propagates the AXI write response.

4.2.6 Endianness

The AHB side of the AHB2AXIB bridge is always assumed to be big-endian. The endianness on the AXI side is configurable through the *endianness_mode* generic.

When *endianness_mode* generic is set to zero a byte-invariant big-endian endianness mode is used on the AXI side. In order to translate big-endian AHB to byte-invariant big-endian AXI the byte order is reversed (see Fig. 7). No address translation occurs inside the adapter in this mode.

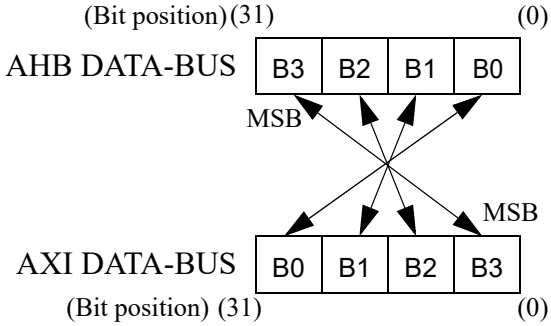


Figure 7. Big-endian AHB to byte-invariant Big-endian AXI translation (32-bit data-width)

When *endianness_mode* generic is set to one then big-endian AHB is translated to little-endian AXI. In order to achieve this the byte order is preserved but the address is translated from big-endian representation to little-endian representation when a narrow sized transaction is encountered (See Fig. 8 for an example with 32-bit data-bus width.).

The address translation formula for 32-bit, 64-bit, 128-bit and 256-bit data-bus widths are following:

32-bit data bus width:

if *HSIZE* < “010” :

axi_address(1:0) = (“100” - “1”<<“*HSIZE*” - ahb_address(1:0))(1:0)

otherwise:

axi_address(1:0) = ahb_address(1:0)

64-bit data bus width:

if *HSIZE* < “011” :

axi_address(2:0) = (“1000” - “1”<<“*HSIZE*” - ahb_address(2:0))(2:0)

otherwise:

axi_address(2:0) = ahb_address(2:0)

128-bit data bus width:

if *HSIZE* < “100” :

axi_address(3:0) = (“10000” - “1”<<“*HSIZE*” - ahb_address(3:0))(3:0)

otherwise:

axi_address(3:0) = ahb_address(3:0)

256-bit data bus width:

if *HSIZE* < “101” :

axi_address(4:0) = (“100000” - “1”<<“*HSIZE*” - ahb_address(4:0))(4:0)

otherwise:

axi_address(4:0) = ahb_address(4:0)

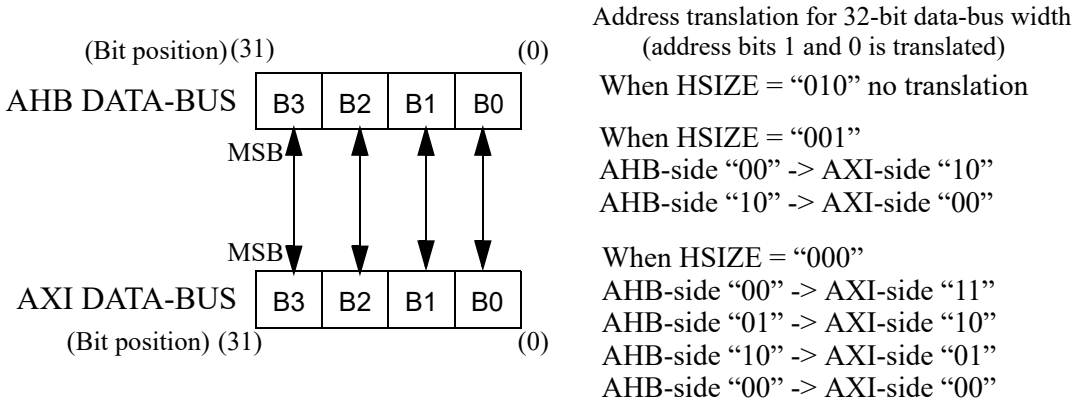


Figure 8. Big-endian AHB to little-endian AXI through address translation (32-bit data-width)

4.3 AXI AxPROT and AxCACHE Translations

The AxPROT and AxCACHE signals are translated partly according to the HPROT signal of AHB transactions. The full list of translation can be seen from Table 36.

Table 36. AxPROT and AxCACHE translations

AXI signal	Assignment
AxCACHE[3]	always logic ‘0’
AxCACHE[2]	always logic ‘0’
AxCACHE[1]	HPROT[3]
AxCACHE[0]	HPROT[2]
AxPROT[2]	not (HPROT[0])
AxPROT[1]	See configuration options (Table. 37)
AxPROT[0]	HPROT[1]

4.4 Configuration Options

Table 37. Configuration options (both AHB2AXI3B and AHB2AXI4B)

Generic	Function	Allowed range	Default
memtech	Memory technology		
aximid	AXI master ID used for Read and Write transactions	0 - 15	0
always_secure	When set to 1 the AxPROT[1] bit is tied to logic '0' (always secure access), when set to 0 the AxPROT[1] bit is tied to logic '1' (always unsecure access).	0-1	1
endianness_mode	Determines the endianness mode (see section 4.2.6 for more detail) 0 -> Big-endian AHB to byte-invariant big-endian AXI 1 -> Big-endian AHB to little-endian AXI	0-1	0
narrow_acc_mode	Determines if bursts with narrow access size than the data-bus width should be directly translated to narrow access size AXI bursts or single AXI transactions with narrow access size. (see section 4.2.4 for more detail) 0-> Each beat in the narrow sized AHB burst is treated as single transaction on the AXI side. 1-> Narrow sized AHB bursts are translated to narrow sized AXI bursts. (supported only when *endianness_mode* generic is 0) **Note:** This generic must be set to 0 if *endianness_mode* is set to 1.	0-1	0
vendor	GRLIB plug&play vendor ID		GAISLER
device	GRLIB plug&play device ID		AHB2AXI
bar0	Address area 0 decoded by the bridge's slave interface. Appears as memory address register (BAR0) on the slave interface. The generic has the same bit layout as bank address registers with bits [19:18] suppressed (use functions ahb2ahb_membar and ahb2ahb_iobar in gaisler.misc package to generate this generic).	0 - 1073741823	0
bar1	Address area 1 (BAR1)	0 - 1073741823	0
bar2	Address area 2 (BAR2)	0 - 1073741823	0
bar3	Address area 3 (BAR2)	0 - 1073741823	0

Table 38. Configuration options specific for AXI3 (AHB2AXI3B)

Generic	Function	Allowed range	Default
wbuffer_num	Write-buffer length which determines the memory size also.	1-16	8
rprefetch_num	Read prefetch length.	1-16	8

Table 39. Configuration options specific for AXI4 (AHB2AXI4B)

Generic	Function	Allowed range	Default
wbuffer_num	Write-buffer length which determines the memory size also.	1-256 for data-width of 32-bit, 1-128 for data-width of 64-bit 1-64 for data-width of 128-bit 1-32 for data-width of 256-bit	8
rprefetch_num	Read prefetch length.	1-256 for data-width of 32-bit, 1-128 for data-width of 64-bit 1-64 for data-width of 128-bit 1-32 for data-width of 256-bit	8

4.5 Signal descriptions

Table 40 shows the interface signals of the core (VHDL ports).

Table 40. Signal descriptions (VHDL ports)

Signal name	Field	Type	Function	Active
RST		Input	Reset	Low
CLK		Input	AHB & AXI bus clock	-
AHBSI	*	Input	AHB slave input signals	-
AHBSO	*	Output	AHB slave output signals	-
AXIMI	*	Input	AXI3/4 master input signals	-
AXIMO	*	Output	AXI3/4 master output signals	-

* see GRLIB IP Library User's Manual

4.6 Library dependencies

Table 41 shows the libraries used when instantiating the core (VHDL libraries).

Table 41. Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA & AXI signal definitions
GAISLER	AXI	Component	Component declaration

4.7 Instantiation

The instantiation of the AHB2AXIB bridge depends on the AXI protocol type. There are two components called AHB2AXI3B which is built for AXI3 protocol and AHB2AXI4B which is built for AXI4 protocol. The difference between these two components are the AXI master output signals and the maximum values that can be set for read prefetching and write buffering.

4.7.1 AHB2AXIB bridge is used to connect an AXI slave to an AHB bus

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.axi.all;


entity ahb2axib_ex is
  port (
    rstn  : in  std_logic;
    clk   : in  std_logic;
    .
    .
    .
    aximi : in  axi_somi_type;
    aximo : out axi4_mosi_type;
);
end;


architecture rtl of ahb2axib_ex is
.
.
constant hindex_ahb2axi4b : integer := 2;

begin


.
.
ahbctrl & other components
.
.


bridge:ahb2axi4b
generic map (
 hindex => hindex_ahb2axi4b,
 aximid => 0
)
port map (
 rstn => rstn,
 clk => clk,
 ahbsi => ahbsi,
 ahbso => ahbso(hindex_ahb2axi4b),
 aximi => aximi,
 aximo => aximo);
```

4.7.2 AHB2AXIB bridge is used to connect a standalone AHB master to an AXI slave.

If AHB2AXIB bridge is intended to be used to connect a standalone AHB master to an AXI slave then the following assignments are needed for correct operations:

The *hsel* input of the AHB2AXIB must be assigned to an array of (others=>'1') so that it works regardless of the assigned *hindex* value.

The *hready* input of the AHB2AXIB must be connected to the *hready* output of the AHB2AXIB.

The *hgrant* input of the AHB master must be assigned to an array of (others=>'1') so that it works regardless of the assigned *hindex* value.

5 AHBBRIDGE - Bi-directional AHB/AHB bridge

5.1 Overview

A pair of uni-directional bridges (AHB2AHB) can be instantiated to form a bi-directional bridge. The bi-directional AHB/AHB bridge (AHBBRIDGE) instantiates two uni-directional bridges that are configured to suit the bus architecture shown in figure 9. The bus architecture consists of two AHB buses: a high-speed AHB bus hosting LEON3 CPU(s) and an external memory controller and a low-speed AHB bus hosting communication IP-cores.

Note: For other architectures, a more general bi-directional bridge that is more suitable can be created by instantiating two uni-directional AHB to AHB bridges (see AHB2AHB core). AHBBRIDGE is not suitable for LEON4 systems and for other systems with wide AHB buses.

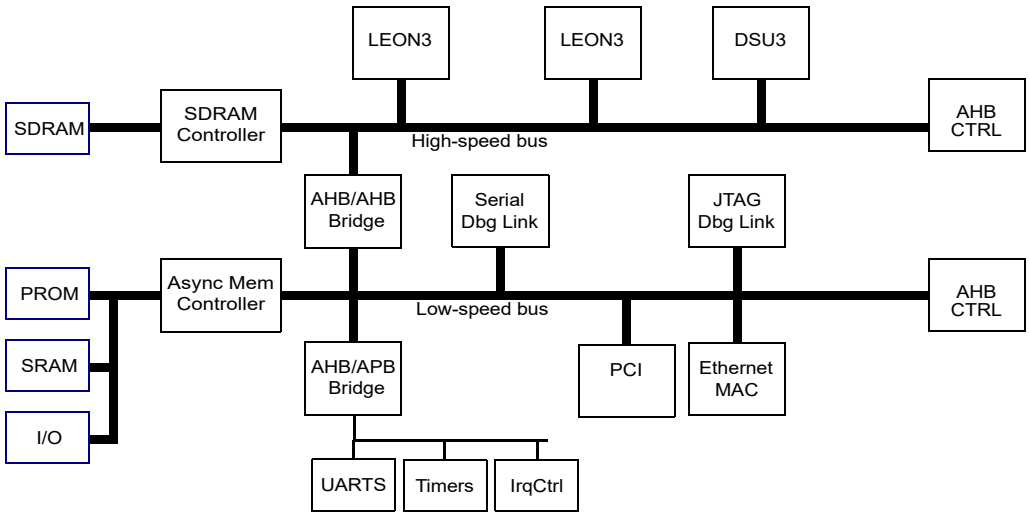


Figure 9. LEON3 system with a bi-directional AHB/AHB bridge

5.2 Operation

5.2.1 General

The AHB/AHB bridge is connected to each AHB bus through a pair consisting of an AHB master and an AHB slave interface. The address space occupied by the AHB/AHB bridge on each bus is determined by Bank Address Registers which are configured through VHDL generics. The bridge is capable of handling single and burst transfers in both directions. Internal FIFOs are used for data buffering. The bridge implements the AMBA SPLIT response to improve AHB bus utilization. For more information on AHB transfers please refer to the documentation for the uni-directional AHB/AHB bridge (AHB2AHB).

The requirements on the two bus clocks are that they are synchronous. The two uni-directional bridges forming the bi-directional AHB/AHB bridge are configured asymmetrically. Configuration of the bridge connecting high-speed bus with the low-speed bus (down bus) is optimized for the bus traffic generated by the LEON3 CPU since the CPU is the only master on the high-speed bus (except for the bridge itself). Read transfers generated by the CPU are single read transfers generated by single load instructions (LD), read bursts of length two generated by double load instructions (LDD) or incremental read bursts of maximal length equal to cache line size (4 or 8 words) generated during instruction cache line fill. The size of the read FIFO for the down bridge is therefore configurable to 4 or 8 entries which is the maximal read burst length. If a read burst is an instruction fetch (indicated on AHB HPROT signal) to a prefetchable area the bridge will prefetch data to the end of a instruction

cache line. If a read burst to a prefetchable area is a data access, two words will be prefetched (this transfer is generated by the LDD instruction). The write FIFO has two entries capable of buffering the longest write burst (generated by the STD instruction). The down bridge also performs interrupt forwarding, interrupt lines 1-15 on both buses are monitored and an interrupt on one bus is forwarded to the other one.

Since the low-speed bus does not host a LEON3 CPU, all AHB transfers forwarded by the uni-directional bridge connecting the low-speed bus and the high-speed bus (up bridge) are data transfers. Therefore the bridge does not make a distinction between instruction and data transfers. The size of the read and write FIFOs for this bridge is configurable and should be set by the user to suite burst transfers generated by the cores on the low-speed bus.

Note that the bridge has been optimized for a LEON3 system with a specific set of masters and a specific bus topology. Therefore the core may not be suitable for a design containing later versions of the LEON processor or other masters. In general it is not recommended instantiate the AHBBRIDGE core and instead instantiate two uni-directional AHB to AHB bridges (AHB2AHB cores) with configurations tailored for a specific design.

5.2.2 Deadlock conditions

A deadlock situation can occur if the bridge is simultaneously accessed from both buses. The bridge contains deadlock detection logic which will resolve a deadlock condition by giving a RETRY response on the low-speed bus.

There are several deadlock conditions that can occur with locked accesses. If the VHDL generic *lckdac* is 0, the bridge will deadlock if two simultaneous accesses from both buses are locked, or if a locked access is made while the bridge has issued a SPLIT response to a read access and the splitted access has not completed. If *lckdac* is greater than 0, the bridge will resolve the deadlock condition from two simultaneous locked accesses by giving an ERROR response on the low-speed bus. If *lckdac* is 1 and a locked access is made while the bridge has issued a SPLIT response to a read access, the bridge will respond with ERROR to the incoming locked access. If *lckdac* is 2 the bridge will allow both the locked access and the splitted read access to complete. Note that with *lckdac* set to 2 and two incoming locked accesses, the access on the low-speed bus will still receive an ERROR response.

5.2.3 Read and write combining

The bridge can be configured to support read and write combining so that prefetch operations and write bursts are always performed with the maximum access size possible on the master interface. Please see the documentation for the uni-directional AHB/AHB bridge (AHB2AHB) for a description of read and write combining and note that the same VHDL generics are used to specify both the maximum master and maximum slave access size on the bi-directional AHB/AHB bridge.

5.2.4 Endianness

The core is designed for big-endian systems

5.3 Registers

The core does not implement any registers.

5.4 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x020. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

5.5 Implementation

See documentation for AHB2AHB.

5.6 Configuration options

Table 42 shows the configuration options of the core (VHDL generics).

Table 42. Configuration options

Generic	Function	Allowed range	Default
memtech	Memory technology	-	0
ffact	Frequency ratio	1 -	2
hsb_hsindex	AHB slave index on the high-speed bus	0 to NAHBMAX-1	0
hsb_hmindex	AHB master index on the high-speed bus	0 to NAHBMAX-1	0
hsb_iclsize	Cache line size (in number of 32-bit words) for CPUs on the high-speed bus. Determines the number of the words that are prefetched by the bridge when CPU performs instruction bursts.	4, 8	8
hsb_bank0	Address area 0 mapped on the high-speed bus and decoded by the bridge's slave interface on the low-speed bus. Appears as memory address register (BAR0) on the bridge's low-speed bus slave interface. The generic has the same bit layout as bank address registers with bits [19:18] suppressed (use functions ahb2ahb_membar and ahb2ahb_iobar in gaisler.misc package to generate this generic).	0 - 1073741823	0
hsb_bank1	Address area 1 mapped on the high-speed bus	0 - 1073741823	0
hsb_bank2	Address area 2 mapped on the high-speed bus	0 - 1073741823	0
hsb_bank3	Address area 3 mapped on the high-speed bus	0 - 1073741823	0
hsb_ioarea	Address of high-speed bus I/O area that contains the high-speed bus configuration area. Will appear in the bridge's user-defined register 1 on the low-speed bus. Note that to allow low-speed bus masters to read the high-speed bus configuration area, the area must be mapped on one of the *hsb_bank* generics.	0 - 16#FFF#	0
lsb_hsindex	AHB slave index on the low-speed bus	0 to NAHBMAX-1	0
lsb_hmindex	AHB master index on the low-speed bus	0 to NAHBMAX-1	0
lsb_rburst	Size of the prefetch buffer for read transfers initiated on the low-speed-bus and crossing the bridge.	16, 32	16
lsb_wburst	Size of the write buffer for write transfers initiated on the low-speed bus and crossing the bridge.	16, 32	16
lsb_bank0	Address area 0 mapped on the low-speed bus and decoded by the bridge's slave interface on the high-speed bus. Appears as memory address register (BAR0) on the bridge's high-speed bus slave interface. The generic has the same bit layout as bank address registers with bits [19:18] suppressed (use functions ahb2ahb_membar and ahb2ahb_iobar in gaisler.misc package to generate this generic).	0 - 1073741823	0
lsb_bank1	Address area 1 mapped on the low-speed bus	0 - 1073741823	0
lsb_bank2	Address area 2 mapped on the low-speed bus	0 - 1073741823	0
lsb_bank3	Address area 3 mapped on the low-speed bus	0 - 1073741823	0

Table 42. Configuration options

Generic	Function	Allowed range	Default
lsb_ioarea	Address of low-speed bus I/O area that contains the low-speed bus configuration area. Will appear in the bridge's user-defined register 1 on the high-speed bus. Note that to allow high-speed bus masters to read the low-speed bus configuration area, the area must be mapped on one of the *lsb_bank* generics.	0 - 16#FFF#	0
lckdac	Locked access error detection and correction. This generic is mapped to the generic with the same name on the two AHB2AHB cores instantiated by AHBBRIDGE. Please see the documentation for the AHB2AHB core's VHDL generics for more information.	0 - 2	0
maccsz	This generic is propagated to the slvmaccsz and mstmaccsz VHDL generics on the two AHB2AHB cores instantiated by AHBBRIDGE. The generic determines the maximum AHB access size supported by the bridge. Please see the documentation for the AHB2AHB core's VHDL generics for more information.	32 - 256	32
rdcomb	Read combining, this generic is mapped to the generic with the same name on the two AHB2AHB cores instantiated by AHBBRIDGE. Please see the documentation for the AHB2AHB core's VHDL generics for more information.	0 - 2	0
wrcomb	Write combining, this generic is mapped to the generic with the same name on the two AHB2AHB cores instantiated by AHBBRIDGE. Please see the documentation for the AHB2AHB core's VHDL generics for more information.	0 - 2	0
combmask	Read/Write combining mask, this generic is mapped to the generic with the same name on the two AHB2AHB cores instantiated by AHBBRIDGE. Please see the documentation for the AHB2AHB core's VHDL generics for more information.	0 - 16#FFFF#	16#FFFF#
allbrst	Support all burst types, this generic is mapped to the generic with the same name on the two AHB2AHB cores instantiated by AHBBRIDGE. Please see the documentation for the AHB2AHB core's VHDL generics for more information.	0 - 2	0
fcfs	First-come, first-served operation, this generic is mapped to the generic with the same name on the two AHB2AHB cores instantiated by AHBBRIDGE. Please see the documentation for the AHB2AHB core's VHDL generics for more information.	0 - NAHBMST	0
scantest	Enable scan support	0 - 1	0

5.7 Signal descriptions

Table 43 shows the interface signals of the core (VHDL ports).

Table 43. Signal descriptions

Signal name	Type	Function	Active
RST	Input	Reset	Low
HSB_HCLK	Input	High-speed AHB clock	-
LSB_HCLK	Input	Low-speed AHB clock	-
HSB_AHBSI	Input	High-speed bus AHB slave input signals	-
HSB_AHBSO	Output	High-speed bus AHB slave output signals	-
HSB_AHBSOV	Input	High-speed bus AHB slave input signals	-
HSB_AHBMI	Input	High-speed bus AHB master input signals	-
HSB_AHBMO	Output	High-speed bus AHB master output signals	-
LSB_AHBSI	Input	Low-speed bus AHB slave input signals	-
LSB_AHBSO	Output	Low-speed bus AHB slave output signals	-
LSB_AHBSOV	Input	Low-speed bus AHB slave input signals	-
LSB_AHBMI	Input	Low-speed bus AHB master input signals	-
LSB_AHBMO	Output	Low-speed bus AHB master output signals	-

5.8 Library dependencies

Table 44 shows the libraries used when instantiating the core (VHDL libraries).

Table 44. Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	MISC	Component	Component declaration

6 AHBCTRL - AMBA AHB controller with plug&play support

6.1 Overview

The AMBA AHB controller is a combined AHB arbiter, bus multiplexer and slave decoder according to the AMBA 2.0 standard.

The controller supports up to 16 AHB masters, and 16 AHB slaves. The maximum number of masters and slaves are defined in the GRLIB.AMBA package, in the VHDL constants NAHBSLV and NAHBMST. It can also be set with the *nahbm* and *nahbs* VHDL generics.

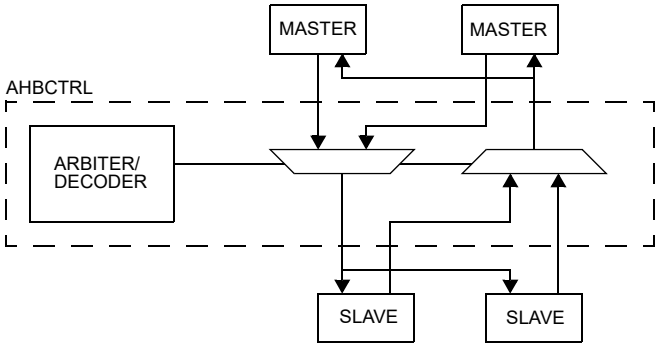


Figure 10. AHB controller block diagram

6.2 Operation

6.2.1 Arbitration

The AHB controller supports two arbitration algorithms: fixed-priority and round-robin. The selection is done by the VHDL generic *rrobin*. In fixed-priority mode (*rrobin* = 0), the bus request priority is equal to the master's bus index, with index 0 being the lowest priority. If no master requests the bus, the master with bus index 0 (set by the VHDL generic *defmast)* will be granted.

In round-robin mode, priority is rotated one step after each AHB transfer. If no master requests the bus, the last owner will be granted (bus parking). The VHDL generic *mprio* can be used to specify one or more masters that should be prioritized when the core is configured for round-robin mode.

Note that there are AHB slaves that implement split-like functionality by giving AHB retry responses until the access has finished and the original master tries again. All masters on the bus accessing such slaves must be round-robin arbitrated without prioritization to avoid deadlock situations. For GRLIB this applies to the GRPCI and GRPCI2 cores.

During incremental bursts, the AHB master should keep the bus request asserted until the last access as recommended in the AMBA 2.0 specification, or it might loose bus ownership. For fixed-length burst, the AHB master will be granted the bus during the full burst, and can release the bus request immediately after the first access has started. For this to work however, the VHDL generic *fixbrst* should be set to 1.

6.2.2 Decoding

Decoding (generation of HSEL) of AHB slaves is done using the plug&play method explained in the GRLIB User's Manual. A slave can occupy any binary aligned address space with a size of 1 - 4096 Mbyte. A specific I/O area is also decoded, where slaves can occupy 256 byte - 1 Mbyte. The default address of the I/O area is 0xFFF00000, but can be changed with the *ioaddr* and *iomask* VHDL generics. Access to unused addresses will cause an AHB error response.

The I/O area can be placed within a memory area occupied by a slave. The slave will not be selected when the I/O area is accessed.

6.2.3 Plug&play information

GRLIB devices contain a number of plug&play information words which are included in the AHB records they drive on the bus (see the GRLIB user's manual for more information). These records are combined into an array which is connected to the AHB controller unit.

The plug&play information is mapped on a read-only address area, defined by the *cfgaddr* and *cfgmask* VHDL generics, in combination with the *ioaddr* and *iomask* VHDL generics. By default, the area is mapped on address 0xFFFFF000 - 0xFFFFFFFF. The master information is placed on the first 2 kbyte of the block (0xFFFFF000 - 0xFFFFF800), while the slave information is placed on the second 2 kbyte block. Each unit occupies 32 bytes, which means that the area has place for 64 masters and 64 slaves. The address of the plug&play information for a certain unit is defined by its bus index. The address for masters is thus 0xFFFFF000 + n*32, and 0xFFFFF800 + n*32 for slaves.

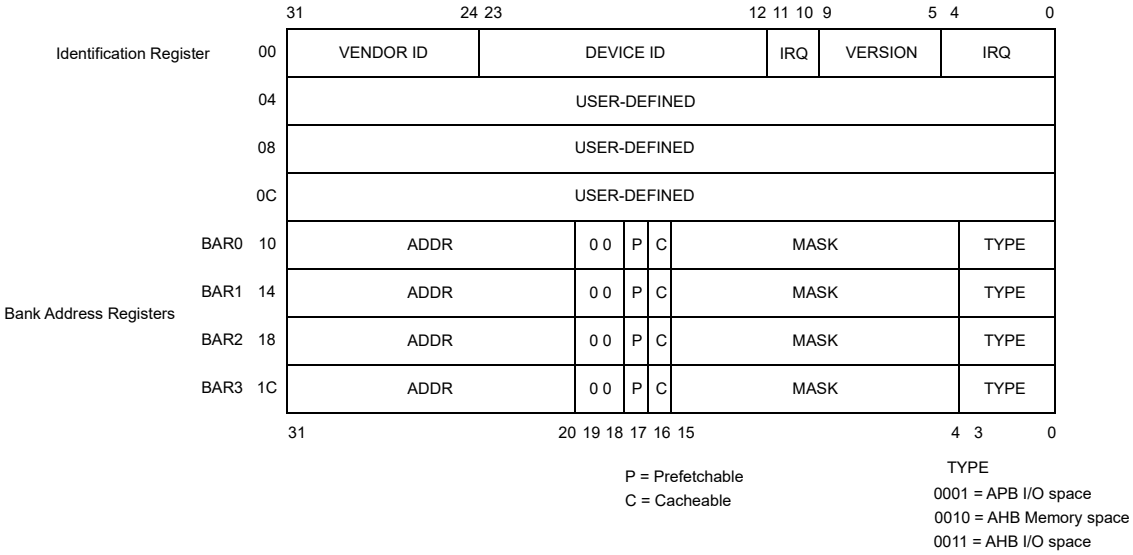


Figure 11. AHB plug&play information record

6.3 AHB split support

AHB SPLIT functionality is supported if the *split* VHDL generic is set to 1. In this case, all slaves must drive the AHB SPLIT signal.

It is important to implement the split functionality in slaves carefully since locked splits can otherwise easily lead to deadlocks. A locked access to a slave which is currently processing (it has returned a split response but not yet split complete) an access which it returned split for to another master must be handled first. This means that the slave must either be able to return an OKAY response to the locked access immediately or it has to split it but return split complete to the master performing the locked transfer before it has finished the first access which received split.

6.4 Locked accesses

The GRLIB AHB controller treats HLOCK as coupled to a specific access. If a previous access by a master received a SPLIT/RETRY response then the arbiter will disregard the current value of HLOCK. This is done as opposed to always treating HLOCK as being valid for the next access which can result in a previously non-locked access being treated as locked when it is retried. Consider the following sequence:

T0: MSTx write 0
T1: MSTx write 1, HLOCK asserted as next access performed by master will be locked
T2: MSTx locked read

If (the non-locked) write 0 access at T0 receives a RETRY or SPLIT response (given at time T1), then the next access to be performed may be a retry of write 0. In this case the arbiter will disregard the HLOCK setting and the retried access will not have HMASTLOCK set.

6.5 AHB bus monitor

An AHB bus monitor is integrated into the core. It is enabled with the *enbusmon* generic. It has the same functionality as the AHB and arbiter parts in the AMBA monitor core (AMBAMON). For more information on which rules are checked se the AMBAMON documentation.

6.6 Registers

The core does not implement any registers.

6.7 Implementation

6.7.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core will use asynchronous reset for all registers if the GRLIB config package setting *grlib_async_reset_enable* is set.

6.8 Configuration options

Table 45 shows the configuration options of the core (VHDL generics).

Table 45. Configuration options

Generic	Function	Allowed range	Default
ioaddr	The MSB address of the I/O area. Sets the 12 most significant bits in the 32-bit AHB address (i.e. 31 downto 20)	0 - 16#FFF#	16#FFF#
iomask	The I/O area address mask. Sets the size of the I/O area and the start address together with ioaddr.	0 - 16#FFF#	16#FFF#
cfgaddr	The MSB address of the configuration area. Sets 12 bits in the 32-bit AHB address (i.e. 19 downto 8).	0 - 16#FFF#	16#FF0#
cfgmask	The address mask of the configuration area. Sets the size of the configuration area and the start address together with cfgaddr. If set to 0, the configuration will be disabled.	0 - 16#FFF#	16#FF0#
rrobin	Selects between round-robin (1) or fixed-priority (0) bus arbitration algorithm.	0 - 1	0
split	Enable support for AHB SPLIT response	0 - 1	0
defmast	Default AHB master	0 - NAHBMST-1	0
ioen	AHB I/O area enable. Set to 0 to disable the I/O area	0 - 1	1
disirq	Set to 1 to disable interrupt routing	0 - 1	0
nahbm	Number of AHB masters	1 - NAHBMST	NAHBMST
nahbs	Number of AHB slaves	1 - NAHBSLV	NAHBSLV

Table 45. Configuration options

Generic	Function	Allowed range	Default
timeout	Perform bus timeout checks (NOT IMPLEMENTED).	0 - 1	0
fixbrst	Enable support for fixed-length bursts	0 - 1	0
debug	Print configuration (0=none, 1=short, 2=all cores)	0 - 2	2
fpnpen	Enables full decoding of the PnP configuration records. When disabled the user-defined registers in the PnP configuration records are not mapped in the configuration area.	0 - 1	0
icheck	Check bus index	0 - 1	1
devid	Assign unique device identifier readable from plug and play area.	N/A	0
enbusmon	Enable AHB bus monitor	0 - 1	0
assertwarn	Enable assertions for AMBA recommendations. Violations are asserted with severity warning.	0 - 1	0
asserterr	Enable assertions for AMBA requirements. Violations are asserted with severity error.	0 - 1	0
hmstdisable	Disable AHB master rule check. To disable a master rule check a value is assigned so that the binary representation contains a one at the position corresponding to the rule number, e.g 0x80 disables rule 7.	N/A	0
hslvdisable	Disable AHB slave tests. Values are assigned as for hmstdisable.	N/A	0
arbdisable	Disable Arbiter tests. Values are assigned as for hmstdisable.	N/A	0
mprio	Master(s) with highest priority. This value is converted to a vector where each position corresponds to a master. To prioritize masters x and y set this generic to $2^x + 2^y$.	N/A	0
mcheck	Check if there are any intersections between core memory areas. If two areas intersect an assert with level failure will be triggered (in simulation). mcheck = 1 does not report intersects between AHB IO areas and AHB memory areas (as IO areas are allowed to override memory areas). mcheck = 2 triggers on all overlaps. See also documentation of VHDL generic shadow below.	0 - 2	1
ccheck	Perform sanity checks on PnP configuration records (in simulation).	0 - 1	1
acdm	AMBA compliant data multiplexing (for HSIZE > word). If this generic is set to 1, and the AMBA bus data width in the system exceeds 32-bits, the core will ensure AMBA compliant data multiplexing for access sizes (HSIZE) over 32-bits. GRLIB cores have an optimization where they drive the same data on all lanes. Read data is always taken from the lowest lanes. If an AMBA compliant core from another vendor is introduced in the design, that core may not always place valid data on the low part of the bus. By setting this generic to 1, the AHBCTRL core will replicate the data, allowing the non-GRLIB cores to be instantiated without modification.	0 - 1	0
index	AHB index for trace print-out, currently unused	N/A	0
ahbtrace	AHB trace print-out to simulator console in simulation.	0 - 1	0

Table 45. Configuration options

Generic	Function	Allowed range	Default
hwdebug	Enable hardware debug registers. If this generic is set to 1 the configuration area will include to diagnostic registers at offsets 0xFF4 and 0xFF8. Offset 0xFF4 will show a 32-bit register where bit n shows the current status of AHB master n's HBUSREQ signal. Offset 0xFF8 will show a 32-bit register where bit n shows the current SPLIT status of AHB master n. The bit will be set when AHB master n receives a SPLIT reply and will be re-set to '0' when HSPLIT for AHB master n has been asserted. This functionality is not intended to be used in production systems but can provide valuable information while debugging systems with cores that have problems with AMBA SPLIT replies.	0 - 1	0
fourgslave	Allow and optimize for case with one single slave that has one 4 GiB bar	0 - 1	0
shadow	Allow memory areas to shadow other memory areas. If this generic is set to 0 and two slaves map the same memory area then HSEL/HMBSEL signals will be asserted for both memory bars / slaves. This may lead to system malfunctions and causes a simulation failure if the mcheck VHDL generic is set to a non-zero value. If the shadow generic is set to 1 then memory area intersects are allowed and only the lowest HSEL and HMBSEL (HSEL has priority) will be asserted - only the slave or bar with the lowest index will be selected instead of both slaves / bars. The mcheck simulation failure will instead be asserted as a note about intersecting memory areas. Also note that intersections of cacheable and noncacheable areas will be treated as cacheable by GRLB cores that decode the plug&play information. If a non-cacheable area is placed in a cacheable area then it is recommended to use fixed cacheability.	0 - 1	0
unmapslv	If this generic is non-zero then accesses to unmapped address space (address space not occupied by any slave) will be redirected to the slave and bar selected via: 256+bar*32+slv.		0

6.9 Signal descriptions

Table 46 shows the interface signals of the core (VHDL ports).

Table 46. Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	AHB reset	Low
CLK	N/A	Input	AHB clock	-
MSTI	*	Output	AMBA AHB master interface record array	-
MSTO	*	Input	AMBA AHB master interface record array	-
SLVI	*	Output	AMBA AHB slave interface record array	-
SLVO	*	Input	AMBA AHB slave interface record array	-

* see GRLIB IP Library User's Manual

6.10 Library dependencies

Table 47 shows libraries used when instantiating the core (VHDL libraries).

Table 47. Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Types	AMBA signal type definitions

6.11 Component declaration

```
library grlib;
use grlib.amba.all;

component ahbctrl
  generic (
    defmast : integer := 0;-- default master
    split   : integer := 0;-- split support
    rrobin  : integer := 0;-- round-robin arbitration
    timeout : integer range 0 to 255 := 0;  -- HREADY timeout
    ioaddr  : ahb_addr_type := 16#fff#;  -- I/O area MSB address
    iomask  : ahb_addr_type := 16#fff#;   -- I/O area address mask
    cfgaddr : ahb_addr_type := 16#ff0#;  -- config area MSB address
    cfgmask : ahb_addr_type := 16#ff0#; -- config area address maskk
    nahbm   : integer range 1 to NAHBMST := NAHBMST; -- number of masters
    nahbs   : integer range 1 to NAHBSLV := NAHBSLV; -- number of slaves
    ioen    : integer range 0 to 15 := 1;   -- enable I/O area
    disirq  : integer range 0 to 1 := 0; -- disable interrupt routing
    fixbrst : integer range 0 to 1 := 0; -- support fix-length bursts
    debug : integer range 0 to 2 := 2; -- print configuration to consolee
    fpnpen : integer range 0 to 1 := 0;     -- full PnP configuration decoding
    icheck  : integer range 0 to 1 := 1
    devid       : integer := 0;     -- unique device ID
    enbusmon    : integer range 0 to 1 := 0; --enable bus monitor
    assertwarn  : integer range 0 to 1 := 0; --enable assertions for warnings
    asserterr   : integer range 0 to 1 := 0; --enable assertions for errors
    hmstdisable : integer := 0; --disable master checks
    hslvdisable : integer := 0; --disable slave checks
    arbdisable  : integer := 0; --disable arbiter checks
    mprio       : integer := 0; --master with highest priority
    enebterm    : integer range 0 to 1 := 0  --enable early burst termination
);
  port (
    rst     : in  std_ulogic;
    clk     : in  std_ulogic;
    msti    : out ahb_mst_in_type;
    msto    : in  ahb_mst_out_vector;
    slvi    : out ahb_slv_in_type;
    slvo    : in  ahb_slv_out_vector;
    testen  : in  std_ulogic := '0';
    testrst : in  std_ulogic := '1';
    scanen  : in  std_ulogic := '0';
    testoen : in  std_ulogic := '1'
  );
  end component;
```

6.12 Instantiation

This example shows the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
```

```
.
.

  -- AMBA signals
  signal ahbsi : ahb_slv_in_type;
  signal ahbso : ahb_slv_out_vector := (others => ahbs_none);
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);

begin

-- ARBITER

ahb0 : ahbctrl -- AHB arbiter/multiplexer
  generic map (defmast => CFG_DEFMST, split => CFG_SPLIT,
rrobin => CFG_RROBIN, ioaddr => CFG_AHBIO, nahbm => 8, nahbs => 8)
  port map (rstn, clkm, ahbmi, ahbmo, ahbsi, ahbso);


-- AHB slave

sr0 : srctrl generic map (hindex => 3)
port map (rstn, clkm, ahbsi, ahbso(3), memi, memo, sdo3);

-- AHB master

e1 : eth_oc
      generic map (mstndx => 2, slvndx => 5, ioaddr => CFG_ETHIO, irq => 12, memtech =>
memtech)
      port map (rstn, clkm, ahbsi, ahbso(5), ahbmi  => ahbmi,
ahbmo => ahbmo(2), ethi1, etho1);
...
end;
```

6.13 Debug print-out

If the debug generic is set to 2, the plug&play information of all attached AHB units are printed to the console during the start of simulation. Reporting starts by scanning the master interface array from 0 to NAHBMST - 1 (defined in the grlib.amba package). It checks each entry in the array for a valid vendor-id (all nonzero ids are considered valid) and if one is found, it also retrieves the device-id. The descriptions for these ids are obtained from the GRLIB.DEVICES package, and are then printed on standard out together with the master number. If the index check is enabled (done with a VHDL generic), the report module also checks if the hindex number returned in the record matches the array number of the record currently checked (the array index). If they do not match, the simulation is aborted and an error message is printed.

This procedure is repeated for slave interfaces found in the slave interface array. It is scanned from 0 to NAHBSLV - 1 and the same information is printed and the same checks are done as for the master interfaces. In addition, the address range and memory type is checked and printed. The address information includes type, address, mask, cacheable and pre-fetchable fields. From this information, the report module calculates the start address of the device and the size of the range. The information finally printed is type, start address, size, cacheability and pre-fetchability. The address ranges currently defined are AHB memory, AHB I/O and APB I/O. APB I/O ranges are ignored by this module.

```
# vsim -c -quiet leon3mp
VSIM 1> run
# LEON3 MP Demonstration design
# GRLIB Version 1.0.7
# Target technology: inferred,  memory library: inferred
# ahbctrl: AHB arbiter/multiplexer rev 1
# ahbctrl: Common I/O area disabled
# ahbctrl: Configuration area at 0xfffff000, 4 kbyte
# ahbctrl: mst0: Cobham Gaisler        Leon3 SPARC V8 Processor
# ahbctrl: mst1: Cobham Gaisler        AHB Debug UART
# ahbctrl: slv0: European Space Agency   Leon2 Memory Controller
```

```
# ahbctrl:       memory at 0x00000000, size 512 Mbyte, cacheable, prefetch
# ahbctrl:       memory at 0x20000000, size 512 Mbyte
# ahbctrl:       memory at 0x40000000, size 1024 Mbyte, cacheable, prefetch
# ahbctrl: slv1: Cobham Gaisler        AHB/APB Bridge
# ahbctrl:       memory at 0x80000000, size 1 Mbyte
# apbctrl: APB Bridge at 0x80000000 rev 1
# apbctrl: slv0: European Space Agency   Leon2 Memory Controller
# apbctrl:       I/O ports at 0x80000000, size 256 byte
# apbctrl: slv1: Cobham Gaisler        Generic UART
# apbctrl:       I/O ports at 0x80000100, size 256 byte
# apbctrl: slv2: Cobham Gaisler        Multi-processor Interrupt Ctrl.
# apbctrl:       I/O ports at 0x80000200, size 256 byte
# apbctrl: slv3: Cobham Gaisler        Modular Timer Unit
# apbctrl:       I/O ports at 0x80000300, size 256 byte
# apbctrl: slv7: Cobham Gaisler        AHB Debug UART
# apbctrl:       I/O ports at 0x80000700, size 256 byte
# apbctrl: slv11: Cobham Gaisler        General Purpose I/O port
# apbctrl:       I/O ports at 0x80000b00, size 256 byte
# grgpio11: 8-bit GPIO Unit rev 0
# gptimer3: GR Timer Unit rev 0, 8-bit scaler, 2 32-bit timers, irq 8
# irqmp: Multi-processor Interrupt Controller rev 3, #cpu 1
# apbuart1: Generic UART rev 1, fifo 4, irq 2
# ahbuart7: AHB Debug UART rev 0
# leon3_0: LEON3 SPARC V8 processor rev 0
# leon3_0: icache 1*8 kbyte, dcache 1*8 kbyte
VSIM 2>
```

7 AHBJTAG - JTAG Debug Link with AHB Master Interface

7.1 Overview

The JTAG debug interface provides access to on-chip AMBA AHB bus through JTAG. The JTAG debug interface implements a simple protocol which translates JTAG instructions to AHB transfers. Through this link, a read or write transfer can be generated to any address on the AHB bus.

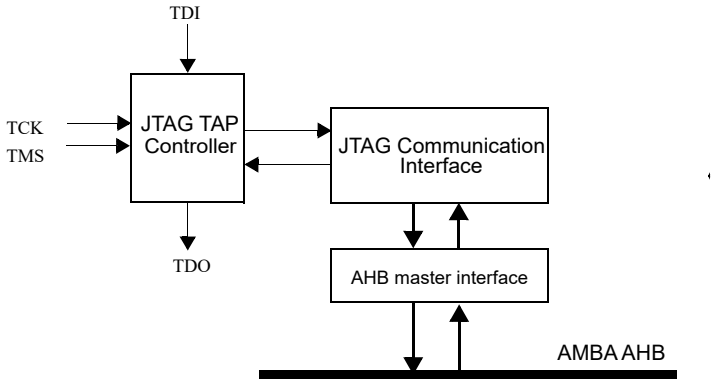


Figure 12. JTAG Debug link block diagram

7.2 Operation

7.2.1 Transmission protocol

The JTAG Debug link decodes two JTAG instructions and implements two JTAG data registers: the command/address register and data register. A read access is initiated by shifting in a command consisting of read/write bit, AHB access size and AHB address into the command/address register. The AHB read access is performed and data is ready to be shifted out of the data register. Write access is performed by shifting in command, AHB size and AHB address into the command/data register followed by shifting in write data into the data register. Sequential transfers can be performed by shifting in command and address for the transfer start address and shifting in SEQ bit in data register for following accesses. The SEQ bit will increment the AHB address for the subsequent access. Sequential transfers should not cross a 1 kB boundary. Sequential transfers are always word based.

Table 48. JTAG debug link Command/Address register

34	33 32	31 ... 0
W	SIZE	AHB ADDRESS

34	Write (W) - ‘0’ - read transfer, ‘1’ - write transfer
33 32	AHB transfer size - “00” - byte, “01” - half-word, “10” - word, “11”- reserved
31 30	AHB address

Table 49. JTAG debug link Data register

32	31 ... 0
SEQ	AHB DATA

32	Sequential transfer (SEQ) - If ‘1’ is shifted in this bit position when read data is shifted out or write data shifted in, the subsequent transfer will be to next word address. When read out from the device, this bit is ‘1’ if the AHB access has completed and ‘0’ otherwise.
31 30	AHB Data - AHB write/read data. For byte and half-word transfers data is aligned according to big-endian order where data with address offset 0 data is placed in MSB bits.

As of version 1 of the JTAG debug link the core will signal AHB access completion by setting bit 32 of the data register. In previous versions the debug host could not determine if an AHB accesses had finished when the read data was shifted out of the JTAG debug link data register. As of version 1 a debug host can look at bit 32 of the received data to determine if the access was successful. If bit 32 is '1' the access completed and the data is valid. If bit 32 is '0', the AHB access was not finished when the host started to read data. In this case the host can repeat the read of the data register until bit 32 is set to '1', signaling that the data is valid and that the AMBA AHB access has completed.

It should be noted that while bit 32 returns '0', new data will not be shifted into the data register. The debug host should therefore inspect bit 32 when shifting in data for a sequential AHB access to see if the previous command has completed. If bit 32 is '0', the read data is not valid and the command just shifted in has been dropped by the core.

Inspection of bit 32 should not be done for JTAG Debug links with version number 0.

7.2.2 Endianness

The core is designed for big-endian systems.

7.3 Implementation

7.3.1 Clocking

Except for the TAP state machine and instruction register, the JTAG debug link operates in the AMBA clock domain. To detect when to shift the address/data register, the JTAG clock and TDI are resynchronized to the AMBA domain. The JTAG clock must be less than 1/3 of the AHB clock frequency for the debug link commands to work when nsync=2, and less than 1/2 of the AHB frequency when nsync=1.

7.3.2 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). Registers in the JTAG clock domain have asynchronous reset connected to the JTAG trst. Registers in the system clock domain have synchronous reset.

7.4 Registers

The core does not implement any registers mapped in the AMBA AHB or APB address space.

7.5 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x01C. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

7.6 Implementation

7.6.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers, except synchronization registers, if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support the GRLIB config package setting *grlib_async_reset_enable*.

7.7 Configuration options

Table 50 shows the configuration options of the core (VHDL generics).

Table 50. Configuration options

Generic	Function	Allowed range	Default
tech	Target technology	0 - NTECH	0
hindex	AHB master index	0 - NAHBMST-1	0
nsync	Number of synchronization registers between clock regions	1 - 2	1
idcode	JTAG IDCODE instruction code (generic tech only)	0 - 255	9
manf	Manufacturer id. Appears as bits 11-1 in TAP controllers device identification register. Used only for generic technology. Default is Cobham Gaisler manufacturer id.	0 - 2047	804
part	Part number (generic tech only). Bits 27-12 in device id. reg.	0 - 65535	0
ver	Version number (generic tech only). Bits 31-28 in device id. reg.	0 - 15	0
ainst	Code of the JTAG instruction used to access JTAG Debug link command/address register. For Actel TAPs (tech VHDL generic is set to an Actel technology) this generic should be set to 16, for all other technologies the default value (2) can be used.	0 - 255	2
dinst	Code of the JTAG instruction used to access JTAG Debug link data register For Actel TAPs (tech VHDL generic is set to an Actel technology) this generic should be set to 17, for all other technologies the default value (3) can be used.	0 - 255	3
scantest	Enable scan test support	0 - 1	0
oepol	Output enable polarity for TDOEN	0 - 1	1
tcknen	Support externally inverted TCK (generic tech only)	0 - 1	0

7.8 Signal descriptions

Table 51 shows the interface signals of the core (VHDL ports).

Table 51. Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	System clock (AHB clock domain)	-
TCK	N/A	Input	JTAG clock*	-
TMS	N/A	Input	JTAG TMS signal*	High
TDI	N/A	Input	JTAG TDI signal*	High
TDO	N/A	Output	JTAG TDO signal*	High
AHBI	***	Input	AHB Master interface input	-
AHBO	***	Output	AHB Master interface output	-
TAPO_TCK	N/A	Output	TAP Controller User interface TCK signal**	High
TAPO_TDI	N/A	Output	TAP Controller User interface TDI signal**	High
TAPO_INST[7:0]	N/A	Output	TAP Controller User interface INSTsignal**	High
TAPO_RST	N/A	Output	TAP Controller User interface RST signal**	High
TAPO_CAPT	N/A	Output	TAP Controller User interface CAPT signal**	High
TAPO_SHFT	N/A	Output	TAP Controller User interface SHFT signal**	High
TAPO_UPD	N/A	Output	TAP Controller User interface UPD signal**	High
TAPI_TDO	N/A	Input	TAP Controller User interface TDO signal**	High
TRST	N/A	Input	JTAG TRST signal	Low
TDOEN	N/A	Output	Output-enable for TDO	See oepol
TCKN	N/A	Input	Inverted JTAG clock* (if tcknen is set)	-
TAPO_TCKN	N/A	Output	TAP Controller User interface TCKN signal**	High
TAPO_NINST	N/A	Output	TAP Controller User interface NINSTsignal**	High
TAPO_IUPD	N/A	Output	TAP Controller User interface IUPD signal**	High

*) If the target technology is Xilinx or Altera the cores JTAG signals TCK, TCKN, TMS, TDI and TDO are not used. Instead the dedicated FPGA JTAG pins are used. These pins are implicitly made visible to the core through TAP controller instantiation.

**) User interface signals from the JTAG TAP controller. These signals are used to interface additional user defined JTAG data registers such as boundary-scan register. For more information on the JTAG TAP controller user interface see JTAG TAP Controller IP-core documentation. If not used tie TAPI_TDO to ground and leave TAPO_* outputs unconnected.

***) see GRLIB IP Library User's Manual

7.9 Signal definitions and reset values

The signals and their reset values are described in table 52.

Table 52. Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
dsutck	Input	JTAG clock	-	-
dsutms	Input	JTAG TMS	High	-
dsutdi	Input	JTAG TDI	High	-
dsutdo	Output	JTAG TDO	High	undefined

7.10 Timing

The timing waveforms and timing parameters are shown in figure 13 and are defined in table 53.

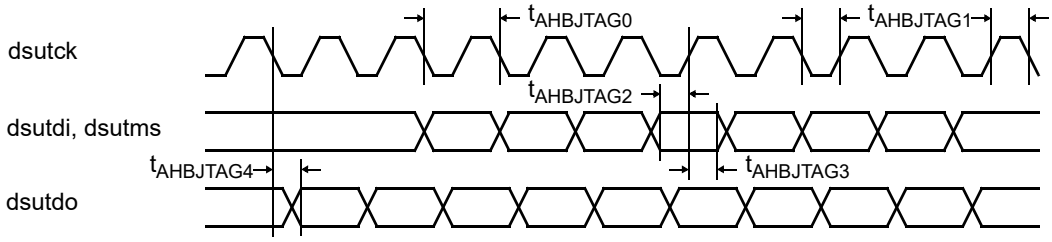


Figure 13. Timing waveforms

Table 53. Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{AHBJTAG0}$	clock period	-	TBD	-	ns
$t_{AHBJTAG1}$	clock low/high period	-	TBD	-	ns
$t_{AHBJTAG2}$	data input to clock setup	rising *dsutck* edge	TBD	-	ns
$t_{AHBJTAG3}$	data input from clock hold	rising *dsutck* edge	TBD	-	ns
$t_{AHBJTAG4}$	clock to data output delay	falling *dsutck* edge	-	TBD	ns

7.11 Library dependencies

Table 54 shows libraries used when instantiating the core (VHDL libraries).

Table 54. Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	JTAG	Signals, component	Signals and component declaration

7.12 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.jtag.all;

entity ahbjtag_ex is
  port (
    clk : in std_ulogic;
    rstn : in std_ulogic;

    -- JTAG signals
    tck  : in std_ulogic;
    tms  : in std_ulogic;
    tdi  : in std_ulogic;
    tdo  : out std_ulogic
);
end;

architecture rtl of ahbjtag_ex is
```

```
  -- AMBA signals
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);
signal gnd : std_ulogic;

constant clkperiod : integer := 100;

begin

gnd <= '0';

  -- AMBA Components are instantiated here
  ...

-- AHB JTAG
  ahbjtag0 : ahbjtag generic map(tech => 0, hindex => 1)
 port map(rstn, clkm, tck, tckn, tms, tdi, tdo, ahbmi, ahbmo(1),
               open, open, open, open, open, open, open, gnd);


jtagproc : process
  begin
wait;
    jtagcom(tdo, tck, tms, tdi, 100, 20, 16#40000000#, true);
    wait;
   end process;

end;
```

7.13 Simulation

DSU communication over the JTAG debug link can be simulated using *jtagcom* procedure. The *jtagcom* procedure sends JTAG commands to the AHBJTAG on JTAG signals TCK, TMS, TDI and TDO. The commands read out and report the device identification code, optionally put the CPU(s) in debug mode, perform three write operations to the memory and read out the data from the memory. The JTAG test works if the generic JTAG tap controller is used and will not work with built-in TAP macros (such as Altera and Xilinx JTAG macros) since these macros don't have visible JTAG pins. The jtagcom procedure is part of *jtagtst* package in *gaisler* library and has following declaration:

```
procedure jtagcom(signal tdo           : in std_ulogic;
                  signal tck, tms, tdi : out std_ulogic;
                  cp, start, addr      : in integer;
                        -- cp - TCK clock period in ns
                        -- start - time in us when JTAG test is started
                        -- addr - read/write operation destination address
                  haltcpu          : in boolean);
```

8 AHBRAM - Single-port RAM with AHB interface

8.1 Overview

AHBRAM implements on-chip RAM with an AHB slave interface. Memory size is configurable in binary steps through a VHDL generic. Minimum size is 1KiB and maximum size is dependent on target technology and physical resources. Read accesses have zero or one waitstate (configured at implementation time), write access have one waitstate. The RAM supports byte- and half-word accesses, as well as all types of AHB burst accesses.

Internally, the AHBRAM instantiates a SYNCRAM block with byte writes. Depending on the target technology map, this will translate into memory with byte enables or to multiple 8-bit wide SYNCRAM blocks.

The size of the RAM implemented within AHBRAM can be read via the core's AMBA plug&play version field. The version field will display log2(number of bytes), for a 1 KiB SYNCRAM the version field will have the value 10, where 2^{10} = 1024 bytes = 1 KiB.

8.1.1 Endianness

The core is designed for big-endian systems.

8.2 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x00E. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

8.3 Implementation

8.3.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support *grlib_async_reset_enable*. All registers that react on the reset signal will have a synchronous reset.

8.4 Configuration options

Table 55 shows the configuration options of the core (VHDL generics).

Table 55. Configuration options

Generic	Function	Allowed range	Default
hindex	AHB slave bus index	0 - NAHBSLV-1	0
haddr	The MSB address of the AHB area. Sets the 12 most significant bits in the 32-bit AHB address.	0 - 16#FFF#	16#FFF#
hmask	The AHB area address mask. Sets the size of the AHB area and the start address together with *haddr*.	0 - 16#FFF#	16#FF0#
tech	Technology to implement on-chip RAM	0 - NTECH	0
kbytes	RAM size in KiB. The size of the RAM implemented will be the minumum size that will hold the size specified by *kbytes*. A value of 1 here will instantiate a 1 KiB SYNCRAM, a value of 3 will instantiate a 4 KiB SYNCRAM. The actual RAM usage on the target technology then depends on the available RAM resources and the technology map.	target-dependent	1
pipe	Add registers on data outputs. If set to 0 the AMBA data outputs will be connected directly to the core's internal RAM. If set to 1 the core will include registers on the data outputs. Settings this generic to 1 makes read accesses have one waitstate, otherwise the core will respond to read accesses with zero waitstates.	0 - 1	0
maccsz	Maximum access size supported. This generic restricts the maximum AMBA access size supported by the core and selects the width of the SYNCRAMBW RAM used internally. The default value is assigned from AHBDW, which sets the maximum bus width for the GRLIB design.	32, 64, 128, 256	AHBDW
scantest	Enable scan test support (passed on to syncram)	0 - 1	0

8.5 Signal descriptions

Table 56 shows the interface signals of the core (VHDL ports).

Table 56. Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
AHBSI	*	Input	AMB slave input signals	-
AHBSO	*	Output	AHB slave output signals	-

* see GRLIB IP Library User's Manual

8.6 Library dependencies

Table 57 shows libraries used when instantiating the core (VHDL libraries).

Table 57. Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Types	AMBA signal type definitions
GAISLER	MISC	Component	Component declaration

8.7 Component declaration

```
library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.misc.all;

component ahbram
generic ( hindex : integer := 0; haddr : integer := 0; hmask : integer := 16#fff#;
tech : integer := 0; kbytes : integer := 1);
port (
rst : in std_ulogic;
clk : in std_ulogic;
ahbsi : in ahb_slv_in_type;
ahbso : out ahb_slv_out_type
);
end component;
```

8.8 Instantiation

This example shows how the core can be instantiated.

```
library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.misc.all;

.
.

ahbram0 : ahbram generic map (hindex => 7, haddr => CFG_AHBRADDR,
tech => CFG_MEMTECH, kbytes => 8)
    port map ( rstn, clkm, ahbsi, ahbso(7));
```

9 AHBDPRAM - Dual-port RAM with AHB interface

9.1 Overview

AHBDPRAM implements a 32-bit wide on-chip RAM with one AHB slave interface port and one back-end port for a user application. The AHBDPRAM is therefore useful as a buffer memory between the AHB bus and a custom IP core with a RAM interface

The memory size is configurable in binary steps through the *abits* VHDL generic. The minimum size is 1kB while maximum size is dependent on target technology and physical resources. Read accesses are zero-waitstate, write access have one waitstate. The RAM optionally supports byte- and half-word accesses, as well as all types of AHB burst accesses. Internally, the AHBRAM instantiates one 32-bit or four 8-bit wide SYNCRAM_DP blocks. The target technology must have support for dual-port RAM cells.

The back-end port consists of separate clock, address, datain, dataout, enable and write signals. All these signals are sampled on the rising edge of the back-end clock (CLKDP), implementing a synchronous RAM interface. Read-write collisions between the AHB port and the back-end port are not handled and must be prevented by the user. If byte write is enabled, the WRITE(0:3) signal controls the writing of each byte lane in big-endian fashion. WRITE(0) controls the writing of DATAIN(31:24) and so on. If byte write is disabled, WRITE(0) controls writing to the complete 32-bit word.

9.1.1 Endianness

The core is designed for big-endian systems.

9.2 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x00F. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

9.3 Implementation

9.3.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset.

9.4 Configuration options

Table 58 shows the configuration options of the core (VHDL generics).

Table 58. Configuration options

Generic	Function	Allowed range	Default
hindex	AHB slave bus index	0 - NAHBSLV-1	0
haddr	The MSB address of the AHB area. Sets the 12 most significant bits in the 32-bit AHB address.	0 - 16#FFF#	16#FFF#
hmask	The AHB area address mask. Sets the size of the AHB area and the start address together with *haddr*.	0 - 16#FFF#	16#FF0#
tech	Technology to implement on-chip RAM	0 - NTECH	2
abits	Address bits. The RAM size in Kbytes is equal to 2**(abits +2)	8 - 19	8
bytewrite	If set to 1, enabled support for byte and half-word writes	0 - 1	0

9.5 Signal descriptions

Table 59 shows the interface signals of the core (VHDL ports).

Table 59. Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	AHB Reset	Low
CLK	N/A	Input	AHB Clock	-
AHBSI	*	Input	AMB slave input signals	-
AHBSO	*	Output	AHB slave output signals	-
CLKDP		Input	Clock for back-end port	-
ADDRESS(abits-1:0)		Input	Address for back-end port	-
DATAIN(31 : 0)		Input	Write data for back-end port	-
DATAOUT(31 : 0)		Output	Read data from back-end port	-
ENABLE		Input	Chip select for back-end port	High
WRITE(0 : 3)		Input	Write-enable byte select for back-end port	High

* see GRLIB IP Library User's Manual

9.6 Library dependencies

Table 60 shows libraries used when instantiating the core (VHDL libraries).

Table 60. Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Types	AMBA signal type definitions
GAISLER	MISC	Component	Component declaration

9.7 Component declaration

```
library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.misc.all;

component ahbdpram
  generic (
    hindex  : integer := 0;
    haddr   : integer := 0;
    hmask   : integer := 16#fff#;
    tech    : integer := 2;
    abits   : integer range 8 to 19 := 8;
    bytewrite : integer range 0 to 1 := 0
  );
  port (
    rst     : in  std_ulogic;
    clk     : in  std_ulogic;
    ahbsi   : in  ahb_slv_in_type;
    ahbso   : out ahb_slv_out_type;
    clkdp   : in std_ulogic;
    address : in std_logic_vector((abits -1) downto 0);
    datain  : in std_logic_vector(31 downto 0);
    dataout : out std_logic_vector(31 downto 0);
    enable  : in std_ulogic;-- active high chip select
    write   : in std_logic_vector(0 to 3)-- active high byte write enable
  );
  end component;
```

10 AHBROM - Single-port ROM with AHB interface

10.1 Overview

The AHBROM core implements a 32/64/128-bit wide on-chip ROM with an AHB slave interface. Read accesses take zero waitstates, or one waitstate if the pipeline option is enabled. The ROM supports byte- and half-word accesses, as well as all types of AHB burst accesses.

10.2 PROM generation

The AHBPROM is automatically generated by the make utility in GRLIB. The input format is a sparc-elf binary file, produced by the BCC cross-compiler (sparc-elf-gcc). To create a PROM, first compile a suitable binary and the run the make utility:

```
bash$ sparc-elf-gcc prom.S -o prom.exe
bash$ make ahbrom.vhd

Creating ahbrom.vhd : file size 272 bytes, address bits 9
```

The default binary file for creating a PROM is prom.exe. To use a different file, run make with the FILE parameter set to the input file:

```
bash$ make ahbrom.vhd FILE=myfile.exe
```

The created PROM is realized in synthesizable VHDL code, using a CASE statement. For FPGA targets, most synthesis tools will map the CASE statement on a block RAM/ROM if available. For ASIC implementations, the ROM will be synthesized as gates. It is then recommended to use the *pipe* option to improve the timing.

The default is to build a 32-bit wide ahbrom, to instead build 64-bit or 128-bit wide ahbrom versions, use the flow described above but with the “make ahbrom64.vhd” and “make ahbrom128.vhd” make targets.

10.2.1 Endianness

The core is designed for big-endian systems.

10.3 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x01B. For description of vendor and device identifiers see GRLIB IP Library User’s Manual.

10.4 Implementation

10.4.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User’s Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support the GRLIB config package setting *grlib_async_reset_enable*.

10.5 Configuration options

Table 61 shows the configuration options of the core (VHDL generics).

Table 61. Configuration options

Generic	Function	Allowed range	Default
hindex	AHB slave bus index	0 - NAHBSLV-1	0
haddr	The MSB address of the AHB area. Sets the 12 most significant bits in the 32-bit AHB address.	0 - 16#FFF#	16#FFF#
hmask	The AHB area address mask. Sets the size of the AHB area and the start address together with *haddr*.	0 - 16#FFF#	16#FF0#
tech	Not used		
pipe	Add a pipeline stage on read data	0	0
kbytes	Not used		
Only on ahbrom64 and ahbrom128:			
wideonly	Removes muxing logic needed to properly support 32-bit masters on wide bus	0 - 1	0

10.6 Signal descriptions

Table 62 shows the interface signals of the core (VHDL ports).

Table 62. Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
AHBSI	*	Input	AMB slave input signals	-
AHBSO	*	Output	AHB slave output signals	-

* see GRLIB IP Library User's Manual

10.7 Library dependencies

Table 63 shows libraries used when instantiating the core (VHDL libraries).

Table 63. Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Types	AMBA signal type definitions

10.8 Component declaration

```
component ahbrom
generic ( hindex : integer := 0; haddr : integer := 0; hmask : integer := 16#fff#;
pipe : integer := 0; tech : integer := 0);
port (
rst : in std_ulogic;
clk : in std_ulogic;
ahbsi : in ahb_slv_in_type;
ahbso : out ahb_slv_out_type
);
end component;
```

10.9 Instantiation

This example shows how the core can be instantiated.

```
library grlib;
use grlib.amba.all;
.
.

brom : entity work.ahbrom
      generic map (hindex => 8, haddr => CFG_AHBRODDR, pipe => CFG_AHBROPIP)
      port map ( rstn, clkm, ahbsi, ahbso(8));
```

11 AHBSTAT - AHB Status Registers

11.1 Overview

The status registers store information about AMBA AHB accesses triggering an error response. There is a status register and a failing address register capturing the control and address signal values of a failing AMBA bus transaction, or the occurrence of a correctable error being signaled from a another peripheral in the system.

The status register and the failing address register are accessed from the AMBA APB bus.

11.2 Operation

11.2.1 Errors

The registers monitor AMBA AHB bus transactions and store the current HADDR, HWRITE, HMASTER and HSIZE internally. The monitoring are always active after startup and reset until an error response (HRESP = “01”) is detected. When the error is detected, the status and address register contents are frozen and the New Error (NE) bit is set to one. At the same time an interrupt is generated, as described hereunder.

Note that many of the fault tolerant units containing EDAC signal an un-correctable error as an AMBA error response, so that it can be detected by the processor as described above.

11.2.2 Correctable errors

Not only error responses on the AHB bus can be detected. Many of the fault tolerant units containing EDAC have a correctable error signal which is asserted each time a correctable error is detected. When such an error is detected, the effect will be the same as for an AHB error response. The only difference is that the Correctable Error (CE) bit in the status register is set to one when a correctable error is detected.

When the CE bit is set the interrupt routine can acquire the address containing the correctable error from the failing address register and correct it. When it is finished it resets the NE bit and the monitoring becomes active again. Interrupt handling is described in detail hereunder.

The correctable error signals from the fault tolerant units should be connected to the *stati.cerror* input signal vector of the AHB status register core, which is or-ed internally and if the resulting signal is asserted, it will have the same effect as an AHB error response.

11.2.3 Interrupts

The interrupt is generated on the line selected by the *pirq* VHDL generic.

The interrupt is connected to the interrupt controller to inform the processor of the error condition. The normal procedure is that an interrupt routine handles the error with the aid of the information in the status registers. When it is finished it resets the NE bit and the monitoring becomes active again. Interrupts are generated for both AMBA error responses and correctable errors as described above.

11.2.4 Filtering and multiple error detection

The status register can optionally be implemented with two sets of status and failing address register. In this case the core also supports filtering on errors and has a status bit that gets set in case additional errors are detected when the New Error (NE) bit is set. The core will only react to the first error in a burst operation. After the first error has been detected, monitoring of the burst is suspended. An error event will only be recorded by the first status register that should react based on filter settings. If register set 1 has reacted then register 2 will not be set for the same error event.

The extra register set, filtering, and multiple error detection is available in revision 1 of the status register. The functionality is enabled through the *ver* VHDL generic. The value of this generic also affects the core version in the GRLIB plug&play information.

11.3 Registers

The core is programmed through registers mapped into APB address space.

Table 64. AHB Status registers

APB address offset	Registers
0x00	AHB Status register
0x04	AHB Failing address register
0x08	AHB Status register 2 (optional)
0x0C	AHB Failing Address register 2 (optional)

11.3.1 AHB Status register

Table 65. 0x00, 0x08- AHBS - AHB Status register

31 14	13	12	11	10	9	8	7	6 3	2 0
RESERVED	ME	FW	CF	AF	CE	NE	HWRITE	HMASTER	HSIZE
0	0	0	0	0	0	0	NR	NR	NR
r	rw*	w*	rw*	rw*	rw	rw	r	r	r

31: 14	RESERVED
13	Multiple Error detection (ME) - This field is set to 1 when the New Error bit is set and one more error is detected. Filtering is considered when setting the ME bit. This field is only available in version 1 of the core (version is selected at implementation).
12	Filter Write (FW) - This bit needs to be set to '1' during a write operation for CF and AF fields to be updated in the same write operation. Always reads as zero. This field is only available in version 1 of the core (version is selected at implementation).
11	Correctable Error Filter (CF) - If this bit is set to 1 then this status register will ignore correctable errors. This field will only be written if the FW bit is set. This field is only available in version 1 of the core (version is selected at implementation).
10	AMBA ERROR Filter (AF) - If this bit is set to 1 then this status register will ignore AMBA ERROR. This field will only be written if the FW bit is set. This field is only available in version 1 of the core (version is selected at implementation).
9	Correctable Error (CE) - Set if the detected error was caused by a correctable error and zero otherwise.
8	New Error (NE) - Deasserted at start-up and after reset. Asserted when an error is detected. Reset by writing a zero to it.
7	The HWRITE signal of the AHB transaction that caused the error.
6: 3	The HMASTER signal of the AHB transaction that caused the error.
2: 0	The HSIZE signal of the AHB transaction that caused the error

11.3.2 AHB Failing address register

Table 66. 0x04, 0x0C - AHBFAR - AHB Failing address register

31 0
AHB FAILING ADDRESS
NR
t

31: 0	The HADDR of the AHB transaction that caused the error.

11.4 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x052. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

11.5 Implementation

11.5.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). When reset is asserted the new error and correctable error registers are reset to zero.

11.6 Configuration options

Table 67 shows the configuration options of the core (VHDL generics).

Table 67. Configuration options

Generic	Function	Allowed range	Default
pindex	APB slave index	0 - NAHBSLV-1	0
paddr	APB address	0 - 16#FFF#	0
pmask	APB address mask	0 - 16#FFF#	16#FFF#
pirq	Interrupt line driven by the core	0 - 16#FFF#	0
nftslv	Number of FT slaves connected to the cerror vector	1 - NAHBSLV-1	3
ver	Selects version of the core. Setting this value to 1 implements the two sets of registers, multiple error detection, and filter functionality.	0 - 1	0

11.7 Signal descriptions

Table 68 shows the interface signals of the core (VHDL ports).

Table 68. Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
AHBMI	*	Input	AHB slave input signals	-
AHBSI	*	Input	AHB slave output signals	-
STATI	CERROR	Input	Correctable Error Signals	High
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-

* see GRLIB IP Library User's Manual

11.8 Library dependencies

Table 69 shows libraries used when instantiating the core (VHDL libraries).

Table 69. Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AHB signal definitions
GAISLER	MISC	Component	Component declaration

11.9 Instantiation

This example shows how the core can be instantiated.

The example design contains an AMBA bus with a number of AHB components connected to it including the status register. There are three Fault Tolerant units with EDAC connected to the status register *cerror* vector. The connection of the different memory controllers to external memory is not shown.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
```

```
use grlib.tech.all;
library gaisler;
use gaisler.memctrl.all;
use gaisler.misc.all;

entity mctrl_ex is
  port (
    clk : in std_ulogic;
    rstn : in std_ulogic;
  --other signals
  ....
    );
end;

architecture rtl of mctrl_ex is

  -- AMBA bus (AHB and APB)
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbsi : ahb_slv_in_type;
  signal ahbso : ahb_slv_out_vector := (others => ahbs_none);
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);

  -- signals used to connect memory controller and memory bus
  signal memi : memory_in_type;
  signal memo : memory_out_type;

  signal sdo, sdo2: sdctrl_out_type;

  signal sdi : sdctrl_in_type;

-- correctable error vector
  signal stati : ahbstat_in_type;
  signal aramo : ahbram_out_type;

begin

  -- AMBA Components are defined here ...

-- AHB Status Register
  astat0 : ahbstat generic map(pindex => 13, paddr => 13, pirq => 11,
    nftslv => 3)
    port map(rstn, clkm, ahbmi, ahbsi, stati, apbi, apbo(13));
    stati.cerror(3 to NAHBSLV-1) <= (others => '0');

--FT AHB RAM
  a0 : ftahbram generic map(hindex => 1, haddr => 1, tech => inferred,
    kbytes => 64, pindex => 4, paddr => 4, edacen => 1, autoscrub => 0,
    errcnt => 1, cntbits => 4)
    port map(rst, clk, ahbsi, ahbso, apbi, apbo(4), aramo);
    stati.cerror(0) <= aramo.ce;
-- SDRAM controller
  sdc : ftsdctrl generic map (hindex => 3, haddr => 16#600#, hmask => 16#F00#,
    ioaddr => 1, fast => 0, pwron => 1, invclk => 0, edacen => 1, errcnt => 1,
    cntbits => 4)
    port map (rstn, clk, ahbsi, ahbso(3), sdi, sdo);
    stati.cerror(1) <= sdo.ce;

-- Memory controller
  mctrl0 : ftsrctrl generic map (rmw => 1, pindex => 10, paddr => 10,
    edacen => 1, errcnt => 1, cntbits => 4)
    port map (rstn, clk, ahbsi, ahbso(0), apbi, apbo(10), memi, memo, sdo2);
    stati.cerror(2) <= memo.ce;
end;
```

12 AHBTRACE - AHB Trace buffer

12.1 Overview

The trace buffer consists of a circular buffer that stores AMBA AHB data transfers. The address, data and various control signals of the AHB bus are stored and can be read out for later analysis.

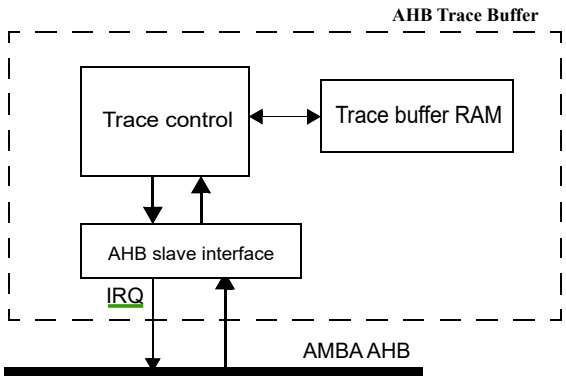


Figure 14. Block diagram

When the trace buffer is configured in 32-bit bus mode, it is 128 bits wide. The information stored is indicated in the table below:

Table 70. AHB Trace buffer data allocation

Bits	Name	Definition
127:96	Time tag	The value of the time tag counter
95	AHB breakpoint hit	Set to '1' if a DSU AHB breakpoint hit occurred.
94:80	-	Not used
79	Hwrite	AHB HWRITE
78:77	Htrans	AHB HTRANS
76:74	Hsize	AHB HSIZE
73:71	Hburst	AHB HBURST
70:67	Hmaster	AHB HMASTER
66	Hmastlock	AHB HMASTLOCK
65:64	Hresp	AHB HRESP
63:32	Load/Store data	AHB HRDATA[31:0] or HWDATA[31:0]
31:0	Load/Store address	AHB HADDR

In addition to the AHB signals, a 32-bit counter is also stored in the trace as time tag.

When the trace buffer is configured in 64-bit or 128-bit bus mode, its contents are extended according to the table below.

Bits	Name	Definition
223:160	128-bit extended load/store data	AHB HRDATA[127:64] or HWDATA[127:64]
159:128	64-bit extended load/store data	AHB HRDATA[63:32] or HWDATA[63:32]

12.2 Operation

12.2.1 Overview

The trace buffer is enabled by setting the enable bit (EN) in the trace control register. Each AMBA AHB transfer is then stored in the buffer in a circular manner. The address to which the next transfer is written is held in the trace buffer index register, and is automatically incremented after each transfer. Tracing is stopped when the EN bit is reset, or when a AHB breakpoint is hit. An interrupt is generated when a breakpoint is hit.

Note: the LEON3 and LEON4 Debug Support Units (DSU3/DSU4) also includes an AHB trace buffer. The standalone trace buffer is intended to be used in system without a processor or when the DSU3 is not present.

The size of the trace buffer is configured by means of the *kbytes* VHDL generic, defining the size of the complete buffer in kbytes.

The number of lines in the trace buffer is *kbytes* * 1024 / 16 bytes.

The total size of the trace buffer depends on the *bwidth* generic. When the ahb trace buffer is in 32-bit bus mode, the size of the buffer is simply *kbytes* kbytes.

When the ahb trace buffer is configured in 64-bit or 128-bit bus mode, the *kbytes* generic will not reflect the exact amount of memory used in the core. You will have to multiply each line, calculated as above, for 20 bytes or 28 bytes, for 64-bit bus mode or 128-bit bus mode respectively. Therefore the total size for the buffer when in 64-bit mode is *kbytes* * 1.25 kbytes, and for the buffer in 128-bit bus mode it is *kbytes* * 1.75 kbytes.

12.2.2 AHB statistics

The core can be implemented to generate statistics from the traced AHB bus. When statistics collection is enabled the core will assert outputs that are suitable to connect to a LEON statistics unit (L3STAT and L4STAT). The statistical outputs can be filtered by the AHB trace buffer filters, this is controlled by the Performance counter Filter bit (PF) in the AHB trace buffer control register. The core can collect data for the events listed in table 71 below.

Table 71. AHB events

Event	Description	Note
idle	HTRANS=IDLE	Active when HTRANS IDLE is driven on the AHB slave inputs and slave has asserted HREADY.
busy	HTRANS=BUSY	Active when HTRANS BUSY is driven on the AHB slave inputs and slave has asserted HREADY.
nseq	HTRANS=NONSEQ	Active when HTRANS NONSEQ is driven on the AHB slave inputs and slave has asserted HREADY.
seq	HTRANS=SEQ	Active when HTRANS SEQUENTIAL is driven on the AHB slave inputs and slave has asserted HREADY.
read	Read access	Active when HTRANS is SEQUENTIAL or NON-SEQUENTIAL, slave has asserted HREADY and the HWRITE input is low.
write	Write access	Active when HTRANS is SEQUENTIAL or NON-SEQUENTIAL, slave has asserted HREADY and the HWRITE input is high.
hsize[5:0]	Transfer size	Active when HTRANS is SEQUENTIAL or NON-SEQUENTIAL, slave has asserted HREADY and HSIZE is BYTE (hsize[0]), HWORD (HSIZE[1]), WORD (hsize[2]), DWORD (hsize[3]), 4WORD hsize[4], or 8WORD (hsize[5]).
ws	Wait state	Active when HREADY input to AHB slaves is low and AMBA response is OKAY.
retry	RETRY response	Active when master receives RETRY response

Table 71. AHB events

Event	Description	Note
split	SPLIT response	Active when master receives SPLIT response
spdel	SPLIT delay	Active during the time a master waits to be granted access to the bus after reception of a SPLIT response. The core will only keep track of one master at a time. This means that when a SPLIT response is detected, the core will save the master index. This event will then be active until the same master is re-allowed into bus arbitration and is granted access to the bus. This also means that the delay measured will include the time for re-arbitration, delays from other ongoing transfers and delays resulting from other masters being granted access to the bus before the SPLIT:ed master is granted again after receiving SPLIT complete. If another master receives a SPLIT response while this event is active, the SPLIT delay for the second master will not be measured.
locked	Locked access	Active while the HMASTLOCK signal is asserted on the AHB slave inputs. (Currently not used by L3STATand L4STAT)

12.3 Registers

12.3.1 Register address map

The trace buffer occupies 128 KiB of address space in the AHB I/O area. The address mapping in parentheses is only available when the core is in 64-bit or 128-bit bus mode. The following register addresses are decoded:

Table 72. Trace buffer address space

Address	Register
0x000000	Trace buffer control register
0x000004	Trace buffer index register
0x000008	Time tag counter
0x00000C	Trace buffer master/slave filter register
0x000010	AHB break address 1
0x000014	AHB mask 1
0x000018	AHB break address 2
0x00001C	AHB mask 2
0x010000 - 0x020000	Trace buffer
...0	Trace bits 127 - 96
...4	Trace bits 95 - 64
...8	Trace bits 63 - 32
...C	Trace bits 31 - 0
(...10)	Trace bits 159 - 128, when in 64- or 128-bit bus mode
(...14)	Trace bits 223 - 192, when in 128-bit bus mode
(...18)	Trace bits 191 - 160, when in 128-bit bus mode
(...1C)	Zero

12.3.2 Trace buffer control register

The trace buffer is controlled by the trace buffer control register:

Table 73. 0x000000 - CTRL - Trace buffer control register

31 16	15	14 12	11 9	8	7 6	5	4	3	2	1	0
DCNT	BA	BSEL	RESERVED	PF	BW	RF	AF	FR	FW	DM	EN
0	*	0	0	0	*	0	0	0	0	0	*
rw	r	rw	r	rw	r	rw	rw	rw	rw	r	rw

31: 16 Trace buffer delay counter (DCNT) - Note that the number of bits actually implemented depends on the size of the trace buffer.

15 Bus select Available (BA) - If this field is set to '1', the core has several buses connected. The bus to trace is selected via the BSEL field. If this field is '0', the core is only capable of tracing one AHB bus.

14: 12 Bus select (BSEL) - If the BA field is '1' this field selects the bus to trace. If the BA field is '0', this field is not writable.

11: 9 RESERVED

8 Performance counter Filter (PF) - If this bit is set to '1', the cores performance counter (statistical) outputs will be filtered using the same filter settings as used for the trace buffer. If a filter inhibits a write to the trace buffer, setting this bit to '1' will cause the same filter setting to inhibit the pulse on the statistical output.

7: 6 Bus width (BW) - This value corresponds to log2(Supported bus width / 32)

5 Retry filter (RF) - If this bit is set to '1', AHB retry responses will not be included in the trace buffer. This bit can only be set of the core has been implemented with support for filtering

4 Address Filter (AF) - If this bit is set to '1', only the address range defined by AHB trace buffer breakpoint 2's address and mask will be included in the trace buffer. This bit can only be set of the core has been implemented with support for filtering

3 Filter Reads (FR) - If this bit is set to '1', read accesses will not be included in the trace buffer. This bit can only be set of the core has been implemented with support for filtering.

2 Filter Writes (FW) - If this bit is set to '1', write accesses will not be included in the trace buffer. This bit can only be set of the core has been implemented with support for filtering.

1 Delay counter mode (DM) - Indicates that the trace buffer is in delay counter mode.

0 Trace enable (EN) - Enables the trace buffer

12.3.3 Trace buffer index register

The trace buffer index register indicates the address of the next 128-bit line to be written.

Table 74. 0x000004 - INDEX - Trace buffer index register

31 4	3 0
INDEX	0x0
NR	0
rw	r

31: 4 Trace buffer index counter (INDEX). Note that the number of bits actually implemented depends on the size of the trace buffer

3: 0 Read as 0x0

12.3.4 Trace buffer time tag register

The time tag register contains a 32-bit counter that increments each clock when the trace buffer is enabled. The value of the counter is stored in the trace to provide a time tag.

Table 75. 0x000008 - TIMETAG - Trace buffer time tag counter

31	0
TIME TAG VALUE	
0	
r	

12.3.5 Trace buffer master/slave filter register

The master/slave filter register allows filtering out specified master and slaves from the trace. This register can only be assigned if the trace buffer has been implemented with support for filtering.

Table 76. Trace buffer master/slave filter register

31	16	15	0
SMASK[15:0]		MMASK[15:0]	
0		0	
rw		rw	

31: 16 Slave Mask (SMASK) - If SMASK[n] is set to '1', the trace buffer will not save accesses performed to slave n.

15: 0 Master Mask (MMASK) - If MMASK[n] is set to '1', the trace buffer will not save accesses performed by master n.

12.3.6 Trace buffer breakpoint registers

The DSU contains two breakpoint registers for matching AHB addresses. A breakpoint hit is used to freeze the trace buffer by clearing the enable bit. Freezing can be delayed by programming the DCNT field in the trace buffer control register to a non-zero value. In this case, the DCNT value will be decremented for each additional trace until it reaches zero and after two additional entries, the trace buffer is frozen. A mask register is associated with each breakpoint, allowing breaking on a block of addresses. Only address bits with the corresponding mask bit set to '1' are compared during breakpoint detection. To break on AHB load or store accesses, the LD and/or ST bits should be set.

Table 77. Trace buffer AHB breakpoint address register

31	2	1	0
BADDR[31:2]		0b00	
NR		0	
rw		r	

31: 2 Breakpoint address (BADDR) - Bits 31:2 of breakpoint address

1: 0 Reserved, read as 0

Table 78. Trace buffer AHB breakpoint mask register

31	2	1	0
BMASK[31:2]		LD	ST
NR		0	0
rw		rw	rw

31: 2 Breakpoint mask (BMASK) - Bits 31:2 of breakpoint mask

1 Load (LD) - Break on data load address

0 Store (ST) - Break on data store address

12.4 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x017. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

12.5 Implementation

12.5.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

12.6 Configuration options

Table 79 shows the configuration options of the core (VHDL generics).

Table 79. Configuration options

Generic	Function	Allowed range	Default
hindex	AHB slave bus index	0 - NAHBSLV-1	0
ioaddr	The MSB address of the I/O area. Sets the 12 most significant bits in the 20-bit I/O address.	0 - 16#FFF#	16#000#
iomask	The I/O area address mask. Sets the size of the I/O area and the start address together with ioaddr.	0 - 16#FFF#	16#E00#
irq	Interrupt number	0 - NAHBIRQ-1	0
tech	Technology to implement on-chip RAM	0 - NTECH	0
kbytes	Trace buffer size in kbytes	1 - 64	1
bwidth	Traced AHB bus width	32, 64, 128	64
ahbfilt	If this generic is set to 1 the core will be implemented with support for AHB trace buffer filters. If *ahbpf* is larger than 1 then the core's statistical outputs will be enabled.	0 - 2	0
ntrace	Number of buses to trace. This generic is only available if the entity ahbtrace_mmb is instantiated.	1 - 8	1
scantest	Support scan test and memory BIST	0 - 1	0
exttimer	If set to 1 then the time tag value will be taken from the core's timer signal input. Otherwise the core will use an internal timer.	0 - 1	0

12.7 Signal descriptions

Table 80 shows the interface signals of the core (VHDL ports).

Table 80. Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
AHBMI	*	Input	AHB master input signals	-
AHBSI	*	Input	AHB slave input signals	-
AHBSO	*	Output	AHB slave output signals	-
TIMER[30:0]	N/A	Input	External timestamp (only used when VHDL generic exttimer is nonzero). Suitable for connection to dbgo.timer signal from debug support unit (DSU IP Core)	-
ASTAT	*	Output	AHB statistics outputs. Intended to be connected to L3STAT and L4STAT core.	-

* see GRLIB IP Library User's Manual

12.8 Library dependencies

Table 81 shows libraries used when instantiating the core (VHDL libraries).

Table 81. Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Types	AMBA signal type definitions
GAISLER	MISC	Component	Component declaration

12.9 Component declaration

```
library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.misc.all;

component ahbtrace is
  generic (
    hindex  : integer := 0;
    ioaddr  : integer := 16#000#;
    iomask  : integer := 16#E00#;
    tech    : integer := 0;
    irq     : integer := 0;
    kbytes  : integer := 1;
    exttimer : integer range 0 to 1 := 0);
  port (
    rst    : in  std_ulogic;
    clk    : in  std_ulogic;
    ahbmi  : in  ahb_mst_in_type;
    ahbsi  : in  ahb_slv_in_type;
    ahbso  : out ahb_slv_out_type;
    timer  : in  std_logic_vector(30 downto 0) := (others => '0'));
end component;

-- Tracebuffer that can trace separate bus:
component ahbtrace_mb is
  generic (
    hindex  : integer := 0;
    ioaddr    : integer := 16#000#;
    iomask    : integer := 16#E00#;
```

```
    tech    : integer := DEFMEMTECH;
    irq     : integer := 0;
    kbytes  : integer := 1;
    exttimer : integer range 0 to 1 := 0);
  port (
    rst    : in  std_ulogic; clk    : in  std_ulogic;
    ahbsi  : in  ahb_slv_in_type;       -- Register interface
    ahbso  : out ahb_slv_out_type;
    tahbmi : in  ahb_mst_in_type; tahbsi : in  ahb_slv_in_type -- Trace
    timer  : in  std_logic_vector(30 downto 0) := (others => '0'));
  end component;

-- Tracebuffer that can trace several separate buses:
component ahbtrace_mmb is
  generic (
    hindex  : integer := 0;
    ioaddr    : integer := 16#000#;
    iomask    : integer := 16#E00#;
    tech    : integer := DEFMEMTECH;
    irq     : integer := 0;
    kbytes  : integer := 1;
    ntrace  : integer range 1 to 8 := 1;
    exttimer : integer range 0 to 1 := 0);
  port (
    rst     : in  std_ulogic; clk    : in  std_ulogic;
    ahbsi   : in  ahb_slv_in_type;       -- Register interface
    ahbso   : out ahb_slv_out_type;
    tahbmiv : in  ahb_mst_in_vector_type(0 to ntrace-1);
    tahbsiv : in  ahb_slv_in_vector_type(0 to ntrace-1) -- Trace
    timer   : in  std_logic_vector(30 downto 0) := (others => '0'));
  end component;
```

13 AHBUART- AMBA AHB Serial Debug Interface

13.1 Overview

The interface consists of a UART connected to the AMBA AHB bus as a master. A simple communication protocol is supported to transmit access parameters and data. Through the communication link, a read or write transfer can be generated to any address on the AMBA AHB bus.

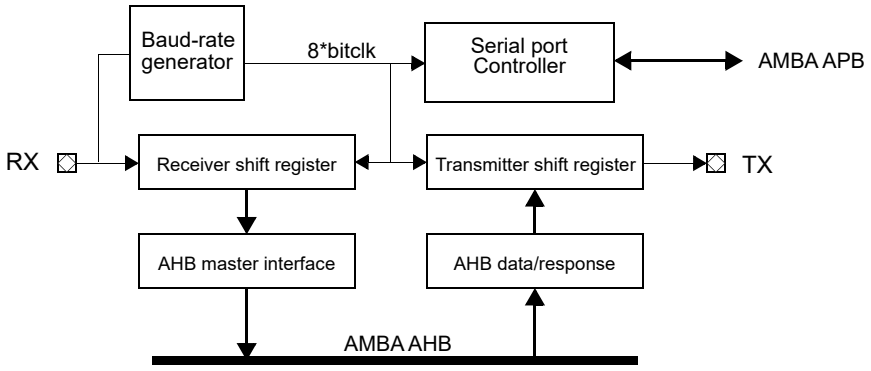


Figure 15. **Block diagram**

13.2 Operation

13.2.1 Transmission protocol

The interface supports a simple protocol where commands consist of a control byte, followed by a 32-bit address, followed by optional write data. Write access does not return any response, while a read access only returns the read data. Data is sent on 8-bit basis as shown below.

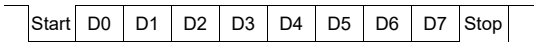


Figure 16. **Data frame**

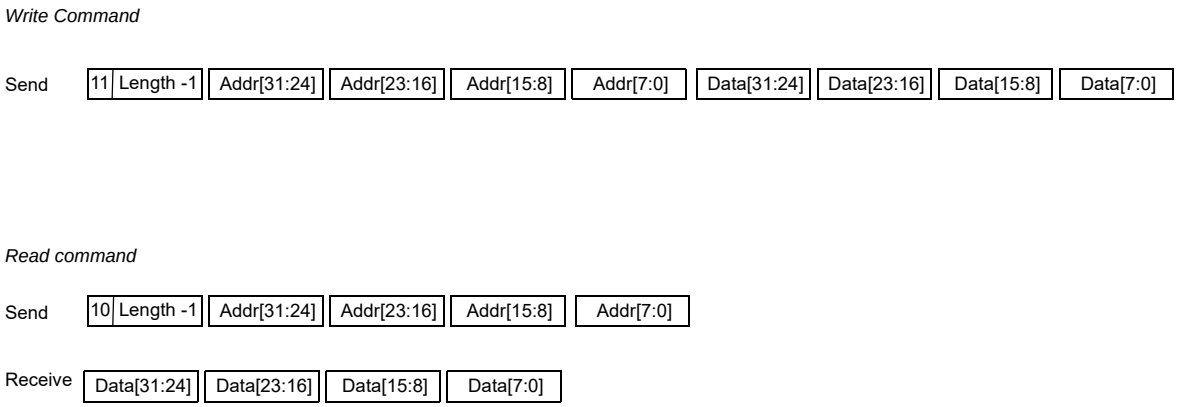


Figure 17. **Commands**

Block transfers can be performed be setting the length field to n-1, where n denotes the number of transferred words. For write accesses, the control byte and address is sent once, followed by the number of data words to be written. The address is automatically incremented after each data word. For

read accesses, the control byte and address is sent once and the corresponding number of data words is returned.

13.2.2 Baud rate generation

The UART contains a 18-bit down-counting scaler to generate the desired baud-rate. The scaler is clocked by the system clock and generates a UART tick each time it underflows. The scaler is reloaded with the value of the UART scaler reload register after each underflow. The resulting UART tick frequency should be 8 times the desired baud-rate.

If not programmed by software, the baud rate will be automatically discovered. This is done by searching for the shortest period between two falling edges of the received data (corresponding to two bit periods). When three identical two-bit periods has been found, the corresponding scaler reload value is latched into the reload register, and the BL bit is set in the UART control register. If the BL bit is reset by software, the baud rate discovery process is restarted. The baud-rate discovery is also restarted when a 'break' or framing error is detected by the receiver, allowing to change to baudrate from the external transmitter. For proper baudrate detection, the value 0x55 should be transmitted to the receiver after reset or after sending break.

The best scaler value for manually programming the baudrate can be calculated as follows:

```
scaler = (((system_clk*10)/(baudrate*8))-5)/10
```

13.3 Registers

The core is programmed through registers mapped into APB address space.

Table 82. AHB UART registers

APB address offset	Register
0x4	AHB UART status register
0x8	AHB UART control register
0xC	AHB UART scaler register

13.3.1 AHB UART control register

Table 83. 0x08 - CTRL - AHB UART control register

31 … 2	1	2
RESERVED	BL	EN
0	0	0
r	rw	rw

0: Receiver enable (EN) - if set, enables both the transmitter and receiver. Reset value: ‘0’.

1: Baud rate locked (BL) - is automatically set when the baud rate is locked. Reset value: ‘0’.

13.3.2 AHB UART status register

Table 84. 0x04 - STAT - AHB UART status register

31 … 10	9	8	7	6	5	4	3	2	1	0
RESERVED		RX	FE	R	OV	BR	TH	TS	DR	
	0	MR	0	0	0	0	1	1	0	
	r	r	rw	r	rw	rw	r	r	r	

0: Data ready (DR) - indicates that new data has been received by the AMBA AHB master interface. Read only. Reset value: ‘0’.

1: Transmitter shift register empty (TS) - indicates that the transmitter shift register is empty. Read only. Reset value: ‘1’

2: Transmitter hold register empty (TH) - indicates that the transmitter hold register is empty. Read only. Reset value: ‘1

3: Break (BR) - indicates that a BREAKE has been received. Reset value: ‘0’

4: Overflow (OV) - indicates that one or more character have been lost due to receiver overflow. Reset value: ‘0’

6: Frame error (FE) - indicates that a framing error was detected. Reset value: ‘0’

13.3.3 AHB UART scaler register

Table 85. 0x0C - SCALER - AHB UART scaler register

31 … 18	17 … 0
RESERVED	SCALER RELOAD VALUE
0	0x3FFFB
r	rw

17: 0 Baudrate scaler reload value = (((system_clk*10)/(baudrate*8))-5)/10. Reset value: “3FFFF“.

13.4 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x007. For description of vendor and device identifiers see GRLIB IP Library User’s Manual.

13.5 Implementation

13.5.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User’s Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support *grlib_async_reset_enable*. All registers that react on the reset signal will have a synchronous reset.

13.6 Configuration options

Table 86 shows the configuration options of the core (VHDL generics).

Table 86. Configuration options

Generic	Function	Allowed range	Default
hindex	AHB master index	0 - NAHBMST-1	0
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	ADDR field of the APB BAR.	0 - 16#FFF#	0
pmask	MASK field of the APB BAR.	0 - 16#FFF#	16#FFF#

13.7 Signal descriptions

Table 87 shows the interface signals of the core (VHDL ports)..

Table 87. Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
UARTI	RXD	Input	UART receiver data	High
	CTSN	Input	UART clear-to-send	High
	EXTCLK	Input	Use as alternative UART clock	-
UARTO	RTSN	Output	UART request-to-send	High
	TXD	Output	UART transmit data	High
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
AHBI	*	Input	AMB master input signals	-
AHBO	*	Output	AHB master output signals	-

* see GRLIB IP Library User's Manual

13.8 Signal definitions and reset values

The signals and their reset values are described in table 88.

Table 88. Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
dsutx	Output	UART transmit data line	-	Logical 1
dsurx	Input	UART receive data line	-	-

13.9 Timing

The timing waveforms and timing parameters are shown in figure 18 and are defined in table 89.

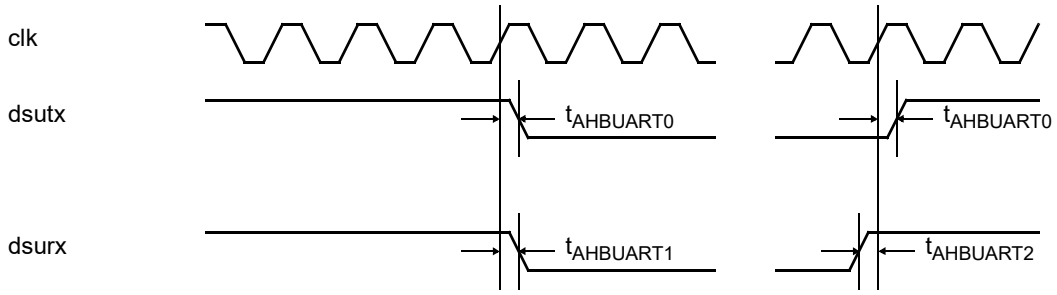


Figure 18. **Timing waveforms**

Table 89. Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{AHBUART0}$	clock to output delay	rising clk edge	TBD	TBD	ns
$t_{AHBUART1}$	input to clock hold	rising clk edge	-	-	ns
$t_{AHBUART2}$	input to clock setup	rising clk edge	-	-	ns

Note: The dsurx input is re-synchronized internally. The signal does not have to meet any setup or hold requirements.

13.10 Library dependencies

Table 90 shows libraries used when instantiating the core (VHDL libraries).

Table 90. Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	UART	Signals, component	Signals and component declaration

13.11 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.uart.all;

entity ahbuart_ex is
  port (
    clk : in std_ulogic;
    rstn : in std_ulogic;

    -- UART signals
    ahbrxd   : in  std_ulogic;
    ahbtxd   : out std_ulogic
    );
end;

architecture rtl of ahbuart_ex is
```

```
  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);

  -- UART signals
  signal ahbuarti : uart_in_type;
  signal ahbuarto : uart_out_type;

begin

  -- AMBA Components are instantiated here
  ...


  -- AHB UART
  ahbuart0 : ahbuart
  generic map (hindex => 5, pindex => 7, paddr => 7)
  port map (rstn, clk, ahbuarti, ahbuarto, apbi, apbo(7), ahbmi, ahbmo(5));

  -- AHB UART input data
  ahbuarti.rxd <= ahbrxd;

  -- connect AHB UART output to entity output signal
  ahbtxd <= ahbuarto.txd;

end;
```

14 AMBAMON - AMBA Bus Monitor

14.1 Overview

The AMBA bus monitor checks the AHB and APB buses for violations against a set of rules. When an error is detected a signal is asserted and error message is (optionally) printed.

14.2 Rules

This section lists all rules checked by the AMBA monitor. The rules are divided into four different tables depending on which type of device they apply to.

Some requirements of the AMBA specification are not adopted by the GRLIB implementation (on a system level). These requirements are listed in the table below.

Table 91. Requirements not checked in GRLIB

Rule Number	Description	References
1	A slave which issues RETRY must only be accessed by one master at a time.	AMBA Spec. Rev 2.0 3-38.

Table 92. AHB master rules.

Rule Number	Description	References
1	Busy can only occur in the middle of bursts. That is only after a NON-SEQ, SEQ or BUSY.	AMBA Spec. Rev 2.0 3-9. http://www.arm.com/support/faqip/492.html
2	Busy can only occur in the middle of bursts. It can be the last access of a burst but only for INCR bursts.	AMBA Spec. Rev 2.0 3-9. http://www.arm.com/support/faqip/492.html
3	The address and control signals must reflect the next transfer in the burst during busy cycles.	AMBA Spec. Rev 2.0 3-9.
4	The first transfer of a single access or a burst must be NONSEQ (this is ensured together with rule 1).	AMBA Spec. Rev 2.0 3-9.
5	HSIZE must never be larger than the bus width.	AMBA Spec. Rev 2.0 3-43.
6	HADDR must be aligned to the transfer size.	AMBA Spec. Rev 2.0 3-12, 3-25. http://www.arm.com/support/faqip/582.html
7	Address and controls signals can only change when hready is low if the previous HTRANS value was IDLE, BUSY or if an ERROR, SPLIT or RETRY response is given.	http://www.arm.com/support/faqip/487.html http://www.arm.com/support/faqip/579.html
8	Address and control signals cannot change between consecutive BUSY cycles.	AMBA Spec. Rev 2.0 3-9.
9	Address must be related to the previous access according to HBURST and HSIZE and control signals must be identical for SEQUENTIAL accesses.	AMBA Spec. Rev 2.0 3-9.
10	Master must cancel the following transfer when receiving an RETRY response.	AMBA Spec. Rev 2.0 3-22.
11	Master must cancel the following transfer when receiving an SPLIT response.	AMBA Spec. Rev 2.0 3-22.

Table 92. AHB master rules.

Rule Number	Description	References
12	Master must reattempt the transfer which received a RETRY response.	AMBA Spec. Rev 2.0 3-21. http://www.arm.com/support/faqip/603.html.
13	Master must reattempt the transfer which received a SPLIT response.	AMBA Spec. Rev 2.0 3-21. http://www.arm.com/support/faqip/603.html.
14	Master can optionally cancel the following transfer when receiving an ERROR response. Only a warning is given if assertions are enabled if it does not cancel the following transfer.	AMBA Spec. Rev 2.0 3-23.
15	Master must hold HWDATA stable for the whole data phase when wait states are inserted. Only the appropriate byte lanes need to be driven for subword transfers.	AMBA Spec. Rev 2.0 3-7. AMBA Spec. Rev 2.0 3-25.
16	Bursts must not cross a 1 kB address boundary.	AMBA Spec. Rev 2.0 3-11.
17	HMASTLOCK indicates that the current transfer is part of a locked sequence. It must have the same timing as address/control.	AMBA Spec. Rev 2.0 3-28.
18	HLOCK must be asserted at least one clock cycle before the address phase to which it refers.	AMBA Spec. Rev 2.0 3-28.
19	HLOCK must be asserted for the duration of a burst and can only be deasserted so that HMASTLOCK is deasserted after the final address phase.	http://www.arm.com/support/faqip/597.html
20	HLOCK must be deasserted in the last address phase of a burst.	http://www.arm.com/support/faqip/588.html
21	HTRANS must be driven to IDLE during reset.	http://www.arm.com/support/faqip/495.html
22	HTRANS can only change from IDLE to NONSEQ or stay IDLE when HREADY is deasserted.	http://www.arm.com/support/faqip/579.html

Table 93. AHB slave rules.

Rule Number	Description	References
1	AHB slave must respond with a zero wait state OKAY response to BUSY cycles in the same way as for IDLE.	AMBA Spec. Rev 2.0 3-9.
2	AHB slave must respond with a zero wait state OKAY response to IDLE.	AMBA Spec. Rev 2.0 3-9.
3	HRESP should be set to ERROR, SPLIT or RETRY only one cycle before HREADY is driven high.	AMBA Spec. Rev 2.0 3-22.
4	Two-cycle ERROR response must be given.	AMBA Spec. Rev 2.0 3-22.
5	Two-cycle SPLIT response must be given.	AMBA Spec. Rev 2.0 3-22.
6	Two-cycle RETRY response must be given.	AMBA Spec. Rev 2.0 3-22.
7	SPLIT complete signalled to master which did not have pending access.	AMBA Spec. Rev 2.0 3-36.
8	Split complete must not be signalled during same cycle as SPLIT.	http://www.arm.com/support/faqip/616.html
9	It is recommended that slaves drive HREADY high and HRESP to OKAY when not selected. A warning will be given if this is not followed.	http://www.arm.com/support/faqip/476.html

Table 93. AHB slave rules.

Rule Number	Description	References
10	It is recommended that slaves do not insert more than 16 wait states. If this is violated a warning will be given if assertions are enabled.	AMBA Spec. Rev 2.0 3-20.
11	Slaves should not assert the HSPLIT (Split complete) signal for more than one cycle for each SPLIT response. If a slave asserts HSPLIT for more than one cycle it will not cause the system to malfunction. It can however be a indication that a core does not perform as expected. Therefore assertion of HSPLIT during more than one cycle for a SPLIT response is reported as a warning.	No reference

Table 94. APB slave rules.

Rule Number	Description	References
1	The bus must move to the SETUP state or remain in the IDLE state when in the IDLE state.	AMBA Spec. Rev 2.0 5-4.
2	The bus must move from SETUP to ENABLE in one cycle.	AMBA Spec. Rev 2.0 5-4.
3	The bus must move from ENABLE to SETUP or IDLE in one cycle.	AMBA Spec. Rev 2.0 5-5.
4	The bus must never be in another state than IDLE, SETUP, ENABLE.	AMBA Spec. Rev 2.0 5-4.
5	PADDR must be stable during transition from SETUP to ENABLE.	AMBA Spec. Rev 2.0 5-5.
6	PWRITE must be stable during transition from SETUP to ENABLE.	AMBA Spec. Rev 2.0 5-5.
7	PWDATA must be stable during transition from SETUP to ENABLE.	AMBA Spec. Rev 2.0 5-5.
8	Only one PSEL must be enabled at a time.	AMBA Spec. Rev 2.0 5-4.
9	PSEL must be stable during transition from SETUP to ENABLE.	AMBA Spec. Rev 2.0 5-5.

Table 95. Arbiter rules

Rule Number	Description	References
1	HreadyIn to slaves and master must be driven by the currently selected device.	http://www.arm.com/support/faqip/482.html
2	A master which received a SPLIT response must not be granted the bus until the slave has set the corresponding HSPLIT line.	AMBA Spec. Rev 2.0 3-35.
3	The dummy master must be selected when a SPLIT response is received for a locked transfer.	http://www.arm.com/support/faqip/14307.html

14.3 Configuration options

Table 96 shows the configuration options of the core (VHDL generics).

***Table 96.* Configuration options**

Generic	Function	Allowed range	Default
asserterr	Enable assertions for AMBA requirements. Violations are asserted with severity error.	0 - 1	1
assertwarn	Enable assertions for AMBA recommendations. Violations are asserted with severity warning.	0 - 1	1
hmstdisable	Disable AHB master rule check. To disable a master rule check a value is assigned so that the binary representation contains a one at the position corresponding to the rule number, e.g 0x80 disables rule 7.	-	0
hslvdisable	Disable AHB slave tests. Values are assigned as for hmstdisable.	-	0
pslvdisable	Disable APB slave tests. Values are assigned as for hmstdisable.	-	0
arbdisable	Disable Arbiter tests. Values are assigned as for hmstdisable.	-	0
nahbm	Number of AHB masters in the system.	0 - NAHBMST	NAHBMST
nahbs	Number of AHB slaves in the system.	0 - NAHBSLV	NAHBSLV
napb	Number of APB slaves in the system.	0 - NAPBSLV	NAPBSLV
ebterm	Relax rule checks to allow use in systems with early burst termination. This generic should be set to 0 for systems that use GRLIB's AHBCTRL core.	0 - 1	0

14.4 Signal descriptions

Table 97 shows the interface signals of the core (VHDL ports).

Table 97. Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	AHB reset	Low
CLK	N/A	Input	AHB clock	-
AHBMI	*	Input	AHB master interface input record	-
AHBMO	*	Input	AHB master interface output record array	-
AHBSI	*	Input	AHB slave interface input record	-
AHBSO	*	Input	AHB slave interface output record array	-
APBI	*	Input	APB slave interface input record	
APBO	*	Input	APB slave interface output record array	
ERR	N/A	Output	Error signal (error detected)	High

* see GRLIB IP Library User's Manual

14.5 Library dependencies

Table 98 shows libraries used when instantiating the core (VHDL libraries).

Table 98. Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Types	AMBA signal type definitions
GAISLER	SIM	Component	Component declaration

14.6 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.sim.all;

entity ambamon_ex is
  port (
    clk : in std_ulogic;
    rst : in std_ulogic
end;

architecture rtl of ambamon_ex is
-- APB signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);


  -- APB signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);


begin
  -- AMBA Components are instantiated here
   ...
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.sim.all;

entity ambamon_ex is
  port (
    clk : in  std_ulogic;
    rst : in  std_ulogic;
    err : out std_ulogic
end;

architecture rtl of ambamon_ex is
  -- AHB signals
  signal ahbmi  : ahb_mst_in_type;
  signal ahbmo  : ahb_mst_out_vector := (others => apb_none);

  -- AHB signals
  signal ahbsi  : ahb_slv_in_type;
  signal ahbso  : ahb_slv_out_vector := (others => apb_none);

  -- APB signals
```

```
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);


begin

  mon0 : ambamon
  generic map(
    assert_err => 1,
    assert_war => 0,
    nahbm      => 2,
    nahbs      => 2,
    napb       => 1
  )
  port map(
    rst        => rst,
    clk        => clk,
    ahbmi      => ahbmi,
    ahbmo      => ahbmo,
    ahbsi      => ahbsi,
    ahbso      => ahbso,
    apbi       => apbi,
    apbo       => apbo,
    err        => err);

end;
```

15 APBCTRL - AMBA AHB/APB bridge with plug&play support

15.1 Overview

The AMBA AHB/APB bridge is a APB bus master according the AMBA 2.0 standard.

The controller supports up to 16 slaves. The actual maximum number of slaves is defined in the GRLIB.AMBA package, in the VHDL constant NAPBSLV. The number of slaves can also be set using the *nslaves* VHDL generic.

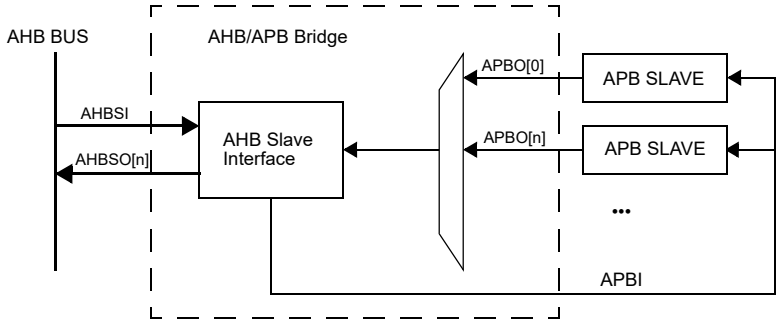


Figure 19. AHB/APB bridge block diagram

15.2 Operation

15.2.1 Decoding

Decoding (generation of PSEL) of APB slaves is done using the plug&play method explained in the GRLIB IP Library User's Manual. A slave can occupy any binary aligned address space with a size of 256 bytes - 1 Mbyte. Writes to unassigned areas will be ignored, while reads from unassigned areas will return an arbitrary value. AHB error response will never be generated.

15.2.2 Plug&play information

GRLIB APB slaves contain two plug&play information words which are included in the APB records they drive on the bus (see the GRLIB IP Library User's Manual for more information). These records are combined into an array which is connected to the APB bridge.

The plug&play information is mapped on a read-only address area at the top 4 kbytes of the bridge address space. Each plug&play block occupies 8 bytes. The address of the plug&play information for a certain unit is defined by its bus index. If the bridge is mapped on AHB address 0x80000000, the address for the plug&play records is thus 0x800FF000 + n*8.

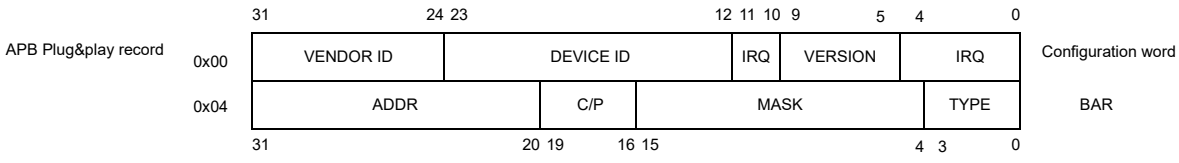


Figure 20. APB plug&play information

15.3 APB bus monitor

An APB bus monitor is integrated into the core. It is enabled with the enbusmon generic. It has the same functionality as the APB parts in the AMBA monitor core (AMBAMON). For more information on which rules are checked se the AMBAMON documentation.

15.4 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x006. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

15.5 Implementation

15.5.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core will use asynchronous reset for all registers if the GRLIB config package setting *grlib_async_reset_enable* is set.

15.6 Configuration options

Table 99 shows the configuration options of the core (VHDL generics).

Table 99. Configuration options

Generic	Function	Allowed range	Default
hindex	AHB slave index	0 - NAHBSLV-1	0
haddr	The MSB address of the AHB area. Sets the 12 most significant bits in the 32-bit AHB address.	0 - 16#FFF#	0
hmask	The AHB area address mask. Sets the size of the AHB area and the start address together with haddr.	0 - 16#FFF#	16#FFF#
nslaves	The maximum number of slaves	1 - NAPBSLV	NAPBSLV
debug	Print debug information during simulation	0 - 2	2
icheck	Enable bus index checking (PINDEX)	0 - 1	1
enbusmon	Enable APB bus monitor	0 - 1	0
asserterr	Enable assertions for AMBA requirements. Violations are asserted with severity error.	0 - 1	0
assertwarn	Enable assertions for AMBA recommendations. Violations are asserted with severity warning.	0 - 1	0
pslvdisable	Disable APB slave rule check. To disable a slave rule check a value is assigned so that the binary representation contains a one at the position corresponding to the rule number, e.g 0x80 disables rule 7.	N/A	0
mcheck	Check if there are any intersections between APB slave memory areas. If two areas intersect an assert with level failure will be triggered (in simulation).	0 - 1	1
ccheck	Perform sanity checks on PnP configuration records (in simulation).	0 - 1	1

15.7 Signal descriptions

Table 100 shows the interface signals of the core (VHDL ports).

*Table 100.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	AHB reset	Low
CLK	N/A	Input	AHB clock	-
AHBI	*	Input	AHB slave input	-
AHBO	*	Output	AHB slave output	-
APBI	*	Output	APB slave inputs	-
APBO	*	Input	APB slave outputs	-

* see GRLIB IP Library User's Manual

15.8 Library dependencies

Table 101 shows libraries used when instantiating the core (VHDL libraries).

*Table 101.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Types	AMBA signal type definitions

15.9 Component declaration

```
library grlib;
use grlib.amba.all;

component apbctrl
  generic (
    hindex  : integer := 0;
    haddr   : integer := 0;
    hmask   : integer := 16#fff#;
    nslaves : integer range 1 to NAPBSLV := NAPBSLV;
    debug   : integer range 0 to 2 := 2;   -- print config to console
    icheck  : integer range 0 to 1 := 1
  );
  port (
    rst     : in  std_ulogic;
    clk     : in  std_ulogic;
    ahbi    : in  ahb_slv_in_type;
    ahbo    : out ahb_slv_out_type;
    apbi    : out apb_slv_in_type;
    apbo    : in  apb_slv_out_vector
  );
  end component;
```

15.10 Instantiation

This example shows how an APB bridge can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
use work.debug.all;

.
.
```

```
  -- AMBA signals

  signal ahbsi : ahb_slv_in_type;
  signal ahbso : ahb_slv_out_vector := (others => ahbs_none);

signal apbi  : apb_slv_in_type;
signal apbo  : apb_slv_out_vector := (others => apb_none);


begin


-- APB bridge

apb0 : apbctrl-- AHB/APB bridge
  generic map (hindex => 1, haddr => CFG_APBADDR)
  port map (rstn, clk, ahbsi, ahbso(1), apbi, apbo );


-- APB slaves

uart1 : apbuart
    generic map (pindex => 1, paddr => 1,  pirq => 2)
    port map (rstn, clk, apbi, apbo(1), u1i, u1o);

irqctrl0 : irqmp
    generic map (pindex => 2, paddr => 2)
    port map (rstn, clk, apbi, apbo(2), irqo, irqi);


...
end;
```

15.11 Debug print-out

The APB bridge can print-out the plug-play information from the attached during simulation. This is enabled by setting the debug VHDL generic to 2. Reporting starts by scanning the array from 0 to NAPBSLV - 1 (defined in the grlib.amba package). It checks each entry in the array for a valid vendor-id (all nonzero ids are considered valid) and if one is found, it also retrieves the device-id. The description for these ids are obtained from the GRLIB.DEVICES package, and is printed on standard out together with the slave number. If the index check is enabled (done with a VHDL generic), the report module also checks if the pindex number returned in the record matches the array number of the record currently checked (the array index). If they do not match, the simulation is aborted and an error message is printed.

The address range and memory type is also checked and printed. The address information includes type, address and mask. The address ranges currently defined are AHB memory, AHB I/O and APB I/O. All APB devices are in the APB I/O range so the type does not have to be checked. From this information, the report module calculates the start address of the device and the size of the range. The information finally printed is start address and size.

16 APBPS2 - PS/2 host controller with APB interface

16.1 Introduction

The PS/2 interface is a bidirectional synchronous serial bus primarily used for keyboard and mouse communications. The APBPS2 core implements the PS2 protocol with a APB back-end. Figure 21 shows a model of APBPS2 and the electrical interface.

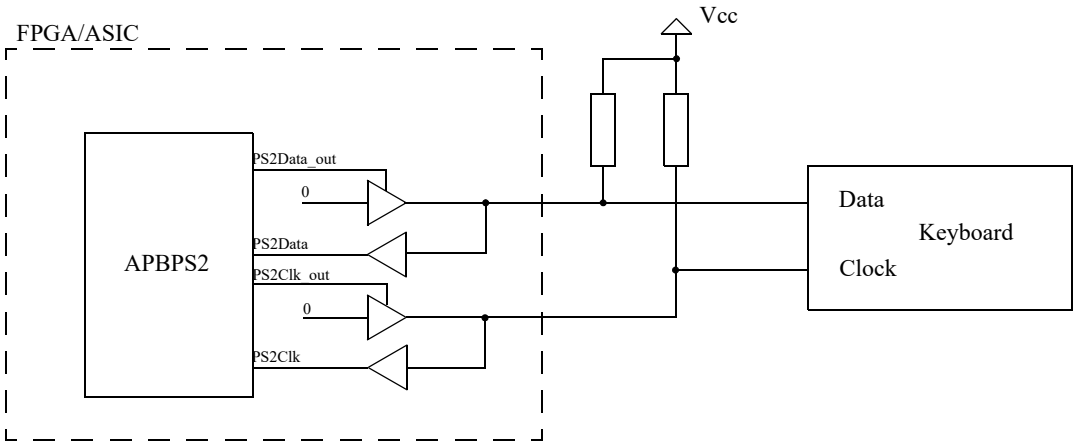


Figure 21. APBPS2 electrical interface

PS/2 data is sent in 11 bits frames. The first bit is a start bit followed by eight data bits, one odd parity bit and finally one stop bit. Figure 22 shows a typical PS/2 data frame.

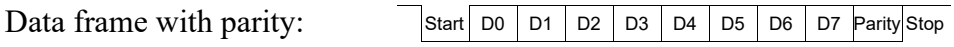


Figure 22. PS/2 data frame

16.2 Receiver operation

The receiver of APBPS2 receives the data from the keyboard or mouse, and converts it to 8-bit data frames to be read out via the APB bus. It is enabled through the receiver enable (RE) bit in the PS/2 control register. If a parity error or framing error occurs, the data frame will be discarded. Correctly received data will be transferred to a 16 byte FIFO. The data ready (DR) bit in the PS/2 status register will be set, and retained as long as the FIFO contains at least one data frame. When the FIFO is full, the receiver buffer full (RF) bit in the status register is set. The keyboard will be inhibited and buffer data until the FIFO gets read again. Interrupt is sent when a correct stop bit is received then it's up to the software to handle any resend operations if the parity bit is wrong. Figure 23 shows a flow chart for the operations of the receiver state machine.

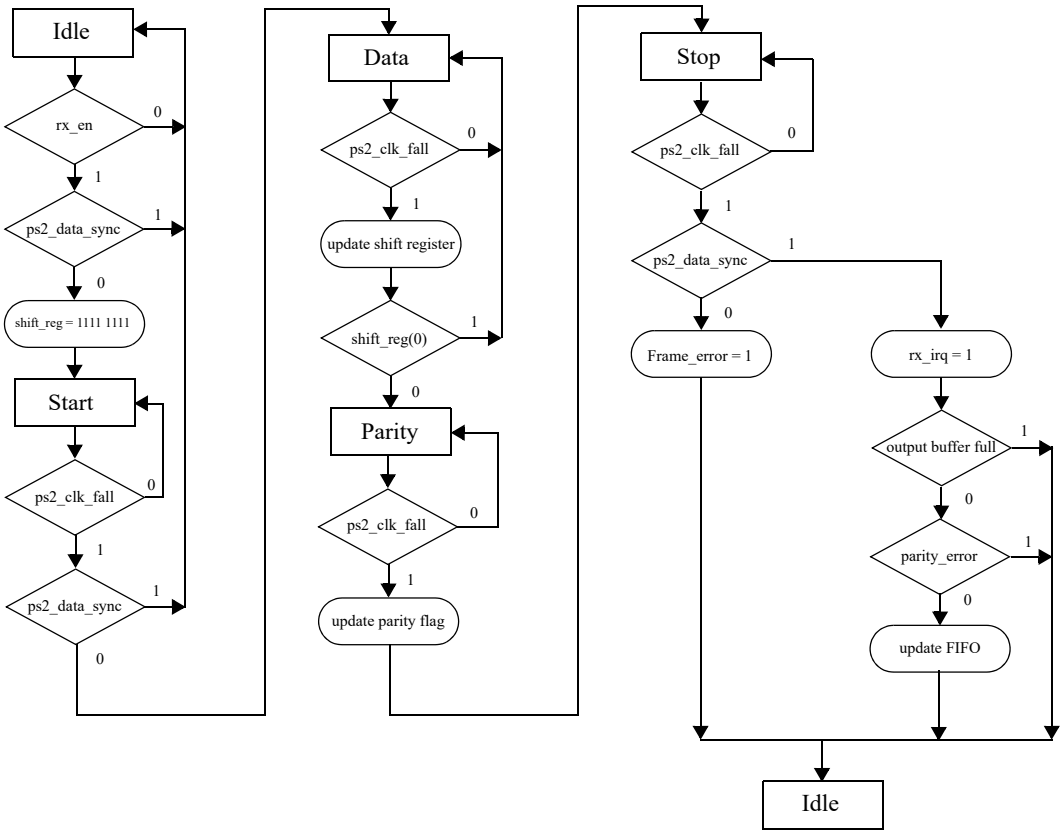


Figure 23. Flow chart for the receiver state machine

16.3 Transmitter operations

The transmitter part of APBPS2 is enabled for through the transmitter enable (TE) bit in the PS/2 control register. The PS/2 interface has a 16 byte transmission FIFO that stores commands sent by the CPU. Commands are used to set the LEDs on the keyboard, and the typematic rate and delay. Typematic rate is the repeat rate of a key that is held down, while the delay controls for how long a key has to be held down before it begins automatically repeating. Typematic repeat rates, delays and possible other commands are listed in table 113.

If the TE bit is set and the transmission FIFO is not empty a transmission of the command will start. The host will pull the clock line low for at least 100 us and then transmit a start bit, the eight bit command, an odd parity bit, a stop bit and wait for an acknowledgement bit by the device. When this happens an interrupt is generated. Figure 24 shows the flow chart for the transmission state machine.

16.4 Clock generation

A PS/2 interface should generate a clock of 10.0 - 16.7 kHz. To transmit data, a PS/2 host must inhibit communication by pulling the clock low for at least 100 microseconds. To do this, APBPS2 divides the APB clock with either a fixed or programmable division factor. The divider consist of a 17-bit down-counter and can divide the APB clock with a factor of 1 - 131071. The division rate, and the reset value of the timer reload register, is set to the *fKHz* generic divided by 10 in order to generate the 100 microsecond clock low time. If the VHDL generic *fixed* is 0, the division rate can be programmed through the timer reload register and should be programmed with the system frequency in kHz divided by ten. The reset value of the reload register is always set to the *fKHz* value divided by ten. However, the register will not be readable via the APB interface unless the *fixed* VHDL generic has been set to 0.

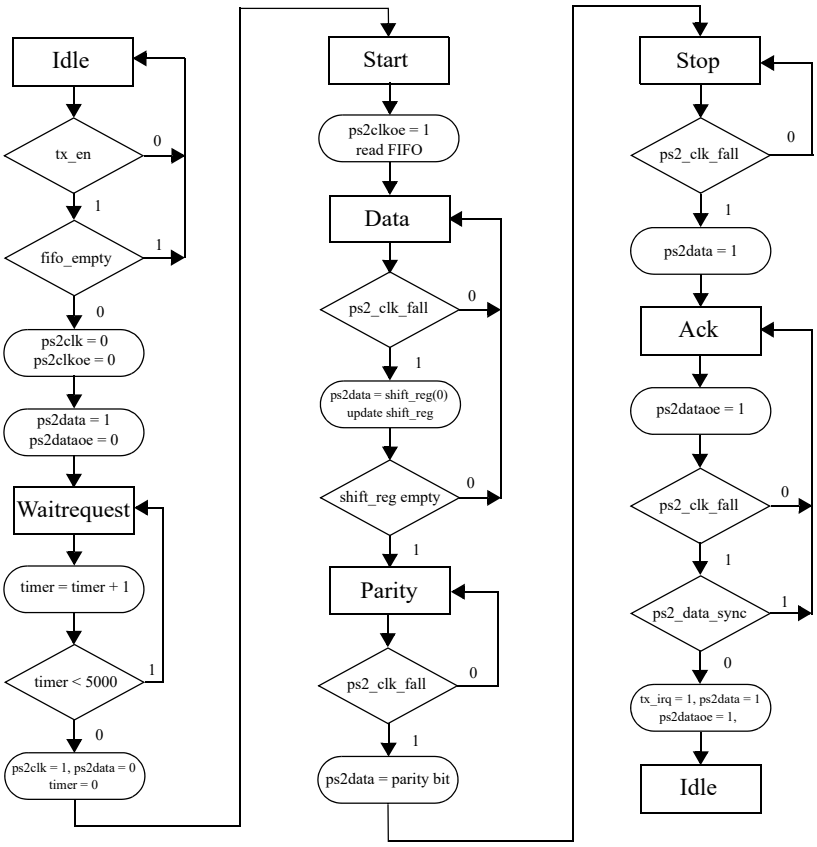


Figure 24. Flow chart for the transmitter state machine

16.5 Registers

The core is controlled through registers mapped into APB address space.

*Table 102.*APB PS/2 registers

APB address offset	Register
0x00	PS/2 Data register
0x04	PS/2 Status register
0x08	PS/2 Control register
0x0C	PS/2 Timer reload register

16.5.1 PS/2 Data Register

*Table 103.*0x00 - DATA - PS/2 data register

31 … 8	7 … 0
RESERVED	DATA
0	NR
r	rw

7: 0 Receiver holding FIFO (read access) and Transmitter holding FIFO (write access). If the receiver FIFO is not empty, read accesses retrieve the next byte from the FIFO. Bytes written to this field are stored in the transmitter holding FIFO if it is not full.

16.5.2 PS/2 Status Register

*Table 104.*0x04 - STAT - PS/2 status register

31 27	26 22	6	5	4	3	2	1	0
RCNT	TCNT	RESERVED	TF	RF	KI	FE	PE	DR
0	0	0	0	0	0	0	0	0
r	r	r	r	r	rw	rw	rw	r

0: Data ready (DR) - indicates that new data is available in the receiver holding register (read only).

1: Parity error (PE) - indicates that a parity error was detected

2: Framing error (FE) - indicates that a framing error was detected.

3: Keyboard inhibit (KI) - indicates that the keyboard is inhibited.

4: Receiver buffer full (RF) - indicates that the output buffer (FIFO) is full (read only).

5: Transmitter buffer full (TF) - indicates that the input buffer (FIFO) is full (read only).

26: 22 Transmit FIFO count (TCNT) - shows the number of data frames in the transmit FIFO (read only).

31: 27 Receiver FIFO count (RCNT) - shows the number of data frames in the receiver FIFO (read only).

16.5.3 PS/2 Control Register

*Table 105.*0x08 - CTRL - PS/2 control register

31 4	3	2	1	0
RESERVED	TI	RI	TE	RE
0	0	0	0	0
r	rw	rw	rw	rw

0: Receiver enable (RE) - if set, enables the receiver.

1: Transmitter enable (TE) - if set, enables the transmitter.

2: Keyboard interrupt enable (RI) - if set, interrupts are generated when a frame is received.

3: Host interrupt enable (TI) - if set, interrupts are generated when a frame is transmitted.

16.5.4 PS/2 Timer Reload Register

*Table 106.*0x0C - TIMER - PS/2 reload register

31 17	16 0
RESERVED	TIMER RELOAD REG
0	*
r	rw*

16: 0 PS/2 timer reload register - Reset value determined by fktlz VHDL generic. Register only present it “fixed” VHDL generic is zero.

16.6 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x060. For a description of vendor and device identifiers see GRLIB IP Library User’s Manual.

16.7 Implementation

16.7.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User’s Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

16.8 Configuration options

Table 107 shows the configuration options of the core (VHDL generics).

*Table 107.*Configuration options

Generic	Function	Allowed range	Default
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	ADDR field of the APB BAR.	0 - 16#FFF#	0
pmask	MASK field of the APB BAR.	0 - 16#FFF#	16#FFF#
pirq	Index of the interrupt line.	0 - NAHBIRQ-1	0
fKHz	Frequency of APB clock in KHz. This value divided by 10 is the reset value of the timer reload register.	1 - 1310710	50000
fixed	Used fixed clock divider to generate PS/2 clock.	0 - 1	0
oepol	Output enable polarity	0 - 1	0

16.9 Signal descriptions

Table 108 shows the interface signals of the core (VHDL ports).

*Table 108.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
PS2I	PS2_CLK_I	Input	PS/2 clock input	-
	PS2_DATA_I	Input	PS/2 data input	-
PS2O	PS2_CLK_O	Output	PS/2 clock output	-
	PS2_CLK_OE	Output	PS/2 clock output enable	Low
	PS2_DATA_O	Output	PS/2 data output	-
	PS2_DATA_OE	Output	PS/2 data output enable	Low

* see GRLIB IP Library User's Manual

16.10 Library dependencies

Table 109 shows libraries used when instantiating the core (VHDL libraries).

*Table 109.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	APB signal definitions
GAISLER	MISC	Signals, component	PS/2 signal and component declaration

16.11 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
```

```
use grlib.amba.all;
use grlib.gencomp.all;

library gaisler;
use gaisler.misc.all;

entity apbps2_ex is
 port (
    rstn : in std_ulogic;
    clk : in std_ulogic;

    -- PS/2 signals
    ps2clk : inout std_ulogic;
    ps2data : inout std_ulogic
    );
end;

architecture rtl of apbuart_ex is

  -- APB signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);

  -- PS/2 signals
  signal kbdi : ps2_in_type;
  signal kbdo : ps2_out_type;

begin

ps20 : apbps2 generic map(pindex => 5, paddr => 5, pirq => 4)
      port map(rstn, clkm, apbi, apbo(5), kbdi, kbdo);

kbdclk_pad : iopad generic map (tech => padtech)
      port map (ps2clk,kbdo.ps2_clk_o, kbdo.ps2_clk_oe, kbdi.ps2_clk_i);

kbdata_pad : iopad generic map (tech => padtech)
        port map (ps2data, kbdo.ps2_data_o, kbdo.ps2_data_oe, kbdi.ps2_data_i);

end;
```

16.12 Keboard scan codes

*Table 110.*Scan code set 2, 104-key keyboard

KEY	MAKE	BREAK	--	KEY	MAKE	BREAK	--	KEY	MAKE	BREAK
A	1C	F0,1C		9	46	F0,46		[	54	FO,54
B	32	F0,32			`0E	F0,0E		INSERT	E0,70	E0,F0,70
C	21	F0,21		-	4E	F0,4E		HOME	E0,6C	E0,F0,6C
D	23	F0,23		=	55	FO,55		PG UP	E0,7D	E0,F0,7D
E	24	F0,24		\	5D	F0,5D		DELETE	E0,71	E0,F0,71
F	2B	F0,2B		BKSP	66	F0,66		END	E0,69	E0,F0,69
G	34	F0,34		SPACE	29	F0,29		PG DN	E0,7A	E0,F0,7A
H	33	F0,33		TAB	0D	F0,0D		U ARROW	E0,75	E0,F0,75
I	43	F0,43		CAPS	58	F0,58		L ARROW	E0,6B	E0,F0,6B
J	3B	F0,3B		L SHFT	12	FO,12		D ARROW	E0,72	E0,F0,72
K	42	F0,42		L CTRL	14	FO,14		R ARROW	E0,74	E0,F0,74
L	4B	F0,4B		L GUI	E0,1F	E0,F0,1F		NUM	77	F0,77
M	3A	F0,3A		L ALT	11	F0,11		KP /	E0,4A	E0,F0,4A
N	31	F0,31		R SHFT	59	F0,59		KP *	7C	F0,7C
O	44	F0,44		R CTRL	E0,14	E0,F0,14		KP -	7B	F0,7B
P	4D	F0,4D		R GUI	E0,27	E0,F0,27		KP +	79	F0,79
Q	15	F0,15		R ALT	E0,11	E0,F0,11		KP EN	E0,5A	E0,F0,5A
R	2D	F0,2D		APPS	E0,2F	E0,F0,2F		KP .	71	F0,71
S	1B	F0,1B		ENTER	5A	F0,5A		KP 0	70	F0,70
T	2C	F0,2C		ESC	76	F0,76		KP 1	69	F0,69
U	3C	F0,3C		F1	5	F0,05		KP 2	72	F0,72
V	2A	F0,2A		F2	6	F0,06		KP 3	7A	F0,7A
W	1D	F0,1D		F3	4	F0,04		KP 4	6B	F0,6B
X	22	F0,22		F4	0C	F0,0C		KP 5	73	F0,73
Y	35	F0,35		F5	3	F0,03		KP 6	74	F0,74
Z	1A	F0,1A		F6	0B	F0,0B		KP 7	6C	F0,6C
0	45	F0,45		F7	83	F0,83		KP 8	75	F0,75
1	16	F0,16		F8	0A	F0,0A		KP 9	7D	F0,7D
2	1E	F0,1E		F9	1	F0,01		]	5B	F0,5B
3	26	F0,26		F10	9	F0,09		;	4C	F0,4C
4	25	F0,25		F11	78	F0,78			52	F0,52
5	2E	F0,2E		F12	7	F0,07		,	41	F0,41
6	36	F0,36		PRNT SCRN	E0,12, E0,7C	E0,F0, 7C,E0, F0,12		.	49	F0,49
7	3D	F0,3D		SCROLL	7E	F0,7E		/	4A	F0,4A
8	3E	F0,3E		PAUSE	E1,14,77, E1,F0,14, F0,77	-NONE-				

*Table 111.*Windows multimedia scan codes

KEY	MAKE	BREAK
Next Track	E0, 4D	E0, F0, 4D
Previous Track	E0, 15	E0, F0, 15
Stop	E0, 3B	E0, F0, 3B
Play/Pause	E0, 34	E0, F0, 34
Mute	E0, 23	E0, F0, 23
Volume Up	E0, 32	E0, F0, 32
Volume Down	E0, 21	E0, F0, 21
Media Select	E0, 50	E0, F0, 50
E-Mail	E0, 48	E0, F0, 48
Calculator	E0, 2B	E0, F0, 2B
My Computer	E0, 40	E0, F0, 40
WWW Search	E0, 10	E0, F0, 10
WWW Home	E0, 3A	E0, F0, 3A
WWW Back	E0, 38	E0, F0, 38
WWW Forward	E0, 30	E0, F0, 30
WWW Stop	E0, 28	E0, F0, 28
WWW Refresh	E0, 20	E0, F0, 20
WWW Favor-ites	E0, 18	E0, F0, 18

*Table 112.*ACPI scan codes (Advanced Configuration and Power Interface)

KEY	MAKE	BREAK
Power	E0, 37	E0, F0, 37
Sleep	E0, 3F	E0, F0, 3F
Wake	E0, 5E	E0, F0, 5E

16.13 Keyboard commands

*Table 113.*Transmit commands:

Command	Description
0xED	Set status LED's - keyboard will reply with ACK (0xFA). The host follows this command with an argument byte*
0xEE	Echo command - expects an echo response
0xF0	Set scan code set - keyboard will reply with ACK (0xFA) and wait for another byte. 0x01-0x03 which determines the scan code set to use. 0x00 returns the current set.
0xF2	Read ID - the keyboard responds by sending a two byte device ID of 0xAB 0x83
0xF3	Set typematic repeat rate - keyboard will reply with ACK (0xFA) and wait for another byte which determines the typematic rate.
0xF4	Keyboard enable - clears the keyboards output buffer, enables keyboard scanning and returns an acknowledgement.
0xF5	Keyboard disable - resets the keyboard, disables keyboard scanning and returns an acknowledgement.
0xF6	Set default - load default typematic rate/delay (10.9cps/500ms) and scan code set 2
0xFE	Resend - upon receipt of the resend command the keyboard will retransmit the last byte
0xFF	Reset - resets the keyboard

* bit 0 controls the scroll lock, bit 1 the num lock, bit 2 the caps lock, bit 3-7 are ignored

*Table 114.*Receive commands:

Command	Description
0xFA	Acknowledge
0xAA	Power on self test passed (BAT completed)
0xEE	Echo respond
0xFE	Resend - upon receipt of the resend command the host should retransmit the last byte
0x00	Error or buffer overflow
0xFF	Error of buffer overflow

*Table 115.*The typematic rate/delay argument byte

MSB							LSB
0	DELAY	DELAY	RATE	RATE	RATE	RATE	RATE

*Table 116.*Typematic repeat rates

Bits 0-4	Rate (cps)	Bits 0-4	Rate (cps)	Bits 0-4	Rate (cps)	Bits 0-4	Rate (cps)
00h	30	08h	15	10h	7.5	18h	3.7
01h	26.7	09h	13.3	11h	6.7	19h	3.3
02h	24	0Ah	12	12h	6	1Ah	3
03h	21.8	0Bh	10.9	13h	5.5	1Bh	2.7
04h	20.7	0Ch	10	14h	5	1Ch	2.5
05h	18.5	0Dh	9.2	15h	4.6	1Dh	2.3
06h	17.1	0Eh	8.6	16h	4.3	1Eh	2.1
07h	16	0Fh	8	17h	4	1Fh	2

*Table 117.*Typematic delays

Bits 5-6	Delay (seconds)
00b	0.25
01b	0.5
10b	0.75
11b	1

17 APBUART - AMBA APB UART Serial Interface

17.1 Overview

The interface is provided for serial communications. The UART supports data frames with 8 data bits, one optional parity bit and one or two stop bits. To generate the bit-rate, each UART has a programmable 12-bit clock divider. Two FIFOs are used for data transfer between the APB bus and UART, when *fifosize* VHDL generic > 1. Two holding registers are used data transfer between the APB bus and UART, when *fifosize* VHDL generic = 1. Hardware flow-control is supported through the RTSN/CTSN hand-shake signals, when *flow* VHDL generic is set. Parity is supported, when *parity* VHDL generic is set.

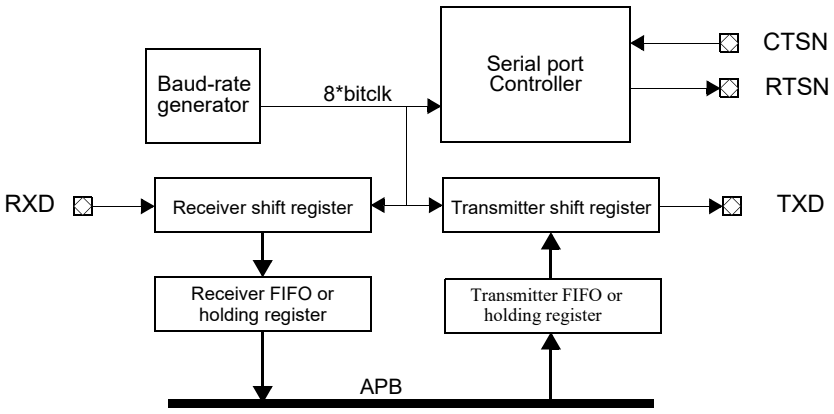


Figure 25. Block diagram

17.2 Operation

17.2.1 Transmitter operation

The transmitter is enabled through the TE bit in the UART control register. Data that is to be transferred is stored in the FIFO/holding register by writing to the data register. This FIFO is configurable to different sizes via the *fifosize* VHDL generic. When the size is 1, only a single holding register is used but in the following discussion both will be referred to as FIFOs. When ready to transmit, data is transferred from the transmitter FIFO/holding register to the transmitter shift register and converted to a serial stream on the transmitter serial output pin (TXD). It automatically sends a start bit followed by eight data bits, an optional parity bit, and one stop bit (figure 26). The least significant bit of the data is sent first. It is also possible to use two stop bits, this is configured via the control register.

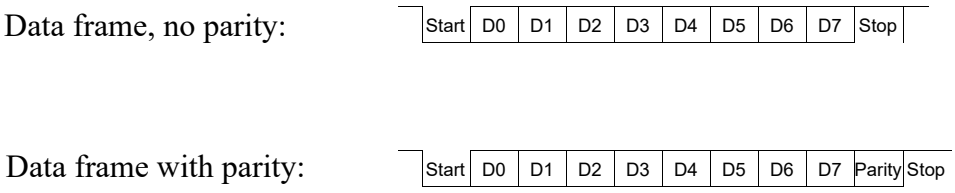


Figure 26. UART data frames

Following the transmission of the stop bit, if a new character is not available in the transmitter FIFO, the transmitter serial data output remains high and the transmitter shift register empty bit (TS) will be set in the UART status register. Transmission resumes and the TS is cleared when a new character is loaded into the transmitter FIFO. When the FIFO is empty the TE bit is set in the status register. If the transmitter is disabled, it will immediately stop any active transmissions including the character currently being shifted out from the transmitter shift register. The transmitter holding register may not be loaded when the transmitter is disabled or when the FIFO (or holding register) is full. If this is done, data might be overwritten and one or more frames are lost.

The discussion above applies to any FIFO configurations including the special case with a holding register (VHDL generic *fifosize* = 1). If FIFOs are used (VHDL generic *fifosize* > 1) some additional status and control bits are available. The TF status bit (not to be confused with the TF control bit) is set if the transmitter FIFO is currently full and the TH bit is set as long as the FIFO is *less* than half-full (less than half of entries in the FIFO contain data). The TF control bit enables FIFO interrupts when set. The status register also contains a counter (TCNT) showing the current number of data entries in the FIFO.

When flow control is enabled, the CTSN input must be low in order for the character to be transmitted. If it is deasserted in the middle of a transmission, the character in the shift register is transmitted and the transmitter serial output then remains inactive until CTSN is asserted again. If the CTSN is connected to a receivers RTSN, overrun can effectively be prevented.

17.2.2 Receiver operation

The receiver is enabled for data reception through the receiver enable (RE) bit in the UART control register. The receiver looks for a high to low transition of a start bit on the receiver serial data input pin. If a transition is detected, the state of the serial input is sampled a half bit clocks later. If the serial input is sampled high the start bit is invalid and the search for a valid start bit continues. If the serial input is still low, a valid start bit is assumed and the receiver continues to sample the serial input at one bit time intervals (at the theoretical centre of the bit) until the proper number of data bits and the parity bit have been assembled and one stop bit has been detected. The serial input is shifted through an 8-bit shift register where all bits have to have the same value before the new value is taken into account, effectively forming a low-pass filter with a cut-off frequency of 1/8 system clock.

The receiver also has a configurable FIFO which is identical to the one in the transmitter. As mentioned in the transmitter part, both the holding register and FIFO will be referred to as FIFO.

During reception, the least significant bit is received first. The data is then transferred to the receiver FIFO and the data ready (DR) bit is set in the UART status register as soon as the FIFO contains at least one data frame. The parity, framing and overrun error bits are set at the received byte boundary, at the same time as the data ready bit would have been set. The data frame is not stored in the FIFO if an error is detected. Also, the new error status bits are or:ed with the old values before they are stored into the status register. Thus, they are not cleared until written to with zeros from the AMBA APB bus. If both the receiver FIFO and shift registers are full when a new start bit is detected, then the

character held in the receiver shift register will be lost and the overrun bit will be set in the UART status register. A break received (BR) is indicated when a BREAK has been received, which is a framing error with all data received being zero.

If flow control is enabled, then the RTSN will be negated (high) when a valid start bit is detected and the receiver FIFO is full. When the holding register is read, the RTSN will automatically be reasserted again.

When the VHDL generic *fifosize* > 1, which means that holding registers are not considered here, some additional status and control bits are available. The RF status bit (not to be confused with the RF control bit) is set when the receiver FIFO is full. The RH status bit is set when the receiver FIFO is half-full (at least half of the entries in the FIFO contain data frames). The RF control bit enables receiver FIFO interrupts when set. A RCNT field is also available showing the current number of data frames in the FIFO.

17.3 Baud-rate generation

Each UART contains a 12-bit down-counting scaler to generate the desired baud-rate, the number of scaler bits can be increased with VHDL generic *sbits*. The scaler is clocked by the system clock and generates a UART tick each time it underflows. It is reloaded with the value of the UART scaler reload register after each underflow. The resulting UART tick frequency should be 8 times the desired baud-rate. One appropriate formula to calculate the scaler value for a desired baud rate, using integer division where the remainder is discarded, is:

*scaler value = (system_clock_frequency) / (baud_rate * 8 + 7).*

To calculate the exact required scaler value use:

*scaler value = (system_clock_frequency) / (baud_rate * 8) - 1*

If the EC bit is set, the ticks will be generated with the same frequency as the external clock input instead of at the scaler underflow rate. In this case, the frequency of external clock must be less than half the frequency of the system clock.

17.4 Loop back mode

If the LB bit in the UART control register is set, the UART will be in loop back mode. In this mode, the transmitter output is internally connected to the receiver input and the RTSN is connected to the CTSN. It is then possible to perform loop back tests to verify operation of receiver, transmitter and associated software routines. In this mode, the outputs remain in the inactive state, in order to avoid sending out data.

17.5 FIFO debug mode

FIFO debug mode is entered by setting the debug mode bit in the control register. In this mode it is possible to read the transmitter FIFO and write the receiver FIFO through the FIFO debug register. The transmitter output is held inactive when in debug mode. A write to the receiver FIFO generates an interrupt if receiver interrupts are enabled.

17.6 Interrupt generation

Interrupts are generated differently when a holding register is used (VHDL generic *fifosize* = 1) and when FIFOs are used (VHDL generic *fifosize* > 1). When holding registers are used, the UART will generate an interrupt under the following conditions: when the transmitter is enabled, the transmitter interrupt is enabled and the transmitter holding register moves from full to empty; when the receiver is enabled, the receiver interrupt is enabled and the receiver holding register moves from empty to full; when the receiver is enabled, the receiver interrupt is enabled and a character with either parity, framing or overrun error is received.

For FIFOs, two different kinds of interrupts are available: normal interrupts and FIFO interrupts. For the transmitter, normal interrupts are generated when transmitter interrupts are enabled (TI), the transmitter is enabled and the transmitter FIFO goes from containing data to being empty. FIFO interrupts are generated when the FIFO interrupts are enabled (TF), transmissions are enabled (TE) and the UART is less than half-full (that is, whenever the TH status bit is set). This is a level interrupt and the interrupt signal is continuously driven high as long as the condition prevails. The receiver interrupts work in the same way. Normal interrupts are generated in the same manner as for the holding register. FIFO interrupts are generated when receiver FIFO interrupts are enabled, the receiver is enabled and the FIFO is half-full. The interrupt signal is continuously driven high as long as the receiver FIFO is half-full (at least half of the entries contain data frames). Note that when using any of the LEON interrupt controllers, the processor acknowledges and clears the corresponding interrupt pending register but as the interrupt signal is continuously driven high another instance of interrupt pending is set in the interrupt controller.

To reduce interrupt occurrence a delayed receiver interrupt is available. It is enabled using the delayed interrupt enable (DI) bit. When enabled a timer is started each time a character is received and an interrupt is only generated if another character has not been received within 4 character + 4 bit times. If receiver FIFO interrupts are enabled a pending character interrupt will be cleared when the FIFO interrupt is active since the character causing the pending irq state is already in the FIFO and is noticed by the driver through the FIFO interrupt. In order to not take one additional interrupt (due to the interrupt signal being driven continuously high as described above), software should clear the corresponding pending bit in the interrupt controller after the FIFO has been emptied.

There is also a separate interrupt for break characters. When enabled an interrupt will always be generated immediately when a break character is received even when delayed receiver interrupts are enabled. When break interrupts are disabled no interrupt will be generated for break characters when delayed interrupts are enabled.

When delayed interrupts are disabled the behavior is the same for the break interrupt bit except that an interrupt will be generated for break characters if receiver interrupt enable is set even if break interrupt is disabled.

An interrupt can also be enabled for the transmitter shift register. When enabled the core will generate an interrupt each time the shift register goes from a non-empty to an empty state.

17.7 Registers

The core is controlled through registers mapped into APB address space.

*Table 118.*UART registers

APB address offset	Register
0x0	UART Data register
0x4	UART Status register
0x8	UART Control register
0xC	UART Scaler register
0x10	UART FIFO debug register

17.7.1 UART Data Register

Table 119. 0x00 - DATA - UART data register

31 … 8	7 … 0
RESERVED	DATA
	NR
	rw

7: 0 Receiver holding register or FIFO (read access)

7: 0 Transmitter holding register or FIFO (write access)

17.7.2 UART Status Register

Table 120. 0x04 - STAT - UART status register

31 … 26	25 … 20	19 … 11	10	9	8	7	6	5	4	3	2	1	0
RCNT	TCNT	RESERVED	RF	TF	RH	TH	FE	PE	OV	BR	TE	TS	DR
0	0	0	0	0	0	0	0	0	0	0	1	1	0
r	r	r	r	r	r	r	rw	rw	rw	rw	r	r	r

31: 26 Receiver FIFO count (RCNT) - shows the number of data frames in the receiver FIFO. Reset: 0

25: 20 Transmitter FIFO count (TCNT) - shows the number of data frames in the transmitter FIFO. Reset: 0

10 Receiver FIFO full (RF) - indicates that the Receiver FIFO is full. Reset: 0

9 Transmitter FIFO full (TF) - indicates that the Transmitter FIFO is full. Reset: 0

8 Receiver FIFO half-full (RH) -indicates that at least half of the FIFO is holding data. Reset: 0

7 Transmitter FIFO half-full (TH) - indicates that the FIFO is less than half-full. Reset: 0

6 Framing error (FE) - indicates that a framing error was detected. Reset: 0

5 Parity error (PE) - indicates that a parity error was detected. Reset: 0

4 Overrun (OV) - indicates that one or more character have been lost due to overrun. Reset: 0

3 Break received (BR) - indicates that a BREAK has been received. Reset: 0

2 Transmitter FIFO empty (TE) - indicates that the transmitter FIFO is empty. Reset: 1

1 Transmitter shift register empty (TS) - indicates that the transmitter shift register is empty. Reset: 1

0 Data ready (DR) - indicates that new data is available in the receiver holding register. Reset: 0

17.7.3 UART Control Register

Table 121. UART control register

31	30	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FA	RESERVED		NS	SI	DI	BI	DB	RF	TF	EC	LB	FL	PE	PS	TI	RI	TE	RE
0		0	NR	NR	NR	NR	NR	NR	NR	0	NR	0	NR	NR	NR	NR	0	0
r		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

31 FIFOs available (FA) - Set to 1 when receiver and transmitter FIFOs are available. When 0, only holding register are available.

30: 16 RESERVED

15 Number of stop bits (NS) - When set to '1' then two stop bits will be used, otherwise one stop bit will be used.

14 Transmitter shift register empty interrupt enable (SI) - When set, an interrupt will be generated when the transmitter shift register becomes empty. See section 17.6 for more details.

13 Delayed interrupt enable (DI) - When set, delayed receiver interrupts will be enabled and an interrupt will only be generated for received characters after a delay of 4 character times + 4 bits if no new character has been received during that interval. This is only applicable if receiver interrupt enable is set. See section 17.6 for more details.

12 Break interrupt enable (BI) - When set, an interrupt will be generated each time a break character is received. See section 16.6 for more details.

11 FIFO debug mode enable (DB) - when set, it is possible to read and write the FIFO debug register.

10 Receiver FIFO interrupt enable (RF) - when set, Receiver FIFO level interrupts are enabled.

9 Transmitter FIFO interrupt enable (TF) - when set, Transmitter FIFO level interrupts are enabled.

8 External Clock (EC) - if set, the UART scaler will be clocked by UARTI.EXTCLK.

7 Loop back (LB) - if set, loop back mode will be enabled.

6 Flow control (FL) - if set, enables flow control using CTS/RTS (when implemented).

5 Parity enable (PE) - if set, enables parity generation and checking (when implemented).

4 Parity select (PS) - selects parity polarity (0 = even parity, 1 = odd parity) (when implemented).

3 Transmitter interrupt enable (TI) - if set, interrupts are generated when characters are transmitted (see section 17.6 for details).

2 Receiver interrupt enable (RI) - if set, interrupts are generated when characters are received (see section 17.6 for details).

1 Transmitter enable (TE) - if set, enables the transmitter.

0 Receiver enable (RE) - if set, enables the receiver.

17.7.4 UART Scaler Register

*Table 122.*0x0C - SCALER - UART scaler reload register

31 sbits	sbits-1 0
RESERVED	SCALER RELOAD VALUE
0	NR
r	rw

sbits-1:0 Scaler reload value

17.7.5 UART FIFO Debug Register

Table 123. 0x10 - DEBUG - UART FIFO debug register

31 8	7 0
RESERVED	DATA
0	NR
r	rw

7: 0 Transmitter holding register or FIFO (read access)

7: 0 Receiver holding register or FIFO (write access)

17.8 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x00C. For a description of vendor and device identifiers see GRLIB IP Library User's Manual.

17.9 Implementation

17.9.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support *grlib_async_reset_enable*. All registers that react on the reset signal will have a synchronous reset.

17.10 Configuration options

Table 124 shows the configuration options of the core (VHDL generics).

*Table 124.*Configuration options

Generic	Function	Allowed range	Default
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	ADDR field of the APB BAR.	0 - 16#FFF#	0
pmask	MASK field of the APB BAR.	0 - 16#FFF#	16#FFF#
console	Prints output from the UART on console during VHDL simulation and speeds up simulation by always returning '1' for Data Ready bit of UART Status register. Does not affect synthesis.	0 - 1	0
pirq	Index of the interrupt line.	0 - NAHBIRQ-1	0
parity	Enables parity	0 - 1	1
flow	Enables flow control. Flow control must be implemented for FIFO debug mode to be supported. Setting this generic to 0 also disables FIFO debug mode.	0 - 1	1
fifosize	Selects the size of the Receiver and Transmitter FIFOs	1, 2, 4, 8, 16, 32	1
abits	Selects the number of APB address bits used to decode the register addresses	3 - 8	8
sbits	Selects the number of bits in the scaler	12-32	12

17.11 Signal descriptions

Table 125 shows the interface signals of the core (VHDL ports).

*Table 125.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
UARTI	RXD	Input	UART receiver data	-
	CTSN	Input	UART clear-to-send	Low
	EXTCLK	Input	Use as alternative UART clock	-
UARTO	RTSN	Output	UART request-to-send	Low
	TXD	Output	UART transmit data	-
	SCALER	Output	UART scaler value	-
	TXEN	Output	Output enable for transmitter	High
	FLOW	Output	Unused	-
	RXEN	Output	Receiver enable	High

* see GRLIB IP Library User's Manual

17.12 Signal definitions and reset values

The signals and their reset values are described in table 126.

*Table 126.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
txd[]	Output	UART transmit data line	-	Logical 1
rtsn[]	Output	Ready To Send	Low	Logical 1
rxd[]	Input	UART receive data line	-	-
ctsn[]	Input	Clear To Send	Low	-

17.13 Timing

The timing waveforms and timing parameters are shown in figure 27 and are defined in table 127.

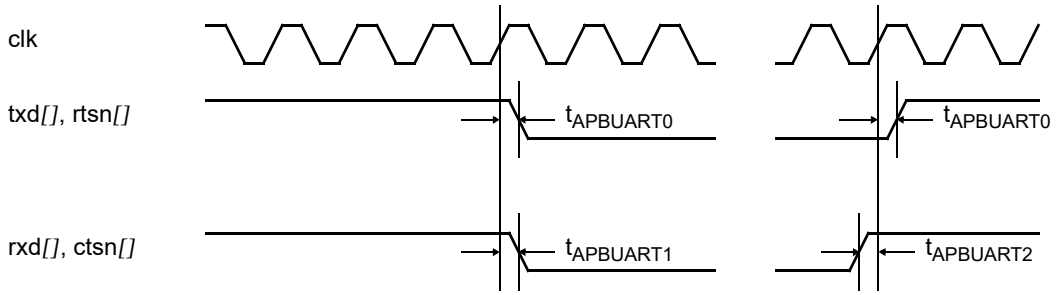


Figure 27. Timing waveforms

*Table 127.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{APBUART0}$	clock to output delay	rising *clk* edge	TBD	TBD	ns
$t_{APBUART1}$	input to clock hold	rising *clk* edge	-	-	ns
$t_{APBUART2}$	input to clock setup	rising *clk* edge	-	-	ns

Note: The *ctsn[]* and *rxd[]* inputs are re-synchronized internally. These signals do not have to meet any setup or hold requirements.

17.14 Library dependencies

Table 128 shows libraries that should be used when instantiating the core.

*Table 128.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	APB signal definitions
GAISLER	UART	Signals, component	Signal and component declaration

17.15 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.uart.all;

entity apbuart_ex is
  port (
    clk : in std_ulogic;
    rstn : in std_ulogic;

    -- UART signals
    rxd   : in  std_ulogic;
    txd   : out std_ulogic
    );
end;

architecture rtl of apbuart_ex is
```

```
  -- APB signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);

  -- UART signals
  signal uarti : uart_in_type;
  signal uarto : uart_out_type;

begin

  -- AMBA Components are instantiated here
   ...


  -- APB UART
  uart0 : apbuart
  generic map (pindex => 1, paddr => 1,  pirq => 2,
console => 1, fifosize => 1)
  port map (rstn, clk, apbi, apbo(1), uarti, uarto);

  -- UART input data
  uarti.rxd <= rxd;

  -- APB UART inputs not used in this configuration
  uarti.ctsn <= '0'; uarti.extclk <= '0';

  -- connect APB UART output to entity output signal
  txd <= uarto.txd;

end;
```

18 APBVGA - VGA controller with APB interface

18.1 Introduction

The APBVGA core is a text-only video controller with a resolution of 640x480 pixels, creating a display of 80x37 characters. The controller consists of a video signal generator, a 4 Kbyte text buffer, and a ROM for character pixel information. The video controller is controlled through an APB interface.

A block diagram for the data path is shown in figure 28.

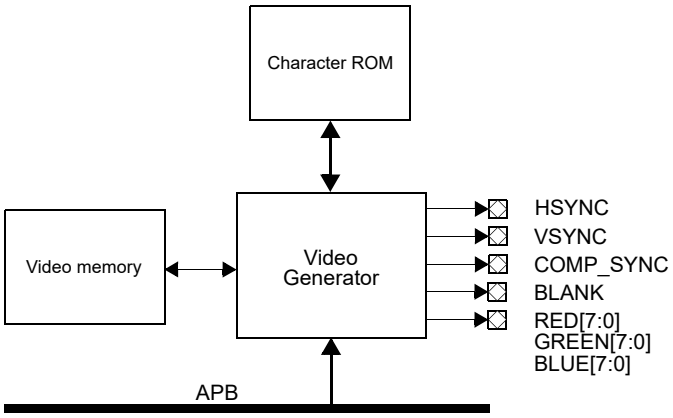


Figure 28. APBVGA block diagram

18.2 Operation

The video timing of APBVGA is fixed to generate a 640x480 display with 60 Hz refresh rate. The text font is encoded using 8x13 pixels. The display is created by scanning a segment of 2960 characters of the 4 Kbyte text buffer, rasterizing the characters using the character ROM, and sending the pixel data to an external video DAC using three 8-bit color channels. The required pixel clock is 25.175 MHz, which should be provided on the VGACLK input.

Writing to the video memory is made through the VGA data register. Bits [7:0] contains the character to be written, while bits [19:8] defines the text buffer address. Foreground and background colours are set through the background and foreground registers. These 24 bits corresponds to the three pixel colors, RED, GREEN and BLUE. The eight most significant bits defines the red intensity, the next eight bits defines the green intensity and the eight least significant bits defines the blue intensity. Maximum intensity for a color is received when all eight bits are set and minimum intensity when none of the bits are set. Changing the foreground color results in that all characters change their color, it is not possible to just change the color of one character. In addition to the color channels, the video controller generates HSYNC, VSYNC, CSYNC and BLANK. Togetherm the signals are suitable to drive an external video DAC such as ADV7125 or similar.

APBVGA implements hardware scrolling to minimize processor overhead. The controller monitors maintains a reference pointer containing the buffer address of the first character on the top-most line. When the text buffer is written with an address larger than the reference pointer + 2960, the pointer is incremented with 80. The 4 Kbyte text buffer is sufficient to buffer 51 lines of 80 characters. To simplify hardware design, the last 16 bytes (4080 - 4095) should not be written. When address 4079 has been written, the software driver should wrap to address 0. Sofware scrolling can be implemented by only using the first 2960 address in the text buffer, thereby never activating the hardware scolling mechanism.

18.3 Registers

The APB VGA is controlled through three registers mapped into APB address space.

*Table 129.*APB VGA registers

APB address offset	Register
0x0	VGA Data register (write-only, reads will return 0x00000000).
0x4	VGA Background color (write-only, reads will return 0x00000000).
0x8	VGA Foreground color (write-only, reads will return 0x00000000).

18.3.1 VGA Data Register

Table 130. 0x00 - DATA - VGA data register

31 20	19 8	7 0
RESERVED	ADDRESS	DATA
0	0	0
r	w	w

19: 8 Video memory address (write access)

7: 0 Video memory data (write access)

18.3.2 VGA Background Color

Table 131. 0x04 - BGCOL - VGA background register

31 24	23 16	15 8	7 0
RESERVED	RED	GREEN	BLUE
0			
r	w	w	w

23: 16 Video background color red.

15: 8 Video background color green.

7: 0 Video background color blue.

18.3.3 VGA Foreground Color

Table 132. 0x00 - FGCOL - VGA foreground register

31 24	23 16	15 8	7 0
RESERVED	RED	GREEN	BLUE
0			
r	w	w	w

23: 16 Video foreground color red.

15: 8 Video foreground color green.

7: 0 Video foreground color blue.

18.4 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x061. For a description of vendor and device identifiers see GRLIB IP Library User's Manual.

18.5 Implementation

18.5.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

18.6 Configuration options

Table 133 shows the configuration options of the core (VHDL generics).

*Table 133.*Configuration options

Generic	Function	Allowed range	Default
memtech	Technology to implement on-chip RAM	0 - NTECH	2
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	ADDR field of the APB BAR.	0 - 16#FFF#	0
pmask	MASK field of the APB BAR.	0 - 16#FFF#	16#FFF#

18.7 Signal descriptions

Table 134 shows the interface signals of the core (VHDL ports).

*Table 134.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
VGACLK	N/A	Input	VGA Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
VGAO	HSYNC	Output	Horizontal synchronization	High
	VSYNC		Vertical synchronization	High
	COMP_SYNC		Composite synchronization	Low
	BLANK		Blanking	Low
	VIDEO_OUT_R[7:0]		Video out, color red	-
	VIDEO_OUT_G[7:0]		Video out, color green	-
	VIDEO_OUT_B[7:0]		Video out, color blue	-
	BITDEPTH[1:0]		Constant High	-

* see GRLIB IP Library User's Manual

18.8 Library dependencies

Table 135 shows libraries used when instantiating the core (VHDL libraries).

*Table 135.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	APB signal definitions
GAISLER	MISC	Signals, component	VGA signal and component declaration

18.9 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.misc.all;

.
.


architecture rtl of apbuart_ex is

signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
signal vgao  : apbvga_out_type;

begin
  -- AMBA Components are instantiated here
   ...

  -- APB VGA
  vga0 : apbvga
  generic map (memtech => 2, pindex => 6, paddr => 6)
  port map (rstn, clk, vgaclk, apbi, apbo(6), vgao);
end;
```

19 CAN_OC - GRLIB wrapper for OpenCores CAN Interface core

19.1 Overview

CAN_OC is GRLIB wrapper for the CAN core from Opencores. It provides a bridge between AMBA AHB and the CAN Core registers. The AHB slave interface is mapped in the AHB I/O space using the GRLIB plug&play functionality. The CAN core interrupt is routed to the AHB interrupt bus, and the interrupt number is selected through the *irq* generic. The FIFO RAM in the CAN core is implemented using the GRLIB parametrizable SYNCRAM_2P memories, assuring portability to all supported technologies.

This CAN interface implements the CAN 20.A and 2.0B protocols. It is based on the Philips SJA1000 and has a compatible register map with a few exceptions.

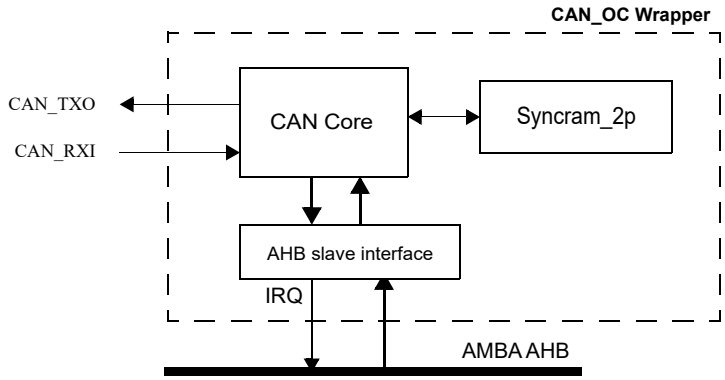


Figure 29. Block diagram

19.2 Opencores CAN controller overview

This CAN controller is based on the Philips SJA1000 and has a compatible register map with a few exceptions. It also supports both BasicCAN (PCA82C200 like) and PeliCAN mode. In PeliCAN mode the extended features of CAN 2.0B is supported. The mode of operation is chosen through the Clock Divider register.

This document will list the registers and their functionality. The Philips SJA1000 data sheet can be used as a reference if something needs clarification. See also the Design considerations chapter for differences between this core and the SJA1000.

The register map and functionality is different between the two modes of operation. First the Basic-CAN mode will be described followed by PeliCAN. Common registers (clock divisor and bus timing) are described in a separate chapter. The register map also differs depending on whether the core is in operating mode or in reset mode. When reset the core starts in reset mode awaiting configuration. Operating mode is entered by clearing the reset request bit in the command register. To re-enter reset mode set this bit high again.

19.3 AHB interface

All registers are one byte wide and the addresses specified in this document are byte addresses. Byte reads and writes should be used when interfacing with this core. The read byte is duplicated on all byte lanes of the AHB bus. The wrapper is big endian so the core expects the MSB at the lowest address.

The bit numbering in this document uses bit 7 as MSB and bit 0 as LSB.

The core is designed for big-endian systems.

19.4 BasicCAN mode

19.4.1 BasicCAN register map

*Table 136.*BasicCAN address allocation

Address	Operating mode		Reset mode	
	Read	**Write**	**Read**	**Write**
0	Control	Control	Control	Control
1	(0xFF)	Command	(0xFF)	Command
2	Status	-	Status	-
3	Interrupt	-	Interrupt	-
4	(0xFF)	-	Acceptance code	Acceptance code
5	(0xFF)	-	Acceptance mask	Acceptance mask
6	(0xFF)	-	Bus timing 0	Bus timing 0
7	(0xFF)	-	Bus timing 1	Bus timing 1
8	(0x00)	-	(0x00)	-
9	(0x00)	-	(0x00)	-
10	TX id1	TX id1	(0xFF)	-
11	TX id2, rtr, dlc	TX id2, rtr, dlc	(0xFF)	-
12	TX data byte 1	TX data byte 1	(0xFF)	-
13	TX data byte 2	TX data byte 2	(0xFF)	-
14	TX data byte 3	TX data byte 3	(0xFF)	-
15	TX data byte 4	TX data byte 4	(0xFF)	-
16	TX data byte 5	TX data byte 5	(0xFF)	-
17	TX data byte 6	TX data byte 6	(0xFF)	-
18	TX data byte 7	TX data byte 7	(0xFF)	-
19	TX data byte 8	TX data byte 8	(0xFF)	-
20	RX id1	-	RX id1	-
21	RX id2, rtr, dlc	-	RX id2, rtr, dlc	-
22	RX data byte 1	-	RX data byte 1	-
23	RX data byte 2	-	RX data byte 2	-
24	RX data byte 3	-	RX data byte 3	-
25	RX data byte 4	-	RX data byte 4	-
26	RX data byte 5	-	RX data byte 5	-
27	RX data byte 6	-	RX data byte 6	-
28	RX data byte 7	-	RX data byte 7	-
29	RX data byte 8	-	RX data byte 8	-
30	(0x00)	-	(0x00)	-
31	Clock divider	Clock divider	Clock divider	Clock divider

19.4.2 Control register

The control register contains interrupt enable bits as well as the reset request bit.

*Table 137.*Bit interpretation of control register (CR) (address 0)

Bit	Name	Description
CR.7	-	reserved
CR.6	-	reserved
CR.5	-	reserved (reads as 1)
CR.4	Overrun Interrupt Enable	1 - enabled, 0 - disabled
CR.3	Error Interrupt Enable	1 - enabled, 0 - disabled
CR.2	Transmit Interrupt Enable	1 - enabled, 0 - disabled
CR.1	Receive Interrupt Enable	1 - enabled, 0 - disabled
CR.0	Reset request	Writing 1 to this bit aborts any ongoing transfer and enters reset mode. Writing 0 returns to operating mode.

19.4.3 Command register

Writing a one to the corresponding bit in this register initiates an action supported by the core.

*Table 138.*Bit interpretation of command register (CMR) (address 1)

Bit	Name	Description
CMR.7	-	reserved
CMR.6	-	reserved
CMR.5	-	reserved
CMR.4	-	not used (go to sleep in SJA1000 core)
CMR.3	Clear data overrun	Clear the data overrun status bit
CMR.2	Release receive buffer	Free the current receive buffer for new reception
CMR.1	Abort transmission	Aborts a not yet started transmission.
CMR.0	Transmission request	Starts the transfer of the message in the TX buffer

A transmission is started by writing 1 to CMR.0. It can only be aborted by writing 1 to CMR.1 and only if the transfer has not yet started. If the transmission has started it will not be aborted when setting CMR.1 but it will not be retransmitted if an error occurs.

Giving the Release receive buffer command should be done after reading the contents of the receive buffer in order to release this memory. If there is another message waiting in the FIFO a new receive interrupt will be generated (if enabled) and the receive buffer status bit will be set again.

To clear the Data overrun status bit CMR.3 must be written with 1.

19.4.4 Status register

The status register is read only and reflects the current status of the core.

*Table 139.*Bit interpretation of status register (SR) (address 2)

Bit	Name	Description
SR.7	Bus status	1 when the core is in bus-off and not involved in bus activities
SR.6	Error status	At least one of the error counters have reached or exceeded the CPU warning limit (96).
SR.5	Transmit status	1 when transmitting a message
SR.4	Receive status	1 when receiving a message
SR.3	Transmission complete	1 indicates the last message was successfully transferred.
SR.2	Transmit buffer status	1 means CPU can write into the transmit buffer
SR.1	Data overrun status	1 if a message was lost because no space in fifo.
SR.0	Receive buffer status	1 if messages available in the receive fifo.

Receive buffer status is cleared when the Release receive buffer command is given and set high if there are more messages available in the fifo.

The data overrun status signals that a message which was accepted could not be placed in the fifo because not enough space left. NOTE: This bit differs from the SJA1000 behavior and is set first when the fifo has been read out.

When the transmit buffer status is high the transmit buffer is available to be written into by the CPU. During an on-going transmission the buffer is locked and this bit is 0.

The transmission complete bit is set to 0 when a transmission request has been issued and will not be set to 1 again until a message has successfully been transmitted.

19.4.5 Interrupt register

The interrupt register signals to CPU what caused the interrupt. The interrupt bits are only set if the corresponding interrupt enable bit is set in the control register.

*Table 140.*Bit interpretation of interrupt register (IR) (address 3)

Bit	Name	Description
IR.7	-	reserved (reads as 1)
IR.6	-	reserved (reads as 1)
IR.5	-	reserved (reads as 1)
IR.4	-	not used (wake-up interrupt of SJA1000)
IR.3	Data overrun interrupt	Set when SR.1 goes from 0 to 1.
IR.2	Error interrupt	Set when the error status or bus status are changed.
IR.1	Transmit interrupt	Set when the transmit buffer is released (status bit 0->1)
IR.0	Receive interrupt	This bit is set while there are more messages in the fifo.

This register is reset on read with the exception of IR.0. Note that this differs from the SJA1000 behavior where all bits are reset on read in BasicCAN mode. This core resets the receive interrupt bit when the release receive buffer command is given (like in PeliCAN mode).

Also note that bit IR.5 through IR.7 reads as 1 but IR.4 is 0.

19.4.6 Transmit buffer

The table below shows the layout of the transmit buffer. In BasicCAN only standard frame messages can be transmitted and received (EFF messages on the bus are ignored).

*Table 141.*Transmit buffer layout

Addr	Name	Bits							
		7	6	5	4	3	2	1	0
10	ID byte 1	ID.10	ID.9	ID.8	ID.7	ID.6	ID.5	ID.4	ID.3
11	ID byte 2	ID.2	ID.1	ID.0	RTR	DLC.3	DLC.2	DLC.1	DLC.0
12	TX data 1	TX byte 1							
13	TX data 2	TX byte 2							
14	TX data 3	TX byte 3							
15	TX data 4	TX byte 4							
16	TX data 5	TX byte 5							
17	TX data 6	TX byte 6							
18	TX data 7	TX byte 7							
19	TX data 8	TX byte 8							

If the RTR bit is set no data bytes will be sent but DLC is still part of the frame and must be specified according to the requested frame. Note that it is possible to specify a DLC larger than 8 bytes but should not be done for compatibility reasons. If DLC > 8 still only 8 bytes can be sent.

19.4.7 Receive buffer

The receive buffer on address 20 through 29 is the visible part of the 64 byte RX FIFO. Its layout is identical to that of the transmit buffer.

19.4.8 Acceptance filter

Messages can be filtered based on their identifiers using the acceptance code and acceptance mask registers. The top 8 bits of the 11 bit identifier are compared with the acceptance code register only comparing the bits set to zero in the acceptance mask register. If a match is detected the message is stored to the fifo.

19.5 PeliCAN mode

19.5.1 PeliCAN register map

*Table 142.*PeliCAN address allocation

#	Operating mode				Reset mode	
	Read		**Write**		**Read**	**Write**
0	Mode		Mode		Mode	Mode
1	(0x00)		Command		(0x00)	Command
2	Status		-		Status	-
3	Interrupt		-		Interrupt	-
4	Interrupt enable		Interrupt enable		Interrupt enable	Interrupt enable
5	reserved (0x00)		-		reserved (0x00)	-
6	Bus timing 0		-		Bus timing 0	Bus timing 0
7	Bus timing 1		-		Bus timing 1	Bus timing 1
8	(0x00)		-		(0x00)	-
9	(0x00)		-		(0x00)	-
10	reserved (0x00)		-		reserved (0x00)	-
11	Arbitration lost capture		-		Arbitration lost capture	-
12	Error code capture		-		Error code capture	-
13	Error warning limit		-		Error warning limit	Error warning limit
14	RX error counter		-		RX error counter	RX error counter
15	TX error counter		-		TX error counter	TX error counter
16	RX FI SFF	RX FI EFF	TX FI SFF	TX FI EFF	Acceptance code 0	Acceptance code 0
17	RX ID 1	RX ID 1	TX ID 1	TX ID 1	Acceptance code 1	Acceptance code 1
18	RX ID 2	RX ID 2	TX ID 2	TX ID 2	Acceptance code 2	Acceptance code 2
19	RX data 1	RX ID 3	TX data 1	TX ID 3	Acceptance code 3	Acceptance code 3
20	RX data 2	RX ID 4	TX data 2	TX ID 4	Acceptance mask 0	Acceptance mask 0
21	RX data 3	RX data 1	TX data 3	TX data 1	Acceptance mask 1	Acceptance mask 1
22	RX data 4	RX data 2	TX data 4	TX data 2	Acceptance mask 2	Acceptance mask 2
23	RX data 5	RX data 3	TX data 5	TX data 3	Acceptance mask 3	Acceptance mask 3
24	RX data 6	RX data 4	TX data 6	TX data 4	reserved (0x00)	-
25	RX data 7	RX data 5	TX data 7	TX data 5	reserved (0x00)	-
26	RX data 8	RX data 6	TX data 8	TX data 6	reserved (0x00)	-
27	FIFO	RX data 7	-	TX data 7	reserved (0x00)	-
28	FIFO	RX data 8	-	TX data 8	reserved (0x00)	-
29	RX message counter		-		RX msg counter	-
30	(0x00)		-		(0x00)	-
31	Clock divider		Clock divider		Clock divider	Clock divider

The transmit and receive buffers have different layout depending on if standard frame format (SFF) or extended frame format (EFF) is to be transmitted/received. See the specific section below.

19.5.2 Mode register

*Table 143.*Bit interpretation of mode register (MOD) (address 0)

Bit	Name	Description
MOD.7	-	reserved
MOD.6	-	reserved
MOD.5	-	reserved
MOD.4	-	not used (sleep mode in SJA1000)
MOD.3	Acceptance filter mode	1 - single filter mode, 0 - dual filter mode
MOD.2	Self test mode	If set the controller is in self test mode
MOD.1	Listen only mode	If set the controller is in listen only mode
MOD.0	Reset mode	Writing 1 to this bit aborts any ongoing transfer and enters reset mode. Writing 0 returns to operating mode

Writing to MOD.1-3 can only be done when reset mode has been entered previously.

In Listen only mode the core will not send any acknowledgements. Note that unlike the SJA1000 the Opencores core does not become error passive and active error frames are still sent!

When in Self test mode the core can complete a successful transmission without getting an acknowledgement if given the Self reception request command. Note that the core must still be connected to a real bus, it does not do an internal loopback.

19.5.3 Command register

Writing a one to the corresponding bit in this register initiates an action supported by the core.

*Table 144.*Bit interpretation of command register (CMR) (address 1)

Bit	Name	Description
CMR.7	-	reserved
CMR.6	-	reserved
CMR.5	-	reserved
CMR.4	Self reception request	Transmits and simultaneously receives a message
CMR.3	Clear data overrun	Clears the data overrun status bit
CMR.2	Release receive buffer	Free the current receive buffer for new reception
CMR.1	Abort transmission	Aborts a not yet started transmission.
CMR.0	Transmission request	Starts the transfer of the message in the TX buffer

A transmission is started by writing 1 to CMR.0. It can only be aborted by writing 1 to CMR.1 and only if the transfer has not yet started. Setting CMR.0 and CMR.1 simultaneously will result in a so called single shot transfer, i.e. the core will not try to retransmit the message if not successful the first time.

Giving the Release receive buffer command should be done after reading the contents of the receive buffer in order to release this memory. If there is another message waiting in the FIFO a new receive interrupt will be generated (if enabled) and the receive buffer status bit will be set again.

The Self reception request bit together with the self test mode makes it possible to do a self test of the core without any other cores on the bus. A message will simultaneously be transmitted and received and both receive and transmit interrupt will be generated.

19.5.4 Status register

The status register is read only and reflects the current status of the core.

*Table 145.*Bit interpretation of command register (SR) (address 2)

Bit	Name	Description
SR.7	Bus status	1 when the core is in bus-off and not involved in bus activities
SR.6	Error status	At least one of the error counters have reached or exceeded the error warning limit.
SR.5	Transmit status	1 when transmitting a message
SR.4	Receive status	1 when receiving a message
SR.3	Transmission complete	1 indicates the last message was successfully transferred.
SR.2	Transmit buffer status	1 means CPU can write into the transmit buffer
SR.1	Data overrun status	1 if a message was lost because no space in fifo.
SR.0	Receive buffer status	1 if messages available in the receive fifo.

Receive buffer status is cleared when there are no more messages in the fifo. The data overrun status signals that a message which was accepted could not be placed in the fifo because not enough space left. NOTE: This bit differs from the SJA1000 behavior and is set first when the fifo has been read out.

When the transmit buffer status is high the transmit buffer is available to be written into by the CPU. During an on-going transmission the buffer is locked and this bit is 0.

The transmission complete bit is set to 0 when a transmission request or self reception request has been issued and will not be set to 1 again until a message has successfully been transmitted.

19.5.5 Interrupt register

The interrupt register signals to CPU what caused the interrupt. The interrupt bits are only set if the corresponding interrupt enable bit is set in the interrupt enable register.

*Table 146.*Bit interpretation of interrupt register (IR) (address 3)

Bit	Name	Description
IR.7	Bus error interrupt	Set if an error on the bus has been detected
IR.6	Arbitration lost interrupt	Set when the core has lost arbitration
IR.5	Error passive interrupt	Set when the core goes between error active and error passive
IR.4	-	not used (wake-up interrupt of SJA1000)
IR.3	Data overrun interrupt	Set when data overrun status bit is set
IR.2	Error warning interrupt	Set on every change of the error status or bus status
IR.1	Transmit interrupt	Set when the transmit buffer is released
IR.0	Receive interrupt	Set while the fifo is not empty.

This register is reset on read with the exception of IR.0 which is reset when the fifo has been emptied.

19.5.6 Interrupt enable register

In the interrupt enable register the separate interrupt sources can be enabled/disabled. If enabled the corresponding bit in the interrupt register can be set and an interrupt generated.

*Table 147.*Bit interpretation of interrupt enable register (IER) (address 4)

Bit	Name	Description
IR.7	Bus error interrupt	1 - enabled, 0 - disabled
IR.6	Arbitration lost interrupt	1 - enabled, 0 - disabled
IR.5	Error passive interrupt	1 - enabled, 0 - disabled
IR.4	-	not used (wake-up interrupt of SJA1000)
IR.3	Data overrun interrupt	1 - enabled, 0 - disabled
IR.2	Error warning interrupt	1 - enabled, 0 - disabled.
IR.1	Transmit interrupt	1 - enabled, 0 - disabled
IR.0	Receive interrupt	1 - enabled, 0 - disabled

19.5.7 Arbitration lost capture register

*Table 148.*Bit interpretation of arbitration lost capture register (ALC) (address 11)

Bit	Name	Description
ALC.7-5	-	reserved
ALC.4-0	Bit number	Bit where arbitration is lost

When the core loses arbitration the bit position of the bit stream processor is captured into arbitration lost capture register. The register will not change content again until read out.

19.5.8 Error code capture register

*Table 149.*Bit interpretation of error code capture register (ECC) (address 12)

Bit	Name	Description
ECC.7-6	Error code	Error code number
ECC.5	Direction	1 - Reception, 0 - transmission error
ECC.4-0	Segment	Where in the frame the error occurred

When a bus error occurs the error code capture register is set according to what kind of error occurred, if it was while transmitting or receiving and where in the frame it happened. As with the ALC register the ECC register will not change value until it has been read out. The table below shows how to interpret bit 7-6 of ECC.

*Table 150.*Error code interpretation

ECC.7-6	Description
0	Bit error
1	Form error
2	Stuff error
3	Other

Bit 4 downto 0 of the ECC register is interpreted as below

*Table 151.*Bit interpretation of ECC.4-0

ECC.4-0	Description
0x03	Start of frame
0x02	ID.28 - ID.21
0x06	ID.20 - ID.18
0x04	Bit SRTR
0x05	Bit IDE
0x07	ID.17 - ID.13
0x0F	ID.12 - ID.5
0x0E	ID.4 - ID.0
0x0C	Bit RTR
0x0D	Reserved bit 1
0x09	Reserved bit 0
0x0B	Data length code
0x0A	Data field
0x08	CRC sequence
0x18	CRC delimiter
0x19	Acknowledge slot
0x1B	Acknowledge delimiter
0x1A	End of frame
0x12	Intermission
0x11	Active error flag
0x16	Passive error flag
0x13	Tolerate dominant bits
0x17	Error delimiter
0x1C	Overload flag

19.5.9 Error warning limit register

This registers allows for setting the CPU error warning limit. It defaults to 96. Note that this register is only writable in reset mode.

19.5.10 RX error counter register (address 14)

This register shows the value of the rx error counter. It is writable in reset mode. A bus-off event resets this counter to 0.

19.5.11 TX error counter register (address 15)

This register shows the value of the tx error counter. It is writable in reset mode. If a bus-off event occurs this register is initialized as to count down the protocol defined 128 occurrences of the bus-free signal and the status of the bus-off recovery can be read out from this register. The CPU can force a bus-off by writing 255 to this register. Note that unlike the SJA1000 this core will signal bus-off immediately and not first when entering operating mode. The bus-off recovery sequence starts when entering operating mode after writing 255 to this register in reset mode.

19.5.12 Transmit buffer

The transmit buffer is write-only and mapped on address 16 to 28. Reading of this area is mapped to the receive buffer described in the next section. The layout of the transmit buffer depends on whether a standard frame (SFF) or an extended frame (EFF) is to be sent as seen below.

Table 152.

#	Write (SFF)	Write(EFF)
16	TX frame information	TX frame information
17	TX ID 1	TX ID 1
18	TX ID 2	TX ID 2
19	TX data 1	TX ID 3
20	TX data 2	TX ID 4
21	TX data 3	TX data 1
22	TX data 4	TX data 2
23	TX data 5	TX data 3
24	TX data 6	TX data 4
25	TX data 7	TX data 5
26	TX data 8	TX data 6
27	-	TX data 7
28	-	TX data 8

TX frame information (this field has the same layout for both SFF and EFF frames)

*Table 153.*TX frame information address 16

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FF	RTR	-	-	DLC.3	DLC.2	DLC.1	DLC.0

Bit 7 - FF selects the frame format, i.e. whether this is to be interpreted as an extended or standard frame. 1 = EFF, 0 = SFF.
Bit 6 - RTR should be set to 1 for an remote transmission request frame.
Bit 5:4 - are don't care.
Bit 3:0 - DLC specifies the Data Length Code and should be a value between 0 and 8. If a value greater than 8 is used 8 bytes will be transmitted.

TX identifier 1 (this field is the same for both SFF and EFF frames)

*Table 154.*TX identifier 1 address 17

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID.28	ID.27	ID.26	ID.25	ID.24	ID.23	ID.22	ID.21

Bit 7:0 - The top eight bits of the identifier.

TX identifier 2, SFF frame

*Table 155.*TX identifier 2 address 18

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID.20	ID.19	ID.18	-	-	-	-	-

Bit 7:5 - Bottom three bits of an SFF identifier.
Bit 4:0 - Don't care.

TX identifier 2, EFF frame

*Table 156.*TX identifier 2 address 18

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID.20	ID.19	ID.18	ID.17	ID.16	ID.15	ID.14	ID.13

Bit 7:0 - Bit 20 downto 13 of 29 bit EFF identifier.

TX identifier 3, EFF frame

*Table 157.*TX identifier 3 address 19

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID.12	ID.11	ID.10	ID.9	ID.8	ID.7	ID.6	ID.5

Bit 7:0 - Bit 12 downto 5 of 29 bit EFF identifier.

TX identifier 4, EFF frame

*Table 158.*TX identifier 4 address 20

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID.4	ID.3	ID.2	ID.1	ID.0	-	-	-

Bit 7:3 - Bit 4 downto 0 of 29 bit EFF identifier
Bit 2:0 - Don’t care

Data field

For SFF frames the data field is located at address 19 to 26 and for EFF frames at 21 to 28. The data is transmitted starting from the MSB at the lowest address.

19.5.13 Receive buffer

Table 159.

#	Read (SFF)	Read (EFF)
16	RX frame information	RX frame information
17	RX ID 1	RX ID 1
18	RX ID 2	RX ID 2
19	RX data 1	RX ID 3
20	RX data 2	RX ID 4
21	RX data 3	RX data 1
22	RX data 4	RX data 2
23	RX data 5	RX data 3
24	RX data 6	RX data 4
25	RX data 7	RX data 5
26	RX data 8	RX data 6
27	RX FI of next message in fifo	RX data 7
28	RX ID1 of next message in fifo	RX data 8

RX frame information (this field has the same layout for both SFF and EFF frames)

*Table 160.*RX frame information address 16

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FF	RTR	0	0	DLC.3	DLC.2	DLC.1	DLC.0

Bit 7 - Frame format of received message. 1 = EFF, 0 = SFF.
Bit 6 - 1 if RTR frame.
Bit 5:4 - Always 0.
Bit 3:0 - DLC specifies the Data Length Code.

RX identifier 1(this field is the same for both SFF and EFF frames)

*Table 161.*RX identifier 1 address 17

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID.28	ID.27	ID.26	ID.25	ID.24	ID.23	ID.22	ID.21

Bit 7:0 - The top eight bits of the identifier.

RX identifier 2, SFF frame

*Table 162.*RX identifier 2 address 18

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID.20	ID.19	ID.18	RTR	0	0	0	0

Bit 7:5 - Bottom three bits of an SFF identifier.
Bit 4 - 1 if RTR frame.
Bit 3:0 - Always 0.

RX identifier 2, EFF frame

*Table 163.*RX identifier 2 address 18

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID.20	ID.19	ID.18	ID.17	ID.16	ID.15	ID.14	ID.13

Bit 7:0 - Bit 20 downto 13 of 29 bit EFF identifier.

RX identifier 3, EFF frame

*Table 164.*RX identifier 3 address 19

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID.12	ID.11	ID.10	ID.9	ID.8	ID.7	ID.6	ID.5

Bit 7:0 - Bit 12 downto 5 of 29 bit EFF identifier.

RX identifier 4, EFF frame

*Table 165.*RX identifier 4 address 20

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID.4	ID.3	ID.2	ID.1	ID.0	RTR	0	0

Bit 7:3 - Bit 4 downto 0 of 29 bit EFF identifier
Bit 2- 1 if RTR frame
Bit 1:0 - Don’t care

Data field

For received SFF frames the data field is located at address 19 to 26 and for EFF frames at 21 to 28.

19.5.14 Acceptance filter

The acceptance filter can be used to filter out messages not meeting certain demands. If a message is filtered out it will not be put into the receive fifo and the CPU will not have to deal with it.

There are two different filtering modes, single and dual filter. Which one is used is controlled by bit 3 in the mode register. In single filter mode only one 4 byte filter is used. In dual filter two smaller filters are used and if either of these signals a match the message is accepted. Each filter consists of two parts the acceptance code and the acceptance mask. The code registers are used for specifying the pattern to match and the mask registers specify don’t care bits. In total eight registers are used for the acceptance filter as shown in the table below. Note that they are only read/writable in reset mode.

*Table 166.*Acceptance filter registers

Address	Description
16	Acceptance code 0 (ACR0)
17	Acceptance code 1 (ACR1)
18	Acceptance code 2 (ACR2)
19	Acceptance code 3 (ACR3)
20	Acceptance mask 0 (AMR0)
21	Acceptance mask 1 (AMR1)
22	Acceptance mask 2 (AMR2)
23	Acceptance mask 3 (AMR3)

Single filter mode, standard frame

When receiving a standard frame in single filter mode the registers ACR0-3 are compared against the incoming message in the following way:

ACR0.7-0 & ACR1.7-5 are compared to ID.28-18
ACR1.4 is compared to the RTR bit.
ACR1.3-0 are unused.
ACR2 & ACR3 are compared to data byte 1 & 2.

The corresponding bits in the AMR registers selects if the results of the comparison doesn't matter. A set bit in the mask register means don't care.

Single filter mode, extended frame

When receiving an extended frame in single filter mode the registers ACR0-3 are compared against the incoming message in the following way:

ACR0.7-0 & ACR1.7-0 are compared to ID.28-13
ACR2.7-0 & ACR3.7-3 are compared to ID.12-0
ACR3.2 are compared to the RTR bit
ACR3.1-0 are unused.

The corresponding bits in the AMR registers selects if the results of the comparison doesn't matter. A set bit in the mask register means don't care.

Dual filter mode, standard frame

When receiving a standard frame in dual filter mode the registers ACR0-3 are compared against the incoming message in the following way:

Filter 1

ACR0.7-0 & ACR1.7-5 are compared to ID.28-18
ACR1.4 is compared to the RTR bit.
ACR1.3-0 are compared against upper nibble of data byte 1
ACR3.3-0 are compared against lower nibble of data byte 1

Filter 2

ACR2.7-0 & ACR3.7-5 are compared to ID.28-18
ACR3.4 is compared to the RTR bit.

The corresponding bits in the AMR registers selects if the results of the comparison doesn't matter. A set bit in the mask register means don't care.

Dual filter mode, extended frame

When receiving a standard frame in dual filter mode the registers ACR0-3 are compared against the incoming message in the following way:

Filter 1

ACR0.7-0 & ACR1.7-0 are compared to ID.28-13

Filter 2

ACR2.7-0 & ACR3.7-0 are compared to ID.28-13

The corresponding bits in the AMR registers selects if the results of the comparison doesn't matter. A set bit in the mask register means don't care.

19.5.15 RX message counter

The RX message counter register at address 29 holds the number of messages currently stored in the receive fifo. The top three bits are always 0.

19.6 Common registers

There are three common registers with the same addresses and the same functionality in both Basi-CAN and PeliCAN mode. These are the clock divider register and bus timing register 0 and 1.

19.6.1 Clock divider register

The only real function of this register in the GRLIB version of the Opencores CAN is to choose between PeliCAN and BasiCAN. The clkout output of the Opencore CAN core is not connected and it is its frequency that can be controlled with this register.

*Table 167.*Bit interpretation of clock divider register (CDR) (address 31)

Bit	Name	Description
CDR.7	CAN mode	1 - PeliCAN, 0 - BasiCAN
CDR.6	-	unused (cbp bit of SJA1000)
CDR.5	-	unused (rxinten bit of SJA1000)
CDR.4	-	reserved
CDR.3	Clock off	Disable the clkout output
CDR.2-0	Clock divisor	Frequency selector

19.6.2 Bus timing 0

*Table 168.*Bit interpretation of bus timing 0 register (BTR0) (address 6)

Bit	Name	Description
BTR0.7-6	SJW	Synchronization jump width
BTR0.5-0	BRP	Baud rate prescaler

The CAN core system clock is calculated as:

$$t_{scl} = 2*t_{clk}*(BRP+1)$$

where t_{clk} is the system clock.

The sync jump width defines how many clock cycles (t_{scl}) a bit period may be adjusted with by one re-synchronization.

19.6.3 Bus timing 1

*Table 169.*Bit interpretation of bus timing 1 register (BTR1) (address 7)

Bit	Name	Description
BTR1.7	SAM	1 - The bus is sampled three times, 0 - single sample point
BTR1.6-4	TSEG2	Time segment 2
BTR1.3-0	TSEG1	Time segment 1

The CAN bus bit period is determined by the CAN system clock and time segment 1 and 2 as shown in the equations below:

$$t_{tseg1} = t_{scl} * (TSEG1+1)$$
$$t_{tseg2} = t_{scl} * (TSEG2+1)$$
$$t_{bit} = t_{tseg1} + t_{tseg2} + t_{scl}$$

The additional t_{scl} term comes from the initial sync segment. Sampling is done between TSEG1 and TSEG2 in the bit period.

19.7 Design considerations

This section lists known differences between this CAN controller and SJA1000 on which is it based:

- All bits related to sleep mode are unavailable
- Output control and test registers do not exist (reads 0x00)
- Clock divisor register bit 6 (CBP) and 5 (RXINTEN) are not implemented
- Overrun irq and status not set until fifo is read out

BasicCAN specific differences:

- The receive irq bit is not reset on read, works like in PeliCAN mode
- Bit CR.6 always reads 0 and is not a flip flop with no effect as in SJA1000

PeliCAN specific differences:

- Writing 256 to tx error counter gives immediate bus-off when still in reset mode
- Read Buffer Start Address register does not exist
- Addresses above 31 are not implemented (i.e. the internal RAM/FIFO access)
- The core transmits active error frames in Listen only mode

19.8 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x019. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

19.9 Implementation

19.9.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). See the description of the *syncrst* VHDL generic for further information.

19.10 Configuration options

Table 170 shows the configuration options of the core (VHDL generics).

*Table 170.*Configuration options

Generic	Function	Allowed range	Default
slvndx	AHB slave bus index	0 - NAHBSLV-1	0
ioaddr	The AHB I/O area base address. Compared with bit 19-8 of the 32-bit AHB address.	0 - 16#FFF#	16#FFF#
iomask	The I/O area address mask. Sets the size of the I/O area and the start address together with ioaddr.	0 - 16#FFF#	16#FF0#
irq	Interrupt number	0 - NAHBIRQ-1	0
memtech	Technology to implement on-chip RAM	0	0 - NTECH
syncrst	Reset implementation 0: Use asynchronous reset 1: Use synchronous reset, leave internal buffers without reset 2: Use synchronous reset, initialize internal buffers to zero at reset.	0 - 2	0
ft	Enable fault-tolerance	0 - 1	0

19.11 Signal descriptions

Table 171 shows the interface signals of the core (VHDL ports).

*Table 171.*Signal descriptions

Signal name	Field	Type	Function	Active
CLK		Input	AHB clock	
RESETN		Input	Reset	Low
AHBSI	*	Input	AMBA AHB slave inputs	-
AHBSO	*	Input	AMBA AHB slave outputs	
CAN_RXI		Input	CAN receiver input	High
CAN_TXO		Output	CAN transmitter output	High
MTESTI**	FIFO	Input	Memory BIST input signal to fifo RAM	-
	INFO	Input	Memory BIST input signal to info RAM	-
MTESTO**	FIFO	Output	Memory BIST output signal from fifo RAM	-
	INFO	Output	Memory BIST output signal from info RAM	-
MTESTCLK**	N/A	Input	Memory BIST clock	-

*1) see AMBA specification

** not available in FPGA releases

19.12 Signal definitions and reset values

The signals and their reset values are described in table 172.

*Table 172.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
cantx[]	Output	CAN transmit data	Low	Logical 1
canen[]	Output	CAN transmit enabel	-	Logical 0
canrx[]	Input	CAN receive data	Low	-

19.13 Timing

The timing waveforms and timing parameters are shown in figure 30 and are defined in table 173.

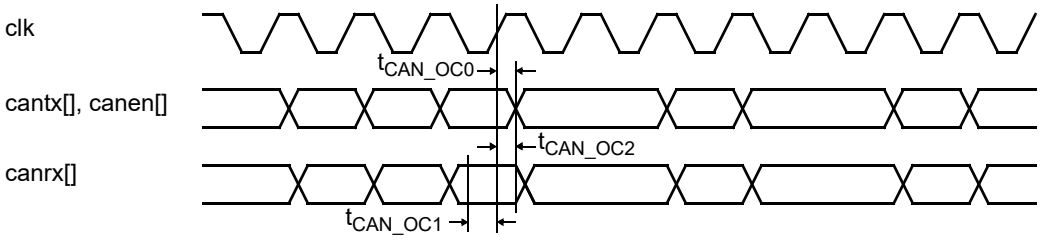


Figure 30. Timing waveforms

*Table 173.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{CAN_OC0}	clock to data output delay	rising *clk* edge	TBD	TBD	ns
t_{CAN_OC1}	data input to clock setup	rising *clk* edge	-	-	ns
t_{CAN_OC2}	data input from clock hold	rising *clk* edge	-	-	ns

Note: The *canrx[]* input is re-synchronized internally. The signal does not have to meet any setup or hold requirements.

19.14 Library dependencies

Table 174 shows libraries that should be used when instantiating the core.

*Table 174.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Types	AMBA signal type definitions
GAISLER	CAN	Component	Component declaration

19.15 Component declaration

```
library grlib;
use grlib.amba.all;
use gaisler.can.all;

component can_oc
   generic (
    slvndx    : integer := 0;
    ioaddr    : integer := 16#000#;
    iomask    : integer := 16#FF0#;
    irq       : integer := 0;
    memtech   : integer := 0);
   port (
      resetn  : in  std_logic;
      clk     : in  std_logic;
      ahbsi   : in  ahb_slv_in_type;
      ahbso   : out ahb_slv_out_type;
      can_rxi : in  std_logic;
      can_txo : out std_logic
);
   end component;
```

20 CLKGEN - Clock generation

20.1 Overview

The CLKGEN clock generator implements internal clock generation and buffering.

20.2 Technology specific clock generators

20.2.1 Overview

The core is a wrapper that instantiates technology specific primitives depending on the value of the *tech* VHDL generic. Each supported technology has its own subsection below. Table 175 lists the sub-section applicable for each technology setting. The table is arranged after the technology's numerical value in GRLIB. The subsections are ordered in alphabetical order after technology vendor.

*Table 175.*Overview of technology specific clock generator sections

Technology	Numerical value	Comment	Section
inferred	0	Default when no technology specific generator is available.	20.2.2
virtex	1		20.2.12
virtex2	2		20.2.13
memvirage	3	No technology specific clock generator available.	20.2.2
axcel	4		20.2.3
proasic	5		20.2.3
atc18s	6	No technology specific clock generator available.	20.2.2
altera	7		20.2.7
umc	8	No technology specific clock generator available.	20.2.2
rhumc	9		20.2.10
apa3	10		20.2.5
spartan3	11		20.2.11
ihp25	12	No technology specific clock generator available.	20.2.2
rhlib18t	13		20.2.9
virtex4	14		20.2.13
lattice	15	No technology specific clock generator available.	20.2.2
ut25	16	No technology specific clock generator available.	20.2.2
spartan3e	17		20.2.11
peregrine	18	No technology specific clock generator available.	20.2.2
memartisan	19	No technology specific clock generator available.	20.2.2
virtex5	20		20.2.14
custom1	21	No technology specific clock generator available.	20.2.2
ihp25rh	22	No technology specific clock generator available.	20.2.2
stratix1	23		20.2.7
stratix2	24		20.2.7
eclipse	25	No technology specific clock generator available.	20.2.2
stratix3	26		20.2.8
cyclone3	27		20.2.6
memvirage90	28	No technology specific clock generator available.	20.2.2
tsmc90	29	No technology specific clock generator available.	20.2.2
easic90	30		20.2.15
atc18rha	31	No technology specific clock generator available.	20.2.2

*Table 175.*Overview of technology specific clock generator sections

Technology	Numerical value	Comment	Section
smic013	32	No technology specific clock generator available.	20.2.2
tm65gpl	33	No technology specific clock generator available.	20.2.2
axdsp	34		20.2.3
spartan6	35		20.2.11
virtex6	36		20.2.14
actfus	37		20.2.17
stratix4	38		20.2.18
st65lp	39	No technology specific clock generator available.	20.2.2
st65gp	40	No technology specific clock generator available.	20.2.2
easic45	41		20.2.16

20.2.2 Generic technology

This implementation is used when the clock generator does not support instantiation of technology specific primitives or when the inferred technology has been selected.

This implementation connects the input clock, CLKIN or PCICLKIN depending on the *pcien* and *pcisysclk* VHDL generic, to the SDCLK, CLK1XU, and CLK outputs. The CLKN output is driven by the inverted input clock. The PCICLK output is directly driven by PCICLKIN. Both clock lock signals are always driven to '1' and the CLK2X output is always driven to '0'.

In simulation, CLK, CLKN and CLK1XU transitions are skewed 1 ns relative to the SDRAM clock output.

20.2.3 ProASIC

Generics used in this technology:	pcisysclk
Instantiated technology primitives:	None
Signals not driven in this technology:	clk4x, clk1xu, clk2xu, clkb, clkc

This technology selection does not instantiate any technology specific primitives. The core's clock output, CLK, is driven by the CLKIN or PCICLKIN input depending on the value of VHDL generics *pcien* and *pcisysclk*.

The PCICLK is always directly connected to PCICLKIN. Outputs SDCLK, CLKN and CLK2X, are driven to ground. Both clock lock signals, CGO.CLKLOCK and CGO.PCILOCK, are always driven high.

20.2.4 Actel Axcelerator

Generics used in this technology:	pcisysclk, clk_mul, clk_div, pcien, freq
Instantiated technology primitives:	PLL
Signals not driven in this technology:	clk4x, clk1xu, clk2xu, clkb, clkc

This technology selection has two modes. The first one is used if VHDL generics *clk_mul* and *clk_div* are equal and does not instantiate any technology specific primitives. The core's clock output, CLK, is driven by the CLKIN or PCICLKIN input depending on the value of VHDL generics *pcien* and *pcisysclk*.

The second mode is used if VHDL generics *clk_mul* and *clk_div* are different and instantiates a PLL. The core's clock output CLK is either driven by the pciclkin input or the main output from the PLL depending on the values of VHDL generics *pcien* and *pcisysclk*. When the PLL drives the CLK output

the resulting frequency is the frequency of CLKIN multiplied by the VHDL generic *clk_mul* and divided by the VHDL generic *clk_div*. Clock buffers are not instantiated within the clock generator and has to be done externally.

For both modes the following applies:

The PCICLK is always directly connected to PCICLKIN. Outputs SDCLK, CLKN and CLK2X, are driven to ground. Both clock lock signals, CGO.CLKLOCK and CGO.PCILOCK, are always driven high.

20.2.5 Actel ProASIC3

Generics used in this technology:	clk_mul, clk_div, clk_odiv, pcisysclk, pcien, freq, clkb_odiv, clkc_odiv
Instantiated technology primitives:	PLLINT, PLL
Signals not driven in this technology:	clkn, sdclk, clk2x, clk4x, clk1xu, clk2xu

This technology instantiates a PLL and a PLLINT to generate the main clock. The instantiation of a PLLINT macro allows the PLL reference clock to be driven from an I/O that is routed through the regular FPGA routing fabric. Figure 31 shows the instantiated primitives, the PLL EXTFB input is not shown and the EXTFB port on the instantiated component is always tied to ground. The figure shows which of the core's output ports that are driven by the PLL. The PCICLOCK will directly connected to PCICLKIN if VHDL generic *pcien* is non-zero, while CGO.PCILOCK is always driven high. The VHDL generics *pcien* and *pcisysclk* are used to select the reference clock. The values driven on the PLL inputs are listed in tables 176 and 177.

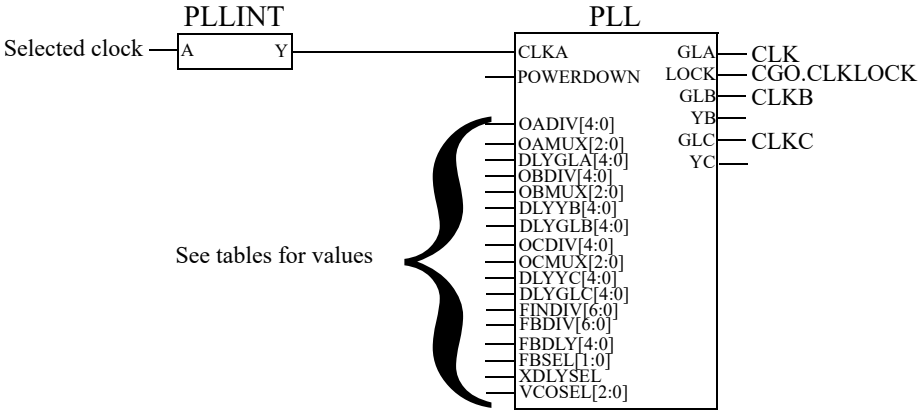


Figure 31. Actel ProASIC3 clock generation

*Table 176.*Constant input signals on Actel ProASIC3 PLL

Signal name	Value	Comment
OADIV[4:0]	VHDL generic *clk_odiv* - 1	Output divider
OAMUX[2:0]	0b100	Post-PLL MUXA
DLYGLA[4:0]	0	Delay on Global A
OBDIV[4:0]	VHDL generic *clkb_odiv* - 1 when *clkb_odiv* > 0, otherwise 0	Output divider
OBMUX[2:0]	0 when VHDL generic *clkb_odiv* = 0, otherwise 0b100	Post-PLL MUXB
DLYYB[4:0]	0	Delay on YB
DLYGLB[4:0]	0	Delay on Global B
OCDIV[4:0]	VHDL generic *clkc_odiv* - 1 when *clkc_odiv* > 0, otherwise 0	Output divider
OCMUX[2:0]	0 when VHDL generic *clkc_odiv* = 0, otherwise 0b100	Post-PLL MUXC
DLYYC[4:0]	0	Delay on YC
DLYGLC[4:0]	0	Delay on Global C
FINDIV[6:0]	VHDL generic *clk_div* - 1	Input divider
FBDIV[6:0]	VHDL generic *clk_mul* - 1	Feedback divider
FBDLY[4:0]	0	Feedback delay
FBSEL[1:0]	0b01	2-bit PLL feedback MUX
XDLYSEL	0	1-bit PLL feedback MUX
VCOSEL[2:0]	*See table 177 below*	VCO gear control. Selects one of four frequency ranges.

The PLL primitive has one parameter, VCOFREQUENCY, which is calculated with:

$$VCOFREQUENCY = \frac{freq \cdot clkmul}{clkdiv} / 1000$$

The calculations are performed with integer precision. This value is also used to determine the value driven on PLL input VCOSEL[2:0]. Table 177 lists the signal value depending on the value of VCOFREQUENCY.

*Table 177.*VCOSEL[2:0] on Actel ProASIC3 PLL

Value of VCOFREQUENCY	Value driven on VCOSEL[2:0]
< 44	0b000
< 88	0b010
< 175	0b100
>= 175	0b110

20.2.6 Altera Cyclone III

Generics used in this technology:	clk_mul, clk_div, sdramen, pcien, pcisysclk, freq, clk2xen
Instantiated technology primitives:	ALTPLL
Signals not driven in this technology:	clk4x, clk1xu, clk2xu, clkb, clkc

This technology instantiates an ALTPLL primitive to generate the required clocks, see figure 32. The ALTPLL attributes are listed in table 178. As can be seen in this table the attributes OPERATION_-MODE and COMPENSATE_CLOCK depend on the VHDL generic *sdramen*.

*Table 178.*Altera Cyclone III ALTPLL attributes

Attribute name*	**Value with *sdramen* = 1**	**Value with *sdramen* = 0**
INTENDED_DEVICE_FAMILY	“Cyclone III”	“Cyclone III”
OPERATION_MODE	“ZERO_DELAY_BUFFER”	“NORMAL”
COMPENSATE_CLOCK	“CLK1”	“clock0”
INCLK0_INPUT_FREQUENCY	1000000000 / (VHDL generic *freq*)	1000000000 / (VHDL generic *freq*)
WIDTH_CLOCK	5	5
CLK0_MULTIPLY_BY	VHDL generic *clk_mul*	VHDL generic *clk_mul*
CLK0_DIVIDE_BY	VHDL generic *clk_div*	VHDL generic *clk_div*
CLK1_MULTIPLY_BY	VHDL generic *clk_mul*	VHDL generic *clk_mul*
CLK1_DIVIDE_BY	VHDL generic *clk_div*	VHDL generic *clk_div*
CLK2_MULTIPLY_BY	VHDL generic *clk_mul * 2*	VHDL generic *clk_mul * 2*
CLK2_DIVIDE_BY	VHDL generic *clk_div*	VHDL generic *clk_div*

*Any attributes not listed are assumed to have their default value

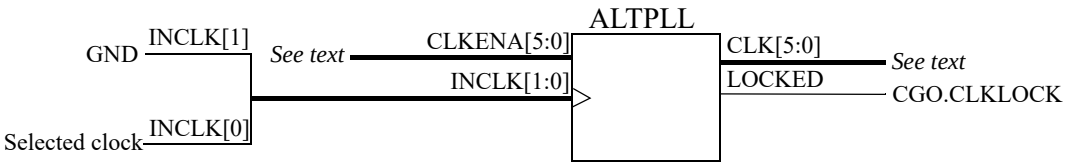


Figure 32. Altera Cyclone III ALTPLL

The value driven on the ALTPLL clock enable signal is dependent on the VHDL generics *clk2xen* and *sdramen*, table 179 lists the effect of these generics.

*Table 179.*Effect of VHDL generics *clk2xen* and *sdramen* on ALTPLL clock enable input

Value of sdramen	**Value of clk2xen**	**Value of CLKENA[5:0]**
0	0	0b000001
0	1	0b000101
1	0	0b000011
1	1	0b000111

Table 180 lists the connections of the core's input and outputs to the ALTPLL ports.

*Table 180.*Connections between core ports and ALTPLL ports

Core signal	Core direction	ALTPLL signal
CLKIN/PCICLKIN*	Input	INCLK[0]
CLK	Output	CLK[0]
CLKN	Output	$\overline{\text{CLK[0]}}$ (CLK[0] through an inverter)
CLK2X	Output	CLK[2]
SDCLK	Output	CLK[1]
CGO.CLKLOCK	Output	LOCKED

* Depending on VHDL generics PCIEN and PCISYSCLK, as described below.

The clocks can be generated using either the CLKIN input or the PCICLKIN input. This is selected with the VHDL generics *pcien* and *pcisysclk*. If *pcien* is 0 or *pcisysclk* is 0 the input clock to the ALTPLL will be CLKIN. If *pcien* is non-zero and *pcisysclk* is 1 the input to the ALTPLL will be PCICLKIN.

The PCICLK output will connected to the PCICLKIN input if VHDL generic *pcien* is non-zero. Otherwise the PCICLK output will be driven to ground. The CGO.PCILOCK signal is always driven high.

20.2.7 Altera Stratix 1/2

Generics used in this technology:	clk_mul, clk_div, sdramen, pcien, pcisysclk, freq, clk2xen
Instantiated technology primitives:	ALTPLL
Signals not driven in this technology:	clk4x, clk1xu, clk2xu, clkb, clkc

This technology instantiates an ALTPLL primitive to generate the required clocks, see figure 33. The ALTPLL attributes are listed in table 181. As can be seen in this table the OPERATION_MODE attribute depends on the VHDL generic *sdramen*.

*Table 181.*Altera Stratix 1/2 ALTPLL attributes

Attribute name*	Value with *sdramen* = 1	Value with *sdramen* = 0
OPERATION_MODE	"ZERO_DELAY_BUFFER"	"NORMAL"
INCLK0_INPUT_FREQUENCY	1000000000 / (VHDL generic *freq*)	1000000000 / (VHDL generic *freq*)
WIDTH_CLOCK	6	6
CLK0_MULTIPLY_BY	VHDL generic *clk_mul*	VHDL generic *clk_mul*
CLK0_DIVIDE_BY	VHDL generic *clk_div*	VHDL generic *clk_div*
CLK1_MULTIPLY_BY	VHDL generic *clk_mul* * 2	VHDL generic *clk_mul* * 2
CLK1_DIVIDE_BY	VHDL generic *clk_div*	VHDL generic *clk_div*
EXTCLK0_MULTIPLY_BY	VHDL generic *clk_mul*	VHDL generic *clk_mul*
EXTCLK0_DIVIDE_BY	VHDL generic *clk_div*	VHDL generic *clk_div*

*Any attributes not listed are assumed to have their default value

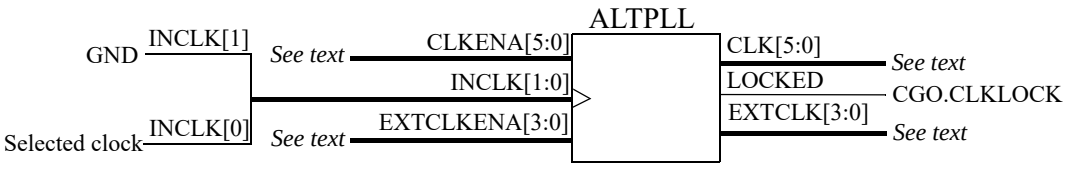


Figure 33. Altera Stratix 1/2 ALTPLL

The values driven on the ALTPLL clock enable signals are dependent on the VHDL generic *clk2xen*, table 182 lists the effect of *clk2xen*.

*Table 182.*Effect of VHDL generic *clk2xen* on ALTPLL clock enable inputs

Signal	**Value with *clk2xen* = 0**	**Value with *clk2xen* /= 0**
CLKENA[5:0]	0b000001	0b000011
EXTCLKENA[3:0]	0b0001	0b0011

Table 183 lists the connections of the core's input and outputs to the ALTPLL ports.

*Table 183.*Connections between core ports and ALTPLL ports

Core signal	**Core direction**	**ALTPLL signal**
CLKIN/PCICLKIN*	Input	INCLK[0]
CLK	Output	CLK[0]
CLKN	Output	$\overline{\text{CLK[0]}}$ (CLK[0] through an inverter)
CLK2X	Output	CLK[1]
SDCLK	Output	EXTCLK[0]
CGO.CLKLOCK	Output	LOCKED

* Depending on VHDL generics PCIEN and PCISYSCLK, as described below.

The clocks can be generated using either the CLKIN input or the PCICLKIN input. This is selected with the VHDL generics *pcien* and *pcisysclk*. If *pcien* is 0 or *pcisysclk* is 0 the input clock to the ALTPLL will be CLKIN. If *pcien* is non-zero and *pcisysclk* is 1 the input to the ALTPLL will be PCICLKIN.

The PCICLK output will connected to the PCICLKIN input if VHDL generic *pcien* is non-zero. Otherwise the PCICLK output will be driven to ground. The CGO.PCILOCK signal is always driven high.

20.2.8 Altera Stratix 3

This technology is not fully supported at this time.

20.2.9 RHLIB18t

Generics used in this technology:	clk_mul, clk_div
Instantiated technology primitives:	lfdll_top
Signals not driven in this technology:	-

Please contact Cobham Gaisler for information concerning the use of this clock generator.

20.2.10 RHUMC

Generics used in this technology:	None
Instantiated technology primitives:	pll_ip
Signals not driven in this technology:	-

Please contact Cobham Gaisler for information concerning the use of this clock generator.

20.2.11 Xilinx Spartan 3/3e/6

Generics used in this technology:	clk_mul, clk_div, sdramen, noclkfb, pcien, pcidll, pcisysclk, freq, clk2xen, clksel
Instantiated technology primitives:	BUFG, BUFMUX, DCM, BUFGDLL
Signals not driven in this technology:	clk4x, clkb, clkc

The main clock is generated with a DCM which is instantiated with the attributes listed in table 184. The input clock source connected to the CLKIN input is either the core's CLKIN input or the PCI-CLKIN input. This is selected with the VHDL generics *pcien* and *pcisysclk*. The main DCM's connections is shown in figure 34.

*Table 184.*Spartan 3/e DCM attributes

Attribute name*	**Value**
CLKDV_DIVIDE	2.0
CLKFX_DIVIDE	Determined by core's VHDL generic *clk_div*
CLKFX_MULTIPLY	Determined by core's VHDL generic *clk_mul*
CLKIN_DIVIDE_BY_2	false
CLKIN_PERIOD	10.0
CLKOUT_PHASE_SHIFT	"NONE"
CLK_FEEDBACK	"2X"
DESKEW_ADJUST	"SYSTEM_SYNCHRONOUS"
DFS_FREQUENCY_MODE	"LOW"
DLL_FREQUENCY_MODE	"LOW"
DSS_MODE	"NONE"
DUTY_CYCLE_CORRECTION	true
FACTORY_JF	X"C080"
PHASE_SHIFT	0
STARTUP_WAIT	false

*Any attributes not listed are assumed to have their default value

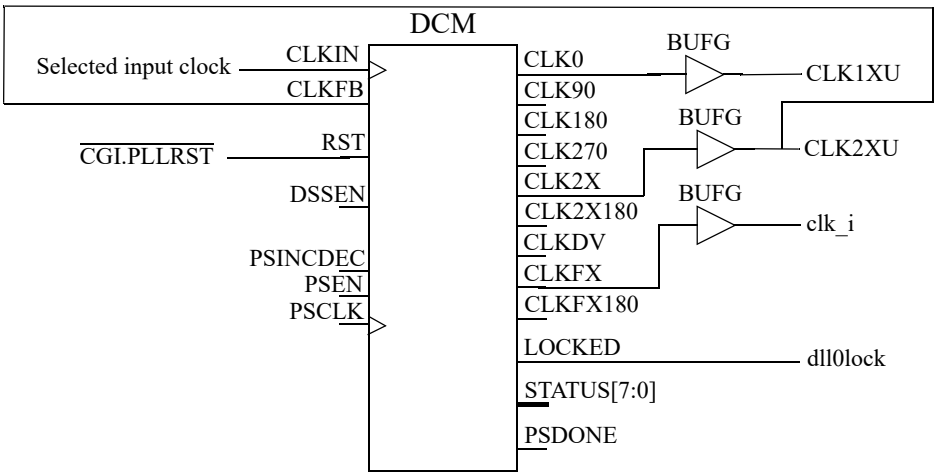


Figure 34. Spartan 3/e generation of main clock

If the VHDL generic *clk2xen* is non-zero the DCM shown in figure 35 is instantiated. The attributes of this DCM are the same as in table 184, except that the CLKFX_MULTIPLY and CLKFX_DIVIDE attributes are both set to 2 and the CLK_FEEDBACK attribute is set to "1X". The dll0lock signal is connected to the LOCKED output of the main clock DCM. When this signal is low all the bits in the

shift register connected to the CLK2X DCM's RST input are set to '1'. When the dll0lock signal is asserted it will take four main clock cycles until the RST input is deasserted. Depending on the value of the *clksel* VHDL generic the core's CLK2X output is either driven by a BUFG or a BUFGMUX. Figure 36 shows the two alternatives and how the CGI.CLKSEL(0) input is used to selected between the CLK0 and CLK2X output of the CLK2X DCM.

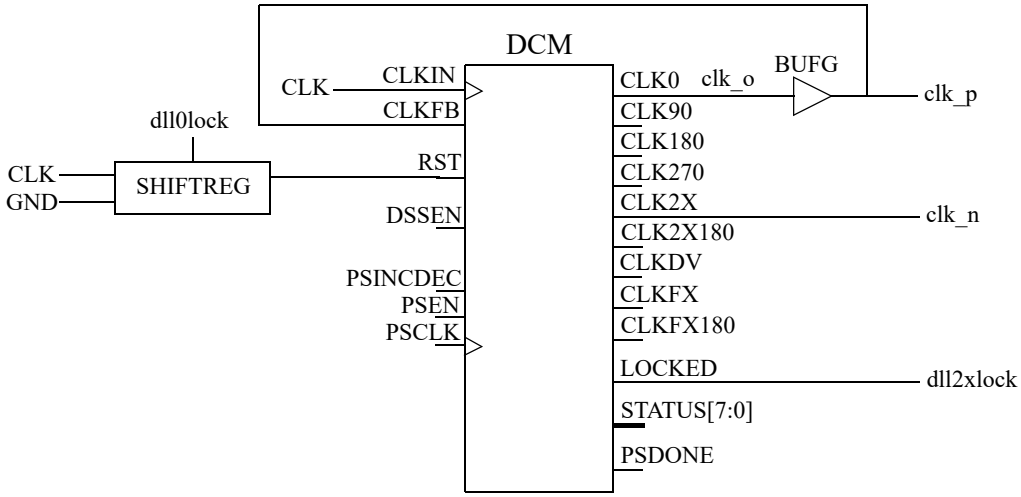


Figure 35. Spartan 3/e generation of CLK2X clock when VHDL generic *clk2xen* is non-zero

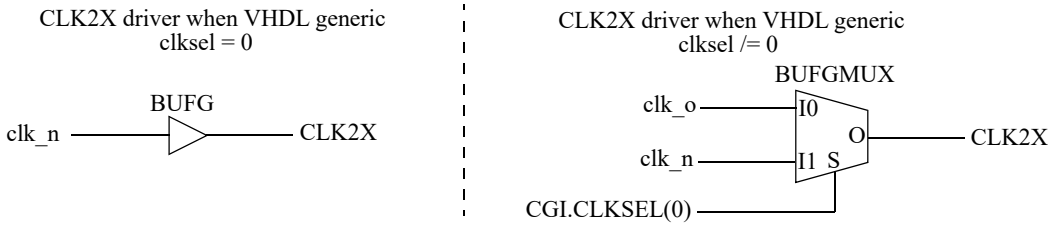


Figure 36. Spartan 3/e selection of CLK2X clock when VHDL generic *clk2xen* is non-zero

The value of the *clk2xen* VHDL generic also decides which output that drives the core's CLK output. If the VHDL generic is non-zero the CLK output is driven by the clk_p signal originating from the CLK2X DCM. Otherwise the CLK output is connected to the clk_i signal originating from the main clock DCM. The core's CLKN output is driven by the selected signal through an inverter. Figure 37 illustrates the connections.

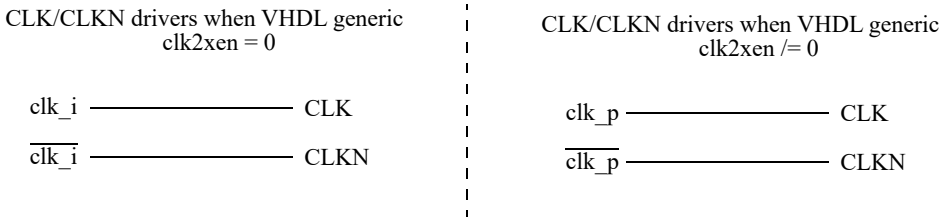


Figure 37. Spartan 3/e clock generator outputs CLK and CLKN

If the VHDL generic *clk2xen* is zero the dll0lock signal from the main clock DCM is either connected to the SDRAM DCM, described below, or if the SDRAM DCM is non-existent, to the core's CGO.CLKLOCK output. This setting also leads to the core's CLK2X output being driven by the main clock DCM's CLK2X output via a BUFG, please see figure 38.

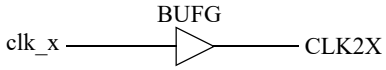


Figure 38. Spartan 3/e generation of CLK2X clock when VHDL generic *clk2xen* is zero

If the SDRAM clock is enabled, via the *sdramen* VHDL generic, and the clock generator is configured to use clock feedback the DCM shown in figure 39 is instantiated. This DCM has the same attributes as the CLK2X DCM. The input to the SDRAM DCM input clock is determined via the *clk2xen* VHDL generic. If the VHDL generic is set to 0 the input is the main CLK, if the generic is set to 1 the input is the clk_p out of the CLK2X DCM shown in figure 36. If the *clk2xen* VHDL generic is set to 2 the clock input to the SDRAM DCM depends on the *clksel* VHDL generic. The input in this last case is the CLK2X output shown in figure 38.

If the CLK2X DCM has been instantiated the SDRAM DCM RST input depends on the LOCKED output of the CLK2X DCM. If the CLK2X DCM has not been instantiated the SDRAM DCM RST input depends on the LOCKED output from the main clock DCM. The applicable LOCKED signal is utilized to keep the SDRAM DCM in reset until its input clock has been stabilized. This is done with a shift register with the same method used for the CLK2X DCM RST.

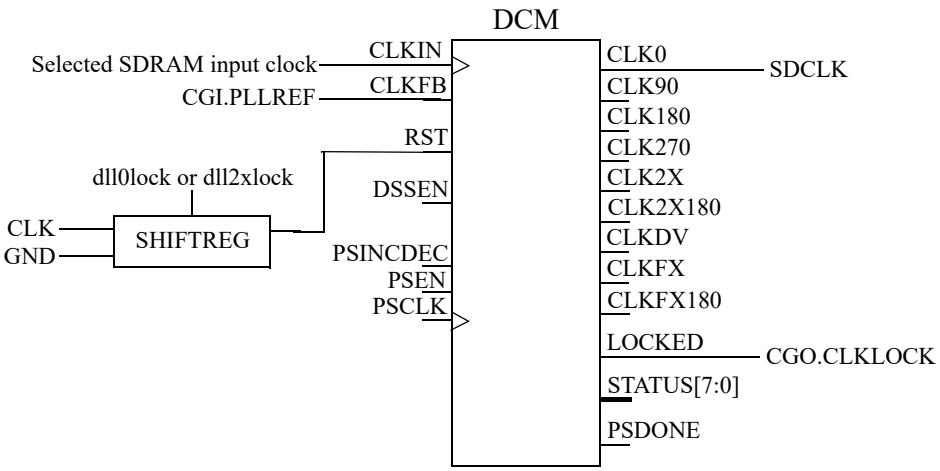


Figure 39. Spartan 3/e generation of SDRAM clock

If the SDRAM clock is disabled (*sdramen* VHDL generic set to 0) or the core has been configured not to use clock feedback (*noclockfb* VHDL generic set to 1) the driver of the core's SDCLK output is determined by the value of the *clk2xen* VHDL generic. If the *clk2xen* VHDL generic is set to 2, the SDRAM clock output is the same as the CLK2X output shown in figure 36, in other words it also depends on the *clksel* VHDL generic. If the *clk2xen* VHDL generic has any other value the SDCLK output is the same as the core's CLK output.

When the *sdramen* VHDL generic is set to 0 the core's CGO.CLKLOCK output is connected to the CLK2X DCM's LOCKED output, if the DCM exists, otherwise the CGO.CLKLOCK output is connected to the main clock DCM's LOCKED output.

If PCI clock generation is enabled via the *pcien* VHDL generic the core instantiates either a BUFG or a BUFGDLL as depicted in figure 40 below. Note that the PCI clock must be enabled if the main clock is to be driven by the PCICLKIN input. If the PCI clock is disabled the PCICLK output is driven to zero. The CGO.PCILOCK output is always driven high in all configurations.

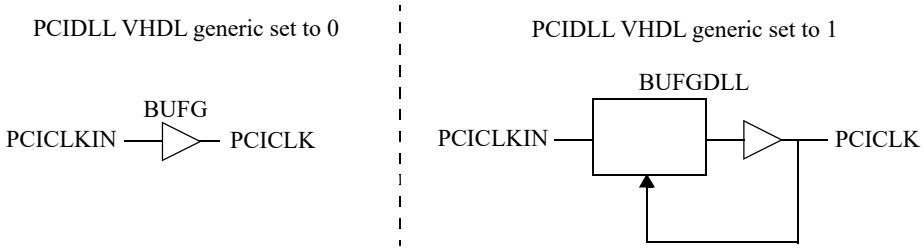


Figure 40. Spartan 3/e PCI clock generation

20.2.12 Xilinx Virtex

Generics used in this technology:	clk_mul, clk_div, sdramen, noclkfb, pcien, pcidll, pcisysclk
Instantiated technology primitives:	BUFG, BUFGDLL, CLKDLL
Signals not driven in this technology:	clk4x, clk1xu, clk2xu, clkb, clkc

The main clock is generated with the help of a CLKDLL. Figure 41 below shows how the CLKDLL primitive is connected. The input clock source is either the core's CLKIN input or the PCICLKIN input. This is selected with the VHDL generics *pcien* and *pcisysclk*. The figure shows three potential drivers of the BUFG driving the output clock CLK, the driver is selected via the VHDL generics *clk_mul* and *clk_div*. If *clk_mul/clk_div* is equal to 2 the CLK2X output is selected, if *clk_div/clk_mul* equals 2 the CLKDV output is selected, otherwise the CLK0 output drives the BUFG. The inverted main clock output, CLKN, is the BUFG output connected via an inverter.

The figure shows a dashed line connecting the CLKDLL's LOCKED output to the core output CGO.CLKLOCK. The driver of the CGO.CLKLOCK output depends on the instantiation of a CLKDLL for the SDRAM clock. See description of the SDRAM clock below.

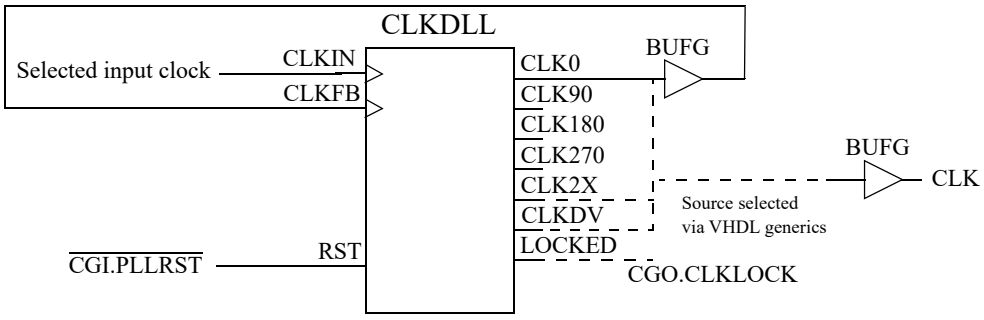


Figure 41. Virtex generation of main clock

If the SDRAM clock is enabled, via the *sdramen* VHDL generic, and the clock generator is configured to use clock feedback, VHDL generic *noclkfb* set to 0, a CLKDLL is instantiated as depicted in figure 42. Note how the CLKDLL's RST input is connected via a shift register clocked by the main clock. The shift register is loaded with all '1' when the LOCKED signal of the main clock CLKDLL is low. When the LOCKED signal from the main clock CLKDLL is asserted the SDRAM CLKDLL's RST input will be deasserted after four main clock cycles.

For all other configurations the SDRAM clock is driven by the main clock and the CGO.CLKLOCK signal is driven by the main clock CLKDLL's LOCKED output. The SDRAM CLKDLL must be present if the core's CLK2X output shall be driven.

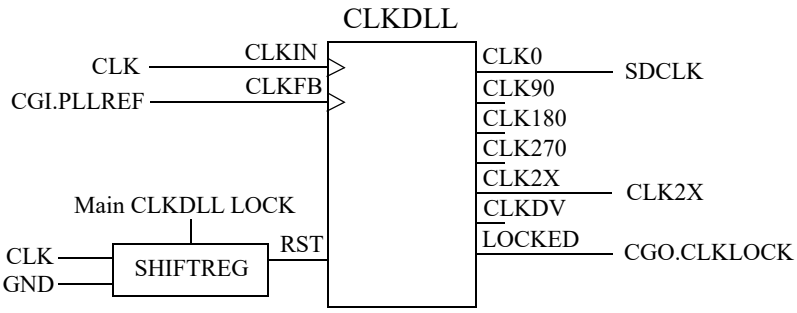


Figure 42. Virtex generation of SDRAM clock with feedback clock enabled

If PCI clock generation is enabled via the *pcien* VHDL generic the core instantiates either a BUFG or a BUFGDLL as depicted in figure 43 below. Note that the PCI clock must be enabled if the main clock is to be driven by the PCICLKIN input. If the PCI clock is disabled the PCICLK output is driven to zero. The CGO.PCILOCK output is always driven high in all configurations.

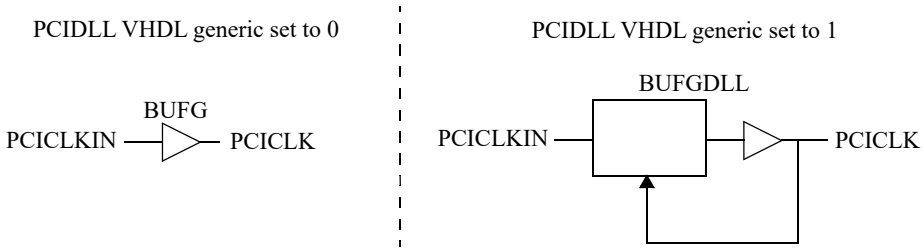


Figure 43. Virtex PCI clock generation

20.2.13 Xilinx Virtex 2/4

Generics used in this technology:	clk_mul, clk_div, sdramen, noclkfb, pcien, pcidll, pcisysclk, freq, clk2xen, clksel
Instantiated technology primitives:	BUFG, BUFMUX, DCM, BUFGDLL
Signals not driven in this technology:	clk4x, clkb, clkc

The main clock is generated with a DCM which is instantiated with the attributes listed in table 185. The input clock source connected to the CLKIN input is either the core's CLKIN input or the PCI-CLKIN input. This is selected with the VHDL generics *pcien* and *pcisysclk*. The main DCM's connections is shown in figure 44.

*Table 185.*Virtex 2/4 DCM attributes

Attribute name*	Value
CLKDV_DIVIDE	2.0
CLKFX_DIVIDE	Determined by core's VHDL generic *clk_div*
CLKFX_MULTIPLY	Determined by core's VHDL generic *clk_mul*
CLKIN_DIVIDE_BY_2	false
CLKIN_PERIOD	10.0
CLKOUT_PHASE_SHIFT	"NONE"
CLK_FEEDBACK	"1X"
DESKEW_ADJUST	"SYSTEM_SYNCHRONOUS"
DFS_FREQUENCY_MODE	"LOW"
DLL_FREQUENCY_MODE	"LOW"
DSS_MODE	"NONE"
DUTY_CYCLE_CORRECTION	true
FACTORY_JF	X"C080"
PHASE_SHIFT	0
STARTUP_WAIT	false

*Any attributes not listed are assumed to have their default value

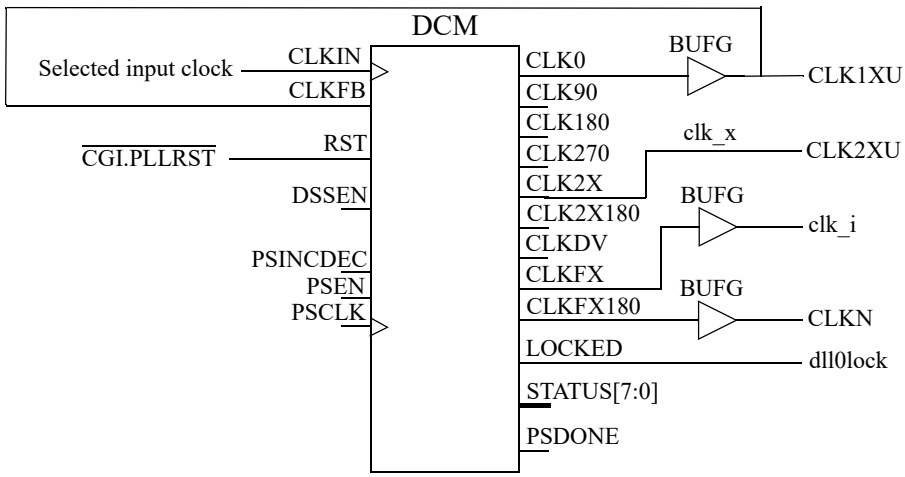


Figure 44. Virtex 2/4 generation of main clock

If the VHDL generic *clk2xen* is non-zero the DCM shown in figure 45 is instantiated. The attributes of this DCM are the same as in table 185, except that the CLKFX_MULTIPLY and CLKFX_DIVIDE attributes are both set to 2. The dll0lock signal is connected to the LOCKED output of the main clock DCM. When this signal is low all the bits in the shift register connected to the CLK2X DCM's RST input are set to '1'. When the dll0lock signal is asserted it will take four main clock cycles until the RST input is deasserted. Depending on the value of the *clksel* VHDL generic the core's CLK2X output is either driven by a BUFG or a BUFGMUX. Figure 46 shows the two alternatives and how the CGI.CLKSEL(0) input is used to selected between the CLK0 and CLK2X output of the CLK2X DCM.

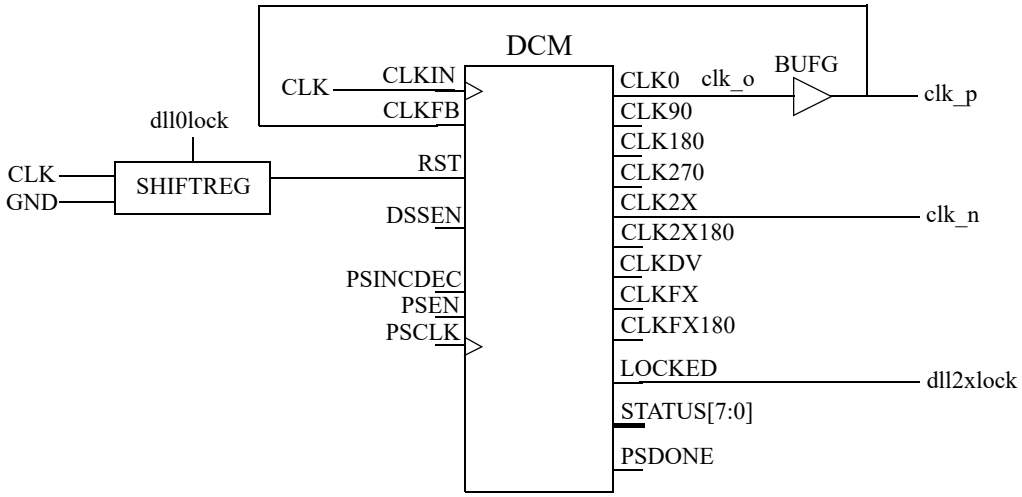


Figure 45. Virtex 2/4 generation of CLK2X clock when VHDL generic *clk2xen* is non-zero

The value of the *clk2xen* VHDL generic also decides which output that drives the core's CLK output. If the VHDL generic is non-zero the CLK output is driven by the clk_p signal originating from the CLK2X DCM. Otherwise the CLK output is connected to the clk_i signal originating from the main clock DCM. Note that the CLKN output always originates from the main clock DCM, as shown in figure 44.

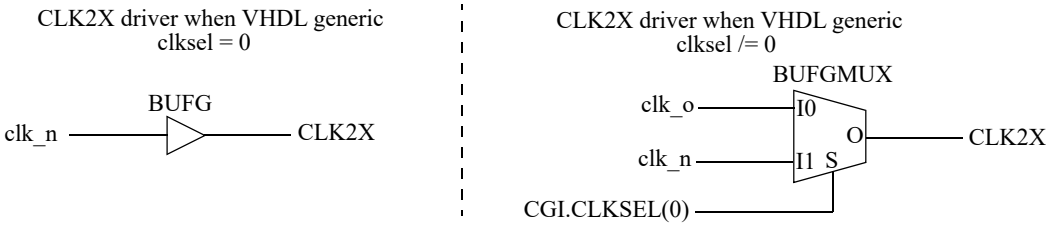


Figure 46. Virtex 2/4 selection of CLK2X clock when VHDL generic *clk2xen* is non-zero

If the VHDL generic *clk2xen* is zero the dll0lock signal from the main clock DCM is either connected to the SDRAM DCM, described below, or if the SDRAM DCM is non-existent, to the core's CGO.CLKLOCK output. This setting also leads to the core's CLK2X output being driven by the main clock DCM's CLK2X output via a BUFG, please see figure 47.

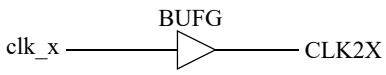


Figure 47. Virtex 2/4 generation of CLK2X clock when VHDL generic *clk2xen* is zero

If the SDRAM clock is enabled, via the *sdramen* VHDL generic, and the clock generator is configured to use clock feedback the DCM shown in figure 48. The input to the SDRAM DCM input clock is determined via the *clk2xen* VHDL generic. If the VHDL generic is set to 0 the input is the main CLK, if the generic is set to 1 the input is the clk_p out of the CLK2X DCM shown in figure 45. If the *clk2xen* VHDL generic is set to 2 the clock input to the SDRAM DCM depends on the *clksel* VHDL generic. The input in this last case is the CLK2X output shown in figure 46.

If the CLK2X DCM has been instantiated the SDRAM DCM RST input depends on the LOCKED output of the CLK2X DCM. If the CLK2X DCM has not been instantiated the SDRAM DCM RST input depends on the LOCKED output from the main clock DCM. The applicable LOCKED signal is

utilized to keep the SDRAM DCM in reset until its input clock has been stabilized. This is done with a shift register with the same method used for the CLK2X DCM RST.

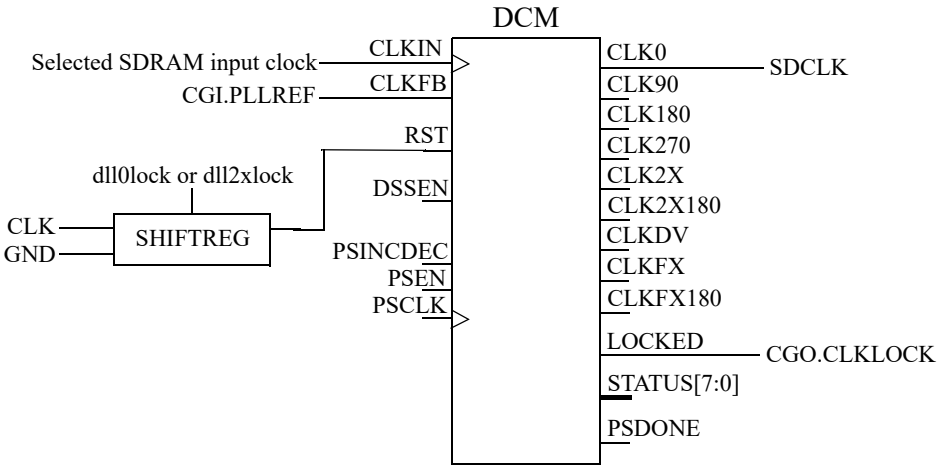


Figure 48. Virtex 2/4 generation of SDRAM clock

If the SDRAM clock is disabled (*sdramen* VHDL generic set to 0) or the core has been configured not to use clock feedback (*noclockfb* VHDL generic set to 1) the driver of the core's SDCLK output is determined by the value of the *clk2xen* VHDL generic. If the clk2xen VHDL generic is set to 2, the SDRAM clock output is the same as the CLK2X output shown in figure 46, in other words it also depends on the *clksel* VHDL generic. If the *clk2xen* VHDL generic has any other value the SDCLK output is the same as the core's CLK output.

When the *sdramen* VHDL generic is set to 0 the core's CGO.CLKLOCK output is connected to the CLK2X DCM's LOCKED output, if the DCM exists, otherwise the CGO.CLKLOCK output is connected to the main clock DCM's LOCKED output.

If PCI clock generation is enabled via the *pcien* VHDL generic the core instantiates either a BUFG or a BUFGDLL as depicted in figure 49 below. Note that the PCI clock must be enabled if the main clock is to be driven by the PCICLKIN input. If the PCI clock is disabled the PCICLK output is driven to zero. The CGO.PCILOCK output is always driven high in all configurations.

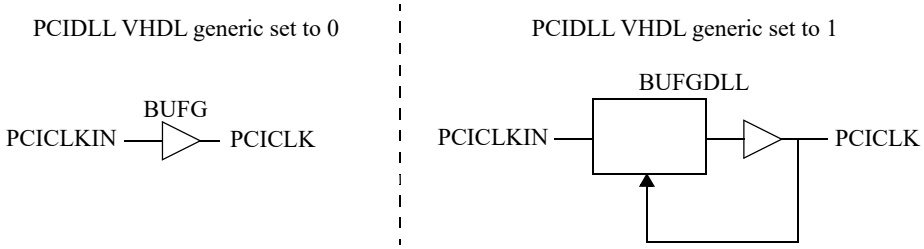


Figure 49. Virtex 2/4 PCI clock generation

20.2.14 Xilinx Virtex 5/6

Generics used in this technology:	clk_mul, clk_div, sdramen, noclkfb, pcien, pcidll, pcisysclk, freq, clk2xen, clksel
Instantiated technology primitives:	BUFG, BUFMUX, DCM, BUFGDLL
Signals not driven in this technology:	clk4x, clkb, clkc

The main clock is generated with a DCM which is instantiated with the attributes listed in table 186. The input clock source connected to the CLKIN input is either the core's CLKIN input or the PCI-

CLKIN input. This is selected with the VHDL generics *pcien* and *pcisysclk*. The main DCM's connections is shown in figure 50.

*Table 186.*Virtex 5 DCM attributes

Attribute name*	**Value**
CLKDV_DIVIDE	2.0
CLKFX_DIVIDE	Determined by core's VHDL generic *clk_div*
CLKFX_MULTIPLY	Determined by core's VHDL generic *clk_mul*
CLKIN_DIVIDE_BY_2	false
CLKIN_PERIOD	10.0
CLKOUT_PHASE_SHIFT	"NONE"
CLK_FEEDBACK	"1X"
DESKEW_ADJUST	"SYSTEM_SYNCHRONOUS"
DFS_FREQUENCY_MODE	"LOW"
DLL_FREQUENCY_MODE	"LOW"
DSS_MODE	"NONE"
DUTY_CYCLE_CORRECTION	true
FACTORY_JF	X"C080"
PHASE_SHIFT	0
STARTUP_WAIT	false

*Any attributes not listed are assumed to have their default value

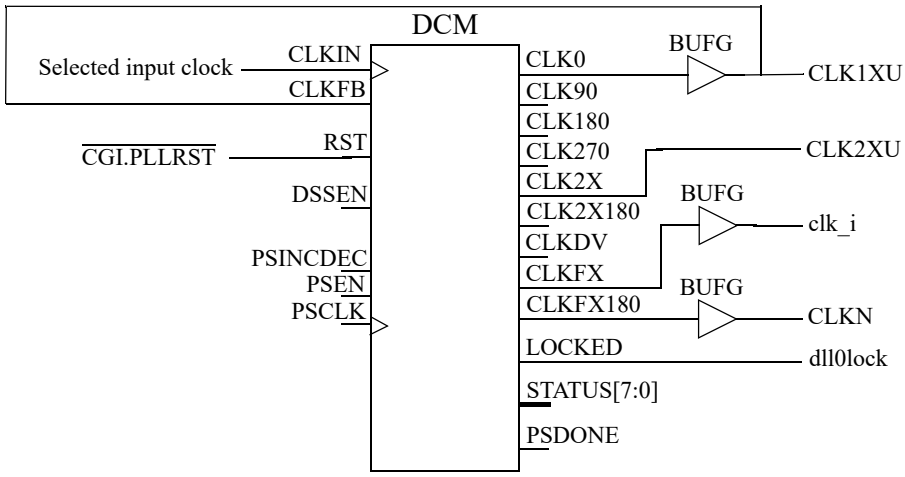


Figure 50. Virtex 5 generation of main clock

If the VHDL generic *clk2xen* is non-zero the DCM shown in figure 51 is instantiated. The attributes of this DCM are the same as in table 186, except that the CLKFX_MULTIPLY and CLKFX_DIVIDE attributes are both set to 2. The dll0lock signal is connected to the LOCKED output of the main clock DCM. When this signal is low all the bits in the shift register connected to the CLK2X DCM's RST input are set to '1'. When the dll0lock signal is asserted it will take four main clock cycles until the RST input is deasserted. Depending on the value of the *clksel* VHDL generic the core's CLK2X output is either driven by a BUFG or a BUFGMUX. Figure 52 shows the two alternatives and how the CGI.CLKSEL(0) input is used to selected between the CLK0 and CLK2X output of the CLK2X DCM.

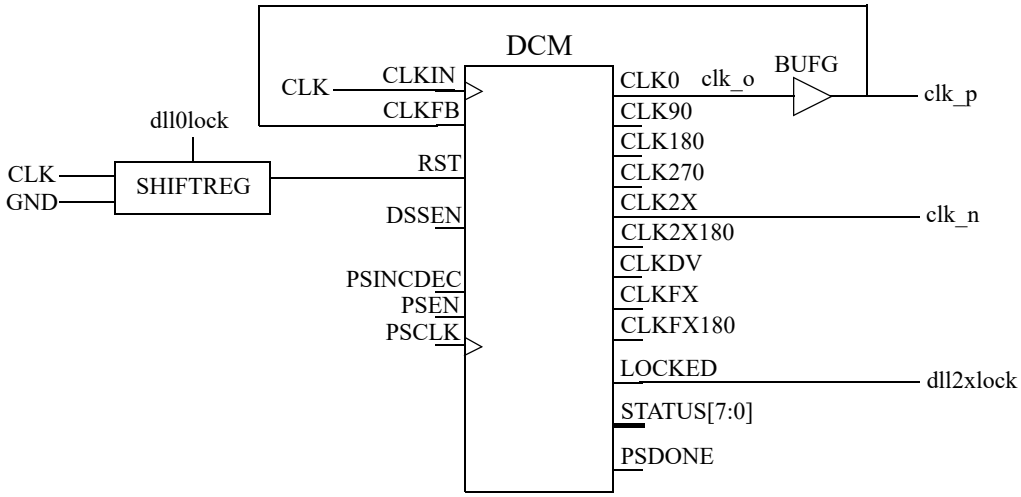


Figure 51. Virtex 5 generation of CLK2X clock when VHDL generic *clk2xen* is non-zero

The value of the *clk2xen* VHDL generic also decides which output that drives the core's CLK output. If the VHDL generic is non-zero the CLK output is driven by the clk_p signal originating from the CLK2X DCM. Otherwise the CLK output is connected to the clk_i signal originating from the main clock DCM. Note that the CLKN output always originates from the main clock DCM, as shown in figure 50.

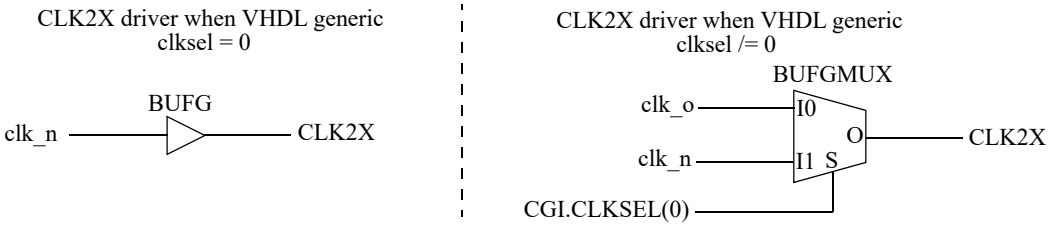


Figure 52. Virtex 5 selection of CLK2X clock when VHDL generic *clk2xen* is non-zero

If the VHDL generic *clk2xen* is zero the dll0lock signal from the main clock DCM is either connected to the SDRAM DCM, described below, or if the SDRAM DCM is non-existent, to the core's CGO.CLKLOCK output. This setting also leads to the core's CLK2X output being driven directly by the main clock DCM's CLK2X output.

If the SDRAM clock is enabled, via the *sdramen* VHDL generic, and the clock generator is configured to use clock feedback the DCM shown in figure 53. This DCM has the same attributes as the main clock DCM described in table 186, with the exceptions that CLKFX_MULTIPLY and CLKFX_DIVIDE are both set to 2 and DESKEW_ADJUST is set to "SOURCE_SYNCHRONOUS".

The input to the SDRAM DCM input clock is determined via the *clk2xen* VHDL generic. If the VHDL generic is set to 0 the input is the main CLK, if the generic is set to 1 the input is the clk_p out of the CLK2X DCM shown in figure 45. If the *clk2xen* VHDL generic is set to 2 the clock input to the SDRAM DCM depends on the *clksel* VHDL generic. The input in this last case is the CLK2X output shown in figure 52.

If the CLK2X DCM has been instantiated the SDRAM DCM RST input depends on the LOCKED output of the CLK2X DCM. If the CLK2X DCM has not been instantiated the SDRAM DCM RST input depends on the LOCKED output from the main clock DCM. The applicable LOCKED signal is utilized to keep the SDRAM DCM in reset until its input clock has been stabilized. This is done with a shift register with the same method used for the CLK2X DCM RST.

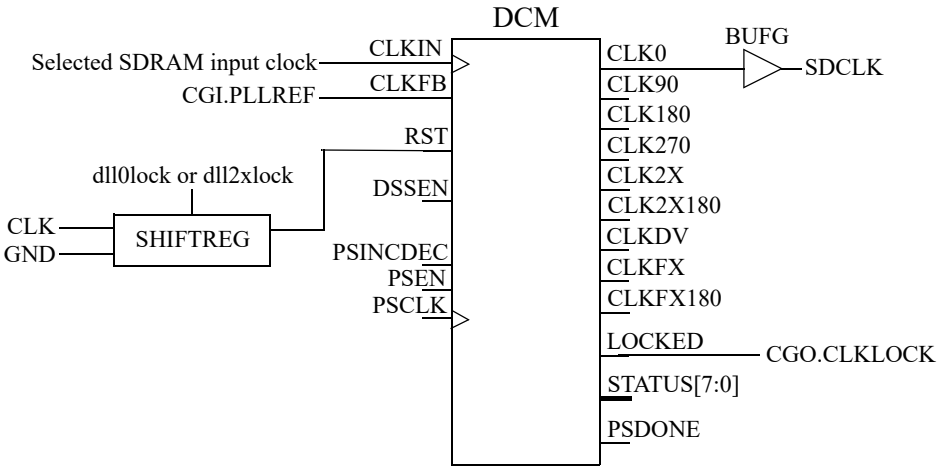


Figure 53. Virtex 5 generation of SDRAM clock

If the SDRAM clock is disabled (*sdramen* VHDL generic set to 0) or the core has been configured not to use clock feedback (*noclockfb* VHDL generic set to 1) the driver of the core's SDCLK output is determined by the value of the *clk2xen* VHDL generic. If the clk2xen VHDL generic is set to 2, the SDRAM clock output is the same as the CLK2X output shown in figure 52, in other words it also depends on the *clksel* VHDL generic. If the *clk2xen* VHDL generic has any other value the SDCLK output is the same as the core's CLK output.

When the *sdramen* VHDL generic is set to 0 the core's CGO.CLKLOCK output is connected to the CLK2X DCM's LOCKED output, if the DCM exists, otherwise the CGO.CLKLOCK output is connected to the main clock DCM's LOCKED output.

If PCI clock generation is enabled via the *pcien* VHDL generic the core instantiates either a BUFG or a BUFGDLL as depicted in figure 54 below. Note that the PCI clock must be enabled if the main clock is to be driven by the PCICLKIN input. If the PCI clock is disabled the PCICLK output is driven to zero. The CGO.PCILOCK output is always driven high in all configurations.

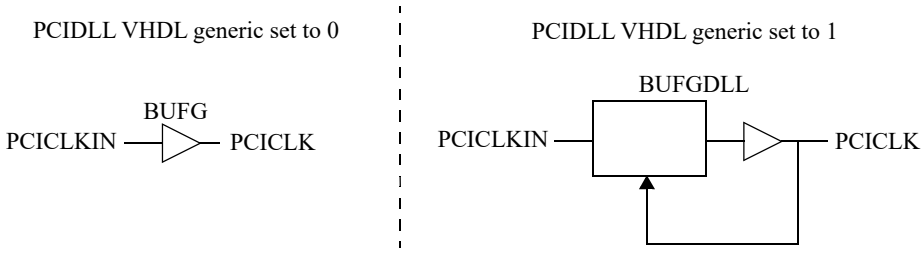


Figure 54. Virtex 5 PCI clock generation

20.2.15 eASIC90 (Nextreme)

Generics used in this technology:	clk_mul, clk_div, freq, pcisysclk, pcien
Instantiated technology primitives:	eclkgen
Signals not driven in this technology:	sdclk, pciclk, clk1xu, clk2xu, clkb, clkc

Please contact Cobham Gaisler for information concerning the use of this clock generator.

20.2.16 eASIC45 (Nextreme2)

Generics used in this technology:	clk_mul, clk_div, freq, pcisysclk, pcien, sdramen, clk2xen
Instantiated technology primitives:	eclkgen
Signals not driven in this technology:	clk1xu, clk2xu, clkb, clkc

An example instantiating eASIC's clock generator wrapper that generates clk, clkn and clk2x is provided. Note that the example does not instantiate buffers on the clock outputs. Please contact Cobham Gaisler for information concerning the use of this clock generator.

20.2.17 Actel Fusion

Generics used in this technology:	clk_mul, clk_div, clk_odiv, pcisysclk, pcien, freq, clkb_odiv, clkc_odiv
Instantiated technology primitives:	PLLINT, PLL
Signals not driven in this technology:	clkn, sdclk, clk2x, clk4x, clk1xu, clk2xu

This technology instantiates a PLL and a PLLINT to generate the main clock. The instantiation of a PLLINT macro allows the PLL reference clock to be driven from an I/O that is routed through the regular FPGA routing fabric. Figure 55 shows the instantiated primitives, the PLL EXTFB input is not shown and the EXTFB port on the instantiated component is always tied to ground. The OADIVRST port on the PLL is driven by CGI.PLLRST. The figure shows which of the core's output ports that are driven by the PLL. The PCICLOCK will directly connected to PCICLKIN if VHDL generic *pcien* is non-zero, while CGO.PCILOCK is always driven high. The VHDL generics *pcien* and *pcisysclk* are used to select the reference clock. The values driven on the PLL inputs are listed in tables 187 and 188.

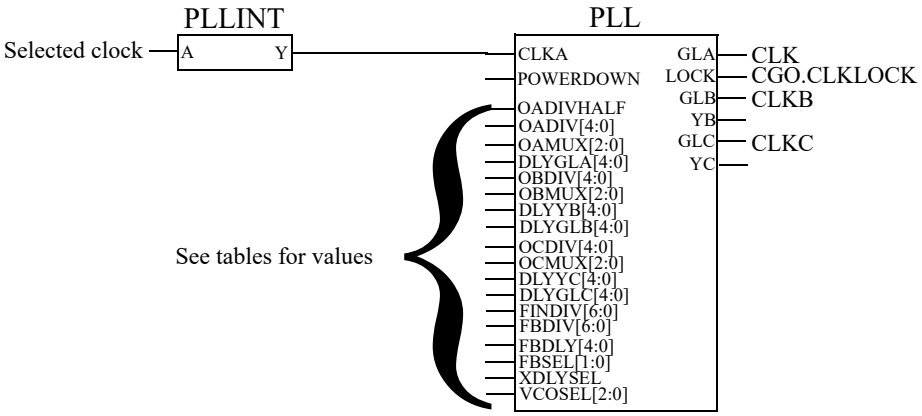


Figure 55. Actel Fusion clock generation

*Table 187.*Constant input signals on Actel Fusion PLL

Signal name	Value	Comment
OADIVHALF	0	Division by half
OADIV[4:0]	VHDL generic *clk_odiv* - 1	Output divider
OAMUX[2:0]	0b100	Post-PLL MUXA
DLYGLA[4:0]	0	Delay on Global A
OBDIV[4:0]	VHDL generic *clkb_odiv* - 1 when *clkb_odiv* > 0, otherwise 0	Output divider
OBMUX[2:0]	0 when VHDL generic *clkb_odiv* = 0, otherwise 0b100	Post-PLL MUXB

*Table 187.*Constant input signals on Actel Fusion PLL

Signal name	Value	Comment
DLYYB[4:0]	0	Delay on YB
DLYGLB[4:0]	0	Delay on Global B
OCDIV[4:0]	VHDL generic *clkc_odiv* - 1 when *clkc_odiv* > 0, otherwise 0	Output divider
OCMUX[2:0]	0 when VHDL generic *clkc_odiv* = 0, otherwise 0b100	Post-PLL MUXC
DLYYC[4:0]	0	Delay on YC
DLYGLC[4:0]	0	Delay on Global C
FINDIV[6:0]	VHDL generic *clk_div* - 1	Input divider
FBDIV[6:0]	VHDL generic *clk_mul* - 1	Feedback divider
FBDLY[4:0]	0	Feedback delay
FBSEL[1:0]	0b01	2-bit PLL feedback MUX
XDLYSEL	0	1-bit PLL feedback MUX
VCOSEL[2:0]	*See table 177 below*	VCO gear control. Selects one of four frequency ranges.

The PLL primitive has one parameter, VCOFREQUENCY, which is calculated with:

$$VCOFREQUENCY = \frac{freq \cdot clkmul}{clkdiv} / 1000$$

The calculations are performed with integer precision. This value is also used to determine the value driven on PLL input VCOSEL[2:0]. Table 177 lists the signal value depending on the value of VCOFREQUENCY.

*Table 188.*VCOSEL[2:0] on Actel Fusion PLL

Value of VCOFREQUENCY	Value driven on VCOSEL[2:0]
< 44	0b000
< 88	0b010
< 175	0b100
>= 175	0b110

20.2.18 Altera Stratix 4

This technology is not fully supported at this time.

20.3 Configuration options

Table 189 shows the configuration options of the core (VHDL generics).

*Table 189.*Configuration options

Generic name	Function	Allowed range	Default
tech	Target technology	0 - NTECH	inferred
clk_mul	Clock multiplier, used in clock scaling. Not all techbolo-gies support clock scaling.		1
clk_div	Clock divisor, used in clock scaling. Not all technologies support clock scaling.		1
sdramen	When this generic is set to 1 the core will generate a clock on the SDCLK. Not supported by all technologies. See technology specific description.		0
noclkfb	When this generic is set to 0 the core will use the CGI.PLLREF input as feedback clock for some technol-ogies. See technology specific description.		1
pcien	When this generic is set to 1 the PCI clock is activated. Otherwise the PCICLKIN input is typically unused. See technology specific descriptions.		0
pcidll	When this generic is set to 1, a DLL will be instantiated for the PCI input clock for some technologies. See the technology specific descriptions.		0
pcisysclk	When this generic is set to 1 the clock generator will use the pciclkin input as the main clock reference. This also requires generic pcien to be set to 1.		0
freq	Clock frequency in kHz		25000
clk2xen	Enables 2x clock output. Not available in all technolgies and may have additional options. See technology spe-cific description.		0
clksel	Enable clock select. Not available in all technologies.		0
clk_odiv	ProASIC3/Fusion output divider for GLA. Only used in ProASIC3/Fusion technology.	1 - 32	1
clkb_odiv	ProASIC3/Fusion output divider for GLB. Only used in ProASIC3/Fusion technology. Set this value to 0 to dis-able generation of GLB.	0 - 32	0
clkc_odiv	ProASIC3/Fusion output divider for GLC. Only used in ProASIC3/Fusion technology. Set this value to 0 to dis-able generation of GLC.	0 - 32	0

20.4 Signal descriptions

Table 190 shows the interface signals of the core (VHDL ports).

*Table 190.*Signal descriptions

Signal name	Field	Type	Function	Active
CLKIN	N/A	Input	Reference clock input	-
PCICLKIN	N/A	Input	PCI clock input	
CLK	N/A	Output	Main clock	-
CLKN	N/A	Output	Inverted main clock	-
CLK2X	N/A	Output	2x clock	-
SDCLK	N/A	Output	SDRAM clock	-
PCICLK	N/A	Output	PCI clock	-
CGI	PLLREF	Input	Optional reference for PLL	-
	PLLRST	Input	Optional reset for PLL	
	PLLCTRL	Input	Optional control for PLL	
	CLKSEL	Input	Optional clock select	
CGO	CLKLOCK	Output	Lock signal for main clock	
	PCILOCK	Output	Lock signal for PCI clock	
CLK4X	N/A	Output	4x clock	
CLK1XU	N/A	Output	Unscaled 1x clock	
CLK2XU	N/A	Output	Unscaled 2x clock	
CLKB	N/A	Output	GLB output from ProASIC3/Fusion PLL	-
CLKC	N/A	Output	GLC output from ProASIC3/Fusion PLL	

20.5 Signal definitions and reset values

The signals and their reset values are described in table 191.

*Table 191.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
clk	Input	System clock	Rising edge	-

20.6 Timing

The timing waveforms and timing parameters are shown in figure 56 and are defined in table 192.

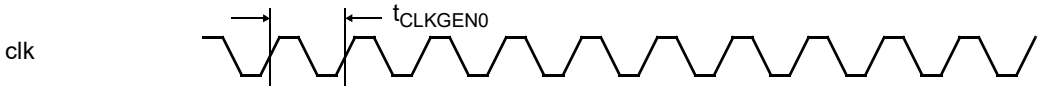


Figure 56. Timing waveforms

*Table 192.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{CLKGEN0}$	clock period	-	TBD	-	ns

20.7 Library dependencies

Table 193 shows the libraries used when instantiating the core (VHDL libraries).

*Table 193.*Library dependencies

Library	Package	Imported unit(s)	Description
TECHMAP	GENCOMP	Component, signals	Core signal definitions
TECHMAP	ALLCLKGEN	Component	Technology specific CLKGEN components

20.8 Instantiation

This example shows how the core can be instantiated together with the GRLIB reset generator.

```
library ieee;
use ieee.std_logic_1164.all;
library techmap;
use techmap.gencomp.all;
library gaisler;
use gaisler.misc.all;

entity clkgen_ex is
  port (
    resetn  : in  std_ulogic;
    clk  : in  std_ulogic; -- 50 MHz main clock
    pllref   : in  std_ulogic
  );
end;

architecture example of clkgen_ex is

signal lclk, clkm, rstn, rstraw, sdclkl, clk50: std_ulogic;
signal cgi   : clkgen_in_type;
signal cgo   : clkgen_out_type;

begin
  cgi.pllctrl <= "00"; cgi.pllrst <= rstraw;

  pllref_pad : clkpad generic map (tech => padtech) port map (pllref, cgi.pllref);

  clk_pad : clkpad generic map (tech => padtech) port map (clk, lclk);

  clkgen0 : clkgen  -- clock generator
    generic map (clktech, CFG_CLKMUL, CFG_CLKDIV, CFG_MCTRL_SDEN,
                 CFG_CLK_NOFB, 0, 0, 0, BOARD_FREQ)
    port map (lclk, lclk, clkm, open, open, sdclkl, open, cgi, cgo, open, clk50);

  sdclk_pad : outpad generic map (tech => padtech, slew => 1, strength => 24)
    port map (sdclk, sdclkl);

  resetn_pad : inpad generic map (tech => padtech) port map (resetn, rst);

  rst0 : rstgen  -- reset generator
    port map (rst, clkm, cgo.clklock, rstn, rstraw);

end;
```

21 DDRSPA - 16-, 32- and 64-bit DDR266 Controller

21.1 Overview

DDRSPA is a DDR266 SDRAM controller with AMBA AHB back-end. The controller can interface two 16-, 32- or 64-bit DDR266 memory banks to a 32-bit AHB bus. The controller acts as a slave on the AHB bus where it occupies a configurable amount of address space for DDR SDRAM access. The DDR controller is programmed by writing to a configuration register mapped located in AHB I/O address space. Internally, DDRSPA consists of a ABH/DDR controller and a technology specific DDR PHY. For currently supported technologies for the PHY see section 21.6.2. The modular design of DDRSPA allows to add support for other target technologies in a simple manner.

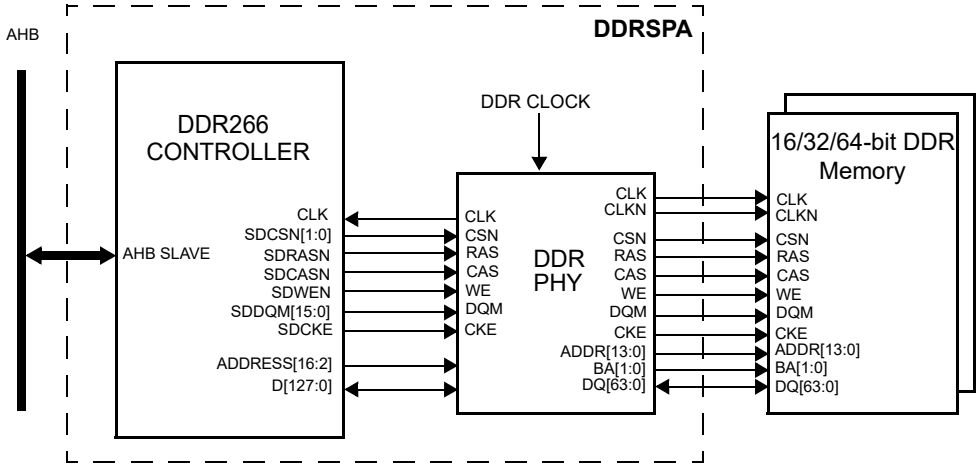


Figure 57. DDRSPA Memory controller conected to AMBA bus and DDR SDRAM

21.2 Operation

21.2.1 General

Double data-rate SDRAM (DDR RAM) access is supported to two banks of 16-, 32- or 64-bit DDR266 compatible memory devices. The controller supports 64M, 128M, 256M, 512M and 1G devices with 9- 12 column-address bits, up to 14 row-address bits, and 4 internal banks. The size of each of each chip select can be programmed in binary steps between 8 Mbyte and 1024 Mbyte. The DDR data width is set by the *ddrbits* VHDL generic, and will affect the width of DM, DQS and DQ signals. The DDR data width does not change the behavior of the AHB interface, except for data latency. When the VHDL generic *mobile* is set to a value not equal to 0, the controller supports mobile DDR SDRAM (LPDDR).

21.2.2 Read cycles

An AHB read access to the controller will cause a corresponding access to the external DDR RAM. The read cycle is started by performing an ACTIVATE command to the desired bank and row, followed by a READ command. CAS latency of 2 (CL=2) or 3 (CL=3) can be used. Byte, half-word (16-bit) and word (32-bit) AHB accesses are supported. Incremental AHB burst access are supported for 32-bit words only. The read cycle(s) are always terminated with a PRE-CHARGE command, no banks are left open between two accesses. DDR read cycles are always performed in (aligned) 8-word bursts, which are stored in a FIFO. After an initial latency, the data is then read out on the AHB bus with zero waitstates.

21.2.3 Write cycles

Write cycles are performed similarly to read cycles, with the difference that WRITE commands are issued after activation. An AHB write burst will store up to 8 words in a FIFO, before writing the data to the DDR memory. As in the read case, only word bursts are supported

21.2.4 Initialization

If the *pwron* VHDL generic is 1, then the DDR controller will automatically perform the DDR initialization sequence as described in the JEDEC DDR266 standard: PRE-CHARGE, LOAD-EXTMODE-REG, LOAD-MODE-REG, PRE-CHARGE, 2xREFRESH and LOAD-MODE-REG; or as described in the JEDEC LPDDR standard when mobile DDR is enabled: PRE-CHARGE, 2xREFRESH, LOAD-MODE-REG and LOAD-EXTMODE-REG. The VHDL generics *col* and *Mbyte* can be used to also set the correct address decoding after reset. In this case, no further software initialization is needed. The DDR initialization can be performed at a later stage by setting bit 15 in the DDR control register.

21.2.5 Configurable DDR SDRAM timing parameters

To provide optimum access cycles for different DDR devices (and at different frequencies), three timing parameters can be programmed through the memory configuration register (SDCFG): TRCD, TRP and TRFCD. The value of these field affects the SDRAM timing as described in table 194.

*Table 194.*DDR SDRAM programmable minimum timing parameters

SDRAM timing parameter	**Minimum timing (clocks)**
Precharge to activate (t_{RP})	TRP + 2
Auto-refresh command period (t_{RFC})	TRFC + 3
Activate to read/write (t_{RCD})	TRCD + 2
Activate to Activate (t_{RC})	TRCD + 8
Activate to Precharge (t_{RAS})	TRCD + 6

If the TCD, TRP and TRFC are programmed such that the DDR200/266 specifications are fulfilled, the remaining SDRAM timing parameters will also be met. The table below shows typical settings for 100 and 133 MHz operation and the resulting SDRAM timing (in ns):

*Table 195.*DDR SDRAM example programming

DDR SDRAM settings	**t_{RCD}**	**t_{RC}**	**t_{RP}**	**t_{RFC}**	**t_{RAS}**
100 MHz: CL=2, TRP=0, TRFC=4, TRCD=0	20	80	20	70	60
133 MHz: CL=2, TRP=1, TRFC=6, TRCD=1	22.5	75	22.5	67.5	52.5

When the DDRSPA controller uses CAS latency (CL) of two cycles a DDR SDRAM speed grade of -75Z or better is needed to meet 133 MHz timing.

When mobile DDR support is enabled, two additional timing parameters can be programmed though the Power-Saving configuration register.

*Table 196.*Mobile DDR SDRAM programmable minimum timing parameters

SDRAM timing parameter	**Minimum timing (clocks)**
Exit Power-down mode to first valid command (t_{XP})	TXP + 1
Exit Self Refresh mode to first valid command (t_{XSR})	TXSR + 1
CKE minimum pulse width (t_{CKE})	TCKE + 1

21.2.6 Extended timing fields

The DDRSPA controller can be configured with extended timing fields to provide support for DDR333 and DDR400. These fields can be detected by checking the XTF bit in the SDCFG register.

When the extended timing fields are enabled, extra upper bits are added to increase the range of the TRP, TRFC, TXSR and TXP fields. A new TWR field allow increasing the write recovery time. A new TRAS field to directly control the Active to Precharge period has been added.

*Table 197.*DDR SDRAM extended timing parameters

SDRAM timing parameter	Minimum timing (clocks)
Activate to Activate (t_{RC})	TRAS+TRCD + 2
Activate to Precharge (t_{RAS})	TRAS + 6
Write recovery time (t_{WR})	TWR+2

*Table 198.*DDR SDRAM extended timing example programming

DDR SDRAM settings	t_{RCD}	t_{RC}	t_{RP}	t_{RFC}	t_{RAS}	t_{WR}
166 MHz: CL=2, TRP=1, TRFC=9, TRCD=1, TRAS=1, TWR=1	18	60	18	72	42	18
200 MHz: CL=3, TRP=1, TRFC=11, TRCD=1, TRAS=2, TWR=1	15	55	15	70	40	15

21.2.7 Refresh

The DDRSPA controller contains a refresh function that periodically issues an AUTO-REFRESH command to both SDRAM banks. The period between the commands (in clock periods) is programmed in the refresh counter reload field in the SDCFG register. Depending on SDRAM type, the required period is typically 7.8 us (corresponding to 780 at 100 MHz). The generated refresh period is calculated as (reload value+1)/sysclk. The refresh function is enabled by bit 31 in SDCTRL register.

21.2.8 Self Refresh

The self refresh mode can be used to retain data in the SDRAM even when the rest of the system is powered down. When in the self refresh mode, the SDRAM retains data without external clocking and refresh are handled internally. The memory array that is refreshed during the self refresh operation is defined in the extended mode register. These settings can be changed by setting the PASR bits in the Power-Saving configuration register. The extended mode register is automatically updated when the PASR bits are changed. The supported “Partial Array Self Refresh” modes are: Full, Half, Quarter, Eighth, and Sixteenth array. “Partial Array Self Refresh” is only supported when mobile DDR functionality is enabled. To enable the self refresh mode, set the PMODE bits in the Power-Saving configuration register to “010” (Self Refresh). The controller will enter self refresh mode after every memory access (when the controller has been idle for 16 clock cycles), until the PMODE bits are cleared. When exiting this mode and mobile DDR is disabled, the controller introduce a delay of 200 clock cycles and a AUTO REFRESH command before any other memory access is allowed. When mobile DDR is enabled the delay before the AUTO REFRESH command is defined by tXSR in the Power-Saving configuration register. The minimum duration of this mode is defined by tRFC. This mode is only available when the VHDL generic *mobile* is >= 1.

21.2.9 Clock Stop

In the clock stop mode, the external clock to the SDRAM is stop at a low level (DDR_CLK is low and DDR_CLKB is high). This reduce the power consumption of the SDRAM while retaining the data. To enable the clock stop mode, set the PMODE bits in the Power-Saving configuration register to “100” (Clock Stop). The controller will enter clock stop mode after every memory access (when the controller has been idle for 16 clock cycles), until the PMODE bits are cleared. The REFRESH command

will still be issued by the controller in this mode. This mode is only available when the VHDL generic *mobile* is >= 1 and mobile DDR functionality is enabled.

21.2.10 Power-Down

When entering the power-down mode all input and output buffers, including DDR_CLK and DDR_-CLKB and excluding DDR_CKE, are deactivated. This is a more efficient power saving mode then clock stop mode, with a grater reduction of the SDRAM's power consumption. All data in the SDRAM is retained during this operation. To enable the power-down mode, set the PMODE bits in the Power-Saving configuration register to "001" (Power-Down). The controller will enter power-down mode after every memory access (when the controller has been idle for 16 clock cycles), until the PMODE bits is cleared. The REFRESH command will still be issued by the controller in this mode. When exiting this mode a delay of one or two (when tXP in the Power-Saving configuration register is '1') clock cycles are added before issue any command to the memory. This mode is only available when the VHDL generic *mobile* is >= 1.

21.2.11 Deep Power-Down

The deep power-down operating mode is used to achieve maximum power reduction by eliminating the power of the memory array. Data will not be retained after the device enters deep power-down mode. To enable the deep power-down mode, set the PMODE bits in the Power-Saving configuration register to "101" (Deep Power-Down). To exit the deep power-down mode the PMODE bits in the Power-Saving configuration register must be cleared followed by the mobile SDRAM initialization sequence. The mobile SDRAM initialization sequence can be performed by setting bit 15 in the DDR control register. This mode is only available when the VHDL generic *mobile* is >= 1 and mobile DDR functionality is enabled.

21.2.12 Status Read Register

The status read register (SRR) is used to read the manufacturer ID, revision ID, refresh multiplier, width type, and density of the SDRAM. To Read the SSR a LOAD MODE REGISTER command with BA0 = 1 and BA1 = 0 must be issued followed by a READ command with the address set to 0. This command sequence is executed then the Status Read Register is read. This register is only available when the VHDL generic *mobile* is >= 1 and mobile DDR functionality is enabled. Only DDR_CSB[0] is enabled during this operation.

21.2.13 Temperature-Compensated Self Refresh

The settings for the temperature-compensation of the Self Refresh rate can be controlled by setting the TCSR bits in the Power-Saving configuration register. The extended mode register is automatically updated when the TCSR bits are changed. Note that some vendors implements a Internal Temperature-Compensated Self Refresh feature, which makes the memory to ignore the TCSR bits. This functionality is only available when the VHDL generic *mobile* >= 1 and mobile DDR functionality is enabled.

21.2.14 Drive Strength

The drive strength of the output buffers can be controlled by setting the DS bits in the Power-Saving configuration register. The extended mode register is automatically updated when the DS bits are changed. The available options are: full, three-quarter, one-half, and one-quarter drive strengths. This functionality is only available when the VHDL generic *mobile* is >= 1 and mobile DDR functionality is enabled.

21.2.15 SDRAM commands

The controller can issue four SDRAM commands by writing to the SDRAM command field in SDCFG: PRE-CHARGE, LOAD-EXTMODE-REG, LOAD-MODE-REG and REFRESH. If the LEMR command is issued, the PLL Reset bit as programmed in SDCFG will be used, when mobile DDR support is enabled the DS, TCSR and PASR as programmed in Power-Saving configuration register will be used. If the LMR command is issued, the CAS latency as programmed in the Power-Saving configuration register will be used and remaining fields are fixed: 8 word sequential burst. The command field will be cleared after a command has been executed.

21.2.16 Clocking

The DDR controller is designed to operate with two clock domains, one for the DDR memory clock and one for the AHB clock. The two clock domains do not have to be the same or be phase-aligned. The DDR input clock (CLK_DDR) can be multiplied and divided by the DDR PHY to form the final DDR clock frequency. The final DDR clock is driven on one output (CLKDDRO), which should always be connected to the CLKDDRI input. If the AHB clock and DDR clock area generated from the same clock source, a timing-ignore constraint should be placed between the CLK_AHB and CLKDDRI to avoid optimization of false-paths during synthesis and place&route.

The Xilinx version of the PHY generates the internal DDR read clock using an external clock feed-back. The feed-back should have the same delay as DDR signals to and from the DDR memories. The feed-back should be driven by DDR_CLK_FB_OUT, and returned on DDR_CLK_FB. Most Xilinx FPGA boards with DDR provides clock feed-backs of this sort. The supported frequencies for the Xilinx PHY depends on the clock-to-output delay of the DDR output registers, and the internal delay from the DDR input registers to the read data FIFO. Virtex2 and Virtex4 can typically run at 120 MHz, while Spartan3e can run at 100 MHz.

The read data clock in the Xilinx version of the PHY is generated using a DCM to offset internal delay of the DDR clock feed back. If the automatic DCM phase adjustment does not work due to unsuitable pin selection, extra delay can be added through the RSKEW VHDL generic. The VHDL generic can be between -255 and 255, and is passed directly to the PHASE_SHIFT generic of the DCM.

The Altera version of the PHY use the DQS signals and an internal PLL to generate the DDR read clock. No external clock feed-back is needed and the DDR_CLK_FB_OUT/DDR_CLK_FB signals are not used. The supported frequencies for the Altera PHY are 100, 110, 120 and 130 MHz. For Altera CycloneIII, the read data clock is generated by the PLL. The phase shift of the read data clock is set be the VHDL generic RSKEW in ps (e.g. a value of 2500 equals 90’ phase for a 100MHz system).

21.2.17 Pads

The DDRSPA core has technology-specific pads inside the core. The external DDR signals should therefore be connected directly the top-level ports, without any logic in between.

21.2.18 Endianness

The core is designed for big-endian systems.

21.3 Registers

The DDRSPA core implements two control registers. The registers are mapped into AHB I/O address space defined by the AHB BAR1 of the core.

*Table 199.*DDR controller registers

Address offset - AHB I/O - BAR1	Register
0x00	SDRAM control register
0x04	SDRAM configuration register (read-only)
0x08	SDRAM Power-Saving configuration register
0x0C	Reserved
0x10	Status Read Register (Only available when mobile DDR support is enabled)
0x14	PHY configuration register 0 (Only available when VHDL generic confapi = 1, TCI RTL_PHY)
0x18	PHY configuration register 1 (Only available when VHDL generic confapi = 1, TCI TRL_PHY)

21.3.1 Control Register

Table 200. SDRAM control register (SDCTRL)

31	30	29 27	26	25 23	22 21	20 18	17	16	15	14 0
Refresh	tRP	tRFC	tRCD	SDRAM bank size	SDRAM col. size	SDRAM command	PR	IN	CE	SDRAM refresh load value

31 SDRAM refresh. If set, the SDRAM refresh will be enabled. This register bit is read only when Power-Saving mode is other then none.

30 SDRAM tRP timing. tRP will be equal to 2 or 3 system clocks (0/1). When mobile DDR support is enabled, this bit also represent the MSB in the tRFC timing.

29: 27 SDRAM tRFC timing. tRFC will be equal to 3 + field-value system clocks. When mobile DDR support is enabled, this field is extended with the bit 30.

26 SDRAM tRCD delay. Sets tRCD to 2 + field value clocks.

25: 23 SDRAM banks size. Defines the decoded memory size for each SDRAM chip select: “000”= 8 Mbyte, “001”= 16 Mbyte, “010”= 32 Mbyte .... “111”= 1024 Mbyte.

22: 21 SDRAM column size. “00”=512, “01”=1024, “10”=2048, “11”=4096

20: 18 SDRAM command. Writing a non-zero value will generate an SDRAM command: “010”=PRECHARGE, “100”=AUTO-REFRESH, “110”=LOAD-COMMAND-REGISTER, “111”=LOAD-EXTENDED-COMMAND-REGISTER. The field is reset after command has been executed.

17 PLL Reset. This bit is used to set the PLL RESET bit during LOAD-CONFIG-REG commands.

16 Initialize (IN). Set to ‘1’ to perform power-on DDR RAM initialisation. Is automatically cleared when initialisation is completed. This register bit is read only when Power-Saving mode is other then none.

15 Clock enable (CE). This value is driven on the CKE inputs of the DDR RAM. Should be set to ‘1’ for correct operation. This register bit is read only when Power-Saving mode is other then none.

14: 0 The period between each AUTO-REFRESH command - Calculated as follows: tREFRESH = ((reload value) + 1) / DDRCLOCK

21.3.2 Configuration Register

Table 201. SDRAM configuration register (SDCFG)

31 21	20	19 16	15	14 12	11 0
Reserved	XTF	CONFAPI	MD	Data width	DDR Clock frequency

31: 21 Reserved

20 Extended timing fields for DDR400 available

19: 16 Register API configuration.
0 = Standard register API.
1 = TCI TSMC90 PHY register API.

15 Mobile DDR support enabled. ‘1’ = Enabled, ‘0’ = Disabled (read-only)

14: 12 DDR data width: “001” = 16 bits, “010” = 32 bits, “011” = 64 bits (read-only)

11: 0 Frequency of the (external) DDR clock (read-only)

21.3.3 Power-Saving Configuration Register

*Table 202.*SDRAM Power-Saving configuration register

31	30	29 28	27 26	25	24	23 20	19	18 16	15 12	11	10	9	8 7 5	4 3	2 0
ME	CL	TRAS	xXS*	xXP	tC	tXSR	tXP	PMODE	Reserved	TWR	xTRP	xTRFC	DS	TCSR	PASR

*Table 202.*SDRAM Power-Saving configuration register

31	Mobile DDR functionality enabled. '1' = Enabled (support for Mobile DDR SDRAM), '0' = disabled (support for standard DDR SDRAM)
30	CAS latency; '0' => CL = 2, '1' => CL = 3
29: 28	SDRAM extended tRAS timing, tRAS will be equal to field-value + 6 system clocks. (Reserved when extended timing fields are disabled)
27: 26	SDRAM extended tXSR field, extend tXSR with field-value * 16 clocks (Reserved when extended timing fields are disabled)
25	SDRAM extended tXP field, extend tXP with 2*field-value clocks (Reserved when extended timing fields are disabled)
24	SDRAM tCKE timing, tCKE will be equal to 1 or 2 clocks (0/1). (Read only when Mobile DDR support is disabled).
23: 20	SDRAM tXSR timing. tXSR will be equal to field-value system clocks. (Read only when Mobile DDR support is disabled).
19	SDRAM tXP timing. tXP will be equal to 2 or 3 system clocks (0/1). (Read only when Mobile DDR support is disabled).
18: 16	Power-Saving mode (Read only when Mobile DDR support is disabled). "000": none "001": Power-Down (PD) "010": Self-Refresh (SR) "100": Clock-Stop (CKS) "101": Deep Power-Down (DPD)
15: 12	Reserved
11	SDRAM extended tWR timing, tWR will be equal to field-value + 2 clocks (Reserved when extended timing fields are disabled)
10	SDRAM extended tRP timing, extend tRP with field-value * 2 clocks
9: 8	SDRAM extended tRFC timing, extend tRFC with field-value * 8 clocks
7: 5	Selectable output drive strength (Read only when Mobile DDR support is disabled). "000": Full "001": One-half "010": One-quarter "011": Three-quarter
4: 3	Reserved for Temperature-Compensated Self Refresh (Read only when Mobile DDR support is disabled). "00": 70ªC "01": 45ªC "10": 15ªC "11": 85ªC
2: 0	Partial Array Self Refresh (Read only when Mobile DDR support is disabled). "000": Full array (Banks 0, 1, 2 and 3) "001": Half array (Banks 0 and 1) "010": Quarter array (Bank 0) "101": One-eighth array (Bank 0 with row MSB = 0) "110": One-sixteenth array (Bank 0 with row MSB = 00)

21.3.4 Status Read Register

Table 203. Status Read Register

31 16	15 0
SRR_16	SRR

31: 16 Status Read Register when 16-bit DDR memory is used (read only)

15: 0 Status Read Register when 32/64-bit DDR memory is used (read only)

21.3.5 PHY Configuration Register 0

Table 204. PHY configuration register 0 (TCI RTL_PHY only)

31	30	29	28	27 22	21 16	15 8	7 0
R1	R0	P1	P0	TSTCTRL1	TSTCTRL0	MDAJ_DLL1	MDAJ_DLL0

31 Reset DLL 1 (active high)

30 Reset DLL 1 (active high)

29 Power Down DLL 1 (active high)

28 Power Down DLL 1 (active high)

27: 22 Test control DLL 1
tstclkin(1) is connected to SIGI_1 on DDL 1 when bit 26:25 is NOT equal to “00“.
tstclkin(0) is connected to SIGI_0 on DDL 1 when bit 23:22 is NOT equal to “00“.

21: 16 Test control DLL 0

15: 8 Master delay adjustment input DLL 1

7: 0 Master delay adjustment input DLL 0

21.3.6 PHY Configuration Register 1

Table 205. PHY configuration register 1 (TCI RTL_PHY only)

31 24	23 16	15 8	7 0
ADJ_RSYNC	ADJ_90	ADJ_DQS1	ADJ_DQS0

31: 24 Slave delay adjustment input for resync clock (Slave 1 DLL 1)

23: 16 Slave delay adjustment input for 90’ clock (Slave 0 DLL 1)

15: 8 Slave delay adjustment input for DQS 1 (Slave 1 DLL 0)

7: 0 Slave delay adjustment input for DQS 0 (Slave 0 DLL 0)

21.4 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x025. For description of vendor and device identifiers see GRLIB IP Library User’s Manual.

21.5 Configuration options

Table 206 shows the configuration options of the core (VHDL generics).

*Table 206.*Configuration options

Generic	Function	Allowed range	Default
fabtech	PHY technology selection	virtex2, virtex4, spartan3e, altera	virtex2
memtech	Technology selection for DDR FIFOs	infered, virtex2, virtex4, spartan3e, altera	infered
hindex	AHB slave index	0 - NAHBSLV-1	0
haddr	ADDR field of the AHB BAR0 defining SDRAM area. Default is 0xF0000000 - 0xFFFFFFFF.	0 - 16#FFF#	16#000#
hmask	MASK field of the AHB BAR0 defining SDRAM area.	0 - 16#FFF#	16#F00#
ioaddr	ADDR field of the AHB BAR1 defining I/O address space where DDR control register is mapped.	0 - 16#FFF#	16#000#
iomask	MASK field of the AHB BAR1 defining I/O address space	0 - 16#FFF#	16#FFF#
ddrbits	Data bus width of external DDR memory	16, 32, 64	16
MHz	DDR clock input frequency in MHz.	10 - 200	100
clkmul, clkdiv	The DDR input clock is multiplied with the clkmul generic and divided with clkdiv to create the final DDR clock	2 - 32	2
rstdel	Clock reset delay in micro-seconds.	1 - 1023	200
col	Default number of column address bits	9 - 12	9
Mbyte	Default memory chip select bank size in Mbyte	8 - 1024	16
pwron	Enable SDRAM at power-on initialization	0 - 1	0
oepol	Polarity of bdrive and vbdrive signals. 0=active low, 1=active high	0 - 1	0
ahbfreq	Frequency in MHz of the AHB clock domain	1 - 1023	50
rskew	Additional read data clock skew Read data clock phase for Altera CycloneIII	-255 - 255. 0 - 9999	0
mobile	Enable Mobile DDR support 0: Mobile DDR support disabled 1: Mobile DDR support enabled but not default 2: Mobile DDR support enabled by default 3: Mobile DDR support only (no regular DDR support)	0 - 3	0
confapi	Set the PHY configuration register API: 0 = standard register API (conf0 and conf1 disabled). 1 = TCI RTL_PHY register API.		
conf0	Reset value for PHY register 0, conf[31:0]	0 - 16#FFFFFFFF#	0
conf1	Reset value for PHY register1, conf[63:32]	0 - 16#FFFFFFFF#	0
regoutput	Enables registers on signal going from controller to PHY	0 - 1	0
ddr400	Enables extended timing fields for DDR400 support	0 - 1	1
scantest	Enable scan test support	0 - 1	0
phyiconf	PHY implementation configuration. This generic sets technology specific implementation options for the DDR PHY. Meaning of values depend on the setting of VHDL generic *fabtech*. For fabtech:s virtex4, virtex5, virtex6: phyiconf selects type of pads used for DDR clock pairs. 0 instantiates a differiental pad and 1 instantiates two outpads.	0 - 16#FFFFFFFF#	0

21.6 Implementation

21.6.1 Technology mapping

The core has two technology mapping VHDL generics: *memtech* and *fabtech*. The VHDL generic *memtech* controls the technology used for memory cell implementation. The VHDL generic *fabtech* controls the technology used in the PHY implementation. See the GRLIB Users's Manual for available settings.

21.6.2 FPGA support

Complete PHY:s for a number FPGA technologies are included in the distribution, see table below. Unless otherwise noted these have been only functionally tested on evaluation board in lab environment and detailed timing analysis has not been performed. Note also that some of the FPGA phy:s use simplified sampling approaches which may require the memory timing to be better than the JEDEC standard specifies.

Scripts for post-layout static timing analysis are not included. Because these PHY:s are based on dedicated hard macros with fixed placement in the FPGA:s pad structure, just a minimal set of constraints are normally neccessary for synthesis purposes.

*Table 207.*FPGA DDR PHYs included in GRLIB

Technology	fabtech	Read clock method	Built-in pads
Virtex4,5,6	virtex4, virtex5, virtex6	Clock feedback loop + static shift	Yes
Virtex2, Spartan3	virtex2, spartan3	Clock feedback loop + static shift	Yes
Spartan3E,6	spartan3	Clock feedback loop + static shift	Yes
Stratix II	stratix2	Tech intrinsics (DQS based)	Yes
Cyclone 3	cyclone3	Static shift	Yes

21.6.3 RAM usage

The FIFOs in the core are implemented with the *syncram_2p* (with separate clock for each port) component found in the technology mapping library (TECHMAP). The number of RAMs used for the FIFO implementation depends on the DDR data width, set by the *ddrbits* VHDL generic.

*Table 208.*RAM usage

RAM dimension (depth x width)	Number of RAMs (DDR data width 64)	Number of RAMs (DDR data width 32)	Number of RAMs (DDR data width 16)
4 x 128	1		
4 x 32	4		
5 x 64		1	
5 x 32		2	
6 x 32			2

21.7 Signal descriptions

Table 209 shows the interface signals of the core (VHDL ports).

*Table 209.*Signal descriptions

Signal name	Type	Function	Active
RST_DDR	Input	Reset input for DDR clock domain	Low
RST_AHB	Input	Reset input for AHB clock domain	Low
CLK_DDR	Input	DDR input Clock	-
CLK_AHB	Input	AHB clock	-
LOCK	Output	DDR clock generator locked	High
CLKDDRO		Internal DDR clock output after clock multiplication	
CLKDDRI		Clock input for the internal DDR clock domain. Must be connected to CLKDDRO.	
AHBSI	Input	AHB slave input signals	-
AHBSO	Output	AHB slave output signals	-
DDR_CLK[2:0]	Output	DDR memory clocks (positive)	High
DDR_CLKB[2:0]	Output	DDR memory clocks (negative)	Low
DDR_CLK_FB_OUT	Output	Same a DDR_CLK, but used to drive an external clock feedback.	-
DDR_CLK_FB	Input	Clock input for the DDR clock feed-back	-
DDR_CKE[1:0]	Output	DDR memory clock enable	High
DDR_CSB[1:0]	Output	DDR memory chip select	Low
DDR_WEB	Output	DDR memory write enable	Low
DDR_RASB	Output	DDR memory row address strobe	Low
DDR_CASB	Output	DDR memory column address strobe	Low
DDR_DM[DDRBITS/8-1:0]	Output	DDR memory data mask	Low
DDR_DQS[DDRBITS/8-1:0]	Bidir	DDR memory data strobe	Low
DDR_AD[13:0]	Output	DDR memory address bus	Low
DDR_BA[1:0]	Output	DDR memory bank address	Low
DDR_DQ[DDRBITS-1:0]	BiDir	DDR memory data bus	-

1) see GRLIB IP Library User's Manual 2) Polarity selected with the oepol generic

21.8 Library dependencies

Table 210 shows libraries used when instantiating the core (VHDL libraries).

*Table 210.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AHB signal definitions
GAISLER	MEMCTRL	Signals, component	Memory bus signals definitions, component declaration

21.9 Component declaration

```
component ddrspa
  generic (
    fabtech : integer := 0;
    memtech : integer := 0;
    hindex  : integer := 0;
    haddr   : integer := 0;
    hmask   : integer := 16#f00#;
    ioaddr  : integer := 16#000#;
    iomask  : integer := 16#fff#;
    MHz     : integer := 100;
    clkmul  : integer := 2;
    clkdiv  : integer := 2;
    col     : integer := 9;
    Mbyte   : integer := 16;
    rstdel  : integer := 200;
    pwron   : integer := 0;
    oepol   : integer := 0;
    ddrbits : integer := 16;
    ahbfreq : integer := 50
  );
  port (
    rst_ddr : in  std_ulogic;
    rst_ahb : in  std_ulogic;
    clk_ddr : in  std_ulogic;
    clk_ahb : in  std_ulogic;
    lock    : out std_ulogic;-- DCM locked
    clkddro : out std_ulogic;-- DCM locked
    clkddri : in  std_ulogic;
    ahbsi   : in  ahb_slv_in_type;
    ahbso   : out ahb_slv_out_type;
    ddr_clk : out std_logic_vector(2 downto 0);
    ddr_clkb: out std_logic_vector(2 downto 0);
    ddr_clk_fb_out  : out std_logic;
    ddr_clk_fb  : in std_logic;
    ddr_cke  : out std_logic_vector(1 downto 0);
    ddr_csb  : out std_logic_vector(1 downto 0);
    ddr_web  : out std_ulogic;                        -- ddr write enable
    ddr_rasb  : out std_ulogic;                        -- ddr ras
    ddr_casb  : out std_ulogic;                        -- ddr cas
    ddr_dm   : out std_logic_vector (ddrbits/8-1 downto 0);    -- ddr dm
    ddr_dqs  : inout std_logic_vector (ddrbits/8-1 downto 0);    -- ddr dqs
    ddr_ad     : out std_logic_vector (13 downto 0);   -- ddr address
    ddr_ba     : out std_logic_vector (1 downto 0);    -- ddr bank address
    ddr_dq    : inout  std_logic_vector (ddrbits-1 downto 0) -- ddr data

  );
  end component;
```

21.10 Instantiation

This examples shows how the core can be instantiated.

The DDR SDRAM controller decodes SDRAM area at 0x40000000 - 0x7FFFFFFF. The SDRAM registers are mapped into AHB I/O space on address (AHB I/O base address + 0x100).

```
library ieee;
use ieee.std_logic_1164.all;
library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.memctrl.all;

entity ddr_Interface is
  port ( ddr_clk  : out std_logic_vector(2 downto 0);
    ddr_clkb  : out std_logic_vector(2 downto 0);
    ddr_clk_fb  : in std_logic;
    ddr_clk_fb_out  : out std_logic;
    ddr_cke  : out std_logic_vector(1 downto 0);
    ddr_csb  : out std_logic_vector(1 downto 0);
    ddr_web  : out std_ulogic;                        -- ddr write enable
    ddr_rasb  : out std_ulogic;                        -- ddr ras
    ddr_casb  : out std_ulogic;                        -- ddr cas
    ddr_dm   : out std_logic_vector (7 downto 0);    -- ddr dm
    ddr_dqs  : inout std_logic_vector (7 downto 0);    -- ddr dqs
    ddr_ad      : out std_logic_vector (13 downto 0);   -- ddr address
    ddr_ba      : out std_logic_vector (1 downto 0);    -- ddr bank address
    ddr_dq  : inout std_logic_vector (63 downto 0); -- ddr data

);
end;

architecture rtl of mctrl_ex is

  -- AMBA bus
signal ahbsi : ahb_slv_in_type;
signal ahbso : ahb_slv_out_vector := (others => ahbs_none);
signal clkml, lock : std_ulogic;


begin

-- DDR controller


ddrc : ddrspa generic map ( fabtech => virtex4, ddrbits => 64, memtech => memtech,
hindex => 4, haddr => 16#400#, hmask => 16#F00#, ioaddr => 1,
pwron => 1, MHz => 100, col => 9, Mbyte => 32, ahbfreq => 50, ddrbits => 64)
port map (
rstneg, rstn, lclk, clkm, lock, clkml, clkml,  ahbsi, ahbso(4),
ddr_clk, ddr_clkb, ddr_clk_fb_out, ddr_clk_fb,
ddr_cke, ddr_csb, ddr_web, ddr_rasb, ddr_casb,
ddr_dm, ddr_dqs, ddr_adl, ddr_ba, ddr_dq);
```

22 DDR2SPA - 16-, 32- and 64-bit Single-Port Asynchronous DDR2 Controller

22.1 Overview

DDR2SPA is a DDR2 SDRAM controller with AMBA AHB back-end. The controller can interface 16-, 32- or 64-bit wide DDR2 memory with one or two chip selects. The controller acts as a slave on the AHB bus where it occupies a configurable amount of address space for DDR2 SDRAM access. The DDR2 controller is programmed by writing to configuration registers mapped located in AHB I/O address space.

Internally, DDR2SPA consists of a ABH/DDR2 controller and a technology specific DDR2 PHY. For currently supported technologies for the PHY, see section 22.7.2. The modular design of DDR2SPA allows to add support for other target technologies in a simple manner.

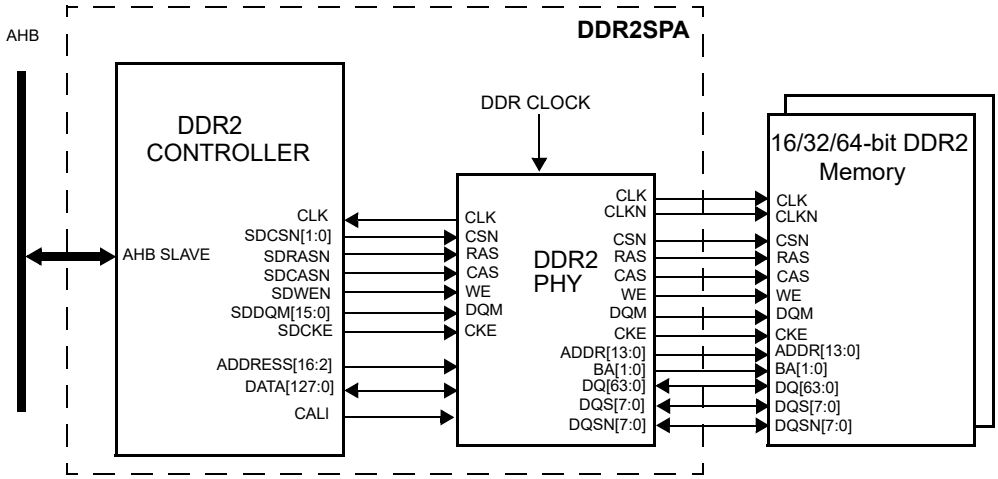


Figure 58. DDR2SPA Memory controller connected to AMBA bus and DDR2 SDRAM

22.2 Operation

22.2.1 General

Single DDR2 SDRAM chips are typically 4,8 or 16 data bits wide. By putting multiple identical chips side by side, wider SDRAM memory banks can be built. Since the command signals are common for all chips, the memories behave as one single wide memory chip.

This memory controller supports one or two (identical) such 16/32/64-bit wide DDR2 SDRAM memory banks. The size of the memory can be programmed in binary steps between 8 Mbyte and 1024 Mbyte, or between 32 Mbyte and 4096 Mbyte. The DDR data width is set by the DDRBITS generic, and will affect the width of DM, DQS and DQ signals. The DDR data width does not change the behavior of the AHB interface, except for data latency.

22.2.2 Data transfers

An AHB read or write access to the controller will cause a corresponding access cycle to the external DDR2 RAM. The cycle is started by performing an ACTIVATE command to the desired bank and row, followed by a sequence of READ or WRITE commands (the count depending on memory width and burst length setting). After the sequence, a PRECHARGE command is performed to deactivate the SDRAM bank.

All access types are supported, but only incremental bursts of 32 bit width and incremental bursts of maximum width (if wider than 32) are handled efficiently. All other bursts are handled as single-

accesses. For maximum throughput, incremental bursts of full AHB width with both alignment and length corresponding to the burstlen generic should be performed.

The maximum supported access size can be limited by using the ahbbits generic, which is set to the full AHB bus size by default. Accesses larger than this size are not supported.

The memory controller's FIFO has room for two write bursts which improves throughput, since the second write can be written into the FIFO while the first write is being written to the DDR memory.

In systems with high DDR clock frequencies, the controller may have to insert wait states for the minimum activate-to-precharge time (t_{RAS}) to expire before performing the precharge command. If a new AHB access to the same memory row is performed during this time, the controller will perform the access in the same access cycle.

22.2.3 Initialization

If the **pwron** VHDL generic is 1, then the DDR2 controller will automatically on start-up perform the DDR2 initialization sequence as described in the JEDEC DDR2 standard. The VHDL generics **col** and **Mbyte** can be used to also set the correct address decoding after reset. In this case, no further software initialization is needed except for enabling the auto-refresh function. If power-on initialization is not enabled, the DDR2 initialization can be started at a later stage by setting bit 16 in the DDR2 control register DDR2CFG1.

22.2.4 Big memory support

The total memory size for each chip select is set through the 3-bit wide SDRAM banks size field, which can be set in binary steps between 8 Mbyte and 1024 Mbyte. To support setting even larger memory sizes of 2048 and 4096 Mbyte, a fourth bit has been added to this configuration field.

Only 8 different sizes are supported by the controller, either the lower range of 8 MB - 1 GB, or the higher range of 32 MB - 4 GB. Which range is determined by the bigmem generic, and can be read by software through the DDR2CFG2 register.

22.2.5 Configurable DDR2 SDRAM timing parameters

To provide optimum access cycles for different DDR2 devices (and at different frequencies), six timing parameters can be programmed through the memory configuration registers: TRCD, TCL, TRTP, TWR, TRP and TRFC. For faster memories (DDR2-533 and higher), the TRAS setting also needs to be configured to satisfy timing. The value of these fields affects the DDR2RAM timing as described in table 211. Note that if the CAS latency setting is changed after initialization, this change needs also to be programmed into the memory chips by executing the Load Mode Register command.

*Table 211.*DDR2 SDRAM programmable minimum timing parameters

DDR2 SDRAM timing parameter	Minimum timing (clocks)
CAS latency, CL	TCL + 3
Activate to read/write command (t_{RCD})	TRCD + 2
Read to precharge (t_{RTP})	TRTP + 2
Write recovery time (t_{WR})	TWR-2
Precharge to activate (t_{RP})	TRP + 2
Activate to precharge (t_{RAS})	TRAS + 1
Auto-refresh command period (t_{RFC})	TRFC + 3

If TRCD, TCL, TRTP, TWR, TRP, TRFC and TRAS are programmed such that the DDR2 specifications are full filled, the remaining SDRAM timing parameters will also be met. The table below

shows typical settings for 130, 200 and 400 MHz operation and the resulting DDR2 SDRAM timing (in ns):

*Table 212.*DDR2 SDRAM example programming

DDR2 SDRAM settings	CL	t_{RCD}	t_{RC}	t_{RP}	t_{RFC}	t_{RAS}
130 MHz: TCL=0,TRCD=0,TRTP=0,TRP=0,TRAS=0,TRFC=7	3	15	76	15	76	61
200 MHz: TCL=0,TRCD=1,TRTP=0,TRP=1,TRAS=1,TRFC=13	3	15	60	15	80	45
400 MHz: TCL=2,TRCD=4,TRTP=1,TRP=4,TRAS=10,TRFC=29	5	15	60	15	80	45

22.2.6 Refresh

The DDR2SPA controller contains a refresh function that periodically issues an AUTO-REFRESH command to both SDRAM banks. The period between the commands (in clock periods) is programmed in the refresh counter reload field in the DDR2CFG1 register. Depending on SDRAM type, the required period is typically 7.8 us (corresponding to 780 at 100 MHz). The generated refresh period is calculated as (reload value+1)/sysclk. The refresh function is enabled by bit 31 in DDR2CFG1 register.

22.2.7 DDR2 SDRAM commands

The controller can issue four SDRAM commands by writing to the SDRAM command field in SDCFG1: PRE-CHARGE, LOAD-EXTMODE-REG, LOAD-MODE-REG and REFRESH. If the LMR command is issued, the PLL Reset bit as programmed in DDR2CFG1, CAS Latency setting as programmed in DDR2CFG4 and the WR setting from DDR2CFG3 will be used, remaining fields are fixed: 4 word sequential burst. If the LEMR command is issued, the OCD bits will be used as programmed in the DDR2CFG1 register, and all other bits are set to zero. The command field will be cleared after a command has been executed.

22.2.8 Registered SDRAM

Registered memory modules (RDIMM:s) have one cycle extra latency on the control signals due to the external register. They can be supported with this core by setting the REG bit in the DDR2CFG4 register.

This should not be confused with Fully-Buffered DDR2 memory, which uses a different protocol and is not supported by this controller.

22.2.9 Clocking

The DDR2 controller operates in two separate clock domains, one domain synchronous to the DDR2 memory and one domain synchronous to the AHB bus. The two clock domains do not have to be the same or be phase-aligned.

The clock for the DDR2 memory domain is generated from the controller's ddr_clk input via a technology-specific PLL component. The multiplication and division factor can be selected via the clkmul/clkdiv configuration options. The final DDR2 clock is driven on one output (CLKDDRO), which should always be connected to the CLKDDRI input.

The ddr_rst input asynchronously resets the PHY layer and the built-in PLL. The ahb_rst input should be reset simultaneously and then kept in reset until the PLL has locked (indicated by the lock output).

If the AHB and DDR2 clocks are based on the same source clock and are kept phase-aligned by the PLL, the clock domain transition is synchronous to the least common multiple of the two clock frequencies. In this case, the nosync configuration option can be used to remove the synchronization and handshaking between the two clock domains, which saves a few cycles of memory access latency. If nosync is not set in this case, a timing-ignore constraint should be placed between the CLK_AHB and CLKDDRI to avoid optimization of false-paths during synthesis and place&route.

The supported DDR2 frequencies depends on the clock-to-output delay of the DDR output registers, and the internal delay from the DDR input registers to the read data FIFO. Virtex5 can typically run at 200 MHz.

When reading data, the data bus (DQ) signals should ideally be sampled 1/4 cycle after each data strobe (DQS) edge. How this is achieved is technology-specific as described in the following sections.

22.2.10 Read data clock calibration on Xilinx Virtex

On Xilinx Virtex4/5 the data signal inputs are delayed via the I/O pad IDELAY feature to get the required 1/4 cycle shift. The delay of each byte lane is tuned independently between 0-63 tap delays, each tap giving 78 ps delay, and the initial value on startup is set via the generics ddelayb[7:0].

The delays can be tuned at runtime by using the DDR2CFG3 control register. There are two bits in the control register for each byte. One bit determines if the delay should be increased or decreased and the other bit is set to perform the update. Setting bit 31 in the DDR2CFG3 register resets the delays to the initial value.

To increase the calibration range, the controller can add additional read latency cycles. The number of additional read latency cycles is set by the RD bits in the DDR2CFG3 register.

22.2.11 Read data clock calibration on Altera Stratix

On Altera StratixIII, the technology's delay chain feature is used to delay bytes of input data in a similar fashion as the Virtex case above. The delay of each byte lane is tuned between 0-15 tap delays, each tap giving 50 ps delay, and the initial value on startup is 0.

The delays are tuned at runtime using the DDR2CFG3 register, and extra read cycles can be added using DDR2CFG3, the same way as described for Virtex.

The data sampling clock can also be skewed on Stratix to increase the calibration range. This is done writing the PLL_SKEW bits in the DDR2CFG3 register.

22.2.12 Read data clock calibration on Xilinx Spartan-3

On Spartan3, a clock loop is utilized for sampling of incoming data. The DDR_CLK_FB_OUT port should therefore be connected to a signal path of equal length as the DDR_CLK + DDR_DQS signal path. The other end of the signal path is to be connected to the DDR_CLK_FB port. The fed back clock can then be skewed for alignment with incoming data using the rskew generic. The rskew generic can be set between +/-255 resulting in a linear +/-360 degree change of the clock skew. Bits 29 and 30 in the DDR2CFG3 register can be used for altering the skew at runtime.

22.2.13 Pads

The DDR2SPA core has technology-specific pads inside the core. The external DDR2 signals should therefore be connected directly the top-level ports, without any logic in between.

22.2.14 Endianness

The core is designed for big-endian systems.

22.3 Fault-tolerant operation (preliminary)

22.3.1 Overview

The memory controller can be configured to support bit-error tolerant operation by setting the ft generic (not supported in all versions of GRLIB). In this mode, the DDR data bus is widened and the extra bits are used to store 16 or 32 checkbits corresponding to each 64 bit data word. The variant to

be used can be configured at run-time depending on the connected DDR2 data width and the desired level of fault tolerance.

When writing, the controller generates the check bits and stores them along with the data. When reading, the controller will transparently correct any correctable bit errors and provide the corrected data on the AHB bus. However, the corrected bits are not written back to the memory so external scrubbing is necessary to avoid uncorrectable errors accumulating over time.

An extra corrected error output signal is asserted when a correctable read error occurs, at the same cycle as the corrected data is delivered. This can be connected to an interrupt input or to a memory scrubber. In case of uncorrectable error, this is signaled by giving an AHB error response to the master.

22.3.2 Memory setup

In order to support error-correction, the DDR2 data bus needs to be expanded. The different possible physical configurations are tabulated below. For software, there is no noticeable difference between these configurations.

If the hardware is built for the wider code, it is still possible to leave the upper half of the checkbit data bus unconnected and use it for code B.

*Table 213.*Configurations of FT DDR2 memory banks

Data bits (DDRBITS)	Checkbits (FTBITS)	Interleaving modes supported
64	32	A and B
64	16	B only
32	16	A and B
32	8	B only
16	8	A only

22.3.3 Error-correction properties

The memory controller uses an interleaved error correcting code which works on nibble (4-bit) units of data. The codec can be used in two interleaving modes, mode A and mode B.

In mode A, the basic code has 16 data bits, 8 check bits and can correct one nibble error. This code is interleaved by 4 using the pattern in table 214 to create a code with 64 data bits and 32 check bits.

This code can tolerate one nibble error in each of the A,B,C,D groups shown below. This means that we can correct 100% of single errors in two adjacent nibbles, or in any 8/16-bit wide data bus lane, that would correspond to a physical DDR2 chip. The code can also correct 18/23=78% of all possible random two-nibble errors.

This interleaving pattern was designed to also provide good protection in case of reduced (32/16-bit) DDR bus width with the same data-checkbit relation, so software will see the exact same checkbits on diagnostic reads.

In mode B, the basic code has 32 data bits, 8 check bits and can correct one nibble error. This code is then interleaved by a factor of two to create a code with 64 data bits and 16 check bits.

Note that when configured for a 16-bit wide DDR data bus, code A must be used to get protection from multi-column errors since each data bus nibbles holds four code word nibbles.

*Table 214.*Mode Ax4 interleaving pattern (64-bit data width)

63:60	59:56	55:52	51:48	47:44	43:40	39:36	35:32	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
C	D	A	B	A	B	C	D	B	A	D	C	D	C	B	A
								127:120	119:112	111:104	103:96	95:88	87:80	79:72	71:64
								C_{cb}	D_{cb}	A_{cb}	B_{cb}	C_{cb}	D_{cb}	A_{cb}	B_{cb}

*Table 215.*Mode Bx2 interleaving pattern (64-bit data width)

63:60	59:56	55:52	51:48	47:44	43:40	39:36	35:32	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
A	B	A	B	A	B	A	B	B	A	B	A	B	A	B	A

95:88	87:80	79:72	71:64
A_{cb}	B_{cb}	A_{cb}	B_{cb}

22.3.4 Data transfers

The read case behaves the same way as the non-FT counterpart, except a few cycles extra are needed for error detection and correction. There is no extra time penalty in the case data is corrected compared to the error-free case.

Only writes of 64 bit width or higher will translate directly into write cycles to the DDR memory. Other types of write accesses will generate a read-modify-write cycle in order to correctly update the check-bits. In the special case where an uncorrectable error is detected while performing the RMW cycle, the write is aborted and the incorrect checkbits are left unchanged so they will be detected upon the next read.

Only bursts of maximum AHB width is supported, other bursts will be treated as single accesses.

The write FIFO only has room for one write (single or burst).

22.3.5 DDR2 behavior

The behavior over the DDR2 interface is largely unchanged, the same timing parameters and setup applies as for the non-FT case. The checkbit data and data-mask signals follow the same timing as the corresponding signals for regular data.

22.3.6 Configuration

Whether the memory controller is the FT or the non-FT version can be detected by looking at the FTV bit in the DDR2CFG2 register.

Checkbits are always written out to memory when writing even if EDACEN is disabled. Which type of code, A or B, that is used for both read and write is controlled by the CODE field in the DDR2FTCFG register.

Code checking on read is disabled on reset and is enabled by setting the EDACEN bit in the DDR2FTCFG register. Before enabling this, the code to be used should be set in the CODE field and the memory contents should be (re-)initialized.

22.3.7 Diagnostic checkbit access

The checkbits and data can be accessed directly for testing and fault injection. This is done by writing the address of into the DDR2FTDA register. The check-bits and data can then be read and written via the DDR2FTDC and DDR2FTDD register. Note that for checkbits the DDR2FTDA address is 64-bit aligned, while for data it is 32-bit aligned.

After the diagnostic data register has been read, the FT control register bits 31:19 can be read out to see if there were any correctable or uncorrectable errors detected, and where the correctable errors were located. For the 64 databit wide version, there is one bit per byte lane describing whether a correctable error occurred.

22.3.8 Code boundary

The code boundary feature allows you to gradually switch the memory from one interleaving mode to the other and regenerate the checkbits without stopping normal operation. This can be used when recovering from memory faults, as explained further below.

If the boundary address enable (BAEN) control bit is set, the core will look at the address of each access, and use the interleaving mode selected in the CODE field for memory accesses above or equal to the boundary address, and the opposite code for memory accesses below to the boundary address.

If the boundary address update (BAUPD) control bit is also set, the core will shift the boundary upwards whenever the the address directly above the boundary is written to. Since the written data is now below the boundary, it will be written using the opposite code. The write can be done with any size supported by the controller.

22.3.9 Data muxing

When code B is used instead of code A, the upper half of the checkbits are unused. The controller supports switching in this part of the data bus to replace another faulty part of the bus. To do this, one sets the DATAMUX field to a value between 1-4 to replace a quarter of the data bus, or to 5 to replace the active checkbit half.

22.3.10 Memory fault recovery

The above features are designed to, when combined and integrated correctly, make the system cabable to deal with a permanent fault in an external memory chip.

A basic sequence of events is as follows:

1. The system is running correctly with EDAC enabled and the larger code A is used.
2. A memory chip gets a fault and delivers incorrect data. The DDR2 controller keeps delivering error-free data but reports a correctable error on every read access.
3. A logging device (such as the memory scrubber core) registers the high frequency of correctable errors and signals an interrupt.
4. The CPU performs a probe using the DDR2 FT diagnostic registers to confirm that the error is permanent and on which physical lane the error is.
5. After determining that a permanent fault has occurred, the CPU reconfigures the FTDDR2 controller as follows (all configuration register fields changed with a single register write):

   The data muxing control field is set so the top checkbit half replaces the failed part of the data bus.

   The code boundary register is set to the lowest memory address.

   The boundary address enable and boundary address update enable bits are set.

   The mask correctable error bit is set
6. The memory data and checkbits are now regenerated using locked read-write cycles to use the smaller code and replace the broken data with the upper half of the checkbit bus. This can be done in hardware using an IP core, such as the AHB memory scrubber, or by some other means depending on system design.
7. After the whole memory has been regenerated, the CPU disables the code boundary, changes the code selection field to code B, and unsets the mask correctable error bit.

After this sequence, the system is now again fully operational, but running with the smaller code and replacement chip and can again recover from any single-nibble error. Note that during this sequence, it is possible for the system to operate and other masters can both read and write to memory while the regeneration is ongoing.

22.4 Registers

The DDR2SPA core implements between 5 and 12 control registers, depending on the FT generic and target technology. The registers are mapped into AHB I/O address space defined by the AHB BAR1 of the core. Only 32-bit single-accesses are supported to the registers.

Older revisions of the core only have registers DDRCFG1-4, which are aliased on the following addresses. For that reason, check the REG5 bit in DDR2CFG2 before using these bits for backward compatibility.

For backward compatibility, some of the bits in DDR2CFG5 are mirrored in other registers. Writing to these bits will affect the contents of DDR2CFG5 and vice versa.

*Table 216.*DDR2 controller registers

Address offset - AHB I/O - BAR1	Register
0x00	DDR2 SDRAM control register (DDR2CFG1)
0x04	DDR2 SDRAM configuration register (DDR2CFG2)
0x08	DDR2 SDRAM control register (DDR2CFG3)
0x0C	DDR2 SDRAM control register (DDR2CFG4)
0x10*	DDR2 SDRAM control register (DDR2CFG5)
0x14*	Reserved
0x18	DDR2 Technology specific register (DDR2TSR1)
0x1C*	DDR2 Technology specific register (DDR2TSR2)
0x20	DDR2 FT Configuration Register (FT only) (DDR2FTCFG)
0x24	DDR2 FT Diagnostic Address register (FT only) (DDR2FTDA)
0x28	DDR2 FT Diagnostic Checkbit register (FT only) (DDR2FTDC)
0x2C	DDR2 FT Diagnostic Data register (FT only) (DDR2FTDD)
0x30	DDR2 FT Code Boundary Register (FT only) (DDR2FTBND)

* Older DDR2SPA versions contain aliases of DDR2CFG1-4 at these addresses. Therefore, check bit 15 of DDR2CFG2 before using these registers.

22.4.1 DDR2 SDRAM Configuration Register 1

Table 217. 0x00 - DDR2CFG1 - DDR2 SRAM control register 1

31	30	29 28	27	26	25 23	22 21	20 18	17	16	15	14 0
Refresh	OCD	EMR	bank size 3	(TRCD)	SDRAM bank size2:0	SDRAM col. size	SDRAM command	PR	IN	CE	SDRAM refresh load value
0	0	0	0	0	0	0	0	0	0	0	0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

31 SDRAM refresh. If set, the SDRAM refresh will be enabled.

30 OCD operation

29: 28 Selects Extended mode register (1,2,3)

27 SDRAM banks size bit 3. By enabling this bit the memory size can be set to “1000” = 2048 Mbyte and “1001” = 4096 Mbyte. See the section on big-memory support.

26 Lowest bit of TRCD field in DDR2CFG, for backward compatibility

25: 23 SDRAM banks size. Defines the decoded memory size for each SDRAM chip select: “000”= 8 Mbyte, “001”= 16 Mbyte, “010”= 32 Mbyte.... “111”= 1024 Mbyte.

22: 21 SDRAM column size. “00”=512, “01”=1024, “10”=2048, “11”=4096

20: 18 SDRAM command. Writing a non-zero value will generate an SDRAM command: “010”=PRE-CHARGE, “100”=AUTO-REFRESH, “110”=LOAD-COMMAND-REGISTER, “111”=LOAD-EXTENDED-COMMAND-REGISTER. The field is reset after command has been executed.

17 PLL Reset. This bit is used to set the PLL RESET bit during LOAD-CONFIG-REG commands.

16 Initialize (IN). Set to ‘1’ to perform power-on DDR RAM initialisation. Is automatically cleared when initialisation is completed.

15 Clock enable (CE). This value is driven on the CKE inputs of the DDR RAM. Should be set to ‘1’ for correct operation.

14: 0 The period between each AUTO-REFRESH command - Calculated as follows: tREFRESH = ((reload value) + 1) / DDRCLOCK

22.4.2 DDR2 SDRAM Configuration Register 2

Table 218. 0x04 - DDR2CFG2 - DDR2 SDRAM configuration register 2

31 26	25 18	17	16	15	14 12	11 0
RESERVED	PHY Tech	BIG	FTV	REG5	Data width	DDR Clock frequency
0	0	0	0	0	0	0
r	r	r	r	r	r	r

31: 26 Reserved

25: 18 PHY technology identifier, value 0 is for generic/unknown

17 Big memory support, if ‘1’ then memory can be set between 32 Mbyte and 4 Gbyte, if ‘0’ then memory size can be set between 8 Mbyte and 1 Gbyte.

16 Reads ‘1’ if the controller is fault-tolerant version and EDAC registers exist.

15 Reads ‘1’ if DDR2CFG5 register exists.

14: 12 SDRAM data width: “001” = 16 bits, “010” = 32 bits, “011” = 64 bits.

11: 0 Frequency of the (external) DDR clock.

22.4.3 DDR2 SDRAM Configuration Register 3

*Table 219.*0x08 - DDR2CFG3 - DDR2 SDRAM configuration register 3

31	30 29	28	27 23	22 18	17 16	15 8	7 0
	PLL	(TRP)	tWR	(TRFC)	RD	inc/dec delay	Update delay
		0	0	*	*	0	0
		rw	rw	rw	rw	rw	rw

31 Reset byte delay

30: 29 PLL_SKEW
Bit 29: Update clock phase
Bit 30: 1 = Inc / 0 = Dec clock phase

28 Lowest bit of DDR2CFG4 TRP field for backward compatibility

27: 23 SDRAM write recovery time. tWR will be equal to field value - 2DDR clock cycles

22: 18 Lower 5 bits of DDR2CFG4 TRFC field for backward compatibility.

17: 16 Number of added read delay cycles, default = 1

15: 8 Set to '1' to increment byte delay, set to '0' to decrement delay

7: 0 Set to '1' to update byte delay

22.4.4 DDR2 SDRAM Configuration Register 4

*Table 220.*0x0C - DDR2CFG4 - DDR2 SDRAM configuration register 4

31 28	27 24	23 22	21	20 14	13	12 11	10 9	8	7 0
inc/dec CB delay	Update CB delay	RDH	REG	RESERVED	TRTP	RES	TCL	B8	DQS gating offset
0	0	0	0	0	*	0	*	*	0
rw	rw	rw	rw	r	rw	r	rw	rw	rw

31: 28 Set to '1' to increment checkbits byte delay, set to '0' to decrement delay

27: 24 Set to '1' to update checkbits byte delay

23: 22 Read delay high bits, setting this field to N adds 4 x N read delay cycles

21 Registered memory (1 cycle extra latency on control signals)

20: 14 Reserved

13 SDRAM read-to-precharge timing, tRTP will be equal to field value + 2 DDR-clock cycles.

12: 11 Reserved

10: 9 SDRAM CAS latency timing. CL will be equal to field value + 3 DDR-clock cycles.
Note: You must reprogram the memory's MR register after changing this value

8 Enables address generation for DDR2 chips with eight banks

1=addressess generation for eight banks 0=address generation for four banks

7: 0 Number of half clock cycles for which the DQS input signal will be active after a read command is given. After this time the DQS signal will be gated off to prevent latching of faulty data. Only valid if the dqsgating generic is enabled.

22.4.5 DDR2 SDRAM Configuration Register 5

Table 221. 0x10 - DDR2CFG5 - DDR2 SDRAM configuration register 5

31	30 28	27 26	25 18	17 16	15	14 11	10 8	7 5	4 0
R	TRP	RES	TRFC	ODT	DS	RESERVED	TRCD	RESERVED	TRAS
0	*	0	0	0	0	0	*	0	0
r	rw	r	rw	rw	rw	r	rw	r	rw

31	Reserved
30: 28	SDRAM tRP timing. tRP will be equal to 2 + field value DDR-clock cycles
27: 26	Reserved
25: 18	SDRAM tRFC timing. tRFC will be equal to 3 + field-value DDR-clock cycles.
17: 16	SDRAM-side on-die termination setting (0=disabled, 1-3=75/150/50 ohm) Note: You must reprogram the EMR1 register after changing this value.
15	SDRAM-side output drive strength control (0=full strength, 1=half strength) Note: You must reprogram the EMR1 register after changing this value
14: 11	Reserved
10: 8	SDRAM RAS-to-CAS delay (TRCD). tRCD will be equal to field value + 2 DDR-clock cycles
7: 5	Reserved
4: 0	SDRAM RAS to precharge timing. TRAS will be equal to 2+ field value DDR-clock cycles

22.4.6 DDR2 FT Configuration Register

Table 222. 0x20 - DDR2FTCFG - DDR2 FT configuration register

31 20	19	18 16	15 8	7 5	4	3	2	1	0
Diag data read error location	DDERR	DM	RESERVED	DATAMUX	CEM	BAUPD	BAEN	CODE	EDEN
0	0	0	0	0	0	0	0	0	0
r	r	rw	r	rw	rw	rw	rw	rw	rw

31: 20	Bit field describing location of corrected errors for last diagnostic data read (read-only) One bit per byte lane in 64+32-bit configuration
19	Set high if last diagnostic data read contained an uncorrectable error (read-only)
18: 16	Data width, read-only field. 001=16+8, 010=32+16, 011=64+32 bits
15: 8	Reserved
7: 5	Data mux control, setting this nonzero switches in the upper checkbit half with another data lane. For 64-bit interface 000 = no switching 001 = Data bits 15:0, 010 = Data bits 31:16, 011: Data bits 47:32, 100: Data bits 63:48, 101 = Checkbits 79:64, 110,111 = Undefined
4	If set high, the correctable error signal is masked out.
3	Enable automatic boundary shifting on write
2	Enable the code boundary
1	Code selection, 0=Code A (64+32/32+16/16+8), 1=Code B (64+16/32+8)
0	EDAC Enable

22.4.7 DDR2 FT Diagnostic Address

*Table 223.*0x24 - DDR2FTDA - DDR2 FT Diagnostic Address

31 … 2	1 … 0
MEMORY ADDRESS	RESERVED
0	0
rw	r

31: 3 Address to memory location for checkbit read/write, 64/32-bit aligned for checkbits/data

1: 0 Reserved (address bits always 0 due to alignment)

22.4.8 DDR2 FT Diagnostic Checkbits

Table 224. 0x28 - DDR2FTDC - DDR2 FT Diagnostic Checkbits

31 … 24	23 … 16	15 … 8	7 … 0
CHECKBITS D	CHECKBITS C	CHECKBITS B	CHECKBITS A
*	*	*	0
rw	rw	rw	rw

31: 24 Checkbits for part D of 64-bit data word (undefined for code B)

23: 16 Checkbits for part C of 64-bit data word (undefined for code B)

15: 8 Checkbits for part B of 64-bit data word

7: 0 Checkbits for part A of 64-it data word.

22.4.9 DDR2 FT Diagnostic Data

Table 225. 0x2C - DDR2FTDD - DDR2 FT Diagnostic Data

31 … 0
DATA BITS
*
r

31: 0 Uncorrected data bits for 32-bit address set in DDR2FTDA

22.4.10 DDR2 FT Boundary Address Register

Table 226. 0x30 - DDR2FTBND - DDR2 FT Boundary Address Register

31 … 3	2 … 0
CHECKBIT CODE BOUNDARY ADDRESS	R
0	0
rw	r

31: 3 Code boundary address, 64-bit aligned

2: 0 Zero due to alignment

22.5 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x02E. The revision decribed in this document is revision 1. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

22.6 Configuration options

Table 227 shows the configuration options of the core (VHDL generics).

*Table 227.*Configuration options

Generic	Function	Allowed range	Default
fabtech	PHY technology selection	virtex4, virtex5, stratix3	virtex4
memtech	Technology selection for DDR FIFOs	inferred, virtex2, virtex4, spartan3e, altera	inferred
hindex	AHB slave index	0 - NAHBSLV-1	0
haddr	ADDR field of the AHB BAR0 defining SDRAM area. Default is 0xF0000000 - 0xFFFFFFFF.	0 - 16#FFF#	16#000#
hmask	MASK field of the AHB BAR0 defining SDRAM area.	0 - 16#FFF#	16#F00#
ioaddr	ADDR field of the AHB BAR1 defining I/O address space where DDR control register is mapped.	0 - 16#FFF#	16#000#
iomask	MASK field of the AHB BAR1 defining I/O address space	0 - 16#FFF#	16#FFF#
ddrbits	Data bus width of external DDR memory	16, 32, 64	16
MHz	DDR clock input frequency in MHz.	10 - 200	100
clkmul, clkdiv	The DDR input clock is multiplied with the clkmul generic and divided with clkdiv to create the final DDR clock	2 - 32	2
rstdel	Clock reset delay in micro-seconds.	1 - 1023	200
col	Default number of column address bits	9 - 12	9
Mbyte	Default memory chip select bank size in Mbyte	8 - 1024	16
pwron	Enable SDRAM at power-on initialization	0 - 1	0
oepol	Polarity of bdrive and vbdrive signals. 0=active low, 1=active high	0 - 1	0
ahbfreq	Frequency in MHz of the AHB clock domain	1 - 1023	50
readdly	Additional read latency cycles (used to increase calibration range)	0-3	1
TRFC	Reset value for the tRFC timing parameter in ns.	75-155	130
ddelayb0*	Input data delay for bit[7:0]	0-63	0
ddelayb1*	Input data delay for bit[15:8]	0-63	0
ddelayb2*	Input data delay for bit[23:16]	0-63	0
ddelayb3*	Input data delay for bit[31:24]	0-63	0
ddelayb4*	Input data delay for bit[39:32]	0-63	0
ddelayb5*	Input data delay for bit[47:40]	0-63	0
ddelayb6*	Input data delay for bit[55:48]	0-63	0
ddelayb7*	Input data delay for bit[63:56]	0-63	0
cbdelayb0*	Input data delay for checkbit[7:0]	0-63	0
cbdelayb1*	Input data delay for checkbit[15:8]	0-63	0
cbdelayb2*	Input data delay for checkbit[23:16]	0-63	0
cbdelayb3*	Input data delay for checkbit[31:24]	0-63	0
numidelctrl*	Number of IDELAYCTRL the core will instantiate	-	4
norefclk*	Set to 1 if no 200 MHz reference clock is connected to clkref200 input.	0-1	0
odten	Enable odt: 0 = Disabled, 1 = 75Ohm, 2 =150Ohm, 3 = 50Ohm	0-3	0

*Table 227.*Configuration options

Generic	Function	Allowed range	Default
rskew**	Set the phase relationship between the DDR controller clock and the input data sampling clock. Sets the phase in ps.	0 - 9999	0
octen**	Enable on chip termination: 1 = enabled, 0 = disabled	0 - 1	0
dqsgating***	Enable gating of DQS signals when doing reads. 1 = enable, 0 = disable	0 - 1	0
nosync	Disable insertion of synchronization registers between AHB clock domain and DDR clock domain. This can be done if the AHB clock's rising edges always are in phase with a rising edge on the DDR clock. If this generic is set to 1 the clkmul and clkdiv generics should be equal. Otherwise the DDR controller may scale the incoming clock and loose the clocks' edge alignment in the process.	0 - 1	0
eightbanks	Enables address generation for DDR2 chips with eight banks. The DDR_BA is extended to 3 bits if set to 1.	0 - 1	0
dqsse	Single-ended DQS. The value of this generic is written to bit 10 in the memory's Extended Mode register. If this bit is 1 DQS is used in a single-ended mode. Currently this bit should only, and must be, set to 1 when the Stratix2 DDR2 PHY is used. This is the only PHY that supports single ended DQS without modification.	0 - 1	0
burstlen	DDR access burst length in 32-bit words	8,16,32,..,256	8
ahbbits	AHB bus width	32,64,128,256	AHBDW
ft	Enable fault-tolerant version	0 - 1	0
ftbits	Extra DDR data bits used for checkbits	0,8,16,32	0
bigmem	Big memory support, changes the range of supported total memory bank sizes from 8MB-1GB to 32MB-4GB	0 - 1	0
raspipe	Enables an extra pipeline stage in the address decoding to improve timing at the cost of one DDR-cycle latency	0 - 1	0
* only available in Virtex4/5 implementation. ** only available in Altera and Spartan3 implementations. *** only available on Nextreme/eASIC implementations			

22.7 Implementation

22.7.1 Technology mapping

The core has two technology mapping VHDL generics: *memtech* and *fabtech*. The VHDL generic *memtech* controls the technology used for memory cell implementation. The VHDL generic *fabtech* controls the technology used in the PHY implementation. See the GRLIB Users's Manual for available settings.

22.7.2 FPGA support

Complete PHY:s for a number of FPGA technologies are included in the distribution, see table below. Unless otherwise noted these have been only functionally tested on evaluation board in lab environment and detailed timing analysis has not been performed. Note also that some of the FPGA phy:s use simplified sampling approaches which may require the memory timing to be better than the JEDEC standard specifies.

Scripts for post-layout static timing analysis are not included. Because these PHY:s are based on dedicated hard macros with fixed placement in the FPGA:s pad structure, just a minimal set of constraints are normally neccessary for synthesis purposes.

Some PHY:s support instantiation without built-in pads, to separate the pads from the PHY the internal ddr2spax entity and the phy must be instantiated manually.

*Table 228.*FPGA DDR2 PHYs included in GRLIB

Technology	fabtech	Read clock method	Built-in pads
Stratix 2	stratix2	Tech intrinsics (DQS based)	Yes
Stratix 3	stratix3	Tunable static shift	Yes
Spartan 3	spartan3	Clock feedback loop + static shift	Yes
Virtex4,5,6	virtex4, virtex5, virtex6	Fixed clock, DQ shifted using IDELAY	Yes or No
Spartan6	spartan6	Fixed clock, DQ shifted using IDELAY	Yes or No

22.7.3 RAM usage

The FIFOs in the core are implemented with the *syncram_2p* (with separate clock for each port) component found in the technology mapping library (TECHMAP). The number of RAMs used for the FIFO implementation depends om the DDR data width, set by the *ddrbits* VHDL generic, and the AHB bus width in the system.

The RAM block usage is tabulated below for the default burst length of 8 words. If the burst length is doubled, the depths for all the RAMs double as well but the count and width remain the same.

*Table 229.*Block-RAM usage for default burst length

DDR width	AHB width	Write FIFO block-RAM usage			Read-FIFO block-RAM usage			Total RAM count
		Count	Depth	Width	Count	Depth	Width	
16	32	1	16	32	1	8	32	2
16	64	2	8	32	2	4	32	4
16	128	4	4	32	4	2	32	8
16	256	8	2	32	8	1	32	16
32	32	2	8	32	1	4	64	3
32	64	2	8	32	1	4	64	3
32	128	4	4	32	2	2	64	6
32	256	8	2	32	4	1	64	12
64	32	4	4	32	1	2	128	5
64	64	4	4	32	1	2	128	5
64	128	4	4	32	1	2	128	5
64	256	8	2	32	2	1	128	10

22.7.4 Xilinx Virtex-specific issues

The Xilinx tools require one IDELAYCTRL macro to be instantiated in every region where the IDELAY feature is used. Since the DDR2 PHY uses the IDELAY on every data (DQ) pin, this affects the DDR2 core. For this purpose, the core has a numidelctrl generic, controlling how many IDELAYCTRL's get instantiated in the PHY.

The tools allow for two ways to do this instantiation:

- Instantiate the same number of IDELAYCTRL as the number of clock regions containing DQ pins and place the instances manually using UCF LOC constraints.
- Instantiate just one IDELAYCTRL, which the ISE tools will then replicate over all regions.

The second solution is the simplest, since you just need to set the numidelctrl to 1 and no extra constraints are needed. However, this approach will not work if IDELAY is used anywhere else in the FPGA design.

For more information on IDELAYCTRL, see Xilinx Virtex4/5 User's Guide.

22.7.5 Design tools

To run the design in Altera Quartus 7.2 you have to uncomment the lines in the .qsf file that assigns the MEMORY_INTERFACE_DATA_PIN_GROUP for the DDR2 interface. These group assignments result in error when Altera Quartus 8.0 is used.

22.8 Signal descriptions

Table 230 shows the interface signals of the core (VHDL ports).

*Table 230.*Signal descriptions

Signal name	Type	Function	Active
RST_DDR	Input	Reset input for the DDR PHY	Low
RST_AHB	Input	Reset input for AHB clock domain	Low
CLK_DDR	Input	DDR input Clock	-
CLK_AHB	Input	AHB clock	-
CLKREF200	Input	200 MHz reference clock	-
LOCK	Output	DDR clock generator locked	High
CLKDDRO		Internal DDR clock output after clock multiplication	
CLKDDRI		Clock input for the internal DDR clock domain. Must be connected to CLKDDRO.	
AHBSI	Input	AHB slave input signals	-
AHBSO	Output	AHB slave output signals	-
DDR_CLK[2:0]	Output	DDR memory clocks (positive)	High
DDR_CLKB[2:0]	Output	DDR memory clocks (negative)	Low
DDR_CLK_FB_OUT	Output	DDR data synchronization clock, connect this to a signal path with equal length of the DDR_CLK trace + DDR_DQS trace	-
DDR_CLK_FB	Input	DDR data synchronization clock, connect this to the other end of the signal path connected to DDR_-CLK_FB_OUT	-
DDR_CKE[1:0]	Output	DDR memory clock enable	High
DDR_CSB[1:0]	Output	DDR memory chip select	Low
DDR_WEB	Output	DDR memory write enable	Low
DDR_RASB	Output	DDR memory row address strobe	Low
DDR_CASB	Output	DDR memory column address strobe	Low
DDR_DM[(DDRBITS+FTBITS)/8-1:0]	Output	DDR memory data mask	Low
DDR_DQS[(DDRBITS+FTBITS)/8-1:0]	Bidir	DDR memory data strobe	Low
DDR_DQSN[(DDRBITS+FTBITS)/8-1:0]	Bidir	DDR memory data strobe (inverted)	High
DDR_AD[13:0]	Output	DDR memory address bus	Low
DDR_BA[2 or 1:0] 3)	Output	DDR memory bank address	Low
DDR_DQ[DDRBITS+FTBITS-1:0]	BiDir	DDR memory data bus	-
DDR_ODT[1:0]	Output	DDR memory odt	Low

1) see GRLIB IP Library User's Manual
2) Polarity selected with the oepol generic
3) DDR_BA[2:0] if the eightbanks generic is set to 1 else DDR_BA[1:0]
4) Only used on Virtex4/5
5) Only used on Spartan3

22.9 Library dependencies

Table 231 shows libraries used when instantiating the core (VHDL libraries).

*Table 231.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AHB signal definitions
GAISLER	MEMCTRL	Signals, component	Memory bus signals definitions, component declaration

22.10 Component declaration

```
component ddr2spa
  generic (
    fabtech : integer := 0;
    memtech : integer := 0;
    hindex  : integer := 0;
    haddr   : integer := 0;
    hmask   : integer := 16#f00#;
    ioaddr  : integer := 16#000#;
    iomask  : integer := 16#fff#;
    MHz     : integer := 100;
    clkmul  : integer := 2;
    clkdiv  : integer := 2;
    col     : integer := 9;
    Mbyte   : integer := 16;
    rstdel  : integer := 200;
    pwron   : integer := 0;
    oepol   : integer := 0;
    ddrbits : integer := 16;
    ahbfreq : integer := 50;
    readdly : integer := 1;
    ddelayb0: integer := 0;
    ddelayb1: integer := 0;
    ddelayb2: integer := 0;
    ddelayb3: integer := 0;
    ddelayb4: integer := 0;
    ddelayb5: integer := 0;
    ddelayb6: integer := 0;
    ddelayb7: integer := 0
  );
  port (
    rst_ddr    : in  std_ulogic;
    rst_ahb    : in  std_ulogic;
    clk_ddr    : in  std_ulogic;
    clk_ahb    : in  std_ulogic;
    clkref200 : in std_ulogic;
    lock       : out std_ulogic;-- DCM locked
    clkddro    : out std_ulogic;-- DCM locked
    clkddri    : in  std_ulogic;
    ahbsi      : in  ahb_slv_in_type;
    ahbso      : out ahb_slv_out_type;
    ddr_clk    : out std_logic_vector(2 downto 0);
    ddr_clkb   : out std_logic_vector(2 downto 0);
    ddr_cke    : out std_logic_vector(1 downto 0);
    ddr_csb    : out std_logic_vector(1 downto 0);
    ddr_web    : out std_ulogic;                       -- ddr write enable
    ddr_rasb   : out std_ulogic;                       -- ddr ras
    ddr_casb   : out std_ulogic;                       -- ddr cas
    ddr_dm     : out std_logic_vector (ddrbits/8-1 downto 0);    -- ddr dm
    ddr_dqs    : inout std_logic_vector (ddrbits/8-1 downto 0);    -- ddr dqs
    ddr_dqsn   : inout std_logic_vector (ddrbits/8-1 downto 0);    -- ddr dqs
    ddr_ad     : out std_logic_vector (13 downto 0);   -- ddr address
    ddr_ba     : out std_logic_vector (1 downto 0);    -- ddr bank address
    ddr_dq     : inout  std_logic_vector (ddrbits-1 downto 0); -- ddr data
    ddr_odt    : out std_logic_vector(1 downto 0) -- odt
  );
  end component;
```

22.11 Instantiation

This example shows how the core can be instantiated.

The DDR SDRAM controller decodes SDRAM area at 0x40000000 - 0x7FFFFFFF. The DDR2 SDRAM registers are mapped into AHB I/O space on address (AHB I/O base address + 0x100).

```
library ieee;
use ieee.std_logic_1164.all;
library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.memctrl.all;

entity ddr_Interface is
  port (
    ddr_clk  : out std_logic_vector(2 downto 0);
    ddr_clkb : out std_logic_vector(2 downto 0);
    ddr_cke  : out std_logic_vector(1 downto 0);
    ddr_csb  : out std_logic_vector(1 downto 0);
    ddr_web  : out std_ulogic;                        -- ddr write enable
    ddr_rasb : out std_ulogic;                        -- ddr ras
    ddr_casb : out std_ulogic;                        -- ddr cas
    ddr_dm   : out std_logic_vector (7 downto 0);     -- ddr dm
    ddr_dqs  : inout std_logic_vector (7 downto 0);     -- ddr dqs
    ddr_dqsn : inout std_logic_vector (7 downto 0);     -- ddr dqsn
    ddr_ad   : out std_logic_vector (13 downto 0);    -- ddr address
    ddr_ba   : out std_logic_vector (1 downto 0);     -- ddr bank address
    ddr_dq   : inout std_logic_vector (63 downto 0); -- ddr data
    ddr_odt  : out std_logic_vector (1 downto 0) -- ddr odt
);
end;

architecture rtl of mctrl_ex is

  -- AMBA bus
signal ahbsi : ahb_slv_in_type;
signal ahbso : ahb_slv_out_vector := (others => ahbs_none);
signal clkml, lock, clk_200,
signal clk_200 : std_ulogic; -- 200 MHz reference clock
signal ddrclkin, ahbclk : std_ulogic; -- DDR input clock and AMBA sys clock
signal rstn  : std_ulogic; -- Synchronous reset signal
signal reset : std_ulogic; -- Asynchronous reset signal


begin

-- DDR controller


ddrc : ddr2spa generic map ( fabtech => virtex4, ddrbits => 64, memtech => memtech,
hindex => 4, haddr => 16#400#, hmask => 16#F00#, ioaddr => 1,
pwron => 1, MHz => 100, col => 9, Mbyte => 32, ahbfreq => 50, ddrbits => 64,
readdly => 1, ddelayb0 => 0, ddelayb1 => 0, ddelayb2 => 0, ddelayb3 => 0,
ddelayb4 => 0, ddelayb5 => 0, ddelayb6 => 0, ddelayb7 => 0)
port map (
reset, rstn, ddrclkin, ahbclk, clk_200, lock, clkml, clkml,  ahbsi, ahbso(4),
ddr_clk, ddr_clkb,
ddr_cke, ddr_csb, ddr_web, ddr_rasb, ddr_casb,
ddr_dm, ddr_dqs, ddr_adl, ddr_ba, ddr_dq, ddr_odt);
```

23 DIV32 - Signed/unsigned 64/32 divider module

23.1 Overview

The divider module performs signed/unsigned 64-bit by 32-bit division. It implements the radix-2 non-restoring iterative division algorithm. The division operation takes 36 clock cycles. The divider leaves no remainder. The result is rounded towards zero. Negative result, zero result and overflow (according to the overflow detection method B of SPARC V8 Architecture manual) are detected.

23.2 Operation

The division is started when '1' is samples on DIVI.START on positive clock edge. Operands are latched externally and provided on inputs DIVI.Y, DIVI.OP1 and DIVI.OP2 during the whole operation. The result appears on the outputs during the clock cycle following the clock cycle after the DIVO.READY was asserted. Asserting the HOLD input at any time will freeze the operation, until HOLDN is de-asserted.

23.3 Implementation

23.3.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core will use asynchronous reset for all registers if the GRLIB config package setting *grlib_async_reset_enable* is set.

23.4 Configurations options

Core has only one VHDL generic, scantest, that should be set to 1 if GRLIB has been configured to use asynchronous reset.

23.5 Signal descriptions

Table 232 shows the interface signals of the core (VHDL ports).

*Table 232.*Signal declarations

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
HOLDN	N/A	Input	Hold	Low
DIVI	Y[32:0]	Input	Dividend - MSB part Y[32] - Sign bit Y[31:0] - Dividend MSB part in 2's complement format	High
	OP1[32:0]		Dividend - LSB part OP1[32] - Sign bit OP1[31:0] - Dividend LSB part in 2's complement format	High
	FLUSH		Flush current operation	High
	SIGNED		Signed division	High
	START		Start division	High
DIVO	READY	Output	The result is available one clock after the ready signal is asserted.	High
	NREADY		The result is available three clock cycles, assuming hold=HIGH, after the nready signal is asserted.	High
	ICC[3:0]		Condition codes ICC[3] - Negative result ICC[2] - Zero result ICC[1] - Overflow ICC[0] - Not used. Always '0'.	High
	RESULT[31:0]		Result	High
TESTEN	N/A	Input	Test enable (only used together with async. reset)	High
TESTRST	N/A	Input	Test reset (only used together with async. reset)	Low

23.6 Library dependencies

Table 233 shows libraries used when instantiating the core (VHDL libraries).

*Table 233.*Library dependencies

Library	Package	Imported unit(s)	Description
GAISLER	ARITH	Signals, component	Divider module signals, component declaration

23.7 Component declaration

The core has the following component declaration.

```
component div32
port (
    rst     : in  std_ulogic;
    clk     : in  std_ulogic;
    holdn   : in  std_ulogic;
```

```
    divi    : in  div32_in_type;
    divo    : out div32_out_type
);
end component;
```

23.8 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use gaisler.arith.all;

.
.
.

signal divi  : div32_in_type;
signal divo  : div32_out_type;

begin

div0 : div32 port map (rst, clk, holdn, divi, divo);

end;
```

24 DSU3 - LEON3 Hardware Debug Support Unit

24.1 Overview

To simplify debugging on target hardware, the LEON3 processor implements a debug mode during which the pipeline is idle and the processor is controlled through a special debug interface. The LEON3 Debug Support Unit (DSU) is used to control the processor during debug mode. The DSU acts as an AHB slave and can be accessed by any AHB master. An external debug host can therefore access the DSU through several different interfaces. Such an interface can be a serial UART (RS232), JTAG, PCI, USB or Ethernet. The DSU supports multi-processor systems and can handle up to 16 processors.

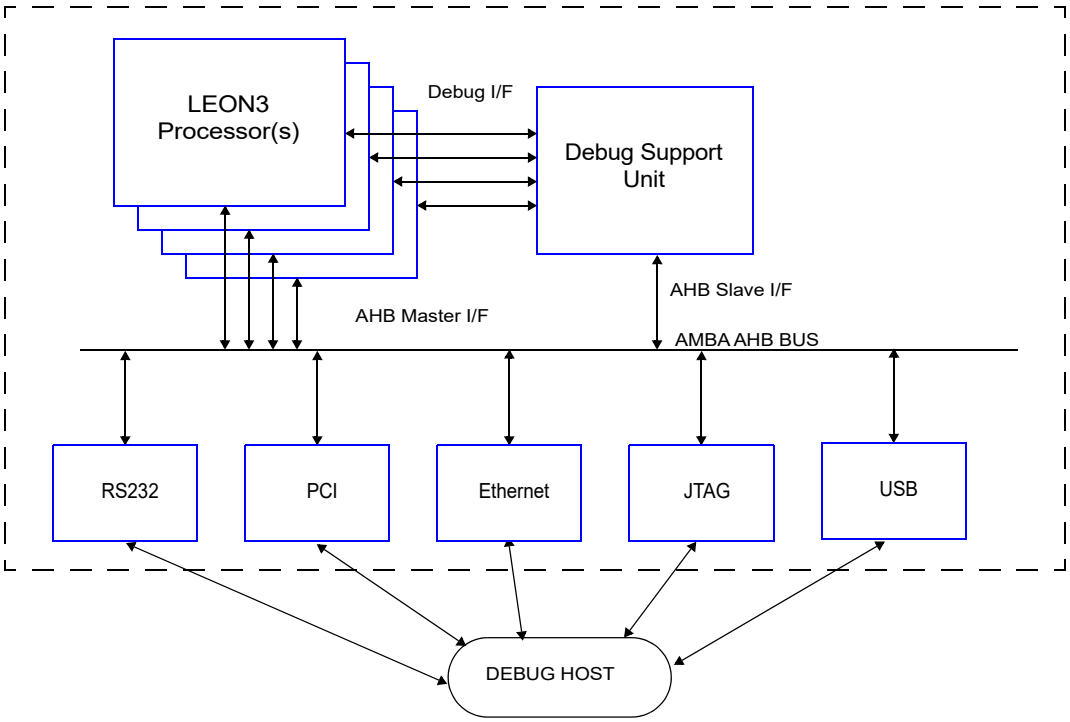


Figure 59. LEON3/DSU Connection

24.2 Operation

Through the DSU AHB slave interface, any AHB master can access the processor registers and the contents of the instruction trace buffer. The DSU control registers can be accessed at any time, while the processor registers and caches can only be accessed when the processor has entered debug mode. In debug mode, the processor pipeline is held and the processor state can be accessed by the DSU. Entering the debug mode can occur on the following events:

- executing a breakpoint instruction (ta 1)
- integer unit hardware breakpoint/watchpoint hit (trap 0xb)
- rising edge of the external break signal (DSUBRE)
- setting the break-now (BN) bit in the DSU control register
- a trap that would cause the processor to enter error mode
- occurrence of any, or a selection of traps as defined in the DSU control register
- after a single-step operation
- one of the processors in a multiprocessor system has entered the debug mode
- DSU AHB breakpoint or watchpoint hit

The debug mode can only be entered when the debug support unit is enabled through an external signal (DSUEN). For DSU break (DSUBRE), and the break-now BN bit, to have effect the Break-on-IU-watchpoint (BW) bit must be set in the DSU control register. This bit is set when DSUBRE is active after reset and should also be set by debug monitor software when initializing the DSU. When the debug mode is entered, the following actions are taken:

- PC and nPC are saved in temporary registers (accessible by the debug unit)
- an output signal (DSUACT) is asserted to indicate the debug state
- the timer unit is (optionally) stopped to freeze the LEON timers and watchdog

The instruction that caused the processor to enter debug mode is not executed, and the processor state is kept unmodified. Execution is resumed by clearing the BN bit in the DSU control register or by de-asserting DSUEN. The timer unit will be re-enabled and execution will continue from the saved PC and nPC. Debug mode can also be entered after the processor has entered error mode, for instance when an application has terminated and halted the processor. The error mode can be reset and the processor restarted at any address.

When a processor is in the debug mode, an access to ASI diagnostic area is forwarded to the IU which performs access with ASI equal to value in the DSU ASI register and address consisting of 20 LSB bits of the original address.

24.3 AHB trace buffer

The AHB trace buffer consists of a circular buffer that stores AHB data transfers, the monitored AHB bus is either the same bus as the DSU AHB slave interface is connected to, or a completely separate bus. The address, data and various control signals of the AHB bus are stored and can be read out for later analysis. The trace buffer is 128, 160 or 224 bits wide, depending on the AHB bus width. The way information stored is indicated in the table below:

*Table 234.*AHB Trace buffer data allocation

Bits	Name	Definition
223:160	Load/Store data	AHB HRDATA/HWDATA(127:64)
159:129	Load/Store data	AHB HRDATA/HWDATA(63:32)
127	AHB breakpoint hit	Set to ‘1’ if a DSU AHB breakpoint hit occurred.
126	-	Not used
125:96	Time tag	DSU time tag counter
95:80	-	Not used
79	Hwrite	AHB HWRITE
78:77	Htrans	AHB HTRANS
76:74	Hsize	AHB HSIZE
73:71	Hburst	AHB HBURST
70:67	Hmaster	AHB HMASTER
66	Hmastlock	AHB HMASTLOCK
65:64	Hresp	AHB HRESP
63:32	Load/Store data	AHB HRDATA/HWDATA(31:0)
31:0	Load/Store address	AHB HADDR

In addition to the AHB signals, the DSU time tag counter is also stored in the trace.

The trace buffer is enabled by setting the enable bit (EN) in the trace control register. Each AHB transfer is then stored in the buffer in a circular manner. The address to which the next transfer is written is held in the trace buffer index register, and is automatically incremented after each transfer. Trac-

ing is stopped when the EN bit is reset, or when a AHB breakpoint is hit. Tracing is temporarily suspended when the processor enters debug mode, unless the trace force bit (TF) in the trace control register is set. If the trace force bit is set, the trace buffer is activated as long as the enable bit is set. The force bit is reset if an AHB breakpoint is hit and can also be cleared by software. Note that neither the trace buffer memory nor the breakpoint registers (see below) can be read/written by software when the trace buffer is enabled.

The DSU has an internal time tag counter and this counter is frozen when the processor enters debug mode. When AHB tracing is performed in debug mode (using the trace force bit) it may be desirable to also enable the time tag counter. This can be done using the timer enable bit (TE). Note that the time tag is also used for the instruction trace buffer and the timer enable bit should only be set when using the DSU as an AHB trace buffer only, and not when performing profiling or software debugging. The timer enable bit is reset on the same events as the trace force bit.

24.3.1 AHB trace buffer filters

The DSU can be implemented with filters that can be applied to the AHB trace buffer, breakpoints and watchpoints. If implemented, these filters are controlled via the AHB trace buffer filter control and AHB trace buffer filter mask registers. The fields in these registers allows masking access characteristics such as master, slave, read, write and address range so that accesses that correspond to the specified mask are not written into the trace buffer. Address range masking is done using the second AHB breakpoint register set. The values of the LD and ST fields of this register has no effect on filtering.

24.3.2 AHB statistics

The DSU can be implemented to generate statistics from the traced AHB bus. When statistics collection is enabled the DSU will assert outputs that are suitable to connect to a LEON3 statistics unit (L3STAT). The statistical outputs can be filtered by the AHB trace buffer filters, this is controlled by the Performance counter Filter bit (PF) in the AHB trace buffer filter control register. The DSU can collect data for the events listed in table 235 below.

*Table 235.*AHB events

Event	Description	Note
idle	HTRANS=IDLE	Active when HTRANS IDLE is driven on the AHB slave inputs and slave has asserted HREADY.
busy	HTRANS=BUSY	Active when HTRANS BUSY is driven on the AHB slave inputs and slave has asserted HREADY.
nseq	HTRANS=NONSEQ	Active when HTRANS NONSEQ is driven on the AHB slave inputs and slave has asserted HREADY.
seq	HTRANS=SEQ	Active when HTRANS SEQUENTIAL is driven on the AHB slave inputs and slave has asserted HREADY.
read	Read access	Active when HTRANS is SEQUENTIAL or NON-SEQUENTIAL, slave has asserted HREADY and the HWRITE input is low.
write	Write access	Active when HTRANS is SEQUENTIAL or NON-SEQUENTIAL, slave has asserted HREADY and the HWRITE input is high.
hsize[5:0]	Transfer size	Active when HTRANS is SEQUENTIAL or NON-SEQUENTIAL, slave has asserted HREADY and HSIZE is BYTE (hsize[0]), HWORD (HSIZE[1]), WORD (hsize[2]), DWORD (hsize[3]), 4WORD hsize[4], or 8WORD (hsize[5]).
ws	Wait state	Active when HREADY input to AHB slaves is low and AMBA response is OKAY.
retry	RETRY response	Active when master receives RETRY response
split	SPLIT response	Active when master receives SPLIT response

*Table 235.*AHB events

Event	Description	Note
spdel	SPLIT delay	Active during the time a master waits to be granted access to the bus after reception of a SPLIT response. The core will only keep track of one master at a time. This means that when a SPLIT response is detected, the core will save the master index. This event will then be active until the same master is re-allowed into bus arbitration and is granted access to the bus. This also means that the delay measured will include the time for re-arbitration, delays from other ongoing transfers and delays resulting from other masters being granted access to the bus before the SPLIT:ed master is granted again after receiving SPLIT complete. If another master receives a SPLIT response while this event is active, the SPLIT delay for the second master will not be measured.
locked	Locked access	Active while the HMASTLOCK signal is asserted on the AHB slave inputs.

24.4 Instruction trace buffer

The instruction trace buffer consists of a circular buffer that stores executed instructions. The instruction trace buffer is located in the processor, and read out via the DSU. The trace buffer is 128 bits wide, the information stored is indicated in the table below:

*Table 236.*Instruction trace buffer data allocation

Bits	Name	Definition
127	-	Unused
126	Multi-cycle instruction	Set to '1' on the second and third instance of a multi-cycle instruction (LDD, ST or FPOP)
125:96	Time tag	The value of the DSU time tag counter
95:64	Load/Store parameters	Instruction result, Store address or Store data
63:34	Program counter	Program counter (2 lsb bits removed since they are always zero)
33	Instruction trap	Set to '1' if traced instruction trapped
32	Processor error mode	Set to '1' if the traced instruction caused processor error mode
31:0	Opcode	Instruction opcode

During tracing, one instruction is stored per line in the trace buffer with the exception of multi-cycle instructions. Multi-cycle instructions are entered two or three times in the trace buffer. For store instructions, bits [95:64] correspond to the store address on the first entry and to the stored data on the second entry (and third in case of STD). Bit 126 is set on the second and third entry to indicate this. A double load (LDD) is entered twice in the trace buffer, with bits [95:64] containing the loaded data. Bit 126 is set for the second entry.

When the processor enters debug mode, tracing is suspended. The trace buffer and the trace buffer control register can be read and written while the processor is in the debug mode. During the instruction tracing (processor in normal mode) the trace buffer and trace buffer control register 0 can not be written. If the two-port trace buffer is enabled (refer to the *tbuf* generic in section 80.16), then the trace buffer can be read contextually to the instruction tracing (processor in normal mode). The traced instructions can optionally be filtered on instruction types. Which instructions are traced is defined in the instruction trace register [31:28], as defined in the table below:

*Table 237.*Trace filter operation

Trace filter	Instructions traced
0x0	All instructions
0x1	SPARC Fomat 2 instructions
0x2	Control-flow changes. All Call, branch and trap instructions including branch targets
0x4	SPARC Format 1 instructions (CALL)
0x8	SPARC Format 3 instructions except LOAD or STORE
0xC	SPARC Format 3 LOAD or STORE instructions
0xD	SPARC Format 3 LOAD or STORE instructions to alternate space
0xE	SPARC Format 3 LOAD or STORE instructions to alternate space 0x80 - 0xFF with ASI last digit base filtering

It is also possible to filter traced instructions based on the program counter value. This option is combined with the filtering option if an additional filtering mechanism is activated from Table 237. Refer to section 24.6.13 for detailed information.

24.5 DSU memory map

The DSU memory map can be seen in table 238 below. In a multiprocessor systems, the register map is duplicated and address bits 27 - 24 are used to index the processor.

Note: The DSU memory interface is intended to be accessed by a debug monitor. Software running on the LEON processors should not access the DSU interface. Registers, such as ASR registers, may not have all fields available via the DSU interface

*Table 238.*DSU memory map

Address offset	Register
0x000000	DSU control register
0x000008	Time tag counter
0x000020	Break and Single Step register
0x000024	Debug Mode Mask register
0x000040	AHB trace buffer control register
0x000044	AHB trace buffer index register
0x000048	AHB trace buffer filter control register
0x00004c	AHB trace buffer filter mask register
0x000050	AHB breakpoint address 1
0x000054	AHB mask register 1
0x000058	AHB breakpoint address 2
0x00005c	AHB mask register 2
0x100000 - 0x10FFFF	Instruction trace buffer (..0: Trace bits 127 - 96, ..4: Trace bits 95 - 64, ..8: Trace bits 63 - 32, ..C : Trace bits 31 - 0)
0x110000	Instruction Trace buffer control register 0
0x110004	Instruction Trace buffer control register 1
0x200000 - 0x210000	AHB trace buffer (..0: Trace bits 127 - 96, ..4: Trace bits 95 - 64, ..8: Trace bits 63 - 32, ..C : Trace bits 31 - 0)
0x300000 - 0x3007FC	IU register file, port1 (%asr16.dpsel = 0) IU register file, port 2 (%asr16.dpsel = 1)
0x300800 - 0x300FFC	IU register file check bits (LEON3FT only)

*Table 238.*DSU memory map

Address offset	Register
0x301000 - 0x30107C	FPU register file
0x301800 - 0x30187C	FPU register file check bits (LEON3FT only)
0x400000 - 0x4FFFFC	IU special purpose registers
0x400000	Y register
0x400004	PSR register
0x400008	WIM register
0x40000C	TBR register
0x400010	PC register
0x400014	NPC register
0x400018	FSR register
0x40001C	CPSR register
0x400020	DSU trap register
0x400024	DSU ASI register
0x400040 - 0x40007C	ASR16 - ASR31 (when implemented)
0x700000 - 0x7FFFFC	ASI diagnostic access (ASI = value in DSU ASI register, address = address[19:0]) ASI = 0x9 : Local instruction RAM, ASI = 0xB : Local data RAM ASI = 0xC : Instruction cache tags, ASI = 0xD : Instruction cache data ASI = 0xE : Data cache tags, ASI = 0xF : Data cache data ASI = 0x1E : Separate snoop tags

The addresses of the IU registers depends on how many register windows has been implemented:

- %o*n* : 0x300000 + (((psr.cwp * 64) + 32 + *n**4) mod (NWINDOWS*64))
- %l*n* : 0x300000 + (((psr.cwp * 64) + 64 + *n**4) mod (NWINDOWS*64))
- %i*n* : 0x300000 + (((psr.cwp * 64) + 96 + *n**4) mod (NWINDOWS*64))
- %g*n* : 0x300000 + (NWINDOWS*64) + n*4
- %f*n* : 0x301000 + *n**4

24.6 DSU registers

24.6.1 DSU control register

The DSU is controlled by the DSU control register:

*Table 239.*0x000000 - CTRL - DSU control register

31	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PW	HL	PE	EB	EE	DM	BZ	BX	BS	BW	BE	TE
0		0	0	0	*	*		*	*	*	*	*	*
r		r	rw	rw	r	r	r	rw	rw	rw	rw	rw	rw

31: 12 Reserved

11 Power down (PW) - Returns ‘1’ when processor is in power-down mode.

10 Processor halt (HL) - Returns ‘1’ on read when processor is halted. If the processor is in debug mode, setting this bit will put the processor in halt mode.

9 Processor error mode (PE) - returns ‘1’ on read when processor is in error mode, else ‘0’. If written with ‘1’, it will clear the error and halt mode.

8 External Break (EB) - Value of the external DSUBRE signal (read-only)

7 External Enable (EE) - Value of the external DSUEN signal (read-only)

6 Debug mode (DM) - Indicates when the processor has entered debug mode (read-only).

5 Break on error traps (BZ) - if set, will force the processor into debug mode on all *except* the following traps: priviledged_instruction, fpu_disabled, window_overflow, window_underflow, asynchronous_interrupt, ticc_trap.

*Table 239.*0x000000 - CTRL - DSU control register

4	Break on trap (BX) - if set, will force the processor into debug mode when any trap occurs.
3	Break on S/W breakpoint (BS) - if set, debug mode will be forced when an breakpoint instruction (ta 1) is executed.
2	Break on IU watchpoint (BW) - if set, debug mode will be forced on a IU watchpoint (trap 0xb).
1	Break on error (BE) - if set, will force the processor to debug mode when the processor would have entered error condition (trap in trap).
0	Trace enable (TE) - Enables instruction tracing. If set the instructions will be stored in the trace buffer. Remains set when then processor enters debug or error mode

24.6.2 DSU Break and Single Step register

This register is used to break or single step the processor(s). This register controls all processors in a multi-processor system, and is only accessible in the DSU memory map of processor 0.

*Table 240.*0x000020 - BRSS - BRSS - DSU Break and Single Step register

31 16	15 0
SS[15:0]	BN[15:0]

31: 16	Single step (SSx) - if set, the processor x will execute one instruction and return to debug mode. The bit remains set after the processor goes into the debug mode. As an exception, if the instruction is a branch with the annul bit set, and if the delay instruction is effectively annulled, the processor will execute the branch, the annulled delay instruction and the instruction thereafter before returning to debug mode.
15: 0	Break now (BNx) -Force processor x into debug mode if the Break on watchpoint (BW) bit in the processors DSU control register is set. If cleared, the processor x will resume execution.

24.6.3 DSU Debug Mode Mask Register

When one of the processors in a multiprocessor LEON3 system enters the debug mode the value of the DSU Debug Mode Mask register determines if the other processors are forced in the debug mode. This register controls all processors in a multi-processor system, and is only accessible in the DSU memory map of processor 0.

*Table 241.*0x000024 - DBGM - DSU Debug Mode Mask register

31 16	15 0
DM[15:0]	ED[15:0]

31: 16	Debug mode mask (DMx) - If set, the corresponding processor will not be able to force running processors into debug mode even if it enters debug mode.
15: 0	Enter debug mode (EDx) - Force processor x into debug mode if any of processors in a multiprocessor system enters the debug mode. If 0, the processor x will not enter the debug mode.

24.6.4 DSU trap register

The DSU trap register is a read-only register that indicates which SPARC trap type that caused the processor to enter debug mode. When debug mode is force by setting the BN bit in the DSU control register, the trap type will be 0xb (hardware watchpoint trap).

*Table 242.*0x400020 - DTR - DSU Trap register

31 13	12	11 4	3 0
RESERVED	EM	TRAPTYPE	R

31: 13 RESERVED

12 Error mode (EM) - Set if the trap would have cause the processor to enter error mode.

11: 4 Trap type (TRAPTYPE) - 8-bit SPARC trap type

3: 0 Read as 0x0

24.6.5 DSU time tag counter

The trace buffer time tag counter is incremented each clock as long as the processor is running. The counter is stopped when the processor enters debug mode and when the DSU is disabled (unless the timer enable bit in the AHB trace buffer control register is set), and restarted when execution is resumed.

*Table 243.*0x000008 - DTTC - DSU time tag counter

31 0
TIMETAG
0
rw

31: 0 DSU Time Tag Value (TIMETAG)

The value is used as time tag in the instruction and AHB trace buffer.

The width of the timer is configurable at implementation time.

24.6.6 DSU ASI register

The DSU can perform diagnostic accesses to different ASI areas. The value in the ASI diagnostic access register is used as ASI while the address is supplied from the DSU.

*Table 244.*0x400024 - DASI - ASI diagnostic access register

31 8	7 0
RESERVED	ASI
0	NR
r	rw

31: 8 RESERVED

7: 0 ASI (ASI) - ASI to be used on diagnostic ASI access

24.6.7 AHB Trace buffer control register

The AHB trace buffer is controlled by the AHB trace buffer control register:

*Table 245.*0x000040 - ATBC - AHB trace buffer control register

31 16	15 8	7	6	5	4 3	2	1	0
DCNT	RESERVED	DF	SF	TE	TF	BW	BR	DM	EN

*Table 245.*0x000040 - ATBC - AHB trace buffer control register

0	0	0	0	0	0	0	0	0	0
rw	r	rw	rw	rw	rw	r	rw	rw	rw

31: 16 Trace buffer delay counter (DCNT) - Note that the number of bits actually implemented depends on the size of the trace buffer.

15: 9 RESERVED

8 Enable Debug Mode Timer Freeze (DF) - The time tag counter keeps counting in debug mode when at least one of the processors has the internal timer enabled. If this bit is set to '1' then the time tag counter is frozen when the processors have entered debug mode.

7 Sample Force (SF) - If this bit is written to '1' it will have the same effect on the AHB trace buffer as if HREADY was asserted on the bus at the same time as a sequential or non-sequential transfer is made. This means that setting this bit to '1' will cause the values in the trace buffer's sample registers to be written into the trace buffer, and new values will be sampled into the registers. This bit will automatically be cleared after one clock cycle.

Writing to the trace buffer still requires that the trace buffer is enabled (EN bit set to '1') and that the CPU is not in debug mode or that tracing is forced (TF bit set to '1'). This functionality is primarily of interest when the trace buffer is tracing a separate bus and the traced bus appears to have frozen.

6 Timer enable (TE) - Activates time tag counter also in debug mode.

5 Trace force (TF) - Activates trace buffer also in debug mode. Note that the trace buffer must be disabled when reading out trace buffer data via the core's register interface.

4: 3 Bus width (BW) - This value corresponds to log2(Supported bus width / 32)

2 Break (BR) - If set, the processor will be put in debug mode when AHB trace buffer stops due to AHB breakpoint hit.

1 Delay counter mode (DM) - Indicates that the trace buffer is in delay counter mode.

0 Trace enable (EN) - Enables the trace buffer.

24.6.8 AHB trace buffer index register

The AHB trace buffer index register contains the address of the next trace line to be written.

*Table 246.*0x000044 - ATBI - AHB trace buffer index register

31 4	3 0
INDEX	R
NR	0
rw	r

31: 4 Trace buffer index counter (INDEX) - Note that the number of bits actually implemented depends on the size of the trace buffer.

3: 0 Read as 0x0

24.6.9 AHB trace buffer filter control register

The trace buffer filter control register is only available if the core has been implemented with support for AHB trace buffer filtering.

*Table 247.*0x000048 - ATBFC - AHB trace buffer filter control register

31 14	13 12	11 10	9 8	7 4	3	2	1	0
RESERVED	WPF	R	BPF	RESERVED	PF	AF	FR	FW
0	0	0	0	0	0	0	0	0
r	rw	r	rw	r	rw	rw	rw	rw

31: 14 RESERVED

*Table 247.*0x000048 - ATBFC - AHB trace buffer filter control register

13: 12	AHB watchpoint filtering (WPF) - Bit 13 of this field applies to AHB watchpoint 2 and bit 12 applies to AHB watchpoint 1. If the WPF bit for a watchpoint is set to '1' then the watchpoint will not trigger unless the access also passes through the filter. This functionality can be used to, for instance, set a AHB watchpoint that only triggers if a specified master performs an access to a specified slave.
11: 10	RESERVED
9: 8	AHB breakpoint filtering (BPF) - Bit 9 of this field applies to AHB breakpoint 2 and bit 8 applies to AHB breakpoint 1. If the BPF bit for a breakpoint is set to '1' then the breakpoint will not trigger unless the access also passes through the filter. This functionality can be used to, for instance, set a AHB breakpoint that only triggers if a specified master performs an access to a specified slave. Note that if a AHB breakpoint is coupled with an AHB watchpoint then the setting of the corresponding bit in this field has no effect.
7: 4	RESERVED
3	Performance counter Filter (PF) - If this bit is set to '1', the cores performance counter (statistical) outputs will be filtered using the same filter settings as used for the trace buffer. If a filter inhibits a write to the trace buffer, setting this bit to '1' will cause the same filter setting to inhibit the pulse on the statistical output.
2	Address Filter (AF) - If this bit is set to '1', only the address range defined by AHB trace buffer breakpoint 2's address and mask will be included in the trace buffer.
1	Filter Reads (FR) - If this bit is set to '1', read accesses will not be included in the trace buffer.
0	Filter Writes (FW) - If this bit is set to '1', write accesses will not be included in the trace buffer.

24.6.10 AHB trace buffer filter mask register

The trace buffer filter mask register is only available if the core has been implemented with support for AHB trace buffer filtering.

*Table 248.*0x00004C - ATBFM - AHB trace buffer filter mask register

31 16	15 0
SMASK[15:0]	MMASK[15:0]
0	0
rw	rw

31: 16	Slave Mask (SMASK) - If SMASK[n] is set to '1', the trace buffer will not save accesses performed to slave n.
15: 0	Master Mask (MMASK) - If MMASK[n] is set to '1', the trace buffer will not save accesses performed by master n.

24.6.11 AHB trace buffer breakpoint registers

The DSU contains two breakpoint registers for matching AHB addresses. A breakpoint hit is used to freeze the trace buffer by automatically clearing the enable bit. Freezing can be delayed by programming the DCNT field in the trace buffer control register to a non-zero value. In this case, the DCNT value will be decremented for each additional trace until it reaches zero, after which the trace buffer is frozen. A mask register is associated with each breakpoint, allowing breaking on a block of addresses. Only address bits with the corresponding mask bit set to '1' are compared during breakpoint detection. To break on AHB load or store accesses, the LD and/or ST bits should be set.

*Table 249.*0x000050, 0x000058 - ATBBA - AHB trace buffer break address register

31 2	1	0
BADDR[31:2]		R
NR		0
rw		r

31: 2	Break point address (BADDR) - Bits 31:2 of breakpoint address
1: 0	Read as 0b00

*Table 250.*0x000054, 0x00005C - ATBBM - AHB trace buffer break mask register

31	2	1	0
BMASK[31:2]		LD	ST
NR		0	0
rw		rw	rw

31: 2	Breakpoint mask (BMASK) - (see text)
1	Load (LD) - Break on data load address
0	Store (ST) - Break on data store address

24.6.12 Instruction trace control register 0

The instruction trace control register 0 contains a pointer that indicates the next line of the instruction trace buffer to be written.

*Table 251.*0x110000 - ITBCO - Instruction trace control register 0

31 29	28 16	15 0
	RESERVED	ITPOINTER
	0	NR
	r	rw

31: 28	Trace filter configuration
27: 16	RESERVED
15: 0	Instruction trace pointer (ITPOINTER) - Note that the number of bits actually implemented depends on the size of the trace buffer

24.6.13 Instruction trace control register 1

The instruction trace control register 1 contains settings used for trace buffer overflow detection, in addition it includes settings used for some of the instruction trace buffer filtering options. This register can be written while the processor is running.

Bits [31:28] is used to enable or disable Instruction Trace Buffer Address based Filtering (ITBAF). ITBAF is intended to allow the available hardware watch-point (HWP) registers to be used as instruction trace buffer filters when they are not used for breakpoint operation. If a bit is set to '1' in ITBAF, the corresponding address and mask information in the HWP register will be used to filter instruction trace entries based on the program counter (PC) value. Bits[31:28] corresponds to HWP[3:0] respectively. ITBAF can only be used if the corresponding HWP register exist in the hardware. Instruction Trace Buffer Address based Filtering Option (ITBAFO, Bits[19:16]) determines the type of filtering for the corresponding ITBAF entry. If an ITBAFO entry is set to '0' only the PC value(s) that match the address and mask option in the corresponding HWP register will be logged in the instruction trace buffer (ITB). If a bit is set to '1' only the PC value(s) that does not match the address and mask option in the corresponding HWP register will be logged in the ITB. Bits[19:16] corresponds to the option for ITBAF[3:0] respectively. If there is more than one address filtering operation is enabled, the corresponding filtering operations will be combined together.

Bits[15:0] corresponds to ASI last digit based filtering mask (ASIFMASK). ASIFMASK is in effect when the trace filter configuration is set to 0xE (SPARC Format 3 LOAD or STORE instructions to alternate space 0x80 - 0xFF with ASI last digit base filtering). Bits[15:0] corresponds to digits [0xF:0x0] respectively. If a bit is set to '0' in the ASIFMASK, the load and store instructions which have an ASI between the range of 0x80-0xFF and have the corresponding last digit are logged in the instruction trace buffer. For example if only the bit0 and bit2 of the ASIFMASK are '0' then only the load and store instructions with ASIs 0x80, 0x82, 0x90, 0x92, 0xA0, 0xA2, 0xB0, 0xB2, 0xC0, 0xC2, 0xD0, 0xD2, 0xE0, 0xE2, 0xF0, 0xF2 are tracked in the ITB. After the reset of processor all the bits

in the ASIFMASK is set to 0x0000 which means by default all the ASIs in the range of 0x80-0xFF are tracked.

*Table 252.*0x110004 - ITBCI - Instruction trace control register 1

31 28	27	26 24	23	22 20	19 16	15 0
ITBAF	WO	TLIM	OV	RESERVED	ITBAFO	ASIFMASK
0	0	0	0	0	0	0
rw	rw	rw	rw	r	rw	rw

31: 28 Instruction Trace Buffer Address based Filtering (ITBAF) (see text)

27 Watchpoint on overflow (WO) - If this bit is set, and Break on iu watchpoint (BW) is enabled in the DSU control register, then a watchpoint will be inserted when a trace overflow is detected (TOV field in this register gets set).

26: 24 Trace Limit (TLIM) - TLIM is compared with the top bits of ITPOINTER in Instruction trace control register 0 to generate the value in the TOV field below.

23 Trace Overflow (TOV) - Gets set to '1' when the DSU detects that TLIM equals the top three bits of ITPOINTER.

22: 20 RESERVED

19: 16 Instruction Trace Buffer Address based Filtering Option (ITBAFO) (see text)

15: 0 ASI last digit based filtering mask (ASIFMASK) (see text)

24.7 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x017. For a description of vendor and device identifiers see GRLIB IP Library User's Manual.

24.8 Implementation

24.8.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support *grlib_async_reset_enable*. All registers that react on the reset signal will have a synchronous reset.

24.8.2 Technology mapping

DSU3 has one technology mapping generic, *tech*. This generic controls the implementation of which technology that will be used to implement the trace buffer memories. The AHB trace buffer will use two identical SYNCRAM64 blocks to implement the buffer memory (SYNCRAM64 may then result in two 32-bit wide memories on the target technology, depending on the technology map), with one additional 32-bit wide SYNCRAM if the system's AMBA data bus width is 64-bits, and also one additional 64-bit wide SYNCRAM if the system's AMBA data bus width exceeds 64 bits.

The depth of the RAMs depends on the KBYTES generic. If KBYTES = 1 (1 Kbyte), then the depth will be 64. If KBYTES = 2, then the RAM depth will be 128 and so on.

24.9 Configuration options

Table 253 shows the configuration options of the core (VHDL generics).

*Table 253.*Configuration options

Generic	Function	Allowed range	Default
hindex	AHB slave index	0 - NAHBSLV-1	0
haddr	AHB slave address (AHB[31:20])	0 - 16#FFF#	16#900#
hmask	AHB slave address mask	0 - 16#FFF#	16#F00#
ncpu	Number of attached processors	1 - 16	1
tbits	Number of bits in the time tag counter	2 - 63	30
tech	Memory technology for trace buffer RAM	0 - NTECH-1	0 (inferred)
kbytes	Size of trace buffer memory in Kbytes. A value of 0 will disable the trace buffer function.	0 - 64	0 (disabled)
clk2x	Support for LEON3 double-clocking (this generic is only available on dsu3x entity), see next section.	0 - 1	0 (disabled)
testen	Scan test support enable	0 - 1	0
bwidth	Traced AHB bus width	32, 64, 128	32
ahbpf	AHB performance counters and filtering. If *ahbpf* is non-zero the core will support AHB trace buffer filtering. If *ahbpf* is larger than 1 then the core's statistical outputs will be enabled.	0 - 2	0

24.10 Signal descriptions

Table 254 shows the interface signals of the core (VHDL ports). There are several top-level entities available for the DSU3. The dsu3x entity contains all signals and settings. The other entities are wrappers around dsu3x. The available entities are:

- dsu3 - Entity without support for double clocking. AHB trace of same bus as DSU AHB slave interface is connected to.
- dsu3_2x - Entity with support for LEON3 double-clocking. AHB trace of same bus as DSU AHB slave interface is connected to.
- dsu3_mb - Entity with support for AHB tracing of separate bus
- dsu3x - Entity with support for all features (double-clocking and tracing of separate bus)

24.11 Signal definitions and reset values

*Table 254.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	CPU and bus clock, on dsu3 and dsu3_mb entites	-
HCLK	N/A	Input	Bus clock, on dsu3_2x and dsu3x entities. Only used when double-clocking is enabled.	-
CPUCLK	N/A	Input	CPU clock, on dsu3_2x and dsu3x entities	-
AHBMI	*	Input	AHB master input signals, used for AHB tracing	-
AHBSI	*	Input	AHB slave input signals, used for AHB tracing when using dsu3 and dsu3_2x entities	-
AHBSO	*	Output	AHB slave output signals	-
TAHBSI	*	Input	AHB slave input signals, used for AHB tracing when using dsu3_mb and dsu3x entities	-
DBGI	-	Input	Debug signals from LEON3	-
DBGO	-	Output	Debug signals to LEON3	-
DSUI	ENABLE	Input	DSU enable	High
	BREAK	Input	DSU break	High
DSUO	ACTIVE	Output	Debug mode	High
	PWD[n-1 : 0]	Output	Clock gating enable for processor [n]	High
	ASTAT (record)	Output	AHB statistic/performance counter events	-
HCLKEN	N/A	Input	Double-clocking qualifier signal. Only used with double-clocking on dsu4_2x and dsu4x entities	High

* see GRLIB IP Library User's Manual

The signals and their reset values are described in table 255.

*Table 255.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
dsuen	Input	DSU enable	High	-
dsubre	Input	DSU break	High	-
dsuact	Output	Debug mode	High	Logical 0

24.12 Timing

The timing waveforms and timing parameters are shown in figure 60 and are defined in table 256.

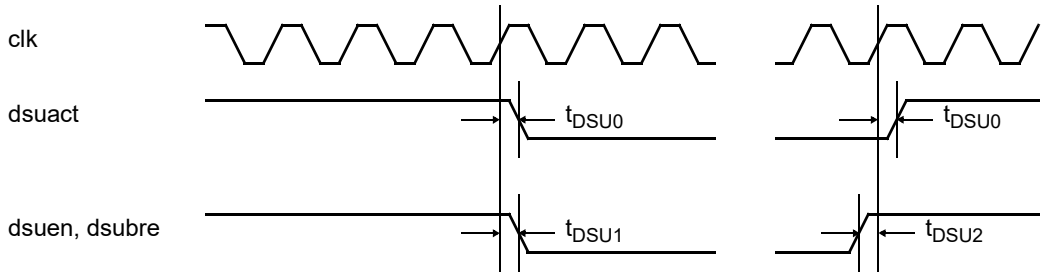


Figure 60. Timing waveforms

*Table 256.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{DSU0}	clock to output delay	rising *clk* edge	TBD	TBD	ns
t_{DSU1}	input to clock hold	rising *clk* edge	-	-	ns
t_{DSU2}	input to clock setup	rising *clk* edge	-	-	ns

- Note: The *dsubre* and *dsuen* are re-synchronized internally. These signals do not have to meet any setup or hold requirements.

24.13 Library dependencies

Table 257 shows libraries used when instantiating the core (VHDL libraries).

*Table 257.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AHB signal definitions
GAISLER	LEON3	Component, signals	Component declaration, signals declaration

24.14 Component declaration

The core has the following component declaration.

```
component dsu3
  generic (
    hindex : integer := 0;
    haddr : integer := 16#900#;
    hmask : integer := 16#f00#;
    ncpu    : integer := 1;
    tbits   : integer := 30;
    tech    : integer := 0;
    irq     : integer := 0;
    kbytes  : integer := 0
  );
  port (
    rst    : in  std_ulogic;
    clk    : in  std_ulogic;
    ahbmi  : in  ahb_mst_in_type;
    ahbsi  : in  ahb_slv_in_type;
    ahbso  : out ahb_slv_out_type;
    dbgi   : in l3_debug_out_vector(0 to NCPU-1);
    dbgo   : out l3_debug_in_vector(0 to NCPU-1);
    dsui   : in dsu_in_type;
    dsuo   : out dsu_out_type
```

```
  );
  end component;
```

24.15 Instantiation

This example shows how the core can be instantiated.

The DSU is always instantiated with at least one LEON3 processor. It is suitable to use a generate loop for the instantiation of the processors and DSU and showed below.

```
library ieee;
use ieee.std_logic_1164.all;
library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.leon3.all;

constant NCPU : integer := 1; -- select number of processors

signal leon3i : l3_in_vector(0 to NCPU-1);
signal leon3o : l3_out_vector(0 to NCPU-1);
signal irqi   : irq_in_vector(0 to NCPU-1);
signal irqo   : irq_out_vector(0 to NCPU-1);

signal dbgi : l3_debug_in_vector(0 to NCPU-1);
signal dbgo : l3_debug_out_vector(0 to NCPU-1);

signal dsui   : dsu_in_type;
signal dsuo   : dsu_out_type;

.
begin

cpu : for i in 0 to NCPU-1 generate
    u0 : leon3s-- LEON3 processor
    generic map (ahbndx => i, fabtech => FABTECH, memtech => MEMTECH)
    port map (clkm, rstn, ahbmi, ahbmo(i), ahbsi, ahbsi, ahbso,
 irqi(i), irqo(i), dbgi(i), dbgo(i));
    irqi(i) <= leon3o(i).irq; leon3i(i).irq <= irqo(i);
end generate;

dsu0 : dsu3-- LEON3 Debug Support Unit
    generic map (ahbndx => 2, ncpu => NCPU, tech => memtech, kbytes => 2)
    port map (rstn, clkm, ahbmi, ahbsi, ahbso(2), dbgo, dbgi, dsui, dsuo);
dsui.enable <= dsuen; dsui.break <= dsubre; dsuact <= dsuo.active;
```

25 DSU4 - LEON4 Hardware Debug Support Unit

25.1 Overview

To simplify debugging on target hardware, the LEON4 processor implements a debug mode during which the pipeline is idle and the processor is controlled through a special debug interface. The LEON4 Debug Support Unit (DSU) is used to control the processor during debug mode. The DSU acts as an AHB slave and can be accessed by any AHB master. An external debug host can therefore access the DSU through several different interfaces. Such an interface can be a serial UART (RS232), JTAG, PCI, USB or Ethernet. The DSU supports multi-processor systems and can handle up to 16 processors.

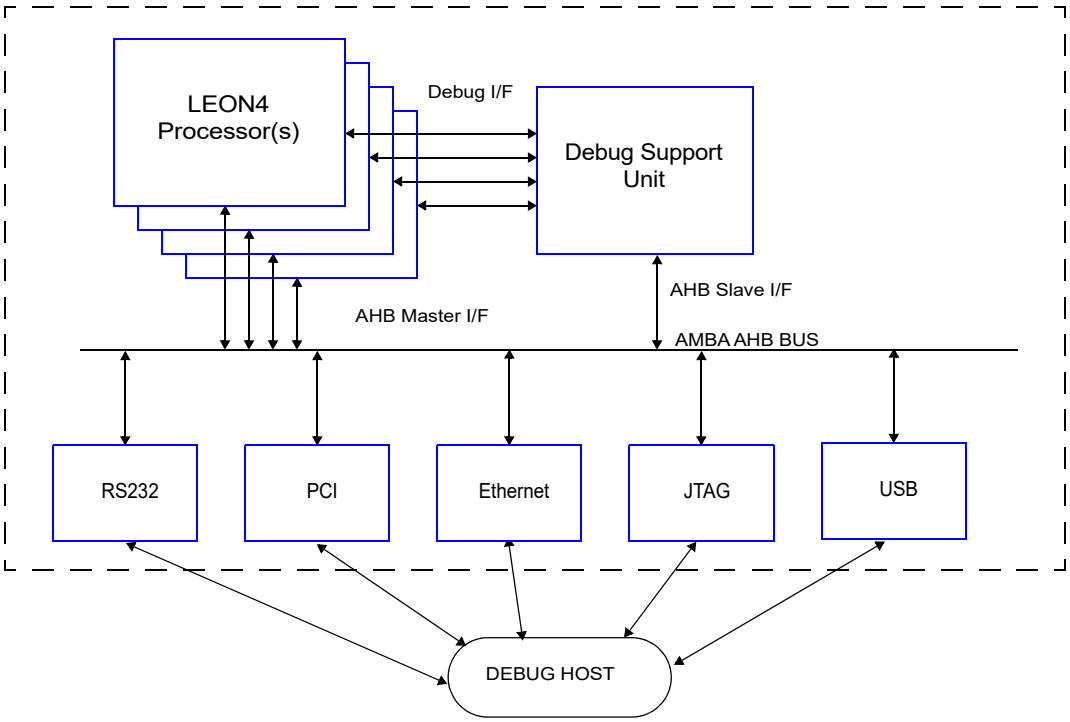


Figure 61. LEON4/DSU Connection

25.2 Operation

Through the DSU AHB slave interface, any AHB master can access the processor registers and the contents of the instruction trace buffer. The DSU control registers can be accessed at any time, while the processor registers and caches can only be accessed when the processor has entered debug mode. In debug mode, the processor pipeline is held and the processor state can be accessed by the DSU. Entering the debug mode can occur on the following events:

- executing a breakpoint instruction (ta 1)
- integer unit hardware breakpoint/watchpoint hit (trap 0xb)
- rising edge of the external break signal (DSUBRE)
- setting the break-now (BN) bit in the DSU control register
- a trap that would cause the processor to enter error mode
- occurrence of any, or a selection of traps as defined in the DSU control register
- after a single-step operation
- one of the processors in a multiprocessor system has entered the debug mode
- DSU AHB breakpoint or watchpoint hit

The debug mode can only be entered when the debug support unit is enabled through an external signal (DSUEN). For DSU break, and the break-now BN bit, to have effect the Break-on-IU-watchpoint (BW) bit must be set in the DSU control register. This bit is set when DSUBRE is active after reset and should also be set by debug monitor software when initializing the DSU. When the debug mode is entered, the following actions are taken:

- PC and nPC are saved in temporary registers (accessible by the debug unit)
- an output signal (DSUACT) is asserted to indicate the debug state
- the timer unit is (optionally) stopped to freeze the LEON timers and watchdog

The instruction that caused the processor to enter debug mode is not executed, and the processor state is kept unmodified. Execution is resumed by clearing the BN bit in the DSU control register or by deasserting DSUEN. The timer unit will be re-enabled and execution will continue from the saved PC and nPC. Debug mode can also be entered after the processor has entered error mode, for instance when an application has terminated and halted the processor. The error mode can be reset and the processor restarted at any address.

When a processor is in the debug mode, an access to ASI diagnostic area is forwarded to the IU which performs access with ASI equal to value in the DSU ASI register and address consisting of 20 LSB bits of the original address.

25.3 AHB trace buffer

The AHB trace buffer consists of a circular buffer that stores AHB data transfers, the monitored AHB bus is either the same bus as the DSU AHB slave interface is connected to, or a completely separate bus. The address, data and various control signals of the AHB bus are stored and can be read out for later analysis. The trace buffer is 128, 160 or 224 bits wide, depending on the AHB bus width. The way information stored is indicated in the table below:

*Table 258.*AHB Trace buffer data allocation

Bits	Name	Definition
223:160	Load/Store data	AHB HRDATA/HWDATA(127:64)
159:129	Load/Store data	AHB HRDATA/HWDATA(63:32)
127	AHB breakpoint hit	Set to ‘1’ if a DSU AHB breakpoint hit occurred.
126	-	Not used
125:96	Time tag	DSU time tag counter
95:80	-	Not used
79	Hwrite	AHB HWRITE
78:77	Htrans	AHB HTRANS
76:74	Hsize	AHB HSIZE
73:71	Hburst	AHB HBURST
70:67	Hmaster	AHB HMASTER
66	Hmastlock	AHB HMASTLOCK
65:64	Hresp	AHB HRESP
63:32	Load/Store data	AHB HRDATA/HWDATA(31:0)
31:0	Load/Store address	AHB HADDR

In addition to the AHB signals, the DSU time tag counter is also stored in the trace.

The trace buffer is enabled by setting the enable bit (EN) in the trace control register. Each AHB transfer is then stored in the buffer in a circular manner. The address to which the next transfer is written is held in the trace buffer index register, and is automatically incremented after each transfer. Trac-

ing is stopped when the EN bit is reset, or when a AHB breakpoint is hit. Tracing is temporarily suspended when the processor enters debug mode, unless the trace force bit (TF) in the trace control register is set. If the trace force bit is set, the trace buffer is activated as long as the enable bit is set. The force bit is reset if an AHB breakpoint is hit and can also be cleared by software. Note that neither the trace buffer memory nor the breakpoint registers (see below) can be read/written by software when the trace buffer is enabled.

The DSU has an internal time tag counter and this counter is frozen when the processor enters debug mode. When AHB tracing is performed in debug mode (using the trace force bit) it may be desirable to also enable the time tag counter. This can be done using the timer enable bit (TE). Note that the time tag is also used for the instruction trace buffer and the timer enable bit should only be set when using the DSU as an AHB trace buffer only, and not when performing profiling or software debugging. The timer enable bit is reset on the same events as the trace force bit.

25.3.1 AHB trace buffer filters

The DSU can be implemented with filters that can be applied to the AHB trace buffer, breakpoints and watchpoints. If implemented, these filters are controlled via the AHB trace buffer filter control and AHB trace buffer filter mask registers. The fields in these registers allows masking access characteristics such as master, slave, read, write and address range so that accesses that correspond to the specified mask are not written into the trace buffer. Address range masking is done using the second AHB breakpoint register set. The values of the LD and ST fields of this register has no effect on filtering.

25.3.2 AHB statistics

The DSU can be implemented to generate statistics from the traced AHB bus. When statistics collection is enabled the DSU will assert outputs that are suitable to connect to a LEON4 statistics unit (L4STAT). The statistical outputs can be filtered by the AHB trace buffer filters, this is controlled by the Performance counter Filter bit (PF) in the AHB trace buffer filter control register. The DSU can collect data for the events listed in table 259 below.

*Table 259.*AHB events

Event	Description	Note
idle	HTRANS=IDLE	Active when HTRANS IDLE is driven on the AHB slave inputs and slave has asserted HREADY.
busy	HTRANS=BUSY	Active when HTRANS BUSY is driven on the AHB slave inputs and slave has asserted HREADY.
nseq	HTRANS=NONSEQ	Active when HTRANS NONSEQ is driven on the AHB slave inputs and slave has asserted HREADY.
seq	HTRANS=SEQ	Active when HTRANS SEQUENTIAL is driven on the AHB slave inputs and slave has asserted HREADY.
read	Read access	Active when HTRANS is SEQUENTIAL or NON-SEQUENTIAL, slave has asserted HREADY and the HWRITE input is low.
write	Write access	Active when HTRANS is SEQUENTIAL or NON-SEQUENTIAL, slave has asserted HREADY and the HWRITE input is high.
hsize[5:0]	Transfer size	Active when HTRANS is SEQUENTIAL or NON-SEQUENTIAL, slave has asserted HREADY and HSIZE is BYTE (hsize[0]), HWORD (HSIZE[1]), WORD (hsize[2]), DWORD (hsize[3]), 4WORD hsize[4], or 8WORD (hsize[5]).
ws	Wait state	Active when HREADY input to AHB slaves is low and AMBA response is OKAY.
retry	RETRY response	Active when master receives RETRY response
split	SPLIT response	Active when master receives SPLIT response

*Table 259.*AHB events

Event	Description	Note
spdel	SPLIT delay	Active during the time a master waits to be granted access to the bus after reception of a SPLIT response. The core will only keep track of one master at a time. This means that when a SPLIT response is detected, the core will save the master index. This event will then be active until the same master is re-allowed into bus arbitration and is granted access to the bus. This also means that the delay measured will include the time for re-arbitration, delays from other ongoing transfers and delays resulting from other masters being granted access to the bus before the SPLIT:ed master is granted again after receiving SPLIT complete. If another master receives a SPLIT response while this event is active, the SPLIT delay for the second master will not be measured.
locked	Locked access	Active while the HMASTLOCK signal is asserted on the AHB slave inputs.

25.4 Instruction trace buffer

The instruction trace buffer consists of a circular buffer that stores executed instructions. The instruction trace buffer is located in the processor, and read out via the DSU. The trace buffer is 128 bits wide, the information stored is indicated in the table below:

*Table 260.*Instruction trace buffer data allocation

Bits	Name	Definition
126	Multi-cycle instruction	Set to '1' on the second instance of a multi-cycle instruction
125:96	Time tag	The value of the DSU time tag counter
95:64	Result or Store address/data	Instruction result, Store address or Store data
63:34	Program counter	Program counter (2 lsb bits removed since they are always zero)
33	Instruction trap	Set to '1' if traced instruction trapped
32	Processor error mode	Set to '1' if the traced instruction caused processor error mode
31:0	Opcode	Instruction opcode

During tracing, one instruction is stored per line in the trace buffer with the exception of atomic load/store instructions, which are entered twice (one for the load and one for the store operation). Bits [95:64] in the buffer correspond to the store address and the loaded data for load instructions. Bit 126 is set for the second entry.

When the processor enters debug mode, tracing is suspended. The trace buffer and the trace buffer control register can be read and written while the processor is in the debug mode. During the instruction tracing (processor in normal mode) the trace buffer and trace buffer control register 0 can not be written. If the two-port trace buffer is enabled (refer to the *tbuf* generic in section 81.15), then the trace buffer can be read contextually to the instruction tracing (processor in normal mode). The traced instructions can optionally be filtered on instruction types. Which instructions are traced is defined in the instruction trace register [31:28], as defined in the table below:

*Table 261.*Trace filter operation

Trace filter	Instructions traced
0x0	All instructions
0x1	SPARC Format 2 instructions
0x2	Control-flow changes. All Call, branch and trap instructions including branch targets
0x4	SPARC Format 1 instructions (CALL)
0x8	SPARC Format 3 instructions except LOAD or STORE
0xC	SPARC Format 3 LOAD or STORE instructions
0xD	SPARC Format 3 LOAD or STORE instructions to alternate space
0xE	SPARC Format 3 LOAD or STORE instructions to alternate space 0x80 - 0xFF with ASI last digit base filtering

It is also possible to filter traced instructions based on the program counter value. This option is combined with the filtering option if an additional filtering mechanism is activated from Table 261. Refer to section 25.6.13 for detailed information.

25.5 DSU memory map

The DSU memory map can be seen in table 262 below. In a multiprocessor systems, the register map is duplicated and address bits 27 - 24 are used to index the processor.

Note: The DSU memory interface is intended to be accessed by a debug monitor. Software running on the LEON processors should not access the DSU interface. Registers, such as ASR registers, may not have all fields available via the DSU interface.

*Table 262.*DSU memory map

Address offset	Register
0x000000	DSU control register
0x000008	Time tag counter
0x000020	Break and Single Step register
0x000024	Debug Mode Mask register
0x000040	AHB trace buffer control register
0x000044	AHB trace buffer index register
0x000048	AHB trace buffer filter control register
0x00004c	AHB trace buffer filter mask register
0x000050	AHB breakpoint address 1
0x000054	AHB mask register 1
0x000058	AHB breakpoint address 2
0x00005c	AHB mask register 2
0x000070	Instruction count register
0x000080	AHB watchpoint control register
0x000090 - 0x00009C	AHB watchpoint 1 data registers
0x0000A0 - 0x0000AC	AHB watchpoint 1 mask registers
0x0000B0 - 0x0000BC	AHB watchpoint 2 data registers
0x0000C0 - 0x0000CC	AHB watchpoint 2 mask registers
0x100000 - 0x10FFFF	Instruction trace buffer (..0: Trace bits 127 - 96, ..4: Trace bits 95 - 64, ..8: Trace bits 63 - 32, ..C : Trace bits 31 - 0)

*Table 262.*DSU memory map

Address offset	Register
0x110000	Instruction Trace buffer control register 0
0x110004	Instruction Trace buffer control register 1
0x200000 - 0x210000	AHB trace buffer (..0: Trace bits 127 - 96, ..4: Trace bits 95 - 64, ..8: Trace bits 63 - 32, ..C : Trace bits 31 - 0)
0x300000 - 0x3007FC	IU register file. The addresses of the IU registers depends on how many register windows has been implemented: %o*n*: 0x300000 + (((psr.cwp * 64) + 32 + *n**4) mod (NWINDOWS*64)) %l*n*: 0x300000 + (((psr.cwp * 64) + 64 + *n**4) mod (NWINDOWS*64)) %i*n*: 0x300000 + (((psr.cwp * 64) + 96 + *n**4) mod (NWINDOWS*64)) %g*n*: 0x300000 + (NWINDOWS*64) + n*4 %f*n*: 0x301000 + *n**4
0x300800 - 0x300FFC	IU register file check bits (LEON4FT only)
0x301000 - 0x30107C	FPU register file
0x400000	Y register
0x400004	PSR register
0x400008	WIM register
0x40000C	TBR register
0x400010	PC register
0x400014	NPC register
0x400018	FSR register
0x40001C	CPSR register
0x400020	DSU trap register
0x400024	DSU ASI register
0x400040 - 0x40007C	ASR16 - ASR31 (when implemented)
0x700000 - 0x7FFFFC	ASI diagnostic access (ASI = value in DSU ASI register, address = address[19:0]) ASI = 0x9 : Local instruction RAM ASI = 0xB : Local data RAM ASI = 0xC : Instruction cache tags ASI = 0xD : Instruction cache data ASI = 0xE : Data cache tags ASI = 0xF : Data cache data ASI = 0x1E : Separate snoop tags

25.6 DSU registers

25.6.1 DSU control register

The DSU is controlled by the DSU control register:

*Table 263.*0x000000 - CTRL - DSU control register

31	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		PW	HL	PE	EB	EE	DM	BZ	BX	BS	BW	BE	TE
0		0	0	0	*	*		*	*	0	*	*	*
r		r	rw	uc	r	r	r	rw	rw	rw	rw	rw	rw

31: 12 Reserved

11 Power down (PW) - Returns ‘1’ when processor is in power-down mode.

10 Processor halt (HL) - Returns ‘1’ on read when processor is halted. If the processor is in debug mode, setting this bit will put the processor in halt mode.

*Table 263.*0x000000 - CTRL - DSU control register

9	Processor error mode (PE) - returns '1' on read when processor is in error mode, else '0'. If written with '1', it will clear the error and halt mode.
8	External Break (EB) - Value of the external DSUBRE signal (read-only)
7	External Enable (EE) - Value of the external DSUEN signal (read-only)
6	Debug mode (DM) - Indicates when the processor has entered debug mode (read-only).
5	Break on error traps (BZ) - if set, will force the processor into debug mode on all *except* the following traps: priviledged_instruction, fpu_disabled, window_overflow, window_underflow, asynchronous_interrupt, ticc_trap.
4	Break on trap (BX) - if set, will force the processor into debug mode when any trap occurs.
3	Break on S/W breakpoint (BS) - if set, debug mode will be forced when an breakpoint instruction (ta 1) is executed.
2	Break on IU watchpoint (BW) - if set, debug mode will be forced on a IU watchpoint (trap 0xb).
1	Break on error (BE) - if set, will force the processor to debug mode when the processor would have entered error condition (trap in trap).
0	Trace enable (TE) - Enables instruction tracing. If set the instructions will be stored in the trace buffer. Remains set when then processor enters debug or error mode

25.6.2 DSU Break and Single Step register

This register is used to break or single step the processor(s). This register controls all processors in a multi-processor system, and is only accessible in the DSU memory map of processor 0.

*Table 264.*0x000020 - BRSS - DSU Break and Single Step register

31 16	15 0
SS[15:0]	BN[15:0]
0	0
rw	rw

31: 16	Single step (SSx) - if set, the processor x will execute one instruction and return to debug mode. The bit remains set after the processor goes into the debug mode. As an exception, if the instruction is a branch with the annul bit set, and if the delay instruction is effectively annulled, the processor will execute the branch, the annulled delay instruction and the instruction thereafter before returning to debug mode.
15: 0	Break now (BNx) -Force processor x into debug mode if the Break on watchpoint (BW) bit in the processors DSU control register is set. If cleared, the processor x will resume execution.

25.6.3 DSU Debug Mode Mask Register

When one of the processors in a multiprocessor LEON4 system enters the debug mode the value of the DSU Debug Mode Mask register determines if the other processors are forced in the debug mode. This register controls all processors in a multi-processor system, and is only accessible in the DSU memory map of processor 0.

*Table 265.*0x000024 - DBGM - DSU Debug Mode Mask register

31 16	15 0
DM[15:0]	ED[15:0]
0	0
rw	rw

31: 16	Debug mode mask (DMx) - If set, the corresponding processor will not be able to force running processors into debug mode even if it enters debug mode.
15: 0	Enter debug mode (EDx) - Force processor x into debug mode if any of processors in a multiprocessor system enters the debug mode. If 0, the processor x will not enter the debug mode.

25.6.4 DSU trap register

The DSU trap register is a read-only register that indicates which SPARC trap type that caused the processor to enter debug mode. When debug mode is force by setting the BN bit in the DSU control register, the trap type will be 0xb (hardware watchpoint trap).

*Table 266.*0x400020 - DTR - DSU Trap register

31 13	12	11 4	3 0
RESERVED	EM	TRAPTYPE	R
0	NR	NR	0
r	r	r	r

31: 13 RESERVED

12 Error mode (EM) - Set if the trap would have cause the processor to enter error mode.

11: 4 Trap type (TRAPTYPE) - 8-bit SPARC trap type

3: 0 Read as 0x0

25.6.5 DSU time tag counter

The trace buffer time tag counter is incremented each clock as long as the processor is running. The counter is stopped when the processor enters debug mode and when the DSU is disabled (unless the timer enable bit in the AHB trace buffer control register is set), and restarted when execution is resumed.

*Table 267.*0x000008 - DTTL - DSU time tag counter

31 0
TIMETAG
0
rw

31: 0 DSU Time Tag Value (TIMETAG)

The value is used as time tag in the instruction and AHB trace buffer.

The width of the timer is configurable at implementation time.

25.6.6 DSU ASI register

The DSU can perform diagnostic accesses to different ASI areas. The value in the ASI diagnostic access register is used as ASI while the address is supplied from the DSU.

*Table 268.*0x400024 -DASI - ASI diagnostic access register

31 8	7 0
RESERVED	ASI
0	NR
r	rw

31: 8 RESERVED

7: 0 ASI (ASI) - ASI to be used on diagnostic ASI access

25.6.7 AHB Trace buffer control register

The AHB trace buffer is controlled by the AHB trace buffer control register:

*Table 269.*0x000040 - ATBC - AHB trace buffer control register

31 16	15 9	8	7	6	5	4 3	2	1	0
DCNT	RESERVED	DF	SF	TE	TF	BW	BR	DM	EN
0	0	0	0	0	0	*	0	0	*
rw	r	rw	rw	rw	rw	r	rw	rw	rw

31: 16 Trace buffer delay counter (DCNT) - Note that the number of bits actually implemented depends on the size of the trace buffer.

15: 9 RESERVED

8 Enable Debug Mode Timer Freeze (DF) - The time tag counter keeps counting in debug mode when at least one of the processors has the internal timer enabled. If this bit is set to '1' then the time tag counter is frozen when the processors have entered debug mode.

7 Sample Force (SF) - If this bit is written to '1' it will have the same effect on the AHB trace buffer as if HREADY was asserted on the bus at the same time as a sequential or non-sequential transfer is made. This means that setting this bit to '1' will cause the values in the trace buffer's sample registers to be written into the trace buffer, and new values will be sampled into the registers. This bit will automatically be cleared after one clock cycle.

Writing to the trace buffer still requires that the trace buffer is enabled (EN bit set to '1') and that the CPU is not in debug mode or that tracing is forced (TF bit set to '1'). This functionality is primarily of interest when the trace buffer is tracing a separate bus and the traced bus appears to have frozen.

6 Timer enable (TE) - Activates time tag counter also in debug mode.

5 Trace force (TF) - Activates trace buffer also in debug mode. Note that the trace buffer must be disabled when reading out trace buffer data via the core's register interface.

4: 3 Bus width (BW) - This value corresponds to log2(Supported bus width / 32)

2 Break (BR) - If set, the processor will be put in debug mode when AHB trace buffer stops due to AHB breakpoint hit.

1 Delay counter mode (DM) - Indicates that the trace buffer is in delay counter mode.

0 Trace enable (EN) - Enables the trace buffer.

25.6.8 AHB trace buffer index register

The AHB trace buffer index register contains the address of the next trace line to be written.

*Table 270.*0x000044 - ATBI - AHB trace buffer index register

31 4	3 0
INDEX	R
NR	0
rw	r

31: 4 Trace buffer index counter (INDEX) - Note that the number of bits actually implemented depends on the size of the trace buffer.

3: 0 Read as 0x0

25.6.9 AHB trace buffer filter control register

The trace buffer filter control register is only available if the core has been implemented with support for AHB trace buffer filtering.

*Table 271.*0x000048 - ATBFC - AHB trace buffer filter control register

31 14	13	12	11	10	9	8	7 4	3	2	1	0
RESERVED	WPF		R		BPF		RESERVED	PF	AF	FR	FW
0	0		0		0		0	0	0	0	0
r	rw		r		rw		r	rw	rw	rw	rw

*Table 271.*0x000048 - ATBFC - AHB trace buffer filter control register

31: 14	RESERVED
13: 12	AHB watchpoint filtering (WPF) - Bit 13 of this field applies to AHB watchpoint 2 and bit 12 applies to AHB watchpoint 1. If the WPF bit for a watchpoint is set to '1' then the watchpoint will not trigger unless the access also passes through the filter. This functionality can be used to, for instance, set a AHB watchpoint that only triggers if a specified master performs an access to a specified slave.
11: 10	RESERVED
9: 8	AHB breakpoint filtering (BPF) - Bit 9 of this field applies to AHB breakpoint 2 and bit 8 applies to AHB breakpoint 1. If the BPF bit for a breakpoint is set to '1' then the breakpoint will not trigger unless the access also passes through the filter. This functionality can be used to, for instance, set a AHB breakpoint that only triggers if a specified master performs an access to a specified slave. Note that if a AHB breakpoint is coupled with an AHB watchpoint then the setting of the corresponding bit in this field has no effect.
7: 4	RESERVED
3	Performance counter Filter (PF) - If this bit is set to '1', the cores performance counter (statistical) outputs will be filtered using the same filter settings as used for the trace buffer. If a filter inhibits a write to the trace buffer, setting this bit to '1' will cause the same filter setting to inhibit the pulse on the statistical output.
2	Address Filter (AF) - If this bit is set to '1', only the address range defined by AHB trace buffer breakpoint 2's address and mask will be included in the trace buffer.
1	Filter Reads (FR) - If this bit is set to '1', read accesses will not be included in the trace buffer.
0	Filter Writes (FW) - If this bit is set to '1', write accesses will not be included in the trace buffer.

25.6.10 AHB trace buffer filter mask register

The trace buffer filter mask register is only available if the core has been implemented with support for AHB trace buffer filtering.

*Table 272.*0x00004C - ATBFM - AHB trace buffer filter mask register

31 16	15 0
SMASK[15:0]	MMASK[15:0]
0	0
rw	rw

31: 16	Slave Mask (SMASK) - If SMASK[n] is set to '1', the trace buffer will not save accesses performed to slave n.
15: 0	Master Mask (MMASK) - If MMASK[n] is set to '1', the trace buffer will not save accesses performed by master n.

25.6.11 AHB trace buffer breakpoint registers

The DSU contains two breakpoint registers for matching AHB addresses. A breakpoint hit is used to freeze the trace buffer by automatically clearing the enable bit. Freezing can be delayed by programming the DCNT field in the trace buffer control register to a non-zero value. In this case, the DCNT value will be decremented for each additional trace until it reaches zero, after which the trace buffer is frozen. A mask register is associated with each breakpoint, allowing breaking on a block of addresses. Only address bits with the corresponding mask bit set to '1' are compared during breakpoint detection. To break on AHB load or store accesses, the LD and/or ST bits should be set.

*Table 273.*0x000050, 0x000058 - ATBBA - AHB trace buffer break address register

31 2	1	0
BADDR[31:2]		R
NR		0
rw		r

*Table 273.*0x000050, 0x000058 - ATBBA - AHB trace buffer break address register

31: 2	Break point address (BADDR) - Bits 31:2 of breakpoint address
1: 0	Read as 0b00

*Table 274.*0x000054, 0x00005C - ATBBM - AHB trace buffer break mask register

31 2	1	0
BMASK[31:2]	LD	ST
NR	0	0
rw	rw	rw

31: 2	Breakpoint mask (BMASK) - (see text)
1	Load (LD) - Break on data load address
0	Store (ST) - Break on data store address

25.6.12 Instruction trace control register 0

The instruction trace control register 0 contains a pointer that indicates the next line of the instruction trace buffer to be written.

*Table 275.*0x110000 - ITBCO - Instruction trace control register 0

31 28	27 16	15 0
TFILT	RESERVED	ITPOINTER
0	0	0
rw	r	rw

31: 28	Trace filter configuration
27: 16	RESERVED
15: 0	Instruction trace pointer (ITPOINTER) - Note that the number of bits actually implemented depends on the size of the trace buffer

25.6.13 Instruction trace control register 1

The instruction trace control register 1 contains settings used for trace buffer overflow detection, in addition it includes settings used for some of the instruction trace buffer filtering options. This register can be written while the processor is running.

Bits [31:28] is used to enable or disable Instruction Trace Buffer Address based Filtering (ITBAF). ITBAF is intended to allow the available hardware watch-point (HWP) registers to be used as instruction trace buffer filters when they are not used for breakpoint operation. If a bit is set to ‘1’ in ITBAF, the corresponding address and mask information in the HWP register will be used to filter instruction trace entries based on the program counter (PC) value. Bits[31:28] corresponds to HWP[3:0] respectively. ITBAF can only be used if the corresponding HWP register exist in the hardware. Instruction Trace Buffer Address based Filtering Option (ITBAFO, Bits[19:16]) determines the type of filtering for the corresponding ITBAF entry. If an ITBAFO entry is set to ‘0’ only the PC value(s) that match the address and mask option in the corresponding HWP register will be logged in the instruction trace buffer (ITB). If a bit is set to ‘1’ only the PC value(s) that does not match the address and mask option in the corresponding HWP register will be logged in the ITB. Bits[19:16] corresponds to the option for ITBAF[3:0] respectively. If there is more than one address filtering operation is enabled, the corresponding filtering operations will be combined together.

Bits[15:0] corresponds to ASI last digit based filtering mask (ASIFMASK). ASIFMASK is in effect when the trace filter configuration is set to 0xE (SPARC Format 3 LOAD or STORE instructions to alternate space 0x80 - 0xFF with ASI last digit base filtering). Bits[15:0] corresponds to digits [0xF:0x0] respectively. If a bit is set to ‘0’ in the ASIFMASK, the load and store instructions which have an ASI between the range of 0x80-0xFF and have the corresponding last digit are logged in the instruction trace buffer. For example if only the bit0 and bit2 of the ASIFMASK is set then only the load and store instructions with ASIs 0x80, 0x82, 0x90, 0x92, 0xA0, 0xA2, 0xB0, 0xB2, 0xC0, 0xC2,

0xD0, 0xD2, 0xE0, 0xE2, 0xF0, 0xF2 are tracked. After the reset of processor all the bits in the ASIFMASK is set to 0x0000 which means by default all the ASIs in the range of 0x80-0xFF are tracked.

*Table 276.*0x110004 - ITBCI - Instruction trace control register 1

31 28	27	26 24	23	22 20	19 16	15 0
ITBAF	WO	TLIM	OV	RESERVED	ITBAFO	ASIFMASK
0	0	0	0	0	0	0
rw	rw	rw	rw	r	rw	rw

31: 28 Instruction Trace Buffer Address based Filtering (ITBAF) (see text)

27 Watchpoint on overflow (WO) - If this bit is set, and Break on iu watchpoint (BW) is enabled in the DSU control register, then a watchpoint will be inserted when a trace overflow is detected (TOV field in this register gets set).

26: 24 Trace Limit (TLIM) - TLIM is compared with the top bits of ITPOINTER in Instruction trace control register 0 to generate the value in the TOV field below.

23 Trace Overflow (TOV) - Gets set to '1' when the DSU detects that TLIM equals the top three bits of ITPOINTER.

22: 20 RESERVED

19: 16 Instruction Trace Buffer Address based Filtering Option (ITBAFO) (see text)

15: 0 ASI last digit based filtering mask (ASIFMASK) (see text)

25.6.14 Instruction count register

The DSU contains an instruction count register to allow profiling of application, or generation of debug mode after a certain clocks or instructions. The instruction count register consists of a 29-bit down-counter, which is decremented on either each clock (IC=0) or on each executed instruction (IC=1). In profiling mode (PE=1), the counter will set to all ones after an underflow without generating a processor break. In this mode, the counter can be periodically polled and statistics can be formed on CPI (clocks per instructions). In non-profiling mode (PE=0), the processor will be put in debug mode when the counter underflows. This allows a debug tool such as GRMON to execute a defined number of instructions, or for a defined number of clocks.

*Table 277.*0x000070 - ICNT - Instruction count register

31	30	29	28 0
CE	IC	PE	ICOUNT[28:0]
0	0	0	NR
rw	rw	rw	rw

31 Counter Enable (CE) - Counter enable

30 Instruction Count (IC) - Instruction (1) or clock (0) counting

29 Profiling Enable (PE) - Profiling enable

28: 0 Instruction count (ICOUNT) - Instruction count

25.6.15 AHB watchpoint control register

The DSU has two AHB watchpoints that can be used to freeze the AHB tracebuffer, or put the processor in debug mode, when a specified data pattern occurs on the AMBA bus. These watchpoints can also be coupled with the two AHB breakpoints so that a watchpoint will not trigger unless the AHB breakpoint is triggered. This also means that when a watchpoint is coupled with an AHB breakpoint,

the breakpoint will not cause an AHB tracebuffer freeze, or put the processor(s), in debug mode unless also the watchpoint is triggered.

*Table 278.*0x000080 - AHBWPC - AHB watchpoint control register

31	7	6	5	4	3	2	1	0
RESERVED		IN	CP	EN	R	IN	CP	EN
0		0	0	0	0	0	0	0
r		rw	rw	rw	r	rw	rw	rw

31: 7 RESERVED

6 Invert (IN) - Invert AHB watchpoint 2. If this bit is set the watchpoint will trigger if data on the AHB bus does NOT match the specified data pattern (typically only usable if the watchpoint has been coupled with an address by setting the CP field).

5 Couple (CP) - Couple AHB watchpoint 2 with AHB breakpoint 1

4 Enable (EN) - Enable AHB watchpoint 2

3 RESERVED

2 Invert (IN) - Invert AHB watchpoint 1. If this bit is set the watchpoint will trigger if data on the AHB bus does NOT match the specified data pattern (typically only usable if the watchpoint has been coupled with an address by setting the CP field).

1 Couple (CP) - Couple AHB watchpoint 1 with AHB breakpoint 1

0 Enable (EN) - Enable AHB watchpoint 1

25.6.16 AHB watchpoint data and mask registers

The AHB watchpoint data and mask registers specify the data pattern for an AHB watchpoint. A watchpoint hit is used to freeze the trace buffer by automatically clearing the enable bit. A watchpoint hit can also be used to force the processor(s) to debug mode.

A mask register is associated with each data register. Only data bits with the corresponding mask bit set to '1' are compared during watchpoint detection.

*Table 279.*0x000040 to 0x00004C - 0x0000B0 to 0x0000BC - AHBWPPO-7 - AHB watchpoint data register

31	0
DATA[127-n*32 : 96-n*32]	
NR	
rw	

31: 0 AHB watchpoint data (DATA) - Specifies the data pattern of one word for an AHB watchpoint. The lower part of the register address specifies with part of the bus that the register value will be compared against: Offset 0x0 specifies the data value for AHB bus bits 127:96, 0x4 for bits 95:64, 0x8 for 63:32 and offset 0xC for bits 31:0.

*Table 280.*0x0000A0 - 0x0000AC - 0x0000C0 to 0x0000CC - AHBWPMO-7 - AHB watchpoint mask register

31	0
MASK[127-n*32 : 96-n*32]	
NR	
rw	

31: 0 AHB watchpoint mask (MASK) - Specifies the mask to select bits for comparison out of one word for an AHB watchpoint. The lower part of the register address specifies with part of the bus that the register value will be compared against: Offset 0x0 specifies the data value for AHB bus bits 127:96, 0x4 for bits 95:64, 0x8 for 63:32 and offset 0xC for bits 31:0.

In a system with 64-bit bus width only half of the data and mask registers must be written. For AHB watchpoint 1, a data value with 64-bits would be written to the AHB watchpoint data registers at offsets 0x98 and 0x9C. The corresponding mask bits would be set in mask registers at offsets 0xA8 and 0xAC.

In most GRLIB systems with wide AMBA buses, the data for an access size that is less than the full bus width will be replicated over the full bus. For instance, a 32-bit write access from a LEON processor on a 64-bit bus will place the same data on bus bits 64:32 and 31:0.

25.7 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x017. For a description of vendor and device identifiers see GRLIB IP Library User's Manual.

25.8 Implementation

25.8.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers, except synchronization registers, if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core will use asynchronous reset for all registers, except synchronization registers, if the GRLIB config package setting *grlib_async_reset_enable* is set.

25.8.2 Technology mapping

DSU4 has one technology mapping generic, *tech*. This generic controls the implementation of which technology that will be used to implement the trace buffer memories. The AHB trace buffer will use two identical SYNCRAM64 blocks to implement the buffer memory (SYNCRAM64 may then result in two 32-bit wide memories on the target technology, depending on the technology map), with one additional 32-bit wide SYNCRAM if the system's AMBA data bus width is 64-bits, and also one additional 64-bit wide SYNCRAM if the system's AMBA data bus width exceeds 64 bits.

The depth of the RAMs depends on the KBYTES generic. If KBYTES = 1 (1 Kbyte), then the depth will be 64. If KBYTES = 2, then the RAM depth will be 128 and so on.

25.9 Configuration options

Table 281 shows the configuration options of the core (VHDL generics).

*Table 281.*Configuration options

Generic	Function	Allowed range	Default
hindex	AHB slave index	0 - NAHBSLV-1	0
haddr	AHB slave address (AHB[31:20])	0 - 16#FFF#	16#900#
hmask	AHB slave address mask	0 - 16#FFF#	16#F00#
ncpu	Number of attached processors	1 - 16	1
tbits	Number of bits in the time tag counter	2 - 63	30
tech	Memory technology for trace buffer RAM	0 - NTECH-1	0 (inferred)
kbytes	Size of trace buffer memory in KiB. A value of 0 will disable the trace buffer function.	0 - 64	0 (disabled)
clk2x	Enable LEON4 double-clocking (generic is only available on dsu4_2x and dsu4x entities, see next section)	0 - 1	0
bwidth	Traced AHB bus width	32, 64, 128	64
ahbpf	AHB performance counters and filtering. If *ahbpf* is non-zero the core will support AHB trace buffer filtering. If *ahbpf* is larger than 1 then the core's statistical outputs will be enabled.	0 - 2	0
ahbwp	AHB watchpoint enable. If *ahbwp* is non-zero (default) then the core will support AHB watchpoints (also referred to as AHB data breakpoints). Pipeline registers will be added when *ahbwp* is set to 2 (default value), one register for each bit on the AMBA data bus. This setting is recommended in order to improve timing but has a cost in area. The pipeline registers will also lead to the AHB watchpoint being triggered one cycle later. It is recommended to leave this functionality enabled. However, the added logic can create critical timing paths from the AMBA data vectors and so AHB watchpoints can be completely disabled by setting this generic to 0.	0 - 2	2
scantest	Scan test support enable	0 - 1	0
pipedbg	Add pipeline registers on signals from LEON4. If critical timing paths show between, or through, the DSU4 and LEON4 then this value can be set to 1 to add pipeline registers on the dbgi input vector. This adds one additional wait state on some DSU register accesses.	0 - 1	0
pipeahbt	Add pipeline registers on AMBA signals to AHB trace buffer. If there are critical timing paths between the AMBA AHB bus and the DSU AHB trace buffer memory then this value can be set to 1 to add one stage of pipelining between the AHB bus and the trace buffer RAM.	0 - 1	0

25.10 Signal descriptions

Table 282 shows the interface signals of the core (VHDL ports). There are several top-level entities available for the DSU4. The dsu4x entity contains all signals and settings. The other entities are wrappers around dsu4x. The available entities are:

- dsu4 - Entity without support for double clocking. AHB trace of same bus as DSU AHB slave interface is connected to.
- dsu4_2x - Entity with support for LEON4 double-clocking. AHB trace of same bus as DSU AHB slave interface is connected to.
- dsu4_mb - Entity with support for AHB tracing of separate bus
- dsu4x - Entity with support for all features (tracing of separate bus and LEON4 double-clocking).

*Table 282.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock, used in dsu4_mb and dsu4 entities	-
HCLK	N/A	Input	Bus clock, used in dsu4_2x and dsu4x entites, only used when double-clocking is enabled	-
CPUCLK	N/A	Input	CPU clock, used in dsu4x and dsu4_2x entities	-
FCPUCLK	N/A	Input	Free running (never gated) CPU clock, only used on dsu4x entity.	-
AHBMI	*	Input	AHB master input signals, used for AHB tracing	-
AHBSI	*	Input	AHB slave input signals, used for AHB tracing when using dsu4 and dsu4_2x entities	-
AHBSO	*	Output	AHB slave output signals	-
TAHBSI	*	Input	AHB slave input signals, used for AHB tracing when using dsu4_mb and dsu4x entities.	-
DBGI	-	Input	Debug signals from LEON4	-
DBGO	-	Output	Debug signals to LEON4	-
DSUI	ENABLE	Input	DSU enable	High
	BREAK	Input	DSU break	High
DSUO	ACTIVE	Output	Debug mode	High
	PWD[n-1 : 0]	Output	Clock gating enable for processor [n]	High
	ASTAT (record)	Output	AHB statistic/performance counter events	-
HCLKEN	N/A	Input	Double-clocking qualifier signal. Only used with double-clocking on dsu4_2x and dsu4x entities	High

* see GRLIB IP Library User's Manual

25.11 Signal definitions and reset values

The signals and their reset values are described in table 283.

*Table 283.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
dsuen	Input	DSU enable	High	-
dsubre	Input	DSU break	High	-
dsuact	Output	Debug mode	High	Logical 0

25.12 Timing

The timing waveforms and timing parameters are shown in figure 62 and are defined in table 284.

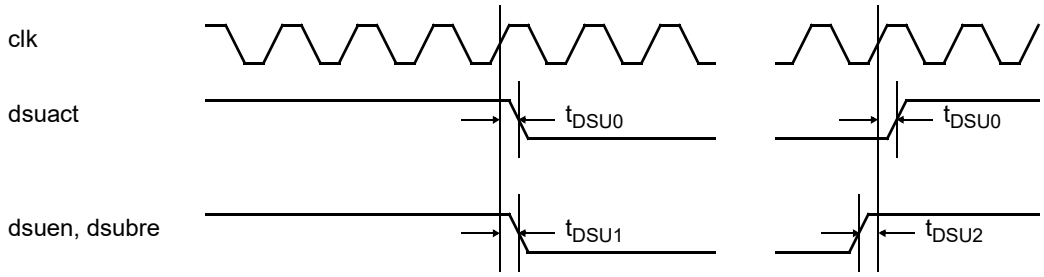


Figure 62. Timing waveforms

*Table 284.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{DSU0}	clock to output delay	rising *clk* edge	TBD	TBD	ns
t_{DSU1}	input to clock hold	rising *clk* edge	-	-	ns
t_{DSU2}	input to clock setup	rising *clk* edge	-	-	ns

Note: The *dsubre* and *dsuen* are re-synchronized internally. These signals do not have to meet any setup or hold requirements.

25.13 Library dependencies

Table 285 shows libraries used when instantiating the core (VHDL libraries).

*Table 285.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AHB signal definitions
GAISLER	LEON4	Component, signals	Component declaration, signals declaration

25.14 Component declaration

The core has the following component declaration.

```
component dsu4
  generic (
    hindex : integer := 0;
    haddr : integer := 16#900#;
    hmask : integer := 16#f00#;
    ncpu    : integer := 1;
    tbits   : integer := 30;
    tech    : integer := 0;
    irq     : integer := 0;
    kbytes  : integer := 0
  );
  port (
    rst    : in  std_ulogic;
    clk    : in  std_ulogic;
    ahbmi  : in  ahb_mst_in_type;
    ahbsi  : in  ahb_slv_in_type;
    ahbso  : out ahb_slv_out_type;
    dbgi   : in l4_debug_out_vector(0 to NCPU-1);
    dbgo   : out l4_debug_in_vector(0 to NCPU-1);
    dsui   : in dsu4_in_type;
    dsuo   : out dsu4_out_type
```

```
  );
  end component;
```

25.15 Instantiation

This example shows how the core can be instantiated.

The DSU is always instantiated with at least one LEON4 processor. It is suitable to use a generate loop for the instantiation of the processors and DSU and showed below.

```
library ieee;
use ieee.std_logic_1164.all;
library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.leon4.all;

constant NCPU : integer := 1; -- select number of processors

signal leon4i : l4_in_vector(0 to NCPU-1);
signal leon4o : l4_out_vector(0 to NCPU-1);
signal irqi   : irq_in_vector(0 to NCPU-1);
signal irqo   : irq_out_vector(0 to NCPU-1);

signal dbgi : l4_debug_in_vector(0 to NCPU-1);
signal dbgo : l4_debug_out_vector(0 to NCPU-1);

signal dsui   : dsu4_in_type;
signal dsuo   : dsu4_out_type;

.
begin

cpu : for i in 0 to NCPU-1 generate
    u0 : leon4s                    -- LEON4 processor
    generic map (ahbndx => i, fabtech => FABTECH, memtech => MEMTECH)
    port map (clkm, rstn, ahbmi, ahbmo(i), ahbsi, ahbsi, ahbso,
 irqi(i), irqo(i), dbgi(i), dbgo(i));
    irqi(i) <= leon4o(i).irq; leon4i(i).irq <= irqo(i);
end generate;

dsu0 : dsu4           -- LEON4 Debug Support Unit
    generic map (ahbndx => 2, ncpu => NCPU, tech => memtech, kbytes => 2)
    port map (rstn, clkm, ahbmi, ahbsi, ahbso(2), dbgo, dbgi, dsui, dsuo);
dsui.enable <= dsuen; dsui.break <= dsubre; dsuact <= dsuo.active;
```

26 FTAHBRAM - On-chip SRAM with EDAC and AHB interface

26.1 Overview

The FTAHBRAM core is a version of the AHBRAM core with added Error Detection And Correction (EDAC). The on-chip memory is accessed via an AMBA AHB slave interface. The memory implements a configurable amount of accessible memory (configured via the *kbytes* VHDL generic). Registers are accessed via an AMB APB interface.

The on-chip memory implements volatile memory that is protected by means of Error Detection And Correction (EDAC). One error can be corrected and two errors can be detected, which is performed by using a (32, 7) BCH code or by technology specific protection provided by the target technology RAMs (implementation option, if supported by target technology). Some of the optional features available are single error counter, diagnostic reads and writes and additional pipeline registers. Configuration is performed via a configuration register.

Figure 63 shows a block diagram of the internals of the controller. The block diagram shows the technology agnostic implementation. If target technology specific protection is selected then the encoder and decoder are not implemented in the FTAHBRAM.

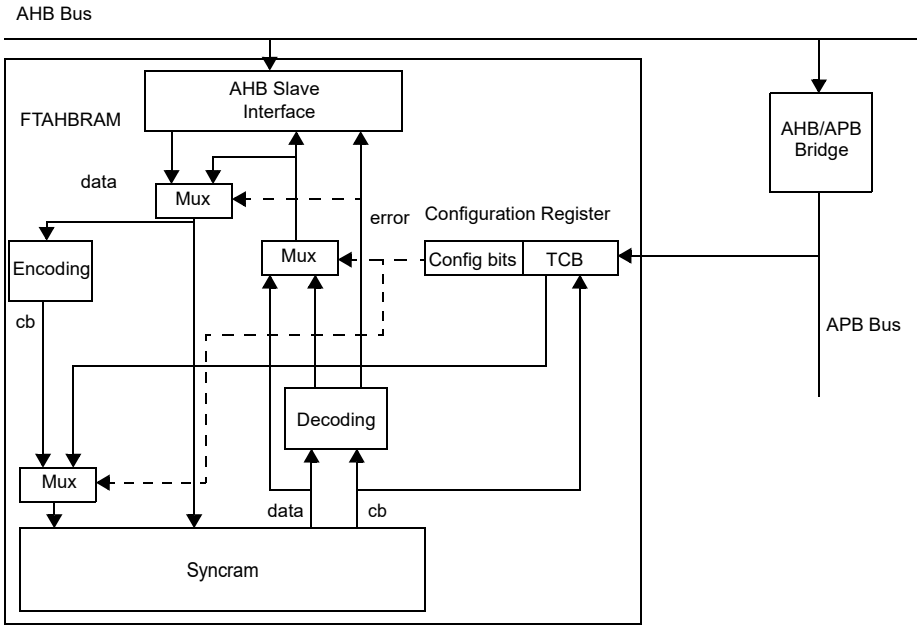


Figure 63. Block diagram

26.2 Operation

26.2.1 Overview

The on-chip fault tolerant memory is accessed through an AMBA AHB slave interface. The maximum AMBA access size supported is configurable through the *maccsz* VHDL generic. The controller supports all access sizes up to *maccsz* and the default value for *maccsz* is set to the maximum bus width configured for GRLIB (AHBDW constant).

The memory address range is configurable with VHDL generics. As for the standard AHB RAM, the memory technology and size is configurable through the *tech* and *kbytes* VHDL generics. The minimum size is 1 KiB and the maximum is technology dependent.

If the core is implemented without AHB pipeline registers then the EDAC functionality can be completely removed by setting the edacen VHDL generic to zero during synthesis. The APB interface is

also removed since it is redundant without EDAC. If AHB pipeline registers are included then EDAC is always enabled and the APB interface is present.

Run-time configuration is done by writing to a configuration register accessed through an AMBA APB interface. The following can be configured during run-time: EDAC can be enabled and disabled. When it is disabled, reads and writes will behave as the standard memory. Read and write diagnostics can be controlled through separate bits. The single error counter can be reset.

26.2.2 Read and write behaviour

If EDAC is disabled (EN bit in configuration register set to 0) write data is passed directly to the memory area and read data will appear on the AHB bus immediately after it arrives from memory. If EDAC is enabled write data is passed to an encoder which outputs a 7-bit checksum. The checksum is stored together with the data in memory and the whole operation is performed without any added waitstates. This applies to word and wider stores (32-bit, 64-bit, 128-bit). If a byte or halfword store is performed, the whole word to which the byte or halfword belongs must first be read from memory (read - modify - write). A new checksum is calculated when the new data is placed in the word and both data and checksum are stored in memory. This is done with 1 - 2 additional waitstates compared to the non EDAC case.

Reads with EDAC disabled are performed with 0 or 1 waitstates while there could also be 2 waitstates when EDAC is enabled. There is no difference between wide, word and subword reads. Table 286 shows a summary of the number of waitstates for the different operations with and without EDAC.

*Table 286.*Summary of the number of waitstates for the different operations for the memory.

Operation	Waitstates with EDAC Disabled	Waitstates with EDAC Enabled
Read	0 - 1	0 - 2
Word, DWord, 4Word write	0	0
Subword write	0	1 - 2

When EDAC is used, the data is decoded the first cycle after it arrives from the memory and appears on the bus the next cycle if no uncorrectable error is detected. The decoding is done by comparing the stored checksum with a new one which is calculated from the stored data. This decoding is also done during the read phase for a subword write. A so-called syndrome is generated from the comparison between the checksum and it determines the number of errors that occured. One error is automatically corrected and this situation is not visible on the bus. Two or more detected errors cannot be corrected so the operation is aborted and the required two cycle error response is given on the AHB bus (see the AMBA manual for more details). If no errors are detected data is passed through the decoder unaltered.

26.2.3 Read and write diagnostics

As mentioned earlier the memory provides read and write diagnostics when EDAC is enabled. When write diagnostics are enabled, the calculated checksum is not stored in memory during the write phase. Instead, the TCB field from the configuration register is used. In the same manner, if read diagnostics are enabled, the stored checksum from memory is stored in the TCB field during a read (and also during a subword write). This way, the EDAC functionality can be tested during run-time. Note that checkbits are stored in TCB during reads and subword writes even if a multiple error is detected. Also note that the TCB field contains the check bits for a 32-bit word. If the controller has been implemented with support for wider accesses then it is recommended to load and bypass via TCB using only word accesses. For larger write accesses, the contents of TCB will be written as the checksum for all of the words within the larger access. For wide read accesses, the TCB field will hold the check bits for the least significant word.

26.2.4 Error counter

An additional feature is the single error counter which can be enabled with the *errcnten* VHDL generic or by enabling AHB pipeline registers. A single error counter (SEC) field is present in the configuration register, and is incremented each time a single databit error is encountered (reads or subword writes). The number of bits of this counter is 8, set with the *cntbits* VHDL generic. It is accessed through the configuration register. Each counter bit can be reset to zero by writing a one to it. The counter saturates at the value 2^8 - 1 ($2^{cntbits}$ - 1). For each access where single errors are detected the aramo.ce signal will be driven high for one cycle. This signal should be connected to an AHB status register which stores information and generates interrupts (see the AHB Status register documentation for more information). Note that if the maximum supported access size is 32 bits then only one single error can be detected. To support wider access sizes, the core implements several EDAC protected memories with 32-bit data in parallel. This means that a 64- or 128-bit access can trigger multiple single errors. If this happens then the error counter will be incremented with one.

26.2.5 Endianness

The core is designed for big-endian systems.

26.3 Registers

The core is programmed through registers mapped into APB address space.

*Table 287.*FTAHBRAM registers

APB Address offset	Register
0x0	Configuration Register

Table 288. 0x00 - CFG - Configuration Register

31 30	29 28	27 24	23 21	12+8 13	12 10	9	8	7	6 0
DIAG	R	EDACEN	MEMSIZE	SEC	MEMSIZE	WB	RB	EN	TCB
0	0	*		0	*	0	0	0	NR
rw	r	r		wc	r	*	*	*	rw

27 24 Value of edacen VHDL generic.

0: EDAC not implemented
1: Technology agnostic BCH EDAC (traditional FTAHBRAM EDAC)
2: Technology agnostic BCH EDAC, provided by SYNCRAMFT
3: Technology specific EDAC (SECDED)

23: 21 Log2 of the current memory size, bits 3:0 of value. Only used when ahbpupe VHDL generic is non-zero.

12+8: 13 Single error counter (SEC): Incremented each time a single error is corrected (includes errors on checkbits). Each bit can be set to zero by writing a one to it. This feature is only available if the errcnten VHDL generic is set.

12: 10 Log2 of the current memory size, bits 2:0 of value

9 Write Bypass (WB): When set, the TCB field is stored as check bits when a write is performed to the memory.

8 Read Bypass (RB) : When set during a read or subword write, the check bits loaded from memory are stored in the TCB field.

7 EDAC Enable (EN): When set, the EDAC is used otherwise it is bypassed during read and write operations.

If edacen (bits 27:24 of this register) is 2 or 3 then the core always behaves as if it is enabled for write and read timing.

Table 288. 0x00 - CFG - Configuration Register

6: 0 Test Check Bits (TCB) : Used as checkbits when the WB bit is set during writes and loaded with the check bits during a read operation when the RB bit is set.

When the core makes use of technology specific EDAC then the behaviour of error injection is different. The TCB checkbits are propagated to the error injection bits of the SYNCRAMFT entity used within FTAHBRAM when the WB field is set to 1. Normally only one or two bits are used and the type of error injection supported is technology specific and described further in the SYNCRAMFT documentation. The RB field has no effect for technology specific EDAC.

Any unused most significant bits are reserved. Always read as '000...0'.

All fields except TCB are initialised at reset. The EDAC is initally disabled (EN = 0), which also applies to diagnostics fiels (RB and WB are zero).

When available, the single error counter (SEC) field is cleared to zero.

26.4 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x050. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

26.5 Implementation

26.5.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

26.6 Configuration options

Table 289 shows the configuration options of the core (VHDL generics).

*Table 289.*Configuration options

Generic	Function	Allowed range	Default
hindex	Selects which AHB select signal (HSEL) will be used to access the memory.	0 to NAHBMAX-1	0
haddr	ADDR field of the AHB BAR	0 to 16#FFF#	0
hmask	MASK field of the AHB BAR	0 to 16#FFF#	16#FFF#
tech	Memory technology	0 to NTECH	0
kbytes	SRAM size in KiB. The RAM size needs to be a power of two. Otherwise the RAM size will be rounded up to the nearest power of two. For implementations with ahbpipe=1 it is allowed to specify RAM sizes that are of the form 2^x+2^x-1. For example. Specifying a 192 KiB RAM size with ahbpipe = 0 will lead to a 256 KiB RAM area. Specifying a 192 KiB RAM size with ahbpipe = 0 allows a 192 KiB RAM to be implemented. However, specifying a 160 KiB RAM size will still lead to a 192 KiB RAM.	1 to targetdep.	1
pindex	Selects which APB select signal (PSEL) will be used to access the memory configuration registers	0 to NAPBMAX-1	0
paddr	The 12-bit MSB APB address	0 to 16#FFF#	0
pmask	The APB address mask	0 to 16#FFF#	16#FFF#

*Table 289.*Configuration options

Generic	Function	Allowed range	Default
hindex	Selects which AHB select signal (HSEL) will be used to access the memory.	0 to NAHBMAX-1	0
haddr	ADDR field of the AHB BAR	0 to 16#FFF#	0
hmask	MASK field of the AHB BAR	0 to 16#FFF#	16#FFF#
tech	Memory technology	0 to NTECH	0
kbytes	SRAM size in KiB. The RAM size needs to be a power of two. Otherwise the RAM size will be rounded up to the nearest power of two. For implementations with ahbpipe=1 it is allowed to specify RAM sizes that are of the form 2^x+2^x-1. For example. Specifying a 192 KiB RAM size with ahbpipe = 0 will lead to a 256 KiB RAM area. Specifying a 192 KiB RAM size with ahbpipe = 0 allows a 192 KiB RAM to be implemented. However, specifying a 160 KiB RAM size will still lead to a 192 KiB RAM.	1 to targetdep.	1
edacen	Enable and select on-chip EDAC. Must be set to 1 or larger if ahbpipe generic is set to 1. 0: Disabled 1: Technology agnostic BCH EDAC (traditional FTAHBRAM EDAC) 2: Technology agnostic BCH EDAC, provided by SYNCRAMFT 3: Technology specific EDAC (SECDED)	0 to 3	0
autoscrub	Automatically store back corrected data with new check-bits during a read when a single error is detected. Is ignored when edacen is deasserted. This generic must be set to 0 if the ahbpipe generic is set to 1.	0 to 1	0
errcnten	Enables a single error counter. This generic must be set to 1 if the ahbpipe generic is set to 1.	0 to 1	0
cntbits	number of bits in the single error counter. This generic must be set to 8 if the ahbpipe generic is set to 1.	1 to 8	1
ahbpipe	Selects to use FTAHBRAM2 architecture. Adds pipeline registers and requires edacen = 1, autoscrub = 0, errcnten = 1, cntbits = 8.	0 to 1	0
testen	Test enable	0 to 1	0
maccsz	Maximum access size supported by core	32 to 128	AHBDW

26.7 Signal descriptions

Table 290 shows the interface signals of the core (VHDL ports).

*Table 290.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
AHBSI	*	Input	AHB slave input signals	-
AHBSO	*	Output	AHB slave output signals	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
ARAMO	CE	Output	Single error detected	High
MTESTI**	N/A	Input	Memory BIST input signal	-
MTESTO**	N/A	Output	Memory BIST output signal	-
MTESTCLK**	N/A	Input	Memory BIST clock	-

* see GRLIB IP Library User's Manual

** not available in FPGA releases

The aramo.ce signal is normally used to generate interrupts which starts an interrupt routine that corrects errors. Since this is not necessary when autoscrubbing is enabled, aramo.ce should not be connected to an AHB status register or the interrupt should be disabled in the interrupt controller

26.8 Library dependencies

Tabel 291 shows libraries used when instantiating the core (VHDL libraries).

*Table 291.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	MISC	Component	Signals and component declaration

26.9 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
library gaisler;

use grlib.amba.all;
use gaisler.misc.all;

entity ftram_ex is
  port(
    rst : std_ulogic;
    clk : std_ulogic;

    .... --others signals
  );
end;

architecture rtl of ftram_ex is
```

```
--AMBA signals
signal ahbsi : ahb_slv_in_type;
signal ahbso : ahb_slv_out_type;
signal apbi  : apb_slv_in_type;
signal apbo  : apb_slv_out_vector;



--other needed signals here
signal stati   : ahbstat_in_type;
signal aramo   : ahbram_out_type;

begin

--other component instantiations here
...

-- AHB Status Register
  astat0 : ahbstat generic map(pindex => 13, paddr => 13, pirq => 11,
    nftslv => 3)
    port map(rstn, clkm, ahbmi, ahbso, stati, apbi, apbo(13));
    stati.cerror(1 to NAHBSLV-1) <= (others => '0');

--FT AHB RAM
a0 : ftahbram generic map(hindex => 1, haddr => 1, tech => inferred,
  kbytes => 64, pindex => 4, paddr => 4, edacen => 1, autoscrub => 0,
  errcnt => 1, cntbits => 4)
  port map(rst, clk, ahbsi, ahbso(1), apbi, apbo(4), aramo);
  stati.cerror(0) <= aramo.ce;

end architecture;
```

27 FTMCTRL - 8/16/32-bit Memory Controller with EDAC

27.1 Overview

The FTMCTRL combined 8/16/32-bit memory controller provides a bridge between external memory and the AHB bus. The memory controller can handle four types of devices: PROM, asynchronous static ram (SRAM), synchronous dynamic ram (SDRAM) and memory mapped I/O devices (IO). The PROM, SRAM and SDRAM areas can be EDAC-protected using a (39,7) BCH code. The BCH code provides single-error correction and double-error detection for each 32-bit memory word.

The SDRAM area can optionally also be protected using Reed-Solomon coding. In this case a 16-bit checksum is used for each 32-bit word, and any two adjacent 4-bit (nibble) errors can be corrected.

The EDAC capability is determined through a VHDL generic.

The memory controller is configured through three configuration registers accessible via an APB bus interface. The PROM, IO, and SRAM external data bus can be configured in 8-, 16-, or 32-bit mode, depending on application requirements. The controller decodes three address spaces on the AHB bus (PROM, IO, and SRAM/SDRAM). The addresses are determined through VHDL generics. The IO area is marked as non-cacheable in the core's AMBA plug'n'play information record.

External chip-selects are provided for up to four PROM banks, one IO bank, five SRAM banks and two SDRAM banks. Figure 64 below shows how the connection to the different device types is made.

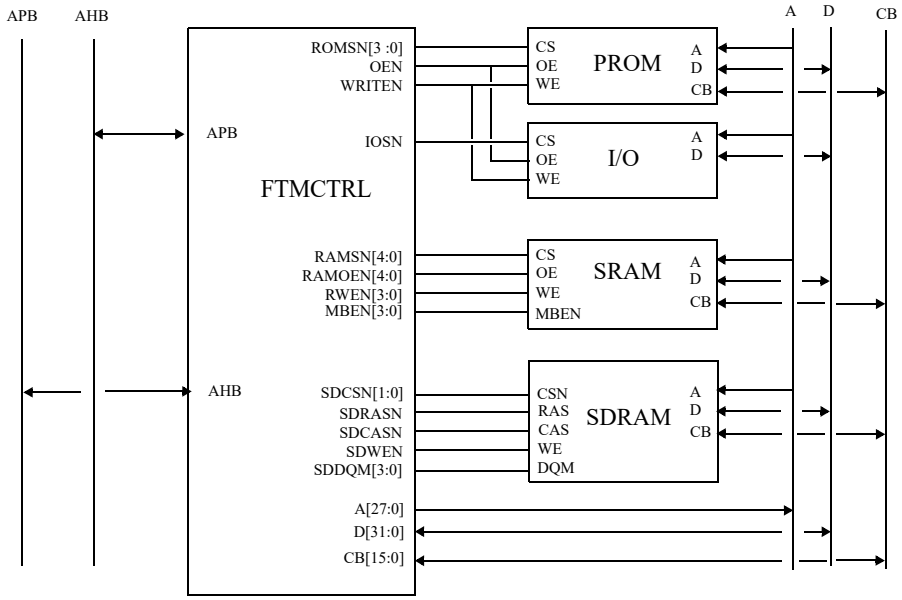


Figure 64. FTMCTRL connected to different types of 32+cb-bit memory devices

27.2 PROM access

Up to four PROM chip-select signals are provided for the PROM area, ROMSN[3:0]. There are two modes: one with two chip-select signals and one with four. The size of the banks can be set in binary steps from 16KiB to 256MiB. If the AHB memory area assigned to the memory controller for PROM accesses is larger than the combined size of the memory banks then the PROM memory area will wrap, starting with the first chip-select being asserted again when accessing addresses higher than the last decoded bank.

A read access to PROM consists of two data cycles and between 0 and 30 waitstates (in the default configuration, see *wsshift* VHDL generic documentation for details). The read data (and optional

EDAC check-bits) are latched on the rising edge of the clock on the last data cycle. On non-consecutive accesses, a idle cycle is placed between the read cycles to prevent bus contention due to slow turn-off time of PROM devices. Figure 65 shows the basic read cycle waveform (zero waitstate) for non-consecutive PROM reads. Note that the address is undefined in the idle cycle. Figure 66 shows the timing for consecutive cycles (zero waitstate). Waitstates are added by extending the data2 phase. This is shown in figure 67 and applies to both consecutive and non-consecutive cycles. Only an even number of waitstates can be assigned to the PROM area.

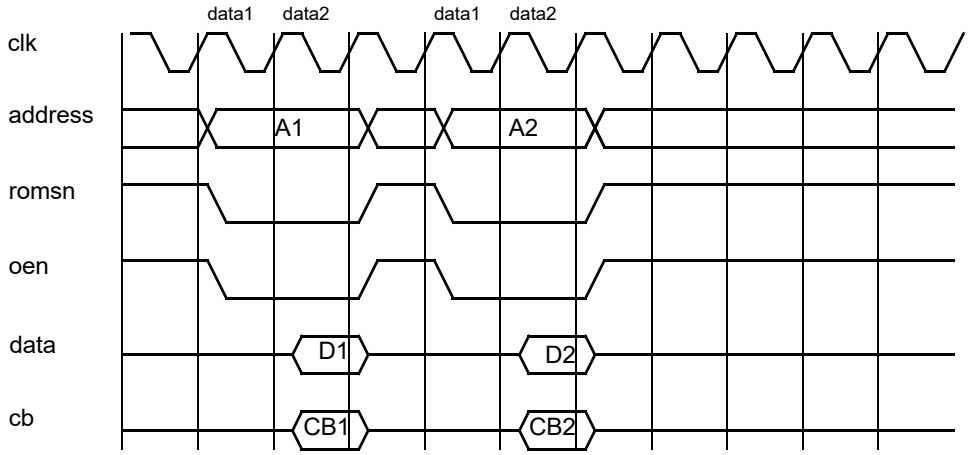


Figure 65. Prom non-consecutive read cyclecs.

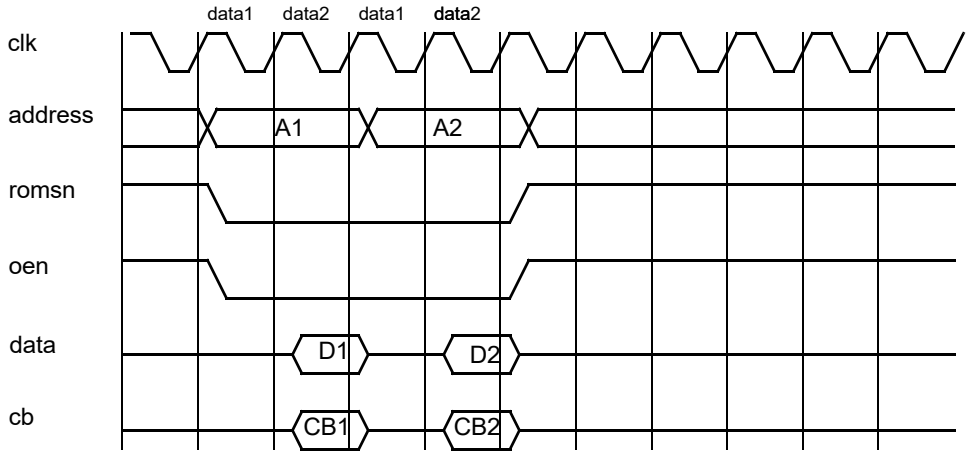


Figure 66. Prom consecutive read cyclecs.

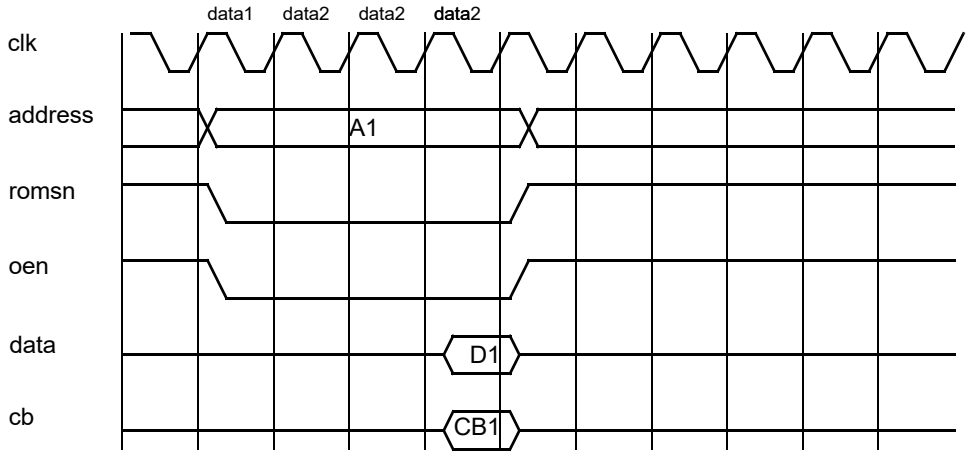


Figure 67. Prom read access with two waitstates.

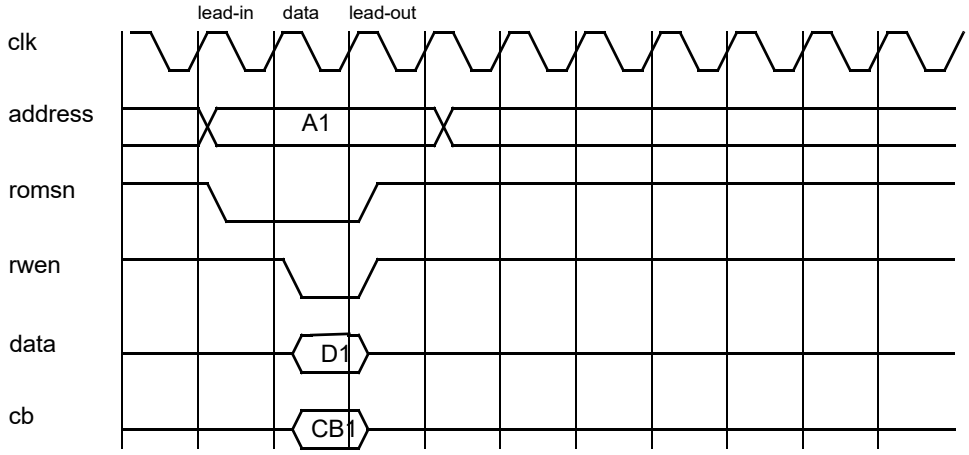


Figure 68. Prom write cycle (0-waitstates)

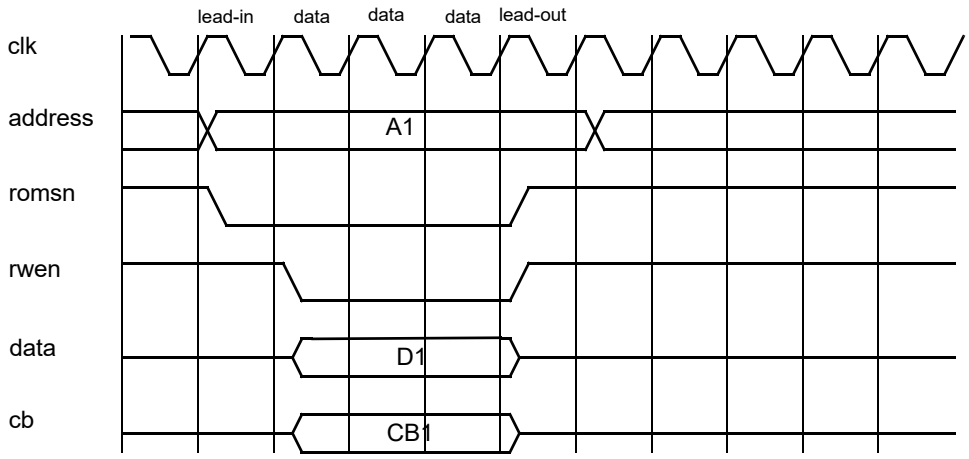


Figure 69. Prom write cycle (2-waitstates)

27.3 Memory mapped IO

Accesses to IO have similar timing as PROM accesses. The IO select (IOSN) and output enable (OEN) signals are delayed one clock to provide stable address before IOSN is asserted. All accesses are performed as non-consecutive accesses as shown in figure 70. The data2 phase is extended when waitstates are added.

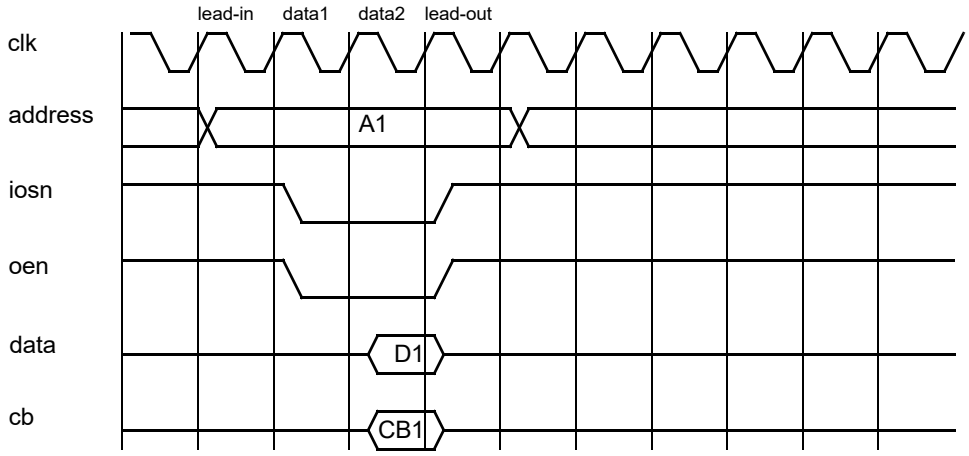


Figure 70. I/O read cycle (0-waitstates)

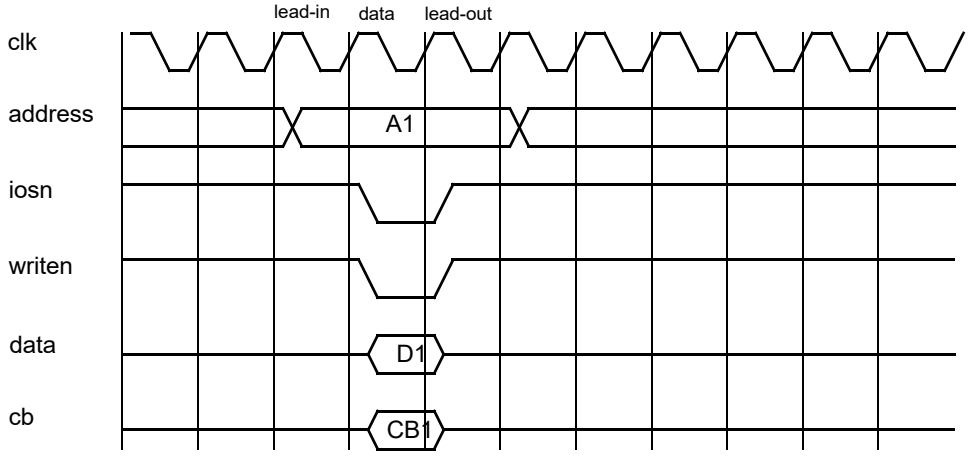


Figure 71. I/O write cycle (0-waitstates)

27.4 SRAM access

The SRAM area is divided on up to five RAM banks. The size of banks 1-4 (RAMSN[3:0]) is programmed in the RAM bank-size field (MCFG2[12:9]) and can be set in binary steps from 8KiB to 256MiB. The fifth bank (RAMSN[4]) decodes the upper 512MiB (controlled by means of the *sdrasel* VHDL generic) and cannot be used simultaneously with SDRAM memory. A read access to SRAM consists of two data cycles and between zero and three waitstates (in the default configuration, see *wsshift* VHDL generic documentation for details). The read data (and optional EDAC check-bits) are latched on the rising edge of the clock on the last data cycle. Accesses to RAMSN[4] can further be stretched by de-asserting BRDYN until the data is available. On non-consecutive accesses, a idle cycle is added after a read cycle to prevent bus contention due to slow turn-off time of memories. Fig-

ure 72 shows the basic read cycle waveform (zero waitstate). Waitstates are added in the same way as for PROM in figure 67.

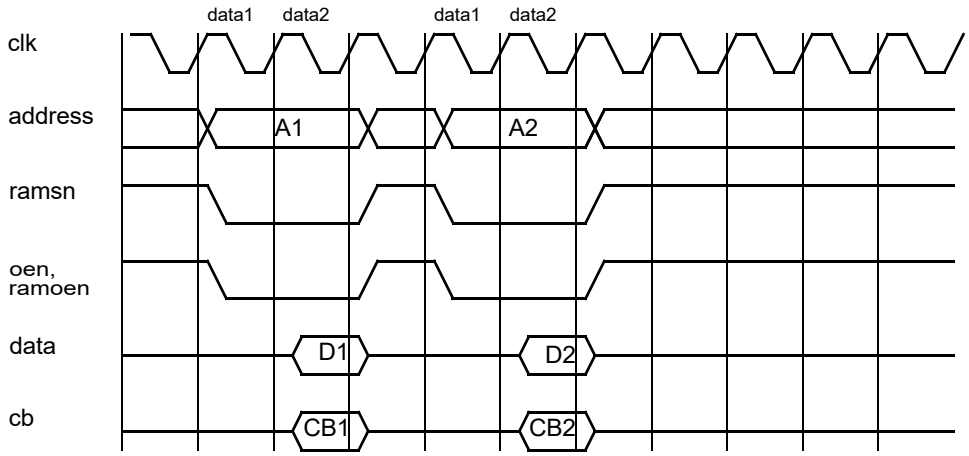


Figure 72. Sram non-consecutive read cyclecs.

For read accesses to RAMSN[4:0], a separate output enable signal (RAMOEN[n]) is provided for each RAM bank and only asserted when that bank is selected. A write access is similar to the read access but takes a minimum of three cycles. Waitstates are added in the same way as for PROM.

Each byte lane has an individual write strobe to allow efficient byte and half-word writes. If the memory uses a common write strobe for the full 16- or 32-bit data, the read-modify-write bit MCFG2 should be set to enable read-modify-write cycles for sub-word writes.

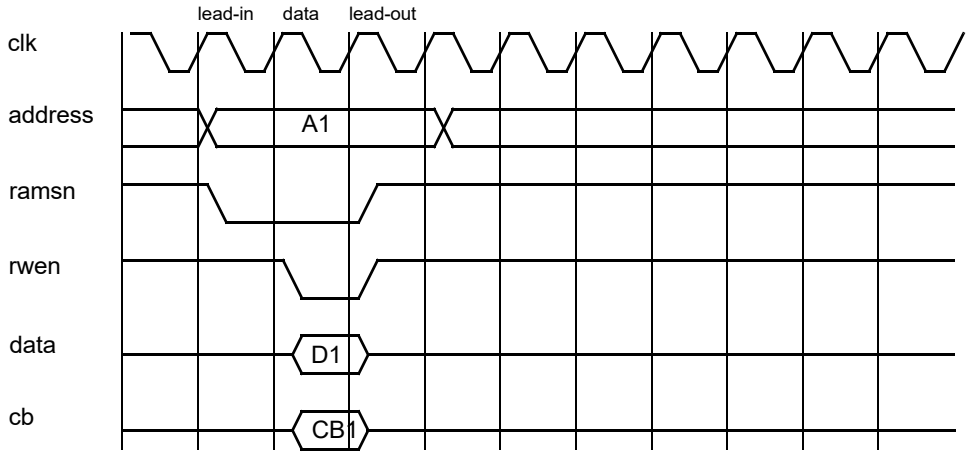


Figure 73. Sram write cycle (0-waitstates)

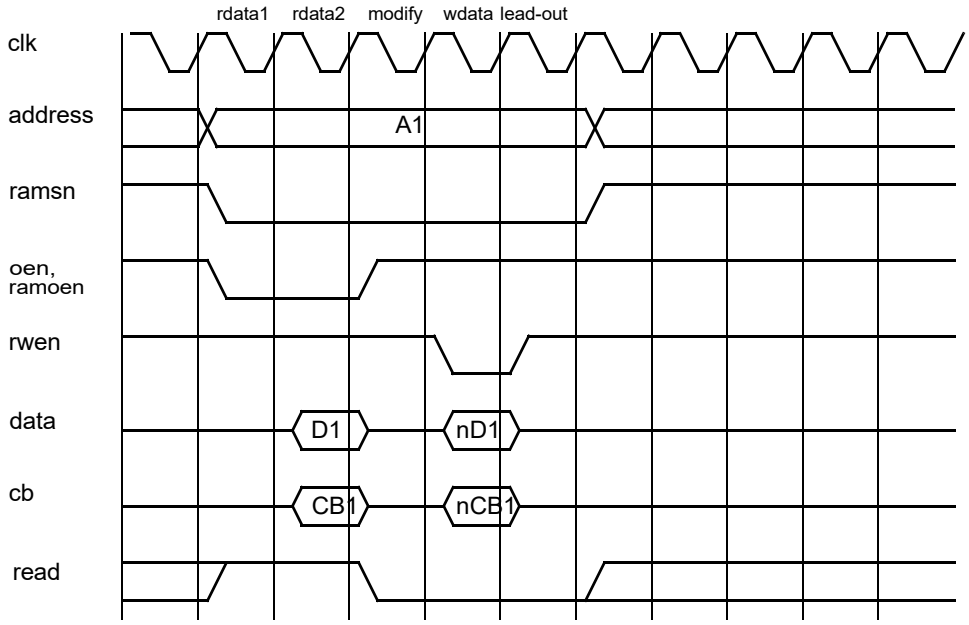


Figure 74. Sram read-modify-write cycle (0-waitstates)

27.5 8-bit and 16-bit PROM and SRAM access

To support applications with low memory and performance requirements efficiently, the SRAM and PROM areas can be individually configured for 8- or 16-bit operation by programming the ROM and RAM width fields in the memory configuration registers. Since reads to memory are always done on 32-bit word basis, read access to 8-bit memory will be transformed in a burst of four read cycles while access to 16-bit memory will generate a burst of two 16-bit reads. During writes, only the necessary bytes will be written. Figure 75 shows an interface example with 8-bit PROM and 8-bit SRAM. Figure 76 shows an example of a 16-bit memory interface.

All possible combinations of width, EDAC, and RMW are not supported. The supported combinations are given in table 292, and the behavior of setting an unsupported combination is undefined. It is not allowed to set the ROM or RAM width fields to 8-bit or 16-bit width if the core does not implement support for these widths.

*Table 292.*FTMCTRL supported SRAM and PROM configurations

PROM/SRAM bus width	RWEN resolution (SRAM)	EDAC	RMW bit (SRAM)	Core configuration
8	Bus width	None	0	8-bit support
8	Bus width	BCH	1	8-bit support, EDAC
16	Byte	None	0	16-bit support
16	Bus width	None	1	16-bit support
32	Byte	None	0	
32	Bus width	None	1	
32+7	Bus width	BCH	1	EDAC support

8-bit width support is set with *ram8* VHDL generic and 16-bit width support is set with *ram16* VHDL genericis.

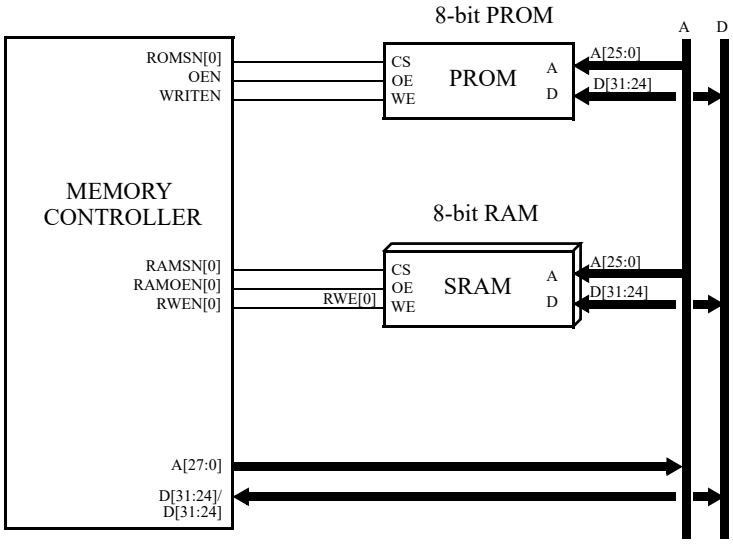


Figure 75. 8-bit memory interface example

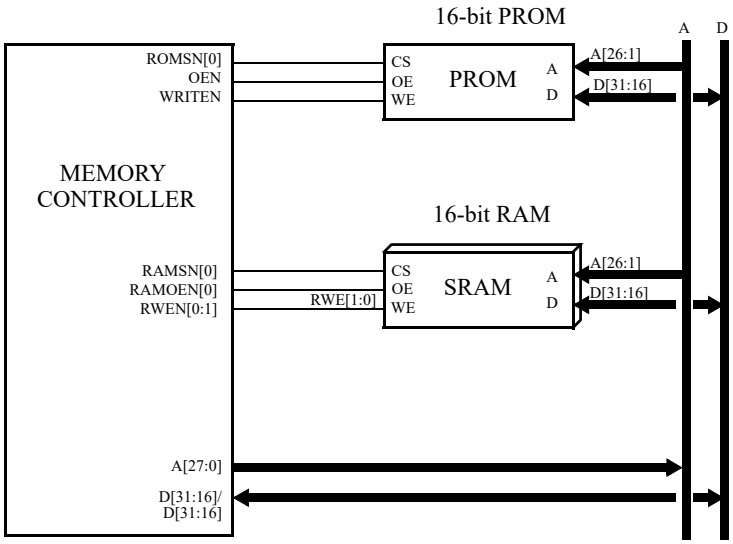


Figure 76. 16-bit memory interface example

In 8-bit mode, the PROM/SRAM devices should be connected to the MSB byte of the data bus (D[31:24]). The LSB address bus should be used for addressing (A[25:0]). In 16-bit mode, D[31:16] should be used as data bus, and A[26:1] as address bus.

27.6 8- and 16-bit I/O access

Similar to the PROM/SRAM areas, the IO area can also be configured to 8- or 16-bits mode. However, the I/O device will NOT be accessed by multiple 8/16 bits accesses as the memory areas, but only with one single access just as in 32-bit mode. To access an IO device on an 8-bit bus, only byte accesses should be used (LDUB/STB instructions for the CPU). To accesses an IO device on a 16-bit bus, only halfword accesses should be used (LDUH/STH instructions for the CPU).

To access the I/O-area in 8- or 16-bit mode, *ram8* VHDL generic or *ram16* VHDL generic must be set respectively.

27.7 Burst cycles

To improve the bandwidth of the memory bus, accesses to consecutive addresses can be performed in burst mode. Burst transfers will be generated when the memory controller is accessed using an AHB burst request. These includes instruction cache-line fills, double loads and double stores. The timing of a burst cycle is identical to the programmed basic cycle with the exception that during read cycles, the idle cycle will only occurs after the last transfer. Burst cycles will not be generated to the IO area.

Only word (HSIZE = “010”) bursts of incremental type (HBURST=INCR, INCR4, INCR8 or INCR16) are supported.

27.8 SDRAM access

27.8.1 General

Synchronous dynamic RAM (SDRAM) access is supported to two banks of PC100/PC133 compatible devices. This is implemented by a special version of the SDCTRL SDRAM controller core from Cobham Gaisler, which is optionally instantiated as a sub-block. The SDRAM controller supports 64M, 256M and 512M devices with 8 - 12 column-address bits, and up to 13 row-address bits. The size of the two banks can be programmed in binary steps between 4MiB and 512MiB. The operation of the SDRAM controller is controlled through MCFG2 and MCFG3 (see below). Both 32- and 64-bit data bus width is supported, allowing the interface of 64-bit DIMM modules. The memory controller can be configured to use either a shared or separate bus connecting the controller and SDRAM devices.

27.8.2 Address mapping

The two SDRAM chip-select signals are decoded. SDRAM area is mapped into the upper half of the RAM area defined by BAR2 register, and cannot be used simultaneously with fifth SRAM bank (RAMSN[4]). When the SDRAM enable bit is set in MCFG2, the controller is enabled and mapped into upper half of the RAM area as long as the SRAM disable bit is not set. If the SRAM disable bit is set, all access to SRAM is disabled and the SDRAM banks are mapped into the lower half of the RAM area.

27.8.3 Initialisation

When the SDRAM controller is enabled, it automatically performs the SDRAM initialisation sequence of PRECHARGE, 8x AUTO-REFRESH and LOAD-MODE-REG on both banks simultaneously. The controller programs the SDRAM to use single location access on write. The controller programs the SDRAM to use line burst of length 8 when *pageburst* VHDL generic is 0. The controller programs the SDRAM to use page burst when *pageburst* VHDL generic is 1. The controller programs the SDRAM to use page burst or line burst of length 8, selectable via the MCFG2 register, when *pageburst* VHDL generic is 2.

27.8.4 Configurable SDRAM timing parameters

To provide optimum access cycles for different SDRAM devices (and at different frequencies), three SDRAM parameters can be programmed through memory configuration register 2 (MCFG2): TCAS, TRP and TRFCD. The value of these field affects the SDRAM timing as described in table 293.

*Table 293.*SDRAM programmable minimum timing parameters

SDRAM timing parameter	Minimum timing (clocks)
CAS latency, RAS/CAS delay (t_{CAS}, t_{RCD})	TCAS + 2
Precharge to activate (t_{RP})	TRP + 2
Auto-refresh command period (t_{RFC})	TRFC + 3
Activate to precharge (t_{RAS})	TRFC + 1
Activate to Activate (t_{RC})	TRP + TRFC + 4

If the TCAS, TRP and TRFC are programmed such that the PC100/133 specifications are fulfilled, the remaining SDRAM timing parameters will also be met. The table below shows typical settings for 100 and 133 MHz operation and the resulting SDRAM timing (in ns):

*Table 294.*SDRAM example programming

SDRAM settings	t_{CAS}	t_{RC}	t_{RP}	t_{RFC}	t_{RAS}
100 MHz, CL=2; TRP=0, TCAS=0, TRFC=4	20	80	20	70	50
100 MHz, CL=3; TRP=0, TCAS=1, TRFC=4	30	80	20	70	50
133 MHz, CL=2; TRP=1, TCAS=0, TRFC=6	15	82	22	67	52
133 MHz, CL=3; TRP=1, TCAS=1, TRFC=6	22	82	22	67	52

27.8.5 Refresh

The SDRAM controller contains a refresh function that periodically issues an AUTO-REFRESH command to both SDRAM banks. The period between the commands (in clock periods) is programmed in the refresh counter reload field in the MCFG3 register. Depending on SDRAM type, the required period is typically 7.8 or 15.6 µs (corresponding to 780 or 1560 clocks at 100 MHz). The generated refresh period is calculated as (reload value+1)/sysclk. The refresh function is enabled by setting bit 31 in MCFG2.

27.8.6 SDRAM commands

The controller can issue three SDRAM commands by writing to the SDRAM command field in MCFG2: PRE-CHARGE, AUTO-REFRESH and LOAD-MODE-REG (LMR). If the LMR command is issued, the CAS delay as programmed in MCFG2 will be used. Line burst of length 8 will be set for read when *pageburst* VHDL generic is 0. Page burst will be set for read when *pageburst* VHDL generic is 1. Page burst or line burst of length 8, selectable via the MCFG2 register will be set, when *pageburst* VHDL generic is 2. Remaining fields are fixed: single location write, sequential burst. The command field will be cleared after a command has been executed. When changing the value of the CAS delay, a LOAD-MODE-REGISTER command should be generated at the same time. NOTE: when issuing SDRAM commands, the SDRAM refresh must be disabled.

27.8.7 Read cycles

A read cycle is started by performing an ACTIVATE command to the desired bank and row, followed by a READ command after the programmed CAS delay. A read burst is performed if a burst access has been requested on the AHB bus. The read cycle is terminated with a PRE-CHARGE command, no banks are left open between two accesses.

27.8.8 Write cycles

Write cycles are performed similarly to read cycles, with the difference that WRITE commands are issued after activation. A write burst on the AHB bus will generate a burst of write commands without idle cycles in-between.

After the WRITE command has completed, if there is an immediately following read or write access (not RMW) to the same 1KiB page on the AHB bus, this access is performed during the same access cycle without closing and re-opening the row.

27.8.9 Read-modify-write cycles

If EDAC is enabled and a byte or half-word write is performed, the controller will perform a read-modify-write cycle to update the checkbits correctly. This is done by performing an ACTIVATE command, followed by READ, WRITE and PRE-CHARGE. The write command interrupts the read burst and the data mask signals will be raised two cycles before this happens as required by the SDRAM standard.

27.8.10 Address bus

The memory controller can be configured to either share the address and data buses with the SRAM, or to use separate address and data buses. When the buses are shared, the address bus of the SDRAMs should be connected to A[14:2], the bank address to A[16:15]. The MSB part of A[14:2] can be left unconnected if not used. When separate buses are used, the SDRAM address bus should be connected to SA[12:0] and the bank address to SA[14:13].

27.8.11 Data bus

SDRAM can be connected to the memory controller through the common or separate data bus. If the separate bus is used the width is configurable to 32 or 64 bits. 64-bit data bus allows the 64-bit SDRAM devices to be connected using the full data capacity of the devices. 64-bit SDRAM devices can be connected to 32-bit data bus if 64-bit data bus is not available but in this case only half the full data capacity will be used. There is a drive signal vector and separate data vector available for SDRAM. The drive vector has one drive signal for each data bit. These signals can be used to remove timing problems with the output delay when a separate SDRAM bus is used.

27.8.12 Clocking

The SDRAM controller is designed for an external SDRAM clock that is in phase or slightly earlier than the internal AHB clock. This provides the maximum margin for setup and hold on the external signals, and allows highest possible frequency. For Xilinx and Altera device, the GRLIB Clock Generator (CLKGEN) can be configured to produce a properly synchronized SDRAM clock. For other FPGA targets, the custom clock synchronization must be designed. For ASIC targets, the SDRAM clock can be derived from the AHB clock with proper delay adjustments during place&route.

27.8.13 Initialisation

Each time the SDRAM is enabled (bit 14 in MCFG2), an SDRAM initialisation sequence will be sent to both SDRAM banks. The sequence consists of one PRECHARGE, eight AUTO-REFRESH and one LOAD-COMMAND-REGISTER command.

27.9 Memory EDAC

27.9.1 BCH EDAC

The FTMCTRL is provided with an BCH EDAC that can correct one error and detect two errors in a 32-bit word. For each word, a 7-bit checksum is generated according to the equations below. A cor-

rectable error will be handled transparently by the memory controller, but adding one waitstate to the access. If an un-correctable error (double-error) is detected, the current AHB cycle will end with an error response. The EDAC can be used during access to PROM, SRAM and SDRAM areas by setting the corresponding EDAC enable bits in the MCFG3 register. The equations below show how the EDAC checkbits are generated:

```
CB0 = D0 ^ D4 ^ D6 ^ D7 ^ D8 ^ D9 ^ D11 ^ D14 ^ D17 ^ D18 ^ D19 ^ D21 ^ D26 ^ D28 ^ D29 ^ D31
CB1 = D0 ^ D1 ^ D2 ^ D4 ^ D6 ^ D8 ^ D10 ^ D12 ^ D16 ^ D17 ^ D18 ^ D20 ^ D22 ^ D24 ^ D26 ^ D28
CB2 = D0 ^ D3 ^ D4 ^ D7 ^ D9 ^ D10 ^ D13 ^ D15 ^ D16 ^ D19 ^ D20 ^ D23 ^ D25 ^ D26 ^ D29 ^ D31
CB3 = D0 ^ D1 ^ D5 ^ D6 ^ D7 ^ D11 ^ D12 ^ D13 ^ D16 ^ D17 ^ D21 ^ D22 ^ D23 ^ D27 ^ D28 ^ D29
CB4 = D2 ^ D3 ^ D4 ^ D5 ^ D6 ^ D7 ^ D14 ^ D15 ^ D18 ^ D19 ^ D20 ^ D21 ^ D22 ^ D23 ^ D30 ^ D31
CB5 = D8 ^ D9 ^ D10 ^ D11 ^ D12 ^ D13 ^ D14 ^ D15 ^ D24 ^ D25 ^ D26 ^ D27 ^ D28 ^ D29 ^ D30 ^ D31
CB6 = D0 ^ D1 ^ D2 ^ D3 ^ D4 ^ D5 ^ D6 ^ D7 ^ D24 ^ D25 ^ D26 ^ D27 ^ D28 ^ D29 ^ D30 ^ D31
```

If the SRAM is configured in 8-bit mode, the EDAC checkbit bus (CB[7:0]) is not used but it is still possible to use EDAC protection. Data is always accessed as words (4 bytes at a time) and the corresponding checkbits are located at the address acquired by inverting the word address (bits 2 to 27) and using it as a byte address. The same chip-select is kept active. A word written as four bytes to addresses 0, 1, 2, 3 will have its checkbits at address 0xFFFFFFF, addresses 4, 5, 6, 7 at 0xFFFFFFE and so on. All the bits up to the maximum bank size will be inverted while the same chip-select is always asserted. This way all the bank sizes can be supported and no memory will be unused (except for a maximum of 4 byte in the gap between the data and checkbit area). A read access will automatically read the four data bytes individually from the nominal addresses and the EDAC checkbit byte from the top part of the bank. A write cycle is performed the same way. Byte or half-word write accesses will result in an automatic read-modify-write access where 4 data bytes and the checkbit byte are firstly read, and then 4 data bytes and the newly calculated checkbit byte are writen back to the memory. This 8-bit mode applies to SRAM while SDRAM always uses 32-bit accesses. The size of the memory bank is determined from the settings in MCFG2. The EDAC cannot be used on memory areas configured in 16-bit mode.

If the ROM is configured in 8-bit mode, EDAC protection is provided in a similar way as for the SRAM memory described above. The difference is that write accesses are not being handled automatically. Instead, write accesses must only be performed as individual byte accesses by the software, writing one byte at a time, and the corresponding checkbit byte must be calculated and be written to the correct location by the software.

NOTE: when the EDAC is enabled in 8-bit bus mode, only the first bank select (RAMSN[0], PROMSN[0]) can be used.

The operation of the EDAC can be tested trough the MCFG3 register. If the WB (write bypass) bit is set, the value in the TCB field will replace the normal checkbits during memory write cycles. If the RB (read bypass) is set, the memory checkbits of the loaded data will be stored in the TCB field during memory read cycles. NOTE: when the EDAC is enabled, the RMW bit in memory configuration register 2 must be set.

Data access timing with EDAC enabled is identical to access without EDAC, if the *edac* VHDL generic is set to 1. To improve timing of the HREADY output, a pipeline stage can be inserted in the EDAC error detection by setting the *edac* VHDL generic to 2. One clock extra latency will then occur on single word reads, or on the first data word in a burst.

EDAC is not supported for 64-bit wide SDRAM data buses.

27.9.2 Reed-Solomon EDAC

The Reed-Solomon EDAC provides block error correction, and is capable of correcting up to two 4-bit nibble errors in a 32-bit data word or 16-bit checksum. The Reed-Solomon EDAC can be enabled for the SDRAM area only, and uses a 16-bit checksum. Operation and timing is identical to the BCH EDAC with the pipeline option enabled. The Reed-Solomon EDAC is enabled by setting the RSE and

RE bits in MCFG3, and the RMW bit in MCFG2. The Reed-Solomon EDAC is not supported for 64-bit wide SDRAM buses.

The Reed-Solomon data symbols are 4-bit wide, represented as GF(2^4). The basic Reed-Solomon code is a shortened RS(15, 13, 2) code, represented as RS(6, 4, 2). It has the capability to detect and correct a single symbol error anywhere in the codeword. The EDAC implements an interleaved RS(6, 4, 2) code where the overall data is represented as 32 bits and the overall checksum is represented as 16 bits. The codewords are interleaved nibble-wise. The interleaved code can correct two 4-bit errors when each error is located in a nibble and not in the same original RS(6, 4, 2) codeword.

The Reed-Solomon RS(15, 13, 2) code has the following definition:

- there are 4 bits per symbol;
- there are 15 symbols per codeword;
- the code is systematic;
- the code can correct one symbol error per codeword;
- the field polynomial is

$$f(x) = x^4 + x + 1$$

- the code generator polynomial is

$$g(x) = \prod_{i=0}^{1} (x + \alpha^i) = \sum_{j=0}^{2} g_j \cdot x^j$$

  for which the highest power of x is stored first;
- a codeword is defined as 15 symbols:

  $c_0, c_1, c_2, c_3, c_4, c_5, c_6, c_7, c_8, c_9, c_{10}, c_{11}, c_{12}, c_{13}, c_{14}$

  where c_0 to c_{12} represent information symbols and c_{13} to c_{14} represent check symbols.

The shortened and interleaved RS(6, 4, 2) code has the following definition:

- the codeword length is shortened to 4 information symbols and 2 check symbols and as follows:

  $c_0 = c_1 = c_2 = c_3 = c_4 = c_5 = c_6 = c_7 = c_8 = 0$

  where the above information symbols are suppressed or virtually filled with zeros;
- two codewords are interleaved (i.e. interleaved depth I=2) with the following mapping to the 32-bit data and 16-bit checksum, were $c_{i,j}$ is a symbol with codeword index i and symbol index j:

  $c_{0,9}$ = sd[31:28]

  $c_{1,9}$ = sd[27:24]

  $c_{0,10}$ = sd[23:20]

  $c_{1,10}$ = sd[19:16]

  $c_{0,11}$ = sd[15:12]

  $c_{1,11}$ = sd[11:8]

  $c_{0,12}$ = sd[7:4]

  $c_{1,12}$ = sd[3:0]

  $c_{0,13}$ = scb[15:12]

  $c_{1,13}$ = scb[11:8]

$c_{0,14}$ = scb[7:4]

$c_{1,14}$ = scb[3:0]

where SD[ ] is interchanable with DATA[] and SCB[ ] is interchangable with CB[ ]

Note that the FTMCTRL must have the *edac* VHDL generic set to 3 to enable the RS EDAC functionality. The Reed-Solomon EDAC is not supported for 64-bit wide SDRAM buses.

27.9.3 EDAC Error reporting

As mentioned above an un-correctable error results in an AHB error response which can be monitored on the bus. Correctable errors however are handled transparently and are not visible on the AHB bus. A sideband signal is provided which is asserted during one clock cycle for each access for which a correctable error is detected. This can be used for providing an external scrubbing mechanism and/or statistics. The correctable error signal is most commonly connected to the AHB status register which monitors both this signal and error responses on the bus. Please see the AHB status register section for more information.

27.10 Bus Ready signalling

The BRDYN signal can be used to stretch all types of access cycles to the PROM, I/O area and the SRAM area decoded by RAMSN[4]. This covers read and write accesses in general, and additionally read-modify-write accesses to the SRAM area. The accesses will always have at least the pre-programmed number of waitstates as defined in memory configuration registers 1 & 2, but will be further stretched until BRDYN is asserted. BRDYN should be asserted in the cycle preceding the last one. If bit 29 in MCFG1 is set, BRDYN can be asserted asynchronously with the system clock. In this case, the read data must be kept stable until the de-assertion of OEN/RAMOEN and BRDYN must be asserted for at least 1.5 clock cycle. The use of BRDYN can be enabled separately for the PROM, I/O and RAMSN[4] areas. It is recommended that BRDYN is asserted until the corresponding chip select signal is de-asserted, to ensure that the access has been properly completed and avoiding the system to stall.

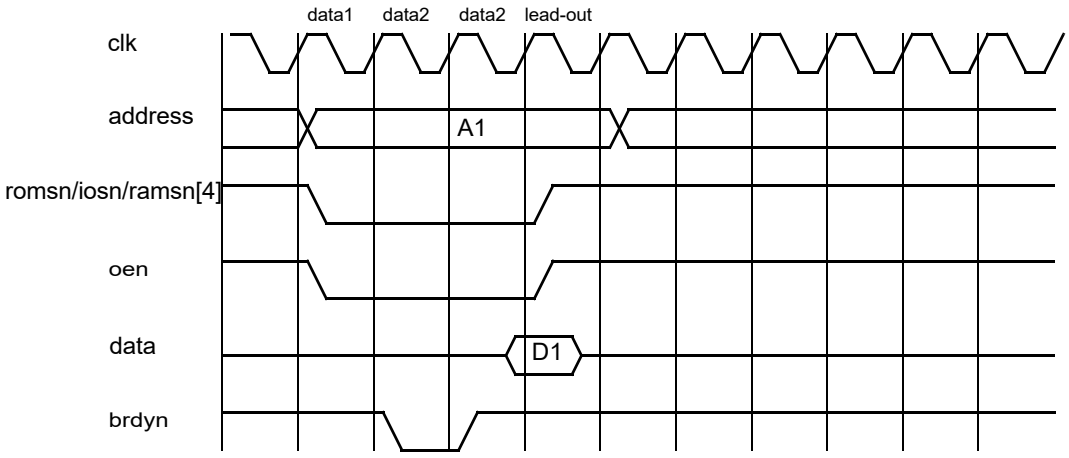


Figure 77. READ cycle with one extra data2 cycle added with BRDYN (synchronous sampling). Lead-out cycle is only applicable for I/O accesses.

Figure 78 shows the use of BRDYN with asynchronous sampling. BRDYN is kept asserted for more than 1.5 clock-cycle. Two synchronization registers are used so it will take at least one additional cycle from when BRDYN is first asserted until it is visible internally. In figure 78 one cycle is added to the data2 phase.

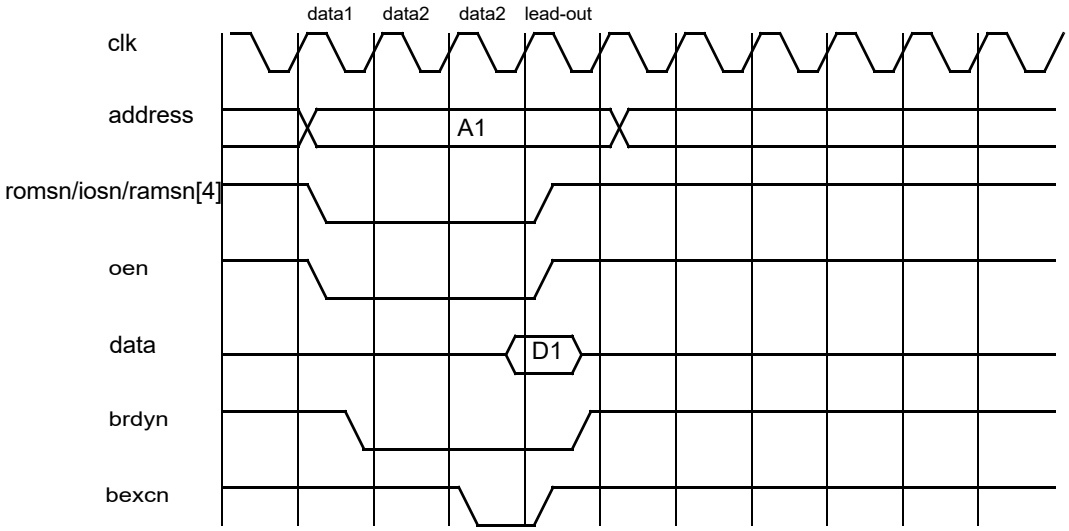


Figure 78. BRDYN (asynchronous) sampling and BEXCN timing. Lead-out cycle is only applicable for I/O-accesses.

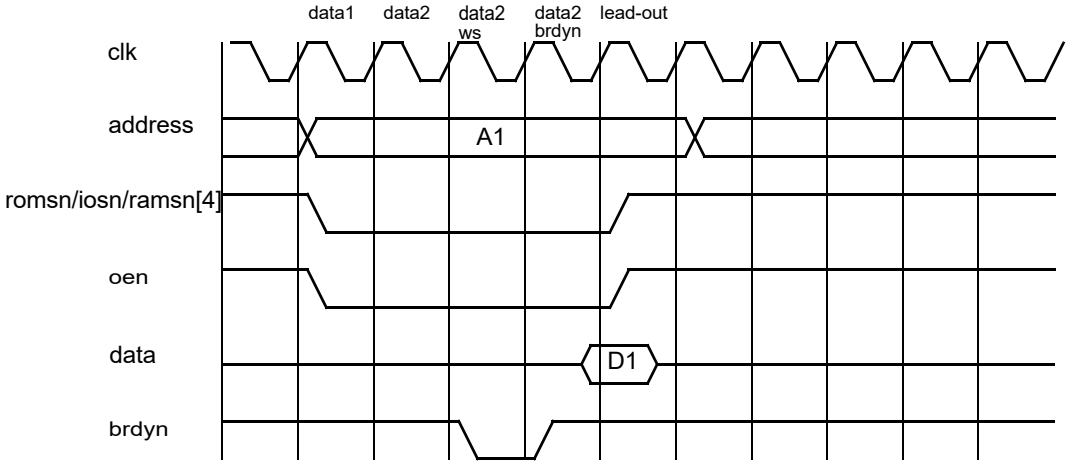


Figure 79. Read cycle with one waitstate (configured) and one BRDYN generated waitstate (synchronous sampling).

If burst accesses and BRDYN signaling are to be used together, special care needs to be taken to make sure BRDYN is raised between the separate accesses of the burst. The controller does not raise the select and OEN signal (in the read case) between accesses during the burst so if BRDYN is kept asserted until the select signal is raised, all remaining accesses in the burst will finish with the configured fixed number of wait states.

The core can optionally be implemented with a bus ready timeout counter. The counter value and counter reload value are then available in MCFG7. The counter will be reloaded whenever the bus ready signal is low (asserted). If the reload value is nonzero, then the counter will decrement with one each clock cycle the core is waiting for bus ready to be asserted. If the counter reaches zero, the action taken depends on the state of Bus Error Enable (BEXCN) in MCFG1. If BEXCN is ‘1’, then an AMBA ERROR response will be generated and the counter will be reloaded. If BEXCN is ‘0’, then the bus ready enable for the accessed memory area will be disabled and the core will ignore bus ready for the accessed area.

Bus ready timeout functionality is disabled when the bus ready counter reload value is zero (MCFG7.BRDYCNTRLD = 0).

27.11 Access errors

An access error can be signalled by asserting the BEXCN signal for read and write accesses. For reads it is sampled together with the read data. For writes it is sampled on the last rising edge before chip select is de-asserted, which is controlled by means of waitstates or bus ready signalling. If the usage of BEXCN is enabled in memory configuration register 1, an error response will be generated on the internal AHB bus. BEXCN can be enabled or disabled through memory configuration register 1, and is active for all areas (PROM, IO and RAM). BEXCN is only sampled in the last access for 8- and 16-bit mode for RAM and PROM. That is, when four bytes are written for a word access to 8-bit wide memory BEXCN is only sampled in the last access with the same timing as a single access in 32-bit mode.

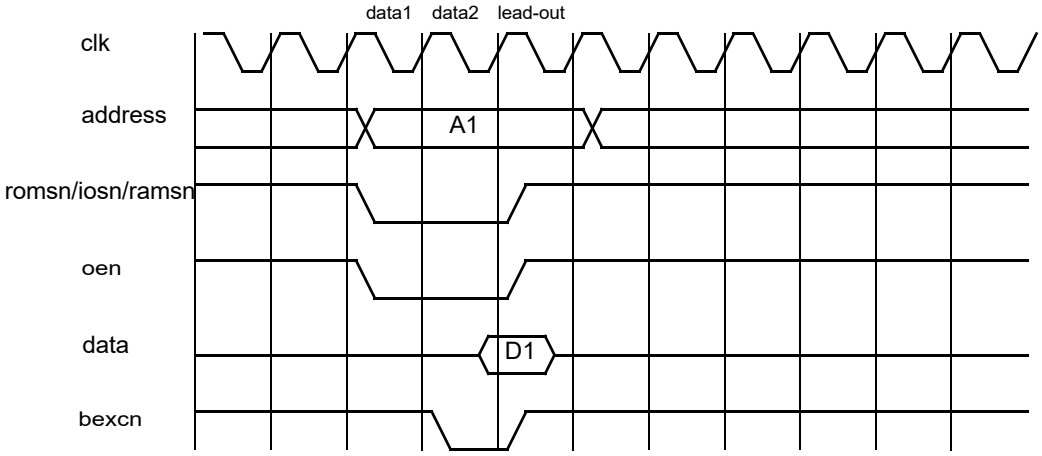


Figure 80. Read cycle with BEXCN.

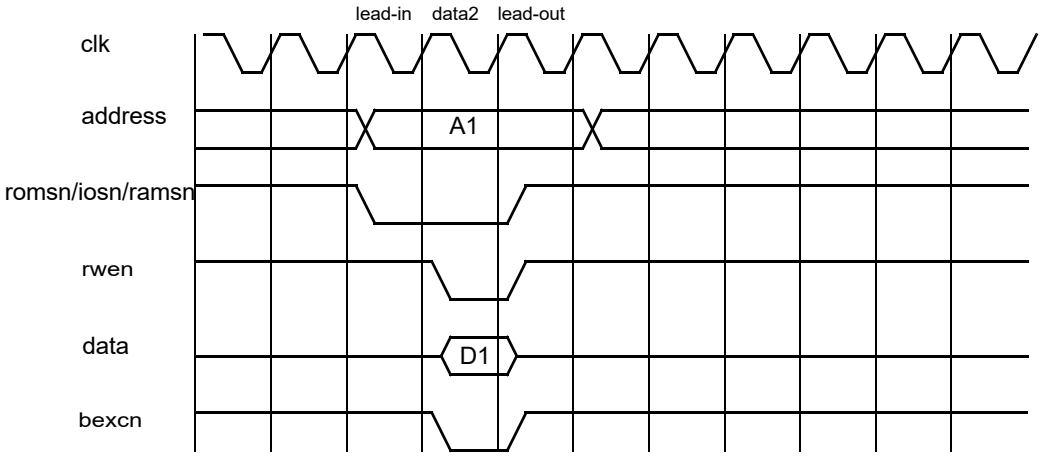


Figure 81. Write cycle with BEXCN. Chip-select (iosn) is not asserted in lead-in cycle for io-accesses.

27.12 Attaching an external DRAM controller

To attach an external DRAM controller, RAMSN[4] should be used since it allows the cycle time to vary through the use of BRDYN. In this way, delays can be inserted as required for opening of banks and refresh.

27.13 Output enable timing

A drive signal vector for the data I/O-pads is provided which has one drive signal for each data bit. It can be used if the synthesis tool does not generate separate registers automatically for the current technology. This can remove timing problems with output delay. An additional vector is used for the separate SDRAM bus.

27.14 Read strobe

The READ signal indicates the direction of the current PROM,SRAM,IO or SDRAM transfer, and it can be used to drive external bi-directional buffers on the data bus. It always is valid at least one cycle before and after the bus is driven, at other times it is held either constant high or low.

27.15 Endianness

The core is designed for big-endian systems.

27.16 Registers

The core is programmed through registers mapped into APB address space.

*Table 295.*FTMCTRL memory controller registers

APB Address offset	Register
0x0	Memory configuration register 1 (MCFG1)
0x4	Memory configuration register 2 (MCFG2)
0x8	Memory configuration register 3 (MCFG3)
0xC	Memory configuration register 4 (MCFG4)
0x10	Memory configuration register 5 (MCFG5)
0x14	Memory configuration register 6 (MCFG6)
0x18	Memory configuration register 7 (MCFG7)

27.16.1 Memory configuration register 1 (MCFG1)

Memory configuration register 1 is used to program the timing of rom and IO accesses.

*Table 296.*0x00 - MCFG1 - Memory configuration register 1

31	30	29	28	27	26	25	24	23 20	19	18	17
	PBRDY	ABRDY	IOBUSW		IBRDY	BEXCN		IO WAITSTATES	IOEN	R	ROMBANKSZ
	0	0	NR		0	0	0	0x00	0	0	0x0
	rw	rw	rw		rw	rw	r	rw	rw	r	rw

14	13 12	11	10	9 8	7 4	3 0
ROMANKS7	RESERVED	PWEN	RES	PROM WIDTH	PROM WRITE WS	PROM READ WS
	0	0	0	*	0xE	0xE
rw	r	rw	r	rw	rw	rw

31 RESERVED

30 PROM area bus ready enable (PBRDY) - Enables bus ready (BRDYN) signalling for the PROM area. Reset to ‘0’.

29 Asynchronous bus ready (ABRDY) - Enables asynchronous bus ready.

28 : 27 I/O bus width (IOBUSW) - Sets the data width of the I/O area (“00”=8, “01”=16, “10” =32).

26 I/O bus ready enable (IBRDY) - Enables bus ready (BRDYN) signalling for the I/O area. Reset to ‘0’.

25 Bus error enable (BEXCN) - Enables bus error signalling for all areas. Reset to ‘0’.

24 RESERVED

*Table 296.*0x00 - MCFG1 - Memory configuration register 1

23 : 20 I/O waitstates (IO WAITSTATES) - Sets the number of waitstates during I/O accesses (“0000”=0, “0001”=1, “0010”=2,..., “1111”=15).
The values above describe the default configuration The core can be configred at implementation to extend the number of waitstates. The number of wait states inserted will be (IO WAITSTATES)*$2^{wsshift}$, where *wsshift* can be read from the first user-defined register in the core’s plug&play area (default is wsshift = 0).

19 I/O enable (IOEN) - Enables accesses to the memory bus I/O area.

18 RESERVED

17: 14 PROM bank size (ROMBANKSZ) - Returns current PROM bank size when read. “0000” is a special case and corresponds to a bank size of 256MiB. All other values give the bank size in binary steps: “0001”=16KiB, “0010”=32KiB, “0011”=64KiB,... , “1111”=256MiB (i.e. 8KiB * 2**ROMBANKSZ). For value “0000” or “1111” only two chip selects are available. For other values, two chip select signals are available for fixed bank sizes. For other values, four chip select signals are available for programmable bank sizes.

Programmable bank sizes can be changed by writing to this register field. The written values correspond to the bank sizes and number of chip-selects as above. Reset to “0000” when programmable.

Programmable ROMBANKSZ is only available when romasel VHDL generic is 0. For other values this is a read-only register field containing the fixed bank size value.

13:12 RESERVED

11 PROM write enable (PWEN) - Enables write cycles to the PROM area.

10 RESERVED

9 : 8 PROM width (PROM WIDTH) - Sets the data width of the PROM area (“00”=8, “01”=16, “10”=32).

7 : 4 PROM write waitstates (PROM WRITE WS) - Sets the number of wait states for PROM write cycles (“0000”=0, “0001”=2, “0010”=4,..., “1111”=30).

The values above describe the default configuration The core can be configred at implementation to extend the number of waitstates. The number of wait states inserted will be (PROM WRITE WS)*2*$2^{wsshift}$, where *wsshift* can be read from the first user-defined register in the core’s plug&play area (default is wsshift = 0).

3 : 0 PROM read waitstates (PROM READ WS) - Sets the number of wait states for PROM read cycles (“0000”=0, “0001”=2, “0010”=4,...,”1111”=30). Reset to “1111”.

The values above describe the default configuration The core can be configred at implementation to extend the number of waitstates. The number of wait states inserted will be (PROM READ WS)*2*$2^{wsshift}$, where *wsshift* can be read from the first user-defined register in the core’s plug&play area (default is wsshift = 0).

During reset, the prom width (bits [9:8]) are set with value on BWIDTH inputs. The prom waitstates fields are set to 15 (maximum). External bus error and bus ready are disabled. All other fields are undefined.

27.16.2 Memory configuration register 2 (MCFG2)

Memory configuration register 2 is used to control the timing of the SRAM and SDRAM.

*Table 297.*0x04 - MCFG2 - Memory configuration register 2

31	30	29 27	26	25 23	22 21	20 19	18	17	16
SDRF	TRP	SDRAM TRFC	TCAS	SDRAM BANKSZ	SDRAM COLSZ	SDRAM CMD	D64	SDPB	R
0	1	0x3	1	0	0x2	0	*	0	0
rw	rw	rw	rw	rw	rw	rw	r	rw	r

15	14	13	12 9	8	7	6	5 4	3 2	1 0
R	SE	SI	RAM BANK SIZE		RBRDY	RMW	RAM WIDTH	RAM WRITE WS	RAM READ WS
0	0	0	NR		NR	NR	NR	0	0
r	rw	rw	rw		rw*	rw	rw	rw	rw

31 SDRAM refresh (SDRF) - Enables SDRAM refresh.

*Table 297.*0x04 - MCFG2 - Memory configuration register 2

30	SDRAM TRP parameter (TRP) - t_{RP} will be equal to 2 or 3 system clocks (0/1).
29 : 27	SDRAM TRFC parameter (SDRAM TRFC) - t_{RFC} will be equal to 3+field-value system clocks.
26	SDRAM TCAS parameter (TCAS) - Selects 2 or 3 cycle CAS delay (0/1). When changed, a LOAD-COMMAND-REGISTER command must be issued at the same time. Also sets RAS/CAS delay (t_{RCD}).
25 : 23	SDRAM bank size (SDRAM BANKSZ) - Sets the bank size for SDRAM chip selects (“000”=4MiB, “001”=8MiB, “010”=16MiB,...,. “111”=512MiB). When configured for 64-bit wide SDRAM data bus (sdbits=64), the meaning of this field doubles so that “000”=8 MiB, .., “111”=1024 MiB
22 : 21	SDRAM column size (SDRAM COLSZ) - “00”=256, “01”=512, “10”=1024, “11”=2048 except when bit[25:23]=˜111˜ then ˜11˜=4096
20 : 19	SDRAM command (SDRAM CMD) - Writing a non-zero value will generate a SDRAM command. “01”=PRECHARGE, “10”=AUTO-REFRESH, “11”=LOAD-COMMAND-REGISTER. The field is reset after the command has been executed.
18	64-bit SDRAM data bus (D64) - Reads ‘1’ if the memory controller is configured for 64-bit SDRAM data bus width, ‘0’ otherwise. Read-only.
17	SDRAM Page Burst (SDPB) - SDRAM programmed for page bursts on read when set, else programmed for line burst lengths of 8 on read. Programmable when pageburst VHDL generic is 2, else read-only.
16 : 15	RESERVED
14	SDRAM enable (SE) - Enables the SDRAM controller and disables fifth SRAM bank (RAMSN[4]).
13	SRAM disable (SI) - Disables accesses to SRAM bank if bit 14 (SE) is set to ‘1’.
12 : 9	RAM bank size (RAM BANK SIZE) - Sets the size of each RAM bank (“0000”=8KiB, “0001”=16KiB, “0010”=32KiB, “0011”= 64KiB,.., “1111”=256MiB)(i.e. 8KiB * 2**RAM BANK SIZE).
8	RESERVED
7	RAM bus ready enable (RBRDY) - Enables bus ready signaling for the RAM area. Bus read signaling for the RAM area is only available for the fifth chip-select and this field is only available if the memory controller has been implemented with the VHDL generic srbanks set to 5.
6	Read-modify-write enable (RMW) - Enables read-modify-write cycles for sub-word writes to 16- bit 32-bit areas with common write strobe (no byte write strobe).
5 : 4	RAM width (RAM WIDTH) - Sets the data width of the RAM area (“00”=8, “01”=16, “1X”=32).
3 : 2	RAM write waitstates (RAM WRITE WS) - Sets the number of wait states for RAM write cycles (“00”=0, “01”=1, “10”=2, “11”=3). The values above describe the default configuration The core can be configred at implementation to extend the number of waitstates. The number of wait states inserted will be (RAM WRITE WS)*$2^{ws\text{-}shift}$, where *wsshift* can be read from the first user-defined register in the core’s plug&play area (default is wsshift = 0).
1 : 0	RAM read waitstates (RAM READ WS) - Sets the number of wait states for RAM read cycles (“00”=0, “01”=1, “10”=2, “11”=3). The values above describe the default configuration The core can be configred at implementation to extend the number of waitstates. The number of wait states inserted will be (RAM READ WS)*$2^{ws\text{-}shift}$, where *wsshift* can be read from the first user-defined register in the core’s plug&play area (default is wsshift = 0).

27.16.3 Memory configuration register 3 (MCFG3)

MCFG3 contains the reload value for the SDRAM refresh counter and to control and monitor the memory EDAC.

*Table 298.*0x08 - MCFG3 - Memory configuration register 3

31 29	28	27	26
RESERVED	RSE	ME	SDRAM REFRESH COUNTER
0	0	1	NR

*Table 298.*0x08 - MCFG3 - Memory configuration register 3

r	rw	r	rw				
	12	11	10	9	8	7	0
		WB	RB	RE	PE	TCB	
		0	0	NR	0	NR	
		rw	rw	rw	rw	rw	

31 : 29	RESERVED
28	Reed-Solomon EDAC enable (RSE) - if set, will enable Reed-Solomon protection of SDRAM area when implemented
27	Memory EDAC (ME) - Indicates if memory EDAC is present. (read-only)
26 : 12	SDRAM refresh counter reload value (SDRAM REFRESH COUNTER)
11	EDAC diagnostic write bypass (WB) - Enables EDAC write bypass.
10	EDAC diagnostic read bypass (RB) - Enables EDAC read bypass.
9	RAM EDAC enable (RE) - Enable EDAC checking of the RAM area (including SDRAM).
8	PROM EDAC enable (PE) - Enable EDAC checking of the PROM area. Ar reset, this bit is initialized with the value of MEMI.EDAC.
7 : 0	Test checkbits (TCB) - This field replaces the normal checkbits during write cycles when WB is set. It is also loaded with the memory checkbits during read cycles when RB is set.

The period between each AUTO-REFRESH command is calculated as follows:

$t_{REFRESH}$ = ((reload value) + 1) / SYSCLK

27.16.4 Memory configuration register 4 (MCFG4)

MCFG4 is only present if the Reed-Solomon EDAC has been enabled with the *edac* VHDL generic. MCFG4 provides means to insert Reed-Solomon EDAC errors into memory for diagnostic purposes.

*Table 299.*0x0C - MCFG4 - Memory configuration register 4

31	16
RESERVED	WB

15	0
TCB[15:0]	

31 : 17	RESERVED
16	EDAC diagnostic write bypass (WB) - Enables EDAC write bypass. Identical to WB in MCFG3.
15 : 0	Test checkbits (TCB) - This field replaces the normal checkbits during write cycles when WB is set. It is also loaded with the memory checkbits during read cycles when RB is set. Note that TCB[7:0] are identical to TCB[7:0] in MCFG3

27.16.5 Memory configuration register 5 (MCFG5)

MCFG5 contains fields to control lead out cycles for the ROM and IO areas.

*Table 300.*0x10 - MCFG5 - Memory configuration register 5

31	30	29	23	22	16
RESERVED		IOHWS		RESERVED	
		0x00			
		rw			

15	14	13	7	6	0
RESERVED		ROMHWS		RESERVED	
		0x00			

*Table 300.*0x10 - MCFG5 - Memory configuration register 5

	rw	

31 : 30 RESERVED

29:23 IO lead out (IOHWS) - Lead out cycles added to IO accesses are IOHWS(3:0)*$2^{IOHWS(6:4)}$

22 : 14 RESERVED

13:7 ROM lead out (ROMHWS) - Lead out cycles added to ROM accesses are ROMHWS(3:0)*$2^{ROMHWS(6:4)}$

6 : 0 RESERVED

27.16.6 Memory configuration register 6 (MCFG6)

MCFG6 contains fields to control lead out cycles for the (S)RAM area.

*Table 301.*0x14 - MCFG6 - Memory configuration register 6

31		16
RESERVED		
0		
r		

15 14	13 7	6 0
RESERVED	RAMHWS	RESERVED
r	0x00	r
0	rw	0

31 : 14 RESERVED

13:7 RAM lead out (RAMHWS) - Lead out cycles added to RAM accesses are RAMHWS(3:0)*$2^{RAMHWS(6:4)}$

6 : 0 RESERVED

27.16.7 Memory configuration register 7 (MCFG7)

MCFG7 contains fields to control bus ready timeout.

*Table 302.*0x18 - MCFG7 - Memory configuration register 7

31		16
BRDYNCNT		
0		
rw		

15		0
BRDYNRLD		
0		
rw		

31 : 16 Bus ready count (BRDYNCOUNT) - Counter value. If this register is written then the counter shall be written with the same value as BRDYNRLD.

15: 0 Bus ready reload value (BRDYNRLD) - Reload value for BRDYNCNT

27.17 Vendor and device identifiers

The core has vendor identifier 0x01 (GAISLER) and device identifier 0x054. For description of vendor and device identifiers, see GRLIB IP Library User's Manual.

27.18 Implementation

27.18.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers. See the documentation for the *syncrst* VHDL generic for information on asynchronous reset affecting external signals.

27.19 Configuration options

Table 303 shows the configuration options of the core (VHDL generics).

*Table 303.*Configuration options

Generic	Function	Allowed range	Default
hindex	AHB slave index	1 - NAHBSLV-1	0
pindex	APB slave index	0 - NAPBSLV-1	0
romaddr	ADDR field of the AHB BAR0 defining PROM address space. Default PROM area is 0x0 - 0x1FFFFFFF. Also see documentation of romasel VHDL generic below.	0 - 16#FFF#	16#000#
rommask	MASK field of the AHB BAR0 defining PROM address space.. Also see documentation of romasel VHDL generic below.	0 - 16#FFF#	16#E00#
ioaddr	ADDR field of the AHB BAR1 defining I/O address space. Default I/O area is 0x20000000 - 0x2FFFFFFF.	0 - 16#FFF#	16#200#
iomask	MASK field of the AHB BAR1 defining I/O address space.	0 - 16#FFF#	16#E00#
ramaddr	ADDR field of the AHB BAR2 defining RAM address space. Default RAM area is 0x40000000-0x7FFFFFFF.	0 - 16#FFF#	16#400#
rammask	MASK field of the AHB BAR2 defining RAM address space.	0 -16#FFF#	16#C00#
paddr	ADDR field of the APB BAR configuration registers address space.	0 - 16#FFF#	0
pmask	MASK field of the APB BAR configuration registers address space.	0 - 16#FFF#	16#FFF#
wprot	RAM write protection.	0 - 1	0
invclk	unused	N/A	0
fast	Enable fast SDRAM address decoding.	0 - 1	0

*Table 303.*Configuration options

Generic	Function	Allowed range	Default
romasel	Sets the PROM bank size. *romasel 0*: selects a programmable mode where the ROMBANKSZ field in the MCFG1 register sets the bank size. When romasel is 0 and the bank size is configured (MCFG1 register, ROMBANKSZ field, via the core's register interface) to 0b000 or 0b1111 then address bit 28 is used to decode the banks. This means that the core must be mapped at a 512 MiB address boundary (0x0, 0x20000000, 0x40000000, .. see romaddr and rommask VHDL generics) for address decoding to work correctly. *romasel 1 - 14:* Values 1 - 14 sets the size in binary steps (1 = 16KiB, 2 = 32KiB, 3=64KiB, ..., 14=128MiB). Four chip-selects are available for these values. 15 sets the bank size to 256MiB with two chip-selects. *romasel 16 - 28:* Values 16 - 28 sets the bank size in binary steps (16 = 64 KiB, 17 = 128KiB, ... 28 = 256MiB). Two chip-selects are available for this range. The selected bank size is readable from the rombanksz field in the MCFG1 register for the non-programmable modes. The PROM area will wrap back to the first bank after the end of the last decoded bank. As an example, if romasel is set to 14 the following banks will be decoded: bank 0: 0x00000000 - 0x07FFFFFF bank 1: 0x08000000 - 0x0FFFFFFF bank 2: 0x10000000 - 0x17FFFFFF bank 3: 0x18000000 - 0x1FFFFFFF ...bank 0 starting again at 0x20000000 (the same pattern applies for other values less than 14, addresses will wrap after the last decoded bank). If romasel is 15 then the address decoding will result in the following: bank 0: 0x00000000 - 0x0FFFFFFF bank 1: 0x10000000 - 0x1FFFFFFF .. bank 0 starting again at offset 0x20000000 When instantiating the core care must be taken to see how many chip-selects that will be used as a result of the setting of romasel. This affects the base address at which the core can be placed (setting of romaddr and rommask VHDL generics). As an example, placing the PROM area at a 256 MiB address boundary, like the base address 0x10000000 and using romasel = 0, 14, 15 or 28 will NOT result in ROM chip-select 0 getting asserted for an access to the PROM base address as the address decoding requires that the core has been placed on a 512 MiB address boundary.	0 - 28	28
sdrasel	log2(RAM address space size) - 1. E.g if size of the RAM address space is 0x40000000 sdrasel is log2(2^30)-1= 29.	0 - 31	29
srbanks	Number of SRAM banks.	0 - 5	4
ram8	Enable 8-bit PROM, SRAM and I/O access.	0 - 1	0
ram16	Enable 16-bit PROM, SRAM and I/O access.	0 - 1	0
sden	Enable SDRAM controller.	0 - 1	0
sepbus	SDRAM is located on separate bus.	0 - 1	1
sdbits	32 or 64 -bit SDRAM data bus.	32, 64	32
oepol	Select polarity of drive signals for data pads. 0 = active low, 1 = active high.	0 - 1	0

*Table 303.*Configuration options

Generic	Function	Allowed range	Default
edac	Enable EDAC. 0 = No EDAC; 1 = BCH EDAC; 2 = BCH EDAC with pipelining; 3 = BCH + RS EDAC	0 - 3	0
sdlsb	Select least significant bit of the address bus that is connected to SDRAM.	-	2
syncrst	Choose between synchronous and asynchronous reset for chip-select, oen and drive signals.	0 - 1	0
pageburst	Line burst read of length 8 when 0, page burst read when 1, programmable read burst type when 2.	0-2	0
scantest	Enable scan test support	0 - 1	0
netlist	Use technology specific netlist instead of RTL code	0 - 1	0
tech	Technology to use for netlists	0 - NTECH	0
rahold	Unused	0 - 16	0
wsshift	Wait state counter shift. This value defines the number of steps to shift the wait state counter. The number of waitstates that the core can generate is limited by $2^{wsshift}$. See the wait state fields in the core's APB register descriptions to see the effect of this generic. The value of this generic can be read out in the first user-defined register of the core's plug&play area. This means that if wsshift is non-zero then the AHB controller must have full plug&play decoding enabled.	-	0
brdynto	Bus ready timeout conunter enable. If this generic is non-zero then the core will be implemented with a bus ready timeout counter (see MCFG7).	0 - 1	0

27.20 Scan support

Scan support is enabled by setting the SCANTEST generic to 1. When enabled, the asynchronous reset of any flip-flop will be connected to AHBI.testrst during when AHBI.testen = '1'.

27.21 Signal descriptions

Table 304 shows the interface signals of the core (VHDL ports).

*Table 304.*Signal descriptions

Signal name	Field	Type	Function	Active
CLK	N/A	Input	Clock	-
RST	N/A	Input	Reset	Low
MEMI	DATA[31:0]	Input	Memory data	High
	BRDYN	Input	Bus ready strobe	Low
	BEXCN	Input	Bus exception	Low
	CB[15:0]	Input	EDAC checkbits	High
	WRN[3:0]	Input	SRAM write enable feedback signal	Low
	BWIDTH[1:0]	Input	Sets the reset value of the PROM data bus width field in the MCFG1 register	High
	EDAC	Input	The reset value for the PROM EDAC enable bit	High
	SD[31:0]	Input	SDRAM separate data bus	High
	SCB[15:0]	Input	SDRAM separate checkbit bus	High

*Table 304.*Signal descriptions

Signal name	Field	Type	Function	Active
MEMO	ADDRESS[31:0]	Output	Memory address	High
	CB[15:0]	Output	EDAC Checkbit	
	DATA[31:0]	Output	Memory data	-
	SDDATA[63:0]	Output	Sdram memory data	-
	RAMSN[4:0]	Output	SRAM chip-select	Low
	RAMOEN[4:0]	Output	SRAM output enable	Low
	IOSN	Output	Local I/O select	Low
	ROMSN[3:0]	Output	PROM chip-select	Low
	OEN	Output	Output enable	Low
	WRITEN	Output	Write strobe	Low
	WRN[3:0]	Output	SRAM write enable: WRN[0] corresponds to DATA[31:24], WRN[1] corresponds to DATA[23:16], WRN[2] corresponds to DATA[15:8], WRN[3] corresponds to DATA[7:0]. Any WRN[ ] signal can be used for CB[ ].	Low
	MBEN[3:0]	Output	Read/write byte enable: MBEN[0] corresponds to DATA[31:24], MBEN[1] corresponds to DATA[23:16], MBEN[2] corresponds to DATA[15:8], MBEN[3] corresponds to DATA[7:0]. Any MBEN[ ] signal can be used for CB[ ].	Low
	BDRIVE[3:0]	Output	Drive byte lanes on external memory bus. Controls I/O-pads connected to external memory bus: BDRIVE[0] corresponds to DATA[31:24], BDRIVE[1] corresponds to DATA[23:16], BDRIVE[2] corresponds to DATA[15:8], BDRIVE[3] corresponds to DATA[7:0]. Any BDRIVE[ ] signal can be used for CB[ ].	Low/High
	VBDRIVE[31:0]	Output	Vectored I/O-pad drive signals.	Low/High
	SVBDRIVE[63:0]	Output	Vectored I/O-pad drive signals for separate sdram bus.	Low/High
	READ	Output	Read strobe	High
	SA[14:0]	Output	SDRAM separate address bus	High
	CE	Output	Single error detected	High
AHBSI	*	Input	AHB slave input signals	-
AHBSO	*	Output	AHB slave output signals	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
WPROT	WPROTHIT	Input	Unused	-

*Table 304.*Signal descriptions

Signal name	Field	Type	Function	Active
SDO	SDCASN	Output	SDRAM column address strobe	Low
	SDCKE[1:0]	Output	SDRAM clock enable	High
	SDCSN[1:0]	Output	SDRAM chip select	Low
	SDDQM[7:0]	Output	SDRAM data mask: SDDQM[7] corresponds to SD[63:56], SDDQM[6] corresponds to SD[55:48], SDDQM[5] corresponds to SD[47:40], SDDQM[4] corresponds to SD[39:32], SDDQM[3] corresponds to SD[31:24], SDDQM[2] corresponds to SD[23:16], SDDQM[1] corresponds to SD[15:8], SDDQM[0] corresponds to SD[7:0]. Any SDDQM[ ] signal can be used for CB[ ].	Low
	SDRASN	Output	SDRAM row address strobe	Low
	SDWEN	Output	SDRAM write enable	Low

* see GRLIB IP Library User's Manual

27.22 Signal definitions and reset values

The signals and their reset values are described in table 305.

*Table 305.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
address[27:0]	Output	Memory address	High	Undefined
data[31:0]	Input/Output	Memory data	High	Tri-state
cb[15:0]	Input/Output	Check bits	High	Tri-state
ramsn[4:0]	Output	SRAM chip select	Low	Logical 1
ramoen[4:0]	Output	SRAM output enable	Low	Logical 1
rwen[3:0]	Output,	SRAM write byte enable: rwen[0] corresponds to data[31:24], rwen[1] corresponds to data[23:16], rwen[2] corresponds to data[15:8], rwen[3] corresponds to data[7:0]. Any rwen[ ] signal can be used for cb[ ].	Low	Logical 1
ramben[3:0]	Output	SRAM read/write byte enable: ramben[0] corresponds to data[31:24], ramben[1] corresponds to data[23:16], ramben[2] corresponds to data[15:8], ramben[3] corresponds to data[7:0]. Any ramben[ ] signal can be used for cb[ ].	Low	Logical 1
oen	Output	Output enable	Low	Logical 1
writen	Output	Write strobe	Low	Logical 1
read	Output	Read strobe	High	Logical 1
iosn	Output	IO area chip select	Low	Logical 1
romsn[3:0]	Output	PROM chip select	Low	Logical 1
brdyn	Input	Bus ready. Extends accesses to the IO area.	Low	-
bexcn	Input	Bus exception.	Low	-
sa[15:0]	Output	SDRAM address	High	Undefined
sd[31:0]	Input/Output	SDRAM data	High	Tri-state
scb[15:0]	Input/Output	SDRAM check bits	High	Tri-state
sdcsn[1:0]	Output	SDRAM chip select	Low	Logical 1
sdwen	Output	SDRAM write enable	Low	Logical 1
sdrasn	Output	SDRAM row address strobe	Low	Logical 1
sdcasn	Output	SDRAM column address strobe	Low	Logical 1
sddqm[3:0]	Output	SDRAM data mask: sddqm[5] corresponds to scb[15:8], sddqm[4] corresponds to scb[7:0], sddqm[3] corresponds to sd[31:24], sddqm[2] corresponds to sd[23:16], sddqm[1] corresponds to sd[15:8], sddqm[0] corresponds to sd[7:0]. Any sddqm[ ] signal can be used for scb[ ].	Low	Logical 1

27.23 Timing

The timing waveforms and timing parameters are shown in figure 82 and are defined in table 306.

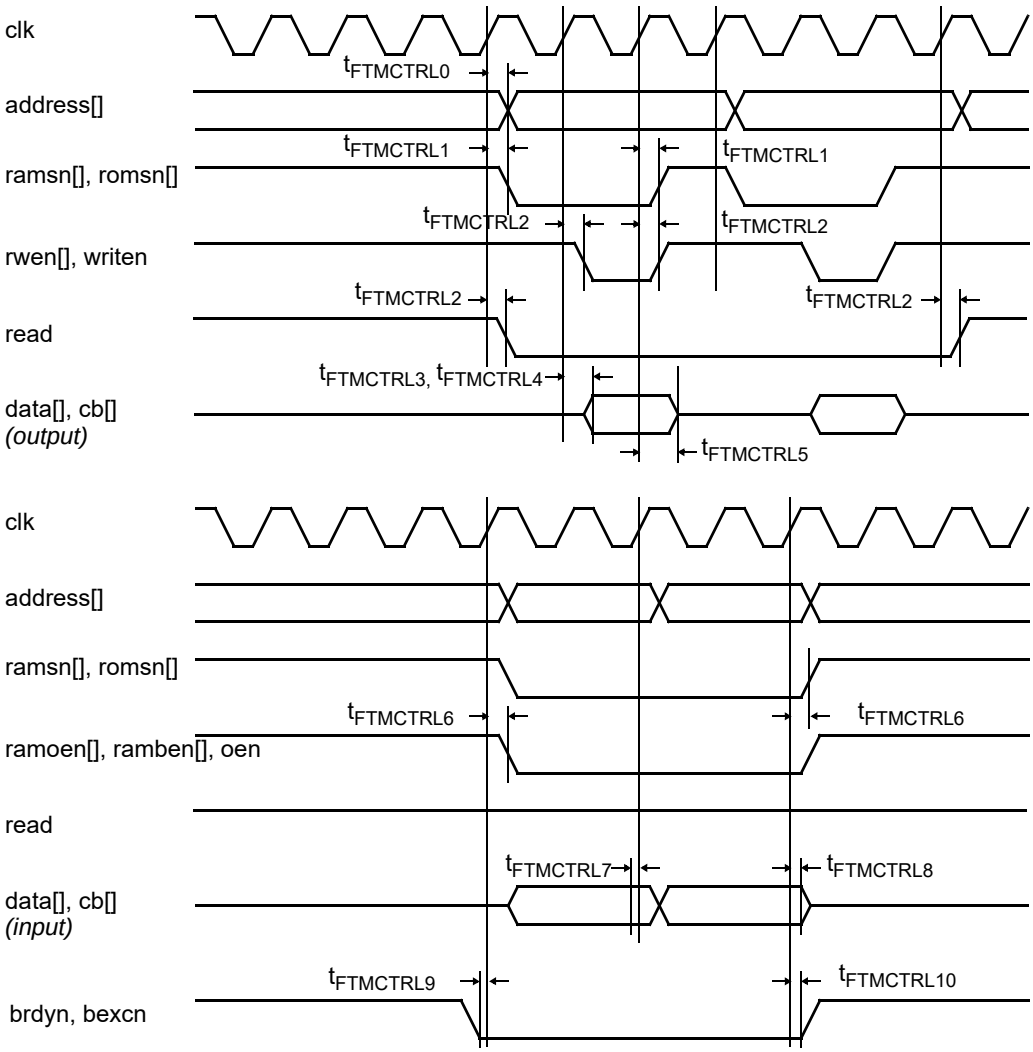


Figure 82. Timing waveforms - SRAM, PROM accesses

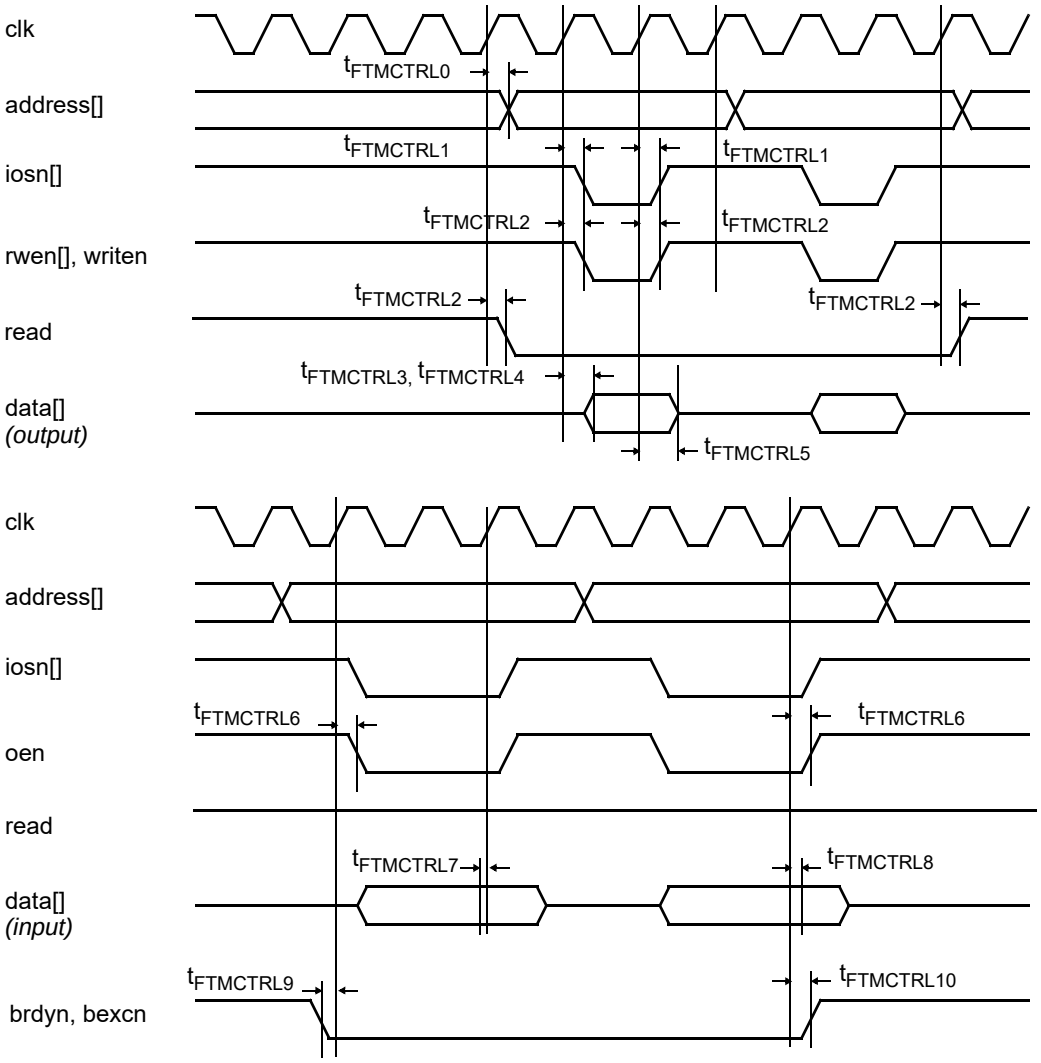


Figure 83. Timing waveforms - I/O accesses

*Table 306.*Timing parameters - SRAM, PROM and I/O accesses

Name	Parameter	Reference edge	Min	Max	Unit
$t_{FTMCTRL0}$	address clock to output delay	rising clk edge	TBD	TBD	ns
$t_{FTMCTRL1}$	clock to output delay	rising clk edge	TBD	TBD	ns
$t_{FTMCTRL2}$	clock to output delay	rising clk edge	TBD	TBD	ns
$t_{FTMCTRL3}$	clock to data output delay	rising clk edge	TBD	TBD	ns
$t_{FTMCTRL4}$	clock to data non-tri-state delay	rising clk edge	TBD	TBD	ns
$t_{FTMCTRL5}$	clock to data tri-state delay	rising clk edge	TBD	TBD	ns
$t_{FTMCTRL6}$	clock to output delay	rising clk edge	TBD	TBD	ns
$t_{FTMCTRL7}$	data input to clock setup	rising clk edge	TBD	-	ns
$t_{FTMCTRL8}$	data input from clock hold	rising clk edge	TBD	-	ns
$t_{FTMCTRL9}$	input to clock setup	rising clk edge	TBD	-	ns
$t_{FTMCTRL10}$	input from clock hold	rising clk edge	TBD	-	ns

The timing waveforms and timing parameters are shown in figure 82 and are defined in table 306.

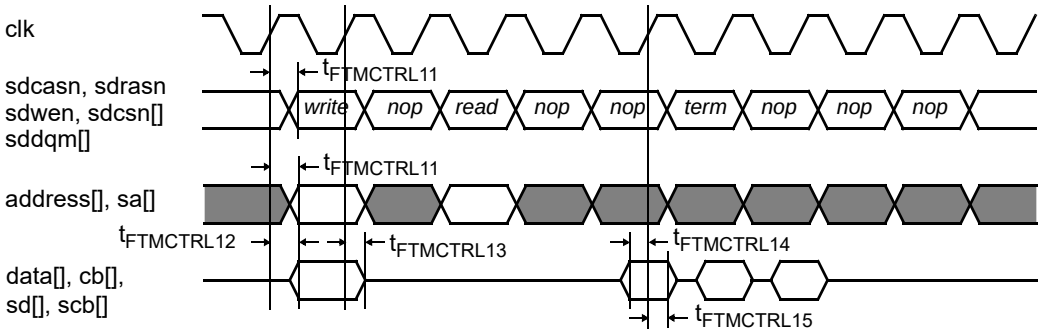


Figure 84. Timing waveforms - SDRAM accesses

*Table 307.*Timing parameters - SDRAM accesses

Name	Parameter	Reference edge	Min	Max	Unit
$t_{FTMCTRL11}$	clock to output delay	rising clk edge	TBD	TBD	ns
$t_{FTMCTRL12}$	clock to data output delay	rising clk edge	TBD	TBD	ns
$t_{FTMCTRL13}$	data clock to data tri-state delay	rising clk edge	TBD	TBD	ns
$t_{FTMCTRL14}$	data input to clock setup	rising clk edge	TBD	-	ns
$t_{FTMCTRL15}$	data input from clock hold	rising clk edge	TBD	-	ns

27.24 Library dependencies

Table 308 shows libraries used when instantiating the core (VHDL libraries).

*Table 308.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AHB signal definitions
GAISLER	MEMCTRL	Signals	Memory bus signals definitions
		Components	FTMCTRL component

27.25 Instantiation

This example shows how the core can be instantiated.

The example design contains an AMBA bus with a number of AHB components connected to it including the memory controller. The external memory bus is defined on the example designs port map and connected to the memory controller. System clock and reset are generated by GR Clock Generator and Reset Generator.

Memory controller decodes default memory areas: PROM area is 0x0 - 0x1FFFFFFF, I/O-area is 0x20000000-0x3FFFFFFF and RAM area is 0x40000000 - 0x7FFFFFFF. SDRAM controller is enabled. SDRAM clock is synchronized with system clock by clock generator.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.memctrl.all;
use gaisler.pads.all;   -- used for I/O pads

entity mctrl_ex is
```

```
  port (
    clk : in std_ulogic;
    resetn : in std_ulogic;
    pllref : in  std_ulogic;

    -- memory bus
    address  : out   std_logic_vector(27 downto 0); -- memory bus
    data     : inout std_logic_vector(31 downto 0);
    ramsn    : out   std_logic_vector(4 downto 0);
    ramoen   : out   std_logic_vector(4 downto 0);
    rwen     : inout std_logic_vector(3 downto 0);
    romsn    : out   std_logic_vector(3 downto 0);
    iosn     : out   std_logic;
    oen      : out   std_logic;
    read     : out   std_logic;
    writen   : inout std_logic;
    brdyn    : in    std_logic;
    bexcn    : in    std_logic;
-- sdram i/f
    sdcke    : out std_logic_vector ( 1 downto 0);  -- clk en
    sdcsn    : out std_logic_vector ( 1 downto 0);  -- chip sel
    sdwen    : out std_logic;                       -- write en
    sdrasn   : out std_logic;                       -- row addr stb
    sdcasn   : out std_logic;                       -- col addr stb
    sddqm    : out std_logic_vector (7 downto 0);  -- data i/o mask
    sdclk    : out std_logic;                        -- sdram clk output
    sa       : out std_logic_vector(14 downto 0); -- optional sdram address
    sd       : inout std_logic_vector(63 downto 0) -- optional sdram data
    );
end;

architecture rtl of mctrl_ex is

  -- AMBA bus (AHB and APB)
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbsi : ahb_slv_in_type;
  signal ahbso : ahb_slv_out_vector := (others => ahbs_none);
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);

  -- signals used to connect memory controller and memory bus
  signal memi : memory_in_type;
  signal memo : memory_out_type;

  signal sdo : sdram_out_type;

  signal wprot : wprot_out_type;  -- dummy signal, not used
  signal clkm, rstn : std_ulogic; -- system clock and reset

-- signals used by clock and reset generators
  signal cgi : clkgen_in_type;
  signal cgo : clkgen_out_type;

  signal gnd : std_ulogic;

begin

  -- Clock and reset generators
  clkgen0 : clkgen generic map (clk_mul => 2, clk_div => 2, sdramen => 1,
                                tech => virtex2, sdinvclk => 0)
  port map (clk, gnd, clkm, open, open, sdclk, open, cgi, cgo);

  cgi.pllctrl <= "00"; cgi.pllrst <= resetn; cgi.pllref <= pllref;

  -- Memory controller
  ftmctrl0 : ftmctrl generic map (srbanks => 1, sden => 1, edac => 1)
    port map (rstn, clkm, memi, memo, ahbsi, ahbso(0), apbi, apbo(0), wprot, sdo);

  -- memory controller inputs not used in this configuration
  memi.brdyn <= '1'; memi.bexcn <= '1'; memi.wrn <= "1111";
```

```
  memi.sd <= sd;

  -- prom width at reset
  memi.bwidth <= "10";

  -- I/O pads driving data memory bus data signals
  datapads : for i in 0 to 3 generate
      data_pad : iopadv generic map (width => 8)
      port map (pad => memi.data(31-i*8 downto 24-i*8),
                o => memi.data(31-i*8 downto 24-i*8),
                en => memo.bdrive(i),
                i => memo.data(31-i*8 downto 24-i*8));
  end generate;

  -- connect memory controller outputs to entity output signals
  address <= memo.address; ramsn <= memo.ramsn; romsn <= memo.romsn;
  oen <= memo.oen; rwen <= memo.wrn; ramoen <= "1111" & memo.ramoen(0);
  sa <= memo.sa;
  writen <= memo.writen; read <= memo.read; iosn <= memo.iosn;
  sdcke <= sdo.sdcke; sdwen <= sdo.sdwen; sdcsn <= sdo.sdcsn;
  sdrasn <= sdo.rasn; sdcasn <= sdo.casn; sddqm <= sdo.dqm;
end;
```

28 FTSDCTRL - 32/64-bit PC133 SDRAM Controller with EDAC

28.1 Overview

The fault tolerant SDRAM memory interface handles PC133 SDRAM compatible memory devices attached to a 32- or 64-bit wide data bus. The interface acts as a slave on the AHB bus where it occupies configurable amount of address space for SDRAM access. An optional Error Detection And Correction Unit (EDAC) logic (only for the 32 - bit bus) corrects one bit error and detects two bit errors.

The SDRAM controller function is programmed by means of register(s) mapped into AHB I/O address space. Chip-select decoding is done for two SDRAM banks.

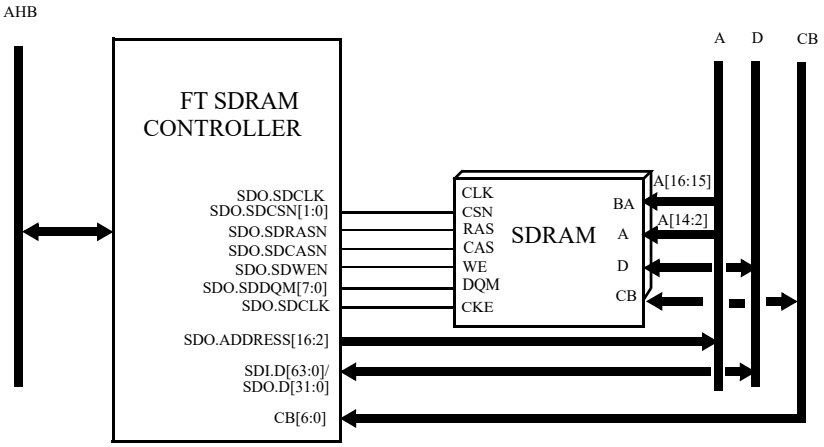


Figure 85. FT SDRAM memory controller connected to AMBA bus and SDRAM

28.2 Operation

28.2.1 General

Synchronous Dynamic RAM (SDRAM) access is supported to two banks of PC100/PC133 compatible devices. The controller supports 64, 256 and 512 Mbyte devices with 8 - 12 column-address bits, up to 13 row-address bits, and 4 banks. The size of each of the two banks can be programmed in binary steps between 4 Mbyte and 512 Mbyte. The operation of the SDRAM controller is controlled through the configuration register SDCFG. A second register, ECFG, is available for configuring the EDAC functions. SDRAM banks data bus width is configurable between 32 and 64 bits.

28.2.2 Initialization

When the SDRAM controller is enabled, it automatically performs the SDRAM initialization sequence of PRECHARGE, 8x AUTO-REFRESH and LOAD-MODE-REG on both banks simultaneously. When mobile SDRAM functionality is enabled, the initialization sequence is appended with a LOAD-EXTMODE-REG command. The controller programs the SDRAM to use page burst on read accesses and single location access on write accesses. If the *pwron* VHDL generic is 1, the initialization sequence is also sent automatically when reset is released. Note that some SDRAM devices require a stable clock of 100 us before any commands might be sent. When using on-chip PLL, this might not always be the case and the *pwron* VHDL generic should be set to 0 in such cases.

28.2.3 Configurable SDRAM timing parameters

To provide optimum access cycles for different SDRAM devices (and at different frequencies), three SDRAM parameters can be programmed through memory configuration register 2 (MCFG2): TCAS, TRP and TRFCD. The value of these fields affect the SDRAM timing as described in table 309.

*Table 309.*SDRAM programmable minimum timing parameters

SDRAM timing parameter	Minimum timing (clocks)
CAS latency, RAS/CAS delay (t_{CAS}, t_{RCD})	TCAS + 2
Precharge to activate (t_{RP})	TRP + 2
Auto-refresh command period (t_{RFC})	TRFC + 3
Activate to precharge (t_{RAS})	TRFC + 1
Activate to Activate (t_{RC})	TRP + TRFC + 4

If the TCAS, TRP and TRFC are programmed such that the PC100/133 specifications are fulfilled, the remaining SDRAM timing parameters will also be met. The table below shows typical settings for 100 and 133 MHz operation and the resulting SDRAM timing (in ns):

*Table 310.*SDRAM example programming

SDRAM settings	t_{CAS}	t_{RC}	t_{RP}	t_{RFC}	t_{RAS}
100 MHz, CL=2; TRP=0, TCAS=0, TRFC=4	20	80	20	70	50
100 MHz, CL=3; TRP=0, TCAS=1, TRFC=4	30	80	20	70	50
133 MHz, CL=2; TRP=1, TCAS=0, TRFC=6	15	82	22	67	52
133 MHz, CL=3; TRP=1, TCAS=1, TRFC=6	22	82	22	67	52

When mobile SDRAM support is enabled, one additional timing parameter (TXSR) can be programmed though the Power-Saving configuration register.

*Table 311.*Mobile SDRAM programmable minimum timing parameters

SDRAM timing parameter	Minimum timing (clocks)
Exit Self Refresh mode to first valid command (t_{XSR})	tXSR

28.2.4 Refresh

The SDRAM controller contains a refresh function that periodically issues an AUTO-REFRESH command to both SDRAM banks. The period between the commands (in clock periods) is programmed in the refresh counter reload field in the SDCFG register. Depending on SDRAM type, the required period is typically 7.8 or 15.6 µs (corresponding to 780 or 1560 clocks at 100 MHz). The generated refresh period is calculated as (reload value+1)/sysclk. The refresh function is enabled by setting bit 31 in SDCFG register.

28.2.5 Self Refresh

The self refresh mode can be used to retain data in the SDRAM even when the rest of the system is powered down. When in the self refresh mode, the SDRAM retains data without external clocking and refresh are handled internally. The memory array that is refreshed during the self refresh operation is defined in the extended mode register. These settings can be changed by setting the PASR bits in the Power-Saving configuration register. The extended mode register is automatically updated when the PASR bits are changed. The supported “Partial Array Self Refresh” modes are: Full, Half, Quarter, Eighth, and Sixteenth array. “Partial Array Self Refresh” is only supported when mobile SDRAM functionality is enabled. To enable the self refresh mode, set the PMODE bits in the Power-Saving configuration register to “010” (Self Refresh). The controller will enter self refresh mode after

every memory access (when the controller has been idle for 16 clock cycles), until the PMODE bits are cleared. When exiting this mode the controller introduce a delay defined by tXSR in the Power-Saving configuration register and a AUTO REFRESH command before any other memory access is allowed. The minimum duration of this mode is defined by tRAS. This mode is only available when the VHDL generic *mobile* is >= 1.

28.2.6 Power-Down

When entering the power-down mode all input and output buffers, excluding SDCKE, are deactivated. All data in the SDRAM is retained during this operation. To enable the power-down mode, set the PMODE bits in the Power-Saving configuration register to “001” (Power-Down). The controller will enter power-down mode after every memory access (when the controller has been idle for 16 clock cycles), until the PMODE bits is cleared. The REFRESH command will still be issued by the controller in this mode. When exiting this mode a delay of one clock cycles are added before issue any command to the memory. This mode is only available when the VHDL generic *mobile* is >= 1.

28.2.7 Deep Power-Down

The deep power-down operating mode is used to achieve maximum power reduction by eliminating the power of the memory array. Data will not be retained after the device enters deep power-down mode. To enable the deep power-down mode, set the PMODE bits in the Power-Saving configuration register to “101” (Deep Power-Down). To exit the deep power-down mode the PMODE bits in the Power-Saving configuration register must be cleared. The controller will respond with an AMBA ERROR response to an AMBA access, that will result in a memory access, during Deep Power-Down mode. This mode is only available when the VHDL generic *mobile* is >= 1 and mobile SDRAM functionality is enabled.

28.2.8 Temperature-Compensated Self Refresh

The settings for the temperature-compensation of the Self Refresh rate can be controlled by setting the TCSR bits in the Power-Saving configuration register. The extended mode register is automatically updated when the TCSR bits are changed. Note that some vendors implements a Internal Temperature-Compensated Self Refresh feature, which makes the memory ignore the TCSR bits. This functionality is only available when the VHDL generic *mobile* is >= 1 and mobile SDRAM functionality is enabled.

28.2.9 Drive Strength

The drive strength of the output buffers can be controlled by setting the DS bits in the Power-Saving configuration register. The extended mode register is automatically updated when the DS bits are changed. The available options are: full, three-quarter, one-half, and one-quarter drive strengths. This functionality is only available when the VHDL generic *mobile* is >= 1 and mobile SDRAM functionality is enabled.

28.2.10 SDRAM commands

The controller can issue three SDRAM commands by writing to the SDRAM command field in SDCFG: PRE-CHARGE, AUTO-REFRESH and LOAD-MODE-REG (LMR). If the LMR command is issued, the CAS delay as programmed in SDCFG will be used. Line burst of length 8 will be set for read when pageburst VHDL generic is 0. Page burst will be set for read when pageburst VHDL generic is 1. Page burst or line burst of length 8, selectable via the SDCFG register will be set, when pageburst VHDL generic is 2. Remaining fields are fixed: page read burst, single location write, sequential burst. The command field will be cleared after a command has been executed. Note that when changing the value of the CAS delay, a LOAD-MODE-REGISTER command should be generated at the same time.

28.2.11 Read cycles

A read cycle is started by performing an ACTIVATE command to the desired bank and row, followed by a READ command after the programmed CAS delay. A read burst is performed if a burst access has been requested on the AHB bus. The read cycle is terminated with a PRE-CHARGE command, no banks are left open between two accesses. Note that only word bursts are supported by the SDRAM controller. The AHB bus supports bursts of different sizes such as bytes and halfwords but they cannot be used.

28.2.12 Write cycles

Write cycles are performed similarly to read cycles, with the difference that WRITE commands are issued after activation. A write burst on the AHB bus will generate a burst of write commands without idle cycles in-between. As in the read case, only word bursts are supported.

28.2.13 Address bus connection

The SDRAM address bus should be connected to SA[12:0], the bank address to SA[14:13], and the data bus to SD[31:0] or SD[63:0] if 64-bit data bus is used.

28.2.14 Data bus

Data bus width is configurable to 32 or 64 bits. 64-bit data bus allows the 64-bit SDRAM devices to be connected using the full data capacity of the devices. 64-bit SDRAM devices can be connected to 32-bit data bus if 64-bit data bus is not available but in this case only half the full data capacity will be used.

28.2.15 EDAC

The controller optionally contains Error Detection And Correction (EDAC) logic, using a BCH(32, 7) code. It is capable of correcting one bit error and detecting two bit errors. The EDAC logic does not add any additional waitstates during normal operation. Detected errors will cause additional waitstates for correction (single errors) or error reporting (multiple errors). Single errors are automatically corrected and generally not visible externally unless explicitly checked.

This checking is done by monitoring the ce signal and single error counter. This counter holds the number of detected single errors. The ce signal is asserted one clock cycle when a single error is detected and should be connected to the AHB status register. This module stores the AHB status of the instruction causing the single error and generates interrupts (see the AHB status register documentation for more information).

The EDAC functionality can be enabled/disabled during run-time from the ECFG register (and the logic can also be completely removed during synthesis with VHDL generics. The ECFG register also contains control bits and checkbit fields for diagnostic reads. These diagnostic functions are used for testing the EDAC functions on-chip and allows one to store arbitrary checkbits with each written word. Checkbits read from memory can also be controlled.

64-bit bus support is not provided when EDAC is enabled. Thus, the and edacen VHDL generic should never be set to one when the sdbits VHDL generic is set to 64.

The equations below show how the EDAC checkbits are generated:

```
CB0 = D0 ^ D4 ^ D6 ^ D7 ^ D8 ^ D9 ^ D11 ^ D14 ^ D17 ^ D18 ^ D19 ^ D21 ^ D26 ^ D28 ^ D29 ^ D31
CB1 = D0 ^ D1 ^ D2 ^ D4 ^ D6 ^ D8 ^ D10 ^ D12 ^ D16 ^ D17 ^ D18 ^ D20 ^ D22 ^ D24 ^ D26 ^ D28
CB2 = D0 ^ D3 ^ D4 ^ D7 ^ D9 ^ D10 ^ D13 ^ D15 ^ D16 ^ D19 ^ D20 ^ D23 ^ D25 ^ D26 ^ D29 ^ D31
CB3 = D0 ^ D1 ^ D5 ^ D6 ^ D7 ^ D11 ^ D12 ^ D13 ^ D16 ^ D17 ^ D21 ^ D22 ^ D23 ^ D27 ^ D28 ^ D29
CB4 = D2 ^ D3 ^ D4 ^ D5 ^ D6 ^ D7 ^ D14 ^ D15 ^ D18 ^ D19 ^ D20 ^ D21 ^ D22 ^ D23 ^ D30 ^ D31
CB5 = D8 ^ D9 ^ D10 ^ D11 ^ D12 ^ D13 ^ D14 ^ D15 ^ D24 ^ D25 ^ D26 ^ D27 ^ D28 ^ D29 ^ D30 ^ D31
CB6 = D0 ^ D1 ^ D2 ^ D3 ^ D4 ^ D5 ^ D6 ^ D7 ^ D24 ^ D25 ^ D26 ^ D27 ^ D28 ^ D29 ^ D30 ^ D31
```

28.2.16 Clocking

The SDRAM controller is designed for an external SDRAM clock that is in phase or slightly earlier than the internal AHB clock. This provides the maximum margin for setup and hold on the external signals, and allows highest possible frequency. For Xilinx and Altera devices, the GRLIB Clock Generator (CLKGEN) can be configured to produce a properly synchronized SDRAM clock. For other FPGA targets, the custom clock synchronization must be designed, or the inverted clock option can be used (see below). For ASIC targets, the SDRAM clock can be derived from the AHB clock with proper delay adjustments during place&route.

If the VHDL generic INVCLK is set, then all outputs from the SDRAM controller are delayed for 1/2 clock. This is done by clocking all output registers on the falling clock edge. This option can be used on FPGA targets where proper SDRAM clock synchronization cannot be achieved. The SDRAM clock can be the internal AHB clock without further phase adjustments. Since the SDRAM signals will only have 1/2 clock period to propagate, this option typically limits the maximum SDRAM frequency to 40 - 50 MHz.

28.2.17 Endianness

The core is designed for big-endian systems.

28.3 Registers

The memory controller is programmed through register(s) mapped into the AHB I/O space defined by the controllers AHB BAR1.

If EDAC is enabled through the use of the edacen VHDL generic, an EDAC configuration register will be available.

*Table 312.*FT SDRAM controller registers

AHB address offset	Register
0x0	SDRAM Configuration register
0x4	EDAC Configuration register

28.3.1 SDRAM configuration register (SDCFG)

SDRAM configuration register is used to control the timing of the SDRAM.

Table 313. 0x00 - SDCFG - SDRAM configuration register

31	30	29 27	26	25 23	22 21	20 19	18	17	16	15	14 0
Refresh	tRP	tRFC	tCD	SDRAM bank size	SDRAM col. size	SDRAM command	R	Page-Burst	R	D64	SDRAM refresh load value
0	1	0b111	1	0	0b10	0	*	*	*	*	NR
rw	rw	rw	rw	rw	rw	rw	r	rw*	r	r	rw

31 SDRAM refresh. If set, the SDRAM refresh will be enabled.

30 SDRAM t_{RP} timing. t_{RP} will be equal to 2 or 3 system clocks (0/1).

29: 27 SDRAM t_{RFC} timing. t_{RFC} will be equal to 3 + field-value system clocks.

26 SDRAM CAS delay. Selects 2 or 3 cycle CAS delay (0/1). When changed, a LOAD-COMMAND-REGISTER command must be issued at the same time. Also sets RAS/CAS delay (tRCD).

25: 23 SDRAM banks size. Defines the decoded memory size for each SDRAM chip select: “000”= 4 Mbyte, “001”= 8 Mbyte, “010”= 16 Mbyte .... “111”= 512 Mbyte.

When configured for 64-bit wide SDRAM data bus (sdbits=64), the meaning of this field doubles so that “000”=8 Mbyte, .., “111”=1024 Mbyte

22: 21 SDRAM column size. “00”=256, “01”=512, “10”=1024, “11”=2048 except when bit[25:23]=˜111˜ then ˜11˜=4096

Table 313. 0x00 - SDCFG - SDRAM configuration register

20: 19	SDRAM command. Writing a non-zero value will generate an SDRAM command: “01”=PRE-CHARGE, “10”=AUTO-REFRESH, “11”=LOAD-COMMAND-REGISTER. The field is reset after command has been executed.
17	1 = pageburst is used for read operations, 0 = line burst of length 8 is used for read operations. (Only available when VHDL generic pageburst i set to 2)
15	64-bit data bus (D64) - Reads ‘1’ if memory controller is configured for 64-bit data bus, otherwise ‘0’. Read-only.
14: 0	The period between each AUTO-REFRESH command - Calculated as follows: tREFRESH = ((reload value) + 1) / SYSCLK

28.3.2 EDAC Configuration register (ECFG)

The EDAC configuration register controls the EDAC functions of the SDRAM controller during run time.

*Table 314.*0x04 - ECFG - EDAC configuration register

31	30 ... cntbits + 10	cnbits + 9 ... 10	9	8	7	6 ... 0
EAV	RESERVED	SEC	WB	RB	EN	TCB
*	0	NR	NR	NR	0	NR
r	r	wc	rw	rw	rw	rw

6: 0	TCB : Test checkbits. These bits are written as checkbits into memory during a write operation when the WB bit in the ECFG register is set. Checkbits read from memory during a read operation are written to this field when the RB bit is set.
7:	EN : EDAC enable. Run time enable/disable of the EDAC functions. If EDAC is disabled no error detection will be done during reads and subword writes. Checkbits will still be written to memory during write operations.
8:	RB : Read bypass. Store the checkbits read from memory during a read operation into the TCB field.
9:	WB : Write bypass. Write the TCB field as checkbits into memory for all write operations.
cntbits + 9: 10	SEC : Single error counter. This field is available when the errcnt VHDL generic is set to one during synthesis. It increments each time a single error is detected. It saturates when the maximum value is reached. The maximum value is the largest number representable in the number of bits used, which in turn is determined by the cntbits VHDL generic. Each bit in the counter can be reset by writing a one to it.
30:cntbits + 10	Reserved.
31:	EAV : EDAC available. This bit is always one if the SDRAM controller contains EDAC.

28.4 Vendor and device identifiers

The module has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x055. For a description of vendor and device identifiers see GRLIB IP Library User’s Manual.

28.5 Implementation

28.5.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User’s Manual). By default, the core makes use of synchronous reset and resets a subset of its internal registers.

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core will use asynchronous reset for all registers, except synchronization registers, if the GRLIB config package setting *grlib_async_reset_enable* is set.

The registers driving SDRAM chip select and output enables for the SDRAM data bus have asynchronous reset.

28.6 Configuration options

Table 315 shows the configuration options of the core (VHDL generics).

*Table 315.*Configuration options

Generic	Function	Allowed range	Default
hindex	AHB slave index	1 - NAHBSLV-1	0
haddr	ADDR field of the AHB BAR0 defining SDRAM area. Default is 0xF0000000 - 0xFFFFFFFF.	0 - 16#FFF#	16#000#
hmask	MASK field of the AHB BAR0 defining SDRAM area.	0 - 16#FFF#	16#F00#
ioaddr	ADDR field of the AHB BAR1 defining I/O address space where SDCFG register is mapped.	0 - 16#FFF#	16#000#
iomask	MASK field of the AHB BAR1 defining I/O address space.	0 - 16#FFF#	16#FFF#
wprot	Write protection.	0 - 1	0
invclk	Inverted clock is used for the SDRAM.	0 - 1	0
fast	Enable fast SDRAM address decoding.	0 - 1	0
pwron	Enable SDRAM at power-on.	0 - 1	0
sdbits	32 or 64 -bit data bus width.	32, 64	32
edacen	EDAC enable. If set to one, EDAC logic will be included in the synthesized design. An EDAC configuration register will also be available.	0 - 1	0
errcnt	Include an single error counter which is accessible from the EDAC configuration register.	0 - 1	0
cntbits	Number of bits used in the single error counter	1 - 8	1
pageburst	Enable SDRAM page burst operation. 0: Controller uses line burst of length 8 for read operations. 1: Controller uses pageburst for read operations. 2: Controller uses pageburst/line burst depending on PageBurst bit in SDRAM configuration register.	0 - 2	0
mobile	Enable Mobile SDRAM support 0: Mobile SDRAM support disabled 1: Mobile SDRAM support enabled but not default 2: Mobile SDRAM support enabled by default 3: Mobile SDRAM support only (no regular SDR support)	0 - 3	0

28.7 Signal descriptions

Table 316 shows the interface signals of the core (VHDL ports).

*Table 316.*Signals declarations

Signal name	Field	Type	Function	Active
CLK	N/A	Input	Clock	-
RST	N/A	Input	Reset	Low
AHBSI	*	Input	AHB slave input signals	-
AHBSO	*	Output	AHB slave output signals	-
SDI	WPROT	Input	Not used	-
	DATA[63:0]	Input	Data	-
	CB[7:0]	Input	Checkbits	-
SDO	SDCKE[1:0]	Output	SDRAM clock enable	High
	SDCSN[1:0]	Output	SDRAM chip select	Low
	SDWEN	Output	SDRAM write enable	Low
	RASN	Output	SDRAM row address strobe	Low
	CASN	Output	SDRAM column address strobe	Low
	DQM[7:0]	Output	SDRAM data mask: DQM[7] corresponds to DATA[63:56], DQM[6] corresponds to DATA[55:48], DQM[5] corresponds to DATA[47:40], DQM[4] corresponds to DATA[39:32], DQM[3] corresponds to DATA[31:24], DQM[2] corresponds to DATA[23:16], DQM[1] corresponds to DATA[15:8], DQM[0] corresponds to DATA[7:0]. Any DQM[ ] signal can be used for CB[ ].	Low
	BDRIVE	Output	Drive SDRAM data bus	Low
	ADDRESS[16:2]	Output	SDRAM address	-
	DATA[31:0]	Output	SDRAM data	-
	CB[7:0]	Output	Checkbits	-
	CE	Output	Correctable Error	High

* see GRLIB IP Library User's Manual

28.8 Signal definitions and reset values

The signals and their reset values are described in table 317.

*Table 317.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
sa[14:0]	Output	SDRAM address	High	Undefined
sd[31:0]	Input/Output	SDRAM data	High	Tri-state
scb[15:0]	Input/Output	SDRAM check bits	High	Tri-state
sdcsn[1:0]	Output	SDRAM chip select	Low	Logical 1
sdwen	Output	SDRAM write enable	Low	Logical 1
sdrasn	Output	SDRAM row address strobe	Low	Logical 1
sdcasn	Output	SDRAM column address strobe	Low	Logical 1
sddqm[3:0]	Output	SDRAM data mask: sddqm[3] corresponds to sd[31:24], sddqm[2] corresponds to sd[23:16], sddqm[1] corresponds to sd[15:8], sddqm[0] corresponds to sd[7:0]. Any sddqm[] signal can be used for scb[ ].	Low	Logical 1

28.9 Timing

The timing waveforms and timing parameters are shown in figure 86 and are defined in table 318.

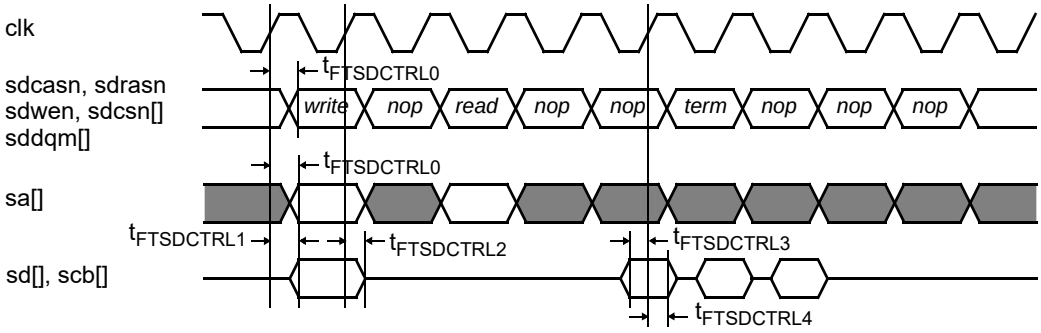


Figure 86. Timing waveforms

*Table 318.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{FTSDCTRL0}$	clock to output delay	rising *clk* edge	TBD	TBD	ns
$t_{FTSDCTRL1}$	clock to data output delay	rising *clk* edge	TBD	TBD	ns
$t_{FTSDCTRL2}$	data clock to data tri-state delay	rising *clk* edge	TBD	TBD	ns
$t_{FTSDCTRL3}$	data input to clock setup	rising *clk* edge	TBD	-	ns
$t_{FTSDCTRL4}$	data input from clock hold	rising *clk* edge	TBD	-	ns

28.10 Library dependencies

Table 5 shows libraries used when instantiating the core (VHDL libraries).

*Table 319.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AHB signal definitions
GAISLER	MEMCTRL	Signals, component	Memory bus signals definitions, component declaration

28.11 Instantiation

This example shows how the core can be instantiated.

The example design contains an AMBA bus with a number of AHB components connected to it including the FT SDRAM controller. The external SDRAM bus is defined in the example designs port map and connected to the SDRAM controller. System clock and reset are generated by GR Clock Generator and Reset Generator. It is also shown how the correctable error (CE) signal is connected to the ahb status register. It is not mandatory to connect this signal. In this example, 3 units can be connected to the status register.

The SDRAM controller decodes SDRAM area: 0x60000000 - 0x6FFFFFFF. SDRAM Configuration and EDAC configuration registers are mapped into AHB I/O space on address (AHB I/O base address + 0x100).

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.memctrl.all;
use gaisler.pads.all;   -- used for I/O pads
use gaisler.misc.all;

entity mctrl_ex is
  port (
    clk : in std_ulogic;
    resetn : in std_ulogic;
    pllref : in  std_ulogic;
    ... -- other signals

-- sdram memory bus
    sdcke    : out std_logic_vector ( 1 downto 0);  -- clk en
    sdcsn    : out std_logic_vector ( 1 downto 0);  -- chip sel
    sdwen    : out std_logic;                       -- write en
    sdrasn   : out std_logic;                       -- row addr stb
    sdcasn   : out std_logic;                       -- col addr stb
    sddqm    : out std_logic_vector (7 downto 0);  -- data i/o mask
    sdclk    : out std_logic;                       -- sdram clk output
    sa       : out std_logic_vector(14 downto 0); -- optional sdram address
    sd       : inout std_logic_vector(63 downto 0); -- optional sdram data
    cb       : inout std_logic_vector(7 downto 0) --EDAC checkbits
    );
end;

architecture rtl of mctrl_ex is

  -- AMBA bus (AHB and APB)
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbsi : ahb_slv_in_type;
  signal ahbso : ahb_slv_out_vector := (others => ahbs_none);
  signal ahbmi : ahb_mst_in_type;
```

```
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);

  -- signals used to connect SDRAM controller and SDRAM memory bus
  signal sdi   : sdctrl_in_type;
  signal sdo   : sdctrl_out_type;

  signal clkm, rstn : std_ulogic; -- system clock and reset
signal ce : std_logic_vector(0 to 2); --correctable error signal vector

-- signals used by clock and reset generators
  signal cgi : clkgen_in_type;
  signal cgo : clkgen_out_type;

  signal gnd : std_ulogic;

begin

  -- AMBA Components are defined here ...
  ...

  -- Clock and reset generators
  clkgen0 : clkgen generic map (clk_mul => 2, clk_div => 2, sdramen => 1,
                                tech => virtex2, sdinvclk => 0)
  port map (clk, gnd, clkm, open, open, sdclk, open, cgi, cgo);

  cgi.pllctrl <= "00"; cgi.pllrst <= resetn; cgi.pllref <= pllref;

  rst0 : rstgen
  port map (resetn, clkm, cgo.clklock, rstn);

  -- AHB Status Register
  astat0 : ahbstat generic map(pindex => 13, paddr => 13, pirq => 11,
    nftslv => 3)
    port map(rstn, clkm, ahbmi, ahbsi, ce, apbi, apbo(13));

  -- SDRAM controller
  sdc : ftsdctrl generic map (hindex => 3, haddr => 16#600#, hmask => 16#F00#,
    ioaddr => 1, fast => 0, pwron => 1, invclk => 0, edacen => 1, errcnt => 1,
    cntbits => 4)
    port map (rstn, clkm, ahbsi, ahbso(3), sdi, sdo, ce(0));

  -- input signals
  sdi.data(31 downto 0) <= sd(31 downto 0);

  -- connect SDRAM controller outputs to entity output signals
  sa <= sdo.address; sdcke <= sdo.sdcke; sdwen <= sdo.sdwen;
  sdcsn <= sdo.sdcsn; sdrasn <= sdo.rasn; sdcasn <= sdo.casn;
  sddqm <= sdo.dqm;

  -- I/O pads driving data bus signals
  sd_pad : iopadv generic map (width => 32)
      port map (sd(31 downto 0), sdo.data, sdo.bdrive, sdi.data(31 downto 0));

  -- I/O pads driving checkbit signals
  cb_pad : iopadv generic map (width => 8)
      port map (cb, sdo.cb, sdo.bdrive, sdi.cb);


end;
```

28.12 Constraints

This section contains example constraints for the SDRAM controller.

```
###### SDRAM interface
###

set sdram_freq 100.0
set sdram_clkper [ expr { 1000.0 / $sdram_freq } ]
```

```
create_clock -name "c_memclk" -period $sdram_clkper [get_ports "mem_clk"]

set sdram_cmd_ports [get_ports {mem_wen mem_rasn mem_cke mem_casn mem_ba mem_addr[12]
mem_addr[11] mem_addr[10] mem_addr[9] mem_addr[8] mem_addr[7] mem_addr[6] mem_addr[5]
mem_addr[4] mem_addr[3] mem_addr[2] mem_addr[1] mem_addr[0]}]
set sdram_cs_ports [get_ports {mem_sn*}]
set sdram_dq_ports [get_ports mem_dq]
set sdram_dqm_ports [get_ports mem_dqm]

# Use Micron datasheet values for SDRAM plus 1 ns margin for PCB propagation and other un-
modeled effects
set sdram_tAC 6.0
set sdram_tOHN 1.8
set sdram_ts_cmd 1.5
set sdram_th_cmd 0.8
set sdram_ts_cs 1.5
set sdram_th_cs 0.8
set sdram_ts_dq 1.5
set sdram_th_dq 0.8
set sdram_ts_dqm 1.5
set sdram_th_dqm 0.8

set_input_delay -clock "c_memclk" -min $sdram_tOHN $sdram_dq_ports
set_input_delay -clock "c_memclk" -max [expr { $sdram_tAC + 1.0 }] $sdram_dq_ports

set_output_delay -clock "c_memclk" -max [expr {$sdram_ts_cmd+1.0}] $sdram_cmd_ports
set_output_delay -clock "c_memclk" -min -$sdram_th_cmd $sdram_cmd_ports
set_output_delay -clock "c_memclk" -max [expr {$sdram_ts_cs+1.0}] $sdram_cs_ports
set_output_delay -clock "c_memclk" -min -$sdram_th_cs $sdram_cs_ports
set_output_delay -clock "c_memclk" -max [expr {$sdram_ts_dq+1.0}] $sdram_dq_ports
set_output_delay -clock "c_memclk" -min -$sdram_th_dq $sdram_dq_ports
set_output_delay -clock "c_memclk" -max [expr {$sdram_ts_dqm+1.0}] $sdram_dqm_ports
set_output_delay -clock "c_memclk" -min -$sdram_th_dqm $sdram_dqm_ports
```

29 FTSRCTRL - Fault Tolerant 32-bit PROM/SRAM/IO Controller

29.1 Overview

The fault tolerant 32-bit PROM/SRAM memory interface uses a common 32-bit memory bus to interface PROM, SRAM and I/O devices. Support for 8-bit PROM banks can also be separately enabled. In addition it also provides an Error Detection And Correction Unit (EDAC), correcting one and detecting two errors. Configuration of the memory controller functions is performed through the APB bus interface.

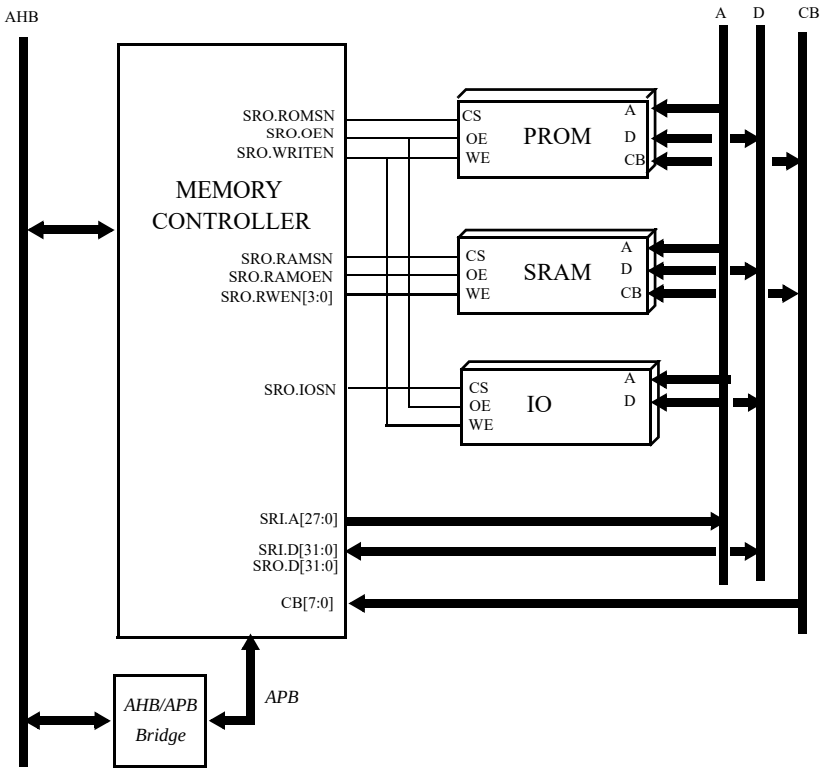


Figure 87. 32-bit FT PROM/SRAM/IO controller

29.2 Operation

The controller is configured through VHDL generics to decode three address ranges: PROM, SRAM and I/O area. By default the PROM area is mapped into address range 0x0 - 0x00FFFFFF, the SRAM area is mapped into address range 0x40000000 - 0x40FFFFFF, and the I/O area is mapped to 0x20000000 - 0x20FFFFFF.

One chip select is decoded for the I/O area, while SRAM and PROM can have up to 8 chip select signals. The controller generates both a common write-enable signal (WRITEN) as well as four byte-write enable signals (WREN). If the SRAM uses a common write enable signal the controller can be configured to perform read-modify-write cycles for byte and half-word write accesses. Number of waitstates is separately configurable for the three address ranges.

The EDAC function is optional, and can be enabled with the *edacen* VHDL generic. The configuration of the EDAC is done through a configuration register accessed from the APB bus. During nominal operation, the EDAC checksum is generated and checked automatically. Single errors are corrected without generating any indication of this condition in the bus response. If a multiple error is detected, a two cycle error response is given on the AHB bus.

Single errors can be monitored in two ways:

- by monitoring the CE signal which is asserted for one cycle each time a single error is detected.
- by checking the single error counter which is accessed from the MCFG3 configuration register.

The CE signal can be connected to the AHB status register which stores information of the AHB instruction causing the error and also generates interrupts. See the AHB status register documentation for more information. When EDAC is enabled, one extra latency cycle is generated during reads and subword writes.

The EDAC function can be enabled for SRAM and PROM area accesses, but not for I/O area accesses. For the SRAM area, the EDAC functionality is only supported for accessing 32-bit wide SRAM banks. For the PROM area, the EDAC functionality is supported for accessing 32-bit wide PROM banks, as well as for read accesses to 8-bit wide PROM banks.

The equations below show how the EDAC checkbits are generated:

```
CB0 = D0 ^ D4 ^ D6 ^ D7 ^ D8 ^ D9 ^ D11 ^ D14 ^ D17 ^ D18 ^ D19 ^ D21 ^ D26 ^ D28 ^ D29 ^ D31
CB1 = D0 ^ D1 ^ D2 ^ D4 ^ D6 ^ D8 ^ D10 ^ D12 ^ D16 ^ D17 ^ D18 ^ D20 ^ D22 ^ D24 ^ D26 ^ D28
CB2 = D0 ^ D3 ^ D4 ^ D7 ^ D9 ^ D10 ^ D13 ^ D15 ^ D16 ^ D19 ^ D20 ^ D23 ^ D25 ^ D26 ^ D29 ^ D31
CB3 = D0 ^ D1 ^ D5 ^ D6 ^ D7 ^ D11 ^ D12 ^ D13 ^ D16 ^ D17 ^ D21 ^ D22 ^ D23 ^ D27 ^ D28 ^ D29
CB4 = D2 ^ D3 ^ D4 ^ D5 ^ D6 ^ D7 ^ D14 ^ D15 ^ D18 ^ D19 ^ D20 ^ D21 ^ D22 ^ D23 ^ D30 ^ D31
CB5 = D8 ^ D9 ^ D10 ^ D11 ^ D12 ^ D13 ^ D14 ^ D15 ^ D24 ^ D25 ^ D26 ^ D27 ^ D28 ^ D29 ^ D30 ^ D31
CB6 = D0 ^ D1 ^ D2 ^ D3 ^ D4 ^ D5 ^ D6 ^ D7 ^ D24 ^ D25 ^ D26 ^ D27 ^ D28 ^ D29 ^ D30 ^ D31
```

29.2.1 8-bit PROM access

The FTSRCTRL controller can be configured to access an 8-bit wide PROM. The data bus of the external PROM should be connected to the upper byte of the 32-bit data bus, i.e. D[31:24]. The 8-bit mode is enabled with the prom8en VHDL generic. When enabled, read accesses to the PROM area will be done in four-byte bursts for all 32-, 16- and 8-bit AMBA AHB accesses. The whole 32-bit word is then output on the AHB data bus, allowing the master to chose the bytes needed (big-endian).

Writes should be done one byte at a time. For correct word aligned 32-bit word write accesses, the byte should always be driven on bits 31 to 24 on the AHB data bus. For non-aligned 32-bit word write accesses, the byte should be driven on the bits of the AHB data bus that correspond to the byte address (big-endian). For correct half-word aligned 16-bit half-word write accesses, the byte should always be driven on bits 31 to 24, or 15 to 8, on the AHB data bus. For non-aligned 16-bit half-word write accesses, the byte should be driven on the bits of the AHB data bus that correspond to the byte address (big-endian). For 8-bit word write accesses the byte should always be driven on the AHB data bus bits that corresponds to the byte address (big-endian). To summarize, all legal AMBA AHB write accesses are supported according to the AMBA standard, additional illegal accesses are supported as described above, and it is always the addressed byte that is output.

It is possible to dynamically switch between 8- and 32-bit PROM mode by writing to the RBW field of the MCFG1 register. The BWIDTH[1:0] input signal determines the reset value of this RBW register field. When RBW is “00” then 8-bit mode is selected. If RBW is “10” then 32-bit mode is selected. Other RBW values are reserved for future use. SRAM access is not affected by the 8-bit PROM mode.

It is also possible to use the EDAC in the 8-bit PROM mode, configured by the edacen VHDL generic, and enabled via the MCFG3 register. Read accesses to the 8-bit PROM area will be done in five-byte bursts for all 32-, 16- and 8-bit AMBA AHB accesses. After a potential correction, the whole 32-bit word is output on the AHB data bus, allowing the master to chose the bytes needed (big-endian). EDAC support is not provided for write accesses, they are instead performed in the same way as without the EDAC enabled. The checksum byte must be written by the user into the correct byte address location.

The fifth byte corresponds to the EDAC checksum and is located in the upper part of the effective memory area, as explained in detail in the definition of the MCFG1 memory configuration register. The EDAC checksums are located in the upper quarter of what is defined as available EDAC area by means of the EBSZ field and the ROMBSZ field or rombanksz VHDL generic. When set to 0, the size

of the available EDAC area is defined as the PROM bank size. When set to 1, as twice the PROM bank size. When set to 2, as four times the PROM bank size. And when set to 3, as eight times the PROM bank size. For any other value than 0, the use of multiple PROM banks is required.

Example, if ROMBSZ=10 and EBSZ=1, the EDAC area is 8KiB*2^ROMBSZ*2^EBSZ= 16MiB=0x01000000. The checksum byte for the first word located at address 0x00000000 to 0x00000003 is located at 0x00C00000. The checksum byte for the second word located at address 0x00000004 to 0x00000007 is located at 0x00C00001, and so on. Since EBSZ=1, two PROM banks are required for implementing the EDAC area, each bank with size 8MiB=0x00800000.

29.2.2 Access errors

The active low Bus Exception signal (BEXCN) can be used to signal access errors. It is enabled by setting the BEXCEN bit in MCFG1 and is active for all types of accesses to all areas (PROM, SRAM and I/O). The BEXCN signal is sampled on the same cycle as read data is sampled. For writes it is sampled on the last rising edge before writen/rwen is de-asserted (writen and rwen are clocked on the falling edge). When a bus exception is detected an error response will be generated for the access.

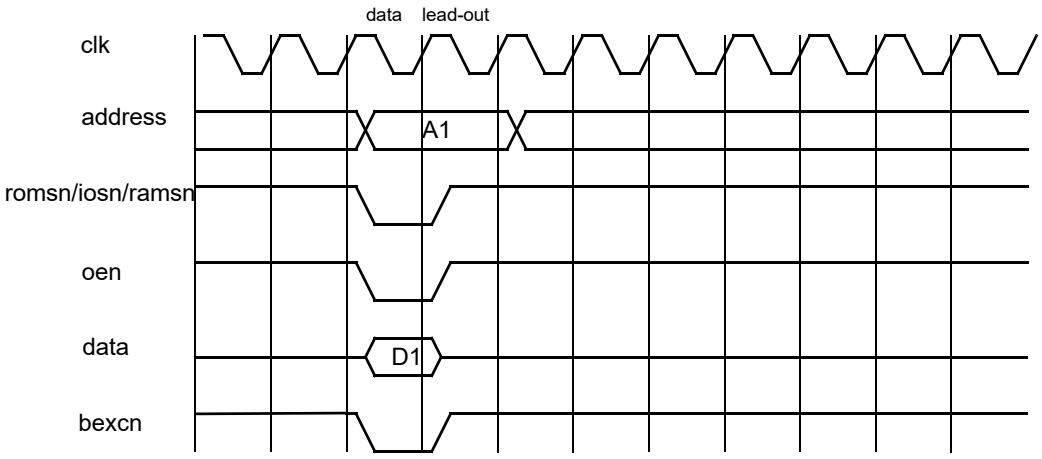


Figure 88. Read cycle with BEXCN.

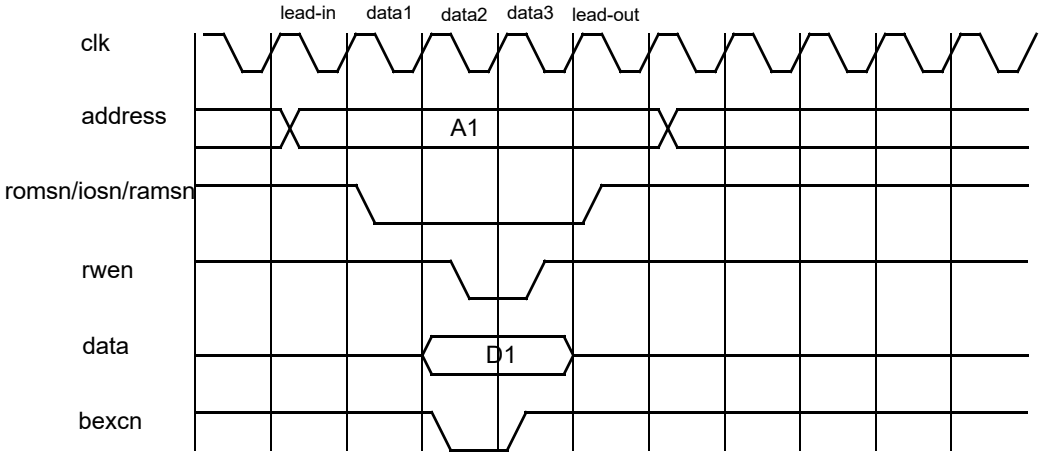


Figure 89. Write cycle with BEXCN.

29.2.3 Using bus ready signalling

The Bus Ready (BRDYN) signal can be used to add waitstates to I/O-area accesses, covering the complete memory area and both read and write accesses. It is enabled by setting the Bus Ready

Enable (BRDYEN) bit in the MCFG1 register. An access will have at least the amount of waitstates set with the VHDL generic or through the register, but will be further stretched until BRDYN is asserted. Additional waitstates can thus be inserted after the pre-set number of waitstates by de-asserting the BRDYN signal. BRDYN should be asserted in the cycle preceding the last one. It is recommended that BRDYN remains asserted until the IOSN signal is de-asserted, to ensure that the access has been properly completed and avoiding the system to stall. Read accesses will have the same timing as when EDAC is enabled while write accesses will have the timing as for single accesses even if bursts are performed.

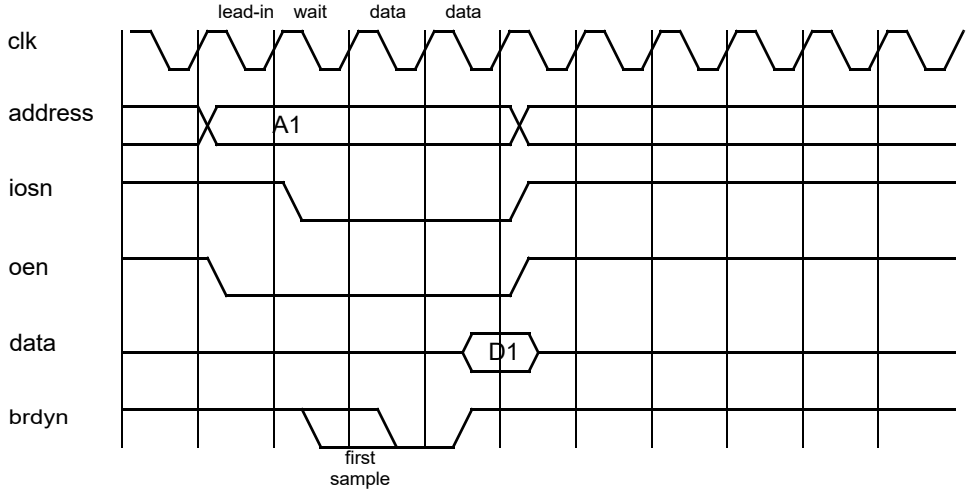


Figure 90. I/O READ cycle, programmed with 1 wait state, and with an extra data cycle added with BRDYN.

29.3 PROM/SRAM/IO waveforms

The internal and external waveforms of the interface are presented in the figures hereafter.

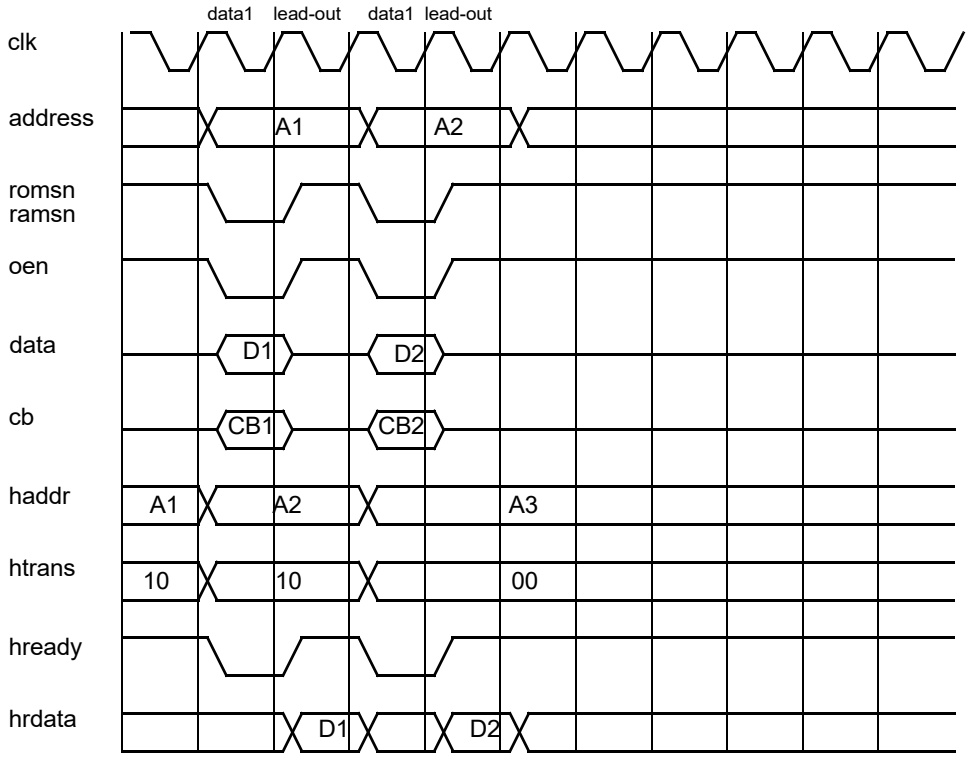


Figure 91. PROM/SRAM non-consecutive read cyclecs.

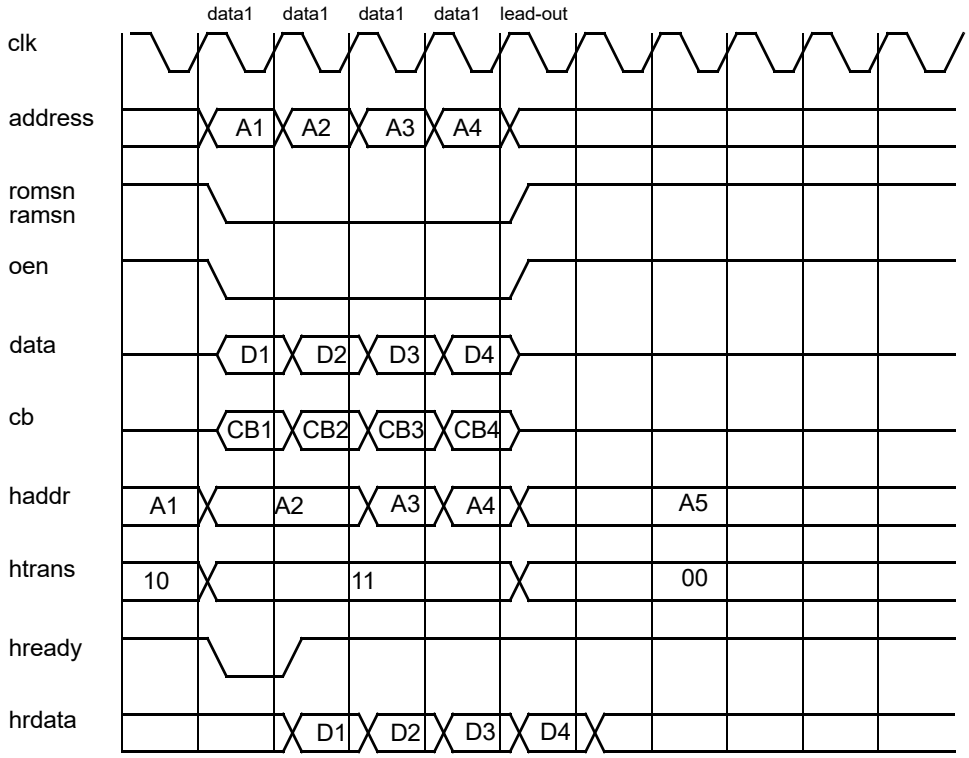


Figure 92. 32-bit PROM/SRAM sequential read access with 0 wait-states and EDAC disabled.

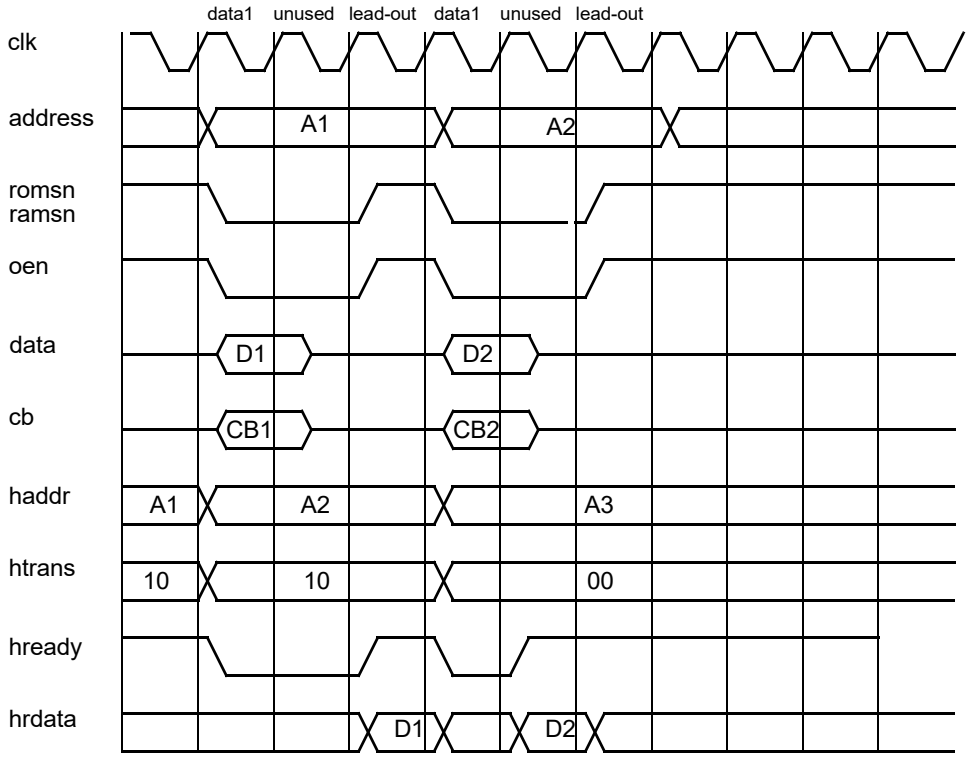


Figure 93. 32-bit PROM/SRAM non-sequential read access with 0 wait-states and EDAC enabled.

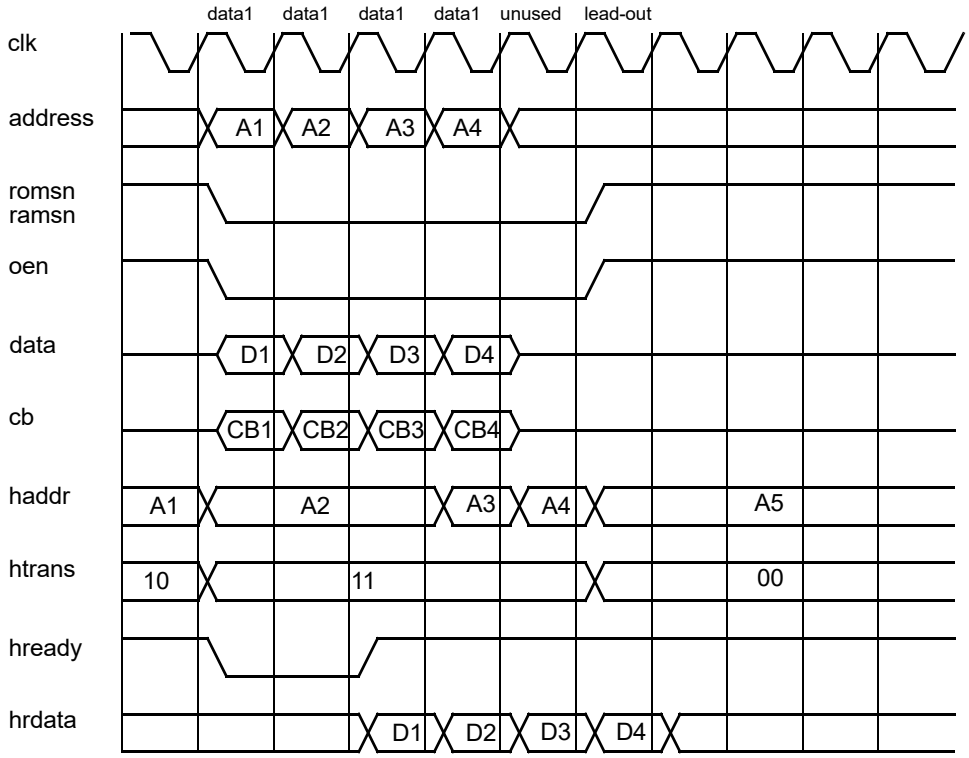


Figure 94. 32-bit PROM/SRAM sequential read access with 0 wait-states and EDAC enabled..

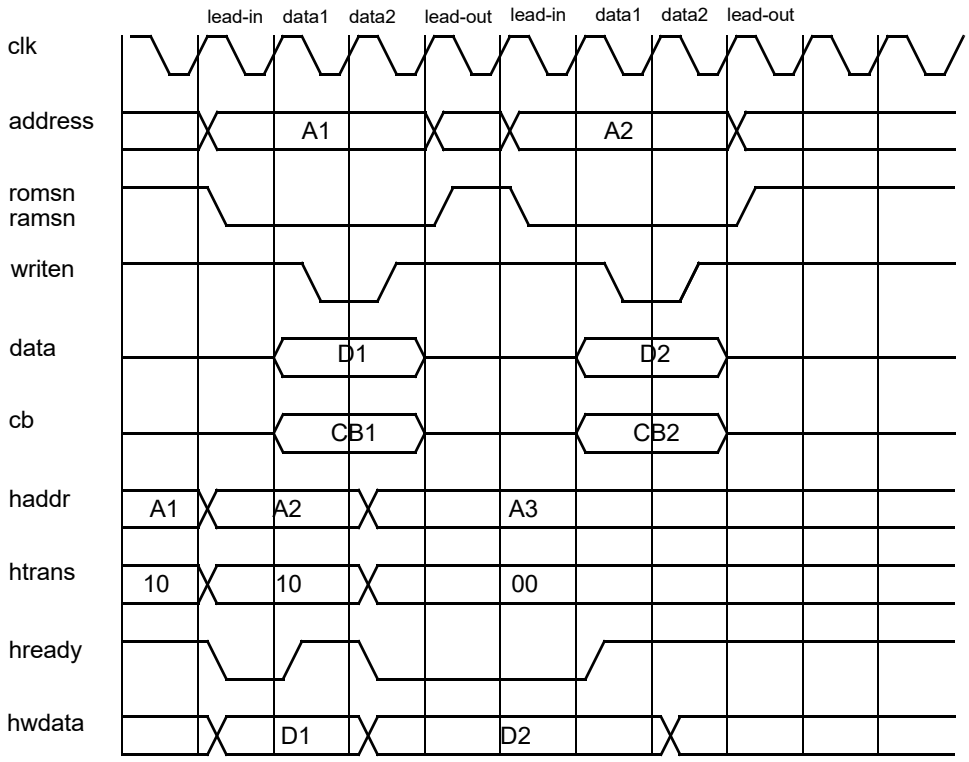


Figure 95. 32-bit PROM/SRAM non-sequential write access with 0 wait-states and EDAC disabled.

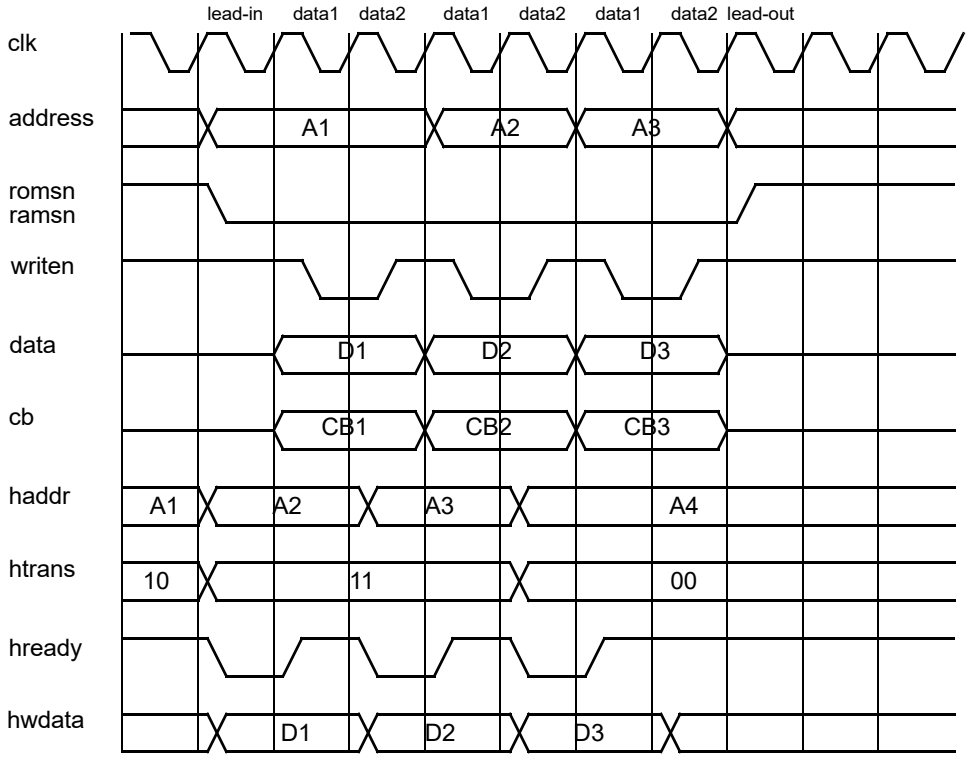


Figure 96. 32-bit PROM/SRAM sequential write access with 0 wait-states and EDAC disabled.

If waitstates are configured through the VHDL generics or registers, one extra data cycle will be inserted for each waitstate in both read and write cycles. The timing for write accesses is not affected when EDAC is enabled while one extra latency cycle is introduced for single access reads and at the beginning of read bursts.

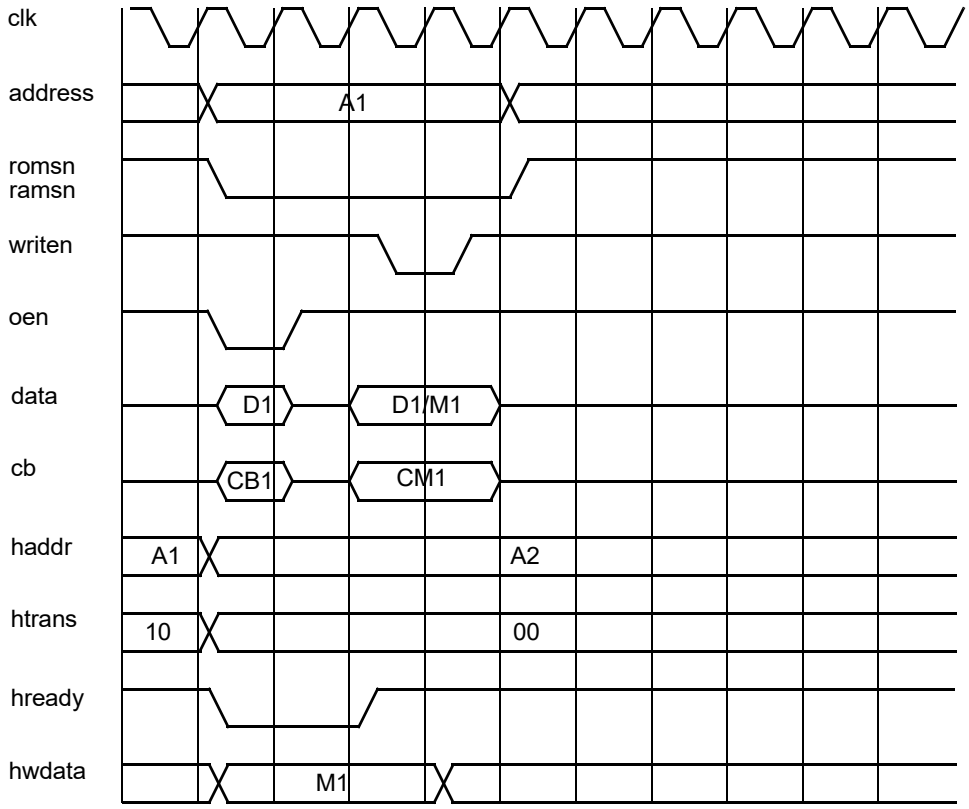


Figure 97. 32-bit PROM/SRAM rmw access with 0 wait-states and EDAC disabled.

Read-Modify-Write (RMW) accesses will have an additional waitstate inserted to accommodate decoding when EDAC is enabled.

I/O accesses are similar to PROM and SRAM accesses but a lead-in and lead-out cycle is always present.

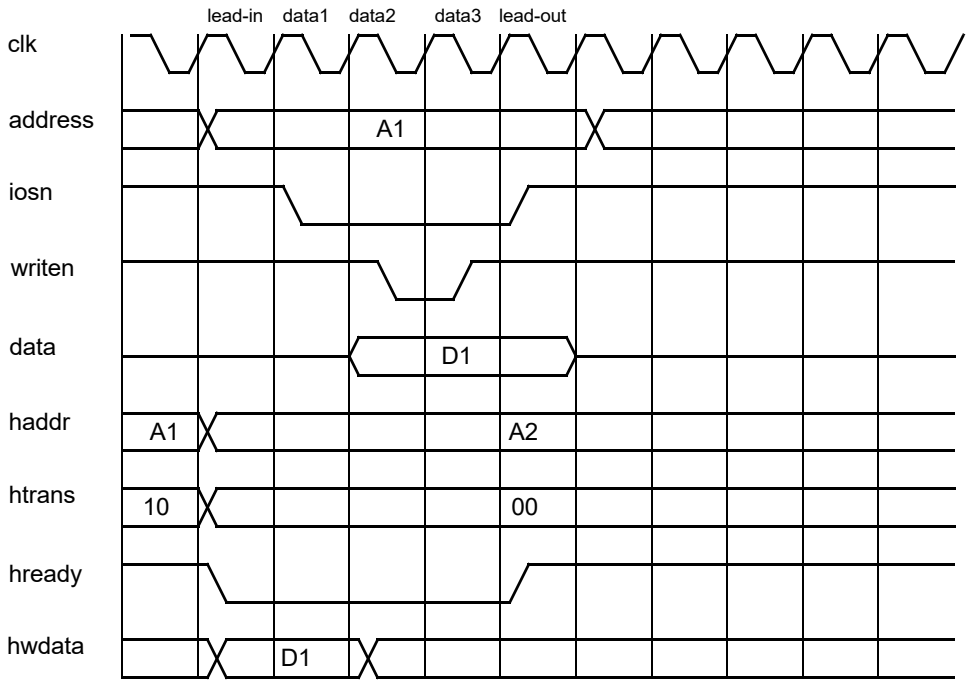


Figure 98. I/O write access with 0 wait-states.

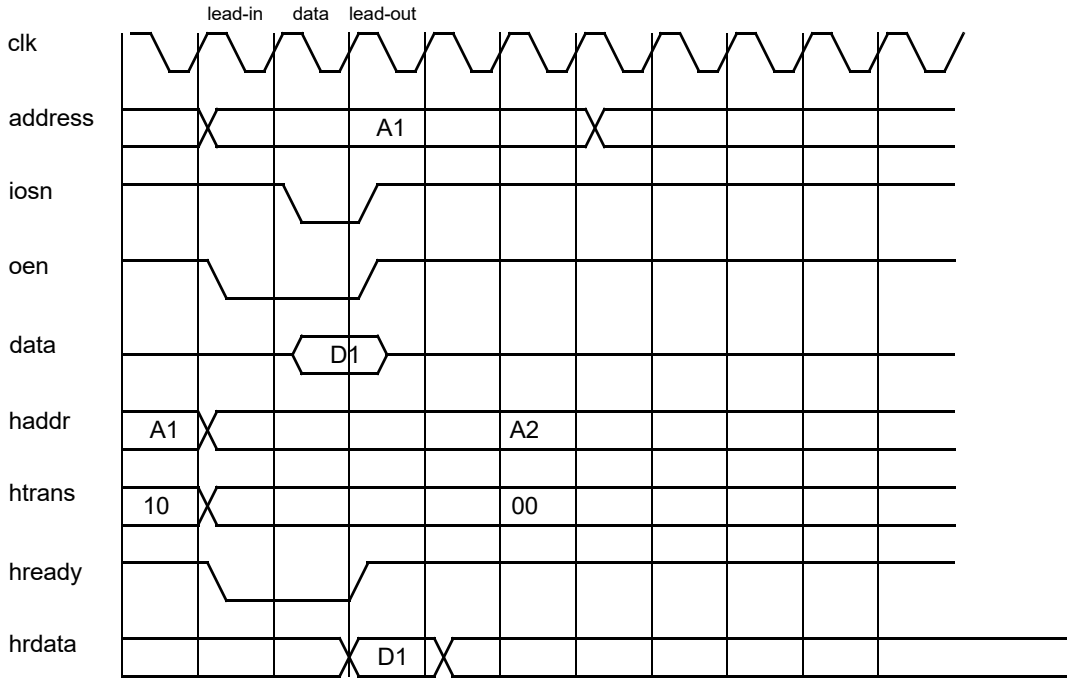


Figure 99. I/O read access with 0 wait-states

29.4 Endianness

The core is designed for big-endian systems.

29.5 Registers

The core is programmed through registers mapped into APB address space.

*Table 320.*FT PROM/SRAM/IO controller registers

APB Address offset	Register
0x0	Memory configuration register 1
0x4	Memory configuration register 2
0x8	Memory configuration register 3

29.5.1 Memory Configuration Register 1

*Table 321.*0x00 - MCFG1 - Memory configuration register 1.

31 27	26	25	24	23 20	19 18	17 14	13 12	11	10	9 8	7 4	3 0
RESERVED	BR	BE	R	IOWS	R	ROMBSZ	EBSZ	RW	R	RBW	RESERVED	ROMWS
0	0	0	0	0	0	*	*	0	0	*	0	0xF
r	rw	rw	r	rw	r	rw*	rw*	rw	r	rw	r	rw

31: 27 RESERVED

26 Bus ready enable (BR) - Enables the bus ready signal (BRDYN) for I/O-area.

25 Bus exception enable (BE) - Enables the bus exception signal (BEXCEN) for PROM, SRAM and I/O areas

24 RESERVED

23: 20 I/O wait states (IOWS) - Sets the number of waitstates for accesses to the I/O-area. Only available if the wsreg VHDL generic is set to one.

19: 18 RESERVED

17: 14 ROM bank size (ROMBSZ) - Sets the PROM bank size. Only available if the rombanksz VHDL generic is set to zero. Otherwise, the rombanksz VHDL generic sets the bank size and the value can be read from this field. 0 = 8KiB, 1 = 16KiB, 2 = 32KiB, 3 = 64KiB, ..., 15=256 MiB (i.e. 8 KiB * 2**ROMBSZ).

13: 12 EDAC bank size (EBSZ) - Sets the EDAC bank size for 8-bit PROM support. Only available if the rombanksz VHDL generic is zero, and edacen and prom8en VHDL generics are one. Otherwise, the value is fixed to 0. The resulting EDAC bank size is 2^EBSZ * 2^ROMBSZ * 8KiB. Note that only the three lower quarters of the bank can be used for user data. The EDAC checksums are placed in the upper quarter of the bank.

11 ROM write enable (RW) - Enables writes to the PROM memory area. When disabled, writes to the PROM area will generate an ERROR response on the AHB bus.

10 RESERVED

9: 8 ROM data bus width (RBW) - Sets the PROM data bus width. “00” = 8-bit, “10” = 32-bit, others reserved.

7: 4 RESERVED

3: 0 ROM waitstates (ROMWS) - Sets the number of waitstates for accesses to the PROM area. Reset to all-ones. Only available if the wsreg generic is set to one.

29.5.2 Memory Configuration Register 2

*Table 322.*0x04 - MCFG2 - Memory configuration register 2.

31 13	12 9	8	7	6	5 2	1 0
RESERVED	RAMBSZ	R	RW	RESERVED	RAMW	
0	*	0	*	0	0	
r	rw*	r	rw*	r	rw*	

31: 13 RESERVED

12: 9 RAM bank size (RAMBSZ) - Sets the RAM bank size. Only available if the banksz VHDL generic is set to zero. Otherwise, the banksz VHDL generic sets the bank size and the value can be read from this field. 0 = 8KiB, 1 = 16KiB, 2 = 32KiB, 3 = 64KiB, ..., 15=256 MiB (i.e. 8 KiB * 2**RAMBSZ)

8: 7 RESERVED

6 Read-modify-write enable (RW) - Enables read-modify-write cycles for write accesses. Only available if the rmw VHDL generic is set to one.

5: 2 RESERVED

1: 0 RAM waitstates (RAMW) - Sets the number of waitstates for accesses to the RAM area. Only available if the wsreg VHDL generic is set to one.

29.5.3 Memory Configuration Register 3

*Table 323.*0x08 - MCFG3 - Memory configuration register 3.

31 20	19 12	11	10	9	8	7 0
RESERVED	SEC	WB	RB	SE	PE	TCB
0	0	0	0	0	0	NR
r	wc	rw	rw	rw	rw	rw*

31: 20	RESERVED
19: 12	Single error counter.(SEC) - This field increments each time a single error is detected until the maximum value that can be stored in the field is reached. Each bit can be reset by writing a one to it.
11	Write bypass (WB) - Enables EDAC write bypass. When enabled the TCB field will be used as checkbits in all write operations.
10	Read bypass (RB) - Enables EDAC read bypass. When enabled checkbits read from memory in all read operations will be stored in the TCB field.
9	SRAM EDAC enable (SE) - Enables EDAC for the SRAM area.
8	PROM EDAC enable (PE) - Enables EDAC for the PROM area. Reset value is taken from the input signal sri.edac.
7: 0	Test checkbits (TCB) - Used as checkbits in write operations when WB is activated and checkbits from read operations are stored here when RB is activated.

All the fields in MCFG3 register are available if the edacen VHDL generic is set to one except SEC field which also requires that the errcnt VHDL generic is set to one. The exact breakpoint between the SEC and RESERVED field depends on the cntbits generic. The breakpoint is 11+cntbits. The values shown in the table is for maximum cntbits value 8.

29.6 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x051. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

29.7 Implementation

29.7.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers. The registers driving external chip select, output enable and output enables for the data bus have asynchronous reset.

29.8 Configuration options

Table 320 shows the configuration options of the core (VHDL generics).

Table 324. Controller configuration options

Generic	Function	Allowed range	Default
hindex	AHB slave index.	1 - NAHBSLV-1	0
romaddr	ADDR field of the AHB BAR0 defining PROM address space. Default PROM area is 0x0 - 0xFFFFFF.	0 - 16#FFF#	16#000#
rommask	MASK field of the AHB BAR0 defining PROM address space.	0 - 16#FFF#	16#FF0#
ramaddr	ADDR field of the AHB BAR1 defining RAM address space. Default RAM area is 0x40000000-0x40FFFFFF.	0 - 16#FFF#	16#400#
rammask	MASK field of the AHB BAR1 defining RAM address space.	0 -16#FFF#	16#FF0#
ioaddr	ADDR field of the AHB BAR2 defining IO address space. Default RAM area is 0x20000000-0x20FFFFFF.	0 - 16#FFF#	16#200#
iomask	MASK field of the AHB BAR2 defining IO address space.	0 - 16#FFF#	16#FF0#
ramws	Number of waitstates during access to SRAM area.	0 - 15	0
romws	Number of waitstates during access to PROM area.	0 - 15	2
iows	Number of waitstates during access to IO area.	0 - 15	2
rmw	Enable read-modify-write cycles.	0 - 1	0
srbanks	Set the number of RAM banks.	1 - 8	1
banksz	Set the size of bank 1 - 4. 1 = 16KiB, 2 = 32KiB, 3 = 64KiB, ... , 15 = 256 MiB (i.e. 8 KiB * 2**banksz). If set to zero, the bank size is set with the rambsz field in the MCFG2 register.	0 - 15	15
rombanks	Sets the number of PROM banks available.	1 - 8	1
rombanksz	Sets the size of one PROM bank. 1 = 16KiB, 2 = 32KiB, 3 = 64KiB, ... , 15 = 256 MiB (i.e. 8 KiB * 2**rombanksz). If set to zero, the bank size is set with the rombsz field in the MCFG1 register.	0 - 15	15
rombankszdef	Sets the reset value of the rombsz register field in MCFG1 if available.	0 - 15	15
pindex	APB slave index.	1 - NAPBSLV-1	0
paddr	APB address.	1 - 16#FFF#	0
pmask	APB address mask.	1 - 16#FFF#	16#FFF#
edacen	EDAC enable. If set to one, EDAC logic is synthesized.	0 - 1	0
errcnt	If one, a single error counter is added.	0 - 1	0
cntbits	Number of bits in the single error counter.	1 - 8	1
wsreg	Enable programmable waitstate generation.	0 - 1	0
prom8en	Enable 8-bit PROM mode.	0 - 1	0
oepol	Select polarity of output enable signals. 0 = active low, 1 = active high.	0 - 1	0

29.9 Signal descriptions

Table 325 shows the interface signals of the core (VHDL ports).

*Table 325.*Signal descriptions

Signal name	Field	Type	Function	Active
CLK	N/A	Input	Clock	-
RST	N/A	Input	Reset	Low

*Table 325.*Signal descriptions

Signal name	Field	Type	Function	Active
SRI	DATA[31:0]	Input	Memory data	High
	BRDYN	Input	Bus ready strobe	Low
	BEXCN	Input	Bus exception	Low
	WRN[3:0]	Input	Not used	-
	BWIDTH[1:0]	Input	Sets the reset value of the PROM data bus width field in the MCFG1 register	-
	SD[31:0]	Input	Not used	-
	CB[7:0]	Input	Checkbits	-
	PROMDATA[31:0]	Input	Not used	-
	EDAC	Input	The reset value for the PROM EDAC enable bit	High

*Table 325.*Signal descriptions

Signal name	Field	Type	Function	Active
SRO	ADDRESS[31:0]	Output	Memory address	High
	DATA[31:0]	Output	Memory data	High
	RAMSN[7:0]	Output	SRAM chip-select	Low
	RAMOEN[7:0]	Output	SRAM output enable	Low
	IOSN	Output	IO area chip select	Low
	ROMSN[7:0]	Output	PROM chip-select	Low
	OEN	Output	Output enable	Low
	WRITEN	Output	Write strobe	Low
	WRN[3:0]	Output	SRAM write enable: WRN[0] corresponds to DATA[31:24], WRN[1] corresponds to DATA[23:16], WRN[2] corresponds to DATA[15:8], WRN[3] corresponds to DATA[7:0]. Any WRN[ ] signal can be used for CB[ ].	Low
	MBEN[3:0]	Output	Byte enable: MBEN[0] corresponds to DATA[31:24], MBEN[1] corresponds to DATA[23:16], MBEN[2] corresponds to DATA[15:8], MBEN[3] corresponds to DATA[7:0]. Any MBEN[ ] signal can be used for CB[ ].	
	BDRIVE[3:0]	Output	Drive byte lanes on external memory bus.Controls I/O-pads connected to external memory bus: BDRIVE[0] corresponds to DATA[31:24], BDRIVE[1] corresponds to DATA[23:16], BDRIVE[2] corresponds to DATA[15:8], BDRIVE[3] corresponds to DATA[7:0]. Any BDRIVE[ ] signal can be used for CB[ ].	Low
	READ	Output	Read strobe	High
	RAMN	Output	Common SRAM Chip Select. Always asserted when one of the 8 RAMSN signals is asserted.	Low
	ROMN	Output	Common PROM Chip Select. Always asserted when one of the 8 ROMSN signals is asserted.	Low
	SA[14:0]	Output	Not used	-
	CB[7:0]	Output	Checkbits	-
	PSEL	Output	Not used	-
	CE	Output	Single error detected.	High
AHBSI	*	Input	AHB slave input signals	-
AHBSO	*	Output	AHB slave output signals	-
SDO	SDCASN	Output	Not used. All signals are drive to inactive state.	Low

* see GRLIB IP Library User's Manual

29.10 Signal definitions and reset values

The signals and their reset values are described in table 326.

*Table 326.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
address[27:0]	Output	Memory address	High	Undefined
data[31:0]	Input/Output	Memory data	High	Tri-state
cb[7:0]	Input/Output	Check bits	High	Tri-state
ramsn[3:0]	Output	SRAM chip select	Low	Logical 1
ramoen[3:0]	Output	SRAM output enable	Low	Logical 1
rwen[3:0]	Output,	SRAM write byte enable: rwen[0] corresponds to data[31:24], rwen[1] corresponds to data[23:16], rwen[2] corresponds to data[15:8], rwen[3] corresponds to data[7:0]. Any rwen[ ] signal can be used for cb[ ].	Low	Logical 1
ramben[3:0]	Output	SRAM read/write byte enable: ramben[0] corresponds to data[31:24], ramben[1] corresponds to data[23:16], ramben[2] corresponds to data[15:8], ramben[3] corresponds to data[7:0]. Any ramben[ ] signal can be used for cb[ ].	Low	Logical 1
oen	Output	Output enable	Low	Logical 1
writen	Output	Write strobe	Low	Logical 1
read	Output	Read strobe	High	Logical 1
iosn	Output	IO area chip select	Low	Logical 1
romsn[1:0]	Output	PROM chip select	Low	Logical 1
brdyn	Input	Bus ready. Extends accesses to the IO area.	Low	-
bexcn	Input	Bus exception.	Low	-

29.11 Timing

The timing waveforms and timing parameters are shown in figure 100 and are defined in table 327.

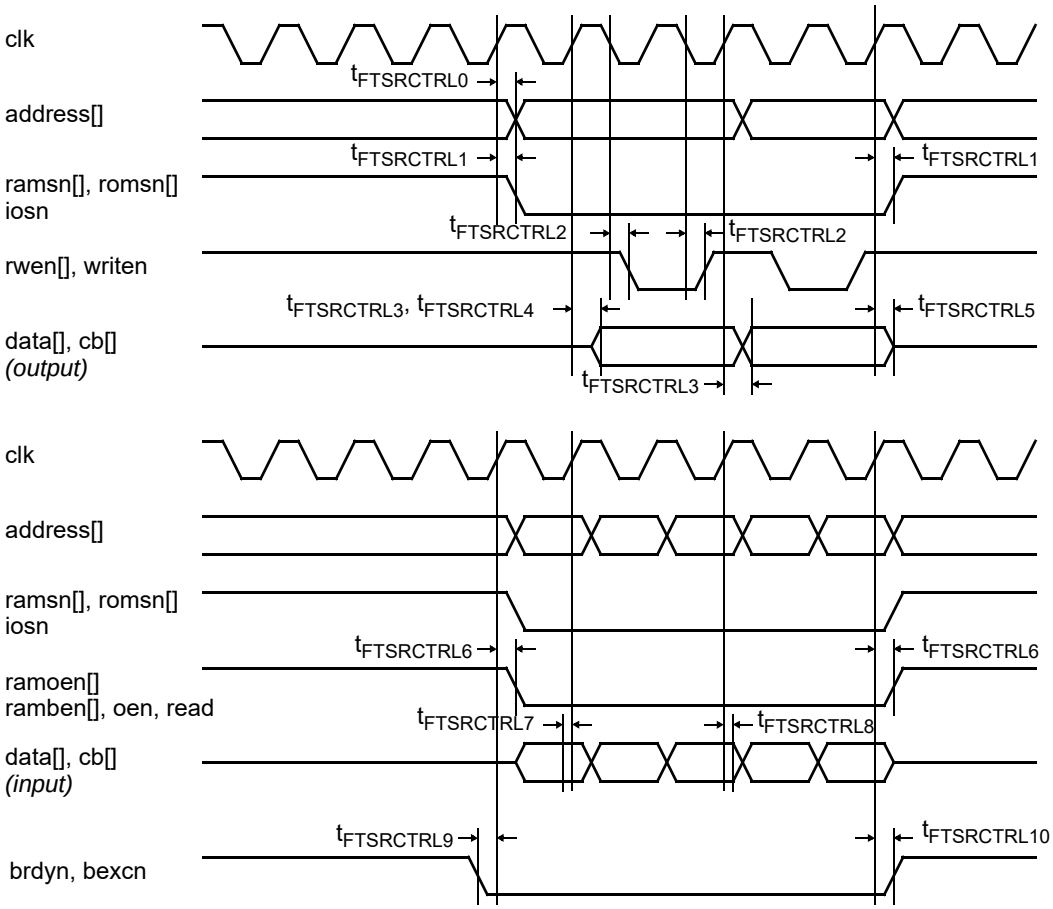


Figure 100. Timing waveforms

*Table 327.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{FTSRCTRL0}$	address clock to output delay	rising *clk* edge	TBD	TBD	ns
$t_{FTSRCTRL1}$	clock to output delay	rising *clk* edge	TBD	TBD	ns
$t_{FTSRCTRL2}$	clock to output delay	rising *clk* edge	TBD	TBD	ns
$t_{FTSRCTRL3}$	clock to data output delay	falling *clk* edge	TBD	TBD	ns
$t_{FTSRCTRL4}$	clock to data non-tri-state delay	rising *clk* edge	TBD	TBD	ns
$t_{FTSRCTRL5}$	clock to data tri-state delay	rising *clk* edge	TBD	TBD	ns
$t_{FTSRCTRL6}$	clock to output delay	rising *clk* edge	TBD	TBD	ns
$t_{FTSRCTRL7}$	data input to clock setup	rising *clk* edge	TBD	-	ns
$t_{FTSRCTRL8}$	data input from clock hold	rising *clk* edge	TBD	-	ns
$t_{FTSRCTRL9}$	input to clock setup	rising *clk* edge	TBD	-	ns
$t_{FTSRCTRL10}$	input from clock hold	rising *clk* edge	TBD	-	ns

29.12 Library dependencies

Table 328 shows libraries used when instantiating the core (VHDL libraries).

*Table 328.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AHB signal definitions
GAISLER	MEMCTRL	Signals, component	Memory bus signals definitions, component declaration

29.13 Component declaration

The core has the following component declaration.

```
component ftsrctrl is
  generic (
    hindex       : integer := 0;
    romaddr      : integer := 0;
    rommask      : integer := 16#ff0#;
    ramaddr      : integer := 16#400#;
    rammask      : integer := 16#ff0#;
    ioaddr       : integer := 16#200#;
    iomask       : integer := 16#ff0#;
    ramws        : integer := 0;
    romws        : integer := 2;
    iows         : integer := 2;
    rmw          : integer := 0;
    srbanks      : integer range 1 to 8  := 1;
    banksz       : integer range 0 to 15 := 15;
    rombanks     : integer range 1 to 8  := 1;
    rombanksz    : integer range 0 to 15 := 15;
    rombankszdef : integer range 0 to 15 := 15;
    pindex       : integer := 0;
    paddr        : integer := 0;
    pmask        : integer := 16#fff#;
    edacen       : integer range 0 to 1 := 1;
    errcnt       : integer range 0 to 1 := 0;
    cntbits      : integer range 1 to 8 := 1;
    wsreg        : integer := 0;
    oepol        : integer := 0;
    prom8en      : integer := 0
  );
  port (
    rst          : in  std_ulogic;
    clk          : in  std_ulogic;
    ahbsi        : in  ahb_slv_in_type;
    ahbso        : out ahb_slv_out_type;
    apbi         : in  apb_slv_in_type;
    apbo         : out apb_slv_out_type;
    sri          : in  memory_in_type;
    sro          : out memory_out_type;
    sdo          : out sdctrl_out_type
  );
end component;
```

29.14 Instantiation

This example shows how the core can be instantiated.

The example design contains an AMBA bus with a number of AHB components connected to it including the memory controller. The external memory bus is defined in the example design's port map and connected to the memory controller. System clock and reset are generated by GR Clock Generator and Reset Generator. The CE signal of the memory controller is also connected to the AHB status register.

Memory controller decodes default memory areas: PROM area is 0x0 - 0xFFFFFF and RAM area is 0x40000000 - 0x40FFFFF.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.memctrl.all;
use gaisler.pads.all;   -- used for I/O pads
use gaisler.misc.all;

entity mctrl_ex is
  port (
    clk : in std_ulogic;
    resetn : in std_ulogic;
    pllref : in  std_ulogic;

    -- memory bus
    address  : out   std_logic_vector(27 downto 0); -- memory bus
    data     : inout std_logic_vector(31 downto 0);
    ramsn    : out   std_logic_vector(4 downto 0);
    ramoen   : out   std_logic_vector(4 downto 0);
    rwen     : inout std_logic_vector(3 downto 0);
    romsn    : out   std_logic_vector(1 downto 0);
    iosn     : out   std_logic;
    oen      : out   std_logic;
    read     : out   std_logic;
    writen   : inout std_logic;
    brdyn    : in    std_logic;
    bexcn    : in    std_logic;
-- sdram i/f
    sdcke    : out std_logic_vector ( 1 downto 0);  -- clk en
    sdcsn    : out std_logic_vector ( 1 downto 0);  -- chip sel
    sdwen    : out std_logic;                       -- write en
    sdrasn   : out std_logic;                       -- row addr stb
    sdcasn   : out std_logic;                       -- col addr stb
    sddqm    : out std_logic_vector (7 downto 0);  -- data i/o mask
    sdclk    : out std_logic;                       -- sdram clk output
    sa       : out std_logic_vector(14 downto 0); -- optional sdram address
    sd       : inout std_logic_vector(63 downto 0); -- optional sdram data
    cb       : inout std_logic_vector(7 downto 0); --checkbits
    );
end;

architecture rtl of mctrl_ex is

  -- AMBA bus (AHB and APB)
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbsi : ahb_slv_in_type;
  signal ahbso : ahb_slv_out_vector := (others => ahbs_none);
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);

  -- signals used to connect memory controller and memory bus
  signal memi : memory_in_type;
  signal memo : memory_out_type;

  signal sdo : sdctrl_out_type;

  signal wprot : wprot_out_type;  -- dummy signal, not used
  signal clkm, rstn : std_ulogic; -- system clock and reset

-- signals used by clock and reset generators
  signal cgi : clkgen_in_type;
  signal cgo : clkgen_out_type;
```

```
  signal gnd : std_ulogic;

  signal stati : ahbstat_in_type; --correctable error vector

begin

  -- AMBA Components are defined here ...


  -- Clock and reset generators
  clkgen0 : clkgen generic map (clk_mul => 2, clk_div => 2, sdramen => 1,
                                tech => virtex2, sdinvclk => 0)
  port map (clk, gnd, clkm, open, open, sdclk, open, cgi, cgo);

  cgi.pllctrl <= "00"; cgi.pllrst <= resetn; cgi.pllref <= pllref;

  rst0 : rstgen
  port map (resetn, clkm, cgo.clklock, rstn);

  -- AHB Status Register
  astat0 : ahbstat generic map(pindex => 13, paddr => 13, pirq => 11,
    nftslv => 1)
    port map(rstn, clkm, ahbmi, ahbsi, stati, apbi, apbo(13));

  stati.cerror(0) <= memo.ce;

  -- Memory controller
  mctrl0 : ftsrctrl generic map (rmw => 1, pindex => 10, paddr => 10,
    edacen => 1, errcnt => 1, cntbits => 4)
    port map (rstn, clkm, ahbsi, ahbso(0), apbi, apbo(10), memi, memo,
  sdo);


  -- I/O pads driving data memory bus data signals
  datapads : for i in 0 to 3 generate
      data_pad : iopadv generic map (width => 8)
      port map (pad => data(31-i*8 downto 24-i*8),
                o => memi.data(31-i*8 downto 24-i*8),
                en => memo.bdrive(i),
                i => memo.data(31-i*8 downto 24-i*8));
  end generate;

  --I/O pads driving checkbit signals
  cb_pad : iopadv generic map (width => 8)
      port map (pad => cb,
                o => memi.cb,
                en => memo.bdrive(0),
                i => memo.cb;

  -- connect memory controller outputs to entity output signals
  address <= memo.address; ramsn <= memo.ramsn; romsn <= memo.romsn;
  oen <= memo.oen; rwen <= memo.wrn; ramoen <= memo.ramoen;
  writen <= memo.writen; read <= memo.read; iosn <= memo.iosn;
  sdcke <= sdo.sdcke; sdwen <= sdo.sdwen; sdcsn <= sdo.sdcsn;
  sdrasn <= sdo.rasn; sdcasn <= sdo.casn; sddqm <= sdo.dqm;

end;
```

30 FTSRCTRL8 - 8-bit SRAM/16-bit IO Memory Controller with EDAC

30.1 Overview

The fault tolerant 8-bit SRAM/16-bit I/O memory interface uses a common 16-bit data bus to interface 8-bit SRAM and 16-bit I/O devices. It provides an Error Detection And Correction unit (EDAC), correcting up to two errors and detecting up to four errors in a data byte. The EDAC eight checkbits are stored in parallel with the 8-bit data in SRAM memory. Configuration of the memory controller functions is performed through the APB bus interface.

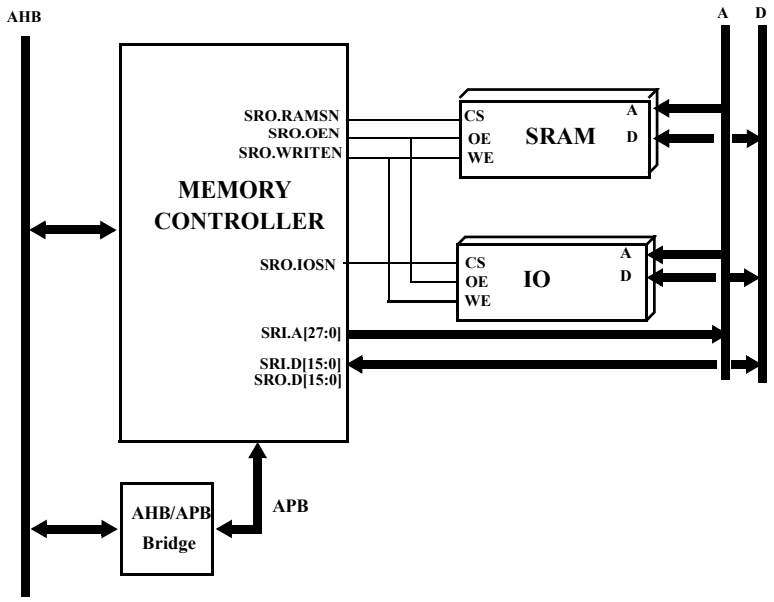


Figure 101. Block diagram

30.2 Operation

The controller is configured through VHDL generics to decode two address ranges: SRAM and I/O area. By default the SRAM area is mapped into address range 0x40000000 - 0x40FFFFFF, and the I/O area is mapped to 0x20000000 - 0x20FFFFFF.

One chip select is decoded for the I/O area, while SRAM can have up to 8 chip select signals. The controller generates a common write-enable signal (WRITEN) for both SRAM and I/O. The number of waitstates may be separately configured for the two address ranges.

The EDAC function is optional, and can be enabled with the edacen VHDL generic. The configuration of the EDAC is done through a configuration register accessed from the APB bus. During nominal operation, the EDAC checksum is generated and checked automatically. The 8-bit input to the EDAC function is split into two 4-bit nibbles. A modified hamming(8,4,4) coding featuring a single error correction and double error detection is applied to each 4-bit nibble. This makes the EDAC capable of correcting up to two errors and detecting up to four errors per 8-bit data. Single errors (correctable errors) are corrected without generating any indication of this condition in the bus response. If a multiple error (uncorrectable errors) is detected, a two cycle error response is given on the AHB bus.

Single errors may be monitored in two ways:

- by monitoring the CE signal which is asserted for one cycle each time a correctable error is detected.
- by checking the single error counter which is accessed from the MCFG3 configuration register.

The CE signal can be connected to the AHB status register which stores information of the AHB instruction causing the error and also generates interrupts. See the AHB status register documentation for more information.

The EDAC function can only be enabled for SRAM area accesses. If a 16-bit or 32-bit bus access is performed, the memory controller calculates the EDAC checksum for each byte read from the memory but the indication of single error is only signaled when the access is done. (I.e. if more than one byte in a 32-bit access has a single error, only one error is indicated for the hole 32-bit access.)

The equations below show how the EDAC checkbits are generated:

```
CB7 = Data[15] ^ Data[14] ^ Data[13]     // i.e. Data[7]
CB6 = Data[15] ^ Data[14] ^ Data[12]     // i.e. Data[6]
CB5 = Data[15] ^ Data[13] ^ Data[12]     // i.e. Data[5]
CB4 = Data[14] ^ Data[13] ^ Data[12]     // i.e. Data[4]
CB3 = Data[11] ^ Data[10] ^ Data[ 9]     // i.e. Data[3]
CB2 = Data[11] ^ Data[10] ^ Data[ 8]     // i.e. Data[2]
CB1 = Data[11] ^ Data[ 9] ^ Data[ 8]     // i.e. Data[1]
CB0 = Data[10] ^ Data[ 9] ^ Data[ 8]     // i.e. Data[0]
```

30.2.1 Memory access

The memory controller supports 32/16/8-bit single accesses and 32-bit burst accesses to the SRAM. A 32-bit or a 16-bit access is performed as multiple 8-bit accesses on the 16-bit memory bus, where data is transferred on data lines 8 to 15 (Data[15:8]). The eight checkbits generated/used by the EDAC are transferred on the eight first data lines (Data[7:0]). For 32-bit and 16-bit accesses, the bytes read from the memory are arranged according to the big-endian order (i.e. for a 32-bit read access, the bytes read from memory address A, A+1, A+2, and A+3 correspond to the bit[31:24], bit[23:16], bit[15:8], and bit[7:0] in the 32-bit word transferred to the AMBA bus. The table 338 shows the expected latency from the memory controller.

*Table 329.*FTSCTRL8 access latency

Accesses	Single data	First data (burst)	Middle data (burst)	Last data (burst)
32-bit write	10	8	8	10
32-bit read	6	6	4	4
16-bit write	4 (+1)	-	-	-
16-bit read	4	-	-	-
8-bit write	4	-	-	-
8-bit read	3	-	-	-

One extra cycle is added for 16-bit burst accesses when Bus Exception is enabled.

30.2.2 I/O access

The memory controller accepts 32/16/8-bit single accesses to the I/O area, but the access generated towards the I/O device is always 16-bit. The two least significant bits of the AMBA address (byte address) determine which half word that should be transferred to the I/O device. (i.e. If the byte address is 0 and it is a 32-bit access, bits 16 to 31 on the AHB bus is transferred on the 16-bit memory bus. If the byte address is 2 and it is a 16-bit access, bit 0 to 15 on the AHB bus is transferred on the 16-bit memory bus.) If the access is an 8-bit access, the data is transferred on data lines 8 to 15 (Data[15:8]) on the memory bus. In case of a write, data lines 0 to 7 is also written to the I/O device but these data lines do not transfer any valid data.

30.2.3 Using Bus Exception

The active low Bus Exception signal (BEXCN) can be used to signal access errors. It is enabled by setting the BEXCEN bit in MCFG1 and is only active for the I/O area. The BEXCN signal is sampled on the same cycle as data is written to memory or read data is sampled. When a bus exception is detected an error response will be generated for the access. One additional latency cycle is added to the AMBA access when the Bus Exception is enable.

30.2.4 Using Bus Ready

The Bus Ready (BRDYN) signal can be used to add waitstates to I/O-area accesses. It is enabled by setting the Bus Ready Enable (BRDYEN) bit in the MCFG1 register. An access will have at least the amount of waitstates set with the VHDL generic or through the register, but will be further stretched until BRDYN is asserted. Additional waitstates can thus be inserted after the pre-set number of wait-states by deasserting the BRDYN signal. BRDYN should be asserted in the cycle preceding the last one. It is recommended that BRDY remains asserted until the IOSN signal is de-asserted, to ensure that the access has been properly completed and avoiding the system to stall.

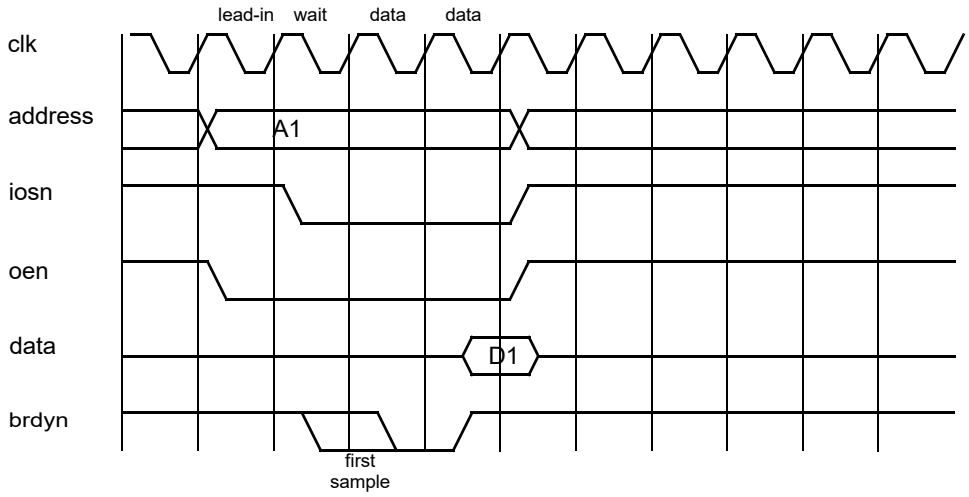


Figure 102. I/O READ cycle, programmed with 1 wait state, and with an extra data cycle added with BRDYN.

30.3 SRAM/IO waveforms

The internal and external waveforms of the interface are presented in the figures below.

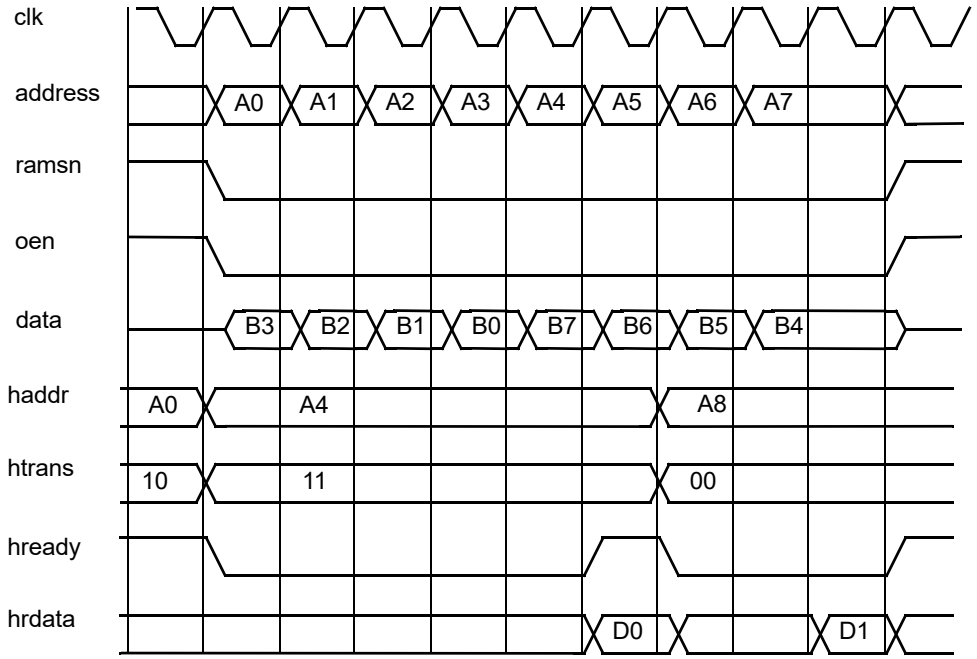


Figure 103. 32-bit SRAM sequential read accesses with 0 wait-states and EDAC enabled.

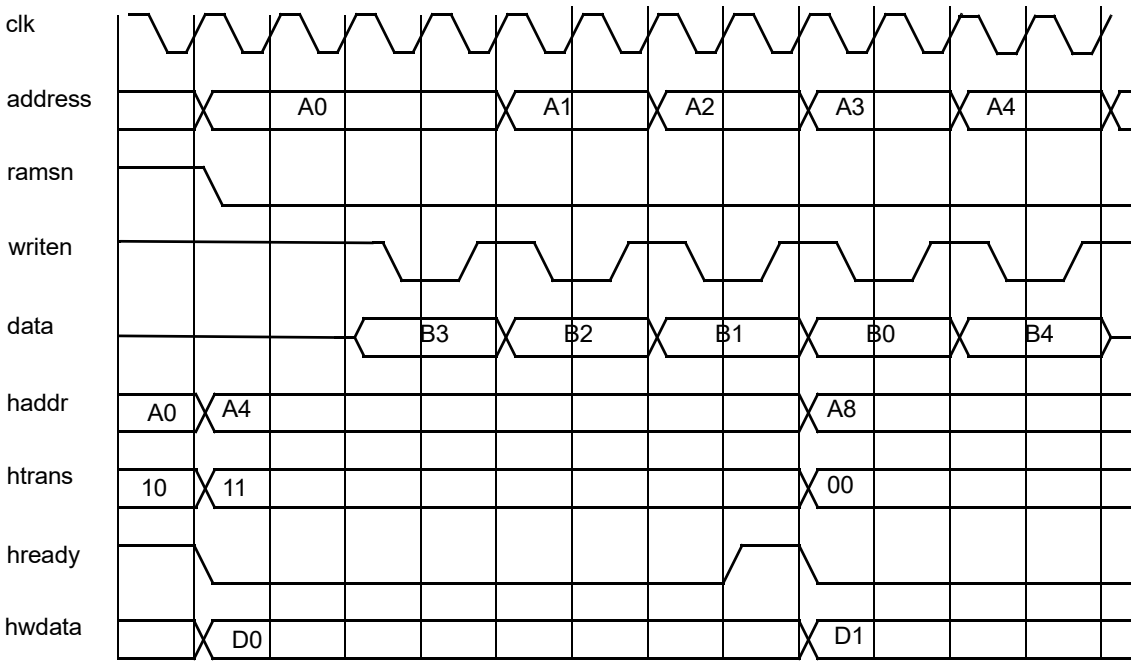


Figure 104. 32-bit SRAM sequential writeaccess with 0 wait-states and EDAC enabled.

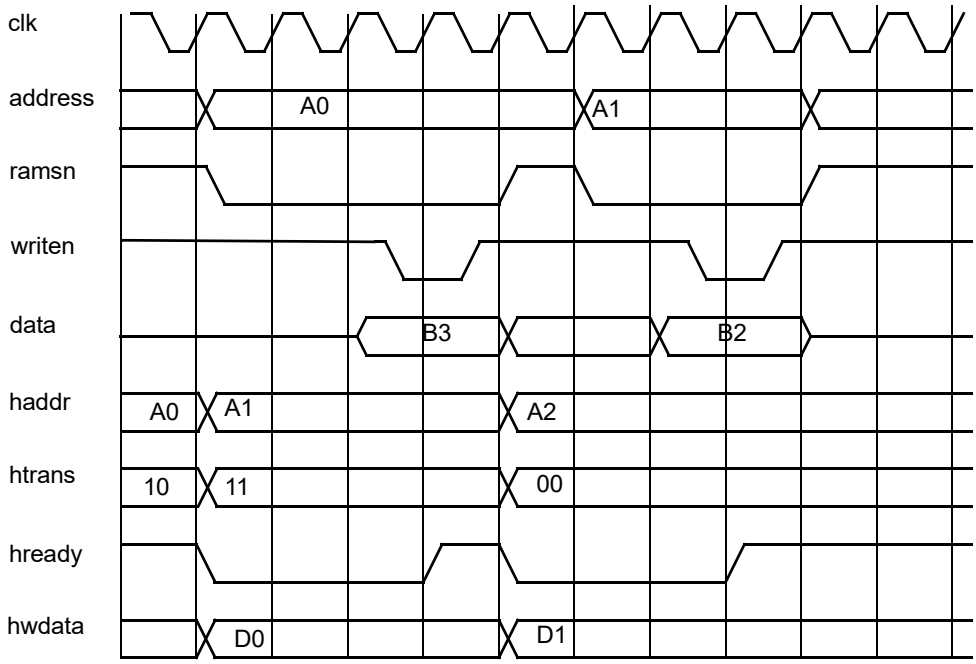


Figure 105. 8-bit SRAM non-sequential write access with 0 wait-states and EDAC enabled.

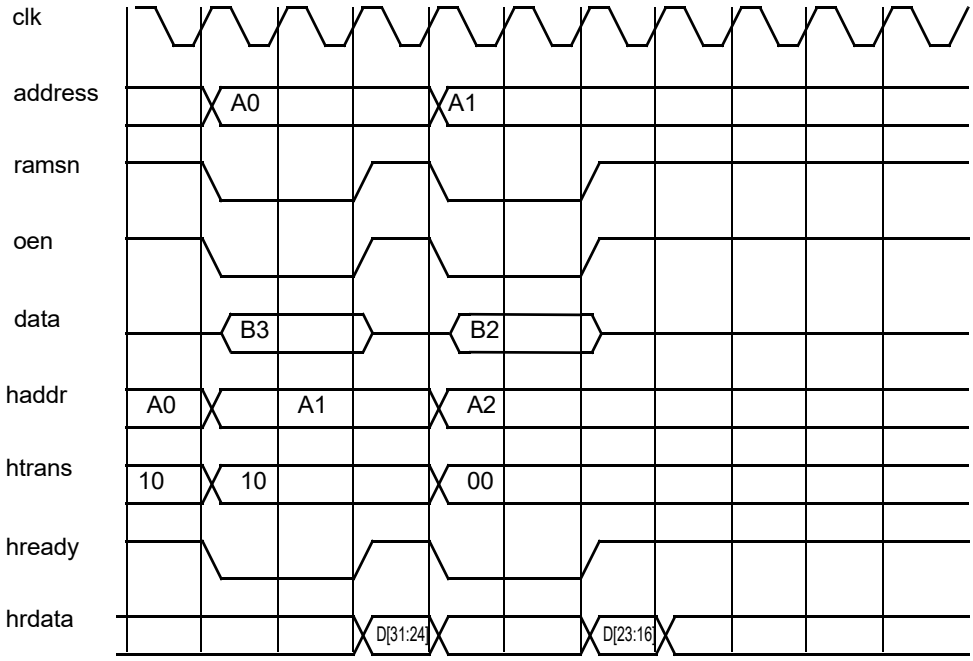


Figure 106. 8-bit SRAM non-sequential read access with 0 wait-states and EDAC enabled.

On a read access, data is sampled one clock cycle before HREADY is asserted.

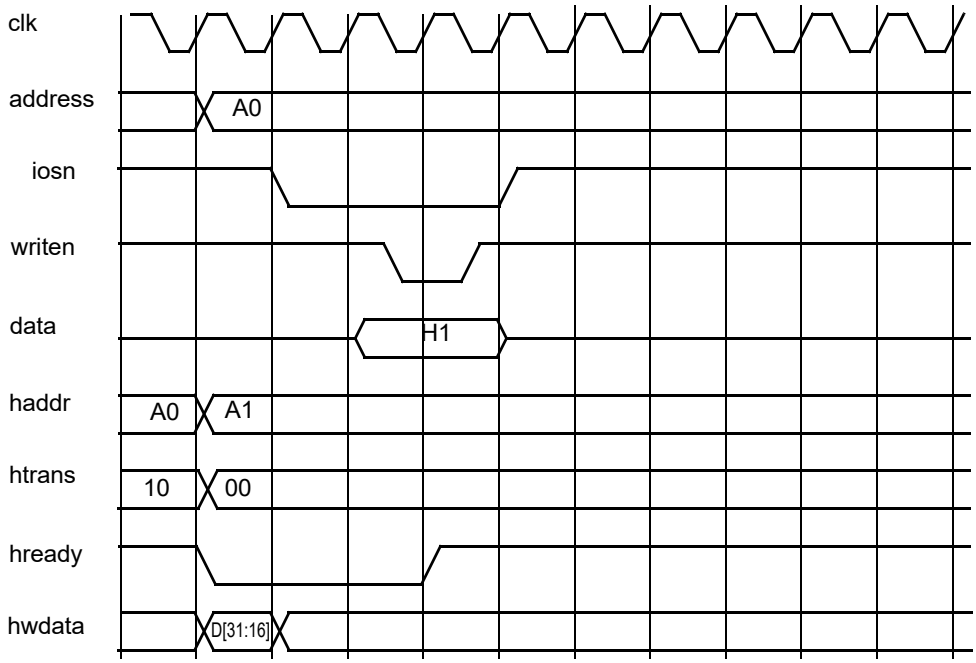


Figure 107. 16-bit I/O non-sequential write access with 0 wait-states.

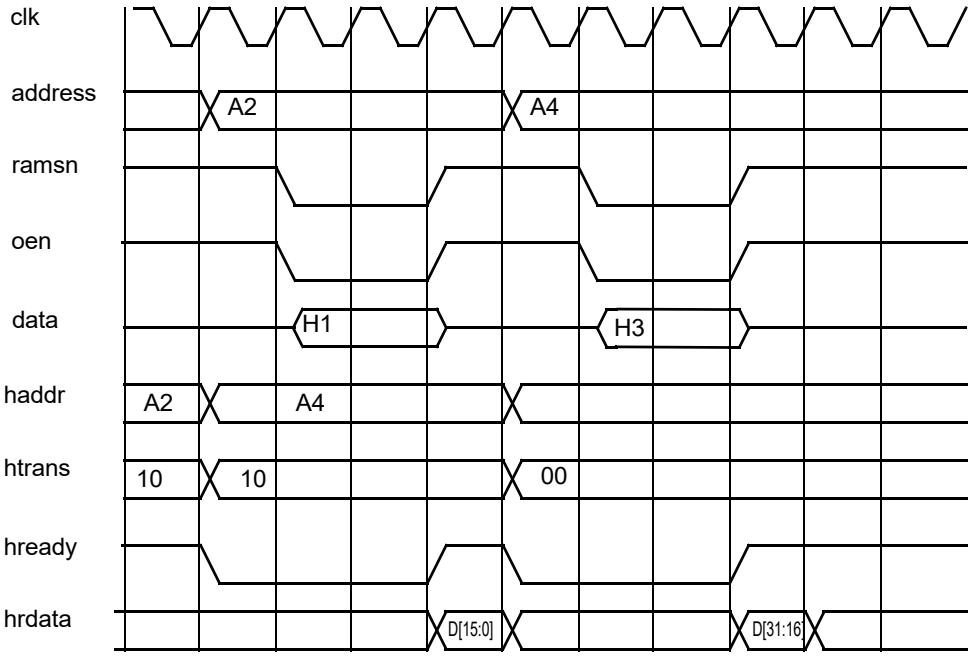


Figure 108. 16-bit I/O non-sequential read access with 0 wait-states.

I/O write accesses are extended with one extra latency cycle if the bus exception is enabled.

If waitstates are configured through the VHDL generics or registers, one extra data cycle will be inserted for each waitstate in both read and write cycles.

30.4 Endianness

The core is designed for big-endian systems.

30.5 Registers

The core is programmed through registers mapped into APB address space.

*Table 330.*FT SRAM/IO controller registers

APB Address offset	Register
0x00	Memory configuration register 1
0x04	Memory configuration register 2
0x08	Memory configuration register 3

30.5.1 Memory Configuration Register 1

*Table 331.*0x00 - MCFG1 - Memory configuration register 1

31 27	26	25	24	23 20	19 0
RESERVED	BRDY	BEXC	R	IOWS	RESERVED
0	0	0	0	0xF	0
r	rw	rw	r	rw	r

31 : 27 RESERVED

26 BRDYEN: Enables the BRDYN signal.

25 BEXCEN: Enables the BEXCN signal.

24 RESERVED

23 : 20 IOWS: Sets the number of waitstates for accesses to the IO area. Only available if the wsreg VHDL generic is set to one.

19 : 0 RESERVED

30.5.2 Memory Configuration Register 2

*Table 332.*0x04 - MCFG2 - Memory configuration register 2

31 13	12 9	8 2	1 0
RESERVED	RAMBSZ	RESERVED	RAMWS
0	*	0	*
r	rw*	r	rw*

31 : 12 RESERVED

12 : 9 RAMBSZ: Sets the SRAM bank size. Only available if the banksz VHDL generic is set to zero. Otherwise the banksz VHDL generic sets the bank size. 0 = 8 kB, 15 = 256 MB.

8 : 2 RESERVED

1 : 0 RAMWS: Sets the number of waitstates for accesses to the RAM area. Only available if the wsreg VHDL generic is set to one.

30.5.3 Memory Configuration 3

*Table 333.*0x08 - MCFG2 - Memory configuration register 3

31 cnt + 13	cnt + 12 12	11	10	9	8	7 0
RESERVED	SEC	WB	RB	SEN		TCB
0	0	0	0	0	0	NR
r	wc	rw	rw	rw	r	rw

31 : cnt+13 RESERVED

cnt+12 : 12 SEC. Single error counter. This field increments each time a single error is detected. It saturates at the maximum value that can be stored in this field. Each bit can be reset by writing a one to it. cnt = the number of counter bits.

11 WB: Write bypass. If set, the TCB field will be used as checkbits in all write operations.

10 RB: Read bypass. If set, checkbits read from memory in all read operations will be stored in the TCB field.

9 SEN: SRAM EDAC enable. If set, EDAC will be active for the SRAM area.

8 RESERVED

7 : 0 TCB: Used as checkbits in write operations when WB is one and checkbits from read operations are stored here when RB is one.

All the fields in the MCFG3 register are available if the edacen VHDL generic is set to one except for the SEC field which also requires that the errcnt VHDL generic is set to one.

30.6 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x056. For description of vendor and device identifiers see the GRLIB IP Library User's Manual.

30.7 Implementation

30.7.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers. The registers driving external chip select, output enable and output enables for the data bus have asynchronous reset.

30.8 Configuration options

Table 330 shows the configuration options of the core (VHDL generics).

Table 334. Controller configuration options

Generic	Function	Allowed range	Default
hindex	AHB slave index.	1 - NAHBSLV-1	0
ramaddr	ADDR field of the AHB BAR1 defining RAM address space. Default RAM area is 0x40000000-0x40FFFFFF.	0 - 16#FFF#	16#400#
rammask	MASK field of the AHB BAR1 defining RAM address space.	0 -16#FFF#	16#FF0#
ioaddr	ADDR field of the AHB BAR2 defining IO address space. Default RAM area is 0x20000000-0x20FFFFFF.	0 - 16#FFF#	16#200#
iomask	MASK field of the AHB BAR2 defining IO address space.	0 - 16#FFF#	16#FF0#
ramws	Number of waitstates during access to SRAM area.	0 - 15	0
iows	Number of waitstates during access to IO area.	0 - 15	2
srbanks	Set the number of RAM banks.	1 - 8	1
banksz	Set the size of bank 1 - 4. 1 = 16 kB, ... , 15 = 256 MB. If set to zero, the bank size is set with the rambsz field in the MCFG2 register.	0 - 15	15
pindex	APB slave index.	1 - NAPBSLV-1	0
paddr	APB address.	1 - 16#FFF#	0
pmask	APB address mask.	1 - 16#FFF#	16#FFF#
edacen	EDAC enable. If set to one, EDAC logic is synthesized.	0 - 1	0
errcnt	If one, a single error counter is added.	0 - 1	0
cntbits	Number of bits in the single error counter.	1 - 8	1
wsreg	Enable programmable waitstate generation.	0 - 1	0

30.9 Signal descriptions

Table 335 shows the interface signals of the core (VHDL ports).

*Table 335.*Signal descriptions

Signal name	Field	Type	Function	Active
CLK	N/A	Input	Clock	-
RST	N/A	Input	Reset	Low

*Table 335.*Signal descriptions

Signal name	Field	Type	Function	Active
SRI	DATA[31:0]	Input	Memory data: [15:0] used for IO accesses [7:0] used for checkbits for SRAM accesses [15:8] use for data for SRAM accesses	High
	BRDYN	Input	Bus ready strobe	Low
	BEXCN	Input	Bus exception	Low
	WRN[3:0]	Input	Not used	-
	BWIDTH[1:0]	Input	Not used	-
	SD[31:0]	Input	Not used	-
	CB[7:0]	Input	Not used	-
	PROMDATA[31:0]	Input	Not used	-
	EDAC	Input	Not used	-
SRO	ADDRESS[31:0]	Output	Memory address	High
	DATA[31:0]	Output	Memory data: [15:0] used for IO accesses [7:0] used for checkbits for SRAM accesses [15:8] use for data for SRAM accesses	High
	RAMSN[7:0]	Output	SRAM chip-select	Low
	RAMOEN[7:0]	Output	SRAM output enable	Low
	IOSN	Output	IO area chip select	Low
	ROMSN[7:0]	Output	Not used	Low
	OEN	Output	Output enable	Low
	WRITEN	Output	Write strobe	Low
	WRN[3:0]	Output	SRAM write enable: WRN[0] corresponds to DATA[15:8], WRN[1] corresponds to DATA[7:0], WRN[3:2] Not used	Low
	BDRIVE[3:0]	Output	Drive byte lanes on external memory bus. Controls I/O-pads connected to external memory bus: BDRIVE[0] corresponds to DATA[15:8], BDRIVE[1] corresponds to DATA[7:0], BDRIVE[3:2] Not used	Low
	VBDRIVE[31:0]	Output	Vectored I/O-pad drive signal.	Low
	READ	Output	Read strobe	High
	RAMN	Output	Common SRAM Chip Select. Always asserted when one of the 8 RAMSN signals is asserted.	Low
	ROMN	Output	Not used	-
	SA[14:0]	Output	Not used	-
	CB[7:0]	Output	Not used	-
	PSEL	Output	Not used	-
	CE	Output	Single error detected.	High
AHBSI	*	Input	AHB slave input signals	-
AHBSO	*	Output	AHB slave output signals	-

* see GRLIB IP Library User's Manual

30.10 Signal definitions and reset values

The signals and their reset values are described in table 336.

*Table 336.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
address[25:0]	Output	Memory address	High	Undefined
data[31:0]	Input/Output	Memory data	High	Tri-state
cb[7:0]	Input/Output	Check bits	High	Tri-state
ramsn[3:0]	Output	SRAM chip select	Low	Logical 1
ramoen[3:0]	Output	SRAM output enable	Low	Logical 1
rwen[3:0]	Output,	SRAM write enable: rwen[0] corresponds to data[15:8], rwen[1] corresponds to data[7:0], rwen[3:2] Not used	Low	Logical 1
ramben[3:0]	Output	SRAM bank enable: ramben[0] corresponds to data[15:8], ramben[1] corresponds to data[7:8], ramben[3:2] Not used	Low	Logical 1
oen	Output	Output enable	Low	Logical 1
writen	Output	Write strobe	Low	Logical 1
read	Output	Read strobe	High	Logical 1
iosn	Output	IO area chip select	Low	Logical 1
brdyn	Input	Bus ready. Extends accesses to the IO area.	Low	-
bexcn	Input	Bus exception.	Low	-

30.11 Timing

The timing waveforms and timing parameters are shown in figure 109 and are defined in table 337.

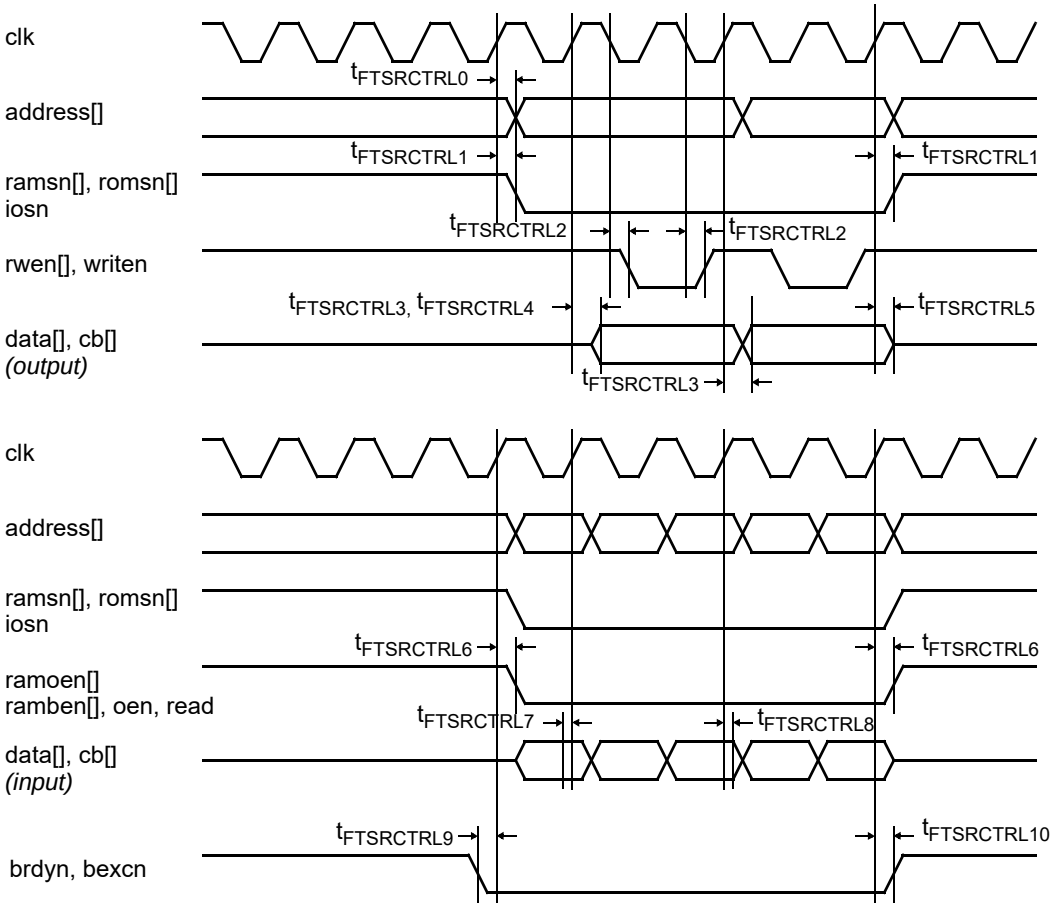


Figure 109. Timing waveforms

*Table 337.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{FTSRCTRL0}$	address clock to output delay	rising clk edge	TBD	TBD	ns
$t_{FTSRCTRL1}$	clock to output delay	rising clk edge	TBD	TBD	ns
$t_{FTSRCTRL2}$	clock to output delay	rising clk edge	TBD	TBD	ns
$t_{FTSRCTRL3}$	clock to data output delay	falling clk edge	TBD	TBD	ns
$t_{FTSRCTRL4}$	clock to data non-tri-state delay	rising clk edge	TBD	TBD	ns
$t_{FTSRCTRL5}$	clock to data tri-state delay	rising clk edge	TBD	TBD	ns
$t_{FTSRCTRL6}$	clock to output delay	rising clk edge	TBD	TBD	ns
$t_{FTSRCTRL7}$	data input to clock setup	rising clk edge	TBD	-	ns
$t_{FTSRCTRL8}$	data input from clock hold	rising clk edge	TBD	-	ns
$t_{FTSRCTRL9}$	input to clock setup	rising clk edge	TBD	-	ns
$t_{FTSRCTRL10}$	input from clock hold	rising clk edge	TBD	-	ns

30.12 Library dependencies

Table 338 shows libraries used when instantiating the core (VHDL libraries).

*Table 338.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AHB signal definitions
GAISLER	MEMCTRL	Signals, component	Memory bus signals definitions, component declaration

30.13 Component declaration

The core has the following component declaration.

```
component ftsrctrl8 is
  generic (
    hindex       : integer := 0;
    ramaddr      : integer := 16#400#;
    rammask      : integer := 16#ff0#;
    ioaddr       : integer := 16#200#;
    iomask       : integer := 16#ff0#;
    ramws        : integer := 0;
    iows         : integer := 2;
    srbanks      : integer range 1 to 8  := 1;
    banksz       : integer range 0 to 15 := 15;
    pindex       : integer := 0;
    paddr        : integer := 0;
    pmask        : integer := 16#fff#;
    edacen       : integer range 0 to 1 := 1;
    errcnt       : integer range 0 to 1 := 0;
    cntbits      : integer range 1 to 8 := 1;
    wsreg        : integer := 0;
    oepol        : integer := 0
  );
  port (
    rst          : in  std_ulogic;
    clk          : in  std_ulogic;
    ahbsi        : in  ahb_slv_in_type;
    ahbso        : out ahb_slv_out_type;
    apbi         : in  apb_slv_in_type;
    apbo         : out apb_slv_out_type;
    sri          : in  memory_in_type;
    sro          : out memory_out_type
  );
end component;
```

30.14 Instantiation

This example shows how the core can be instantiated.

The example design contains an AMBA bus with a number of AHB components connected to it including the memory controller. The external memory bus is defined in the example design's port map and connected to the memory controller. The system clock and reset are generated by GR Clock Generator and Reset Generator. The CE signal of the memory controller is also connected to the AHB status register.

The memory controller decodes default memory areas: I/O area is 0x20000000 - 0x20FFFFFF and RAM area is 0x40000000 - 0x40FFFFF.

```
library ieee;
use ieee.std_logic_1164.all;
library grlib;
use grlib.amba.all;
library techmap;
use techmap.gencomp.all;
library gaisler;
```

```
use gaisler.memctrl.all;
use gaisler.misc.all;

entity ftsrctrl8_ex is
  port (
    resetn     : in  std_ulogic;
    clk        : in  std_ulogic;

    address    : out std_logic_vector(27 downto 0);
    data       : inout std_logic_vector(31 downto 0);
    ramsn      : out std_logic_vector (3 downto 0);
    ramoen     : out std_logic_vector (3 downto 0);
    rwen       : out std_logic_vector (3 downto 0);
    oen        : out std_ulogic;
    writen     : out std_ulogic;
    read       : out std_ulogic;
    iosn       : out std_ulogic;
    brdyn      : in  std_ulogic; -- Bus ready
    bexcn      : in  std_ulogic  -- Bus exception
   );
end;

architecture rtl of ftsrctrl8_ex is
signal memi  : memory_in_type;
signal memo  : memory_out_type;

signal apbi  : apb_slv_in_type;
signal apbo  : apb_slv_out_vector := (others => apb_none);
signal ahbsi : ahb_slv_in_type;
signal ahbso : ahb_slv_out_vector := (others => ahbs_none);
signal ahbmi : ahb_mst_in_type;
signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);

signal clkm, rstn, rstraw : std_ulogic;
signal cgi   : clkgen_in_type;
signal cgo   : clkgen_out_type;

signal stati : ahbstat_in_type;

begin

  -- clock and reset
  cgi.pllctrl <= "00"; cgi.pllrst <= rstraw; cgi.pllref  <= '0';
  clk_pad : clkpad port map (clk, clkm);
  rst0 : rstgen               -- reset generator
  port map (resetn, clkm, '1', rstn, rstraw);

  -- AHB controller
  ahb0 : ahbctrl              -- AHB arbiter/multiplexer
  generic map (rrobin => 1, ioaddr => 16#fff#, devid => 16#201#)
  port map (rstn, clkm, ahbmi, ahbmo, ahbsi, ahbso);

  -- Memory controller
  sr0 : ftsrctrl8 generic map (hindex => 0, pindex => 0, edacen => 1)
    port map (rstn, clkm, ahbsi, ahbso(0), apbi, apbo(0), memi, memo);

  brdyn_pad : inpad port map (brdyn, memi.brdyn);
  bexcn_pad : inpad port map (bexcn, memi.bexcn);

  addr_pad : outpadv generic map (width => 28 )
    port map (address, memo.address(27 downto 0));
  rams_pad : outpadv generic map (width => 4)
    port map (ramsn, memo.ramsn(3 downto 0));
  oen_pad  : outpad
    port map (oen, memo.oen);
  rwen_pad : outpadv generic map (width => 4)
    port map (rwen, memo.wrn);
  roen_pad : outpadv generic map (width => 4)
    port map (ramoen, memo.ramoen(3 downto 0));
  wri_pad  : outpad
    port map (writen, memo.writen);
```

```
  read_pad : outpad
    port map (read, memo.read);
  iosn_pad : outpad
    port map (iosn, memo.iosn);
  data_pad : iopadvv generic map (width => 8) -- SRAM and I/O Data
    port map (data(15 downto 8), memo.data(15 downto 8),
       memo.vbdrive(15 downto 8), memi.data(15 downto 8));
  cbdata_pad : iopadvv generic map (width => 8) -- SRAM checkbits and I/O Data
    port map (data(7 downto 0), memo.data(7 downto 0),
       memo.vbdrive(7 downto 0), memi.data(7 downto 0));

  -- APB bridge and AHB stat
  apb0 : apbctrl              -- AHB/APB bridge
  generic map (hindex => 1, haddr => 16#800#)
    port map (rstn, clkm, ahbsi, ahbso(1), apbi, apbo );

  stati.cerror(0) <= memo.ce;
  ahbstat0 : ahbstat generic map (pindex => 15, paddr => 15, pirq => 1)
    port map (rstn, clkm, ahbmi, ahbsi, stati, apbi, apbo(15));
end;
```

31 GPTIMER - General Purpose Timer Unit

31.1 Overview

The General Purpose Timer Unit provides a common prescaler and decrementing timer(s). The number of timers is configurable through the *ntimers* VHDL generic in the range 1 to 7. The prescaler width is configured through the *sbits* VHDL generic. Timer width is configured through the *tbits* VHDL generic. The timer unit acts a slave on AMBA APB bus. The unit is capable of asserting interrupts on timer underflow. The interrupt to use is configurable to be common for the whole unit or separate for each timer.

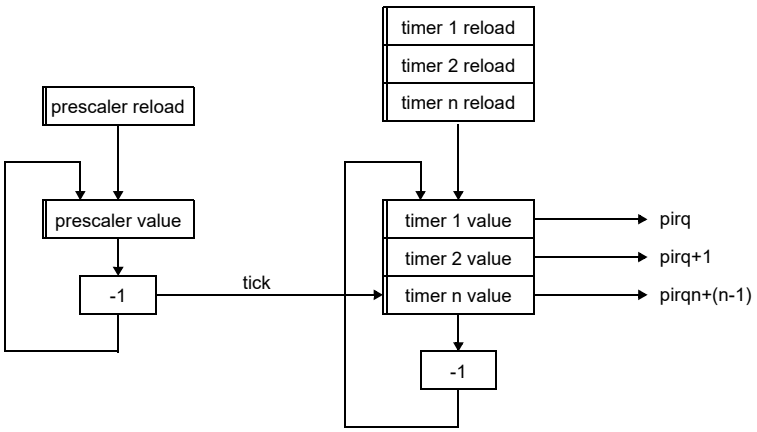


Figure 110. General Purpose Timer Unit block diagram

31.2 Operation

The prescaler is clocked by the system clock and decremented on each clock cycle when at least one timer is enabled. When the prescaler underflows, it is reloaded from the prescaler reload register and a timer tick is generated.

The operation of each timers is controlled through its control register. A timer is enabled by setting the enable bit in the control register. The timer value is then decremented on each prescaler tick. When a timer underflows, it will automatically be reloaded with the value of the corresponding timer reload register if the restart bit in the control register is set, otherwise it will stop at -1 and reset the enable bit.

The timer unit can be configured to generate common interrupt through a VHDL-generic. The shared interrupt will be signaled when any of the timers with interrupt enable bit underflows. The timer unit will signal an interrupt on appropriate line when a timer underflows (if the interrupt enable bit for the current timer is set), when configured to signal interrupt for each timer. The interrupt pending bit in the control register of the underflown timer will be set and remain set until cleared by writing '1'.

To minimize complexity, timers share the same decrementer. This means that the minimum allowed prescaler division factor is *ntimers*+1 (reload register = *ntimers*) where *ntimers* is the number of implemented timers. By setting the chain bit in the control register timer *n* can be chained with preceding timer *n*-1. Timer *n* will be decremented each time when timer *n*-1 underflows.

Each timer can be reloaded with the value in its reload register at any time by writing a 'one' to the load bit in the control register. The last timer acts as a watchdog, driving a watchdog output signal when expired, when the *wdog* VHDL generic is set to a time-out value larger than 0. The watchdog timer also implements a window functionality when the *wdogwin* VHDL generic is set to 1. This enables a decrementing counter which reloads each time the timer is reloaded. If the timer is reloaded and the window counter has not reached zero, this will also assert the watchdog output.

Each timer can be configured to latch its value to a dedicated register when an event is detected on the interrupt (functionality enabled via VHDL generic *glatch*). All timers can be forced to reload when an event is detected on the interrupt bus (functionality enabled via VHDL generic *gset*). A dedicated mask register is provided to filter the interrupts.

At reset, all timers are disabled except the watchdog timer (if enabled by the generics). The prescaler value and reload registers are set to all ones, while the watchdog timer is set to the *wdog* VHDL generic. All other registers are uninitialized except for the WDOGDIS and WDOGNMI fields that are reset to '0'.

31.3 Registers

The core is programmed through registers mapped into APB address space. The number of implemented registers depend on the number of implemented timers.

*Table 339.*General Purpose Timer Unit registers

APB address offset	Register
0x00	Scaler value
0x04	Scaler reload value
0x08	Configuration register
0x0C	Timer latch configuration register
0x10	Timer 1 counter value register
0x14	Timer 1 reload value register
0x18	Timer 1 control register
0x1C	Timer 1 latch register
0x*n*0	Timer *n* counter value register
0x*n*4	Timer *n* reload value register
0x*n*8	Timer *n* control register
0x*n*C	Timer *n* latch register

31.3.1 Scaler Value Register

*Table 340.*0x00 - SCALER - Scaler value register

31 16	16-1 0
RESERVED	SCALER
0	all 1
r	rw

16-1: 0 Scaler value. This value will also be set by writes to the Scaler reload value register.
Any unused most significant bits are reserved. Always reads as '000...0'.

31.3.2 Scaler Reload Value Register

*Table 341.*0x04 - SRELOAD - Scaler reload value register

31 16	16-1 0
RESERVED	SCALER RELOAD VALUE
0	all 1
r	rw

16-1: 0 Scaler reload value. Writes to this register also set the scaler value.
Any unused most significant bits are reserved. Always read as '000...0'.

31.3.3 Configuration Register

*Table 342.*0x08 - CONFIG - Configuration register

31 23	22 16	15 14	13	12	11	10	9	8	7 3	2 0
"000..0"	TIMEREN	00	EV	ES	EL	EE	DF	SI	IRQ	TIMERS
0	0	0	0	0	0	0	0	*	*	*
r	rw	r	rw	rw	rw	rw	rw	r	r	r

31: 23 Reserved. Always reads as '000...0'.

22: 16 Enable bits for each timer. Writing '1' to one of this bits sets the enable bit in the corresponding timers control register. Writing '0' has no effect to the timers. bit[16] corresponds to timer0, bit[17] to timer 1,...

15: 14 Reserved

13 External Events (EV). If set then the latch events are taken from the secondary input. If this field is zero then the source of the latch events is the interrupt bus.

12 Enable set (ES). If set, on the next matching interrupt, the timers will be loaded with the corresponding timer reload values. The bit is then automatically cleared, not to reload the timer values until set again.

11 Enable latching (EL). If set, on the next matching interrupt, the latches will be loaded with the corresponding timer values. The bit is then automatically cleared, not to load a timer value until set again.

10 Enable external clock source (EE). If set the prescaler is clocked from the external clock source.

9 Disable timer freeze (DF). If set the timer unit can not be freezed, otherwise signal GPTI.DHALT freezes the timer unit.

8 Separate interrupts (SI). Reads '1' if the timer unit generates separate interrupts for each timer, otherwise '0'. Read-only.

7: 3 APB Interrupt: If configured to use common interrupt all timers will drive APB interrupt nr. IRQ, otherwise timer *n* will drive APB Interrupt IRQ+*n* (has to be less the MAXIRQ). Read-only.

2: 0 Number of implemented timers. Read-only.

31.3.4 Timer Latch Configuration Register

*Table 343.*0x0C - CATCHCFG - Timer latch configuration register

31 0
LATCHSEL
0
rw

31: 0 Specifies what bits of the interrupt bus, or external latch vector, bus that shall cause the Timer Latch Registers to latch the timer values. If the configuration register EV field is zero then latching is done based on events on the interrupt bus. If the EV field is '1' then the external latch vecor is used.

31.3.5 Timer N Counter Value Register

*Table 344.*0xn0, when n selects the times - TCNTVALn - Timer n counter value register

32-1 0
TCVAL
0
rw

32-1: 0 Timer Counter value. Decremented by 1 for each prescaler tick.

Any unused most significant bits are reserved. Always reads as '000...0'.

31.3.6 Timer N Reload Value Register

*Table 345.*0xn4, when n selects the times - TRLDVALn - Timer n reload value register

32-1	0
TRCDUAL	
*	
rw	

32-1: 0 Timer Reload value. This value is loaded into the timer counter value register when '1' is written to load bit in the timers control register or when the RS bit is set in the control register and the timer underflows.

Any unused most significant bits are reserved. Always reads as '000...0'.

31.3.7 Timer N Control Register

*Table 346.*0xn8, when n selects the times - TCTRLn - Timer n control register

31	16	15	9	8	7	6	5	4	3	2	1	0
WDOGWINC		RESERVED		WS	WN	DH	CH	IP	IE	LD	RS	EN
0		0		0	0	0	0	0	*	0	*	*
rw		r		rw	rw	r	rw	wc	rw	rw	rw	rw

31: 16 Reload value for the watchdog window counter. The window counter is reloaded with this value each time the watchdog counter is reloaded. This functionality is only available when the core has been implemented with VHDL generic wdog /= 0, wdogwin /= 0 and only for the last timer

15: 9 Reserved. Always reads as '000...0'.

8 Disable Watchdog Output (WS/WDOGDIS): If this field is set to '1' then the GPTO.WDOG and GPTO.WDOGN outputs are disabled (fixed to '0' and '1' respectively). This functionality is only available when the core has been implemented with VHDL generic wdog /= 0 and only for the last timer. If wdog = 0 then this register is read-only and always '0'.

7 Enable Watchdog NMI (WN/WDOGNMI): If this field is set to '1' then the watchdog timer will also generate a non-maskable interrupt (interrupt 15) when an interrupt is signalled. This functionality is only available when the core has been implemented with VHDL generic wdog /= 0 and only for the last timer. If wdog = 0 then this register is read-only and always '0'.

6 Debug Halt (DH): Value of GPTI.DHALT signal which is used to freeze counters (e.g. when a system is in debug mode). Read-only.

5 Chain (CH): Chain with preceding timer. If set for timer *n*, timer *n* will be decremented each time when timer (*n*-1) underflows.

4 Interrupt Pending (IP): The core sets this bit to '1' when an interrupt is signalled. This bit remains '1' until cleared by writing '1' to this bit, writes of '0' have no effect.

3 Interrupt Enable (IE): If set the timer signals interrupt when it underflows. The reset value for this bit is '0' unless watchdog functionality has been enabled. If watchdog functionality has been enabled then this bit for the last timer will have reset value '1'.

2 Load (LD): Load value from the timer reload register to the timer counter value register. This bit is automatically cleared when the value has been loaded.

1 Restart (RS): If set, the timer counter value register is reloaded with the value of the reload register when the timer underflows

0 Enable (EN): Enable the timer.

31.3.8 Timer N Latch Register

*Table 347.*0xnC, when n selects the times - TLATCHn - Timer n latch register

31	0
LTCV	
0	
r	

31: 0 Latched timer counter value (LTCV): Valued latched from corresponding timer. Read-only.

31.4 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x011. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

31.5 Implementation

31.5.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support *grlib_async_reset_enable*. All registers that react on the reset signal will have a synchronous reset.

31.6 Configuration options

Table 348 shows the configuration options of the core (VHDL generics).

*Table 348.*Configuration options

Generic	Function	Allowed range	Default
pindex	Selects which APB select signal (PSEL) will be used to access the timer unit	0 to NAPBSLV-1	0
paddr	The 12-bit MSB APB address	0 to 4095	0
pmask	The APB address mask	0 to 4095	4095
nbits	Defines the number of bits in the timers	1 to 32	32
ntimers	Defines the number of timers in the unit	1 to 7	1
pirq	Defines which APB interrupt the timers will generate	0 to NAHBIRQ-1	0
sepirq	If set to 1, each timer will drive an individual interrupt line, starting with interrupt *pirq*. If set to 0, all timers will drive the same interrupt line (*pirq*).	0 to 1 (note: *ntimers* + p*irq* must be less than or equal to NAHBIRQ if *sepirq* is set to 1)	0
sbits	Defines the number of bits in the scaler	1 to 32	16
wdog	Watchdog reset value. When set to a non-zero value, the last timer will be enabled and pre-loaded with this value at reset. When the timer value reaches 0, the WDOG output is driven active.	0 to 2^{nbits} - 1	0
ewdogen	External watchdog enable. When set to a non-zero value, the enable bit of the watchdog timer will be set during core reset via the signal gpti.wdogen.Otherwise the enable bit will be set to '1' during core reset.	0 - 1	0
glatch	Enable external timer latch (via interrupt or external vector)	0 - 1	0
gextclk	Enable external timer clock input	0 - 1	0
gset	Enable external timer reload (via interrupt or external vector)	0 - 1	0
gelatch	Enable support for external latch events 0: Timer latch/set is only support for interrupt bus (if enabled via glatch and gset generics) 1: Timer latch/set is disabled after an, unmasked, event on GPTI.LATCHV 2: Timer latch/set is performed on an, unmasked, event on GPTI.LATCHV and timer latch/set is disabled on GPTI.LATCHD events.	0 - 2	0
wdogwin	Enables the watchdog window counter.	0 - 1	0

31.7 Signal descriptions

Table 349 shows the interface signals of the core (VHDL ports).

*Table 349.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
GPTI	DHALT	Input	Freeze timers	High
	EXTCLK	Input	Use as alternative clock	-
	WDOGEN	Input	Sets enable bit of the watchdog timer if VHDL generics wdog and ewdogen are set to non-zero values.	-
	LATCHV[31:0]	Input	External latch/set vector, used if VHDLgeneric gelatch /=0	High
	LATCHD[31:0]	Input	External latch/set disable vector, used if VHDL generic gelatch = 2.	High
GPTO	TICK[0:7]	Output	Timer ticks. TICK[0] is high for one clock each time the scaler underflows. TICK[1-n] are high for one clock each time the corresponding timer underflows.	High
	WDOG	Output	Watchdog output. Equivalent to interrupt pending bit of last timer.	High
	WDOGN	Output	Watchdog output. Equivalent to interrupt pending bit of last timer.	Low

* see GRLIB IP Library User's Manual

31.8 Signal definitions and reset values

When the watchdog times out, the *wdogn* output is driven active low, else it is in tri-state and therefore requires an external pull-up.

The signals and their reset values are described in table 350.

*Table 350.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
wdogn	Tri-state output	Watchdog output. Equivalent to interrupt pending bit of last timer.	Low	Tri-state

31.9 Timing

The timing waveforms and timing parameters are shown in figure 111 and are defined in table 351.

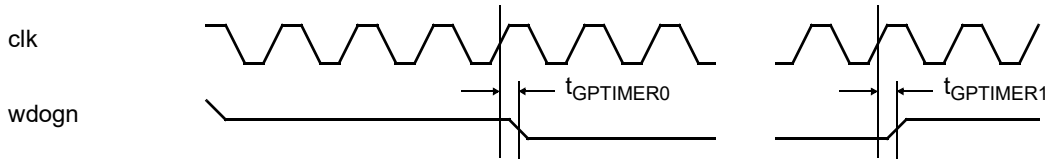


Figure 111. Timing waveforms

*Table 351.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{GPTIMER0}$	clock to output delay	rising *clk* edge	TBD	TBD	ns
$t_{GPTIMER1}$	clock to output tri-state	rising *clk* edge	TBD	TBD	ns

31.10 Library dependencies

Table 352 shows libraries used when instantiating the core (VHDL libraries).

*Table 352.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	MISC	Signals, component	Component declaration

31.11 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.misc.all;

entity gptimer_ex is
  port (
    clk : in std_ulogic;
    rstn : in std_ulogic;

    ... -- other signals
    );
end;

architecture rtl of gptimer_ex is

  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);

  -- GP Timer Unit input signals
  signal gpti : gptimer_in_type;

begin
```

```
  -- AMBA Components are instantiated here
  ...


  -- General Purpose Timer Unit
  timer0 : gptimer
  generic map (pindex => 3, paddr => 3, pirq => 8, sepirq => 1)
  port map (rstn, clk, apbi, apbo(3), gpti, open);

  gpti.dhalt <= '0'; gpti.extclk <= '0'; -- unused inputs

end;
```

32 GR1553B - MIL-STD-1553B / AS15531 Interface

32.1 Overview

This interface core connects the AMBA AHB/APB bus to a single- or dual redundant MIL-STD-1553B bus, and can act as either Bus Controller, Remote Terminal or Bus Monitor.

MIL-STD-1553B (and derived standard SAE AS15531) is a bus standard for transferring data between up to 32 devices over a shared (typically dual-redundant) differential wire. The bus is designed for predictable real-time behavior and fault-tolerance. The raw bus data rate is fixed at 1 Mbit/s, giving a maximum of around 770 kbit/s payload data rate.

One of the terminals on the bus is the Bus Controller (BC), which controls all traffic on the bus. The other terminals are Remote Terminals (RTs), which act on commands issued by the bus controller. Each RT is assigned a unique address between 0-30. In addition, the bus may have passive Bus Monitors (BM:s) connected.

There are 5 possible data transfer types on the MIL-STD-1553 bus:

- BC-to-RT transfer (“receive”)
- RT-to-BC transfer (“transmit”)
- RT-to-RT transfer
- Broadcast BC-to-RTs
- Broadcast RT-to-RTs

Each transfer can contain 1-32 data words of 16 bits each.

The bus controller can also send “mode codes” to the RTs to perform administrative tasks such as time synchronization, and reading out terminal status.

32.2 Electrical interface

The core is connected to the MIL-STD-1553B bus wire through single or dual transceivers, isolation transformers and transformer or stub couplers as shown in figure 112. If single-redundancy is used, the unused bus receive P/N signals should be tied both-high or both-low. The transmitter enables are typically inverted and therefore called transmitter inibit (txinh). See the standard and the respective component’s data sheets for more information on the electrical connection.

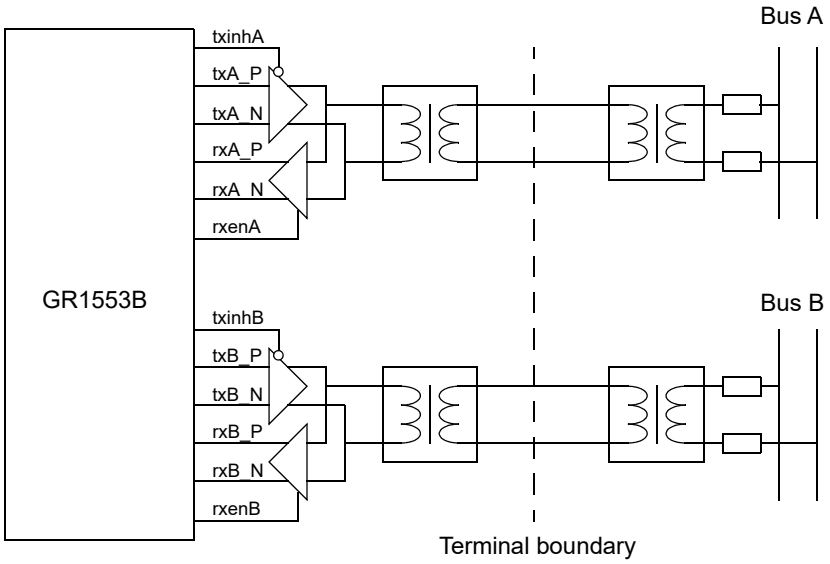


Figure 112. Interface between core and MIL-STD-1553B bus (dual-redundant, transformer coupled)

32.3 Operation

32.3.1 Operating modes

The core contains three separate control units for the Bus Controller, Remote Terminal and Bus Monitor handling, with a shared 1553 codec. All parts may not be present in the hardware, which parts are available can be checked from software by looking at the BCSUP/RTSUP/BMSUP register bits.

The operating mode of the core is controlled by starting and stopping of the BC/RT/BM units via register writes. At start-up, none of the parts are enabled, and the core is completely passive on both the 1553 and AMBA bus.

The BC and RT parts of the core can not be active on the 1553 bus at the same time. While the BC is running or suspended, only the BC (and possibly BM) has access to the 1553 bus, and the RT can only receive and respond to commands when both the BC schedules are completely stopped (not running or even suspended).

The Bus Monitor, however, is only listening on the codec receivers and can therefore operate regardless of the enabled/disabled state of the other two parts.

32.3.2 Register interface

The core is configured and controlled through control registers accessed over the APB bus. Each of the BC,RT,BM parts has a separate set of registers, plus there is a small set of shared registers.

Some of the control register fields for the BC and RT are protected using a ‘key’, a field in the same register that has to be written with a certain value for the write to take effect. The purpose of the keys are to give RT/BM designers a way to ensure that the software can not interfere with the bus traffic by enabling the BC or changing the RT address. If the software is built without knowledge of the key to a certain register, it is very unlikely that it will accidentally perform a write with the correct key to that control register.

32.3.3 Interrupting

The core has one interrupt output, which can be generated from several different source events. Which events should cause an interrupt can be controlled through the IRQ Enable Mask register.

32.3.4 MIL-STD-1553 Codec

The core’s internal codec receives and transmits data words on the 1553 bus, and generates and checks sync patterns and parity.

Loop-back checking logic checks that each transmitted word is also seen on the receive inputs. If the transmitted word is not echoed back, the transmitter stops and signals an error condition, which is then reported back to the user.

32.4 Bus Controller Operation

32.4.1 Overview

When operating as Bus Controller, the core acts as master on the MIL-STD-1553 bus, initiates and performs transfers.

This mode works based on a scheduled transfer list concept. The software sets up in memory a sequence of transfer descriptors and branches, data buffers for sent and received data, and an IRQ pointer ring buffer. When the schedule is started (through a BC action register write), the core processes the list, performs the transfers one after another and writes resulting status into the transfer list and incoming data into the corresponding buffers.

32.4.2 Timing control

In each transfer descriptor in the schedule is a “slot time” field. If the scheduled transfer finishes sooner than its slot time, the core will pause the remaining time before scheduling the next command. This allows the user to accurately control the message timing during a communication frame.

If the transfer uses more than its slot time, the overshooting time will be subtracted from the following command’s time slot. The following command may in turn borrow time from the following command and so on. The core can keep track of up to one second of borrowed time, and will not insert pauses again until the balance is positive, except for intermessage gaps and pauses that the standard requires.

If you wish to execute the schedule as fast as possible you can set all slot times in the schedule to zero. If you want to group a number of transfers you can move all the slot time to the last transfer.

The schedule can be stopped or suspended by writing into the BC action register. When suspended, the schedule’s time will still be accounted, so that the schedule timing will still be correct when the schedule is resumed. When stopped, on the other hand, the schedule’s timers will be reset.

When the extsync bit is set in the schedule’s next transfer descriptor, the core will wait for a positive edge on the external sync input before starting the command. The schedule timer and the time slot balance will then be reset and the command is started. If the sync pulse arrives before the transfer is reached, it is stored so the command will begin immediately. The trigger memory is cleared when stopping (but not when suspending) the schedule. Also, the trigger can be set/cleared by software through the BC action register.

32.4.3 Bus selection

Each transfer descriptor has a bus selection bit that allows you to control on which one of the two redundant buses (‘0’ for bus A, ‘1’ for bus B) the transfer will occur.

Another way to control the bus usage is through the per-RT bus swap register, which has one register bit for each RT address. The bus swap register is an optional feature, software can check the BCFEAT read-only register field to see if it is available.

Writing a ‘1’ to a bit in the per-RT Bus Swap register inverts the meaning of the bus selection bit for all transfers to the corresponding RT, so ‘0’ now means bus ‘B’ and ‘1’ means bus ‘A’. This allows you to switch all transfers to one or a set of RT:s over to the other bus with a single register write and without having to modify any descriptors.

The hardware determines which bus to use by taking the exclusive-or of the bus swap register bit and the bus selection bit. Normally it only makes sense to use one of these two methods for each RT, either the bus selection bit is always zero and the swap register is used, or the swap register bit is always zero and the bus selection bit is used.

If the bus swap register is used for bus selection, the store-bus descriptor bit can be enabled to automatically update the register depending on transfer outcome. If the transfer succeeded on bus A, the bus swap register bit is set to ‘0’, if it succeeds on bus B, the swap register bit is set to ‘1’. If the transfer fails, the bus swap register is set to the opposite value.

32.4.4 Secondary transfer list

The core can be set up with a secondary “asynchronous” transfer list with the same format as the ordinary schedule. This transfer list can be commanded to start at any time during the ordinary schedule. While the core is waiting for a scheduled command’s slot time to finish, it will check if the next asynchronous transfer’s slot time is lower than the remaining sleep time. In that case, the asynchronous command will be scheduled.

If the asynchronous command doesn’t finish in time, time will be borrowed from the next command in the ordinary schedule. In order to not disturb the ordinary schedule, the slot time for the asynchronous messages must therefore be set to pessimistic values.

The exclusive bit in the transfer descriptor can be set if one does not want an asynchronous command scheduled during the sleep time following the transfer.

Asynchronous messages will not be scheduled while the schedule is waiting for a sync pulse or the schedule is suspended and the current slot time has expired, since it is then not known when the next scheduled command will start.

32.4.5 Interrupt generation

Each command in the transfer schedule can be set to generate an interrupt after certain transfers have completed, with or without error. Invalid command descriptors always generate interrupts and stop the schedule. Before a transfer-triggered interrupt is generated, the address to the corresponding descriptor is written into the BC transfer-triggered IRQ ring buffer and the BC Transfer-triggered IRQ Ring Position Register is incremented.

A separate error interrupt signals DMA errors. If a DMA error occurs when reading/writing descriptors, the executing schedule will be suspended. DMA errors in data buffers will cause the corresponding transfer to fail with an error code (see table 356).

Whether any of these interrupt events actually cause an interrupt request on the AMBA bus is controlled by the IRQ Mask Register setting.

32.4.6 Transfer list format

The BC:s transfer list is an array of transfer descriptors mixed with branches as shown in table 353. Each entry has to be aligned to start on a 128-bit (16-byte) boundary. The two unused words in the branch case are free to be used by software to store arbitrary data.

*Table 353.*GR1553B transfer descriptor format

Offset	Value for transfer descriptor	DMA R/W	Value for branch	DMA R/W
0x00	Transfer descriptor word 0 (see table 354)	R	Condition word (see table 358)	R
0x04	Transfer descriptor word 1 (see table 355)	R	Jump address, 128-bit aligned	R
0x08	Data buffer pointer, 16-bit aligned. For write buffers, if bit 0 is set the received data is discarded and the pointer is ignored. This can be used for RT-to-RT transfers where the BC is not interested in the data transferred.	R	Unused	-
0x0C	Result word, written by core (see table 356)	W	Unused	-

The transfer descriptor words are structured as shown in tables 354-356 below.

*Table 354.*GR1553B BC transfer descriptor word 0 (offset 0x00)

31	30	29	28	27	26	25	24	23	22	20	19	18	17	16	15	0
0	WTRIG	EXCL	IRQE	IRQN	SUSE	SUSN	RETMD		NRET		STBUS	GAP	RESERVED		STIME	

31	Must be 0 to identify as descriptor
30	Wait for external trigger (WTRIG)
29	Exclusive time slot (EXCL) - Do not schedule asynchronous messages
28	IRQ after transfer on Error (IRQE)
27	IRQ normally (IRQN) - Always interrupts after transfer
26	Suspend on Error (SUSE) - Suspends the schedule (or stops the async transfer list) on error
25	Suspend normally (SUSN) - Always suspends after transfer
24 : 23	Retry mode (RETMD). 00 - Retry on same bus only. 01 - Retry alternating on both buses 10: Retry first on same bus, then on alternating bus. 11 - Reserved, do not use
22 : 20	Number of retries (NRET) - Number of automatic retries per bus The total number of tries (including the first attempt) is NRET+1 for RETMD=00, 2 x (NRET+1) for RETMD=01/10
19	Store bus (STBUS) - If the transfer succeeds and this bit is set, store the bus on which the transfer succeeded (0 for bus A, 1 for bus B) into the per-RT bus swap register. If the transfer fails and this bit is set, store the opposite bus instead. (only if the per-RT bus mask is supported in the core) See section 32.4.3 for more information.
18	Extended intermessage gap (GAP) - If set, adds an additional amount of gap time, corresponding to the RTTO field, after the transfer
17 : 16	Reserved - Set to 0 for forward compatibility
15 : 0	Slot time (STIME) - Allocated time in 4 microsecond units, remaining time after transfer will insert delay

*Table 355.*GR1553B BC transfer descriptor word 1 (offset 0x04)

31	30	29	26	25	21	20	16	15	11	10	9	5	4	0
DUM	BUS	RTTO		RTAD2		RTSA2		RTAD1		TR	RTSA1		WCMC	

31	Dummy transfer (DUM) - If set to ‘1’ no bus traffic is generated and transfer “succeeds” immediately For dummy transfers, the EXCL,IRQN,SUSN,STBUS,GAP,STIME settings are still in effect, other bits and the data buffer pointer are ignored.	
30	Bus selection (BUS) - Bus to use for transfer, 0 - Bus A, 1 - Bus B	
29:26	RT Timeout (RTTO) - Extra RT status word timeout above nominal in units of 4 us (0000 -14 us, 1111 -74 us). Note: This extra time is also used as extra intermessage gap time if the GAP bit is set.	
25:21	Second RT Address for RT-to-RT transfer (RTAD2)	See table 357 for details on how to setup RTAD1,RTSA1,RTAD2,RTSA2,WCMC,TR for different transfer types. Note that bits 15:0 correspond to the (first) command word on the 1553 bus
20:16	Second RT Subaddress for RT-to-RT transfer (RTSA2)	
15:11	RT Address (RTAD1)	
10	Transmit/receive (TR)	
9:5	RT Subaddress (RTSA1)	
4:0	Word count/Mode code (WCMC)	

*Table 356.*GR1553B transfer descriptor result word (offset 0x0C)

31	30 24	23 16	15 8	7 4	3	2 0
0	Reserved	RT2ST	RTST	RETCNT	RES	TFRST

31	Always written as 0
30:24	Reserved - Mask away on read for forward compatibility
23:16	RT 2 Status Bits (RT2ST) - Status bits from receiving RT in RT-to-RT transfer, otherwise 0 Same bit pattern as for RTST below
15:8	RT Status Bits (RTST) - Status bits from RT (transmitting RT in RT-to-RT transfer) 15 - Message error, 14 - Instrumentation bit or reserved bit set, 13 - Service request, 12 - Broadcast command received, 11 - Busy bit, 10 - Subsystem flag, 9 - Dynamic bus control acceptance, 8 - Terminal flag
7:4	Retry count (RETCNT) - Number of retries performed
3	Reserved - Mask away on read for forward compatibility
2:0	Transfer status (TFRST) - Outcome of last try 000 - Success (or dummy bit was set) 001 - RT did not respond (transmitting RT in RT-to-RT transfer) 010 - Receiving RT of RT-to-RT transfer did not respond 011 - A responding RT:s status word had message error, busy, instrumentation or reserved bit set (*) 100 - Protocol error (improperly timed data words, decoder error, wrong number of data words) 101 - The transfer descriptor was invalid 110 - Data buffer DMA timeout or error response 111 - Transfer aborted due to loop back check failure

* Error code 011 is issued only when the number of data words match the success case, otherwise code 100 is used. Error code 011 can be issued for a correctly executed “transmit last command” or “transmit last status word” mode code since these commands do not reset the status word.

*Table 357.*GR1553B BC Transfer configuration bits for different transfer types

Transfer type	**RTAD1 (15:11)**	**RTSA1 (9:5)**	**RTAD2 (25:21)**	**RTSA2 (20:16)**	**WCMC (4:0)**	**TR (10)**	**Data buffer direction**
Data, BC-to-RT	RT address (0-30)	RT subaddr (1-30)	Don’t care	0	Word count (0 for 32)	0	Read (2-64 bytes)
Data, RT-to-BC	RT address (0-30)	RT subaddr (1-30)	Don’t care	0	Word count (0 for 32)	1	Write (2-64 bytes)
Data, RT-to-RT	Recv-RT addr (0-30)	Recv-RT subad. (1-30)	Xmit-RT addr (0-30)	Xmit-RT subad. (1-30)	Word count (0 for 32)	0	Write (2-64 bytes)
Mode, no data	RT address (0-30)	0 or 31 (*)	Don’t care	Don’t care	Mode code (0-8)	1	Unused
Mode, RT-to-BC	RT address (0-30)	0 or 31 (*)	Don’t care	Don’t care	Mode code (16/18/19)	1	Write (2 bytes)
Mode, BC-to-RT	RT address (0-30)	0 or 31 (*)	Don’t care	Don’t care	Mode code (17/20/21)	0	Read (2 bytes)
Broadcast Data, BC-to-RTs	31	RTs subaddr (1-30)	Don’t care	0	Word count (0 for 32)	0	Read (2-64 bytes)
Broadcast Data, RT-to-RTs	31	Recv-RTs subad. (1-30)	Xmit-RT addr (0-30)	Xmit-RT subad. (1-30)	Word count (0 for 32)	0	Write (2-64 bytes)
Broadcast Mode, no data	31	0 or 31 (*)	Don’t care	Don’t care	Mode code (1, 3-8)	1	Unused
Broadcast Mode, BC-to-RT	31	0 or 31 (*)	Don’t care	Don’t care	Mode code (17/20/21)	0	Read (2 bytes)

(*) The standard allows using either of subaddress 0 or 31 for mode commands.

The branch condition word is formed as shown in table 358.

*Table 358.*GR1553B branch condition word (offset 0x00)

31	30 27	26	25	24	23 16	15 8	7 0
1	Reserved (0)	IRQC	ACT	MODE	RT2CC	RTCC	STCC

31	Must be 1 to identify as branch
30 : 27	Reserved - Set to 0
26	Interrupt if condition met (IRQC)
25	Action (ACT) - What to do if condition is met, 0 - Suspend schedule, 1 - Jump
24	Logic mode (MODE): 0 = Or mode (any bit set in RT2CC, RTCC is set in RT2ST,RTST, or result is in STCC mask) 1 - And mode (all bits set in RT2CC,RTCC are set in RT2ST,RTST and result is in STCC mask)
23:16	RT 2 Condition Code (RT2CC) - Mask with bits corresponding to RT2ST in result word of last transfer
15:8	RT Condition Code (RTCC) - Mask with bits corresponding to RTST in result word of last transfer
7:0	Status Condition Code (STCC) - Mask with bits corresponding to status value of last transfer

Note that you can get a constant true condition by setting MODE=0 and STCC=0xFF, and a constant false condition by setting STCC=0x00. 0x800000FF can thus be used as an end-of-list marker.

32.5 Remote Terminal Operation

32.5.1 Overview

When operating as Remote Terminal, the core acts as a slave on the MIL-STD-1553B bus. It listens for requests to its own RT address (or broadcast transfers), checks whether they are configured as legal and, if legal, performs the corresponding transfer or, if illegal, sets the message error flag in the status word. Legality is controlled by the subaddress control word for data transfers and by the mode code control register for mode codes.

To start the RT, set up the subaddress table and log ring buffer, and then write the address and RT enable bit is into the RT Config Register.

32.5.2 Data transfer handling

The Remote Terminal mode uses a three-level structure to handle data transfer DMA. The top level is a subaddress table, where each subaddress has a subaddress control word, and pointers to a transmit descriptor and a receive descriptor. Each descriptor in turn contains a descriptor control/status word, pointer to a data buffer, and a pointer to a next descriptor, forming a linked list or ring of descriptors. Data buffers can reside anywhere in memory with 16-bit alignment.

When the RT receives a data transfer request, it checks in the subaddress table that the request is legal. If it is legal, the transfer is then performed with DMA to or from the corresponding data buffer. After a data transfer, the descriptor's control/status word is updated with success or failure status and the subaddress table pointer is changed to point to the next descriptor.

If logging is enabled, a log entry will be written into a log ring buffer area. A transfer-triggered IRQ may also be enabled. To identify which transfer caused the interrupt, the RT Event Log IRQ Position points to the corresponding log entry. For that reason, logging must be enabled in order to enable interrupts.

If a request is legal but can not be fulfilled, either because there is no valid descriptor ready or because the data can not be accessed within the required response time, the core will signal a RT table access error interrupt and not respond to the request. Optionally, the terminal flag status bit can be automatically set on these error conditions.

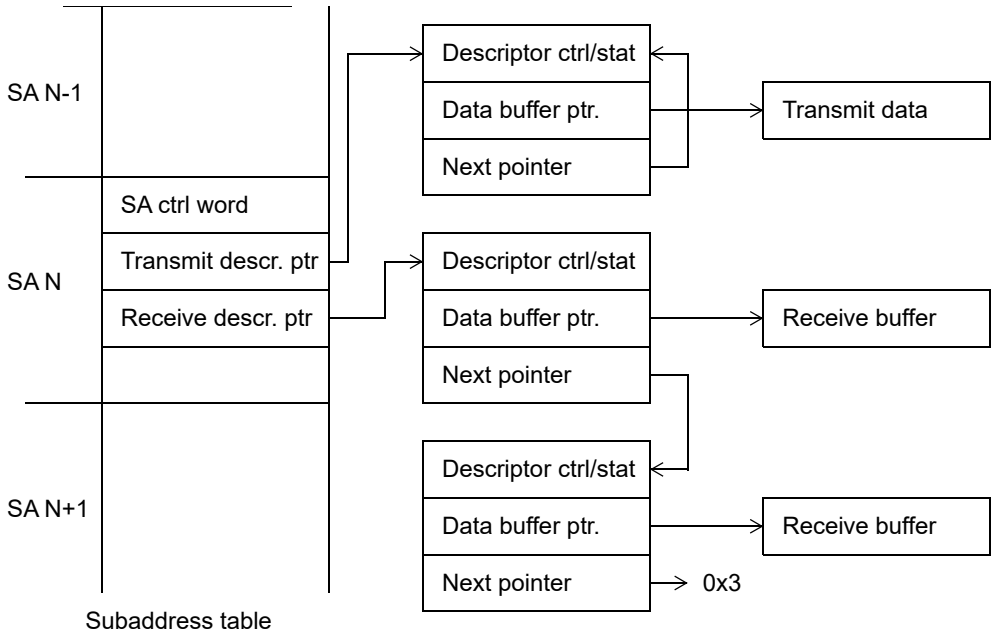


Figure 113. RT subaddress data structure example diagram

32.5.3 Mode Codes

Which of the MIL-STD-1553B mode codes that are legal and should be logged and interrupted are controlled by the RT Mode Code Control register. As for data transfers, to enable interrupts you must also enable logging. Inhibit mode codes are controlled by the same fields as their non-inhibit counterpart and mode codes that can be broadcast have two separate fields to control the broadcast and non-broadcast variants.

The different mode codes and the corresponding action taken by the RT are tabulated below. Some mode codes do not have a built-in action, so they will need to be implemented in software if desired. The relation between each mode code to the fields in the RT Mode Code control register is also shown.

*Table 359.*RT Mode Codes

Mode code		Description	Built-in action, if mode code is enabled	Can log/ IRQ	Enabled after reset	Ctrl. reg bits
0	00000	Dynamic bus control	If the DBCA bit is set in the RT Bus Status register, a Dynamic Bus Control Acceptance response is sent.	Yes	No	17:16
1	00001	Synchronize	The time field in the RT sync register is updated. The output rtsync is pulsed high one AMBA cycle.	Yes	Yes	3:0
2	00010	Transmit status word	Transmits the RT:s status word Enabled always, can not be logged or disabled.	No	Yes	-
3	00011	Initiate self test	No built-in action	Yes	No	21:18
4	00100	Transmitter shutdown	The RT will stop responding to commands on the other bus (not the bus on which this command was given).	Yes	Yes	11:8
5	00101	Override transmitter shutdown	Removes the effect of an earlier transmitter shutdown mode code received on the same bus	Yes	Yes	11:8
6	00110	Inhibit terminal flag	Masks the terminal flag of the sent RT status words	Yes	No	25:22
7	00111	Override inhibit terminal flag	Removes the effect of an earlier inhibit terminal flag mode code.	Yes	No	25:22
8	01000	Reset remote terminal	The fail-safe timers, transmitter shutdown and inhibit terminal flag inhibit status are reset. The Terminal Flag and Service Request bits in the RT Bus Status register are cleared. The extreset output is pulsed high one AMBA cycle.	Yes	No	29:26
16	10000	Transmit vector word	Responds with vector word from RT Status Words Register	Yes	No	13:12
17	10001	Synchronize with data word	The time and data fields in the RT sync register are updated. The rtsync output is pulsed high one AMBA cycle	Yes	Yes	7:4
18	10010	Transmit last command	Transmits the last command sent to the RT. Enabled always, can not be logged or disabled.	No	Yes	-
19	10011	Transmit BIT word	Responds with BIT word from RT Status Words Register	Yes	No	15:14
20	10100	Selected transmitter shutdown	No built-in action	No	No	-
21	10101	Override selected transmitter shutdown	No built-in action	No	No	-

32.5.4 Event Log

The event log is a ring of 32-bit entries, each entry having the format given in table 360. Note that for data transfers, bits 23-0 in the event log are identical to bits 23-0 in the descriptor status word.

*Table 360.*GR1553B RT Event Log entry format

31	30 29	28 24	23 10	9	8 3	2 0
IRQSR	TYPE	SAMC	TIMEL	BC	SZ	TRES

31	IRQ Source (IRQSRC) - Set to '1' if this transfer caused an interrupt
30 : 29	Transfer type (TYPE) - 00 - Transmit data, 01 - Receive data, 10 - Mode code
28 : 24	Subaddress / Mode code (SAMC) - If TYPE=00/01 this is the transfer subaddress, If TYPE=10, this is the mode code
23 : 10	TIMEL - Low 14 bits of time tag counter.
9	Broadcast (BC) - Set to 1 if request was to the broadcast address
8 : 3	Transfer size (SZ) - Count in 16-bit words (0-32)
2 : 0	Transfer result (TRES) 000 = Success 001 = Superseded (canceled because a new command was given on the other bus) 010 = DMA error or memory timeout occurred 011 = Protocol error (improperly timed data words or decoder error) 100 = The busy bit or message error bit was set in the transmitted status word and no data was sent 101 = Transfer aborted due to loop back checker error

32.5.5 Subaddress table format

*Table 361.*GR1553B RT Subaddress table entry for subaddress number N, 0<N<31

Offset	Value	DMA R/W
0x10*N + 0x00	Subaddress N control word (table 362)	R
0x10*N + 0x04	Transmit descriptor pointer, 16-byte aligned (0x3 to indicate invalid pointer)	R/W
0x10*N + 0x08	Receive descriptor pointer, 16-byte aligned (0x3 to indicate invalid pointer)	R/W
0x10*N + 0x0C	Unused	-

Note: The table entries for mode code subaddresses 0 and 31 are never accessed by the core.

*Table 362.*GR1553B RT Subaddress table control word (offset 0x00)

31 19	18	17	16	15	14	13	12 8	7	6	5	4 0
0 (reserved)	WRAP	IGNDV	BCRXE	RXEN	RXLOG	RXIRQ	RXSZ	TXEN	TXLOG	TXIRQ	TXSZ

31 : 19	Reserved - set to 0 for forward compatibility
18	Auto-wraparound enable (WRAP) - Enables a test mode for this subaddress, where transmit transfers send back the last received data. This is done by copying the finished transfer's descriptor pointer to the transmit descriptor pointer address after each successful transfer. Note: If WRAP=1, you should not set TXSZ > RXSZ as this might cause reading beyond buffer end
17	Ignore data valid bit (IGNDV) - If this is '1' then receive transfers will proceed (and overwrite the buffer) if the receive descriptor has the data valid bit set, instead of not responding to the request. This can be used for descriptor rings where you don't care if the oldest data is overwritten.
16	Broadcast receive enable (BCRXEN) - Allow broadcast receive transfers to this subaddress
15	Receive enable (RXEN) - Allow receive transfers to this subaddress
14	Log receive transfers (RXLOG) - Log all receive transfers in event log ring (only used if RXEN=1)
13	Interrupt on receive transfers (RXIRQ) - Each receive transfer will cause an interrupt (only if also RXEN,RXLOG=1)
12 : 8	Maximum legal receive size (RXSZ) to this subaddress - in16-bit words, 0 means 32
7	Transmit enable (TXEN) - Allow transmit transfers from this subaddress
6	Log transmit transfers (TXLOG) - Log all transmit transfers in event log ring (only if also TXEN=1)
5	Interrupt on transmit transfers (TXIRQ) - Each transmit transfer will cause an interrupt (only if TXEN,TXLOG=1)
4 : 0	Maximum legal transmit size (TXSZ) from this subaddress - in 16-bit words, 0 means 32

*Table 363.*GR1553B RT Descriptor format

Offset	Value	DMA R/W
0x00	Control and status word, see table 364	R/W
0x04	Data buffer pointer, 16-bit aligned	R
0x08	Pointer to next descriptor, 16-byte aligned or 0x0000003 to indicate end of list	R

*Table 364.*GR1553B RT Descriptor control/status word (offset 0x00)

31	30	29 26	25 10	9	8 3	2 0
DV	IRQEN	Reserved (0)	TIME	BC	SZ	TRES

31	Data valid (DV) - Should be set to 0 by software before and set to 1 by hardware after transfer. If DV=1 in the current receive descriptor before the receive transfer begins then a descriptor table error will be triggered. You can override this by setting the IGNDV bit in the subaddress table.
30	IRQ Enable override (IRQEN) - Log and IRQ after transfer regardless of SA control word settings Can be used for getting an interrupt when nearing the end of a descriptor list.
29 : 26	Reserved - Write 0 and mask out on read for forward compatibility
25 : 10	Transmission time tag (TTIME) - Set by the core to the value of the RT timer when the transfer finished.
9	Broadcast (BC) - Set by the core if the transfer was a broadcast transfer
8 : 3	Transfer size (SZ) - Count in 16-bit words (0-32)
2 : 0	Transfer result (TRES) 000 = Success 001 = Superseded (canceled because a new command was given on the other bus) 010 = DMA error or memory timeout occurred 011 = Protocol error (improperly timed data words or decoder error) 100 = The busy bit or message error bit was set in the transmitted status word and no data was sent 101 = Transfer aborted due to loop back checker error

32.6 Bus Monitor Operation

32.6.1 Overview

The Bus Monitor (BM) can be enabled by itself, or in parallel to the BC or RT. The BM acts as a passive logging device, writing received data with time stamps to a ring buffer.

32.6.2 Filtering

The Bus Monitor can also support filtering. This is an optional feature, software can check for this by testing whether the BM filter registers are writable.

Transfers can be filtered per RT address and per subaddress or mode code, and the filter conditions are logically AND:ed. If all bits of the three filter registers and bits 2-3 of the control register are set to '1', the BM core will log all words that are received on the bus.

In order to filter on subaddress/mode code, the BM has logic to track 1553 words belonging to the same message. All 10 message types are supported. If an unexpected word appears, the filter logic will restart. Data words not appearing to belong to any message can be logged by setting a bit in the control register.

The filter logic can be manually restarted by setting the BM enable bit low and then back to high. This feature is mainly to improve testability of the BM itself.

The filtering capability can be configured out of the BM to save area. If this is done, all words seen are logged and the filter control registers become read-only and always read out as all-ones. You can, however, still control whether Manchester/parity errors are logged.

32.6.3 No-response handling

In the MIL-STD-1553B protocol, a command word for a mode code using indicator 0 or a regular transfer to subaddress 8 has the same structure as a legal status word. Therefore ambiguity can arise when the subaddress or mode code filters are used, an RT is not responding on a subaddress, and the BC then commands the same RT again on subaddress 8 or mode code indicator 0 on the same bus. This can lead to the second command word being interpreted as a status word and filtered out.

The BM can use the instrumentation bit and reserved bits to disambiguate, which means that this case will never occur when subaddresses 1-7, 9-30 and mode code indicator 31 are used. Also, this case does not occur when the subaddress/mode code filters are unused and only the RT address filter is used.

32.6.4 Log entry format

Each log entry is two 32-bit words.

*Table 365.*GR1553B BM Log entry word 0 (offset 0x00)

31	30 24	23 0
1	Reserved	TIME

31	Always written as 1
30 : 24	Reserved - Mask out on read for forward compatibility
23 : 0	Time tag (TIME)

*Table 366.*GR1553B BM Log entry word 1 (offset 0x04)

31	30 20	19	18 17	16	15 0
0	Reserved	BUS	WST	WTP	WD

31	Always written as 0
30 : 20	Reserved - Mask out on read for forward compatibility
19	Receive data bus (BUS) - 0:A, 1:B
18 : 17	Word status (WST) - 00=word OK, 01=Manchester error, 10=Parity error
16	Word type (WTP) - 0:Data, 1:Command/status
15 : 0	Word data (WD)

32.7 Clocking

The core needs a separate clock for the 1553 codec.

The core operates in two clock domains, the AMBA clock domain and the 1553 codec clock domain, with synchronization and handshaking between the domains. The AMBA clock can be at any frequency but must be at a minimum of 10 MHz. A propagation delay of up to one codec clock cycle (50 ns) can be tolerated in each clock-domain crossing signal.

The core has two separate reset inputs for the two clock domains. They should be reset simultaneously, for instance by using two Reset generator cores connected to the same reset input but clocked by the respective clocks.

32.8 Registers

The core is programmed through registers mapped into APB address space. If the RT, BC or BM parts of the core have been configured out, the corresponding registers will become unimplemented and return zero when read. Reserved register fields should be written as zeroes and masked out on read.

*Table 367.*MIL-STD-1553B interface registers

APB address offset	Register	R/W	Reset value
0x00	IRQ Register	RW (write '1' to clear)	0x00000000
0x04	IRQ Enable	RW	0x00000000
0x08...0x0F	(Reserved)		
0x10	Hardware config register	R (constant)	0x00000000*
0x14...0x3F	(Reserved)		
0x40...0x7F	BC Register area (see table 368)		
0x80...0xBF	RT Register area (see table 369)		
0xC0...0xFF	BM Register area (see table 370)		

(*) May differ depending on core configuration

*Table 368.*MIL-STD-1553B interface BC-specific registers

APB address offset	Register	R/W	Reset value
0x40	BC Status and Config register	RW	0xf0000000*
0x44	BC Action register	W	
0x48	BC Transfer list next pointer	RW	0x00000000
0x4C	BC Asynchronous list next pointer	RW	0x00000000
0x50	BC Timer register	R	0x00000000
0x54	BC Timer wake-up register	RW	0x00000000
0x58	BC Transfer-triggered IRQ ring position	RW	0x00000000
0x5C	BC Per-RT bus swap register	RW	0x00000000
0x60...0x67	(Reserved)		
0x68	BC Transfer list current slot pointer	R	0x00000000
0x6C	BC Asynchronous list current slot pointer	R	0x00000000
0x70...0x7F	(Reserved)		

(*) May differ depending on core configuration

*Table 369.*MIL-STD-1553B interface RT-specific registers

APB address offset	Register	R/W	Reset value
0x80	RT Status register	R	0x80000000*
0x84	RT Config register	RW	0x0000e03e***
0x88	RT Bus status bits register	RW	0x00000000
0x8C	RT Status words register	RW	0x00000000
0x90	RT Sync register	R	0x00000000
0x94	RT Subaddress table base address	RW	0x00000000
0x98	RT Mode code control register	RW	0x00000555
0x9C...0xA3	(Reserved)		
0xA4	RT Time tag control register	RW	0x00000000
0xA8	(Reserved)		
0xAC	RT Event log size mask	RW	0xfffffffc
0xB0	RT Event log position	RW	0x00000000
0xB4	RT Event log interrupt position	R	0x00000000
0xB8.. 0xBF	(Reserved)		

(*) May differ depending on core configuration

(***) Reset value is affected by the external RTADDR/RTPAR input signals

*Table 370.*MIL-STD-1553B interface BM-specific registers

APB address offset	Register	R/W	Reset value
0xC0	BM Status register	R	0x80000000*
0xC4	BM Control register	RW	0x00000000
0xC8	BM RT Address filter register	RW	0xffffffff
0xCC	BM RT Subaddress filter register	RW	0xffffffff
0xD0	BM RT Mode code filter register	RW	0xffffffff
0xD4	BM Log buffer start	RW	0x00000000
0xD8	BM Log buffer end	RW	0x00000007
0xDC	BM Log buffer position	RW	0x00000000
0xE0	BM Time tag control register	RW	0x00000000
0xE4...0xFF	(Reserved)		

(*) May differ depending on core configuration

32.8.1 IRQ Register

*Table 371.*0x00 - IRQ - GR1553B IRQ Register

31 18	17	16	15 11	10	9	8	7 3	2	1	0
RESERVED	BMTOF	BMD	RESERVED	RTTE	RTD	RTEV	RESERVED	BCWK	BCD	BCEV
0	0	0	0	0	0	0	0	0	0	0
r	wc	wc	r	wc	wc	wc	r	wc	wc	wc

Bits read '1' if interrupt occurred, write back '1' to acknowledge

17 BM Timer overflow (BMTOF)

16 BM DMA Error (BMD)

10 RT Table access error (RTTE)

9 RT DMA Error (RTD)

8 RT transfer-triggered event interrupt (RTEV)

2 BC Wake-up timer interrupt (BCWK)

1 BC DMA Error (BCD)

0 BC Transfer-triggered event interrupt (BCEV)

32.8.2 IRQ Enable Register

*Table 372.*0x04 - IRQE - GR1553B IRQ Enable Register

31 18	17	16	15 11	10	9	8	7 3	2	1	0
RESERVED	BMTOE	BMDE	RESERVED	RTTEE	RTDE	RTEVE	RESERVED	BCWKE	BCDE	BCEVE
0	0	0	0	0	0	0	0	0	0	0
r	rw	rw	r	rw	rw	rw	r	rw	rw	rw

17 BM Timer overflow interrupt enable (BMTOE)

16 BM DMA error interrupt enable (BMDE)

10 RT Table access error interrupt enable (RTTEE)

9 RT DMA error interrupt enable (RTDE)

8 RT Transfer-triggered event interrupt enable (RTEVE)

2 BC Wake up timer interrupt (BCWKE)

1 BC DMA Error Enable (BCDE)

0 BC Transfer-triggered event interrupt (BCEVE)

32.8.3 Hardware Configuration Register

*Table 373.*GR1553B Hardware Configuration Register

31	30 12	11	10 9	8	7 0
MOD	RESERVED	XKEYS	ENDIAN	SCLK	CCFREQ
*	0	*	*	*	'
r	r	r	r	r	r

Note: This register reads 0x0000 for the standard configuration of the core

31 Modified (MOD) - Reserved to indicate that the core has been modified / customized in an unspecified manner

11 Set if safety keys are enabled for the BM Control Register and for all RT Control Register fields.

10 : 9 AHB Endianness - 00=Big-endian, 01=Little-endian, 10/11=Reserved

8 Same clock (SCLK) - Reserved for future versions to indicate that the core has been modified to run with a single clock

7 : 0 Codec clock frequency (CCFREQ) - Reserved for future versions of the core to indicate that the core runs at a different codec clock frequency. Frequency value in MHz, a value of 0 means 20 MHz.

32.8.4 BC Status and Config Register

*Table 374.*0x40 - BCSL - GR1553B BC Status and Config Register

31	30 28	27 17	16	15 11	10	9 8	7 3	2 0
BCSUP	BCFEAT	RESERVED	BCCHK	ASADL	R	ASST	SCADL	SCST
*	*	0	0	0	0	0	0	0
r	r	r	rw	r	r	r	r	r

31 BC Supported (BCSUP) - Reads '1' if core supports BC mode

30 : 28 BC Features (BCFEAT) - Bit field describing supported optional features ('1'=supported):

- 30 BC Schedule timer supported
- 29 BC Schedule time wake-up interrupt supported
- 28 BC per-RT bus swap register and STBUS descriptor bit supported

16 Check broadcasts (BCCHK) - Writable bit, if set to '1' enables waiting and checking for (unexpected) responses to all broadcasts.

15 : 11 Asynchronous list address low bits (ASADL) - Bit 8-4 of currently executing (if ASST=01) or next asynchronous command descriptor address

9 : 8 Asynchronous list state (ASST) - 00=Stopped, 01=Executing command, 10=Waiting for time slot

7 : 3 Schedule address low bits (SCADL) - Bit 8-4 of currently executing (if SCST=001) or next schedule descriptor address

2 : 0 Schedule state (SCST) - 000=Stopped, 001=Executing command, 010=Waiting for time slot, 011=Suspended, 100=Waiting for external trigger

32.8.5 BC Action Register

*Table 375.*0x44 - BCA - GR1553B BC Action Register

31 16	15 10	9	8	7 5	4	3	2	1	0
BCKEY	RESERVED	ASSTP	ASSRT	RESERVED	CLRT	SETT	SCSTP	SCSUS	SCSRT
-	-	-	-	-	-	-	-	-	-
w	-	w	w	-	w	w	w	w	w

31 : 16 Safety code (BCKEY) - Must be 0x1552 when writing, otherwise register write is ignored

9 Asynchronous list stop (ASSTP) - Write '1' to stop asynchronous list (after current transfer, if executing)

8 Asynchronous list start (ASSRT) - Write '1' to start asynchronous list

4 Clear external trigger (CLRT) - Write '1' to clear trigger memory

3 Set external trigger (SETT) - Write '1' to force the trigger memory to set

2 Schedule stop (SCSTP) - Write '1' to stop schedule (after current transfer, if executing)

1 Schedule suspend (SCSUS) - Write '1' to suspend schedule (after current transfer, if executing)

0 Schedule start (SCSRT) - Write '1' to start schedule

32.8.6 BC Tranfer List Next Pointer Register

*Table 376.*0x48 - BCTNP - GR1553B BC Transfer list next pointer register

31 0
SCHEDULE TRANSFER LIST POINTER
0
rw

31 : 0 Read: Currently executing (if SCST=001) or next transfer to be executed in regular schedule.
Write: Change address. If running, this will cause a jump after the current transfer has finished.

32.8.7 BC Asynchronous List Next Pointer Register

*Table 377.*0x4C - BCANP - GR1553B BC Asynchronous list next pointer register

31	0
ASYNCHRONOUS LIST POINTER	
0	
rw	

31 :0 Read: Currently executing (if ASST=01) or next transfer to be executed in asynchronous schedule.
Write: Change address. If running, this will cause a jump after the current transfer has finished.

32.8.8 BC Timer Register

*Table 378.*0x50 - BCT - GR1553B BC Timer register

31 24	23 0
RESERVED	SCHEDULE TIME (SCTM)
0	0
r	r

23 : 0 Elapsed “transfer list” time in microseconds (read-only)
Set to zero when schedule is stopped or on external sync.

Note: This register is an optional feature, see BC Status and Config Register, bit 30

32.8.9 BC Timer Wake-up Register

*Table 379.*0x54 - BCTW - GR1553B BC Timer Wake-up register

31	30 24	23 0
WKEN	RESERVED	WAKE-UP TIME (WKTM)
0	0	0
rw	r	rw

31 Wake-up timer enable (WKEN) - If set, an interrupt will be triggered when WKTM=SCTM

23 : 0 Wake-up time (WKTM).

Note: This register is an optional feature, see BC Status and Config Register, bit 29

32.8.10 BC Transfer-triggered IRQ Ring Position Register

*Table 380.*0x58 - BCRD - GR1553B BC Transfer-triggered IRQ ring position register

31	0
BC IRQ SOURCE POINTER RING POSITION	
0	
rw	

31 : 0 The current write pointer into the transfer-tirggered IRQ descriptor pointer ring.
Bits 1:0 are constant zero (4-byte aligned)
The ring wraps at the 64-byte boundary, so bits 31:6 are only changed by user

32.8.11 BC per-RT Bus Swap Register

*Table 381.*0x5C - BCBS - GR1553B BC per-RT Bus swap register

31	0
BC PER-RT BUS SWAP	
0	
rw	

31 : 0 The bus selection value will be logically exclusive-or:ed with the bit in this mask corresponding to the addressed RT (the receiving RT for RT-to-RT transfers). This register gets updated by the core if the STBUS descriptor bit is used.

For more information on how to use this feature, see section 32.4.3.

Note: This register is an optional feature, see BC Status and Config Register, bit 28

32.8.12 BC Transfer List Current Slot Pointer

*Table 382.*0x68 - BCTCP - GR1553B BC Transfer list current slot pointer

31	0
BC TRANSFER SLOT POINTER	
0	
r	

31 : 0 Points to the transfer descriptor corresponding to the current time slot (read-only, only valid while transfer list is running).

Bits 3:0 are constant zero (128-bit/16-byte aligned)

32.8.13 BC Asynchronous List Current Slot Pointer

*Table 383.*0x6C - BCACP - GR1553B BC Asynchronous list current slot pointer

31	0
BC TRANSFER SLOT POINTER	
0	
r	

31 : 0 Points to the transfer descriptor corresponding to the current asynchronous schedule time slot (read-only, only valid while asynchronous list is running).

Bits 3:0 are constant zero (128-bit/16-byte aligned)

32.8.14 RT Status Register

*Table 384.*0x80 - RTS - GR1553B RT Status register (read-only)

31	30	4	3	2	1	0
RTSUP	RESERVED		ACT	SHDA	SHDB	RUN

31 RT Supported (RTSUP) - Reads ‘1’ if core supports RT mode

3 RT Active (ACT) - ‘1’ if RT is currently processing a transfer

2 Bus A shutdown (SHDA) - Reads ‘1’ if bus A has been shut down by the BC (using the transmitter shutdown mode command on bus B)

1 Bus B shutdown (SHDB) - Reads ‘1’ if bus B has been shut down by the BC (using the transmitter shutdown mode command on bus A)

0 RT Running (RUN) - ‘1’ if the RT is listening to commands.

32.8.15 RT Config Register

*Table 385.*0x84 - RTC - GR1553B RT Config register

31 16	15	14	13	12 7	6	5 1	0
RTKEY	SYS	SYDS	BRS	RESERVED	RTEIS	RTADDR	RTEN
0	1	1	1	0	*	*	0
w	rw	rw	rw	r	r	rw	rw

31 : 16 Safety code (RTKEY) - Must be written as 0x1553 when changing the RT address, otherwise the address field is unaffected by the write. When reading the register, this field reads 0x0000.
If extra safety keys are enabled (see Hardware Config Register), the lower half of the key is used to also protect the other fields in this register.

15 Sync signal enable (SYS) - Set to '1' to pulse the rtsync output when a synchronize mode code (without data) has been received

14 Sync with data signal enable (SYDS) - Set to '1' to pulse the rtsync output when a synchronize with data word mode code has been received

13 Bus reset signal enable (BRS) - Set to '1' to pulse the busreset output when a reset remote terminal mode code has been received.

6 Reads '1' if current address was set through external inputs.
After setting the address from software this field is set to '0'

5 : 1 RT Address (RTADDR) - This RT:s address (0-30)

0 RT Enable (RTEN) - Set to '1' to enable listening for requests

32.8.16 RT Bus Status Register

*Table 386.*0x88 - RTBS - GR1553B RT Bus status register

31 9	8	7 5	4	3	2	1	0
RESERVED	TFDE	RESERVED	SREQ	BUSY	SSF	DBCA	TFLG
0	0	0	0	0	0	0	0
r	rw	rw	rw	rw	rw	rw	rw

8 Set Terminal flag automatically on DMA and descriptor table errors (TFDE)

4 : 0 These bits will be sent in the RT:s status responses over the 1553 bus.

4 Service request (SREQ)

3 Busy bit (BUSY)
Note: If the busy bit is set, the RT will respond with only the status word and the transfer "fails"

2 Subsystem Flag (SSF)

1 Dynamic Bus Control Acceptance (DBCA)
Note: This bit is only sent in response to the Dynamic Bus Control mode code

0 Terminal Flag (TFLG)
The BC can mask this flag using the "inhibit terminal flag" mode command, if legal

32.8.17 RT Status Words Register

*Table 387.*0x8C - RTSW - GR1553B RT Status words register

31 16	15 0
BIT WORD (BITW)	VECTOR WORD (VECW)
0	0
rw	rw

31 : 16 BIT Word - Transmitted in response to the "Transmit BIT Word" mode command, if legal

15 : 0 Vector word - Transmitted in response to the "Transmit vector word" mode command, if legal.

32.8.18 RT Sync Register

*Table 388.*0x90 - RTSY - GR1553B RT Sync register

31 16	15 0
SYNC TIME (SYTM)	SYNC DATA (SYD)
0	0
r	r

31 : 16 The value of the RT timer at the last sync or sync with data word mode command, if legal.

15 : 0 The data received with the last synchronize with data word mode command, if legal

32.8.19 Sub Address Table Base Address Register

*Table 389.*0x94 - RTSTBA - GR1553B RT Sub address table base address register

31 9	8 0
SUBADDRESS TABLE BASE (SATB)	RESERVED
0	0
rw	r

31 : 9 Base address, bits 31-9 for subaddress table

8 : 0 Always read ‘0’, writing has no effect

32.8.20 RT Mode Code Control Register

*Table 390.*0x98 - RTMCC - GR1553B RT Mode code control register

31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16
RESERVED	RRTB	RRT	ITFB	ITF	ISTB	IST	DBC
0	0	0	0	0	0	0	0
r	rw	rw	rw	rw	rw	rw	rw

15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
TBW	TVW	TSB	TS	SDB	SD	SB	S
0	0	1	1	1	1	1	1
rw	rw	rw	rw	rw	rw	rw	rw

For each mode code: “00” - Illegal, “01” - Legal, “10” - Legal, log enabled, “11” - Legal, log and interrupt

29 : 28 Reset remote terminal broadcast (RRTB)

27 : 26 Reset remote terminal (RRT)

25 : 24 Inhibit & override inhibit terminal flag bit broadcast (ITFB)

23 : 22 Inhibit & override inhibit terminal flag (ITF)

21 : 20 Initiate self test broadcast (ISTB)

19 : 18 Initiate self test (IST)

17 : 16 Dynamic bus control (DBC)

15 : 14 Transmit BIT word (TBW)

13 : 12 Transmit vector word (TVW)

11 : 10 Transmitter shutdown & override transmitter shutdown broadcast (TSB)

9 : 8 Transmitter shutdown & override transmitter shutdown (TS)

7 : 6 Synchronize with data word broadcast (SDB)

5 : 4 Synchronize with data word (SD)

3 : 2 Synchronize broadcast (SB)

1 : 0 Synchronize (S)

32.8.21 RT Time Tag Control Register

*Table 391.*0xA4 - RTTTC - GR1553B RT Time tag control register

31 16	15 0
TIME RESOLUTION (TRES)	TIME TAG VALUE (TVAL)
0	0
rw	rw

31 : 16 Time tag resolution (TRES) - Time unit of RT:s time tag counter in microseconds, minus 1

15 : 0 Time tag value (TVAL) - Current value of running time tag counter

32.8.22 RT Event Log Mask Register

*Table 392.*0xAC - RTELM - GR1553B RT Event Log mask register

31 21	16 2	1 0
RESERVED	EVENT LOG SIZE MASK	RES
	0xFFFFFFC	
r	rw	r

31 : 0 Mask determining size and alignment of the RT event log ring buffer. All bits “above” the size should be set to ‘1’, all bits below should be set to ‘0’

32.8.23 RT Event Log Position Register

*Table 393.*0xB0 - RTELP - GR1553B RT Event Log position register

31 0
EVENT LOG WRITE POINTER
0
rw

31 : 0 Address to first unused/oldest entry of event log buffer, 32-bit aligned

32.8.24 RT Event Log Interrupt Position Register

*Table 394.*0xB4 - RTELIP - GR1553B RT Event Log interrupt position register

31 0
EVENT LOG IRQ POINTER
0
r

31 : 0 Address to event log entry corresponding to interrupt, 32-bit aligned
The register is set for the first interrupt and not set again until the interrupt has been acknowledged.

32.8.25 BM Status Register

*Table 395.*0xC0 - BMS - GR1553B BM Status register

31	30	29 0
BMSUP	KEYEN	RESERVED
*	*	0
r	r	r

31 BM Supported (BMSUP) - Reads ‘1’ if BM support is in the core.

30 Key Enabled (KEYEN) - Reads ‘1’ if the BM validates the BMKEY field when the control register is written.

32.8.26 BM Control Register

*Table 396.*0xC4 - BMC - GR1553B BM Control register

31 16	15 6	5	4	3	2	1	0
BMKEY	RESERVED	WRSTP	EXST	IMCL	UDWL	MANL	BMEN
0	0	0	0	0	0	0	0
rw	r	rw	rw	rw	rw	rw	rw

31 : 16	Safety key - If extra safety keys are enabled (see KEYEN), this field must be 0x1543 for a write to be accepted. Is 0x0000 when read.
5	Wrap stop (WRSTP) - If set to ‘1’, BMEN will be set to ‘0’ and stop the BM when the BM log position wraps around from buffer end to buffer start
4	External sync start (EXST) - If set to ‘1’,BMEN will be set to ‘1’ and the BM is started when an external BC sync pulse is received
3	Invalid mode code log (IMCL) - Set to ‘1’ to log invalid or reserved mode codes.
2	Unexpected data word logging (UDWL) - Set to ‘1’ to log data words not seeming to be part of any command
1	Manchester/parity error logging (MANL) - Set to ‘1’ to log bit decoding errors
0	BM Enable (BMEN) - Must be set to ‘1’ to enable any BM logging

32.8.27 BMRT Address Filter Register

*Table 397.*0xC8 - BMRTAF - GR1553B BM RT Address filter register

31 0
ADDRESS FILTER MASK
0xFFFFFFFF
rw

31	Enables logging of broadcast transfers
30 : 0	Each bit position set to ‘1’ enables logging of transfers with the corresponding RT address

32.8.28 BMRT Sub address Filter Register

*Table 398.*0xCC - BMRTSF - GR1553B BM RT Sub address filter register

31 0
SUBADDRESS FILTER MASK
0xFFFFFFFF
rw

31	Enables logging of mode commands on sub address 31
30 : 1	Each bit position set to ‘1’ enables logging of transfers with the corresponding RT sub address
0	Enables logging of mode commands on sub address 0

32.8.29 BMRT Mode Code Filter Register

*Table 399.*0xCC - BMRTMC - GR1553B BM RT Mode code filter register

31	19	18	17	16
RESERVED		STSB	STS	TLC
0x1ttt		1	1	1
r		rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSW	RRTB	RRT	ITFB	ITF	ISTB	IST	DBC	TBW	TVW	TSB	TS	SDB	SD	SB	S
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Each bit set to '1' enables logging of a mode code:

- 18 Selected transmitter shutdown broadcast & override selected transmitter shutdown broadcast (STSB)
- 17 Selected transmitter shutdown & override selected transmitter shutdown (STS)
- 16 Transmit last command (TLC)
- 15 Transmit status word (TSW)
- 14 Reset remote terminal broadcast (RRTB)
- 13 Reset remote terminal (RRT)
- 12 Inhibit & override inhibit terminal flag bit broadcast (ITFB)
- 11 Inhibit & override inhibit terminal flag (ITF)
- 10 Initiate self test broadcast (ISTB)
- 9 Initiate self test (IST)
- 8 Dynamic bus control (DBC)
- 7 Transmit BIT word (TBW)
- 6 Transmit vector word (TVW)
- 5 Transmitter shutdown & override transmitter shutdown broadcast (TSB)
- 4 Transmitter shutdown & override transmitter shutdown (TS)
- 3 Synchronize with data word broadcast (SDB)
- 2 Synchronize with data word (SD)
- 1 Synchronize broadcast (SB)
- 0 Synchronize (S)

32.8.30 BMLog Buffer Start

*Table 400.*0xD4 - BMLBS - GR1553B BM Log buffer start

31	0
BM LOG BUFFER START	
0	
rw	

31 : 0 Pointer to the lowest address of the BM log buffer (8-byte aligned)
Due to alignment, bits 2:0 are always 0.

32.8.31 BMLog Buffer End

*Table 401.*0xD8 - BMLBE - GR1553B BM Log buffer end

31 22	21 3	2 0
-	BM LOG BUFFER END	-
	0x0000007	
r	rw	r

31 : 0 Pointer to the highest address of the BM log buffer
Only bits 21:3 are settable, i.e. the buffer can not cross a 4 MB boundary Bits 31:22 read the same as the buffer start address.Due to alignment, bits 2:0 are always equal to 1

32.8.32 BMLog Buffer Position

*Table 402.*0xDC - BMLBP - GR1553B BM Log buffer position

31 22	21 3	2 0
-	BM LOG BUFFER POSITION	-
	0x00000000	
r	rw	r

31 : 0	Pointer to the next position that will be written to in the BM log buffer Only bits 21:3 are settable, i.e. the buffer can not cross a 4 MB boundary Bits 31:22 read the same as the buffer start address.Due to alignment, bits 2:0 are always equal to 0

32.8.33 BM Time Tag Control Register

*Table 403.*0xE0 - BMTTC - GR1553B BM Time tag control register

31 24	23 0
TIME TAG RESOLUTION	TIME TAG VALUE
0	0
rw	rw

31 : 24	Time tag resolution (TRES) - Time unit of BM:s time tag counter in microseconds, minus 1
23 : 0	Time tag value (TVAL) - Current value of running time tag counter

32.9 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x04D. For a description of vendor and device identifiers see GRLIB IP Library User's Manual.

32.10 Implementation

32.10.1 Reset

The core does not changs reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core has two separate reset inputs for the two clock domains. They should be reset simultaneously, for instance by using two Reset generator cores connected to the same reset input but clocked by the respective clocks See the documentation of the *syncrst* VHDL generic for possible reset implementations.

32.11 Configuration options

Table 404 shows the configuration options of the core (VHDL generics).

*Table 404.*Configuration options

Generic	Function	Allowed range	Default
hindex	AHB master index	0 - NAHBMST-1	0
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	ADDR field of the APB BAR.	0 - 16#FFF#	0
pmask	MASK field of the APB BAR.	0 - 16#FFF#	16#FFF#
pirq	Index of the interrupt line.	0 - NAHBIRQ-1	0
bc_enable	Selects whether BC support is built into the core	0 - 1	1
rt_enable	Selects whether RT support is built into the core	0 - 1	1
bm_enable	Selects whether BM support is built into the core	0 - 1	1
bc_timer	Selects whether the BC timer and wake-up interrupt features are built into the core. 0=None, 1=Timer, 2=Timer and wake-up	0-2	1
bc_rtbusmask	Selects whether the BC per-RT bus swap register is built into the core.	0-1	1
extra_regkeys	Enables extra safety keys for the BM control register and for all fields in the RT control registers	0-1	0
syncrst	Selects reset configuration: 0: Asynchronous reset, all registers in core are reset 1: Synchronous, minimal set of registers are reset 2: Synchronous, most registers reset (increases area slightly to simplify netlist simulation)	0-2	1
ahbendian	Selects AHB bus endianness (for use in non-GRLIB systems), 0=Big endian, 1=Little endian	0 - 1	0
bm_filters	Enable BM filtering capability	0 - 1	1
codecfreq	Codec clock domain frequency in MHz	20 or 24	20
sameclk	AMBA clock and reset is same as codec (removes internal synchronization)	0 - 1	0

32.12 Signal descriptions

Tables 405-406 shows the interface signals of the core (VHDL ports).

*Table 405.*Signal descriptions on AMBA side

Signal name	Field	Type	Function	Active
CLK	N/A	Input	Clock, AMBA clock domain	-
RST	N/A	Input	Reset for registers in CLK clock domain	Low
AHBMI	*	Input	AHB master input signals	-
AHBMO	*	Output	AHB master output signals	-
APBSI	*	Input	APB slave input signals	-
APBSO	*	Output	APB slave output signals	-
AUXIN	EXTSYNC	Input	External sync input for Bus Controller Re-synchronized to AMBA clk internally. Edge-detection checks for the sampled pattern "01", i.e. pulses should be at least one CLK cycle to always get detected.	Pos. edge
	RTADDR	Input	Reset value for RT address, if parity matches.	-
	RTPAR	Input	RT address odd parity	-
AUXOUT	RTSYNC	Output	Pulsed for one CLK cycle after receiving a synchronize mode command in RT mode	High
	BUSRESET	Output	Pulsed for one CLK cycle after receiving a reset remote terminal mode command in RT mode	High
	VALIDCMDA	Output	Pulsed for one CLK cycle after receiving a valid command word on bus A/B in RT mode	High
	VALIDCMDB	Output		High
	TIMEDOUTA	Output	Asserted when the terminal fail-safe timer has triggered on bus A/B.	High
	TIMEDOUTB	Output		High
	BADREG	Output	Pulsed for one CLK cycle when an invalid register access is performed, either: - an access to an undefined register, - read/write from a write-only/read-only register, - a read/write to a non-implemented part of the core - an incorrect BCKEY/BMKEY	High
	IRQVEC	Output	Auxiliary IRQ vector. Pulsed at the same time as the ordinary PIRQ line, but with a separate line for each interrupt: 7: BM Timer overflow, 6: BM DMA Error, 5: RT Table error, 4: RT DMA Error, 3: RT Event 2: BC Wake-up, 1: BC DMA Error, 0: BC Event	High

* see GRLIB IP Library User's Manual

*Table 406.*Signal descriptions on 1553 side

Signal name	Field	Type	Function	Active
CODEC_CLK	N/A	Input	Codec clock	-
CODEC_RST	N/A	Input	Reset for registers in CODEC_CLK domain	Low
TXOUT	BUSA_TXP	Output	Bus A transmitter, positive output	High **
	BUSA_TXN	Output	Bus A transmitter, negative output	High **
	BUSA_TXEN	Output	Bus A transmitter enable	High
	BUSA_RXEN	Output	Bus A receiver enable	High
	BUSB_TXP	Output	Bus B transmitter, positive output	High **
	BUSB_TXN	Output	Bus B transmitter, negative output	High **
	BUSB_TXEN	Output	Bus B transmitter enable	High
	BUSB_RXEN	Output	Bus B receiver enable	High
	BUSA_TXIN	Output	Inverted version of BUSA_TXEN (for VHDL coding convenience)	High
	BUSB_TXIN	Output	Inverted version of BUSB_TXEN	High
TXOUT_FB	See TXOUT	Input	Feedback input to the terminal fail-safe timers. Should be tied directly to TXOUT, but are exposed to allow testing the fail-safe timer function. This input is re synchronized to CODEC_CLK so it can be asynchronous.	See TXOUT
RXIN	BUSA_RXP	Input	Bus A receiver, positive input	High **
	BUSA_RXN	Input	Bus A receiver, negative input	High **
	BUSB_RXP	Input	Bus B receiver, positive input	High **
	BUSB_RXN	Input	Bus B receiver, negative input	High **

** The core will put both P/N outputs low when not transmitting. For input, it accepts either both-low or both-high idle.

32.13 Signal definitions and reset values

The signals and their reset values are described in table 407.

*Table 407.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
busa_rxen	Output	Enable for the A receiver	High	Logical 0
busa_rxp	Input	Positive data input from the A receiver	High*	-
busa_rxn	Input	Negative data input from the A receiver	High*	-
busa_txinh	Output	Enable for the A transmitter	Low**	Logical 1
busa_txp	Output	Positive data to the A transmitter	High	Logical 0
busa_txn	Output	Negative data to the A transmitter	High	Logical 0
busb_rxen	Output	Enable for the B receiver	High	Logical 0
busb_rxp	Input	Positive data input from the B receiver	High*	-
busb_rxn	Input	Negative data input from the B receiver	High*	-
busb_txinh	Output	Enable for the B transmitter	Low**	Logical 1
busb_txp	Output	Positive data to the B transmitter	High	Logical 0
busb_txn	Output	Negative data to the B transmitter	High	Logical 0

* rx inputs can be either both-high or both-low when bus is idle

** txinh inhibits (disables) transmission when high, enables transmission when low

32.14 Timing

The timing waveforms and timing parameters are shown in figure 114 and are defined in table 408.

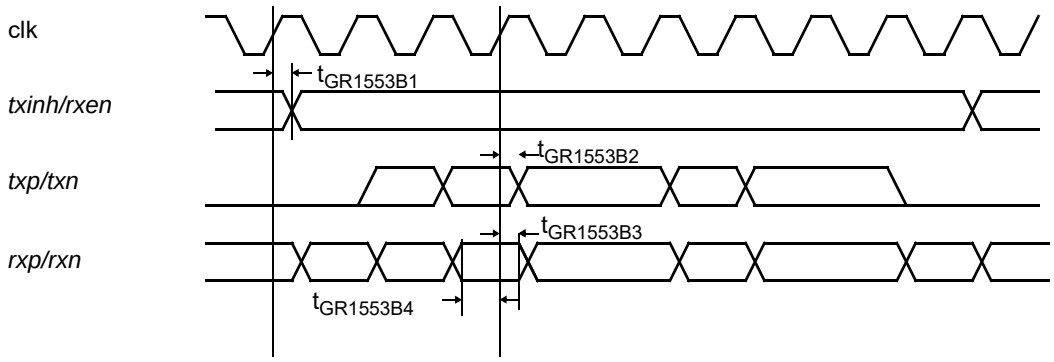


Figure 114. Timing waveforms

*Table 408.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{GR1553B1}$	clock to output delay, control signals	rising *clk* edge	-	TBD	ns
$t_{GR1553B2}$	clock to output delay, transmit data	rising clk edge	TBD	TBD	ns
$t_{GR1553B3}$	data input to clock setup	rising *clk* edge	TBD *	-	ns
$t_{GR1553B4}$	data input from clock hold	rising *clk* edge	TBD *	-	ns

* The rx input signals are re-synchronized to clk internally

32.15 Library dependencies

Table 409 shows libraries used when instantiating the core (VHDL libraries).

*Table 409.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AHB/APB signal definitions
GAISLER	GR1553B_PKG	Signals, component	signal and component declaration

32.16 Instantiation

This example shows how the core can be instantiated in a GRLIB design.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib, gaisler;
use grlib.amba.all;
use gaisler.gr1553b_pkg.all;
use gaisler.misc.rstgen;

entity gr1553b_ex is
  generic (
    padtech     : integer
    );
  port (
    rstn        : in std_ulogic;
    clk         : in std_ulogic;
    codec_clk   : in std_ulogic;
```

```
    -- MIL-STD-1553 signals
    txAen       : out std_ulogic;
    txAP        : out std_ulogic;
    txAN        : out std_ulogic;
    rxAen       : out std_ulogic;
    rxAP        : in std_ulogic;
    rxAN        : in std_ulogic;
    txAen       : out std_ulogic;
    txAP        : out std_ulogic;
    txAN        : out std_ulogic;
    rxAen       : out std_ulogic;
    rxAP        : in std_ulogic;
    rxAN        : in std_ulogic
    );
end;

architecture rtl of gr1553b_ex is

  -- System-wide synchronous reset
  signal rst       : std_logic;

  -- AMBA signals
  signal apbi      : apb_slv_in_type;
  signal apbo      : apb_slv_out_vector := (others => apb_none);
  signal ahbi      : ahb_mst_in_type;
  signal ahbo      : ahb_mst_out_vector := (others => apb_none);

  -- GR1553B signals
  signal codec_rst : std_ulogic;
  signal txout     : gr1553b_txout_type;
  signal rxin      : gr1553b_rxin_type;
  signal auxin     : gr1553b_auxin_type;
  signal auxout    : gr1553b_auxout_type;

begin

  rg0: rstgen port map (rstn, clk, '1', rst, open);

  -- AMBA Components are instantiated here
  ...

  -- Reset generation for 1553 codec
  rgc: rstgen port map (rstn, codec_clk, '1', codec_rst, open);

  -- GR1553B

  gr1553b0: gr1553b
  generic map (hindex => 4, pindex => 7, paddr => 7, pirq => 13, syncrst => 1,
               bc_enable => 1, rt_enable => 1, bm_enable => 1)
  port map (clk, rst, ahbi, ahbo(4), apbi, apbo(7), auxin, auxout,
            codec_clk, codec_rst, txout, txout, rxin);

  p: gr1553b_pads
  generic map (padtech => padtech, outen_pol => 0)
  port map (txout,rxin,
            rxAen,rxAP,rxAN,txAen,txAP,txAN,
            rxBen,rxBP,rxBN,txBen,txBP,txBN);

  auxin         <= gr1553b_auxin_zero;

end;
```

32.17 Constraints

This section contains example constraints for GR1553B.

0. Define a clock called 'mil_clk'

1. milclkperiod = 1553B Maximum clock frequency

2. tech_lib_setup = Setup timing for FlipFlop used in technology

3. tech_lib_hold = Hold timing for FlipFlop used in technology

```
set_input_delay -clock [get_clocks mil_clk] -min [expr $tech_lib_hold] [get_ports
$mil_inputs]
set_input_delay -clock [get_clocks mil_clk] -max [expr $milclkperiod/2 - $tech_lib_setup]
[get_ports $mil_inputs] -add_delay
set_output_delay -clock [get_clocks mil_clk] -max [expr $milclkperiod/2 + $tech_lib_setup]
[get_ports $mil_outputs] -add_delay
set_output_delay -clock [get_clocks mil_clk] -min [expr -1 * $tech_lib_hold]
[get_ports $mil_outputs] -add_delay
```

32.18 Note: AHB Interface Compatibility

32.18.1 Introduction

When using the GR1553B core in a non-GRLIB environment, the AHB system designer must make sure that the slaves to be accessed by the core are compatible with the accesses the master makes.

32.18.2 Generic access patterns

The GR1553B core performs the following accesses on the AHB bus:

- 32-bit sequential read burst, unspecified length, Length 2-3, 128-bit aligned start address. (BC,RT)
- 32-bit sequential write burst, length 2 (BM)
- Single 32-bit read/write (BC,RT)
- Single 16-bit write (BC,RT)
- Idle transfers

The master supports wait states (hready low) as well as split and retry responses. In either case, it will retry accesses indefinitely until getting an OKAY or ERROR response.

Busy cycles and locked transfers are not used by the core.

32.18.3 Endianness

The GR1553B core, in its standard configuration, only works on big-endian systems. Byte-swapping in software is not enough because of the 16-bit writes.

Little-endian bus support can be configured by setting the ahbendian generic to 1. The endian-ness setting only changes the handling of data buffers, data structures are still read using 32-bit reads/ writes and bit fields extracted from the same bit positions.

For data buffers, the core is designed to make 16-bit addressing correct, so that each 16-bit data word in memory is transferred msb to lsb in increasing address order. Note that with little-endian addressing this means that the data will not be sent in byte order. This means that care must be taken to ensure correct ordering when transferring data from 1553 buffers to/from byte streams (files, network packets, etc.).

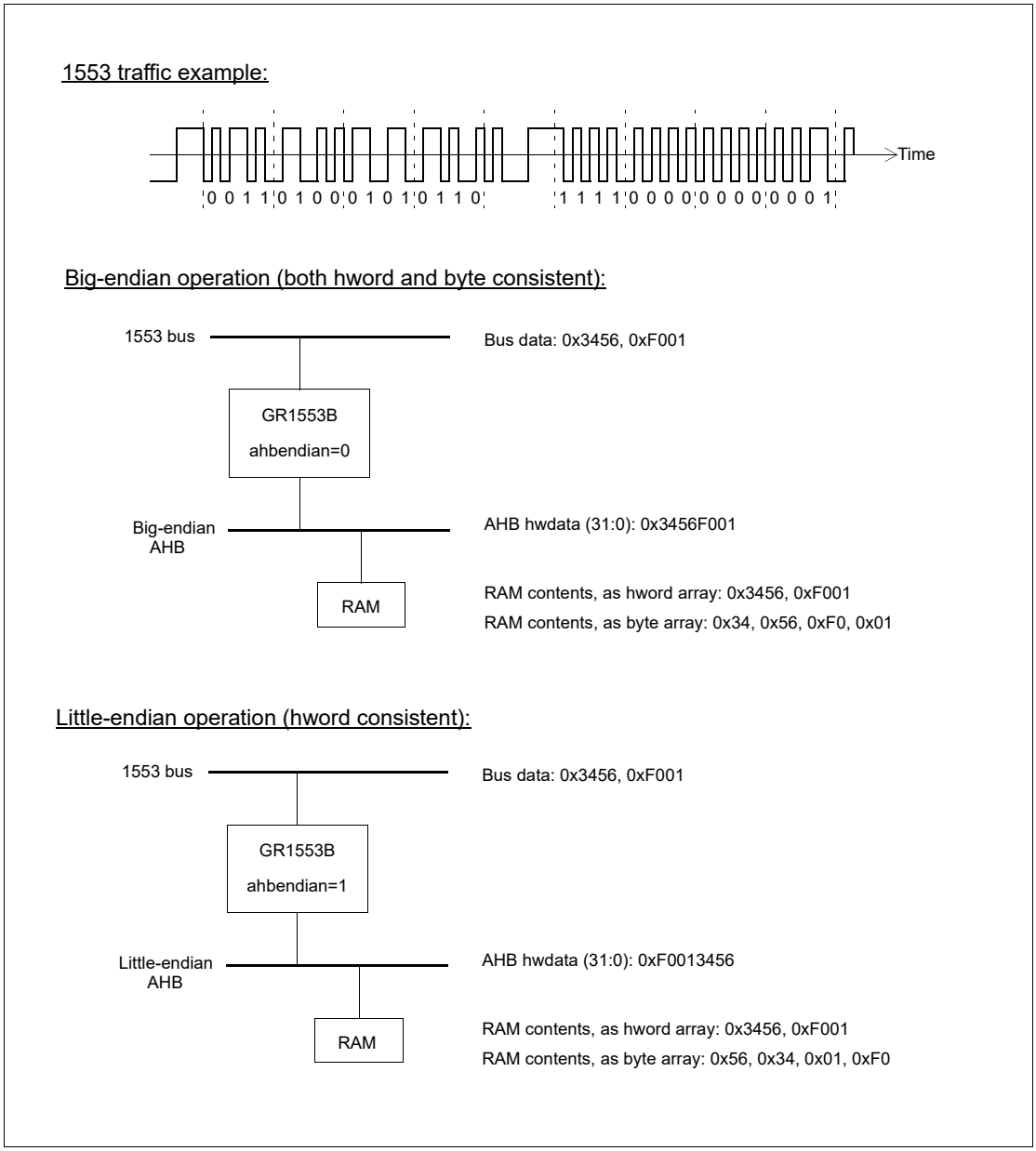


Figure 115. Relation between transferred 1553 data order and RAM contents for little/big-

32.19 Note: AHB Latency and throughput requirements

32.19.1 Introduction

Since the AMBA AHB bus standard does not in itself guarantee any maximum latency or throughput, the AHB bus system must be carefully designed so that the core can satisfy the 1553 requirements reliably.

Throughput is not normally a problem, since even at the lowest supported AMBA frequency of 10 MHz, the core can only use a few percent of the bus bandwidth.

Latency is a larger concern, especially when there are other bus masters with high bandwidth utilization or large burst access patterns.

Some general recommendations:

- Make GR1553B the highest priority master on the bus
- Limit the maximum length of other master's bursts to the order of 5 us.
- Use local RAM for descriptors and preferably also data.

32.19.2 BC Descriptor processing

Between transfers, the BC core first writes the descriptor status word using a 32-bit write, then fetches the following descriptor using a 3 x 32-bit read burst.

If the next location in the schedule is a branch, then the burst fetches only the first two 32-bit words, then processes the condition for one cycle, and then continues.

The core keeps the bus request signal high continuously until the next descriptor has been read. Between the status write and the descriptor read, there is one idle AHB transaction, i.e. the descriptor read is started the cycle after the status write finishes. Between a branch read and the next descriptor read, there are two idle AHB transactions, i.e. one completely idle cycle between the end of branch read and the start of descriptor read.

32.19.3 BC Asynchronous scheduling

If the asynchronous list is started and there is slack in the regular schedule, the BC needs to read the next asynchronous descriptor in order to make the scheduling decision. In case there is less slack than was specified in the asynchronous descriptor, the BC will then read the regular descriptor and proceed with the regular schedule. In this case, the BC remembers the asynchronous time requirement and will not need to re-read the asynchronous descriptor until the asynchronous transfer is actually scheduled.

If there is less than 24 us of slack in the regular schedule, then the BC will assume there is no time for the asynchronous transfer, not read the asynchronous descriptor and just proceed with the regular schedule. This means that as long as two BC descriptors can be read within 24 us, the asynchronous descriptor processing can not affect the ordinary schedule.

32.19.4 BC Data Buffer processing

When transferring data from BC-to-RT, the core reads the first one or two (depending on alignment) 16-bit data words from memory using a 32-bit read, while the command word is being transferred. The core then reads an additional 32-bit word every time the last previously read data word is sent and there is more to send.

For transfers from RT-to-BC, the core either writes the first data word using a 16-bit write, or writes the first two data words using a 32-bit write, depending on data buffer alignment. It will then perform a 32-bit write after every two data words received. While performing the write, the core does not buffer another data word so the write has to complete within 20 us.

If there is one received data word left after the transfer, it is written during the 5 us message gap. If it doesn't finish in that time, the descriptor processing will be delayed until after the write finishes.

32.19.5 BC Requirements

The hard requirement on the BC comes from the data buffers, where one read/write should finish in 20 us.

The time needed for descriptor processing will affect the schedule. In order to reduce this time, the time for a 32-bit write followed by a 3x32-bit read burst should be reduced, preferably to the 2-3 us range. This is more of a soft requirement, and for larger schedules it can often be viewed as an average over minor frames or other groups of transfers.

If the asynchronous scheduling feature is used, and you do not want the regular schedule to be affected by this, two 3x32-bit read bursts must be able to finish within 24 us.

32.19.6 RT Transfer Processing

For the RT there are two cases to consider, receive and transmit.

The receive case:

1. The RT gets the receive command
2. While the first data word is transmitted over the bus, the RT looks up the subaddress table and receive descriptor.
3. The data words are stored
4. The RT waits 5-6 us to see that there are no extra (unwanted) data words.
5. The status word is transmitted. In parallel, the results are written to the descriptor and the log and table is updated.

The transmit case:

1. The RT gets the transmit command
2. In parallel there are two processes working:
    - Process A:
        - A.1 The RT looks up in the subaddress table that the request is legal.
        - A.2 The RT looks up the descriptor and reads the first word of data
    - Process B:
        - B.1 The RT waits 5-6 us to see that there are no extra (unwanted) data words received.
        - B.2 Wait for A.1 to finish
        - B.3 Send status word
        - B.4 Send data
3. The data words are sent
4. The results are written to the descriptor and the log and table is updated.

In the receive case, the subaddress table and descriptor reads (two 3x32-bit read bursts) have to finish within the 20 us period that the data word is transferred.

In the transmit case, the subaddress table read (one 2x32-bit read burst) has to finish in time so that the RT satisfies the response time requirement.

The RT has a status word response time requirement of 12 us mid-bit to mid-sync, which translates into in 10 us maximum bus dead time before responding. These 10 us also include transceiver delays, so the actual time available is typically closer to 9 us.

The core has a safety limit of 9 us, after which a table error interrupt is generated and no response is generated. However, this should be seen as a fallback solution and triggering this time-out should be considered a fault at the AMBA bus design level.

32.19.7 RT Requirements

From the cases above, the following requirements can be derived:

One 2x32-bit read burst must finish in 8.5-9 us (from the transmit case above)

Two 3x32-bit read bursts plus one 32-bit read must finish in 20 us.

Each 32-bit data buffer read/write must finish in 20 us.

32.19.8 Bus Monitor

The bus monitor will at full bus traffic, write 2x32-bit data words every 20 us.

If run in parallel with the BC or RT, this will need to be added to the requirements. The core is designed so that, after an RT+BM receives a command word, the RT will access the bus first to do the more urgent accesses.

32.20 Note: BC transfer timing

32.20.1 Introduction

In order to design a transfer schedule for the Bus Controller, the worst-case times for each transfer must be calculated. This note is intended to give some hints on how to do this. Understanding of the 1553B protocol is assumed, see the AS15531 standard (in particular, Figure 9) for details.

32.20.2 Overview

Except for the case of automatic retries, the longest time a transfer takes is the success case, where all permitted time-outs and slack is used.

When reading the standard, there are a few points to note for the calculations:

- The time-outs and gaps in the standard are specified mid-parity to mid-sync. To convert into bus dead time, one must subtract 2 us.
- The timings are specified on the bus side, so transceiver delays must be taken into account.

32.20.3 Transceiver delay

The timings in the 1553 standard are specified on the terminal boundary which is on the bus side of the transceiver. However, the core operates on the other side of the transceiver. Therefore, the transceiver delays must be taken into account.

The BC mode uses the loopback checking mechanism to compensate for transceiver delay. After the command words have been sent, it waits for the words to loop back through the receiver and then starts the RT time-out timer.

32.20.4 BC Transfer Steps: Parts

A BC transfer can be divided into the following steps:

1. Transmission of control words and receive data

This is a continuous transmission which takes 20 us per word sent. Also include 0.2 us starting delay.

2. Transceiver turnaround

The core waits for the transmitted command to loop back into the receiver. By doing this before starting the RT time-out clock, we get an accurate RT timeout regardless of transceiver delay.

The time this takes is the sum of the transmitter and receiver delay, plus internal decoding delays of 0.15-0.40 us.

3. RT Response Time-out

The core allows a maximum of 12.0-12.5 us bus dead time before the beginning of the RT Response. Note that this time can be increased via a descriptor setting.

4. RT Response and transmit data

The BC receives the RT status word and the specified number of data words.

The Bus Controller checks for message continuity and allows a maximum of 1 us of sync drift over the entire message. The maximum time for this part is thus 20 us/word + 1 us.

5. Second RT Response Time-out

For RT-to-RT transfers. See step 3.

6. Second RT Response

For RT-to-RT transfers. See step 4.

7. Word count verification

For non-broadcast and RT-to-RT messages, the BC waits an additional 5 us to ensure that there is no additional word sent out by the last transmitting RT.

8. Store result, fetch next descriptor

The time this takes to perform depends completely on the AMBA system the core is connected to.

9. Broadcast message gap and descriptor processing

For single-RT broadcasts, instead of step 7-8 the core inserts a 3 us message gap, and in parallel starts fetching the next descriptor. This step therefore takes the maximum of 3 us and the time needed for step 8.

32.20.5 BC transfer steps: Composition

The different 1553 message types map to the above steps as:

BC-to-RT, RT-to-BC, Mode: Steps 1-4,7-8

RT-to-RT: Steps 1-8

BC-to-RT broadcast, Mode broadcast: Steps 1,2,9

RT-to-RT broadcast: Steps 1-4,7-8

If broadcast response checking is enabled in the BC status register, the core waits and checks that no RT produces a response on the bus after each broadcast. Thus, the broadcast case changes to 1-4,7-8, and 30-35 us is added to the worst-case transfer time.

32.20.6 Timing calculation

Based on the steps above, and also taking automatic replies into account, we end up with the following calculations:

BC-to-RT, RT-to-BC or Mode, N data words:

$T = C_{try} \times (20.2 + Nx20 + T_{loop} + 12.5 + T_{extra} + 21 + 5) + T_{dpr}$
$= C_{try} \times (58.7 + Nx20 + T_{extra} + T_{loop}) + T_{dpr}$

RT-to-RT, N data words:

$T = C_{try} \times (40.2 + T_{loop} + 12.5 + T_{extra} + 21 + Nx20 + 12.5 + T_{extra} + 21 + 5) + T_{dpr}$
$= C_{try} \times (112.2 + Nx20 + 2T_{extra} + T_{loop}) + T_{dpr}$

BC-to-RT broadcast or Mode broadcast, N data words:

$T = Ctry \times (20.2 + Nx20 + T_{loop} + 3) - 3 + \max(T_{dpr},3)$

RT-to-RT broadcast:

$T = Ctry \times (40.2 + T_{loop} + 12.5 + T_{extra} + 21 + Nx20 + 5) + T_{dpr}$

Where:

T Worst-case time usage for transfer (i.e. how much the following transfer is delayed when running at maximum rate)

C_{try} The maximum number of attempts, controlled by descriptor, equal to 1 unless automatic retries are used.

T_{loop} Time from the end of a word transmission to receiver decoding the looped-back word. Sum of transceiver transmit and receive delay, plus internal delay of 400 ns.

T_{dpr} Time needed for data processing between this and the next transfer. This includes storing result, processing any branches, and fetching the next descriptor

T_{extra} Extra RT response time, equal to the RTTO field in the transfer descriptor multiplied by 4 us.

32.20.7 Example

Assume for this example that T_{loop} = 1.4 us (transceiver delay of 500 ns + 500 ns) and T_{dpr} = 3 us (90 cycles at 30 MHz).

An RT-to-RT transfer of 5 data words then needs up to 1 x (112.2 + 5x20 + 2x0 + 1.4) + 3 = 216.6 us of time to execute.

32.21 Note: Time synchronization

32.21.1 Introduction

The purpose of time synchronization is to get a common notion of time between the terminals on the bus. This allows the user to relate time stamps from different terminals and coordinate events. If there is an external time base available on one of the terminals it is also interesting to be able to translate the time stamps over into this time base.

This note describes the GR1553B IP core's BC-to-RT time synchronization capabilities and discusses some applications.

32.21.2 Hardware features: BC features

The BC supports sending the 1553 bus standard's two mode commands dedicated to synchronization, synchronize (code 1) and synchronize with data word (code 17). The commands can be sent either to a specific RT, or sent on the broadcast address to all RT:s on one bus.

With the "wait for external trigger" (WTRIG) descriptor bit, any data transfer or mode code in the schedule can be set up to wait for a positive edge on the IP core's auxin.extsync input signal before starting. The external sync can also be triggered from software by writing to the BC Action Register.

It is also possible to use the regular scheduling features of the core to plan synchronization commands within a frame with high precision, just like any other transfer can be planned. This makes it possible to send timed sync pulses at a different interval than the external sync pulses, or to use the internal BC timer as time master with no external time base at all.

32.21.3 Hardware features: RT features

The RT supports receiving the two synchronization mode commands that can be emitted by the BC. In case of synchronization with data word, the attached data word can be read out through the RT sync register.

The RT has an internal timer with configurable scaler, which can be read-out and configured through the RT Time tag control register. When a mode command is received, the timer value is stored into the RT Sync Register which can be read out by software.

There are also a number of core output signals related to synchronization. The validcmdA/B outputs are raised whenever a valid command word is received in the RT, and this happens at the same time as the internal time stamp is taken. There is also an output called rtsync which is set high only after a successfully received sync command. The rtsync output pulse always occurs after the validcmd pulse.

If software handling of synchronization is desired, the core can be configured to generate an IRQ after a sync mode command has been received.

32.21.4 Hardware features: Internal timers

Both the internal timer used for BC scheduling and the timer used for the RT time stamps are based on 1 MHz clock ticks generated in the codec clock domain that are resynchronized to the AMBA clock domain. When the RT timer register is written, the tick generator and the (optional) scaler gets reset, therefore for best timestamp accuracy, the RT timer should be left free-running and used as differential measurements.

In terms of frequency accuracy, the internal timers will have the same characteristics as the codec clock, which is limited by the 1553 standard to 1000 ppm long-term. If the user has a more accurate clock source than this, this will naturally translate into more accurate timing.

32.21.5 Synchronization schemes

32.21.6 Synchronization schemes: Overview

This section describes a few ways to generate and receive synchronization commands on the bus. There are many possible ways to do this, but in this section the basic scheme assumed is by broadcasting sync mode commands from the BC at a regular interval. To handle fault conditions, the sync commands are sent on alternating buses.

Typically the user also wants to send a frame number or a coarse time stamp with the sync command. This can be sent either as the attached data word when using the sync with data mode command, or it can be sent beforehand to a dedicated subaddress on the RT:s. This is not described further in the section.

32.21.7 Synchronization schemes: BC without external time base

If no external real time base is available on the BC, regular sync commands can still be generated by scheduling as shown in the example below.

*Table 410.*Example BC descriptor structure with synchronization

	Sum of slot times assigned in each frame = sync period/2				
Frame 1	Sync broadcast Bus A	Transfer	Transfer	...	Jump to frame 2
Frame 2	Sync broadcast Bus B	Transfer	Transfer	...	Jump to frame 3
Frame 3	Sync broadcast Bus A	Transfer	Transfer	...	Jump to frame 4
Frame 4	Sync broadcast Bus B	Transfer	Transfer	...	Jump to frame 1

32.21.8 Synchronization schemes: BC with external time base

If there is an external time base connected to the extsync input of the core, this can be used by setting the wait for external trigger descriptor bit at intervals in the schedule corresponding to the sync interval. The schedule can otherwise be kept as is. As the figure shows it is possible to have the sync pulses at a multiple of the sync interval and use the internal time base for the sync commands in between.

*Table 411.*Example BC descriptor structure with external synchronization

	Sum of slot times assigned in each frame = sync period/2					
Frame 1	Sync broadcast Bus A, wtrig set	Transfer	Transfer	...	Jump to frame 2	Sum of slot times in all four frames gives external sync period
Frame 2	Sync broadcast Bus B	Transfer	Transfer	...	Jump to frame 3	
Frame 3	Sync broadcast Bus A	Transfer	Transfer	...	Jump to frame 4	
Frame 4	Sync broadcast Bus B	Transfer	Transfer	...	Jump to frame 1	

32.21.9 Synchronization schemes: RT without external time base

If the resolution of the sync period from the BC is good enough, then the simplest solution is to just take the frame number sent by the BC directly and use it as the time stamp.

If more resolution is needed, the user can read out the current value of the RT Timer, compare with the last sync time stamp in the RT Sync register, and use the difference as a time offset from the last sync time from the BC.

32.21.10Synchronization schemes: RT with external time base(s)

If an external timer is available, its value can be read out at the same time as the sync time stamp by the hardware using a construct like the one shown below. The first register captures the external timer value whenever a command word is received, and the second register records the time stamp if the command was a sync mode code. With this value, the user will then obtain a common time stamp between the BC time, RT time and external time that can be used in different ways.

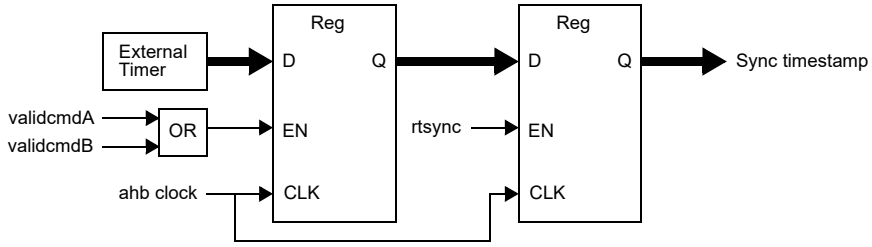


Figure 116. Obtaining an RT sync timestamp in hardware with an external time base

32.21.11Accuracy

32.21.12Accuracy: Propagation delays

When the sync command is sent, there is first an approximate 500 ns of delay inside the core, followed by analog delays, consisting of BC pad delays, BC transmitter delay, bus propagation delays, RT receiver delays, and RT pad delays.

When using the external BC sync, there is also a 2-3 AHB cycle delay before the sync is detected due to synchronization. This creates a small offset between the external time reference and the internal time.

On the RT digital side, there will first be a delay of 20000 ns to receive the whole command word, followed by internal decoding delays of approximately 500 ns before the command word is recognized and the time stamp is taken.

Most of this delay is constant, in particular the 20 us word length, and can therefore be easily compensated for by offsetting the time stamps. Offsetting the RT timestamps by 24 us should be a reasonable first-order approach, accurate within +/- 4 us or so. If more accuracy is needed, characterization measurements or further analysis of the bus system would need to be done.

32.21.13Accuracy: Clock drift

Relative drift between the clocks determine how often synchronization is necessary. Since the internal timers of the BC and RT are as accurate as the codec clocks, and both the clocks must have the 1000 ppm worst-case accuracy permitted by the 1553 standard, the BC and RT timers can drift apart up to 2 us for a sync period of 1 ms. Assuming the external time base is much more accurate, the internal and external BC time bases will drift apart of up to 1 us for every ms of external sync period.

33 GRTIMER - General Purpose Timer Unit

33.1 Overview

The GRTIMER IP core's functionality for latching timer values, external clocking and reload on external events has been merged into the GPTIMER core. All new designs should instantiate the GPTIMER IP core.
A GRTIMER entity exists that is a wrapper around the GPTIMER IP core for backward compatibility.

34 GRACECTRL - AMBA System ACE Interface Controller

34.1 Overview

The core provides an AMBA AHB interface to the microprocessor interface of a Xilinx System ACE Compact Flash Solution. Accesses to the core's memory space are directly translated to accesses on the System ACE microprocessor interface (MPU).

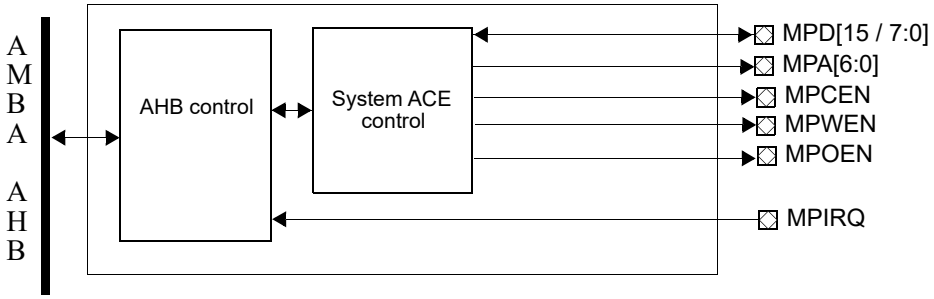


Figure 117. Block diagram

34.2 Operation

34.2.1 Operational model

The core has one AHB I/O area, accesses to this area are directly translated to accesses on the Xilinx System ACE's Microprocessor Interface (MPU). When an access is made to the I/O area, the core first checks if there already is an ongoing access on the MPU. If an access is currently active, the core will respond with an AMBA SPLIT response. If the MPU bus is available, the core will start an access on the MPU bus and issue a SPLIT response to the AMBA master. If the core has been configured for a system that does not support SPLIT responses, it will insert wait states instead.

34.2.2 Bus widths

The AMBA access is directly translated to an MPU access where bits 6:0 of the AMBA address bus are connected to the MPU address bus. The core can be configured to connect to a 16-bit MPU interface or a 8-bit MPU interface. When the core is connected to a 8-bit MPU interface it can emulate 16-bit mode by translating 16-bit (half-word) AMBA accesses into two 8-bit MPU accesses. The mode to use is decided at implementation time via the VHDL generic *mode*.

The core does not perform any checks on the size of the AMBA access and software should only make half-word (16-bit), or byte (8-bit) depending on the setting of VHDL generic *mode*, accesses to the core's memory area. Any other access size will be accepted by the core but the operation may not have the desired result. On AMBA writes the core uses address bit 1 (or address bits 1:0 for 8-bit mode) to select if it should propagate the high or the low part of the AMBA data bus to the MPU data bus. On read operations the core will propagate the read MPU data to all parts of the AMBA data bus.

It is recommended to set the *mode* VHDL generic to 2 for 8-bit MPU interfaces, and to 0 for 16-bit MPU interfaces. This way software can always assume that it communicates via a 16-bit MPU interface (accesses to the System ACE BUSMODEREG register are overriden by the core with suitable values when *mode* is set to 2).

34.2.3 Clocking and synchronization

The core has two clock inputs; the AMBA clock and the System ACE clock. The AMBA clock drives the AHB slave interface and the System ACE clock drives the System ACE interface state machine.

All signals crossing between the two clock domains are synchronized to prevent meta-stability. The system clock should have a higher frequency than the System ACE clock.

34.2.4 Endianness

The core is designed for big-endian systems.

34.3 Registers

The core does implement any registers accessible via AMBA.

34.4 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x067. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

34.5 Implementation

34.5.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

34.5.2 Technology mapping

The core does not instantiate any technology specific primitives.

34.5.3 RAM usage

The core does not use any RAM components.

34.6 Configuration options

Table 412 shows the configuration options of the core (VHDL generics).

*Table 412.*Configuration options

Generic name	Function	Allowed range	Default
hindex	AHB slave index	0 - (NAHBSLV-1)	0
hirq	Interrupt line	0 - (NAHBIRQ-1)	0
haddr	ADDR field of the AHB BAR0	0 - 16#FFF#	16#000#
hmask	MASK field of the AHB BAR0	0 - 16#FFF#	16#FFF#
split	If this generic is set to 1 the core will issue AMBA SPLIT responses when it is busy performing an access to the System ACE. Otherwise the core will insert wait states until the operation completes. Note that SPLIT support on the AHBCTRL core MUST be enabled if this generic is set to 1.	0 - 1	0
swap	If this generic is set to 0 the core will connect the System ACE data(15:0) to AMBA data(15:0). If this generic is set to 1, the core will swap the System ACE data line and connect: System ACE data(15:8) <-> AMBA data(7:0) System ACE data(7 :0) <-> AMBA data(15:8). This generic only has effect for *mode* = 0.	0 - 1	0
oepol	Polarity of pad output enable signal	0 - 1	0

*Table 412.*Configuration options

Generic name	Function	Allowed range	Default
mode	Bus width mode 0: Core is connected to 16-bit MPU. Only half-word AMBA accesses should be made to the core. 1: Core is connected to 8-bit MPU. Only byte AMBA accesses should be made to the core. 2: Core is connected to 8-bit MPU but will emulate a 16-bit MPU interface. Only half-word AMBA accesses should be made to the core (recommended setting for 8-bit MPU interfaces).	0 - 2	0

34.7 Signal descriptions

Table 413 shows the interface signals of the core (VHDL ports).

*Table 413.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
CLKACE	N/A	Input	System ACE clock	-
AHBSI	*	Input	AHB slave input signals	-
AHBSO	*	Output	AHB slave output signals	-
ACEI	DI(15:0)	Input	Data line	-
	IRQ	Input	System ACE interrupt request	High
ACEO	ADDR(6:0)	Output	System ACE address	-
	DO(15:0)	Output	Data line	-
	CEN	Output	System ACE chip enable	Low
	WEN	Output	System ACE write enable	Low
	OEN	Output	System ACE output enable	Low
	DOEN	Output	Data line output enable	-

* see GRLIB IP Library User's Manual

34.8 Signal definitions and reset values

The signals and their reset values are described in table 414.

*Table 414.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
d[15:0]	InputOutput	System ACE data line	-	-
irq	Input	System ACE interrupt request	Logical 1	-
addr[6:0]	Output	System ACE address	-	-
cen	Output	System ACE chip enable	Logical 0	-
wen	Output	System ACE write enable	Logical 0	-
oen	Output	System ACE output enable	Logical 0	-

34.9 Library dependencies

Table 415 shows the libraries used when instantiating the core (VHDL libraries).

*Table 415.*Library dependencies

Library	Package	Imported unit(s)	Description
GAISLER	MISC	Component, signals	Component and signal definitions
GRLIB	AMBA	Signals	AMBA signal definitions

34.10 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib, techmap;
use grlib.amba.all;
use techmap.gencomp.all;

library gaisler;
use gaisler.misc.all;

entity gracectrl_ex is
  port (
    clk        : in  std_ulogic;
    clkace     : in  std_ulogic;
    rstn       : in  std_ulogic;
    sace_a     : out std_logic_vector(6 downto 0);
    sace_mpce  : out std_ulogic;
    sace_d     : inout std_logic_vector(15 downto 0);
    sace_oen   : out std_ulogic;
    sace_wen   : out std_ulogic;
    sace_mpirq : in  std_ulogic;
    );
end;

architecture rtl of gracectrl_ex is
  -- AMBA signals
  signal ahbsi  : ahb_slv_in_type;
  signal ahbso  : ahb_slv_out_vector := (others => ahbs_none);
  ...
  -- GRACECTRL signals
  signal acei : gracectrl_in_type;
  signal aceo : gracectrl_out_type;

begin

  -- AMBA Components are instantiated here
  ...

  -- GRACECTRL core is instantiated below
  grace0 : gracectrl generic map (hindex => 4, hirq => 4, haddr => 16#002#,
                                  hmask => 16#fff#, split => 1)
    port map (rstn, clk, ahbsi, ahbso(4), acei, acoo);
  sace_a_pads : outpadv generic map (width => 7, tech => padtech)
    port map (sace_a, aceo.addr);
  sace_mpce_pad : outpad generic map(tech => padtech)
    port map (sace_mpce, aceo.cen);
  sace_d_pads : iopadv generic map (tech => padtech, width => 16)
    port map (sace_d, aceo.do, aceo.doen, aceo.di);
  sace_oen_pad : outpad generic map (tech => padtech)
    port map (sace_oen, aceo.oen);
  sace_wen_pad : outpad generic map (tech => padtech)
    port map (sace_wen, aceo.wen);
  sace_mpirq_pad : inpad generic map (tech => padtech)
    port map (sace_mpirq, acei.irq);
```

```
end;
```

35 GRAES - Advanced Encryption Standard

35.1 Overview

The Advanced Encryption Standard (AES) is a symmetric encryption algorithm for high throughput application (like audio or video streams). The GRAES core implements the AES-128 algorithm, supporting the Electronic Codebook (ECB) method. The AES-128 algorithm is specified in the "Advanced Encryption Standard (AES)" document, Federal Information Processing Standards (FIPS) Publication 197. The document is established by the National Institute of Standards and Technology (NIST).

The core provides the following internal AMBA AHB slave interface, with sideband signals as per [GRLIB] including:

- interrupt bus
- configuration information
- diagnostic information

The core can be partition in the following hierarchical elements:

- Advanced Encryption Standard (AES) core
- AMBA AHB slave
- GRLIB plug&play wrapper

Note that the core can also be used without the GRLIB plug&play information.

35.2 Operation

The input and output for the AES algorithm each consist of sequences of 128 bits (digits with values of 0 or 1). These sequences will sometimes be referred to as blocks and the number of bits they contain will be referred to as their length. The cipher key for the AES-128 algorithm is a sequence of 128 bits (can also be 192 or 256 bits for other algorithms).

To transfer a 128 bit key or data block four write operations are necessary since the bus interface is 32 bit wide. After supplying a "key will be input" command to the control register, the key is input via four registers. After supplying a "data will be input" command to the control register, the input data is written via four registers. After the last input data register is written, the encryption or decryption is started. The progress can be observed via the debug register. When the operation is completed, an interrupt is generated. The output data is then read out via four registers. Note that the above sequence must be respected. It is not required to write a new key between each data input. There is no command needed for reading out the result.

The implementation requires around 89 clock cycles for a 128 bit data block in encryption direction and around 90 clock cycles for decryption direction. For decryption an initial key calculation is required. This takes around 10 additional clock cycles per every new key. Typically large amounts of data are decrypted (and also encrypted) with the same key. The key initialization for the decryption round does not influence the throughput.

35.3 Background

The Federal Information Processing Standards (FIPS) Publication Series of the National Institute of Standards and Technology (NIST) is the official series of publications relating to standards and guidelines adopted and promulgated under the provisions of the Information Technology Management Reform Act.

The Advanced Encryption Standard (AES) standard specifies the Rijndael algorithm, a symmetric block cipher that can process data blocks of 128 bits, using cipher keys with lengths of 128, 192, and 256 bits. Rijndael was designed to handle additional block sizes and key lengths, however they are not adopted in this standard.

35.4 AES-128 parameters

The GRAES core implements AES-128. An AES algorithm is defined by the following parameters according to FIPS-197:

- *Nk* number of 32-bit words comprising the cipher key
- *Nr* number of rounds

The AES-128 algorithm is specified as *Nk*=4 and *Nr*=10.

The GRAES core has been verified against the complete set of Known Answer Test vectors included in the AES Algorithm Validation Suite (AESAVS) from National Institute of Standards and Technology (NIST), Information Technology Laboratory, Computer Security Division.

35.5 Throughput

The data throughput for the GRAES core is around 128/90 bits per clock cycle, i.e. approximately 1.4 Mbits per MHz.

The underlaying AES core has been implemented in a dual crypto chip on 250 nm technology as depicted in the figure below. The throughput at 33 MHz operating frequency was 42 Mbit/s, the power consumption was 9,6 mW, and the size was 14,5 kgates.

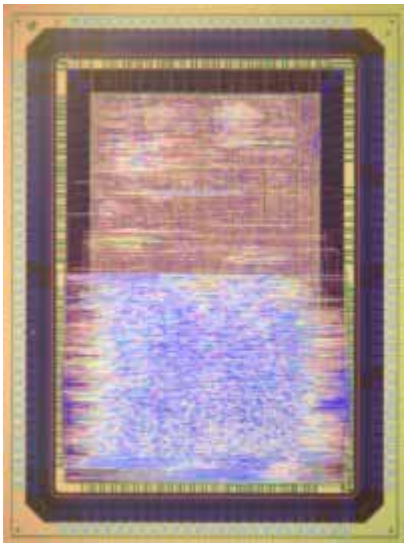


Figure 118. Dual Crypto Chip

35.6 Characteristics

The GRAES core has been synthesized for a Xilinx Virtex-2 XC2V6000-4 devices with the following results:

- LUTs: 5040 (7%)
- 256x1 ROMs (ROM256X1): 128

- Frequency:125 MHz

35.7 Registers

The core is programmed through registers mapped into AHB I/O address space.

*Table 416.*GRAES registers

AHB I/O address offset	Register
0x00	Control Register
0x10	Data Input 0 Register
0x14	Data Input 1 Register
0x18	Data Input 2 Register
0x1C	Data Input 3 Register
0x20	Data Output 0 Register
0x24	Data Output 1 Register
0x28	Data Output 2 Register
0x2C	Data Output 3 Register
0x3C	Debug Register

35.7.1 Control Register

*Table 417.*0x00 - CTRL - Control Register

31 ... 2	1	0
RESERVED	DEC	KEY
-	-	-
w	w	w

31-2: - Unused
1: DEC 0 = “encrypt”, 1 = “decrypt” (only relevant when KEY=1)
0: KEY 0 = “data will be input”, 1 = “key will be input”

Note that the Data Input Registers cannot be written before a command is given to the Control Register. Note that the Data Input Registers must then be written in sequence, and all four registers must be written else the core ends up in an undefined state.

The KEY bit determines whether a key will be input (KEY=1), or data will be input (KEY=0). When a “key will be input” command is written, the DEC bit determines whether decryption (DEC=1) or encryption (DEC=0) should be applied to the subsequent data input.

Note that the register cannot be written after a command has been given, until the specific operation completes. A write access will be terminated with an AMBA AHB error response till the Data Input Register 3 has been written, and the with an AMBA AHB retry response till the operation completes. Any read access to this register results in an AMBA AHB error response.

35.7.2 Debug Register (R)

*Table 418.*0x3C - DEBUG - Debug Register

31	0
FSM	
r	

31-0: FSM Finite State Machine
Any write access to this register results in an AMBA AHB error response.

35.7.3 Data Input Registers (W)

*Table 419.*0x10 - DATAI0 - Data Input 0 Register

31	0
Data/Key(127 downto 96)	
-	
w	

*Table 420.*0x14 - DATAI1 - Data Input 1 Register

31	0
Data/Key(95 downto 64)	
-	
w	

*Table 421.*0x18 - DATAI2 - Data Input 2 Register

31	0
Data/Key(63 downto 32)	
-	
w	

*Table 422.*0x1C - DATAI3 - Data Input 3 Register

31	0
Data/Key(31 downto 0)	
-	
w	

Note that these registers can only be written with a key after a “key will be input” command has been written to the control register. Note that the registers must then be written in sequence, and all four registers must be written else the core ends up in an undefined state.

Note that these registers can only be written with data after a “data will be input” command has been written to the control register, else an AMBA AHB error response is given. Note that the registers must then be written in sequence and all four registers must be written else the core ends up in an undefined state. The encryption or decryption operation is started when the Data Input 3 Register is written to with data.

35.7.4 Data Output Registers (R)

*Table 423.*0x20 - DATAO0 - Data Output 0 Register

31	0
Data(127 downto 96)	
-	
r*	

*Table 424.*0x24 - DATAO1 - Data Output 1 Register

31	0
Data(95 downto 64)	
-	
r*	

*Table 425.*0x28 - DATAO2 - Data Output 2 Register

31	0
Data(63 downto 32)	
-	
r*	

*Table 426.*0x2C - DATAO3 - Data Output 3 Register

31	0
Data(31 downto 0)	
-	
r*	

Note that these registers can only be read after encryption or decryption has been completed. An AMBA AHB retry response is given to read accesses that occur while the encryption or decryption is in progress. If a read access is attempted before an encryption or decryption has even been initiated, then an AMBA AHB erro response is given. Write accesses to these registers result in an AMBA AHB error response.

35.8 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x073. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

35.9 Configuration options

Table 427 shows the configuration options of the core (VHDL generics).

*Table 427.*Configuration options

Generic	Function	Allowed range	Default
hindex	AHB slave index	0 - NAHBSLV-1	0
ioaddr	Addr field of the AHB I/O BAR	0 - 16#FFF#	0
iomask	Mask field of the AHB I/O BAR	0 - 16#FFF#	16#FFC#
hirq	Interrupt line used by the GRAES	0 - NAHBIRQ-1	0

35.10 Signal descriptions

Table 428 shows the interface signals of the core (VHDL ports).

*Table 428.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
AHBI	*	Input	AHB slave input signals	-
AHBO	*	Output	AHB slave output signals	-
DEBUG[0:4]	N/A	Output	Debug information	-

* see GRLIB IP Library User's Manual

Note that the AES core can also be used without the GRLIB plug&play information. The AMBA AHB signals are then provided as IEEE Std_Logic_1164 compatible scalars and vectors.

35.11 Library dependencies

Table 429 shows libraries used when instantiating the core (VHDL libraries).

*Table 429.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	CRYPTO	Component	GRAES component declarations

35.12 Instantiation

This example shows how the core can be instantiated.

```
library  ieee;
use      ieee.std_logic_1164.all;

library  grlib;
use      grlib.amba.all;

library  gaisler;
use      gaisler.crypto.all;
...
...
   signal debug: std_logic_vector(0 to 4);
..
..
   GRAES0: graes
      generic map (
         hindex         => hindex,
         ioaddr         => ioaddr,
         iomask         => iomask,
         hirq           => hirq)
      port map (
         rstn           => rstn,
         clk            => clk,
         ahbi           => ahbsi,
         ahbo           => ahbso(hindex),
         debug          => debug);
```

36 GRAES_DMA - Advanced Encryption Standard with DMA

36.1 Overview

The Advanced Encryption Standard (AES) is a symmetric encryption algorithm for high throughput applications (like audio or video streams). The GRAES_DMA core implements the AES algorithm with 256-bit key length using CTR mode of operation. The AES algorithm is specified in the "Advanced Encryption Standard (AES)" document, Federal Information Processing Standards (FIPS) Publication 197. The document is established by the National Institute of Standards and Technology (NIST). DMA is used for efficiently transferring plaintext and ciphertext to the cryptographic core with minimum CPU involvement.

The core provides an AMBA AHB master interface, with sideband signals as per [GRLIB] including:

- interrupt bus
- configuration information
- diagnostic information

The core can be partition in the following hierarchical elements:

- Advanced Encryption Standard (AES) core
- AMBA AHB master

36.2 Operation

The input and output for the AES algorithm each consist of sequences of 128 bits (digits with values of 0 or 1). These sequences will sometimes be referred to as blocks and the number of bits they contain will be referred to as their length. The cipher key for the AES algorithm supported in this core is a sequence of 256 bits.

To encrypt a message a descriptor must be setup. It contains pointers to memory locations where the key, initialization vector and plaintext are located. The memory addresses for the key and initialization vector must be word aligned while the plaintext can start at any address. If the previous key and/or init vector are to be reused there are control bits in the descriptor which can be used to make the core skip the fetching of the respective pointers and also subsequently skip the fetching of the actual key and initvector. Currently the initvector and key always have to be loaded for the core to operate correctly.

The core can also read the key and initialization vector from input signals. This is done by setting the keyvector and initvector address pointers to all ones.

When one or more descriptors have been enabled the core can be enabled and it will automatically start fetching the necessary values from memory, split the data into the required blocks, encrypt/decrypt and finally write back the result to memory. When each descriptor is finished the core will set the enable bit to 0. An interrupt can also optionally be generated. The result of the encryption or decryption can be either written back to the same memory address from where the plain or ciphertext was read or to a different location specified in an additional pointer. The layout of the descriptor is shown in the tables below.

*Table 430.*GRAES_DMA descriptor word 0 (address offset 0x0)

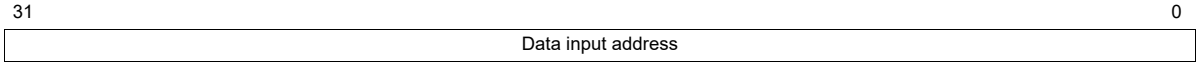
31	21	20	8	7	6	5	4	3	2	1	0
LEN		RESERVED		KE	IV	DO	ED	MD		IE	EN

31: 21	Length (LEN) - Length in bytes of message to process
20: 8	RESERVED
7	Key (KE) - When set a new key will be fetched and used from the memory address set in the key address descriptor word. If not set the currently stored key is used and the key adddress word should not be included in the descriptor.

*Table 430.*GRAES_DMA descriptor word 0 (address offset 0x0)

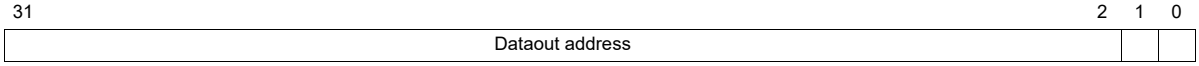
6	Initialization vector (IV) - When set a new initialization vectir will be fetched and used from the memory address set in the initialization vector address descriptor word. If not set the currently stored initialization vector is used and the initialization vector adddress word should not be included in the descriptor.
5	Dataout (DO) - When set the encrypted/decrypted output will be written to the memory address specified in the dataout descriptor word. Otherwise data is written to the same memory address from where the original plaintext/ciphertext was fetched and the dataout address word should not be included in the descriptor.
4	Encrypt-decrypt (ED) - If set to one encryption will be performed otherwise decryption
3	RESERVED
2	RESERVED
1	Interrupt enable (IE) - When set an interrupt will be generated when the processing of the current enabled descriptor is finished and the interrupt enable bit in the control register is set. It should be noted that, the enable bit in the control register might not be cleared yet when a finish interrupt is generated for the last descriptor because the core will read the next descriptor and stop after encountering a '0' on the descriptor control word enable bit which takes some clock cycles.
0	Enable (EN) - When set to '1' indicates that descriptor is enabled and the GRAES core will process it. After the processing is finished this bit will be cleared and the core will jump to the next register. It should be noted that this bit will not be cleared in case a DMA error is encountered at any point of the processing of the current descriptor. If this bit is clear on the first read from the GRAES_DMA core the core will stop processing.

*Table 431.*GRAES_DMA descriptor word 1 (address offset 0x4)



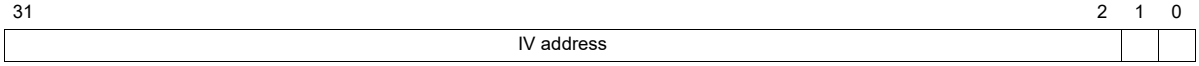
31: 0	Data input address - Memory address pointer where plaintext/ciphertext for encryption/descryption is located.

*Table 432.*GRAES_DMA descriptor word 2(address offset 0x8 if DO is set, otherwise not exist)



31: 2	Dataout address - Memory address where encrypted/decrypted data shall be stored. If the data should be stored at the same location as the input data (DO bit in word 0 is 0) then this word shall not be included in the descriptor.
1: 0	Reserved

*Table 433.*GRAES_DMA descriptor word 3(address offset 0xC if DO and IV is set; address offset 0x8 if DO is clear and IV is set; otherwise not exist.)



31: 2	Initialization vector address - Memory address where initialization vector is located. If a new init-vector is not needed (IV bit in word 0 is 0) then this word shall not be included in the descriptor. If this value is set to 0xFFFFFFFF then the core will take the initialization value from the ivin input signal instead.
1: 0	Must be set to zero unless the init value shall be taken from signal input.

*Table 434.*GRAES_DMA descriptor word 4(address offset 0x10 if DO, IV and KEY is set; address offset 0xC if one of the following bits are set and one of them is clear (DO, IV) and KEY is set; address offset 0x8 if DO and IV is clear and KEY is set; otherwise not exist)

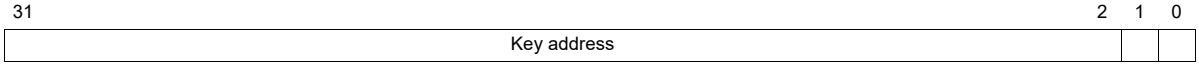
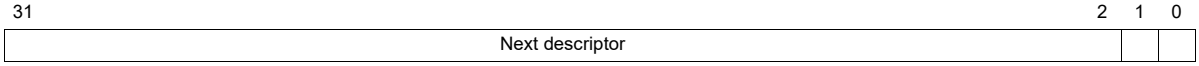


*Table 434.*GRAES_DMA descriptor word 4(address offset 0x10 if DO, IV and KEY is set; address offset 0xC if one of the following bits are set and one of them is clear (DO, IV) and KEY is set; address offset 0x8 if DO and IV is clear and KEY is set; otherwise not exist)

31: 2	Key address - Memory address where key is located. If a new key is not needed (KE bit in word 0 is 0) then this word shall not be included in the descriptor. If this value is set to 0xFFFFFFFF then the core will take the key value from the keyin input signal instead.
1: 0	Must be set to zero unless the init value shall be taken from signal input.

*Table 435.*GRAES_DMA descriptor word 5(address offset 0x14 if DO,IV, KEY is set; address offset 0x10 if two of the following bits are set and one of them is clear (DO,IV,KEY); address offset 0xC if two of the following bits are clear and one of them is set (DO,IV,KEY); address offset 0x8 if DO,IV, and KEY is clear)



31: 2	Next descriptor address - Memory address to the next descriptor.
1: 0	Reserved

The descriptor control word should be written last. If one or more words are not included the offsets of the following words should be adjusted accordingly.

36.3 Background

The Federal Information Processing Standards (FIPS) Publication Series of the National Institute of Standards and Technology (NIST) is the official series of publications relating to standards and guidelines adopted and promulgated under the provisions of the Information Technology Management Reform Act.

The Advanced Encryption Standard (AES) standard specifies the Rijndael algorithm, a symmetric block cipher that can process data blocks of 128 bits, using cipher keys with lengths of 128, 192, and 256 bits. Rijndael was designed to handle additional block sizes and key lengths, however they are not adopted in this standard.

36.4 Characteristics

The GRAES_DMA core has been synthesized for a Actel AX2000-std device with the following results:

- Combinational Cells: 9364 of 21504 (44%)
- Sequential Cells: 2374 of 10752 (22%)
- Total Cells: 11738 of 32256 (37%)
- Block Rams : 0 of 64 (0%)
- Frequency:60 MHz

36.5 Endianness

The core is designed for big-endian systems.

36.6 Registers

The core is programmed through registers mapped into APB address space.

*Table 436.*GRAES_DMA registers

APB address offset	Register
0x0	Control
0x4	Status
0x8	Descriptor address

36.6.1 Control Register

*Table 437.*0x00 - CTRL - GRAES_DMA control register

31	4	3	2	1	0
RESERVED	AB	IOE	KS	IE	EN
0	0	0	0	0	0
r	rw	rw	rw	rw	rw

31: 5 RESERVED

4 Abort (AB) - If set to '1' the core will stop processing after reaching a new descriptor and it will self-clear the Abort and Enable (bit-0) bits. The software can check the status of Abort or Enable bits after setting the Abort bit to see when the core becomes idle.It should be noted that if the last descriptor that is processed when abort bit is set causes a DMA error the DMA error status bit will be set so the software has to make sure to handle a potential error after abort. This bit can only be written if it is clear. Reset value : '0'

3 Interrupt On Error (IOE)- If set to '1' then the core will generate an interrupt when an DMA error is encountered. This bit is independent from the bit-1 (IE). Read the section related to DMA error handling for further details about error handling. This bit can only be written if enable bit is clear.Reset value : '0'

2 Keysize (KS) - If set to '1' then the core will use 128 bit key length. Otherwise the core makes use of 256 bit key length. This bit can only be written if enable bit is clear.Reset value : '0'

1 Interrupt Enable (IE) - If set, an interrupt is generated each time a message has been decrypted. This bit can only be written if enable bit is clear.Reset value: '0'.

0 Enable (EN) - Write a one to this bit each time new descriptors are activated in the list. Writing a one will cause the core to read a new descriptor and perform the requested operation. This bit is automatically cleared when the core encounters a descriptor which is not enabled or if a DMA error is encountered. This bit can not be set when the error bit in the status register is set. Software has to clear the error bit in the status register to be able to set the Enable bit again. Read the Status Register section for more details. This bit can only be written when it is clear but it can initiate the processing of the last descriptor again in certain conditions to allow dynamic addition of descriptors to the link list. For further details read the descriptor processing section. Reset value: '0'

36.6.2 Status Register

*Table 438.*0x04 - STAT - GRAES_DMA status register

31	0
RESERVED	ER
0	0
r	rw

31: 1 RESERVED

0 Error (ER) - The bit is automatically set to 1 when a DMA error is encountered. When it is set, the enable bit in the ctrl register is locked and can not be set until the error bit is cleared. The error bit is cleared by writing '1' to it.

36.6.3 Descriptor Address

*Table 439.*0x08 - ADDR - GRAES_DMA Descriptor address

31	2	1	0
Descriptor address			R
0			0
rw			r

31: 2 Current descriptor address - Points to current descriptor. Can be initialized with a new pointer when the core is disabled. Is updated by the core while it is progressing through the list of descriptors.

1: 0 RESERVED

36.7 Descriptor Processing

Software should set up the descriptor or descriptor chain as it described in the operation section. There are two ways to finish the processing of a descriptor or a descriptor chain. First way is to link the next descriptor to itself for the last descriptor in the chain. After processing, the enable bit of the descriptor control word is automatically cleared so if the next descriptor points to itself the enable bit will be cleared and when read again and the core will stop. Another way is to allocate an empty pointer in which the enable bit of the descriptor word is cleared and link it as a last descriptor. It should be noted that when an empty pointer is allocated, size of it should be equal to the maximum possible size (6 words), although the content of the unused words does not matter as soon as the descriptor is not enabled.

If interrupt enable bit is set, an interrupt will be generated after processing an enabled descriptor. But it should be noted that after an interrupt is generated for the last enabled descriptor in the chain, the enable bit in the control word might not be cleared yet due to core being started to process the next descriptor in which it encounters a cleared enable bit and clears the enable bit in the control register. If the software updates the last disabled pointer in the list and enables it while the core is running, and sets the enable bit in the control register while it is already set and it was reading the last pointer, the core will reprocess the last descriptor if the descriptor enable bit was cleared (it did not read the updated descriptor control word), to make sure operation to continue. If the software makes this modification and sets the enable bit in the control register while it was set, then the core will anyway continue operation because it will read the last descriptor as enabled. This feature allows for safe dynamic addition of descriptors to the list while processing is ongoing. It should be noted the control word of a descriptor should always be written last.

The core will immediately stop processing on an DMA error and software has to take certain steps which are explained in the next section (Error Handling).

36.8 Error Handling

If the core encounters a DMA error, the processing will be immediately stopped (enable bit in the core control register will be cleared) and the error bit in the status register will be set. If interrupt on error is enabled an interrupt will also be generated regardless of interrupt enable bit is set on the descriptor control word. When the error bit in the status register is set, the descriptor address that resides in the descriptor address register is the descriptor that caused the DMA error. It should be noted that the enable bit in the descriptor control word will not be cleared during error. In addition, the enable bit in the control word will be locked if the error bit in the status register is set. So after an error the software has to clear the error bit by writing ‘1’ to the position of error bit in the status register. The software should check the status of error bit after the processing of a descriptor chain is finished (en bit is cleared in the control register), to make sure no error has occurred and clear the error bit after an error in order to be able to proceed with the next operations.

After an error is generated the software should either fix the problem related to the error in the descriptor or set the descriptor address to a new descriptor after clearing the error bit and before starting a new operation. Otherwise it can cause an infinite loop because the enable bit of the descriptor word which causes a DMA error is not automatically cleared and the descriptor address points to the failing descriptor when the core stops due to a DMA error.

36.9 Aborting Operation

It is possible to abort the processing of descriptor at a certain point. When the abort bit in the core’s control word is set, the processing will stop when the current descriptor has finished processing. After

the abort operation has successfully finished the abort bit and enable bit in the core's control word will be cleared. After finishing, the descriptor address register points to the descriptor which is not processed due to stopping. It should be noted that abort bit will not interrupt the processing of the current descriptor when it is set, hence it can not resolve a problem of unresponsive DMA. The abort bit can be used to make sure the core goes into idle state as soon as possible and does not create any transactions on the DMA bus anymore.

36.10 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x07B. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

36.11 Implementation

36.11.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core will use asynchronous reset for all registers, if the GRLIB config package setting *grlib_async_reset_enable* is set.

36.12 Configuration options

Table 440 shows the configuration options of the core (VHDL generics).

*Table 440.*Configuration options

Generic	Function	Allowed range	Default
hindex	AHB master index	0 - NAHBMST-1	0
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	Addr field of the APB BAR	0 - 16#FFF#	0
pmask	Mask field of the APB BAR	0 - 16#FFF#	16#FFF#
pirq	Interrupt line used by the GRAES	0 - NAHBIRQ-1	0
extkeyiv	Support key and IV initalization from signals. If this generic is 1 then the keyin and ivin signals can be used to set key and IV values.	0 - 1	0
scantest	Enable SCAN test support	0 - 1	0

36.13 Signal descriptions

Table 441 shows the interface signals of the core (VHDL ports).

*Table 441.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
AHBI	*	Input	AHB master input signals	-
AHBO	*	Output	AHB master output signals	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
KEYIN[255:0]	N/A	Input	Alternative key input	-
IVIN[127:0]	N/A	Input	Alternative IV input	-

* see GRLIB IP Library User's Manual

36.14 Library dependencies

Table 442 shows libraries used when instantiating the core (VHDL libraries).

*Table 442.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	CRYPTO	Component	GRAES component declarations

36.15 Instantiation

This example shows how the core can be instantiated.

```
entity graes_dma_tb is
   generic(
      hindex:        in    Integer := 0;
      pindex:        in    Integer := 0;
      paddr:         in    Integer := 0;
      pmask:         in    Integer := 16#fff#;
      pirq:          in    Integer := 1);

end entity graes_dma_tb;


signal   rstn:          std_ulogic := '0';
signal   clk:           std_ulogic := '0';
signal   apbi:          apb_slv_in_type;
signal   apbo:          apb_slv_out_vector := (others => apb_none);
signal   ahbmi:         ahb_mst_in_type;
signal   ahbmo:         ahb_mst_out_vector := (others => ahbm_none);

graes0: graes_dma
     generic map(
       hindex         => hindex,
       pindex         => pindex,
       paddr          => paddr,
       pmask          => pmask,
       pirq           => pirq)
     port map(
       rstn           => rstn,
       clk            => clk,
       ahbi           => ahbmi,
```

```
      ahbo            => ahbmo(hindex),
      apbi            => apbi,
      apbo            => apbo(pindex));
```

37 GRCAN - CAN 2.0 Controller with DMA

37.1 Overview

The CAN controller is assumed to operate in an AMBA bus system where both the AMBA AHB bus and the APB bus are present. The AMBA APB bus is used for configuration, control and status handling. The AMBA AHB bus is used for retrieving and storing CAN messages in memory external to the CAN controller. This memory can be located on-chip, as shown in the block diagram, or external to the chip.

The CAN controller supports transmission and reception of sets of messages by use of circular buffers located in memory external to the core. Separate transmit and receive buffers are assumed. Reception and transmission of sets of messages can be ongoing simultaneously.

After a set of message transfers has been set up via the AMBA APB interface the DMA controller initiates a burst of read accesses on the AMBA AHB bus to fetch messages from memory, which are performed by the AHB master. The messages are then transmitted by the CAN core. When a programmable number of messages have been transmitted, the DMA controller issues an interrupt.

After the reception has been set up via the AMBA APB interface, messages are received by the CAN core. To store messages to memory, the DMA controller initiates a burst of write accesses on the AMBA AHB bus, which are performed by the AHB master. When a programmable number of messages have been received, the DMA controller issues an interrupt.

The CAN controller can detect a SYNC message and generate an interrupt, which is also available as an output signal from the core. The SYNC message identifier is programmable via the AMBA APB interface. Separate synchronisation message interrupts are provided.

The CAN controller can transmit and receive messages on either of two CAN busses, but only on one at a time. The selection is programmable via the AMBA APB interface.

Note that it is not possible to receive a CAN message while transmitting one.

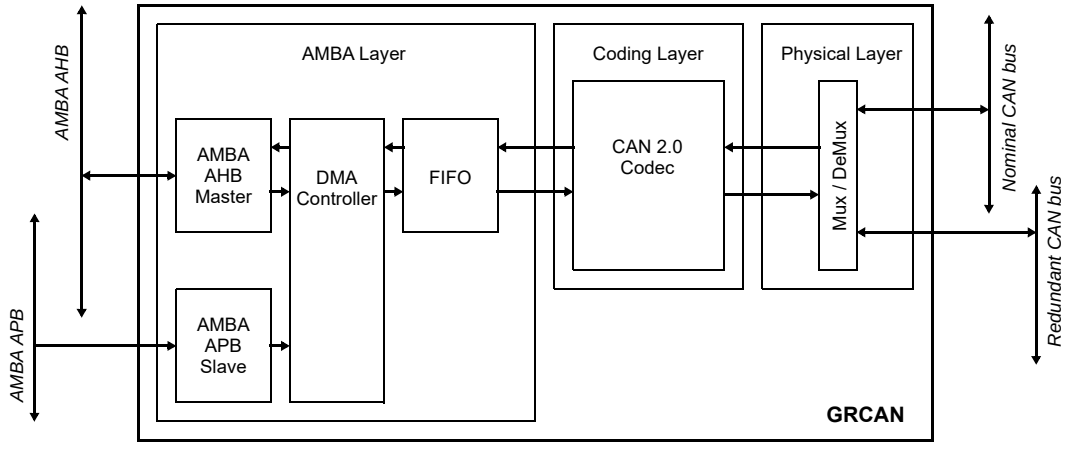


Figure 119. Block diagram

37.1.1 Function

The core implements the following functions:

- CAN protocol
- Message transmission
- Message filtering and reception

- SYNC message reception
- Status and monitoring
- Interrupt generation
- Redundancy selection

37.1.2 Interfaces

The core provides the following external and internal interfaces:

- CAN interface
- AMBA AHB master interface, with sideband signals as per [GRLIB] including:
- cacheability information
- interrupt bus
- configuration information
- diagnostic information
- AMBA APB slave interface, with sideband signals as per [GRLIB] including:
- interrupt bus
- configuration information
- diagnostic information

37.1.3 Hierarchy

The CAN controller core can be partitioned in the following hierarchical elements:

- CAN 2.0 Core
- Redundancy Multiplexer / De-multiplexer
- Direct Memory Access controller
- AMBA APB slave
- AMBA AHB master

37.2 Interface

The external interface towards the CAN bus features two redundant pairs of transmit output and receive input (i.e. 0 and 1).

The active pair (i.e. 0 or 1) is selectable by means of a configuration register bit. Note that all reception and transmission is made over the active pair.

For each pair, there is one enable output (i.e. 0 and 1), each being individually programmable. Note that the enable outputs can be used for enabling an external physical driver. Note that both pairs can be enabled simultaneously. Note that the polarity for the enable/inhibit inputs on physical interface drivers differs, thus the meaning of the enable output is undefined.

Redundancy is implemented by means of Selective Bus Access. Note that the active pair selection above provides means to meet this requirement.

37.3 Protocol

The CAN protocol is based on a CAN 2.0 controller VHDL core. The CAN controller complies with CAN Specification Version 2.0 Part B, except for the overload frame generation.

Note that there are three different CAN types generally defined:

- 2.0A, which considers 29 bit ID messages as an error

- 2.0B Passive, which ignores 29 bit ID messages
- 2.0B Active, which handles 11 and 29 bit ID messages

Only 2.0B Active is implemented.

37.4 Status and monitoring

The CAN interface incorporates status and monitoring functionalities. This includes:

- Transmitter active indicator
- Bus-Off condition indicator
- Error-Passive condition indicator
- Over-run indicator
- 8-bit Transmission error counter
- 8-bit Reception error counter

The status is available via a register and is also stored in a circular buffer for each received message.

37.5 Transmission

The transmit channel is defined by the following parameters:

- base address
- buffer size
- write pointer
- read pointer

The transmit channel can be enabled or disabled.

37.5.1 Circular buffer

The transmit channel operates on a circular buffer located in memory external to the CAN controller. The circular buffer can also be used as a straight buffer. The buffer memory is accessed via the AMBA AHB master interface.

Each CAN message occupies 4 consecutive 32-bit words in memory. Each CAN message is aligned to 4 words address boundaries (i.e. the 4 least significant byte address bits are zero for the first word in a CAN message).

The size of the buffer is defined by the CanTxSIZE.SIZE field, specifying the number of CAN messages * 4 that fit in the buffer.

E.g. CanTxSIZE.SIZE =2 means 8 CAN messages fit in the buffer.

Note however that it is not possible to fill the buffer completely, leaving at least one message position in the buffer empty. This is to simplify wrap-around condition checking.

E.g. CanTxSIZE.SIZE =2 means that 7 CAN messages fit in the buffer at any given time.

37.5.2 Write and read pointers

The write pointer (CanTxWR.WRITE) indicates the position+1 of the last CAN message written to the buffer. The write pointer operates on number of CAN messages, not on absolute or relative addresses.

The read pointer (CanTxRD.READ) indicates the position+1 of the last CAN message read from the buffer. The read pointer operates on number of CAN messages, not on absolute or relative addresses.

The difference between the write and the read pointers is the number of CAN messages available in the buffer for transmission. The difference is calculated using the buffer size, specified by the CanTxSIZE.SIZE field, taking wrap around effects of the circular buffer into account.

Examples:

- There are 2 CAN messages available for transmit when CanTxSIZE.SIZE=2, CanTxWR.WRITE=2 and CanTxRD.READ=0.
- There are 2 CAN messages available for transmit when CanTxSIZE.SIZE=2, CanTxWR.WRITE =0 and CanTxRD.READ =6.
- There are 2 CAN messages available for transmit when CanTxSIZE.SIZE=2, CanTxWR.WRITE =1 and CanTxRD.READ =7.
- There are 2 CAN messages available for transmit when CanTxSIZE.SIZE=2, CanTxWR.WRITE =5 and CanTxRD.READ =3.

When a CAN message has been successfully transmitted, the read pointer (CanTxRD.READ) is automatically incremented, taking wrap around effects of the circular buffer into account. Whenever the write pointer CanTxWR.WRITE and read pointer CanTxRD.READ are equal, there are no CAN messages available for transmission.

37.5.3 Location

The location of the circular buffer is defined by a base address (CanTxADDR.ADDR), which is an absolute address. The location of a circular buffer is aligned on a 1kbyte address boundary.

37.5.4 Transmission procedure

When the channel is enabled (CanTxCTRL.ENABLE=1), as soon as there is a difference between the write and read pointer, a message transmission will be started. Note that the channel should not be enabled if a potential difference between the write and read pointers could be created, to avoid the message transmission to start prematurely.

A message transmission will begin with a fetch of the complete CAN message from the circular buffer to a local fetch-buffer in the CAN controller. After a successful data fetch, a transmission request will be forwarded to the CAN core. If there is at least an additional CAN message available in the circular buffer, a prefetch of this CAN message from the circular buffer to a local prefetch-buffer in the CAN controller will be performed. The CAN controller can thus hold two CAN messages for transmission: one in the fetch buffer, which is fed to the CAN core, and one in the prefetch buffer.

After a message has been successfully transmitted, the prefetch-buffer contents are moved to the fetch buffer (provided that there is message ready). The read pointer (CanTxRD.READ) is automatically incremented after a successful transmission, i.e. after the fetch-buffer contents have been transmitted, taking wrap around effects of the circular buffer into account. If there is at least an additional CAN message available in the circular buffer, a new prefetch will be performed.

If the write and read pointers are equal, no more prefetches and fetches will be performed, and transmission will stop.

If the single shot mode is enabled for the transmit channel (CanTxCTRL.SINGLE=1), any message for which the arbitration is lost, or failed for some other reason, will lead to the disabling of the channel (CanTxCTRL.ENABLE=0), and the message will not be put up for re-arbitration.

Interrupts are provided to aid the user during transmission, as described in detail later in this section. The main interrupts are the Tx, TxEmpty and TxIrq which are issued on the successful transmission of a message, when all messages have been transmitted successfully and when a predefined number of messages have been transmitted successfully. The TxLoss interrupt is issued whenever transmission arbitration has been lost, could also be caused by a communications error. The TxSync interrupt is issued when a message matching the SYNC Code Filter Register.SYNC and SYNC Mask Filter Reg-

ister.MASK registers is successfully transmitted. Additional interrupts are provided to signal error conditions on the CAN bus and AMBA bus.

37.5.5 Straight buffer

It is possible to use the circular buffer as a straight buffer, with a higher granularity than the 1kbyte address boundary limited by the base address (CanTxADDR.ADDR) field.

While the channel is disabled, the read pointer (CanTxRD.READ) can be changed to an arbitrary value pointing to the first message to be transmitted, and the write pointer (CanTxWR.WRITE) can be changed to an arbitrary value.

When the channel is enabled, the transmission will start from the read pointer and continue to the write pointer.

37.5.6 AMBA AHB error

Definition:

- a message fetch occurs when no other messages is being transmitted
- a message prefetch occurs when a previously fetched message is being transmitted
- the local fetch buffer holds the message being fetched
- the local prefetch buffer holds the message being prefetched
- the local fetch buffer holds the message being transmitted by the CAN core
- a successfully prefetched message is copied from the local prefetch buffer to the local fetch buffer when that buffer is freed after a successful transmission.

An AHB error response occurring on the AMBA AHB bus while a CAN message is being fetched will result in a TxAHBErr interrupt.

If the CanCONF.ABORT bit is set to 0b, the channel causing the AHB error will skip the message being fetched from memory and will increment the read pointer. No message will be transmitted.

If the CanCONF.ABORT bit is set to 1b, the channel causing the AHB error will be disabled (CanTxCTRL.ENABLE is cleared automatically to 0 b). The read pointer can be used to determine which message caused the AHB error. Note that it could be any of the four word accesses required to read a message that caused the AHB error.

If the CanCONF.ABORT bit is set to 1b, all accesses to the AMBA AHB bus will be disabled after an AMBA AHB error occurs, as indicated by the CanSTAT.AHBErr bit being 1b. The accesses will be disabled until the CanSTAT register is read, and automatically clearing bit CanSTAT.AHBErr.

An AHB error response occurring on the AMBA AHB bus while a CAN message is being prefetched will not cause an interrupt, but will stop the ongoing prefetch and further prefetch will be prevented temporarily. The ongoing transmission of a CAN message from the fetch buffer will not be affected. When the fetch buffer is freed after a successful transmission, a new fetch will be initiated, and if this fetch results in an AHB error response occurring on the AMBA AHB bus, this will be handled as for the case above. If no AHB error occurs, prefetch will be allowed again.

37.5.7 Enable and disable

When an enabled transmit channel is disabled (CanTxCTRL.ENABLE=0b), any ongoing CAN message transfer request will not be aborted until a CAN bus arbitration is lost or the message has been sent successfully. If the message is sent successfully, the read pointer (CanTxRD.READ) is automatically incremented. Any associated interrupts will be generated.

The progress of the any ongoing access can be observed via the CanTxCTRL.ONGOING bit. The CanTxCTRL.ONGOING must be 0b before the channel can be re-configured safely (i.e. changing

address, size or read pointer). It is also possible to wait for the Tx and TxLoss interrupts described hereafter.

The channel can be re-enabled again without the need to re-configure the address, size and pointers.

Priority inversion is handled by disabling the transmitting channel, i.e. setting CanTxCTRL.ENABLE=0b as described above, and observing the progress, i.e. reading via the CanTxCTRL.ONGOING bit as described above. When the transmit channel is disabled, it can be reconfigured and a higher priority message can be transmitted. Note that the single shot mode does not require the channel to be disabled, but the progress should still be observed as above.

No message transmission is started while the channel is not enabled.

37.5.8 Interrupts

During transmission several interrupts can be generated:

- TxLoss: Message arbitration lost for transmit (could be caused by communications error, as indicated by other interrupts as well)
- TxErrCntr: Error counter incremented for transmit
- TxSync: Synchronization message transmitted
- Tx: Successful transmission of one message
- TxEmpty: Successful transmission of all messages in buffer
- TxIrq: Successful transmission of a predefined number of messages
- TxAHBErr: AHB access error during transmission
- Off: Bus-off condition
- Pass: Error-passive condition

The Tx, TxEmpty and TxIrq interrupts are only generated as the result of a successful message transmission, after the CanTxRD.READ pointer has been incremented.

37.6 Reception

The receive channel is defined by the following parameters:

- base address
- buffer size
- write pointer
- read pointer

The receive channel can be enabled or disabled.

37.6.1 Circular buffer

The receive channel operates on a circular buffer located in memory external to the CAN controller. The circular buffer can also be used as a straight buffer. The buffer memory is accessed via the AMBA AHB master interface.

Each CAN message occupies 4 consecutive 32-bit words in memory. Each CAN message is aligned to 4 words address boundaries (i.e. the 4 least significant byte address bits are zero for the first word in a CAN message).

The size of the buffer is defined by the CanRxSIZE.SIZE field, specifying the number of CAN messages * 4 that fit in the buffer.

E.g. CanRxSIZE.SIZE=2 means 8 CAN messages fit in the buffer.

Note however that it is not possible to fill the buffer completely, leaving at least one message position in the buffer empty. This is to simplify wrap-around condition checking.

E.g. CanRxSIZE.SIZE=2 means that 7 CAN messages fit in the buffer at any given time.

37.6.2 Write and read pointers

The write pointer (CanRxWR.WRITE) indicates the position+1 of the last CAN message written to the buffer. The write pointer operates on number of CAN messages, not on absolute or relative addresses.

The read pointer (CanRxRD.READ) indicates the position+1 of the last CAN message read from the buffer. The read pointer operates on number of CAN messages, not on absolute or relative addresses.

The difference between the write and the read pointers is the number of CAN message positions available in the buffer for reception. The difference is calculated using the buffer size, specified by the CanRxSIZE.SIZE field, taking wrap around effects of the circular buffer into account.

Examples:

- There are 2 CAN messages available for read-out when CanRxSIZE.SIZE=2, CanRxWR.WRITE=2 and CanRxRD.READ=0.
- There are 2 CAN messages available for read-out when CanRxSIZE.SIZE=2, CanRxWR.WRITE =0 and CanRxRD.READ=6.
- There are 2 CAN messages available for read-out when CanRxSIZE.SIZE=2, CanRxWR.WRITE =1 and CanRxRD.READ=7.
- There are 2 CAN messages available for read-out when CanRxSIZE.SIZE=2, CanRxWR.WRITE =5 and CanRxRD.READ=3.

When a CAN message has been successfully received and stored, the write pointer (CanRxWR.WRITE) is automatically incremented, taking wrap around effects of the circular buffer into account. Whenever the read pointer CanRxRD.READ equals (CanRxWR.WRITE+1) modulo (CanRxSIZE.SIZE*4), there is no space available for receiving another CAN message.

The error behavior of the CAN core is according to the CAN standard, which applies to the error counter, buss-off condition and error-passive condition.

37.6.3 Location

The location of the circular buffer is defined by a base address (CanRxADDR.ADDR), which is an absolute address. The location of a circular buffer is aligned on a 1kbyte address boundary.

37.6.4 Reception procedure

When the channel is enabled (CanRxCTRL.ENABLE=1), and there is space available for a message in the circular buffer (as defined by the write and read pointer), as soon as a message is received by the CAN core, an AMBA AHB store access will be started. The received message will be temporarily stored in a local store-buffer in the CAN controller. Note that the channel should not be enabled until the write and read pointers are configured, to avoid the message reception to start prematurely

After a message has been successfully stored the CAN controller is ready to receive a new message. The write pointer (CanRxWR.WRITE) is automatically incremented, taking wrap around effects of the circular buffer into account.

Interrupts are provided to aid the user during reception, as described in detail later in this section. The main interrupts are the Rx, RxFull and RxIrq which are issued on the successful reception of a message, when the message buffer has been successfully filled and when a predefined number of messages have been received successfully. The RxMiss interrupt is issued whenever a message has been received but does not match a message filtering setting, i.e. neither for the receive channel nor for the SYNC message described hereafter.

The RxSync interrupt is issued when a message matching the SYNC Code Filter Register.SYNC and SYNC Mask Filter Register.MASK registers has been successfully received. Additional interrupts are provided to signal error conditions on the CAN bus and AMBA bus.

37.6.5 Straight buffer

It is possible to use the circular buffer as a straight buffer, with a higher granularity than the 1kbyte address boundary limited by the base address (CanRxADDR.ADDR) field.

While the channel is disabled, the write pointer (CanRxWR.WRITE) can be changed to an arbitrary value pointing to the first message to be received, and the read pointer (CanRxRD.READ) can be changed to an arbitrary value.

When the channel is enabled, the reception will start from the write pointer and continue to the read pointer.

37.6.6 AMBA AHB error

An AHB error response occurring on the AMBA AHB bus while a CAN message is being stored will result in an RxAHBErr interrupt.

If the CanCONF.ABORT bit is set to 0b, the channel causing the AHB error will skip the received message, not storing it to memory. The write pointer will be incremented.

If the CanCONF.ABORT bit is set to 1b, the channel causing the AHB error will be disabled (CanRxCTRL.ENABLE is cleared automatically to 0b). The write pointer can be used to determine which message caused the AHB error. Note that it could be any of the four word accesses required to writ a message that caused the AHB error.

If the CanCONF.ABORT bit is set to 1b, all accesses to the AMBA AHB bus will be disabled after an AMBA AHB error occurs, as indicated by the CanSTAT.AHBErr bit being 1b. The accesses will be disabled until the CanSTAT register is read, and automatically clearing bit CanSTAT.AHBErr.

37.6.7 Enable and disable

When an enabled receive channel is disabled (CanRxCTRL.ENABLE=0b), any ongoing CAN message storage on the AHB bus will not be aborted, and no new message storage will be started. Note that only complete messages can be received from the CAN core. If the message is stored successfully, the write pointer (CanRxWR.WRITE) is automatically incremented. Any associated interrupts will be generated.

The progress of the any ongoing access can be observed via the CanRxCTRL.ONGOING bit. The CanRxCTRL.ONGOING must be 0b before the channel can be re-configured safely (i.e. changing address, size or write pointer). It is also possible to wait for the Rx and RxMiss interrupts described hereafter.

The channel can be re-enabled again without the need to re-configure the address, size and pointers.

No message reception is performed while the channel is not enabled

37.6.8 Interrupts

During reception several interrupts can be generated:

- RxMiss: Message filtered away for receive
- RxErrCntr: Error counter incremented for receive
- RxSync: Synchronization message received
- Rx: Successful reception of one message
- RxFull: Successful reception of all messages possible to store in buffer

- RxIrq: Successful reception of a predefined number of messages
- RxAHBErr: AHB access error during reception
- OR: Over-run during reception
- OFF: Bus-off condition
- PASS: Error-passive condition

The Rx, RxFull and RxIrq interrupts are only generated as the result of a successful message reception, after the CanRxWR.WRITE pointer has been incremented.

The OR interrupt is generated when a message is received while a previously received message is still being stored. A full circular buffer will lead to OR interrupts for any subsequently received messages. Note that the last message stored which fills the circular buffer will not generate an OR interrupt. The overrun is also reported with the CanSTAT.OR bit, which is cleared when reading the register.

The error behavior of the CAN core is according to the CAN standard, which applies to the error counter, buss-off condition and error-passive condition.

37.7 Global reset and enable

When the CanCTRL.RESET bit is set to 1b, a reset of the core is performed. The reset clears all the register fields to their default values. Any ongoing CAN message transfer request will be aborted, potentially violating the CAN protocol.

When the CanCTRL.ENABLE bit is cleared to 0b, the CAN core is reset and the configuration bits CanCONF.SCALER, CanCONF.PS1, CanCONF.PS2, CanCONF.RSJ and CanCONF.BPR may be modified. When disabled, the CAN controller will be in sleep mode not affecting the CAN bus by only sending recessive bits. Note that the CAN core requires that 10 recessive bits are received before any reception or transmission can be initiated. This can be caused either by no unit sending on the CAN bus, or by random bits in message transfers.

37.8 Interrupt

Three interrupts are implemented by the CAN interface:

Index:	Name:	Description:
0	IRQ	Common output from interrupt handler
1	TxSYNC	Synchronization message transmitted (optional)
2	RxSYNC	Synchronization message received (optional)

The interrupts are configured by means of the *pirq* VHDL generic and the *singleirq* VHDL generic.

37.9 Endianness

The core is designed for big-endian systems.

37.10 Registers

The core is programmed through registers mapped into APB address space.

*Table 443.*GRCAN registers

APB address offset	Register
0x000	Configuration Register
0x004	Status Register
0x008	Control Register
0x018	SYNC Mask Filter Register
0x01C	SYNC Code Filter Register
0x100	Pending Interrupt Masked Status Register
0x104	Pending Interrupt Masked Register
0x108	Pending Interrupt Status Register
0x10C	Pending Interrupt Register
0x110	Interrupt Mask Register
0x114	Pending Interrupt Clear Register
0x200	Transmit Channel Control Register
0x204	Transmit Channel Address Register
0x208	Transmit Channel Size Register
0x20C	Transmit Channel Write Register
0x210	Transmit Channel Read Register
0x214	Transmit Channel Interrupt Register
0x300	Receive Channel Control Register
0x304	Receive Channel Address Register
0x308	Receive Channel Size Register
0x30C	Receive Channel Write Register
0x310	Receive Channel Read Register
0x314	Receive Channel Interrupt Register
0x318	Receive Channel Mask Register
0x31C	Receive Channel Code Register

37.10.1 Configuration Register

*Table 444.*Configuration Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCALER								PS1				PS2			
0								0				0			
rw								rw				rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSJ					BPR				SAM	Silent	Select	Enable1	Enable0	Abort
	0					0				0	0	0	0	0	0
	rw					rw				rw	rw	rw	rw	rw	rw

31-24: SCALER Prescaler setting, 8-bit: system clock / (SCALER +1)
23-20: PS1 Phase Segment 1, 4-bit: (valid range 1 to 15)
19-16: PS2 Phase Segment 2, 4-bit: (valid range 2 to 8)
14-12: RSJ ReSynchronization Jumps, 3-bit: (valid range 1 to 4)

9:8:	BPR	Baud rate, 2-bit: 00b = system clock / (SCALER +1) / 1 01b = system clock / (SCALER +1) / 2 10b = system clock / (SCALER +1) / 4 11b = system clock / (SCALER +1) / 8
5:	SAM	Single sample when 0b. Triple sample when 1b.
4:	SILENT	Listen only to the CAN bus, send recessive bits.
3:	SELECT	Selection receiver input and transmitter output: Select receive input 0 as active when 0b, Select receive input 1 as active when 1b Select transmit output 0 as active when 0b, Select transmit output 1 as active when 1b
2:	ENABLE1	Set value of output 1 enable
1:	ENABLE0	Set value of output 0 enable
0:	ABORT	Abort transfer on AHB ERROR

All bits are cleared to 0 at reset.

Note that constraints on PS1, PS2 and RSJ are defined as:

- PS1 +1 >= PS2
- PS1 > PS2
- PS2 >= RSJ

Note that CAN standard TSEG1 is defined by PS1+1.

Note that CAN standard TSEG2 is defined by PS2.

Note that the SCALER setting defines the CAN time quantum, together with the BPR setting:

system clock / ((SCALER+1) * BPR)

where SCALER is in range 0 to 255, and the resulting division factor due to BPR is 1, 2, 4 or 8.

For a quantum equal to one system clock period, an additional quantum is added to the node delay. Note that for minimizing the node delay, then set either SCALER > 0 or BRP > 0.

Note that the resulting bit rate is:

system clock / ((SCALER+1) * BPR * (1+ PS1+1 + PS2))

where PS1 is in the range 1 to 15, and PS2 is in the range 2 to 8.

Note that RSJ defines the number of allowed re-synchronization jumps according to the CAN standard, being in the range 1 to 4.

For SAM = 0b (single), the bus is sampled once; recommended for high speed buses (SAE class C).

For SAM = 1b (triple), the bus is sampled three times; recommended for low/medium speed buses (SAE class A and B) where filtering spikes on the bus line is beneficial.

Note that the transmit or receive channel active during the AMBA AHB error is disabled if the ABORT bit is set to 1b. Note that all accesses to the AMBA AHB bus will be disabled after an AMBA AHB error occurs while the ABORT bit is set to 1b. The accesses will be disabled until the CanSTAT register is read.

37.10.2 Status Register

*Table 445.*Status register

31 28	27 24	23 16
TxChannels	RxChannels	TxErrCntr
0	0	0
r	r	r

15 8	7	6	5	4	3	2	1	0
RxErrCntr				Active	AHB Err	OR	Off	Pass
0				0	0	0	0	0
r				r	r	r	r	r

31-28: TxChannelsNumber of TxChannels -1, 4-bit
27-24: RxChannelsNumber of RxChannels -1, 4-bit
23-16: TxErrCntr Transmission error counter, 8-bit
15-8: RxErrCntr Reception error counter, 8-bit
4: ACTIVE Transmission ongoing
3: AHBErr AMBA AHB master interface blocked due to previous AHB error
2: OR Overrun during reception
1: OFF Bus-off condition
0: PASS Error-passive condition

All bits are cleared to 0 at reset.

The OR bit is set if a message with a matching ID is received and cannot be stored via the AMBA AHB bus, this can be caused by bandwidth limitations or when the circular buffer for reception is already full.

The OR and AHBErr status bits are cleared when the register has been read.

Note that TxErrCntr and RxErrCntr are defined according to CAN protocol.

Note that the AHBErr bit is only set to 1b if an AMBA AHB error occurs while the Can-CONF.ABORT bit is set to 1b.

37.10.3 Control Register

*Table 446.*Control Register

31 2	1	0
	Reset	Enable
	0	0
	rw	rw

1: RESET Reset complete core when 1
0: ENABLE Enable CAN controller, when 1. Reset CAN controller, when 0

All bits are cleared to 0 at reset.

Note that RESET is read back as 0b.

Note that ENABLE should be cleared to 0b to while other settings are modified, ensuring that the CAN core is properly synchronized.

Note that when ENABLE is cleared to 0b, the CAN interface is in sleep mode, only outputting recessive bits.

Note that the CAN core requires that 10 recessive bits be received before receive and transmit operations can begin.

37.10.4 SYNC Code Filter Register

*Table 447.*SYNC Code Filter Register

31	30	29	28	0
			SYNC	
			0	
			rw	

28-0: SYNC Message Identifier

All bits are cleared to 0 at reset.

Note that Base ID is bits 28 to 18 and Extended ID is bits 17 to 0.

37.10.5 SYNC Mask Filter Register

*Table 448.*SYNC Mask Filter Register

31	30	29	28	0
			MASK	
			0x1FFFFFFF	
			rw	

28-0: MASK Message Identifier

All bits are set to 1 at reset.

Note that Base ID is bits 28 to 18 and Extended ID is bits 17 to 0.

A RxSYNC message ID is matched when:

((Received-ID XOR CanCODE.SYNC) AND CanMASK.MASK) = 0

A TxSYNC message ID is matched when:

((Transmitted-ID XOR CanCODE.SYNC) AND CanMASK.MASK) = 0

37.10.6 Transmit Channel Control Register

*Table 449.*Transmit Channel Control Register

31												3	2	1	0
													Sin-gle	Ong oing	Ena ble
													0	0	0
													rw	rw	rw

2: SINGLE Single shot mode
1: ONGOING Transmission ongoing
0: ENABLE Enable channel

All bits are cleared to 0 at reset.

Note that if the SINGLE bit is 1b, the channel is disabled (i.e. the ENABLE bit is cleared to 0b) if the arbitration on the CAN bus is lost.

Note that in the case an AHB bus error occurs during an access while fetching transmit data, and the CanCONF.ABORT bit is 1b, then the ENABLE bit will be reset automatically.

At the time the ENABLE is cleared to 0b, any ongoing message transmission is not aborted, unless the CAN arbitration is lost or communication has failed.

Note that the ONGOING bit being 1b indicates that message transmission is ongoing and that configuration of the channel is not safe.

37.10.7 Transmit Channel Address Register

*Table 450.*Transmit Channel Address Register

31 10	9 0
ADDR	
0	
rw	

31-10: ADDR Base address for circular buffer

All bits are cleared to 0 at reset.

37.10.8 Transmit Channel Size Register

*Table 451.*Transmit Channel Size Register

31 21	20 6	5 0
	SIZE	
	0	
	rw	

20-6: SIZE The size of the circular buffer is SIZE*4 messages

All bits are cleared to 0 at reset.

Valid SIZE values are between 0 and 16384.

Note that each message occupies four 32-bit words.

Note that the resulting behavior of invalid SIZE values is undefined.

Note that only (SIZE*4)-1 messages can be stored simultaneously in the buffer. This is to simplify wrap-around condition checking.

The width of the SIZE field may be made configurable by means of a VHDL generic. In this case it should be set to 16-1 bits width.

37.10.9 Transmit Channel Write Register

*Table 452.*Transmit Channel Write Register

31 20	19 4	3 0
	WRITE	
	0	
	rw	

19-4: WRITE Pointer to last written message +1

All bits are cleared to 0 at reset.

The WRITE field is written to in order to initiate a transfer, indicating the position +1 of the last message to transmit.

Note that it is not possible to fill the buffer. There is always one message position in buffer unused. Software is responsible for not over-writing the buffer on wrap around (i.e. setting WRITE=READ).

The field is implemented as relative to the buffer base address (scaled with the SIZE field).

37.10.10Transmit Channel Read Register

*Table 453.*Transmit Channel Read Register

31 20	19 4	3 0
	READ	
	0	
	rw	

19-4: READ Pointer to last read message +1

All bits are cleared to 0 at reset.

The READ field is written to automatically when a transfer has been completed successfully, indicating the position +1 of the last message transmitted.

Note that the READ field can be use to read out the progress of a transfer.

Note that the READ field can be written to in order to set up the starting point of a transfer. This should only be done while the transmit channel is not enabled.

Note that the READ field can be automatically incremented even if the transmit channel has been disabled, since the last requested transfer is not aborted until CAN bus arbitration is lost.

When the Transmit Channel Read Pointer catches up with the Transmit Channel Write Register, an interrupt is generated (TxEmpty). Note that this indicates that all messages in the buffer have been transmitted.

The field is implemented as relative to the buffer base address (scaled with the SIZE field).

37.10.11Transmit Channel Interrupt Register

*Table 454.*Transmit Channel Interrupt Register

31 20	19 4	3 0
	IRQ	
	0	
	rw	

19-4: IRQ Interrupt is generated when CanTxRD.READ=IRQ, as a consequence of a message transmission

All bits are cleared to 0 at reset.

Note that this indicates that a programmed number of messages have been transmitted.

The field is implemented as relative to the buffer base address (scaled with the SIZE field).

37.10.12Receive Channel Control Register

*Table 455.*Receive Channel Control Register

31	2	1	0
		OnGoing	Enable
		0	0
		r	rw

1: ONGOING Reception ongoing (read-only)
0: ENABLE Enable channel

All bits are cleared to 0 at reset.

Note that in the case an AHB bus error occurs during an access while fetching transmit data, and the CanCONF.ABORT bit is 1b, then the ENALBE bit will be reset automatically.

At the time the ENABLE is cleared to 0b, any ongoing message reception is not aborted

Note that the ONGOING bit being 1b indicates that message reception is ongoing and that configuration of the channel is not safe.

37.10.13Receive Channel Address Register

*Table 456.*Receive Channel Address Register

31	10	9	0
ADDR			
0			
rw			

31-10: ADDR Base address for circular buffer

All bits are cleared to 0 at reset.

37.10.14Receive Channel Size Register

*Table 457.*Receive Channel Size Register

31	21	20	6	5	0
		SIZE			
		0			
		rw			

20-6: SIZE The size of the circular buffer is SIZE*4 messages

All bits are cleared to 0 at reset.

Valid SIZE values are between 0 and 16384.

Note that each message occupies four 32-bit words.

Note that the resulting behavior of invalid SIZE values is undefined.

Note that only (SIZE*4)-1 messages can be stored simultaneously in the buffer. This is to simplify wrap-around condition checking.

The width of the SIZE field may be made configurable by means of a VHDL generic. In this case it should be set to 16-1 bits width.

37.10.15Receive Channel Write Register

*Table 458.*Receive Channel Write Register

31 20	19 4	3 0
	WRITE	
	0	
	rw	

19-4: WRITE Pointer to last written message +1

All bits are cleared to 0 at reset.

The field is implemented as relative to the buffer base address (scaled with the SIZE field).

The WRITE field is written to automatically when a transfer has been completed successfully, indicating the position +1 of the last message received.

Note that the WRITE field can be use to read out the progress of a transfer.

Note that the WRITE field can be written to in order to set up the starting point of a transfer. This should only be done while the receive channel is not enabled.

37.10.16Receive Channel Read Register

*Table 459.*Receive Channel Read Register

31 20	19 4	3 0
	READ	
	0	
	rw	

19-4: READ Pointer to last read message +1

All bits are cleared to 0 at reset.

The field is implemented as relative to the buffer base address (scaled with the SIZE field).

The READ field is written to in order to release the receive buffer, indicating the position +1 of the last message that has been read out.

Note that it is not possible to fill the buffer. There is always one message position in buffer unused. Software is responsible for not over-reading the buffer on wrap around (i.e. setting WRITE=READ).

37.10.17Receive Channel Interrupt Register

*Table 460.*Receive Channel Interrupt Register

31 20	19 4	3 0
	IRQ	
	0	
	rw	

19-4: IRQ Interrupt is generated when CanRxWR.WRITE=IRQ, as a consequence of a message reception

All bits are cleared to 0 at reset.

Note that this indicates that a programmed number of messages have been received.

The field is implemented as relative to the buffer base address (scaled with the SIZE field).

37.10.18Receive Channel Mask Register

*Table 461.*Receive Channel Mask Register

31	30	29	28	0
			AM	
			0x1FFFFFFF	
			rw	

28-0: AM Acceptance Mask, bits set to 1b are taken into account in the comparison between the received message ID and the CanRxCODE.AC field

All bits are set to 1 at reset.

Note that Base ID is bits 28 to 18 and Extended ID is bits 17 to 0.

37.10.19Receive Channel Code Register

*Table 462.*Receive Channel Code Register

31	30	29	28	0
			AC	
			0	
			rw	

28-0: AC Acceptance Code, used in comparison with the received message

All bits are cleared to 0at reset.

Note that Base ID is bits 28 to 18 and Extended ID is bits 17 to 0.

A message ID is matched when:

((Received-ID XOR CanRxCODE.AC) AND CanRxMASS.AM) = 0

37.10.20Interrupt registers

The interrupt registers give complete freedom to the software, by providing means to mask interrupts, clear interrupts, force interrupts and read interrupt status.

When an interrupt occurs the corresponding bit in the Pending Interrupt Register is set. The normal sequence to initialize and handle a module interrupt is:

- Set up the software interrupt-handler to accept an interrupt from the module.
- Read the Pending Interrupt Register to clear any spurious interrupts.
- Initialize the Interrupt Mask Register, unmasking each bit that should generate the module interrupt.
- When an interrupt occurs, read the Pending Interrupt Status Register in the software interrupt-handler to determine the causes of the interrupt.
- Handle the interrupt, taking into account all causes of the interrupt.
- Clear the handled interrupt using Pending Interrupt Clear Register.

Masking interrupts: After reset, all interrupt bits are masked, since the Interrupt Mask Register is zero. To enable generation of a module interrupt for an interrupt bit, set the corresponding bit in the Interrupt Mask Register.

Clearing interrupts: All bits of the Pending Interrupt Register are cleared when it is read or when the Pending Interrupt Masked Register is read. Reading the Pending Interrupt Masked Register yields the

contents of the Pending Interrupt Register masked with the contents of the Interrupt Mask Register. Selected bits can be cleared by writing ones to the bits that shall be cleared to the Pending Interrupt Clear Register.

Forcing interrupts: When the Pending Interrupt Register is written, the resulting value is the original contents of the register logically OR-ed with the write data. This means that writing the register can force (set) an interrupt bit, but never clear it.

Reading interrupt status: Reading the Pending Interrupt Status Register yields the same data as a read of the Pending Interrupt Register, but without clearing the contents.

Reading interrupt status of unmasked bits: Reading the Pending Interrupt Masked Status Register yields the contents of the Pending Interrupt Register masked with the contents of the Interrupt Mask Register, but without clearing the contents.

The interrupt registers comprise the following:

- Pending Interrupt Masked Status Register [CanPIMSR] R
- Pending Interrupt Masked Register [CanPIMR] R
- Pending Interrupt Status Register [CanPISR] R
- Pending Interrupt Register [CanPIR] R/W
- Interrupt Mask Register [CanIMR] R/W
- Pending Interrupt Clear Register [CanPICR] W

*Table 463.*Interrupt registers

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
															Tx Loss
															0
															*
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rx Miss	Tx Err Cntr	Rx Err Cntr	Tx Sync	Rx Sync	Tx	Rx	Tx Empty	Rx Full	Tx IRQ	Rx IRQ	Tx AHB Err	Rx AHB Err	OR	Off	Pass
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

16:	TxLoss	Message arbitration lost during transmission (could be caused by communications error, as indicated by other interrupts as well)
15:	RxMiss	Message filtered away during reception
14:	TxErrCntr	Transmission error counter incremented
13:	RxErrCntr	Reception error counter incremented
12:	TxSync	Synchronization message transmitted
11:	RxSync	Synchronization message received
10:	Tx	Successful transmission of message
9:	Rx	Successful reception of message
8:	TxEmpty	Successful transmission of all messages in buffer
7:	RxFull	Successful reception of all messages possible to store in buffer
6:	TxIRQ	Successful transmission of a predefined number of messages
5:	RxIRQ	Successful reception of a predefined number of messages
4:	TxAHBErr	AHB error during transmission
3:	RxAHBErr	AHB error during reception
2:	OR	Over-run during reception
1:	OFF	Bus-off condition

0: PASS Error-passive condition

All bits in all interrupt registers are reset to 0b after reset.

Note that the TxAHBErr interrupt is generated in such way that the corresponding read and write pointers are valid for failure analysis. The interrupt generation is independent of the CanCONF.ABORT field setting.

Note that the RxAHBErr interrupt is generated in such way that the corresponding read and write pointers are valid for failure analysis. The interrupt generation is independent of the CanCONF.ABORT field setting.

37.11 Memory mapping

The CAN message is represented in memory as shown in table 464.

*Table 464.*CAN message representation in memory.

AHB addr	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0x0	IDE	RTR	-	bID											eID	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	eID															
0x4	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DLC				-	-	-	-	TxErrCntr							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RxErrCntr								-	-	-	-	AhbErr	OR	Off	Pass
0x8	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Byte 0 (first transmitted)								Byte 1							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Byte 2								Byte 3							
0xC	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Byte 4								Byte 5							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Byte 6								Byte 7 (last transmitted)							

Values: Levels according to CAN standard: 1b is recessive, 0b is dominant

Legend: Naming and number in according to CAN standard

IDE Identifier Extension: 1b for Extended Format, 0b for Standard Format

RTR Remote Transmission Request: 1b for Remote Frame, 0b for Data Frame

bID Base Identifier

eID Extended Identifier

DLC Data Length Code, according to CAN standard:

0000b	0 bytes
0001b	1 byte
0010b	2 bytes
0011b	3 bytes

0100b	4 bytes
0101b	5 bytes
0110b	6 bytes
0111b	7 bytes
1000b	8 bytes
OTHERS	illegal

TxErrCntr	Transmission Error Counter
RxErrCntr	Reception Error Counter
AHBErr	AHB interface blocked due to AHB Error when 1b
OR	Reception Over run when 1b
OFF	Bus Off mode when 1b
PASS	Error Passive mode when 1b
Byte 00 to 07	Transmit/Receive data, Byte 00 first Byte 07 last

37.12 Vendor and device identifiers

The module has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x03D. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

37.13 Implementation

37.13.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

37.14 Configuration options

Table 465 shows the configuration options of the core (VHDL generics).

*Table 465.*Configuration options

Generic name	Function	Allowed range	Default
hindex	AHB master index.	0 - NAHBMST-1	0
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	Addr field of the APB bar.	0 - 16#FFF#	0
pmask	Mask field of the APB bar.	0 - 16#FFF#	16#FFC#
pirq	Interrupt line used by the GRCAN.	0 - NAHBIRQ-1	0
singleirq	Implement only one common interrupt	0 - 1	0
txchannels	Number of transmit channels	1 - 1	1
rxchannels	Number of receive channels	1 - 1	1
ptrwidth	Width of message pointers	16 - 16	16

37.15 Signal descriptions

Table 466 shows the interface signals of the core (VHDL ports).

*Table 466.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
AHBI	*	Input	AMB master input signals	-
AHBO	*	Output	AHB master output signals	-
CANI	Rx[1:0]	Input	Receive lines	-
CANO	Tx[1:0]	Output	Transmit lines	-
	En[1:0]		Transmit enables	-

* see GRLIB IP Library User's Manual

37.16 Signal definitions and reset values

The signals and their reset values are described in table 467.

*Table 467.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
cantx[]	Output	CAN transmit data	Low	Logical 1
canen[]	Output	CAN transmitter enable	High	Logical 0
canrx[]	Input	CAN receive data	Low	-

37.17 Timing

The timing waveforms and timing parameters are shown in figure 120 and are defined in table 468.

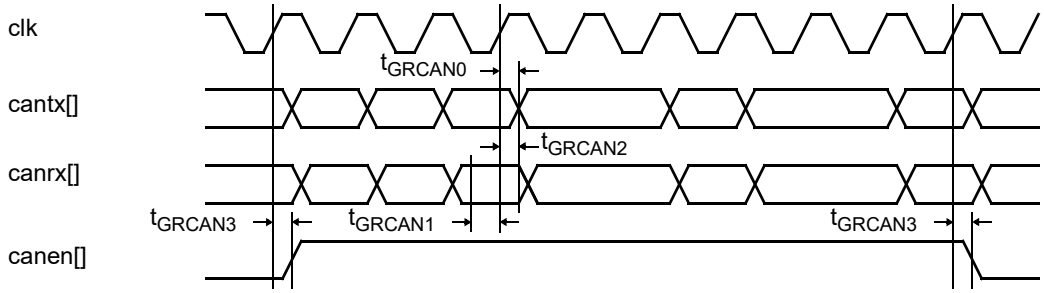


Figure 120. Timing waveforms

*Table 468.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{GRCAN0}	clock to data output delay	rising *clk* edge	-	TBD	ns
t_{GRCAN1}	data input to clock setup	rising *clk* edge	TBD	-	ns
t_{GRCAN2}	data input from clock hold	rising *clk* edge	TBD	-	ns
t_{GRCAN3}	clock to output delay	rising *clk* edge	-	TBD	ns

37.18 Library dependencies

Table 469 shows the libraries used when instantiating the core (VHDL libraries).

*Table 469.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	CAN	Signals, component	GRCAN component and signal declarations.

37.19 Instantiation

This example shows how the core can be instantiated.

```
library  ieee;
use      ieee.std_logic_1164.all;

library  gaisler;
use      gaisler.can.all;

entity example is
   generic (
      padtech:       in    integer := 0);
   port (
      -- CAN interface
      cantx:         out   std_logic_vector(1 downto 0);
      canrx:         in    std_logic_vector(1 downto 0);
      canen:         out   std_logic_vector(1 downto 0);

...

   -- Signal declarations
   signal   rstn:          std_ulogic;
   signal   clk:           std_ulogic;

   signal   ahbmo:         ahb_mst_out_vector := (others => ahbm_none);
   signal   ahbmi:         ahb_mst_in_type;

   signal   apbi:          apb_slv_in_type;
   signal   apbo:          apb_slv_out_vector := (others => apb_none);

   signal   cani0:         can_in_type;
   signal   cano0:         can_out_type;

...

   -- Component instantiation
   grcan0: grcan
      generic map (
         hindex         => 1,
         pindex         => 1,
         paddr          => 16#00C",
         pmask          => 16#FFC",
         pirq           => 1,
         txchannels     => 1,
         rxchannels     => 1,
         ptrwidth       => 16)
      port map (
         rstn           => rstn,
         clk            => clk,
         apbi           => apbi,
         apbo           => apbo(1),
         ahbi           => ahbmi,
         ahbo           => ahbmo(1),
         cani           => cani0,
         cano           => cano0);
```

```
cantx0_pad : outpad
   generic map (tech => padtech) port map (cantx(0), cani0.tx(0));

canrx0_pad : inpad
   generic map (tech => padtech) port map (canrx(0), cani0.rx(0));

canen0_pad : outpad
   generic map (tech => padtech) port map (canen(0), cani0.en(0));

cantx1_pad : outpad
   generic map (tech => padtech) port map (cantx(1), cani0.tx(1));

canrx1_pad : inpad
   generic map (tech => padtech) port map (canrx(1), cani0.rx(1));

canen1_pad : outpad
   generic map (tech => padtech) port map (canen(1), cani0.en(1));
```

38 GRCLKGATE / GRCLKGATE2X - Clock gating unit

38.1 Overview

The clock gating unit provides a means to save power by disabling the clock to unused functional blocks. The core provides a mechanism to automatically disabling the clock to LEON processors in power-down mode, and optionally also to disable the clock for floating-point units.

The core provides a register interface via its APB slave bus interface.

The clock gate unit has two main top-level units, GRCLKGATE and GRCLKGATE2X. GRCLKGATE2X exposes the full functionality and is the recommended top-level for new designs.

38.2 Operation

The operation of the clock gating unit is controlled through four registers: the unlock, clock enable, core reset and CPU/FPU override registers. The clock enable register defines if a clock is enabled or disabled. A '1' in a bit location will enable the corresponding clock, while a '0' will disable the clock. The core reset register allows to generate a reset signal for each generated clock. A reset will be generated as long as the corresponding bit is set to '1'. The bits in clock enable and core reset registers can only be written when the corresponding bit in the unlock register is 1. If a bit in the unlock register is 0, the corresponding bits in the clock enable and core reset registers cannot be written.

To gate the clock for a core, the following procedure should be applied:

1. Disable the core through software to make sure it does not initialize any AHB accesses
2. Write a 1 to the corresponding bit in the unlock register
3. Write a 0 to the corresponding bit in the clock enable register
4. Write a 0 to the corresponding bit in the unlock register

To enable the clock for a core, the following procedure should be applied

1. Write a 1 to the corresponding bit in the unlock register
2. Write a 1 to the corresponding bit in the core reset register
3. Write a 1 to the corresponding bit in the clock enable register
4. Write a 0 to the corresponding bit in the clock enable register
5. Write a 0 to the corresponding bit in the core reset register
6. Write a 1 to the corresponding bit in the clock enable register
7. Write a 0 to the corresponding bit in the unlock register

The clock gating unit also provides gating for the processor core and, optionally, floating-point units. A processor core will be automatically gated off when it enters power-down mode.

With the GRCLKGATE and GRCLKGATE2X units, any shared FPU will be gated off when all processor cores connected to the FPU have floating-point disabled or when all connected processor cores are in power-down mode.

With the GRCLKGATE2X unit it is also possible to support dedicated FPU clock gating. In this case a FPU will be gated off when processor core connected to the FPU has floating-point disabled or when the processor core is in power down mode.

Processor/FPU clock gating can be disabled by writing '1' to bit 0 of the CPU/FPU override register.

38.2.1 Shared FPU

For systems with shared FPU, a processor may be clock gated off while the connected FPU continues to be clocked. The power-down instruction may overtake a previously issued floating-point instruc-

tion and cause the processor to be gated off before the floating-point operation has completed. This can in turn lead to the processor not reacting to the completion of the floating-point operation and to a subsequent processor freeze after the processor wakes up and continues to wait for the completion of the floating-point operation.

In order to avoid this, software must make sure that all floating-point operations have completed before the processor enters power-down. This is generally not a problem in real-world applications as the power-down instruction is typically used in a idle loop and floating-point results have been stored to memory before entering the idle loop. To make sure that there are no floating-point operations pending, software should perform a store of the %fsr register before the power-down instruction.

38.3 Registers

The core's registers are mapped into APB address space.

Table 470. Clock gate unit registers

APB address offset	Register
0x00	Unlock register
0x04	Clock enable register
0x08	Core reset register
0x0C	CPU/FPU override register
0x10 - 0xFF	Reserved

38.3.1 Unlock register

*Table 471.*0x00 - UNLOCK - Unlock register

31 x+1	x 0
RESERVED	UNLOCK
0	0
r	rw

31: x+1 RESERVED

x: 0 Unlock clock enable and reset registers (UNLOCK) - The bits in clock enable and core reset registers can only be written when the corresponding bit in this field is 1.

38.3.2 Clock enable register

*Table 472.*0x04 - CLKEN - Clock enable register

31 x+1	x 0
RESERVED	ENABLE
0	*
r	rw

31: x+1 RESERVED

x: 0 Cock enable (ENABLE) - A ‘1’ in a bit location will enable the corresponding clock, while a ‘0’ will disable the clock.

38.3.3 Core reset register

Table 473. 0x08 - RESET - Reset register

31 x+1	x 0
RESERVED	RESET
0	0
r	rw

31: x+1 RESERVED

x: 0 Reset (RESET) - A reset will be generated as long as the corresponding bit is set to ‘1’.

38.3.4 CPU/FPU override register

Table 474. 0x0c - OVERRIDE - CPU/FPU override register

31 y+1	y 16	15 x+1	x 0
RESERVED	FOVERRIDE	RESERVED	OVERRIDE
0	0	0	0
r	rw	r	rw

31: y+1 RESERVED

y: 16 Override FPU clock gating (FOVERRIDE) - If bit n of this field is set to ’1’ then the clock for FPU n will be active regardless of the value of %PSR.EF. Only available if FPU clock is enabled at implementation.

15: x+1 RESERVED

x: 0 Override CPU clock gating (OVERRIDE) - If bit n of this field is set to ’1’ then the clock for processor n and FPU n will always be active.

38.4 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x02C. For description of vendor and device identifiers see GRLIB IP Library User’s Manual.

38.5 Implementation

38.5.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset for its internal registers.

38.5.2 Clock gate implementation

The clock gates are implemented using the CLKAND core in the techmap library, that instantiates the appropriate cell for the selected technology.

For ungated clocks, dummy clock gates are instantiated with the same technology but the isdummy generic set to 1. The technology mapping for the technology can decide whether to instantiate real clock gating cells for the technology or to pass the clock through as-is without any gating.

38.5.3 Scan test support

The test-enable signal is taken in through the APB input record and passed through to the techmap layer where it can be connected to the clock gating cell's test enable input or OR:ed into the normal enable if no test-enable input is available. Another alternative is to drive the cell's test enable input with constant 0 and hook it up to test-enable or scan-enable during the DFT implementation. Refer to the synthesis/DFT tools documentation for more details.

A separate ungate active-high input signal that also sets all clock gates to pass-through can be enabled in the core. This is passed in through the functional path.

38.5.4 Simulation

The underlying technology-specific gating in the techmap layer should ensure that all the gated and ungated clocks generated are delay and delta aligned to avoid zero-delay simulation problems. The standard solution is to add a 5 ps delay that gets removed on synthesis, however some technologies may use a different approach.

38.6 Configuration options

Table 475 shows the configuration options of the core (VHDL generics).

*Table 475.*Configuration options

Generic	Function	Allowed range	Default
tech	Clock/fabrication technology	0 to NTECH-1	0
pindex	Selects which APB select signal (PSEL) will be used to access the unit		
paddr	The 12-bit MSB APB address	0 to 16#FFF#	0
pmask	The APB address mask	0 to 16#FFF#	16#FFF#
ncpu	Number of processors that will connect to the unit	-	1
nclks	Number of peripheral units (clock/reset pairs) in addition to any processors and floating-point units that will connect to the unit.	0 - 31	8
emask	Bit mask where bit n (0 is the least significant bit) decides if a unit should be enabled (1) or disabled (0) after system reset.	0 - 16#FFFFFFFF#	0
extemask	If this generic is set to a non-zero value then the after-reset-enable-mask will be taken from the input signal epwen.	0 - 1	0
scantest	Enable scan test support	0 - 1	0

*Table 475.*Configuration options

Generic	Function	Allowed range	Default
edges	Extra clock edges provided by the clock gate unit after reset completes. CPUs get *edges* + 3 rising edges after reset and other cores get *edges* + 1 rising edges after system reset.	-	0
noinv	Do not use inverted clock for clock gate enable register. This generic can be set to one for technologies that have glitch free clock gates.	0 - 1	0
fpush	Selects FPU configuration 0: System has processors without, or with dedicated, FPUs 1: System has one FPU shared between all processors 3: System has one FPU for each parir of processors. (FPU0 is connected to CPU0 and CPU1, FPU1 is connected to CPU2 and CPU3, ...)	0 - 2	0
clk2xen	Enable double clocking. Only available on GRCLKGATE2X entity	0 - 1	1
ungateen	Enable separate ungate input for asynchronous un-gating of all clocks.	0 - 16#FFFFFFFF#	0
fpuclken	Enable separate clocks for FPU. Requires that generic *fpush* is set to 0. Only available on GRCLKGATE2X entity	0 - 1	0
nahbclk	Length of clkahb output vector Only available on GRCLKGATE2X entity	0 - 16#FFFFFFFF#	1
nahbclk2x	Length of clkahb2x output vector Only available on GRCLKGATE2X entity	0 - 16#FFFFFFFF#	1
balance	If balance is set to 1 then an always-enabled clock gate is inserted on each clkahb output. This option is obsolete as the techmap layer can now decide what to do with dummy clock gates, and only the value 1 is supported in the core.	1 - 1	1

38.7 Signal descriptions

Table 476 shows the interface signals of the core (VHDL ports).

*Table 476.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLKIN	N/A	Input	Clock	-
CLKIN2X	N/A	Input	Clock with higher frequency. Only present on GRCLKGATE2X entity.	-
PWD	N/A	Input	Power-down signal from processor cores	High
FPEN	N/A	Input	Floating-point enable signal from processor cores, only used in configurations with shared FPU when using the GRCLKGATE entity. For GRCLKGATE2X this input is also used when VHDL generic *fpuclken* is set to 1.	High
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
GCLK[nclks-1:0]	N/A	Output	Clock(s) to peripheral unit	-
RESET[nclks-1:0]	N/A	Output	Reset(s) to peripheral units	Low
CLKAHB[nahbclk**-1:0]	N/A	Output	Clock to non-gated units	-
CLKAHB2X[nahbclk2x**-1:0]	N/A	Output	2x Clock to non-gated units	-
CLKCPU[ncpu-1:0]	N/A	Output	Clock to processor cores	-
ENABLE[nclks-1:0]	N/A	Output	Enable signal(s) for peripheral units	High
CLKFPU[nfpu***:0]	N/A	Output	Clock to shared floating-point units, only used in configurations with shared FPU.	-
EPWEN	N/A	Input	External enable reset vector	High
UNGATE	N/A	Input	Ungate all clocks for test mode (only used if enabled in configuration)	High

* see GRLIB IP Library User's Manual

** Single output on GRCLKGATE entity, vector on GRCLKGATE2X entity.
*** where nfpu = (fpush/2)*(ncpu/2-1) for GRCLKGATE and (fpush/2+fpuclken)*(ncpu/(2-fpuclken)-1) for GRCLK-GATE2X

38.8 Library dependencies

Table 477 shows libraries used when instantiating the core (VHDL libraries).

*Table 477.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	MISC	Component	Component declaration

38.9 Instantiation

This example shows how the core can be instantiated.

```
clkg0: grclkgate
      generic map (
        tech     => fabtech,
        pindex   => 4,
        paddr    => 16#040#,
        pmask    => 16#fff#,
        ncpu     => CFG_NCPU,
```

```
    nclks    => NCLKS,
    emask    => 0,                -- Don't care
    extemask => 1,                -- Reset value defined by input vector (epwen below)
    scantest => scantest,
    edges    => CG_EDGES,
    noinv    => CG_NOINV,
    fpush    => CFG_GRFPUSH)
  port map(
    rst      => rstn,      -- from reset generator
    clkin    => ahb_clk,   -- from clock generator
    pwd      => pwd,  -- from processors, typically dsuo.pwd(CFG_NCPU-1 downto 0)
    fpen     => fpen, -- from processors, if shared FPU is used
    apbi     => apbi,
    apbo     => apbo(4),
    gclk     => gclk,      -- clock to (gated) peripheral cores
    reset    => grst,      -- reset to (gated) peripheral cores
    clkahb   => clkm,      -- clock to AMBA system (not gated)
    clkcpu   => cpuclk,    -- clock to processor cores
    enable   => clkenable, -- enable(n) signals that peripheral n is enabled
    clkfpu   => fpuclk,    -- clock to any shared FPU cores
    epwen    => pwenmask,  -- signal to set enable-after-reset
    ungate   => gnd);
```

39 GRDMAC - DMA Controller with internal AHB/APB bridge

39.1 Overview

The GRDMAC core provides a flexible direct memory access controller. The core can perform burst transfers of data between AHB and APB peripherals at aligned or unaligned memory addresses. The core can be instantiated with one or two AHB master interfaces to perform transfers among different AHB buses.

The core's configuration registers are accessible through an APB interface. Up to 16 DMA channels are supported. Each channel can be configured flexibly by means of two descriptor chains residing in main memory: a Memory to Buffer (M2B) chain and a Buffer to Memory (B2M) chain. Each chain is composed of a linked list of descriptors, where each descriptor specifies an AHB address and the size of the data to read/write, supporting a scatter/gather behavior.

Once enabled, the core will proceed in reading the descriptor chains, then reading memory mapped addresses specified by the M2B chain and filling its internal buffer. It will then write the content of the buffer back to memory mapped addresses by elaborating the B2M descriptor chain.

The core supports a simplified mode of operation, with only one channel. In this mode of operation only one descriptor is present for each of the M2B and B2M chains. These two descriptors are written directly in the core's register via APB.

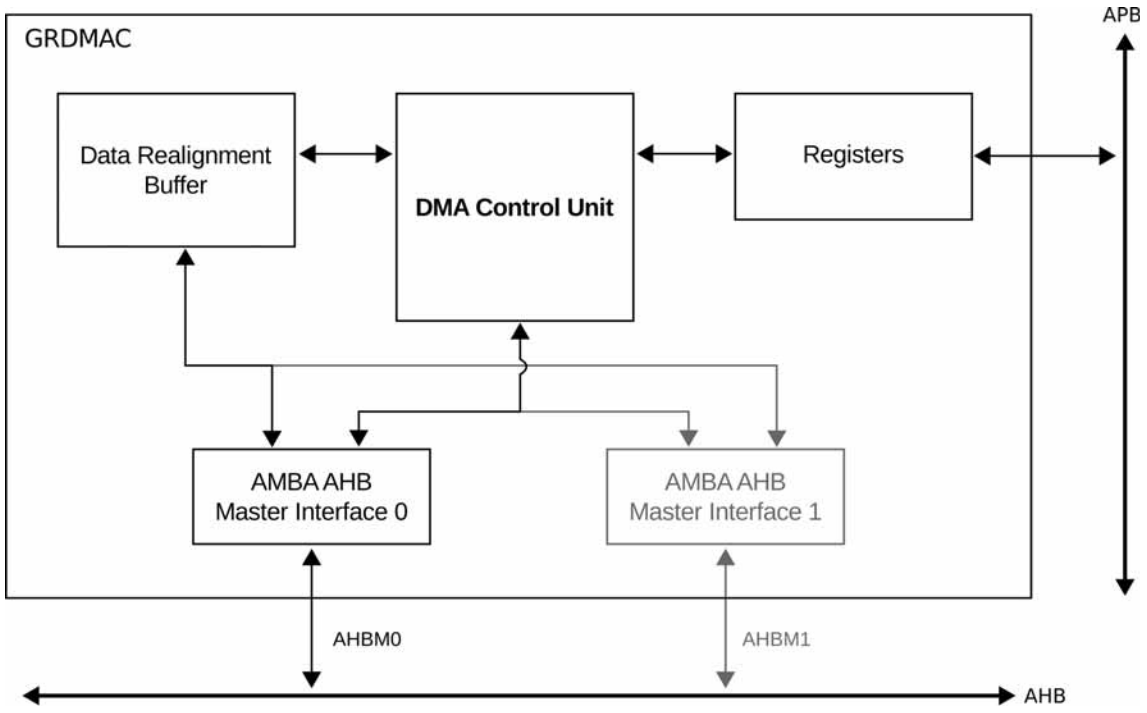


Figure 121. Block diagram

39.2 Configuration

The GRDMAC core consists of four main components: the DMA control unit, the AHB Master interface, the internal buffer with realignment support and an optional second AHB Master interface. The core supports being attached to any AHB bus with a data width of 32-bit, 64-bit or 128-bit. For every DMA channel the core will perform two types of DMA transfers through one of the AMBA AHB Master interfaces: from memory to the internal buffer (M2B) and from the internal buffer to memory (B2M). The core will read data from memory until its internal buffer is filled or until the M2B

descriptor chain is completed. When one of these two events is detected, GRDMAC will start writing the buffer content into memory, by switching to the B2M chain.

The internal buffer size is configurable through the generic *bufsize*. In case the buffer size is smaller that the total size of the M2B chain, the core will switch multiple times from the M2B chain to the B2M chain and vice versa.

The second AHB Master Interface is enabled by setting the *en_ahbm1* generic to 1. If the second interface is not enabled, all settings related to it will be ignored and the core will default to the main AHB Master Interface for all transfers.

39.2.1 Core setup

The GRDMAC core reads its configuration from any AHB mapped address (typically main memory) through its main AMBA AHB Master interface (AHBM0 if instantiated with support for two master interfaces). The core supports up to 16 DMA channels, a number configurable through the *ndmach* generic. For each channel, the M2B and B2M descriptor linked lists must be set up, and a pointer to the first descriptor in the two chains must be provided. These pointers are organized in a structure called Channel Vector. The Channel Vector is organized as in Table 478, below. For each of the GRDMAC channels there are two pointers: one pointer to the M2B descriptor linked list and one pointer to the B2M descriptor linked list. The Channel Vector array must be created at a 128-byte-aligned address. The GRDMAC core will read the Channel Vector entries for each channel up to *ndmach* channels.

*Table 478.*GRDMAC Channel Vector format

Address offset	Field
0x00	Channel 0: M2B descriptor pointer
0x04	Channel 0: B2M descriptor pointer
0x08	Channel 1: M2B descriptor pointer
0x0C	Channel 1: B2M descriptor pointer
...	...
...	...
0x78	Channel 15: M2B descriptor pointer
0x7C	Channel 15: B2M descriptor pointer

39.2.2 Descriptor types

Each descriptor consists of a four-field structure as provided in the tables below and must be created at a 16-byte-aligned address. There are three descriptor types: M2B descriptors, B2M descriptors and conditional descriptors.

The former two descriptors, categorized as data descriptors, are only allowed in the respective descriptor linked lists (M2B descriptor linked list and B2M descriptor linked list).

Conditional descriptors on the other hand, are required to be followed by a data descriptor, to which they bond to, and they can be specified in both the M2B and B2M descriptor linked lists. They are special descriptors that enable conditional behavior in a descriptor linked list and they are described in more detail in paragraph 39.3.2.

39.2.3 Data descriptors

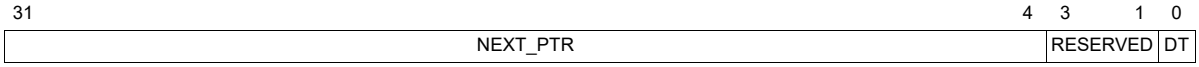
For data descriptors, the first field, the next_descriptor field, is the address of the next descriptor in the chain. The chain ends with a descriptor whose next_descriptor field is all zeroes (NULL pointer).

The second field of an M2B descriptor, the address field, defines the address to read the data from. It can be any address in the system, and there are no alignment requirements. The number of bytes to transfer from memory to the internal buffer is specified in the third field, the control field, as seen in the table below.

*Table 479.*GRDMAC M2B descriptor format

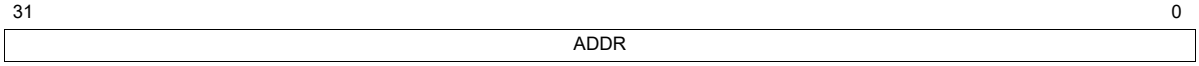
Address offset	Field
0x0	M2B next_descriptor
0x4	M2B address
0x8	M2B control
0xC	M2B status

Table 480. GRDMAC M2B descriptor next_descriptor field (address offset 0x00)



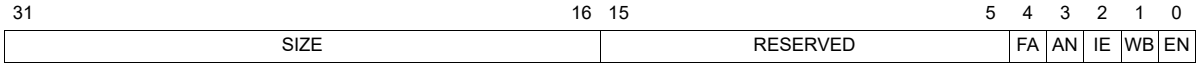
31: 4	M2B Next descriptor pointer address (NEXT_PTR) - MSb of 16 Byte aligned address of the next descriptor in the M2B descriptor chain or NULL.
0	M2B descriptor type (DT) - Descriptor type field, ‘0’ for data descriptors, ‘1’ for conditional descriptors. Must be set to ‘0’ for this type of descriptor.

Table 481. GRDMAC M2B descriptor address field (address offset 0x04)



31: 0	M2B Address (ADDR) - Starting address the core will read data from.

Table 482. GRDMAC M2B descriptor control field (address offset 0x08)



31: 16	M2B descriptor size (SIZE) - Size in Bytes of the data that will be fetched from the address specified in the M2B address register.
4	M2B descriptor Fixed Address (FA) - If set to ‘1’, the data will be fetched from the same address for the entire size of the descriptor transfer. This is useful when reading from IO peripheral registers in combination with a conditional descriptor. If set to ‘0’, normal operation mode is attained.
3	M2B descriptor AHB Master Interface Number (AN) - If set to ‘0’, the descriptor’s transfer will be performed by the main AHB Master Interface (AHBM0). If set to ‘1’, the descriptor’s transfer will be performed by the second AHB Master Interface (AHBM1). If this interface is not enabled by the configuration generic *en_ahbm1*, then the transfer will fall back to the main AHB Master Interface (AHBM0).
2	M2B descriptor Interrupt Enable (IE) - If set to one, an interrupt will be generated when the M2B descriptor is completed. Descriptor interrupt generation also depends on interrupt mask for channel 0 and global interrupt enable.
1	M2B descriptor write-back (WB) - If set to one, the descriptor’s status field will be written back in main memory after completion.
0	M2B descriptor Enable (EN) - If set to one, the descriptor will be enabled, otherwise it will be skipped and the next descriptor fetched from memory.

Table 483. GRDMAC M2B descriptor status field (address offset 0x0C)

31	3	2	1	0
RESERVED		E	S	C

2 M2B descriptor error (E) - If set to one, an error was generated during execution of the M2B descriptor. See error register for more information.

1 M2B descriptor status (S) - If set to one, the descriptor is being executed and running. Otherwise set to zero.

0 M2B descriptor completion (C) - If set to one, the descriptor was completed successfully.

For the B2M chain, the same holds true, with the exception of the address field, which specifies the address in main memory to write to.

*Table 484.*GRDMAC B2M descriptor format

Address offset	Field
0x0	B2M next_descriptor
0x4	B2M address
0x8	B2M control
0xC	B2M status

Table 485. GRDMAC B2M descriptor next_descriptor field (address offset 0x00)

31	4	3	1	0
NEXT_PTR		RESERVED		DT

31: 4 B2M Next descriptor pointer address (NEXT_PTR) - Address of the next descriptor in the B2M descriptor chain or NULL.

0 B2M descriptor type (DT) - Descriptor type field, ‘0’ for data descriptors, ‘1’ for conditional descriptors. Must be set to ‘0’ for this type of descriptor.

Table 486. GRDMAC B2M descriptor address field (address offset 0x04)

31	0
ADDR	

31: 0 B2M Address (ADDR) - Starting address the core will write data to.

Table 487. GRDMAC B2M descriptor control field (address offset 0x08)

31	16	15	5	4	3	2	1	0
SIZE		RESERVED		FA	AN	IE	WB	EN

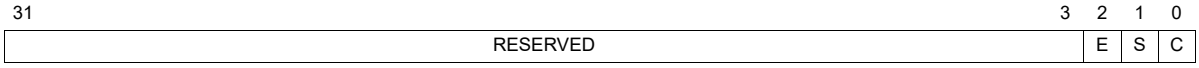
31: 16 B2M descriptor size (SIZE) - Size in Bytes of the data that will be written to the address specified in the B2M address register.

4 B2M descriptor Fixed Address (FA) - If set to ‘1’, the data will be fetched from the same address for the entire size of the descriptor transfer. This is useful when writing to IO peripheral registers in combination with a conditional descriptor. If set to ‘0’, normal operation mode is attained.

Table 487. GRDMAC B2M descriptor control field (address offset 0x08)

3	B2M descriptor AHB Master Interface Number (AN) - If set to '0', the descriptor's transfer will be performed by the main AHB Master Interface (AHBM0). If set to '1', the descriptor's transfer will be performed by the second AHB Master Interface (AHBM1). If this interface is not enabled by the configuration generic *en_ahbm1*, then the transfer will fall back to the main AHB Master Interface (AHBM0).
2	B2M descriptor Interrupt Enable (IE) - If set to one, an interrupt will be generated when the B2M descriptor is completed. Descriptor interrupt generation also depends on interrupt mask for channel 0 and global interrupt enable.
1	B2M descriptor write-back (WB) - If set to one, the descriptor's status field will be written back in main memory after completion.
0	B2M descriptor Enable (EN) - If set to one, the descriptor will be enabled, otherwise it will be skipped and the next descriptor fetched from memory.

Table 488. GRDMAC B2M descriptor status field (address offset 0x0C)



2	B2M descriptor error (E) - If set to one, an error was generated during execution of the B2M descriptor. See error register for more information.
1	B2M descriptor status (S) - If set to one, the descriptor is being executed and running. Otherwise set to zero.
0	B2M descriptor completion (C) - If set to one, the descriptor was completed successfully.

If a descriptor's write-back bit in its control field is set to one, the descriptor's status field will be written back to memory after completion. The transfer uses the AMBA AHB Master interface of the core.

39.2.4 Conditional descriptors

A conditional descriptor is a special kind of descriptor which bonds to a data descriptor and provides additional conditional behavior to it. A conditional descriptor can be used to create a DMA channel that retrieves data from IO cores, therefore off loading the CPU from the task. Usually IO cores provide a status register or an interrupt line to notify the CPU of the availability of new data. A conditional descriptor can be set up to poll this status register or to be triggered by an interrupt, signaling for instance, the availability of new data. Once data is available, the bond data descriptor is executed, accumulating the data in the internal buffer of the DMA core, before bursting it to memory for the software to handle it.

There are, hence, two kinds of conditional descriptors: polling conditional descriptors or triggering conditional descriptors. The former kind will continuously poll an address for data, and once a termination condition on the retrieved data is met, will yield to the data descriptor. The latter kind will instead have the core entering a state where it waits for a monitored input signal line to trigger. When the monitored input line is sampled to a value of '1', the data descriptor will be executed.

To set up a triggering conditional descriptor, the IT bit field in the descriptor's control field needs to be set to '1'. Bits 5:0 of the conditional address/triggering line field will specify which of the 64 input lines of the IRQ_TRIG signal will be monitored. During the execution of the triggering conditional descriptor, the triggering line is monitored every clock cycle, and when the value of the line is '1', the conditional execution will terminate and the data descriptor will be yield, fetching COND_SIZE bytes before going back to executing the conditional triggering. The data descriptor will be considered completed when all the bytes from the data descriptor, specified in the SIZE field, have been transfered, in amounts of COND_SIZE at each triggering. If the *timer_en* VHDL configuration generic is set to '1', an optional timeout counter can be enabled during the triggering conditional descriptor execution. By setting the TE bit field in the core's control register to '1' and by setting the Timer Reset Value Register to the required number of clock cycles, the descriptor execution is halted with a Timeout Error if

an interrupt is not received before the timer expires. The error halts the channel execution after eventual descriptor write-back is performed.

To set up a polling conditional descriptor, the IT bit field in the descriptor's control field needs to be set to '0'. Bits 31:0 of the conditional address/triggering line field will point to the address that the DMA core will poll for data until the termination condition is TRUE. The condition is specified as the bitwise AND between the 32-bit word pointed by COND_ADDR and the COND_MASK. This value is compared to 0 according to the following formulas, according to the termination condition type selected in the conditional control field (CT).

Table 489. GRDMAC Conditional descriptor Termination condition type 0

$$(*\text{COND\_ADDR} \wedge \text{COND\_MASK}) = 0$$

Table 490. GRDMAC Conditional descriptor Termination condition type 1

$$*\text{COND\_ADDR} \wedge \text{COND\_MASK} \neq 0$$

When the condition is TRUE, the conditional descriptor will stop polling and will proceed with fetching COND_SIZE bytes from the data descriptor pointed by NEXT_PTR. The behavior of conditional descriptors is explained in depth in paragraph 39.3.2.

Also in paragraph 39.3.2 is an example configuration of a conditional DMA channel for UART reading.

*Table 491.*GRDMAC Conditional descriptor format

Address offset	Field
0x0	Conditional next_descriptor
0x4	Conditional address/triggering line
0x8	Conditional control
0xC	Conditional mask

Table 492. GRDMAC Conditional descriptor next_descriptor field (address offset 0x00)

31	4	3	1	0
NEXT_PTR		RESERVED		DT

31: 4	Conditional Next descriptor pointer address (NEXT_PTR) - Address of the data descriptor in the descriptor chain which the conditional descriptor is bond to. Cannot be NULL.
0	Conditional descriptor type (DT) - Descriptor type field, '0' for data descriptors, '1' for conditional descriptors. Must be set to '1' for this type of descriptor.

Table 493. GRDMAC Conditional descriptor address field (address offset 0x04)

31	6	5	0
COND_ADDR[31:6]		COND_ADDR[5:0] / IRQN	

Table 493. GRDMAC Conditional descriptor address field (address offset 0x04)

31: 0	Conditional Address (COND_ADDR) - Address of the 32-bit word the core will read for the conditional termination expression matching.
5: 0	IRQ Trigger Line Number (IRQN) - Index of the IRQ_TRIG signal input vector which is used as the triggering line for triggered conditional descriptors, 0 to 63.

Table 494. GRDMAC Conditional descriptor control field (address offset 0x08)

31 16	15 4	3	2	1	0
COND_SIZE	COUNTER_RST	AN	CT	IT	EN

31: 16	Conditional descriptor total size (COND_SIZE) - Total size in Bytes of the data that will be fetched from the bond data descriptor each time the conditional termination expression matches to true.
15: 4	Conditional descriptor counter reset value (COUNTER_RST) - Reset value of the conditional counter timer that is executed before every polling or triggering. The unit is number of clock cycles and the purpose is to provide a timer between polling requests onto the AMBA AHB bus with enough clock cycles in order not to clog the bus.
3	Conditional descriptor AHB Master Interface Number (AN) - If set to ‘0’, the descriptor’s transfer will be performed by the main AHB Master Interface (AHBM0). If set to ‘1’, the descriptor’s transfer will be performed by the second AHB Master Interface (AHBM1). If this interface is not enabled by the configuration generic *en_ahbm1*, then the transfer will fall back to the main AHB Master Interface (AHBM0).
2	Conditional descriptor Termination Condition type (CT) - If the conditional descriptor is of type “polling”, this bits specifies which type of termination condition is used. If ‘0’, the termination condition is of type 0 as specified in this paragraph. If ‘1’, the termination condition is of type 1.
1	Conditional Descriptor Irq Trigger (IT) - If set to ‘1’, the conditional descriptor will wait for the input interrupt line to go high before executing the bond data descriptor. The selected interrupt line is the one indexed by IRQN in the IRQ_TRIG signal input vector. This bit enables triggering behavior of conditional descriptors. If this bit is set to ‘0’, normal polling behavior with termination condition is enabled.
0	Conditional descriptor Enable (EN) - If set to one, the descriptor will be enabled, otherwise it will be skipped and the next descriptor fetched from memory.

Table 495. GRDMAC Conditional descriptor mask field (address offset 0x0C)

31 0
COND_MASK

31: 0	Conditional Mask (COND_MASK) - Bit mask used in the conditional descriptor termination condition matching.

39.2.5 Register setup

Once the channel vector and the relative descriptor chains are setup in main memory, the GRDMAC register must be also setup. The 128-byte-aligned address, where the Channel Vector resides, must be written in the Channel Vector Pointer register. The control register must also be setup. Once the enable bit of the control register is set to one, the core will start running and will execute all the channels which are enabled.

39.3 Operation

39.3.1 Normal mode of operation

In normal mode of execution, GRDMAC will start executing all the enabled channels until they are complete or an error is generated.

When executing a DMA channel, the core will initially fetch the two descriptor pointers from the address provided in the CVP register which are relative to the channel. It will then fetch the first M2B and B2M descriptors from main memory. The M2B descriptor chain is then executed until either the internal buffer is full, or the M2B chain is completed. If one of this events happen, the core will switch to the B2M descriptor chain. The B2M chain will switch back to the M2B chain when the buffer is empty. The DMA channel is marked complete when the last descriptor in the B2M chain is executed, finally emptying the buffer.

During the execution of a chain, the core will fetch a new descriptor after the successful completion of the previous one, following the pointers in the linked list. When the core reaches a NULL pointer in the M2B chain, it will switch to the B2M chain. When it reaches a NULL pointer in the B2M chain, the core will update the DMA channel status and switch to the next enabled DMA channel, until all the channels are completed.

39.3.2 Operation with conditional descriptors

Conditional descriptors bond to the following data descriptor in the linked list and provide conditional behavior to the execution of the data descriptor. During the execution of a DMA channel, when the core fetches a conditional descriptor from memory, it will proceed and fetch the following descriptor in the chain as well, which must be a data descriptor.

After the descriptors' pair has been fetched, the conditional execution will follow these steps:

a) the core will execute the conditional counter, down counting for COUNTER_RST clock cycles

b) if the conditional descriptor is a polling descriptor, go to step **c1**, if it's a triggering descriptor, go to step **c2**.

c1) the core will fetch a 32-bit word at the COND_ADDR address.

d1) if the conditional termination condition of Table 490 is *false* then the core will go back to step **a,** if the conditional termination condition of Table 490 is *true*, the core will fetch a portion of the data from the data descriptor which is COND_SIZE bytes, then go back to step **a**.

c2) the core will monitor line IRQN of the IRQ_TRIG input signal, indefinitely or until the trigger counter expires.

d2) when the monitored line has a value of '1', the core will fetch a portion of the data from the data descriptor which is COND_SIZE bytes, then go back to step **a**.

The total SIZE of the bond data descriptor will be decremented by COND_SIZE bytes every time the bond data descriptor is executed, and the ADDRESS will be incremented by the same amount (unless the FA flag is set).

The FA (Fixed Address) bit field in the data descriptor control field is useful when accessing data to/from a peripheral data register, i.e. UART data register, when you need to read/write always from/to the same address.

The execution of the descriptor pair (conditional and bond data descriptors) ends when the SIZE field of the data descriptor reaches 0. In other words, the execution ends when SIZE bytes have been fetched in total from the data descriptor, by fetching COND_SIZE byte amounts every time the conditional condition (polling or triggering) is true.

39.3.3 Simplified mode of operation

In Simplified Mode of Operation, the GRDMAC core configuration resides entirely in its configuration registers and the Channel Vector structure is not used. The core will not perform any memory access to fetch configuration data. This mode of operation makes use of only two data descriptors, respectively one descriptor for M2B transfers and one for B2M transfers. Conditional descriptors are not supported in this mode. The descriptors are written directly onto GRDMAC via APB at offsets 0x20 and 0x30. Their next_descriptor field is hardwired to zeroes. Their status is always written-back to their relative descriptor status register.

When the core is configured in Simplified mode of operation, the relative bit (SM) must be set to one in the control register. The core will execute the two internal descriptors on channel zero. Channel zero must therefore be enabled, and the core status can be read on channel zero's status bits in the status register.

39.4 AHB transfers

For every descriptor executed, GRDMAC will perform an AHB data transfer at the address and of the size specified. The AHB accesses that it can perform are up to 128-bit wide and can be at aligned or unaligned memory addresses. The maximum AHB access width depends on the AHB bus width and on the *busw* and *wbmask* generics, as described in paragraph 39.7.

The core will perform unaligned memory access if defined by the descriptors. It will perform byte (8 bit) accesses at byte-aligned addresses, half-word (16 bit) accesses at half-word aligned addresses, and so on. The core will perform burst transfers of the maximum supported width for as long as possible according to the total transfer size. For example, if the maximum supported bus width for one transfer is 64-bit, and a descriptor requests 18 bytes at address 0x40000006, the core will perform one 16-bit half-word access, and one two-beat burst of double words. In some cases, the total transfer size might require GRDMAC to perform additional word, half-word and/or byte accesses at the end of the transfer. The burst accesses performed by GRDMAC are of type incrementing burst of unspecified length. These bursts will never cross a 1KB memory boundary, or a smaller boundary that can be set with the generic *burstbound*. At the specified memory boundary set by *burstbound*, the burst will be interrupted, an idle cycle will be inserted and the incrementing burst of unspecified length will restart from the next address. This generic can be used to limit the maximum burst length performed by the core, making re-arbitration on the AHB bus more frequent.

When the core is configured with the VHDL generic *en_ahbm1* set to '1', a secondary AHB Master interface will be instantiated inside the GRDMAC core. This interface can be connected to a second AHB bus to provide bridging capabilities to the DMA controller. The core will fetch data from this interface when the AN flag in the descriptor's control field is set accordingly. This flag will be ignored in case the core is configured with the *en_ahbm1* VHDL generic set to '0'.

39.5 Data realignment buffer

The realignment buffer is the data buffer used internally by the GRDMAC core. The component allows the core to store the data in a tightly packed way, being optimized to store AMBA AHB transfer data of different size and at different address offsets.

The internal buffer uses RAM implemented using GRLIB parameterizable SYNCRAMBW memories, assuring portability to all supported technologies. Internally two SYNCRAMBW are used, one for even words and one for odd words. The total number of RAMs used depends on the *bufsize* generic, and its minimum size is two words, 8 bytes. To control the implementation technology of the internal RAMs, the technology mapping generic *memtech* may be used. Additionally, the generic *testen* will be propagated to the SYNCRAMBW and is used to enable scan test support.

Fault tolerance can be added to the RAM by setting the *ft* generic to a value different than 0. To obtain byte parity DMR memories, set the *ft* generic to 1. To use TMR set it to 2. Note that the *ft* generic needs to be set to 0 unless the core is used together with the fault tolerant version of GRLIB, which is not available under the terms of the GPL.

39.6 Interrupts

GRDMAC provides fine-grained control of interrupt generation. At the highest level, the global Interrupt Enable bit (IE) in the control register can be set to zero to mask every interrupt setting in the core. If set to one, interrupt generation depends on the following settings.

The Interrupt on Error Enable bit (IEE) in the control register provides a way to generate interrupts in the event of errors. Error generation is discussed further in the next paragraph.

An interrupt can be also generated by the successful completion of a descriptor, if the Interrupt Enable (IE) bit is set to one in the descriptor's control field. The Interrupt Mask bit (Ix) in the Interrupt Mask register can be set to zero to mask all the descriptor completion interrupts. If descriptor write-back is enabled, the interrupt will be generated after writing back the descriptor's status in main memory.

For both interrupts on error and interrupts on descriptor completion events, a flag will be raised in the interrupt flag register at the bit corresponding to the channel where the interrupt event happened (IFx).

As an example of interrupt generation setup, one can enable interrupt on channel completion by performing the following steps. The Interrupt Enable (IE) bit in GRDMAC control register must be set to one, as must be the relevant channel's interrupt mask bit in the Interrupt mask register. Finally the Interrupt Enable (IE) bit in the control field of the last descriptor in the B2M chain of the channel must be set to one, while the same field must be set to zero in every other descriptor in the channel. This way, when the last descriptor in the buffer to memory chain is completed successfully, an interrupt will be generated.

39.7 Wide Data Bus support

The size of AMBA accesses supported through GRDMAC's AHB master interfaces depends on the maximum bus width and if the accessed memory area has been marked as being on the wide bus.

The generic *wbmask* is treated as a 16 bit mask where every bit represents a 256 MiB block of memory, with the least significative bit representing the range 0 - 0x10000000. If the corresponding bit is set to one, GRDMAC with perform wide accesses to that memory area. The size of the accesses is controlled with the *busw* generic. If the generic is set to 0, only 32 bit accesses will be performed.

Furthermore, the size of the AHB accesses can be limited with the Transfer Size Limit (TSL) field in the control register of GRDMAC. If the field is set to 1, the core will limit its maximum AHB transfer size to 32 bits. If it is set to 2, the limit will be 64 bits, and if it is set to 3, the limit will be 128 bits. The field must be interpreted as an upper limit on the transfer size and is subject to the *wbmask* and *busw* generic.

39.8 Errors

Four types of errors can be generated by GRDMAC. Transfer errors, descriptor errors, Channel Vector Pointer errors, conditional errors and timeout errors, as defined in the Error Register.

Transfer errors are generated when the core is accessing DMA data from and to memory and it encounters an AMBA AHB ERROR response. When a transfer error occurs on a descriptor which has the write-back flag enabled, the descriptor status will be written back to main memory with the error field set to one. An eventual interrupt will be generated only after the write back.

Descriptor errors are generated when an ERROR response is received while reading or writing back a descriptor in main memory.

Channel Vector Pointer errors are generated when the core receives an ERROR response when accessing the Channel Vector data structure in main memory.

Conditional errors are generated when a conditional polling descriptor encounters a problem during an AHB polling operation such as an ERROR response.

Finally timeout errors are caused by the timeout counter expiring before receiving an interrupt during triggered conditional descriptor execution. This requires the *timer_en* VHDL configuration generic to be set to '1' and the TE bit field in the control register to be configured to '1' during execution.

The core will enable the corresponding error type bit in the error register in addition to the error flag bit (E). The channel number where the error happened can be also read directly from the channel error field (CHERR) of the error register. Additionally an interrupt will be generated if the Interrupt on Error Enable bit (IEE) and the global Interrupt Enable (IE) bit in GRDMAC control register are set to one, and a flag will be raised in the interrupt flag register bit corresponding to the channel where the error event occurred (IFx).

39.9 Internal Buffer Readout Interface

In case of an error, the execution of the DMA channels will halt and the error will be reported as described in the previous session. It can happen that data that has been accumulated in the internal buffer during the M2B chain transactions, is not written out as part of the B2M chain, due to the channel halting. This internal data can still be read via the APB interface of the GRDMAC core, through the Internal Buffer Readout Interface memory area. The memory area is located at offset 0x800 to 0xFFF of the GRDMAC core memory address, totaling 2 KiB of accessible Internal Buffer space, as seen in Table 496. This area can only be read when the core is in an idle state and bit flag EN of the Control Register is set to '0'. The amount of valid data in the internal buffer can be inferred by reading the read pointer and write pointers to the buffer from the Internal Buffer Pointers Register (offset 0x40).

39.10 Endianness

The core is designed for big-endian systems.

39.11 Registers

The core is programmed through registers mapped into APB address space. The APB address is configured with the *paddr* and *pmask* generics. If the core is instantiated with the internal AHB/APB bridge, the *haddr* and *hmask* generics will configure the APB address space.

*Table 496.*GRDMAC controller registers

APB address offset	Register
0x00	Control register
0x04	Status register
0x08	Interrupt mask register
0x0C	Error register
0x10	Channel Vector Pointer
0x14	Timer Reset Value register
0x18	Capability register
0x1C	Interrupt flag register
0x20	Reserved
0x24	M2B Descriptor Address register*
0x28	M2B Descriptor Control register*
0x2C	M2B Descriptor Status register*
0x30	Reserved
0x34	B2M Descriptor Address register*
0x38	B2M Descriptor Control register*
0x3C	B2M Descriptor Status register*
0x40	Internal Buffer Pointers Register
0x800-0xFFF	Internal Buffer Readout Area

*Only used in Simplified Mode of Operation

39.11.1 Control Register

*Table 497.*GRDMAC control register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15 12	11 6	5	4	3	2	1	0
EF	EE	ED	EC	EB	EA	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0	TSL	RESERVED	TE	SM	IEE	IE	RS	EN
NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR		0	NR	NR	NR	0	0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		*	rw	rw	rw	rw	rw

31: 16 Enable channel x (Ex) - Set to one to enable DMA channel x, from 0 to 15.

15 12 Transfer Size limit (TSL) - If set to 1, the GRDMAC core will limit its maximum transfer size to 32b accesses. If set to 2, it will limit the transfer size to 64 bits. If set to 3, it will limit the maximum transfer size to 128 bit. If set to 0 no limit is imposed. The maximum transfer size is controlled by the *wbmask* and *busw* generics.

5 Timer Enable (TE) - Set to '1' to enable the timeout timer during triggered conditional descriptor execution. If the *timer_en* generic is set to '1', the field is rw, read-only otherwise.

4 Simplified mode (SM) - Set to one to use the core in simplified mode of operation

3 Interrupt enable for Errors (IEE) - Set to one to enable interrupt generation on error. Interrupt generation on error depends on the global Interrupt Enable (IE).

2 Interrupt Enable (IE) - Global Interrupt Enable. If set to zero, no interrupt will be generated. If set to one, interrupts from errors, descriptor completion, won't be masked.

1 Reset (RS) - Resets the core register if set to one.

0 Enable/Run (EN) - When set to one, the core will be enabled and start running.

39.11.2 Status Register

*Table 498.*GRDMAC status register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SF	SE	SD	SC	SB	SA	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0	CF	CE	CD	CC	CB	CA	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

31: 16 Status of channel x (Sx) - Set to one if DMA channel x is running, set to zero otherwise.

15: 0 Completion of channel x(Cx) - Set to one if DMA channel x has completed successfully, zero otherwise.

39.11.3 Interrupt Mask

*Table 499.*GRDMAC Interrupt Mask

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
																IF	IE	ID	IC	IB	IA	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
																NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR
																rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15: 0 Interrupt Mask for channel x (Ix) - Set to 0 to mask descriptor interrupt generation from channel x. Interrupt generation depends on the global Interrupt Enable in the control register.

39.11.4 Error Register

*Table 500.*GRDMAC error register

31 20	19 16	15 6	5	4	3	2	1	0
RESERVED	CHERR	RESERVED	ME	OE	TE	DE	CE	E
			0	0	0	0	0	0
	r		wc	wc	wc	wc	wc	wc

19: 16 Channel error (CHERR) - Channel number where last error was generated.

5 Timeout Error (ME) - One if the last generated error was of type timeout error. This field is cleared by writing a one to it.

4 Conditional Error (OE) - One if the last generated error was of type conditional execution error. This field is cleared by writing a one to it.

3 Transfer Error (TE) - One if the last generated error was of type transfer error. This field is cleared by writing a one to it.

2 Descriptor Error (DE) - One if the last generated error was of type descriptor error. This field is cleared by writing a one to it.

1 CVP Error (CE) - One if the last generated error was of type CVP error. This field is cleared by writing a one to it.

0 Error (E) - If set to one, an error was generated by the entity. This field is cleared by writing a one to it.

39.11.5 Channel Vector Pointer

*Table 501.*GRDMAC Channel Vector Pointer

31 7	6 0
CVP	RESERVED
NR	
rw	

31: 7 Channel Vector Pointer (CVP) - 128 Byte aligned memory address pointing to the vector of up to 16 couples of descriptor chain pointers.

39.11.6 Timer Reset Value Register

*Table 502.*GRDMAC Timer Reset Value Register

31 0
TIMER_RST
0x00000000
*

31: 0 Timer Reset Value (TIMER_RST) - Reset value for the triggered conditional descriptor timeout timer. If the *timer_en* generic is set to '1', the field is rw, read-only otherwise.

39.11.7 Capability Register

*Table 503.*GRDMAC capability register

31 16	15 12	11	10 9	8	7 4	3 0
BUFSZ	RESERVED	TT	FT	H1	NCH	VER
*		*	*	*	*	*
r		r	r	r	r	r

31: 16 Buffer size (BUFSZ) - Binary logarithm of the internal buffer size of the entity.

11 Timer (TT) - If set to '1', the timeout timer is enabled.

*Table 503.*GRDMAC capability register

10: 9		Fault Tolerant buffer (FT) - These bits indicate if the internal buffers in the core is implemented with fault tolerance. When 0, no fault tolerance, when 1, byte parity DMR, when 2, TMR. Reflects the VHDL generic ft.
	8	Second AHB Master (H1) - If set to one, the second AHB master interface (AHBM1) is enabled.
7:	4	Channel Number (NCH) - The maximum number of supported DMA channels in the core is NCH+1.
3:	0	Version (VER) - GRDMAC version number.

39.11.8 Interrupt Flag Register

*Table 504.*GRDMAC interrupt flag register

31 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	IFF	IFE	IFD	IFC	IFB	IFA	IF9	IF8	IF7	IF6	IF5	IF4	IF3	IF2	IF1	IF0
	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR
	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15: 0 Interrupt flag for channel x (IFx) - When set to one, an interrupt event (descriptor completion or error) was generated on channel x. This field is cleared by writing a one to it.

39.11.9 M2B Descriptor Address Register*

*Table 505.*GRDMAC M2B descriptor address register*

31 0
ADDR
NR
rw

31: 0 M2B Address (ADDR) - Starting address the core will read data from.

39.11.10M2B Descriptor Control Register*

*Table 506.*GRDMAC M2B descriptor control register*

31 16	15 3	2	1	0
SIZE	RESERVED	IE	R	EN
NR		NR		NR
rw		rw		rw*

31: 16 M2B descriptor size (SIZE) - Size in Bytes of the data that will be fetched from the address specified in the M2B address register.

2 M2B descriptor Interrupt Enable (IE) - If set to one, an interrupt will be generated when the M2B descriptor is completed. Descriptor interrupt generation also depends on interrupt mask for channel 0 and global interrupt enable.

0 M2B descriptor Enable (EN) - Set to one when the descriptor is written the first time. Write value ignored.

39.11.11 M2B Descriptor Status Register*

*Table 507.*GRDMAC M2B descriptor status register*

31 3	2	1	0
RESERVED	E	S	C
	0	0	0
	rw	rw	rw

2 M2B descriptor error - If set to one, an error was generated during execution of the M2B descriptor. See error register for more information.

1 M2B descriptor status (S) - If set to one, the descriptor is being executed and running. Otherwise set to zero.

0 M2B descriptor completetion (C) - If set to one, the descriptor was completed successfully.

39.11.12 B2M Descriptor Address Register*

*Table 508.*GRDMAC B2M descriptor address register*

31 0
ADDR

*Table 508.*GRDMAC B2M descriptor address register*

NR
rw

31: 0 B2M Address (ADDR) - Starting address the core will write data to.

39.11.13 B2M Descriptor Control Register*

*Table 509.*GRDMAC B2M descriptor control register*

31 16	15 3	2	1	0
SIZE	RESERVED	IE	R	EN
NR		NR		NR
rw		rw		rw*

31: 16 B2M descriptor size (SIZE) - Size in Bytes of the data that will be written to the address specified in the B2M address register.

2 B2M descriptor Interrupt Enable (IE) - If set to one, an interrupt will be generated when the B2M descriptor is completed. Descriptor interrupt generation also depends on interrupt mask for channel 0 and global interrupt enable.

0 B2M descriptor Enable (EN) - Set to one when the descriptor is written the first time. Write value ignored.

39.11.14 B2M Descriptor Status Register*

*Table 510.*GRDMAC B2M descriptor status register*

31 3	2	1	0
RESERVED	E	S	C
	0	0	0
	rw	rw	rw

2 B2M descriptor error - If set to one, an error was generated during execution of the B2M descriptor. See error register for more information.

1 B2M descriptor status (S) - If set to one, the descriptor is being executed and running. Otherwise set to zero.

0 B2M descriptor completion (C) - If set to one, the descriptor was completed successfully.

39.11.15 Internal Buffer Pointers Register

*Table 511.*GRDMAC internal buffer pointers register*

31 16	15 0
READ_P	WRITE_P
0	0
r	r

31: 16 B2M Internal Buffer Read Pointer (READ_P)- Points to the last offset in the internal buffer which was correctly read by the core and output on the bus.

15: 0 B2M Internal Buffer Write Pointer (WRITE_P) - Points to the last offset in the internal buffer which was correctly written by the core as an input from the bus.

*Register used only when the core is set to work in Simplified mode of operation.

39.12 Example DMA channel set-up

In this example a single DMA channel will be set-up, using conditional descriptors, to gather data from the UART core (APBUART) and write it into main memory.

The GRDMAC core is configured with its register address-space starting at address 0xCCC00200 and main memory starts at 0x40000000. The APBUART core's register is mapped at 0xCCC00100 and the UART receiver FIFO queue is configured as 4 bytes.

The DMA channel will need two descriptors in the M2B chain: a conditional descriptor bound to a data descriptor. The B2M chain will only need one data descriptor.

The conditional descriptor will poll the UART status register, mapped at 0xCCC00104, and will use the mask 0x00000100 for the termination condition. This mask will be ANDed with the status register, and the result of this operation will only show the value of the "Receiver FIFO half-full" field in the status register. This will enable the conditional register to stop polling when this bit becomes '1'. At this point the data descriptor will be executed for the amount of bytes specified in the conditional descriptor, which in this case is 1 bytes (half of the FIFO size). For the data transfer to read and accumulate correct data, the core must perform a single-byte access. The UART data register contains only one byte of relevant data. The size limit per transfer is therefore 1 byte and the address is marked as fixed, so the core will not increment it after every transfer.

The polling counter for the conditional descriptor is set according to the UART speed. If the UART baud rate is 38.4K and the system frequency is 100 MHz, one can assume that there is going to be 1 Byte available in the UART every 26k clock cycles. Setting the polling period to a value less than 26K will let the DMA get all the characters from the UART without missing any. The conditional counter reset value is set to its maximum, a period of 4095 clock cycles (0xFFF).

The polling will restart after the last read and the transfers will go on until the total size specified in the SIZE field of the data descriptor is reached. At this point the M2B chain is completed and the core will proceed with the B2M chain, emptying the contents of its buffer into memory, at the address specified.

Table 512 shows the memory layout of the system with the required data to set-up this example. Note that the Channel Vector is 128-byte aligned and the descriptors are 16-byte aligned,

Table 512. Memory Content

Address	Data	Description
0x40000080	0x40020010	Channel Vector - Channel 0 M2B descriptor chain pointer
0x40000084	0x40020040	Channel Vector - Channel 0 B2M descriptor chain pointer
...	...	
0x40020010	0x40020031	M2B conditional descriptor 0 - next descriptor pointer (lsb set to 1 for cond. desc.)
0x40020014	0xCCC00104	M2B conditional descriptor 0 - address (UART status register address)
0x40020018	0x0001FFF1	M2B conditional descriptor 0 - control (poll every 4095 cycles, get 1 Byte)
0x4002001C	0x00000080	M2B conditional descriptor 0 - mask (only check “Receiver FIFO half-full”)
...	...	
0x40020030	0x00000000	M2B data descriptor 0 - next descriptor pointer (NULL, end of chain)
0x40020034	0xCCC00100	M2B data descriptor 0 - address (UART data register address)
0x40020038	0x04000011	M2B data descriptor 0 - control (1024 Bytes from fixed address)
0x4002003C	-	M2B data descriptor 0 - status (written by core)
...	...	
0x40020040	0x00000000	B2M data descriptor 0 - next descriptor pointer (NULL, end of chain)
0x40020044	0x40030000	B2M data descriptor 0 - address (DMA write address for UART data)
0x40020048	0x04000001	B2M data descriptor 0 - control (1024 Bytes)
0x4002004C	-	B2M data descriptor 0 - status (written by core)
...	...	
0x40030000	-	UART data written by the DMA core
...	...	
0xCCC00200	0x0001000C	GRDMAC Control register
0xCCC00204	-	GRDMAC Status register (updated by the DMA core)
0xCCC00208	0x00000001	GRDMAC interrupt mask register
0xCCC0020C	-	GRDMAC error register (updated by the DMA core)
0xCCC00200	0x40000080	GRDMAC channel vector pointer
0xCCC00204	-	Reserved
0xCCC00208	0x02000812	GRDMAC capability register
0xCCC0020C	-	GRDMAC interrupt flag register (updated by the DMA core)

as required by the core.

The core is configured with only one DMA channel (channel 0) and one master interface, as can be seen in the capability register. Additionally the internal core’s buffer is 512 Bytes and the time-out timer is available.

The core’s control register is pre-set to enable channel 0 and to enable interrupts and interrupts on errors. To start the execution of the channel the software will write a ‘1’ to the enable bit in the control register, usually by reading the register, performing a logical OR with 0x00000001, and writing the value back to the register. In this case the value that needs to be written to address 0xCCC00200 to correctly start execution is 0x0001000D.

39.13 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x095. For description of vendor and device identifiers see GRLIB IP Library User’s Manual.

39.14 Implementation

39.14.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User’s Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support *grlib_async_reset_enable*. All registers that react on the reset signal will have a synchronous reset.

39.15 Configuration options

Table 513 shows the configuration options of the GRDMAC core (VHDL generics). These options are specific to the generic entity *grdmac*. See the chapter Instantiation for more details on specialized versions of GRDMAC.

*Table 513.*Configuration options

Generic	Function	Allowed range	Default
hmindex	AHB master index (AHBM0)	0 - NAHBMST-1	0
hirq	IRQ line used by GRDMAC	0 - NAHBIRQ-1	0
pindex	APB slave index	0 - NAPBSLV-1	0
paddress	Addr field of the APB bar.	0 - 16#FFF#	1
pmask	Mask field of the APB bar.	0 - 16#FFF#	16#FFF#
en_ahbm1	Enable second AHB master interface (AHBM1)	0 - NAHBMST-1	0
hmindex1	Second AHB master (AHBM1) index	0 - NAHBMST-1	1
ndmach	Number of available DMA channels.	1 - 16	1
bufsize	Internal buffer size. Must be a power of 2.	8 - 65536	256
burstbound	Boundary that the burst will never cross. Maximum is 1KB as per the AMBA AHB standard. Could be set to smaller values to ease re-arbitration. Must be a multiple of 2.	4 - 1024	512
timer_en	Enables the implementation of the timeout counter which can be set during triggered conditional descriptor execution.	0 - 1	0
memtech	Internal buffer’s memory technology selection	0 - NTECH	0
testen	Enable bypass logic for scan testing	0 - 1	0
ft	This generic determines if fault tolerance should be added to the internal data realignment buffer. 0 = no fault tolerance, 1 = byte parity DMR, 2 = TMR. Note that this generic needs to be set to 0 if the core is used together with the GPL version of GRLIB, since that version does not include any fault tolerance capability.	0 - 2	0
wbmask	Wide-bus mask. Indicates which address ranges are 64/128 bit capable. Treated as a 16-bit vector with LSB bit (right-most) indicating address 0 - 0x10000000. See section 39.7 for more information.	0 - 16#FFFF#	0
busw	Bus width of the wide bus area (64 or 128). See section 39.7 for more information.	64, 128	64

39.16 Signal descriptions

Table 514 shows the interface signals of the core (VHDL ports).

*Table 514.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	AHB reset	Low
CLK	N/A	Input	AHB clock	-
AHBMI	*	Input	AHB master input	-
AHBMO	*	Output	AHB master output	-
AHBMI1	*	Input	AHB second master input	-
AHBMO1	*	Output	AHB second master output	-
APBI	*	Output	APB slave inputs	-
APBO	*	Input	APB slave outputs	-
IRQ_TRIG[63:0]		Input	Descriptor triggering input	

* see GRLIB IP Library User's Manual

39.17 Library dependencies

Table 515 shows the libraries used when instantiating the core (VHDL libraries).

*Table 515.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	GRDMAC_PKG	Components, signals	GRDMAC internal components and signals.

39.18 Instantiation

In addition to the generic GRDMAC version, *grdmac*, a single-port version of the core is available, *grdmac_1p*, where the *en_ahbm1* generic is preset to '0', and the generics and ports related to the dual-port functionality are removed for convenience.

```
library ieee;
use ieee.std_logic_1164.all;

library gaisler;
use gaisler.misc.all;
use gaisler.grdmac_pkg.all;

library grlib;
use grlib.amba.all;
use grlib.stdlib.all;

entity grdmac_ex is

end entity;

architecture rtl of grdmac_ex is

    -- AMBA signals
    signal apbi : apb_slv_in_type;
    signal apbo : apb_slv_out_vector := (others => apb_none);

    signal ahbsi : ahb_slv_in_type;
    signal ahbso : ahb_slv_out_vector := (others => ahbs_none);

    signal ahbmi : ahb_mst_in_type;
    signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);
```

```
begin

    -- ... AHBCTRL

    -- GRDMAC one-AHB-port, AHB master index 1, APB index 0
    -- internal buffer size 1024 bytes, will break bursts at 512 byte boundaries
    -- APB registers at address 0xCCC00200
    dma0 : grdmac_1p
        generic map (
            hmindex     => 1,
            pindex      => 0,
            paddr       => 16#002#,
            hirq        => 1,
            ndmach      => 2,
            bufsize     => 1024, --bytes
            burstbound  => 512 -- bytes
        )
        port map (rstn, clk, ahbmi, ahbmo(1), apbi, apbo(0));

    -- AHB/APB bridge, AHB slave index 2
    apb0: apbctrl
        generic map (hindex => 2, haddr => 16#CCC#)
        port map (rstn,  clk,  ahbsi, ahbso(2), apbi, apbo);

    -- ... APB peripherals

end architecture ; -- rtl
```

40 GRECC - Elliptic Curve Cryptography

40.1 Overview

Elliptic Curve Cryptography (ECC) is used as a public key mechanism. The computational burden that is inhibited by ECC is less than the one of RSA. ECC provides the same level of security as RSA but with a significantly shorter key length. ECC is well suited for application in mobile communication.

The GRECC core implements encryption and decryption for an elliptic curve based on 233-bit key and point lengths. The implemented curve is denoted as *sect233r1* or *B-233*.

The *sect233r1* elliptic curve domain parameters are specified in the “Standards for Efficient Cryptography (SEC) - SEC2: Recommended Elliptic Curve Domain Parameters” document. The document is established by the Standards for Efficient Cryptography Group (SECG).

The *B-233* elliptic curve domain parameters are specified in the “Digital Signature Standard (DSS)” document, Federal Information Processing Standards (FIPS) Publication 186-2. The document is established by the National Institute of Standards and Technology (NIST).

The GRECC can be used with algorithms such as:

- Elliptic Curve Digital Signature Algorithm DSA (ECDSA), which appears in FIPS 186-2, IEEE 1363-2000 and ISO/IEC 15946-2
- Elliptic Curve El Gamal Method (key exchange protocol)
- Elliptic Curve Diffie-Hellman (ECDH) (key agreement protocol)

The core provides the following internal AMBA APB slave interface, with sideband signals as per [GRLIB] including:

- interrupt bus
- configuration information
- diagnostic information

The core can be partition in the following hierarchical elements:

- Elliptic Curve Cryptography (ECC) core
- AMBA APB slave
- GRLIB plug&play wrapper

Note that the core can also be used without the GRLIB plug&play information.

40.2 Operation

Elliptic Curve Cryptography (ECC) is an asymmetric cryptographic approach (also known as public key cryptography) that applies different keys for encryption and decryption. The most expensive operation during both encryption and decryption is the elliptic curve point multiplication. Hereby, a point on the elliptic curve is multiplied with a long integer ($k*P$ multiplication). The bit sizes of the coordinates of the point $P=(x, y)$ and the factor k have a length of hundreds of bits.

In this implementation the key and the point lengths are 233 bit, so that for every key there are 8 write cycles necessary and for every point (consisting of x and y) there are 16 write cycles necessary. After at least 16700 clock cycles the result can be read out.

The key is input via eight registers. The input point P_{in}=(x, y) is written via eight registers for x and eight registers for y. After the last y input register is written, the encryption or decryption is started. The progress can be observed via the status register. When the operation is completed, an interrupt is generated. The output point P_{out}=(x, y) is then read out via eight registers for x and eight registers for y.

40.3 Advantages

The main operation in ECC is the k*P multiplication. One k*P multiplication requires about 1500 field multiplications in the base field, which is the most expensive base operation. The complexity of a field multiplication can be reduced by applying the Karatsuba method. Normally the Karatsuba approach is applied recursively. The GRECC core includes an iterative implementation of the Karatsuba method which allows to realize area efficient hardware accelerators for the *k*P* multiplication. Hardware accelerators which are realized applying an iterative approach need up to 60 per cent less area and about 30 per cent less energy per multiplication than the recursive variants.

40.4 Background

The Standards for Efficient Cryptography Group (SECG) was initiated by Certicom Corporation to address the difficulty vendors and users face when building and deploying interoperable security solutions. The SECG is a broad international coalition comprised of leading technology companies and key industry players in the information security industry. One of the goals is to enable the effective incorporation of Elliptic Curve Cryptographic (ECC) technology into these various cryptographic solutions.

The Standards for Efficient Cryptography Group (SECG) has develop two sets of documents. The first set, under the name SEC, specifies interoperable cryptographic technologies and solutions. The second set, Guidelines for Efficient Cryptography (GEC), provides background information on elliptic curve cryptography and recommendations for ECC parameter and curve selection.

The Federal Information Processing Standards Publication Series of the National Institute of Standards and Technology (NIST) is the official series of publications relating to standards and guidelines adopted under the provisions of the Information Technology Management Reform Act.

This Digital Signature Standard (DSS) specifies a suite of algorithms which can be used to generate a digital signature. Digital signatures are used to detect unauthorized modifications to data and to authenticate the identity of the signatory. In addition, the recipient of signed data can use a digital signature in proving to a third party that the signature was in fact generated by the signatory. This is known as nonrepudiation since the signatory cannot, at a later time, repudiate the signature.

40.5 233-bit elliptic curve domain parameters

The core implements the 233-bit elliptic curve domain parameters *sect233r1,* or the equivalent *B-233*, which are verifiably random parameters. The following specification is established in “Standards for Efficient Cryptography (SEC) - SEC 2: Recommended Elliptic Curve Domain Parameters”. The verifiably random elliptic curve domain parameters over F_{2m} are specified by the septuple T = (m; f (x); a; b; G; n; h) where m = 233 and the representation of F_{2233} is defined by:

$f(x) = x^{233}+x^{74}+1$

The curve E: $y^2+xy = x^3+ax^2+b$ over F_{2m} is defined by:

a = 0000 00000000 00000000 00000000 00000000 00000000 00000000 00000001

b = 0066 647EDE6C 332C7F8C 0923BB58 213B333B 20E9CE42 81FE115F 7D8F90AD

The base point G in compressed form is:

G = 0300FA C9DFCBAC 8313BB21 39F1BB75 5FEF65BC 391F8B36 F8F8EB73 71FD558B

and in uncompressed form is:

G = 04 00FAC9DF CBAC8313 BB2139F1 BB755FEF 65BC391F 8B36F8F8
EB7371FD 558B0100 6A08A419 03350678 E58528BE BF8A0BEF F867A7CA
36716F7E 01F81052

Finally the order *n* of *G* and the cofactor are:

n = 0100 00000000 00000000 00000000 0013E974 E72F8A69 22031D26 03CFE0D7

h = 02

40.6 Throughput

The data throughput for the GRECC core is around 233/16700 bits per clock cycle, i.e. approximately 13.9 kbits per MHz.

The underlaying EEC core has been implemented in a dual crypto chip on 250 nm technology as depicted in the figure below. The throughput at 33 MHz operating frequency was 850 kbit/s, the power consumption was 56,8 mW, and the size was 48,5 kgates.

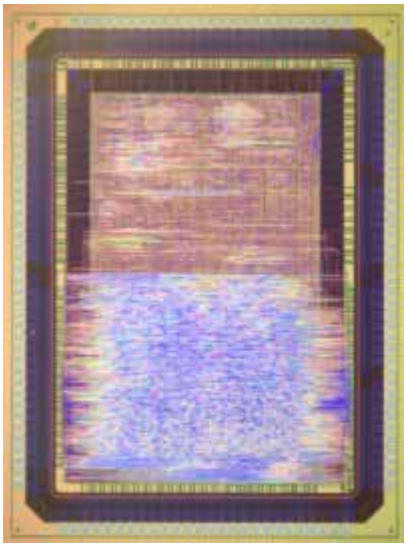


Figure 122. Dual Crypto Chip

40.7 Characteristics

The GRECC core has been synthesized for a Xilinx Virtex-2 XC2V6000-4 devices with the following results:

- LUTs: 12850 (19%)
- Frequency:93 MHz

40.8 Registers

The core is programmed through registers mapped into APB address space.

*Table 516.*GRECC registers

APB address offset	Register
0x20	Key 0 Register
0x24	Key 1 Register
0x28	Key 2 Register
2C	Key 3 Register
0x30	Key 4 Register
0x34	Key 5 Register
0x38	Key 6 Register
0x3C	Key 7 Register
0x40	Point X Input 0 Register
0x044	Point X Input 1 Register
0x048	Point X Input 2 Register
0x04C	Point X Input 3 Register
0x050	Point X Input 4 Register
0x054	Point X Input 5 Register
0x58	Point X Input 6 Register
0x5C	Point X Input 7 Register
0x60	Point Y Input 0 Register
0x64	Point Y Input 1 Register
0x68	Point Y Input 2 Register
0x6C	Point Y Input 3 Register
0x70	Point Y Input 4 Register
0x74	Point Y Input 5 Register
0x78	Point Y Input 6 Register
0x7C	Point Y Input 7 Register
0xA0	Point X Output 0 Register
0xA4	Point X Output 1 Register
0xA8	Point X Output 2 Register
0xAC	Point X Output 3 Register
0xB0	Point X Output 4 Register
0xB4	Point X Output 5 Register
0xB8	Point X Output 6 Register
0xBC	Point X Output 7 Register
0xC0	Point Y Output 0 Register
0xC4	Point Y Output 1 Register
0xC8	Point Y Output 2 Register
0xCC	Point Y Output 3 Register
0xD0	Point Y Output 4 Register
0xD4	Point Y Output 5 Register
0xD8	Point Y Output 6 Register
0xDC	Point Y Output 7 Register
0xFC	Status Register

40.8.1 Key 0 to 7 Registers

*Table 517.*0x20 - KEY0 - Key 0 Register (least significant)

31	0
KEY(31 downto 0)	
0	
w	

*Table 518.*0x24 - KEY1 - Key 1 Register

31	0
KEY(63 downto32)	
0	
w	

*Table 519.*0x28 - KEY2 - Key 2 Register

31	0
KEY(95 downto 64)	
0	
w	

*Table 520.*0x2C - KEY3 - Key 3 Register

31	0
KEY(127 downto 96)	
0	
w	

*Table 521.*0x30 - KEY4 - Key 4 Register

31	0
KEY(159 downto 128)	
0	
w	

*Table 522.*0x34 - KEY5 - Key 5 Register

31	0
KEY(191 downto 160)	
0	
w	

*Table 523.*0x38 - KEY6 - Key 6 Register

31	0
KEY(223 downto 192)	
0	
w	

*Table 524.*0x3C - KEY7 - Key 7 Register (most significant)

31 9	8 0
RESERVED	KEY(232 downto 224)
0	0
-	w

40.8.2 Point X Input 0 to 7 Registers

*Table 525.*0x40 - PXI0 - Point X Input 0 Register (least significant)

31	0
X(31 downto 0)	
0	
w	

*Table 526.*0x44 - PXI1 - Point X Input 1 Register

31	0
X(63 downto32)	
0	
w	

*Table 527.*0x48 - PXI2 - Point X Input 2 Register

31	0
X(95 downto 64)	
0	
w	

*Table 528.*0x4C - PXI3 - Point X Input 3 Register

31	0
X(127 downto 96)	
0	
w	

*Table 529.*0x50 - PXI4 - Point X Input 4 Register

31	0
X(159 downto 128)	
0	
w	

*Table 530.*0x54 - PXI5 - Point X Input 5 Register

31	0
X(191 downto 160)	
0	
w	

*Table 531.*0x58 - PXI6 - Point X Input 6 Register

31	0
X(223 downto 192)	
0	
w	

*Table 532.*0x5C - PXI7 - Point X Input 7 Register (most significant)

31 9	8 0
RESERVED	X(232 downto 224)
0	0
-	w

40.8.3 Point Y Input 0 to 7 Registers (W)

*Table 533.*0x60 - PYI0 - Point Y Input 0 Register (least significant)

31	0
Y(31 downto 0)	

*Table 534.*0x64 - PYI1 - Point Y Input 1 Register

31	0
Y(63 downto32)	

*Table 535.*0x68 - PYI2 - Point Y Input 2 Register

31	0
Y(95 downto 64)	

*Table 536.*0x6C - PYI3 - Point Y Input 3 Register

31	0
Y(127 downto 96)	

*Table 537.*0x70 - PYI4 - Point Y Input 4 Register

31	0
Y(159 downto 128)	

*Table 538.*0x74 - PYI5 - Point Y Input 5 Register

31	0
Y(191 downto 160)	

*Table 539.*0x78 - PYI6 - Point Y Input 6 Register

31	0
Y(223 downto 192)	

*Table 540.*0x7C - PYI7 - Point Y Input 7 Register (most significant)

31 9	8 0
RESERVED	Y(232 downto 224)
	0
	w

The encryption or decryption operation is started when the Point Y Input 7 Register is written.

40.8.4 Point X Output 0 to 7 Registers (R)

*Table 541.*0xA0 - PXO0 - Point X Output 0 Register (least significant)

31	0
X(31 downto 0)	
NR	
r	

*Table 542.*0xA4 - PXO1 - Point X Output 1 Register

31	0
X(63 downto32)	
NR	
r	

*Table 543.*0xA8 - PXO2 - Point X Output 2 Register

31	0
X(95 downto 64)	
NR	
r	

*Table 544.*0xAC - PXO3 - Point X Output 3 Register

31	0
X(127 downto 96)	
NR	
r	

*Table 545.*0xB0 - PXO4 - Point X Output 4 Register

31	0
X(159 downto 128)	
NR	
r	

*Table 546.*0xB4 - PXO5 - Point X Output 5 Register

31	0
X(191 downto 160)	
NR	
r	

*Table 547.*0xB8 - PXO6 - Point X Output 6 Register

31	0
X(223 downto 192)	
NR	
r	

*Table 548.*0xBC - PXO7 - Point X Output 7 Register (most significant)

31 9	8 0
RESERVED	X(232 downto 224)
-	NR
r	r

40.8.5 Point Y Output 0 to 7 Registers (R)

*Table 549.*0xC0 - PYO0 - Point Y Output 0 Register (least significant)

31	0
Y(31 downto 0)	
NR	
r	

*Table 550.*0xC4 - PYO1 - Point Y Output 1 Register

31	0
Y(63 downto32)	
NR	
r	

*Table 551.*0xC8 - PYO2 - Point Y Output 2 Register

31	0
Y(95 downto 64)	
NR	
r	

*Table 552.*0xCC - PYO3 - Point Y Output 3 Register

31	0
Y(127 downto 96)	
NR	
r	

*Table 553.*0xD0 - PYO4 - Point Y Output 4 Register

31	0
Y(159 downto 128)	
NR	
r	

*Table 554.*0xD4 - PYO5 - Point Y Output 5 Register

31	0
Y(191 downto 160)	
NR	
r	

*Table 555.*0xD8 - PYO6 - Point Y Output 6 Register

31	0
Y(223 downto 192)	
NR	
r	

*Table 556.*0xDC - PYO7 - Point Y Output 7 Register (most significant)

31 9	8 0
RESERVED	Y(232 downto 224)
-	NR
r	r

40.8.6 Status Register (R)

*Table 557.*0xFC - STAT - Status Register

31 1	0
.	FSM
0	1
r	r

31-1: - Unused
0: FSM 0 when ongoing, 1 when idle or ready

40.9 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x074. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

40.10 Configuration options

Table 558 shows the configuration options of the core (VHDL generics).

*Table 558.*Configuration options

Generic	Function	Allowed range	Default
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	Addr field of the APB BAR	0 - 16#FFF#	0
pmask	Mask field of the APB BAR	0 - 16#FFF#	16#FFC#
pirq	Interrupt line used by the GRECC	0 - NAHBIRQ-1	0

40.11 Signal descriptions

Table 559 shows the interface signals of the core (VHDL ports).

*Table 559.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
DEBUG[10:0]	N/A	Output	Debug information	-

* see GRLIB IP Library User's Manual

Note that the ECC core can also be used without the GRLIB plug&play information. The AMBA APB signals are then provided as IEEE Std_Logic_1164 compatible scalars and vectors.

40.12 Library dependencies

Table 560 shows libraries used when instantiating the core (VHDL libraries).

*Table 560.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	CRYPTO	Component	GRECC component declarations

40.13 Instantiation

This example shows how the core can be instantiated.

```
library  ieee;
use      ieee.std_logic_1164.all;

library  grlib;
use      grlib.amba.all;

library  gaisler;
use      gaisler.crypto.all;
...
...
   signal debug: std_logic_vector(10 downto 0);
..
..
   grecc0: grecc
      generic map (
         pindex         => pindex,
         paddr          => paddr,
         pmask          => pmask,
         pirq           => pirq)
      port map (
         rstn           => rstn,
         clk            => clk,
         apbi           => apbi,
         apbo           => apbo(pindex),
         debug          => debug);
```

41 GRETH - Ethernet Media Access Controller (MAC) with EDCL support

41.1 Overview

Cobham Gaisler's Ethernet Media Access Controller (GRETH) provides an interface between an AMBA-AHB bus and an Ethernet network. It supports 10/100 Mbit speed in both full- and half-duplex. The AMBA interface consists of an APB interface for configuration and control and an AHB master interface which handles the dataflow. The dataflow is handled through DMA channels. There is one DMA engine for the transmitter and one for the receiver. Both share the same AHB master interface. The ethernet interface supports both the MII and RMII interfaces which should be connected to an external PHY. The GRETH also provides access to the MII Management interface which is used to configure the PHY.

Optional hardware support for the Ethernet Debug Communication Link (EDCL) protocol is also provided. This is an UDP/IP based protocol used for remote debugging.

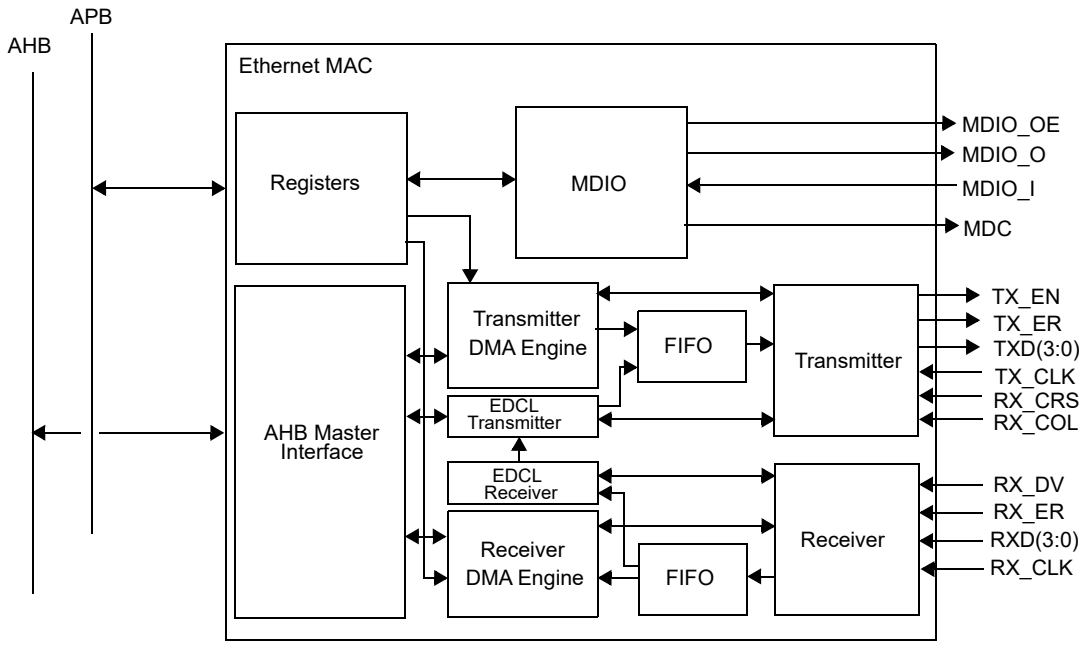


Figure 123. Block diagram of the internal structure of the GRETH.

41.2 Operation

41.2.1 System overview

The GRETH consists of 3 functional units: The DMA channels, MDIO interface and the optional Ethernet Debug Communication Link (EDCL).

The main functionality consists of the DMA channels which are used to transfer data between an AHB bus and an Ethernet network. There is one transmitter DMA channel and one Receiver DMA channel. The operation of the DMA channels is controlled through registers accessible through the APB interface.

The MDIO interface is used for accessing configuration and status registers in one or more PHYs connected to the MAC. The operation of this interface is also controlled through the APB interface.

The optional EDCL provides read and write access to an AHB bus through Ethernet. It uses the UDP, IP, ARP protocols together with a custom application layer protocol to accomplish this. The EDCL contains no user accessible registers and always runs in parallel with the DMA channels.

The Media Independent Interface (MII) is used for communicating with the PHY. There is an Ethernet transmitter which sends all data from the AHB domain on the Ethernet using the MII interface. Correspondingly, there is an Ethernet receiver which stores all data from the Ethernet on the AHB bus. Both of these interfaces use FIFOs when transferring the data streams. The GRETH also supports the RMII which uses a subset of the MII signals.

The EDCL and the DMA channels share the Ethernet receiver and transmitter.

41.2.2 Protocol support

The GRETH is implemented according to IEEE standard 802.3-2002 and IEEE standard 802.3Q-2003. There is no support for the optional control sublayer. This means that packets with type 0x8808 (the only currently defined ctrl packets) are discarded. The support for 802.3Q is optional and need to be enabled via generics.

41.2.3 Clocking

GRETH has three clock domains: The AHB clock, Ethernet receiver clock and the Ethernet transmitter clock. The ethernet transmitter and receiver clocks are generated by the external ethernet PHY, and are inputs to the core through the MII interface. The three clock domains are unrelated to each other and all signals crossing the clock regions are fully synchronized inside the core.

Both full-duplex and half-duplex operating modes are supported and both can be run in either 10 or 100 Mbit. The minimum AHB clock for 10 Mbit operation is 2.5 MHz, while 18 MHz is needed for 100 Mbit. Using a lower AHB clock than specified will lead to excessive packet loss.

41.2.4 RAM debug support

Support for debug accesses the core's internal RAM blocks can be optionally enabled using the ramdebug VHDL generic. Setting it to 1 enables accesses to the transmitter and receiver RAM buffers and setting it to 2 enables accesses to the EDCL buffer in addition to the previous two buffers.

The transmitter RAM buffer is accessed starting from APB address offset 0x10000 which corresponds to location 0 in the RAM. There are 512 32-bit wide locations in the RAM which results in the last address being 0x107FC corresponding to RAM location 511 (byte addressing used on the APB bus).

Correspondingly the receiver RAM buffer is accessed starting from APB address offset 0x20000. The addresses, width and depth is the same.

The EDCL buffers are accessed starting from address 0x30000. The number of locations depend on the configuration and can be from 256 to 16384. Each location is 32-bits wide so the maximum address is 0x3FC and 0xFFFC correspondingly.

Before any debug accesses can be made the ramdebugen bit in the control register has to be set. During this time the debug interface controls the RAM blocks and normal operations is stopped. EDCL packets are not received. The MAC transmitter and receiver could still operate if enabled but the RAM buffers would be corrupt if debug accces are made simultaneously. Thus they MUST be disabled before the RAM debug mode is enabled.

41.2.5 Multibus version

There is a version of the core which has an additional master interface that can be used for the EDCL. Otherwise this version is identical to the basic version. The additional master interface is enabled with the edclsepahb VHDL generic. Then the ethi.edclsepahb signal control whether EDCL accesses are done on the standard master interface or the additional interface. Setting the signal to '0' makes the EDCL use the standard master interface while '1' selects the additional master. This signal is only sampled at reset and changes to this signal have no effect until the next reset.

41.2.6 Endianness

The core is designed for big-endian systems.

41.3 Tx DMA interface

The transmitter DMA interface is used for transmitting data on an Ethernet network. The transmission is done using descriptors located in memory.

41.3.1 Setting up a descriptor.

A single descriptor is shown in table 561 and 562. The number of bytes to be sent should be set in the length field and the address field should point to the data. The address must be word-aligned. If the interrupt enable (IE) bit is set, an interrupt will be generated when the packet has been sent (this requires that the transmitter interrupt bit in the control register is also set). The interrupt will be generated regardless of whether the packet was transmitted successfully or not. The Wrap (WR) bit is also a control bit that should be set before transmission and it will be explained later in this section.

*Table 561.*GRETH transmit descriptor word 0 (address offset 0x0)

31 16	15	14	13	12	11	10 0
RESERVED	AL	UE	IE	WR	EN	LENGTH

31: 16	RESERVED
15	Attempt Limit Error (AL) - The packet was not transmitted because the maximum number of attempts was reached.
14	Underrun Error (UE) - The packet was incorrectly transmitted due to a FIFO underrun error.
13	Interrupt Enable (IE) - Enable Interrupts. An interrupt will be generated when the packet from this descriptor has been sent provided that the transmitter interrupt enable bit in the control register is set. The interrupt is generated regardless if the packet was transmitted successfully or if it terminated with an error.
12	Wrap (WR) - Set to one to make the descriptor pointer wrap to zero after this descriptor has been used. If this bit is not set the pointer will increment by 8. The pointer automatically wraps to zero when the 1 kB boundary of the descriptor table is reached.
11	Enable (EN) - Set to one to enable the descriptor. Should always be set last of all the descriptor fields.
10: 0	LENGTH - The number of bytes to be transmitted.

*Table 562.*GRETH transmit descriptor word 1 (address offset 0x4)

31 2	1	0
ADDRESS	RES	

31: 2	Address (ADDRESS) - Pointer to the buffer area from where the packet data will be loaded.
1: 0	RESERVED

To enable a descriptor the enable (EN) bit should be set and after this is done, the descriptor should not be touched until the enable bit has been cleared by the GRETH.

41.3.2 Starting transmissions

Enabling a descriptor is not enough to start a transmission. A pointer to the memory area holding the descriptors must first be set in the GRETH. This is done in the transmitter descriptor pointer register. The address must be aligned to a 1 kB boundary. Bits 31 to 10 hold the base address of descriptor area while bits 9 to 3 form a pointer to an individual descriptor.The first descriptor should be located at the base address and when it has been used by the GRETH the pointer field is incremented by 8 to point at the next descriptor. The pointer will automatically wrap back to zero when the next 1 kB boundary has

been reached (the descriptor at address offset 0x3F8 has been used). The WR bit in the descriptors can be set to make the pointer wrap back to zero before the 1 kB boundary.

The pointer field has also been made writable for maximum flexibility but care should be taken when writing to the descriptor pointer register. It should never be touched when a transmission is active.

The final step to activate the transmission is to set the transmit enable bit in the control register. This tells the GRETH that there are more active descriptors in the descriptor table. This bit should always be set when new descriptors are enabled, even if transmissions are already active. The descriptors must always be enabled before the transmit enable bit is set.

41.3.3 Descriptor handling after transmission

When a transmission of a packet has finished, status is written to the first word in the corresponding descriptor. The Underrun Error bit is set if the FIFO became empty before the packet was completely transmitted while the Attempt Limit Error bit is set if more collisions occurred than allowed. The packet was successfully transmitted only if both of these bits are zero. The other bits in the first descriptor word are set to zero after transmission while the second word is left untouched.

The enable bit should be used as the indicator when a descriptor can be used again, which is when it has been cleared by the GRETH. There are three bits in the GRETH status register that hold transmission status. The Transmitter Error (TE) bit is set each time an transmission ended with an error (when at least one of the two status bits in the transmit descriptor has been set). The Transmitter Interrupt (TI) is set each time a transmission ended successfully.

The transmitter AHB error (TA) bit is set when an AHB error was encountered either when reading a descriptor or when reading packet data. Any active transmissions were aborted and the transmitter was disabled. The transmitter can be activated again by setting the transmit enable register.

41.3.4 Setting up the data for transmission

The data to be transmitted should be placed beginning at the address pointed by the descriptor address field. The GRETH does not add the Ethernet address and type fields so they must also be stored in the data buffer. The 4 B Ethernet CRC is automatically appended at the end of each packet. Each descriptor will be sent as a single Ethernet packet. If the size field in a descriptor is greater than defined by maxsize generic + header size bytes, the packet will not be sent.

41.4 Rx DMA interface

The receiver DMA interface is used for receiving data from an Ethernet network. The reception is done using descriptors located in memory.

41.4.1 Setting up descriptors

A single descriptor is shown in table 563 and 564. The address field should point to a word-aligned buffer where the received data should be stored. The GRETH will never store more than defined by the maxisize generic + header size bytes to the buffer. If the interrupt enable (IE) bit is set, an interrupt will be generated when a packet has been received to this buffer (this requires that the receiver interrupt bit in the control register is also set). The interrupt will be generated regardless of whether the packet was received successfully or not. The Wrap (WR) bit is also a control bit that should be set before the descriptor is enabled and it will be explained later in this section.

*Table 563.*GRETH receive descriptor word 0 (address offset 0x0)

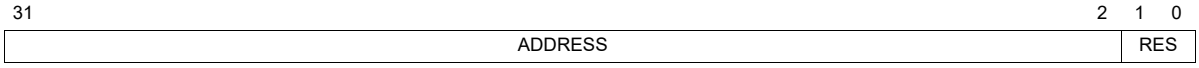
31 27	26	25 19	18	17	16	15	14	13	12	11	10 0
RESERVED	MC	RESERVED	LE	OE	CE	FT	AE	IE	WR	EN	LENGTH

31: 27 RESERVED

*Table 563.*GRETH receive descriptor word 0 (address offset 0x0)

26	Multicast address (MC) - The destination address of the packet was a multicast address (not broadcast).
25: 19	RESERVED
18	Length error (LE) - The length/type field of the packet did not match the actual number of received bytes.
17	Overrun error (OE) - The frame was incorrectly received due to a FIFO overrun.
16	CRC error (CE) - A CRC error was detected in this frame.
15	Frame too long (FT) - A frame larger than the maximum size was received. The excessive part was truncated.
14	Alignment error (AE) - An odd number of nibbles were received.
13	Interrupt Enable (IE) - Enable Interrupts. An interrupt will be generated when a packet has been received to this descriptor provided that the receiver interrupt enable bit in the control register is set. The interrupt is generated regardless if the packet was received successfully or if it terminated with an error.
12	Wrap (WR) - Set to one to make the descriptor pointer wrap to zero after this descriptor has been used. If this bit is not set the pointer will increment by 8. The pointer automatically wraps to zero when the 1 kB boundary of the descriptor table is reached.
11	Enable (EN) - Set to one to enable the descriptor. Should always be set last of all the descriptor fields.
10: 0	LENGTH - The number of bytes received to this descriptor.

*Table 564.*GRETH receive descriptor word 1 (address offset 0x4)



31: 2	Address (ADDRESS) - Pointer to the buffer area from where the packet data will be loaded.
1: 0	RESERVED

41.4.2 Starting reception

Enabling a descriptor is not enough to start reception. A pointer to the memory area holding the descriptors must first be set in the GRETH. This is done in the receiver descriptor pointer register. The address must be aligned to a 1 kB boundary. Bits 31 to 10 hold the base address of descriptor area while bits 9 to 3 form a pointer to an individual descriptor. The first descriptor should be located at the base address and when it has been used by the GRETH the pointer field is incremented by 8 to point at the next descriptor. The pointer will automatically wrap back to zero when the next 1 kB boundary has been reached (the descriptor at address offset 0x3F8 has been used). The WR bit in the descriptors can be set to make the pointer wrap back to zero before the 1 kB boundary.

The pointer field has also been made writable for maximum flexibility but care should be taken when writing to the descriptor pointer register. It should never be touched when reception is active.

The final step to activate reception is to set the receiver enable bit in the control register. This will make the GRETH read the first descriptor and wait for an incoming packet.

41.4.3 Descriptor handling after reception

The GRETH indicates a completed reception by clearing the descriptor enable bit. The other control bits (WR, IE) are also cleared. The number of received bytes is shown in the length field. The parts of the Ethernet frame stored are the destination address, source address, type and data fields. Bits 17-14 in the first descriptor word are status bits indicating different receive errors. All four bits are zero after a reception without errors. The status bits are described in table 563.

Packets arriving that are smaller than the minimum Ethernet size of 64 B are not considered as a reception and are discarded. The current receive descriptor will be left untouched an used for the first packet arriving with an accepted size. The TS bit in the status register is set each time this event occurs.

If a packet is received with an address not accepted by the MAC, the IA status register bit will be set.

Packets larger than maximum size cause the FT bit in the receive descriptor to be set. The length field is not guaranteed to hold the correct value of received bytes. The counting stops after the word containing the last byte up to the maximum size limit has been written to memory.

The address word of the descriptor is never touched by the GRETH.

41.4.4 Reception with AHB errors

If an AHB error occurs during a descriptor read or data store, the Receiver AHB Error (RA) bit in the status register will be set and the receiver is disabled. The current reception is aborted. The receiver can be enabled again by setting the Receive Enable bit in the control register.

41.4.5 Accepted MAC addresses

In the default configuration the core receives packets with either the unicast address set in the MAC address register or the broadcast address. Multicast support can also be enabled and in that case a hash function is used to filter received multicast packets. A 64-bit register, which is accessible through the APB interface, determines which addresses should be received. Each address is mapped to one of the 64 bits using the hash function and if the bit is set to one the packet will be received. The address is mapped to the table by taking the 6 least significant bits of the 32-bit Ethernet crc calculated over the destination address of the MAC frame. A bit in the receive descriptor is set if a packet with a multicast address has been received to it.

41.5 MDIO Interface

The MDIO interface provides access to PHY configuration and status registers through a two-wire interface which is included in the MII interface. The GRETH provided full support for the MDIO interface. If it is not needed in a design it can be removed with a VHDL generic.

The MDIO interface can be used to access from 1 to 32 PHY containing 1 to 32 16-bit registers. A read transfer i set up by writing the PHY and register addresses to the MDIO Control register and setting the read bit. This caused the Busy bit to be set and the operation is finished when the Busy bit is cleared. If the operation was successful the Linkfail bit is zero and the data field contains the read data. An unsuccessful operation is indicated by the Linkfail bit being set. The data field is undefined in this case.

A write operation is started by writing the 16-bit data, PHY address and register address to the MDIO Control register and setting the write bit. The operation is finished when the busy bit is cleared and it was successful if the Linkfail bit is zero.

41.5.1 PHY interrupts

The core also supports status change interrupts from the PHY. A level sensitive interrupt signal can be connected on the mdint input. The mdint_pol vhdl generic can be used to select the polarity. The PHY status change bit in the status register is set each time an event is detected in this signal. If the PHY status interrupt enable bit is set at the time of the event the core will also generate an interrupt on the AHB bus.

41.6 Ethernet Debug Communication Link (EDCL)

The EDCL provides access to an on-chip AHB bus through Ethernet. It uses the UDP, IP and ARP protocols together with a custom application layer protocol. The application layer protocol uses an ARQ algorithm to provide reliable AHB instruction transfers. Through this link, a read or write transfer can be generated to any address on the AHB bus. The EDCL is optional and must be enabled with a generic.

41.6.1 Operation

The EDCL receives packets in parallel with the MAC receive DMA channel. It uses a separate MAC address which is used for distinguishing EDCL packets from packets destined to the MAC DMA channel. The EDCL also has an IP address which is set through generics. Since ARP packets use the Ethernet broadcast address, the IP-address must be used in this case to distinguish between EDCL ARP packets and those that should go to the DMA-channel. Packets that are determined to be EDCL packets are not processed by the receive DMA channel.

When the packets are checked to be correct, the AHB operation is performed. The operation is performed with the same AHB master interface that the DMA-engines use. The replies are automatically sent by the EDCL transmitter when the operation is finished. It shares the Ethernet transmitter with the transmitter DMA-engine but has higher priority.

41.6.2 EDCL protocols

The EDCL accepts Ethernet frames containing IP or ARP data. ARP is handled according to the protocol specification with no exceptions.

IP packets carry the actual AHB commands. The EDCL expects an Ethernet frame containing IP, UDP and the EDCL specific application layer parts. Table 565 shows the IP packet required by the EDCL. The contents of the different protocol headers can be found in TCP/IP literature.

*Table 565.*The IP packet expected by the EDCL.

Ethernet Header	IP Header	UDP Header	2 B Offset	4 B Control word	4 B Address	Data 0 - 242 4B Words	Ethernet CRC

The following is required for successful communication with the EDCL: A correct destination MAC address as set by the generics, an Ethernet type field containing 0x0806 (ARP) or 0x0800 (IP). The IP-address is then compared with the value determined by the generics for a match. The IP-header checksum and identification fields are not checked. There are a few restrictions on the IP-header fields. The version must be four and the header size must be 5 B (no options). The protocol field must always be 0x11 indicating a UDP packet. The length and checksum are the only IP fields changed for the reply.

The EDCL only provides one service at the moment and it is therefore not required to check the UDP port number. The reply will have the original source port number in both the source and destination fields. UDP checksum are not used and the checksum field is set to zero in the replies.

The UDP data field contains the EDCL application protocol fields. Table 566 shows the application protocol fields (data field excluded) in packets received by the EDCL. The 16-bit offset is used to align the rest of the application layer data to word boundaries in memory and can thus be set to any value. The R/W field determines whether a read (0) or a write(1) should be performed. The length

*Table 566.*The EDCL application layer fields in received frames.

16-bit Offset	14-bit Sequence number	1-bit R/W	10-bit Length	7-bit Unused

field contains the number of bytes to be read or written. If R/W is one the data field shown in table 565 contains the data to be written. If R/W is zero the data field is empty in the received packets. Table 567 shows the application layer fields of the replies from the EDCL. The length field is always zero for replies to write requests. For read requests it contains the number of bytes of data contained in the data field.

*Table 567.*The EDCL application layer fields in transmitted frames.

16-bit Offset	14-bit sequence number	1-bit ACK/NAK	10-bit Length	7-bit Unused

The EDCL implements a Go-Back-N algorithm providing reliable transfers. The 14-bit sequence number in received packets are checked against an internal counter for a match. If they do not match, no operation is performed and the ACK/NAK field is set to 1 in the reply frame. The reply frame contains the internal counter value in the sequence number field. If the sequence number matches, the operation is performed, the internal counter value is stored in the sequence number field, the ACK/NAK field is set to 0 in the reply and the internal counter is incremented, . The length field is always set to 0 for ACK/NAK=1 frames. The unused field is not checked and is copied to the reply. It can thus be set to hold for example some extra identifier bits if needed.

41.6.3 EDCL IP and Ethernet address settings

The default value of the EDCL IP and MAC addresses are set by `ipaddrh, ipaddrl, macaddrh and macaddrl` generics. The IP address can later be changed by software, but the MAC address is fixed. To allow several EDCL enabled GRETH controllers on the same sub-net, the 4 LSB bits of the IP and MAC address can optionally be set by an input signal. This is enabled by setting the `edcl` generic = 2, and driving the 4-bit LSB value on ethi.edcladdr.

41.6.4 EDCL buffer size

The EDCL has a dedicated internal buffer memory which stores the received packets during processing. The size of this buffer is configurable with a VHDL generic to be able to obtain a suitable compromise between throughput and resource utilization in the hardware. Table 568 lists the different buffer configurations. For each size the table shows how many concurrent packets the EDCL can handle, the maximum size of each packet including headers and the maximum size of the data payload. Sending more packets before receiving a reply than specified for the selected buffer size will lead to dropped packets. The behavior is unspecified if sending larger packets than the maximum allowed.

*Table 568.*EDCL buffer sizes

Total buffer size (kB)	Number of packet buffers	Packet buffer size (B)	Maximum data payload (B)
1	4	256	200
2	4	512	456
4	8	512	456
8	8	1024	968
16	16	1024	968
32	32	1024	968
64	64	1024	968

41.7 Media Independent Interfaces

There are several interfaces defined between the MAC sublayer and the Physical layer. The GRETH supports two of them: The Media Independent Interface (MII) and the Reduced Media Independent Interface (RMII).

The MII was defined in the 802.3 standard and is most commonly supported. The ethernet interface have been implemented according to this specification. It uses 16 signals.

To support lower speed where the operation and clock frequency of the core and phy remains unchanged i.e. running at 10Mb/s when the IP is configured for 100Mb/s speed enable signals should be created to mimic the desired bit rate.

When operating at 10Mb/s, every byte of the MAC frame is repeated 10 clock periods to achieve the correct bit rate. The GRETH_GBIT core does not take care of this operation and enable signals with toggling frequency of the correct bit rate needs to be created.

The RMII was developed to meet the need for an interface allowing Ethernet controllers with smaller pin counts. It uses 6 (7) signals which are a subset of the MII signals. Table 569 shows the mapping between the RMII signals and the GRLIB MII interface.

*Table 569.*Signal mappings between RMII and the GRLIB MII interface.

RMII	MII
txd[1:0]	txd[1:0]
tx_en	tx_en
crs_dv	rx_crs
rxd[1:0]	rxd[1:0]
ref_clk	rmii_clk
rx_er	not used

41.8 Registers

The core is programmed through registers mapped into APB address space.

*Table 570.*GRETH registers

APB address offset	**Register**
0x0	Control register
0x4	Status/Interrupt-source register
0x8	MAC Address MSB
0xC	MAC Address LSB
0x10	MDIO Control/Status
0x14	Transmit descriptor pointer
0x18	Receiver descriptor pointer
0x1C	EDCL IP
0x20	Hash table msb
0x24	Hash table lsb
0x28	EDCL MAC address MSB
0x2C	EDCL MAC address LSB
0x10000 - 0x107FC	Transmit RAM buffer debug access
0x20000 - 0x207FC	Receiver RAM buffer debug access
0x30000 - 0x3FFFC	EDCL buffer debug access

41.8.1 Control Register

*Table 571.*0x00 - CTRL - GRETH control register

31	30 28	27	26	25	24 15	14	13	12	11	10	9 8	7	6	5	4	3	2	1	0
EA	BS		MA	MC	RESERVED	ED	RD	DD	ME	PI	RES	SP	RS	PM	FD	RI	TI	RE	TE
*	*	*	*	*	0	*	*	0	0	0	0	1	0	0	0	0	0	0	0
r	r	r	r	r	r	rw	rw	rw	rw	rw	r	rw	wc	rw	rw	rw	rw	rw	rw

31 EDCL available (EA) - Set to one if the EDCL is available.

30: 28 EDCL buffer size (BS) - Shows the amount of memory used for EDCL buffers. 0 = 1 kB, 1 = 2 kB, ..., 6 = 64 kB.

27 RESERVED

26 MDIO interrupts available (MA) - Set to one when the core supports mdio interrupts. Read only.

25 Multicast available (MC) - Set to one when the core supports multicast address reception. Read only.

24: 15 RESERVED

14 EDCL Disable (ED) - Set to one to disable the EDCL and zero to enable it. Reset value taken from the ethi.edcldisable signal. Only available if the EDCL hardware is present in the core.

13 RAM debug enable (RD) - Set to one to enable the RAM debug mode. Reset value: '0'. Only available if the VHDL generic ramdebug is nonzero.

12 Disable duplex detection (DD) - Disable the EDCL speed/duplex detection FSM. If the FSM cannot complete the detection the MDIO interface will be locked in busy mode. If software needs to access the MDIO the FSM can be disabled here and as soon as the MDIO busy bit is 0 the interface is available. Note that the FSM cannot be reenabled again.

11 Multicast enable (ME) - Enable reception of multicast addresses. Reset value: '0'.

10 PHY status change interrupt enable (PI) - Enables interrupts for detected PHY status changes.

9: 8 RESERVED

7 Speed (SP) - Sets the current speed mode. 0 = 10 Mbit, 1 = 100 Mbit. Only used in RMII mode (rmii = 1). A default value is automatically read from the PHY after reset. Reset value: '1'.

6 Reset (RS) - A one written to this bit resets the GRETH core. Self clearing. No other accesses should be done .to the slave interface other than polling this bit until it is cleared.

5 Promiscuous mode (PM) - If set, the GRETH operates in promiscuous mode which means it will receive all packets regardless of the destination address. Reset value: '0'.

4 Full duplex (FD) - If set, the GRETH operates in full-duplex mode otherwise it operates in half-duplex. Reset value: '0'.

3 Receiver interrupt (RI) - Enable Receiver Interrupts. An interrupt will be generated each time a packet is received when this bit is set. The interrupt is generated regardless if the packet was received successfully or if it terminated with an error. Reset value: '0'.

2 Transmitter interrupt (TI) - Enable Transmitter Interrupts. An interrupt will be generated each time a packet is transmitted when this bit is set. The interrupt is generated regardless if the packet was transmitted successfully or if it terminated with an error. Reset value: '0'.

1 Receive enable (RE) - Should be written with a one each time new descriptors are enabled. As long as this bit is one the GRETH will read new descriptors and as soon as it encounters a disabled descriptor it will stop until RE is set again. This bit should be written with a one after the new descriptors have been enabled. Reset value: '0'.

0 Transmit enable (TE) - Should be written with a one each time new descriptors are enabled. As long as this bit is one the GRETH will read new descriptors and as soon as it encounters a disabled descriptor it will stop until TE is set again. This bit should be written with a one after the new descriptors have been enabled. Reset value: '0'.

41.8.2 Status Register

*Table 572.*0x04 - STAT - GRETH status register

31 9	8	7	6	5	4	3	2	1	0
RESERVED	PS	IA	TS	TA	RA	TI	RI	TE	RE
	0	0	0	NR	NR	NR	NR	NR	NR
	wc	wc	wc	wc	wc	wc	wc	wc	wc

*Table 572.*0x04 - STAT - GRETH status register

8	PHY status changes (PS) - Set each time a PHY status change is detected.
7	Invalid address (IA) - A packet with an address not accepted by the MAC was received. Cleared when written with a one. Reset value: ‘0’.
6	Too small (TS) - A packet smaller than the minimum size was received. Cleared when written with a one. Reset value: ‘0’.
5	Transmitter AHB error (TA) - An AHB error was encountered in transmitter DMA engine. Cleared when written with a one. Not Reset.
4	Receiver AHB error (RA) - An AHB error was encountered in receiver DMA engine. Cleared when written with a one. Not Reset.
3	Transmitter interrupt (TI) - A packet was transmitted without errors. Cleared when written with a one. Not Reset.
2	Receiver interrupt (RI) - A packet was received without errors. Cleared when written with a one. Not Reset.
1	Transmitter error (TE) - A packet was transmitted which terminated with an error. Cleared when written with a one. Not Reset.
0	Receiver error (RE) - A packet has been received which terminated with an error. Cleared when written with a one. Not Reset.

41.8.3 MAC Address MSB

*Table 573.*0x08 - MACMSB - GRETH MAC address MSB.

31 16	15 0
RESERVED	Bit 47 downto 32 of the MAC address
	NR
	rw

31: 16 RESERVED

15: 0 The two most significant bytes of the MAC Address. Not Reset.

41.8.4 MAC Address LSB

*Table 574.*0x0C - MACLSB - GRETH MAC address LSB.

31 0
Bit 31 downto 0 of the MAC address

31: 0 The four least significant bytes of the MAC Address. Not Reset.

41.8.5 MDIO ctrl/status Register

*Table 575.*0x10 - MDIO - GRETH MDIO ctrl/status register.

31 16	15 11	10 6	5 4	3	2	1	0
DATA	PHYADDR	REGADDR	RES	BU	LF	RD	WR
0	*	0		0	1	0	0
rw	rw	rw		r	r	rw	rw

31: 16 Data (DATA) - Contains data read during a read operation and data that is transmitted is taken from this field. Reset value: 0x0000.

15: 11 PHY address (PHYADDR) - This field contains the address of the PHY that should be accessed during a write or read operation. Reset value: “00000”.

10: 6 Register address (REGADDR) - This field contains the address of the register that should be accessed during a write or read operation. Reset value: “00000”.

5:4 RESERVED

3 Busy (BU) - When an operation is performed this bit is set to one. As soon as the operation is finished and the management link is idle this bit is cleared. Reset value: ‘0’.

2 Linkfail (LF) - When an operation completes (BUSY = 0) this bit is set if a functional management link was not detected. Reset value: ‘1’.

1 Read (RD) - Start a read operation on the management interface. Data is stored in the data field. Reset value: ‘0’.

0 Write (WR) - Start a write operation on the management interface. Data is taken from the Data field. Reset value: ‘0’.

41.8.6 Transmitter Descriptor Table Base Address Register

*Table 576.*0x14 - TXBASE - GRETH transmitter descriptor table base address register.

31 10	9 3	2 0
BASEADDR	DESCPNT	RES
NR	0	0
rw	rw	r

31: 10 Transmitter descriptor table base address (BASEADDR) - Base address to the transmitter descriptor table.Not Reset.

9: 3 Descriptor pointer (DESCPNT) - Pointer to individual descriptors. Automatically incremented by the Ethernet MAC.

2: 0 RESERVED

41.8.7 Receiver Descriptor Table Base Address Register

*Table 577.*0x18 - RXBASE - GRETH receiver descriptor table base address register.

31 10	9 3	2 0
BASEADDR	DESCPNT	RES
NR	0	0
rw	rw	r

31: 10 Receiver descriptor table base address (BASEADDR) - Base address to the receiver descriptor table.Not Reset.

9: 3 Descriptor pointer (DESCPNT) - Pointer to individual descriptors. Automatically incremented by the Ethernet MAC.

2: 0 RESERVED

41.8.8 EDCL IP Register

*Table 578.*0x1C - EDCLIP - GRETH EDCL IP register

31 0
EDCL IP ADDRESS
*
rw

31: 0 EDCL IP address. Reset value is set with the ipaddrh and ipaddrl generics.

41.8.9 Hash Table Msb Register

*Table 579.*0x20 - HhSB - GRETH Hash table msb register

31 0
Hash table (64:32)
NR
rw

31: 0 Hash table msb. Bits 64 downto 32 of the hash table.

41.8.10 Hash Table Lsb Register

*Table 580.*0x24 - HCSB - GRETH Hash table lsb register

31	0
Hash table (64:32)	
NR	
rw	

31: 0 Hash table lsb. Bits 31downto 0 of the hash table.

41.8.11 EDCL MAC Address MSB

*Table 581.*0x28 - EMACMSB - GRETH EDCL MAC address MSB.

31 16	15 0
RESERVED	Bit 47 downto 32 of the EDCL MAC Address
	*
	rw

31: 16 RESERVED

15: 0 The two most significant bytes of the EDCL MAC Address. Hardcoded reset value set with the VHDL generic macaddrh.

41.8.12 EDCL MAC Address LSB

*Table 582.*0x2C - EMACLSB - GRETH EDCL MAC address LSB.

31	0
Bit 31 downto 0 of the EDCL MAC Address	
*	
rw	

31: 0 The 4 least significant bytes of the EDCL MAC Address. Hardcoded reset value set with the VHDL generics macaddrh and macaddrl. If the VHDL generic edcl is set to 2 bits 3 downto 0 are set with the edcladdr input signal.

41.9 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x1D. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

41.10 Implementation

41.10.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

41.11 Configuration options

Table 583 shows the configuration options of the core (VHDL generics).

*Table 583.*Configuration options

Generic	Function	Allowed range	Default
hindex	AHB master index.	0 - NAHBMST-1	0
pindex	APB slave index	0 - NAPBSLV-1	0

*Table 583.*Configuration options

Generic	Function	Allowed range	Default
paddr	Addr field of the APB bar.	0 - 16#FFF#	0
pmask	Mask field of the APB bar.	0 - 16#FFF#	16#FFF#
pirq	Interrupt line used by the GRETH.	0 - NAHBIRQ-1	0
memtech	Memory technology used for the FIFOs.	0 - NTECH	inferred
ifg_gap	Number of ethernet clock cycles used for one interframe gap. Default value as required by the standard. Do not change unless you know what you are doing.	1 - 255	24
attempt_limit	Maximum number of transmission attempts for one packet. Default value as required by the standard.	1 - 255	16
backoff_limit	Limit on the backoff size of the backoff time. Default value as required by the standard. Sets the number of bits used for the random value. Do not change unless you know what your doing.	1 - 10	10
slot_time	Number of ethernet clock cycles used for one slot- time. Default value as required by the ethernet standard. Do not change unless you know what you are doing.	1 - 255	128
mdcscaler	Sets the divisor value use to generate the mdio clock (mdc). The mdc frequency will be clk/(2*(mdcs-caler+1)).	0 - 255	25
enable_mdio	Enable the Management interface,	0 - 1	0
fifosize	Sets the size in 32-bit words of the receiver and transmit-ter FIFOs.	4 - 32	8
nsync	Number of synchronization registers used.	1 - 2	2
edcl	Enable EDCL. 0 = disabled. 1 = enabled. 2 = enabled and 4-bit LSB of IP and ethernet MAC address pro-grammed by ethi.edcladdr, 3=in addition to features for value 2 the reset value for the EDCL disable bit is taken from the ethi.edcldisable signal instead of being hard-coded to 0. 4=in addition to features for value 2 and 3 the an option is given to disable the EDCL via external input signal.	0 - 4	0
edclbufsz	Select the size of the EDCL buffer in kB.	1 - 64	1
macaddrh	Sets the upper 24 bits of the EDCL MAC address. Not all addresses are allowed and most NICs and proto-col implementations will discard frames with illegal addresses silently. Consult network literature if unsure about the addresses.	0 - 16#FFFFFF#	16#00005E#
macaddrl	Sets the lower 24 bits of the EDCL MAC address. Not all addresses are allowed and most NICs and proto-col implementations will discard frames with illegal addresses silently. Consult network literature if unsure about the addresses.	0 - 16#FFFFFF#	16#000000#
ipaddrh	Sets the upper 16 bits of the EDCL IP address reset value.	0 - 16#FFFF#	16#C0A8#
ipaddrl	Sets the lower 16 bits of the EDCL IP address reset value.	0 - 16#FFFF#	16#0035#
phyrstadr	Sets the reset value of the PHY address field in the MDIO register.	0 - 31	0
rmii	Selects the desired PHY interface. 0 = MII, 1 = RMII.	0 - 1	0
oepol	Selects polarity on output enable (ETHO.MDIO_OE). 0 = active low, 1 = active high	0 - 1	0

*Table 583.*Configuration options

Generic	Function	Allowed range	Default
mdint_pol	Selects polarity for level sensitive PHY interrupt line. 0 = active low, 1 = active high	0 - 1	0
enable_mdint	Enable mdio interrupts	0 - 1	0
multicast	Enable multicast support	0 - 1	0
ramdebug	Enables debug access to the core's RAM blocks through the APB interface. 1=enables access to the receiver and transmitter RAM buffers, 2=enables access to the EDCL buffers in addition to the functionality of value 1. Setting this generic to 2 will have no effect if the edcl generic is 0.	0 - 2	0
ehindex	AHB master index for the separate EDCL master interface. Only used if edclsepahb is 1.	0 - NAHBMST-1	0
edclsepahb	Enables separate EDCL AHB master interface. A signal determines if the separate interface or the common interface is used. Only available in the GRETH_GBIT_MB version of the core.	0 - 1	0
mdiohold	Set output hold time for MDIO in number of AHB cycles. Should be 10 ns or more.	1 - 30	1
maxsize	Set maximum length of the data field of Ethernet 802.3 frame. Values of 'maxsize' and below for this field indicate that the ethernet type field is used as the size of the payload of the Ethernet Frame while values of above 'maxsize' indicate that the field is used to represent EtherType. For 802.3q support set the length of the payload to 1504	64 - 2047	1500
gmiimode	Enable the use of receive and transmit valid signals to enter data to/from the PHY at the correct rate.	0-1	0

41.12 Signal descriptions

Table 584 shows the interface signals of the core (VHDL ports).

*Table 584.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
AHBMI	*	Input	AMB master input signals	-
AHBMO	*	Output	AHB master output signals	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-

*Table 584.*Signal descriptions

Signal name	Field	Type	Function	Active
ETHI	gtx_clk	Input	Ethernet gigabit transmit clock.	-
	rmii_clk	Input	Ethernet RMII clock.	-
	tx_clk	Input	Ethernet transmit clock.	-
	tx_dv	Input	Ethernet transmitter enable	-
	rx_clk	Input	Ethernet receive clock.	-
	rxd	Input	Ethernet receive data.	-
	rx_dv	Input	Ethernet receive data valid.	High
	rx_er	Input	Ethernet receive error.	High
	rx_col	Input	Ethernet collision detected. (Asynchronous, sampled with tx_clk)	High
	rx_crs	Input	Ethernet carrier sense. (Asynchronous, sampled with tx_clk)	High
	rx_en	Input	Ethernet receiver enable.	-
	mdio_i	Input	Ethernet management data input	-
	mdint	Input	Ethernet management interrupt	-
	phyrstaddr	Input	Reset address for GRETH PHY address field.	-
	edcldis	Input	Disable EDCL functionality	-
	edcladdr	Input	Sets the four least significant bits of the EDCL MAC address and the EDCL IP address when the edcl generic is set to 2.	-
	edclsepahb	Input	Selects AHB master interface for the EDCL. ‘0’ selects the common interface and ‘1’ selects the separate interface. Only available in the GRETH_GBIT_MB version of the core when the VHDL generic edclsepahb is set to 1.	-
	edcldisable	Input	Reset value for edcl disable register bit. Setting the signal to 1 disables the EDCL at reset and 0 enables it.	-
ETHO	reset	Output	Ethernet reset (asserted when the MAC is reset).	Low
	txd	Output	Ethernet transmit data.	-
	tx_en	Output	Ethernet transmit enable.	High
	tx_er	Output	Ethernet transmit error.	High
	mdc	Output	Ethernet management data clock.	-
	mdio_o	Output	Ethernet management data output.	-
	mdio_oe	Output	Ethernet management data output enable.	Set by the oepol generic.
MTESTI**	BUF	Input	Memory BIST input signal to buffer RAM	-
	EDCL	Input	Memory BIST input signal to EDCL RAM	-
MTESTO**	BUF	Output	Memory BIST output signal from buffer RAM	-
	EDCL	Output	Memory BIST output signal from EDCL RAM	-
MTESTCLK**	N/A	Input	Memory BIST clock	-

* see GRLIB IP Library User’s Manual

** not available in FPGA releases

41.13 Library dependencies

Table 585 shows libraries used when instantiating the core (VHDL libraries).

*Table 585.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	NET	Signals, components	GRETH component declaration

41.14 Instantiation

The first example shows how the non-mb version of the core can be instantiated and the second one show the mb version.

41.14.1 Non-MB version

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.ethernet_mac.all;

entity greth_ex is
  port (
    clk  : in std_ulogic;
    rstn : in std_ulogic;

    -- ethernet signals
    ethi :: in  eth_in_type;
    etho :  in  eth_out_type
    );
end;

architecture rtl of greth_ex is

  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);

begin

  -- AMBA Components are instantiated here
  ...

  -- GRETH
  e1 : greth
    generic map(
     hindex       => 0,
     pindex       => 12,
     paddr        => 12,
     pirq         => 12,
     memtech      => inferred,
     mdcscaler    => 50,
     enable_mdio  => 1,
     fifosize     => 32,
     nsync        => 1,
     edcl         => 1,
     edclbufsz    => 8,
     macaddrh     => 16#00005E#,
```

```
     macaddrl     => 16#00005D#,
     ipaddrh      => 16#c0a8#,
     ipaddrl      => 16#0035#)
 port map(
   rst          => rstn,
   clk          => clk,
   ahbmi        => ahbmi,
   ahbmo        => ahbmo(0),
   apbi         => apbi,
   apbo         => apbo(12),
   ethi         => ethi,
   etho         => etho
   );
end;
```

41.14.2 MB version

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.ethernet_mac.all;

entity greth_ex is
  port (
    clk  : in std_ulogic;
    rstn : in std_ulogic;

    -- ethernet signals
    ethi :: in  eth_in_type;
    etho :  in  eth_out_type
    );
end;

architecture rtl of greth_ex is

  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);

begin

  -- AMBA Components are instantiated here
  ...

  -- GRETH
  e1 : greth_mb
    generic map(
     hindex       => 0,
     pindex       => 12,
     paddr        => 12,
     pirq         => 12,
     memtech      => inferred,
     mdcscaler    => 50,
     enable_mdio  => 1,
     fifosize     => 32,
     nsync        => 1,
     edcl         => 1,
     edclbufsz    => 8,
     macaddrh     => 16#00005E#,
     macaddrl     => 16#00005D#,
     ipaddrh      => 16#c0a8#,
     ipaddrl      => 16#0035#,
     ehindex      => 1,
     edclsepahb   => 1)
```

```
 port map(
   rst          => rstn,
   clk          => clk,
   ahbmi        => ahbmi,
   ahbmo        => ahbmo(0),
   ahbmi2       => ahbmi,
   ahbmo2       => ahbmo(1),
   apbi         => apbi,
   apbo         => apbo(12),
   ethi         => ethi,
   etho         => etho
   );
end;
```

42 GRETH_GBIT - Gigabit Ethernet Media Access Controller (MAC) w. EDCL

42.1 Overview

Cobham Gaisler's Gigabit Ethernet Media Access Controller (GRETH_GBIT) provides an interface between an AMBA-AHB bus and an Ethernet network. It supports 10/100/1000 Mbit speed in both full- and half-duplex. The AMBA interface consists of an APB interface for configuration and control and an AHB master interface which handles the dataflow. The dataflow is handled through DMA channels. There is one DMA engine for the transmitter and one for the receiver. Both share the same AHB master interface.

The ethernet interface supports the MII and GMII interfaces which should be connected to an external PHY. The GRETH also provides access to the MII Management interface which is used to configure the PHY. Optional hardware support for the Ethernet Debug Communication Link (EDCL) protocol is also provided. This is an UDP/IP based protocol used for remote debugging.

Supported features for the DMA channels are Scatter Gather I/O and TCP/UDP over IPv4 checksum offloading for both receiver and transmitter. Software Drivers are provided for RTEMS, eCos, uClinux and Linux 2.6.

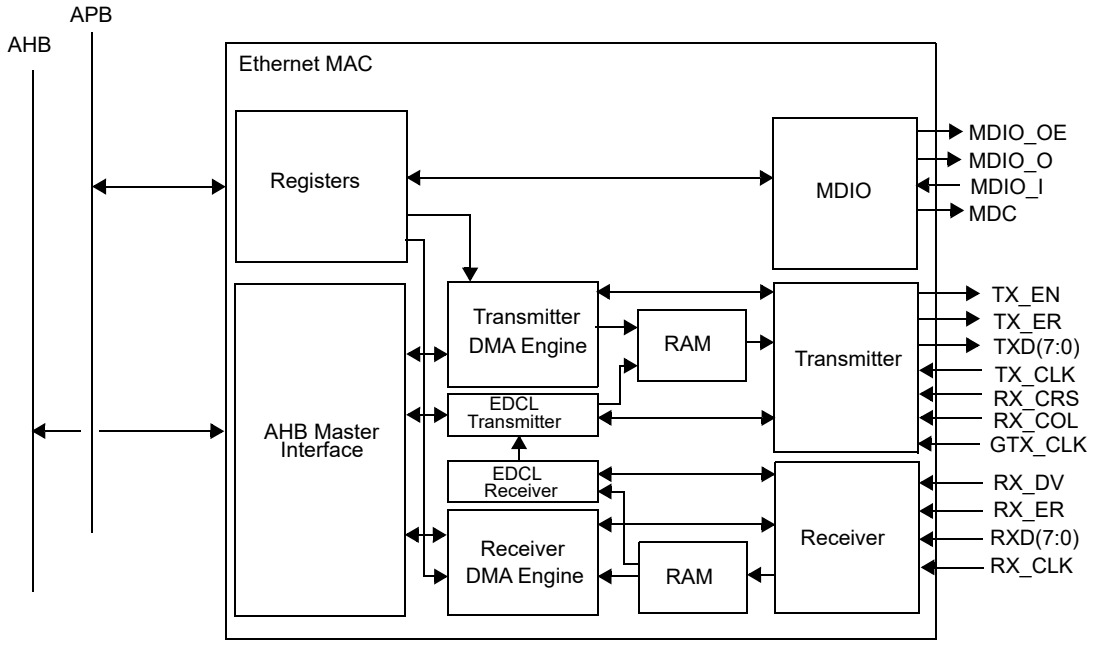


Figure 124. Block diagram of the internal structure of the GRETH_GBIT.

42.2 Operation

42.2.1 System overview

The GRETH_GBIT consists of 3 functional units: The DMA channels, MDIO interface and the optional Ethernet Debug Communication Link (EDCL).

The main functionality consists of the DMA channels which are used for transferring data between an AHB bus and an Ethernet network. There is one transmitter DMA channel and one Receiver DMA channel. The operation of the DMA channels is controlled through registers accessible through the APB interface.

The MDIO interface is used for accessing configuration and status registers in one or more PHYs connected to the MAC. The operation of this interface is also controlled through the APB interface.

The optional EDCL provides read and write access to an AHB bus through Ethernet. It uses the UDP, IP and ARP protocols together with a custom application layer protocol to accomplish this. The EDCL contains no user accessible registers and always runs in parallel with the DMA channels.

The Media Independent Interface (MII) and Gigabit Media Independent Interface (GMII) are used for communicating with the PHY. More information can be found in section 42.7.

The EDCL and the DMA channels share the Ethernet receiver and transmitter. More information on these functional units is provided in sections 42.3 - 42.6.

42.2.2 Protocol support

The GRETH_GBIT is implemented according to IEEE standard 802.3-2002. There is no support for the optional control sublayer. This means that packets with type 0x8808 (the only currently defined ctrl packets) are discarded.

42.2.3 Hardware requirements

The GRETH_GBIT is synthesisable with most Synthesis tools. There are three or four clock domains depending on if the gigabit mode is used. The three domains always present are the AHB clock, Ethernet Receiver clock (RX_CLK) and the 10/100 Ethernet transmitter clock (TX_CLK). If the gigabit mode is also used the fourth clock domain is the gigabit transmitter clock (GTX_CLK). Both full-duplex and half-duplex operating modes are supported and both can be run in either 10/100 or 1000 Mbit. The system frequency requirement (AHB clock) for 10 Mbit operation is 2.5 MHz, 18 MHz for 100 Mbit and 40 MHz for 1000 Mbit mode. The 18 MHz limit was tested on a Xilinx board with a DCM that did not support lower frequencies so it might be possible to run it on lower frequencies. It might also be possible to run the 10 Mbit mode on lower frequencies.

RX_CLK and TX_CLK are sourced by the PHY while GTX_CLK is sourced by the MAC according to the 802.3-2002 standard. The GRETH_GBIT does not contain an internal clock generator so GTX_CLK should either be generated in the FPGA (with a PLL/DLL) or with an external oscillator.

42.2.4 RAM debug support

Support for debug accesses the core's internal RAM blocks can be optionally enabled using the ramdebug VHDL generic. Setting it to 1 enables accesses to the transmitter and receiver RAM buffers and setting it to 2 enables accesses to the EDCL buffer in addition to the previous two buffers.

The transmitter RAM buffer is accessed starting from APB address offset 0x10000 which corresponds to location 0 in the RAM. There are 512 32-bit wide locations in the RAM which results in the last address being 0x107FC corresponding to RAM location 511 (byte addressing used on the APB bus).

Correspondingly the receiver RAM buffer is accessed starting from APB address offset 0x20000. The addresses, width and depth is the same.

The EDCL buffers are accessed starting from address 0x30000. The number of locations depend on the configuration and can be from 256 to 16384. Each location is 32-bits wide so the maximum address is 0x3FC and 0xFFFC correspondingly.

Before any debug accesses can be made the ramdebugen bit in the control register has to be set. During this time the debug interface controls the RAM blocks and normal operations is stopped. EDCL packets are not received. The MAC transmitter and receiver could still operate if enabled but the RAM buffers would be corrupt if debug accces are made simultaneously. Thus they MUST be disabled before the RAM debug mode is enabled.

42.2.5 Multibus version

There is a version of the core which has an additional master interface that can be used for the EDCL. Otherwise this version is identical to the basic version. The additional master interface is enabled with the edclsepahb VHDL generic. Then the ethi.edclsepahb signal control whether EDCL accesses are done on the standard master interface or the additional interface. Setting the signal to '0' makes the EDCL use the standard master interface while '1' selects the additional master. This signal is only sampled at reset and changes to this signal have no effect until the next reset.

42.2.6 Endianness

The core is designed for big-endian systems.

42.3 Tx DMA interface

The transmitter DMA interface is used for transmitting data on an Ethernet network. The transmission is done using descriptors located in memory.

42.3.1 Setting up a descriptor.

A single descriptor is shown in table 586 and 587. The number of bytes to be sent should be set in the length field and the address field should point to the data. There are no alignment restrictions on the address field. If the interrupt enable (IE) bit is set, an interrupt will be generated when the packet has been sent (this requires that the transmitter interrupt bit in the control register is also set). The interrupt will be generated regardless of whether the packet was transmitted successfully or not.

*Table 586.*GRETH_GBIT transmit descriptor word 0 (address offset 0x0)

31 21	20	19	18	17	16	15	14	13	12	11	10 0
RESERVED	UC	TC	IC	MO	LC	AL	UE	IE	WR	EN	LENGTH

31: 21	RESERVED
20	UDP checksum (UC) - Calculate and insert the UDP checksum for this packet. The checksum is only inserted if an UDP packet is detected.
19	TCP checksum (TC) - Calculate and insert the TCP checksum for this packet. The checksum is only inserted if an TCP packet is detected.
18	IP checksum (IC) - Calculate and insert the IP header checksum for this packet. The checksum is only inserted if an IP packet is detected.
17	More (MO) - More descriptors should be fetched for this packet (Scatter Gather I/O).
16	Late collision (LC) - A late collision occurred during the transmission (1000 Mbit mode only).
15	Attempt limit error (AL) - The packet was not transmitted because the maximum number of attempts was reached.
14	Underrun error (UE) - The packet was incorrectly transmitted due to a FIFO underrun error.
13	Interrupt enable (IE) - Enable Interrupts. An interrupt will be generated when the packet from this descriptor has been sent provided that the transmitter interrupt enable bit in the control register is set. The interrupt is generated regardless if the packet was transmitted successfully or if it terminated with an error.
12	Wrap (WR) - Set to one to make the descriptor pointer wrap to zero after this descriptor has been used. If this bit is not set the pointer will increment by 8. The pointer automatically wraps to zero when the 1 kB boundary of the descriptor table is reached.
11	Enable (EN) - Set to one to enable the descriptor. Should always be set last of all the descriptor fields.
10: 0	LENGTH - The number of bytes to be transmitted.

*Table 587.*GRETH_GBIT transmit descriptor word 1 (address offset 0x4)

31 0
ADDRESS

*Table 587.*GRETH_GBIT transmit descriptor word 1 (address offset 0x4)

31: 0	Address (ADDRESS) - Pointer to the buffer area from where the packet data will be loaded.

To enable a descriptor the enable (EN) bit should be set and after this is done, the descriptor should not be touched until the enable bit has been cleared by the GRETH_GBIT. The rest of the fields in the descriptor are explained later in this section.

42.3.2 Starting transmissions

Enabling a descriptor is not enough to start a transmission. A pointer to the memory area holding the descriptors must first be set in the GRETH_GBIT. This is done in the transmitter descriptor pointer register. The address must be aligned to a 1 kB boundary. Bits 31 to 10 hold the base address of descriptor area while bits 9 to 3 form a pointer to an individual descriptor. The first descriptor should be located at the base address and when it has been used by the GRETH_GBIT the pointer field is incremented by 8 to point at the next descriptor. The pointer will automatically wrap back to zero when the next 1 kB boundary has been reached (the descriptor at address offset 0x3F8 has been used). The WR bit in the descriptors can be set to make the pointer wrap back to zero before the 1 kB boundary.

The pointer field has also been made writable for maximum flexibility but care should be taken when writing to the descriptor pointer register. It should never be touched when a transmission is active.

The final step to activate the transmission is to set the transmit enable bit in the control register. This tells the GRETH_GBIT that there are more active descriptors in the descriptor table. This bit should always be set when new descriptors are enabled, even if transmissions are already active. The descriptors must always be enabled before the transmit enable bit is set.

42.3.3 Descriptor handling after transmission

When a transmission of a packet has finished, status is written to the first word in the corresponding descriptor. The Underrun Error bit is set if the transmitter RAM was not able to provide data at a sufficient rate. This indicates a synchronization problem most probably caused by a low clock rate on the AHB clock. The whole packet is buffered in the transmitter RAM before transmission so underruns cannot be caused by bus congestion. The Attempt Limit Error bit is set if more collisions occurred than allowed. When running in 1000 Mbit mode the Late Collision bit indicates that a collision occurred after the slottime boundary was passed.

The packet was successfully transmitted only if these three bits are zero. The other bits in the first descriptor word are set to zero after transmission while the second word is left untouched.

The enable bit should be used as the indicator when a descriptor can be used again, which is when it has been cleared by the GRETH_GBIT. There are three bits in the GRETH_GBIT status register that hold transmission status. The Transmit Error (TE) bit is set each time an transmission ended with an error (when at least one of the three status bits in the transmit descriptor has been set). The Transmit Successful (TI) is set each time a transmission ended successfully.

The Transmit AHB Error (TA) bit is set when an AHB error was encountered either when reading a descriptor, reading packet data or writing status to the descriptor. Any active transmissions are aborted and the transmitter is disabled. The transmitter can be activated again by setting the transmit enable register.

42.3.4 Setting up the data for transmission

The data to be transmitted should be placed beginning at the address pointed by the descriptor address field. The GRETH_GBIT does not add the Ethernet address and type fields so they must also be stored in the data buffer. The 4 B Ethernet CRC is automatically appended at the end of each packet.

Each descriptor will be sent as a single Ethernet packet. If the size field in a descriptor is greater than 1514 B, the packet will not be sent.

42.3.5 Scatter Gather I/O

A packet can be generated from data fetched from several descriptors. This is called Scatter Gather I/O. The More (MO) bit should be set to 1 to indicate that more descriptors should be used to generate the current packet. When data from the current descriptor has been read to the RAM the next descriptor is fetched and the new data is appended to the previous data. This continues until a descriptor with the MO bit set to 0 is encountered. The packet will then be transmitted.

Status is written immediately when data has been read to RAM for descriptors with MO set to 1. The status bits are always set to 0 since no transmission has occurred. The status bits will be written to the last descriptor for the packet (which had MO set to 0) when the transmission has finished.

No interrupts are generated for descriptors with MO set to 1 so the IE bit is don't care in this case.

The checksum offload control bits (explained in section 42.3.6) must be set to the same values for all descriptors used for a single packet.

42.3.6 Checksum offloading

Support is provided for correct checksum calculations in hardware for TCP and UDP over IPv4 for non-fragmented packets with data length less or equal to maximum transmission unit. The checksum calculations are enabled in each descriptor and applies only to that packet (when the MO bit is set all descriptors used for a single packet must have the checksum control bits set in the same way).

The IP Checksum bit (IC) enables IP header checksum calculations. If an IPv4 packet is detected when transmitting the packet associated with the descriptor the header checksum is calculated and inserted. If TCP Checksum (TC) is set the TCP checksum is calculated and inserted if an TCP/IPv4 packet is detected. Finally, if the UDP Checksum bit is set the UDP checksum is calculated and inserted if a UDP/IPv4 packet is detected. In the case of fragmented IP packets, incorrect checksums for TCP and UDP are inserted for the first fragment (which contains the TCP or UDP header).

42.4 Rx DMA interface

The receiver DMA interface is used for receiving data from an Ethernet network. The reception is done using descriptors located in memory.

42.4.1 Setting up descriptors

A single descriptor is shown in table 588 and 589. The address field points at the location where the received data should be stored. There are no restrictions on alignment. The GRETH_GBIT will never store more than 1518 B to the buffer (the tagged maximum frame size excluding CRC). The CRC field (4 B) is never stored to memory so it is not included in this number. If the interrupt enable (IE) bit is set, an interrupt will be generated when a packet has been received to this buffer (this requires that the receiver interrupt bit in the control register is also set). The interrupt will be generated regardless of whether the packet was received successfully or not.

The enable bit is set to indicate that the descriptor is valid which means it can be used by the to store a packet. After it is set the descriptor should not be touched until the EN bit has been cleared by the GRETH_GBIT.

The rest of the fields in the descriptor are explained later in this section..

*Table 588.*GRETH_GBIT receive descriptor word 0 (address offset 0x0)

31 27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10 0
RESERVED	MC	IF	TR	TD	UR	UD	IR	ID	LE	OE	CE	FT	AE	IE	WR	EN	LENGTH

31: 27	RESERVED
26	Multicast address (MC) - The destination address of the packet was a multicast address (not broadcast).
25	IP fragment (IF) - Fragmented IP packet detected.
24	TCP error (TR) - TCP checksum error detected.
23	TCP detected (TD) - TCP packet detected.
22	UDP error (UR) - UDP checksum error detected.
21	UDP detected (UD) - UDP packet detected.
20	IP error (IR) - IP checksum error detected.
19	IP detected (ID) - IP packet detected.
18	Length error (LE) - The length/type field of the packet did not match the actual number of received bytes.
17	Overrun error (OE) - The frame was incorrectly received due to a FIFO overrun.
16	CRC error (CE) - A CRC error was detected in this frame.
15	Frame too long (FT) - A frame larger than the maximum size was received. The excessive part was truncated.
14	Alignment error (AE) - An odd number of nibbles were received.
13	Interrupt Enable (IE) - Enable Interrupts. An interrupt will be generated when a packet has been received to this descriptor provided that the receiver interrupt enable bit in the control register is set. The interrupt is generated regardless if the packet was received successfully or if it terminated with an error.
12	Wrap (WR) - Set to one to make the descriptor pointer wrap to zero after this descriptor has been used. If this bit is not set the pointer will increment by 8. The pointer automatically wraps to zero when the 1 kB boundary of the descriptor table is reached.
11	Enable (EN) - Set to one to enable the descriptor. Should always be set last of all the descriptor fields.
10: 0	LENGTH - The number of bytes received to this descriptor.

*Table 589.*GRETH_GBIT receive descriptor word 1 (address offset 0x4)

31 0
ADDRESS

31: 0	Address (ADDRESS) - Pointer to the buffer area from where the packet data will be loaded.

42.4.2 Starting reception

Enabling a descriptor is not enough to start reception. A pointer to the memory area holding the descriptors must first be set in the GRETH_GBIT. This is done in the receiver descriptor pointer register. The address must be aligned to a 1 kB boundary. Bits 31 to 10 hold the base address of descriptor area while bits 9 to 3 form a pointer to an individual descriptor. The first descriptor should be located at the base address and when it has been used by the GRETH_GBIT the pointer field is incremented by 8 to point at the next descriptor. The pointer will automatically wrap back to zero when the next 1 kB boundary has been reached (the descriptor at address offset 0x3F8 has been used). The WR bit in the descriptors can be set to make the pointer wrap back to zero before the 1 kB boundary.

The pointer field has also been made writable for maximum flexibility but care should be taken when writing to the descriptor pointer register. It should never be touched when reception is active.

The final step to activate reception is to set the receiver enable bit in the control register. This will make the GRETH_GBIT read the first descriptor and wait for an incoming packet.

42.4.3 Descriptor handling after reception

The GRETH indicates a completed reception by clearing the descriptor enable bit. The other control bits (WR, IE) are also cleared. The number of received bytes is shown in the length field. The parts of the Ethernet frame stored are the destination address, source address, type and data fields. Bits 24-14 in the first descriptor word are status bits indicating different receive errors. Bits 18 - 14 are zero after a reception without link layer errors. The status bits are described in table 588 (except the checksum offload bits which are also described in section 42.4.6).

Packets arriving that are smaller than the minimum Ethernet size of 64 B are not considered as a reception and are discarded. The current receive descriptor will be left untouched an used for the first packet arriving with an accepted size. The TS bit in the status register is set each time this event occurs.

If a packet is received with an address not accepted by the MAC, the IA status register bit will be set.

Packets larger than maximum size cause the FT bit in the receive descriptor to be set. The length field is not guaranteed to hold the correct value of received bytes. The counting stops after the word containing the last byte up to the maximum size limit has been written to memory.

The address word of the descriptor is never touched by the GRETH.

42.4.4 Reception with AHB errors

If an AHB error occurs during a descriptor read or data store, the Receiver AHB Error (RA) bit in the status register will be set and the receiver is disabled. The current reception is aborted. The receiver can be enabled again by setting the Receive Enable bit in the control register.

42.4.5 Accepted MAC addresses

In the default configuration the core receives packets with either the unicast address set in the MAC address register or the broadcast address. Multicast support can also be enabled and in that case a hash function is used to filter received multicast packets. A 64-bit register, which is accessible through the APB interface, determines which addresses should be received. Each address is mapped to one of the 64 bits using the hash function and if the bit is set to one the packet will be received. The address is mapped to the table by taking the 6 least significant bits of the 32-bit Ethernet crc calculated over the destination address of the MAC frame. A bit in the receive descriptor is set if a packet with a multicast address has been received to it.

42.4.6 Checksum offload

Support is provided for checksum calculations in hardware for TCP/UDP over IPv4. The checksum logic is always active and detects IPv4 packets with TCP or UDP payloads. If IPv4 is detected the ID bit is set, UD is set if an UDP payload is detected in the IP packet and TD is set if a TCP payload is detected in the IP packet (TD and UD are never set if an IPv4 packet is not detected). When one or more of these packet types is detected its corresponding checksum is calculated and if an error is detected the checksum error bit for that packet type is set. The error bits are never set if the corresponding packet type is not detected. The core does not support checksum calculations for TCP and UDP when the IP packet has been fragmented. This condition is indicated by the IF bit in the receiver descriptor and when set neither the TCP nor the UDP checksum error indications are valid.

42.5 MDIO Interface

The MDIO interface provides access to PHY configuration and status registers through a two-wire interface which is included in the MII interface. The GRETH_GBIT provides full support for the MDIO interface.

The MDIO interface can be used to access from 1 to 32 PHY containing 1 to 32 16-bit registers. A read transfer i set up by writing the PHY and register addresses to the MDIO Control register and set-

ting the read bit. This caused the Busy bit to be set and the operation is finished when the Busy bit is cleared. If the operation was successful the Linkfail bit is zero and the data field contains the read data. An unsuccessful operation is indicated by the Linkfail bit being set. The data field is undefined in this case.

A write operation is started by writing the 16-bit data, PHY address and register address to the MDIO Control register and setting the write bit. The operation is finished when the busy bit is cleared and it was successful if the Linkfail bit is zero.

42.5.1 PHY interrupts

The core also supports status change interrupts from the PHY. A level sensitive interrupt signal can be connected on the mdint input. The mdint_pol vhdl generic can be used to select the polarity. The PHY status change bit in the status register is set each time an event is detected in this signal. If the PHY status interrupt enable bit is set at the time of the event the core will also generate an interrupt on the AHB bus.

42.6 Ethernet Debug Communication Link (EDCL)

The EDCL provides access to an on-chip AHB bus through Ethernet. It uses the UDP, IP and ARP protocols together with a custom application layer protocol. The application layer protocol uses an ARQ algorithm to provide reliable AHB instruction transfers. Through this link, a read or write transfer can be generated to any address on the AHB bus. The EDCL is optional and must be enabled with a generic.

42.6.1 Operation

The EDCL receives packets in parallel with the MAC receive DMA channel. It uses a separate MAC address which is used for distinguishing EDCL packets from packets destined to the MAC DMA channel. The EDCL also has an IP address which is set through generics. Since ARP packets use the Ethernet broadcast address, the IP-address must be used in this case to distinguish between EDCL ARP packets and those that should go to the DMA-channel. Packets that are determined to be EDCL packets are not processed by the receive DMA channel.

When the packets are checked to be correct, the AHB operation is performed. The operation is performed with the same AHB master interface that the DMA-engines use. The replies are automatically sent by the EDCL transmitter when the operation is finished. It shares the Ethernet transmitter with the transmitter DMA-engine but has higher priority.

42.6.2 EDCL protocols

The EDCL accepts Ethernet frames containing IP or ARP data. ARP is handled according to the protocol specification with no exceptions.

IP packets carry the actual AHB commands. The EDCL expects an Ethernet frame containing IP, UDP and the EDCL specific application layer parts. Table 590 shows the IP packet required by the EDCL. The contents of the different protocol headers can be found in TCP/IP literature.

*Table 590.*The IP packet expected by the EDCL.

Ethernet Header	IP Header	UDP Header	2 B Offset	4 B Control word	4 B Address	Data 0 - 242 4B Words	Ethernet CRC

The following is required for successful communication with the EDCL: A correct destination MAC address as set by the generics, an Ethernet type field containing 0x0806 (ARP) or 0x0800 (IP). The IP-address is then compared with the value determined by the generics for a match. The IP-header checksum and identification fields are not checked. There are a few restrictions on the IP-header fields. The version must be four and the header size must be 5 B (no options). The protocol field must

always be 0x11 indicating a UDP packet. The length and checksum are the only IP fields changed for the reply.

The EDCL only provides one service at the moment and it is therefore not required to check the UDP port number. The reply will have the original source port number in both the source and destination fields. UDP checksum are not used and the checksum field is set to zero in the replies.

The UDP data field contains the EDCL application protocol fields. Table 591 shows the application protocol fields (data field excluded) in packets received by the EDCL. The 16-bit offset is used to align the rest of the application layer data to word boundaries in memory and can thus be set to any value. The R/W field determines whether a read (0) or a write(1) should be performed. The length

*Table 591.*The EDCL application layer fields in received frames.

16-bit Offset	14-bit Sequence number	1-bit R/W	10-bit Length	7-bit Unused

field contains the number of bytes to be read or written. If R/W is one the data field shown in Table 590 contains the data to be written. If R/W is zero the data field is empty in the received packets. Table 592 shows the application layer fields of the replies from the EDCL. The length field is always zero for replies to write requests. For read requests it contains the number of bytes of data contained in the data field.

*Table 592.*The EDCL application layer fields in transmitted frames.

16-bit Offset	14-bit sequence number	1-bit ACK/NAK	10-bit Length	7-bit Unused

The EDCL implements a Go-Back-N algorithm providing reliable transfers. The 14-bit sequence number in received packets are checked against an internal counter for a match. If they do not match, no operation is performed and the ACK/NAK field is set to 1 in the reply frame. The reply frame contains the internal counter value in the sequence number field. If the sequence number matches, the operation is performed, the internal counter is incremented, the internal counter value is stored in the sequence number field and the ACK/NAK field is set to 0 in the reply. The length field is always set to 0 for ACK/NAK=1 frames. The unused field is not checked and is copied to the reply. It can thus be set to hold for example some extra id bits if needed.

42.6.3 EDCL IP and Ethernet address settings

The default value of the EDCL IP and MAC addresses are set by `ipaddrh, ipaddrl, macaddrh and macaddrl` generics. The IP address can later be changed by software, but the MAC address is fixed. To allow several EDCL enabled GRETH controllers on the same sub-net, the 4 LSB bits of the IP and MAC address can optionally be set by an input signal. This is enabled by setting the `edcl` generic = 2, and driving the 4-bit LSB value on ethi.edcladdr.

42.6.4 EDCL buffer size

The EDCL has a dedicated internal buffer memory which stores the received packets during processing. The size of this buffer is configurable with a VHDL generic to be able to obtain a suitable compromise between throughput and resource utilization in the hardware. Table 593 lists the different buffer configurations. For each size the table shows how many concurrent packets the EDCL can handle, the maximum size of each packet including headers and the maximum size of the data payload.

Sending more packets before receiving a reply than specified for the selected buffer size will lead to dropped packets. The behavior is unspecified if sending larger packets than the maximum allowed.

*Table 593.*EDCL buffer sizes

Total buffer size (kB)	Number of packet buffers	Packet buffer size (B)	Maximum data payload (B)
1	4	256	200
2	4	512	456
4	8	512	456
8	8	1024	968
16	16	1024	968
32	32	1024	968
64	64	1024	968

42.7 Media Independent Interfaces

There are several interfaces defined between the MAC sublayer and the Physical layer. The GRETH_GBIT supports the Media Independent Interface (MII) and the Gigabit Media Independent Interface (GMII).

The GMII is used in 1000 Mbit mode and the MII in 10 and 100 Mbit. These interfaces are defined separately in the 802.3-2002 standard but in practice they share most of the signals. The GMII has 9 additional signals compared to the MII. Four data signals are added to the receiver and transmitter data interfaces respectively and a new transmit clock for the gigabit mode is also introduced.

To support lower speed where the operation and clock frequency of the core and phy remains unchanged i.e. running at 100Mb/s when the IP is configured for 1000Mb/s speed enable signals should be created to mimic the desired bit rate.

When operating at 100Mb/s, every byte of the MAC frame is repeated 10 clock periods to achieve the correct bit rate. The GRETH_GBIT core does not take care of this operation and enable signals with toggling frequency of the correct bit rate needs to be created.

When operating at 10Mb/s, every byte of the MAC frame is repeated 100 clock periods to achieve the correct bit rate. The GRETH_GBIT core does not take care of this operation and enable signals with toggling frequency of the correct bit rate needs to be created.

*Table 594.*Signals in GMII and MII.

MII and GMII	**GMII Only**
txd[3:0]	txd[7:4]
tx_en	rxd[7:4]
tx_er	gtx_clk
rx_col	
rx_crs	
rxd[3:0]	
rx_clk	
rx_er	
rx_dv	
rx_en	
tx_dv	

42.8 Registers

The core is programmed through registers mapped into APB address space.

*Table 595.*GRETH_GBIT registers

APB address offset	Register
0x00	Control register
0x04	Status/Interrupt-source register
0x08	MAC Address MSB
0x0C	MAC Address LSB
0x10	MDIO Control/Status
0x14	Transmit descriptor pointer
0x18	Receiver descriptor pointer
0x1C	EDCL IP
0x20	Hash table msb
0x24	Hash table lsb
0x28	EDCL MAC address MSB
0x2C	EDCL MAC address LSB
0x10000 - 0x107FC	Transmit RAM buffer debug access
0x20000 - 0x207FC	Receiver RAM buffer debug access
0x30000 - 0x3FFFC	EDCL buffer debug access

42.8.1 Control register

*Table 596.*0x00 - CTRL - GRETH control register

31	30 28	27	26	25	24 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EA	BS	GA	MA	MC	RESERVED	ED	RD	DD	ME	PI	BM	GB	SP	RS	PM	FD	RI	TI	RE	TE
*	*	*	*	*	0	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	wc	rw	rw	rw	rw	rw	rw

31 EDCL available (EA) - Set to one if the EDCL is available.

30: 28 EDCL buffer size (BS) - Shows the amount of memory used for EDCL buffers. 0 = 1 kB, 1 = 2 kB, ..., 6 = 64 kB.

27 Gigabit MAC available (GA) - This bit always reads as a 1 and indicates that the MAC has 1000 Mbit capability.

26 Mdio interrupts enabled (ME) - Set to one when the core supports mdio interrupts. Read only.

25 Multicast available (MC) - Set to one when the core supports multicast address reception. Read only.

24: 15 RESERVED

14 EDCL Disable(ED) - Set to one to disablethe EDCL and zero to enable it. Reset value taken from the ethi.edcldisable signal. Only available if the EDCL hardware is present in the core.

13 RAM debug enable (RD) - Set to one to enable the RAM debug mode. Reset value: ‘0’. Only available if the VHDL generic ramdebug is nonzero.

12 Disable duplex detection (DD) - Disable the EDCL speed/duplex detection FSM. If the FSM cannot complete the detection the MDIO interface will be locked in busy mode. If software needs to access the MDIO the FSM can be disabled here and as soon as the MDIO busy bit is 0 the interface is available. Note that the FSM cannot be reenabled again.

11 Multicast enable (ME) - Enable reception of multicast addresses. Reset value: ‘0’.

10 PHY status change interrupt enable (PI) - Enables interrupts for detected PHY status changes.

9 Burstmode (BM) - When set to 1, transmissions use burstmode in 1000 Mbit Half-duplex mode (GB=1, FD = 0). When 0 in this speed mode normal transmissions are always used with extension inserted. Operation is undefined when set to 1 in other speed modes. Reset value: ‘0’.

8 Gigabit (GB) - 1 sets the current speed mode to 1000 Mbit and when set to 0, the speed mode is selected with bit 7 (SP). Reset value: ‘0’.

7 Speed (SP) - Sets the current speed mode. 0 = 10 Mbit, 1 = 100 Mbit. Must not be set to 1 at the same time as bit 8 (GB). Reset valuie: ‘0’.

6 Reset (RS) - A one written to this bit resets the GRETH_GBIT core. Self clearing. No other accesses should be done .to the slave interface other than polling this bit until it is cleared.

5 Promiscuous mode (PM) - If set, the GRETH_GBIT operates in promiscuous mode which means it will receive all packets regardless of the destination address. Reset value: ‘0’.

4 Full duplex (FD) - If set, the GRETH_GBIT operates in full-duplex mode otherwise it operates in half-duplex. Reset value: ‘0’.

3 Receiver interrupt (RI) - Enable Receiver Interrupts. An interrupt will be generated each time a packet is received when this bit is set. The interrupt is generated regardless if the packet was received successfully or if it terminated with an error. Reset value: ‘0’.

2 Transmitter interrupt (TI) - Enable Transmitter Interrupts. An interrupt will be generated each time a packet is transmitted when this bit is set. The interrupt is generated regardless if the packet was transmitted successfully or if it terminated with an error. Reset value: ‘0’.

1 Receive enable (RE) - Should be written with a one each time new descriptors are enabled. As long as this bit is one the GRETH_GBIT will read new descriptors and as soon as it encounters a disabled descriptor it will stop until RE is set again. This bit should be written with a one after the new descriptors have been enabled. Reset value: ‘0’.

0 Transmit enable (TE) - Should be written with a one each time new descriptors are enabled. As long as this bit is one the GRETH_GBIT will read new descriptors and as soon as it encounters a disabled descriptor it will stop until TE is set again. This bit should be written with a one after the new descriptors have been enabled. Reset value: ‘0’.

42.8.2 Status Register

*Table 597.*0x04 - STAT - GRETH_GBIT status register.

31 9	8	7	6	5	4	3	2	1	0
RESERVED	PS	IA	TS	TA	RA	TI	RI	TE	RE
0	0	0	0	NR	NR	NR	NR	NR	NR
r	wc	wc	wc	wc	wc	wc	wc	wc	wc

31: 9 RESERVED

8 PHY status changes (PS) - Set each time a PHY status change is detected.

7 Invalid address (IA) - A packet with an address not accepted by the MAC was received. Cleared when written with a one. Reset value: ‘0’.

6 Too small (TS) - A packet smaller than the minimum size was received. Cleared when written with a one. Reset value: ‘0’.

5 Transmitter AHB error (TA) - An AHB error was encountered in transmitter DMA engine. Cleared when written with a one. Not Reset.

4 Receiver AHB error (RA) - An AHB error was encountered in receiver DMA engine. Cleared when written with a one. Not Reset.

3 Transmit successful (TI) - A packet was transmitted without errors. Cleared when written with a one. Not Reset.

2 Receive successful (RI) - A packet was received without errors. Cleared when written with a one. Not Reset.

1 Transmitter error (TE) - A packet was transmitted which terminated with an error. Cleared when written with a one. Not Reset.

0 Receiver error (RE) - A packet has been received which terminated with an error. Cleared when written with a one. Not Reset.

42.8.3 Mac Address MSB

*Table 598.*0x08 - MACMSB - GRETH_GBIT MAC address MSB.

31 16	15 0
RESERVED	Bit 47 downto 32 of the MAC Address
0	DR
r	rw

31: 16 RESERVED

15: 0 The two most significant bytes of the MAC Address. Not Reset.

42.8.4 Mac Address LSB

*Table 599.*0x0C - MACLSB - GRETH_GBIT MAC address LSB.

31 0
Bit 31 downto 0 of the MAC Address
NR
rw

31: 0 The 4 least significant bytes of the MAC Address. Not Reset.

42.8.5 MDIO control/status Register

*Table 600.*0x10 - MDIO - GRETH_GBIT MDIO control/status register.

31 16	15 11	10 5	4	3	2	1	0
DATA	PHYADDR	REGADDR	RES	BU	LF	RD	WR
0	*	0		0	1	0	0
rw	rw	rw		r	r	rw	rw

31: 16 Data (DATA) - Contains data read during a read operation and data that is transmitted is taken from this field. Reset value: 0x0000.

15: 11 PHY address (PHYADDR) - This field contains the address of the PHY that should be accessed during a write or read operation. Reset value: “00000”.

10: 6 Register address (REGADDR) - This field contains the address of the register that should be accessed during a write or read operation. Reset value: ‘”00000”.

5: 4 RESERVED

3 Busy (BU) - When an operation is performed this bit is set to one. As soon as the operation is finished and the management link is idle this bit is cleared. Reset value: ‘0’.

2 Linkfail (LF) - When an operation completes (BUSY = 0) this bit is set if a functional management link was not detected. Reset value: ‘1’.

1 Read (RD) - Start a read operation on the management interface. Data is stored in the data field. Reset value: ‘0’.

0 Write (WR) - Start a write operation on the management interface. Data is taken from the Data field. Reset value: ‘0’.

42.8.6 Transmitter Descripter Table Base Address Register

*Table 601.*0x14 - TXBASE - GRETH_GBIT transmitter descriptor table base address register.

31 10	9 3	2 0
BASEADDR	DESCPNT	RES
NR	0	0
rw	rw	r

31: 10 Transmitter descriptor table base address (BASEADDR) - Base address to the transmitter descriptor table.Not Reset.

9: 3 Descriptor pointer (DESCPNT) - Pointer to individual descriptors. Automatically incremented by the Ethernet MAC.

2: 0 RESERVED

42.8.7 Receiver Descriptor Table Base Address Register

*Table 602.*0x18 - RXBASE - GRETH_GBIT receiver descriptor table base address register.

31 10	9 3	2 0
BASEADDR	DESCPNT	RES
NR	0	0
rw	rw	r

31: 10 Receiver descriptor table base address (BASEADDR) - Base address to the receiver descriptor table.Not Reset.

9: 3 Descriptor pointer (DESCPNT) - Pointer to individual descriptors. Automatically incremented by the Ethernet MAC.

2: 0 RESERVED

42.8.8 IP Register

*Table 603.*0x1C - EDCLIP - GRETH_GBIT EDCL IP register

31	0
EDCL IP ADDRESS	
0	
rw	

31: 0 EDCL IP address. Reset value is set with the ipaddrh and ipaddrl generics.

42.8.9 Hash Table MSB Register

*Table 604.*0x20 - HMSB - GRETH Hash table MSB register

31	0
Hash table (64:32)	
NR	
rw	

31: 0 Hash table msb. Bits 64 downto 32 of the hash table.

42.8.10 Hash Table LSB Register

*Table 605.*0x24 - HLSB - GRETH Hash table LSB register

31	0
Hash table (64:32)	
NR	
rw	

31: 0 Hash table lsb. Bits 31downto 0 of the hash table.

42.8.11 MAC Address MSB

*Table 606.*0x28 - EMACMSB - GRETH_GBIT EDCL MAC address MSB.

31 16	15 0
RESERVED	Bit 47 downto 32 of the EDCL MAC Address
0	*
r	rw

31: 16 RESERVED

15: 0 The two most significant bytes of the EDCL MAC Address. Hardcoded reset value set with the VHDL generic macaddrh.

42.8.12 Mac Address LSB

*Table 607.*0x2C - EMACLSB - GRETH_GBIT EDCL MAC address LSB.

31	0
Bit 31 downto 0 of the EDCL MAC Address	
*	
rw	

31: 0 The 4 least significant bytes of the EDCL MAC Address. Hardcoded reset value set with the VHDL generics macaddrh and macaddrl. If the VHDL generic edcl is set to 2 bits 3 downto 0 are set with the edcladdr input signal.

42.9 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x01D. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

42.10 Implementation

42.10.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers, except synchronization registers, if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core will use asynchronous reset for all registers if the GRLIB config package setting *grlib_async_reset_enable* is set.

42.11 Configuration options

Table 608 shows the configuration options of the core (VHDL generics).*) Not all addresses are allowed and most NICs and protocol implementations will discard frames with illegal addresses silently. Consult network literature if unsure about the addresses.

*Table 608.*Configuration options

Generic	Function	Allowed range	Default
hindex	AHB master index.	0 - NAHBMST-1	0
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	Addr field of the APB bar.	0 - 16#FFF#	0
pmask	Mask field of the APB bar.	0 - 16#FFF#	16#FFF#
pirq	Interrupt line used by the GRETH.	0 - NAHBIRQ-1	0
memtech	Memory technology used for the FIFOs.	0 - NTECH	inferred
ifg_gap	Number of ethernet clock cycles used for one interframe gap. Default value as required by the standard. Do not change unless you know what your doing.	1 - 255	24
attempt_limit	Maximum number of transmission attempts for one packet. Default value as required by the standard.	1 - 255	16
backoff_limit	Limit on the backoff size of the backoff time. Default value as required by the standard. Sets the number of bits used for the random value. Do not change unless you know what your doing.	1 - 10	10
slot_time	Number of ethernet clock cycles used for one slot- time. Default value as required by the ethernet standard. Do not change unless you know what you are doing.	1 - 255	128
mdcscaler	Sets the divisor value use to generate the mdio clock (mdc). The mdc frequency will be clk/(2*(mdcscaler+1)).	0 - 255	25
nsync	Number of synchronization registers used.	1 - 2	2
edcl	Enable EDCL. 0 = disabled. 1 = enabled. 2 = enabled and 4-bit LSB of IP and ethernet MAC address programmed by ethi.edcladdr, 3=in addition to features for value 2 the reset value for the EDCL disable bit is taken from the ethi.edcldisable signal instead of being hardcoded to 0. 4=in addition to features for value 2 and 3 the an option is given to disable the EDCL via external input signal.	0 - 4	0
edclbufsz	Select the size of the EDCL buffer in kB.	1 - 64	1
burstlength	Sets the maximum burstlength used during DMA	4 - 128	32

*Table 608.*Configuration options

Generic	Function	Allowed range	Default
macaddrh	Sets the upper 24 bits of the EDCL MAC address. Not all addresses are allowed and most NICs and protocol implementations will discard frames with illegal addresses silently. Consult network literature if unsure about the addresses.	0 - 16#FFFFFF#	16#00005E#
macaddrl	Sets the lower 24 bits of the EDCL MAC address. Not all addresses are allowed and most NICs and protocol implementations will discard frames with illegal addresses silently. Consult network literature if unsure about the addresses.	0 - 16#FFFFFF#	16#000000#
ipaddrh	Sets the upper 16 bits of the EDCL IP address reset value.	0 - 16#FFFF#	16#C0A8#
ipaddrl	Sets the lower 16 bits of the EDCL IP address reset value.	0 - 16#FFFF#	16#0035#
phyrstadr	Sets the reset value of the PHY address field in the MDIO register. When set to 32, the address is taken from the ethi.phyrstaddr signal.	0 - 32	0
sim	Set to 1 for simulations and 0 for synthesis. 1 selects a faster mdc clock to speed up simulations.	0 - 1	0
mdint_pol	Selects polarity for level sensitive PHY interrupt line. 0 = active low, 1 = active high	0 - 1	0
enable_mdint	Enables mdio interrupts.	0 - 1	0
multicast	Enables multicast support.	0 - 1	0
ramdebug	Enables debug access to the core's RAM blocks through the APB interface. 1=enables access to the receiver and transmitter RAM buffers, 2=enables access to the EDCL buffers in addition to the functionality of value 1. Setting this generic to 2 will have no effect if the edcl generic is 0.	0 - 2	0
ehindex	AHB master index for the separate EDCL master interface. Only used if edclsepahb is 1.	0 - NAHBMST-1	0
edclsepahb	Enables separate EDCL AHB master interface. A signal determines if the separate interface or the common interface is used. Only available in the GRETH_GBIT_MB version of the core.	0 - 1	0
mdiohold	Set output hold time for MDIO in number of AHB cycles. Should be 10 ns or more.	1 - 30	1
gmiimode	Enable the use of receive and transmit valid signals to enter data to/from the PHY at the correct rate.	0-1	0

42.12 Signal descriptions

Table 609 shows the interface signals of the core (VHDL ports).

*Table 609.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
AHBMI	*	Input	AMB master input signals	-
AHBMO	*	Output	AHB master output signals	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-

*Table 609.*Signal descriptions

Signal name	Field	Type	Function	Active
ETHI	gtx_clk	Input	Ethernet gigabit transmit clock.	-
	rmii_clk	Input	Ethernet RMII clock.	-
	tx_clk	Input	Ethernet transmit clock.	-
	tx_dv	Input	Ethernet transmitter enable	-
	rx_clk	Input	Ethernet receive clock.	-
	rxd	Input	Ethernet receive data.	-
	rx_dv	Input	Ethernet receive data valid.	High
	rx_er	Input	Ethernet receive error.	High
	rx_col	Input	Ethernet collision detected. (Asynchronous, sampled with tx_clk)	High
	rx_crs	Input	Ethernet carrier sense. (Asynchronous, sampled with tx_clk)	High
	rx_en	Input	Ethernet receiver enable.	-
	mdio_i	Input	Ethernet management data input	-
	mdint	Input	Ethernet management interrupt	-
	phyrstaddr	Input	Reset address for GRETH PHY address field.	-
	edcldis	Input	Disable EDCL functionality	-
	edcladdr	Input	Sets the four least significant bits of the EDCL MAC address and the EDCL IP address when the edcl generic is set to 2.	-
	edclsepahb	Input	Selects AHB master interface for the EDCL. ‘0’ selects the common interface and ‘1’ selects the separate interface. Only available in the GRETH_GBIT_MB version of the core when the VHDL generic edclsepahb is set to 1.	-
	edcldisable	Input	Reset value for edcl disable register bit. Setting the signal to 1 disables the EDCL at reset and 0 enables it.	-
ETHO	reset	Output	Ethernet reset (asserted when the MAC is reset).	Low
	txd	Output	Ethernet transmit data.	-
	tx_en	Output	Ethernet transmit enable.	High
	tx_er	Output	Ethernet transmit error.	High
	mdc	Output	Ethernet management data clock.	-
	mdio_o	Output	Ethernet management data output.	-
	mdio_oe	Output	Ethernet management data output enable.	Set by the oepol generic.
MTESTI**	BUF	Input	Memory BIST input signal to buffer RAM	-
	EDCL	Input	Memory BIST input signal to EDCL RAM	-
MTESTO**	BUF	Output	Memory BIST output signal from buffer RAM	-
	EDCL	Output	Memory BIST output signal from EDCL RAM	-
MTESTCLK**	N/A	Input	Memory BIST clock	-

* see GRLIB IP Library User’s Manual

** not available in FPGA releases

42.13 Library dependencies

Table 610 shows libraries used when instantiating the core (VHDL libraries).

*Table 610.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	ETHERNET_MAC	Signals, component	GRETH_GBIT component declarations, GRETH_GBIT signals.
GAISLER	NET	Signals	Ethernet signals

42.14 Instantiation

The first example shows how the non-mb version of the core can be instantiated and the second one show the mb version.

42.14.1 Non-MB version

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.ethernet_mac.all;

entity greth_ex is
  port (
    clk  : in std_ulogic;
    rstn : in std_ulogic;

    -- ethernet signals
    ethi :  in  eth_in_type;
    etho :  in  eth_out_type
    );
end;

architecture rtl of greth_ex is

  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);

begin

  -- AMBA Components are instantiated here
  ...

  -- GRETH
  e1 : greth_gbit
    generic map(
     hindex       => 0,
     pindex       => 12,
     paddr        => 12,
     pirq         => 12,
     memtech      => inferred,
     mdcscaler    => 50,
     burstlength  => 32,
     nsync        => 1,
     edcl         => 1,
```

```
     edclbufsz    => 8,
     macaddrh     => 16#00005E#,
     macaddrl     => 16#00005D#,
     ipaddrh      => 16#c0a8#,
     ipaddrl      => 16#0035#)
 port map(
   rst          => rstn,
   clk          => clk,
   ahbmi        => ahbmi,
   ahbmo        => ahbmo(0),
   apbi         => apbi,
   apbo         => apbo(12),
   ethi         => ethi,
   etho         => etho
   );
end;
```

42.14.2 MB version

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.ethernet_mac.all;

entity greth_ex is
  port (
    clk  : in std_ulogic;
    rstn : in std_ulogic;

    -- ethernet signals
    ethi :  in  eth_in_type;
    etho :  in  eth_out_type
    );
end;

architecture rtl of greth_ex is

  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);
begin

  -- AMBA Components are instantiated here
  ...

  -- GRETH
  e1 : greth_gbit_mb
    generic map(
     hindex       => 0,
     pindex       => 12,
     paddr        => 12,
     pirq         => 12,
     memtech      => inferred,
     mdcscaler    => 50,
     burstlength  => 32,
     nsync        => 1,
     edcl         => 1,
     edclbufsz    => 8,
     macaddrh     => 16#00005E#,
     macaddrl     => 16#00005D#,
     ipaddrh      => 16#c0a8#,
     ipaddrl      => 16#0035#,
     ehindex      => 1
```

```
      edclsepahb   => 1)
  port map(
    rst           => rstn,
    clk           => clk,
    ahbmi         => ahbmi,
    ahbmo         => ahbmo(0),
    ahbmi2        => ahbmi,
    ahbmo2        => ahbmo(1),
    apbi          => apbi,
    apbo          => apbo(12),
    ethi          => ethi,
    etho          => etho
    );
end;
```

43 GRFIFO - FIFO Interface

43.1 Overview

The FIFO interface is assumed to operate in an AMBA bus system where both the AMBA AHB bus and the APB bus are present. The AMBA APB bus is used for configuration, control and status handling. The AMBA AHB bus is used for retrieving and storing FIFO data in memory external to the FIFO interface. This memory can be located on-chip or external to the chip.

The FIFO interface supports transmission and reception of blocks of data by use of circular buffers located in memory external to the core. Separate transmit and receive buffers are assumed. Reception and transmission of data can be ongoing simultaneously.

After a data transfer has been set up via the AMBA APB interface, the DMA controller initiates a burst of read accesses on the AMBA AHB bus to fetch data from memory that are performed by the AHB master. The data are then written to the external FIFO. When a programmable amount of data has been transmitted, the DMA controller issues an interrupt.

After reception has been set up via the AMBA APB interface, data are read from the external FIFO. To store data to memory, the DMA controller initiates a burst of write accesses on the AMBA AHB bus that are performed by the AHB master. When a programmable amount of data has been received, the DMA controller issues an interrupt.

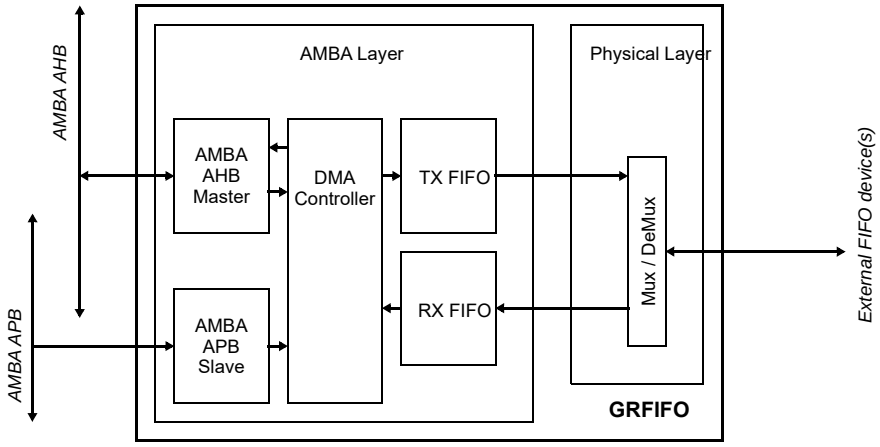


Figure 125. Block diagram

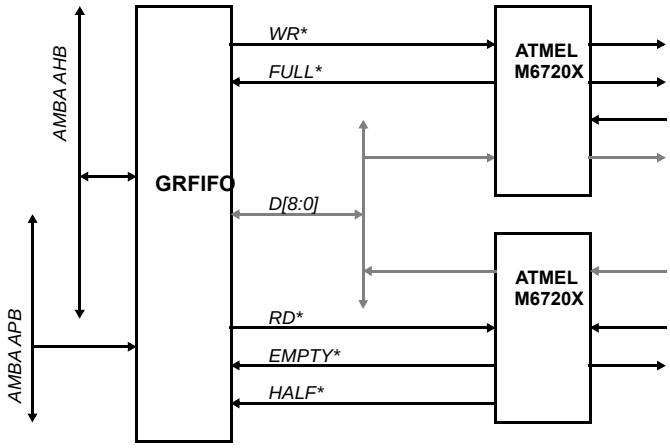


Figure 126. Example of usage, with shared external data bus

43.1.1 Function

The core implements the following functions:

- data transmission to external FIFO
- circular transmit buffer
- direct memory access for transmitter
- data reception from external FIFO
- circular receive buffer for receiver
- direct memory access
- automatic 8- and 16-bit data width conversion
- general purpose input output

43.1.2 Transmission

Data to be transferred via the FIFO interface are fetched via the AMBA AHB master interface from on-chip or off-chip memory. This is performed by means of direct memory access (DMA), implementing a circular transmit buffer in the memory. The transmit channel is programmable via the AMBA APB slave interface, which is also used for the monitoring of the FIFO and DMA status.

The transmit channel is programmed in terms of a base address and size of the circular transmit buffer. The outgoing data are stored in the circular transmit buffer by the system. A write address pointer register is then set by the system to indicate the last byte written to the circular transmit buffer. An interrupt address pointer register is used by the system to specify a location in the circular transmit buffer from which a data read should cause an interrupt to be generated.

The FIFO interface automatically indicates with a read address pointer register the location of the last fetched byte from the circular transmit buffer. Read accesses are performed as incremental bursts, except when close to the location specified by the interrupt pointer register at which point the last bytes might be fetched by means of single accesses.

Data transferred via the FIFO interface can be either 8- or 16-bit wide. The handling of the transmit channel is however the same. All transfers performed by the AMBA AHB master are 32-bit word based. No byte or half-word transfers are performed.

To handle the 8- and 16-bit FIFO data width, a 32-bit read access might carry less than four valid bytes. In such a case, the remaining bytes are ignored. When additional data are available in the circular transmit buffer, the previously fetched bytes will be re-read together with the newly written bytes to form the 32-bit data. Only the new bytes will be transmitted to the FIFO, not to transmit the same byte more than once. The aforementioned write address pointer indicates what bytes are valid.

An interrupt is generated when the circular transmit buffer is empty. The status of the external FIFO is observed via the AMBA APB slave interface, indicating Full Flag and Half-Full Flag.

43.1.3 Reception

Data received via the FIFO interface are stored via the AMBA AHB master interface to on-chip or off-chip memory. This is performed by means of direct memory access (DMA), implementing a circular receive buffer in the memory. The receive channel is programmable via the AMBA APB slave interface, which is also used for the monitoring of the FIFO and DMA status.

The receive channel is programmed in terms of a base address and size of the circular receive buffer. The incoming data are stored in the circular receive buffer. The interface automatically indicates with a write address pointer register the location of the last stored byte. A read address pointer register is used by the system to indicate the last byte read from the circular receive buffer. An interrupt address pointer register is used by the system to specify a location in the circular receive buffer to which a data write should cause an interrupt to be generated.

Write accesses are performed as incremental bursts, except when close to the location specified by the interrupt pointer register at which point the last bytes might be stored by means of single accesses.

Data transferred via the FIFO interface can be either 8- or 16-bit wide. The handling of the receive channel is however the same. All transfers performed by the AMBA AHB master are 32-bit word based. No byte or half-word transfers are performed.

To handle the 8- and 16-bit FIFO data width, a 32-bit write access might carry less than four valid bytes. In such a case, the remaining bytes will all be zero. When additional data are received from the FIFO interface, the previously stored bytes will be re-written together with the newly received bytes to form the 32-bit data. In this way, the previously written bytes are never overwritten. The aforementioned write address pointer indicates what bytes are valid.

An interrupt is generated when the circular receive buffer is full. If more FIFO data are available, they will not be moved to the circular receive buffer. The status of the external FIFO is observed via the AMBA APB slave interface, indicating Empty Flag and Half-Full Flag.

43.1.4 General purpose input output

Data input and output signals unused by the FIFO interface can be used as general purpose input output, providing 0, 8 or 16 individually programmable channels.

43.1.5 Interfaces

The core provides the following external and internal interfaces:

- FIFO interface
- AMBA AHB master interface, with sideband signals as per [GLRIB] including:
- cachability information
- interrupt bus
- configuration information
- diagnostic information
- AMBA APB slave interface, with sideband signals as per [GLRIB] including:
- interrupt bus
- configuration information
- diagnostic information

The interface is intended to be used with the following FIFO devices from ATMEL:

Name:Type:

M67204H4K x 9 FIFOESA/SCC 9301/049, SMD/5962-89568

M67206H16K x 9 FIFOESA/SCC 9301/048, SMD/5962-93177

M672061H16K x 9 FIFO ESA/SCC 9301/048, SMD/5962-93177

43.2 Interface

The external interface supports one or more FIFO devices for data output (transmission) and/or one or more FIFO devices for data input (reception). The external interface supports FIFO devices with 8- and 16-bit data width. Note that one device is used when 8-bit and two devices are used when 16-bit data width is needed. The data width is programmable. Note that this is performed commonly for both directions.

The external interface supports one parity bit over every 8 data bits. Note that there can be up to two parity bits in either direction. The parity is programmable in terms of odd or even parity. Note that odd parity is defined as an odd number of logical ones in the data bits and parity bit. Note that even parity is defined as an even number of logical ones in the data bits and parity bit. Parity is generated for write accesses to the external FIFO devices. Parity is checked for read accesses from the external FIFO devices and a parity failure results in an internal interrupt.

The external interface provides a Write Enable output signal. The external interface provides a Read Enable output signal. The timing of the access towards the FIFO devices is programmable in terms of wait states based on system clock periods.

The external interface provides an Empty Flag input signal, which is used for flow-control during the reading of data from the external FIFO, not reading any data while the external FIFO is empty. Note that the Empty Flag is sampled at the end of the read access to determine if the FIFO is empty. To determine when the FIFO is not empty, the Empty Flag is re-synchronized with Clk.

The external interface provides a Full Flag input signal, which is used for flow-control during the writing of data to the external FIFO, not writing any data while the external FIFO is full. Note that the Full Flag is sampled at the end of the write access to determine if the FIFO is full. To determine when the FIFO is not full, the Full Flag is re-synchronized with Clk.

The external interface provides a Half-Full Flag input signal, which is used as status information only.

The data input and output signals are possible to use as general purpose input output channels. This need is only realized when the data signals are not used by the FIFO interface. Each general purpose input output channel is individually programmed as input or output. The default reset configuration for each general purpose input output channel is as input. The default reset value each general purpose input output channel is logical zero. Note that protection toward spurious pulse commands during power up shall be mitigated as far as possible by means of I/O cell selection from the target technology.

43.3 Waveforms

The following figures show read and write accesses to the FIFO with 0 and 4 wait states, respectively.

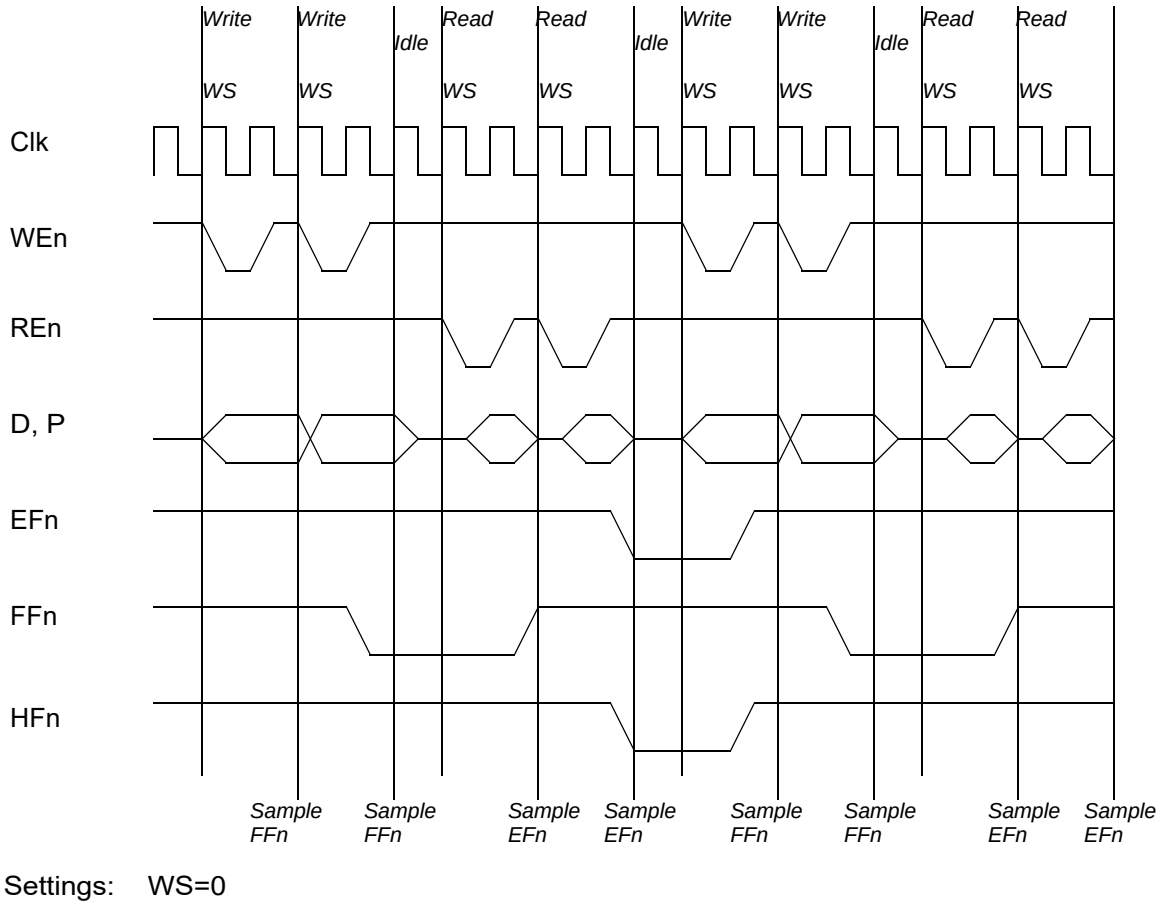


Figure 127. FIFO read and write access waveform, 0 wait states (WS)

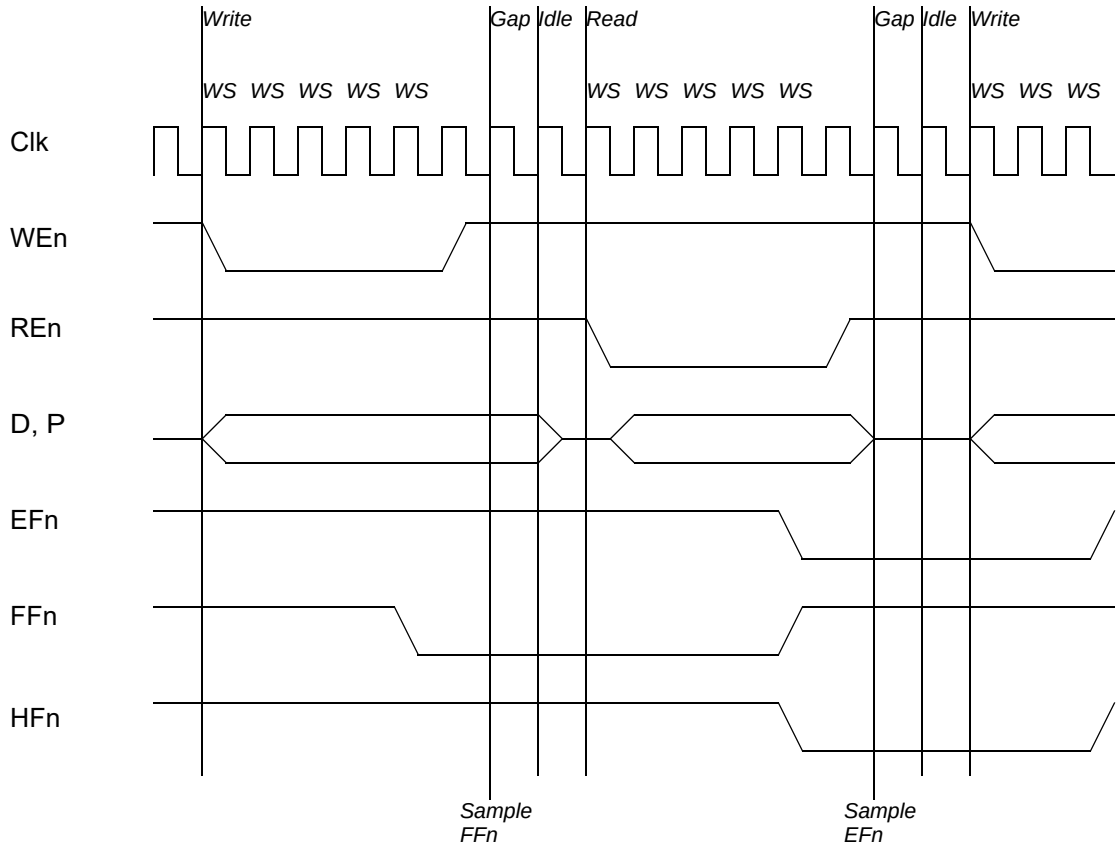


Figure 128. FIFO read and write access waveform, 4 wait states (WS)

43.4 Transmission

The transmit channel is defined by the following parameters:

- base address
- buffer size
- write pointer
- read pointer

The transmit channel can be enabled or disabled.

43.4.1 Circular buffer

The transmit channel operates on a circular buffer located in memory external to the FIFO controller. The circular buffer can also be used as a straight buffer. The buffer memory is accessed via the AMBA AHB master interface.

The size of the buffer is defined by the FifoTxSIZE.SIZE field, specifying the number of 64 byte blocks that fit in the buffer.

E.g. FifoTxSIZE.SIZE = 1 means 64 bytes fit in the buffer.

Note however that it is not possible to fill the buffer completely, leaving at least one word in the buffer empty. This is to simplify wrap-around condition checking.

E.g. FifoTxSIZE.SIZE = 1 means that 60 bytes fit in the buffer at any given time.

43.4.2 Write and read pointers

The write pointer (FifoTxWR.WRITE) indicates the position+1 of the last byte written to the buffer. The write pointer operates on number of bytes, not on absolute or relative addresses.

The read pointer (FifoTxRD.READ) indicates the position+1 of the last byte read from the buffer. The read pointer operates on number of bytes, not on absolute or relative addresses.

The difference between the write and the read pointers is the number of bytes available in the buffer for transmission. The difference is calculated using the buffer size, specified by the FifoTxSIZE.SIZE field, taking wrap around effects of the circular buffer into account.

Examples:

- There are 2 bytes available for transmit when FifoTxSIZE.SIZE=1, FifoTxWR.WRITE=2 and FifoTxRD.READ=0.
- There are 2 bytes available for transmit when FifoTxSIZE.SIZE=1, FifoTxWR.WRITE =0 and FifoTxRD.READ =62.
- There are 2 bytes available for transmit when FifoTxSIZE.SIZE=1, FifoTxWR.WRITE =1 and FifoTxRD.READ =63.
- There are 2 bytes available for transmit when FifoTxSIZE.SIZE=1, FifoTxWR.WRITE =5 and FifoTxRD.READ =3.

When a byte has been successfully written to the FIFO, the read pointer (FifoTxRD.READ) is automatically incremented, taking wrap around effects of the circular buffer into account. Whenever the write pointer FifoTxWR.WRITE and read pointer FifoTxRD.READ are equal, there are no bytes available for transmission.

43.4.3 Location

The location of the circular buffer is defined by a base address (FifoTxADDR.ADDR), which is an absolute address. The location of a circular buffer is aligned on a 1kbyte address boundary.

43.4.4 Transmission procedure

When the channel is enabled (FifoTxCTRL.ENABLE=1), as soon as there is a difference between the write and read pointer, a transmission will be started. Note that the channel should not be enabled if a potential difference between the write and read pointers could be created, to avoid the data transmission to start prematurely.

A data transmission will begin with a fetch of the data from the circular buffer to a local buffer in the FIFO controller. After a successful fetch, a write access will be performed to the FIFO.

The read pointer (FifoTxRD.READ) is automatically incremented after a successful transmission, taking wrap around effects of the circular buffer into account. If there is at least one byte available in the circular buffer, a new fetch will be performed.

If the write and read pointers are equal, no more prefetches and fetches will be performed, and transmission will stop.

Interrupts are provided to aid the user during transmission, as described in detail later in this section. The main interrupts are the TxError, TxEmpty and TxIrq which are issued on the unsuccessful transmission of a byte due to an error condition on the AMBA bus, when all bytes have been transmitted successfully and when a predefined number of bytes have been transmitted successfully.

Note that 32-bit wide read accesses past the address of the last byte or halfword available for transmission can be performed as part of a burst operation, although no read accesses are made beyond the circular buffer size.

All accesses to the AMBA AHB bus are performed as two consecutive 32-bit accesses in a burst, or as a single 32-bit access in case of an AMBA AHB bus error.

43.4.5 Straight buffer

It is possible to use the circular buffer as a straight buffer, with a higher granularity than the 1kbyte address boundary limited by the base address (FifoTxADDR.ADDR) field.

While the channel is disabled, the read pointer (FifoTxRD.READ) can be changed to an arbitrary value pointing to the first byte to be transmitted, and the write pointer (FifoTxWR.WRITE) can be changed to an arbitrary value.

When the channel is enabled, the transmission will start from the read pointer and continue to the write pointer.

43.4.6 AMBA AHB error

An AHB error response occurring on the AMBA AHB bus while data is being fetched will result in a TxError interrupt.

If the FifoCONF.ABORT bit is set to 0b, the channel causing the AHB error will re-try to read the data being fetched from memory till successful.

If the FifoCONF.ABORT bit is set to 1b, the channel causing the AHB error will be disabled (FifoTxCTRL.ENABLE is cleared automatically to 0 b). The read pointer can be used to determine which data caused the AHB error. The interface will not start any new write accesses to the FIFO. Any ongoing FIFO access will be completed and the FifoTxSTAT.TxOnGoing bit will be cleared. When the channel is re-enabled, the fetch and transmission of data will resume at the position where it was disabled, without losing any data.

43.4.7 Enable and disable

When an enabled transmit channel is disabled (FifoTxCTRL.ENABLE=0b), the interface will not start any new read accesses to the circular buffer by means of DMA over the AMBA AHB bus. No new write accesses to the FIFO will be started. Any ongoing FIFO access will be completed. If the

data is written successfully, the read pointer (FifoTxRD.READ) is automatically incremented and the FifoTxSTAT.TxOnGoing bit will be cleared. Any associated interrupts will be generated.

Any other fetched or pre-fetched data from the circular buffer which is temporarily stored in the local buffer will be discarded, and will be fetched again when the transmit channel is re-enabled.

The progress of the any ongoing access can be observed via the FifoTxSTAT.TxOnGoing bit. The FifoTxSTAT.TxOnGoing must be 0b before the channel can be re-configured safely (i.e. changing address, size or read/write pointers). It is also possible to wait for the TxEmpty interrupt described hereafter.

The channel can be re-enabled again without the need to re-configure the address, size and pointers. No data transmission is started while the channel is not enabled.

43.4.8 Interrupts

During transmission several interrupts can be generated:

- TxEmpty: Successful transmission of all data in buffer
- TxIrq: Successful transmission of a predefined number of data
- TxError: AHB access error during transmission

The TxEmpty and TxIrq interrupts are only generated as the result of a successful data transmission, after the FifoTxRD.READ pointer has been incremented.

43.5 Reception

The receive channel is defined by the following parameters:

- base address
- buffer size
- write pointer
- read pointer

The receive channel can be enabled or disabled.

43.5.1 Circular buffer

The receive channel operates on a circular buffer located in memory external to the FIFO controller. The circular buffer can also be used as a straight buffer. The buffer memory is accessed via the AMBA AHB master interface.

The size of the buffer is defined by the FifoRxSIZE.SIZE field, specifying the number 64 byte blocks that fit in the buffer.

E.g. FifoRxSIZE.SIZE=1 means 64 bytes fit in the buffer.

Note however that it is not possible for the hardware to fill the buffer completely, leaving at least two words in the buffer empty. This is to simplify wrap-around condition checking.

E.g. FifoRxSIZE.SIZE=1 means that 56 bytes fit in the buffer at any given time.

43.5.2 Write and read pointers

The write pointer (FifoRxWR.WRITE) indicates the position+1 of the last byte written to the buffer. The write pointer operates on number of bytes, not on absolute or relative addresses.

The read pointer (FifoRxRD.READ) indicates the position+1 of the last byte read from the buffer. The read pointer operates on number of bytes, not on absolute or relative addresses.

The difference between the write and the read pointers is the number of bytes available in the buffer for reception. The difference is calculated using the buffer size, specified by the FifoRxSIZE.SIZE field, taking wrap around effects of the circular buffer into account.

Examples:

- There are 2 bytes available for read-out when FifoRxSIZE.SIZE=1, FifoRxWR.WRITE =2 and FifoRxRD.READ=0.
- There are 2 bytes available for read-out when FifoRxSIZE.SIZE=1, FifoRxWR.WRITE =0 and FifoRxRD.READ=62.
- There are 2 bytes available for read-out when FifoRxSIZE.SIZE=1, FifoRxWR.WRITE =1 and FifoRxRD.READ=63.
- There are 2 bytes available for read-out when FifoRxSIZE.SIZE=1, FifoRxWR.WRITE =5 and FifoRxRD.READ=3.

When a byte has been successfully received and stored, the write pointer (FifoRxWR.WRITE) is automatically incremented, taking wrap around effects of the circular buffer into account.

43.5.3 Location

The location of the circular buffer is defined by a base address (FifoRxADDR.ADDR), which is an absolute address. The location of a circular buffer is aligned on a 1kbyte address boundary.

43.5.4 Reception procedure

When the channel is enabled (FifoRxCTRL.ENABLE=1), and there is space available for data in the circular buffer (as defined by the write and read pointer), a read access will be started towards the FIFO, and then an AMBA AHB store access will be started. The received data will be temporarily stored in a local store-buffer in the FIFO controller. Note that the channel should not be enabled until the write and read pointers are configured, to avoid the data reception to start prematurely

After a datum has been successfully stored the FIFO controller is ready to receive new data. The write pointer (FifoRxWR.WRITE) is automatically incremented, taking wrap around effects of the circular buffer into account.

Interrupts are provided to aid the user during reception, as described in detail later in this section. The main interrupts are the RxError, RxParity, RxFull and RxIrq which are issued on the unsuccessful reception of data due to an AMBA AHB error or parity error, when the buffer has been successfully filled and when a predefined number of data have been received successfully.

All accesses to the AMBA AHB bus are performed as two consecutive 32-bit accesses in a burst, or as a single 32-bit access in case of an AMBA AHB bus error.

43.5.5 Straight buffer

It is possible to use the circular buffer as a straight buffer, with a higher granularity than the 1kbyte address boundary limited by the base address (FifoRxADDR.ADDR) field.

While the channel is disabled, the write pointer (FifoRxWR.WRITE) can be changed to an arbitrary value pointing to the first data to be received, and the read pointer (FifoRxRD.READ) can be changed to an arbitrary value.

When the channel is enabled, the reception will start from the write pointer and continue to the read pointer.

43.5.6 AMBA AHB error

An AHB error response occurring on the AMBA AHB bus while data is being stored will result in an RxError interrupt.

If the FifoCONF.ABORT bit is set to 0b, the channel causing the AHB error will retry to store the received data till successful

If the FifoCONF.ABORT bit is set to 1b, the channel causing the AHB error will be disabled (FifoRxCTRL.ENABLE is cleared automatically to 0b). The write pointer can be used to determine which address caused the AHB error. The interface will not start any new read accesses to the FIFO. Any ongoing FIFO access will be completed and the data will be stored in the local receive buffer. The FifoRxSTAT.ONGOING bit will be cleared. When the receive channel is re-enabled, the reception and storage of data will resume at the position where it was disabled, without losing any data.

43.5.7 Enable and disable

When an enabled receive channel is disabled (FifoRxCTRL.ENABLE=0b), any ongoing data storage on the AHB bus will not be aborted, and no new storage will be started. If the data is stored successfully, the write pointer (FifoRxWR.WRITE) is automatically incremented. Any associated interrupts will be generated. The interface will not start any new read accesses to the FIFO. Any ongoing FIFO access will be completed.

The channel can be re-enabled again without the need to re-configure the address, size and pointers. No data reception is performed while the channel is not enabled.

The progress of the any ongoing access can be observed via the FifoRxSTAT.ONGOING bit. Note that the there might be data left in the local store-buffer in the FIFO controller. This can be observed via the FifoRxSTAT.RxByteCntr field. The data will not be lost if the channel is not reconfigured before re-enabled.

To empty this data from the local store-buffer to the external memory, the channel needs to be renabled. By setting the FifoRxIRQ.IRQ field to match the value of the FifoRxWR.WRITE field plus the value of the FifoRxSTAT.RxByteCntr field, an emptying to the external memory is forced of any data temporarily stored in the local store-buffer. Note however that additional data could be received in the local store-buffer when the channel is re-enabled.

The FifoRxSTAT.ONGOING must be 0b before the channel can be re-configured safely (i.e. changing address, size or read/write pointers).

43.5.8 Interrupts

During reception several interrupts can be generated:

- RxFull: Successful reception of all data possible to store in buffer
- RxIrq: Successful reception of a predefined number of data
- RxError: AHB access error during reception
- RxParity: Parity error during reception

The RxFull and RxIrq interrupts are only generated as the result of a successful data reception, after the FifoRxWR.WRITE pointer has been incremented.

43.6 Operation

43.6.1 Global reset and enable

When the FifoCTRL.RESET bit is set to 1b, a reset of the core is performed. The reset clears all the register fields to their default values. Any ongoing data transfers will be aborted.

43.6.2 Interrupt

Seven interrupts are implemented by the FIFO interface:

Index:	Name:Description:
0	TxIrq Successful transmission of block of data
1	TxEmptyCircular transmission buffer empty
2	TxErrorAMBA AHB access error during transmission
3	RxIrq Successful reception of block of data
4	RxFullCircular reception buffer full
5	RxErrorAMBA AHB access error during reception
6	RxParityParity error during reception

The interrupts are configured by means of the *pirq* VHDL generic. The setting of the *singleirq* VHDL generic results in a single interrupt output, instead of multiple, configured by the means of the *pirq* VHDL generic, and enables the read and write of the interrupt registers. When multiple interrupts are implemented, each interrupt is generated as a one system clock period long active high output pulse. When a single interrupt is implemented, it is generated as an active high level output.

43.6.3 Reset

After a reset the values of the output signals are as follows:

Signal:	Value after reset:
FIFOO.WEnde-asserted	
FIFOO.REnde-asserted	

43.6.4 Asynchronous interfaces

The following input signals are synchronized to Clk:

- FIFOI.EFn
- FIFOI.FFn
- FIFOI.HFn

43.7 Registers

The core is programmed through registers mapped into APB address space.

*Table 611.*GRFIFO registers

APB address offset	Register
0x000	Configuration Register
0x004	Status Register
0x008	Control Register
0x020	Transmit Channel Control Register
0x024	Transmit Channel Status Register
0x028	Transmit Channel Address Register
0x02C	Transmit Channel Size Register
0x030	Transmit Channel Write Register
0x034	Transmit Channel Read Register
0x038	Transmit Channel Interrupt Register
0x040	Receive Channel Control Register
0x044	Receive Channel Status Register
0x048	Receive Channel Address Register
0x04C	Receive Channel Size Register
0x050	Receive Channel Write Register
0x054	Receive Channel Read Register
0x058	Receive Channel Interrupt Register
0x060	Data Input Register
0x064	Data Output Register
0x068	Data Direction Register
0x100	Pending Interrupt Masked Status Register
0x104	Pending Interrupt Masked Register
0x108	Pending Interrupt Status Register
0x10C	Pending Interrupt Register
0x110	Interrupt Mask Register
0x114	Pending Interrupt Clear Register

43.7.1 Configuration Register [FifoCONF]

*Table 612.*Configuration Register

31 30 29 28 27 26 25 24 7	6	5 4	3	2 0
RESERVED	Abort	DW	Parity	WS
	0	0	0	0
	rw	rw	rw	rw

Field: Description:
6: ABORT Abort transfer on AHB ERROR
5-4: DW Data width:
00b = none
01b = 8 bitFIFOO.Dout[7:0],
FIFOI.Din[7:0]
10b = 16 bitFIFOO.Dout[15:0]
FIFOI.Din[15:0]

		11b = spare/none
3:	PARITY	Parity type: 0b = even 1b = odd
2-0:	WS	Number of wait states, 0 to 7

Note that the transmit or receive channel active during the AMBA AHB error is disabled if the ABORT bit is set to 1b. Note that all accesses on the affected channel will be disabled after an AMBA AHB error occurs while the ABORT bit is set to 1b. The accesses will be disabled until the affected channel is re-enabled setting the FifoTxCTRL.ENABLE or FifoRxCTRL.ENABLE bit, respectively.

Note that a wait states corresponds to an additional clock cycle added to the period when the read or write strobe is asserted. The default asserted width is one clock period for the read or write strobe when WS=0. Note that an idle gap of one clock cycle is always inserted between read and write accesses, with neither the read nor the write strobe being asserted.

Note that an additional gap of one clock cycle with the read or write strobe de-asserted is inserted between two accesses when WS is equal to or larger than 100b.

43.7.2 Status Register [FifoSTAT]

*Table 613.*Status register

31 – 6	5	4 – 0
-	SingleIrq	-
	*	
	r	

5: SingleIrq — Single interrupt output and interrupt registers when set to 1
*Reflect, VHDL generic /singleirq/

43.7.3 Control Register [FifoCTRL]

*Table 614.*Control Register

31 – 2	1	0
	Reset	
	0	
	w	

1: RESET — Reset complete FIFO interface, all registers

43.7.4 Transmit Channel Control Register [FifoTxCTRL]

*Table 615.*Transmit Channel Control Register

31 – 1	0
	Enable
	0
	rw

0: ENABLE — Enable channel

All bits are cleared to 0 at reset.

Note that in the case of an AHB bus error during an access while fetching transmit data, and the FifoConf.ABORT bit is 1b, then the ENABLE bit will be reset automatically.

At the time the ENABLE is cleared to 0b, any ongoing data writes to the FIFO are not aborted.

43.7.5 Transmit Channel Status Register [FifoTxSTAT]

*Table 616.*Transmit Channel Status Register

32	7	6	5	4	3	2	1	0
		TxOnGoing	R	TxIrq	TxEmpty	TxError	FF	HF

6: TxOnGoing Access ongoing
4: TxIrq Successful transmission of block of data. cleared on read
3: TxEmpty Transmission buffer has been emptied. cleared on read
2: TxError AMB AHB access error during transmission. cleared on read
1: FF FIFO Full Flag
0: HF FIFO Half-Full Flag

43.7.6 Transmit Channel Address Register [FifoTxADDR]

*Table 617.*Transmit Channel Address Register

31	10	9	0
ADDR			
0			
rw			

31-10: ADDR Base address for circular buffer

43.7.7 Transmit Channel Size Register [FifoTxSIZE]

*Table 618.*Transmit Channel Size Register

31	17	16	6	5	0
		SIZE			
		0			
		rw			

16-6: SIZE Size of circular buffer, in number of 64 bytes block

Valid SIZE values are 0, and between 1 and 1024. Note that the resulting behavior of invalid SIZE values is undefined.

Note that only SIZE*64-4 bytes can be stored simultaneously in the buffer. This is to simplify wrap-around condition checking.

The width of the SIZE field is configurable indirectly by means of the VHDL generic (ptrwidth) which sets the width of the read and write data pointers. In the above example VHDL generic ptrwidth=16, making the SIZE field 11 bits wide.

43.7.8 Transmit Channel Write Register [FifoTxWR]

*Table 619.*Transmit Channel Write Register

31 16	15 0
	WRITE
	0
	rw

15-0: WRITE Pointer to last written byte + 1

The WRITE field is written to in order to initiate a transfer, indicating the position +1 of the last byte to transmit.

Note that it is not possible to fill the buffer. There is always one word position in buffer unused. Software is responsible for not over-writing the buffer on wrap around (i.e. setting WRITE=READ).

Note that the LSB may be ignored for 16-bit wide FIFO devices.

The field is implemented as relative to the buffer base address (scaled with the SIZE field).

43.7.9 Transmit Channel Read Register [FifoTxRD]

*Table 620.*Transmit Channel Read Register

31 16	15 0
	READ
	0
	rw

15-0: READ Pointer to last read byte + 1

The READ field is written to automatically when a transfer has been completed successfully, indicating the position +1 of the last byte transmitted.

Note that the READ field can be used to read out the progress of a transfer.

Note that the READ field can be written to in order to set up the starting point of a transfer. This should only be done while the transmit channel is not enabled.

Note that the READ field can be automatically incremented even if the transmit channel has been disabled, since the last requested transfer is not aborted until completed.

Note that the LSB may be ignored for 16-bit wide FIFO devices.

The field is implemented as relative to the buffer base address (scaled with the SIZE field).

43.7.10 Transmit Channel Interrupt Register [FifoTxIRQ]

*Table 621.*Transmit Channel Interrupt Register

31 16	15 0
	IRQ
	0
	rw

15-0: IRQ Pointer+1 to a byte address from which the read of transmitted data shall result in an interrupt

Note that this indicates that a programmed amount of data has been sent. Note that the LSB may be ignored for 16-bit wide FIFO devices.

The field is implemented as relative to the buffer base address (scaled with the SIZE field).

43.7.11 Receive Channel Control Register [FifoRxCTRL]

*Table 622.*Receive Channel Control Register

31	2	1	0
			Enable
			0
			rw

0: ENABLE Enable channel

Note that in the case of an AHB bus error during an access while storing receive data, and the FifoConf.ABORT bit is 1b, then the ENABLE bit will be reset automatically.

At the time the ENABLE is cleared to 0b, any ongoing data reads from the FIFO are not aborted.

43.7.12 Receive Channel Status Register [FifoRxSTAT]

*Table 623.*Receive Channel Status Register

31	11	10	8	7	6	5	4	3	2	1	0
RESERVED		RxByteCntr		R	RxOnGoing	RxParity	RxIrq	RxFull	RxError	EF	HF
		0			0	0	0	0	0	1	1
		r			r	r*	r*	r*	r*	r	r

10-8: RxByteCntrNumber of bytes in local buffer
6: RxOnGoingAccess ongoing
5: RxParity Parity error during reception. Cleared on error.
4: RxIrq Successful reception of block of data. Cleared on error.
3: RxFull Reception buffer has been filled. Cleared on error.
2: RxError AMB AHB access error during reception. Cleared on error.
1: EF FIFO Empty Flag
0: HF FIFO Half-Full Flag

The circular buffer is considered as full when there are two words or less left in the buffer.

43.7.13 Receive Channel Address Register [FifoRxADDR]

*Table 624.*Receive Channel Address Register

31	10	9	0
ADDR			
0			
rw			

31-10: ADDR Base address for circular buffer

43.7.14 Receive Channel Size Register [FifoRxSIZE]

*Table 625.*Receive Channel Size Register

31 17	16 6	5 0
	SIZE	
	0	
	rw	

16-6: SIZE Size of circular buffer, in number of 64 byte blocks

Valid SIZE values are 0, and between 1 and 1024. Note that the resulting behavior of invalid SIZE values is undefined.

Note that only SIZE*64-8 bytes can be stored simultaneously in the buffer. This is to simplify wrap-around condition checking.

The width of the SIZE field is configurable indirectly by means of the VHDL generic (ptrwidth) which sets the width of the read and write data pointers. In the above example VHDL generic ptr-width=16, making the SIZE field 11 bits wide.

43.7.15 Receive Channel Write Register [FifoRxWR]

*Table 626.*Receive Channel Write Register

31 16	15 0
	WRITE
	0
	rw

15-0: WRITE Pointer to last written byte +1

The field is implemented as relative to the buffer base address (scaled with SIZE field).

The WRITE field is written to automatically when a transfer has been completed successfully, indicating the position +1 of the last byte received.

Note that the WRITE field can be used to read out the progress of a transfer.

Note that the WRITE field can be written to in order to set up the starting point of a transfer. This should only be done while the transmit channel is not enabled.

Note that the LSB may be ignored for 16-bit wide FIFO devices.

43.7.16 Receive Channel Read Register [FifoRxRD]

*Table 627.*Receive Channel Read Register

31 16	15 0
	READ
	0
	rw

15-0: READ Pointer to last read byte +1

The field is implemented as relative to the buffer base address (scaled with SIZE field).

The READ field is written to in order to release the receive buffer, indicating the position +1 of the last byte that has been read out.

Note that it is not possible to fill the buffer. There is always one word position unused in the buffer. Software is responsible for not over-reading the buffer on wrap around (i.e. setting WRITE=READ).

Note that the LSB may be ignored for 16-bit wide FIFO devices

43.7.17 Receive Channel Interrupt Register [FifoRxIRQ]

*Table 628.*Receive Channel Interrupt Register

31 16	15 0
	IRQ
	0
	rw

15-0: IRQ Pointer+1 to a byte address to which the write of received data shall result in an interrupt

Note that this indicates that a programmed amount of data has been received.

The field is implemented as relative to the buffer base address (scaled with SIZE field).

Note that the LSB may be ignored for 16-bit wide FIFO devices.

Note that by setting the IRQ field to match the value of the Receive Channel Write Register.WRITE field plus the value of the Receive Channel Status Register.RxByteCntr field, an emptying to the external memory is forced of any data temporarily stored in the local buffer.

43.7.18 Data Input Register [FifoDIN]

*Table 629.*Data Input Register

31 16	15 0
	DIN
	0
	r

15-0: DIN Input data *FIFOI.Din[15:0]*

Note that only the part of FIFOI.Din[15:0] not used by the FIFO can be used as general purpose input output, see FifoCONF.DW.

Note that only bits dwidth-1 to 0 are implemented.

43.7.19 Data Output Register [FifoDOUT]

*Table 630.*Data Output Register

31 16	15 0
	DOUT
	0
	rw

15-0: DOUT Output data *FIFOO.Dout[15:0]*

Note that only the part of FIFOO.Dout[15:0] not used by the FIFO can be used as general purpose input output, see FifoCONF.DW.

Note that only bits dwidth-1 to 0 are implemented.

43.7.20 Data Register [FifoDDIR]

*Table 631.*Data Direction Register

31 16	15 0
	DDIR
	0
	rw

15-0: DDIR Direction: *FIFOO.Dout[15:0]*
0b = input = high impedance,
1b = output = driven

Note that only the part of FIFOO.Dout[15:0] not used by the FIFO can be used as general purpose input output, see FifoCONF.DW.

Note that only bits dwidth-1 to 0 are implemented.

43.7.21 Interrupt registers

The interrupt registers give complete freedom to the software, by providing means to mask interrupts, clear interrupts, force interrupts and read interrupt status.

When an interrupt occurs the corresponding bit in the Pending Interrupt Register is set. The normal sequence to initialize and handle a module interrupt is:

- Set up the software interrupt-handler to accept an interrupt from the module.
- Read the Pending Interrupt Register to clear any spurious interrupts.
- Initialize the Interrupt Mask Register, unmasking each bit that should generate the module interrupt.
- When an interrupt occurs, read the Pending Interrupt Status Register in the software interrupt-handler to determine the causes of the interrupt.
- Handle the interrupt, taking into account all causes of the interrupt.
- Clear the handled interrupt using Pending Interrupt Clear Register.

Masking interrupts: After reset, all interrupt bits are masked, since the Interrupt Mask Register is zero. To enable generation of a module interrupt for an interrupt bit, set the corresponding bit in the Interrupt Mask Register.

Clearing interrupts: All bits of the Pending Interrupt Register are cleared when it is read or when the Pending Interrupt Masked Register is read. Reading the Pending Interrupt Masked Register yields the contents of the Pending Interrupt Register masked with the contents of the Interrupt Mask Register. Selected bits can be cleared by writing ones to the bits that shall be cleared to the Pending Interrupt Clear Register.

Forcing interrupts: When the Pending Interrupt Register is written, the resulting value is the original contents of the register logically OR-ed with the write data. This means that writing the register can force (set) an interrupt bit, but never clear it.

Reading interrupt status: Reading the Pending Interrupt Status Register yields the same data as a read of the Pending Interrupt Register, but without clearing the contents.

Reading interrupt status of unmasked bits: Reading the Pending Interrupt Masked Status Register yields the contents of the Pending Interrupt Register masked with the contents of the Interrupt Mask Register, but without clearing the contents.

The interrupt registers comprise the following:

*Table 632.*Interrupt registers

Description	Name	Mode
Pending Interrupt Masked Status Register	FifoPIMSR	r
Pending Interrupt Masked Register	FifoPIMR	r
Pending Interrupt Status Register	FifoPISR	r
Pending Interrupt Register	FifoPIR	rw
Interrupt Mask Register	FifoIMR	rw
Pending Interrupt Clear Register	FifoPICR	w

*Table 633.*Interrupt registers template

31 7	6	5	4	3	2	1	0
R	RxParity	RxError	RxFull	RxIrq	TxError	TxEmpty	TxIrq
	0	0	0	0	0	0	0
	*	*	*	*	*	*	*

6: RxParity Parity error during reception*
5: RxError AMBA AHB access error during reception*
4: RxFull Circular reception buffer full*
3: RxIrq Successful reception of block of data*
2: TxError AMBA AHB access error during transmission*
1: TxEmpty Circular transmission buffer empty*
0: TxIrq Successful transmission of block of data*

*See table 632.

43.8 Vendor and device identifiers

The module has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x035. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

43.9 Implementation

43.9.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

43.10 Configuration options

Table 634 shows the configuration options of the core (VHDL generics).

*Table 634.*Configuration options

Generic name	Function	Allowed range	Default
hindex	AHB master index.	0 - NAHBMST-1	0
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	Addr field of the APB bar.	0 - 16#FFF#	0
pmask	Mask field of the APB bar.	0 - 16#FFF#	16#FFF#
pirq	Interrupt line used by the GRFIFO.	0 - NAHBIRQ-1	0
dwidth	Data width	16	16
ptrwidth	Width of data pointers	16 - 16	16
singleirq	Single interrupt output. A single interrupt is assigned to the AMBA APB interrupt bus instead of multiple separate ones. The single interrupt output is controlled by the interrupt registers which are also enabled with this VHDL generic.	0, 1	0
oepol	Output enable polarity	0, 1	1

43.11 Signal descriptions

Table 635 shows the interface signals of the core (VHDL ports).

*Table 635.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
AHBI	*	Input	AMB master input signals	-
AHBO	*	Output	AHB master output signals	-
FIFOI	DIN[31:0]	Input	Data input	-
	PIN[3:0]		Parity input	-
	EFN		Empty flag	Low
	FFN		Full flag	Low
	HFN		Half flag	Low
FIFOO	DOUT[31:0]	Output	Data output	-
	DEN[31:0]		Data output enable	-
	POUT[3:0]		Parity output	-
	PEN[3:0]		Parity output enable	-
	WEN		Write enable	Low
	REN		Read enable	Low

* see GRLIB IP Library User's Manual

43.12 Signal definitions and reset values

The signals and their reset values are described in table 636.

*Table 636.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
d[]	Input/Output	Data	High	Tri-state
p[]	Input/Output	Parity	High	Tri-state
wen	Output	Write Enable	-	Logical 1
ren	Output	Read Enable	-	Logical 1
efn	Input	Empty Flag	-	-
ffn	Input	Full Flag	-	-
hfn	Input	Half Flag	-	-

43.13 Timing

The timing waveforms and timing parameters are shown in figure 129 and are defined in table 637.

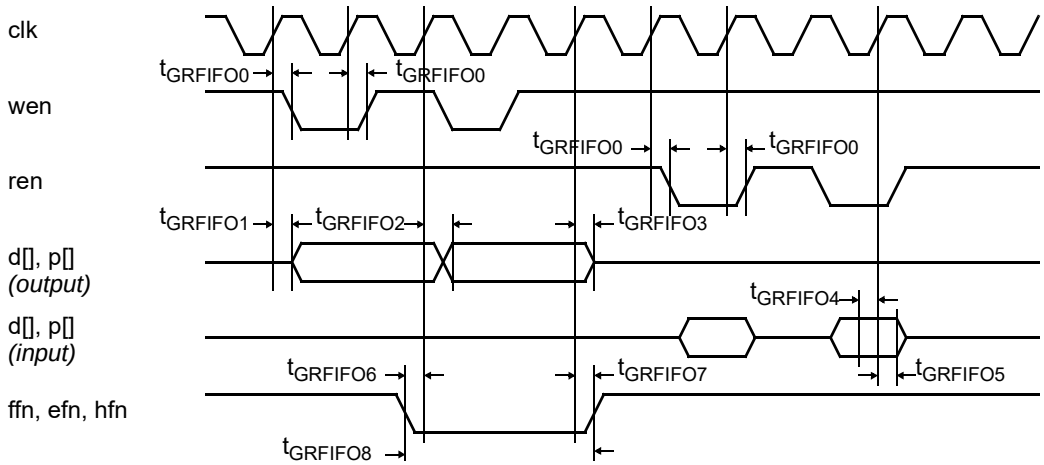


Figure 129. Timing waveforms

*Table 637.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{GRFIFO0}$	clock to output delay	rising *clk* edge	-	TBD	ns
$t_{GRFIFO1}$	clock to non-tri-state delay	rising *clk* edge	TBD	-	ns
$t_{GRFIFO2}$	clock to output delay	rising *clk* edge	-	TBD	ns
$t_{GRFIFO3}$	clock to tri-state delay	rising *clk* edge	-	TBD	ns
$t_{GRFIFO4}$	input to clock setup	rising *clk* edge	TBD	-	ns
t_{GRIFO5}	input from clock hold	rising *clk* edge	TBD	-	ns
t_{GRIFO6}	input to clock setup	rising *clk* edge	-	TBD	ns
t_{GRIFO7}	input from clock hold	rising *clk* edge	TBD	-	ns
t_{GRIFO8}	input assertion duration	-	TBD	-	*clk* periods

43.14 Library dependencies

Table 638 shows the libraries used when instantiating the core (VHDL libraries).

*Table 638.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GRLIB	AMBA	Signals, component	DMA2AHB definitions
GAISLER	MISC	Signals, component	Component declarations, signals.

43.15 Instantiation

This example shows how the core can be instantiated.

```
grfifo0: grfifo
  generic map (
    hindex    => GRFIFO_HINDEX,
    pindex    => GRFIFO_PINDEX,
    paddr     => GRFIFO_PADDR,
    pmask     => 16#fff#,
    pirq      => CFG_GRFIFO_IRQ,
    dwidth    => CFG_GRFIFO_WIDTH,
    ptrwidth  => CFG_GRFIFO_ABITS,
    singleirq => CFG_GRFIFO_SINGLE,
    oepol     => 1)
  port map (
    rstn  => rstn,
    clk   => clk,
    apbi  => apbi,
    apbo  => apbo(GRFIFO_PINDEX),
    ahbi  => ahbi,
    ahbo  => ahbo(GRFIFO_HINDEX),
    fifoi => fifoi,
    fifoo => fifoo);
```

44 GRADCDAC - ADC / DAC Interface

44.1 Overview

The block diagram shows a possible partitioning of the combined analogue-to-digital converter (ADC) and digital-to-analogue converter (DAC) interface.

The combined analogue-to-digital converter (ADC) and digital-to-analogue converter (DAC) interface is assumed to operate in an AMBA bus system where an APB bus is present. The AMBA APB bus is used for data access, control and status handling.

The ADC/DAC interface provides a combined signal interface to parallel ADC and DAC devices. The two interfaces are merged both at the pin/pad level as well as at the interface towards the AMBA bus. The interface supports simultaneously one ADC device and one DAC device in parallel.

Address and data signals unused by the ADC and the DAC can be used for general purpose input output, providing 0, 8, 16 or 24 channels.

The ADC interface supports 8 and 16 bit data widths. It provides chip select, read/convert and ready signals. The timing is programmable. It also provides an 8-bit address output. The ADC conversion can be initiated either via the AMBA interface or by internal or external triggers. An interrupt is generated when a conversion is completed.

The DAC interface supports 8 and 16 bit data widths. It provides a write strobe signal. The timing is programmable. It also provides an 8-bit address output. The DAC conversion is initiated via the AMBA interface. An interrupt is generated when a conversion is completed.

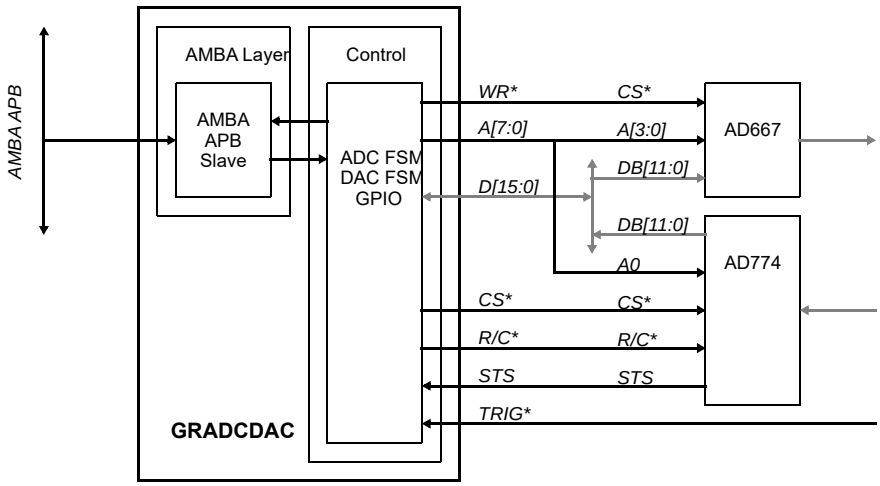


Figure 130. Block diagram and usage example

44.1.1 Function

The core implements the following functions:

- ADC interface conversion:
- ready feed-back, or
- timed open-loop
- DAC interface conversion:
- timed open-loop
- General purpose input output:
- unused data bus, and

- unused address bus
- Status and monitoring:
- on-going conversion
- completed conversion
- timed-out conversion

Note that it is not possible to perform ADC and DAC conversions simultaneously. On only one conversion can be performed at a time.

44.1.2 Interfaces

The core provides the following external and internal interfaces:

- Combined ADC/DAC interface
- programmable timing
- programmable signal polarity
- programmable conversion modes
- AMBA APB slave interface

The ADC interface is intended for amongst others the following devices:

Name:Width:Type:

AD574 12-bit R/C*, CE, CS*, RDY*, tri-state

AD674 12-bit R/C*, CE, CS*, RDY*, tri-state

AD774 12-bit R/C*, CE, CS*, RDY*, tri-state

AD670 8-bit R/W*, CE*, CS*, RDY, tri-state

AD571 10-bit Blank/Convert*, RDY*, tri-state

AD1671 12-bit Encode, RDY*, non-tri-state

LTC141414-bitConvert*, RDY, non-tri-state

The DAC interface is intended for amongst others the following devices:

Name:Width:Type:

AD56110-bitParallel-Data-in-Analogue-out

AD56512-bitParallel-Data-in-Analogue-out

AD66712-bitParallel-Data-in-Analogue-out, CS*

AD76712-bitParallel-Data-in-Analogue-out, CS*

DAC08 8-bit Parallel-Data-in-Analogue-out

44.2 Operation

44.2.1 Interfaces

The internal interface on the on-chip bus towards the core is a common AMBA APB slave for data access, configuration and status monitoring, used by both the ADC interface and the DAC interface.

The ADC address output and the DAC address output signals are shared on the external interface. The address signals are possible to use as general purpose input output channels. This is only realized when the address signals are not used by either ADC or DAC.

The ADC data input and the DAC data output signals are shared on the external interface. The data input and output signals are possible to use as general purpose input output channels. This is only realized when the data signals are not used by either ADC or DAC.

Each general purpose input output channel shall be individually programmed as input or output. This applies to both the address bus and the data bus. The default reset configuration for each general purpose input output channel is as input. The default reset value each general purpose input output channel is logical zero.

Note that protection toward spurious pulse commands during power up shall be mitigated as far as possible by means of I/O cell selection from the target technology.

44.2.2 Analogue to digital conversion

The ADC interface supports 8 and 16 bit wide input data.

The ADC interface provides an 8-bit address output, shared with the DAC interface. Note that the address timing is independent of the acquisition timing.

The ADC interface shall provide the following control signals:

- Chip Select
- Read/Convert
- Ready

The timing of the control signals is made up of two phases:

- Start Conversion
- Read Result

The Start Conversion phase is initiated by one of the following sources, provided that no other conversion is ongoing:

- Event on one of three separate trigger inputs
- Write access to the AMBA APB slave interface

Note that the trigger inputs can be connected to internal or external sources to the ASIC incorporating the core. Note that any of the trigger inputs can be connected to a timer to facilitate cyclic acquisition. The selection of the trigger source is programmable. The trigger inputs is programmable in terms of: Rising edge or Falling edge. Triggering events are ignored if ADC or DAC conversion is in progress.

The transition between the two phases is controlled by the Ready signal. The Ready input signal is programmable in terms of: Rising edge or Falling edge. The Ready input signaling is protected by means of a programmable time-out period, to assure that every conversion terminates. It is also possible to perform an ADC conversion without the use of the Ready signal, by means of a programmable conversion time duration. This can be seen as an open-loop conversion.

The Chip Select output signal is programmable in terms of:

- Polarity
- Number of assertions during a conversion, either
- Pulsed once during Start Conversion phase only,
- Pulsed once during Start Conversion phase and once during Read Result phase, or
- Asserted at the beginning of the Start Conversion phase and de-asserted at the end of the Read Result phase

The duration of the asserted period is programmable, in terms of system clock periods, for the Chip Select signal when pulsed in either of two phases.

The Read/Convert signal is de-asserted during the Start Conversion phase, and asserted during the Read Result phase. The Read/Convert output signal is programmable in terms of: Polarity. The setup timing from Read/Convert signal being asserted till the Chip Select signal is asserted is programmable, in terms of system clock periods. Note that the programming of Chip Select and Read/Convert timing is implemented as a common parameter.

At the end of the Read Result phase, an interrupt is generated, indicating that data is ready for readout via the AMBA APB slave interface. The status of an on-going conversion is possible to read out via the AMBA APB slave interface. The result of a conversion is read out via the AMBA APB slave interface. Note that this is independent of what trigger started the conversion.

An ADC conversion is non-interruptible. It is possible to perform at least 1000 conversions per second.

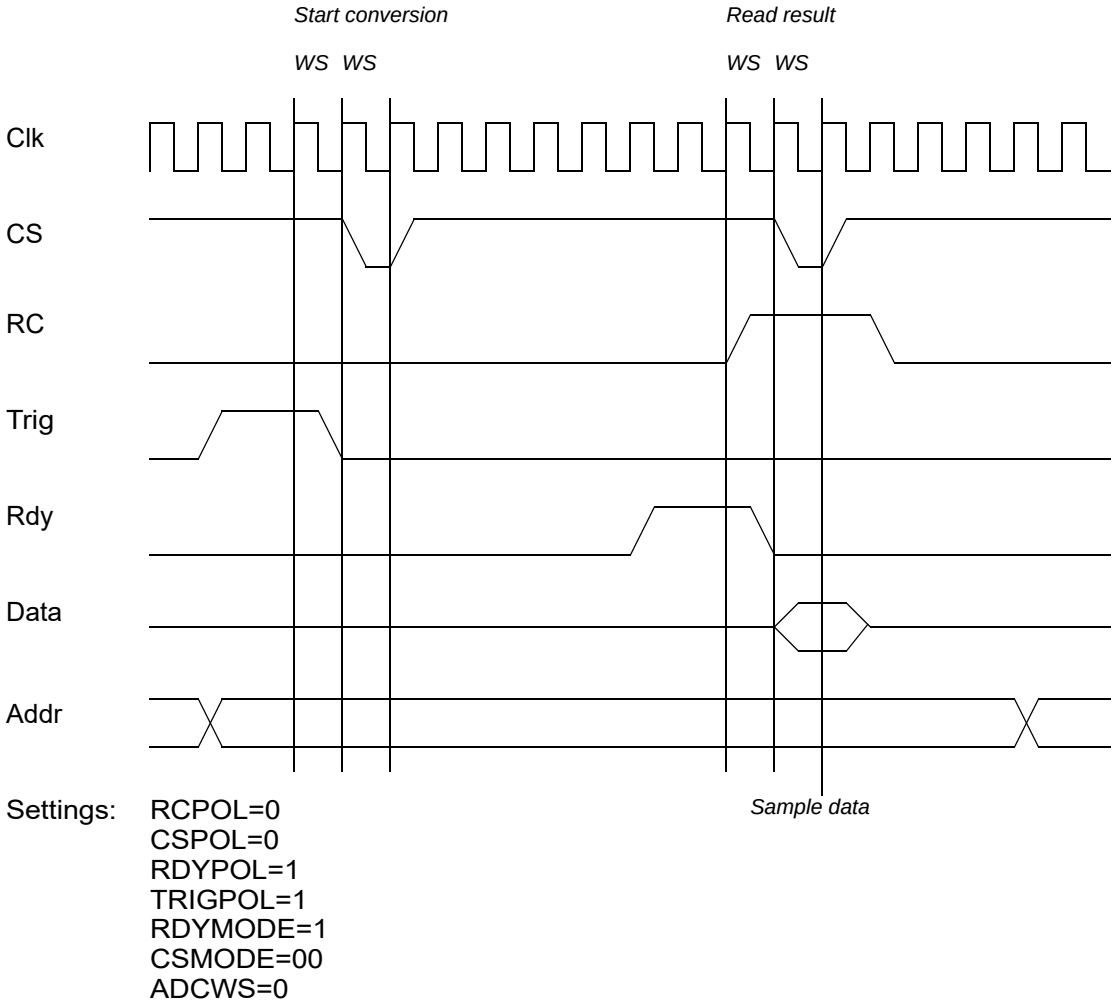


Figure 131. Analogue to digital conversion waveform, 0 wait states (WS)

44.2.3 Digital to analogue conversion

The DAC interface supports 8 and 16 bit wide output data. The data output signal is driven during the conversion and is placed in high impedance state after the conversion.

The DAC interface provides an 8-bit address output, shared with the ADC interface. Note that the address timing is independent of the acquisition timing.

The DAC interface provides the following control signal: Write Strobe. Note that the Write Strobe signal can also be used as a chip select signal. The Write Strobe output signal is programmable in terms of: Polarity. The Write Strobe signal is asserted during the conversion. The duration of the asserted period of the Write Strobe is programmable in terms of system clock periods.

At the end the conversion, an interrupt is generated. The status of an on-going conversion is possible to read out via the AMBA APB slave interface. A DAC conversion is non-interruptible.

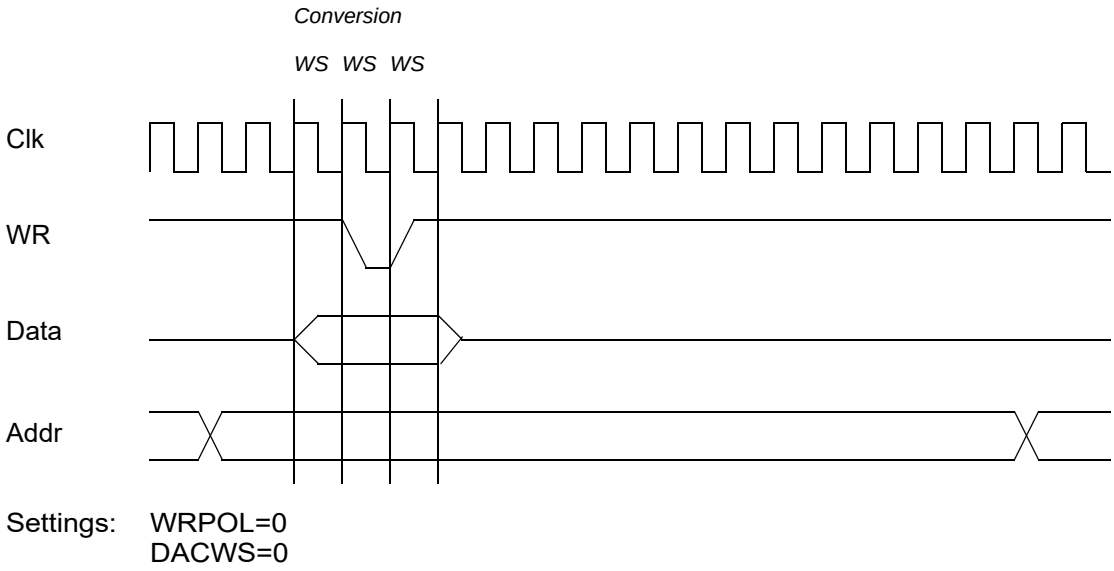


Figure 132. Digital to analogue conversion waveform, 0 wait states (WS)

44.3 Operation

44.3.1 Interrupt

Two interrupts are implemented by the ADC/DAC interface:

Index:	Name:	Description:
0	ADC	ADC conversion ready
1	DAC	DAC conversion ready

The interrupts are configured by means of the *pirq* VHDL generic.

44.3.2 Reset

After a reset the values of the output signals are as follows:

Signal:	Value after reset:
ADO.Aout[7:0]	de-asserted
ADO.Aen[7:0]	de-asserted
ADO.Dout[15:0]	de-asserted
ADO.Den[15:0]	de-asserted
ADO.WR	de-asserted (logical one)
ADO.CS	de-asserted (logical one)
ADO.RC	de-asserted (logical one)

44.3.3 Asynchronous interfaces

The following input signals are synchronized to Clk:

- ADI.Ain[7:0]
- ADI.Din[15:0]
- ADI.RDY
- ADI.TRIG[2:0]

44.4 Registers

The core is programmed through registers mapped into APB address space.

*Table 639.*GRADCDAC registers

APB address offset	Register
0x000	Configuration Register
0x004	Status Register
0x010	ADC Data Input Register
0x014	DAC Data Output Register
0x020	Address Input Register
0x024	Address Output Register
0x028	Address Direction Register
0x030	Data Input Register
0x034	Data Output Register
0x038	Data Direction Register

44.4.1 Configuration Register [ADCONF]

*Table 640.*Configuration register

31 24	23 19	18	17 16
	DACWS	WRPOL	DACDW
	0	0	0
	rw	rw	rw

15 11	10	9 8	7	6	5	4	3	2 1 0
ADCWS	RCPOL	CSMODE	CSPOL	RDYMODE	RDYPOL	TRIGPOL	TRIG-MODE	ADCDW
0	0	0	0	0	0	0	0	0
rw	rw	rw	rw	rw	rw	rw	rw	rw

23-19: DACWS Number of DAC wait states, 0 to 31 [5 bits]
18: WRPOL Polarity of DAC write strobe:
0b = active low
1b = active high
17-16: DACDW DAC data width
00b = none
01b = 8 bit ADO.Dout[7:0]
10b = 16 bit ADO.Dout[15:0]
11b = none/spare
15-11: ADCWS Number of ADC wait states, 0 to 31 [5 bits]

10: RCPOL Polarity of ADC read convert:
0b = active low read
1b = active high read
9-8: CSMODE Mode of ADC chip select:
00b = asserted during conversion and read phases
01b = asserted during conversion phase
10b = asserted during read phase
11b = asserted continuously during both phases
7: CSPOL Polarity of ADC chip select:0b = active low
1b = active high
6: RDYMODE:Mode of ADC ready:
0b = unused, i.e. open-loop
1b = used, with time-out
5: RDYPOL Polarity of ADC ready:
0b = falling edge
1b = rising edge
4: TRIGPOL Polarity of ADC triggers:
0b = falling edge
1b = rising edge
3-2: TRIGMODEADC trigger source:
00b = none
01b = ADI.TRIG[0]
10b = ADI.TRIG[1]
11b = ADI.TRIG[2]
1-0: ADCDW ADC data width:
00b = none
01b = 8 bit ADI.Din[7:0]
10b = 16 bit ADI.Din[15:0]
11b = none/spare

The ADCDW field defines what part of ADI.Din[15:0] is read by the ADC.

The DACDW field defines what part of ADO.Dout[15:0] is written by the DAC.

Parts of the data input/output signals used neither by ADC nor by DAC are available for the general purpose input output functionality.

Note that an ADC conversion can be initiated by means of a write access via the AMBA APB slave interface, thus not requiring an explicit ADC trigger source setting.

The ADCONF.ADCWS field defines the number of system clock periods, ranging from 1 to 32, for the following timing relationships between the ADC control signals:

- ADO.RC stable before ADO.CS period
- ADO.CS asserted period, when pulsed
- ADO.TRIG[2:0] event until ADO.CS asserted period
- Time-out period for ADO.RDY: 2048 * (1+ADCONF.ADCWS)
- Open-loop conversion timing: 512 * (1+ADCONF.ADCWS)

The ADCONF.DACWS field defines the number of system clock periods, ranging from 1 to 32, for the following timing relationships between the DAC control signals:

- ADO.Dout[15:0] stable before ADO.WR period
- ADO.WR asserted period
- ADO.Dout[15:0] stable after ADO.WR period

44.4.2 Status Register [ADSTAT]

*Table 641.*Status register

31 14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DACNO	DACRDY	DACON	ADCTO	ADCNO	ADCRDY	ADCON
								0	0	0	0	0	0	0
								r*	r*	r	r*	r*	r*	r

6: DACNO DAC conversion request rejected (due to ongoing DAC or ADC conversion). Cleared on rest.
5: DACRDY DAC conversion completed. Cleared on rest.
4: DACON DAC conversion ongoing
3: ADCTO ADC conversion timeout. Cleared on rest.
2: ADCNO ADC conversion request rejected (due to ongoing ADC or DAC conversion). Cleared on rest.
1: ADCRDY ADC conversion completed. Cleared on rest.
0: ADCON ADC conversion ongoing

Note that the status bits can be used for monitoring the progress of a conversion or to ascertain that the interface is free for usage.

44.4.3 ADC Data Input Register [ADIN]

*Table 642.*ADC Data Input Register

31 16	15 0
	ADCIN
	0
	rw*

15-0: ADCIN ADC input data A write access to the register initiates an analogue to digital conversion, provided that no other ADC or DAC conversion is ongoing (otherwise the request is rejected). A read access that occurs before an ADC conversion has been completed returns the result from a previous conversion. *ADI.Din[15:0]*

Note that any data can be written and that it cannot be read back, since not relevant to the initiation of the conversion.
Note that only the part of ADI.Din[15:0] that is specified by means of bit ADCONF.ADCDW is used by the ADC. The rest of the bits are read as zeros.

Note that only bits dwidth-1 to 0 are implemented.

44.4.4 DAC Data Output Register [ADOUT]

*Table 643.*DAC Data Output Register

31 16	15 0
	DACOUT
	0
	rw*

15-0: DACOUT DAC output data A write access to the register initiates a digital to analogue conversion, provided that no other DAC or ADC conversion is ongoing (otherwise the request is rejected). *ADO.Dout[15:0]*

Note that only the part of ADO.Dout[15:0] that is specified by means of ADCONF.DACDW is driven by the DAC. The rest of the bits are not driven by the DAC during a conversion.

Note that only the part of ADO.Dout[15:0] which is specified by means of ADCONF.DACDW can be read back, whilst the rest of the bits are read as zeros.

Note that only bits dwidth-1 to 0 are implemented.

44.4.5 Address Input Register [ADAIN]

*Table 644.*Address Input Register

31 8	7 0
	AIN
	0
	r

7-0: AIN Input address *ADI.Ain[7:0]*

Note that only bits awidth-1 to 0 are implemented.

44.4.6 Address Output Register [ADAOUT]

*Table 645.*Address Output Register

31 8	7 0
	AOUT
	0
	rw

7-0: AOUT Output address *ADO.Aout[7:0]*

Note that only bits awidth-1 to 0 are implemented.

44.4.7 Address Direction Register [ADADIR]

*Table 646.*Address Direction Register

31 8	7 0
	ADIR
	0
	rw

7-0: ADIR Direction: *ADO.Aout[7:0]*
0b = input = high impedance,
1b = output = driven

Note that only bits awidth-1 to 0 are implemented.

44.4.8 Data Input Register [ADDIN]

*Table 647.*Data Input Register

31 16	15 0
	DIN
	0
	r

15-0: DIN Input data *ADI.Din[15:0]*

Note that only the part of ADI.Din[15:0] not used by the ADC can be used as general purpose input output, see ADCONF.ADCDW.

Note that only bits dwidth-1 to 0 are implemented.

44.4.9 1Data Output Register [ADDOUT]

*Table 648.*Data Output Register

31 16	15 0
	DOUT
	0
	rw

15-0: DOUT Output data *ADO.Dout[15:0]*

Note that only the part of ADO.Dout[15:0] neither used by the DAC nor the ADC can be used as general purpose input output, see ADCONF.DACDW and ADCONF. ADCDW.

Note that only bits dwidth-1 to 0 are implemented.

44.4.10 Data Register [ADDDIR]

*Table 649.*Data Direction Register

31 16	15 0
	DDIR
	0
	rw

15-0: DDIR Direction: *ADO.Dout[15:0]*
0b = input = high impedance,
1b = output = driven

Note that only the part of ADO.Dout[15:0] not used by the DAC can be used as general purpose input output, see ADCONF.DACDW.

Note that only bits dwidth-1 to 0 are implemented.

44.5 Vendor and device identifiers

The module has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x036. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

44.6 Implementation

44.6.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

44.7 Configuration options

Table 650 shows the configuration options of the core (VHDL generics).

*Table 650.*Configuration options

Generic	Function	Allowed range	Default
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	Addr field of the APB bar.	0 - 16#FFF#	0
pmask	Mask field of the APB bar.	0 - 16#FFF#	16#FFF#
pirq	Interrupt line used by the GRADCDAC.	0 - NAHBIRQ-1	1
nchannel	Number of input/outputs	1 - 32	24
npulse	Number of pulses	1 - 32	8
invertpulse	Invert pulse output when set	1 - 32	0
cntrwidth	Pulse counter width	4 to 32	20
oepol	Output enable polarity	0, 1	1

44.8 Signal descriptions

Table 651 shows the interface signals of the core (VHDL ports).

*Table 651.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
ADI	ADI.Ain[7:0]	Input	Common Address input	-
	ADI.Din[15:0]		ADC Data input	
	ADI.RDY		ADC Ready input	
	ADI.TRIG[2:0]		ADC Trigger inputs	
ADO	ADO.Aout[7:0]	Output	Common Address output	-
	ADO.Aen[7:0]		Common Address output enable	
	ADO.Dout[15:0]		DAC Data output	-
	ADO.Den[15:0]		DAC Data output enable	
	ADO.WRDAC		Write Strobe	
	ADO.CSADC		Chip Select	
	ADO.RCADC		Read/Convert	

* see GRLIB IP Library User's Manual

Note that the VHDL generic oepol is used for configuring the logical level of ADO.Den and ADO.Aen while asserted.

44.9 Signal definitions and reset values

The signals and their reset values are described in table 652.

*Table 652.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
a[]	Input/Output	Address	High	Tri-state
d[]	Input/Output	Data	High	Tri-state
wr	Output	DAC Write Strobe	-	Logical 0
cs	Output	ADC Chip Select	-	Logical 0
rc	Output	ADC Read/Convert	-	Logical 0
rdy	Input	ADC Ready	-	-
trig[]	Input	ADC Trigger	-	-

44.10 Timing

The timing waveforms and timing parameters are shown in figure 133 and are defined in table 653. Note that the input and output polarities of control and response signals are programmable. The figures shows operation where there are zero wait states. Note also that the address timing has no direct correlation with the ADC and DAC accesses, since controlled by a separate set of registers.

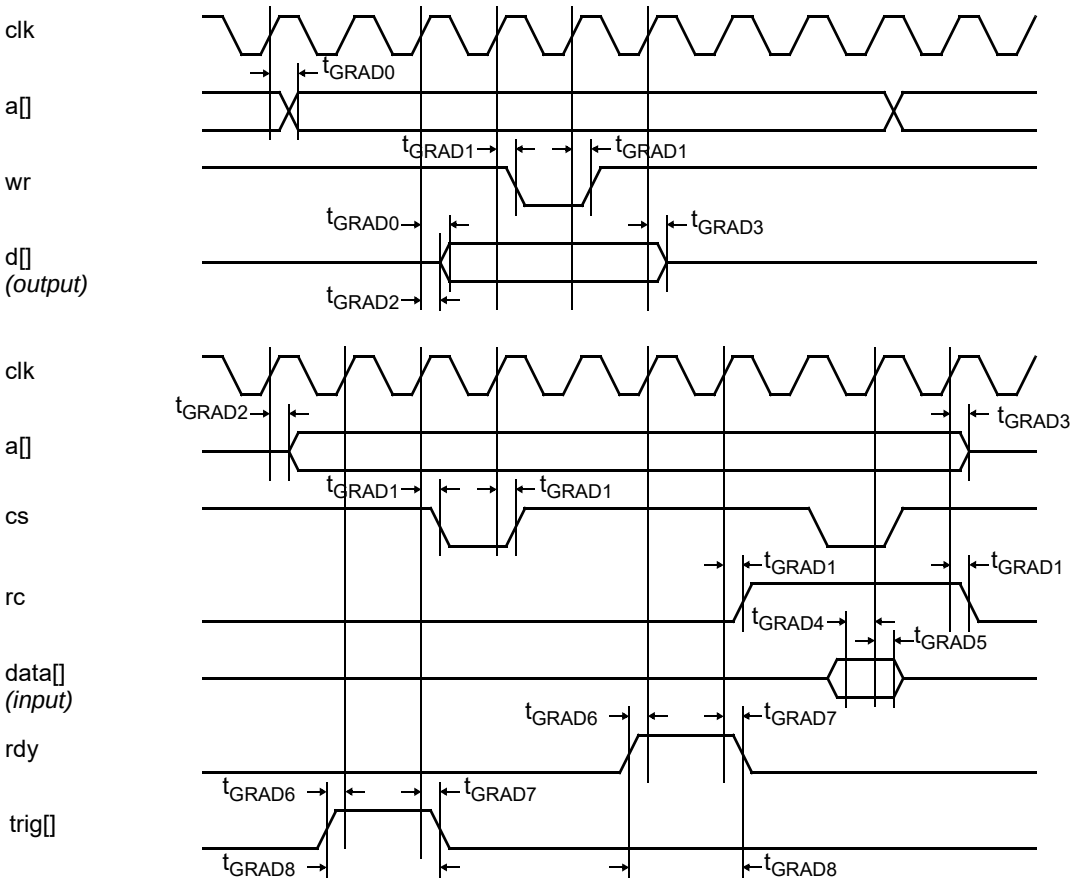


Figure 133. Timing waveforms

*Table 653.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{GRAD0}	a/d clock to output delay	rising *clk* edge	-	TBD	ns
t_{GRAD1}	clock to output delay	rising *clk* edge	-	TBD	ns
t_{GRAD2}	clock to a/d non-tri-state delay	rising *clk* edge	TBD	-	ns
t_{GRAD3}	a/d clock to data tri-state delay	rising *clk* edge	-	TBD	ns
t_{GRAD4}	a/d input to clock setup	rising *clk* edge	TBD	-	ns
t_{GRAD5}	a/d input from clock hold	rising *clk* edge	TBD	-	ns
t_{GRAD6}	input to clock setup	rising *clk* edge	-	TBD	ns
t_{GRAD7}	input from clock hold	rising *clk* edge	TBD	-	ns
t_{GRAD8}	input assertion duration	-	TBD	-	*clk* periods

44.11 Library dependencies

Table 654 shows the libraries used when instantiating the core (VHDL libraries).

*Table 654.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	MISC	Signals	GRADCDAC component declaration

44.12 Instantiation

This example shows how the core can be instantiated.

TBD

45 GRFPU - High-performance IEEE-754 Floating-point unit

45.1 Overview

GRFPU is a high-performance FPU implementing floating-point operations as defined in the IEEE Standard for Binary Floating-Point Arithmetic (IEEE-754) and the SPARC V8 standard (IEEE-1754). Supported formats are single and double precision floating-point numbers. The advanced design combines two execution units, a fully pipelined unit for execution of the most common FP operations and a non-blocking unit for execution of divide and square-root operations.

The logical view of the GRFPU is shown in figure 134.

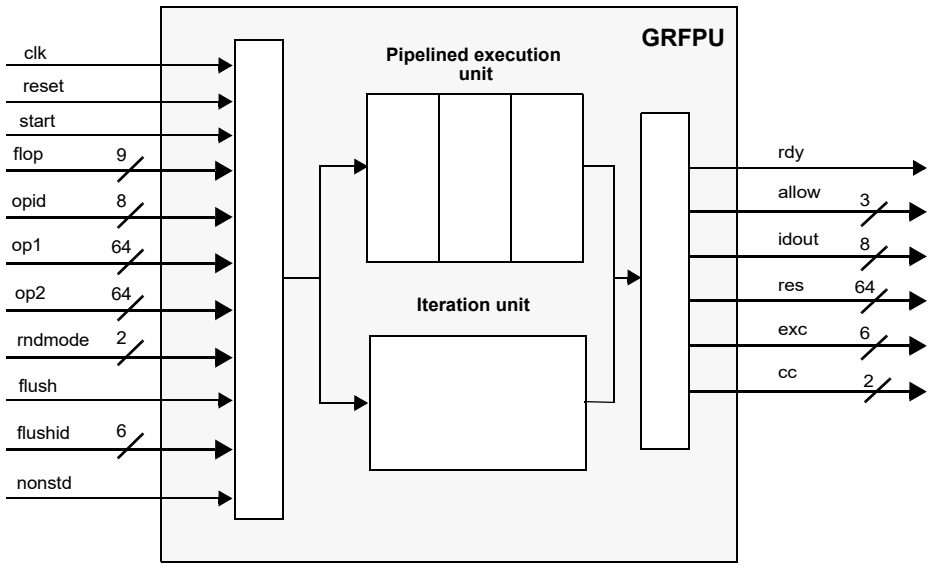


Figure 134. GRFPU Logical View

This document describes GRFPU from functional point of view. Chapter “Functional description” gives details about GRFPU’s implementation of the IEEE-754 standard including FP formats, operations, opcodes, operation timing, rounding and exceptions. “Signals and timing” describes the GRFPU interface and its signals. “GRFPU Control Unit” describes the software aspects of the GRFPU integration into a LEON processor through the GRFPU Control Unit - GRFPC. For implementation details refer to the white paper, “GRFPU - High Performance IEEE-754 Floating-Point Unit” (available at *www.gaisler.com*).

45.2 Functional description

45.2.1 Floating-point number formats

GRFPU handles floating-point numbers in single or double precision format as defined in the IEEE-754 standard with exception for denormalized numbers. See section 45.2.5 for more information on denormalized numbers.

45.2.2 FP operations

GRFPU supports four types of floating-point operations: arithmetic, compare, convert and move. The operations implement all FP instructions specified by SPARC V8 instruction set, and most of the operations defined in IEEE-754. All operations are summarized in table 655, with their opcodes, operands, results and exception codes. Throughputs and latencies and are shown in table 655.

Table 655.: GRFPU operations

Operation	OpCode[8:0]	Op1	Op2	Result	Exceptions	Description
Arithmetic operations						
FADDS FADDD	001000001 001000010	SP DP	SP DP	SP DP	UNF, NV, OF, UF, NX	Addition
FSUBS FSUBD	001000101 001000110	SP DP	SP DP	SP DP	UNF, NV, OF, UF, NX	Subtraction
FMULS FMULD FSMULD	001001001 001001010 001101001	SP DP SP	SP DP SP	SP DP DP	UNF, NV, OF, UF, NX UNF, NV, OF, UF, NX UNF, NV, OF, UF	Multiplication, FSMULD gives exact double-precision product of two single-precision operands.
FDIVS FDIVD	001001101 001001110	SP DP	SP DP	SP DP	UNF, NV, OF, UF, NX, DZ	Division
FSQRTS FSQRTD	000101001 000101010	- -	SP DP	SP DP	UNF, NV, NX	Square-root
Conversion operations						
FITOS FITOD	011000100 011001000	-	INT	SP DP	NX -	Integer to floating-point conversion
FSTOI FDTOI	011010001 011010010	-	SP DP	INT	UNF, NV, NX	Floating-point to integer conversion. The result is rounded in round-to-zero mode.
FSTOI_RND FDTOI_RND	111010001 111010010	-	SP DP	INT	UNF, NV, NX	Floating-point to integer conversion. Rounding according to RND input.
FSTOD FDTOS	011001001 011000110	-	SP DP	DP SP	UNF, NV UNF, NV, OF, UF, NX	Conversion between floating-point formats
Comparison operations						
FCMPS FCMPD	001010001 001010010	SP DP	SP DP	CC	NV	Floating-point compare. Invalid exception is generated if either operand is a signaling NaN.
FCMPES FCMPED	001010101 001010110	SP DP	SP DP	CC	NV	Floating point compare. Invalid exception is generated if either operand is a NaN (quiet or signaling).
Negate, Absolute value and Move						
FABSS	000001001	-	SP	SP	-	Absolute value.
FNEGS	000000101	-	SP	SP	-	Negate.
FMOVS	000000001		SP	SP	-	Move. Copies operand to result output.

SP - single precision floating-point number
DP - double precision floating-point number
INT - 32 bit integer
CC - condition codes, see table 658
UNF, NV, OF, UF, NX - floating-point exceptions, see section 45.2.3

Arithmetic operations include addition, subtraction, multiplication, division and square-root. Each arithmetic operation can be performed in single or double precision formats. Arithmetic operations have one clock cycle throughput and a latency of four clock cycles, except for divide and square-root operations, which have a throughput of 16 - 25 clock cycles and latency of 16 - 25 clock cycles (see

table 656). Add, sub and multiply can be started on every clock cycle, providing high throughput for these common operations. Divide and square-root operations have lower throughput and higher latency due to complexity of the algorithms, but are executed in parallel with all other FP operations in a non-blocking iteration unit. Out-of-order execution of operations with different latencies is easily handled through the GRFPU interface by assigning an id to every operation which appears with the result on the output once the operation is completed (see section 45.4).

Table 656.: Throughput and latency

Operation	Throughput	Latency
FADDS, FADDD, FSUBS, FSUBD, FMULS, FMULD, FSMULD	1	4
FITOS, FITOD, FSTOI, FSTOI_RND, FDTOI, FDTOI_RND, FSTOD, FDTOS	1	4
FCMPS, FCMPD, FCMPES, FCMPED	1	4
FDIVS	16	16
FDIVD	16.5 (15/18)*	16.5 (15/18)*
FSQRTS	24	24
FSQRTD	24.5 (23/26)*	24.5 (23/26)*

* Throughput and latency are data dependant with two possible cases with equal statistical possibility.

Conversion operations execute in a pipelined execution unit and have throughput of one clock cycle and latency of four clock cycles. Conversion operations provide conversion between different floating-point numbers and between floating-point numbers and integers.

Comparison functions offering two different types of quiet Not-a-Numbers (QNaNs) handling are provided. Move, negate and absolute value are also provided. These operations do not ever generate unfinished exception (unfinished exception is never signaled since compare, negate, absolute value and move handle denormalized numbers).

45.2.3 Exceptions

GRFPU detects all exceptions defined by the IEEE-754 standard. This includes detection of Invalid Operation (NV), Overflow (OF), Underflow (UF), Division-by-Zero (DZ) and Inexact (NX) exception conditions. Generation of special results such as NaNs and infinity is also implemented. Overflow (OF) and underflow (UF) are detected before rounding. If an operation underflows the result is flushed to zero (GRFPU does not support denormalized numbers or gradual underflow). A special Unfinished exception (UNF) is signaled when one of the operands is a denormalized number which is not handled by the arithmetic and conversion operations.

45.2.4 Rounding

All four rounding modes defined in the IEEE-754 standard are supported: round-to-nearest, round-to-+inf, round-to--inf and round-to-zero.

45.2.5 Denormalized numbers

Denormalized numbers are not handled by the GRFPU arithmetic and conversion operations. A system (microprocessor) with the GRFPU could emulate rare cases of operations on denormals in software using non-FPU operations. A special Unfinished exception (UNF) is used to signal an arithmetic or conversion operation on the denormalized numbers. Compare, move, negate and absolute value operations can handle denormalized numbers and do not raise the unfinished exception. GRFPU does not generate any denormalized numbers during arithmetic and conversion operations on normalized numbers. If the infinitely precise result of an operation is a tiny number (smaller than minimum value representable in normal format) the result is flushed to zero (with underflow and inexact flags set).

45.2.6 Non-standard Mode

GRFPU can operate in a non-standard mode where all denormalized operands to arithmetic and conversion operations are treated as (correctly signed) zeroes. Calculations are performed on zero operands instead of the denormalized numbers obeying all rules of the floating-point arithmetics including rounding of the results and detecting exceptions.

45.2.7 NaNs

GRFPU supports handling of Not-a-Numbers (NaNs) as defined in the IEEE-754 standard. Operations on signaling NaNs (SNaNs) and invalid operations (e.g. inf/inf) generate the Invalid exception and deliver QNaN_GEN as result. Operations on Quiet NaNs (QNaNs), except for FCMPES and FCMPED, do not raise any exceptions and propagate QNaNs through the FP operations by delivering NaN-results according to table 657. QNaN_GEN is 0x7fffe00000000000 for double precision results and 0x7fff0000 for single precision results.

Table 657.: Operations on NaNs

	Operand 2			
Operand 1		FP	QNaN2	SNaN2
	none	FP	QNaN2	QNaN_GEN
	FP	FP	QNaN2	QNaN_GEN
	QNaN1	QNaN1	QNaN2	QNaN_GEN
	SNaN1	QNaN_GEN	QNaN_GEN	QNaN_GEN

45.3 Signal descriptions

Table 658 shows the interface signals of the core (VHDL ports). All signals are active high except for RST which is active low.

Table 658.: Signal descriptions

Signal	I/O	Description
CLK	I	Clock
RESET	I	Reset
START	I	Start an FP operation on the next rising clock edge
NONSTD	I	Nonstandard mode. Denormalized operands are converted to zero.
FLOP[8:0]	I	FP operation. For codes see table 655.
OP1[63:0] OP2[63:0]	I	FP operation operands are provided on these one or both of these inputs. All 64 bits are used for IEEE-754 double precision floating-point numbers, bits [63:32] are used for IEEE-754 single precision floating-point numbers and 32-bit integers.
OPID[7:0]	I	FP operation id. Every operation is associated with an id which will appear on the RESID output when the FP operation is completed. This value shall be incremented by 1 (with wrap-around) for every started FP operation. If flushing is used, FP operation id is 6 -bits wide (OPID[5:0] are used for id, OPID[7:6] are tied to “00”). If flushing is not used (input signal FLUSH is tied to ‘0’), all 8-bits (OPID[7:0]) are used.
FLUSH	I	Flush FP operation with FLUSHID.
FLUSHID[5:0]	I	Id of the FP operation to be flushed.
RNDMODE[1:0]	I	Rounding mode. 00 - rounding-to-nearest, 01 - round-to-zero, 10 - round-to-+inf, 11 - round-to--inf.
RES[63:0]	O	Result of an FP operation. If the result is double precision floating-point number all 64 bits are used, otherwise single precision or integer result appears on RESULT[63:32].
EXC[5:0]	O	Floating-point exceptions generated by an FP operation. EXC[5] - Unfinished FP operation. Generated by an arithmetic or conversion operation with denormalized input(s). EXC[4] - Invalid exception. EXC[3] - Overflow. EXC[2] - Underflow. EXC[1] - Division by zero. EXC[0] - Inexact.
ALLOW[2:0]	O	Indicates allowed FP operations during the next clock cycle. ALLOW[0] - FDIVS, FDIVD, FSQRTS and FSQRTD allowed ALLOW[1] - FMULS, FMULD, FSMULD allowed ALLOW[2] - all other FP operations allowed
RDY	O	The result of a FP operation will be available at the end of the next clock cycle.
CC[1:0]	O	Result (condition code) of an FP compare operation. 00 - equal 01 - operand1 < operand2 10 - operand1 > operand2 11 - unordered
IDOUT[7:0]	O	Id of the FP operation whose result appears at the end of the next clock cycle.
TESTEN	I	Test enable. When GRLIB has been configured to use asynchronous reset then TESTEN selects if the internal reset signal should come from RESET or TESTRST.
TESTRST	I	Reset signal in test mode (TESTEN = High). Only used when GRLIB has been configured to use asynchronous reset,

45.4 Timing

An FP operation is started by providing the operands, opcode, rounding mode and id before rising edge. The operands need to be provided a small set-up time before a rising edge while all other signals are latched on rising edge.

The FPU is fully pipelined and a new operation can be started every clock cycle. The only exceptions are divide and square-root operations which require 16 to 26 clock cycles to complete, and which are not pipelined. Division and square-root are implemented through iterative series expansion algorithm. Since the algorithms basic step is multiplication the floating-point multiplier is shared between multiplication, division and square-root. Division and square-root do not occupy the multiplier during the whole operation and allow multiplication to be interleaved and executed parallelly with division or square-root.

One clock cycle before an operation is completed, the output signal RDY is asserted to indicate that the result of an FPU operation will appear on the output signals at the end of the next cycle. The id of the operation to be completed and allowed operations are reported on signals RESID and ALLOW. During the next clock cycle the result appears on RES, EXCEPT and CC outputs.

Figure 135 shows signal timing during four arithmetic operations on GRFPU.

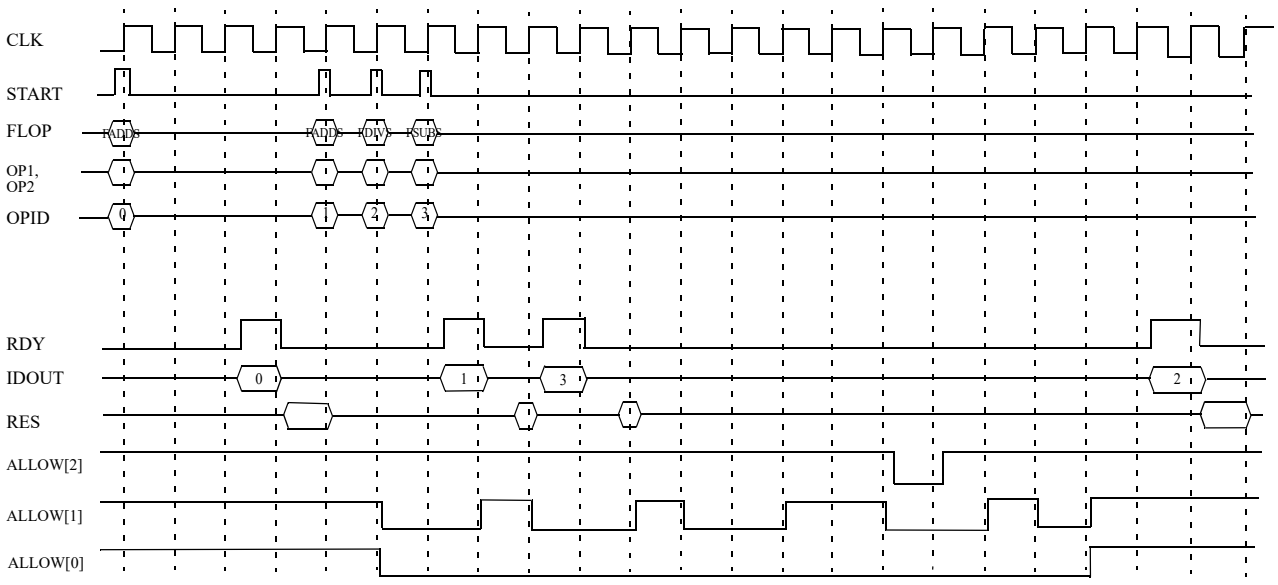


Figure 135. Signal timing

45.5 Shared FPU

45.5.1 Overview

In multi-processor systems, a single GRFPU can be shared between multiple CPU cores providing an area efficient solution. In this configuration, the GRFPU is extended with a wrapper. Each CPU core issues a request to execute a specific FP operation to the wrapper, which performs fair arbitration using the round-robin algorithm. When a CPU core has started a divide or square-root operation, the FPU is not able to accept a new division or square-root until the current operation has finished. Also, during the execution of a division or square-root, other operations cannot be accepted during certain cycles. This can lead to the, currently, highest prioritized CPU core being prevented from issuing an operation to the FPU. If this happens, the next CPU core that has a operation that can be started will be allowed to access the FPU and the current arbitration order will be saved. The arbitration order will be restored when the operation type that was prevented can be started. This allows the FPU resource

the be fairly shared between several CPU cores while at the same time allowing maximum utilization of the FPU.

In shared FPU configuration, GRFPU uses an 8 bit wide id for each operation. The three high-order bits are used to identify the CPU core which issued the FP operation, while the five low-order bits are used to enumerate FP operations issued by one core. FP operation flushing is not possible in shared FPU configuration.

45.5.2 Shared FPU and clock gating

Clock gating of LEON processors is typically implemented so that the clock for a processor core is gated off when the processor is idle. The clock for a shared FPU is typically gated off when the connected processors are all idle or have floating-point disabled.

This means that, in a shared FPU configuration, a processor may be clock gated off while the connected FPU continues to be clocked. The power-down instruction may overtake a previously issued floating-point instruction and cause the processor to be gated off before the floating-point operation has completed. This can in turn lead to the processor not reacting to the completion of the floating-point operation and to a subsequent processor freeze after the processor wakes up and continues to wait for the completion of the floating-point operation.

In order to avoid this, software must make sure that all floating-point operations have completed before the processor enters power-down. This is generally not a problem in real-world applications as the power-down instruction is typically used in a idle loop and floating-point results have been stored to memory before entering the idle loop. To make sure that there are no floating-point operations pending, software should perform a store of the %fsr register before the power-down instruction.

45.6 Implementation

45.6.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers, except synchronization registers, if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core will use asynchronous reset for all registers, except synchronization registers, if the GRLIB config package setting *grlib_async_reset_enable* is set.

46 GRFPC - GRFPU Control Unit

The GRFPU Control Unit (GRFPC) is used to attach the GRFPU to the LEON integer unit (IU). GRFPC performs scheduling, decoding and dispatching of the FP operations to the GRFPU as well as managing the floating-point register file, the floating-point state register (FSR) and the floating-point deferred-trap queue (FQ). Floating-point operations are executed in parallel with other integer instructions, the LEON integer pipeline is only stalled in case of operand or resource conflicts.

In the FT-version, all registers are protected with TMR and the floating-point register file is protected using parity coding.

46.1 Floating-Point register file

The GRFPU floating-point register file contains 32 32-bit floating-point registers (%f0-%f31). The register file is accessed by floating-point load and store instructions (LDF, LDDF, STD, STDF) and floating-point operate instructions (FPop).

46.2 Floating-Point State Register (FSR)

The GRFPC manages the floating-point state register (FSR) containing FPU mode and status information. All fields of the FSR register as defined in SPARC V8 specification are implemented and managed by the GRFPU conforming to the SPARC V8 specification and the IEEE-754 standard. Implementation-specific parts of the FSR managing are the NS (non-standard) bit and *ftt* field.

If the NS (non-standard) bit of the FSR register is set, all floating-point operations will be performed in non-standard mode as described in section 45.2.6. When the NS bit is cleared all operations are performed in standard IEEE-compliant mode.

Following floating-point trap types never occur and are therefore never set in the ftt field:
- unimplemented_FPop: all FPop operations are implemented
- hardware_error: non-resumable hardware error
- invalid_fp_register: no check that double-precision register is 0 mod 2 is performed

GRFPU implements the *qne* bit of the FSR register which reads 0 if the floating-point deferred-queue (FQ) is empty and 1 otherwise.

The FSR is accessed using LDFSR and STFSR instructions.

46.3 Floating-Point Exceptions and Floating-Point Deferred-Queue

GRFPU implements the SPARC deferred trap model for floating-point exceptions (fp_exception). A floating-point exception is caused by a floating-point instruction performing an operation resulting in one of following conditions:

- an operation raises IEEE floating-point exception (ftt = IEEE_754_exception) e.g. executing invalid operation such as 0/0 while the NVM bit of the TEM field id set (invalid exception enabled).
- an operation on denormalized floating-point numbers (in standard IEEE-mode) raises unfinished_FPop floating-point exception
- sequence error: abnormal error condition in the FPU due to the erroneous use of the floating-point instructions in the supervisor software.

The trap is deferred to one of the floating-point instructions (FPop, FP load/store, FP branch) following the trap-inducing instruction (note that this may not be next floating-point instruction in the program order due to exception-detecting mechanism and out-of-order instruction execution in the GRFPC). When the trap is taken the floating-point deferred-queue (FQ) contains the trap-inducing instruction and up to seven FPop instructions that were dispatched in the GRFPC but did not complete.

After the trap is taken the *qne* bit of the FSR is set and remains set until the FQ is emptied. The STDFQ instruction reads a double-word from the floating-point deferred queue, the first word is the address of the instruction and the second word is the instruction code. All instructions in the FQ are FPop type instructions. The first access to the FQ gives a double-word with the trap-inducing instruction, following double-words contain pending floating-point instructions. Supervisor software should emulate FPops from the FQ in the same order as they were read from the FQ.

Note that instructions in the FQ may not appear in the same order as the program order since GRFPU executes floating-point instructions out-of-order. A floating-point trap is never deferred past an instruction specifying source registers, destination registers or condition codes that could be modified by the trap-inducing instruction. Execution or emulation of instructions in the FQ by the supervisor software gives therefore the same FPU state as if the instructions were executed in the program order.

46.4 Implementation

46.4.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers, except synchronization registers, if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

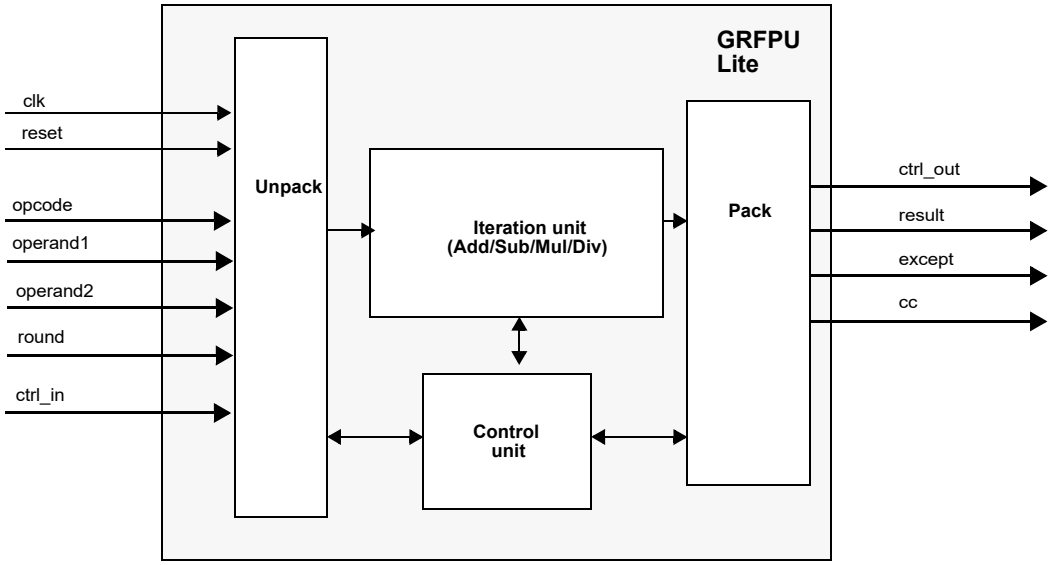
The GRFPC4 core will use asynchronous reset for all registers, except synchronization registers, if the GRLIB config package setting *grlib_async_reset_enable* is set. The GRFPC core does not support *grlib_async_reset_enable.*

47 GRFPU Lite - IEEE-754 Floating-Point Unit

47.1 Overview

The GRFPU Lite floating-point unit implements floating-point operations as defined in IEEE Standard for Binary Floating-Point Arithmetic (IEEE-754) and SPARC V8 standard (IEEE-1754).

Supported formats are single and double precision floating-point numbers. The floating-point unit is not pipelined and executes one floating-point operation at a time.



47.2 Functional Description

47.2.1 Floating-point number formats

The floating-point unit handles floating-point numbers in single or double precision format as defined in IEEE-754 standard.

47.2.2 FP operations

The floating-point unit supports four types of floating-point operations: arithmetic, compare, convert and move. The operations, summarised in the table below, implement all FP instructions specified by the SPARC V8 instruction set except FSMULD and instructions with quadruple precision.

Table 659.:Floating-point operations

Operation	Op1	Op2	Result	Exceptions	Description
Arithmetic operations					
FADDS FADDD	SP DP	SP DP	SP DP	NV, OF, UF, NX	Addition
FSUBS FSUBD	SP DP	SP DP	SP DP	NV, OF, UF, NX	Subtraction
FMULS FMULD	SP DP	SP DP	SP DP	NV, OF, UF, NX NV, OF, UF, NX	Multiplication
FDIVS FDIVD	SP DP	SP DP	SP DP	NV, OF, UF, NX, DZ	Division
FSQRTS FSQRTD	- -	SP DP	SP DP	NV, NX	Square-root
Conversion operations					
FITOS FITOD	-	INT	SP DP	NX -	Integer to floating-point conversion
FSTOI FDTOI	-	SP DP	INT	NV, NX	Floating-point to integer conversion. The result is rounded in round-to-zero mode.
FSTOD FDTOS	-	SP DP	DP SP	NV NV, OF, UF, NX	Conversion between floating-point formats
Comparison operations					
FCMPS FCMPD	SP DP	SP DP	CC	NV	Floating-point compare. Invalid exception is generated if either operand is a signaling NaN.
FCMPES FCMPED	SP DP	SP DP	CC	NV	Floating point compare. Invalid exception is generated if either operand is a NaN (quiet or signaling).
Negate, Absolute value and Move					
FABSS	-	SP	SP	-	Absolute value.
FNEGS	-	SP	SP	-	Negate.
FMOVS		SP	SP	-	Move. Copies operand to result output.

SP - single precision floating-point number

DP - double precision floating-point number

INT - 32 bit integer

CC - condition codes

NV, OF, UF, NX - floating-point exceptions, see section 47.2.3

Below is a table of worst-case throughput of the floating point unit.

*Table 660.*Worst-case instruction timing

Instruction	Throughput	Latency
FADDS, FADDD, FSUBS, FSUBD,FMULS, FMULD, FITOS, FITOD, FSTOI, FDTOI, FSTOD, FDTOS, FCMPS, FCMPD, FCMPES. FCMPED	8	8
FDIVS	31	31
FDIVD	57	57
FSQRTS	46	46
FSQRTD	65	65

47.2.3 Exceptions

The floating-point unit detects all exceptions defined by the IEEE-754 standard. This includes detection of Invalid Operation (NV), Overflow (OF), Underflow (UF), Division-by-Zero (DZ) and Inexact (NX) exception conditions. Generation of special results such as NaNs and infinity is also implemented.

47.2.4 Rounding

All four rounding modes defined in the IEEE-754 standard are supported: round-to-nearest, round-to-+inf, round-to--inf and round-to-zero.

47.3 Implementation

47.3.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

48 GRLFPC - GRFPU Lite Floating-point unit Controller

48.1 Overview

The GRFPU Lite Floating-Point Unit Controller (GRLFPC) is used to attach the GRFPU Lite floating-point unit (FPU) to the LEON integer unit (IU). It performs decoding and dispatching of the floating-point (FP) operations to the floating-point unit as well as managing the floating-point register file, the floating-point state register (FSR) and the floating-point deferred-trap queue (FQ).

The GRFPU Lite floating-point unit is not pipelined and executes only one instruction at a time. To improve performance, the controller (GRLFPC) allows the GRFPU Lite floating-point unit to execute in parallel with the processor pipeline as long as no new floating-point instructions are pending.

48.2 Floating-Point register file

The floating-point register file contains 32 32-bit floating-point registers (%f0-%f31). The register file is accessed by floating-point load and store instructions (LDF, LDDF, STD, STDF) and floating-point operate instructions (FPop).

In the FT-version, the floating-point register file is protected using 4-bit parity per 32-bit word. The controller is capable of detecting and correcting one bit error per byte. Errors are corrected using the instruction restart function in the IU.

48.3 Floating-Point State Register (FSR)

The controller manages the floating-point state register (FSR) containing FPU mode and status information. All fields of the FSR register as defined in SPARC V8 specification are implemented and managed by the controller conform to the SPARC V8 specification and IEEE-754 standard.

The non-standard bit of the FSR register is not used, all floating-point operations are performed in standard IEEE-compliant mode.

Following floating-point trap types never occur and are therefore never set in the ftt field:
- unimplemented_FPop: all FPop operations are implemented
- unfinished_FPop: all FPop operation complete with valid result
- invalid_fp_register: no check that double-precision register is 0 mod 2 is performed

The controller implements the *qne* bit of the FSR register which reads 0 if the floating-point deferred-queue (FQ) is empty and 1 otherwise. The FSR is accessed using LDFSR and STFSR instructions.

48.4 Floating-Point Exceptions and Floating-Point Deferred-Queue

The floating-point unit implements the SPARC deferred trap model for floating-point exceptions (fp_exception). A floating-point exception is caused by a floating-point instruction performing an operation resulting in one of following conditions:

- an operation raises IEEE floating-point exception (ftt = IEEE_754_exception) e.g. executing invalid operation such as 0/0 while the NVM bit of the TEM field id set (invalid exception enabled).
- sequence error: abnormal error condition in the FPU due to the erroneous use of the floating-point instructions in the supervisor software.
- hardware_error: uncorrectable parity error is detected in the FP register file

The trap is deferred to the next floating-point instruction (FPop, FP load/store, FP branch) following the trap-inducing instruction. When the trap is taken the floating-point deferred-queue (FQ) contains the trap-inducing instruction.

After the trap is taken the *qne* bit of the FSR is set and remains set until the FQ is emptied. STDFQ instruction reads a double-word from the floating-point deferred queue, the first word is the address of the instruction and the second word is the instruction code.

48.5 Implementation

48.5.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

49 GRGPIO - General Purpose I/O Port

49.1 Overview

The general purpose input output port core is a scalable and provides optional interrupt support. The port width can be set to 2 - 32 bits through the *nbits* VHDL generic. Interrupt generation and shaping is only available for those I/O lines where the corresponding bit in the *imask* VHDL generic has been set to 1.

Each bit in the general purpose input output port can be individually set to input or output, and can optionally generate an interrupt. For interrupt generation, the input can be filtered for polarity and level/edge detection.

It is possible to share GPIO pins with other signals. The output register can then be bypassed through the bypass register.

The figure 136 shows a diagram for one I/O line.

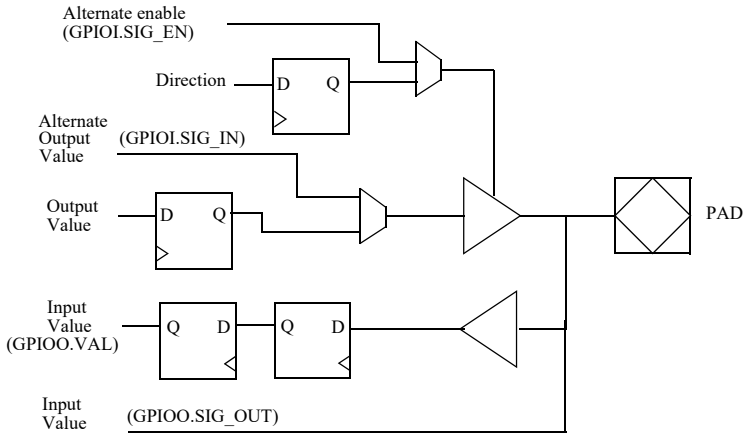


Figure 136. General Purpose I/O Port diagram

49.2 Operation

The I/O ports are implemented as bi-directional buffers with programmable output enable. The input from each buffer is synchronized by two flip-flops in series to remove potential meta-stability. The synchronized values can be read-out from the I/O port data register. They are also available on the GPIOO.VAL signals. The output enable is controlled by the I/O port direction register. A '1' in a bit position will enable the output buffer for the corresponding I/O line. The output value driven is taken from the I/O port output register.

The core can be implemented with one of three different alternatives for interrupt generation. Either each I/O line can drive a separate interrupt line on the APB interrupt bus, the interrupt line to use can be assigned dynamically for each I/O line, or one interrupt line can be shared for all I/O lines. In the fixed mapping with a separate interrupt line for each I/O line, the interrupt number is equal to the I/O line index plus an offset given by the first interrupt line assigned to the core, *pirq*, (PIO[1] = interrupt *pirq*+1, etc.). If the core has been implemented to support dynamic mapping of interrupts, each I/O line can be mapped using the Interrupt map register(s) to an interrupt line starting at interrupt *pirq*. When the core is implemented to drive one, fixed, shared interrupt line for all I/O lines, the core will drive interrupt line *pirq* only. The value of *pirq* can be read out from the core's AMBA plug'n'play information.

Interrupt generation is controlled by three registers: interrupt mask, polarity and edge registers. To enable an interrupt, the corresponding bit in the interrupt mask register must be set. If the edge register is '0', the interrupt is treated as level sensitive. If the polarity register is '0', the interrupt is active

low. If the polarity register is ‘1’, the interrupt is active high. If the edge register is ‘1’, the interrupt is edge-triggered. The polarity register then selects between rising edge (‘1’) or falling edge (‘0’).

The core can be implemented with a Interrupt flag register that can be used to determine if, and which, GPIO pine that caused an interrupt to be assered. The core implements the Interrupt flag register, and the Interrupt available register, if the IFL field in the core’s capability register is non-zero.

A GPIO pin can be shared with other signals. The ports that should have the capability to be shared are specified with the *bypass* generic (the corresponding bit in the generic must be 1). The unfiltered inputs are available through GPIOO.SIG_OUT and the alternate output value must be provided in GPIOI.SIG_IN. The bypass register then controls whether the alternate output is chosen. The direction of the GPIO pin can also be shared, if the corresponding bit is set in the *bpdir* generic. In such case, the output buffer is enabled when GPIOI.SIG_EN is active. The direction of the pin can also be made to depend on the bypass register. See the documentation of the *bpmode* VHDL generic for details.

A GPIO pin can also be toggled when a pulse is detected on an internal signal. If the pulse VHDL generic is nonzero, then the Pulse register is available in the core.

49.3 Registers

The core is programmed through registers mapped into APB address space.

Table 661. General Purpose I/O Port registers

APB address offset	Register
0x00	I/O port data register
0x04	I/O port output register
0x08	I/O port direction register
0x0C	Interrupt mask register
0x10	Interrupt polarity register
0x14	Interrupt edge register
0x18	Bypass register
0x1C	Capability register
0x20 - 0x3C	Interrupt map register(s). Address 0x20 + 4*n contains interrupt map registers for IO[4*n : 3+4+n], if implemented.
0x40	Interrupt available register, if implemented
0x44	Interrupt flag register, if implemented
0x48	Input enable register, if implemented
0x4C	Pulse register, if implemented
0x50	Input enable register, if implemented, logical-OR
0x54	I/O port output register, logical-OR
0x58	I/O port direction register, logical-OR
0x5C	Interrupt mask register, logical-OR
0x60	Input enable register, if implemented, logical-AND
0x64	I/O port output register, logical-AND
0x68	I/O port direction register, logical-AND
0x6C	Interrupt mask register, logical-AND
0x70	Input enable register, if implemented, logical-XOR
0x74	I/O port output register, logical-XOR
0x78	I/O port direction register, logical-XOR
0x7C	Interrupt mask register, logical-XOR

49.3.1 I/O Port Data Register

*Table 662.*0x00 - DATA - I/O port data register

31 nbits	nbits-1 0
RESERVED	DATA
0	*
r	r

nbits-1: 0 I/O port input value (DATA) - Data value read from GPIO lines

49.3.2 I/O Port Output Register

*Table 663.*0x04 - OUTPUT - I/O port output register

31 nbits	nbits-1 0
RESERVED	DATA
0	0
r	rw

nbits-1: 0 I/O port output value (DATA) - Output value for GPIO lines

49.3.3 I/O Port Direction Register

*Table 664.*0x08 - DIRECTION - I/O port direction register

31 nbits	nbits-1 0
RESERVED	DIR
0	0
r	rw

nbits-1: 0 I/O port direction value (DIR) - 0=output disabled, 1=output enabled

49.3.4 Interrupt Mask Register

*Table 665.*0x0C - IMASK - Interrupt mask register

31 nbits	nbits-1 0
RESERVED	MASK
0	0
r	rw

nbits-1: 0 Interrupt mask (MASK) - 0=interrupt masked, 1=intrrupt enabled

49.3.5 Interrupt Polarity Register

*Table 666.*0x10 - IPOL - Interrupt polarity register

31 nbits	nbits-1 0
RESERVED	POL
0	NR
r	rw

nbits-1: 0 Interrupt polarity (POL) - 0=low/falling, 1=high/rising

49.3.6 Interrupt Edge Register

*Table 667.*0x14 - IEDGE - Interrupt edge register

31 nbits	nbits-1 0
RESERVED	EDGE
0	NR
r	rw

nbits-1: 0 Interrupt edge (EDGE) - 0=level, 1=edge

49.3.7 Bypass Register

*Table 668.*0x18 - BYPASS - Bypass register

31 nbits	nbits-1 0
RESERVED	BYPASS
0	0
r	rw

nbits-1: 0 Bypass.(BYPASS) - 0=normal output, 1=alternate output

49.3.8 Capability Register

*Table 669.*0x1C - CAP - Capability register

31 18	17	16	15 13	12 8	7 5	4 0
RESERVED	PU	IER	IFL	r	IRQGEN	r	NLINES
0	*	*	*	0	0	0	*
r	r	r	r	r	r	r	r

18 PU: Pulse register implemented: If this field is '1' then the core implements the Pulse register.

This field is available in revision 2 and above of the GPIO port. This field is read-only.

17 IER: Input Enable register implemented. If this field is '1' then the core implements the Input enable register.

This field is available in revision 2 and above of the GPIO port. This field is read-only.

16 IFL: Interrupt flag register implemented. If this field is '1' then the core implements the Interrrupt available and Interrupt flag registers (registers at offsets 0x40 and 0x44).

This field is available in revision 2 and above of the GPIO port. This field is read-only.

12 8 IRQGEN: Interrupt generation setting: If irqgen = 0, I/O line n will drive interrupt line pirq + n, up to NAHBIRQ-1. No Interrupt map registers will be implemented. This is the default, and traditional, implementation of the core.

If irqgen = 1, all I/O lines capable of generating interrupts will use interrupt pirq and no Interrupt map registers are implemented.

If irqgen > 1, the core will include Interrupt map registers allowing software to dynamically map which lines that should drive interrupt lines [pirq : pirq+irqgen-1].

The value of pirq can be read out from the core's plug&play information.

This field is available in revision 2 and above of the GPIO port. This field is read-only.

4: 0 NLINES. Number of pins in GPIO port - 1. Compatibility note: This field is available in revision 2 and above of the GPIO port. This field is read-only.

49.3.9 Interrupt Map Register n

*Table 670.*0x20+un - IRQMAPRn - Interrupt map register n

31 29	28 24	23 21	20 16	15 13	12 8	7 6	4 0
RESERVED	IRQMAP[4*n]	RESERVED	IRQMAP[4*n+1]	RESERVED	IRQMAP[4*n+2]	RESERVED	IRQMAP[4*n+3]
0	un+i	0	un+i+1	0	un+i+2	0	uni+i+3
r	rw	r	rw	r	rw	r	rw

31: 0 IRQMAP[i] : The field IRQMAP[i] determines to which interrupt I/O line i is connected. If IRQMAP[i] is set to *x*, IO[i] will drive interrupt *pirq*+*x*. Where *pirq* is the first interrupt assigned to the core. Several I/O can be mapped to the same interrupt.

The core has one IRQMAP field per I/O line. The Interrupt map register at offset 0x20+*4*n* contains the IRQMAP fields for IO[*4*n* : *4*n+3*]. This means that the fields for IO[0:3] are located on offset 0x20, IO[4:7] on offset 0x24, IO[8:11] on offset 0x28, and so on. An I/O line's interrupt generation must be enabled in the Interrupt mask register in order for the I/O line to drive the interrupt specified by the IRQMAP field. The Interrupt map register(s) can only be written if the core was implemented with support for interrupt mapping.

49.3.10 Interrupt Available Register

*Table 671.*0x40 - IAVAIL - Interrupt available register

31 0
IMASK
*
r

31: 0 IMASK: Interrupt mask bit field. If IMASK[n] is 1 then GPIO line n can generate interrupts.

This register is not available in all implementations. See capability register.

49.3.11 Interrupt Flag Register

*Table 672.*0x44 - IFLAG - Interrupt flag register

31 0
IFLAG
0
wc

31: 0 IFLAG : If IFLAG[n] is set to '1' then GPIO line n has generated an interrupt. Write '1' to the orresponding bit to clear. Writes of '0' have no effect.

This register is not available in all implementations, see capability register.

49.3.12 Input Enable Register

*Table 673.*0x48 - IPEN - Input enable register

31 0
IPEN
0
rw

31: 0 IPEN : If IPEN[n] is set to '1' then values from GPIO line n will be visible in the data register. Otherwise the GPIO line input is gated-off to disable input signal propagation.

This register is not available in all implementations, see capability register.

49.3.13 Pulse Register

*Table 674.*0x4C - PULSE - Pulse register

31	0
PULSE	
0	
rw	

31: 0 PULSE : If PULSE[n] is set to '1' then I/O port output register bit n will be inverted whenever GPIOI.SIG_IN[n] is high.

This register is not available in all implementations, see capability register.

49.3.14 Logical-OR/AND/XOR Register

*Table 675.*0x54-0x7C - LOR,LAND,LXOR - Logical-OR/AND/XOR registers

31	0
VALUE	
-	
w*	

31: 0 The logical-OR/AND/XOR registers will update the corresponding register according to:

New value = <Old value> logical-op <Write data>

There exists logical-OR, AND and XOR registers for the Input enable, I/O port output, I/O port direction and Interrupt mask registers.

49.4 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x01A. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

49.5 Implementation

49.5.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support *grlib_async_reset_enable*. See also the description for the *syncrst* VHDL generic for how the core implements reset.

49.6 Configuration options

Table 676 shows the configuration options of the core (VHDL generics).

*Table 676.*Configuration options

Generic	Function	Allowed range	Default
pindex	Selects which APB select signal (PSEL) will be used to access the GPIO unit	0 to NAHBIRQ-1	0
paddr	The 12-bit MSB APB address	0 to 16#FFF#	0
pmask	The APB address mask	0 to 16#FFF#	16#FFF#
nbits	Defines the number of bits in the I/O port	1 to 32	8

*Table 676.*Configuration options

Generic	Function	Allowed range	Default
imask	Defines which I/O lines are provided with interrupt generation and shaping. Note that line 31 (out of lines 0 to 31 in a 32-bit GPIO port) cannot be configured to assert interrupts.	0 - 16#7FFFFFF#	0
oepol	Select polarity of output enable signals. 0 = active low, 1 = active high.	0 - 1	0
syncrst	Selects between synchronous (1) or asynchronous (0) reset during power-up. 0: Logic is placed on the output enable signals to keep them as inputs while reset is enabled. 1: The register controlling the output enable signals are reset with an asynchronous reset.	0 - 1	0
bypass	Defines which I/O lines are provided bypass capabilities. Note that line 31 (out of lines 0 to 31 in a 32-bit GPIO port) cannot be configured for bypass.	0 - 16#7FFFFFF#	0
scantest	Enable scan support for asyncronous-reset flip-flops	0 - 1	0
bpdir	Defines which I/O lines are provided output enable bypass capabilities. Note that line 31 (out of lines 0 to 31 in a 32-bit GPIO port) cannot be configured for bypass.	0 - 16#7FFFFFF#	0
pirq	First interrupt line that the core will drive. The core will only drive interrupt lines up to line NAHBIRQ-1. If NAHBIRQ is set to 32 and *pirq* is set to 16, the core will only be able to generate interrupts for I/O lines 0 - 15.	0 - NAHBIRQ-1	0
irqgen	This generic configures interrupt generation. If *irqgen* = 0, I/O line *n* will drive interrupt line *pirq* + *n*, up to NAHBIRQ-1. No Interrupt map registers will be implemented. This is the default, and traditional, implementation of the core. If *irqgen* = 1, all I/O lines capable of generating interrupts will use interrupt *pirq* and no Interrupt map registers will be implemented. If *irqgen* > 1, the core will include Interrupt map registers allowing software to dynamically map which lines that should drive interrupt lines [*pirq* : *pirq*+*irqgen*-1]	0 - NAHBIRQ-1	0
iflagreg	If this generic is set to 1 then the core will be implemented with the Interrupt available and Interrupt flag registers. If this generic is set to 1 then the IFL field in the core's capability register is also set.	0 - 1	0
bpmode	Controls if output enable bypass depends on the bypass register and the behaviour of the gpioi.sig_en inputs. If bpmode = 0 then gpioi.sig_en(i) enables GPIO line *i* and connects gpioi.sig_in(i) to the output, regardless of the value in the bypass register. If bpmode = 1 then the corresponding bit in the bypass register must be set to '1' for the output enable bypass to be active. When the bypass register is active then the gpioi.sig_en(i) controls the output enable of the corresponding GPIO line and gpioi.sig_in(i) is connected to the the corresponding output. In both cases, bit *i* in the bpdir VHDL generic must be set for the gpioi.sig_en(i) signal to have any effect.	0 - 1	0
inpen	If this generic is non-zero, then the core will be implemented with the Input enable register that can be used to prevent input signal propagation.	0 - 1	0

*Table 676.*Configuration options

Generic	Function	Allowed range	Default
doutresv	Reset value for output register		0
dirresv	Reset value for direction register		0
bpresv	Reset value for bypass register		0
inpresv	Reset value for input enable register (if implemented)		0
pulse	If this generic is non-zero, then the core will be implemented with the Pulse register and corresponding functionality.	0 - 1	0

49.7 Signal descriptions

Table 677 shows the interface signals of the core (VHDL ports).

*Table 677.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
GPIOO	OEN[31:0]	Output	I/O port output enable	see oepol
	DOUT[31:0]	Output	I/O port outputs	-
	VAL[31:0]	Output	The current (synchronized) value of the GPIO signals	-
	SIG_OUT[31:0]	Output	The current (unsynchronized) value of the GPIO signals. Note that this value is affected by the Input enable register, if implemented.	
GPIOI	DIN[31:0]	Input	I/O port inputs	-
	SIG_IN[31:0]	Input	Alternative output	-
	SIG_EN[31:0]	Input	Alternative output enable	High

* see GRLIB IP Library User's Manual

49.8 Signal definitions and reset values

The signals and their reset values are described in table 678.

*Table 678.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
gpio[]	Input/Output	General purpose input output	-	Tri-state

49.9 Timing

The timing waveforms and timing parameters are shown in figure 137 and are defined in table 679.

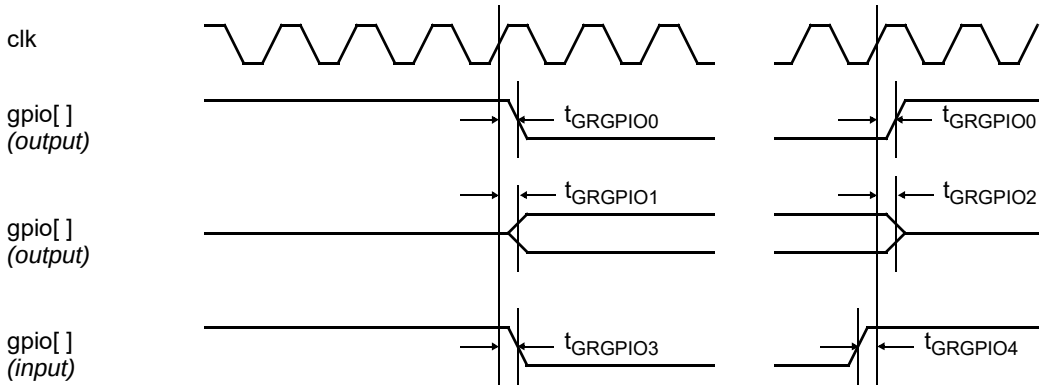


Figure 137. Timing waveforms

*Table 679.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{GRGPIO0}$	clock to output delay	rising *clk* edge	TBD	TBD	ns
$t_{GRGPIO1}$	clock to non-tri-state delay	rising *clk* edge	TBD	TBD	ns
$t_{GRGPIO2}$	clock to tri-state delay	rising *clk* edge	TBD	TBD	ns
$t_{GRGPIO3}$	input to clock hold	rising *clk* edge	-	-	ns
$t_{GRGPIO4}$	input to clock setup	rising *clk* edge	-	-	ns

Note: The *gpio* inputs are re-synchronized internally. The signals do not have to meet any setup or hold requirements.

49.10 Library dependencies

Table 680 shows libraries used when instantiating the core (VHDL libraries).

*Table 680.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	MISC	Signals, component	Component declaration

49.11 Component declaration

The core has the following component declaration.

```
ibrary gaisler;
use gaisler.misc.all;

entity grgpio is
  generic (
    pindex   : integer := 0;
    paddr    : integer := 0;
    pmask    : integer := 16#fff#;
    imask    : integer := 16#0000#;
    nbits    : integer := 16-- GPIO bits

  );
  port (
```

```
    rst    : in  std_ulogic;
    clk    : in  std_ulogic;
    apbi   : in  apb_slv_in_type;
    apbo   : out apb_slv_out_type;
    gpioi  : in  gpio_in_type;
    gpioo  : out gpio_out_type
  );
end;
```

49.12 Instantiation

This example shows how the core can be instantiated.

```
library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.misc.all;

signal gpti : gptimer_in_type;

begin

gpio0 : if CFG_GRGPIO_EN /= 0 generate     -- GR GPIO unit
    grgpio0: grgpio
      generic map( pindex => 11, paddr => 11, imask => CFG_GRGPIO_IMASK, nbits => 8)
      port map( rstn, clkm, apbi, apbo(11), gpioi, gpioo);

      pio_pads : for i in 0 to 7 generate
        pio_pad : iopad generic map (tech => padtech)
            port map (gpio(i), gpioo.dout(i), gpioo.oen(i), gpioi.din(i));
      end generate;
end generate;
```

50 GRGPREG - General Purpose Register

50.1 Overview

The core provides a programmable register that drives an output vector that can be used to control miscellaneous options in a design.

50.2 Operation

The core contains one register of configurable length that is mapped into APB address space. The value of this register is propagated to an output vector. The reset value of the register can be specified via VHDL generics, or via an input vector.

50.3 Registers

The core is programmed through registers mapped into APB address space.

*Table 681.*General purpose register registers

APB address offset	Register
0x00	General purpose register bits 31:0
0x04	General purpose register bits 63:0

50.3.1 General Purpose Register

*Table 682.*0x00 - GPREG0 - General purpose register

31 nbits	nbits-1 0
RESERVED	REGISTER BITS
0	*
r	rw

31:nbits RESERVED (not present if nbits >= 32)

nbits-1:0 Register bits. Position i corresponds to bit i in the core's output vector

50.3.2 General Purpose Register (extended)

*Table 683.*0x04 - GRPEG1 - General purpose register (extended)

31 nbits-32	nbits-33 0
RESERVED	REGISTER BITS
0	*
r	rw

31:nbits-32 RESERVED (not present if nbits = 64 or nbits <= 32)

nbits-33:0 Register bits. Position i corresponds to bit 31+i in the core's output vector (not present if nbits < 33)

50.4 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x087. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

50.5 Implementation

50.5.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset for its internal registers.

50.6 Configuration options

Table 684 shows the configuration options of the core (VHDL generics).

*Table 684.*Configuration options

Generic name	Function	Allowed range	Default
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	ADDR field of the APB BAR.	0 - 16#FFF#	0
pmask	MASK field of the APB BAR.	0 - 16#FFF#	16#FFF#
nbits	Number of register bits	1 - 64	16
rstval	Reset value for bits 31:0	0 - 16#FFFFFFFF#	0
rstval2	Reset value for bits 63:32	0 - 16#FFFFFFFF#	0
extrst	Use input vector *resval* to specify reset value. If this generic is 0 the register reset value is determined by VHDL generics *rstval* and *rstval2*. If this generic is 1, the reset value is specified by the input vector *resval*.	0 - 1	0

50.7 Signal descriptions

Table 685 shows the interface signals of the core (VHDL ports).

*Table 685.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
GRGPREGO	N/A	Output	Value of register mapped into APB address space	-
RESVAL	N/A	Input	(Optionally) specifes register reset value	-

* see GRLIB IP Library User's Manual

50.8 Library dependencies

Table 686 shows the libraries used when instantiating the core (VHDL libraries).

*Table 686.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	MISC	Component, signals	Component declaration, I2C signal definitions

50.9 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
```

```
use ieee.std_logic_1164.all;

library grlib, techmap;
use grlib.amba.all;

library gaisler;
use gaisler.misc.all;

entity grgpreg_ex is
  port (
    clkm  : in std_ulogic;
    rstn : in std_ulogic;

    -- I2C signals
    iic_scl : inout std_ulogic;
    iic_sda : inout std_ulogic
    );
end;

architecture rtl of i2c_ex is
  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);

  -- Width of general purpose register
  constant GRGPREG_NBITS : integer := 9;

  signal gprego           : std_logic_vector(GRGPREG_NBITS-1 downto 0);
  signal gpregresval      : std_logic_vector(GRGPREG_NBITS-1 downto 0);
begin

  -- AMBA Components are instantiated here
  ...

  -- General purpose register
  grgpreg0 : grgpreg                  -- General purpose register
    generic map (
      pindex  => 10,
      paddr   => 16#0a0#,
      pmask   => 16#fff#,
      nbits   => GRGPREG_NBITS,
      rstval  => 0,                   -- Not used
      rstval2 => 0,                   -- Not used
      extrst  => 1)                   -- Use input vector for reset value
    port map (
      rst     => rstn,
      clk     => clkm,
      apbi    => apbi,
      apbo    => apbo(10),
      gprego  => gprego,
      resval  => gpregresval);
end;
```

51 GRIOMMU - AHB/AHB bridge with access protection and address translation

51.1 Overview

The core is used to connect two AMBA AHB buses clocked by synchronous clocks with any frequency ratio. The two buses are connected through an interface pair consisting of an AHB slave and an AHB master interface. AHB transfer forwarding is performed in one direction, where AHB transfers to the slave interface are forwarded to the master interface. The core can be configured to provide access protection and address translation for AMBA accesses traversing over the core. Access protection can be provided using a bit vector to restrict access to memory. Access protection and address translation can also be provided using page tables in main memory, providing full IOMMU functionality. Both protection strategies allow devices to be placed into a configurable number of groups that share data structures located in main memory. The protection and address translation functionality provides protection for memory assigned to processes and operating systems from unwanted accesses by units capable of direct memory access.

Applications of the core include system partitioning, clock domain partitioning, system expansion and secure software partitioning.

Features offered by the core include:

- Single and burst AHB transfer forwarding
- Access protection and address translation that can provide full IOMMU functionality
- Devices can be placed into groups where a group shares page tables / access restriction vectors
- Hardware table-walk
- Efficient bus utilization through (optional) use of SPLIT response, data prefetching and posted writes. **NOTE:** SPLIT responses require an AHB arbiter that allows assertion of HSPLIT during second cycle of SPLIT response. This is supported by GRLIB's AHBCTRL IP core.
- Read and write combining, improves bus utilization and allows connecting cores with differing AMBA access size restrictions.
- Deadlock detection logic enables use of two uni-directional bridges to build a bi-directional bridge. The core can be connected with an another instance of the core, or with a uni-directional AHB/AHB bridge core (AHB2AHB), to form a bi-directional bridge.

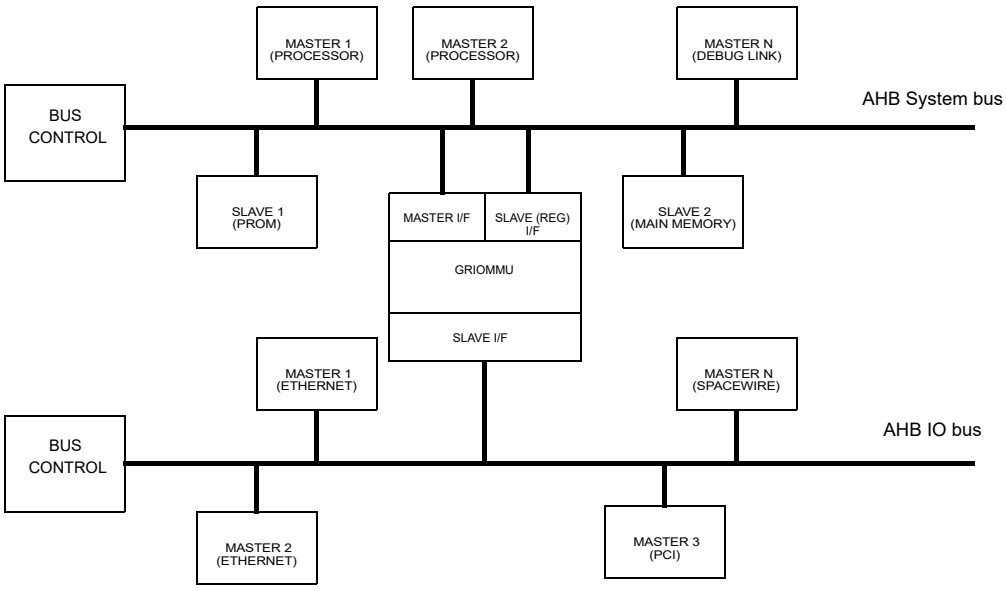


Figure 138. System with core providing access restricion/address translation for masters on AHB IO bus

51.2 Bridge operation

51.2.1 General

The first sub sections below describe the general AHB bridge function. The functionality providing access restriction and address translation is described starting with section 51.3. In the description of AHB accesses below the core propagates accesses from the IO bus to the System bus, see figure 138.

The address space occupied by the core on the IO bus is configurable and determined by Bank Address Registers in the slave interface's AHB Plug&Play configuration record.

The core is capable of handling single and burst transfers of all burst types. Supported transfer sizes (HSIZE) are BYTE, HALF-WORD, WORD, DWORD, 4WORD and 8WORD.

For AHB write transfers write data is always buffered in an internal FIFO implementing posted writes. For AHB read transfers the core uses GRLIB's AMBA Plug&Play information to determine whether the read data will be prefetched and buffered in an internal FIFO. If the target address for an AHB read burst transfer is a prefetchable location the read data will be prefetched and buffered.

The core can be implemented to use SPLIT responses or to insert wait states when handling an access. With SPLIT responses enabled, an AHB master initiating a read transfer to the core is always splitted on the first transfer attempt to allow other masters to use the slave bus while the core performs read transfer on the master bus. The descriptions of operation in the sections below assume that the core has been implemented with support for AMBA SPLIT responses. The effects of disabling support for AMBA SPLIT responses are described in section 51.2.11.

If interrupt forwarding is enabled the interrupts on the IO bus interrupt lines will be forwarded to the system bus and vice versa.

51.2.2 AHB read transfers

When a read transfer is registered on the slave interface connected to the IO bus, the core gives a SPLIT response. The master that initiated the transfer will be de-granted allowing other bus masters to use the slave bus while the core performs a read transfer on the master side. The master interface then requests the bus and starts the read transfer on the master side. Single transfers on the slave side are normally translated to single transfers with the same AHB address and control signals on the master side, however read combining can translate one access into several smaller accesses. Translation of burst transfers from the slave to the master side depends on the burst type, burst length, access size and core configuration.

If the read FIFO is enabled and the transfer is a burst transfer to a prefetchable location, the master interface will prefetch data in the internal read FIFO. If the splitted burst on the slave side was an incremental burst of unspecified length (INCR), the length of the burst is unknown. In this case the master interface performs an incremental burst up to a specified address boundary (determined by the VHDL generic *rburst).* The core can be configured to recognize an INCR read burst marked as instruction fetch (indicated on HPROT signal). In this case the prefetching on the master side is completed at the end of a cache line (the cache line size is configurable through the VHDL generic *iburst*). When the burst transfer is completed on the master side, the splitted master that initiated the transfer (on the slave side) is allowed in bus arbitration by asserting the appropriate HSPLIT signal to the AHB controller. The splitted master re-attempts the transfer and the core will return data with zero wait states.

If the read FIFO is disabled, or the burst is to non-prefetchable area, the burst transfer on the master side is performed using sequence of NONSEQ, BUSY and SEQ transfers. The first access in the burst on the master side is of NONSEQ type. Since the master interface can not decide whether the splitted burst will continue on the slave side or not, the system bus is held by performing BUSY transfers. On the slave side the splitted master that initiated the transfer is allowed in bus arbitration by asserting the HSPLIT signal to the AHB controller. The first access in the transfer is completed by returning read data. The next access in the transfer on the slave side is extended by asserting HREADY low. On the

master side the next access is started by performing a SEQ transfer (and then holding the bus using BUSY transfers). This sequence is repeated until the transfer is ended on the slave side.

In case of an ERROR response on the master side the ERROR response will be given for the same access (address) on the slave side. SPLIT and RETRY responses on the master side are re-attempted until an OKAY or ERROR response is received.

51.2.3 AHB write transfers

The core implements posted writes. During the AHB write transfer on the slave side the data is buffered in the internal write FIFO and the transfer is completed on the slave side by always giving an OKAY response. The master interface requests the bus and performs the write transfer when the master bus is granted. If the burst transfer crosses the write burst boundary (defined by VHDL generic *wburst*), a SPLIT response is given. When the core has written the contents of the FIFO out on the master side, the core will allow the master on the slave side to perform the remaining accesses of the write burst transfer.

Writes are accepted with zero wait states if the core is idle and the incoming access is not locked. If the incoming access is locked, each access will have one wait state. If write combining is disabled a non-locked BUSY cycle will lead to a flush of the write FIFO. If write combining is enabled or if the incoming access is locked, the core will not flush the write FIFO during the BUSY cycle.

51.2.4 Deadlock conditions

When two cores are used to form a bi-directional bridge, a deadlock situation can occur if the cores are simultaneously accessed from both buses. The core that has been configured as a slave contains deadlock detection logic which will resolve a deadlock condition by giving a RETRY response, or by issuing SPLIT complete followed by a new SPLIT response. When the core resolves a deadlock while prefetching data, any data in the prefetch buffer will be dropped when the core's slave interface issues the AMBA RETRY response. When the access is retried it may lead to the same memory locations being read twice.

Deadlock detection logic for bi-directional configurations may lead to deadlocks in other parts of the system. Consider the case where a processor on bus A on one side of the bidirectional bridge needs to perform an instruction fetch over the bridge before it can release a semaphore located in memory on bus A. Another processor on bus B, on the other side of the bridge, may spin on the semaphore waiting for its release. In this scenario, the accesses from the processor on bus B could, depending on system configuration, continuously trigger a deadlock condition where the core will drop data in, or be prevented from initiating, the instruction fetch for the processor on bus A. Due to scenarios of this kind the bridge should not be used in bi-directional configurations where dependencies as the one described above exist between the buses connected by the bridge.

Other deadlock conditions exist with locked transfers, see section 51.2.5.

51.2.5 Locked transfers

The core supports locked transfers. The master bus will be locked when the bus is granted and remain locked until the transfer completes on the slave side. Locked transfers can lead to deadlock conditions, the core's VHDL generic *lckdac* determines if and how the deadlock conditions are resolved.

With the VHDL generic *lckdac* set to 0, locked transfers may *not* be made after another read access which received SPLIT until the first read access has received split complete. This is because the core will return split complete for the first access first and wait for the first master to return. This will cause deadlock since the arbiter is not allowed to change master until a locked transfer has been completed. The AMBA specification requires that the locked transfer is handled before the previous transfer, which received a SPLIT response, is completed.

With *lckdac* set to 1, the core will respond with an AMBA ERROR response to locked access that is made while an ongoing read access has received a SPLIT response. With *lckdac* set to 2 the core will

save state for the read access that received a SPLIT response, allow the locked access to complete, and then complete the first access. All non-locked accesses from other masters will receive SPLIT responses until the saved data has been read out.

If the core is used to create a bi-directional bridge there is one more deadlock condition that may arise when locked accesses are made simultaneously in both directions. If the VHDL generic *lckdac* is set to 0 the core will deadlock. If *lckdac* is set to a non-zero value the slave bridge will resolve the deadlock condition by issuing an AMBA ERROR response to the incoming locked access.

51.2.6 Read and write combining

Read and write combining allows the core to assemble or split AMBA accesses on the core's slave interface into one or several accesses on the master interface. This functionality can improve bus utilization and also allows cores that have differing AMBA access size restrictions to communicate with each other. The functionality attained by read and write combining depends on the VHDL generics *rdcomb* (defines type of read combining), *wrcomb* (defines type of write combining), *slvmstaccsz* (defines maximum AHB access size supported by the core's slave interface) and *mstmaccsz* (defines maximum AHB access size that can be used by core's master interface). These VHDL generics are described in section 51.13. The table below shows the effect of different settings. BYTE and HALF-WORD accesses are special cases. The table does not list illegal combinations, for instance *mstmaccsz* /= *slvmaccsz* requires that *wrcomb* /= 0 and *rdcomb* /= 0.

*Table 687.*Read and write combining

Access on slave interface	Access size	wrcomb	rdcomb	Resulting access(es) on master interface
BYTE or HALF-WORD single read access to any area	-	-	-	Single access of same size
BYTE or HALF-WORD read burst to prefetchable area	-	-	-	Incremental read burst of same access size as on slave interface, the length is the same as the number of 32-bit words in the read buffer, but will not cross the read burst boundary.
BYTE or HALF-WORD read burst to non-prefetchable area	-	-	-	Incremental read burst of same access size as on slave interface, the length is the same as the length of the incoming burst. The master interface will insert BUSY cycles between the sequential accesses.
BYTE or HALF-WORD single write	-	-	-	Single access of same size
BYTE or HALF-WORD write burst	-	-	-	Incremental write burst of same size and length, the maximum length is the number of 32-bit words in the write FIFO.
Single read access to any area	Access size <= mstmaccsz	-	-	Single access of same size
Single read access to any area	Access size > mstmaccsz	-	1	Sequence of single accesses of mstmaccsz. Number of accesses: (access size)/mstmaccsz
Single read access to any area	Access size > mstmaccsz	-	2	Burst of accesses of size mstmaccsz. Length of burst: (access size)/mstmaccsz
Read burst to prefetchable area	-	-	0	Burst of accesses of incoming access size up to address boundary defined by rburst.
Read burst to prefetchable area	-	-	1 or 2	Burst of accesses of size mstmaccsz up to address boundary defined by rburst.
Read burst to non-prefetchable area	Access size <= mstmaccsz	-	-	Incremental read burst of same access size as on slave interface, the length is the same as the length of the incoming burst. The master interface will insert BUSY cycles between the sequential accesses.

*Table 687.*Read and write combining

Access on slave interface	Access size	wrcomb	rdcomb	Resulting access(es) on master interface
Read burst to non-prefetch-able area	Access size > mstmaccsz	-	1 or 2	Burst of accesses of size mstmaccsz. Length of burst: (incoming burst length)*(access size)/mstmaccsz
Single write	Access size <= mstmaccsz	-	-	Single write access of same size
Single write	Access size > mstmaccsz	1	-	Sequence of single access of mstmaccsz. Number of accesses: (access size)/mstmaccsz.
Single write	Access size > mstmaccsz	2	-	Burst of accesses of mstmaccsz. Length of burst: (access size)/mstmaccsz.
Write burst	-	0	-	Burst of same size as incoming burst, up to address boundary defined by VHDL generic wburst.
Write burst	-	1 or 2	-	Burst write of maximum possible size. The core will use the maximum size (up to mstmaccsz) that it can use to empty the write buffer.

Read and write combining prevents the bridge from propagating fixed length bursts and wrapping bursts. See section 51.2.7 for a discussion on burst operation.

Read and write combining with VHDL generics *wrcomb/rdcomb* set to 1 cause the core to use single accesses when dividing an incoming access into several smaller accesses. This means that another master on the bus may write or read parts of the memory area to be accessed by the core before the core has read or written all the data. In bi-directional configurations, an incoming access on the master core may cause a collision that aborts the operation on the slave core. This may cause the core to read the same memory locations twice. This is normally not a problem when accessing memory areas. The same issues apply when using an AHB arbiter that performs early burst termination. The standard GRLIB AHBCTRL core does not perform early burst termination.

To ensure that the core does not re-read an address, and that all data in an access from the core's slave interface is propagated out on the master interface without interruption the VHDL generics *rdcomb* and *wrcomb* should both be set to 0 or 2. In addition to this, the AHB arbiter may not perform early burst termination (early burst termination is not performed by the GRLIB AHBCTRL arbiter).

Read and write combining can be limited to specified address ranges. See description of the *combmask* VHDL generic for more information. Note that if the core is implemented with support for prefetch and read combining, it will not obey combmask for prefetch operations (burst read to prefetchable areas). Prefetch operations will always be performed with the maximum allowed size on the master interface.

51.2.7 Burst operation

The core can be configured to support all AMBA 2.0 burst types (single access, incrementing burst of unspecified length, fixed length incrementing bursts and wrapping bursts). Single accesses and incrementing bursts of unspecified length have previously been discussed in this document. An incoming single access will lead to one access, or multiple accesses for some cases with read/write combining, on the other side of the bridge. An incoming incrementing burst of unspecified length to a prefetchable area will lead to the prefetch buffer (if available) being filled using the same access size, or the maximum allowed access size if read/write combining is enabled, on the master interface.

If the core is used in a system where no fixed length bursts or incremental bursts will be used in accesses to the bridge, then set the *allbrst* generic to 0 and skip the remainder of this section.

The VHDL generic *allbrst* controls if the core will support fixed length and wrapping burst accesses. If *allbrst* is set to 0, the core will treat all burst accesses as incrementing of unspecified length. For fixed length and wrapping bursts this can lead to performance penalties and malfunctions. Support for

fixed length and wrapping bursts is enabled by setting *allbrst* to 1 or 2. Table 51.2.7 describes how the core will handle different burst types depending on the setting of *allbrst*.

*Table 688.*Burst handling

Value of allbrst generic	**Access type***	**Undefined length incrementing burst INCR**	**Fixed length incrementing burst INCR{4,8,16}**	**Wrapping burst WRAP{4,8,16}**
0	Reads to non-prefetchable area	Incrementing burst with BUSY cycles inserted. Same behaviour with read and write combining.	Fixed length burst with BUSY cycles inserted. If the burst is short then the burst may end with a BUSY cycle. If access combining is used the HBURST signal will get incorrect values.	Malfunction. Not supported
	Reads to prefetchable area	Incrementing burst of maximum allowed size, filling prefetch buffer, starting at address boundary defined by prefetch buffer.		Malfunction. Not supported
	Write burst	Incrementing burst	Incrementing burst, if write combining is enabled, and triggered, the burst will be translated to an incrementing burst of undefined length. VHDL generic *wrcomb* should not be set to 1 (but to 0 or 2) in this case	Write combining is not supported. Same access size will be used on both sides of the bridge.
1	Reads to non-prefetchable area	Incrementing burst with BUSY cycles inserted. Same behaviour with read and write combining.	Same burst type with BUSY cycles inserted. If read combining is enabled, and triggered by the incoming access size, an incremental burst of unspecified length will be used. If the burst is short then the burst may end with a BUSY cycle.	Same burst type with BUSY cycles inserted. If read combining is enabled, and triggered by the incoming access size, an incremental burst of unspecified length will be used. This will cause AMBA violations if the wrapping burst does not start from offset 0.
	Reads to prefetchable area	Incrementing burst of maximum allowed size, filling prefetch buffer.	For reads, the core will perform full (or part that fits in prefetch buffer) fixed/wrapping burst on master interface and then respond with data. No BUSY cycles are inserted. If the access made to the slave interface is larger than the maximum supported access size on the master interface then a incrementing burst of unspecified length will be used to fill the prefetch buffer. This (read combining) is not supported for wrapping bursts.	
	Write burst	Same as for allbrst = 0		
2	Reads to non-prefetchable area	Incrementing burst with BUSY cycles inserted. Same behaviour with read and write combining.	Reads are treated as a prefetchable burst. See below.	
	Reads to prefetchable area	Incrementing burst of maximum allowed size, filling prefetch buffer, starting at address boundary defined by prefetch buffer.	Core will perform full (or part that fits in prefetch buffer) fixed/wrapping burst on master interface and then respond with data. No BUSY cycles are inserted. If the access made to the slave interface is larger than the maximum supported access size on the master interface then a incrementing burst of unspecified length will be used to fill the prefetch buffer. This (read combining) is not supported for wrapping bursts.	
	Write burst	Same as for allbrst = 0		

* Access to prefetchable area where the core's prefetch buffer is ised (VHDL generic pfen /= 0).

51.2.8 Transaction ordering, starvation and AMBA arbitration schemes

The core is configured at implementation to use one of two available schemes to handle incoming accesses. The core will issue SPLIT responses when it is busy and on incoming read accesses. If the core has been configured to use first-come, first-served ordering it will keep track of the order of incoming accesses and serve the requests in the same order. If first-come, first-served ordering is disabled the core will give some advantage to the master it has a response for and then allow all masters in to arbitration simultaneously, moving the decision on which master that should be allowed to access the core to the bus arbitration.

When designing a system containing a core the expected traffic patterns should be analyzed. The designer must be aware how SPLIT responses affect arbitration and how the selected transaction ordering in the core will affect the system. The two different schemes are further described in sections 51.2.9 and 51.2.10.

51.2.9 First-come, first-served ordering

First-come, first served ordering is used when the VHDL generic *fcfs* is non-zero.

With first-come, first-served ordering the core will keep track of the order of incoming accesses. The accesses will then be served in the same order. For instance, if master 0 initiates an access to the core, followed by master 3 and then master 5, the core will propagate the access from master 0 (and respond with SPLIT on a read access) and then respond with SPLIT to the other masters. When the core has a response for master 0, this master will be allowed in arbitration again by the core asserting HSPLIT. When the core has finished serving master 0 it will allow the next queued master in arbitration, in this case master 3. Other incoming masters will receive SPLIT responses and will not be allowed in arbitration until all previous masters have been served.

An incoming locked access will always be given precedence over any other masters in the queue.

A burst that has initiated a pre-fetch operation will receive SPLIT and be inserted last in the master queue if the burst is longer than the maximum burst length that the core has been configured for.

It should be noted that first-come, first-served ordering may not work well in systems where an AHB master needs to have higher priority compared to the other masters. The core will not prioritize any master, except for masters performing locked accesses.

51.2.10 Bus arbiter ordering

Bus arbiter ordering is used when VHDL generic *fcfs* is set to zero.

When several masters have received SPLIT and the core has a response for one of these masters, the master with the queued response will be allowed in to bus arbitration by the core asserting the corresponding HSPLIT signal. In the following clock cycle, all other masters that have received SPLIT responses will also be allowed in bus arbitration as the core asserts their HSPLIT signals simultaneously. By doing this the core defers the decision on the master to be granted next to the AHB arbiter. The core does not show any preference based on the order in which it issued SPLIT responses to masters, except to the master that initially started a read or write operation. Care has been taken so that the core shows a consistent behavior when issuing SPLIT responses. For instance, the core could be simplified if it could issue a SPLIT response just to be able to change state, and not initiate a new operation, to an access coming after an access that read out prefetched data. When the core entered its idle state it could then allow all masters in bus arbitration and resume normal operation. That solution could lead to starvation issues such as:

T0: Master 1 and Master 2 have received SPLIT responses, the core is prefetching data for Master 1

T1: Master 1 is allowed in bus arbitration by setting the corresponding HSPLIT

T2: Master 1 reads out prefetch data, Master 2 HSPLIT is asserted to let Master 2 in to bus arbitration

T3: Master 2 performs an access, receives SPLIT, however the core does not initiate an access, it just stalls in order to enter its idle state.

T4: Master 2 is allowed in to bus arbitration, Master 1 initiates an access that leads to a prefetch and Master 1 receives a SPLIT response

T5: Master 2 performs an access, receives SPLIT since the core is prefetching data for master 1

T6: Go back to T0

This pattern will repeat until Master 1 backs away from the bus and Master 2 is able to make an access that starts an operation over the core. In most systems it is unlikely that this behavior would introduce a bus lock. However, the case above could lead to an unexpectedly long time for Master 2 to complete its access. Please note that the example above is illustrative and the problem does not exist in the core as the core does not issue SPLIT responses to (non-locked) accesses in order to just change state but a similar pattern could appear as a result of decisions taken by the AHB arbiter if Master 1 is given higher priority than Master 2.

In the case of write operations the scenario is slightly different. The core will accept a write immediately and will not issue a SPLIT response. While the core is busy performing the write on the master side it will issue SPLIT responses to all incoming accesses. When the core has completed the write operation on the master side it will continue to issue SPLIT responses to any incoming access until there is a cycle where the core does not receive an access. In this cycle the core will assert HSPLIT for all masters that have received a SPLIT response and return to its idle state. The first master to access the core in the idle state will be able to start a new operation. This can lead to the following behavior:

T0: Master 1 performs a write operation, does NOT receive a SPLIT response

T1: Master 2 accesses the core and receives a SPLIT response

T2: The core now switches state to idle since the write completed and asserts HSPLIT for Master 2.

T3: Master 1 is before Master 2 in the arbitration order and we are back at T0.

In order to avoid this last pattern the core would have to keep track of the order in which it has issued SPLIT responses and then assert HSPLIT in the same order. This is done with first-come, first-served ordering described in section 51.2.9.

51.2.11 AMBA SPLIT support

Support for AMBA SPLIT responses is enabled/disabled through the VHDL generic *split*. SPLIT support should be enabled for most systems. The benefits of using SPLIT responses is that the bus on the core's slave interface side can be free while the core is performing an operation on the master side. This will allow other masters to access the bus and generally improve system performance. The use of SPLIT responses also allows First-come, first-served transaction ordering.

For configurations where the core is the only slave interface on a bus, it can be beneficial to implement the core without support for AMBA SPLIT responses. Removing support for SPLIT responses reduces the area used by the core and may also reduce the time required to perform accesses that traverse the core. It should be noted that building a bi-directional core without support for SPLIT responses will increase the risk of access collisions.

If SPLIT support is disabled the core will insert wait states where it would otherwise issue a SPLIT response. This means that the arbitration ordering will be left to the bus arbiter and the core cannot be implemented with the First-come, first-served transaction ordering scheme. The core will still issue RETRY responses to resolve dead lock conditions, to split up long burst and also when the core is busy emptying it's write buffer on the master side.

The core may also be implemented with dynamic SPLIT support, this allows the use of SPLIT responses to be configurable via the core's register interface (see SP field in the core's Control register).

51.2.12 Core latency

The delay incurred when performing an access over the core depends on several parameters such as core configuration, the operating frequency of the AMBA buses, AMBA bus widths and memory access patterns. This section deals with latencies in the core's bridge function. Access protection mechanisms may add additional delays, please refer to the description of access protection for a description of any additional delays.

Table 689 below shows core behavior in a system where both AMBA buses are running at the same frequency and the core has been configured to use AMBA SPLIT responses. Table 690 further down shows core behavior in the same system without support for SPLIT responses.

*Table 689.*Example of single read with FFACT = 1, and SPLIT support

Clock cycle	Core slave side activity	Core master side activity
0	Discovers access and transitions from idle state	Idle
1	Slave side waits for master side, SPLIT response is given to incoming access, any new incoming accesses also receive SPLIT responses.	Discovers slave side transition. Master interface output signals are assigned.
2		If bus access is granted, perform address phase. Otherwise wait for bus grant.
3		Register read data and transition to data ready state.
4	Discovers that read data is ready, assign read data output and assign SPLIT complete	Idle
5	SPLIT complete output is HIGH	
6	Typically a wait cycle for the SPLIT:ed master to be allowed into arbitration. Core waits for master to return. Other masters receive SPLIT responses.	
7	Master has been allowed into arbitration and performs address phase. Core keeps HREADY high	
8	Access data phase. Core has returned to idle state.	

*Table 690.*Example of single read with FFACT = 1, without SPLIT support

Clock cycle	Core slave side activity	Core master side activity
0	Discovers access and transitions from idle state	Idle
1	Slave side waits for master side, wait states are inserted on the AMBA bus.	Discovers slave side transition. Master interface output signals are assigned.
2		Bus access is granted, perform address phase.
3		Register read data and transition to data ready state.
4	Discovers that read data is ready, assign HREADY output register and data output register.	Idle
5	HREADY is driven on AMBA bus. Core has returned to idle state	

While the transitions shown in tables 689 and 690 are simplified they give an accurate view of the core delay. If the master interface needs to wait for a bus grant or if the read operation receives wait states, these cycles must be added to the cycle count in the tables. The behavior of the core with a fre-

quency factor of two between the buses is shown in tables 691 and 692 (best case, delay may be larger depending on which slave clock cycle an access is made to the core).

*Table 691.*Example of single read with FFACT = 2, Master freq. > Slave freq, without SPLIT support

Slave side clock cycle	Core slave side activity	Master side clock cycle	Core master side activity
0	Discovers access and transitions from idle state	0	Discovers slave side transition. Master interface output signals are assigned.
1	Slave side waits for master side, wait states are inserted on the AMBA bus.		
2		1	Bus access is granted, perform address phase.
3			
4		2	Register read data and transition to data ready state.
5			
6	Discovers that read data is ready, assign HREADY output register and data output register.	3	Idle
7	HREADY is driven on AMBA bus. Core has returned to idle state		

*Table 692.*Example of single read with FFACT = 2, Master freq. > Slave freq, without SPLIT support

Slave side clock cycle	Core slave side activity	Master side clock cycle	Core master side activity
0	Discovers access and transitions from idle state	0	Idle
		1	
1	Slave side waits for master side, wait states are inserted on the AMBA bus.	2	Discovers slave side transition. Master interface output signals are assigned.
		3	Bus access is granted, perform address phase.
2	Discovers that read data is ready, assign HREADY output register and data output register.	4	Register read data and transition to data ready state.
		5	Idle
3	HREADY is driven on AMBA bus. Core has returned to idle state	6	
		7	

Table 693 below lists the delays incurred for single operations that traverse the bridge while the bridge is in its idle state. The second column shows the number of cycles it takes the master side to perform the requested access, this column assumes that the master slave gets access to the bus immediately and that each access is completed with zero wait states. The table only includes the delay incurred by traversing the core. For instance, when the access initiating master reads the core's prefetch buffer, each additional read will consume one clock cycle. However, this delay would also have been present if the master accessed any other slave.

Write accesses are accepted with zero wait states if the bridge is idle, this means that performing a write to the idle core does not incur any extra latency. However, the core must complete the write operation on the master side before it can handle a new access on the slave side. If the core has not transitioned into its idle state, pending the completion of an earlier access, the delay suffered by an access be longer than what is shown in the tables in this section. Accesses may also suffer increased delays during collisions when the core has been instantiated to form a bi-directional bridge. Locked accesses that abort on-going read operations will also mean additional delays.

If the core has been implemented to use AMBA SPLIT responses there will be an additional delay where, typically, one cycle is required for the arbiter to react to the assertion of HSPLIT and one clock cycle for the repetition of the address phase.

Note that if the core has support for read and/or write combining, the number of cycles required for the master will change depending on the access size and length of the incoming burst access. For instance, in a system where the bus in the core's master side is wider than the bus on the slave side, write combining will allow the core to accept writes with zero wait states and then combine several accesses into one or several larger access. Depending on memory controller implementation this could reduce the time required to move data to external memory, and will reduce the load on the master side bus.

*Table 693.*Access latencies

Access	Master acc. cycles	Slave cycles	Delay incurred by performing access over core
Single read	3	1	1 * clk_{slv} + 3 * clk_{mst}
Burst read with prefetch	2 + (burst length)[x]	2	2 * clk_{slv} + (2 + burst length)* clk_{mst}
Single write[xx]	(2)	0	0
Burst write[xx]	(2 + (burst length))	0	0

[x] A prefetch operation ends at the address boundary defined by the prefetch buffer's size

[xx] The core implements posted writes, the number of cycles taken by the master side can only affect the next access.

51.2.13 Endianness

The core is designed for big-endian systems.

51.3 General access protection and address translation

51.3.1 Overview

The core provides two types of access protection. The first option is to use a bit vector to implement access restriction on a memory page basis. The second option is to use a page-table to provide access restriction and address translation. Regardless of the protection strategy, the core provides means to assign masters on the IO bus in groups where each group can be associated with a data structure (access restriction vector or page table) in memory. The core can be implemented to support a dynamically configurable page size from 4 to 512 KiB, or a fixed page size of 4 KiB.

When a master on the IO bus initiates an access to be propagated by the core, the core will first look at the incoming master's group assignment setting to determine to which group the master belongs. When the group is known, the core can propagate or inhibit the access based on the group's attributes, or determine the address of the in-memory data structures to use for access checks (and possibly address translation). The in-memory data structure may be cached by the core, otherwise the information will be fetched from main memory.

Once the core has the necessary information to process the incoming access, the access will be either allowed to propagate through the core or, in case the access is to a restricted memory location, be inhibited. If the access is inhibited, the core will issue an AMBA ERROR response to the master if the incoming access is a read access. The core implements posted writes, therefore write operations will not receive an AMBA ERROR response. An interrupt can, optionally, be asserted when an access is inhibited. The AHB failing access register can be configured to log the first or most recent access that was inhibited.

When enabled, the core always checks access permissions when a master initiates an access. For the access protection and translation operation to be effective the masters are required to adhere to the AMBA 2.0 specification and not issue burst transfers that cross a 1 KiB address boundary.

It is possible for masters to access the core's register interface through the core. In this case the core will perform an access to itself on the System AHB bus. For configurations where the core is used to form a bi-directional core, any data structures read by the core must be located on the same bus as the core's master interface. The core cannot access data structures that are placed on the same bus as masters that the core protects against, in other words data structures must be accessible on a slave on the System bus, see figure 138.

51.3.2 Delays incurred from access protection

The time required for the core's master interface to start an access may be delayed by access protection checks. Table 694 below shows the added delays, please refer to section 51.2.12 for a description of delays from the core's bridge operation.

*Table 694.*Access protection check latencies

Protection mode	Delay in clock cycles on master side
Disabled	0
Write-protection only and read access	0
Master assigned to group in passthrough or inactive group	1
Access Protection Vector, cache hit	1
Access Protection Vector cache miss, cache disabled/not implemented	Minimum[x] 4 clock cycles
IOMMU Protection, cache hit	1
IOMMU Protection, TLB miss, TLB disabled/not implemented	Minimum[x] 4 clock cycles

[x] The core may suffer additional AMBA bus delays when accessing the vector in memory. 4 cycles is the minimum time required and assumes that the core is instantly granted access to the bus and that data is delivered with zero wait states.

51.4 Access Protection Vector

The Access Protection Vector (APV) consists of a continuous bit vector where each bit determines the access rights to a memory page. The bit vector provides access restriction on the full 4 GiB AMBA address space. The required size of the bit vector depends on the page size used by the core, see table below:

*Table 695.*Bit vector size vs. page size

Page size	Bit vector size
4 KiB	128 KiB
8 KiB	64 KiB
16 KiB	32 KiB
32 KiB	16 KiB
64 KiB	8 KiB
128 KiB	4 KiB
256 KiB	2 KiB
512 KiB	1 KiB

Each group can have a bit vector with a base address specified by a field in the group's Group Control Register. When a master performs an access to the core, the master's group number is used to select one of the available bit vectors. The AMBA access size used to fetch the vector is fixed at implementation time and can be read out from the core's Capability register 1. If the AMBA access size to use is 32-bits (WORD sized) and the page size is 4 KiB, bits 31:17 of the incoming address (HADDR) are used to index a word in the bit vector, and bits HADDR[16:12] are used to select one of the 32 bits in the word. For each increase in AMBA access size (DWORD, 4WORD, 8WORD), one bit less of the

physical address is used to index the vector and this bit is instead used to select one specific bit in the data read from memory. Similarly, for each increase in page size one bit less of the physical address is used.

The lowest page is protected by the most significant bit in the bit vector. This means that page 0 is protected by the most significant bit in byte 0 read from the bit vector's base address (using big endian addressing). When performing WORD accesses, the lowest page is protected by bit 31 in the accessed word (using the bit numbering convention used throughout this document).

If the bit at the selected position is '0', the access to the page is allowed and the core will propagate the access. If the selected bit is '1', and the access is an read access, an AMBA ERROR response is given to the master initiating the access. If the selected bit is '1', and the access is a write access, the write is inhibited (not propagated through the core).

51.4.1 Access Protection Vector cache

The core can be implemented with an internal memory that caches the Access Protection Vector. The cache size is configurable at implementation time and depends on a number of parameters that can be read out via Capability registers 0 and 1. If the core has been implemented with IOMMU functionality and a IOMMU Translation Lookaside Buffer (TLB), the RAMs in the APV cache will be shared with the IOMMU TLB.

The cache is implemented as a direct-mapped cache built up of one data RAM and one tag RAM. The number of locations in each RAM is the number of lines in the cache. The width of the data RAM (cache line size) is the same as the size of the AMBA accesses used to fetch the APV from main memory. The width and contents of the tag RAM depends on the number of supported groups, cache line size and number of lines in the cache.

The address used to select a position in the RAMs, called the set address, must have *log2(number of lines in the cache)* bits. The number of address bits taken from the physical address required to uniquely address one position in the bit vector depends on the cache line size. The number of required bits for each allowed cache line size is shown in table 696 below.

*Table 696.*Cache line size vs. physical address bits

Cache line size in bits	Bits of physical address needed to identify one position depending on page size							
	4 KiB	8 KiB	16 KiB	32 KiB	64 KiB	128 KiB	256 KiB	512 KiB
32	15	14	13	12	11	10	9	8
64	14	13	12	11	10	9	8	7
128	13	12	11	10	9	8	7	6
256	12	11	10	9	8	7	6	5

If the core has support for more than one group, the cache must also be tagged with the group ID. The number of bits required to uniquely select one group is *log2(number of groups)*.

This means that in order to be able to cache the full bit vectors for all supported groups the cache address (set address) must have *log2(number of groups) + (required physical address bits)* address bits. The number of required lines in the cache to be able to hold all vectors is:

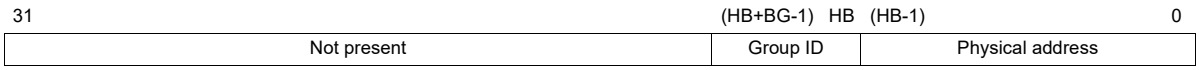
*cache lines = (number of groups) * (2^{20} / (cache line size))*

If the cache size is not large enough to hold a copy of each position in the bit vector, part of the physical address and group will be placed in the cache tag RAM instead. If the number of lines in the cache allows keeping a cached data of all positions in all bit vectors, the set address and tag data arrangement shown in table 697 will be used.

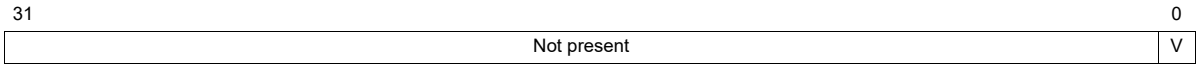
For the set address/tag RAM tables below the following values are used:

SB = Set address bits = log2(cache line size)
HB = Required number of bits of physical address = See table 696 above.
GB = Required number of bits to select one group = *log2(number of groups)*

*Table 697.*Set address bits = (group ID bits) + (Physical address bits)
Set address:



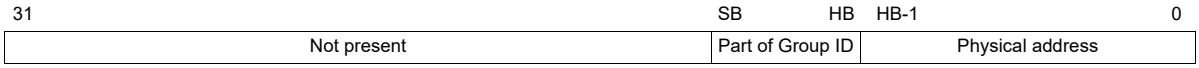
Contents of Tag RAM:



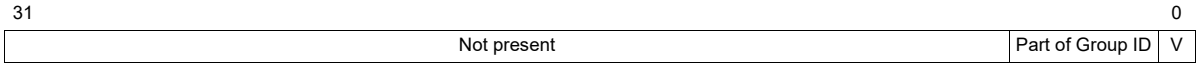
0 Valid (V) - Signals that addressed position in cache contains valid data

If the number of lines in the cache allows part of the group ID to be part of the set address, the arrangement will be:

*Table 698.*Set address bits < (group ID bits) + (Physical address bits)
Set address:



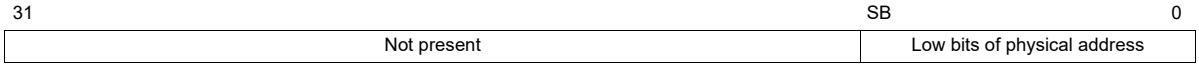
Contents of Tag RAM:



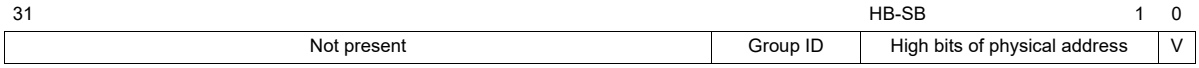
0 Valid (V) - Signals that addressed position in cache contains valid data

If the number of lines in the cache only allows part of the required physical address to be part of the set address, the arrangement will be:

*Table 699.*Set address bits < (group ID bits) + (Physical address bits)
Set address:



Contents of Tag RAM:



0 Valid (V) - Signals that addressed position in cache contains valid data

In the first arrangement, where *(set address bits) = (group ID bits) + (physical address bits)*, there will never be a collision in the cache. In the two other arrangements there is not room for all positions in the bit vector(s). This means that a cached copy for one memory page can be replaced with the bit vector for another memory page. Since the physical address is used as the set address, accesses from a master assigned to one group may evict cached bit vector data belonging to another group. This may not be wanted in systems where interference between groups of masters should be minimized. In order to minimize inter-group interference, the core can be implemented with support for using as much of the group ID as possible in the set address, this functionality is called group-set-addressing.

The core has support for group-set-addressing if the CA field in Capability register 0 is non-zero. If the number of set address bits (cache lines) is large enough to cache all bit vectors, the set address and

tag RAM arrangement will be as described by table 697. If the number of set address bits will allow the whole group ID to be part of the set address, the arrangement will be:

*Table 700.*Group set address: Set address bits < (group ID bits) + (Physical address bits)

Set address:

31	SB	GB-1	0
Not present	Low bits of physical address	Group ID	

Contents of Tag RAM:

31	1	0
Not present	High bits of physical address	V

0 Valid (V) - Signals that addressed position in cache contains valid data

If only part of the group ID can be used for the set address, the arrangement will be:

*Table 701.*Group set address: Set address bits < (group ID bits)

Set address:

31	GB-SB-1	0
Not present	Low part of Group ID	

Contents of Tag RAM:

31		1	0
Not present	Physical address	High part of group ID	V

0 Valid (V) - Signals that addressed position in cache contains valid data

Group-set-addressing is enabled via the GS field in the core's Control register.

51.4.2 Constraining the memory area covered by the APV cache

In a typical system, the normal case for an AMBA master core is to perform accesses to main memory. In order to reduce latency, the protection data for these accesses is ideally cached within the core. However, main memory is not likely to occupy the full AMBA address range. If accesses outside a certain access range is expected to be rare, and if it is not critical if these accesses suffer a higher latency, it can be beneficial to restrict the memory range for which the core caches the Access Protection Vector. The benefit of this is that the cache size can be reduced while the same hit rate is kept for the specified memory area, alternatively the hit rate could possibly be increased while keeping the cache size constant.

The core can be configured at implementation to only cache the bit vector for a specified memory range. Capability register 1 contains an address and a mask that describes this area. Bit vector data for the specified memory range will be cached by the core. Bit vector data for accesses made outside the memory range will not be placed in the cache, and will instead be fetched for memory on each access. The impact of having a non-zero mask in Capability register 1 is that for each '1' in the mask, one physical address bit can be removed from the cache set address in the examples given earlier in this section.

51.4.3 Access Protection Vector cache flush operation

If the contents of a vector is modified the core cache must be flushed by writing to the TLB/Cache Flush Register. The TLB/Cache Flush register contains fields to flush the entire cache or to flush the lines belonging to a specified group. In order to flush entries for a specific group, group-set-addressing must be implemented and enabled. Performing a group flush without group-set-addressing may only flush part of the cache and can lead to unexpected behavior.

The core will not propagate any transfers while a cache flush operation is in progress.

51.5 IO Memory Management Unit (IOMMU) functionality

The IOMMU functionality of the core provides address translation and access protection on the full 4 GiB AMBA address space. The size of the address range where addresses are translated is specified by the IOMMU Translation Range (ITR) field in the core's Control register:

*Size of translated address range in MiB = 16 MiB * 2^{ITR}*

The maximum allowed value of the ITR field is eight, which means that the IOMMU can provide address translation to an area of size $16*2^8$ = 4096 MiB, which is the full 32-bit address space. When ITR is set to eight and a page size of 4 KiB is used, bits 31:12 of the incoming IO address are translated to physical addresses, using IO Page Tables entries describes below. Bits 11:0 of the incoming access are propagated through the IOMMU. For each increase in page size one more bit will be directly propagated through the IOMMU instead of being translated.

If ITR is less then eight the most significant bits of the IO address must match the value of the TMASK field in Capability register 2. If an access is outside the range specified by TMASK the access will be inhibited. Table 702 shows the the effect of different ITR values. As an example, with ITR set to 2, the IOMMU will perform address translation for a range that spans 64 MiB. This range will be located at offset TMASK[31:26]. Accesses to addresses that do not have their most significant bits set to match TMASK[31:26] will be inhibited. The table also shows the number of pages within the decoded range and the memory required to hold the translation information (page tables) in main memory. The *pgsz* value is the value of the PGSZ field in the control register.

*Table 702.*Effects of IOMMU Translation Range setting

ITR	Size of translated range	TMASK bits used	Number of pages	Size of page tables
0	16 MiB	TMASK[31:24]	4096 / 2^{pgsz}	16 / 2^{pgsz} KiB
1	32 MiB	TMASK[31:25]	8192 / 2^{pgsz}	32 / 2^{pgsz} KiB
2	64 MiB	TMASK[31:26]	16384 / 2^{pgsz}	64 / 2^{pgsz}KiB
3	128 MiB	TMASK[31:27]	32768 / 2^{pgsz}	128 / 2^{pgsz} KiB
4	256 MiB	TMASK[31:28]	655536 / 2^{pgsz}	256 / 2^{pgsz} KiB
5	512 MiB	TMASK[31:29]	131072 / 2^{pgsz}	512 / 2^{pgsz} KiB
6	1024 MiB	TMASK[31:30]	262144 / 2^{pgsz}	1 / 2^{pgsz} MiB
7	2048 MiB	TMASK[31]	524288 / 2^{pgsz}	2 / 2^{pgsz} MiB
8	4096 MiB	TMASK not used	1048576 / 2^{pgsz}	4 / 2^{pgsz} MiB

51.5.1 IO Page Table Entry

Address translation is performed by looking up translation information in a one-level table present in main memory. Part of the incoming address is used to index the table that consists of IO Page Table Entries. The format of an IO Page Table Entry (IOPTE) is shown in table 703 below.

*Table 703.*IOMMU Page Table Entry (IOPTE)

31 … 8	7	6 … 5	4	3	2	1	0
PPAGE	C	R	BO	BS	W	V	R

31:8	Physical Page (PPAGE) - Bits 27:8 of this field corresponds to physical address bits 31:12 of the page. With a 4 KiB page size, PPAGE[27:8] is concatenated with the incoming IO address bits [11:0] to form the translated address. For each increase in page size one bit less of PPAGE is used and one bit more of the incoming IO address is used: this means that with a 16 KiB page size , PPAGE[27:10] will be concatenated with the incoming IO address bits [13:0] to form the translated address. Bits 31:27 of this field are currently discarded by the IOMMU and are present in the data structure for forward compatibility with systems using 36-bit AMBA address space.
7	Cacheable (C) - This field is currently not used by the IOMMU
6:5	RESERVED
4	Bus select Override (BO) - If this field is set to ‘1’ then the bus selection is made via the IOPTE.BS field.
3	Bus Select (BS) - Overrides master configuration register BS field when BO field in this PTE is set.
2	Writeable (W) - If this field is ‘1’ write access is allowed to the page. If this field is ‘0’, only read accesses are allowed.
1	Valid (V) - If this field is ‘1’ the PTE is valid. If this field is ‘0’, accesses to the page covered by this PTE will be inhibited.
0	RESERVED

When the core has IOMMU protection enabled all, incoming accesses from masters belonging to an active group, which is not in pass-through mode, will be matched against TMASK. If an access is outside the range specified by ITR/TMASK, the access will be inhibited and may receive an AMBA ERROR response (not applicable when the access is a posted write).

If the incoming access is within the range specified by ITR/TMASK, the core will use the incoming IO address to index the page table containing the address translation information for the master/IO address. The core may be implemented with an Translation Lookaside Buffer (TLB) that may hold a cached copy of the translation information. Otherwise the translation information will be fetched from main memory. The base address of the page table to use is given by the Group Configuration register to which the master performing the access is assigned. Please see the register description of the Group Configuration register for constraints on the page table base address. The core will use bits X:Y to index the table, where X depends on the value of the ITR field in the core’s Control register, and Y depends on the page size (Y = 12 + PGSZ field in Control register).

When the core has fetched the translation information (IOPTE) for the accesses page it will check the IOPTE’s Valid (V) and Writeable (W) fields. If the IOPTE is invalid, the access will be inhibited. If the Writeable (W) field is unset and the access is a write access, the access will be inhibited. Otherwise the core will, for a page size of 4 KiB, use the IOPTE field PPAGE, bits 27:8, and bits 11:0 of the incoming IO address to form the physical address to use when the access is propagated by the core (physical address: PPAGE[27:8] & IOADDR[11:0]).

If the valid (V) bit of the IOPTE is ‘0’ the core may or may not store the IOPTE in the TLB (if implemented). This is controlled via the SIV field in the core’s Control register.

51.5.2 Prefetch operations and IOMMU protection

During normal bridge operation, and with Access Protection Vector protection, the core determines if data for an access can be prefetched by looking at the IO address and the System bus plug and play

information. This operation cannot be done without introducing additional delays when the core is using IOMMU protection. The incoming IO address must first be translated before it can be determined if the access is to a memory area that can be prefetched. In order to minimize delays the core makes the assumption that any incoming burst access is to a prefetchable area. The result is that when using IOMMU protection all burst accesses will result in the core performing a prefetch operation.

51.5.3 Translation Lookaside Buffer operation

The core can be implemented with an internal memory that caches IO Page Table Entries. This memory is referred to as a Translation Lookaside Buffer (TLB). The TLB size is configurable at implementation time and depends on a number of parameters that can be read out via Capability registers 0 and 2. If the core has been implemented with Access Protection Vector functionality and an APV cache, the RAMs for the APV cache will be shared with the IOMMU TLB.

The TLB is implemented as a direct-mapped cache built up of one data RAM and one tag RAM. The number of locations in each RAM is the number of entries in the TLB. The width of the data RAM (entry size) is the same as the size of the AMBA accesses used to fetch page table entries from main memory. The width and contents of the tag RAM depends on the number of supported groups, entry size and number of entries in the TLB.

The address used to select a position in the RAMs, called the set address, must have *log2(number of entries in the TLB)* bits. The number of address bits taken from the physical address required to uniquely address one position in the TLB depends on the entry size. The number of required bits for each allowed entry size is shown in table 696 below, the values in the third column is the number of address bits that must be used to accommodate the largest translatable range (maximum value of ITR field in the core's Control register). Note that an entry size larger than 32 bits results in an TLB that holds multiple IOPTEs per entry.

*Table 704.*TLB entry size vs. physical address bits

Entry size in bits	Entry size in IOPTEs	Bits of physical address needed to identify one position depending on page size							
		4 KiB	8 KiB	16 KiB	32 KiB	64 KiB	128 KiB	256 KiB	512 KiB
32	1	20	19	18	17	16	15	14	13
64	2	19	18	17	16	15	14	13	12
128	4	18	17	16	15	14	13	12	11
256	8	17	16	15	14	13	12	11	10

If the core has support for more than one group, the TLB entries must also be tagged with the group ID. The number of bits required to uniquely select one group is *log2(number of groups)*.

This means that in order to be able to cache the page tables for all supported groups the TLB address (set address) must have *log2(number of groups) + (required physical address bits)* address bits. The number of required entries in the TLB to be able to hold all vectors is:

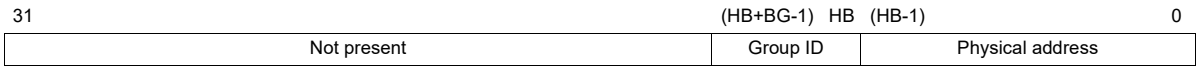
*TLB entries = (number of groups) * (2^{20} / (entry size))*

If the TLB is not large enough to hold a copy of each position in the page table, part of the physical address and group will be placed in the tag RAM. The core will implement the TLB depending on the parameters mentioned above. If the number of entries in the TLB allows keeping a copy of all positions in all page tables, the set address and tag data arrangement shown in table 705 will be used.

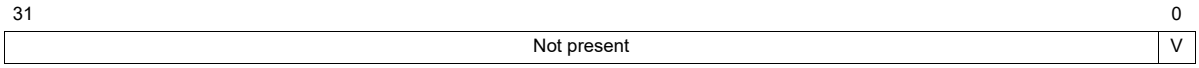
For the set address/tag RAM tables below the following values are used:

SB = Set address bits = log2(number of TLB entries)
HB = Required number of bits of physical address = See table 704 above.
GB = Required number of bits to select one group = *log2(number of groups)*

*Table 705.*Set address bits = (group ID bits) + (Physical address bits)
Set address:



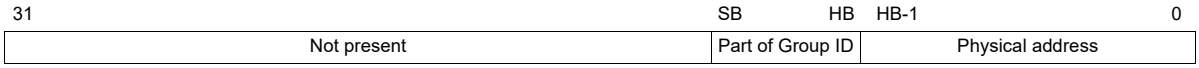
Contents of Tag RAM:



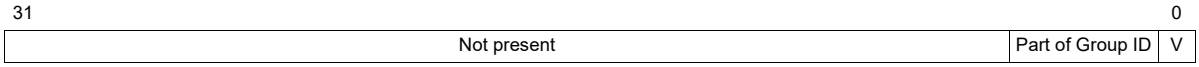
0 Valid (V) - Signals that addressed position in cache contains valid data

If the number of entries in the TLB allows part of the group ID to be part of the set address, the arrangement will be:

*Table 706.*Set address bits < (group ID bits) + (Physical address bits)
Set address:



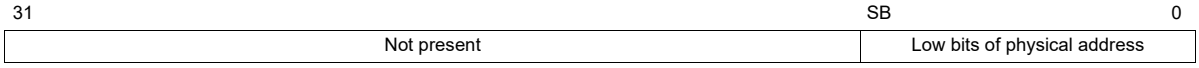
Contents of Tag RAM:



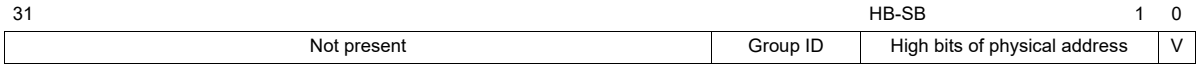
0 Valid (V) - Signals that addressed position in cache contains valid data

If the number of entries in the TLB only allows part of the required physical address to be part of the set address, the arrangement will be:

*Table 707.*Set address bits < (group ID bits) + (Physical address bits)
Set address:



Contents of Tag RAM:



0 Valid (V) - Signals that addressed position in cache contains valid data

In the first arrangement, where *(set address bits) = (group ID bits) + (physical address bits)*, there will never be a collision in the TLB. In the two other arrangements there is not room for all entries in the page table(s). This means that a cached IOPTE for one memory page can be replaced with the IOPTE for another memory page. Since the physical address is used as the set address, accesses from a master assigned to one group may evict cached IOPTE's belonging to another group. This may not be wanted in systems where interference between groups of masters should be minimized. In order to minimize inter-group interference, the core can be implemented with support for using as much of the group ID as possible in the set address, this functionality is called group-set-addressing.

The core has support for group-set-addressing if the IT field in Capability register 0 is non-zero. If the number of set address bits (TLB entries) is large enough to cache all page tables, the set address and

tag RAM arrangement will be as described by table 705. If the number of set address bits will allow the whole group ID to be part of the set address, the arrangement will be:

*Table 708.*Group set address: Set address bits < (group ID bits) + (Physical address bits)

Set address:

31	SB	(GB-1)	0
Not present	Low bits of physi-cal address	Group ID	

Contents of Tag RAM:

31	1	0
Not present	High bits of physical address	V

0 Valid (V) - Signals that addressed position in cache contains valid data

If only part of the group ID can be used for the set address, the arrangement will be:

*Table 709.*Group set address: Set address bits < (group ID bits)

Set address:

31	GB-SB-1	0
Not present	Low part of group ID	

Contents of Tag RAM:

31		1	0
Not present	Physical address	High part of Group ID	V

0 Valid (V) - Signals that addressed position in cache contains valid data

Group-set-addressing is enabled via the GS field in the core's Control register.

51.5.4 TLB flush operation

If the contents of a page table is modified the TLB must be flushed by writing to the TLB/Cache Flush Register. The TLB/Cache Flush register contains fields to flush the entire TLB or to flush the entries belonging to a specified group. In order to flush entries for a specific group, group-set-addressing must be implemented and enabled. Performing a group flush without group-set-addressing may only flush part of the TLB and can lead to unexpected behavior.

When working in IOMMU mode, the core can be configured to not store a IOPTE in the TLB if the IOPTE's valid (V) bit is cleared. This behavior is controller via the SIV field in the core's Control register.

The core will not propagate any transfers while a flush operation is in progress.

51.6 Fault-tolerance

In order to attain fault-tolerance the core should be implemented with inferred memory technology for the read buffer, write buffer and any FCFS buffer. This will implement the buffers in flip-flops and the core must then be implemented using techniques such as radiation hardened registers or TMR insertion.

The Access Protection Vector cache and IOMMU TLB can be implemented with the same options as above or using non-protected memory cells. When using non-protected memory cells the core can be implemented to use byte-parity to protect entries in the cache/TLB. If an error is detected it will be processed as a cache/TLB miss and the data will be re-read from main memory. A detected error will also be reported via the core's status register and the core also has support for signaling errors via its statistic output.

Errors can be injected in the Access Protection Vector cache and IOMMU TLB via the Data and Tag RAM Error Injection registers.

51.7 Statistics

In order to record statistics, a LEON4 Statistics Unit should be connected to the core. The core has the following statistics outputs:

*Table 710.*IOMMU Statistics

Output	Description
hit	High for one cycle during TLB/cache hit.
miss	High for one cycle during TLB/cache miss
pass	High for one cycle during passthrough access
accok	High for one cycle during access allowed
accerr	High for one cycle during access denied
walk	High while core is busy performing a table walk or accessing the access protection vector
lookup	High while core is performing cache lookup/table walk
perr	High for one cycle when core detects a parity error in the APV cache

51.8 Multi-bus bridge

The core can be instantiated in a version with two AHB master interfaces. These interfaces can be connected to separate AHB buses. The top-level entity griommu_mb contains additional signals for the second AHB master interface. Using the griommu_mb entity will enable bus select fields in the core's master configuration registers and the LB field in the core's control register. The bus select fields in the Master configuration registers allows the user to select which AHB master interface that should be used for accesses initiated by a specific master. The control register field LB selects which AHB master interfaces that should be used when the core fetches IOPTEs or APV bit vector data from memory.

Note that the bus selection in registers is active even if the core is disabled through the core's control register.

51.9 ASMP support

In some systems there may be a need to have separated instances of software each controlling a group of masters. In this case, sharing of the IOMMU register interface may not be wanted as it would allow software to modify the protection settings for a group of masters that belongs to another software instance. The core can be implemented with ASMP support to support systems where software entities are separated by address space. In this case, the core's register interface is mirrored on different 4 KiB pages. Different write protection settings can be set for each mirrored block of registers. This allows use of a memory management unit to control that software running can write to one, and only one, subset of registers.

When ASMP support is enabled, the field NARB in Capability register 0 is non-zero. The value of NARB tells how many ASMP register blocks that are available. Each ASMP register block mirrors the standard register set described in section 51.10 with the addition that some registers may be write protected. Table 711 contains a column that shows if a register is writable when accessed from an ASMP register block. The core's Control register, Master configuration register(s), Diagnostic cache registers, the ASMP access control register(s) can never be written via ASMP register block. These registers are only available in the first register set starting at the core register set base address. ASMP register block *n* is mapped at an offset *n**0x1000 from the core's register base address.

Software should first set up the IOMMU and assign the masters into groups. Then the ASMP control registers should be configured to constrain which registers that can be written from each ASMP block. After this initialization is done, other parts of the software environment can be brought up.

As an example, consider the case where OS A will control masters 0, 1 and 4 while OS B will control masters 2 and 3. In this case it may be appropriate to map masters 0, 1 and 4 to group 0 and master 2 and 3 to group 1. The ASMP access control registers can then be configured to only allow accesses to the Group control register for group 0 from ASMP register block 1 and likewise only allow accesses to the Group control register for group 1 from ASMP register block 2.

OS A will then map in ASMP register block 1 (registers within page located at core base offset + 0x1000) and OS B will then map in ASMP register block 2 (registers within page located at core base offset + 0x2000). This way OS a will be able to change the base address and the properties of group 0, containing its masters, without being able to change the protection mechanisms of group 1 belonging to OS B. Note that since an OS is able to flush the TLB/cache it is able to impact the I/O performance of masters assigned to other OS instances. Also note that care must be taken when clearing status bits and setting the mask register that controls interrupt generation.

51.10 Registers

The core is programmed through registers mapped into AHB I/O address space. All accesses to register address space must be made with word (32-bit) accesses.

*Table 711.*GRIOMMU registers

AHB address offset	Register	Writable in ASMP block
0x00	Capability register 0	No
0x04	Capability register 1	No
0x08	Capability register 2	No
0x0C	Reserved	-
0x10	Control register	No
0x14	TLB/cache flush register	Yes, protected**
0x18	Status register	Yes, protected**
0x1C	Interrupt mask register	Yes, protected**
0x20	AHB Failing Access register	No
0x24 - 0x3C	Reserved, must not be accessed	-
0x40 - 0x7C	Master configuration registers. Master n configuration register is located at offset 0x40 + n*0x4.	No
0x80-0xBC	Group control registers. Group n's control register is located at offset 0x80 + n*0x4.	Yes, protected**
0xC0	Diagnostic cache access register	No
0xC4 - 0xE0	Diagnostic cache access data registers 0 - 7	No
0xE4	Diagnostic cache access tag register	No
0xE8	Data RAM error injection register	No
0xEC	Tag RAM error injection register	No
0xF0 - 0xFF	Reserved, must not be accessed	No
0x100 - 0x13F	ASMP access control registers. The control register for ASMP block n is located at offset 0x100+n*0x4.	No

* Register is duplicated in ASMP register block at offset 0x1000 + register offset. The number of ASMP register blocks is given by the NARB field in Capability register 0. ASMP register block *n* starts at offset *n**0x1000. Register is only writable if allowed by the corresponding ASMP access control register field.

51.10.1 Capability Register 0

*Table 712.*0x00 - LAP0 - Capability register 0

31	30	29	28	27 24	23 20	19	18 17	16	15	14	13	12	11 9	8	7 4	3 0
A	AC	CA	CP	RESERVED	NARB	CS	FT	ST	I	IT	IA	IP	RESERVED	MB	GRPS	MSTS
*	*	*	*	0	*	*	*	*	*	*	*	*	0	*	*	*
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

31 Access Protection Vector (A) - If this bit is ‘1’, the core has support for Access Protection Vector

30 Access Protection Vector Cache (AC) - If this bit is ‘1’, the core has a internal cache for Access Protection vector lookups.

29 Access Protection Vector Cache Addressing (CA):
0: Core only supports standard addressing, group number is used as tag
1: Core supports using group ID as part of cache set address

28 Access Protection Vector Cache Pipeline (CP) - If this bit is set to ‘1’ the core has a pipeline stage added on the APV cache’s address. This means one cycle additional latency.

27:24 RESERVED

23:20 ASMP Register Blocks (NARB) - This field contains the number of ASMP register blocks that the core implements. If this field is non-zero the core has NARB ASMP register blocks with the first block starting at offset 0x1000 and the last block starting at offset NARB*0x1000.

19 Configurable Page Size (CS) - If this bit is ‘1’ the core supports several page sizes and the size is set via the Control register field PGSZ. If this bit is ‘0’, a fixed page size of 4 KiB is used.

18:17 Fault Tolerance (FT) - “00” - No fault tolerance, “01” - APV cache and/or IOMMU TLB is protected by parity

16 Statistics (S) - If this field is ‘1’ the core collects statistics

15 IOMMU functionality enable (I) - If this bit is ‘1’, the core has support for IOMMU functionality.

14 IOMMU TLB (IT) - If this bit is ‘1’, the core has an IOMMU Translation Lookaside Buffer (TLB)

13 IOMMU Addressing (IA):
0: Core only supports standard addressing, group number is used as tag
1: Core supports using group ID as part of TLB set address

12 IOMMU TLB Address Pipeline (IP) - If this bit is set to ‘1’ the core has a pipeline stage added on the TLB’s address. This means one cycle additional latency.

11:9 RESERVED

8 Multi-bus (MB) - Set to 1 if core is connected to two system buses.

7:4 Number of groups (GRPS) - Number of groups that the core has been implemented to support - 1.

3:0 Numbers of masters (MSTS) - Number of masters that the core has been implemented to support - 1.

Reset value: Implementation dependent

51.10.2 Capability Register 1

*Table 713.*0x04 - LAP1 - Capability register 1

31 20	19 16	15 8	7 5	4 0
CADDR	CMASK	CTAGBITS	CISIZE	CLINES
*	*	*	*	*
r	r	r	r	r

31:20 Access Protection Vector Cacheable Address (CADDR) - If the CMASK field of this register is non-zero the CADDR and CMASK fields specify the base address of the memory area protected by the part of the bit vector that can be cached by the core.

19:16 Access Protection Vector Cacheable Mask (CMASK) - Number of '1's in the Access Protection Vector Cachable mask. If the core is implemented with a Access Protection Vector cache and this value is non-zero, the CMASK field together with the CADDR field specify a memory area protected by a part of the bit vector that can be cached by the core. The CMASK value corresponds to the number of most significant bits of the CADDR field that are matched against the incoming AMBA address when determining if the protection bits for the memory area should be cached. As an example, if CMASK is 1 and CADDR is 0x000, the core will cache protection information for the address range 0x00000000 - 0x7FFFFFFF. With the same mask and CADDR = 0x800, the core would cache protection information for the address range 0x80000000 - 0xFFFFFFFF.

15:8 Access Protection Vector Cache Tag bits (CTAGBITS) - The width in bits of the Access Protection Vector cache's tags.

7:5 Access Protection Vector Access size (CSIZE) - This field indicates the AMBA access size used when accessing the Access Protection Vector in main memory. This is also the cache line size for the APV cache (if enabled). The values are:
000: 32-bit (4 byte)
001: 64-bit (8 byte)
010: 128-bit (16 byte)
011: 256-bit (32-byte)

4:0 Access Protection Vector Cache Lines (CLINES) - Number of lines in the Access Protection Vector cache. The number of lines in the cache is 2^{CLINES}.

51.10.3 Capability Register 2

*Table 714.*0x04 - CAP2 - Capability register 2

31 24	23 20	19 18	17 16	15 8	7 5	4 0
TMASK	RESERVED	MTYPE	TTYPE	TTAGBITS	ISIZE	TLBENT
*	0	*	*	*	*	*
r	r	r	r	r	r	r

31:24 Translation Mask (TMASK) - The incoming IO address bits IOADDR[31:24] must match this field, depending on the setting of the ITR field in the core's Control register, for an address translation operation to be performed.

23:20 RESERVED

19:18 IOMMU Type (MTYPE) - Shows IOMMU implementation type. This field is always 0, other values are reserved for future versions of the core. If this field is non-zero, it should trigger a software alert as future versions of the core may not be backward compatible.

17:16 TLB Type (TTYPE) - Show implementation of Translation Lookaside Buffer. This field is always 0, other values are reserved for future versions of the core. If this field is non-zero, it should trigger a software alert as future versions of the core may not be backward compatible.

15:8 TLB Tag bits (TTAGBITS) - The width in bits of the TLB tag.

7:5 IOMMU Access size (ISIZE) - This field indicates the AMBA access size used when accessing page tables in main memory. This is also the line size for the TLB (if enabled). The values are:
000: 32-bit (4 byte)
001: 64-bit (8 byte)
010: 128-bit (16 byte)
011: 256-bit (32-byte)

4:0 TLB entries (TLBENT) - Number of entries in the TLB. The number of entries is 2^{TLBENT}.

Reset value: implementation dependent

51.10.4 Control Register

*Table 715.*0x10 - CTRL - Control register

31 21	20 18	17	16	15 12	11	10	9 8	7	6	5	4	3	2 1	0
RESERVED	PGSZ	LB	SP	ITR	DP	SIV	HPROT	AU	WP	DM	GS	CE	PM	EN
0	0	0	0	0	0	0	0	0	0	0	0	0	*	0
r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

31:21 RESERVED

20:18 Page Size (PGSZ) - The value in this field determines the page size mapped by page table entries and bit vector positions. Valid values are:

000: 4 KiB
001: 8 KiB
010: 16 KiB
011: 32 KiB
100: 64 KiB
101: 128 KiB
110: 256 KiB
111: 512 KiB

This field is only writable if the CS field in Capability register 0 is non-zero.

17 Lookup bus (LB) - The value of this bit controls AHB master interface to use for fetching bit vector and/or page table entries from memory when the core has been implemented with support for multiple buses (multiple AHB master interfaces). If this field is '0', the first master interface will be used for vector/table lookups. If this field is '1', the second master interface will be used for lookups.

This field is only writable if the MB field in Capability register 0 is non-zero.

*Table 715.*0x10 - CTRL - Control register

16	SPLIT support (SP) - The value of this bit controls if the core can issue AMBA SPLIT responses to masters on the IO bus. If this bit is '1' the core will use AMBA SPLIT responses. If this bit is '0', the core will insert waitstates and not issue AMBA SPLIT responses. This bit is read-only if the core has been implemented with support for only one response mode. If this bit is writable, software must make sure that the IO bus is free and that the core is not handling any ongoing accesses before changing the value of this bit. The core performs rudimentary checks in order to determine if the slave side is idle before changing SPLIT behavior. Therefore AMBA SPLIT responses may not be disabled or enabled immediately after this bit is written.
15:12	IOMMU Translation Range (ITR) - This field defines the size of the address range translated by the core's IOMMU functionality. The size of the decoded address range is 16 MiB * 2^{ITR} and the decoded memory area is located on an address with the most significant bits specified by the TMASK field in Capability register 2, unless ITR = 8 in which case the whole address space is covered by the translated range.
11	Disable Prefetch (DP) - When this bit is '1' the core will not perform any prefetch operations. This bit is read only if the core has been implemented without support for prefetching data. During normal operation prefetch of data improves performance and should be enabled (the value of this bit should be '0'). Prefetching may need to be disabled in scenarios where IOMMU protection is enabled, which leads to a prefetch operation on every incoming burst access, and when the core is used in bi-directional bridge configurations where dead locks may be resolved by the core dropping prefetch data.
10	Save Invalid IOPTE (SIV) - If this field is '1' the core will save IOPTEs that have their valid (V) bit set to '0' if the core has been implemented with a TLB. If this field is '0' the core will not buffer an IOPTE with valid (V) set to '0' and perform an page table lookup every time the page covered by the IOPTE is accessed. If the value of this field is changed, a TLB flush must be made to remove any existing IOPTEs from the core's internal buffer. Also if this field is set to '0', any diagnostic accesses to the TLB should not set the IOPTE valid bit to '0' unless the Tag valid bit is also set to '0'. This field is only accessible if the core has support for IOMMU protection and is implemented with a Translation Lookaside Buffer (TLB).

*Table 715.*0x10 - CTRL - Control register

9:8	HPROT encoding (HPROT) - The value of this field will be assigned to the AMBA AHB HPROT signal bits 3:2 when the core is fetching protection data from main memory. HPROT(3) signals if the access is cacheable and HPROT(2) signals if the access is bufferable. This field is only used when the core has been implemented with support for Access Protection Vector or IOMMU functionality.
7	Always Update (AU) - If this bit is set to '0' the AHB failing access register will only be updated if the Access Denied (AD) bit in the Status register is '0' when the access is denied. Otherwise the AHB failing access register will be updated each time an access is denied, regardless of the Access Denied (AD) bit's value.
6	Write Protection only (WP) - If this bit is set to '1' the core will only used the Access Protection Vector to protect against write accesses. Read accesses will be propagated over the core without any access restriction checks. This will improve the latency for read operations. This field has no effect when the core is using IOMMU protection (PM field = "01"). When using IOMMU protection all accesses to the range determined by TMASK and ITR will be checked against the page table, unless the access is from a master that is assigned to an inactive group or a group in pass-through mode.
5	Diagnostic Mode (DM) - If this bit is set to '1' the core's internal buffers can be accessed via the Diagnostic interface (see Diagnostic cache access register) when the DE field of the Status register has been set by the core. Set this bit to '0' to leave Diagnostic mode. While in this mode the core will not forward any incoming AMBA accesses.
4	Group-Set-addressing (GS) - When this bit is set to '1', the core will use the group number as part of the Access Protection Vector cache set address. This bit can only be set if fields A and CA, or I and IA, of Capability register 0 are non-zero.
3	Cache/TLB Enable (CE) - When this bit is set to '1', the core's internal cache/TLB is enabled. Note that the core can be implemented without internal cache/TLB. Capability register 0, fields AC and IT show if the core has internal cache.
2:1	Protection Mode (PM) - This value selects the protection mode to use. "00" selects Group Mode and/or Access Protection Vector mode (if available). "01" selects IOMMU mode. This field is read only if the core only has support for one mode setting.
0	Enable (EN) - Core enable. If this bit is set to 1 the core is enabled. If this bit is set to 0 the core is disabled and in pass-through mode. After writing this bit software should read back the value. The change has not taken effect before the value of this bit has changed. The bit transition may be blocked if the core is in diagnostic access mode or otherwise occupied.

51.10.5 TLB/cache Flush Register

*Table 716.*0x14 - FLUSH - TLB/cache flush register

31 8	7 4	3 2	1	0
RESERVED	FGRP	RES	GF	F
0	0	0	0	0
r	rw	r	rw	rw

31:1 RESERVED

7:4 Flush Group (FGRP) - This field specifies the group to be used for a Group Flush, see GF field below.

3:2 RESERVED

1 Group Flush (GF) - When this bit is written to '1' the cache entries for the group selected by the FGRP field will be flushed. More precisely the core will use the FGRP field as (part of the) set address when performing the flush. This flush option is only available if the core has support for group set addressing (CA field of Capability register 1 is non-zero). This flush option must only be used if the GS bit in the Control register is set to '1', otherwise old data may still be marked as valid in the Access Protection Vector cache or IOMMU TLB. This bit will be reset to '0' when a flush operation has completed. A flush operation also affects the FL and FC fields in the Status register.

0 Flush (F) - When this bit is written to '1' the core's internal cache will be flushed. This bit will be reset to '0' when a flush operation has completed. A flush operation also affects the FL and FC fields in the Status register.

51.10.6 Status Register

*Table 717.*0x18 - STAT - Status register

31 6	5	4	3	2	1	0
RESERVED	PE	DE	FC	FL	AD	TE
0	0	0	0	0	0	0
r	uc	uc	uc	uc	uc	uc

31:6 RESERVED

5 Parity Error (PE) - The core sets this bit to '1' when it detects a parity error in the tag or data RAM of the APV cache. This field is cleared by writing '1' to this position, writes of '0' have no effect.

4 Diagnostic Mode Enabled (DE) - If this bit is set to '1' the core is in Diagnostic Mode where the core's internal buffers can be accessed via the Diagnostic access registers. While in this mode the core will not forward any incoming AMBA accesses.

3 Flush Completed (FC) - The core sets this bit to '1' when a flush operation completes. This field is cleared by writing '1' to this position, writes of '0' have no effect.

2 Flush started (FL) - The core sets this bit to '1' when a Flush operation has started. This field is cleared by writing '1' to this position, writes of '0' have no effect.

1 Access Denied (AD) - The core denied an AMBA access. This field is cleared by writing '1' to this position, writes of '0' have no effect.

0 Translation Error (TE) - The core received an AMBA ERROR response while accessing the bit vector or page tables in memory. This also leads to the incoming AMBA access being inhibited. Depending on the status of the Control register's AU field and this register's AD field this may also lead to an update of the AHB Failing Access register.

51.10.7 Interrupt Mask Register

*Table 718.*0x1C - IMASK - Interrupt mask register

31 6	5	4	3	2	1	0
RESERVED	PEI	R	FCI	FLI	ADI	TEI
0	0	0	0	0	0	0
r	rw	rw	rw	rw	rw	rw

31:6 RESERVED

5 Parity Error Interrupt (PEI) - If this bit is set to '1' an interrupt will be generated when the PE bit in the Status register transitions from '0' to '1'.

4 RESERVED

3 Flush Completed Interrupt (FCI) - If this bit is set to '1' an interrupt will be generated when the FC bit in the Status register transitions from '0' to '1'.

2 Flush Started Interrupt (FLI) - If this bit is set to '1' an interrupt will be generated when the FL bit in the Status register transitions from '0' to '1'..

1 Access Denied Interrupt (ADI) - If this bit is set to '1' an interrupt will be generated when the AD bit in the Status register transitions from '0' to '1'.

0 Translation Error Interrupt (TEI) - If this bit is set to '1' an interrupt will be generated when the TE bit in the Status register transitions from '0' to '1'.

Reset value: 0x00000000

51.10.8 Failing Access Register

*Table 719.*0x20 - AHBFAS - failing access register

31 5	4	3 0
FADDR[31:5]	FW	FMASTER
0	0	0
r	r	r

31:5 Failing Address (FADDR[31:5]) - Bits 31:5 of IO address in access that was inhibited by the core. This field is updated depending on the value of the Control register AU field and the Status register AD field.

4 Failing Write (FW) - If this bit is set to '1' the failed access was a write access, otherwise the failed access was a read access. This field is updated depending on the value of the Control register AU field and the Status register AD field.

3:0 Failing Master (FMASTER) - Index of the master that initiated the failed access. This field is updated depending on the value of the Control register AU field and the Status register AD field.

Reset value: 0x00000000

51.10.9 Master Configuration Register(s)

*Table 720.*0x40-0x7C - MSTLFGO-15 - Master configuration register(s)

31 24	23 12	11 5	4	3 0
VENDOR	DEVICE	RESERVED	BS	GROUP
*	*	0	0	0
r	r	r	rw	rw

31: 24 Vendor ID (VENDOR) - GRLIB Plug'n'play Vendor ID of master

23: 12 Device ID (DEVICE) - GRLIB Plug'n'play Device ID of master

11: 5 RESERVED

*Table 720.*0x40-0x7C - MSTLFGO-15 - Master configuration register(s)

4	Bus select for master (BS) - Master n's bus select register is located at register address offset 0x40 + n*0x4. This field specifies the the bus to use for accesses initiated by AHB master n. This field is only available if the MB field in Capability register 0 is non-zero. Bus selection is active even if the core control register enable bit is zero.
3:0	Group assignment for master - Master n's group assignment field is located at register address offset 0x40 + n*0x4. This field specifies the group to which a master is assigned.

51.10.10 Group Control Register(s)

*Table 721.*0x80-0xAC - GRPCTRCO-15 - Group control register(s)

31	1	0
BASE[31:2+SIZE]	P	AG
0	0	0
rw	rw	rw

31: 2 Base address (BASE) - Group n's control register is located at offset 0x80 + n*0x4. This field contains the base address of the data structure for the group.

The number of bits writeable in the data structure base address depends on the access size used to fetch entries in the Access Protection Vector and/or the IOMMU page table. The access size is given in the ISIZE and CSIZE Capability register fields.

This field is only writable if the core has been implemented with support for Access Protection Vector and/or IOMMU functionality.

1 Pass-through (P) - If this bit is set to '1' and the group is active (see bit 0 below) the core will pass-through all accesses made by master in this group and not use the address specified by BASE to perform look-ups in main memory. Note that this also means that the access will pass through untranslated when the core is using IOMMU protection (even if the access is outside the translated range defined by TMASK in Capability register 2).

If this bit is set to '0', the core will use the contents in its cache, or in main memory, to perform checks and possibly address translation on incoming accesses.

If the core has been implemented without support for Access Protection Vector and IOMMU, this field is disabled.

0 Active Group (AG) - Indicates if the group is active. If this bit is set to '0', all accesses made by masters assigned to this group will be blocked.

If the core has been implemented without support for Access Protection Vector and IOMMU, accesses will be propagated if this bit is set to '1'. If the core has been implemented with support for Access Protection Vector and/or IOMMU the core will check the P field of this register and possibly also the in-memory data structure before allowing or blocking the access.

51.10.11 Diagnostic Cache Access Register

*Table 722.*0xC0 - DIAGCTRL - Diagnostic cache access register

31	30	29 22	21	20	19	18 0
DA	RW	RESERVED	DP	TP	R	SETADDR
0	0	0	0	0	0	NR
rw	rw	r	rw	rw	r	rw*

31 Diagnostic Access (DA) - When this bit is set to '1' the core will perform a diagnostic operation to the cache address specified by the SETADDR field. When the operation has finished this bit will be reset to '0'.

30 Read/Write (RW) - If this bit is '1' and the A field is set to '1' the core will perform a read operation to the cache. The result will be available in the Diagnostic cache access tag and data register(s). If this bit is set to '0' and the A field is set to '1', the core will write the contents of the Diagnostic cache access tag and data registers to the internal cache.

29:22 RESERVED

21 Data Parity error (DP) - This bit is set to '1' if a parity error has been detected in the word read from the cache's data RAM. This bit can be set even if no diagnostic cache access has been made and it can also be set after a cache write operation. This bit is read-only.

20 Tag Parity error (TP) - This bit is set to '1' if a parity error has been detected in the word read from the cache's tag RAM. This bit can be set even if no diagnostic cache access has been made and it can also be set after a cache write operation. This bit is read-only.

19 RESERVED

*Table 722.*0xC0 - DIAGCTRL - Diagnostic cache access register

18:0	Cache Set Address (SETADDR) - Set address to use for diagnostic cache access. When a read operation has been performed, this field should not be changed until all wanted data has been read from the Diagnostic cache access data and tag registers. Changing this field invalidates the contents of the data and tag registers.

* This register can only be accessed if the core has an internal cache and the DE bit in the Status register is set

51.10.12 Diagnostic Cache Access Data Register 0 - 7

*Table 723.*0xC4-0xE0 - DIAG0 - Diagnostic cache access data register 0 - 7

31	0
CDATAn	
NR	
rw*	

31:0 Cache data word n (CDATAn) - The core has 8 Diagnostic cache access data registers. Diagnostic cache access data register n holds data bits [31+32*n:32*n] in the cache line.

* This register can only be accessed if the core has an internal cache and the DE bit in the Status register is set
Reset value: Undefined

51.10.13 Diagnostic Cache Access Tag Register

*Table 724.*0xE4 - DIAG 7 - Diagnostic cache access tag register

31	0
TAG	V
NR	
rw*	

31:1 Cache tag (TAG) - The size of the tag depends on cache size. The contents of the tag depends on cache size and addressing settings.

0 Valid (V) - Valid bit of tag

* This register can only be accessed if the core has an internal cache and the DE bit in the Status register is set
Reset value: Undefined

51.10.14 Data RAM Error Injection Register

*Table 725.*0xE8 - DERRI - Data RAM error injection register

31	0
DPERRINJ	
0	
rw	

31:0 Data RAM Parity Error Injection (DPERRINJ) - Bit DPERRINJ[n] in this register is XOR:ed with the parity bit for data bits [*7+8*n:8*n*] in the data RAM.

* This register can only be accessed if the core has an internal cache and the FT field in Capability register 0 is non-zero
Reset value: 0x00000000

51.10.15 Tag RAM Error Injection Register

*Table 726.*0xEC - TERRI - Tag RAM error injection register

31	0
TPERRINJ	
0	
rw	

0 Tag RAM Parity Error Injection (TPERRINJ) - Bit TPERRINJ[n] in this register is XOR:ed with the parity bit for tag bits [*7+8*n:8*n*] in the tag RAM.

* This register can only be accessed if the core has an internal cache and the FT field in Capability register 0 is non-zero
Reset value: 0x00000000

51.10.16 ASMP Access Control Register

*Table 727.*0x100-0x10C - ASMPCTRL - ASMP access control register(s)

31 19	18	17	16	15 0
RESERVED	FC	SC	MC	GRPACCSZCTRL
0	0	0	0	0
r	rw	rw	rw	rw

31: 19	RESERVED
18	Flush register access control (FC) - If this bit is set to '1' in the ASMP control register at offset 0x100 + n*0x4 then the TLB/cache flush register in ASMP register block n is writable. Otherwise writes to the TLB/cache flush register in ASMP register block n will be inhibited.
17	Status register access control (SC) - If this bit is set to '1' in the ASMP control register at offset 0x100 + n*0x4 then the Status register in ASMP register block n is writable. Otherwise writes to the Status register in ASMP register block n will be inhibited.
16	Mask register access control (MC) - If this bit is set to '1' in the ASMP control register at offset 0x100 + n*0x4 then the Master register in ASMP register block n is writable. Otherwise writes to the Mask register in ASMP register block n will be inhibited.
15:0	Group control register access control (GRPACCSZCTRL) - ASMP register block n's group access control field is located at register address offset 0x100 + n*0x4. This field specifies which of the Group control registers that are writable from an ASMP register block. If GRPACCSZCTRL[i] in the ASMP access control register at offset 0x100 + n*0x4 is set to '1' then Group control register i is writable from ASMP register block n.

Reset value: 0x00000000

51.11 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x04F. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

If implemented, the core's second AHB master interface has 0x01 (Cobham Gaisler) and device identifier 0x010.

51.12 Implementation

51.12.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support *grlib_async_reset_enable*. All registers that react on the reset signal will have a synchronous reset.

51.12.2 Technology mapping

The core has two technology mapping generics *memtech* and fcfsmtech. *memtech* selects which memory technology that will be used to implement the FIFO memories. *fcfsmtech* selects the memory technology to be used to implement the First-come, first-served buffer, if FCFS is enaled.

51.12.3 RAM usage

The core instantiates one or several *syncram_2p* blocks from the technology mapping library (TECHMAP). If prefetching is enabled max(*mstmaccsz*, *slvaccsz*)/32 *syncram_2p* block(s) with organization (max*(rburst,iburst*)-max(*mstmaccsz*, *slvaccsz*)/32) x 32 is used to implement read FIFO (max*(rburst,iburst*) is the size of the read FIFO in 32-bit words). max(*mstmaccsz*, *slvaccsz*)/32 *syn-*

cram_2p block(s) with organization *(wburst* - max(*mstmaccsz*, *slvaccsz*)/32) x 32, is always used to implement the write FIFO (where *wburst* is the size of the write FIFO in 32-bit words).

If the core has support for first-come, first-served ordering then one *fcfs* x 4 *syncram_2p* block will be instantiated, using the technology specified by the VHDL generic *fcfsmtech*.

If the core has an Access Protection Vector cache and/or IOMMU TLB, the cache/TLB will be implemented using one *syncramft* block for the tag RAM and one *syncramft* block for the data RAM.

51.13 Configuration options

Table 728 shows the configuration options of the core (VHDL generics).

*Table 728.*Configuration options (VHDL generics)

Generic	Function	Allowed range	Default
memtech	Memory technology		
iohsindex	Slave I/F AHB index on IO bus	0 to NAHBMST-1	0
syshmindex	Master I/F AHB index on System bus	0 to NAHBMST-1	0
syshmindex2	Master I/F AHB index for second AHB interface. Only available if the entity griommu_mb is instantiated.	0 to NAHBMST-1	0
syshsindex	Index for register slave AHB I/F connected to same bus as core Master I/F	0 to NAHBMST-1	0
syshmaddr	ADDR field of AHB slave BAR 0 on system bus	0 - 16#FFF#	0
syshmask	MASK field of AHB slave BAR 0 on system bus. The requied value of this generic depends on the setting of generic narb (see below).	0 - 16#FFF#	16#FFF#
syshirq	Interrupt line to use for IOMMU interrupts	1 - NAHBIRQ-1	1
dir	0 - clock frequency on the master bus is lower than or equal to the frequency on the slave bus 1 - clock frequency on the master bus is higher than or equal to the frequency on the slave bus (for VHDL generic *ffact* = 1 the value of dir does not matter)	0 - 1	0
ffact	Frequency scaling factor between AHB clocks on master and slave buses.	1 - 15	2
slv	Slave bridge. Used in bi-directional bridge configuration where *slv* is set to 0 for master bridge and 1 for slave bridge. When a deadlock condition is detected slave bridge (*slv*=1) will give RETRY response to current access, effectively resolving the deadlock situation. This generic must only be set to 1 for a bridge where the frequency of the bus connecting the master interface is higher or equal to the frequency of the AHB bus connecting to the bridge's slave interface. Otherwise a race condition during access collisions may cause the bridge to deadlock.	0 - 1	0
pfen	Prefetch enable. Enables read FIFO.	0 - 1	0
irqsync	Interrupt forwarding. Forward interrupts from slave interface to master interface and vice versa. 0 - no interrupt forwarding, 1 - forward interrupts 1 - 15, 2 - forward interrupts 0 - 31. Since interrupts are forwarded in both directions, interrupt forwarding should be enabled for one bridge only in a bi-directional AHB/AHB bridge.	0 - 2	0

*Table 728.*Configuration options (VHDL generics)

Generic	Function	Allowed range	Default
wburst	Length of write bursts in 32-bit words. Determines write FIFO size and write burst address boundary. If the wburst generic is set to 2 the bridge will not perform write bursts over a 2x4=8 byte boundary. This generic must be set so that the buffer can contain two of the maximum sized accesses that the bridge can handle.	2 - 32	8
iburst	Instruction fetch burst length. This value is only used if the generic *ibrsten* is set to 1. Determines the length of prefetching instruction read bursts on the master side. The maximum of (iburst,rburst) determines the size of the core's read buffer FIFO.	4 - 8	8
rburst	Incremental read burst length. Determines the maximum length of incremental read burst of unspecified length (INCR) on the master interface. The maximum of *rburst* and *iburst* determine the read burst boundary. As an example, if the maximum value of these generics is 8 the bridge will not perform read bursts over a 8x4=32 byte boundary. This generic must be set so that the buffer can contain two of the maximum sized accesses that the bridge can handle. For systems where AHB masters perform fixed length burst (INCRx , WRAPx) *rburst* should not be less than the length of the longest fixed length burst.	4 - 32	8
bar0	Address area 0 decoded by the bridge's slave interface. Appears as memory address register (BAR0) on the slave interface. The generic has the same bit layout as bank address registers with bits [19:18] suppressed (use functions ahb2ahb_membar and ahb2ahb_iobar in gaisler.misc package to generate this generic).	0 - 1073741823	0
bar1	Address area 1 (BAR1)	0 - 1073741823	0
bar2	Address area 2 (BAR2)	0 - 1073741823	0
bar3	Address area 3 (BAR2)	0 - 1073741823	0
sbus	The number of the AHB bus to which the slave interface is connected. The value appears in bits [1:0] of the user-defined register 0 in the slave interface configuration record and master configuration record.	0-3	0
mbus	The number of the AHB bus to which the master interface is connected. The value appears in bits [3:2] of the user-defined register 0 in the slave interface configuration record and master configuration record.	0-3	0
ioarea	Address of the I/O area containing the configuration area for AHB bus connected to the bridge's master interface. This address appears in the bridge's slave interface user-defined register 1. In order for a master on the slave interface's bus to access the configuration area on the bus connected to the bridge's master interface, the I/O area must be mapped on one of the bridge's BARs. If this generic is set to 0, some tools, such as Cobham Gaisler's GRMON debug monitor, will not perform Plug'n'Play scanning over the bridge.	0 - 16#FFF#	0
ibrsten	Instruction fetch burst enable. If set, the bridge will perform bursts of *iburst* length for opcode access (HPROT[0] = '0'), otherwise bursts of *rburst* length will be used for both data and opcode accesses.	0 - 1	0

*Table 728.*Configuration options (VHDL generics)

Generic	Function	Allowed range	Default
lckdac	Locked access error detection and correction. Locked accesses may lead to deadlock if a locked access is made while an ongoing read access has received a SPLIT response. The value of *lckdac* determines how the core handles this scenario: 0: Core will deadlock 1: Core will issue an AMBA ERROR response to the locked access 2: Core will allow both accesses to complete. If the core is used to create a bidirectional bridge, a deadlock condition may arise when locked accesses are made simultaneously in both directions. With *lckdac* set to 0 the core will deadlock. With *lckdac* set to a non-zero value the slave bridge will issue an ERROR response to the incoming locked access.	0 - 2	0
slvmaccsz	The maximum size of accesses that will be made to the bridge's slave interface. This value must equal *mstmaccsz* unless *rdcomb* /= 0 and *wrcomb* /= 0.	32 - 256	32
mstmaccsz	The maximum size of accesses that will be performed by the bridge's master interface. This value must equal *mstmaccsz* unless *rdcomb* /= 0 and *wrcomb* /= 0.	32 - 256	32
rdcomb	Read combining. If this generic is set to a non-zero value the core will use the master interface's maximum AHB access size when prefetching data and allow data to be read out using any other access size supported by the slave interface. If slvmaccsz > 32 and mstmaccsz > 32 and an incoming single access, or access to a non-prefetchable area, is larger than the size supported by the master interface the bridge will perform a series of small accesses in order to fetch all the data. If this generic is set to 2 the core will use a burst of small fetches. If this generic is set to 1 the bridge will not use a burst unless the incoming access was a burst. Read combining is only supported for single accesses and incremental bursts of unspecified length.	0 - 2	0
wrcomb	Write combining. If this generic is set to a non-zero value the core may assemble several small write accesses (that are part of a burst) into one or more larger accesses or assemble one or more accesses into several smaller accesses. The settings are as follows: 0: No write combining 1: Combine if burst can be preserved 2: Combine if burst can be preserved and allow single accesses to be converted to bursts (only applicable if slvmaccsz > 32) Only supported for single accesses and incremental bursts of unspecified length	0 - 2	0

*Table 728.*Configuration options (VHDL generics)

Generic	Function	Allowed range	Default
combmask	Read/write combining mask. This generic determines which ranges that the core can perform read/write combining to (only available when rdcomb respectively wrcomb are non-zero). The value given for combmask is treated as a 16-bit vector with LSB bit (right-most) indicating address 0x0 - 0x10000000. Making an access to an address in an area marked as '0' in combmask is equivalent to making an access over a bridge with rdcomb = 0 and wrcomb = 0. However, combmask is not taken into account when the core performs a prefetch operation (see pfen generic). When a prefetch operation is initiated, the core will always use the maximum supported access size (when rdcomb /= 0).	0 - 16#FFFF#	16#FFFF#
allbrst	Support all burst types 2: Support all types of burst and always prefetch for wrapping and fixed length bursts. 1: Support all types of bursts 0: Only support incremental bursts of unspecified length See section 51.2.7 for more information. When allbrst is enabled, the core's read buffer (size set via rburst/iburst generics) must have at least 16 slots.	0 - 2	0
ifctrlen	Interface control enable. When this generic is set to 1 the input signals *ifctrl.mstifen* and *ifctrl.slvifen* can be used to force the AMBA slave respectively master interface into an idle state. This functionality is intended to be used when the clock of one interface has been gated-off and any stimuli on one side of the bridge should not be propagated to the interface on the other side of the bridge. When this generic is set to 0, the ifctrl.* input signals are unused.	0 - 1	0
fcfs	First-come, first-served operation. When this generic is set to a non-zero value, the core will keep track of the order of incoming accesses and handle the requests in the same order. If this generic is set to zero the bridge will not preserve the order and leave this up to bus arbitration. If FCFS is enabled the value of this generic must be higher or equal to the number of masters that may perform accesses over the bridge.	0 - NAHBMST	0
fcfsmtech	Memory technology to use for FCFS buffer. When VHDL generic *fcfs* is set to a non-zero value, the core will instantiate a 4 bit x *fcfs* buffer to keep track of the incoming master indexes. This generic decides the memory technology to use for the buffer.	0 - NTECH	0 (inferred)
scantest	Enable scan support	0 - 1	0
split	Use AMBA SPLIT responses. When this generic is set to 1 the core will issue AMBA SPLIT responses. When this generic is set to 0 the core will insert waitstates instead and may also issue AMBA RETRY responses. If this generic is set to 0, the *fcfs* generic must also be set to 0, otherwise a simulation failure will be asserted.	0 - 1	1
dynsplit	Dynamic SPLIT responses. If this generic is non-zero the Control register field SP will be writable. This allows software to control if the core should use AMBA SPLIT responses or waitstates on the IO bus. The VHDL generic *split* must be set to 1 if this generic is set to 1.	0 - 1	0

*Table 728.*Configuration options (VHDL generics)

Generic	Function	Allowed range	Default
nummst	Number of masters connected to the bus that the core's slave interface connects to.	1 - NAHBMST-1	1
numgrp	Number of groups	1 - NAHBMST-1	1
stat	Enable statistics outputs	0 - 1	0
apv	Include support for Access Protection Vector (APV). Setting this generic to 1 includes support.	0 - 1	1
apvc_en	Access Protection Vector cache. 0: disabled, 1: enabled.	0 - 1	0
apvc_ways	Number of ways in Access Protection Vector cache	1 - 1	1
apvc_lines	Number of lines in each way of the Access Protection vector cache. The total size of the data cache in bytes will be apvc_ways * tbw_accsz/8 * apvc_lines. This value must be a power of two. If the core is implemented with an IOMMU TLB, the maximum value of this generic and VHDL generic *tlb_num* determines the number of lines in the cache.		16
apvc_tech	Access Protection Vector cache memory technology. This generic decides the technology setting for the cache's tag and data RAM.	0 - NTECH	0 (inferred)
apvc_gseta	Allow use of group ID as part of cache set address. This allows cache addressing scheme 2 to be used. The value 0 disables the use of group ID as part of the cache set address and 1 enables the functionality. If the core is implemented with an IOMMU TLB and VHDL generic *tlb_gseta* is set to non-zero value, this will also enable *apvc_gseta*. This generic may only be set to a non-zero value if VHDL generic *numgrp* > 1.	0 - 1	0
apvc_caddr	If generic *apvc_cmask* is non-zero this generic specifies the base address of the memory area that the core will cache protection information for.The area is specified in the same way as addresses for AHB slaves. To cache protection information for the block 0x40000000 - 0x7FFFFFFF, set this generic to 0x400 and *apvc_cmask* to 0xC00.	0 - 16#FFF#	0
apvc_cmask	Specifies size of memory block for which protection information will be cached by the core. If this generic is zero the core will cache protection information for the full AMBA address range. If this generic is 0x800 the core will cache information for half the AMBA address range, the base address for the cacheable area is specified by *apvc_caddr*.	0 - 16#FFF#	0
apvc_pipe	Insert pipelining registers on APV cache. The master -> group -> cache path may become critical in a design. If there are timing problem on the tag or cache RAM address inputs, set this generic to 1 and suffer one cycle in additional penalty on cache accesses. If the core is implemented with an IOMMU TLB and VHDL generic *tlb_pipe* is set to non-zero value, this will also enable *apvc_pipe*.	0 - 1	0
iommu	Enable IOMMU functionality	0 - 1	0
iommutype	Selects type of IOMMU functionality. Set to 0	0 - 1	0

*Table 728.*Configuration options (VHDL generics)

Generic	Function	Allowed range	Default
tlb_num	Number of entries in the IOMMU translation lookaside buffer (TLB). A value of zero here implements the core without a TLB. The width of an entry is determined through the VHDL generic tbw_accsz. The total size of the TLB in bytes will be tbw_accsz/8 * tlb_num. This value must be a power of two. If the core has been implemented with an APV cache, the maximum value of this generic and VHDL generic *apvc_lines* determines the number of entries in the TLB.	0 - 64	0
tlb_type	Selects TLB implementation. Set to 0.	0 - 1	0
tlb_tech	TLB memory technology. This generic decides the technology setting to use for implementing the TLB. In the current version of the bridge this generic and VHDL generic *apvc_tech* must have the same value.	0 - NTECH	0 (inferred)
tlb_gseta	Allow use of group ID as part of TLB set address. This allows cache addressing scheme 2 to be used. The value 0 disables the use of group ID as part of the TLB set address and 1 enables the functionality. If the core is implemented with an APV cache and VHDL generic *apvc_gseta* is set to non-zero value, this will also enable *tlb_gseta*. This generic may only be set to a non-zero value if VHDL generic *numgrp* > 1.	0 - 1	0
tlb_pipe	Insert pipelining registers on TLB address. The master -> group -> TLB path may become critical in a design. If there are timing problem on the tag or cache RAM address inputs, set this generic to 1 and suffer one cycle in additional penalty on cache accesses. If the core is implemented with an APV cache and VHDL generic *apvc_pipe* is set to non-zero value, this will also enable *tlb_pipe*.	0 - 1	0
tmask	Translation mask. Specifies the value that the most significant bits of the IO address must have for an address to be translated. Bits 7:0 of this value specified TMASK[31:24]. The default value 0xff is recommended. However, this may not work well if the IO bus has a GRLIB plug'n'play area. Note that tmask must specify an address range that is covered by one of the core's memory bars. Otherwise the core will not be selected by the AHB bus controller when the tmask area is accessed.	0 - 16#ff#	16#ff#
tbw_accsz	AMBA access size to use when fetching entries of the Access Protection Vector and/or the IOMMU page table. This value also sets the Access Protection Vector cache line size and the TLB entry size. This value must not exceed the maximum access size for the AHB master interface.	32 - *mstmaccsz*	32
dpagesz	Support for dynamic page size. If this generic is set to 1 the core will support selecting the page size via the Control register. If this generic is set to 0, the page size is fixed to 4 KiB.	0 - 1	0
ft	Fault tolerance. This setting determines if the APV cache and/or TLB tag and data RAMs should be protected against faults. Possible values are: 0 - disabled, 1 - byte parity	0 - 1	0

*Table 728.*Configuration options (VHDL generics)

Generic	Function	Allowed range	Default
narb	Number of ASMP register blocks. The core will be implemented with narb ASMP register blocks. the required syshmask settings for different narb values are: narb 0 : hmask 0xfff, narb 1 : hmask 0xfe, narb 2 -3 : hmask 0xfc, narb 4-7 : hmask 0xf80, narb 8 - 15 : hmask 0xf00		
multiirq	Enable interrupt propagation for second AHB master interface. This generic is only available if the the entity griommu_mb is instantiated. If this generic is set to '1', interrupt propagation, as configured via the irqsync generic, will also be done for the second AHB master interface.	0 - 1	0

51.14 Signal descriptions

Table 729 shows the interface signals of the core (VHDL ports).

*Table 729.*Signal descriptions (VHDL ports)

Signal name	Field	Type	Function	Active
RST		Input	Reset	Low
HCLKSYS		Input	AHB system bus clock	-
HCLKIO		Input	AHB IO bus clock	-
IO_AHBSI	*	Input	AHB slave input signals	-
IO_AHBSO	*	Output	AHB slave output signals	-
IO_AHBPNP	*	Input	AHB master output vector signals (on io/slave i/f side). Used to decode plug'n'play vendor/device ID of masters so that these values can be visible in the Master control register(s).	-
SYS_AHBMI	*	Input	AHB master input signals	-
SYS_AHBMO	*	Output	AHB master output signals	-
SYS_AHBPNP	*	Input	AHB slave input vector signals (on system/master i/f side). Used to decode cachability and prefetchability Plug&Play information on bus connected to the bridge's master interface.	-
SYS_AHBMI2	*	Input	AHB master input signals, second interface. Only available on griommu_mb entity.	-
SYS_AHBMO2	*	Output	AHB master output signals, second interface. Only available on griommu_mb entity.	-
SYS_AHBPNP2	*	Input	AHB slave input vector signals (on system/master i/f side). Used to decode cachability and prefetchability Plug&Play information on bus connected to the bridge's second master interface. Only available on griommu_mb entity.	-
SYS_AHBSI	*	Input	AHB slave input signals	-
SYS_AHBSO	*	Output	AHB slave output signals	-
WLK_AHBMI	*	Input	AHB master input signals	-
WLK_AHBMO	*	Output	AHB master output signals	-
LCKI	slck blck mlck	Input	Used in systems with multiple AHB/AHB bridges (e.g. bi-directional AHB/AHB bridge) to detect deadlock conditions. Tie to "000" in systems with only uni-directional AHB/AHB bus.	High
LCKO	slck blck mlck	Output	Indicates possible deadlock condition	High
STATO (clocked by HCLKSYS)	hit	Output	High for one cycle during TLB/cache hit.	High
	miss	Output	High for one cycle during TLB/cache miss	High
	pass	Output	High for one cycle during passthrough access	High
	accok	Output	High for one cycle during access allowed	High
	accerr	Output	High for one cycle during access OK	High
	walk	Output	High while core is busy performing a table walk or accessing the access protection vector	High
	lookup	Output	High while core is performing cache lookup/ table walk	High
	perr	Output	High for one cycle when core detects a parity error in the APV cache	High

*Table 729.*Signal descriptions (VHDL ports)

Signal name	Field	Type	Function	Active
IFCTRL	mstifen	Input	Enable master interface. This input signal is unused if the VHDL generic *ifctrlen* is 0. If VHDL generic *ifctrlen* is 1 this signal must be set to '1' in order to enable the core's AMBA master interface, otherwise the master interface will always be idle and will not respond to stimuli on the core's AMBA slave interface.	High
	slvifen	Input	Enable slave interface. This input signal is unused if the VHDL generic *ifctrlen* is 0. If VHDL generic *ifctrlen* is 1 this signal must be set to '1' in order to enable the core's AMBA slave interface, otherwise the interface will always be ready and the bridge will not propagate stimuli on the core's AMBA slave interface to the core's AMBA master interface.	High

* see GRLIB IP Library User's Manual

51.15 Library dependencies

Table 730 shows the libraries used when instantiating the core (VHDL libraries).

*Table 730.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	MISC	Component	Component declaration

51.16 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.iommu.all;

entity griommu_ex is
  port (
    clk : in std_ulogic;
    rstn : in std_ulogic;

    ...  -- other signals
    );
end;

architecture rtl of griommu_ex is

  -- AMBA signals, system bus
  signal proc_ahbsi       : ahb_slv_in_type;
  signal proc_ahbso       : ahb_slv_out_vector;
  signal proc_ahbmi       : ahb_mst_in_type;
  signal proc_ahbmo       : ahb_mst_out_vector;

  -- AMBA signals, IO bus
  signal io_ahbsi         : ahb_slv_in_type;
  signal io_ahbso         : ahb_slv_out_vector;
```

```
  signal io_ahbmi         : ahb_mst_in_type;
  signal io_ahbmo         : ahb_mst_out_vector;

  signal nolock           : griommu_ctrl_type;
  signal noifctrl         : griommu_ifctrl_type;
  signal dbgifctrl        : griommu_ifctrl_type;
  signal griommu_stato    : griommu_stat_type;

begin

nolock <= griommu_ctrl_none;
noifctrl <= griommu_ifctrl_none


-- Instantiate clock generators and AHBCTRL cores here
....
....
-- GRIOMMU
iommu: griommu
    generic map (
      memtech     => memtech,
      iohsindex   => 0,
      syshmindex  => 4,
      syshsindex  => 4,
      syshaddr    => 16#200#,
      syshmask    => 16#FFE#,
      syshirq     => 1,
      slv         => 0,
      dir         => 1,
      ffact       => 1,
      pfen        => 1,
      wburst      => 8,
      iburst      => 8,
      rburst      => 8,
      irqsync     => 0, -- No interrupt synchronization
      bar0        => ahb2ahb_membar(16#000#, '0', '0', 16#800#),
      bar1        => ahb2ahb_membar(16#800#, '0', '0', 16#800#),
      sbus        => 1,
      mbus        => 0,
      ioarea      => 16#FFF#,
      ibrsten     => 0,
      lckdac      => 0,
      slvmaccsz   => 32,  -- Maximum allowed access size by masters on io bus
      mstmaccsz   => 128, -- Maximum allowed access size on system bus
      rdcomb      => 2,
      wrcomb      => 2B,
      allbrst     => 0,
      ifctrlen    => 0,
      fcfs        => IO_NAHBM*CFG_IOMMU_FCFS,
      fcfsmtech   => 0,
      scantest    => scantest,
      split       => CFG_IOMMU_FCFS,
      nummst      => IO_NAHBM, -- Number of masters to support
      numgrp      => CFG_IOMMU_NUMGRP,
      stat        => CFG_IOMMU_STAT,
      apv         => CFG_IOMMU_APV,
      apv_accsz   => CFG_IOMMU_APVACCSZ,
      apvc_en     => CFG_IOMMU_APVCEN,
      apvc_ways   => 1,                  -- Only valid value
      apvc_lines  => CFG_IOMMU_APVCLINES,
      apvc_tech   => CFG_IOMMU_APVCTECH,
      apvc_gseta  => CFG_IOMMU_APVCGSETA,
      apvc_caddr  => CFG_IOMMU_APVCCADDR,
      apvc_cmask  => CFG_IOMMU_APVCCMASK,
      apvc_pipe   => CFG_IOMMU_APVCPIPE,
      iommu       => CFG_IOMMU_IOMMU,
      iommutype   => CFG_IOMMU_IOMMUTYPE,
      tlb_num     => CFG_IOMMU_TLBNUM,
      tlb_type    => CFG_IOMMU_TLBTYPE,
      tlb_tech    => CFG_IOMMU_TLBTECH,
      tlb_gseta   => CFG_IOMMU_TLBGSETA,
```

```
      tlb_pipe    => CFG_IOMMU_TLBPIPE,
      tmask       => 16#ff#,
      tbw_accsz   => CFG_IOMMU_TBWACCSZ,
      ft          => CFG_IOMMU_FT)
    port map (
      rstn        => rstn,
      hclksys     => clkm,
      hclkio      => clkm,
      io_ahbsi    => io_ahbsi,
      io_ahbso    => io_ahbso(0),
      io_ahbpnp   => io_ahbmo(IO_NAHBM-1 downto 0),
      sys_ahbmi   => sys_ahbmi,
      sys_ahbmo   => sys_ahbmo(4),
      sys_ahbpnp  => sys_ahbso,
      sys_ahbsi   => io_ahbsi,
      sys_ahbso   => io_ahbso(4),
      lcki        => nolock,
      lcko        => open,
      stato       => griommu_stato,
      ifctrl      => noifctrl);

end;
```

52 GRPCI2 - 32-bit PCI(Initiator/Target) / AHB(Master/Slave) bridge

52.1 Overview

The GRPCI2 core is a bridge between the PCI bus and the AMBA AHB bus. The core is capable of connecting to the PCI bus via both a target and a initiator/master interface. The connection to the AMBA bus is an AHB master interface for the PCI target functionality and an AHB slave interface for the PCI initiator functionality. The core also contains a DMA controller. For the DMA functionality, the core uses the PCI initiator to connect to the PCI bus and an AHB master to connect to the AMBA bus. Configuration registers in the core are accessible via a AMBA APB slave interface.

The PCI and AMBA interfaces belong to two different clock domains. Synchronization is performed inside the core through FIFOs with configurable depth.

The PCI interface is compliant with the 2.3 PCI Local Bus Specification.

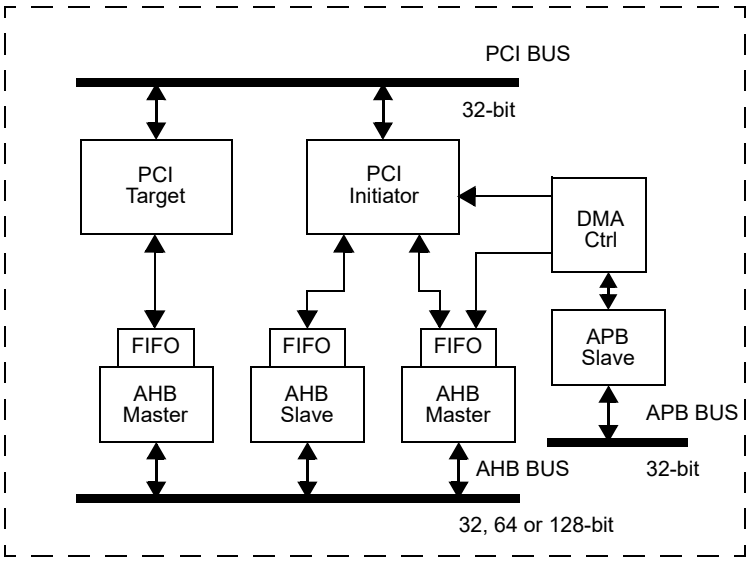


Figure 139. Block diagram

52.2 Configuration

The core has configuration registers located both in PCI Configuration Space (Compliant with the 2.3 PCI Local Bus Specification) and via an AMBA APB slave interface (for core function control and DMA control). This section defines which configuration options that are implemented in the PCI configuration space together with a list of capabilities implemented in the core. For a more detailed description of the core registers and DMA controller registers, see section Registers.

52.2.1 Configuration & Capabilities

Which of the core capabilities that are implemented is configured through VHDL generics at core instantiation. The implemented configuration can be determined by reading the Status & Capability register accessible via the APB slave interface.

- The PCI vendor and device ID is set with the VHDL generic *vendorid* and *deciceid*.
- The PCI class code and revision ID is set with the VHDL generic *classcode* and *revisionid*.
- 32-bit PCI initiator interface is implemented when the VHDL generic *master* is enabled.
- 32-bit PCI target interface is implemented when the VHDL generic *target* is enabled.

- DMA controller is implemented when the VHDL generic *dma* is enabled.
- The depth and number of FIFOs is configured with the VHDL generic *fifo_depth* and *fifo_count*.
- PCI BARs. The default size and number of BARs implemented is configured with the VHDL generic *bar0* to *bar5*.
- User defined register in Extended PCI Configuration Space can be enabled with the VHDL generic *ext_cap_pointer*.
- Device interrupt generation is enabled with the VHDL generic *deviceirq*.
- PCI interrupt sampling and forwarding is enabled with the VHDL generic *hostirq*.
- Support for two PCI functions is enabled with the VHDL generic multifunc.

52.2.2 PCI Configuration Space

The core implements the following registers in the PCI Configuration Space Header. For more detailed information regarding each field in these registers please refer to the PCI Local Bus Specification.

*Table 731.*GRPCI2: Implemented registers in the PCI Configuration Space Header

PCI address offset	Register
0x00	Device ID, Vendor ID
0x04	Status, Command
0x08	Class Code, Revision ID
0x0C	BIST, Header Type, Latency Timer, Cache Line Size
0x10 - 0x24	Base Address Registers
0x34	Capabilities Pointer
0x3C	Max_Lat, Min_Gnt, Interrupt Pin, Interrupt Line

52.2.2.1 Device ID and Vendor ID register

*Table 732.*0x00-0x10 - Device ID and Vendor ID register

31 16	15 0
Device ID	Vendor ID
*	*
r	r

31 : 16 Device ID, Set by the *deviceid* VHDL generic.

15 : 0 Vendor ID, Set by the *vendorid* VHDL generic.

52.2.2.2 Status and Command Register

*Table 733.*G0x04 - STSCMD - Status and Command register

31	30	29	28	27	26 25	24	23	22	21	20	19	18 11	10	9	8	7	6	5	4	3	2	1	0
DPE	SSE	RMA	RTA	STA	DEVSEL timing	MDPE	FBBC	RES	66MHz	CL	IS	RESERVED	ID	Not Imp	SE	RES	PER	Not Imp	MWI	Not Imp	BM	MS	Not Imp
0	0	0	0	0	0b01	0	0	0	*	1	0	0	0	0	0	0	0	0	0	0	0	0	0
wc	wc	wc	wc	wc	r	r	r	r	r	r		r	rw	r	rw	r	rw	r	rw	r	rw	rw	r

31 Detected Parity Error

30 Signaled System Error

29 Received Master Abort

28 Received Target Abort

27 Signaled Target Abort

26: 25 DEVSEL timing, Returns “01“ indicating medium

24 Master Data Parity Error

23 Fast Back-to-Back Capable, Returns zero. (Read only)

22 RESERVED

21 66 MHz Capable (Read only)
NOTE: In this core this bit has been defined as the status of the M66EN signal rather than the capability of the core. For a 33 MHz design, this signal should be connected to ground and this status bit will have the correct value of ‘0’. For a 66 MHz design, this signal is pulled-up by the backplane and this status bit will have the correct value of ‘1’. For a 66 MHz capable design inserted in a 33 MHz system, this bit will then unfortunate only indicate a 33 MHz capable device.

20 Capabilities List, Returns one (Read only)

19 Interrupt Status (Read only)

18: 11 RESERVED

10 Interrupt Disable

9 NOT IMPLEMENTED, Returns zero.

8 SERR# Enable

7 RESERVED

6 Parity Error Response

5 NOT IMPLEMENTED, Returns zero.

4 Memory Write and Invalidate Enable

3 NOT IMPLEMENTED, Returns zero.

2 Bus Master

1 Memory Space

0 NOT IMPLEMENTED, Returns zero.

52.2.2.3 Class Code and Revision ID Register

*Table 734.*0x08 - CCRID - Class Code and Revision ID register

31	8	7	0
Class Code		Revision ID	
*		*	
r		r	

31 : 8 Class Code, Set by the *classcode* VHDL generic.

7 : 0 Revision ID, Set by the *revisionid* VHDL generic.

52.2.2.4 BIST, Header Type, Latency Timer, and Cache Line Size Register

*Table 735.*0x0C- CCFG - BIST, Header Type, Latency Timer, and Cache Line Size register

31	24	23	16	15	8	7	0
BIST		Header Type		Latency Timer		Cache Line Size	
0		0		0		0	
r		r		rw		rw	

31 : 24 NOT IMPLEMENTED, Returns zeros

23 : 16 Header Type, Returns 00

15 : 8 Latency Timer, All bits are writable.

7 : 0 NOT IMPLEMENTED, Returns zero.

52.2.2.5 Base Address Registers

*Table 736.*0xC0-0x24 - BASEADDR - Base Address Registers

31	4	3	2	1	0
Base Address		PF	Type		MS
0		*	0		0
rw		r	r		r

31 : 4 Base Address. The size of the BAR is determine by how many of the bits (starting from bit 31) are implemented. Bits not implemented returns zero.

3 Prefetchable, Returns zero indicating non-prefetchable.

2 : 1 Type, Returns zero.

0 Memory Space Indicator

52.2.2.6 Capabilities Pointer Register

*Table 737.*0x34 - CAPP - Capabilities Pointer Register

31	8	7	0
RESERVED		Capabilities Pointer	
0		*	
r		r	

31 : 8 RESERVED

7 : 0 Capabilities Pointer. Indicates the first item in the list of capabilities of the Extended PCI Configuration Space. This offset is set with the VHDL generic *cap_pointer*.

52.2.2.7 Max_Lat, Min_Gnt, Interrupt Pin and Interrupt Line Register

*Table 738.*0x3C - CCFG2 - Max_Lat, Min_Gnt, Interrupt Pin and Interrupt Line register

31 24	23 16	15 8	7 0
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line
0	0	*	0
r	r	r	rw

31 : 24 NOT IMPLEMENTED, Returns zero

23 : 16 NOT IMPLEMENTED, Returns zero

15 : 8 Interrupt Pin, Indicates INTA# when VHDL generic *deviceirq* is 1, otherwise zero is returned (Read only)

7 : 0 Interrupt Line

52.2.3 Extended PCI Configuration Space

This section describes the first item in the list of capabilities implemented in the Extended PCI Configuration Space. This capability is core specific and contains the PCI to AMBA address mapping and the option to change endianess of the PCI bus.

When user defined capability list items are implemented, the next pointer defines the offset of this list item. The AMBA address mapping for these registers can be accessed in the core specific item (first list item). The registers implemented in this AMBA address range must be compliant to the capability list items defined in the 2.3 PCI Local Bus Specification.

*Table 739.*GRPCI2: Internal capabilities of the Extended PCI Configuration Space

PCI address offset (with the Capabilities pointer as base)	**Register**
0x00	Length, Next Pointer, ID
0x04 - 0x18	PCI BAR to AHB address mapping
0x1C	Extended PCI Configuration Space to AHB address mapping
0x20	AHB IO base address and PCI bus config (endianess switch)
0x24 - 0x38	PCI BAR size and prefetch
0x3C	AHB master burst limit

52.2.3.1 Length, Next Pointer and ID

Table 740. Length, Next pointer and ID (address offset 0x00)

31 24	23 16	15 8	7 0
RESERVED	Length	Next Pointer	Capability ID

31 : 24	RESERVED.
23 : 16	Length, Returns 0x40. (Read only)
15 : 8	Pointer to the next item in the list of capabilites.This offset is set with the VHDL generic *ext_cap_pointer*. (Read only)
7 : 0	Capability ID, Returns 0x09 indicating Vendor Specific. (Read only)

52.2.3.2 PCI BAR to AHB Address Mapping Register

Table 741. PCI BAR to AHB address mapping register (address offset 0x04 - 0x18)

31 0
PCI BAR to AHB address mapping

31 : 0	32-bit mapping register for each PCI BAR. Translate an access to a PCI BAR to a AHB base address. The size of the BAR determine how many bits (starting form bit 31) are implemented. Bits non implemented returns zero.

52.2.3.3 Extended PCI Configuration Space to AHB Address Mapping Register

Table 742. Extended PCI Configuration Space to AHB address mapping register (address offset 0x1C)

31 8	7 0
Extended PCI Configuration Space to AHB address mapping	RESERVED

31 : 8	Translates an access to the Extended PCI Configuration Space (excluding the address range for the internal register located in this configuration space) to a AHB address.
7 : 0	RESERVED

52.2.3.4 AHB IO Base Address and PCI Bus Config

Table 743. AHB IO base address and PCI bus config (endianess register) (address offset 0x20)

31 20	19 1	0
AHB IO base address	RESERVED	DISEN	Endian

31 : 8	Base address of the AHB IO area. (Read only, not replicated for each PCI function)
19 : 2	RESERVED
1	Target access discard time out enable. When set to ‘1’, the target will discard a pending access if no retry of the access is detected during 2**15 PCI clock cycles. (Not replicated for each PCI function)
0	PCI bus endianess switch. 1: defines the PCI bus to be little-endian, 0: defines the PCI bus to be big-endian. Reset value is set be the conv_endian VHDL generic. (Not replicated for each PCI function)

52.2.3.5 PCI BAR Size and Prefetch Register

Table 744. PCI BAR size and prefetch register (address offset 0x24 - 0x38)

31 : 4	3	2 : 1	0
PCI BAR size mask	Pre	RESERVED	Type

31 : 4	A size mask register for each PCI BAR. When bit[n] is set to '1' bit[n] in the PCI BAR register is implemented and can return a non-zero value. All bits from the lowest bit set to '1' up to bit 31 need to be set to '1'. When bit 31 is '0', this PCI BAR is disabled. The number of implemented bits in this field depends in the VHDL generic barminsize. The minimal size of the BAR is not allowed to be smaller than the internal FIFO.
3	Prefetch bit in PCI BAR register
2 : 1	RESERVED
0	BAR type. 0 = Memory BAR, 1 = IO BAR

52.2.3.6 AHB Master Prefetch Burst Limit

Table 745. AHB master burst limit (address offset 0x3C)

31	30 : 16	15 : 0
SRF	RESERVED	Burst length

31	Store Read FIFO. When set to 1, the prefetched FIFO will be stored until the next PCI access when the PCI target terminates the access with disconnect without data.
30 : 16	RESERVED
15 : 0	Maximum number of beats - 1 in the burst. (Maximum value is 0xFFFF => 0x10000 beats => 65kB address)

52.2.4 Multi-Function

The core supports up to two PCI functions starting from function 0. Each function has its own PCI configuration space located at offset 0x0 for function 0 and offset 0x100 for function 1. Some registers in the Extended PCI configuration space is shared between all functions. All functions also share the same Vendor ID.

52.3 Operation

52.3.1 Access support

The core supports both single and burst accesses on the AMBA AHB bus and on the PCI bus. For more information on which PCI commands that are supported, see the PCI target section and for burst limitations see the Burst section.

52.3.2 FIFOs

The core has separate FIFOs for each data path: PCI target read, PCI target write, PCI master read, PCI master write, DMA AHB-to-PCI, and DMA PCI-to-AHB. The number and depth of the FIFOs for each data path is configurable by VHDL generics.

52.3.3 Byte enables and byte twisting (endianess)

The core has the capability of converting endianess between the two busses. This means that all byte lanes can be swapped by the core as shown in figure below.

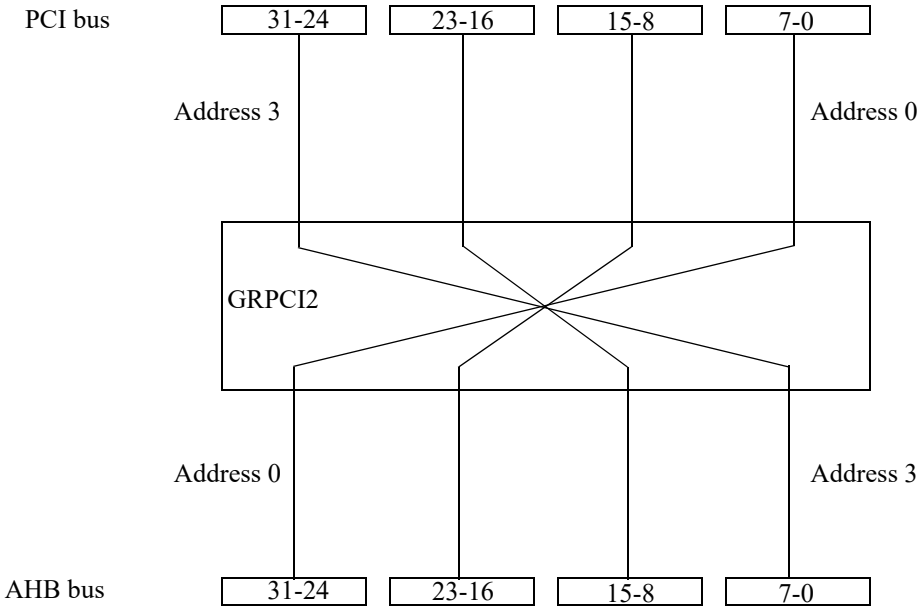


Figure 140. GRPCI2 byte twisting

Table 746 defines the supported AHB address/size and PCI byte enable combinations.

*Table 746.*AHB address/size <=> PCI byte enable combinations.

AHB HSIZE	AHB ADDRESS[1:0]	Little-endian CBE[3:0]	Big-endian CBE[3:0]
00 (8-bit)	00	1110	0111
00 (8-bit)	01	1101	1011
00 (8-bit)	10	1011	1101
00 (8-bit)	11	0111	1110
01 (16-bit)	00	1100	0011
01 (16-bit)	10	0011	1100
10 (32-bit)	00	0000	0000

As the AHB bus in GRLIB is defined as big-endian, the core is able to define the PCI bus as little-endian (as defined by the PCI Local Bus Specification) with endianess conversion or define the PCI bus as big-endian without endianess conversion.

The endianess of the PCI bus is configured via the core specific Extended PCI Configuration Space. The default value is set by a VHDL generic *conv_endian*.

52.3.4 PCI configuration cycles

Accesses to PCI Configuration Space are not altered by the endianess settings. The PCI Configuration Space is always defined as little-endian (as specified in the PCI Local Bus Specification). This means that the PCI target does not change the byte order even if the endianess conversion is enabled and the PCI master always converts PCI Configuration Space accesses to little-endian.

Data stored in a register in the PCI Configuration Space as 0x12345678 (bit[31:0]) is transferred to the AHB bus as 0x78563412 (bit[31:0]). This means that non-8-bit accesses to the PCI Configuration Space must be converted in software to get the correct byte order.

52.3.5 Memory and I/O accesses

Memory and I/O accesses are always affected by the endianess conversion setting. The core should define the PCI bus as little-endian in the following scenarios: When the core is the PCI host and little-endian peripherals issues DMA transfers to host memory. When the core is a peripheral device and issues DMA transfers to a little-endian PCI host.

52.3.6 Bursts

PCI bus: The PCI target terminates a burst when no FIFO is available (the AMBA AHB master is not able to fill or empty the FIFO fast enough) or when the burst reached the length specified by the "AHB master burst limit" register. This register defines a boundary which a burst can not cross i.e. when set to 0x400 beats (address boundary at 4kB) the core only prefetch data up to this boundary and then terminates the burst with a disconnect.

The PCI master stops the burst when the latency timer times out (see the PCI Local Bus Specification for information on the latency timer) or for reads when the burst reaches the limit defined by "PCI master prefetch burst limit" register (if AHB master performing the access is unmasked). If the master is masked in this register, the limit is set to 1kB. The PCI master do not prefetch data across this address boundary.

AHB bus: As long as FIFOs are available for writes and data in a FIFO is available for read, the AHB slave do not limit the burst length. The burst length for the AHB master is limited by the FIFO depth. The AHB master only burst up to the FIFO boundary. Only linear-incremental burst mode is supported.

DMA: DMA accesses are not affected by the "AHB master prefetch burst limit" register or the "PCI master prefetch burst limit" register.

All FIFOs are filled starting at the same word offset as the bus access (i.e. with a FIFO of depth 8 words and the start address of a burst is 0x4, the first data word is stored in the second FIFO entry and only 7 words can be stored in this FIFO).

52.3.7 Host operation

The core provides a system host input signal that must be asserted (active low) for PCI system host operations. The status of this signal is available in the Status & Capability register accessible via the APB slave interface. The device is only allowed to generate PCI configuration cycles when this signal is asserted (device is the system host).

For designs intended to be host or peripherals only the PCI system host signal can be tied low or high internally in the design. For multi-purpose designs it should be connected to a pin. The PCI Industrial Computer Manufacturers Group (PCIMG) cPCI specification uses pin C2 on connector P2 for this purpose. The pin should have a pull-up resistor since peripheral slots leave it unconnected.

An asserted PCI system host signal makes the PCI target respond to configuration cycles when no IDSEL signal is asserted (none of AD[31:11] are asserted). This is done for the PCI master to be able to configure its own PCI target.

52.4 PCI Initiator interface

The PCI master interface is accessible via the AMBA AHB slave interface. The AHB slave interface occupies 1MB to 2GB of the AHB memory address space and 128kB to 256kB of AHB I/O address space. An access to the AHB memory address area is translated to a PCI memory cycle. An access to the first 64kB of the AHB IO area is translated to a PCI I/O cycle. The next 64kB are translated to PCI

configuration cycles. When the PCI trace buffer is implemented, it is accessible via the last 128kB of the AHB I/O area.

52.4.1 Memory cycles

A single read access to the AHB memory area is translated into a PCI memory read access, while a burst read translates into a PCI memory read multiple access. A write to this memory area is translated into a PCI write access.

The address translation is determined by AHB master to PCI address mapping registers accessible via the APB slave interface. Each AHB master on the AMBA AHB bus has its own mapping register. These registers contain the MSBs of the PCI address.

When the PCI master is busy performing a transaction on the PCI bus and not able to accept new requests, the AHB slave interface will respond with an AMBA RETRY response. This occurs on reads when the PCI master is fetching the requested data to fill the read FIFO or on writes when no write FIFO is available. This means that all masters on the AMBA bus accessing the AHB slave interface must be round-robin arbitrated without prioritization to avoid deadlock situations.

52.4.2 I/O cycles

Accesses to the lowest 64kB of the AHB I/O address area are translated into PCI I/O cycles. The address translation is determined by the “AHB to PCI mapping register for PCI I/O”. This register sets the 16 MSB of the PCI address. The “AHB to PCI mapping register for PCI I/O” is accessible via the APB slave interface. When the “IB” (PCI IO burst) bit in the Control register (accessible via the APB slave interface) is cleared, the PCI master does not perform burst I/O accesses.

52.4.3 Configuration cycles

Accesses to the second 64kB address block (address offset range 64kB to 128kB) of the AHB I/O address area is translated into PCI configuration cycles. The AHB address is translated into PCI configuration address different for type 0 and type 1 PCI configuration cycles. When the “bus number” field in the control register (accessible via the APB slave interface) is zero, type 0 PCI configuration cycles is issued. When the “bus number“ field is non-zero, type 1 PCI configuration cycles are issued to the PCI bus determine by this field. The AHB I/O address mapping to PCI configuration address for type 0 and type 1 PCI configuration cycles is defined in table 747 and table 748.

Only the system host is allowed to generate PCI configuration cycles. The core provides a system host input signal that must be asserted (active low) for PCI system host operations. The status of this signal is available in the Status & Capability register accessible via the APB slave interface.When the “CB” (PCI Configuration burst) bit in the Control register (accessible via the APB slave interface) is cleared, the PCI master does not perform burst configuration accesses.

52.4.3.1 Mapping of AHB I/O address to PCI Configuration Cycle, type 0

Table 747. GRPCI2 Mapping of AHB I/O address to PCI configuration cycle, type 0

31 16	15 11	10 8	7 2	1 0
AHB ADDRESS MSB	IDSEL	FUNC	REGISTER	BYTE

31: 16	AHB address MSBs: Not used for PCI configuration cycle address mapping.
15: 11	IDSEL: This field is decoded to drive PCI AD[IDSEL+10]. Each of the signals AD[31:11] are suppose to be connected (by the PCI back plane) to one corresponding IDSEL line.
10: 8	FUNC: Selects function on a multi-function device.
7: 2	REGISTER: Used to index a PCI DWORD in configuration space.
1: 0	BYTE: Used to set the CBE correctly for non PCI DWORD accesses.

52.4.3.2 Mapping of AHB I/O address to PCI Configuration Cycle, type 1

Table 748. GRPCI2 Mapping of AHB I/O address to PCI configuration cycle, type 1

31 16	15 11	10 8	7 2	1 0
AHB ADDRESS MSB	DEVICE	FUNC	REGISTER	BYTE

31: 16	AHB address MSBs: Not used for PCI configuration cycle address mapping.
15: 11	DEVICE: Selects which device on the bus to access.
10: 8	FUNC: Selects function on a multi-function device.
7: 2	REGISTER: Used to index a PCI DWORD in configuration space.
1: 0	BYTE: Used to set the CBE correctly for non PCI DWORD accesses.

52.4.4 Error handling

When a read access issued by the PCI master is terminated with target-abort or master-abort, the AHB slave generates an AMBA ERROR response when the “ER” bit in the control register is set. When the “EI“ bit in the control register is set, an AMBA interrupt is generated for the error. The interrupt status field in the control register indicates the cause of the error.

52.4.5 Bus parking

The PCI initiator supports bus parking and will drive the PCI bus to a defined state when granted without requesting the bus. In systems with one single initiator the grant input to the PCI interface can be constantly asserted.

52.5 PCI Target interface

The PCI Target occupies memory areas in the PCI address space corresponding to the BAR registers in the PCI Configuration Space. Each BAR register (BAR0 to BAR5) defines the address allocation in the PCI address space. The size of each BAR is set by the “BAR size and prefetch” registers accessible via the core specific Extended PCI Configuration Space. The size of a BAR can be determined by checking the number of implemented bits in the BAR register. Non-implemented bits returns zero and are read only. The size of the BAR is not allowed to be smaller then the size of the internal FIFO.

52.5.1 Supported PCI commands

These are the PCI commands that are supported by the PCI target.

- **PCI Configuration Read/Write:** Burst and single access to the PCI Configuration Space. These accesses are not transferred to the AMBA AHB bus except for the access of the user defined capability list item in the Extended PCI Configuration Space.

- **Memory Read:** A read command to the PCI memory BAR is transferred to a single read access on the AMBA AHB bus.
- **Memory Read Multiple, Memory Read Line:** A read multiple command to the PCI memory BAR is transferred to a burst access on the AMBA AHB bus. This burst access prefetch data to fill the maximum amount of data that can be stored in the FIFO.
- **Memory Write, Memory Write and Invalidate:** These command are handled similarly and are transferred to the AMBA AHB bus as a single or burst access depending on the length of the PCI access (a single or burst access).
- **IO Read:** A read command to the PCI IO BAR is transferred to a single read access on the AMBA AHB bus.
- **IO Write:** A write command to the PCI IO BAR is transferred to the AMBA AHB bus as a single access.

52.5.2 Implemented PCI responses

The PCI target can terminate a PCI access with the following responses.

- **Retry:** This response indicates the PCI target is busy by either fetching data for the AMBA AHB bus on a PCI read or emptying the write FIFO for a PCI write. A new PCI read access will always be terminated with a retry at least one time before the PCI target is ready to deliver data.
- **Disconnect with data:** Terminate the transaction and transfer data in the current data phase. This occurs when the PCI master request more data and the next FIFO is not yet available or for a PCI burst access with the Memory Read command.
- **Disconnect without data:** Terminate the transaction without transferring data in the current data phase. This occurs if the CBE change within a PCI burst write.
- **Target Abort:** Indicates that the current access caused an internal error and the target is unable to finish the access. This occurs when the core receives a AMBA AHB error during a read operation.

52.5.3 Supported byte-enables (CBE)

The PCI-target only supports aligned 8-, 16-, and 32-bit accesses. The supported combinations of CBE are 0000, 1110, 1101, 1011, 0111, 1100, 0011. All other combinations of CBE are interpret as a 32-bit access (CBE = 0000) except for writes with CBE set to 1111, which is treated as a no-operation (no write will be performed).

52.5.4 PCI to AHB translation

Each PCI BAR has translation register (mapping register) to translate the PCI access to a AMBA AHB address area. These mapping registers are accessible via the core specific Extended PCI Configuration Space. The number of implemented bits in these registers correspond to the size of (and number of implemented bits in) the BARs registers.

52.5.5 PCI system host signal

When the PCI system host signal is asserted the PCI target responds to configuration cycles when no IDSEL signal is asserted (none of AD[31:11] are asserted). This is done for the PCI master, in a system host position, to be able to configure its own PCI target.

52.5.6 Error handling

The PCI target terminates the access with target-abort when the PCI target requests data from the AHB bus which results in an error response on the AHB bus. Because the writes to the PCI target is posted, no error is reported on write AHB errors.

When a PCI master is terminated with a retry response it is mandatory for that master to retry this access until the access is completed or terminated with target-abort. If the master never retries the access, the PCI target interface would be locked on this access and never accept any new access. To recover from this situation, the PCI target has a option to discard an access if it is not retried within 2**15 clock cycles. This discard time out can be enabled via the “AHB IO base address and PCI bus config” located in the core specific Extended PCI Configuration Space.

52.6 DMA Controller

The DMA engine is descriptor base and uses two levels of descriptors.

52.6.1 DMA channel

The first level is a linked list of DMA channel descriptors. Each descriptor has a pointer to its data descriptor list and a pointer to the next DMA channel. The last DMA channel descriptor should always points to the first DMA channel for the list to be a closed loop. The descriptor needs to be aligned to 4 words (0x10) in memory and have the following structure.

*Table 749.*GRPCI2: DMA channel descriptor structure

Descriptor address offset	Descriptor word
0x00	DMA channel control
0x04	Next DMA channel (32-bit address to next DMA channel descriptor).
0x08	Next data descriptor in this DMA channel (32-bit address to next data descriptor).
0x0C	RESERVED

52.6.1.1 DMA Channel Control

Table 750. GRPCI2 DMA channel control

31	25	24	22	21	20	19	16	15	0
EN	RESERVED		CID		Type	RESERVED		Data descriptor count	

31	Channel descriptor enable (for version < 2, this bit should always be set to ‘1’).
30: 25	RESERVED
24: 22	Channel ID. Each DMA channel needs a ID to determine the source of a DMA interrupt.
21: 20	Descriptor type. 01 = DMA channel descriptor.
19: 16	RESERVED
15: 0	Maximum number of data descriptors to be executed before moving to the next DMA channel. 0 indicates that all data descriptors should be executed before moving to the next DMA channel.

The number of enabled DMA channels must be stored in the “Number of DMA channels“ field in the DMA control register accessible via the APB slave interface.

52.6.2 Data descriptor

The second descriptor level is a linked list of data transfers. The last descriptor in this list needs to be a disabled descriptor. To add a new data transfer, this disabled descriptor is updated to reflect the data transfer and to point to a new disabled descriptor. The control word in the descriptor should be

updated last to enable the valid descriptor. To make sure the DMA engine reads this new descriptor, the enable bit in the DMA control register should be updated. The descriptor needs to be aligned to 4 words (0x10) in memory and have the following structure.

*Table 751.*GRPCI2: DMA data descriptor structure

Descriptor address offset	Descriptor word
0x00	DMA data control
0x04	32-bit PCI start address
0x08	32-bit AHB start address
0x0C	Next data descriptor in this DMA channel (32-bit address to next data descriptor).

52.6.2.1 DMA Data Control

Table 752. GRPCI2 DMA data control

31	30	29	28	22	21	20	19	18	16	15	0
EN	IE	DR	BE	RESERVED		Type	ER	RESERVED		LEN	

31	Data descriptor enable.
30	Interrupt generation enable.
29	Transfer direction. 0: PCI to AMBA, 1: AMBA to PCI.
28	PCI bus endianess switch. 1: defines the PCI bus to be little-endian for this transfer, 0: defines the PCI bus to be big-endian for this transfer.
27: 22	RESERVED (Must be set to zero)
21: 20	Descriptor type. 00 = DMA data descriptor.
19	Error status
18: 16	RESERVED
15: 0	Transfer length. The number of word of the transfer is (this field)+1.

52.6.3 Data transfer

The DMA engine starts by reading the descriptor for the first DMA channel. If the DMA channel is enabled the first data descriptor in this channel is read and executed. When the transfer is done the data descriptor is disabled and status is written to the control word. If no error occurred during the transfer, the error bit is not set and the transfer length field is unchanged. If the transfer was terminated because of an error, the error bit is set in the control word and the length field indicates where in the transfer the error occurred. If no error has occurred, the next data descriptor is read and executed. When a disabled data descriptor is read or the maximum number of data descriptors has been executed, the DMA channel descriptor is updated to point to the next data descriptor and the DMA engine moves on to the next DMA channel.

When a disabled channel descriptor is read, the DMA controller will move on to the next DMA channel without reading in any data descriptors form the disabled channel (Only applies to version 2 of the core).

When the DMA is disabled (via the APB interface), the channel descriptor is updated to point to the next data descriptor (Only applies to version 2 of the core).

The DMA engine will stop when an error is detected or when no enabled data descriptors is found. The error type is indicated by bit 7 to bit 11 in the DMA control register. The error type bits must be cleared (by writing ‘1’) before the DMA can be reenabled.

52.6.4 Interrupt

The DMA controller has an interrupt enable bit in the DMA control register (accessible via the APB slave interface) which enables interrupt generation.

Each data descriptor has an interrupt enable bit which determine if the core should generate a interrupt when the descriptor has been executed.

The VHDL generic *irqmode* determines if the DMA engine assert the same interrupt as the PCI core or the DMA uses the irq signal following the PCI core interrupt, see the IRQ mode field in the Status and Capability register for irq routing information.

52.7 PCI trace buffer

52.7.1 Trace data

The data from the trace buffer is accessible in the last 128 kB block of the AHB I/O address area. Each 32-bit word in the first 64kB of this block represents a sample of the AD PCI signal. The second 64kB of the block is the corresponding PCI control signal. Each 32-bit word is defined in table 753.

52.7.1.1 PCI Control Signal Trace (32-bit word)

Table 753. GRPCI2 PCI control signal trace (32-bit word)

31	20	19	16	15	14	13	12	11	10	9	8	7	6	5	4	3	0
RESERVED		CBE[3:0]		FRAME	IRDY	TRDY	STOP	DEVSEL	PAR	PERR	SERR	IDSEL	REQ	GNT	LOCK	RST	RES

31: 20	RESERVED
19: 3	The state of the PCI control signals.
2: 0	RESERVED

52.7.2 Triggering function

The core can be programmed to trigger on any combination of the PCI AD and PCI Control signals by setting up the desired pattern and mask in the PCI trace buffer registers accessible via the APB slave interface. Each bit the PCI AD signal and any PCI control signal can be masked (mask bit equal to zero) to always match the triggering condition.

The “Trig count” field in the “PCI trace buffer: counter & mode” register defines how many times the trigger condition should occur before the trace buffer disarms and eventually stops sampling. The number of samples stored after the triggering condition occurs defines by the “Delayed stop“ + 2.

To start sampling, the trace buffer needs to be armed by writing one to the start bit in the “PCI trace buffer: Control“ register. The state of the trace buffer can be determine by reading the Armed and Enable/Running bit in the control register. When the Armed bit is set, the triggering condition has not occurred. The Enable/Running bit indicates that the trace buffer still is storing new samples. When the delayed stop field is set to a non zero value, the Enabled bit is not cleared until all samples are stored in the buffer). The trace buffer can also be disarmed by writing the “stop” bit in the “PCI trace buffer: control” register.

When the trace buffer has been disarmed, the “trig index” in the “PCI trace buffer: control” register is updated with index of trace entry which match the triggering condition. The address offset of this entry is the value of the “trig index“ field times 4.

52.7.3 Trace Buffer APB interface

A separate APB register can optionally be enabled for access of the PCI trace buffer. The register layout is the same as the core APB interface but only registers related to the PCI trace buffer is accessable. The trace buffer data is located at offset 0x20000 for PCI AD and offset 0x30000 for PCI control signals.

52.8 Interrupts

The core is capable of sampling the PCI INTA-D signals and forwarding the interrupt to the APB bus. The PCI INTA-D signals can be connected to one APB irq signal or to 4 different irq signals. This is configured by the VHDL generic *irqmode*. The “host INT mask” field in the control register is used only for sampling the valid PCI INT signal.

The core supports PCI interrupt generation. For single function configuration the dirq signal is sampled and forwarded to the PCI INTA signal. For a multi function (and multi interrupt) configured device, each bit of the dirq signal is connected to one of the PCI INTA..D signal (dirq[0] => INTA, dirq[1] => INTB, ...). The core has a mask bit (the “device INT mask“ field in the control register) for each bit in the dirq vector. The core also has a PCI interrupt force bit in the control register to be able to force the PCI INT asserted. For a multi interrupt configuration the PCI interrupt force bit is masked by the “device INT mask” to be able to assert all PCI INT signals separately.

When the system error PCI signal (SERR) is asserted the core sets the system error bit in the “core interrupt status” field in the Status & Capability register. If the system interrupts is enabled the core will also generate a interrupt on the APB bus.

52.9 Registers

The core is configured via registers mapped into the APB memory address space.

*Table 754.*GRPCI2: APB registers

APB address offset	Register
0x00	Control
0x04	Status & Capability (Read only)
0x08	PCI master prefetch burst limit
0x0C	AHB to PCI mapping for PCI IO
0x10	DMA Control & Status
0x14	DMA descriptor base
0x18	DMA channel active (read only)
0x1C	RESERVED
0x20 - 0x34	PCI BAR to AHB address mapping (Read only)
0x38	RESERVED
0x3C	RESERVED
0x40 - 0x7C	AHB master to PCI memory address mapping
0x80	PCI trace buffer: control & status
0x84	PCI trace buffer: counter & mode
0x88	PCI trace buffer: AD pattern
0x8C	PCI trace buffer: AD mask
0x90	PCI trace buffer: Ctrl signal pattern
0x94	PCI trace buffer: Ctrl signal mask
0x98	PCI trace buffer: AD state
0x9C	PCI trace buffer: Ctrl signal state

52.9.1 Control Register

Table 755. 0x00 - CTRL - Control register

31	30	29	28	27	26	25	24	23 16	15 12	11	10	9	8	7 4	3 0
RE	MR	TR	R	SI	PE	ER	EI	Bus Number	RESERVED	DFA	IB	CB	DIF	Device INT mask	Host INT mask
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rw	rw	rw	r	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw

31 PCI reset. When set, the PCI reset signal is asserted. Needs to be cleared to deassert PCI reset.

30 PCI master reset. Set to reset the cores PCI master. This bit is self clearing.

29 PCI target reset. Set to reset the cores PCI target. This bit is self clearing.

28 RESERVED

27 When set, Interrupt is enabled for System error (SERR)

26 When set, AHB error response is enabled for Parity error

25 When set, AHB error response is enabled for Master and Target abort.

24 When set, Interrupt is enabled for Master and Target abort and Parity error.

23: 16 When not zero, type 1 configuration cycles is generated.This field is also used as the Bus Number in type 1 configuration cycles.

15: 12 RESERVED

11 Disable internal AHB-slave / DMA fair arbitration (DFA). When this bit is set, the arbitration is done when the current transfer has complete.

10 When set, burst accesses may be generated by the PCI master for PCI IO cycles

9 When set, burst accesses may be generated by the PCI master for PCI configuration cycles.

8 Device interrupt force. When set, a PCI interrupt is forced.

7: 4 Device interrupt mask. When bit[n] is set dirq[n] is unmasked

3: 0 Host interrupt mask
bit[3] = 1: unmask INTD.
bit[2] = 1: unmask INTC.
bit[1] = 1: unmask INTB.
bit[0] = 1: unmask INTA.

52.9.2 Status and Capability Register

Table 756. 0x04 - STATCAP - Status and Capability register

31	30	29	28	27	26	25 24	23	22	21	20	19	18 12	11 8	7 5	4 2	1 0
Host	MST	TAR	DMA	DI	HI	IRQ mode	Trace	RES	FH	CFGDO	CFGER	Core interrupt status	Host interrupt status	RES	FDEPTH	FNUM
*	*	*	*	*	*	*	*	0	0	0	0	0	*	0	*	*
r	r	r	r	r	r	r	r	r	r	r	r	wc	r	r	r	r

31 When zero, the core is inserted in the System slot and is allowed to act as System Host.

30 Master implemented

29 Target implemented

28 DMA implemented

27 Device drives PCI INTA

26 Device samples PCI INTA..D (for host operations)

25: 24 APB IRQ mode
00: PCI INTA..D, Error interrupt and DMA interrupt on the same IRQ signal
01: PCI INTA..D and Error interrupt on the same IRQ signal. DMA interrupt on IRQ+1
10: PCI INTA..D on IRQ..IRQ+3. Error interrupt and DMA interrupt on IRQ.
11: PCI INTA..D on IRQ..IRQ+3. Error interrupt on IRQ. DMA interrupt on IRQ+4

23 PCI trace buffer implemented

Table 756. 0x04 - STATCAP - Status and Capability register

22	RESERVED
21	Fake device in system slot (Host). This bit should always be written with '0'. Only for debugging.
20	PCI configuration access done, PCI configuration error status valid.
19	Error during PCI configuration access
18: 12	Interrupt status: bit[6]: PCI target access discarded due to time out (access not retried for 2**15 PCI clock cycles) bit[5]: System error bit[4]: DMA interrupt bit[3]: DMA error bit[2]: Master abort. bit[1]: Target abort. bit[0]: Parity error.
11: 8	Host interrupt status bit[3] = 0: indicates that INTD is asserted. bit[2] = 0: indicates that INTC is asserted. bit[1] = 0: indicates that INTB is asserted. bit[0] = 0: indicates that INTA is asserted.
7: 5	RESERVED
4: 2	Words in each FIFO = 2**(FIFO depth)
1: 0	Number of FIFOs

52.9.3 Master Prefetch Burst Limit

Table 757. 0x08 - BCIM - PCI master prefetch burst limit

31 24	23 16	15 8	7 0
AHB master unmask		RESERVED	Burst length
0		0	0xFF
rw		r	rw

31 : 16 When bit[n] is set, the prefetch burst of AHB master n is limited by the “Burst length” field.

15 : 8 RESERVED

7 : 0 Maximum number of beats - 1 in the burst. (Maximin value is 0xFF => 0x100 beats => 1kB address)

52.9.4 AHB to PCI Mapping for PCI IO

Table 758. 0x0C - AHB2PCI - AHB to PCI mapping for PCI IO

31 16	15 0
AHB to PCI IO	RESERVED
0	0
rw	r

31 : 16 Used as the MSBs of the base address for a PCI IO access.

15 : 0 RESERVED

52.9.5 DMA Control and Status Register

Table 759. 0x10 - DMACTRL - GRPCI2 DMA control and status register

31	30 - 20	19 12	11	10	9	8	7	6 4	3	2	1	0
SAFE	RES	CHIRQ	MA	TA	PE	AE	DE	Number of DMA channels	ACTIVE	DIS	IE	EN
1	0	0	0	0	0	0	0	0	0	0	0	0
rw	r	wc	wc	wc	wc	wc	wc	rw	r	rw	rw	rw

31 Safety guard for update of control fields. Needs to be set to ‘1’ for the control fields to be updated.

30 : 20 RESERVED

19 : 12 Channel IRQ status. Set to ‘1’ when a descriptor is configured to signal interrupt. bit[0] corresponds to the channel with ID 0, bit[1] corresponds to the channel with ID 1, ... Clear by writing ‘1’.

11 Master abort during PCI access. Clear by writing ‘1’

10 Target abort during PCI access. Clear by writing ‘1’

9 Parity error during PCI access. Clear by writing ‘1’

8 Error during AHB data access. Clear by writing ‘1’

7 Error during descriptor access. Clear by writing ‘1’.

6 : 4 Number of DMA channels (Guarded by bit[31], safety guard)

3 DMA is active (read only)

2 DMA disable/stop. Writing ‘1’ to this bit disables the DMA.

1 Interrupt enable (Guarded by bit[31], safety guard).

0 DMA enable/start. Writing ‘1’ to this bit enables the DMA.

52.9.6 DMA Descriptor Base Address (/ Active Descriptor) Register

Table 760. 0x14 - DMABASE - DMA descriptor base address (/ Active Descriptor) register

31	0
DMA descriptor base address	
0	
rw	

31 : 0 Base address of the DMA descriptor table. When running, this register points to the active descriptor.

52.9.7 DMA Channel Active Register

Table 761. 0x18 - DMACHAN - DMA channel active register

31	0
DMA descriptor base address	
0	
rw	

31 : 0 Base address of the active DMA channel.

52.9.8 PCI BAR to AHB Address Mapping Register

Table 762. 0x20-0x34 - PCI2AHB - PCI BAR to AHB address mapping register

31	0
PCI BAR to AHB address mapping	
0	
rw	

31 : 0 32-bit mapping register for each PCI BAR. Translate an access to a PCI BAR to a AHB base address.

52.9.9 AHB Master to PCI Memory Address Mapping Register

Table 763. 0x40-0x7C - AHBM2PCI - AHB master to PCI memory address mapping register

31	0
AHB master to PCI memory address mapping	
0	
rw	

31 : 0 32-bit mapping register for each AHB master. Translate an access from a specific AHB master to a PCI base address. The size of the AHB slave address area determine how many bits (starting from bit 31) are implemented. Bits not implemented returns zero. The mapping register for AHB master 0 is located at offset 0x40, AHB master 1 at offset 0x44, and so on up to AHB master 15 at offset 0x7C. Mapping registers are only implemented for existing AHB masters.

52.9.10 PCI Trace Control and Status Register

Table 764. 0x80 - TCTRC - PCI trace Control and Status register

31 16	15	14	13 12	11 4	3 2	1	0
TRIG INDEX	AR	EN	RES	DEPTH	RES	SO	SA
NR	0	0	0	*	0		
r	r	r	r	r	r	w	w

31: 16 Index of the first entry of the trace.

15 Set when trace buffer is armed (started but the trig condition has not occurred).

14 Set when trace buffer is running

13: 12 RESERVED

11: 4 Number of buffer entries = 2**DEPTH

3: 2 RESERVED

1 Stop tracing. (Write only)

0 Start tracing. (Write only)

52.9.11 PCI Trace Counter and Mode Register

Table 765. 0x84 - TMODE - PCI trace counter and mode register

31 28	27 24	23 16	15 0
RES	Trace mode	Trig count	Delayed stop
0	0	0	0
r	rw	rw	rw

31: 28 RESERVED

27: 24 Tracing mode
00: Continuos sampling
01: RESERVED
10: RESERVED
11: RESERVED

23: 16 The number of times the trig condition should occur before the trace is disarmed.

15: 0 The number of entries stored after the trace buffer has been disarmed. (Should not be lager than number of buffer entries - 2).

52.9.12 PCI Trace AD Pattern Register

Table 766. 0x88 - TADP - PCI trace AD pattern register

31 0
PCI AD pattern
NR
rq

31: 0 AD pattern to trig on

52.9.13 PCI Trace AD Mask Register

Table 767. 0x8C - TADM - PCI trace AD mask register

31 0
PCI AD mask
NR
rw

31: 0 Mask for the AD pattern. When mask bit[n] = 0 pattern bit[n] will always be a match.

52.9.14 PCI Trace Ctrl Signal Pattern Register

Table 768. 0x90 - TCP - PCI trace Ctrl signal pattern register

31 20	19 16	15	14	13	12	11	10	9	8	7	6	5	4	3 0
RESERVED	CBE[3:0]	FRAME	IRDY	TRDY	STOP	DEVSEL	PAR	PERR	SERR	IDSEL	REQ	GNT	LOCK	RST	RES
0	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	0
r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	r

31: 20 RESERVED

19: 3 PCI Ctrl signal pattern to trig on

2: 0 RESERVED

52.9.15 PCI Trace Ctrl Signal Mask Register

Table 769. 0x94 - TCM - PCI trace Ctrl signal mask register

31 20	19 16	15	14	13	12	11	10	9	8	7	6	5	4	3 0
RESERVED	CBE[3:0]	FRAME	IRDY	TRDY	STOP	DEVSEL	PAR	PERR	SERR	IDSEL	REQ	GNT	LOCK	RST	RES
0	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	0
r		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	r

31: 20 RESERVED

19: 3 Mask for the Ctrl signal pattern. When mask bit[n] = 0 pattern bit[n] will always be a match.

2: 0 RESERVED

52.9.16 PCI Trace PCI AD State Register

Table 770. 0x98 - TADS - PCI trace PCI AD state register

31 0
Sampled PCI AD signal
NR
r

31: 0 The state of the PCI AD signal.

52.9.17 PCI Trace PCI Ctrl Signal State Register

Table 771. 0x9C - TCS - PCI trace PCI Ctrl signal state register

31 20	19 16	15	14	13	12	11	10	9	8	7	6	5	4	3 0
RESERVED	CBE[3:0]	FRAME	IRDY	TRDY	STOP	DEVSEL	PAR	PERR	SERR	IDSEL	REQ	GNT	LOCK	RST	RES
0	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR	NR
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

31: 20 RESERVED

19: 3 The state of the PCI Ctrl signals.

2: 0 RESERVED

52.10 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x07C. The DMA engine has device identifier 0x07D. The separate APB interface for the PCI Trace-Buffer has device identifier 0x07E. For description of vendor and device identifier see GRLIB IP Library User's Manual

52.11 Implementation

52.11.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). By default, the core makes use of synchronous reset and resets a subset of its internal registers in the system clock domain.

The deassertion of the PCI reset is synchronized to the PCI clock and delayed 3 clock cycles.

The core can be configured to drive the AHB reset on the PCI reset signal. This option is used when the backplane does not have logic to drive the PCI reset.

The PCI reset signal can optionally be forwarded to the AHB reset via the ptarst signal. This functionality can be used then the AMBA clock domain needs to be reset when the PCI reset is asserted.

The core require that the PCI and AMBA clock domain is reset at the same time, i.e. the PCI reset and the AMBA reset needs to be asserted at the same time.

52.11.2 Technology mapping

The core has a technology mapping VHDL generic, *memtech*, which controls how the memory cell used will be implemented. See the GRLIB Users's Manual for available settings.

52.11.3 RAM usage

The FIFOs in the core is implemented with the *syncram_2pft* (with separate clocks for each port) component from the technology mapping library (TECHMAP). Each data path implements its FIFOs in a separate 32-bit wide syncram_2pft component. The depth of each of these RAMs is the FIFO depth * number of FIFOs.

52.11.4 Pull-ups

Please refer to the PCI Local Bus Specification on which of the PCI signals needs to have pull-ups for correct operations.

52.11.5 PHY

All logic and registers directly controlled by the PCI bus signals has be placed in a separate entity. This makes it easier to control the setup-, hold- and clock-to-out timing for the PCI bus signals. This logic can also be implemented as a netlist which can be manually placed before running place-and-route for the entire design. A netlist is provided for Axcelerator and RTAX targets.

52.12 Configuration options

Table 772 shows the configuration options of the core (VHDL generics).

*Table 772.*Configuration options

Generic name	Function	Allowed range	Default
memtech	The memory technology used for the internal FIFOs.	0 - NTECH	0
tbmemtech	The memory technology used for trace buffers	0 - NTECH	0
oepol	Polarity of the pad output enable signal. 0 = active low, 1 = active high.	0 - 1	0
hmindex	AHB master index.	0 - NAHBMST-1	0
hdmindex	DMA AHB master index.	0 - NAHBMST-1	0
hsindex	AHB slave index.	0 - NAHBSLV-1	0
haddr	ADDR field of the AHB BAR (for PCI memory access).	0 - 16#FFF#	16#000#
hmask	MASK field of the AHB BAR.	0 - 16#FFF#	16#000#
ioaddr	ADDR field of the AHB IO BAR (for PCI configuration and PCI IO access).	0 - 16#FFF#	16#000#
pindex	APB slave index	0 - APBMAX-1	0
paddr	APB interface base address	0 - 16#FFF#	0
pmask	APB interface address mask	0 - 16#FFF#	16#FFF#
irq	Interrupt line used by the core.	0 - NAHBIRQ-1	0
irqmode	IRQ routing option: 00: PCI INTA..D, Error interrupt and DMA interrupt on the same IRQ signal 01: PCI INTA..D and Error interrupt on the same IRQ signal. DMA interrupt on IRQ+1 10: PCI INTA..D on IRQ..IRQ+3. Error interrupt and DMA interrupt on IRQ. 11: PCI INTA..D on IRQ..IRQ+3. Error interrupt on IRQ. DMA interrupt on IRQ+4	0 - 3	0
master	Enable the PCI master	0 - 1	1
target	Enable the PCI target	0 - 1	1
dma	Enable the PCI dma	0 - 1	1
tracebuffer	Enable and number of entries of the PCI trace buffer, Allowed values is 0, 32, 64, 128, ..., 16384.	0 - 16384	0
confspace	Enable the PCI Configuration Space when PCI target is disabled	0 - 1	1
vendorid	PCI vendor ID	0 - 16#FFFF#	0
deviceid	PCI device ID	0 - 16#FFFF#	0
classcode	PCI class code	0 - 16#FFFFFF#	0
revisionid	PCI revision ID	0 - 16#FF#	0
cap_pointer	Enabled and sets the offset of the first item in the Extended PCI Configuration Space	0 - 16#C0#	0
ext_cap_pointer	Offset of the first user defined item in the capability list	0 - 16#FC#	0
iobase	AHB base address of the AHB I/O area	0 - 16#FFF#	16#FFF#
extcfg	Default value of the user defined Extended PCI Configuration Space to AHB address mapping.	0 - 16#FFFFFFF#	0
bar0	Sets the default size of BAR0 in address bits.	0 - 31	0
bar1	Sets the default size of BAR1 in address bits.	0 - 31	0
bar2	Sets the default size of BAR2 in address bits.	0 - 31	0
bar3	Sets the default size of BAR3 in address bits.	0 - 31	0

*Table 772.*Configuration options

Generic name	Function	Allowed range	Default
bar4	Sets the default size of BAR4 in address bits.	0 - 31	0
bar5	Sets the default size of BAR5 in address bits.	0 - 31	0
bar0_map	Set the default PCI BAR to AHB address mapping for BAR0	0 - 16#FFFFFF#	0
bar1_map	Set the default PCI BAR to AHB address mapping for BAR1	0 - 16#FFFFFF#	0
bar2_map	Set the default PCI BAR to AHB address mapping for BAR2	0 - 16#FFFFFF#	0
bar3_map	Set the default PCI BAR to AHB address mapping for BAR3	0 - 16#FFFFFF#	0
bar4_map	Set the default PCI BAR to AHB address mapping for BAR4	0 - 16#FFFFFF#	0
bar5_map	Set the default PCI BAR to AHB address mapping for BAR5	0 - 16#FFFFFF#	0
bartype	Bit[5:0] set the reset value of the prefetch bit for the BAR. bit[n] corresponds to BARn . Bit[13:8] set the reset value of the BAR type bit for the BAR. bit[n + 8] corresponds to BARn.	0 - 16#FFFF#	0
barminsize	Sets the minimal supported BAR size in address bits. The minimal BAR size is not allowed to be smaller then the internal FIFO (or barminsize >= 2 + fifo_depth).	5 - 31	12
fifo_depth	Depth of each of the FIFOs in the data path. Depth = 2**fifo_depth.The minimal BAR size is not allowed to be smaller then the internal FIFO (or barminsize >= 2 + fifo_depth).	3 - 7	3
fifo_count	Number of FIFOs in the data path	2 - 4	2
conv_endian	Default value of the endianess conversion setting	0 - 1	1
deviceirq	Enable the device to drive the PCI INTA signal	0 - 1	1
deviceirqmask	Default value of the irq mask for the dirq input	0 - 16#F#	16#0#
hostirq	Enable the core to sample the PCI INTA-D signals to drive a AHB irq.	0 - 1	1
hostirqmask	Default value for the PCI INTA-D signals.	0 - 16#F#	16#0#
nsync	Number of synchronization registers between the two clock domains.	0 - 2	2
hostrst	Mode of the reset signal. 0: PCI reset is input only 1: The AHB reset is driven on the PCI reset when PCII.HOST is asserted 2: The AHB reset is driven on the PCI reset.	0 - 2	0
bypass	When 1, logic is implemented to bypass the pad on signals driven by the core.	0 - 1	1
ft	Enable fault-tolerance against SEU errors	0 - 1	0

*Table 772.*Configuration options

Generic name	Function	Allowed range	Default
scantest	Enable support for scan test	0 - 1	0
debug	Enables debug output signals	0 - 1	0
tbapben	Enables a separate APB interface for access of the Trace-Buffer.	0 - 1	0
tbpindex	Trace-Buffer APB slave index	0 - APBMAX-1	0
tbpaddr	Trace-Buffer APB interface base address	0 - 16#FFF#	0
tbmask	Trace-Buffer APB interface address mask	0 - 16#FFF#	16#FFF#
netlist	Enables a netlist implementation of the logic controlled by the PCI bus signals (GRPCI2_PHY).	0 - 1	0
masters	Controls which AHB masters belongs to PCI function0	0 - 16#FFFF#	16#FFFF#
multifunc	Enables Multi-Function support	0 - 1	0
multiint	Enables support to drive all PCI interrupt signalsINTA...D	0 - 1	0
mf1_deviceid	PCI device ID (PCI function1)	0 - 16#FFFF#	0
mf1_classcode	PCI class code (PCI function1)	0 - 16#FFFFFF#	0
mf1_revisionid	PCI revision ID (PCI function1)	0 - 16#FF#	0
mf1_bar0	Sets the default size of BAR0 in address bits. (PCI function1)	0 - 31	0
mf1_bar1	Sets the default size of BAR1 in address bits. (PCI function1)	0 - 31	0
mf1_bar2	Sets the default size of BAR2 in address bits. (PCI function1)	0 - 31	0
mf1_bar3	Sets the default size of BAR3 in address bits. (PCI function1)	0 - 31	0
mf1_bar4	Sets the default size of BAR4 in address bits. (PCI function1)	0 - 31	0
mf1_bar5	Sets the default size of BAR5 in address bits. (PCI function1)	0 - 31	0
mf1_bartype	Bit[5:0] set the reset value of the prefetch bit for the BAR. bit[n] corresponds to BARn . Bit[13:8] set the reset value of the BAR type bit for the BAR. bit[n + 8] corresponds to BARn.	0 - 16#FFFF#	0
mf1_bar0_map	Set the default PCI BAR to AHB address mapping for BAR0 (PCI function1)	0 - 16#FFFFFF#	0
mf1_bar1_map	Set the default PCI BAR to AHB address mapping for BAR1 (PCI function1)	0 - 16#FFFFFF#	0
mf1_bar2_map	Set the default PCI BAR to AHB address mapping for BAR2 (PCI function1)	0 - 16#FFFFFF#	0
mf1_bar3_map	Set the default PCI BAR to AHB address mapping for BAR3 (PCI function1)	0 - 16#FFFFFF#	0
mf1_bar4_map	Set the default PCI BAR to AHB address mapping for BAR4 (PCI function1)	0 - 16#FFFFFF#	0
mf1_bar5_map	Set the default PCI BAR to AHB address mapping for BAR5 (PCI function1)	0 - 16#FFFFFF#	0
mf1_cap_pointer	Enabled and sets the offset of the first item in the Extended PCI Configuration Space (PCI function1)	0 - 16#C0#	0
mf1_ext_-cap_pointer	Offset of the first user defined item in the capability list (PCI function1)	0 - 16#FC#	0

*Table 772.*Configuration options

Generic name	Function	Allowed range	Default
mf1_extcfg	Default value of the user defined Extended PCI Configuration Space to AHB address mapping. (PCI function1)	0 - 16#FFFFFFF#	0
mf1_masters	Controls which AHB masters belongs to PCI function1	0 - 16#FFFF#	16#0000#

52.13 Signal descriptions

Table 773 shows the interface signals of the core (VHDL ports).

*Table 773.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
PCICLK	N/A	Input	PCI Clock	-
AHBSI	*1	Input	AHB slave input signals	-
AHBSO	*1	Output	AHB slave output signals	-
AHBMI	*1	Input	AHB master input signals	-
AHBMO	*1	Output	AHB master output signals	-
AHBDMI	*1	Input	DMA AHB master input signals	-
AHBDMO	*1	Output	DMA AHB master output signals	-
APBI	*1	Input	APB slave input signals	-
APBO	*1	Output	APB slave output signals	-
PCII	*2	Input	PCI input signals	-
PCIO	*2	Output	PCI output signals	-
DIRQ		Input	Interrupt signals	High
TBAPBI	*1,*3	Input	Trace-Buffer APB slave input signals	-
TBAPBO	*1, *3	Output	Trace-Buffer APB slave output signals	-
PTARST	N/A, *3	Output	PCI reset to AMBA reset output signal	Low
DEBUG	N/A, *3	Output	Debug signals	-

*1) see GRLIB IP Library User's Manual.
*2) see PCI Local Bus Specification
*3) Can be left unconnected, if not used.

The PCII.HOST signal selects of the core should operate as a system host or peripheral device.

52.14 Library dependencies

Table 774 shows the libraries used when instantiating the core (VHDL libraries).

*Table 774.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	PCI	Component	Component declaration

52.15 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
```

```
use ieee.std_logic_1164.all;
library grlib;
use grlib.amba.all;
use grlib.stdlib.all;
use grlib.tech.all;
library gaisler;
use gaisler.pci.all;

.
.
signal apbi : apb_slv_in_type;
signal apbo : apb_slv_out_type;
signal ahbsi : ahb_slv_in_type;
signal ahbso : ahb_slv_out_vector;
signal ahbmi : ahb_mst_in_type;
signal ahbmo : ahb_mst_out_vector;

signal pcii : pci_in_type;
signal pcio : pci_out_type;

begin

pci0 : grpci2
generic map (
 memtech => memtech,
 oepol => OEPOL,
 hmindex => CFG_NCPU+CFG_AHB_UART+CFG_AHB_JTAG,
 hdmindex => CFG_NCPU+CFG_AHB_UART+CFG_AHB_JTAG+1,
 hsindex => 4,
 haddr => 16#c00#,
 hmask => 16#f00#,
 ioaddr => 16#000#,
 pindex => 4,
 paddr => 4,
 irq => 0,
 irqmode => 0,
 master => CFG_GRPCI2_MASTER,
 target => CFG_GRPCI2_TARGET,
 dma => CFG_GRPCI2_DMA,
 tracebuffer => CFG_GRPCI2_TRACE,
 vendorid => CFG_GRPCI2_VID,
 deviceid => CFG_GRPCI2_DID,
 classcode => CFG_GRPCI2_CLASS,
 revisionid => CFG_GRPCI2_RID,
 cap_pointer => CFG_GRPCI2_CAP,
 ext_cap_pointer => CFG_GRPCI2_NCAP,
 iobase => CFG_AHBIO,
 extcfg => CFG_GRPCI2_EXTCFG,
 bar0 => CFG_GRPCI2_BAR0,
 bar1 => CFG_GRPCI2_BAR1,
 bar2 => CFG_GRPCI2_BAR2,
 bar3 => CFG_GRPCI2_BAR3,
 bar4 => CFG_GRPCI2_BAR4,
 bar5 => CFG_GRPCI2_BAR5,
 fifo_depth => log2(CFG_GRPCI2_FDEPTH),
 fifo_count => CFG_GRPCI2_FCOUNT,
 conv_endian => CFG_GRPCI2_ENDIAN,
 deviceirq => CFG_GRPCI2_DEVINT,
 deviceirqmask => CFG_GRPCI2_DEVINTMSK,
 hostirq => CFG_GRPCI2_HOSTINT,
 hostirqmask => CFG_GRPCI2_HOSTINTMSK,
 nsync => 2,
 hostrst => 2,
 bypass => CFG_GRPCI2_BYPASS)
port map (
 rstn,
 clkm,
 pciclk,
 gnd(3 downto 0),
 pcii,
 pcio,
```

```
 apbi,
 apbo(4),
 ahbsi,
 ahbso(4),
 ahbmi,
 ahbmo(CFG_NCPU+CFG_AHB_UART+CFG_AHB_JTAG),
 ahbdmi,
 ahbmo(CFG_NCPU+CFG_AHB_UART+CFG_AHB_JTAG+1);

pcipads0 : pcipads generic map (padtech => padtech, host => 1, oepol => OEPOL,
                                noreset => 0, drivereset => 1)  -- PCI pads
    port map ( pci_rst, pci_gnt, pci_idsel, pci_lock, pci_ad, pci_cbe,
      pci_frame, pci_irdy, pci_trdy, pci_devsel, pci_stop, pci_perr,
      pci_par, pci_req, pci_serr, pci_host, pci_66, pcii, pcio );
;
```

53 GRPULSE - General Purpose Input Output

53.1 Overview

The General Purpose Input Output interface is assumed to operate in an AMBA bus system where the APB bus is present. The AMBA APB bus is used for control and status handling.

The General Purpose Input Output interface provides a configurable number of channels. Each channel is individually programmed as input or output. Additionally, a configurable number of the channels are also programmable as pulse command outputs. The default reset configuration for each channel is as input. The default reset value each channel is logical zero.

The pulse command outputs have a common counter for establishing the pulse command length. The pulse command length defines the logical one (active) part of the pulse. It is possible to select which of the channels shall generate a pulse command. The pulse command outputs are generated simultaneously in phase with each other, and with the same length (or duration). It is not possible to generate pulse commands out of phase with each other.

Each channel can generate a separate internal interrupt. Each interrupt is individually programmed as enabled or disabled, as active high or active low level sensitive, or as rising edge or falling edge sensitive.

53.1.1 Function

The core implements the following functions:

- Input
- Output
- Output pulse commands
- Input interrupts
- Status and monitoring

53.1.2 Interfaces

The core provides the following external and internal interfaces:

- Discrete input and output interface
- AMBA APB slave interface, with sideband signals as per [GRLIB] including:
- interrupt bus
- configuration information
- diagnostic information

53.2 Registers

The core is programmed through registers mapped into APB address space.

*Table 775.*GRPULSE registers

APB address offset	Register
0x00	Input Register
0x04	Output Register
0x08	Direction Register
0x0C	Interrupt Mask Register
0x10	Interrupt Polarity Register
0x14	Interrupt Edge Register
0x18	Pulse Register
0x1C	Pulse Counter Register

53.2.1 Input Register

*Table 776.*0x00 - GPIOIN - Input Register

31 24	23 0
RESERVED	IN
0	*
r	r

23-0: IN Input Data

Note that only bits nchannel-1 to 0 are implemented.

53.2.2 Output Register

*Table 777.*0x04 - GPIOOUT - Output Register

31 24	23 0
RESERVED	OUT
0	0
r	r

23: 0 OUT Output Data

All bits are cleared to 0 at reset.

Note that only bits nchannel-1 to 0 are implemented.

53.2.3 Direction Register

*Table 778.*0x08 - GPIODIR - Direction Register

31 24	23 0
RESERVED	DIR
0	0
r	rw

23: 0 DIR Direction:
0b=input,
1b=output

All bits are cleared to 0 at reset.

Note that only bits nchannel-1 to 0 are implemented.

53.2.4 Pulse Register

*Table 779.*0x18 - GPIOPULSE - Pulse Register

31 24	23 0
RESERVED	PULSE
0	0
r	rw

23-0: PULSE Pulse enable:
0b=output,
1b=pulse command output

All bits are cleared to 0 at reset.

Only channels configured as outputs are possible to enable as command pulse outputs.

Note that only bits npulse-1 to 0 are implemented.

53.2.5 Pulse Counter Register

*Table 780.*0x1C - GPIONTR - Pulse Counter Register

31 24	23 0
RESERVED	CNTR
0	0
r	rw

23-0: CNTR Pulse counter value

The pulse counter is decremented each clock period, and does not wrap after reaching zero.

Command pulse channels, with the corresponding output data and pulse enable bits set, are (asserted) while the pulse counter is greater than zero.

Setting CNTR to 0 does not give a pulse.

Setting CNTR to 1 does give a pulse with of 1 Clk period.

Setting CNTR to 255 does give a pulse with of 255 Clk periods.

Note that only bits cntrwidth-1 to 0 need be implemented.

53.2.6 Interrupt Mask Register

*Table 781.*0x0C - GPIOMASK - Interrupt Mask Register

31 24	23 16	15 0
RESERVED	MASK	RESERVED
0	0	0
r	rw	r

23-16: MASK Interrupt enable, 0b=disable, 1b=enable

Note that only bits that are enabled by the imask VHDL generic and that are in the range nchannel-1 to 0 are implemented.

53.2.7 Interrupt Polarity Register

*Table 782.*0x10 - GPIOPOL - Interrupt Polarity Register

31 24	23 16	15 0
RESERVED	POL	RESERVED
0	0	0
r	rw	r

23-16: POL Interrupt polarity, 0b=active low or falling edge, 1b=active high or rising edge

Note that only bits that are enabled by the imask VHDL generic and that are in the range nchannel-1 to 0 are implemented.

53.2.8 Interrupt Edge Register

*Table 783.*0x14 - GPIOEDGE - Interrupt Edge Register

31 24	23 16	15 0
RESERVED	EDGE	RESERVED
0	0	0
r	rw	r

23-16: EDGE Interrupt edge or level, 0b=level, 1b=edge

Note that only bits that are enabled by the imask VHDL generic and that are in the range nchannel-1 to 0 are implemented.

53.3 Operation

53.3.1 Interrupt

Two interrupts are implemented by the interface:

Index:Name:Description:

0 PULSEPulse command completed

31:0 IRQ Filtered input interrupt

The PULSE interrupt is configured by means of the *pirq* VHDL generic.

The IRQ interrupts are configured by means of the *imask* and *ioffset* VHDL generics, where *imask* enables individually the input interrupts, and *ioffset* adds an offset to the resulting index on the interrupt bus.

53.3.2 Reset

After a reset the values of the output signals are as follows:

Signal:Value after reset:

GPIOO.Dout[31:0]de-asserted

GPIOO.OEn[31:0]de-asserted

53.3.3 Asynchronous interfaces

The following input signals are synchronized to Clk:

- GPIOI.Din[31:0]

53.4 Vendor and device identifiers

The module has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x037. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

53.5 Implementation

53.5.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support *grlib_async_reset_enable*. See also the description for the *syncrst* VHDL generic for how the core implements reset.

53.6 Configuration options

Table 784 shows the configuration options of the core (VHDL generics).

*Table 784.*Configuration options

Generic name	Function	Allowed range	Default
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	Addr field of the APB bar.	0 - 16#FFF#	0
pmask	Mask field of the APB bar.	0 - 16#FFF#	16#FFF#
pirq	Interrupt line used by the GRPULSE.	0 - NAHBIRQ-1	1
nchannel	Number of input/outputs	1 - 32	24
npulse	Number of pulses	1 - 32	8
imask	Interrupt mask	0 - 16#FFFFFFFF#	16#FF00#
ioffset	Interrupt offset	0-32	8
invertpulse	Invert pulse output when set	1 - 32	0
cntrwidth	Pulse counter width	4 to 32	20
syncrst	Use synchronous reset 0: Core makes use of synchronous reset only 1: Output registers and registers controlling output enable are implemented with asynchronous reset.	0, 1	0
oepol	Output enable polarity	0, 1	1

53.7 Signal descriptions

Table 785 shows the interface signals of the core (VHDL ports).

*Table 785.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
GPIOI	*	Input		-
GPIOO	*	Output		-

* see GRLIB IP Library User's Manual

53.8 Signal definitions and reset values

The signals and their reset values are described in table 786.

*Table 786.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
gpio[]	Input/Output	General purpose input output	-	Tri-state

53.9 Timing

The timing waveforms and timing parameters are shown in figure 141 and are defined in table 787.

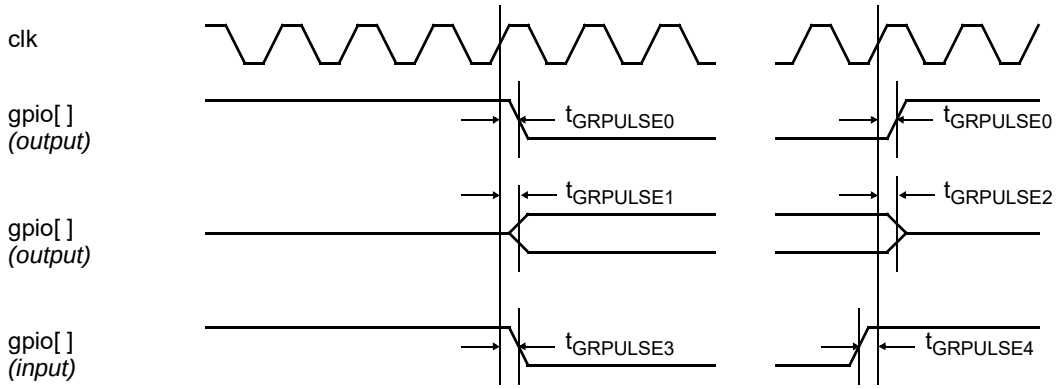


Figure 141. Timing waveforms

*Table 787.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{GRPULSE0}$	clock to output delay	rising *clk* edge	-	TBD	ns
$t_{GRPULSE1}$	clock to non-tri-state delay	rising *clk* edge	TBD	-	ns
$t_{GRPULSE2}$	clock to tri-state delay	rising *clk* edge	-	TBD	ns
$t_{GRPULSE3}$	input to clock hold	rising *clk* edge	TBD	-	ns
$t_{GRPULSE4}$	input to clock setup	rising *clk* edge	TBD	-	ns

53.10 Library dependencies

Table 788 shows the libraries used when instantiating the core (VHDL libraries).

*Table 788.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	MISC	Signals, Components	Signal and component declarations

53.11 Instantiation

This example shows how the core can be instantiated.

TBD

54 GRPWM - Pulse Width Modulation Generator

54.1 Overview

GRPWM is a pulse width modulation (PWM) generator that supports several outputs, with different frequencies. The core is configured through a set of APB registers, described in section 54.3. The core supports both asymmetric and symmetric PWM generation. Each of the PWM outputs can be configured to be either a single PWM signal or a pair of PWM signals (where the two signals are each others' inverse), with configurable amount of dead band time in between them. The core also supports programming of the output polarity, setting the outputs to fixed values, and configurable interrupt schemes. Hardware support to simplify the generation of a PWM signal that emulate an arbitrary repetitive waveform is also included.

54.2 Operation

54.2.1 System clock scaling

In order to support a wide range of system clock and PWM frequencies the core includes programmable clock scalers. Each scaler is clocked by the system clock and decrement on each clock cycle. When a scaler underflows it is reloaded with the value of its reload register and a tick is generated. This tick can then be used to increment (or decrement) one or more PWM counters. The reload value(s) of the scaler(s) can be read and written through the APB register called *Scaler reload register*, described in section 54.3. The number of system clock scalers is configurable through the VHDL generic *nscalers* and the width of the scaler(s) is determined by the VHDL generic *sbits*.

54.2.2 Asymmetric and symmetric PWM generation

An asymmetric PWM is a pulse signal that is inactive at the beginning of its period and after a certain amount of time goes active, and then stays active for the rest of the period. A symmetric PWM is a pulse signal that is inactive for a certain amount of time at the beginning of the period and a certain amount of time at the end of the period, and stays active in between. The two inactive time periods are normally, but not necessarily, equally long.

For the core to generate a PWM, independent of whether asymmetric or symmetric method is used, software need to do the following (also see section 54.3 for more detailed description of register interface):

- Enable the core by writing the *en* bit in *Core control register*.
- Configure the scaler (see section 54.2.1) and set the PWM period in the *PWM period register*.
- Write the *PWM compare register* with the value at which the PWM's counter should match and switch the outputs.
- If dead band time should be generated, write the value at which the current PWM's dead band time counter should match to the *PWM dead band compare register*. Also set the *dben* bit in the *PWM control register* to 1. See section 54.2.4 for information on dead band time.
- Set the meth bit in PWM control register to either asymmetric och symmetric.
- Set the polarity of the PWM output be setting the *pol* bit in the *PWM control register*.
- If the PWM output should be paired with its inverse then set the *pair* bit in the *PWM control register* to 1, otherwise set it to 0. Note that each PWM always has two ouputs, but if the *pair* bit is set to 0 then the second output is constantly inactive or 0 when the *PWM control register* bit pz is set to 1.
- Program the interrupt, see section 54.2.5.
- Enable the PWM generation by writing the *en* bit in *PWM control register* to 1.

- If software wants the PWM output(s) to assume fix value(s) it can write the *fix* bits in the PWM *control register* appropriately.

Specific configuration required for symmetric PWM if dual compare mode should be used:

- If the core should update the PWM's compare register twice every PWM period, then set the *dcomp* bit in the *PWM control register* to a 1.
- If the *dcomp* bit in the *PWM control register* is set, and it is desired that the two inactive time periods are not of equal length, software needs to continuously update the *PWM compare register* with new values. Since the core updates its internal register at the start of and middle of the PWM period, software need to update the *PWM compare register* sometime during the first half of the period.

Note that the core's internal period register is updated from the *PWM period register* at the start of every period, both for asymmetric and symmetric PWM generation.

54.2.3 Waveform PWM generation

That, which in this document is referred to as a *waveform PWM* is not a PWM generated in a different way than the asymmetric or symmetric methods described above. In fact a waveform PWM is either generated asymmetrically or symmetrically. The difference is that when the compare registers are loaded with new values they are read from an internal RAM instead of the *PWM compare register*. The advantage with this is that if software wants to, for example, generate a PWM signals that emulates a sine wave, it can load a number of compare values into the RAM before starting the PWM generation. Once started, the core will read the RAM, increasing the address at every compare match, and generate the same pattern over and over without the need for software intervention. Note that any pattern that is loaded into the RAM is generated, the core is not limited to a sine wave. This feature is supported if the *wpwm* bit in *Capability register 2* is set to 1. The core only support one waveform PWM and it is always the PWM with the highest index. The index is determined by the VHDL generic *npwm*. If for example *npwm* = 4, then it is only PWM four that can be put in waveform mode. For details on how to configure the waveform mode and read/write the RAM please see the description of the *Waveform configuration register*, *Waveform RAM, word X* registers, and *PWM control register* in section 54.3.

54.2.4 Dead band time

It is often desired to have a delay between when one of the PWM signals of a PWM pair goes inactive and when the other signal goes active. This delay is called dead band time. By default the core does not generate any dead band time, but can be configured to do so by setting the *dben* bit in the *PWM control register* to 0b1. When dead band time is enabled the core will start a counter each time a PWM pair switch its outputs. The output going inactive is not delayed while the output going active is delayed until the counter matches the value in the *PWM dead band compare register*. To support a wide range of applications the amount of dead band time inserted is programmable. The number of bits used in the *PWM dead band compare register* is configurable through the VHDL generic *dbbits*, and also a four bit system clock scaler can be enabled for each PWM's dead band counter by setting the *dbscaler* VHDL generic to 1.

54.2.5 Interrupts

Interrupts can programmed individually for each PWM to be generated at PWM compare match, at PWM period match, or not generated at all. This is programmed in each PWM's *PWM control register.* Each PWM also has a 6-bit interrupt counter that can be used to scale down the frequency at which the interrupts occur. When an interrupt is generated the bit in the *Interrupt pending register* for the PWM in question is set. The bits in the *Interrupt pending register* stay set until software clears them by writing 1 to them. Through the *sepirq* and *npwm* VHDL generics the core supports several different interrupt numbers, this is described in section *54.6*.

When an interrupt is generated, or when the interrupt scaler counter is increased, an output tick is generated on the core's *tick* output signal. The output tick bit has the same index as the PWM in question.

54.3 Registers

The core is programmed through registers mapped into APB address space.

*Table 789.*GRPWM registers

APB address offset	Register
0x00	Core control register
0x04	Scaler reload register
0x08	Interrupt pending register
0x0C	Capability register 1
0x10	Capability register 2
0x14*	Waveform configuration registers
0x18 - 0x1C	Reserved, always zero.
0x20**	PWM period register
0x24**	PWM compare register
0x28**	PWM dead band compare register
0x2C**	PWM control register
0x8000***	Waveform RAM, word 0
0x8004***	Waveform RAM, word 1
...	...
0xFFFC***	Waveform RAM, word 8191

* This register is only implemented if the wpwm bit (bit 0) in *Capability register 2* is set to 1.

** This register is implemented once for every PWM (value of *npwm* VHDL generic decides the number of registers), with an offset of 0x10 from the previous PWM's register. The functionality is the same for each PWM.

*** The implementation of this register depends on if the *wpwm* bit (bit 0) in *Capability register 2* is set to 1 and if the waveform RAM is large enough (the value of the field *wabits* in *Capability register 2* reports the number of address bits - 1 that is used for the waveform RAM).

54.3.1 Core Control Register

*Table 790.*0x00 - CTRL - Core control register

31 x+13	x+12 12	11	10 8	7 1	0
R	noup	R	scalersel	R	en
0	0	0	0	0	0
r	rw	r	rw	r	rw

31:x+13 Reserved, always zero. x is the value of bits 2:0 in *Capability register 1*

12+x:12 No update bits for each PWM. x is the value of bits 2:0 in *Capability register 1*. Bit 12 is for the first PWM, bit 13 for the second etc. If a bit is set to 0b1 then that PWM's internal period register, compare register, and dead band compare registers are not updated from the corresponding APB registers. These bits can be used by software if it wants to change more than one of the values and it is required that all values change in the same PWM period. It can also be used to synhronize the use of new values for different PWMs. Reset value 0b0..0.

11 Reserved, always zero.

10:8 System clock scaler select bits. These bits determine which of the implemented system clock scalers' reload value that can be read/written from the *Scaler reload register*.These bits are only present if the *nscalers* generic is greater than 1. Reset value is 0b000

7:1 Reserved, always zero.

0 Core enable bit. 0b0 = Core is disabled, no operations are performed and all outputs are disabled. 0b1 = Core is enabled, PWM outputs can be generated. Reset value is 0b0.

54.3.2 Scaler Reload Register

*Table 791.*0x04 - SCALER - Scaler reload register

31 sbits	sbits-1 0
R	reload
0	all 1
r	rw

31:sbits Reserved, always zero. If sbits = 32 then this field is not present. (sbits is the value of the *sbits* generic)

(sbits-1):0 The value of this field is used to reload the system clock scaler when it underflows. If the core is configured with more than one scaler (*nscalers* generic greater than 1) then the *scalersel* bits in the *Core control register* determine which of the scalers that is read/written. Reset value is 0b1..1 (all ones).

54.3.3 Interrupt Pending Register

*Table 792.*0x08 - IPEND - Interrupt pending register

31 npwm	npwm-1 0
R	irq pending
0	0
r	wc

31:npwm Reserved, always zero.

(npwm-1):0 Interrup pending bits for the PWM(s). When an interrupt event for a specific PWM occurs the core sets the corresponding bit in the interrupt pending register and generates an interrupt. Software can read this register to see which PWM that generated the interrupt.

54.3.4 Capability Register 1

*Table 793.*0x0C - CAP1 - Capability register 1

31 29	28	27	26 25	24	23	22	21	20 16	15 13	12 8	7 3	2 0
R	def-pol	dcm ode	sepirq	R	sym pwm	asyp wm	dbsc aler	dbbits	nscalers	sbits	pbits	npwm
0	*	*	*	0	*	*	*	*	*	*	*	*
r	r	r	r	r	r	r	r	r	r	r	r	r

31:29 Reserved, always zero.

28 0 = Default polarity is active low (outputs are high after reset/power-up). 1 = Default polarity is active high (outputs are low after reset/power-up).

27 0 = Dual compare mode not implemented. 1 = Dual compare mode implemented.

26:25 Reports interrupt configuration. Value of *sepirq* VHDL generic. Read only.

24 Reserved, always zero.

23 0 = Symmetric PWM generation is not implemented. 1 = Symmetric PWM generation is implemented. Value of *sympwm* VHDL generic. Read only.

22 0 = Asymmetric PWM generation is not implemented. 1 = Asymmetric PWM generation is implemented. Value of *asympwm* VHDL generic. Read only.

21 0 = Dead band time scaler(s) is not implemented. 1 = Dead band time scaler(s) is implemented. Value of *dbscaler* VHDL generic. Read only.

20:16 Reports number of bits, -1, for the PWM's dead band time counters. Value of the *dbbits* VHDL generic - 1. Read only.

15:13 Reports number of implemented scalers, -1. Value of the *nscalers* VHDL generic - 1. Read only.

12:8 Reports number of bits for the scalers, -1. Value of the *sbits* VHDL generic - 1. Read only.

7:3 Reports number of bits for the PWM counters, -1. Value of the *pbits* VHDL generic - 1. Read only.

2:0 Reports number of implemented PWMs. Value of the *npwm* VHDL generic - 1. Read only.

54.3.5 Capability Register 2

*Table 794.*0x10 - CAP2 - Capability register 2

31 11	10	9 6	5 1	0
R	wsync	wabits	wdbits	wpwm
0	*	*	*	*
r	r	r	r	r

31:11 Reserved, always zero

10 1 if Waveform PWM synch signal generation is implemented, 0 if not. Value of VHDL generic *wsync*. Read only

9:6 Reports the number of address bits - 1 used for the waveform RAM. Value is log2(*wdepth*) - 1, where *wdepth* is the VHDL generic *wdepth*. Read only.

5:1 Reports number of bits -1 for each word in the waveform RAM. Value of VHDL generic *wbits* - 1. Read only

0 1 if waveform PWM generation is implemented, 0 if not. Value of VHDL generic *wavepwm*. Read only

54.3.6 Waveform Configuration Register

*Table 795.*0x14 - WCFG - Waveform configuration register

31	30	29	28	wabits +17	wabits +16	16	15	wabits +1	wabits	0
wsynccfg		wsen	R		wsynccomp		R		wstopaddr	
0		0	0		0		0		all 1	
rw		rw	r		rw		r		rw	

31:30 These bits are used to configure at which point in the PWM period matching the *wsynccomp* field (see description below) that the *wsync* ouput will be set high. 0b00 = The wsync ouput will be set at the start of the PWM period. 0b01 = The output will be set at the first compare match. 0b10 = If the *meth* bit in the *PWM Control Register* is set to one (symmetric) for the waveform PWM, then the output will be set at the middle of the PWM period. 0b11 = If the *meth* bit is set to one for the waveform PWM, then the output will be set at the second compare match.

29 Enables/disables the waveform sync signal. This bit is only present if the *wsync* bit in *Capability register 2* is set to 1. Reset value is 0b0

28:wabits+17 Reserved, always zero. wabits is the value of the *wabits* field in *Capability register 2*. Note that this field is not present if wabits is 12.

16+wabits:16 wabits is the value of the *wabits* field in *Capability register 2*. The number of words in the waveform RAM is the same as the maximum number of PWM periods that will occur before the waveform is restarted. The value of this field is used as an offset into the waveform PWM. A counter is increased every PWM period and when the counter matches this value the *wsync* output of the core will be set to 1 sometime during that period. These bits are only present if the *wsync* bit in *Capability register 2* is set to 1. Reset value is 0b0..0.

15:wabits+1 Reserved, always zero.

wabits:0 The value of this field is used by the core to wrap when accessing the waveform RAM. wabits is the value of the *wabits* field in *Capability register 2*. This field is reset to 0b1..1 (all ones) so that by default the core reads the whole RAM. If software wants to put a waveform in the RAM that does not fill the whole RAM it should set these bits to the address where the last waveform PWM compare value will be stored.

54.3.7 PWM Period Register

*Table 796.*0x20 - PPERIOD - PWM period register

31	pbits	pbits-1	0
R		per	
0		0	
r		rw	

31:pbits Reserved, always zero. If pbits = 32 then this field is not present. (pbits is the value of the *pbits* generic)

(pbits-1):0 When the PWM counter reaches this value a PWM period has passed. Depending on the method used to generate the PWM the output could then be switched. When this register is written the actual PWM period value used inside the core is not updated immediately, instead a shadow register is used to hold the new value until a new PWM period starts. Reset value 0b0..0 (all zeroes).

54.3.8 PWM Compare Register

*Table 797.*0x24 - PCOMP - PWM compare register

31 pbits	pbits-1 0
R	comp
0	0
r	rw

31:pbits Reserved, always zero. If pbits = 32 then this field is not present. (pbits is the value of the *pbits* generic)

(pbits-1):0 When the PWM counter reaches this value the PWM output is switched. Depending on the method used to generate the PWM this register is used once or twice during each PWM period. When this register is written the actual PWM compare value used inside the core is not updated immediately, instead a shadow register is used to hold the new value until a new PWM period starts. Reset value 0b0..0 (all zeroes).

54.3.9 PWM Dead Band Compare Register

*Table 798.*0x28 - PDEAD - PWM dead band compare register

31 dbbits	dbbits-1 0
R	dbcomp
0	0
r	rw

31:dbbits Reserved, always zero. If dbbits = 32 then this field is not present. (dbbits is the value of the *dbbits* generic)

(dbbits-1):0 The dead band time has passed once the dead band counter reach the value of this field. When this register is written the actual compare value used inside the core is not updated immediately, instead a shadow register is used to hold the new value until a new PWM period starts. Reset value 0b0..0 (all zeroes).

54.3.10 PWM Control Register

*Table 799.*0x2C - PCTRL - PWM control register

31 27	26	25 22	21	20 15	14	13	12 10	9	8	7	6	5 3	2	1	0
R	flip	dbscaler	dben	irqscaler	irqt	irqen	scalersel	wen	dcen	pz	meth	fix	pair	pol	en
0	0	0	0	0	0	0	0	0	0	0	*	0	1	*	0
r	rw	rw	rw	rw	rw	rw	rw	rw*	rw*	r	rw	rw	rw	rw	rw

31:27 Reserved, always zero.

26 Output flip bit. When this bit is set to 0b1 the PWM outputs are flipped.

25:22 Dead band scaler. These bits are used to scale the system clock when generating dead band time. This field is only present if the *dbscaler* generic is set to 1. When these bits are written the dead band scaler register inside the core is not updated immediately. Instead these bits are written to a reload register which updates the actual scaler when it underflows. This is done in order to prevent the dead band scaler register to change during the actual dead band time. Reset value is 0b0..0 (all zeroes).

21 Dead band enable. 0b0 = Dead band time generation is disabled, no dead band time will be inserted when the PWM output switch from deactive to active. 0b1 = Dead band time will be inserted when the PWM output switch from deactive to active. Reset value is 0b0.

20:15 Interrupt scaler. Determines how many compare/period matches that need to occur before an interrupt is generated. All zeroes means that an interrupt will occur every compare/period match, a one means that an interrupt will occur every second match etc. Note that when generating a symmetric PWM two compare matches occur during a PWM period but when generating an asymmetric PWM only one compare match occur during a period. Reset value is 0b0..0 (all zeroes).

14 Interrupt type. 0b0 = Generate interrupt on PWM period match. 0b1 = Generate interrupt on PWM compare match. Reset value is 0b0.

13 Interrupt enable/disable bit. 0b0 = Interrupt is disabled. 0b1 = Interrupt is enabled. Reset value is 0b0.

*Table 799.*0x2C - PCTRL - PWM control register

12:10	Scaler select bits. These bits are used to select which of the system clock scalers that will be used when generating the current PWM. This field is only present when the *nscalers* generic is greater than 1. These bits can only be set if the PWM is disabled, i.e. *en* bit (see below) set to 0b0. Reset value is 0b000.
9	Waveform PWM enable. This bit can only be set if the current PWM is the PWM with the highest index (determined by the generic *npwm*) and if the *wavepwm* field in *Capability register 2* is set to 1. Also the PWM need to be disabled, i.e. *en* bit (see below) set to 0b0. When this bit is set the core will reload the internal PWM compare registers with values from the waveform RAM instead of values from the *PWM compare register*. Reset value is 0b0.
8	Dual compare mode enable. If this bit is set to 0b1 and the *meth* bit (see below) is set to 0b1 (symmetric) then the core will update its internal PWM compare register twice every PWM period, once when the counter is zero and once when a period match occur and the counter starts counting downwards again. In this way it is possible to have two different compare values, one when counter is counting upwards and one when counter is counting downwards. If this bit is 0b0 the compare register is only updated when the counter is zero. This bit has no effect if an asymmetric PWM is generated. Reset value is 0b0. This bit is only present if the *dcmode* bit in the *Capability register* is set.
7	When this pair_zero bit is set to 0b1 and the pair bit is set to 0b0 the complement output is always set to zero. When this bit is set to 0b0 and the pair bit is set to 0b0 the complement output is inactive (depending on the polarity). When the pair bit is set to 0b1, this bit has no function.
6	PWM generation method select bit. This bit selects if an asymmetric or symmetric PWM will be generated, where 0b0 = asymmetric and 0b1 = symmetric. . The asymmetric and symmetric methods are only available if the generics *asympwm* and *sympwm* respectively are set to 1. This bit can only be set if the PWM is disabled, i.e. *en* bit (see below) set to 0b0. The core prevents software from setting this bit to an invalid value. Reset value is 0b0 if asymmetric PWM is supported otherwise 0b1.
5:3	PWM fix value select bits. These bits can be used to set the PWM output to a fix value. If bit 3 is set to 0b1 then bit 4 decides what value the PWM output will have. If the *pair* bit (see below) is set to 0b1 while bit 3 is set to 0b1 as well then bit 5 determines what value the complement output will have. Reset value is 0b000.
2	PWM pair bit. If this bit is set to 0b1 a complement output for this PWM will be generated, creating a PWM pair instead of a single PWM. The complement output will be the first ouput's inverse, with the exception that dead band time might be added when the values switch from deactive to active. Reset value is 0b1.
1	PWM polarity select bit. 0b0 = PWM is active low, 0b1 = PWM is active high. This bit can only be set if the PWM is disabled, i.e. *en* bit (see below) set to 0b0. Reset value equals *defpol* bit in *Capability Register 1*.
0	PWM enable/disable bit. 0b0 = PWM is disabled. 0b1 = PWM is enabled. When this bit is set to 1 (from 0) and the *wen* bit (see bit 9 above) is set the core's internal address counter for the waveform RAM is reset. Reset value is 0b0.

54.3.11 Waveform RAM, Word X

*Table 800.*0x8000 - 0xFFFC - Waveform RAM, word X

31 wbits+1	wbits 0
R	waveform data
0	NR
r	rw

31:wbits+1	Reserved, always zero. wbits is the value of the *wdbits* field in *Capability register 2*. Note that this field is not present if wbits = 31.
wbits:0	wbits is the value of the wdbits field in *Capability register 2*. Data in the waveform RAM at the address which the current register maps to can be read/written through these bits. This register can only be read/written if either the *wen* bit or *en* bit in the associated PWM's PWM control register are set to 0.

54.4 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x04A. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

54.5 Implementation

54.5.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support *grlib_async_reset_enable*. The registers driving PWM output are always implemented with asynchronous reset.

54.5.2 RAM usage

The core maps all usage of RAM on the *syncram* (or *syncramft* if *ft* generic is not set to 0) component from the technology mapping library (TECHMAP). RAM is only used if the core is configured with support for generation of a waveform PWM (*wavepwm* generic set to 1). The size of the instantiated RAM is determined by the *wbits* and *wdepth* generics. *wdepth* is the number of words that the RAM can hold, and *wbits* is the number of bits in each word. Fault tolerance - byte parity DMR or TMR - can be added to the RAM by setting the *ft* generic to 1 or 2. Note that the *ft* generic need to be set to 0 if the core is used together with the GPL version of GRLIB, since that version does not support any fault tolerance.

54.6 Configuration options

Table 801 shows the configuration options of the core (VHDL generics).

*Table 801.*Configuration options

Generic name	Function	Allowed range	Default
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	ADDR field of the APB BAR.	0 - 16#FFF#	0
pmask	MASK field of the APB BAR. Need to be set to 16#F00# or smaller if the generic *wavepwm* is set to 1.	0 - 16#FFF#	16#F00#
pirq	APB irq number.	0 - NAHBIRQ-1	0
memtech	Memory technology used for waveform buffer. This generic has no impact if *wavepwm* is 0.	0 - NTECH	inferred
npwm	Number of PWM outputs.	1 - 8	3
pbits	Number of bits used for each PWM.	1 - 32	16
sbits	Number of bits in the system clock scaler(s).	1 - 32	16
nscalers	Number of system clock scalers.	1 - 8	1
dbbits	Number of bits used for the dead band configuration for each PWM.	1 - 32	8
dbscaler	Decides if a scaler is implemeted for the dead band configuration for each PWM. 1 = A four bit system clock scaler is implemented for each PWM. 0 = No scaling of the system clock when calculating the dead band time is implemented.	0 - 1	1
asympwm	Decides if assymetric PWM generation is implemented. This generic can not be set to 0 if the *sympwm* generic is set to 0 as well.	0 - 1	1
sympwm	Decides if symmetric PWM generation is implemented. This generic can not be set to 0 if the *asympwm* generic is set to 0 as well.	0 - 1	1

*Table 801.*Configuration options

Generic name	Function	Allowed range	Default
dcmode	Enables dual compare mode. Core then supports updates of the PWM's compare registers twice during every (symmetric) PWM period. This generic has no effect if sympwm is set to 0.	0 - 1	0
wavepwm	Decides if the core implements support for generating a waveform PWM. If this generic is set to 1 then a RAM block of size *wdepth***wbits* bits will be instantiated.	0 - 1	1
wbits	The number of bits in each of the wdepth words in the internal RAM that holds the waveform. This generic has no impact if *wavepwm* is 0. This generic can not be larger than the *pbits* generic.	1 - 32	8
wdepth	The number of *wbits* wide words that need to fit in the internal buffer holding the waveform. If *wdepth* is not a power of two then the actual number of words that will fit in the buffer is the closest power of two above *wdepth*. This generic has no impact if *wavepwm* is 0.	1 - 8192	512
wsync	If this generic is set the core supports the generation of a synchronization signal. The synchronization signal can be configured to go active any time during the waveform PWM. This generic has no impact if *wavepwm* is 0.	0 - 1	1
sepirq	0 = One irq number (value of *pirq* generic) is used for all PWMs. 1 = Each PWM has it's own irq number, starting with the value of *pirq* and counting up to *pirq*+(*npwm*-1). 2 = The interrupt configuration depend on the *npwm* generic in the following way: If *npwm* < 3, each PWM has its own irq (*pirq* and possibly *pirq*+1). If *npwm* = 3 the PWMs share irq (*pirq*). If 3 < *npwm* < 6 the first three PWMs share irq (*pirq*) and the remaining PWM(s) have their own irq (*pirq*+1 and possibly *pirq*+2). If *npwm* >= 6 the first three PWMs share irq number *pirq*, the second three PWMs share irq number *pirq*+1, and (if implemented) the last two PWMs have their own irq (*pirq*+2 and *pirq*+3).	0 - 2	0
ft	This generic determines if fault tolerance should be added to the RAM that holds the waveform PWM. This generic has no impact if *wavepwm* is 0. 0 = no fault tolerance, 1 = Byte parity DMR, 2 = TMR. Note that this generic need to be set to 0 if the core is used together with the GPL verison of GRLIB, since that version does not include any fault tolerance.	0 - 2	0
defpol	This generic sets the default polarity of the PWM outputs. 0 = Active low polarity, outputs are high after reset/power-up. 1 = Active high polarity, outputs are low after reset/power-up.	0 - 1	1

54.7 Signal descriptions

Table 802 shows the interface signals of the core (VHDL ports).

*Table 802.*Signal descriptions

Signal name	Field	Type	Function	Active
rst	N/A	Input	Reset	Logical 0
clk	N/A	Input	Clock	-
apbi	*	Input	APB slave input signals	-
apbo	*	Output	APB slave output signals	-
o	pwm(x:0)**	Output	PWM signals	***
	wavesync****	Output	Waveform PWM synchronization signal	Logical 1
	tick(y:0)*****	Output	PWM synchronization tick outputs	Logical 1

* see GRLIB IP Library User's Manual

** The width depends on core configuration in the following way: x = <number of PWMs>*2-1 (<number of PWMs> = value of VHDL generic *npwm*)

*** Depends on core configuration.

**** Signal is only driven if the waveform PWM and and waveform sync functionality are implemented (VHDL generics *wavepwm* and *wsync* need to be set to 1).

***** The width depends on core configuration in the following way: y = <number of PWMs>-1 (<number of PWMs> = value of VHDL generic *npwm*)

54.8 Signal definitions and reset values

The signals and their reset values are described in table 803.

*Table 803.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
pwm(x:0)*	Output	PWM signals	**	**
wavesync***	Output	Optional synchronization signal	Logical 1	Logical 0
tick(y:0)****	Output	PWM synchronization tick outputs	Logical 1	Logical 0

* The width depends on core configuration in the following way: x = <number of PWMs>*2-1 (<number of PWMs> = value of VHDL generic *npwm*)

** Depends on core configuration.

*** Signal is only driven if the waveform PWM and and waveform sync functionality are implemented (VHDL generics *wavepwm* and *wsync* need to be set to 1).

**** The width depends on core configuration in the following way: y = <number of PWMs>-1 (<number of PWMs> = value of VHDL generic *npwm*)

54.9 Library dependencies

Table 804 shows the libraries used when instantiating the core (VHDL libraries).

*Table 804.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	PWM	Signals, component	Component declaration
TECHMAP	GENCOMP	Constants, components	Components etc. for technology mapping.

54.10 Timing

The timing waveforms and timing parameters are shown in figure 142 and are defined in table 805.

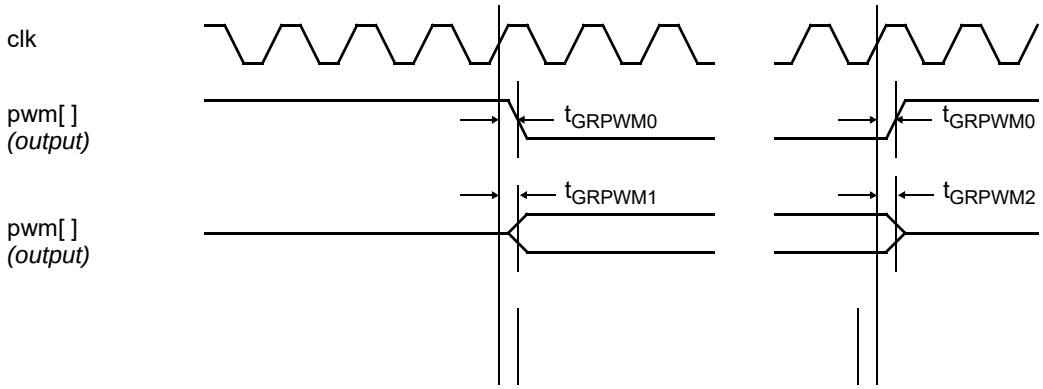


Figure 142. Timing waveforms

*Table 805.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{GRPWM0}	clock to output delay	rising *clk* edge	TBD	TBD	ns
t_{GRPWM1}	clock to non-tri-state delay	rising *clk* edge	-	-	ns
t_{GRPWM2}	clock to tri-state delay	rising *clk* edge	-	-	ns

54.11 Instantiation

This example shows how the core can be instantiated. The instantiated core has all its generics, except *pindex*, *paddr*, and *pirq* at their default values. The impact of the generics can be seen in table 801.

```
library ieee, grlib, gaisler;
use ieee.std_logic_1164.all;
use grlib.amba.all;
use gaisler.pwm.all;

entity grpwm_ex is
  port (
    clk : in std_ulogic;
    rstn : in std_ulogic;
    pwm : out std_logic_vector(5 downto 0)
    );
end;

architecture rtl of grpwm_ex is

  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);

  -- GRPWM signals
  signal pwm : grpwm_out_type;

begin

  -- AMBA Components are instantiated here
  ...

  -- GRPWM core
  grpwm0 : grpwm
    generic map (pindex => 10, paddr => 10, pirq => 10)
    port map (rstn, clk, apbi, apbo(10), pwm);
```

```
  -- Pads for GRPWM core
  pwm_pad : outpadv generic map (tech => padtech, width => 6)
                  port map (pwmo, pwm.pwm);

end;
```

55 GRRT - MIL-STD-1553B / AS15531 Remote Terminal Back-End

55.1 Overview

This core provides the back-end logic for a MIL-STD-1553B Remote Terminal, taking care of the details of the bus protocol. The core provides a simple signaling interface, that can be converted by a front-end to bus master accesses, direct block-RAM, FIFO or register accesses, depending on requirements.

The RT supports single or dual-redundant buses, and all types of transfers allowed by the 1553B standard. The back-end includes 1553 codec, RT protocol handling state machines, and terminal fail-safe timers.

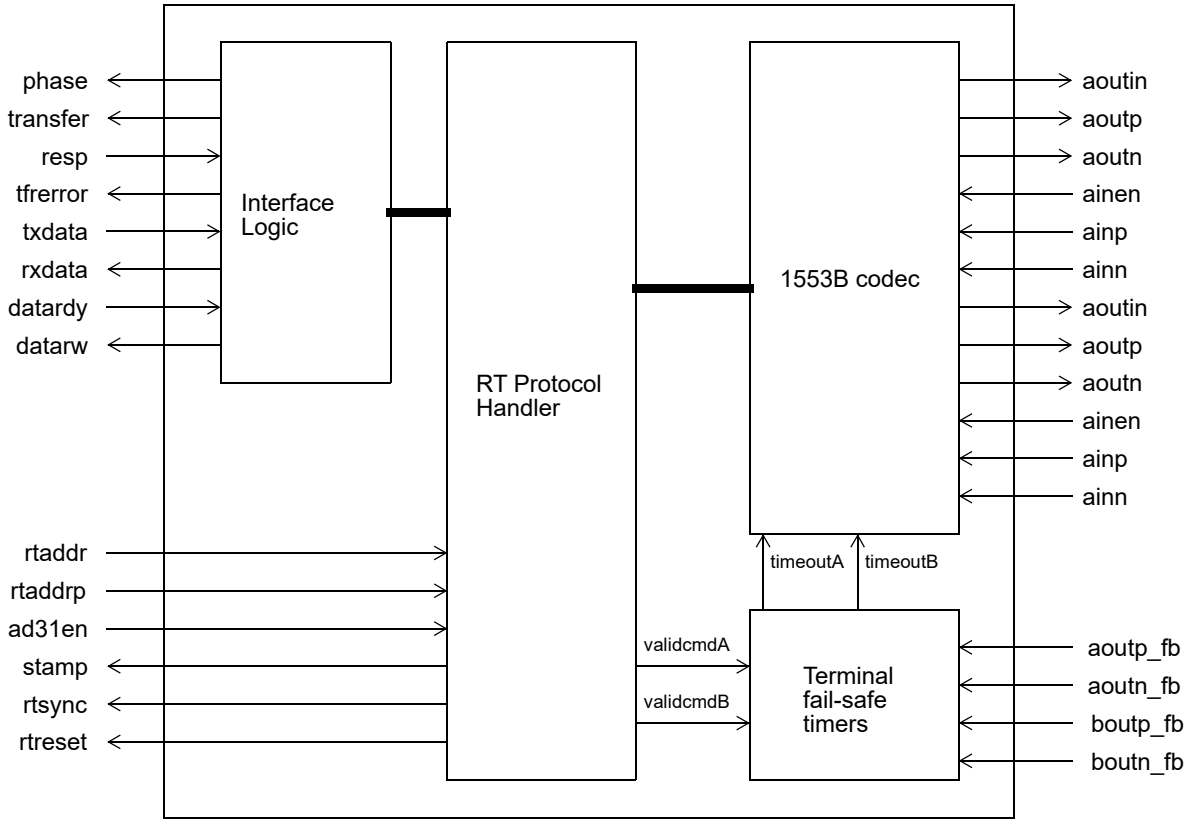


Figure 143. GRRT block diagram showing interfacing signals

55.2 Electrical interface

The core is connected to the MIL-STD-1553B bus wire through single or dual transceivers, isolation transformers and transformer or stub couplers as shown in figure 144. If single-redundancy is used, the unused bus receive P/N signals should be tied both-high or both-low. The transmit enable output is

inverted (called transmitter inhibit) as is the standard on most transceivers. See the standard and the respective component's data sheets for more information on the electrical connection.

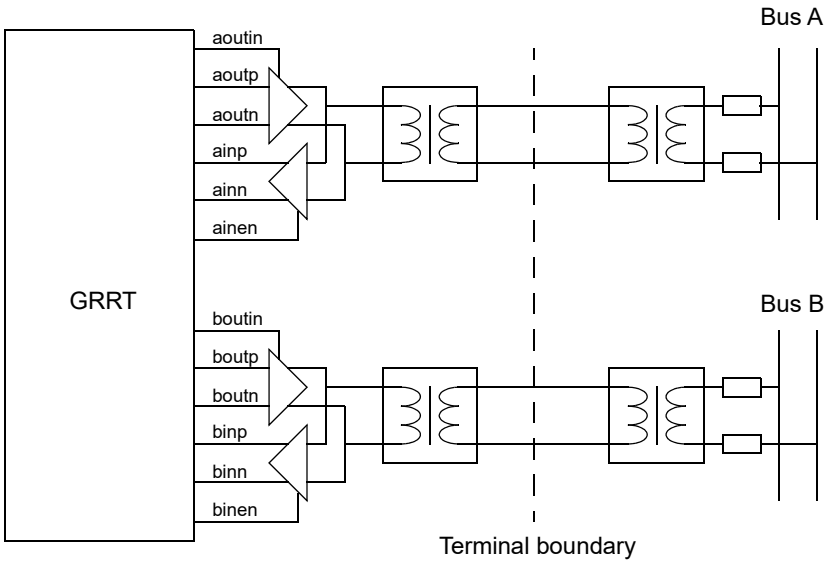


Figure 144. Interface between core and MIL-STD-1553B bus (dual-redundant, transformer coupled)

55.3 Operation

55.3.1 Address configuration

The core's RT address is set through RT address and parity input signals. If the parity is not odd (the exclusive-or of the RT address lines and parity line is zero), the back-end will not respond to commands from the bus.

There is also an input bootstrap signal ad31en, determining whether the address 31 should be treated as a normal RT address or as the broadcast address. If ad31en is high and the RT is configured to address 31, it will respond on this address. If ad31en is low, then the RT will use address 31 as broadcast address and never respond on this address regardless of address configuration.

*Table 806.*Possble address configurations

ad31en	rtaddr	rtaddrp	Regular address	Broadcast address
0	0..30	Correct	=rtaddr	31
		Wrong	None	None
	31	Correct (0)	None	31
		Wrong (1)	None	None
1	0,2,...,30	Correct	=rtaddr	None
		Wrong	None	None
	31	Correct (0)	=rtaddr(=31)	None
		Wrong (1)	None	None

55.3.2 Transfer handling

Each transfer is processed in the following four stages:

- Idle (phase="00") - waiting for command on the bus, "transfer" signal outputs at undefined
- Legalize (phase="01") - Waiting for front-end to respond to legalization request by setting resp inputs to legal (resp="01") or illegal (resp="10").
- Transfer (phase="11") - Transferring data words.

- Commit (phase=”10”) - Transfer completed, successfully if tferror=0. Waiting for frontend to deassert resp input, then goes back to idle.

After the front-end has legalized or illegalized the command by setting resp to “01” or “10”, it should keep the resp signal set until the transfer has completed. In the idle and commit stages, the response should be set back to unknown (“00”). The core will delay going from idle to legalize state if the response signal is already set. This acts as a handshake and prevents earlier responses from getting used multiple times.

55.3.3 Data transfers

During the transfer phase, data words are transferred depending on direction (transfer bit 10).

For receive transfers, received data words will be available on the rxdata output when the datarw signal is high. For transmit transfers, outgoing data words are read from the txdata input when the datarw signal is high.

To provide flow control, the datardy input signals whether the user logic is ready for the datarw signal to be asserted.

The number of words to be transferred is given by bits 4:0 of the transfer output signal, all all-zero value indicates 32 data words. An exception to this is for mode commands with data, where the word count is always 1. In case of error, less words than expected may be transferred.

55.3.4 Error handling

Normally, the best way to handle errors in an RT is to ignore the failed command and let the BC perform the error recovery appropriate for the system. The design of the 1553 bus means the BC can always see an error occured so there is no need to signal this separately.

To simplify the user logic design, transfers will always go through all the four phases and spend at least one cycle in each state, even if an error occurs during the transfer. If an error occurs during the transfer or the request was illegalized by the user logic, the tfrerror output signal is asserted and kept high until the core has left the commit phase.

55.3.5 Response-time requirements

The core will wait for the user logic in three cases:

1. In the legalize phase, waiting for command legalization.

2. In the transfer phase, waiting for the datardy signal to go high.

3, In the commit phase, waiting for the resp signal to go low.

In these cases, the user logic must respond within a limited time in order for the core to continue. Failing to meet these limits will result in the RT not responding to the command or not sending the full word count. It does not cause any permanent error so after the user logic has caught up, it will again work as before.

For the datardy signaling, the maximum tolerated delay is 20 us (400 cycles at 20 MHz), which is the time it takes to send a data word on the 1553 bus.

To analyze the maximum value tolerated for the legalization interface one must consider the bus switching requirement, where another command may arrive on the other bus at any time and override the current command. This could happen while an old transfer is still in the legalize phase. Since the GRRT always processes commands through all four phases, the old command must be legalized, then go to the commit phase and wait for resp to go low, then the new command needs to be legalized. All this must complete within 8.5 us (170 cycles at 20 MHz).

55.3.6 Mode commands

The following mode commands without external data are supported by the core and can not be illegalized:

- Synchronize - will assert the rtsync output one cycle
- Transmit status word - transmits the current value of the 1553 status word
- Transmit last command - transmits the current value of the 1553 status word followed by the last valid command word received by the RT.
- Transmitter shutdown - Shuts down the transmitter on the other bus than the one where the command
- Override transmitter shutdown - Cancels an earlier transmitter shutdown command
- Inhibit terminal flag - Masks the terminal flag bit
- Override inhibit terminal flag bit - Cancels an earlier inhibit terminal flag command
- Reset remote terminal - Clears the transmitter shutdown and inhibit terminal flag status, and asserts the rtreset output for one cycle. The front-end can use this to reset the core, if appropriate.

They will be handled internally by the core, keeping the phase at idle state during the command.

The following mode commands without data are not supported and will be treated as an illegal command (the core will respond with the message error status bit set):

- Dynamic bus control (only applicable to backup bus controllers)
- Initiate self test (no self test implemented)

55.3.7 Mode commands with external data

Three mode commands with external data are supported by the core:

- Synchronize with data word - One received data word is transferred
- Transmit vector word - One data word to transmit is transferred
- Transmit BIT word - One data word is transferred

These will be handled using the same four-phase scheme as regular data transfers, however to identify the mode command bits 9:5 of the transfer output will be set to “00000” or “11111” and bits 4:0 are set to the mode command number. As for regular transfers, it is also possible for the front-end to illegalize these two commands if they are not implemented.

Not supported (always illegalized) mode commands with data are:

- Selected Transmitter Shutdown (not applicable for dual-redundant RTs)
- Override Selected Transmitter Shutdown (not applicable for dual-redundant RTs)

55.3.8 Timestamping

The core has a stamp output which is asserted for one cycle when the command word is received. This is mainly useful together with the rtsync for accurately time-stamping the synchronize mode command for time synchronization purposes.

55.4 Implementation

55.4.1 Clocking

The core operates in two clock domains, the front-end clock domain and the codec clock domain, with internal synchronization between the domains. The codec clock must be 20 or 24 MHz, configured

via the codecfreq generic, but the front-end clock can be any frequency from 10 MHz and up. All the signals interfacing the front-end are synchronous to the front-end clock.

If the front-end clock is the same (20 or 24 MHz) clock as the codec, the generic sameclk can be set to 1 to remove the internal synchronization registers to save some area.

55.4.2 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core has two separate reset inputs for the two clock domain's registers. The resets can be configured as either synchronous or asynchronous.

55.5 Configuration options

Table 807 shows the configuration options of the core (VHDL generics).

*Table 807.*Configuration options

Generic	Function	Allowed range	Default
codecfreq	Codec clock frequency, 20 or 24 MHz	20 or 24	20
sameclk	Set to 1 if codec clock and user clock are tied to the same clock signal (removes synchronization registers)	0-1	1
syncrst	Chooses between synchronous ('1') or asynchronous ('0') reset.	0 - 1	1

55.6 Signal descriptions

Tables 808 shows the interface signals of the core (VHDL ports).

*Table 808.*Signal descriptions on AMBA side

Signal name	Type	Function	Active
CLK	Input	Clock, front-end clock domain	-
RST	Input	Reset, deasserted synchronously to CLK	Low
CLK1553	Input	Codec clock	
RST1553	Input	Reset, deasserted synchronously to CLK1553	Low
RTADDR	Input	RT address (bootstrap signal)	-
RTADDRP	Input	Odd parity for RTADDR (bootstrap signal)	-
RTSTAT	Input	RT status bits Bit 3 - Service request Bit 2 - Busy Bit 1 - Subsystem flag Bit 0 - Terminal flag	
AD31EN	Input	Address 31 configuration: 0 = Address 31 is broadcast address 1 = Address 31 is valid normal RT address Should be kept constant during operation	-
RTSYNC	Output	Asserted for synchonize mode command	High
RTRESET	Output	Asserted for reset remote terminal mode command	High
STAMP	Output	Asserted when receiving a valid command word	High

*Table 808.*Signal descriptions on AMBA side

Signal name	Type	Function	Active
PHASE	Output	Transfer phase: 00 = Idle 01 = Legalize 11 = Transfer 10 = Commit	-
TRANSFER	Output	Transfer description, see section Bit 11 - Broadcast Bit 10 - TX/RX Bit 9:5 - Subaddress / mode code indicator Bit 4:0 - Word count/mode code	-
RESP	Input	Transfer legality response: 00 = Unknown/Idle 01 = Legal 10 = Illegal	-
TFRERROR	Output	Asserted when an error occurs during transfer	
TXDATA	Input	Data for transmit (RT-to-BC) commands	-
RXDATA	Output	Data for receive (BC-to-RT) commands	-
DATARDY	Input	Ready for read/write	High
DATARW	Output	Data word read or write	High
AOUTIN	Output	Bus A Transmitter Inhibit	High inhibit, Low enable
AOUTP	Output	Bus A Transmit Data, Positive	-
AOUTN	Output	Bus A Transmit Data, Negative	-
AINEN	Output	Bus A Receiver Enable	High
AINP	Input	Bus A Receive Data, Positive	-
AINN	Input	Bus A Receive Data, Negative	-
BOUTIN	Output	Bus B Transmitter Inhibit	High inhibit, Low enable
BOUTP	Output	Bus B Transmit Data, Positive	-
BOUTN	Output	Bus B Transmit Data, Negative	-
BINEN	Output	Bus B Receiver Enable	High
BINP	Input	Bus B Receive Data, Positive	-
BINN	Input	Bus B Receive Data, Negative	-
AOUTP_FB	Input	Feedback signal for fail-safe timers, tie to corresponding output signal.	-
AOUTN_FB			
BOUTP_FB			
BOUTN_FB			

55.7 Library dependencies

Table 809 shows libraries used when instantiating the core (VHDL libraries).

*Table 809.*Library dependencies

Library	Package	Imported unit(s)	Description
GAISLER	GR1553B_PKG	Component	Component declaration

56 GRSPW - SpaceWire codec with AHB host Interface and RMAP target

56.1 Overview

The SpaceWire core provides an interface between the AHB bus and a SpaceWire network. It implements the SpaceWire standard (ECSS-E-ST-50-12C) with the protocol identification extension (ECSS-E-ST-50-51C). The optional Remote Memory Access Protocol (RMAP) target implements the ECSS standard (ECSS-E-ST-50-52C).

The core is configured through a set of registers accessed through an APB interface. Data is transferred through DMA channels using an AHB master interface.

Currently, there is one DMA channel but the core can easily be extended to use separate DMA channels for specific protocols. The core can also be configured to have either one or two ports.

There can be up to four clock domains: one for the AHB interface (system clock), one for the transmitter and one or two for the receiver depending on the number of configured ports. The receiver clock can be twice as fast and the transmitter clock four times as fast as the system clock whose frequency should be at least 10 MHz.

The core only supports byte addressed 32-bit big-endian host systems.

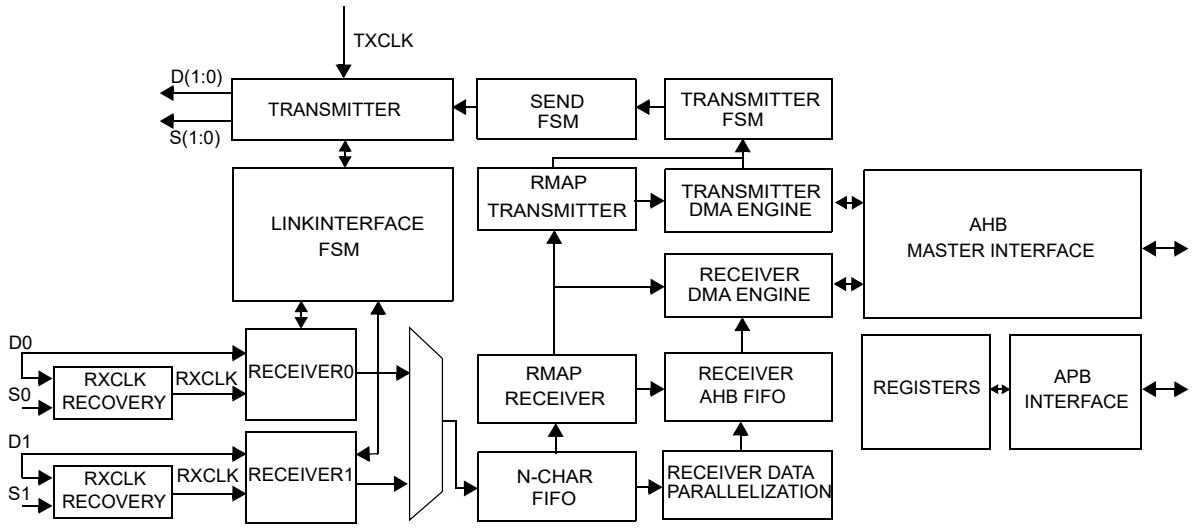


Figure 145. Block diagram

56.2 Operation

56.2.1 Overview

The main sub-blocks of the core are the link-interface, the RMAP target and the AMBA interface. A block diagram of the internal structure can be found in figure 145.

The link interface consists of the receiver, transmitter and the link interface FSM. They handle communication on the SpaceWire network. The AMBA interface consists of the DMA engines, the AHB master interface and the APB interface. The link interface provides FIFO interfaces to the DMA engines. These FIFOs are used to transfer N-Chars between the AMBA and SpaceWire domains during reception and transmission.

The RMAP target is an optional part of the core which can be enabled with a VHDL generic. The RMAP target handles incoming packets which are determined to be RMAP commands instead of the receiver DMA engine. The RMAP command is decoded and if it is valid, the operation is performed

on the AHB bus. If a reply was requested it is automatically transmitted back to the source by the RMAP transmitter.

The core is controlled by writing to a set of user registers through the APB interface and three signals: tick-in, rmapen and clkdiv10. The controlled parts are clock-generation, DMA engines, RMAP target and the link interface.

The link interface, DMA engines, RMAP target and AMBA interface are described in section 56.3, 56.4, 56.5 and 56.7 respectively.

56.2.2 Protocol support

The core only accepts packets with a destination address corresponding to the one set in the node address register. Packets with address mismatch will be silently discarded (except in promiscuous mode which is covered in section 56.4.10). The node address register is initialized to the default address 254 during reset. It can then be changed to other values by writing to the register.

The core has support for the protocol ID specified in ECSS-E-ST-50-51C. It is used for identifying RMAP commands that should be received by the RMAP target. Other packets are stored to the DMA channel. This is only applicable if the RMAP target is present and enabled. When the RMAP target is not present or disabled all the bytes after the address are treated as normal cargo.

RMAP commands are identified using the protocol ID (0x01) and the instruction field. They are handled separately from other packets if the hardware RMAP target is enabled. When enabled, all RMAP commands are processed, executed and replied in hardware. RMAP replies received are always stored to the DMA channel. If the RMAP target is disabled, all packets are stored to the DMA channel. More information on the RMAP protocol support is found in section 56.7.

RMAP packets arriving with the extended protocol ID (0x000001) are stored to the DMA channel which means that the hardware RMAP target will not work if the incoming RMAP packets use the extended protocol ID. Note also that packets with the reserved extended protocol identifier (ID = 0x000000) are not ignored by the core. It is up to the client receiving the packets to ignore them.

When transmitting packets, the address and protocol-ID fields must be included in the buffers from where data is fetched. They are *not* automatically added by the core.

Figure 146 shows the packet types supported by the core. The core also allows reception and transmission with extended protocol identifiers but without support for RMAP CRC calculations and the RMAP target.

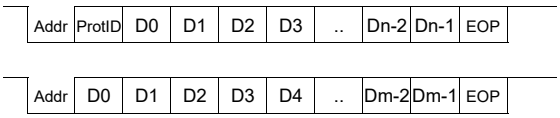


Figure 146. The SpaceWire packet types supported by the GRSPW.

56.3 Link interface

The link interface handles the communication on the SpaceWire network and consists of a transmitter, receiver, a FSM and FIFO interfaces. An overview of the architecture is found in figure 145.

56.3.1 Link interface FSM

The FSM controls the link interface (a more detailed description is found in the SpaceWire standard). The low-level protocol handling (the signal and character level of the SpaceWire standard) is handled by the transmitter and receiver while the FSM in the host domain handles the exchange level.

The link interface FSM is controlled through the control register. The link can be disabled through the link disable bit, which depending on the current state, either prevents the link interface from reaching the started state or forces it to the error-reset state. When the link is not disabled, the link interface FSM is allowed to enter the started state when either the link start bit is set or when a NULL character has been received and the autostart bit is set.

The current state of the link interface determines which type of characters are allowed to be transmitted which together with the requests made from the host interfaces determine what character will be sent.

Time-codes are sent when the FSM is in the run-state and a request is made through the time-interface (described in section 56.3.5).

When the link interface is in the connecting- or run-state it is allowed to send FCTs. FCTs are sent automatically by the link interface when possible. This is done based on the maximum value of 56 for the outstanding credit counter and the currently free space in the receiver N-Char FIFO. FCTs are sent as long as the outstanding counter is less than or equal to 48 and there are at least 8 more empty FIFO entries than the counter value.

N-Chars are sent in the run-state when they are available from the transmitter FIFO and there are credits available. NULLs are sent when no other character transmission is requested or the FSM is in a state where no other transmissions are allowed.

The credit counter (incoming credits) is automatically increased when FCTs are received and decreased when N-Chars are transmitted. Received N-Chars are stored to the receiver N-Char FIFO for further handling by the DMA interface. Received Time-codes are handled by the time-interface.

56.3.2 Transmitter

The state of the FSM, credit counters, requests from the time-interface and requests from the DMA-interface are used to decide the next character to be transmitted. The type of character and the character itself (for N-Chars and Time-codes) to be transmitted are presented to the low-level transmitter which is located in a separate clock-domain.

This is done because one usually wants to run the SpaceWire link on a different frequency than the host system clock. The core has a separate clock input which is used to generate the transmitter clock. More information on transmitter clock generation is found in section 56.8.2. Since the transmitter often runs on high frequency clocks (> 100 MHz) as much logic as possible has been placed in the system clock domain to minimize power consumption and timing issues.

The transmitter logic in the host clock domain decides what character to send next and sets the proper control signal and presents any needed character to the low-level transmitter as shown in figure 147. The transmitter sends the requested characters and generates parity and control bits as needed. If no requests are made from the host domain, NULLs are sent as long as the transmitter is enabled. Most of the signal and character levels of the SpaceWire standard is handled in the transmitter. External LVDS drivers are needed for the data and strobe signals.

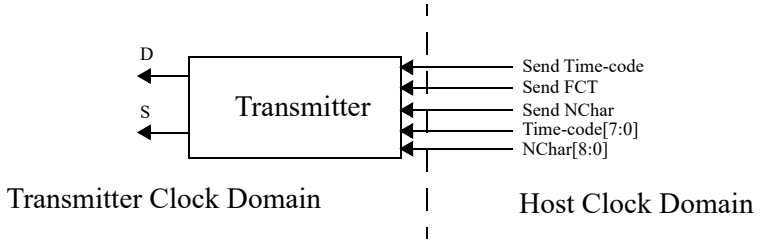


Figure 147. Schematic of the link interface transmitter.

A transmission FSM reads N-Chars for transmission from the transmitter FIFO. It is given packet lengths from the DMA interface and appends EOPs/EEPs and RMAP CRC values if requested. When it is finished with a packet the DMA interface is notified and a new packet length value is given.

56.3.3 Receiver

The receiver detects connections from other nodes and receives characters as a bit stream on the data and strobe signals. It is also located in a separate clock domain which runs on a clock generated from the received data and strobe signals. More information on the clock-generation can be found in section 56.8.2.

The receiver is activated as soon as the link interface leaves the error reset state. Then after a NULL is received it can start receiving any characters. It detects parity, escape and credit errors which causes the link interface to enter the error reset state. Disconnections are handled in the link interface part in the system clock domain because no receiver clock is available when disconnected.

Received Characters are flagged to the host domain and the data is presented in parallel form. The interface to the host domain is shown in figure 148. L-Chars are the handled automatically by the host domain link interface part while all N-Chars are stored in the receiver FIFO for further handling. If two or more consecutive EOPs/EEPs are received all but the first are discarded.

There are no signals going directly from the transmitter clock domain to the receiver clock domain and vice versa. All the synchronization is done to the system clock.

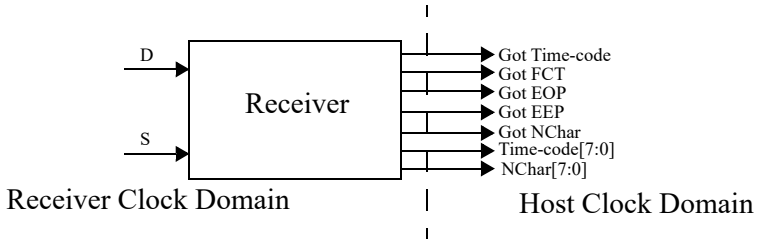


Figure 148. Schematic of the link interface receiver.

56.3.4 Dual port support

The core can be configured to include an additional SpaceWire port. With dual ports the transmitter drives an additional pair of data/strobe output signals and one extra receiver is added to handle a second pair of data/strobe input signals.

One of the ports is set as active (how the active port is selected is explained below) and the transmitter drives the data/strobe signals of the active port with the actual output values as explained in section 56.3.2. The inactive port is driven with zero on both data and strobe.

Both receivers will always be active but only the active port's interface signals (see figure 148) will be propagated to the link interface FSM. Each time the active port is changed, the link will be reset so that the new link is started in a controlled manner.

When the noportforce register is zero the portsel register bit selects the active link and when set to one it is determined by the current link activity. In the latter mode the port is changed when no activity is seen on the currently active link while there is activity on the deselected receive port. Activity is defined as a detected null. This definition is selected so that glitches (e.g. port unconnected) do not cause unwanted port switches.

56.3.5 Time interface

The time interface is used for sending Time-codes over the SpaceWire network and consists of a time-counter register, time-ctrl register, tick-in signal, tick-out signal, tick-in register field and a tick-out

register field. There are also two control register bits which enable the time receiver and transmitter respectively.

Each Time-code sent from the core is a concatenation of the time-ctrl and the time-counter register. There is a timetxen bit which is used to enable Time-code transmissions. It is not possible to send time-codes if this bit is zero.

Received Time-codes are stored to the same time-ctrl and time-counter registers which are used for transmission. The timerxen bit in the control register is used for enabling time-code reception. No time-codes will be received if this bit is zero.

The two enable bits are used for ensuring that a node will not (accidentally) both transmit and receive time-codes which violates the SpaceWire standard. It also ensures that a the master sending time-codes on a network will not have its time-counter overwritten if another (faulty) node starts sending time-codes.

The time-counter register is set to 0 after reset and is incremented each time the tick-in signal is asserted for one clock-period and the timetxen bit is set. This also causes the link interface to send the new value on the network. Tick-in can be generated either by writing a one to the register field or by asserting the tick-in signal. A Tick-in should not be generated too often since if the time-code after the previous Tick-in has not been sent the register will not be incremented and no new value will be sent. The tick-in field is automatically cleared when the value has been sent and thus no new ticks should be generated until this field is zero. If the tick-in signal is used there should be at least 4 system-clock and 25 transmit-clock cycles between each assertion.

A tick-out is generated each time a valid time-code is received and the timerxen bit is set. When the tick-out is generated the tick-out signal will be asserted one clock-cycle and the tick-out register field is asserted until it is cleared by writing a one to it.

The current time counter value can be read from the time register. It is updated each time a Time-code is received and the timerxen bit is set. The same register is used for transmissions and can also be written directly from the APB interface.

The control bits of the Time-code are always stored to the time-ctrl register when a Time-code is received whose time-count is one more than the nodes current time-counter register. The time-ctrl register can be read through the APB interface. The same register is used during time-code transmissions.

It is possible to have both the time-transmission and reception functions enabled at the same time.

56.4 Receiver DMA engine

The receiver DMA engine handles reception of data from the SpaceWire network to different DMA channels. Currently there is only one receive DMA channel available but the core has been written so that additional channels can be easily added if needed.

56.4.1 Basic functionality

The receiver DMA engine reads N-Chars from the N-Char FIFO and stores them to a DMA channel. Reception is based on descriptors located in a consecutive area in memory that hold pointers to buffers where packets should be stored. When a packet arrives at the core it reads a descriptor from memory and stores the packet to the memory area pointed to by the descriptor. Then it stores status to the same descriptor and increments the descriptor pointer to the next one.

56.4.2 Setting up the core for reception

A few registers need to be initialized before reception can take place. First the link interface need to be put in the run state before any data can be sent. The DMA channel has a maximum length register which sets the maximum size of packet that can be received to this channel. Larger packets are truncated and the excessive part is spilled. If this happens an indication will be given in the status field of the descriptor. The minimum value for the receiver maximum length field is 4 and the value can only

be incremented in steps of four bytes. If the maximum length is set to zero the receiver will *not* function correctly.

The node address register needs to be set to hold the address of this SpaceWire node. Packets received with the incorrect address are discarded. Finally, the descriptor table and control register must be initialized. This will be described in the two following sections.

56.4.3 Setting up the descriptor table address

The core reads descriptors from an area in memory pointed to by the receiver descriptor table address register. The register consists of a base address and a descriptor selector. The base address points to the beginning of the area and must start on a 1 kbytes aligned address. It is also limited to be 1 kbytes in size which means the maximum number of descriptors is 128.

The descriptor selector points to individual descriptors and is increased by 1 when a descriptor has been used. When the selector reaches the upper limit of the area it wraps to the beginning automatically. It can also be set to wrap automatically by setting a bit in the descriptors. The idea is that the selector should be initialized to 0 (start of the descriptor area) but it can also be written with another 8 bytes aligned value to start somewhere in the middle of the area. It will still wrap to the beginning of the area.

If one wants to use a new descriptor table the receiver enable bit has to be cleared first. When the rxactive bit for the channel is cleared it is safe to update the descriptor table register. When this is finished and descriptors are enabled the receiver enable bit can be set again.

56.4.4 Enabling descriptors

As mentioned earlier one or more descriptors must be enabled before reception can take place. Each descriptor is 8 byte in size and the layout can be found in the tables below. The descriptors should be written to the memory area pointed to by the receiver descriptor table address register. When new descriptors are added they must always be placed after the previous one written to the area. Otherwise they will not be noticed.

A descriptor is enabled by setting the address pointer to point at a location where data can be stored and then setting the enable bit. The WR bit can be set to cause the selector to be set to zero when reception has finished to this descriptor. IE should be set if an interrupt is wanted when the reception has finished. The DMA control register interrupt enable bit must also be set for this to happen.

The descriptor packet address should be word aligned. All accesses on the bus are word accesses so complete words will always be overwritten regardless of whether all 32-bit contain received data. Also if the packet does not end on a word boundary the complete word containing the last data byte will be overwritten. If the *rxunaligned* or *rmap* VHDL generic is set to 1 this restriction is removed

and any number of bytes can be received to any packet address without excessive bytes being overwritten.

*Table 810.*GRSPW receive descriptor word 0 (address offset 0x0)

31	30	29	28	27	26	25	24 ... 0
TR	DC	HC	EP	IE	WR	EN	PACKETLENGTH

31	Truncated (TR) - Packet was truncated due to maximum length violation.
30	Data CRC (DC) - 1 if a CRC error was detected for the data and 0 otherwise.
29	Header CRC (HC) - 1 if a CRC error was detected for the header and 0 otherwise.
28	EEP termination (EP) - This packet ended with an Error End of Packet character.
27	Interrupt enable (IE) - If set, an interrupt will be generated when a packet has been received if the receive interrupt enable bit in the DMA channel control register is set.
26	Wrap (WR) - If set, the next descriptor used by the GRSPW will be the first one in the descriptor table (at the base address). Otherwise the descriptor pointer will be increased with 0x8 to use the descriptor at the next higher memory location. The descriptor table is limited to 1 kbytes in size and the pointer will be automatically wrap back to the base address when it reaches the 1 kbytes boundary.
25	Enable (EN) - Set to one to activate this descriptor. This means that the descriptor contains valid control values and the memory area pointed to by the packet address field can be used to store a packet.
24: 0	Packet length (PACKETLENGTH) - The number of bytes received to this buffer. Only valid after EN has been set to 0 by the GRSPW.

*Table 811.*GRSPW receive descriptor word 1 (address offset 0x4)

31 ... 0
PACKETADDRESS

31: 0	Packet address (PACKETADDRESS) - The address pointing at the buffer which will be used to store the received packet. If the rxunaligned and rmap VHDL generics are both set to zero only bit 31 to 2 are used.

56.4.5 Setting up the DMA control register

The final step to receive packets is to set the control register in the following steps: The receiver must be enabled by setting the rxen bit in the DMA control register (see section 56.9). This can be done anytime and before this bit is set nothing will happen. The rxdescav bit in the DMA control register is then set to indicate that there are new active descriptors. This must always be done after the descriptors have been enabled or the core might not notice the new descriptors. More descriptors can be activated when reception has already started by enabling the descriptors and writing the rxdescav bit. When these bits are set reception will start immediately when data is arriving.

56.4.6 The effect to the control bits during reception

When the receiver is disabled all packets going to the DMA-channel are discarded. If the receiver is enabled the next state is entered where the rxdescav bit is checked. This bit indicates whether there are active descriptors or not and should be set by the external application using the DMA channel each time descriptors are enabled as mentioned above. If the rxdescav bit is ‘0’ and the nospill bit is ‘0’ the packets will be discarded. If nospill is one the core waits until rxdescav is set.

When rxdescav is set the next descriptor is read and if enabled the packet is received to the buffer. If the read descriptor is not enabled, rxdescav is set to ‘0’ and the packet is spilled depending on the value of nospill.

The receiver can be disabled at any time and will cause all packets received afterwards to be discarded. If a packet is currently received when the receiver is disabled the reception will still be finished. The rxdescav bit can also be cleared at any time. It will not affect any ongoing receptions but

no more descriptors will be read until it is set again. Rxdescav is also cleared by the core when it reads a disabled descriptor.

56.4.7 Address recognition and packet handling

When the receiver N-Char FIFO is not empty, N-Chars are read by the receiver DMA engine. The first character is interpreted as the logical address which is compared to the node address register. If it does not match, the complete packet is discarded (up to and including the next EOP/EEP).

If the address matches the next action taken depends on whether RMAP is enabled or not. If RMAP is disabled all packets are stored to the DMA channel and depending on the conditions mentioned in the previous section, the packet will be received or not. If the packet is received the complete packet including address and protocol ID but excluding EOP/EEP is stored to the address indicated in the descriptor, otherwise the complete packet is discarded.

If RMAP is enabled the protocol ID and 3rd byte in the packet is first checked before any decisions are made. If incoming packet is an RMAP packet (ID = 0x01) and the command type field is 01b the packet is processed by the RMAP command handler which is described in section 56.6. Otherwise the packet is processed by the DMA engine as when RMAP is disabled.

At least 2 non EOP/EEP N-Chars need to be received for a packet to be stored to the DMA channel. If it is an RMAP packet 3 N-Chars are needed since the command byte determines where the packet is processed. Packets smaller than the minimum size are discarded.

56.4.8 Status bits

When the reception of a packet is finished the enable bit in the current descriptor is set to zero. When enable is zero, the status bits are also valid and the number of received bytes is indicated in the length field. The DMA control register contains a status bit which is set each time a packet has been received. The core can also be made to generate an interrupt for this event as mentioned in section 56.4.4.

RMAP CRC logic is included in the implementation if the *rmapcrc* or *rmap* VHDL generic set to 1. The RMAP CRC calculation is always active for all received packets and all bytes except the EOP/EEP are included. The packet is always assumed to be a RMAP packet and the length of the header is determined by checking byte 3 which should be the command field. The calculated CRC value is then checked when the header has been received (according to the calculated number of bytes) and if it is non-zero the HC bit is set indicating a header CRC error.

The CRC value is not set to zero after the header has been received, instead the calculation continues in the same way until the complete packet has been received. Then if the CRC value is non-zero the DC bit is set indicating a data CRC error. This means that the core can indicate a data CRC error even if the data field was correct when the header CRC was incorrect. However, the data should not be used when the header is corrupt and therefore the DC bit is unimportant in this case. When the header is not corrupted the CRC value will always be zero when the calculation continues with the data field and the behaviour will be as if the CRC calculation was restarted

If the received packet is not of RMAP type the header CRC error indication bit cannot be used. It is still possible to use the DC bit if the complete packet is covered by a CRC calculated using the RMAP CRC definition. This is because the core does not restart the calculation after the header has been received but instead calculates a complete CRC over the packet. Thus any packet format with one CRC at the end of the packet calculated according to RMAP standard can be checked using the DC bit.

If the packet is neither of RMAP type nor of the type above with RMAP CRC at the end, then both the HC and DC bits should be ignored.

56.4.9 Error handling

If a packet reception needs to be aborted because of congestion on the network, the suggested solution is to set link disable to '1'. Unfortunately, this will also cause the packet currently being transmitted to be truncated but this is the only safe solution since packet reception is a passive operation depending on the transmitter at the other end. A channel reset bit could be provided but is not a satisfactory solution since the untransmitted characters would still be in the transmitter node. The next character (somewhere in the middle of the packet) would be interpreted as the node address which would probably cause the packet to be discarded but not with 100% certainty. Usually this action is performed when a reception has stuck because of the transmitter not providing more data. The channel reset would not resolve this congestion.

If an AHB error occurs during reception the current packet is spilled up to and including the next EEP/EOP and then the currently active channel is disabled and the receiver enters the idle state. A bit in the channels control/status register is set to indicate this condition.

56.4.10 Promiscuous mode

The core supports a promiscuous mode where all the data received is stored to the DMA channel regardless of the node address and possible early EOPs/EEPs. This means that all non-eop/eep N-Chars received will be stored to the DMA channel. The rxmaxlength register is still checked and packets exceeding this size will be truncated.

RMAP commands will still be handled by the RMAP target when promiscuous mode is enabled if the rmapen bit is set. If it is cleared, RMAP commands will also be stored to the DMA channel.

56.5 Transmitter DMA engine

The transmitter DMA engine handles transmission of data from the DMA channel to the SpaceWire network. There is one DMA channel available but the core has been written so that additional DMA channels can be easily added if needed.

56.5.1 Basic functionality

The transmit DMA engine reads data from the AHB bus and stores them in the transmitter FIFO for transmission on the SpaceWire network. Transmission is based on the same type of descriptors as for the receiver and the descriptor table has the same alignment and size restrictions. When there are new descriptors enabled the core reads them and transfer the amount data indicated.

56.5.2 Setting up the core for transmission

Four steps need to be performed before transmissions can be done with the core. First the link interface must be enabled and started by writing the appropriate value to the ctrl register. Then the address to the descriptor table needs to be written to the transmitter descriptor table address register and one or more descriptors must also be enabled in the table. Finally, the txen bit in the DMA control register should be written with a one which triggers the transmission. These steps will be covered in more detail in the next sections.

56.5.3 Enabling descriptors

The descriptor table address register works in the same way as the receiver's corresponding register which was covered in section 56.4.

To transmit packets one or more descriptors have to be initialized in memory which is done in the following way: The number of bytes to be transmitted and a pointer to the data has to be set. There are two different length and address fields in the transmit descriptors because there are separate pointers for header and data. If a length field is zero the corresponding part of a packet is skipped and if both are zero no packet is sent. The maximum header length is 255 bytes and the maximum data length is

16 Mbyte - 1. When the pointer and length fields have been set the enable bit should be set to enable the descriptor. This must always be done last. The other control bits must also be set before enabling the descriptor.

The transmit descriptors are 16 bytes in size so the maximum number in a single table is 64. The different fields of the descriptor together with the memory offsets are shown in the tables below.

The HC bit should be set if RMAP CRC should be calculated and inserted for the header field and correspondingly the DC bit should be set for the data field. This field is only used by the core when the CRC logic is available (*rmap* or *rmapcrc* VHDL generic set to 1). The header CRC will be calculated from the data fetched from the header pointer and the data CRC is generated from data fetched from the data pointer. The CRCs are appended after the corresponding fields. The NON-CRC bytes field is set to the number of bytes in the beginning of the header field that should not be included in the CRC calculation. The CRCs are sent even if the corresponding length is zero.

When both header and data length are zero no packet is sent not even an EOP.

56.5.4 Starting transmissions

When the descriptors have been initialized, the transmit enable bit in the DMA control register has to be set to tell the core to start transmitting. New descriptors can be activated in the table on the fly (while transmission is active). Each time a set of descriptors is added the transmit enable register bit should be set. This has to be done because each time the core encounters a disabled descriptor this register bit is set to 0.

*Table 812.*GRSPW transmit descriptor word 0 (address offset 0x0)

31 18	17	16	15	14	13	12	11 8	7 0
RESERVED	DC	HC	LE	IE	WR	EN	NONCRCLEN	HEADERLEN

31: 18	RESERVED
17	Append data CRC (DC) - Append CRC calculated according to the RMAP specification after the data sent from the data pointer. The CRC covers all the bytes from this pointer. A null CRC will be sent if the length of the data field is zero.
16	Append header CRC (HC) - Append CRC calculated according to the RMAP specification after the data sent from the header pointer. The CRC covers all bytes from this pointer except a number of bytes in the beginning specified by the non-crc bytes field. The CRC will not be sent if the header length field is zero.
15	Link error (LE) - A Link error occurred during the transmission of this packet.
14	Interrupt enable (IE) - If set, an interrupt will be generated when the packet has been transmitted and the transmitter interrupt enable bit in the DMA control register is set.
13	Wrap (WR) - If set, the descriptor pointer will wrap and the next descriptor read will be the first one in the table (at the base address). Otherwise the pointer is increased with 0x10 to use the descriptor at the next higher memory location.
12	Enable (EN) - Enable transmitter descriptor. When all control fields (address, length, wrap and crc) are set, this bit should be set. While the bit is set the descriptor should not be touched since this might corrupt the transmission. The GRSPW clears this bit when the transmission has finished.
11: 8	Non-CRC bytes (NONCRCLEN)- Sets the number of bytes in the beginning of the header which should not be included in the CRC calculation. This is necessary when using path addressing since one or more bytes in the beginning of the packet might be discarded before the packet reaches its destination.
7: 0	Header length (HEADERLEN) - Header Length in bytes. If set to zero, the header is skipped.

*Table 813.*GRSPW transmit descriptor word 1 (address offset 0x4)

31 0
HEADERADDRESS

31: 0	Header address (HEADERADDRESS) - Address from where the packet header is fetched. Does not need to be word aligned.

*Table 814.*GRSPW transmit descriptor word 2 (address offset 0x8)

31 24	23 0
RESERVED	DATALEN

31: 24	RESERVED
23: 0	Data length (DATALEN) - Length of data part of packet. If set to zero, no data will be sent. If both data- and header-lengths are set to zero no packet will be sent.

*Table 815.*GRSPW transmit descriptor word 3(address offset 0xC)

31 0
DATAADDRESS

31: 0	Data address (DATAADDRESS) - Address from where data is read. Does not need to be word aligned.

56.5.5 The transmission process

When the txen bit is set the core starts reading descriptors immediately. The number of bytes indicated are read and transmitted. When a transmission has finished, status will be written to the first field of the descriptor and a packet sent bit is set in the DMA control register. If an interrupt was requested it will also be generated. Then a new descriptor is read and if enabled a new transmission starts, otherwise the transmit enable bit is cleared and nothing will happen until it is enabled again.

56.5.6 The descriptor table address register

The internal pointer which is used to keep the current position in the descriptor table can be read and written through the APB interface. This pointer is set to zero during reset and is incremented each time a descriptor is used. It wraps automatically when the 1 kbytes limit for the descriptor table is reached or it can be set to wrap earlier by setting a bit in the current descriptor.

The descriptor table register can be updated with a new table anytime when no transmission is active. No transmission is active if the transmit enable bit is zero and the complete table has been sent or if the table is aborted (explained below). If the table is aborted one has to wait until the transmit enable bit is zero before updating the table pointer.

56.5.7 Error handling

Abort Tx

The DMA control register contains a bit called Abort TX which if set causes the current transmission to be aborted, the packet is truncated and an EEP is inserted. This is only useful if the packet needs to be aborted because of congestion on the SpaceWire network. If the congestion is on the AHB bus this will not help (This should not be a problem since AHB slaves should have a maximum of 16 wait-states). The aborted packet will have its LE bit set in the descriptor. The transmit enable register bit is also cleared and no new transmissions will be done until the transmitter is enabled again.

AHB error

When an AHB error is encountered during transmission the currently active DMA channel is disabled and the transmitter goes to the idle mode. A bit in the DMA channel's control/status register is set to indicate this error condition and, if enabled, an interrupt will also be generated. Further error handling depends on what state the transmitter DMA engine was in when the AHB error occurred. If the descriptor was being read the packet transmission had not been started yet and no more actions need to be taken.

If the AHB error occurs during packet transmission the packet is truncated and an EEP is inserted. Lastly, if it occurs when status is written to the descriptor the packet has been successfully transmitted but the descriptor is not written and will continue to be enabled (this also means that no error bits are set in the descriptor for AHB errors).

The client using the channel has to correct the AHB error condition and enable the channel again. No more AHB transfers are done again from the same unit (receiver or transmitter) which was active during the AHB error until the error state is cleared and the unit is enabled again.

Link error

When a link error occurs during the transmission the remaining part of the packet is discarded up to and including the next EOP/EEP. When this is done status is immediately written (with the LE bit set) and the descriptor pointer is incremented. The link will be disconnected when the link error occurs but the core will automatically try to connect again provided that the link-start bit is asserted and the link-disabled bit is deasserted. If the LE bit in the DMA channel's control register is not set the transmitter DMA engine will wait for the link to enter run-state and start a new transmission immediately when possible if packets are pending. Otherwise the transmitter will be disabled when a link error occurs during the transmission of the current packet and no more packets will be transmitted until it is enabled again.

56.6 RMAP

The Remote Memory Access Protocol (RMAP) is used to implement access to resources in the node via the SpaceWire Link. Some common operations are reading and writing to memory, registers and FIFOs. The core has an optional hardware RMAP target which is enabled with a VHDL generic. This section describes the basics of the RMAP protocol and the target implementation.

56.6.1 Fundamentals of the protocol

RMAP is a protocol which is designed to provide remote access via a SpaceWire network to memory mapped resources on a SpaceWire node. It has been assigned protocol ID 0x01. It provides three operations write, read and read-modify-write. These operations are posted operations which means that a source does not wait for an acknowledge or reply. It also implies that any number of operations can be outstanding at any time and that no timeout mechanism is implemented in the protocol. Time-outs must be implemented in the user application which sends the commands. Data payloads of up to 16 Mb - 1 is supported in the protocol. A destination can be requested to send replies and to verify data before executing an operation. A complete description of the protocol is found in the RMAP standard.

56.6.2 Implementation

The core includes a taget for RMAP commands which processes all incoming packets with protocol ID = 0x01 and type field (bit 7 and 6 of the 3rd byte in the packet) equal to 01b. When such a packet is detected it is not stored to the DMA channel, instead it is passed to the RMAP receiver.

The core implements all three commands defined in the standard with some restrictions. First of all the optional error code 12 is not implemented and support is only provided for 32-bit big-endian systems. This means that the first byte received is the msb in a word. The command handler will not receive RMAP packets using the extended protocol ID which are always dumped to the DMA channel.

The RMAP receiver processes commands. If they are correct and accepted the operation is performed on the AHB bus and a reply is formatted. If an acknowledge is requested the RMAP transmitter automatically send the reply. RMAP transmissions have priority over DMA channel transmissions.

Packets with a mismatching destination logical address are never passed to the RMAP target. There is a user accessible destination key register which is compared to destination key field in incoming packets. If there is a mismatch and a reply has been requested the error code in the reply is set to 3. Replies are sent if and only if the ack field is set to '1'.

Detection of all error codes except code 12 is supported. When a failure occurs during a bus access the error code is set to 1 (General Error). There is predetermined order in which error-codes are set in the case of multiple errors in the core. It is shown in table 816.

*Table 816.*The order of error detection in case of multiple errors in the GRSPW. The error detected first has number 1.

Detection Order	Error Code	Error
1	2	Unused RMAP packet type or command code
2	3	Invalid destination key
3	9	Verify buffer overrun
4	11	RMW data length error
5	10	Authorization failure
6*	1	General Error (AHB errors during non-verified writes)
7	5/7	Early EOP / EEP (if early)
8	4	Invalid Data CRC
9	1	General Error (AHB errors during verified writes or RMW)
10	7	EEP
11	6	Cargo Too Large
*The AHB error is not guaranteed to be detected before Early EOP/EEP or Invalid Data CRC. For very long accesses the AHB error detection might be delayed causing the other two errors to appear first.		

Read accesses are performed on the fly, that is they are not stored in a temporary buffer before transmission. This means that the error code 1 will never be seen in a read reply since the header has already been sent when the data is read. If the AHB error occurs the packet will be truncated and ended with an EEP.

Errors up to and including Invalid Data CRC (number 8) are checked before verified commands. The other errors do not prevent verified operations from being performed.

The details of the support for the different commands are now presented. All defined commands which are received but have an option set which is not supported in this specific implementation will not be executed and a possible reply is sent with error code 10.

56.6.3 Write commands

The write commands are divided into two subcategories when examining their capabilities: verified writes and non-verified writes. Verified writes have a length restriction of 4 B and the address must be aligned to the size. That is 1 B writes can be done to any address, 2 B must be halfword aligned, 3 B are not allowed and 4 B writes must be word aligned. Since there will always be only one AHB operation performed for each RMAP verified write command the incrementing address bit can be set to any value.

Non-verified writes have no restrictions when the incrementing bit is set to 1. If it is set to 0 the number of bytes must be a multiple of 4 and the address word aligned. There is no guarantee how many words will be written when early EOP/EEP is detected for non-verified writes.

56.6.4 Read commands

Read commands are performed on the fly when the reply is sent. Thus if an AHB error occurs the packet will be truncated and ended with an EEP. There are no restrictions for incrementing reads but non-incrementing reads have the same alignment restrictions as non-verified writes. Note that the “Authorization failure” error code will be sent in the reply if a violation was detected even if the length field was zero. Also note that no data is sent in the reply if an error was detected i.e. if the status field is non-zero.

56.6.5 RMW commands

All read-modify-write sizes are supported except 6 which would have caused 3 B being read and written on the bus. The RMW bus accesses have the same restrictions as the verified writes. As in the verified write case, the incrementing bit can be set to any value since only one AHB bus operation will be performed for each RMW command. Cargo too large is detected after the bus accesses so this error will not prevent the operation from being performed. No data is sent in a reply if an error is detected i.e. the status field is non-zero.

56.6.6 Control

The RMAP command handler mostly runs in the background without any external intervention, but there are a few control possibilities.

There is an enable bit in the control register of the core which can be used to completely disable the RMAP command handler. When it is set to '0' no RMAP packets will be handled in hardware, instead they are all stored to the DMA channel.

There is a possibility that RMAP commands will not be performed in the order they arrive. This can happen if a read arrives before one or more writes. Since the command handler stores replies in a buffer with more than one entry several commands can be processed even if no replies are sent. Data for read replies is read when the reply is sent and thus writes coming after the read might have been performed already if there was congestion in the transmitter. To avoid this the RMAP buffer disable bit can be set to force the command handler to only use one buffer which prevents this situation.

The last control option for the command handler is the possibility to set the destination key which is found in a separate register.

*Table 817.*GRSPW hardware RMAP handling of different packet type and command fields.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Command	Action
Reserved	Command / Response	Write / Read	Verify data before write	Acknow-ledge	Increment Address		
0	0	-	-	-	-	Response	Stored to DMA-channel.
0	1	0	0	0	0	Not used	Does nothing. No reply is sent.
0	1	0	0	0	1	Not used	Does nothing. No reply is sent.
0	1	0	0	1	0	Read single address	Executed normally. Address has to be word aligned and data size a multiple of four. Reply is sent. If alignment restrictions are violated error code is set to 10.
0	1	0	0	1	1	Read incre-menting address.	Executed normally. No restric-tions. Reply is sent.
0	1	0	1	0	0	Not used	Does nothing. No reply is sent.
0	1	0	1	0	1	Not used	Does nothing. No reply is sent.
0	1	0	1	1	0	Not used	Does nothing. Reply is sent with error code 2.
0	1	0	1	1	1	Read-Mod-ify-Write incrament-ing address	Executed normally. If length is not one of the allowed rmw val-ues nothing is done and error code is set to 11. If the length was correct, alignment restric-tions are checked next. 1 byte can be rmw to any address. 2 bytes must be halfword aligned. 3 bytes are not allowed. 4 bytes must be word aligned. If these restrictions are violated nothing is done and error code is set to 10. If an AHB error occurs error code is set to 1. Reply is sent.
0	1	1	0	0	0	Write, sin-gle-address, do not verify before writ-ing, no acknowledge	Executed normally. Address has to be word aligned and data size a multiple of four. If alignment is violated nothing is done. No reply is sent.
0	1	1	0	0	1	Write, incre-menting address, do not verify before writ-ing, no acknowledge	Executed normally. No restric-tions. No reply is sent.
0	1	1	0	1	0	Write, sin-gle-address, do not verify before writ-ing, send acknowledge	Executed normally. Address has to be word aligned and data size a multiple of four. If alignment is violated nothing is done and error code is set to 10. If an AHB error occurs error code is set to 1. Reply is sent.

*Table 817.*GRSPW hardware RMAP handling of different packet type and command fields.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Command	Action
Reserved	Command / Response	Write / Read	Verify data before write	Acknow-ledge	Increment Address		
0	1	1	0	1	1	Write, incre-menting address, do not verify before writ-ing, send acknowledge	Executed normally. No restric-tions. If AHB error occurs error code is set to 1. Reply is sent.
0	1	1	1	0	0	Write, single address, ver-ify before writing, no acknowledge	Executed normally. Length must be 4 or less. Otherwise nothing is done. Same alignment restric-tions apply as for rmw. No reply is sent.
0	1	1	1	0	1	Write, incre-menting address, ver-ify before writing, no acknowledge	Executed normally. Length must be 4 or less. Otherwise nothing is done. Same alignment restric-tions apply as for rmw. If they are violated nothing is done. No reply is sent.
0	1	1	1	1	0	Write, single address, ver-ify before writing, send acknowledge	Executed normally. Length must be 4 or less. Otherwise nothing is done and error code is set to 9. Same alignment restrictions apply as for rmw. If they are vio-lated nothing is done and error code is set to 10. If an AHB error occurs error code is set to 1. Reply is sent.
0	1	1	1	1	1	Write, incre-menting address, ver-ify before writing, send acknowledge	Executed normally. Length must be 4 or less. Otherwise nothing is done and error code is set to 9. Same alignment restrictions apply as for rmw. If they are vio-lated nothing is done and error code is set to 10. If an AHB error occurs error code is set to 1. Reply is sent.
1	0	-	-	-	-	Unused	Stored to DMA-channel.
1	1	-	-	-	-	Unused	Stored to DMA-channel.

56.7 AMBA interface

The AMBA interface consists of an APB interface, an AHB master interface and DMA FIFOs. The APB interface provides access to the user registers which are described in section 56.9. The DMA engines have 32-bit wide FIFOs to the AHB master interface which are used when reading and writing to the bus.

The transmitter DMA engine reads data from the bus in bursts which are half the FIFO size in length. A burst is always started when the FIFO is half-empty or if it can hold the last data for the packet. The burst containing the last data might have shorter length if the packet is not an even number of bursts in size.

The receiver DMA works in the same way except that it checks if the FIFO is half-full and then performs a burst write to the bus which is half the fifo size in length. The last burst might be shorter. If the *rmap* or *rxunaligned* VHDL generics are set to 1 the interface also handles byte accesses. Byte accesses are used for non word-aligned buffers and/or packet lengths that are not a multiple of four bytes. There might be 1 to 3 single byte writes when writing the beginning and end of the received packets.

56.7.1 APB slave interface

As mentioned above, the APB interface provides access to the user registers which are 32-bits in width. The accesses to this interface are required to be aligned word accesses. The result is undefined if this restriction is violated.

56.7.2 AHB master interface

The core contains a single master interface which is used by both the transmitter and receiver DMA engines. The arbitration algorithm between the channels is done so that if the current owner requests the interface again it will always acquire it. This will not lead to starvation problems since the DMA engines always deassert their requests between accesses.

The AHB accesses are always word accesses (HSIZE = 0x010) of type incremental burst with unspecified length (HBURST = 0x001) if VHDL generics rmap and rxunaligned are disabled. The AHB accesses can be of size byte, halfword and word (HSIZE = 0x000, 0x001, 0x010) otherwise. Byte and halfword accesses are always NONSEQ. Note that read accesses are always word accesses (HSIZE = 0x010), which can result in destructive read.

The burst length will be half the AHB FIFO size except for the last transfer for a packet which might be smaller. Shorter accesses are also done during descriptor reads and status writes.

The AHB master also supports non-incrementing accesses where the address will be constant for several consecutive accesses. HTRANS will always be NONSEQ in this case while for incrementing accesses it is set to SEQ after the first access. This feature is included to support non-incrementing reads and writes for RMAP.

If the core does not need the bus after a burst has finished there will be one wasted cycle (HTRANS = IDLE).

BUSY transfer types are never requested and the core provides full support for ERROR, RETRY and SPLIT responses.

56.8 Implementation

56.8.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

56.8.2 Clock-generation

Figure 149 shows the clock recovery scheme for the receiver. Data and strobe are coupled directly from their pads to an xor gate which generates the clock. The output from the xor is then connected to a clock network. The specific type of clock network depends on the technology used. The xor gate is actually all that logically belongs to the Rx clock recovery module in figure 149.

The clock output drives all flip-flops in the receiver module found in figure 145. The data signal which is used for generating the clock is also coupled to the data inputs of several flip-flops clocked

by the Rx clock as seen in figure 149. Care must be taken so that the delay from the data and strobe signals through the clock network are longer than the delay to the data input + setup time.

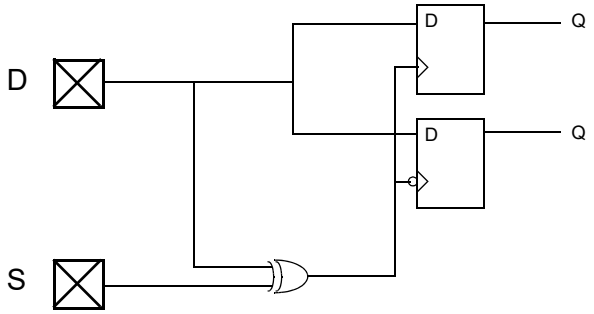


Figure 149. The clocking scheme for the receiver. The clock is

The transmitter clock is generated from the txclk input. A separate clock input is used to allow the transmitter to be run at much higher frequencies than the system clock. The SpaceWire node contains a clock-divider which divides the txclk signal to the wanted frequency. The transmitter clock should be 10 MHz during initialization and any frequency above 2 MHz in the run-state.

There is an input signal called clkdiv10 which sets the clock divisor value during initialization and the reset value for the user accessible clock divisor register. The user register value will be used in run-state. The resulting tx clock frequency will be txclk/(clock divisor value+1). So if no clock division is wanted, the clock divisor should be set to 0.

Since only integer values are allowed for the clock division and the required init-frequency is 10 Mhz the frequency of the txclk input must be a multiple of 10 MHz. The clock divisor value is 8-bits wide so the maximum txclk frequency supported is 2.56 GHz (note that there is also a restriction on the relation between the system and transmit clock frequencies).

56.8.3 Timers

There are two timers in the core: one for generating the 6.4/12.8 us periods and one for disconnect timing. They run on the system (AMBA) clock and the frequency must be at least 10 MHz to guarantee disconnect timing limits.

There are two user accessible registers which are used to the set the number of clock cycles used for the timeout periods. These registers are described in section 56.9.

The reset value for the timer registers can be set in two different ways selected by the usegen VHDL generic. If usegen is set to 1, the sysfreq VHDL generic is used to generate reset values for the disconnect, 6.4 us and 12.8 us timers. Otherwise, the input signals dcrstval and timerrstval will be used as reset values. If the system clock frequency is 10 MHz or above the disconnect time will be within the limits specified in the SpaceWire standard.

56.8.4 Synchronization

The VHDL generic nsync selects how many synchronization registers are used between clock domains. The default is one and should be used when maximum performance is needed. It allows the transmitter to be clocked 4 times faster than the system clock and the receiver 2 times faster. These are theoretical values without consideration for clock skew and jitter. Note also that the receiver clocks data at both negative and positive edges. Thus, the bitrate is twice as high as the clock-rate.

The synchronization limits the Tx and Rx clocks to be at most 4 and 2 times faster than the system clock. But it might not be possible to achieve such high clock rates for the Tx and Rx clocks for all technologies.

The asynchronous reset to the receiver clock domain has to have a maximum delay of one receiver clock cycle to ensure correct operation. This is needed because the receiver uses has a completely

asynchronous reset. To make sure that nothing bad happens the is a synchronous reset guard which prevents any signals from being assigned before all registers have their reset signals released.

56.8.5 Fault-tolerance

The core can optionally be implemented with fault-tolerance against SEU errors in the FIFO memories. The fault-tolerance is enabled through the *ft* VHDL generic. Possible options are byte parity protection (*ft = 1*) or TMR registers (*ft = 2*). Note: the GPL version of GRLIB does not include fault-tolerance, and the core will not work unless the *ft* VHDL generic is 0.

56.8.6 Synthesis

Since the receiver and transmitter may run on very high frequency clocks their clock signals have been coupled through a clock buffer with a technology wrapper. This clock buffer will utilize a low skew net available in the selected technology for the clock.

The clock buffer will also enable most synthesis tools to recognize the clocks and it is thus easier to find them and place constraints on them. The fact there are three clock domains in the GRSPW of which all are possibly high frequency clocks makes it necessary to declare all paths between the clock domains as false paths.

In Synplify this is most easily done by declaring all the clocks to be in different clockgroups in the sdc file (if Synplify does not automatically put them in different groups). This will disable any timing considerations between the clock domains and these constraints will also propagate to the place and route tool.

The type of clock buffer is selectable with a VHDL generic and the value zero provides a normal feed through which lets the synthesis tool infer the type of net used.

56.8.7 Technology mapping

The core has three generics for technology mapping: *tech*, *techfifo* and *memtech*. *Tech* selects the technology used for the clock buffers and also adds reset to some registers for technologies where they would otherwise cause problems with gate-level simulations. *Techfifo* selects whether *memtech* should be used to select the technology for the FIFO memories (the RMAP buffer is not affected by the this generic) or if they should be inferred. *Tech* and *memtech* can be set to any value from 0 to NTECH as defined in the GRLIB.TECH package.

56.8.8 RAM usage

The core maps all RAM memories on the syncram_2p component if the *ft* generic is 0 and to the syncram_2pft component for other values. The syncrams are located in the technology mapping library (TECHMAP). The organization of the different memories are described below. If techfifo and/or memtech is set to 0 the synthesis tool will infer the memories. Either RAM blocks or flip-flops will be used depending on the tool and technology. The number of flip-flops used is *syncram depth x syncram width* for all the different memories. The receiver AHB FIFO with fifosize 32 will for example use 1024 flips-flops.

Receiver ahb FIFO

The receiver AHB fifo consists of one syncram_2p block with a width of 32-bits. The depth is determined by the configured FIFO depth. Table 818 shows the syncram organization for the allowed configurations.

*Table 818.*syncram_2p sizes for GRSPW receiver AHB FIFO.

Fifosize	Syncram_2p organization
4	4x32
8	8x32
16	16x32
32	32x32

Transmitter ahb FIFO

The transmitter AHB fifo consists of one syncram_2p block with a width of 32-bits. The depth is determined by the configured FIFO depth. Table 819 shows the syncram organization for the allowed configurations.

*Table 819.*syncram_2p sizes for transmitter AHB FIFO.

Fifosize	Syncram_2p organization
4	4x32
8	8x32
16	16x32
32	32x32

Receiver N-Char FIFO

The receiver N-Char fifo consists of one syncram_2p block with a width of 10-bits. The depth is determined by the configured FIFO depth. Table 820 shows the syncram organization for the allowed configurations.

*Table 820.*syncram_2p sizes for the receiver N-Char FIFO.

Fifosize	Syncram_2p organization
16	16x10
32	32x10
64	64x10

RMAP buffer

The RMAP buffer consists of one syncram_2p block with a width of 8-bits. The depth is determined by the number of configured RMAP buffers. Table 821 shows the syncram organization for the allowed configurations.

*Table 821.*syncram_2p sizes for RMAP buffer memory.

RMAP buffers	Syncram_2p organization
2	64x8
4	128x8
8	256x8

56.9 Registers

The core is programmed through registers mapped into APB address space.

*Table 822.*GRSPW registers

APB address offset	Register
0x0	Control
0x4	Status/Interrupt-source
0x8	Node address
0xC	Clock divisor
0x10	Destination key
0x14	Time
0x18	Timer and Disconnect
0x20	DMA channel 1 control/status
0x24	DMA channel 1 rx maximum length
0x28	DMA channel 1 transmit descriptor table address.
0x2C	DMA channel 1 receive descriptor table address.

56.9.1 Control Register

*Table 823.*0x00 - CTRL - control register

31	30	29	28	27	26	25	22	21	20	19	18	17	16	15	12	11	10	9	8	7	6	5	4	3	2	1	0
RA	RX	RC	R		PO	RESERVED		PS	NP	R		RD	RE	RESERVED		TR	TT	LI	TQ	R	RS	PM	TI	IE	AS	LS	LD
*	*	*	0		*	0		0	*	0		0	*	0		0	0	NR	NR	0	0	0	0	0	*	0	0
r	r	r	r		r	r		rw*	rw*	r		rw*	rw*	r		rw	rw	rw	rw	rw	rw*	rw	rw	rw	rw	rw	rw

31 RMAP available (RA) - Set to one if the RMAP command handler is available. Only readable.

30 RX unaligned access (RX) - Set to one if unaligned writes are available for the receiver. Only readable.

29 RMAP CRC available (RC) - Set to one if RMAP CRC is enabled in the core. Only readable.

28: 27 RESERVED

26 Number of ports (PO) - The number of available SpaceWire ports minus one. Only readable.

25: 22 RESERVED

21 Port select (PS) - Selects the active port when the no port force bit is zero. ‘0’ selects the port connected to data and strobe on index 0 while ‘1’ selects index 1. Only available if the ports VHDL generic is set to 2. Reset value: ‘0’.

20 No port force (NP) - Disable port force. When disabled the port select bit cannot be used to select the active port. Instead, it is automatically selected by checking the activity on the respective receive links. Only available if the ports VHDL generic is set to 2. Reset value: ‘0’ if the RMAP command handler is not available. If available the reset value is set to the value of the rmapen input signal.

19: 18 RESERVED

17 RMAP buffer disable (RD) - If set only one RMAP buffer is used. This ensures that all RMAP commands will be executed consecutively. Only available if the rmap VHDL generic is set to 1. Reset value: ‘0’.

16 RMAP Enable (RE) - Enable RMAP command handler. Only available if rmap VHDL generic is set to 1. Reset value: ‘1’.

15: 12 RESERVED

11 Time Rx Enable (TR) - Enable time-code receptions. Reset value: ‘0’.

10 Time Tx Enable (TT) - Enable time-code transmissions. Reset value: ‘0’.

9 Link error IRQ (LI) - Generate interrupt when a link error occurs. Not reset.

8 Tick-out IRQ (TQ) - Generate interrupt when a valid time-code is received. Not reset.

7 RESERVED

6 Reset (RS) - Make complete reset of the SpaceWire node. Self clearing. Reset value: ‘0’.

5 Promiscuous Mode (PM) - Enable Promiscuous mode. Reset value: ‘0’.

4 Tick In (TI) - The host can generate a tick by writing a one to this field. This will increment the timer counter and the new value is transmitted after the current character is transferred. A tick can also be generated by asserting the tick_in signal. Reset value: ‘0’.

3 Interrupt Enable (IE) - If set, an interrupt is generated when one or both of bit 8 to 9 is set and its corresponding event occurs. Reset value: ‘0’.

2 Autostart (AS) - Automatically start the link when a NULL has been received. Reset value: ‘0’ if the RMAP command handler is not available. If available the reset value is set to the value of the rmapen input signal.

1 Link Start (LS) - Start the link, i.e. allow a transition from ready to started state. Reset value: ‘0’.

0 Link Disable (LD) - Disable the SpaceWire codec. Reset value: ‘0’.

56.9.2 Status Register

*Table 824.*0x04 - STS - status register

31 24	23 21	20 10	9	8	7	6	5	4	3	2	1	0
RESERVED	LS	RESERVED	AP	EE	IA	WE	R	PE	DE	ER	CE	TO
0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	rw*	wc	wc	wc	r	wc	wc	wc	wc	wc

31: 24 RESERVED

23: 21 Link State (LS) - The current state of the start-up sequence. 0 = Error-reset, 1 = Error-wait, 2 = Ready, 3 = Started, 4 = Connecting, 5 = Run. Reset value: 0.

20: 10 RESERVED

9 Active port (AP) - Shows the currently active port. ‘0’ = Port 0 and ‘1’ = Port 1 where the port numbers refer to the index number of the data and strobe signals. Only available if the ports generic is set to 2.

8 Early EOP/EEP (EE) - Set to one when a packet is received with an EOP after the first byte for a non-rmap packet and after the second byte for a RMAP packet. Cleared when written with a one. Reset value: ‘0’.

7 Invalid Address (IA) - Set to one when a packet is received with an invalid destination address field, i.e it does not match the nodeaddr register. Cleared when written with a one. Reset value: ‘0’.

6 Write synchronization Error (WE) - A synchronization problem has occurred when receiving N-Chars. Cleared when written with a one. Reset value: ‘0’.

5 RESERVED

4 Parity Error (PE) - A parity error has occurred. Cleared when written with a one. Reset value: ‘0’.

3 Disconnect Error (DE) - A disconnection error has occurred. Cleared when written with a one. Reset value: ‘0’.

2 Escape Error (ER) - An escape error has occurred. Cleared when written with a one. Reset value: ‘0’.

1 Credit Error (CE) - A credit has occurred. Cleared when written with a one. Reset value: ‘0’.

0 Tick Out (TO) - A new time count value was received and is stored in the time counter field. Cleared when written with a one. Reset value: ‘0’.

56.9.3 Node Address Register

*Table 825.*0x08 - NODEADDR - node address register

31 8	7 0
RESERVED	NODEADDR
0	*
r	rw

31: 8 RESERVED

7: 0 Node address (NODEADDR) - 8-bit node address used for node identification on the SpaceWire network. Reset value: 254 (taken from the nodeaddr VHDL generic when /= 255, else from the rmapnodeaddr input signal)

56.9.4 Clock Divisor Register

*Table 826.*0x0C - CLKDIV - clock divisor register

31 16	15 8	7 0
RESERVED	CLKDIVSTART	CLKDIVRUN
0	*	*
r	rw	rw

31: 16 RESERVED

15: 8 Clock divisor startup (CLKDIVSTART) - 8-bit Clock divisor value used for the clock-divider during startup (link-interface is in other states than run). The actual divisor value is Clock Divisor register + 1. Reset value: clkdiv10 input signal.

7: 0 Clock divisor run (CLKDIVRUN) - 8-bit Clock divisor value used for the clock-divider when the link-interface is in the run-state. The actual divisor value is Clock Divisor register + 1. Reset value: clkdiv10 input signal.

56.9.5 Destination Key

*Table 827.*0x10 - DKEY - destination key

31 8	7 0
RESERVED	DESTKEY
0	*
r	rw

31: 8 RESERVED

7: 0 Destination key (DESTKEY) - RMAP destination key. Only available if the rmap VHDL generic is set to 1. Reset value: 0 (taken from the deskey VHDL generic)

56.9.6 Time Register

*Table 828.*0x14 - TIME - time register

31 8	7 6	5 0
RESERVED	TCTRL	TIMECNT
0	0	0
r	rw	rw

31: 8 RESERVED

7: 6 Time control flags (TCTRL) - The current value of the time control flags. Sent with time-code resulting from a tick-in. Received control flags are also stored in this register. Reset value: ‘0’.

5: 0 Time counter (TIMECNT) - The current value of the system time counter. It is incremented for each tick-in and the incremented value is transmitted. The register can also be written directly but the written value will not be transmitted. Received time-counter values are also stored in this register. Reset value: ‘0’.

56.9.7 Timer and Disconnect Register

*Table 829.*0x18 - TDR - timer and disconnect register.

31 22	21 12	11 0
RESERVED	DISCONNECT	TIMER64

31: 22 RESERVED

21: 12 Disconnect (DISCONNECT) - Used to generate the 850 ns disconnect time period. The disconnect period is the number is the number of clock cycles in the disconnect register + 3. So to get a 850 ns period, the smallest number of clock cycles that is greater than or equal to 850 ns should be calculated and this values - 3 should be stored in the register. Reset value is set with VHDL generics or with input signals depending on the value of the usegen VHDL generic.

11: 0 6.4 us timer (TIMER64) - Used to generate the 6.4 and 12.8 us time periods. Should be set to the smallest number of clock cycles that is greater than or equal to 6.4 us. Reset value is set with VHDL generics or with input signals depending on the value of the usegen VHDL generic.

56.9.8 DMA Control Register

*Table 830.*0x20 - DMACTRL - dma control register

31 17	16	15 13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	LE	RESERVED	NS	RD	RX	AT	RA	TA	PR	PS	AI	RI	TI	RE	TE
0	0	0	0	0	0	0	0	0	0	0	NR	NR	NR	0	0
r	rw	r	rw	rw	r	r	wc	wc	wc	wc	rw	rw	rw	rw	rw

31: 17 RESERVED

16 Link error disable (LE) - Disable transmitter when a link error occurs. No more packets will be transmitted until the transmitter is enabled again. Reset value: ‘0’.

15: 13 RESERVED

12 No spill (NS) - If cleared, packets will be discarded when a packet is arriving and there are no active descriptors. If set, the GRSPW will wait for a descriptor to be activated.

11 Rx descriptors available (RD) - Set to one, to indicate to the GRSPW that there are enabled descriptors in the descriptor table. Cleared by the GRSPW when it encounters a disabled descriptor: Reset value: ‘0’.

10 RX active (RX) - Is set to ‘1’ if a reception to the DMA channel is currently active otherwise it is ‘0’. Only readable.

9 Abort TX (AT) - Set to one to abort the currently transmitting packet and disable transmissions. If no transmission is active the only effect is to disable transmissions. Self clearing. Reset value: ‘0’.

8 RX AHB error (RA) - An error response was detected on the AHB bus while this receive DMA channel was accessing the bus. Cleared when written with a one. Reset value: ‘0’.

7 TX AHB error (TA) - An error response was detected on the AHB bus while this transmit DMA channel was accessing the bus. Cleared when written with a one. Reset value: ‘0’.

6 Packet received (PR) - This bit is set each time a packet has been received. never cleared by the SW-node. Cleared when written with a one. Reset value: ‘0’.

5 Packet sent (PS) - This bit is set each time a packet has been sent. Never cleared by the SW-node. Cleared when written with a one. Reset value: ‘0’.

4 AHB error interrupt (AI) - If set, an interrupt will be generated each time an AHB error occurs when this DMA channel is accessing the bus. Not reset.

3 Receive interrupt (RI) - If set, an interrupt will be generated each time a packet has been received. This happens both if the packet is terminated by an EEP or EOP. Not reset.

2 Transmit interrupt (TI) - If set, an interrupt will be generated each time a packet is transmitted. The interrupt is generated regardless of whether the transmission was successful or not. Not reset.

*Table 830.*0x20 - DMACTRL - dma control register

1 Receiver enable (RE) - Set to one when packets are allowed to be received to this channel. Reset value: ‘0’.

0 Transmitter enable (TE) - Write a one to this bit each time new descriptors are activated in the table. Writing a one will cause the SW-node to read a new descriptor and try to transmit the packet it points to. This bit is automatically cleared when the SW-node encounters a descriptor which is disabled. Reset value: ‘0’.

56.9.9 RX Maximum Length Register

*Table 831.*0x24 - DMAMAXLEN - RX maximum length register.

31 25	24 2	1 0
RESERVED	RXMAXLEN	R
0	NR	0
r	rw	r

31: 25 RESERVED

24: 2 RX maximum length (RXMAXLEN) - Receiver packet maximum length in bytes. Only bits 24 - 2 are writable. Bits 1 - 0 are always 0. Not reset.

1: 0 RESERVED

56.9.10 Transmitter Descriptor Table Address Register

*Table 832.*0x28 - DMATYDESC - transmitter descriptor table address register.

31 10	9 4	3 0
DESCBASEADDR	DESCSEL	RESERVED
NR	0	0
rw	rw	r

31: 10 Descriptor table base address (DESCBASEADDR) - Sets the base address of the descriptor table. Not reset.

9: 4 Descriptor selector (DESCSEL) - Offset into the descriptor table. Shows which descriptor is currently used by the GRSPW. For each new descriptor read, the selector will increase with 16 and eventually wrap to zero again. Reset value: 0.

3: 0 RESERVED

56.9.11 Receiver Descriptor Table Address Register

*Table 833.*0x2C - DMARXDESC - receiver descriptor table address register.

31 10	9 3	2 0
DESCBASEADDR	DESCSEL	RESERVED
NR	0	0
rw	rw	r

31: 10 Descriptor table base address (DESCBASEADDR) - Sets the base address of the descriptor table. Not reset.

9: 3 Descriptor selector (DESCSEL) - Offset into the descriptor table. Shows which descriptor is currently used by the GRSPW. For each new descriptor read, the selector will increase with 8 and eventually wrap to zero again. Reset value: 0.

2: 0 RESERVED

56.10 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x1F. For description of vendor and device identifiers see GRLIB IP Library User’s Manual.

56.11 Configuration options

Table 834 shows the configuration options of the core (VHDL generics).

*Table 834.*Configuration options

Generic	Function	Allowed range	Default
tech	Technology for clock buffers	0 - NTECH	inferred
hindex	AHB master index.	0 - NAHBMST-1	0
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	Addr field of the APB bar.	0 - 16#FFF#	0
pmask	Mask field of the APB bar.	0 - 16#FFF#	16#FFF#
pirq	Interrupt line used by GRSPW.	0 - NAHBIRQ-1	0
sysfreq	Frequency of clock input “clk” in kHz.	-	10000
usegen	Use values calculated from sysfreq generic as reset values for 6.4 us timer and disconnect timer.	0 - 1	1
nsync	Number of synchronization registers. Warning: Value 2 only to be used when bit rate is equal or less than the system clock frequency.	1 - 2	1
rmap	Include hardware RMAP target. RMAP CRC logic will also be added. If set to 2 the core will only implement the RMAP target, provide a limited APB interface, enable time code reception and its interrupt.	0 - 2	0
rmapcrc	Enable RMAP CRC logic.	0 - 1	0
fifosize1	Sets the number of entries in the 32-bit receiver and transmitter AHB fifos.	4 - 32	32
fifosize2	Sets the number of entries in the 9-bit receiver fifo (N-Char fifo).	16 - 64	64
rxclkbuftype	Select clock buffer type for receiver clock. 0 does not select a buffer, instead i connects the input directly to the output (synthesis tools may still infer a buffer). 1 selects hardwired clock while 2 selects routed clock.	0 - 2	0
rxunaligned	Receiver unaligned write support. If set, the receiver can write any number of bytes to any start address without writing any excessive bytes.	0 - 1	0
rmapbufs	Sets the number of buffers to hold RMAP replies.	2 - 8	4
ft	Enable fault-tolerance against SEU errors	0 - 2	0
scantest	Enable support for scan test	0 - 1	0
techfifo	Implement FIFO with RAM cells (1) or flip-flops (0)	0 - 1	1
netlist	Use netlist rather then RTL code	0 - 1	0
ports	Sets the number of ports	1 - 2	1
memtech	Technology for RAM blocks	0 - NTECH	inferred
nodeaddr	Sets the reset value for the core’s node address. Value 255 enables rmapnodeaddr input instead.	0 - 254 255	254
destkey	Sets the reset value for the core’s destination key.	0 - 255	0

56.12 Signal descriptions

Table 835 shows the interface signals of the core (VHDL ports). As indicated in the table the core consists of two different entities, called GRSPW and GRSPW_PHY. The GRSPW entity is the main part and includes most core’s functionality, while the GRSPW_PHY only handles the receiver clock

generation and the lower parts of the PHY layer. One GRSPW_PHY entity is used per port. See section 56.16 for information on how to interface GRSPW with GRSPW_PHY.

Table 835. Signal descriptions

Entity	Signal name	Field	Type	Function	Active
GRSPW	RST	N/A	Input	Reset	Low
	CLK	N/A	Input	Clock	-
	RXCLK[1:0]	N/A	Input	Receiver clock. One clock per port.	-
	TXCLK	N/A	Input	Transmitter default run-state clock	-
	AHBMI	*	Input	AHB master input signals	-
	AHBMO	*	Output	AHB master output signals	-
	APBI	*	Input	APB slave input signals	-
	APBO	*	Output	APB slave output signals	-
	SWNI	D[1:0]	Input	Data input synchronous to RXCLK (rising edge). One bit per port.	-
		ND[9:0]	Input	Data input synchronous to RXCLK (falling edge). Five bits per port.	
		TICKIN	Input	Time counter tick input	High
		CLKDIV10	Input	Clock divisor value used during initialization and as reset value for the clock divisor register	-
		RMAPEN	Input	Reset value for the rmapen control register bit	-
		RMAPNODEADDR	Input	Reset value for nodeaddr register bits when nodeaddr VHDL generic /= 255	-
		DCRSTVAL	Input	Reset value for disconnect timer. Used if usegen VHDL generic is set to 0.	-
		TIMERRSTVAL	Input	Reset value for 6.4 us timer. Used if usegen VHDL generic is set to 0.	-
		DCONNECT[3:0]	Input	Disconnect strobes. Two bits per port.	
	SWNO	D[1:0]	Output	SpaceWire data output. One bit per port.	-
		S[1:0]	Output	SpaceWire strobe output. One bit per port.	-
		TICKOUT	Output	Time counter tick output	High
		LINKDIS	Output	Linkdisabled status	High
		RMAPACT	Output	RMAP command processing active	High
		RXRST	Output	Receiver reset.	Low

Table 835. Signal descriptions

Entity	Signal name	Field	Type	Function	Active
GRSPW_PHY	RXRST	N/A	Input	Receiver reset.	Low
	DI	N/A	Input	SpaceWire data input.	-
	SI	N/A	Input	SpaceWire strobe input.	-
	RXCLKO	N/A	Output	Receiver clock recovered from data and strobe input.	-
	DO	N/A	Ouput	Recovered data, synchronous to RXCLKO (rising edge).	-
	NDO[4:0]	N/A	Ouput	Recovered data, synchronous to RXCLKO (falling edge)	-
	DCON-NECT[1:0]	N/A	Ouput	Disconnect strobe signals.	-
	TESTEN	N/A	Input	Scan test enable	High
	TESTCLK	N/A	Input	Scan test clock. Used inside the GRSP-W_PHY entity instead of recovered RXCLK when TESTEN is active.	-
	* see GRLIB IP Library User's Manual				

56.13 Signal definitions and reset values

The signals and their reset values are described in table 836.

*Table 836.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
spw_clk	Input	Transmitter default run-state clock	Rising edge	-
spw_rxd	Input, LVDS	Data input, positive	High	-
spw_rxdn	Input, LVDS	Data input, negative	Low	-
spw_rxs	Input, LVDS	Strobe input, positive	High	-
spw_rxsn	Input, LVDS	Strobe input, negative	Low	-
spw_txd	Output, LVDS	Data output, positive	High	Logical 0
spw_txdn	Output, LVDS	Data output, negative	Low	Logical 1
spw_txs	Output, LVDS	Strobe output, positive	High	Logical 0
spw_txsn	Output, LVDS	Strobe output, negative	Low	Logical 1

56.14 Timing

The timing waveforms and timing parameters are shown in figure 150 and are defined in table 837.

The SpaceWire jitter and skew timing waveforms and timing parameters are shown in figure 151 and are defined in table 838.

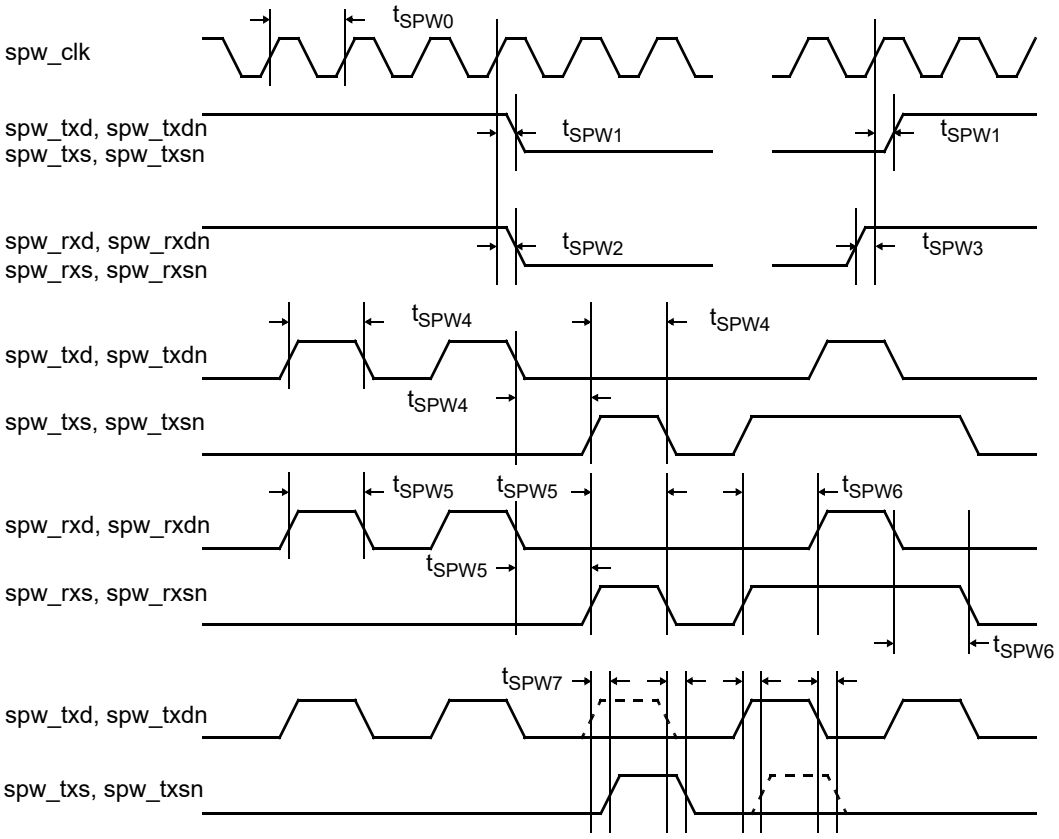


Figure 150. Timing waveforms

*Table 837.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{SPW0}	transmit clock period	-	TBD	-	ns
t_{SPW1}	clock to output delay	rising *spw_clk* edge	TBD	TBD	ns
t_{SPW2}	input to clock hold	-	-	-	not applicable
t_{SPW3}	input to clock setup	-	-	-	not applicable
t_{SPW4}	output data bit period	-	-		*clk* periods
		-	t_{SPW0} - TBD	t_{SPW0} +TBD	ns
t_{SPW5}	input data bit period	-	TBD	-	ns
t_{SPW6}	data & strobe edge separation	-	TBD	-	ns
t_{SPW7}	data & strobe output skew	-	-	TBD	ns

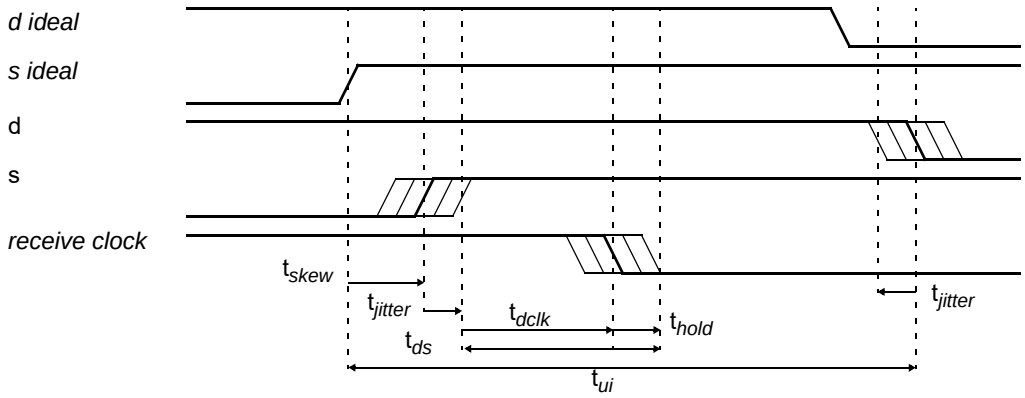


Figure 151. Skew and jitter timing waveforms

*Table 838.*Skew and jitter timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{skew}	skew between data and strobe	-	-	TBD	ns
t_{jitter}	jitter on data or strobe	-	-	TBD	ns
t_{ds}	minimum separation between data and strobe edges	-	TBD	-	ns
t_{dclk}	delay from edge of data or strobe to the receiver flip-flop	-	-	TBD	ns
t_{hold}	hold timer on receiver flip-flop	-	TBD	-	ns
t_{ui}	unit interval (bit period)	-	TBD	-	ns

56.15 Library dependencies

Table 839 shows libraries used when instantiating the core (VHDL libraries).

*Table 839.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	SPACEWIRE	Signals, component	Component and record declarations.

56.16 Instantiation

This example shows how the core can be instantiated.

Normally di, si, do and so should be connected to input and output pads configured with LVDS drivers. How this is done is technology dependent.

The GRSPW in the example is a 2-port core configured with non-ft memories of size 4, 64 and 8 entries for AHB FIFOs, N-Char FIFO and RMAP buffers respectively. The system frequency (clk) is 40 MHz and the transmitter frequency (txclk) is 20 MHz.

The memory technology is inferred which means that the synthesis tool will select the appropriate components. The rx clk buffer uses a hardwired clock.

The hardware RMAP command handler is enabled which also automatically enables rxunaligned and rmapcrc. Finally, the DMA channel interrupt line is 2 and the number of synchronization registers is 1.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.spacewire.all;

entity spacewire_ex is
  port (
    clk  : in std_ulogic;
    rstn : in std_ulogic;

    -- spacewire signals
    di :  in  std_logic_vector(1 downto 0);
    si :  in  std_logic_vector(1 downto 0);
    do :  out std_logic_vector(1 downto 0);
    so :  out std_logic_vector(1 downto 0)
    );
end;

architecture rtl of spacewire_ex is

  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);

  -- Spacewire signals
  signal swni : grspw_in_type;
  signal swno : grspw_out_type;
  signal rxclk : std_logic_vector(1 downto 0);

begin

  -- AMBA Components are instantiated here
  ...

  -- GRSPW
  sw0 : grspw
  generic map (tech => inferred, hindex => 5, pindex => 7, paddr => 7, nsync => 1,
    rmap => 1, rxunaligned => 0, rmapcrc => 0, rxclkbuftype => 0, sysfreq => 40000,
    pirq => 2, fifosize1 => 4, fifosize2 => 64, rmapbufs => 8, ft => 0, ports => 2)
  port map (rstn, clk, rxclk, apbi, apbo(7), ahbmi, ahbmo(5), swni, swno);

  phy0 : grspw_phy
  generic map (tech => inferred, rxclkbuftype => 0, scantest => 0)
  port map (rxrst => swno.rxrst, di => di(0), si => si(0),
    rxclko => rxclk(0), do => swni.d(0), ndo => swni.nd(4 downto 0),
    dconnect => swni.dconnect(1 downto 0));

  phy1 : grspw_phy
  generic map (tech => inferred, rxclkbuftype => 0)
  port map (rxrst => swno.rxrst, di => di(1), si => si(1),
    rxclko => rxclk(1), do => swni.d(1), ndo => swni.nd(9 downto 5),
    dconnect => swni.dconnect(3 downto 2));

  swni.rmapen   <= '1';
  swni.clkdiv10 <= "00000001";
  swni.tickin   <= '0';
  do(0)         <= swno.d(0);
  so(0)         <= swno.s(0);
  do(1)         <= swno.d(1);
  so(1)         <= swno.s(1);
end;
```

56.17 API

A simple Application Programming Interface (API) is provided together with the GRSPW. The API is located in $(GRLIB)/software/spw. The files are rmapapi.c, spwapi.c, rmapapi.h, spwapi.h. The spwapi.h file contains the declarations of the functions used for configuring the GRSPW and transferring data. The corresponding definitions are located in spwapi.c. The rmapapi is structured in the same manner and contains a function for building RMAP packets.

These functions could be used as a simple starting point for developing drivers for the GRSPW. The different functions are described in this section.

56.17.1 GRSPW Basic API

The basic GRSPW API is based on a struct spwvars which stores all the information for a single GRSPW core. The information includes its address on the AMBA bus as well as SpaceWire parameters such as node address and clock divisor. A pointer to this struct is used as a input parameter to all the functions. If several cores are used, a separate struct for each core is created and used when the specific core is accessed.

*Table 840.*The spwvars struct

Field	Description	Allowed range
regs	Pointer to the GRSPW	-
nospill	The nospill value used for the core.	0 - 1
rmap	Indicates whether the core is configured with RMAP. Set by spw_init.	0 - 1
rxunaligned	Indicates whether the core is configured with rxunaligned support. Set by spw_init.	0 - 1
rmapcrc	Indicates whether the core is configured with RMAPCRC support. Set by spw_init.	0 - 1
clkdiv	The clock divisor value used for the core.	0 - 255
nodeaddr	The node address value used for the core.	0 - 255
destkey	The destination key value used for the core.	0 - 255
rxmaxlen	The Receiver maximum length value used for the core.	0 - 33554431
rxpnt	Pointer to the next receiver descriptor.	0 - 127
rxchkpnt	Pointer to the next receiver descriptor that will be polled.	0 - 127
txpnt	Pointer to the next transmitter descriptor.	0 - 63
txchkpnt	Pointer to the next transmitter descriptor that will be polled.	0 - 63
timetxen	The timetxen value used for this core.	0 - 1
timerxen	The timerxen value used for this core.	0 - 1
txd	Pointer to the transmitter descriptor table.	-
rxd	Pointer to the receiver descriptor table	-

The following functions are available in the basic API:

```
int spw_setparam(int nodeaddr, int clkdiv, int destkey, int nospill, int timetxen, int
timerxen, int rxmaxlen, int spwadr, struct spwvars *spw);
```

Used for setting the different parameters in the spwvars struct. Should always be run first after creating a spwvars struct. This function only initializes the struct. Does not write anything to the SpaceWire core.

*Table 841.*Return values for spw_setparam

Value	Description
0	The function completed successfully
1	One or more of the parameters had an illegal value

*Table 842.*Parameters for spw_setparam

Parameter	Description	Allowed range
nodeaddr	Sets the node address value of the struct spw passed to the function.	0-255
clkdiv	Sets the clock divisor value of the struct spw passed to the function.	0-255
destkey	Sets the destination key of the struct spw passed to the function.	0-255
nospill	Sets the nospill value of the struct spw passed to the function.	0 - 1
timetxen	Sets the timetxen value of the struct spw passed to the function.	0 - 1
timerxen	Sets the timerxen value of the struct spw passed to the function.	0 - 1
rxmaxlen	Sets the receiver maximum length field of the struct spw passed to the function.	0 - 2^{25}-1
spwadr	Sets the address to the GRSPW core which will be associated with the struct passed to the function.	0 - 2^{32}-1

```
int spw_init(struct spwvars *spw);
```

Initializes the GRSPW core located at the address set in the struct spw. Sets the following registers: node address, destination key, clock divisor, receiver maximum length, transmitter descriptor table address, receiver descriptor table address, ctrl and dmactrl. All bits are set to the values found in the spwvars struct. If a register bit is not present in the struct it will be set to zero. The descriptor tables are allocated to an aligned area using malloc. The status register is cleared and lastly the link interface is enabled. The run state frequency will be set according to the value in clkdiv.

*Table 843.*Return values for spw_init

Value	Description
0	The function completed successfully
1	One or more of the parameters could not be set correctly or the link failed to initialize.

*Table 844.*Parameters for spw_init

Parameter	Description	Allowed range
spw	The spwvars struct associated with the GRSPW core that should be initialized.	-

```
int set_txdesc(int pnt, struct spwvars *spw);
```

Sets a new address to the transmitter descriptor table address register. Should only be used when no transmission is active. Also resets the pointers for spw_tx and spw_checktx (Explained in the section for those functions).

*Table 845.*Return values for spw_txdesc

Value	Description
0	The function completed successfully
1	The new address could not be written correctly

*Table 846.*Parameters for spw_txdesc

Parameter	Description	Allowed range
pnt	The new address to the descriptor table area	0 - 2^{32}-1
spw	Pointer to the spwvars struct associated with GRSPW core that should be configured	-

```
int set_rxdesc(int pnt, struct spwvars *spw);
```

Sets a new address to the Receiver descriptor table address register. Should only be used when no transmission is active. Also resets the pointers for spw_rx and spw_checkrx (Explained in the section for those functions).

*Table 847.*Return values for spw_rxdesc

Value	Description
0	The function completed successfully
1	The new address could not be written correctly

*Table 848.*Parameters for spw_rxdesc

Parameter	Description	Allowed range
pnt	The new address to the descriptor table area	0 - 2^{32}-1
spw	Pointer to the spwvars struct associated with GRSPW core that should be configured	-

```
void spw_disable(struct spwvars *spw);
```

Disables the GRSPW core (the link disable bit is set to ‘1’).

*Table 849.*Parameters for spw_disable

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW core that should be configured	-

```
void spw_enable(struct spwvars *spw);
```

Enables the GRSPW core (the link disable bit is set to ‘0’).

*Table 850.*Parameters for spw_enable

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW core that should be configured	-

```
void spw_start(struct spwvars *spw);
```

Starts the GRSPW core (the link start bit is set to ‘1’).

*Table 851.*Parameters for spw_start

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW core that should be configured	-

```
void spw_stop(struct spwvars *spw);
```

Stops the GRSPW core (the link start bit is set to ‘0’).

*Table 852.*Parameters for spw_start

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW core that should be configured	-

```
int spw_setclockdiv(struct spwvars *spw);
```

Sets the clock divisor register with the clock divisor value stored in the spwvars struct.

*Table 853.*Return values for spw_setclockdiv

Value	Description
0	The function completed successfully
1	The new clock divisor value is illegal.

*Table 854.*Parameters for spw_setclockdiv

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW core that should be configured	-

```
int spw_set_nodeadr(struct spwvars *spw);
```

Sets the node address register with the node address value stored in the spwvars struct.

*Table 855.*Return values for spw_set_nodeadr

Value	Description
0	The function completed successfully
1	The new node address value is illegal.

*Table 856.*Parameters for spw_set_nodeadr

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW core that should be configured	-

```
int spw_set_rxmaxlength(struct spwvars *spw);
```

Sets the Receiver maximum length register with the rxmaxlen value stored in the spwvars struct.

*Table 857.*Return values for spw_set_rxmaxlength

Value	Description
0	The function completed successfully
1	The new node address value is illegal.

*Table 858.*Parameters for spw_set_rxmaxlength

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW core that should be configured	-

```
int spw_tx(int crc, int skipcrcsize, int hsize, char *hbuf, int dsize, char *dbuf, struct
spwvars *spw);
```

Transmits a packet. Separate header and data buffers can be used. If CRC logic is available the GSPW inserts RMAP CRC values after the header and data fields if crc is set to one. This function only sets a descriptor and initiates the transmission. Spw_checktx must be used to check if the packet has been transmitted. A pointer into the descriptor table is stored in the spwvars struct to keep track of the next location to use. It is incremented each time the function returns 0.

*Table 859.*Return values for spw_tx

Value	Description
0	The function completed successfully
1	There are no free transmit descriptors currently available
2	There was illegal parameters passed to the function

*Table 860.*Parameters for spw_tx

Parameter	Description	Allowed range
crc	Set to one to append RMAP CRC after the header and data fields. Only available if hardware CRC is available in the core.	0 - 1
skipcrcsize	The number of bytes in the beginning of a packet that should not be included in the CRC calculation	0 - 15
hsize	The size of the header in bytes	0 - 255
hbuf	Pointer to the header data	-
dsize	The size of the data field in bytes	0 - 2^{24}-1
dbuf	Pointer to the data area.	-
spw	Pointer to the spwvars struct associated with GRSPW core that should transmit the packet	-

```
int spw_rx(char *buf, struct spwvars *spw);
```

Enables a descriptor for reception. The packet will be stored to buf. Spw_checkrx must be used to check if a packet has been received. A pointer in the spwvars struct is used to keep track of the next location to use in the descriptor table. It is incremented each time the function returns 0.

*Table 861.*Return values for spw_rx

Value	Description
0	The function completed successfully
1	There are no free receive descriptors currently available

*Table 862.*Parameters for spw_rx

Parameter	Description	Allowed range
buf	Pointer to the data area.	-
spw	Pointer to the spwvars struct associated with GRSPW core that should receive the packet	-

```
int spw_checkrx(int *size, struct rxstatus *rxs, struct spwvars *spw);
```

Checks if a packet has been received. When a packet has been received the size in bytes will be stored in the size parameter and status is found in the rxs struct. A pointer in the spwvars struct is used to keep track of the location in the descriptor table to poll. It is incremented each time the function returns nonzero.

*Table 863.*Return values for spw_checkrx

Value	Description
0	No packet has been received
1	A packet has been received

*Table 864.*Parameters for spw_checkrx

Parameter	Description	Allowed range
size	When the function returns 1 this variable holds the number of bytes received	-
rxs	When the function returns 1 this variable holds status information	-
spw	Pointer to the spwvars struct associated with GRSPW core that should be polled	-

*Table 865.*The rxstatus struct

Field	Description	Allowed range
truncated	Packet was truncated	0 - 1
dcrcerr	Data CRC error bit was set. Only indicates an error if the packet received was an RMAP packet.	0 - 1
hcrcerr	Header CRC error bit was se.t. Only indicates an error if the packet received was an RMAP packet.	0 - 1
eep	Packet was terminated with EEP	0 - 1

```
int spw_checktx(struct spwvars *spw);
```

Checks if a packet has been transmitted. A pointer is used to keep track of the location in the descriptor table to poll. It is incremented each time the function returns nonzero.

*Table 866.*Return values for spw_checktx

Value	Description
0	No packet has been transmitted
1	A packet has been correctly transmitted
2	A packet has been incorrectly transmitted

*Table 867.*Parameters for spw_checktx

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW core that should be polled	-

```
void send_time(struct spwvars *spw);
```

Sends a new time-code. Increments the time-counter in the GRSPW and transmits the value.

*Table 868.*Parameters for send time

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW core that should be polled	-

```
int check_time(struct spwvars *spw);
```

Check if a new time-code has been received.

*Table 869.*Return values for check_time

Value	Description
0	No time-code has been received
1	A new time-code has been received

*Table 870.*Parameters for check_time

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW core that should be polled	-

```
int get_time(struct spwvars *spw);
```

Get the current time counter value.

*Table 871.*Return values for get_time

Value	Description
0 - 63	Returns the current time counter value

*Table 872.*Parameters for get_time

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW core that should be polled	-

```
void spw_reset(struct spwvars *spw);
```

Resets the GRSPW.

*Table 873.*Parameters for spw_reset

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW core that should be reset	-

```
void spw_rmapen(struct spwvars *spw);
```

Enables hardware RMAP. Has no effect if the RMAP command handler is not available in GRSPW.

*Table 874.*Parameters for spw_rmapen

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW core that should be set	-

```
void spw_rmapdis(struct spwvars *spw);
```

Disables hardware RMAP. Has no effect if the RMAP command handler is not available in GRSPW

*Table 875.*Parameters for spw_rmapdis

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW core that should be set	-

```
int spw_setdestkey(struct spwvars *spw);
```

Set the destination key of the GRSPW. Has no effect if the RMAP command handler is not available. The value from the spwvars struct is used.

*Table 876.*Return values for spw_setdestkey

Value	Description
0	The function completed successfully
1	The destination key parameter in the spwvars struct contains an illegal value

*Table 877.*Parameters for spw_setdestkey

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW core that should be set.	-

56.17.2 GRSPW RMAP API

The RMAP API contains only one function which is used for building RMAP headers.

```
int build_rmap_hdr(struct rmap_pkt *pkt, char *hdr, int *size);
```

Builds a RMAP header to the buffer pointed to by hdr. The header data is taken from the rmap_pkt struct.

*Table 878.*Return values for build_rmap_hdr

Value	Description
0	The function completed successfully
1	One or more of the parameters contained illegal values

*Table 879.*Parameters for build_rmap_hdr

Parameter	Description	Allowed range
pkt	Pointer to a rmap_pkt struct which contains the data from which the header should be built	
hdr	Pointer to the buffer where the header will be built	
spw	Pointer to the spwvars struct associated with GRSPW core that should be set	-

*Table 880.*rmap_pkt struct fields

Field	Description	Allowed Range
type	Selects the type of packet to build.	writecmd, readcmd, rmwcmd, writerep, readrep, rmwrep
verify	Selects whether the data should be verified before writing	yes, no
ack	Selects whether an acknowledge should be sent	yes, no
incr	Selects whether the address should be incremented or not	yes, no
destaddr	Sets the destination address	0 - 255
destkey	Sets the destination key	0 - 255
srcaddr	Sets the source address	0 - 255
tid	Sets the transaction identifier field	0 - 65535
addr	Sets the address of the operation to be performed. The extended address field is currently always set to 0.	0 - 2^{32}-1
len	The number of bytes to be writte, read or read-modify-written	0 - 2^{24}-1
status	Sets the status field	0 - 11
dstspalen	Number of source path address bytes to insert before the destination address	0 - 228
dstspa	Pointer to memory holding the destination path address bytes	-
srcspalen	Number of source path address bytes to insert in a command. For a reply these bytes are placed before the return address	0 - 12
srcspa	Pointer to memory holding the source path address bytes	-

56.18 Appendix A Clarifications of the GRSPW implementation of the standard

6.3.1 page 9 RMAP draft F

"The user application at destination will be informed that there was an error in the data transferred. The source will be informed of the data error if the acknowledge bit in the command has been set."

We view the RMAP command handler as both protocol parser and user application. All commands are parsed in the first stage and various (internal) status bits are set. The next step (which can be viewed as the user application) will make the decision of how to act upon the received command from these bits. Therefore, the various errors that can occur are not externally observable.

If an error occurs when the command handler is accessing the AHB bus through the DMA interface errors will be externally observable using the AHB status register in GRLIB.

6.3.6 page 13 RMAP draft F

“The Write Command packet arrives at the destination and its header is found to be in error. This fact is added to the error statistics in the destination node.”

This text does not state how and if these statistics should be observable. At the moment the error handling is internal to the RMAP command handler and therefore no statistics are internally observable. A counter for this particular error might be added in the future.

6.3.6 page 15 RMAP draft F

"These various errors will be reported to the user application running on the destination node (Write Data Error Indication)."

Again the RMAP command handler is the user application and all these errors are handled internally.

6.5.6 page 31 RMAP draft F

"The source user application, in fact immediately rejects this as an authorisation failure as the command is trying to RMW an area of protected memory."

It should probably be destination user application instead of source. It is unclear what immediately means. Should it be rejected before any accesses are done on the bus and thus requiring the RMAP command handler to include a complete bus decoding. The GRSPW does (probably) not comply to this paragraph at the moment. If a bus error occurs a general error code will be returned.

6.5.6 page 32

"If the header of the RMW reply packet is received intact but the data field is corrupted as indicated by an incorrect data field length (too long or too short) or by a CRC error, then an error can be flagged to the application immediately (RMW Data Failure) without having to wait for an application timeout."

This is not applicable to the GRSPW since it does not handle replies. However this is practically an unnecessary comment since it is not specified in the standard in which manner received replies are indicated to the higher layers.

57 GRSPW2 - SpaceWire codec with AHB host Interface and RMAP target

57.1 Overview

The SpaceWire core provides an interface between the AHB bus and a SpaceWire network. It implements the SpaceWire standard (ECSS-E-ST-50-12C) with the protocol identification extension (ECSS-E-ST-50-51C). The optional Remote Memory Access Protocol (RMAP) target implements the ECSS standard (ECSS-E-ST-50-52C).

The SpaceWire interface is configured through a set of registers accessed through an APB interface. Data is transferred through DMA channels using an AHB master interface. The number of DMA channels is configurable from one to four.

The core can also be configured with two SpaceWire ports with manual or automatic switching between them.

There can be up to four clock domains: one for the AHB interface (system clock), one for the transmitter and one or two for the receiver depending on the number of configured ports.

The core only supports byte addressed 32-bit big-endian host systems. Transmitter outputs can be either Single Data Rate (SDR) or Double Data Rate (DDR). The receiver can be connected either to an Cobham SpaceWire transceiver or recover the data itself using a self-clocking scheme or sampling (SDR or DDR).

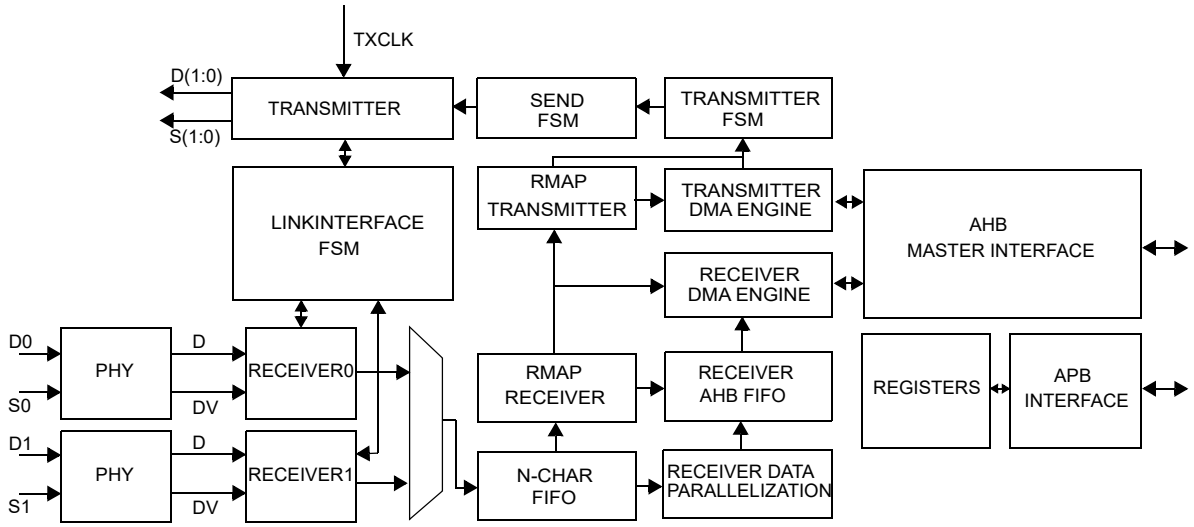


Figure 152. Block diagram

57.2 Operation

57.2.1 Overview

The main sub-blocks of the core are the link interface, the RMAP target and the AMBA interface. A block diagram of the internal structure can be found in figure 152.

The link interface consists of the receiver, transmitter, and the link interface FSM. They handle communication on the SpaceWire network. The PHY block provides a common interface for the receiver to the four different data recovery schemes and is external to this core. A short description is found in section 57.3.5. The complete documentation is found in the GRSPW2_PHY section of GRLIB IP Core User's Manual. The AMBA interface consists of the DMA engines, the AHB master interface and the APB interface. The link interface provides FIFO interfaces to the DMA engines. These FIFOs

are used to transfer N-Chars between the AMBA and SpaceWire domains during reception and transmission.

The RMAP target is an optional part of the core which can be enabled with a VHDL generic. The RMAP target handles incoming packets which are determined to be RMAP commands instead of the receiver DMA engine. The RMAP command is decoded and if it is valid, the operation is performed on the AHB bus. If a reply was requested it is automatically transmitted back to the source by the RMAP transmitter.

The link interface, DMA engines, RMAP target and AMBA interface are described in section 57.3, 57.6, 57.8 and 57.9 respectively.

57.2.2 Protocol support

The core only accepts packets with a valid destination address in the first received byte. Packets with address mismatch will be silently discarded (except in promiscuous mode, which is covered in section 57.6.10).

The second byte is sometimes interpreted as a protocol ID a described hereafter. The RMAP protocol (ID=0x1) is the only protocol handled separately in hardware while other packets are stored to a DMA channel. If the RMAP target is present and enabled all RMAP commands will be processed, executed and replied automatically in hardware. Otherwise RMAP commands are stored to a DMA channel in the same way as other packets. RMAP replies are always stored to a DMA channel. More information on the RMAP protocol support is found in section 57.8. When the RMAP target is not present or disabled, there is no need to include a protocol ID in the packets and the data can start immediately after the address.

All packets arriving with the extended protocol ID (0x00) are stored to a DMA channel. This means that the hardware RMAP target will not work if the incoming RMAP packets use the extended protocol ID. Note also that packets with the reserved extended protocol identifier (ID = 0x000000) are not ignored by the core. It is up to the client receiving the packets to ignore them.

When transmitting packets, the address and protocol-ID fields must be included in the buffers from where data is fetched. They are *not* automatically added by the core.

Figure 153 shows the packet types accepted by the core. The core also allows reception and transmission with extended protocol identifiers but without support for RMAP CRC calculations and the RMAP target.

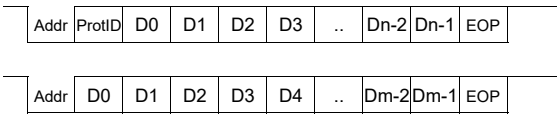


Figure 153. The SpaceWire packet types supported by the core.

When a package is received with a protocol ID = 0x02 (CCSDS) the core can, if enabled, automatically calculate and check the CCSDS/CCITT CRC-16 and 16-bit ISO-checksum (J.G. Fletcher, ISO 8473-1:1998) assuming this is included in the package.

57.2.3 Endianness

The core is designed for big-endian systems.

57.3 Link interface

The link interface handles the communication on the SpaceWire network and consists of a transmitter, receiver, a FSM and FIFO interfaces. An overview of the architecture is found in figure 152.

57.3.1 Link interface FSM

The FSM controls the link interface (a more detailed description is found in the SpaceWire standard). The low-level protocol handling (the signal and character level of the SpaceWire standard) is handled by the transmitter and receiver while the FSM handles the exchange level.

The link interface FSM is controlled through the Control register (CTRL). The link can be disabled through the CTRL.LD bit, which depending on the current state, either prevents the link interface from reaching the started state or forces it to the error-reset state. When the link is not disabled, the link interface FSM is allowed to enter the started-state when either the CTRL.LS bit is set or when a NULL character has been received and the CTRL.AS bit is set.

The state of the link interface determines which type of characters that are allowed to be transmitted, which together with the requests made from the host interfaces determine what character will be sent.

Time-codes are sent when the FSM is in the run-state and a request is made through the time-interface (described in section 57.4).

When the link interface is in the connecting- or run-state it is allowed to send FCTs. FCTs are sent automatically by the link interface when possible. This is done based on the maximum value of 56 for the outstanding credit counter and the currently free space in the receiver N-Char FIFO. FCTs are sent as long as the outstanding counter is less than or equal to 48 and there are at least 8 more empty FIFO entries than the counter value.

N-Chars are sent in the run-state when they are available from the transmitter FIFO and there are credits available. NULLs are sent when no other character transmission is requested, or when the FSM is in a state where no other transmissions are allowed.

The credit counter (incoming credits) is automatically increased when a FCTs is received, and decreased when N-Chars are transmitted. Received N-Chars are stored to the receiver N-Char FIFO for further handling by the DMA interface. Received Time-codes are handled by the time-interface.

57.3.2 Transmitter

The state of the FSM, credit counters, requests from the time-interface and requests from the DMA-interface are used to decide the next character to be transmitted. The type of character and the character itself (for N-Chars and Time-codes) to be transmitted are presented to the low-level transmitter which is located in a separate clock-domain.

This is done because one usually wants to run the SpaceWire link on a different frequency than the host system clock. The core has a separate clock input which is used to generate the transmitter clock. More information on transmitter clock generation is found in section 57.11.2. Since the transmitter often runs on high frequency clocks (> 100 MHz) as much logic as possible has been placed in the system clock domain to minimize power consumption and timing issues.

The transmitter logic in the host clock domain decides what character to send next and sets the proper control signal and presents any needed character to the low-level transmitter as shown in figure 154. The transmitter sends the requested characters and generates parity and control bits as needed. If no requests are made from the host domain, NULLs are sent as long as the transmitter is enabled. Most of the signal and character levels of the SpaceWire standard is handled in the transmitter. External LVDS drivers are needed for the data and strobe signals. The outputs can be configured as either single- or

double data rate. The latter increases maximum bitrate significantly but is not available for all technologies.

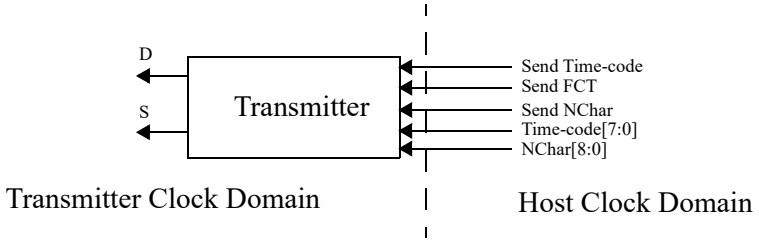


Figure 154. Schematic of the link interface transmitter.

A transmission FSM reads N-Chars for transmission from the transmitter FIFO. It is given packet lengths from the DMA interface and appends EOPs/EEPs and RMAP/CCSDS-CRC (or ISO-checksum) values if requested. When it is finished with a packet the DMA interface is notified and a new packet length value is given.

57.3.3 Receiver

The receiver detects connections from other nodes and receives characters as a bit stream recovered from the data and strobe signals by the GRSPW2_PHY module, which presents it as a data and data-valid signal. The receiver and GRSPW2_PHY are located in a separate clock domain which runs on a clock outputed by the GRSPW2_PHY. More information on the clock-generation can be found in section 57.11.2.

The receiver is activated as soon as the link interface leaves the error reset state. Then after a NULL is received it can start receiving any characters. It detects parity, escape and credit errors which causes the link interface to enter the error reset state. Disconnections are handled in the link interface part in the tx clock domain because no receiver clock is available when disconnected.

Received Characters are flagged to the host domain and the data is presented in parallel form. The interface to the host domain is shown in figure 155. L-Chars are the handled automatically by the host domain link interface part while all N-Chars are stored in the receiver FIFO for further handling. If two or more consecutive EOPs/EEPs are received all but the first one are discarded.

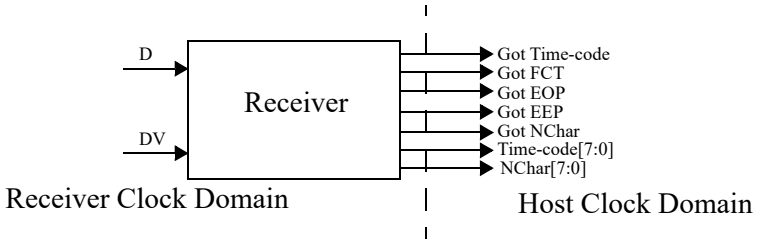


Figure 155. Schematic of the link interface receiver.

57.3.4 Dual port support

The core can be configured to include an additional SpaceWire port. With dual ports the transmitter drives an additional pair of data/strobe output signals and one extra receiver is added to handle a second pair of data/strobe input signals.

One of the ports is set as active (how the active port is selected is explained below) and the transmitter drives the data/strobe signals of the active port with the actual output values as explained in section 57.3.2. The inactive port is driven with zero on both data and strobe.

Both receivers will always be active but only the active port's interface signals (see figure 155) will be propagated to the link interface FSM. Each time the active port is changed, the link will be reset so that the new link is started in a controlled manner.

When the CTRL.NP bit is zero, the CTRL.PS bit selects the active port. When the CTRL.NP bit is set to one, the active port is automatically selected during initialization. For the latter mode, the port on which the first bit is received will be selected as the active port. If the initialization attempt fails on that port the link is reset and the active port is again sected based on which port the first bit is received.

57.3.5 Receiver PHY

The receiver supports four different input data recovery schemes: self-clocking (xor), sampling SDR, sampling DDR and the Cobham SpaceWire transceiver. These four recovery types are handled in the PHY module and data is presented to the receiver as a data and data-valid signal. This part of the receiver must often be constrained and placing it in a separate module makes this process easier with the most common synthesis tools. The input type is selected using the VHDL generic *input_type*. More information about the PHY can be found in the GRSPW2_PHY section of the GRLIP IP Core User's Manual.

57.3.6 Setting link-rate

The register field CLKDIV.CLKDIVSTART determines the link-rate during initialization (all states up to and including the connecting-state). The register is also used to calculate the link interface FSM timeouts (6.4 us and 12.8 us, as defined in the SpaceWire standard). The CLKDIV.CLKDIVSTART field should always be set so that a 10 Mbit/s link-rate is achieved during initialization. In that case the timeout values will also be calculated correctly.

To achieve a 10 Mbit/s link-rate, the CLKDIV.CLKDIVSTART field should be set according to the following formulas:

With single data rate (SDR) outputs:

CLKDIV.CLKDIVSTART = (<frequency in MHz of TXCLK> / 10) - 1

With double data rate (DDR) outputs, or when connected to Cobham SpaceWire transceiver:

CLKDIV.CLKDIVSTART = (2 x <frequency in MHz of TXCLK> / 10) - 1

The link-rate in run-state is controlled with the run-state divisor, the CLKDIV.CLKDIVRUN register field. The link-rate in run-state is calculated according to the following formulas:

With SDR outputs:

<link-rate in Mbits/s> = <frequency in MHz of TXCLK> / (CLKDIV.CLKDIVRUN+1)

With DDR outputs / Cobham SpaceWire transceiver:

<link-rate in Mbits/s> = 2 x <frequency in MHz of TXCLK> / (CLKDIV.CLKDIVRUN+1)

The value of CLKDIV.CLKDIVRUN only affects the link-rate in run-state, and does not affect the 6.4 us or 12.8 us timeouts values.

Note that when using DDR ouputs, or when connected to Cobham SpaceWire transceiver, there is a limitation in the usable clock divisor values. All even values (except 0) will result in the same bitrate as the one higher odd number.

An example of clock divisor and resulting link-rate, with a TXCLK frequency of 50 MHz, is shown in the table 881. Also see 57.11.2 for information on clock requirements.

*Table 881.*SpaceWire link-rate example with 50 MHz TXCLK

Clock divisor value	Link-rate in Mbit/s	
	SDR outputs	DDR outputs / Cobham SpaceWire transceiver
0	50	100
1	25	50
2	16.67	25
3	12.5	25
4	10	16.67
5	8.33	16.67
6	7.14	12.5
7	6.25	12.5
8	5.56	10
9	5	10

57.4 Time-code distribution

Time-codes are control codes that consists of two control flags (bits 7:6) and a time value (bits 5:0), and they are used to distribute time over the SpaceWire network. The current time value (value of latest received or transmitted time-code), and control flags, can be read from the Time-code register (TC).

57.4.1 Receiving time-codes

When a control-code is received, and either the control flags (bits 7:6) have value “00”, or both control flag filtering and interrupt receive is disabled (CTRL.TF bit, and INTCTRL.IR bit both set to 0), then the received control code is considered to be a Time-Code. If Time-Code reception is enabled (CTRL.TR bit set to 1) then the received time value is stored in the TC.TIMECNT field. If the received time value equals TC.TIMECNT+1 (modulo 64), then the Time-Code is considered valid.

When a valid Time-Code is received, in addition to the time value being updated, the received control flags are stored to the TC.TCTRL field. Also, when a valid Time-Code is received, the TICKOUT output signal is asserted for one system clock cycle, the STS.TO bit is set to 1, and an AMBA interrupt is generated if the CTRL.IE bit and CTRL.TQ bit are both set to 1.

For all received control codes, Time-Codes or not, the control flags together with the time value are outputted on the TIMEOUT[7:0] signals, and the TICKOUTRAW signal is asserted for one system clock cycle.

57.4.2 Transmitting time-codes

Time-codes can be transmitted either through the AMBA APB registers or through the signals TICKIN, TICKINRAW, TIMEIN, and TICKINDONE.

In order to send a Time-code, Time-Code transmission must be enabled by setting the CTRL.TT bit to 1. To transmit a time-code through the register interface the CTRL.TI bit should be written to 1. When the bit is written the current time value (TC.TIMECNT field) is incremented, and a Time-Code consisting of the new time value together with the current control flags (TC.TCTRL field) is sent. The CTRL.TI bit will stay high until the Time-Code has been transmitted. If time-code transmission is disabled, writing the CTRL.TI bit has no effect.

To transmit a time-code using the TICKIN signal the sender must wait until the TICKINDONE output is low, then assert TICKIN. When TICKINDONE is asserted again, the TICKIN signal should be de-asserted the same cycle. Following this procedure will make the core transmit a Time-Code consisting of the current control flags and the current time value + 1 (modulo 64). This also requires that time-code transmission is enabled through the CTRL.TT bit.

To transmit a Time-Code using the TICKINRAW signal the sender must wait until TICKINDONE is low, then assert TICKINRAW and place the value of the Time-Code to be sent on the TIMEIN[7:0] signals. When TICKINDONE is asserted again, the TICKINRAW signal should be de-asserted the same cycle. Note that sending Time-Codes by using TICKINRAW does not require that Time-Code transmission is enabled from the Control register. However, in order to send Time-Codes with control flags different than “00”, interrupt transmit must be disabled (INTCTRL.IT bit set to 0). If interrupt transmit is enabled then control codes “10” are interpreted as interrupt-codes, while control codes “01” and “11” are discarded.

Note that the link interface must be in run-state in order to be able to send a Time-Code.

57.5 Interrupt distribution

The core supports interrupt distribution functionality. Whether or not this functionality is implemented is indicated by the CTRL.ID bit, and the number of supported interrupt numbers is indicated by the INTCFG.NUMINT field. Either 1, 2, 4, or 32 interrupt numbers (in the range 0-31) can be supported. When less than 32 interrupt numbers are supported it is programmable through the INTCFG register which interrupt numbers in the range 0-31 that are allowed to be sent and received. When extended interrupt mode is enabled (INTCFG.EE bit set to 1), the supported interrupt number in “interrupt mode” is extended to 0-63).

The interrupts are distributed as control codes with the control flags (bits 7:6) set to “10”. Bit 5 of the control code specifies if the code is an interrupt-code (bit 5 = ‘0’) or an interrupt-acknowledge-code (bit 5 = ‘1’). An interrupt-code is generated by the source of the interrupt event, while the interrupt-acknowledge-code is sent by the interrupt handler for the corresponding interrupt number. When extended interrupt mode is enabled (INTCFG.EE bit set to 1), then interrupt-acknowledge-code is interpret as interrupt-codes in the range 32-63.

An Interrupt distribution ISR register holds the current state of all the interrupt numbers in the SpaceWire network. A bit in the ISR register is set to 1 when an interrupt-code with the corresponding interrupt number is received / transmitted, and the bit is set to 0 when an interrupt-acknowledge-code with the corresponding interrupt number is received / transmitted.

Each interrupt number also has its own timer that is used to clear the ISR bit if an interrupt-acknowledge-code is not received before the timer expires. There is also a timer for each interrupt-number that controls the minimum time between and interrupt-code and interrupt-acknowledge-code (and vice versa), in order to allow propagation of the codes through the whole network before a new code with the same interrupt number is sent.

57.5.1 Interrupt distribution timers

Each interrupt number has three corresponding timers, called the ISR timer, INT/ACK-timer, and ISR change timer. Whether or not these timers are implemented in hardware, and how large they are, can be detected by probing the ISRTIMER, IATIMER, and ICTIMER registers respectively.

If the ISR timers are enabled (ISRTIMER.EN bit set to 1), the ISR timer is started and reloaded with the value from the ISRTIMER.RL field each time an interrupt-code is received such that the corresponding ISR bit is set to 1. If a matching interrupt-acknowledge-code is received, the corresponding ISR timer is stopped. If the ISR timer expires before an interrupt-acknowledge-code is received, the corresponding ISR bit is cleared. The purpose of the ISR timer is to recover from situations where an interrupt-acknowledge-code is lost. If an interrupt-acknowledge-code is lost and there were no ISR

timer, then the corresponding ISR bit would stay set forever, and prevent future interrupt-codes with that interrupt number to be distributed. It is important to configure the reload value for the ISR timer correctly. The reload value shall not be less than the worst network propagation delay for the interrupt-code, plus the maximum delay in the interrupt handler, plus the worst network propagation delay for the interrupt-acknowledge-code. Note that use of the ISR timer is mandatory, so if the hardware timers are either disabled or not implemented, software must handle the timers.

The INT/ACK-timer is used to control the minimum time between an interrupt-code and interrupt-acknowledge-code with the same interrupt number, and vice versa. The purpose of the INT/ACK-timer is to make sure that each interrupt- / interrupt-acknowledge-code gets enough time to propagate through the complete network before the next interrupt- / interrupt-acknowledge-code is sent, ensuring that no interrupt- / interrupt-acknowledge-code is received out of order. If the INT/ACK-timers are enabled (IATIMER.EN bit set to 1), then each time an interrupt- / interrupt-acknowledge-code is received the corresponding INT/ACK-timer is started and reloaded with the value from the IATIMER.RL field. As long as the timer is running, an interrupt- / interrupt-acknowledge-code with that interrupt number will not be sent.

The ISR change timer is used to control the minimum time between two consecutive changes to the same ISR bit. The purpose of the timer is to protect against unexpected occurrences of interrupt- / interrupt-acknowledge-codes that could occur, for example, due to a network malfunction or a babbling idiot. If the ISR change timers are enabled (ICTIMER.EN bit set to 1), then the timer for an ISR bit is started and reloaded with the value from the ICTIMER.RL field each time a received interrupt- / interrupt-acknowledge-code makes the ISR bit change value. Until the timer has expired, the corresponding ISR bit is not allowed to change value, and any received interrupt- / interrupt-acknowledge-codes with that interrupt number are discarded.

57.5.2 Receiving interrupt- / interrupt-acknowledge-codes

When a control code with control flags set to “10” is received, and interrupt receive is enable (IR bit in Interrupt distribution control register set to 1), the control code is considered an interrupt-code if bit 5 is 0, and an interrupt-acknowledge-code if bit 5 is 1. If an interrupt-code is received and the interrupt number’s corresponding ISR bit is already set to 1, or an interrupt-acknowledge-code when the ISR bit is 0, then the received interrupt- / interrupt-acknowledge-code is discarded without any further action.

When an interrupt-code is received, and the corresponding ISR bit is 0, the ISR bit is set to 1. If the interrupt number’s corresponding bit in the Interrupt tick-out mask register is set to 1 then the corresponding bit in the Interrupt-code receive register is set to 1, the TICKOUT signal is asserted for one clock cycle (if the INTCTRL.IT bit is 1), and an AMBA interrupt is generated (if the IE bit in the Control register, and IQ bit in the Interrupt distribution control register are both set to 1). If the interrupt number’s corresponding bit in the Interrupt-code auto acknowledge mask register is set to 1, then an interrupt-acknowledge-code will be automatically sent once the INT/ACK-timer has expired, and the ISR bit will be cleared again.

When an interrupt-acknowledge-code is received, and the corresponding ISR bit is 1, the ISR bit is set to 0. If the interrupt number’s corresponding bit in the Interrupt tick-out mask register is set to 1, and the interrupt-code that made the ISR bit get set to 1 in the first place was sent by software (through register access), then the corresponding bit in the Interrupt-acknowledge-code receive register is set to 1. The TICKOUT signal is asserted for one clock cycle as well (if the INTCTRL.AT bit is 1), and an AMBA interrupt is generated (if the IE bit in the Control register, and IQ bit in the Interrupt distribution control register are both set to 1).

Note that all received control codes, interrupt- / interrupt-acknowledge-codes or not, are outputted on the TIMEOUT[7:0] signals, and the TICKOUTRAW signal is asserted for one clock cycle.

For more details regarding interrupt- / interrupt-acknowledge-code reception, please see the description of the interrupt distribution registers in section 57.12.

57.5.3 Transmitting interrupt- / interrupt-acknowledge-codes

Interrupt- / interrupt-acknowledge-codes can be transmitted either through the AMBA APB registers or through the signals TICKINRAW, TIMEIN, and TICKINDONE.

To transmit an interrupt- / interrupt-acknowledge-code through the register interface the II bit in the Interrupt distribution control register should be written to 1. When the bit is written the value of the TXINT field determine which interrupt- / interrupt-acknowledge-code that will be sent.

To transmit an interrupt- / interrupt-acknowledge-code using the TICKINRAW signal the sender must wait until TICKINDONE is low, then assert TICKINRAW and place the value of the interrupt- / interrupt-acknowledge-code to be sent on the TIMEIN[7:0] signals. When TICKINDONE is asserted again, the TICKINRAW signal should be de-asserted the same cycle.

Both methods of sending an interrupt- / interrupt-acknowledge-code requires that interrupt transmission is enabled (IT bit in Interrupt distribution control register set to 1). The actual sending of the interrupt- / interrupt-acknowledge-code is delayed until the corresponding INT/ACK-timer has expired.

For more details regarding interrupt- / interrupt-acknowledge-code transmission, please see the description of the interrupt distribution registers in section 57.12.

57.5.4 Interrupt-code generation

Interrupt-codes can be generated automatically due to a number of internal events. Which events that should force an interrupt-code to be sent, and what interrupt-number to use, is controlled from the Interrupt distribution control register, and the DMA control/status register. Interrupt transmission must also be enabled (IT bit in Interrupt distribution control register) for interrupt-codes to be generated. Internally generated interrupt-codes are sent in the same manner as interrupt-codes transmitted through the register interface and the TICKINRAW signal, as described in section 57.5.3. For more details regarding interrupt-code generation please see the description of the Interrupt distribution control register and DMA control/status register in section 57.12.

57.6 Receiver DMA channels

The receiver DMA engine handles reception of data from the SpaceWire network to different DMA channels.

57.6.1 Address comparison and channel selection

Packets are received to different channels based on the address and whether a channel is enabled or not. When the receiver N-Char FIFO contains one or more characters, N-Chars are read by the receiver DMA engine. The first character is interpreted as the logical address and is compared with the addresses of each channel starting from 0. The packet will be stored to the first channel with an matching address. The complete packet including address and protocol ID but excluding EOP/EEP is stored to the memory address pointed to by the descriptors (explained later in this section) of the channel.

Each SpaceWire address register has a corresponding mask register. Only bits at an index containing a zero in the corresponding mask register are compared. This way a DMA channel can accept a range of addresses. There is a Default address register which is used for address checking in all implemented DMA channels that do not have separate addressing enabled and for RMAP commands in the RMAP target. With separate addressing enabled the DMA channels' own address/mask register pair is used instead.

If an RMAP command is received it is only handled by the target if the Default address register (including mask) matches the received address. Otherwise the packet will be stored to a DMA channel if one or more of them has a matching address. If the address does not match neither the default address nor one of the DMA channels' separate register, the packet is still handled by the RMAP tar-

get if enabled since it has to return the invalid address error code. The packet is only discarded (up to and including the next EOP/EEP) if an address match cannot be found and the RMAP target is disabled.

Packets, other than RMAP commands, that do not match neither the default address register nor the DMA channels' address register will be discarded. Figure 156 shows a flowchart of packet reception.

At least 2 non EOP/EEP N-Chars needs to be received for a packet to be stored to the DMA channel unless the promiscuous mode is enabled in which case 1 N-Char is enough. If it is an RMAP packet with hardware RMAP enabled 3 N-Chars are needed since the command byte determines where the packet is processed. Packets smaller than these sizes are discarded.

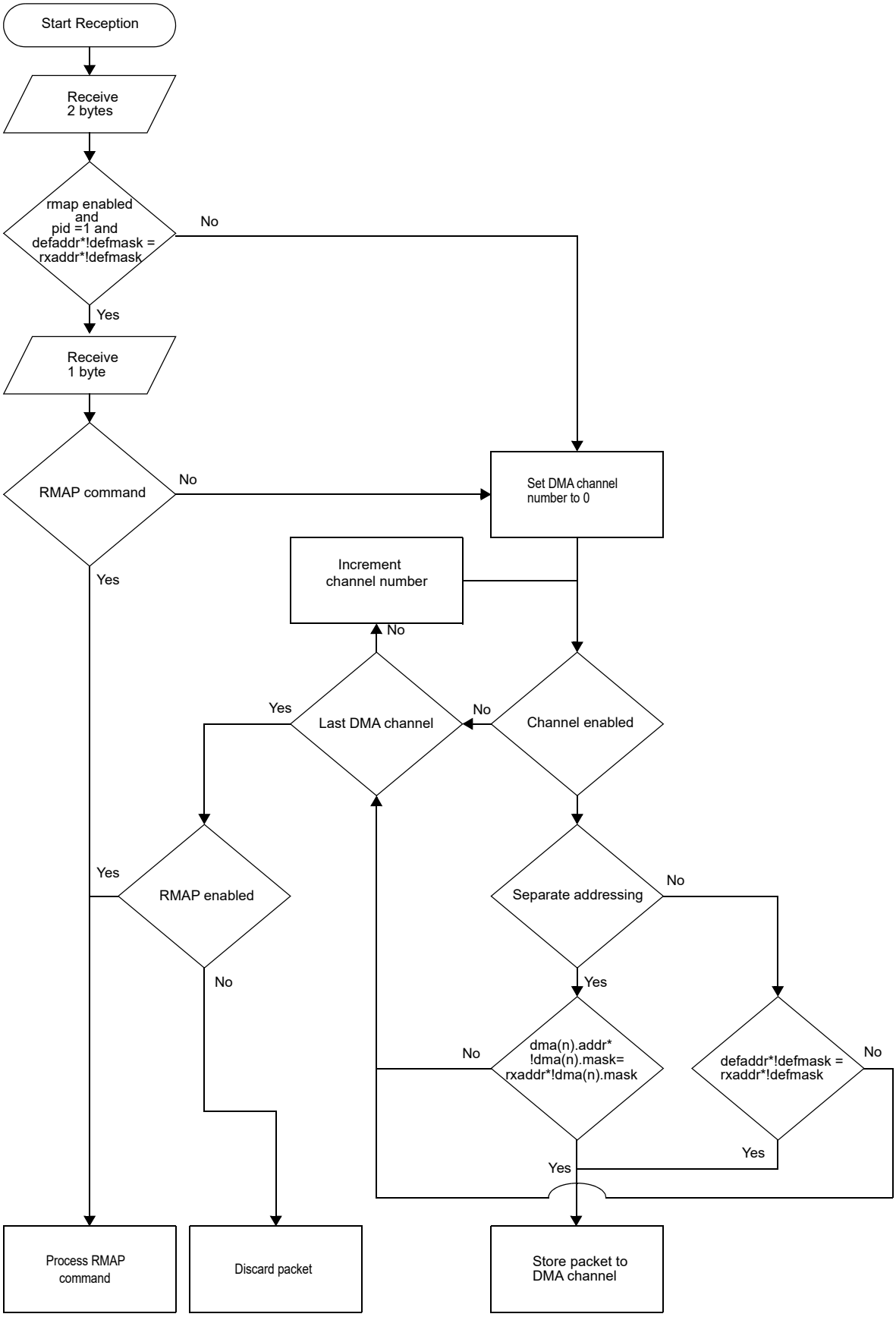


Figure 156. Flow chart of packet reception.

57.6.2 Basic functionality of a channel

Reception is based on descriptors located in a consecutive area in memory that hold pointers to buffers where packets should be stored. When a packet arrives at the core the channel which should receive it is first determined as described in the previous section. A descriptor is then read from the channels' descriptor area and the packet is stored to the memory area pointed to by the descriptor. Lastly, status is stored to the same descriptor and increments the descriptor pointer to the next one. The following sections will describe DMA channel reception in more detail.

57.6.3 Setting up the core for reception

A few registers need to be initialized before reception to a channel can take place. First the link interface need to be put in the run state before any data can be sent. The DMA channel has a maximum length register which sets the maximum packet size in bytes that can be received to this channel. Larger packets are truncated and the excessive part is spilled. If this happens an indication will be given in the status field of the descriptor. The minimum value for the receiver maximum length field is 4 and the value can only be incremented in steps of four bytes up to the maximum value 33554428. If the maximum length is set to zero the receiver will *not* function correctly.

Either the Default address register or the channel specific address register (the accompanying mask register must also be set) needs to be set to hold the address used by the channel. A control bit in the DMA channel control register determines whether the channel should use default address and mask registers for address comparison or the channel's own registers. Using the default register the same address range is accepted as for other channels with default addressing and the RMAP target while the separate address provides the channel its own range. If all channels use the default registers they will accept the same address range and the enabled channel with the lowest number will receive the packet.

Finally, the descriptor table and Control register must be initialized. This will be described in the two following sections.

57.6.4 Setting up the descriptor table address

The core reads descriptors from an area in memory pointed to by the receiver descriptor table address register. The register consists of a base address and a descriptor selector. The base address points to the beginning of the area and must start on an address that is aligned to the size of the descriptor table. The size of the descriptor table can be determined from the formula: STS.NRXD*8. The STS.NRXD field shows the number of entries in the descriptor table, and each descriptor size is 8 bytes.

The descriptor selector points to individual descriptors and is increased by 1 when a descriptor has been used. When the selector reaches the upper limit of the area it wraps to the beginning automatically. It can also be set to wrap at a specific descriptor before the upper limit by setting the wrap bit in the descriptor. The idea is that the selector should be initialized to 0 (start of the descriptor area) but it can also be written with another 8 bytes aligned value to start somewhere in the middle of the area. It will still wrap to the beginning of the area.

If one wants to use a new descriptor table the receiver enable bit has to be cleared first. When the rxactive bit for the channel is cleared it is safe to update the descriptor table register. When this is finished and descriptors are enabled the receiver enable bit can be set again.

57.6.5 Enabling descriptors

As mentioned earlier one or more descriptors must be enabled before reception can take place. Each descriptor is 8 byte in size and the layout can be found in the tables below. The descriptors should be written to the memory area pointed to by the receiver descriptor table address register. When new descriptors are added they must always be placed after the previous one written to the area. Otherwise they will not be noticed.

A descriptor is enabled by setting the address pointer to point at a location where data can be stored and then setting the enable bit. The WR bit can be set to cause the selector to be set to zero when reception has finished to this descriptor. IE should be set if an interrupt is wanted when the reception has finished. The DMA control register interrupt enable bit must also be set for an interrupt to be generated.

The descriptor packet address should be word aligned. All accesses on the bus are word accesses so complete words will always be overwritten regardless of whether all 32-bit contain received data. Also if the packet does not end on a word boundary the complete word containing the last data byte will be overwritten. If the *rxunaligned* or *rmap* VHDL generics are set to 1, this restriction is removed and any number of bytes can be received to any packet address without excessive bytes being overwritten.

*Table 882.*GRSPW2 receive descriptor word 0 (address offset 0x0)

31	30	29	28	27	26	25	24 ... 0
TR	DC	HC	EP	IE	WR	EN	PACKETLENGTH

31	Truncated (TR) - Packet was truncated due to maximum length violation.
30	Data CRC (DC) - Unused. 1 if a CRC error was detected for the data and 0 otherwise. If the Protocol ID of the received package is 0x02 a 1 indicates a CCSDS/CCITT CRC-16 error was detected.
29	Header CRC (HC) - 1 if a CRC error was detected for the header and 0 otherwise. If the Protocol ID of the received package is 0x02 a 1 indicates a 16-bit ISO-Checksum error was detected.
28	EEP termination (EP) - This packet ended with an Error End of Packet character.
27	Interrupt enable (IE) - If set, an interrupt will be generated when a packet has been received if the receive interrupt enable bit in the DMA channel control register is set.
26	Wrap (WR) - If set, the next descriptor used by the GRSPW will be the first one in the descriptor table (at the base address). Otherwise the descriptor pointer will be increased with 0x8 to use the descriptor at the next higher memory location. The descriptor table is limited to 1 kbytes in size and the pointer will be automatically wrap back to the base address when it reaches the 1 kbytes boundary.
25	Enable (EN) - Set to one to activate this descriptor. This means that the descriptor contains valid control values and the memory area pointed to by the packet address field can be used to store a packet.
24: 0	Packet length (PACKETLENGTH) - The number of bytes received to this buffer. Only valid after EN has been set to 0 by the GRSPW.

*Table 883.*GRSPW2 receive descriptor word 1 (address offset 0x4)

31 ... 0
PACKETADDRESS

31: 0	Packet address (PACKETADDRESS) - The address pointing at the buffer which will be used to store the received packet. If the *rxunaligned* and *rmap* VHDL generics are both set to zero only bit 31 to 2 are used.

57.6.6 Setting up the DMA control register

The final step to receive packets is to set the control register in the following steps: The receiver must be enabled by setting the rxen bit in the DMA control register (see section 57.12). This can be done anytime and before this bit is set nothing will happen. The rxdescav bit in the DMA control register is then set to indicate that there are new active descriptors. This must always be done after the descriptors have been enabled or the core might not notice the new descriptors. More descriptors can be activated when reception has already started by enabling the descriptors and writing the rxdescav bit. When these bits are set reception will start immediately when data is arriving.

57.6.7 The effect to the control bits during reception

When the receiver is disabled all packets going to the DMA-channel are discarded if the packet's address does not fall into the range of another DMA channel. If the receiver is enabled and the address falls into the accepted address range, the next state is entered where the rxdescav bit is checked. This bit indicates whether there are active descriptors or not and should be set by the external application using the DMA channel each time descriptors are enabled as mentioned above. If the rxdescav bit is '0' and the nospill bit is '0' the packets will be discarded. If nospill is '1' the core waits until rxdescav is set and the characters are kept in the N-Char fifo during this time. If the fifo becomes full further N-char transmissions are inhibited by stopping the transmission of FCTs.

When rxdescav is set the next descriptor is read and if enabled the packet is received to the buffer. If the read descriptor is not enabled, rxdescav is set to '0' and the packet is spilled depending on the value of nospill.

The receiver can be disabled at any time and will stop packets from being received to this channel. If a packet is currently received when the receiver is disabled the reception will still be finished. The rxdescav bit can also be cleared at any time. It will not affect any ongoing receptions but no more descriptors will be read until it is set again. Rxdescav is also cleared by the core when it reads a disabled descriptor.

57.6.8 Status bits

When the reception of a packet is finished the enable bit in the current descriptor is set to zero. When enable is zero, the status bits are also valid and the number of received bytes is indicated in the length field. The DMA control register contains a status bit which is set each time a packet has been received. The core can also be made to generate an interrupt for this event.

RMAP CRC logic is included in the implementation if the *rmapcrc* or *rmap* VHDL generics are set to 1. The RMAP CRC calculation is always active for all received packets and all bytes except the EOP/EEP are included. The packet is always assumed to be an RMAP packet and the length of the header is determined by checking byte 3 which should be the command field. The calculated CRC value is then checked when the header has been received (according to the calculated number of bytes) and if it is non-zero the HC bit is set indicating a header CRC error.

The CRC value is not set to zero after the header has been received, instead the calculation continues in the same way until the complete packet has been received. Then if the CRC value is non-zero the DC bit is set indicating a data CRC error. This means that the core can indicate a data CRC error even if the data field was correct when the header CRC was incorrect. However, the data should not be used when the header is corrupt and therefore the DC bit is unimportant in this case. When the header is not corrupted the CRC value will always be zero when the calculation continues with the data field and the behaviour will be as if the CRC calculation was restarted

If the received packet is not of RMAP type the header CRC error indication bit cannot be used. It is still possible to use the DC bit if the complete packet is covered by a CRC calculated using the RMAP CRC definition. This is because the core does not restart the calculation after the header has been received but instead calculates a complete CRC over the packet. Thus any packet format with one CRC at the end of the packet calculated according to RMAP standard can be checked using the DC bit.

CCSDS/CCITT CRC-16 and 16-bit ISO Checksum logic is included in the implementation when the VHDL generct ccsdscrc are set to 1. When a package is received with a protocol ID equal to 0x02 (CCSDS), the core will use the CCSDS CRC/ISO-checksum logic instead of RMAP CRC logic to calculate the CRC. The result is presented by the same status bits as for the RMAP head/data CRC error, but the interpretation of these bits is changed to ISO-checksum/CCSDS CRC error instead.

If the packet is neither of RMAP type nor of the type above with RMAP CRC at the end, then both the HC and DC bits should be ignored.

57.6.9 Error handling

If a packet reception needs to be aborted because of congestion on the network, the suggested solution is to set link disable to '1'. Unfortunately, this will also cause the packet currently being transmitted to be truncated but this is the only safe solution since packet reception is a passive operation depending on the transmitter at the other end. A channel reset bit could be provided but is not a satisfactory solution since the untransmitted characters would still be in the transmitter node. The next character (somewhere in the middle of the packet) would be interpreted as the node address which would probably cause the packet to be discarded but not with 100% certainty. Usually this action is performed when a reception has stuck because of the transmitter not providing more data. The channel reset would not resolve this congestion.

If an AHB error occurs during reception the current packet is spilled up to and including the next EEP/EOP and then the currently active channel is disabled and the receiver enters the idle state. A bit in the channels control/status register is set to indicate this condition.

57.6.10 Promiscuous mode

The core supports a promiscuous mode where all the data received is stored to the first DMA channel enabled regardless of the node address and possible early EOPs/EEPs. This means that all non-EOP/EEP N-Chars received will be stored to the DMA channel. The rxmaxlength register is still checked and packets exceeding this size will be truncated.

RMAP commands will still be handled by the hardware RMAP target when promiscuous mode is enabled, if the RMAP enable bit in the core's Control register is set. If the RMAP enable bit is cleared, RMAP commands will also be stored to a DMA channel.

57.7 Transmitter DMA channels

The transmitter DMA engine handles transmission of data from the DMA channels to the SpaceWire network. Each receive channel has a corresponding transmit channel which means there can be up to 4 transmit channels. It is however only necessary to use a separate transmit channel for each receive channel if there are also separate entities controlling the transmissions. The use of a single channel with multiple controlling entities would cause them to corrupt each other's transmissions. A single channel is more efficient and should be used when possible.

Multiple transmit channels with pending transmissions are arbitrated in a round-robin fashion.

57.7.1 Basic functionality of a channel

A transmit DMA channel reads data from the AHB bus and stores them in the transmitter FIFO for transmission on the SpaceWire network. Transmission is based on the same type of descriptors as for the receiver and the descriptor table has the same alignment and size restrictions. When there are new descriptors enabled the core reads them and transfer the amount data indicated.

57.7.2 Setting up the core for transmission

Four steps need to be performed before transmissions can be done with the core. First the link interface must be enabled and started by writing the appropriate value to the ctrl register. Then the address to the descriptor table needs to be written to the transmitter descriptor table address register and one or more descriptors must also be enabled in the table. Finally, the txen bit in the DMA control register is written with a one which triggers the transmission. These steps will be covered in more detail in the next sections.

57.7.3 Enabling descriptors

The core reads descriptors from an area in memory pointed to by the transmit descriptor table address register. The register consists of a base address and a descriptor selector. The base address points to

the beginning of the area and must start on an address that is aligned to the size of the descriptor table. The size of the descriptor table can be determined from the formula: STS.NTXD*16. The STS.NTXD field shows the number of entries in the descriptor table, and each descriptor size is 16 bytes.

To transmit packets one or more descriptors have to be initialized in memory which is done in the following way: The number of bytes to be transmitted and a pointer to the data has to be set. There are two different length and address fields in the transmit descriptors because there are separate pointers for header and data. If a length field is zero the corresponding part of a packet is skipped and if both are zero no packet is sent. The maximum header length is 255 bytes and the maximum data length is 16 Mbyte - 1. When the pointer and length fields have been set the enable bit should be set to enable the descriptor. This must always be done last. The other control bits must also be set before enabling the descriptor.

The transmit descriptors are 16 bytes in size so the maximum number in a single table is 64. The different fields of the descriptor together with the memory offsets are shown in the tables below.

The HC bit should be set if RMAP CRC should be calculated and inserted for the header field and correspondingly the DC bit should be set for the data field. This field is only used by the core when the CRC logic is available (*rmap* or *rmapcrc* VHDL generic set to 1). The header CRC will be calculated from the data fetched from the header pointer and the data CRC is generated from data fetched from the data pointer. The CRCs are appended after the corresponding fields. The NON-CRC bytes field is set to the number of bytes in the beginning of the header field that should not be included in the CRC calculation.

When the CCSDS/CCITT CRC-16 and 16-bit ISO-checksum logic is available (VHDL generic ccsdscrc set to 1) the core uses the CRC-type filed to determine which CRC logic should be used to calculate the data checksum. When the CCSDS CRC/ISO-checksum logic is not available, the CRC-type field is assumed to be 00 (RMAP CRC).

The CRCs are sent even if the corresponding length is zero, but when both lengths are zero no packet is sent not even an EOP.

57.7.4 Starting transmissions

When the descriptors have been initialized, the transmit enable bit in the DMA control register has to be set to tell the core to start transmitting. New descriptors can be activated in the table on the fly (while transmission is active). Each time a set of descriptors is added the transmit enable bit in the corresponding DMA channel control/status register should be set. This has to be done because each time the core encounters a disabled descriptor this register bit is set to 0.

*Table 884.*GRSPW2 transmit descriptor word 0 (address offset 0x0)

31 20	19 18	17	16	15	14	13	12	11 8	7 0
RESERVED	CRC-T	DC	HC	LE	IE	WR	EN	NONCRCLEN	HEADERLEN

31: 20	RESERVED
19: 18	CRC type (CRC-T) - Defines the type of data CRC to use. 00: RMAP CRC 01: CCSDS/CCITT CRC-16 10: 16-bit ISO Checksum (J.G. Fletcher, ISO 8473-1:1998) 11: Reserved
17	Append data CRC (DC) - Unused. Append CRC calculated according to the RMAP specification (or CCSDS/CCITT CRC-16 or 16-bit ISO-checksum when available) after the data sent from the data pointer. The CRC covers all the bytes from this pointer. A null CRC will be sent if the length of the data field is zero.
16	Append header CRC (HC) - Append CRC calculated according to the RMAP specification after the data sent from the header pointer. The CRC covers all bytes from this pointer except a number of bytes in the beginning specified by the non-crc bytes field. The CRC will not be sent if the header length field is zero.

*Table 884.*GRSPW2 transmit descriptor word 0 (address offset 0x0)

15	Link error (LE) - A Link error occurred during the transmission of this packet.
14	Interrupt enable (IE) - If set, an interrupt will be generated when the packet has been transmitted and the transmitter interrupt enable bit in the DMA control register is set.
13	Wrap (WR) - If set, the descriptor pointer will wrap and the next descriptor read will be the first one in the table (at the base address). Otherwise the pointer is increased with 0x10 to use the descriptor at the next higher memory location.
12	Enable (EN) - Enable transmitter descriptor. When all control fields (address, length, wrap and crc) are set, this bit should be set. While the bit is set the descriptor should not be touched since this might corrupt the transmission. The core clears this bit when the transmission has finished.
11: 8	Non-CRC bytes (NONCRCLEN)- Sets the number of bytes in the beginning of the header which should not be included in the CRC calculation. This is necessary when using path addressing since one or more bytes in the beginning of the packet might be discarded before the packet reaches its destination.
7: 0	Header length (HEADERLEN) - Header Length in bytes. If set to zero, the header is skipped.

*Table 885.*GRSPW2 transmit descriptor word 1 (address offset 0x4)

31	0
HEADERADDRESS	

31: 0	Header address (HEADERADDRESS) - Address from where the packet header is fetched. Does not need to be word aligned.

*Table 886.*GRSPW2 transmit descriptor word 2 (address offset 0x8)

31 24	23 0
RESERVED	DATALEN

31: 24	RESERVED
23: 0	Data length (DATALEN) - Length in bytes of data part of packet. If set to zero, no data will be sent. If both data- and header-lengths are set to zero no packet will be sent.

*Table 887.*GRSPW2 transmit descriptor word 3(address offset 0xC)

31	0
DATAADDRESS	

31: 0	Data address (DATAADDRESS) - Address from where data is read. Does not need to be word aligned.

57.7.5 The transmission process

When the transmitter enable bit in the DMA channel control/status register is set the core starts reading descriptors immediately. The number of bytes indicated are read and transmitted. When a transmission has finished, status will be written to the first field of the descriptor and a packet sent bit is set in the DMA control register. If an interrupt was requested it will also be generated. Then a new descriptor is read and if enabled a new transmission starts, otherwise the transmit enable bit is cleared and nothing will happen until it is enabled again.

57.7.6 The descriptor table address register

The internal pointer which is used to keep the current position in the descriptor table can be read and written through the APB interface. This pointer is set to zero during reset and is incremented each time a descriptor is used. It wraps automatically when the limit for the descriptor table is reached, or it can be set to wrap earlier by setting a bit in the current descriptor.

The descriptor table register can be updated with a new table anytime when no transmission is active. No transmission is active if the transmit enable bit is zero and the complete table has been sent or if

the table is aborted (explained below). If the table is aborted one has to wait until the transmit enable bit is zero before updating the table pointer.

57.7.7 Error handling

Abort Tx

The DMA control register contains a bit called Abort TX which if set causes the current transmission to be aborted, the packet is truncated and an EEP is inserted. This is only useful if the packet needs to be aborted because of congestion on the SpaceWire network. If the congestion is on the AHB bus this will not help (This should not be a problem since AHB slaves should have a maximum of 16 wait-states). The aborted packet will have its LE bit set in the descriptor. The transmit enable register bit is also cleared and no new transmissions will be done until the transmitter is enabled again.

AHB error

When an AHB error is encountered during transmission the currently active DMA channel is disabled and the transmitter goes to the idle mode. A bit in the DMA channel's control/status register is set to indicate this error condition and, if enabled, an interrupt will also be generated. Further error handling depends on what state the transmitter DMA engine was in when the AHB error occurred. If the descriptor was being read the packet transmission had not been started yet and no more actions need to be taken.

If the AHB error occurs during packet transmission the packet is truncated and an EEP is inserted. Lastly, if it occurs when status is written to the descriptor the packet has been successfully transmitted but the descriptor is not written and will continue to be enabled (this also means that no error bits are set in the descriptor for AHB errors).

The client using the channel has to correct the AHB error condition and enable the channel again. No more AHB transfers are done again from the same unit (receiver or transmitter) which was active during the AHB error until the error state is cleared and the unit is enabled again.

Link error

When a link error occurs during the transmission, the remaining part of the packet is discarded up to, and including, the next EOP/EEP. When this is done, status is immediately written back to the descriptor (with the LE bit set) and the descriptor pointer is incremented. The link will be disconnected when the link error occurs but the core will automatically try to connect again, provided that the link-start bit (LS bit in Control register) is asserted, and the link-disabled bit (LD bit in Control register) is deasserted. If the LE bit in the DMA channel's control register is not set the transmitter DMA engine will wait for the link to enter run-state, and start a new transmission immediately when possible, assuming there are packets pending. If the LE bit in the DMA channel's control register is set, the transmitter will be disabled when a link error occurs during a transmission of a packet. In that case, no more packets will be transmitted until the transmitter is enabled again. See description of the DMA channel's control register for more details.

57.8 RMAP

The Remote Memory Access Protocol (RMAP) is used to implement access to resources in the node via the SpaceWire link. Some common operations are reading and writing to memory, registers and FIFOs. The core has an optional hardware RMAP target. Whether or not the RMAP target is implemented is indicated by the CTRL.RA bit. This section describes the basics of the RMAP protocol and the target implementation.

57.8.1 Fundamentals of the protocol

RMAP is a protocol which is designed to provide remote access via a SpaceWire network to memory mapped resources on a SpaceWire node. It has been assigned protocol ID 0x01. It provides three operations: write, read and read-modify-write. These operations are posted operations, which means that a

source does not wait for an acknowledge or reply. It also implies that any number of operations can be outstanding at any time and that no timeout mechanism is implemented in the protocol. Time-outs must instead be implemented in the user application which sends the commands. Data payloads of up to 2^{24} - 1 bytes is supported by the protocol. A destination can be requested to send replies and to verify data before executing an operation. For a complete description of the protocol, see the RMAP standard (ECSS-E-ST-50-52C).

57.8.2 Implementation

The core includes a target for RMAP commands which processes all incoming packets with protocol ID = 0x01, type field (bit 7 and 6 of the 3rd byte in the packet) equal to 01b and an address falling in the range set by the default address and mask register. When such a packet is detected it is not stored to the DMA channel, instead it is passed to the RMAP receiver.

The core implements all three commands defined in the standard with some restrictions. Support is only provided for 32-bit big-endian systems. This means that the first byte received is the msb in a word. The target will not receive RMAP packets using the extended protocol ID which are always dumped to the DMA channel.

The RMAP receiver processes commands. If they are correct and accepted the operation is performed on the AHB bus and a reply is formatted. If an acknowledge is requested the RMAP transmitter automatically send the reply. RMAP transmissions have priority over DMA channel transmissions.

There is a user accessible destination key register which is compared to destination key field in incoming packets. If there is a mismatch and a reply has been requested the error code in the reply is set to 3. Replies are sent if and only if the ack field is set to ‘1’.

When a failure occurs during a bus access the error code is set to 1 (General Error). There is predetermined order in which error-codes are set in the case of multiple errors in the core. It is shown in table 888.

*Table 888.*The order of error detection in case of multiple errors. The error detected first has number 1.

Detection Order	Error Code	Error
1	12	Invalid destination logical address
2	2	Unused RMAP packet type or command code
3	3	Invalid destination key
4	9	Verify buffer overrun
5	11	RMW data length error
6	10	Authorization failure
7*	1	General Error (AHB errors during non-verified writes)
8	5/7	Early EOP / EEP (if early)
9	4	Invalid Data CRC
10	1	General Error (AHB errors during verified writes or RMW)
11	7	EEP
12	6	Cargo Too Large
*The AHB error is not guaranteed to be detected before Early EOP/EEP or Invalid Data CRC. For very long accesses the AHB error detection might be delayed causing the other two errors to appear first.		

Read accesses are performed on the fly, that is they are not stored in a temporary buffer before transmitting. This means that the error code 1 will never be seen in a read reply since the header has already been sent when the data is read. If the AHB error occurs the packet will be truncated and ended with an EEP.

Errors up to and including Invalid Data CRC (number 8) are checked before verified commands. The other errors do not prevent verified operations from being performed.

The details of the support for the different commands are now presented. All defined commands which are received but have an option set which is not supported in this specific implementation will not be executed and a possible reply is sent with error code 10.

57.8.3 Write commands

The write commands are divided into two subcategories when examining their capabilities: verified writes and non-verified writes. Verified writes have a length restriction of 4 bytes and the address must be aligned to the size. That is 1 byte writes can be done to any address, 2 bytes must be halfword aligned, 3 bytes are not allowed and 4 bytes writes must be word aligned. Since there will always be only one AHB operation performed for each RMAP verified write command the incrementing address bit can be set to any value.

Non-verified writes have no restrictions when the incrementing bit is set to 1. If it is set to 0 the number of bytes must be a multiple of 4 and the address word aligned. There is no guarantee how many words will be written when early EOP/EEP is detected for non-verified writes.

57.8.4 Read commands

Read commands are performed on the fly when the reply is sent. Thus if an AHB error occurs the packet will be truncated and ended with an EEP. There are no restrictions for incrementing reads but non-incrementing reads have the same alignment restrictions as non-verified writes. Note that the “Authorization failure” error code will be sent in the reply if a violation was detected even if the length field was zero. Also note that no data is sent in the reply if an error was detected i.e. if the status field is non-zero.

57.8.5 RMW commands

All read-modify-write sizes are supported except 6 which would have caused 3 B being read and written on the bus. The RMW bus accesses have the same restrictions as the verified writes. As in the verified write case, the incrementing bit can be set to any value since only one AHB bus operation will be performed for each RMW command. Cargo too large is detected after the bus accesses so this error will not prevent the operation from being performed. No data is sent in a reply if an error is detected i.e. the status field is non-zero.

57.8.6 Control

The RMAP target mostly runs in the background without any external intervention, but there are a few control possibilities.

There is an enable bit in the control register of the core which can be used to completely disable the RMAP target. When it is set to ‘0’ no RMAP packets will be handled in hardware, instead they are all stored to the DMA channel.

There is a possibility that RMAP commands will not be performed in the order they arrive. This can happen if a read arrives before one or more writes. Since the target stores replies in a buffer with more than one entry several commands can be processed even if no replies are sent. Data for read replies is read when the reply is sent and thus writes coming after the read might have been performed already if there was congestion in the transmitter. To avoid this the RMAP buffer disable bit can be set to force the target to only use one buffer which prevents this situation.

The last control option for the target is the possibility to set the destination key which is found in a separate register.

*Table 889.*GRSPW2 hardware RMAP handling of different packet type and command fields.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Command	Action
Reserved	Command / Response	Write / Read	Verify data before write	Acknow-ledge	Increment Address		
0	0	-	-	-	-	Response	Stored to DMA-channel.
0	1	0	0	0	0	Not used	Does nothing. No reply is sent.
0	1	0	0	0	1	Not used	Does nothing. No reply is sent.
0	1	0	0	1	0	Read single address	Executed normally. Address has to be word aligned and data size a multiple of four. Reply is sent. If alignment restrictions are violated error code is set to 10.
0	1	0	0	1	1	Read incre-menting address.	Executed normally. No restric-tions. Reply is sent.
0	1	0	1	0	0	Not used	Does nothing. No reply is sent.
0	1	0	1	0	1	Not used	Does nothing. No reply is sent.
0	1	0	1	1	0	Not used	Does nothing. Reply is sent with error code 2.
0	1	0	1	1	1	Read-Mod-ify-Write incrament-ing address	Executed normally. If length is not one of the allowed rmw val-ues nothing is done and error code is set to 11. If the length was correct, alignment restric-tions are checked next. 1 byte can be rmw to any address. 2 bytes must be halfword aligned. 3 bytes are not allowed. 4 bytes must be word aligned. If these restrictions are violated nothing is done and error code is set to 10. If an AHB error occurs error code is set to 1. Reply is sent.
0	1	1	0	0	0	Write, sin-gle-address, do not verify before writ-ing, no acknowledge	Executed normally. Address has to be word aligned and data size a multiple of four. If alignment is violated nothing is done. No reply is sent.
0	1	1	0	0	1	Write, incre-menting address, do not verify before writ-ing, no acknowledge	Executed normally. No restric-tions. No reply is sent.
0	1	1	0	1	0	Write, sin-gle-address, do not verify before writ-ing, send acknowledge	Executed normally. Address has to be word aligned and data size a multiple of four. If alignment is violated nothing is done and error code is set to 10. If an AHB error occurs error code is set to 1. Reply is sent.

*Table 889.*GRSPW2 hardware RMAP handling of different packet type and command fields.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Command	Action
Reserved	Command / Response	Write / Read	Verify data before write	Acknow-ledge	Increment Address		
0	1	1	0	1	1	Write, incre-menting address, do not verify before writ-ing, send acknowledge	Executed normally. No restric-tions. If AHB error occurs error code is set to 1. Reply is sent.
0	1	1	1	0	0	Write, single address, ver-ify before writing, no acknowledge	Executed normally. Length must be 4 or less. Otherwise nothing is done. Same alignment restric-tions apply as for rmw. No reply is sent.
0	1	1	1	0	1	Write, incre-menting address, ver-ify before writing, no acknowledge	Executed normally. Length must be 4 or less. Otherwise nothing is done. Same alignment restric-tions apply as for rmw. If they are violated nothing is done. No reply is sent.
0	1	1	1	1	0	Write, single address, ver-ify before writing, send acknowledge	Executed normally. Length must be 4 or less. Otherwise nothing is done and error code is set to 9. Same alignment restrictions apply as for rmw. If they are vio-lated nothing is done and error code is set to 10. If an AHB error occurs error code is set to 1. Reply is sent.
0	1	1	1	1	1	Write, incre-menting address, ver-ify before writing, send acknowledge	Executed normally. Length must be 4 or less. Otherwise nothing is done and error code is set to 9. Same alignment restrictions apply as for rmw. If they are vio-lated nothing is done and error code is set to 10. If an AHB error occurs error code is set to 1. Reply is sent.
1	0	-	-	-	-	Unused	Stored to DMA-channel.
1	1	-	-	-	-	Unused	Stored to DMA-channel.

57.9 AMBA interface

The AMBA interface consists of an APB interface, an AHB master interface and DMA FIFOs. The APB interface provides access to the user registers which are described in section 57.12. The DMA engines have 32-bit wide FIFOs to the AHB master interface which are used when reading and writing to the bus.

The transmitter DMA engine reads data from the bus in bursts which are half the FIFO size in length. A burst is always started when the FIFO is half-empty or if it can hold the last data for the packet. The burst containing the last data might have shorter length if the packet is not an even number of bursts in size.

The receiver DMA works in the same way except that it checks if the FIFO is half-full and then performs a burst write to the bus which is half the fifo size in length. The last burst might be shorter. If the *rmap* or *rxunaligned* VHDL generics are set to 1 the interface also handles byte accesses. Byte accesses are used for non word-aligned buffers and/or packet lengths that are not a multiple of four bytes. There might be 1 to 3 single byte writes when writing the beginning and end of the received packets.

57.9.1 APB slave interface

As mentioned above, the APB interface provides access to the user registers which are 32-bits in width. The accesses to this interface are required to be aligned word accesses. The result is undefined if this restriction is violated.

57.9.2 AHB master interface

The core contains a single master interface which is used by both the transmitter and receiver DMA engines. The arbitration algorithm between the channels is done so that if the current owner requests the interface again it will always acquire it. This will not lead to starvation problems since the DMA engines always deassert their requests between accesses.

The AHB accesses are always word accesses (HSIZE = 0x010) of type incremental burst with unspecified length (HBURST = 0x001) if the RMAP target is not implemented (RA bit in Control register = 0) and unaligned transfers are not supported (RX bit in the Control register = 0). If either the RMAP target is implemented, or unaligned transfers are supported, then AHB accesses can be of size byte, halfword and word (HSIZE = 0x000, 0x001, 0x010) otherwise. Byte and halfword accesses are always NONSEQ. Note that read accesses are always word accesses (HSIZE = 0x010), which can result in destructive read.

The burst length will be half the AHB FIFO size except for the last transfer for a packet which might be smaller. Shorter accesses are also done during descriptor reads and status writes.

The AHB master also supports non-incrementing accesses where the address will be constant for several consecutive accesses. HTRANS will always be NONSEQ in this case while for incrementing accesses it is set to SEQ after the first access. This feature is included to support non-incrementing reads and writes for RMAP.

If the core does not need the bus after a burst has finished there will be one wasted cycle (HTRANS = IDLE).

BUSY transfer types are never requested and the core provides full support for ERROR, RETRY and SPLIT responses.

57.10 SpaceWire Plug-and-Play

The core supports parts of the SpaceWire Plug-and-Play protocol. The supported fields are listed in table 892, and explained in more detail in tables 893 through 907. Table 892 also shows which type of SpaceWire Plug-and-Play access type (read, write, compare-and-swap) that is allowed for the field. Note that two different amount of SpaceWire Plug-and-Play support may be included. Either only device identification through the Device Information fields is supported, or device configuration through the SpaceWire Protocol fields is supported as well. The amount of support is indicated by the CTRL.PNPA field. Note also that the CTRL.PE must be set in order to enable the SpaceWire Plug-and-Play support.

The SpaceWire Plug-and-Play protocol uses standard RMAP commands and replies with the same requirements as presented in section 57.8, but with the following differences:

- Protocol Identifier field of a command shall be set to 0x03.
- A command's address fields shall contain a word address. The SpaceWire Plug-and-Play addresses are encoded as shown in table 890.

- The increment bit in the command's instruction field shall be set to 1, otherwise a reply with Status field set to 0x0A (authorization failure) is sent.
- RMAP read-modify-write command is replaced by a compare-and-swap command. The command's data fields shall contain the new data to be written, while the mask fields shall contain the value that the current data must match in order for the new data to be written. If there is a mismatch, a reply with Status field set to 0x0A (authorization failure) is sent.
- The reply packet's Status field can contain the additional status codes described in table 891.

Table 890. SpaceWire Plug-and-Play address encoding

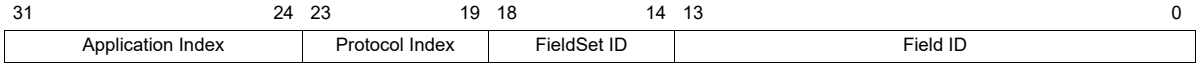


Table 891. SpaceWire Plug-and-Play status codes

Value	Description
0xF0	Unauthorized access - A write, or compare-and-swap command, with an address other then the Device ID field's address, arrived when the core was not configured (Device ID field = 0), or the command did not match the owner information saved in the Link Information field and Owner Address fields.
0xF1	Reserved field set - A read, write, or compare-and-swap command's address field points to a non existing field set. 1)
0xF2	Read-only field - A write, or compare-and-swap command's address points to a read-only field.
0xF3	Compare-and-swap-only-field - A write command's address points to a field that is only writable through a compare-and-swap-only.
Note 1: An access to a non existing field, within a existing field set, does not generate an error response. The data returned in a read access is zero, while a write access has no effect.	

Table 892. SpaceWire Plug-and-Play support

SpW PnP Address	Name	Acronym	Service - Field set - Field	Access type
0x00000000	SpaceWire Plug-and-Play - Device Vendor and Product ID	PNPVEND	Device Information - Device Identification - Device Vendor and Product ID	read
0x00000001	SpaceWire Plug-and-Play - Version	PNPVER	Device Information - Device Identification - Version	read
0x00000002	SpaceWire Plug-and-Play - Device Status	PNPDEVSTS	Device Information - Device Identification - Device Status	read
0x00000003	SpaceWire Plug-and-Play - Active Links	PNPALINK	Device Information - Device Identification - Active Links	read
0x00000004	SpaceWire Plug-and-Play - Link Information	PNPLINFO	Device Information - Device Identification - Link Information	read
0x00000005	SpaceWire Plug-and-Play - Owner Address 0	PNPOA0	Device Information - Device Identification - Owner Address 0	read
0x00000006	SpaceWire Plug-and-Play - Owner Address 1	PNPOA1	Device Information - Device Identification - Owner Address 1	read
0x00000007	SpaceWire Plug-and-Play - Owner Address 2	PNPOA2	Device Information - Device Identification - Owner Address 2	read
0x00000008	SpaceWire Plug-and-Play - Device ID	PNPDEVID	Device Information - Device Identification - Device ID	read, cas

Table 892. SpaceWire Plug-and-Play support

SpW PnP Address	Name	Acronym	Service - Field set - Field	Access type
0x00000009	SpaceWire Plug-and-Play - Unit Vendor and Product ID	PNPUVEND	Device Information - Device Identification - Unit Vendor and Product ID	read
0x0000000A	SpaceWire Plug-and-Play - Unit Serial Number	PNPUSN	Device Information - Device Identification - Unit Serial Number	read
0x00004000	SpaceWire Plug-and-Play - Vendor String Length	PNPVSTRL	Device Information - Vendor / Product String - Vendor String Length	read
0x00006000	SpaceWire Plug-and-Play - Product String Length	PNPPSTRL	Device Information - Vendor / Product String - Product String Length	read
0x00008000	SpaceWire Plug-and-Play - Protocol Count	PNPPCNT	Device Information - Protocol Support - Protocol Count	read
0x00008001	SpaceWire Plug-and-Play - Protocol Identification 1	PNPPID1	Device Information - Protocol Support - Protocol Identification 1	read
0x00008002	SpaceWire Plug-and-Play - Protocol Identification 2	PNPPID2	Device Information - Protocol Support - Protocol Identification 2	read
0x0000C000	SpaceWire Plug-and-Play - Application Count	PNPACNT	Device Information - Application Support- Application Count	read
0x00080000	SpaceWire Plug-and-Play - Time-Code Counter [1)]	PNPTCC	SpaceWire Protocol - Device Configuration - Time-Code Counter	read, write, cas
0x00084008	SpaceWire Plug-and-Play - Link Status [1)]	PNPLSTS	SpaceWire Protocol - Link Configuration - Link Status	read, write, cas
0x00084009	SpaceWire Plug-and-Play - Link Control [1)]	PNPLCTRL	SpaceWire Protocol - Link Configuration - Link Control	read, write, cas
0x00100000	SpaceWire Plug-and-Play - Maximum Write Length [1)]	PNPMWLEN	SpaceWire PnP Protocol - Protocol Information - Maximum Write Length	read
0x00100001	SpaceWire Plug-and-Play - Maximum Read Length [1)]	PNPMRLEN	SpaceWire PnP Protocol - Protocol Information - Maximum Read Length	read
Note 1: Register is only available when device configuration through SpaceWire Plug-and-Play is supported, which is indicated by the value of the CTRL.PNPA field.				

The layout of the SpaceWire Plug-and-Play registers used in this section is the same as for the registers described in section 57.12, and is exemplified in table 917. The reset value field

and bit-field type definitions are also the same as in section 57.12, and are explained in tables 918 and 919 respectively.

*Table 893.*0x00000000 - PNPVEND - SpaceWire Plug-and-Play - Device Vendor and Product ID

31 16	15 0
VEND	PROD
*	*
r	r

31: 16 Vendor ID (VEND) - SpaceWire vendor ID assigned at implementation time. Value taken from the VHDL generic *pnpvendid*.

15: 0 Product ID (PROD) - Product ID assigned at implementation time. Value taken from the VHDL generic *pnpprodid*.

*Table 894.*0x00000001 - PNPVER - SpaceWire Plug-and-Play - Version

31 24	23 16	15 8	7 0
MAJOR	MINOR	PATCH	RESERVED
*	*	*	*
r	r	r	r

31: 24 Major version number (MAJOR) - Major version number set at implementation time. Value taken from the VHDL generic *pnpmajorid*.

23: 16 Minor version number (MINOR) - Minor version number set at implementation time. Value taken from the VHDL generic *pnpminorid*.

15: 8 Patch / Build number (PATCH) - Patch / Build number set at implementation time. Value taken from the VHDL generic *pnppatchid*.

7: 0 RESERVED

*Table 895.*0x00000002 - PNPDEVSTS - SpaceWire Plug-and-Play - Device Status

31 8	7 0
RESERVED	STATUS
0x000000	0x00
r	r

31: 8 RESERVED

7: 0 Device status (STATUS) - Constant value of 0x00.

*Table 896.*0x00000003 - PNPALINK - SpaceWire Plug-and-Play - Active Links

31 2	1	0
RESERVED	AC	R
0x00000000	0	0
r	r	r

31: 20 RESERVED

19: 1 Link active (AC) - Indicates if the link interface is in run-state. 0 = Not run-state, 1 = run-state.

0 RESERVED

*Table 897.*0x00000004 - PNPLINFO -SpaceWire Plug-and-Play - Link Information

31 24	23 22	21	20 16	15 13	12 8	7	6	5	4 0
OLA	OAL	R	OL	RES	RL	T	U	R	LC
0x00	0x0	0	0x0	0x0	0x0	1	0	0	0x13
r	r	r	r	r	r	r	r	r	r

31: 24 Owner logical address (OLA) - Shows the value of the Initiator Logical Address field from the last successful compare-and-swap command that set the Device ID field.

23: 22 Owner address length (OAL) - Shows how many of the three Owner Address fields that contain valid data.

21 RESERVED

20: 16 Owner link (OL) - Shows the number of the port which was used for the last successful operation to set the value of the Device ID field.

15: 13 RESERVED

12: 8 Return link (RL) - Shows the number of the port through which the reply to the current read command will be transmitted.

7 Device type (T) - Constant value of 0, indicating a node.

6 Unit information (U) - Indicates if the unit identification information (Unit Vendor and Product ID field, and Unit Serial Number field) are valid. 0 = invalid, 1 = valid. This bit will be 0 after reset / power-up. Once the Unit Vendor and Product ID field has been written with a non-zero value, this bit will be set to 1.

5 RESERVED

4: 0 Link count (LC) - Shows the number of router ports. Constant value of 0x13.

*Table 898.*0x00000005 - PNPOA0 - SpaceWire Plug-and-Play - Owner Address 0

31 0
RA
0x00000000
r

31: 0 Reply address (RA) - Shows byte 0-3 of the Reply Address from the last successful compare-and-swap command that set to the Device ID field. If there was no Reply Address, then this field is zero.

*Table 899.*0x00000006 - PNPOA1 - SpaceWire Plug-and-Play - Owner Address 1

31 0
RA
0x00000000
r

31: 0 Reply address (RA) - Shows byte 4-7 of the Reply Address from the last successful compare-and-swap command that set to the Device ID field. If the Reply Address was four bytes or less, then this field is zero.

*Table 900.*0x00000007 - PNPOA2 - SpaceWire Plug-and-Play - Owner Address 2

31 0
RA
0x00000000
r

31: 0 Reply address (RA) - Shows byte 8-11 of the Reply Address from the last successful compare-and-swap command that set to the Device ID field. If the Reply Address was eight bytes or less, then this field is zero.

*Table 901.*0x00000008 - PNPDEVID - SpaceWire Plug-and-Play - Device ID

31	0
DID	
0x00000000	
cas	

31: 0 Device ID (DID) - Shows the device identifier. This field is set to zero after reset / power-up, and when the link-interface is not in run-state.

*Table 902.*0x00000009 - PNPUVEND - SpaceWire Plug-and-Play - Unit Vendor and Product ID

31	16	15	0
VEND		PROD	
*		*	
r		r	

31: 16 Unit vendor ID (VEND) - Shows the unit vendor identifier. This field is read-only through the SpaceWire Plug-and-Play protocol, however it is writable through an APB register (see section 57.12). Reset value is taken from the input signal PNPUVENDID. Whenever this field, or the PROD field, is set to a non-zero value, the PNPLINFO.U bit is set to 1.

15: 0 Unit product ID (PROD) - Shows the unit product identifier. This field is read-only through the SpaceWire Plug-and-Play protocol, however it is writable through an APB register (see section 57.12). Reset value is taken from the input signal PNPUPRODID. Whenever this field, or the VEND field, is set to a non-zero value, the PNPLINFO.U bit is set to 1.

*Table 903.*0x0000000A - PNPUSN - SpaceWire Plug-and-Play - Unit Serial Number

31	0
USN	
*	
r	

31: 0 Unit serial number (USN) - Shows the unit serial number. This field is read-only through the SpaceWire Plug-and-Play protocol, however it is writable through the APB register (see section 57.12). Reset value is taken from the input signal PNPUSN.

*Table 904.*0x00004000 - PNPVSTRL - SpaceWire Plug-and-Play - Vendor String Length

31	15	14	0
RESERVED		LEN	
0x00000		0x0000	
r		r	

31: 15 RESERVED

14: 0 Vendor string length (LEN) - Constant value of 0, indicating that no vendor string is present.

*Table 905.*0x00006000 - PNPPSTRL - SpaceWire Plug-and-Play - Product String Length

31	15	14	0
RESERVED		LEN	
0x00000		0x0000	
r		r	

31: 15 RESERVED

14: 0 Product string length (LEN) - Constant value of 0, indicating that no product string is present.

*Table 906.*0x00008000 - PNPPCNT - SpaceWire Plug-and-Play - Protocol Count

31 5	4 0
RESERVED	PC
0x0000000	*
r	r

31: 5 RESERVED

4: 0 Protocol count (PC) - Constant value of 0 when only device identification is supported (CTRL.PNPA = 1). Constant value of 2 when device configuration is supported (CTRL.PNPA = 2).

*Table 907.*0x0000C000 - PNPACNT - SpaceWire Plug-and-Play - Application Count

31 8	7 0
RESERVED	AC
0x000000	0x00
r	r

31: 8 RESERVED

7: 0 Application count (AC) - Constant value of 0, indicating that no applications can be managed by using SpaceWire Plug-and-Play.

*Table 908.*0x00080000 - PNPTCC - SpaceWire Plug-and-Play - Time-Code Counter

31 6	5 0
RESERVED	TC
0x0000000	0x00
r	rw*

31: 6 RESERVED

5: 0 Time Count (TC) - Current time value. This bitfield can be reset by writing zero to it. Writing any other value has no effect. Double map of TC.TIMECNT value (see TC register in section 57.12 for a functional description).

*Table 909.*0x00084008 - PNPLSTS - SpaceWire Plug-and-Play - Link Status

31	30	29 19	18 16	15 8	7	6	5	4	3	2	1	0
ND	LT	RESERVED	LS	RESERVED	R	CE	ER	PE	DE	R	IA	R
1	1	0x000	0x0	0x00	0	0	0	0	0	0	0	0
r	r	r	r	r	r	rw*	rw*	rw*	rw*	r	rw*	r

31 Network discovery (ND) - Constant value of 1, indicating that the link can be used for network discovery.

30 Link type (LT) - Constant value of 1, indicating that the link is a SpaceWire link.

29: 19 RESERVED

18: 16 Link State (LS) - The current state of the link interface. 0 = Error-reset, 1 = Error-wait, 2 = Ready, 3 = Started, 4 = Connecting, 5 = Run.

25: 8 RESERVED

7 RESERVED

6 Credit Error (CE) - A credit has occurred. Cleared when complete PNPLSTS is written with zero.

5 Escape Error (ER) - An escape error has occurred. Cleared when complete PNPLSTS is written with zero.

4 Parity Error (PE) - A parity error has occurred. Cleared when complete PNPLSTS is written with zero.

3 Disconnect Error (DE) - A disconnection error has occurred. Cleared when complete PNPLSTS is written with zero.

2 RESERVED

1 Invalid Address (IA) - Set to one when a packet is received with an invalid destination address field, i.e it does not match the DEFADDR register. Cleared when complete PNPLSTS is written with zero.

0 RESERVED

*Table 910.*0x00084009 - PNPLCTRL - SpaceWire Plug-and-Play - Link Control

31 5	4	3	2	1	0
RESERVED	TT	R	LD	LS	AS
	0	0	0	0	*
	rw	r	rw	rw	rw

31: 5 RESERVED

4 Time-Code transmission (TT) - Enable Time-Code transmission.

3 RESERVED

2 Link Disable (LD) - Disable the SpaceWire codec link-interface.

1 Link Start (LS) - Start the link, i.e. allow a transition from ready-state to started-state.

0 Autostart (AS) - Automatically start the link when a NULL has been received. Reset value is set from input signal RMAPEN if RMAP target is available (CTRL.RA bit = 1), otherwise the reset value is '0'.

*Table 911.*0x00100000 - PNPMWLEN - SpaceWire Plug-and-Play - Maximum Write Length

31 15	14 0
RESERVED	LEN
0x00000	0x0002
r	r

31: 15 RESERVED

14: 0 Length (LEN) - Constant value, indicating the maximum number of fields that can be written with a single write command.

*Table 912.*0x00100001 - PNPMRLEN - SpaceWire Plug-and-Play - Maximum Read Length

31 15	14 0
RESERVED	LEN
0x00000	0x4000
r	r

31: 15 RESERVED

14: 0 Length (LEN) - Constant value, indicating the maximum number of fields that can be read with a single read command.

57.11 Implementation

57.11.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

There are five input resets, in order to cover every clock domain: AMBA reset (rst), transmitter synchronous reset (txsyncrst), receiver synchronous reset for port 0 (rxsyncrst0), receiver synchronous reset for port 1 (rxsyncrst1) and a receiver asynchronous reset shared by both ports (rxasyncrst).

Additionally, the core outputs two internal resets: the register reset, swno.ctrlregrst (bit 6 of the Control Register. See 57.12.1. Control Register), and the internal reset for synchronization between transmitter and receivers, swno.rxrst.

The core does not implement any kind of internal reset generation or synchronization, the input resets are completely independent. The reset generation shall be done in a higher instance, taking into account the clock domains and also the output resets of the core. A description of how the resets shall be combined and generated can be found below. Cobham Gaisler advise to follow these guidelines unless indicated otherwise.

- The AMBA reset is the combination of the external reset and the output register reset negated (swno.ctrlregrst), as it is active high. Then, the reset is synchronized with the AMBA clock by using a reset generator. Its output is the AMBA reset, rst.
- The transmitter reset is the combination of the external reset and the output register reset negated (swno.ctrlregrst), as it is active high. Then, the reset is synchronized with the transmitter clock by using a reset generator. Its output is the transmitter reset, txsyncrst.
- The asynchronous reset for both receiver channels is simply the output synchronization reset, swno.rxrst, connected directly to the input rxasyncrst.
- The synchronous reset for each receiver channel is the output receiver reset, swno.rxrst, synchronized with the appropriate clock domain by using a reset generator. Its output is the synchronous reset for the specific receiver port, rxsyncrst0 or rxsyncrst1.

In order to avoid the process of generating all these resets, GRLIB includes a wrapper called grspwm which instantiates either GRSPW or GRSPW2. If the latter is chosen, there is a generic to directly implement the previous reset generators in the wrapper itself, so the top entity does not need to generate the resets anymore. Further information about the proper way of combining the reset signals or using the wrapper can be found in 57.19. Instantiation, including an example for both possibilities.

57.11.2 Clock-generation

The receiver module found in figure 152 should be clocked with a clock outputed by the GRSPW2_PHY module. See the example instantiation in this section and the GRSPW2_PHY section of the GRLIB IP Core User's Manual for more information on how to connect this clock.

The transmitter clock is generated from the TXCLK input. A separate clock input is used to allow the transmitter to be run at much higher frequencies than the system clock. The SpaceWire node contains a clock-divider which divides the TXCLK signal to the wanted frequency. The transmitter clock should be 10 MHz during initialization and any frequency above 2 MHz in the run-state.

There is an input signal called CLKDIV10 which sets the reset values for the user accessible clock divisor registers. There is one register value which is used during initialisation and one which is used in run-state. See 57.3.6 for details on how to set the clock divisor values.

Since only integer values are allowed for the clock division and the required init-frequency is 10 Mhz the frequency of the txclk input must be a multiple of 10 MHz. The clock divisor value is 8-bits wide so the maximum txclk frequency supported is 2.56 GHz (note that there is also a restriction on the relation between the system and transmit clock frequencies).

57.11.3 Timers

There are two timers in the core: one for generating the 6.4/12.8 us periods and one for disconnect timing.

The timeout periods are generated from the tx clock whose frequency must be at least 10 MHz to guarantee disconnect timing limits. The same clock divisor is used as for the tx clock during initialisation so it must be set correctly for the link timing to work.

57.11.4 Synchronization

The transmitter and receiver bit rates can be eight times higher than the system clock frequency. This includes a large margin for clock skew and jitter so it might be possible to run at even higher rate differences. Note also that the receiver clocks data at both negative and positive edges for the input modes 0 and 1 so the bitrate is twice the clock frequency. There is no direct relationship between bitrate and frequency for the sampling modes.

The clock synchronization is just one limiting factor for the clock frequency, it might for example not be possible to achieve the highest possible frequency for certain technologies.

The asynchronous reset to the receiver clock domain has to have a maximum delay of one receiver clock cycle to ensure correct operation. This is needed because the receiver uses a completely asynchronous reset. To make sure that nothing bad happens the is a synchronous reset guard which prevents any signals from being assigned before all registers have their reset signals released.

In the sampling modes this asynchronous reset can be removed if both the receiver and transmitter runs on the same clock. The core is configured to use the same receiver and transmitter clock by setting the *rxtx_sameclk* generic to 1.

57.11.5 Fault-tolerance

The core can optionally be implemented with fault-tolerance against SEU errors in the FIFO memories. The fault-tolerance is enabled through the *ft* VHDL generic. Possible options are byte parity protection (*ft = 1*) or TMR registers (*ft = 2*).

57.11.6 Synthesis

The fact there are three clock domains in the core of which all are possibly high frequency clocks makes it necessary to declare all paths between the clock domains as false paths. In Synplify this is most easily done by declaring all the clocks to be in different clockgroups in the sdc file (if Synplify does not automatically put them in different groups). This will disable any timing considerations between the clock domains and these constraints will also propagate to the place and route tool.

57.11.7 Technology mapping

The core has three generics for technology mapping: *tech*, *techfifo* and *memtech*. *Tech* selects the technology used for the clock buffers and also adds reset to some registers for technologies where they would otherwise cause problems with gate-level simulations. *Techfifo* selects whether *memtech* should be used to select the technology for the FIFO memories (the RMAP buffer is not affected by the this generic) or if they should be inferred. *Tech* and *memtech* can be set to any value from 0 to NTECH as defined in the GRLIB.TECH package.

57.11.8 RAM usage

The core maps all RAM memories on the syncram_2p component if the *ft* generic is 0 and to the syncram_2pft component for other values. The syncrams are located in the technology mapping library (TECHMAP). The organization of the different memories are described below. If techfifo and/or memtech is set to 0 the synthesis tool will infer the memories. Either RAM blocks or flip-flops will be used depending on the tool and technology. The number of flip-flops used is *syncram depth x syncram width* for all the different memories. The receiver AHB FIFO with fifosize 32 will for example use 1024 flips-flops.

Receiver ahb FIFO

The receiver AHB fifo consists of one syncram_2p block with a width of 32-bits. The depth is determined by the configured FIFO depth. Table 913 shows the syncram organization for the allowed configurations.

*Table 913.*syncram_2p sizes for GRSPW2 receiver AHB FIFO.

Fifosize	Syncram_2p organization
4	4x32
8	8x32
16	16x32
32	32x32
64	64x32

Transmitter ahb FIFO

The transmitter AHB fifo consists of one syncram_2p block with a width of 32-bits. The depth is determined by the configured FIFO depth. Table 914 shows the syncram organization for the allowed configurations.

*Table 914.*syncram_2p sizes for transmitter AHB FIFO.

Fifosize	Syncram_2p organization
4	4x32
8	8x32
16	16x32
32	32x32
64	64x32

Receiver N-Char FIFO

The receiver N-Char fifo consists of one syncram_2p block with a width of 10-bits. The depth is determined by the configured FIFO depth. Table 915 shows the syncram organization for the allowed configurations.

*Table 915.*syncram_2p sizes for the receiver N-Char FIFO.

Fifosize	Syncram_2p organization
16	16x10
32	32x10
64	64x10

RMAP buffer

The RMAP buffer consists of one syncram_2p block with a width of 8-bits. The depth is determined by the number of configured RMAP buffers. Table 916 shows the syncram organization for the allowed configurations.

*Table 916.*syncram_2p sizes for RMAP buffer memory.

RMAP buffers	Syncram_2p organization
2	64x8
4	128x8
8	256x8

57.12 Registers

The core is programmed through registers mapped into APB address space. The registers are listed in table, 920 and described in detail in the subsequent tables. Addresses not listed in table 920 are reserved. A read access to a reserved register, or reserved field with a register, will always return zero,

and a write access has no effect. The register layout used is exemplified in table 917, and the values used in the reset value row and field type row are explained in tables 918 and 919.

Table 917.<APB ddress offset> - <Register acronym> - <Register name>

31 24	23 16	15 8	7 0
EF3	EF2	EF1	EF0
<Reset value for EF3>	<Reset value for EF2>	<Reset value for EF1>	<Reset value for EF0>
<Bit-field type for EF3>	<Bit-field type for EF2>	<Bit-field type for EF1>	<Bit-field type for EF0>

31: 24 Example bit-field 3 (EF3) - <Bit-field description>

23: 16 Example bit-field 2 (EF2) - <Bit-field description>

15: 8 Example bit-field 1 (EF1) - <Bit-field description>

7: 0 Example bit-field 0 (EF0) - <Bit-field description>

Table 918. Reset value definitions

Value	Description
0	Reset value 0. Used for single-bit fields.
1	Reset value 1. Used for single-bit fields.
0xNN	Hexadecimal representation of reset value. Used for multi-bit fields.
n/r	Field not reseted
*	Special reset condition, described in textual description of the bit-field. Used for example when reset value is taken from an input signal.

Table 919. Bit-field type definitions

Value	Description
r	Read-only. Writes have no effect.
rw	Readable and writable.
rw*	Readable and writeable. Special condition for write, described in textual description of the bit-field.
wc	Write-clear. Readable, and cleared when written with a 1. Writing 0 has no effect.

*Table 920.*GRSPW2 registers

APB address offset	Register acronym	Register name
0x00	CTRL	Control
0x04	STS	Status
0x08	DEFADDR	Default address
0x0C	CLKDIV	Clock divisor
0x10	DKEY	Destination key
0x14	TC	Time-code
0x18 - 0x1C	-	RESERVED
0x20, 0x40, 0x60, 0x80	DMACTRL	DMA control/status, channel 1 - 4 [1)]
0x24, 0x44, 0x64, 0x84	DMAMAXLEN	DMA RX maximum length, channel 1 - 4 [1)]
0x28, 0x48, 0x68, 0x88	DMATXDESC	DMA transmit descriptor table address, channel 1 - 4 [1)]
0x2C, 0x4C, 0x6C, 0x8C	DMARXDESC	DMA receive descriptor table address, channel 1 - 4 [1)]
0x30, 0x50, 0x70, 0x90	DMAADDR	DMA address, channel 1 - 4 [1)]
0x34, 0x54, 0x74, 0x94	-	RESERVED
0x38, 0x58, 0x78, 0x98	-	RESERVED
0x3C, 0x5C, 0x7C, 0x9C	-	RESERVED
0xA0	INTCTRL	Interrupt distribution control [2)]
0xA4	INTRX	Interrupt receive [2)]
0xA8	ACKRX / INTRXEXT	Interrupt-acknowledge receive / Interrupt receive extended [2)]
0xAC	INTTO	Interrupt timeout [2) 5)]
0xB0	INTTOEXT	Interrupt timeout extended [2) 5)]
0xB4	TICKMASK	Interrupt tick-out mask [2)]
0xB8	TICKMASKEXT / AUTO-ACK	Interrupt auto acknowledge mask / Interrupt tick-out mask extended [2)]
0xBC	INTCFG	Interrupt distribution configuration [2)]
0xC0	-	RESERVED
0xC4	ISR	Interrupt distribution ISR[2)]
0xC8	ISREXT	Interrupt distribution Extended ISR [2)]
0xCC	-	RESERVED
0xD0	PRESCALER	Interrupt distribution prescaler reload [3)]
0cD4	ISRTIMER	Interrupt distribution ISR timer reload [3)]
0xD8	IATIMER	Interrupt distribution INT / ACK timer reload [3)]
0xDC	ICTIMER	Interrupt distribution change timer reload [3)]
0xE0	PNPVEND	SpaceWire PnP Device Vendor and Product ID [4)]
0xE4	PNPLINKINFO	SpaceWire PnP Link Information [4)]
0xE8	PNPOA0	SpaceWire PnP Owner Address 0 [4)]
0xEC	PNPOA1	SpaceWire PnP Owner Address 1 [4)]
0xF0	PNPOA2	SpaceWire PnP Owner Address 2 [4)]
0xF4	PNPDEVID	SpaceWire PnP Device ID [4)]
0xF8	PNPUVEND	SpaceWire PnP Unit Vendor and Product ID [4)]
0xFC	PNPUSN	SpaceWire PnP Unit Serial Number [4)]

*Table 920.*GRSPW2 registers

APB address offset	Register acronym	Register name

Note 1: Registers for non implemented DMA channels are reserved. Number of implemented DMA channels is indicated by the NCH field in the Control register.

Note 2: Register is only available if the interrupt distribution is supported, which is indicated by the value of the CTRL.ID bit.

Note 3: Register is only available if support for the corresponding timer is implemented, otherwise the register is reserved. This can be detected by probing the RL field of corresponding register.

Note 4: Register is only available if the SpaceWire Plug-and-Play is supported, which is indicated by the value of the CTRL.PNPA field.

Note 5: Register is only available if support for the Interrupt distribution ISR timer is implemented. This ca be detected by probing the ISRTIMER.RL field.

57.12.1 Control Register

*Table 921.*0x00 - CTRL - Control

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RA	RX	RC	NCH		PO	CC	ID	R	LE	PS	NP	PNPA		RD	RE	PE	R	TL	TF	TR	TT	LI	TQ	R	RS	PM	TI	IE	AS	LS	LD
*	*	*	*		*	0	*	0	0	0	*	*		0	*	*	0	0	0	0	0	0	0	0	0	0	0	0	*	0	0
r	r	r	r		r	r	r	r	rw	rw	rw	r		rw	rw	rw	r	rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw

31 RMAP available (RA) - Set to one if the RMAP target is available. Value determined by the *rmap* VHDL generic.

30 RX unaligned access (RX) - Set to one if unaligned writes are available for the receiver. Value determined by the *rxunaligned* VHDL generic.

29 RMAP CRC available (RC) - Set to one if RMAP CRC is enabled in the core. Value determined by the *rmapcrc* VHDL generic.

28: 27 Number of DMA channels (NCH) - The number of available DMA channels minus one (Number of channels = NCH+1). Value determined by the *dmachan* VHDL generic.

26 Number of ports (PO) - The number of available SpaceWire ports minus one. Value determined by the *ports* VHDL generic.

25 CCSDS/CCITT CRC-16 and 16-bit ISO-checksum available (CC) - Set to one if this crc logic is enabled in the core. Value determined by the ccsdscrc VHDL generic.

24 Interrupt distribution available (ID) - Set to 1 if interrupt distribution support is available, otherwise set to 0. If set to 1, then the INTCTRL.NUMINT field indicates the number of supported interrupt numbers. Value determined by the *interruptdist* VHDL generic (ID = 1 if *interruptdist* /= 0).

23 RESERVED

22 Loop-back enable (LE). The value of this bit is driven on the LOOPBACK output signal.

21 Port select (PS) - Selects the active port when the CTRL.NP bit is zero. ‘0’ selects the port connected to data and strobe on index 0, while ‘1’ selects index data and strobe on 1. Only available in two-port configurations, which is indicated by CTRL.PO bit. This bit is reserved in one-port-configurations.

20 No port force (NP) - Disable port force. When this bit is set, the CTRL.PS bit cannot be used to select the active port. Instead, the active port is automatically selected by checking the activity on the respective receive links. Only available in two-port configurations, which is indicated by CTRL.PO bit. Reserved bit in one-port configurations. Reset value is set from input signal RMAPEN if RMAP target is available (indicated by CTRL.RA bit), otherwise the reset value is ‘0’.

19: 18 SpaceWire Plug-and-Play available (PNPA) - Indicates SpaceWire Plug-and-Play support. 0 = No support, 1 = Support for the device identification, 2 = Support for device identification and configuration. See section 57.10 for details. Value determined by the *pnp* VHDL generic.

17 RMAP buffer disable (RD) - If set, only one RMAP buffer is used. This ensures that all RMAP commands will be executed consecutively. Only available if the *rmap* VHDL generic is set to 1, otherwise the bit is reserved.

16 RMAP Enable (RE) - Enable RMAP target. Only available if *rmap* VHDL generic is set to 1, otherwise the bit is reserved. Reset value take from RMAPEN input signal.

15 SpaceWire Plug-and-Play enable (PE) - Enable SpaceWire Plug-and-Play support. Only available if the CTRL.PA bit is 1, otherwise this bit is reserved. Reset value taken from the PNPEN input signal.

14 RESERVED

13 Transmitter enable lock control (TL) - Enables / disables the transmitter enable lock functionality described by the DMACTRL.TL bit. 0 = Disabled, 1 = Enabled.

12 Time-code control flag filter (TF) - When set to 1, a received time-code must have its control flag bits set to “00” to be considered valid. When set to 0, all control flag bits are allowed. Note that if the interrupt code receive enable bit (INTCTRL.IR) is set to 1, then the only time-code control flag bits of “00” are allowed, regardless of the setting of this bit.

11 Time Rx Enable (TR) - Enable time-code reception.

10 Time Tx Enable (TT) - Enable time-code transmission.

9 Link error IRQ (LI) - Enables / disables AMBA interrupt generation when a link error occurs. Note that the CTRL.IE bit also must be set for this bit to have any effect.

8 Tick-out IRQ (TQ) - Enables / disables AMBA interrupt generation when a valid time-code is received. Note that the CTRL.IE bit also must be set for this bit to have any effect.

7 RESERVED

*Table 921.*0x00 - CTRL - Control

6	Reset (RS) - Make complete reset of the SpaceWire node. Self clearing.
5	Promiscuous Mode (PM) - Enable promiscuous mode. See section 57.6.10.
4	Tick In (TI) - The host can generate a tick by writing a one to this bit. This incrementd the timer counter (TC.TIMECNT), and the new value is transmitted. This bit will stay high until the time-code has been sent. Note that the link interface must be in run-state for the time-code to be sent.
3	Interrupt Enable (IE) - If set, AMBA interrupt generation is enabled for the events that are individually maskable by the CTRL.TQ, CTRL.LI, INTCTRL.IQ, INTCTRL.AQ, and INTCTRL.TQ bits.
2	Autostart (AS) - Automatically start the link when a NULL has been received. Reset value is set from input signal RMAPEN if RMAP target is available (CTRL.RA bit = 1), otherwise the reset value is ‘0’.
1	Link Start (LS) - Start the link, i.e. allow a transition from ready-state to started-state.
0	Link Disable (LD) - Disable the SpaceWire codec.

57.12.2 Status Register

*Table 922.*0x04 - STS - Status

31 28	27 26	25 24	23 22 21	20 19 18 17 16 15 14 13 12 11 10	9	8	7	6 5	4	3	2	1	0
RESERVED	NRXD	NTXD	LS	RESERVED	AP	EE	IA	RES	PE	DE	ER	CE	TO
0x00	*	*	0x0	0x000	0	0	0	0x0	0	0	0	0	0
r	r	r	r	r	r	wc	wc	r	wc	wc	wc	wc	wc

31: 28 RESERVED

27: 26 Number of receive descriptors (NRXD) - Shows the size of the DMA receive descriptor table. 0b00 = 128, 0b01 = 256, 0b10 = 512, 0b11 = 1024

25 24 Number of transmit descriptors (NTXD) - Shows the size of the DMA transmit descriptor table. 0b00 = 64, 0b01 = 128, 0b10 = 256, 0b11 = 512

23: 21 Link State (LS) - The current state of the start-up sequence. 0 = Error-reset, 1 = Error-wait, 2 = Ready, 3 = Started, 4 = Connecting, 5 = Run.

20: 10 RESERVED

9 Active port (AP) - Shows the currently active port. '0' = Port 0 and '1' = Port 1 where the port numbers refer to the index number of the data and strobe signals. Only available if the *ports* generic is set to 2.

8 Early EOP/EEP (EE) - Set to one when a packet is received with an EOP after the first byte for a non-rmap packet and after the second byte for an RMAP packet.

7 Invalid Address (IA) - Set to one when a packet is received with an invalid destination address field, i.e it does not match the DEFADDR register.

6: 5 RESERVED

4 Parity Error (PE) - A parity error has occurred.

3 Disconnect Error (DE) - A disconnection error has occurred.

2 Escape Error (ER) - An escape error has occurred.

1 Credit Error (CE) - A credit has occurred.

0 Tick Out (TO) - A new time count value was received and is stored in the time counter field.

57.12.3 Default Address Register

*Table 923.*0x08 - DEFADDR - Default address

31 16	15 8	7 0
RESERVED	DEFMASK	DEFADDR
0x0000	0x00	*
r	rw	rw

31: 8 RESERVED

15: 8 Default mask (DEFMASK) - Default mask used for node identification on the SpaceWire network. This field is used for masking the address before comparison. Both the received address and the DEFADDR.DEFADDR field are anded with the inverse of this field before the address check.

7: 0 Default address (DEFADDR) - Default address used for node identification on the SpaceWire network. Reset value: 254 (taken from the *nodeaddr* VHDL generic when /= 255, else from the RMAPNODEADDR input signal)

57.12.4 Clock Divisor Register

*Table 924.*0x0C - CLKDIV - Clock divisor

31 16	15 8	7 0
RESERVED	CLKDIVSTART	CLKDIVRUN
0x0000	*	*
r	rw	rw

31: 16 RESERVED

15: 8 Clock divisor startup (CLKDIVSTART) - The value of this field is used as a clock divider during startup (link interface is in other states than run-state). See 57.3.6 for details on how to set this field. Reset value taken from the CLKDIV10 input signal.

7: 0 Clock divisor run (CLKDIVRUN) - The value of this field is used as a clock divider when the link-interface is in run-state. See 57.3.6 for details on how to set this field. Reset value taken from the CLKDIV10 input signal.

57.12.5 Destination Key Register

*Table 925.*0x10 - DKEY - Destination key

31 8	7 0
RESERVED	DESTKEY
0x000000	*
r	rw

31: 8 RESERVED

7: 0 Destination key (DESTKEY) - RMAP destination key. Only available if the *rmap* VHDL generic is set to 1. Set from *destkey* VHDL generic.

57.12.6 Time-code Register

*Table 926.*0x14 - TC - Time-code

31 8	7 6	5 0
RESERVED	TCTRL	TIMECNT
0x000000	0x0	0x00
r	rw	rw

31: 8 RESERVED

7: 6 Time control flags (TCTRL) - The current value of the time-code control flags. Sent in a time-code each time the TICKIN signal is set, or the CTRL.TI bit is written. This field is also updated with the control flags from all received time-codes, and with the value of the TIMEIN[7:6] signals if TICKINRAW is asserted.

5: 0 Time counter (TIMECNT) - The current time value. Incremented, and transmitted in a time-code, each time the TICKIN signal is set, or the CTRL.TI bit is written. This field is also updated with the time value from all received time-codes, and with the value of the TIMEIN[5:0] signals if TICKINRAW is asserted. Note that the register can be written, but that the written value is not transmitted, since the value is incremented before transmission.

57.12.7 DMA Control/Status

*Table 927.*0x20, 0x40, 0x60, 0x80 - DMACTRL - DMA control/status

31 26	25 24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTNUM	RES	EP	TR	IE	IT	RP	TP	TL	LE	SP	SA	EN	NS	RD	RX	AT	RA	TA	PR	PS	AI	RI	TI	RE	TE
*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rw	r	wc	wc	rw	rw	wc	wc	wc	rw	rw	rw	rw	rw	rw	r	rw	wc	wc	wc	wc	rw	rw	rw	rw	rw

31: 26 Interrupt-number (INTNUM) - The interrupt-number used for this DMA channel when sending an interrupt-code that was generated due to any of the events maskable by the DMACTRL.IE and DMACTRL.IT bits. Reset value is taken from the IRQTXDEFAULT input signal. Field is only present if interrupt distribution is supported, which is indicated by the CTRL.ID bit. Note that this field must be set to a value within the range defined by the INCTRL.NUMINT and INTCTRL.BASEINT fields. A value outside the range will result in no interrupt-code being sent. This field is only available when distributed interrupt is implemented.

25: 24 RESERVED

23 EEP termination (EP) - Set to 1 when a received packet for the corresponding DMA channel ended with an Error End of Packet (EEP) character.

22 Truncated (TR) - Set to 1 when a received packet for the corresponding DMA channel is truncated due to a maximum length violation.

21 Interrupt-code transmit enable on EEP (IE) - When set to 1, and the interrupt-code transmit enable bit (INTCTRL.IT) is set, an interrupt-code is generated when a received packet on this DMA channel ended with an Error End of Packet (EEP) character. Field is only present if interrupt distribution is supported, which is indicated by the CTRL.ID bit. This field is only available when distributed interrupt is implemented.

20 Interrupt-code transmit enable on truncation (IT) - When set to 1, and the interrupt-code transmit enable (INTCTRL.IT) bit in the Interrupt distribution control register is set, an interrupt-code is generated when a received packet on this DMA channel is truncated due to a maximum length violation. Field is only present if interrupt distribution is supported, which is indicated by the CTRL.ID bit. This field is only available when distributed interrupt is implemented.

19 Receive packet IRQ (RP) - This bit is set to 1 when an AMBA interrupt was generated due to the fact that a packet was received for the corresponding DMA channel.

18 Transmit packet IRQ (TP) - This bit is set to 1 when an AMBA interrupt was generated due to the fact that a packet was transmitted for the corresponding DMA channel.

17 Transmitter enable lock (TL) - This bit is set to 1 if the CTRL.TL bit is set, and the transmitter for the corresponding DMA channel is disabled due to a link error (controlled by the DMACTRL.LE bit). While this bit is set, it is not possible to re-enable the transmitter (e.g. not possible to set the DMACTRL.TE bit to 1).

16 Link error disable (LE) - Disable transmitter when a link error occurs. No more packets will be transmitted until the transmitter is enabled again.

15 Strip pid (SP) - Remove the pid byte (second byte) of each packet. The address byte (first byte) will also be removed when this bit is set, independent of the value of the DMACTRL.SA bit.

14 Strip addr (SA) - Remove the addr byte (first byte) of each packet.

13 Enable addr (EN) - Enable separate node address for this channel.

12 No spill (NS) - If cleared, packets will be discarded when a packet is arriving and there are no active descriptors. If set, the core will wait for a descriptor to be activated.

11 Rx descriptors available (RD) - Set to one, to indicate to the core that there are enabled descriptors in the descriptor table. Cleared by the core when it encounters a disabled descriptor.

10 RX active (RX) - Is set to ‘1’ if a reception to the DMA channel is currently active, otherwise it is ‘0’.

9 Abort TX (AT) - Set to one to abort the currently transmitting packet and disable transmissions. If no packet is currently being transmitted, the only effect is to disable transmissions. Self clearing.

*Table 927.*0x20, 0x40, 0x60, 0x80 - DMACTRL - DMA control/status

8	RX AHB error (RA) - An error response was detected on the AHB bus while this receive DMA channel was accessing the bus.
7	TX AHB error (TA) - An error response was detected on the AHB bus while this transmit DMA channel was accessing the bus.
6	Packet received (PR) - This bit is set each time a packet has been received.
5	Packet sent (PS) - This bit is set each time a packet has been sent.
4	AHB error interrupt (AI) - If set, an interrupt will be generated each time an AHB error occurs when this DMA channel is accessing the bus.
3	Receive interrupt (RI) - If set, an interrupt will be generated when a packet is received, if the interrupt enable (IE) bit in the corresponding receive descriptor is set as well. This happens both if the packet is terminated by an EEP or EOP.
2	Transmit interrupt (TI) - If set, an interrupt will be generated when a packet is transmitted, if the interrupt enable (IE) bit in the corresponding transmit descriptor is set as well. The interrupt is generated regardless of whether the transmission was successful or not.
1	Receiver enable (RE) - Set to one when packets are allowed to be received to this channel.
0	Transmitter enable (TE) - Enables the transmitter for the corresponding DMA channel. Setting this bit to 1 will cause the SW-node to read a new descriptor and try to transmit the packet it points to. Note that it is only possible to set this bit to 1 if the TL bit is 0. This bit is automatically cleared when the SW-node encounters a descriptor which is disabled, or if a link error occurs during the transmission of a packet, and the LE bit is set.

57.12.8 DMA RX Maximum Length

*Table 928.*0x24, 0x44, 0x64, 0x84 - DMAMAXLEN - DMA RX maximum length

31 25	24 2	1 0
RESERVED	RXMAXLEN	RES
0x00	n/r	0x0
r	rw	r

31: 25 RESERVED

24: 2 RX maximum length (RXMAXLEN) - Receiver packet maximum length, counted in 32-bit words.

1: 0 RESERVED

57.12.9 DMA Transmit Descriptor Table Address

*Table 929.*0x28, 0x48, 0x68, 0x88 - DMATXDESC - DMA transmit descriptor table address

31 x+1	x 4	3 0
DESCBASEADDR	DESCSEL	RESERVED
n/r	0x00	0x0
rw	rw	r

31: x+1 Descriptor table base address (DESCBASEADDR) - Sets the base address of the descriptor table. The number of bits in this field depends on the size of the DMA transmit descriptor table. The value of x is given by the formula: 9 + STS.NTXD.

x: 4 Descriptor selector (DESCSEL) - Offset into the descriptor table. Shows which descriptor is currently used by the core. For each new descriptor read, the selector will increase with 16 and eventually wrap to zero again. The number of bits in this field depends on the size of the DMA transmit descriptor table. The value of x is given by the formula: 9 + STS.NTXD.

3: 0 RESERVED

57.12.10 DMA Receive Descriptor Table Address

*Table 930.*0x2C, 0x4C, 0x6C, 0x8C - DMARXDESC - DMA receive descriptor table address

31 x+1	x 3	2 0
DESCBASEADDR	DESCSEL	RESERVED
n/r	0x00	0x0
rw	rw	r

31: 10 Descriptor table base address (DESCBASEADDR) - Sets the base address of the descriptor table. The number of bits in this field depends on the size of the DMA receive descriptor table. The value of x is given by the formula: 9 + STS.NRXD.

9: 3 Descriptor selector (DESCSEL) - Offset into the descriptor table. Shows which descriptor is currently used by the core. For each new descriptor read, the selector will increase with 8 and eventually wrap to zero again. The number of bits in this field depends on the size of the DMA receive descriptor table. The value of x is given by the formula: 9 + STS.NRXD

2: 0 RESERVED

57.12.11 DMA Address

*Table 931.*0x30, 0x50, 0x70, 0x90 - DMAADDR - DMA address

31 16	15 8	7 0
RESERVED	MASK	ADDR
0x0000	n/r	n/r
r	rw	rw

31: 8 RESERVED

15: 8 Mask (MASK) - Mask used for node identification on the SpaceWire network. This field is used for masking the address before comparison. Both the received address and the ADDR field are anded with the inverse of MASK before the address check.

7: 0 Address (ADDR) - Address used for node identification on the SpaceWire network for the corresponding dma channel when the EN bit in the DMA control register is set.

57.12.12 Interrupt Distribution Control

*Table 932.*0xA0 - INTCTRL - Interrupt distribution control

31 26	25	24	23	22 21	20	19	18	17 16	15	14	13	12 8	7	6	5 0
INTNUM	RS	EE	IA	RES	TQ	AQ	IQ	RES	AA	AT	IT	RES	ID	II	TXINT
*	0	0	0	0	0	0	0	0	0	0	0	0x00	0	0	*
rw	rw	rw	rw	r	rw	rw	rw	r	rw	rw	rw	r	wc	rw	rw

31: 26 Interrupt number (INTNUM) - The interrupt-number used when sending an interrupt-code that was generated due to any of the events maskable by the RS, ER or IA bits. Reset value is taken from the IRQTXDEFAULT input signal. Note that this field must be set to a value within the range defined by the NUMINT and BASEINT fields. A value outside the range will result in no interrupt-code being sent.

25 Interrupt-code transmit on run-state entry (RS) - If set to 1, and interrupt-code with the interrupt number specified in the INTNUM field is sent each time the link interface enters run-state.

24 Interrupt-code transmit on early EOP/EEP (EE) - If set to 1, an interrupt-code with the interrupt number specified in the INTNUM field is sent each time an event occurs such that the STS.EE bit is set to 1 (even if the bit was already set when the event occurrepriod).

23 Interrupt-code transmit on invalid address (IA) - If set to 1, an interrupt-code with the interrupt number specified in the INTNUM field is sent each time an event occurs such that the STS.IA bit is set to 1 (even if the bit was already set when the event occurred).

22: 21 RESERVED

20 Interrupt-code timeout IRQ enable (TQ) - When set to 1, an AMBA interrupt is generated when a bit in the INTTO register is set. Note that the IE bit in the Control register also must be set for this bit to have any effect. Bit is only available if support for the Interrupt distribution ISR timer is implemented.

19 Interrupt-code-acknowledge receive IRQ enable (AQ) - When set to 1, an AMBA interrupt is generated when an interrupt-acknowledge-code is received for which the corresponding bit in the Interrupt tick-out mask register is set, and the core was the source of the matching interrupt-code. Note that the IE bit in the Control register also must be set for this bit to have any effect.

18 Interrupt-code receive IRQ enable (IQ) - When set to 1, an AMBA interrupt is generated when an interrupt-code is received for which the corresponding bit in the Interrupt tick-out mask register is set to 1. Note that the IE bit in the Control register also must be set for this bit to have any effect.

17: 16 RESERVED

15 Handle all interrupt acknowledgement codes (AA) - Is set to 0, only those received interrupt acknowledgement codes that match an interrupt code sent by software are handled. If set to 1, all received interrupt acknowledgement codes are handled.

14 Interrupt acknowledgement / extended interrupt tickout enable (AT) - When set to 1, the internal tickout signal is set when an interrupt acknowledgement code or extended interrupt code is received such that a bit in the AUTOACK / INTRXEXT register is set to 1 (even if the bit was already set when the code was received).

*Table 932.*0xA0 - INTCTRL - Interrupt distribution control

13	Interrupt tickout enable (IT) - When set to 1, the internal tickout signal is set when an interrupt code is received such that a bit in the INTRX register is set to 1 (even if the bit was already set when the code was received).
12: 8	RESERVED
7	Interrupt-code discarded (ID) - This bit is set to 1 when and interrupt-code that software tried to send by writing the II bit was discarded, either because there already was a pending request to send an interrupt-code with the same interrupt-number, or because the corresponding ISR bit is 1. There is a one clock cycle delay between the II bit being written and this bit being set.
6	Interrupt-code tick-in (II) - When this field is written to 1 the interrupt- / interrupt-acknowledge-code specified in the TXINT field will be sent. The actual sending of the interrupt- / interrupt-acknowledge-code might be delayed, depending on the value for the corresponding ISR bit and INT/ACK-timer. Note that the interrupt-code transmit enable bit (IT) must be set to '1', otherwise writing this bit has no effect. This bit is automatically cleared and always reads '0'. Writing a '0' has no effect.
5: 0	Transmit interrupt- / interrupt-code (TXINT) - The interrupt- / interrupt-acknowledge-code that the core will send when the Interrupt-code tick-in bit (II) is written with 1. Reset value for bit 5 is '0', while bits 4:0 are set from the input signal IRQTXDEFAULT. Note that bits 4:0 of this field must be set to a value within the range defined by the NUMINT and BASEINT fields. A value outside the range will result in no interrupt-code being sent.

57.12.13 Interrupt Receive

*Table 933.*0xA4 - INTRX - Interrupt-code receive

31	0
RXIRQ	
0x00000000	
wc	

31: 0 Received interrupt-code (RXIRQ) - Each bit corresponds to the interrupt number with the same number as the bit index. The core sets a bit to 1 when it receives an interrupt-code for which the corresponding bit in the Interrupt tick out mask register is set to 1. Note that the number of implemented bits depends on the number of supported interrupts (INTCTRL.NUMINT field).

57.12.14 Interrupt-acknowledge-code Receive

*Table 934.*0xA8 - ACKRX / INTRXEXT - Interrupt-acknowledge-code receive / Interrupt receive extended

31	0
RXACK / INTRXEXT	
0x00000000	
wc	

31: 0 Received interrupt-acknowledge-code (RXACK) / Interrupt receive extended (INTRXEXT) - Each bit corresponds to the interrupt number with the same number as the bit index. The core sets a bit to 1 when it receives a interrupt-acknowledge-code for which the corresponding bit in the Interrupt tick out mask register is set, and for which the matching interrupt-code was sent by software (valid for interrupt-acknowledge). Note that the number of implemented bits depends on the number of supported interrupts (INTCTRL.NUMINT field). When extended interrupt mode is enabled this register is an extension of the Interrupt Receive register for interrupt 32-63.

57.12.15 Interrupt Timeout

*Table 935.*0xAC - INTTO - Interrupt timeout

31	0
INTTO	
0x00000000	
wc	

31: 0 Interrupt-code timeout (INTTO) - Each bit corresponds to the interrupt number with the same number as the bit index. The core sets a bit to 1 when an interrupt-code that was sent by software doesn't receive an interrupt-acknowledge-code for the duration of a timeout period (specified in the Interrupt distribution ISR timer reload registers), and if the corresponding bit in the Interrupt-code tick out mask register is set. Note that the number of implemented bits depends on the number of supported interrupts (INTCTRL.NUMINT field).

57.12.16 Interrupt Timeout Extended

*Table 936.*0xB0 - INTTOEXT - Interrupt timeout extended

31	0
INTTOEXT	
0x00000000	
wc	

31: 0 Interrupt timeout extended (INTTOEXT) - When extended interrupt mode is enabled, each bit corresponds to the interrupt number between 32 and 63. The core sets a bit to 1 when an interrupt-code that was sent by software and the time specified in the Interrupt distribution ISR timer reload registers has past and if the corresponding bit in the Interrupt-code tick out mask register is set. Note that the number of implemented bits depends on the number of supported interrupts (INTCTRL.NUMINT field).

57.12.17 Interrupt Tick-out Mask

*Table 937.*0xB4 - TICKMASK - Interrupt tick-out mask

31	0
MASK	
0x00000000	
rw*	

31: 0 Interrupt tick-out mask (MASK) - Each bit corresponds to the interrupt number with the same value as the bit index. If a bit is set, the TICKOUT signal as well as the corresponding bit in the Interrupt-code receive register, Interrupt-acknowledge-code receive register, and Interrupt-code timeout register is set when respective event occurs. Note that the number of implemented bits depends on the number of supported interrupts (INTCTRL.NUMINT field).

57.12.18 Interrupt-code Auto Acknowledge Mask

*Table 938.*0xB8 - AUTOACK / TICKMASKEXT - Interrupt-code auto acknowledge mask / Interrupt tick-out mask extended.

31	0
AAMASK	
0x00000000	
rw*	

31: 0 Auto acknowledge mask (AAMASK) - For each bit set to 1, the core will automatically send an interrupt-acknowledge-code when it receives an interrupt-code with the corresponding interrupt number. If the interrupt distribution timers are implemented (VHDL generic intiatimerbits /= 0) and enabled, then the core will reload the INT-to-ACK timer and wait until it expires before the interrupt-acknowledge-code is sent. Note that the number of implemented bits depends on the number of supported interrupts (INTCFG.NUMINT field). When extended interrupt mode is enabled this register is an extension of the Interrupt Tick-out Mask register.

57.12.19Interrupt Distribution Configuration

*Table 939.*0xBC - INTCFG - Interrupt distribution control

31 26	25 20	19 14	13 8	7 4	3	2	1	0
INTNUM3	INTNUM2	INTNUM1	INTNUM0	NUMINT	PR	IR	IT	EE
*	*	*	*	0	0	0	0	0
rw	rw		rw	r	rw	rw	rw	rw

31: 26 Interrupt number (INTNUM3) - Defines the which interrupt number to support when the device supports less then 32 interrupts.

25: 20 Interrupt number (INTNUM2) - Defines the which interrupt number to support when the device supports less then 32 interrupts.

19: 14 Interrupt number (INTNUM1) - Defines the which interrupt number to support when the device supports less then 32 interrupts.

13: 8 Interrupt number (INTNUM0) - Defines the which interrupt number to support when the device supports less then 32 interrupts.

7: 4 Number of interrupts (NUMINT) - Indicates the number of supported interrupts according to the formula: *Number of interrupts* = 2^{NUMINT}.

3 Interrupt- / interrupt-acknowledge-code priority (PR) - When set to 0, interrupt-codes have priority over interrupt-acknowledge-codes when there are multiple codes waiting to be sent. When set to 1, interrupt-acknowledge-codes have priority.

2 Interrupt receive enable (IR) - Enable interrupt- / interrupt-acknowledge-code reception.

1 Interrupt transmit enable (IT) - Enable interrupt- / interrupt-acknowledge-code transmission. Must be set to 1 in order for any interrupt- / interrupt-acknowledge-codes to be sent.

0 Enable external interrupt (EE) - Enable the external interrupt mode, which enable the core to use and interpret the interrupt-acknowledge-code as interrupt 32-63.

57.12.20 Interrupt Distribution ISR

*Table 940.*0xC4 - ISR - Interrupt distribution ISR

31	0
ISR	
0x00000000	
wc	

31: 0 Interrupt distribution ISR (ISR) - Each bit index holds the ISR bit value for the corresponding interrupt number. A bit value of 1 indicates that a interrupt-code with the corresponding interrupt number has been received, and that it has not yet been acknowledged (and not yet timed-out). A bit value of 0 indicates that either no interrupt-code with that interrupt number has been received, or that the interrupt has been acknowledged (or timed out). This register is write-clear, but should normally only be used for diagnostics and/or FDIR. Note that the number of implemented bits depends on the number of supported interrupts (INTCTRL.NUMINT field).

57.12.21 Interrupt Distribution ISR Extended

*Table 941.*0xC4 - ISREXT - Interrupt distribution ISR extended

31	0
ISR	
0x00000000	
wc	

31: 0 Interrupt distribution ISR (ISR) - Each bit index holds the ISR bit value for the corresponding interrupt number. A bit value of 1 indicates that a interrupt-code with the corresponding interrupt number has been received, and that it has not yet been acknowledged (and not yet timed-out). A bit value of 0 indicates that either no interrupt-code with that interrupt number has been received, or that the interrupt has been acknowledged (or timed out). This register is write-clear, but should normally only be used for diagnostics and/or FDIR. Note that the number of implemented bits depends on the number of supported interrupts (INTCTRL.NUMINT field).

57.12.22 Interrupt Distribution Prescaler Reload

*Table 942.*0xD0 - PRESCALER - Interrupt distribution prescaler reload

31	30	0
R	RL	
0	*	
r	rw	

31 RESERVED

30: 0 Prescaler reload (RL) - Reload value for the interrupt distribution prescaler. The prescaler runs on the system clock, and an internal tick is generated every RL+1 cycle. The number of bits implemented for this field is set by the VHDL generic *intscalerbits*, and might be lower than the 31 depicted here. Any unimplemented bits are reserved. Reset value set from the input signal INTPRELOAD.

57.12.23 Interrupt Distribution ISR Timer Reload

*Table 943.*0xD4 - ISRTIMER - Interrupt distribution ISR timer reload

31	30 … 0
EN	RL
1	*
rw	rw

31 Timer enable (EN) - Enables the use of ISR timer for each ISR bit. One global timer enable bit used for all ISR bits. If this bit is set to 1, the timer for each ISR bit is reloaded with the value in the RL field when the ISR bit is set. If the timer expires before an interrupt-code-acknowledge has been received, then ISR bit is cleared.

30: 0 Timer reload (RL) - Common reload value for the interrupt distribution ISR timers. The number of bits implemented for this field is set by the VHDL generic *intisrtimerbits*, and might be lower than the 31 depicted here. Any unimplemented bits are reserved. Reset value set from the input signal INTTRELOAD.

57.12.24 Interrupt Distribution INT/ACK Timer Reload

*Table 944.*0xD8 - IATIMER - Interrupt distribution INT / ACK timer reload

31	30 … 0
EN	RL
1	*
rw	rw

31 Timer enable (EN) - Enables the use of timers to control the time between an interrupt-code and an interrupt-acknowledge-code, and vice versa. One global timer enable bit is used for all ISR bits. If this bit is set to 1, the timer for each ISR bit is reloaded with the value in the RL field each time an interrupt-code is received. The core will then wait until the timer expires before an interrupt-code-acknowledge with the same interrupt number is sent. The same applies when an interrupt-code-acknowledge is received and a new interrupt-code with the same number should be sent.

30: 0 Timer reload (RL) - The number of bits implemented for this field is set by the VHDL generic *intiatimerbits*, and might be lower than the 31 depicted here. Any unimplemented bits are reserved. Reset value set from the input signal INTIARELOAD.

57.12.25 Interrupt Distribution Change Timer Reload

*Table 945.*0xDC - ICTIMER - Interrupt distribution change timer reload

31	30 … 0
EN	RL
1	*
rw	rw

31 Timer enable (EN) - Enables the use of timers to control the time that must pass between two changes in value for the same ISR bit. One global timer enable bit is used for all ISR bits. If this bit is set to 1, the timer for each ISR bit is reloaded with the value in the RL field each time the ISR bit changes value. All potential interrupt- / interrupt-acknowledge-codes received before the timer expires is discarded.

30: 0 Timer reload (RL) - The number of bits implemented for this field is set by the VHDL generic *intctimerbits*, and might be lower than the 31 depicted here. Any unimplemented bits are reserved. Reset value set from the input signal INTCRELOAD.

57.12.26 SpaceWire Plug-and-Play - Device Vendor and Product ID

*Table 946.*0xE0 - PNPVEND - SpaceWire Plug-and-Play - Device Vendor and Product ID

31 16	15 0
VEND	PROD
*	*
r	r

Note: Register is double mapped from SpaceWire Plug-and-Play address space into APB address space. See section 57.10 for details.

57.12.27 SpaceWire Plug-and-Play - Link Information

*Table 947.*0xE4 - PNPLINFO -SpaceWire Plug-and-Play - Link Information

31 24	23	22	21	20 16	15 13	12 8	7	6	5	4 0
OLA	OAL	R		OL	RES	RL	T	U	R	LC
0x00	0x0	0		0x0	0x0	0x0	1	0	0	0x13
r	r	r		r	r	r	r	r	r	r

Note: Register is double mapped from SpaceWire Plug-and-Play address space into APB address space. See section 57.10 for details.

57.12.28 SpaceWire Plug-and-Play - Owner Address 0

*Table 948.*0xE8 - PNPOA0 - SpaceWire Plug-and-Play - Owner Address 0

31 0
RA
0x00000000
r

Note: Register is double mapped from SpaceWire Plug-and-Play address space into APB address space. See section 57.10 for details.

57.12.29 SpaceWire Plug-and-Play - Owner Address 1

*Table 949.*0xEC - PNPOA1 - SpaceWire Plug-and-Play - Owner Address 1

31 0
RA
0x00000000
r

Note: Register is double mapped from SpaceWire Plug-and-Play address space into APB address space. See section 57.10 for details.

57.12.30 SpaceWire Plug-and-Play - Owner Address 2

*Table 950.*0xF0 - PNPOA2 - SpaceWire Plug-and-Play - Owner Address 2

31 0
RA
0x00000000
r

Note: Register is double mapped from SpaceWire Plug-and-Play address space into APB address space. See section 57.10 for details.

57.12.31 SpaceWire Plug-and-Play - Device ID

*Table 951.*0xF4 - PNPDEVID - SpaceWire Plug-and-Play - Device ID

31	0
DID	
0x00000000	
r	

Note: Register is double mapped from SpaceWire Plug-and-Play address space into APB address space. See section 57.10 for details.

57.12.32 SpaceWire Plug-and-Play - Unit Vendor and Product ID

*Table 952.*0xF8 - PNPUVEND - SpaceWire Plug-and-Play - Unit Vendor and Product ID

31	16	15	0
VEND		PROD	
*		*	
rw		rw	

Note: Register is double mapped from SpaceWire Plug-and-Play address space into APB address space. See section 57.10 for details. This register is read-only in SpaceWire Plug-and-Play interface, while it is writable from the APB address space.

57.12.33 SpaceWire Plug-and-Play - Unit Serial Number

*Table 953.*0xFC - PNPUSN - SpaceWire Plug-and-Play - Unit Serial Number

31	0
USN	
*	
rw	

Note: Register is double mapped from SpaceWire Plug-and-Play address space into APB address space. See section 57.10 for details. This register is read-only in SpaceWire Plug-and-Play interface, while it is writable from the APB address space.

57.13 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x29. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

57.14 Configuration options

Table 954 shows the configuration options of the core (VHDL generics).

*Table 954.*Configuration options

Generic	Function	Allowed values	Default
tech	Selects technology for transmitter DDR registers (if output_type=1) and enables a reset of additional registers for ASIC technologies.	0 - NTECH	inferred
hindex	AHB master index.	0 - NAHBMST-1	0
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	Addr field of the APB bar.	0 - 16#FFF#	0
pmask	Mask field of the APB bar.	0 - 16#FFF#	16#FFF#
pirq	Interrupt line used by GRSPW2.	0 - NAHBIRQ-1	0
rmap	Include hardware RMAP target. RMAP CRC logic will also be added. If set to 2 the core will only implement the RMAP target, provide a limited APB interface, enable time code reception and its interrupt.	0 - 2	0
rmapcrc	Enable RMAP CRC logic.	0 - 1	0
ccsdscrc	Enables CCSDS/CCITT CRC-16 and 16-bit ISO-checksum (J.G. Fletcher, ISO 8473-1:1998) logic. For the core to calculate CRC rmap or rmapcrc also need to be set to 1.	0 - 1	0
fifosize1	Sets the number of entries in the 32-bit receiver and transmitter AHB fifos.	4 - 64	32
fifosize2	Sets the number of entries in the 9-bit receiver fifo (N-Char fifo).	16 - 64	64
rxunaligned	Receiver unaligned write support. If set, the receiver can write any number of bytes to any start address without writing any excessive bytes.	0 - 1	0
rmapbufs	Sets the number of buffers to hold RMAP replies.	2 - 8	4
ft	Enable fault-tolerance against SEU errors. The core can optionally be implemented with fault-tolerance against SEU errors in the FIFO memories. The fault-tolerance is enabled through the ft VHDL generic to 1 or 2. Possible options are byte parity protection (ft = 1) or TMR registers (ft = 2).	0 - 2	0
scantest	Enables scantest support	0 - 1	0
techfifo	Enables technology specific RAM blocks selected with memtech. When disabled the memtech generic will have no effect.	0 - 1	1
ports	Sets the number of ports	1 - 2	1
dmachan	Sets the number of DMA channels	1 - 4	1
memtech	Selects technology for RAM blocks.	0 - NTECH	DEFMEMTECH
input_type	Select receiver type. 0 = Self clocking (xor), 1 = Interface for Cobham SpaceWire transceiver, 2 = Single data rate sampling, 3 and 4 = Double data rate sampling, 5 = Self-clocking with external recovery, 6 = Self-clocking with external recovery and DDR register for data.. This generic must be set to the same value as the GRSPW2_PHY generic with the same name.	0 - 6	0
output_type	Select transmitter type. 0 = Single data rate, 1 = Double data rate, 2 = Interface for Cobham SpaceWire transceiver.	0 - 2	0

*Table 954.*Configuration options

Generic	Function	Allowed values	Default
rxtx_sameclk	Set to one if the same clock net is connected to both the receiver and transmitter (which means this feature is only applicable when the receiver uses sampling). This will remove some unnecessary synchronization registers.	0 - 1	0
netlist	Select pre-synthesized netlist instead of synthesizing from source. When enabled the specific netlist is selected with the tech generic.	0 - 1	0
nodeaddr	When set to 0 - 254: Generic specifies the reset value for the node address (DEFADDR.DEFADDR field). When set to 255: Reset value for the node address is taken from the RMAPNODEADDR input signal.	0 - 255	254
destkey	Sets the reset value for the core's destination key.	0 - 255	0
interruptdist	Enables interrupt distribution support and sets the number of supported interrupts.	0, 1, 2, 4, 8, 16, 32	0
intscalerbits	Sets the number of bits for the interrupt distribution prescaler. 0 = No Interrupt distribution prescaler implemented.	0 - 31	0
intisrtimerbits	Sets the number of bits for the Interrupt distribution ISR timers. 0 = No Interrupt distribution ISR timer implemented.	0 - 31	0
intiatimerbits	Sets the number of bits for the Interrupt distribution INT / ACK timers. 0 = No Interrupt distribution INT / ACK timers implemented.	0 - 31	0
intctimerbits	Sets the number of bits for the Interrupt distribution change timers. 0 = No Interrupt distribution change timers implemented.	0 - 31	0
tickinasync	Determines whether the TICKIN, TICKINRAW, and TIMEIN signals are synchrnous or asynchronous to CLK. 0 = synchronous, 1 = asynchronous	0 - 1	0
pnp	Enabled / disables support for SpaceWire Plug-and-Play	0 - 1	0
pnpvendid	Specifies the SpaceWire Plug-and-Play Device Vendor ID	0 - 16#FFFF#	0
pnpprodid	Specifies the SpaceWire Plug-and-Play Device Product ID	0 - 16#FFFF#	0
pnpmajorver	Specifies the device's SpaceWire Plug-and-Play Major Version	0 - 16#FFFF#	0
pnpminorver	Specifies the device's SpaceWire Plug-and-Play Minor Version	0 - 16#FFFF#	0
pnppatch	Specifies the device's SpaceWire Plug-and-Play Patch/ Build Number	0 - 16#FFFF#	0
num_txdesc	Specifies the number of entries in the transmit descriptor table	64, 128, 256, 512	64
num_rxdesc	Specifies the number of entries in the receive descriptor table	128, 256, 512, 1024	128
rstsrctmr	Enables the Triple Module Redundancy for the asynchronous reset nets of the core	0 - 1	0

57.15 Signal descriptions

Table 955 shows the interface signals of the core (VHDL ports).

Table 955. Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
RXASYNCRST	N/A	Input	Asynchronous reset for ports 0 and 1 of the receiver	Low
RXSYNCRST0	N/A	Input	Synchronous reset for port 0 of the receiver	Low
RXCLK0	N/A	Input	Receiver clock for port 0	-
RXSYNCRST1	N/A	Input	Synchronous reset for port 1 of the receiver	Low
RXCLK1	N/A	Input	Receiver clock for port 1. Unused in one-port configurations.	-
TXSYNCRST	N/A	Input	Synchronous reset for the transmitter	Low
TXCLK	N/A	Input	Transmitter default run-state clock	-
TXCLKN	N/A	Input	Transmitter inverted default run-state clock. Only used in DDR transmitter mode for technologies not supporting local generation of inverted clock.	-
AHBMI	*	Input	AMB master input signals	-
AHBMO	*	Output	AHB master output signals	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
SWNI	D[3:0]	Input	Data input. Bits 3:2 are unused in one-port configurations.	-
	DV[3:0]	Input	Data valid. Bits 3:2 are unused in one-port configurations.	-
	DCONNECT[3:0]	Input	Disconnect. Bits 3:2 are unused in one-port configurations.	
	DCONNECT2[3:0]	Input	Disconnect. Bits 3:2 are unused in one-port configurations. This is a copy of DCONNECT, as part of the triplication of the combinational logic related to asynchronous reset nets.	
	DCONNECT3[3:0]	Input	Disconnect. Bits 3:2 are unused in one-port configurations. This is a copy of DCONNECT, as part of the triplication of the combinational logic related to asynchronous reset nets.	
	TICKIN	Input	Time counter tick input. Increments internal time-counter and transmits the new value.	High
	TICKINRAW	Input	Raw tick input. Send time-code or interrupt- / interrupt-acknowledge-code from TIMEIN signal. TICKINRAW must be deasserted the same clock cycle as the output signal TICKINDONE is asserted.	High
	TIMEIN[7:0]	Input	The time-code or interrupt- / interrupt-acknowledge-code sent when TICKINRAW is asserted.	
	CLKDIV10[7:0]	Input	Reset value for the Clock divisor register.	-
	RMAPEN	Input	Reset value for the CTRL.RE bit (RMAP enable bit in the Control register).	-

Table 955. Signal descriptions

Signal name	Field	Type	Function	Active
	RMAPNODEADDR[7:0]	Input	Reset value for the node address (DEFADDR.DEFADDR field) when the *nodeaddr* VHDL generic = 255. Unused if *nodeaddr* /= 255.	-
	INTPRELOAD[30:0]	Input	Reset value for the Interrupt distribution prescaler reload register	-
	INTTRELOAD[30:0]	Input	Reset value for the Interrupt distribution ISR timer reload register	-
	INTIARELOAD[30:0]	Input	Reset value the Interrupt distribution INT / ACK timer reload register	-
	INTCRELOAD[30:0]	Input	Reset value the Interrupt distribution change timer reload register	-
	IRQTXDEFAULT[5:0]	Input	Reset value for the differemt transmit interrupt numbers for the interrupt distribution	-
	PNPEN	Input	Reset value for the SpaceWire Plug-and-Play enable bit (CTRL.PE)	-
	PNPUVENDID	Input	Reset value for the SpaceWire Plug-and-Play Unit Vendor ID (PNPUVEND.VEND field)	-
	PNPUPRODID	Input	Reset value for the SpaceWire Plug-and-Play Unit Product ID (PNPUVEND.PROD field)	-
	PNPUSN	Input	Reset value for the SpaceWire Plug-and-Play Unit Serial Number (PNPUSN register)	-

Table 955. Signal descriptions

Signal name	Field	Type	Function	Active
SWNO	D[3:0]	Output	Data output. Bits 3:2 are unused in one-port configurations.	-
	S[3:0]	Output	Strobe output. Bits 3:2 are unused in one-port configurations.	-
	TICKOUT	Output	Tick-out signal that is asserted when a valid time-code or interrupt- / interrupt-acknowledge-code has been received.	High
	TICKOUTRAW	Output	Tick-out that is always asserted when a time-code or interrupt- / interrupt-acknowledge-code is received.	High
	TIMEOUT[7:0]	Output	Contains the received time-code or interrupt- / interrupt-acknowledge-code when TICKOUTRAW is asserted.	
	TICKINDONE	Output	Asserted when a time-code or interupt- / interrupt-acknowledge-code sent via the TICKINRAW signal has been accepted for transmission. TICKINRAW must be deasserted the same clock cycle as TICKINDONE is asserted.	High
	RXDAV	Output	Asserted for one CLK cycle when a character has been receved on the SpaceWire link.	High
	RXDATAOUT[8:0]	Output	When RXDAV is asserted, these signals contain the received character.	
	LINKDIS	Output	Asserted when the link is disabled	High
	LOOPBACK	Output	Reflects the value of the loopback bit in the Control register. Can be used to control on-chip loopback for test purposes.	High
	RXRST	Output	Internal reset generated by the transmitter for synchronization purpose between transmitter and both receiver channels. It shall be used to generate the asynchronous and synchronous receiver resets.	Low
	CTRLREGRST	Output	Register reset. It corresponds to the bit 6 of the Control Register (see 57.12.1. Control Register). It shall be used negated (it is active high) to generate the AMBA and transmitter resets.	High
* see GRLIB IP Library User's Manual				

57.16 Signal definitions and reset values

The signals and their reset values are described in table 956.

*Table 956.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
spw_clk	Input	Transmitter default run-state clock	Rising edge	-
spw_rxd	Input, LVDS	Data input, positive	High	-
spw_rxdn	Input, LVDS	Data input, negative	Low	-
spw_rxs	Input, LVDS	Strobe input, positive	High	-
spw_rxsn	Input, LVDS	Strobe input, negative	Low	-
spw_txd	Output, LVDS	Data output, positive	High	Logical 0
spw_txdn	Output, LVDS	Data output, negative	Low	Logical 1
spw_txs	Output, LVDS	Strobe output, positive	High	Logical 0
spw_txsn	Output, LVDS	Strobe output, negative	Low	Logical 1

57.17 Timing

The timing waveforms and timing parameters are shown in figure 157 and are defined in table 957.

The SpaceWire jitter and skew timing waveforms and timing parameters are shown in figure 158 and are defined in table 958.

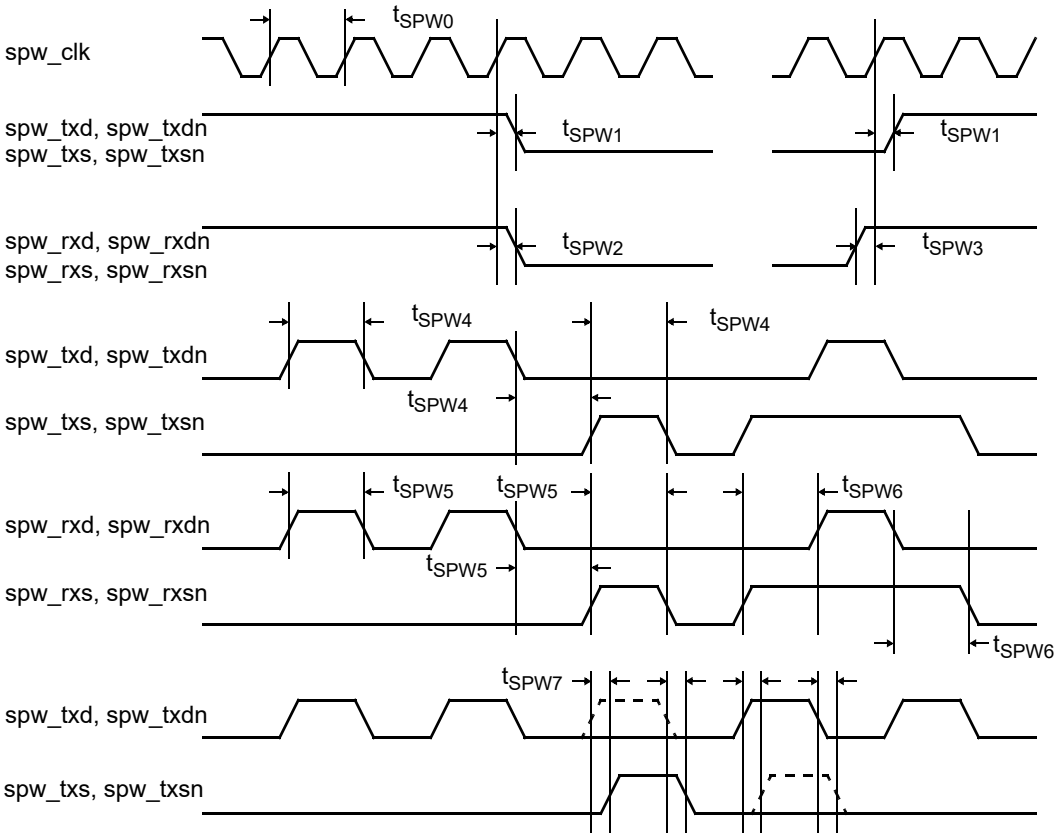


Figure 157. Timing waveforms

*Table 957.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{SPW0}	transmit clock period	-	TBD	-	ns
t_{SPW1}	clock to output delay	rising *spw_clk* edge	TBD	TBD	ns
t_{SPW2}	input to clock hold	-	-	-	not applicable
t_{SPW3}	input to clock setup	-	-	-	not applicable
t_{SPW4}	output data bit period	-	-		*clk* periods
		-	t_{SPW0} - TBD	t_{SPW0} +TBD	ns
t_{SPW5}	input data bit period	-	TBD	-	ns
t_{SPW6}	data & strobe edge separation	-	TBD	-	ns
t_{SPW7}	data & strobe output skew	-	-	TBD	ns

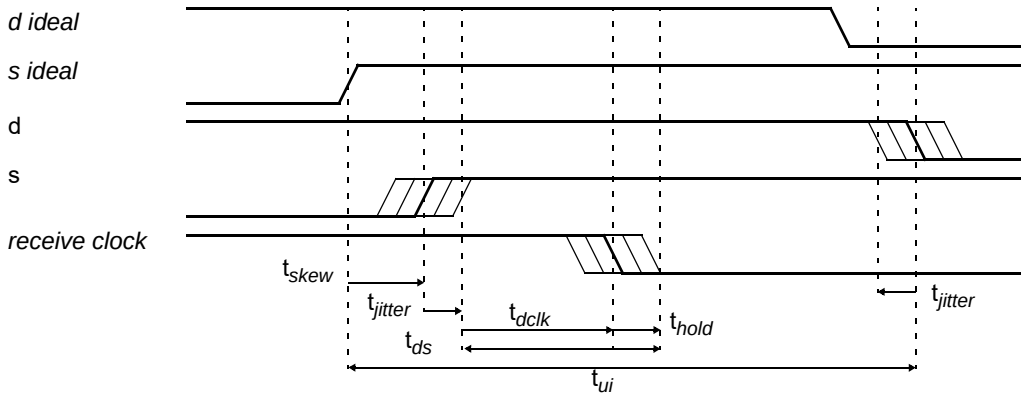


Figure 158. Skew and jitter timing waveforms

*Table 958.*Skew and jitter timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{skew}	skew between data and strobe	-	-	TBD	ns
t_{jitter}	jitter on data or strobe	-	-	TBD	ns
t_{ds}	minimum separation between data and strobe edges	-	TBD	-	ns
t_{dclk}	delay from edge of data or strobe to the receiver flip-flop	-	-	TBD	ns
t_{hold}	hold timer on receiver flip-flop	-	TBD	-	ns
t_{ui}	unit interval (bit period)	-	TBD	-	ns

57.18 Library dependencies

Table 959 shows libraries used when instantiating the core (VHDL libraries).

*Table 959.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	SPACEWIRE	Signals, component	Component and record declarations.

57.19 Instantiation

This example shows how the core can be instantiated.

Normally di, si, do and so should be connected to input and output pads configured with LVDS drivers. How this is done is technology dependent.

The core in the example is configured with non-ft memories of size 32, 32 and 4 entries for AHB FIFOs, N-Char FIFO and RMAP buffers respectively.

The memory technology is inferred which means that the synthesis tool will select the appropriate components.

The hardware RMAP target is enabled which also automatically enables rxunaligned and rmapcrc.

The core can be instantiated directly (grspw2) or using a wrapper (grspwm). In the first case, the top level instance is in charge of generating the resets appropriately, whereas the wrapper may include the reset generation and synchronization if the generic internalrstgen is set to 1 (default value).

Example of direct instantiation, including reset generators:

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.spacewire.all;

entity spacewire_ex is
  port (
    clk           : in  std_ulogic;
    rstn          : in  std_ulogic;

    -- spacewire signals
    spw_rxdp      : in  std_ulogic;
    spw_rxdn      : in  std_ulogic;
    spw_rxsp      : in  std_ulogic;
    spw_rxsn      : in  std_ulogic;
    spw_txdp      : out std_ulogic;
    spw_txdn      : out std_ulogic;
    spw_txsp      : out std_ulogic;
    spw_txsn      : out std_ulogic;

    spw_rxtxclk   : in  std_ulogic;
    spw_rxclkn    : in  std_ulogic
    );
end;

architecture rtl of spacewire_ex is

  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);

  -- Spacewire signals
  signal swni      : grspw_in_type;
  signal swno      : grspw_out_type;
  signal dtmp      : std_ulogic;
  signal stmp      : std_ulogic;
  signal rxclk0    : std_ulogic;
  -- Only 1 port in this design. rxclk1 is unused. Instantiate
  -- two PHY's (grspw2_phy) if two ports are enabled in the receiver
  signal rxclk1    : std_ulogic := '0';

  -- Internal resets
  signal tmp_reset : std_ulogic;
  signal mrst      : std_ulogic;
  signal rxasyncrst: std_ulogic;
  signal rxsyncrst0: std_ulogic;
  signal rxsyncrst1: std_ulogic := '0'; -- Unused in this design
  signal txsyncrst : std_ulogic;

begin

  -- AMBA Components are instantiated here

  spw_phy0 : grspw2_phy
    generic map(
      scantest   => 0,
      tech       => 0,
      input_type => 3)
    port map(
      rstn       => rstn,
      rxclki     => spw_rxtxclk,
      rxclkin    => spw_rxclkn,
      nrxclki    => spw_rxtxclk,
```

```
    di         => dtmp,
    si         => stmp,
    do         => swni.d(1 downto 0),
    dov        => swni.dv(1 downto 0),
    dconnect   => swni.dconnect(1 downto 0),
    dconnect2  => swni.dconnect2(1 downto 0),
    dconnect3  => swni.dconnect3(1 downto 0),
    rxclko     => rxclk0);

-- Internal reset generators (TX, RX0 and RX1 clock domains)

-- The AMBA and TX resets take into account the bit 6 of the Control
-- Register (software reset)
tmp_reset <= rstn and not swno.ctrlregrst;

-- CLK domain (synchronous reset)
AMBA_rst : rstgen
port map (tmp_reset, clk, vcc, mrst, open);

-- TX domain (synchronous reset)
txrst : rstgen
port map (tmp_reset, spw_rxtxclk, vcc, txsyncrst, open);

-- RX domain (asynchronous reset)
rxasyncrst <= swno.rxrst;

-- RX domain (synchronous reset)
rxsyncrst0 : rstgen
port map (swno.rxrst, rxclk0, vcc, rxsyncrst0, open);
-- RXCLK1 is unused. Uncomment if two ports are enabled
--rxsyncrst1 : rstgen
--port map (swno.rxrst, rxclk1, vcc, rxsyncrst1, open);

sw0 : grspw2
generic map(
  tech         => 0,
  hindex       => 0,
  pindex       => 10,
  paddr        => 10,
  pirq         => 10,
  ports        => 1,
  dmachan      => 1,
  rmap         => 1,
  rmapcrc      => 1,
  fifosize1    => 32,
  fifosize2    => 32,
  rxunaligned  => 1,
  rmapbufs     => 4,
  output_type  => 1,
  input_type   => 3,
  rxtx_sameclk => 1)
port map(mrst, clk, rxasyncrst, rxsyncrst0, rxclk0, rxsyncrst1, rxclk1,
     txsyncrst, spw_rxtxclk, spw_rxtxclk, ahbmi, ahbmo(0), apbi, apbo(10),
     swni, swno);

swni.tickin <= '0'; swni.rmapen <= '1';
swni.clkdiv10 <= conv_std_logic_vector(SPW_TX_FREQ_KHZ/10000-1, 8);

spw_rxd_pad : inpad_ds generic map (padtech, lvds, x25v)
  port map (spw_rxdp, spw_rxdn, dtmp);
spw_rxs_pad : inpad_ds generic map (padtech, lvds, x25v)
  port map (spw_rxsp, spw_rxsn, stmp);
spw_txd_pad : outpad_ds generic map (padtech, lvds, x25v)
  port map (spw_txdp, spw_txdn, swno.d(0), gnd(0));
spw_txs_pad : outpad_ds generic map (padtech, lvds, x25v)
  port map (spw_txsp, spw_txsn, swno.s(0), gnd(0));
...
```

Example using the wrapper and the internal reset generators enabled. Replace the reset generators and the GRSPW2 core with the following wrapper:

```
sw0 : grspwm
generic map(
     tech           => fabtech,
     hindex         => CFG_NCPU+CFG_AHB_UART+CFG_AHB_JTAG+CFG_GRETH+i,
     pindex         => 13+i,
     paddr          => 13+i,
     pirq           => 8+i,
     sysfreq        => CPU_FREQ,
     nsync          => 1,
     rmap           => CFG_SPW_RMAP,
     rmapcrc        => CFG_SPW_RMAPCRC,
     fifosize1      => CFG_SPW_AHBFIFO,
     fifosize2      => CFG_SPW_RXFIFO,
     rxclkbuftype   => 1,
     memtech        => memtech,
     rmapbufs       => CFG_SPW_RMAPBUF,
     ft             => CFG_SPW_FT,
     ports          => CFG_SPW_PORTS,
     dmachan        => CFG_SPW_DMACHAN,
     netlist        => CFG_SPW_NETLIST,
     spwcore        => 2, -- GRSPW2 is instantiated
     input_type     => CFG_SPW_INPUT,
     output_type    => CFG_SPW_OUTPUT,
     rxtx_sameclk   => CFG_SPW_RTSAME,
     rxunaligned    => CFG_SPW_RXUNAL,
     internalrstgen => 1) -- The wrapper will instantiate internally the reset generators
port map(  rst => rstn, clk => clkm, rxasyncrst => gnd,
           rxsyncrst0 => gnd, rxclk0 => spw_rxclk0,
           rxsyncrst1 => gnd, rxclk1 => spw_rxclk1,
           txsyncrst => gnd, txclk => spw_txclk, txclkn => spw_txclk,
           ahbmi => ahbmi, ahbmo => ahbmo(CFG_NCPU+CFG_AHB_UART+CFG_AHB_JTAG+CFG_GRETH+i),
           apbi => apbi, apbo => apbo(13),
           swni => spwi, swno => spwo);
```

It is important to note that the input resets are tied to GND in the second example, as these signals are internally generated in the wrapper and therefore nor generated neither used in the top level entity.

57.20 Constraints

This section contains example constraints for GRSPW2.

0. Define a clock called 'spw_clk'
1. spw_peri = SpaceWire Maximum clock frequency
2. tech_lib_setup = Setup timing for FlipFlop used in technology
3. tech_lib_hold = Hold timing for FlipFlop used in technology

```
### SpaceWire (LVDS)
set spw_rx_rise_max  [expr $spw_peri / 2 - $tech_lib_setup]
set spw_rx_rise_min  [expr $tech_lib_hold ]
set spw_rx_fall_max  [expr $spw_peri / 2 - $tech_lib_setup]
set spw_rx_fall_min  [expr $tech_lib_hold ]

set spw_tx_max [expr      $tech_lib_setup ]
set spw_tx_min [expr -1 * $tech_lib_hold  ]
```

```
for { set port 0 } { $port < 2 } { incr port } {
   # Inputs
   set_input_delay -max -clock [get_clocks spw_clk]  $spw_rx_rise_max [get_ports
   lvds_rxp[[expr $port + 1]]] -add
   set_input_delay -min -clock [get_clocks spw_clk]  $spw_rx_rise_min [get_ports
   lvds_rxp[[expr $port + 1]]] -add
   set_input_delay -max -clock [get_clocks spw_clk]  $spw_rx_fall_max [get_ports
   lvds_rxp[[expr $port + 1]]] -add -clock_fall
   set_input_delay -min -clock [get_clocks spw_clk]  $spw_rx_fall_min [get_ports
   lvds_rxp[[expr $port + 1]]] -add -clock_fall

   set_input_delay -max -clock [get_clocks spw_clk]  $spw_rx_rise_max [get_ports
   lvds_rxn[[expr $port + 1]]] -add
   set_input_delay -min -clock [get_clocks spw_clk]  $spw_rx_rise_min [get_ports
   lvds_rxn[[expr $port + 1]]] -add
   set_input_delay -max -clock [get_clocks spw_clk]  $spw_rx_fall_max [get_ports
   lvds_rxn[[expr $port + 1]]] -add -clock_fall
   set_input_delay -min -clock [get_clocks spw_clk]  $spw_rx_fall_min [get_ports
   lvds_rxn[[expr $port + 1]]] -add -clock_fall
}

for { set port 0 } { $port < 2 } { incr port } {
   set_output_delay -clock [get_clocks spw_clk] -max $spw_tx_max [get_ports lvds_txp[[expr
   $port + 1]]] -add
   set_output_delay -clock [get_clocks spw_clk] -min $spw_tx_min [get_ports lvds_txp[[expr
   $port + 1]]] -add_delay

   set_output_delay -clock [get_clocks spw_clk] -max $spw_tx_max [get_ports lvds_txn[[expr
   $port + 1]]] -add
   set_output_delay -clock [get_clocks spw_clk] -min $spw_tx_min [get_ports lvds_txn[[expr
   $port + 1]]] -add_delay
}
```

57.21 API

A simple Application Programming Interface (API) is provided together with the GRSPW2. The API is located in $(GRLIB)/software/spw. The files are rmapapi.c, spwapi.c, rmapapi.h, spwapi.h. The spwapi.h file contains the declarations of the functions used for configuring the GRSPW2 and transferring data. The corresponding definitions are located in spwapi.c. The rmapapi is structured in the same manner and contains a function for building RMAP packets.

These functions could be used as a simple starting point for developing drivers for the GRSPW2. The different functions are described in this section.

57.21.1 GRSPW2 Basic API

The basic GRSPW2 API is based on a struct spwvars which stores all the information for a single GRSPW2 core. The information includes its address on the AMBA bus as well as SpaceWire parameters such as node address and clock divisor. A pointer to this struct is used as a input parameter to all the functions. If several cores are used, a separate struct for each core is created and used when the specific core is accessed.

*Table 960.*The spwvars struct

Field	Description	Allowed range
regs	Pointer to the GRSPW2	-
nospill	The nospill value used for the core.	0 - 1
rmap	Indicates whether the core is configured with RMAP. Set by spw_init.	0 - 1
rxunaligned	Indicates whether the core is configured with rxunaligned support. Set by spw_init.	0 - 1
rmapcrc	Indicates whether the core is configured with RMAPCRC support. Set by spw_init.	0 - 1
clkdiv	The clock divisor value used for the core.	0 - 255
nodeaddr	The node address value used for the core.	0 - 255
destkey	The destination key value used for the core.	0 - 255
rxmaxlen	The Receiver maximum length value used for the core.	0 - 33554431
rxpnt	Pointer to the next receiver descriptor.	0 - 127
rxchkpnt	Pointer to the next receiver descriptor that will be polled.	0 - 127
txpnt	Pointer to the next transmitter descriptor.	0 - 63
txchkpnt	Pointer to the next transmitter descriptor that will be polled.	0 - 63
timetxen	The timetxen value used for this core.	0 - 1
timerxen	The timerxen value used for this core.	0 - 1
txd	Pointer to the transmitter descriptor table.	-
rxd	Pointer to the receiver descriptor table	-

The following functions are available in the basic API:

```
int spw_setparam(int nodeaddr, int clkdiv, int destkey, int nospill, int timetxen, int
timerxen, int rxmaxlen, int spwadr, struct spwvars *spw);
```

Used for setting the different parameters in the spwvars struct. Should always be run first after creating a spwvars struct. This function only initializes the struct. Does not write anything to the SpaceWire core.

*Table 961.*Return values for spw_setparam

Value	Description
0	The function completed successfully
1	One or more of the parameters had an illegal value

*Table 962.*Parameters for spw_setparam

Parameter	Description	Allowed range
nodeaddr	Sets the node address value of the struct spw passed to the function.	0-255
clkdiv	Sets the clock divisor value of the struct spw passed to the function.	0-255
destkey	Sets the destination key of the struct spw passed to the function.	0-255
nospill	Sets the nospill value of the struct spw passed to the function.	0 - 1
timetxen	Sets the timetxen value of the struct spw passed to the function.	0 - 1
timerxen	Sets the timerxen value of the struct spw passed to the function.	0 - 1
rxmaxlen	Sets the receiver maximum length field of the struct spw passed to the function.	0 - 2^{25}-1
spwadr	Sets the address to the GRSPW2 core which will be associated with the struct passed to the function.	0 - 2^{32}-1

```
int spw_init(struct spwvars *spw);
```

Initializes the GRSPW2 core located at the address set in the struct spw. Sets the following registers: node address, destination key, clock divisor, receiver maximum length, transmitter descriptor table address, receiver descriptor table address, ctrl and dmactrl. All bits are set to the values found in the spwvars struct. If a register bit is not present in the struct it will be set to zero. The descriptor tables are allocated to an aligned area using malloc. The status register is cleared and lastly the link interface is enabled. The run state frequency will be set according to the value in clkdiv.

*Table 963.*Return values for spw_init

Value	Description
0	The function completed successfully
1	One or more of the parameters could not be set correctly or the link failed to initialize.

*Table 964.*Parameters for spw_init

Parameter	Description	Allowed range
spw	The spwvars struct associated with the GRSPW2 core that should be initialized.	-

```
int set_txdesc(int pnt, struct spwvars *spw);
```

Sets a new address to the transmitter descriptor table address register. Should only be used when no transmission is active. Also resets the pointers for spw_tx and spw_checktx (Explained in the section for those functions).

*Table 965.*Return values for spw_txdesc

Value	Description
0	The function completed successfully
1	The new address could not be written correctly

*Table 966.*Parameters for spw_txdesc

Parameter	Description	Allowed range
pnt	The new address to the descriptor table area	0 - 2^{32}-1
spw	Pointer to the spwvars struct associated with GRSPW2 core that should be configured	-

```
int set_rxdesc(int pnt, struct spwvars *spw);
```

Sets a new address to the Receiver descriptor table address register. Should only be used when no transmission is active. Also resets the pointers for spw_rx and spw_checkrx (Explained in the section for those functions).

*Table 967.*Return values for spw_rxdesc

Value	Description
0	The function completed successfully
1	The new address could not be written correctly

*Table 968.*Parameters for spw_rxdesc

Parameter	Description	Allowed range
pnt	The new address to the descriptor table area	0 - 2^{32}-1
spw	Pointer to the spwvars struct associated with GRSPW2 core that should be configured	-

```
void spw_disable(struct spwvars *spw);
```

Disables the GRSPW2 core (the link disable bit is set to ‘1’).

*Table 969.*Parameters for spw_disable

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW2 core that should be configured	-

```
void spw_enable(struct spwvars *spw);
```

Enables the GRSPW2 core (the link disable bit is set to ‘0’).

*Table 970.*Parameters for spw_enable

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW2 core that should be configured	-

```
void spw_start(struct spwvars *spw);
```

Starts the GRSPW2 core (the link start bit is set to ‘1’).

*Table 971.*Parameters for spw_start

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW2 core that should be configured	-

```
void spw_stop(struct spwvars *spw);
```

Stops the GRSPW2 core (the link start bit is set to ‘0’).

*Table 972.*Parameters for spw_start

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW2 core that should be configured	-

```
int spw_setclockdiv(struct spwvars *spw);
```

Sets the clock divisor register with the clock divisor value stored in the spwvars struct.

*Table 973.*Return values for spw_setclockdiv

Value	Description
0	The function completed successfully
1	The new clock divisor value is illegal.

*Table 974.*Parameters for spw_setclockdiv

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW2 core that should be configured	-

```
int spw_set_nodeadr(struct spwvars *spw);
```

Sets the node address register with the node address value stored in the spwvars struct.

*Table 975.*Return values for spw_set_nodeadr

Value	Description
0	The function completed successfully
1	The new node address value is illegal.

*Table 976.*Parameters for spw_set_nodeadr

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW2 core that should be configured	-

```
int spw_set_rxmaxlength(struct spwvars *spw);
```

Sets the Receiver maximum length register with the rxmaxlen value stored in the spwvars struct.

*Table 977.*Return values for spw_set_rxmaxlength

Value	Description
0	The function completed successfully
1	The new node address value is illegal.

*Table 978.*Parameters for spw_set_rxmaxlength

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW2 core that should be configured	-

```
int spw_tx(int crc, int skipcrcsize, int hsize, char *hbuf, int dsize, char *dbuf, struct
spwvars *spw);
```

Transmits a packet. Separate header and data buffers can be used. If CRC logic is available the GSPW inserts RMAP CRC values after the header and data fields if crc is set to one. This function only sets a descriptor and initiates the transmission. Spw_checktx must be used to check if the packet has been transmitted. A pointer into the descriptor table is stored in the spwvars struct to keep track of the next location to use. It is incremented each time the function returns 0.

*Table 979.*Return values for spw_tx

Value	Description
0	The function completed successfully
1	There are no free transmit descriptors currently available
2	There was illegal parameters passed to the function

*Table 980.*Parameters for spw_tx

Parameter	Description	Allowed range
crc	Set to one to append RMAP CRC after the header and data fields. Only available if hardware CRC is available in the core.	0 - 1
skipcrcsize	The number of bytes in the beginning of a packet that should not be included in the CRC calculation	0 - 15
hsize	The size of the header in bytes	0 - 255
hbuf	Pointer to the header data	-
dsize	The size of the data field in bytes	0 - 2^{24}-1
dbuf	Pointer to the data area.	-
spw	Pointer to the spwvars struct associated with GRSPW2 core that should transmit the packet	-

```
int spw_rx(char *buf, struct spwvars *spw);
```

Enables a descriptor for reception. The packet will be stored to buf. Spw_checkrx must be used to check if a packet has been received. A pointer in the spwvars struct is used to keep track of the next location to use in the descriptor table. It is incremented each time the function returns 0.

*Table 981.*Return values for spw_rx

Value	Description
0	The function completed successfully
1	There are no free receive descriptors currently available

*Table 982.*Parameters for spw_rx

Parameter	Description	Allowed range
buf	Pointer to the data area.	-
spw	Pointer to the spwvars struct associated with GRSPW2 core that should receive the packet	-

```
int spw_checkrx(int *size, struct rxstatus *rxs, struct spwvars *spw);
```

Checks if a packet has been received. When a packet has been received the size in bytes will be stored in the size parameter and status is found in the rxs struct. A pointer in the spwvars struct is used to keep track of the location in the descriptor table to poll. It is incremented each time the function returns nonzero.

*Table 983.*Return values for spw_checkrx

Value	Description
0	No packet has been received
1	A packet has been received

*Table 984.*Parameters for spw_checkrx

Parameter	Description	Allowed range
size	When the function returns 1 this variable holds the number of bytes received	-
rxs	When the function returns 1 this variable holds status information	-
spw	Pointer to the spwvars struct associated with GRSPW2 core that should be polled	-

*Table 985.*The rxstatus struct

Field	Description	Allowed range
truncated	Packet was truncated	0 - 1
dcrcerr	Data CRC error bit was set. Only indicates an error if the packet received was an RMAP packet.	0 - 1
hcrcerr	Header CRC error bit was se.t. Only indicates an error if the packet received was an RMAP packet.	0 - 1
eep	Packet was terminated with EEP	0 - 1

```
int spw_checktx(struct spwvars *spw);
```

Checks if a packet has been transmitted. A pointer is used to keep track of the location in the descriptor table to poll. It is incremented each time the function returns nonzero.

*Table 986.*Return values for spw_checktx

Value	Description
0	No packet has been transmitted
1	A packet has been correctly transmitted
2	A packet has been incorrectly transmitted

*Table 987.*Parameters for spw_checktx

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW2 core that should be polled	-

```
void send_time(struct spwvars *spw);
```

Sends a new time-code. Increments the time-counter in the GRSPW2 and transmits the value.

*Table 988.*Parameters for send time

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW2 core that should be polled	-

```
int check_time(struct spwvars *spw);
```

Check if a new time-code has been received.

*Table 989.*Return values for check_time

Value	Description
0	No time-code has been received
1	A new time-code has been received

*Table 990.*Parameters for check_time

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW2 core that should be polled	-

```
int get_time(struct spwvars *spw);
```

Get the current time counter value.

*Table 991.*Return values for get_time

Value	Description
0 - 63	Returns the current time counter value

*Table 992.*Parameters for get_time

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW2 core that should be polled	-

```
void spw_reset(struct spwvars *spw);
```

Resets the GRSPW2.

*Table 993.*Parameters for spw_reset

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW2 core that should be reset	-

```
void spw_rmapen(struct spwvars *spw);
```

Enables hardware RMAP. Has no effect if the RMAP command handler is not available in GRSPW2.

*Table 994.*Parameters for spw_rmapen

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW2 core that should be set	-

```
void spw_rmapdis(struct spwvars *spw);
```

Disables hardware RMAP. Has no effect if the RMAP command handler is not available in GRSPW2

*Table 995.*Parameters for spw_rmapdis

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW2 core that should be set	-

```
int spw_setdestkey(struct spwvars *spw);
```

Set the destination key of the GRSPW2. Has no effect if the RMAP command handler is not available. The value from the spwvars struct is used.

*Table 996.*Return values for spw_setdestkey

Value	Description
0	The function completed successfully
1	The destination key parameter in the spwvars struct contains an illegal value

*Table 997.*Parameters for spw_setdestkey

Parameter	Description	Allowed range
spw	Pointer to the spwvars struct associated with GRSPW2 core that should be set.	-

57.21.2 GRSPW2 RMAP API

The RMAP API contains only one function which is used for building RMAP headers.

```
int build_rmap_hdr(struct rmap_pkt *pkt, char *hdr, int *size);
```

Builds an RMAP header to the buffer pointed to by hdr. The header data is taken from the rmap_pkt struct.

*Table 998.*Return values for build_rmap_hdr

Value	Description
0	The function completed successfully
1	One or more of the parameters contained illegal values

*Table 999.*Parameters for build_rmap_hdr

Parameter	Description	Allowed range
pkt	Pointer to an rmap_pkt struct which contains the data from which the header should be built	
hdr	Pointer to the buffer where the header will be built	
spw	Pointer to the spwvars struct associated with GRSPW2 core that should be set	-

*Table 1000.*rmap_pkt struct fields

Field	Description	Allowed Range
type	Selects the type of packet to build.	writecmd, readcmd, rmwcmd, writerep, readrep, rmwrep
verify	Selects whether the data should be verified before writing	yes, no
ack	Selects whether an acknowledge should be sent	yes, no
incr	Selects whether the address should be incremented or not	yes, no
destaddr	Sets the destination address	0 - 255
destkey	Sets the destination key	0 - 255
srcaddr	Sets the source address	0 - 255
tid	Sets the transaction identifier field	0 - 65535
addr	Sets the address of the operation to be performed. The extended address field is currently always set to 0.	0 - 2^{32}-1
len	The number of bytes to be writte, read or read-modify-written	0 - 2^{24}-1
status	Sets the status field	0 - 11
dstspalen	Number of source path address bytes to insert before the destination address	0 - 228
dstspa	Pointer to memory holding the destination path address bytes	-
srcspalen	Number of source path address bytes to insert in a command. For a reply these bytes are placed before the return address	0 - 12
srcspa	Pointer to memory holding the source path address bytes	-

58 GRSPW2_GEN - GRSPW2 wrapper with Std_Logic interface

58.1 Overview

The GRSPW2_GEN wrapper provides an interface to the GRSPW2 core only using Std_Logic signals instead of GRLIB records. The GRLIB AMBA plug and play extensions have also been removed. This document describes the signal interface and how they map to the signal names in GRLIB. For a user manual on the core function please refer to the GRSPW2 section. An example instantiation of the core can be found at the end of this document.

58.2 Signal descriptions

Table 955 shows the interface signals of the core (VHDL ports).

Table 1001. Signal descriptions

Signal name	Type	Function	Active	GRLIB signal name
RST	Input	Reset	Low	RST
CLK	Input	System (AMBA) Clock.	-	CLK
RXASYNCRST	Input	Receiver asynchronous reset for both ports 0 and 1	Low	RXASYNCRST
RXSYNCRST0	Input	Receiver synchronous reset for port 0	Low	RXSYNCRST0
RXCLK0	Input	Receiver clock for port 0.	-	RXCLK0
RXSYNCRST1	Input	Receiver synchronous reset for port 1	Low	RXSYNCRST1
RXCLK1	Input	Receiver clock for port 1. Unused if the VHDL generic ports is 2.	-	RXCLK1
TXSYNCRST	Input	Transmitter synchronous reset	Low	TXSYNCRST
TXCLK	Input	Transmitter clock	-	TXCLK
TXCLKN	Input	Transmitter inverted clock. Only used in DDR transmitter mode for technologies not supporting local generation of inverted clock.	-	TXCLKN
HGRANT	Input	See AMBA manual.	-	AHBMI.HGRANT
HREADY	Input	See AMBA manual.	-	AHBMI.HREADY
HRESP[1:0]	Input	See AMBA manual.	-	AHBMI.HRESP
HRDATA[31:0]	Input	See AMBA manual.	-	AHBMI.HRDATA
HBUSREQ	Output	See AMBA manual.	-	AHBMO.HBUSREQ
HLOCK	Output	See AMBA manual.	-	AHBMO.HLOCK
HTRANS[1:0]	Output	See AMBA manual.	-	AHBMO.HTRANS
HADDR[31:0]	Output	See AMBA manual.	-	AHBMO.HADDR
HWRITE	Output	See AMBA manual.	-	AHBMO.HWRITE
HSIZE[2:0]	Output	See AMBA manual.	-	AHBMO.HSIZE
HBURST[2:0]	Output	See AMBA manual.	-	AHBMO.HBURST
HPROT[3:0]	Output	See AMBA manual.	-	AHBMO.HPROT
HWDATA[31:0]	Output	See AMBA manual.	-	AHBMO.HWDATA

Table 1001. Signal descriptions

Signal name	Type	Function	Active	GRLIB signal name
PSEL	Input	See AMBA manual.	-	APBI.PSEL
PENABLE	Input	See AMBA manual.	-	APBI.PENABLE
PADDR[31:0]	Input	See AMBA manual.	-	APBI.PADDR
PWRITE	Input	See AMBA manual.	-	APBI.PWRITE
PWDATA[31:0]	Input	See AMBA manual.	-	APBI.PWDATA
PRDATA[31:0]	Output	See AMBA manual.	-	APBO.PRDATA
D[3:0]	Input	SpaceWire Data input	-	SWNI.D
DV[3:0]	Input	SpaceWire Data valid.	High	SWNI.DV
DCONNECT[3:0]	Input	SpaceWire Disconnect.	-	SWNI.DCONNECT
DCONNECT2[3:0]	Input	SpaceWire Disconnect. Copy of DCONNECT (triplication of the asynchronous resets logic)	-	SWNI.DCONNECT2
DCONNECT3[3:0]	Input	SpaceWire Disconnect. Copy of DCONNECT (triplication of the asynchronous resets logic)	-	SWNI.DCONNECT3
DO[3:0]	Output	SpaceWire Data output.	-	SWNO.D
SO[3:0]	Output	SpaceWire Strobe output.	-	SWNO.S
TICKIN	Input	Time counter tick input. Increments internal time-counter and transmits the new value.	High	SWNI.TICKIN
TICKINRAW	Input	Raw tick input. Send time-code from timein input.	High	SWNI.TICKINRAW
TIMEIN[7:0]	Input	Raw tick input. Send time-code from timein input.	-	SWNI.TIMEIN
TICKINDONE	Output	Asserted when a time-code has been accepted for transmission when tickinraw is asserted. Tickinraw must be deasserted the same clock cycle as tickindone is asserted.	High	SWNO.TICKINDONE
TICKOUT	Output	Time counter tick output. Asserted when a valid time-code has been received	High	SWNO.TICKOUT
TICKOUTRAW	Output	Tick out which is always set when a time-code is received.	High	SWNO.TICKOUTRAW
TIMEOUT[7:0]	Output	Contains the received time-code when tick-inraw is asserted.	-	SWNO.TIMEOUT
IRQ	Output	Common interrupt line for the core. Asserted one clock cycle for each interrupt.	High	N/A
CLKDIV10[7:0]	Input	Clock divisor value used during initialization and as reset value for the clock divisor register	-	SWNI.CLKDIV10
LINKDIS	Output	Asserted when the link is disabled	High	SWNO.LINKDIS
TESTRST	Output	Scan test reset	Low	-
TESTEN	Input	Scan test enable	High	-
RMAPEN	Input	Reset value for the rmapen control register bit	High	SWNI.RMAPEN
RXDAV	Output	Asserted each cycle a character has been receved on the SpaceWire link.	High	SWNO.RXDAV
RXDATAOUT[8:0]	Output	Contains the received character when rxdav is asserted	-	SWNO.RXDATAOUT

Table 1001. Signal descriptions

Signal name	Type	Function	Active	GRLIB signal name
CTRLREGRST	Output	Register reset. It corresponds to the bit 6 of the Control Register (see 57.12.1. Control Register). It shall be used negated (it is active high) to generate the AMBA and transmitter resets.	High	SWNO.CTRLREGRST
RXRST	Output	Internal reset generated by the transmitter for synchronization purpose between transmitter and both receiver channels. It shall be used to generate the asynchronous and synchronous receiver resets.	Low	SWNO.RXRST

58.3 Instantiation

This example shows how the core can be instantiated. The reset generators have been instantiated according to the implementation section in GRSPW2 (refer to 57.11.1. Reset for further information).

Normally di, si, do and so should be connected to input and output pads configured with LVDS drivers. How this is done is technology dependent. Instead the single ended inputs and outputs are connected directly to the external interface. The example uses only one port and the output is in SDR mode which means parts of the SpaceWire input and output vectors are unused.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.spacewire.all;

entity spacewire_ex is
  port (
    clk           : in  std_ulogic;
    rstn          : in  std_ulogic;
    txclk         : in  std_ulogic;
    --ahb mst in
    hgrant        : in  std_ulogic;
    hready        : in  std_ulogic;
    hresp         : in  std_logic_vector(1 downto 0);
    hrdata        : in  std_logic_vector(31 downto 0);
    --ahb mst out
    hbusreq       : out  std_ulogic;
    hlock         : out  std_ulogic;
    htrans        : out  std_logic_vector(1 downto 0);
    haddr         : out  std_logic_vector(31 downto 0);
    hwrite        : out  std_ulogic;
    hsize         : out  std_logic_vector(2 downto 0);
    hburst        : out  std_logic_vector(2 downto 0);
    hprot         : out  std_logic_vector(3 downto 0);
    hwdata        : out  std_logic_vector(31 downto 0);
    --apb slv in
    psel  : in   std_ulogic;
    penable  : in   std_ulogic;
    paddr  : in   std_logic_vector(31 downto 0);
    pwrite  : in   std_ulogic;
    pwdata  : in   std_logic_vector(31 downto 0);
    --apb slv out
    prdata  : out  std_logic_vector(31 downto 0);
    --spw in
    di            : in   std_ulogic;
    si            : in   std_ulogic;
    --spw out
    do            : out  std_ulogic;
```

```
    so            : out  std_ulogic;
    --time iface
    tickin        : in   std_ulogic;
    tickout       : out  std_ulogic;
    --misc
    irq           : out  std_logic;
    clkdiv10      : in   std_logic_vector(7 downto 0);
    rmapen        : in   std_ulogic;
    );
end;

architecture rtl of spacewire_ex is
  signal rxclko    : std_ulogic;
  signal d         : std_logic_vector(3 downto 0);
  signal do_int    : std_logic_vector(3 downto 0);
  signal so_int    : std_logic_vector(3 downto 0);
  signal dv        : std_logic_vector(3 downto 0);
  signal dconnect  : std_logic_vector(3 downto 0);
  signal dconnect2 : std_logic_vector(3 downto 0);
  signal dconnect3 : std_logic_vector(3 downto 0);
  signal timein    : std_logic_vector(7 downto 0);
  signal tickinraw : std_ulogic;
  signal testen    : std_ulogic;
  signal testrst   : std_ulogic;

  -- Internal resets
  signal tmp_reset : std_ulogic;
  signal mrst      : std_ulogic;
  signal rxasyncrst: std_ulogic;
  signal rxsyncrst0: std_ulogic;
  signal rxsyncrst1: std_ulogic;
  signal txsyncrst : std_ulogic;

begin

  do <= do_int(0);
  so <= so_int(0);
  tickinraw <= '0';
  testrst <= '0';
  testen  <= '0';

  spw_phy0 : grspw2_phy
    generic map(
      scantest   => 0,
      tech       => 0,
      input_type => 3)
    port map(
      rstn       => rstn,
      rxclki     => rxclk0,
      rxclkin    => rxclk0,
      nrxclki    => rxclk0,
      di         => di,
      si         => si,
      do         => d(1 downto 0),
      dov        => dv(1 downto 0),
      dconnect   => dconnect(1 downto 0),
      dconnect2  => dconnect2(1 downto 0),
      dconnect3  => dconnect3(1 downto 0),
      rxclko     => rxclko);

  -- Internal reset generators (TX, RX0 and RX1 clock domains)

  -- The AMBA and TX resets take into account the bit 6 of the Control
  -- Register (software reset)
  tmp_reset <= rstn and not ctrlregrst;

  -- CLK domain (synchronous reset)
  AMBA_rst : rstgen
  port map (tmp_reset, clk, vcc, mrst, open);

  -- TX domain (synchronous reset)
```

```
txrst : rstgen
port map (tmp_reset, spw_rxtxclk, vcc, txsyncrst, open);

-- RX domain (asynchronous reset)
rxasyncrst <= rxrst;

-- RX domain (synchronous reset)
rxsyncrst0 : rstgen
port map (rxrst, rxclk0, vcc, rxsyncrst0, open);

rxsyncrst1 : rstgen
port map (rxrst, rxclk1, vcc, rxsyncrst1, open);

sw0 : grspw2_gen
generic map(
  tech         => 0,
  ports        => 1,
  dmachan      => 1,
  rmap         => 0,
  rmapcrc      => 1,
  fifosize1    => 32,
  fifosize2    => 32,
  rxunaligned  => 1,
  rmapbufs     => 4,
  output_type  => 1,
  input_type   => 3,
  rxtx_sameclk => 1)
port map(
  rst          => mrst,
  clk          => clk,
  rxasyncrst   => rxasyncrst,
  rxsyncrst0   => rxsyncrst0,
  rxclk0       => rxclk0,
  rxsyncrst1   => rxsyncrst1,
  rxclk1       => rxclk1,
  txsyncrst    => txsyncrst,
  txclk        => txclk,
  txclkn       => txclkn,
  --ahb mst in
  hgrant       => hgrant,
  hready       => hready,
  hresp        => hresp,
  hrdata       => hrdata,
  --ahb mst out
  hbusreq      => hbusreq,
  hlock        => hlock,
  htrans       => htrans,
  haddr        => haddr,
  hwrite       => hwrite,
  hsize        => hsize,
  hburst       => hburst,
  hprot        => hprot,
  hwdata       => hwdata,
  --apb slv in
  psel => psel,
  penable => penable,
  paddr => paddr,
  pwrite => pwrite,
  pwdata => pwdata,
  --apb slv out
  prdata => prdata,
  --spw in
  d            => d,
  dv           => dv,
  dconnect     => dconnect,
  dconnect2    => dconnect2,
  dconnect3    => dconnect3,
  --spw out
  do           => do_int,
  so           => so_int,
  --time iface
```

```
tickin       => tickin,
tickinraw    => tickinraw,
timein       => timein,
tickindone   => open,
tickout      => tickout,
tickoutraw   => open,
timeout      => open,
--irq
irq          => irq,
--misc
clkdiv10     => clkdiv10,
linkdis      => open,
testrst      => testrst,
testen       => testen,
--rmapen
rmapen       => rmapen,
--parallel rx data out
rxdav        => open,
rxdataout    => open,
-- Reset interconnection
ctrlregrst   => ctrlregrst,
rxrst        => rxrst);
```

59 GRSPW2_PHY - GRSPW2 Receiver Physical Interface

59.1 Overview

The GRSPW2_PHY provides a common interface for the receiver modules in GRSPW2, GRSPWROUTER, and GRSPW_CODEC to the actual data recovery circuit. The data can be recovered in four different ways: Self-clocking (xor on data and strobe), Single Data Rate (SDR) sampling, Double Data Rate (DDR) sampling and from an SpaceWire transceiver. The GRSPW2_PHY presents the data with a data, and a data-valid signal, as well as outputs the clock used by the receiver modules. One GRSPW2_PHY core is needed for each SpaceWire link (data and strobe pair).

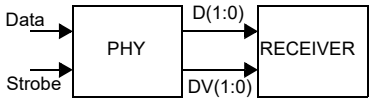


Figure 159. Data connection between the GRSPW2_PHY and the GRSPW2 / GRSPWROUTER / GRSPW_CODEC receiver.

59.2 Operation

As mentioned above the core supports four different input schemes, configurable through the VHDL generic input_type. The GRSPW2, GRSPWROUTER and GRSPW_CODEC cores also each have a generic named input_type, and it is important that it is set to the same value as for GRSPW2_PHY. The four different input schemes are explained in more detail in the following subsections.

59.2.1 Self-clocking (input_type = 0)

In self-clocking mode the receiver clock is recovered from the SpaceWire data and strobe by using an xor gate. The recovered clock is then used to clock the registers to which the data is stored. The recovered clock is coupled to the GRSPW2_PHY output signal RXCLKO, which should be connected to the receiver clock input of GRSPW2 / GRSPWROUTER / GRSPW_CODEC.

Since data will appear on both the rising and falling edge of the recovered clock there must be two registers, one for each edge. Figure 160 shows the clock recovery scheme. As can be seen in the figure, the SpaceWire data input is used for generating the reciver clock as well as input of several flip-flops. Care must be taken so that the delay from the data and strobe signals through the clock network is longer than the delay to the flip-flop's data input + setup time.

For self-clocking mode, the core's RXCLKI and RXCLKIN inputs are unused. The NRXCLKI input is unused if scan test support is not implemented (scantest generic set to 0). If scan test mode is implemented (scantest generic set to 1) then the NRXCLKI input is used as the receiver clock during scan test (TESTEN input high), otherwise it is not used. Details on how to connect the other input / output signals are found in section 59.5.

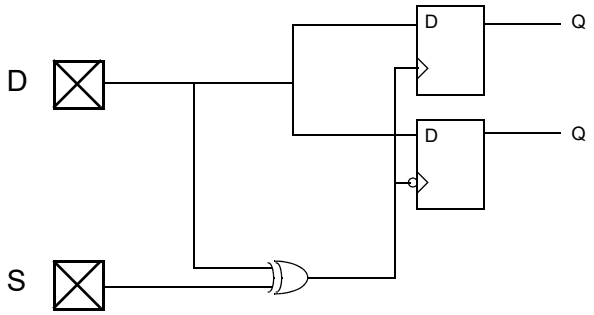


Figure 160. The clocking scheme for self clocking mode. The clock is recovered from the SpaceWire data and strobe signals using an xor gate.

59.2.2 Cobham transceiver (input_type = 1)

When using the Cobham transceiver the RxClk output from the transceiver shall be connected to the RXCLKI input of GRSPW2_PHY. RxDR and RxDF should be connected to DI and SI respectively. The GRSPW2_PHY outputs DO, DOV and DCONNECT are generated in the same way as for the self-clocking mode.

RXCLKIN is unused in this configuration. NRXCLKI is unused if scan test support is not implemented (SCANTEST generic set to 0). If scan test support is implemented (SCANTEST generic set to 1) the NRXCLKI is used in the following way: When not in scan test mode (TESTEN input is low) the NRXCLKI input should be the inverse of the RXCLKI input, and when in scan test mode (TESTEN input is high) the NRXCLKI input should be the same clock as the RXCLKI input. Details on how to connect the other input / output signals is found in section 59.5.

59.2.3 SDR sampling (input_type = 2)

In this mode the sampling clock should be connected to the RXCLKI input. RXCLKIN and NRXCKLI are unused in this mode. Details on how to connect the other input / output signals is found in section 59.5.

The core internally detects new data on the data line. Since only one bit can be detected each clock cycle only bit 0 of the data signal to the receiver (DO output) is used. Normally the sampling frequency has to be at least 1,5 higher than the maximum bitrate for correct operation.

59.2.4 DDR sampling (input_type = 3)

The sampling clock should be connected to RXCLKI. If the selected technology does not have DDR primitives that automatically generate the inverted clock then the inverted sampling clock has to be connected to RXCLKIN. NRXCLKI is unused in this mode. Details on how to connect the other input / output signals is found in section 59.5.

The core internally detects new data on the data line. There can be two bits detected each clock cycle so both data signals to the receive (DO output) have to be used. The sampling frequency times two has to be at least 1,5 times the maximum bitrate.

59.2.5 DDR sampling with internal pad (input_type = 4)

Same as DDR sampling (input_type = 3) except that both DDR registers and input pads are instantiated within the GRSPW2_PHY. This option can be used on technologies where DDR registers and pads must be instantiated as one entity. This option (input_type = 4) should not be used unless recommended by Cobham Gaisler. If input_type = 4 is selected then the level and voltage of the instantiated pads are specified via the VHDL generics input_level and input_voltage, and external pads should not be instantiated for the SpaceWire input signals.

59.2.6 Self-clocking with external clock recovery (input_type = 5)

Same as self-clocking (input_type = 0) except that the clock recovery is done externally to the GRSPW2_PHY. The rxclki input is used to clock the receiver registers within the core.

The core's RXCLKIN input is unused. The NRXCLKI input is unused if scan test support is not implemented (scantest generic set to 0). If scan test mode is implemented (scantest generic set to 1) then the NRXCLKI input is used as the receiver clock during scan test (TESTEN input high), otherwise it is not used.

59.2.7 Self-clocking with external clock recovery and DDR register (input_type = 6)

Same as self-clocking with external clock recovery (input_type = 5) except that a DDR register is used internally in GRSPW2_PHY for the incoming data.

59.3 Configuration options

Table 1002 shows the configuration options of the core (VHDL generics).

*Table 1002.*Configuration options

Generic	Function	Allowed range	Default
scantest	Enable scantest mode	0 - 1	0
tech	Selects technology for DDR registers when input_type = 3, 4 or 6, as well as technology for clock buffer when input_type = 0, 5, 6 and rxclkbuftype /= 0.	0 - NTECH	1
input_type	Selects receiver type. 0 = Self clocking (xor), 1 = Interface for SpaceWire transceiver, 2 = Single data rate sampling, 3 and 4 = Double data rate sampling, 5 = Self-clocking with external recovery, 6 = Self-clocking with external recovery and DDR register for data. This generic must be set to the same value as the GRSPW2 / GRSPWROUTER / GRSPW_CODEC generic with the same name.	0 - 4	0
input_level	Selects level for pads instantiated within PHY. Only used when input_type = 4.	-	0
inpput_voltage	Selects voltage for pads insantiated within PHY. Only used when input_type = 4.	-	0
rxclkbuftype	Selects clock buffer type for receiver clock. 0 = No clock buffer (synthesis tools may still infer a buffer). 1 = Hard-wired clock, 2 = Routed clock.	0 - 2	0
rstsrctmr	Enables the Triple Module Redundancy for the asynchronous reset nets of the core	0 - 1	0

59.4 Scan support

Scan support is enabled by setting the SCANTEST generic to 1. When enabled, the asynchronous reset of any flip-flop will be connected to TESTRT when TESTEN = ‘1’.

59.5 Signal descriptions

Table 1003 shows the interface signals of the model (VHDL ports).

*Table 1003.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	-	Input	Reset	Low
RXCLKI	-	Input	Receiver clock input. See sections 59.2.1 through 59.2.1 for details on how this signal is used for respective input type.	-
RXCLKIN	-	Input	The inverse of RXCLKI should be inputed here. See sections 59.2.1 through 59.2.1 for details on how this signal is used for respective input type.	-
NRXCLKI	-	Input	The inverse of RXCLKI should be inputed here. See sections 59.2.1 through 59.2.1 for details on how this signal is used for respective input type.	-
DI	-	Input	SpaceWire data input. When using a transceiver (input_type = 1), the transceiver's RxDR output should be connected to this input.	-
SI	-	Input	SpaceWire strobe input. When using a transceiver (input_type = 1), the transceiver's RxDF output should be connected to this input.	-
DO(1:0)	-	Output	Recovered data. Synchronous to RXCLKO. Should be connected to data inputs on GRSPW2 / GRSPWROUTER / GRSPW_CODEC.	-
DOV(1:0)	-	Output	Data valid. Synchronous to RXCLKO. Should be connected to data valid inputs on GRSPW2 / GRSPWROUTER / GRSPW_CODEC.	High
DCONNECT(1:0)	-	Output	Disconnect strobe signals. Synchronous to RXCLKO. Should be connected to the disconnect inputs on GRSPW2 / GRSPWROUTER / GRSPW_CODEC.	-
DCONNECT2 (1:0)	-	Output	If the generic rstsrctmr is set to 1 (TMR enabled), it is a replication of DCONNECT. It should be connected to the disconnect inputs on GRSPW2 / GRSPW_CODEC. If the generic rstsrctmr is set to 0 (TMR disabled), this signal is set to low and has no use.	-
DCONNECT3 (1:0)	-	Output	If the generic rstsrctmr is set to 1 (TMR enabled), it is a replication of DCONNECT. It should be connected to the disconnect inputs on GRSPW2 / GRSPW_CODEC. If the generic rstsrctmr is set to 0 (TMR disabled), this signal is set to low and has no use.	-
RXCLKO	-	Output	Receiver clock output. Should be connected to receiver clock inputs on GRSPW2 / GRSPWROUTER / GRSPW_CODEC.	-
TESTRST	-	Input	Scan test reset.	Low
TESTEN	-	Input	Scan test enable.	High

59.6 Library dependencies

Table 1004 shows the libraries used when instantiating the model (VHDL libraries).

*Table 1004.*Library dependencies

Library	Package	Imported unit(s)	Description
GAISLER	SPACEWIRE	component	Component declaration.

59.7 Instantiation

This example shows how the core can be instantiated in DDR mode (input_type = 3). rxclkin is used if the technology cannot generate the inverted clock in the DDR register otherwise it can be left floating. nrxclki is not needed at all for this mode and spw_rxtxclk is only connected not to violate VHDL syntax. Only one port is used so the same clock is coupled to both receiver clock inputs.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.spacewire.all;

entity spacewire_ex is
  port (
    clk   : in  std_ulogic;
    rstn          : in  std_ulogic;

    -- spacewire signals
    spw_rxdp      : in  std_ulogic;
    spw_rxdn      : in  std_ulogic;
    spw_rxsp      : in  std_ulogic;
    spw_rxsn      : in  std_ulogic;
    spw_txdp      : out std_ulogic;
    spw_txdn      : out std_ulogic;
    spw_txsp      : out std_ulogic;
    spw_txsn      : out std_ulogic;

    spw_rxtxclk   : in  std_ulogic;
    spw_rxclkn    : in  std_ulogic
    );
end;

architecture rtl of spacewire_ex is

  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);

  -- Spacewire signals
  signal swni      : grspw_in_type;
  signal swno      : grspw_out_type;
  signal spw_rxclk : std_logic_vector(1 downto 0);
  signal dtmp    : std_ulogic;
  signal stmp      : std_ulogic;
  signal rxclko    : std_ulogic;
begin

  -- AMBA Components are instantiated here

  spw_phy0 : grspw2_phy
    generic map(
      scantest   => 0,
```

```
    tech       => memtech,
    input_type => 3)
  port map(
    rstn       => rstn,
    rxclki     => spw_rxtxclk,
    rxclkin    => spw_rxclkn,
    nrxclki    => spw_rxtxclk,
    di         => dtmp,
    si         => stmp,
    do         => swni.d(1 downto 0),
    dov        => swni.dov(1 downto 0),
    dconnect   => swni.dconnect(1 downto 0),
    dconnect2  => swni.dconnect2(1 downto 0),
    dconnect3  => swni.dconnect3(1 downto 0),
    rxclko     => rxclko);

sw0 : grspw2
generic map(
  tech         => memtech,
  hindex       => 0,
  pindex       => 10,
  paddr        => 10,
  pirq         => 10,
  ports        => 1,
  dmachan      => 1,
  rmap         => 0,
  rmapcrc      => 1,
  fifosize1    => 32,
  fifosize2    => 32,
  rxunaligned  => 1,
  rmapbufs     => 4,
  output_type  => 1,
  input_type   => 3,
  rxtx_sameclk => 1)
port map(rstn, clkm, rxclko, rxclko, spw_rxtxclk, spw_rxtxclk, ahbmi,
     ahbmo(0), apbi, apbo(10), swni, swno);

swni.tickin <= '0'; swni.rmapen <= '1';
swni.clkdiv10 <= conv_std_logic_vector(SPW_TX_FREQ_KHZ/10000-1, 8);

spw_rxd_pad : inpad_ds generic map (padtech, lvds, x25v)
  port map (spw_rxdp, spw_rxdn, dtmp);
spw_rxs_pad : inpad_ds generic map (padtech, lvds, x25v)
  port map (spw_rxsp, spw_rxsn, stmp);
spw_txd_pad : outpad_ds generic map (padtech, lvds, x25v)
  port map (spw_txdp, spw_txdn, swno.d(0), gnd(0));
spw_txs_pad : outpad_ds generic map (padtech, lvds, x25v)
  port map (spw_txsp, spw_txsn, swno.s(0), gnd(0));
...
```

60 GRSPW_CODEC - SpaceWire encoder-decoder

60.1 Overview

The SpaceWire encoder-decoder implements an encoder-decoder compliant to the SpaceWire standard (ECSS-E-50-12C). It provides a generic host-interface consisting of control signals, status signals, time-code interface and 9-bit wide data buses connecting to a pair of FIFOs.

The core can also be configured with two SpaceWire ports with manual or automatic switching between them.

Transmitter outputs can be either Single Data Rate (SDR), Double Data Rate (DDR) or connected to an SpaceWire transceiver. The receiver can be connected either to an SpaceWire transceiver or recover the data itself using a self-clocking scheme or sampling (SDR or DDR).

The core is practically identical to the encoder-decoder used in the GRSPW2, the only difference being the host-interface.

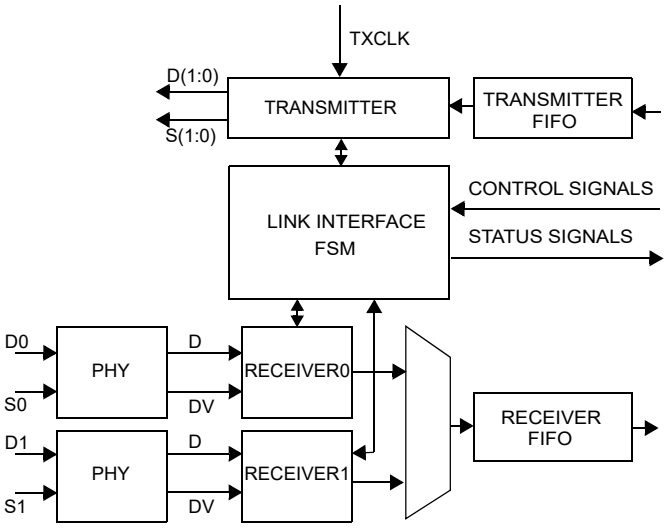


Figure 161. Block diagram

60.2 Operation

60.2.1 Overview

A block diagram of the internal structure of the core can be found in figure 161. It consists of the receiver, transmitter and the link interface FSM. They handle communication on the SpaceWire network. The PHY blocks provides a common interface for the receiver to the four different data recovery schemes and is external to this core. A short description is found in section 60.2.6. The complete documentation is found in the GRSPW2_PHY section of the GRIP user manual.

Time-codes are transmitted through a signal interface as specified in the SpaceWire standard.

60.2.2 Link-interface FSM

The link-interface FSM controls the link interface (a more detailed description is found in the SpaceWire standard). The low-level protocol handling (the signal and character level of the SpaceWire standard) is handled by the transmitter and receiver while the FSM handles the exchange level.

The link-interface FSM is controlled through the control signals. The link can be disabled through the link disabled signal, which depending on the current state, either prevents the link-interface from reaching the started state or forces it to the error-reset state. When the link is not disabled, the link

interface FSM is allowed to enter the started state when either the link start signal is asserted or when a NULL character has been received and the autostart signal is asserted.

The current state of the link-interface determines which type of characters are allowed to be transmitted which together with the requests made from the host interface determine what character will be sent.

Time-codes are sent when the FSM is in the run-state and a request is made through the time-interface (described in section 60.2.8).

When the link-interface is in the connecting- or run-state it is allowed to send FCTs. FCTs are sent automatically by the link-interface when possible. This is done based on the maximum value of 56 for the outstanding credit counter and the currently free space in the receiver FIFO. FCTs are sent as long as the outstanding counter is less than or equal to 48 and there are at least 8 more empty FIFO entries than the counter value.

N-Chars are sent in the run-state when they are available from the transmitter FIFO and there are credits available. NULLs are sent when no other character transmission is requested or the FSM is in a state where no other transmissions are allowed.

The credit counter (incoming credits) is automatically increased when FCTs are received and decreased when N-Chars are transmitted. Received N-Chars are stored to the receiver N-Char FIFO while received Time-codes are handled by the time-interface.

60.2.3 Transmitter

The state of the FSM, credit counters, requests from the time-interface and requests from the transmitter FIFO are used to decide the next character to be transmitted. The type of character and the character itself (for N-Chars and Time-codes) to be transmitted are presented to the low-level transmitter which is located in a separate clock-domain.

This is done because the SpaceWire link is usually run on a different frequency than the host system clock. The core has a separate clock input which is used to generate the transmitter clock. More information on transmitter clock generation is found in section 60.5.2. Since the transmitter often runs on high frequency clocks (> 100 MHz) as much logic as possible has been placed in the system clock domain to minimize power consumption and timing issues.

The transmitter logic in the host clock domain decides what character to send next and sets the proper control signal and presents any needed character to the low-level transmitter as shown in figure 162. The transmitter sends the requested characters and generates parity and control bits as needed. If no requests are made from the host domain, NULLs are sent as long as the transmitter is enabled. Most of the signal and character levels of the SpaceWire standard is handled in the transmitter. External LVDS drivers are needed for the data and strobe signals. The outputs can be configured as either single- or double data rate. The latter increases maximum bitrate significantly but is not available for all technologies.

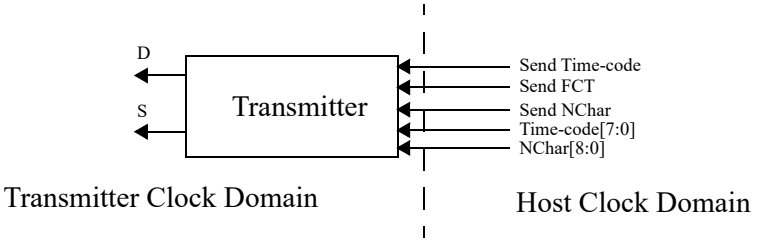


Figure 162. Schematic of the link interface transmitter.

60.2.4 Receiver

The receiver detects connections from other nodes and receives characters as a bit stream recovered from the data and strobe signals by the GRSPW2_PHY module which presents it as a data and data-valid signal. Both the receiver and GRSPW2_PHY are located in a separate clock domain which runs on a clock outputed by the PHY. More information on the clock-generation can be found in section 60.5.2.

The receiver is activated as soon as the link-interface leaves the error reset state. Then after a NULL is received it can start receiving any characters. It detects parity, escape and credit errors which causes the link interface to enter the error-reset state. Disconnections are handled in the link-interface part in the tx clock domain because no receiver clock is available when disconnected.

Received characters are flagged to the host domain and the data is presented in parallel form. The interface to the host domain is shown in figure 163. L-Chars are the handled automatically by the host domain link-interface part while all N-Chars are stored in the receiver FIFO for further handling. If two or more consecutive EOPs/EEPs are received all but the first are discarded.

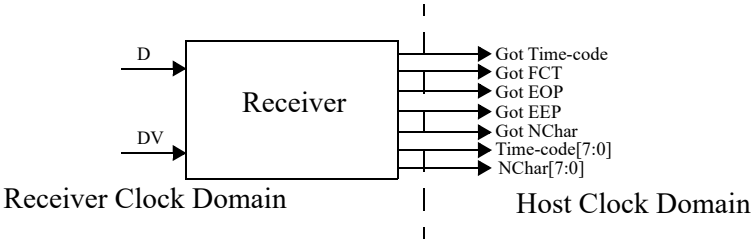


Figure 163. Schematic of the link interface receiver.

60.2.5 Dual port support

The core can be configured to include an additional SpaceWire port. With dual ports the transmitter drives an additional pair of data/strobe output signals and one extra receiver is added to handle a second pair of data/strobe input signals.

One of the ports is set as active (how the active port is selected is explained below) and the transmitter drives the data/strobe signals of the active port with the actual output values as explained in section 60.2.3. The inactive port is driven with zero on both data and strobe.

Both receivers will always be active but only the active port's interface signals (see figure 163) will be propagated to the link interface FSM. Each time the active port is changed, the link will be reset so that the new link is started in a controlled manner.

When the noportforce signal is zero, the portsel signal selects the active port. When the noportforce signal is set to one, the active port is automatically selected during initialization. For the latter mode, the port on which the first bit is received will be selected as the active port. If the initialization attempt fails on that port the link is reset and the active port is again sected based on which port the first bit is received.

60.2.6 Receiver PHY

The receiver supports four different input data recovery schemes: self-clocking (xor), sampling SDR, sampling DDR and the SpaceWire transceiver. These four recovery types are handled in the PHY module and data is presented to the receiver as a data and data-valid signal. This part of the receiver must often be constrained and placing it in a separate module makes this process easier with the most common synthesis tools. The input type is selected using a VHDL generic. More information about the PHY can be found in the GRSPW2_PHY section of the GRIP user manual.

60.2.7 Setting link-rate

The input signal IDIVISOR determines the link-rate during initialization (all states up to and including the connecting-state). The value of this input signal is also used to calculate the link interface FSM timeouts (6.4 us and 12.8 us, as defined in the SpaceWire standard). The IDIVISOR signal should always be set so that a 10 Mbit/s link-rate is achieved during initialization. In that case the timeout values will also be calculated correctly.

To achieve a 10 Mbit/s link-rate, the IDIVISOR signal should be set according to the following formulas:

With single data rate (SDR) outputs:

IDIVISOR = (<frequency in MHz of TXCLK> / 10) - 1

With double data rate (DDR) outputs, or when connected to Cobham SpaceWire transceiver:

IDIVISOR = (2 x <frequency in MHz of TXCLK> / 10) - 1

The link-rate in run-state is controlled with the run-state divisor, the RDIVISOR input signal. The link-rate in run-state is calculated according to the following formulas:

With SDR outputs:

<link-rate in Mbits/s> = <frequency in MHz of TXCLK> / (RDIVISOR+1)

With DDR outputs / Cobham SpaceWire transceiver:

<link-rate in Mbits/s> = 2 x <frequency in MHz of TXCLK> / (RDIVISOR+1)

The value of RDIVISOR only affects the link-rate in run-state, and does not affect the 6.4 us or 12.8 us timeouts values.

Note that when using DDR ouputs, or when connected to Cobham SpaceWire transceiver, there is a limitation in the usable clock divisor values. All even values (except 0) will result in the same bitrate as the one higher odd number.

An example of clock divisor and resulting link-rate, with a TXCLK frequency of 50 MHz, is shown in the table 1005. Also see 60.5.2 for information on clock requirements.

*Table 1005.*SpaceWire link-rate example with 50 MHz TXCLK

	Link-rate in Mbit/s	
Clock divisor value	**SDR outputs**	**DDR outputs / Cobham SpaceWire transceiver**
0	50	100
1	25	50
2	16.67	25
3	12.5	25
4	10	16.67
5	8.33	16.67
6	7.14	12.5
7	6.25	12.5
8	5.56	10
9	5	10

60.2.8 Time interface

The time interface is used for sending Time-codes over the SpaceWire network and consists of a timein signal, timectrlin signal, tickin signal, timeout signal, timectrlout signal and a tickout signal.

Each Time-code sent from the core is a concatenation of the timectrlin and the timein signal. It is transmitted each time tickin is kept asserted until the tickin_done output is asserted. Time-codes are only transmitted when the link-interface FSM is in run-state and when the previous character transmission is finished. This can cause a delay between when the assertion of tickin_done after tickin has been asserted. If tickin is not kept asserted until tickin_done is asserted the time-code will not be transmitted. Figure 164 shows an example of how a time-code is transmitted.

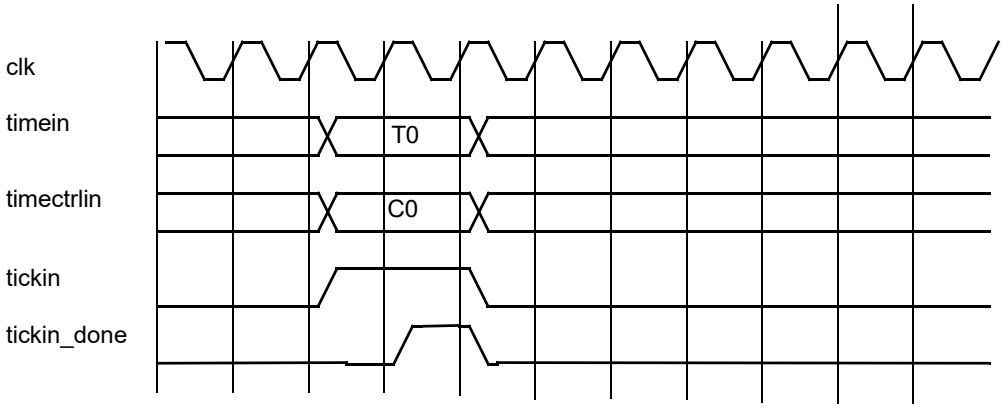


Figure 164. Transmitting a time-code using tickin, timein and timectrlin.

Received Time-codes are presented on the timectrlout and timectrl signals. They are valid when the tickout output is asserted. A tickout is generated each time a valid time-code is received. When the tickout is generated the tick-out signal will be asserted one clock-cycle. Figure 165 shows how time-codes are received.

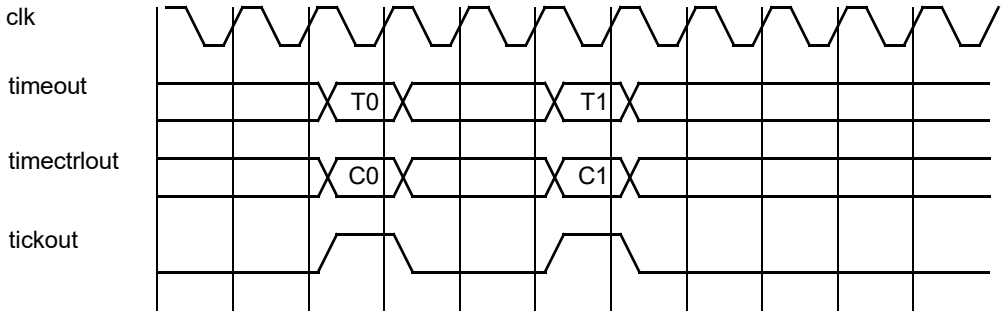


Figure 165. Receiving time-codes using tickout, timeout and timectrlout.

60.3 Receiver interface

The receiver interface consists of the following signals connected to the receiver FIFO: rxicharav, rxicharcnt, rxichar, rxiread. Rxicharav is asserted when there are one or more characters available in the receiver FIFO while rxicharcnt shows the actual number available. Rxiread should be asserted for one cycle when rxicharav is asserted to read out a character. The character will be available on rxichar the cycle following the assertion of rxiread. Figure 166 shows an example of reading characters from the receiver FIFO.

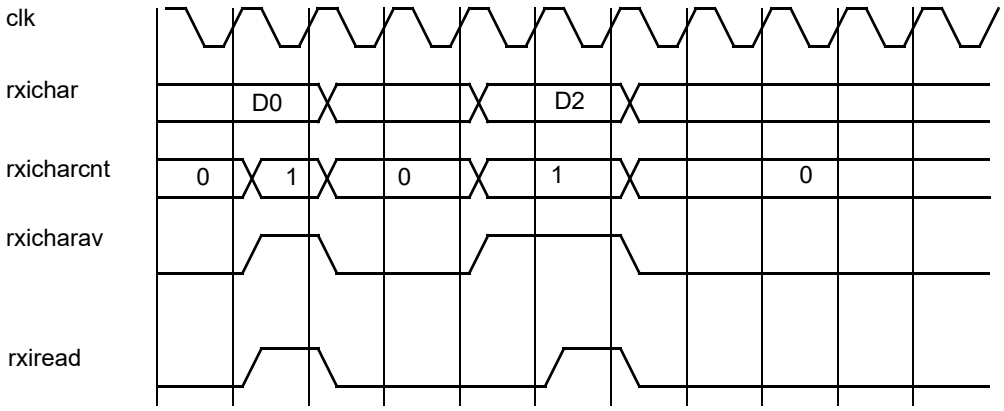


Figure 166. Receiving characters through the FIFO interface.

60.3.1 Link errors

When an link error occurs during reception an EEP is automatically inserted into the Receiver FIFO if the previous character written to the FIFO was not an EOP or EEP.

60.4 Transmitter interface

The transmitter interface consists of the following signals: txiwrite, txichar, txiflush, txicharcnt, txifull. Txifull is asserted when the transmitter FIFO is full while txicharcnt shows the actual number of characters currently in the FIFO. Txiwrite should be asserted for one cycle to write the value on txichar into the FIFO. Txiflush should be asserted for one cycle to discard all characters in the FIFO. No new characters should be written to the FIFO the same or the following cycle that txiflush is asserted. Figure 167 shows an example of writing characters to the transmitter FIFO.

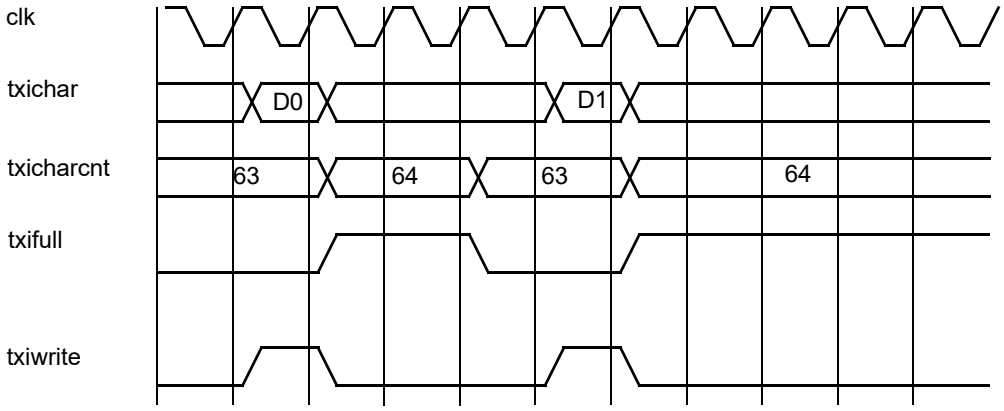


Figure 167. Transmitting characters through the FIFO interface.

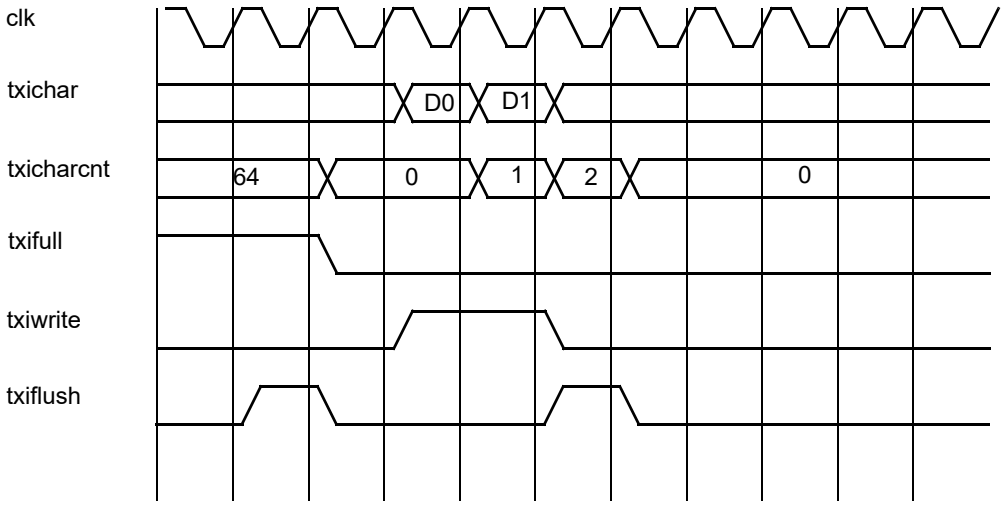


Figure 168. Use of txiflush.

60.4.1 Link errors

When a link error occurs characters read from the transmitter FIFO by the transmission logic will be discarded up to and including the next EOP or EEP character.

60.5 Implementation

60.5.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

There are five input resets, in order to cover every clock domain: AMBA reset (rst), transmitter synchronous reset (txsyncrst), receiver synchronous reset for port 0 (rxsyncrst0), receiver synchronous reset for port 1 (rxsyncrst1) and a receiver asynchronous reset shared by both ports (rxasyncrst).

Additionally, the core outputs an internal reset for synchronization between transmitter and receivers, lio.rxrst.

The core does not implement any kind of internal reset generation or synchronization, the input resets are completely independent. The reset generation shall be done in a higher instance, taking into account the clock domains and also the output reset of the core. A description of how the resets shall be combined and generated can be found below. Cobham Gaisler advise to follow these guidelines unless indicated otherwise.

- The AMBA reset is the external reset synchronized with the AMBA clock by using a reset generator.
- The transmitter reset is the external reset synchronized with the transmitter clock by using a reset generator.
- The asynchronous reset for both receiver channels is simply the output synchronization reset, lio.rxrst, connected directly to the input rxasyncrst.
- The synchronous reset for each receiver channel is the output receiver reset, lio.rxrst, synchronized with the appropriate clock domain by using a reset generator. Its output is the synchronous reset for the specific receiver port, rxsyncrst0 or rxsyncrst1.

Further information about the proper way of combining the reset signals or using the wrapper can be found in 60.13. Instantiation.

60.5.2 Clock-generation

The receiver module found in figure 161 should be clocked with a clock outputed by the GRSPW2_-PHY module. See the example instantiation in this section and the GRSPW2_PHY section of the grip manual for more information on how to connect this clock.

The transmitter clock is generated from the txclk input. A separate clock input is used to allow the transmitter to be run at much higher frequencies than the system clock. The SpaceWire node contains a clock-divider which divides the txclk signal to the wanted frequency. The transmitter clock should be 10 MHz during initialization and any frequency above 2 MHz in the run-state.

There is an input signal called clkdiv10 which sets the frequency during initialisation and one called clkdiv which is used in run-state. See 60.2.7 for details on how to set the clock divisor values.

Since only integer values are allowed for the clock division and the required init-frequency is 10 Mhz the frequency of the txclk input must be a multiple of 10 MHz. The clock divisor value is 8-bits wide so the maximum txclk frequency supported is 2.56 GHz (note that there is also a restriction on the relation between the system and transmit clock frequencies).

60.5.3 Timers

There are two timers in the codec: one for generating the 6.4/12.8 us periods and one for disconnect timing.

The timeout periods are generated from the tx clock whose frequency must be at least 10 MHz to guarantee disconnect timing limits. The same clock divisor is used as for the tx clock during initialisation so it must be set correctly for the link timing to work.

60.5.4 Synchronization

The transmitter and receiver bit rates can be eight times higher than the system clock frequency. This includes a large margin for clock skew and jitter so it might be possible to run at even higher rate differences. Note also that the receiver clocks data at both negative and positive edges for the input modes 0 and 1 so the bitrate is twice the clock frequency. There is no direct relationship between bitrate and frequency for the sampling modes.

The clock synchronization is just one limiting factor for the clock frequency, it might for example not be possible to achieve the highest possible frequency for certain technologies.

The asynchronous reset to the receiver clock domain has to have a maximum delay of one receiver clock cycle to ensure correct operation. This is needed because the receiver uses a completely asynchronous reset. To make sure that nothing bad happens there is a synchronous reset guard which prevents any signals from being assigned before all registers have their reset signals released.

In the sampling modes this asynchronous reset can be removed if both the receiver and transmitter runs on the same clock. In that case set the RXTX_SAMECLK generic to 1.

60.5.5 Fault-tolerance

The core can optionally be implemented with fault-tolerance against SEU errors in the FIFO memories. The fault-tolerance is enabled through the *ft* VHDL generic. Possible options are byte parity protection (*ft = 1*) or TMR registers (*ft = 2*). Note: the GPL version of GRLIB does not include fault-tolerance, and the core will not work unless the *ft* VHDL generic is 0.

60.5.6 Synthesis

The fact there are three clock domains in the core of which all are possibly high frequency clocks makes it necessary to declare all paths between the clock domains as false paths. In Synplify this is most easily done by declaring all the clocks to be in different clockgroups in the sdc file (if Synplify

does not automatically put them in different groups). This will disable any timing considerations between the clock domains and these constraints will also propagate to the place and route tool.

60.5.7 Technology mapping

The core has two generics for technology mapping: *tech and techfifo*. *Tech* selects the technology for DDR registers (if applicable) and FIFO memories. *Techfifo* selects whether *tech* should be used to select the technology for the FIFO memories or if they should be inferred. *Tech* and *memtech* can be set to any value from 0 to NTECH as defined in the GRLIB.TECH package.

60.5.8 RAM usage

The core maps all RAM memories on the syncram_2p component if the *ft* generic is 0 and to the syncram_2pft component for other values. The syncrams are located in the technology mapping library (TECHMAP). The organization of the different memories are described below. If techfifo and/or memtech is set to 0 the synthesis tool will infer the memories. Either RAM blocks or flip-flops will be used depending on the tool and technology. The number of flip-flops used is *syncram depth x syncram width* for all the different memories.

Transmitter FIFO

The transmitter FIFO consists of one syncram_2p block with a width of 9-bits. The depth is determined by the configured FIFO depth. Table 1006 shows the syncram organization for the allowed configurations.

Table 1006.syncram_2p sizes for the transmitter FIFO.

Fifosize	Syncram_2p organization
16	16x9
32	32x9
64	64x9
...	...
2048	2048x9

Receiver FIFO

The receiver FIFO consists of one syncram_2p block with a width of 9-bits. The depth is determined by the configured FIFO depth. Table 1007 shows the syncram organization for the allowed configurations.

Table 1007.syncram_2p sizes for the receiver FIFO.

Fifosize	Syncram_2p organization
16	16x9
32	32x9
64	64x9
...	...
2048	2048x9

60.6 Registers

There are no user accessible registers in the core.

60.7 Vendor and device identifiers

The vendor and device identifiers are only applicable for cores with AHB interfaces.

60.8 Configuration options

Table 1008 shows the configuration options of the core (VHDL generics).

*Table 1008.*Configuration options

Generic	Function	Allowed range	Default
ports	Sets the number of ports	1 - 2	1
input_type	Select receiver type. 0 = Self clocking (xor), 1 = Interface for SpaceWire transceiver, 2 = Single data rate sampling, 3 and 4 = Double data rate sampling, 5 = Self-clocking with external recovery, 6 = Self-clocking with external recovery and DDR register for data.. This generic must be set to the same value as the GRSPW2_PHY generic with the same name.	0 - 6	0
output_type	Select transmitter type. 0 = single data rate, 1 = double data rate, 2 = interface for SpaceWire transceiver	0 - 2	0
rxtx_sameclk	Set to one if the same clock net is connected to both the receiver and transmitter (which means this feature is only applicable when the receiver uses sampling). This will remove some unnecessary synchronization registers.	0 - 1	0
fifosize	Sets the number of entries in the 9-bit wide transmitter and receiver FIFOs.	16 - 2048	64
tech	Technology for FIFO memories.	0 - NTECH	inferred
scantest	Enable scantest features.	0 - 1	0
techfifo	Enable GRLIB technology mapped FIFO memories. If not enabled a behavioral model is used and the result will be synthesis tool dependent.	0 - 1	0
ft	Enable fault-tolerance against SEU errors	0 - 2	0
rstsrctmr	Enables the Triple Module Redundancy for the asynchronous reset nets of the core	0 - 1	0

60.9 Signal descriptions

Table 1009 shows the interface signals of the core (VHDL ports).

Table 1009. Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	AMBA Reset	Low
CLK	N/A	Input	AMBA Clock	-
RXASYNCRST	N/A	Input	Asynchronous reset for ports 0 and 1 of the receiver	Low
RXSYNCRST0	N/A	Input	Synchronous reset for port 0 of the receiver	Low
RXCLK0	N/A	Input	Receiver clock for port 0.	-
RXSYNCRST1	N/A	Input	Synchronous reset for port 1 of the receiver	Low
RXCLK1	N/A	Input	Receiver clock for port 1. Unused if the VHDL generic ports is 2.	-
TXSYNCRST	N/A	Input	Synchronous reset for the transmitter	Low
TXCLK	N/A	Input	Transmitter default run-state clock	-

Table 1009. Signal descriptions

Signal name	Field	Type	Function	Active
TXCLKN	N/A	Input	Transmitter inverted default run-state clock. Only used in DDR transmitter mode for technologies not supporting local generation of inverted clock.	-
TESTEN	N/A	Input	Scan test enable	High
TESTRST	N/A	Output	Scan test reset	Low
LII	D[3:0]	Input	Data input. Should be connected to the GRSPW2_PHY. Each bit is valid when the bit at the corresponding index in the DV signal is asserted. Bits (1:0) are used for port 0 and bits (3:2) are used for port 1 if enabled. If only one bit is received during one clock cycle then only the bit at the lower index is valid. If both bits are valid then the one at the lower index was the one received first. Bits (1:0) should be sycnhronous to RXCLK0 and bits (3:2) to RXCLK1.	-
	DV[3:0]	Input	Data valid qualifier for the D input.	High
	DCONNECT[3:0]	Input	Disconnect reset. When asserted the corresponding disconnect counter will be reset. The counters connected to bits (1:0) apply to port 0 while (3:2) apply to port 1 if enabled.	Low
	DCONNECT2[3:0]	Input	Disconnect. Bits 3:2 are unused in one-port configurations. This is a copy of DCONNECT, as part of the triplication of the combinational logic related to asynchronous reset nets.	Low
	DCONNECT3[3:0]	Input	Disconnect. Bits 3:2 are unused in one-port configurations. This is a copy of DCONNECT, as part of the triplication of the combinational logic related to asynchronous reset nets.	Low
	LINKDISABLED	Input	Disables the SpaceWire link	High
	LINKSTART	Input	Starts the SpaceWire link	High
	AUTOSTART	Input	Enables the autostart feature for the SpaceWire link	High
	PORTSEL	Input	Selects the active port if the NOPORTFORCE signal is set to 0 and the core is configured with dual ports.	-
	NOPORTFORCE	Input	Disables forced portselection using the PORTSEL signal and lets the core automatically select the active link.	High
	RDIVISOR[7:0]	Input	Clock divisor value used for generating the transmit frequency from the txclk input in run-state. Bit 0 is the least significant. See 60.2.7 for details on how to set this input signal.	-
	IDIVISOR[7:0]	Input	Clock divisor value used for generating the transmit frequency from the txclk input during initialization (started and connecting states). Bit 0 is the least significant. See 60.2.7 for details on how to set this input signal.	-
	RXIREAD	Input	Receiver FIFO read. Assert for one cycle (synchronous to CLK) and the next character will be available on the RXICHAR output the next clock cycle if available in the FIFO.	High

Table 1009. Signal descriptions

Signal name	Field	Type	Function	Active
	RXIFIFORST	Input	Empty the receiver FIFO. When asserted for one cycle (synchronous to CLK) all characters currently present in the FIFO will be discarded. The reset will have taken on the second cycle after the reset. The first cycle after characters may still be present.	High
	TXIWRITE	Input	Transmitter FIFO write. Assert for one cycle (synchronous to CLK) to write the character on the TXICHAR input into the FIFO on the rising edge of the clock.	High
	TXICHAR[8:0]	Input	Transmit character input to FIFO. Characters are transmitted in the order they are written into the FIFO. Bit 0 is the SpaceWire control bit. When set to 1 only bits (2:1) are transmitted (EOP or EEP). Bits are transmitted in order beginning at the lowest index.	-
	TXIFIFORST	Input	Empty the transmitter FIFO. When asserted for one cycle (synchronous to CLK) all characters currently present in the FIFO will be discarded. New characters shall not be written to the transmitter FIFO the same cycle or the cycle after TXIFIFORST is asserted.	High
	TICKIN	Input	Time counter tick input. Should be asserted one clock cycle (synchronous to CLK) to transmit a time-code. If the FSM is not in run-state no time-code will be transmitted and the tick will not be registered. The TICKIN_DONE output can be used to verify that the time-code has been transmitted,	High
	TIMECTRLIN[1:0]	Input	Control bits for time-code. Transmitted in order starting at the lowest index when tickin is asserted. The controlbits are transmitted after the time-count value.	-
	TIMEIN[5:0]	Input	Time-count value for time-code. Transmitted in order starting at the lowest index when tickin is asserted.	-

Table 1009. Signal descriptions

Signal name	Field	Type	Function	Active
LIO	DO[3:0]	Output	Data output. Bit 0 is the standard output for port 0 and bit 2 for port 1 if enabled. Bit 1 is used for port 0 and bit 3 for port 1 if the core is connected to an external PHY.	-
	SO[3:0]	Output	Strobe output. Bit indexes are used correspondingly to the DO output.	-
	STATE[2:0]	Output	Current linkinterface FSM state. 0=error-reset, 1=error-wait, 2=ready, 3=started, 4=connecting, 5=run.	-
	ACTPORT	Output	0=port 0 is active and 1=port 1 is active. Unused if the second port is not enabled.	-
	DCONNECTERR	Output	Asserted for one clock cycle (synchronous to CLK) when a disconnect error is detected.	High
	CREDERR	Output	Asserted for one clock cycle (synchronous to CLK) when a credit error is detected.	High
	ESCERR	Output	Asserted for one clock cycle (synchronous to CLK) when an escape error is detected.	High
	PARERR	Output	Asserted for one clock cycle (synchronous to CLK) when a parity error is detected.	High
	RXICHARAV	Output	Asserted when one or more characters are available in the receiver FIFO. Synchronous to CLK.	High
	RXICHARCNT[6:0]	Output	Number of characters present in the receiver FIFO. Synchronous to CLK.	-
	RXICHAR[8:0]	Output	Character read from the receiver FIFO. Valid the clock cycle following the assertion of the RXIREAD input. Synchronous to CLK. Bit 0 corresponds to the SpaceWire control bit and when set to 1 only bits (2:1) are valid (EOP or EEP).	-
	TXICHARCNT[6:0]	Output	Number of characters present in the transmitter FIFO. Synchronous to CLK.	-
	TXIFULL	Output	Asserted when the transmitter FIFO is full. Synchronous to CLK.	High
	TXIEMPTY	Output	Asserted when the transmitter FIFO is empty. Synhronous to CLK.	High
	TICKIN_DONE	Output	Asserted for one cycle when the time-code has been transmitted resulting from an assertion of TICKIN. When TICKIN_DONE is asserted the TICKIN should be deasserted the same cycle if it is not desired that another time-code should be deasserted.	High
	TICKOUT	Output	Time-code tickout output. Asserted for one clock cycle (synchronous to CLK) when a time-code has been received. When asserted the TIMEOUT and TIMECTRLOUT outputs are valid.	High
	TIMEOUT[7:0]	Output	Time-code output. Synchronous to CLK.	-
	RXRST	Output	Internal reset generated by the transmitter for synchronization purpose between transmitter and both receiver channels. It shall be used to generate the asynchronous and synchronous receiver resets.	Low

60.10 Signal definitions and reset values

The signals and their reset values are described in table 1010.

*Table 1010.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
spw_clk	Input	Transmitter default run-state clock	Rising edge	-
spw_rxd	Input, LVDS	Data input, positive	High	-
spw_rxdn	Input, LVDS	Data input, negative	Low	-
spw_rxs	Input, LVDS	Strobe input, positive	High	-
spw_rxsn	Input, LVDS	Strobe input, negative	Low	-
spw_txd	Output, LVDS	Data output, positive	High	Logical 0
spw_txdn	Output, LVDS	Data output, negative	Low	Logical 1
spw_txs	Output, LVDS	Strobe output, positive	High	Logical 0
spw_txsn	Output, LVDS	Strobe output, negative	Low	Logical 1

60.11 Timing

The timing waveforms and timing parameters are shown in figure 169 and are defined in table 1011.

The SpaceWire jitter and skew timing waveforms and timing parameters are shown in figure 170 and are defined in table 1012.

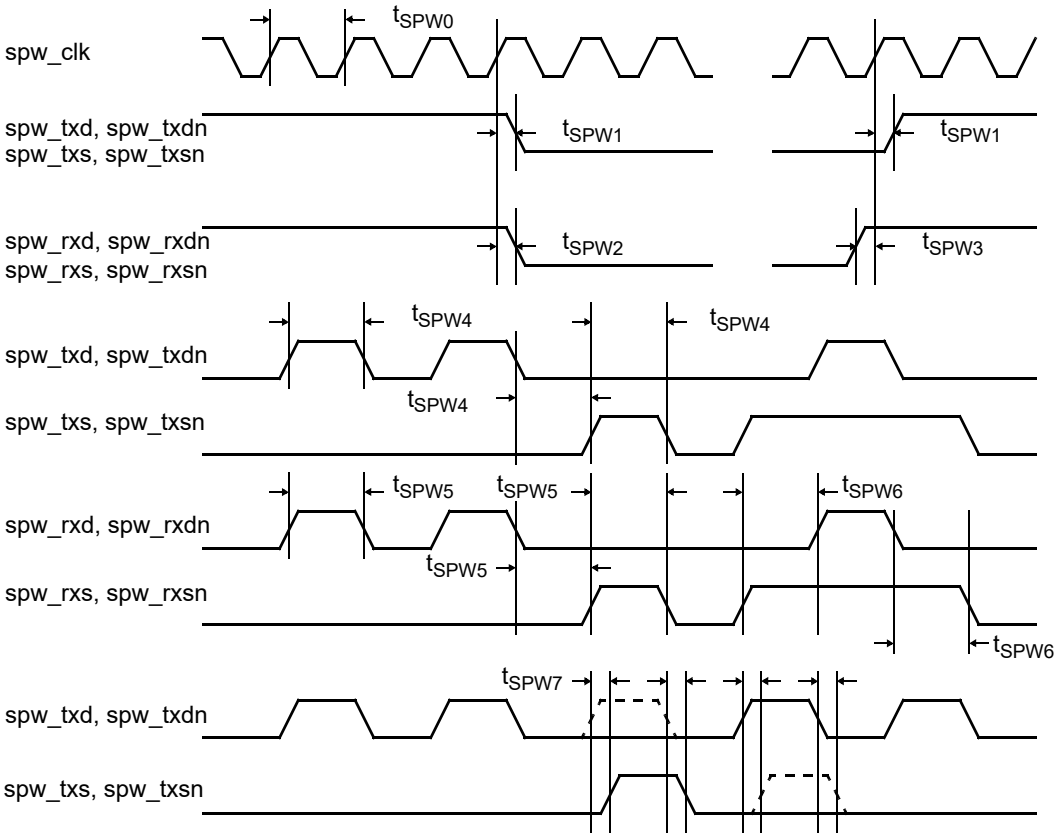


Figure 169. Timing waveforms

*Table 1011.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{SPW0}	transmit clock period	-	TBD	-	ns
t_{SPW1}	clock to output delay	rising *spw_clk* edge	TBD	TBD	ns
t_{SPW2}	input to clock hold	-	-	-	not applicable
t_{SPW3}	input to clock setup	-	-	-	not applicable
t_{SPW4}	output data bit period	-	-		*clk* periods
		-	t_{SPW0} - TBD	t_{SPW0} +TBD	ns
t_{SPW5}	input data bit period	-	TBD	-	ns
t_{SPW6}	data & strobe edge separation	-	TBD	-	ns
t_{SPW7}	data & strobe output skew	-	-	TBD	ns

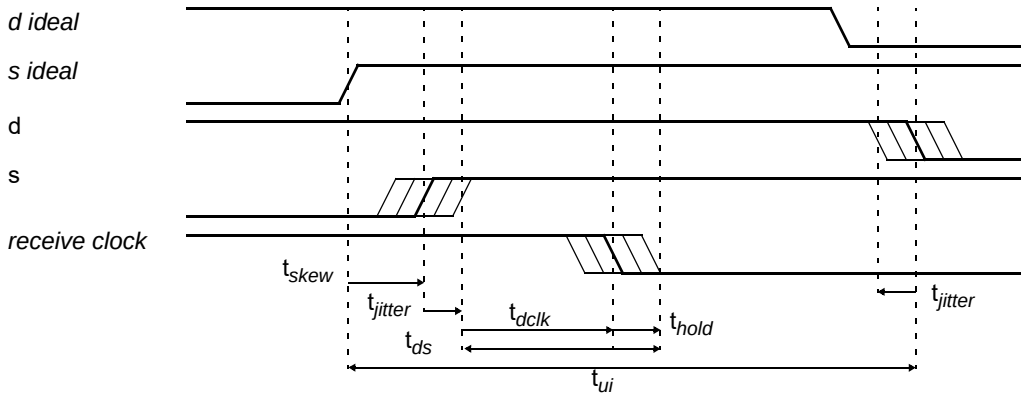


Figure 170. Skew and jitter timing waveforms

*Table 1012.*Skew and jitter timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{skew}	skew between data and strobe	-	-	TBD	ns
t_{jitter}	jitter on data or strobe	-	-	TBD	ns
t_{ds}	minimum separation between data and strobe edges	-	TBD	-	ns
t_{dclk}	delay from edge of data or strobe to the receiver flip-flop	-	-	TBD	ns
t_{hold}	hold timer on receiver flip-flop	-	TBD	-	ns
t_{ui}	unit interval (bit period)	-	TBD	-	ns

60.12 Library dependencies

Table 1013 shows libraries used when instantiating the core (VHDL libraries).

*Table 1013.*Library dependencies

Library	Package	Imported unit(s)	Description
GAISLER	SPACEWIRE	Signals, component	Component and record declarations.

60.13 Instantiation

This example shows how the core can be instantiated.

Normally di, si, do and so should be connected to input and output pads configured with LVDS drivers. How this is done is technology dependent.

The core in the example is configured with non-ft technology mapped FIFOs of size 64. It uses DDR sampling on the input and the combined sampling/transmitter frequency (spw_rxtxclk) is 50MHz.

The minimum amount of signals that need to be driven to put the codec in a deterministic initial state is shown.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.tech.all;
library gaisler;
use gaisler.spacewire.all;
```

```
entity spacewire_ex is
  port (
    clk           : in  std_ulogic;
    rstn          : in  std_ulogic;

    -- spacewire signals
    spw_rxdp      : in  std_ulogic;
    spw_rxdn      : in  std_ulogic;
    spw_rxsp      : in  std_ulogic;
    spw_rxsn      : in  std_ulogic;
    spw_txdp      : out std_ulogic;
    spw_txdn      : out std_ulogic;
    spw_txsp      : out std_ulogic;
    spw_txsn      : out std_ulogic;

    spw_rxtxclk   : in  std_ulogic;
    spw_rxclkn    : in  std_ulogic;
    testen        : in  std_ulogic;
    testrst       : in  std_ulogic
    );
end;

architecture rtl of spacewire_ex is

  -- Spacewire signals
  signal lii       : grspw_codec_in_type;
  signal lio       : grspw_codec_out_type;
  signal di        : std_ulogic;
  signal si        : std_ulogic;
  signal rxclko    : std_ulogic;

  -- Internal resets
  signal mrst      : std_ulogic;
  signal rxasyncrst: std_ulogic;
  signal rxsyncrst0: std_ulogic;
  signal rxsyncrst1: std_ulogic;
  signal txsyncrst : std_ulogic;

begin

  spw_phy0 : grspw2_phy
    generic map(
      scantest   => 0,
      tech       => memtech,
      input_type => 3)
    port map(
      rstn       => rstn,
      rxclki     => spw_rxtxclk,
      rxclkin    => spw_rxclkn,
      nrxclki    => spw_rxtxclk,
      di         => di,
      si         => si,
      do         => lii.d(1 downto 0),
      dov        => lii.dv(1 downto 0),
      dconnect   => lii.dconnect(1 downto 0),
      dconnect2  => lii.dconnect2(1 downto 0),
      dconnect3  => lii.dconnect3(1 downto 0),
      rxclko     => rxclko);

  -- Internal reset generators (TX, RX0 and RX1 clock domains)

  -- CLK domain (synchronous reset)
  AMBA_rst : rstgen
  port map (rstn, clk, vcc, mrst, open);

  -- TX domain (synchronous reset)
  txrst : rstgen
  port map (rstn, spw_rxtxclk, vcc, txsyncrst, open);

  -- RX domain (asynchronous reset)
  rxasyncrst <= lio.rxrst;
```

```
-- RX domain (synchronous reset)
rxsyncrst0 : rstgen
port map (lio.rxrst, rxclk0, vcc, rxsyncrst0, open);
rxsyncrst1 : rstgen
port map (lio.rxrst, rxclk1, vcc, rxsyncrst1, open);

codec : grspw_codec
  generic map(
    ports        => 1,
    input_type   => 0,
    output_type  => 3,
    rxtx_sameclk => 1,
    fifosize     => 64,
    tech         => 11,
    scantest     => 0,
    techfifo     => 1,
    ft           => 0)
  port map(
    rst          => mrst,
    clk          => clk,
    rxasyncrst   => rxasyncrst,
    rxsyncrst0   => rxsyncrst0,
    rxclk0       => rxclk0,
    rxsyncrst1   => rxsyncrst1,
    rxclk1       => rxclk1,
    txsyncrst    => txsyncrst,
    txclk        => spw_rxtxclk,
    txclkn       => spw_rxtxclk,
    testen       => testen,
    testrst      => testrst,
    lii          => lii,
    lio          => lio);

lii.linkdisabled <= '1';
lii.linkstart    <= '0';
lii.autostart    <= '0';
lii.portsel      <= '0';
lii.noportforce  <= '0';
lii.idivisor     <= conv_std_logic_vector(4, 8);
lii.rdivisor     <= conv_std_logic_vector(0, 8);

lii.rxiread      <= '0';
lii.txiwrite     <= '0';
lii.txichar      <= (others => '0');
lii.txiflush     <= '0';
lii.tickin       <= '0';
lii.timectrlin   <= (others => '0');

spw_rxd_pad : inpad_ds generic map (padtech, lvds, x25v)
  port map (spw_rxdp, spw_rxdn, di);
spw_rxs_pad : inpad_ds generic map (padtech, lvds, x25v)
  port map (spw_rxsp, spw_rxsn, si);
spw_txd_pad : outpad_ds generic map (padtech, lvds, x25v)
  port map (spw_txdp, spw_txdn, lio.d(0), gnd(0));
spw_txs_pad : outpad_ds generic map (padtech, lvds, x25v)
  port map (spw_txsp, spw_txsn, lio.s(0), gnd(0));
...
```

61 GRSPW_CODEC_GEN - GRSPW_CODEC wrapper with Std_Logic interface

61.1 Overview

The GRSPW_CODEC_GEN wrapper provides an interface to the GRSPW_CODEC core only using Std_Logic signals instead of GRLIB records. The GRLIB AMBA plug and play extensions have also been removed. This document describes the signal interface and how they map to the signal names in GRLIB. An example instantiation of the core can be found at the end of this document.

61.2 Signal descriptions

Table 1009 shows the interface signals of the core (VHDL ports).

Table 1014. Signal descriptions

Signal name	Type	Function	Active	GRLIB signal name
RST	Input	AMBA reset	Low	RST
CLK	Input	System (AMBA) Clock.	-	CLK
RXASYNCRST	Input	Receiver asynchronous reset for both ports 0 and 1	Low	RXASYNCRST
RXSYNCRST0	Input	Receiver synchronous reset for port 0	Low	RXSYNCRST0
RXCLK0	Input	Receiver clock for port 0.	-	RXCLK0
RXSYNCRST1	Input	Receiver synchronous reset for port 1	Low	RXSYNCRST1
RXCLK1	Input	Receiver clock for port 1. Unused if the VHDL generic ports is 2.	-	RXCLK1
TXSYNCRST	Input	Transmitter synchronous reset	Low	TXSYNCRST
TXCLK	Input	Transmitter default run-state clock	-	TXCLK
TXCLKN	Input	Transmitter inverted default run-state clock. Only used in DDR transmitter mode for technologies not supporting local generation of inverted clock.	-	TXCLKN
TESTEN	Input	Scan test enable	High	TESTEN
TESTRST	Output	Scan test reset	Low	TESTRST
D[3:0]	Input	Data input. Should be connected to the GRSPW2_PHY. Each bit is valid when the bit at the corresponding index in the DV signal is asserted. Bits (1:0) are used for port 0 and bits (3:2) are used for port 1 if enabled. If only one bit is received during one clock cycle then only the bit at the lower index is valid. If both bits are valid then the one at the lower index was the one received first. Bits (1:0) should be sycnhronous to RXCLK0 and bits (3:2) to RXCLK1.	-	LII.D
DV[3:0]	Input	Data valid qualifier for the D input.	High	LII.DV
DCONNECT[3:0]	Input	Disconnect reset. When asserted the corresponding disconnect counter will be reset. The counters connected to bits (1:0) apply to port 0 while (3:2) apply to port 1 if enabled.	Low	LII.DCONNECT
DCONNECT2 [3:0]	Input	SpaceWire Disconnect reset. Copy of DCONNECT (triplication of the asynchronous resets logic).	Low	LII.DCONNECT2
DCONNECT3 [3:0]	Input	SpaceWire Disconnect reset. Copy of DCONNECT (triplication of the asynchronous resets logic).	Low	LII.DCONNECT3
LINKDISABLED	Input	Disables the SpaceWire link	High	LII.LINKDISABLED

Table 1014. Signal descriptions

Signal name	Type	Function	Active	GRLIB signal name
LINKSTART	Input	Starts the SpaceWire link	High	LII.LINKSTART
AUTOSTART	Input	Enables the autostart feature for the SpaceWire link	High	LII.AUTOSTART
PORTSEL	Input	Selects the active port if the NOPORTFORCE signal is set to 0 and the core is configured with dual ports.	-	LII.PORTSEL
NOPORTFORCE	Input	Disables forced portselection using the PORTSEL signal and lets the core automatically select the active link.	High	LII.NOPORTFORCE
RDIVISOR[7:0]	Input	Clock divisor value used for generating the transmit frequency from the txclk input in run-state. Bit 0 is the least significant.	-	LII.RDIVISOR
IDIVISOR[7:0]	Input	Clock divisor value used for generating the transmit frequency from the txclk input during initialization (started and connecting states). This value is also used to generate the disconnect timing and the FSM timeouts (6.4 us and 12.8 us). Bit 0 is the least significant.	-	LII.IDIVISOR
RXIREAD	Input	Receiver FIFO read. Assert for one cycle (synchronous to CLK) and the next character will be available on the RXICHAR output the next clock cycle if available in the FIFO.	High	LII.RXIREAD
RXIFIFORST	Input	Empty the receiver FIFO. When asserted for one cycle (synchronous to CLK) all characters currently present in the FIFO will be discarded. The reset will have taken on the second cycle after the reset. The first cycle after characters may still be present.	High	LII.RXIFIFORST
TXIWRITE	Input	Transmitter FIFO write. Assert for one cycle (synchronous to CLK) to write the character on the TXICHAR input into the FIFO on the rising edge of the clock.	High	LII.TXIWRITE
TXICHAR[8:0]	Input	Transmit character input to FIFO. Characters are transmitted in the order they are written into the FIFO. Bit 0 is the SpaceWire control bit. When set to 1 only bits (2:1) are transmitted (EOP or EEP). Bits are transmitted in order beginning at the lowest index.	-	LII.TXICHAR
TXIFIFORST	Input	Empty the transmitter FIFO. When asserted for one cycle (synchronous to CLK) all characters currently present in the FIFO will be discarded. New characters shall not be written to the transmitter FIFO the same cycle or the cycle after TXIFIFORST is asserted.	High	LII.TXIFIFORST
TICKIN	Input	Time counter tick input. Should be asserted one clock cycle (synchronous to CLK) to transmit a time-code. If the FSM is not in run-state no time-code will be transmitted and the tick will not be registered. The TICKIN_DONE output can be used to verify that the time-code has been transmitted,	High	LII.TICKIN
TIMEIN[7:0]	Input	Time-code input. Transmitted in order starting at the lowest index when tickin is asserted.	-	LII.TIMEIN

Table 1014. Signal descriptions

Signal name	Type	Function	Active	GRLIB signal name
DO[3:0]	Output	Data output. Bit 0 is the standard output for port 0 and bit 2 for port 1 if enabled. Bit 1 is used for port 0 and bit 3 for port 1 if the core is connected to an external Aeroflex PHY.	-	LIO.DO
SO[3:0]	Output	Strobe output. Bit indexes are used correspondingly to the DO output.	-	LIO.SO
STATE[2:0]	Output	Current linkinterface FSM state. 0=error-reset, 1=error-wait, 2=ready, 3=started, 4=connecting, 5=run.	-	LIO.STATE
ACTPORT	Output	0=port 0 is active and 1=port 1 is active. Unused if the second port is not enabled.	-	LIO.ACTPORT
DCONNECTERR	Output	Asserted for one clock cycle (synchronous to CLK) when a disconnect error is detected.	High	LIO.DCONNECTERR
CREDERR	Output	Asserted for one clock cycle (synchronous to CLK) when a credit error is detected.	High	LIO.CREDERR
ESCERR	Output	Asserted for one clock cycle (synchronous to CLK) when an escape error is detected.	High	LIO.ESCERR
PARERR	Output	Asserted for one clock cycle (synchronous to CLK) when a parity error is detected.	High	LIO.PARERR
RXICHARAV	Output	Asserted when one or more characters are available in the receiver FIFO. Synchronous to CLK.	High	LIO.RXICHARAV
RXICH-ARCNT[11:0]	Output	Number of characters present in the receiver FIFO. Synchronous to CLK.	-	LIO.RXICHARCNT
RXICHAR[8:0]	Output	Character read from the receiver FIFO. Valid the clock cycle following the assertion of the RXIREAD input. Synchronous to CLK. Bit 0 corresponds to the SpaceWire control bit and when set to 1 only bits (2:1) are valid (EOP or EEP).	-	LIO.RXICHAR
TXICH-ARCNT[11:0]	Output	Number of characters present in the transmitter FIFO. Synchronous to CLK.	-	LIO.TXICHARCNT
TXIFULL	Output	Asserted when the transmitter FIFO is full. Synchronous to CLK.	High	LIO.TXIFULL
TXIEMPTY	Output	Asserted when the transmitter FIFO is empty. Synhronous to CLK.	High	LIO.TXIEMPTY
TXIFIFORSTACT	Output	FIFO reset active. Used in router when writing EEP after reset.	High	LIO.TXIFIFORSTACT

Table 1014. Signal descriptions

Signal name	Type	Function	Active	GRLIB signal name
TICKIN_DONE	Output	Asserted for one cycle when the time-code has been transmitted resulting from an assertion of TICKIN. When TICKIN_DONE is asserted the TICKIN should be deasserted the same cycle if it is not desired that another time-code should be deasserted.	High	LIO.TICKIN_DONE
TICKOUT	Output	Time-code tickout output. Asserted for one clock cycle (synchronous to CLK) when a time-code has been received. When asserted the TIMEOUT output is valid.	High	LIO.TICKOUT
TIMEOUT[7:0]	Output	Time-code output. Synchronous to CLK.	-	LIO.TIMEOUT
MERROR	Output	Asserted one clock cycle when an EDAC memory error is detected.	High	LIO.MERROR
RXRST	Output	Internal reset generated by the transmitter for synchronization purpose between transmitter and both receiver channels. It shall be used to generate the asynchronous and synchronous receiver resets.	Low	LIO.RXRST

61.3 Instantiation

This example shows how the core can be instantiated. It also includes the reset generators.

Normally di, si, do and so should be connected to input and output pads configured with LVDS drivers. How this is done is technology dependent.

The core in the example is configured with non-ft technology mapped FIFOs of size 64. It uses DDR sampling on the input and the combined sampling/transmitter frequency (spw_rxtxclk) is 50MHz.

The minimum amount of signals that need to be driven to put the codec in a deterministic initial state is shown.

```
library grlib;
use grlib.tech.all;
library gaisler;
use gaisler.spacewire.all;

entity spacewire_ex is
  port (
    clk           : in  std_ulogic;
    rstn          : in  std_ulogic;
    -- spacewire signals
    spw_rxdp      : in  std_ulogic;
    spw_rxdn      : in  std_ulogic;
    spw_rxsp      : in  std_ulogic;
    spw_rxsn      : in  std_ulogic;
    spw_txdp      : out std_ulogic;
    spw_txdn      : out std_ulogic;
    spw_txsp      : out std_ulogic;
    spw_txsn      : out std_ulogic;
    spw_rxtxclk   : in  std_ulogic;
    spw_rxclkn    : in  std_ulogic;
    testen        : in  std_ulogic;
    testrst       : in  std_ulogic
    );
end;

architecture rtl of spacewire_ex is

  signal di              : std_ulogic;
```

```
  signal si              : std_ulogic;
  signal d               : std_logic_vector(3 downto 0);
  signal dv              : std_logic_vector(3 downto 0);
  signal dconnect        : std_logic_vector(3 downto 0);
  signal dconnect2       : std_logic_vector(3 downto 0);
  signal dconnect3       : std_logic_vector(3 downto 0);
  signal do              : std_logic_vector(3 downto 0);
  signal so              : std_logic_vector(3 downto 0);
  signal rxclko          : std_ulogic;
  signal linkdisabled    : std_ulogic;
  signal linkstart       : std_ulogic;
  signal autostart       : std_ulogic;
  signal portsel         : std_ulogic;
  signal noportforce     : std_ulogic;
  signal rdivisor        : std_logic_vector(7 downto 0);
  signal idivisor        : std_logic_vector(7 downto 0);
  signal rxiread         : std_ulogic;
  signal rxififorst      : std_ulogic;
  signal txiwrite        : std_ulogic;
  signal txichar         : std_logic_vector(8 downto 0);
  signal txififorst      : std_ulogic;
  signal tickin          : std_ulogic;
  signal timein          : std_logic_vector(7 downto 0);
  signal do              : std_logic_vector(3 downto 0);
  signal so              : std_logic_vector(3 downto 0);
  signal state           : std_logic_vector(2 downto 0);
  signal actport         : std_ulogic;
  signal dconnecterr     : std_ulogic;
  signal crederr         : std_ulogic;
  signal escerr          : std_ulogic;
  signal parerr          : std_ulogic;
  signal rxicharav       : std_ulogic;
  signal rxicharcnt      : std_logic_vector(11 downto 0);
  signal rxichar         : std_logic_vector(8 downto 0);
  signal txicharcnt      : std_logic_vector(11 downto 0);
  signal txifull         : std_ulogic;
  signal txiempty        : std_ulogic;
  signal tickin_done     : std_ulogic;
  signal tickout         : std_ulogic;
  signal timeout         : std_logic_vector(7 downto 0);
  signal merror          : std_ulogic;

  -- Internal resets
  signal mrst      : std_ulogic;
  signal rxasyncrst: std_ulogic;
  signal rxsyncrst0: std_ulogic;
  signal rxsyncrst1: std_ulogic;
  signal txsyncrst : std_ulogic;

begin

  spw_rxd_pad : inpad_ds generic map (tech => padtech, level => lvds)
                           port map (spw_rxd, spw_rxdn, di);
  spw_rxs_pad : inpad_ds generic map (tech => padtech, level => lvds)
                           port map (spw_rxs, spw_rxsn, si);

  spw_phy0 : grspw2_phy
    generic map(
      scantest   => 0,
      tech       => memtech,
      input_type => 3)
    port map(
      rstn       => rstn,
      rxclki     => spw_rxtxclk,
      rxclkin    => spw_rxclkn,
      nrxclki    => spw_rxtxclk,
      di         => di,
      si         => si,
      do         => d(1 downto 0),
      dov        => dv(1 downto 0),
      dconnect   => dconnect(1 downto 0),
```

```
    dconnect2  => dconnect2(1 downto 0),
    dconnect3  => dconnect3(1 downto 0),
    rxclko     => rxclk0);

d(3 downto 2)         <= "00"; -- For second port
dv(3 downto 2)        <= "00"; -- For second port
dconnect(3 downto 2)  <= "00"; -- For second port
dconnect2(3 downto 2) <= "00"; -- For second port
dconnect3(3 downto 2) <= "00"; -- For second port

-- Internal reset generators (TX, RX0 and RX1 clock domains)

-- CLK domain (synchronous reset)
AMBA_rst : rstgen
port map (rstn, clk, vcc, mrst, open);

-- TX domain (synchronous reset)
txrst : rstgen
port map (rstn, spw_rxtxclk, vcc, txsyncrst, open);

-- RX domain (asynchronous reset)
rxasyncrst <= rxrst;

-- RX domain (synchronous reset)
rxsyncrst0 : rstgen
port map (rxrst, rxclk0, vcc, rxsyncrst0, open);
rxsyncrst1 : rstgen
port map (rxrst, rxclk1, vcc, rxsyncrst1, open);

codec : grspw_codec_gen
  generic map(
    ports        => 1,
    input_type   => 0,
    output_type  => 3,
    rxtx_sameclk => 1,
    fifosize     => 64,
    tech         => 11,
    scantest     => 0,
    techfifo     => 1,
    ft           => 0)
  port map(
    rst           => mrst,
    clk           => clk,
    rxasyncrst    => rxasyncrst,
    rxsyncrst0    => rxsyncrst0,
    rxclk0        => rxclk0,
    rxsyncrst1    => rxsyncrst1,
    rxclk1        => rxclk1,
    txsyncrst     => txsyncrst,
    txclk         => spw_rxtxclk,
    txclkn        => spw_rxtxclk,
    testen        => testen,
    testrst       => testrst,
    d             => d,
    dv            => dv,
    dconnect      => dconnect,
    dconnect2     => dconnect2,
    dconnect3     => dconnect3,
    do            => do,
    so            => so,
    linkdisabled  => linkdisabled,
    linkstart     => linkstart,
    autostart     => autostart,
    portsel       => portsel,
    noportforce   => noportforce,
    rdivisor      => rdivisor,
    idivisor      => idivisor,
    state         => state,
    actport       => actport,
    dconnecterr   => dconnecterr,
    crederr       => crederr,
```

```
    escerr        => escerr,
    parerr        => parerr,
    rxicharav     => rxicharav,
    rxicharcnt    => rxicharcnt,
    rxichar       => rxichar,
    rxiread       => rxiread,
    rxififorst    => rxififorst,
    txicharcnt    => txicharcnt,
    txifull       => txifull,
    txiempty      => txiempty,
    txiwrite      => txiwrite,
    txichar       => txichar,
    txififorst    => txififorst,
    txififorstact => txififorstact,
    tickin        => tickin,
    timein        => timein,
    tickin_done   => tickin_done,
    tickout       => tickout,
    timeout       => timeout,
    merror        => merror,
    rxrst         => rxrst);

linkdisabled <= '1';
linkstart    <= '0';
autostart    <= '0';
portsel      <= '0';
noportforce  <= '0';
idivisor     <= conv_std_logic_vector(4, 8);
rdivisor     <= conv_std_logic_vector(0, 8);

rxiread      <= '0';
txiwrite     <= '0';
txichar      <= (others => '0');
txiflush     <= '0';
tickin       <= '0';
timein       <= (others => '0');

spw_rxd_pad : inpad_ds generic map (padtech, lvds, x25v)
  port map (spw_rxdp, spw_rxdn, di);
spw_rxs_pad : inpad_ds generic map (padtech, lvds, x25v)
  port map (spw_rxsp, spw_rxsn, si);
spw_txd_pad : outpad_ds generic map (padtech, lvds, x25v)
  port map (spw_txdp, spw_txdn, do(0), gnd(0));
spw_txs_pad : outpad_ds generic map (padtech, lvds, x25v)
  port map (spw_txsp, spw_txsn, so(0), gnd(0));
...
```

62 GRSPWROUTER - SpaceWire router

62.1 Overview

The SpaceWire router core implements a SpaceWire routing switch as defined in the ECSS-E-ST-50-12C standard. It supports from 2 to 31 ports in addition to the mandatory configuration port where each port (except the configuration port) can be individually configured to be SpaceWire links, FIFO interfaces or AMBA interfaces. The AMBA ports are limited to a maximum of 16 in a single router. Status and configuration are read and written through a RMAP target at port 0. There is an optional AHB slave interface for accessing the router configuration registers. Group adaptive routing and packet distribution are fully supported (two ports up to all ports can be assigned to an address). System time-distribution is also supported. The router is designed to be technology independent and configurable. This enables it to be implemented in all technologies supported by the GRLIB IP library and also to remove optional features to save area.

It provides an RMAP target for configuration at port 0 used for accessing internal configuration and status registers. In addition to this there are three different external port types: SpaceWire links, FIFO interfaces and AMBA interfaces. An AHB slave interface is also provided for accessing the port 0 registers from the AHB bus. Group adaptive routing and packet distribution are fully supported (two ports up to all ports can be assigned to an address). System time-distribution is also supported. Timers are available for each port to prevent deadlock situations.

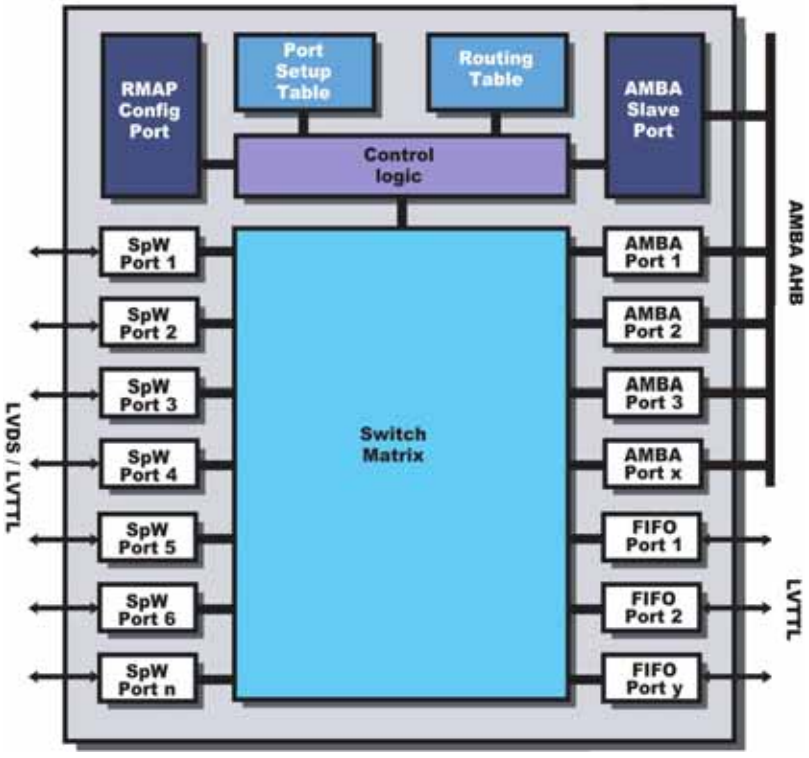


Figure 171. Block diagram

62.2 Operation

The router ports are interconnected using a non-blocking switch matrix which can connect any input port to any output port. Access to each output port is arbitrated using a round-robin arbitration scheme. A single routing-table is used for the whole router. Access to the table is also arbitrated using a round-robin scheme.

The ports consist of configuration port 0 and three different types of external ports: SpaceWire links, FIFO interfaces and AMBA interfaces. Up to 31 external ports are supported and each can be individually configured to one of the three supported types.

All the ports regardless of their type have the same interface to the switch matrix and behave in the same manner. The difference in behavior is on the external side of the port. The SpaceWire ports provide standard SpaceWire link interfaces using either on- or off-chip LVDS. The FIFO interfaces store characters in two FIFOs which are accessed using 9-bit wide data paths with read/write signals. Lastly the AMBA ports transfer characters from and to an AHB bus using DMA. The four different port types are described in further detail in sections 62.3, 62.4, 62.5 and 62.6.

62.2.1 Endianness

The core is designed for big-endian systems.

62.2.2 Port numbering

The ports are numbered in the following order: configuration port, SpW ports, AMBA ports, FIFO ports. The configuration port is always present and has number 0. If SpW ports are present in the router they are numbered starting from number 1. If AMBA ports are present they are numbered starting from the last SpW ports. If no SpW ports are present the AMBA ports start at number 1. Lastly, the FIFO ports are numbered starting after the last AMBA port, SpW port or at number 1 depending on if AMBA ports and SpW ports are present respectively.

For example if 7 SpW ports and 4 FIFO ports are included in the router they will have port numbers 1-7 and 8-11. If 16 SpW ports, 2 AMBA ports and 7 FIFO ports are included they have port numbers 1-16, 17-18 and 19-25 respectively.

62.2.3 Routing table

A single routing table is provided. The access to this routing table is arbitrated using a round-robin arbiter with each port being of equal priority. The operation is pipelined and one lookup can be done each cycle. This way the maximum latency is equal to the number of ports in the router minus one. The impact on throughput should be negligible provided that packets are not incoming at the same time. The probability for this is higher when the traffic only consist of very small packets sent continuously (the average size being about the same as the number of ports). This should be a very uncommon case. Latency is still bounded and probably negligible in comparison to other latencies in most systems. The benefit is a reduced area enabling the router to be implemented with a higher number of ports on many FPGA technologies.

Since the latency for the lookup is very small and deterministic there is not much to gain by having configurable priorities for this. Priorities are instead used for arbitrating packets contending for an output port as described in the next section.

The routing table and all the configuration registers are configured through an RMAP target or an optional AHB slave interface which use the same routing table as the logic handling packet traffic. They do not introduce any extra latency because they have lower priority than the packet traffic and thus are only allowed access on cycles when no lookup is needed for packets. This can slow down configuration accesses but they are probably mostly done before packet traffic starts and very seldom afterwards.

Logical addresses have a routing table entry containing a priority bit, header deletion enable bit and a entry enable bit. The routing table entry is enabled by writing a 1 to the enable bit. It can be disabled again by writing a 0. The contents of the routing table is undetermined after reset and should not be read. When a routing table entry is disabled, packets with a destination address corresponding to that entry will be discarded and the invalid address error bit asserted.

Before the routing table entry is enabled the corresponding port setup register must be initialized. The port setup register should be written with ones to one or more bits to enable packets to be transmitted

on the ports corresponding to the bit numbers. See sections 62.2.5 and 62.2.6 for more details on how to use the port setup register. If the port setup register is not initialized but the routing table entry is enabled packets with that logical address will be discarded and the invalid address error bit asserted.

The mechanism is the same for path addresses except that they do not have a routing table entry and header deletion is always enabled. Packets will be routed to the output corresponding to the path address in the packet even if the port setup register has not been initialized. For group adaptive routing and packet distribution to be used the port setup register must be initialized also for path addresses.

The routing table entries are also marked as invalid before they have been written the first time. When the entries are invalid, packets with the corresponding logical address will be discarded and an invalid address error bit asserted.

62.2.4 Output port arbitration

Each output port is arbitrated individually using two priority levels with round-robin at each level. Each path or logical address can be configured to be high or low priority. In this case the delays can be very long (compared to when arbiting for access to the routing table) before the next arbitration because packets can be very large and the speed of the data consumer and the link itself cannot be known. In this case priority assignments can have a large impact on the amount of bandwidth a source port can use on a destination port.

The priority for path addresses is set in the port's control register with the port number corresponding to the path address. For logical addresses the priority is set in the routing table entry.

62.2.5 Group adaptive routing

Group adaptive routing is used to enable a packet to be transmitted on several different paths. For example a packet with address 45 can be enabled to be transmitted on port 1 and 2. If port 1 is busy when a packet with address 45 arrives it is transmitted on port 2 instead if not busy.

Group adaptive routing is used if bit 0 in the port setup register for the corresponding path or logical address is 0. Each bit in the register corresponds to the port with the same number as the bit index. So if bit 5 is set to 1 at address offset 0x80 it means that incoming packets with logical address 32 can be transmitted on port 5. If only one bit is set for an address all packets with that address will be transmitted on that port. If one or more bits are set the group adaptive function is used and the packet is transmitted on the first available port with a bit set to 1 starting from the lowest number. A port being available means that no other packet transmission is active at the moment and also for SpaceWire links that the link is in run-state. For path addresses the bit corresponding to the path address will always be set. This is done as specified in the standard which requires a packet with a path address to be transmitted on the port with the same number as the address. The standard does not mention what should happen when group adaptive routing is used for path addresses but in this router the bit corresponding to the port number of the path address is always set so that the packet *can* be transmitted on that port also when group adaptive routing is used.

For logical addresses the corresponding routing table entry and port setup register must be valid for the packet to be routed (otherwise it is discarded). There is no default port as with path addresses so at least one bit in the port setup register must be 1 for the packet to be routed otherwise it is discarded.

62.2.6 Packet distribution

Packet distribution can be used to implement multicast and broadcast addresses. Packets with logical address 50 can for example be configured to be transmitted on ports 1, 2 and 3 while address 51 can be configured to be transmitted on all ports (broadcast).

When packet distribution is enabled the group adaptive routing register is used to determine the ports that a packet should be transmitted on. Packet distribution is enabled for a path or logical address by setting bit 0 in the corresponding port setup register to 1. The packet will be transmitted on all the ports with a bit set to 1 in the register. This means that if one of the ports enabled for packet distribu-

tion is busy the router will wait for it to become free before transmitting on any of the ports. Due to the wormhole routing implementation the slowest link will determine the speed at which a packet is transmitted on all the ports.

When packet distribution is used with path addresses the port with the same number as the address will always be enabled (as for group adaptive routing).

62.2.7 Port disable

The disable port bit in the port's control register can be used to disable a port for data traffic. It will behave just like if the physical port was not existing. Packets transmitted to it will be spilt and the invalid address bit on the source port is set. Packets received to the port will be silently discarded, no status bits are set.

All ports except the configuration port (0) and port 1 can be disabled to prevent the situation of all ports being locked out from happening.

62.2.8 Timers

Timer functionality can be optionally implemented by setting the timerbits VHDL generic to a non-zero value. Timers are individually enabled for each port by writing the timer enable bit in the port control register. When timers are enabled during packet transmission on a port the timer is reset each time a character is transmitted. If the timer expires the packet will be discarded and an EEP is inserted on all the ports to which the packet was transmitted (can be more than one if packet distribution was used). It does not matter if it is the output port or source port which is stalling. The blocking situation is always detected at the source port which handles the spilling. It also does not matter if the stall is caused by the link being stopped or lack of credits, the discard mechanism is always the same. When the timers are not implemented or disabled the source and destination ports will always block until the blocking situation is resolved.

The timers use a global prescaler and an individual timer per port. Both the prescaler and the individual timer tick rate can be configured through the configuration port.

In group adaptive routing mode the packet will be spilt if no characters have been transmitted for the timeout period after being assigned to a port. For packet distribution a packet will be spilt if no character has been transmitted for the timeout period after being assigned to all the ports. This means that it is enough for one port to stall for the packet to timeout and be spilt.

The behavior described above also means that the timeout is handled in the same way regardless of the port type (SpW, FIFO or AMBA).

If a destination port is disabled it behaves as if it is not existing and will not be used thus being spilt immediately. Timers are not applicable in that case. For group adaptive routing and packet distribution disabled ports are also masked before transmission starts and will not affect timers.

Details for the different scenarios will be listed in the remaining sub-sections.

62.2.8.1 Timers not present in the implementation or disabled

If timers are not available or disabled packets will always wait indefinitely regardless of stall reason. In the case that timers are present but are enabled on some ports and disabled on others it is always the source port that determines whether the timer will be active or not. This means that if a packet arrives at port 2 which has its timer enabled and it is routed to port 4 which has timers disabled a timer will be active for that packet routing and transmission. The same applies for group adaptive routing and packet distribution.

62.2.8.2 Timer enabled and output port not in run state

The timer is started when the packet arrives and if the link has not entered run-state until the timer expires the packet will be spilt. No EEP will be written to the destination port in this case. If the link

start on request feature has been enabled the router will try to start the link but still only waits for the timeout period for the link to start.

62.2.8.3 Timer enabled and output port in run state but busy with other transmission

The packet will wait indefinitely until the destination port becomes free. In the case that the destination port is stalled the port currently sourcing the packet for it has to have its timer enabled and spill the packet before the new port can be allocated for it. If the port stalls again the new port will also spill its packet after the timeout period. In this case and EEP will be written to the destination port since the transmission of the packet had started.

62.2.8.4 Timer enabled and group adaptive routing is enabled, ports not running

The timer is started when the packet arrives and if no port has been allocated until the timer expires the packet will be spilt. If link start on request is enabled the router will try to start all the links.

62.2.8.5 Timer enabled and group adaptive routing enabled, ports running but busy

The packet will wait until one port becomes free and then start transmitting. The timer is not started while waiting for busy ports.

62.2.8.6 Timer enabled and packet distribution enabled, ports not running

If at least one of the destination ports is not running the timer is started and the packet will be discarded if all the ports are not running when the timer expires.

62.2.8.7 Timer enabled and packet distribution enabled, ports running but busy

If at least one port is busy but all are running when packet distribution is enabled the packet will wait indefinitely. When the transmission has started the timer is restarted each time a character is transmitted and if the timer expires the remaining part of the packet is spilt and an EEP written to all the destination ports.

62.2.8.8 Timer functionality when accessing the configuration port

Timers work in the same way when accessing the configuration port as for the other ports. When the command is being received by the RMAP target the timer on the source port will trigger if the source of the command is too slow, spill the remaining part of the packet and insert an EEP to the configuration port. The RMAP target will always be able to receive the characters quick enough. If the source is too slow when the reply is sent the configuration port's timer will trigger and the remaining part of the packet is spilled and an EEP is inserted. This is to prevent the configuration port from being locked up by a malfunctioning source port.

62.2.9 On-chip memories

The router can have several memories on-chip. They are usually selected from technology specific RAM blocks but generic models can also be used which either make the synthesis tool infer the memories or use registers instead.

There are two memory blocks in the routing table, one for the port setup registers and one for the routing table. The port setup memory bit width is equal to the number of ports including the configuration port with depth 256. The routing table is 256 locations deep and 2 bits wide.

Each port excluding the configuration port also have FIFO memories. The SpaceWire ports have one FIFO per direction (rx, tx) which are 9-wide. The depth is controlled with the fifosize VHDL generic. The FIFO ports have the exact same FIFO configuration as the SpaceWire ports controlled by the same generic.

The AMBA ports have one 9-bit wide receiver FIFO controlled by the fifosize generic and two 32-bit wide AHB FIFOs. The depth of the latter two is controlled with the fifosize2 generic (see the AMBA port section for more information).

All of the memories are instantiated using either the syncram_2p of syncram_2pft components from GRLIB (see the syncram_2p section in the GRIP manual for more information) depending on the value of the ft generic. If ft is set to 0 the syncram_2p is used and there is no fault-tolerance support. If ft is nonzero the syncram_2pft component is chosen and there are two variants of fault-tolerance depending on the value. Setting ft=1 selects parity and ft=2 selects TMR.

Parity is used to protect the memories and up to four bits per word can be corrected and there is a signal indicating an uncorrectable error. TMR is used to protect the memories and a voter determines the correct result. No errors are detectable for TMR and thus the error signal is not used.

If a memory error occurs in the port setup table or the routing table the memory error (ME) bit in the router configuration/status register is set and remains set until cleared by the user. If a memory error is detected in any of the ports FIFO memories the memory error (ME) bit in the respective port status register is set and remains set until cleared by the user. The ME bits are only set for uncorrectable errors.

When an uncorrectable error is detected in the port setup or routing table when a packet is being routed it will be discarded. Unocrrectable errors in the FIFO memories are not handled since they only affect the contents of the routed packet not the operation of the router itself. These type of errors should be caught by CRC checks if used in the packet.

The ME bit for the ports is only usable for detecting errors and statistics since there is no need to correct the error manually since the packet has already been routed when it is detected. The ME indication for the routing table and port setup registers can be used for starting a scrubbing operation if detected. There is also an option of having automatic scrubbing (see section 62.2.9.1)

If one or more of the memory error bits described above are set the signal ro.merror will be asserted.

62.2.9.1 Autoscrub

An autoscrubbing feature can be optionally enabled using the autoscrub VHDL generic.

With autoscrubbing the routing table and port setup registers will be periodically read and rewritten. This is done to prevent buildup of SEUs to cause an uncorrectable error in the memories. It will run in the background and has no impact on routing table lookup for traffic but can delay configuration accesses with two cycles.

The scrubber starts at address 0 and simultaneously writes one location in the port setup memory and the routing table memory. It then waits for a timeout period until it writes the next word. Eventually the last location is reached and the process starts over from address 0.

The period between each word refresh is approximately 2^{26} core clock cycles. The scrubber uses a free slot when data traffic does not need to perform a table lookup to read and write the memories which causes a small undeterminism in the period.

62.2.10 Plug and play support

The configuration port optionally also supports the SpaceWire Plug and Play protocol draft A issue 2.1 (enabled with a VHDL generic). Currently the complete protocol is not supported but only the device identification and network management services. These services are enough to identify the router, the number of ports etc and once identified the user can access all the features the other two services provide using the registers accessible through the RMAP target. The level of support will change in later versions of the core. Since the protocol has not been standardized yet it should only be used for testing purposes.

The PnP protocol uses standard RMAP packets but with protocol ID 2 instead of 1. The supported commands and the address space is defined in the SpW PnP specification.

62.2.11 System time-distribution

The router contains a global time-counter register which handles system time-distribution. All the different port types support time-code transmission. Incoming time-codes on the ports are checked against the time-counter which is then updated. If time-code was determined to have a count value one more modulo 64 than the previous value then a tick is generated and the time-code is forwarded to all the other ports. The time-codes are also forwarded to the FIFO and AMBA ports where they appear on their respective external interfaces. Time-codes can also be transmitted from the FIFO and AMBA ports. In that case they are also compared to the time-counter and propagated to the other ports if valid.

The current router master time-counter and control flag values can be read through the configuration port (see the time-code register in section 62.8).

In default mode the router does not check the control flags so time-codes will be accepted regardless of their value. If the TF bit in the router configuration/status register is set to 1 time-code control flag filtering is enabled and the time-codes are required to have the control flags set to “00” to be accepted, otherwise they are dropped when received.

After reset all the ports are enabled to receive and transmit time-codes. The TE bit in a port’s control register can be set to 0 to disable time-code transmission and reception on that port.

Time-code transfers can also be disabled globally using a signal (ri.timecodeen).

62.2.12 Invalid address error

An invalid address error occurs when a port receives a packet with an destination address that belongs to one or more of the three following groups:

1. Destination address is a path address corresponding to a non-existing port number. For example if the router only has 8 ports and a packet has destination address 15 this error will occur. If a router has 31 ports (32 including the configuration port) this error cannot occur.

2. Destination address is a logical address corresponding to a routing table entry which has not been configured. The routing table entries start at address 0x480.

3. Destination address is a logical address corresponding to a port setup register which has not been configured. The port setup registers start at address 0x80 for logical addresses.

4. The destination port determined either through physical or logical address has the disable (DI) bit set in the port control register.

62.2.13 Packet counters

Counters for characters and packets can be optionally enabled using the charcntbits and pktcntbits VHDL generics respectively.

Each port except port 0 has a separate character counter for incoming and outgoing characters. Only SpaceWire data characters are counted (not EOP, EEP). The counters saturate at the maximum value and can be cleared through register access. The counter is accessed through the configuration port. Characters deleted due to header deletion are counted on the incoming port but not on the outgoing.

Each port also has separate incoming and outgoing packet counters. Each EOP/EEP preceded by at least one data character is counted as one packet.

62.2.14 Global configuration features

62.2.14.1 Self addressing

Normally the ports are allowed to address themselves i.e. a packet is received on a port with a destination address configured to be transmitted on the same port (which the packet was received on). This can be disabled by setting the self addressing enable (SA) bit in the router configuration/status register to 0. The reset value of this bit is set using a signal (ri.selfaddren signal).

This also applies to group adaptive routing and packet distribution. When group adaptive routing is enabled for an address a packet with that destination address will be spilt due to self-addressing only if the packet is actually routed to the source port. That is if ports 1 and 2 are enabled for address 1 and a packet with address 1 arrives and it is routed to port 2 the transfer will be performed normally. If it is routed to port 1 and self-addressing is disabled it will be discarded.

For packet distribution the packet will always be discarded if the source port is included in the list of destination ports since the packet will be sent to all destinations.

62.2.14.2 Link start on request

Ports can be configured to start automatically when a packet is waiting to be transmitted on it. This is done by setting the LS bit in the router configuration/status register to 1. If the port link is disabled it will override the start feature and the link will not start. The reset value of this bit is set using a signal (ri.linkstartreq signal). This feature is only applicable for SpaceWire ports.

If the linkstart bit for the port is set the setting for the link start on request bit will have no effect. The link will continue to be started until a '0' is written to the linkstart bit of the port or if the auto disconnect feature is enabled (see next section).

62.2.14.3 Auto disconnect

If the link was started by the link start feature the auto disconnect feature can be enabled to automatically stop the link if inactive during a timeout period. This will only be possible if the timer feature is available (timerbits VHDL generic is nonzero). The auto disconnect feature is enabled by setting the AD bit in the router configuration/status register. The reset value is set using a signal (ri.autodconnect signal). This feature is only applicable to SpaceWire ports.

The link will be disconnected under the following conditions. The link start on request feature is enabled and the link was not in run-state when the packet arrived at the output port. Then the link will be disconnected when the packet transmission has finished (output port free), the transmit FIFO is empty, no receive operation is active and the timeout period has expired since the last of the requirements for disconnect (the ones listed here) became true.

62.3 SpaceWire ports

When a port is configured as a SpaceWire link it consists of a SpaceWire codec with FIFO interfaces. This is the same SpaceWire codec core (GRSPW_CODEC) provided in GRLIB as a separate core. It is a very versatile core providing several external interface types. The receiver can be configured as self-clocking (XOR gate based), SDR-, DDR sampling or with an interface to an Cobham SpW transceiver (UT200SpWPHY01). The transmitter can also be configured with SDR, DDR or SpWPHY outputs. Both internal and external LVDS transceivers are supported. All the configurable parameters for the link are accessible through the router configuration port (see the register section for the configurable parameters). For more detailed information about the codec itself see the SpaceWire codec section in the GRLIB IP library manual.

62.3.1 Redundant ports

Redundant ports can be optionally enabled for SpaceWire ports. The redundant port is part of the codec implementation and provides an extra set of SpaceWire transmit and receive signals. Only one of the links can be active at each time and data transferred on that router port will be received and transmitted on the active link. The active link can be dynamically configured to be forced or determined automatically based on the current activity of primary and redunant port links.

62.3.2 Setting link-rate

The router's Initialization divisor register determines the link-rate during initialization (all states up to and including the connecting-state). The register is also used to calculate the link interface FSM timeouts (6.4 us and 12.8 us, as defined in the SpaceWire standard). The register's ID field should always be set so that a 10 Mbit/s link-rate is achieved during initialization. In that case the timeout values will also be calculated correctly.

To achieve a 10 Mbit/s link-rate, the ID field should be set according to the following formulas:

With single data rate (SDR) outputs:

ID = (<frequency in MHz of TXCLK> / 10) - 1

With double data rate (DDR) outputs, or when connected to Cobham SpaceWire transceiver:

ID = (2 x <frequency in MHz of TXCLK> / 10) - 1

The link-rate in run-state is controlled with the run-state divisor, which is set through the RD field of each port's Port control register. The link-rate in run-state is calculated according to the following formulas:

With SDR outputs:

<link-rate in Mbits/s> = <frequency in MHz of TXCLK> / (RD+1)

With DDR outputs / Cobham SpaceWire transceiver:

<link-rate in Mbits/s> = 2 x <frequency in MHz of TXCLK> / (RD+1)

The value of the RD field only affects the link-rate in run-state, and does not affect the 6.4 us or 12.8 us timeouts values.

Note that when using DDR ouputs, or when connected to Cobham SpaceWire transceiver, there is a limitation in the usable clock divisor values. All even values (except 0) will result in the same bitrate as the one higher odd number.

An example of clock divisor and resulting link-rate, with a TXCLK frequency of 50 MHz, is shown in the table 1015.

*Table 1015.*SpaceWire link-rate example with 50 MHz TXCLK

Clock divisor value	Link-rate in Mbit/s	
	SDR outputs	DDR outputs / Cobham SpaceWire transceiver
0	50	100
1	25	50
2	16.67	25
3	12.5	25
4	10	16.67
5	8.33	16.67
6	7.14	12.5
7	6.25	12.5
8	5.56	10
9	5	10

62.4 FIFO ports

A port configured as a FIFO port contains one FIFO in each direction to/from the switch matrix. The fifosize can be configured to 8, 16, 32 and 64 using a VHDL generic (note that the same generic is used for the fifosizes in the SpaceWire links and the AHB interfaces).

62.4.1 Transmitter

The transmitter FIFO interface consists of the following signals: txfull, txafull, txwrite, txchar, txcharcnt. Figure 172 illustrates the write operation. Note that txfull would only be asserted as illustrated in the figure when txcharcnt is 4 if the FIFO size is 4 (which is not the case typically).

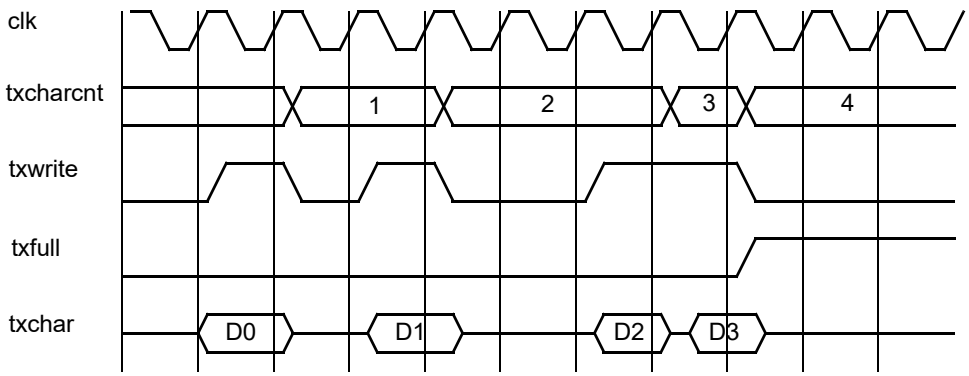


Figure 172. Transmitter FIFO interface write cycle.

Txwrite is the write signal and each time when asserted on the rising edge of the clock the value on the txchar signal will be written into the transmitter FIFO if it is not full. If it is full the character will be dropped. Txcharcnt indicates the number of characters currently in the FIFO. Txfull is asserted when the FIFO is full and txafull is asserted when the FIFO is almost full. The almost full signal is

configurable through the almostsize VHDL generic and will be asserted when the FIFO contains a number of characters more than or equal to fifosize-almostsize.

The transmitter FIFO can be reset through the port's control register using the TF bit.

62.4.2 Receiver

The receiver FIFO interface consists of the following signals: rxread, rxchar, rxcharav and rxaempty. Figure 173 illustrates the read operation. Note that rxcharav would only be deasserted as illustrated in the figure if the FIFO contained 4 characters.

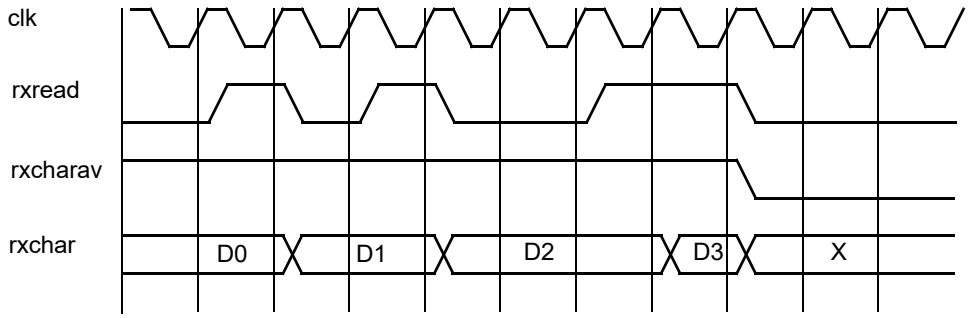


Figure 173. Receiver FIFO interface read cycle.

Each time rxread is asserted on the rising edge of the clock a new character will be available on the rxchar output the next cycle if available. If the FIFO is empty the value is undefined. Rxcharav is asserted when the FIFO contains at least one character. Rxaempty is asserted when the FIFO is almost empty and is defined as when the FIFO contains a number of characters less than or equal to the almostsize VHDL generic.

The receiver FIFO can be reset using the RF bit in the port's control register.

62.4.3 Time-code transmit

The time-code transmit interface consists of the following signals: tickin, timein. Figure 174 illustrates the tickin operation.

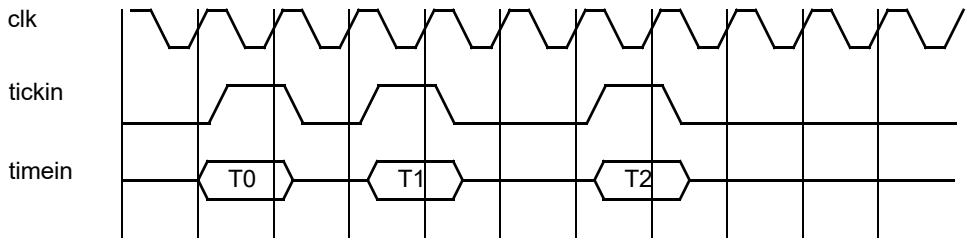


Figure 174. Time interface tickin operation.

62.4.4 Time-code receive

The time-code receive interface consists of the following signals: tickout, timeout. Figure 175 illustrates the tickout operation.

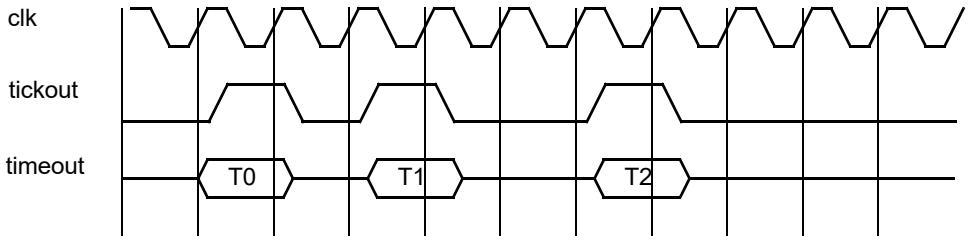


Figure 175. Time interface tickout operation.

The clock that all the interface signals are synchronized to is the same as the core clock (the clock that everything except the SpaceWire links' transmitters and receivers are running on). It can run on any frequency but to support the maximum throughput it has to be at least one eighth of the maximum link bitrate.

62.4.5 Bridge mode

The FIFO ports normally operate in standard mode which has been described so far in this section. But they can also be set in bridge mode through the bridge enable (BE) bit in the port's control register. The reset value of this signal is set through an input signal so this mode can be enabled per default after reset.

In bridge mode two FIFO ports can be connected together with automatic packet and time-code transfer without any glue logic. Table 1016 shows how the signals should be mapped. Rxaempty and txafull are unused in this mode.

*Table 1016.*Signal mappings of FIFO port in bridge mode.

Port 0	Port 1
rxchar	txchar
rxread	txfull
txwrite	rxcharav
txchar	rxchar
txfull	rxread
rxcharav	txwrite
tickin	tickout
timein	timeout
tickout	tickin
timeout	timein

62.5 AMBA ports

The AMBA ports consists of what is basically a GRSPW2 core (see the GRSPW2 section in the GRLIB IP library manual) with the SpaceWire codec removed. The same drivers that are provided for the GRSPW2 core can be used for each AMBA port on the router. Only an additional driver is needed which handles the setup of all the registers on the configuration port. In this way a router can be connected to a LEON3 system and also provide the functionality of one or more GRSPW2 links. It is also easy to provide bridging to other buses supported in GRLIB such as PCI, 1553, CAN, Ethernet etc.

62.5.1 Overview

The Router AMBA port is configured through a set of registers accessed through an APB interface. Data is transferred through DMA channels using an AHB master interface. The number of DMA channels is configurable from one to four. Only byte addressed 32-bit big-endian AHB buses are supported.

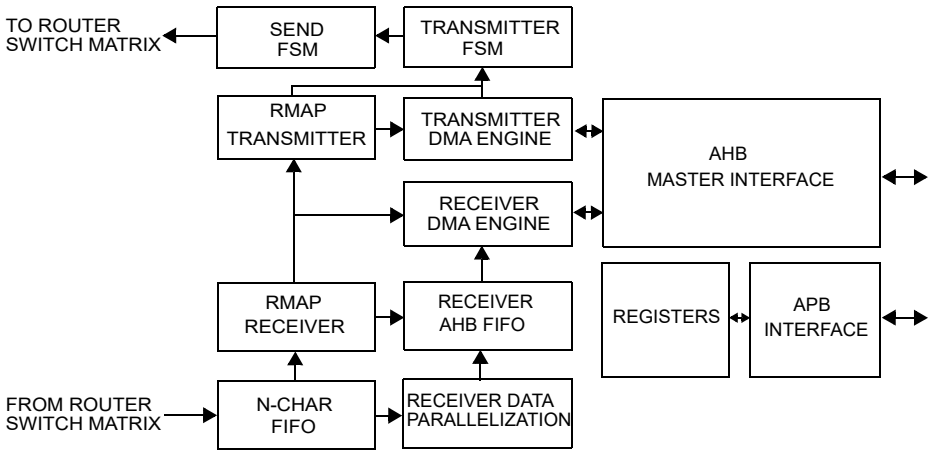


Figure 176. Block diagram of the Router DMA port

62.5.2 Operation

The main sub-blocks of the router AHB interfaces are the DMA engines, the RMAP target and the AMBA interface. A block diagram of the internal structure can be found in figure 176.

The AMBA interface is divided into the AHB master interface and the APB interface. The DMA engines have FIFO interfaces to the router switch matrix. These FIFOs are used to transfer N-Chars between the AMBA bus and the other ports in the router.

The RMAP target is an optional part of the DMA port which can be enabled with a VHDL generic. The RMAP target handles incoming packets which are determined to be RMAP commands instead of the receiver DMA engine. The RMAP command is decoded and if it is valid, the operation is performed on the AHB bus. If a reply was requested it is automatically transmitted back to the source by the RMAP transmitter.

The core is controlled by writing to a set of user registers through the APB interface and a set of signals. The different sub-modules are discussed in further detail in later sections.

62.5.2.1 Protocol support

The AMBA port only accepts packets with a valid destination address in the first received byte. Packets with address mismatch will be silently discarded (except in promiscuous mode which is covered in section 62.5.3.10).

The second byte is sometimes interpreted as a protocol ID a described hereafter. The RMAP protocol (ID=0x1) is the only protocol handled separately in hardware while other packets are stored to a DMA channel. If the RMAP target is present and enabled all RMAP commands will be processed, executed and replied automatically in hardware. Otherwise RMAP commands are stored to a DMA channel in the same way as other packets. RMAP replies are always stored to a DMA channel. More information on the RMAP protocol support is found in section 62.5.5 (note that this RMAP target is different from the one in the configuration port). When the RMAP target is not present or disabled, there is no need to include a protocol ID in the packets and the data can start immediately after the address.

All packets arriving with the extended protocol ID (0x00) are stored to a DMA channel. This means that the hardware RMAP target will not work if the incoming RMAP packets use the extended protocol ID. Note also that packets with the reserved extended protocol identifier (ID = 0x000000) are not ignored by the AMBA port. It is up to the client receiving the packets to ignore them.

When transmitting packets, the address and protocol-ID fields must be included in the buffers from where data is fetched. They are *not* automatically added by the AMBA port DMA engine.

Figure 177 shows the packet types accepted by the port. The port also allows reception and transmission with extended protocol identifiers but without support for RMAP CRC calculations and the RMAP target.

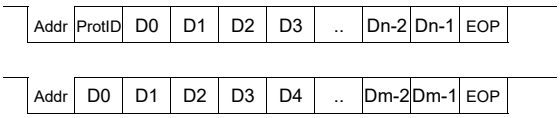


Figure 177. The SpaceWire packet types supported by the port.

62.5.2.2 Time interface

The time interface is used for sending Time-codes over the SpaceWire network and consists of a time-counter register, time-ctrl register, tick-in signal, tick-out signal, tick-in register field and a tick-out register field. There are also two control register bits which enable the time receiver and transmitter respectively.

Each Time-code sent from the port is a concatenation of the time-ctrl and the time-counter register. There is a timetxen bit which is used to enable Time-code transmissions. It is not possible to send time-codes if this bit is zero.

Received Time-codes are stored to the same time-ctrl and time-counter registers which are used for transmission. The timerxen bit in the control register is used for enabling time-code reception. No time-codes will be received if this bit is zero.

The two enable bits are used for ensuring that a node will not (accidentally) both transmit and receive time-codes which violates the SpaceWire standard. It also ensures that a master sending time-codes on a network will not have its time-counter overwritten if another (faulty) node starts sending time-codes.

The time-counter register is set to 0 after reset and is incremented each time the tick-in signal is asserted for one clock-period and the timetxen bit is set. This also causes the new value to be sent to the router (which will propagate the time-code to the other ports if valid just as if it was transmitted on a normal SpW link). Tick-in can be generated either by writing a one to the register field or by asserting the tick-in signal. A Tick-in should not be generated too often since if the time-code after the previous Tick-in has not been sent the register will not be incremented and no new value will be sent. The tick-in field is automatically cleared when the value has been sent and thus no new ticks should be generated until this field is zero. If the tick-in signal is used there should be at least 4 system-clock plus 25 transmit-clock cycles between each assertion.

A tick-out is generated each time a valid time-code is received and the timerxen bit is set. When the tick-out is generated the tick-out signal will be asserted one clock-cycle and the tick-out register field is asserted until it is cleared by writing a one to it.

The current time counter value can be read from the time register. It is updated each time a Time-code is received and the timerxen bit is set. The same register is used for transmissions and can also be written directly from the APB interface.

The control bits of the Time-code are stored to the time-ctrl register when a Time-code is received whose time-count is one more than the nodes current time-counter register. The time-ctrl register can be read through the APB interface. The same register is used during time-code transmissions.

It is possible to have both the time-transmission and reception functions enabled at the same time.

62.5.3 Receiver DMA channels

The receiver DMA engine handles reception of data from the SpaceWire network to different DMA channels.

62.5.3.1 Address comparison and channel selection

Packets are received to different channels based on the address and whether a channel is enabled or not. When the receiver N-Char FIFO contains one or more characters, N-Chars are read by the receiver DMA engine. The first character is interpreted as the logical address and is compared with the addresses of each channel starting from 0. The packet will be stored to the first channel with an matching address. The complete packet including address and protocol ID but excluding EOP/EEP is stored to the memory address pointed to by the descriptors (explained later in this section) of the channel.

Each SpaceWire address register has a corresponding mask register. Only bits at an index containing a zero in the corresponding mask register are compared. This way a DMA channel can accept a range of addresses. There is a default address register which is used for address checking in all implemented DMA channels that do not have separate addressing enabled and for RMAP commands in the RMAP target. With separate addressing enabled the DMA channels' own address/mask register pair is used instead.

If an RMAP command is received it is only handled by the target if the default address register (including mask) matches the received address. Otherwise the packet will be stored to a DMA channel if one or more of them has a matching address. If the address does not match neither the default address nor one of the DMA channels' separate register, the packet is still handled by the RMAP target if enabled since it has to return the invalid address error code. The packet is only discarded (up to and including the next EOP/EEP) if an address match cannot be found and the RMAP target is disabled.

Packets, other than RMAP commands, that do not match neither the default address register nor the DMA channels' address register will be discarded. Figure 178 shows a flowchart of packet reception.

At least 2 non EOP/EEP N-Chars needs to be received for a packet to be stored to the DMA channel unless the promiscuous mode is enabled in which case 1 N-Char is enough. If it is an RMAP packet with hardware RMAP enabled 3 N-Chars are needed since the command byte determines where the packet is processed. Packets smaller than these sizes are discarded.

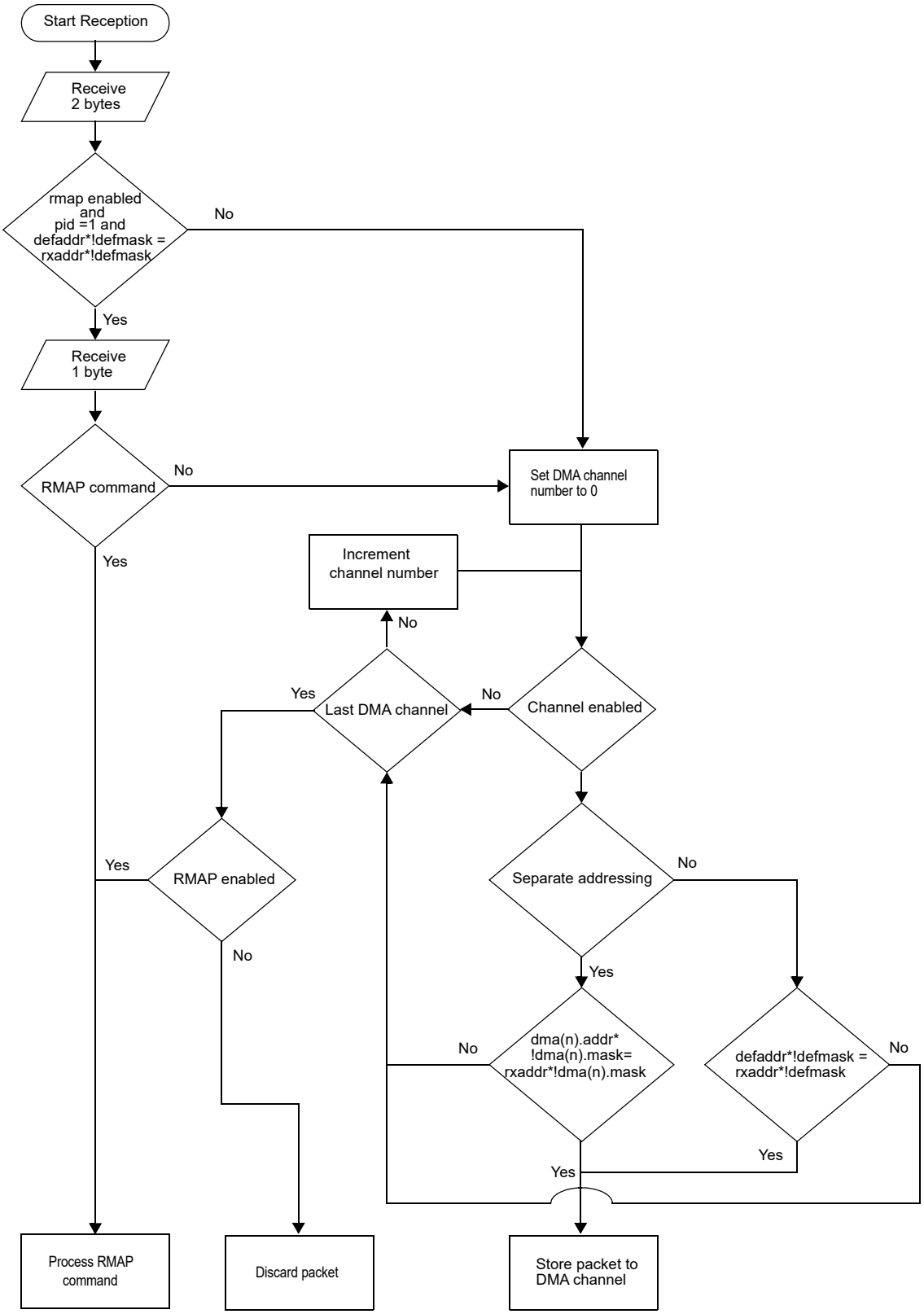


Figure 178. Flow chart of packet reception (promiscuous mode disabled).

62.5.3.2 Basic functionality of a channel

Reception is based on descriptors located in a consecutive area in memory that hold pointers to buffers where packets should be stored. When a packet arrives at the port the channel which should receive it is first determined as described in the previous section. A descriptor is then read from the channels' descriptor area and the packet is stored to the memory area pointed to by the descriptor. Lastly, status is stored to the same descriptor and increments the descriptor pointer to the next one. The following sections will describe DMA channel reception in more detail.

62.5.3.3 Setting up the port for reception

A few registers need to be initialized before reception to a channel can take place. The DMA channel has a maximum length register which sets the maximum packet size in bytes that can be received to this channel. Larger packets are truncated and the excessive part is spilled. If this happens an indication will be given in the status field of the descriptor. The minimum value for the receiver maximum length field is 4 and the value can only be incremented in steps of four bytes up to the maximum value 33554428. If the maximum length is set to zero the receiver will *not* function correctly.

Either the default address register or the channel specific address register (the accompanying mask register must also be set) needs to be set to hold the address used by the channel. A control bit in the DMA channel control register determines whether the channel should use default address and mask registers for address comparison or the channel's own registers. Using the default register the same address range is accepted as for other channels with default addressing and the RMAP target while the separate address provides the channel its own range. If all channels use the default registers they will accept the same address range and the enabled channel with the lowest number will receive the packet.

Finally, the descriptor table and control register must be initialized. This will be described in the two following sections.

62.5.3.4 Setting up the descriptor table address

The port reads descriptors from an area in memory pointed to by the receiver descriptor table address register. The register consists of a base address and a descriptor selector. The base address points to the beginning of the area and must start on a 1024 bytes aligned address. It is also limited to be 1024 bytes in size which means the maximum number of descriptors is 128 since the descriptor size is 8 bytes.

The descriptor selector points to individual descriptors and is increased by 1 when a descriptor has been used. When the selector reaches the upper limit of the area it wraps to the beginning automatically. It can also be set to wrap at a specific descriptor before the upper limit by setting the wrap bit in the descriptor. The idea is that the selector should be initialized to 0 (start of the descriptor area) but it can also be written with another 8 bytes aligned value to start somewhere in the middle of the area. It will still wrap to the beginning of the area.

If one wants to use a new descriptor table the receiver enable bit has to be cleared first. When the rxactive bit for the channel is cleared it is safe to update the descriptor table register. When this is finished and descriptors are enabled the receiver enable bit can be set again.

62.5.3.5 Enabling descriptors

As mentioned earlier one or more descriptors must be enabled before reception can take place. Each descriptor is 8 byte in size and the layout can be found in the tables below. The descriptors should be written to the memory area pointed to by the receiver descriptor table address register. When new descriptors are added they must always be placed after the previous one written to the area. Otherwise they will not be noticed.

A descriptor is enabled by setting the address pointer to point at a location where data can be stored and then setting the enable bit. The WR bit can be set to cause the selector to be set to zero when

reception has finished to this descriptor. IE should be set if an interrupt is wanted when the reception has finished. The DMA control register interrupt enable bit must also be set for an interrupt to be generated. The descriptor packet address should be word aligned. All accesses on the bus are word accesses so complete words will always be overwritten regardless of whether all 32-bit contain received data. Also if the packet does not end on a word boundary the complete word containing the last data byte will be overwritten. If the rxunaligned or rmap VHDL generic is set to 1 this restriction is removed and any number of bytes can be received to any packet address without excessive bytes being overwritten.

*Table 1017.*RXDMA receive descriptor word 0 (address offset 0x0)

31	30	29	28	27	26	25	24	0
TR	DC	HC	EP	IE	WR	EN	PACKETLENGTH	

31	Truncated (TR) - Packet was truncated due to maximum length violation.
30	Data CRC (DC) - 1 if a CRC error was detected for the data and 0 otherwise.
29	Header CRC (HC) - 1 if a CRC error was detected for the header and 0 otherwise.
28	EEP termination (EP) - This packet ended with an Error End of Packet character.
27	Interrupt enable (IE) - If set, an interrupt will be generated when a packet has been received if the receive interrupt enable bit in the DMA channel control register is set.
26	Wrap (WR) - If set, the next descriptor used by the GRSPW will be the first one in the descriptor table (at the base address). Otherwise the descriptor pointer will be increased with 0x8 to use the descriptor at the next higher memory location. The descriptor table is limited to 1 kbytes in size and the pointer will be automatically wrap back to the base address when it reaches the 1 kbytes boundary.
25	Enable (EN) - Set to one to activate this descriptor. This means that the descriptor contains valid control values and the memory area pointed to by the packet address field can be used to store a packet.
24: 0	Packet length (PACKETLENGTH) - The number of bytes received to this buffer. Only valid after EN has been set to 0 by the GRSPW.

*Table 1018.*RXDMA receive descriptor word 1 (address offset 0x4)

31	0
PACKETADDRESS	

31: 0	Packet address (PACKETADDRESS) - The address pointing at the buffer which will be used to store the received packet. If the rxunaligned and rmap VHDL generics are both set to zero only bit 31 to 2 are used.

62.5.3.6 Setting up the DMA control register

The final step to receive packets is to set the control register in the following steps: The receiver must be enabled by setting the rxen bit in the DMA control register (see section 62.8). This can be done anytime and before this bit is set nothing will happen. The rxdescav bit in the DMA control register is then set to indicate that there are new active descriptors. This must always be done after the descriptors have been enabled or the port might not notice the new descriptors. More descriptors can be activated when reception has already started by enabling the descriptors and writing the rxdescav bit. When these bits are set reception will start immediately when data is arriving.

62.5.3.7 The effect to the control bits during reception

When the receiver is disabled all packets going to the DMA-channel are discarded if the packet's address does not fall into the range of another DMA channel. If the receiver is enabled and the address falls into the accepted address range, the next state is entered where the rxdescav bit is checked. This bit indicates whether there are active descriptors or not and should be set by the external application using the DMA channel each time descriptors are enabled as mentioned above. If the rxdescav bit is '0' and the nospill bit is '0' the packets will be discarded. If nospill is one the grspw waits until rxdes-

cav is set and the characters are kept in the N-Char fifo during this time. If the fifo becomes full further N-char transmissions are inhibited by stopping the transmission of FCTs.

When rxdescav is set the next descriptor is read and if enabled the packet is received to the buffer. If the read descriptor is not enabled, rxdescav is set to '0' and the packet is spilled depending on the value of nospill.

The receiver can be disabled at any time and will stop packets from being received to this channel. If a packet is currently received when the receiver is disabled the reception will still be finished. The rxdescav bit can also be cleared at any time. It will not affect any ongoing receptions but no more descriptors will be read until it is set again. Rxdescav is also cleared by the port when it reads a disabled descriptor.

62.5.3.8 Status bits

When the reception of a packet is finished the enable bit in the current descriptor is set to zero. When enable is zero, the status bits are also valid and the number of received bytes is indicated in the length field. The DMA control register contains a status bit which is set each time a packet has been received. The port can also be made to generate an interrupt for this event.

RMAP CRC logic is included in the implementation if the rmapcrc or rmap VHDL generic set to 1. The RMAP CRC calculation is always active for all received packets and all bytes except the EOP/EEP are included. The packet is always assumed to be a RMAP packet and the length of the header is determined by checking byte 3 which should be the command field. The calculated CRC value is then checked when the header has been received (according to the calculated number of bytes) and if it is non-zero the HC bit is set indicating a header CRC error.

The CRC value is not set to zero after the header has been received, instead the calculation continues in the same way until the complete packet has been received. Then if the CRC value is non-zero the DC bit is set indicating a data CRC error. This means that the port can indicate a data CRC error even if the data field was correct when the header CRC was incorrect. However, the data should not be used when the header is corrupt and therefore the DC bit is unimportant in this case. When the header is not corrupted the CRC value will always be zero when the calculation continues with the data field and the behaviour will be as if the CRC calculation was restarted

If the received packet is not of RMAP type the header CRC error indication bit cannot be used. It is still possible to use the DC bit if the complete packet is covered by a CRC calculated using the RMAP CRC definition. This is because the port does not restart the calculation after the header has been received but instead calculates a complete CRC over the packet. Thus any packet format with one CRC at the end of the packet calculated according to RMAP standard can be checked using the DC bit.

If the packet is neither of RMAP type nor of the type above with RMAP CRC at the end, then both the HC and DC bits should be ignored.

62.5.3.9 Error handling

If an AHB error occurs during reception the current packet is spilled up to and including the next EEP/EOP and then the currently active channel is disabled and the receiver enters the idle state. A bit in the channels control/status register is set to indicate this condition.

62.5.3.10 Promiscuous mode

The port supports a promiscuous mode where all the data received is stored to the first DMA channel enabled regardless of the node address and possible early EOPs/EEPs. This means that all non-eop/eep N-Chars received will be stored to the DMA channel. The rxmaxlength register is still checked and packets exceeding this size will be truncated.

RMAP commands will still be handled by it when promiscuous mode is enabled if the rmapen bit is set. If it is cleared, RMAP commands will also be stored to a DMA channel.

62.5.4 Transmitter DMA channels

The transmitter DMA engine handles transmission of data from the DMA channels to the SpaceWire network. Each receive channel has a corresponding transmit channel which means there can be up to 4 transmit channels. It is however only necessary to use a separate transmit channel for each receive channel if there are also separate entities controlling the transmissions. The use of a single channel with multiple controlling entities would cause them to corrupt each other's transmissions. A single channel is more efficient and should be used when possible.

Multiple transmit channels with pending transmissions are arbitrated in a round-robin fashion.

62.5.4.1 Basic functionality of a channel

A transmit DMA channel reads data from the AHB bus and stores them in the transmitter FIFO for transmission on the SpaceWire network. Transmission is based on the same type of descriptors as for the receiver and the descriptor table has the same alignment and size restrictions. When there are new descriptors enabled the port reads them and transfer the amount data indicated.

62.5.4.2 Setting up the core for transmission

Four steps need to be performed before transmissions can be done with the port. First the link interface must be enabled and started by writing the appropriate value to the ctrl register. Then the address to the descriptor table needs to be written to the transmitter descriptor table address register and one or more descriptors must also be enabled in the table. Finally, the txen bit in the DMA control register is written with a one which triggers the transmission. These steps will be covered in more detail in the next sections.

62.5.4.3 Enabling descriptors

The descriptor table address register works in the same way as the receiver's corresponding register which was covered in section 62.5.3. The maximum size is 1024 bytes as for the receiver but since the descriptor size is 16 bytes the number of descriptors is 64.

To transmit packets one or more descriptors have to be initialized in memory which is done in the following way: The number of bytes to be transmitted and a pointer to the data has to be set. There are two different length and address fields in the transmit descriptors because there are separate pointers for header and data. If a length field is zero the corresponding part of a packet is skipped and if both are zero no packet is sent. The maximum header length is 255 bytes and the maximum data length is 16 Mbyte - 1. When the pointer and length fields have been set the enable bit should be set to enable the descriptor. This must always be done last. The other control bits must also be set before enabling the descriptor.

The transmit descriptors are 16 bytes in size so the maximum number in a single table is 64. The different fields of the descriptor together with the memory offsets are shown in the tables below.

The HC bit should be set if RMAP CRC should be calculated and inserted for the header field and correspondingly the DC bit should be set for the data field. This field is only used by the GRSPW when the CRC logic is available (*rmap* or *rmapcrc* VHDL generic set to 1). The header CRC will be calculated from the data fetched from the header pointer and the data CRC is generated from data fetched from the data pointer. The CRCs are appended after the corresponding fields. The NON-CRC bytes field is set to the number of bytes in the beginning of the header field that should not be included in the CRC calculation.

The CRCs are sent even if the corresponding length is zero, but when both lengths are zero no packet is sent not even an EOP.

62.5.4.4 Starting transmissions

When the descriptors have been initialized, the transmit enable bit in the DMA control register has to be set to tell the port to start transmitting. New descriptors can be activated in the table on the fly (while transmission is active). Each time a set of descriptors is added the transmit enable register bit should be set. This has to be done because each time the core encounters a disabled descriptor this register bit is set to 0.

*Table 1019.*TXDMA transmit descriptor word 0 (address offset 0x0)

31 18	17	16	15	14	13	12	11 8	7 0
RESERVED	DC	HC	RE	IE	WR	EN	NONCRCLEN	HEADERLEN

31: 18	RESERVED
17	Append data CRC (DC) - Append CRC calculated according to the RMAP specification after the data sent from the data pointer. The CRC covers all the bytes from this pointer. A null CRC will be sent if the length of the data field is zero.
16	Append header CRC (HC) - Append CRC calculated according to the RMAP specification after the data sent from the header pointer. The CRC covers all bytes from this pointer except a number of bytes in the beginning specified by the non-crc bytes field. The CRC will not be sent if the header length field is zero.
15	RESERVED
14	Interrupt enable (IE) - If set, an interrupt will be generated when the packet has been transmitted and the transmitter interrupt enable bit in the DMA control register is set.
13	Wrap (WR) - If set, the descriptor pointer will wrap and the next descriptor read will be the first one in the table (at the base address). Otherwise the pointer is increased with 0x10 to use the descriptor at the next higher memory location.
12	Enable (EN) - Enable transmitter descriptor. When all control fields (address, length, wrap and crc) are set, this bit should be set. While the bit is set the descriptor should not be touched since this might corrupt the transmission. The GRSPW clears this bit when the transmission has finished.
11: 8	Non-CRC bytes (NONCRCLEN)- Sets the number of bytes in the beginning of the header which should not be included in the CRC calculation. This is necessary when using path addressing since one or more bytes in the beginning of the packet might be discarded before the packet reaches its destination.
7: 0	Header length (HEADERLEN) - Header Length in bytes. If set to zero, the header is skipped.

*Table 1020.*TXDMA transmit descriptor word 1 (address offset 0x4)

31 0
HEADERADDRESS

31: 0	Header address (HEADERADDRESS) - Address from where the packet header is fetched. Does not need to be word aligned.

*Table 1021.*TXDMA transmit descriptor word 2 (address offset 0x8)

31 24	23 0
RESERVED	DATALEN

31: 24	RESERVED
23: 0	Data length (DATALEN) - Length of data part of packet. If set to zero, no data will be sent. If both data- and header-lengths are set to zero no packet will be sent.

*Table 1022.*TXDMA transmit descriptor word 3(address offset 0xC)

31	0
DATAADDRESS	

31: 0	Data address (DATAADDRESS) - Address from where data is read. Does not need to be word aligned.

62.5.4.5 The transmission process

When the txen bit is set the port starts reading descriptors immediately. The number of bytes indicated are read and transmitted. When a transmission has finished, status will be written to the first field of the descriptor and a packet sent bit is set in the DMA control register. If an interrupt was requested it will also be generated. Then a new descriptor is read and if enabled a new transmission starts, otherwise the transmit enable bit is cleared and nothing will happen until it is enabled again.

62.5.4.6 The descriptor table address register

The internal pointer which is used to keep the current position in the descriptor table can be read and written through the APB interface. This pointer is set to zero during reset and is incremented each time a descriptor is used. It wraps automatically when the 1024 bytes limit for the descriptor table is reached or it can be set to wrap earlier by setting a bit in the current descriptor.

The descriptor table register can be updated with a new table anytime when no transmission is active. No transmission is active if the transmit enable bit is zero and the complete table has been sent or if the table is aborted (explained below). If the table is aborted one has to wait until the transmit enable bit is zero before updating the table pointer.

62.5.4.7 Error handling

62.5.4.7.1Abort Tx

The DMA control register contains a bit called Abort TX which if set causes the current transmission to be aborted, the packet is truncated and an EEP is inserted. This is only useful if the packet needs to be aborted because of congestion on the SpaceWire network. If the congestion is on the AHB bus this will not help (This should not be a problem since AHB slaves should have a maximum of 16 wait-states). The aborted packet will have its LE bit set in the descriptor. The transmit enable register bit is also cleared and no new transmissions will be done until the transmitter is enabled again.

62.5.4.7.2AHB error

When an AHB error is encountered during transmission the currently active DMA channel is disabled and the transmitter goes to the idle mode. A bit in the DMA channel's control/status register is set to indicate this error condition and, if enabled, an interrupt will also be generated. Further error handling depends on what state the transmitter DMA engine was in when the AHB error occurred. If the descriptor was being read the packet transmission had not been started yet and no more actions need to be taken.

If the AHB error occurs during packet transmission the packet is truncated and an EEP is inserted. Lastly, if it occurs when status is written to the descriptor the packet has been successfully transmitted but the descriptor is not written and will continue to be enabled (this also means that no error bits are set in the descriptor for AHB errors).

The client using the channel has to correct the AHB error condition and enable the channel again. No more AHB transfers are done again from the same unit (receiver or transmitter) which was active during the AHB error until the error state is cleared and the unit is enabled again.

62.5.5 RMAP target

The Remote Memory Access Protocol (RMAP) is used to implement access to resources on the AHB bus via the SpaceWire Link. Some common operations are reading and writing to memory, registers and FIFOs. The port has an optional hardware RMAP target which is enabled with a VHDL generic. This section describes the target implementation.

62.5.5.1 Fundamentals of the protocol

RMAP is a protocol which is designed to provide remote access via a SpaceWire network to memory mapped resources on a SpaceWire node. It has been assigned protocol ID 0x01. It provides three operations write, read and read-modify-write. These operations are posted operations which means that a source does not wait for an acknowledge or reply. It also implies that any number of operations can be outstanding at any time and that no timeout mechanism is implemented in the protocol. Time-outs must be implemented in the user application which sends the commands. Data payloads of up to 16 Mb - 1 is supported in the protocol. A destination can be requested to send replies and to verify data before executing an operation. A complete description of the protocol is found in the RMAP standard.

62.5.5.2 Implementation

The port includes a target for RMAP commands which processes all incoming packets with protocol ID = 0x01, type field (bit 7 and 6 of the 3rd byte in the packet) equal to 01b and an address falling in the range set by the default address and mask register. When such a packet is detected it is not stored to the DMA channel, instead it is passed to the RMAP receiver.

The target implements all three commands defined in the standard with some restrictions. Support is only provided for 32-bit big-endian systems. This means that the first byte received is the msb in a word. The target will not receive RMAP packets using the extended protocol ID which are always dumped to the DMA channel.

The RMAP receiver processes commands. If they are correct and accepted the operation is performed on the AHB bus and a reply is formatted. If an acknowledge is requested the RMAP transmitter automatically send the reply. RMAP transmissions have priority over DMA channel transmissions.

There is a user accessible destination key register which is compared to destination key field in incoming packets. If there is a mismatch and a reply has been requested the error code in the reply is set to 3. Replies are sent if and only if the ack field is set to ‘1’.

When a failure occurs during a bus access the error code is set to 1 (General Error). There is predetermined order in which error-codes are set in the case of multiple errors in the core. It is shown in table 1040.

*Table 1023.*The order of error detection in case of multiple errors in the GRSPW. The error detected first has number 1.

Detection Order	Error Code	Error
1	12	Invalid destination logical address
2	2	Unused RMAP packet type or command code
3	3	Invalid destination key
4	9	Verify buffer overrun
5	11	RMW data length error
6	10	Authorization failure
7*	1	General Error (AHB errors during non-verified writes)
8	5/7	Early EOP / EEP (if early)
9	4	Invalid Data CRC
10	1	General Error (AHB errors during verified writes or RMW)
11	7	EEP
12	6	Too Much Data
*The AHB error is not guaranteed to be detected before Early EOP/EEP or Invalid Data CRC. For very long accesses the AHB error detection might be delayed causing the other two errors to appear first.		

Read accesses are performed on the fly, that is they are not stored in a temporary buffer before transmitting. This means that the error code 1 will never be seen in a read reply since the header has already been sent when the data is read. If the AHB error occurs the packet will be truncated and ended with an EEP.

Errors up to and including Invalid Data CRC (number 8) are checked before verified commands. The other errors do not prevent verified operations from being performed.

The details of the support for the different commands are now presented. All defined commands which are received but have an option set which is not supported in this specific implementation will not be executed and a possible reply is sent with error code 10.

62.5.5.3 Write commands

The write commands are divided into two subcategories when examining their capabilities: verified writes and non-verified writes. Verified writes have a length restriction of 4 bytes and the address must be aligned to the size. That is 1 byte writes can be done to any address, 2 bytes must be halfword aligned, 3 bytes are not allowed and 4 bytes writes must be word aligned. Since there will always be only on AHB operation performed for each RMAP verified write command the incrementing address bit can be set to any value.

Non-verified writes have no restrictions when the incrementing bit is set to 1. If it is set to 0 the number of bytes must be a multiple of 4 and the address word aligned. There is no guarantee how many words will be written when early EOP/EEP is detected for non-verified writes.

62.5.5.4 Read commands

Read commands are performed on the fly when the reply is sent. Thus if an AHB error occurs the packet will be truncated and ended with an EEP. There are no restrictions for incrementing reads but non-incrementing reads have the same alignment restrictions as non-verified writes. Note that the “Authorization failure” error code will be sent in the reply if a violation was detected even if the length field was zero. Also note that no data is sent in the reply if an error was detected i.e. if the status field is non-zero.

62.5.5.5 RMW commands

All read-modify-write sizes are supported except 6 which would have caused 3 B being read and written on the bus. The RMW bus accesses have the same restrictions as the verified writes. As in the verified write case, the incrementing bit can be set to any value since only one AHB bus operation will be performed for each RMW command. Cargo too large is detected after the bus accesses so this error will not prevent the operation from being performed. No data is sent in a reply if an error is detected i.e. the status field is non-zero.

62.5.5.6 Control

The RMAP target mostly runs in the background without any external intervention, but there are a few control possibilities.

There is an enable bit in the control register of the core which can be used to completely disable the RMAP target. When it is set to '0' no RMAP packets will be handled in hardware, instead they are all stored to the DMA channel.

There is a possibility that RMAP commands will not be performed in the order they arrive. This can happen if a read arrives before one or more writes. Since the target stores replies in a buffer with more than one entry several commands can be processed even if no replies are sent. Data for read replies is read when the reply is sent and thus writes coming after the read might have been performed already if there was congestion in the transmitter. To avoid this the RMAP buffer disable bit can be set to force the target to only use one buffer which prevents this situation.

The last control option for the target is the possibility to set the destination key which is found in a separate register.

*Table 1024.*AMBA port hardware RMAP handling of different packet type and command fields.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Command	Action
Reserved	Command / Response	Write / Read	Verify data before write	Acknow-ledge	Increment Address		
0	0	-	-	-	-	Response	Stored to DMA-channel.
0	1	0	0	0	0	Not used	Does nothing. No reply is sent.
0	1	0	0	0	1	Not used	Does nothing. No reply is sent.
0	1	0	0	1	0	Read single address	Executed normally. Address has to be word aligned and data size a multiple of four. Reply is sent. If alignment restrictions are violated error code is set to 10.
0	1	0	0	1	1	Read incre-menting address.	Executed normally. No restrictions. Reply is sent.
0	1	0	1	0	0	Not used	Does nothing. No reply is sent.
0	1	0	1	0	1	Not used	Does nothing. No reply is sent.
0	1	0	1	1	0	Not used	Does nothing. Reply is sent with error code 2.

*Table 1024.*AMBA port hardware RMAP handling of different packet type and command fields.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Command	Action
Reserved	Command / Response	Write / Read	Verify data before write	Acknow-ledge	Increment Address		
0	1	0	1	1	1	Read-Mod-ify-Write increment-ing address	Executed normally. If length is not one of the allowed rmw val-ues nothing is done and error code is set to 11. If the length was correct, alignment restric-tions are checked next. 1 byte can be rmw to any address. 2 bytes must be halfword aligned. 3 bytes are not allowed. 4 bytes must be word aligned. If these restrictions are violated nothing is done and error code is set to 10. If an AHB error occurs error code is set to 1. Reply is sent.
0	1	1	0	0	0	Write, sin-gle-address, do not verify before writ-ing, no acknowledge	Executed normally. Address has to be word aligned and data size a multiple of four. If alignment is violated nothing is done. No reply is sent.
0	1	1	0	0	1	Write, incre-menting address, do not verify before writ-ing, no acknowledge	Executed normally. No restric-tions. No reply is sent.
0	1	1	0	1	0	Write, sin-gle-address, do not verify before writ-ing, send acknowledge	Executed normally. Address has to be word aligned and data size a multiple of four. If alignment is violated nothing is done and error code is set to 10. If an AHB error occurs error code is set to 1. Reply is sent.
0	1	1	0	1	1	Write, incre-menting address, do not verify before writ-ing, send acknowledge	Executed normally. No restric-tions. If AHB error occurs error code is set to 1. Reply is sent.
0	1	1	1	0	0	Write, single address, ver-ify before writing, no acknowledge	Executed normally. Length must be 4 or less. Otherwise nothing is done. Same alignment restric-tions apply as for rmw. No reply is sent.

*Table 1024.*AMBA port hardware RMAP handling of different packet type and command fields.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Command	Action
Reserved	Command / Response	Write / Read	Verify data before write	Acknow-ledge	Increment Address		
0	1	1	1	0	1	Write, incre-menting address, ver-ify before writing, no acknowledge	Executed normally. Length must be 4 or less. Otherwise nothing is done. Same alignment restric-tions apply as for rmw. If they are violated nothing is done. No reply is sent.
0	1	1	1	1	0	Write, single address, ver-ify before writing, send acknowledge	Executed normally. Length must be 4 or less. Otherwise nothing is done and error code is set to 9. Same alignment restrictions apply as for rmw. If they are vio-lated nothing is done and error code is set to 10. If an AHB error occurs error code is set to 1. Reply is sent.
0	1	1	1	1	1	Write, incre-menting address, ver-ify before writing, send acknowledge	Executed normally. Length must be 4 or less. Otherwise nothing is done and error code is set to 9. Same alignment restrictions apply as for rmw. If they are vio-lated nothing is done and error code is set to 10. If an AHB error occurs error code is set to 1. Reply is sent.
1	0	-	-	-	-	Unused	Stored to DMA-channel.
1	1	-	-	-	-	Unused	Stored to DMA-channel.

62.5.6 AMBA interface

The AMBA interface consists of an APB interface, an AHB master interface and DMA FIFOs. The APB interface provides access to the user registers which are described in section 62.8. The DMA engines have 32-bit wide FIFOs to the AHB master interface which are used when reading and writing to the bus.

The transmitter DMA engine reads data from the bus in bursts which are half the FIFO size in length. A burst is always started when the FIFO is half-empty or if it can hold the last data for the packet. The burst containing the last data might have shorter length if the packet is not an even number of bursts in size.

The receiver DMA works in the same way except that it checks if the FIFO is half-full and then performs a burst write to the bus which is half the fifo size in length. The last burst might be shorter. If the rmap or rxunaligned VHDL generics are set to 1 the interface also handles byte accesses. Byte accesses are used for non word-aligned buffers and/or packet lengths that are not a multiple of four bytes. There might be 1 to 3 single byte writes when writing the beginning and end of the received packets.

62.5.6.1 APB slave interface

As mentioned above, the APB interface provides access to the user registers which are 32-bits in width. The accesses to this interface are required to be aligned word accesses. The result is undefined if this restriction is violated.

62.5.6.2 AHB master interface

The port contains a single master interface which is used by both the transmitter and receiver DMA engines. The arbitration algorithm between the channels is done so that if the current owner requests the interface again it will always acquire it. This will not lead to starvation problems since the DMA engines always deassert their requests between accesses.

The AHB accesses are always word accesses (HSIZE = 0x010) of type incremental burst with unspecified length (HBURST = 0x001) if VHDL generics rmap and rxunaligned are disabled. The AHB accesses can be of size byte, halfword and word (HSIZE = 0x000, 0x001, 0x010) otherwise. Byte and halfword accesses are always NONSEQ. Note that read accesses are always word accesses (HSIZE = 0x010), which can result in destructive read.

The burst length will be half the AHB FIFO size except for the last transfer for a packet which might be smaller. Shorter accesses are also done during descriptor reads and status writes.

The AHB master also supports non-incrementing accesses where the address will be constant for several consecutive accesses. HTRANS will always be NONSEQ in this case while for incrementing accesses it is set to SEQ after the first access. This feature is included to support non-incrementing reads and writes for RMAP.

If the core does not need the bus after a burst has finished there will be one wasted cycle (HTRANS = IDLE).

BUSY transfer types are never requested and the port provides full support for ERROR, RETRY and SPLIT responses.

62.5.7 Synthesis and hardware

62.5.7.1 Clocking

The AMBA ports run on the same clock as the router switch matrix.

62.5.7.2 Fault-tolerance

The ports can optionally be implemented with fault-tolerance against SEU errors in the FIFO memories. The fault-tolerance is enabled through the *ft* VHDL generic. Possible options are byte parity protection (*ft = 1*) or TMR (*ft = 2*).

62.5.7.3 Technology mapping

The core has three generics for technology mapping: *tech*, *techfifo* and *memtech*. *Tech* selects the technology used for the clock buffers and also adds reset to some registers for technologies where they would otherwise cause problems with gate-level simulations. *Techfifo* selects whether *memtech* should be used to select the technology for the FIFO memories (the RMAP buffer is not affected by the this generic) or if they should be inferred. *Tech* and *memtech* can be set to any value from 0 to NTECH as defined in the GRLIB.TECH package.

62.5.7.4 RAM usage

The core maps all RAM memories on the syncram_2p component if the *ft* generic is 0 and to the syncram_2pft component for other values. The syncrams are located in the technology mapping library (TECHMAP). The organization of the different memories are described below. If techfifo and/or memtech is set to 0 the synthesis tool will infer the memories. Either RAM blocks or flip-flops will be used depending on the tool and technology. The number of flip-flops used is *syncram depth x syncram width* for all the different memories. The receiver AHB FIFO with fifosize 32 will for example use 1024 flips-flops.

62.5.7.4.1Receiver ahb FIFO

The receiver AHB fifo consists of one syncram_2p block with a width of 32-bits. The depth is determined by the configured FIFO depth. Table 1025 shows the syncram organization for the allowed configurations.

Table 1025.syncram_2p sizes for GRSPW receiver AHB FIFO.

Fifosize	Syncram_2p organization
4	4x32
8	8x32
16	16x32
32	32x32

62.5.7.4.2Transmitter ahb FIFO

The transmitter AHB fifo consists of one syncram_2p block with a width of 32-bits. The depth is determined by the configured FIFO depth. Table 1026 shows the syncram organization for the allowed configurations.

Table 1026.syncram_2p sizes for transmitter AHB FIFO.

Fifosize	Syncram_2p organization
4	4x32
8	8x32
16	16x32
32	32x32

62.5.7.4.3Receiver N-Char FIFO

The receiver N-Char fifo consists of one syncram_2p block with a width of 9-bits. The depth is determined by the configured FIFO depth. Table 1027 shows the syncram organization for the allowed configurations.

Table 1027.syncram_2p sizes for the receiver N-Char FIFO.

Fifosize	Syncram_2p organization
16	16x9
32	32x9
64	64x9

62.5.7.4.4RMAP buffer

The RMAP buffer consists of one syncram_2p block with a width of 8-bits. The depth is determined by the number of configured RMAP buffers. Table 1028 shows the syncram organization for the allowed configurations.

*Table 1028.*syncram_2p sizes for RMAP buffer memory.

RMAP buffers	Syncram_2p organization
2	64x8
4	128x8
8	256x8

62.5.8 Registers

The port is programmed through registers mapped into APB address space. The addresses in the table below are offsets from each port's base address. The actual AMBA AHB address used to access the port is determined as follows: The AMBA ports' registers are accessed through an APB interface which resides on the APB bus. The APB bus is connected to the AHB bus using an APB controller whose AHB address determines the first base address for the AMBA ports.

See the grlib manual and APB controller manual on howto determine this base address. The starting base address on the APB bus for each AMBA port APB interface is set by the paddr and pmask VHDL generics. The starting paddr value is then incremented by one for each port. Finally a registers address is determined by adding the APB controller's AHB base address, the ports APB base address and the registers offset.

*Table 1029.*AMBA port registers

APB address offset	Register
0x0	Control
0x4	Status/Interrupt-source
0x8	Default address
0xC	Reserved
0x10	Destination key
0x14	Time
0x20	DMA channel 1 control/status
0x24	DMA channel 1 rx maximum length
0x28	DMA channel 1 transmit descriptor table address.
0x2C	DMA channel 1 receive descriptor table address.
0x30	DMA channel 1 address register
0x34	Unused
0x38	Unused
0x3C	Unused
0x40 - 0x5C	DMA channel 2 registers
0x60 - 0x7C	DMA channel 3 registers
0x80 - 0x9C	DMA channel 4 registers

62.5.8.1 AMBA Port Control Register

*Table 1030.*AMBA port control register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RA	RX	RC	NCH		RESERVED									RD	RE	RESERVED				TR	TT	R	TQ	R	RS	PM	TI	IE	RESERVED		
*	*	*	*		0									0	*	0				0	0	0	0	0	0	0	0	0	0		
r	r	r	r		r									rw	rw	r				rw	rw	r	rw	r	rw	rw	rw	rw	r		

31	RMAP available (RA) - Set to one if the RMAP target is available.	r
30	RX unaligned access (RX) - Set to one if unaligned writes are available for the receiver.	r
29	RMAP CRC available (RC) - Set to one if RMAP CRC is enabled in the core.	r
28: 27	Number of DMA channels (NCH) - The number of available DMA channels minus one (Number of channels = NCH+1).	r
26: 18	RESERVED	r
17	RMAP buffer disable (RD) - If set only one RMAP buffer is used. This ensures that all RMAP commands will be executed consecutively. Only available if the rmap VHDL generic is set to 1.	rw
16	RMAP Enable (RE) - Enable RMAP target. Reset value taken from the ri.rmapen signal with index corresponding to this port starting with 0 for the first AMBA port. Only available if rmap VHDL generic is set to 1.	rw
15: 12	RESERVED	r
11	Time Rx Enable (TR) - Enable time-code receptions.	rw
10	Time Tx Enable (TT) - Enable time-code transmissions.	rw
9	RESERVED	r
8	Tick-out IRQ (TQ) - Generate interrupt when a valid time-code is received.	rw
7	RESERVED	t
6	Reset (RS) - Make complete reset of the SpaceWire node. Self clearing.	rw
5	Promiscuous Mode (PM) - Enable Promiscuous mode.	rw
4	Tick In (TI) - The host can generate a tick by writing a one to this field. This will increment the timer counter and the new value is transmitted after the current character is transferred. A tick can also be generated by asserting the tick_in signal.	rw
3	Interrupt Enable (IE) - If set, an interrupt is generated when bit 8 is set and its corresponding event occurs.	rw
2: 0	RESERVED	r

62.5.8.2 AMBA Port Status Register

*Table 1031.*AMBA port status register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																							EE	IA	RESERVED						TO
0																							0	0	0						0
r																							wc	wc	r						wc

31: 9	RESERVED	r
8	Early EOP/EEP (EE) - Set to one when a packet is received with an EOP after the first byte for a non-rmap packet and after the second byte for a RMAP packet.	wc
7	Invalid Address (IA) - Set to one when a packet is received with an invalid destination address field, i.e it does not match the nodeaddr register.	wc
6: 1	RESERVED	r
0	Tick Out (TO) - A new time count value was received and is stored in the time counter field.	wc

62.5.8.3 AMBA Port Default Address Register

*Table 1032.*AMBA port default address register

31 16	15 8	7 0
RESERVED	DEFMASK	DEFADDR
0	0x00	0xFE
r	rw	rw

31: 8	RESERVED	r
15: 8	Default mask (DEFMASK) - Default mask used for node identification on the SpaceWire network. This field is used for masking the address before comparison. Both the received address and the DEFADDR field are anded with the inverse of DEFMASK before the address check.	rw
7: 0	Default address (DEFADDR) - Default address used for node identification on the SpaceWire network. Reset value: 254.	rw

62.5.8.4 AMBA Port Destination Key

*Table 1033.*AMBA port destination key

31 8	7 0
RESERVED	DESTKEY
0	0x00
r	rw

31: 8	RESERVED	r
7: 0	Destination key (DESTKEY) - RMAP destination key. Only available if the rmap VHDL generic is set to 1.	rw

62.5.8.5 AMBA Port Time Register

*Table 1034.*AMBA port time register

31 8	7 6	5 0
RESERVED	TCTRL	TIMECNT
0	00	0x00
r	rw	rw

31: 8	RESERVED	r
7: 6	Time control flags (TCTRL) - The current value of the time control flags. Sent with time-code resulting from a tick-in. Received control flags are also stored in this register.	rw
5: 0	Time counter (TIMECNT) - The current value of the system time counter. It is incremented for each tick-in and the incremented value is transmitted. The register can also be written directly but the written value will not be transmitted. Received time-counter values are also stored in this register	rw

62.5.8.6 AMBA DMA Control Register

*Table 1035.*AMBA port dma control register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																SP	SA	EN	NS	RD	RX	AT	RA	TA	PR	PS	AI	RI	TI	RE	TE
0																0	0	0	0	0	0	0	0	0	0	0	NR	NR	NR	0	0
r																rw	rw	rw	rw	rw	r	rw	wc	wc	wc	wc	rw	rw	rw	rw	rw

31: 16	RESERVED	r
15	Strip pid (SP) - Remove the pid byte (second byte) of each packet. The address byte (first byte) will also be removed when this bit is set independent of the SA bit.	rw
14	Strip addr (SA) - Remove the addr byte (first byte) of each packet.	rw
13	Enable addr (EN) - Enable separate node address for this channel.	rw
12	No spill (NS) - If cleared, packets will be discarded when a packet is arriving and there are no active descriptors. If set, the GRSPW will wait for a descriptor to be activated.	rw
11	Rx descriptors available (RD) - Set to one, to indicate to the GRSPW that there are enabled descriptors in the descriptor table. Cleared by the GRSPW when it encounters a disabled descriptor:	rw
10	RX active (RX) - Is set to ‘1’ if a reception to the DMA channel is currently active otherwise it is ‘0’.	r
9	Abort TX (AT) - Set to one to abort the currently transmitting packet and disable transmissions. If no transmission is active the only effect is to disable transmissions. Self clearing.	rw
8	RX AHB error (RA) - An error response was detected on the AHB bus while this receive DMA channel was accessing the bus.	wc
7	TX AHB error (TA) - An error response was detected on the AHB bus while this transmit DMA channel was accessing the bus.	wc
6	Packet received (PR) - This bit is set each time a packet has been received. never cleared by the SW-node.	wc
5	Packet sent (PS) - This bit is set each time a packet has been sent. Never cleared by the SW-node.	wc
4	AHB error interrupt (AI) - If set, an interrupt will be generated each time an AHB error occurs when this DMA channel is accessing the bus.	rw
3	Receive interrupt (RI) - If set, an interrupt will be generated each time a packet has been received. This happens both if the packet is terminated by an EEP or EOP.	rw
2	Transmit interrupt (TI) - If set, an interrupt will be generated each time a packet is transmitted. The interrupt is generated regardless of whether the transmission was successful or not.	rw
1	Receiver enable (RE) - Set to one when packets are allowed to be received to this channel.	rw
0	Transmitter enable (TE) - Write a one to this bit each time new descriptors are activated in the table. Writing a one will cause the SW-node to read a new descriptor and try to transmit the packet it points to. This bit is automatically cleared when the SW-node encounters a descriptor which is disabled.	rw

62.5.8.7 AMBA Port RX Maximum Length Register

*Table 1036.*AMBA port RX maximum length register.

31	25	24	0
RESERVED		RXMAXLEN	
0		NR	
r		rw	

31: 25	RESERVED	r
24: 0	RX maximum length (RXMAXLEN) - Receiver packet maximum length in bytes. Only bits 24 - 2 are writable. Bits 1 - 0 are always 0.	rw

62.5.8.8 AMBA Port Transmitter Descriptor Table Address Register

*Table 1037.*AMBA port transmitter descriptor table address register.

31 10	9 4	3 0
DESCBASEADDR	DESCSEL	RESERVED
NR	0	0
rw	rw	r

31: 10	Descriptor table base address (DESCBASEADDR) - Sets the base address of the descriptor table.	rw
9: 4	Descriptor selector (DESCSEL) - Offset into the descriptor table. Shows which descriptor is currently used by the GRSPW. For each new descriptor read, the selector will increase with 16 and eventually wrap to zero again.	rw
3: 0	RESERVED	r

62.5.8.9 AMBA Port Receiver Descriptor Table Address Register

*Table 1038.*AMBA port receiver descriptor table address register.

31 10	9 3	2 0
DESCBASEADDR	DESCSEL	RESERVED
NR	0	0
rw	rw	r

31: 10	Descriptor table base address (DESCBASEADDR) - Sets the base address of the descriptor table. Not reset.	rw
9: 3	Descriptor selector (DESCSEL) - Offset into the descriptor table. Shows which descriptor is currently used by the GRSPW. For each new descriptor read, the selector will increase with 8 and eventually wrap to zero again. Reset value: 0.	rw
2: 0	RESERVED	r

62.5.8.10 AMBA Port DMA Channel Address Register

*Table 1039.*AMBA port dma channel address register

31 16	15 8	7 0
RESERVED	MASK	ADDR
0	NR	NR
r	rw	rw

31: 8	RESERVED	r
15: 8	Mask (MASK) - Mask used for node identification on the SpaceWire network. This field is used for masking the address before comparison. Both the received address and the ADDR field are anded with the inverse of MASK before the address check.	rw
7: 0	Address (ADDR) - Address used for node identification on the SpaceWire network for the corresponding dma channel when the EN bit in the DMA control register is set.	rw

62.5.9 Vendor and device identifiers

The port has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x8A. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

62.6 Configuration port

The configuration port uses the RMAP protocol (ECSS-E-ST-50-52C). Verified writes, reads and read-modify-writes all of length 4 bytes are supported (8B for RMW if the mask field is included in the count). Replies sent from the configuration port are always replied to the port they arrived from

regardless of the source address. The address space of the configuration port is specified in section 62.8. Addresses outside of the range will result in an authorization error. Table 1041 gives a detailed listing of the configuration port's handling of RMAP packets.

Per default the configuration area can be accessed from all the ports. Configuration accesses can be individually disabled per port using the CE bit in the port control register. Writes to the configuration area can be globally disabled by writing a 0 to the WE bit in the configuration write enable register. This disables write accesses from all ports to all registers except the configuration write enable register itself.

There is also a signal, ri.cfglock, which can be used to disable configuration accesses from all ports except port 1. This signal overrides the settings of the CE bits in the port control registers. The global write enable register still affects port 1 in this case.

When an otherwise correct RMAP command destined to the configuration port is received but not allowed due to one or more of the configuration access disable options being enabled a reply with status set to authorization failure will be sent if requested. If a reply is not requested the packet will be silently discarded. In both cases the command will not be performed and has no effect on the configuration port registers.

62.6.1 AMBA AHB slave interface

An AMBA AHB slave interface can be optionally included which makes the whole configuration port memory area accessible from the AHB bus. The address offsets are the same as when accessing through RMAP but the base address is different. The 32-bit AHB base address is calculated by setting bits 19 downto 0 to 0x00000 and bits 31 downto 20 to the VHDL generics cfghaddr and cfghmask anded. So if for example cfghaddr is 0xC00 and cfghmask is 0xFFF the routers AHB memory area will occupy 1 MB starting from 0xC0000000.

Only word accesses (32-bit) are allowed. The routing table is shared between the ports, RMAP target and AHB slave so accesses from the AHB slave might be stalled because the of accesses from the other sources. The priority order starting from the highest is router ports, RMAP target and AHB slave. The router ports access order is controlled using a round-robin abitration mechanism.

None of the registers and signals for limiting configuration accesses have any effect on the AHB slave interface.

There is predetermined order in which error-codes are set in the case of multiple errors in the core. It is shown in table 1040.

Table 1040. The order of error detection in case of multiple errors in the configuration port RMAP target. The error detected first has number 1.

Detection Order	Error Code	Error
1	12	Invalid destination logical address
2	2	Unused RMAP packet type or command code
3	3	Invalid destination key
4	9	Verify buffer overrun
5	11	RMW data length error
6	10	Authorization failure
8	5/7	Early EOP / EEP (if early)
9	4	Invalid Data CRC
11	7	EEP
12	6	Too much data

Errors up to and including Invalid Data CRC (number 8) are checked before executing a command. The other errors do not prevent verified operations from being performed.

The details of the support for the different commands are now presented. All defined commands which are received but have an option set which is not supported in this specific implementation will not be executed and a reply is sent (if the acknowledge bit was set) with error code 10.

62.6.2 Write commands

The write commands are divided into two subcategories when examining their capabilities: verified writes and non-verified writes. The configuration port only supports verified writes with the length restricted to 4 and 0 bytes and the address must be 4 B aligned (address(1:0)=00). Since only one location can be accessed for each command the incrementing address bit can be set to either 0 or 1 and the behavior will be the same. If any of the restrictions mentioned above are violated an reply (if requested) will be sent with the status field set to 10.

62.6.3 Read commands

Read commands are also restricted to 4 or 0 bytes in length and the address has to be 4 B aligned. As for writes each read command only accesses one location so the increment bit can be either 0 or 1.

62.6.4 RMW commands

RMW supports the size 4 or 0 bytes (8 B or 0 B if the mask field is included in the count). The RMW accesses have the same restrictions as the verified writes. As in the verified write case, the incrementing bit can be set to any value since only one operation will be performed for each command. Too much data is detected after the complete command was received and will not prevent the write from being executed. No data is sent in a reply if an error is detected i.e. the status field is non-zero.

The RMW operation is performed by first reading the address location and then writing the same location with the value obtained from the formula data = (writedata and mask) or (readdata and not mask). This means the data bits corresponding to mask bits set to 0 will retain their old value and other bits will be updated with a new value from the data provided in the rmw command.

*Table 1041.*RMAP command support by the configuration port.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Packet type	Action
Reserved	Command / Response	Write / Read	Verify data before write	Acknow-ledge	Increment Address		
0	0	-	-	-	-	Response	Packet is discarded, no operation is performed and no reply is sent.
0	1	0	0	0	0	Not used	Packet is discarded, no operation is performed and no reply is sent.
0	1	0	0	0	1	Not used	Packet is discarded, no operation is performed and no reply is sent.
0	1	0	0	1	0	Read single address	Supported. Address has to be word aligned and belonging to the defined address range, data length has to be 4. Reply is sent. If alignment restrictions or address ranges are violated error code is set to 10.
0	1	0	0	1	1	Read incrementing address.	Supported. Address has to be word aligned and belonging to the defined address range, data length has to be 4. Reply is sent. If alignment restrictions or address ranges are violated error code is set to 10.
0	1	0	1	0	0	Not used	Packet is discarded, no operation is performed and no reply is sent.
0	1	0	1	0	1	Not used	Packet is discarded, no operation is performed and no reply is sent.
0	1	0	1	1	0	Not used	No operation is performed. Reply is sent with error code 2.
0	1	0	1	1	1	Read-Modify-Write incrementing address	Supported. The data length has to be 8 (4 B mask and 4 B data) and the address word aligned and within the supported range. If these restrictions are violated the command is not executed and the error code is set to 10. Reply is sent.
0	1	1	0	0	0	Write, single-address, do not verify before writing, no acknowledge	Not implemented. Packet is discarded and no reply is sent.
0	1	1	0	0	1	Write, incrementing address, do not verify before writing, no acknowledge	Not implemented. Packet is discarded and no reply is sent.

*Table 1041.*RMAP command support by the configuration port.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Packet type	Action
Reserved	Command / Response	Write / Read	Verify data before write	Acknow-ledge	Increment Address		
0	1	1	0	1	0	Write, sin-gle-address, do not verify before writ-ing, send acknowledge	Not implemented. Command is not executed. Error code is set to 10 and a Reply is sent.
0	1	1	0	1	1	Write, incre-menting address, do not verify before writ-ing, send acknowledge	Not implemented. Command is not executed. Error code is set to 10 and a Reply is sent.
0	1	1	1	0	0	Write, single address, ver-ify before writing, no acknowledge	Supported. Length must be 4, address must be word aligned and within the allowed range. Otherwise the command is not executed. No reply is sent.
0	1	1	1	0	1	Write, incre-menting address, ver-ify before writing, no acknowledge	Supported. Length must be 4, address must be word aligned and within the allowed range. Otherwise the command is not executed. No reply is sent.
0	1	1	1	1	0	Write, single address, ver-ify before writing, send acknowledge	Supported. Length must be 4, address must be word aligned and within the allowed range. Otherwise the command is not executed. If one of these errors are detected the error code is set to 10. Reply is sent.
0	1	1	1	1	1	Write, incre-menting address, ver-ify before writing, send acknowledge	Supported. Length must be 4, address must be word aligned and within the allowed range. Otherwise the command is not executed. If one of these errors are detected the error code is set to 10. Reply is sent.
1	0	-	-	-	-	Unused	Packet is discarded, no opera-tion is performed and no reply is sent.
1	1	-	-	-	-	Unused	Packet is discarded, no opera-tion is performed and no reply is sent.

62.7 Configuration options

Table 1042 shows the configuration options of the core (VHDL generics).

*Table 1042.*Configuration options

Generic	Function	Allowed range	Default
input_type	Select receiver type. 0 = Self clocking (xor), 1 = Interface for Cobham SpaceWire transceiver, 2 = Single data rate sampling, 3 and 4 = Double data rate sampling, 5 = Self-clocking with external recovery, 6 = Self-clocking with external recovery and DDR register for data. This generic must be set to the same value as the GRSPW2_PHY generic with the same name.	0 - 6	0
output_type	Select transmitter type. 0 = single data rate, 1 = double data rate, 2 = interface for Cobham SpaceWire transceiver	0 - 2	0
rxtx_sameclk	Set to one if the same clock net is connected to both the receiver and transmitter (which means this feature is only applicable when the receiver uses sampling). This will remove some unnecessary synchronization registers.	0 - 1	0
fifosize	Sets the number of entries in the 9-bit receiver fifo (N-Char fifo).	16 - 2048	64
tech	Technology for on-chip memories.	-	-
scantest	Enable scan test support	0 - 1	0
techfifo	Enable tech support for on-chip memories.	0 - 1	0
ft	Enable fault-tolerance against SEU errors	0 - 2	0
spwports	Sets the number of SpaceWire link ports.	0 - 31	2
ambaports	Sets the number of AMBA ports.	0 - 16	0
fifoports	Sets the number of FIFO ports.	0 - 31	0
arbitration	Select the arbitration type. Currently unused.	0 - 1	0
rmap	Include hardware RMAP target in the AMBA ports. RMAP CRC logic will also be added in this case and the rmapcrc generic will have no additional effect. Bit index 0 of the binary representation of the integer corresponds to amba port 1, index 1 to amba port 2 etc.	0 - 16#FFFF#	0
rmapcrc	Enable RMAP CRC logic for the AMBA ports. Bit index 0 of the binary representation of the integer corresponds to amba port 1, index 1 to amba port 2 etc.	0 - 16#FFFF#	0
fifosize2	Sets the number of entries in the 32-bit AHB fifos for the AMBA ports.	4 - 32	32
almostsize	Sets the number of characters from the full or empty conditions that is used as the limit for the almost full and almost empty indications for the FIFO ports.	1 - 32	8
rxunaligned	Receiver unaligned write support. If set, the receiver can write any number of bytes to any start address without writing any excessive bytes. Bit index 0 of the binary representation of the integer corresponds to amba port 1, index 1 to amba port 2 etc.	0 - 16#FFFF#	0
rmapbufs	Sets the number of buffers to hold RMAP replies.	2 - 8	4
dmachan	Sets the number of DMA channels	1 - 4	1
hindex	AHB master index.	0 - NAHBMST-1	0
pindex	APB interface index value for first AMBA port. Incremented by one for each subsequent port.	0 - NAPBLSV-1	0

*Table 1042.*Configuration options

Generic	Function	Allowed range	Default
paddr	Determines the starting APB address for theAMBA ports together with pmask. For the first port bits 19 downto 12 in the address will be paddr anded with pmask. See the grlib manual for more details. Subsequent ports will have a starting address which is an increment of the previous value. The increment is determined by pmask. 16#FFF# = increment 1, 16#FFE# = increment 2, 16#FFC# = increment 4 etc.	0 - 16#FFF#	0
pmask	Mask for the APB address for the AMBA ports. Anded with paddr to determine the starting address and the range of the area for each port.	0 - 16#FFF#	16#FFF#
pirq	Interrupt number for first AMBA port. Will be incremented by one for each subsequent port.	0 - NAHBIRQ-1	0
cfghindex	AHB slave index.	0 to NAHBSLV-1	0
cfghaddr	ADDR field of the AHB BAR0 defining the AHB slave address space.	0 to 16#FFF#	0
cfghmask	MASK field of the AHB BAR0 defining the AHB slave address space.	0 to 16#FFF#	16#FFF#
ahbslven	Enable AHB slave interface.	0 to 1	0
timerbits	Enables timers when set to a nonzero value. The value determines the number prescaler bits.	0 to 31	0
pnp	Enable Plug and play on the configuration port.	0 to 1	0
autoscrub	Enable automatic scrubbing of routing table and port setup memories.	0 to 1	0
sim	Enable simulation mode. It has no effect when synthesizing but for simulation it shortens the autoscrub period to 1024 clock cycles to make simulation times shorter.	0 to 1	0
dualport	Enable dual port mode (primary and redundant) for SpaceWire ports.	0 to 1	1
charcntbits	Enables characters counters if nonzero and sets the number of counter bits.	0-31	0
pktcntbits	Enables packet counters if nonzero and sets the number of counter bits.	0-31	0
prescalermin	Sets the minimum value of the prescaler reload register. This only affects writes to the register, not the reset value.	-	250
codecclkgate	Enable the internal clockgate for the router clocks by setting this generic to 1. Note that this generic is only applicable to the wrapper grspwrouterm, as the clockgate is instantiated in there. If using the router without wrapper (grspwrouter), this generic is not available and the clockgate is disabled	0 - 1	0
internalrstgen	If this generic is set to 1, the reset generators for every clock domain are instantiated internally in the wrapper of the SpW router (grspwrouterm). Otherwise, the user is expected to implement the reset generation from the top level entity. This generic is only available when using the wrapper.	0 - 1	1
rstsrctmr	Enables the Triple Module Redundancy for the asynchronous reset nets of the core	0 - 1	0

62.8 Registers

The registers listed here are accessed through the RMAP target and the addresses specified shall be set in the address field of the RMAP command. They can also be accessed through AHB if the AHB slave is available. The AHB addresses are determined by adding the addresses in table 1045 to the AHB base address determined by the cfghaddr and cfghmask VHDL generics.

62.8.1 Reset value definitions

*Table 1043.*Reset value definitions

Value	Description
0	Reset to value 0
1	Reset to value 1
0x0	Hexadecimal value which can be used for multibit fields
NA	Not applicable. For example reserved fields or read only fields which are constant
NR	Not reset
*	Special reset condition. Described in textual description of the bit. Used for example when reset value is taken from a signal

62.8.2 Register type definitions

*Table 1044.*Register type definitions

Value	Description
r	Read only
w	Write only
rw	Readable and writable
wc	Readable and cleared when written with a 1
rc	Readable and cleared when read

*Table 1045.*GRSPWROUTER registers

RMAP address	Register
0x0	RESERVED
0x4-0x7C	Port setup for ports 1-31
0x80-0x3FC	Port setup for logical addresses 32-255
0x400-0x47C	RESERVED
0x480-0x7FC	Routing table entry for logical addresses 32-255
0x800-0x87C	Port 0-31 control
0x880-0x8FC	Port 0-31 status
0x900-0x97C	Timer reload ports 0-31
0xA00	Router configuration/status
0xA04	Time-code
0xA08	Version/instance ID
0xA0C	Initialization divisor
0xA10	Configuration write enable
0xA14	Timer prescaler reload
0xC04-0xC7C	Port 1-31 outgoing character count
0xC84-CFC	Port 1-31 incoming character count
0xD04-0xD7C	Port 1-31 outgoing packet count
0xD84-0xDFC	Port 1-31 incoming packet count

Table 1046. Port setup register

31	1	0
PORT ENABLE BITS		PD
NR		NR

31: 1 Port enable bits (PORT ENABLE BITS) - Each individual bit enables, when set to 1, packets with the path or logical address corresponding to this port setup register to be sent on the port with the same number as the bit index. Only bits up to and including the highest port number are valid. rw

0 Packet distribution (PD) - When set to 1 packet distribution is used for the path or logical address corresponding to this port setup register. When set to 0 group adaptive routing is used. rw

NOTE: When this register has been written with a non-zero value it will be considered valid and used for determinig the destination port. A memory error at location of the port setup information for the destination address will cause the packet to be discarded which will make the associated physical address unusable until the error is fixed (done automatically if auto-scrubbing is enabled). If this behavior is unacceptable GAR or PD should not be enabled for physical addresses. If a port setup entry for a physical address is valid it can be invalidated by writing zeros (to the valid bits in the register) to the memory location.

Table 1047. Routing table entry

31	3	2	1	0
RESERVED		EN	PR	HD
NA		NR	NR	NR

31: 3 RESERVED

2 Enable (EN) - Enables routing table entry. If enabled the corresponding logical address can be used to route packets, otherwise an invalid address error will be generated and the packet is discarded. Note that the corresponding port setup register must not be set to 0 when a routing table entry is enabled. rw

1 Priority (PR) - Sets the arbitration priority of this port. 0=low priority, 1=high priority. rw

0 Header deletion (HD) - Enable header deletion for this logical address. rw

Table 1048. Port control for configuration port (port 0)

31	10	9	8	7	6	5	4	3	2	1	0
RESERVED		TR	RESERVED								
N/A		*	N/A								

31: 10 RESERVED r

9 Timer enable (TR) - Enable timer for packet transfer timeouts for this port. Only available if the timerbits VHDL generic is 1. Reset value set from the ri.timeren signal. rw

8: 0 RESERVED r

Table 1049. Port control

31	24	23	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD		RESERVED		ET	NP	PS	BE	DI	TR	PR	TF	RS	TE	RE	CE	AS	LS	LD
*		N/A		*	0	0	*	0	*	0	0	0	1	NA	1	1	0	0

31: 24 Run-state clock divisor (RD) - Clock divisor value used for this link when in the run-state. Only available for SpW ports, reads as 0 otherwise. See 62.3.2 for details on how to set this field. Reset value taken from ri.idivisor signal. rw

23: 15 RESERVED r

Table 1049. Port control

14	Enable external time (ET) - When 0 an icnrement (+1)of the internal time-counter is used when sending a time-code as a result from a tickin. When 1 the time-code value is taken from external pins at the clock edge the tickin is asserted. Reset value taken from the ri.en_ext_time signal with the index corresponding to the current FIFO port starting with 0 from the lowest index FIFO port. Only available for FIFO ports.	rw
13	No portforce (NP)- When set to 1 the active port between the primary and redundant port is selected automatically by detecting activity on the incoming signals. When 0 the active port is selected using the PS bit. Only applicable to SpaceWire ports. Only available when dualport is enabled.	rw
12	Port select (PS) - Selects between the primary and redunant port when NP is 0. It has no effect when NP is 1. Only applicable to SpaceWire ports. Only available when dualport is enabled.	rw
11	FIFO bridge enable (BE) - Set to 1 to enable bridge mode for the FIFO port which will enable it to be connected to another GRSPWROUTER FIFO port with automatic transfers. Only available for FIFO ports. Reset value set from the signal index of ri.enbridge corresponding to this FIFO port number.	rw
10	Disable port (DI) - Disable data transfers on this port. When asserted packets sent to this port will be spilt and the invalid address bit is set in the source port. For group adaptive routing disabled ports will not be included in the group of possible destinations. For packet distribution they will not be transmitted to but the other destination ports will still be transmitted to. Port 1 cannot be disabled and this bit is read only 0 in that case.	rw
9	Timer enable (TR) - Enable timer for packet transfer timeouts for this port. Only available if the timerbits VHDL generic is 1. Reset value set from the ri.timeren signal.	rw
8	Priority (PR) - Sets the arbitration priority for the path address corresponding to this port. 0=low priority, 1=high priority.	rw
7	Transmitter FIFO reset (TF) - Resets the transmitter FIFO on this port. This means that the FIFO is emptied (counters and pointers set to 0) and lastly an EEP is written to the FIFO to ensure that incomplete packets are detected by the receiver. If a packet transmission was active (a source port was writing to the destination port) when the FIFO reset was asserted the remainder of that packet up to and including EOP/EEP will be spilt.	rw
6	Receiver spill (RS) - Spills the receiver FIFO meaning that the packet currently being received is spilt up to and including the EOP/EEP. If no packet reception is currently active on this port nothing happens. The port or ports in the case of packet distribution will have an EEP written to the transmit FIFO to indicate that the packet was ended prematurely. Not available for AMBA ports.	rw
5	Time-code enable (TE) - Enables time-codes to be received and transmitted on this port. When enabled received time-codes are processed and if valid a tick-out will be generated and the time-code is forwarded to the other ports. When disabled received time-codes are ignored. Time-codes are only transmitted on this port if this bit is set to 1 and tick-in is ignored otherwise.	rw
4	RESERVED	r
3	Configuration port enable (CE) - Enable accesses to the configuration port. If disabled packets to the configuration port will be spilt.	rw
2	Autostart (AS) - Enable the Link interface FSM Autostart feature. Only available for SpW ports, reads as 0 otherwise.	rw
1	Link start (LS) - Start the link interface FSM. Only available for SpW ports, reads as 0 otherwise.	rw
0	Link disabled (LD) - Disable the link interface FSM. Only available for SpW ports, reads as 0 otherwise.	rw

Table 1050. Port status configuration port (port 0)

31 25	24	23 20	19	18	17 12	11 7	6 5 4 3 2 1 0
RESERVED	CE	ERRCODE	RE	TS	RESERVED	TP	RESERVED
NA	0	NR	NA	0	NA	00000	NA

31: 25	RESERVED	r
24	Clear error code (CE) - Write with a 1 to clear th ERRCODE field.	rw
23: 20	Error code (ERRCODE) - Shows the latest nonzero RMAP status code. If zero no error has occurred.	r
19	RESERVED	r
18	Timeout spill (TS) - Packet spilled due to timeout. Only available if timerbits is nonzero.	wc
17: 12	RESERVED	r

Table 1050. Port status configuration port (port 0)

11: 7	Transmitting port (TP) - The number of the port currently accessing the configuration port.	r
6: 0	RESERVED	r

Table 1051. Port status

31	30	29 ... 20	19	18	17	16	15	14 ... 12	11 ... 7	6	5	4	3	2	1	0
PT		RESERVED	AP	TS	ME	TF	RE	LS	TP	PB	PR	IA	CE	ER	DE	PE
NA		NA	NR	0	0	0	1	000	00000	NA	NA	0	0	0	0	0

31: 30	Port type (PT) - The type of this port. “00” = SpaceWire port, “01” = AMBA port, “10”= FIFO port	r
29: 20	RESERVED	r
19	Active port(AP) - Show which of the primary and redundant port is active. 0 = primary port, 1 = redundant port. Only applicable to SpaceWire ports. Only available when dualport is enabled..	r
18	Timeout spill (TS) - Packet spilled due to timeout. Only available if timerbits is nonzero.	wc
17	Memory error (ME) - Uncorrectable parity error detected in FIFO memories on this link.	wc
16	Transmit FIFO full (TF) - Set to 1 when the transmit FIFO on this port is full.	r
15	Receive FIFO empty(RE) - Set to 1 when the receive FIFO on this port is full. Not available for AMBA ports.	r
14: 12	Link state (LS) - Current link state. 000 = Error reset. 001 = Error wait, 010 = Ready, 011 = Started, 100 = Connecting, 101 = Run state. Only available for SpW ports, reads as 0 otherwise.	r
11: 7	Transmitting port (TP) - The number of the port currently transmitting on this port. Only valid if the PB bit is set to 1.	r
6	Port transmit busy (PB) - Set to 1 when a packet is being transmitted on this port.	r
5	Port receive busy (PR) - Set to 1 when a packet is being received on this port.	r
4	Invalid address (IA) - A packet with an invalid address was received on this link.	wc
3	Credit error (CE) - Set when a credit error has occurred on the link. Only available for SpW ports, reads as 0 otherwise.	wc
2	Escape error (ER) - Set when an escape error has occurred on the link. Only available for SpW ports, reads as 0 otherwise.	wc
1	Disconnect error (DE) - Set when a disconnect error has occurred on the link. Only available for SpW ports, reads as 0 otherwise.	wc
0	Parity error (PE) - Set when a parity error has occurred on the link. Only available for SpW ports, reads as 0 otherwise.	wc

Table 1052. Timer reload

31 ... 10	9 ... 0
RESERVED	RELOAD
	*

31: 10	RESERVED	r
9: 0	Timer reload (RELOAD) - Port specific timer reload value. This timer runs on the prescaler generated tick and determines the timeout period for the port it is associated with. The minium value of this register is 1. Writing a 0 will result in 1 being written. Reset value set from the ri.reloadn signal.	rw

Table 1053. Router configuration/status

31 ... 27	26 ... 22	21 ... 17	16 ... 8	7	6	5	4	3	2	1	0
SPWPORTS	AMBAPORTS	FIFOPORTS	RESERVED	RE	AD	LS	SA	TF	ME	TA	PP
NA	NA	NA	NA	0	*	*	*	0	0	NA	NA

Table 1053. Router configuration/status

31: 27	SpaceWire ports (SPWPORTS) - Set to the number of SpaceWire ports in the router.	r
26: 22	AMBA ports (AMBAPORTS) - Set to the number of AMBA ports in the router.	r
21: 17	FIFO ports (FIFOPORTS) - Set to the number of FIFO ports in the router.	r
16: 8	RESERVED	r
7	Reset (RE) - Resets the complete router when written with a 1. The router will not respond for 6-7 core clock cycles. Thus when writing this register through RMAP the reply bit should NOT bet set since the reply will not be sent.	rw
6	Auto disconnect (AD) - When set to 1 ports will be automatically stopped after a timeout period of inactivity. Only available if timers are enabled. Reset value taken from the ri.autodconnect signal.	rw
5	Link start on request (LS) - When set to 1 ports will be started automatically when there is a request to transmit a packet on the port. The link will only start if it is not disabled. Reset value taken from the ri.linkstartreq signal.	rw
4	Self addressing enable (SA) - If set to 1 ports are allowed to send packets to themselves. If 0 packets with the same source and destiination port are spilt and an invalid address error is asserted. Reset value taken from the ri.selfaddren signal.	rw
3	Time-code control flag mode (TF) - When 0 the time-code control flags can have any value for normal operation. When set to 1 the control flags must have the value “00” for normal time-code operation, otherwise the time-codes are discarded.	rw
2	Memory error (ME) - Set to one each time an uncorrectable error has been detected in either the routing table or port setup memory.	wc
1	Timers available(TA) - Set to one if the router has watchdog timer support.	r
0	Plug and Play available (PP) - Set to one if the router has Plug and Play support.	r

Table 1054. Time-code

31 … 9	8	7 … 6	5 … 0
RESERVED	RE	EN	CF	TIMECNT
NA	0	1	0	0

31: 10	RESERVED	r
9	Reset time-code (RE) - Resets the control flags and time counters to 0 when written with a 1. Always reads as 0.	rw
8	Enable time-codes (EN) - Enable time-codes to propagate and update the counter and control flags. When disabled time-codes are ignored.	rw
7: 6	Time-control flags (CF) - The current value of the router control flags.	r
5: 0	Time-counter (TIMECNT) - Current value of the router time counter.	r

Table 1055. Version/Instance ID

31 … 24	23 … 16	15 … 8	7 … 0
MAJOR VERSION	MINOR VERSION	PATCH	INSTANCE ID
NA	NA	NA	*

31: 24	Major version (MAJOR VERSION) - Holds the major version number of the router.	r
23: 16	Minor version (MINOR VERSION) - Holds the minor version number of the router.	r
15: 8	Patch (PATCH) - Holds the patch number of the router.	r
7: 0	Instance ID (INSTANCE ID) - Holds the instance ID number of the router. Reset value taken from the ri.instanceid signal.	rw

Table 1056. Initialization divisor

31 8	7 0
RESERVED	ID
N/A	*

31: 8	RESERVED	r
7: 0	Initialization clock divisor (ID) - Clock divisor value used by all the SpaceWire links to generate the 10 Mbit/s rate during initialization. All the links use a common clock for this so only one divisor is needed. Only available if there is at least one SpaceWire port in the router, reads as 0 otherwise. See 62.3.2 for details on how to set this field. Reset value taken from ri.idivisor signal.	rw

Table 1057. Configuration write enable

31 1	0
RESERVED	WE
NA	1

31: 1	RESERVED	r
0	Configuration write enable (WE) - When set to 1 write accesses to the configuration area are allowed. When set to 0 writes are not allowed except to this register. Write or RMW commands will be replied with an authorization error if a reply was requested.	rw

Table 1058. Timer prescaler

31 16	16-1 0
RESERVED	PRESCALER
NA	*

31: 16	RESERVED	r
16 0 -1:	Timer prescaler (PRESCALER) - Global prescaler value used for generating a common tick for the port timers. The prescaler runs on clk (table 539) and a tick is generated every prescaler+1 cycle. Only available if the timerbits (table 528) generic is nonzero and the minimum value is set with the prescalermin generic. The minimum value of this register is 250. The timerbits generic also sets the number of bits of the prescaler and this value should replace x in this register description. Reset value taken from the ri.reload signal.	rw

Table 1059. Outgoing/incoming character count

31	16	16-1 0
RE	RESERVED	CHARCNT
0	NA	0x0000

31	Reset counter (RE) - Write with a 1 to reset the character counter.	rw
30: 16	RESERVED	r
16 0 -1:	Character count (CHARCNT) - Number of SpaceWire data character received/transmitted on this port. Note that EOP/EEP are not included.	rw

Table 1060. Outgoing/incoming packet count

31	16	16-1	0
RE	RESERVED	PKTCNT	
0	NA	0x0000	

31	Reset counter (RE) - Write with a 1 to reset the packte counter.	rw
30: 16	RESERVED	r
16 0 -1:	Packet count (PKTCNT) - Nnumber of packets received/transmitted on this port. Only packets of non-zero length are counted that is consecutive EOPs or EEPs are not counted.	rw

62.9 Vendor and device identifiers

The core has AMBA vendor ID 0x01 and device ID 0x8B (applies to the AHB slave interface). SpaceWire Plug and Play is not a standard yet so identifiers for this protocol have not been assigned.

62.10 Signal descriptions

Table 1061 shows the interface signals of the core (VHDL ports).

Table 1061. Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Core clock	-
RST_CODEC [SPWPORTS-1:0]	N/A	Input	Resets to be used by the internal SpW codecs. There is one per SpW port. This signal is not used by the core if the internal reset generators are enabled in the wrapper (generic internalrst-gen to 1). In that case, it is recommended to set every element of the array to '0'.	Low
CLK_CODEC [SPWPORTS-1:0]	N/A	Input	Main clock to be used by the internal SpW codecs. There is one per SpW port. This signal is not used by the core if the internal reset generators are enabled in the wrapper (generic internalrstgen to 1). In that case, it is recommended to set every element of the array to '0'.	-
RXASYNCRST [SPWPORTS-1:0]	N/A	Input	Asynchronous resets for the SpW RX clocks to be used by the internal SpW codecs. There is one per SpW port. This signal is not used by the core if the internal reset generators are enabled in the wrapper (generic internalrstgen to 1). In that case, it is recommended to set every element of the array to '0'.	Low
RXSYNCRST [SPWPORTS *(1+dualport)-1:0]	N/A	Input	Synchronous resets for the SpW RX clocks to be used by the internal SpW codecs. There are one or two per SpW port, depending on the value of the generic dualport. This signal is not used by the core if the internal reset generators are enabled in the wrapper (generic internalrstgen to 1). In that case, it is recommended to set every element of the array to '0'.	Low
RXCLK [SPWPORTS *(1+dualport)-1:0]	N/A	Input	Receiver clock vector. One or two clocks for each SpaceWire link, depending on the value of the generic dualport.	-
TXSYNCRST [SPWPORTS-1:0]	N/A	Input	Synchronous resets for the SpW TX clocks to be used by the internal SpW codecs. There is one per SpW port. This signal is not used by the core if the internal reset generators are enabled in the wrapper (generic internalrstgen to 1). In that case, it is recommended to set every element of the array to '0'.	Low
TXCLK [SPWPORTS-1:0]	N/A	Input	SpaceWire link transmitter clock. If not using the wrapper or the internal reset generator feature, a clock per link is required. However, if the generic internalrstgen is set to 1, only the first element (LSB) of the array is required, and the same clock will be used for every link. Clock division is done locally.	-
TXCLKN [SPWPORTS-1:0]	N/A	Input	Transmitter inverted default run-state clock. Only used in DDR transmitter mode for technologies not supporting local generation of inverted clock. As for TXCLK, only the first element of the array is required if the internal reset generation is enabled.	-
TESTEN	N/A	Input	Scan test enable.	High
TESTRST	N/A	Input	Scan test reset.	Low
TESTIN	N/A	Input	Scan test data input	-

Table 1061. Signal descriptions

Signal name	Field	Type	Function	Active
DI[61:0]	N/A	Input	SpaceWire link data input vector. It should be connected to the number of GRSPW2_PHY entities corresponding to the number of SpaceWire links in the router. 1:0 go to link 0, 3:2 to link 1 etc.	-
DVI[61:0]	N/A	Input	SpaceWire link data valid input vector. It should be connected to the number of GRSPW2_PHY entities corresponding to the number of SpaceWire links in the router. 1:0 go to link 0, 3:2 to link 1 etc.	
DCONNECT [61:0]	N/A	Input	Disconnect vector. It should be connected to the number of GRSPW2_PHY entities corresponding to the number of SpaceWire links in the router. 1:0 go to link 0, 3:2 to link 1 etc.	
DCONNECT2 [61:0]			Copy of the signal DCONNECT as part of the Triple Modular Redundancy protection.	
DCONNECT3 [61:0]			Copy of the signal DCONNECT as part of the Triple Modular Redundancy protection.	
DO[61:0]	N/A	Output	Data output vector. In Cobham PHY mode two bits per link are used. 1:0 correspond to link 0, 3:2 to link 1 and so on. In the other two modes only the lower of the two bits in each pair are used.	
SO[61:0]	N/A	Output	Strobe output vector. In Cobham PHY mode two bits per link are used. 1:0 correspond to link 0, 3:2 to link 1 and so on. In the other two modes only the lower of the two bits in each pair are used.	
AHBMI	*	Input	AHB master in signals.	
AHBMO	*	Output	Vector of AHB master out signals. One set of signals for each AMBA port.	
AHBSI	*	Input	AHB slave in signals.	
AHBSO	*	Output	AHB slave out signals.	

Table 1061. Signal descriptions

Signal name	Field	Type	Function	Active
RI	RMAPEN[30:0]	Input	RMAP enable signal for each AMBA port. AMBA port 0 is connected to RMAPEN[0] and port 1 to [1] etc.	-
	IDIVISOR[7:0]	Input	Initialization divisor value for the SpaceWire links.	-
	TXWRITE[30:0]	Input	Transmitter FIFO write signals for the FIFO interfaces.	-
	TXCHAR[30:0][8:0]	Input	Transmitter character signals for the FIFO interfaces.	-
	RXREAD[30:0]	Input	Receiver FIFO read signals for the FIFO interfaces.	-
	TICKIN[30:0]	Input	Tick input signals for the FIFO and AHB interfaces	High
	TIMEIN[30:0][7:0]	Input	Time input signals for the FIFO and AHB interfaces.	-
	ENEXTTIME[30:0]	Input	Sets the reset value for the external time selection bit for FIFO interfaces. When 0 a tick-in on the corresponding TICKIN signal causes the internal time-counter to be incremented and the new value to be transmitted. When 1 the value from the TIMEIN signal will be used. In both causes the control flags are taken from TIMEIN[7:6].	High
	RELOAD[31:0]	Input	Prescaler default reload value (set during reset).	-
	RELOADN[9:0]	Input	Individual timer default reload value (set during reset).	-
	TIMEREN	Input	Sets the reset value for the timer enable bit in the port control registers..	-
	TIMECODEEN	Input	Enable time-code functionality. If 0 no time-codes will be propagated by the router. When 1 time-code functionality is enabled.	High
	CFGLOCK	Input	Lock configuration port accesses from all ports except port 1. When set to 0 the configuration port can be accessed from all ports (if not individually disabled through register). If set to 1 the configuration area can only be accessed from port 1 (the AHB slave interface is not affected byt this). The configuration enable bit for port 1 does not have any effect in this case.	High
	SELFADDREN	Input	Reset value for selfaddren register bit. This bit enables ports to address themselves i.e a packet received on a port will be transmitted on the same port. If not enabled the packet will be discarded with an invalid address error.	High
	LINKSTARTREQ	Input	Reset value for the linkstartreq register bit. When set ports will be automatically started (provided they are not disabled) if a packet needs to be transmitted on them.	
	AUTODCONNECT	Input	Reset value for the autodconnect register bit. When set ports started with the linkstartreq feature will automatically disconnect after a timeout period of no activity.	
	INSTANCEID	Input	Sets the reset value of the instance ID field of the version register.	

Table 1061. Signal descriptions

Signal name	Field	Type	Function	Active
RO	RXCHARAV[30:0]	Output	Receiver data available vector. One signal per FIFO port.	-
	RXAEMPTY[30:0]	Output	Receiver FIFO almost empty vector. One signal per FIFO port.	-
	TXFULL[30:0]	Output	Transmitter FIFO full vector. One signal per FIFO port.	-
	TXAFULL[30:0]	Output	Transmitter FIFO almost full vector. One signal per FIFO port.	-
	RXCHAR[30:0][8:0]	Output	Receiver FIFO character output vector. One character vector per FIFO port.	-
	TICKOUT[30:0]	Output	Tick out vector. One signal per FIFO or AMBA port.	High
	TIME-OUT[30:0][7:0]	Output	Time-code output vector. One time-code signal per FIFO or AMBA port.	-
	GERROR	Output	Global error. Asserted high when one or both of LERROR and MERROR are asserted.	High
	LERROR	Output	Asserted when one or more link errors have been detected on the SpaceWire ports. Asserted until the corresponding status bits have been c leared.	High
	MERROR	Output	Asserted when one or more uncorrectable parity errors have been detected in the on-chip memories. Asserted until the corresponding status bits have been cleared.	High
	LINKRUN[30:0]	Output	Each bit is asserted (set to 1) when the corresponding link is in run-state. Bit 0 corresponds to port 1, bit 1 to port 2 etc. This is only valid if the port is configured as a SpaceWire link.	
	RESET	Output	Signal which indicates that the SpW Router is globally reset. Its value is that of the bit 7 of the Router Configuration/Status register (offset: 0xA00). It shall be used to generate the resets of the core. This process is internally done by the wrapper grspwrouterm if the generic internalrstgen is set to 1.	Low
	RXRST[30:0]	Output	Internal reset generated by each SpW link transmitter for synchronization purpose between transmitter and both its receiver channels. It shall be used to generate the asynchronous and synchronous receiver resets of each port. This process can be skipped by activating the internal reset generation in the wrapper (internalrstgen set to 1).	High
	CLOCKGATE[30:0]	Output	Signal to indicate that the clocks for a specific link can be clockgated. They are used internally by the wrapper if the generic internalrstgen is set to 1.	High
* see GRLIB IP Library User's Manual				

62.11 Signal definitions and reset values

The signals and their reset values are described in table 1062.

*Table 1062.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
spw_clk	Input	Transmitter default run-state clock	Rising edge	-
spw_rxd	Input, LVDS	Data input, positive	High	-
spw_rxdn	Input, LVDS	Data input, negative	Low	-
spw_rxs	Input, LVDS	Strobe input, positive	High	-
spw_rxsn	Input, LVDS	Strobe input, negative	Low	-
spw_txd	Output, LVDS	Data output, positive	High	Logical 0
spw_txdn	Output, LVDS	Data output, negative	Low	Logical 1
spw_txs	Output, LVDS	Strobe output, positive	High	Logical 0
spw_txsn	Output, LVDS	Strobe output, negative	Low	Logical 1

62.12 Timing

The timing waveforms are shown in figure 179 and 180. Timing parameters are defined in table 1063 and 1064.

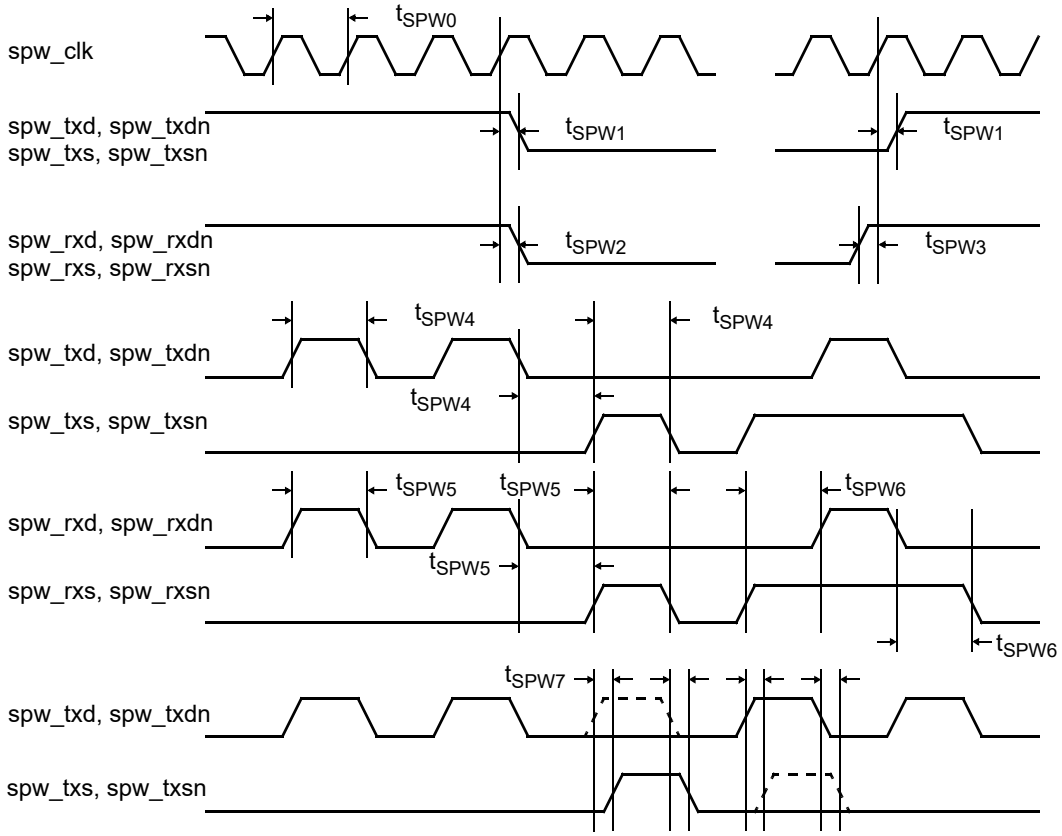


Figure 179. Timing waveforms

*Table 1063.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{SPW0}	transmit clock period	-	TBD	-	ns
t_{SPW1}	clock to output delay	rising *spw_clk* edge	TBD	TBD	ns
t_{SPW2}	input to clock hold	-	-	-	not applicable
t_{SPW3}	input to clock setup	-	-	-	not applicable
t_{SPW4}	output data bit period	-	-		*clk* periods
		-	t_{SPW0} - TBD	t_{SPW0} +TBD	ns
t_{SPW5}	input data bit period	-	TBD	-	ns
t_{SPW6}	data & strobe edge separation	-	TBD	-	ns
t_{SPW7}	data & strobe output skew	-	-	TBD	ns

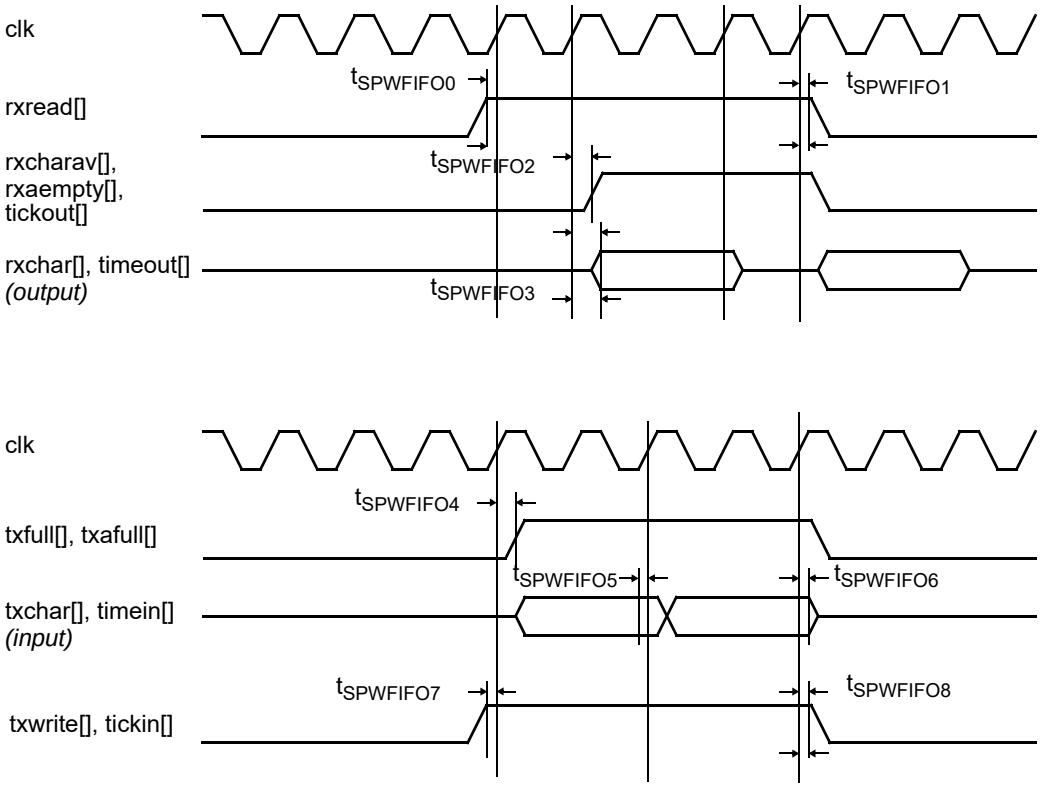


Figure 180. Timing waveforms - FIFO interface

*Table 1064.*Timing parameters - FIFO interface

Name	Parameter	Reference edge	Min	Max	Unit
$t_{SPWFIFO0}$	input to clock setup	rising clk edge	TBD	TBD	ns
$t_{SPWFIFO1}$	input from clock hold	rising clk edge	TBD	TBD	ns
$t_{SPWFIFO2}$	clock to output delay	rising clk edge	TBD	TBD	ns
$t_{SPWFIFO3}$	clock to rxchar, timeout output delay	rising clk edge	TBD	TBD	ns
$t_{SPWFIFO4}$	clock to output delay	rising clk edge	TBD	TBD	ns
$t_{SPWFIFO5}$	txchar, timein input to clock setup	rising clk edge	TBD	-	ns
$t_{SPWFIFO6}$	txchar, timein input from clock hold	rising clk edge	TBD	-	ns
$t_{SPWFIFO7}$	input to clock setup	rising clk edge	TBD	-	ns
$t_{SPWFIFO8}$	input from clock hold	rising clk edge	TBD	-	ns

62.13 Instantiation

This example of instantiation assumes that the router wrapper is used and the internal reset generators are automatically included. If the user prefers to generate the resets externally, it is advised to use the wrapper as a baseline to understand how some signals are taken into account for each clock domain.

```
-- Since the resets and clockgate are generated internally in the wrapper,
-- the only element from TXCLK and TXCLKN to be used is the bit '0' (spw_clk).
-- The others remain unconnected
txclk_array(0)                           <= spw_clkl;
txclkn_array(0)                          <= spw_clkln;
txclk_array(CFG_SPW_SPWPORTS-1 downto 1)  <= (others => '0');
txclkn_array(CFG_SPW_SPWPORTS-1 downto 1) <= (others => '0');

router0 : grspwrouterm
        generic map (
          input_type   => 0,
          output_type  => 0,
          rxtx_sameclk => 0,
          fifosize     => 64,
          tech         => CFG_SPW_TECH,
          scantest     => 0,
          techfifo     => CFG_SPW_TECHFIFO,
          ft           => 0,
          spwen        => 1,              -- Enable spacewire ports
          ambaen       => 1,              -- Enable AMBA interfaces
          fifoen       => 0,              -- Disable FIFO interfaces
          spwports     => CFG_SPW_SPWPORTS,
          ambaports    => 1,              -- Number of AMBA ports
          fifoports    => 0,              -- Number of FIFO ports
          arbitration  => 0,
          rmap         => CFG_SPW_RMAP,
          rmapcrc      => CFG_SPW_RMAPCRC,
          fifosize2    => 32,
          almostsize   => 1,              -- Only used for FIFO ports
          rxunaligned  => CFG_SPW_RXUNALIGNED,
          rmapbufs     => 4,
          dmachan      => 1,
          hindex       => 4,              -- Starting index
          pindex       => 10,             -- Starting index
          paddr        => 16#0d0#,        -- Starting base address
          pmask        => 16#ff0#,        -- Each reg base on 4 KiB boundary
          pirq         => 20,             -- Starting IRQ
          cfghindex    => 3,
          cfghaddr     => 16#800#,
          cfghmask     => 16#ff0#,
          ahbslven     => 1,
          timerbits    => 0,
          pnp          => 0,
          autoscrub    => 0,
          sim          => 0,              -- Simulation mode, not used
          dualport     => CFG_SPW_DUALPORT,
          charcntbits  => 0,              -- Character counters disabled
          pktcntbits   => 0,              -- Packet counters disabled
```

```
  prescalermin => 250,            -- Minimum value for writes to reload reg
  spacewired   => 1,
  interruptdist=> 2,
  apbctrl      => 0,
  rmapmaxsize  => 4,
  gpolbits     => 0,
  gpopbits     => 0,
  gpibits      => 0,
  customport   => 0,
  codecclkgate => 0,
  inputtest    => 0,
  porttimerbits=> 10,
  irqtimerbits => 10,
  auxtimeen    => 1,
  num_txdesc   => 64,
  num_rxdesc   => 128,
  auxasync     => 0)
port map(
  rst          => rstn,
  clk          => hclk,
  rst_codec    => (others => '0'), -- Resets generated internally
  clk_codec    => (others => '0'), -- Clockgate generated internally
  rxasyncrst   => (others => '0'), -- Resets generated internally
  rxsyncrst    => (others => '0'), -- Resets generated internally
  rxclk        => rxclko,
  txsyncrst    => (others => '0'), -- Resets generated internally
  txclk        => txclk_array,     -- Only the element 0 will be used (spw_clkl)
  txclkn       => txclkn_array,    -- Only the element 0 will be used (spw_clkln)
  testen       => testen,
  testrst      => testrst,
  scanen       => scanen,
  testoen      => testoen,
  di           => di,
  dvi          => dvi,
  dconnect     => dconnect,  -- From GRSPW2_PHY
  dconnect2    => dconnect2, -- From GRSPW2_PHY
  dconnect3    => dconnect3, -- From GRSPW2_PHY
  do           => do,
  so           => so,
  ahbmi        => ahbmi,
  ahbmo        => ahbmo,
  apbi         => apbi,
  apbo         => apbo,
  ahbsi        => ahbsi,
  ahbso        => ahbso,
  ri           => ri,
  ro           => ro,
  mtesti       => mtesti,
  mtesto       => mtesto,
  mtestclk     => mtestclk
  );
```

63 SPWTDP - SpaceWire - Time Distribution Protocol

63.1 Overview

This interface implements the SpaceWire - Time Distribution Protocol (TDP). The protocol provides capability to transfer time values and synchronise them between onboard users of SpaceWire network. The time values are transferred as CCSDS Time Codes and synchronisation is performed through SpaceWire Time-Codes. The core also provides datation services. The core operates in an AMBA APB bus system. The AMBA APB bus is used for configuration, control and status handling. The interface is coupled with a SpaceWire node with AMBA AHB master and RMAP target implementation.

63.2 Protocol

The initiator and target maintain their own time locally. The Time Distribution Protocol provides the means for transferring time of initiator to targets and for providing a synchronization point in time. The time is transferred by means of an RMAP write command carrying a CCSDS Time Code (time message). The synchronization event is signaled by means of transferring a SpaceWire Time-Code. The transfer of the SpaceWire Time-Code is synchronized with time maintained by the initiator. To distinguish which SpaceWire Time-Code is to be used for synchronization, the value of SpaceWire Time-Code is transferred from initiator to target by means of an RMAP write command prior to actual transmission of SpaceWire Time-Code itself. When there is more than one target the CCSDS Time Code need to be transferred to each individual target separately [SPWCUC].

63.3 Functionality

The block diagram below explains the complete system.

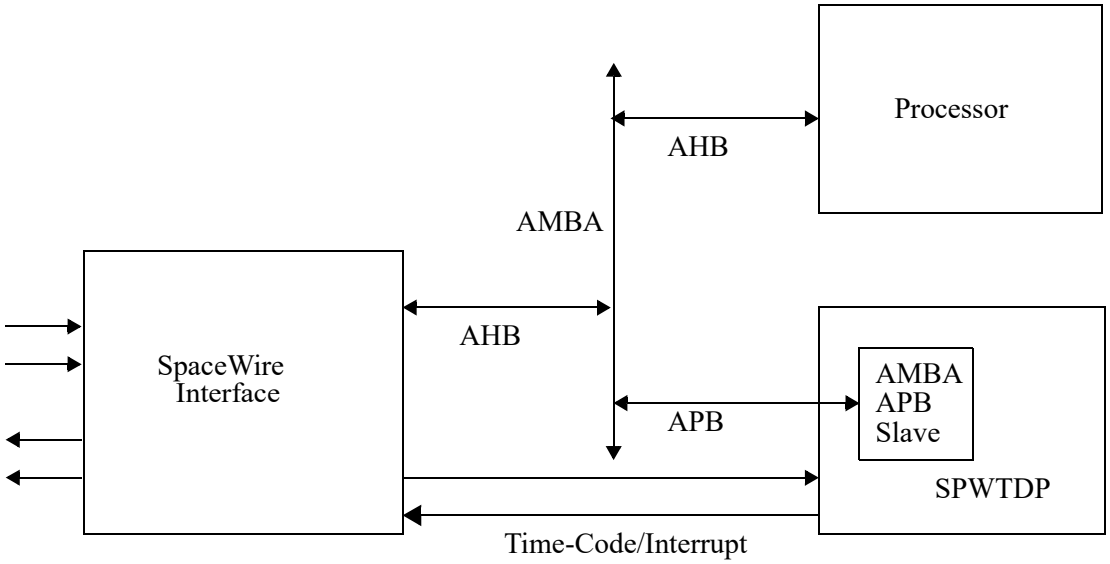


Figure 181. Block diagram

The foreseen usage of this core is to distribute and synchronise time between an initiator SPWTDP core and one or more target SPWTDP (slave) cores using the SpaceWire interface for communication between them.

The system can act as initiator (time master) and target being able to send and receive SpaceWire Time-Codes. The initiator requires SpaceWire link interface implements an RMAP initiator. The Target requires SpaceWire link interface implements an RMAP target. The SPWTDP component is a part of this system providing SpaceWire Time-Codes, CCSDS Time Codes, datation, time-stamping of

distributed interrupts, support for transmission of CCSDS Time Codes through RMAP and support for latency measurement and correction. In this implementation the CCSDS Time Codes carried between the SpaceWire network is based on CCSDS Unsegmented Code format (CUC) which is explained below [CCSDS]. The table below shows an example Preamble Field (P-Field) which corresponds to 40 bits of coarse time and 24 bits of fine time.

63.3.1 CCSDS Unsegmented Code: Preamble Field (P-Field)

*Table 1065.*CCSDS Unsegmented Code P-Field definition

Bit	Value		Interpretation
0	"1"		Extension flag, P-Field extended with 2nd octet
1-3	"010"	Agency-defined epoch (Level 2)	Time code identification
4 - 5	"11"	(number of octets of coarse time) + 1	Detail bits for information on the code
6 - 7	"11"	(number of octets of fine time)	
8	"0"		Extension flag, P-Field not extended with 3rd octet
9-10	"01"	Number of additional octets of the coarse time.	added to octet 1
11-13	"000"	Number of additional octets of the fine time.	added to octet 1
14-15			RESERVED

63.3.2 CCSDS Unsegmented Code: Time Field (T-Field)

For the unsegmented binary time codes described herein, the T-Field consists of a selected number of contiguous time elements, each element being one octet in length. An element represents the state of 8 consecutive bits of a binary counter, cascaded with adjacent counters, which rolls over at a modulo of 256.

*Table 1066.*Example CCSDS Unsegmented Code T-Field with 32 bit coarse and 24 bit fine time

CCSDS Unsegmented Code									
Preamble Field	Time Field								
	Coarse time						Fine time		
-	2^{31} 2^{24}	2^{23} 2^{16}	2^{15} 2^{8}	2^{7} 2^{0}	2^{-1} 2^{-8}	2^{-9} 2^{-15}	2^{-16} 2^{-24}		
0:15	0			31	32		55		

The basic time unit is the second. The T-Field coarse time (seconds) can be maximum 56 bits and minimum 8 bits. The T-Field fine time (sub seconds) can be maximum 80 bits and minimum of 0 bits.

The number of bits representing coarse and fine time implemented in this core can be obtained by reading the DPF bits of Datation Preamble Field register.

The coarse time code elements are a count of the number of seconds elapsed from the initial time value. This code is not UTC-based and leap second corrections do not apply according to CCSDS.

63.3.3 Time generation

The core consist of time generator which is the source for time in this system. The core may act as initiator or a target but both have their respective time generator. The Elapsed Time (ET) counter is implemented complying with the CUC T-Field. The number of bits representing coarse and fine time of a ET counter implemented in a design can be obtained by reading the DPF bits of Datation Preamble Field register.

The ET counter can be incremented either using an internal frequency synthesizer or by using an external enable signal. The External ET Increment Enable bit in Configuration 0 register must be enabled if external inputs are to be used.

Increment ET using internal frequency synthesizer:

The counter is incremented on the system clock only when enabled by the frequency synthesizer. The binary frequency required to determine the counter increment is derived from the system clock using a frequency synthesizer (FS). The frequency synthesizer is incremented with a pre-calculated increment value, which matches the available system clock frequency. The frequency synthesizer generates a tick every time it wraps around, which makes the ET time counter to step forward with the precalculated increment value. The output of frequency synthesizer is used for enabling the increment of ET counter. The increment rate of the ET counter and frequency synthesizer counter should be set according to the system clock frequency. The ET counter increment rate is set by providing values to ETINC bits in Configuration 2 register and frequency synthesizer counter is set by providing values to FSINC bits in Configuration 1 register. The following table specifies some example ETINC and FSINC values for some frequencies. The below values are also obtained for Coarse time width 32, Fine time width 24 and Frequency synthesizer width of 30. To calculate for other frequencies and configuration refer the spreadsheet provided along with this document.

*Table 1067.*Example values of ETINC and FSINC for corresponding frequencies

Frequency	ETINC	FSINC
50 MHz	0	360287970
250 MHz	0	72057594
33333333	2	135107990

Increment ET using external input:

The EP register in Configuration 0 specify whether to increment the ET counter based on rising or falling edge of the external enable signal. Also the ETINC bits in Configuration 2 register specify from which bit the ET counter must increment.

The following section describes the cores capabilities if it configured as initiator or target.

63.3.4 Initiator

An initiator is a SpaceWire node distributing CCSDS Time Codes and SpaceWire Time-Codes. It is also an RMAP initiator, capable of transmitting RMAP commands and receiving RMAP replies. There is only one active initiator in a SpaceWire network during a mission phase.

The initiator performs the following tasks

- Transmission of SpaceWire Time-Codes

The SpaceWire Time-Codes are provided by this component and transmission of those codes to targets should be performed by a SpaceWire interface.

- Transmission of CCSDS Time Codes through RMAP
- Datation, time-stamping and latency measurement

63.3.5 Target

A target is a SpaceWire node receiving CCSDS Time Codes and SpaceWire Time-Codes. A target is also an RMAP target, capable of receiving RMAP commands and transmitting RMAP replies. There can be one or more targets in a SpaceWire network.

The target performs the following tasks

- Reception of SpaceWire Time-Codes

The SpaceWire Time-Codes sent from initiator are received by SpaceWire interface and provided to this component in target.

- Reception of CCSDS Time Codes through RMAP
- Qualification of received time messages (CCSDS Time Codes) using SpaceWire Time-Codes
- Initialization and Synchronisation of received CCSDS Time Codes with Elapsed Time counter available in this component
- Datation, time-stamping and latency correction
- Jitter and drift mitigation (the MA bit in Status 0 register specify the availability of this service)

63.3.6 Configuring initiator and target

The core is interfaced via an AMBA Advanced Peripheral Bus (APB) slave interface, providing a register view that is compatible with the Time Distribution Protocol (TDP). The core must be configured according to the requirement either as initiator or target.

- Initializing initiator

The initiator transmits the SpaceWire Time-Codes out of the core only when the Transmit Enable TE bit in Configuration 0 register is enabled. The ET counter in initiator can be initialized (to provide any initial value). Initialization is done by writing a time value into the Command Elapsed Time registers available in the command field, the NC bit in the Control register of command field should be enabled to initialize the time value stored in the Command Elapsed Time registers to be the local time (Transmit Enable TE bit in Configuration 0 register must be enabled). The NC bit in the Control register will disable itself when the time is initialized. The INSYNC bit in Status 0 register will enable when initialization is performed. The MAPPING bits in Configuration 0 register determines the interval between SpaceWire Time-Code transmissions which is explained in detail in the section below.

The target time must be configured with time values from the initiator. The targets register space must be configured and controlled through RMAP by an initiator to achieve time synchronisation. The target time synchronisation is explained in detail under the section initialization and synchronisation of target through RMAP.

63.3.7 SpaceWire Time-Code

SpaceWire Time-Codes are continuously transmitted from an initiator node (time master) to all slave nodes. The transmission of the SpaceWire Time-Code is synchronized with the ET counter in the initiator node. The six bits of the Time-Code time information correspond to six bits of the local ET counter (MAPPING bits in Configuration 0 register determines its exact mapping and interval between SpaceWire Time-Code transmissions). Value of 0b00000 for MAPPING bits in Configuration 0 register will send SpaceWire Time-Code at every Second. When the value is 0b00001 SpaceWire Time-Codes are sent at every 0.5 Seconds interval and so on (maximum value of MAPPING can be 0b11111 but this value cannot be more than the number of bits implemented as fine time). The ET bits with lower weights than the size bits mapped to Time Codes time information bits are all zero at time of SpaceWire Time-Codes transmission. The Table below shows an example Local ET counter and Mapping. If the Coarse time is 32 bits and Fine time is 24 bits and mapping value is 6 then 0 to 31 is coarse(32 bits), 32 to 55 is fine time and mapped SpaceWire Time-Code is 32 to 37.

*Table 1068.*Example Local ET counter with Mapping values

0															25	26	27	28	29	30	31	32	33	34	35	36	37	38				55
Mapping Values																					0	1	2	3	4	5	6	7				24
If the Mapping value is 6 then the mapped SpaceWire Time-Codes is 32 to 37																						32	33	34	35	36	37					

*Table 1068.*Example Local ET counter with Mapping values

If the Mapping value is 0 then the mapped SpaceWire Time-Codes is 26 to 31	26	27	28	29	30	31											
If the Mapping value is 5 then the mapped SpaceWire Time-Codes is 31 to 36						31	32	33	34	35	36						
If the Mapping value is 7 then the mapped SpaceWire Time-Codes is 33 to 38								33	34	35	36	37	38				

63.3.8 Initialization and synchronisation of target through RMAP

An initiator must provide the time values and set the target in order to get the time synchronized. The below text explains how an initiator can synchronise the target.

The SPWTC in Control register of initiator core component should be configured initially with a SpaceWire Time-Code value at which the time message needed to be transferred. When the SpaceWire Time-Code generated internally using the ET counter matches the SPWTC in Control register a Time Message TM interrupt will be generated (TME bit Time Message Enable should be enabled in the Interrupt Enable register). Based on this interrupt the local time (ET counter) in initiator should be accessed from the Datation registers and used to calculate the time message needed to be transmitted.

- Time message generation

The Time message transmitted using RMAP should be an exact mapping of the Command field (explained under Registers section). The Time message transmitted should write the Command field available in target. Control register available in Command field specify weather the target should be initialized or synchronized, at which SpaceWire Time-Codes it should happen (synchronization event) and details of coarse and fine time available in the time message. The New code NC bit available in Control register should be enabled and if the target should be initialized then Init Sync IS bit in Control register must be enabled otherwise target will be synchronized.

The Command Elapsed Time in time message are calculated from the local time (ET counter) available in the initiator. The local time can be obtained by reading the Datation Field of initiator component. While reading the Datation registers always the total implemented coarse time and fine time must be read in order (from 0 till the implemented Datation Elapsed Time registers). The DPF of Datation Preamble Field register gives the coarse and fine time implemented which gives the total local ET counter (coarse + fine width).

For example if the implementation has 32 bit coarse and 24 bit fine time then it is enough to access the first two Datation Elapsed Time registers (0 and 1). The 32 bits of Datation Elapsed Time 0 and only the most significant 24 bits (31 to 8) of Datation Elapsed Time 1 registers (32 + 24 =56 bits) represents the local time. These 56 bits only be used for Command Elapsed time (time message) calculation.

The SpaceWire Time-Codes at which the Time Message interrupt generated is embedded in the local ET counter. The Command Elapsed time which is transmitted as time message should be an incremented time value of this SpaceWire Time-Code and Command Elapsed time bits with lower weights than the size bits mapped to SpaceWire Time-Code time information bits are all must be zero.

The incremented time value is to make the initialization or synchronisation of time message in target will happen after the reception of qualifying SpaceWire Time-Codes. The qualifying SpaceWire Time-Code is embedded in the Command Elapsed time (part of time message) sent from initiator. This qualifying SpaceWire Time-Code value should also be written in the SPWTC in Control section of the time message.

- Time qualification in target

In target, the Command field will contain the time message when it is written by the initiator through RMAP. When the SPWTC of Control register in Command field matches with a received SpaceWire Time-Code then initialization or synchronization will occur (according to NC bit and IS bit in the Control register) to the local ET counter of the target SPWTDP component. The Time message qualified TCQ bit in the status register will enable itself, this bit will disable itself when the conditions for

time message qualification is achieved (SPWTC of Control register matches with a received SpaceWire Time-Code) but no new time message is received (NC bit is zero). When the local ET counter is initialized or synchronized the NC bit in the control register will disable itself. The INSYNC bit in Status 0 register will enable when initialization is performed specifying the target is initialized. Initialization completely writes time message values into the implemented local Elapsed time counter and synchronisation verifies whether the time message Command Elapsed Time and local Elapsed Time counter matches till the mapped SpaceWire Time-Code level (with a tolerance of previous value) and only modifies the local Elapsed Time if their is a mismatch. If the target is not implemented with jitter and mitigation unit then the synchronisation forces the target time (ET counter) with the time message received.

For example, the initiator can create time message exactly at 0x00000001 coarse time and 0x040000 fine time (32 bit coarse time and 24 bit fine time, mapping value of 6 i.e. 64 SpaceWire Time-Codes per second, time message is generated at 0b000001 SpaceWire Time-Code), the value in the time message to be sent to the target can be coarse time 0x00000002 and 0x040000 fine time, (32 bit coarse time and 24 bit fine time, mapping value of 6, time message is qualified at the next reception of 0b000001 SpaceWire Time-Code, i.e. after a second). Both SPWTC in Control registers available in the initiator and target can be 0b000001 for this example. The time is synchronized after a second in this example. Depending on the frequency of SpaceWire Time-Codes and data link rate several different combination of ways to achieve time synchronisation is possible.

63.3.9 Latency measurement using Time-Stamps

The incoming and outgoing SpaceWire Distributed Interrupts are time stamped in initiator and target. The initiator calculates latency based on these time stamp values. The time stamped values in target are accessed from initiator through RMAP. The Latency Enable LE bit in Configuration 0 register must be enabled between the two nodes in the SpaceWire network for which the latency is to be calculated. The core supports 32 distributed interrupts and acknowledgment (Interrupt and acknowledgment numbers 0 to 31) or 64 distributed interrupts. The distributed interrupt transmission from initiator (which is the origin for latency calculation) is controlled by a mask register STM available in Configuration 3 register and SpaceWire time code register TSTC available in Time-Stamp SpaceWire Time-Code and Preamble Field Tx register, these registers specifies how often and at which time code distributed interrupt is transmitted and time stamping is performed.

The time stamping can be performed in two methods (only Interrupts or Interrupts and Acknowledgment), the DI bit in Configuration 3 register of SPWTDP component in target should be configured to specify which type of method is used. If only distributed interrupts (no acknowledgment) are used then DI bit should be 0. The transmitted and received distributed interrupts INTX and INRX in the Configuration 0 registers of both initiator and target must be configured with the interrupt number which will be used for the latency measurement. For example if the INTX in initiator Configuration 0 is configured with 0b00100 then the target INRX should be configured with the same value. Similarly if the INTX in target Configuration 0 is configured to be 0b00101 then the initiator INRX should be configured with the same value. Initially initiator sends a distributed interrupt when the conditions are matched (STM and TSTC registers match) and when the target received this distributed interrupt it will send another interrupt which will be received by the initiator. At each end transmission and reception is time stamped (current local time is stored in Time Stamp registers) and interrupt transmitted is INTX and received interrupt is checked whether it received INRX.

If both distributed interrupts and acknowledgment method is to be used then DI bit should be 1. The transmitted and received distributed interrupts INTX and INRX in the Configuration 0 registers of both initiator and target can have the same interrupt number (the acknowledgment number for a particular interrupt will be same as interrupt number). Similar to the previous method at each end transmission and reception is time stamped which will be used for latency calculations.

The Latency calculation can be started in initiator based on DIR (distributed interrupt received) interrupt available in Interrupt Status register (the interrupt should be enabled in the Interrupt Enable register). The latency is calculated form the time stamp registers based on the equation explained below

Latency = ((initiator time stamp Rx - initiator time stamp Tx) - (target time stamp Tx - target time stamp Rx)) /2

By calculating the Latency value repeatedly (at least for about 128 times, more number of times provides increased accuracy) and taking an average of it will provide the final latency value. The initiator should transfer the latency correction information to the Latency Field registers in the target by means of RMAP transfer. When the latency values are written it will be adjusted to local time in the target and the LC bit in Status 0 register is enabled (set to '1'), this status register can be disabled by writing '1' into the corresponding field.

63.3.10 Mitigation of jitter and drift

The Jitter and drift mitigation is performed in target when Jitter Enable JE and Mitigation Enable ME bit in Configuration 0 register is enabled. The process will only start when the target is initialized (the target local ET counter should have initialized through a time message from initiator and INSYNC bit in Status 0 register is enabled). The SPWTDP must have implemented with mitigation unit for jitter and drift mitigation (the MA bit in Status 0 register specify the availability of this service).

63.3.11 External Datation

The external signals latch and save are used to provide external datation services. The Elapsed Time is continuously latched when the latch input signal goes high, the corresponding External datation mask register must be enabled for that particular signal. When save input goes high the latched value will remain same (at when the previous latch condition met) and all the mask bit previously enabled will be cleared. The EDS bit in Status Register 0 will go high when the latch and save condition matches and cleared when the latched elapsed time is read. The purpose of this status register is to ensure that all the implemented coarse and fine time are read. Reading the lowest implemented fine time makes the status register to go low. An output pulse is also produced when conditions for external datation is met. The pulse is driven for one system clock period on the occurrence of external save condition.

If a simpler version of latching the time is needed based on a signal going high at any instance then the latch and save signals can be provided with the same input.

There are four External datation services implemented and each of them has its own mask EDMx, status EDS and time EDxETx registers. All the four External datation services are based on the input latch and save signal vectors. The external datation pulse vector consist of four outputs corresponding to each of the external datation services.

63.3.12 Pulses

The core provides eight external outputs used for clock pulse distribution. The timing of each pulse output is individually derived from the Elapsed Time counter. It is possible to program for each pulse output individually the following parameters:

- periodicity pulse
- width of pulse
- polarity of pulse
- enable/disable pulse generation (reset status is disabled)

The pulse has two parts, the active and the inactive part. The active part always starts the pulse, followed by the inactive part. The polarity or logical level of the active part is programmable. The inactive part takes the logical inversion of the active pulse, and is the default output from the generator when the pulse is not issued or the overall generation is disabled.

The periodicity of the pulse corresponds to one of the ET bits that can be selected in the range 27 to 2-8 seconds, providing a range from 128 seconds to 3,91 ms, i.e. 0,0078 to 256 Hz frequency. See register definition for details.

The width of the active part of the pulse corresponds to one of the ET bits that can be selected in the range 26 to 2-9 seconds, providing a range from 64 seconds to 1,95 ms. See register definition for details.

It is possible to generate a pulse that has a duty cycle of 50%. It is also possible to generate a pulse for which the active part is as short as 2^{-9} seconds, and its period is as high as 27 seconds. The effective duty cycle can be as low as $2^{-9}/27$ for the longest period, up to 50% for the shortest period of 2-8 seconds = 256 Hz. The duty cycle choice becomes more restricted as the frequency increases. Note that it is only possible to reduce the duty cycle in one direction: 50%/50%, 25%/75%... 1%/99%. The active part of the pulse can thus never be more than 50% of the cycle. It should be noted that the active pulse width must be at most 50% of the pulse period.

The pulse outputs are guaranteed to be spike free. If a pulse output is disabled by means of writing to the corresponding register (PDRx) (i.e. writing a zero to the Pulse Enable bit (PE)), the pulse output will be immediately driven to the inversion of the Pulse Level bit (PL), which corresponds to the level of the inactive part of the pulse. It is thus possible to modify immediately the pulse output by disabling it using the PE bit and then changing the PL bit, since the output will always drive the inversion of the PL bit while disabled.

An ongoing pulse output will be immediately disabled (the pulse output will be immediately driven to the inversion of the Pulse Level bit) if any external modification of the ET counter is triggered (for both master and slave) due to initialization/synchronisation or set using APB registers.

63.3.13 Set Elapsed Time using external input

The ET counter can be set using an external enable signal (configurable rising or falling edge, see register SP in Configuration 0 register). To set the ET counter the SE bit in configuration register must be enabled, the value to be loaded into the ET counter must be written into the Command Elapsed Time registers. The ARM bit field in the Status 0 register will set itself to ‘1’ when the first Command Elapsed Time register is written. After the occurrence of the external enable signal the value will be loaded into the ET counter and the ARM bit field in the Status 0 register will set itself to ‘0’. An interrupt can also be generated when the ET counter is loaded, the corresponding interrupt (Set ET External Interrupt Enable) must be enabled.

63.3.14 Multiple Port

It is possible to transmit or receive SpaceWire Time-Codes to multiple SpaceWire links. The Multiple port enable bit in the Configuration 0 register must be enabled, using the Inport and Outport fields in the Configuration 3 register the corresponding inputs and outputs can be enabled or disabled.

At every system clock (if the system is configured as target) all the enabled ports are monitored for a SpaceWire Time-Code input. If received the SpaceWire Time-Code is compared with the previously received Time-code. If the newly received Time-code is same as the previously received then no modification is performed other than updating the Received port RP register in Status 0. If an incremented Time-code is received then the corresponding Time-code is used for further processing (time qualification etc.). In all other case (Time-code - X or Time-code + X) the received Time code is stored (in previously received Time-code internal register, used for processing the next time-code) and an interrupt is generated if corresponding interrupt (Non consecutive SpaceWire Time-code Interrupt) bit is enabled. For all the Time-Code received the corresponding port in which it is received is updated at Received port RP register in Status 0.

The Inport and Outport fields also control the reception and transmission of Distributed interrupts. While performing latency calculation only one port must be enabled, since distributed interrupts cannot be filtered out based on increments like in SpaceWire Time-Codes.

Multiple port transmission can also be disabled and only one port can be used for transmission or reception using SEL register in Configuration 0.

63.3.15 Synchronisation of target using SpaceWire Time-Codes

It is possible to synchronise the target only using SpaceWire Time-Codes. A master sending SpaceWire Time-Codes (using its Elapsed time counter) at regular interval can synchronise the Elapsed time in the target. The frequency of Time-code transmission in the master and the frequency of (when to expect a) Time-code in the target must match, this can be achieved by setting the Mapping fields in the Configuration 0 register. The incoming SpaceWire Time-Codes and the Time-code position mapped in the target Elapsed Time is compared, if they match the bits available after the compared bits are made zero, if the local time map is less than one (External Time-code arrived early) then the bits available after the compared bits are made zero and the other part (including the mapped part) is incremented by one. If the above two cases occurred then the target time is in sync with the master time and the Insync bit in Status 0 register is enabled. If the incoming Time-code is in out of order (Non consecutive) then the synchronisation is stopped, the Insync bit in Status 0 register is disabled (but the local time keeps running) and an interrupt is generated if corresponding interrupt (Non consecutive SpaceWire Time-code Interrupt) bit is enabled.

63.4 Data formats

All Elapsed Time (ET) information is compliant with the CCSDS Unsegmented Code defined in [CCSDS] and repeated hereafter.

63.4.1 Numbering and naming conventions

Convention according to the CCSDS recommendations, applying to time structures:

- The most significant bit of an array is located to the left, carrying index number zero.
- An octet comprises eight bits.

*Table 1069.*CCSDS n-bit field definition

CCSDS n-bit field		
most significant		least significant
0	1 to n-2	n-1

Convention according to AMBA specification:

- The least significant bit of an array is located to the right, carrying index number zero.
- Big-endian support.

*Table 1070.*AMBA n-bit field definition

AMBA n-bit field		
most significant		least significant
n-1	n-2 down to 1	0

63.5 Reference documents

[CCSDS] Time Code Formats, CCSDS 301.0-B-4, www.CCSDS.org

[SPW] Space engineering: SpaceWire - Links, nodes, routers and networks, ECSS-E-ST-50-12C

[RMAP] Space engineering: SpaceWire - Remote memory access protocol, ECSS-E-ST-50-52C

[SPWCUC] High Accuracy Time Synchronization over SpaceWire Networks

63.6 Registers

The core is programmed through registers mapped into AMBA APB address space.

*Table 1071.*Registers

APB address offset	Register
0x000-0x00F	Configuration Field
0x000	Configuration 0
0x004	Configuration 1
0x008	Configuration 2
0x00C	Configuration 3
0x010 - 0x01F	Status Field
0x010	Status 0
0x014	Status 1
0x018	RESERVED
0x01C	RESERVED
0x020 - 0x03F	Command Field
0x020	Control
0x024	Command Elapsed Time 0
0x028	Command Elapsed Time 1
0x02C	Command Elapsed Time 2
0x030	Command Elapsed Time 3
0x034	Command Elapsed Time 4
0x038	RESERVED
0x03C	RESERVED
0x040 - 0x05F	Datation Field
0x040	Datation Preamble Field
0x044	Datation Elapsed Time 0
0x048	Datation Elapsed Time 1
0x04C	Datation Elapsed Time 2
0x050	Datation Elapsed Time 3
0x054	Datation Elapsed Time 4
0x058	RESERVED
0x05C	RESERVED
0x060 - 0x09F	Time-Stamp Field
0x060	Time-Stamp Preamble Field Rx
0x064	Time-Stamp Elapsed Time 0 Rx
0x068	Time-Stamp Elapsed Time 1 Rx
0x06C	Time-Stamp Elapsed Time 2 Rx
0x070	Time-Stamp Elapsed Time 3 Rx
0x074	Time-Stamp Elapsed Time 4 Rx
0x078	RESERVED
0x07C	RESERVED
0x080	Time-Stamp SpaceWire Time-Code and Preamble Field Tx
0x084	Time-Stamp Elapsed Time 0 Tx

APB address offset	Register
0x088	Time-Stamp Elapsed Time 1 Tx
0x08C	Time-Stamp Elapsed Time 2 Tx
0x090	Time-Stamp Elapsed Time 3 Tx
0X094	Time-Stamp Elapsed Time 4 Tx
0x098	RESERVED
0x09C	RESERVED
0x0A0-0x0BF	Latency Field
0x0A0	Latency Preamble Field
0x0A4	Latency Elapsed Time 0
0x0A8	Latency Elapsed Time 1
0x0AC	Latency Elapsed Time 2
0x0B0	Latency Elapsed Time 3
0x0B4	Latency Elapsed Time 4
0x0B8	RESERVED
0x0BC	RESERVED
0x0C0	Interrupt Enable
0x0C4	Interrupt Status
0x0C8	Delay Count
0x0CC	Disable Sync
0x0D0-0x0FF	RESERVED
0x100-0x18F	External Datation Field
0x100	External Datation 0 Mask
0x104	External Datation 1 Mask
0x108	External Datation 2 Mask
0x10C	External Datation 3 Mask
0x110-0x12F	External Datation 0 Time
0x110	External Datation 0 Preamble Field
0x114	External Datation 0 Elapsed Time 0
0x118	External Datation 0 Elapsed Time 1
0x11C	External Datation 0 Elapsed Time 2
0x120	External Datation 0 Elapsed Time 3
0x124	External Datation 0 Elapsed Time 4
0x128	RESERVED
0x12C	RESERVED
0x130-0x14F	External Datation 1 Time
0x150-0x16F	External Datation 2 Time
0x170-0x18F	External Datation 3 Time
0x190-0x19F	RESERVED
0x1A0-1BC	Pulse Definition Register 0 to 7
0x1C0-0x1FF	RESERVED

63.6.1 Configuration 0

*Table 1072.*0x000 - CONF0 - Configuration 0

31 25	24	23 21	20	19	18	17	16	15	14 13	12 8	7	6	5 4	3	2	1	0
RESERVED	JE	RES	ST	EP	ET	SP	SE	LE	AE	RES	MAPPING	TD	MU	SEL	ME	RE	TE	RS
0	0	0	0	1	0	1	0	0	0	0	*	0	0	0	0	0	0	0
r	rw	r	rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw

31: 25	RESERVED	
24:	JE	Jitter Correction Enable (only for target) The jitter correction process in target will start when this bit is enabled. (Mitigation Enable bit should also be enabled). Reset value: '0'. (valid only when Mitigation unit available)
23: 20	RESERVED	
21:	ST	Synchronisation using SpaceWire Time-Code Enable (only for target) Reset value: '0'.
20:	EP	External ET Increment Polarity. To select the rising or falling edge of the external enable signal to increment the Elapsed time. Value '1' Rising edge. Value '0' Falling edge. Reset value: '1'.
19:	ET	External ET Increment Enable. Enable to increment the Elapsed Time based on external signal. When disabled the internal frequency synthesizer is used to increment the Elapsed Time counter. Reset value: '0'.
18:	SP	Set ET External Polarity. To select the rising or falling edge of the external enable signal to load the Elapsed Time with the contents of the command field register. Reset value: '1'.
17:	SE	Set ET External Enable. Based on the external enable signal load the Elapsed Time with the contents of the command field register. Reset value: '0'.
16:	LE	Latency Enable. To calculate latency between an initiator and target this bit must be enabled in both of them. Reset value: '0'.
15:	AE	AMBA Interrupt Enable The interrupts (explained in interrupt registers) in this core will generate an AMBA interrupt only when this bit is enabled. Reset value: '0'
14 13	RESERVED	
12: 8	MAPPING	Defines mapping of SpaceWire Time-Codes versus CCSDS Time-code. Value 0b00000 will send SpaceWire Time-Codes every Second, Value 0b00001 will send SpaceWire Time-Codes every 0.5 Second, Value 0b00010 will send SpaceWire Time-Codes every 0.25 Second, Value 0b00011 will send SpaceWire Time-Codes every 0.125 Second Maximum value it can take is 0b11111 but this value cannot be more than the number of bits implemented as fine time. Reset value: Implementation dependent
7:	TD	Enable TDP when set. Reset value: '0'.
6:	MU	Multiple Port Enable. Reset value '0'.
5: 4	SEL	Select for SpaceWire Time-Codes and Distributed Interrupt transmission and reception, one of 0 through 3. Can be used only when Multiple Port MU is disabled. Reset value: 0b00
3:	ME	Mitigation Enable (only for target) The drift correction process in target will start when this bit is enabled. Reset value: '0'.(valid only when Mitigation unit available)
2:	RE	Receiver Enable (only for target) Reset value: '0'.
1	TE	Transmit Enable (only for initiator) Reset value: '0'.
0	RS	Reset core. Makes complete reset when enabled. Reset value: '0'.

63.6.2 Configuration 1

*Table 1073.*0x004 - CONF1 - Configuration 1

31 30 29	0
R	FSINC
0	0
r	rw

31: 30 RESERVED

29: 0 FSINC

Increment value of the Frequency Synthesizer which is added to the counter every system clock cycle. It defines the frequency of the synthesized reference time.

Refer the spreadsheet provided along with this document to obtain this value.

Reset value: Implementation dependent

All implemented registers are writable and readable.

63.6.3 Configuration 2

*Table 1074.*0x008 - CONF2 - Configuration 2

31	8	7	0
CV		ETINC	
*		*	
rw		rw	

31: 8 CV Compensation Value

Value added to FSINC for variations of drift of the target clock.(only for target)

Refer the spreadsheet provided along with this document to obtain this value.

This value also depends on the MAPPING value in configuration 0 register. Specify the needed MAPPING value in the spreadsheet while calculating this value.

Reset value: Implementation Dependent

(valid only when Mitigation unit available)

7: 0 ETINC Value of the Elapsed Time counter is to be incremented each time when the Frequency Synthesizer wraps around.

Refer the spreadsheet provided along with this document to obtain this value.

Reset value: Implementation dependent

63.6.4 Configuration 3

*Table 1075.*0x00C - CONF3 - Configuration 3

31 28	27 24	23 22	21 16	15 14	13	12	11	10	9 5	4 0
OUTPORT	INPORT	RESERVED	STM	RESERVED	DI64R	DI64T	DI64	DI	INRX	INTX
0	0	0	0	0	0	0	0	0	0	0
rw	rw	r	rw	r	rw	rw	rw	rw	rw	rw

31: 28	OUTPORT	Enable the corresponding output ports. The multiple port enable bit MU in Configuration 0 register must be enabled. Reset value: ‘0’
27: 24	INPORT	Enable the corresponding input ports. The multiple port enable bit MU in Configuration 0 register must be enabled. Reset value: ‘0’
23: 22	RESERVED	
21: 16	STM	SpaceWire Time-Code Mask Mask For TSTC register available at Time-Stamp SpaceWire Time-Code and Preamble Field Tx register. Value all bits zero will send Distributed interrupts at all SpaceWire Time-Codes irrespective of any values in TSTC register. Value all ones will send Distributed interrupts at complete match of SpaceWire Time-Code with TSTC register. (only for initiator)
15: 14	RESERVED	
13:	DI64R	The MSb for received Distributed Interrupt when interrupt numbers 32 to 63 is used. Possible only for DI = ‘0’ (only interrupt mode) and DI64 is enabled. Reset value: ‘0’
12:	DI64T	The MSb for transmitted Distributed Interrupt when interrupt numbers 32 to 63 is used. Possible only for DI = ‘0’ (only interrupt mode) and DI64 is enabled. Reset value: ‘0’
11:	DI64	Enable Distributed Interrupts 64, when set all 64 Distributed interrupt numbers can be used for latency calculation. Possible only for DI = ‘0’ (only interrupt mode). Reset value: ‘0’
10:	DI	Distributed Interrupt method, when set interrupt and acknowledge mode else only interrupt mode. (only for target) Reset value: ‘0’
9: 5	INRX	Interrupt Received.(Distributed) The distributed interrupt number received by initiator or target. Reset value: 0b000000
4: 0	INTX	Interrupt Transmitted.(Distributed) The distributed interrupt number transmitted by initiator or target. Reset value: 0b000000

63.6.5 Status Register 0

*Table 1076.*0x010 - STAT0 - Status Register 0

31	30 29	28	27 24	23	22 16	15 14	13 8	7 4	3	2	1	0
MA	RP	R	EDS	R	FW	RES	CW	RES	ARM	LC	TCQ	INSYNC
0	0	0	0	0	0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	wc	r	r

31: MA — Mitigation unit available

1 Drift and Jitter mitigation unit available in target

0 Not available

(only for target)

30: 29 Received Port — When multiple ports receive SpaceWire time-codes, this register specify on which port the SpaceWire Time-Code is received recently.

28: RESERVED

27: 24 EDS — External Datation Status

24: External Datation 0 Status bit

25: External Datation 1 Status bit

26: External Datation 2 Status bit

27: External Datation 3 Status bit

When conditions matched for external datation this bit will go high. This bit will go low when all the implemented time values are read.

23 RESERVED

22: 16 FW — Fine width of command CCSDS Time Code received. Calculated from Preamble field of Command Register.

15: 14 RESERVED

13: 8 CW — Coarse width of command CCSDS Time Code received, calculated from Preamble field of Command Register.

7: 4 RESERVED

3: ARM — This field is enabled when the command field register is written with the value to be loaded into the Elapsed time. The Set ET External Enable SE bit in the Configuration 1 must be enabled. When an external enable signal occurred and the command field register contents are loaded into the Elapsed time then this bit will get disabled.

2 LC — Latency Corrected (only for target)

This register can be cleared by writing value '1' to this field.

1 TCQ — Time message is qualified by SpaceWire Time-Codes.

0 INSYNC — In Sync at Time code level, enabled when time values are Initialized or Synchronized

63.6.6 Status Register 1

*Table 1077.*0x014 - STAT1 - Status Register 1

31 30 29	0
R	IV
0	*
r	r

31: 30 RESERVED

29: 0 IV — Increment Variation. The variation in FSINC while achieving the time synchronisation (only for target)

Reset value: Implementation dependent

(valid only when Mitigation unit available)

63.6.7 Control

*Table 1078.*0x20 - CTRL - Control

31	30	29 24	23 16	15 0
NC	IS	R	SPWTC	CPF
0	0	0	0	0
rw	rw	r	rw	rw

31:	NC	New Command
30:	IS	Init or Sync 1 Initialization of received time message 0 Synchronisation of received time message (only for target)
29: 24	RESERVED	
23: 16	SPWTC	SpaceWire Time-Code value used for initialization and synchronisation In initiator the SpaceWire Time-Codes generated internally using the local ET counter matches this register a Time Message TM interrupt will be generated which is used to send Time message over the SpaceWire network. In target this register should match the received SpaceWire Time-Code for time qualification.
15: 0	CPF	Command Preamble Field. The number of coarse and fine time available in Command Elapsed Time registers should be mentioned in this field. Based on this preamble field the target will initialize or synchronise the local ET counter.(only for target)

63.6.8 Command Elapsed Time 0

*Table 1079.*0x024 - CET0 - Command Elapsed Time 0

31 0
CET0
0
rw

31: 0	CET0	Command Elapsed Time 0 Initialize or Synchronise local ET counter value (0 to 31).

63.6.9 Command Elapsed Time 1

*Table 1080.*0x028 - CET1 - Command Elapsed Time 1

31 0
CET1
0
rw

31: 0	CET1	Command Elapsed Time 1 Initialize or Synchronise local ET counter value (32 to 63)

63.6.10 Command Elapsed Time 2

*Table 1081.*0x02C - CET2 - Command Elapsed Time 2

31	0
CET2	
0	
rw	

31: 0 CET2 Command Elapsed Time 2

Initialize or Synchronise local ET counter value (64 to 95).

63.6.11 Command Elapsed Time 3

*Table 1082.*0x030 - CET3 - Command Elapsed Time 3

31	0
CET3	
0	
rw	

31: 0 CET3 Command Elapsed Time 3

Initialize or Synchronise local ET counter value (96 to 127).

63.6.12 Command Elapsed Time 4

*Table 1083.*0x034 - CET4 - Command Elapsed Time 4

31 24	23 0
CET4	RESERVED
0	0
rw	r

31: 24 CET4 Command Elapsed Time 4

Initialize or Synchronise local ET counter value (128 to 135).

23: 0 RESERVED

63.6.13 Datation Preamble Field

*Table 1084.*0x040 - DPF - Datation Preamble Field

31 16	15 0
RESERVED	DPF
0	0x2F00
r	r

31: 16 RESERVED

15: 0 DPF Datation Preamble Field

The number of coarse and fine time implemented can be obtained from this Preamble Field.

63.6.14 Datation Elapsed Time 0

*Table 1085.*0x044 - DET0 - Datation Elapsed Time 0

31	0
DET0	
0	
r	

31: 0	DET0	Datation Elapsed Time 0 CCSDS Time Code value (0 to 31) of local ET counter value.

63.6.15 Datation Elapsed Time 1

*Table 1086.*0x048 - DET1 - Datation Elapsed Time 1

31	0
DET1	
0	
r	

31: 0	DET1	Datation Elapsed Time 1 CCSDS Time Code value (32 to 63) of local ET counter value.

63.6.16 Datation Elapsed Time 2

*Table 1087.*0x04C - DET2 - Datation Elapsed Time 2

31	0
DET2	
0	
r	

31: 0	DET2	Datation Elapsed Time 2 CCSDS Time Code value (64 to 95) of local ET counter value.

63.6.17 Datation Elapsed Time 3

*Table 1088.*0x050 - DET3 - Datation Elapsed Time 3

31	0
DET3	
0	
r	

31: 0	DET3	Datation Elapsed Time 3 CCSDS Time Code value (96 to 127) of local ET counter value.

63.6.18 Datation Elapsed Time 4

*Table 1089.*0x054 - DET4 - Datation Elapsed Time 4

31 24	23 0
DET4	RESERVED
0	0
r	r

31: 24 DET4 Datation Elapsed Time 4

CCSDS Time Code value (128 to 135) of local ET counter value.

23: 0 RESERVED

63.6.19 Time-Stamp Preamble Field Rx

*Table 1090.*0x060 - TRPFRx - Time-Stamp Preamble Field Rx

31 16	15 0
RESERVED	TRPF
0	0x2F00
r	r

31: 16 RESERVED

15: 0 TRPF Time stamp Preamble Field

The number of coarse and fine time implemented can be obtained from this Preamble Field.

63.6.20 Time Stamp Elapsed Time 0 Rx

*Table 1091.*0x064 - TR0 - Time Stamp Elapsed Time 0 Rx

31 0
TR0
0
r

31: 0 TR0 Time stamped local ET value (0 To 31) when distributed interrupt received.

63.6.21 Time Stamp Elapsed Time 1 Rx

*Table 1092.*0x068 - TR1 - Time Stamp Elapsed Time 1 Rx

31 0
TR1
0
r

31: 0 TR1 Time stamped local ET value (32 to 63) when distributed interrupt received.

63.6.22 Time Stamp Elapsed Time 2 Rx

*Table 1093.*0x06C - TR2 - Time Stamp Elapsed Time 2 Rx

31 0
TR2
0
r

31: 0 TR2 Time stamped local ET value (64 to 95) when distributed interrupt received.

63.6.23 Time Stamp Elapsed Time 3 Rx

*Table 1094.*0x070 - TR3 - Time Stamp Elapsed Time 3 Rx

31	0
TR3	
0	
r	

31: 0 TR3 Time stamped local ET value (96 to 127) when distributed interrupt received.

63.6.24 Time Stamp Elapsed Time 4 Rx

*Table 1095.*0x074 - TR4 - Time Stamp Elapsed Time 4 Rx

31 24	23 0
TR4	RESERVED
0	0
r	r

31: 24 TR4 Time stamped local ET value (128 to 135) when distributed interrupt received.

23: 0 RESERVED

63.6.25 Time-Stamp SpaceWire Time-Code and Preamble Field Tx

*Table 1096.*0x080 - TTPFTx - Time-Stamp SpaceWire Time-Code and Preamble Field Tx

31 24	23 16	15 0
TSTC	RESERVED	TTPF
0	0	0x2800
rw	r	r

31: 24 TSTC Time stamp time code

Time stamp on this time-code value, used for time stamping when this register matched with SpaceWire Time-Codes. The mask for this matching is available in configuration register 3. (only for initiator)

23: 16 RESERVED

15: 0 TTPF Time stamp Preamble Field

The number of coarse and fine time implemented can be obtained from this Preamble Field.

63.6.26 Time Stamp Elapsed Time 0 Tx

*Table 1097.*0x084 - TT0 - Time Stamp Elapsed Time 0 Tx

31	0
TT0	
0	
r	

31: 0 TT0 Time stamped local ET value (0 to 31) when distributed interrupt transmitted.

63.6.27 Time Stamp Elapsed Time 1 Tx

*Table 1098.*0x088 - TT1 - Time Stamp Elapsed Time 1 Tx

31	0
TT1	
0	
r	

31: 0 TT1 Time stamped local ET value (32 to 63) when distributed interrupt transmitted.

63.6.28 Time Stamp Elapsed Time 2 Tx

*Table 1099.*0x08C - TT2 - Time Stamp Elapsed Time 2 Tx

31	0
TT2	
0	
r	

31: 0 TT2 Time stamped local ET value (64 to 95) when distributed interrupt transmitted.

63.6.29 Time Stamp Elapsed Time 3 Tx

*Table 1100.*0x090 - TT3 - Time Stamp Elapsed Time 3 Tx

31	0
TT3	
0	
r	

31: 0 TT3 Time stamped local ET value (96 to 127) when distributed interrupt transmitted.

63.6.30 Time Stamp Elapsed Time 4 Tx

*Table 1101.*0x094 - TT4 - Time Stamp Elapsed Time 4 Tx

31 24	23 0
TTT0	RESERVED
0	0
r	r

31: 24 TT4 Time stamped local ET value (128 to 135) when distributed interrupt transmitted.

23: 0 RESERVED

63.6.31 Latency Preamble Field

*Table 1102.*0x0A0 - LPF - Latency Preamble Field

31 16	15 0
RESERVED	LPF
0	0x2F00
r	r

31: 16 RESERVED

15: 0 LPF Latency Preamble Field

The number of coarse and fine time implemented can be obtained from this Preamble Field. (only for target)

63.6.32 Latency Elapsed Time 0

*Table 1103.*0x0A4 - LE0 - Latency Elapsed Time 0

31	0
LE0	
0	
rw	

31: 0 LE0 Latency Value (0 to 31) written by initiator. (only for target)

63.6.33 Latency Elapsed Time 1

*Table 1104.*0x0A8 - LE1 - Latency Elapsed Time 1

31	0
LE1	
0	
rw	

31: 0 LE1 Latency Value (32 to 63) written by initiator. (only for target)

63.6.34 Latency Elapsed Time 2

*Table 1105.*0x0AC - LE2 - Latency Elapsed Time 2

31	0
LE2	
0	
rw	

31: 0 LE2 Latency Value (64 to 95) written by initiator. (only for target)

63.6.35 Latency Elapsed Time 3

*Table 1106.*0x0B0 - LE3 - Latency Elapsed Time 3

31	0
LE3	
0	
rw	

31: 0 LE3 Latency Value (96 to 127) written by initiator. (only for target)

63.6.36 Latency Elapsed Time 4

*Table 1107.*0x0B4 - LE4 - Latency Elapsed Time 4

31 24	23 0
LE4	RESERVED
0	0
rw	r

31: 24 LE4 Latency Value (128 to 135) written by initiator. (only for target)

23: 0 RESERVED

63.6.37 Interrupt Enable

*Table 1108.*0x0C0 - IE - Interrupt Enable

31 20	19	18 11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	NCTCE	PE(7-0)	SETE	EDIE3	EDIE2	EDIE1	EDIE0	DITE	DIRE	TTE	TME	TRE	SE
0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

31: 20	RESERVED	
19:	NCTCE	Non consecutive SpaceWire Time-Code received Interrupt Enable
18: 11	PE(7-0)	Pulse Interrupt Enable
10	SETE	Set ET External Interrupt Enable
9	EDIE3	External Datation 3 Interrupt Enable
8	EDIE2	External Datation 2 Interrupt Enable
7	EDIE1	External Datation 1 Interrupt Enable
6	EDIE0	External Datation 0 Interrupt Enable
5	DITE	Distributed Interrupt Transmitted Interrupt Enable
4	DIRE	Distributed Interrupt Received Interrupt Enable
3	TTE	SpaceWire Time-Code Transmitted Interrupt Enable (only for initiator)
2	TME	Time Message transmit Interrupt Enable (only for initiator)
1	TRE	SpaceWire Time-Code Received Interrupt Enable (only for target)
0	SE	Sync Interrupt Enable (only for target)

63.6.38 Interrupt Status

*Table 1109.*0x0C4 - IS - Interrupt Status

31 20	19	18 11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	NCTC	P(7-0)	SET	EDI3	EDI2	EDI1	EDI0	DIT	DIR	TT	TM	TR	S
0	0	0	0	0	0	0	0	0	0	0	0	0	0
r	wc	wc	wc	wc	wc	wc	wc	wc	wc	wc	wc	wc	wc

31: 20	RESERVED	
19:	NCTC	Generated when Non consecutive SpaceWire Time-Code is received
18: 11	P(7-0)	Generated when an active Pulse is transmitted, at the start of active pulse an interrupt is generated
10	SET	Generated when Elapsed Time is loaded with contents of the Command Field register based on external enable signal.
9	EDI3	Generated when conditions for External Datation 3 is matched
8	EDI2	Generated when conditions for External Datation 2 is matched
7	EDI1	Generated when conditions for External Datation 1is matched
6	EDI0	Generated when conditions for External Datation 0 is matched
5	DIT	Generated when distributed interrupt is transmitted (Latency calculation should be enabled)
4	DIR	Generated when distributed interrupt is Received (Latency calculation should be enabled)
3	TT	Generated when SpaceWire Time-Codes is transmitted (only for initiator)
2	TM	Generated when the conditions for transmitting time message occurred, based on this time message should be transmitted from initiator (only for initiator)
1	TR	Generated when SpaceWire Time-Code is received (only for target)
0	S	Generated when the target is initialized or synchronized with initiator (only for target)

The interrupts are cleared by writing value 1 on respective bits.

63.6.39 Delay Count

*Table 1110.*0x0C8 - DC - Delay Count

31 15	14 0
RESERVED	DC
0	0x7FFF
r	r

31: 15 RESERVED

14: 0 DC Delay Count

Delay induced between SpaceWire Time-Codes and Distributed Interrupt transmission in system clock units. The delay introduced is the value in this register multiplied by the system clock.

(only for initiator)

63.6.40 Disable Sync

*Table 1111.*0x0CC - DS - Disable Sync

31	30 24	23 0
EN	RESERVED	CD
0	0	0xFFFFFF
rw	r	rw

31: EN Enable

30: 24 RESERVED

23: 0 CD Configurable delay to capture missing SpaceWire Time-Code (only for target)

The INSYNC bit in the Status 0 register will disable itself when an expected SpaceWire Time-Code is not arrived after the delay mentioned in this register. The delay corresponds to the fine time of Elapsed Time counter and should not overlap with the MAPPING register. Any Overlapping register must also be set to Zero.

63.6.41 External Datation 0 Mask

*Table 1112.*0x100 - EDM0 - External Datation 0 Mask

31 0
EDM0
0
rw

31: 0 EDM0 External datation can be enabled by writing ‘1’ into the bit for that corresponding external input. When conditions are matched the Elapsed Time will be latched.

The latched values are available at External Datation 0 Time Register.

All the mask bits will go low after any one of the conditions with respect to the enabled mask bits.are matched.

63.6.42 External Datation 0 Preamble Field

*Table 1113.*0x110 - EDPF0 - External Datation 0 Preamble Field

31 16	15 0
RESERVED	EDPF0
0	0x2F00
r	r

*Table 1113.*0x110 - EDPF0 - External Datation 0 Preamble Field

31: 16	RESERVED	
15: 0	EDPF0	External Datation Preamble Field The number of coarse and fine time implemented can be obtained from this Preamble Field.

63.6.43 External Datation 0 Elapsed Time 0

*Table 1114.*0x114 - ED0ET0 - External Datation 0 Elapsed Time 0

31	0
ED0ET0	
0	
r	

31: 0	ED0ET0	External Datation Elapsed Time 0 Latched CCSDS Time Code value (0 to 31) of local ET counter.

63.6.44 External Datation 0 Elapsed Time 1

*Table 1115.*0x118 - ED0ET1 - External Datation 0 Elapsed Time 1

31	0
ED0ET1	
0	
r	

31: 0	ED0ET1	External Datation Elapsed Time 1 Latched CCSDS Time Code value (32 to 63) of local ET counter.

63.6.45 External Datation 0 Elapsed Time 2

*Table 1116.*0x11C - ED0ET2 - External Datation 0 Elapsed Time 2

31	0
ED0ET2	
0	
r	

31: 0	ED0ET2	External Datation 0 Elapsed Time 2 Latched CCSDS Time Code value (64 to 95) of local ET counter.

63.6.46 External Datation 0 Elapsed Time 3

*Table 1117.*0x120 - ED0ER3 - External Datation 0 Elapsed Time 3

31	0
ED0ET3	
0	
r	

31: 0	ED0ET3	External Datation 0 Elapsed Time 3 Latched CCSDS Time Code value (96 to 127) of local ET counter.

63.6.47 External Datation 0 Elapsed Time 4

*Table 1118.*0x124 - ED0ET4 - External Datation 0 Elapsed Time 4

31 24	23 0
ED0ET4	RESERVED
0	0
r	r

*Table 1118.*0x124 - ED0ET4 - External Datation 0 Elapsed Time 4

31: 24	ED0ET4	External Datation 0 Elapsed Time 4 Latched CCSDS Time Code value (128 to 135) of local ET counter.
23: 0	RESERVED	

63.6.48 Pulse Definition Register 0 to 7

*Table 1119.*0x1A0-0x1BC - PDR0 to PDR7 - Pulse Definition Register 0 to 7

31 24	23 20	19 16	15 11	10	9 2	1	0
RESERVED	PP	PW	RESERVED	PL	RESERVED	PE	R
0	0	0	0	1	0	0	0
r	rw	rw	r	rw	r	rw	r

31: 24	RESERVED	
23: 20	PP	Pulse Period Value ‘0000’ = 2^7 seconds Value ‘0001’ = 2^6 seconds ... Value ‘1110’ = 2^{-7} seconds Value ‘1111’ = 2^{-8} seconds Period = $2^{(7-PP)}$ Frequency = $2^{-(7-PP)}$
19: 16	PW	Pulse Width Value ‘0000’ = 2^6 seconds Value ‘0001’ = 2^5 seconds ... Value ‘1110’ = 2^{-8} seconds Value ‘1111’ = 2^{-9} seconds Width = $2^{(6-PW)}$
15: 11	RESERVED	
10:	PL	Pulse Level Defines logical level of active part of pulse output. ‘0’ = Low, ‘1’ = High
9: 2	RESERVED	
1:	PE	Pulse Enable ‘0’ = disabled, ‘1’ = enabled
0:	RESERVED	

Note: The registers which are not mentioned either as only for initiator or target are used in both initiator and target.

The Definition of External Datation 1 Mask, External Datation 2 Mask and External Datation 3 Mask registers are exactly same as External Datation 0 Mask Register.

The Definition of External Datation 1 Time, External Datation 2 Time and External Datation 3 Time registers are exactly same as External Datation 0 Time Registers (i.e. External Datation 0 Preamble Field and External Datation 0 Elapsed Time 0,1,2,3,4).

63.7 Vendor and device identifiers

The module has vendor identifier 0x01 and device identifier 0x097. For description of vendor and device identifiers see GRLIB IP Library User’s Manual.

63.8 Implementation

63.8.1 Reset

The core does not change reset behavior depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

63.9 Configuration options

Table below shows the configuration options of the core (VHDL generics).

*Table 1120.*Configuration options

Generic	Description	Allowed range	Default
mitigation	Jitter and drift correction unit enable	0-1	0
tech	Select technology	0-NTECH	inferred
gCoarse	Number of CUC coarse bits	8-56	32
gFine	Number of CUC fine bits	0-80	24
gMaster	Initiator implementation enable	0-1	1
gSlave	Target implementation enable	0-1	1
gFrequency	Width of Frequency Synthesizer	2-30	30
gFSIncrement	Increment of FS counter	0-0x3FFFFFFF	360287970
gETIncrement	Increment of ET counter	0-255	0
gComp	Compensation value for jitter and drift variations	0-0xFFFFFF	461
gPField	P-Field	0-0xAF7C	0x2F00
gMapping	Initial mapping value	0-31	6
gExtDatation	Implementation of External Datation	0-1	1
gNoExtDat	Number of External Datation services	1-4	4
gPulses	Pulse support	0-1	1
gNoPulses	Number of Pulse generation services	1-8	8
gMulEN	Multiple ports Enable	0-1	1
gNoPorts	Number of ports	1-4	4
gSetET	Set ET support	0-1	1
gExtETInc	Increment Elapsed Time based on external input	0-1	1
gSpWSync	Support for Synchronisation using only SpaceWire Time-Codes	0-1	1
delay	Number of Delay Count bits need to be implemented.	2-15	9
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	Addr field of the APB bar.	0 - 16#FFF#	0
pmask	Mask field of the APB bar.	0 - 16#FFF#	16#FFF#
pirq	Interrupt line used by the core.	0 - NAHBIRQ-1	1

63.10 Signal descriptions

Table below shows the interface signals of the core (VHDL ports).

*Table 1121.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
GRTDPI	tickindone	Input	SpaceWire Time-Code input processed	High
	tickoutraw	Input	SpaceWire Time-Code/Distributed interrupt output event	High
	timeout	Input	SpaceWire Time-Code/Distributed interrupt output	-
	ext_dat_latch	Input	Vector to input external signals on which the Elapsed Time is latched. Used for External datation service.	-
	ext_dat_save	Input	Vector to input external signals on which the Elapsed Time is saved. Used for External datation service.	-
	setet	Input	Input to set ET from Register	-
	ext_et_inc	Input	Input to increment ET	-
GRTDPO	tickinraw	Output	SpaceWire Time-Code/Distributed interrupt input request	High
	timein	Output	SpaceWire Time-Code/Distributed interrupt input	-
	elapsedtime	Output	Elapsed time	-
	enable	Output	TDP enable, this signal reflects the content of the TD bit in the Configuration 0 register.	High
	ext_dat_pulse	Output	Produces an output pulse when conditions for external datation is met. The pulse is driven for one system clock period on the occurrence of external save condition. This vector consist of four outputs corresponding to each external datation services.	-
	pulses	Output	Pulse output	-
DIAG_CTICK	N/A	Output	This tick is generated when SpaceWire Time-Code is transmitted in initiator. This tick is generated when a diagnostic SpaceWire Time-Code is generated from targets fully corrected time.	High
DIAG_JTICK	N/A	Output	The incoming SpaceWire Time-Code tick, to visualize the jitter (only for target)	High

* see GRLIB IP Library User's Manual

The inputs setet and ext_et_inc are re-synchronized internally. All the other inputs does not have internal support to remove meta-stability resulting from clock domain crossings. If the inputs are driven from clock domains other than the clock provided for this core then the clock synchronisation conditions must be dealt externally for these inputs.

63.11 Signal definitions and reset values

The core has no external signals.

63.12 Timing

The core has no external timing.

63.13 Library dependencies

Table 1122 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1122.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
TMTC	GRSPACE-WIRETDP	Signals, component	Component declarations, signals.
TMTC	SPACEWIRETDP	Signals, component	Component declarations, signals.

63.14 Instantiation

This example shows how the core can be instantiated.

```
library  ieee;
use      ieee.std_logic_1164.all;

library  grlib;
use      grlib.amba.all;
use      grlib.devices.all;
use      grlib.stdlib.all;

library  tmtc;
use      tmtc.grspacewiretdp.all;
use      tmtc.spacewiretdp.all;

entity grspwtdp_ex is

end entity grspwtdp_ex;

architecture rtl of grspwtdp_ex is

signal apbi            : apb_slv_in_type;
signal apbo            : apb_slv_out_vector := (others => apb_none);

signal spwi            : grspw_in_type;
signal spwo            : grspw_out_type;

signal tdpi            : grtdp_In_Type;
signal tdpo            : grtdp_Out_Type;
signal tdp_enable      : Std_ULogic;
signal tdp_elapsedtime : Std_Logic_Vector(0 to 135);
signal ext_dat_latch   : Std_Logic_Vector(31 downto 0);
signal ext_dat_save    : Std_Logic_Vector(31 downto 0);
signal tdp_elapsedtime : Std_Logic_Vector(0 to 135);
signal ext_dat_pulse   : Std_Logic_Vector(3 downto 0);
signal pulses          : Std_Logic_Vector(7 downto 0);
signal setet           : Std_ULogic;
signal ext_et_inc      : Std_ULogic;

signal diag_ctick      : Std_ULogic;
signal diag_jtick      : Std_ULogic;


begin

spw_time_0: grspwtdp
  generic map(
     mitigation         => 1,
     tech               => 0,
```

```
      gCoarse           => 32,
      gFine             => 24,
      gMaster           => 1,
      gSlave            => 1,
      gFrequency        => 30,
      gETIncrement      => 0,
      gFSIncrement      => 360287970, -- Default for 50 Mhz
      gComp             => 461,
      gPField           => 16#2F00#,
      gMapping          => 6,
      delay             => 9,
      pindex            => 4,
      paddr             => 4,
      pmask             => 16#ffe#,
      pirq              => 1)
  port map(
      rstn              => rstn,
      clk               => clkm,
      apbi              => apbi,
      apbo              => apbo(4),
      grtdpi            => tdpi,
      grtdpo            => tdpo,
      diag_ctick        => diag_ctick,
      diag_jtick        => diag_jtick);

spwi.timein             <= tdpo.timein;
spwi.tickinraw          <= tdpo.tickinraw(0);
tdp_elapsedtime         <= tdpo.elapsedtime;
tdp_enable              <= tdpo.enable;
ext_dat_pulse           <= tdpo.ext_dat_pulse;
pulses                  <= tdpo.pulses;

tdpi.tickindone(0)      <= spwo.tickindone;
tdpi.tickoutraw(0)      <= spwo.tickoutraw;
tdpi.timeout(0)         <= spwo.timeout;
tdpi.ext_dat_latch      <= ext_dat_latch;
tdpi.ext_dat_save       <= ext_dat_save;
tdpi.setet              <= setet;
tdpi.ext_et_inc         <= ext_et_inc;
end;
```

64 GRSPFI_CODEC - SpaceFibre encoder/decoder

64.1 Overview

SpaceFibre is a high-speed serial link mainly designed for payload data processing applications on board spacecraft. Like many other modern network architectures, SpaceFibre utilises a Serialiser/ Deserialiser (SerDes) circuit at its physical layer, allowing data rates of 2 Gbit/s and more. The SerDes can either be part of the chip design or a standalone device can be used.

Interfacing a SpaceFibre port from the user application is simple as it closely follows the procedure known from SpaceWire. A SpaceFibre port has one or more pairs of transmit and receive buffers, referred to as virtual channels, and each virtual channel acts like a single SpaceWire interface, i.e. several SpaceWire network streams can be multiplexed into one SpaceFibre network stream. The multiplexer is called medium access controller and is choosing the active virtual channel according to a number of Quality-of-Service (QoS) rules.

Data is always transferred in frames with a size of 256 bytes or less. While such a data frame is passed to the physical link, it is also stored in an error recovery buffer. It remains in this buffer until the far end node acknowledges the correct reception of the frame, which is detected by checking a CRC checksum at the end of the frame. However, if the far end node sends a negative-acknowledgement (NACK) word instead, the frame is re-transmitted from the error-recovery buffer.

Aside from data frames, SpaceFibre also supports broadcast frames, which are multi-purpose high-priority messages. These messages are comparable to SpaceWire time-codes but in addition to a simple sequence number they also transmit a data payload of 8 bytes. Broadcast frames are stored in the replay buffer just like the data frames, i.e. they are automatically retransmitted after a link error.

On the receive side, incoming data from the physical link is processed continuously, i.e. one 32-bit word is processed every clock cycle. To avoid buffer overruns in the virtual channel receive buffers, the communication between a virtual channel transmit buffer in the local node and the virtual channel receive buffer in the far end node is flow-controlled by means of Flow Control Token (FCT) words. Just like the data and broadcast frames, the FCT words are stored in the error-recovery buffer and are therefore retransmitted in case of errors.

A simplified block diagram of the SpaceFibre IP core can be seen in Figure 182. The SpaceFibre IP port comprises a data link layer and lane layer. Internally, the data link layer is further divided into the so-called broadcast layer, virtual channel layer and retry layer, which are responsible for the transmission and reception of broadcast frames, for the transmission and reception of data frames and for the error recovery mechanism, respectively.

Signals related to the broadcast interface have the prefix 'bc', signals related to the virtual channel interface the prefix 'vc', and signals related to the SerDes the prefix 'se'. Furthermore, the prefix 'cf' describes a configuration parameter signal whereas the prefix 'sr' describes a status register signal.

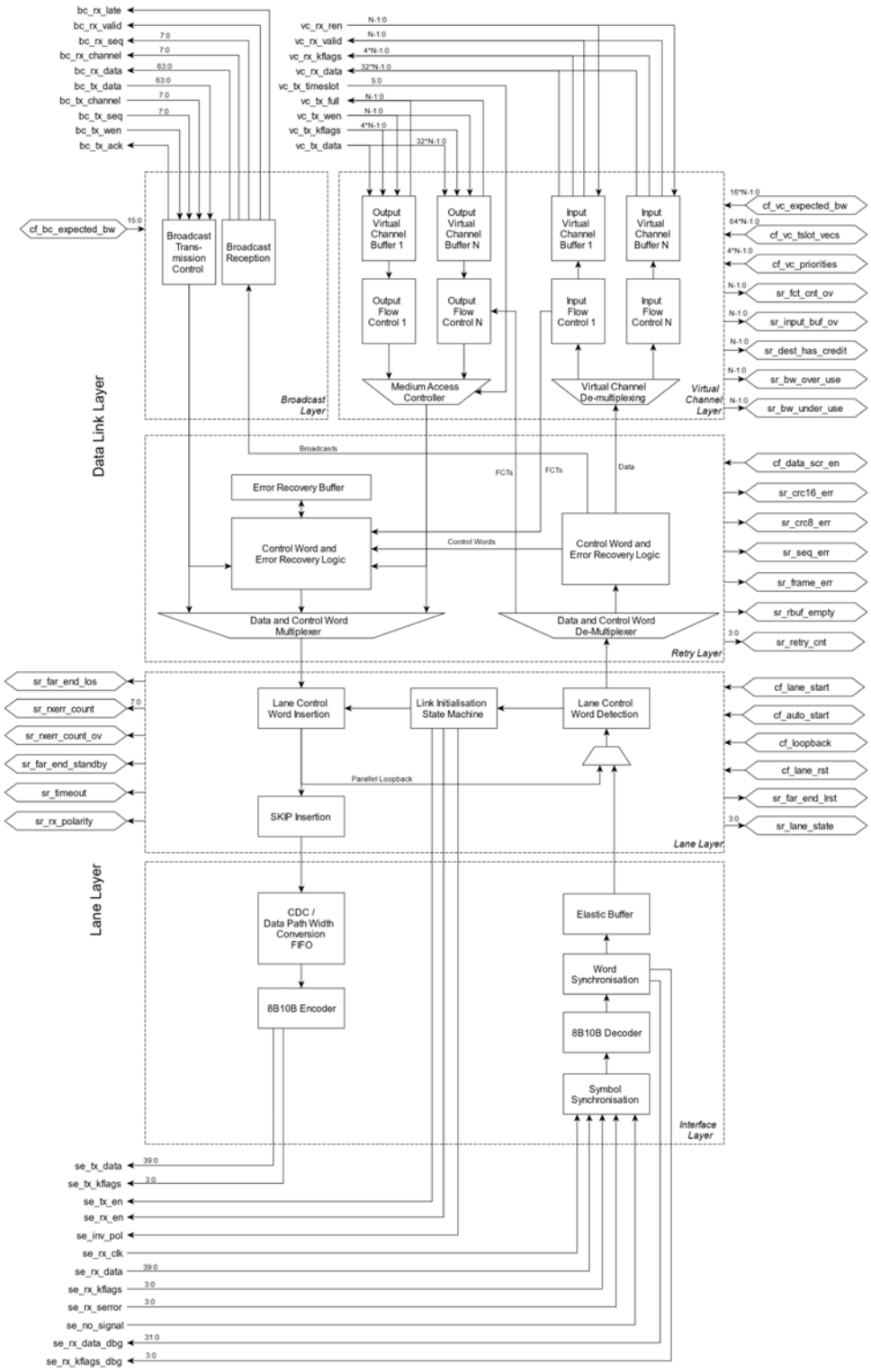


Figure 182. Block diagram

64.2 Operation

64.2.1 Configuration

All soft configuration parameters are synchronous to clock *clk* and should be stored in registers external to the SpaceFibre IP core.

Global configuration

The SpaceFibre link can be reset by asserting *cf_link_rst*. As a consequence, outbound packets are spilled up to and including the next EOP and inbound packets are terminated by an EEP.

Lane Layer

The lane initialization state machine is controlled with the signals *cf_lane_start* and *cf_auto_start*. When *cf_lane_start* is asserted, the lane layer will actively try to build up a connection with the far end by sending out INIT1 words. When *cf_auto_start* is asserted, the lane layer will passively listen to incoming words from the far end and start the handshake procedure once INIT1 words are received. *cf_lane_start* has higher precedence than *cf_lane_auto_start*. To shut down the lane, both *cf_lane_auto_start* and *cf_lane_start* must be de-asserted. When shut down, the transmitter and receiver parts of the SerDes are disabled as well.

The lane can be reset at any time by asserting *cf_lane_rst*. In contrast to link resets, a lane reset is only reinitialising the lane. Therefore, ongoing transmissions are probably delayed but never canceled.

The SpaceFibre IP core has an internal loop-back feature that can be enabled/ disabled with *cf_la_loopback*. The SpaceFibre IP core must be reset after asserting/de-asserting this flag.

Retry Layer

The retry layer comprises a data scrambler, which can be enabled/disabled with *cf_data_scr_en*. The data scrambler becomes directly active after asserting this flag. This will lead to continuous data retries if the de-scrambler of the remote node is not activated. Therefore, a lane reset must be triggered after asserting/de-asserting this flag. By doing so, the remote node is informed during the subsequent handshake if the data is scrambled or not and will then switch on or off the de-scrambler accordingly.

Broadcast Layer

The transmission of broadcasts is limited in bandwidth depending on an expected bandwidth value defined by the 16-bit wide port *cf_bc_expected_bw*. Typical values are between 1% and 95%. If the user application tries to send more broadcasts than allowed, the bandwidth limitation becomes automatically active. *cf_bc_expected_bw* is expressed in 0.16 fixed point format and is calculated as follows:

$$ExpectedBandwidth = \frac{1}{Percentage \cdot 4}$$

For example, the expected bandwidth value of 10% is expressed as: 1/(10*4) = 0.025. In 0.16 fixed point notation: 0x0666. For convenience, these values are pre-calculated for 1% to 95% and stored in a constant array in the package file spfi_pkg.vhd. The transmission of broadcasts can also be completely switched off by setting the expected bandwidth value to 0x0000.

Virtual Channel Layer

The transmission of data frames is bandwidth-limited for each virtual channel. The expected bandwidth values for all virtual channels are concatenated in port vector cf_vc_expected_bw. Each expected bandwidth value is 16-bit wide. For instance, the value for virtual channel 0 is stored at bit positions 15:0 and the value for virtual channel 1 is stored at bit positions 31:16. The expected bandwidth values are expressed in 8.8 fixed point format and are calculated as follows:

$$ExpectedBandwidth = \left|1 - \frac{100}{Percentage}\right|$$

For example, the expected bandwidth value of 15% is expressed as: abs(1-(100/15)) = 5.6667. In 8.8 fixed point notation: 0x05ab. For convenience, these values are pre-calculated for 1% to 95% and stored in a constant array in the package file spfi_pkg.vhd. A virtual channel can also be completely switched off by setting its expected bandwidth value to 0x0000.

The timeslot vectors for all virtual channels are concatenated in port vector *cf_vc_tslot_vecs*. Since SpaceFibre offers 64 timeslots per virtual channel, the timeslot vector for virtual channel 0 is stored at bit positions 63:0, the timeslot vector for virtual channel 1 at bit positions 127:0 and so on. Each bit enables or disables the transmission of data frames in the timeslot with the number of the bit position. For instance, to allow virtual channel 0 to send data in timeslot 0, timeslot 3 and timeslot 7, one can set its timeslot vector to: 0b10001001 = 0x89.

The priority values for all virtual channels are concatenated in port vector *cf_vc_priorities*. Each priority value is 4-bit wide, i.e. the priority levels 0 to 15 are supported. For instance, the value for virtual channel 0 is stored at bit positions 3:0 and the value for virtual channel 1 is stored at bit positions 7:4. Priority level 15 has the lowest precedence and priority level 0 has the highest precedence.

64.2.2 Status signaling

Lane Layer

The status flag *sr_far_end_lrst* is pulsed high if a link reset was triggered due to a system reset in the far end node. *sr_far_end_los* is pulsed if a new handshake is started due to a loss of signal at the SerDes receiver. *sr_rxerr_count* is an 8-bit wide counter for received RXERR words. The counter is automatically decreased by one every time 16,384 more words have been received. *sr_rxerr_count_of* is pulsed when the RXERR word counter overflows. *sr_rx_polarity* is set when the lane layer detects inverted receive polarity during handshake. If internal 8B10B decoding is activated, the polarity of the incoming bitstream is automatically inverted.

sr_far_end_standby is pulsed when STANDBY words are received. This is always the case when the link initialization state machine in the far end node is deactivated. *sr_timeout* is set when a connection timeout occurs during lane initialization. *sr_lane_state* is a 4-bit wide unsigned value encoding the current lane initialization state as follows:

*Table 1123.*Lane initialization state encoding

1	Clear Line
2	Disabled
3	Wait
4	Started
5	Invert Rx Polarity
6	Connecting
7	Connected
8	Active
9	Loss Of Signal
10	Prepare Standby

Retry Layer

sr_crc16_err is pulsed when a CRC error has occurred during the reception of a data frame. *sr_crc8_err* is pulsed when a CRC error has occurred during the reception of a control word or broadcast frame. *sr_seq_err* is pulsed when a sequence number error occurred during the reception of data frames, broadcast frames, idle frames, FCT or FULL words. *sr_frame_err* is pulsed when an invalid data, broadcast, or idle frame is received.

sr_rbuf_empty is set when the error recovery buffer is empty, i.e. all data frames, broadcast frames and FCT words have been sent and acknowledged. *sr_retry_cnt* is an 4-bit wide counter that increments for every RETRY event initiated. It is automatically reset when an ACK word is received from the far end. The SpaceFibre link is automatically reset when the counter reaches 16.

Virtual Channel Layer

sr_fct_cnt_ov is a bit vector where each bit position corresponds to a virtual channel number. The bit is pulsed when the corresponding FCT credit counter has overflowed. This indicates that the width of the FCT counter, defined by *g_remote_fct_cnt_max*, is too small. *sr_input_buf_ov* is a bit vector where each bit position corresponds to a virtual channel number. The bit is set when a virtual channel input buffer is receiving data when it is full. This indicates a fatal protocol error. *sr_dest_has_credit* is a bit vector where each bit position corresponds to a virtual channel number. The bit is set when there is space in the virtual channel input buffer of the far end node. *sr_bw_over_use* is a bit vector where each bit position corresponds to a virtual channel number. The bit is set when the virtual channel uses more bandwidth than expected, i.e. when the bandwidth overuse mechanism is active. In contrast, *sr_bw_under_use* indicates that a virtual channel uses less bandwidth than expected. Note that this flag is also set when a virtual channel is deactivated due to an expected bandwidth value of 0, even if the user application tries to transmit data over this virtual channel.

64.2.3 Virtual channel interface

Transmit side

On port *vc_tx_data*, data is fed into the virtual channel transmit buffers. The input vectors are 32-bit wide and concatenated, i.e. the data word for virtual channel 0 is stored at bit positions 31:0, the data word for virtual channel 1 is stored at bit positions 63:32 and so on. The lowest byte is transmitted first. On port *vc_tx_kflags*, a 4-bit vector for each virtual channel defines which bytes of the data transmit word are k-codes. The vectors are concatenated as well, i.e. the k-flags vector for virtual channel 0 is stored at bit positions 3:0, the k-flags vector for virtual channel 1 is stored at bit positions 7:4 and so on. The lowest bit in the k-flags vector corresponds to the lowest byte of the data word. The following k-codes are allowed:

*Table 1124.*SpaceFibre k-codes

SpaceFibre Character	K-Code	Corresponding data byte
EOP – End of packet	K29.7	0xFD
EEP – Error end of packet	K30.7	0xFE
FILL – Fill character	K27.7	0xFB

An example of how to use the k-codes correctly is shown in figure 183. The first four lines are normal data words, which are part of the payload of a SpaceWire packet. The k-flags vector must be set to 0b0000. In line 5, the SpaceWire packet is terminated by an EOP. Due to the byte-order, the k-code for the EOP is transmitted as least significant byte. The EOP is followed by three FILL characters for achieving word alignment. The k-flags vector must be set to 0b1111 because all bytes of the word are k-codes. In line 6, a new SpaceWire packet begins, starting with physical address 0x08. The address is transmitted as most significant byte since three FILL characters must be transmitted first. Here, the k-flags vector must be set to 0b0111 because only the FILL characters are k-codes.

Usage of any other k-codes than the aforementioned ones for EOP, EEP an FILL characters must be avoided. SpaceFibre uses k-codes for control words on lower protocol layers. Injecting the wrong combination of k-codes through the virtual channel interface can compromise the correct functionality of the SpaceFibre protocol.

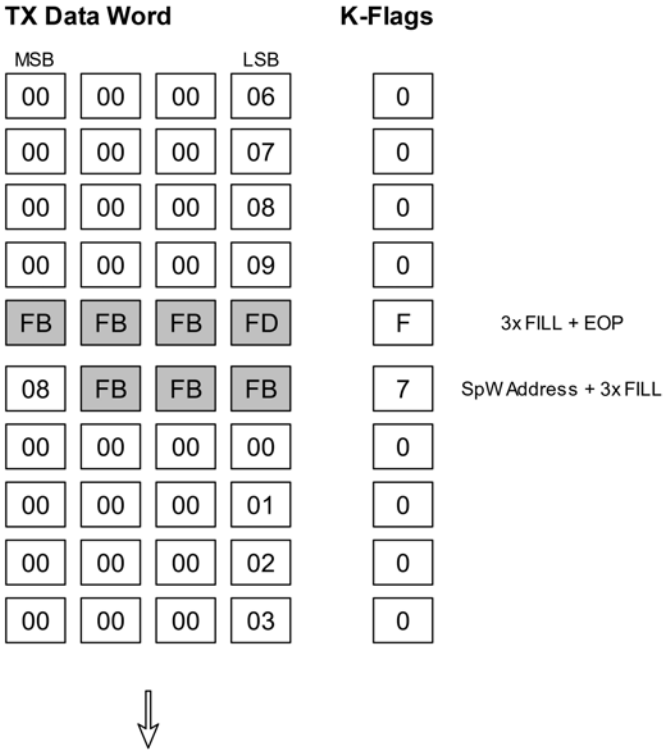


Figure 183. Example of k-code usage

To write into a virtual channel transmit buffer, the write enable flag for the virtual channel in bit vector *vc_tx_wen* must be asserted. The bit position corresponds to the virtual channel number. If the transmit buffer is full, the full flag for the virtual channel in bit vector *vc_tx_full* is asserted. Again, the bit position of the flag corresponds to the virtual channel number. If the transmit buffer is full, any further write attempts are ignored. An example timing diagram for virtual channel 0 is shown in figure 184.

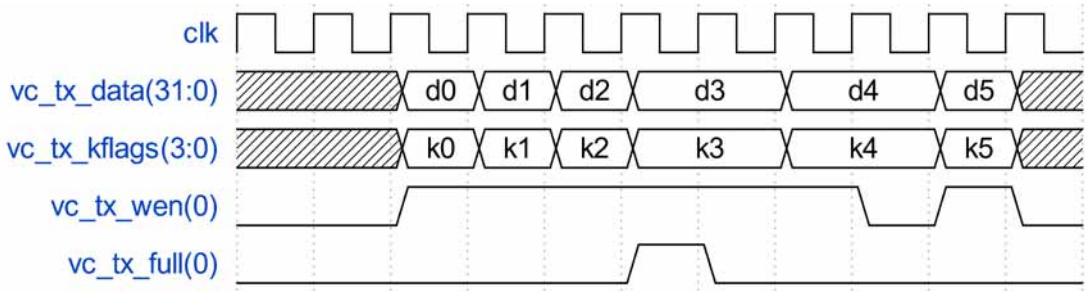


Figure 184. Example timing diagram - virtual channel 0 transmit side

The medium access controller allows the assignment of virtual channels to specific timeslots. *vc_tx_timeslot* is a 6-bit wide unsigned value defining the current timeslot number between 0 and 63.

Receive side

On port *vc_rx_data*, data is read out from the virtual channel input buffers. The output vectors are 32-bit wide and concatenated, i.e. the data word for virtual channel 0 is stored at bit positions 31:0, the

data word for virtual channel 1 is stored at bit positions 63:32 and so on. The lowest byte is the one received first. On port *vc_rx_kflags*, a 4-bit vector for each virtual channel defines which bytes of the received data word are k-codes. The vectors are concatenated as well, i.e. the k-flags vector for virtual channel 0 is stored at bit positions 3:0, the k-flags vector for virtual channel 1 is stored at bit positions 7:4 and so on. The lowest bit in the k-flags vector corresponds to the lowest byte of the data word. The same k-codes as described in table 1124 can occur, i.e. EOP, EEP and FILL characters.

To read from a virtual channel receive buffer, the read enable flag for the virtual channel in bit vector *vc_rx_ren* must be asserted. The bit position corresponds to the virtual channel number. Data on *vc_rx_data* is only valid if the corresponding valid flag in bit vector *vc_rx_valid* is asserted. Again, the bit position corresponds to the virtual channel number. This FIFO scheme makes it particularly easy to interface other FIFO-like interfaces in the user logic. For instance, one could loopback the received data to the transmit side by simply connecting *vc_tx_data* to *vc_rx_data*, *vc_tx_kflags* to *vc_rx_kflags*, *vc_tx_wen* to *vc_rx_valid* and *vc_rx_ren* to not(*vc_tx_full*). An example timing diagram is shown in figure 185.

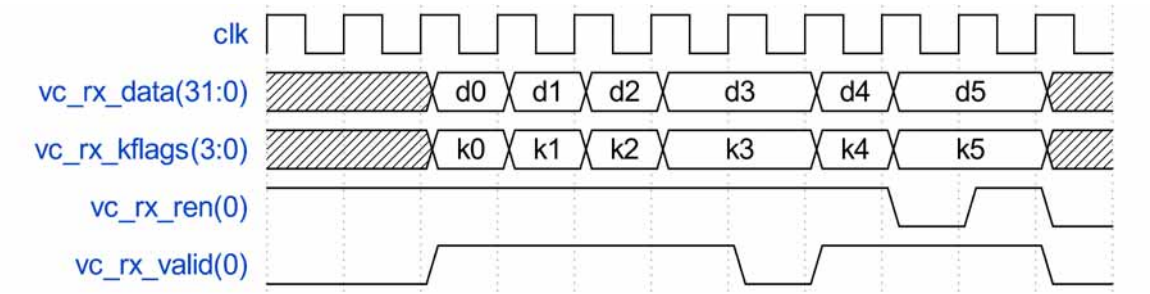


Figure 185. Example timing diagram - virtual channel 0 receive side

64.2.4 Broadcast interface

Transmit side

A broadcast delivers 8 bytes of payload, which are fed into the SpaceFibre IP core on port *bc_tx_data*. The lowest byte is transmitted first. Each broadcast has a channel and sequence number, which can be fed in at port *bc_tx_channel* and *bc_tx_seq* respectively. The write enable flag *bc_tx_wen* must be asserted to write the broadcast. Once the flag is set, an internal state machine prepares and executes the transmission of the broadcast frame. During this process the broadcast data, channel and sequence number must be kept stable. The SpaceFibre IP core signals the end of the transmission by pulsing the active-high flag bc_tx_ack for one clock cycle. An example timing diagram is shown in figure 186.

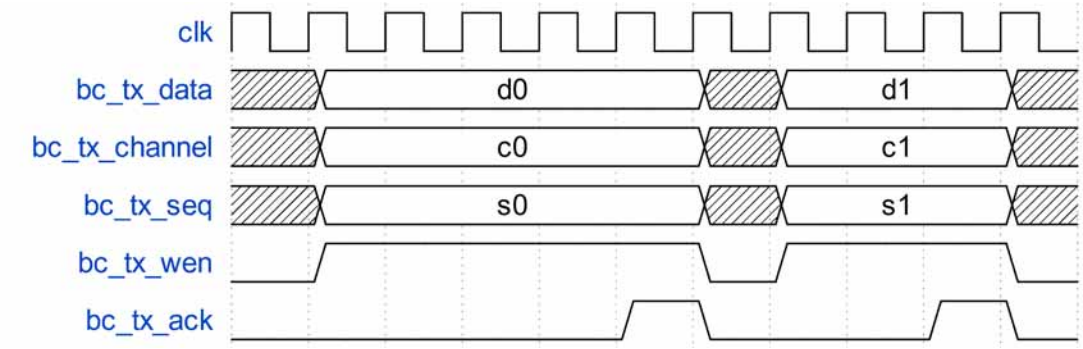


Figure 186. Example timing diagram - broadcast channel transmit side

Receive side

On the receive side, broadcast payload data is available on port *bc_rx_data*, the broadcast channel number on port *bc_rx_channel* and the broadcast sequence number on port *bc_rx_seq*. If the broadcast was sent during a retry, i.e. if the broadcast is unusually delayed, the flag *bc_rx_late* is high. Data

on the aforementioned ports is only valid when the active-high flag *bc_rx_valid* is pulsed for one clock-cycle. From a user's perspective, this flag can be used as a write enable signal for some sort of memory to store the broadcast data for further processing.

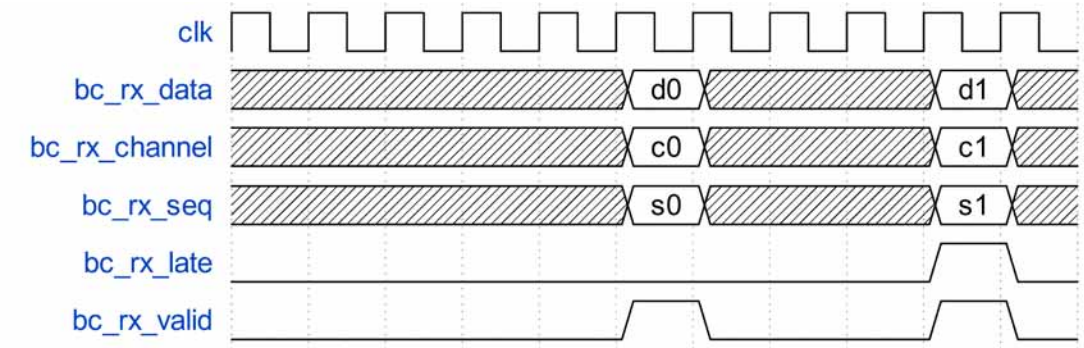


Figure 187. Example timing diagram - broadcast channel receive side

64.2.5 Serdes interface

Transmit

The internal data path width of the SpaceFibre IP core is 32 bits. The SpaceFibre IP core allows several different configurations:

- Large SerDes interface (*g_16_20_bit_mode* is false), internal 8B10B encoding is activated (*g_use_8b10b* is true): In this configuration, 8B10B encoded 40-bit wide transmit data is outputted at *se_tx_data*(39:0). *se_tx_kflags*(3:0) is unused and can be left open.
- Large SerDes interface (*g_16_20_bit_mode* is false), internal 8B10B encoding is deactivated (*g_use_8b10b* is false): In this configuration, unencoded 32-bit wide transmit data is outputted at *se_tx_data*(31:0). *se_tx_kflags*(3:0) is active and must be connected to the external 8B10B encoder, e.g. within the SerDes device.
- Small SerDes interface (*g_16_20_bit_mode* is true), internal 8B10B encoding is activated (*g_use_8b10b* is true): In this configuration, 8B10B encoded 20-bit wide transmit data is outputted at *se_tx_data*(19:0). *se_tx_kflags*(3:0) is unused and can be left open.
- Small SerDes interface (*g_16_20_bit_mode* is true), internal 8B10B encoding is deactivated (*g_use_8b10b* is false): In this configuration, unencoded 16-bit wide transmit data is outputted at *se_tx_data*(15:0). *se_tx_kflags*(1:0) is active and must be connected to the external 8B10B encoder, e.g. within the SerDes device.

If the lane layer of the SpaceFibre IP core is deactivated, the flag *se_tx_en* is low. It can be used to switch off the transmit side of the SerDes to save power during idle times.

For debug purposes, the transmit data and k-flags before any possible data path width conversion and 8B10B encoding can be monitored at *se_tx_data_dbg* and *se_tx_kflags_dbg*.

Receive

Similarly to the transmit side, the SerDes interface is used differently depending on the configuration:

- Large SerDes interface (*g_16_20_bit_mode* is false), internal 8B10B decoding is activated (*g_use_8b10b* is true): In this configuration, 8B10B encoded 40-bit wide receive data is fed in on port *se_rx_data*(39:0). *se_rx_kflags*(3:0) is unused and can be tied to ground.
- Large SerDes interface (*g_16_20_bit_mode* is false), internal 8B10B encoding is deactivated (*g_use_8b10b* is false): In this configuration, unencoded 32-bit wide receive data is fed in on port *se_rx_data*(31:0). *se_rx_kflags*(3:0) is active and must be connected to the external 8B10B decoder, e.g. within the SerDes device.

- Small SerDes interface (*g_16_20_bit_mode* is true), internal 8B10B encoding is activated (*g_use_8b10b* is true): In this configuration, 8B10B encoded 20-bit wide receive data is fed in on port *se_rx_data*(19:0). *se_rx_data*(39:20) should be tied to ground. *se_rx_kflags*(3:0) is unused and can be tied to ground as well.
- Small SerDes interface (*g_16_20_bit_mode* is true), internal 8B10B encoding is deactivated (*g_use_8b10b* is false): In this configuration, unencoded 16-bit wide receive data is fed in on port *se_rx_data*(15:0). *se_rx_kflags*(1:0) is active and must be connected to the external 8B10B encoder, e.g. within the SerDes device. *se_rx_data*(39:16) and *se_rx_kflags*(3:2) are unused and can be tied to ground.

If internal 8B10B decoding is not activated and the SerDes provides byte related error flags, for instance for disparity errors, these can be connected to the *se_rx_serror* port, with the lowest bit corresponding to the lowest byte of the receive data. If this is not the case, this port should be tied to ground. If the received data from the SerDes device is not synchronous to the SpaceFibre clock clk, the recovered SerDes receive clock must be connected to port *se_rx_clk*. If the data is already synchronous, for instance because the SerDes comprises its own elastic buffer, the SpaceFibre clock clk must be connected to *se_rx_clk*. If the lane layer of the SpaceFibre IP core is deactivated, the flag *se_rx_en* is low. It can be used to switch off the receive side of the SerDes to save power during idle times. If the SerDes provides a “No Signal” flag, it should be connected to port *se_no_signal*, otherwise this port must be tied to ground. If internal 8B10 decoding is not activated and the SerDes provides the capability to invert incoming bits, port *se_inv_pol* can be connected to the corresponding control port of the SerDes. If not, this port can be left unconnected.

For debug purposes, the receive data and k-flags after any possible data path width conversion and 8B10B decoding can be monitored at *se_rx_data_dbg* and *se_rx_kflags_dbg*.

64.3 Registers

There are no user accessible registers in the core. It is suggested to connect the configuration input signals (CF_*) and the status output signals (ST_*) to registers outside the core.

64.4 Vendor and device identifier

The vendor and device identifiers are only applicable for cores with AHB interfaces.

64.5 Implementation

64.5.1 Reset

The core changes reset behavior depending on settings in the GRLIB configuration package (see GRLIB User’s Manual). By default, the core makes use of synchronous reset and resets all its internal registers.

The core will use asynchronous reset for all registers if the GRLIB config package setting *grlib_async_reset_enable* is set.

64.6 Configuration options

Table 1125 shows the configuration options of the core (VHDL generics).

*Table 1125.*Configuration options

Generic name	Function	Allowed range	Default
g_tech	This generic can be used for technology-specific internal components such as memories.	0 - NTECH	inferred
g_use_8b10b	If set, internal 8B10B encoding and decoding is activated.	0 - 1	1
g_use_sep_txclk	If set, the SerDes transmission clock is decoupled from the SpaceFibre port clock. An additional transmit buffer is instantiated for this reason.	0 - 1	0
g_16_20_bit_mode	If set, the SerDes interface is 16+2 bit (without 8B10B) or 20 bit (with 8B10B) wide instead of 36/40 bit. If set, g_use_sep_txclk must also be set.	0 - 1	0
g_ticks_2us	Clock ticks corresponding to 2 µs.	1 - 16#2000#	125
g_tx_skip_freq	Frequency of SKIP word transmission in clock cycles.	1 - 16#2000#	5000
g_prbs_init1	If set, the INIT1 sequence during lane initialisation is embedded into a stream of pseudo-random numbers.	0 - 1	1
g_depth_rbuf_data	Log(Depth) of the data retry buffer.	1 - 32	8
g_depth_rbuf_fct	Log(Depth) of the FCT retry buffer.	1 - 32	4
g_depth_rbuf_bc	Log(Depth) of the broadcast retry buffer.	1 - 32	8
g_no_vc	Number of virtual channels.	1 - 32	4
g_depth_vc_rx_buf	Log(Depth) of virtual channel input buffer.	1 - 32	8
g_depth_vc_tx_buf	Log(Depth) of virtual channel output buffer.	1 - 32	8
g_remote_fct_cnt_max	Width of the remote FCT counter.	0 - 32	8
g_width_bw_credit	Width of the bandwidth credit counter.	0 - 16#FFFFFFFF#	20
g_min_bw_credit	Minimum bandwidth credit threshold limit.	0 - 16#FFFFFFFF#	52428
g_idle_time_limit	Bandwidth idle time limit in clock cycles.	0 - 16#FFFF#	62500

64.7 Signal Descriptions

Table 1126 shows the interface signals of the core (VHDL ports).

*Table 1126.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
TX_RST	N/A	Input	Reset of tx_clk clock domain	Low
TX_CLK	N/A	Input	Optional transmit clock	-
RX_RST	N/A	Input	Reset of se_rx_clk clock domain	Low
SE_RX_CLK	N/A	Input	SerDes receive clock	-
CF_RESET	N/A	Output	Active-high configuration register reset	High
VC_TX_DATA	N/A	Input	Virtual Channel Transmit Data	-
VC_TX_KFLAGS	N/A	Input	Virtual Channel Transmit K-Flags	-
VC_TX_WEN	N/A	Input	Virtual Channel Write Enable	?
VC_TX_FULL	N/A	Output	Virtual Channel Full Flags	?

*Table 1126.*Signal descriptions

Signal name	Field	Type	Function	Active
VC_TX_TIMESLOT	N/A	Input	Current timeslot	-
VC_RX_DATA	N/A	Output	Virtual Channel Receive Data	-
VC_RX_KFLAGS	N/A	Output	Virtual Channel Receive K-Flags	-
VC_RX_VALID	N/A	Output	Virtual Channel Valid Flags	?
VC_RX_REN	N/A	Input	Virtual Channel Read Enable Flags	?
BC_TX_DATA	N/A	Input	Broadcast Transmit Data	-
BC_TX_CHANNEL	N/A	Input	Broadcast Transmit Channel	-
BC_TX_SEQ	N/A	Input	Broadcast Transmit Sequence Number	-
BC_TX_WEN	N/A	Input	Broadcast Write Enable Flag	?
BC_TX_ACK	N/A	Output	Broadcast Acknowledgement Flag	?
BC_RX_DATA	N/A	Output	Broadcast Receive Data	-
BC_RX_CHANNEL	N/A	Output	Broadcast Receive Channel	-
BC_RX_SEQ	N/A	Output	Broadcast Receive Sequence Number	-
BC_RX_VALID	N/A	Output	Broadcast Valid Flag	?
BC_RX_LATE	N/A	Output	Broadcast Late Flag	?
SE_TX_DATA	N/A	Output	Transmit Data	-
SE_TX_KFLAGS	N/A	Output	Transmit K-Flags	-
SE_TX_EN	N/A	Output	SerDes Transmitter Enable Flag	?
SE_TX_DATA_DBG	N/A	Output	Unencoded 32-bit transmit data	-
SE_TX_KFLAGS_DBG	N/A	Output	4-bit K-Flags	-
SE_RX_DATA	N/A	Input	Receive Data	-
SE_RK_KFLAGS	N/A	Input	Receive K-Flags	-
SE_RX_SERROR	N/A	Input	Receive Error Flags	?
SE_RX_EN	N/A	Output	SerDes Receiver Enable Flag	?
SE_NO_SIGNAL	N/A	Input	SerDes No Signal Flag	?
SE_INV_POL	N/A	Output	SerDes Invert Polarity Flag	?
SE_RX_DATA_DBG	N/A	Output	Unencoded 32-bit receive data	-
SE_RX_KFLAGS_DBG	N/A	Output	4-bit K-Flags	-
CF_LINK_RST	N/A	Input	Active-high link reset	High
CF_LANE_START	N/A	Input	Lane Start flag of the lane initialisation state machine	High
CF_AUTO_START	N/A	Input	Autostart flag of the lane initialisation state machine	High
CF_LANE_RST	N/A	Input	Active-high lane reset	High
CF_LA_LOOPBACK	N/A	Input	Activates/deactivates internal loopback	
CF_DATA_SCR_EN	N/A	Input	Activates/deactivates data scrambler on transmission side	
CF_BC_EXPECTED_BW	N/A	Input	Expected broadcast bandwidth value	-
CF_VC_PRIORITIES	N/A	Input	Priority values for the virtual channels	-
CF_VC_EXPECTED_BW	N/A	Input	Expected virtual channel bandwidth value	-
CF_VC_TSLOT_VECS	N/A	Input	Timeslot vectors for the virtual channels	-
SR_FAR_END_LRST	N/A	Output	Pulsed high when the far end triggered a link reset	High
SR_LANE_STATE	N/A	Output	Indicates the current state of the lane initialisation state machine	-
SR_RXERR_COUNT	N/A	Output	Counts the number of RXERR words	-

*Table 1126.*Signal descriptions

Signal name	Field	Type	Function	Active
SR_RXERR_COUNT_OF	N/A	Output	Pulsed high when the RXERR counter overflows	High
SR_FAR_END_-STANDBY	N/A	Output	Pulsed high when STANDBY words are received	High
SR_TIMEOUT	N/A	Output	Pulsed high when a connection timeout during lane initialisation has occurred	High
SR_FAR_END_LOS	N/A	Output	Pulsed high when LOS words are received	High
SR_RX_POLARITY	N/A	Output	Set when the SerDes receiver polarity is inverted	High
SR_CRC16_ERR	N/A	Output	Pulsed high when a CRC-16 error has occurred	High
SR_FRAME_ERR	N/A	Output	Pulsed high when a frame error has occurred	High
SR_CRC8_ERR	N/A	Output	Pulsed high when a CRC-8 error has occurred	High
SR_SEQ_ERR	N/A	Output	Pulsed high when a sequence error has occurred	High
SR_RBUF_EMPTY	N/A	Output	Set when the error recovery buffer is empty	High
SR_RETRY_CNT	N/A	Output	The number of error recovery attempts made by the SpaceFibre port	-
SR_BW_OVER_USE	N/A	Output	Set when a virtual channel is using much more bandwidth than expected	High
SR_BW_UNDER_USE	N/A	Output	Set when a virtual channel is using much less bandwidth than expected	High
SR_DEST_HAS_CREDIT	N/A	Output	Set when there is space in the input buffer of the destination node	High
SR_INPUT_BUF_OV	N/A	Output	Set when an input buffer is receiving data when it is full	High
SR_FCT_CNT_OV	N/A	Output	Pulsed high when the FCT credit counter of a virtual channel has overflowed	High

* see GRLIB IP Library User's Manual

64.8 Library dependencies

Table 1127 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1127.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
SPFI	SPFICOMP	Signals, component	Component declaration

64.9 Instantiation

This example shows how the core can be instantiated.

```
grspfi_codec0: grspfi_codec
  generic map (
    g_tech              => inferred,
    g_use_8b10b         => 1,
    g_use_sep_txclk     => 0,
    g_16_20_bit_mode    => 0,
    g_ticks_2us         => 125,
    g_tx_skip_freq      => 5000,
    g_prbs_init1        => 1,
    g_depth_rbuf_data   => 8,
    g_depth_rbuf_fct    => 4,
    g_depth_rbuf_bc     => 8,
    g_no_vc             => 4,
```

```
    g_depth_vc_rx_buf    => 8,
    g_depth_vc_tx_buf    => 8,
    g_remote_fct_cnt_max => 8,
    g_width_bw_credit    => 20,
    g_min_bw_credit      => 52428,
    g_idle_time_limit    => 62500)
  port map (
    clk                => clk,
    tx_clk             => tx_clk,
    rst                => rst,
    rx_rst             => rx_rst,
    tx_rst             => tx_rst,
    vc_tx_full         => vc_tx_full,
    vc_rx_data         => vc_rx_data,
    vc_rx_kflags       => vc_rx_kflags,
    vc_rx_valid        => vc_rx_valid,
    vc_rx_ren          => vc_rx_ren,
    vc_tx_data         => vc_tx_data,
    vc_tx_kflags       => vc_tx_kflags,
    vc_tx_wen          => vc_tx_wen,
    vc_tx_timeslot     => vc_tx_timeslot,
    bc_rx_data         => bc_rx_data,
    bc_rx_channel      => bc_rx_channel,
    bc_rx_seq          => bc_rx_seq,
    bc_rx_valid        => bc_rx_valid,
    bc_rx_late         => bc_rx_late,
    bc_tx_ack          => bc_tx_ack,
    bc_tx_data         => bc_tx_data,
    bc_tx_channel      => bc_tx_channel,
    bc_tx_seq          => bc_tx_seq,
    bc_tx_wen          => bc_tx_wen,
    se_tx_data         => se_tx_data,
    se_tx_kflags       => se_tx_kflags,
    se_tx_en           => se_tx_en,
    se_rx_en           => se_rx_en,
    se_inv_pol         => se_inv_pol,
    se_rx_clk          => se_rx_clk,
    se_rx_data         => se_rx_data,
    se_rx_kflags       => se_rx_kflags,
    se_rx_serror       => se_rx_serror,
    se_no_signal       => se_no_signal,
    se_tx_data_dbg     => se_tx_data_dbg,
    se_tx_kflags_dbg   => se_tx_kflags_dbg,
    se_rx_data_dbg     => se_rx_data_dbg,
    se_rx_kflags_dbg   => se_rx_kflags_dbg,
    cf_reset           => cf_reset,
    cf_vc_priorities   => cf_vc_priorities,
    cf_vc_expected_bw  => cf_vc_expected_bw,
    cf_vc_tslot_vecs   => cf_vc_tslot_vecs,
    cf_bc_expected_bw  => cf_bc_expected_bw,
    cf_data_scr_en     => cf_data_scr_en,
    cf_link_rst        => cf_link_rst,
    cf_lane_start      => cf_lane_start,
    cf_auto_start      => cf_auto_start,
    cf_lane_rst        => cf_lane_rst,
    cf_loopback        => cf_loopback,
    sr_bw_over_use     => sr_bw_over_use,
    sr_bw_under_use    => sr_bw_under_use,
    sr_dest_has_credit => sr_dest_has_credit,
    sr_input_buf_ov    => sr_input_buf_ov,
    sr_fct_cnt_ov      => sr_fct_cnt_ov,
    sr_crc16_err       => sr_crc16_err,
    sr_frame_err       => sr_frame_err,
    sr_crc8_err        => sr_crc8_err,
    sr_seq_err         => sr_seq_err,
    sr_rbuf_empty      => sr_rbuf_empty,
    sr_retry_cnt       => sr_retry_cnt,
    sr_far_end_lrst    => sr_far_end_lrst,
    sr_lane_state      => sr_lane_state,
    sr_rxerr_count     => sr_rxerr_count,
    sr_rxerr_count_of  => sr_rxerr_count_of,
```

```
sr_far_end_standby => sr_far_end_standby,
sr_timeout         => sr_timeout,
sr_far_end_los     => sr_far_end_los,
sr_rx_polarity     => sr_rx_polarity);
```

65 GRSRIO - Serial RapidIO endpoint with AHB or AXI4 bus master interface

65.1 Overview

The GRSRIO core implements the RapidIO Interconnect Specification Part 1 (I/O Logical Specification) and Part 2 (Message Passing Logical Specification) for data messages, doorbell messages, outbound maintenance messages and I/O operations, as defined in Rev. 2.1. This is done by means of a flexible and configurable DMA engine with a configurable bus master interface.

Additionally the core implements the MECS Time Synchronization Protocol according to Rev. 4.0.

The targeted SRIO endpoint is the SRIOIP-GEN2IP core by Integrated Device Technology. The choice of the SRIOIP-GEN2 end point has several implications on the SRIO:

- CAR and CSR registers defined in I/O and Message Passing Logical Specification are assumed to be already implemented in the end point
- Inbound maintenance request are assumed to be already handled by the end point

Two wrappers are available for the core, one with an AHB AMBA 2.0 Bus Master (grsrio_gen2ahb) to be readily compatible with Cobham Gaisler's GRLIB and one with an AXI4 (grsrio_gen2axi) to also support latest System-on-Chip (SoC) architectures.

The DMA engine serves several queues of descriptors placed in memory with two possible modes, selectable at compile time:

- Legacy mode: When *g_hyb_que* is set to “false”, descriptors for data messages and I/O operations are 8 words long and the ones for doorbell messages 4. In this configuration, each kind of operation (IO memory access, data message and doorbell message) have separated transmission queues, from 1 up to 32 each. In this configuration, descriptors for data messages and I/O operations are 8 words long, while ones for doorbell messages 4. In this configuration, the core has an interface and a behavior compatible with the GRSRIO Logical Layer IP core Version 1.
- Hybrid-queues mode: When *g_hyb_que* is set to “true”, there are just *g_no_hyb_tx* transmission queues, each capable of transmitting all kinds of logical operations. This allows a larger CPU offload and a lower number of queues required for each software entity. In this configuration, all TX descriptors are 8 words long. RX descriptors for data messages and I/O operations are 8 words long and the ones for doorbell messages 4.

A timestamp functionality is provided for each descriptor. When *g_mecs* is set to “true” the time value is taken by the internal MECS Timestamp Generator, while when *g_mecs* is set to false or the MECS functionality is disabled, the time value is taken from an external source.

The core provides a capability register to allow the software to know what functionalities the core instantiation supports and the number of queues instantiated.

65.2 Operation

65.2.1 Receiving Data messages

Inbound data messages are stored in one or more message reception queues. The desired number of reception queues can be set by VHDL generic *g_no_msg_rx* at compile time.

The inbound data messages are stored to a specific queue depending on their destination ID and mailbox number. The accepted destination ID of a queue can be defined in register RXMSG_DST_ID and the accepted mailbox number in the field RXMSG_CTRL.MBOX. Furthermore, ranges of destination IDs and mailbox numbers can be accepted by also setting the masking register RXMSG_DST_MSK and in the field RXMSG_CTRL.MBOXMSK. For instance, the user could set up five queues, the first four queues accepting messages addressed to mailbox 0 to 3 and the fifth queue accepting messages addressed to all the other ones (4-63). If several message reception queues are configured to accept

the same destination ID / mailbox number pair, the message queue with the lowest index number, that is currently not busy, will receive the message.

If a message is received, which is addressed to a mailbox number /destination ID combination that is not accepted by any message reception queue, the processing core automatically generates and transmits ERROR responses to the source node.

A single queue can receive only a multi-segment data message per time, but more queues can be set with the same destination ID or destination ID/Mailbox combination, effectively allowing up to 16 transfer between a couple of destination/source IDs.

Each reception queue is a circular buffer that is located in memory. Before activating the queue, the memory start address of the circular buffer must be set in register RXMSG_MADDR(_LSW) and RXMSG_MADDR_MSW (if CFG_AW is set to 64) and its depth in register RXMSG_CONF.CBD. Each queue can be configured to store between 2 and 65,536 message descriptors. Each descriptor has a size of 32 bytes and it is up to the software to reserve the necessary memory space for the whole circular buffer.

Each reception queue can be configured to trigger a set of interrupts: (i) full interrupts that indicate that no more inbound data message can be accepted because the reception queue is full (RXMSG_STAT.IF), (ii) error interrupts that indicate bus errors and timeout errors in case of multi-packet messages (RXMSG_STAT.IE), and (iii) reception interrupts that indicate that a full message was successfully received (RXMSG_STAT.IR).

The GRSRIO logical layer does not distinguish between single (up to 256 bytes) and multi-packet messages (up to 4K) and only one DMA descriptor is used for both types of messages. However, the user must set the maximum allowed message size for the queue in register RXMSG_CONF.MAX_SIZE.

All following conditions must be true for a message to be accepted by the queue:

- The queue is enabled.
- The queue is not full.
- The destination ID is accepted.
- The mailbox number is accepted.
- The message does not exceed the maximum allowed size.

If no queue is available that can accept the message, the GRSRIO logical layer replies to the destination node with an ERROR response. If there are queues that could accept the packet but they are all full or busy with ongoing multi-segment data messages, the GRSRIO logical layer replies to the destination node with a RETRY response.

The timeout can be configured globally in register TO_CONF and expresses the maximum allowed time span between a DONE response for one message segment and the reception of the next segment. If the timeout elapses, the descriptor will be closed with the Serial RapidIO Error (SE) flag set and an error interrupt is generated if enabled.

The circular buffer management between hardware and software is done via two descriptor pointers. The tail pointer in RXMSG_TLPTR is managed by hardware whereas the head pointer in RXMSG_HDPTR is managed by software.

The software can add one or more descriptors to the circular buffer and then activate them by increasing the head pointer value in RXMSG_HDPTR. Every time the GRSRIO logical layer receives a new message successfully, it will increment the tail pointer to the next descriptor. The software can always check how many free descriptors are left in the buffer by subtracting the tail pointer value from the head pointer value.

In the following, the relevant descriptor words of the message reception queues are described:

*Table 1128.*GRSRIO message reception descriptor word 0 (address offset 0x0)

31	0
ADDR_MSW	

31: 0 Most Significant Word of the Memory Start Addres (ADDR_MSW): MSW of the address of the start of the memory block reserved for the reception of data messages. This field is reserved when *CFG_AW* is set to “true”.

*Table 1129.*GRSRIO message reception descriptor word 1 (address offset 0x4)

31	0
ADDR(_LSW)	

31: 0 Memory Start Address (ADDR(_LSW)): when *CFG_AW* is set to 32, this is the address of the start of the memory block reserved for the reception of this message. When *CFG_AW* is set to 64, this is the LSW of that address.

*Table 1130.*GRSRIO message reception descriptor word 2 (address offset 0x8)

31	0
SOURCE_ID	

31: 0 Source Identifier (SOURCE_ID). RapidIO source device identifier. If the GRSIO is configured for 8-bit identifiers, only the lower 8 bits are valid.

*Table 1131.*GRSRIO message reception descriptor word 3 (address offset 0xC)

31	0
DEST_ID	

31: 0 Destination Identifier (DEST_ID). Rapid IO destination device identifier. If the GRSIO is configured for 8-bit identifiers, only the lower 8 bits are valid.

*Table 1132.*GRSRIO message reception descriptor word 4 (address offset 0x10)

31	30	29	28	27	26	25	20	19	18	17	16	15	4	3	2	1	0
VC	CR	PRIOR		LET		MBOX		TT		RES		MSIZE		R	SE	DO	RI

31 Virtual Channel (VC). Set if also the VC bit of the message packet was set.

30 Critical Request Flow (CR). Set when the message arrived in a packet in a critical or preferred flow with respect to other flows of the same priority.

29: 28 Priority (PRIOR). Priority of the packet in which this message arrived.

27: 26 Letter (LET). Although concurrent reception of different letters is not supported, messages can still arrive in different letters. This field contains the letter number (0-3) of the message.

25: 20 Mailbox (MBOX). This field contains the number of the mailbox to which this message was addressed. Messages for mailbox numbers greater than 3 have a maximum size of 256 bytes whereas messages for mailbox numbers 0 to 3 can have a size of up to 4K.

19: 18 Transport Type Field (TT). Set to 0b00 if device ID is 8-bit wide and set to 0b01 if device ID is 16-bit wide.

17: 16 RESERVED

*Table 1132.*GRSRIO message reception descriptor word 4 (address offset 0x10)

15: 4	Message Size (MSIZE). Size of the received message in bytes: Size = (MSIZE+1) bytes.
3	RESERVED
2	Serial RapidIO Error (SE). Set when a multi-packet message was not received correctly. The GRSRIO implements a response-to-request timeout mechanism according to RapidIO specification part 8. If this timeout elapses during the reception of a message, the descriptor is closed and this error flag is set.
1	Done Flag (DO). Set when the message was correctly received, that is, when the processing core generated and transmitted a DONE response to the destination node.
0	Enable Reception Interrupt (RI). If set, the GRSRIO triggers an interrupt when the message was correctly received, that is, when also the done flag DO is set. The interrupt is triggered after the DMA engine has finished all memory accesses related to this descriptor.

*Table 1133.*GRSRIO message reception descriptor word 5 (address offset 0x14)

31	0
TIMESTAMP_MSW	

31: 0	LSW of the Timestamp (TIMESTAMP_LSW). MSW of the local timer when the message was completely received or when message reception was aborted due to timeout.

*Table 1134.*GRSRIO message reception descriptor word 6 (address offset 0x18)

31	0
TIMESTAMP_LSW	

31: 0	LSW of the Timestamp (TIMESTAMP_LSW). LSW of the local timer when the message was completely received or when message reception was aborted due to timeout.

*Table 1135.*GRSRIO message reception descriptor word 7 (address offset 0x1C)

31	0
RESERVED	

31: 0	RESERVED

65.2.2 Transmitting Data Messages

Outbound data messages are stored in message or hybrid (depending on *g_hyb_que*) transmission queues. The desired number of transmission queues can be set by VHDL generic *g_no_msg_tx* or *g_no_hyb_tx* at compile time. In the latter case the queues are shared with the other transaction types.

If several transmission queues have messages ready to be sent, the one with the highest priority gets to transmit first. If more than one active queues have the highest priority, the arbitration between them is done with a round robin algorithm. However, the following conditions must be true:

- The queue is enabled.
- The message has a priority level that can currently be accepted by the SRIO end point.

Each transmission queue is a circular buffer that is located in memory. Before activating the queue, the memory start address of the circular buffer must be set in register TXMSG_MADDR(_LSW) and TXMSG_ADDR_MSW (or TX_MADDR(_LSW) and TX_MADDR_MSW) and its depth in register TXMSG_CTRL.CBD or TX_CTRL.CBD. Each queue can be configured to store between 2 and 65,536 message descriptors. Each descriptor has a size of 32 bytes and it is up to the software to reserve the necessary memory space for the whole circular buffer.

Each transmission queue can be configured to trigger a set of interrupts: (i) error interrupts that indicate bus errors, retry errors, and timeout errors (TXMSG_CTRL.IE or TX_CTRL.IE), and (ii) transmission interrupts that indicate that a full message was successfully transmitted (TXMSG_STAT.IT or TX_STAT.IT). The generation of transmission interrupts can be further configured by setting the transmission interrupt mode bit (TXMSG_CTRL.IM or TX_CTRL.IM). If set, a transmission interrupt is always triggered after the transmission queue became empty. If not set, the generation of transmission interrupts depends on the Enable Transmission Interrupt (TI) field of each message descriptor.

Messages or segments of messages are automatically retried until either the packet is accepted by the destination node or until the threshold level defined in the descriptor field RCOUNT is reached. For multi-packet messages, RCOUNT is the number of possible retries for all message segments together. If RCOUNT in the descriptor is set to zero the transmission will be retried until the transmission is successful.

Each transmission queue has a fixed source ID (TXMSG_SRC_ID or TX_SRC_ID), priority (TXMSG_CTRL.PRIO), critical request flow setting (TXMSG_CTRL.CR or TX_CTRL.CR), virtual channel setting (TXMSG_CTRL.VC) and transport type (TXMSG_CTRL.TT or TX_CTRL.TT). For each message individually, the destination ID (DEST_ID), mailbox number (MBOX, XMBOX) and letter number (LET) can be set up in the corresponding descriptor.

Each transmission queue implements a request-to-response timeout mechanism that counts the time between the transmission of a message (or message segment) and a response from the destination node. This timeout can be configured globally in the TO_CONF register. If the timeout elapses, the descriptor will be closed with the Timeout Error (TE) flag set and an error interrupt is generated if enabled.

A transmission queue serves one descriptor at a time. Two packets are sent from the same queue when the descriptor defines more than one packet, and then replies for them are awaited before moving to the next couple. This is done in order to enhance the throughput of transfers up to 4 KB. Receiving a RETRY request when two packets are outstanding will cause both packets to be sent again and when an ERROR response is received the descriptor is written back with the number of segment causing the error.

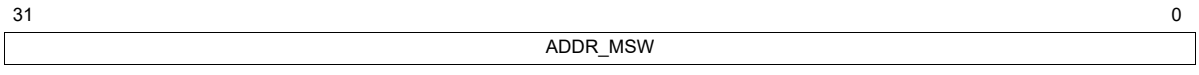
The circular buffer management between hardware and software is done via two descriptor pointers. The tail pointer in TXMSG_TLPTR or TX_TLPTR is managed by hardware whereas the head pointer in TXMSG_HDPTR or TX_HDPTR is managed by software.

Sending a data message does not increase the internal srcTID counter, as data messages are not identified using this field.

The software can add one or more descriptors to the circular buffer and then activate them by increasing the head pointer value in TXMSG_HDPTR or TX_HDPTR. Every time the GRSRIO logical layer transmits a new message successfully, it will increment the tail pointer to the next descriptor. The software can always check how many descriptors awaiting transmission are left in the buffer by subtracting the tail pointer value from the head pointer value.

In the following, the relevant descriptor words of the message transmission queues are described:

*Table 1136.*GRSRIO message transmission descriptor word 0 (address offset 0x0)



31: 0	Most Significant Word of the Memory Start Address: MSW of the address of the start of the memory block storing the payloads of the data messages to be transmitted. This field is reserved when CFG_AW = 32.

*Table 1137.*GRSRIO message transmission descriptor word 1 (address offset 0x4)

31	0
ADDR(_LSW)	

31: 0 (Less Significant Word of the) Memory Start Address: When CFG_AW = 32, this is the address pointing to the start of the memory block storing the payload of the message to be transmitted, otherwise it is the LSW of such address.

*Table 1138.*GRSRIO message transmission descriptor word 2 (address offset 0x8)

31	0
DEST_ID	

31: 0 Destination Identifier (DEST_ID). Rapid IO destination device identifier. If the GRSRIO is configured for 8-bit identifiers, only the lower 8 bits are valid.

*Table 1139.*GRSRIO message transmission descriptor word 3 (address offset 0xC)

31 24	23 22	21 20	19 16	15 1	0
RESERVED	LET	MBOX	XMBOX	RESERVED	TI

31: 24 RESERVED

23: 22 Letter (LET). This field contains the letter number (0-3) of the message.

21: 20 Mailbox (MBOX). This field contains the number of the mailbox to which this message is addressed. Messages for mailbox numbers greater than 3 (using XMBOX as extension) are only allowed to have a maximum size of 256 bytes whereas messages for mailbox numbers 0 to 3 can have a size of up to 4K.

19: 16 Extended Mailbox (XMBOX). This field specifies the upper four bits of the mailbox to which this message is addressed. If the message size is larger than 256 bytes, this field must be zero.

15: 1 RESERVED

0 Enable Transmission Interrupt (TI). If set, the GRSRIO triggers an interrupt when the message was correctly transmitted, that is, when also the done flag DO is set (only if TXMSG_CONF.IM or TX_CONF.IM is set to 0). The interrupt is triggered after the DMA engine has finished all memory accesses related to this descriptor.

*Table 1140.*GRSRIO message transmission descriptor word 4 (address offset 0x10)

31	30 22	21 6	5 4	3	2	1	0
R	MSIZE	RCOUNT	RES	RE	TE	SE	DO

31 RESERVED

30: 22 Message Size (MSIZE). Size of the message in multiples of 8 bytes: Size = (MSIZE+1)*8 bytes. After transmission, this field is updated by GRSRIO with the remaining data that could not be transmitted, that is, in case of a correctly transmitted message this field should always read 0.

21: 16 Retry Count (RCOUNT). Outbound messages are automatically retried until the destination node either accepts the message or until the user-defined retry threshold level in this field is reached. For multi-packet messages, this retry threshold level applies to all segments on the whole. After transmission, this field is updated by GRSRIO with the remaining number of retries, that is, if no retry was required the original field content does not change. When set to zero the transmission will be retried forever.

15: 4 RESERVED

*Table 1140.*GRSRIO message transmission descriptor word 4 (address offset 0x10)

3	Retry Error (RE). Set when this message was retried too many times and the retry threshold level was reached.
2	Timeout Error (TE). Set when the request-to-response timeout has expired, that is, when the destination node did not acknowledge the reception of the message (or part of the message in case of a multi-packet message) in time.
1	Serial RapidIO Error (SE). Set when an ERROR or unknown response was received from the destination node.
0	Done Flag (DO). Set when the message was correctly transmitted, that is, when the processing core received a DONE response from the destination node for each packet of the message.

*Table 1141.*GRSRIO message transmission descriptor word 5 (address offset 0x14)

31	0
TIMESTAMP_MSW	

31: 0	MSW of the Message Time-Stamp (TIMESTAMP_MSW): This is the MSW of the local timer when message transmission was completed (with or without an error), that is when the response or the last response for multi-segment messages is received.

*Table 1142.*GRSRIO message transmission descriptor word 6 (address offset 0x18)

31	0
TIMESTAMP_LSW	

31: 0	LSW of the Message Time-Stamp (TIMESTAMP_LSW): This is the LSW of the local timer when message transmission was completed (with or without an error), that is when the response or the last response for multi-segment messages is received.

*Table 1143.*GRSRIO message transmission descriptor word 7 (address offset 0x1C)

31	2	1	0
RESERVED			DSC_TYP

31: 2	RESERVED
1: 0	DSC_TYP: when *g_hyb_que* is set to true, this field must be set to 0b01 to mark the operation defined by the descriptor as a Data Message operation. This field is reserved and will be ignored when *g_hyb_que* is set to false.

65.2.3 Receiving Doorbell Messages

Inbound doorbell messages are stored in one or more doorbell reception buffers. The desired number of reception buffers can be set by VHDL generic *g_no_dbell_rx* at compile time. Doorbell messages are small enough to be stored directly in the circular buffer and therefore do not need DMA descriptors. Furthermore, descriptors are 4 words long instead of 8 to decrease latency of operations.

The inbound doorbell messages are stored to a specific buffer depending on their destination ID. The accepted destination ID of a buffer can be defined in register RXDBL_DST_ID. Furthermore, ranges of destination IDs can be accepted by also setting the masking field RXDBL_DST_MSK. If several doorbell reception buffers are configured to accept the same destination ID, the doorbell buffer with the lowest index number, that is currently not busy, will receive the doorbell message.

Each reception buffer is a circular buffer that is located in memory. Before activating the buffer, the memory start address of the circular buffer must be set in register RXDBL_MADDR_LSW (and RXDBL_MADDR_MSW if *CFG_AW = 64*) and its depth in register RXDBL_CTRL.CBD. Each

queue can be configured to store between 2 and 65,536 doorbell messages. Each doorbell message buffer entry has a size of 16 bytes and it is up to the software to reserve the necessary memory space for the whole circular buffer.

Each reception buffer can be configured to trigger a set of interrupts: (i) full interrupts that indicate that no more inbound doorbell messages can be accepted because the reception buffer is full (RXDBL_CTRL.IF), (ii) error interrupts that indicate bus errors (RXDBL_CTRL.IE), and (iii) reception interrupts that indicate that a doorbell message was successfully received (RXDBL_CTRL.IR).

All following conditions must be true for a doorbell message to be accepted by the queue:

- The queue is enabled.
- The queue is not full.
- The destination ID is accepted.

If no buffer is available that can accept the message, the GRSRIO logical layer replies to the destination node with an ERROR response. If a buffer is available but full, the GRSRIO logical layer replies to the destination node with a RETRY response.

The circular buffer management between hardware and software is done via two descriptor pointers. The tail pointer in RXDBL_TLPTR is managed by hardware whereas the head pointer in RXDBL_HDPTR is managed by software.

The software can add one or more buffer entries to the circular buffer and then activate them by increasing the head pointer value in RXDBL_HDPTR. Every time the GRSRIO logical layer receives a new doorbell message successfully, it will increment the tail pointer to the next buffer entry. The software can always check how many free buffer entries are left in the buffer by subtracting the tail pointer value from the head pointer value.

The GRSRIO logical layer also allows the forwarding of received doorbell messages to an external port. To enable this feature, the EXTDBL_CONF.DO signal must be set. In addition, the logical layer can be configured to only forward specific doorbell messages. This feature can be enabled by setting the EXTDBL_CONF.DC bit and by setting up a compare value in EXTDBL_FLTR.DBCOMP and a mask value in EXTDBL_FLTR.DBMASK.

In the following, the relevant buffer entry words of the doorbell reception buffers are described:

*Table 1144.*GRSRIO doorbell message reception buffer word 0 (address offset 0x0)

31	0
SOURCE_ID	

31: 0	Source Identifier (SOURCE_ID). RapidIO source device identifier. If the GRSIO is configured for 8-bit identifiers, only the lower 8 bits are valid.

*Table 1145.*GRSRIO doorbell message reception buffer word 1 (address offset 0x4)

31	0
DEST_ID	

31: 0	Destination Identifier (DEST_ID). Rapid IO destination device identifier. If the GRSIO is configured for 8-bit identifiers, only the lower 8 bits are valid.

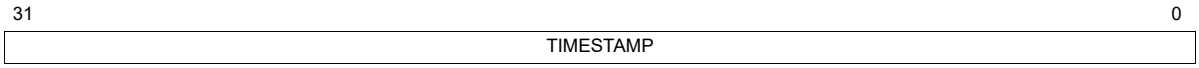
*Table 1146.*GRSRIO doorbell message reception buffer word 2 (address offset 0x8)

31	16	15	11	10	9	8	7	6	5	4	3	1	0
INFO		RESERVED		TT		VC	CR	PRIOR		DO	RES		RI

*Table 1146.*GRSRIO doorbell message reception buffer word 2 (address offset 0x8)

31: 16	Doorbell Information (INFO). This field contains the payload of the received doorbell message.
15: 11	RESERVED
10: 9	Transport Type Field (TT). Set to 0b00 if device ID is 8-bit wide and set to 0b01 if device ID is 16-bit wide.
8	Virtual Channel (VC). Set if also the VC bit of the doorbell message packet was set.
7	Critical Request Flow (CR). Set when the doorbell message arrived in a packet in a critical or preferred flow with respect to other flows of the same priority.
6: 5	Priority (PRIOR). Priority of the packet in which this doorbell message arrived.
4	Done Flag (DO). Set when the doorbell message was correctly received, that is, when the processing core generated and transmitted a DONE response to the destination node.
3: 1	RESERVED
0	Enable Reception Interrupt (RI). If set, the GRSRIO triggers an interrupt when the doorbell message was correctly received, that is, when also the done flag DO is set. The interrupt is triggered after the DMA engine has finished all memory accesses to this buffer entry.

*Table 1147.*GRSRIO doorbell message reception buffer word 3 (address offset 0xC)



31: 0	Message Time-Stamp (TIMESTAMP). LSW of the local timer when the message was completely received or when message reception was aborted due to timeout.Timestamp of 64 bits are not supported for reception of doorbells.

65.2.4 Transmitting doorbell messages

Outbound doorbell messages are stored in doorbell or hybrid transmission queues (depending on *g_hyb_que*). The desired number of transmission buffers can be set by VHDL generic *g_no_dbell_tx* or *g_no_hyb_tx* at compile time. The descriptor in this case directly contains the SRIO payload, as it is just 2 B long. Furthermore, when *g_hyb_que* is set to false, descriptors are 4 words long instead of 8 to decrease latency of operations. When *g_hyb_que* is set to true TX descriptors of doorbells messages are 8 words long like the ones for the other transaction types.

If several transmission queues have messages ready to be sent, the one with the highest priority gets to transmit first. If more than one active queues have the highest priority, the arbitration between them is done with a round robin algorithm. However, the following conditions must be true:

- The queue is enabled.
- The doorbell message has a priority level that can currently be accepted by the SRIO end point.

Each transmission queue is a circular buffer that is located in memory. Before activating the buffer, the memory start address of the circular buffer must be set in register TXDBL_MADDR_LSW (and TXDBL_MADDR(_MSW)) or TX_MADDR_LSW (and TX_MADDR(_MSW)) and its depth in the register field TXDBL_CTRL.CBD or TX_CTRL.CBD. Each queue can be configured to store between 2 and 65,536 doorbell messages. Each buffer entry has a size of 16 bytes when *g_hyb_que* is set to “false” and 32 bytes when *g_hyb_que* is set to “true”. It is up to the software to reserve the necessary memory space for the whole circular buffer.

Each transmission buffer can be configured to trigger a set of interrupts: (i) error interrupts that indicate bus errors, retry errors, and timeout errors (TXDBL_CTRL.IE or TX_CTRL.IE), and (ii) transmission interrupts that indicate that a doorbell message was successfully transmitted (TXDBL_CTRL.IT or TX_CTRL.IT). The generation of transmission interrupts can be further con-

figured by setting the transmission interrupt mode bit (TXDBL_CTRL.IM or TX_CTRL.IM). If set, a transmission interrupt is always but only triggered after the transmission buffer became empty. If not set, the generation of transmission interrupts depends on the Enable Transmission Interrupt (TI) setting of the doorbell buffer entry.

Doorbell messages are automatically retried until either the packet is accepted by the destination node or until the threshold level defined in the buffer entry field RCOUNT is reached. If RCOUNT is set to zero they are retried forever.

Each transmission buffer has a fixed source ID (TXDBL_SRC_ID), priority (TXDBL_CTLR.PRIO), critical request flow setting (TXDBL_CTRL.CR), virtual channel setting (TXDBL_CTRL.VC) and transport type (TXDBL_CTRL.TT). For each doorbell message individually, the destination ID (DEST_ID) can be set up in the corresponding buffer entry.

Each transmission buffer implements a request-to-response timeout mechanism that counts the time between the transmission of a doorbell message and a response from the destination node. This timeout can be configured globally in register TO_CONF. If the timeout elapses, the buffer entry will be closed with the Timeout Error (TE) flag set and an error interrupt is generated if enabled. A transmission queue is blocked while it is awaiting a response from the destination node. However, other transmission queues can be serviced in the meanwhile.

Every time a new packet is sent the srcTID field of the packet is increased, also when a transaction is retried.

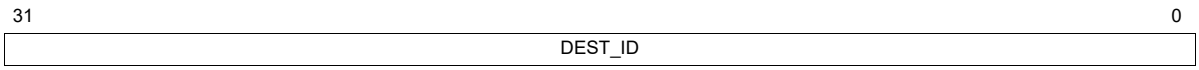
The circular buffer management between hardware and software is done via two descriptor pointers. The tail pointer in TXDBELLMSG3.TLPTR is managed by hardware whereas the head pointer in TXDBELLMSG3.HDPTR is managed by software.

The software can add one or more buffer entries to the circular buffer and then activate them by increasing the head pointer value in TXDBELLMSG3.HDPTR. Every time the GRSRIO logical layer transmits a new doorbell message successfully, it will increment the tail pointer to the next buffer entry. The software can always check how many buffer entries awaiting transmission are left in the buffer by subtracting the tail pointer value from the head pointer value.

The GRSRIO logical layer also allows the generation of doorbell messages through an external port. To enable this feature, the CORECONF1.DI bit must be set. Pending external doorbell transmission requests have always priority over internal transmission requests.

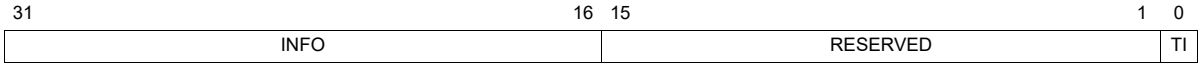
In the following, the relevant descriptor words of the message transmission queues are described:

*Table 1148.*GRSRIO doorbell message transmission buffer word 0 (address offset 0x0)



31: 0	Destination Identifier (DEST_ID). Rapid IO destination device identifier. If the GRSIO is configured for 8-bit identifiers, only the lower 8 bits are valid.

*Table 1149.*GRSRIO doorbell message transmission buffer word 1 (address offset 0x4)



31: 16	Doorbell Information (INFO). This field contains the payload of the doorbell message.
15: 1	RESERVED
0	Enable Transmission Interrupt (TI). If set, the GRSRIO triggers an interrupt when the doorbell message was correctly transmitted, that is, when also the done flag DO is set. The interrupt is triggered after the DMA engine has finished all memory accesses to this buffer entry.

*Table 1150.*GRSRIO doorbell message transmission buffer word 2 (address offset 0x8)

31 22	21 6	5 4	3	2	1	0
RESERVED	RCOUNT	RES	RE	TE	SE	DO

31: 22	RESERVED
21: 16	Retry Count (RCOUNT). Outbound doorbell messages are automatically retried until the destination node either accepts the message or until the user-defined retry threshold level in this field is reached. After transmission, this field is updated by GRSRIO with the remaining number of retries, that is, if no retry was required the original field content does not change.When this field is set to zero the transmission will be retried forever.
15: 4	RESERVED
3	Retry Error (RE). Set if the doorbell message was retried as many times as defined by RCOUNT but the transmission was still not successful.
2	Timeout Error (TE). Set when the request-to-response timeout has elapsed, that is, when the destination node did not acknowledge the reception of the doorbell message in time.
1	Serial RapidIO Error (SE). Set when an ERROR response was received from the destination node.
0	Done Flag (DO). Set when the doorbell message was correctly transmitted, that is, when the processing core received a DONE response from the destination node.

*Table 1151.*GRSRIO doorbell message transmission buffer word 3 (address offset 0xC)

31 0
TIMESTAMP(_MSW_/_LSW)

31: 0	Message Time-Stamp (TIMESTAMP). When *g_hyb_que* is set to “false” 64 bit timestamps are not supported and this is the LSW of the local timer when message transmission was completed, that is when the response is received (with or without an error). When *g_hyb_que* is set to “false” it is the MSW instead.

The fields below exist only when *g_hyb_que* is set to “true” (hybrid-queues mode).

*Table 1152.*GRSRIO doorbell message transmission buffer word 4 (address offset 0x10)

31 0
TIMESTAMP(_LSW)

31: 0	Least significant Word of the Time-Stamp: LSW of the local timer when message transmission was completed, that is when the response is received (with or without an error), captured just before the “Transmission interrupt” is triggered.

*Table 1153.*GRSRIO doorbell message transmission buffer word 5 (address offset 0x14)

31 0
RESERVED

31: 0	Reserved

*Table 1154.*GRSRIO doorbell message transmission buffer word 6 (address offset 0x18)

31 0
RESERVED

31: 0	Reserved

*Table 1155.*GRSRIO doorbell message transmission buffer word 7 (address offset 0x1C)

31	2	1	0
RESERVED		DES_TYP	

31: 2	Reserved
1: 0	Descriptor Type (DES_TYP): indicates which kind of descriptor this is when in hybrid queues mode. Must be set to 0b00 or to 0b11 to indicate that this is a doorbell descriptor.

65.2.5 Inbound I/O operations

Inbound memory I/O operations can gain direct access to the local memory. The GRSRIO logical layer supports all memory I/O operations except of MAINTENANCE Read, Write and Port-Write Requests since these operations are already handled by the SRIO End-Point. The core provides both memory protection on physical addresses and address translation by means of two independent sets of partitions and windows.

When *CFG_AW* = 32 (local addresses of 32 bits), the physical address is decided according to SRIO Address(33:0), effectively allowing to handle a virtual memory space bigger than the physical one. The values of Address(33:30) are used to decide which TRNSWIN_CONF.WIN_ADDR to use in the final result of the translation. The physical address is then calculated by the following formula:

Physical Address = TRNSLWIN.WIN_ADDR (window *i*) &
SRIO Address((27- RXIO_CONF.ADDR_SHIFT):0)

Where *i* is the non negative integer found in Address(33:30), “&” is the concatenation operator and i is the index of the hit translation window.

When *CFG_AW = 64* (local addresses of 64 bits), the physical address is decided according to the SRIO Address(65:0), effectively allowing the handling of a virtual memory space bigger than the physical one. The values of Address(65:62) are used to decide which TRNSWIN_-CONF.WIN_ADDR in the final result of the translation. The physical address is then defined by the following formula:

Physical Address = TRNSLWIN.WIN_ADDR (window *i*) &
SRIO Address((59-RXIO_CONF.ADDR_SHIFT):0)

Where *i* is the non negative integer found in Address(65:62) and “&” is the concatenation operator.

The translation windows are all disabled by default and only the ones enabled by setting the respective TRNSWIN.EN to “1” are kept into account for translation. If no enabled translation windows are hit, the physical address is obtained directly assigning the value of SRIO Address(31:0) to the physical address in case of *CFG_AW = 32* and SRIO Address(63:0) to the physical address in case of in case of *CFG_AW = 64*.

Remote memory access is by default deactivated. The software can activate up to four (if *g_8_in_win* is set to “false”) or eight (if *g_8_in_win* is set to “true”) memory partitions using the switches MEMPRT.PWE for writing and MEMPRT.PRE for reading each partition. Operations trying to read from a partition where read is not enable or writing in a partition where writing is not enabled are ignored and the GRSRIO logical layer replies an ERROR response to the destination node in such a case.

The start address of each partition is defined in the respective MEMPRT.PART_ADDR. These fields contain the upper 12 bits of such address. The size of each partition can be adjusted by setting a corresponding mask value in the respective MEMPRT.PART_MASK.

A physical address of an inbound memory I/O operation falls into the memory protection partition *i* if it satisfies the following condition:

(Physical Address (CFG_AW-1:CFG_AW-11) **xor** MEMPRT.PART_ADDR (partition *i*))
and MEMPRT.PART_MASK (partition *i*)= 0x000

In this case, a mask value of 0xFFF defines the smallest possible partition with a size of 1MB and a mask value of 0x000 creates a partition that spans the whole 32-bit wide memory space. In this case, a

mask value of 0xFFF defines the smallest possible partition with a size of 4GB and a mask value of 0x000 creates a partition that spans the whole 64-bit wide memory space. In the next release (GEN3) it is planned to have a mask value of 0xFFF to define the smallest possible partition with a size of 1MB and a mask value of 0x000 to define partitions of 4GB.

The software can set up two types of interrupts: Memory access interrupts (RXIO_CTRL.IM) are triggered after each successful memory access, error interrupts (RXIO_CTRL.IE) are triggered in case of bus errors or forbidden memory access error, that is, when the destination node tries to access a memory space, which is either not covered by a partition or which does not allow write or read access.

For debug purposes, the last accessed local memory address is logged in the read-only field RXIO_LACCESS_MSW (if *CFG_AW* is set to 64) and RXIO_LACCES(_LSW).

65.2.6 Transmitting Memory I/O operations

Outbound memory I/O operations are stored in one or more memory I/O or hybrid transmission queues. The desired number of transmission queues can be set by VHDL generic *g_no_io_tx* or *g_no_hyb_tx* at compile time.

If several transmission queues have messages ready to be sent, the one with the highest priority gets to transmit first. If more than one active queues have the highest priority, the arbitration between them is done with a round robin algorithm. However, the following conditions must be true:

- The queue is enabled.
- The memory I/O operation message has a priority level that can currently be accepted by the SRIO end point.

Each transmission queue is a circular buffer that is located in memory. Before activating the buffer, the memory start address of the circular buffer must be set in register TXIO_MADDR_MSW and TXIO_MADDR(_LSW) or TX_MADDR_MSW and TX_MADDR(_LSW) and its depth in the field register TXIO_CTRL.CBD or TX_CTRL.CBD. The queue can be configured to store between 2 and 65,536 memory I/O operation descriptors. Each descriptor has a size of 32 bytes and it is up to the software to reserve the necessary memory space for the whole circular buffer.

Each I/O descriptor for NREAD, NWRITE, NWRITE_R and SWRITE can define a number of operations with contiguous payload from 1 to 4096. This is done in order to be able to send contiguous data up to 1MB with a single descriptor (avoid dead time due to the opening and the closing of descriptor at the end of each operation). In this case the RapidIO address will be increased according to the formula below each time the packet will be sent, although the one contained in the descriptor will not be updated:

$$\text{RapidIO address} = (\text{EXT} \,\&\, \text{SRIO\_EXT\_ADDR} \,\&\, \text{SRIO\_ADDR} \,\&\, b000) + P_B * I_p$$

Where "&" is the concatenation operator, P_B is the length in bytes of the payload in each operation of the descriptor (defined by the field SIZE of the descriptor), I_p is the number of packets already sent from this descriptor, and EXT, SRIO_EXT_ADDR, SRIO_ADDR are the respective fields in the TX descriptor.

Each queue can be configured to trigger a set of interrupts: (i) error interrupts that indicate bus errors, SRIO errors and timeout errors (TXIO_CTRL.IE or TX_CTRL.IE), and (ii) transmission interrupts that indicate that a memory I/O operation was successfully transmitted (TXIO_CTRL.IT or TX_CTRL.IT). The generation of transmission interrupts can be further configured by setting the transmission interrupt mode bit (TXIO_CTRL.IM or TX_CTRL.IM). If set, a transmission interrupt is only triggered after the transmission queue became empty. If not set, the generation of transmission interrupts depends on the Enable Transmission Interrupt (TI) setting of the descriptor.

Each transmission queue has a fixed source ID (TXIO_SRC_ID or TX_SRC_ID), priority (TXIO_CTRL.PRIO or TX_CTRL.PRIO), critical request flow setting (TXIO_CTRL.CR or TX_CTRL.CR), virtual channel setting (TXIO_CTRL.VC) and transport type (TXIO_CTRL.TT or TX_CTRL.TT).

For each memory I/O operation individually, the destination ID (DEST_ID) can be set up in the corresponding descriptor.

Each transmission queue implements a request-to-response timeout mechanism that counts the time between the transmission of a memory I/O operation and a response from the destination node (in case of operations that require a response such as NWRITE_R or atomic transactions). This timeout can be configured globally in register TO_CONF. If the timeout elapses, the descriptor will be closed with the Timeout Error (TE) flag set and an error interrupt is generated if enabled.

A transmission queue serves one descriptor at a time. Anyway, more outstanding packets per queue (two, planned to be extended to 64 in future releases) is blocked while it is awaiting a response from the destination node. However, other transmission queues can be serviced in the meanwhile.

The circular buffer management between hardware and software is done via two descriptor pointers. The tail pointer in TXIO_TLPTR or TX_TLPTR is managed by hardware whereas the head pointer in TXIO_HDPTR or TX_HDPTR is managed by software.

The software can add one or more descriptors to the circular buffer and then activate them by increasing the head pointer value in TXIO_HDPTR or TX_HDPTR. Every time the GRSRIO logical layer transmits a new memory I/O operation successfully, it will increment the tail pointer to the next descriptor. The software can always check how many operations awaiting transmission are left in the buffer by subtracting the tail pointer value from the head pointer value.

Every time a new packet is sent the srcTID field of the packet is increased, except when NWRITE and SWRITE transactions are sent (they have no srcTID field).

The type of the operation is defined in field TYPE, and the read- or write size in field SIZE. The size field is the concatenation of wdptr and rdsize/wrsize (see also RapidIO Interconnect Specification Part 1), the possible values are listed in Table 1156.

- For NREAD operations, the data read from the destination node will be stored at the memory address defined in ADDR.
- For NWRITE, NWRITE_R and SWRITE operations, the data which should be written to the remote node must be stored at the address defined in ADDR.
- For ATOMIC Set, Clear, Increment and Decrement operations, the data returned from the destination node will be stored at the memory address defined in ADDR. It is always fixed to 8 bytes. However, only wdptr and rdsize combinations are allowed that modify 1, 2, or 4 bytes.
- For ATOMIC Test-and-Swap and Swap operations, both the data transmitted to the destination node (the “swap” data) and the data returned from the destination node is stored at the address defined in ADDR. It is always fixed to 8 bytes. But again, only wdptr and wrsize combinations are allowed that modify 1, 2, or 4 bytes.
- For ATOMIC Compare-and-Swap operations, both the data transmitted to the destination node (the “compare” data and the “swap” data) and the data returned from the destination node is stored at the address defined in ADDR. The outgoing data is fixed to 16 bytes, where the first 8 bytes store the “compare” data and the second 8 bytes the “swap” data. The data returned from the destination node has always 8 bytes. Like for the other ATOMIC transactions, only wdptr and wrsize combinations that modify 1, 2, or 4 bytes are allowed.
- For MAINTENANCE Read operations, the data read from the destination node will be stored at the memory address defined in ADDR. It can be 4 or 8 bytes long, therefore the SIZE field must be set to b0100, b1100 or b01011.

- For MAINTENANCE Write and Port-Write Request operations, the data which should be written to the remote node must be stored at the address defined in ADDR. It can be 4 or 8 bytes long, therefore the SIZE field must be set to b0100, b1100 or b01011.

*Table 1156.*Allowed combinations of wdptr and rdsize/wrsize for SIZE field

wdptr	rdsize/wrsize	No. of Bytes	Bytes Lanes	Notes
0	0000	1	10000000	
0	0001	1	01000000	
0	0010	1	00100000	
0	0011	1	00010000	
1	0000	1	00001000	
1	0001	1	00000100	
1	0010	1	00000010	
1	0011	1	00000001	
0	0100	2	11000000	
0	0101	3	11100000	
0	0110	2	00110000	
0	0111	5	11111000	
1	0100	2	00001100	
1	0101	3	00000111	
1	0110	2	00000011	
1	0111	5	00011111	
0	1000	4	11110000	
1	1000	4	00001111	
0	1001	6	11111100	
1	1001	6	00111111	
0	1010	7	11111110	
1	1010	7	01111111	
0	1011	8	11111111	
1	1011	16		
0	1100	32		
1	1100	64		
0	1101	96		only read
1	1101	128		
0	1110	160		only read
1	1110	192		only read
0	1111	224		only read
1	1111	256		

In the following, the relevant descriptor words of the memory I/O operations transmission queues are described:

*Table 1157.*GRSRIO I/O operation transmission descriptor word 0 (address offset 0x0)

31	0
ADDR_MSW	

31: 0 This field is effective only when the CFG_AW is set to 64.

*Table 1158.*GRSRIO I/O operation transmission descriptor word 1 (address offset 0x4)

31	0
ADDR(_LSW)	

31: 0 LSW Local Memory Start Address (LSW_ADDR). Lowest 32 bits of the address pointing to the start of the memory block storing the payload of the I/O write operation (NWRITE, NWRITE_R, SWRITE, MAINTENANCE Write and Port-Write Request) to be transmitted. For NREAD operations, this address is the start address where the received data will be stored. When CFG_AW = 32 this is the full 32-bit local memory address.

*Table 1159.*GRSRIO I/O operation transmission descriptor word 2 (address offset 0x8)

31	0
SRIO_EXT_ADDR	

31: 0 Serial RapidIO Extended Address (SRIO_EXT_ADDR). The extended 32 bits of a 66-bit physical address (bits 32:63 in big-endian notation).

*Table 1160.*GRSRIO I/O operation transmission descriptor word 3 (address offset 0xC)

31	30 29	28	0
R	EXT	SRIO_ADDR/HOP_CONF	

31 RESERVED

30: 29 Serial RapidIO XAMSBS Field (EXT). Most significant bits of a 66-bit physical address (bits 64:65 in big-endian notation).

28: 0 Serial RapidIO Address / Hop Count & Configuration Offset (SRIO_ADDR/HOP_CONF). Lower part of the RapidIO memory address. The least significant three bits of the address are not specified as they are always set to logic 0. Therefore, this field contains bits 0:28 (in big-endian notation) of the RapidIO address. In case of maintenance operations, this field contains the hop count (28:21) concatenated with the configuration offset value (20:0).

*Table 1161.*GRSRIO I/O operation transmission descriptor word 4 (address offset 0x10)

31	0
DEST_ID	

31: 0 Destination Identifier (DEST_ID). Rapid IO destination device identifier. If the GRSIO is configured for 8-bit identifiers, only the lower 8 bits are valid.

*Table 1162.*GRSRIO I/O operation transmission descriptor word 5 (address offset 0x14)

31 26	25 21	20 17	16	15 ¨4	3	2	1	0
RESERVED	SIZE	TYPE	TI	NIOOP	R	TE	SE	DO

31: 26 RESERVED

25: 21 I/O Operation Size (SIZE). Read or write size of I/O operation. Concatenation of wdptr and rdsize/wrsize.

*Table 1162.*GRSRIO I/O operation transmission descriptor word 5 (address offset 0x14)

20: 17	I/O Operation Type (TYPE). Type of the I/O operation: 0: NREAD, 1: NWRITE, 2: NWRITE_R, 3: SWRITE, 4: ATOMIC Set, 5: ATOMIC Clear, 6: ATOMIC Increment, 7: ATOMIC Decrement, 8: ATOMIC Test-and-Swap, 9: ATOMIC Swap, 10: ATOMIC Compare-and-Swap, 11: MAINTENANCE Read, 12: MAINTENANCE Write, 13: MAINTENANCE Port-Write Request, all others: reserved.
16	Enable Transmission Interrupt (TI). If set, the GRSRIO triggers an interrupt when the I/O operation was correctly transmitted, that is, when also the done flag DO is set. The interrupt is triggered after the DMA engine has finished all memory accesses related to this descriptor.
15: 4	Number of I/O operations (NIOOP): indicates how many I/O operations are defined by the descriptor (the number of I/O transactions with contiguous payload will be NIOOP+1). This functionality can be used (NIOOP greater than 0) only with NREAD, NWRITE,NWRITE_R and SWRITE descriptors. The maximum number of I/O operations definable by a single descriptor is 4096, which allows transfers up to 1 MB with a single descriptor (when SIZE is set to 0b11111).
3	Reserved
2	Timeout Error (TE). Set when the request-to-response timeout has elapsed, that is, when the destination node did not acknowledge the reception of the message (only for operations such as NWRITE_R that generate DONE responses).
1	Serial RapidIO Error (SE). Set when an ERROR response was received from the destination node.
0	Done Flag (DO). Set when the I/O operation was correctly transmitted, that is, when the processing core received a DONE response from the destination node (only for operations such as NWRITE_R that generate DONE responses).

*Table 1163.*GRSRIO I/O operation transmission descriptor word 6 (address offset 0x18)

31	0
TIMESTAMP	

31: 0	I/O Operation Time-Stamp (TIMESTAMP). LSW of the local timer when transmission of all the transactions defined by the descriptor is completed, that is when the last response is received. For requests without responses, the timestamp is set when the last request is generated. 64 bit timestamp are not supported Please confirm:

*Table 1164.*GRSRIO I/O operation transmission descriptor word 7 (address offset 0x1C)

31	2	1	0
RESERVED		DES_TYP	

31: 2	RESERVED
1: 0	Descriptor Type (DES_TYP): indicates which kind of descriptor this is when in hybrid queues mode. Must be set to 0b10 to indicate that this is a I/O descriptor.

65.3 MECS Time Synchronization Protocol

The core, combined with the SRIOGEN2-IP end point, implements the “MECS Time Synchronization Protocol” according to RapidIO specifications Rev 4.0 if *g_mecs* is set to “true”. SMECS are not implemented. “Enhanced” MECS events with cmd = i are signaled from and triggered in the end point as changes in the signal level of respectively MECS_CAPTURED_IN[i] and MECS_TRIGGER_OUT[i].

65.4 Bus Master interface

65.4.1 Overview

Atomicity of operations as a target is supported by the AHB Master. Atomicity of operations as a target is currently not supported by the AXI4 Master. For this reason, when the grsrio_gen2axi wrapper is used inbound atomic operations are discarded and flagged as unsupported transaction.

The generic_bm_x is designed to use a standard bus master interface in which the translation of bus master commands to AHB or AXI bus protocol is handled by the component. This way if an IP core is designed to handle memory accesses with the standard bus master interface, which is defined in this document, it can be made compatible to AHB or AXI buses without additional effort. In addition, memory access control is simplified since standard bus interface (AHB,AXI) features like boundary crossing, alignment requirements is handled by the generic_bm_x IP core and no special action needed on the standard bus mater interface. Furthermore, additional bus protocols apart from AHB or AXI might be added in the future. The generic_bm_x core has a variety of configuration options to simplify the memory access logic required for bus master interface and optimize the bus accesses on AHB or AXI bus.

Fig. 188 illustrates the overall block diagram of generic_bm_x. Front-End handles all the handshaking on the bus_master interface. Middle-End handles all the burst related operations and generate standard commands to the back-end interface. Back-end interface generates bus specific burst commands depending on the selected bus protocol type. For each specific bus protocol (AHB,AXI) the back-end component is changed.

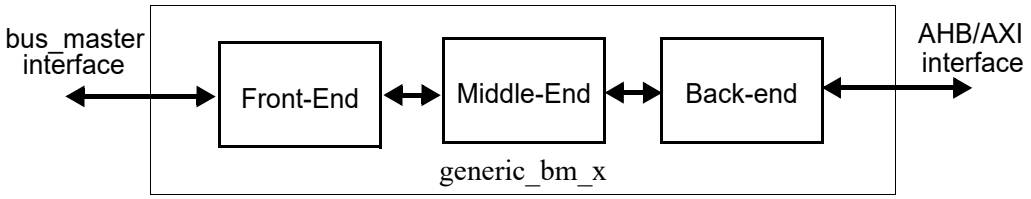


Figure 188. Overall block diagram of generic_bm_x

65.4.2 Configuration Options

MAX_SIZE: this generic determines the total maximum possible size of the burst on the bus master interface in terms of **bytes**. It has to be power of two. This generic also determines the width of the bmrd_size and bmwr_size input ports. This generic is fixed to 256 for GRSRIO core.

BM_DW: Data-width of the bus master interface in terms of **bits** and has to be a multiple of 32. This generic is fixed to 128 for GRSRIO core.

BE_DW: Data-width of the back-end bus in terms of **bits**. It can be equal or narrower compared to BM_DW and has to be a multiple of 32.

ADDR_WIDTH: Address width of the front-end and back-end bus.

MAX_BURST_LENGTH: Determines the maximum length of a burst transaction in terms of **number of beats** that is generated on the back-end bus. This generic can be useful if the maximum burst length needs to be limited to have fair arbitration in the system. It should be noted that the total maximum size of the burst in terms of bytes that is generated on the back-end bus depends on the be_dw

and can be calculated with the formula “number_of_beats*(be_dw/8)”. Limiting the maximum burst length can reduce the throughput hence it is recommended not be limited unless there is a need, for example due to arbitration fairness on the back-end bus side. In order to calculate the maximum possible burst length the following formula can be used “max_size/(be_dw/8)” and max_burst_length generic can not exceed this value. Also if max_size is bigger than the allowed burst_chop_mask value for the specific bus protocol then max_size can be replaced with maximum burst_chop_mask value since the total allowed burst size in terms of bytes can not exceed maximum burst_chop_mask value.

BURST_CHOP_MASK: Determines when a burst should end a new burst should start on the back-end bus in terms of **byte alignment.** Maximum and default value of this generic depends on the back-end protocol. Maximum value is 1024 bytes for AHB and 4096 bytes for AXI which is determined by the protocol specifications. Reducing the byte alignment might be useful when combined with max_burst_length in cases where the memory that is accessed by the back-end bus has an internal buffer which gives better throughput on specific alignments. For example if max_burst_length is limited to 8 beats on a 32-bit bus and a slave memory gives the best throughput when bursts are aligned to 32-byte boundary than burst_chop_mask can be set to 32. This way, if a burst on the bus_master front and starts with an address which is not aligned to 32-bytes, the first burst will be limited to finish on 32-byte alignment so that the remaining bursts will be always aligned to 32-bytes. It should be noted that, value of this generic is not recommended to be reduced from the default value unless a specific optimization is needed as explained in this chapter , otherwise the throughput will be reduced unnecessarily.

BE_RD_PIPE: When it is set to zero a pipeline stage exists between the read data path of the back-end bus to the read data-path of the bus_master interface. When set to one, this pipeline stage is removed. Setting this value to zero reduces read latency by one for aligned accesses but if the timing requirements do not met it can be set to a non-zero value.

UNALIGN_LOAD_OPT: When set to one, unaligned load optimization is enabled. When the optimization is enabled and a burst access do not finish exactly at the end of the data word of the back-end bus, then instead of generating a separate narrow access for the last word, the entire word is read and the corresponding part is used. This reduces the latency for unaligned burst accesses. But since this optimization reads more data than requested it should not be activated if the data is going to be read from a FIFO-like structure otherwise it can cause data loss.

EXCL_ENABLED: This generic only exists in AHB back-end bus and not compatible with the AXI back-end bus. When set to true it generates locked accesses on the AHB bus. This generic is fixed to true with the AHB back-end. GRSRIO core supports atomic transactions only when using AHB back-end.

65.4.3 Access Alignment

The generic_bm_x IP core does not have any alignment restriction on the bus_master interface. All accesses on the bus_master interface will be translated to access types that are allowed by the back-end bus. If the start address of an access is unaligned relative to the back-end bus, the first accesses on the back-end bus will be narrow accesses until the address reaches to an aligned value. After that a burst access will be generated as much as the size allows. If the ending is not aligned the last accesses will also be narrow accesses. For highest throughput the accesses should be aligned relative to the back-end bus width.

The generic_bm_x IP core will handle the boundary crossing for the back-end bus hence there is no restriction on the start address or the size of the burst on the bus_master interface. But since the burst has to restart on boundary crossing, in order to achieve high throughput with long bursts, the start address should be aligned such a way that boundary crossings are eliminated or minimized.

65.4.4 Endianness

The endianness on the back-end side is always big-endian. On the bus-master interface the most significant byte of the access is always placed to the uppermost bits (relative to the vhdl std_logic_vec-

tor). It should be noted that, the bus_master interface is not byte-invariant. Regardless of the access size or start address, the data word that is outputted do not have any gaps and the most significant byte of the access is placed to the uppermost bits and the remaining data follows to the low order bits.

In order to achieve big-endianness on the AXI back-end bus the bytes are swapped since the AXI protocol is byte-invariant. Following examples shows different access patterns with different back-end bus protocols and data-widths. For all accesses the bit position is relative to the std_logic_vector used in VHDL.

Fig. 189 illustrates a 16Byte access on both AHB and AXI backends, when both BM_DW and BE_DW generics are set to 128. Fig. 190 illustrates a 16 Byte access on both AHB and AXI backends, when BM_DW is set to 128 and BE_DW is set to 64. Fig. 191 illustrates a 2 Byte access on both AHB and AXI backends, when BM_DW is set to 128 and BE_DW is set to 64.

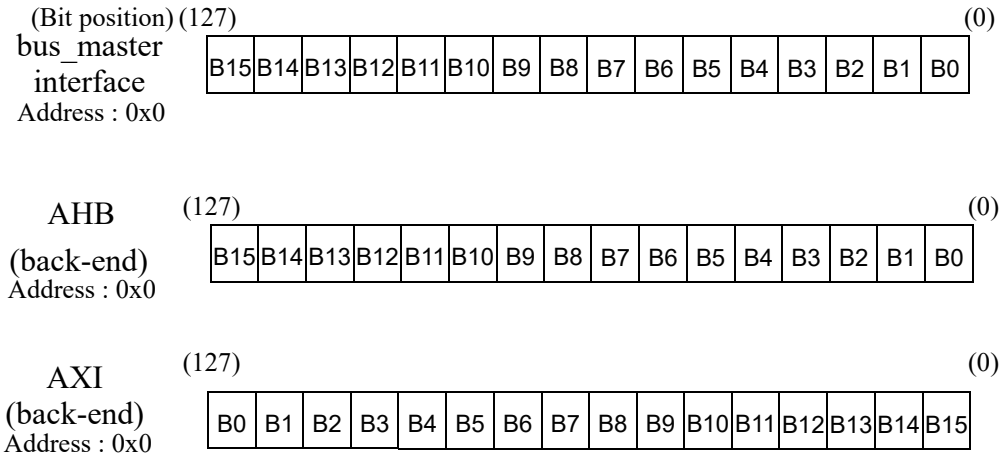


Figure 189. 16 Byte Access on AHB and AXI back-ends (BM_DW=128-bit, BE_DW=128-bit)

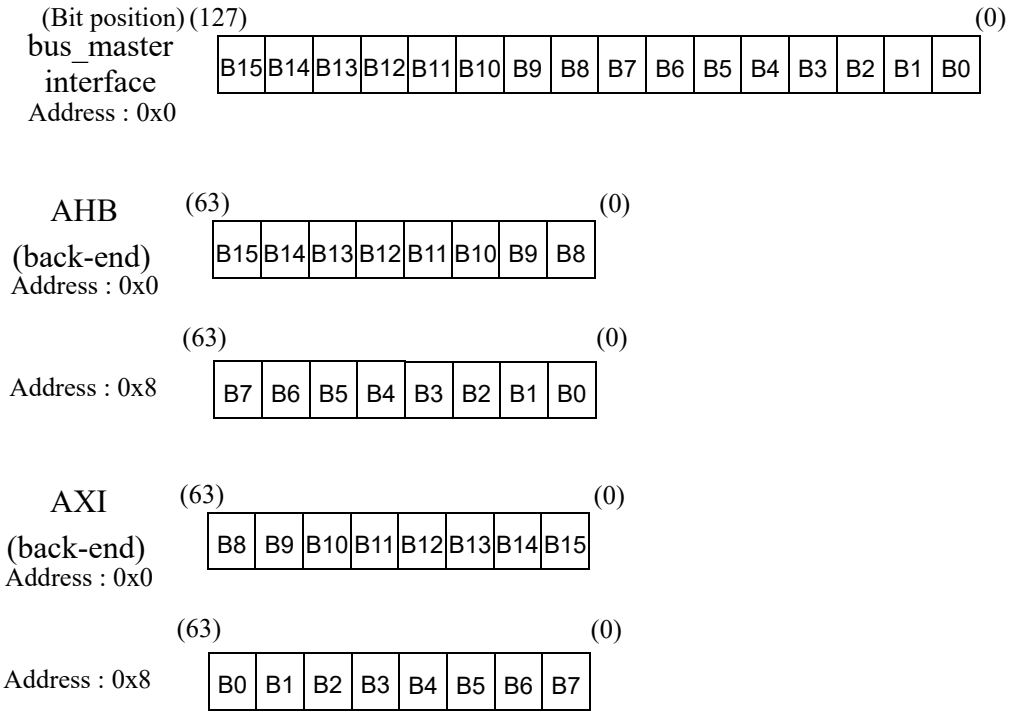


Figure 190. 16 Byte Access on AHB and AXI back-ends (BM_DW=128-bit, BE_DW=64-bit)

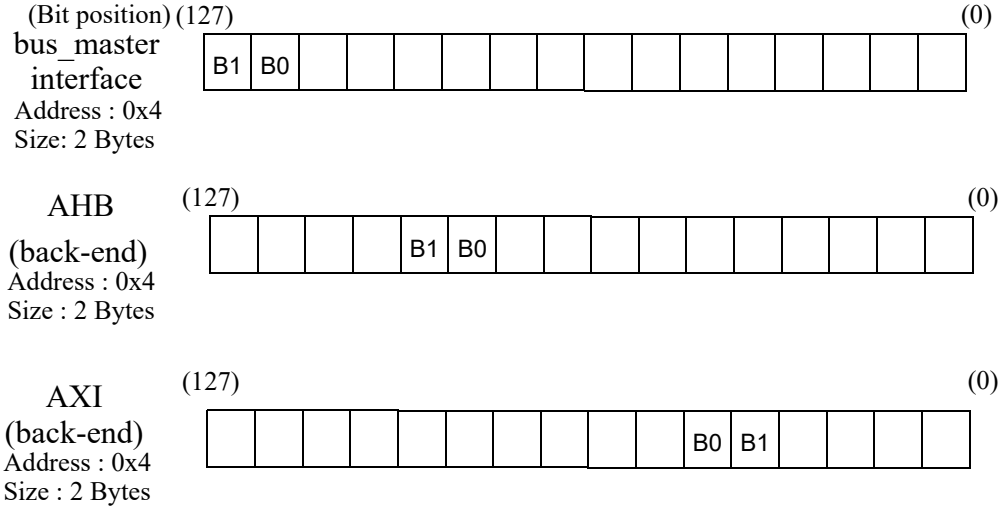


Figure 191. 2 Byte Access on AHB and AXI back-ends (BM_DW=128-bit, BE_DW=128-bit)

65.4.5 Software Considerations

The bus master interface of the GRSRIO core does not have any alignment restriction. But alignment can be important to achieve low latency and high throughput. In order to improve latency of doorbell messages (where the payload is contained in the descriptor), the descriptor should be aligned to 16 Byte boundary. When transmitting packets with 256 Byte payload, the best throughput can be achieved if data-packet is aligned to 256 Byte boundary since it will avoid boundary crossing on both AHB and AXI.

65.5 Registers

The core is programmed through registers mapped into APB address space. The registers are listed in table and described in detail in the subsequent tables. Addresses not listed in table are reserved. A read access to a reserved register, or reserved field with a register, will always return zero, and a write access has no effect. The register layout used is exemplified in table 1166, and the values used in the reset value row and field type row are explained in tables 1167 and 1168.

To easily support allocation of hardware resources to software entities, the address space for each hardware resource (queues, translation windows, memory protection partitions) are placed on 4KB boundaries.

Internally, the GRSRIO core decodes the address as listed in table 1165:

Table 1165. Decoding of ABP address

Bits	Description
19:17	Type of register block.
16:12	Index of queues/windows/partitions
11:2	Number of register.

The memory map has a size of 1MB and must also be aligned to 1MB boundaries.

Table 1166.<APB address offset> - <Register acronym> - <Register name>

31 24	23 16	15 8	7 0
EF3	EF2	EF1	EF0
<Reset value for EF3>	<Reset value for EF2>	<Reset value for EF1>	<Reset value for EF0>
<Bit-field type for EF3>	<Bit-field type for EF2>	<Bit-field type for EF1>	<Bit-field type for EF0>

31: 24 Example bit-field 3 (EF3) - <Bit-field description>
23: 16 Example bit-field 2 (EF2) - <Bit-field description>
15: 8 Example bit-field 1 (EF1) - <Bit-field description>
7: 0 Example bit-field 0 (EF0) - <Bit-field description>

Table 1167. Reset value definitions

Value	Description
0	Reset value 0. Used for single-bit fields.
1	Reset value 1. Used for single-bit fields.
0xNN	Hexadecimal representation of reset value. Used for multi-bit fields.
n/r	Field not reseted
*	Special reset condition, described in textual description of the bit-field. Used for example when reset value is taken from an input signal.

Table 1168. Bit-field type definitions

Value	Description
r	Read-only. Writes have no effect.
rw	Readable and writable.
rw*	Readable and writable. Special condition for write, described in textual description of the bit-field.
wc	Write-clear. Readable, and cleared when written with a 1. Writing 0 has no effect.

*Table 1169.*GRSRIO registers when *g_hyb_que* is set to false.

APB address offset	**Register**
0x00000	CORE_CAP
0x00004	CORE_RST
0x00008	TO_CONF
0x0000C	CORE_STAT
0x00010	INT_TXMSG_STAT
0x00014	INT_RXMSG_STAT
0x00018	INT_TXDBL_STAT
0x0001C	INT_RXDBL_STAT
0x00020	INT_TXIO_STAT
0x00024	INT_RXIO_STAT
0x00028	EXTDBL_CTRL
0x0002C	EXTDBL_FLTR
0x00030	EXTDBL_SRC_ID
0x00034	EXTDBL_DEST_ID
0x00038	ADDRTRNSL_SHIFT
0x10000+ i*0x1000	TRNSLWIN_CONF (window *i*)
0x20000+ i*0x1000	MEMPRT_CONF (partition *i*)
0x40000 + i*0x1000	TXMSG_CTRL (queue i)
0x40004 + i*0x1000	TXMSG_STAT (queue i)
0x40008 + i*0x1000	TXMSG_SRC_ID (queue i)
0x40010 + i*0x1000	TXMSG_TLPTR (queue i)
0x40014 + i*0x1000	TXMSG_HDPTR (queue i)
0x40018 + i*0x1000	TXMSG_MADDR_MSW[1] (queue i)
0x4001C + i*0x1000	TXMSG_MADDR(_LSW) (queue i)
0x60000 + i*0x1000	RXMSG_CTRL (queue i)
0x60004 + i*0x1000	RXMSG_STAT (queue i)
0x60008 + i*0x1000	RXMSG_DST_ID (queue i)
0x6000C + i*0x1000	RXMSG_DST_MSK (queue i)
0x60010 + i*0x1000	RXMSG_TLPTR (queue i)
0x60014 + i*0x1000	RXMSG_HDPTR (queue i)
0x60018 + i*0x1000	RXMSG_MADDR_MSW[1] (queue i)

*Table 1169.*GRSRIO registers when *g_hyb_que* is set to false.

APB address offset	Register
0x6001C + i*0x1000	RXMSG_MADDR(_LSW) (queue i)
0x80000 + i*0x1000	TXDBL_CTRL (queue i)
0x80004 + i*0x1000	TXDBL_STAT (queue i)
0x80008 + i*0x1000	TXDBL_SRC_ID (queue i)
0x80010 + i*0x1000	TXDBL_TLPTR (queue i)
0x80014 + i*0x1000	TXDBL_HLPTR (queue i)
0x80018 + i*0x1000	TXDBL_MADDR_MSW[1] (queue i)
0x8001C + i*0x1000	TXDBL_MADDR(_LSW) (queue i)
0xA0000+ i*0x1000	RXDBL_CTRL (queue i)
0xA0004 + i*0x1000	RXDBL_STAT (queue *i*)
0xA0008 + i*0x1000	RXDBL_ID (queue *i*)
0xA000C+ i*0x1000	RXDBL_MSK (queue *i*)
0xA0010+ i*0x1000	RXDBL_TLPTR (queue *i*)
0xA0014+ i*0x1000	RXDBL_HLPTR (queue *i*)
0xA0018+ i*0x1000	RXDBL_MADDR_MSW[1] (queue *i*)
0xA001C+ i*0x1000	RXDBL_MADDR(_LSW) (queue *i*)
0xC0000+ i*0x1000	TXIO_CTRL (queue *i*)
0xC0004+ i*0x1000	TXIO_STAT (queue *i*)
0xC0008+ i*0x1000	TXIO_SRC_ID (queue *i*)
0xC0010+ i*0x1000	TXIO_TLPTR (queue *i*)
0xC0014+ i*0x1000	TXIO_HDPTR (queue *i*)
0xC0018+ i*0x1000	TXIO_MADDR_MSW[1] (queue *i*)
0xC001C+ i*0x1000	TXIO_MADDR(_LSW) (queue *i*)
0xE0000	RXIO_CTRL
0xE0004	RXIO_STAT
0xE0008	RXIO_LACCESS_MSW[1]
0xE000C	RXIO_LACCESS(_LSW)
0xE0010	RXIO_LADDR_MEM_ERR_MSW[1]
0xE0014	RXIO_LADDR_MEM_ERR(_LSW)
0xE0018	RXIO_CNTRS

Where *i* is (depending on the register):

- the index of the queue for each type, configurable with generics *g_no_io_tx*, *g_no_dbell_rx*, *g_no_dbell_tx*, *g_no_msg_rx* and *g_no_msg_tx* at compile time (from 0 up to 31)
- the index of the translation window (from 0 to 15)
- the index of the memory protection partition (from 0 up to 3 or 7, depending if *g_8_in_win* is set to false or true)

[1] This field is reserved when *CFG_AW = 32*

*Table 1170.*GRSRIO registers when *g_hyb_que* is set to true.

APB address offset	Register
0x00000	CORE_CAP
0x00004	CORE_RST
0x00008	TO_CONF
0x0000C	CORE_STAT
0x00010	TX_INT_STAT
0x00014	RXMSG_INT_STAT
0x0001C	RXDBL_INT_STAT
0x00024	RXIO_INT_STAT
0x00028	EXTDBL_CTRL
0x0002C	EXTDBL_FLTR
0x00030	EXTDBL_SRC_ID
0x00034	EXTDBL_DST_ID
0x00038	ADDRTRNSL_SHIFT
0x10000+ i*0x1000	TRNSLWIN_CONF (window *i*)
0x20000+ i*0x1000	MEMPRT_CONF (partition *i*)

*Table 1170.*GRSRIO registers when *g_hyb_que* is set to true.

APB address offset	Register
0x40000 + i*0x1000	TX_CTRL (queue i)
0x40004 + i*0x1000	TX_STAT (queue i)
0x40008 + i*0x1000	TX_SRC_ID (queue i)
0x40010 + i*0x1000	TX_TLPTR (queue i)
0x40014 + i*0x1000	TX_HDPTR (queue i)
0x40018 + i*0x1000	TX_MADDR_MSW[1] (queue i)
0x4001C + i*0x1000	TX_MADDR(_LSW) (queue i)
0x60000 + i*0x1000	RXMSG_CTRL (queue i)
0x60004 + i*0x1000	RXMSG_STAT (queue i)
0x60008 + i*0x1000	RXMSG_DST_ID (queue i)
0x6000C + i*0x1000	RXMSG_DST_MSK (queue i)
0x60010 + i*0x1000	RXMSG_TLPTR (queue i)
0x60014 + i*0x1000	RXMSG_HDPTR (queue i)
0x60018 + i*0x1000	RXMSG_MADDR_MSW[1] (queue i)
0x6001C + i*0x1000	RXMSG_MADDR(_LSW) (queue i)
0xA0000+ i*0x1000	RXDBL_CTRL (queue i)
0xA0004 + i*0x1000	RXDBL_STAT (queue *i*)
0xA0008 + i*0x1000	RXDBL_ID (queue *i*)
0xA000C+ i*0x1000	RXDBL_MSK (queue *i*)
0xA0010+ i*0x1000	RXDBL_TLPTR (queue *i*)
0xA0014+ i*0x1000	RXDBL_HLPTR (queue *i*)
0xA0018+ i*0x1000	RXDBL_MADDR_MSW[1] (queue *i*)
0xA001C+ i*0x1000	RXDBL_MADDR(_LSW) (queue *i*)
0xE0000	RXIO_CTRL
0xE0004	RXIO_STATUS
0xE0008	RXIO_LACCESS_MSW[1]
0xE000C	RXIO_LACCESS_LSW
0xE0010	RXIO_LADDR_MEM_ERR_MSW[1]
0xE0014	RXIO_LADDR_MEM_ERR(_LSW)
0xE0018	RXIO_CNTRS

The following registers are available only when *g_mecs* is set to true, otherwise they are reserved.

*Table 1171.*Additional GRSRIO registers available when g_mecs is set to true.

APB address offset	Register
0xF0000	RESERVED
0xF0004	Timestamp CAR
0xF0008	Timestamp Generator Status CSR
0xF000C	MECS Tick Interval CSR
0xF0010	RESERVED
0xF0014	MECS Next Timestamp MSW
0xF0018	MECS Next Timestamp LSW
0xF001C	RESERVED
0xF0020	MECS Implementation Specific Settings
from 0xF0024 to 0xF0030	RESERVED
0xF0034	Timestamp Generator MSW CSR
0xF0038	Timestamp Generator LSW CSR

65.5.1 General registers

*Table 1172.*CORE_CAP - Core Capability Register

31 27	26 22	21 17	16 12	11 7	6 4	3	2	1	0
NO_TX_HYB_MSG	NO_RX_MSG	NO_TX_DBL	NO_RX_DBL	NO_TX_IO	RESERVED	AXI	NP	HM	MS
*	*	*	*	*	0	*	*	*	*
r	r	r	r	r	r	r	r	r	r

31: 27 Number of hybrid transmission queues or transmission queues for Data Messages (NO_TX_HYB_MSG): Number of transmission queues in hybrid mode (when g_hyb_que is set to “true”) or for Data Messages (when g_hyb_que is set to false) available in the core.

26: 22 Number of reception queues for Data Messages (NO_RX_MSG): Number of reception queues for data messages available in the core.

21: 17 Number of transmission queues for Doorbell Messages (NO_TX_DBL): Number of transmission queues for doorbell available in the core, reads zero when in hybrid-queues mode.

16: 12 Number of reception queues for Doorbell Messages (NO_RX_DBL): Number of reception queues for doorbell messages available in the core.

11: 7 Number of transmission queues for IO operations (NO_TX_IO): Number of transmission queues for IO operations available in the core, reads zero when in hybrid-queues mode.

6: 4 RESERVED

3 AXI4 bus master: this bit is set to one in case an AXI4 bus master is used, otherwise if an AHB bus master is used this is set to 0.

2 Number of Partitions (NP): reads 1 if the core supports 8 memory protection partition (*g_8_in_win* = “true”), reads 0 if it supports just 4 of them.

1 Hybrid-queues Mode (HM): reads 1 if the core is instantiated in hybrid mode (*g_hyb_que* = “true”)

0 MECS Supported (MS): reads 1 if the core supports the MECS Time Synchronization Protocol (*g_mecs* = “true”)

*Table 1173.*CORE_RST - Core Reset Register

31	30 0
RS	RESERVED
0	0
rw	r

*Table 1173.*CORE_RST - Core Reset Register

31 GRSRIO Soft Reset (RS). Writing 1 resets the GRSRIO logical layer core. Always reads 0.

30: 0 RESERVED

*Table 1174.*TO_CONF - Timeout Configuration Register

31	0
TIMEOUT	
0xFFFFFFFF	
rw	

31: 0 Response-to-Request and Request-to-Response Timeout Value (TIMEOUT). The timeout value is expressed in clock cycles.

*Table 1175.*CORE_STAT - Core General Status Register

31 16	15 3	2	1	0
NUR	RESERVED	FE	UT	UR
0	0	0	0	0
r	r	wc	wc	wc

31: 16 Number of unexpected responses (NUR): number of received unexpected responses since last time UR was cleaned.

15: 3 RESERVED

2 Clock Domain Crossing FIFO Error (FE). This bit is set when the asynchronous FIFO overflows, which transfers credit information from the SRIO end point to the GRSRIO core. This is a fatal error that should only occur when the clock frequency of the GRSRIO is lower than the clock frequency of the SRIO end point user interface. Writing 1 clears this bit.

1 Unsupported Transaction (UT). This bit is set when the GRSRIO core receives an unsupported transaction. Writing 1 clears this bit.

0 Unexpected Response (UR). This bit is set when the GRSRIO core receives an unexpected response. Writing 1 clears this bit.

*Table 1176.*INT_TX/MSG_STAT - Data Message Transmission Queues or Hybrid Queue Interrupt Level 1 Register

31	0
TXMSGINT/TXINT	
0	
r	

31: 0 Interrupts in Message Transmission or Hybrid Queues (TXMSGINT/TXINT). A bit is set if an interrupt occurred in the message transmission queue (if g_hyb_que is set to false) or in the mixed queues (if g_hyb_que is set to true) with the index corresponding to the number of the bit. This field is read-only, the interrupts must be individually cleared in the respective TXMSG_STAT or TX_STAT.

*Table 1177.*INT_RXMSG_STAT - Data Message Reception Queues Interrupt Level 1 Register

31	0
RXMSGINT	
0	
r	

31: 0 Interrupts in Message Reception Queues (RXMSGINT). A bit is set if an interrupt occurred in the message reception queue with the index corresponding to the number of the bit. This field is read-only, the interrupts must be individually cleared for each queue in the respective RXMSG_STAT.

*Table 1178.*INT_TXDBL_STAT - Doorbell Message Transmission Queues Interrupt Level 1 Register

This register is available only when “g_hyb_que” is set to false.

31	0
TXDBELLINT	

*Table 1178.*INT_TXDBL_STAT - Doorbell Message Transmission Queues Interrupt Level 1 Register

This register is available only when “g_hyb_que” is set to false.

0
r

31: 0 Interrupts in Doorbell Transmission Buffers (TXDBELLINT). A bit is set if an interrupt occurred in the doorbell transmission buffer with the index corresponding to the number of the bit. This field is read-only, the interrupts must be individually cleared in the respective TXDBELLMSG1.

*Table 1179.*INT_RXDBL_STAT- Doorbell Messages Reception Queues Interrupt Level 1 Register

31	0
RXDBLINT	
0	
r	

31: 0 Interrupts in Doorbell Reception Buffers (RXDBLINT). A bit is set if an interrupt occurred in the doorbell reception buffer with the index corresponding to the number of the bit. This field is read-only, the interrupts must be individually cleared in the respective RXDBL_STAT.

*Table 1180.*INT_TXIO_STAT - IO Operations Transmission Queues Interrupt Level 1 Register - (0x00020)

This register is available only when g_hyb_que is set to “false”

31	0
TXIOINT	
0	
r	

31: 1 RESERVED

0 Interrupt in I/O operation transmission queue (TXIOINT). A bit is set if an interrupt occurred in the IO transmission queue with the index corresponding to the number of the bit. This field is read-only, the interrupts must be individually cleared in the respective RXDBL_STAT.

*Table 1181.*INT_RXIO_STAT - IO Operations Reception Queues Interrupt Level 1 Register

31	1	0
RESERVED		RI
0		0
r		r

31: 1 RESERVED

0 Interrupt in I/O operation reception unit (RI). This field is read-only, the interrupts must be cleared in the respective RXIO_STAT.

*Table 1182.*EXTDBL_CONF - External Doorbell Configuration Register

31 16	15 14	13 12	11	10	9 8	7 5	4	3	2	1	0
RCOUNT	RES	TT	VC	CR	PRIO	RESERVED	IB	IFB	DC	DO	DI
0	0	0	0	0	0	0	0	0	0	0	0
rw	r	rw	rw	rw	rw	r	rw	rw	rw	rw	rw

31: 16 External Outbound Doorbell Message Retry Count (RCOUNT). External outbound doorbell messages are automatically retried until the destination node either accepts the message or until the user-defined retry threshold level in this field is reached.

15: 14 RESERVED

*Table 1182.*EXTDBL_CONF - External Doorbell Configuration Register

13: 12	External Outbound Doorbell Message Transport Type (TT). If set to 0b00, the destination ID and source IDs of external outbound doorbell messages are 8-bit wide. If set to 0b01, the fields are 16-bit wide.
11	External Outbound Doorbell Message Virtual Channel Bit (VC). If set, the virtual channel bit of the external outbound doorbell message packet is also set.
10	External Outbound Doorbell Message Critical Request Flow Bit (CR). If set, the CRF bit of the external outbound doorbell message is also set.
9: 8	External Outbound Doorbell Message Priority (PRIO). Priority of the external outbound doorbell message. To avoid deadlock, the highest priority level is not allowed for request packets. If 0b11 is written to this field, it is automatically overwritten by 0b10.
7: 5	RESERVED
4	Ignore Doorbell Buffer (IB). If this bit is set and DO is set and the doorbell info matches DBCOMP (in case DC is also set), the GRSRIO core outputs the doorbell to the external port without storing it to any possibly set up doorbell reception buffer and therefore always returns a DONE response to the destination node. If the bit is not set, the doorbell message is also outputted to the external port, however, the GRSRIO core still tries to store it in a doorbell reception buffer. Then, the response type depends on the doorbell reception buffer. If a buffer is available and the doorbell message was successfully stored, the GRSRIO core returns a DONE response, otherwise a RETRY response.
3	Ignore Full Doorbell Buffer (IFB). In case DO is set and IB is not set but no free doorbell reception buffer is available (see above), the GRSRIO core always returns a DONE response.
2	Enable Doorbell Info Comparison (DC). If set and if DO is set, inbound doorbell messages are only forwarded to the external port if the doorbell info field matches the value in the DBCOMP field.
1	Enable Doorbell Output Signals (DO). If set, inbound doorbell messages are forwarded to the external port.
0	Enable Doorbell Input Signals (DI). If set, outbound doorbell messages can be generated through the external port.

*Table 1183.*EXTDBL_FLTR - Processing Core Configuration Register 2

31 16	15 0
DBMASK	DBCOMP
0	0
rw	rw

31: 16	Doorbell Message Mask Value (DBMASK). If DC and DO are set, inbound doorbell messages are compared with the compare value DBCOMP. If a bit is set in this mask field, the corresponding bit of DBCOMP is compared.
15: 0	Doorbell Message Compare Value (DBCOMP). If DC and DO are set, the doorbell message is only forwarded to the external port if the doorbell info field matches the value in this field.

*Table 1184.*EXTDBL_SRC_ID - Processing Core Configuration Register 4

31 0
SRC_ID
0
rw

31: 0	External Outbound Doorbell Message Destination ID (DEST_ID). Destination ID of all outbound doorbell messages generated through the external port.

*Table 1185.*EXTDBL_DST_ID - Processing Core Configuration Register 4

31 0
DST_ID
0
rw

31: 0	External Outbound Doorbell Message Destination ID (DEST_ID). Destination ID of all outbound doorbell messages generated through the external port.

*Table 1186.*ADDRTRNSL_SHIFT - Address Shift for Address Translation Register

31 4	3 0
RESERVED	ADDR_SHIFT
0	0
r	rw

31: 4 RESERVED

3: 0 ADDR_SHIFT: Address Shift for Address Translation: number of position the translated bits are right-shifted (when SHIFT = 0 the translated bits are placed in Physical Address (MSB: MSB-3))

*Table 1187.*TRNSLWIN_CONF- Translation Window Configuration Register

31 20	19 16	15 1	0
RESERVED	WIN_ADDR	RESERVED	TEN
0	0	0	0
r	rw*	r	rw*

31: 20 RESERVED

19: 16 Values of the translated 4 bits of the physical base address for this window. Writing to this field has only an effect when memory I/O operations are not enabled, that is, when EN is 0.

19: 16 RESERVED

0 Enable This Translation Window (TEN). Writing to this field has only an effect when memory I/O operations are not enabled, that is, when EN is 0.

*Table 1188.*MEMPRT_CONF - Configuration Register for Partition *i*

31	30	29 28	27 16	15 12	11 0
PRE	PWE	RES	PART_ADDR	RESERVED	PART_MASK
0	0	0	0	0	0
rw	rw	r	rw*	r	rw*

31 Enable Read for the partition (PRE): Enable Read from the partition

30 Enable Write for the partition (PWE): Enable Write in the partition

27: 16 Memory Partition Address (PART_ADDR). These 12 bits are compared to the most significant 12 bits of the corresponding physical address of the memory I/O operation address. Writing to this field has only an effect when the reception of memory I/O operations is not enabled, that is, when RXIO_CONF.EN is 0.

15: 12 RESERVED

11: 0 Memory Partition Mask (PART_MASK). The mask can be used to adjust the size of the memory partition. An incoming I/O operation's address falls into this memory partition if the following condition is true: (SRIO Address (MSB:MSB-11) XOR PART1_ADDR) AND PART1_MASK = 0x000. Writing to this field has only an effect when memory I/O operations are not enabled, that is, when EN is 0.

65.5.2 Transmission Queues Registers

*Table 1189.*TXMSG_CTRL/TXDBL_CTRL/TXIO_CTRL/TX_CTRL - Transmission queue configuration register

31 22	21 20	19	18	17 16	15 10	9 6	5	4	3	2	1	0
RESERVED	PRIO	CR	VC	TT	RESERVED	CBD	IM	IE	IT	ST	TP	EN
0	0	0	0	0	0	0	0	0	0	0	0	0
r	rw	rw	rw	rw	r	rw*	rw	rw	rw	rw	rw*	rw*

31: 22 RESERVED

21: 20 Priority (PRIO). Priority of the outbound message or IO operation packets. To avoid deadlock, the highest priority level is not allowed for request packets (if 0b11 is written to this field, it is automatically overwritten by 0b10)

19 Critical Request Flow Bit (CR). If set, the CRF bit of the outbound message or IO operation packet is also set.

18 Virtual Channel Bit (VC). If set, the virtual channel bit of the outbound message packet is also set.

17: 16 Transport Type (TT). If set to 0b00, the destination ID and source IDs of this transmission queue are 8-bit wide. If set to 0b01, the fields are 16-bit wide.

15: 10 RESERVED

9: 6 Circular Buffer Depth (CBD). Depth of the circular queue of this message transmission queue. A queue can be configured to store between 2 and 65,536 messages: Depth = 2^(CBD+1). Writing to this field has only an effect when the transmission queue is not enabled, that is, when EN is 0. Note that even if the size of the queue is 2^(CBD+1), setting the head point directly to this value will not enable the queue as only the least significant CBD+1 bits of the tail pointer will be compared to the CBD+1 least significant bit of the head pointer.

5 Transmission Interrupt Mode (IM). If set, a transmission interrupt is only generated after the transmission queue became empty, that is, when the tail pointer equals the head pointer. If not set, the generation of transmission interrupts depends on the setting of the corresponding TI bits in the transmission descriptor words.

4 Enable Error Interrupts (IE). If set, interrupts are generated for any kind of transmission or bus error related to this transmission queue.

3 Enable Transmission Interrupts (IT). If set, interrupts are generated for successful message or IO operation packets transmission. The way how the interrupts are generated depends on the Transmission Interrupt Mode (IM).

2 Stop on Transmission Error (ST). If set, the transmission queue is automatically disabled after a transmission error has occurred. The tail pointer is not incremented and is therefore pointing to the descriptor that was processed during the occurrence of the error, allowing the software to quickly initiate some error recovery procedure. The type of transmission error can be read from the descriptor and includes: Serial RapidIO Error, Retry Error, and Timeout Error. If not set, the DMA engine increments the tail pointer and processes the next descriptor (if available) in case of errors.

1 Enable two-outstanding-packets mode: if this bit is set to 1, when a single descriptor defines more than one packet, two packet will be transmitted without waiting for the reply to the first one. Writing to this field has only an effect when the transmission queue is not enabled, that is, when EN is 0.

0 Enable Transmission Queue (EN). If set, the DMA engine executes the operations defined in the descriptors queue until the circular buffer is empty, that is, until the tail pointer reaches the head pointer. Then, once the software increments the head pointer again, the transmission is automatically resumed. Writing 1 while the queue is disabled, enables the queue. Writing 0 while the queue is enabled disables the transmission queue. If a transmission is ongoing, the queue is disabled after processing the current descriptor. When disabled and after all memory accesses in conjunction with this descriptor have been completed, this bit clears to 0.

*Table 1190.*TXMSG_STAT/TXDBL_STAT/TXIO_STAT/TX_STAT - Transmission Queue Status Register

31 8	7	6	5	4	3	2	1	0
RESERVED	SR	SS	SW	TI	EI	BE	TE	TA
0	0	0	0	0	0	0	0	0
r	r	r	r	wc	wc	wc	wc	r

*Table 1190.*TXMSG_STAT/TXDBL_STAT/TXIO_STAT/TX_STAT - Transmission Queue Status Register

7	Two packet sent and one response received (SR): reads 1 when two packet have been sent from a descriptor defining the transmission of more packets and one response has been already received (in two-outstanding-packets mode) (two-outstanding-packets mode)
6	Two packets sent and no responses received (SS): reads 1 when two packet have been sent from a descriptor defining the transmission of more packets and no responses have been received (in two-outstanding-packets mode)
5	One packet sent and one waiting to be sent (SW): reads 1 when one packet has been sent from a descriptor defining the transmission of more packets and the second one is still waiting to be transmitted (in two-outstanding-packets mode)
4	Transmission Interrupt (TI). Indicates a transmission interrupt. Writing 1 clears this bit and the corresponding bit in the Interrupt Level 1 register.
3	Error Interrupt (EI). Indicates an error interrupt. Writing 1 clears this bit and the corresponding bit in the Interrupt Level 1 register.
2	Bus Error (BE). Set when a bus memory access error occurs while a descriptor in this queue is processed. The transmission queue is automatically disabled and the tail pointer is not incremented. Writing 1 clears the bit, writing 0 has no effect.
1	Transmission Error (TE). Set when a transmission error occurs while a descriptor in this queue is processed. The type of transmission error can be read from the descriptor and includes: Serial RapidIO Error, Retry Error, and Timeout Error. Writing 1 clears the bit, writing 0 has no effect.
0	Transmission Active (TA). Indicates that a transmission is ongoing. This bit remains high as long as the GRSRIO core has not closed the current descriptor.

*Table 1191.*TXMSG_SRC_ID/TXDBL_SRC_ID/TXIO_SRC_ID/TX_SRC_ID - Transmission Queue Source ID Register

31	0
SOURCE_ID	
0	
rw	

31: 0	Source Identifier (SOURCE_ID). Source ID of this transmission queue.

*Table 1192.*TXMSG_TLPTR/TX_TLPTR/TXDBL_TLPTR/TXIO_TLPTR - Transmission Queue Tail Pointer Register

31	16	15	0
RESERVED		TLPTR	
0		0	
r		rw*	

31: 16	RESERVED
15: 0	Message Transmission Queue Tail Pointer (TLPTR). The tail pointer is updated by the DMA engine and is therefore read-only during operation. It is incremented by one for each message that was successfully committed to the Serial RapidIO port. Writing to this field has only an effect when the transmission queue is not enabled, that is, when EN is 0. The software can flush a disabled queue by programming both the tail and head pointer to point to the same descriptor.

*Table 1193.*TXMSG_HDPTR/TXDBL_HDPTR/TXIO_HDPTR/TX_HDPTR - Transmission Queue Head Pointer

31	16	15	0
TLPTR_R		HDPTR	
0		0	
r		rw	

31: 16	Transmission Queue Tail Pointer (READ ONLY) (TLPTR_R): read only value of the tail pointer to allow the SW to know both head and tail pointer with just one access and take faster decisions.
15: 0	Transmission Queue Head Pointer (HDPTR). The head pointer is updated by software after setting up the messages or IO operations payload in memory and the corresponding descriptors in the circular buffer.

*Table 1194.*TXMSG_MADDR_MSW)/TXDBL_MADDR_MSW/TXIO_MADDR_MSW/TX_MADDR_MSW - Transmission Queue Most Significant Word Start Address Register

This register is available only when CFG_AW is set to 64.

31	0
MADDRESS_MSW	
0	
rw*	

31: 0 Most Significant Word of the Start Memory Address (MADDRESS_MSW). Address of the start of the queue containing the transmission descriptors. Writing to this field has only an effect when the transmission queue is not enabled, that is, when EN is 0. This register is reserved when *CFG_AW = 32*.

*Table 1195.*TXMSG_MADDR(_LSW)/TXDBL_MADDR(_LSW)/TXIO_MADDR(_LSW)/TX_MADDR(_LSW) - Transmission Queue Most Significant Word Start Address Register

31	0
MADDRESS(_LSW)	
0	
rw*	

31: 0 Least Significant Word of the Start Memory Address (MADDRESS(_LSW)). Address of the start of the queue containing the transmission descriptors. When *CFG*_AW = 64, this field indicates the LSW of such address. Writing to this field has only an effect when the transmission buffer is not enabled, that is, when EN is 0.

65.5.3 Message Reception Queues Register

*Table 1196.*RXMSG_CTRL - Message Reception Control Register, Queue i

31 23	22	21 16	15 10	9 6	5	4	3	2	1	0
MAX_SIZE	R	MBOXMSK	MBOX	CBD	IF	IE	IR	ST	R	EN
0	0	0	0	0	0	0	0	0	0	0
rw*	r	rw*	rw*	rw*	rw	rw	rw	rw	r	rw*

31: 23 Maximum allowed message size (MAX_SIZE). Only messages with a size up to MAX_SIZE are accepted in this queue. Maximum size of the message in multiples of 8 bytes: Maximum Size = (MAX_SIZE+1)*8 bytes. Writing to this field has only an effect when the reception queue is not enabled, that is, when EN is 0.

22 RESERVED

21: 16 Mailbox Mask (MBOXMSK). Using this mask field, ranges of mailbox numbers can be accepted. If a bit is set, the corresponding bit of the mailbox field MBOX is compared. The example in the data-sheet is wrong: the formula to accept a packet is: (RECEIVED ID XOR QUEUE ID) AND MASK = b000000. This means that to accept mailboxes from 0 to 3, ID must be set to b000000 and MASK must be b111100.

15: 10 Mailbox Number (MBOX). Only messages addressed to the here defined mailbox number are accepted. Writing to this field has only an effect when the reception queue is not enabled, that is, when EN is 0.

9: 6 Circular Buffer Depth (CBD). Depth of the circular buffer of this message reception queue. A queue can be configured to store between 2 and 65,536 messages: Depth = 2^(CBD+1). Writing to this field has only an effect when the reception queue is not enabled, that is, when EN is 0.

5 Enable Full Interrupts (IF). If set, an interrupt is generated each time the reception queue becomes full, that is, when also the FQ bit is set.

4 Enable Error Interrupts (IE). If set, interrupts are generated in case of reception errors or bus errors.

3 Enable Reception Interrupts (IR). If set, interrupts are generated for successful message receptions. Reception interrupts must be enabled for each descriptor individually by setting the corresponding RI bits in the message reception descriptors.

2 Stop on Reception Error (ST). If set, the reception queue is automatically disabled after a reception error has occurred. The tail pointer is not incremented and is therefore pointing to the descriptor that was processed during the occurrence of the error, allowing the software to quickly initiate some error recovery procedure. If not set, the DMA engine increments the tail pointer and processes the next descriptor (if available) in case of errors.

1 RESERVED

0 Enable Reception Queue (EN). If set, the DMA engine executes the reception of messages until the circular buffer is full, that is, until the address of the tail pointer equals the address of the head pointer - 1 (modulo buffer depth). Then, once the software increments the head pointer again, the reception is automatically resumed. Writing 1 while the queue is disabled, enables the queue. Writing 0 while the queue is enabled disables the reception queue. If a reception is ongoing, the queue is disabled after processing the current descriptor. When disabled and after all memory accesses in conjunction with this descriptor have been completed, this bit clears to 0.

*Table 1197.*RXMSG_STAT - Message Reception Status Register, Queue i

31 8	7	6	5	4	3	2	1	0
RESERVED	RI	EI	FI	WL	FQ	BE	RE	RA
0	0	0	0	0	0	0	0	0
r	wc	wc	wc	wc	wc	wc	wc	wc

31: 8 RESERVED

7 Reception Interrupt (RI). Indicates a reception interrupt. Writing 1 clears this bit and the corresponding bit in the Interrupt Level 1 register.

6 Error Interrupt (EI). Indicates an error interrupt. Writing 1 clears this bit and the corresponding bit in the Interrupt Level 1 register.

*Table 1197.*RXMSG_STAT - Message Reception Status Register, Queue i

5	Full Interrupt (FI). Indicates a full interrupt. Writing 1 clears this bit and the corresponding bit in the Interrupt Level 1 register.
4	Wrong Letter (WL). Set when a message with wrong letter number is received during the reception of a multi-packet message. Writing 1 clears the bit, writing 0 has no effect.
3	Full Queue (FQ). Set when the reception queue becomes full, that is, when the address of the tail pointer equals the address of the head pointer - 1 (modulo buffer depth). Writing 1 clears the bit, writing 0 has no effect.
2	Bus Error (BE). Set when a bus memory access error occurs while a descriptor in this queue is processed. The reception queue is automatically disabled and the tail pointer is not incremented. Writing 1 clears the bit, writing 0 has no effect.
1	Reception Error (RE). Set when a reception error occurs while a descriptor in this queue is processed. The type of reception error can be read from the descriptor and includes: Serial RapidIO Error and Truncation Error. Writing 1 clears the bit, writing 0 has no effect.
0	Reception Active (RA). Indicates that a reception is ongoing. This bit remains high as long as the GRSRIO core has not closed the current descriptor.

*Table 1198.*RXMSG_DEST_ID - Message Reception Acceptance ID Register, Queue i

31	0
DEST_ID_ACC	
0	
rw*	

31: 0	Accepted Destination ID (DEST_ID_ACC). Only messages addressed to the here defined destination ID are accepted. Writing to this field has only an effect when the reception queue is not enabled, that is, when EN is 0.

*Table 1199.*RXMSG_DEST_ID - Message Reception Mask ID Register, Queue i

31	0
DEST_ID_MASK	
0	
rw*	

31: 0	Accepted Destination ID Mask (DEST_ID_MASK). Using this mask field, ranges of destination IDs can be accepted. If a bit is set, the corresponding bit of the accepted destination ID field DEST_ID_ACC is compared. Writing to this field has only an effect when the reception queue is not enabled, that is, when EN is 0.

*Table 1200.*RXMSG_TLPTR - Message Reception Queue Tail Pointer Register, Queue i

31	16	15	0
RESERVED		TLPTR	
0		0	
r		rw*	

31: 16	RESERVED
15: 0	Message Reception Queue Tail Pointer (TLPTR). The tail pointer is updated by the DMA engine and is therefore read-only during operation. It is incremented by one for each message that was successfully stored to memory. Writing to this field has only an effect when the reception queue is not enabled, that is, when EN is 0. The software can flush a disabled queue by programming both the tail and head pointer to point to the same descriptor.

*Table 1201.*RXMSG_HDPTR - Message Reception Queue Head Pointer Register, Queue i

31 16	15 0
TLPTR_R	HDPTR
0	0
r	rw

31: 16 Message Reception Queue Tail Pointer (READ ONLY) (TLPTR_R): read only value of the tail pointer to allow the SW to know both head and tail pointer with just one access and take faster decisions.

15: 0 Message Reception Queue Head Pointer (HDPTR). The head pointer is updated by software after reserving the memory space for incoming messages and after setting up the descriptors in the circular buffer. The head pointer must be increased by one for each message that shall be received.

*Table 1202.*RXMSG_MADD_MSW - Message Reception Most Significant Word of the Start Address, Queue *i*

This register is only available when CFG_AW = 64.

31 0
MADDRESS_MSW
0
rw*

31: 0 Most Significant Word of the Reception Queue Start Memory Address (MADDRESS_MSW). Address pointing to the start of the memory block storing the descriptors of this queue. Writing to this field has only an effect when the reception queue is not enabled, that is, when EN is 0.

*Table 1203.*RXMSG_MADDR(_LSW) - Message Reception Least Significant Word of the Start Address, Queue *i*

31 0
MADDRESS(_LSW)
0
rw*

31: 0 Least Significant Word of the Reception Queue Start Memory Address (MADDRESS(_LSW)). Address pointing to the start of the memory block storing the descriptors of this queue. When CFG_AW is set to 64, it is the LSW of such address. Writing to this field has only an effect when the reception queue is not enabled, that is, when EN is 0.

65.5.4 Doorbell Message Reception Buffer Register

*Table 1204.*RXDBELL_CTRL - Doorbell Message Reception Configuration Register, Queue i

31 30 29 28 27 26 25 24 23 10	9 6	5	4	3	2 1	0
RESERVED	CBD	IF	IE	IR	RES	EN
0	0	0	0	0	0	0
r	rw*	rw	rw	rw	r	rw*

31: 10 RESERVED

9: 6 Circular Buffer Depth (CBD). Depth of this doorbell message reception buffer. A buffer can be configured to store between 2 and 65,536 doorbell messages: Depth = 2^(CBD+1). Writing to this field has only an effect when the reception buffer is not enabled, that is, when EN is 0.

15: 10 RESERVED

5 Enable Full Interrupts (IF). If set, an interrupt is generated each time the reception buffer becomes full, that is, when also the FB bit is set.

4 Enable Error Interrupts (IE). If set, interrupts are generated in case of bus errors.

3 Enable Reception Interrupts (IR). If set, interrupts are generated for successful doorbell message receptions. Reception interrupts must be enabled for each doorbell message individually by setting the corresponding RI bits in the reception buffer words.

2: 1 RESERVED

0 Enable Reception Buffer (EN). If set, the DMA engine executes the reception of doorbell messages until the circular buffer is full, that is, until the address of the tail pointer equals the address of the head pointer - 1 (modulo buffer depth). Then, once the software increments the head pointer again, the reception is automatically resumed. Writing 1 while the buffer is disabled, enables the buffer. Writing 0 while the buffer is enabled disables the reception buffer. If a reception is ongoing, the buffer is disabled after processing the current doorbell message. When disabled and after all memory accesses to this buffer entry have been completed, this bit clears to 0.

*Table 1205.*RXDBELLMSG_STAT - Doorbell Message Reception Status Register, Queue i

31 6	5	4	3	2	1	0
RESERVED	RI	EI	FI	FB	BE	RA
0	0	0	0	0	0	0
r	wc	wc	wc	wc	wc	r

5 Reception Interrupt (RI). Indicates a reception interrupt. Writing 1 clears this bit and the corresponding bit in the Interrupt Level 1 register.

4 Error Interrupt (EI). Indicates an error interrupt. Writing 1 clears this bit and the corresponding bit in the Interrupt Level 1 register.

3 Full Interrupt (FI). Indicates a full interrupt. Writing 1 clears this bit and the corresponding bit in the Interrupt Level 1 register.

2 Full Buffer (FB). Set when the reception buffer becomes full, that is, when the address of the tail pointer equals the address of the head pointer - 1 (modulo buffer depth). Writing 1 clears the bit, writing 0 has no effect.

1 Bus Error (BE). Set when a bus memory access error occurs while a doorbell message in this buffer is processed. The reception buffer is automatically disabled and the tail pointer is not incremented. Writing 1 clears the bit, writing 0 has no effect.

0 Reception Active (RA). Indicates that a reception is ongoing. This bit remains high as long as the GRSRIO core has not closed the current buffer entry.

*Table 1206.*RXDBL_MSK - Doorbell Reception Message Destination ID - Queue *i*

31	0
DEST_ID_ACC	
0	
rw*	

31: 0 Accepted Destination ID (DEST_ID_ACC). Only doorbell messages addressed to the here defined destination ID are accepted. Writing to this field has only an effect when the reception buffer is not enabled, that is, when EN is 0.

*Table 1207.*RXDBL_DST_MSK - Doorbell Reception Message ID Mask - Queue *i*

31	0
DEST_ID_MASK	
0	
rw*	

31: 0 Accepted Destination ID Mask (DEST_ID_MASK). Using this mask field, ranges of destination IDs can be accepted. If a bit is set, the corresponding bit of the accepted destination ID field DEST_ID_ACC is compared. Writing to this field has only an effect when the reception buffer is not enabled, that is, when EN is 0.

*Table 1208.*RXDBELL_TLPTR - Doorbell Message Reception, Queue i, Register 4

31	16	15	0
RESERVED		TLPTR	
0		0	
r		rw*	

31: 16 RESERVED

15: 0 Doorbell Message Reception Buffer Tail Pointer (TLPTR). The tail pointer is updated by the DMA engine and is therefore read-only during operation. It is incremented by one for each doorbell message that was successfully stored to memory. Writing to this field has only an effect when the reception buffer is not enabled, that is, when EN is 0. The software can flush a disabled buffer by programming both the tail and head pointer to point to the same buffer entry.

*Table 1209.*RXDBELL_HDPTR - Doorbell Message Reception, Queue i, Register 5

31	16	15	0
TLPTR_R		HDPTR	
0		0	
r		rw	

31: 16 Doorbell Message Reception Queue Tail Pointer (READ ONLY) (TLPTR_R): read only value of the tail pointer to allow the SW to know both head and tail pointer with just one access and take faster decisions.

15: 0 Doorbell Message Reception Queue Head Pointer (HDPTR). The head pointer is updated by software after setting up the buffer entries in the circular buffer. The head pointer must be increased by one for each doorbell message that shall be received.

*Table 1210.*RXDBL_MADDR_MSW - Doorbell Message Reception, Queue i

This register is only available when CFG_AW = 64.

31	0
MADDRESS_MSW	
0	
rw*	

31: 0 Most Significant Word of the Reception Buffer Start Memory Address (MADDRESS_MSW). Address pointing to the start of the memory block reserved for the reception of doorbell messages. Writing to this field has only an effect when the reception buffer is not enabled, that is, when EN is 0.

*Table 1211.*RXDBL_MADDR(_LSW) - Doorbell Message Reception, Queue i

31	0
MADDRESS(_LSW)	
0	
rw*	

31: 0 (Least Significant Word of the) Start Memory Address of the Doorbell Queues (MADDRESS_LSW). Address pointing to the start of the memory block reserved for the reception of doorbell messages. Writing to this field has only an effect when the reception buffer is not enabled, that is, when EN is 0.

65.5.5 I/O Operation Reception Unit Registers

*Table 1212.*RXIO_CONF - I/O Operation Reception Configuration Register

31	3	2	1	0
RESERVED		IE	IM	EN
0		0	0	0
r		rw	rw	rw*

31: 3 RESERVED

2 Enable Error Interrupts (IE). If set, interrupts are generated in case of bus errors or forbidden memory access errors.

1 Enable Memory Access Interrupts (IM). If set, interrupts are generated for successful memory I/O operations.

0 Enable Memory I/O (EN). If set, incoming memory I/O operations are executed by the DMA engine, otherwise packets are automatically rejected and an ERROR response is returned to the destination node (for those memory I/O operations that require a response). Writing 1 while memory I/O operations are disabled, enables them. Writing 0 while memory I/O operations are enabled disables them. If a memory access is ongoing, this access is allowed to finish. Then, once the access has been completed, this bit clears to 0.

*Table 1213.*RXIO_STAT - I/O Operation Reception Status Register

31	5	4	3	2	1	0
RESERVED		RI	EI	BE	ME	RA
0		0	0	0	0	0
r		wc	wc	wc	wc	r

31: 5 RESERVED

*Table 1213.*RXIO_STAT - I/O Operation Reception Status Register

4	Reception Interrupt (RI). Indicates a reception interrupt. Writing 1 clears this bit and the corresponding bit in the Interrupt Level 1 register.
3	Error Interrupt (EI). Indicates an error interrupt. Writing 1 clears this bit and the corresponding bit in the Interrupt Level 1 register.
2	Bus Error (BE). Set when a bus memory access error occurs while an inbound I/O operation is processed. The I/O reception unit is automatically disabled. Writing 1 clears the bit, writing 0 has no effect.
1	Forbidden Memory Access Error (ME). Set when an inbound I/O operation tries to access a forbidden memory address. Writing 1 clears the bit, writing 0 has no effect.
0	Reception Active (RA). Indicates that a reception is ongoing. This bit remains high as long as the GRSRIO core has not finished the memory access.

*Table 1214.*RXIO_LACCESS_MSW - Most Significant Word of the Last Access Register

This register is only available when *CFG_AW* is set to 64.

31	0
LACCESS_MSW	
0	
r	

31: 0	Most Significant Word of the Last Accessed Address Causing a Memory Error(LACCESS_MSW). The last accessed memory address can be read from this field.

*Table 1215.*RXIO_LACCESS(_LSW) - (Least Most Significant Word of the Last Access Register

31	0
LACCESS(_LSW)	
0	
r	

31: 0	Last Accessed Address (LACCESS(_LSW)). The last accessed memory address can be read from this field. When *CFG_AW = 64* this is the LSW of such address.

*Table 1216.*RXIO_LACCESS(_LSW) - (Least Most Significant Word of the Last Access Register

This register is only available when *CFG_AW* is set to 64.

31	0
LAST_MEM_ERR_ADDR_MSW	
0	
r	

31: 0	Last Accessed Address Causing a Memory Error (LACCESS(_LSW)). The last MSW of the last accessed memory address causing a memory error can be read from this field.

*Table 1217.*RXIO_LACCESS(_LSW) - (Least Most Significant Word of the Last Access Register

31	0
LAST_MEM_ERR_ADDR(_LSW)	
0	

*Table 1217.*RXIO_LACCESS(_LSW) - (Least Most Significant Word of the Last Access Register

r

31: 0 Last Accessed Address (LACCESS(_LSW)). The last accessed memory address causing a memory error can be read from this field. When *CFG_AW = 64* this is the LSW of such address.

*Table 1218.*RXIO_CNTRS - Reception Unit Events Counters Register

31 16	15 0
NME	NRI
0	0
r	r

31: 16 Number of Memory Error (NME): Number of memory errors occured since last time RXIO_STAT.ME was cleaned.

15: 0 Number of Reception Interrupts Error (NRI): Number of reception interrupts occured since last time RXIO_STAT.RI was cleaned.

65.5.6 MECS registers

The MECS registers are implemented according to RapidIO specification, Rev. 4.0 and only if *g_mecs* is set to “true”. Timestamp Generation Extension Block Header is not implemented, as MECS registers are not implemented together with the other CAR and CSR registers in the SRIOGEN2IP.

*Table 1219.*Timestamp CAR (T_CAR)- offset 0xF004

31 6	5	4	3	2	1	0
RESERVED	SS	MMS	MSS	CFS	TMS	TSS
0	0	1	1	0	0	0
r	r	r	r	r	r	r

31: 1 RESERVED

5 SMECS Supported: not supported (0)

4 MECS Master Supported: supported (1)

3 MECS Slave Supported: supported (1)

2 Common Clock Frequency supported (CFS): not supported (0)

1 Timestamp Master Supported (TMS): not supported (0)

0 Timestamp Slave Supported (TSS): not supported (0)

*Table 1220.*Timestamp Generator Status CSR (TGS_CSR) - offset 0xF008

31 4	3	2	1	0
RESERVED	WST	ST	R	CL
0	0	0	0	0
r	wc	r	r	r

31: 4 RESERVED

Table 1220. Timestamp Generator Status CSR (TGS_CSR) - offset 0xF008

3	Timestamp Generator Was Stopped: Indicates if the Timestamp Generator counter has not advanced because it has been set to an earlier time. 0b0 - Timestamp Generator has advanced continuously since this bit was last cleared 0b1 - Timestamp Generator has temporarily stopped advancing at least once since this bit was last cleared. This bit is cleared by writing "1" to it.
2	Timestamp Generator Stopped: Indicates if the Timestamp Generator counter is not advancing because it is being set to an earlier time. 0b0 - Timestamp Generator is advancing 0b1 - Timestamp Generator is temporarily not advancing
1	RESERVED
0	Timestamp Generator Clock Locked (CL): Indicates whether the Timestamp Generator counter is operating from a good clock source. 0b0 - Timestamp Generator is not operating with a good clock source. 0b1 - Timestamp Generator is operating with a good clock source.

Table 1221. MECS Tick Interval CSR (MTI_CSR) - (0xF00C)

31 8	7	6	5	4	3 2	1	0
TICK_INT	RES.		LS	LT	LSTHR	SS	SR
0	0		0	0	00	0	0
rw	r		wc	wc	rw	r	rw

31: 8	Tick Interval (TICK_INT): For a MECS Master, a MECS shall be sent when time has advanced by this many nanoseconds. For an MECS Slave, time has advanced by this many nanoseconds whenever an MECS is received. MECS transmission, and MECS timestamp synchronization for received MECS, is disabled when this register is 0.
7: 6	RESERVED
5	Lost TSG Sync Error Status: This field indicates that the device has detected at least "Lost TSG Sync Error Threshold" consecutive ticks have been lost. 0 - A Lost TSG Sync Error has not been detected 1 - A Lost TSG Sync Error has been detected This bit must be written with 1 to be cleared.
4	Lost Tick Error Status 0 This field indicates if the device has detected at least one lost tick. 0 - A Lost Tick Error has not been detected 1 - A Lost Tick Error has been detected This bit must be written with 1 to be cleared.
3: 2	Lost TSG Sync Error Threshold: controls the number of MECS/SMECS "ticks" that must be lost before declaring the timestamp generator to be out of sync. 0b00 - Lost Tick Error Threshold is disabled 0b01 - If one tick is lost, declare the timestamp generator out of sync 0b10 - If two ticks are lost, declare the timestamp generator out of sync 0b11 - If three ticks are lost, declare the timestamp generator out of sync

*Table 1221.*MECS Tick Interval CSR (MTI_CSR) - (0xF00C)

1	SMECS Selection (SS): The device uses MECS and doesn't support SMECS (0)
0	MECS Time synchronization Role: Controls whether a device operates as a MECS Master or MECS Slave. 0 - The device is operating as a MECS Slave 1 - The device is operating as a MECS Master

*Table 1222.*MECS Next Timestamp MSW CSR (NMSW_CSR) - offset 0xF0014

31	0
NMSW	
0	
rw	

31: 0	Most significant 32 bits for the timestamp value used to update the Timestamp Generator MSW CSR when a Multicast Event Control Symbol is received by an MECS Slave. Most significant 32 bits of the timestamp value compared with the Timestamp Generator value to determine when a Multicast Event Control Symbol must be transmitted by an MECS Master

*Table 1223.*MECS Next Timestamp LSW CSR (NLSW_CSR) - (0xF0018)

31	0
NLSW	
0	
rw	

31: 0	Least significant 32 bits for the timestamp value used to update the Timestamp Generator LSW CSR when a Multicast Event Control Symbol is received by an MECS Slave. Least significant 32 bits of the timestamp value compared with the Timestamp Generator value to determine when a Multicast Event Control Symbol shall be transmitted by an MECS Master

*Table 1224.*MECS Implementation Specific Settings Register (MECS_S) - (0xF0020)

31	30 28	27 16	15 11	10 8	7 0
EN	RES.	NS_LM	RESERVED	CMD	NS_CC
0	0	0xFFF	0	0	0
rw	r	rw	r	rw	rw

31	MECS Time Synchronization Protocol enabled when this field is set to 1.
30: 28	RESERVED
26: 16	Nanoseconds required to assume the MECS tick lost (NS_LM): when the MECS is set as a slave, the core assumes that the MECS tick is lost when this amount of nanoseconds is elapsed after the local timer reaches TICK_INT. When a tick is lost the Next Timestamp is incremented of MTI_CSR.TICK_INT.
15: 11	RESERVED
8: 10	CMD of the Enhanced MECS (CMD): when the node is a MECS master, this field indicates the CMD of the Enhanced MECS to be transmitted. When the node is a MECS slave, this field indicates the CMD of the last MECS received, all values are considered valid ticks.
0: 7	Increment of local timer in nanoseconds every clock cycles: the Timestamp Generator will be incremented of NS_CC every clock cycles. This field must be set accordingly to the frequency of the systems (some examples below)

*Table 1225.*MECS Timestamp Generator MSW CSR (MSW_CSR)- offset 0xF0034

31	0
MSW	
0	
rw	

*Table 1225.*MECS Timestamp Generator MSW CSR (MSW_CSR)- offset 0xF0034

31: 0	MSW Bits: Most significant 32 bits for the timestamp generator.

*Table 1226.*MECS Timestamp Generator LSW CSR (LSW_CSR)- offset 0xF0038

31	0
LSW	
0	
rw	

31: 0	LSW Bits: Least significant 32 bits for the timestamp generator.

65.6 External doorbell interface

65.6.1 Outbound doorbell messages

The following timing diagram illustrates how outbound doorbell messages can be generated through the external interface (if this feature is enabled):

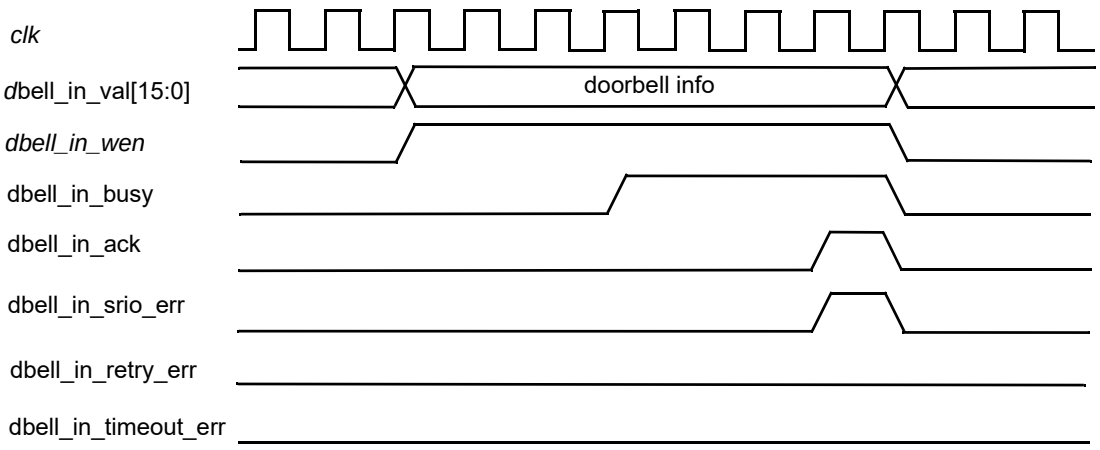


Figure 192. Skew and jitter timing waveforms

The doorbell info value must be provided on DBELL_IN_VAL and kept stable together with DBELL_IN_WEN asserted to 1 until the interface acknowledges the transmission by asserting DBELL_IN_ACK. In case of errors, DBELL_IN_SRIO_ERR, DBELL_IN_RETRY_ERR or DBELL_IN_TIMEOUT_ERR is asserted together with DBELL_IN_ACK (in the example above a SRIO error occurred during transmission, that is, an ERROR response has been received from the destination node).

65.6.2 Inbound doorbell messages

The following timing diagram illustrates how inbound doorbell messages are made available to the external interface (if this feature is enabled):

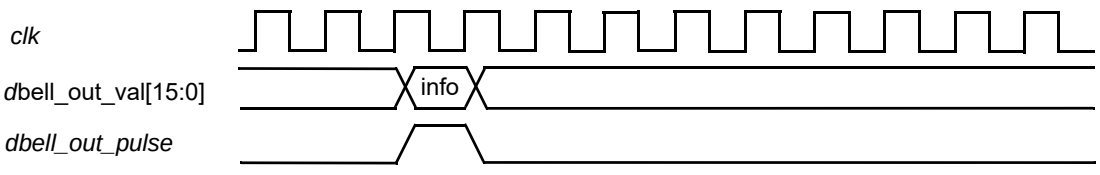


Figure 193. Skew and jitter timing waveforms

The doorbell info value is available at DBELL_OUT_VAL for one clock cycle when DBELL_OUT_-PULSE is asserted to 1. DBELL_OUT_PULSE can be used as a write enable signal to a register or memory that stores the doorbell info value for further processing.

65.7 Configuration options

Table 1227 shows the configuration options of the core (VHDL generics).

*Table 1227.*Configuration options

Generic	Function	Allowed values	Default
g_tech	Selects technology for RAM blocks.	0 - NTECH	DEFMEMTECH
g_use_async_rst	Use asynchronous instead of synchronous resets.	FALSE, TRUE	FALSE
g_data_width	See section 65.4 for details.	32 - 128	32
g_max_burst_length	See section 65.4 for details.	2 - 256	256
g_burst_chop_mask	See section 65.4 for details.	8 - 4096 (AXI) 8 - 1024 (AHB)	4096 (AXI) 1024 (AHB)
g_be_rd_pipe	See section 65.4 for details.	0-1	1
g_unalign_load_opt	See section 65.4 for details.	0-1	0
g_bm_info_print[1]	When it is set to a value apart from 0, prints out bus master configuration information during simulation.	-	1
g_axi_bm_id_width[1]	Determines the ID width for read address/data, write address, and write response channels.	-	5
g_axi_bm_addr_width[1]	Determines the address width for both front-end and back-end of the bus master.	32 - 64	32
g_no_dbell_rx	Number of doorbell reception queues.	1 - 32	4
g_no_dbell_tx[4]	Number of doorbell transmission queues[4]	1 - 32	4
g_no_msg_rx	Number of data message reception queues	1 - 32	4
g_no_hyb_tx[3]	Number of hybrid queues[3]	1-32	4
g_no_io_tx[4]	Number of IO memory access transmission queues[4]	1-32	4
g_no_msg_tx[4]	Number of data message transmission queues[4]	1 - 32	4
g_init_nodes	Number of data nodes initially available in SRIO end point.	0 - 255	72
g_init_crq	Number of CRQ entries initially available in SRIO end point.	0 - 255	64
g_wm_p0	Watermark for priority 0.	0 - 255	72

*Table 1227.*Configuration options

Generic	Function	Allowed values	Default
g_wm_p1	Watermark for priority 1.	0 - 255	63
g_wm_p2	Watermark for priority 2.	0 - 255	54
g_wm_p3	Watermark for priority 3.	0 - 255	45
g_wm_p4	Watermark for priority 4.	0 - 255	36
g_wm_p5	Watermark for priority 5.	0 - 255	27
g_wm_p6	Watermark for priority 6.	0 - 255	18
g_wm_p7	Watermark for priority 7.	0 - 255	9
g_8_in_win	Choose between 4 (false) and 8 inbound windows (true)	FALSE,TRUE	FALSE
g_mecs	Enable support for enhanced MECS (true)	FALSE,TRUE	FALSE
g_hyb_que	If set to “true” each TX queues can handle every kind of operations.	FALSE,TRUE	FALSE

[1] Only available in grsrio_gen2axi.vhd
[2] Only available in grsrio_gen2ahb.vhd
[3] Effective only when g_hyb_que is set to “true”
[4] Effective only when g_hyb_que is set to “false”

The core is configurate as 32 or 64-bit address according to the value of CFG_AW in grsrio_conf.vhd.

65.8 Signal Descriptions

Table 1228 shows the interface signals of the core (VHDL ports).

*Table 1228.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	AHB reset	Low
CLK	N/A	Input	AHB clock	-
SRIO_RSTN	N/A	Input	SRIO physical layer reset	Low
SRIO_CLK	N/A	Input	SRIO physical layer clock	-
APBO_PRDATA[31:0][2]	N/A	Output	APB slave: Read Data Bus	-
APBO_PIRQ[2]	N/A	Output	APB slave: Interrupt Output	High
APBI_PENABLE[2]	N/A	Input	APB slave: Strobe	High
APBI_PWRITE[2]	N/A	Input	APB slave: Transfer Direction	High
APBI_PADDR[31:0][2]	N/A	Input	APB slave: Address Bus	-
APBI_PWDATA[31:0][2]	N/A	Input	APB slave: Write Data Bus	-
APBI_PSEL[2]	N/A	Input	APB slave: Select	High
AHBMO_HBUSREQ[2]	N/A	Output	AHB master: Bus Request	High
AHBMO_HLOCK[2]	N/A	Output	AHB master: Locked Transfers	High
AHBMO_HTRANS[1:0][2]	N/A	Output	AHB master: Transfer Type	-
AHBMO_HADDR[31:0][2]	N/A	Output	AHB master: Address Bus	-
AHBMO_HWRITE[2]	N/A	Output	AHB master: Transfer Direction	High
AHBMO_HSIZE[2:0][2]	N/A	Output	AHB master: Transfer Size	-
AHBMO_HBURST[2:0][2]	N/A	Output	AHB master: Burst Type	-
AHBMO_HPROT[3:0][2]	N/A	Output	AHB master: Protection Control	-

*Table 1228.*Signal descriptions

Signal name	Field	Type	Function	Active
AHBMO_HWDATA [g_ahb_width-1:0][2]	N/A	Output	AHB master: Write Data Bus	-
AHBMI_HGRANT[2]	N/A	Input	AHB master: Bus Grant	High
AHBMI_HREADY[2]	N/A	Input	AHB master: Transfer Done	High
AHBMI_HRESP[1:0][2]	N/A	Input	AHB master: Transfer Response	-
AHBMI_HRDATA [g_ahb_width-1:0][2]	N/A	Input	AHB master: Read Data Bus	-
AXI_AW_ID [axi_bm_id_width-1:0][1]	N/A	Output	AXI4 master write address channel: Write Address ID	-
AXI_AW_ADDR [axi_bm_addr_width-1:0][1]	N/A	Output	AXI4 master write address channel: Write Address.	-
AXI_AW_LEN [7:0][1]	N/A	Output	AXI4 Master write address channel: Burst Length	-
AXI_AW_SIZE [2:0][1]	N/A	Output	AXI4 master write address channel: Burst Size	-
AXI_AW_BURST [1:0][1]	N/A	Output	AXI4 master write address channel: Burst Type	-
AXI_AW_LOCK [1:0][1]	N/A	Output	AXI4 master write address channel: Lock Type	-
AXI_AW_CACHE [3:0][1]	N/A	Output	AXI4 master write address channel: Memory type	-
AXI_AW_PROT [2:0][1]	N/A	Output	AXI4 master write address channel: Protection type	-
AXI_AW_VALID[1]	N/A	Output	AXI4 master write address channel: Write address valid	High
AXI_AW_QOS [3:0][1]	N/A	Output	AXI4 master write address channel: Quality of Service	-
AXI_AW_READY[1]	N/A	Input	AXI4 master write address channel: Write address ready.	High
AXI_W_DATA [be_dw-1:0][1]	N/A	Output	AXI4 write data channel signals: Write data.	-
AXI_W_STRB [log2(be_dw)-1:0][1]	N/A	Output	AXI4 write data channel signals: Write strobes	High
AXI_W_LAST[1]	N/A	Output	AXI4 write data channel signalsWrite last.	High
AXI_W_VALID[1]	N/A	Output	AXI4 write data channel signalsWrite valid.	High
AXI_B_READY[1]	N/A	Output	AXI4 write response channel signals: Response ready	High
AXI_B_ID [axi_bm_id_width-1 : 0][1]	N/A	Input	AXI4 write response channel signals: Response ID tag	-
AXI_B_RESP [1 downto 0][1]	N/A	Input	AXI4 write response channel signals: Write response	-
AXI_B_VALID[1]	N/A	Input	AXI4 write response channel signals: Write response valid	High
AXI_AR_ID [axi_bm_id_width-1:0][1]	N/A	Output	AXI4 read address channel signals: Read address ID	-
axi_ar_addr [axi_bm_addr_width-1:0][1]	N/A	Output	AXI4 read address channel signals: Read address	-

*Table 1228.*Signal descriptions

Signal name	Field	Type	Function	Active
AXI_AR_LEN [7:0][1]	N/A	Output	AXI4 read address channel signals: Burst length.	-
AXI_AR_SIZE [2:0][1]	N/A	Output	AXI4 read address channel signals: Burst size	-
AXI_AR_BURST [1:0][1]	N/A	Output	AXI4 read address channel signals: Burst type.	-
AXI_AR_LOCK [1:0][1]	N/A	Output	AXI4 read address channel signals: Lock type.	-
AXI_AR_CACHE [3:0][1]	N/A	Output	AXI4 read address channel signals: Memory type	-
AXI_AR_PROT [2:0][1]	N/A	Output	AXI4 read address channel signals: Protection type.	-
AXI_AR_VALID[1]	N/A	Output	AXI4 read address channel signals: Read address valid	High
AXI_AR_QOS[3:0][1]	N/A	Output	AXI4 read address channel signals: Quality of Service	-
AXI_AR_READY[1]	N/A	Input	AXI4 read address channel signals: Read address ready.	High
AXI_R_READY[1]	N/A	Output	AXI4 read address channel signals: Read ready.	High
AXI_R_ID [axi_bm_id_width-1:0][1]	N/A	Input	AXI4 read address channel signals: Read ID tag.	-
AXI_R_DATA [be_dw-1:0][1]	N/A	Input	AXI4 read address channel signals	-
AXI_R_RESP [1:0][1]	N/A	Input	AXI4 read address channel signals	-
AXI_R_LAST[1]	N/A	Input	AXI4 read address channel signals	High
AXI_R_VALID[1]	N/A	Input	AXI4 read address channel signals	High
TIMESTAMP[63:0]	N/A	Input	External time-stamp value, used to timestamp descriptors if g_mecs is set to false or MECS are not enabled.	-
DBELL_OUT_VAL[15:0]	N/A	Output	Doorbell info value of inbound message, valid when DBELL_OUT_PULSE is pulsed.	-
DBELL_OUT_PULSE	N/A	Output	Pulse signaling that outputted doorbell info value is valid.	High
DBELL_IN_VAL[15:0]	N/A	Input	Doorbell info value of outbound message. Must be kept stable until DBELL_IN_ACK goes high.	-
DBELL_IN_WEN	N/A	Input	Doorbell info write enable signal. Must be asserted together with DBELL_IN_VAL and kept asserted until DBELL_IN_ACK goes high.	High
DBELL_IN_BUSY	N/A	Output	Asserted while external outbound doorbell message is processed.	High
DBELL_IN_ACK	N/A	Output	Pulse acknowledging transmission of external outbound doorbell message.	High
DBELL_IN_SRIO_ERR	N/A	Output	Indicates a SRIO error during doorbell transmission. Valid together with DBELL_IN_ACK.	High
DBELL_IN_RETRY_ERR	N/A	Output	Indicates a retry error during doorbell transmission. Valid together with DBELL_IN_ACK.	High
DBELL_IN_TIMEOUT_ERR	N/A	Output	Indicates a timeout error during doorbell transmission. Valid together with DBELL_IN_ACK.	High
MECS_CAPTURED_IN[7:0]	N/A	Input	The SRIO end point signals to this IP core the reception of an extended MECS with cmd = i when the i-th signal changes	Edge
MECS_TRIGGER_OUT[7:0]	N/A	Output	Extended MECS with cmd = i are triggered in the endpoint when the ith signal changes	Edge

*Table 1228.*Signal descriptions

Signal name	Field	Type	Function	Active
SRIO_TX_DATA[127:0]	N/A	Output	Outbound UDI packet data bus	-
SRIO_TX_VALID	N/A	Output	When asserted, SRIO_TX_DATA is valid.	High
SRIO_TX_EOP	N/A	Output	When asserted, data SRIO_TX_DATA is the end of the packet.	High
SRIO_TX_HWORD[2:0]	N/A	Output	Indicates which half-words of SRIO_TX_DATA are valid.	-
SRIO_TX_HALT_ACK	N/A	Output	Two-way handshake to SRIO_TX_HALT.	High
SRIO_TX_CCOUNT[4:0]	N/A	Input	The value signals the number of data nodes that have been freed by the physical layer.	-
SRIO_TX_HALT	N/A	Input	When asserted, the GRSRIO IP core stops Egress traffic after finishing the current in-flight packet.	High
SRIO_RX_FULL	N/A	Output	Used by the GRSRIO IP core to pause the transfer of packets.	High
SRIO_RX_RELEASE[5:0]	N/A	Output	Indicates the number of ingress FIFO entries that have been freed by the GRSRIO IP core.	-
SRIO_RX_DATA[127:0]	N/A	Input	Inbound UDI packet data bus.	-
SRIO_RX_VALID	N/A	Input	When asserted, SRIO_RX_DATA is valid.	High
SRIO_RX_EOP	N/A	Input	When asserted, SRIO_RX_DATA is the end of the packet	High
SRIO_RX_HWORD[2:0]	N/A	Input	Indicates which half-words of SRIO_RX_DATA are valid.	-
SRIO_RX_STOMP	N/A	Input	Asserted together with SRIO_RX_EOP to flag a packet with CRC error (not supported by GRSRIO IP core)	High

[1] Only available in grsrio_gen2axi.vhd

[2] Only available in grsrio_gen2ahb.vhd

65.9 Clocks

The GRSRIO core operates in the CLK clock domain. Clock domain crossing between the CLK clock domain and the SRIO_CLK clock domain is accomplished by various CDC techniques.

The SRIO end point provides the signal SRIO_TX_CCOUNT[4:0] to the GRSRIO core, which is synchronous to and valid on every clock cycle of SRIO_CLK. Lost samples corrupt the flow control and must therefore be avoided. As a consequence, the AHB clock must be greater than or equal the SRIO clock. Lost samples are reported in CORECONF1.FE.

65.10 Resets

To ensure proper initialisation of synchronous logic related to the clock domain crossing between the SRIO_CLK and CLK clock domain, both the SRIO_RSTN and RSTN reset must be asserted for at least three clock cycles in the slower clock domain.

65.11 Library dependencies

Table 1229 shows libraries used when instantiating the core (VHDL libraries).

*Table 1229.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Types	AMBA signal type definitions

65.12 Component declaration

For the AXI4 wrapper:

```
component grsrio_gen2axi
  generic (
    g_tech             : integer;
    g_use_async_rst    : boolean;
    g_data_width       : integer range 32 to 128;
    g_max_burst_length : integer range 2 to 64;
    g_burst_chop_mask  : integer range 8 to 4096;
    g_be_rd_pipe       : integer range 0 to 1;
    g_unalign_load_opt : integer range 0 to 1;
    axi_bm_id_width    : integer;
    axi_bm_addr_width  : integer;
    g_bm_info_print    : integer;
    g_no_dbell_tx      : integer range 1 to 32;
    g_no_dbell_rx      : integer range 1 to 32;
    g_no_msg_tx        : integer range 1 to 32;
    g_no_msg_rx        : integer range 1 to 32;
    g_no_io_tx         : integer range 1 to 32;
    g_no_hyb_tx        : integer range 1 to 32;
    g_init_nodes       : integer range 0 to 255;
    g_init_crq         : integer range 0 to 255;
    g_wm_p0            : integer range 0 to 255;
    g_wm_p1            : integer range 0 to 255;
    g_wm_p2            : integer range 0 to 255;
    g_wm_p3            : integer range 0 to 255;
    g_wm_p4            : integer range 0 to 255;
    g_wm_p5            : integer range 0 to 255;
    g_wm_p6            : integer range 0 to 255;
    g_wm_p7            : integer range 0 to 255;
    g_8_in_win         : boolean;
    g_mecs             : boolean;
    g_hyb_que          : boolean;
    pindex             : integer range 0 to NAPBSLV-1;
    pirq               : integer range 0 to NAHBIRQ-1;
    paddr              : integer range 0 to 16#FFF#;
    pmask              : integer range 0 to 16#FFF#);
  port (
    clk                  : in  std_logic;
    clk_lock             : in  std_logic;
    rstn                 : in  std_logic;
    srio_clk             : in  std_logic;
    srio_rstn            : in  std_logic;
    soft_reset           : out std_logic;
    timestamp            : in  std_logic_vector(63 downto 0);
    dbell_out_val        : out std_logic_vector(15 downto 0);
    dbell_out_pulse      : out std_logic;
    dbell_in_val         : in  std_logic_vector(15 downto 0);
    dbell_in_wen         : in  std_logic;
    dbell_in_busy        : out std_logic;
    dbell_in_ack         : out std_logic;
    dbell_in_srio_err    : out std_logic;
```

```
dbell_in_retry_err   : out std_logic;
dbell_in_timeout_err : out std_logic;
apbo_prdata          : out std_logic_vector(31 downto 0);
apbo_pirq            : out std_logic;
apbo_pindex          : out integer range 0 to NAPBSLV -1;
apbo_pconfig         : out apb_config_type;
apbi_penable         : in  std_logic;
apbi_pwrite          : in  std_logic;
apbi_paddr           : in  std_logic_vector(31 downto 0);
apbi_pwdata          : in  std_logic_vector(31 downto 0);
apbi_psel            : in  std_logic;
axi_aw_id            : out std_logic_vector(axi_bm_id_width-1 downto 0);
axi_aw_addr          : out std_logic_vector(axi_bm_addr_width-1 downto 0);
axi_aw_len           : out std_logic_vector(7 downto 0);
axi_aw_size          : out std_logic_vector(2 downto 0);
axi_aw_burst         : out std_logic_vector(1 downto 0);
axi_aw_lock          : out std_logic;
axi_aw_cache         : out std_logic_vector(3 downto 0);
axi_aw_prot          : out std_logic_vector(2 downto 0);
axi_aw_valid         : out std_logic;
axi_aw_qos           : out std_logic_vector(3 downto 0);
axi_aw_ready         : in  std_logic;
axi_w_data           : out std_logic_vector(g_data_width-1 downto 0);
axi_w_strb           : out std_logic_vector((g_data_width/8)-1 downto 0);
axi_w_last           : out std_logic;
axi_w_valid          : out std_logic;
axi_w_ready          : in  std_logic;
axi_b_ready          : out std_logic;
axi_b_id             : in  std_logic_vector(axi_bm_id_width-1 downto 0);
axi_b_resp           : in  std_logic_vector(1 downto 0);
axi_b_valid          : in  std_logic;
axi_ar_id            : out std_logic_vector(axi_bm_id_width-1 downto 0);
axi_ar_addr          : out std_logic_vector(axi_bm_addr_width-1 downto 0);
axi_ar_len           : out std_logic_vector(7 downto 0);
axi_ar_size          : out std_logic_vector(2 downto 0);
axi_ar_burst         : out std_logic_vector(1 downto 0);
axi_ar_lock          : out std_logic;
axi_ar_cache         : out std_logic_vector(3 downto 0);
axi_ar_prot          : out std_logic_vector(2 downto 0);
axi_ar_valid         : out std_logic;
axi_ar_qos           : out std_logic_vector(3 downto 0);
axi_ar_ready         : in  std_logic;
axi_r_ready          : out std_logic;
axi_r_id             : in  std_logic_vector(axi_bm_id_width-1 downto 0);
axi_r_data           : in  std_logic_vector(g_data_width-1 downto 0);
axi_r_resp           : in  std_logic_vector(1 downto 0);
axi_r_last           : in  std_logic;
axi_r_valid          : in  std_logic;
srio_tx_data         : out std_logic_vector(127 downto 0);
srio_tx_eop          : out std_logic;
srio_tx_hword        : out std_logic_vector(2 downto 0);
srio_tx_valid        : out std_logic;
srio_tx_halt_ack     : out std_logic;
srio_tx_halt         : in  std_logic;
srio_tx_ccount       : in  std_logic_vector(4 downto 0);
srio_rx_full         : out std_logic;
srio_rx_release      : out std_logic_vector(5 downto 0);
srio_rx_data         : in  std_logic_vector(127 downto 0);
srio_rx_valid        : in  std_logic;
srio_rx_eop          : in  std_logic;
srio_rx_hword        : in  std_logic_vector(2 downto 0);
srio_rx_stomp        : in  std_logic;
send_mecs            : out std_logic_vector(7 downto 0);
received_mecs        : in  std_logic_vector(7 downto 0));
```

```
end component;
```

For the AHB wrapper:

```
component grsrio_gen2ahb
  generic (
    g_tech              : integer;
    g_use_async_rst     : boolean;
    g_data_width        : integer range 32 to 128;
    g_addr_width        : integer range 32 to 64;
    g_max_burst_length  : integer range 2 to 64;
    g_burst_chop_mask   : integer range 8 to 1024;
    g_be_rd_pipe        : integer range 0 to 1;
    g_unalign_load_opt  : integer range 0 to 1;
    g_no_dbell_tx       : integer range 1 to 32;
    g_no_dbell_rx       : integer range 1 to 32;
    g_no_msg_tx         : integer range 1 to 32;
    g_no_msg_rx         : integer range 1 to 32;
    g_no_io_tx          : integer range 1 to 32;
    g_no_hyb_tx         : integer range 1 to 32;
    g_init_nodes        : integer range 0 to 255;
    g_init_crq          : integer range 0 to 255;
    g_wm_p0             : integer range 0 to 255;
    g_wm_p1             : integer range 0 to 255;
    g_wm_p2             : integer range 0 to 255;
    g_wm_p3             : integer range 0 to 255;
    g_wm_p4             : integer range 0 to 255;
    g_wm_p5             : integer range 0 to 255;
    g_wm_p6             : integer range 0 to 255;
    g_wm_p7             : integer range 0 to 255;
    g_8_in_win          : boolean;
    g_mecs              : boolean;
    g_hyb_que           : boolean;
    pindex              : integer range 0 to NAPBSLV-1;
    pirq                : integer range 0 to NAHBIRQ-1;
    paddr               : integer range 0 to 16#FFF#;
    pmask               : integer range 0 to 16#FFF#);
  port (
    clk                   : in  std_logic;
    clk_lock              : in  std_logic;
    rstn                  : in  std_logic;
    srio_clk              : in  std_logic;
    srio_rstn             : in  std_logic;
    soft_reset            : out std_logic;
    timestamp             : in  std_logic_vector(63 downto 0);
    dbell_out_val         : out std_logic_vector(15 downto 0);
    dbell_out_pulse       : out std_logic;
    dbell_in_val          : in  std_logic_vector(15 downto 0);
    dbell_in_wen          : in  std_logic;
    dbell_in_busy         : out std_logic;
    dbell_in_ack          : out std_logic;
    dbell_in_srio_err     : out std_logic;
    dbell_in_retry_err    : out std_logic;
    dbell_in_timeout_err  : out std_logic;
    apbo_prdata           : out std_logic_vector(31 downto 0);
    apbo_pirq             : out std_logic;
    apbo_pindex           : out integer range 0 to NAPBSLV -1;
    apbo_pconfig          : out apb_config_type;
    apbi_penable          : in  std_logic;
    apbi_pwrite           : in  std_logic;
    apbi_paddr            : in  std_logic_vector(31 downto 0);
    apbi_pwdata           : in  std_logic_vector(31 downto 0);
    apbi_psel             : in  std_logic;
    ahbmo_hbusreq         : out std_logic;
```

```
    ahbmo_hlock          : out std_logic;
    ahbmo_htrans         : out std_logic_vector(1 downto 0);
    ahbmo_haddr          : out std_logic_vector(g_addr_width-1 downto 0);
    ahbmo_hwrite         : out std_logic;
    ahbmo_hsize          : out std_logic_vector(2 downto 0);
    ahbmo_hburst         : out std_logic_vector(2 downto 0);
    ahbmo_hprot          : out std_logic_vector(3 downto 0);
    ahbmo_hwdata         : out std_logic_vector(g_data_width-1 downto 0);
    ahbmi_hgrant         : in  std_logic;
    ahbmi_hready         : in  std_logic;
    ahbmi_hresp          : in  std_logic_vector(1 downto 0);
    ahbmi_hrdata         : in  std_logic_vector(g_data_width-1 downto 0);
    srio_tx_data         : out std_logic_vector(127 downto 0);
    srio_tx_eop          : out std_logic;
    srio_tx_hword        : out std_logic_vector(2 downto 0);
    srio_tx_valid        : out std_logic;
    srio_tx_halt_ack     : out std_logic;
    srio_tx_halt         : in  std_logic;
    srio_tx_ccount       : in  std_logic_vector(4 downto 0);
    srio_rx_full         : out std_logic;
    srio_rx_release      : out std_logic_vector(5 downto 0);
    srio_rx_data         : in  std_logic_vector(127 downto 0);
    srio_rx_valid        : in  std_logic;
    srio_rx_eop          : in  std_logic;
    srio_rx_hword        : in  std_logic_vector(2 downto 0);
    srio_rx_stomp        : in  std_logic;
    send_mecs            : out std_logic_vector(7 downto 0);
    received_mecs        : in  std_logic_vector(7 downto 0));
end component;
```

65.13 Instantiation

This example shows how the core can be instantiated.

```
library grlib;
use grlib.amba.all;

..

grsrio_gen2axi_1 : grsrio_gen2axi
    generic map (
      g_tech => CFG_MEMTECH,
      g_use_async_rst => false,
      g_data_width => 128,
      g_max_burst_length => 16,
      g_be_rd_pipe       => 0,
      g_unalign_load_opt => 1,
      axi_bm_id_width => 4,
      axi_bm_addr_width => 32,
      g_bm_info_print => 0,
      g_no_dbell_tx => 6,
      g_no_dbell_rx => 6,
      g_no_msg_tx => 6,
      g_no_msg_rx => 6,
      g_no_io_tx => 6,
      g_no_hyb_tx => 6,
      g_init_nodes => 72,
      g_init_crq => 64,
      g_wm_p0 => 72,
      g_wm_p1 => 63,
      g_wm_p2 => 54,
      g_wm_p3 => 45,
      g_wm_p4 => 36,
      g_wm_p5 => 27,
```

```
      g_wm_p6 => 18,
      g_wm_p7 => 9,
      g_8_in_win => true,
      g_mecs => true,
      g_hyb_que => true,
      pindex => 6,
      pirq => 6,
      paddr => 16#000#,
      pmask => 16#000#)
  port map (
    clk => clkm,
    clk_lock => lock,
    rstn => grsrio_rst,
    srio_clk => udi_clk,
    srio_rstn => udi_rst,
    soft_reset => soft_reset,
    timestamp => timestamp,
    dbell_out_val => dbell_out_val,
    dbell_out_pulse => dbell_out_pulse,
    dbell_in_val => dbell_in_val,
    dbell_in_wen => dbell_in_wen,
    dbell_in_busy => dbell_in_busy,
    dbell_in_ack => dbell_in_ack,
    dbell_in_srio_err => dbell_in_srio_err,
    dbell_in_retry_err => dbell_in_retry_err,
    dbell_in_timeout_err => dbell_in_timeout_err,
    apbo_prdata => apbo(6).prdata,
    apbo_pirq => apbo(6).pirq(6),
    apbo_pindex => apbo(6).pindex,
    apbo_pconfig => apbo(6).pconfig,
    apbi_penable => apbi.penable,
    apbi_pwrite => apbi.pwrite,
    apbi_paddr => apbi.paddr,
    apbi_pwdata => apbi.pwdata,
    apbi_psel => apbi.psel(6),
    axi_aw_id => grsrio_axi_awid,
    axi_aw_addr => grsrio_axi_awaddr,
    axi_aw_len => grsrio_axi_awlen,
    axi_aw_size => grsrio_axi_awsize,
    axi_aw_burst => grsrio_axi_awburst,
    axi_aw_lock => grsrio_axi_awlock,
    axi_aw_cache => grsrio_axi_awcache,
    axi_aw_prot => grsrio_axi_awprot,
    axi_aw_valid => grsrio_axi_awvalid,
    axi_aw_qos => grsrio_axi_awqos,
    axi_aw_ready => grsrio_axi_awready,
    axi_w_data => grsrio_axi_wdata,
    axi_w_strb => grsrio_axi_wstrb,
    axi_w_last => grsrio_axi_wlast,
    axi_w_valid => grsrio_axi_wvalid,
    axi_w_ready => grsrio_axi_wready,
    axi_b_ready => grsrio_axi_bready,
    axi_b_id => grsrio_axi_bid,
    axi_b_resp => grsrio_axi_bresp,
    axi_b_valid => grsrio_axi_bvalid,
    axi_ar_id => grsrio_axi_arid,
    axi_ar_addr => grsrio_axi_araddr,
    axi_ar_len => grsrio_axi_arlen,
    axi_ar_size => grsrio_axi_arsize,
    axi_ar_burst => grsrio_axi_arburst,
    axi_ar_lock => grsrio_axi_arlock,
    axi_ar_cache => grsrio_axi_arcache,
    axi_ar_prot => grsrio_axi_arprot,
    axi_ar_valid => grsrio_axi_arvalid,
```

```
axi_ar_qos => grsrio_axi_arqos,
axi_ar_ready => grsrio_axi_arready,
axi_r_ready => grsrio_axi_rready,
axi_r_id => grsrio_axi_rid,
axi_r_data => grsrio_axi_rdata,
axi_r_resp => grsrio_axi_rresp,
axi_r_last => grsrio_axi_rlast,
axi_r_valid => grsrio_axi_rvalid,
srio_tx_data => srio_tx_data,
srio_tx_eop => srio_tx_eop,
srio_tx_hword => srio_tx_hword,
srio_tx_valid => srio_tx_valid,
srio_tx_halt_ack => srio_tx_halt_ack,
srio_tx_halt => srio_tx_halt,
srio_tx_ccount => srio_tx_ccount,
srio_rx_full => srio_rx_full,
srio_rx_release => srio_rx_release,
srio_rx_data => srio_rx_data,
srio_rx_valid => srio_rx_valid,
srio_rx_eop => srio_rx_eop,
srio_rx_hword => srio_rx_hword,
srio_rx_stomp => srio_rx_stomp,
send_mecs => send_mecs,
received_mecs => received_mecs);
```

66 GRSYSMON - AMBA Wrapper for Xilinx System Monitor

66.1 Overview

The core provides an AMBA AHB interface to the Xilinx System Monitor present in Virtex-5 FPGAs. All Xilinx System Monitor registers are mapped into AMBA address space. The core also includes functionality for generating interrupts triggered by System Monitor outputs, and allows triggering of conversion start via a separate register interface.

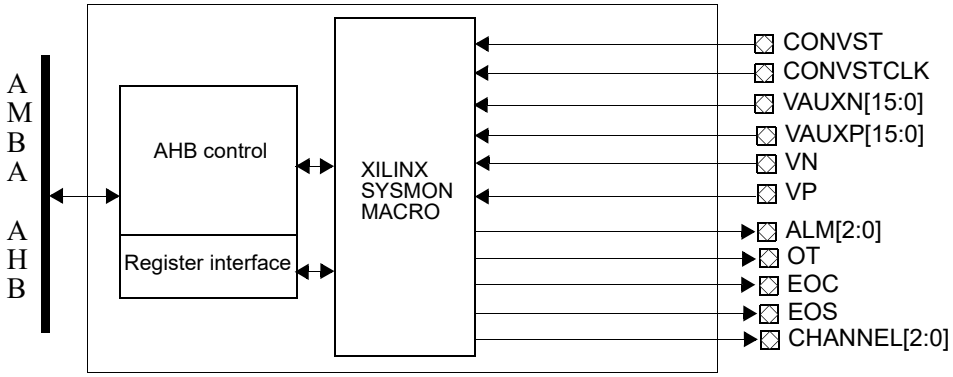


Figure 194. Block diagram

66.2 Operation

66.2.1 Operational model

The core has two I/O areas that can be accessed via the AMBA bus; the core configuration area and the System Monitor register area.

66.2.2 Configuration area

The configuration area, accessed via AHB I/O bank 0, contains two registers that provide status information and allow the user to generate interrupts from the Xilinx System Monitor's outputs. Write accesses to the configuration area have no AHB wait state and read accesses have one wait state. To ensure correct operation, only word (32-bit) sized accesses should be made to the configuration area.

66.2.3 System Monitor register area

The System Monitor register area is located in AHB I/O bank 1 and provides a direct-mapping to the System Monitor's Dynamic Reconfiguration Port. The System Monitor's first register is located at address offset 0x00000000 in this area.

Since the System Monitor documentation defines its addresses using half-word addressing, and AMBA uses byte-addressing, the addresses in the System Monitor documentation should be multiplied to get the correct offset in AMBA memory space. If the Configuration register bit WAL is '0' the address in System Monitor documentation should be multiplied by two to get the address mapped by the AMBA wrapper. A System Monitor register with address n is at AMBA offset 2*n. If the Configuration register bit WAL is '1', all registers start at a word boundary and the address in the System Monitor documentation should be multiplied by four to get the address mapped in AMBA address space. In this case, a System Monitor register with address n is at AMBA offset 4*n.

The wrapper always makes a single register access as the result of an access to the System Monitor register area. The size of the AMBA access is not checked and to ensure correct operation the mapped area should only be accessed using half-word (16-bit) accesses.

If the core has been implemented with AMBA split support, it will issue a SPLIT response to all accesses made to the mapped System Monitor registers. If the core is implemented without AMBA SPLIT support, wait states will be inserted until the System Monitor signals completion of a register access.

For a description of the System Monitor's capabilities and configuration, please refer to the Xilinx Virtex-5 FPGA System Monitor User Guide.

66.3 Registers

The core is programmed through registers mapped into AHB address space.

*Table 1230.*GRSYSMON registers

AHB address offset	Register
0x00	Configuration register
0x04	Status register

66.3.1 Configuration Register

*Table 1231.*0x00 - CONF - Configuration register

31	31 13	12	11 9	8 7	6	5	4	3	2	1	0
WAL	RESERVED	OT_IEN	ALM_IEN	RESERVED	CON-VST	EOS_ IEN	EOC_ IEN	BUSY_ IEN	JB_IEN	JL_IEN	JM_IEN
*	0	0	0	0	0	0	0	0	0	0	0
r	r	rw	rw	r	rw*	rw	rw	rw	rw	rw	rw

31 Word aligned registers (WAL) - If this bit is set to '1' each System Monitor memory mapped register start at a word boundary.

30 :13 RESERVED

12 Over temperature Interrupt Enable (OT_IEN) - If this bit is set to '1' the core will generate an interrupt when the corresponding bit in the Status register is set to '1'. This bit is automatically cleared after the interrupt has been generated.

11:9 Alarm Interrupt Enable (ALM_IEN) - If a bit in this field is set to '1' the core will generate an interrupt when the corresponding bit in the Status register is set to '1'. This bit is automatically cleared after the interrupt has been generated.

8:7 RESERVED

6 Conversion Start (CONVST) - If the core has been configured, at implementation, to use the an internal source for the Xilinx System Monitor CONVST signal, this bit can be written to '1' to generate a pulse on the System Monitor's CONVST input. This bit is automatically cleared after one clock cycle.

5 End of Sequence Interrupt Enable (EOS_IEN) - If this bit is set to '1' the core will generate an interrupt when the corresponding bit in the Status register is set to '1'. This bit is automatically cleared after the interrupt has been generated.

4 End of Conversion Interrupt Enable (EOC_IEN) - If this bit is set to '1' the core will generate an interrupt when the corresponding bit in the Status register is set to '1'. This bit is automatically cleared after the interrupt has been generated.

3 Busy Interrupt Enable (BUSY_IEN) - If this bit is set to '1' the core will generate an interrupt when the corresponding bit in the Status register is set to '1'. This bit is automatically cleared after the interrupt has been generated.

2 JTAG Busy Interrupt Enable (JB_IEN) - If this bit is set to '1' the core will generate an interrupt when the corresponding bit in the Status register is set to '1'. This bit is automatically cleared after the interrupt has been generated.

1 JTAG Locked Interrupt Enable (JL_IEN) - If this bit is set to '1' the core will generate an interrupt when the corresponding bit in the Status register is set to '1'. This bit is automatically cleared after the interrupt has been generated.

0 JTAG Modified Interrupt Enable (JM_IEN) - .If this bit is set to '1' the core will generate an interrupt when the corresponding bit in the Status register is set to '1'. This bit is automatically cleared after the interrupt has been generated.

Reset value: 0x00000000

66.3.2 Status Register

*Table 1232.*0x04 - STAT - Status register

31	30 13	12	11 9	8 6	5	4	3	2	1	0
WAL	RESERVED	OT	ALM	RESERVED	EOS	EOC	BUSY	JB	JL	JM
0	0	-	-	0	-	-	-	-	-	-
r	r	r	r	r	r	r	r	r	r	r

31 Word aligned registers (WAL) - If this bit is set to '1' each System Monitor memory mapped register start at a word boundary.

30 :13 RESERVED

12 Over Temperature (OT) - Connected to the System Monitor's Temperature Alarm output.

11:9 Alarm (ALM) - Connected to the System Monitor's alarm outputs.

8:6 RESERVED

*Table 1232.*0x04 - STAT - Status register

5	End of Sequence (EOS) - Connected to the System Monitor's End of Sequence output.
4	End of Conversion (EOC) - Connected to the System Monitors End of Conversion output.
3	Busy (BUSY) - Connected to the System Monitor's Busy output.
2	JTAG Busy (JB) - Connected to the System Monitor's JTAG Busy output.
1	JTAG Locked (JL) - Connected to the System Monitor's JTAG Locked output.
0	JTAG Modified (JM) - Connected to the System Monitor's JTAG Modified output.

Reset value: See Xilinx System Monitor documentation

66.4 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x066. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

66.5 Implementation

66.5.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

66.5.2 Technology mapping

The core instantiates a SYSMON primitive.

66.5.3 RAM usage

The core does not use any RAM components.

66.6 Configuration options

Table 1233 shows the configuration options of the core (VHDL generics).

*Table 1233.*Configuration options

Generic name	Function	Allowed range	Default
tech	Target technology	0 - NTECH	0
hindex	AHB slave index	0 - (NAHBSLV-1)	0
hirq	Interrupt line	0 - (NAHBIRQ-1)	0
caddr	ADDR field of the AHB BAR0 defining configuration register address space.	0 - 16#FFF#	16#000#
cmask	MASK field of the AHB BAR0 defining configuration register address space.	0 - 16#FFF#	16#FFF#
saddr	ADDR field of the AHB BAR1 defining System Monitor register address space.	0 - 16#FFF#	16#001#
smask	MASK field of the AHB BAR1 defining System Monitor register space.	0 - 16#FFF#	16#FFF#
split	If this generic is set to 1 the core will issue AMBA SPLIT responses when it is busy performing an operation with the System Monitor. Otherwise the core will insert wait states until the operation completes.	0 - 1	0

*Table 1233.*Configuration options

Generic name	Function	Allowed range	Default
extconvst	Connect CONVST input to System Monitor. If this generic is set to '0' the System Monitor's CONVST is controlled via the configuration register, otherwise the System Monitor CONVST input is taken from the core input signal.	0 - 1	0
wrdalign	Word align System Monitor registers. If this generic is set to 1 all System Monitor registers will begin on a word boundary. The first register will be mapped at offset 0x00, the second at 0x04. To translate a register access specified in the Xilinx System Monitor register documentation the register address should be multiplied by four to get the correct offset in AMBA address space. If this generic is set to 0, the register address should be multiplied by two to get the offset in AMBA address space.	0 - 1	0
INIT_40	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_41	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_42	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	16#0800#
INIT_43	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_44	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_45	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_46	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_47	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_48	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_49	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_4A	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_4B	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_4C	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_4D	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_4E	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_4F	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_50	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_51	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_52	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_53	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_54	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_55	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_56	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
INIT_57	Xilinx System Monitor register initialization value.	0 - 16#FFFF#	0
SIM_MONITOR_FILE	Simulation analog entry file. See Xilinx System Monitor documentation for a description of use and format.	-	"sysmon.txt"

66.7 Signal descriptions

Table 1234 shows the interface signals of the core (VHDL ports).

*Table 1234.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
AHBSI	*	Input	AHB slave input signals	-
AHBSO	*	Output	AHB slave output signals	-
SYSMONI	CONVST	Input	Convert start input, connected to Xilinx System Monitor if the *extconvst* VHDL generic is set to '1'.	High
	CONVSTCLK	Input	Convert start input, connected to Xilinx System Monitor.	High
	VAUXN[15:0]	Input	Auxiliary analog input, connected to Xilinx System Monitor.	-
	VAUXP[15:0]	Input	Auxiliary analog input, connected to Xilinx System Monitor.	-
	VN	Input	Dedicated analog-input, connected to Xilinx System Monitor.	-
	VP	Input	Dedicated analog-input, connected to Xilinx System Monitor.	-
SYSMONO	ALM[2:0]	Output	Alarm outputs, connected to Xilinx System Monitor.	High
	OT	Output	Over-Temperature alarm output, connected to Xilinx System Monitor.	High
	EOC	Output	End of Conversion, connected to Xilinx System Monitor.	High
	EOS	Output	End of Sequence, connected to Xilinx System Monitor.	High
	CHANNEL[4:0]	Output	Channel selection, connected to Xilinx System Monitor.	-

* see GRLIB IP Library User's Manual

66.8 Signal definitions and reset values

The signals and their reset values are described in table 1235.

*Table 1235.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
convst	Input	Convert start input, connected to Xilinx System Monitor if the *extconvst* VHDL generic is set to '1'.	Logical 1	-
convstclk	Input	Convert start input, connected to Xilinx System Monitor.	-	-
vauxn[15:0]	Input	Auxiliary analog input, connected to Xilinx System Monitor.	-	-
vauxp[15:0]	Input	Auxiliary analog input, connected to Xilinx System Monitor.	-	-
vn	Input	Dedicated analog-input, connected to Xilinx System Monitor.	-	-
vp	Input	Dedicated analog-input, connected to Xilinx System Monitor.	-	-
alm[2:0]	Output	Alarm outputs, connected to Xilinx System Monitor.	Logical 1	-
ot	Output	Over-Temperature alarm output, connected to Xilinx System Monitor.	Logical 1	-
eoc	Output	End of Conversion, connected to Xilinx System Monitor.	Logical 1	-
eos	Output	End of Sequence, connected to Xilinx System Monitor.	Logical 1	-
channel[4:0]	Output	Channel selection, connected to Xilinx System Monitor.	-	-

66.9 Library dependencies

Table 1236 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1236.*Library dependencies

Library	Package	Imported unit(s)	Description
GAISLER	MISC	Component, signals	Component and signal definitions
GRLIB	AMBA	Signals	AMBA signal definitions

66.10 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib, techmap;
use grlib.amba.all;
use techmap.gencomp.all;

library gaisler;
use gaisler.misc.all;

entity grsysmon_ex is
  port (
    clk       : in  std_ulogic;
    rstn      : in  std_ulogic
    );
end;
```

```
architecture rtl of grsysmon_ex is
  -- AMBA signals
  signal ahbsi  : ahb_slv_in_type;
  signal ahbso  : ahb_slv_out_vector := (others => ahbs_none);
  ...
  -- GRSYSMON signals
  signal sysmoni : grsysmon_in_type;
  signal sysmono : grsysmon_out_type;

begin

  -- AMBA Components are instantiated here
  ...

  -- GRSYSMON core is instantiated below
  sysm0 : grsysmon generic map (tech => virtex5, hindex => 4,
     hirq => 4, caddr => 16#002#, cmask => 16#fff#,
     saddr => 16#003#, smask => 16#fff#, split => 1, extconvst => 0)
    port map (rstn, clk, ahbsi, ahbso(4), sysmoni, sysmono);
  sysmoni <= grsysmon_in_gnd; -- Inputs are all driven to '0'

end;
```

67 GRUSBDC - USB Device controller

67.1 Overview

The Universal Serial Bus Device Controller provides a USB 2.0 function interface accessible from an AMBA-AHB bus interface. The core must be connected to the USB through an external PHY (shown in figure 235) compliant to either UTMI, UTMI+ or ULPI. Both full-speed and high-speed mode are supported.

Endpoints are controlled through a set of registers accessed through an AHB slave interface. Each of the up to 16 IN and 16 OUT endpoints can be individually configured to any of the four USB transfer types.

USB data cargo is moved to the core's internal buffers using a master or a slave data interface. The data slave interface allows access directly to the internal buffers using AHB transactions and therefore does not need external memory. This makes it suitable for slow and simple functions. The data master interface requires an additional AHB master interface through which data is transferred autonomously using descriptor based DMA. This is suitable for functions requiring large bandwidth.

These two interfaces are mutually exclusive and cannot be present in the same implementation of the core.

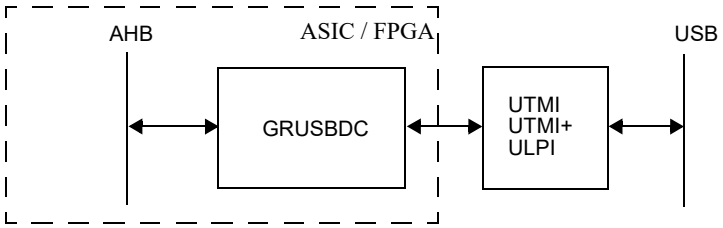


Figure 195. GRUSBDC connected to an external PHY device.

67.2 Operation

67.2.1 System overview

Figure 196 shows the internal structure of the core. This section briefly describes the function of the different blocks.

The Speed Negotiation Engine (SNE) detects connection by monitoring the VBUS signal on the USB connector. When a steady 5 V voltage is detected the SNE waits for a reset and then starts the High-speed negotiation. When the Speed negotiation and reset procedure is finished the selected speed mode (full-speed or high-speed) is notified to the Serial Interface Engine (SIE) which now can start operation. The SNE also detects and handles suspend and resume operations.

The SIE is enabled when the SNE notifies that the reset procedure has finished. It then waits for packets to arrive and processes them according to the USB 2.0 specification. The data cargo is stored to an internal buffer belonging to the recipient endpoint.

The AHB Interface Engine AIE is responsible for transferring USB data cargo from the endpoint's internal buffers to the AHB bus using descriptor based DMA through an AHB master interface when configured in master mode or by direct accesses to the AHB slave interface when configured in slave mode.

For received data it is then up to the external (to the device controller) function to continue processing of the USB data cargo after it has been transferred on the AHB bus. The function is the application specific core which determines the functionality of the complete USB device. It sets up endpoints in the device controller and notifies their existence through the appropriate USB descriptors. When the function wants to transmit a packet it either uses the slave interface to write to the endpoint buffers or establishes a DMA transfer.

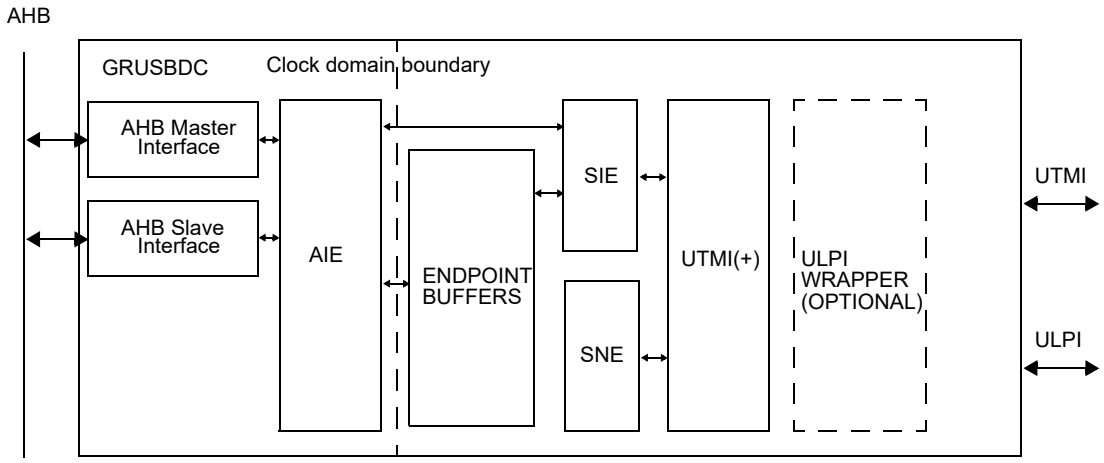


Figure 196. Block diagram of the internal structure of the core.

67.2.2 PHY interface

The core supports three different interfaces to the external PHY which is used to connect to the USB bus. The supported interfaces are UTMI, UTMI+ and ULPI. UTMI+ is an extension of the UTMI specification with optional additional support for host controllers and on-the-go devices while UTMI only supports devices. There are different so called levels in the UTMI+ specification, each with an added degree of support for hosts and on-the-go. The lowest level and common denominator for all the levels is identical to UTMI and uses the exact same signals. The core only supports devices and thus the support for UTMI+ refers to level 0. The data path to the UTMI/UTMI+ cores can be 8-bits or 16-bits wide and also uni- or bi-directional. All combinations are supported by the core.

The UTMI+ Low Pin Interface (ULPI) specifies a generic reduced pin interface and how it can be used to wrap a UTMI+ interface. The core has UTMI/UTMI+ as the main interface (they are identical) and when ULPI is used an extra conversion layer is added. When ULPI is enabled, the UTMI layer is always in 8-bit mode since this is what is required by the ULPI specification.

67.2.3 Speed Negotiation Engine (SNE)

The SNE detects attach, handles reset, high-speed handshake and suspend/resume operation. It also contains support for the various test-modes, which all USB device have to support.

The attached state is entered when a valid VBUS signal is detected. After this the core waits for a USB reset and then starts the high-speed handshake which determines whether full-speed or high-speed mode should be entered. No bus traffic will be accepted by the core until a valid reset has been detected.

The core supports soft connect/disconnect which means that the pull-up on the D+ line can be controlled from a user accessible register. The pull-up is disabled after reset and thus the function implementation has full control over when the device will be visible to the host.

The SNE also continuously monitors for the suspend condition (3 ms of idle on the USB bus) when the suspend state will be entered. The suspend state is left either through an USB reset or resume signaling. The resume signaling can come from either a downstream facing port (hub or host controller) or the device itself (Remote wakeup). The device controller core can generate remote wakeup signaling which is activated through an user accessible register. If this feature is used the function should indicate this in the descriptor returned to a device GetStatus request.

Transactions are only handled by the SIE if the SNE is in full-speed or high-speed mode. When in suspend, notattached, attached or during the reset process all transactions will be dropped.

The current status of the SNE such as VBUS valid, suspend active, USB reset received and current speed mode can be accessed through a status register. Each of these status bits have a corresponding interrupt enable bit which can be used to generate interrupts when a change occurs in the status bits.

If full-speed only mode is desired the core can be set to not perform the high-speed handshake through a register.

The different test-modes required by the USB standard are also enabled through user accessible registers. When enabled they can only be left by power-cycling the complete core or resetting the device controller (by using the rst signal to the core, not an USB reset).

The test modes are Test_SE0_NAK, Test_J, Test_K and Test_Packet.

In Test_SE0_NAK mode the high-speed receiver is enabled and only valid IN transactions (CRC correct, device and endpoint addresses match, PID is not corrupt) are responded to with a NAK.

Test_J continuously drives a high-speed J state.

Test_K continuously drives a high-speed K state.

Test_Packet repetitively sends a test packet. Please refer to the USB 2.0 standard for the packet contents. Minimum interpacket delay when device is sending two or more consecutive packets seems not to be specified in the standard. The core uses 192 bit times as its minimum delay which is the maximum value of the various minimum delays in the standard for any packet sequence and should therefore be compliant.

The core also supports a functional test-mode where all timeouts in the speed-negotiation engine have been shortened to eight clock cycles. This intended to be used in simulations and for ASIC testers where time and test-vector length respectively are important.

67.2.4 Serial Interface Engine (SIE)

The SIE handles transmission and reception of USB packets. The core will not respond to any transactions until a reset has been received and either full-speed or high-speed mode has been successfully entered.

The SIE always begins with waiting for a token packet. Depending on the type of token, data is either transferred from the core to the host or in the opposite direction. Special tokens are handled without any data transfers. The special tokens are PING and SOF which cause only a handshake to be sent or the frame number to be stored respectively. IN tokens initiate transfers to the host while SETUP and OUT tokens initiate transfers to the device. Packets received in the token stage with other PIDs than those mentioned in this paragraph are discarded.

A data packet is transmitted in the next stage if the token determined that data should be transferred to the host. When the data transmission is finished the core waits for a handshake before returning to the token stage.

If data was determined to be transferred to the device the core waits for and receives a data packet and then sends a handshake in return before entering the token stage again.

More detailed descriptions of the SIE and how it interacts with the core function are found in section 67.5.

67.2.5 Endpoint buffers

Each endpoint has two buffers to which packets are stored. The core automatically alternates between them when a packet has been received/transmitted so that data from one of the buffers can be transferred on the AHB bus while a new packet is being received/transmitted on the USB to/from the second buffer.

The state of the buffers affects the handshake sent to the host at the end of a transaction. In high-speed mode BULK OUT endpoints and CONTROL OUT endpoints which are not in the SETUP stage support the PING protocol. This means that at the end of an OUT transaction to one of these endpoints the device should return ACK if it could accept the current data and has space for another packet. For the USB device controller this is done if the second buffer for the endpoint is empty when the transaction is ready.

If the second buffer is non-empty a NYET is sent instead. If the current data could not be accepted (both buffers non-empty when the packet arrives) a NAK is returned.

For other endpoint types in high-speed mode and all endpoint types in full-speed mode an ACK is always returned if the data is accepted and a NAK if it could not be accepted.

An endpoint buffer can be configured to be larger than the maximum payload for that endpoint. For IN endpoints the writing of data larger than the maximum payload size to a buffer will result in a number of maximum sized packets being transferred ending with a packet smaller than or equal to the maximum size.

In the OUT direction larger buffers are only used for high-bandwidth endpoints where more than one transaction per microframe can occur for that endpoint. In that case the data from all packets during one microframe is stored in the order it arrives to a single buffer and is then handed over to the AHB interface. All non-high-bandwidth endpoints always store one packet data cargo to a buffer.

The endpoint buffers do not use separate physical RAM blocks in hardware instead they reside consecutively in the same memory space to avoid wasting memory.

67.2.6 AMBA Interface Engine (AIE)

The AIE can either be configured in slave mode or master mode. This is selected in synthesis process with a VHDL generic. Both cannot be present at the same time. The two interfaces will be described separately in this section.

Master interface

In master mode an AHB master interface is included in the core and handles all data transfers to and from the cores internal buffers using DMA operations. The DMA operation is described in detail in section 67.3. There is a separate DMA engine in the IN direction and the OUT direction respectively. They are multiplexed on the single master interface available for the core on the AHB bus. This scheme is used to limit the load on the AHB bus.

If both engines request the bus at the same time the owner will always be switched. That is, if the OUT direction DMA engine currently was allowed to make an access and when finished it still requests the bus for a new transaction and at the same time the IN direction engine also requests the bus, the IN direction will be granted access. If the situation is the same after the next access ownership will be switched back to the OUT engine etc.

The IN engine only reads data (note that this only applies to DATA, descriptor status is written) from the bus and always performs word transfers. Any byte alignment and length can still be used since this will only cause the core to skip the appropriate amount of leading and trailing bytes from the first and last words read.

The OUT engine writes data to the bus and performs both word and byte transfers. If the start transfer for an access is not word-aligned byte writes will be performed until a word boundary is reached. From then and onwards word writes are performed in burst mode until less than 4 bytes are left. If remaining number of bytes is not zero byte writes are performed for the last accesses. The byte accesses are always done as single accesses.

The bursts are of type incremental burst of unspecified length (refer to AMBA specification for more details). The core can only operate in big-endian mode that is the byte at the lowest address in a word is the most significant byte. This corresponds to bits 31 downto 24 in the GRLIB implementation. The

first byte received on the USB will be stored to the msb location. In a single byte the lowest bit index corresponds to the first bit transmitted on the USB.

Slave interface

The slave interface is used for accessing registers and also for data transfers when the core is configured in slave mode. Byte, half-word and word accesses are supported. At least one waitstate is always inserted due to the pipelined nature of the interface but the upper limit is not fixed due to registers being accessed across clock domains. The maximum number of waitstates will thus depend on the difference in clock frequency between the USB and AHB clock domains. An upper bound can be calculated when the clock frequencies have been determined.

67.2.7 Synchronization

There are two clock domains in the core: the AHB clock domain and the USB clock domain. The AHB clock domain runs on the same clock as the AHB bus while the USB domain runs on the UTMI or ULPI clock. The boundary is between then AIE, SIE and Endpoint buffers. All signals between the two domains are synchronized and should be declared as false paths during synthesis.

67.2.8 Reset generation

The main reset (AMBA reset) resets AHB domain registers, whereas the USB reset resets registers in USB clock domain. There is no internal reset generation or synchronization between both AMBA and USB resets, they are independent inputs. If necessary, the reset generation shall be done in a higher instance, externally to this IP.

Endpoint specific registers related to the state of the USB protocol in the SIE are reset when an USB reset is received.

67.2.9 Synthesis

All number of endpoints with up to maximum size payloads cannot be supported due to limitations in the RAM block generator size in GRLIB. The maximum size also varies with technology. Note that large buffers can also have a large timing impact at least on FPGA since the a large RAM buffer will consist of several separate physical block RAMs located at different places causing large routing delays.

As mentioned in section 67.2.7, signals between the clock domains are synchronized and should be declared as false paths.

The complete AHB domain runs at the same frequency as the AHB bus and will be completely constrained by the bus frequency requirement.

The USB domain runs on different frequencies depending on the data path width. In 8-bit mode the frequency is 60 MHz and in 16-bit mode it is 30 MHz. Input and output constraints also need to be applied to the signals to and from the PHY. Please refer to the PHY documentation and/or UTMI/ULPI specification for the exact values of the I/O constraints.

67.2.10 Functional test-mode

A functional test-mode can be enabled in the core using the functesten VHDL generic. The functional test-mode is intended to reduce the number of required test-vectors during functional testing of an ASIC chip. During normal operation it would be required to go through the whole speed detection sequence before being able to start USB transactions. Since the speed detection takes a relatively long time this would make the test-vector amount very large often making it incompatible with existing test equipment.

In functional test-mode the core shortens the speed detection thus making it possible to test the functionality without a long initial delay. The test-mode can be disabled using the FT control register bit.

67.2.11 Scan test support

The VHDL generic *scantest* enables scan test support. If the core has been implemented with scan test support it will:

- disable the internal RAM blocks when the testen and scanen signals are asserted.
- use the testoen signal as output enable signal.
- use the testrst signal as the reset signal for those registers that are asynchronously reseted.

The testen, scanen, testrst, and testoen signals are routed via the AHB slave interface.

67.3 DMA operation

DMA operation is used when the core is configured in AHB master mode. Each IN and each OUT endpoint has a dedicated DMA channel which transfers data to and from the endpoint's internal buffers using descriptor based autonomous DMA. Each direction (IN and OUT) has its own DMA engine which requests the AHB master interface in contention with the other direction. Also each endpoint in a direction contends for the usage of the DMA engine with the other endpoints in the same direction. The arbitration is done in a round-robin fashion for all endpoints which are enabled and have data to send or receive.

The operation is nearly identical in both directions and the common properties will be explained here while the differences are outlined in the two following sub-sections.

The DMA operation is based on a linked list of descriptors located in memory. Each endpoint has its own linked list. The first word in a descriptor is the control word which contains an enable bit that determines whether the descriptor is active or not and other control bits. The following word is a pointer to a memory buffer where data should be written to or read from for this descriptor. The last word is a pointer to the location of the next descriptor. A bit in the control word determines if the next descriptor pointer is valid or not. If not valid the descriptor fetching stops after the current descriptor is processed and the DMA channel is disabled.

The DMA operation is started by first setting up a list with descriptors in memory and then writing a pointer to the first descriptor to the endpoint's descriptor pointer register in the core and setting the descriptor available bit. The pointer register is updated as the list is traversed and can be read through the AHB slave interface. When the list is ended with a descriptor that has its next descriptor available bit disabled the list must not be touched until the core has finished processing the list and the channel is disabled. Otherwise a deadlock situation might occur and behavior is undefined.

Another way to use the linked list is to always set the next descriptor available bit and instead make sure that the last descriptor is disabled. This way new descriptors can be added and enabled on the fly to the end of the list as long as the descriptor available bit is always set after the new descriptors have

been written to memory. This ensures that no dead lock will occur and that no descriptors are missed. Figure 197 shows the structure of the descriptor linked list.

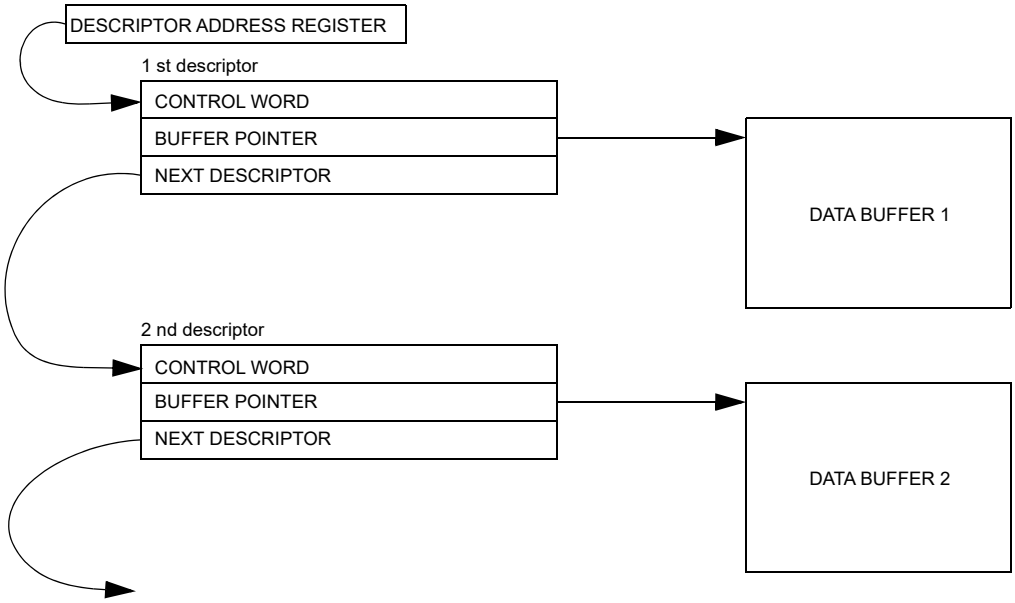


Figure 197. Example of the structure of a DMA descriptor linked list in memory.

67.3.1 OUT endpoints

The DMA operation for OUT endpoints conforms to the general description in the previous subsection. There are small differences in individual bits and the meaning of the length field. The contents of the different descriptor words can be found in the tables below.

When a descriptor has been enabled it will be fetched by the core when the descriptor available bit is set and as soon as a buffer for the corresponding endpoint contains data received from the USB it will be written to memory starting from the address specified in the buffer pointer word of the descriptor. The contents of a single internal memory buffer is always written to a single descriptor buffer. This always corresponds to a single USB packet except for high-bandwidth isochronous and interrupt endpoints. The number of bytes written is stored in the length field when writing is finished which is indicated by the enable bit being cleared. Then the SETUP status bit will also be valid. When the enable bit is cleared the memory location can be used again.

Interrupts are generated if requested as soon as the writing to memory is finished. The endpoint can also be configured to generate an interrupt immediately when a packet has been received to the internal buffers. This can not be enabled per packet since the core cannot associate a received packet with a specific descriptor in advance. This interrupt is enabled from the endpoint’s control register.

When the data has been fetched from the internal buffer it is cleared and can be used by the SIE again for receiving a new packet.

*Table 1237.*OUT descriptor word 0 (address offset 0x0) ctrl word

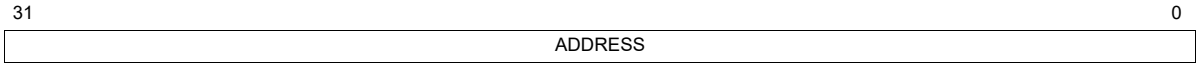
31	18	17	16	15	14	13	12	0
RESERVED		SE	RE	IE	NX	EN	LENGTH	

31: 18	RESERVED
17	Setup packet (SE) - The data was received from a SETUP packet instead of an OUT.
16	RESERVED

*Table 1237.*OUT descriptor word 0 (address offset 0x0) ctrl word

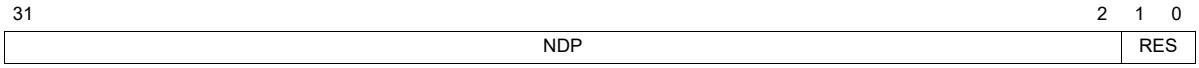
15	Interrupt Enable (IE) - Enable Interrupts. An interrupt will be generated when the packet from this descriptor has been read to the internal buffers and handed over to the SIE. This does not mean that packet has also been transmitted.
14	Next descriptor available (NX) - The next descriptor field is valid and points to the next descriptor.
13	Enable (EN) - Set to one to enable the descriptor. Should always be set last of all the descriptor fields.
12: 0	LENGTH - The number of bytes received. Valid when the EN bit has been cleared by the core.

*Table 1238.*OUT descriptor word 1 (address offset 0x4) Buffer pointer



31: 2	Address (ADDRESS) - Pointer to the buffer area from where the packet data will be loaded.
1: 0	RESERVED

*Table 1239.*OUT descriptor word 2 (address offset 0x8) Next descriptor pointer



31: 2	Next descriptor pointer (NDP) - Pointer to the next descriptor.
1: 0	RESERVED

67.3.2 IN endpoints

The DMA operation for IN endpoints conforms to the general DMA description. There are small differences in individual bits and the meaning of the length field. The contents of the different descriptor words can be found in the tables below.

When a descriptor has been enabled and the descriptor available bit is set the core will start processing the descriptor and fetch the number of bytes indicated in the length field to an internal buffer belonging to the endpoint as soon as one is available. An interrupt will be generated if requested when data has been written to the internal buffer and status has been written back to the descriptor. The packet might not have been transmitted on the USB yet.

A separate interrupt is available which is generated when the packet has actually been transmitted. It needs to be enabled from the endpoint's control register and also in the descriptor (using the PI bit) for each packet that should generate the interrupt.

A descriptor with length zero will result in a packet with length zero being transmitted while a length larger than the maximum payload for the endpoint will result in two or more packets with all but the last being of maximum payload in length. The last transaction can be less than or equal to the maximum payload. If the length field is larger than the internal buffer size the data will not written to the internal buffer and status will be immediately written to the descriptor with an error bit set.

When the more bit is set the data from the current descriptor is written to the internal buffer and it then continues to the next descriptor without enabling the buffer for transmission. The next descriptor's data is also read to the same buffer and this continues until a descriptor is encountered which does not have more set.

If the total byte count becomes larger than the internal buffer size the packet is not sent (the data from the internal buffer is dropped) and the ML bit is set for the last descriptor. Then the descriptor fetching starts over again.

If the next bit is not set when the more bit is, the core will wait for a descriptor to be enabled without letting other endpoints access the AHB bus in between.

*Table 1240.*IN descriptor word 0 (address offset 0x0) ctrl word

31	19	18	17	16	15	14	13	12	0
RESERVED		MO	PI	ML	IE	NX	EN		LENGTH

31: 19	RESERVED
18	More (MO) - The data from the next descriptor should be read to the same buffer.
17	Packet sent interrupt (PI) - Generate an interrupt when packet has been transmitted on the USB.
16	Maximum length violation (ML) - Attempted to transmit a data cargo amount larger than the buffer.
15	Interrupt Enable (IE) - Enable Interrupts. An interrupt will be generated when the packet from this descriptor has been read to the internal buffers and handed over to the SIE. This does not mean that packet has also been transmitted.
14	Next descriptor available (NX) - The next descriptor field is valid and points to the next descriptor.
13	Enable (EN) - Set to one to enable the descriptor. Should always be set last of all the descriptor fields.
12: 0	LENGTH - The number of bytes to be transmitted.

*Table 1241.*IN descriptor word 1 (address offset 0x4) Buffer pointer

31	0
ADDRESS	

31: 2	Address (ADDRESS) - Pointer to the buffer area from where the packet data will be loaded.
1: 0	RESERVED

*Table 1242.*IN descriptor word 2 (address offset 0x8) Next descriptor pointer

31	2	1	0
NDP		RES	

31: 2	Next descriptor pointer (NDP) - Pointer to the next descriptor.
1: 0	RESERVED

67.4 Slave data transfer interface operation

The AHB slave interface is used for data transfers instead of the DMA interface when the core is configured in AHB slave mode. This mode is selected by setting the aiface VHDL generic to 0. In this mode the core's internal buffers containing data to/from USB packets are accessed directly using AHB read and write transfers. This is usually much slower than DMA but much simpler and does not require any external memory, thus suitable for slow devices which need to be small and simple.

As for the DMA mode each endpoint is operated separately using four registers at the same addresses. Two of them, the control and status registers, are the same while the DMA control and the descriptor address registers have been replaced with the slave control and slave write/read data registers. The slave interface does not use descriptors so these four registers provides the complete control of the endpoint.

The details for data transfers in the two different endpoint directions will be explained in separate sections.

67.4.1 OUT slave endpoint

As stated earlier, in slave mode the core's buffers are accessed directly from the AHB bus through the slave interface. For OUT endpoints it has to be checked that data is available in the selected buffer and then reserve it. This is done using the slave control register by writing a one to the CB bit. The CB bit is always automatically cleared when the write access is finished and then the BS, DA and BUFCNT

read-only bits/fields contain valid information. The BS bit is set to 0 if buffer 0 is currently selected and to 1 if buffer 1 is selected. DA is set to 1 if data is available in the buffer and in that case BUFCNT contains the number of bytes.

If data is available (DA is 1) it can be read from the slave data read register. One byte at a time is read using byte accesses, two bytes using half-word accesses and four bytes using word accesses. No other widths are supported. In each case data is available from bit 31 and downwards regardless of the value of the two least significant address bits. This is summarized in table 1243. The BUFCNT field is continuously updated when reading the buffer so that it can be monitored how many bytes are left.

*Table 1243.*AHB slave interface data transfer sizes

Size (byte)	AHB transfer size (HSIZE)	Data alignment (HRDATA)
1	byte (000)	31:24
2	half-word (001)	31:16
4	word (010)	31:0

When all the data has been read, a new buffer can be acquired by writing a one to CB. In this case when a buffer is currently reserved and the DA bit is set it will be released when CB is written. If a new buffer was available it will be reserved and DA is set to 1 again. If no new buffer is available DA will be 0 and the process has to be repeated. The current buffer (if one is selected) will be released regardless of whether a new one is available or not. Also, if all data has not been read yet when a buffer change request is issued the rest of the data will be lost.

The core does not have to be polled to determine whether a packet is available. A packet received interrupt is available which can be enabled from the control register and when set an interrupt will be generated each time a packet is stored to the internal buffers. The status of the buffers can also be read through the endpoint's status register without actually reserving the buffer.

One buffer consists of the data payload from one single packet except for high-bandwidth interrupt and isochronous endpoints for which up to three packet data payloads can reside in a single buffer.

A buffer does not have to be read consecutively. Buffers for several endpoints can be acquired simultaneously and read interleaved with each other.

67.4.2 IN slave endpoint

The slave operation of IN endpoints is mostly identical to that for OUT. For IN endpoints it has to be checked that a buffer is free and then reserve it before writing data to it. This is done using the slave control register by writing a one to the EB bit. The EB bit is always automatically cleared when the write access is finished and then the BS, BA and BUFCNT fields are updated. The BS bit is set to 0 if buffer 0 is currently selected and to 1 if buffer 1 is selected. BA is set to 1 if a buffer is available to write data to. BUFCNT contains the number of bytes currently written to the selected buffer. It is cleared to zero when a new buffer is acquired.

If a buffer is available (BA is 1) data can be written through the slave data write register. One byte at a time is written using byte accesses, two bytes using half-word accesses and four bytes using word accesses. No other widths are supported. In each case data should be placed from bit 31 and downwards regardless of the value of the two least significant address bits. This is summarized in table 1244.

*Table 1244.*AHB slave interface data transfer sizes

Size (byte)	AHB transfer size (HSIZE)	Data alignment (HWDATA)
1	byte (000)	31:24
2	half-word (001)	31:16
4	word (010)	31:0

When all the data has been written, the buffer is enabled for transmission by writing a one to EB. If a new buffer was available it will be reserved and BA is set to 1 again. If no new buffer is available BA will be 0 and the process has to be repeated. The current buffer (if one is reserved) will be enabled for transmission regardless of whether a new one is available or not.

The core does not have to be polled to determine whether a buffer is available. A packet transmitted interrupt is available which can be enabled from the endpoint control register. Then when enabling a packet for transmission the PI bit in the slave control register can be set which will be cause an interrupt to be generated when this packet has been transmitted and cleared from the internal buffers. The status of the buffers can also be read through the endpoint's status register without actually reserving the buffer.

Maximum payload size packets will be generated from the buffer until the last packet which will contain the remaining bytes.

A buffer does not have to be written consecutively. Buffers for several endpoints can be acquired simultaneously and written interleaved with each other. This will however cause additional waitstates to be inserted.

67.5 Endpoints

An endpoint needs to have both its AHB and USB function configured before usage. The AHB configuration comprises the DMA operation described in the previous section. The USB configuration comprises enabling the endpoint for USB transactions, setting up transfer type (control, bulk, isochronous, interrupt), payload size, high-bandwidth among others. The configuration options are accessed through a register available from the AHB slave interface. See section 67.8 for the complete set of options.

When setting the configuration options the endpoint valid bit should be set. This will enable transfers to this endpoint as soon as a USB reset has been received. If the endpoint is reconfigured the valid bit must first be set to zero before enabling it again. Otherwise the endpoint will not be correctly initialized. When the endpoint is enabled the toggle scheme will be reset and data buffers cleared and buffer selectors set to buffer zero. The maximum payload, number of additional transactions and transfer type fields may only be changed when endpoint valid is zero or when setting endpoint valid to one again after being disabled. Other bits in the endpoint control register can be changed at any time.

No configuration options should be changed when the endpoint is enabled except the halt, control halt and disable bits.

An endpoint can also be halted by setting the halt bit of the endpoint. This will cause all transactions to receive a STALL handshake. When clearing the halt condition the toggle scheme will also be reset as required by the USB standard.

When the endpoint is setup, data transfers from and to the endpoint can take place. There is no difference in how data is transferred on the AHB bus depending on the selected transfer type. This only affects the transfers on the USB. For control endpoints some extra handling is required by the core user during error conditions which will be explained in the control endpoint section.

Packets that are received to an endpoint (independent of endpoint type) with a larger payload than the configured maximum value for the endpoint will receive a STALL handshake and cause the endpoint to enter halt mode.

When a USB reset is detected the CS, ED and EH bits of the endpoint control register will be cleared for all endpoints. The EV bit will also be cleared except for control endpoint 0.

The CB bit in the endpoint control register is for clearing the internal buffers of an endpoint. When set the data will be discarded from the buffers, the data available bits for the corresponding buffers will be cleared and the CB bit is cleared when it is done. This will however not work if a transaction is currently active to the same endpoint so this feature must be used with caution.

67.5.1 Control endpoints

Endpoint 0 must always be a control endpoint according to the USB standard and be accessible as soon as a USB reset is received. The core does not accept any transactions until a USB reset has been received so this endpoint can be enabled directly after power up. More control endpoints can be enabled as needed with the same constraints as the default control endpoint except that they should not be accessible until after configuration. If the function controlling the core is slow during startup it might not be able complete configuration of endpoint 0 before a USB reset is received. This problem is avoided in the core because its pull-up on D+ is disabled after reset which gives the function full control of when the device will be visible on the bus.

A control endpoint is a message pipe and therefore transfers data both in the IN and OUT direction. Thus control endpoints must use the endpoint in both directions with the same number in the device controller. This requires both to be configured in the same mode (same transfer type, payload ...). Otherwise device behavior is undefined.

A control transfer is always started with a SETUP transaction which will be received to the OUT endpoint. If the control transfer is a write the subsequent data phase will be in the OUT direction and this data will also be received to the OUT endpoint. The function should read both the setup data and the other data cargo and respond correspondingly. If the request was valid the function should enable a zero length packet for the endpoint in the IN direction which will lead to a valid status stage. If an error is detected it should instead halt the endpoint. There are two alternatives for this: A non-clearing halt which will last even after the next SETUP transaction or a clearing halt which will be removed when the next SETUP is received. The latter is the recommended behavior in the USB standard since the other will require the complete core to be reset to continue operation if the permanent halt appears on the default control endpoint.

The core can detect errors in single transactions which cause the endpoint to enter halt mode automatically. In this case the clearing halt feature will be used for control endpoints.

If a SETUP transaction indicates a control read the data phase will be in the IN direction. In that case the core user should enable data for the endpoint in the IN direction if the request was accepted otherwise the halt feature should be set. The transfer is finished when the host sends a zero length packet to the OUT endpoint.

Note that when entering halt for a control endpoint both the IN and OUT endpoints halt bits should be set.

Each time a control endpoint receives a setup token the buffers in the IN direction are emptied. This is done to prevent inconsistencies if the data and status stage were missing or corrupted and thus the data never fetched. The old data would still be in the buffer and the next setup transaction would receive erroneous data. The USB standard states that this can happen during error conditions and a new SETUP is transmitted before the previous transfer finished. The core user can also clear the buffer through the IN endpoint control register and is encouraged to do this when it detects a new SETUP before finishing the previous transfer. This must be done since the user might have enabled buffers after the core cleared them when receiving the new SETUP.

Whether data received to a descriptor for an OUT endpoint was from a SETUP transaction or an OUT transaction is indicated in a descriptor status bit.

67.5.2 Bulk endpoints

Bulk endpoints are stream pipes and therefore only use a single endpoint in either the IN or OUT direction. The endpoint with the same number in the other direction can be used independently. Data is accessed normally through the AHB interface and no special consideration need to be taken apart from the general endpoint guidelines.

67.5.3 Interrupt endpoints

Interrupt data is handled in the same manner as for bulk endpoints on the AHB interface. The differences only appear on the USB. These endpoints are also of stream type.

Interrupt endpoints support a high-bandwidth state which means that more than one transaction per microframe is performed. This necessitates buffers larger than the maximum payload size. The endpoint should be configured with a buffer larger or equal to the maximum payload times the number of transactions. All transactions will be received to/transmitted from the same buffer. The endpoint is configured as a high-bandwidth endpoint by setting the number of additional transactions to non-zero in the endpoint control register.

67.5.4 Isochronous endpoints

Isochronous endpoints are of stream type are identical to other endpoints regarding the handling on the AHB bus.

A big difference between isochronous endpoints and the other types is that they do not use handshakes. If no data is available when an IN token arrives to an Isochronous endpoint a data packet with length 0 is transmitted. This will indicate to the host that no error occurred but data was not ready. If no packet is sent the host will not know whether the packet was corrupted or not.

When not in high-bandwidth mode only one transaction in the OUT direction will be stored to a single buffer. In high-bandwidth mode all transactions during a microframe are stored to the same buffer.

In the IN direction data is always transferred from the same buffer until it is out of data. For high-bandwidth endpoints the buffer should be configured to be the maximum payload times the number of transactions in size.

Isochronous high-bandwidth endpoints use PID sequencing. When an error is detected in the PID sequence in the OUT direction no data is handed over to AHB domain for the complete microframe.

67.6 Device implementation example in master mode

This section will shortly describe how the USB device controller can be used in master mode.

A function controlling the device controller and implementing the actual application specific device will be needed. It can be either hardware, software or a combination. The only requirement is that it can control the device controller through the AHB bus.

The first thing needed for successful operation is a correctly configured PHY. This is automatically done by the device controller.

After this the device controller waits for attachment to the USB bus indicated by the VBUS becoming valid. This can be notified to the function either by polling or an interrupt. The time of attachment can be controlled by the function through the pull-up enable/disable bit in the core control register. When disabled the USB host will not notice the device even when it is plugged in.

After attachment a USB reset needs to be received before transactions are allowed to be accepted. This can also notified by polling or an interrupt.

Only control endpoint 0 should be accessible after reset. The function is responsible for enabling and configuring at the right time. It can wait until a USB reset has been received but it is easier to enable it immediately after power-up. This can be done since the device controller will not accept any transactions until USB reset has been received. When enabling the endpoint descriptors should also be enabled for both the IN and OUT direction and also the descriptor available bits should be set.

Then the endpoint is ready to accept packets and the function should wait for SETUP packets arriving. It can be notified of packets arriving either through polling or interrupts. The core should process the requests and return descriptors as requested. When a Set address request is received the function should write the new address to the device controller's global control register. It will take effect after

the next successful IN transaction for the control endpoint. This should correspond to the status stage of the Set address transfer.

When a Set configuration request is received the function should enable the appropriate interface and endpoints according to the selected configuration. This is done by writing to the various endpoint control registers. The function is responsible for advertising the configurations and interfaces through the descriptors requested by SETUP transactions.

When the endpoints for the selected configuration are enabled the function should also setup the DMA operation. Then it is ready to transmit and receive data through the application specific endpoints. Interrupts can be used to notify that new packets have transferred and then polling will determine which endpoint had a status change.

67.7 Device implementation example in slave mode

This section will shortly describe how the USB device controller can be used in slave mode.

A function controlling the device controller and implementing the actual application specific device will be needed. It can be either hardware, software or a combination. The only requirement is that it can control the device controller through the AHB bus.

The first thing needed for successful operation is a correctly configured PHY. This is automatically done by the device controller.

After this the device controller waits for attachment to the USB bus indicated by the VBUS becoming valid. This can be notified to the function either by polling or an interrupt. The time of attachment can be controlled by the function through the pull-up enable/disable bit in the core control register. When disabled the USB host will not notice the device even when it is plugged in.

After attachment an USB reset needs to be received before transactions are allowed to be accepted. This can also notified by polling or an interrupt.

Only control endpoint 0 should be accessible after reset. The function is responsible for enabling and configuring at the right time. It can wait until a USB reset has been received but it is easier to enable it immediately after power-up. This can be done since the device controller will not accept any transactions until USB reset has been received. When enabling the endpoint packet interrupts should be enabled or the function should start polling the buffer status so that it will notice when packets arrive.

Then the endpoint is ready to accept packets and the function should wait for SETUP packets arriving. When a packet arrives the core should process the requests and return USB descriptors as requested. When a Set address request is received the function should write the new address to the device controller's global control register. It will take effect immediately. It should not be written until the status stage has been finished for the Set address request. It can be determined that the request has finished if a packet transmitted interrupt is enabled for the handshake packet of the request and an interrupt is received.

When a Set configuration request is received the function should enable the appropriate interface and endpoints according to the selected configuration. This is done by writing to the various endpoint control registers. The function is responsible for advertising the configurations and interfaces through the descriptors requested by SETUP transactions.

When the endpoints for the selected configuration are enabled the function should also enable interrupts or start polling these endpoints. Then it is ready to transmit and receive data through the application specific endpoints. Interrupts can be used to notify that new packets have been transferred and then status reads will determine which endpoint had a status change.

67.8 Registers

The core is programmed through registers mapped into AHB address space.

*Table 1245.*GRUSBDC registers

AHB address offset	Register
0x00	OUT Endpoint 0 control register
0x04	OUT Endpoint 0 slave ctrl / DMA ctrl register
0x08	OUT Endpoint 0 slave data / DMA descriptor address register
0x0C	OUT Endpoint 0 status register
0x10-0x1C	OUT Endpoint 1
...	
0xF0-0xFC	OUT Endpoint 15
0x100-0x1FC	IN Endpoints 0-15
0x200	Global Ctrl register
0x204	Global Status register

67.8.1 OUT Endpoint Control Register

*Table 1246.*0x00,... - EOCTRL - OUT endpoint control register

31 21	20	19	18	17 7	6 5	4 3	2	1	0
BUFSZ	PI	CB	CS	MAXPL	NT	TT	EH	ED	EV
*	0	0	0	NR	NR	NR	0	0	0
r	rw	rw	rw	rw	rw	rw	rw	rw	rw

31: 21 Buffer size (BUFSZ) - Size/8 in bytes of one hardware buffer slot for this endpoint. Two slots are available for each endpoint.

20 Packet received interrupt (PI) - Generate an interrupt for each packet that is received on the USB for this endpoint (packet has been stored in the internal buffers). Reset value: ‘0’.

19 Clear buffers (CB) - Clears any buffers for the endpoint that contain data if the buffer is not currently active.

18 Control Stall (CS) - Return stall for data and status stages in a control transfer. Automatically cleared when the next setup token is received. Only used when the endpoint is configured as a control endpoint.

17: 7 Maximum payload (MAXPL) - Sets the maximum USB payload (maximum size of a single packet sent to/from the endpoint) size for the endpoint. All bits of the field are not always used. The maximum value for the maximum payload is determined with a generic for each endpoint. Not Reset.

6: 5 Number of transactions (NT) - Sets the number of additional transactions per microframe for high-speed endpoints and per frame for full-speed endpoints. Only valid for isochronous endpoints. Not Reset.

4: 3 Transfer type (TT) - Sets the transfer type for the endpoint. “00”=CTRL, “01” =ISOCH, “10”=BULK, “11”=INTERRUPT. Only OUT endpoints should be set to the CTRL type and then the IN endpoint with the same number will be automatically used. It is important not to use OUT endpoints that do not have a corresponding IN endpoint as a CTRL endpoint. Not Reset.

2 Endpoint halted (EH) - Halt the endpoint. If set, all transfers to this endpoint will receive a STALL handshake. Reset value: ‘0’.

1 Endpoint disabled (ED) - Disables the endpoint. If set, all transfers to this endpoint will receive a NAK handshake. Reset value: ‘0’.

0 Endpoint valid (EV) - Enables the endpoint. If not enabled, all transfers to this endpoint will be ignored and no handshake is sent. Reset value; ‘0’.

67.8.2 OUT Slave Control Register

*Table 1247.*0x04,... - EOSLUCTRL - OUT slave control register.

31 17	16	15 3	2	1	0
RESERVED	SE	BUFCNT	DA	BS	CB
0	0	0	0	0	0
r	r	r	r	r	rw

31: 17 RESERVED

16 Setup packet (SE) - The data was received from a SETUP packet instead of an OUT.

15: 3 Buffer counter (BUFCNT) - The number bytes available(OUT)

2 Data available (DA) - Set to one if a valid packet was acquired when requested using the CB. If no valid packet was available it is set to zero. Reset value: ‘0’.

1 Buffer select (BS) - Current buffer selected. Read only.

0 Change or acquire buffer (CB) - If no buffer is currently active try to acquire a new one. If one is already acquired, free it and try to acquire a new one.

67.8.3 OUT Slave Buffer Read Register

*Table 1248.*0x08,... - EOSLUDATA - OUT slave buffer read register.

31	0
DATA	
NR	
r	

31: 0 Data (DATA) - In AHB slave mode, data is fetched directly from the internal buffer by reading from this register. Data always starts from bit 31. For word accesses bits 31-0 are valid, for half-word bits 31-16 and for byte accesses bits 31-24.

67.8.4 OUT DMA Control Register

*Table 1249.*0x04,... - EODMACTRL - OUT DMA control register.

31	11	10	9	4	3	2	1	0
RESERVED		AE	RESERVED		AD	AI	IE	DA
0		0	0		0	0	0	0
r		wc	r		rw	rw	rw	rw

31: 11 RESERVED

10 AHB error (AE) - An AHB error has occurred for this endpoint.

9: 4 RESERVED

3 Abort DMA (AD) - Disable descriptor processing (set DA to 0) and abort the current DMA transfer if one is active. Reset value: ‘0’.

2 AHB error interrupt (AI) - Generate interrupt when an AHB error occurs for this endpoint.

1 Interrupt enable (IE) - Enable DMA interrupts. Each time data has been received or transmitted to/ from a descriptor with its interrupt enable bit set an interrupt will be generated when this bit is set.

0 Descriptors available (DA) - Set to indicate to the GRUSBDC that one or more descriptors have been enabled.

67.8.5 OUT Descriptor Address Register

*Table 1250.*0x08,... - EODMADESL - OUT descriptor address register.

31	2	1	0
DESCADDR		RES	
NR		00	
rw		r	

31: 2 Descriptor table address (DESCADDR) - Address to the next descriptor.Not Reset.

1: 0 RESERVED

67.8.6 OUT Endpoint Status Register

*Table 1251.*0x0C,... - EOSTAT - OUT endpoint status register

31 30	29	28 16	15 3	2	1	0
RES	PR	B1CNT	B0CNT	B1	B0	BS
0	0	0	0	0	0	0
r	wc	r	r	r	r	r

31: 30 RESERVED.

29 Packet received (PR) - Set each time a packet has been received (OUT) and stored in the internal buffers. Cleared when written with a '1'.

28: 16 Buffer 1 byte count (B1CNT) - Number of bytes in buffer one.

15: 3 Buffer 0 byte count (B0CNT) - Number of bytes in buffer zero.

2 Buffer 1 data valid (B1) - Set when buffer one contains valid data.

1 Buffer 0 data valid (B0) - Set when buffer zero contains valid data.

0 Buffer select (BS) - The currently selected buffer.

67.8.7 IN Endpoint Control Register

*Table 1252.*0x000 - EICTRL - IN endpoint control register

31 21	20	19	18	17 7	6	5	4	3	2	1	0
BUFSZ	PI	CB	CS	MAXPL	NT		TT		EH	ED	EV
*	0	0	0	NR	NR		NR		0	0	0
r	rw	rw	rw	rw	rw		rw		rw	rw	rw

31: 21 Buffer size (BUFSZ) - Size/8 in bytes of one hardware buffer slot for this endpoint. Two slots are available for each endpoint.

20 Packet transmitted interrupt (PI) - Generate an interrupt each time a packet has been transmitted on the USB and the internal buffer is cleared. Reset value: '0'.

19 Clear buffers (CB) - Clears any buffers for the endpoint that contain data if the buffer is not currently active.

18 Control Stall (CS) - Return stall for data and status stages in a control transfer. Automatically cleared when the next setup token is received. Only used when the endpoint is configured as a control endpoint.

17: 7 Maximum payload (MAXPL) - Sets the maximum USB payload (maximum size of a single packet sent to/from the endpoint) size for the endpoint. All bits of the field are not always used. The maximum value for the maximum payload is determined with a generic for each endpoint. Not Reset.

6: 5 Number of transactions (NT) - Sets the number of additional transactions per microframe for high-speed endpoints and per frame for full-speed endpoints. Only valid for isochronous endpoints. Not Reset.

4: 3 Transfer type (TT) - Sets the transfer type for the endpoint. "00"=CTRL, "01" =ISOCH, "10"=BULK, "11"=INTERRUPT. Only OUT endpoints should be set to the CTRL type and then the IN endpoint with the same number will be automatically used. It is important not to use OUT endpoints that do not have a corresponding IN endpoint as a CTRL endpoint. Not Reset.

2 Endpoint halted (EH) - Halt the endpoint. If set, all transfers to this endpoint will receive a STALL handshake. Reset value: '0'.

1 Endpoint disabled (ED) - Disables the endpoint. If set, all transfers to this endpoint will receive a NAK handshake. Reset value: '0'.

0 Endpoint valid (EV) - Enables the endpoint. If not enabled, all transfers to this endpoint will be ignored and no handshake is sent. Reset value; '0'.

67.8.8 IN Slave Control Register

*Table 1253.*0x104 - EISLVCTRL - IN slave control register.

31 17	16 4	3	2	1	0
RESERVED	BUFCNT	PI	BA	BS	EB
0	0	0	0	0	0
r	r	rw	r	r	rw

31: 17 RESERVED

16: 4 Buffer counter (BUFCNT) - The number of bytes written in the current buffer.

3 Packet interrupt enable (PI) - Generate interrupt when the activated packet has been transmitted. Should be set together with EB when enabling a packet for transmission. Reset value: ‘0’.

2 Buffer active (BA) - A free buffer was acquired and is available for use.

1 Buffer select (BS) - Current buffer selected. Read only.

0 Enable (EB) - Enable current buffer for transmission if one has been acquired and try to acquire a new buffer. If no data has been written to the buffer a zero length packet will be transmitted.

67.8.9 IN Slave Buffer read/write Register

*Table 1254.*0x108 - EISLVDATA - IN slave buffer read/write register.

31 0
DATA
NR
r

31: 0 Data (DATA) - Data written to this register is placed into the current buffer for transmission. Byte, Halfword and word sizes are allowed but only a word aligned address should be used. This means that data is always placed on 31-0 for word, 31-16 for half-word and 31-24 for byte.

67.8.10 IN DMA Control Register

*Table 1255.*0x104 - EIDMACTRL - IN DMA control register.

31 11	10	9 4	3	2	1	0
RESERVED	AE	RESERVED	AD	AI	IE	DA
0	0	0	0	0	0	0
r	wc	r	rw	rw	rw	rw

31: 11 RESERVED

10 AHB error (AE) - An AHB has occurred for this endpoint.

9: 4 RESERVED

3 Abort DMA (AD) - Disable descriptor processing (set DA to 0) and abort the current DMA transfer if one is active. Reset value: ‘0’.

2 AHB error interrupt (AI) - Generate interrupt when an AHB error occurs for this endpoint.

1 Interrupt enable (IE) - Enable DMA interrupts. Each time data has been received or transmitted to/from a descriptor with its interrupt enable bit set an interrupt will be generated when this bit is set.

0 Descriptors available (DA) - Set to indicate to the GRUSBDC that one or more descriptors have been enabled.

67.8.11 IN Descriptor Address Register

*Table 1256.*0x108 - EIDMADESC - IN descriptor address register.

31	2	1	0
DESCADDR		RES	

31: 2 Descriptor table address (DESCADDR) - Address to the next descriptor.Not Reset.

1: 0 RESERVED

67.8.12 IN Endpoint Status Register

*Table 1257.*0x10C - EISTAT - IN endpoint status register

31	30	29	28	16	15	3	2	1	0
RES		PT	B1CNT		B0CNT		B1	B0	BS
0		0	0		0		0	0	0
r		wc	r		r		r	r	r

31: 30 RESERVED.

29 Packet transmitted (PT) - Packet has been transmitted and cleared from the internal buffers. Cleared when written with a ‘1’.

28: 16 Buffer 1 byte count (B1CNT) - Number of bytes in buffer one.

15: 3 Buffer 0 byte count (B0CNT) - Number of bytes in buffer zero.

2 Buffer 1 data valid (B1) - Set when buffer one contains valid data.

1 Buffer 0 data valid (B0) - Set when buffer zero contains valid data.

0 Buffer select (BS) - The currently selected buffer.

67.8.13 CTRL Register

*Table 1258.*0x200 - GCTRL - ctrl register

31	30	29	28	27	26	16	15	14	13	12	11	9	8	7	1	0
SI	UI	VI	SP	FI	RESERVED		FT	EP	DH	RW	TS		TM	UA		SU
0	0	0	0	0	0		0	0	0	0	0		0	0		0
rw	rw	rw	rw	rw	r		rw	rw	rw	rw*	rw		rw*	rw*		w

31: Suspend interrupt (SI) - Generate interrupt when suspend status changes. Reset value: ‘0’.

30 USB reset (UI) - Generate interrupt when USB reset is detected. Reset value: ‘0’.

29 VBUS valid interrupt (VI) - Generate interrupt when VBUS status changes. Reset value: ‘0’.

28 Speed mode interrupt (SP) - Generate interrupt when Speed mode changes. Reset value: ‘0’.

27 Frame number received interrupt (FI) - Generate interrupt when a new Start of frame (SOF) token is received. Reset value: ‘0’.

26: 16 RESERVED

15 Functional test mode (FT) - Enables functional test-mode which shortens all timer such as reset and chirp timers to 8 clock cycles.

14 Enable pull-up (EP) - Enable pull-up on the D+ line signaling a connect to the host. Reset value: ‘0’.

13 Disable High-speed (DH) - Disable high-speed handshake to make the core full-speed only.

12 Remote wakeup (RW) - Start remote wakeup signaling. It is self clearing and will be cleared when it has finished transmitting remote wakeup if it was currently in suspend mode. If not in suspend mode when set it will self clear immediately. Writes to this bit when it is already asserted are ignored. Reset value: ‘0’.

11: 9 Testmode selector (TS) - Select which testmode to enter. “001”= Test_J, “010”= Test_K, “011”= Test_SE0_NAK, “100”= Test_Packet.

8 Enable test mode (TM) - Set to one to enable test mode. Note that the testmode cannot be left without resetting or power-cycling the core and cannot be entered if hsdis is set to ‘1’. Reset value: ‘0’.

*Table 1258.*0x200 - GCTRL - ctrl register

7: 1	USB address (UA) - The address assigned to the device on the USB bus.
0	Set USB address (SU) - Write with a one to set the usb address stored in the USB address field.

67.8.14 Status Register

*Table 1259.*0x204 - GSTAT - status register

31 28	27 24	23	22 18	17	16	15	14	13 11	10 0
NEPI	NEPO	DM	RESERVED	SU	UR	VB	SP	AF	FN
*	*	*	0	0	0	0	0	0	0
r	r	r	r	r	wc	r	r	r	r

31: 28	Number of implemented IN endpoints (NEPI) - The number of configurable IN endpoints available in the core (including endpoint 0) minus one.
27: 24	Number of implemented OUT endpoints (NEPO) - The number of configurable OUT endpoints available in the core (including endpoint 0) minus one.
23	Data mode (DM) - 0 = core uses slave mode for data transfers, 1 = core uses master mode (DMA) for data transfers.
22: 18	RESERVED
17	Suspended (SU) - Set to ‘0’ when the device is suspended and ‘1’ when not suspended.
16	USB reset (UR) - Set each time an USB reset has been detected. Cleared when written with a ‘1’.
15	Vbus valid (VB) - Set to one when a valid voltage has been detected on the USB vbus line.
14	Speed (SP) - The current speed mode of the USB bus. ‘0’ = high-speed, ‘1’ = full-speed.
13: 11	Additional frames (AF) - Number of additional frames received with the current frame number.
10: 0	Frame number (FN) - The value of the last SOF token received.

67.9 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x021. For description of vendor and device identifiers see GRLIB IP Library User’s Manual.

67.10 Implementation

67.10.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User’s Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support *grlib_async_reset_enable*. A subset of the registers in the USB clock domain make use of asynchronous reset.

The IP core has two different reset inputs: the AMBA reset and the USB reset. They work independently on their respective clock domains. If reset generation/synchronization is desired, it shall be done in a higher instance, out of the IP.

See also documentation of *prst* VHDL generic.

67.11 Configuration options

Table 1260 shows the configuration options of the core (VHDL generics). Buffer sizes are given in bytes and determines the sizes of one hardware buffer for the endpoint. Two buffers are available for each endpoint. The buffer size must be equal to or larger than the desired maximum payload size. In

the case of high-bandwidth endpoints the buffer size must be equal to or larger than the maximum payload times the number of transactions per (micro) frame.

*Table 1260.*Configuration options

Generic	Function	Allowed range	Default
hsindex	AHB slave index.	0 - NAHBSLV-1	0
hirq	AHB interrupt number	0 - NAHBIRQ-1	0
haddr	AHB slave address	-	0
hmask	AHB slave address mask	-	16#FFF#
hmindex	AHB master index	0 - NAHBMST-1	
aiface	0 selects the AHB slave interface for data transfer while 1 selects the AHB master interface.	0 - 1	0
memtech	Memory technology used for blockrams (endpoint buffers).	0 - NTECH	0
uiface	0 selects the UTMI interface while 1 selects ULPI.	0 - 1	0
dwidth	Selects the data path width for UTMI.	8 - 16	8
blen	Maximum number of beats in burst accesses on the AHB bus.	4 - 128	16
ninep	Number of IN endpoints	1 - 16	1
noutep	Number of OUT endpoints	1 - 16	1
i0	Buffer size for IN endpoint 0.	8, 16, 24, ... , 3072	1024
i1	Buffer size for IN endpoint 1.	8, 16, 24, ... , 3072	1024
i2	Buffer size for IN endpoint 2.	8, 16, 24, ... , 3072	1024
i3	Buffer size for IN endpoint 3.	8, 16, 24, ... , 3072	1024
i4	Buffer size for IN endpoint 4.	8, 16, 24, ... , 3072	1024
i5	Buffer size for IN endpoint 5.	8, 16, 24, ... , 3072	1024
i6	Buffer size for IN endpoint 6.	8, 16, 24, ... , 3072	1024
i7	Buffer size for IN endpoint 7.	8, 16, 24, ... , 3072	1024
i8	Buffer size for IN endpoint 8.	8, 16, 24, ... , 3072	1024
i9	Buffer size for IN endpoint 9.	8, 16, 24, ... , 3072	1024
i10	Buffer size for IN endpoint 10.	8, 16, 24, ... , 3072	1024
i11	Buffer size for IN endpoint 11.	8, 16, 24, ... , 3072	1024
i12	Buffer size for IN endpoint 12.	8, 16, 24, ... , 3072	1024
i13	Buffer size for IN endpoint 13.	8, 16, 24, ... , 3072	1024
i14	Buffer size for IN endpoint 14.	8, 16, 24, ... , 3072	1024
i15	Buffer size for IN endpoint 15.	8, 16, 24, ... , 3072	1024
o0	Buffer size for OUT endpoint 0.	8, 16, 24, ... , 3072	1024
o1	Buffer size for OUT endpoint 1.	8, 16, 24, ... , 3072	1024
o2	Buffer size for OUT endpoint 2.	8, 16, 24, ... , 3072	1024
o3	Buffer size for OUT endpoint 3.	8, 16, 24, ... , 3072	1024
o4	Buffer size for OUT endpoint 4.	8, 16, 24, ... , 3072	1024
o5	Buffer size for OUT endpoint 5.	8, 16, 24, ... , 3072	1024
o6	Buffer size for OUT endpoint 6.	8, 16, 24, ... , 3072	1024
o7	Buffer size for OUT endpoint 7.	8, 16, 24, ... , 3072	1024
o8	Buffer size for OUT endpoint 8.	8, 16, 24, ... , 3072	1024
o9	Buffer size for OUT endpoint 9.	8, 16, 24, ... , 3072	1024
o10	Buffer size for OUT endpoint 10.	8, 16, 24, ... , 3072	1024
o11	Buffer size for OUT endpoint 11.	8, 16, 24, ... , 3072	1024

*Table 1260.*Configuration options

Generic	Function	Allowed range	Default
o12	Buffer size for OUT endpoint 12.	8, 16, 24, ... , 3072	1024
o13	Buffer size for OUT endpoint 13.	8, 16, 24, ... , 3072	1024
o14	Buffer size for OUT endpoint 14.	8, 16, 24, ... , 3072	1024
o15	Buffer size for OUT endpoint 15.	8, 16, 24, ... , 3072	1024
oepol	Select polarity of output enable signal. 1 selects active high and 0 selects active low.	0 - 1	0
keepclk	This generic determines wheter or not the USB transceiver will be suspended and have its clock turned off during USB suspend. Set this generic to 1 if the clock should not be turned off. This might be needed for some technologies that can't handle that the USB clock is turned off for long periods of time.	0 - 1	0
sepirq*	Set this generic to 1 if three seperate interrupt lines should be used, one for status related interrupts, one for IN endpoint related interrupts, and one for OUT endpoint related interrupts. The irq number for the three different interrupts are set with the hirq (status), irqi (IN), and irqo (OUT) generics. If sepirq = 0 then only interrupts with irq number hirq will be generated.	0 - 1	0
irqi*	Sets the irq number for IN endpoint related interrupts. Only used if sepirq generic is set to 1.	0 - NAHBIRQ-1	1
irqo*	Sets the irq number for OUT endpoint related interrupts. Only used if sepirq generic is set to 1.	0 - NAHBIRQ-1	2
functesten	Enable functional test mode. This is used to skip the USB high-speed detection sequence to reduce the number of test vectors during functional testing.	0 - 1	0
scantest	Set this generic to 1 if scan test support should be implemented.	0 - 1	0

* The values of these generics are stored in the first User-Defined word of the core's AHB plug-n-play area as follows: bit 0 = sepirq, bits 7:4 = irqi, bits 11:8 = irqo. Please see the AHBCTRL section of GRLIB IP Core User's Manual.

67.12 Signal descriptions

Table 1261 shows the interface signals of the core (VHDL ports).

*Table 1261.*Signal descriptions

Signal name	Field	Type	Function	Active
UCLK	N/A	Input	USB UTMI/ULPI Clock	-
URST		Input	USB Reset	Low
HCLK		Input	AMBA Clock	-
HRST		Input	AMBA Reset	Low
AHBMI	*	Input	AHB master input signals	-
AHBMO	*	Output	AHB master output signals	-
AHBSI	*	Input	AHB slave input signals	-
AHBSO	*	Output	AHB slave output signals	-
USBI	datain[15:0]	Input	UTMI/UTMI+/ULPI. Bits 15:8 are only used in 16-bit UTMI/UTMI+ mode.	-
	rxactive	Input	UTMI/UTMI+	High
	rxvalid	Input	UTMI/UTMI+	High
	rxvalidh	Input	UTMI/UTMI+ 16-bit	High

*Table 1261.*Signal descriptions

Signal name	Field	Type	Function	Active
	rxerror	Input	UTMI/UTMI+	High
	txready	Input	UTMI/UTMI+	High
	linestate[1:0]	Input	UTMI/UTMI+	-
	nxt	Input	ULPI	High
	dir	Input	ULPI	High
	vbusvalid	Input	UTMI+	High
	urstdrive	Input	This input determines if the cores should drive the transceiver data lines low during USB transceiver reset, even if the dir input is High. This is needed for some transceivers, such as the NXP ISP1504. When this input is low the direction of the transceiver data lines are exclusively controlled by the dir signal from the transceiver. When this input is high the core will drive the data lines low during transceiver reset. Only applicable for ULPI transceivers.	High
USBO	dataout[15:0]	Output	UTMI/UTMI+/ULPI. Bits 15:8 are only used in 16-bit UTMI/UTMI+ mode.	-
	txvalid	Output	UTMI+	High
	txvalidh	Output	UTMI+ 16-bit	High
	opmode[1:0]	Output	UTMI+	-
	xcvrselect[1:0]	Output	UTMI/UTMI+. Bit 1 is constant low.	-
	termselect	Output	UTMI/UTMI+	-
	suspendm	Output	UTMI/UTMI+	Low
	reset	Output	Transceiver reset signal. Asserted asynchronously and deasserted synchrnously to the USB clock.	**
	stp	Output	ULPI	High
	oen	Output	Data bus direction control for ULPI and bi-directional UTMI/UTMI+ interfaces.	***
	databus16_8	Output	UTMI+. Constant high for 16-bit interface, constant low for 8-bit interface.	-
	dppulldown	Output	UTMI+. Constant low.	High
	dmpulldown	Output	UTMI+. Constant low.	High
	idpullup	Output	UTMI+. Constant low.	High
	drvvbus	Output	UTMI+. Constant low.	High
	dischrgvbus	Output	UTMI+. Constant low.	High
	chrgvbus	Output	UTMI+. Constant low.	High
	txbitstuffenable	Output	UTMI+. Constant low.	High
	txbitstuffenableh	Output	UTMI+. Constant low.	High
	fslsserialmode	Output	UTMI+. Constant low.	High
	tx_enable_n	Output	UTMI+. Constant high.	Low
	tx_dat	Output	UTMI+. Constant low.	High
	tx_se0	Output	UTMI+. Constant low.	High

* See GRLIB IP Library User's Manual.

** Depends on transceiver interface. Active high for UTMI/UTMI+ and active low for ULPI.

*** Implementation dependent.

67.13 Library dependencies

Table 1262 shows libraries used when instantiating the core (VHDL libraries).

*Table 1262.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	GRUSB	Signals, component	GRUSBDC component declarations, USB signals

67.14 Instantiation

This example shows how the core can be instantiated.

```
usbdc0: GRUSBDC
    generic map(
      hsindex       => 4,
      hirq          => 0,
      haddr         => 16#001#,
      hmask         => 16#FFF#,
      hmindex       => 14,
      aiface        => 1,
      memtech       => memtech,
      uiface        => 0,
      dwidth        => 8,
      nepi          => 16,
      nepo          => 16)
    port map(
      uclk          => uclk,
      urst          => urstn,
      usbi          => usbi,
      usbo          => usbo,
      hclk          => clkm,
      hrst          => rstn,
      ahbmi         => ahbmi,
      ahbmo         => ahbmo(14),
      ahbsi         => ahbsi,
      ahbso         => ahbso(4)
     );

usb_d_pads: for i in 0 to 15 generate
  usb_d_pad: iopad generic map(tech => padtech, slew => 1)
    port map (usb_d(i), usbo.dataout(i), usbo.oen, usbi.datain(i));
end generate;

usb_h_pad:iopad generic map(tech => padtech, slew => 1)
  port map (usb_validh, usbo.txvalidh, usbo.oen, usbi.rxvalidh);

usb_i0_pad : inpad generic map (tech => padtech) port map (usb_txready,usbi.txready);
usb_i1_pad : inpad generic map (tech => padtech) port map (usb_rxvalid,usbi.rxvalid);
usb_i2_pad : inpad generic map (tech => padtech) port map (usb_rxerror,usbi.rxerror);
usb_i3_pad : inpad generic map (tech => padtech) port map (usb_rxactive,usbi.rxactive);
usb_i4_pad : inpad generic map (tech => padtech) port map
(usb_linestate(0),usbi.linestate(0));
usb_i5_pad : inpad generic map (tech => padtech) port map
(usb_linestate(1),usbi.linestate(1));
usb_i6_pad : inpad generic map (tech => padtech) port map (usb_vbus, usbi.vbusvalid);

usb_o0_pad : outpad generic map (tech => padtech, slew => 1) port map (usb_reset,usbo.reset);
usb_o1_pad : outpad generic map (tech => padtech, slew => 1) port map
(usb_suspend,usbo.suspendm);
usb_o2_pad : outpad generic map (tech => padtech, slew => 1) port map
(usb_termsel,usbo.termselect);
usb_o3_pad : outpad generic map (tech => padtech, slew => 1) port map
(usb_xcvrsel,usbo.xcvrselect(0));
usb_o4_pad : outpad generic map (tech => padtech, slew => 1) port map
(usb_opmode(0),usbo.opmode(0));
```

```
usb_o5_pad : outpad generic map (tech => padtech, slew => 1) port map
(usb_opmode(1),usbo.opmode(1));
usb_o6_pad : outpad generic map (tech => padtech, slew => 1) port map
(usb_txvalid,usbo.txvalid);

usb_clk_pad : clkpad generic map (tech => padtech, arch => 2) port map (usb_clkout, uclk);

usbi.urstdrive <= '0';
```

68 GRUSB_DCL - USB Debug Communication Link

68.1 Overview

The Universal Serial Bus Debug Communication Link (GRUSB_DCL) provides an interface between a USB 2.0 bus and an AMBA-AHB bus. The core must be connected to the USB through an UTMI, UTMI+, or ULPI compliant PHY. Both full-speed and high-speed mode are supported. The GRUSB_DCL rely on the GRUSBDC core for handling the USB communication and communication with the PHY. The GRUSB_DCL implements the minimum required set of USB requests to be Version 2.0 compliant and a simple protocol for performing read and write accesses on the AHB bus. Figure 198 show how the GRUSB_DCL can be connected to a PHY. For more information on the GRUSBDC and the connection to the USB PHY please refer to the GRLIB IP Core User's Manual.

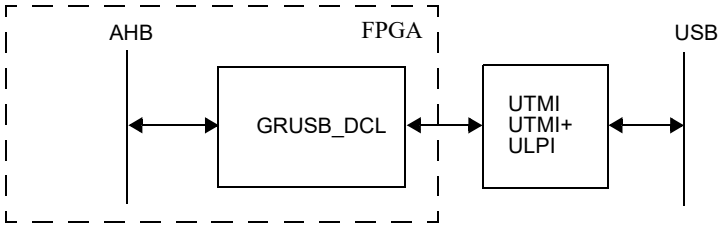


Figure 198. USBDCL connected to an external UTM.

68.2 Operation

68.2.1 System overview

The internal structure of the GRUSB_DCL can be seen in figure 199. The GRUSB_DCL is constructed with two internal AHB busses for communication with the GRUSBDC and one external AHB master interface for reading and writing the external AHB bus. Since the GRUSBDC is connected with point-to-point links there is no need for a conventional AHB arbiter on the internal bus.

The GRUSBDC is configured with two bidirectional endpoints with endpoint zero (EP0) being the default USB control endpoint and endpoint one (EP1) the communication endpoint for the DCL protocol. The GRUSBDC is configured to use DMA and its descriptors as well as the DMA buffers are stored in a local memory with separate read and write ports (SYNCRAM_2P). The two ports makes it possible for the GRUSBDC and the internal workings of the GRUSB_DCL to access the memory in parallel. Arbitration for the read and write port is implemented as two separate procedures. The main functionality of the GRUSB_DCL is implemented in the main FSM procedure. The FSM can be seen in figure 200.

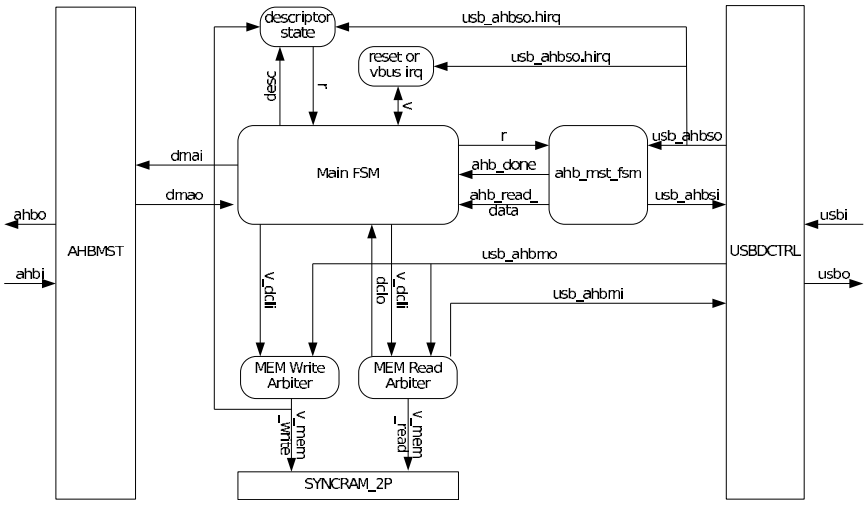


Figure 199. Block diagram of the internal structure of the GRUSBDCL. Blocks with rounded corners are implemented as VHDL procdures while squares represent VHDL entities.

Upon reset the FSM begins with setting up the DMA descriptors in the local memory and then configures the GRUSBDC such that it becomes active. The FSM then waits for incoming requests on either EP0 or EP1. For EP0 each request is validated and then appropriate action is taken according to the USB Version 2.0 standard. For undefined requests the GRUSB_DCL returns an error by stalling EP0. For EP1 the DCL request is fetched and either data is written to the AHB buss from the local memory or data is read from the AHB and stored in the local memory. In the case of the AHB is being read the data is then sent on EP1 IN. To keep track of the state of the DMA descriptors the FSM has help from the descriptor-state procedure. The descriptor-state procedure uses the IRQ from the GRUSBDC to identify incoming packets on either EP0 or EP1. By storing the last accessed address by the GRUSBDC to the local memory the descriptor-state procedure can tell which EP that has been updated. The FSM in turn signals the procedure telling it when a DMA descriptor/buffer has been read/write. A small FSM (ahb_mst_fsm) is also used when the main FSM wants to update the state of the GRUSBDC through the AHB slave interface. Finally, the reset-or-vbus-irq procedure listens on irqs from the USBDC that informs the core that a USB reset or that a change on the VBUS has occured. In that case the core stops what ever it was doing and moves into the USB default state (no addresse set and not configured).

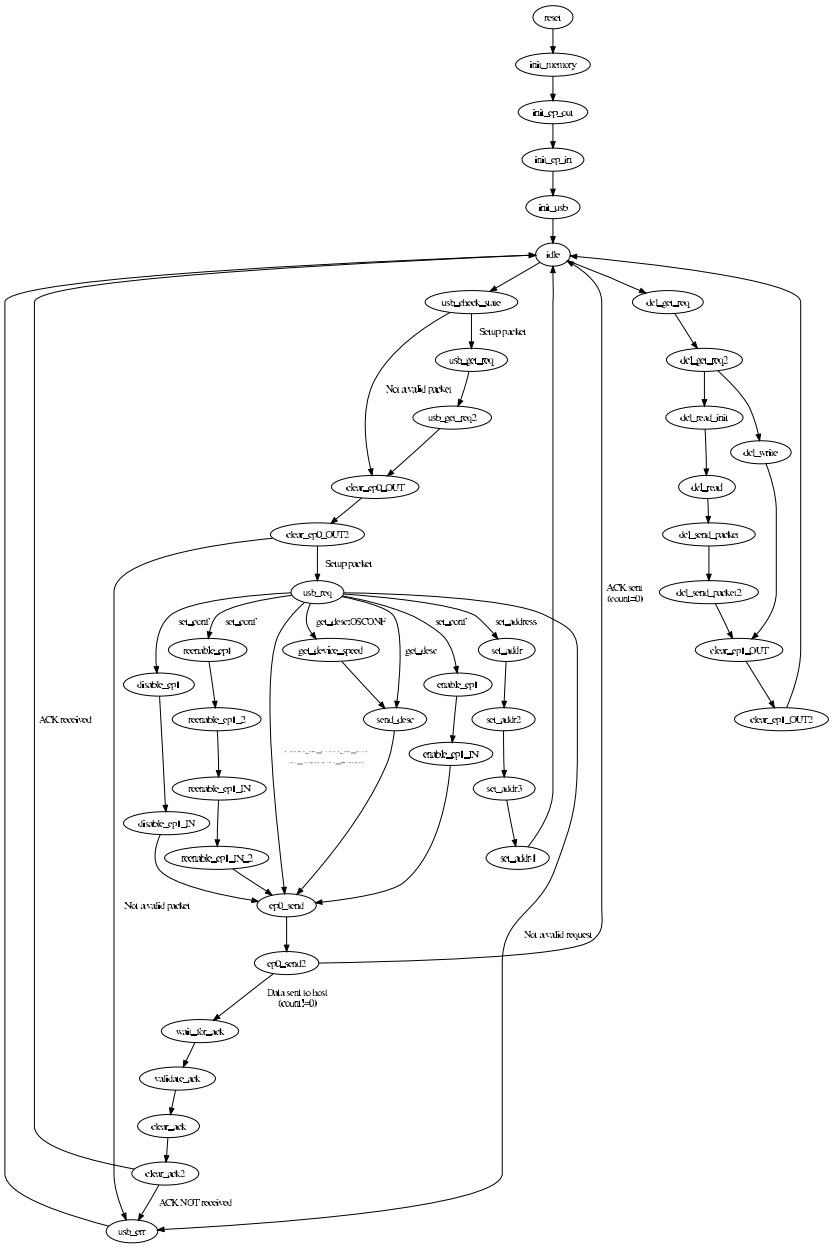


Figure 200. The main FSM of the GRUSBDCL. The FSM can be divided into three major parts i) the initialization (reset to idle), ii) handling of USB requests (seen to the left of idle), and iii) handling of DCL requests (seen to the right of idle).

68.2.2 Protocol

The protocol used for the AHB commands is very simple and consists of two 32-bit control words. The first word consists of the 32-bit AHB address and the second consists of a read/write bit at bit 31 and the number of words to be written at bits 16 downto 2. All other bits in the second word are reserved for future use and must be set to 0. The read/write bit must be set to 1 for writes.

Figure 201 shows the layout of a write command. The command should be sent as the data cargo of an OUT transaction to endpoint 1. The data for a command must be included in the same packet. The maximum payload is 512 B when running in high-speed mode and 64 B in full-speed mode. Since the control information takes 8 B the maximum number of bytes per command is 504 B and 56 B respectively. Subword writes are not supported so the number of bytes must be a multiple of four between 0 and 504.

The words should be sent with the one to be written at the start address first. Individual bytes should be transmitted msb first, i.e. the one at bits 31-24.

There is no reply sent for writes since the USB handshake mechanism for bulk writes guarantees that the packet has been correctly received by the target.

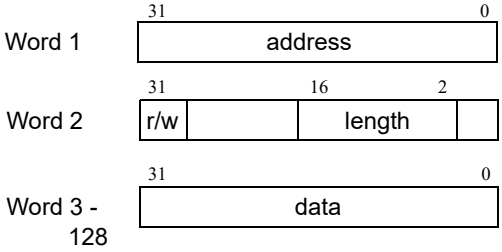


Figure 201. Layout of USBDCL write commands.

Figure 202 shows the layout of read commands and replies. In this case the command only consists of two words containing the same control information as the two first words for write commands. However, for reads the r/w bit must be set to 0.

When the read is performed data is read to the buffer belonging to IN endpoint 1. The reply packet is sent when the next IN token arrives after all data has been stored to the buffer. The reply packets only contains the read data (no control information is needed) with the word read from the start address transmitted first. Individual bytes are sent with most significant byte first, i.e. the byte at bit 31 downto 24.

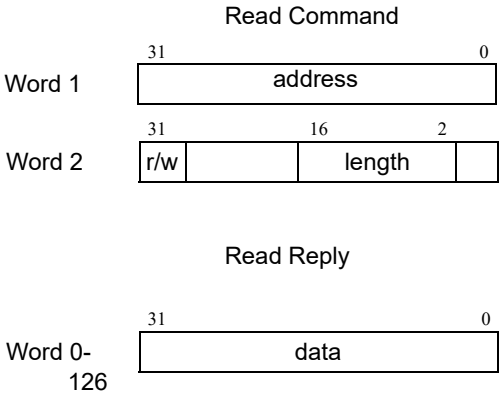


Figure 202. Layout of USBDCL read commands and replies.

68.2.3 AHB operations

All AHB operations are performed as incremental bursts of unspecified length. Only word size accesses are done.

68.3 Registers

The core does not contain any user accessible registers.

68.4 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x022. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

The USB vendor identifier is 0x1781 and product identifier is 0x0AA0.

68.5 Implementation

68.5.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support *grlib_async_reset_enable*. A subset of the registers in the USB clock domain make use of asynchronous reset.

The IP core has two different reset inputs: the AMBA reset and the USB reset. They work independently on their respective clock domains. If reset generation/synchronization is desired, it shall be done in a higher instance, out of the IP.

See also documentation of *syncprst* VHDL generic.

68.5.2 Scan test support

The VHDL generic *scantest* enables scan test support for both the GRUSB_DCL and GRUSBDC. When the scanen and testen signals in the AHB master input record are high the GRUSB_DCL will disable the internal RAM blocks.

See GRUSBDC section of GRLIB IP Core User's Manual for details on the scan support for GRUSBDC.

68.6 Configuration options

Table 1263 shows the configuration options of the core (VHDL generics).

*Table 1263.*Configuration options

Generic	Function	Allowed range	Default
hindex	AHB master index.	0 - NAHBMST-1	0
memtech	Memory technology used for blockrams (endpoint buffers).	0 - NTECH	0
uiface	Please see GRUSBDC section in the GRLIB IP Core User's Manual.		
dwidth	Please see GRUSBDC section in the GRLIB IP Core User's Manual.		
oepol	Please see GRUSBDC section in the GRLIB IP Core User's Manual.		
keepclk	Please see GRUSBDC section in the GRLIB IP Core User's Manual.		
functesten	Please see GRUSBDC section in the GRLIB IP Core User's Manual. If this generic is non-zero, the core will sample the value of its functesten input signal during reset. This value will then be used when assigning the Functional Testmode field in the GRUSBDC control register. The functesten input can be useful during netlist simulation as functional test mode reduces simulation time. If this generic is set to zero, the value of the functesten input will be disregarded and the Functional Testmode field will always be written with '0'.		
burstlength	Sets the maximum burst length in 32-bit words. The core will not burst over a burstlength word boundary.	8	1 - 512
scantest	Set this generic to 1 if scan test support should be implemented.	0 - 1	0

68.7 Signal descriptions

Table 1264 shows the interface signals of the core (VHDL ports).

*Table 1264.*Signal descriptions

Signal name	Field	Type	Function	Active
UCLK	N/A	Input	USB UTMI/ULPI Clock	-
URST	N/A	Input	USB Reset	Low
USBI	*	Input	USB Input signals	-
	functesten	Input	Functional test enable. If the core has been implemented with support for functional test mode (VHDL generic *functesten*), this signal will be sampled during core reset. Its value will then be used to set the functional testmode enable bit in the GRUSBDC core's control register.	High
USBO	*	Output	USB Output signals	-
HCLK		Input	AMBA Clock	-
HRST		Input	AMBA Reset	Low
AHBMI	**	Input	AHB master input signals	-
AHBMO	**	Output	AHB master output signals	-

* see GRUSBDC section og GRLIB IP Core User's Manual

** see GRLIB IP Library User's Manual

68.8 Library dependencies

Table 1265 shows libraries used when instantiating the core (VHDL libraries).

*Table 1265.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	GRUSB	Signals, components	GRUSB_DCL and GRUSBDC component declarations, USB signals

68.9 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.grusb.all;

entity usbdcl_ex is
  port (
    clk : in std_ulogic; --AHB Clock
    rstn : in std_ulogic;

    -- usb signals
    usb_clkout  : in std_ulogic;
    usb_rst     : in std_ulogic;
    usb_d       : inout std_logic_vector(7 downto 0);
    usb_nxt     : in  std_ulogic;
    usb_stp     : out std_ulogic;
    usb_dir     : in  std_ulogic;
    usb_resetn  : out std_ulogic
end;

architecture rtl of usbdcl_ex is
  constant padtech : integer := inferred;
  constant memtech : integer := inferred;

  -- AMBA signals
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);
  -- USB signals
  signal usbi : grusb_in_type;
  signal usbo : grusb_out_type;
  signal uclk : std_ulogic;
  signal urstn : std_ulogic;

begin

  -- AMBA Components are instantiated here
  ...

  -- GRUSB_DCL
  usb_d_pad: iopadv
    generic map(tech => padtech, width => 8)
    port map (usb_d, usbo.dataout, usbo.oen, usbi.datain);
  usb_nxt_pad : inpad generic map (tech => padtech)
    port map (usb_nxt, usbi.nxt);
  usb_dir_pad : inpad generic map (tech => padtech)
    port map (usb_dir, usbi.dir);
  usb_resetn_pad : outpad generic map (tech => padtech)
    port map (usb_resetn, usbo.reset);
  usb_stp_pad : outpad generic map (tech => padtech)
```

```
    port map (usb_stp, usbo.stp);

  usb_clkout_pad : clkpad
    generic map (tech => padtech)
    port map (usb_clkout, uclk);

  usb_input_rst_pad : inpad
    generic map (tech => padtech)
    port map (usb_rst, urstn);

  usbi.urstdrive <= '0';

  usbdcl0: grusb_dcl
    generic map (
        hindex  => 0,
        memtech => memtech,
        uiface  => 1,
        dwidth  => 8,
        oepol   => 0)
    port map (
        uclk => uclk,
        urst => urstn,
        usbi => usbi,
        usbo => usbo,
        hclk => clk,
        hrst => rstn,
        ahbi => ahbmi,
        ahbo => ahbmo(0));
end;
```

69 GRUSBHC - USB 2.0 Host Controller

69.1 Overview

The Cobham Gaisler USB 2.0 Host Controller provides a link between the AMBA AHB bus and the Universal Serial Bus. The host controller supports High-, Full-, and Low-Speed USB traffic. USB 2.0 High-Speed functionality is supplied by an enhanced host controller implementing the Enhanced Host Controller Interface revision 1.0. Full- and Low-Speed traffic is handled by up to 15 (USB 1.1) companion controllers implementing the Universal Host Controller Interface, revision 1.1. Each controller has its own AMBA AHB master interface. Configuration and control of the enhanced host controller is done via the AMBA APB bus. Companion controller registers are accessed via an AMBA AHB slave interface. Figure 203 shows a USB 2.0 host system and the organization of the controller types. Figure 204 shows an example with both host controller types present.

The controller supports both UTMI+ and ULPI transceivers and can handle up to 15 ports.

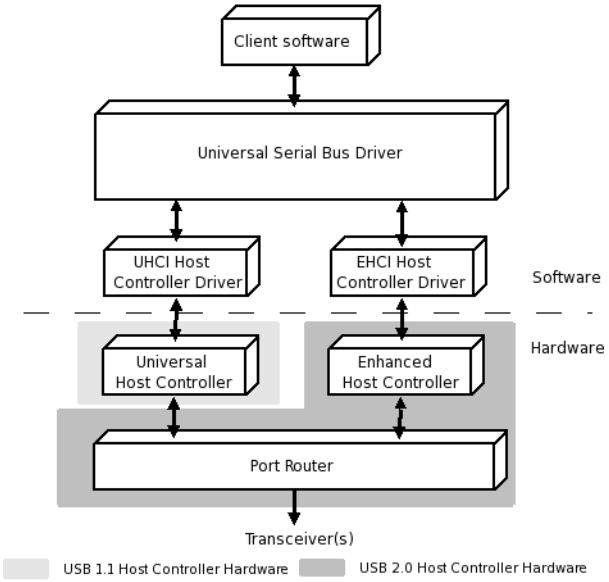


Figure 203. Block diagram of USB 2.0 host system

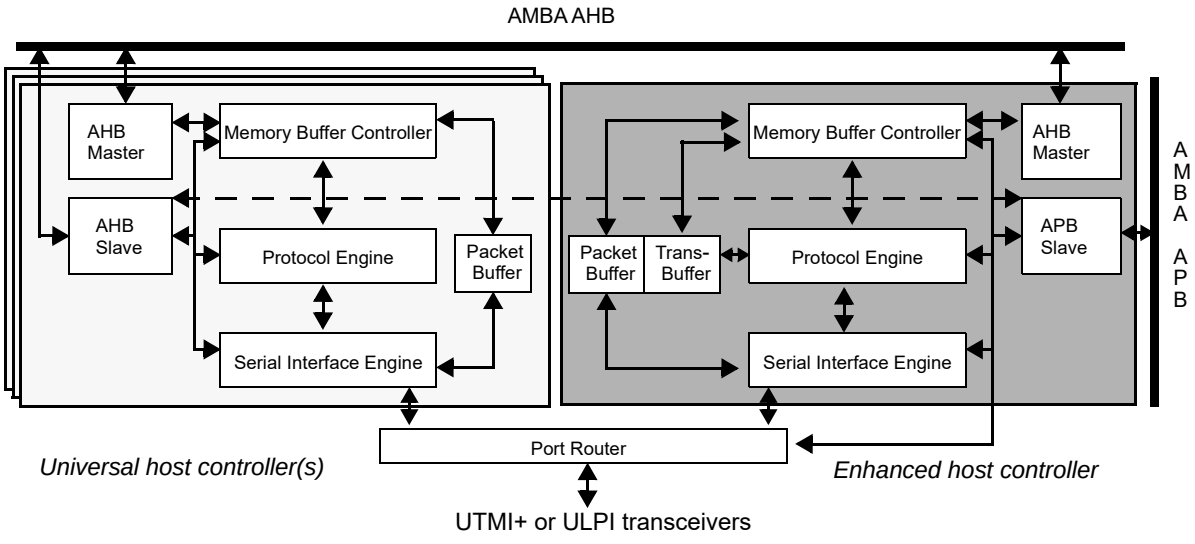


Figure 204. Block diagram of both host controller types

69.2 Operation

69.2.1 System overview

Depending on the core's configuration it may contain both controller types, one enhanced host controller, or up to 15 standalone universal host controllers. If both controller types are present, each universal host controller acts as a companion controller to the enhanced host controller.

The enhanced host controller complies with the Enhanced Host Controller Interface with the exception of the optional Light Host Controller Reset, which is not implemented.

The universal host controller complies with the Universal Host Controller Interface, with exceptions. The HCHalted field in the USB Command register is implemented as Read Only instead of Read/Write Clear. The Port Status/Control registers have been extended with Over Current and Over Current Change fields. Changes to both registers have been done in accordance with contemporary implementations of the interface. Both changes match the description of corresponding bits in the EHCI specification.

69.2.2 Protocol support

The enhanced host controller has full support for High-Speed traffic as defined in the USB Specification, revision 2.0. In addition Asynchronous Park Mode is supported, and the controller has a NAK counter.

The universal host controller supports Full- and Low-Speed traffic.

69.2.3 Descriptor and data buffering

The enhanced host controller prefetches one frame of isochronous descriptors. All payload data for a transaction is fetched before the transaction is executed. The enhanced host controller has a 2048 byte buffer for descriptors and a 2048 byte buffer for payload data, which can hold data for two transactions.

The universal host controller does not prefetch descriptors. Depending on controller configuration a transaction on the bus may be initiated before all payload data has been fetched from memory. Each universal host controller has a 1024 byte buffer for payload data. A transfer descriptor in UHCI may describe a transaction that has a payload of 1280 bytes. The USB specification limits the maximum allowed data payload to 1023 bytes and the controller will not transfer a larger payload than 1023 bytes. If a descriptor has a, legal, larger payload than 1023 bytes, the controller will only attempt to transfer the first 1023 bytes before the transaction is marked as completed.

In the event that the host controller has just one port, the universal host controller and the enhanced host controller will share the data payload buffer. Thus only two 2048 byte buffers are required.

69.2.4 Endianness

The core always accesses the least significant byte of a data payload at offset zero. Depending on the core's configuration, registers may be big endian, little endian, or byte swapped little endian.

69.2.5 RAM test facilities

The VHDL generic *ramtest* adds the possibility to test the RAM by mapping the core's internal buffers into the register space. If the core is implemented with RAM test facilities the universal host controller maps the packet buffer at offset 0x400 - 0x7FF. An enhanced host controller will map the packet buffer at offset 0x1000 - 0x17FF and the transaction buffer at 0x1800 - 0x1FFF. Note that the VHDL generics *uhchmask* and *ehcpmask* must be modified to allow access to the increased number of registers. The three least significant bits of the universal host controller's mask must be set to zero. The enhanced host controller's mask must have its five least significant bits set to zero.

When the *ramtest* generic is set to one an extra register called *RAM test control* register is added to both the universal and the enhanced controller. This register is described in section 69.8.1 and 69.8.2. To perform the RAM tests the user should first make sure that both the universal host controller and enhanced host controller are in their respective idle state. Note that if the core has only one port then the enhanced controller and the universal controller share the packet buffer. The shared buffer can be tested through both of the controllers but the controller performing the test must be the current owner of the port. For information on how to enter idle state and change ownership of the port please see section 69.8. When the controllers are in their idle states the enable bit in the *RAM test control* register should be set to one.

Once RAM test is enabled the whole RAM can be tested by first filling the buffers by writing to the corresponding register addresses and then setting the start bit in the *RAM test control* register. When the start bit is set the controller will, in order to access to the RAM from all its ports, read and write the whole packet buffer from the USB domain. If the core uses dual port RAM (see section 69.10.2 for more information on RAM usage) the same thing is done with the transaction buffer (if it is the enhanced controller that is performing the test). When the core uses double port RAM both the read and write port of the transaction buffer is located in the AHB domain, and therefore both the read and write port is tested during read and write accesses to register space. When the transfers are finished the core will clear the start bit and the data can then be read back through register space and be compared with the values that were written. When the core is implemented with dual port RAM individual addresses in the packet buffer and transaction buffer can be written and read without using the start bit. When using double port RAM only the transaction buffer can be read without using the start bit. However when individual addresses are accessed the buffers are only read/written from the AHB domain.

69.3 Port routing

Port routing is implemented according to the EHCI specification but functions regardless of whether the core is configured with or without an enhanced host controller. The VHDL generic prr enables or disables Port Routing Rules. With Port Routing Rules enabled, each port can be individually routed to a specific universal host controller via the VHDL generics portroute1 and portroute2. If Port Routing Rules is disabled the n_pcc lowest ports are routed to the first companion controller, the next n_pcc ports to the second companion controller, and so forth. The HCSP-PORTROUTE array is communicated via the portroute VHDL generics, which are calculated with the following algorithm:

$$\text{portroute1} = 2^{26}*CC_8 + 2^{22}*CC_7 + 2^{18}*CC_6 + 2^{14}*CC_5 + 2^{10}*CC_4 + 2^{6}*CC_3 + 2^{2}*CC_2 + CC_1 / 4$$

$$\text{portroute1} = 2^{26}*CC_{15} + 2^{22}*CC_{14} + 2^{18}*CC_{13} + 2^{14}*CC_{12} + 2^{10}*CC_{11} + 2^{6}*CC_{10} + 2^{2}*CC_9 + CC_1 \bmod 4$$

where CC_P is the companion controller that port P is routed to. Companion controllers are enumerated starting at 1.

When the enhanced host controller has not been configured by software, or when it is nonexistent, each port is routed to its companion controller. This allows a universal host controller to function even if the host system does not have support for the enhanced host controller. Please see the EHCI specification for a complete description of port routing.

69.4 DMA operations

Both host controller types have configurable DMA burst lengths. The burst length in words is defined by the VHDL generic bwrd. The value of bwrd limits how many words a controller may access in memory during a burst and not the number of memory operations performed after bus access has been granted. When writing a data payload back to memory that requires half-word or byte addressing the number of memory operations may exceed bwrd by one before the bus is released. If a host controller

is given a byte-aligned data buffer its burst length may exceed the bwrd limit with one word when fetching payload data from memory.

The universal host controller uses a burst length of four words when fetching descriptors. This descriptor burst length is not affected by the bwrd VHDL generic. The universal host controller may be configured to start transactions on the USB before all data has been fetched from memory. The VHDL generic uhcblo specifies the number of words that must have been fetched from memory before a USB transaction is started. Since the USB traffic handled by the universal host controller can be expected to have significantly lower bandwidth than the system memory bus, this generic should be set to a low value.

69.5 Endianness

The core works internally with little endian. If the core is connected to a big endian bus, endian conversion must be enabled. When the VHDL generic endian_conv is set, all AMBA data lines are byte swapped. With endian_conv correctly set the core will start accessing data payloads from byte offset zero in the buffer, this is the first byte that is moved on the USB. The VHDL generic endian_conv must be set correctly for byte and halfword accesses to work. Therefore it is not possible to change the byte order of the buffer by configuring the controller for a little endian bus when it is connected to a big endian bus or vice versa.

The VHDL generics be_regs and be_desc are used to place the controller into big endian mode when endian conversion is enabled. These configuration options have no effect when the core is connected to a little endian bus, as determined by the value of VHDL generic endian_conv. The VHDL generic be_regs arranges the core's registers in accordance with big endian addressing. In the enhanced host controller this will only affect the placement of the register fields CAPLENGTH and HCIVERSION, the HCSP-PORTROUTE array, and - if implemented - the PCI registers *Serial Bus Release Number Register* and *Frame Length Adjustment Register*. In the universal host controller be_regs will affect the placement of all registers. When be_regs is set, the bus to the register interface is never byte swapped. Tables 1266 - 1268 below illustrate the difference between big endian, little endian, and little endian layout with byte swapped (32 bit) WORDs on two 16 bit registers. Register R1 is located at address 0x00 and register R2 is located at address 0x02.

*Table 1266.*R1 and R2 with big endian addressing

31	16	15	0
R1(15:0)		R2(15:0)	

*Table 1267.*R1 and R2 with little endian addressing

31	16	15	0
R2(15:0)		R1(15:0)	

*Table 1268.*R1 and R2 with little endian layout and byte swapped DWORD

31	24	23	16	15	8	7	0
R1(7:0)		R1(15:8)		R2(7:0)		R2(15:8)	

The VHDL generic be_desc removes the byte swapping of descriptors on big endian systems. Tables 1269 and 1270 below list the effects of endian_conv and be_regs on a big endian and a little endian system respectively.

*Table 1269.*Effect of endian_conv, be_regs, and be_desc on a big endian system

endian_conv	be_regs	be_desc	System configuration
0	-	-	Illegal. DMA will not function.
1	0	0	Host controller registers will be arranged according to little endian addressing and each DWORD will be byte swapped. In-memory transfer descriptors will also be byte swapped. This is the correct configuration for operating systems, such as Linux, that swap the bytes on big endian systems.
1	0	1	Host controller registers are arranged according to little endian addressing and will be byte swapped. Transfer descriptors will not be byte swapped.
1	1	0	Host controller registers will be arranged according to big endian addressing and will not be byte swapped. In memory transfer descriptors will be byte swapped.
1	1	1	Host controller registers will be arranged according to big endian addressing. In memory transfer descriptors will not be byte swapped.

*Table 1270.*Effect of endian_conv, be_regs and be_desc on a little endian system

endian_conv	be_regs	be_desc	System configuration
0	-	-	Host controller registers will be placed as specified in the register interface specifications.
1	-	-	Illegal. DMA will not function.

69.6 Transceiver support

The controller supports UTMI+ 8-bit, UTMI+ 16-bit, and ULPI transceivers. All connected transceivers must be of the same type. Note that the transceiver type is fixed and the core can therefore not change between 8-bit and 16-bit UTMI+ interface during operation. Transceiver signals not belonging to the selected transceiver type are not connected and do not need to be driven. When using ULPI transceivers the default, and recommended, configuration is to use an external source for USB bus power (VBUS) as well as external VBUS fault detection. However the core can be configured to support configurations where the ULPI transceiver handles VBUS generation and fault detection internally, and configurations where VBUS generation is external to transceiver but fault detection is handled internally. Also the active level of the VBUS fault indicator can be configured. The configuration is handled by the vbusconf generic. If UTMI+ transceivers are used it does not matter to the core how VBUS generation and fault detection is handled as long as the VBUS enable signal and VBUS fault indicator are connected to the core's drvvbus and vbusvalid signals respectively. The UTMI+ specification defines these two signals to be active high, however in order to support different types of USB power switches and fault detectors the core can be configured to have active low drvvbus and vbusvalid signals. This configuration is also handled by the vbusconf generic. The UTMI+ interface is described in *USB 2.0 Transceiver Macrocell Interface (UTMI) Specification* and *UTMI+ Specification Revision 1.0*. The ULPI interface is described in *UTMI+ Low Pin Interface (ULPI) Specification Revision 1.1*.

69.7 PCI configuration registers and legacy support

The VHDL generic *pcidev* is used to configure the core to be used as a PCI device. If the core is configured to be used as a PCI device then the PCI registers *Serial Bus Release Number Register* and *Frame Length Adjustment Register* are implemented in the enhanced controller. The *Serial Bus Release Number Register* is also implemented for the universal controller. See *Enhanced Host Controller Interface Specification (EHCI) for Universal Serial Bus revision 1.0* and *Universal Host Controller Interface (UHCI) Design Guide revision 1.1* for details.

Legacy support is not implemented.

69.8 Registers

69.8.1 Enhanced host controller

The core is programmed through registers mapped into APB address space. The contents of each register is described in the *Enhanced Host Controller Interface Specification (EHCI) for Universal Serial Bus revision 1.0. A* register called *RAM test control* is added when the VHDL generic *ramtest* is set to one. The *RAM test control* register is not part of the EHCI interface and is described below. Also registers mapped to the packet buffer and transaction buffer are added if RAM test facilities are implemented.

*Table 1271.*Enhanced Host Controller capability registers

APB address offset	Register
0x00	Capability Register Length
0x01	Reserved
0x02	Interface Version Number
0x04	Structural Parameters
0x08	Capability Parameters
0x0C	Companion Port Route Description

*Table 1272.*Enhanced Host Controller operational registers

APB address offset	Register
0x14	USB Command*
0x18	USB Status
0x1C	USB Interrupt Enable
0x20	USB Frame Index
0x24	4G Segment Selector (Reserved)
0x28	Frame List Base Address
0x2C	Next Asynchronous List Address
0x54	Configured Flag Register
0x58 - 0x90	Port Status/Control Registers**

*Light Host Controller reset is not implemented.

**One 32-bit register for each port

*Table 1273.*Enhanced Host Controller RAM test registers

APB address offset	Register
0x100 - 0xFFF	RAM test control*
0x1000 - 0x17FF	Packet buffer**
0x1800 - 0x1FFF	Transaction buffer**

*Register is only present if *ramtest* generic is set to one. Accessible through any of the offsets specified.

**Registers are only present if *ramtest* generic is set to one.

*Table 1274.*0x100 - RAMTEST - RAM test control

31	2	1	0
RESERVED		ST	EN
0		0	0
r		w	w

*Table 1274.*0x100 - RAMTEST - RAM test control

31: 2	R (Reserved): Always reads zero.
1	ST (Start): Starts the automatic RAM test. Can only be written to '1'. Cleared by the core when test is finished.
0	EN (Enable): Enable RAM test. Need to be set to '1' in order to access the buffers.

*Table 1275.*Enhanced Host Controller PCI registers

APB address offset	Register
0x2060	PCI registers *Serial Bus Release Number Register* and *Frame Length Adjustment Register**

*Only implemented if configured to be used as a PCI device.

69.8.2 Universal host controller

The core is programmed through registers mapped into AHB I/O address space. The contents of each register is described in the *Universal Host Controller Interface (UHCI) Design Guide revision 1.1*. A register called *RAM test control* is added when the VHDL generic *ramtest* is set to one. The *RAM test control* register is not part of the UHCI interface and is described below. Also registers mapped to the packet buffer are added when RAM test facilities are implemented.

*Table 1276.*Universal Host Controller I/O registers

AHB address offset	Register
0x00	USB Command
0x02	USB Status*
0x04	USB Interrupt Enable
0x06	Frame Number
0x08	Frame List Base Address
0x0C	Start Of Frame Modify
0x10 - 0x2C	Port Status/Control**

*The HCHalted bit is implemented as Read Only and has the default value 1.

**Over Current and Over Current Change fields have been added. Each port has a 16-bit register.

*Table 1277.*Changes to USB Status register

15 … 6	5	4 … 0
UHCI compliant	HCH	UHCI compliant
	1	
	r	

15: 6	UHCI compliant
5	Host Controller Halted (HCH) - Same behaviour as specified in the UHCI specification but the field has been changed from Read/Write Clear to Read Only and is cleared when Run/Stop is set. The default value of this bit has been changed to 1.
4:0	UHCI compliant

*Table 1278.*Changes to Port Status/Control registers

15 … 12	11	10	9 … 0
UHCI compliant	OCC	OC	UHCI compliant
	0	0	
	wc	r	

15: 12	UHCI compliant

*Table 1278.*Changes to Port Status/Control registers

11	Over Current Change (OCC) - Set to 1 when Over Current (OC) toggles. Read/Write Clear.
10	Over Current Active (OC) - Set to 1 when there is an over current condition. Read Only.
9:0	UHCI compliant

Table 1279. Universal Host Controller RAM test registers

AHB address offset	Register
0x100 - 0x3FF	RAM test control*
0x400 - 0x7FF	Packet buffer**

*Register is only present if *ramtest* generic is set to one. Accessible through any of the offsets specified.

**Registers are only present if *ramtest* generic is set to one.

*Table 1280.*0x100 - RAMTEST - RAM test control

31 ... 2	1	0
RESERVED	ST	EN
*	0	0
r	w	rw

31: 2	R (Reserved): Always reads zero.
1	ST (Start): Starts the automatic RAM test. Can only be written to '1'. Cleared by the core when test is finished.
0	EN (Enable): Enable RAM test. Need to be set to '1' in order to access the buffers.

Table 1281. Universal Host Controller PCI registers

AHB address offset	Register
0x60	PCI register *Serial Bus Release Number Register**

*Only implemented if configured to be used as a PCI device.

69.9 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler), the enhanced host controller has device identifier 0x026, the universal host controller has device identifier 0x027. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

69.10 Implementation

69.10.1 Clocking and reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set. The core does not support *grlib_async_reset_enable*.

The core has two clock domains; a system clock domain and a USB clock domain. The USB clock domain always operates in either 60 MHz or 30 MHz, depending on the transceiver interface. All signals that cross a clock domain boundary are synchronized to prevent meta-stability.

The IP core has two different reset inputs, according to the two existing clock domains: the AMBA reset and the USB reset. They work independently on their respective clock domains. If reset generation/synchronization is desired, it shall be done in a higher instance, out of the IP, as this is not performed internally.

The reset input can be asserted and deasserted asynchronously or synchronously. All registers that in the system clock domain that require a reset value are synchronously reseted. It is assumed that the

reset input is held asserted until the system clock input is stable. In order to insure that no unwanted USB activity take place, a few registers in the USB clock domain are asynchronously reseted. Once the USB clock starts to toggle, all other registers in the USB domain that require a reset value will be reset as well.

Some ULPI transceivers require the data bus to be kept low by the core during transceiver reset, this behaviour is controlled by the *urstdrive* input signal.

69.10.2 RAM usage

The core maps all usage of RAM on either the *syncram_dp* component (dual port) or the *syncram_2p* component (double port), both from the technology mapping library (TECHMAP). Which component that is used can be configured with generics. The default, and recommended, configuration will use *syncram_dp*. A universal host controller requires one 256x32 *syncram_dp*, or two 256x32 *syncram_2p* for its packet buffer. The extra amount of *syncram_2p* needed comes from the fact that the packet buffer is both read and written from the AHB clock domain and the USB clock domain. It can not be guaranteed that a synchronization scheme would be fast enough and therefore one buffer for data beeing sent and one buffer for data beeing received are needed. An enhanced host controller requires one 512x32 *syncram_dp* (or two 512x32 *syncram_2p*, for the same reason discussed above) for its packet buffer and two 512x16 *syncram_dp/syncram_2p* for its transaction buffer. The transaction buffer is not doubled when using *syncram_2p*, instead synchronization and arbitration logic is added. When the core is instantiated with only one port, the enhanced host controller and universal host controller will share the packet buffer and the core only requires one 512x32 *syncram_dp* (or two 512x32 *syncram_2p*) for the packet buffer. Table 1282 below shows RAM usage for all legal configurations.

*Table 1282.*RAM usage for USB Host Controller core

Enhanced Host Controller present	Number of Universal Host Controllers	Number of ports	RAM component	RAM 256x32	RAM 512x32	RAM 512x16
No	x*	Don’t care	syncram_dp	x*	0	0
No	x*	Don’t care	syncram_2p	x**	0	0
Yes	1	1	syncram_dp	0	1	2
Yes	1	1	syncram_2p	0	2	2
Yes	x*	> 1	syncram_dp	x*	1	2
Yes	x*	> 1	syncram_2p	x**	2	2

* The number of required 256x32 *syncram_dp* equals the number of instantiated universal host controllers.

** The number of required 256x32 *syncram_2p* equals the double amount of instantiated universal host controllers.

69.10.3 ASIC implementation details

When synthesizing the core for ASIC it might be required to use DC Ultra to reach the desired performance of the AMBA interface.

69.10.4 Scan test support

The VHDL generic *scantest* enables scan test support. If the core has been implemented with scan test support it will:

- disable the internal RAM blocks when the testen and scanen signals are asserted.
- use the testoen signal as output enable signal.
- clock all registers with the clk input (i.e. not use the USB clock).
- use the testrst signal as the reset signal for those registers that are asynchronously reseted.

The testen, scanen, testrst, and testoen signals are routed via the AHB master interface.

69.11 Configuration options

Table 1283 shows the configuration options of the core (VHDL generics).

*Table 1283.*Configuration options

Generic name	Function	Allowed range	Default
ehchindex	Enhanced host controller AHB master index	0 - NAHBMST-1	0
ehcpindex	Enhanced host controller APB slave index	0 - NAPBSLV-1	0
ehcpaddr	Enhanced host controller ADDR field of the APB BAR.	0 - 16#FFF#	0
ehcpmask	Enhanced host controller MASK field of the APB BAR. Note that if the *ramtest* generic is set to 1 then the allowed range for this generic changes to 0 - 16#FE0#. If the pcidev generic is set to 1 then the allowed range for *ehcpmask* is 0 - 16#FC0#	0 - 16#FFF#	16#FFF#
ehcpirq	Enhanced host controller interrupt line	0 - NAHBIRQ-1	0
uhchindex	Universal host controller AHB master index. If the core contains more than one universal host controller the controllers will be assigned indexes from uhchindex to uhchindex+n_cc-1.	0 - NAHBMST-1	0
uhchsindex	Universal host controller AHB slave index. If the core contains more than one universal host controller the controllers will be assigned indexes from uhc_hsindex to uhchsindex+n_cc-1.	0 - NAHBSLV-n_cc	0
uhchaddr	Universal host controller ADDR field of the AHB BAR. If the core contains more than one universal host controller the controllers will be assigned the address space uhchaddr to uhchaddr + n_cc.	0 - 16#FFF#	0
uhchmask	Universal host controller MASK field of the AHB BAR. Note that if the *ramtest* generic is set to 1 then the allowed range for this generic changes to 0 - 16#FF8#	0 - 16#FFF#	16#FFF#
uhchirq	Universal host controller interrupt line. If the core contains more than one universal host controller the controller will be assigned interrupt lines uhc_hirq to uhchirq+n_cc-1.	0 - NAHBIRQ-1	0
tech	Technology for clock buffers	0 - NTECH	inferred
memtech	Memory Technology used for buffers.	0 - NTECH	inferred
nports	Number of USB ports	1 - 15	1
ehcgen	Enable enhanced host controller	0 - 1	1
uhcgen	Enable universal host controller(s)	0 - 1	1
n_cc	Number of universal host controllers. This value must be consistent with nports and n_pcc, or portroute1 and portroute2, depending on the value of the generic prr. This value must be at least 1, regardless the value of generic uhcgen.	1 - 15	1
n_pcc	Number of ports per universal host controller. This value must be consistent with n_cc and nports: nports <= (n_cc * n_pcc) < (nports + n_pcc) when Port Routing Rules is disabled. The only allowed deviation is if (nports mod n_cc) < n_pcc in which case the last universal host controller will get (nports mod n_cc) ports. This generic is not used then Port Routing Rules (prr) is enabled.	1 - 15	1

*Table 1283.*Configuration options

Generic name	Function	Allowed range	Default
prr	Port Routing Rules. Determines if the core's ports are routed to companion controller(s) with n_cc and n_pcc or with the help of portroute1 and portroute2.	0 - 1	0
portroute1	Defines part of the HCSP-PORTROUTE array	-	0
portroute2	Defines part of the HCSP-PORTROUTE array	-	0
endian_conv	Enable endian conversion. When set, all AMBA data lines are byte swapped. This generic must be set to 1 if the core is attached to a big endian bus, it must be set to 0 if the core is attached to a little endian bus.	0 - 1	1
be_regs	Arrange host controller registers according to big endian addressing. When set no endian conversion is made on the AMBA data lines connected to the host controller registers, regardless of endian_conv. Valid when endian_conv is enabled.	0 - 1	0
be_desc	Disable byte swapping of in-memory descriptors. Valid when endian_conv is enabled.	0 - 1	0
uhcblo	Universal Host Controller Buffer Limit Out. A universal host controller will start OUT bus transactions when uhcblo words of payload data has been fetched from memory. Note that if the core uses the UTMI+ 16 bit interface this generic must have a value larger than 2.	1 - 255	2
bwrd	Burst length in words. A universal host controller has a fixed, not affected by bwrd, burst length of four words when fetching transfer descriptors. See comments under section 69.2 DMA operations.	0 - 256	16
utm_type	Transceiver type: 0: UTMI+ 16 bit data bus 1: UTMI+ 8 bit data bus 2: ULPI	0 - 2	2

*Table 1283.*Configuration options

Generic name	Function	Allowed range	Default
vbusconf*	Selects configuration for USB power source and fault detection (external and internal below is from the USB transceivers point of view): ULPI transceivers: 0: ULPI transceiver generates VBUS internally and no external fault indicator present 1: External power source but no external fault indicator. Transceiver implement the optional ULPI pin DrvVbusExternal but not ExternalVbusIndicator. 2: External power source and external active high fault indicator. Transceiver implement both the optional ULPI signals DrvvbusExternal and ExternalVbusIndicator. 3: External power source and external active low fault indicator. Transceiver implement both the optional signals DrvvbusExternal and ExternalVbusIndicator. 4: External power source, but transceiver does not implement the optional ULPI signal DrvVbusExternal. Active low drvvbus output from Host Controller will be used. Don't care if ExternalVbusIndicator is implemented, not used. 5: External power source, but transceiver does not implement the optional ULPI signal DrvVbusExternal. Active high drvvbus output from Host Controller will be used. Don't care if ExternalVbusIndicator is implemented, not used. UTMI+ transceivers: 0: vbusvalid and drvvbus are both active low 1: vbusvalid is active low, drvvbus is active high 2: vbusvalid is active high, drvvbus is active low 3: vbusvalid and drvvbus are both active high	0 - 3	3
ramtest	When set each controller maps its internal buffers into the controller's register space.**	0 - 1	0
oepol	The polarity of the output enable signal for the data input/output buffers, 0 means active low and 1 means active high.	0 - 1	0
scantest	Scan test support will be included if this generic is set to 1.	0 - 1	0
memsel	Selects if dual port or double port memories should be used for the host controllers' internal buffers. Dual port memories are used if this generic is set to 0 (or MEMSEL_DUALPORT). Double port memories are used if this generic is set to 1 (or MEMSEL_DOUBLEPORT). It is strongly recommended to use dual port memories in the host controllers. Double port memories should only be used on technologies that lack support for dual port memories or where the area overhead for dual port memories preventively large.***	0 - 1	0
pcidev	This generic should be set to one if the core is to be used as a PCI device. If set to 1 the core will hold its interrupt signal(s) high until cleared by software. Also a few PCI registers will be added. See section 69.7 and 69.8 for details on the registers. Note that if this generic is set to 1 then the allowed range for *ehcpmask* changes to 0 - 16#FC0#.	0 - 1	0

*Table 1283.*Configuration options

Generic name	Function	Allowed range	Default

*see section 69.6 Transceiver support for more information

**see section 69.2.5 RAM test facilities for more information

***see section 69.10.2 RAM usage for more information

69.12 Signal descriptions

Table 1284 shows the interface signals of the core (VHDL ports).

*Table 1284.*Signal descriptions

Signal name	Field	Type	Function	Active
CLK	N/A	Input	AMBA clock	-
UCLK	N/A	Input	USB clock	-
RST	N/A	Input	AMBA reset	Low
URST	N/A	Input	USB reset	Low
APBI	*	Input	APB slave input signals	-
EHC_APBO	*	Output	APB slave output signals	-
AHBMI	*	Input	AHB master input signals	-
AHBSI	*	Input	AHB slave input signals	-
EHC_AHBMO	*	Output	AHB master output signals.	-
UHC_AHBMO[]	*	Output	AHB master output vector.	
UHC_AHBSO[]	*	Output	AHB slave output vector.	-
O[]	xcvrselect[1:0]	Output	UTMI+	-
	termselect	Output	UTMI+	-
	suspendm	Output	UTMI+	Low
	opmode[1:0]	Output	UTMI+	-
	txvalid	Output	UTMI+	High
	dataout[15:0]	Output	UTMI+/ULPI. Bits 15:8 are only used in 16-bit UTMI+ mode.	-
	txvalidh	Output	UTMI+ 16-bit	High
	stp	Output	ULPI	High
	reset	Output	Transceiver reset signal. Asserted asynchronously and deasserted synchrnously to the USB clock.	**
	oen	Output	Data bus direction control for ULPI and bi-directional UTMI+ interfaces.	***
	databus16_8	Output	UTMI+ Constant high for 16-bit interface, constant low for 8-bit interface.	-
	dppulldown	Output	UTMI+ Constant high.	High
	dmpulldown	Output	UTMI+ Constant high.	High
	idpullup	Output	UTMI+ Constant low.	High
	drvvbus	Output	UTMI+/ULPI	***
	dischrgvbus	Output	UTMI+ Constant low.	High
	chrgvbus	Output	UTMI+ Constant low.	High
	txbitstuffenable	Output	UTMI+ Constant low.	High
	txbitstuffenableh	Output	UTMI+ Constant low.	High
	fslsserialmode	Output	UTMI+ Constant low.	High

*Table 1284.*Signal descriptions

Signal name	Field	Type	Function	Active
	tx_enable_n	Output	UTMI+ Constant high.	High
	tx_dat	Output	UTMI+ Constant low.	High
	tx_se0	Output	UTMI+ Constant low.	High
I[]	linestate[1:0]	Input	UTMI+	-
	txready	Input	UTMI+	High
	rxvalid	Input	UTMI+	High
	rxactive	Input	UTMI+	High
	rxerror	Input	UTMI+	High
	vbusvalid	Input	UTMI+	***
	datain[15:0]	Input	UTMI+/ULPI. Bits 15:8 are only used in 16-bit UTMI+ interface.	-
	rxvalidh	Input	UTMI+ 16-bit	High
	hostdisconnect	Input	UTMI+	High
	nxt	Input	ULPI	High
	dir	Input	ULPI	-
	urstdrive	Input	This input determines if the cores should drive the transceiver data lines low during USB transceiver reset, even if the dir input is High. This is needed for some transceivers, such as the NXP ISP1504. When this input is low the direction of the transceiver data lines are exclusively controlled by the dir signal from the transceiver. When this input is high the core will drive the data lines low during transceiver reset. Only applicable for ULPI transceivers.	High

* See GRLIB IP Library User's Manual.

** Depends on transceiver interface. Active high for UTMI+ and active low for ULPI.

*** Implementation dependent.

69.13 Signal definitions and reset values

The signals and their reset values are described in table 1285.

*Table 1285.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
xcvrselect[1:0]	Output	UTMI+	-	-
termselect	Output	UTMI+	-	-
suspendm	Output	UTMI+	Logical 0	Logical 1
opmode[1:0]	Output	UTMI+	-	-
txvalid	Output	UTMI+	Logical 1	Logical 0
dataout[15:0]	Output	UTMI+/ULPI. Bits 15:8 are only used in 16-bit UTMI+ mode.	-	-
txvalidh	Output	UTMI+ 16-bit	Logical 1	Logical 0
stp	Output	ULPI	Logical 1	Logical 0
reset	Output	Transceiver reset signal. Set asynchronously and cleared synchrnously to the USB clock.	*	*
oen	Output	Data bus direction control for ULPI and bi-directional UTMI+ interfaces.		

*Table 1285.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
databus16_8	Output	UTMI+ Constant high for 16-bit interface, constant low for 8-bit interface.	-	**
dppulldown	Output	UTMI+ Constant high.	Logical 1	Logical 1
dmpulldown	Output	UTMI+ Constant high.	Logical 1	Logical 1
idpullup	Output	UTMI+ Constant low.	Logical 1	Logical 0
drvvbus	Output	UTMI+	**	**
dischrgvbus	Output	UTMI+ Constant low.	Logical 1	Logical 0
chrgvbus	Output	UTMI+ Constant low.	Logical 1	Logical 0
txbitstuffenable	Output	UTMI+ Constant low.	Logical 1	Logical 0
txbitstuffenableh	Output	UTMI+ Constant low.	Logical 1	Logical 0
fslsserialmode	Output	UTMI+ Constant low.	Logical 1	Logical 0
tx_enable_n	Output	UTMI+ Constant low.	Logical 1	Logical 0
tx_dat	Output	UTMI+ Constant low.	Logical 1	Logical 0
tx_se0	Output	UTMI+ Constant low.	Logical 1	Logical 0
linestate[1:0]	Input	UTMI+	-	-
txready	Input	UTMI+	Logical 1	-
rxvalid	Input	UTMI+	Logical 1	-
rxactive	Input	UTMI+	Logical 1	-
rxerror	Input	UTMI+	Logical 1	-
vbusvalid	Input	UTMI+	***	-
datin[15:0]	Input	UTMI+/ULPI. Bits 15:8 are only used in 16-bit UTMI+ mode.	-	-
rxvalidh	Input	UTMI+ 16 bit interface	Logical 1	-
hostdisconnect	Input	UTMI+	Logical 1	-
nxt	Input	ULPI	Logical 1	-
dir	Input	ULPI	-	-

* Depends on transceiver interface. UTMI+ is active high, ULPI is active low.

** Implementation dependent

69.14 Library dependencies

Table 1286 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1286.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	GRUSB	Signals, component	Component declaration, USB signals

69.15 Instantiation

This example shows how the core can be instantiated.

```
library ieee, grlib, gaisler;
use ieee.std_logic_1164.all;
use grlib.amba.all;
use gaisler.grusb.all;

-- USB Host controller with 2 ports. One enhanced
```

```
-- host controller and two universal host controllers. Note that not all generics are set
-- in this example, many are kept at their defaulr values.

entity usbhc_ex is
  generic (
    tech    => tech;
    memtech => memtech;
    padtech => padtech);
  port (
    clk : in std_ulogic;
    rstn : in std_ulogic;

    -- USBHC signals
    usbh_clkin     : in std_ulogic;
    usbh_rstin     : in std_ulogic;
    usbh_d         : inout std_logic_vector(15 downto 0);
    usbh_reset     : out std_logic_vector(1 downto 0);
    usbh_nxt       : in std_logic_vector(1 downto 0);
    usbh_stp       : out std_logic_vector(1 downto 0);
    usbh_dir       : in std_logic_vector(1 downto 0)
    );
end;

architecture rtl of usbhc_ex is

  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);
  signal ahbsi : ahb_slv_in_type;
  signal ahbso : ahb_slv_out_vector := (others => ahbs_none);

  -- USBHC signals
  signal usbhci : grusb_in_vector(1 downto 0);
  signal usbhco : grusb_out_vector(1 downto 0);
  signal uhclk : std_ulogic;
  signal uhrstn : std_ulogic;

begin

  -- AMBA Components are instantiated here
  ...

  -- Instantiate pads, one iteration for each port
  multi_pads: for i in 0 to 1 generate
    usbh_d_pad: iopadv
      generic map(tech => padtech, width => 8)
      port map (usbh_d((i*8+7) downto (i*8)),
                usbhco(i).dataout(7 downto 0), usbhco(i).oen,
                usbhci(i).datain(7 downto 0));
    usbh_nxt_pad : inpad generic map (tech => padtech)
      port map (usbh_nxt(i),usbhci(i).nxt);
    usbh_dir_pad : inpad generic map (tech => padtech)
      port map (usbh_dir(i),usbhci(i).dir);
    usbh_reset_pad : outpad generic map (tech => padtech)
      port map (usbh_reset(i),usbhco(i).reset);
    usbh_stp_pad : outpad generic map (tech => padtech)
      port map (usbh_stp(i),usbhco(i).stp);

    -- No need to drive ULPI data bus during USB reset
    usbhci(i).urstdrive <= '0';
  end generate multi_pads;

  usbh_clkin_pad : clkpad:
    generic map (tech => padtech)
    port map(usbh_clkin, uhclk);

  usbh_rstin_pad : inpad:
    generic map (tech => padtech)
    port map(usbh_rstin, uhrstn);
```

```
  usbhostcontroller0: grusbhc
    generic map (
      ehchindex => 5,
      ehcpindex => 14,
      ehcpaddr => 14,
      ehcpirq => 9,
      ehcpmask => 16#fff#,
      uhchindex => 6,
      uhchsindex => 3,
      uhchaddr => 16#A00#,
      uhchmask => 16#fff#,
      uhchirq => 10,
      tech => tech,
      memtech => memtech,
      nports => 2,
      ehcgen => 1,
      uhcgen => 1,
      n_cc => 2,
      n_pcc => 1,
      endian_conv => 1,
      utm_type => 2,
      vbusconf => 3)
    port map (
      clk => clk,
      uclk => uhclk,
      rst => rstn,
      urst => uhrstn,
      apbi => apbi,
      ehc_apbo => apbo(14),
      ahbmi => ahbmi,
      ahbsi => ahbsi,
      ehc_ahbmo => ahbmo(5),
      uhc_ahbmo => ahbmo(7 downto 6),
      uhc_ahbso => ahbso(4 downto 3),
      o => usbhco,
      i => usbhci);
end;
```

70 GRVERSION - Version and Revision information register

70.1 Overview

The GRVERSION provides a register containing a 16 bit version field and a 16 bit revision field. The values for the two fields are taken from two corresponding VHDL generics. The register is available via the AMBA APB bus.

70.2 Registers

The core is programmed through registers mapped into APB address space.

*Table 1287.*GRVERSION registers

APB address offset	Register
0x00	Configuration Register

70.2.1 Configuration Register

*Table 1288.*0x00 - CONFIG - Configuration Register

31 16	15 0
VERSION	REVISION
*	*
r	r

31-16: VERSION Version number
15- 0: REVISIONRevision number

70.3 Vendor and device identifiers

The module has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x03A. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

70.4 Implementation

70.4.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

70.5 Configuration options

Table 1289 shows the configuration options of the core (VHDL generics).

*Table 1289.*Configuration options

Generic name	Function	Allowed range	Default
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	Addr field of the APB bar.	0 - 16#FFF#	0
pmask	Mask field of the APB bar.	0 - 16#FFF#	16#FFF#
versionnr	Version number	0 - 2^16-1	0
revisionnr	Revision number	0 - 2^16-1	0

70.6 Signal descriptions

Table 1290 shows the interface signals of the core (VHDL ports).

*Table 1290.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-

* see GRLIB IP Library User's Manual

70.7 Library dependencies

Table 1291 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1291.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	MISC	Component	Component declaration

71 I2C2AHB - I^{2}C to AHB bridge

71.1 Overview

The I^{2}C slave to AHB bridge is an I^{2}C slave that provides a link between the I^{2}C bus and AMBA AHB. The core is compatible with the Philips I^{2}C standard and external pull-up resistors must be supplied for both bus lines.

On the I^{2}C bus the slave acts as an I^{2}C memory device where accesses to the slave are translated to AMBA accesses. The core can translate I^{2}C accesses to AMBA byte, halfword or word accesses. The core makes use of I^{2}C clock stretching but can also be configured to use a special mode without clock stretching in order to support systems where master or physical layer limitations prevent stretching of the I^{2}C clock period.

GRLIB also contains another I^{2}C slave core, without an AHB interface, where the transfer of each individual byte is controlled by software via an APB interface, see the I2CSLV core documentation for more information.

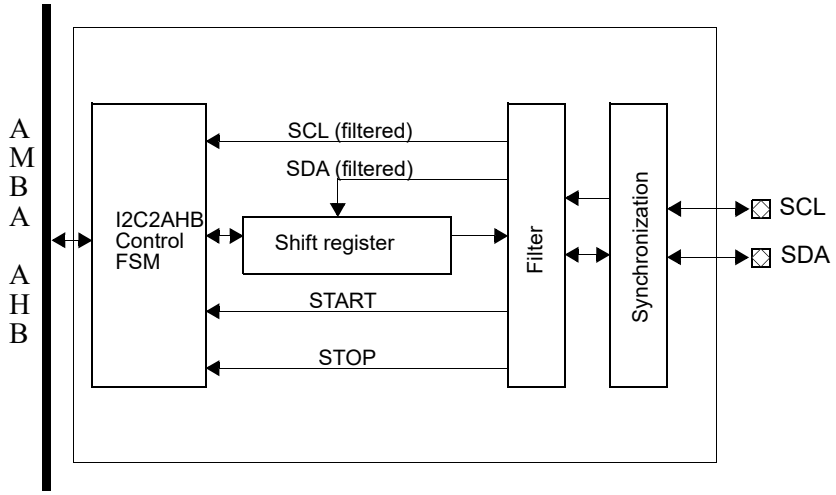


Figure 205. Block diagram, optional APB interface not shown

71.2 Operation

71.2.1 Transmission protocol

The I^{2}C-bus is a simple 2-wire serial multi-master bus with collision detection and arbitration. The bus consists of a serial data line (SDA) and a serial clock line (SCL). The I^{2}C standard defines three transmission speeds; Standard (100 kb/s), Fast (400 kb/s) and High speed (3.4 Mb/s).

A transfer on the I^{2}C-bus begins with a START condition. A START condition is defined as a high to low transition of the SDA line while SCL is high. Transfers end with a STOP condition, defined as a low to high transition of the SDA line while SCL is high. These conditions are always generated by a master. The bus is considered to be busy after the START condition and is free after a certain amount of time following a STOP condition. The bus free time required between a STOP and a START condition is defined in the I^{2}C-bus specification and is dependent on the bus bit rate.

Figure 206 shows a data transfer taking place over the I^{2}C-bus. The master first generates a START condition and then transmits the 7-bit slave address. The bit following the slave address is the R/$\overline{W}$ bit which determines the direction of the data transfer. In this case the R/$\overline{W}$ bit is zero indicating a write operation. After the master has transmitted the address and the R/$\overline{W}$ bit it releases the SDA line. The receiver pulls the SDA line low to acknowledge the transfer. If the receiver does not acknowledge the

transfer, the master may generate a STOP condition to abort the transfer or start a new transfer by generating a repeated START condition.

After the address has been acknowledged the master transmits the data byte. If the R/$\overline{W}$ bit had been set to '1' the master would have acted as a receiver during this phase of the transfer. After the data byte has been transferred the receiver acknowledges the byte and the master generates a STOP condition to complete the transfer.

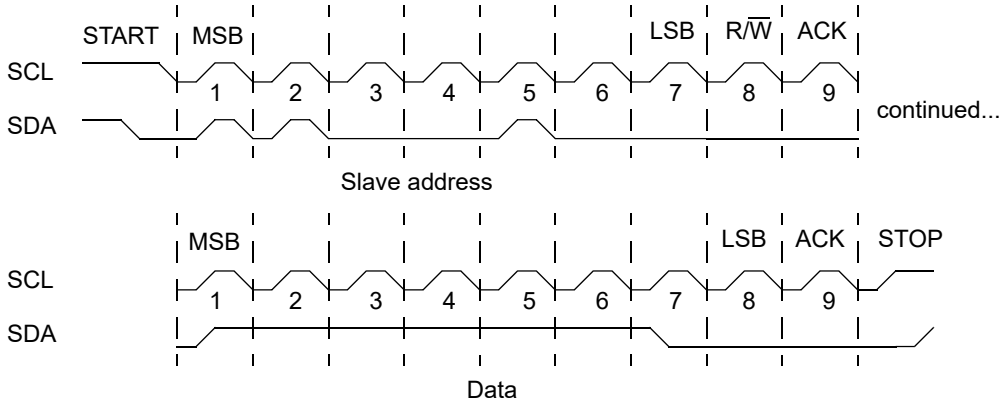


Figure 206. Complete I^{2}C data transfer

If the data bit rate is too high for a slave device or if the slave needs time to process data, it may stretch the clock period by keeping SCL low after the master has driven SCL low. Clock stretching is a configurable parameter of the core (see sections 71.2.4 and 71.2.6).

71.2.2 Slave addressing

The core's I^{2}C addresses are set with VHDL generics at implementation time. If the core has been implemented with the optional APB interface, then the I^{2}C addresses can be changed via registers available via APB.

The core responds to two addresses on the I^{2}C bus. Accesses to the I2C memory address are translated to AMBA AHB accesses and accesses to the I^{2}C configuration address access the core's configuration register.

71.2.3 System clock requirements and sampling

The core samples the incoming I^{2}C SCL clock and does not introduce any additional clock domains into the system. Both the SCL and SDA lines first pass through two stage synchronizers and are then filtered with a low pass filter consisting of four registers.

START and STOP conditions are detected if the SDA line, while SCL is high, is at one value for two system clock cycles, toggles and keeps the new level for two system clock cycles.

The synchronizers and filters constrain the minimum system frequency. The core requires the SCL signal to be stable for at least four system clock cycles before the core accepts the SCL value as the new clock value. The core's reaction to transitions will be additionally delayed since both lines are taken through two-stage synchronizers before they are filtered. Therefore it takes the core over eight system clock cycles to discover a transition on SCL.

71.2.4 Configuration register access

The I^{2}C configuration register is accessed via a separate I^{2}C address (I^{2}C configuration address). The configuration register has the layout shown in table 1292.

*Table 1292.*I2C2AHB configuration register

7	6	5	4	3	2	1	0
Reserved		PROT	MEXC	DMAACT	NACK	HSIZE	

7:6	Reserved, always zero (read only)
5	Memory protection triggered (PROT) - '1' if last AHB access was outside the allowed memory area. Updated after each AMBA access (read only)
4	Memory exception (MEXC) - '1' if core receives AMBA ERROR response. Updated after each AMBA access (read only)
3	DMA active (DMAACT) - '1' if core is currently performing a DMA operation.
2	NACK (NACK) - Use NACK instead of clock stretching. See documentation in section 71.2.6.
1:0	AMBA access size (HSIZE) - Controls the access size that the core will use for AMBA accesses. 0: byte, 1: halfword, 2: word. HSIZE = "11" is illegal.

Reset value: 0x02

Reads from the I^{2}C configuration address will return the current value of the configuration register. Writes to the I^{2}C configuration address will affect the writable bits in the configuration register.

71.2.5 AHB accesses

All AMBA accesses are done in big endian format. The first byte sent to or from the slave is the most significant byte.

To write a word on the AHB bus the following I2C bus sequence should be performed:

1. Generate START condition
2. Send I2C memory address with the R/$\overline{W}$ bit set to '0'.
3. Send four byte AMBA address, the most significant byte is transferred first
4. Send four bytes to write to the specified address
5. If more than four consecutive bytes should be written, continue to send additional bytes, otherwise go to 6.
6. Generate STOP condition

To perform a read access on the AHB bus, the following I2C bus sequence should be performed:

1. Generate START condition
2. Send I2C memory address with the R/$\overline{W}$ bit set to '0'.
3. Send four byte AMBA address, the most significant byte is transferred first
4. Generate (repeated) START condition
5. Send I2C memory address with the R/$\overline{W}$ bit set to '1'.
6. Read the required number of bytes and NACK the last byte
7. Generate stop condition

During consecutive read or write operations, the core will automatically increment the address. The access size (byte, halfword or word) used on AHB is set via the HSIZE field in the I2C2AHB configuration register.

The core always respects the access size specified via the HSIZE field. If a write operation writes fewer bytes than what is required to do an access of the specified HSIZE then the write data will be dropped, no access will be made on AHB. If a read operation reads fewer bytes than what is specified by HSIZE then the remaining read data will be dropped at a START or STOP condition. This means,

for instance, that if HSIZE is “10” (word) the core will perform two word accesses if a master reads one byte, generates a repeated start condition, and reads one more byte. Between these two accesses the address will have been automatically increased, so the fist access will be to address *n* and the second to address *n+4*.

The automatic address increment means that it is possible to write data and then immediately read the data located at the next memory position. As an example, the following sequence will write a word to address 0 and then read a word from address 4:

1. Generate START condition
2. Send I2C memory address with the R/$\overline{W}$ bit set to ‘0’.
3. Send four byte AMBA address, all zero.
4. Send four bytes to write to the specified address
5. Generate (repeated) START condition
6. Send I2C memory address with the R/$\overline{W}$ bit set to ‘1’.
7. Read the required number of bytes and lack the last byte
8. Generate stop condition

The core will not mask any address bits. Therefore it is important that the I^2C master respects AMBA rules when performing halfword and word accesses. A halfword access must be aligned on a two byte address boundary (least significant bit of address must be zero) and a word access must be aligned on a four byte boundary (two least significant address bits must be zero).

The core can be configured to generate interrupt requests when an AHB access is performed if the core is implemented with the APB register interface, see the APB register documentation for details.

71.2.6 Clock stretching or NACK mode

The core has two main modes of operation for AMBA accesses. In one mode the core will use clock stretching while performing an AHB operation and in the other mode the core will not acknowledge bytes (abort the I^2C access) when the core is busy. Clock stretching is the preferred mode of operation. The NACK mode can be used in scenarios where the I^2C master or physical layer does not support clock stretching. The mode to use is selected via the NACK field in the I^2C configuration register.

When clock stretching is enabled (NACK field is ‘0’) the core will stretch the clock when the slave is accessed (via the I2C memory address) and the slave is busy processing a transfer. Clock stretching is also used when a data byte has been transmitted, or received, to keep SCL low until a DMA operation has completed. In the transmit (AMBA read) case SCL is kept low before the rising edge of the first byte. In the receive case (AMBA write) the ACK cycle for the previous byte is stretched.

When clock stretching is disabled (NACK field is ‘1’) the core will never stretch the SCL line. If the core is busy performing DMA when it is addressed, the address will not be acknowledged. If the core performs consecutive writes and the first write operation has not finished the core will now acknowledge the written byte. If the core performs a read operation and the read DMA operation has not finished when the core is supposed to deliver data then the core will go to its idle state and not respond to more accesses until a START condition is generated on the bus. This last part means that the NACK mode is practically unusable in systems where the AMBA access can take longer than one I^2C clock period. This can be compensated by using a very slow I^2C clock.

71.2.7 Memory protection

The core is configured at implementation time to only allow accesses to a specified AHB address range (which can be the full 4 GiB AMBA address range). If the core has been implemented with the optional APB register interface then the address range is soft configurable and the reset value is specified with VHDL generics.

The VHDL generics *ahbaddrh* and *ahbaddrl* define the base address for the allowed area. The VHDL generics *ahbmaskh* and *ahbmaskl* define the size of the area. The generics are used to assign the memory protection area's address and mask in the following way:

Protection address, bits 31:16 (*protaddr[31:16]*): ahbaddrh
Protection address, bits 15:0 (*protaddr[15:0]*): ahbaddrl
Protection mask, bits 31:16 (*protmask[31:16]*): ahbmaskh
Protection mask, bits 15:0 (*protmask[15:0]*): ahbmaskl

Before the core performs an AMBA access it will perform the check:

(((incoming address) xor (protaddr)) and protmask) /= 0x00000000

If the above expression is true (one or several bits in the incoming address differ from the protection address, and the corresponding mask bits are set to '1') then the access is inhibited. As an example, assume that *protaddr* is 0xA0000000 and *protmask* is 0xF0000000. Since *protmask* only has ones in the most significant nibble, the check above can only be triggered for these bits. The address range of allowed accessed will thus be 0xA0000000 - 0xAFFFFFFF.

The memory protection check is performed at the time when the core is to perform the AHB access. It is possible to start a write operation and transmit an illegal address to the core without any errors. If additional bytes are transmitted (so that a HSIZE access can be made) the core will NACK the byte that triggers the AHB access.

For a read operation the core will NACK the I^2C memory address of the first AHB access of the read in case the access would be to restricted memory. If consecutive bytes are read from the core and one of the later accesses lead to restricted memory being accessed, then the core will abort all operations and enter its idle state. In this case junk data will be returned and there is no way for the core to alert the master that memory protection has been triggered.

The core will set the configuration register bit PROT if an access is attempted outside the allowed address range. This bit is updated on each AHB access and will be cleared by an access inside the allowed range. Note that the (optional) APB status register has a PROT field with a slightly different behavior.

71.3 Registers

The core can optionally be implemented with an APB interface that provides registers mapped into APB address space.

Table 1293.I^2C slave registers

APB address offset	Register
0x00	Control register
0x04	Status register
0x08	Protection address register
0x0C	Protection mask register
0x10	I2C slave memory address register
0x14	I2C slave configuration address register

71.3.1 Control Register

*Table 1294.*0x0 - CTRL - Control register

31	2	1	0
RESERVED		IRQEN	EN
0		0	*
r		rw	rw

31 : 2 RESERVED

1 Interrupt enable (IRQEN) - When this bit is set to '1' the core will generate an interrupt each time the DMA field in the status register transitions from '0' to '1'.

0 Core enable (EN) - When this bit is set to '1' the core is enabled and will respond to I2C accesses. Otherwise the core will not react to I2C traffic.

Reset value: Implementation dependent

71.3.2 Status Register

*Table 1295.*0x04 - STAT - Status register

31	3	2	1	0
RESERVED		PROT	WR	DMA

31 : 3 RESERVED

2 Protection triggered (PROT) - Set to '1' if an access has triggered the memory protection. This bit will remain set until cleared by writing '1' to this position. Note that the other fields in this register will be updated on each AHB access while the PROT bit will remain at '1' once set.

1 Write access (WR) - Last AHB access performed was a write access. This bit is read only.

0 Direct Memory Access (DMA) - This bit gets set to '1' each time the core attempts to perform an AHB access. By setting the IRQEN field in the control register this condition can generate an interrupt. This bit can be cleared by software by writing '1' to this position.

71.3.3 Protection Address Register

*Table 1296.*0x08 - PADDR - Protection address register

31	0
PROTADDR	
*	
rw	

31 : 0 Protection address (PROTADDR) - Defines the base address for the memory area where the core is allowed to make accesses.

71.3.4 Protection Mask Register

*Table 1297.*0x0C - PMASK - Protection mask register

31	0
PROTMASK	
*	
rw	

31 : 0 Protection mask (PROTMASK) - Selects which bits in the Protection address register that are used to define the protected memory area.

71.3.5 I2C Slave Memory Address Register

Table 1298. 0x10 - SLVADDR - I2C slave memory address register

31 7	6 0
RESERVED	I2CSLVADDR
0	*
r	rw

31 : 7 RESERVED

6 : 0 I2C slave memory address (I2CSLVADDR) - Address that slave responds to for AHB memory accesses

71.3.6 I2C Slave Configuration Address Register

*Table 1299.*0x14 - SLVCFG - I2C slave configuration address register

31 7	6 0
RESERVED	I2CCFGADDR
0	*
r	rw

31 : 7 RESERVED

6 : 0 I2C slave configuration address (I2CCFGADDR) - Address that slave responds to for configuration register accesses.

71.4 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x00B. For a description of vendor and device identifiers see the GRLIB IP Library User's Manual.

71.5 Implementation

71.5.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

71.6 Configuration options

Table 1300 shows the configuration options of the core (VHDL generics). Two different top level entites for the core is available. One with the optional APB interface (i2c2ahb_apb) and one without the APB interface (i2c2ahb). The entity without the APB interface has fewer generics as indicated in the table below.

*Table 1300.*Configuration options

Generic name	Function	Allowed range	Default
hindex	AHB master index	0 - NAHBMST	0
ahbaddrh	Defines bits 31:16 of the address used for the memory protection area	0 - 16#FFFF#	0
ahbaddrl	Defines bits 15:0 of the address used for the memory protection area	0 - 16#FFFF#	0
ahbmaskh	Defines bits 31:16 of the mask used for the memory protection area	0 - 16#FFFF#	0
ahbmaskl	Defines bits 15:0 of the mask used for the memory protection area	0 - 16#FFFF#	0

*Table 1300.*Configuration options

Generic name	Function	Allowed range	Default
resen	Reset value for core enable bit (only available on the i2c2ahb_apb entity).	0 - 1	0
pindex	APB slave index (only available on the i2c2ahb_apb entity).	0 - NAPBSLV-1	0
paddr	ADDR field of the APB BAR (only available on the i2c2ahb_apb entity).	0 - 16#FFF#	0
pmask	MASK field of the APB BAR (only available on the i2c2ahb_apb entity).	0 - 16#FFF#	16#FFF#
pirq	Interrupt line driven by APB interface (only available on the i2c2ahb_apb entity).	0 - NAHBIRQ-1	0
i2caddr	The slave's (initial) I^2C address. i2caddr specified the core's I2C memory address and (i2caddr+1) will be the cores I2C configuration address.	0 - 126	0
oepol	Output enable polarity	0 - 1	0
filter	Low-pass filter length. This generic should specify, in number of system clock cycles plus one, the time of the shortest pulse on the I2C bus to be registered as a valid value. For instance, to disregard any pulse that is 50 ns or shorter in a system with a system frequency of 54 MHz this generic should be set to: ((pulse time) / (clock period)) + 1 = (50 ns) / ((1/(54 MHz)) + 1 = 3.7 The value from this calculation should always be rounded up. In other words an appropriate filter length for a 54 MHz system is 4.	2 - 512	2

71.7 Signal descriptions

Table 1301 shows the interface signals of the core (VHDL ports).

*Table 1301.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
AHBI	*	Input	AHB master input signals	-
AHBO	*	Output	AHB master output signals	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
I2CI	SCL	Input	I^2C clock line input	-
	SDA	Input	I^2C data line input	-
I2CO	SCL	Output	I^2C clock line output	-
	SCLOEN	Output	I^2C clock line output enable	Low**
	SDA	Output	I^2C data line output	-
	SDAOEN	Output	I^2C data line output enable	Low**
	ENABLE	Output	High when core is enabled, low otherwise.	High

* see GRLIB IP Library User's Manual
** depends on value of OEPOL VHDL generic.

71.8 Signal definitions and reset values

The signals and their reset values are described in table 1302.

*Table 1302.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
scl	InputOutput	I^2C clock line	-	Hi-Z
sda	InputOutput	I^2C data line	-	Hi-Z

71.9 Library dependencies

Table 1303 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1303.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	I2C	Component, signals	Component declaration, I2C signal definitions

71.10 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib, techmap;
use grlib.amba.all;
use techmap.gencomp.all;

library gaisler;
use gaisler.misc.all;

entity i2c2ahb_ex is
  port (
    clk  : in std_ulogic;
    rstn : in std_ulogic;

    -- I2C signals
    iic_scl : inout std_ulogic;
    iic_sda : inout std_ulogic
    );
end;

architecture rtl of i2c2ahb_ex is

  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector;
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector;

  -- I2C signals
  signal i2ci : i2c_in_type;
  signal i2co : i2c_out_type;
begin

  -- AMBA Components are instantiated here
  ...

  -- NOTE: There are also wrappers for the top-level entities that do not make use of VHDL
  --       records. These wrappers are called i2c2ahb_apb_gen and i2c2ahb_gen.
```

```
  -- I2C-slave, with APB interface
  i2c2ahb0 : i2c2ahb_apb
    generic map (
      hindex   => 1,
      ahbaddrh => ahbaddrh,
      ahbaddrl => ahbaddrl,
      ahbmaskh => ahbmaskh,
      ahbmaskl => ahbmaskl,
      resen    => 1,
      pindex   => 1,
      paddr    => 1,
      pmask    => 16#fff#,
      i2caddr  => i2caddr,
      oepol    => 0,
      filter   => I2C_FILTER)
    port map (rstn, clk, ahbmi, ahbmo(1), apbi, apbo(1),
              i2ci, i2co);
  scl_pad : iopad generic map (tech => padtech)
    port map (iic_scl, i2co.scl, i2co.scloen, i2ci.scl);
  sda_pad : iopad generic map (tech => padtech)
    port map (iic_sda, i2co.sda, i2co.sdaoen, i2ci.sda);
end;
```

72 I2CMST - I²C-master

72.1 Overview

The I²C-master core is a modified version of the OpenCores I²C-Master with an AMBA APB interface. The core is compatible with Philips I²C standard and supports 7- and 10-bit addressing. Standard-mode (100 kb/s) and Fast-mode (400 kb/s) operation are supported directly. External pull-up resistors must be supplied for both bus lines.

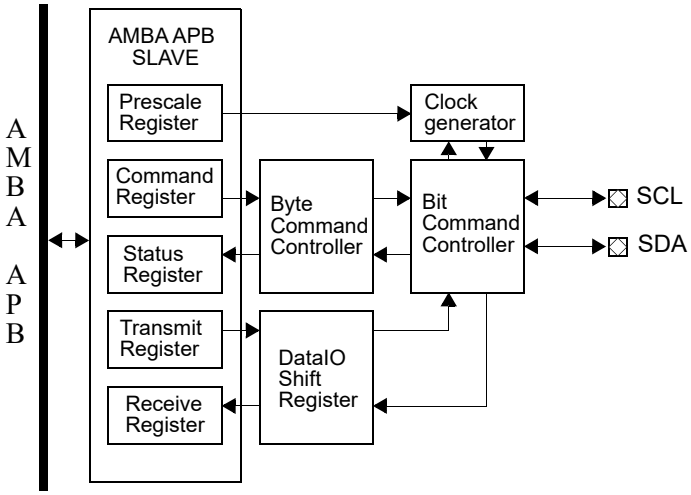


Figure 207. Block diagram

72.2 Operation

72.2.1 Transmission protocol

The I²C-bus is a simple 2-wire serial multi-master bus with collision detection and arbitration. The bus consists of a serial data line (SDA) and a serial clock line (SCL). The I²C standard defines three transmission speeds; Standard (100 kb/s), Fast (400 kb/s) and High speed (3.4 Mb/s).

A transfer on the I²C-bus begins with a START condition. A START condition is defined as a high to low transition of the SDA line while SCL is high. Transfers end with a STOP condition, defined as a low to high transition of the SDA line while SCL is high. These conditions are always generated by a master. The bus is considered to be busy after the START condition and is free after a certain amount of time following a STOP condition. The bus free time required between a STOP and a START condition is defined in the I²C-bus specification and is dependent on the bus bit rate.

Figure 208 shows a data transfer taking place over the I²C-bus. The master first generates a START condition and then transmits the 7-bit slave address. The bit following the slave address is the R/$\overline{W}$ bit which determines the direction of the data transfer. In this case the R/$\overline{W}$ bit is zero indicating a write operation. After the master has transmitted the address and the R/$\overline{W}$ bit it releases the SDA line. The receiver pulls the SDA line low to acknowledge the transfer. If the receiver does not acknowledge the transfer, the master may generate a STOP condition to abort the transfer or start a new transfer by generating a repeated START condition.

After the first byte has been acknowledged the master transmits the data byte. If the R/$\overline{W}$ bit had been set to ‘1’ the master would have acted as a receiver during this phase of the transfer. After the data byte has been transferred the receiver acknowledges the byte and the master generates a STOP condition to complete the transfer. Section 72.2.3 contains three more example transfers from the perspective of a software driver.

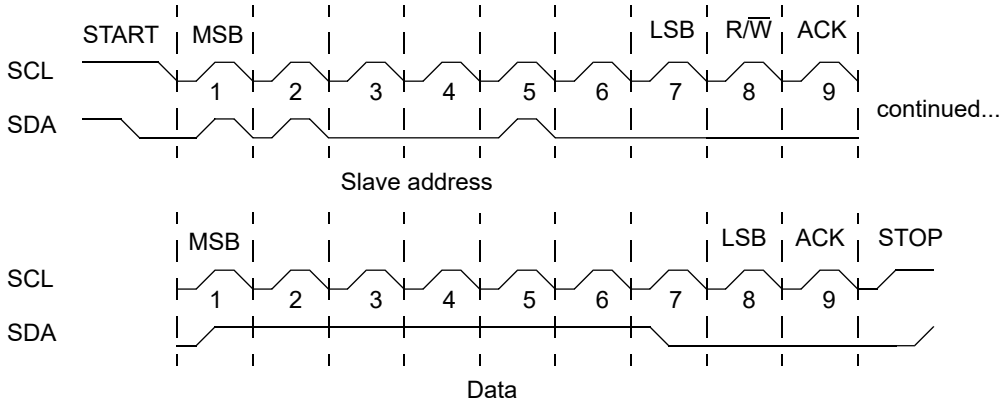


Figure 208. Complete I^{2}C data transfer

If the data bitrate is too high for a slave device, it may stretch the clock period by keeping SCL low after the master has driven SCL low.

72.2.2 Clock generation

The core uses the prescale register to determine the frequency of the SCL clock line and of the 5*SCL clock that the core uses internally. To calculate the prescale value use the formula:

$$Prescale = \frac{AMBAclockfrequency}{5 \cdot SCLfrequency} - 1$$

The *SCLfrequency* is 100 kHz for Standard-mode operation (100 kb/s) and 400 kHz for Fast mode operation. To use the core in Standard-mode in a system with a 60 MHz clock driving the AMBA bus the required prescale value is:

$$Prescale = \frac{60Mhz}{5 \cdot 100kHz} - 1 = 119 = 0x77$$

Note that the prescale register should only be changed when the core is disabled. The minimum recommended prescale value is 3 due to synchronization issues. This limits the minimum system frequency to 2 MHz for operation in Standard-mode (to be able to generate a 100 kHz SCL clock). However, a system frequency of 2 MHz will not allow the implementation fulfill the 100 ns minimum requirement for data setup time (required for Fast-mode operation). For compatibility with the I^{2}C Specification, in terms of minimum required data setup time, the minimum allowed system frequency is 20 MHz due to synchronization issues. If the core is run at lower system frequencies, care should be taken so that data from devices is stable on the bus one system clock period before the rising edge of SCL.

72.2.3 Software operational model

The core is initialized by writing an appropriate value to the clock prescale register and then setting the enable (EN) bit in the control register. Interrupts are enabled via the interrupt enable (IEN) bit in the control register.

To write a byte to a slave the I^{2}C-master must generate a START condition and send the slave address with the R/$\overline{W}$ bit set to ‘0’. After the slave has acknowledged the address, the master transmits the

data, waits for an acknowledge and generates a STOP condition. The sequence below instructs the core to perform a write:

1. Left-shift the I^{2}C-device address one position and write the result to the transmit register. The least significant bit of the transmit register (R/$\overline{W}$) is set to '0'.

2. Generate START condition and send contents of transmit register by setting the STA and WR bits in the command register.

3. Wait for interrupt, or for TIP bit in the status register to go low.

4. Read RxACK bit in status register. If RxACK is low the slave has acknowledged the transfer, proceed to step 5. If RxACK is set the device did not acknowledge the transfer, go to step 1.

5. Write the slave-data to the transmit register.

6. Send the data to the slave and generate a stop condition by setting STO and WR in the command register.

7. Wait for interrupt, or for TIP bit in the status register to go low.

8. Verify that the slave has acknowledged the data by reading the RxACK bit in the status register. RxACK should not be set.

To read a byte from an I^{2}C-connected memory much of the sequence above is repeated. The data written in this case is the memory location on the I^{2}C slave. After the address has been written the master generates a repeated START condition and reads the data from the slave. The sequence that software should perform to read from a memory device:

1. Left-shift the I^{2}C-device address one position and write the result to the transmit register. The least significant bit of the transmit register (R/W) is set to '0'.

2. Generate START condition and send contents of transmit register by setting the STA and WR bits in the command register.

3. Wait for interrupt or for TIP bit in the status register to go low.

4. Read RxACK bit in status register. If RxACK is low the slave has acknowledged the transfer, proceed to step 5. If RxACK is set the device did not acknowledge the transfer, go to step 1.

5. Write the memory location to be read from the slave to the transmit register.

6. Set the WR bit in the command register. Note that a STOP condition is not generated here.

7. Wait for interrupt, or for TIP bit in the status register to go low.

8. Read RxACK bit in the status register. RxACK should be low.

9. Address the I^{2}C-slave again by writing its left-shifted address into the transmit register. Set the least significant bit of the transmit register (R/W) to '1' to read from the slave.

10. Set the STA and WR bits in the command register to generate a repeated START condition.

11. Wait for interrupt, or for TIP bit in the status register to go low.

12. Read RxACK bit in the status register. The slave should acknowledge the transfer.

13. Prepare to receive the data read from the I^{2}C-connected memory. Set bits RD, ACK and STO on the command register. Setting the ACK bit NAKs the received data and signifies the end of the transfer.

14. Wait for interrupt, or for TIP in the status register to go low.

15. The received data can now be read from the receive register.

To perform sequential reads the master can iterate over steps 13 - 15 by not setting the ACK and STO bits in step 13. To end the sequential reads the ACK and STO bits are set. Consult the documentation of the I^{2}C-slave to see if sequential reads are supported.

The final sequence illustrates how to write one byte to an I^{2}C-slave which requires addressing. First the slave is addressed and the memory location on the slave is transmitted. After the slave has acknowledged the memory location the data to be written is transmitted without a generating a new START condition:

1. Left-shift the I^{2}C-device address one position and write the result to the transmit register. The least significant bit of the transmit register (R/W) is set to '0'.
2. Generate START condition and send contents of transmit register by setting the STA and WR bits in the command register.
3. Wait for interrupt or for TIP bit in the status register to go low.
4. Read RxACK bit in status register. If RxACK is low the slave has acknowledged the transfer, proceed to step 5. If RxACK is set the device did not acknowledge the transfer, go to step 1.
5. Write the memory location to be written from the slave to the transmit register.
6. Set the WR bit in the command register.
7. Wait for interrupt, or for TIP bit in the status register to go low.
8. Read RxACK bit in the status register. RxACK should be low.
9. Write the data byte to the transmit register.
10. Set WR and STO in the command register to send the data byte and then generate a STOP condition.
11. Wait for interrupt, or for TIP bit in the status register to go low.
12. Check RxACK bit in the status register. If the write succeeded the slave should acknowledge the data byte transfer.

The example sequences presented here can be generally applied to I^{2}C-slaves. However, some devices may deviate from the protocol above, please consult the documentation of the I^{2}C-slave in question. Note that a software driver should also monitor the arbitration lost (AL) bit in the status register.

72.2.4 Signal filters

The core is configured at implementation to use one of two possible filter strategies: a static filter or a dynamic filter, the selection between the two options is made with the *dynfilt* VHDL generic.

With a static filter (*dynfilt* = 0) the core will implement low-pass filters using simple shift registers. The number of shift registers is determined by the VHDL generic *filter*. When all bits in a shift register are equal, the core will consider the state of the input signal (SCL or SDA) to have changed. An appropriate value for the filter generic is calculated via:

$$filter = \frac{\overline{pulsetime}}{systemclockperiod} + 1$$

To disregard any pulse that is 50 ns or shorter in a system with a system frequency of 54 MHz the *filter* generic should be set to: (50 ns) / ((1/(54 MHz)) + 1 = 3.7. The value from this calculation should always be rounded up. In other words an appropriate filter length for a 54 MHz system is 4.

With a dynamic filter (*dynfilt* = 1) the VHDL generic *filter* determines the number of bits implemented in a counter that controls the sample window. The reload value for the counter can then be specified by software by writing to the core's dynamic filter register available via the APB interface. The number of bits required for the dynamic counter is calculated using (where system clock period is the shortest system clock period that the design will use):

$$filter = \log 2\left(\frac{\overline{pulsetime}}{systemclockperiod} + 1\right)$$

When using dynamic filtering, the core will ignore all pulses shorter than the system clock period multiplied with the value of the FILT field in the core's Dynamic Filter register and may also ignore pulses that are shorter than 2 * FILT * (system clock period) - 1.

72.3 Registers

The core is programmed through registers mapped into APB address space.

Table 1304. I^2C-master registers

APB address offset	Register
0x00	Clock prescale register
0x04	Control register
0x08	Transmit register*
0x08	Receive register**
0x0C	Command register*
0x0C	Status register**
0x10	Dynamic filter register***

* Write only

** Read only

*** Only available on some implementations

72.3.1 I²C-Master Clock Prescale Register

*Table 1305.*0x00 - PRESCALE - I²C-master Clock prescale register

31 16	15 0
RESERVED	Clock prescale
0	0xFFFF
r	rw

31 : 16 RESERVED

15:0 Clock prescale - Value is used to prescale the SCL clock line. Do not change the value of this register unless the EN field of the control register is set to '0'. The minimum recommended value of this register is 0x0003. Lower values may cause the master to violate I²C timing requirements due to synchronization issues.

72.3.2 I²C-Master Control Register

*Table 1306.*0x04 - CTRL - I²C-master control register

31 8	7	6	5 0
RESERVED	EN	IEN	RESERVED
0	0	0	0
r	rw	rw	r

31 : 8 RESERVED

7 Enable (EN) - Enable I²C core. The core is enabled when this bit is set to '1'.

6 Interrupt enable (IEN) - When this bit is set to '1' the core will generate interrupts upon transfer completion.

5:0 RESERVED

72.3.3 I²C-Master Transmit Register

*Table 1307.*0x08 - TX - I²C-master transmit register

31 8	7 1	0
RESERVED	TDATA	RW
0	0	0
-	w	w

31 : 8 RESERVED

7:1 Transmit data (TDATA) - Most significant bits of next byte to transmit via I²C

0 Read/Write (RW) - In a data transfer this is the data's least significant bit. In a slave address transfer this is the RW bit. '1' reads from the slave and '0' writes to the slave.

72.3.4 I²C-Master Receive Register

*Table 1308.*0x08 - RX - I²C-master receive register

31 8	7 0
RESERVED	RDATA
	0
	r

31 : 8 RESERVED

7:0 Receive data (RDATA) - Last byte received over I²C-bus.

72.3.5 I²C-Master Command Register

*Table 1309.*0x0C -CMD - I²C-master command register

31 … 8	7	6	5	4	3	2 … 1	0
RESERVED	STA	STO	RD	WR	ACK	RESERVED	IACK
0	0	0	0	0	0	0	0
r	w*	w*	w*	w*	w*	r	-

31 : 8 RESERVED

7 Start (STA) - Generate START condition on I²C-bus. This bit is also used to generate repeated START conditions.

6 Stop (STO) - Generate STOP condition

5 Read (RD) - Read from slave

4 Write (WR) - Write to slave

3 Acknowledge (ACK) - Used when acting as a receiver. ‘0’ sends an ACK, ‘1’ sends a NACK.

2:1 RESERVED

0 Interrupt acknowledge (IACK) - Clears interrupt flag (IF) in status register.

72.3.6 I²C-Master Status Register

*Table 1310.*0x0C - STAT - I²C-master status register

31 … 8	7	6	5	4 … 2	1	0
RESERVED	RxACK	BUSY	AL	RESERVED	TIP	IF
0	0	0	0	0		
r	r	r	r	r	r	wc

31 : 8 RESERVED

7 Receive acknowledge (RxACK) - Received acknowledge from slave. ‘1’ when no acknowledge is received, ‘0’ when slave has acked the transfer.

6 I²C-bus busy (BUSY) - This bit is set to ‘1’ when a start signal is detected and reset to ‘0’ when a stop signal is detected.

5 Arbitration lost (AL) - Set to ‘1’ when the core has lost arbitration. This happens when a stop signal is detected but not requested or when the master drives SDA high but SDA is low.

4:2 RESERVED

1 Transfer in progress (TIP) - ‘1’ when transferring data and ‘0’ when the transfer is complete. This bit is also set when the core will generate a STOP condition.

0 Interrupt flag (IF) - This bit is set when a byte transfer has been completed and when arbitration is lost. If IEN in the control register is set an interrupt will be generated. New interrupts will ge generated even if this bit has not been cleared.

72.3.7 I²C-Master Dynamic Filter Register

*Table 1311.*0x10 - FILT - I²C-master dynamic filter register

31 x	x-1 0
RESERVED	FILT
0	all 1
r	rw*

31 : x RESERVED

x-1 : 0 Dynamic filter reload value (FILT) - This field sets the reload value for the dynamic filter counter. The core will ignore all pulses on the bus shorter than FILT * (system clock period) and may also ignore pulses shorter than 2 * FILT * (system clock period) - 1. The reset value of this register is all '1'.

This register is not available in all implementations, and only for core revisions higher than two (the core's version number can be read from the plug'n'play area). When implemented, the number of bits in the FILT field is implementation dependent. Software can probe the precense of this register by writing 0x1 to the register location and reading back the value. If the read value is non-zero then the core has been implemented with a dynamic filter.

72.4 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x028. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

72.5 Implementation

72.5.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

72.6 Configuration options

Table 1312 shows the configuration options of the core (VHDL generics).

*Table 1312.*Configuration options

Generic name	Function	Allowed range	Default
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	ADDR field of the APB BAR.	0 - 16#FFF#	0
pmask	MASK field of the APB BAR.	0 - 16#FFF#	16#FFF#
pirq	Interrupt line used by I^2C-master	0 - NAHBIRQ-1	0
oepol	Output enable polarity	0 - 1	0
filter	Low-pass filter length. This generic should specify, in number of system clock cycles plus one, the time of the shortest pulse on the I2C bus to be registered as a valid value. For instance, to disregard any pulse that is 50 ns or shorter in a system with a system frequency of 54 MHz this generic should be set to: ((pulse time) / (clock period)) + 1 = (50 ns) / ((1/(54 MHz)) + 1 = 3.7 The value from this calculation should always be rounded up. In other words an appropriate filter length for a 54 MHz system is 4. Note that the value of this generic changes meaning if the dynfilt generic described below is non-zero. See description below.	2 - 512	2
dynfilt	Dynamic low-pass filter length. If this generic is non-zero the core will be implemented with a configurable filter. If dynfilt is non-zero the filter generic, described above, specifies how many bits that will be implemented for the dynamic filter counter.	0 - 1	0

72.7 Signal descriptions

Table 1313 shows the interface signals of the core (VHDL ports).

*Table 1313.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
I2CI	SCL	Input	I^2C clock line input	-
	SDA	Input	I^2C data line input	-
I2CO	SCL	Output	I^2C clock line output	-
	SCLOEN	Output	I^2C clock line output enable	Low
	SDA	Output	I^2C data line output	-
	SDAOEN	Output	I^2C data line output enable	Low

* see GRLIB IP Library User's Manual

72.8 Signal definitions and reset values

The signals and their reset values are described in table 1314.

*Table 1314.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
scl	InputOutput	I^2C clock line		Tri-state
sda	InputOutput	I^2C data line	-	Tri-state

72.9 Timing

The timing waveforms and timing parameters are shown in figure 209 and are defined in table 1315.

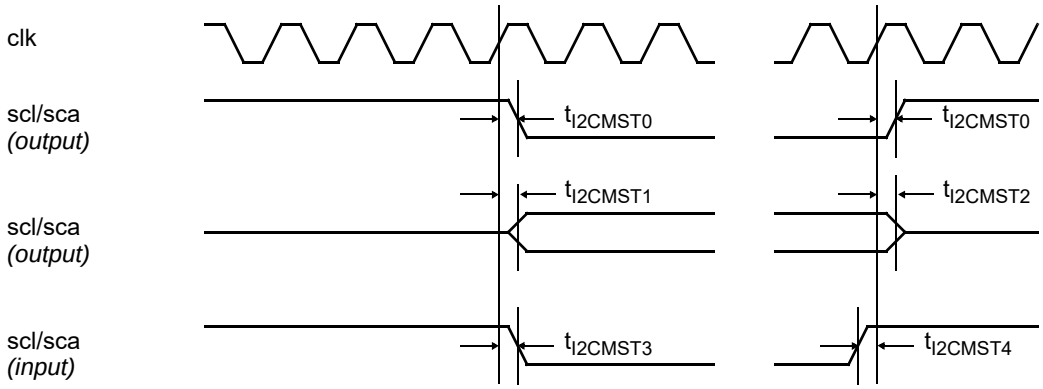


Figure 209. Timing waveforms

*Table 1315.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{I2CMST0}$	clock to output delay	rising *clk* edge	TBD	TBD	ns
$t_{I2CMST1}$	clock to non-tri-state delay	rising *clk* edge	TBD	TBD	ns
$t_{I2CMST2}$	clock to tri-state delay	rising *clk* edge	TBD	TBD	ns
$t_{I2CMST3}$	input to clock hold[x]	rising *clk* edge	x	x	ns
$t_{I2CMST4}$	input to clock setup[x]	rising *clk* edge	x	x	ns
[x] The SCL and SDA inputs are re-synchronized internally and do not need to meet any setup or hold requirements relative to the core's AMBA APB clock.					

The core's I^2C bus functional timing depends on the core's scaler value. When the scaler is set for the core to operate in Fast- or Standard-Mode, the timing characteristics specified in the I^2C-bus Specification apply.

72.10 Library dependencies

Table 1316 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1316.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	I2C	Component, signals	Component declaration, I2C signal definitions

72.11 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib, techmap;
use grlib.amba.all;
use techmap.gencomp.all;

library gaisler;
use gaisler.misc.all;

entity i2c_ex is
  port (
    clk  : in std_ulogic;
    rstn : in std_ulogic;

    -- I2C signals
    iic_scl : inout std_ulogic;
    iic_sda : inout std_ulogic
    );
end;

architecture rtl of i2c_ex is

  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);

  -- I2C signals
  signal i2ci : i2c_in_type;
  signal i2co : i2c_out_type;
begin

  -- AMBA Components are instantiated here
  ...

  -- I2C-master
  i2c0 : i2cmst
    generic map (pindex => 12, paddr => 12, pmask => 16#FFF#,
                 pirq => 8, filter => (BUS_FREQ_in_kHz*5+50000)/100000+1)
    port map (rstn, clkm, apbi, apbo(12), i2ci, i2co);

  -- Using bi-directional pads:
  i2c_scl_pad : iopad generic map (tech => padtech)
    port map (iic_scl, i2co.scl, i2co.scloen, i2ci.scl);
  i2c_sda_pad : iopad generic map (tech => padtech)
    port map (iic_sda, i2co.sda, i2co.sdaoen, i2ci.sda);
  -- Note: Some designs may want to use a uni-directional pad for the clock. In this case the
  -- the clock should have a on-chip feedback like: i2ci.scl <= i2co.scloen (for OEPOL = 0)
  -- This feedback connection should have the same delay as i2co.sdaoen to i2ci.sda
end;
```

73 I2CSLV - I^{2}C slave

73.1 Overview

The I^{2}C slave core is a simple I^{2}C slave that provides a link between the I^{2}C bus and the AMBA APB. The core is compatible with Philips I^{2}C standard and supports 7- and 10-bit addressing with an optionally software programmable address. Standard-mode (100 kb/s) and Fast-mode (400 kb/s) operation are supported directly. External pull-up resistors must be supplied for both bus lines.

GRLIB also contains another I^{2}C slave core that has DMA capabilities, see the I2C2AHB core documentation for details.

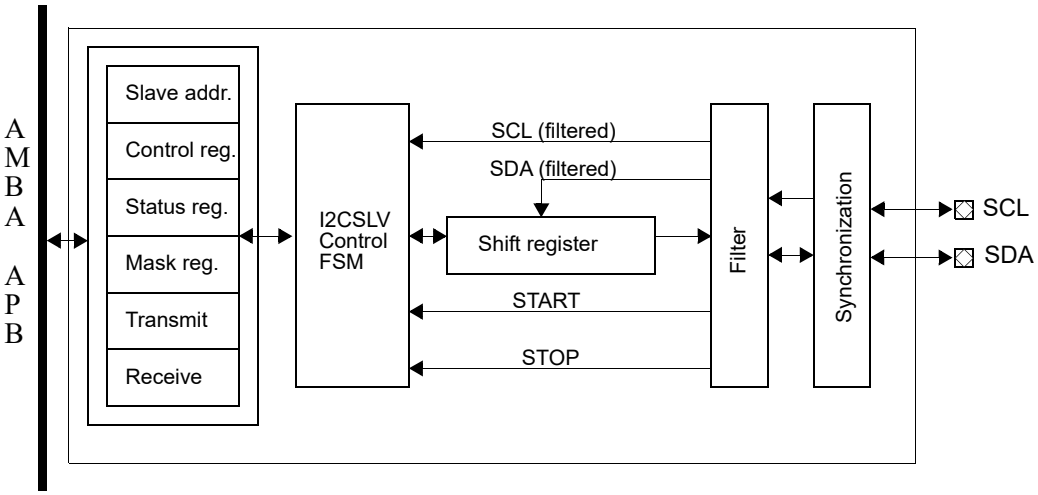


Figure 210. Block diagram

73.2 Operation

73.2.1 Transmission protocol

The I^{2}C-bus is a simple 2-wire serial multi-master bus with collision detection and arbitration. The bus consists of a serial data line (SDA) and a serial clock line (SCL). The I^{2}C standard defines three transmission speeds; Standard (100 kb/s), Fast (400 kb/s) and High speed (3.4 Mb/s).

A transfer on the I^{2}C-bus begins with a START condition. A START condition is defined as a high to low transition of the SDA line while SCL is high. Transfers end with a STOP condition, defined as a low to high transition of the SDA line while SCL is high. These conditions are always generated by a master. The bus is considered to be busy after the START condition and is free after a certain amount of time following a STOP condition. The bus free time required between a STOP and a START condition is defined in the I^{2}C-bus specification and is dependent on the bus bit rate.

Figure 211 shows a data transfer taking place over the I^{2}C-bus. The master first generates a START condition and then transmits the 7-bit slave address. I^{2}C also supports 10-bit addresses, which are discussed briefly below. The bit following the slave address is the R/$\overline{W}$ bit which determines the direction of the data transfer. In this case the R/$\overline{W}$ bit is zero indicating a write operation. After the master has transmitted the address and the R/$\overline{W}$ bit it releases the SDA line. The receiver pulls the SDA line low to acknowledge the transfer. If the receiver does not acknowledge the transfer, the master may generate a STOP condition to abort the transfer or start a new transfer by generating a repeated START condition.

After the address has been acknowledged the master transmits the data byte. If the R/$\overline{W}$ bit had been set to ‘1’ the master would have acted as a receiver during this phase of the transfer. After the data

byte has been transferred the receiver acknowledges the byte and the master generates a STOP condition to complete the transfer.

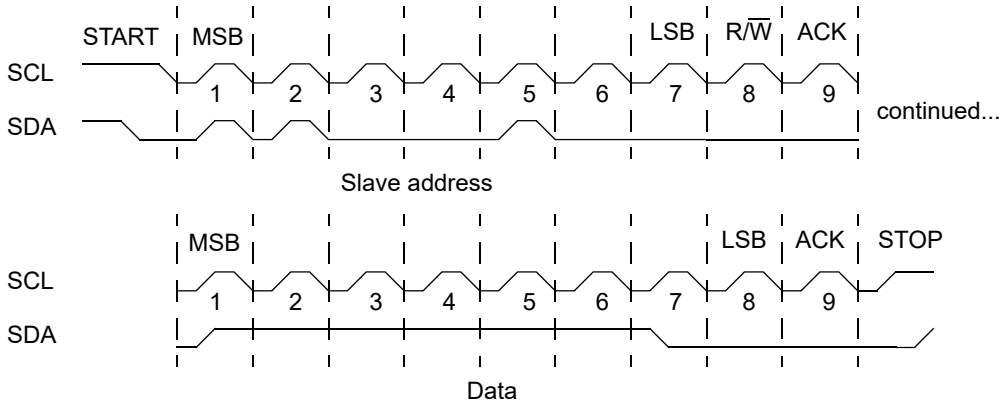


Figure 211. Complete I^{2}C data transfer

An I^{2}C slave may also support 10-bit addressing. In this case the master first transmits a pattern of five reserved bits followed by the two first bits of the 10-bit address and the R/$\overline{W}$ bit set to '0'. The next byte contains the remaining bits of the 10-bit address. If the transfer is a write operation the master then transmits data to the slave. To perform a read operation the master generates a repeated START condition and repeats the first part of the 10-bit address phase with the R/$\overline{W}$ bit set to '1'.

If the data bitrate is too high for a slave device or if the slave needs time to process data, it may stretch the clock period by keeping SCL low after the master has driven SCL low.

73.2.2 Slave addressing

The core's addressing support is implementation dependent. The core may have a programmable address and may support 10-bit addresses. If the core has support for 10-bit addressing, the TBA bit of the Slave address register will be set to '1' after reset. If the core's address is programmable this bit is writable and is used by the core to determine if it should listen to a 7- or 10-bit address.

Software can determine the addressing characteristics of the core by writing and reading the Slave address register. The core supports 10-bit addresses if the TBA bit is, or can be set, to '1'. The core has a software programmable address if the SLVADDR field in the same register can be changed.

73.2.3 System clock requirements and sampling

The core samples the incoming I^{2}C SCL clock and does not introduce any additional clock domains into the system. Both the SCL and SDA lines first pass through two stage synchronizers and are then filtered with a low pass filter consisting of four registers.

START and STOP conditions are detected if the SDA line, while SCL is high, is at one value for two system clock cycles, toggles and keeps the new level for two system clock cycles.

The synchronizers and filters constrain the minimum system frequency. The core requires the SCL signal to be stable for at least four system clock cycles before the core accepts the SCL value as the new clock value. The core's reaction to transitions will be additionally delayed since both lines are taken through two-stage synchronizers before they are filtered. Therefore it takes the core over eight system clock cycles to discover a transition on SCL. To use the slave in Standard-mode operation at 100 kHz the recommended minimum system frequency is 2 MHz. For Fast-mode operation at 400 kHz the recommended minimum system frequency is 6 MHz.

73.2.4 Operational model

The core has four main modes of operation and is configured to use one of these modes via the Control register bits Receive Mode (RMOD) and Transmit Mode (TMOD). The mode setting controls the core's behavior after a byte has been received or transmitted.

The core will always NAK a received byte if the receive register is full when the whole byte is received. If the receive register is free the value of RMOD determines if the core should continue to listen to the bus for the master's next action or if the core should drive SCL low to force the master into a wait state. If the value of the RMOD field is '0' the core will listen for the master's next action. If the value of the RMOD field is '1' the core will drive SCL low until the Receive register has been read and the Status register bit Byte Received (REC) has been cleared. Note that the core has not accepted a byte if it does not acknowledge the byte.

When the core receives a read request it evaluates the Transmit Valid (TV) bit in the Control register. If the Transmit Valid bit is set the core will acknowledge the address and proceed to transmit the data held in the Transmit register. After a byte has been transmitted the core assigns the value of the Control register bit Transmit Always Valid (TAV) to the Transmit Valid (TV) bit. This mechanism allows the same byte to be sent on all read requests without software intervention. The value of the Transmit Mode (TMOD) bit determines how the core acts after a byte has been transmitted and the master has acknowledged the byte, if the master NAKs the transmitted byte the transfer has ended and the core goes into an idle state. If TMOD is set to '0' when the master acknowledges a byte the core will continue to listen to the bus and wait for the master's next action. If the master continues with a sequential read operation the core will respond to all subsequent requests with the byte located in the Transmit Register. If TMOD is '1' the core will drive SCL low after a master has acknowledged the transmitted byte. SCL will be driven low until the Transmit Valid bit in the control register is set to '1'. Note that if the Transmit Always Valid (TAV) bit is set to '1' the Transmit Valid bit will immediately be set and the core will have show the same behavior for both Transmit modes.

When operating in Receive or Transmit Mode '1', the bus will be blocked by the core until software has acknowledged the transmitted or received byte. This may have a negative impact on bus performance and it also affects single byte transfers since the master is prevented to generate STOP or repeated START conditions when SCL is driven low by the core.

The core reports three types of events via the Status register. When the core NAKs a received byte, or its address in a read transfer, the NAK bit in the Status register will be set. When a byte is successfully received the core asserts the Byte Received (REC) bit. After transmission of a byte, the Byte Transmitted (TRA) bit is asserted. These three bits can be used as interrupt sources by setting the corresponding bits in the Mask register.

73.3 Registers

The core is programmed through registers mapped into APB address space.

Table 1317. I^2C slave registers

APB address offset	Register
0x00	Slave address register
0x04	Control register
0x08	Status register
0x0C	Mask register
0x10	Receive register
0x14	Transmit register

73.3.1 Slave Address Register

*Table 1318.*0x00 - SLVADDR - Slave address register

31	30 ... ALEN	ALEN-1 ... 0
TBA	RESERVED	SLVADDR
*	0	*
rw	r	rw*

31 Ten-bit Address (TBA) - When this bit is set the core will interpret the value in the SLVADDR field as a 10-bit address. If the core has 10-bit address support this bit will have the reset value '1'.

30 : ALEN RESERVED

(ALEN-1):0 Slave address (SLVADDR) - Contains the slave I2C address. The width of the slave address field, ALEN, is 7 bits (6:0) if the core only has support for 7-bit addresses. If the core has support for 10-bit addressing the width of SLVADDR is 10 bits. Depending on the hardware configuration this register may be read only. The core checks the length of the programmed address and will function with 7-bit addresses even if it has support for 10-bit addresses.

I^2C addresses can be allocated by NXP, please see the link in the core's overview section.

73.3.2 Control Register

*Table 1319.*0x04 - CTRL - Control register

31 ... 5	4	3	2	1	0
RESERVED	RMOD	TMOD	TV	TAV	EN
0	NR	NR	NR	NR	NR
r	rw	rw	rw	rw	rw

31 : 5 RESERVED

4 Receive Mode (RMOD) - Selects how the core handles writes:

'0': The slave accepts one byte and NAKs all other transfers until software has acknowledged the received byte by reading the Receive register.

'1': The slave accepts one byte and keeps SCL low until software has acknowledged the received byte by reading the Receive register.

3 Transmit Mode (TMOD) - Selects how the core handles reads:

'0': The slave transmits the same byte to all if the master requests more than one byte in the transfer. The slave then NAKs all read requests as long as the Transmit Valid (TV) bit is unset.

'1': The slave transmits one byte and then keeps SCL low until software has acknowledged that the byte has been transmitted by setting the Transmit Valid (TV) bit.

2 Transmit Valid (TV) - Software sets this bit to indicate that the data in the transmit register is valid. The core automatically resets this bit when the byte has been transmitted. When this bit is '0' the core will either NAK or insert wait states on incoming read requests, depending on the Transmit Mode (TMOD).

1 Transmit Always Valid (TAV) - When this bit is set, the core will not clear the Transmit Valid (TV) bit when a byte has been transmitted.

0 Enable core (EN) - Enables core. When this bit is set to '1' the core will react to requests to the address set in the Slave address register. If this bit is '0' the core will keep both SCL and SDA inputs in Hi-Z state.

73.3.3 Status Register

*Table 1320.*0x08 - STAT - Status register

31	3	2	1	0
RESERVED		REC	TRA	NAK
0		0	0	0
r		*	wc	wc

31 : 3 RESERVED

2 Byte Received (REC) - This bit is set to '1' when the core accepts a byte and is automatically cleared when the Receive register has been read.

1 Byte Transmitted (TRA) - This bit is set to '1' when the core has transmitted a byte and is cleared by writing '1' to this position. Writes of '0' have no effect.

0 NAK Response (NAK) - This bit is set to '1' when the core has responded with NAK to a read or write request. This bit does not get set to '1' when the core responds with a NAK to an address that does not match the cores address. This bit is cleared by writing '1' to this position, writes of '0' have no effect.

73.3.4 Mask Register

*Table 1321.*0x0C - MASK - Mask register

31	3	2	1	0
RESERVED		RECE	TRAE	NAKE
0		0	0	0
r		rw	rw	rw

31 : 3 RESERVED

2 Byte Received Enable (RECE) - When this bit is set the core will generate an interrupt when bit 2 in the Status register gets set.

1 Byte Transmitted Enable (TRAE) - When this bit is set the core will generate an interrupt when bit 1 in the Status register gets set.

0 NAK Response Enable (NAKE) - When this bit is set the core will generate an interrupt when bit 0 in the Status register gets set.

73.3.5 Receive Register

*Table 1322.*0x10 - RX - Receive register

31	8	7	0
RESERVED		RECBYTE	
0		NR	
r		r	

31 : 8 RESERVED

7:0 Received Byte (RECBYTE) - Last byte received from master. This field only contains valid data if the Byte received (REC) bit in the status register has been set.

73.3.6 Transmit Register

*Table 1323.*0x14 - TX - Transmit register

31 8	8 7 0
RESERVED	TRABYTE
0	NR
r	rw

31 : 8 RESERVED

7:0 Transmit Byte (TRABYTE) - Byte to transmit on the next master read request.

Reset value: Undefined

73.4 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x03E. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

73.5 Implementation

73.5.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

73.6 Configuration options

Table 1324 shows the configuration options of the core (VHDL generics).

*Table 1324.*Configuration options

Generic name	Function	Allowed range	Default
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	ADDR field of the APB BAR.	0 - 16#FFF#	0
pmask	MASK field of the APB BAR.	0 - 16#FFF#	16#FFF#
pirq	Interrupt line used by I^2C slave	0 - NAHBIRQ-1	0
hardaddr	If this generic is set to 1 the core uses the value of generic i2caddr as the hard coded address. If hardaddr is set to 0 the core's address can be changed via the Slave address register.	0 - 1	0
tenbit	If this generic is set to 1 the core will support 10-bit addresses. Note that the core can still be configured to use a 7-bit address.	0 - 1	0
i2caddr	The slave's (initial) I^2C address.	0 - 1023	0
oepol	Output enable polarity	0 - 1	0
filter	Low-pass filter length. This generic should specify, in number of system clock cycles plus one, the time of the shortest pulse on the I2C bus to be registered as a valid value. For instance, to disregard any pulse that is 50 ns or shorter in a system with a system frequency of 54 MHz this generic should be set to: ((pulse time) / (clock period)) + 1 = (50 ns) / ((1/(54 MHz)) + 1 = 3.7 The value from this calculation should always be rounded up. In other words an appropriate filter length for a 54 MHz system is 4.	2 - 512	2

73.7 Signal descriptions

Table 1325 shows the interface signals of the core (VHDL ports).

*Table 1325.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
I2CI	SCL	Input	I^2C clock line input	-
	SDA	Input	I^2C data line input	-
I2CO	SCL	Output	I^2C clock line output	-
	SCLOEN	Output	I^2C clock line output enable	Low**
	SDA	Output	I^2C data line output	-
	SDAOEN	Output	I^2C data line output enable	Low**
	ENABLE	Output	High when core is enabled, low otherwise	High

* see GRLIB IP Library User's Manual
** Depends on OEPOL VHDL generic

73.8 Signal definitions and reset values

The signals and their reset values are described in table 1326.

*Table 1326.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
scl	InputOutput	I^2C clock line	-	Hi-Z
sda	InputOutput	I^2C data line	-	Hi-Z

73.9 Library dependencies

Table 1327 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1327.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	I2C	Component, signals	Component declaration, I2C signal definitions

73.10 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib, techmap;
use grlib.amba.all;
use techmap.gencomp.all;

library gaisler;
use gaisler.misc.all;
```

```
entity i2cslv_ex is
  port (
    clk  : in std_ulogic;
    rstn : in std_ulogic;

    -- I2C signals
    iic_scl : inout std_ulogic;
    iic_sda : inout std_ulogic
    );
end;

architecture rtl of i2cslv_ex is

  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);

  -- I2C signals
  signal i2ci : i2c_in_type;
  signal i2co : i2c_out_type;
begin

  -- AMBA Components are instantiated here
  ...

  -- I2C-slave
  i2cslv0 : i2cslv
    generic map (pindex => 1, paddr => 1, pmask => 16#FFF#, pirq => 1,
                 hardaddr => 0, tenbit => 1, i2caddr => 16#50#)
    port map (rstn, clk, apbi, apbo(1), i2ci, i2co);
  i2cslv0_scl_pad : iopad generic map (tech => padtech)
    port map (iic_scl, i2co.scl, i2co.scloen, i2ci.scl);
  i2cslv0_sda_pad : iopad generic map (tech => padtech)
    port map (iic_sda, i2co.sda, i2co.sdaoen, i2ci.sda);
end;
```

74 IRQMP - Multiprocessor Interrupt Controller

74.1 Overview

The AMBA system in GRLIB provides an interrupt scheme where interrupt lines are routed together with the remaining AHB/APB bus signals, forming an interrupt bus. Interrupts from AHB and APB units are routed through the bus, combined together, and propagated back to all units. The multiprocessor interrupt controller core is attached to the AMBA bus as an APB slave, and monitors the combined interrupt signals.

The interrupts generated on the interrupt bus are all forwarded to the interrupt controller. The interrupt controller prioritizes, masks and propagates the interrupt with the highest priority to the processor. In multiprocessor systems, the interrupts are propagated to all processors.

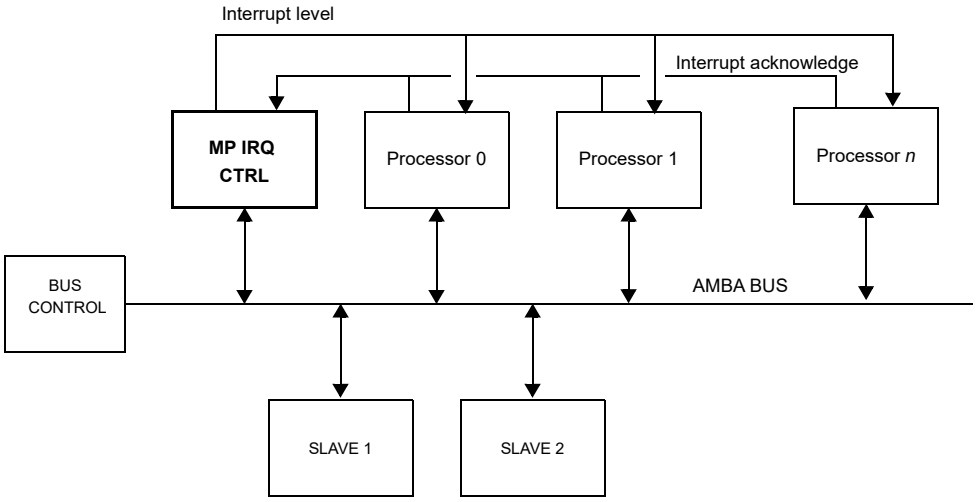


Figure 212. LEON multiprocessor system with Multiprocessor Interrupt controller

74.2 Operation

74.2.1 Interrupt prioritization

The interrupt controller monitors interrupt 1 - 15 of the interrupt bus (APBI.PIRQ[15:1]). When any of these lines are asserted high, the corresponding bit in the interrupt pending register is set. The pending bits will stay set even if the PIRQ line is de-asserted, until cleared by software or by an interrupt acknowledge from the processor. The default behaviour for peripherals is to use pulsed interrupts (an interrupt line is asserted for one clock cycle to signal an interrupt).

Each interrupt can be assigned to one of two levels (0 or 1) as programmed in the interrupt level register. Level 1 has higher priority than level 0. The interrupts are prioritised within each level, with interrupt 15 having the highest priority and interrupt 1 the lowest. The highest interrupt from level 1 will be forwarded to the processor. If no unmasked pending interrupt exists on level 1, then the highest unmasked interrupt from level 0 will be forwarded. PIRQ[31:16] are not used by the IRQMP core.

Interrupts are prioritised at system level, while masking and forwarding of interrupts in done for each processor separately. Each processor in an multiprocessor system has separate interrupt mask and force registers. When an interrupt is signalled on the interrupt bus, the interrupt controller will prioritize interrupts, perform interrupt masking for each processor according to the mask in the corresponding mask register and forward the interrupts to the processors.

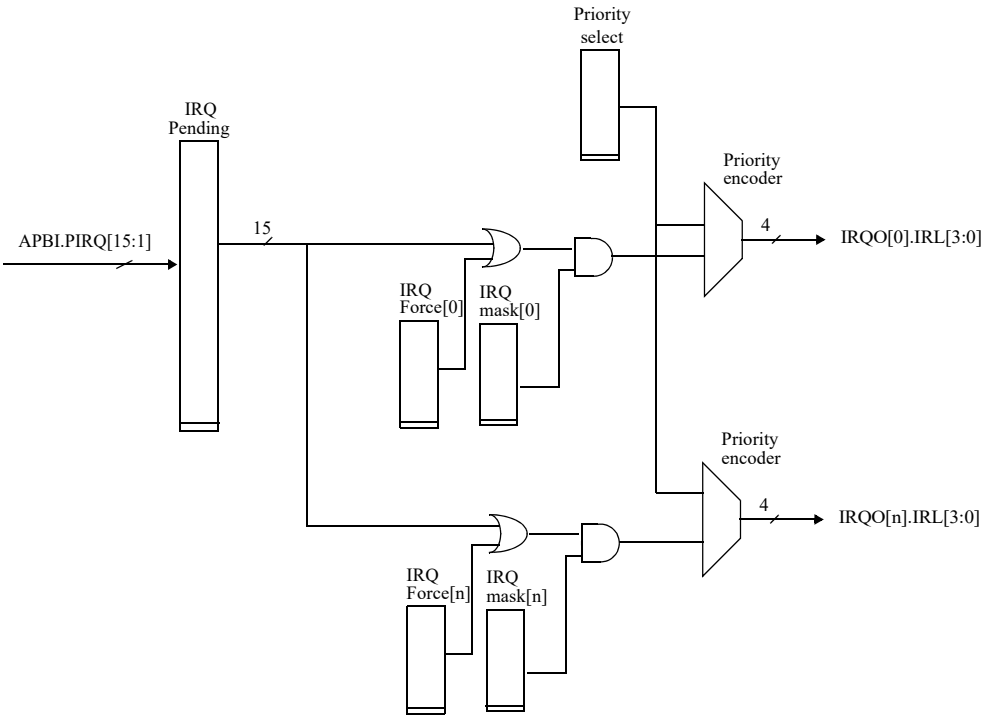


Figure 213. Interrupt controller block diagram

When a processor acknowledges the interrupt, the corresponding pending bit will automatically be cleared. Note that in a multiprocessor system, the bit in the pending register will be cleared as soon as one of the processors acknowledges the interrupt and interrupt broadcast functionality should be used for interrupts that need to be propagated to all processors. Interrupt can also be forced by setting a bit in the interrupt force register. In this case, the processor acknowledgement will clear the force bit rather than the pending bit. After reset, the interrupt mask register is set to all zeros while the remaining control registers are undefined. Note that interrupt 15 cannot be maskable by the LEON processor and should be used with care - most operating systems do not safely handle this interrupt.

74.2.2 Extended interrupts

The AHB/APB interrupt consist of 32 signals ([31:0]), while the IRQMP only uses lines 1 - 15 in the nominal mode. To use the additional 16 interrupt lines (16-31), extended interrupt handling can be enabled by setting the VHDL generic *eirq* to a value between 1 - 15. The interrupt lines 16 - 31 will then also be handled by the interrupt controller, and the interrupt pending and mask registers will be extended to 32 bits. Since the processor only has 15 interrupt levels (1 - 15), the extended interrupts will generate one of the regular interrupts, indicated by the value of the *eirq* generic. When the interrupt is taken and acknowledged by the processor, the regular interrupt (*eirq*) and the extended interrupt pending bits are automatically cleared. The extended interrupt acknowledge register will identify which extended interrupt that was most recently acknowledged. This register can be used by software to invoke the appropriate interrupt handler for the extended interrupts.

74.2.3 Processor status monitoring

The processor status can be monitored through the Multiprocessor Status Register. The STATUS field in this register indicates if a processor is in power-down (‘1’) or running (‘0’). A processor can be made running by writing a ‘1’ to its status field. After reset, all processors except processor 0 are halted (can be changed using the functionality associated with the *extrun* VHDL generic). When the system is properly initialized, processor 0 can start the remaining processors by writing to their STATUS bits. See also the extended boot support in section 74.2.4.

74.2.4 Extended boot support

When the bootreg generic is set, registers are added to allow starting a halted CPU from an arbitrary 8 byte aligned entry point. The CPU can be started with the same register write as when the entry point is written, or the CPU can be started later using the regular multiprocessor status register bit.

An error register is also added to allow monitoring CPUs for error mode, and to allow forcing a specific CPU into error mode. This can be used to monitor and re-boot CPUs without resetting the system.

A read-only bit in the multiprocessor status register can be read to see if the bootreg functionality has been configured in.

74.2.5 Interrupt broadcasting

The Broadcast Register is activated when the generic *ncpu* is > 1. An incoming irq that has its bit set in the Broadcast Register is propagated to the force register of *all* CPUs instead of to the Pending Register. This can be used to implement a timer that fires to all CPUs with that same irq.

74.2.6 Interrupt (re)map functionality

The interrupt controller can optionally be implemented (as an alternative to the two-interrupt levels scheme) with functionality to allow dynamic remapping between bus interrupt lines and interrupt controller interrupt lines. If the design includes this functionality then switch-logic will be placed on the incoming interrupt vector from the AMBA bus before the IRQ pending register. The Interrupt map registers will be available starting at offset 0x300 from the interrupt controller's base address.

The interrupt map registers contain one field for each bus interrupt line in the system. The value within this field determines to which interrupt controller line the bus interrupt line is connected. In case several bus interrupt lines are mapped to the same controller interrupt line (several fields in the Interrupt map registers have the same value) then the bus interrupt lines will be OR:ed together.

Note that if bus interrupt line X is remapped to controller interrupt line Y then bit Y of the pending register will be set when a peripheral asserts interrupt X. Remapping interrupt lines via the Interrupt map registers has the same effect as changing the interrupt assignments in the RTL code.

74.3 Registers

The core is controlled through registers mapped into APB address space. The number of implemented registers depends on the number of processor in the multiprocessor system.

In order to make the boot registers available in the lower 256-byte space that is in the commonly used mapping, the registers are mapped into space that becomes unused when the number of processors is 8 or lower. If the number of CPUs is higher than 8, then the registers are only available in the higher space and a larger APB address mapping must be used to make them available.

*Table 1328.*Interrupt Controller registers

APB address offset	Register
0x00	Interrupt level register
0x04	Interrupt pending register
0x08	Interrupt force register (NCPU = 0)
0x0C	Interrupt clear register
0x10	Multiprocessor status register
0x14	Broadcast register
0x18	Error mode register
0x40	Processor interrupt mask register
0x44	Processor 1 interrupt mask register
0x40 + 4 * *n*	Processor *n* interrupt mask register
0x60 + 4 * n	Alias for processor n boot address register (only if BOOTREG=1 and NCPU < 9)
0x80	Processor interrupt force register
0x84	Processor 1 interrupt force register
0x80 + 4 * *n*	Processor *n* interrupt force register
0xC0	Processor extended interrupt acknowledge register
0xC4	Processor 1 extended interrupt acknowledge register
0xC0 + 4 * *n*	Processor *n* extended interrupt acknowledge register
0x200 + 0x4 * *n*	Processor n boot address register (if BOOTREG = 1)
0x300 + 0x4 * *n*	Interrupt map register *n*

74.3.1 Interrupt Level Register

*Table 1329.*0x000 - ILEVEL - Interrupt Level Register

31 16	15 1	0
RESERVED	IL[15:1]	R
0	NR	0
r	rw	r

31:16 Reserved

15:1 Interrupt Level n (IL[n]) - Interrupt level for interrupt n

0 Reserved

74.3.2 Interrupt Pending Register

*Table 1330.*0x004 - IPEND - Interrupt Pending Register

31 16	15 1	0
EIP[31:16]	IP[15:1]	R
0	0	0
rw	rw	r

31:16 Extended Interrupt Pending n (EIP[n])

15:1 Interrupt Pending n (IP[n]) - Interrupt pending for interrupt n

0 Reserved

74.3.3 Interrupt Force Register (NCPU = 0)

*Table 1331.*0x008 - IFORCE - Interrupt Force Register (NCPU = 0)

31 16	15 1	0
RESERVED	IF[15:1]	R
0	0	0
r	rw	r

31:16 Reserved

15:1 Interrupt Force n (IF[n]) - Force interrupt nr n.

0 Reserved

74.3.4 Interrupt Clear Register

*Table 1332.*0x00C - ICLEAR - Interrupt Clear Register

31 16	15 1	0
EIC[31:16]	IC[15:1]	R
0	0	0
w	w	r

31:16 Extended Interrupt Clear n (EIC[n])

15:1 Interrupt Clear n (IC[n]) - Writing ‘1’ to IC[n] will clear interrupt n

0 Reserved

74.3.5 Multiprocessor Status Register

*Table 1333.*0x010 - MPSTAT - Multiprocessor Status Register

31 28	27	26	25 20	19 16	15 0
NCPU	BA	ER	RESERVED	EIRQ	STATUS[15:0]
*	*	*	0	*	*
r	r	r	r	r	rw

31:28 Number of CPUs (NCPU) - Number of CPUs in the system - 1

27 Broadcast Available (BA) - Set to '1' if NCPU > 0.

26 Extended boot registers available (ER). Set to '1' if bootreg generic is 1.

25:20 Reserved

19:16 Extended IRQ (EIRQ) - Interrupt number (1 - 15) used for extended interrupts. Fixed to 0 if extended interrupts are disabled.

15:0 Power-down status of CPU[n] (STATUS[n]) - '1' = power-down, '0' = running. Write STATUS[n] with '1' to start processor n.

74.3.6 Broadcast Register (NCPU > 0)

*Table 1334.*0x014 - BRDCST - Broadcast Register (NCPU > 0)

31 16	15 1	0
RESERVED	BM15:1]	R
0	0	0
r	rw	r

31:16 Reserved

15:1 Broadcast Mask n (BM[n]) - If BM[n] = '1' then interrupt n is broadcasted (written to the Force Register of all CPUs), otherwise standard semantic applies (Pending register)

0 Reserved

74.3.7 Error Mode Status Register

*Table 1335.*0x018 - ERRSTAT - Error Mode Status Register

31 28	27 26	20 19	16	15 0
RESERVED				ERRMODE[15:0]
0				*
r				rw

31:16 Reserved

15:0 Read: Error mode status of CPU[n] (STATUS[n]) - '1' = error mode, '0' = other (debug/run/power-down).

Write: Force CPU[n] into error mode

Register is read-only if bootreg generic is 0..

74.3.8 Processor Interrupt Mask Register

*Table 1336.*0x040 - PIMASK - Processor Interrupt Mask Register

31 16	15 1	0
EIM[31:16]	IM15:1]	R
0	0	0
rw	rw	r

31:16 Extended Interrupt Mask n (EIC[n]) - Interrupt mask for extended interrupts

15:1 Interrupt Mask n (IM[n]) - If IM[n] = '0' then interrupt n is masked, otherwise it is enabled.

0 Reserved

74.3.9 Processor Interrupt Force Register (NCPU > 0)

*Table 1337.*0x080 - PIFORCE - Processor Interrupt Force Register (NCPU > 0)

31 17	16	15 1	0
IFC[15:1]	R	IF15:1]	R
0	0	0	0
wc	r	rw*	r

31:17 Interrupt Force Clear n (IFC[n]) - Interrupt force clear for interrupt n

16 Reserved

15:1 Interrupt Force n (IF[n]) - Force interrupt nr n

0 Reserved

74.3.10 Extended Interrupt Acknowledge Register

*Table 1338.*0x0C0 - PEXTACK - Extended Interrupt Acknowledge Register

31 5	4 0
RESERVED	EID[4:0]
0	0
r	r

31:5 Reserved

4:0 Extended interrupt ID (EID) - ID (16-31) of the most recent acknowledged extended interrupt.

If this field is 0, and support for extended interrupts exist, the last assertion of interrupt *eirq* was not the result of an extended interrupt being asserted. If interrupt *eirq* is forced, or asserted, this field will be cleared unless one, or more, of the interrupts 31 - 16 are enabled and set in the pending register.

74.3.11 Processor N Boot Address Register

*Table 1339.*0x200 + 0x4* n - BADDRn - Processor n Boot Address register

31 28	27 26	20 19	16 15	3	2 1	0
BOOTADDR[31:3]					RES	AS
-					-	-
w					-	w

31:3 Entry point for booting up processor N, 8-byte aligned

2:1 Reserved (write 0)

0 Start processor immediately after setting address

74.3.12 Interrupt Map Register N

*Table 1340.*0x300+4.n - IRQMAPn - Interrupt map register n

31 24	23 16	15 8	7 0
IRQMAP[n*4]	IRQMAP[n*4+1]	IRQMAP[n*4+2]	IRQMAP[n*4+3]
n.4	n.4+1	n.4+2	n.4+3
rw	rw	rw	rw

b+7 : b Interrupt map (IRQMAP) - If the core has been implemented to support interrupt mapping then the Interrupt map register at offset 0x300 + 4*n specifies the mapping for interrupt lines 4*n to 4*n+3. The bus interrupt line 4*n+x will be mapped to the interrupt controller interrupt line specified by the value of IRQMAP[n*4+x].

74.4 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x00D. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

74.5 Implementation

74.5.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support *grlib_async_reset_enable*. All registers that react on the reset signal will have a synchronous reset.

74.6 Configuration options

Table 1341 shows the configuration options of the core (VHDL generics).

*Table 1341.*Configuration options

Generic	Function	Allowed range	Defau1lt
pindex	Selects which APB select signal (PSEL) that will be used to access the interrupt controller	0 to NAPBMAX-1	0
paddr	The 12-bit MSB APB address	0 to 4095	0
pmask	The APB address mask	0 to 4095	4095
ncpu	Number of processors in multiprocessor system	1 to 16	1
eirq	Enable extended interrupts	0 - 15	0
irqmap	Enable interrupt (re-)map registers. If irqmap is set to 0 then interrupt map functionality is disabled. If irqmap is nonzero then (irqmap + eirq) = 1 includes map registers for bus interrupt lines 0 - 15. If (irqmap + eirq) > 1 then interrupt map registers are available for bus interrupt lines 0 - 31.	0 - 2	0
bootreg	Enable boot address register and error mode register.	0 - 1	1
extrun	Use external run vector. If this generic is set to 1 the start of processors after reset will be controlled via the input signal cpurun. If this generic is set to 0, CPU 0 will be started after reset and the other CPUs will be put in power-down mode. This requires that the SMP VHDL generic on the LEON entity is nonzero.	0 - 1	0

74.7 Signal descriptions

Table 1342 shows the interface signals of the core (VHDL ports).

*Table 1342.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
IRQI[n]	INTACK	Input	Processor *n* Interrupt acknowledge	High
	IRL[3:0]		Processor *n* interrupt level	High
	PWD		Processor *n* in power down mode	High
	FPEN		Unused	-
	ERR		Processor *n* in error mode	High
IRQO[n]	IRL[3:0]	Output	Processor *n* Input interrupt level	High
	RESUME		Reset power-down and error mode of processor *n*	High
	RSTRUN		Start processor *n* after reset (SMP systems only)	High
	RSTVEC[31:12]		Always zero	-
	INDEX[3:0]		CPU index	-
	PWDSETADDR		In power-down/error mode, shift PC to nPC and set PWDNEWADDR to PC.	High
	PWDNEWADDR [31:2]		New PC value used with PWDSETADDR	-
	FORCEERR		Force CPU into error mode	High
CPURUN[]	N/A	Input	If position n in this vector is set to '1', processor n will be started after reset. Otherwise processor n will go into power-down. This signal is only used if VHDL generic extrun is /= 0.	High

* see GRLIB IP Library User's Manual

74.8 Library dependencies

Table 1343 shows libraries that should be used when instantiating the core.

*Table 1343.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	LEON3	Signals, component	Signals and component declaration

74.9 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.leon3.all;
```

```
entity irqmp_ex is
  port (
    clk : in std_ulogic;
    rstn : in std_ulogic;

    ...  -- other signals
    );
end;

architecture rtl of irqmp_ex is
  constant NCPU : integer := 4;

  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);
  signal ahbsi : ahb_slv_in_type;

  -- GP Timer Unit input signals
  signal irqi   : irq_in_vector(0 to NCPU-1);
  signal irqo   : irq_out_vector(0 to NCPU-1);

  -- LEON3 signals
  signal leon3i : l3_in_vector(0 to NCPU-1);
  signal leon3o : l3_out_vector(0 to NCPU-1);

begin

  -- 4 LEON3 processors are instantiated here
  cpu : for i in 0 to NCPU-1 generate
    u0 : leon3s generic map (hindex => i)
    port map (clk, rstn, ahbmi, ahbmo(i), ahbsi,
irqi(i), irqo(i), dbgi(i), dbgo(i));
  end generate;

  -- MP IRQ controller
  irqctrl0 : irqmp
  generic map (pindex => 2, paddr => 2, ncpu => NCPU)
  port map (rstn, clk, apbi, apbo(2), irqi, irqo);
end
```

75 IRQ(A)MP - Multiprocessor Interrupt Controller with extended ASMP support

75.1 Overview

The AMBA system in GRLIB provides an interrupt scheme where interrupt lines are routed together with the remaining AHB/APB bus signals, forming an interrupt bus. Interrupts from AHB and APB units are routed through the bus, combined together, and propagated back to all units. The multiprocessor interrupt controller core is attached to the AMBA bus as an APB slave, and monitors the combined interrupt signals.

The interrupts generated on the interrupt bus are all forwarded to the interrupt controller. The interrupt controller prioritizes, masks and propagates the interrupt with the highest priority. The interrupt controller is configured at instantiation to implement one or several internal interrupt controllers. Each processor in a system can then be dynamically routed to one of the internal controllers. This allows safe Asymmetric Multiprocessing (ASMP) operation. For Symmetric Multiprocessor (SMP) operation, several processors can be routed to the same internal interrupt controller.

The IRQ(A)MP core is an extended version of the traditional multiprocessor interrupt controller. If a design does not need to have extended support for Asymmetric Multiprocessing, nor support for interrupt timestamping, it is recommended to use the IRQMP core instead.

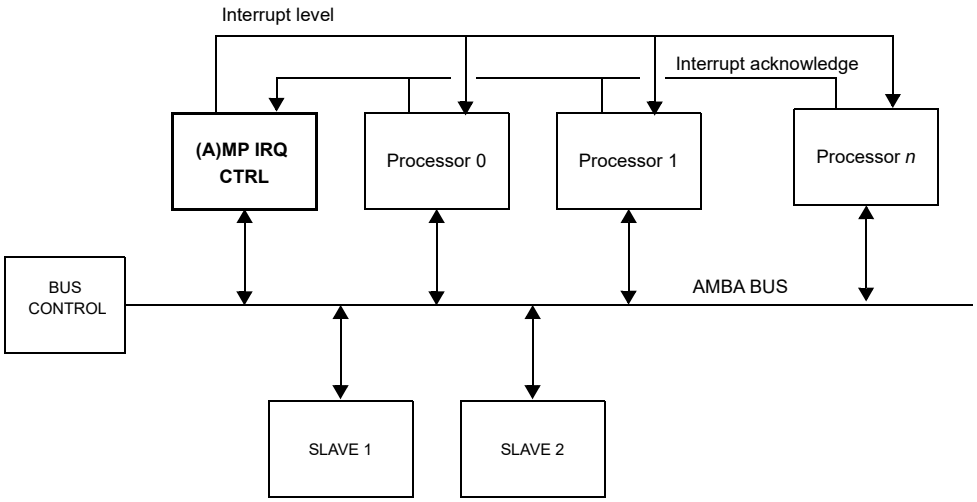


Figure 214. LEON multiprocessor system with Multiprocessor Interrupt controller

75.2 Operation

75.2.1 Support for Asymmetric Multiprocessing

Extended support for Asymmetric Multiprocessing (ASMP) is activated when the VHDL generic *nctrl* is > 1. Asymmetric Multiprocessing support means that parts of the interrupt controller are duplicated in order to provide safe ASMP operation. If the VHDL generic nctrl = 1 the core will have the same behavior as the normal IRQMP Multiprocessor interrupt controller core. If nctrl > 1, the core's register set will be duplicated on 4 KiB address boundaries. The core's register interface will also enable the use of three new registers, one Asymmetric Multiprocessing Control Register and two Interrupt Controller Select Registers.

Software can detect if the controller has been implemented with support for ASMP by reading the Asymmetric Multiprocessing Control register. If the field NCTRL is 0, the core was not implemented

with ASMP extensions. If the value of NCTRL is non-zero, the core has NCTRL+1 sets of registers with additional underlying functionality. From a software view this is equivalent to having NCTRL+1 interrupt controllers available and software can configure to which interrupt controller a processor should connect.

After system reset, all processors are connected to the first interrupt controller accessible at the core's base address. Software can then use the Interrupt Controller Select Registers to assign processors to other (internal) interrupt controllers. After assignments have been made, it is recommended to freeze the contents of the select registers by writing '1' to the lock bit in the Asymmetric Multiprocessing Control Register. The lock bit can be cleared by software by writing '0' to the bit.

When a software driver for the interrupt controller is loaded, the driver should check the Asymmetric Multiprocessing Control Register and Interrupt Controller Select Registers to determine to which controller the current processor is connected. After software has determined that it has been assigned to controller n, software should only access the controller with registers at offset 0x1000 * n. Note that the controllers are enumerated with the first controller being n = 0.

The processor specific registers (mask, force, interrupt acknowledge) can be read from all interrupt controllers. However the processor specific mask and interrupt acknowledge registers can only be written from the interrupt controller to which the processor is assigned. This also applies to individual bits in the Multiprocessor Status Register. Interrupt Force bits in a processor's Interrupt Force Register can only be cleared through the controller to which the processor is assigned. If the ICF field in the Asymmetric Multiprocessing Control Register is set to '1', all bits in all Interrupt Force Registers can be set, but not cleared, from all controllers. If the ICF field is '0' the bits in a processor's Interrupt Force register can only be set from the controller to which the processor is assigned.

75.2.2 Interrupt prioritization

The interrupt controller monitors interrupt 1 - 15 of the interrupt bus (APBI.PIRQ[15:1]). When any of these lines are asserted high, the corresponding bit in the interrupt pending register is set. The pending bits will stay set even if the PIRQ line is de-asserted, until cleared by software or by an interrupt acknowledge from the processor. The default behaviour for peripherals is to use pulsed interrupts (an interrupt line is asserted for one clock cycle to signal an interrupt).

Each interrupt can be assigned to one of two levels (0 or 1) as programmed in the interrupt level register. Level 1 has higher priority than level 0. The interrupts are prioritised within each level, with interrupt 15 having the highest priority and interrupt 1 the lowest. The highest interrupt from level 1 will be forwarded to the processor. If no unmasked pending interrupt exists on level 1, then the highest unmasked interrupt from level 0 will be forwarded. PIRQ[31:16] are not used by the IRQMP core.

Interrupts are prioritised at system level, while masking and forwarding of interrupts in done for each processor separately. Each processor in an multiprocessor system has separate interrupt mask and force registers. When an interrupt is signalled on the interrupt bus, the interrupt controller will prioritize interrupts, perform interrupt masking for each processor according to the mask in the corresponding mask register and forward the interrupts to the processors.

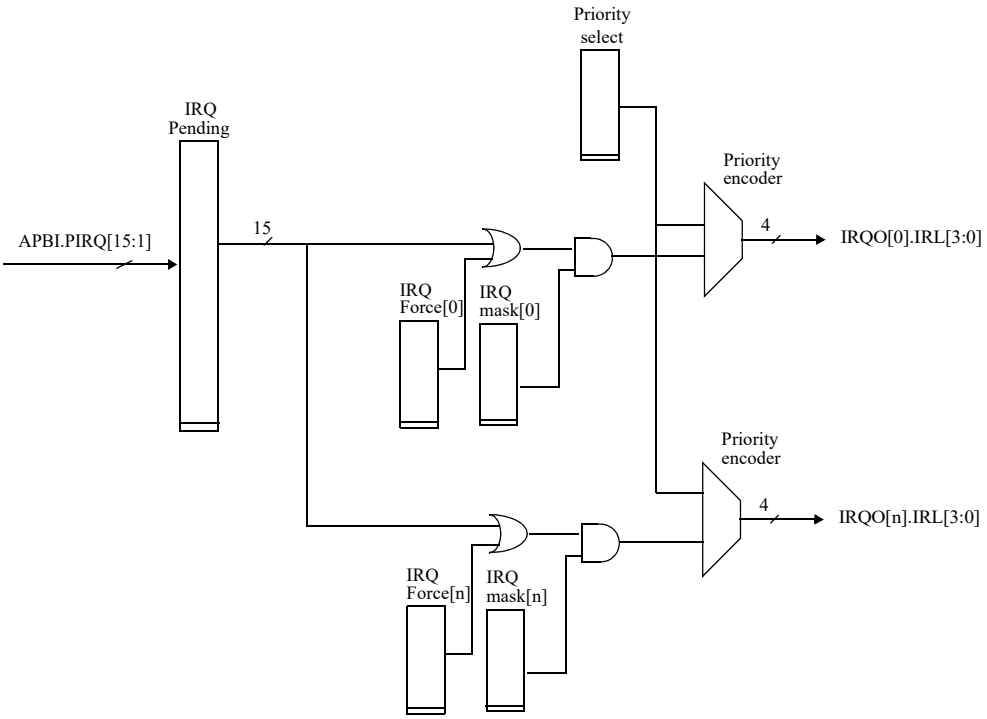


Figure 215. Interrupt controller block diagram

When a processor acknowledges the interrupt, the corresponding pending bit will automatically be cleared. Note that in a multiprocessor system, the bit in the pending register will be cleared as soon as one of the processors acknowledges the interrupt and interrupt broadcast functionality should be used for interrupts that need to be propagated to all processors. Interrupt can also be forced by setting a bit in the interrupt force register. In this case, the processor acknowledgement will clear the force bit rather than the pending bit. After reset, the interrupt mask register is set to all zeros while the remaining control registers are undefined. Note that interrupt 15 cannot be maskable by the LEON processor and should be used with care - most operating systems do not safely handle this interrupt.

75.2.3 Extended interrupts

The AHB/APB interrupt consist of 32 signals ([31:0]), while the IRQMP only uses lines 1 - 15 in the nominal mode. To use the additional 16 interrupt lines (16-31), extended interrupt handling can be enabled by setting the VHDL generic *eirq* to a value between 1 - 15. The interrupt lines 16 - 31 will then also be handled by the interrupt controller, and the interrupt pending and mask registers will be extended to 32 bits. Since the processor only has 15 interrupt levels (1 - 15), the extended interrupts will generate one of the regular interrupts, indicated by the value of the *eirq* generic. When the interrupt is taken and acknowledged by the processor, the regular interrupt (*eirq*) and the extended interrupt pending bits are automatically cleared. The extended interrupt acknowledge register will identify which extended interrupt that was most recently acknowledged. This register can be used by software to invoke the appropriate interrupt handler for the extended interrupts. When VHDL generic *irqmap* has a value of 3, support for 64 AHB/APB interrupts lines are enabled. Interrupt 32 - 63 are not handled by the interrupt controller and therefor needs to be remapped to one of the interrupt 1 - 31.

75.2.4 Processor status monitoring

The processor status can be monitored through the Multiprocessor Status Register. The STATUS field in this register indicates if a processor is in power-down (‘1’) or running (‘0’). A processor can be made running by writing a ‘1’ to its status field. After reset, all processors except processor 0 are in power-down (can be changed using the functionality associated with the *extrun* VHDL generic).

When the system is properly initialized, processor 0 can start the remaining processors by writing to their STATUS bits.

The core can be implemented with support for specifying the processor reset start address dynamically. Please see section 75.2.10 for further information.

75.2.5 Interrupt broadcasting

The Broadcast Register is activated when the generic *ncpu* is > 1. An incoming irq that has its bit set in the Broadcast Register is propagated to the force register of *all* CPUs instead of to the Pending Register. This can be used to implement a timer that fires to all CPUs with that same irq.

75.2.6 Interrupt timestamping description

Support for interrupt timestamping is implemented when the VHDL generic *tstamp* is > 0.

Interrupt timestamping is controlled via the Interrupt Timestamp Control register(s). Each Interrupt Timestamp Control register contains a field (TSTAMP) that contains the number of timestamp registers sets that the core implements. A timestamp register sets consist of one Interrupt Timestamp Counter register, one Interrupt Timestamp Control register, one Interrupt Assertion Timestamp register and one Interrupt Acknowledge Timestamp register.

Software enables timestamping for a specific interrupt via a Interrupt Timestamp Control Register. When the selected interrupt line is asserted, software will save the current value of the interrupt timestamp counter into the Interrupt Assertion Timestamp register and set the S1 field in the Interrupt Timestamp Control Register. When the processor acknowledges the interrupt, the S2 field of the Interrupt Timestamp Control register will be set and the current value of the timestamp counter will be saved in the Interrupt Acknowledge Timestamp Register. The difference between the Interrupt Assertion timestamp and the Interrupt Acknowledge timestamp is the number of system clock cycles that was required for the processor to react to the interrupt and divert execution to the trap handler.

The core can be configured to stamp only the first occurrence of an interrupt or to continuously stamp interrupts. The behavior is controlled via the Keep Stamp (KS) field in the Interrupt Timestamp Control Register. If KS is set, only the first assertion and acknowledge of an interrupt is stamped. Software must then clear the S1 and S2 fields for a new timestamp to be taken. If Keep Stamp is disabled (KS field not set), the controller will update the Interrupt Assertion Timestamp Register every time the selected interrupt line is asserted. In this case the controller will also automatically clear the S2 field and also update the Interrupt Acknowledge Timestamp register with the current value when the interrupt is acknowledged.

For controllers with extended ASMP support, each internal controller has a dedicated set of Interrupt timestamp registers. This means that the Interrupt Acknowledge Timestamp Register(s) on a specific controller will only be updated if and when the processor connected to the controller acknowledges the selected interrupt. The Interrupt Timestamp Counter is shared by all controllers and will be incremented when an Interrupt Timestamp Control register has the ITSEL field set to a non-zero value.

75.2.7 Interrupt timestamping usage guidelines

Note that KS = ‘0’ and a high interrupt rate may cause the Interrupt Assertion Timestamp register to be updated (and the S2 field reset) before the processor has acknowledged the first occurrence of the interrupt. When the processor then acknowledges the first occurrence, the Interrupt Acknowledge Timestamp register will be updated and the difference between the two Timestamp registers will not show how long it took the processor to react to the first interrupt request. If the interrupt frequency is expected to be high it is recommended to keep the first stamp (KS field set to ‘1’) in order to get reliable measurements. KS = ‘0’ should not be used in systems that include cores that use level interrupts, the timestamp logic will register each cycle that the interrupt line is asserted as an interrupt.

In order to measure the full interrupt handling latency in a system, software should also read the current value of the Interrupt Timestamp Counter when entering the interrupt handler. In the typical case,

a software driver's interrupt handler reads a status register and then determines the action to take. Adding a read of the timestamp counter before this status register read can give an accurate view of the latency during interrupt handling.

The core listens to the system interrupt vector when reacting to interrupt line assertions. This means that the Interrupt Assertion Timestamp Register(s) will not be updated if software writes directly to the pending or force registers. To measure the time required to serve a forced interrupt, read the value of the Interrupt Timestamp counter before forcing the interrupt and then read the Interrupt Acknowledge Timestamp and Interrupt Timestamp counter when the processor has reacted to the interrupt.

75.2.8 Watchdog

Support for watchdog inputs is implemented when the VHDL generic *wdogen* > 0, the number of watchdog input is determined by the VHDL generic *nwdog*.

The core can be implemented with support for asserting a bit in the controller's Interrupt Pending Register when an external watchdog signal is asserted. This functionality can be used to implement a sort of soft watchdog for one or several processor cores. The controller's Watchdog Control Register contains a field that shows the number of external watchdog inputs supported and fields for configuring which watchdog inputs that should be able to assert a bit in the Interrupt Pending Register. The pending register will be assigned in each cycle that a selected watchdog input is high. Therefore it is recommended that the watchdog inputs are connected to sources which send a one clock cycle long pulse when a watchdog expires. Otherwise software should make sure that the watchdog signal is deasserted before re-enabling interrupts during interrupt handling.

For controllers with extended ASMP support, each internal controller has a dedicated Watchdog Control register. Assertion of a watchdog input will only affect the pending register on the internal interrupt controllers that have enabled the watchdog input in their Watchdog Control Register.

75.2.9 Interrupt (re)map functionality

The interrupt controller can optionally be implemented (as an alternative to the two-interrupt levels scheme) with functionality to allow dynamic remapping between bus interrupt lines and interrupt controller interrupt lines. If the design includes this functionality then switch-logic will be placed on the incoming interrupt vector from the AMBA bus before the IRQ pending register. The Interrupt map registers will be available starting at offset 0x300 from the interrupt controller's base address.

The interrupt map registers contain one field for each bus interrupt line in the system. The value within this field determines to which interrupt controller line the bus interrupt line is connected. In case several bus interrupt lines are mapped to the same controller interrupt line (several fields in the Interrupt map registers have the same value) then the bus interrupt lines will be OR:ed together.

Note that if bus interrupt line X is remapped to controller interrupt line Y then bit Y of the pending register will be set when a peripheral asserts interrupt X. Remapping interrupt lines via the Interrupt map registers has the same effect as changing the interrupt assignments in the RTL code.

75.2.10 Dynamic processor reset start address

When the bootreg generic is set, registers are added to allow starting a halted CPU from an arbitrary 8 byte aligned entry point. The CPU can be started with the same register write as when the entry point is written, or the CPU can be started later using the regular multiprocessor status register bit.

An error register is also added to allow monitoring CPUs for error mode, and to allow forcing a specific CPU into error mode. This can be used to monitor and re-boot CPUs without resetting the system.

A read-only bit in the multiprocessor status register can be read to see if the bootreg functionality has been configured in.

75.3 Registers

The core is controlled through registers mapped into APB address space. The number of implemented registers depends on the number of processors in the multiprocessor system. The number of accessible register sets depend on the value of the NCTRL field in the Asymmetric Multiprocessing Control Register. The register set for controller n is accessed at offset 0x1000*n.

In order to make the boot registers available in the lower 256-byte space that is in legacy mappings, the registers are mapped into space that becomes unused when the number of processors is 8 or lower. If the number of CPUs is higher than 8, then the registers are only available in the higher space and a larger APB address mapping must be used to make them available.

*Table 1344.*Interrupt Controller registers

APB address offset	Register
0x000	Interrupt level register
0x004	Interrupt pending register
0x008	Interrupt force register (NCPU = 0)
0x00C	Interrupt clear register
0x010	Multiprocessor status register
0x014	Broadcast register
0x018	Error mode register
0x01C	Watchdog control register
0x020	Asymmetric multiprocessing control register
0x024	Interrupt controller select register for processor 0 - 7
0x028	Interrupt controller select register for processor 8 - 15
0x02C - 0x03C	Reserved
0x040	Processor interrupt mask register
0x044	Processor 1 interrupt mask register
0x040 + 0x4 * *n*	Processor *n* interrupt mask register
0x060 + 0x4 * *n*	Alias for processor *n* boot address register if NCPU < 9
0x080	Processor interrupt force register
0x084	Processor 1 interrupt force register
0x080 + 0x4 * *n*	Processor *n* interrupt force register
0x0C0	Processor extended interrupt acknowledge register
0x0C4	Processor 1 extended interrupt acknowledge register
0x0C0 + 0x4 * *n*	Processor *n* extended interrupt acknowledge register
0x100	Interrupt timestamp counter register
0x104	Interrupt timestamp 0 control register
0x108	Interrupt assertion timestamp 0 register
0x10C	Interrupt acknowledge timestamp 0 register
0x100 + 0x10 * *n*	Interrupt timestamp counter register (mirrored in each set)
0x104 + 0x10 * *n*	Interrupt timestamp *n* control register
0x108 + 0x10 * *n*	Interrupt assertion timestamp *n* register
0x10C + 0x10 * *n*	Interrupt acknowledge timestamp *n* register
0x200 + 0x4* *n*	Processor n boot address register
0x300 + 0x4 * *n*	Interrupt map register *n*

75.3.1 Interrupt Level Register

*Table 1345.*0x000 - ILEVEL - Interrupt Level Register

31 16	15 1	0
RESERVED	IL[15:1]	R
0	NR	0
r	rw	r

31:16 Reserved

15:1 Interrupt Level n (IL[n]) - Interrupt level for interrupt n

0 Reserved

75.3.2 Interrupt Pending Register

*Table 1346.*0x004 - IPEND - Interrupt Pending Register

31 16	15 1	0
EIP[31:16]	IP[15:1]	R
0	0	0
rw	rw	r

31:16 Extended Interrupt Pending n (EIP[n])

15:1 Interrupt Pending n (IP[n]) - Interrupt pending for interrupt n

0 Reserved

75.3.3 Interrupt Force Register (NCPU = 0)

*Table 1347.*0x008 - IFORCE0 - Interrupt Force Register (NCPU = 0)

31 16	15 1	0
RESERVED	IF[15:1]	R
0	0	0
r	rw	r

31:16 Reserved

15:1 Interrupt Force n (IF[n]) - Force interrupt nr n.

0 Reserved

75.3.4 Interrupt Clear Register

*Table 1348.*0x00C - ICLEAR - Interrupt Clear Register

31 16	15 1	0
EIC[31:16]	IC[15:1]	R
0	0	0
w	w	r

31:16 Extended Interrupt Clear n (EIC[n])

15:1 Interrupt Clear n (IC[n]) - Writing ‘1’ to IC[n] will clear interrupt n

0 Reserved

75.3.5 Multiprocessor Status Register

*Table 1349.*0x010 - MPSTAT - Multiprocessor Status Register

31 28	27	26	25 20	19 16	15 0
NCPU	BA	ER	RESERVED	EIRQ	STATUS[15:0]
*	*	0		*	*
r	r	r		r	rw

31:28 Number of CPUs (NCPU) - Number of CPUs in the system - 1

27 Broadcast Available (BA) - Set to '1' if NCPU > 0.

26 Extended boot registers available (ER). Set to '1' if bootreg generic is 1.

25:20 Reserved

19:16 Extended IRQ (EIRQ) - Interrupt number (1 - 15) used for extended interrupts. Fixed to 0 if extended interrupts are disabled.

15:0 Power-down status of CPU[n] (STATUS[n]) - '1' = power-down, '0' = running. Write STATUS[n] with '1' to start processor n.

75.3.6 Broadcast Register (NCPU > 0)

*Table 1350.*0x014 - BRDCST - Broadcast Register (NCPU > 0)

31 16	15 1	0
RESERVED	BM15:1]	R
0	0	0
r	rw	r

31:16 Reserved

15:1 Broadcast Mask n (BM[n]) - If BM[n] = '1' then interrupt n is broadcasted (written to the Force Register of all CPUs), otherwise standard semantic applies (Pending register)

0 Reserved

75.3.7 Error Mode Status Register

*Table 1351.*0x018 - ERRSTAT - Error Mode Status Register

31 28	27 26	20 19	16 15	0
RESERVED			ERRMODE[15:0]	
0			*	
r			rw	

31:16 Reserved

15:0 Read: Error mode status of CPU[n] (STATUS[n]) - '1' = error mode, '0' = other (debug/run/power-down).

Write: Force CPU[n] into error mode

Register is read-only if bootreg generic is 0..

75.3.8 Watchdog Control Register (NCPU > 0)

*Table 1352.*0x01C - WDOGCTRL - Watchdog Control Register (NCPU > 0)

31 27	26 20	19 16	15 0
NWDOG	Reserved	WDOGIRQ	WDOGMSK
*	0	NR	0
r	r	rw	rw

31:27 Number of watchdog inputs (NWDOG) - Number of watchdog inputs that the core supports.

26:20 Reserved

19:16 Watchdog interrupt (WDOGIRQ) - Selects the bit in the pending register to set when any line watchdog line selected by the WDOGMSK field is asserted.

15:0 Watchdog Mask n (WDOGMSK[n]) - If WDOGMSK[n] = '1' then the assertion of watchdog input n will lead to the bit selected by the WDOGIRQ field being set in the controller's Interrupt Pending Register.

75.3.9 Asymmetric Multiprocessing Control Register

*Table 1353.*0x020 - ASMPCTRL - Asymmetric Multiprocessing Control Register

31 28	27 2	1	0
NCTRL	RESERVED	ICF	L
*	0	0	0
r	r	rw	rw

31:28 Number of internal controllers (NCTRL) - NCTRL + 1 is the number of internal interrupt controllers available.

27:2 Reserved

1 Inter-controller Force (ICF) - If this bit is set to '1' all Interrupt Force Registers can be set from any internal controller. If this bit is '0', a processor's Interrupt Force Register can only be set from the controller to which the processor is connected. Bits in an Interrupt Force Register can only be cleared by the controller or by writing the Interrupt Force Clear field on the controller to which the processor is connected.

0 Lock (L) - If this bit is written to '1', the contents of the Interrupt Controller Select registers is frozen. This bit can only be set if NCTRL > 0.

75.3.10 Interrupt Controller Select Register for Processors 0 - 7 (NCTRL > 0)

*Table 1354.*0x024 - ICLSELR0 - Interrupt Controller Select Register for Processors 0 -7 (NCTRL > 0)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
ICSEL0	ICSEL1	ICSEL2	ICSEL3	ICSEL4	ICSEL5	ICSEL6	ICSEL7
0	0	0	0	0	0	0	0
rw	rw	rw	rw	rw	rw	rw	rw

31:0 Interrupt controller select for processor n (ICSEL[n]) - The nibble ICSEL[n] selects the (internal) interrupt controller to connect to processor n.

75.3.11 Interrupt Controller Select Register for Processors 8 - 15 (NCTRL > 0)

*Table 1355.*0x028 - ICSELR1 - Interrupt Controller Select Register for Processors 8 - 15 (NCTRL > 0)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
ICSEL8	ICSEL9	ICSEL10	ICSEL11	ICSEL12	ICSEL13	ICSEL14	ICSEL15
0	0	0	0	0	0	0	0
rw	rw	rw	rw	rw	rw	rw	rw

31:0 Interrupt controller select for processor n (ICSEL[n]) - The nibble ICSEL[n] selects the (internal) interrupt controller to connect to processor n.

75.3.12 Processor Interrupt Mask Register

*Table 1356.*0x040,... - PIMASK - Processor Interrupt Mask Register

31 16	15 1	0
EIM[31:16]	IM15:1]	R
0	0	0
rw	rw	r

31:16 Extended Interrupt Mask n (EIC[n]) - Interrupt mask for extended interrupts

15:1 Interrupt Mask n (IM[n]) - If IM[n] = ‘0’ then interrupt n is masked, otherwise it is enabled.

0 Reserved

75.3.13 Processor Interrupt Force Register (NCPU > 0)

*Table 1357.*0x080 - PCFORCE - Processor Interrupt Force Register (NCPU > 0)

31 17	16	15 1	0
IFC[15:1]	R	IF15:1]	R
0	0	0	0
wc	r	rw*	r

31:17 Interrupt Force Clear n (IFC[n]) - Interrupt force clear for interrupt n

16 Reserved

15:1 Interrupt Force n (IF[n]) - Force interrupt nr n

0 Reserved

75.3.14 Extended Interrupt Acknowledge Register

*Table 1358.*0x0C0,... PEXTACK - Extended Interrupt Acknowledge Register

31 5	4 0
RESERVED	EID[4:0]
0	0
r	r

31:5 Reserved

4:0 Extended interrupt ID (EID) - ID (16-31) of the most recent acknowledged extended interrupt

If this field is 0, and support for extended interrupts exist, the last assertion of interrupt *eirq* was not the result of an extended interrupt being asserted. If interrupt *eirq* is forced, or asserted, this field will be cleared unless one, or more, of the interrupts 31 - 16 are enabled and set in the pending register.

75.3.15 Interrupt Timestamp Counter Register

*Table 1359.*0x100,110 - TCNT - Interrupt Timestamp Counter register

31 0
TCNT
0
r

31:0 Timestamp Counter (TCNT) - Current value of timestamp counter. The counter increments whenever a TSISEL field in a Timestamp Control Register is non-zero. The counter will wrap to zero upon overflow and is read only.

75.3.16 Timestamp N Control Register

*Table 1360.*0x1n4 - ITSTMPCn - Timestamp n Control Register

31 27	26	25	24 6	5	4 0
TSTAMP	S1	S2	RESERVED	KS	TSISEL
*	0	0	0	0	0
r	wc	wc	r	rw	rw

31:27 Number of timestamp register sets (TSTAMP) - The number of available timestamp register sets.

26 Assertion Stamped (S1) - Set to ‘1’ when the assertion of the selected line has received a timestamp. This bit is cleared by writing ‘1’ to its position. Writes of ‘0’ have no effect.

25 Acknowledge Stamped (S2) - Set to ‘1’ when the processor acknowledge of the selected interrupt has received a timestamp. This bit can be cleared by writing ‘1’ to this position, writes of ‘0’ have no effect. This bit can also be cleared automatically by the core, see description of the KS field below.

24:6 RESERVED

5 Keep Stamp (KS) - If this bit is set to ‘1’ the core will keep the first stamp value for the first interrupt until the S1 and S2 fields are cleared by software. If this bit is set to ‘0’ the core will time stamp the most recent interrupt. This also has the effect that the core will automatically clear the S2 field whenever the selected interrupt line is asserted and thereby also stamp the next acknowledge of the interrupt.

4:0 Timestamp Interrupt Select (TSISEL) - This field selects the interrupt line (0 - 31) to timestamp.

75.3.17 Interrupt Assertion Timestamp Register

*Table 1361.*0x1n8 - ITSTMPASn - Interrupt Assertion Timestamp register N

31	0
TASSERTION	
0	
r	

31:0 Timestamp of Assertion (TASSERTION) - The current Timestamp Counter value is saved in this register when timestamping is enabled and the interrupt line selected by TSISEL is asserted.

75.3.18 Interrupt Acknowledge Timestamp Register

*Table 1362.*0x1nC - ITSTMPASn - Interrupt Acknowledge Timestamp register N

31	0
TACKNOWLEDGE	
0	
r	

31:0 Timestamp of Acknowledge (TACKNOWLEDGE) - The current Timestamp Counter value is saved in this register when timestamping is enabled, the Acknowledge Stamped (S2) field is ‘0’, and the interrupt selected by TSISEL is acknowledged by a processor connected to the interrupt controller.

75.3.19 Processor N Boot Address Register

*Table 1363.*0x200 + 0x4* n - BADDRn - Processor n Boot Address register

31 28	27 26	20 19	16 15	3	2 1	0
BOOTADDR[31:3]					RES	AS
-					-	-
w					-	w

31:3 Entry point for booting up processor N, 8-byte aligned

2:1 Reserved (write 0)

0 Start processor immediately after setting address

75.3.20 Interrupt Map Register N

*Table 1364.*0x300 + IRQMAPn - Interrupt map register n

31 24	23 16	15 8	7 0
IRQMAP[n*4]	IRQMAP[n*4+1]	IRQMAP[n*4+2]	IRQMAP[n*4+3]
n.n	n.4+1	n.4+2	n.4+3
rw	rw	rw	rw

b+7 : b Interrupt map (IRQMAP) - If the core has been implemented to support interrupt mapping then the Interrupt map register at offset 0x300 + 4*n specifies the mapping for interrupt lines 4*n to 4*n+3. The bus interrupt line 4*n+x will be mapped to the interrupt controller interrupt line specified by the value of IRQMAP[n*4+x].

75.4 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x00D (same as IRQMP core). For description of vendor and device identifiers see GRLIB IP Library User’s Manual.

75.5 Implementation

75.5.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

75.6 Configuration options

Table 1365 shows the configuration options of the core (VHDL generics).

*Table 1365.*Configuration options

Generic	Function	Allowed range	Default
pindex	Selects which APB select signal (PSEL) that will be used to access the interrupt controller	0 to NAPBSLV-1	0
paddr	The 12-bit MSB APB address	0 - 16#FFF#	0
pmask	The APB address mask. The mask determines the size of the memory area occupied by the core. The minimum required memory area based on the *nctrl* VHDL generic gives (nctrl : pmask) = 1 : 16#FFF#, 2: 16#FE0#, 3-4 : 16#FC0#, 5-8 : 16#F80#, 9-16 : 16#F00#. Note that even with nctrl = 1 the core may require a larger area than 256 bytes if the core has been implemented with support for timestamping and/or dynamic reset addresses.	0 - 16#FFF#	16#FFF#
ncpu	Number of processors in multiprocessor system	1 to 16	1
eirq	Enable extended interrupts	0 - 15	0
nctrl	Asymmetric multiprocessing system extension. This generic defines the number of internal interrupt controllers that will be implemented in the core.	1 - 16	1
tstamp	Interrupt timestamping. If this generic is non-zero the core will include a timestamp counter and *tstamp* set(s) of interrupt timestamp register(s).	0 - 16	0
wdogen	Enable watchdog inputs. If this generic is set to 1 the core will include logic to assert a selected interrupt when a watchdog input is asserted.	0 - 1	0
nwdog	Number of watchdog inputs	1 - 16	1
dynrstaddr	Deprecated feature, must be set to 0	0 - 0	0
rstaddr	Deprecated feature, must be set to 0	0 - (2^{20}-1)	0
extrun	Use external run vector. If this generic is set to 1 the start of processors after reset will be controlled via the input signal cpurun. If this generic is set to 0, CPU 0 will be started after reset and the other CPUs will be put in power-down mode. This requires that the SMP VHDL generic on the LEON entity is nonzero.	0 - 1	0
irqmap	Enable interrupt (re-)map registers. If irqmap is set to 0 then interrupt map functionality is disabled. If irqmap is nonzero then (irqmap + eirq) = 1 includes map registers for bus interrupt lines 0 - 15. If (irqmap + eirq) > 1 then interrupt map registers are available for bus interrupt lines 0 - 31. When irqmap = 3 then support for 64 interrupt sources is enabled and interrupt map registers are available for bus interrupt lines 0 - 63.	0 - 3	0

*Table 1365.*Configuration options

Generic	Function	Allowed range	Default
exttimer	Use external timer input *timer*. The external timer replaces the internal time stamp counter. The counter is no longer started based on the value of the IRQ sel field. Users must ensure that the timer input is toggling when-they want to do timestamps	0 - 1	0
bootreg	Enable boot address register and error mode register.	0 - 1	1

75.7 Signal descriptions

Table 1366 shows the interface signals of the core (VHDL ports).

*Table 1366.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
IRQI[n]	INTACK	Input	Processor *n* Interrupt acknowledge	High
	IRL[3:0]		Processor *n* interrupt level	High
	PWD		Processor *n* in power down mode	High
	FPEN		Unused	-
	ERR		Processor *n* in error mode	High
IRQO[n]	IRL[3:0]	Output	Processor *n* Input interrupt level	High
	RESUME		Reset power-down and error mode of processor *n*	High
	RSTRUN		Start processor *n* after reset (SMP systems only)	High
	RSTVEC[31:12]		Always zero	-
	INDEX[3:0]		CPU index	High
	PWDSETADDR		In power-down/error mode, shift PC to nPC and set PWDNEWADDR to PC.	High
	PWDNEWADDR [31:2]		New PC value used with PWDSETADDR	-
	FORCEERR		Force CPU into error mode	High
WDOG[]	N/A	Input	Watchdog input signals	High
CPURUN[]	N/A	Input	If position n in this vector is set to ‘1’, processor n will be started after reset. Otherwise processor n will go into power-down. This signal is only used if VHDL generic extrun is /= 0.	High
TIMER[]	N/A	Input	Timer value, used then VHDL generic exttimer /=0	-
RSTMAP	N/A	Input	Reset value for IRQ mapping register (only used when 64 interrupt sources is supported). Bit[4:0] = mapping for IRQ0 Bit[9:5] = mapping for IRQ1 ...	-

* see GRLIB IP Library User’s Manual

75.8 Library dependencies

Table 1367 shows libraries that should be used when instantiating the core.

*Table 1367.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	LEON3	Signals, component	Signals and component declaration

75.9 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.leon3.all;

entity irqamp_ex is
  port (
    clk : in std_ulogic;
    rstn : in std_ulogic;

    ...  -- other signals
    );
end;

architecture rtl of irqamp_ex is
  constant NCPU : integer := 4;

  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);
  signal ahbsi : ahb_slv_in_type;

  -- GP Timer Unit input signals
  signal irqi   : irq_in_vector(0 to NCPU-1);
  signal irqo   : irq_out_vector(0 to NCPU-1);

  -- LEON3 signals
  signal leon3i : l3_in_vector(0 to NCPU-1);
  signal leon3o : l3_out_vector(0 to NCPU-1);

begin

  -- 4 LEON3 processors are instantiated here
  cpu : for i in 0 to NCPU-1 generate
    u0 : leon3s generic map (hindex => i)
    port map (clk, rstn, ahbmi, ahbmo(i), ahbsi,
irqi(i), irqo(i), dbgi(i), dbgo(i));
  end generate;

  -- MP IRQ controller
  irqctrl0 : irqamp
  generic map (pindex => 2, paddr => 2, ncpu => NCPU, nctrl => NCPU)
  port map (rstn, clk, apbi, apbo(2), irqi, irqo);
end
```

76 L2C - Level 2 Cache controller

76.1 Overview

The L2C implements a Level-2 cache for processors with AHB interfaces. The L2C works as an AHB to AHB/AXI bridge, caching data that is read or written via the bridge. The cache is a unified cache and in a system with LEON processors, data may exist in the Level-1 and Level-2 cache, or only in the Level-1 or Level-2 cache. A front-side AHB interface is connected to the processor bus, while a backend AHB/AXI interface is connected to the memory bus. Both front-side and backend buses can be individually configured to 32, 64 or 128 bits data width. The front-side bus and the backend bus must be clocked with the same clock. Figure 216 shows a system block diagram for the cache controller.

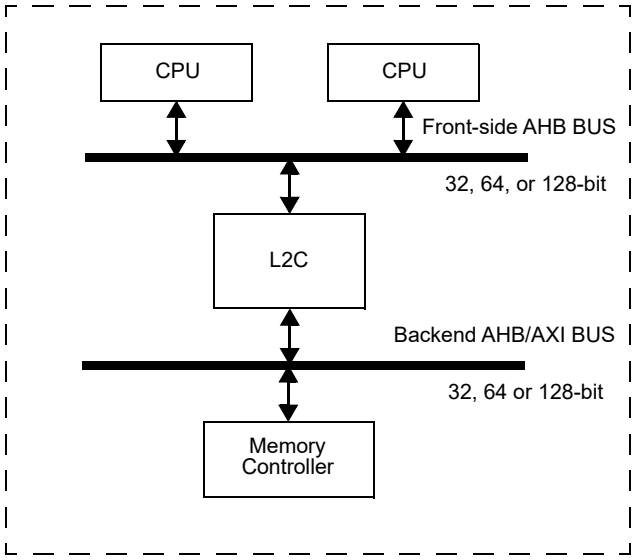


Figure 216. Block diagram

76.2 Configuration

The Level-2 cache can be configured as direct-mapped or multi-way with associativity 2, 3 or 4. The replacement policy for a multi-way configuration can be configured as: LRU (least-recently-used), pseudo-random or master-index (where the way to replace is determined by the master index). The way size is configurable between 1 - 512 KiB with a line size of 32/64 bytes.

76.2.1 Replacement policy

The core can implements three different replacement policies: LRU (least-recently-used), (pseudo-) random and master-index. The LRU replacement policy is configured as default. With master-index replacement policy, master 0 would replace way 1, master 1 would replace way 2, and so on. For master indexes corresponding to a way number larger than the number of implemented ways, there are two options to determine which way to replace. One option is to map all these master indexes to a specific way. This is done by specifying this way in the index-replace field in the control register and selecting this option in the replacement policy field, also located in the control register. It is not allowed to select a locked way in the index-replace field. The second option is to replace way = ((master index) modulus (number of ways)). This option can be selected in the replacement policy field, but is only allowed with multi-way associativity 2 or 4.

76.2.2 Write policy

The cache can be configured to operate as write-through or copy-back cache. Before changing the write policy to write-through, the cache has to be disabled and flushed (to write back dirty cache lines to memory). This can be done by setting the Cache disable bit when issuing a flush all command. The write policy is controlled via the cache control register. More fine-grained control can also be obtained by enabling the MTRR registers (see text below).

76.2.3 Memory type range registers

The memory type range registers (MTRR) are used to control the cache operation with respect to the address. Each MTRR can define an area in memory to be uncached, write-through or write-protected. The MTRR consist of a 14-bit address field, a 14-bit mask and two 2-bit control fields. The address field is compared to the 14 most significant bits of the cache address, masked by the mask field. If the unmasked bits are equal to the address, an MTRR hit is declared. The cache operation is then performed according to the control fields (see register descriptions). If no hit is declared or if the MTRR is disabled, cache operation takes place according to the cache control register. The number of MTRRs is configurable through the *mtrr* VHDL generic. When changing the value of any MTRR register, cache must be disabled and flushed (This can be done by setting the Cache disable bit when issue a flush all command).

Note that the write-protection provided via the MTRR registers is enforced even if the cache is disabled.

76.2.4 Cachability

The core uses a VHDL generic CACHED to determine which address range is cachable. Each bit in this 16-bit value defines the cachability of a 256 Mbyte address block on the AMBA AHB bus. A value of 16#00F3# will thus define cachable areas in 0 - 0x20000000 and 0x40000000 - 0x80000000. When the VHDL generic CACHED is 0, the cachable areas is defined by the plug&play information on the backend bus. When implemented with a AXI backend bus the cachability needs to be defined with the VHDL generic CACHED. The core can also be configured to use the HPROT signal to override the cachable area defined by VHDL generic CACHED. A access can only be redefined as non-cachable by the HPROT signal. See table 1368 for information on how HPROT can change the access cachability within a cachable address area. The AMBA AHB signal HPROT[3] defines the access cacheable when active high and the AMBA AHB signal HPROT[2] defines the access bufferable when active high.

*Table 1368.*Access cachability using HPROT.

HPROT:	**non-cachable, non-bufferable**	**non-cachable, bufferable**	**cacheable**
Read hit	Cache access*	Cache access	Cache access
Read miss	Memory access	Memory access	Cache allocation and Memory access
Write hit	Cache and Memory access	Cache access	Cache access
Write miss	Memory access	Memory access	Cache allocation

* When the HPROT-Read-Hit-Bypass bit is set in the cache control register this will generate a Memory access.

76.2.5 Cache tag entry

Table 1369 show the different fields of the cache tag entry for a cache with set size equal to 1 kbyte. The number of bits implemented is depending on the cache configuration.

Table 1369. L2C Cache tag entry

31	10	9	8	7	6	5	4	0
TAG		Valid		Dirty		RES	LRU	

31 : 10	Address Tag (TAG) - Contains the address of the data held in the cache line.
9 : 8	Valid bits. When set, the corresponding sub-block of the cache line contains valid data. Valid bit 0 corresponds to the lower 16 bytes sub-block (with offset 1) in the cache line and valid bit 1 corresponds to the upper 16 bytes sub-block (with offset 0) in the cache line.
7 : 6	Dirty bits When set, this sub-block contains modified data.
5	RESERVED
4 : 0	LRU bits

76.2.6 AHB address mapping

The AHB slave interface occupies three AHB address ranges. The first AHB memory bar is used for memory/cache data access. The address and size of this bar is configured via VHDL generics. The second AHB memory bar is used for access to configuration registers and the diagnostic interface. This bar has a configurable address via VHDL generic but always occupies 4 MiB in the AHB address space. The last AHB memory bar is used to map the ioarea of the backend AHB bus (to access the plug&play information on that bus, not supported when AXI backend is selected). The address and size of the this bar is configured via VHDL generics.

76.2.7 Memory protection and Error handling

The ft VHDL generic enables the implementation of the Error Detection And Correction (EDAC) protection for the data and tag memory. One error can be corrected and two error can be detected with the use of a (39, 32, 7) BCH code. When implemented, the EDAC functionality can dynamically be enabled or disabled. Before being enabled the cache should be flushed. The dirty and valid bits fore each cache line is implemented with TMR. When EDAC error or backend AHB/AXI error or write-protection hit in a MTRR register is detected the error status register is updated to store the error type. The address which cause the error is also saved in the error address register. The error types is prioritised in the way that a uncorrected EDAC error will overwrite any other previously stored error in the error status register. In all other cases, the error status register has to be cleared before a new error can be stored. Each error type (correctable-, uncorrectable EDAC error, write-protection hit, backend AHB/AXI error) has a pending register bit. When set and this error is unmasked, a interrupt is generated. When uncorrectable error is detected in the read data the core will respond with a AHB error. AHB error response can also be enabled for a access that match a stored error in the error status register. Error detection is done per cache line. The core also provide a correctable error counter accessible via the error status register.

*Table 1370.*Cache action on detected EDAC error

Access/Error type	Cache-line not dirty	Cache-line dirty
Read, Correctable Tag error	Tag is corrected before read is handled, Error status is updated with a corretable error.	Tag is corrected before read is handled, Error status is updated with a corretable error.
Read, Uncorrectable Tag error	Cache-line invalidated before read is handled, Error status is updated with a corretable error.	Cache-line invalidated before read is handled, Error status is updated with a uncorrectable error. Cache data is lost.
Write, Correctable Tag error	Tag is corrected before write is handed, Error status is updated with a corretable error.	Tag is corrected before write is handled, Error status is updated with a corretable error.
Write, Uncorrectable Tag error	Cache-line invalidated before write is handled, Error status is updated with a correctable error.	Cache-line invalidated before write is handled, Error status is updated with a uncorrectable error. Cache data is lost.
Read, Correctable Data error	Cache-data is correted and updated, Error status is updated with a correctable error. AHB access is not affected.	Cache-data is correted and updated, Error status is updated with a correctable error. AHB access is not affected.
Read, Uncorrectable Data error	Cache-line is invalidated, Error status is updated with a correctable error. AHB access is terminated with retry.	Cache-line is invalidated, Error status is updated with a uncorrectable error. AHB access is terminated with error.
Write (<32-bit), Correctable Data error	Cache-data is correted and updated, Error status is updated with a correctable error. AHB access is not affected.	Cache-data is correted and updated, Error status is updated with a correctable error. AHB access is not affected.
Write (<32-bit), Uncorrectable Data error	Cache-line is re-fetched from memory, Error status is updated with a correctable error. AHB access is not affected.	Cache-line is invalidated, Error status is updated with a uncorrectable error. AHB access write data and cache data is lost.

76.2.8 Scrubber

When EDAC protection is implemented a cache scrubber is enabled. The scrubber is controlled via two register in the cache configuration interface. To scrub one specific cache line the index and way of the line is set in the scrub control register. To issue the scrub operation, the pending bit is set to 1. The scrubber can also be configured to continuously loop through and scrub each cache line by setting the enabled bit to 1. In this mode, the delay between the scrub operation on each cache line is determine by the scrub delay register (in clock cycles).

76.2.9 Locked way

One or more ways can be configured to be locked (not replaced). The number of way that should be locked is configured by the locked-way field in the control register. The way to be locked is starting with the uppermost way (for a 4-way associative cache way 4 is the first locked way, way 3 the second, and so on). After a way is locked, this way has to be flushed with the “way flush” function to update the tag match the desired locked address. During this “way flush” operation, the data can also be fetched from memory.

76.2.10 Data priming

Data can be loaded from one or two address ranges. Before triggering the priming operation, the start and stop address need to be configured. To specify if one or both address ranges should be loaded the respective enable bit (PSTART0/1.EN) need to be set. To trigger the operation, the pending bit (PSTART0.P) needs to be set to '1'. If only one address range should be loaded, the first set of priming register (PSTART0, PSTOP0) should be used. The cache lines are loaded from the start address to the stop address. When two address ranges should be loaded, one cache line from each area is loaded before moving to the next line in the address range. If the cache already contains the cache line speci-

fied to be loaded, the priming operation moves to the next line in the priming address range without fetching any data from memory but the LRU replacement information is updated.

76.3 Operation

76.3.1 Read

A cachable read access to the core results in a tag lookup to determine if the requested data is located in the cache memory. For a hit (requested data is in the cache) the data is read from the cache and no read access is issued to the memory. If the requested data is not in the cache (cache miss), the cache controller issue a read access to the memory controller to fetch the cache line including the requested data. The replacement policy determine which cache line in a multi-way configuration that should be replaced and its tag is updated. If the replaced cache line is modified (dirty) this data is stored in a write buffer and after the requested data is fetched from memory the replaced cache line is written to memory.

For a non-cachable read access to the cache, the cache controller can issue a single read access or a burst read access to fetch the data from memory. The access type is determine by how the cache is configured regarding hprot support and bypass line fetch in the access control register. The data is stored in a read buffer and the state of the cache is not modified in any way.

The cache will insert wait-states until the read access is determined to be a cache hit or miss. For a cache hit the data is then delivered. For a miss the cache can insert wait-states during the memory fetch or issue a AMBA SPLIT (depending on how the cache is configured). AMBA SPLIT response is only implemented in version 3 of the core.

76.3.2 Write

A cachable write access to the core results in a tag lookup to determine if the cache line is located in the cache. For a hit the cache line is updated. No access is issued to the memory for a copy-back configuration. When the core is configured as a write-through cache, each write access is also issued towards the memory. For a miss, the replacement policy determines which cache line in a multi-way configuration that should be replaced and updates its tag. If the replaced cache line is dirty, this is stored in a write buffer to be written back to the memory. The new cache line is updated with the data from the write access and for a non 128-bit access the rest of the cache line is fetched from memory. Last (when copy-back policy is used and the replaced cache line was marked dirty) the replaced cache line is written to memory. When the core is configured as a write-through cache, no cache lines are marked as dirty and no cache line needs to be written back to memory. Instead the write access is issued towards the memory as well. A new cache line is allocated on a miss for a cacheable write access independent of write policy (copy-back or write-through).

For a non-cachable write access to the core, the data is stored in a write buffer and the cache controller issue single write accesses to write the data to memory. The state of the cache is unmodified during this access.

The cache can accept a non sub-word write hit access every clock cycle. When the cache is unable to accept a new write access the cache inserts wait-states or issue a AMBA SPLIT response depending on how the cache is configured. AMBA SPLIT response is only implemented in version 3 of the core.

76.3.3 Cache flushing

The cache can be flushed by accessing a cache flush register. There is three flushing modes: invalidate (reset valid bits), write back (write back dirty cache lines to memory, but no invalidation of the cache content) and flush (write back dirty cache lines to memory and invalidate the cache line). The flush command can be applied to the entire cache, one way or to only one cache line. The cache line to be flushed can be addresses in two ways: direct address (specify way and line address) and memory address (specify which memory address that should be flushed in the cache. The controller will make a cache lookup for the specified address and on a hit, flush that cache line). When the entire cache is

flushed the Memory Address field should be set to zero. Invalidate a cache line takes 5 clock cycles. If the cache line needs to be written back to memory one additional clock cycle is needed plus the memory write latency. When the whole cache is flushed the invalidation of the first cache line takes 5 clock cycles, after this one line can be invalidate each clock cycle. When a cache line needs to be written back to memory this memory access will be stored in a access buffer. If the buffer is full the invalidation of the next cache line is stall until a slot in the buffer has opened up. If the cache also should be disabled after the flush is complete, it is recommended to set the cache disable bit together with the flush command instead of writing '0' to the cache enable bit in the cache control register.

Note that after a processor (or any other AHB master) has initiated a flush the processor is not blocked by the flush unless it writes or requests data from the Level-2 cache. The cache blocks all accesses (responds with AMBA SPLIT or wait-states depending on cache configuration) until the flush is complete. AMBA SPLIT response is only implemented in version 3 of the core.

76.3.4 Disabling Cache

To be able to safely disable the cache when it is being accessed, the cache need to be disabled and flushed at the same time. This is accomplished by setting the cache disable bit when issue the flush command.

76.3.5 Diagnostic cache access

The diagnostic interface can be used for RAM block testing and direct access to the cache tag, cache data content and EDAC check bits. The read-check-bits field in the error control register selects if data content or the EDAC check bits should be read out. On writes, the EDAC check bits can be selected from the data-check-bit or tag-check-bit register. These register can also be XOR:ed with the correct check bits on a write. See the error control register for how this is done.

76.3.6 Error injection

Except using the diagnostic interface, the EDAC check bits can also be manipulated on a regular cache access. By setting the xor-check-bit field in the error control register the data EDAC check bits will be XOR:ed with the data-check-bit register on the next write or the tag EDAC check bits will be XOR:ed with the tag-check-bit register on the next tag replacement. The tag check bit manipulation is only done if the tag-check-bit register is not zero. The xor-check-bit is reset on the next tag replacement or data write. Error can also be injected by writing a address (or way, index, offset) together with the inject bit to the "Error injection" register. This will XOR the check-bits for the specified address (or cache-line) with the tag-/data-check-bit register depending on the Error injection configuration register. If the specified address in not cached, the cache content will be unchanged.

76.3.7 AHB slave interface

The slave interface is the core's connection to the CPU and the level 1 cache. The core can accept 8-bit(byte), 16-bit(half word), 32-bit(word), 64-bit, and 128-bit single accesses and also 32-bit, 64-bit, and 128-bit burst accesses. For an access during a flush operation, the core will respond with a AHB SPLIT response or with wait-states. For a uncorrectable error or a backend AHB error on a read access, the core will respond with a AMBA ERROR response. AMBA SPLIT response is only implemented in version 3 of the core.

76.3.8 AHB master interface

The master interface is the core's connection to the memory controller. During cache line fetch, the controller can issue either a 32-bit, 64-bit or 128-bit burst access. For a non cachable access and in write-through mode the core can also issue a 8-bit(byte), 16-bit(half word), 32-bit(word), 64-bit, or 128-bit single write access. The bbuswidth VHDL generic controls the maximum bus access size on the master interface in the "wide-bus" address range. If set to 128 (default), the largest access will be 128-bit. If set to 64, the largest access will be 64-bit. If set to 32, the largest access will be 32-bit. The

“wide-bus address range is defined by the wbmask VHDL generic. Each bit in this 16-bit value represents a 256 Mbyte address block on the AMBA AHB bus. The cache will only generate wide accesses (> 32-bit) to address ranges which wbmask bit is ‘1’. For address ranges which wbmask bit is ‘0’, wide accesses will be translated to 32-bit bursts.

The HBURST value during burst accesses will correspond to SINGLE, INCR, INCR4, INCR8 or INCR16, depending on burst type and AHB data bus width.

76.3.9 AXI master interface

AXI master interface supports data width of 32, 64, or 128-bit, configured with the GRLIB configuration option AXIDW. The interface supports both AXI3/AXI4 bus interfaces (no AXI4 specific operation is performed by the master interface). The value of the AXI AxCACHE can be configured via a configuration register (L2CACCC). When the cache need to fetch a cache line from memory and write a cache line to memory, both the read and write operation are started at the same time.

76.3.10 Cache status

The cache controller has a status register which provide information on the cache configuration (multi-way configuration and set size). The core also provides an access counter and a hit counter via AHB mapped registers. These register can be used to calculate hit rate. The counters increments for each data access to core (i.e. a burst access is only counted as one access). When writing 0 to the access counter, the internal access/hit counters is cleared and its value is loaded to the registers accessible via the AHB interface. In wrapping mode both counters will be cleared when the access counter is wrapping at 0xFFFFFFFF. In shifting mode both counters will be shifted down 16 bits when the access counter reach 0xFFFFFFFF. In this mode the accessible counter registers is updated automatically when the access counter’s 16 LSB reach the value of 0xFFFF.

The core can also implement a front-side bus usage counter. This counter records every clock cycle the bus is not in idle state. The registers accessible via the AHB interface is updated in the same way as for the hit counter registers. Writing 0 to the bus cycle counter register resets the bus usage counters. This counter also has a wrapping and shifting mode similar to the hit counter.

In addition to the counter registers, the core also provide output signals for: cache hit, cache miss, and cache access. These signals can be connected to external statistic counters.

76.3.11 Endianness

The core is designed for big-endian systems.

76.4 Registers

The core is configured via registers mapped into the AHB memory address space.

*Table 1371.*L2C: AHB registers

AHB address offset	Register
0x00	Control register
0x04	Status register
0x08	Flush (Memory address)
0x0C	Flush (set, index)
0x10	Access counter
0x14	Hit counter
0x18	Bus cycle counter
0x1C	Bus usage counter
0x20	Error status/control
0x24	Error address
0x28	TAG-check-bit
0x2C	Data-check-bit
0x30	Scrub Control/Status
0x34	Scrub Delay

*Table 1371.*L2C: AHB registers

AHB address offset	Register
0x38	Error injection
0x3C	Access control (Only available in version 3 of the core)
0x40	Priming start (first area)
0x44	Priming stop (first area)
0x48	Priming start (second area)
0x4C	Priming stop (second area)
0x50	Error handling / injection configuration
0x80 - 0xFC	MTRR registers
0x80000 - 0xFFFFC	Diagnostic interface (Tag) 0x80000: Tag 1, way-1 0x80004: Tag 1, way-2 0x80008: Tag 1, way-3 0x8000C: Tag 1, way-4 0x80010: Tag check-bits way-0,1,2,3 (Read only) bit[31] = RESERVED bit[30:24] = check-bits for way-1. bit[23] = RESERVED bit[22:16] = check-bits for way-2. bit[15] = RESERVED bit[14:8] = check-bits for way-3. bit[7] = RESERVED bit[6:0] = check-bits for way-4. 0x80020: Tag 2, way-1 0x80024: ...
0x200000 - 0x3FFFFC	Diagnostic interface (Data) 0x200000 - 0x27FFFC: Data or check-bits way-1 0x280000 - 0x2FFFFF: Data or check-bits way-2 0x300000 - 0x27FFFC: Data or check-bits way-3 0x380000 - 0x3FFFFF: Data or check-bits way-4 When check-bits are read out: Only 32-word at offset 0x0, 0x10, 0x20,... are valid check-bits. bit[31] = RESERVED bit[30:24] = check-bits for data word at offset 0x0. bit[23] = RESERVED bit[22:16] = check-bits for data word at offset 0x4. bit[15] = RESERVED bit[14:8] = check-bits for data word at offset 0x8. bit[7] = RESERVED bit[6:0] = check-bits for data word at offset 0xc.

76.4.1 Control Register

*Table 1372.*0x00 - L2CC - L2C Control register

31	30	29 28	27 19	18 16	15 12	11 8	7 6	5	4	3	2	1	0
EN	EDAC	REPL	RESERVED	BBS	INDEX-WAY	LOCK	RES	HPRHB	HPB	UC	HC	WP	HP
0	0	0	0	-	0	0	0	0	0	0	0	0	0
rw	rw	rw	r	rw	rw	rw	r	rw	rw	rw	rw	rw	rw

31 Cache enable (EN) - When set, the cache controller is enabled. When disabled, the cache is bypassed.

30 EDAC enable (EDAC)

29: 28 Replacement policy (REPL) -
00: LRU
01: (pseudo-) random
10: Master-index using index-replace field
11: Master-index using the modulus function

27: 19 RESERVED

18: 16 Backend bus size configuration (BBS) -
“100”: Configure backend bus size to 128-bit.
“011”: Configure backend bus size to 64-bit.
“010”: Configure backend bus size to 32-bit.
“000”: No configuration update is done.
Other values: not supported.

15: 12 Master-index replacement (INDEX-WAY) - Way to replace when Master-index replacement policy and master index is larger than number of ways in the cache.

11: 8 Locked ways (LOCK) - Number of locked ways.

7: 6 RESERVED

5 HPROT read hit bypass (HPRHB) - When set, a non-cacheable and non-bufferable read access will bypass the cache on a cache hit and return data from memory. Only used with HPROT support.

4 HPROT bufferable (HPB) - When HPROT is used to determine cachability and this bit is set, all accesses is marked bufferable.

3 Bus usage status mode (UC) - 0 = wrapping mode, 1 = shifting mode.

2 Hit rate status mode (HC) - 0 = wrapping mode, 1 = shifting mode.

1 Write policy (WP) - When set, the cache controller uses the write-through write policy. When not set, the write policy is copy-back.

0 HPROT enable (HP) - When set, use HPROT to determine cachability.

76.4.2 Status Register

*Table 1373.*0x04 - L2CS - L2C Status register

31 25	24	23	22	21 16	15 13	12 2	1 0
RESERVED	DP	LS	AT	MP	MTRR	BBUS-W	WAY-SIZE	WAY
0	*	*	*	*	*	1	*	*
r	r	r	r	r	r	r	r	r

31: 26 RESERVED

25 Data priming (DP) - 1 = supported.

24 Cache line size (LS) - 1 = 64 bytes, 0 = 32 bytes.

23 Access time (AT) - Access timing is simulated as if memory protection is implemented

22 Memory protection (MP) - implemented

21: 16 Memory Type Range Registers (MTRR) - Number of MTRR registers implemented

15: 13 Backend bus width (BBUS-W) 1 = 128-bit, 2 = 64-bit, 4 = 32-bit

*Table 1373.*0x04 - L2CS - L2C Status register

12: 2		Cache way size (WAY-SIZE) - Size in kBytes
1: 0		Multi-Way configuration (WAY) "00": Direct mapped "01": 2-way "10": 3-way "11": 4-way

76.4.3 Flush (Memory Address) Register

*Table 1374.*0x08 - L2CFMA - L2C Flush (Memory address) register

31 5	4	3	2 0
Memory Address (ADDR)	R	DI	FMODE
NR	0	0	0
rw	r	w	rw

31: 5 Memory Address (ADDR) - (For flush all cache lines, this field should be set to zero)

4 RESERVED

3 Cache disable (DI) - Setting this bit to '1' is equal to setting the Cache enable bit to '0' in the Cache Control register

2: 0 Flush mode (FMODE) -
"001": Invalidate one line, "010": Write-back one line, "011": Invalidate & Write-back one line.
"101": Invalidate all lines, "110": Write-back all lines, "111": Invalidate & Write-back all lines.
Only dirty cache lines are written back to memory.

76.4.4 Flush (Set, Index) Register

*Table 1375.*0x0C - L2CFSI - L2C Flush (Set, Index) register

31 16	10	9	8	7	6	5 4	3	2	1 0
INDEX / TAG		FL	VB	DB	R	WAY	DI	WF	FMODE
NR		0	0	0	0	0	0	0	0
rw		rw	rw	rw	r	rw	w	rw	rw

31: 16 Cache line index (INDEX) - used when a specific cache line is flushed

31: 10 (TAG) - used when "way flush" is issued. If a specific cache line is flushed, bit[15:10] should be set to zero. When a way flush is issued, this field will be used as the TAG for the selected cache way.

9 Fetch Line (FL) - If set to '1' data is fetched form memory when a "way flush" is issued. If a specific cache line is flushed, this bit should be set to zero

8 Valid bit (VB) - used when "way flush" is issued. If a specific cache line is flushed, this bit should be set to zero.

7 Dirty bit (DB) - used when "way flush" is issued. If a specific cache line is flushed, this bit should be set to zero

6 RESERVED

5: 4 Cache way (WAY) -

3 Cache disable (DI) - Setting this bit to '1' is equal to setting the Cache enable bit to '0' in the Cache Control register.

2 Way-flush (WF) - When set one way is flushed, If a specific cache line should be flushed, this bit should be set to zero

1: 0 Flush mode (FMODE) -

line flush:
"01": Invalidate one line
"10": Write-back one line (if line is dirty)
"11": Invalidate & Write-back one line (if line is dirty).

way flush:
"01": Update Valid/Dirty bits according to register bit[8:7] and TAG according to register bits[31:10]
"10": Write-back dirty lines to memory
"11": Update Valid/Dirty bits according to register bits [8:7] and TAG according to register bits[31:10], and Write-back dirty lines to memory.

76.4.5 Access Counter Register

*Table 1376.*0x10 - L2CACC - Access counter register

31	0
Access counter	
0	
wc	

31 : 0 Access counter. Write 0 to clear internal access/hit counter and update access/hit counter register.

76.4.6 Hit Counter Register

*Table 1377.*0x14 - L2CHIT - Hit counter register

31	0
Hit counter	
0	
wc	

31 : 0 Hit counter.

76.4.7 Front-side Bus Cycle Counter Register

*Table 1378.*0x18 - L2CFSCCNT - Front-side bus cycle counter register

31	0
Bus cycle counter	
0	
wc	

31 : 0 Bus cycle counter. Write 0 to clear internal bus cycle/usage counter and update bus cycle/usage counter register.

76.4.8 Front-side Bus Usage Counter Register

*Table 1379.*0x1C - L2CFSUCNT - Front-side bus usage counter register (address offset 0x1C)

31	0
Bus usage counter	
0	
wc	

31 : 0 Bus usage counter.

76.4.9 Error Status/Control

*Table 1380.*0x20 - L2CERR - L2CError status/control register

31 28	27	26 24	23	22	21	20	19	18 16	15 12	11 8	7 6	5 4	3	2	1	0
AHB master index	SCRUB	TYPE	TAG/DATA	COR/UCOR	MULTI	VALID	DISERESP	Correctable error counter	IRQ pending	IRQ mask	Select CB	Select TCB	XCB	RCB	COMP	RST
NR	NR	NR	NR	NR	NR	NR	0	NR	NR	0	0	0	0	0	0	0
r	r	r	r	r	r	r	rw	r	r	rw	rw	rw	rw	rw	rw	w

31: 28 AHB master that generated the access

27 Scrub error (SCRUB) - Indicates that the error was trigged by the scrubber.

*Table 1380.*0x20 - L2CERR - L2CError status/control register

26: 24	Access/Error Type: (TYPE) - 000: cache read, 001: cache write, 010: memory fetch, 011: memory write, 100: Write-protection hit, 101: backend read AHB error, 110: backend write AHB error
23	Tag or data Error - 0 tag error, 1: data error
22	Correctable or uncorrectable error - 0: correctable error, 1: uncorrectable error
21	Multiple error (MULTI) - set when multiple errors has been detected.
20	Error status valid (VALID) - register contains valid error status.
19	Disable error responses for uncorrectable EDAC error (DISERESP).
18: 16	Correctable error counter
15: 12	Interrupt pending bit3: Backend AHB error bit2: Write-protection hit bit1: Uncorrectable EDAC error bit0: Correctable EDAC error
11: 8	Interrupt mask (if set this interrupt is unmasked) bit3: Backend AHB error bit2: Write-protection hit bit1: Uncorrectable EDAC error bit0: Correctable EDAC error
7: 6	Selects (CB) - data-check-bits for diagnostic data write: 00: use generated check-bits 01: use check-bits in the data-check-bit register 10: XOR check-bits with the data-check-bit register 11: use generated check-bits
5: 4	Selects (TCB) - tag-check-bits for diagnostic tag write: 00: use generated check-bits 01: use check-bits in the tag-check-bit register 10: XOR check-bits with the tag-check-bit register 11: use generated check-bits
3	Xor check-bits (XOR) - If set, the check-bits for the next data write or tag replace will be XOR:ed withe the check-bit register. Default value is 0.
2	Read check-bits (RCB) - If set, a diagnostic read to the cache data area will return the check-bits related to that data.When this bit is set, check bits for the data at offset 0x0 - 0xc can be read at offset 0x0, the check bits for data at offset 0x10 - 0x1c can be read at offset 0x10, ...
1	Compare error status (COMP) - If set, a read access matching a uncorrectable error stored in the error status register will generate a AHB error response. Default value is 0.
0	Resets (RST) - clear the status register to be able to store a new error. After power up the status register needs to be cleared before any valid data can be read out.

76.4.10 Error Address Register

*Table 1381.*0x24 - L2CERRA - L2C Error address register

31	0
Error address (EADDR)	
NR	
r	

31 : 0 Error address (EADDR)

76.4.11 Tag-check-bit Register

*Table 1382.*0x28 - L2CTCB - L2C TAG-Check-Bits register

31	7	6	0
RESERVED		TCB	
0		0	
r		rw	

31 : 7 RESERVED

6 : 0 TAG Check-bits (TCB) - Check-bits which can be selected by the “Select check-bit“ field in the error status/control register for TAG updates

76.4.12 Data-check-bit Register

*Table 1383.*0x2C - L2CCB - L2C Data-Check-Bits register

31	28	27	0
RESERVED		DCB	
0		0	
r		rw	

31 : 28 RESERVED

27 : 0 Data Check-bits (DCB) - Check-bits which can be selected by the “Select check-bit“ field in the error status/control register for TAG updates

76.4.13 Scrub Control/Status Register

*Table 1384.*0x30 - L2CSCRUB - L2C Scrub control/status register

31	16	15	6	5	4	3	2	1	0
INDEX		RESERVED		WAY		RES		PEN	EN
0		0		0		0		0	0
rw		r		rw		r		rw	rw

31: 16 Scrub Index (INDEX) - Index for the next line scrub operation

15: 6 RESERVED

5: 4 Scrub Way (WAY) - Way for the next line scrub operation

3: 2 RESERVED

1 Scrub Pending (PEN) - Indicates when a line scrub operation is pending. When the scrubber is disabled, writing ‘1’ to this bit scrubs one line.

0 Scrub Enable (EN) - Enables / disables the automatic scrub functionality.

76.4.14 Scrub Delay Register

*Table 1385.*0x34 - L2CSDEL - L2C Scrub delay register

31 16	15 0
RESERVED	DEL
0	0
r	rw

31: 16 RESERVED

15: 0 Scrub Delay (DEL) - Delay the scrubber waits before issue the next line scrub operation

76.4.15 Error Injection Register

*Table 1386.*0x38 - L2CEINJ0 - L2C Error injection register (Mode 0)

31 2	1	0
ADDR	R	INJ
0	0	0
rw	r	rw

31: 2 Error Inject address (ADDR)

1: RESERVED

0 Inject error (INJ) - Set to ‘1’ to inject a error at “address”.

*Table 1387.*0x38 - L2CEINJ1 - L2C Error injection register (Mode 1)

31 28	27 5	4 2	1	0
WAY	INDEX	OFFSET	R	INJ
0	0	0	0	0
rw	rw	rw	r	rw

31: 28 Error Inject cache-line way (WAY)

27: 5 Error Injection cache-line Index (INDEX)

4: 2 Error Injection cache-line offset (OFFSET)

1: RESERVED

0 Inject error (INJ) - Set to ‘1’ to inject a error at “address”.

76.4.16 Access control register

*Table 1388.*0x3C - L2CACCC - L2C Access control register

31 16	15			12	11	10	9	8	7	6	5	4	3	2	1	0
AxCACHE	RES	DSC	SH	RES	PS	SPLITQ	NHM	BERR	OAPM	FLINE	DBPF	128WF	R	DBPWS	SPLIT	R
0xFFEE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
rw	r	rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw	r	rw	rw	r

31: 16 AXI CACHE configuration (AxCACHE) - (only available when AXI backend bus is implemented)
Bit[31:28]: ARCACHE (used when the cache fetches a cache line from memory)
Bit[27:24]: AWCACHE (used when the cache writes back a cache line to memory)
Bit[23:20]: ARCACHE (used for accesses that bypass the cache and reads from memory)
Bit[19:16]: AWCACHE (used for accesses that bypass the cache and writes to memory)

15 RESERVED

14 Disable cancellation and reissue of scrubber operation (DSC) - When set to ’0’, a write access to the same index as an ongoing scrubber operation will cancel and reissue the scrubber operation. When set to ’1’ the scubber operation will complete without detection of the write access. This field is only available in silicon revision 1.

13 Scrubber hold (SH) - When set to ’1’ the cache will delay any new access until the current scrubber operation is complete. This field is only available in silicon revision 1.

12 RESERVED

11 Priming statistic (PS) - When set, priming operation is included in the access/hit/miss statistics.

10 SPLIT queue write order (SPLITQ) When set, all write accesses (except locked) will be placed in the split queue when the split queue is not empty

9 No hit for cache misses (NHM) - When set, the unsplited read access for a read miss will not trig the access/hit counters.

8 Bit error status (BERR) - When set, the error status signals will represent the actual error detected rather then if the error could be corrected by refetching data from memory.

7 One access/master (OAPM) - When set, only one ongoing access per master is allowed to enter the cache. A second access would receive a SPLIT response

6 (FLINE) - When set, a cache line fetched from memory can be replaced before it has been read out by the requesting master.

5 Disable bypass prefetching (DBPF) - When set, bypass accesses will be performed as single accesses towards memory.

4 128-bit write line fetch (128WF) - When set, a 128-bit write miss will fetch the rest of the cache from memory.

3 RESERVED

2 Disable wait-states for discarded bypass data (DBPWS) - When set, split response is given to a bypass read access which data has been discarded and needs to refetch data from memory.

1 Enabled SPLIT response (SPLIT) - When set the cache will issue a AMBA SPLIT response on cache miss

0 RESERVED

76.4.17 Priming start register 0

*Table 1389.*0x40 - PSTART0 - L2C priming start register

31 5	4 1	0
ADDR	RES	P	EN
0	0	0	0
rw	r	rw	rw

31: 2 Priming start address (ADDR)

4: 2 RESERVED

*Table 1389.*0x40 - PSTART0 - L2C priming start register

1	Priming access pending (P) - To start the priming operation this bit and the priming enable bit need to be set to '1'.
0	Priming enable (EN) - This indicates that the first area (defined by PSTART0.ADDR to PSTOP0.ADDR) should be primed.

76.4.18 Priming stop register 0

*Table 1390.*0x40 - PSTOP0 - L2C priming stop register

31 5	4 0
ADDR	RES
0	0
rw	r

31: 5 Priming stop address (ADDR)

4: 0 RESERVED

76.4.19 Priming start register 1

*Table 1391.*0x48 - PSTART1 - L2C priming start (second area) register

31 5	4 1	0
ADDR	RES	P	EN
0	0	0	0
rw	r	r	rw

31: 2 Priming start address (ADDR)

4: 2 RESERVED

1 Priming access pending (P) - This bit is read only and indicates that a priming operation on the second priming area is executing.

0 Priming enable (EN) - This indicates that the first area (defined by PSTART1.ADDR to PSTOP1.ADDR) should be primed.

76.4.20 Priming stop register 1

*Table 1392.*0x4C - PSTOP1 - L2C priming stop (second area) register

31 5	4 0
ADDR	RES
0	0
rw	r

31: 5 Priming stop address (ADDR)

4: 0 RESERVED

76.4.21 Error Handling / Injection configuration

*Table 1393.*0x4C - L2CEINJCFG - L2C injection configuration register

31 11	10	9	8	7 4	3			0
RESERVED	EDI	TER	IMD	RES	M	PI	DT	CB
0	0	0	0	0	0	0	0	0
r	rw	rw	rw	r	rw	rw	rw	rw

31: 11 RESERVED

10 (EDI) - Enable invalidation off cache line with un-correctable data error.
When set to 1 and a un-correctable data error is detected, the cache line will be invalidated (removing the error form the cache).

9 (TER) - Disable error response on un-correctable TAG error detection.
When set to 0 the access detecting a un-correctable TAG error would generate a AMBA error response. When set to 1 this access would not generate an error response.

*Table 1393.*0x4C - L2CEINJCFG - L2C injection configuration register

8	(IMD) - Disable index match only after un-correctable TAG error. When set to 1 the TAG and INDEX are matched against the error address register after a detected un-correctable TAG error. When set to 0 only the INDEX are matched against the error address register.
7: 4	RESERVED
3	Error Injection Mode (M) 0: (Mode0) Error injection register layout is defined as a address. 1: (Mode1) Error injection register layout is defined as way, index, offset.
2	Prevent Error Injection on error (PI) 0: Ignore already existing error in cache-line 1: Prevent error injection when error exists in cache-line
1	Data/TAG Error injection (DT) 0: Inject error in data 1: Inject error in TAG
0	Check-Bit Error Injection (CB) 0: Inject error in check-bits 1: Inject error in data or TAG

76.4.22 Memory Type Range Register

*Table 1394.*0x80-FC - L2CMTRR - L2C Memory type range register

31 18	17 16	15 2	1	0
ADDR	ACC	MASK	WP	AC
0	0	0	0	0
rw	rw	rw	rw	rw

31: 18	Address field (ADDR) - to be compared to the cache address [31:18]
17: 16	Access field (ACC) - 00: uncached, 01: write-through
15: 2	Address mask (MASK) - Only bits set to 1 will be used during address comparison
1	Write-protection (WP) - 0: disabled, 1: enabled
0	Access control field (AC) -. 0: disabled, 1: enabled

76.5 Core versions

The L2 cache controller exists in several different versions. The latest version is v3 and this is the default version used in GRLIB. For existing users of version 2 that want to continue with this version, the GRLIB design Makefile can be modified to add:

```
DIRSKIP=l2cache/v3
DIRADD=l2cache/v2
```

Performing the modification above will mean that the scripts will be generated to use version 2 of the Level-2 cache.

76.6 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x04B. For description of vendor and device identifier see GRLIB IP Library User's Manual

76.7 Implementation

76.7.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core will use asynchronous reset for all registers if the GRLIB config package setting *grlib_async_reset_enable* is set.

76.7.2 RAM usage

The L2C uses single-port RAM to implement both cache tags and data memory. The tags are implemented using the SYNCRAM core, with the width and depth depending on the cache size configuration. The data memory is implemented using the SYNCRAM_128BW or SYNCRAM_156BW core, which is a 128-bit or 156-bit wide RAM wrapper with byte enables. The SYNCRAM_156BW is used when memory protection (EDAC) is implemented. For multi-way caches, each way's tag is implemented with a separate SYNCRAM block. The data memory can be implemented with separate SYNCRAM_128BW/156BW cores, or merged into the same SYNCRAM_128BW/156BW if the ARCH generic is set to 1. This will reduce the number of SYNCRAM_128BW/156BW core in multi-ways cache to one. The valid/dirty bits are stored in a SYNCRAM_2PFT core.

76.8 Configuration options

Table 1395 shows the configuration options of the core (VHDL generics).

*Table 1395.*Configuration options

Generic name	Function	Allowed range	Default
AHB slave interface			
hmstndx	AHB master index.	0 - NAHBMST-1	0
hslvndx	AHB slave index.	0 - NAHBSLV-1	0
haddr	ADDR field of the AHB BAR (for data access).	0 - 16#FFF#	16#F00#
hmask	MASK field of the AHB BAR.	0 - 16#FFF#	16#F00#
ioaddr	ADDR field of the AHB BAR (for register and diagnostic access).	0 - 16#FFF#	16#F00#
AHB master interface			
hmstndx	AHB master index.	0 - NAHBMST-1	0
bbuswidth	Maximum bus width on master AHB interface	32, 64, 128	128
bioaddr	ADDR field of the AHB BAR (for backend ioarea). Appears in the bridge's slave interface user-defined register 1.	0 - 16#FFF#	0
biomask	MASK field of the AHB BAR.	0 - 16#FFF#	0
wbmask	Wide-bus mask. Each bit in this value represent a 256Mbyte address range. To enabled wide accesses (>32-bit) to an address range, set the corresponding bit to '1'.	0 - 16#FFFF#	16#FFFF#
AXI master interface			
axiid	AXI ID	0 - 15	0
Cache configuration			
memtech	The memory technology used for the internal FIFOs.	0 - NTECH	0
cached	Fixed cachability mask.	0 - 16#FFFF#	16#0000#
hirq	Interrupt line used by the core.	0 - NAHBIRQ-1	0
cen	Reset value for cache enable. 1 = cache enabled.	0 - 1	0
hproten	Reset value for enabling hprot functionality (Only available in version 2 of the core)	0 - 1	0
wp	Reset value for write-policy: 0 = copy-back, 1 = write-through (Only available in version 2 of the core)	0 - 1	0
repl	Reset value for replacement policy: 0 = LRU, 1 = pseudo-random (Only available in version 2 of the core)	0 - 1	0

*Table 1395.*Configuration options

Generic name	Function	Allowed range	Default
ways	Number of cache ways	1 - 4	1
waysize	Size of each cache way in kBytes	1 - 512	1
linesize	Cache line size in bytes	32, 64	32
sbus	The number of the AHB bus to which the slave interface is connected. The value appears in bits [1:0] of the user-defined register 0 in the slave interface configuration record and master configuration record.	0-3	0
mbus	The number of the AHB bus to which the master interface is connected. The value appears in bits [3:2] of the user-defined register 0 in the slave interface configuration record and master configuration record.	0-3	1
stat	Enables the statistics counters. 0 all counters is disabled. 1 enables the access/hit counter. 2 enables the bus usage counter in addition to the access/hit counter.	0-2	0
arch	Selects between separate (0) or shared (1) RAM in multi-way configurations (see text below)	0 - 1	0
mtrr	Number of MTRR registers	0 - 32	0
edacen	Default value for the EDACEN field in the cache control register	0 - 1	0
rmw	Enables Read-Modify-Write for sub-word writes.	0 - 1	0
ft	Enables the memory protection (EDAC) implementation	0 - 1	0
fttiming	Simulate access timing as if memory protection was enabled. (Only for prototype testing)	0 - 1	0

76.9 Signal descriptions

Table 1396 shows the interface signals of the core (VHDL ports).

*Table 1396.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
AHBSI	*	Input	AHB slave input signals	-
AHBSO	*	Output	AHB slave output signals	-
AHBMI	*	Input	AHB master input signals	-
AHBMO	*	Output	AHB master output signals	-
AXIMI	*	Input	AXI master input signals	-
AXIMO	*	Output	AXI master output signals	-
AHBSOV	*	Input	Vector of all AHB slave outputs on the backend AHB bus.	
STO	bit[2]: Access bit[1]: Miss bit[0]: Hit	Output	Statistic output.	

*) see GRLIB IP Library User's Manual.

76.10 Library dependencies

Table 1397 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1397.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	L2CACHE	Component	Component declaration

76.11 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;
library grlib;
use grlib.amba.all;
use grlib.stdlib.all;
use grlib.tech.all;
library gaisler;
use gaisler.l2cache.all;

entity l2c_ex is
  port (
    clk : in std_ulogic;
    rst : in std_ulogic
  );
end;
.
.
signal ahbsi  : ahb_slv_in_type;
signal ahbso  : ahb_slv_out_vector := (others => ahbs_none);
signal ahbmi  : ahb_mst_in_type;
signal ahbmo  : ahb_mst_out_vector := (others => ahbm_none);
signal ahbsi2 : ahb_slv_in_type;
signal ahbso2 : ahb_slv_out_vector := (others => ahbs_none);
signal ahbmi2 : ahb_mst_in_type;
signal ahbmo2 : ahb_mst_out_vector := (others => ahbm_none);
signal aximi : ahb_somi_type;
signal aximo : ahb_mosi_type;


architecture rtl of l2c_ex is

begin

(AHB backend instantiation)
...

  l2c0 : l2c
  generic map(hslvidx => 5, hmstidx => 1, cen => 0, haddr => 16#400#, hmask => 16#C00#,
              ioaddr => 16#FF4#, cached => 16#00F3#, repl => 0, ways => 1,
              linesize => 32, waysize => 512, memtech => 0, bbuswidth => 64)
  port map(rst => rst, clk => clk, ahbsi => ahbsi, ahbso => ahbso(5),
           ahbmi => ahbmi2, ahbmo => ahbmo2(1), ahbsov => ahbso2);

...

(AXI backend instantiation)
...

  l2c0 : l2c_axi_be
  generic map(hslvidx => 5, axiid=> 0, cen => 0, haddr => 16#400#, hmask => 16#C00#,
              ioaddr => 16#FF4#, cached => 16#00F3#, repl => 0, ways => 1,
              linesize => 32, waysize => 512, memtech => 0)
```

```
  port map(rst => rst, clk => clk, ahbsi => ahbsi, ahbso => ahbso(5),
           aximi => aximi, aximo => aximo);

...

end;
```

77 L3STAT - LEON3 Statistics Unit

77.1 Overview

The LEON3 Statistics Unit (L3STAT) is used to count events in the LEON3 processor and on the AHB bus, in order to create performance statistics for various software applications.

L3STAT consists of a configurable number of 32-bit counters, which increment on a certain event. The counters roll over to zero when reaching their maximum value, but can also be automatically cleared on reading to facilitate statistics building over longer periods. Each counter has a control register where the event type is selected. In multi-processor systems, the control registers also indicates which particular processor core is monitored. The table 1398 below shows the event types that can be monitored.

NOTE: L3STAT does currently not support double-clocked processor configurations. The processors and statistics unit must be run on the same frequency as the AMBA buses for L3STAT to function correctly.

*Table 1398.*Event types and IDs

ID	Event description
Processor events:	
0x00	Instruction cache miss
0x01	Instruction MMU TLB miss
0x02	Instruction cache hold
0x03	Instruction MMU hold
0x08	Data cache (read) miss
0x09	Data MMU TLB miss
0x0A	Data cache hold
0x0B	Data MMU hold
0x10	Data write buffer hold
0x11	Total instruction count
0x12	Integer instructions
0x13	Floating-point unit instruction count
0x14	Branch prediction miss
0x15	Execution time, excluding debug mode
0x17	AHB utilization (per AHB master) (implementation depedent)
0x18	AHB utilization (total, master/CPU selection is ignored) (implementation dependent)
0x22	Integer branches
0x28	CALL instructions
0x30	Regular type 2 instructions
0x38	LOAD and STORE instructions
0x39	LOAD instructions
0x3A	STORE instructions
AHB events (only available if core is connected to a LEON3 Debug Support Unit):	
0x40	AHB IDLE cycles.
0x41	AHB BUSY cycles.
0x42	AHB NON-SEQUENTIAL transfers. Filtered on CPU/AHBM if SU(1) = ‘1’
0x43	AHB SEQUENTIAL transfers. Filtered on CPU/AHBM if SU(1) = ‘1’
0x44	AHB read accesses. Filtered on CPU/AHBM if SU(1) = ‘1’
0x45	AHB write accesses. Filtered on CPU/AHBM if SU(1) = ‘1’

*Table 1398.*Event types and IDs

ID	Event description
0x46	AHB byte accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x47	AHB half-word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x48	AHB word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x49	AHB double word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x4A	AHB quad word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x4B	AHB eight word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x4C	AHB waitstates. Filtered on CPU/AHBM if SU(1) = '1'
0x4D	AHB RETRY responses. Filtered on CPU/AHBM if SU(1) = '1'
0x4E	AHB SPLIT responses. Filtered on CPU/AHBM if SU(1) = '1'
0x4F	AHB SPLIT delay. Filtered on CPU/AHBM if SU(1) = '1'
0x50	AHB bus locked. Filtered on CPU/AHBM if SU(1) = '1'
0x51-0x5F	Reserved
Implementation specific events:	
0x60 - 0x6F	External event 0 - 15. Filtered on CPU/AHBM if SU(1) = '1'.
AHB events (only available if core is connected to a standalone AHB trace buffer):	
0x70	AHB IDLE cycles.
0x71	AHB BUSY cycles. Filtered on CPU/AHBM if SU(1) = '1'
0x72	AHB NON-SEQUENTIAL transfers. Filtered on CPU/AHBM if SU(1) = '1'
0x73	AHB SEQUENTIAL transfers. Filtered on CPU/AHBM if SU(1) = '1'
0x74	AHB read accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x75	AHB write accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x76	AHB byte accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x77	AHB half-word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x78	AHB word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x79	AHB double word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x7A	AHB quad word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x7B	AHB eight word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x7C	AHB waitstates. Filtered on CPU/AHBM if SU(1) = '1'
0x7D	AHB RETRY responses. Filtered on CPU/AHBM if SU(1) = '1'
0x7E	AHB SPLIT responses. Filtered on CPU/AHBM if SU(1) = '1'
0x7F	AHB SPLIT delay. Filtered on CPU/AHBM if SU(1) = '1'
Events generated from REQ/GNT signals (only available if core has been implemented with VHDL generic reqsel /=0)	
0x80 - 0x8F	Active when master selected by CPU/AHBM field has request asserted while grant is asserted for the master correspoding to the least significant nibble of the event ID. 0x80 is master 0 grant, 0x81 is master 1 grant, .., and so on.
0x90 - 0x9F	Active when master selected by CPU/AHBM field has request asserted while grant is deasserted for the master correspoding to the least significant nibble of the event ID. 0x90 is master 0 grant, 0x91 is master 1 grant, .., and so on.

Note that IDs 0x39 (LOAD instructions) and 0x3A (STORE instructions) will both count all LDST and SWAP instructions. The sum of events counted for 0x39 and 0x3A may therefore be larger than the number of events counted with ID 0x38 (LOAD and STORE instructions).

Event 0x00 - 0x3A can be counted of the core has been connected to one or several LEON3 processor cores. Counting of events 0x40 - 0x5F requires that the core is connected to a LEON3 Debug Support Unit (DSU). The core's Counter control registers have a field that shows if the core has been imple-

mented with this connection. The documentation for the Debug Support Unit contains more information on events 0x40 - 0x5F. Please note that the statistical outputs from the DSU may be subject to AHB trace buffer filters. The same applies to events 0x70 - 0x7F that can come from an AHBTRACE core.

The core can also be implemented with support for counting up to 15 external events. These events can come from any source, but should be clocked by a clock which is synchronous with the AMBA clock used for the L3STAT core.

77.2 Multiple APB interfaces

The core can be implemented with two AMBA APB interfaces. The first APB interface always has precedence when both interfaces handle write operations to the same address.

77.3 Registers

The L3STAT core is programmed through registers mapped into APB address space.

Table 1399. L3STAT counter control register

APB address offset	Register
0x00	Counter 0 value register
0x04	Counter 1 value register
4 * *n*	Counter *n* value register
0x100	Counter 0 control register
0x104	Counter 1 control register
0x100 + (4 * *n*)	Counter *n* control register
0x200	Counter 0 max/latch register
0x204	Counter 1 max/latch register
0x200 + (4 * *n*)	Counter *n* max/latch register
0x300	Timestamp register

Note: Revision 0 of this IP core had control registers starting at 0x80, max/latch registers starting at 0x100 and the timestamp register at 0x180. This IP core documentation is valid for revision 1 of the IP core.

77.3.1 Counter Value Register

*Table 1400.*0x000+n.4 - CVALn - Counter value register

31	0
CVAL	
NR	
rw	

31: 0 Counter value (CVAL) - This register holds the current value of the counter. If the core has been implemented with support for keeping the maximum count (MC field of Counter control register is ‘1’) and the Counter control register field CD is ‘1’, then the value displayed by this register will be the maximum counter value reached with the settings in the counter’s control register. Writing to this register will write both to the counter and, if implemented, the hold register for the maximum counter value.

77.3.2 Counter Control Register

*Table 1401.*0x100+n.4 - CCTRLn - Counter control register

31 23	22	21	20	19	18	17	16	15 14	13	12	11 4	3 0
NCNT	MC	IA	DS	EE	AE	EL	CD	SU	CL	EN	EVENT ID	CPU/AHBM
*	*	*	*	*	*	NR	NR	NR	NR	0	NR	NR
r	r	r	r	r	r	rw	rw	rw	rw	rw	rw	rw

31: 23 Number of counters (NCNT) - Number of implemented counters - 1

Note revision 0 of this core used bits 31:28 to indicate the number of CPUs. This manual applies to revision 1 of the core.

22 Maximum count (MC) - If this field is ‘1’ then this counter has support for keeping the maximum count value

21 Internal AHB count (IA) - If this field is ‘1’ the core supports events 0x17 and 0x18

20 DSU support (DS) - If this field is ‘1’ the core supports events 0x40-0x5F

19 External events (EE) - If this field is ‘1’ the core supports external events (events 0x60 - 0x6F)

18 AHBTRACE Events (AE) - If this field is ‘1’ the core supports events 0x70 - 0x7F.

17 Event Level (EL) - The value of this field determines the level where the counter keeps running when the CD field below has been set to ‘1’. If this field is ‘0’ the counter will count the time between event assertions. If this field is ‘1’ the counter will count the cycles where the event is asserted. This field can only be set if the MC field of this register is ‘1’.

16 Count maximum duration (CD) - If this bit is set to ‘1’ the core will save the maximum time the selected event has been at the level specified by the EL field. This also means that the counter will be reset when the event is activated or deactivated depending on the value of the EL field.

When this bit is set to ‘1’, the value shown in the counter value register will be the maximum current value which may be different from the current value of the counter.

This field can only be set if the MC field of this register is ‘1’.

15: 14 Supervisor/User mode filter (SU) - “01” - Only count supervisor mode events, “10” - Only count user mode events, others values - Count events regardless of user or supervisor mode. This setting only applies to events 0x0 - 0x3A.

When SU = “1x” only events generated by the CPU/AHB master specified in the CPU/AHBM field will be counted. This applies to events 0x40 - 0x7F.

: 13 Clear counter on read (CL) - If this bit is set the counter will be cleared when the counter’s value is read. The register holding the maximum value will also be cleared, if implemented.

If an event occurs in the same cycle as the counter is cleared by a read then the event will not be counted. The counter latch register can be used to guarantee that no events are lost

12 Enable counter (EN) - Enable counter

11: 4 Event ID to be counted

3: 0 CPU or AHB master to monitor.(CPU/AHBM) - The value of this field does not matter when selecting one of the events coming from the Debug Support Unit or one of the external events.

77.3.3 Counter max/latch Register

*Table 1402.*0x200+4n - CSVALn - Counter max/latch register

31	0
CSVAL	
NR	
rw*	

31: 0 Counter max/latch value (CSVAL) - This register holds the current value of the counter max/latch register. It is only available for a specific counter If the core has been implemented with support for keeping the maximum count (MC field of Counter control register is ‘1’).

If the counter control register field CD is ‘1’, then the value displayed by this register will be the maximum counter value reached with the settings in the counter’s control register.

If the counter control register field CDis ‘0’, then the value displayed by this register is the latched (saved) counter value. The counter value is saved whenever a write access is made to the core in address range 0x100 - 0x1FC (all counters are saved simultaneously). If the counter control register CL field is set, then the current counter value will be cleared when the counter value is saved into this register.

77.3.4 Timestamp Register

*Table 1403.*0x300 - TSTAMP - Timestamp register

31	0
TSTAMP	
NR	
rw*	

31: 0 Timestamp (TSTAMP) - Timestamp taken at latch of counters

77.4 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x098. For description of vendor and device identifiers see GRLIB IP Library User’s Manual.

77.5 Implementation

77.5.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User’s Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

77.6 Configuration options

Table 1404 shows the configuration options of the core (VHDL generics).

*Table 1404.*Configuration options

Generic	Function	Allowed range	Default
pindex	Selects which APB select signal (PSEL) will be used to access the statistical unit	0 to NAPBMAX-1	0
paddr	The 12-bit MSB APB address	0 to 16#FFF#	0
pmask	The APB address mask. Needs to be set to 16#FFE# if max/latch registers are enabled (VHDL generic clatch).	0 to 16#FFF#	16#FFF#
ncnt	Defines the number of counters	1 to 32	4
ncpu	Defines the number of CPUs monitored	1 - 16	1
nmax	If this generic is > 0, the core will include functionality for tracking the longest consecutive time that an event is active or inactive. The functionality will be available for the *nmax* first counters.	0 - 32	0
lahben	If this generic is 1, the core makes use of the AHBSI input for events 0x17 and 0x18, otherwise the AHBSI input is unused and events 0x17 and 0x18 will never increment a counter.	0 - 1	0
dsuen	If this generic is 1, the core makes use of the DSUO input for events 0x40 - 0x5F, otherwise the DSUO input is unused and events 0x40 - 0x5F will never increment a counter.	0 - 1	0
nextev	Defines the number of external events monitored	0 - 16	0
apb2en	Enables the second APB port on the core.	0 - 1	0
pindex2	Selects which APB select signal (PSEL) will be used to access the second interface of the statistical unit	0 to NAPBMAX-1	0
paddr2	The 12-bit MSB APB address for second interface	0 to 16#FFF#	0
pmask2	The APB address mask for second interface	0 to 16#FFF#	16#FFF#
astaten	If this generic is 1, the core makes use of the ASTAT input for events 0x70 - 0x7F, otherwise the ASTAT input is unused and events 0x70 - 0x7F will never increment a counter.	0 - 1	0
selreq	Support STATI.REQ/SEL events. If selreq is nonzero then the value+1 defines the number of monitored sel/req signals.	0 - 15	0
clatch	Include support for counter max/latch registers and time-stamp.	0 - 1	0
forcer0	For core to revision 0. If this generic is set to 1 then the maximum number of supported counters is 32 and the register address offsets and layout of the control register changes to comply to revision 0 of the IP core.	0 - 1	0

77.7 Signal descriptions

Table 1405 shows the interface signals of the core (VHDL ports).

*Table 1405.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
AHBSI	*	Input	AHB slave input signals	-
DBGO		Input	LEON3 debug output signals	-
DSUO	ASTAT	Input	DSU3 output signals	-
STATI	EVENT[15:0]	Input	Input for 16 user defined events	High
	ESOURCE [15:0][3:0]	Input	CPU/AHBM for each EVENT	-
	REQ[15:0]	Input	Input for 16 user defined request signals	High
	SEL[15:0]	Input	Input for 16 user defined select/grant signals	-
	TIMER[31:0]	Input	Time stamp value used when VHDL generic clatch /= 0	-
APB2I	*	Input	Secondary APB slave input signals	-
APB2O	*	Output	Secondary APB slave output signals	-
ASTAT	*	Input	AHBTRACE output signals	-

* see GRLIB IP Library User's Manual

77.8 Library dependencies

Table 1406 shows libraries used when instantiating the core (VHDL libraries).

*Table 1406.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	LEON3	Signals, component	Signal definitions and component declaration

77.9 Component declaration

The core has the following component declaration.

```
library gaisler;
use gaisler.leon3.all;

entity l3stat is
  generic (
    pindex      : integer := 0;
    paddr       : integer := 0;
    pmask       : integer := 16#fff#;
    ncnt        : integer := 4;
    ncpu        : integer := 1
    );
  port (
    rstn   : in std_ulogic;
    clk    : in std_ulogic;
    apbi   : in apb_slv_in_type;
```

```
    apbo   : out apb_slv_out_type;
    ahbsi  : in  ahb_slv_in_type;
    dbgo   : in l3_debug_out_vector(0 to NCPU-1));
end;
```

This example shows how the core can be instantiated.

```
library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.leon3.all;

begin

l3sgen : if CFG_L3S_ENABLE = 1 generate
    l3stat0 : l3stat
      generic map (pindex => 11, paddr => 11, ncnt => CFG_L3S_CNT, ncpu => CFG_NCPU)
      port map (rstn, clkm, apbi, apbo(11), ahbsi, dbgo);
end generate;
```

78 L4STAT - LEON4 Statistics Unit

78.1 Overview

The LEON4 Statistics Unit (L4STAT) is used count events in the LEON4 processor and on the AHB bus, in order to create performance statistics for various software applications.

L4STAT consists of a configurable number of 32-bit counters, which increment on a certain event. The counters roll over to zero when reaching their maximum value, but can also be automatically cleared on reading to facilitate statistics building over longer periods. Each counter has a control register where the event type is selected. In multi-processor systems, the control registers also indicates which particular processor core is monitored. The table 1407 below shows the event types that can be monitored.

NOTE: L4STAT does currently not support double-clocked processor configurations. The processors and statistics unit must be run on the same frequency as the AMBA buses for L4STAT to function correctly.

*Table 1407.*Event types and IDs

ID	Event description
Processor events:	
0x00	Instruction cache miss
0x01	Instruction MMU TLB miss
0x02	Instruction cache hold
0x03	Instruction MMU hold
0x08	Data cache (read) miss
0x09	Data MMU TLB miss
0x0A	Data cache hold
0x0B	Data MMU hold
0x10	Data write buffer hold
0x11	Total instruction count
0x12	Integer instructions
0x13	Floating-point unit instruction count
0x14	Branch prediction miss
0x15	Execution time, excluding debug mode
0x17	AHB utilization (per AHB master) (implementation depedent)
0x18	AHB utilization (total, master/CPU selection is ignored) (implementation dependent)
0x22	Integer branches
0x28	CALL instructions
0x30	Regular type 2 instructions
0x38	LOAD and STORE instructions
0x39	LOAD instructions
0x3A	STORE instructions
AHB events (only available if core is connected to a LEON4 Debug Support Unit):	
0x40	AHB IDLE cycles. Filtered on CPU/AHBM if SU(1) = ‘1’
0x41	AHB BUSY cycles. Filtered on CPU/AHBM if SU(1) = ‘1’
0x42	AHB NON-SEQUENTIAL transfers. Filtered on CPU/AHBM if SU(1) = ‘1’
0x43	AHB SEQUENTIAL transfers. Filtered on CPU/AHBM if SU(1) = ‘1’
0x44	AHB read accesses. Filtered on CPU/AHBM if SU(1) = ‘1’
0x45	AHB write accesses. Filtered on CPU/AHBM if SU(1) = ‘1’

*Table 1407.*Event types and IDs

ID	Event description
0x46	AHB byte accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x47	AHB half-word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x48	AHB word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x49	AHB double word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x4A	AHB quad word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x4B	AHB eight word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x4C	AHB waitstates. Filtered on CPU/AHBM if SU(1) = '1'
0x4D	AHB RETRY responses. Filtered on CPU/AHBM if SU(1) = '1'
0x4E	AHB SPLIT responses. Filtered on CPU/AHBM if SU(1) = '1'
0x4F	AHB SPLIT delay. Filtered on CPU/AHBM if SU(1) = '1'
0x50	AHB bus locked. Filtered on CPU/AHBM if SU(1) = '1'
0x51-0x5F	Reserved
Implementation specific events:	
0x60 - 0x6F	External event 0 - 15. Filtered on CPU/AHBM if SU(1) = '1'.
AHB events (only available if core is connected to a standalone AHB trace buffer):	
0x70	AHB IDLE cycles. Filtered on CPU/AHBM if SU(1) = '1'
0x71	AHB BUSY cycles. Filtered on CPU/AHBM if SU(1) = '1'
0x72	AHB NON-SEQUENTIAL transfers. Filtered on CPU/AHBM if SU(1) = '1'
0x73	AHB SEQUENTIAL transfers. Filtered on CPU/AHBM if SU(1) = '1'
0x74	AHB read accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x75	AHB write accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x76	AHB byte accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x77	AHB half-word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x78	AHB word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x79	AHB double word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x7A	AHB quad word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x7B	AHB eight word accesses. Filtered on CPU/AHBM if SU(1) = '1'
0x7C	AHB waitstates. Filtered on CPU/AHBM if SU(1) = '1'
0x7D	AHB RETRY responses. Filtered on CPU/AHBM if SU(1) = '1'
0x7E	AHB SPLIT responses. Filtered on CPU/AHBM if SU(1) = '1'
0x7F	AHB SPLIT delay. Filtered on CPU/AHBM if SU(1) = '1'
Events generated from REQ/GNT signals (only available if core has been implemented with VHDL generic reqsel /=0)	
0x80 - 0x8F	Active when master selected by CPU/AHBM field has request asserted while grant is asserted for the master correspoding to the least significant nibble of the event ID. 0x80 is master 0 grant, 0x81 is master 1 grant, .., and so on.
0x90 - 0x9F	Active when master selected by CPU/AHBM field has request asserted while grant is deasserted for the master correspoding to the least significant nibble of the event ID. 0x90 is master 0 grant, 0x91 is master 1 grant, .., and so on.

Note that IDs 0x39 (LOAD instructions) and 0x3A (STORE instructions) will both count all LDST and SWAP instructions. The sum of events counted for 0x39 and 0x3A may therefore be larger than the number of events counted with ID 0x38 (LOAD and STORE instructions).

Event 0x00 - 0x3A can be counted of the core has been connected to one or several LEON4 processor cores. Counting of events 0x40 - 0x5F requires that the core is connected to a LEON4 Debug Support Unit (DSU). The core's Counter control registers have a field that shows if the core has been imple-

mented with this connection. The documentation for the Debug Support Unit contains more information on events 0x40 - 0x5F. Please note that the statistical outputs from the DSU may be subject to AHB trace buffer filters. The same applies to events 0x70 - 0x7F that can come from an AHBTRACE core.

The core can also be implemented with support for counting up to 15 external events. These events can come from any source, but should be clocked by a clock which is synchronous with the AMBA clock used for the L4STAT core.

78.2 Multiple APB interfaces

The core can be implemented with two AMBA APB interfaces. The first APB interface always has precedence when both interfaces handle write operations to the same address.

78.3 Registers

The L4STAT core is programmed through registers mapped into APB address space.

Table 1408. L4STAT counter control register

APB address offset	Register
0x00	Counter 0 value register
0x04	Counter 1 value register
4 * *n*	Counter *n* value register
0x100	Counter 0 control register
0x104	Counter 1 control register
0x100 + (4 * *n*)	Counter *n* control register
0x200	Counter 0 max/latch register
0x204	Counter 1 max/latch register
0x200 + (4 * *n*)	Counter *n* max/latch register
0x300	Timestamp register

Note: Revision 0 of this IP core had control registers starting at 0x80, max/latch registers starting at 0x100 and the timestamp register at 0x180. This IP core documentation is valid for revision 1 of the IP core.

78.3.1 Counter Value Register

*Table 1409.*0x000+n.4 - CVALn - Counter value register

31	0
CVAL	
NR	
rw	

31: 0 Counter value (CVAL) - This register holds the current value of the counter. If the core has been implemented with support for keeping the maximum count (MC field of Counter control register is ‘1’) and the Counter control register field CD is ‘1’, then the value displayed by this register will be the maximum counter value reached with the settings in the counter’s control register. Writing to this register will write both to the counter and, if implemented, the hold register for the maximum counter value.

78.3.2 Counter Control Register

*Table 1410.*0x100+n.4 - CCTRLn - Counter control register

31 23	22	21	20	19	18	17	16	15 14	13	12	11 4	3 0
NCNT	MC	IA	DS	EE	AE	EL	CD	SU	CL	EN	EVENT ID	CPU/AHBM
*	*	*	*	*	*	NR	NR	NR	NR	0	NR	NR
r	r	r	r	r	r	rw	rw	rw	rw	rw	rw	rw

31: 23 Number of counters (NCNT) - Number of implemented counters - 1

Note revision 0 of this core used bits 31:28 to indicate the number of CPUs. This manual applies to revision 1 of the core.

22 Maximum count (MC) - If this field is ‘1’ then this counter has support for keeping the maximum count value

21 Internal AHB count (IA) - If this field is ‘1’ the core supports events 0x17 and 0x18

20 DSU support (DS) - If this field is ‘1’ the core supports events 0x40-0x5F

19 External events (EE) - If this field is ‘1’ the core supports external events (events 0x60 - 0x6F)

18 AHBTRACE Events (AE) - If this field is ‘1’ the core supports events 0x70 - 0x7F.

17 Event Level (EL) - The value of this field determines the level where the counter keeps running when the CD field below has been set to ‘1’. If this field is ‘0’ the counter will count the time between event assertions. If this field is ‘1’ the counter will count the cycles where the event is asserted. This field can only be set if the MC field of this register is ‘1’.

16 Count maximum duration (CD) - If this bit is set to ‘1’ the core will save the maximum time the selected event has been at the level specified by the EL field. This also means that the counter will be reset when the event is activated or deactivated depending on the value of the EL field.

When this bit is set to ‘1’, the value shown in the counter value register will be the maximum current value which may be different from the current value of the counter.

This field can only be set if the MC field of this register is ‘1’.

15: 14 Supervisor/User mode filter (SU) - “01” - Only count supervisor mode events, “10” - Only count user mode events, others values - Count events regardless of user or supervisor mode. This setting only applies to events 0x0 - 0x3A.

When SU = “1x” only events generated by the CPU/AHB master specified in the CPU/AHBM field will be counted. This applies to events 0x40 - 0x7F

: 13 Clear counter on read (CL) - If this bit is set the counter will be cleared when the counter’s value is read. The register holding the maximum value will also be cleared, if implemented.

If an event occurs in the same cycle as the counter is cleared by a read then the event will not be counted. The counter latch register can be used to guarantee that no events are lost.

12 Enable counter (EN) - Enable counter

11: 4 Event ID to be counted

3: 0 CPU or AHB master to monitor.(CPU/AHBM) - The value of this field does not matter when selecting one of the events coming from the Debug Support Unit or one of the external events.

78.3.3 Counter Max/Latch Register

*Table 1411.*0x200+4n - CSVALn - Counter max/latch register

31	0
CSVAL	
NR	
rw*	

31: 0 Counter max/latch value (CSVAL) - This register holds the current value of the counter max/latch register. It is only available for a specific counter If the core has been implemented with support for keeping the maximum count (MC field of Counter control register is ‘1’).

If the counter control register field CD is ‘1’, then the value displayed by this register will be the maximum counter value reached with the settings in the counter’s control register.

If the counter control register field CDis ‘0’, then the value displayed by this register is the latched (saved) counter value. The counter value is saved whenever a write access is made to the core in address range 0x100 - 0x1FC (all counters are saved simultaneously). If the counter control register CL field is set, then the current counter value will be cleared when the counter value is saved into this register.

78.3.4 Timestamp Register

*Table 1412.*0x300 - TSTAMP - Timestamp register

31	0
TSTAMP	
NR	
rw*	

31: 0 Timestamp (TSTAMP) - Timestamp taken at latch of counters

78.4 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x047. For description of vendor and device identifiers see GRLIB IP Library User’s Manual.

78.5 Implementation

78.5.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User’s Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

78.6 Configuration options

Table 1413 shows the configuration options of the core (VHDL generics).

*Table 1413.*Configuration options

Generic	Function	Allowed range	Default
pindex	Selects which APB select signal (PSEL) will be used to access the statistical unit	0 to NAPBMAX-1	0
paddr	The 12-bit MSB APB address	0 to 16#FFF#	0
pmask	The APB address mask. Needs to be set to 16#FFE# if max/latch registers are enabled (VHDL generic clatch).	0 to 16#FFF#	16#FFF#
ncnt	Defines the number of counters	1 to 32	4
ncpu	Defines the number of CPUs monitored	1 - 16	1
nmax	If this generic is > 0, the core will include functionality for tracking the longest consecutive time that an event is active or inactive. The functionality will be available for the *nmax* first counters.	0 - 32	0
lahben	If this generic is 1, the core makes use of the AHBSI input for events 0x17 and 0x18, otherwise the AHBSI input is unused and events 0x17 and 0x18 will never increment a counter.	0 - 1	0
dsuen	If this generic is 1, the core makes use of the DSUO input for events 0x40 - 0x5F, otherwise the DSUO input is unused and events 0x40 - 0x5F will never increment a counter.	0 - 1	0
nextev	Defines the number of external events monitored	0 - 16	0
apb2en	Enables the second APB port on the core.	0 - 1	0
pindex2	Selects which APB select signal (PSEL) will be used to access the second interface of the statistical unit	0 to NAPBMAX-1	0
paddr2	The 12-bit MSB APB address for second interface	0 to 16#FFF#	0
pmask2	The APB address mask for second interface	0 to 16#FFF#	16#FFF#
astaten	If this generic is 1, the core makes use of the ASTAT input for events 0x70 - 0x7F, otherwise the ASTAT input is unused and events 0x70 - 0x7F will never increment a counter.	0 - 1	0
selreq	Support STATI.REQ/SEL events. If selreq is nonzero then the value+1 defines the number of monitored sel/req signals.	0 - 15	0
clatch	Include support for counter max/latch registers and time-stamp.	0 - 1	0
forcer0	For core to revision 0. If this generic is set to 1 then the maximum number of supported counters is 32 and the register address offsets and layout of the control register changes to comply to revision 0 of the IP core.	0 - 1	0

78.7 Signal descriptions

Table 1414 shows the interface signals of the core (VHDL ports).

*Table 1414.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
AHBSI	*	Input	AHB slave input signals	-
DBGO		Input	LEON4 debug output signals	-
DSUO	ASTAT	Input	DSU4 output signals	-
STATI	EVENT[15:0]	Input	Input for 16 user defined events	High
	ESOURCE[3:0]	Input	CPU/AHBM for each EVENT	-
	REQ[15:0]	Input	Input for 16 user defined request signals	High
	SEL[15:0]	Input	Input for 16 user defined select/grant signals	-
	TIMER[31:0]	Input	Time stamp value used when VHDL generic clatch /= 0	-
APB2I	*	Input	Secondary APB slave input signals	-
APB2O	*	Output	Secondary APB slave output signals	-
ASTAT	*	Input	AHBTRACE output signals	-

* see GRLIB IP Library User's Manual

78.8 Library dependencies

Table 1415 shows libraries used when instantiating the core (VHDL libraries).

*Table 1415.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	LEON3	Signals	Signal definitions
GAISLER	LEON4	Signals, component	Component declaration

78.9 Component declaration

The core has the following component declaration.

```
library gaisler;
use gaisler.leon3.all;
use gausler.leon4.all;

entity l4stat is
  generic (
    pindex      : integer := 0;
    paddr       : integer := 0;
    pmask       : integer := 16#fff#;
    ncnt        : integer := 4;
    ncpu        : integer := 1
    );
  port (
    rstn   : in std_ulogic;
    clk    : in std_ulogic;
```

```
    apbi   : in apb_slv_in_type;
    apbo   : out apb_slv_out_type;
    ahbsi  : in  ahb_slv_in_type;
    dbgo   : in l4_debug_out_vector(0 to NCPU-1));
end;
```

This example shows how the core can be instantiated.

```
library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.leon4.all;

begin

l4sgen : if CFG_L4S_ENABLE = 1 generate
    l4stat0 : l4stat
      generic map (pindex => 11, paddr => 11, ncnt => CFG_L4S_CNT, ncpu => CFG_NCPU)
      port map (rstn, clkm, apbi, apbo(11), ahbsi, dbgo);
end generate;
```

79 LEON_DSU_STAT_BASE - LEON3/4 SUBSYSTEM

79.1 Overview

LEON_DSU_STAT_BASE is a subsystem component that can be used to instantiate LEON3 or LEON4 processors together with their respective debug support unit (DSU) and a statistics unit (performance counters).

LEON_DSU_STAT_BASE allows to select between LEON3 and LEON4, with FT options optionally enabled for both variants. The subsystem also supports sharing one FPU between several processors.

The subsystem makes use of the following interfaces:

- Clock and reset input
- One AHB master output per processor, shared AHB master input and AHB slave inputs for all processors
- One interrupt controller interface per processor
- One AMBA APB port for, optional, performance counters
- Performance counter inputs
- DSU AHB slave interface and trace buffer inputs
- DSU enable, break, active and timer stop signals

The subsystem does not provide any additional functionality to the LEON, DSU and statistics IP cores. The subsystem is provided as a convenient way to include the three separate IP cores and to decrease the amount of top-level code required in designs that can be configured to select between LEON3 and LEON4.

The subsystem is primarily targeted to FPGA designs and for designs without a clock gate unit. The design does not propagate scan test settings and memory BIST signals.

79.2 Operation

79.2.1 Operational model

For a subsystem with LEON3, please refer to the documentation for:

- LEON3, section 80
- DSU3, section 24
- L3STAT, section 77

For a subsystem with LEON4, please refer to the documentation for:

- LEON4, section 81
- DSU4, section 25
- L4STAT, section 78

79.2.2 Bus widths

LEON_DSU_STAT_BASE allows to select between LEON3 and LEON4. If LEON4 is selected then the GRLIB AMBA bus width needs to be set to 64 or 128 bits. This is accomplished by changing the GRLIB configuration (GRLIB_CONFIG) package. The configuration package is described in GRLIB IP Library User's Manual (grlib.pdf). See also section 79.7 for references to example usage of LEON_DSU_STAT_BASE where the designs select the bus width depending on the selection between LEON3 and LEON4.

79.3 Implementation

Please refer to the IP core documentation listed in section 79.2.1.

79.4 Configuration options

Table 1416 shows the configuration options of the core (VHDL generics).

*Table 1416.*Configuration options

Generic name	Function	Allowed range	Default
leon	Selects between LEON3 (3) and LEON4 (4)	0, 3, 4	0
ncpu	Number of processors. Propagated to generic with the same name on LEON and DSU instances.	1 - 16	1
fabtech	Propagated to generic with the same name on LEON instance(s) and (optional) shared GRFPU.	0 - NTECH	0
memtech	Propagated to generic with the same name on LEON instance(s). Propagated to *tech* generic on DSU. See also memtechmod generic below	0 - NTECH	0
memtechmod	memtech + memtechmod are assigned to the memtech VHDL generic on the LEON3 and LEON4 instances. memtech mod can be used to modify memtech to set the high bits forcing inferred memory for registers files and MMU memories. See documentation for memtech in LEON3 and LEON4 documentation.	-	0
nwindows	Propagated to generic with same name on LEON instance(s).	2 - 32	8
dsu	Propagated to generic with same name on LEON instance(s). Selects if DSU core is instantiated in subsystem.	0 - 1	0
fpu	Propagated to generic with same name on LEON instance(s). Corresponding generic on LEON is assigned with the value: *fpu + 32*grfpush*	0 - 63	0
v8	Propagated to generic with same name on LEON instance(s).	0 - 63	0
cp	Unused. cp generic on LEON instances is hardcoded to 0.	0 - 1	0
mac	Propagated to generic with same name on LEON instance(s).	0 - 1	0
pclow	Propagated to generic with same name on LEON instance(s).	0 - 2	2
notag	Propagated to generic with same name on LEON instance(s).	0 - 1	0
nwp	Propagated to generic with same name on LEON instance(s).	0 - 4	0
icen	Propagated to generic with same name on LEON instance(s).	0 - 1	0
irepl	Propagated to generic with same name on LEON instance(s).	0 - 2	2
isets	Propagated to generic with same name on LEON instance(s).	1 - 4	4
ilinesize	Propagated to generic with same name on LEON instance(s).	4 - 8	4
isetsize	Propagated to generic with same name on LEON instance(s).	1 - 256	1

*Table 1416.*Configuration options

Generic name	Function	Allowed range	Default
isetlock	Propagated to generic with same name on LEON instance(s).	0 - 1	0
dcen	Propagated to generic with same name on LEON instance(s).	0 - 1	0
drepl	Propagated to generic with same name on LEON instance(s).	0 - 2	2
dsets	Propagated to generic with same name on LEON instance(s).	1 - 4	1
dlinesize	Propagated to generic with same name on LEON instance(s).	4 - 8	4
dsetsize	Propagated to generic with same name on LEON instance(s).	1 - 256	1
dsetlock	Propagated to generic with same name on LEON instance(s).	0 - 1	0
dsnoop	Propagated to generic with same name on LEON instance(s).	0 - 6	0
ilram	Propagated to generic with same name on LEON instance(s).	0 - 1	0
ilramsize	Propagated to generic with same name on LEON instance(s).	1 - 512	1
ilramstart	Propagated to generic with same name on LEON instance(s).	0 - 255	16#8e#
dlram	Propagated to generic with same name on LEON instance(s).	0 - 1	0
dlramsize	Propagated to generic with same name on LEON instance(s).	1 - 512	1
dlramstart	Propagated to generic with same name on LEON instance(s).	0 - 255	16#8f#
mmuen	Propagated to generic with same name on LEON instance(s).	0 - 2	0
itlbnum	Propagated to generic with same name on LEON instance(s).	2 - 64	8
dtlbnum	Propagated to generic with same name on LEON instance(s).	2 - 64	8
tlb_type	Propagated to generic with same name on LEON instance(s).	0 - 3	1
tlb_rep	Propagated to generic with same name on LEON instance(s).	0 - 1	0
lddel	Propagated to generic with same name on LEON instance(s).	1 - 2	2
disas	Propagated to generic with same name on LEON instance(s).	0 - 2	0
tbuf	Propagated to generic with same name on LEON instance(s).	0 - 128	0
pwd	Propagated to generic with same name on LEON instance(s).	0 - 2	2
svt	Propagated to generic with same name on LEON instance(s).	0 - 1	1
rstaddr	Propagated to generic with same name on LEON instance(s).	-	0

*Table 1416.*Configuration options

Generic name	Function	Allowed range	Default
smp	Propagated to generic with same name on LEON instance(s).	0 - 31	0
cached	Propagated to generic with same name on LEON instance(s).	-	0
clk2x	Double clocking is currently unsupported with LEON_DSU_STAT_BASE. Leave at 0.	-	0
wbmask	Propagated to generic with same name on LEON4 instance(s). Not used for LEON3.	-	0
busw	Propagated to generic with same name on LEON4 instance(s). Not used for LEON3.	-	64
netlist	Propagated to generic with same name on LEON instance(s).	-	0
ft	Configured fault-tolerance. For LEON3 this value combines the settings for *iuft*, *fpft* and *cmft* in the following way: *iuft + (cmft) * 8 + fpft*2048*. For LEON4 the *ft* value is directly assigned to the generic by the same name.	-	0
npasi	Propagated to generic with same name on LEON instance(s).	0 - 1	0
pwrpsr	Propagated to generic with same name on LEON instance(s).	0 - 1	0
rex	Propagated to generic with same name on LEON instance(s).	0 - 1	0
altwin	Propagated to generic with same name on LEON3 instance(s). Not used for LEON4.	0 - 1	0
ahbpipe	Unused	-	0
mmupgsz	Propagated to generic with same name on LEON instance(s).	0 - 4	0
grfpush	Enabled shared FPU between instantiated LEONs.	0 - 1	0
dsu_hindex	Propagated to *hindex* generic on DSU instance.	-	2
dsu_haddr	Propagated to *haddr* generic on DSU instance.	-	16#900#
dsu_hmask	Propagated to *hmask* generic on DSU instance.	-	16#F00#
atbsz	Propagated to *kbytes* generic on DSU instance.	-	4
stat	Enables LEON statistics unit corresponding to *leon* selection of processor.	0 - 1	0
stat_pindex	Propagated to *pindex* generic on L*STAT instance.	-	0
stat_paddr	Propagated to *paddr* generic on L*STAT instance.	-	0
stat_pmask	Propagated to *pmask* generic on L*STAT instance.	-	16#FFC#
stat_ncnt	Propagated to *ncnt* generic on L*STAT instance.	-	1
stat_nmax	Propagated to *nmax* generic on L*STAT instance.	-	0

79.5 Signal descriptions

Table 1417 shows the interface signals of the core (VHDL ports).

*Table 1417.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
AHBCLK	N/A	Input	System clock	-
CPUCLK	N/A	Input	System clock	-
HCLKEN	N/A	Input	Double-clocking signal. Tie HIGH	HIGH
LEON_AHBMI	*	Input	LEON AHB master input signals	-
LEON_AHBMO[]	*	Output	LEON AHB master output signals, one per processor	-
LEON_AHBSI	*	Input	LEON AHB slave input signals (for snooping)	-
LEON_AHBSO	*	Input	LEON AHB slave output signals (for plug&play decoding)	-
IRQI	-	Input	Interrupt controller interface see LEON documentation	-
IRQO	-	Output		-
STAT_APBI	*	Input	L*STAT APB slave input signals	-
STAT_APBO	*	Output	L*STAT APB slave output signals	-
STAT_AHBSI	*	Input	L*STAT AHB slave input signals	-
STATI	-	Input	L*STAT input signal. See L3STAT/L4STAT documentation.	-
DSU_AHBSI	*	Input	DSU AHB slave input signals	-
DSU_AHBSO	*	Output	DSU AHB slave output signals	-
DSU_TAHBMI	*	Input	DSU AHB master input signals, used for AHB tracing	-
DSU_TAHBSI	*	Input	DSU AHB slave input signals, used for AHB tracing	-
SYSI	DSU_ENABLE	Input	Connected to DSU DSUI.ENABLE input	HIGH
	DSU_BREAK	Input	Connected to DSU DSUI.BREAK input	HIGH
SYSO	DSU_ACTIVE	Output	Connected to DSU DSUO.ACTIVE output	HIGH
	DSU_TSTOP	Output	Connected to DSU DSIO.TSTOP output	HIGH

* see GRLIB IP Library User's Manual

79.6 Library dependencies

Table 1418 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1418.*Library dependencies

Library	Package	Imported unit(s)	Description
GAISLER	SUBSYS	Component, signals	Component and signal definitions
GAISLER	LEON3	Signals	Interrupt controller signals
GRLIB	AMBA	Signals	AMBA signal definitions

79.7 Instantiation

Examples on how to use the subsystem can be seen in several GRLIB template designs, including:

- designs/leon3-gr-cpci-xc4v

- designs/leon3-gr-cpci-xc7k
- designs/leon3-gr-pci-xc5v
- designs/leon3-xilinx-kc705
- designs/leon3-xilinx-ml50x
- designs/leon3-xilinx-ml510
- designs/leon3-xilinx-vc707

Note that the Makefile in these designs also contains special conditions that depend on the selection between LEON3 and LEON4.

80 LEON3/FT - High-performance SPARC V8 32-bit Processor

80.1 Overview

LEON3 is a 32-bit processor core conforming to the IEEE-1754 (SPARC V8) architecture. It is designed for embedded applications, combining high performance with low complexity and low power consumption.

The LEON3 core has the following main features: 7-stage pipeline with Harvard architecture, separate instruction and data caches, memory management unit, hardware multiplier and divider, on-chip debug support and multi-processor extensions.

The LEON3 processor can be enhanced with fault-tolerance against SEU errors (referred to as LEON3FT). The fault-tolerance is focused on the protection of on-chip RAM blocks, which are used to implement IU/FPU register files and the cache memory. Configuring the processor to implement fault-tolerance enables additional internal registers, register fields and changes the processor's plug&play device ID. This documentation describes both the LEON3 and LEON3FT versions of the processor.

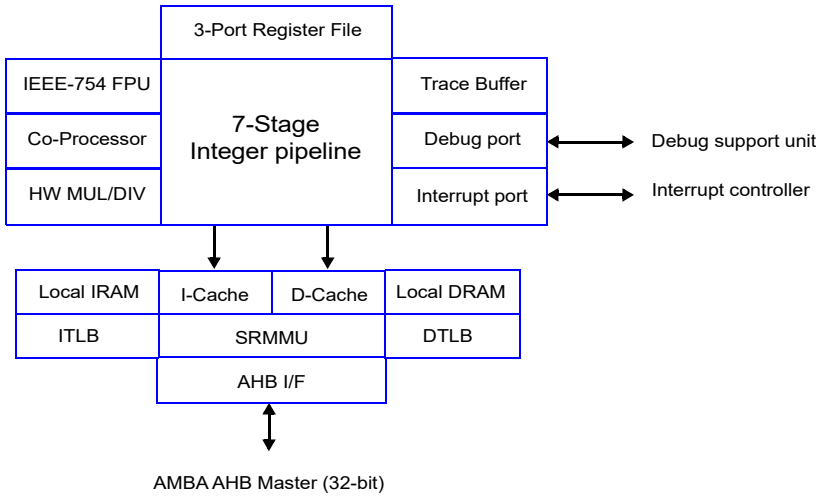


Figure 217. LEON3 processor core block diagram

Note: This manual describes the full functionality of the LEON3 core. Through the use of VHDL generics, parts of the described functionality can be suppressed or modified to generate a smaller or faster implementation. A comparison with earlier revisions can be found in section 80.13.

Please also refer to the *LEON/GRLIB Configuration and Development Guide* for recommendations on system design and LEON3 configuration.

80.1.1 Integer unit

The LEON3 integer unit implements the full SPARC V8 manual, including hardware multiply and divide instructions. The number of register windows is configurable within the limit of the SPARC manual (2 - 32), with a default setting of 8. The pipeline consists of 7 stages with a separate instruction and data cache interface (Harvard architecture).

80.1.2 Cache sub-system

LEON3 has a highly configurable cache system, consisting of a separate instruction and data cache. Both caches can be configured with 1 - 4 ways, 1 - 256 KiB/way, 16 or 32 bytes per line. The instruc-

tion cache maintains one valid bit per 32-bit word and uses streaming during line-refill to minimize refill latency. The data cache has one valid bit per cache line, uses write-through policy and implements a double-word write-buffer. Bus-snooping on the AHB bus can be used to maintain cache coherency for the data cache. Local scratch pad ram can be added to either of the instruction and data caches to allow 0-waitstates access instruction or data memory without any AHB bus access.

80.1.3 Floating-point unit and co-processor

The LEON3 integer unit provides interfaces for a floating-point unit (FPU), and a custom co-processor. Two FPU controllers are available, one for the high-performance GRFPU and one for the GRFPU-Lite core. The floating-point processors and co-processor execute in parallel with the integer unit, and does not block the operation unless a data or resource dependency exists. Note that the FPUs are provided separately.

80.1.4 Memory management unit

A SPARC V8 Reference Memory Management Unit (SRMMU) can optionally be enabled. The SRMMU implements the full SPARC V8 MMU specification, and provides mapping between multiple 32-bit virtual address spaces and physical memory. A three-level hardware table-walk is implemented, and the MMU can be configured to up to 64 fully associative TLB entries per implemented TLB.

80.1.5 On-chip debug support

The LEON3 pipeline includes functionality to allow non-intrusive debugging on target hardware. To aid software debugging, up to four watchpoint registers can be enabled. Each register can cause a breakpoint trap on an arbitrary instruction or data address range. When the (optional) debug support unit is attached, the watchpoints can be used to enter debug mode. Through a debug support interface, full access to all processor registers and caches is provided. The debug interfaces also allows single stepping, instruction tracing and hardware breakpoint/watchpoint control. An internal trace buffer can monitor and store executed instructions, which can later be read out via the debug interface.

80.1.6 Interrupt interface

LEON3 supports the SPARC V8 interrupt model with a total of 15 asynchronous interrupts. The interrupt interface provides functionality to both generate and acknowledge interrupts.

80.1.7 AMBA interface

The cache system implements an AMBA AHB master to load and store data to/from the caches. The interface is compliant with the AMBA-2.0 standard. During line refill, incremental bursts are generated to optimise the data transfer. The processor also has a snoop AHB slave input port which is used to monitor the accesses made by other masters, if snooping has been enabled.

80.1.8 Power-down mode

The LEON3 processor core implements a power-down mode, which halts the pipeline and caches until the next interrupt. The processor supports optional clock gating during the power down period by providing a clock-enable signal that can be tied to an external clock gate cell, and by providing a separate clock input for the small part of the CPU that needs to run during power-down to check for wake-up conditions and maintain cache coherency.

80.1.9 Multi-processor support

LEON3 is designed to be used in multi-processor systems. Each processor has a unique index to allow processor enumeration. The write-through caches and snooping mechanism guarantees cache coherency in shared-memory systems.

80.2 LEON3 integer unit

80.2.1 Overview

The LEON3 integer unit implements the integer part of the SPARC V8 instruction set. The implementation is focused on high performance and low complexity. The LEON3 integer unit has the following main features:

- 7-stage instruction pipeline
- Separate instruction and data cache interface
- Support for 2 - 32 register windows
- Hardware multiplier with optional 16x16 bit MAC and 40-bit accumulator
- Radix-2 divider (non-restoring)
- Static branch prediction
- Single-vector trapping for reduced code size

Figure 218 shows a block diagram of the integer unit.

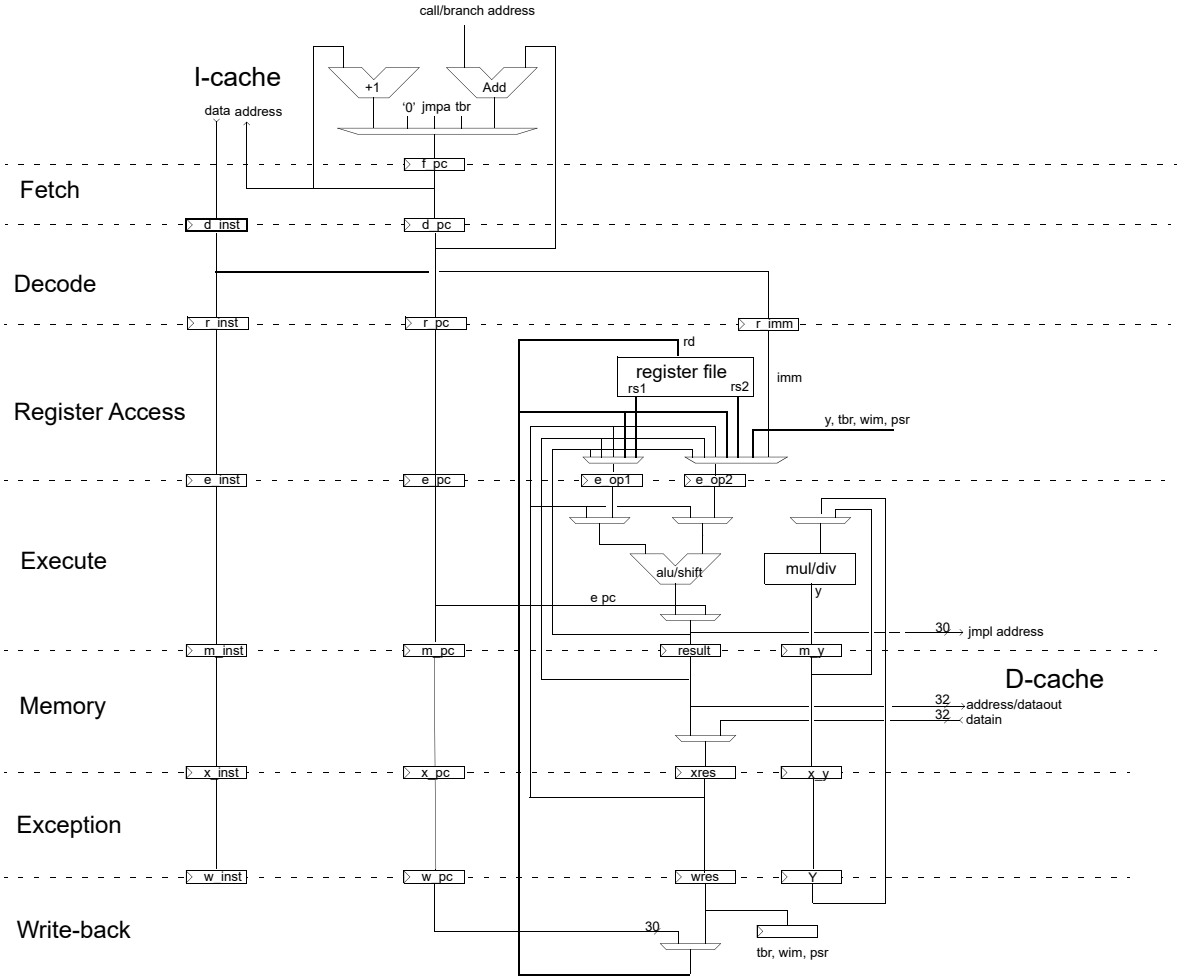


Figure 218. LEON3 integer unit datapath diagram

80.2.2 Instruction pipeline

The LEON3 integer unit uses a single instruction issue pipeline with 7 stages:

1. FE (Instruction Fetch): If the instruction cache is enabled, the instruction is fetched from the instruction cache. Otherwise, the fetch is forwarded to the AHB bus. The instruction is valid at the end of this stage and is latched inside the IU.
2. DE (Decode): The instruction is decoded and the CALL and Branch target addresses are generated.
3. RA (Register access): Operands are read from the register file or from internal data bypasses.
4. EX (Execute): ALU, logical, and shift operations are performed. For memory operations (e.g., LD) and for JMPL/RETT, the address is generated.
5. ME (Memory): Data cache is read or written at this time.
6. XC (Exception) Traps and interrupts are resolved. For cache reads, the data is aligned as appropriate.
7. WR (Write): The result of any ALU, logical, shift, or cache operations are written back to the register file.

Table 1419 lists the cycles per instruction (assuming cache hit and no icc or load interlock):

*Table 1419.*Instruction timing

Instruction	Cycles (MMU disabled)	Cycles (MMU fast-write)	Cycles (MMU slow-write)
JMPL	3[1]	3[1]	3[1]
JMPL,RETT pair	4	4	4
Double load	2	2	2
Single store	2	2	4
Double store	3	3	5
SMUL/UMUL	1/4[2]	1/4[2]	1/4 [2]
SDIV/UDIV	35	35	35
Taken Trap	5	5	5
Atomic load/store	3	3	5
All other instructions	**1**	**1**	**1**

[1] Assuming instruction in JMPL delay slot takes one cycle. Additional cycles spent in the delay slot will reduce the effective time of the JMPL to 2 or 1.

[2] Multiplication cycle count is 1 clock (1 clock issue rate, 2 clock data latency), for the 32x32 multiplier and 4 clocks (issue rate, 4/5 clocks data latency for standard/pipelined version) for the 16x16 version.

A number of conditions can extend an instruction's duration in the pipeline:

Branch interlock: When a conditional branch or trap is performed 1-2 cycles after an instruction which modifies the condition codes, 1-2 cycles of delay is added to allow the condition to be computed. If static branch prediction is enabled, this extra delay is incurred only if the branch is not taken.

Load delay: When using data resulting on a load shortly after the load, the instruction will be delayed to satisfy the pipeline's load delay. The processor pipeline can be configured for one or two cycles load delay. One cycle load delay will improve performance at a fixed speed but may degrade maximum clock frequency due to added forwarding paths in the pipeline.

Mul latency: For pipelined multiplier implementations there is 1 cycle extra data latency, accessing the result immediately after a MUL or MAC will then add one cycle pipeline delay.

Hold cycles: During cache miss processing or when blocking on the store buffer, the pipeline will be held still until the data is ready, effectively extending the execution time of the instruction causing the miss by the corresponding number of cycles. Note that since the whole pipeline is held still, hold cycles will not mask load delay or interlock delays. For instance on a load cache miss followed by a data-dependent instruction, both hold cycles and load delay will be incurred.

FPU/Coprocessor: The floating-point unit or coprocessor may need to hold the pipeline or extend a specific instruction. When this is done is specific to the FP/CP unit.

80.2.3 SPARC Implementor's ID

Cobham Gaisler is assigned number 15 (0xF) as SPARC implementor's identification. This value is hard-coded into bits 31:28 in the %psr register. The version number for LEON3 is 3, which is hard-coded in to bits 27:24 of the %psr.

80.2.4 Divide instructions

Full support for SPARC V8 divide instructions is provided (SDIV, UDIV, SDIVCC & UDIVCC). The divide instructions perform a 64-by-32 bit divide and produce a 32-bit result. Rounding and overflow detection is performed as defined in the SPARC V8 manual.

The divide instruction is required for full SPARC V8 compliance but can be configured out to save area using the *v8* VHDL generic.

80.2.5 Multiply instructions

The LEON processor supports the SPARC integer multiply instructions UMUL, SMUL UMULCC and SMULCC. These instructions perform a 32x32-bit integer multiply, producing a 64-bit result. SMUL and SMULCC performs signed multiply while UMUL and UMULCC performs unsigned multiply. UMULCC and SMULCC also set the condition codes to reflect the result. The multiply instructions are performed using a 32x32 pipelined hardware multiplier, or a 16x16 hardware multiplier which is iterated four times. To improve the maximum frequency on slow technologies, the 16x16 multiplier can optionally be provided with a pipeline stage.

The multiply instruction is required for full SPARC V8 compliance, but can be configured out to save area using the *v8* VHDL generic.

80.2.6 Multiply and accumulate instructions

To accelerate DSP algorithms, two multiply&accumulate instructions are implemented: UMAC and SMAC. The UMAC performs an unsigned 16-bit multiply, producing a 32-bit result, and adds the result to a 40-bit accumulator made up by the 8 lsb bits from the %y register and the %asr18 register. The least significant 32 bits are also written to the destination register. SMAC works similarly but performs signed multiply and accumulate. The MAC instructions execute in one clock but have two clocks latency, meaning that one pipeline stall cycle will be inserted if the following instruction uses the destination register of the MAC as a source operand.

The UMAC and SMAC instructions occupy the unused opcodes op=10,op3=1111110 for UMAC and op=10,op3=1111111 for SMAC.

Assembler syntax:

```
umac rs1, reg_imm, rd
smac rs1, reg_imm, rd
```

Operation:

```
prod[31:0] = rs1[15:0] * reg_imm[15:0]
result[39:0] = (Y[7:0] & %asr18[31:0]) + prod[31:0]
(Y[7:0] & %asr18[31:0]) = result[39:0]
rd = result[31:0]
```

%asr18 can be read and written using the RDASR and WRASR instructions.

The MAC instructions are an optional extension to SPARC V8, and enabled using the *mac* VHDL generic. The multiply and accumulate support also requires MUL/DIV support enabled by the *v8* VHDL generic and can only be used together with a 16x16 multiplier.

80.2.7 Compare and Swap instruction (CASA)

LEON3 implements the SPARC V9 Compare and Swap Alternative (CASA) instruction. The CASA instruction operates as described in the SPARC V9 manual. The instruction is privileged but setting ASI = 0xA (user data) will allow it to be used in user mode.

Software can determine if the processor supports CASA by checking the NOTAG field of the %asr17 register described in section 80.11.2.

80.2.8 Branch prediction

Static branch prediction can be optionally be enabled, and reduces the penalty for branches preceded by an instruction that modifies the integer condition codes (see section 80.2.2). The predictor uses a branch-always strategy, and starts fetching instruction from the branch address. On a prediction hit, 1 or 2 clock cycles are saved, and there is no extra penalty incurred for misprediction as long as the branch target can be fetched from cache. Branch prediction improves the performance with 10 - 20% on most control-type applications.

80.2.9 Register file data protection

Register file data protection is available for the fault-tolerant version of the LEON3 and is enabled via a VHDL generic. Register file data protection is described in section 80.9.2.

80.2.10 Hardware breakpoints

The integer unit can be configured to include up to four hardware breakpoints. Each breakpoint consists of a pair of ancillary state registers (see section 80.11.3). Any binary aligned address range can be watched for instruction or data access, and on a breakpoint hit, trap 0x0B is generated.

80.2.11 Instruction trace buffer

The (optional) instruction trace buffer consists of a circular buffer that stores executed instructions. This is enabled and accessed only through the processor's debug port via the Debug Support Unit. When enabled, the following information is stored in real time, without affecting performance:

- Instruction address and opcode
- Instruction result
- Load/store data and address
- Trap information
- 30-bit time tag

The operation and control of the trace buffer is further described in section 24.4. Note that in multi-processor systems, each processor has its own trace buffer allowing simultaneous tracing of all instruction streams.

The size of the trace buffer is configurable from 1 to 64 KiB through the *tbuf* VHDL generic. If the value of tbuf is in the 65-128 range, a two-port instruction trace buffer of size *tbuf*-64 KiB will be used, allowing contextual reading of instructions while tracing is ongoing.

80.2.12 Processor configuration register

The ancillary state register 17 (%asr17) provides information on how various configuration options were set during synthesis. This can be used to enhance the performance of software, or to support enumeration in multi-processor systems. See section 80.11.2 for layout.

80.2.13 Exceptions

LEON3 adheres to the general SPARC trap model. The table below shows the implemented traps and their individual priority. When PSR (processor status register) bit ET=0, an exception trap causes the processor to halt execution and enter error mode, and the external error signal will then be asserted.

*Table 1420.*Trap allocation and priority

Trap	TT	Pri	Description	Class
reset	0x00	1	Power-on reset	Interrupting
data_store_error	0x2b	2	write buffer error during data store	Interrupting
instruction_access_exception	0x01	3	Error or MMU page fault during instruction fetch	Precise
privileged_instruction	0x03	4	Execution of privileged instruction in user mode	Precise
illegal_instruction	0x02	5	UNIMP or other un-implemented instruction	Precise
fp_disabled	0x04	6	FP instruction while FPU disabled	Precise
cp_disabled	0x24	6	CP instruction while Co-processor disabled	Precise
watchpoint_detected	0x0B	7	Hardware breakpoint match	Precise
window_overflow	0x05	8	SAVE into invalid window	Precise
window_underflow	0x06	8	RESTORE into invalid window	Precise
r_register_access_error	0x20	9	register file EDAC error (LEON3FT only)	Interrupting
mem_address_not_aligned	0x07	10	Memory access to un-aligned address	Precise
fp_exception	0x08	11	FPU exception	Deferred
cp_exception	0x28	11	Co-processor exception	Deferred
data_access_exception	0x09	13	Access error during data load, MMU page fault	Precise
tag_overflow	0x0A	14	Tagged arithmetic overflow	Precise
division_by_zero	0x2A	15	Divide by zero	Precise
trap_instruction	0x80 - 0xFF	16	Software trap instruction (TA)	Precise
interrupt_level_15	0x1F	17	Asynchronous interrupt 15	Interrupting
interrupt_level_14	0x1E	18	Asynchronous interrupt 14	Interrupting
interrupt_level_13	0x1D	19	Asynchronous interrupt 13	Interrupting
interrupt_level_12	0x1C	20	Asynchronous interrupt 12	Interrupting
interrupt_level_11	0x1B	21	Asynchronous interrupt 11	Interrupting
interrupt_level_10	0x1A	22	Asynchronous interrupt 10	Interrupting
interrupt_level_9	0x19	23	Asynchronous interrupt 9	Interrupting
interrupt_level_8	0x18	24	Asynchronous interrupt 8	Interrupting
interrupt_level_7	0x17	25	Asynchronous interrupt 7	Interrupting
interrupt_level_6	0x16	26	Asynchronous interrupt 6	Interrupting
interrupt_level_5	0x15	27	Asynchronous interrupt 5	Interrupting
interrupt_level_4	0x14	28	Asynchronous interrupt 4	Interrupting
interrupt_level_3	0x13	29	Asynchronous interrupt 3	Interrupting
interrupt_level_2	0x12	30	Asynchronous interrupt 2	Interrupting
interrupt_level_1	0x11	31	Asynchronous interrupt 1	Interrupting

The prioritization follows the SPARC V8 manual in the regular non-FT case. In the FT case there is a minor difference for r_register_access_error, which has lower priority than window_over/underflow because the window condition is detected before the register file is accessed on the LEON3FT.

The fp/cp_exception traps may be either deferred or precise depending on implementation, for the GRFPU and GRFPU-Lite implementations they are deferred.

The data_store_error is delivered as a deferred exception but is non-resumable and therefore classed as interrupting. Likewise, r_register_access_error is delivered as a precise trap but since it is non-resumable it is classed as an interrupting trap.

80.2.14 Single vector trapping (SVT)

Single-vector trapping (SVT) is an SPARC V8e option to reduce code size for embedded applications. When enabled, any taken trap will always jump to the reset trap handler (%tbr.tba + 0). The trap type will be indicated in %tbr.tt, and must be decoded by the shared trap handler. SVT is enabled by setting bit 13 in %asr17. The model must also be configured with the VHDL generic *svt* = 1

80.2.15 Address space identifiers (ASI)

In addition to the address, a SPARC processor also generates an 8-bit address space identifier (ASI), providing up to 256 separate, 32-bit address spaces. During normal operation, the LEON3 processor accesses instructions and data using ASI 0x8 - 0xB as defined in the SPARC manual. Using the LDA/STA instructions, alternative address spaces can be accessed. The different available ASIs are described in section 80.10.

80.2.16 Partial WRPSR

Partial write %PSR (WRPSR) is a SPARC V8e option that allows WRPSR instructions to only affect the %PSR.ET field. If the processor has been implemented with support for partial WRPSR and the WRPSR instruction's rd field is non-zero, then the WRPSR write will only update ET.

The model must be configured with the VHDL generic pwrpsr = 1 for partial WRPSR to be supported. Implementations that do not support partial WRPSR will write the full %PSR register regardless of the value of the WRPSR instruction's rd field.

80.2.17 Alternative window pointer

Alternative window pointer (AWP) is a SPARC V8e option intended to reduce interrupt latency by allowing code that manipulates the current window pointer, mainly window over and underflow handlers and context switching code, to run with traps enabled.

Two bits are added to the PSR register, AW (alternative window) and PAW (previous alternative window). Also an AWP (alternative window pointer) field is added in an ASR register.

When the AW bit is set, the current register window used for reading/writing non-global registers is taken from the AWP register field instead of the normal CWP register field, and SAVE and RESTORE operations modify the AWP field instead of the CWP. SAVE and RESTORE can do not trigger the window over/underflow traps while AW is set.

When both AW and PAW are zero, the AWP field is kept equal to the CWP field.

When a trap occurs, the value of AW is copied into the PAW field, and AW is cleared. When returning from a trap using the RETT instruction, the PAW field is copied back into AW. The RETT will not trigger the window underflow trap if PAW is set regardless of if CWP or AWP point to an invalid window.

80.2.18 Register file partitioning

Register file partitioning is an optional extension (enabled through the altwin generic) to allow a subrange of the register windows to be used as if it was the whole register file. The selected subset is connected in a ring so that the outs of the lowest register window is aliased to the ins of the highest register window in the range. Other register windows outside this range are not accessible and will be kept at their old values while the partitioning is enabled.

The partitioning is activated by setting the STWIN and CWPMAX fields of the %asr20 register. This selects the subset of windows between STWIN and STWIN+CWPMAX so that they map to CWP

values 0 to CWPMAX. STWIN and CWPMAX must be set so they map to a valid range, CWPMAX+STWIN must not exceed the highest possible CWP value supported in the normal case. Also, for correct operation, CWP must be set to a value between 0 and CWPMAX before accessing any non-global register.

Writing CWPMAX to (otherwise illegal value) 0 in %asr20 will result in writing only AWP and keeping the values of STWIN and CWPMAX.

A special write-only bit in the %asr20 register can be used to write CWP in the PSR at the same time as writing the STWIN,CWPMAX,AWP fields, this is intended to allow switching between two register file partitions without disabling interrupts.

The WIM register is not managed by the partitioning logic, therefore the lowest bits of the WIM will map to the partitioned windows. The highest bits of the WIM will be masked to 0 on read to simulate a smaller register file, however these bits are still writable.

80.2.19 Power-down

The processor can be configured to include a power-down feature to minimize power consumption during idle periods. The power-down mode is entered by performing a WRASR instruction to %asr19:

```
wr %g0, %asr19
```

During power-down, the pipeline is halted until the next interrupt occurs. Signals inside the processor pipeline and caches are then static, reducing power consumption from dynamic switching.

Note: %asr19 must always be written with the data value zero to ensure compatiblity with future extensions.

Note: This instruction must be performed in supervisor mode with interrupts enabled.

When resuming from power-down, the pipeline will be re-filled from the point of power-down and the first instruction following the WRASR instruction will be executed prior to taking the interrupt trap. Up to six instructions after the WRASR instruction will be fetched (possibly with cache miss if they are not in cache) prior to fetching the trap handler.

80.2.20 Processor reset operation

The processor is reset by asserting the RESET input for at least 4 clock cycles. The following table indicates the reset values of a subset of the registers which are affected by the reset..

*Table 1421.*Processor reset values

Register	Reset value
Trap Base Register	Trap Base Address field reset (value given by *rstaddr* VHDL generic)
PC (program counter)	0x0 (*rstaddr* VHDL generic)
nPC (next program counter)	0x4 (*rstaddr* VHDL generic + 4)
PSR (processor status register)	ET=0, S=1

By default, the execution will start from address 0. This can be overridden by setting the *rstaddr* VHDL generic in the model to a non-zero value. The reset address is always aligned on a 4 KiB boundary. If *rstaddr* is set to 16#FFFFF#, then the reset address is taken from the signal IRQI.RSTVEC. This allows the reset address to be changed dynamically.

80.2.21 Multi-processor systems

In multiprocessor systems, the ID of the processor on which the code is executing can be read out by reading the index field of the LEON3 configuration register. Only processor 0 starts executing after reset, the others are in power-down mode and are activated by a signal from the interrupt controller.

80.2.22 LEON-REX extension

The processor can be built with support for the LEON-REX addition to the SPARC instruction set, allowing a more compact code representation than the regular SPARC machine code. The details of the extension are given in a separate document. The extension is implemented when the *rex* VHDL generic is set.

Detection of whether support is present can be done by checking the REXV field in the asr17 register (see section 80.11.2). The REX support can be set to enabled, illegal or transparent mode via the REXEN/REXILL bits in the asr17 register, after reset the default setting is illegal so any LEON-REX code will cause an illegal instruction trap.

The extension is implemented as a decompressor internally inside the pipeline and does not affect the behavior of the caches, MMU or AHB bus interfaces.

When the *rex* generic is set, the instruction trace buffer entries are changed so the two most significant bits of the time tag are instead used to represent REX mode enabled status, and bit 1 of the program counter. The instructions opcodes logged into the trace buffer are the regular SPARC opcodes that are generated internally in the pipeline, not the LEON-REX opcodes that are in memory and cache.

80.3 Cache system

80.3.1 Overview

The LEON3 processor pipeline implements a Harvard architecture with separate instruction and data buses, connected to two separate cache controllers. As long as the execution does not cause a cache miss, the cache controllers can serve one 32-bit instruction fetch and one 32-bit data load/store per cycle, keeping the pipeline running at full speed. Each cache controller can be configured with different sizes and replacement policy, and it is also possible to attach local RAM to each cache controller.

On cache miss, the cache controller will assert a hold signal freezing the IU pipeline, and after delivering the data the hold signal is again lifted so execution continues. For accessing the bus, the cache controllers share the same AHB connection to the on-chip bus. Certain parts of the MMU (table walk logic, and depending on configuration also TLB buffer) are also shared between the two caches.

Another important component included in the data cache is the write buffer, allowing stores to proceed in parallel to executing instructions.

Cachability (memory areas that are cachable) for both caches is controlled either through the AHB plug&play address information or using a VHDL generic, see section 80.7.2.

80.3.2 Cache operation

Each cache controller has two main memory blocks, the tag memory and the data memory. At each address in the tag memory, a number of cache entries, ways, are stored for a certain set of possible memory addresses. The data memory stores the data for the corresponding ways.

For each way, the tag memory contains the following information:

- Valid bits saying if the entry contains valid data or is free. The I-cache has one valid bit per word (instruction) while the D-cache has a single valid bit for the whole cache line.
- The tag, all bits of the cached memory address that are not implied by the set
- If MMU is enabled, the context ID of the cache entry
- If MMU is enabled with *mmuen* generic set to 2, SO bit (supervisor only access)
- If locking support is enabled, a lock bit for that entry
- If LRR is used, a bit specifying the replacement order
- If FT is enabled, check bits for detecting errors

When a read from cache is performed, the tags and data for all cache ways of the corresponding set are read out in parallel, the tags and valid bits are compared to the desired address and the matching way is selected. In the hit case, this is all done in the same cycle to support the full execution rate of the processor.

In the miss case, the cache will at first deliver incorrect data. However on the following cycle, a hold signal will be asserted to prevent the processor from proceeding with that data. After the miss has been processed, the correct data is injected into the pipeline using a memory data strobe (mds) signal, and afterwards the hold signal can be released. If the missed address is cacheable, then the data read in from the cache miss will be stored into the cache, possibly replacing one of the existing ways.

The miss case is handled slightly differently for the I and D caches. Depending on the instruction burst fetch configuration bit, the instruction cache will either read the single missed instruction, or stream in data from the missed address until to the end of that cache line. The valid bits in the cache will reflect which words in the line were actually read in. The D-cache will always fetch a whole cache line on miss and therefore only has one valid bit.

In the instruction streaming case, the processor pipeline is stepped one step for every received instruction. If the processor needs extra pipeline cycles to stretch a multi-cycle instruction, or due to an interlock condition (see section 80.2), or if the processor jumps/branches away, then the instruction cache will hold the pipe, fetch the remainder of the cache line, and the pipeline will then proceed normally.

80.3.3 Cache configuration options

Each cache controller can be configured to implement a single-way (direct-mapped) cache or a multi-way cache with set associativity of 2 - 4. The way size is configurable to 1 - 256 KiB, divided into cache lines with 16 or 32 bytes of data.

In multi-way configurations, one of three replacement policies can be selected:

- Least-recently-used (LRU) - This maintains the order of usage for each set in the cache and replaces the one that has was used last. The LRU information needs to be updated on every cache hit and is therefore not stored with the tags but in separate flip flops.
- Least-recently-replaced (LRR) - This stores the index of the oldest replaced way along with the tags and uses this to select which way to replace. This policy can only be implemented when the number of ways is set to 2.
- Pseudo-random - This method samples a free-running counter to select which way to replace. System jitter (AMBA bus delay variations) will help to randomize the selected value.

Locking support can also be added to each cache if desired. This option adds a lock bit to each tag that allows you to lock a number of ways in each set, preventing those cache entries from being replaced. Note that when using locking together with LRU and more than two ways, this will add extra lookup tables to determine which way to replace and this might become a critical path in the core.

80.3.4 Address mapping

The addresses seen by the CPU are divided into tag, index and offset bits. The index is used to select the set in the cache, therefore only a limited number of cache lines with the same index part can be stored at one time in the cache. The tag is stored in the cache and compared upon read.

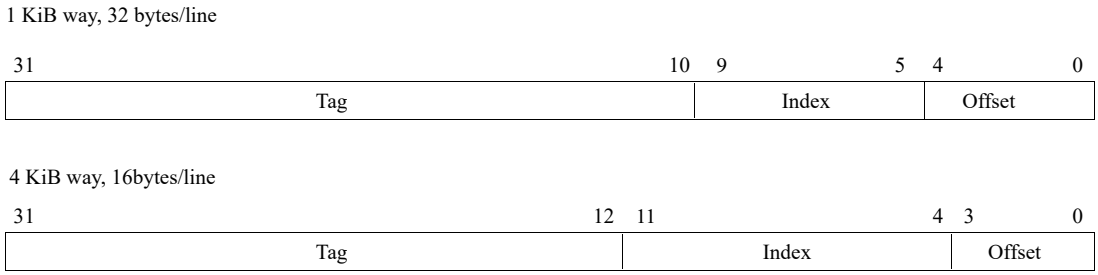


Figure 219. Cache address mapping examples

80.3.5 Data cache policy

The data cache employs a write-through policy, meaning that every store made on the CPU will propagate, via the write buffer, to the bus and there are no “dirty” lines in the cache that has not yet been written out apart from what is in the buffer. The store will also update the cache if the address is present, however a new line will not be allocated in that case

.

*Table 1422.*LEON3 Data caching behavior

Operation	In cache	Cacheable	Bus action	Cache action	Load data
Data load	No	No	Read	No change	Bus
	No	Yes	Read	Line allocated/replaced	Bus
	Yes	-	None	No change	Cache
Data load with forced cache miss (ASI 1)	No	No	Read	No change	Bus
	No	Yes	Read	Line allocated/replaced[1]	Bus
	Yes	-	Read	Data updated[1]	Bus
Data load with MMU bypass (ASI 0x1C)	-	-	Read (phys addr)	No change	Bus
Data store	No	No	Write (via buffer)	No change	(N/A)
	No	Yes	Write (via buffer)	No change	(N/A)
	Yes	-	Write (via buffer)	Data updated	(N/A)
Data store with MMU bypass (ASI 0x1C)	-	-	Write (via buffer, phys addr)	No change	(N/A)

[1] This behavior varies slightly between LEON3 versions, see section 80.13.3

80.3.6 Write buffer

The data cache contains a write buffer able to hold a single 8,16,32, or 64-bit write. For half-word or byte stores, the stored data replicated into proper byte alignment for writing to a word-addressed device. The write is processed in the background so the processor pipeline can keep executing while the write is being processed. However, any following instruction that requires bus access will block until the write buffer has been emptied. Loads served from cache will however not block, due to the cache policy used there can not be a mismatch between cache data and store buffer (the effect of this behavior on SMP systems is discussed in section 80.8).

Since the processor executes in parallel with the write buffer, a write error will not cause an exception to the store instruction. Depending on memory and cache activity, the write cycle may not occur until

several clock cycles after the store instructions has completed. If a write error occurs, the currently executing instruction will take trap 0x2b. This trap can be disabled using the DWT configuration (see section 80.11.2).

Note: a 0x2b trap handler should flush the data cache, since a write hit would update the cache while the memory would keep the old value due the write error.

80.3.7 Operating with MMU

When MMU is enabled, the virtual addresses seen by the running code no longer correspond directly to the physical addresses on the AHB bus. The cache uses tags based on the virtual addresses, as this avoids having to do any additional work to translate the address in the most timing-critical hit case. However, any time a bus access needs to be made, a translation request has to be sent to the MMU to convert the virtual address to a physical address. For the write buffer, this work is included in the background processing of the store. The translation request to the MMU may result in memory accesses from the MMU to perform table walk, depending on the state of the MMU.

The MMU context ID is included in the cache tags in order to allow switching between multiple MMU contexts mapping the same virtual address to different physical addresses. Note that the cache does not detect aliases to the same physical address so in that case the same physical address may be cached in multiple ways (also see snooping below).

80.3.8 Snooping

The data cache can be configured to support AHB bus snooping. The AHB bus the processor is connected to, is monitored for writes from other masters to an address that is in the cache. If a write is done to a cached address, that cache line is marked invalid and the processor will be forced to fetch the (new) data from memory the next time it is read.

For using snooping together with the MMU, an extra tag memory storing physical tags must be added to allow comparing with the physical address on the AHB bus (called separate snoop tags or physical tags).

The processor can snoop on itself and invalidate any other cache lines aliased to the same physical address in case there are multiple virtual mappings to the same physical address that is being written. However, note that this does not happen until the write occurs on the bus so the other virtual aliases will return the old data in the meantime. Note also that the behavior is not available in older LEON3 version.

Snooping requires the way size of the cache to be equal or smaller than the MMU page size, otherwise the index into the physical and virtual tag RAM:s may not match, resulting in aliasing problems.

80.3.9 Enabling and disabling cache

Both I and D caches are disabled after reset. They are enabled by writing to the cache control register (see 80.11.6). Before enabling the caches after a reset they must be flushed to ensure that all tags are marked invalid.

80.3.10 Cache freeze

Each cache can be in one of three modes: disabled, enabled and frozen. If disabled, no cache operation is performed and load and store requests are passed directly to the memory controller. If enabled, the cache operates as described above. In the frozen state, the cache is accessed and kept in sync with the main memory as if it was enabled, but no new lines are allocated on read misses.

If the DF or IF bit is set, the corresponding cache will be frozen when an asynchronous interrupt is taken. This can be beneficial in real-time system to allow a more accurate calculation of worst-case execution time for a code segment. The execution of the interrupt handler will not evict any cache lines and when control is returned to the interrupted task, the cache state is identical to what it was

before the interrupt. If a cache has been frozen by an interrupt, it can only be enabled again by enabling it in the CCR. This is typically done at the end of the interrupt handler before control is returned to the interrupted task.

80.3.11 Flushing

Both instruction and data cache are flushed either by executing the FLUSH instruction, setting the FI/FD bits in the cache control register, or by writing to certain ASI address spaces.

Cache flushing takes one clock cycle per cache set, during which the IU will not be halted, but during which the caches are disabled. When the flush operation is completed, the cache will resume the state (disabled, enabled or frozen) indicated in the cache control register. Diagnostic access to the cache is not possible during a flush operation and will cause a data exception (trap=0x09) if attempted.

Note that while the SPARC V8 specifies only that the instructions pointed to by the FLUSH argument will be flushed, the LEON3 will additionally flush the entire I and D cache (which is permitted by the manual as the additional flushing only affects performance and not operation). While the LEON3 currently ignores the address argument, it is recommended for future compatibility to only use the basic flush %g0 form if you want the full flush behavior.

80.3.12 Locking

In a multi-way configuration the instruction and data cache controllers can be configured with optional lock bit in the cache tag. Setting the lock bit prevents the cache line to be replaced by the replacement algorithm. A cache line is locked by performing a diagnostic write to the instruction tag (ASI 0xC, see 80.10.5) on the cache offset of the line to be locked, setting the Address Tag field to the address tag of the line to be locked, enabling the lock bit and clearing the valid bits. The locked cache line will be updated on a read-miss and will remain in the cache until the line is unlocked.

For correct operation, the ways must always be locked in ascending order, for example if two ways are locked it must always be way 0 and 1. Note also that you must always keep one way unlocked in each set for the cache to function correctly in case of miss to that set.

For run-time detection of this feature, setting the lock bit in a cache tag and reading the same tag will show if the cache line locking was enabled during the LEON3 configuration: the lock bit will be set if the cache line locking was enabled otherwise it will be 0.

80.3.13 Diagnostic access

The cache tag and data contents can be directly accessed for diagnostics and for locking purposes via various ASI:s, see section 80.10.5.

80.3.14 Local scratch pad RAM

Local instruction and data ram can optionally be attached to the cache controllers. The ram can be between 1 - 256 KiB, and mapped on any 16 MiB block in the address space. Accesses performed to the local RAMs are not cached, and will not appear on the AHB bus or in the write buffer. The default address for the instruction ram is 0x8e000000, and for the data ram 0x8f000000, but these can be reconfigured using VHDL generics.

The local instruction RAM is intended for executing instructions and will serve instructions without any wait states. It can be accessed (with a few wait states) through 32-bit load and store instructions only, and is therefore not suitable for general application data. Initializing the instruction local RAM is done from software via stores as that is the only way to write into it.

The local data RAM will serve data accesses of any size without adding wait states. It can however not serve instructions.

The local instruction/data RAM implementation is not compatible with the MMU functionality, as it will “shadow” the virtual address space regardless of page table setup.

Since the local RAM implementation does not support error protection, it is not applicable for FT configurations of the LEON3.

80.3.15 Fault tolerance support

The cache memories (tags and data) can optionally be protected against soft errors using byte-parity-codes. Enabling of the data protection is done through the *cmft* VHDL generic and the functionality is only enabled for users that have licensed the fault-tolerant version of LEON3. Cache memory data protection is further described in section 80.9.5.

80.4 Memory management unit

80.4.1 Overview

A memory-management unit can optionally be enabled. This is compatible with the SPARC V8 reference MMU (SRMMU) architecture described inthe SPARC V8 manual, appendix H.

The MMU provides address translation of both instructions and data via page tables stored in memory.When needed, the MMU will automatically access the page tables to calculate the correct physical address. The latest translations are stored in a special cache called the translation lookaside buffer (TLB), also referred to as Page Descriptor Cache (PDC) in the SRMMU specification. The MMU also provides access control, making it possible to “sandbox” unpriviledged code from accessing the rest of the system.

80.4.2 MMU/Cache operation

When the MMU is disabled, the MMU is bypassed and the caches operate with physical address mapping. When the MMU is enabled, the cache tags store the virtual address and also include an 8-bit context field. Both the tag address and context field must match to generate a cache hit. When *mmuen* generic is set to 2 and MMU is enabled, the cache tags store a bit in addition to context called SO bit (supervisor only access). The SO bit is used to check the access permission of the data and instructions that resides in the level-1 caches when MMU is enabled. Without SO bit, access permissions of the load operations that hit in the data cache or the instruction accesses that hit in the instruction cache will not be checked properly.

If cache snooping is used, physical tags (separate snoop tags) must be enabled for it to work when address translation is used, see section 80.3.8.

Because the cache is virtually tagged, no extra clock cycles are needed in case of a cache load or instruction cache hit. In case of miss or write buffer processing, a translation is required that might add extra latency to the processing time, depending on TLB configuration and if there is a TLB miss.

The TLB can be configured in three different ways:

- Separate TLBs, slow access. TLB lookup adds 2 extra clock cycles.
- Shared TLB, slow access. TLB lookup adds 2 extra clock cycles, the TLB may be used by the other cache, leading to up to 4 extra cycles lookup time in the worst case.
- Separate TLBs, fast access. TLB lookup is done at the same time as tag lookup and therefore add no extra clock cycles.

If there is a TLB miss the page table must be traversed, resulting in up to four AMBA read accesses and one possible writeback operation. See the SRMMU specification for the exact format of the page table.

An MMU page fault will generate trap 0x09 for the D-cache and trap 0x01 for the I cache, and update the MMU status registers according to table 1423 and the SRMMU specification. In case of multiple

errors, they fault type values are prioritized as the SRMMU specification requires. The cache and memory will not be modified on an MMU page fault.

*Table 1423.*LEON3 MMU Fault Status Register, fault type values

Fault type	SPARC V8 ref	Priority	Condition
6	Internal error	1	Never issued by LEON SRMMU
4	Translation error	2	AHB error response while performing table walk. Translations errors as defined in SPARC V8 manual. A translation error caused by an AMBA ERROR response will overwrite all other errors. Other translation errors do no overwrite existing translation errors when FAV = 1.
1	Invalid address error	3	Page table entry for address was marked invalid
3	Privlege violation error	4	Access denied based on page table and su status (see SRMMU spec for how privilege and protection error are prioritized)
2	Protection error	5	
0	None	-	No error (inside trap this means the trap occurred when fetching the actual data)

80.4.3 Translation look-aside buffer (TLB)

The MMU can be configured to use a shared TLB, or separate TLB for instructions and data. The number of TLB entries (for each implemented TLB) can be set to 2 - 64 via VHDL generics. The organisation of the TLB and number of entries is not visible to the software and does thus not require any modification to the operating system. The TLB can be flushed using an STA instruction to ASI 0x18, see section 80.10.7.

80.4.4 Variable minimum page sizes

The standard minimum page size for the SRMMU is 4 KiB. The minimum page size can also be configured to 8, 16 or 32 KiB in order to allow for large data cache ways. The page size can either be configured hard at implementation time or made software-configurable via the MMU control register. The page sizes for level 1, 2 and 3 is seen in the table below:

*Table 1424.*MMU page size

Scheme	Level-1	Level-2	Level-3
4 KiB (default)	16 MiB	256 KiB	4 KiB
8 KiB	32 MiB	512 KiB	8 KiB
16 KiB	64 MiB	1 MiB	16 KiB
32 KiB	256 MiB	2 MiB	32 KiB

The layouts of the indexes are chosen so that PTE page tables can be joined together inside one MMU page without leaving holes.

Note that most operating systems are hard-coded for a specific page size and using one other than 4 KiB usually requires reconfiguration/recompilation of the operating system kernel.

80.5 Floating-point unit

The SPARC V8 architecture defines two (optional) co-processors: one floating-point unit (FPU) and one user-defined co-processor. Two different FPU's can be interfaced the LEON3 pipeline: Cobham Gaisler's GRFPU and GRFPU-Lite. Selection of which FPU to use is done through the fpu generic. The characteristics of the FPU's are described in the next sections.

80.5.1 Cobham Gaisler's floating-point unit (GRFPU)

The high-performance GRFPU operates on single- and double-precision operands, and implements all SPARC V8 FPU operations including square root and division. The FPU is interfaced to the LEON3 pipeline using a LEON3-specific FPU controller (GRFPC) that allows FPU instructions to be executed simultaneously with integer instructions. Only in case of a data or resource dependency is the integer pipeline held. The GRFPU is fully pipelined and allows the start of one instruction each clock cycle, with the exception is FDIV and FSQRT which can only be executed one at a time. The FDIV and FSQRT are however executed in a separate divide unit and do not block the FPU from performing all other operations in parallel.

All instructions except FDIV and FSQRT has a latency of three cycles, but to improve timing, the LEON3 FPU controller inserts an extra pipeline stage in the result forwarding path. This results in a latency of four clock cycles at instruction level. The table below shows the GRFPU instruction timing when used together with GRFPC:

*Table 1425.*GRFPU instruction timing with GRFPC

Instruction	Throughput	Latency
FADDS, FADDD, FSUBS, FSUBD,FMULS, FMULD, FSMULD, FITOS, FITOD, FSTOI, FDTOI, FSTOD, FDTOS, FCMPS, FCMPD, FCMPES. FCMPED	1	4
FDIVS	14	16
FDIVD	15	17
FSQRTS	22	24
FSQRTD	23	25

The GRFPC controller implements the SPARC deferred trap model, and the FPU trap queue (FQ) can contain up to 7 queued instructions when an FPU exception is taken. When the GRFPU is enabled in the model, the version field in %fsr has the value of 2.

The GRFPU does not handle denormalized numbers as inputs and will in that case cause an fp_exception with the FPU trap type set to unfinised_FPOP (tt=2). There is a non-standard mode in the FPU that will instead replace the denormalized inputs with zero and thus never create this condition.

80.5.2 GRFPU-Lite

GRFPU-Lite is a smaller version of GRFPU, suitable for FPGA implementations with limited logic resources. The GRFPU-Lite is not pipelined and executes thus only one instruction at a time. To improve performance, the FPU controller (GRLFPC) allows GRFPU-Lite to execute in parallel with the processor pipeline as long as no new FPU instructions are pending. Below is a table of worst-case throughput of the GRFPU-Lite:

*Table 1426.*GRFPU-Lite worst-case instruction timing with GRLFPC

Instruction	Throughput	Latency
FADDS, FADDD, FSUBS, FSUBD,FMULS, FMULD, FSMULD, FITOS, FITOD, FSTOI, FDTOI, FSTOD, FDTOS, FCMPS, FCMPD, FCMPES. FCMPED	8	8
FDIVS	31	31
FDIVD	57	57
FSQRTS	46	46
FSQRTD	65	65

The GRLFPC controller implements the SPARC deferred trap model, but the FPU trap queue (FQ) can contain only one queued instructions when an FPU exception is taken.When the GRFPU-Lite is enabled in the model, the version field in %fsr has the value of 3.

80.6 Co-processor interface

No implementation for the user-defined co-processor is currently provided.

80.7 AMBA interface

80.7.1 Overview

The LEON3 processor uses one AHB master interface for all data, instruction and MMU table-walk accesses. Instructions are fetched with incremental bursts if the IB bit is set in the cache control register, otherwise single READ cycles are used. Read data is accessed using bursts for cachable data, and byte, half-word and word accesses for uncacheable data. Store data is performed using single accesses or a two-beat incremental burst in case of 64-bit store.

The HPROT signals of the AHB bus are driven to indicate if the accesses is instruction or data, and if it is a user or supervisor access.

*Table 1427.*HPROT values

Type of access	User/Super	HPROT
Instruction	User	1100
Instruction	Super	1110
Data	User	1101
Data	Super	1111
MMU	Any	1101

In case of atomic accesses, a locked access will be made on the AMBA bus to guarantee atomicity as seen from other masters on the bus.

80.7.2 Cachability control

Cachability for both caches can be controlled through the AHB plug&play address information or set manually via the *cached* VHDL generic.

For plug'n'play based cachability, the memory mapping for each AHB slave indicates whether the area is cachable, and this information is used to (statically) determine which access will be treated as cacheable. This approach means that the cachability mapping is always coherent with the current AHB configuration.

When the *cached* VHDL generic is not zero, it is treated as a 16-bit field, defining the cachability of each 256 MiB address block on the AMBA bus. For example, a value of 16#00F3# will define cachable areas in 0 - 0x20000000 and 0x40000000 - 0x80000000.

In order to access the plug'n'play information, the processor takes the ahbso vector as input. Only the static hconfig signals are used so the use of this input will be eliminated through constant propagation during synthesis.

80.7.3 Error handling

An AHB ERROR response received while fetching instructions will normally cause an instruction access exception (tt=0x1). However if this occurs during streaming on an address which is not needed, the I cache controller will just not set the corresponding valid bit in the cache tag. If the IU later fetches an instruction from the failed address, a cache miss will occur, triggering a new access to the failed address.

An AHB ERROR response while fetching data into the data cache will normally trigger a data_access_exception trap (tt=0x9). If the error was for a part of the cache line other than what was currently being requested by the pipeline, a trap is not generated and the valid bit for that line is not set.

An ERROR response during an MMU table walk will lead the MMU to set the fault type to Internal error (1) and generate an instruction or data access exception, depending on which type of access that caused the table walk.

Error responses to writes will result in the data_store_error trap as described in section 80.3.6.

80.7.4 Snoop port

For the snooping logic, the LEON3 has an ahbsi input. For correct function, this must be tied to the same AHB bus that the master interface. It is not possible to snoop on another bus or to add extra pipeline registers to the snoop port, because the snoop logic must be in sync with the master interface.

80.8 Multi-processor system support

This section gives an overview of issues when using the LEON3 in multi-processor configuration.

Using the features described in earlier sections together with a multiprocessor capable IRQ controller (IRQMP), the LEON3 processor can support symmetric multiprocessing (SMP) configurations with shared memory, with up to 16 processors attached to the same AHB bus.

Enabling SMP features (sleeping on reset for CPU 1-N) is done by setting the *smp* VHDL generic to 1 or higher. Cache snooping should always be enabled in SMP systems to maintain data cache coherency between the processors.

80.8.1 Start-up

In multiprocessor systems, only the first processor will start after reset and all other processors will remain halted in power-down mode. After the system has been initialized, the remaining processors can be started by writing to the 'multiprocessor status register', located in the multiprocessor interrupt controller. The halted processors start executing from the reset address (0 or *rstaddr* VHDL generic, see section 80.2.20).

An application in a multiprocessor system can determine which processor it is executing on by checking the processor index field in the LEON3 configuration register (%asr17). As all processors typically have the same reset start address value, boot software must check the processor index and perform processor specific setup (e.g. initialization of stack pointer) based on the value of the processor index.

In recent versions of the LEON3, and if the IRQ controller is configured with the extended boot register extension, it is possible for one processor to monitor and reboot another processor.via the interrupt controller. This requires careful software design.

For earlier versions of the LEON3, this is not supported and if software detects that one processor is unresponsive and needs to restart the processor then the full system should be reset, for example by triggering the system's watchdog, if implemented. In order for software to monitor that all processors in a system are up and running it is recommended to implement a heartbeat mechanism in software.

While it is possible to have more fine-grained control over processor behaviour via the Debug Support Unit (if implemented) this is not recommended as the debug support unit is typically disabled in production mode.

80.8.2 Shared memory model

Each processor core has it's own separate AHB master interface and the AHB controller will arbitrate between them to share access to the on-chip bus.

If caches are not used, the processors will form a sequentially consistent (SC) system, where every processor will execute it's loads, stores and atomics to memory in program order on the AHB bus and the different processors operations will be interleaved in some order through the AHB arbitration. The

shared memory controller AHB slave is assumed to not reorder accesses so a read always returns the latest written value to that location on the bus.

When using caches with snooping (and with physical tags, also called separate snoop tags, if using the MMU), the shared memory will act according to the slightly weaker SPARC Total Store Order (TSO) model. The TSO model is close to SC, except that loads may be reordered before stores coming from the same CPU. The stores and atomics are conceptually placed in a FIFO (see the diagrams in the SPARC manual) and the loads are allowed to bypass the FIFO if they are not to the same address as the stores. Loaded data from other addresses may therefore be either older or newer, with respect to the global memory order, than the stores that have been performed by the same CPU.

In the LEON3 case this happens because cache hits are served without blocking even when there is data in the write buffer. The loaded data will always return the stored data in case of reading the same address, because if it is cached, the store updates the cache before being put in the write buffer, and if it was not in cache then the load will result in a miss which waits for the write buffer to complete. Loaded data from a different address can be older than the store if it is served by cache before the write has completed, or newer if it results in a cache miss or if there is a long enough delay for the store to propagate to memory before reading.

See relevant literature on shared memory systems for more information. These details are mainly of concern for complex applications using lock-free data structures such as the Linux kernel, the recommendation for applications is to instead avoid concurrent access to shared structures by using mutexes/semaphores based on atomic instructions, or to use message passing schemes with one-directional circular buffers.

80.8.3 Memory-mapped hardware

Hardware resources (IP cores) are normally memory mapped on uncacheable address spaces. They will be accessible from all the CPU:s in a sequentially consistent manner. Since software drivers usually expect to be “alone” accessing the IP core and the IP cores register interfaces are not designed for concurrent use by multiple masters, using a bare-C application designed for single-processor usage on multiple cores at the same time will generally not work. This can be solved by partitioning the applications so that each IP core is only accessed by one of the CPU:s. This partitioning also need to be done between the interrupts so the IP core’s interrupts will be received by the correct processor.

80.9 Fault tolerance

80.9.1 Overview

The LEON3 processor can be enhanced with fault-tolerance against SEU errors (referred to as LEON3FT). The fault-tolerance is focused on the protection of on-chip RAM blocks, which are used to implement IU/FPU register files and the cache memory.

The LEON3FT is licensed separately, and in the commercial LEON3 releases setting the FT VHDL generics will not have any effect.

80.9.2 Integer register file protection

The SEU protection for the integer unit register file can be implemented in four different ways, depending on target technology and available RAM blocks. The SEU protection scheme is selected

during synthesis, using the *iuft* VHDL generic. Table 1428 below shows the implementation characteristics of the four possible SEU protection schemes.

*Table 1428.*Integer unit SEU protection schemes

ID	Implementation	Description	Usage
0	No protection (hardening at lower level)	No error checking, equivalent to non-FT version. Register file hardness must be ensured separately, for example by mapping the register file memories to SEU hardened flip-flops.	IU, GRFPU, GRFPU-Lite
1	4-bit parity with restart	4-bit checksum per 32-bit word. Detects and corrects 1 bit per byte (4 bits per word). Pipeline restart on correction.	IU, GRFPU-Lite
2	8-bit parity without restart	8-bit checksum per 32-bit word. Detects and corrects 1 bit per byte (4 bits per word). Correction on-the-fly without pipeline restart.	IU, GRFPU
3	7-bit BCH with restart	7-bit BCH checksum per 32-bit word. Detects 2 bits and corrects 1 bit per word. Pipeline restart on correction.	IU
4	Memory triplication	Memory blocks triplicated and bit by bit voted on outputs. Correction on-the-fly without pipeline restart, no error injection interface or error counters. Note that care must be taken by the implementer to ensure that the TMR is not collapsed in optimization by synthesis tools.	IU, GRFPU, GRFPU-Lite
5	7-bit BCH without restart	7-bit BCH checksum per 32-bit word. Correction on the fly without pipeline restart. Error correction logic performed on same cycle as memory read.	IU
6	Technology specific	Implement register files using native ECC capability of the technology (via syncram_2pft in the techmap library). Only valid for subset of (FPGA) technologies. Correction on-the-fly without pipeline restart. Error injection and error counters may be supported depending on technology.	IU

The SEU error detection has no impact on behavior, but a correction cycle (scheme 1 and 3) will delay the current instruction with 6 clock cycles. An uncorrectable error in the IU register file will cause trap 0x20 (*r_register_access_error*). A dedicated counter exists in ASR16 to count the number of register file corrections.

The register file is implemented using scheme 0 if the regfile_3p_infer array is set for the selected memory technology in the techmap library, or if bits 16-17 of memtech are set, regardless of iuft/fpft setting.

80.9.3 Floating-point register file protection

The FPU register file has similar SEU protection as the IU register file, but with less configuration options. The FPU register file protection scheme is enabled with the fpft generic and has the same encoding as iuft. The protection schemes that are supported for the GRFPU and the GRFPU-Lite are listed in table 1428. An uncorrectable error in the FPU register file will cause an (deferred) FPU exception with %fsr.ftt set to 5 (hardware_error).

Note that the restrictions on protection scheme is not enforced, so it is recommended to simulate the configuration with error injection to ensure that the scheme chosen is functioning correctly. It is also recommended to confirm in the netlist that the expected register file type (memory block or flip flops) was implemented.

80.9.4 Register file EDAC/parity bits diagnostic read-out and error injection

The register file parity bits can be read out via ASI 0xF as described in section 80.10.6.

For test purposes, the IU and FPU register file EDAC/parity checkbits can be modified by software. This is done by setting the ITE or FTE bits in asr16 to '1'. In this mode, the EDAC/parity bits are first XORed with the contents of %asr16.FTB before written to the register files. This is done for all writes into the register file while the feature is enabled, so diagnostic code must be carefully designed to avoid accidentally injecting errors in other registers than intended. Also note that due to result forwarding in the pipeline, an injected error will not affect the immediately following instructions, which might cause surprising behavior such as errors triggering only when single stepping through the code.

Bit 0 (RF EDAC disable) in %asr16 should be set to 1 during diagnostic accesses and fault injection to the register file, to avoid EDAC correction cycles or error traps.

80.9.5 Cache protection

Each word in the tag or data memories is normally protected by four check bits. Use of the SYNCRAM protection allows the processor to use technology specific protection and this can lead to savings in resource utilization on target technologies that have built-in protection of SRAM blocks. If separate physical tags for snooping are enabled, the physical tag memory is also protected. An error during cache access will cause an invalidation of that cache line, and a re-execution of the failing instruction. This will ensure that the complete cache line (tags and data) is refilled from external memory.

If snooping is enabled, an error detected in the tags while snooping a write to that set will lead to that cache data being invalidated (since the tag before the error might have matched the written address).

For every detected error, a counter in the cache control register is incremented. The counters saturate at their maximum value (3), and should be reset by software after read-out.

The cache memory check bits can be diagnostically read and modified by setting the PS bit in the cache control register and then perform a normal tag or data diagnostic access, see section 80.10.5 for details.

80.10 ASI assignments

80.10.1 Summary

The table shows the ASI usage for LEON.

*Table 1429.*ASI usage

ASI	Usage
0x01	Forced cache miss.
0x02	System control registers (cache control register)
0x08, 0x09	Not supported
0x0A	Access level is determined by 'S' bit in %psr when MMU is enabled and *mmuen* generic is set to 1 User Access when MMU is enabled and *mmuen* generic is set to 2 Sets HPROT to user data regardless of MMU
0x0B	Access level is determined by 'S' bit in %psr when MMU is enabled and *mmuen* generic is set to 1 Supervisor Access when MMU is enabled and *mmuen* generic is set to 2, otherwise normal cache access Sets HPROT to supervisor data regardless of MMU
0x0C	Instruction cache tags
0x0D	Instruction cache data
0x0E	Data cache tags
0x0F	Data cache data
0x0F	Register file diagnostic parity read-out (FT only)
0x10	Flush instruction cache (and also data cache when system is implemented with MMU)
0x11	Flush data cache
0x13	MMU only: Flush instruction and data cache
0x14	MMU only: MMU diagnostic D context cache access (deprecated, do not use)
0x15	MMU only: MMU diagnostic I cache context access (deprecated, do not use)
0x18, 0x03	MMU only: Flush TLB and I/D cache
0x19, 0x04	MMU only: MMU registers
0x1C	MMU and cache bypass
0x1D	MMU only: MMU diagnostic access (deprecated, do not use)
0x1E	MMU only: MMU snoop tags diagnostic access

80.10.2 ASI 0x1, Forced cache miss

ASI 1 is used for systems without cache coherency, to load data that may have changed in the background, for example by DMA units. It can also be used for other reasons, for example diagnostic purposes, to force a AHB load from memory regardless of cache state.

The address mapping of this ASI is matched with the regular address space, and if MMU is enabled then the address will be translated normally. Stores to this ASI will perform the same way as ordinary data stores.

For situations where you want to guarantee that the cache is not modified by the access, the MMU and cache bypass ASI, 0x1C, can be used instead.

80.10.3 ASI 0x2, System control registers

ASI 2 contains a few control registers that have not been assigned as ancillary state registers. These should only be read and written using 32-bit LDA/STA instructions.

All cache registers are accessed through load/store operations to the alternate address space (LDA/STA), using ASI = 2. The table below shows the register addresses:

*Table 1430.*ASI 2 (system registers) address map

Address	Register
0x00	Cache control register
0x04	Reserved
0x08	Instruction cache configuration register
0x0C	Data cache configuration register

80.10.4 ASI 0x8-0xB, Data/Instruction

These ASIs are assigned by the SPARC manual for normal data and instruction fetches.

Accessing the instruction ASIs (0x8,0x9) explicitly via LDA/STA instructions is not supported in the LEON3 implementation.

Using LDA/STA with the user/supervisor data ASI (0xA,0xB) will behave as the affect the HPROT signal emitted by the processor according to section 80.7.1. If *mmuen* generic is set to 2, MMU access control will be done according to the indicated user or supervisor ASI inline with reference MMU description in Sparc V8 manual. If *mmuen* generic is set to 1, MMU access control will be done depending on the SU bit in the %psr register.

80.10.5 ASI 0xC-0xF, ICache tags/data, DCache tags/data

Note that on LEON3FT, ASI 0xF is double mapped and the description in this section is valid only if the RFT bit is not set.

ASI 0xC-0xF provide diagnostic access to the instruction cache memories. These ASIs should only be accessed by 32-bit LDA/STA instructions. These ASIs can not be used while a cache flush is in progress.

The same address bits used normally as index are used to index the cache also in the diagnostic access. For a multi-way cache, the lowest bits above the index part, the lowest bits that would normally be used as tag, are used to select which way to read/write. The remaining address bits are don't cares, leading the address map to wrap around.

If fault tolerance is enabled, the tag parity, context and SO bits can also be read out through these ASIs by setting the PS bit in the cache configuration register. When this bit is set, the parity data is read instead of the ordinary data. When writing the tag bits, the context bits will always be written with the current context in the MMU control register. The SO bit in the tag will be written with the SO bit value in the MMU control register (SO bit in MMU control register only exists in the tag when *mmuen* generic is set to 2). The parity to be written is calculated based on the supply write-value, the context ID and optionally SO bit (if mmuen is set to 2) in the MMU control register. The parity bits can be modified via the TB field in the cache control register.

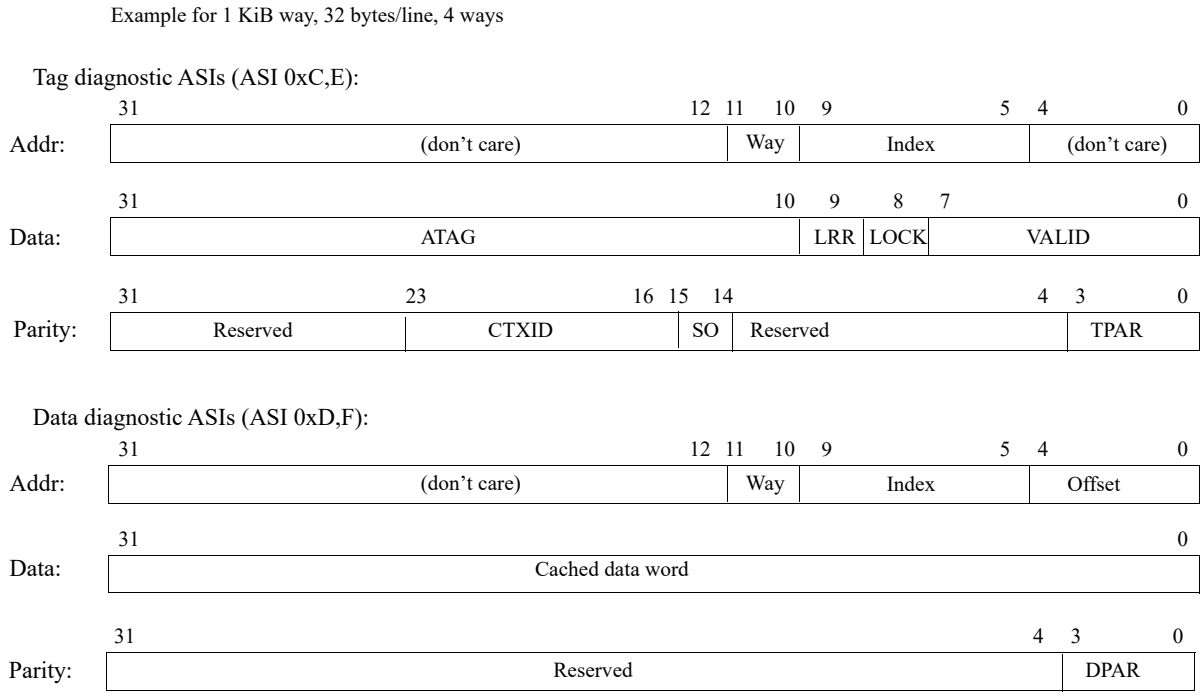


Figure 220. ASI 0xC-0xF address mapping and data layout

Field Definitions:

Address Tag (ATAG) - Contains the tag address of the cache line.

LRR - Used by LRR algorithm to store replacement history, otherwise 0.

LOCK - Locks a cache line when set. 0 if cache locking not implemented.

Valid (V) - When set, the corresponding 32-bit sub-block of the cache line contains valid data. V[0] corresponds to address 0 in the cache line, V[1] to address 1, V[2] to address 2 and so on. The D-Cache only has one valid bit per cache line which is replicated for the whole 8-bit diagnostic field.

CTXID - Context ID, used when MMU is enabled

SO - (Supervisor only access) It is used when MMU is enabled and *mmuen* (see Sec. 80.16) generic is set to 2. This bit is set to 1 when the associated page with the tag has access permission of 6 or 7 (supervisor access only) for other access permissions it is set to 0. (For detailed information about access permissions refer to the reference MMU part of the Sparc V8 manual)

TPAR - Byte-wise parity of tag bits, context ID parity is XOR:ed into bit 3.

DPAR - Byte-wise parity of data bits

NOTE: only the necessary bits will be implemented in the cache tag, depending on the cache configuration. As an example, a 4 KiB cache with 16 bytes per line would only have four valid bits and 20 tag bits. The cache rams are sized automatically by the RAM generators in GRLIB.

80.10.6 ASI 0xF (alternate), FT register file parity read-out

In the FT version, an alternate function to ASI 0xF is selected by enabling the RFT bit in the cache control register. When enabled, this will override (shadow) the D-Cache data ASI function.

This ASI allows you to read out parity bits for the register file. The parity should be read out using a half-word LDUHA instruction. The parity bits are read out simultaneously for the two read ports. This is read only, for write access (fault injection) see section 80.9.4.

The ASI is not address-mapped, instead the registers used in the LDUHA instruction directly select which register's parity bits are returned. For example the instruction:

```
lduha   [%l0 + %l1] 0x0F, %g1
```

will read out the parity bit of %l0 on port 2 and %l1 on port 1, and store those values in register %g1.

The layout is shown in the figure below:

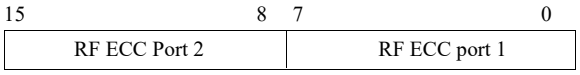


Figure 221. Register file ECC read-out layout

When the checkbits are read out using LDUHA, bit 29 (RFT) in the cache control register should be set to 1. The desired register should be used as address.

80.10.7 ASI 0x10, 0x11, 0x13, 0x18 - Flush

For historical reasons there are multiple ASIs that flush the cache in different ways.

Writing to ASI 0x10 will flush the entire instruction cache. If MMU is implemented in the core, both instruction and data cache will be flushed.

Writing to ASI 0x11 will flush the data cache only.

Writing to ASI 0x13 will flush the data cache and the instruction cache, only available when MMU is implemented.

Writing to ASI 0x18 (and 0x03), which is available only if MMU is implemented, will flush both the MMU TLB, the I-cache, and the D-cache. This will block execution for a few cycles while the TLB is flushed and then continue asynchronously with the cache flushes continuing in the background.

80.10.8 ASI 0x19 and 0x04 - MMU registers

This ASI provides access to the MMU:s control and status registers. The following MMU registers are implemented:

*Table 1431.*MMU registers (ASI = 0x19)

Address	Register
0x000	MMU control register
0x100	Context pointer register
0x200	Context register
0x300	Fault status register
0x400	Fault address register

80.10.9 ASI 0x1C - MMU and cache bypass

Performing an access via ASI 0x1C will act as if MMU and cache were disabled. The address will not be translated and the cache will not be used or updated by the access.

80.10.10ASI 0x1E - MMU snoop/physical tags diagnostic access

If the MMU has been configured to use separate snoop (physical) tags, they can be accessed via ASI 0x1E. This is primarily useful for RAM testing, and should not be performed during normal operation. This ASI is addressed the same way as the regular diagnostic ASI:s 0xC, 0xE, and the read/written data has the layout as shown below (example for a 1 KiB/way data cache):

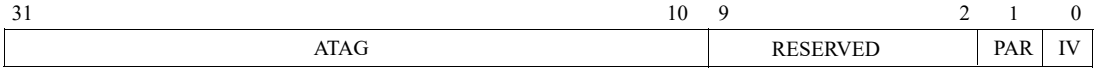


Figure 222. Snoop cache tag layout

[31:10] Address tag. The physical address tag of the cache line.
[1]: Parity. The odd parity over the data tag. LEON3FT only.
[0]: Invalid. When set, the cache line is not valid and will cause a cache miss if accessed by the processor. Only present if fast snooping is enabled.

80.11 Configuration registers

80.11.1 PSR, WIM, TBR registers

The %psr, %wim, %tbr registers are implemented as required by the SPARC V8 manual.

*Table 1432.*LEON3 Processor state register (%psr)

31 28	27 24	23 20	19 16
IMPL	VER	ICC	RESERVED
0xF	0x3	0	0
r	r	r	r

15	14	13	12	11 8	7	6	5	4 0
AW	PAW	EC	EF	PIL	S	PS	ET	CWP
0	0	0	0	0	1	1	0	0
rw'	rw*	r	rw*	rw	rw	rw	rw	rw

31:28 Implementation ID (IMPL), read-only hardwired to “1111” (15)
27:24 Implementation version (VER), read-only hardwired to “0011” (3) for LEON3.
23:20 Integer condition codes (ICC), see sparcv8 for details
19:16 Reserved
15 Alternative window pointer select (AW), read-only if AWP not implemented
14 Previous alternative window pointer select (PAW), read-only if AWP not implemented
13 Enable coprocessor (EC), read-only if coprocessor not implemented
12 Enable floating-point (EF), read-only if FPU not implemented.
11:8 Processor interrupt level (PIL) - controls the lowest IRQ number that can generate a trap
7 Supervisor (S)
6 Previous supervisor (PS), see sparcv8 for details
5 Enable traps (ET)
4:0 Current window pointer

*Table 1433.*LEON3 Window invalid mask (%wim)

31 NWIN	NWIN-1 0
RESERVED	WIM
0	NR
r	rw

*Table 1434.*LEON3 Trap base address register (%tbr)

31 12	11 4	3 0
TBA	TT	R
*	0	0
rw	r	r

31:12 Trap base address (TBA) - Top 20 bits used for trap table address

11:4 Trap type (TT) - Last taken trap type. Read only.

3:0 Always zero, read only

80.11.2 ASR17, LEON3 configuration register

The ancillary state register 17 (%asr17) provides information on how various configuration options were set during synthesis. This can be used to enhance the performance of software, or to support enumeration in multi-processor systems. There are also a few bits that are writable to configure certain aspects of the processor.

*Table 1435.*LEON3 configuration register (%asr17)

31 28	27	26	25	24 23	22 21	20 18	17	16
INDEX	DBP	NOTAG	DBPM	REXV	REXM	RESERVED	CS	CF[1]
*	0	1	1	*	*		*	*
r	rw*	r	rw*	r	rw*	r	r	r

15	14	13	12	11 10	9	8	7 5	4 0
CF[0]	DW	SV	LD	FPU	M	V8	NWP	NWIN
*	0	0	*	*	*	*	*	*
r	rw	rw*	r	r	r	r	r	r

31:28 Processor index (INDEX) - In multi-processor systems, each LEON core gets a unique index to support enumeration. The value in this field is identical to the *hindex* VHDL generic parameter in the VHDL model.

27 Disable Branch Prediction (DBP) - Disables branch prediction when set to '1'. Field is only available if the VHDL generic *bp* is set to the value 2.

26 Tagged arithmetic (NOTAG) - If this read-only field is '1' then the processor supports tagged arithmetic and the compare-and-swap (CASA) instruction. The current version if the LEON3 always supports tagged arithmetic and CASA.

25 Disable Branch Prediction on instruction cache misses (DBPM) - When set to '1' this avoids instruction cache fetches (and possible MMU table walk) for predicted instructions that may be annulled. This feature is on by default (reset value '1'), if branch prediction is programmable then this is also programmable.

24:23 REX version (REXV) - read-only field that is set to '00' if REX is not implemented, '01' if REX is implemented, '10' and '11' values are reserved for future implementations

22:21 REX mode (REXM) - set to '00' for REX enabled, '01' for REX illegal and '10' for REX transparent mode. Writable with reset value '01' when REX support has been enabled

20:18 Reserved for future implementations

17 Clock switching enabled (CS). If set, switching between AHB and CPU frequency is available.

16:15 CPU clock frequency (CF). CPU core runs at (CF+1) times AHB frequency.

14 Disable write error trap (DWT). When set, a write error trap (tt = 0x2b) will be ignored. Set to zero after reset.

13 Single-vector trapping (SVT) enable. If set, will enable single-vector trapping. Fixed to zero if SVT is not implemented. Set to zero after reset.

12 Load delay (LDDEL) - If set, the pipeline uses a 2-cycle load delay. Otherwise, a 1-cycle load delay i s used. Generated from the *lddel* VHDL generic parameter in the VHDL model.

11:10 FPU option. "00" = no FPU; "01" = GRFPU; "10" = Meiko FPU, "11" = GRFPU-Lite

9 If set, the optional multiply-accumulate (MAC) instruction is available

8 If set, the SPARC V8 multiply and divide instructions are available

7:5 Number of implemented watchpoints (NWP) (0 - 4)

4:0 Number of implemented registers windows corresponds to NWIN+1.

80.11.3 ASR20, Alternative window register

This register allows access to the alternative window pointer. It is only implemented if the AWP support has been enabled in the processor.

*Table 1436.*LEON3 alternative window register (%asr20)

31 26	25 21	20 16
RESERVED	STWIN	CWPMAX
0	0	*
r	rw*	rw*

15 5	4 0
RESERVED	WCWP	AWP
0	-	*
r	w	rw

31:26	Reserved for future implementations
25:21	Starting window (STWIN) - Starting window of partition.
20:16	Maximum value of current window pointer (CWPMAX) - Partition size minus 1. Reset value is number of windows minus 1, which with STWIN=0 maps whole register file into partition. If this field is written with value 0, STWIN and CWPMAX fields are unmodified.
15:5	Reserved for future implementations
5	Write CWP - If written with 1, then the CWP field in PSR will simultaneously be written with the value written to AWP.
4:0	Alternative Window Pointer (AWP). Continuously updated with the value of CWP when the alternative window feature is disabled.

80.11.4 ASR22-23 - Up-counter

The ancillary state registers 22 and 23 (%asr22-23) contain an internal up-counter that can be read by software without causing any access on the on-chip AMBA bus. The number of available bits in the counter is implementation dependent and is decided by the number of counter bits in the DSU time tag counter. %ASR23 contains the least significant part of the counter value and %ASR22 contains the most significant part. In case the implementation does not contain a debug support unit connected to the processor then the up-counter is not available (value is always zero).

The time tag value accessible in these registers is the same time tag value used for the system's trace buffers (if implemented) and for all processors connected to the same debug support unit. The time tag counter will increment when any of the trace buffers is enabled, or when the time tag counter is forced to be enabled via the DSU register interface, or when any processor has its %ASR22 Disable Up-counter (DUCNT) field set to zero.

The up-counter value will increment even if all processors have entered power-down mode.

*Table 1437.*LEON3 up-counter MSbs (%ASR22)

31	30 … 0
DUCNT	UPCNT(62:32)

31	Disable Up-counter (DUCNT) - Disable upcounter. When set to '1' the up-counter may be disabled. When cleared, the counter will increment each processor clock cycle. Default (reset) value is '1'.
30:0	Counter value (UPCNT(62:32)) - Most significant bits of internal up-counter. Read-only.

*Table 1438.*LEON3 up-counter LSbs (%ASR23)

31 … 0
UPCNT(31:0)

31:0	Counter value (UPCNT(31:0)) - Least significant bits of internal up-counter. Read-only.

80.11.5 ASR24-31, Hardware watchpoint/breakpoint registers

Each breakpoint consists of a pair of ancillary state registers (%asr24/25, %asr26/27, %asr28/29 and %asr30/31) registers; one with the break address and one with a mask:

%asr24, %asr26
%asr28, %asr30

31 … 2	1	0
WADDR[31:2]		IF
NR	0	0
rw	r	rw

%asr25, %asr27
%asr29, %asr31

31 … 2		0
WMASK[31:2]	DL	DS
NR	0	0
rw	r	rw

Figure 223. Watch-point registers

WADDR - Address to compare against

WMASK - Bit mask controlling which bits to check (1) or ignore (0) for match

IF - break on instruction fetch from the specified address/mask combination

DL - break on data load from the specified address/mask combination

DS - break on data store to the specified address/mask comination

Note: Setting IF=DL=DS=0 disables the breakpoint

When there is a hardware watchpoint match and DL or DS is set then trap 0x0B will be generated. Hardware watchpoints can be used with or without the LEON3 debug support unit (DSU) enabled.

80.11.6 Cache control register

The cache control register located at ASI 0x2, offset 0, contains control and status registers for the I and D cache.

*Table 1439.*LEON3 Cache Control Register (CCR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED		RFT	PS	TB				DS	FD	FI	FT		RES	ST	IB
0		0	0	0				0	0	0	*		0	*	0
r		rw*	rw*	rw*				rw	rw*	rw*	r		r	r	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP	DP	ITE		IDE		DTE		DDE		DF	IF	DCS		ICS	
0	0	0		0		0		0		0	0	0		0	
r	r	r*		r*		r*		r*		rw	rw	rw		rw	

31:30	Reserved for future implementations
29	Register file test select (RFT). If set, will allow the read-out of IU register file checkbits via ASI 0x0F. Only available if fault-tolerance is enabled (FT field in this register is non-zero).
28	Parity Select (PS) - if set diagnostic read will return 4 check bits in the lsb bits, otherwise tag or data word is returned. Only available if fault-tolerance is enabled (FT field in this register is non-zero).
27:24	Test Bits (TB) - if set, check bits will be xored with test bits TB during diagnostic write. Only available if fault-tolerance is enabled (FT field in this register is non-zero).
23	Data cache snoop enable (DS) - if set, will enable data cache snooping.
22	Flush data cache (FD). If set, will flush the data cache. Always reads as zero.
21	Flush Instruction cache (FI). If set, will flush the instruction cache. Always reads as zero.
20:19	FT scheme (FT) - “00” = no FT, “01” = 4-bit checking implemented, “10” - Technology-specific protection implemented
18	Reserved for future implementations
17	Separate snoop tags (ST). This read-only bit is set if separate physical/snoop tags are implemented.
16	Instruction burst fetch (IB). This bit enables burst fill during instruction fetch.
15	Instruction cache flush pending (IP). This bit is set when an instruction cache flush operation is in progress
14	Data cache flush pending (DP). This bit is set when an data cache flush operation is in progress.
13:12	Instruction Tag Errors (ITE) - Number of detected parity errors in the instruction tag cache. Only available if fault-tolerance is enabled (FT field in this register is non-zero).
11:10	Instruction Data Errors (IDE) - Number of detected parity errors in the instruction data cache. Only available if fault-tolerance is enabled (FT field in this register is non-zero).
9:8	Data Tag Errors (DTE) - Number of detected parity errors in the data tag cache. Only available if fault-tolerance is enabled (FT field in this register is non-zero).
7:6	Data Data Errors (DDE) - Number of detected parity errors in the data data cache. Only available if fault-tolerance is enabled (FT field in this register is non-zero).
5	Data Cache Freeze on Interrupt (DF) - If set, the data cache will automatically be frozen when an asynchronous interrupt is taken.
4	Instruction Cache Freeze on Interrupt (IF) - If set, the instruction cache will automatically be frozen when an asynchronous interrupt is taken.
3:2	Data Cache state (DCS) - Indicates the current data cache state according to the following: X0= disabled, 01 = frozen, 11 = enabled.
1:0	Instruction Cache state (ICS) - Indicates the current data cache state according to the following: X0= disabled, 01 = frozen, 11 = enabled.

80.11.7 I-cache and D-cache configuration registers

The configuration of the two caches if defined in two registers: the instruction and data configuration registers. These registers are read-only and indicate the size and configuration of the caches. They are located under ASI 2 at offset 8 and 12.

*Table 1440.*LEON3 Cache configuration register

31	30 28	27	26 24	23 20	19	18 16
CL	REPL	SN	WAYS	WSIZE	LR	LSIZE
*	*	*	*	*	*	*
r	r	r	r	r	r	r

15 12	11 4	3	2 0
LRSIZE	LRSTART	M	RESERVED
*	*	*	0
r	r	r	r

31	Cache locking (CL). Set if cache locking is implemented.
30:28	Cache replacement policy (REPL). 00 - no replacement policy (direct-mapped cache), 01 - least recently used (LRU), 10 - least recently replaced (LRR), 11 - random
27	Cache snooping (SN). Set if snooping is implemented.
26:24	Cache associativity (WAYS). Number of ways in the cache: 000 - direct mapped, 001 - 2-way associative, 010 - 3-way associative, 011 - 4-way associative
23:20	Way size (WSIZE). Indicates the size (Kibs) of each cache way. Size = 2^{SIZE}
19	Local ram (LR). Set if local scratch pad ram is implemented.
18:16	Line size (LSIZE). Indicated the size (words) of each cache line. Line size = 2^{LSZ}
15:12	Local ram size (LRSZ). Indicates the size (Kibs) of the implemented local scratch pad ram. Local ram size = 2^{LRSZ}
11:4	Local ram start address. Indicates the 8 most significant bits of the local ram start address.
3	MMU present. This bit is set to ‘1’ if an MMU is present.
2	SO (supervisor only access) bit is present. This bit is set if *mmuen* generic is set to 2.
2:0	Reserved for future implementations

80.11.8 ASR16, Register protection control register (FT only)

ASR register 16 (%asr16) is used to control the IU/FPU register file SEU protection. It is possible to disable the SEU protection by setting the IDI/FDI bits, and to inject errors using the ITE/FTE bits. Corrected errors in the register file are counted, and available in ICNT and FCNT fields. The counters saturate at their maximum value (7), and should be reset by software after read-out.

*Table 1441.*LEON3FT Register protection control register (%asr16)

31 30	29 27	26 22	21 20	19 18	17	16
FPFT	FCNT	RESERVED	EFPFT	EIUFT	FTE	FDI
*	0	0	*	*	0	0
r	rw	r	r	r	rw	r

15 14	13 11	10 3	2	1	0
IUFT	ICNT	RFTB[7:0]	DP	ITE	IDI
*	0	0	0	0	0
r	rw	rw	rw	rw	rw

31:30	FP FT ID - Defines which SEU protection is implemented in the FPU (see table 1428)
29:27	FP RF error counter - Number of detected parity errors in the FP register file.
26:22	Reserved for future implementations
21:20	Extended IU FT ID - Top bits of IUFT field to indicate FT values higher than 3
19:18	Extended IU FT ID - Top bits of IUFT field to indicate FT values higher than 3
17	FPU RF Test Enable - Enables FPU register file test mode. Parity bits are xored with TB before written to the FPU register file.
16	FP RF protection disable (FDI) - Disables FP RF parity protection when set.
15:14	IU FT ID - Defines which SEU protection is implemented in the IU (see table 1428)
13:11	IU RF error counter - Number of detected parity errors in the IU register file.
10:3	RF Test bits (RFTB) - In test mode, these bits are xored with correct parity bits before written to the register file.
2	DP ram select (DP) - Only applicable if the IU or FPU register files consists of two dual-port rams. See table 1442 below.
1	IU RF Test Enable - Enables register file test mode. Parity bits are xored with TB before written to the register file.
0	IU RF protection disable (IDI) - Disables IU RF parity protection when set.

*Table 1442.*DP ram select usage

ITE/FTE	DP	Function
1	0	Write to IU register (%i, %l, %o, %g) will only write location of %rs2 Write to FPU register (%f) will only write location of %rs2
1	1	Write to IU register (%i, %l, %o, %g) will only write location of %rs1 Write to FPU register (%f) will only write location of %rs1
0	X	IU and FPU registers written nominally

80.11.9 MMU control register

The MMU control register is located in ASI 0x19 offset 0, and the layout can be seen in table 1443.

*Table 1443.*LEON3 MMU control register

31 28	27 24	23 21	20 18	17 16
IMPL	VER	ITLB	DTLB	PSZ
0	1	*	*	0
r	r	r	r	rw*

15	14	13	2	1	0
TD	ST	SO	RESERVED	NF	E
NR	0	0	0	0	0
rw*	r	rw	r	rw	rw

31:28 MMU Implementation ID. Hardcoded to “0000”

27:24 MMU Version ID. Hardcoded to “0001”.

23:21 Number of ITLB entries. The number of ITLB entries is calculated as 2^{ITLB}. If the TLB is shared between instructions and data, this field indicates to total number of TLBs.

20:18 Number of DTLB entries. The number of DTLB entries is calculated as 2^{DTLB}. If the TLB is shared between instructions and data, this field is zero.

17:16 Page size. The size of the smallest MMU page. 0 = 4 Kib; 1 = 8 Kib; 2 = 16 Kib; 3 = 32 Kib. If the page size is programmable, this field is writable, otherwise it is read-only.

15 TLB disable. When set to 1, the TLB will be disabled and each data access will generate an MMU page table walk. See Section 80.12.3 for detailed information.

14 Separate TLB. This bit is set to 1 if separate instruction and data TLBs are implemented

13 This bit only exists if *mmuen* generic is set to 2. This bit is written to the SO (supervisor only access) part of the TAG during diagnostic writes.

12:2 Reserved for future implementations

1 No Fault. When NF= 0, any fault detected by the MMU causes FSR and FAR to be updated and causes a fault to be generated to the processor. When NF= 1, a fault on an access to ASI 9 is handled as when NF= 0; a fault on an access to any other ASI causes FSR and FAR to be updated but no fault is generated to the processor.

0 Enable MMU. 0 = MMU disabled, 1 = MMU enabled.

80.11.10MMU context pointer and context registers

The MMU context pointer register is located in ASI 0x19 offset 0x100 and the MMU context register is located in ASI 0x19 offset 0x200. They together determine the location of the root page table descriptor for the current context. Their definition follows the SRMMU specification in the SPARC V8 manual with layouts shown below..

Table 1444. LEON3 MMU context pointer register

31 2	1 0
CONTEXT TABLE POINTER	R
NR	0
rw	r

31:2 Context table pointer, physical address bits 35:6 (note address is shifted 4 bits)

1:0 Reserved, always 0

Table 1445. LEON3 MMU context register

31 8	7 0
RESERVED	CONTEXT
0	0
r	rw

Table 1445. LEON3 MMU context register

31:8	Reserved
7:0	Current context ID

In the LEON3, the context bits are OR:ed with the lower MMU context pointer bits when calculating the address, so one can use less context bits to reduce the size/alignment requirements for the context table.

80.11.11MMU fault status register

The MMU fault status register is located in ASI 0x19 offset 0x300, and the definition follows the SRMMU specification in the SPARC V8 manual. The SPARC V8 specifies that the fault status register should be cleared on read, on the LEON3 only the FAV bit is cleared on read. The FAV bit is always set on error in the LEON3 implementation, so it can be used as a valid bit for the other fields..

*Table 1446.*LEON3 MMU fault status register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														EBE	
0														0	
r														r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EBE						L		AT			FT			FAV	OW
0						0		0			0			0	0
r						r		r			r			r	r

31:18	Reserved
17:10	External bus error (EBE) - Never set on the LEON3
9:8	Level (L) - Level of page table entry causing the fault
7:5	Access type (AT) - See V8 manual
4:2	Fault type (FT) - See table 1423
1	Fault address valid (FAV) - Cleared on read, always written to 1 on fault
0	Overwrite (W) - Multiple faults of the same priority encountered

80.11.12MMU fault address register

The MMU fault address register is located in ASI 0x19 offset 0x400, and the definition follows the SRMMU specification in the SPARC V8 manual...

*Table 1447.*LEON3 MMU fault address register

31	12	11	0
FAULT ADDRESS		RESERVED	
NR		0	
r		r	

31:12	Top bits of virtual address causing translation fault
11:0	Reserved, always 0

80.12 Software considerations

80.12.1 Register file initialization on power up (for LEON3FT)

After power-on, the check bits in the IU and FPU register files are not initialized. This means that access to an un-initialized (un-written) general-purpose register could cause a register access trap (tt = 0x20). Such behavior is considered as a software error, as the software should not read a register before it has been written. It is recommended that the boot code for the processor writes all registers in

the IU and FPU register files before launching the main application. This can be done also for the regular LEON3 to allow software to be portable to both FT and non-FT versions.

80.12.2 Start-up

After reset, the caches are disabled and the cache control register (CCR) is 0. Before the caches may be enabled, a flush operation must be performed to initialized (clear) the tags and valid bits. A suitable assembly sequence could be:

```
flush
set 0x81000f, %g1
sta %g1, [%g0] 2
```

80.12.3 MMU & TLB

After reset, the MMU is disabled and TLB is configured to be on (will not have any effect until MMU is enabled). Hence with default reset values the TLB has to be flushed before the MMU is being activated to initialize the valid bits in TLB. If the TLB is disabled while the MMU is active, the TLB must be flushed before enabled again.

80.12.4 Data scrubbing (LEON3FT)

There is generally no need to perform data scrubbing on either IU/FPU register files or the cache memory. During normal operation, the active part of the IU/FPU register files will be flushed to memory on each task switch. This will cause all registers to be checked and corrected if necessary. Since most real-time operating systems performs several task switches per second, the data in the register files will be frequently refreshed.

The similar situation arises for the cache memory. In most applications, the cache memory is significantly smaller than the full application image, and the cache contents is gradually replaced as part of normal operation. For very small programs, the only risk of error build-up is if a part of the application is resident in the cache but not executed for a long period of time. In such cases, executing a cache flush instruction periodically (e.g. once per minute) is sufficient to refresh the cache contents.

80.13 LEON3 versions

80.13.1 Overview

The primary way to identify the version of a implemented LEON3 processor is to look at the GRLIB build ID, plug&play device identifier and plug&play core revision (part of plug&play information, see GRLIB User's Manual for additional information). This documentation applies to version 3 of the LEON3 processor. Figure 224 shows the relationship between the different earlier LEON3 versions and the current LEON3v3.

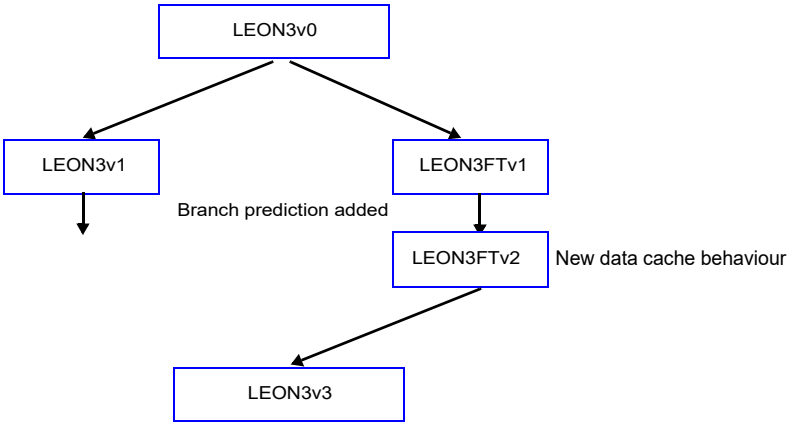


Figure 224. LEON3 processor evolution

80.13.2 Data cache and AMBA behavior changes

Earlier versions of the LEON3 processor made use of one separate word access for each accessed word, even with cache enabled. This manual describes LEON3v3 which is the only LEON3 version included by default in the GRLIB IP Library. The table below also show the behaviour of earlier versions of the processor.

Processor operation	**Area not cacheable[1]**	**LEON3FTv1/LEON3v1**		**LEON3FTv2/LEON3v3**	
		Area is cacheable[1]		**Area is cacheable[1]**	
		Cache enabled[2]	**Cache disabled**	**Cache enabled[2]**	**Cache disabled**
Data load <= 32-bit	*Read access with size specified by load instruction*	*Word access*	*Read access with size specified by load instruction*	Burst of 32-bit accesses to fetch full cache line.	Read access with size specified by load instruction
Data load 64-bit (LDD)	*Burst of two 32-bit accesses*				Burst of two 32-bit accesses
Data store <= 32-bit	Store access with size specified by store instruction.				
Data store 64-bit (STD)	Burst of two 32-bit store accesses				

[1] Cachability is determined by the *cached* VHDL generic, if *cached* is zero then cachability is determined via AMBA PnP.

[2] Bus accesses for reads will only be made on L1 cache miss or forced cache miss.

80.13.3 ASI 0x1 side effects

Reading from ASI 0x1 forces a real AMBA bus read and returns that data to the pipeline, and this behavior is implemented in all LEON3 and LEON3FT versions. However the side effects on the cache state (whether the cache is updated, and whether a line might be allocated) differs between different versions of the LEON3. Customers needing more information on this issue may contact Cobham Gaisler.

80.13.4 ASR writes from user mode

Ancillary state registers ASR17 and ASR19-31 were made privileged on write, starting from LEON3v3. To preserve backward compatibility, these registers are still readable from user mode.

80.13.5 MMU alias handling

LEON3v3 and LEON3FTv2 can handle double-mapped virtual addresses via self-snooping as described in section 80.3.8. This behavior is not available in earlier editions of LEON3, there the aliases can remain with incorrect data indefinitely.

80.13.6 CASA and load delay 2

With the current LEON3 (starting with GRLIB build 4178) CASA is always supported. LEON3 versions before GRLIB build 4161 only supported the compare-and-swap (CASA) instruction when the processor was implemented with load delay 1 (*lddel* VHDL generic set to 1) while the current version supports CASA for all load delays.

For GRLB versions more recent than build 4161, software can check if CASA is supported by reading %asr17 and checking the NOTAG field. For earlier GRLIB versions (prior to GRLIB build 4161) the %asr17 LDDEL field must be set to 0 for CASA to be supported and software can then probe for CASA support by trying to execute the instruction and handle the illegal instruction trap that is generated if CASA is unsupported by the implementation.

80.14 Vendor and device identifiers

The core will have one of two device identifiers depending on if the processor has been implemented with or without fault-tolerance features.

The standard core has vendor identifiers 0x01 (Cobham Gaisler) and device identifier 0x003.

If the core has been implemented with fault-tolerance features then the core will be identified with vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x053.

For a description of vendor and device identifiers see GRLIB IP Library User's Manual.

80.15 Implementation

80.15.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support *grlib_async_reset_enable*. All registers that react on the reset signal will have a synchronous reset.

80.15.2 Technology mapping

LEON3 has two technology mapping VHDL generics, *fabtech* and *memtech*. The *fabtech* generic controls the implementation of some pipeline features, while *memtech* selects which memory blocks will be used to implement cache memories and the IU/FPU register file. *fabtech* can be set to any of the provided technologies (0 - NTECH) as defined in the TECHMAP.GENCOMP package. See the GRLIB Users's Manual for available settings for *memtech*.

80.15.3 RAM usage

The LEON3 core maps all usage of RAM memory on the *syncram*, *syncram_2p* and *syncram_dp* components from the technology mapping library (TECHMAP). The type, configuration and number of RAM blocks is described below.

Register file

The register file is implemented with two *synram_2p* blocks for all technologies where the *regfile_3p_infer* constant in TECHMAP.GENCOMP is set to 0. The organization of the syncram_2p is shown in the following table:

*Table 1448.*syncram_2p sizes for LEON3 register file

Register windows	Syncram_2p organization
2 - 3	64x32
4 - 7	128x32
8 - 15	256x32
16-31	512x31
32	1024x32

If *regfile_3p_infer* is set to 1, the synthesis tool will automatically infer the register. On FPGA technologies, it can be in either flip-flops or RAM cells, depending on the tool and technology. On ASIC technologies, it will be flip-flops. The amount of flip-flops inferred is equal to the number of registers:

Number of flip-flops = ((NWINDOWS *16) + 8) * 32

FP register file

If FPU support is enabled, the FP register file is implemented with four *synram_2p* blocks when the *regfile_3p_infer* constant in TECHMAP.GENCOMP is set to 0. The organization of the syncram_2p blocks is 16x32.

If *regfile_3p_infer* is set to 1, the synthesis tool will automatically infer the FP register file. For ASIC technologies the number of inferred flip-flops is equal to number of bits in the FP register file which is 32 * 32 = 1024.

Cache memories

RAM blocks are used to implement the cache tags and data memories. Depending on cache configuration, different types and sizes of RAM blocks are used.

The tag memory is implemented with one *syncram* per cache way when no snooping is enabled. The tag memory depth and width is calculated as follows:

Depth = (cache way size in bytes) / (cache line size in bytes)

Width = 32 - log2(cache way size in bytes) + (cache line size in bytes)/4 + lrr + lock

For a 2 Kib cache way with lrr replacement and 32 bytes/line, the tag RAM depth will be (2048/32) = 64. The width will be: 32 - log2(2048) + 32/4 + 1 = 32 - 11 + 8 + 1 = 28. The tag RAM organization will thus be 64x28 for the configuration. If the MMU is enabled, the tag memory width will increase with 8 to store the process context ID, and the above configuration will us a 64x36 RAM.

If simple (MMU-less) snooping is enabled, the data cache tag memory will instead of single-port RAM blocks be implemented with a dual-port RAMs (syncram_dp) of the same size.

If physical (MMU-compatible) snooping is enabled, the data cache tag memories will be implemented using two *syncram_2p* components (with one read-only and one write-only port) per way , one memory for virtual and one for physical tags. The size of the virtual tag block will be the same as when snooping is disabled. The physical tag block will have the same depth as above and the data width corresponds to the width of the tag: 32 - log2(way size). A 4 KiB data cache way will thus require a 32 - 12 = 20 bit wide RAM block for the physical tags.

Physical snooping can also be implemented with valid bits placed in flip flops, the tag memories are then implemented using single-port memories and with one bit less in width for the virtual tag.

The data part of the caches (storing instructions or data) is always 32 bit wide. The depth is equal to the way size in bytes, divided by 4. A cache way of 2 KiB will thus use *syncram* component with and organization of 512x32.

Instruction Trace buffer

The instruction trace buffer will use four identical RAM blocks (*syncram*) to implement the buffer memory. The syncrams will always be 32-bit wide. The depth will depend on the *tbuf* VHDL generic, which indicates the total size of trace buffer in KiBs. If *tbuf* = 1 (1 KiB), then four RAM blocks of 64x32 will be used. If *tbuf* = 2, then the RAM blocks will be 128x32 and so on.

Scratch pad RAM

If the instruction scratch pad RAM is enabled, a *syncram* block will be instantiated with a 32-bit data width. The depth of the RAM will correspond to the configured scratch pad size. An 8 KiB scratch pad will use a *syncram* with 2048x32 organization. The RAM block for the data scratch pad will be configured in the same way as the instruction scratch pad.

80.15.4 Double clocking

LEON3 double clocking is described in the LEON/GRLIB Configuration and Development Guide.

80.15.5 Clock gating

LEON3 clock gating is described in the LEON/GRLIB Configuration and Development Guide.

80.15.6 Scan support

Scan test support using signals distributed via the AMBA records is included in the LEON3 as described in the GRLIB User's Manual. It can be enabled using the *scantest* VHDL generic.

80.16 Configuration options

Table 1449 shows the configuration options of the core (VHDL generics).

*Table 1449.*Configuration options

Generic	Function	Allowed range	Default
hindex	AHB master index	0 - NAHBMST-1	0
fabtech	Target technology	0 - NTECH	0 (inferred)
memtech	Vendor library for regfile and cache RAMs. Bits 16, 17 and 18 of this generic can be used to for the MMU TLB data RAM, IU register file and FP register file to inferred technology: + 2**16: Force inferred technology for MMU TLB data RAM + 2**17: Force inferred technology for IU register file + 2**18: Force inferred technology for FP register file Adding the value (2**17 + 2**18) is equivalent to setting the grlib.gencomp.regfile_3p_infer(memtech) to 1 (used for some technologies to force the register file implementations to inferred).	0 - 16#FFFFFFFF#	0 (inferred)
nwindows	Number of SPARC register windows. Choose 8 windows to be compatible with Bare-C and RTEMS cross-compilers.	2 - 32	8
dsu	Enable Debug Support Unit interface	0 - 1	0

*Table 1449.*Configuration options

Generic	Function	Allowed range	Default
fpu	Floating-point Unit 0 : no FPU 1 - 7: GRFPU 1 - inferred multiplier, 2 - DW multiplier, 3 - Module Generator multiplier, 4 - Technology specific multiplier 8 - 14: GRFPU-Lite 8 - simple FPC, 9 - data forwarding FPC, 10 - non-blocking FPC 15: Obsolete 16 - 31: as above (modulo 16) but use netlist	0 - 31	0
v8	Generate SPARC V8 MUL and DIV instructions This generic is assigned with the value: *mult + 4*struct* Where *mult* selects between the following implementation options for the multiplier and divider: 0 : No multiplier or divider 1 : 16x16 multiplier 2 : 16x16 pipelined multiplier 16#32# : 32x32 pipelined multiplier Where *struct* selects the structure option for the integer multiplier. The following structures can be selected: 0: Inferred by synthesis tool 1: Generated using Module Generators from NTNU 2: Using technology specific netlists (techspec). Only supported for RTAX-D FPGAs. Other technologies will assert a simulation error. 3: Using Synopsys DesignWare (DW02_mult and DW_mult_pipe)	0 - 16#3F#	0
cp	Generate co-processor interface	0 -1	0
mac	Generate SPARC V8e SMAC/UMAC instruction. Can only be used together with a 16x16 multiplier.	0 - 1	0
pclow	Least significant bit of PC (Program Counter) that is actually generated. PC[1:0] are always zero and are normally not generated. Generating PC[1:0] is convenient for VHDL-debugging and these bits should be optimized out by the synthesis tool.	0, 2	2
notag	Unused. Was previously used to disable tagged arithmetic and CASA instructions	0 - 1	0
nwp	Number of hardware watchpoints	0 - 4	0
icen	Enable instruction cache	0 - 1	1
irepl	Instruction cache replacement policy. 0 - least recently used (LRU), 1 - least recently replaced (LRR), 2 - random	0 - 1	0
isets	Number of instruction cache ways. Note: Generic named isets due to historical reasons.	1 - 4	1
ilinesize	Instruction cache line size in number of words	4, 8	4
isetsize	Size of each instruction cache way in KiB	1 - 256	1
isetlock	Enable instruction cache line locking	0 - 1	0
dcen	Data cache enable	0 - 1	1
drepl	Data cache replacement policy. 0 - least recently used (LRU), 1 - least recently replaced (LRR), 2 - random	0 - 1	0
dsets	Number of data cache ways Note: Generic named dsets due to historical reasons.	1 - 4	1
dlinesize	Data cache line size in number of words	4, 8	4

*Table 1449.*Configuration options

Generic	Function	Allowed range	Default
dsetsize	Size of each data cache way in KiB Note: If the processor is implemented with the MMU then the cache way size needs to be equal or less then the MMU page size for hardware cache coherency.	1 - 256	1
dsetlock	Enable data cache line locking	0 - 1	0
dsnoop	Enable data cache snooping Bit 0-1: 0: disable, 1: obsolete, 2: enabled, 3: single-port physical Bit 2: 0: simple MMU-less snooping, 1: save extra physical tags (MMU snooping)	0 - 7	0
ilram	Enable local instruction RAM	0 - 1	0
ilramsize	Local instruction RAM size in kB	1 - 512	1
ilramstart	8 MSB bits used to decode local instruction RAM area	0 - 255	16#8E#
dlram	Enable local data RAM (scratch-pad RAM)	0 - 1	0
dlramsize	Local data RAM size in kB	1 - 512	1
dlramstart	8 MSB bits used to decode local data RAM area	0 - 255	16#8F#
mmuen	Enable memory management unit (MMU) Note: Bus snooping is required to avoid cache aliasing effects when the MMU is enabled if the cache has more than one way. 0 : MMU does not exist. 1 : MMU exists. 2 : MMU exists and the cache tags include an additional bit called SO (supervisor only access). See sec. 80.3.2 for more details. If MMU is going to be instantiated in the processor, it is recommended to set the *mmuen* generic to 2.	0 - 2	0
itlbnum	Number of instruction TLB entries	2 - 64	8
dtlbnum	Number of data TLB entries	2 - 64	8
tlb_type	0 : separate TLB with slow write 1: shared TLB with slow write 2: separate TLB with fast write	0 - 2	1
tlb_rep	LRU (0) or Random (1) TLB replacement	0 - 1	0
lddel	Load delay. One cycle gives best performance, but might create a critical path on targets with slow (data) cache memories. A 2-cycle delay can improve timing but will reduce performance with about 5%.	1 - 2	2
disas	Print instruction disassembly in VHDL simulator console. Has no effect on synthesis (code removed via pragma translate_off)	0 - 1	0
tbuf	Size of instruction trace buffer in kB (0 - instruction trace disabled). For values 1-64 a single-port trace buffer of size *tbuf* is used. For values 65-128 a two-port trace buffer of size *tbuf*-64 is used.	0 - 128	0
pwd	Power-down. 0 - disabled, 1 - area efficient, 2 - timing efficient.	0 - 2	1
svt	Enable single-vector trapping	0 - 1	0

*Table 1449.*Configuration options

Generic	Function	Allowed range	Default
rstaddr	Default reset start address. This generic sets the 20 most significant bits of the reset address. The reset address must always be aligned on a 4 KiB address boundary. If this generic is set to 16#fffff# the processor will read its start address from the interrupt controller interface signal IRQI.RSTVEC (dynamic reset start address). See section 80.2.20 for more information.	0 - (2**20-1)	0
smp	Enable multi-processor support in pipeline (usually set in template designs to number of CPUs minus 1)	0 - 15	0
iuft, fpft	Register file SEU protection. (0: no protection; 1 : 4-bit parity, 2 : 8-bit parity; 3 : 7-bit BCH, 4: TMR, 5: BCH on-the-fly, 6: Tech-specific) See section 80.9.3 for fpft value restrictions.	0 - 6	0
cft	Enable cache memory SEU protection., bitfield Bit 7:4: Selects technology specific protection cache protection. 0 is parity protection, 5 is technology specific protection Bit 3:1: Unused Bit 0: If set, enable cache memory protection	0 - 255	0
iuinj ceinj	Enable random error injection during simulation. Used for simulation only, removed on synthesis using pragma translate_off. Only supported for FT version of LEON3FT.	0 - 3	0
cached	Fixed cacheability mask. Setting to nonzero overrides plug'n'play cacheability information.	0 - 16#FFFF#	0
clk2x	Double-clocking, frequency factor		0
netlist	Use netlist rather than RTL code (currently unused)	0 - 1	0
scantest	Enable scan test support	0 - 1	0
mmupgsz	MMU Page size. 0 = 4K, 1 = 8K, 2 = 16K, 3 = 32K, 4 = programmable.	0 - 4	0
bp	Enable branch prediction support, 0 - disabled, 1 - always enabled, 2 - programmable	0 - 2	1
npasi	Enable SPARC V8E nonprivileged ASI access. 0 - All accesses to alternate address space are privileged. 1 - LOAD and STORE from alternate space instructions accessing ASIs 0x00-0x7F are privileged, ASIs 0x80-0xFF are nonprivileged.	0 - 1	0
pwrpsr	Enable SPARC V8E partial write PSR (WRPSR).	0 - 1	0
rex	Enable LEON-REX extension	0 - 1	0
altwin	Enable alternative window pointer extension and register file partitioning	0 - 1	0

80.17 Signal descriptions

Table 1450 shows the interface signals of the core (VHDL ports). There are several top-level entities available for the LEON3 processor. The *leon3x* entity contains all signals and settings. The other entities are wrappers around *leon3x*. The available entities are:

- leon3cg - Top-level with support for clock gating. Deprecated, do not use for new designs.
- leon3ft2x - Top-level with support for FT, double clocking and clock gating.
- leon3ftsh - Entity with support for FT and shared FPU.
- leon3ft - Entity with support for FT and clock gating, no separate FPU clock.
- leon3s2x - Top-level with support for clock gating and double clocking, no separate FPU clock.
- leon3sh - Top-level with support for shared FPU.
- leon3s - Simplest top-level, no FT, clock gating or shared FPU.
- leon3x - Entity with support for all features (double clocking, FT, clock gating, shared FPU)

*Table 1450.*Signal descriptions

Signal name	Field	Type	Function	Active
leon3x:CLK leon3s2x:CLK leon3ftsh:CLK	N/A	Input	AMBA clock, used in 2x mode. Note that this only applies to the processor entities listed.	-
leon3x:GCLK2 leon3s:CLK leon3sh:CLK leon3s2x:GCLK2 leon3ft:GCLK leon3ftsh:GCLK leon3cg:GCLK leon3ft2x:GCLK2	N/A	Input	Processor clock, can be gated when using an entity where the clock name starts with “G”. Note that this clock has different names depending on which top-level entity that is used to instantiate the processor. For example, LEON3S only has one clock input which covers three of the rows in this table (Processor clock, FPU-clock, free running processor clock).	-
leon3x:GFCLK2 leon3s:CLK leon3sh:CLK leon3s2x:GCLK2 leon3ft:CLK leon3ftsh:CLK leon3cg:CLK leon3ft2x:GCLK2	N/A	Input	FPU clock, can be gated Note that this clock has different names depending on which top-level entity that is used to instantiate the processor. For example, LEON3S only has one clock input which covers three of the rows in this table (Processor clock, FPU-clock, free running processor clock).	-
leon3x:CLK2 leon3s:CLK leon3sh:CLK leon3s2x:GCLK2 leon3ft:CLK leon3ftsh:CLK leon3cg:CLK leon3ft2x:GCLK2	N/A	Input	Free running processor clock Note that this clock has different names depending on which top-level entity that is used to instantiate the processor. For example, LEON3S only has one clock input which covers three of the rows in this table (Processor clock, FPU-clock, free running processor clock).	-
RSTN	N/A	Input	Reset	Low
AHBI	*	Input	AHB master input signals	-

*Table 1450.*Signal descriptions

Signal name	Field	Type	Function	Active
AHBO	*	Output	AHB master output signals	-
AHBSI	*	Input	AHB slave input signals	-
AHBSO[]	*	Input	AHB slave output signals from all slaves on same bus. The processor makes use of the plug&play sideband signals to decode cacheability information of the bus. This can be overridden by the cached VHDL generic.	-
IRQI	IRL[3:0]	Input	Interrupt level	High
	RESUME	Input	Clear power-down and error mode	High
	RSTRUN	Input	Start after reset (SMP system only)	High
	RSTVEC[31:12]	Input	Reset start addr. (SMP and dynamic reset addr.)	-
	INDEX[3:0]	Input	Unused	-
	PWDSETADDR	Input	In power-down/error mode, shift PC to nPC and set PWDNEWADDR to PC.	High
	PWDNEWADDR [31:2]	Input	New PC value used with PWDSETADDR	-
	FORCEERR	Input	Force CPU into error mode	High
IRQO	INTACK	Output	Interrupt acknowledge	High
	IRL[3:0]	Output	Processor interrupt level	High
	PWD	Output	Processor in power-down mode	High
	FPEN	Output	Floating-point unit enabled	High
	ERR	Output	Processor in error mode	High
DBGI	-	Input	Debug inputs from DSU	-
DBGO	-	Output	Debug outputs to DSU	-
	ERROR		Processor in error mode, execution halted	Low
CLKEN		Input	Clock enable/qualifier used in 2x mode	High

* see GRLIB IP Library User's Manual

80.18 Signal definitions and reset values

When the processor enters error mode, the *errorn* output is driven active.

The signals and their reset values are described in table 1451.

*Table 1451.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
errorn	Tri-state output	Processor error mode indicator	Low	Tri-state

80.19 Timing

The timing waveforms and timing parameters are shown in figure 225 and are defined in table 1452.

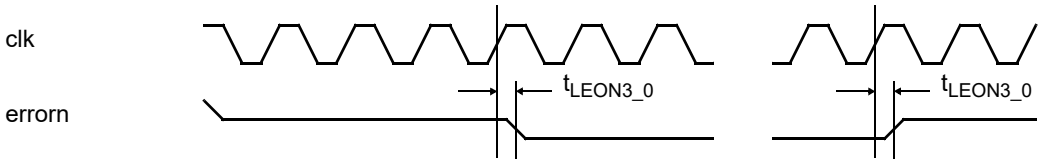


Figure 225. Timing waveforms

*Table 1452.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{LEON3_0}	clock to output delay	rising *clk* edge	TBD	TBD	ns

80.20 Library dependencies

Table 1453 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1453.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AHB signal definitions
GAISLER	LEON3	Component, signals	LEON3 component declaration, interrupt and debug signals declaration

80.21 Component declaration

The core has the following component declaration.

```
entity leon3s is
  generic (
    hindex    : integer                := 0;
    fabtech   : integer range 0 to NTECH  := 0;
    memtech   : integer range 0 to NTECH  := 0;
    nwindows  : integer range 2 to 32 := 8;
    dsu       : integer range 0 to 1  := 0;
    fpu       : integer range 0 to 3  := 0;
    v8        : integer range 0 to 2  := 0;
    cp        : integer range 0 to 1  := 0;
    mac       : integer range 0 to 1  := 0;
    pclow     : integer range 0 to 2  := 2;
    notag     : integer range 0 to 1  := 0;
    nwp       : integer range 0 to 4  := 0;
    icen      : integer range 0 to 1  := 0;
    irepl     : integer range 0 to 2  := 2;
    isets     : integer range 1 to 4  := 1;
    ilinesize : integer range 4 to 8  := 4;
    isetsize  : integer range 1 to 256 := 1;
    isetlock  : integer range 0 to 1  := 0;
    dcen      : integer range 0 to 1  := 0;
    drepl     : integer range 0 to 2  := 2;
    dsets     : integer range 1 to 4  := 1;
    dlinesize : integer range 4 to 8  := 4;
    dsetsize  : integer range 1 to 256 := 1;
    dsetlock  : integer range 0 to 1  := 0;
    dsnoop    : integer range 0 to 6:= 0;
    ilram      : integer range 0 to 1 := 0;
    ilramsize  : integer range 1 to 512 := 1;
```

```
    ilramstart : integer range 0 to 255 := 16#8e#;
    dlram      : integer range 0 to 1 := 0;
    dlramsize  : integer range 1 to 512 := 1;
    dlramstart : integer range 0 to 255 := 16#8f#;
    mmuen      : integer range 0 to 2 := 0;
    itlbnum    : integer range 2 to 64 := 8;
    dtlbnum    : integer range 2 to 64 := 8;
    tlb_type   : integer range 0 to 1 := 1;
    tlb_rep    : integer range 0 to 1 := 0;
    lddel      : integer range 1 to 2  := 2;
    disas      : integer range 0 to 1  := 0;
    tbuf       : integer range 0 to 64 := 0;
    pwd        : integer range 0 to 2  := 2;     -- power-down
    svt        : integer range 0 to 1  := 1;     -- single vector trapping
    rstaddr    : integer               := 0;
    smp        : integer range 0 to 15 := 0;    -- support SMP systems
    cached     : integer               := 0;     -- cacheability table
    scantest   : integer               := 0
    mmupgsz    : integer range 0 to 5  := 0;
    bp         : integer               := 1
);

port (
    clk    : in  std_ulogic;
    rstn   : in  std_ulogic;
    ahbi   : in  ahb_mst_in_type;
    ahbo   : out ahb_mst_out_type;
    ahbsi  : in  ahb_slv_in_type;
    ahbso  : in  ahb_slv_out_vector;
    irqi   : in  l3_irq_in_type;
    irqo   : out l3_irq_out_type;
    dbgi   : in  l3_debug_in_type;
    dbgo   : out l3_debug_out_type
  );
end;
```

81 LEON4 - High-performance SPARC V8 32-bit Processor

81.1 Overview

LEON4 is a 32-bit processor core conforming to the IEEE-1754 (SPARC V8) architecture. It is designed for embedded applications, combining high performance with low complexity and low power consumption.

The LEON4 core has the following main features: 7-stage pipeline with Harvard architecture, separate instruction and data caches, hardware multiplier and divider, on-chip debug support and multiprocessor extensions.

The LEON4 processor can be enhanced with fault-tolerance against SEU errors. The fault-tolerance is focused on the protection of on-chip RAM blocks, which are used to implement IU/FPU register files and the cache memory. Configuring the processor to implement fault-tolerance enables additional internal register and register fields.

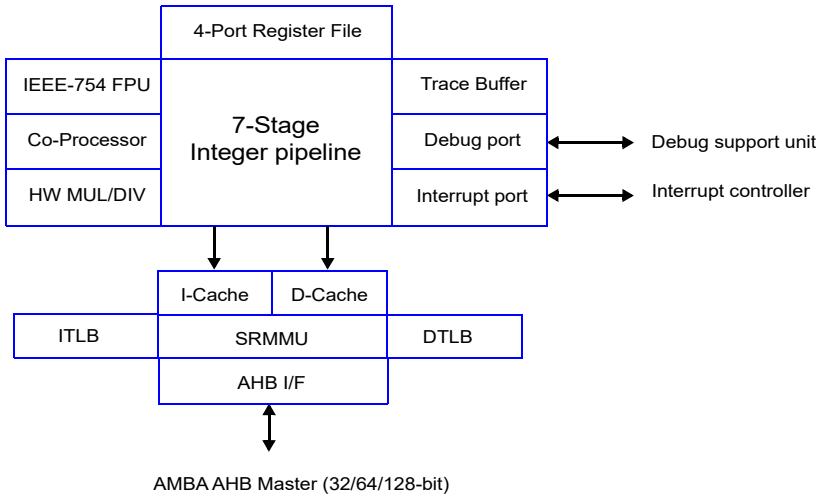


Figure 226. LEON4 processor core block diagram

Note: This manual describes the full functionality of the LEON4 core. Through the use of VHDL generics, parts of the described functionality can be suppressed or modified to generate a smaller or faster implementation.

Please also refer to the *LEON/GRLIB Configuration and Development Guide* for recommendations on system design and LEON4 configuration.

81.1.1 Integer unit

The LEON4 integer unit implements the full SPARC V8 manual, including hardware multiply and divide instructions. The number of register windows is configurable within the limit of the SPARC manual (2 - 32), with a default setting of 8. The pipeline consists of 7 stages with a separate instruction and data cache interface (Harvard architecture).

81.1.2 Cache sub-system

LEON4 has a highly configurable cache system, consisting of a separate instruction and data cache. Both caches can be configured with 1 - 4 ways, 1 - 256 KiB/way, 16 or 32 bytes per line. The instruction cache maintains one valid bit per cache line and uses streaming during line-refill to minimize refill latency. The data cache has one valid bit per cache line, uses write-through policy and imple-

ments a double-word write-buffer. Bus-snooping on the AHB bus can be used to maintain cache coherency for the data cache.

81.1.3 Floating-point unit and co-processor

The LEON4 integer unit provides interfaces for a floating-point unit (FPU), and a custom co-processor. Two FPU controllers are available, one for the high-performance GRFPU and one for the GRFPU-Lite core. The floating-point processors and co-processor execute in parallel with the integer unit, and does not block the operation unless a data or resource dependency exists. Note that the FPUs are provided separately.

81.1.4 Memory management unit

A SPARC V8 Reference Memory Management Unit (SRMMU) can optionally be enabled. The SRMMU implements the full SPARC V8 MMU specification, and provides mapping between multiple 32-bit virtual address spaces and physical memory. A three-level hardware table-walk is implemented, and the MMU can be configured to up to 64 fully associative TLB entries per implemented TLB.

81.1.5 On-chip debug support

The LEON4 pipeline includes functionality to allow non-intrusive debugging on target hardware. To aid software debugging, up to four watchpoint registers can be enabled. Each register can cause a breakpoint trap on an arbitrary instruction or data address range. When the (optional) debug support unit is attached, the watchpoints can be used to enter debug mode. Through a debug support interface, full access to all processor registers and caches is provided. The debug interfaces also allows single stepping, instruction tracing and hardware breakpoint/watchpoint control. An internal trace buffer can monitor and store executed instructions, which can later be read out via the debug interface.

81.1.6 Interrupt interface

LEON4 supports the SPARC V8 interrupt model with a total of 15 asynchronous interrupts. The interrupt interface provides functionality to both generate and acknowledge interrupts.

81.1.7 AMBA interface

The cache system implements an AMBA AHB master to load and store data to/from the caches. The interface is compliant with the AMBA-2.0 standard. During line refill, incremental burst are generated to optimise the data transfer. The AMBA interface can be configured to use a 64 or 128-bit bus on cache line fills. The processor also has a snoop AHB slave input port which is used to monitor the accesses made by other masters, if snooping has been enabled.

81.1.8 Power-down mode

The LEON4 processor core implements a power-down mode, which halts the pipeline and caches until the next interrupt. The processor supports optional clock gating during the power down period by providing a clock-enable signal that can be tied to an external clock gate cell, and by providing a separate clock input for the small part of the CPU that needs to run during power-down to check for wake-up conditions and maintain cache coherency.

81.1.9 Multi-processor support

LEON4 is designed to be used in multi-processor systems. Each processor has a unique index to allow processor enumeration. The write-through caches and snooping mechanism guarantees memory coherency in shared-memory systems.

81.2 LEON4 integer unit

81.2.1 Overview

The LEON4 integer unit implements the integer part of the SPARC V8 instruction set. The implementation is focused on high performance and low complexity. The LEON4 integer unit has the following main features:

- 7-stage instruction pipeline
- Separate instruction and data cache interface
- Support for 2 - 32 register windows
- Hardware multiplier with optional 16x16 bit MAC and 40-bit accumulator
- Radix-2 divider (non-restoring)
- Static branch prediction
- Single-vector trapping for reduced code size

Figure 227 shows a block diagram of the integer unit.

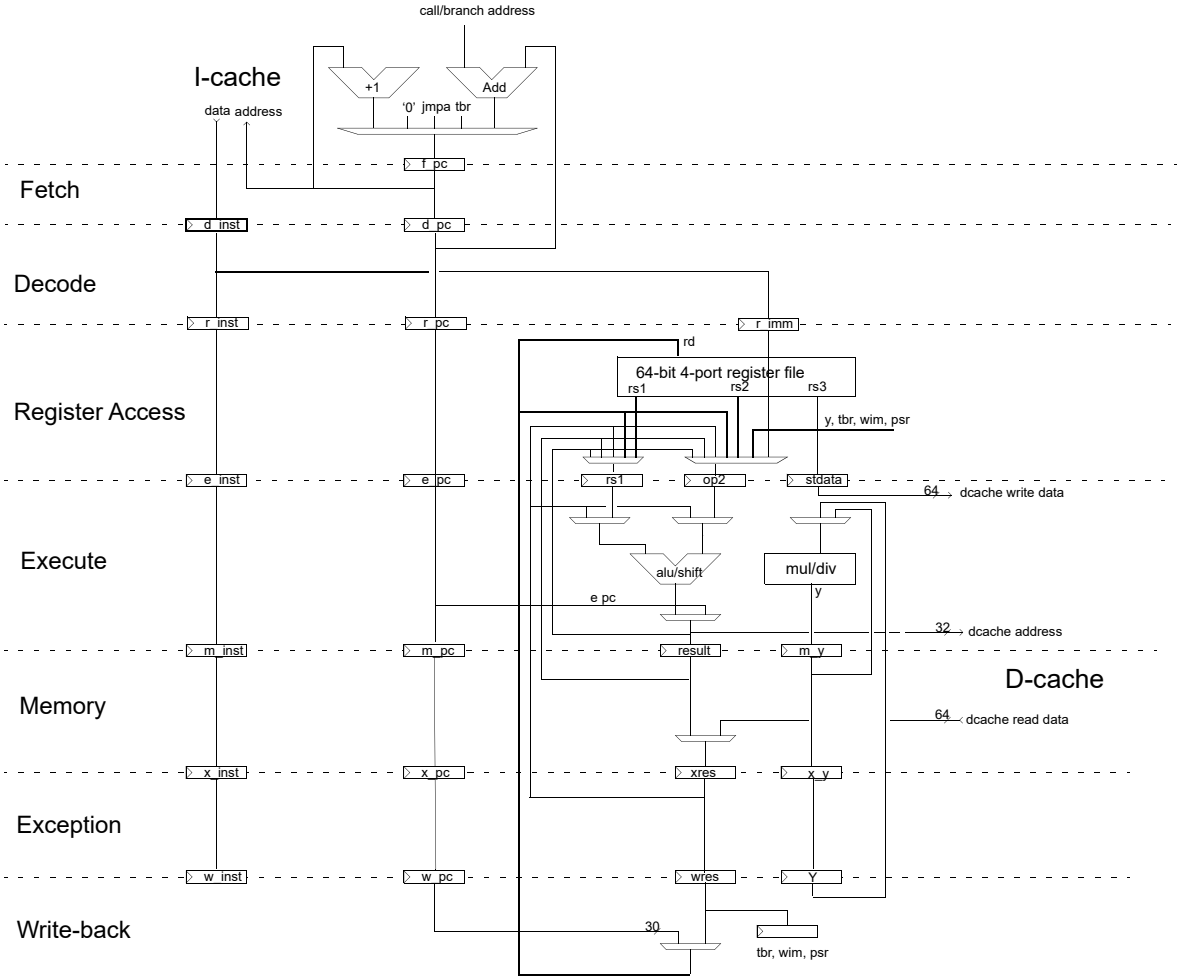


Figure 227. LEON4 integer unit datapath diagram

81.2.2 Instruction pipeline

The LEON4 integer unit uses a single instruction issue pipeline with 7 stages:

1. FE (Instruction Fetch): If the instruction cache is enabled, the instruction is fetched from the instruction cache. Otherwise, the fetch is forwarded to the memory controller. The instruction is valid at the end of this stage and is latched inside the IU.
2. DE (Decode): The instruction is decoded and the CALL/Branch target addresses are generated.
3. RA (Register access): Operands are read from the register file or from internal data bypasses.
4. EX (Execute): ALU, logical, and shift operations are performed. For memory operations (e.g., LD) and for JMPL/RETT, the address is generated.
5. ME (Memory): Data cache is accessed. Store data read out in the execution stage is written to the data cache at this time.
6. XC (Exception) Traps and interrupts are resolved. For cache reads, the data is aligned.
7. WR (Write): The result of ALU and cache operations are written back to the register file.

Table 1454 lists the cycles per instruction (assuming cache hit and no icc or load interlock):

*Table 1454.*Instruction timing

Instruction	Cycles (MMU disabled)
JMPL, RETT	3
SMUL/UMUL	1/4*
SDIV/UDIV	35
Taken Trap	5
Atomic load/store	5
All other instructions	**1**

* Multiplication cycle count is 1 clock (1 clock issue rate, 2 clock data latency), for the 32x32 multiplier and 4 clocks (issue rate, 4/5 clocks data latency for standard/pipelined version) for the 16x16 version.

Additional conditions that can extend an instructions duration in the pipeline are listed in the table and text below.

Branch interlock: When a conditional branch or trap is performed 1-2 cycles after an instruction which modifies the condition codes, 1-2 cycles of delay is added to allow the condition to be computed. If static branch prediction is enabled, this extra delay is incurred only if the branch is not taken.

Load delay: When using data resulting on a load shortly after the load, the instruction will be delayed to satisfy the pipeline's load delay. The processor pipeline has one cycle load delay.

Mul latency: For pipelined multiplier implementations there is 1 cycle extra data latency, accessing the result immediately after a MUL or MAC will then add one cycle pipeline delay.

Hold cycles: During cache miss processing or when blocking on the store buffer, the pipeline will be held still until the data is ready, effectively extending the execution time of the instruction causing the miss by the corresponding number of cycles. Note that since the whole pipeline is held still, hold cycles will not mask load delay or interlock delays. For instance on a load cache miss followed by a data-dependent instruction, both hold cycles and load delay will be incurred.

FPU/Coprocessor: The floating-point unit or coprocessor may need to hold the pipeline or extend a specific instruction. When this is done is specific to the FP/CP unit.

Certain specific events that cause these types of locks and their timing are listed in table 1455 below.

*Table 1455.*Event timing

Event	Cycles
Instruction cache miss processing, MMU disabled	3 + mem latency
Instruction cache miss processing, MMU enabled	5 + mem latency
Data cache miss processing, MMU disabled (read), L2 hit	3 + mem latency
Data cache miss processing, MMU disabled (write), write-buffer empty	0
Data cache miss processing, MMU enabled (read)	5 + mem latency
Data cache miss processing, MMU enabled (write), write-buffer empty	0
MMU page table walk	10 + 3 * mem latency
Branch prediction miss, branch follows ICC setting	2
Branch prediction miss, one instruction between branch and ICC setting	1
Pipeline restart due to register file or cache error correction	7

81.2.3 SPARC Implementor's ID

Cobham Gaisler is assigned number 15 (0xF) as SPARC implementor's identification. This value is hard-coded into bits 31:28 in the %psr register. The version number for LEON4 is 3 (same as for LEON3 to provide software compatibility), which is hard-coded in to bits 27:24 of the %psr.

81.2.4 Divide instructions

Full support for SPARC V8 divide instructions is provided (SDIV, UDIV, SDIVCC & UDIVCC). The divide instructions perform a 64-by-32 bit divide and produce a 32-bit result. Rounding and overflow detection is performed as defined in the SPARC V8 manual.

The divide instruction is required for full SPARC V8 compliance but can be configured out to save area using the *v8* VHDL generic.

81.2.5 Multiply instructions

The LEON processor supports the SPARC integer multiply instructions UMUL, SMUL UMULCC and SMULCC. These instructions perform a 32x32-bit integer multiply, producing a 64-bit result. SMUL and SMULCC performs signed multiply while UMUL and UMULCC performs unsigned multiply. UMULCC and SMULCC also set the condition codes to reflect the result. The multiply instructions are performed using a 32x32 pipelined hardware multiplier, or a 16x16 hardware multiplier which is iterated four times. To improve the timing, the 16x16 multiplier can optionally be provided with a pipeline stage.

The multiply instruction is required for full SPARC V8 compliance, but can be configured out to save area using the *v8* VHDL generic.

81.2.6 Multiply and accumulate instructions

To accelerate DSP algorithms, two multiply&accumulate instructions are implemented: UMAC and SMAC. The UMAC performs an unsigned 16-bit multiply, producing a 32-bit result, and adds the result to a 40-bit accumulator made up by the 8 lsb bits from the %y register and the %asr18 register. The least significant 32 bits are also written to the destination register. SMAC works similarly but performs signed multiply and accumulate. The MAC instructions execute in one clock but have two clocks latency, meaning that one pipeline stall cycle will be inserted if the following instruction uses the destination register of the MAC as a source operand.

The UMAC and SMAC instructions occupy the unused opcodes op=10,op3=1111110 for UMAC and op=10,op3=1111111 for SMAC.

Assembler syntax:

```
umac  rs1, reg_imm, rd
smac  rs1, reg_imm, rd
```

Operation:

```
prod[31:0] = rs1[15:0] * reg_imm[15:0]
result[39:0] = (Y[7:0] & %asr18[31:0]) + prod[31:0]
(Y[7:0] & %asr18[31:0]) = result[39:0]
rd = result[31:0]
```

%asr18 can be read and written using the RDASR and WRASR instructions.

The MAC instructions are an optional extension to SPARC V8, and enabled using the *mac* VHDL generic. The multiply and accumulate support also requires MUL/DIV support enabled by the *v8* VHDL generic and can only be used together with a 16x16 multiplier.

81.2.7 Compare and Swap instruction (CASA)

LEON4 implements the SPARC V9 Compare and Swap Alternative (CASA) instruction. The CASA operates as described in the SPARC V9 manual. The instruction is privileged, except when setting ASI = 0xA (user data).

81.2.8 Branch prediction

Static branch prediction can be optionally be enabled, and reduces the penalty for branches preceded by an instruction that modifies the integer condition codes. The predictor uses a branch-always strategy, and starts fetching instruction from the branch address. On a prediction hit, 1 or 2 clock cycles are saved, and there is no extra penalty incurred for misprediction as long as the branch target can be fetched from cache.

81.2.9 Register file data protection

The integer register file can optionally be protected against soft errors using triple modular redundancy (TMR) or technology specific protection (available for RTG4 target technology). Data errors will then be transparently corrected without impact at application level. The protection is enabled through the *ft* VHDL generic. The floating-point register file should be implemented with registers for applications that need FP register file protection.

81.2.10 Hardware breakpoints

The integer unit can be configured to include up to four hardware breakpoints. Each breakpoint consists of a pair of ancillary state registers (see section 81.11.4). Any binary aligned address range can be watched for instruction or data access, and on a breakpoint hit, trap 0x0B is generated.

81.2.11 Instruction trace buffer

The (optional) instruction trace buffer consists of a circular buffer that stores executed instructions. This is enabled and accessed only through the processor's debug port via the Debug Support Unit. When enabled, the following information is stored in real time, without affecting performance:

- Instruction address and opcode
- Instruction result
- Load/store data and address
- Trap information
- 30-bit time tag

The operation and control of the trace buffer is further described in section 25.4. Note that in multi-processor systems, each processor has its own trace buffer allowing simultaneous tracing of all instruction streams.

The size of the trace buffer is configurable from 1 to 64 KiB through the *tbuf* VHDL generic. If the value of tbuf is in the 65-128 range, a two-port instruction trace buffer of size *tbuf*-64 KiB will be used, allowing contextual reading of instructions while tracing is ongoing.

81.2.12 Processor configuration register

The ancillary state register 17 (%asr17) provides information on how various configuration options were set during synthesis. This can be used to enhance the performance of software, or to support enumeration in multi-processor systems. See section 81.11.4 for layout.

81.2.13 Exceptions

LEON4 adheres to the general SPARC trap model. The table below shows the implemented traps and their individual priority. When PSR (processor status register) bit ET=0, an exception trap causes the processor to halt execution and enter error mode, and the external error signal will then be asserted.

*Table 1456.*Trap allocation and priority

Trap	TT	Pri	Description	Class
reset	0x00	1	Power-on reset	Interrupting
data_store_error	0x2b	2	write buffer error during data store	Interrupting
instruction_access_exception	0x01	3	Error or MMU page fault during instruction fetch	Precise
privileged_instruction	0x03	4	Execution of privileged instruction in user mode	Precise
illegal_instruction	0x02	5	UNIMP or other un-implemented instruction	Precise
fp_disabled	0x04	6	FP instruction while FPU disabled	Precise
cp_disabled	0x24	6	CP instruction while Co-processor disabled	Precise
watchpoint_detected	0x0B	7	Hardware breakpoint match	Precise
window_overflow	0x05	8	SAVE into invalid window	Precise
window_underflow	0x06	8	RESTORE into invalid window	Precise
mem_address_not_aligned	0x07	10	Memory access to un-aligned address	Precise
fp_exception	0x08	11	FPU exception	Deferred
cp_exception	0x28	11	Co-processor exception	Deferred
data_access_exception	0x09	13	Access error during data load, MMU page fault	Precise
tag_overflow	0x0A	14	Tagged arithmetic overflow	Precise
division_by_zero	0x2A	15	Divide by zero	Precise
trap_instruction	0x80 - 0xFF	16	Software trap instruction (TA)	Precise
interrupt_level_15	0x1F	17	Asynchronous interrupt 15	Interrupting
interrupt_level_14	0x1E	18	Asynchronous interrupt 14	Interrupting
interrupt_level_13	0x1D	19	Asynchronous interrupt 13	Interrupting
interrupt_level_12	0x1C	20	Asynchronous interrupt 12	Interrupting
interrupt_level_11	0x1B	21	Asynchronous interrupt 11	Interrupting
interrupt_level_10	0x1A	22	Asynchronous interrupt 10	Interrupting
interrupt_level_9	0x19	23	Asynchronous interrupt 9	Interrupting
interrupt_level_8	0x18	24	Asynchronous interrupt 8	Interrupting
interrupt_level_7	0x17	25	Asynchronous interrupt 7	Interrupting
interrupt_level_6	0x16	26	Asynchronous interrupt 6	Interrupting
interrupt_level_5	0x15	27	Asynchronous interrupt 5	Interrupting
interrupt_level_4	0x14	28	Asynchronous interrupt 4	Interrupting
interrupt_level_3	0x13	29	Asynchronous interrupt 3	Interrupting
interrupt_level_2	0x12	30	Asynchronous interrupt 2	Interrupting
interrupt_level_1	0x11	31	Asynchronous interrupt 1	Interrupting

The prioritization follows the SPARC V8 manual.

The fp/cp_exception traps may be either deferred or precise depending on implementation, for the GRFPU and GRFPU-Lite implementations they are deferred. The data_store_error is delivered as a deferred exception but is non-resumable and therefore classed as interrupting in above table.

81.2.14 Single vector trapping (SVT)

Single-vector trapping (SVT) is an SPARC V8e option to reduce code size for embedded applications. When enabled, any taken trap will always jump to the reset trap handler (%tbr.tba + 0). The trap type will be indicated in %tbr.tt, and must be decoded by the shared trap handler. SVT is enabled by setting bit 13 in %asr17. The model must also be configured with the VHDL generic *svt* = 1.

81.2.15 Address space identifiers (ASI)

In addition to the address, a SPARC processor also generates an 8-bit address space identifier (ASI), providing up to 256 separate, 32-bit address spaces. During normal operation, the LEON4 processor accesses instructions and data using ASI 0x8 - 0xB as defined in the SPARC manual. Using the LDA/STA instructions, alternative address spaces can be accessed. The different available ASIs are described in section 81.10.

81.2.16 Partial WRPSR

Partial write %PSR (WRPSR) is a SPARC V8e option that allows WRPSR instructions to only affect the %PSR.ET field. If the processor has been implemented with support for partial WRPSR and the WRPSR instruction's rd field is non-zero, then the WRPSR write will only update ET.

The model must be configured with the VHDL generic pwrpsr = 1 for partial WRPSR to be supported. Implementations that do not support partial WRPSR will write the full %PSR register regardless of the value of the WRPSR instruction's rd field.

81.2.17 Power-down

The processor can be configured to include a power-down feature to minimize power consumption during idle periods. The power-down mode is entered by performing a WRASR instruction to %asr19:

```
wr %g0, %asr19
```

During power-down, the pipeline is halted until the next interrupt occurs. Signals inside the processor pipeline and caches are then static, reducing power consumption from dynamic switching.

Note: %asr19 must always be written with the data value zero to ensure compatiblity with future extensions.

Note: This instruction must be performed in supervisor mode with interrupts enabled.

When resuming from power-down, the pipeline will be re-filled from the point of power-down and the first instruction following the WRASR instruction will be executed prior to taking the interrupt trap. Up to six instructions after the WRASR instruction will be fetched (possibly with cache miss if they are not in cache) prior to fetching the trap handler.

81.2.18 Processor reset operation

The processor is reset by asserting the RESET input for at least 4 clock cycles. The following table indicates the reset values of a subset of the registers which are affected by the reset..

*Table 1457.*Processor reset values

Register	Reset value
Trap Base Register	Trap Base Address field reset (value given by *rstaddr* VHDL generic)
PC (program counter)	0x0 (*rstaddr* VHDL generic)
nPC (next program counter)	0x4 (*rstaddr* VHDL generic + 4)
PSR (processor status register)	ET=0, S=1

By default, the execution will start from address 0. This can be overridden by setting the *rstaddr* VHDL generic in the model to a non-zero value. The reset address is always aligned on a 4 KiB boundary. If *rstaddr* is set to 16#FFFFF#, then the reset address is taken from the signal IRQI.RST-VEC. This allows the reset address to be changed dynamically.

81.2.19 Multi-processor systems

In multiprocessor systems, the ID of the processor on which the code is executing can be read out by reading the index field of the LEON4 configuration register. Only processor 0 starts executing after reset, the others are in power-down mode and are activated by a signal from the interrupt controller.

81.2.20 LEON-REX extension

The processor can be built with support for the LEON-REX addition to the SPARC instruction set, allowing a more compact code representation than the regular SPARC machine code. The details of the extension are given in a separate document. The extension is implemented when the *rex* VHDL generic is set.

Detection of whether support is present can be done by checking the REXV field in the asr17 register (see section 81.11.2). The REX support can be set to enabled, illegal or transparent mode via the REXEN/REXILL bits in the asr17 register, after reset the default setting is illegal so any LEON-REX code will cause an illegal instruction trap.

The extension is implemented as a decompressor internally inside the pipeline and does not affect the behavior of the caches, MMU or AHB bus interfaces.

When the *rex* generic is set, the instruction trace buffer entries are changed so the two most significant bits of the time tag are instead used to represent REX mode enabled status, and bit 1 of the program counter. The instructions opcodes logged into the trace buffer are the regular SPARC opcodes that are generated internally in the pipeline, not the LEON-REX opcodes that are in memory and cache.

81.3 Cache system

81.3.1 Overview

The LEON4 processor pipeline implements a Harvard architecture with separate instruction and data buses, connected to two separate cache controllers. As long as the execution does not cause a cache miss, the cache controllers can serve one beat of an instruction fetch and one data load/store per cycle, keeping the pipeline running at full speed. Each cache controller can be configured with different sizes and replacement policy.

On cache miss, the cache controller will assert a hold signal freezing the IU pipeline, and after delivering the data the hold signal is again lifted so execution continues. For accessing the bus, the cache controllers share the same AHB connection to the on-chip bus. Certain parts of the MMU (table walk logic, and depending on configuration also TLB buffer) are also shared between the two caches.

Another important component included in the data cache is the write buffer, allowing stores to proceed in parallel to executing instructions.

Cachability (memory areas that are cachable) for both caches is controlled through the AHB plug&play address information or using a VHDL generic, see section 81.7.2.

81.3.2 Cache operation

Each cache controller has two main memory blocks, the tag memory and the data memory. At each address in the tag memory, a number of cache entries, ways, are stored for a certain set of possible memory addresses. The data memory stores the data for the corresponding ways.

For each way, the tag memory contains the following information:

- Valid bits saying if the entry contains valid data or is free. Both caches have a single valid bit for each cache line.
- The tag, all bits of the cached memory address that are not implied by the set
- If MMU is enabled, the context ID of the cache entry
- If MMU is enabled with *mmuen* generic set to 2, SO bit (supervisor only access)
- If LRR is used, a bit specifying the replacement order
- If FT is enabled, check bits for detecting errors (depending on the fault-tolerance implementation selected the check bits may or may not be visible to the user)

When a read from cache is performed, the tags and data for all cache ways of the corresponding set are read out in parallel, the tags and valid bits are compared to the desired address and the matching way is selected. In the hit case, this is all done in the same cycle to support the full execution rate of the processor.

In the miss case, the cache will at first deliver incorrect data. However on the following cycle, a hold signal will be asserted to prevent the processor from proceeding with that data. After the miss has been processed, the correct data is injected into the pipeline using a memory data strobe (mds) signal, and afterwards the hold signal can be released. If the missed address is cacheable, then the data read in from the cache miss will be stored into the cache, possibly replacing one of the existing ways.

In the instruction streaming case, the processor pipeline is stepped one step for every received instruction. If the processor needs extra pipeline cycles to stretch a multi-cycle instruction or due to an interlock condition (see section 81.2), or if the processor jumps/branches away, then the instruction cache will hold the pipe, fetch the remainder of the cache line, and the pipeline will then proceed normally.

81.3.3 Cache configuration options

Each cache controller can be configured to implement a single-way (direct-mapped) cache or a multi-way cache with set associativity of 2 - 4. The way size is configurable to 1 - 256 KiB, divided into cache lines with 16 or 32 bytes of data.

In multi-way configurations, one of three replacement policies can be selected:

- Least-recently-used (LRU) - This maintains the order of usage for each set in the cache and replaces the one which has was used last. The LRU information needs to be updated on every cache hit and is therefore not stored with the tags but in separate flip flops. When the LRU option is enabled the replacement policy becomes dynamically configurable between LRU, Least-recently-replaced, pseudo-random and a direct-mapped mode.
- Least-recently-replaced (LRR) - This stores the index of the oldest replaced way along with the tags and uses this to select which way to replace. This policy can only be implemented when the number of ways is set to 2.
- Pseudo-random - This method samples a free-running counter to select which way to replace. System jitter (AMBA bus delay variations) will help to randomize the selected value.

Note that when using locking together with LRU and more than two ways, this will add extra lookup tables to determine which way to replace and this might become a critical path in the core.

81.3.4 Address mapping

The addresses seen by the CPU are divided into tag, index and offset bits. The index is used to select the set in the cache, therefore only a limited number of cache lines with the same index part can be stored at one time in the cache. The tag is stored in the cache and compared upon read.

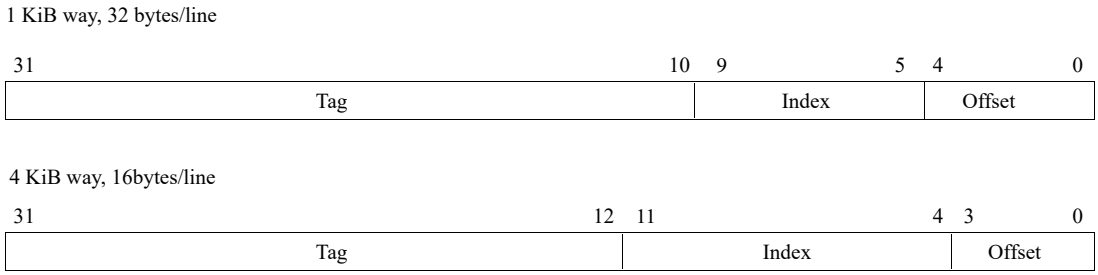


Figure 228. Cache address mapping examples

81.3.5 Data cache policy

The data cache employs a write-through policy, meaning that every store made on the CPU will propagate, via the write buffer, to the bus and there are no “dirty” lines in the cache that has not yet been written out apart from what is in the buffer. The store will also update the cache if the address is present, however a new line will not be allocated in that case.

*Table 1458.*LEON4 Data caching behavior

Operation	In cache	Cacheable	Bus action	Cache action	Load data
Data load	No	No	Read	No change	Bus
	No	Yes	Read	Line allocated/replaced	Bus
	Yes	-	None	No change	Cache
Data load with forced cache miss (ASI 1)	No	No	Read	No change	Bus
	No	Yes	Read	Line allocated/replaced	Bus
	Yes	-	Read	Data updated	Bus
Data load with MMU bypass (ASI 0x1C)	-	-	Read (phys addr)	No change	Bus
Data store	No	No	Write (via buffer)	No change	(N/A)
	No	Yes	Write (via buffer)	No change	(N/A)
	Yes	-	Write (via buffer)	Data updated	(N/A)
Data store with MMU bypass (ASI 0x1C)	-	-	Write (via buffer, phys addr)	No change	(N/A)

81.3.6 Write buffer

The data cache contains a write buffer able to hold a single 8,16,32, or 64-bit write. For half-word or byte stores, the stored data replicated into proper byte alignment for writing to a word-addressed device. The write is processed in the background so the system can keep executing while the write is being processed. However, any following instruction that requires bus access will block until the write buffer has been emptied. Loads served from cache will however not block, due to the cache policy used there can not be a mismatch between cache data and store buffer (the effect of this behavior on SMP systems is discussed in section 81.7).

Since the processor executes in parallel with the write buffer, a write error will not cause an exception to the store instruction. Depending on memory and cache activity, the write cycle may not occur until several clock cycles after the store instructions has completed. If a write error occurs, the currently

executing instruction will take trap 0x2b. This trap can be disabled using the DWT configuration (see section 81.11.2).

Note: a 0x2b trap handler should flush the data cache, since a write hit would update the cache while the memory would keep the old value due the write error

81.3.7 Operating with MMU

When MMU is enabled, the virtual addresses seen by the running code no longer correspond directly to the physical addresses on the AHB bus. The cache uses tags based on the virtual addresses, as this avoids having to do any additional work to translate the address in the most timing-critical hit case. However, any time a bus access needs to be made, a translation request has to be sent to the MMU to convert the virtual address to a physical address. For the write buffer, this work is included in the background processing of the store. The translation request to the MMU may result in memory accesses from the MMU to perform table walk, depending on the state of the MMU.

The MMU context ID is included in the cache tags in order to allow switching between multiple MMU contexts mapping the same virtual address to different physical addresses. Note that the cache does not detect aliases to the same physical address so in that case the same physical address may be cached in multiple ways (also see snooping below).

81.3.8 Snooping

The data cache can be configured to support AHB bus snooping. The AHB bus the processor is connected to, is monitored for writes from other masters to an address which is in the cache. If a write is done to a cached address, that cache line is marked invalid and the processor will be forced to fetch the (new) data from memory the next time it is read.

For using snooping together with the MMU, an extra tag memory storing physical tags must be added to allow comparing with the physical address on the AHB bus (called separate snoop tags or physical tags).

The processor can snoop on itself and invalidate any other cache lines aliased to the same physical address in case there are multiple virtual mappings to the same physical address that is being written. However, note that this does not happen until the write occurs on the bus so the other virtual aliases will return the old data in the meantime.

Snooping requires the way size of the cache to be equal or smaller than the MMU page size, otherwise the index into the physical and virtual tag RAM:s may not match, resulting in aliasing problems.

81.3.9 Enabling and disabling cache

Both I and D caches are disabled after reset. They are enabled by writing to the cache control register (see 81.11.5). Before enabling the caches after a reset they must be flushed to ensure that all tags are marked invalid.

81.3.10 Cache freeze

Each cache can be in one of three modes: disabled, enabled and frozen. If disabled, no cache operation is performed and load and store requests are passed directly to the memory controller. If enabled, the cache operates as described above. In the frozen state, the cache is accessed and kept in sync with the main memory as if it was enabled, but no new lines are allocated on read misses.

If the DF or IF bit is set, the corresponding cache will be frozen when an asynchronous interrupt is taken. This can be beneficial in real-time system to allow a more accurate calculation of worst-case execution time for a code segment. The execution of the interrupt handler will not evict any cache lines and when control is returned to the interrupted task, the cache state is identical to what it was before the interrupt. If a cache has been frozen by an interrupt, it can only be enabled again by

enabling it in the CCR. This is typically done at the end of the interrupt handler before control is returned to the interrupted task.

81.3.11 Flushing

Both instruction and data cache are flushed either by executing the FLUSH instruction, setting the FI/FD bits in the cache control register, or by writing to certain ASI address spaces.

Cache flushing takes one clock cycle per cache set, during which the IU will not be halted, but during which the caches are disabled. When the flush operation is completed, the cache will resume the state (disabled, enabled or frozen) indicated in the cache control register. Diagnostic access to the cache is not possible during a flush operation and will cause a data exception (trap=0x09) if attempted.

Note that while the SPARC V8 specifies only that the instructions pointed to by the FLUSH argument will be flushed, the LEON4 will additionally flush the entire I and D cache (which is permitted by the manual as the additional flushing only affects performance and not operation). While the LEON4 currently ignores the address argument, it is recommended for future compatibility to only use the basic flush %g0 form if you want the full flush behavior.

81.3.12 Locking

Cache line locking is not supported by LEON4. The VHDL generics to enable this feature are present in the LEON4 component declaration, but are unused.

81.3.13 Diagnostic access

The cache tag and data contents can be directly accessed for diagnostics and for locking purposes via various ASI:s, see section 81.10.5.

81.3.14 Local scratch pad RAM

Local scratch pad RAM is not supported by LEON4. The VHDL generics to enable this feature are present in the LEON4 component declaration, but are unused.

81.3.15 Fault tolerance support

The instruction and data cache can be protected a using mechanism implemented in the processor core (byte-parity codes) or by using functionality from SYNCRAMFT and SYNCRAM_2PFT. The most common option is to use parity protection that is provided by the processor. Use of the SYNCRAM protection allows the processor to use technology specific protection and this can lead to savings in resource utilization on target technologies that have built-in protection of SRAM blocks

On a detected error, the corresponding cache (I or D) will be flushed and the data will be refetched from external memory. This is done transparently to execution, and incur the same timing penalty as a regular cache miss. Enabling of the data protection is done through the *ft* VHDL generic and can only be implemented in GRLIB-FT releases.

81.4 Memory management unit

81.4.1 Overview

A memory-management unit can optionally be enabled. This is compatible with the SPARC V8 reference MMU (SRMMU) architecture described inthe SPARC V8 manual, appendix H.

The MMU provides address translation of both instructions and data via page tables stored in memory.When needed, the MMU will automatically access the page tables to calculate the correct physical address. The latest translations are stored in a special cache called the translation lookaside buffer (TLB), also referred to as Page Descriptor Cache (PDC) in the SRMMU specification. The MMU also

provides access control, making it possible to “sandbox” unpriviledged code from accessing the rest of the system.

81.4.2 MMU/Cache operation

When the MMU is disabled, the MMU is bypassed and the caches operate with physical address mapping. When the MMU is enabled, the cache tags store the virtual address and also include an 8-bit context field. Both the tag address and context field must match to generate a cache hit. When *mmuen* generic is set to 2 and MMU is enabled, the cache tags store a bit in addition to context called SO bit (supervisor only access). The SO bit is used to check the access permission of the data and instructions that resides in the level-1 caches when MMU is enabled. Without SO bit, access permissions of the load operations that hit in the data cache or the instruction accesses that hit in the instruction cache will not be checked properly.

If cache snooping is used, physical tags (separate snoop tags) must be enabled for it to work when address translation is used, see section 81.3.8.

Because the cache is virtually tagged, no extra clock cycles are needed in case of a cache load or instruction cache hit. In case of miss or write buffer processing, a translation is required which might add extra latency to the processing time, depending on TLB configuration and if there is a TLB miss.

The TLB can be configured in three different ways:

- Separate TLBs, slow access. TLB lookup adds 2 extra clock cycles.
- Shared TLB, slow access. TLB lookup adds 2 extra clock cycles, the TLB may be used by the other cache, leading to up to 4 extra cycles lookup time in the worst case.
- Separate TLBs, fast access. TLB lookup is done at the same time as tag lookup and therefore add no extra clock cycles.

If there is a TLB miss the page table must be traversed, resulting in up to four AMBA read accesses and one possible writeback operation. See the SRMMU specification for the exact format of the page table.

An MMU page fault will generate trap 0x09 for the D-cache and trap 0x01 for the I cache, and update the MMU status registers according to table 1459 and the SRMMU specification. In case of multiple errors, they fault type values are prioritized as the SRMMU specification requires. The cache and memory will not be modified on an MMU page fault.

*Table 1459.*LEON4 MMU Fault Status Register, fault type values

Fault type	SPARC V8 ref	Priority	Condition
6	Internal error	1	Never issued by LEON SRMMU
4	Translation error	2	AHB error response while performing table walk. Translations errors as defined in SPARC V8 manual. A translation error caused by an AMBA ERROR response will overwrite all other errors. Other translation errors do no overwrite existing translation errors when FAV = 1.
1	Invalid address error	3	Page table entry for address was marked invalid
3	Privilege violation error	4	Access denied based on page table and su status (see SRMMU spec for how privilege and protection error are prioritized)
2	Protection error	5	
0	None	-	No error (inside trap this means the trap occurred when fetching the actual data)

81.4.3 Translation look-aside buffer (TLB)

The MMU can be configured to use a shared TLB, or separate TLB for instructions and data. The number of TLB entries (for each implemented TLB) can be set to 2 - 64 via VHDL generics. The

organisation of the TLB and number of entries is not visible to the software and does thus not require any modification to the operating system. The TLB can be flushed using an STA instruction to ASI 0x18, see section 81.10.6.

81.4.4 Variable minimum page sizes

The standard minimum page size for the SRMMU is 4 KiB. The minimum page size can also be configured to 8, 16 or 32 KiB in order to allow for large data cache ways. The page size can either be configured hard at implementation time or made software-configurable via the MMU control register. The page sizes for level 1, 2 and 3 is seen in the table below:

*Table 1460.*MMU page size

Scheme	Level-1	Level-2	Level-3
4 KiB (default)	16 MiB	256 KiB	4 KiB
8 KiB	32 MiB	512 KiB	8 KiB
16 KiB	64 MiB	1 MiB	16 KiB
32 KiB	256 MiB	2 MiB	32 KiB

The layouts of the indexes are chosen so that PTE page tables can be joined together inside one MMU page without leaving holes.

Note that most operating systems are hard-coded for a specific page size and using one other than 4 KiB usually requires reconfiguration/recompilation of the operating system kernel.

81.5 Floating-point unit

The SPARC V8 architecture defines two (optional) co-processors: one floating-point unit (FPU) and one user-defined co-processor. Two different FPU's can be interfaced the LEON4 pipeline: Cobham Gaisler's GRFPU and GRFPU-Lite. Selection of which FPU to use is done through the VHDL model's VHDL generic map. The characteristics of the FPU's are described in the next sections.

81.5.1 Cobham Gaisler's floating-point unit (GRFPU)

The high-performance GRFPU operates on single- and double-precision operands, and implements all SPARC V8 FPU operations including square root and division. The FPU is interfaced to the LEON4 pipeline using a LEON4-specific FPU controller (GRFPC) that allows FPU instructions to be executed simultaneously with integer instructions. Only in case of a data or resource dependency is the integer pipeline held. The GRFPU is fully pipelined and allows the start of one instruction each clock cycle, with the exception is FDIV and FSQRT which can only be executed one at a time. The FDIV and FSQRT are however executed in a separate divide unit and do not block the FPU from performing all other operations in parallel.

All instructions except FDIV and FSQRT has a latency of three cycles, but to improve timing, the LEON4 FPU controller inserts an extra pipeline stage in the result forwarding path. This results in a

latency of four clock cycles at instruction level. The table below shows the GRFPU instruction timing when used together with GRFPC:

*Table 1461.*GRFPU instruction timing with GRFPC

Instruction	Throughput	Latency
FADDS, FADDD, FSUBS, FSUBD,FMULS, FMULD, FSMULD, FITOS, FITOD, FSTOI, FDTOI, FSTOD, FDTOS, FCMPS, FCMPD, FCMPES. FCMPED	1	4
FDIVS	14	16
FDIVD	15	17
FSQRTS	22	24
FSQRTD	23	25

The GRFPC controller implements the SPARC deferred trap model, and the FPU trap queue (FQ) can contain up to 7 queued instructions when an FPU exception is taken. When the GRFPU is enabled in the model, the version field in %fsr has the value of 2.

The GRFPU does not handle denormalized numbers as inputs and will in that case cause an fp_exception with the FPU trap type set to unfinised_FPOP (tt=2). There is a non-standard mode in the FPU that will instead replace the denormalized inputs with zero and thus never create this condition.

81.5.2 GRFPU-Lite

GRFPU-Lite is a smaller version of GRFPU, suitable for FPGA implementations with limited logic resources. The GRFPU-Lite is not pipelined and executes thus only one instruction at a time. To improve performance, the FPU controller (GRLFPC) allows GRFPU-Lite to execute in parallel with the processor pipeline as long as no new FPU instructions are pending. Below is a table of worst-case throughput of the GRFPU-Lite:

*Table 1462.*GRFPU-Lite worst-case instruction timing with GRLFPC

Instruction	Throughput	Latency
FADDS, FADDD, FSUBS, FSUBD,FMULS, FMULD, FSMULD, FITOS, FITOD, FSTOI, FDTOI, FSTOD, FDTOS, FCMPS, FCMPD, FCMPES. FCMPED	8	8
FDIVS	31	31
FDIVD	57	57
FSQRTS	46	46
FSQRTD	65	65

The GRLFPC controller implements the SPARC deferred trap model, but the FPU trap queue (FQ) can contain only one queued instructions when an FPU exception is taken.When the GRFPU-Lite is enabled in the model, the version field in %fsr has the value of 3.

81.6 Co-processor interface

No implementation for the user-defined co-processor is currently provided.

81.7 AMBA interface

81.7.1 Overview

The LEON4 processor has one AHB master interface. The types of AMBA accesses supported and performed by the processor depend on the accessed memory area's cachability, the maximum bus width, if the corresponding cache is enabled, and if the accessed memory area has been marked as being on the wide bus.

Cacheable instructions are fetched with a burst of 32-bit accesses, or 64- or 128-bit accesses depending on the cache line size and the AHB bus width.

The HPROT signals of the AHB bus are driven to indicate if the accesses is instruction or data, and if it is a user or supervisor access.

*Table 1463.*HPROT values

Type of access	User/Super	HPROT
Instruction	User	1100
Instruction	Super	1110
Data	User	1101
Data	Super	1111
MMU	Any	1101

In case of atomic accesses, a locked access will be made on the AMBA bus to guarantee atomicity as seen from other masters on the bus.

81.7.2 Cachability

Cachability for both caches can be controlled through the AHB plug&play address information or set manually via the *cached* VHDL generic.

For plug'n'play based cachability, the memory mapping for each AHB slave indicates whether the area is cachable, and this information is used to (statically) determine which access will be treated as cacheable. This approach means that the cachability mapping is always coherent with the current AHB configuration.

When the *cached* VHDL generic is not zero, it is treated as a 16-bit field, defining the cachability of each 256 MiB address block on the AMBA bus. For example, a value of 16#00F3# will define cachable areas in 0 - 0x20000000 and 0x40000000 - 0x80000000.

In order to access the plug'n'play information, the processor takes the ahbso vector as input. Only the static hconfig signals are used so the use of this input will be eliminated through constant propagation during synthesis.

81.7.3 AMBA access size

Cacheable data is fetched in a burst of 64- or 128-bit accesses, depending on the cache line size and AHB bus width. Data access to uncacheable areas may only be done with 8-, 16- and 32-bit accesses, i.e. the LDD and STD instructions may not be used.

If an area is marked as cacheable then the data cache will automatically try to use 64- or 128-bit accesses. This means that if 64- or 128-bit accesses need to be avoided, for example when performing Flash programming or if a slave does not support 64- or 128-bit accesses and is mapped as cacheable (this is a system design error), then software should only perform data accesses with using the cache bypass ASI and no 64-bit loads (LDD) when accessing the slave. One example of how to use cache bypass for loads is given by the following function:

```
static inline int load(int addr)
{
    int tmp;
    asm volatile(" lda [%1]0x1c, %0 "
        : "=r"(tmp)
        : "r"(addr)
        );
    return tmp;
}
```

The type of AMBA accesses used, and supported by the processor, for a memory area depends on the area's cachability and the values of the *wbmask* and *busw* VHDL generics.

The area which supports 64- or 128-bit access is indicated in the *wbmask* VHDL generic. This VHDL generic is treated as a 16-bit field, defining the 64/128-bit capability of each 256 MiB address block on the AMBA bus. A value of 16#00F3# will thus define areas in 0 - 0x20000000 and 0x40000000 - 0x80000000 to be 64/128-bit capable. The maximum access size to be used in the area(s) marked with WBMASK is determined by the *busw* VHDL generic.

Store instructions result in a AMBA access with size corresponding to the executed instruction, 64-bit store instructions (STD) are always translated to 64-bit accesses (never converted into two 32-bit stores as is done for LEON3). The table below indicates the access types used for instruction and data accesses depending on cachability, wide bus mask (wbmask), and cache configuration.

<table>
<tr><th rowspan="3">Processor operation</th><th colspan="3">Accessed memory area is 32-bit only, wbmask(address) = 0</th><th colspan="3">Accessed memory area is on wide bus wbmask(address) = 1</th></tr>
<tr><th rowspan="2">Area not cacheable[1]</th><th colspan="2">Area is cacheable[1]</th><th rowspan="2">Area not cacheable[1]</th><th colspan="2">Area is cacheable[1]</th></tr>
<tr><th>Cache enabled[2]</th><th>Cache disabled</th><th>Cache enabled[2]</th><th>Cache disabled</th></tr>
<tr><td>Instruction fetch</td><td>Burst of 32-bit read accesses</td><td colspan="2">Burst of 32-bit read accesses</td><td colspan="3">Burst of 64- or 128-bit accesses[5]</td></tr>
<tr><td>Data load <= 32-bit</td><td rowspan="3">Read access with size specified by load instruction</td><td rowspan="2">Illegal[3,6] Burst of 32-bit accesses, software may get incorrect data</td><td rowspan="2">Read access with size specified by load instruction</td><td rowspan="3">Read access with size specified by load instruction</td><td rowspan="2">Burst of 64- or 128-bit accesses[5]</td><td rowspan="2">Read access with size specified by load instruction</td></tr>
<tr><td>Data load <= 32-bit with ASI 0x01</td></tr>
<tr><td>Data load <= 32-bit with ASI 0x1C</td><td colspan="2">Read access with size specified by load instruction[6]</td><td colspan="2">Read access with size specified by load instruction[6]</td></tr>
<tr><td>Data load 64-bit (LDD)</td><td>Illegal[4] Single 64-bit access will be performed</td><td>Illegal[3] Burst of 64- or 128-bit accesses[5]</td><td>Illegal[3] Single 64-bit access will be performed</td><td>Illegal[4] Single 64-bit access will be performed</td><td>Burst of 64- or 128-bit accesses[5]</td><td>Single 64-bit read access</td></tr>
<tr><td>Data store <= 32-bit</td><td colspan="6">Store access with size specified by store instruction.</td></tr>
<tr><td>Data store 64-bit (STD)</td><td colspan="3">Illegal (64-bit store performed to 32-bit area) 64-bit store access will be performed.</td><td colspan="3">64-bit store access</td></tr>
</table>

Cells with red text show unsupported combinations of settings for wide bus and cacheability. The LEON4 core requires that all cacheable areas are can handle wide bus accesses (64- or 128-bit). Implementing the core with cacheable areas where wbmask is 0 is unsupported. The table lists the behaviour in these cases for completeness.

[1] Cachability is determined by the *cached* VHDL generic, if *cached* is zero then cachability is determined via AMBA PnP.

[2] Bus accesses for reads will only be made on L1 cache miss, load with forced cache miss or loads with cache bypass.

[3] LEON4 is designed to always make use of wide bus accesses for cacheable data. Cacheable data can only be handled with 64- or 128 bit accesses.

[4] Data accesses to uncachable areas may only be done with 8-, 16- and 32-bit accesses.

[5] 64- or 128-bit accesses depending on *busw* VHDL generic.

[6] Loads with cache bypass (ASI 0x1C) can be used to perform single accesses to cachable slaves.

81.7.4 Error handling

An AHB ERROR response received while fetching instructions will normally case an instruction access exception (tt=0x1). However if this occurs during streaming on an address that is not needed, the I cache controller will just not set the corresponding valid bit in the cache tag. If the IU later fetches an instruction from the failed address, a cache miss will occur, triggering a new access to the failed address.

An AHB ERROR response while fetching data into the data cache will normally trigger a data_access_exception trap (tt=0x9). If the error was for a part of the cache line other than what was currently being requested by the pipeline, a trap is not generated and the valid bit for that line is not set.

An ERROR response during an MMU table walk will lead the MMU to set the fault type to Internal error (1) and generate an instruction or data access exception, depending on which type of access that caused the table walk.

81.7.5 Snoop port

For the snooping logic, the LEON4 has an ahbsi input. For correct function, this must be tied to the same AHB bus that the master interface. It is not possible to snoop on another bus or to add extra pipeline registers to the snoop port, because the snoop logic must be in sync with the master interface.

81.8 Multi-processor system support

This section gives an overview of issues when using the LEON4 in multi-processor configuration.

Using the features described in earlier sections together with a multiprocessor capable IRQ controller (IRQMP, IRQ(A)MP), the LEON4 processor can support symmetric multiprocessing (SMP) configurations with shared memory, with up to 16 processors attached to the same AHB bus.

Enabling SMP features (sleeping on reset for CPU 1-N) is done by setting the *smp* VHDL generic to 1 or higher. Cache snooping should always be enabled in SMP systems to maintain data cache coherency between the processors.

81.8.1 Start-up

In multiprocessor systems, only the first processor will start after reset and all other processors will remain halted in power-down mode. After the system has been initialized, the remaining processors can be started by writing to the ‘multiprocessor status register’, located in the multiprocessor interrupt controller. The halted processors start executing from the reset address (0 or *rstaddr* VHDL generic, see section 81.2.18).

An application in a multiprocessor system can determine which processor it is executing on by checking the processor index field in the LEON4 configuration register (%asr17). As all processors typically have the same reset start address value, boot software must check the processor index and perform processor specific setup (e.g. initialization of stack pointer) based on the value of the processor index.

In recent versions of the LEON4, and if the IRQ controller is configured with the extended boot register extension, it is possible for one processor to monitor and reboot another processor.via the interrupt controller. This requires careful software design.

For earlier versions of the LEON4, this is not supported and if software detects that one processor is unresponsive and needs to restart the processor then the full system should be reset, for example by triggering the system’s watchdog, if implemented. In order for software to monitor that all processors in a system are up and running it is recommended to implement a heartbeat mechanism in software.

While it is possible to have more fine-grained control over processor behaviour via the Debug Support Unit (if implemented) this is not recommended as the debug support unit is typically disabled in production mode.

81.8.2 Shared memory model

Each processor core has it’s own separate AHB master interface and the AHB controller will arbitrate between them to share access to the on-chip bus.

If caches are not used, the processors will form a sequentially consistent (SC) system, where every processor will execute it’s loads, stores and atomics to memory in program order on the AHB bus and

the different processors operations will be interleaved in some order through the AHB arbitration. The shared memory controller AHB slave is assumed to not reorder accesses so a read always returns the latest written value to that location on the bus.

When using caches with snooping (and with separate physical tags, also called separate snoop tags, if using the MMU), the shared memory will act according to the slightly weaker SPARC Total Store Order (TSO) model. The TSO model is close to SC, except that loads may be reordered before stores coming from the same CPU. The stores and atomics are conceptually placed in a FIFO (see the diagrams in the SPARC manual) and the loads are allowed to bypass the FIFO if they are not to the same address as the stores. Loaded data from other addresses may therefore be either older or newer, with respect to the global memory order, than the stores that have been performed by the same CPU.

In the LEON4 case this happens because cache hits are served without blocking even when there is data in the write buffer. The loaded data will always return the stored data in case of reading the same address, because if it is cached, the store updates the cache before being put in the write buffer, and if it was not in cache then the load will result in a miss which waits for the write buffer to complete. Loaded data from a different address can be older than the store if it is served by cache before the write has completed, or newer if it results in a cache miss or if there is a long enough delay for the store to propagate to memory before reading.

See relevant literature on shared memory systems for more information. These details are mainly of concern for complex applications using lock-free data structures such as the Linux kernel, the recommendation for applications is to instead avoid concurrent access to shared structures by using mutexes/semaphores based on atomic instructions, or to use message passing schemes with one-directional circular buffers.

81.8.3 Memory-mapped hardware

Hardware resources (IP cores) are normally memory mapped on uncacheable address spaces. They will be accessible from all the CPU:s in a sequentially consistent manner. Since software drivers usually expect to be “alone” accessing the IP core and the IP cores register interfaces are not designed for concurrent use by multiple masters, using a bare-C application designed for single-processor usage on multiple cores at the same time will generally not work. This can be solved by partitioning the applications so that each IP core is only accessed by one of the CPU:s. This partitioning also need to be done between the interrupts so the IP core’s interrupts will be received by the correct processor.

81.9 Fault tolerance

81.9.1 Overview

The LEON3 processor can be enhanced with fault-tolerance against SEU errors (referred to as LEON3FT). The fault-tolerance is focused on the protection of on-chip RAM blocks, which are used to implement IU register file and the cache memory.

The LEON4 with FT features is licensed separately, and in the commercial LEON4 releases setting the FT VHDL generic will not have any effect.

81.9.2 Integer register file protection

The SEU protection for the integer unit register file can be implemented in two different ways, depending on target technology and available RAM blocks. The SEU protection scheme is selected

during synthesis, using the *ft* VHDL generic. Table 1464 below shows the implementation characteristics of the four possible SEU protection schemes.

*Table 1464.*Integer unit SEU protection schemes

ID	Implementation	Description	Usage
0	No protection (hardening at lower level)	No error checking, equivalent to non-FT version. Register file hardness must be ensured separately, for example by mapping the register file memories to SEU hardened flip-flops.	IU
4	Memory triplication	Memory blocks triplicated and bit by bit voted on outputs. Correction on-the-fly without pipeline restart, no error injection interface or error counters. Note that care must be taken by the implementer to ensure that the TMR is not collapsed in optimization by synthesis tools.	IU
6	Technology specific	Implement register files using native ECC capability of the technology (via syncram_2pft in the techmap library). Only valid for subset of (FPGA) technologies. Correction on-the-fly without pipeline restart. Error injection and error counters may be supported depending on technology.	IU

An uncorrectable error in the IU register file will cause trap 0x20 (*r_register_access_error*). A dedicated counter exists in ASR16 to count the number of register file corrections.

The register file is implemented using scheme 0 if the regfile_4p_infer array is set for the selected memory technology in the techmap library, or if bits 16-17 of the memtech VHDL generic are set.

81.9.3 Floating-point register file protection

The FPU register file is implemented with registers.

Note that the restrictions on protection scheme is not enforced, so it is recommended to simulate the configuration with error injection to ensure that the scheme chosen is functioning correctly. It is also recommended to confirm in the netlist that the expected register file type (memory block or flip flops) was implemented.

81.9.4 Cache protection

Each word in the tag or data memories is normally protected by four check bits. Use of the SYNCRAM protection allows the processor to use technology specific protection and this can lead to savings in resource utilization on target technologies that have built-in protection of SRAM blocks. If separate physical tags for snooping are enabled, the physical tag memory is also protected. An error during cache access will cause an invalidation of the cache, and a re-execution of the failing instruction. This will ensure that the complete cache line (tags and data) is refilled from external memory.

If snooping is enabled, an error detected in the tags while snooping a write to that set will lead to that cache data being invalidated (since the tag before the error might have matched the written address).

81.10 ASI assignments

81.10.1 Summary

The table shows the ASI usage for LEON.

*Table 1465.*ASI usage

ASI	Usage
0x01	Forced cache miss.
0x02	System control registers (cache control register)
0x08, 0x09	Not supported
0x0A	Access level is determined by 'S' bit in %psr when MMU is enabled and *mmuen* generic is set to 1 User Access when MMU is enabled and *mmuen* generic is set to 2 Sets HPROT to user data regardless of MMU
0x0B	Access level is determined by 'S' bit in %psr when MMU is enabled and *mmuen* generic is set to 1 Supervisor Access when MMU is enabled and *mmuen* generic is set to 2, otherwise normal cache access Sets HPROT to supervisor data regardless of MMU
0x0C	Instruction cache tags
0x0D	Instruction cache data
0x0E	Data cache tags
0x0F	Data cache data
0x0F	Register file diagnostic parity read-out (FT only)
0x10	Flush instruction cache (and also data cache when system is implemented with MMU)
0x11	Flush data cache
0x13	MMU only: Flush instruction and data cache
0x14	MMU only: MMU diagnostic D context cache access (deprecated, do not use)
0x15	MMU only: MMU diagnostic I cache context access (deprecated, do not use)
0x18, 0x03	MMU only: Flush TLB and I/D cache
0x19, 0x04	MMU only: MMU registers
0x1C	MMU and cache bypass
0x1D	MMU only: MMU diagnostic access (deprecated, do not use)
0x1E	MMU only: MMU snoop tags diagnostic access

81.10.2 ASI 0x1, Forced cache miss

ASI 1 is used for systems without cache coherency, to load data that may have changed in the background, for example by DMA units. It can also be used for other reasons, for example diagnostic purposes, to force a AHB load from memory regardless of cache state.

The address mapping of this ASI is matched with the regular address space, and if MMU is enabled then the address will be translated normally. Stores to this ASI will perform the same way as ordinary data stores.

For situations where you want to guarantee that the cache is not modified by the access, the MMU and cache bypass ASI, 0x1C, can be used instead.

81.10.3 ASI 0x2, System control registers

ASI 2 contains a few control registers that have not been assigned as ancillary state registers. These should only be read and written using 32-bit LDA/STA instructions.

All cache registers are accessed through load/store operations to the alternate address space (LDA/STA), using ASI = 2. The table below shows the register addresses:

*Table 1466.*ASI 2 (system registers) address map

Address	Register
0x00	Cache control register
0x04	Reserved
0x08	Instruction cache configuration register
0x0C	Data cache configuration register

81.10.4 ASI 0x8-0xB, Data/Instruction

These ASIs are assigned by the SPARC manual for normal data and instruction fetches.

Accessing the instruction ASIs explicitly via LDA/STA instructions is not supported in the LEON4 implementation.

Using LDA/STA with the user/supervisor data ASI (0xA,0xB) will behave as the affect the HPROT signal emitted by the processor according to section 81.7.1. If *mmuen* generic is set to 2, MMU access control will be done according to the indicated user or supervisor ASI inline with reference MMU description in Sparc V8 manual. If *mmuen* generic is set to 1, MMU access control will be done depending on the SU bit in the %psr register.

81.10.5 ASI 0xC-0xF, ICache tags/data, DCache tags/data

ASI 0xC-0xF provide diagnostic access to the instruction cache memories. These ASIs should only be accessed by 32-bit LDA/STA instructions. These ASIs can not be used while a cache flush is in progress.

The same address bits used normally as index are used to index the cache also in the diagnostic access. For a multi-way cache, the lowest bits above the index part, the lowest bits that would normally be used as tag, are used to select which way to read/write. The remaining address bits are don't cares, leading the address map to wrap around.

If fault tolerance is enabled, the tag parity, context and SO bits can also be read out through these ASIs by setting the PS bit in the cache configuration register. When this bit is set, the parity data is read instead of the ordinary data. When writing the tag bits, the context bits will always be written with the current context in the MMU control register. The SO bit in the tag will be written with the SO bit value in the MMU control register (SO bit in MMU control register only exists in the tag when *mmuen* generic is set to 2). The parity to be written is calculated based on the supply write-value, the context ID and optionally SO bit (if mmuen is set to 2) in the MMU control register. The parity bits can be modified via the TB field in the cache control register.

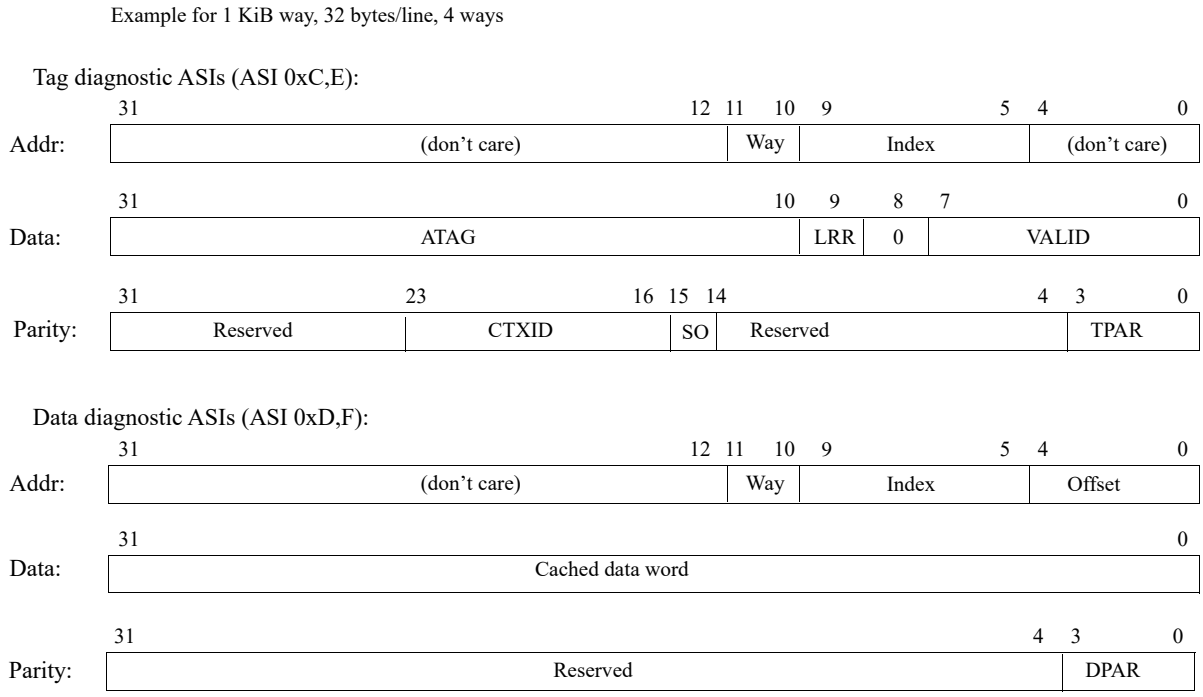


Figure 229. ASI 0xC-0xF address mapping and data layout

Field Definitions:

Address Tag (ATAG) - Contains the tag address of the cache line.

LRR - Used by LRR algorithm to store replacement history, otherwise 0.

Valid (V) - When set, the cache line contains valid data. The LEON4 caches only have one valid bit per cache line which is replicated for the whole 8-bit diagnostic field to keep software backward compatibility.

CTXID - Context ID, used when MMU is enabled.

SO - (Supervisor only access) It is used when MMU is enabled and *mmuen* (see Sec. 81.15) generic is set to 2. This bit is set to 1 when the associated page with the tag has access permission of 6 or 7 (supervisor access only) for other access permissions it is set to 0. (For detailed information about access permissions refer to the reference MMU part of the Sparc V8 manual)

TPAR - Byte-wise parity of tag bits, context ID parity is XOR:ed into bit 3.

DPAR - Byte-wise parity of data bits

NOTE: only the necessary bits will be implemented in the cache tag, depending on the cache configuration. As an example, a 4 KiB cache with 16 bytes per line would only have four valid bits and 20 tag bits. The cache rams are sized automatically by the RAM generators in GRLIB.

81.10.6 ASI 0x10, 0x11, 0x13, 0x18 - Flush

For historical reasons there are multiple ASIs that flush the cache in different ways.

Writing to ASI 0x10 will flush the entire instruction cache. If MMU is implemented in the core, both instruction and data cache will be flushed.

Writing to ASI 0x11 will flush the data cache only.

Writing to ASI 0x13 will flush the instruction cache and data cache. Only available when MMU is implemented.

Writing to ASI 0x18 and 0x03, which is available only if MMU is implemented, will flush both the MMU TLB, the I-cache, and the D-cache. This will block execution for a few cycles while the TLB is flushed and then continue asynchronously with the cache flushes continuing in the background.

81.10.7 ASI 0x19 and 0x04 - MMU registers

This ASI provides access to the MMU:s control and status registers. The following MMU registers are implemented:

*Table 1467.*MMU registers (ASI = 0x19)

Address	Register
0x000	MMU control register
0x100	Context pointer register
0x200	Context register
0x300	Fault status register
0x400	Fault address register

81.10.8 ASI 0x1C - MMU and cache bypass

Performing an access via ASI 0x1C will act as if MMU and cache were disabled. The address will not be translated and the cache will not be used or updated by the access.

81.10.9 ASI 0x1E - MMU physical/snoop tags diagnostic access

If the MMU has been configured to use separate snoop (physical) tags, they can be accessed via ASI 0x1E. This is primarily useful for RAM testing, and should not be performed during normal operation. This ASI is addressed the same way as the regular diagnostic ASI:s 0xC, 0xE, and the read/written data has the layout as shown below (example for a 1 KiB/way data cache):

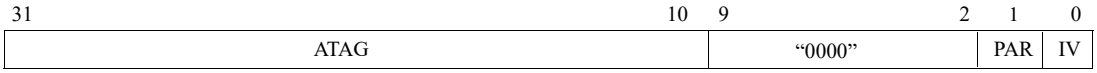


Figure 230. Snoop cache tag layout

[31:10] Address tag. The physical address tag of the cache line.
[1]: Parity. The odd parity over the data tag. Only used when processor is implemented with fault-tolerance features.
[0]: Invalid. When set, the cache line is not valid and will cause a cache miss if accessed by the processor. Only present if fast snooping is enabled.

81.11 Configuration registers

81.11.1 PSR, WIM, TBR registers

The %psr, %wim, %tbr registers are implemented as required by the SPARC V8 manual.

*Table 1468.*LEON4 Processor state register (%psr)

31 28	27 24	23 20	19 16
IMPL	VER	ICC	RESERVED
0xF	0x3	0	0
r	r	r	r

15 14	13	12	11 8	7	6	5	4 0
RESERVED	EC	EF	PIL	S	PS	ET	CWP
0	0	0	0	1	1	0	0
r	r	rw*	rw	rw	rw	rw	rw

31:28	Implementation ID (IMPL), read-only hardwired to “1111” (15)
27:24	Implementation version (VER), read-only hardwired to “0011” (3) for LEON3/LEON4.
23:20	Integer condition codes (ICC), see sparcv8 for details
19:14	Reserved
13	Enable coprocessor (EC), read-only if coprocessor not implemented
12	Enable floating-point (EF), read-only if FPU not implemented.
11:8	Processor interrupt level (PIL) - controls the lowest IRQ number that can generate a trap
7	Supervisor (S)
6	Previous supervisor (PS), see sparcv8 for details
5	Enable traps (ET)
4:0	Current window pointer

*Table 1469.*LEON4 Window invalid mask (%wim)

31 NWIN	NWIN-1 0
RESERVED	WIM
0	NR
r	rw

*Table 1470.*LEON4 Trap base address regsiter (%tbr)

31 12	11 4	3 0
TBA	TT	R
*	0	0
rw	rw	r

31:12	Trap base address (TBA) - Top 20 bits used for trap table address
11:4	Trap type (TT) - Last taken trap type. Read only.
3:0	Always zero, read only

81.11.2 ASR17, LEON4 configuration register

The ancillary state register 17 (%asr17) provides information on how various configuration options were set during synthesis. This can be used to enhance the performance of software, or to support enumeration in multi-processor systems. There are also a few bits that are writable to configure certain aspects of the processor.

*Table 1471.*LEON4 configuration register (%asr17)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INDEX				DBP	RES	DBPM	REXV		REXM		RESERVED			CS	CF[1]
*				0	0	0	*		*		0			*	*
r				rw	r	rw	r		rw*		r			r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CF[0]	DWT	SVT	LD	FPU		M	V8	NWP			NWIN				
*	*	0	0	*		*	*	*			*				
r	rw	rw*	r	r		r	r	r			r				

31:28 Processor index (INDEX) - In multi-processor systems, each LEON core gets a unique index to support enumeration. The value in this field is identical to the *hindex* VHDL generic parameter in the VHDL model.

27 Disable Branch Prediction (DBP) - Disables branch prediction when set to ‘1’. Default value is ‘0’.

26 Reserved for future implementations

25 Disable Branch Prediction on instruction cache misses (DBPM) - When set to ‘1’ this avoids instruction cache fetches (and possible MMU table walk) for predicted instructions that may be annullated. This feature is on by default (reset value ‘1’).

24:23 REX version (REXV) - read-only field that is set to ‘00’ if REX is not implemented, ‘01’ if REX is implemented, ‘10’ and ‘11’ values are reserved for future implementations

22:21 REX mode (REXM) - set to ‘00’ for REX enabled, ‘01’ for REX illegal and ‘10’ for REX transparent mode. Writable with reset value ‘01’ when REX support has been enabled

20:18 Reserved for future implementations

17 Clock switching enabled (CS). If set, switching between AHB and CPU frequency is available.

16:15 CPU clock frequency (CF). CPU core runs at (CF+1) times AHB frequency.

14 Disable write error trap (DWT). When set, a write error trap (tt = 0x2b) will be ignored. Set to zero after reset.

13 Single-vector trapping (SVT) enable. If set, will enable single-vector trapping. Fixed to zero if SVT is not implemented. Set to zero after reset.

12 Load delay. 1-cycle load delay i s used.

11:10 FPU option. “00” = no FPU; “01” = GRFPU; “11” = GRFPU-Lite

9 If set, the optional multiply-accumulate (MAC) instruction is available

8 If set, the SPARC V8 multiply and divide instructions are available

7:5 Number of implemented watchpoints (NWP) (0 - 4)

4:0 Number of implemented registers windows corresponds to NWIN+1.

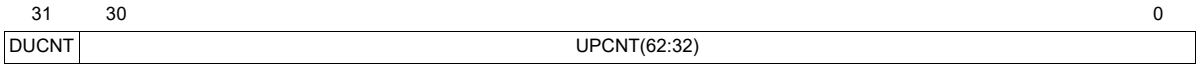
81.11.3 ASR22-23 - Up-counter

The ancillary state registers 22 and 23 (%asr22-23) contain an internal up-counter that can be read by software without causing any access on the on-chip AMBA bus. The number of available bits in the counter is implementation dependent and is decided by the number of counter bits in the DSU time tag counter. %ASR23 contains the least significant part of the counter value and %ASR22 contains the most significant part. In case the implementation does not contain a debug support unit connected to the processor then the up-counter is not available (value is always zero).

The time tag value accessible in these registers is the same time tag value used for the system's trace buffers (if implemented) and for all processors connected to the same debug support unit. The time tag counter will increment when any of the trace buffers is enabled, or when the time tag counter is forced to be enabled via the DSU register interface, or when any processor has its %ASR22 Disable Up-counter (DUCNT) field set to zero.

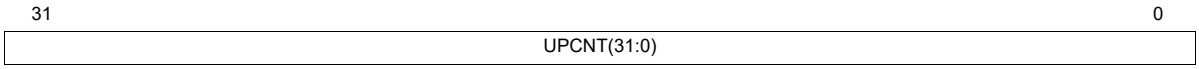
The up-counter value will increment even if all processors have entered power-down mode.

*Table 1472.*LEON4 up-counter MSbs (%ASR22)



31	Disable Up-counter (DUCNT) - Disable upcounter. When set to '1' the up-counter may be disabled. When cleared, the counter will increment each processor clock cycle. Default (reset) value is '1'.
30:0	Counter value (UPCNT(62:32)) - Most significant bits of internal up-counter. Read-only.

*Table 1473.*LEON4 up-counter LSbs (%ASR23)



31:0	Counter value (UPCNT(31:0)) - Least significant bits of internal up-counter. Read-only.

81.11.4 ASR24-31, Hardware watchpoint/breakpoint registers

Each breakpoint consists of a pair of ancillary state registers (%asr24/25, %asr26/27, %asr28/29 and %asr30/31) registers; one with the break address and one with a mask:

%asr24, %asr26
%asr28, %asr30

31	2	1	0
WADDR[31:2]			IF
NR		0	0
rw		r	rw

%asr25, %asr27
%asr29, %asr31

31	2		0
WMASK[31:2]		DL	DS
NR		0	0
rw		rw	rw

Figure 231. Watch-point registers

WADDR - Address to compare against

WMASK - Bit mask controlling which bits to check (1) or ignore (0) for match

IF - break on instruction fetch from the specified address/mask combination

DL - break on data load from the specified address/mask combination

DS - break on data store to the specified address/mask combination

Note: Setting IF=DL=DS=0 disables the breakpoint

When there is a hardware watchpoint match and DL or DS is set then trap 0x0B will be generated. Hardware watchpoints can be used with or without the LEON4 debug support unit (DSU) enabled.

81.11.5 Cache control register

The cache control register located at ASI 0x2, offset 0, contains control and status registers for the I and D cache.

*Table 1474.*LEON4 Cache Control Register (CCR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	STE	R	PS	TB				DS	FD	FI	FT		R	ST	R
0	*	0	*	0				0	0	0	*		0	*	0
r	rw*	r	rw*	rw*				rw	rw	rw	r		r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP	DP	ITE		IDE		DTE		DDE		DF	IF	DCS		ICS	
0	0	0		0		0		0		0	0	0		0	
r	r	rw*		rw*		rw*		rw*		rw*	rw*	rw		rw	

31	Reserved
30	Snoop Tag Flag (STE) - Set when parity error is detected in the data physical (snoop) tags. Only available if fault-tolerance is enabled (FT field in this register is non-zero).
29	Reserved
28	Parity Select (PS) - if set diagnostic read will return 4 check bits in the lsb bits, otherwise tag or data word is returned. Only available if fault-tolerance is enabled (FT field in this register is “01”).
27:24	Test Bits (TB) - if set, check bits will be xored with test bits TB during diagnostic write. Only available if fault-tolerance is enabled (FT field in this register is “01”).
23	Data cache snoop enable (DS) - if set, will enable data cache snooping.
22	Flush data cache (FD). If set, will flush the data cache. Always reads as zero.
21	Flush Instruction cache (FI). If set, will flush the instruction cache. Always reads as zero.
20:19	FT scheme (FT) - “00” = no FT, “01” = 4-bit checking implemented, “10” - Technology-specific protection implemented.
18	Reserved for future implementations
17	Separate snoop tags (ST). This read-only bit is set if separate physical/snoop tags are implemented.
16	Reserved
15	Instruction cache flush pending (IP). This bit is set when an instruction cache flush operation is in progress
14	Data cache flush pending (DP). This bit is set when an data cache flush operation is in progress.
13:12	Instruction Tag Errors (ITE) - Number of detected parity errors in the instruction tag cache. Only available if fault-tolerance is enabled (FT field in this register is non-zero).
11:10	Instruction Data Errors (IDE) - Number of detected parity errors in the instruction data cache. Only available if fault-tolerance is enabled (FT field in this register is non-zero).
9:8	Data Tag Errors (DTE) - Number of detected parity errors in the data tag cache. Only available if fault-tolerance is enabled (FT field in this register is non-zero).
7:6	Data Data Errors (DDE) - Number of detected parity errors in the data data cache. Only available if fault-tolerance is enabled (FT field in this register is non-zero).
5	Data Cache Freeze on Interrupt (DF) - If set, the data cache will automatically be frozen when an asynchronous interrupt is taken.
4	Instruction Cache Freeze on Interrupt (IF) - If set, the instruction cache will automatically be frozen when an asynchronous interrupt is taken.
3:2	Data Cache state (DCS) - Indicates the current data cache state according to the following: X0= disabled, 01 = frozen, 11 = enabled.
1:0	Instruction Cache state (ICS) - Indicates the current data cache state according to the following: X0= disabled, 01 = frozen, 11 = enabled.

81.11.6 I-cache and D-cache configuration registers

The configuration of the two caches if defined in two registers: the instruction and data configuration registers. These registers are read-only, except for the REPL field that may be writable, and indicate the size and configuration of the caches. They are located under ASI 2 at offset 8 and 12.

*Table 1475.*LEON4 Cache configuration register

31	30	29 28	27	26 25 24	23 22 21 20	19	18 17 16
CL	R	REPL	SN	WAYS	WSIZE	LR	LSIZE
0	0	*	*	*	*	0	*
r	r	r	r	r	r	r	r

15 14 13 12 11 10 9 8 7 6 5 4	3	2 1 0
RESERVED	M	RESERVED
0	*	0
r	r	r

31	Cache locking (CL). Set if cache locking is implemented (always zeo)
30:28	Cache replacement policy (REPL). 00 - no replacement policy (direct-mapped cache), 01 - least recently used (LRU), 10 - least recently replaced (LRR), 11 - random. This field is writable when LRU policy is implemented.
27	Cache snooping (SN). Set if snooping is implemented.
26:24	Cache associativity (WAYS). Number of ways in the cache: 000 - direct mapped, 001 - 2-way associative, 010 - 3-way associative, 011 - 4-way associative
23:20	Way size (WSIZE). Indicates the size (KiB) of each cache way. Size = 2^{SIZE}
19	Local ram (LR). Set if local scratch pad ram is implemented. (Always zero for LEON4)
18:16	Line size (LSIZE). Indicated the size (words) of each cache line. Line size = 2^{LSZ}
15:4	RESERVED
3	MMU present. This bit is set to ‘1’ if an MMU is present.
2	SO (supervisor only access) bit is present. This bit is set if *mmuen* generic is set to 2.
2:0	Reserved for future implementations

81.11.7 MMU control register

The MMU control register is located in ASI 0x19 offset 0, and the layout can be seen in table 1476.

*Table 1476.*LEON4 MMU control register

31 28	27 24	23 21	20 18	17 16
IMPL	VER	ITLB	DTLB	PSZ
0	1	*	*	0
r	r	r	r	rw*

15	14	13 2	1	0
TD	ST	RESERVED	NF	E
NR	0	0	0	0
rw*	r	r	rw	rw

31:28	MMU Implementation ID. Hardcoded to “0000”

*Table 1476.*LEON4 MMU control register

27:24	MMU Version ID. Hardcoded to “0001”.
23:21	Number of ITLB entries. The number of ITLB entries is calculated as 2^{ITLB}. If the TLB is shared between instructions and data, this field indicates to total number of TLBs.
20:18	Number of DTLB entries. The number of DTLB entries is calculated as 2^{DTLB}. If the TLB is shared between instructions and data, this field is zero.
17:16	Page size. The size of the smallest MMU page. 0 = 4 Kib; 1 = 8 Kib; 2 = 16 Kib; 3 = 32 Kib. If the page size is programmable, this field is writable, otherwise it is read-only.
15	TLB disable. When set to 1, the TLB will be disabled and each data access will generate an MMU page table walk. See Section 81.12.3 for detailed information.
14	Separate TLB. This bit is set to 1 if separate instruction and data TLBs are implemented
13	This bit only exists if *mmuen* generic is set to 2. This bit is written to the SO (supervisor only access) part of the TAG during diagnostic writes.
13:2	Reserved for future implementations
1	No Fault. When NF= 0, any fault detected by the MMU causes FSR and FAR to be updated and causes a fault to be generated to the processor. When NF= 1, a fault on an access to ASI 9 is handled as when NF= 0; a fault on an access to any other ASI causes FSR and FAR to be updated but no fault is generated to the processor.
0	Enable MMU. 0 = MMU disabled, 1 = MMU enabled.

81.11.8 MMU context pointer and context registers

The MMU context pointer register is located in ASI 0x19 offset 0x100 and the MMU context register is located in ASI 0x19 offset 0x200. They together determine the location of the root page table descriptor for the current context. Their definition follows the SRMMU specification in the SPARC V8 manual with layouts shown below..

*Table 1477.*LEON4 MMU context pointer register

31 2	1	0
CONTEXT TABLE POINTER	RES	
NR	0	
rw	r	

31:2	Context table pointer, physical address bits 35:6 (note address is shifted 4 bits)
1:0	Reserved, always 0

*Table 1478.*LEON4 MMU context register

31 8	7 0
RESERVED	CONTEXT
0	0
r	rw

31:8	Reserved
7:0	Current context ID

In the LEON4, the context bits are OR:ed with the lower MMU context pointer bits when calculating the address, so one can use less context bits to reduce the size/alignment requirements for the context table.

81.11.9 MMU fault status register

The MMU fault status register is located in ASI 0x19 offset 0x300, and the definition is based on the SRMMU specification in the SPARC V8 manual. The SPARC V8 specifies that the fault status regis-

ter should be cleared on read, on the LEON4 only the FAV bit is cleared on read. The FAV bit is always set on error in the LEON4 implementation, so it can be used as a valid bit for the other fields..

*Table 1479.*LEON4 MMU fault status register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED														EBE	
0														0	
r														r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EBE						L		AT			FT			FAV	OW
0						0		0			0			0	0
r						r		r			r			r	r

31:18	Reserved
17:10	External bus error (EBE) - Never set on the LEON3
9:8	Level (L) - Level of page table entry causing the fault
7:5	Access type (AT) - See V8 manual
4:2	Fault type (FT) - See table 1459
1	Fault address valid (FAV) - Cleared on read, always written to 1 on fault
0	Overwrite (W) - Multiple faults of the same priority encountered

81.11.10MMU fault address register

The MMU fault address register is located in ASI 0x19 offset 0x400, and the definition follows the SRMMU specification in the SPARC V8 manual..

*Table 1480.*LEON4 MMU fault address register

31 12	11 0
FAULT ADDRESS	RESERVED
NR	0
r	r

31:12	Top bits of virtual address causing translation fault
11:0	Reserved, always 0

81.12 Software considerations

81.12.1 Register file initialization on power up

It is recommended that the boot code for the processor writes all registers in the IU and FPU register files before launching the main application. This allows software to be portable to both FT and non-FT versions of the LEON3 and LEON4 processors.

81.12.2 Start-up

After reset, the caches are disabled and the cache control register (CCR) is 0. Before the caches may be enabled, a flush operation must be performed to initialized (clear) the tags and valid bits. A suitable assembly sequence could be:

```
flush
set 0x81000f, %g1
sta %g1, [%g0] 2
```

81.12.3 MMU & TLB

After reset, the MMU is disabled and TLB is configured to be on (will not have any effect until MMU is enabled). Hence with default reset values the TLB has to be flushed before the MMU is being activated to initialize the valid bits in TLB. If the TLB is disabled while the MMU is active, the TLB must be flushed before enabled again.

81.12.4 Data scrubbing (for fault-tolerant implementations)

There is generally no need to perform data scrubbing on either IU/FPU register files or the cache memory. During normal operation, the active part of the IU/FPU register files will be flushed to memory on each task switch. This will cause all registers to be checked and corrected if necessary. Since most real-time operating systems performs several task switches per second, the data in the register files will be frequently refreshed.

The similar situation arises for the cache memory. In most applications, the cache memory is significantly smaller than the full application image, and the cache contents is gradually replaced as part of normal operation. For very small programs, the only risk of error build-up is if a part of the application is resident in the cache but not executed for a long period of time. In such cases, executing a cache flush instruction periodically (e.g. once per minute) is sufficient to refresh the cache contents.

81.13 Vendor and device identifiers

The core has vendor identifiers 0x01 (Cobham Gaisler) and device identifiers 0x048. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

81.14 Implementation

81.14.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers, except synchronization registers, if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core will use asynchronous reset for all registers, except synchronization registers, if the GRLIB config package setting *grlib_async_reset_enable* is set.

81.14.2 Technology mapping

LEON4 has two technology mapping VHDL generics, *fabtech* and *memtech*. The *fabtech* generic controls the implementation of some pipeline features, while *memtech* selects which memory blocks will be used to implement cache memories and the IU/FPU register file. *Fabtech* can be set to any of the provided technologies (0 - NTECH) as defined in the TECHMAP.GENCOMP package. See the GRLIB Users's Manual for available settings for *memtech*.

81.14.3 RAM usage

The LEON4 core maps all usage of RAM memory on the *syncram*, *syncram_2p* and *syncram_dp* components from the technology mapping library (TECHMAP). The type, configuration and number of RAM blocks is described below.

Register file

The register file is implemented with six *synram_2p* blocks for all technologies where the *regfile_4p_infer* constant in TECHMAP.GENCOMP is set to 0. The organization of the syncram_2p is shown in the following table:

*Table 1481.*syncram_2p sizes for LEON4 register file

Register windows	Syncram_2p organization
2 - 3	32x32
4 - 7	64x32
8 - 15	128x32
16-31	256x31
32	512x32

If *regfile_4p_infer* is set to 1, the synthesis tool will automatically infer the register. On FPGA technologies, it can be in either flip-flops or RAM cells, depending on the tool and technology. On ASIC technologies, it will be flip-flops. The amount of flip-flops inferred is equal to the number of registers:

Number of flip-flops = ((NWINDOWS *16) + 8) * 32

FP register file

If FPU support is enabled, the FP register file is implemented with four *synram_2p* blocks when the *regfile_3p_infer* constant in TECHMAP.GENCOMP is set to 0. The organization of the syncram_2p blocks is 16x32.

If *regfile_3p_infer* is set to 1, the synthesis tool will automatically infer the FP register file. For ASIC technologies the number of inferred flip-flops is equal to number of bits in the FP register file which is 32 * 32 = 1024.

Cache memories

RAM blocks are used to implement the cache tags and data memories. Depending on cache configuration, different types and sizes of RAM blocks are used.

The tag memory is implemented with one *syncram* per cache way when no snooping is enabled. The tag memory depth and width is calculated as follows:

Depth = (cache way size in bytes) / (cache line size in bytes)

Width = 32 - log2(cache way size in bytes) + 1

For a 2 KiB cache way with 32 bytes/line, the tag RAM depth will be (2048/32) = 64. The width will be: 32 - log2(2048) + 1 = 32 - 11 + 1 = 22. The tag RAM organization will thus be 64x22 for the configuration. If the MMU is enabled, the tag memory width will increase with 8 to store the process context ID, and the above configuration will us a 64x30 RAM.

If simple (MMU-less) snooping is enabled, the data cache tag memory will instead of single-port RAM blocks be implemented with a dual-port RAMs (syncram_dp) of the same size.

If physical (MMU-compatible) snooping is enabled, the data cache tag memories will be implemented using two *syncram_2p* components (with one read-only and one write-only port) per way, one memory for virtual and one for separate physical tags. The size of the virtual tag block will be the same as when snooping is disabled. The physical tag block will have the same depth as above and the data width corresponds to the width of the tag: 32 - log2(way size). A 4 KiB data cache way will thus require a 32 - 12 = 20 bit wide RAM block for the physical tags.

The data part of the caches (storing instructions or data) is either 64 or 128 bit wide, depending on the setting of the *busw* VHDL generic. The depth is equal to the way size in bytes, divided by 8 (BUSW=64) or 16 (BUSW=128). A 64-bit cache way of 4 KiB will use two *syncram* components with and organization of 512x32. If the 128-bit AHB bus option is used, the data RAM will be divided on four 32-bit RAM blocks to allow loading of a 16-bit cache line in one clock. A 4 KiB data cache will then use four 256x32 RAM blocks.

Instruction Trace buffer

The instruction trace buffer will use four identical RAM blocks (*syncram*) to implement the buffer memory. The syncrams will always be 32-bit wide. The depth will depend on the *tbuf* VHDL generic, which indicates the total size of trace buffer in KiBs. If *tbuf* = 1 (1 KiB), then four RAM blocks of 64x32 will be used. If *tbuf* = 2, then the RAM blocks will be 128x32 and so on.

81.14.4 Double clocking

LEON4 implements double clocking in the same way as LEON3. Please refer to the LEON3 Double-Clocking section in the LEON/GRLIB Configuration and Development Guide.

81.14.5 Clock gating

LEON4 clock gating is described in the LEON/GRLIB Configuration and Development Guide.

81.14.6 Scan support

If the *scantest* VHDL generic is set to 1, support for scan testing is enabled. This will make use of the AHB scan support signals in the following manner: when AHBI.testen and AHBI.scanen are both '1', the select signals to all RAM blocks (cache RAM, register file and DSU trace buffers) are disabled. This means that when the scan chain is shifted, no accidental write or read can occur in the RAM blocks. The scan signal AHBI.testrst is not used as there are no asynchronous resets in the LEON4 core.

81.15 Configuration options

Table 1482 shows the configuration options of the core (VHDL generics).

*Table 1482.*Configuration options

Generic	Function	Allowed range	Default
hindex	AHB master index	0 - NAHBMST-1	0
fabtech	Target technology	0 - NTECH	0 (inferred)
memtech	Vendor library for regfile and cache RAMs. Bits 16, 17 and 18 of this generic can be used to for the MMU TLB data RAM, IU register file and FP register file to inferred technology: + 2**16: Force inferred technology for MMU TLB data RAM + 2**17: Force inferred technology for IU register file + 2**18: Force inferred technology for FP register file Adding the value (2**17) is equivalent to setting the grlib.gencomp.regfile_4p_infer(memtech) to 1 (used for some technologies to force the register file implementations to inferred). Adding the value (2**18) is equivalent to setting the grlib.gencomp.regfile_3p_infer(memtech) to 1 (used for some technologies to force the register file implementations to inferred).	0 - 16#FFFFFFFF#	0 (inferred)
nwindows	Number of SPARC register windows. Choose 8 windows to be compatible with Bare-C and RTEMS cross-compilers.	2 - 32	8
dsu	Enable Debug Support Unit interface	0 - 1	0
fpu	Floating-point Unit 0 : no FPU 1 - 7: GRFPU 1 - inferred multiplier, 2 - DW multiplier, 3 - Module Generator multiplier 8 - 14: GRFPU-Lite 8 - simple FPC, 9 - data forwarding FPC, 10 - non-blocking FPC 16 - 31: as above (modulo 16) but use netlist 32 - 63: as above (modulo 32) but uses shared GRFPU interface	0 - 63	0

*Table 1482.*Configuration options

Generic	Function	Allowed range	Default
v8	Generate SPARC V8 MUL and DIV instructions This generic is assigned with the value: *mult + 4*struct* Where mult selects between the following implementation options for the multiplier and divider: 0 : No multiplier or divider 1 : 16x16 multiplier 2 : 16x16 pipelined multiplier 16#32# : 32x32 pipelined multiplier Where *struct* selects the structure option for the integer multiplier. The following structures can be selected: 0: Inferred by synthesis tool 1: Generated using Module Generators from NTNU 2: Using technology specific netlists (techspec). Only supported for RTAX-D FPGAs. Other technologies will assert a simulation error. 3: Using Synopsys DesignWare (DW02_mult and DW_mult_pipe)	0 - 16#3F#	0
cp	Generate co-processor interface	0 -1	0
mac	Generate SPARC V8e SMAC/UMAC instruction. Can only be used together with a 16x16 multiplier.	0 - 1	0
pclow	Least significant bit of PC (Program Counter) that is actually generated. PC[1:0] are always zero and are normally not generated. Generating PC[1:0] makes VHDL-debugging easier.	0, 2	2
notag	Disable tagged instructions.	0 - 1	0
nwp	Number of watchpoints	0 - 4	0
icen	Enable instruction cache	0 - 1	1
irepl	Instruction cache replacement policy. 0 - least recently used (LRU)/LRR/random/direct, 2 - random only	0, 2	0
isets	Number of instruction cache ways	1 - 4	1
ilinesize	Instruction cache line size in number of words	4, 8	4
isetsize	Size of each instruction cache way in KiB	1 - 256	1
isetlock	Unused	0 - 1	0
dcen	Data cache enable	0 - 1	1
drepl	Data cache replacement policy. 0 - least recently used (LRU)/LRR/random/direct, 2 - random only	0, 2	0
dsets	Number of data cache ways	1 - 4	1
dlinesize	Data cache line size in number of words	4, 8	4
dsetsize	Size of each data cache way in KiB Note: If the processor is implemented with the MMU then the cache way size needs to be equal or less then the MMU page size for hardware cache coherency.	1 - 256	1
dsetlock	Unused	0 - 1	0
dsnoop	Enable data cache snooping Bit 0-1: 0: disable, 1: obsolete, 2: enable Bit 2: 0: simple (no-MMU) snooping, 1: separate physical tags	0 - 6	0
ilram	Enable local instruction RAM (not used at this point)	0 - 1	0
ilramsize	Local instruction RAM size in kB (not used at this point)	1 - 512	1

*Table 1482.*Configuration options

Generic	Function	Allowed range	Default
ilramstart	8 MSB bits used to decode local instruction RAM area (not used at this point)	0 - 255	16#8E#
dlram	Enable local data RAM (scratch-pad RAM) (not used at this point)	0 - 1	0
dlramsize	Local data RAM size in kB (not used at this point)	1 - 512	1
dlramstart	8 MSB bits used to decode local data RAM area (not used at this point)	0 - 255	16#8F#
mmuen	Enable memory management unit (MMU) Note: Bus snooping is required to avoid cache aliasing effects when the MMU is enabled if the cache has more than one way. 0 : MMU does not exist. 1 : MMU exists. 2 : MMU exists and the cache tags include an additional bit called SO (supervisor only access). See sec. 81.4.2 for more details. If MMU is going to be instantiated in the processor, it is recommended to set the *mmuen* generic to 2.	0 - 2	0
itlbnum	Number of instruction TLB entries	2 - 64	8
dtlbnum	Number of data TLB entries	2 - 64	8
tlb_type	0 : separate TLB with slow write 1: shared TLB with slow write 2: separate TLB with fast write	0 - 2	1
tlb_rep	LRU (0) or Random (1) TLB replacement	0 - 1	0
lddel	Unused. LEON4 is always implemented with load delay 1.	1 - 2	2
disas	Print instruction disassembly in VHDL simulator console.	0 - 1	0
tbuf	Size of instruction trace buffer in kB (0 - instruction trace disabled). For values 1-64 a single-port trace buffer of size *tbuf* is used. For values 65-128 a two-port trace buffer of size *tbuf*-64 is used.	0 - 128	0
pwd	Power-down. 0 - disabled, 1 - area efficient, 2 - timing efficient.	0 - 2	1
svt	Enable single-vector trapping	0 - 1	0
rstaddr	Default reset start address. This generic sets the 20 most significant bits of the reset address. The reset address must always be aligned on a 4 KiB address boundary. If this generic is set to 16#fffff# the processor will read its start address from the interrupt controller interface signal IRQI.RSTVEC (dynamic reset start address). See section 81.2.18 for more information.	0 - (2**^{20}-1)	0
smp	Enable multi-processor support 0: SMP support disabled 1- 15: SMP enabled, cpu index is taken from hindex generic 16-31: SMP enabled, cpu index is taken from irqi.index signal	0 - 31	0
cached	Fixed cacheability mask. See sections 81.3 and 81.7 for more information.	0 - 16#FFFF#	0
clk2x	Enables double-clocking. See section 81.14.4 and the LEON/GRLIB Design and Configuration Guide. Not present on all top-level entites.	0 - 15	0
scantest	Enable scan test support	0 - 1	0

*Table 1482.*Configuration options

Generic	Function	Allowed range	Default
wbmask	Wide-bus mask. Indicates which address ranges are 64/128 bit capable. Treated as a 16-bit vector with LSB bit (right-most) indicating address 0 - 0x10000000. See section 81.7 for more information.	0 - 16#FFFF#	0
busw	Bus width of the wide bus area (64 or 128). See section 81.7 for more information.	64, 128	64
netlist	Use technology specific netlist	0 - 1	0
ft	Register file and cache memory protection, bitfield Bit 10:7: Selects technology specific protection cache protection. 0 to disable, 5 to enable. Bit 6:4: Unused Bit 3: enable cache memory parity protection Bit 2:0 Register file SEU protection. (0: no protection; 4: TMR, 6: Tech-specific)	0 - 2047	0
npasi	Enable SPARC V8E nonprivileged ASI access. 0 - All accesses to alternate address space are privileged. 1 - LOAD and STORE from alternate space instructions accessing ASIs 0x00-0x7F are privileged, ASIs 0x80 - 0xFF are nonprivileged.	0 - 1	0
pwrpsr	Enable SPARC V8E partial write PSR (WRPSR).	0 - 1	0
ahbpipe	Add pipeline registers to AHB read data vectors. Only has effect for *busw* = 128. Setting only present on leon4x entity.	0 - 1	0
rex	Enable LEON-REX extension	0 - 1	0
mmupgsz	MMU Page size. 0 = 4K, 1 = 8K, 2 = 16K, 3 = 32K, 4 = programmable.	0 - 4	0

81.16 Signal descriptions

Table 1483 shows the interface signals of the core (VHDL ports). Note that there are several top-level entities available for the LEON4 processor: *leon4x, leon4s, leon4sh, leon4s2x, leon4ft* and *leon4cg*. The *leon4x* entity exposes all signals and settings. The other entities are wrapper around *leon4x*.

*Table 1483.*Signal descriptions

Signal name	Field	Type	Function	Active
leon4x:AHBCLK leon4s2x:CLK	N/A	Input	AMBA clock in 2x mode Note that this only applies to the processor entities listed.	-
leon4x:CPUCLK leon4s: CLK leon4sh: CLK leon4s2x: CLK2 leon4ft: CLK leon4cg: CLK	N/A	Input	Processor clock, can be gated. Note that this clock has different names depending on which top-level entity that is used to instantiate the processor. For example, LEON4S only has one clock input which covers three of the rows in this table (Processor clock, FPU-clock, free running processor clock).	-
leon4x:GCPUCLK leon4s: CLK leon4sh: CLK leon4s2x: GCLK2 leon4ft: GCLK leon4cg: GCLK	N/A	Input	Free running processor clock. Note that this clock has different names depending on which top-level entity that is used to instantiate the processor. For example, LEON4S only has one clock input which covers three of the rows in this table (Processor clock, FPU-clock, free running processor clock).	-

*Table 1483.*Signal descriptions

Signal name	Field	Type	Function	Active
leon4x:FPUCLK leon4s: CLK leon4sh: CLK leon4s2x: GCLK2 leon4ft: GCLK leon4cg: GCLK	N/A	Input	FPU clock, can be gated. Note that this clock has different names depending on which top-level entity that is used to instantiate the processor. For example, LEON4S only has one clock input which covers three of the rows in this table (Processor clock, FPU-clock, free running processor clock).	-
RSTN	N/A	Input	Reset	Low
AHBI	*	Input	AHB master input signals	-
AHBO	*	Output	AHB master output signals	-
AHBSI	*	Input	AHB slave input signals	-
AHBSO[]	*	Input	AHB slave output signals from all slaves on same bus. The processor makes use of the plug&play sideband signals to decode cacheability information of the bus. This can be overridden by the cached VHDL generic.	-
IRQI	IRL[3:0]	Input	Interrupt level	High
	RESUME	Input	Reset power-down and error mode	High
	RSTRUN	Input	Start after reset (SMP system only)	High
	RSTVEC[31:12]	Input	Reset start addr. (SMP and dynamic reset addr.)	-
	INDEX[3:0]	Input	CPU index when SMP = 2	-
	PWDSETADDR	Input	In power-down/error mode, shift PC to nPC and set PWDNEWADDR to PC.	High
	PWDNEWADDR [31:2]	Input	New PC value used with PWDSETADDR	-
	FORCEERR	Input	Force CPU into error mode	High
IRQO	INTACK	Output	Interrupt acknowledge	High
	IRL[3:0]	Output	Processor interrupt level	High
	PWD	Output	Processor in power-down mode	High
	FPEN	Output	Floating-point unit enabled	High
	ERR	Output	Processor in error mode	High
DBGI	-	Input	Debug inputs from DSU	-
DBGO	-	Output	Debug outputs to DSU	-
	ERROR		Processor in error mode, execution halted	Low
GCLK		Input	Gated processor clock for LEON4cg	

* see GRLIB IP Library User's Manual

81.17 Signal definitions and reset values

When the processor enters error mode, the *errorn* output is driven active.

The signals and their reset values are described in table 1484.

*Table 1484.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
errorn	Tri-state output	Processor error mode indicator	Low	Tri-state

81.18 Timing

The timing waveforms and timing parameters are shown in figure 232 and are defined in table 1485.

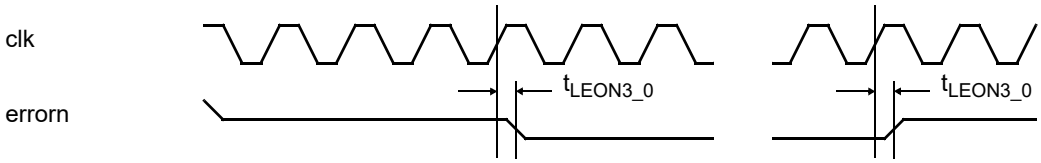


Figure 232. Timing waveforms

*Table 1485.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{LEON3_0}	clock to output delay	rising *clk* edge	TBD	TBD	ns

81.19 Library dependencies

Table 1486 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1486.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AHB signal definitions
GAISLER	LEON3, LEON4	Component, signals	LEON4 component declaration, interrupt and debug signals declaration

81.20 Component declaration

The LEON4 core has the following component declaration. There are also LEON4 top-levels that support clock gating (leon4cg), double-clocking (leon4s2x), shared FPU (leon4sh) and all available interfaces (leon4x). See the GRLIB template designs for instantiation examples.

```
entity leon4s is
  generic (
    hindex    : integer                := 0;
    fabtech   : integer range 0 to NTECH  := DEFFABTECH;
    memtech   : integer range 0 to NTECH  := DEFMEMTECH;
    nwindows  : integer range 2 to 32 := 8;
    dsu       : integer range 0 to 1  := 0;
    fpu       : integer range 0 to 31 := 0;
    v8        : integer range 0 to 63 := 0;
    cp        : integer range 0 to 1  := 0;
    mac       : integer range 0 to 1  := 0;
    pclow     : integer range 0 to 2  := 2;
    notag     : integer range 0 to 1  := 0;
    nwp       : integer range 0 to 4  := 0;
    icen      : integer range 0 to 1  := 0;
    irepl     : integer range 0 to 2  := 2;
    isets     : integer range 1 to 4  := 1;
    ilinesize : integer range 4 to 8  := 4;
    isetsize  : integer range 1 to 256 := 1;
    isetlock  : integer range 0 to 1  := 0;
    dcen      : integer range 0 to 1  := 0;
    drepl     : integer range 0 to 2  := 2;
    dsets     : integer range 1 to 4  := 1;
    dlinesize : integer range 4 to 8  := 4;
    dsetsize  : integer range 1 to 256 := 1;
    dsetlock  : integer range 0 to 1  := 0;
    dsnoop    : integer range 0 to 6  := 0;
    ilram      : integer range 0 to 1 := 0;
    ilramsize  : integer range 1 to 512 := 1;
    ilramstart : integer range 0 to 255 := 16#8e#;
    dlram      : integer range 0 to 1 := 0;
    dlramsize  : integer range 1 to 512 := 1;
    dlramstart : integer range 0 to 255 := 16#8f#;
    mmuen     : integer range 0 to 2 := 0;
    itlbnum   : integer range 2 to 64 := 8;
    dtlbnum   : integer range 2 to 64 := 8;
    tlb_type  : integer range 0 to 3  := 1;
    tlb_rep   : integer range 0 to 1  := 0;
    lddel     : integer range 1 to 2  := 2;
    disas     : integer range 0 to 2  := 0;
    tbuf      : integer range 0 to 64 := 0;
    pwd       : integer range 0 to 2  := 2;     -- power-down
    svt       : integer range 0 to 1  := 1;     -- single vector trapping
    rstaddr   : integer               := 0;
    smp       : integer range 0 to 15 := 0;     -- support SMP systems
    cached    : integer               := 0;     -- cacheability table
    scantest  : integer               := 0;
    wbmask    : integer               := 0;     -- Wide-bus mask
    busw      : integer               := 64;    -- AHB/Cache data width (64/128)
    ft        : integer               := 0
);
  port (
    clk    : in  std_ulogic;
    rstn   : in  std_ulogic;
    ahbi   : in  ahb_mst_in_type;
    ahbo   : out ahb_mst_out_type;
    ahbsi  : in  ahb_slv_in_type;
    ahbso  : in  ahb_slv_out_vector;
    irqi   : in  l3_irq_in_type;
    irqo   : out l3_irq_out_type;
    dbgi   : in  l3_debug_in_type;
    dbgo   : out l3_debug_out_type
  );
end;
```

82 LOGAN - On-chip Logic Analyzer

82.1 Introduction

The LOGAN core implements an on-chip logic analyzer for tracing and displaying of on-chip signals. LOGAN consists of a circular trace buffer and a triggering module. When armed, the logic analyzers stores the traced signals in the circular buffer until a trigger condition occurs. A trigger condition will freeze the buffer, and the traced data can then be read out via an APB interface.

The depth and width of the trace buffer is configurable through VHDL generics, as well as the number of trigger levels.

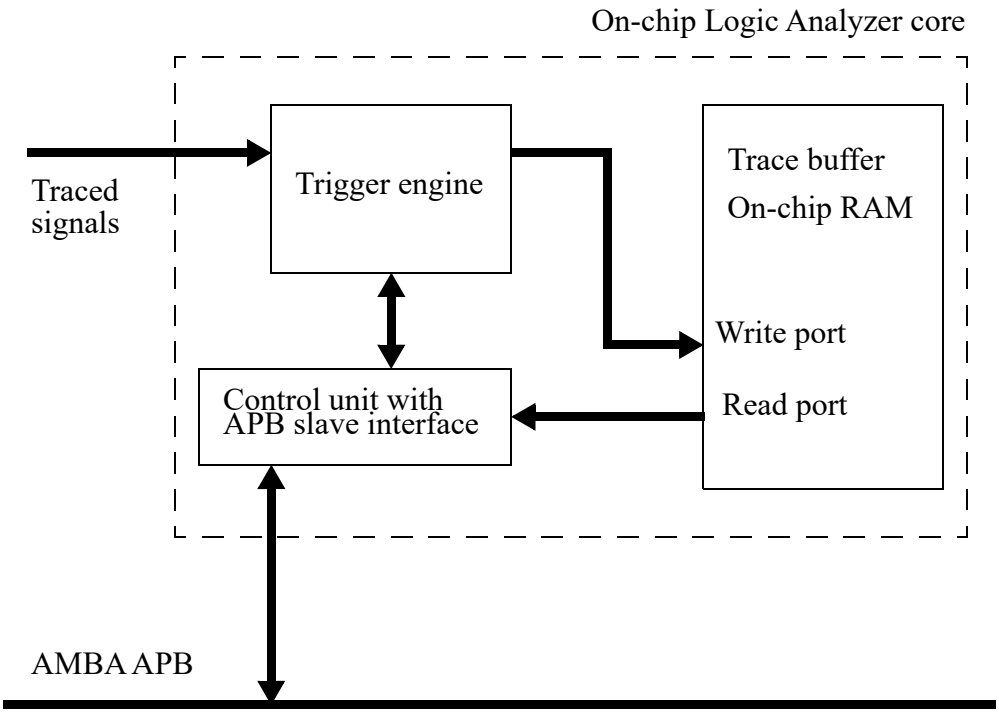


Figure 233. On-chip Logic Analyzer block diagram

82.2 Operation

82.2.1 Trace buffer

When the logic analyzer is armed, the traced signals are sampled and stored to the trace buffer on the rising edge of the sample clock (TCLK). The trace buffer consists of a circular buffer with an index register pointing to the next address in the buffer to be written. The index register is automatically incremented after each store operation to the buffer.

82.2.2 Clocking

LOGAN uses two clocks: TCLK and the APB clock. The trace signals are sampled on the rising edge of the sample clock (TCLK), while the control unit and the APB interface use the APB clock. TCLK and the APB clock does not need to be synchronized or have the same frequency.

82.2.3 Triggering

The logic analyzer contains a configurable number of trig levels. Each trig level is associated with a pattern and a mask. The traced signals are compared with the pattern, only comparing the bits set in the mask. This allows for triggering on any specific value or range. Furthermore each level has a match counter and a boolean equality flag. The equality flag specifies whether a match means that the pattern should equal the traced signals or that it should not be equal. It is possible to configure the trigger engine to stay at a certain level while the traced signals have a certain value using this flag. The match counter is a 6 bit counter which can be used to specify how many times a level should match before proceeding to the next. This is all run-time configurable through registers described in the register section.

To specify post-, center- or pre-triggering mode, the user can set a counter register that controls when the sampling stops relative to the triggering event. It can be set to any value in the range 0 to *depth*-1 thus giving total control of the trace buffer content.

To support the tracing of slowly changing signals, the logic analyzer has a 16-bit sample frequency divider register that controls how often the signals are sampled. The default divider value of 1 will sample the signals every clock cycle.

The *usequal* configuration option has a similar purpose as the sample frequency divider. The user can define one of the traced signals as a qualifier bit that has to have a specified value for the current signals to be stored in the trace buffer. This makes sampling of larger time periods possible if only some easily distinguished samples are interesting. This option has to be enabled with the *usequal* generic and the qualifier bit and value are written to a register.

82.2.4 Arming

To start operation, the logic analyzer needs to be armed. This is done by writing to the status register with bit 0 set to 1. A reset can be performed anytime by writing zero to the status register. After the final triggering event, the trigged flag will be raised and can be read out from the status register. The logic analyzer remains armed and trigged until the trigger counter reaches zero. When this happens the index of the oldest sample can be read from the trace buffer index register.

82.3 Registers

Both trace data and all registers are accessed through an APB interface. The LOGAN core will allocate a 64 kbyte block in the APB address space.

*Table 1487.*APB address mapping

APB address offset	Registers
0x0000	Status register
0x0004	Trace buffer index
0x0008	Page register
0x000C	Trig counter
0x0010	Sample freq. divider
0x0014	Storage qualifier setting
0x2000 - 0x20FF	Trig control settings
0x6000 - 0x6FFF	Pattern/mask configuration
0x8000 - 0xFFFF	Trace data

82.3.1 Status register

Table 1488. 0x0000 - STAT - Status register

31	30	29	28	27 20	19 6	5 0
usereg	qualifier	armed	trigged	dbits	depth	trig levels
*	*	0	0	*	*	*
r	r	rw	rw	r	r	r

31: 28 These bits indicate whether an input register and/or storage qualifier is used and if the Logic Analyzer is armed and/or trigged.

27: 20 Number of traced signals (Read Only).

19: 6 Last index of trace buffer. Depth-1 (Read Only).

5: 0 Number of trig levels (Read Only).

82.3.2 Trace buffer index

Table 1489. 0x0004 - INDEX - Trace buffer index register

31 abits	abits-1 0
RESERVED	the index of the oldest sample
0	0
r	r

31: *abits* Reserved.

abits-1:0 The index of the oldest sample in the buffer. The trace buffer index simply points to where a new sample will be written , in a circular buffer it is the oldest sample if it was previously written. *abits* is the number of bits needed to represent the configured depth.

Note that this register is written by the trigger engine clock domain and thus needs to be known stable when read out. Only when the ‘armed’ bit in the status register is zero is the content of this register reliable.

82.3.3 Page register

Table 1490. 0x0008 - PAGE - Trace buffer index register

31 4	3 0
RESERVED	current page
0	0
r	rw

31: 4 Reserved.

3: 0 This register selects what page that will be used when reading from the trace buffer.

The trace buffer is organized into pages of 1024 samples. Each sample can be between 1 and 256 bits. If the depth of the buffer is more than 1024 the page register has to be used to access the other pages. To access the i:th page the register should be set i (where i=0..15).

82.3.4 Trig counter

Table 1491. 0x000C - TRIGC - Trig counter register

31 abits	abits-1 0
RESERVED	trig counter value
0	0
r	rw

31:abits Reserved.

nbits-1:0 Trig counter value. A counter is incremented by one for each stored sample after the final triggering event and when it reaches the value stored in this register the sampling stops. 0 means posttrig and *depth-1* is pretrig. Any value in between can be used.

82.3.5 Sample frequency divider

*Table 1492.*0x0010 - CLKDIV - Sample freq. divider register

31 16	15 0
RESERVED	divider value
0	0x0001
r	rw

31: 16 Reserved.

15: 0 A sample is stored on every i:th clock cycle where i is specified through this register. This resets to 1 thus sampling occurs every cycle if not changed.

82.3.6 Storage qualifier

*Table 1493.*0x0014 - SQUAL - Storage qualifier register

31 9	8	7 0
RESERVED	val	qualifier
0	0	0
r	rw	rw

31: 9 Reserved.

8: Qualify storage if bit is 1/0.

7: 0 Which bit to use as qualifier.

82.3.7 Trig control registers

This memory area contains the registers that control when the trigger engine shall proceed to the next level, i.e the match counter and a one bit field that specifies if it should trig on equality or inequality. There are *trigl* words where each word is used like in the figure below.

Table 1494. 0x2000-0x20FF - TCTRL - Trigger control register

31 7	6 1	0
RESERVED	match counter	eq
0	NR	nr
r	rw	rw

31: 7 Reserved.

6: 1 Match counter. A counter is increased with one on each match on the current level and when it reaches the value stored in this register the trigger engine proceeds to the next level or if it is the last level it raises the trigged flag and starts the count of the trigger counter.

0: Specifies if a match is that the pattern/mask combination is equal or inequal compared to the traced signals. 1 - equal

0- inequal.

82.3.8 Pattern/mask configuration

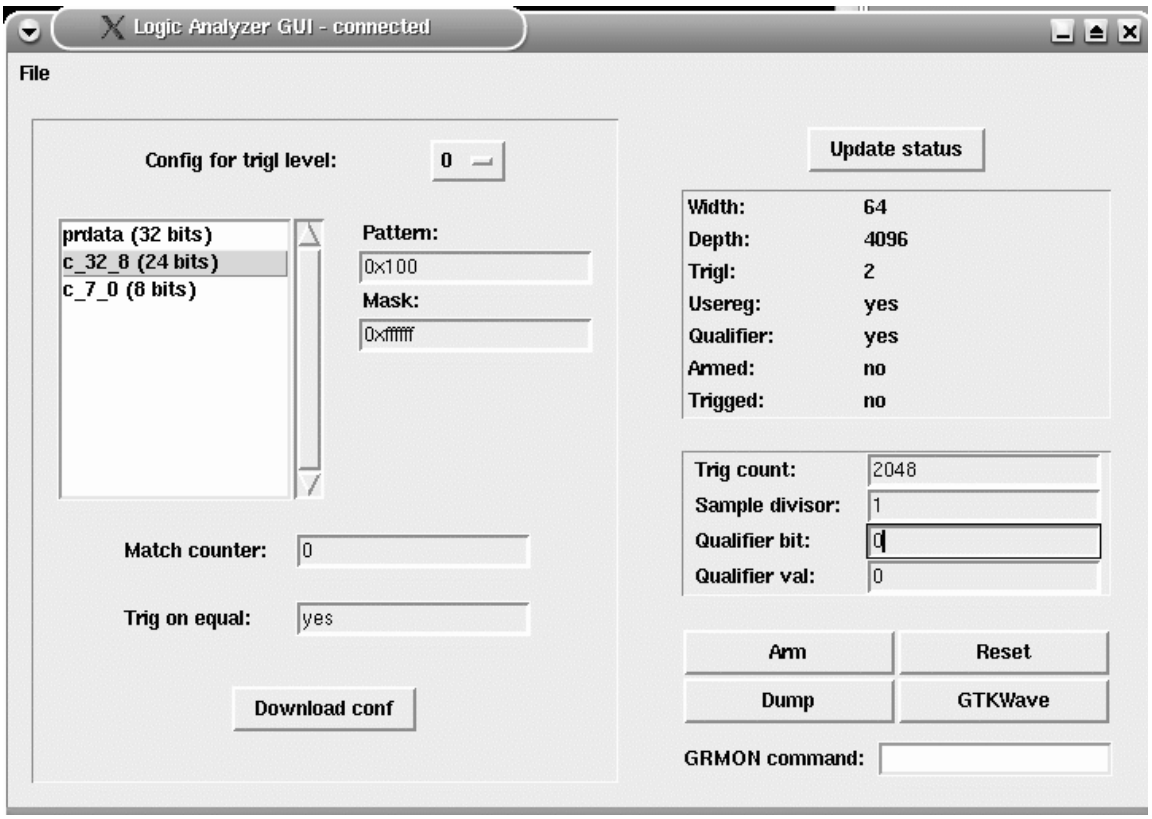
In these registers the pattern and mask for each trig level is configured. The pattern and mask can contain up to 8 words (256 bits) each so a number of writes can be necessary to specify just one pattern. They are stored with the LSB at the lowest address. The pattern of the first trig level is at 0x6000 and the mask is located 8 words later at 0x6020. Then the next trig levels starts at address 0x6040 and so on.

82.3.9 Trace data

It is placed in the upper half of the allocated APB address range. If the configuration needs more than the allocated 32 kB of the APB range the page register is used to page into the trace buffer. Each stored word is *dbits* wide but 8 words of the memory range is always allocated so the entries in the trace buffer are found at multiples of 0x20, i.e. 0x8000, 0x8020 and so on.

82.4 Graphical interface

The logic analyzer is normally controlled by the LOGAN debug driver in GRMON. It is also possible to control the LOGAN operation using a graphical user interface (GUI) written in Tcl/Tk. The GUI is provided with GRMON, refer to the GRMON manual for more details.



82.5 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x062. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

82.6 Implementation

82.6.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

82.7 Configuration options

Table 1495 shows the configuration options of the core (VHDL generics).

*Table 1495.*Configuration options

Generic	Function	Allowed range	Default
dbits	Number of traced signals	1 - 255	32
depth	Number of stored samples	256 - 16384	1024
trigl	Number of trigger levels	1 - 63	1
usereg	Use input register	0 - 1	1
usequal	Use storage qualifier	0 - 1	0
pindex	APB slave index	0 - NAPBSLV - 1	0
paddr	The 12-bit MSB APB address	0 -16#FFF#	0
pmask	The APB address mask	16#000 - 16#F00#	F00
memtech	Memory technology	0 - NTECH	0

The usereg VHDL generic specifies whether to use an input register to synchronize the traced signals and to minimize their fan out. If usereg=1 then all signals will be clocked into a register on the positive edge of the supplied clock signal, otherwise they are sent directly to the RAM.

82.8 Signal descriptions

Table 1496 shows the interface signals of the core (VHDL ports).

*Table 1496.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	System clock	-
TCLK	N/A	Input	Sample clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
SIGNALS	N/A	Input	Vector of traced signals	-

* See GRLIB IP Library users manual

82.9 Library dependencies

Table 1497 shows libraries used when instantiating the core (VHDL libraries).

*Table 1497.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	MISC	Component	Component declaration

82.10 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
library gaisler;
use gaisler.misc.all;

entity logan_ex is
  port (
    clk : in std_ulogic;
    rstn : in std_ulogic;

    ... -- other signals
    );
end;

architecture rtl of logan_ex is

  -- AMBA signals
signal apbi  : apb_slv_in_type;
signal apbo  : apb_slv_out_vector := (others => apb_none);
signal signals : std_logic_vector(63 downto 0);

begin

-- Logic analyzer core
  logan0 : logan
  generic map (dbits=>64,depth=>4096,trigl=>2,usereg=>1,usequal=>0,
            pindex => 3, paddr => 3, pmask => 16#F00#, memtech => memtech)
  port map (rstn, clk, clk, apbi, apbo(3), signals);

end;
```

83 MCTRL - Combined PROM/IO/SRAM/SDRAM Memory Controller

83.1 Overview

The memory controller handles a memory bus hosting PROM, memory mapped I/O devices, asynchronous static ram (SRAM) and synchronous dynamic ram (SDRAM). The controller acts as a slave on the AHB bus. The function of the memory controller is programmed through memory configuration registers 1, 2 & 3 (MCFG1, MCFG2 & MCFG3) through the APB bus. The memory bus supports four types of devices: PROM, SRAM, SDRAM and local I/O. The memory bus can also be configured in 8- or 16-bit mode for applications with low memory and performance demands.

Chip-select decoding is done for two PROM banks, one I/O bank, five SRAM banks and two SDRAM banks.

The controller decodes three address spaces (PROM, I/O and RAM) whose mapping is determined through VHDL-generics.

Figure 234 shows how the connection to the different device types is made.

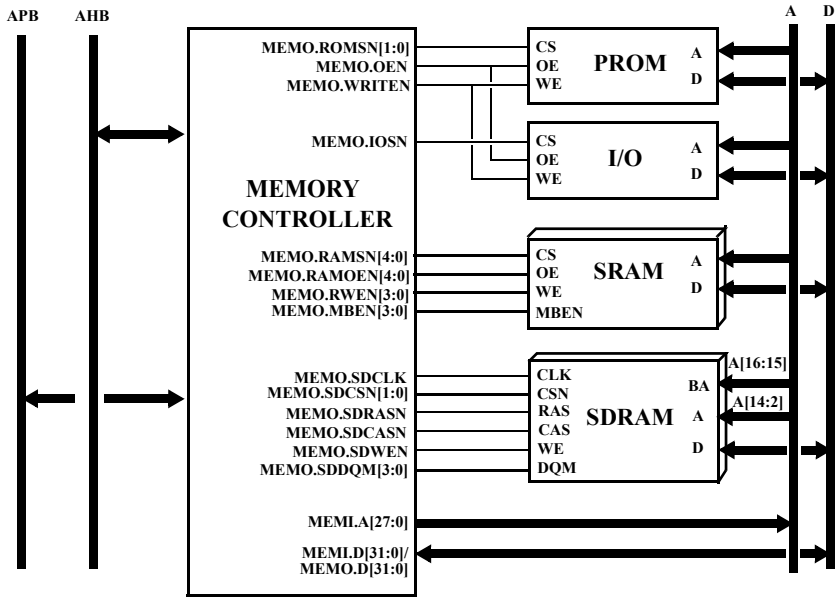


Figure 234. **Memory controller conected to AMBA bus and different types of 32-bit memory devices**

83.2 PROM access

Accesses to prom have the same timing as RAM accesses, the differences being that PROM cycles can have up to 15 waitstates.

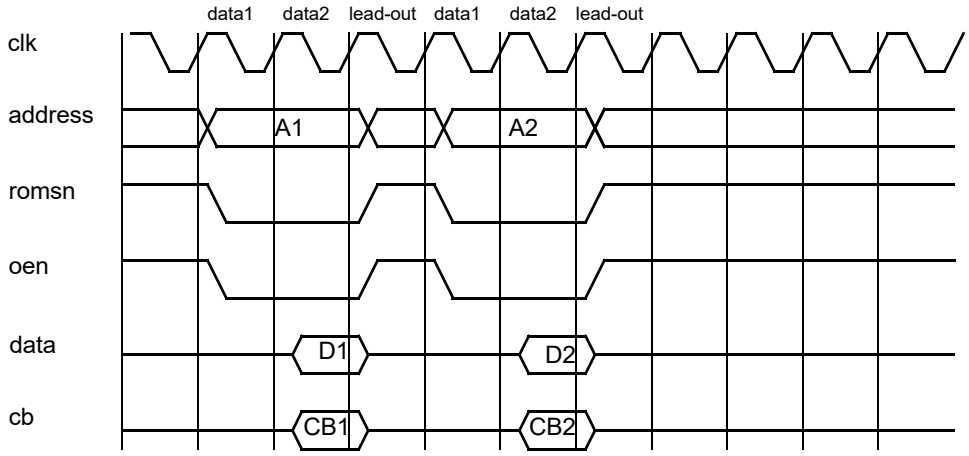


Figure 235. **Prom non-consecutive read cyclecs.**

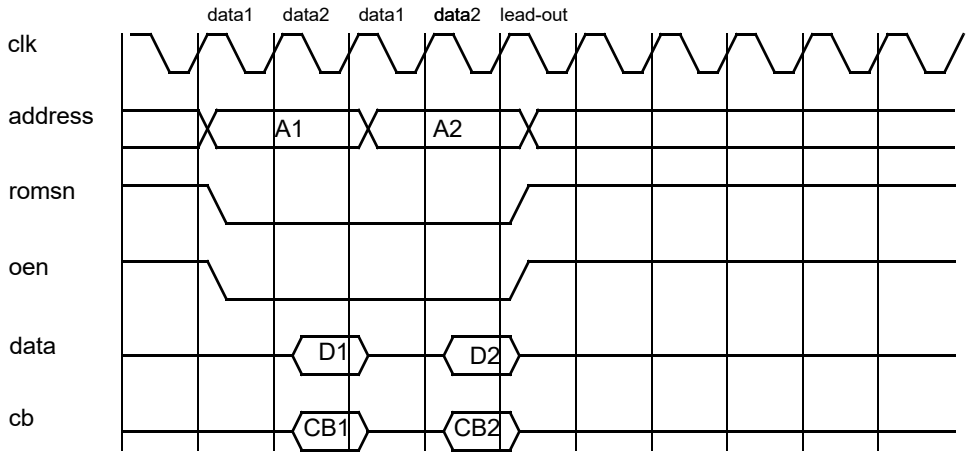


Figure 236. **Prom consecutive read cyclecs.**

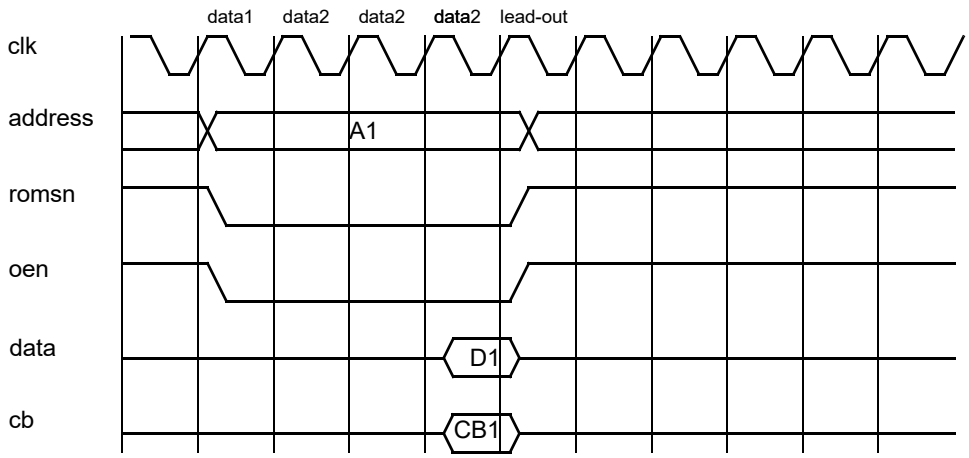


Figure 237. **Prom read access with two waitstates.**

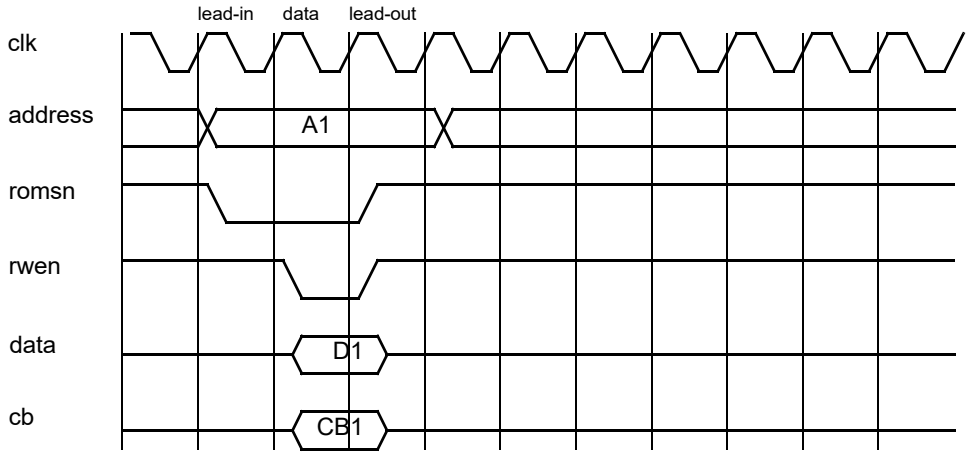


Figure 238. **Prom write cycle (0-waitstates)**

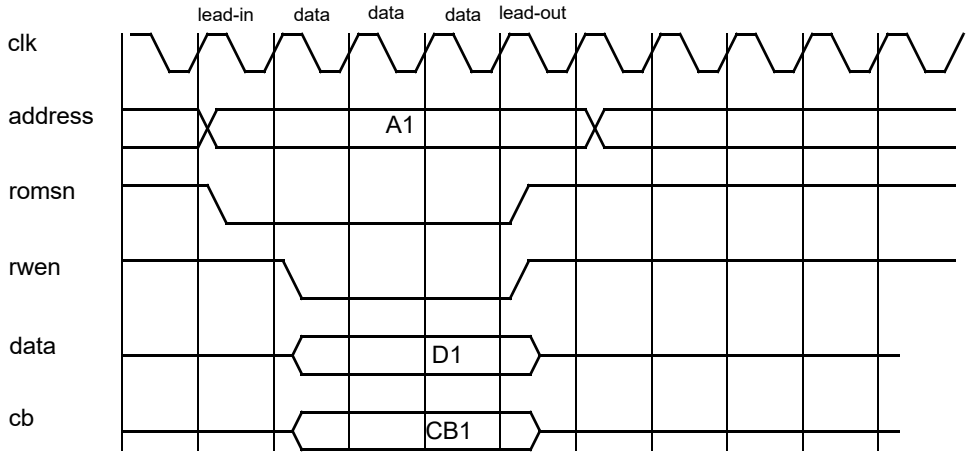


Figure 239. **Prom write cycle (2-waitstates)**

Two PROM chip-select signals are provided, MEMO.ROMSN[1:0]. MEMO.ROMSN[0] is asserted when the lower half of the PROM area as addressed while MEMO.ROMSN[1] is asserted for the upper half.

83.3 Memory mapped I/O

Accesses to I/O have similar timing to ROM/RAM accesses, the differences being that a additional waitstates can be inserted by de-asserting the MEMI.BRDYN signal. The I/O select signal (MEMO.IOSN) is delayed one clock to provide stable address before MEMO.IOSN is asserted.

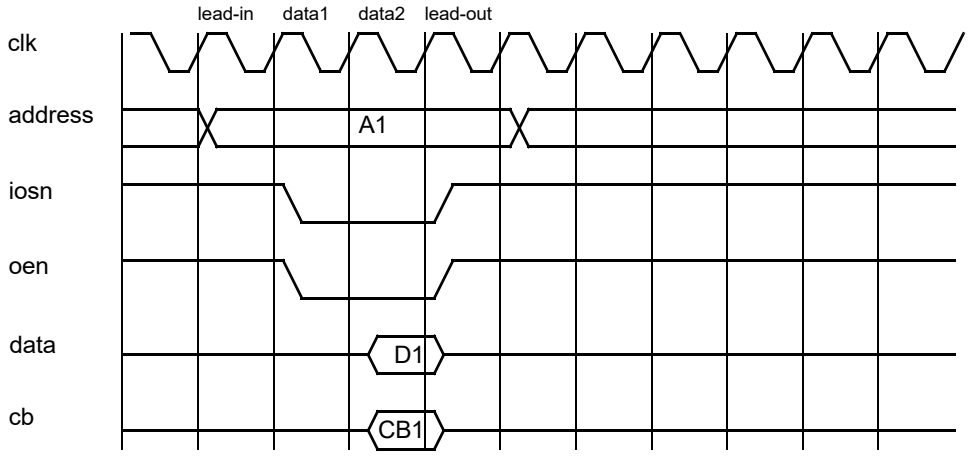


Figure 240. **I/O read cycle (0-waitstates)**

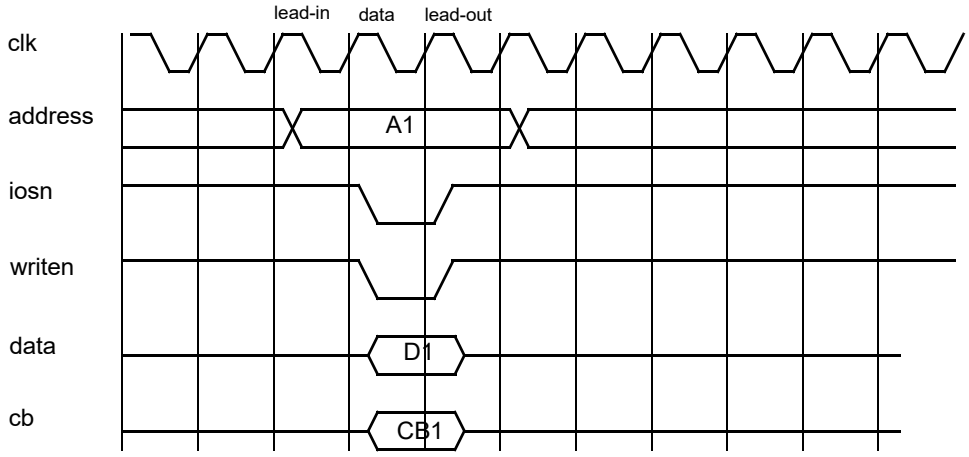


Figure 241. **I/O write cycle (0-waitstates)**

83.4 SRAM access

The SRAM area can be up to 1 Gbyte, divided on up to five RAM banks. The size of banks 1-4 (MEMO.RAMSN[3:0]is programmed in the RAM bank-size field (MCFG2[12:9]) and can be set in binary steps from 8 Kbyte to 256 Mbyte. The fifth bank (RAMSN[4]) decodes the upper 512 Mbyte (controlled by means of the *sdrasel* VHDL generic) and cannot be used simultaneously with SDRAM memory. A read access to SRAM consists of two data cycles and between zero and three waitstates. Accesses to MEMO.RAMSN[4] can further be stretched by de-asserting MEMI.BRDYN until the data is available. On non-consecutive accesses, a lead-out cycle is added after a read cycle to prevent bus contention due to slow turn-off time of memories or I/O devices. Figure 242 shows the basic read cycle waveform (zero waitstate).

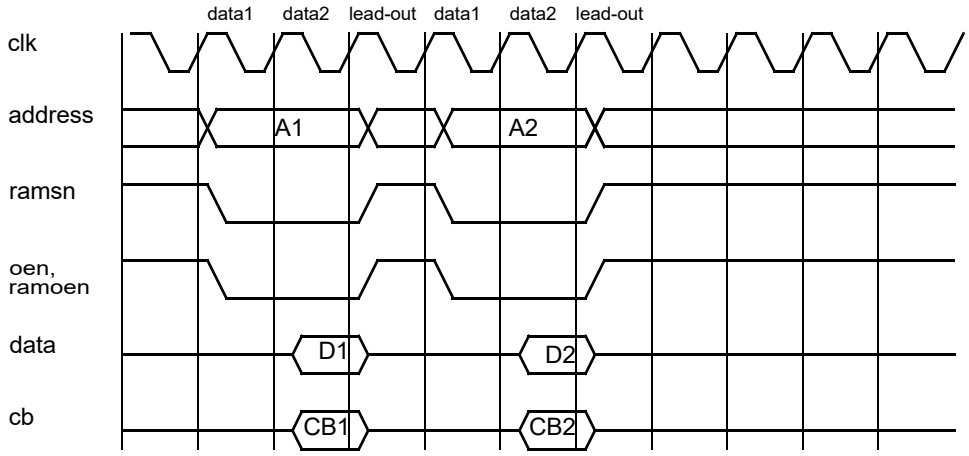


Figure 242. **SRAM non-consecutive read cyclecs.**

For read accesses to MEMO.RAMSN[4:0], a separate output enable signal (MEMO.RAMOEN[n]) is provided for each RAM bank and only asserted when that bank is selected. A write access is similar to the read access but takes a minimum of three cycles:

Through an (optional) feed-back loop from the write strobes, the data bus is guaranteed to be driven until the write strobes are de-asserted. Each byte lane has an individual write strobe to allow efficient byte and half-word writes. If the memory uses a common write strobe for the full 16- or 32-bit data, the read-modify-write bit in the MCFG2 register should be set to enable read-modify-write cycles for sub-word writes.

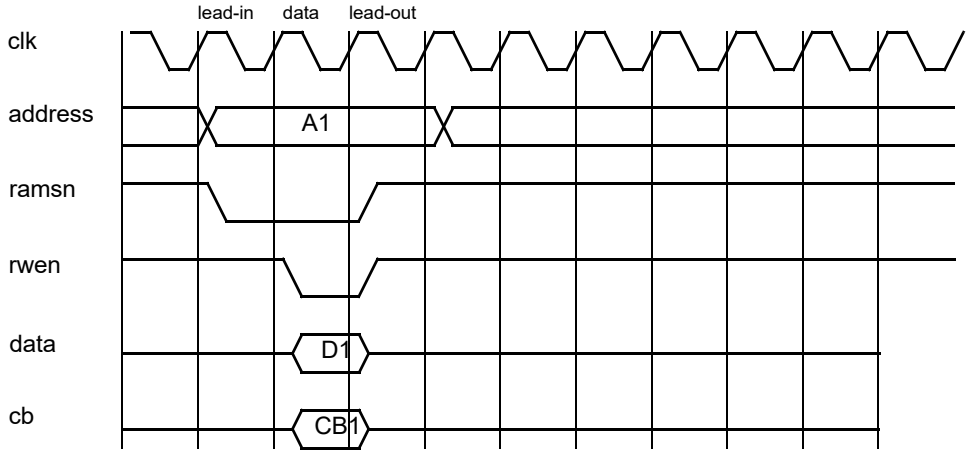


Figure 243. **Sram write cycle (0-waitstates)**

A drive signal vector for the data I/O-pads is provided which has one drive signal for each data bit. It can be used if the synthesis tool does not generate separate registers automatically for the current technology. This can remove timing problems with output delay.

83.5 8-bit and 16-bit PROM and SRAM access

To support applications with low memory and performance requirements efficiently, it is not necessary to always have full 32-bit memory banks. The SRAM and PROM areas can be individually configured for 8- or 16-bit operation by programming the ROM and RAM size fields in the memory configuration registers. Since read access to memory is always done on 32-bit word basis, read access to 8-bit memory will be transformed in a burst of four read cycles while access to 16-bit memory will

generate a burst of two 16-bits reads. During writes, only the necessary bytes will be writen. Figure 244 shows an interface example with 8-bit PROM and 8-bit SRAM. Figure 245 shows an example of a 16-bit memory interface.

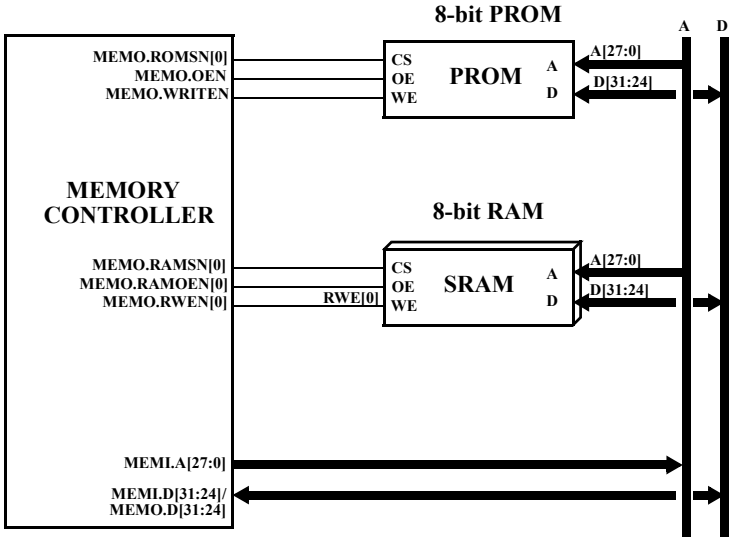


Figure 244. **8-bit memory interface example**

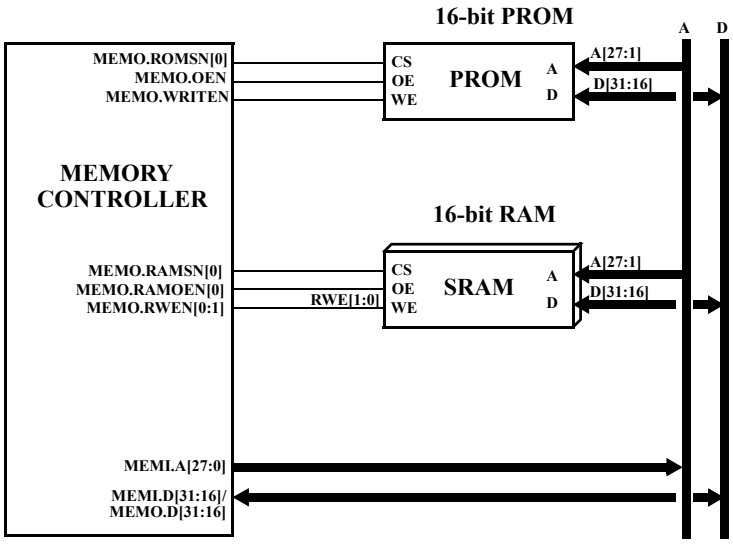


Figure 245. **16-bit memory interface example**

83.6 Burst cycles

To improve the bandwidth of the memory bus, accesses to consecutive addresses can be performed in burst mode. Burst transfers will be generated when the memory controller is accessed using an AHB burst request. These includes instruction cache-line fills, double loads and double stores. The timing of a burst cycle is identical to the programmed basic cycle with the exception that during read cycles, the lead-out cycle will only occurs after the last transfer. Burst cycles will not be generated to the IO area.

Only word (HSIZE = "010") bursts of incremental type (HBURST=INCR, INCR4, INCR8 or INCR16) are supported.

83.7 8- and 16-bit I/O access

Similar to the PROM/RAM areas, the I/O area can also be configured to 8- or 16-bit mode. However, the I/O device will NOT be accessed by multiple 8/16 bit accesses as the memory areas, but only with one single access just as in 32-bit mode. To access an I/O device on a 16-bit bus, LDUH/STH instructions should be used while LDUB/STB should be used with an 8-bit bus.

83.8 SDRAM access

83.8.1 General

Synchronous dynamic RAM (SDRAM) access is supported to two banks of PC100/PC133 compatible devices. This is implemented by a special version of the SDCTRL SDRAM controller core from Cobham Gaisler, which is optionally instantiated as a sub-block. The SDRAM controller supports 64M, 256M and 512M devices with 8 - 12 column-address bits, and up to 13 row-address bits. The size of the two banks can be programmed in binary steps between 4 Mbyte and 512 Mbyte. The operation of the SDRAM controller is controlled through MCFG2 and MCFG3 (see below). Both 32- and 64-bit data bus width is supported, allowing the interface of 64-bit DIMM modules. The memory controller can be configured to use either a shared or separate bus connecting the controller and SDRAM devices. When the VHDL generic **mobile** is set to a value not equal to 0, the controller supports mobile SDRAM.

83.8.2 Address mapping

The two SDRAM chip-select signals are decoded. SDRAM area is mapped into the upper half of the RAM area defined by BAR2 register. When the SDRAM enable bit is set in MCFG2, the controller is enabled and mapped into upper half of the RAM area as long as the SRAM disable bit is not set. If the SRAM disable bit is set, all access to SRAM is disabled and the SDRAM banks are mapped into the lower half of the RAM area.

83.8.3 Initialisation

When the SDRAM controller is enabled, it automatically performs the SDRAM initialisation sequence of PRECHARGE, 2x AUTO-REFRESH and LOAD-MODE-REG on both banks simultaneously. When mobile SDRAM functionality is enabled the initialization sequence is appended by a LOAD-EXTMODE-REG command. The controller programs the SDRAM to use page burst on read and single location access on write.

83.8.4 Configurable SDRAM timing parameters

To provide optimum access cycles for different SDRAM devices (and at different frequencies), some SDRAM parameters can be programmed through memory configuration register 2 (MCFG2) The programmable SDRAM parameters can be seen in tabel 1498.

***Table 1498.*SDRAM programmable timing parameters**

Function	Parameter	Range	Unit
CAS latency, RAS/CAS delay	t_{CAS}, t_{RCD}	2 - 3	clocks
Precharge to activate	t_{RP}	2 - 3	clocks
Auto-refresh command period	t_{RFC}	3 - 11	clocks
Auto-refresh interval		10 - 32768	clocks

Remaining SDRAM timing parameters are according the PC100/PC133 specification.

When mobile SDRAM support is enabled, one additional timing parameter (TXSR) can be programmed though the Power-Saving configuration register.

*Table 1499.*Mobile SDRAM programmable minimum timing parameters

SDRAM timing parameter	Minimum timing (clocks)
Exit Self Refresh mode to first valid command (t_{XSR})	tXSR

83.9 Refresh

The SDRAM controller contains a refresh function that periodically issues an AUTO-REFRESH command to both SDRAM banks. The period between the commands (in clock periods) is programmed in the refresh counter reload field in the MCFG3 register. Depending on SDRAM type, the required period is typically 7.8 or 15.6 µs (corresponding to 780 or 1560 clocks at 100 MHz). The generated refresh period is calculated as (reload value+1)/sysclk. The refresh function is enabled by setting bit 31 in MCFG2.

83.9.1 Self Refresh

The self refresh mode can be used to retain data in the SDRAM even when the rest of the system is powered down. When in the self refresh mode, the SDRAM retains data without external clocking and refresh are handled internally. The memory array that is refreshed during the self refresh operation is defined in the extended mode register. These settings can be changed by setting the PASR bits in the Power-Saving configuration register. The extended mode register is automatically updated when the PASR bits are changed. The supported “Partial Array Self Refresh” modes are: Full, Half, Quarter, Eighth, and Sixteenth array. “Partial Array Self Refresh” is only supported when mobile SDRAM functionality is enabled. To enable the self refresh mode, set the PMODE bits in the Power-Saving configuration register to “010” (Self Refresh). The controller will enter self refresh mode after every memory access (when the controller has been idle for 16 clock cycles), until the PMODE bits are cleared. When exiting this mode the controller introduce a delay defined by tXSR in the Power-Saving configuration register and a AUTO REFRESH command before any other memory access is allowed. The minimum duration of this mode is defined by tRAS. This mode is only available then the VHDL generic **mobile** >=1.

83.9.2 Power-Down

When entering the power-down mode all input and output buffers, excluding SDCKE, are deactivated. All data in the SDRAM is retained during this operation. To enable the power-down mode, set the PMODE bits in the Power-Saving configuration register to “001” (Power-Down). The controller will enter power-down mode after every memory access (when the controller has been idle for 16

clock cycles), until the PMODE bits is cleared. The REFRESH command will still be issued by the controller in this mode. When exiting this mode a delay of one clock cycles are added before issue any command to the memory. This mode is only available then the VHDL generic **mobile** >=1.

83.9.3 Deep Power-Down

The deep power-down operating mode is used to achieve maximum power reduction by eliminating the power of the memory array. Data will not be retained after the device enters deep power-down mode. To enable the deep power-down mode, set the PMODE bits in the Power-Saving configuration register to “101” (Deep Power-Down). To exit the deep power-down mode the PMODE bits in the Power-Saving configuration register must be cleared. The controller will respond with an AMBA ERROR response to an AMBA access, that will result in a memory access, during Deep Power-Down mode. This mode is only available then the VHDL generic **mobile** >=1 and mobile SDRAM functionality is enabled.

83.9.4 Temperature-Compensated Self Refresh

The settings for the temperature-compensation of the Self Refresh rate can be controlled by setting the TCSR bits in the Power-Saving configuration register. The extended mode register is automatically updated when the TCSR bits are changed. Note that some vendors implements a Internal Temperature-Compensated Self Refresh feature, which makes the memory to ignore the TCSR bits. This functionality is only available then the VHDL generic **mobile** >=1 and mobile SDRAM functionality is enabled.

83.9.5 Drive Strength

The drive strength of the output buffers can be controlled by setting the DS bits in the Power-Saving configuration register. The extended mode register is automatically updated when the DS bits are changed. The available options are: full, three-quarter, one-half, and one-quarter drive strengths. This functionality is only available then the VHDL generic **mobile** >=1 and mobile SDRAM functionality is enabled.

83.9.6 SDRAM commands

The controller can issue four SDRAM commands by writing to the SDRAM command field in MCFG2: PRE-CHARGE, AUTO-REFRESH, LOAD-MODE-REG (LMR) and LOAD-EXTMODE-REG (EMR). If the LMR command is issued, the CAS delay as programmed in MCFG2 will be used, remaining fields are fixed: page read burst, single location write, sequential burst. If the EMR command is issued, the DS, TCSR and PASR as programmed in Power-Saving configuration register will be used. To issue the EMR command, the EMR bit in the MCFG4 register has to be set. The command field will be cleared after a command has been executed. Note that when changing the value of the CAS delay, a LOAD-MODE-REGISTER command should be generated at the same time.

83.9.7 Read cycles

A read cycle is started by performing an ACTIVATE command to the desired bank and row, followed by a READ command after the programmed CAS delay. A read burst is performed if a burst access has been requested on the AHB bus. The read cycle is terminated with a PRE-CHARGE command, no banks are left open between two accesses.

83.9.8 Write cycles

Write cycles are performed similarly to read cycles, with the difference that WRITE commands are issued after activation. A write burst on the AHB bus will generate a burst of write commands without idle cycles in-between.

83.9.9 Address bus connection

The memory controller can be configured to either share the address and data buses with the SRAM, or to use separate address and data buses. When the buses are shared, the address bus of the SDRAMs should be connected to A[14:2], the bank address to A[16:15]. The MSB part of A[14:2] can be left unconnected if not used. When separate buses are used, the SDRAM address bus should be connected to SA[12:0] and the bank address to SA[14:13].

83.9.10 Data bus

SDRAM can be connected to the memory controller through the common or separate data bus. If the separate bus is used the width is configurable to 32 or 64 bits. 64-bit data bus allows the 64-bit SDRAM devices to be connected using the full data capacity of the devices. 64-bit SDRAM devices can be connected to 32-bit data bus if 64-bit data bus is not available but in this case only half the full data capacity will be used. There is a drive signal vector and separate data vector available for SDRAM. The drive vector has one drive signal for each data bit. These signals can be used to remove timing problems with the output delay when a separate SDRAM bus is used. SDRAM bus signals are described in section 83.14, for configuration options refer to section 83.17.

83.9.11 Clocking

The SDRAM clock typically requires special synchronisation at layout level. For Xilinx and Altera device, the GR Clock Generator can be configured to produce a properly synchronised SDRAM clock. For other FPGA targets, the GR Clock Generator can produce an inverted clock.

83.10 Using bus ready signaling

The MEMI.BRDYN signal can be used to stretch access cycles to the I/O area and the ram area decoded by MEMO.RAMSN[4]. The accesses will always have at least the pre-programmed number of waitstates as defined in memory configuration registers 1 & 2, but will be further stretched until MEMI.BRDYN is asserted. MEMI.BRDYN should be asserted in the cycle preceding the last one. The use of MEMI.BRDYN can be enabled separately for the I/O and RAM areas.

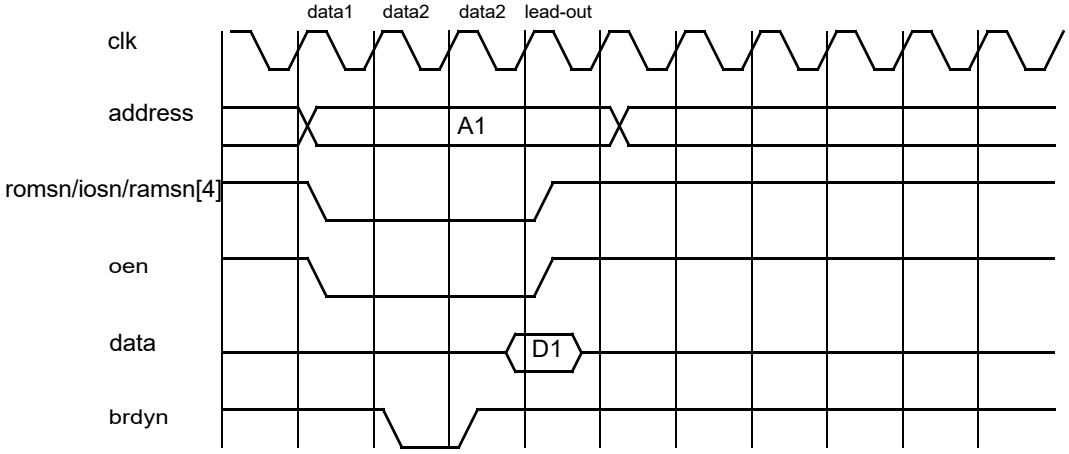


Figure 246. **READ cycle with one extra data2 cycle added with BRDYN (synchronous sampling). Lead-out cycle is only applicable for I/O accesses.**

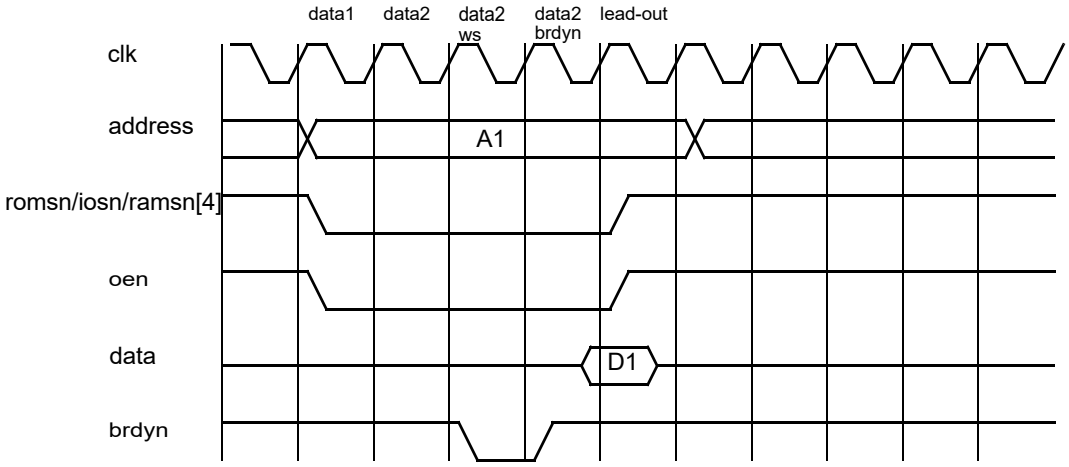


Figure 247. **Read cycle with one waitstate (configured) and one BRDYN generated waitstate (synchronous sampling).**

83.11 Access errors

An access error can be signaled by asserting the MEMI.BEXCN signal, which is sampled together with the data. If the usage of MEMI.BEXCN is enabled in memory configuration register 1, an error response will be generated on the internal AMBA bus. MEMI.BEXCN can be enabled or disabled through memory configuration register 1, and is active for all areas (PROM, I/O an RAM).

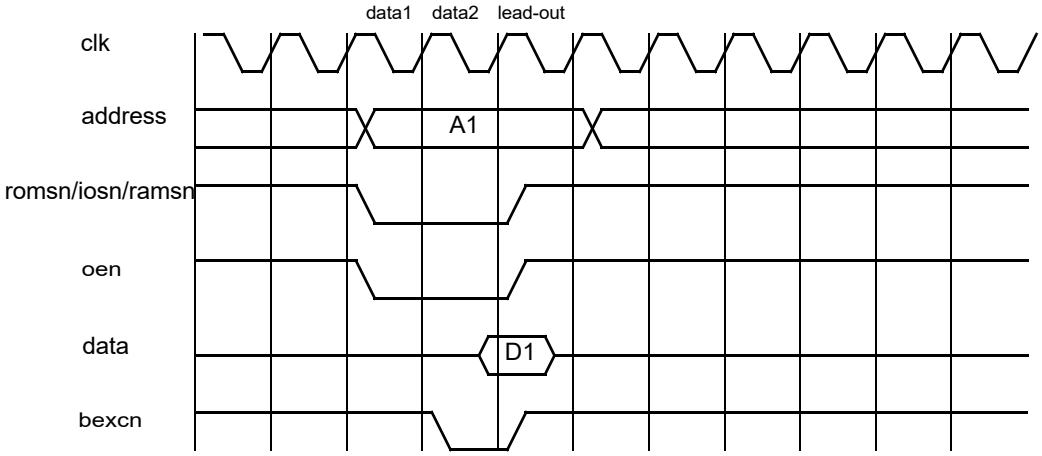


Figure 248. **Read cycle with BEXCN.**

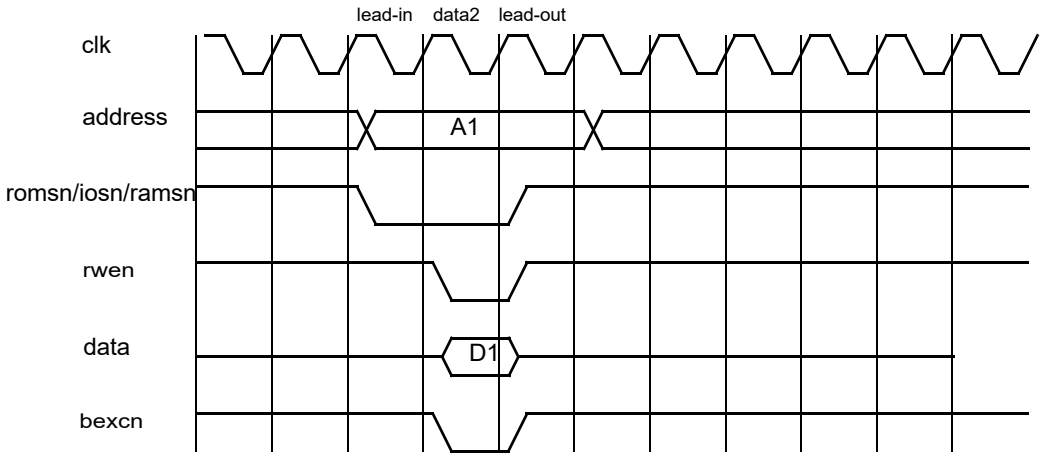


Figure 249. **Write cycle with BEXCN. Chip-select (iosn) is not asserted in lead-in cycle for io-accesses.**

83.12 Attaching an external DRAM controller

To attach an external DRAM controller, MEMO.RAMSN[4] should be used since it allows the cycle time to vary through the use of MEMI.BRDYN. In this way, delays can be inserted as required for opening of banks and refresh.

83.13 Endianness

The core is designed for big-endian systems.

83.14 Registers

The memory controller is programmed through registers mapped into APB address space.

***Table 1500.*Memory controller registers**

APB address offset	Register
0x0	MCFG1
0x4	MCFG2
0x8	MCFG3
0xC	MCFG4 (Power-Saving configuration register)

83.14.1 Memory configuration register 1 (MCFG1)

Memory configuration register 1 is used to program the timing of rom and local I/O accesses.

***Table 1501.*0x00 - MCFG1 - Memory configuration register 1.**

31 29	28 27	26	25	24	23 20	19	18
RESERVED	IOBUSW	IBRDY	BEXCN	R	IO WAITSTATES	IOEN	RESERVED
0	NR	0	0	0	0	0	0
r	rw	rw	rw	r	rw	rw	r

12	11	10	9 8	7 4	3 0
RESERVED	PWEN	R	PROM WIDTH	PROM WRITE WS	PROM READ WS
0	0	0	*	0xF	0xF
r	rw	r	rw	rw	rw

31 : 29 RESERVED

28 : 27 I/O bus width (IOBUSW) - Sets the data width of the I/O area (“00”=8, “01”=16, “10” =32).

***Table 1501.*0x00 - MCFG1 - Memory configuration register 1.**

26	I/O bus ready enable (IBRDY) - Enables bus ready (BRDYN) signalling for the I/O area. Reset to '0'.
25	Bus error enable (BEXCN) - Enables bus error signalling. Reset to '0'.
24	RESERVED
23 : 20	I/O waitstates (IO WAITSTATES) - Sets the number of waitstates during I/O accesses ("0000"=0, "0001"=1, "0010"=2,..., "1111"=15).
19	I/O enable (IOEN) - Enables accesses to the memory bus I/O area.
18:12	RESERVED
11	PROM write enable (PWEN) - Enables write cycles to the PROM area.
10	RESERVED
9 : 8	PROM width (PROM WIDTH) - Sets the data width of the PROM area ("00"=8, "01"=16, "10"=32).
7 : 4	PROM write waitstates (PROM WRITE WS) - Sets the number of wait states for PROM write cycles ("0000"=0, "0001"=1, "0010"=2,..., "1111"=15).
3 : 0	PROM read waitstates (PROM READ WS) - Sets the number of wait states for PROM read cycles ("0000"=0, "0001"=1, "0010"=2,...,"1111"=15). Reset to "1111".

During power-up, the prom width (bits [9:8]) are set with value on MEMI.BWIDTH inputs. The prom waitstates fields are set to 15 (maximum). External bus error and bus ready are disabled. All other fields are undefined.

83.14.2 Memory configuration register 2 (MCFG2)

Memory configuration register 2 is used to control the timing of the SRAM and SDRAM.

***Table 1502.*0x04 - MCFG2 - Memory configuration register 2.**

31	30	29 27	26	25 23	22 21	20 19	18	17	16
SDRF	TRP	SDRAM TRFC	TCAS	SDRAM BANKSZ	SDRAM COLSZ	SDRAM CMD	D64	R	MS
0	1	0b111	1	0	0b10	0	*	0	*
rw	rw	rw	rw	rw	rw	rw	r	r	r

15	14	13	12 9	8	7	6	5 4	3 2	1 0
RES	SE	SI	RAM BANK SIZE	R	RBRDY	RMW	RAM WIDTH	RAM WRITE WS	RAM READ WS
0	0	0	NR	0	NR	NR	NR	0	0
r	rw	rw	rw	r	rw	rw	rw	rw	rw

31	SDRAM refresh (SDRF) - Enables SDRAM refresh.
30	SDRAM TRP parameter (TRP) - t_{RP} will be equal to 2 or 3 system clocks (0/1).
29 : 27	SDRAM TRFC parameter (SDRAM TRFC) - t_{RFC} will be equal to 3+field-value system clocks.
26	SDRAM TCAS parameter (TCAS) - Selects 2 or 3 cycle CAS delay (0/1). When changed, a LOAD-COMMAND-REGISTER command must be issued at the same time. Also sets RAS/CAS delay (t_{RCD}).
25 : 23	SDRAM bank size (SDRAM BANKSZ) - Sets the bank size for SDRAM chip selects ("000"=4 Mbyte, "001"=8 Mbyte, "010"=16 Mbyte.... "111"=512 Mbyte). When configured for 64-bit wide SDRAM data bus (sdbits=64), the meaning of this field doubles so that "000"=8 Mbyte, .., "111"=1024 Mbyte
22 : 21	SDRAM column size (SDRAM COLSZ) - "00"=256, "01"=512, "10"=1024, "11"=2048 except when bit[25:23]="111" then "11"=4096
20 : 19	SDRAM command (SDRAM CMD) - Writing a non-zero value will generate a SDRAM command. "01"=PRECHARGE, "10"=AUTO-REFRESH, "11"=LOAD-COMMAND-REGISTER. The field is reset after the command has been executed.
18	64-bit SDRAM data bus (D64) - Reads '1' if the memory controller is configured for 64-bit SDRAM data bus width, '0' otherwise. Read-only.
17	RESERVED
16	Mobile SDR support enabled. '1' = Enabled, '0' = Disabled (read-only)

***Table 1502*.0x04 - MCFG2 - Memory configuration register 2.**

15	RESERVED
14	SDRAM enable (SE) - Enables the SDRAM controller.
13	SRAM disable (SI) - Disables accesses RAM if bit 14 (SE) is set to '1'.
12 : 9	RAM bank size (RAM BANK SIZE) - Sets the size of each RAM bank ("0000"=8 kbyte, "0001"=16 kbyte, ..., "1111"=256 Mbyte).
8	RESERVED
7	RAM bus ready enable (RBRDY) - Enables bus ready signalling for the RAM area.
6	Read-modify-write enable (RMW) - Enables read-modify-write cycles for sub-word writes to 16- bit 32-bit areas with common write strobe (no byte write strobe).
5 : 4	RAM width (RAM WIDTH) - Sets the data width of the RAM area ("00"=8, "01"=16, "1X"=32).
3 : 2	RAM write waitstates (RAM WRITE WS) - Sets the number of wait states for RAM write cycles ("00"=0, "01"=1, "10"=2, "11"=3).
1 : 0	RAM read waitstates (RAM READ WS) - Sets the number of wait states for RAM read cycles ("00"=0, "01"=1, "10"=2, "11"=3).

83.14.3 Memory configuration register 3 (MCFG3)

MCFG3 is contains the reload value for the SDRAM refresh counter.

TABLE 1503. 0x08 - MCFG3 - Memory Configuration register 3

31 27	26 12	11 0
RESERVED	SDRAM REFRESH RELOAD VALUE	RESERVED

31: 27	RESERVED
26: 12	SDRAM refresh counter reload value (SDRAM REFRESH RELOAD VALUE)
11: 0	RESERVED

The period between each AUTO-REFRESH command is calculated as follows:

$t_{REFRESH}$ = ((reload value) + 1) / SYSCLK

83.14.4 Power-Saving Configuration Register

*Table 1504.*0x0C - MCFG4 - Power-Saving configuration register

31	30	29	28 24	23 20	19	18 16	15 7	6 5	4 3	2 0
ME	CE	EM	RESERVED	tXSR	R	PMODE	RESERVED	DS	TCSR	PASR
*	*	0	0	0b111	0	0	0	0	0	0
rw	rw	rw	r	rw	r	rw	r	rw	rw	rw

31 Mobile SDRAM functionality enabled. ‘1’ = Enabled (support for Mobile SDRAM), ‘0’ = disabled (support for standard SDRAM)

30 Clock enable (CE). This value is driven on the CKE inputs of the SDRAM. Should be set to ‘1’ for correct operation. This register bit is read only when Power-Saving mode is other then none.

29 EMR. When set, the LOAD-COMMAND-REGISTER command issued by the SDRAM command field in MCFG2 will be interpret as a LOAD-EXTENDED-COMMAND-REGISTER command.

28: 24 Reserved

23: 20 SDRAM tXSR timing. tXSR will be equal to field-value system clocks. (Read only when Mobile SDR support is disabled).

19 Reserved

18: 16 Power-Saving mode (Read only when Mobile SDR support is disabled).
“000”: none
“001”: Power-Down (PD)
“010”: Self-Refresh (SR)
“101”: Deep Power-Down (DPD)

15: 7 Reserved

6: 5 Selectable output drive strength (Read only when Mobile SDR support is disabled).
“00”: Full
“01”: One-half
“10”: One-quarter
“11”: Three-quarter

4: 3 Reserved for Temperature-Compensated Self Refresh (Read only when Mobile SDR support is disabled).
“00”: 70ªC
“01”: 45ªC
“10”: 15ªC
“11”: 85ªC

2: 0 Partial Array Self Refresh (Read only when Mobile SDR support is disabled).
“000”: Full array (Banks 0, 1, 2 and 3)
“001”: Half array (Banks 0 and 1)
“010”: Quarter array (Bank 0)
“101”: One-eighth array (Bank 0 with row MSB = 0)
“110”: One-sixteenth array (Bank 0 with row MSB = 00)

83.15 Vendor and device identifiers

The core has vendor identifier 0x04 (ESA) and device identifier 0x00F. For description of vendor and device identifier see GRLIB IP Library User’s Manual.

83.16 Implementation

83.16.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User’s Manual). The core makes use of synchronous reset and resets a subset of its internal registers. See the documentation for the *syncrst* VHDL generic for information on asynchronous reset affecting external signals.

83.17 Configuration options

Table 1505 shows the configuration options of the core (VHDL generics).

***Table 1505.*Configuration options**

Generic	Function	Allowed range	Default
hindex	AHB slave index	1 - NAHBSLV-1	0
pindex	APB slave index	0 - NAPBSLV-1	0
romaddr	ADDR field of the AHB BAR0 defining PROM address space. Default PROM area is 0x0 - 0x1FFFFFFF.	0 - 16#FFF#	16#000#
rommask	MASK field of the AHB BAR0 defining PROM address space.	0 - 16#FFF#	16#E00#
ioaddr	ADDR field of the AHB BAR1 defining I/O address space. Default I/O area is 0x20000000 - 0x2FFFFFFF.	0 - 16#FFF#	16#200#
iomask	MASK field of the AHB BAR1 defining I/O address space.	0 - 16#FFF#	16#E00#
ramaddr	ADDR field of the AHB BAR2 defining RAM address space. Default RAM area is 0x40000000-0x7FFFFFFF.	0 - 16#FFF#	16#400#
rammask	MASK field of the AHB BAR2 defining RAM address space.	0 -16#FFF#	16#C00#
paddr	ADDR field of the APB BAR configuration registers address space.	0 - 16#FFF#	0
pmask	MASK field of the APB BAR configuration registers address space.	0 - 16#FFF#	16#FFF#
wprot	RAM write protection.	0 - 1	0
invclk	Inverted clock is used for the SDRAM.	0 - 1	0
fast	Enable fast SDRAM address decoding.	0 - 1	0
romasel	log2(PROM address space size) - 1. E.g. if size of the PROM area is 0x20000000 romasel is log2(2^29)-1 = 28.	0 - 31	28
sdrasel	log2(RAM address space size) - 1. E.g if size of the RAM address space is 0x40000000 sdrasel is log2(2^30)-1= 29.	0 - 31	29
srbanks	Number of SRAM banks.	0 - 5	4
ram8	Enable 8-bit PROM and SRAM access.	0 - 1	0
ram16	Enable 16-bit PROM and SRAM access.	0 - 1	0
sden	Enable SDRAM controller.	0 - 1	0
sepbus	SDRAM is located on separate bus.	0 - 1	1
sdbits	32 or 64 -bit SDRAM data bus.	32, 64	32
sdlsb	Can be used to shift address lines used for SDRAM. Leave at default value.	-	2
oepol	Select polarity of drive signals for data pads. 0 = active low, 1 = active high.	0 - 1	0
syncrst	When syncrst is set to 0 then the output registers of the core have asynchronous reset. When syncrst is set to 1 only synchronous reset is used within the core and the output signals are instead gated with the reset signal.	0 - 1	0
pageburst	Line burst read of length 8 when 0, page burst read when 1, programmable read burst type when 2.	0 - 2	0
scantest	Enable scan test support (connects test oen to output enables, handles asynchronous reset case).	0 - 1	0
mobile	Enable Mobile SDRAM support 0: Mobile SDRAM support disabled 1: Mobile SDRAM support enabled but not default 2: Mobile SDRAM support enabled by default 3: Mobile SDRAM support only (no regular SDR support)	0 - 3	0

83.18 Signal descriptions

Table 1506 shows the interface signals of the core (VHDL ports).

***Table 1506.*Signal descriptions**

Signal name	Field	Type	Function	Active
CLK	N/A	Input	Clock	-
RST	N/A	Input	Reset	Low
MEMI	DATA[31:0]	Input	Memory data	High
	BRDYN	Input	Bus ready strobe	Low
	BEXCN	Input	Bus exception	Low
	WRN[3:0]	Input	SRAM write enable feedback signal	Low
	BWIDTH[1:0]	Input	Sets the reset value of the PROM data bus width field in the MCFG1 register	High
	SD[31:0]	Input	SDRAM separate data bus	High
MEMO	ADDRESS[31:0]	Output	Memory address	High
	DATA[31:0]	Output	Memory data	-
	SDDATA[63:0]	Output	Sdram memory data	-
	RAMSN[4:0]	Output	SRAM chip-select	Low
	RAMOEN[4:0]	Output	SRAM output enable	Low
	IOSN	Output	Local I/O select	Low
	ROMSN[1:0]	Output	PROM chip-select	Low
	OEN	Output	Output enable	Low
	WRITEN	Output	Write strobe	Low
	WRN[3:0]	Output	SRAM write enable: WRN[0] corresponds to DATA[31:24], WRN[1] corresponds to DATA[23:16], WRN[2] corresponds to DATA[15:8], WRN[3] corresponds to DATA[7:0].	Low
	MBEN[3:0]	Output	Byte enable: MBEN[0] corresponds to DATA[31:24], MBEN[1] corresponds to DATA[23:16], MBEN[2] corresponds to DATA[15:8], MBEN[3] corresponds to DATA[7:0].	Low
	BDRIVE[3:0]	Output	Drive byte lanes on external memory bus.Controls I/O-pads connected to external memory bus: BDRIVE[0] corresponds to DATA[31:24], BDRIVE[1] corresponds to DATA[23:16], BDRIVE[2] corresponds to DATA[15:8], BDRIVE[3] corresponds to DATA[7:0].	Low/High
	VBDRIVE[31:0]	Output	Vectored I/O-pad drive signals.	Low/High
	SVBDRIVE[63:0]	Output	Vectored I/O-pad drive signals for separate sdram bus.	Low/High
	READ	Output	Read strobe	High
	SA[14:0]	Output	SDRAM separate address bus	High
AHBSI	*	Input	AHB slave input signals	-
AHBSO	*	Output	AHB slave output signals	-

Table 1506. **Signal descriptions**

Signal name	Field	Type	Function	Active
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
WPROT	WPROTHIT	Input	Unused	-
SDO	SDCASN	Output	SDRAM column address strobe	Low
	SDCKE[1:0]	Output	SDRAM clock enable	High
	SDCSN[1:0]	Output	SDRAM chip select	Low
	SDDQM[7:0]	Output	SDRAM data mask: DQM[7] corresponds to DATA[63:56], DQM[6] corresponds to DATA[55:48], DQM[5] corresponds to DATA[47:40], DQM[4] corresponds to DATA[39:32], DQM[3] corresponds to DATA[31:24], DQM[2] corresponds to DATA[23:16], DQM[1] corresponds to DATA[15:8], DQM[0] corresponds to DATA[7:0].	Low
	SDRASN	Output	SDRAM row address strobe	Low
	SDWEN	Output	SDRAM write enable	Low

* see GRLIB IP Library User's Manual

83.19 Library dependencies

Table 1507 shows libraries used when instantiating the core (VHDL libraries).

Table 1507. **Library dependencies**

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AHB signal definitions
GAISLER	MEMCTRL	Signals	Memory bus signals definitions
		Components	SDMCTRL component
ESA	MEMORYCTRL	Component	Memory controller component declaration

83.20 Instantiation

This example shows how the core can be instantiated.

The example design contains an AMBA bus with a number of AHB components connected to it including the memory controller. The external memory bus is defined on the example designs port map and connected to the memory controller. System clock and reset are generated by GR Clock Generator and Reset Generator.

Memory controller decodes default memory areas: PROM area is 0x0 - 0x1FFFFFFF, I/O-area is 0x20000000-0x3FFFFFFF and RAM area is 0x40000000 - 0x7FFFFFFF. SDRAM controller is enabled. SDRAM clock is synchronized with system clock by clock generator.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.memctrl.all;
use gaisler.pads.all;   -- used for I/O pads
```

```
library esa;
use esa.memoryctrl.all;

entity mctrl_ex is
  port (
    clk : in std_ulogic;
    resetn : in std_ulogic;
    pllref : in  std_ulogic;

    -- memory bus
    address  : out   std_logic_vector(27 downto 0); -- memory bus
    data     : inout std_logic_vector(31 downto 0);
    ramsn    : out   std_logic_vector(4 downto 0);
    ramoen   : out   std_logic_vector(4 downto 0);
    rwen     : inout std_logic_vector(3 downto 0);
    romsn    : out   std_logic_vector(1 downto 0);
    iosn     : out   std_logic;
    oen      : out   std_logic;
    read     : out   std_logic;
    writen   : inout std_logic;
    brdyn    : in    std_logic;
    bexcn    : in    std_logic;
-- sdram i/f
    sdcke    : out std_logic_vector ( 1 downto 0);  -- clk en
    sdcsn    : out std_logic_vector ( 1 downto 0);  -- chip sel
    sdwen    : out std_logic;                       -- write en
    sdrasn   : out std_logic;                       -- row addr stb
    sdcasn   : out std_logic;                       -- col addr stb
    sddqm    : out std_logic_vector (7 downto 0);  -- data i/o mask
    sdclk    : out std_logic;                       -- sdram clk output
    sa       : out std_logic_vector(14 downto 0); -- optional sdram address
    sd       : inout std_logic_vector(63 downto 0) -- optional sdram data
    );
end;

architecture rtl of mctrl_ex is

  -- AMBA bus (AHB and APB)
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbsi : ahb_slv_in_type;
  signal ahbso : ahb_slv_out_vector := (others => ahbs_none);
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);

  -- signals used to connect memory controller and memory bus
  signal memi : memory_in_type;
  signal memo : memory_out_type;

  signal sdo : sdram_out_type;

  signal wprot : wprot_out_type;  -- dummy signal, not used
  signal clkm, rstn : std_ulogic; -- system clock and reset

-- signals used by clock and reset generators
  signal cgi : clkgen_in_type;
  signal cgo : clkgen_out_type;

  signal gnd : std_ulogic;

begin

  -- Clock and reset generators
  clkgen0 : clkgen generic map (clk_mul => 2, clk_div => 2, sdramen => 1,
                                tech => virtex2, sdinvclk => 0)
  port map (clk, gnd, clkm, open, open, sdclk, open, cgi, cgo);

  cgi.pllctrl <= "00"; cgi.pllrst <= resetn; cgi.pllref <= pllref;

  -- Memory controller
  mctrl0 : mctrl generic map (srbanks => 1, sden => 1)
```

```
    port map (rstn, clkm, memi, memo, ahbsi, ahbso(0), apbi, apbo(0), wprot, sdo);

  -- memory controller inputs not used in this configuration
  memi.brdyn <= '1'; memi.bexcn <= '1'; memi.wrn <= "1111";
  memi.sd <= sd;

  -- prom width at reset
  memi.bwidth <= "10";

  -- I/O pads driving data memory bus data signals
  datapads : for i in 0 to 3 generate
      data_pad : iopadv generic map (width => 8)
      port map (pad => data(31-i*8 downto 24-i*8),
                o => memi.data(31-i*8 downto 24-i*8),
                en => memo.bdrive(i),
                i => memo.data(31-i*8 downto 24-i*8));
  end generate;

  -- connect memory controller outputs to entity output signals
  address <= memo.address; ramsn <= memo.ramsn; romsn <= memo.romsn;
  oen <= memo.oen; rwen <= memo.wrn; ramoen <= "1111" & memo.ramoen(0);
  sa <= memo.sa;
  writen <= memo.writen; read <= memo.read; iosn <= memo.iosn;
  sdcke <= sdo.sdcke; sdwen <= sdo.sdwen; sdcsn <= sdo.sdcsn;
  sdrasn <= sdo.rasn; sdcasn <= sdo.casn; sddqm <= sdo.dqm;
end;
```

84 MEMSCRUB - AHB Memory Scrubber and Status Register

84.1 Overview

The memory scrubber monitors an AMBA AHB bus for accesses triggering an error response, and for correctable errors signaled from fault tolerant slaves on the bus. The core can be programmed to scrub a memory area by reading through the memory and writing back the contents using a locked read-write cycle whenever a correctable error is detected. It can also be programmed to initialize a memory area to known values.

The memory scrubber core is largely backwards compatible with the AHBSTAT core, and can replace it in many cases. Unlike AHBSTAT, the scrubber's registers are accessed through the AMBA AHB bus.

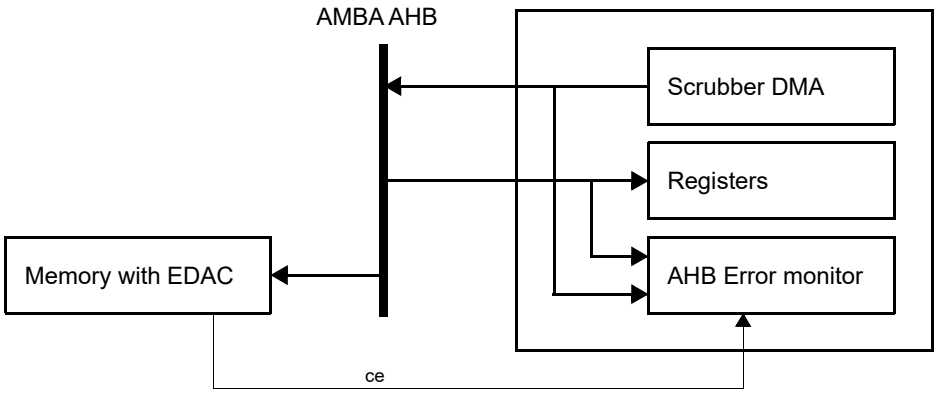


Figure 250. Memory scrubber block diagram

84.2 Operation

84.2.1 Errors

All AMBA AHB bus transactions are monitored and current HADDR, HWRITE, HMASTER and HSIZE values are stored internally. When an error response (HRESP = "01") is detected, an internal counter is increased. When the counter exceeds a user-selected threshold, the status and address register contents are frozen and the New Error (NE) bit is set to one. At the same time an interrupt is generated, as described hereunder.

The default threshold is zero and enabled on reset so the first error on the bus will generate an interrupt.

Note that many of the fault tolerant units containing EDAC signal an un-correctable error as an AMBA error response, so that it can be detected by the processor as described above.

84.2.2 Correctable errors

Not only error responses on the AHB bus can be detected. Many of the fault tolerant units containing EDAC have a correctable error signal which is asserted each time a correctable error is detected. When such an error is detected, the effect will be the same as for an AHB error response. The only difference is that the Correctable Error (CE) bit in the status register is set to one when a correctable error is detected. Correctable and uncorrectable errors use separate counters and threshold values.

When the CE bit is set, the interrupt routine can acquire the address containing the correctable error from the failing address register and correct it. When it is finished it resets the CE bit and the monitoring becomes active again. Interrupt handling is described in detail hereunder.

The correctable error signals from the fault tolerant units should be connected to the *scrubi.cerror* input signal vector of the AHB status register core, which is or-ed internally and if the resulting signal is asserted, it will have the same effect as an AHB error response.

84.2.3 Scrubbing

The memory scrubber can be commanded to scrub a certain memory area, by writing a start and end address to the scrubbers start/end registers, followed by writing “00” to the scrub mode field and ‘1’ to the scrub enable bit in the scrubber control register.

After starting, the core will proceed to read the memory region in bursts. The burst size is fixed (set by the *burstlen* generic) and typically tuned to match the cache-line size or native block size of the slave. When a correctable error is detected, the scrubber performs a locked read-write cycle to correct the error, and then resumes the scrub operation.

If the correctable error detected is in the middle of a burst, the following read in the burst is completed before the read-write cycle begins. The core can handle the special case where that access also had a correctable error within the same locked scrub cycle.

If an uncorrectable error is detected, that location is left untouched.

Note that the status register functionality is running in parallel with the scrubber, so correctable and uncorrectable errors will be logged as usual. To prevent double logging, the core masks out the (expected) correctable error arising during the locked correction cycle.

To allow normal access to the bus, the core sleeps for a number of cycles between each burst. The number of cycles can be adjusted in the config register.

If the ID bit is set in the config register, the core will interrupt when the complete scrub is done.

84.2.4 Scrubber error counters

The core keeps track of the number of correctable errors detected during the current scrub run and the number of errors detected during processing of the current “count block”. The size of the count block is a fixed power of two equal or larger than the burst length (set by the *countlen* generic).

The core can be set up to interrupt when the counters exceed given thresholds. When this happens, the NE bit, plus one of the SEC/SBC bits, is set in the status register.

84.2.5 External start and clear

If the ES bit is set in the config register, the scrub enable bit is set automatically when the start input signal goes high. This can be used to set up periodic scrubbing.

The external input signal clrerr can be used to clear the global error counters. If this is connected to a timer, it is possible to count errors that have occurred within a specific unit of time. This signal can be disabled through the EC bit in the config register.

84.2.6 Memory regeneration

The regeneration mode performs the same basic function as the scrub mode, but is optimised for the case where many (or all) locations have correctable errors.

In this mode, the whole memory area selected is scrubbed using locked read/write bursts.

If an uncorrectable error is encountered during the read burst, that burst block is processed once again using the regular scrub routine, and the regeneration mode resumes on the following block. This avoids overwriting uncorrectable error locations.

84.2.7 Initialization

The scrubber can be used to write a pre-defined pattern to a block of memory. This is often necessary on EDAC memory before it can be used.

Before running the initialization, the pattern to be written to memory should be written into the scrubber initialization data register. The pattern has the same size as the burst length, so the corresponding number of writes to the initialization data register must be made.

84.2.8 Interrupts

The interrupt is generated on the line selected by the *hirq* VHDL generic. The interrupt is connected to the interrupt controller to inform the processor of the event.

After an interrupt is generated, either the NE bit or the DONE bit in the status register is set, to indicate which type of event caused the interrupt.

The normal procedure is that an interrupt routine handles the error with the aid of the information in the status registers. When it is finished it resets the NE bit in the AHB status register or the DONE bit in the scrubber status register, and the monitoring becomes active again. Error interrupts can be generated for both AMBA error responses and correctable errors as described above.

84.2.9 Mode switching

Switching between scrubbing and regeneration modes can be done on the fly during a scrub by modifying the MODE field in the scrubber configuration register. The mode change will take effect on the following scrub burst.

If the address range needs to be changed, then the core should be stopped before updating the registers. This is done by clearing the SCEN bit, and waiting for the ACTIVE bit in the status register to go low. An exception is when making the range larger (i.e. increasing the end address or decreasing the start address), as this can be done on the fly.

84.2.10 Dual range support

The scrubber can work over two non-overlapping memory ranges. This feature is enabled by writing the start/end addresses of the second range into the scrubber's second range start/end registers and setting the SERA bit in the configuration register. The two address ranges should not overlap.

84.3 Registers

The core is programmed through registers mapped into an I/O region in the AHB address space. Only 32-bit accesses are supported.

*Table 1508.*Memory scrubber registers

AHB address offset	Registers
0x00	AHB Status register
0x04	AHB Failing address register
0x08	AHB Error configuration register
0x0C	Reserved
0x10	Scrubber status register
0x14	Scrubber configuration register
0x18	Scrubber range low address register
0x1C	Scrubber range high address register
0x20	Scrubber position register
0x24	Scrubber error threshold register
0x28	Scrubber initialization data register
0x2C	Scrubber second range start address register
0x30	Scrubber second range end address register

84.3.1 AHB Status Register

Table 1509. 0x00 - AHBS - AHB Status register

31 22	21 14	13	12	11	10	9	8	7 6	5 3	2 0
CECNT	UECNT	DONE	RES	SEC	SBC	CE	NE	HWRITE	HMASTER	HSIZE
0	0	0	0	0	0	0	0	NR	NR	NR
rw	rw	r	r	rw	rw	rw	rw	r	r	r

31: 22 CECNT: Global correctable error count

21: 14 UECNT: Global uncorrectable error count

13 DONE: Task completed. (read-only)

This is a read-only copy of the DONE bit in the status register.

12 RESERVED

11 SEC: Scrubber error counter threshold exceeded. Asserted together with NE.

10 SBC: Scrubber block error counter threshold exceeded. Asserted together with NE.

9 CE: Correctable Error. Set if the detected error was caused by a correctable error and zero otherwise.

8 NE: New Error. Deasserted at start-up and after reset. Asserted when an error is detected. Reset by writing a zero to it.

7 The HWRITE signal of the AHB transaction that caused the error.

6: 3 The HMASTER signal of the AHB transaction that caused the error.

2: 0 The HSIZE signal of the AHB transaction that caused the error

84.3.2 AHB Failing Address Register

Table 1510. 0x04 - AHBFAR - AHB Failing address register

31 0
AHB FAILING ADDRESS
NR
r

31: 0 The HADDR signal of the AHB transaction that caused the error.

84.3.3 AHB Error Configuration Register

Table 1511. 0x08 - AHBERC - AHB Error configuration register

31 22	21 14	13 2	1	0
CORRECTABLE ERROR COUNT THRESHOLD	UNCORR. ERROR COUNT THRESH.	RESERVED	CECTE	UECTE
0	0	0	0	0
rw	rw	r	rw	rw

31: 22 Interrupt threshold value for global correctable error count

21: 14 Interrupt threshold value for global uncorrectable error count

13: 2 RESERVED

1 CECTE: Correctable error count threshold enable

0 UECTE: Uncorrectable error count threshold enable

84.3.4 Scrubber Status Register

Table 1512. 0x10 - STAT - Scrubber status register

31 22	21 14	13	12 5	4 1	0
SCRUB RUN ERROR COUNT	BLOCK ERROR COUNT	DONE	RESERVED	BURSTLEN	ACTIVE
0	0	0	0	*	0
r	r	wc	r	r	r

31: 22 Number of correctable errors in current scrub run (read-only)

21: 14 Number of correctable errors in current block (read-only)

13 DONE: Task completed.

Needs to be cleared (by writing zero) before a new task completed interrupt can occur.

12: 5 RESERVED

4: 1 Burst length in 2-log of AHB bus cycles; “0000”=1, “0001”=2, “0010”=4, “0011”=8, ...

0 Current state: 0=Idle, 1=Running (read-only)

84.3.5 Scrubber Configuration Register

*Table 1513.*0x14 - CONFIG - Scrubber configuration register

31 16	15 8	7	6	5	4	3 2	1	0
RESERVED	DELAY	IRQD	EC	SERA	LOOP	MODE	ES	SCEN
0	0	0	0	0	0	0	0	0
r	rw	rw	r	rw	rw	rw	rw	rw

31: 16 RESERVED

15: 8 Delay time between processed blocks, in cycles

7 Interrupt when scrubber has finished

6 External clear counter enable

5 Second memory range enable

4 Loop mode, restart scrubber when run finishes

3: 2 Mode (00=Scrub, 01=Regenerate, 10=Initialize, 11=Undefined)

1 External start enable

0 Enable

84.3.6 Scrubber Range Low Address Register

Table 1514. 0x18 - RANGEL - Scrubber range low address register

31 0
SCRUBBER RANGE LOW ADDRESS
0
rw*

31: 0 The lowest address in the range to be scrubbed

The address bits below the burst size alignment are constant ‘0’

84.3.7 Scrubber Range High Address Register

Table 1515. 0x1C - RANGEH - Scrubber range high address register

31	0
SCRUBBER RANGE HIGH ADDRESS	
0	
rw*	

31: 0 The highest address in the range to be scrubbed

The address bits below the burst size alignment are constant ‘1’

84.3.8 Scrubber Position Register

Table 1516. 0x20 - POS - Scrubber position register

31	0
SCRUBBER POSITION	
0	
rw	

31: 0 The current position of the scrubber while active, otherwise zero.

The address bits below the burst size alignment are constant ‘0’

84.3.9 Scrubber Error Threshold Register

Table 1517. 0x24 - ERROR - Scrubber error threshold register

31 22	21 14	13 2	1	0
RECT	BECT	RESERVED	RECTE	BECTE
0	0	0	0	0
rw	rw	r	rw	rw

31: 22 Interrupt threshold value for current scrub run correctable error count

21: 14 Interrupt threshold value for current scrub block correctable error count

13: 2 RESERVED

1 RECTE: Scrub run correctable error count threshold enable

0 BECTE: Scrub block correctable error count threshold enable

84.3.10 Scrubber Initialization Data Register

Table 1518. 0x28 - INIT - Scrubber initialization data register (write-only)

31 0
SCRUBBER INITIALIZATION DATA
-
w

31: 0 Part of data pattern to be written in initialization mode. A write operation assigns the first part of the buffer and moves the rest of the words in the buffer one step.

84.3.11 Scrubber Second Range Low Address Register

Table 1519. 0x2C - RANGEL2 - Scrubber second range low address register

31 0
SCRUBBER RANGE LOW ADDRESS
0
rw*

31: 0 The lowest address in the second range to be scrubbed (if SERA=1)

The address bits below the burst size alignment are constant ‘0’

84.3.12 Scrubber Second Range High Address Register

Table 1520. 0x30 - RANGEH2 - Scrubber second range high address register

31 0
SCRUBBER RANGE HIGH ADDRESS
0
rw*

31: 0 The highest address in the second range to be scrubbed (if SERA=1)

The address bits below the burst size alignment are constant ‘1’

84.4 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x057. For description of vendor and device identifiers see GRLIB IP Library User’s Manual.

84.5 Implementation

84.5.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

84.6 Configuration options

Table 1521 shows the configuration options of the core (VHDL generics).

*Table 1521.*Configuration options

Generic	Function	Allowed range	Default
hmindex	AHB master index	0 - NAHBMST-1	0
hsindex	AHB slave index	0 - NAHBSLV-1	0
ioaddr	AHB slave register area address	0 - 16#FFF#	0
iomask	AHB slave register area address mask	0 - 16#FFF#	16#FFF#
hirq	Interrupt line driven by the core	0 - 16#FFF#	0
nftslv	Number of FT slaves connected to the cerror vector	1 - NAHBSLV-1	3
memwidth	Width of accesses to scrubbed memory slave in bits	32, 64, ..., 1024	AHBDW
burstlen	Length of burst accesses to scrubbed memory slave	2, 4, 8, 16, ...	2
countlen	Length of blocks used for block error count	burstlen x (1,2,4,8 ...)	8

84.7 Signal descriptions

Table 1522 shows the interface signals of the core (VHDL ports).

*Table 1522.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
AHBMI	*	Input	AHB master input signals	-
AHBMO	*	Output	AHB master output signal	-
AHBSI	*	Input	AHB slave input signals	-
AHBSO	*	Output	AHB slave output signals	-
SCRUBI	CERROR	Input	Correctable Error Signals	High
	CLRCOUNT	Input	Clear global error counters	High
	START	Input	External start signal	High

* see GRLIB IP Library User's Manual

84.8 Library dependencies

Table 1523 shows libraries used when instantiating the core (VHDL libraries).

*Table 1523.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AHB signal definitions
GAISLER	MISC	Component	Component declaration

84.9 Instantiation

This example shows how the core can be instantiated.

The example design contains an AMBA bus with a number of AHB components connected to it including the memory scrubber. There are three Fault Tolerant units with EDAC connected to the scrubber's *cerror* vector. The connection of the different memory controllers to external memory is not shown.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.memctrl.all;
use gaisler.misc.all;

entity mctrl_ex is
  port (
    clk : in std_ulogic;
    rstn : in std_ulogic;
    --other signals
    ....
    );
end;

architecture rtl of mctrl_ex is

  -- AMBA bus (AHB and APB)
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbsi : ahb_slv_in_type;
  signal ahbso : ahb_slv_out_vector := (others => ahbs_none);
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);

  -- signals used to connect memory controller and memory bus
  signal memi : memory_in_type;
  signal memo : memory_out_type;

  signal sdo, sdo2: sdctrl_out_type;

  signal sdi : sdctrl_in_type;

  signal aramo : ahbram_out_type;

  -- correctable error vector
  signal scrubi : memscrub_in_type;

begin

  -- AMBA Components are defined here ...

  -- AHB Memory Scrubber and Status Register
  mscrub0 : memscrub
    generic map(hmindex => 4, hsindex => 5, ioaddr => 16#C00#,
                hirq => 11, nftslv => 3);
    port map(rstn, clkm, ahbmi, ahbmo(4), ahbsi, ahbso(5), scrubi);

  scrubi.start <= '0'; scrubi.clrcount <= '0';
  scrubi.cerror(3 to NAHBSLV-1) <= (others => '0');

  --FT AHB RAM
  a0 : ftahbram
    generic map(hindex => 1, haddr => 1, tech => inferred,  kbytes => 64,
                pindex => 4, paddr => 4, edacen => 1, autoscrub => 0,
                errcnt => 1, cntbits => 4)
```

```
    port map(rst, clk, ahbsi, ahbso(1), apbi, apbo(4), aramo);

  scrubi.cerror(0) <= aramo.ce;

  -- SDRAM controller
  sdc : ftsdctrl
    generic map (hindex => 3, haddr => 16#600#, hmask => 16#F00#, ioaddr => 1,
                 fast => 0, pwron => 1, invclk => 0, edacen => 1, errcnt => 1,
                 cntbits => 4)
    port map (rstn, clk, ahbsi, ahbso(3), sdi, sdo);

  stati.cerror(1) <= sdo.ce;

  -- Memory controller
  mctrl0 : ftsrctrl
    generic map (rmw => 1, pindex => 10, paddr => 10, edacen => 1, errcnt => 1,
                 cntbits => 4)
    port map (rstn, clk, ahbsi, ahbso(0), apbi, apbo(10), memi, memo, sdo2);

  scrubi.cerror(2) <= memo.ce;

end;
```

85 MMA - Memory Mapped AMBA bridge

85.1 Overview

The bridge acts as a slave on the memory bus and provides a master interface on the AMBA AHB bus. A read/write access issued towards the slave memory bus interface for the defined memory range is transferred to the AHB master interface and issued on the AMBA bus.

85.2 Operation

85.2.1 Read

Only 32-bit read accesses is allowed for the slave memory interface. When a read access is detected and decoded by the bridge, the bus ready signal is combinatorially deasserted. When corresponding AMBA access is done, the bus ready signal is asserted and the data is driven on the memory bus. When output enable / chip select signal is detected deasserted the data bus is tri-stated.

85.2.2 Write

Only 32-bit write accesses is allowed for the slave memory interface. When a write access is detected and decoded by the bridge, the bus ready signal is combinatorially deasserted. The bus ready signal is reasserted as soon as the write data is stored by the bridge. The bridge can store a write access when the last access has completed on the AMBA bus.

85.3 Default configuration

The default configuration is set by the defcfg signal. The configuration is arranged in the following order:

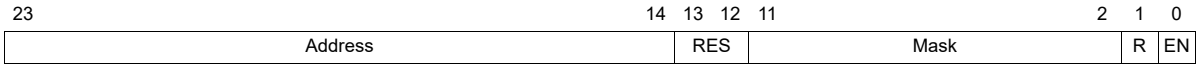
Table 1524.

DEFCFG bits	Configuration
407 - 380	Reconfiguration area
379 - 356	Config for CSN[9]
355 - 332	Config for CSN[8]
331 - 308	Config for CSN[7]
307 - 284	Config for CSN[6]
283 - 260	Config for CSN[5]
259 - 236	Config for CSN[4]
235 - 212	Config for CSN[3]
211 - 188	Config for CSN[2]
187 - 164	Config for CSN[1]
163 - 140	Config for CSN[0]
139 - 126	Address map for CSN[9]
125 - 112	Address map for CSN[8]
111 - 98	Address map for CSN[7]
97 - 84	Address map for CSN[6]
83 - 70	Address map for CSN[5]
69 - 56	Address map for CSN[4]

Table 1524.

DEFCFG bits	Configuration
55 - 42	Address map for CSN[3]
41 - 28	Address map for CSN[2]
27 - 14	Address map for CSN[1]
13 - 0	Address map for CSN[0]

Table 1525. Config for CSN



27: 8 Base memory address for CSN

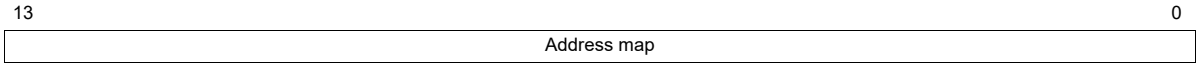
13: 12 Reserved

11: 2 Address mask

1 Reserved

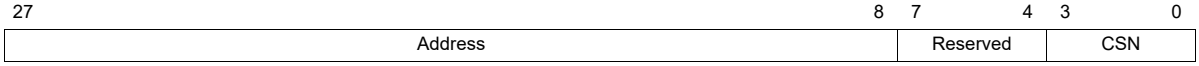
0 CSN enable

Table 1526. Address for CSN



13: 0 Accesses to this CSN are using this address map as bit[31:18] on the AHB bus

Table 1527. Reconfiguration area



27: 8 Base address for the reconfiguration area

7: 4 Reserved

3: 0 The reconfiguration area is located at this CSN

85.4 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x07F. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

85.5 Implementation

85.5.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support *grlib_async_reset_enable*. All registers that react on the reset signal will have a synchronous reset.

85.6 Configuration options

Table 1528 shows the configuration options of the core (VHDL generics).

*Table 1528.*Configuration options

Generic	Function	Allowed range	Default
hindex	AHB master index	0 - NAHBMST-1	0
oepol	Output enable polarity	0 - 1	0
filter	Memory bus signal filtering/sampling	1	1
csnnum	Number of chip selects	1 - 10	1
config	Implement reconfiguration	0 - 1	0

85.7 Signal descriptions

Table 1529 shows the interface signals of the core (VHDL ports).

*Table 1529.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
SCLK	N/A	Input	Not used	-
MMAI	ADDRESS[31:0]	Input	Memory address	High
	CSN[9:0]	Input	Chip select	Low
	DATA[31:0]	Input	Memory data	-
	OEN	Input	Output enable	Low
	WRITEN	Input	Write strobe	Low
	WREN[3:0]	Input	Write enable: WREN[0] corresponds to DATA[31:24], WREN[1] corresponds to DATA[23:16], WREN[2] corresponds to DATA[15:8], WREN[3] corresponds to DATA[7:0].	Low
	READ	Input	Read strobe	High
MMAO	DATA[31:0]	Output	Memory data	High
	DATAOEN[31:0]	Output	Memory data output enable	High/Low
	BRDYN	Output	Bus ready strobe	Low
	BRDYOEN	Output	Bus ready strobe output enable	High/Low
	BEXCN	Output	Bus exception	Low
	BEXCOEN	Output	Bus exception output enable	High/Low
AHBMI	*	Input	AHB master input signals	-
AHBMO	*	Output	AHB master output signals	-
DEFCFG[407:0]		Input	Default configuration	-

* see GRLIB IP Library User's Manual

85.8 Library dependencies

Table 1530 shows libraries used when instantiating the core (VHDL libraries).

*Table 1530.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AHB signal definitions
GAISLER	MMA_PKG	Component	Component declaration

85.9 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.memctrl.all;
use gaisler.misc.all;

entity mctrl_ex is
  port (
     clk : in std_ulogic;
     rstn : in std_ulogic;
    -- memory bus
     address  : in     std_logic_vector(27 downto 0);
     data     : inout std_logic_vector(31 downto 0);
     csn      : in     std_logic_vector(0 downto 0);
     rwen     : in     std_logic_vector(3 downto 0);
     oen      : in     std_logic;
     read     : in     std_logic;
     writen   : in     std_logic;
     brdyn    : out    std_logic;
     bexcn    : out    std_logic;
   --other signals
  ....
    );
end;

architecture rtl of mctrl_ex is

  -- AMBA bus (AHB and APB)
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);

  -- signals used to connect memory controller and memory bus
  signal mmai : mma_in_type;
  signal mmao : mma_out_type;


begin

-- MMA core
mma0 : mma
generic map(
  hindex => 0,
  oepol => 0,
  filter => 1,
  csnnum => 1,
  config => 0)
port map(
  rst => rst,
  clk => clk,
  sclk => '0',
```

```
  mmai => mmai,
  mmao => mmao,
  ahbmi => ahbmi,
  ahbmo => ahbmo(0),
  defcfg => mma_cfgi);

mma_cfgi <= mma_cfg(
  csn0 => mma_csn_cfg(x"2340", x"340", x"FC0", "00", '0', '1'));

-- I/O pads driving data memory bus data signals
  datapads : for i in 0 to 3 generate
      data_pad : iopadv generic map (width => 8)
      port map (pad => data(31-i*8 downto 24-i*8),
                o => mmai.data(31-i*8 downto 24-i*8),
                en => mmao.dataoen(31-i*8 downto 24-i*8),
                i => mmao.data(31-i*8 downto 24-i*8));
  end generate;

  -- connect memory controller outputs to entity output signals
  mmai.address <= address; mmai.csn(0) <= csn(0);
  mmai.oen <= oen; mmai.wren <= rwen;
  mmai.writen <= writen; mmai.read <= read; mmai.iosn <= iosn;
  brdyn <= mmao.brdyn; bexcn <= mmao.bexcn;
end;
```

86 MUL32 - Signed/unsigned 32x32 multiplier module

86.1 Overview

The multiplier module is highly configurable module implementing 32x32 bit multiplier. Multiplier takes two signed or unsigned numbers as input and produces 64-bit result. Multiplication latency and hardware complexity depend on multiplier configuration. Variety of configuration option makes it possible to configure the multiplier to meet wide range of requirements on complexity and performance.

For DSP applications the module can be configured to perform multiply & accumulate (MAC) operation. In this configuration 16x16 multiplication is performed and the 32-bit result is added to 40-bit value accumulator.

86.2 Operation

The multiplication is started when '1' is samples on MULI.START on positive clock edge. Operands are latched externally and provided on inputs MULI.OP1 and MULI.OP2 during the whole operation. The result appears on the outputs during the clock cycle following the clock cycle when MULO.READY is asserted if multiplier if 16x16, 32x8 or 32x16 configuration is used. For 32x32 configuration result appears on the output during the second clock cycle after the MULI.START was asserted.

Signal MULI.MAC shall be asserted to start multiply & accumulate (MAC) operation. This signal is latched on positive clock edge. Multiplication is performed between two 16-bit values on inputs MULI.OP1[15:0] and MULI.OP2[15:0]. The 32-bit result of the multiplication is added to the 40-bit accumulator value on signal MULI.ACC to form a 40-bit value on output MULO.RESULT[39:0]. The result of MAC operation appears during the second clock cycle after the MULI.MAC was asserted.

86.3 Implementation

86.3.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core will use asynchronous reset for all registers if the GRLIB config package setting *grlib_async_reset_enable* is set.

86.3.2 Complexity

Table 1531 shows hardware complexity in ASIC gates and latency for different multiplier configurations.

*Table 1531.*Multiplier latencies and hardware complexity

Multiplier size (multype)	Pipelined (pipe)	Latency (clocks)	Approximate area (gates)
16x16	1	5	6 500
16x16	0	4	6 000
32x8	-	4	5 000
32x16	-	2	9 000
32x32	-	1	15 000

86.4 Configuration options

Table 1532 shows the configuration options of the core (VHDL generics).

*Table 1532.*Configuration options

Generic	Function	Allowed range	Default
tech	Multiplier technolofy selection. If set to 0 the multipliers will be inferred by the synthesis tool. Use this option if your synthesis tool i capable of inferring efficient multiplier implementation.	0 to NTECH-1	0
multype	Size of the multiplier that is actually implemented. All configuration produce 64-bit result with different latencies. 0 - 16x16 bit multiplier 1 - 32x8 bit multiplier 2 - 32x16 bit multiplier 3 - 32x32 bit multiplier	0 to 3	0
pipe	Used in 16x16 bit multiplier configuration. Adds a pipeline register stage to the multiplier. This option gives better timing but adds one clock cycle to latency.	0 to 1	0
mac	Enable multiply & accumulate operation. Use only with 16x16 multiplier option with no pipelining (*pipe* = 0)	0 to 1	0
arch	Multiplier structure 0: Inferred by synthesis tool 1: Generated using Module Generators from NTNU 2: Using technology specific netlists (techspec). Only supported for RTAX-D FPGAs. Other technologies will assert a simulation error. 3: Using Synopsys DesignWare (DW02_mult and DW_mult_pipe)	0 to 3	0
scantest	Enable scan test support. Only required if GRLIB has been changed to use asynchronous reset.	0 - 1	0

86.5 Signal descriptions

Table 1533 shows the interface signals of the core (VHDL ports).

*Table 1533.*Signal declarations

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
HOLDN	N/A	Input	Hold	Low
MULI	OP1[32:0]	Input	Operand 1 OP1[32] - Sign bit. OP1[31:0] - Operand 1 in 2's complement format	High
	OP2[32:0]		Operand 2 OP2[32] - Sign bit. OP2[31:0] - Operand 2in 2's complement format	High
	FLUSH		Flush current operation	High
	SIGNED		Signed multiplication	High
	START		Start multiplication	High
	MAC		Multiply & accumulate	High
	ACC[39:0]		Accumulator. Accumulator value is held externally.	High
MULO	READY	Output	Result is ready during the next clock cycle for 16x16, 32x8 and 32x16 configurations. Not used for 32x32 configuration or MAC operation.	High
	NREADY		Not used	-
	ICC[3:0]		Condition codes ICC[3] - Negative result (not used in 32x32 conf) ICC[1] - Zero result (not used in 32x32 conf) ICC[1:0] - Not used	High
	RESULT[63:0]		Result. Available at the end of the clock cycle if MULO.READY was asserted in previous clock cycle. For 32x32 configuration the result is available during second clock cycle after the MULI.START was asserted.	High
TESTEN	N/A	Input	Test enable (only used together with async. reset)	High
TESTRST	N/A	Input	Test reset (only used together with async. reset)	Low

86.6 Library dependencies

Table 1534 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1534.*Library dependencies

Library	Package	Imported unit(s)	Description
GAISLER	ARITH	Signals, component	Signals, component declaration

86.7 Component declaration

The core has the following component declaration.

```
component mul32
```

```
generic (
    infer   : integer := 1;
    multype : integer := 0;
    pipe    : integer := 0;
    mac     : integer := 0
);
port (
    rst     : in  std_ulogic;
    clk     : in  std_ulogic;
    holdn   : in  std_ulogic;
    muli    : in  mul32_in_type;
    mulo    : out mul32_out_type
);
end component;
```

86.8 Instantiation

This example shows how the core can be instantiated.

The module is configured to implement 16x16 pipelined multiplier with support for MAC operations.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use gaisler.arith.all;

.
.
.

signal muli  : mul32_in_type;
signal mulo  : mul32_out_type;

begin

mul0 : mul32 generic map (infer => 1, multype => 0, pipe => 1, mac => 1)
    port map (rst, clk, holdn, muli, mulo);


end;
```

87 MULTLIB - High-performance multipliers

87.1 Overview

The GRLIB.MULTLIB VHDL-library contains a collection of high-performance multipliers from the Arithmetic Module Generator at Norwegian University of Science and Technology. 32x32, 32x8, 32x16, 16x16 unsigned/signed multipliers are included. 16x16-bit multiplier can be configured to include a pipeline stage. This option improves timing but increases latency with one clock cycle.

87.2 Configuration options

Table 1535 shows the configuration options of the core (VHDL generics).

*Table 1535.*Configuration options

Generic	Function	Allowed range	Default
mulpipe	Include a pipeline stage (0 -pipelining disabled, 1 - pipelining enabled)	0 - 1	0

87.3 Signal descriptions

Table 1536 shows the interface signals of the core (VHDL ports).

*Table 1536.*Signal descriptions

Signal name	Type	Function	Active
CLK (16x16 multiplier only)	Input	Clock	-
HOLDN (16x16 multiplier only)	Input	Hold. When active, the pipeline register is not updates	Low
X[16:0] (16x16 mult) X[32:0] (32x8 mult) X[32:0] (32x16 mult) X[32:0] (32x32 mult)	Input	Operand 1. MBS bit is sign bit.	High
Y[16:0] (16x16 mult) Y[8:0] (32x8 mult) Y[16:0] (32x16 mult) Y[32:0] (32x32 mult)	Input	Operand 2. MSB bit is sign bit.	High
P[33:0] (16x16 mult) P[41:0] (32x8 mult) P[49:0] (32x16 mult) P[65:0] (32x32 mult)		Result. Two MSB bits are sign bits.	High

87.4 Library dependencies

Table 1537 shows libraries used when instantiating the core (VHDL libraries).

*Table 1537.*Library dependencies

Library	Package	Imported unit	Description
GRLIB	MULTLIB	Component	Multiplier component declarations

87.5 Component declaration

The core has the following component declaration.

```
component mul_33_33
  port (
    x    : in  std_logic_vector(32 downto 0);
    y    : in  std_logic_vector(32 downto 0);
    p    : out std_logic_vector(65 downto 0)
  );
end component;
```

87.6 Implementation

87.6.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

87.7 Instantiation

This example shows how the core can be instantiated.

The core is configured to implement 16x16 pipelined multiplier with support for MAC operations.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.multlib.all;

.
.

signal op1, op2 : std_logic_vector(32 downto 0);
signal prod : std_logic_vector(65 downto 0);

begin

m0 : mul_33_33
         port map (op1, op2, prod);

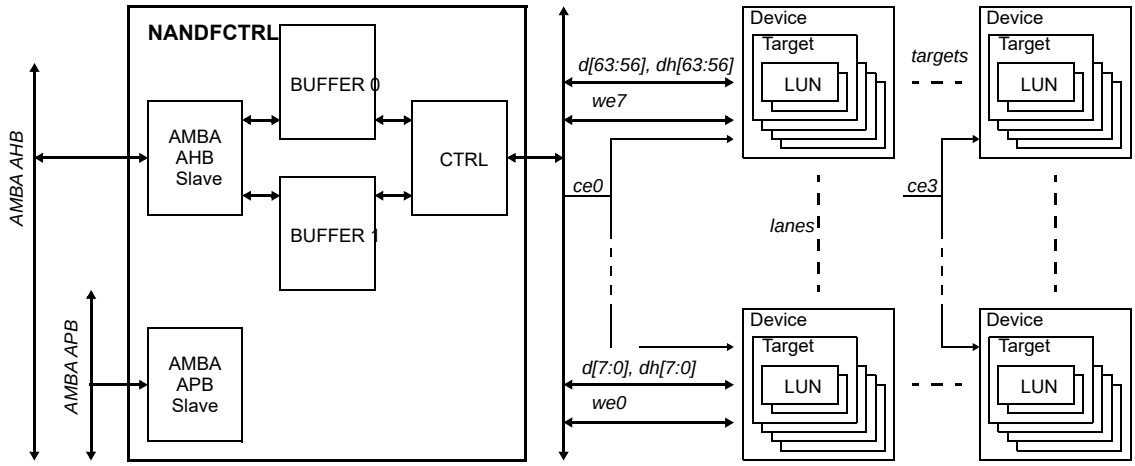
end;
```

88 NANDFCTRL - NAND Flash Memory Controller

88.1 Overview

The NAND Flash Memory Controller (NANDFCTRL) core provides a bridge between external NAND flash memory and the AMBA bus. The memory controller is an Open NAND Flash Interface (ONFI) 2.2 command compliant core (see exceptions below) and it can communicate with multiple parallel flash memory devices simultaneously, where each device in turn can consist of up to four individually addressable targets, one target addressed at a time. The core is configured through a set of AMBA APB registers, described in section 88.4, and data is written to / read from the flash memory by accessing internal buffers mapped over AMBA AHB.

This document mainly describes the NANDFCTRL core's functionality. For details about the actual flash memory interface, flash memory architecture and ONFI 2.2 command set please refer to the *Open NAND Flash Interface specification, revision 2.2*, hereafter called the ONFI 2.2 specification.



Note: One device might have more than one target, using one chip enable signal for each target. This will reduce the number devices that can be placed horizontally in the figure. All devices (and the internal targets) placed vertically in the figure belong to the same chip enable signal, with individual write enable signals controlling each 8-bit/16-bit data lane.

Figure 251. Block diagram

88.2 Operation

88.2.1 System overview

A block diagram of the core can be seen in figure 251. Features and limitations of the core are listed below:

- All commands defined in the ONFI 2.2 standard are supported, except Synchronous Reset and Interleaved Read.
- The core does not implement support for the source synchronous data interface, only asynchronous data interface.
- The core does not place any other limitation on the device architecture other than those specified in the ONFI 2.2 standard. For example, the core does not need to know how many LUNs, blocks, or pages a connected flash memory device has. (See the ONFI 2.2 specification for information about LUNs, blocks, and pages.)
- Multiple parallel data lanes are supported, which gives the possibility to read / write several flash memory devices at the same time.

- To support interleaving of flash memory accesses and AMBA accesses and give greater throughput, two buffers for reading / writing flash memory data are implemented.
- The data interface timing can either be fixed (set at implementation time) or programmable through AMBA APB registers. With fixed data interface timing support for ONFI timing modes 0 - 5 can be implemented and then switched between during run-time. Programmable timing interface allows for clock frequencies unknown at implementation time, as well as custom timing. It is highly recommended to use programmable timing as the additional delays (like I/O timings) might require custom timing options. Read section 88.5 (Timing Modes) for more information.
- The core does not implement any wear-leveling or bad block management.
- The core does not implement any direct access to flash memory devices from the AMBA AHB bus. Instead accesses are performed through two temporary buffers by initiating command and data transfers through control registers via the AMBA APB bus.
- The temporary buffers are mapped into AMBA AHB memory space. Note that the buffer addresses are not directly mapped to the flash memory, but are mapped specific addressing registers. This allows large amount of flash memory to be address, exceeding the 4 Gbyte address space of the AMBA bus.

88.2.2 Internal buffer structure

The number of buffers implemented in the core depends on whether or not the core is implemented with separate buffers for each parallel 8-bit/16-bit data lane or not. This is indicated by the *sepb* field in the *Capability register*. How many data lanes the core implements can be found by reading the *nlane* field of the *Capability register* and adding one. If separate buffers are used then for each data lane there are four different buffers implemented. Two buffers are used for data that are read from / written to any page area in the flash memory device (hereafter called *page buffer*), and the other two are used for data read from / written to any page's spare area (hereafter called *spare buffer*). The size of each page buffer (in bytes) is $2^{\wedge(pbits+1)}$, where pbits is the value of the *pbits* field in the *Capability register*. The size of each spare buffer (in bytes) is $2^{\wedge(sbits+1)}$, where sbits is the value of the *sbits* field in the *Capability register*. If separate buffers aren't used, then the core implements one set of the above mentioned four buffers and uses them for all data lanes.

One page buffer and one spare buffer for each data lane (or all lanes if separate buffers aren't used) are grouped together into what in this document is called *buffer 0*. The other set of page buffers and spare buffers are grouped into *buffer 1*. For example, if the core has support for eight data lanes with separate buffers, and the page buffers are 4096 bytes, and the spare buffers are 256 bytes, then buffer 0 and buffer 1 will each be 32768 + 2048 bytes large. Buffer 0 and buffer 1 are associated with their own set of control registers, described in section 88.4.

Note that support for buffer 1 is optional. Whether or not support for buffer 1 is implemented is indicated by the *b1en* bit in the *Capability register*.

All buffers are mapped into AMBA AHB address space, and the core supports two different mapping schemes, with their own designated AMBA AHB address space:

- For the first address map, called *Consecutive address map*, the first part of the assigned AHB memory area is mapped to the page buffer corresponding to the first 8-bit/16-bit data lane, followed by the page buffer corresponding to the second 8-bit/16-bit data lane etc. After all the page buffers the spare buffers follow in the same manner. See table 1538 for an example with 4096 bytes page buffer and 256 bytes spare buffer and table 1539 for an example with 2048 bytes page buffer and 128 bytes spare buffer.
- For the second address map, called *By page address map*, the first part of the assigned AHB memory area is mapped to the page buffer corresponding to the first 8-bit/16-bit data lane, followed by the spare buffer corresponding to the same data lane. After that follows the page buffer and spare buffer pairs for all other data lanes. Note that since the spare buffers normally are much

smaller than the page buffers there is normally a gap between the last address of a spare buffer and the first address of the next page buffer. The size of the gap is page buffer size - spare buffer size. See table 1540 for an example with 4096 bytes page buffer and 256 bytes spare buffer and see table 1541 for an example with 2048 bytes page buffer and 128 bytes spare buffer.

- See table 1542 for an example which illustrates both *Consecutive address map* and *page address map* for 8192 bytes page buffer and 2048 bytes spare buffer with two lanes, separate buffers and buffer 1 is not implemented.

Note that the page and spare buffer areas might be larger than the size of the page and spare memory implemented in the actual flash memory device. Thus, there might be gaps in the addressing schemes. If the EDAC is implemented (indicated by the *edac* bit in the *Capability register*) then the buffers have an additional AHB address map. Read and write accesses to the additional AHB address space will trigger EDAC operation. This additional address map is also shown in table 1538 and table 1539.

Table 1538. Buffer memory map, consecutive addressing. Example with 4096 B page size, 256 B spare size, separate buffers, both buffer 0 and buffer 1 implemented, and with EDAC.

AMBA AHB offset	address	Contents	AMBA AHB offset	address	Contents
Normal address space (no EDAC operation)			**Normal address space (no EDAC operation)**		
0x00000	0x00FFF	Buffer 0, 4096 byte page data, lane 0	0x10000	0x10FFF	Buffer 1, 4096 byte page data, lane 0
0x01000	0x01FFF	Buffer 0, 4096 byte page data, lane 1	0x11000	0x11FFF	Buffer 1, 4096 byte page data, lane 1
0x02000	0x02FFF	Buffer 0, 4096 byte page data, lane 2	0x12000	0x12FFF	Buffer 1, 4096 byte page data, lane 2
0x03000	0x03FFF	Buffer 0, 4096 byte page data, lane 3	0x13000	0x13FFF	Buffer 1, 4096 byte page data, lane 3
0x04000	0x04FFF	Buffer 0, 4096 byte page data, lane 4	0x14000	0x14FFF	Buffer 1, 4096 byte page data, lane 4
0x05000	0x05FFF	Buffer 0, 4096 byte page data, lane 5	0x15000	0x15FFF	Buffer 1, 4096 byte page data, lane 5
0x06000	0x06FFF	Buffer 0, 4096 byte page data, lane 6	0x16000	0x16FFF	Buffer 1, 4096 byte page data, lane 6
0x07000	0x07FFF	Buffer 0, 4096 byte page data, lane 7	0x17000	0x17FFF	Buffer 1, 4096 byte page data, lane 7
0x08000	0x080FF	Buffer 0, 256 byte spare data, lane 0	0x18000	0x180FF	Buffer 1, 256 byte spare data, lane 0
0x08100	0x081FF	Buffer 0, 256 byte spare data, lane 1	0x18100	0x181FF	Buffer 1, 256 byte spare data, lane 1
0x08200	0x082FF	Buffer 0, 256 byte spare data, lane 2	0x18200	0x182FF	Buffer 1, 256 byte spare data, lane 2
0x08300	0x083FF	Buffer 0, 256 byte spare data, lane 3	0x18300	0x183FF	Buffer 1, 256 byte spare data, lane 3
0x08400	0x084FF	Buffer 0, 256 byte spare data, lane 4	0x18400	0x184FF	Buffer 1, 256 byte spare data, lane 4
0x08500	0x085FF	Buffer 0, 256 byte spare data, lane 5	0x18500	0x185FF	Buffer 1, 256 byte spare data, lane 5
0x08600	0x086FF	Buffer 0, 256 byte spare data, lane 6	0x18600	0x186FF	Buffer 1, 256 byte spare data, lane 6
0x08700	0x087FF	Buffer 0, 256 byte spare data, lane 7	0x18700	0x187FF	Buffer 1, 256 byte spare data, lane 7
EDAC address space (EDAC operation on page buffers)			**EDAC address space (EDAC operation on page buffers)**		
0x20000	0x20FFF	Buffer 0, 4096 byte page data, lane 0	0x30000	0x30FFF	Buffer 1, 4096 byte page data, lane 0
0x21000	0x21FFF	Buffer 0, 4096 byte page data, lane 1	0x31000	0x31FFF	Buffer 1, 4096 byte page data, lane 1
0x22000	0x22FFF	Buffer 0, 4096 byte page data, lane 2	0x32000	0x32FFF	Buffer 1, 4096 byte page data, lane 2
0x23000	0x23FFF	Buffer 0, 4096 byte page data, lane 3	0x33000	0x33FFF	Buffer 1, 4096 byte page data, lane 3
0x24000	0x24FFF	Buffer 0, 4096 byte page data, lane 4	0x34000	0x34FFF	Buffer 1, 4096 byte page data, lane 4
0x25000	0x25FFF	Buffer 0, 4096 byte page data, lane 5	0x35000	0x35FFF	Buffer 1, 4096 byte page data, lane 5
0x26000	0x26FFF	Buffer 0, 4096 byte page data, lane 6	0x36000	0x36FFF	Buffer 1, 4096 byte page data, lane 6
0x27000	0x27FFF	Buffer 0, 4096 byte page data, lane 7	0x37000	0x37FFF	Buffer 1, 4096 byte page data, lane 7
0x28000	0x280FF	Buffer 0, 256 byte spare data, lane 0	0x38000	0x380FF	Buffer 1, 256 byte spare data, lane 0
0x28100	0x281FF	Buffer 0, 256 byte spare data, lane 1	0x38100	0x381FF	Buffer 1, 256 byte spare data, lane 1
0x28200	0x282FF	Buffer 0, 256 byte spare data, lane 2	0x38200	0x382FF	Buffer 1, 256 byte spare data, lane 2
0x28300	0x283FF	Buffer 0, 256 byte spare data, lane 3	0x38300	0x383FF	Buffer 1, 256 byte spare data, lane 3
0x28400	0x284FF	Buffer 0, 256 byte spare data, lane 4	0x38400	0x384FF	Buffer 1, 256 byte spare data, lane 4
0x28500	0x285FF	Buffer 0, 256 byte spare data, lane 5	0x38500	0x385FF	Buffer 1, 256 byte spare data, lane 5
0x28600	0x286FF	Buffer 0, 256 byte spare data, lane 6	0x38600	0x386FF	Buffer 1, 256 byte spare data, lane 6
0x28700	0x287FF	Buffer 0, 256 byte spare data, lane 7	0x38700	0x387FF	Buffer 1, 256 byte spare data, lane 7

Table 1539. Buffer memory map, consecutive addressing. Example with 2048 B page size, 128 B spare size, separate buffers, both buffer 0 and buffer 1 implemented, using sing lane, and with EDAC.

AMBA AHB offset	address	Contents	AMBA AHB offset	address	Contents
Normal address space (no EDAC operation)			**Normal address space (no EDAC operation)**		
0x0000	0x007FF	Buffer 0, 2048 byte page data, lane 0	0x1000	0x17FF	Buffer 1, 2048 byte page data, lane 0
0x0800	0x0087F	Buffer 0, 128 byte spare data, lane 0	0x1800	0x187F	Buffer 1, 128 byte spare data, lane 0
EDAC address space (EDAC operation on page buffer)			**EDAC address space (EDAC operation on page buffer)**		
0x2000	0x27FF	Buffer 0, 2048 byte page data, lane 0	0x3000	0x37FF	Buffer 1, 2048 byte page data, lane 0
0x2800	0x287F	Buffer 0, 128 byte spare data, lane 0	0x3800	0x387F	Buffer 1, 128 byte spare data, lane 0

Table 1540. Buffer memory map, by page addressing. Example with 4096 B page size, 256 B spare size, separate buffers, both buffer 0 and buffer 1 implemented, and with EDAC.

AMBA AHB offset	address	Contents	AMBA AHB offset	address	Contents
Normal address space (no EDAC operation)			**Normal address space (no EDAC operation)**		
0x00000	0x00FFF	Buffer 0, 4096 byte page data, lane 0	0x10000	0x10FFF	Buffer 1, 4096 byte page data, lane 0
0x01000	0x010FF	Buffer 0, 256 byte spare data, lane 0	0x11000	0x110FF	Buffer 1, 256 byte spare data, lane 0
0x02000	0x02FFF	Buffer 0, 4096 byte page data, lane 1	0x12000	0x12FFF	Buffer 1, 4096 byte page data, lane 1
0x03000	0x030FF	Buffer 0, 256 byte spare data, lane 1	0x13000	0x130FF	Buffer 1, 256 byte spare data, lane 1
0x04000	0x04FFF	Buffer 0, 4096 byte page data, lane 2	0x14000	0x14FFF	Buffer 1, 4096 byte page data, lane 2
0x05000	0x050FF	Buffer 0, 256 byte spare data, lane 2	0x15000	0x150FF	Buffer 1, 256 byte spare data, lane 2
0x06000	0x06FFF	Buffer 0, 4096 byte page data, lane 3	0x16000	0x16FFF	Buffer 1, 4096 byte page data, lane 3
0x07000	0x070FF	Buffer 0, 256 byte spare data, lane 3	0x17000	0x170FF	Buffer 1, 256 byte spare data, lane 3
0x08000	0x08FFF	Buffer 0, 4096 byte page data, lane 4	0x18000	0x18FFF	Buffer 1, 4096 byte page data, lane 4
0x09000	0x090FF	Buffer 0, 256 byte spare data, lane 4	0x19000	0x190FF	Buffer 1, 256 byte spare data, lane 4
0x0A000	0x0AFFF	Buffer 0, 4096 byte page data, lane 5	0x1A000	0x1AFFF	Buffer 1, 4096 byte page data, lane 5
0x0B000	0x0B0FF	Buffer 0, 256 byte spare data, lane 5	0x1B000	0x1B0FF	Buffer 1, 256 byte spare data, lane 5
0x0C000	0x0CFFF	Buffer 0, 4096 byte page data, lane 6	0x1C000	0x1CFFF	Buffer 1, 4096 byte page data, lane 6
0x0D000	0x0D0FF	Buffer 0, 256 byte spare data, lane 6	0x1D000	0x1D0FF	Buffer 1, 256 byte spare data, lane 6
0x0E000	0x0EFFF	Buffer 0, 4096 byte page data, lane 7	0x1E000	0x1EFFF	Buffer 1, 4096 byte page data, lane 7
0x0F000	0x0F0FF	Buffer 0, 256 byte spare data, lane 7	0x1F000	0x1F0FF	Buffer 1, 256 byte spare data, lane 7
EDAC address space (EDAC operation on page buffer)			**EDAC address space (EDAC operation on page buffer)**		
0x20000	0x20FFF	Buffer 0, 4096 byte page data, lane 0	0x30000	0x30FFF	Buffer 1, 4096 byte page data, lane 0
0x21000	0x210FF	Buffer 0, 256 byte spare data, lane 0	0x31000	0x310FF	Buffer 1, 256 byte spare data, lane 0
0x22000	0x22FFF	Buffer 0, 4096 byte page data, lane 1	0x32000	0x32FFF	Buffer 1, 4096 byte page data, lane 1
0x23000	0x230FF	Buffer 0, 256 byte spare data, lane 1	0x33000	0x330FF	Buffer 1, 256 byte spare data, lane 1
0x24000	0x24FFF	Buffer 0, 4096 byte page data, lane 2	0x34000	0x34FFF	Buffer 1, 4096 byte page data, lane 2
0x25000	0x250FF	Buffer 0, 256 byte spare data, lane 2	0x35000	0x350FF	Buffer 1, 256 byte spare data, lane 2
0x26000	0x26FFF	Buffer 0, 4096 byte page data, lane 3	0x36000	0x36FFF	Buffer 1, 4096 byte page data, lane 3
0x27000	0x270FF	Buffer 0, 256 byte spare data, lane 3	0x37000	0x370FF	Buffer 1, 256 byte spare data, lane 3
0x28000	0x28FFF	Buffer 0, 4096 byte page data, lane 4	0x38000	0x38FFF	Buffer 1, 4096 byte page data, lane 4
0x29000	0x290FF	Buffer 0, 256 byte spare data, lane 4	0x39000	0x390FF	Buffer 1, 256 byte spare data, lane 4
0x2A000	0x2AFFF	Buffer 0, 4096 byte page data, lane 5	0x3A000	0x3AFFF	Buffer 1, 4096 byte page data, lane 5
0x2B000	0x2B0FF	Buffer 0, 256 byte spare data, lane 5	0x3B000	0x3B0FF	Buffer 1, 256 byte spare data, lane 5
0x2C000	0x2CFFF	Buffer 0, 4096 byte page data, lane 6	0x3C000	0x3CFFF	Buffer 1, 4096 byte page data, lane 6
0x2D000	0x2D0FF	Buffer 0, 256 byte spare data, lane 6	0x3D000	0x3D0FF	Buffer 1, 256 byte spare data, lane 6
0x2E000	0x2EFFF	Buffer 0, 4096 byte page data, lane 7	0x3E000	0x3EFFF	Buffer 1, 4096 byte page data, lane 7
0x2F000	0x2F0FF	Buffer 0, 256 byte spare data, lane 7	0x3F000	0x3F0FF	Buffer 1, 256 byte spare data, lane 7

Table 1541. Buffer memory map, by page addressing. Example with 2048 B page size, 128 B spare size, separate buffers, both buffer 0 and buffer 1 implemented, using sing lane, and with EDAC.

AMBA AHB offset	address	Contents
Normal address space (no EDAC operation)		
0x0000	0x007FF	Buffer 0, 2048 byte page data, lane 0
0x0800	0x0087F	Buffer 0, 128 byte spare data, lane 0
EDAC address space (EDAC operation on page buffer)		
0x2000	0x27FF	Buffer 0, 2048 byte page data, lane 0
0x2800	0x287F	Buffer 0, 128 byte spare data, lane 0

AMBA AHB offset	address	Contents
Normal address space (no EDAC operation)		
0x1000	0x17FF	Buffer 1, 2048 byte page data, lane 0
0x1800	0x187F	Buffer 1, 128 byte spare data, lane 0
EDAC address space (EDAC operation on page buffer)		
0x3000	0x37FF	Buffer 1, 2048 byte page data, lane 0
0x3800	0x387F	Buffer 1, 128 byte spare data, lane 0

Table 1542. Buffer memory map, by consecutive addressing and by page addressing. Example with 8192B page size, 2048 B spare size, separate buffers, only buffer 0 implemented, and with EDAC.

CONSECUTIVE ADDRESSING

AMBA AHB offset	address	Contents
Normal address space (no EDAC operation)		
0x00000	0x01FFF	Buffer 0, 8192 byte page data, lane 0
0x02000	0x03FFF	Buffer 0, 8192 byte page data, lane 1
0x04000	0x047FF	Buffer 0, 2048 byte spare data, lane 0
0x04800	0x04FFF	Buffer 0, 2048 byte spare data, lane 1
EDAC address space (EDAC operation on page buffer)		
0x10000	0x11FFF	Buffer 0, 8192 byte page data, lane 0
0x12000	0x13FFF	Buffer 0, 8192 byte page data, lane 1
0x14000	0x147FF	Buffer 0, 2048 byte spare data, lane 0
0x14800	0x14FFF	Buffer 0, 2048 byte spare data, lane 1

PAGE ADDRESSING

AMBA AHB offset	address	Contents
Normal address space (no EDAC operation)		
0x00000	0x01FFF	Buffer 0, 8192 byte page data, lane 0
0x02000	0x027FF	Buffer 0, 2048 byte spare data, lane 0
0x04000	0x05FFF	Buffer 0, 8192 byte page data, lane 1
0x06000	0x067FF	Buffer 0, 2048 byte spare data, lane 1
EDAC address space (EDAC operation on page buffer)		
0x10000	0x11FFF	Buffer 0, 8192 byte page data, lane 0
0x12000	0x127FF	Buffer 0, 2048 byte spare data, lane 0
0x14000	0x15FFF	Buffer 0, 8192 byte page data, lane 1
0x16000	0x167FF	Buffer 0, 2048 byte spare data, lane 1

88.2.3 Data interface timing

The ONFI timing parameters that the core explicitly handles are:

- tCCS - Change Column setup time
- tADL - ALE to data loading time
- tCS - CE setup time
- tRP - RE pulse width
- tREH - RE high hold time (starting from REV. 2)
- tRR - Ready to RE low (data only)
- tWP - WE pulse width
- tWB - WE high to SR[6] low
- tRHW - RE high to we WE low
- tWH - WE high hold time
- tWHR - WE high to RE low
- tWW - WP transition to WE low

All other timing requirements are either fulfilled through design, or are handled by the flash memory devices. See the ONFI specification for details about the different timing parameters.

The data interface timing can be either fixed (set at implementation time) or programmable to allow both system clock frequencies unknown at implementation time as well as custom timing parameters.

When the timing is fixed all timing parameters are calculated on implementation time based on the specified system clock frequency. When programmable timing is used the timing parameters are programmed through AMBA APB registers, described in section 88.4. The registers power-up / reset values are set at implementation time.

Note that the timing parameter tCCS is always programmable, even if fixed timing is used for all other parameters. This is because the ONFI specification says that after initialization is complete, the value for tCCS specified in the flash memory's parameter page should be used.

88.2.4 Accessing the NAND flash memory devices

The steps that need to be taken to access (i.e. send an ONFI 2.2 command to) the flash memory devices are:

1. Make sure that the chosen buffer is not busy by checking the *run* and *bsy* bits in the *Buffer control / status* register. If both the *run* bit and *bsy* bits are set then the core is currently executing a command associated with that buffer, and the buffer can not be used. If only the *bsy* bit is set then the core is done executing a command but the corresponding data buffer and control bits are still write protected. Software then needs to clear the *bsy* bit by writing '1' to it.

2. If the command requires a row address to be sent, write it to the *Buffer row address register*. Otherwise this step can be skipped.

3. If the command requires a column address to be sent, write it to the *coladdr* field of the *Buffer column address register*. Bits 7:0 of the *coladdr* field also need to be written with the one byte address used for SET FEATURES, GET FEATURES, READ ID, READ UNIQUE ID, and READ PARAMETER PAGE commands. Otherwise this step can be skipped.

4. Write the command value to the *Buffer command register*, and possibly set the control bits *sel*, *cd*, or *sc2* if needed. See table 1550 in section 88.4 for a description of these bits.

5. If the command should include a data phase then set the size of the data by writing to the *size* field of the *Buffer column address register*. This step is not necessary for the SET FEATURES, GET FEATURES, READ STATUS, and READ STATUS ENHANCED commands since they always have a fixed size data phase.

6. If data should be written to the flash memory devices then write this data to the corresponding buffers. Note that the core uses the *coladdr* field in the *Buffer column address register* to index into the buffers, which means that data that should be written with an offset into a flash memory page (i.e. column address is not zero) need to be written with the same offset into the buffers. The exception is the commands mentioned in step 3. They always read from the beginning of the buffers. This step can be skipped if no data are to be written.

7. Select which data lanes and targets the command should be sent to, if an interrupt should be generated when the command is finished, and start execution by writing to the *lanesel*, *targsel*, *irqmsk*, and *exe* bits in the *Buffer control / status register*. See table 1551 in section 88.4 for a description of these bits.

Once command execution has been started software can monitor the *run* bit in the *Buffer control / status register* (or wait for an interrupt if the core was configured to generate one) to learn when the command is finished. If data was read from the flash memory then it can be found in the buffers. Note that the core uses the *coladdr* field in the *Buffer column address register* to index into the buffers, which means that data that was read from a flash memory page with an offset (i.e. column address is not zero) was written into the buffers with the same offset. The exception are the commands mentioned in step 3. They always place their data in the beginning of the buffers.

88.2.5 Endianness

The core is designed for big-endian systems.

88.3 EDAC

88.3.1 EDAC operation

The optional NAND Flash Memory controller EDAC automatically encode and decode data being stored in the NAND Flash memory with an error correcting code. The *edac* bit in the *Capability* register shows if the EDAC is implemented or not. If implemented, the EDAC is enabled by setting the *edacen* bit in the *Core control* register. Optional AHB error responses can be generated upon an uncorrectable error by setting the *ahberren* bit in the same register. See section 88.4 for more information.

The checksum of the code is calculated and stored for each word that is written, via the AMBA interface, into the page data part of the buffer, and automatically stored in parallel in the spare data part of the buffer. For each word of data written, one byte is stored. Note that data must be written into the EDAC part of the AHB address space. Data written to the non EDAC part of the address space does not trigger EDAC operation. See section 88.2.2 for information about the buffer memory map. Halfword and byte writes are not supported when the EDAC is enabled.

Since the number of spare bytes normally is less than what is sufficient to protect the full page data, the page data size is limited by the programmable *lpaddr* field in the *Core control* register. The *lpaddr* field defines how much user data (i.e. page data) is to be used, with the remaining part of the page data and spare data being used for checksums. Note that the spare data buffer portion is therefore made bigger than the actual spare data in the NAND Flash memory. When the NAND Flash memory is written, the data will be fetched first from the page data buffer up to *lpaddr*, and then the rest will be fetched from the spare data buffer. Errors can be detected in the underlying buffer memory when reading them as part of the write operation to the NAND Flash memory.

The reverse applies to when data is fetched from the NAND Flash memory during read. When the buffer contents are read out, via the AMBA interface, each read page data word is automatically corrected using the corresponding spare buffer checksum byte. Two levels of errors can occur, errors stemming from the underlying buffer memory protection, or errors stemming from the EDAC protecting the NAND Flash memory contents. All error flags are described in the *Core status* register.

It is possible to write or read additional dummy words to the page data buffer past the LPADDR address. This can be used to handle any surplus spare data bytes.

The memory contents are protected by means of a Bose Chaudhuri Hocquenghem (BCH) type of code. It is a Quad Error Correction/Quad Error Detection (QEC/QED) code.

The data symbols are 4-bit wide, represented as GF(2^4). The has the capability to detect and correct a single symbol error anywhere in the codeword.

88.3.2 Code

The code has the following definition:

- there are 4 bits per symbol; most significant has index 3 (to the left), least significant has index 0
- there are 17 symbols per codeword, of which 2 symbols represent the checksum;
- the code is systematic;
- the code can correct one symbol error per codeword;
- the field polynomial is

$$f(x) = x^4 + x + 1$$

- all multiplications are performed as Galois Field multiplications over the above field polynomial
- all additions/subtractions are performed as Galois Field additions (i.e. bitwise exclusive-or)

Note that only 4 of the 17 symbols are used for data, 2 symbols are used for the checksum, and the reset are not used, the code is thus shortened by 11 symbols.

88.3.3 Encoding

- a codeword is defined as 17 symbols:

  $[c_0, c_1, c_2, c_3, c_4, c_5, c_6, c_7, c_8, c_9, c_{10}, c_{11}, c_{12}, c_{13}, c_{14}, c_{15}, c_{16}]$

  where c_0 to c_{14} represent information symbols and c_{15} to c_{16} represent check symbols.
- c_{15} is calculated as follows

$$c_{15} = \sum_{0}^{14}(k_i \times c_i)$$

- c_{16} is calculated as follows

$$c_{16} = \sum_{0}^{14} c_i$$

- where the constant vector k is defined as:

  k_0=0xF, k_1=0xE, .., k_{14}=0x1 (one can assume k_{15}=0x1 and k_{16}=0x1 for correction purposes)
- bit 1 of c_{15}, and bits 3 and 1 of c_{16} are inverted after encoded

88.3.4 Decoding

- the corrupt codeword is defined as 17 symbols:

  $[r_0, r_1, r_2, r_3, r_4, r_5, r_6, r_7, r_8, r_9, r_{10}, r_{11}, r_{12}, r_{13}, r_{14}, r_{15}, r_{16}]$
- the corrupt codeword can also be defined as 17 uncorrupt symbols and an error:

  $[c_0, c_1, c_2, c_3, c_4, c_5, c_6, c_7, c_8, c_9, c_{10}, c_{11}, c_{12}, c_{13}, c_{14}, c_{15}, c_{16}] + [e_x]$

  where the error is defined as e_x, e being the unknown magnitude and
  x being the unknown index position in the codeword
- recalculated checksum rc_0 is calculated as follows (k_i is as defined above, x being the unknown index)

$$rc_0 = \sum_{0}^{14}(k_i \times r_i) = \sum_{0}^{14}(k_i \times c_i) + (k_x \times e_x)$$

- recalculated rc_1 is calculated as follows

$$rc_1 = \sum_{0}^{14} r_i = \sum_{0}^{14} c_i + e_x$$

- syndrome s_0 is calculated as follows

$$s_0 = rc_0 + r_{15} = \sum_{0}^{14}(k_i \times r_i) + \sum_{0}^{14}(k_i \times c_i) = k_x \times e_x$$

- syndrome s_1 is calculated as follows, which gives the magnitude (not applicable to c_{15} and c_{16})

$$s_1 = rc_1 + r_{16} = \sum_{0}^{14} r_i + \sum_{0}^{14} c_i = e_x$$

- in case s_0 and s_1 are both non-zero, to located the error in range c_0 to c_{14}, multiply error magnitude e_x with each element of the constant vector defined above:

$$k_i e_x = k_i \times s_1 = k_i \times e_x \qquad i = [0,14]$$

- search the resulting vector to find the element matching syndrome s_0, the resulting index i points to the error location (applicable only to i in [0, 14])

$$k_i e_x \Leftrightarrow k_i \times e_x$$

- finally perform the correction (applicable only to i in [0, 14])

$$c_i = r_i - s_1 = r_i - e_x = (c_i - e_x) \times e_x = c_i - e_x + e_x = c_i$$

- when s_0 is zero and s_1 is non-zero, the error is located in checksum r_{15}, no correction is necessary
- when s_1 is zero and s_0 is non-zero, the error is located in checksum r_{16}, no correction is necessary
- when s_0 and s_1 are both zero, no error has been detected, no correction is necessary
- bit 1 of r_{15}, and bits 3 and 1 of r_{16} are inverted before decoded

88.4 Registers

The core is programmed through registers mapped into APB address space. Vendor and device identifier

*Table 1543.*NANDFCTRL registers

APB address offset	Register
0x00	Core control register
0x04	Core status register
0x08	Interrupt pending register
0x0C	Capability register
0x10	Buffer 0 row address register
0x14	Buffer 0 column address register
0x18	Buffer 0 command register
0x1C	Buffer 0 control / status register
0x20*	Buffer 1 row address register
0x24*	Buffer 1 column address register
0x28*	Buffer 1 command register
0x2C*	Buffer 1 control / status register
0x30	Programmable timing register 0
0x34**	Programmable timing register 1
0x38**	Programmable timing register 2
0x3C**+	Programmable timing register 3

* Only present if buffer 1 registers are implemented. Indicated by *b1en* bit in *Capability register*.

** Only present if programmable timing is implemented. Indicated by *prgt* bit in *Capability register*.

+ Present starting from the revision 2 of the core.

Note: The Buffer 0 and Buffer 1 registers are identical, and therefore only one set of tables describing the registers are presented below.

*Table 1544.*0x00 - CTRL - Core control register

31	16
LPADDR	
0xFFFF	
rw	

15 13	12	11	10	9	8	7	6	5	4 3 2	1	0
R	DW	CMDO	R	AHBERREN	EDACEN	R	EDO	ABORT	TMODE	WP	RST
0	0	*	0	0	0	0	0	0	0	1	0
r	rw*	rw	r	rw	rw*	r	rw*	rw*	rw*	rw	rw

31:16 Last page address (LPADDR) - This field should be set to the last addressable byte in a flash memory page, not including the spare area. The core uses these bits to know when to switch to the internal buffers for the page's spare area. For example: If the flash memory devices have a page size of 4096 bytes (and an arbitrary sized spare area for each page) this field should be set to 0xFFF (= 4095). The actual number of bits used for this field depends on the size of the implemented buffers. The number of bits can be found by reading the *pbits* field of the *Capability register* and adding one. Reset value: 0xF..F

15:13 Reserved (R) - Always reads zero.

12 Data width (DW) - Sets the default data lane width. 0 = Core uses 8-bit data lanes. 1 = Core uses 16-bit data lanes. This can be overridden for individual commands by setting the *dwo* bit in the *Buffer command* register. This bit is only available if the *dw16* bit in the *Capability register* is 1. Reset value 0.

11 Command bit order (CMDO) - When this bit is set to 0 the ONFI command bytes are mapped to the core's data lane(s) as follows: Cmd bit 0 -> Data lane bit 7, Cmd bit 1 -> Data lane bit 6., and so on.

When this bit is set to 1 the commands are mapped as follows: Cmd bit 0 -> Data lane bit 0, Cmd bit 1 -> Data lane bit 1, and so on. Reset value equals the value of the *cmdo* bit in the *Capability register*.

10 Reserved (R) - Always reads zero.

9 AHB error response generation (AHBERREN) - If this bit is set then the core will generate an AMBA error response if the EDAC detects an uncorrectable error, or if the fault tolerance logic for the internal buffers report and uncorrectable error, upon and AHB read. If this bit is not set when an uncorrectable error is detected, the core's output signal *error* is set high for one clock cycle instead. This bit is only present when the EDAC is implemented or when the internal buffers are implemented with either byte parity and DMR or only byte parity. The *ft* bits in the *Capability register* shows which fault tolerance that is implemented, and the *edac* bit in the *Capability register* shows if EDAC is implemented. Reset value 0.

8 EDAC enable (EDACEN) - When this bit is set the EDAC is enabled. This bit is only present when the EDAC is implemented. The *edac* bit in the *Capability register* shows if EDAC is implemented or not. Reset value 0.

7 Reserved (R) - Always reads zero.

6 EDO data output (EDO) - If programmable timing is implemented (indicated by the *prgt* field in the *Capability register*) then this bit should be set if EDO data output cycles should be used. See ONFI 2.2 Specification for more information. If programmable timing is not implemented then this bit is read-only. When programmable timing is not implemented the EDO is only enabled when timing mode 5 is selected and tm5_edoen generic is set to 1.

5 Command abort (ABORT) - This bit can be set to 1 to abort a command that for some reason has put the core in a dead lock waiting for the *rb* input signal to go high. This could happen for example if a program or erase command was issued while the memory was in write protect mode. This bit is automatically cleared by the core. Reset value 0. Only available if the *rev* field in the *Capability register* > 0, otherwise always 0.

4:2 Timing mode (TMODE) - If programmable timing is not implemented (indicated by the *prgt* field in the *Capability register*) then writing this field changes the core's internal timing mode. See ONFI 2.2 Specification for more information on the different timing modes. Note that in order to change timing mode on the flash memory devices a SET FEATURES command needs to be issued. This is not done automatically when writing these bits. Timing mode 0 i always supported. Additional supported timing modes is indicated by the *tm[5:1]* bits in the *Capability register*. Should not be written while a command is in progress. Note that if this field is written with a value matching a timing mode that is not supported, then the core will operate in timing mode 0 (even though this field still changes to the invalid value). If programmable timing is implemented then this field is not present. Reset value: 0b000

*Table 1544.*0x00 - CTRL - Core control register

1 Write protect (WP) - When this bit is set to 1 the core puts the flash memory devices in write protect mode by asserting the *wp* signal. In write protect mode, the memories won't respond to PROGRAM or ERASE commands. If the core is active when software writes this bit there is a delay before the actual write protect signal goes low. Software can use the *wp* field in the *Core status register* to see when the signal has changed value. Reset value: 1

0 Software reset (RST) - If software writes this bit to 1 the core is reset, and a RESET (0xFF) command is issued to all targets on all attached flash memory devices. The only difference between a software reset and a hardware reset / power up is that the core does not reset it's *tmode* field (described above) nor the *Programmable timing registers* during software reset. The reason for this is that the flash memory devices does not change timing mode after receiving a RESET command. This bit is cleared automatically. Reset value: 0

*Table 1545.*0x04 - STAT - Core status register (read only)

31 … 24	23 22	21 20	19 18	17 16
R	FTNERRFLAGS	R	FTAERRFLAGS	R
0	0	0	0	0
r	wc*	r	wc*	r

15 12	11 9	8 … 4	3 2	1	0
EERRFLAGS	R	STATE	R	WP	RDY
0	0	0	0	1	0
wc*	r	r	r	r	r

31:24 Reserved (R) - Always reads zero.

23:22 Fault tolerance error flags on NAND side (FTNERRFLAGS) - The bits in this field indicates the following errors:

Bit 22: Uncorrectable error in buffer 0.

Bit 23: Uncorrectable error in buffer 1.

If the fault tolerance logic for the internal buffers indicates an error when the buffers are read during a NAND flash write operation the corresponding error flag in this register is set. These bits can be cleared by writing a 1 to them. The error flag for each buffer is also automatically cleared when an AHB write access occurs to that buffer (independent of address). These bits are only present when the internal buffers are implemented with either byte parity and DMR or only byte parity. The *ft* bits in the *Capability register* shows which fault tolerance that is implemented. Reset value 0.

21:20 Reserved (R) - Always reads zero.

19:18 Fault tolerance error flags on AHB side (FTAERRFLAGS) - The bits in this field indicates the following errors:

Bit 18: Uncorrectable error in buffer 0.

Bit 19: Uncorrectable error in buffer 1.

If the fault tolerance logic for the internal buffers indicates an error when the buffers are read over AHB the corresponding error flag in this register is set. These bits can be cleared by writing a 1 to them. The error flag for each buffer is also automatically cleared when an AHB read access occurs to that buffer with an address which is at offset 0 in the page data buffer for any data lane. For example, if the core is configured with four data lanes and 4096 byte large page buffers, then an AHB read access with offsets 0x0000, 0x1000, 0x2000, and 0x3000 (with consecutive address scheme) would reset the error flag for buffer 0. These bits are only present when the internal buffers are implemented with either byte parity and DMR or only byte parity. The *ft* bits in the *Capability register* shows which fault tolerance that is implemented.

When these bits get set then the core's output signal *err* is also set high for one clock cycle, if the *ahberren* bit in the *Core control* register is not set.

Reset value 0.

17:16 Reserved (R) - Always reads zero.

*Table 1545.*0x04 - STAT - Core status register (read only)

15:12	EDAC error flags (EERRFLAGS) - The different bits indicate the following errors: Bit 12: Correctable error in buffer 0. Bit 13: Correctable error in buffer 1. Bit14: Uncorrectable error in buffer 0. Bit 15: Uncorrectable error in buffer 1. If the EDAC detects an error while an internal buffer is being read over AHB the corresponding error flag in this register is set. These bits can be cleared by writing a 1 to them. The error flags for each buffer are also automatically cleared when an AHB read access occurs to that buffer with an address which is at offset 0 in the page data buffer for any data lane. For example, if the core is configured with four data lanes and 4096 byte large page buffers, then an AHB read access with offsets 0x0000, 0x1000, 0x2000, and 0x3000 (with the consecutive address scheme) would reset the error flag for buffer 0. These bits are only present when the EDAC is implemented. The *edac* bit in the *Capability register* shows if EDAC is implemented or not. When the correctable error status bits get set then the core's output signal *err* is also set high for one clock cycle. The *err* output is also set for one cycle if the error flags for uncorrectable errors get set and the *ahberren* bit in the *Core control* register is not set. Reset value 0x0.
11:9	Reserved (R) - Always reads zero.
8:4	Core state - Shows the core's internal state. Implemented for debugging purposes. 0 = reset, 1-2 = idle, 3-8 = command state, 9-11 = address state, 12-15 = data in state, 16-18 = data out state, 19-31 = unused.
3:2	Reserved (R) - Always reads zero.
1	Write protect (WP) - Shows if the flash memory devices are in write protect mode or not. 0 = Not in write protect mode. 1 = In write protect mode. Reset value: 1
0	Core ready (RDY) - After a power up / reset this bit will be cleared. Once the core is done with it's reset procedure (waiting for ready signal from all flash memory devices and issuing a RESET command) this bit is set to 1. Reset value: 0

*Table 1546.*0x08 - IPEND - Interrupt pending register

31 … 2	1	0
R	B1IRQ	B0IRQ
0	0	0
r	wc	wc

31:2	Reserved (R) - Always reads zero.
1	Buffer 1 interrupt (B1IRQ) - This bit is set to one when an interrupt linked to buffer 1 is generated. Software can clear this bit by writing 1 to it. Only present if the *b1en* bit in the *Capability register* indicates that buffer 1 is implemented. Reset value: 0
0	Buffer 0 interrupt (B0IRQ) - This bit is set to one when an interrupt linked to buffer 0 is generated. Software can clear this bit by writing 1 to it. Reset value: 0

*Table 1547.*0x0C - CAP - Capability register (read only)

15 14	13 10	9	8	7	6	5	4 2	1 0
SBITS	PBITS	TM5	TM4	TM3	TM2	TM1	NLANES	NTARGS
*	*	*	*	*	*	*	*	*
r	r	r	r	r	r	r	r	r

31 28	27	26	25	24	23 22	21	20	19	18	17 16
REV	R	PRGT	SEPB	CMDO	FT	R	B1EN	EDAC	DW16	SBITS
*	0	*	*	*	*	0	*	*	*	‘
r	r	r	r	r	r	r	r	r	r	r

31:28 Revision (REV) - Indicates the revision of the core.

27 Reserved (R) - Always reads zero.

26 Programmable timing (PRGT) - 0 = Data interface timing is set at implementation time and not programmable. 1 = Data interface timing is programmable (only reset values are set at implementation time). Reflects value of VHDL generic *progtime*.

25 Separate buffers (SEPB) - Indicates if the buffers for the data lanes are shared or separate. 0 = All data lanes share buffers. 1 = All data lanes have their own buffers. When 0 a command with a data in phase should only be issued to one target and lane. A command with a data out phase can still be issued to several lanes but with the limitation that the same data will be sent to all lanes. When set to 1 several lanes can be read at the same time, and lanes can be written with individual data simultaneously. Reflects value of VHDL generic *sepbufs*.

24 Command bit order (CMDO) - Indicates the reset value for the *cmdo* bit in the *Core control register*. Reflects value of VHDL generic *cmdorder*.

23:22 Fault tolerant buffers (FT) - These bits indicate if the internal buffers in the core is implemented with fault tolerance. 0b00 = no fault tolerance, 0b01 = Byte parity DMR, 0b10 = TMR, 0b11 = Byte parity, no DMR. Reflects value of VHDL generic *ft*.

21 Reserved (R) - Always reads zero.

20 Buffer 1 enabled (B1EN) - If this bit is 1 then the core implements both buffer 0 and buffer 1, otherwise only buffer 0 is implemented. See section 88.2.2 for more information about the buffer structure. Reflects value of VHDL generic *b1en*.

19 EDAC support (EDAC) - If this bit is 1 then the core implements error detection and correction on data read from the NAND flash memory. See section 88.3 for details. Reflects value of VHDL generic *edac*.

18 16-bit memory support (DW16) - If this bit is 0 the core only support 8-bit memories. If this bit is 1 the core support both 8-bit and 16-bit memories. Only available if the *rev* field > 0, otherwise always 0. Reflects value of VHDL generic *dwidth16*.

17:14 Spare area buffer address bits (SBITS) - This field indicates how many address bits that are implemented for the buffers for the pages spare area. Add one to the value of this field to get the number of bits. The size of the buffers are $2^{(SBITS+1)}$ Reflects value of VHDL generic *sbufsize*.

13:10 Page buffer address bits (PBITS) - This field indicated how many address bits that are implemented for the page buffers. Add one to the value of this field to get the number of bits. The size (in bytes) of the buffers are $2^{(PBITS+1)}$ Reflects value of VHDL generic *pbufsize*.

9 Timing mode 5 support (TM5) - If the core does not support programmable timing (indicated by *prgt* bit described above) then this bit is 1 if the core supports timing mode 5. If programmable timing is implemented, or if the core does not support timing mode 5 then this bit is 0. Reflects value of VHDL generic *tm5*.

8 Timing mode 4 support (TM4) - If the core does not support programmable timing (indicated by *prgt* bit described above) then this bit is 1 if the core supports timing mode 4. If programmable timing is implemented, or if the core does not support timing mode 4then this bit is 0. Reflects value of VHDL generic *tm4*.

7 Timing mode 3 support (TM3) - If the core does not support programmable timing (indicated by *prgt* bit described above) then this bit is 1 if the core supports timing mode 3. If programmable timing is implemented, or if the core does not support timing mode 3then this bit is 0. Reflects value of VHDL generic *tm3*.

*Table 1547.*0x0C - CAP - Capability register (read only)

6	Timing mode 2 support (TM2) - If the core does not support programmable timing (indicated by *prgt* bit described above) then this bit is 1 if the core supports timing mode 2. If programmable timing is implemented, or if the core does not support timing mode 2then this bit is 0. Reflects value of VHDL generic *tm2*.
5	Timing mode 1 support (TM1) - If the core does not support programmable timing (indicated by *prgt* bit described above) then this bit is 1 if the core supports timing mode 1. If programmable timing is implemented, or if the core does not support timing mode 1 then this bit is 0. Reflects value of VHDL generic *tm1*.
4:2	Number of flash memory devices (NLANES) - This field indicates how many 8-bit/16-bit data lanes (minus one) the core can access, i.e. number of write enable signals. A write enable signal can be connected to one or more targets (i.e. one or more flash memory devices). Reflects value of VHDL generic *nlanes*.
1:0	Number of targets per device (NTARGS) - This field indicates how many individual targets (minus one) the core can access, i.e. number of chip enable signals. A flash memory device can have one or more targets, each with an individual chip enable signal. Reflects value of VHDL generic *ntargets*.

*Table 1548.*0x10,0x20 - ROW - Buffer row address register

31 24	23 0
R	ROWADDR
0	NR
r	rw*

31:24	Reserved (R) - Always reads zero.
23:0	Row address (ROWADDR) - This field sets the three byte row address, which is used to address LUNs, blocks and pages. As described in the ONFI 2.2 specification the least significant part of the row address is the page address, the middle part block address, and the most significant part is the LUN address. Exactly how many bits that are used for each part of the address depends on the architecture of the flash memory. Software needs to write this field prior to issuing any command that has an address phase that includes the row address. The core ignores this field if the command doesn't use the row address. This field can only be written if the *bsy* bit in the *Buffer control / status register* is zero.

*Table 1549.*0x14,0x24 - COL - Buffer column address register

31 16	15 0
SIZE	COLADDR
NR	NR
rw*	rw*

31:16	Command data size (SIZE) - If a command has a data out or data in phase then software needs to set this field to the size of the data that should be read / written. Software does not need to set this field for the commands SET FEATURES, GET FEATURES, READ STATUS, or READ STATUS ENHANCED their data phases are always the same size. The core also ignores this field if the command issued doesn't have a data phase, as for example BLOCK ERASE. The actual number of bits used for this field depends on the size of the implemented buffers. The number of bits can be found by reading the *pbits* field of the *Capability register* and adding one. This field can only be written if the *bsy* bit in the *Buffer control / status register* is zero.
15:0	Column address (COLADDR) - This field sets the two byte column address, which is used to address into a flash memory page. See the ONFI 2.2 specification for more information about column address. Software needs to write this field for those commands that have an address phase that includes the column address, as well as for those special commands that only have a one byte address phase (SET FEATURES; GET FEATURES; READ ID, READ UNIQUE ID, and READ PARAMETER PAGE). The core uses this field as an offset into the buffers when reading / writing data. The exception is the one byte address commands mentioned above, which always store their data in the beginning of the buffers. This field is ignored by the core if the command only uses the row address. This field can only be written if the *bsy* bit in the *Buffer control / status register* is zero.

*Table 1550.*0x18, 0x28 - CMD - Buffer command register

31 21	20	19	18	17	16	15 8	7 0
RESERVED	DWO	R	SEL	SC2	CD	CMD2	CMD1
0	0	0	NR	NR	NR	NR	NR
r	rw*	r	rw*	rw*	rw*	rw*	rw*

31:21 Reserved (R) - Always reads zero.

20 Data width override (DWO) - Set this bit to 1 to override the *dw* bit in the *Core control register* for the current command. If this bit is 0, then the *dw* bit in the *Core control register* decides whether to use an 8-bit or 16-bit data lane for the current command. This bit is only available if the *dw16* bit in the *Capability register* is 1. Reset value 0.

19 Reserved (R) - Always reads zero.

18 Command select (SEL) - This bit is used to select between commands that have the same opcode in the first command cycle. This applies to the CHANGE WRITE COLUMN and COPYBACK PROGRAM commands, which both have a first command byte with the value of 0x85. If a COPYBACK PROGRAM is to be executed, this bit should be set to 0. If a CHANGE WRITE COLUMM command is to be executed, this bit should be set to 1. If the *rev* field in the *Capability register* > 0 then this bit is also used to select between a PAGE PROGRAM and a SMALL DATA MOVE (with opcode 0x80). If the SMALL DATA MOVE should be executed then this bit should be set to 1, otherwise it should be set to 0. The core ignores this bit for all other commands. This field can only be written if the *bsy* bit in the *Buffer control / status register* is zero.

17 Skip second command phase (SC2) - If this bit is set and a program command (PAGE PROGRAM, COPYBACK PROGRAM, or CHANGE WRITE COLUMN) is being executed the core skips the second command phase for that command and jumps back to idle state once all data has been written. This is done in order to support the CHANGE WRITE COLUMN command, which needs to be executed in between the first and second phase of the program command. If a CHANGE WRITE COLUMN command is required during a PAGE PROGRAM, the PAGE PROGRAM command is issued with SC2 set to 1. After that when issuing a CHANGE WRITE COLUMN command if more than one CHANGE WRITE COLUMN commands needs to be issued all the ones apart from the last one is issued with SC" set to 0. The last CHANGE WRITE COLUMN command is issued with SC2 set to '1' this way the PAGE PROGRAM command is ended. See the ONFI 2.2 specification for details on the CHANGE WRITE COLUMN command. This bit is ignored by the core for all other commands. . This field can only be written if the *bsy* bit in the *Buffer control / status register* is zero.

16 Common data (CD) - Sometimes, for example for the SET FEATURES command, it is desirable to send the same data on all data lanes. If this is the case, software can write the data to send in the buffer corresponding to the first data lane and then set to this bit to 1. When the core executes the command it will then send the same data on all lanes without the need for software to fill all the corresponding buffers. Needs to be set to 0 if individual data should be send to the devices. This field can only be written if the *bsy* bit in the *Buffer control / status register* is zero.

15:8 Second command phase (CMD2) - If the command to execute is a two byte (two phase) command then software should write the second byte of the command to this field. The core ignores this field for commands that only have one command phase. This field can only be written if the *bsy* bit in the *Buffer control / status register* is zero.

7:0 First command phase (CMD1) - Software should write this field with the first byte of the command to execute. This field can only be written if the *bsy* bit in the *Buffer control / status register* is zero.

*Table 1551.*0x1C,0x2C - BCS - Buffer control / status register

31 27	26	25	24	23 16	15 8	7 4	3 2	1	0
R	INV	BSY	RUN	R	LANESEL	TARGSEL	R	IRQM	EXE
0	0	0	0	0	NR	NR	0	1	0
r	rw	wc	r	r	rw*	rw*	r	rw*	rw*

31:27 Reserved (R) - Always reads zero.

26 Invalid command (INV) - This bit is set to one if an invalid command is written to the *Buffer command register* when the *exe* bit is written. This bit is cleared automatically once a new command is started. Reset value: 0

25 Buffer busy (BSY) - Core sets this bit to 1 when a command is being executed. Once the command is done (*run* bit is cleared) software can clear this bit by writing 1 to it. While this bit is set it prevents software from writing to the buffer. This bit is write clear, but only when the *run* bit is zero. Reset value: 0

24 Command running (RUN) - Core sets this bit to 1 when a command is being executed, and clears it again automatically once the command is done. While this bit is set it prevents software from accessing the buffer. Reset value: 0

23:16 Reserved (R) - Always reads zero.

15:8 Data lane select (LANESEL) - The core uses this field to select which of the connected 8-bit/16-bit data lanes to send the command to (which write enable (WE) signals to assert). (A write enable signal can be connected to one or more flash memory devices but only one of the targets is selected at a time.) The least significant bit in this field corresponds to the first connected data lane (WE(0)) etc. The actual number of bits implemented equals the *nlanes* field in the *Capability register* plus one. This field can only be written if the *bsy* bit in the *Buffer control / status register* is zero.

7:4 Target select (TARGSEL) - The core uses this field to select which targets to send the command to (which chip enable (CE) signals to assert). The least significant bit in this field corresponds to the first target (CE(0)) etc. (A chip enable signal can be connected to one or more flash memory devices, all on different 8-bit/16-bit memory lanes. One or more chip enable signals can be connected to a flash memory device, depending on how many targets the device implements.) The actual number of bits implemented equals the *ntargs* field in the *Capability register* plus one. This field can only be written if the *bsy* bit in the *Buffer control / status register* is zero.

3:2 Reserved (R) - Always reads zero.

1 Interrupt mask (IRQM) - If this bit is set to 1 an interrupt will be generated when the command linked to the corresponding buffer has been executed. This field can only be written if the *bsy* bit in the *Buffer control / status register* is zero. Reset value: 1

0 Execute command (EXE) - When software writes this bit to 1 the core sends the command programmed into the corresponding *Buffer command register* to the lanes and targets selected by the *lanesel* and *targsel* field in this register. This field can only be written if the *bsy* bit in the *Buffer control / status register* is zero. Reset value: 0

*Table 1552.*0x30 - TIM0 - Programmable timing register 0

15 9	8 0
tCS	tCCS
*	*
rw*	rw*

31 30	29 24	23 16
R	tRP	tRHW
0	*	*
r	rw*	rw*

31:30 Reserved (R) - Always reads zero.

29:24 RE pulse width (tRP) - Length of tRP in clock cycles, minus one. See ONFI 2.2 specification for more information. Field only present if programmable timing is implemented. Indicated by *prgt* bit in *Capability* register. Reset value calculated from VHDL generic *sysfreq* to match value for timing mode 0.

23:16 RE high to WE low (tRHW) - Length of tRHW in clock cycles, minus one. See ONFI 2.2 specification for more information. Field only present if programmable timing is implemented. Indicated by *prgt* bit in *Capability* register. Reset value calculated from VHDL generic *sysfreq* to match value for timing mode 0.

*Table 1552.*0x30 - TIM0 - Programmable timing register 0

15:9 CE setup time (tCS) - Length of tCS in clock cycles, minus one. See ONFI 2.2 specification for more information. Field only present if programmable timing is implemented. Indicated by *prgt* bit in *Capability* register. Reset value calculated from VHDL generic *sysfreq* to match value for timing mode 0.

8:0 Change Column setup time (tCCS) - Length of tCCS in clock cycles, minus one. See ONFI 2.2 specification for more information. Reset value calculated from VHDL generic *sysfreq* to match value for timing mode 0.

Table 1553. 0x34 - TIM1 - Programmable timing register 1 (only present if programmable timing is implemented, which is indicated by *prgt* bit in *Capability* register)

15	14 8	7 5	4 0
R	tWHR	R	tWH
0	*	0	*
r	rw*	r	rw*

31 30 29 24	23 22	21 16
tWB	R	tWP
*	0	*
rw*	r	rw*

31:24 WE high to SR[6] low (tWB) - Length of tWB in clock cycles, minus one.ee ONFI 2.2 specification for more information. Reset value calculated from VHDL generic *sysfreq* to match value for timing mode 0.

23:22 Reserved (R) - Always reads zero.

21:16 WE pulse width (tWP) - Length of tWP in clock cycles, minus one. See ONFI 2.2 specification for more information. Reset value calculated from VHDL generic *sysfreq* to match value for timing mode 0.

15 Reserved (R) - Always reads zero.

14:8 WE high to RE low (tWHR) - Length of tWHR in clock cycles, minus one. See ONFI 2.2 specification for more information. Reset value calculated from VHDL generic *sysfreq* to match value for timing mode 0.

7:5 Reserved (R) - Always reads zero.

4:0 WE high hold time (tWH) - Length of tWH in clock cycles, minus one. See ONFI 2.2 specification for more information. Reset value calculated from VHDL generic *sysfreq* to match value for timing mode 0.

*Table 1554.*0 x38 - TIM2 - Programmable timing register 2 (only present if programmable timing is implemented, which is indicated by *prgt* bit in *Capability* register)

15	14 8	7 6	5 0
R	tWW	R	tRR
0	*	0	*
r	rw*	r	rw*

31 24	23 16
R	tADL
0	*
r	rw*

31:24 Reserved (R) - Always reads zero.

23:16 ALE to data loading time (tADL) - Length of tADL in clock cycles, minus one. See ONFI 2.2 specification for more information. Reset value calculated from VHDL generic *sysfreq* to match value for timing mode 0.

15 Reserved (R) - Always reads zero.

*Table 1554.*0 x38 - TIM2 - Programmable timing register 2 (only present if programmable timing is implemented, which is indicated by *prgt* bit in *Capability* register)

14:8	WP transition to WE low (tWW) - Length of tWW in clock cycles, minus one. See ONFI 2.2 specification for more information. Reset value calculated from VHDL generic *sysfreq* to match value for timing mode 0.
7:6	Reserved (R) - Always reads zero.
5:0	Ready to RE low (tRR) - Length of tRR in clock cycles, minus one. See ONFI 2.2 specification for more information. Reset value calculated from VHDL generic *sysfreq* to match value for timing mode 0.

Table 1555. 0x3C - TIM3 - Programmable timing register 3 (only present if programmable timing is implemented and core revision is bigger or equal to 2, which is indicated by *prgt* bit and *REV* bits in *Capability* register)

31 6	5 0
R	tREH
0	*
r	rw*

31:6	Reserved (R) - Always reads zero.
5:0	RE high hold time (tREH) - Length of tREH in clock cycles, minus one. For backward compatibility purposes the value of tREH is set to the value of tRP when TIM0 register is updated. As a result if the required tREH value is different than tRP, then the TIM3 has to be updated after TIM0 is updated. It should be noted that if tREH value is set something different than tRP, the tRC (tRP+tREH) timing should be met. See ONFI 2.2 specification for more information. Reset value calculated from VHDL generic *sysfreq* to match value for timing mode 0.

Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x059. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

88.5 Timing Modes

It is highly recommended to use programmable timing to be able to customize timing, which is needed when additional timing delays are needed to be accounted like I/O delays. In addition it gives the flexibility to correct timing errors by software. See ONFI specification 2.2 for more details about timing.

88.5.1 Timing Register Values when Programmable Timing is Disabled

This section shows how the timing counter values are calculated when programmable timing is disabled. It should be noted that this values are calculated without taking additional delays into account, for example the delay from the NANDFCTRL core outputs to NANDFLASH DEVICE or vice versa. Hence it is highly recommended to use programmable timing, to mitigate additional delays and manage custom timing.

The values are floored if there is a remainder after the division. The following calculations show which values are used instead of the values that are defined in the timing registers when programmable timing is not enabled.

CLOCK_PERIOD = `1000000/sysfreq (sysfreq is a generic)`

tWW = 100/CLK_PERIOD (TM0,TM1,TM2,TM3,TM4,TM5)

tCCS = 500/CLK_PERIOD (TM0,TM1,TM2,TM3,TM4,TM5)

tADL = 200/CLK_PERIOD (TM0); 100/CLK_PERIOD (TM1); 100/CLK_PERIOD (TM2); 100/CLK_PERIOD (TM3); 70/CLK_PERIOD (TM4); 70/CLK_PERIOD (TM5);

tCS = 70/CLK_PERIOD (TM0); 35/CLK_PERIOD (TM1); 25/CLK_PERIOD (TM2); 25/CLK_PERIOD (TM3); 20/CLK_PERIOD (TM4); 15/CLK_PERIOD (TM5);

tRHW = 200/CLK_PERIOD (TM0); 100/CLK_PERIOD (TM1); 100/CLK_PERIOD (TM2); 100/CLK_PERIOD (TM3); 100/CLK_PERIOD (TM4); 100/CLK_PERIOD (TM5);

tRP = 50/CLK_PERIOD (TM0); 30/CLK_PERIOD (TM1); 25/CLK_PERIOD (TM2); 20/CLK_PERIOD (TM3); 20/CLK_PERIOD (TM4); 16/CLK_PERIOD (TM5);

tREH = 50/CLK_PERIOD (TM0); 20/CLK_PERIOD (TM1); 15/CLK_PERIOD (TM2); 10/CLK_PERIOD (TM3); 10/CLK_PERIOD (TM4); 7/CLK_PERIOD (TM5);

tWH = 30/CLK_PERIOD (TM0); 15/CLK_PERIOD (TM1); 15/CLK_PERIOD (TM2); 10/CLK_PERIOD (TM3); 10/CLK_PERIOD (TM4); 7/CLK_PERIOD (TM5);

tWHR = 120/CLK_PERIOD (TM0); 80/CLK_PERIOD (TM1); 80/CLK_PERIOD (TM2); 60/CLK_PERIOD (TM3); 60/CLK_PERIOD (TM4); 60/CLK_PERIOD (TM5);

tWP = 50/CLK_PERIOD (TM0); 25/CLK_PERIOD (TM1); 17/CLK_PERIOD (TM2); 15/CLK_PERIOD (TM3); 12/CLK_PERIOD (TM4); 10/CLK_PERIOD (TM5);

tWB = 200/CLK_PERIOD (TM0); 100/CLK_PERIOD (TM1); 100/CLK_PERIOD (TM2); 100/CLK_PERIOD (TM3); 100/CLK_PERIOD (TM4); 100/CLK_PERIOD (TM5);

tRR = 40/CLK_PERIOD (TM0); 20/CLK_PERIOD (TM1); 20/CLK_PERIOD (TM2); 20/CLK_PERIOD (TM3); 20/CLK_PERIOD (TM4); 20/CLK_PERIOD (TM5);

If TM5 mode is intended to be used when programmable timing is disabled, the user has to calculate if the *tRC* period is going to be less than 30 ns. If it less than 30 ns the tm5_edoen generic shall be set to 1 according to ONFI 2.2 specification. In other cases tm5_edoen should be set to 0.

88.5.2 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers. The Flash interface signals have asynchronous reset.

88.5.3 Core instantiation

The core maps all usage of RAM on the *syncram* (or *syncramft* if *ft* generic is not set to 0) component from the technology mapping library (TECHMAP). The size of the instantiated RAM is determined by the *pbufsize*, *sbufsize*, *nlanes*, and *sepbufs* generics. Fault tolerance - byte parity DMR or TMR - can be added to the RAM by setting the *ft* generic to 1 or 2.

Note that both the *ft* and *edac* generics need to be set to 0 unless the core is used together with the fault tolerant GRLIB.

The core implements one interrupt, mapped by means of the *pirq* VHDL generic.

88.5.4 Scan test support

The VHDL generic *scantest* enables scan test support. If the core has been implemented with scan test support and the *testen* input signal is high, the core will:

- disable the internal RAM blocks when the *scanen* signal is asserted.
- use the *testoen* signal as output enable signal.
- use the *testrst* signal as the reset signal for those registers that are asynchronously reseted.

The *testen*, *scanen*, *testrst*, and *testoen* signals are routed via the AHB slave interface.

88.6 Configuration options

Table 1556 shows the configuration options of the core (VHDL generics).

*Table 1556.*Configuration options

Generic name	Function	Allowed range	Default
hsindex	AHB slave index	0 - NAHBSLV-1	0
haddr0	AHB slave address for BAR 0. See section 88.2.2 for explanation of address scheme.	0 - 16#FFF#	16#000#
haddr1	AHB slave address for BAR 1. See section 88.2.2 for explanation of address scheme.	0 - 16#FFF#	16#001#
hmask0	AHB slave address mask for BAR 0. If set to zero, BAR 0 is disabled. See section 88.2.2 for explanation of address scheme.	0 - 16#FFF#	16#FFF#
hmask1	AHB slave address mask for BAR 1. If set to zero, BAR 1 is disabled. See section 88.2.2 for explanation of address scheme.	0 - 16#FFF#	16#FFF#
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	ADDR field of the APB BAR.	0 - 16#FFF#	0
pmask	MASK field of the APB BAR.	0 - 16#FFF#	16#FFF#
pirq	APB irq number.	0 - NAHBIRQ-1	0
memtech	Memory technology used for the buffers.	0 - NTECH	inferred
sysfreq	System clock frequency in kHz.	1 - 1 000 000	50000
ntargets	Number of targets = Number of chip select signals connected to the core. A flash memory device can have one or more targets.	1 - 4	2
nlanes	Number of 8-bit/16-bit data lanes = Number of write enable signals. A write enable signal can be connected to one or more targets (i.e. one or more flash memory devices).	1 - 8	8
dwidth16	0 = Core implements 8-bit data lanes. 1 = Core implements 16-bit data lanes.	0 - 1	0
pbufsize	Size of each page buffer (in bytes). One or two page buffers are implemented for each connected flash memory device (depends on value of generic *buf1en*.). Generic needs to be set to a value equal to or greater than the flash memory device's page area. Value also needs to be a power of two.	8, 16, 32 ... 32768	4096
sbufsize	Size of each spare area buffer (in bytes). One or two spare buffers are implemented for each connected flash memory device (depends on value of generic *buf1en*.). Generic needs to be set to a value equal to or greater than the flash memory device's page spare area. Value also needs to be a power of two.	8, 16, 32 ... 32768	256
tm1	Enable support for timing mode 1 in the case with fixed data interface timing (*progtime* generic set to 0). This generic has no effect if the *progtime* generic is set to 1.	0 - 1	0
tm2	Enable support for timing mode 2 in the case with fixed data interface timing (*progtime* generic set to 0). This generic has no effect if the *progtime* generic is set to 1.	0 - 1	0

*Table 1556.*Configuration options

Generic name	Function	Allowed range	Default
tm3	Enable support for timing mode 3 in the case with fixed data interface timing (*progtime* generic set to 0). This generic has no effect if the *progtime* generic is set to 1.	0 - 1	0
tm4	Enable support for timing mode 4 in the case with fixed data interface timing (*progtime* generic set to 0). This generic has no effect if the *progtime* generic is set to 1.	0 - 1	0
tm5	Enable support for timing mode 5 in the case with fixed data interface timing (*progtime* generic set to 0). This generic has no effect if the *progtime* generic is set to 1.	0 - 1	0
tm5_edoen	Enable EDO data output cycles when timing mode 5 is used in the case fixed data interface timing (progtime generic set to 0). This generic has no effect if the *progtime* generic is set to 1. This generic is only available if the core revision is bigger or equal to 2.	0 - 1	0
nsync	Number of synchronization registers on R/B input. (Data input is always synchronized through one set of registers.)	0 - 3	2
ft	This generic determines if fault tolerance should be added to the buffers. 0 = no fault tolerance, 1 = Byte parity DMR, 2 = TMR. 3 = Byte parity, no DMR. Note that this generic needs to be set to 0 if the core is used together with the GPL version of GRLIB, since that version does not include any fault tolerance.	0 - 2	0
oepol	Polarity of pad output enable signal.	0 - 1	0
scantest	Enable scan test support.	0 - 1	0
edac	Enable EDAC support. See section 88.3.1 for EDAC information. Note that this generic needs to be set to 0 if the core is used together with the GPL version of GRLIB, since that version does not include any fault tolerance.	0 - 1	0
cmdorder	Sets the default way the ONFI command bytes are mapped to the core's data lane(s). When set to 0 the commands are mapped as follows: Cmd bit 0 -> Data lane bit 7, Cmd bit 1 -> Data lane bit 6., and so on. When this bit is set to 1 the commands are mapped as follows: Cmd bit 0 -> Data lane bit 0, Cmd bit 1 -> Data lane bit 1, and so on.	0 - 1	1
sepbufs	When set to 0 all data lanes share the same internal memory buffers. When set to 1 all data lanes have their own internal memory buffers. When set to 0 a command with a data in phase should only be issued to one target and lane at the time. A command with a data out phase can still be issued to several lanes and targets but with the limitation that the same data will be sent on all lanes. When set to 1 several lanes can be read at the same time, and lanes can be written with individual data simultaneously.	0 - 1	1
progtime	When set to 0 the data interface timing for the different timing modes are set at implementation time from the *sysfreq* generic. When set to 1 the data interface timing is programmable through APB registers (reset values are set at implementation time from the *sysfreq* generic). Maximum system frequency when this generic is set to 1 is 1 GHz.	0 - 1	0

*Table 1556.*Configuration options

Generic name	Function	Allowed range	Default
buf1en	When this generic is set to 1 then both buffer 0 and buffer 1 are implemented. If set to 0, only buffer 0 is implemented. See section 88.2.2 for more information about the buffer structure.	0 - 1	1

88.7 Signal descriptions

Table 1557 shows the interface signals of the core (VHDL ports).

*Table 1557.*Signal descriptions

Signal name	Field	Type	Function	Active
rst	N/A	Input	Reset	Logical 0
clk	N/A	Input	Clock	-
apbi	*	Input	APB slave input signals	-
apbo	*	Output	APB slave output signals	-
ahbsi	*	Input	AHB slave input signals	-
ahbso	*	Output	AHB slave output signals	-
nandfi	rb	Input	Ready/Busy signal	-
	di(63:0) [2]	Input	Data input (used both for 8-bit and 16-bit lanes)	-
	dih(63:0) [2]	Input	Data input (upper byte for 16-bit lanes)	-
nandfo	ce(3:0) [3]	Output	Chip enable	Logical 0
	we(7:0) [4]	Output	Write enable	Logical 0
	do(63:0) [2]	Output	Data output (used both for 8-bit and 16-bit lanes)	-
	doh(63:0)[2]	Output	Data output (upper byte for 16-bit memories)	-
	cle	Output	Command latch enable	Logical 1
	ale	Output	Address latch enable	Logical 1
	re	Output	Read enable	Logical 0
	wp	Output	Write protect	Logical 0
	err	Output	EDAC / Buffer error on AHB access	Logical 1
	oe	Output	Output enable	5

* see GRLIB IP Library User's Manual

[2] The actual number of data input/output signals used depends on core configuration. Eight bits are used for each lane.

[3] The core drives one chip select signal for each target, i.e. on or more attached flash memory devices.

[4] The core drives one write enable signal for each 8-bit/16-bit data lane, i.e. one or more attached flash memory devices.

[5] The polarity of the output enable signal is implementation dependent.

88.8 Signal definitions and reset values

The signals and their reset values are described in table 1558.

*Table 1558.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
rb	Input	Ready/Busy signal	-	-
d(63:0) [1]	Input/Output	Data (used both for 8-bit and 16-bit lanes)	-	-
dh(63:0) [1]	Input/Output	Data (upper byte for 16-bit lanes)	-	-
ce(3:0) [2]	Output	Chip enable	Logical 0	Logical 1
we(7:0) [3]	Output	Write enable	Logical 0	Logical 1
cle	Output	Command latch enable	Logical 1	Logical 0
ale	Output	Address latch enable	Logical 1	Logical 0
re	Output	Read enable	Logical 0	Logical 1
wp	Output	Write protect	Logical 0	Logical 1
err	Output	EDAC / Buffer error on AHB access	Logical 1	Logical 0
oe	Output	Output enable	[4]	[4]

[1] The actual number of data input/output signals used depends on core configuration. Eight bits are used for each attached flash memory device.

[2] The core drives one chip select signal for each target, i.e. on or more attached flash memory devices.

[3] The core drives one write enable signal for each 8-bit data lane, i.e. on or more attached flash memory devices.

[4] The polarity of the output enable signal is implementation dependent.

88.9 Library dependencies

Table 1559 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1559.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	MEMCTRL	Signals, component	Component declaration

88.10 Timing

The timing waveforms and timing parameters are shown in figure 252 and are defined in table 1560.

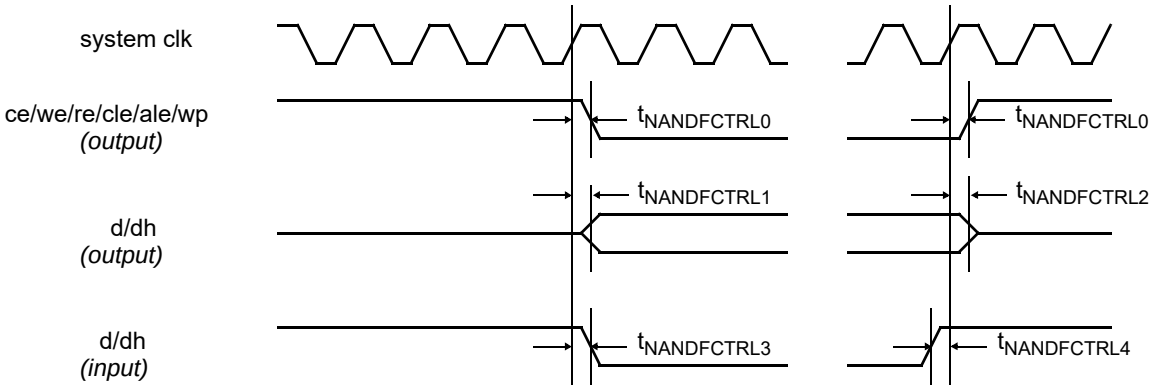


Figure 252. Timing waveforms

*Table 1560.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{NANDFCTRL0}$	clock to output delay	rising *clk* edge	TBD	TBD	ns
$t_{NANDFCTRL1}$	clock to non-tri-state delay	rising *clk* edge	TBD	TBD	ns
$t_{NANDFCTRL2}$	clock to tri-state delay	rising *clk* edge	TBD	TBD	ns
$t_{NANDFCTRL3}$	input to clock hold	rising *clk* edge	TBD	-	ns
$t_{NANDFCTRL4}$	input to clock setup	rising *clk* edge	TBD	-	ns

Note: The *rb* input is re-synchronized internally. The signal does not have to meet any setup or hold requirements.

88.11 Instantiation

This example shows how the core can be instantiated. The instantiated core has all its generics, except *hsindex*, *pindex*, *paddr*, and *pirq* at their default values. The impact of the generics can be seen in table 1556.

```
library ieee, grlib, gaisler;
use ieee.std_logic_1164.all;
use grlib.amba.all;
use gaisler.nandpkg.all;

entity nandfctrl_ex is
  port (
    clk : in std_ulogic;
    rstn : in std_ulogic;
    nandf_d : inout std_logic_vector(63 downto 0);
    nandf_dh : inout std_logic_vector(63 downto 0);
    nandf_rb : in std_ulogic;
    nandf_ce : out std_logic_vector(1 downto 0);
    nandf_we : out std_logic_vector(7 downto 0);
    nandf_re : out std_ulogic;
    nandf_cle : out std_ulogic;
    nandf_ale : out std_ulogic;
    nandf_wp : out std_ulogic;
    nandf_err : out std_ulogic
    );
end;

architecture rtl of nandfctrl_ex is
```

```
  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbsi : ahb_slv_in_type;
  signal ahbso : ahb_slv_out_vector := (others => ahbs_none);


  -- NANDFCTRL signals
  signal nandfo : nandfctrl_out_type;
  signal nandfi : nandfctrl_in_type;

begin

  -- AMBA Components are instantiated here
  ...

  -- NANDFCTRL core
  nand0 : nandfctrl
    generic map (hsindex => 1, pindex => 10, paddr => 10, pirq => 10)
    port map (rstn, clk, apbi, apbo(10), ahbsi, ahbso(1), nandfi, nandfo);

  -- Pads for NANDFCTRL core
  nandf_d : iopadv generic map (tech => padtech, width => 64)
                   port map (nandf_d, nandfo.do, nandfo.oe, nandfi.di);
  nandf_dh : iopadv generic map (tech => padtech, width => 64)
                   port map (nandf_dh, nandfo.doh, nandfo.oe, nandfi.dih);
  nandf_rb : inpad generic map (tech => padtech)
                   port map (nandf_rb, nandfi.rb);
  nandf_ce : outpadv generic map (tech => padtech, width => 2)
                   port map (nandf_ce, nandfo.ce);
  nandf_we : outpadv generic map (tech => padtech, width => 8)
                   port map (nandf_we, nandfo.we);
  nandf_re : outpad generic map (tech => padtech)
                   port map (nandf_re, nandfo.re);
  nandf_cle : outpad generic map (tech => padtech)
                   port map (nandf_cle, nandfo.cle);
  nandf_ale : outpad generic map (tech => padtech)
                   port map (nandf_ale, nandfo.ale);
  nandf_wp : outpad generic map (tech => padtech)
                   port map (nandf_wp, nandfo.wp);
  nandf_err : outpad generic map (tech => padtech)
                   port map (nandf_err, nandfo.err);

end;
```

89 PHY - Ethernet PHY simulation model

89.1 Overview

The PHY is a simulation model of an IEEE 802.3 compliant Ethernet PHY. It provides a complete MII and GMII interface with the basic, extended status and extended capability registers accessible through the management interface (MDIO). Not all of the functionality is implemented and many of the register bits are therefore only writable and readable but do not have any effect. Currently only the loopback is supported.

89.2 Operation

The PHY simulation model was designed to make it possible to perform simple simulations on the GRETH and GRETH_GBIT cores in GRLIB. It provides the complete set of basic, extended capability and extended status registers through the MII management interface (MDIO) and a loopback mode for data transfers. Figure 1 shows a block diagram of a typical connection.

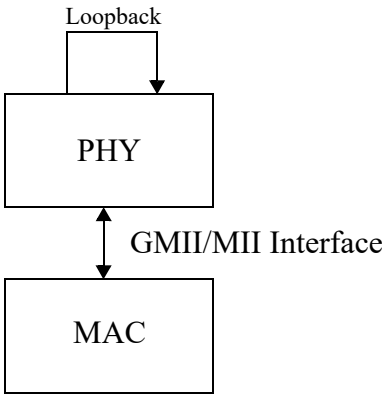


Figure 253. Block diagram of the PHY simulation model connected to a MAC.

The PHY model provides the complete GMII and MII interface as defined by the IEEE 802.3 standard. The model can be used in any of the following modes: 10 Mbit half- or full duplex, 100 Mbit half- or full-duplex and 1000 Mbit half- or full-duplex. This support refers only to the configuration settings available through the MDIO registers. Since the datapath implementation is loopback no collisions will ever be seen on the network and operation will essentially be full-duplex all the time. In loopback mode, rx_clk and tx_clk are identical in both frequency and phase and are driven by the PHY when not in gigabit mode. In gigabit mode the gtx_clk input is used as the transmitter clock and it also drives rx_clk.

When not configured to loopback mode the PHY just sits idle and ignores transmitted packet and does not insert any activity on the receive interface. Clocks are still generated but in this case rx_clk and tx_clk does have the same frequency but not the same phase when not in gigabit mode.

A simple auto-negotiation function is provided and the supported and advertised modes are set through vhdl generics. The generic values will be directly reflected in the reset values and read-only values of all corresponding MII management registers.

89.3 Configuration options

Table 1561 shows the configuration options of the model (VHDL generics).

*Table 1561.*Configuration options

Generic	Function	Allowed range	Default
address	Address of the PHY on the MII management interface	0 - 31	0
extended_regs	Include extended register capability	0 - 1	1
aneg	Enable auto-negotiation functionality	0 - 1	1
base100_t4	Enable support for 100Base-T4	0 - 1	0
base100_x_fd	Enable support for 100Base-X full-duplex	0 - 1	1
base100_x_hd	Enable support for 100Base-X half-duplex	0 - 1	1
fd_10	Enable support for 10Base-T full-duplex	0 - 1	1
hd_10	Enable support for 10Base-T half-duplex	0 - 1	1
base100_t2_fd	Enable support for 100Base-T2 full-duplex	0 - 1	1
base100_t2_hd	Enable support for 100Base-T2 half-duplex	0 - 1	1
base1000_x_fd	Enable support for 1000Base-X full-duplex	0 - 1	0
base1000_x_hd	Enable support for 1000Base-X half-duplex	0 - 1	0
base1000_t_fd	Enable support for 1000Base-T full-duplex	0 - 1	1
base1000_t_hd	Enable support for 1000Base-T half-duplex	0 - 1	1
rmii	Set PHY in RMII mode	0 - 1	0

89.4 Signal descriptions

Table 1562 shows the interface signals of the model (VHDL ports).

*Table 1562.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	-	Input	Reset	Low
MDIO	-	Input/ Output	Data signal for the management interface (Currently not used)	-
TX_CLK	-	Output	Transmitter clock	-
RX_CLK	-	Output	Receiver clock	-
RXD	-	Output	Receiver data	-
RX_DV	-	Output	Receiver data valid	High
RX_ER	-	Output	Receiver error	High
RX_COL	-	Output	Collision	High
RX_CRS	-	Output	Carrier sense	High
TXD	-	Input	Transmitter data	-
TX_EN	-	Input	Transmitter enable	High
TX_ER	-	Input	Transmitter error	High
MDC	-	Input	Management interface clock (Currently not used)	-
GTX_CLK	-	Input	Gigabit transmitter clock	-

see the IEEE 802.3 standard for a description of how the signals are used.

89.5 Library dependencies

Table 1563 shows the libraries used when instantiating the model (VHDL libraries).

*Table 1563.*Library dependencies

Library	Package	Imported unit(s)	Description
GAISLER	SIM	Component	Component declaration

89.6 Instantiation

This example shows how the model can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library gaisler;
use gaisler.sim.all;

entity phy_ex is
  port (
rst : std_ulogic;
clk : std_ulogic;
    );
end;

architecture rtl of phy_ex is

  -- Signals

 signal etx_clk   : std_logic;
 signal gtx_clk   : std_logic;
 signal erx_clk   : std_logic;
 signal erxd      : std_logic_vector(7 downto 0);
 signal erx_dv    : std_logic;
 signal erx_er    : std_logic;
 signal erx_col   : std_logic;
 signal erx_crs   : std_logic;
 signal etxd      : std_logic_vector(7 downto 0);
 signal etx_en    : std_logic;
 signal etx_er    : std_logic;
 signal emdc      : std_logic;

begin

  -- Other components are instantiated here
  ...


  -- PHY model
  phy0 : phy
  generic map (address => 1)
  port map(resetn => rst, mdio => open, tx_clk => etx_clk, rx_clk => erx_clk, rxd => erxd,
  rx_dv => erx_dv, rx_er => erx_er,
  rx_col => erx_col, rx_crs => erx_crs, txd => etxd, tx_en => etx_en,
  tx_er => etx_er, mdc => emdc, gtx_clk => gtx_clk);
end;
```

90 RGMII - Reduced Ethernet Media Access Controller

90.1 Overview

Cobham Gaisler's RGMII IP provides the RGMII adaptation layer between the Ethernet physical media device and the GRETH or GRETH_GBIT IP core.

The RGMII adaptation layer supports version 2.0 of the Reduced Gigabit Media Independent interface and can dynamically switch between diffrent speed modes of operation.

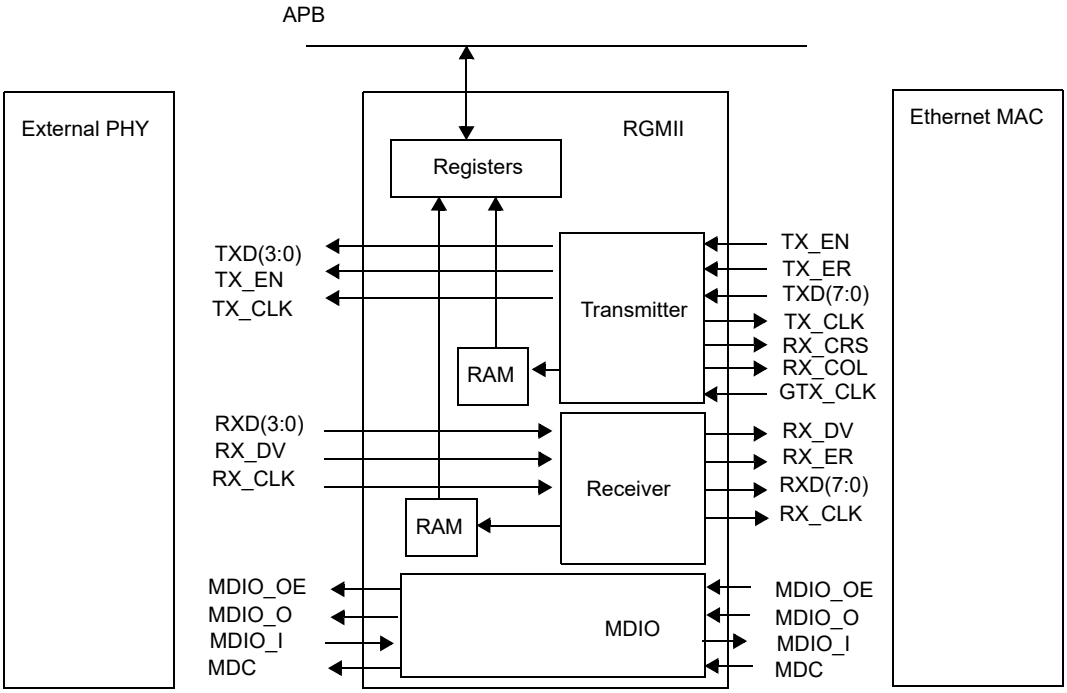


Figure 254. Block diagram of the internal structure of the RGMII.

90.2 Operation

90.2.1 Protocol support

The RGMII adaptation layer supports version 2.0 of the Reduced Gigabit Media Independent interface and IEEE standard 802.3-2002 for GMII.

90.2.2 Transmit clock

The trasnsmitter clock is used by the transmit logic of the core. The transmit clock is also an output from the RGMII IP and will be used as the TX clock in the Ethernet MAC. There are three options of generating and using the transmit clock inside the IP. The VHDL generics ‘no_clock_mux’ and ‘use90degtxclk’ determines the clock mode used by the RGMII IP.

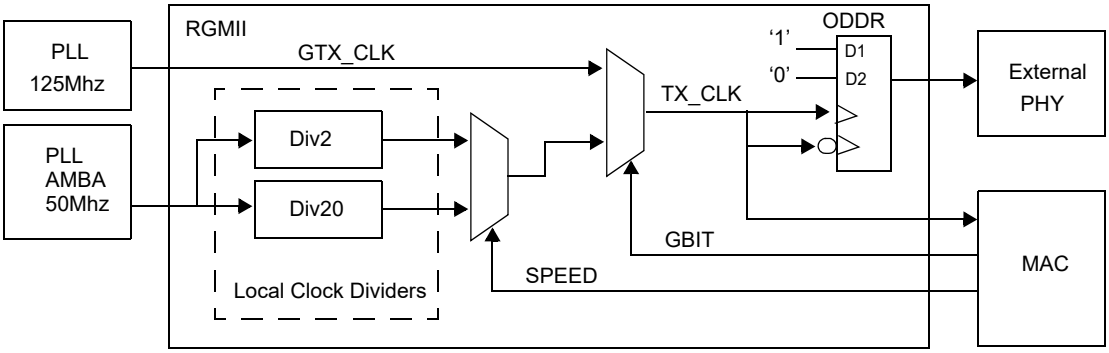


Figure 255. 10/100 Mb/s transmiter clocks generated by internal logic

Figure 255 shows the clocking scheme when the transmit clock for 10Mb/s and 100Mb/s mode is generated internally. This clock mode is used when the VHDL generic 'no_clock_mux' is set to '0'. In this case user must ensure that the GMII clock frequency and AMBA clock frequency is appropriate for the line speed. That is, 50Mhz AMBA clock for 10/100 Mb/s and 125Mhz for 1000Mb/s.

Local clock resources will provide 2.5MHz and 25MHz frequency clocks for 10 Mb/s and 100 Mb/s speeds of operation, respectively. The local clock logic generates the 2.5MHz and 25MHz TX_CLK clock from the 50MHz AHB_CLK.

The SPEED and GBIT signals from the Ethernet MAC are used as selection pins of the local clock muxes.

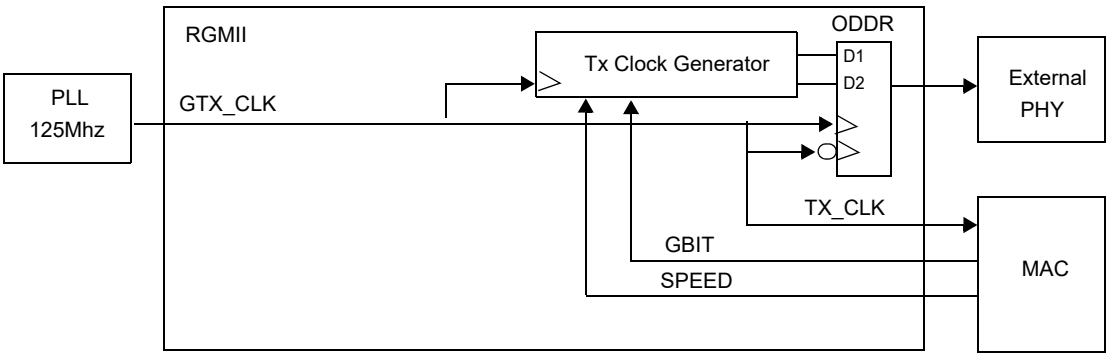


Figure 256. All transmit clocks generated by internal logic

Figure 256 show an alternative clock scheme using only one clock domain for the transmitter. This clock mode is used when setting the VHDL generic 'no_clock_mux' to 1. The local clock divider is replaced by a counter in the GTX_CLK clock domain to generate bit pattern for clock generation in 10 Mb/s, 100 Mb/s, and 1 Gb/s speeds of operation.

The bit pattern is connected to the DDR output buffers data inputs and 125MHz GTX_CLK clock is connected to the DDR output buffer clock in order to generate the transmit clock to the external PHY.

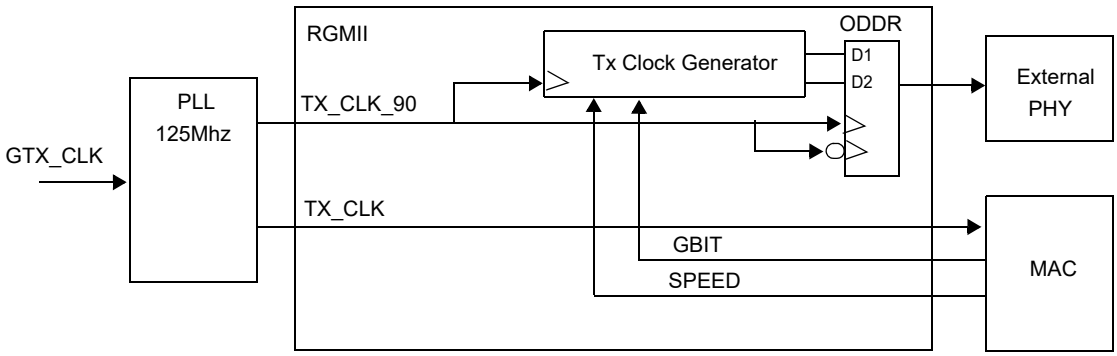


Figure 257. External PHY transmit clock 90deg phase shift

The RGMII v2.0 standard specifies that the external PHY TX clock to have a setup of 2 ns with respect to the TX data. The 2ns setup can be achieved by phase shifting the external transmit clock to the external PHY by 90 degrees relative the internal MAC transmit clock. This mode is shown in figure 257 and is used when setting the VHDL generic 'no_clock_mux' to 1 and 'use90degtxclk' to 1.

90.2.3 Transmitter Operation

The transmitter is enabled when the GMII transmitter enable is high. Data is transferred from the GMII to RGMII as long as the GMII transmitter enable signal is high.

The transmitter enable signal is expected to be high during the complete transmission of the Ethernet MAC frame.

90.2.4 Side-band information

The RGMII receiver samples input data at all time. Side-band information is stored in the RGMII status register accessible via the APB interface. The status register has an address offset of 0x0.

90.2.5 MDIO Management

The RGMII IP only forwards the MDIO signals from the MDIO bus master (GRTEH/GRETH_GBIT) to the external PHY. The RGMII does not affect any MDIO transactions.

90.2.6 RAM debug support

The IP RGMII can optionally be build to include debug memories. The debug memories will record and store the last received and transmitted MAC frame. The RAM debug support is used when the VHDL generic ’debugmem’ to 1.

The transmit frame buffer is accessed starting from the APB address offset 0x400 and the receive frame buffer is located at APB address offset 0x800.

90.3 Media Independent Interfaces

There are several interfaces defined between the MAC sublayer and the Physical layer. The GRETH_GBIT supports the Media Independent Interface (MII) and the Gigabit Media Independent Interface (GMII).

The GMII is used in 1000 Mbit mode and the MII in 10 and 100 Mbit. These interfaces are defined separately in the 802.3-2002 standard but in practice they share most of the signals. The GMII has 9

additional signals compared to the MII. Four data signals are added to the receiver and transmitter data interfaces respectively and a new transmit clock for the gigabit mode is also introduced.

The RGMII interface uses the same signal with the additional signal tx_clk_90.

*Table 1564.*Signals in RGMII, GMII and MII.

MII and GMII	GMII Only	RGMII Only
txd[3:0]	txd[7:4]	tx_clk_90
tx_en	rxd[7:4]	
tx_er	gtx_clk	
rx_col		
rx_crs		
rxd[3:0]		
rx_clk		
rx_er		
rx_dv		
rx_en		
tx_dv		

90.4 Registers

The core is programmed through registers mapped into APB address space.

*Table 1565.*RGMII registers

APB address offset	Register
0x0	Status register
0x4	Interrupt-source register
0x8	Interrupt mask register
0xC	25Mhz bit pattern wrap register
0x10	25Mhz bit pattern first edge register
0x14	25Mhz bit pattern second edge register
0x18	2.5Mhz bit pattern wrap register
0x1C	2.5Mhz bit pattern first edge register
0x20	2.5Mhz bit pattern second edge register
0x24	Bit pattern register
0x28	Data bit 4 to 7 (negative clocked) delay register
0x2C	Data bit 0 to 3 (positive clocked) delay register
0x30	Data bit swap register
0x400 - 0x7FC	Transmit RAM buffer debug access
0x800 - 0xBFC	Receiver RAM buffer debug access

90.4.1 Status / Interrupt / Mask Register

*Table 1566.*RGMII status/interrupt/mask register

31 16	15	14	13	12 10	9	8	7	6	5	4	3	2 1	0
RESERVED	NM	RD	GA	RESERVED	GB	SP	CS	CE	CX	FC	DS	CS	LS

15 No Clock Mux Mode (NM) - If this bit always reads as a 1 no internal clock logic has been used

14 RAM debug enable (RD) - If this bit always reads as a 1 the debug ram is available.

13 Gigabit MAC available (GA) - If this bit always reads as a 1 the MAC has 1000 Mbit capability.

9 Gigabit (GB) - 1 shows the current speed mode is1000 Mbit in the MAC and when set to 0, the speed mode is selected with bit 7 (SP). Reset value: ‘0’.

8 Speed (SP) - Shows the current speed mode of the MAC. 0 = 10 Mbit, 1 = 100 Mbit. Must not be set to 1 at the same time as bit 8 (GB). Reset valuie: ‘0’.

7 Carrier Sense (CS) - Carrier detected

6 Carrier Extend Error (CE) - Carrier Extend frames Error

5 Carrier Extend (CX) - Carrier Extend frames

4 False Carrier (FC) - False Carrier is detected

3 Duplex Status (DS) - Indicates duplex status 0=half-duplex, 1=full duplex

2: 1 Link Clock Speed (CS) - Indicates RXC clock speed 00=2.5Mhz, 01=25Mhz, and 10=125Mhz, 11=reserved

0 Links status (LS) - Indicates link status 0=down, 1=up

90.4.2 25 MHz Clock Warp Register

*Table 1567.*RGMII 25MHz clock warp register

31 16	15 6	5 0
RESERVED		WRAP

31: 6 RESERVED

5: 0 25Mhz warp register (WARP) - Number of GTX_CLK cycles to generate 25Mhz clock pattern

90.4.3 25 MHz First Edge Register

*Table 1568.*RGMII 25MHz first edge register.

31 16	15 6	5 0
RESERVED		EDGE1

31: 6 RESERVED

5: 0 25Mhz first edge (EDGE1) - Number of GTX_CLK cycles to before clock change state

90.4.4 25 MHz Second Edge Register

*Table 1569.*RGMII 25MHz Second edge register.

31 16	15 6	5 0
RESERVED		EDGE2

31: 6 RESERVED

5: 0 25Mhz Second edge (EDGE2) - Number of GTX_CLK cycles after the first edge the clock change state

90.4.5 Bit Pattern Register

*Table 1570.*RGMII bit pattern register.

31 18	17 16	15 14	13 8	7 6	5 0
Not Used	P125M	Not Used	P25M	Not Used	P2M5

17: 16 125Mhz clock pattern (P125M) - Pattern for generating 125Mhz clock

9: 3 25Mhz clock pattern (P25M) - Pattern for generating 25Mhz clock

5: 0 2.5Mhz clock pattern (P2M5) - Pattern for generating 2.5Mhz clock

90.4.6 Positive / Negative Clocked Data Receiver Delay Register

*Table 1571.*RGMII positive / negative clocked data receiver delay register.

31 2	1 0
Not Used	DEL

2: 0 Delay input (DEL) - Number of RX clock cycles to delay input data

90.4.7 Receiver Data Swap Register

*Table 1572.*RGMII receiver data swap register

31 1	0
Not Used	SW

0 Swap receiver input clock edge (SW) - Swaps data between negative and positive clocked data input

90.5 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x093. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

90.6 Implementation

90.6.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support *grlib_async_reset_enable*. All registers that react on the reset signal will have a synchronous reset.

90.7 Configuration options

Table 1573 shows the configuration options of the core (VHDL generics).

*Table 1573.*Configuration options

Generic	Function	Allowed range	Default
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	Addr field of the APB bar.	0 - 16#FFF#	0
pmask	Mask field of the APB bar.	0 - 16#FFF#	16#FFF#
pirq	Interrupt line used by the RGMII.	0 - NAHBIRQ-1	0
tech	Technology used for the DDR buffers.	0 - NTECH	inferred
debugmem	Enables debug access to the core's RAM blocks through the APB interface.	0 - 1	0
abits	Selects the number of APB address bits used to decode the register addresses	3 - 8	8
no_clk_mux	Dont't generate 10Mb and 100Mb mode clock in RGMII logic	0 - 1	0
use90degtxclk	Use external generated trasnmit clock to to have a setup of 2 ns with respect to the TX data. VHDL generic 'no_clk_mux' must be set to '1' to use this option.	0 - 1	0

90.8 Signal descriptions

Table 1574 shows the interface signals of the core (VHDL ports).

*Table 1574.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	System reset	Low
APB_RSTN	N/A	Input	AMBA Reset	Low
APB_CLK	N/A	Input	AMBA Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-

*Table 1574.*Signal descriptions

Signal name	Field	Type	Function	Active
GMIII	gtx_clk	Output	Ethernet gigabit transmit clock.	-
	rmii_clk	Output	Ethernet RMII clock.	-
	tx_clk	Output	Ethernet transmit clock.	-
	tx_dv	Output	Ethernet transmitter enable	-
	rx_clk	Output	Ethernet receive clock.	-
	rxd	Output	Ethernet receive data.	-
	rx_dv	Output	Ethernet receive data valid.	High
	rx_er	Output	Ethernet receive error.	High
	rx_col	Output	Ethernet collision detected. (Asynchronous, sampled with tx_clk)	High
	rx_crs	Output	Ethernet carrier sense. (Asynchronous, sampled with tx_clk)	High
	rx_en	Output	Ethernet receiver enable.	-
	mdio_i	Output	Ethernet management data input	-
	mdint	Output	Ethernet management interrupt	-
GMIIO	reset	Input	Ethernet reset (asserted when the MAC is reset).	Low
	txd	Input	Ethernet transmit data.	-
	tx_en	Input	Ethernet transmit enable.	High
	tx_er	Input	Ethernet transmit error.	High
	mdc	Input	Ethernet management data clock.	-
	mdio_o	Input	Ethernet management data output.	-
	mdio_oe	Input	Ethernet management data output enable.	Set by the oepol generic in MAC.
RGMIII	gtx_clk	Input	Ethernet gigabit transmit clock.	-
	rx_clk	Input	Ethernet receive clock.	-
	tx_clk	Input	Ethernet receive clock.	-
	tx_clk_90	Input	Ethernet receive clock phase shifted 90 deg.	-
	rxd	Input	Ethernet receive data.	-
	rx_dv	Input	Ethernet receive data valid.	High
	mdint	Input	Ethernet management data input	-
	mdio_i	Input	Ethernet management interrupt	-
RGMIIO	reset	Output	External RGMII PHY reset	Low
	tx_clk	Output	Ethernet transmit clock output	-
	txd	Output	Ethernet transmit data.	-
	tx_en	Output	Ethernet transmit data valid.	-
	mdio_o	Output	Ethernet management data output.	-
	mdio_oe	Output	Ethernet management data output enable.	Set by the oepol generic.
	mdc	Output	Ethernet management data output enable.	Set by the oepol generic in MAC.

* see GRLIB IP Library User's Manual

90.9 Library dependencies

Table 1575 shows libraries used when instantiating the core (VHDL libraries).

*Table 1575.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	ETHERNET_MAC	Signals, component	GRETH_GBIT component declarations, GRETH_GBIT signals.
GAISLER	NET	Signals	Ethernet signals

90.10 Instantiation

The first example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.ethernet_mac.all;

entity rgmii_ex is
  port (
    clk    : in std_ulogic;
    rstn   : in std_ulogic;

    -- ethernet signals
    rgmiii :  in  eth_in_type;
    rgmiio :  in  eth_out_type
    );
end;

architecture rtl of rgmii_ex is

  -- AMBA signals
  signal apbi : apb_slv_in_type;
  signal apbo : apb_slv_out_vector := (others => apb_none);
  signal ethi : eth_in_type;
  signal etho : eth_out_type;

begin

  -- AMBA Components are instantiated here
  ...

  -- RGMII
  rgmii0 : rgmii
  generic map (
    pindex        => 11,
    paddr         => 16#010#,
    pmask         => 16#ff0#,
    tech          => fabtech,
    gmii          => CFG_GRETH1G,
    debugmem      => 1,
    abits         => 8,
    no_clk_mux    => 1,
    pirq          => 11,
    use90degtxclk => 1)
  port map (
    rstn     => rstn,
    gmiii    => ethi,
```

```
gmii0    => etho,
rgmiii   => rgmiii,
rgmiio   => rgmii0,
apb_clk  => apb_clk,
apb_rstn => apb_rstn,
apbi     => apbi,
apbo     => apbo(11));
```

91 REGFILE_3P 3-port RAM generator (2 read, 1 write)

91.1 Overview

The 3-port register file has two read ports and one write port. Each port has a separate address and data bus. All inputs are latched on the rising edge of clk. The read data appears on dataout directly after the clk rising edge. Note: on most technologies, the register file is implemented with two 2-port RAMs with combined write ports. Address width, data width and target technology is parametrizable through generics.

Write-through is supported if the function *syncram_2p_write_through(tech)* returns 1 for the target technology.

91.2 Configuration options

Table 1576 shows the configuration options of the core (VHDL generics).

*Table 1576.*Configuration options

Name	Function	Range	Default
tech	Technology selection	0 - NTECH	0
abits	Address bits. Depth of RAM is $2^{abits-1}$	see table 1577	-
dbits	Data width	see table 1577l	-
wrfst	Write-first (write-through). Only applicable to inferred technology	0 - 1	0
numregs	Not used		

Table 1577 shows the supported technologies for the core.

*Table 1577.*Supported technologies

Tech name	Technology	RAM cell	abit range	dbit range
axcel / axdsp	Actel AX/RTAX & RTAX-DSP	RAM64K36	2 - 12	unlimited
altera	All Altera devices	altsyncram	unlimited	unlimited
ihp25	IHP 0.25	flip-flops	unlimited	unlimited
inferred	Behavioural description	synthesis tool dependent		
rhumc	Rad-hard UMC 0.18	flip-flops	unlimited	unlimited
virtex	Xilinx Virtex, Virtex-E, Spartan-2	RAMB4_Sn	2 - 10	unlimited
virtex2	Xilinx Virtex2, Spartan3, Virtex4	RAMB16_Sn	2 - 14	unlimited
proasic3	Actel Proasic3	ram4k9	2 - 12	unlimited
lattice	Lattice XP/EC/ECP	dp8ka	2 - 13	unlimited
memvirage	Virage ASIC RAM	hdss2_64x32cm4sw0 hdss2_128x32cm4sw0 hdss2_256x32cm4sw0 hdss2_512x32cm4sw0	6 - 9	32
eclipse	Aeroflex/Quicklogic FPGA	RAM128x18_25um RAM256X9_25um RAM512X4_25um RAM1024X2_25um	2 - 10	unlimited
easic90	eASIC 90 nm Nextreme	eram	2 - 12	unlimited

91.3 Signal descriptions

Table 1578 shows the interface signals of the core (VHDL ports).

*Table 1578.*Signal descriptions

Signal name	Field	Type	Function	Active
WCLK	N/A	Input	Write port clock	
WADDR	N/A	Input	Write address	
WDATA	N/A	Input	Write data	
WE	N/A	Input	Write enable	High
RCLK	N/A	Input	Read ports clock	-
RADDR1	N/A	Input	Read port1 address	-
RE1	N/A	Input	Read port1 enable	High
RDATA1	N/A	Output	Read port1 data	-
RADDR2	N/A	Input	Read port2 address	-
RE2	N/A	Input	Read port2 enable	High
RDATA2	N/A	Output	Read port2 data	-

91.4 Library dependencies

Table 1579 shows libraries used when instantiating the core (VHDL libraries).

*Table 1579.*Library dependencies

Library	Package	Imported unit(s)	Description
TECHMAP	GENCOMP	Constants	Technology contants

91.5 Component declaration

The core has the following component declaration.

```
library techmap;
use techmap.gencomp.all;

component regfile_3p
  generic (tech : integer := 0; abits : integer := 6; dbits : integer := 8;
           wrfst : integer := 0; numregs : integer := 64);
  port (
    wclk   : in  std_ulogic;
    waddr  : in  std_logic_vector((abits -1) downto 0);
    wdata  : in  std_logic_vector((dbits -1) downto 0);
    we     : in  std_ulogic;
    rclk   : in  std_ulogic;
    raddr1 : in  std_logic_vector((abits -1) downto 0);
    re1    : in  std_ulogic;
    rdata1 : out std_logic_vector((dbits -1) downto 0);
    raddr2 : in  std_logic_vector((abits -1) downto 0);
    re2    : in  std_ulogic;
    rdata2 : out std_logic_vector((dbits -1) downto 0)
  );
  end component;
```

92 RSTGEN - Reset generation

92.1 Overview

The RSTGEN reset generator implements input reset signal synchronization with glitch filtering and generates the internal reset signal. The input reset signal can be asynchronous.

92.2 Operation

The reset generator latches the value of the clock lock signal on each rising edge of the clock. The lock signal serves as input to a five-bit shift register. The three most significant bits of this shift register are clocked into the reset output register. The reset signal to the system is high when both the reset output register and the reset input signal are high. Since the output register depends on the system clock the active low reset output from the core will go high synchronously to the system clock. The raw reset output does not depend on the system clock or clock lock signal and is polarity adjusted to be active low.

The VHDL generic *syncrst* determines how the core resets its shift register and the reset output register. When *syncrst* is set to 1 the core's shift register will have an synchronous reset and no reset signal will be connected to the output reset register, see figure 258. Note that the core's reset output signal will always go low when the input reset signal is activated.

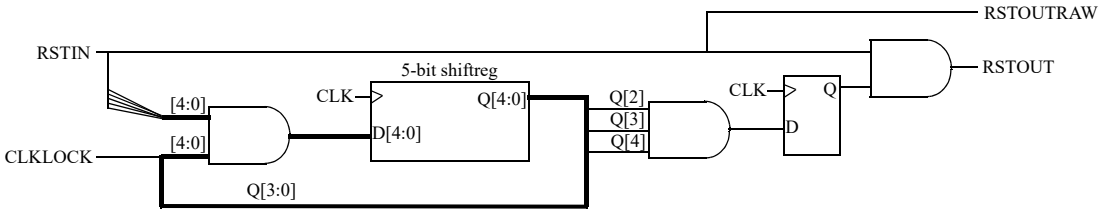


Figure 258. Reset generator with VHDL generic syncrst set to 1

When *syncrst* is 0 the shift register will be reset asynchronously together with the reset output register. Figure 259 shows the reset generator when scan test support is disabled. The shift register reset will be connected to the core's normal reset input and the test reset input will be unused. When scan test support is enabled, the core's test reset input can be connected to the reset input on both registers. The reset signal to use for the registers is selected with the test enable input, see figure 260.

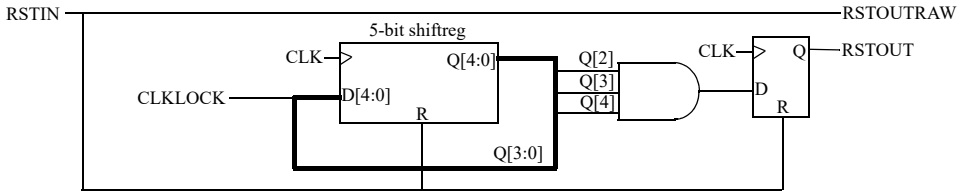


Figure 259. Reset generator with VHDL generic syncrst set to 0 and scan test disabled

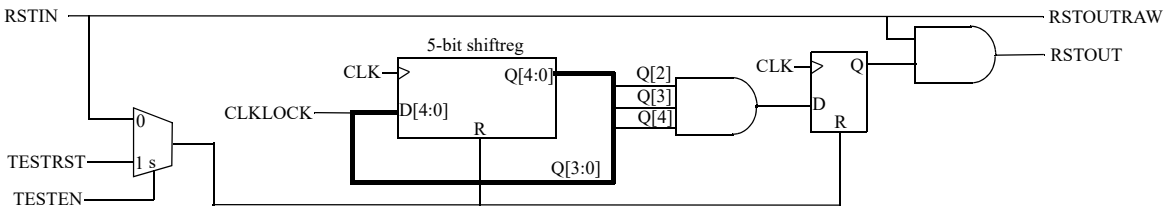


Figure 260. Reset generator with VHDL generic syncrst set to 0 and scan test enabled

When *syncin* is 1 the reset input is synchronized to the same clock domain as the rstgen block.

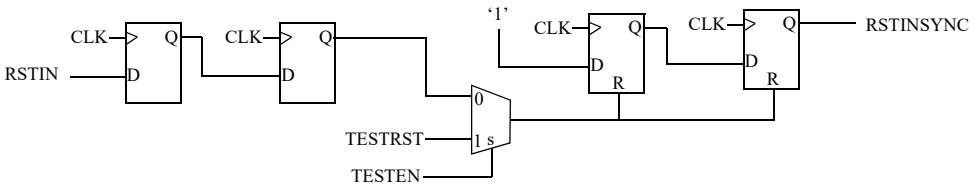


Figure 261. Extra Reset generator logic with VHDL generic syncin set to 1 to synchronize input reset and scan test enabled

92.3 Configuration options

Table 1580 shows the configuration options of the core (VHDL generics).

*Table 1580.*Configuration options

Generic name	Function	Allowed range	Default
acthigh	Set to 1 if reset input is active high. The core outputs an active low reset.	0 - 1	0
syncrst	When this generic is set to 1 the reset signal will use a synchronous reset to reset the filter registers. When this generic is set to 1 the TESTRST and TESTEN inputs will not be used.	0 - 1	0
scanen	Setting this generic to 1 enables scan test support. This connects the TESTRST input via a multiplexer so that the TESTRST and TESTEN signals can be used to asynchronously reset the core's registers. This also requires that the generic syncrst is set to 0.	0 - 1	0
syncin	Setting this generic to 1 will add reset synchronizer to the input reset. This option can be used to break false timing paths in designs when input reset is not generated from same clock domain as the input clock of rstgen	0 - 1	0

92.4 Signal descriptions

Table 1581 shows the interface signals of the core (VHDL ports).

*Table 1581.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTIN	N/A	Input	Reset	-
CLK	N/A	Input	Clock	-
CLKLOCK	N/A	Input	Clock lock	High
RSTOUT	N/A	Output	Filtered reset	Low
RSTOUTRAW	N/A	Output	Raw reset	Low
TESTRST	N/A	Input	Test reset	-
TESTEN	N/A	Input	Test enable	High

92.5 Signal definitions and reset values

The signals and their reset values are described in table 1582.

*Table 1582.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
resetn	Input	Reset	Low	

92.6 Timing

The timing waveforms and timing parameters are shown in figure 262 and are defined in table 1583.

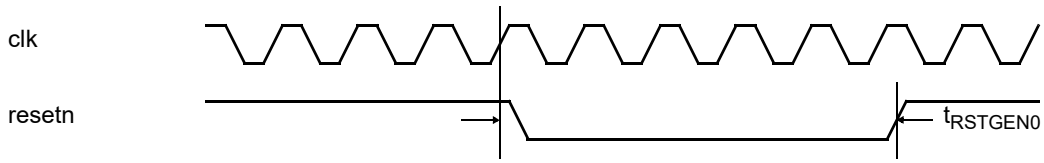


Figure 262. Timing waveforms

*Table 1583.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{RSTGEN0}$	asserted period	-	TBD	-	ns

Note: The *resetn* input is re-synchronized internally. The signals does not have to meet any setup or hold requirements.

92.7 Library dependencies

Table 1584 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1584.*Library dependencies

Library	Package	Imported unit(s)	Description
GAISLER	MISC	Component	Component definition

92.8 Instantiation

This example shows how the core can be instantiated together with the GRLIB clock generator.

```
library ieee;
use ieee.std_logic_1164.all;
library techmap;
use techmap.gencomp.all;
library gaisler;
use gaisler.misc.all;

entity rstgen_ex is
  port (
    resetn  : in  std_ulogic;
    clk     : in  std_ulogic; -- 50 MHz main clock
    pllref  : in  std_ulogic;
    testrst : in std_ulogic;
    testen  : in std_ulogic
  );
end;

architecture example of rstgen_ex is

signal lclk, clkm, rstn, rstraw, sdclkl, clk50: std_ulogic;
signal cgi   : clkgen_in_type;
```

```
signal cgo   : clkgen_out_type;

begin
  cgi.pllctrl <= "00"; cgi.pllrst <= rstraw;
  pllref_pad : clkpad generic map (tech => padtech) port map (pllref, cgi.pllref);
  clk_pad : clkpad generic map (tech => padtech) port map (clk, lclk);
  clkgen0 : clkgen  -- clock generator
    generic map (clktech, CFG_CLKMUL, CFG_CLKDIV, CFG_MCTRL_SDEN,
                 CFG_CLK_NOFB, 0, 0, 0, BOARD_FREQ)
    port map (lclk, lclk, clkm, open, open, sdclkl, open, cgi, cgo, open, clk50);
  sdclk_pad : outpad generic map (tech => padtech, slew => 1, strength => 24)
    port map (sdclk, sdclkl);

  resetn_pad : inpad generic map (tech => padtech) port map (resetn, rst);

  rst0 : rstgen  -- reset generator
    generic map (acthigh => 0, syncrst => 0, scanen => 1)
    port map (rst, clkm, cgo.clklock, rstn, rstraw, testrst, testen);
end;
```

93 GR(2^4)(68, 60, 8, T=1) - QEC/QED error correction code encoder/decoder

93.1 Overview

The gf4_e1 VHDL package provides functions for encoding and decoding a Bose Chaudhuri Hocquenghem (BCH) type of code. It is a Quad Error Correction/Quad Error Detection (QEC/QED) code.

The data symbols are 4-bit wide, represented as GF(2^4). The has the capability to detect and correct a single symbol error anywhere in the codeword. The data is represented as 60 bits and the checksum is represented as 8 bits, and the code can correct up to four bit errors when located in the same nibble.

93.2 Code

The code has the following definition:

- there are 4 bits per symbol;
- there are 17 symbols per codeword, of which 2 symbols represent the checksum;
- the code is systematic;
- the code can correct one symbol error per codeword;
- the field polynomial is

$$f(x) = x^4 + x + 1$$

- all multiplications are performed as Galois Field multiplications over the above field polynomial
- all additions/subtractions are performed as Galois Field additions (i.e. bitwise exclusive-or)

93.3 Encoding

- a codeword is defined as 17 symbols:

  $[c_0, c_1, c_2, c_3, c_4, c_5, c_6, c_7, c_8, c_9, c_{10}, c_{11}, c_{12}, c_{13}, c_{14}, c_{15}, c_{16}]$

  where c_0 to c_{14} represent information symbols and c_{15} to c_{16} represent check symbols.
- c_{15} is calculated as follows

$$c_{15} = \sum_{0}^{14} (k_i \times c_i)$$

- c_{16} is calculated as follows

$$c_{16} = \sum_{0}^{14} c_i$$

- where the constant vector k is defined as:

  k_0=0xF, k_1=0xE, ..., k_{14}=0x1 (one can assume k_{15}=0x1 and k_{16}=0x1 for correction purposes)

93.4 Decoding

- the corrupt codeword is defined as 17 symbols:

  $[r_0, r_1, r_2, r_3, r_4, r_5, r_6, r_7, r_8, r_9, r_{10}, r_{11}, r_{12}, r_{13}, r_{14}, r_{15}, r_{16}]$
- the corrupt codeword can also be defined as 17 uncorrupt symbols and an error:

  $[c_0, c_1, c_2, c_3, c_4, c_5, c_6, c_7, c_8, c_9, c_{10}, c_{11}, c_{12}, c_{13}, c_{14}, c_{15}, c_{16}] + [e_x]$

  where the error is defined as e_x, e being the unknown magnitude and
  x being the unknown index position in the codeword

- recalculated checksum rc_0 is calculated as follows (k_i is as defined above, x being the unknown index)

$$rc_0 = \sum_{0}^{14}(k_i \times r_i) = \sum_{0}^{14}(k_i \times c_i) + (k_x \times e_x)$$

- recalculated rc_1 is calculated as follows

$$rc_1 = \sum_{0}^{14} r_i = \sum_{0}^{14} c_i + e_x$$

- syndrome s_0 is calculated as follows

$$s_0 = rc_0 + r_{15} = \sum_{0}^{14}(k_i \times r_i) + \sum_{0}^{14}(k_i \times c_i) = k_x \times e_x$$

- syndrome s_1 is calculated as follows, which gives the magnitude (not applicable to c_{15} and c_{16})

$$s_1 = rc_1 + r_{16} = \sum_{0}^{14} r_i + \sum_{0}^{14} c_i = e_x$$

- in case s_0 and s_1 are both non-zero, to located the error in range c_0 to c_{14}, multiply error magnitude e_x with each element of the constant vector defined above:

$$k_i e_x = k_i \times s_1 = k_i \times e_x \qquad i = [0,14]$$

- search the resulting vector to find the element matching syndrome s_0, the resulting index i points to the error location (applicable only to i in [0, 14])

$$k_i e_x \Leftrightarrow k_i \times e_x$$

- finally perform the correction (applicable only to i in [0, 14])

$$c_i = r_i - s_1 = r_i - e_x = (c_i - e_x) \times e_x = c_i - e_x + e_x = c_i$$

- when s_0 is zero and s_1 is non-zero, the error is located in checksum r_{15}, no correction is necessary
- when s_1 is zero and s_0 is non-zero, the error is located in checksum r_{16}, no correction is necessary
- when s_0 and s_1 are both zero, no error has been detected, no correction is necessary

93.5 Capability

The decoder has the following capabilities. It detects and corrects up to four bit errors in the same nibble. The described errors can be located anywhere in the codeword.

93.6 Operation

93.6.1 Encoder

The encoder is defined by the gf4_60_8_encode function. The function is called with the 60-bit wide data that should be encoded, and returns a 68-bit wide codeword of which bits 67 downto 8 represent the data and bits 7 downto 0 represent the checksum.

93.6.2 Decoder

The decoder is defined by the gf4_60_8_decode function.

The gf4_60_8_decode function calculates the syndromes, calculates the error magnitude and the error location, and returns a bit indicating whether an error has been detected and corrected, and the corrected data.

The function is called with a 68-bit wide codeword of which bits 67 downto 8 represent the data and bits 7 downto 0 represent the checksum. It returns the record type gf4_60_8_type, containing the 60-bit wide corrected data and an indication if an error was detected and corrected over the complete codeword.

93.7 Type descriptions

Table 1585 shows the type declarations used by the functions in the package (VHDL types).

*Table 1585.*Type declarations

Name	Field	Type	Function	Active
gf4_60_8_type	cerr	Std_Logic	error corrected	
	data	Std_Logic_Vector(59 downto 0)	data	

93.8 Library dependencies

Table 1586 shows the libraries used when instantiating the functions in the package (VHDL libraries).

*Table 1586.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	StdLib	All	Common VHDL functions

93.9 Instantiation

This example shows how the functions in the package can be instantiated. Note that all input and outputs are synchronized to remove any timing constraints for pads in an example design. Timing analysis can then be made purely for the register-to-register paths.

```
library  IEEE;
use      IEEE.Std_Logic_1164.all;

entity gf4_60_8_encode_sync is
   port(
      clk:        in       std_ulogic;
      data:       in       std_logic_vector(59 downto 0);
      codeword:   out      std_logic_vector(67 downto 0));
end entity gf4_60_8_encode_sync;

library  grlib;
use      grlib.gf4_e1.all;

architecture rtl of gf4_60_8_encode_sync is
   signal   int_data:      std_logic_vector(59 downto 0);
   signal   int_codeword:  std_logic_vector(67 downto 0);
begin
   process(clk)
   begin
      if rising_edge(clk) then
          codeword      <= int_codeword;
          int_codeword  <= gf4_60_8_encode(int_data);
          int_data      <= data;
      end if;
   end process;
end architecture;
```

```
library  IEEE;
use      IEEE.Std_Logic_1164.all;

entity gf4_60_8_decode_sync is
   port(
         clk:        in    std_ulogic;
         codeword:   in    std_logic_vector(67 downto 0);
         cerr:       out   std_ulogic;
         data:       out   std_logic_vector(59 downto 0));
end entity gf4_60_8_decode_sync;

library  grlib;
use      grlib.gf4_e1.all;

architecture rtl of gf4_60_8_decode_sync is
   signal   int_codeword:  std_logic_vector(67 downto 0);
   signal   int_result:    gf4_60_8_type;
begin
   process(clk)
   begin
      if rising_edge(clk) then
         cerr           <= int_result.cerr;
         data           <= int_result.data;
         int_result     <= gf4_60_8_decode(int_codeword);
         int_codeword   <= codeword;
      end if;
   end process;
end architecture;
```

94 RS(24, 16, 8, E=1) - Reed-Solomon encoder/decoder

94.1 Overview

The rs_gf4_e1 VHDL package provides functions for encoding and decoding data with a Reed-Solomon code. It also provides a data type storing intermediate results from the functions.

The Reed-Solomon data symbols are 4-bit wide, represented as GF(2^4). The Reed-Solomon code is a shortened RS(15, 13, 2) code, represented as RS(6, 4, 2). It has the capability to detect and correct a single symbol error anywhere in the codeword. The data is represented as 16 bits and the checksum is represented as 8 bits, and the code can correct 4-bit errors when located in the same nibble.

94.2 Capability

The Reed-Solomon decoder has the following capabilities. The described errors can be located anywhere in the codeword.

It detects and corrects any single bit error.

It detects 63% of all double bit errors and reports them as multiple bit errors.

It detects 27% of all double bit errors and reports them (incorrectly) as single bit errors.

It detects 63,5% of all triple bit errors and reports them as multiple bit errors.

It detects 36% of all triple bit errors and reports them (incorrectly) as single bit errors.

It does not detect 0,5% of all triple bit errors and reports them (incorrectly) as without errors.

It detects 63,5% of all quadruple bit errors and reports them as multiple bit errors.

It detects 36% of all quadruple bit errors and reports them (incorrectly) as single bit errors.

It does not detect 0,5% of all quadruple bit errors and reports them (incorrectly) as without error.

It detects and corrects up to four bit errors in the same nibble.

94.3 Operation

94.3.1 Encoder

The encoder is defined by the rs_16_8_encode function. The function is called with the 16-bit wide data that should be encoded, and returns 24-bit wide codeword of which bits 0 to 15 represent the data and bits 16 to 23 represent the checksum.

94.3.2 Decoder

The decoder is defined by the rs_16_8_check, rs_16_8_precorrect and rs_16_8_correct functions. The decoder has been split in three functions to facilitate pipelining, with each function being fairly balanced with respect to the depth of the resulting combinatorial logic.

The rs_16_8_check function calculates the syndrome and returns a bit indicating whether an error has been detected. Note that it can be any type of error: correctable or uncorrectable. The function is called with a 24-bit wide codeword of which bits 0 to 15 represent the data and bits 16 to 23 represent

the checksum. It returns the record type rs_16_8_type, containing the 16-bit wide data to be corrected, the syndrome and an indication if an error was detected over the complete codeword.

The rs_16_8_precorrect function is called with the intermediate result from the rs_16_8_check function. The input is the record type rs_16_8_type. It returns the record type rs_16_8_type, containing the 16-bit wide data to be corrected, the syndrome, intermediate data and an indication if an error was detected over the complete codeword.

The rs_16_8_correct function is called with the intermediate result from the rs_16_8_precorrect function. The input is the record type rs_16_8_type. It returns the record type rs_16_8_type, containing the corrected 16-bit wide data, an indication if the error was correctable or non-correctable over the complete codeword, and the union of the two.

To pipeline the decoder, the rs_16_8_check function should be called in the first stage and the intermediated result should be stored. Note that the intermediate result contains the input data required for the correction in the next stage. The rs_16_8_precorrect function should be called in the second stage. The rs_16_8_correct function should be called in the third stage.

94.4 Type descriptions

Table 1587 shows the type declarations used by the functions in the package (VHDL types).

*Table 1587.*Type declarations

Name	Field	Type	Function	Active
rs_16_8_type	err	Std_Logic	error detected	High
	cerr	Std_Logic	error corrected	
	merr	Std_Logic	errors uncorrected	
	data	Std_Logic_Vector(0 to 15)	data	
	s_1	Std_Logic_Vector(0 to 3)	-	-
	s_2	Std_Logic_Vector(0 to 3)	-	-
	elp_3_1	Std_Logic_Vector(0 to 3)	-	-

94.5 Library dependencies

Table 1588 shows the libraries used when instantiating the functions in the package (VHDL libraries).

*Table 1588.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	StdLib	All	Common VHDL functions

94.6 Instantiation

This example shows how the functions in the package can be instantiated.

The example design shows a codec for which the decoder is pipelined, with the error flag output one clock cycle earlier than the corrected data. Note that all input and outputs are synchronised to remove any timing constraints for pads in an example design. Timing analysis can be made purely for the register-to-register paths.

```
library  IEEE;
use      IEEE.Std_Logic_1164.all;

entity rs_gf4_16_8_codec is
   port(
      clk:        in    Std_Logic;
```

```
      din:        in    Std_Logic_Vector(0 to 15);       -- encoder input
      cout:       out   Std_Logic_Vector(0 to 23);       -- encoder output

      cin:        in    Std_Logic_Vector(0 to 23);       -- decoder input
      terr:       out   Std_Logic;                       -- intermediate error

      dout:       out   Std_Logic_Vector(0 to 15);       -- decoder output
      err:        out   Std_Logic;                       -- error detected
      cerr:       out   Std_Logic;                       -- error corrected
      merr:       out   Std_Logic);                      -- errors uncorrected
end entity;

library  grlib;
use      grlib.rs_gf4_e1.all;

architecture rtl of rs_gf4_16_8_codec is
   signal   s_din:      Std_Logic_Vector(0 to 15);
   signal   s_cout:     Std_Logic_Vector(0 to 23);

   signal   s_cin:      Std_Logic_Vector(0 to 23);
   signal   s_dout:     Std_Logic_Vector(0 to 15);
   signal   s_err:      Std_Logic;
   signal   s_cerr:     Std_Logic;
   signal   s_merr:     Std_Logic;

   signal   check:      rs_16_8_type;                    -- intermediate
   signal   precorr:    rs_16_8_type;
   signal   corr:       rs_16_8_type;
begin
   SyncronizeInput: process(clk)
   begin
      if Rising_Edge(clk) then
         s_din       <= din;
         s_cin       <= cin;
      end if;
   end process;

   SyncronizeOutput: process(clk)
   begin
      if Rising_Edge(clk) then
         cout        <= s_cout;
         err         <= corr.err;
         cerr        <= corr.cerr;
         merr        <= corr.merr;
         dout        <= corr.data;
         terr        <= check.err;
      end if;
   end process;

   encoder: process(clk)
   begin
      if Rising_Edge(clk) then
         s_cout      <= rs_16_8_encode(s_din);
      end if;
   end process;

   decoder: process(clk)
   begin
      if Rising_Edge(clk) then
         corr        <= rs_16_8_correct(precorr);     -- third phase
         precorr     <= rs_16_8_precorrect(check);    -- second phase
         check       <= rs_16_8_check(s_cin);         -- first phase
      end if;
   end process;
end architecture rtl;
```

95 RS(48, 32, 16, E=1+1) - Reed-Solomon encoder/decoder - interleaved

95.1 Overview

The rs_gf4_e1 VHDL package provides functions for encoding and decoding data with a Reed-Solomon code. It also provides a data type storing intermediate results from the functions.

The Reed-Solomon data symbols are 4-bit wide, represented as GF(2^4). The Reed-Solomon code is a shortened RS(15, 13, 2) code, represented as RS(6, 4, 2). It has the capability to detect and correct a single symbol error anywhere in the codeword. The data is represented as 16 bits and the checksum is represented as 8 bits, and the code can correct 4-bit errors when located in the same nibble.

The gf4_32_16 functions provide an interleaved RS(6, 4, 2) where the data is represented as 32 bits and the checksum is represented as 16 bits, and the code can correct two 4-bit errors when each error is located in a nibble and not in the same original RS(6, 4, 2) codeword. The codewords are interleaved nibble-wise.

95.2 Capability

The Reed-Solomon decoder has the same capabilities as the original RS(6, 4, 2) code, but distributed per original RS(6, 4, 2) codeword.

95.3 Operation

95.3.1 Encoder

The encoder is defined by the rs_32_16_encode function. The function is called with the 32-bit wide data that should be encoded, and returns 48-bit wide codeword of which bits 0 to 31 represent the data and bits 32 to 47 represent the checksum.

95.3.2 Decoder

The decoder is defined by the rs_32_16_check, rs_32_16_precorrect and rs_32_16_correct functions. The decoder has been split in three functions to facilitate pipelining, with each function being fairly balanced with respect to the depth of the resulting combinatorial logic.

The rs_32_16_check function calculates the syndrome and returns a bit indicating whether an error has been detected. Note that it can be any type of error: correctable or uncorrectable. The function is called with a 48-bit wide codeword of which bits 0 to 31 represent the data and bits 32 to 47 represent the checksum. It returns the record type rs_32_16_type, containing the 32-bit wide data to be corrected, the syndrome and an indication if an error was detected over the two complete codewords.

The rs_32_16_precorrect function is called with the intermediate result from the rs_32_16_check function. The input is the record type rs_32_16_type. It returns the record type rs_32_16_type, containing the 32-bit wide data to be corrected, the syndrome, intermediate data and an indication if an error was detected over the two complete codewords.

The rs_32_16_correct function is called with the intermediate result from the rs_32_16_precorrect function. The input is the record type rs_32_16_type. It returns the record type rs_32_16_type, containing the corrected 32-bit wide data, an indication if the error was correctable or non-correctable over the complete two codewords, and the union of the two.

To pipeline the decoder, the rs_32_16_check function should be called in the first stage and the intermediated result should be stored. Note that the intermediate result contains the input data required for the correction in the next stage. The rs_32_16_precorrect function should be called in the second stage. The rs_32_16_correct function should be called in the third stage.

95.4 Type descriptions

Table 1589 shows the type declarations used by the functions in the package (VHDL types).

*Table 1589.*Type declarations

Name	Field	Type	Function	Active
rs_32_16_type	err	Std_Logic	error detected	High
	cerr	Std_Logic	error corrected	
	merr	Std_Logic	errors uncorrected	
	data	Std_Logic_Vector(0 to 31)	data	
	e_0	Std_Logic	-	-
	s_1_0	Std_Logic_Vector(0 to 3)	-	-
	s_2_0	Std_Logic_Vector(0 to 3)	-	-
	elp_3_1_0	Std_Logic_Vector(0 to 3)	-	-
	e_1	Std_Logic	-	-
	s_1_1	Std_Logic_Vector(0 to 3)	-	-
	s_2_1	Std_Logic_Vector(0 to 3)	-	-
	elp_3_1_1	Std_Logic_Vector(0 to 3)	-	-

95.5 Library dependencies

Table 1590 shows the libraries used when instantiating the functions in the package (VHDL libraries).

*Table 1590.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	StdLib	All	Common VHDL functions

96 RS(40, 32, 8, E=1) - Reed-Solomon encoder/decoder

96.1 Overview

The rs_gf4_e1 VHDL package provides functions for encoding and decoding data with a Reed-Solomon code. It also provides a data type storing intermediate results from the functions.

The Reed-Solomon data symbols are 4-bit wide, represented as GF(2^4). The Reed-Solomon code is a shortened RS(15, 13, 2) code, represented as RS(10, 8, 2). It has the capability to detect and correct a single symbol error anywhere in the codeword. The data is represented as 32 bits and the checksum is represented as 8 bits, and the code can correct 4-bit errors when located in the same nibble.

96.2 Operation

96.2.1 Encoder

The encoder is defined by the rs_32_8_encode function. The function is called with the 32-bit wide data that should be encoded, and returns 40-bit wide codeword of which bits 0 to 31 represent the data and bits 32 to 39 represent the checksum.

96.2.2 Decoder

The decoder is defined by the rs_32_8_check, rs_32_8_precorrect and rs_32_8_correct functions. The decoder has been split in three functions to facilitate pipelining, with each function being fairly balanced with respect to the depth of the resulting combinatorial logic.

The rs_32_8_check function calculates the syndrome and returns a bit indicating whether an error has been detected. Note that it can be any type of error: correctable or uncorrectable. The function is called with a 24-bit wide codeword of which bits 0 to 31 representsthe data and bits 32 to 39 represent the checksum. It returns the record type rs_32_8_type, containing the 32-bit wide data to be corrected, the syndrome and an indication if an error was detected over the complete codeword.

The rs_32_8_precorrect function is called with the intermediate result from the rs_32_8_check function. The input is the record type rs_32_8_type. It returns the record type rs_32_8_type, containing the 32-bit wide data to be corrected, the syndrome, intermediate data and an indication if an error was detected over the complete codeword.

The rs_32_8_correct function is called with the intermediate result from the rs_32_8_precorrect function. The input is the record type rs_32_8_type. It returns the record type rs_32_8_type, containing the corrected 32-bit wide data, an indication if the error was correctable or non-correctable over the complete codeword, and the union of the two.

To pipeline the decoder, the rs_32_8_check function should be called in the first stage and the intermediated result should be stored. Note that the intermediate result contains the input data required for the correction in the next stage. The rs_32_8_precorrect function should be called in the second stage. The rs_32_8_correct function should be called in the third stage.

96.3 Type descriptions

Table 1591 shows the type declarations used by the functions in the package (VHDL types).

*Table 1591.*Type declarations

Name	Field	Type	Function	Active
rs_32_8_type	err	Std_Logic	error detected	High
	cerr	Std_Logic	error corrected	
	merr	Std_Logic	errors uncorrected	
	data	Std_Logic_Vector(0 to 31)	data	
	s_1	Std_Logic_Vector(0 to 3)	-	-
	s_2	Std_Logic_Vector(0 to 3)	-	-
	elp_3_1	Std_Logic_Vector(0 to 3)	-	-

96.4 Library dependencies

Table 1592 shows the libraries used when instantiating the functions in the package (VHDL libraries).

*Table 1592.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	StdLib	All	Common VHDL functions

96.5 Instantiation

This example shows how the functions in the package can be instantiated.

The example design shows a codec for which the decoder is pipelined, with the error flag output one clock cycle earlier than the corrected data. Note that all input and outputs are synchronised to remove any timing constraints for pads in an example design. Timing analysis can be made purely for the register-to-register paths.

```
library  IEEE;
use      IEEE.Std_Logic_1164.all;

entity rs_gf4_32_8_codec is
   port(
      clk:        in    Std_Logic;

      din:        in    Std_Logic_Vector(0 to 31);       -- encoder input
      cout:       out   Std_Logic_Vector(0 to 39);       -- encoder output

      cin:        in    Std_Logic_Vector(0 to 39);       -- decoder input
      terr:       out   Std_Logic;                       -- intermediate error

      dout:       out   Std_Logic_Vector(0 to 31);       -- decoder output
      err:        out   Std_Logic;                       -- error detected
      cerr:       out   Std_Logic;                       -- error corrected
      merr:       out   Std_Logic);                      -- errors uncorrected
end entity;

library  grlib;
use      grlib.rs_gf4_e1.all;

architecture rtl of rs_gf4_32_8_codec is
   signal   s_din:      Std_Logic_Vector(0 to 31);
   signal   s_cout:     Std_Logic_Vector(0 to 39);

   signal   s_cin:      Std_Logic_Vector(0 to 39);
   signal   s_dout:     Std_Logic_Vector(0 to 31);
```

```
   signal   s_err:      Std_Logic;
   signal   s_cerr:     Std_Logic;
   signal   s_merr:     Std_Logic;

   signal   check:      rs_32_8_type;                    -- intermediate
   signal   precorr:    rs_32_8_type;
   signal   corr:       rs_32_8_type;
begin
   SyncronizeInput: process(clk)
   begin
      if Rising_Edge(clk) then
         s_din       <= din;
         s_cin       <= cin;
      end if;
   end process;

   SyncronizeOutput: process(clk)
   begin
      if Rising_Edge(clk) then
         cout        <= s_cout;
         err         <= corr.err;
         cerr        <= corr.cerr;
         merr        <= corr.merr;
         dout        <= corr.data;
         terr        <= check.err;
      end if;
   end process;

   encoder: process(clk)
   begin
      if Rising_Edge(clk) then
         s_cout      <= rs_32_8_encode(s_din);
      end if;
   end process;

   decoder: process(clk)
   begin
      if Rising_Edge(clk) then
         corr        <= rs_32_8_correct(precorr);        -- third phase
         precorr     <= rs_32_8_precorrect(check);       -- second phase
         check       <= rs_32_8_check(s_cin);            -- first phase
      end if;
   end process;
end architecture rtl;
```

97 RS(48, 32, 16, E=2) - Reed-Solomon encoder/decoder

97.1 Overview

The rs_gf4_e2 VHDL package provides functions for encoding and decoding data with a Reed-Solomon code. It also provides a data type storing intermediate results from the functions.

The Reed-Solomon data symbols are 4-bit wide, represented as GF(2^4). The Reed-Solomon code is a shortened RS(15, 11, 4) code, represented as RS(12, 8, 4). It has the capability to detect and correct two symbol errors anywhere in the codeword. The data is represented as 32 bits and the checksum is represented as 16 bits, and the code can correct up to two 4-bit errors when located within nibble boundaries.

97.2 Operation

97.2.1 Encoder

The encoder is defined by the rs_32_16_2_encode function. The function is called with the 32-bit wide data that should be encoded, and returns 48-bit wide codeword of which bits 0 to 31 represent the data and bits 32 to 47 represent the checksum.

97.2.2 Decoder

The decoder is defined by the rs_32_16_2_check, rs_32_16_2_precorrect and rs_32_16_2_correct functions. The decoder has been split in three functions to facilitate pipelining, with each function being fairly balanced with respect to the depth of the resulting combinatorial logic.

The rs_32_16_2_check function calculates the syndrome and returns a bit indicating whether an error has been detected. Note that it can be any type of error: correctable or uncorrectable. The function is called with a 48-bit wide codeword of which bits 0 to 31 represent the data and bits 32 to 47 represent the checksum. It returns the record type rs_32_16_2_type, containing the 32-bit wide data to be corrected, the syndrome and an indication if an error was detected.

The rs_32_16_2_precorrect function is called with the intermediate result from the rs_32_16_2_check function. The input is the record type rs_32_16_2_type. It returns the record type rs_32_16_2_type, containing the 32-bit wide data to be corrected, the syndrome, intermediate data and an indication if an error was detected.

The rs_32_16_2_correct function is called with the intermediate result from the rs_32_16_2_precorrect function. The input is the record type rs_32_16_2_type. It returns the record type rs_32_16_2_type, containing the corrected 32-bit wide data, an indication if the error was correctable or non-correctable, and the union of the two.

To pipeline the decoder, the rs_32_16_2_check function should be called in the first stage and the intermediated result should be stored. Note that the intermediate result contains the input data required for the correction in the next stage. The rs_32_16_2_precorrect function should be called in the second stage. The rs_32_16_2_correct function should be called in the third stage.

97.3 Type descriptions

Table 1593 shows the type declarations used by the functions in the package (VHDL types).

*Table 1593.*Type declarations

Name	Field	Type	Function	Active
rs_32_16_2_type	err	Std_Logic	errors detected	High
	cerr	Std_Logic	errors corrected	High
	merr	Std_Logic	errors uncorrected	High
	data	Std_Logic_Vector(0 to 31)	data	
	l_u	Std_Logic_Vector(0 to 1)	indicates number of detected errors, only for rs_32_16_2_correct function	
	s_1	Std_Logic_Vector(0 to 3)		
	s_2	Std_Logic_Vector(0 to 3)		
	s_3	Std_Logic_Vector(0 to 3)		
	s_4	Std_Logic_Vector(0 to 3)		
	elp_5_1	Std_Logic_Vector(0 to 3)	indicates index of detected error in code-word, only for rs_32_16_2_correct function: 0x0 = codeword(0:3) 0x1 = codeword(4:7) 0x2 = codeword(8:11) 0x3 = codeword(12:15) 0x4 = codeword(16:19) 0x5 = codeword(20:23) 0x6 = codeword(24:27) 0x7 = codeword(28:31) 0x8 = codeword(32:35) 0x9 = codeword(36:39) 0xA = codeword(40:43) 0xB = codeword(44:47) 0xF = unidentified (can be used with erasure information)	
	elp_5_2	Std_Logic_Vector(0 to 3)	indicates index of detected error, as above	

97.4 Library dependencies

Table 1594 shows the libraries used when instantiating the functions in the package (VHDL libraries).

*Table 1594.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	StdLib	All	Common VHDL functions

97.5 Instantiation

This example shows how the functions in the package can be instantiated.

The example design shows a codec for which the decoder is pipelined, with the error flag output one clock cycle earlier than the corrected data. Note that all input and outputs are synchronised to remove

any timing constraints for pads in an example design. Timing analysis can be made purely for the register-to-register paths.

```
library  IEEE;
use      IEEE.Std_Logic_1164.all;

entity rs_gf4_32_16_2_codec is
   port(
      clk:        in    Std_Logic;

      din:        in    Std_Logic_Vector(0 to 31);       -- encoder input
      cout:       out   Std_Logic_Vector(0 to 47);       -- encoder output

      cin:        in    Std_Logic_Vector(0 to 47);       -- decoder input
      terr:       out   Std_Logic;                       -- intermediate error

      dout:       out   Std_Logic_Vector(0 to 31);       -- decoder output
      err:        out   Std_Logic;                       -- error detected
      cerr:       out   Std_Logic;                       -- error corrected
      merr:       out   Std_Logic);                      -- errors uncorrected
end entity;

library  grlib;
use      grlib.rs_gf4_e2.all;

architecture rtl of rs_gf4_32_16_2_codec is
   signal   s_din:      Std_Logic_Vector(0 to 31);
   signal   s_cout:     Std_Logic_Vector(0 to 47);
   signal   s_cin:      Std_Logic_Vector(0 to 47);
   signal   s_dout:     Std_Logic_Vector(0 to 31);
   signal   s_err:      Std_Logic;
   signal   s_cerr:     Std_Logic;
   signal   s_merr:     Std_Logic;
   signal   check:      rs_32_16_2_type;                 -- intermediate
   signal   precorr:    rs_32_16_2_type;
   signal   corr:       rs_32_16_2_type;
begin
   SyncronizeInput: process(clk)
   begin
      if Rising_Edge(clk) then
         s_din       <= din;
         s_cin       <= cin;
      end if;
   end process;

   SyncronizeOutput: process(clk)
   begin
      if Rising_Edge(clk) then
         cout        <= s_cout;
         err         <= corr.err;
         cerr        <= corr.cerr;
         merr        <= corr.merr;
         dout        <= corr.data;
         terr        <= check.err;
      end if;
   end process;

   encoder: process(clk)
   begin
      if Rising_Edge(clk) then
         s_cout      <= rs_32_16_2_encode(s_din);
      end if;
   end process;

   decoder: process(clk)
   begin
      if Rising_Edge(clk) then
         corr        <= rs_32_16_2_correct(precorr);     -- third phase
         precorr     <= rs_32_16_2_precorrect(check);    -- second phase
```

```
            check       <= rs_32_16_2_check(s_cin);         -- first phase
          end if;
        end process;
      end architecture rtl;
```

98 SDCTRL - 32/64-bit PC133 SDRAM Controller

98.1 Overview

The SDRAM controller handles PC133 SDRAM compatible memory devices attached to a 32 or 64 bit wide data bus. The controller acts as a slave on the AHB bus where it occupies a configurable amount of address space for SDRAM access. The SDRAM controller function is programmed by writing to a configuration register mapped into AHB I/O address space.

Chip-select decoding is provided for two SDRAM banks.

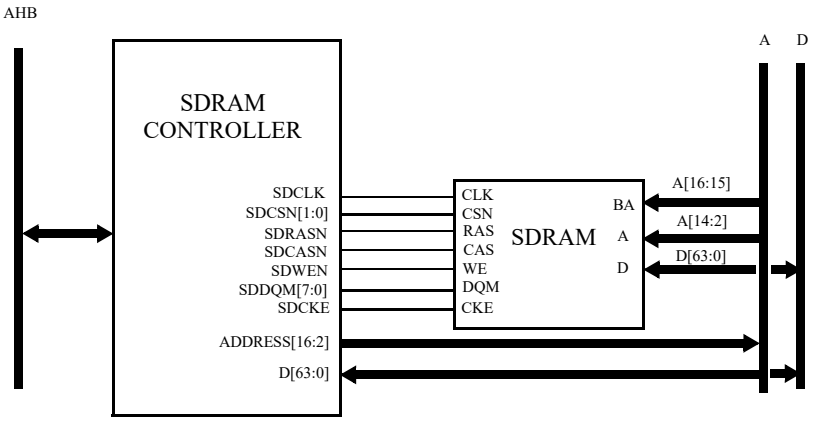


Figure 263. SDRAM Memory controller connected to AMBA bus and SDRAM

98.2 Operation

98.2.1 General

Synchronous dynamic RAM (SDRAM) access is supported to two banks of PC100/PC133 compatible devices. The controller supports 64M, 256M and 512M devices with 8 - 12 column-address bits, up to 13 row-address bits, and 4 banks. The size of each of the two banks can be programmed in binary steps between 4 Mbyte and 512 Mbyte. The operation of the SDRAM controller is controlled through the configuration register SDCFG (see section 98.3). The SDRAM bank's data bus width is configurable between 32 and 64 bits. When the VHDL generic *mobile* is set to a value not equal to 0, the controller supports mobile SDRAM.

98.2.2 Initialization

When the SDRAM controller is enabled, it automatically performs the SDRAM initialization sequence of PRECHARGE, 8x AUTO-REFRESH and LOAD-MODE-REG on both banks simultaneously. When mobile SDRAM functionality is enabled the initialization sequence is appended with a LOAD-EXTMODE-REG command. The controller programs the SDRAM to use page burst on read accesses and single location access on write accesses. If the *pwron* VHDL generic is 1, the initialization sequence is also sent automatically when reset is released. Note that some SDRAM devices require a stable clock of 100 us before any commands might be sent. When using on-chip PLL, this might not always be the case and the *pwron* VHDL generic should be set to 0 in such cases.

98.2.3 Configurable SDRAM timing parameters

To provide optimum access cycles for different SDRAM devices (and at different frequencies), three SDRAM parameters can be programmed through memory configuration register 2 (MCFG2): TCAS, TRP and TRFCD. The value of these fields affect the SDRAM timing as described in table 1595.

*Table 1595.*SDRAM programmable minimum timing parameters

SDRAM timing parameter	Minimum timing (clocks)
CAS latency, RAS/CAS delay (t_{CAS}, t_{RCD})	TCAS + 2
Precharge to activate (t_{RP})	TRP + 2
Auto-refresh command period (t_{RFC})	TRFC + 3
Activate to precharge (t_{RAS})	TRFC + 1
Activate to Activate (t_{RC})	TRP + TRFC + 4

If the TCAS, TRP and TRFC are programmed such that the PC100/133 specifications are fulfilled, the remaining SDRAM timing parameters will also be met. The table below shows typical settings for 100 and 133 MHz operation and the resulting SDRAM timing (in ns):

*Table 1596.*SDRAM example programming

SDRAM settings	t_{CAS}	t_{RC}	t_{RP}	t_{RFC}	t_{RAS}
100 MHz, CL=2; TRP=0, TCAS=0, TRFC=4	20	80	20	70	50
100 MHz, CL=3; TRP=0, TCAS=1, TRFC=4	30	80	20	70	50
133 MHz, CL=2; TRP=1, TCAS=0, TRFC=6	15	82	22	67	52
133 MHz, CL=3; TRP=1, TCAS=1, TRFC=6	22	82	22	67	52

When mobile SDRAM support is enabled, one additional timing parameter (TXSR) can be programmed though the Power-Saving configuration register.

*Table 1597.*Mobile SDRAM programmable minimum timing parameters

SDRAM timing parameter	Minimum timing (clocks)
Exit Self Refresh mode to first valid command (t_{XSR})	tXSR

98.2.4 Refresh

The SDRAM controller contains a refresh function that periodically issues an AUTO-REFRESH command to both SDRAM banks. The period between the commands (in clock periods) is programmed in the refresh counter reload field in the SDCFG register. Depending on SDRAM type, the required period is typically 7.8 or 15.6 µs (corresponding to 780 or 1560 clocks at 100 MHz). The generated refresh period is calculated as (reload value+1)/sysclk. The refresh function is enabled by setting bit 31 in SDCFG register.

98.2.5 Self Refresh

The self refresh mode can be used to retain data in the SDRAM even when the rest of the system is powered down. When in the self refresh mode, the SDRAM retains data without external clocking and refresh are handled internally. The memory array that is refreshed during the self refresh operation is defined in the extended mode register. These settings can be changed by setting the PASR bits in the Power-Saving configuration register. The extended mode register is automatically updated

when the PASR bits are changed. The supported “Partial Array Self Refresh” modes are: Full, Half, Quarter, Eighth, and Sixteenth array. “Partial Array Self Refresh” is only supported when mobile SDRAM functionality is enabled. To enable the self refresh mode, set the PMODE bits in the Power-Saving configuration register to “010” (Self Refresh). The controller will enter self refresh mode after every memory access (when the controller has been idle for 16 clock cycles), until the PMODE bits are cleared. When exiting this mode the controller introduce a delay defined by tXSR in the Power-Saving configuration register and a AUTO REFRESH command before any other memory access is allowed. The minimum duration of this mode is defined by tRAS. This mode is only available when the VHDL generic *mobile* is >= 1.

98.2.6 Power-Down

When entering the power-down mode all input and output buffers, excluding SDCKE, are deactivated. All data in the SDRAM is retained during this operation. To enable the power-down mode, set the PMODE bits in the Power-Saving configuration register to “001” (Power-Down). The controller will enter power-down mode after every memory access (when the controller has been idle for 16 clock cycles), until the PMODE bits is cleared. The REFRESH command will still be issued by the controller in this mode. When exiting this mode a delay of one clock cycles are added before issue any command to the memory. This mode is only available when the VHDL generic *mobile* is >= 1.

98.2.7 Deep Power-Down

The deep power-down operating mode is used to achieve maximum power reduction by eliminating the power of the memory array. Data will not be retained after the device enters deep power-down mode. To enable the deep power-down mode, set the PMODE bits in the Power-Saving configuration register to “101” (Deep Power-Down). To exit the deep power-down mode the PMODE bits in the Power-Saving configuration register must be cleared. The controller will respond with an AMBA ERROR response to an AMBA access, that will result in a memory access, during Deep Power-Down mode. This mode is only available when the VHDL generic *mobile* is >= 1 and mobile SDRAM functionality is enabled.

98.2.8 Temperature-Compensated Self Refresh

The settings for the temperature-compensation of the Self Refresh rate can be controlled by setting the TCSR bits in the Power-Saving configuration register. The extended mode register is automatically updated when the TCSR bits are changed. Note that some vendors implements a Internal Temperature-Compensated Self Refresh feature, which makes the memory ignore the TCSR bits. This functionality is only available when the VHDL generic *mobile* is >= 1 and mobile SDRAM functionality is enabled.

98.2.9 Drive Strength

The drive strength of the output buffers can be controlled by setting the DS bits in the Power-Saving configuration register. The extended mode register is automatically updated when the DS bits are changed. The available options are: full, three-quarter, one-half, and one-quarter drive strengths. This functionality is only available when the VHDL generic *mobile* is >= 1 and mobile SDRAM functionality is enabled.

98.2.10 SDRAM commands

The controller can issue four SDRAM commands by writing to the SDRAM command field in the SDRAM Configuration register: PRE-CHARGE, AUTO-REFRESH, LOAD-MODE-REG (LMR) and LOAD-EXTMODE-REG (EMR). If the LMR command is issued, the CAS delay as programmed in SDCFG will be used, remaining fields are fixed: page read burst, single location write, sequential burst. If the EMR command is issued, the DS, TCSR and PASR as programmed in Power-Saving configuration register will be used. The command field will be cleared after a command has been exe-

cuted. Note that when changing the value of the CAS delay, a LOAD-MODE-REGISTER command should be generated at the same time.

98.2.11 Read cycles

A read cycle is started by performing an ACTIVATE command to the desired bank and row, followed by a READ command with data read after the programmed CAS delay. A read burst is performed if a burst access has been requested on the AHB bus. The read cycle is terminated with a PRE-CHARGE command, no banks are left open between two accesses. Note that only word bursts are supported by the SDRAM controller. The AHB bus supports bursts of different sizes such as bytes and half-words but they cannot be used.

98.2.12 Write cycles

Write cycles are performed similarly to read cycles, with the difference that WRITE commands are issued after activation. A write burst on the AHB bus will generate a burst of write commands without idle cycles in-between. As in the read case, only word bursts are supported.

98.2.13 Address bus connection

The SDRAM address bus should be connected to SA[12:0], the bank address to SA[14:13], and the data bus to SD[31:0] or SD[63:0] if a 64-bit SDRAM data bus is used.

98.2.14 Data bus

The external SDRAM data bus is configurable to either 32 or 64 bits width, using the *sdbits* VHDL generic. A 64-bit data bus allows 64-bit (SO)DIMMs to be connected using the full data capacity of the devices. The polarity of the output enable signal to the data pads can be selected with the oepol generic. Sometimes it is difficult to fulfil the output delay requirements of the output enable signal. In this case, the vbdrive signal can be used instead of bdrive. Each index in this vector is driven by a separate register and a directive is placed on them so that they will not be removed by the synthesis tool.

98.2.15 Clocking

The SDRAM controller is designed for an external SDRAM clock that is in phase or slightly earlier than the internal AHB clock. This provides the maximum margin for setup and hold on the external signals, and allows highest possible frequency. For Xilinx and Altera devices, the GRLIB Clock Generator (CLKGEN) can be configured to produce a properly synchronized SDRAM clock. For other FPGA targets, the custom clock synchronization must be designed, or the inverted clock option can be used (see below). For ASIC targets, the SDRAM clock can be derived from the AHB clock with proper delay adjustments during place&route.

If the VHDL generic INVCLK is set, then all outputs from the SDRAM controller are delayed for 1/2 clock. This is done by clocking all output registers on the falling clock edge. This option can be used on FPGA targets where proper SDRAM clock synchronization cannot be achieved. The SDRAM clock can be the internal AHB clock without further phase adjustments. Since the SDRAM signals will only have 1/2 clock period to propagate, this option typically limits the maximum SDRAM frequency to 40 - 50 MHz.

98.2.16 Endianness

The core is designed for big-endian systems.

98.3 Registers

The memory controller is programmed through register(s) mapped into the AHB I/O space defined by the controllers AHB BAR1.

*Table 1598.*SDRAM controller registers

AHB address offset	Register
0x0	SDRAM Configuration register
0x4	SDRAM Power-Saving configuration register

Table 1599. 0x00 - SDCFG1 - SDRAM configuration register

31	30	29 27	26	25 23	22 21	20 18	17	16	15	14 0
Refresh	tRP	tRFC	tCD	SDRAM bank size	SDRAM col. size	SDRAM command	Page-Burst	MS	D64	SDRAM refresh load value
0	1	0b111	1	0	0b10	0	*	*	*	NR
rw	rw	rw	rw	rw	rw	rw	rw*	r	r	rw

31 SDRAM refresh. If set, the SDRAM refresh will be enabled.

30 SDRAM tRP timing. tRP will be equal to 2 or 3 system clocks (0/1). When mobile SDRAM support is enabled, this bit also represent the MSB in the tRFC timing.

29: 27 SDRAM tRFC timing. tRFC will be equal to 3 + field-value system clocks. When mobile SDRAM support is enabled, this field is extended with the bit 30.

26 SDRAM CAS delay. Selects 2 or 3 cycle CAS delay (0/1). When changed, a LOAD-COMMAND-REGISTER command must be issued at the same time. Also sets RAS/CAS delay (tRCD).

25: 23 SDRAM banks size. Defines the decoded memory size for each SDRAM chip select: “000”= 4 Mbyte, “001”= 8 Mbyte, “010”= 16 Mbyte .... “111”= 512 Mbyte.

When configured for 64-bit wide SDRAM data bus (sdbits=64), the meaning of this field doubles so that “000”=8 Mbyte, .., “111”=1024 Mbyte

22: 21 SDRAM column size. “00”=256, “01”=512, “10”=1024, “11”=2048 except when bit[25:23]=˜111˜ then ˜11˜=4096

20: 18 SDRAM command. Writing a non-zero value will generate an SDRAM command: “010”=PRE-CHARGE, “100”=AUTO-REFRESH, “110”=LOAD-COMMAND-REGISTER, “111”=LOAD-EXTENDED-COMMAND-REGISTER. The field is reset after command has been executed.

17 1 = pageburst is used for read operations, 0 = line burst of length 8 is used for read operations. (Only available when VHDL generic pageburst i set to 2)

16 Mobile SDR support enabled. ‘1’ = Enabled, ‘0’ = Disabled (read-only)

15 64-bit data bus (D64) - Reads ‘1’ if memory controller is configured for 64-bit data bus, otherwise ‘0’. Read-only.

14: 0 The period between each AUTO-REFRESH command - Calculated as follows: tREFRESH = ((reload value) + 1) / SYSCLK

*Table 1600.*0x04 - SDCFG2 - SDRAM Power-Saving configuration register

31	30	29 24	23 20	19	18 16	15 7	6	5	4	3	2 0
ME	CE	RESERVED	tXSR	R	PMODE	RESERVED		DS	TCSR		PASR
*	*	0	*	0	0	0		0	0		0
rw*	rw*	r	rw*	r	rw	r		rw	rw		rw

31 Mobile SDRAM functionality enabled. ‘1’ = Enabled (support for Mobile SDRAM), ‘0’ = disabled (support for standard SDRAM)

30 Clock enable (CE). This value is driven on the CKE inputs of the SDRAM. Should be set to ‘1’ for correct operation. This register bit is read only when Power-Saving mode is other then none.

29: 24 Reserved

*Table 1600.*0x04 - SDCFG2 - SDRAM Power-Saving configuration register

23: 20	SDRAM tXSR timing. tXSR will be equal to field-value system clocks. (Read only when Mobile SDR support is disabled).
19	Reserved
18: 16	Power-Saving mode (Read only when Mobile SDR support is disabled). “000”: none “001”: Power-Down (PD) “010”: Self-Refresh (SR) “101”: Deep Power-Down (DPD)
15: 7	Reserved
6: 5	Selectable output drive strength (Read only when Mobile SDR support is disabled). “00”: Full “01”: One-half “10”: One-quarter “11”: Three-quarter
4: 3	Reserved for Temperature-Compensated Self Refresh (Read only when Mobile SDR support is disabled). “00”: 70ªC “01”: 45ªC “10”: 15ªC “11”: 85ªC
2: 0	Partial Array Self Refresh (Read only when Mobile SDR support is disabled). “000”: Full array (Banks 0, 1, 2 and 3) “001”: Half array (Banks 0 and 1) “010”: Quarter array (Bank 0) “101”: One-eighth array (Bank 0 with row MSB = 0) “110”: One-sixteenth array (Bank 0 with row MSB = 00)

98.4 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x009. For description of vendor and device identifiers see GRLIB IP Library User’s Manual.

98.5 Implementation

98.5.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User’s Manual). The core makes use of synchronous reset and resets a subset of its internal registers. The registers driving SDRAM chip select and output enables for the SDRAM data bus have asynchronous reset.

98.6 Configuration options

Table 1601 shows the configuration options of the core (VHDL generics).

*Table 1601.*Configuration options

Generic	Function	Allowed range	Default
hindex	AHB slave index	1 - NAHBSLV-1	0
haddr	ADDR field of the AHB BAR0 defining SDRAM area. Default is 0xF0000000 - 0xFFFFFFFF.	0 - 16#FFF#	16#000#
hmask	MASK field of the AHB BAR0 defining SDRAM area.	0 - 16#FFF#	16#F00#
ioaddr	ADDR field of the AHB BAR1 defining I/O address space where SDCFG register is mapped.	0 - 16#FFF#	16#000#
iomask	MASK field of the AHB BAR1 defining I/O address space.	0 - 16#FFF#	16#FFF#
wprot	Write protection.	0 - 1	0
invclk	Inverted clock is used for the SDRAM.	0 - 1	0
pwron	Enable SDRAM at power-on initialization	0 - 1	0
sdbits	32 or 64-bit data bus width.	32, 64	32
oepol	Polarity of bdrive and vbdrive signals. 0=active low, 1=active high	0 - 1	0
pageburst	Enable SDRAM page burst operation. 0: Controller uses line burst of length 8 for read operations. 1: Controller uses pageburst for read operations. 2: Controller uses pageburst/line burst depending on PageBurst bit in SDRAM configuration register.	0 - 2	0
mobile	Enable Mobile SDRAM support 0: Mobile SDRAM support disabled 1: Mobile SDRAM support enabled but not default 2: Mobile SDRAM support enabled by default 3: Mobile SDRAM support only (no regular SDR support)	0 - 3	0

98.7 Signal descriptions

Table 1602 shows the interface signals of the core (VHDL ports).

*Table 1602.*Signal descriptions

Signal name	Field	Type	Function	Active
CLK	N/A	Input	Clock	-
RST	N/A	Input	Reset	Low
AHBSI	1)	Input	AHB slave input signals	-
AHBSO	1)	Output	AHB slave output signals	-
SDI	WPROT	Input	Not used	-
	DATA[63:0]	Input	Data	High
SDO	SDCKE[1:0]	Output	SDRAM clock enable	High
	SDCSN[1:0]	Output	SDRAM chip select	Low
	SDWEN	Output	SDRAM write enable	Low
	RASN	Output	SDRAM row address strobe	Low
	CASN	Output	SDRAM column address strobe	Low
	DQM[7:0]	Output	SDRAM data mask: DQM[7] corresponds to DATA[63:56], DQM[6] corresponds to DATA[55:48], DQM[5] corresponds to DATA[47:40], DQM[4] corresponds to DATA[39:32], DQM[3] corresponds to DATA[31:24], DQM[2] corresponds to DATA[23:16], DQM[1] corresponds to DATA[15:8], DQM[0] corresponds to DATA[7:0].	Low
	BDRIVE	Output	Drive SDRAM data bus	Low/High[2]
	VBDRIVE[31:0]	Output	Identical to BDRIVE but has one signal for each data bit. Every index is driven by its own register. This can be used to reduce the output delay.	Low/High[2]
	ADDRESS[16:2]	Output	SDRAM address	Low
	DATA[31:0]	Output	SDRAM data	Low

1) see GRLIB IP Library User's Manual

2) Polarity selected with the oepol generic

98.8 Library dependencies

Table 1603 shows libraries used when instantiating the core (VHDL libraries).

*Table 1603.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AHB signal definitions
GAISLER	MEMCTRL	Signals, component	Memory bus signals definitions, component declaration

98.9 Instantiation

This example shows how the core can be instantiated.

The example design contains an AMBA bus with a number of AHB components connected to it including the SDRAM controller. The external SDRAM bus is defined on the example designs port map and connected to the SDRAM controller. System clock and reset are generated by GR Clock Generator and Reset Generator.

SDRAM controller decodes SDRAM area:0x60000000 - 0x6FFFFFFF. SDRAM Configuration register is mapped into AHB I/O space on address (AHB I/O base address + 0x100).

```
library ieee;
use ieee.std_logic_1164.all;
library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.memctrl.all;
use gaisler.pads.all;   -- used for I/O pads
use gaisler.misc.all;

entity mctrl_ex is
  port (
    clk : in std_ulogic;
    resetn : in std_ulogic;
    pllref : in  std_ulogic;
sdcke    : out std_logic_vector ( 1 downto 0);  -- clk en
    sdcsn    : out std_logic_vector ( 1 downto 0);  -- chip sel
    sdwen    : out std_logic;                       -- write en
    sdrasn   : out std_logic;                       -- row addr stb
    sdcasn   : out std_logic;                       -- col addr stb
    sddqm    : out std_logic_vector (7 downto 0);  -- data i/o mask
    sdclk    : out std_logic;                       -- sdram clk output
    sa       : out std_logic_vector(14 downto 0); -- optional sdram address
    sd       : inout std_logic_vector(63 downto 0) -- optional sdram data
    );
end;

architecture rtl of mctrl_ex is

  -- AMBA bus (AHB and APB)
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbsi : ahb_slv_in_type;
  signal ahbso : ahb_slv_out_vector := (others => ahbs_none);
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);

signal sdi   : sdctrl_in_type;
  signal sdo   : sdctrl_out_type;

  signal clkm, rstn : std_ulogic;
signal cgi : clkgen_in_type;
  signal cgo : clkgen_out_type;
  signal gnd : std_ulogic;

begin

  -- Clock and reset generators
  clkgen0 : clkgen generic map (clk_mul => 2, clk_div => 2, sdramen => 1,
                                tech => virtex2, sdinvclk => 0)
  port map (clk, gnd, clkm, open, open, sdclk, open, cgi, cgo);

  cgi.pllctrl <= "00"; cgi.pllrst <= resetn; cgi.pllref <= pllref;

  rst0 : rstgen
  port map (resetn, clkm, cgo.clklock, rstn);

  -- SDRAM controller
  sdc : sdctrl generic map (hindex => 3, haddr => 16#600#, hmask => 16#F00#,
    ioaddr => 1, pwron => 0, invclk => 0)
```

```
    port map (rstn, clkm, ahbsi, ahbso(3), sdi, sdo);

  -- input signals
  sdi.data(31 downto 0) <= sd(31 downto 0);

  -- connect SDRAM controller outputs to entity output signals
  sa <= sdo.address; sdcke <= sdo.sdcke; sdwen <= sdo.sdwen;
  sdcsn <= sdo.sdcsn; sdrasn <= sdo.rasn; sdcasn <= sdo.casn;
  sddqm <= sdo.dqm;

--Data pad instantiation with scalar bdrive
sd_pad : iopadv generic map (width => 32)
port map (sd(31 downto 0), sdo.data, sdo.bdrive, sdi.data(31 downto 0));
end;

--Alternative data pad instantiation with vectored bdrive
sd_pad : iopadvv generic map (width => 32)
port map (sd(31 downto 0), sdo.data, sdo.vbdrive, sdi.data(31 downto 0));
end;
```

99 SPI2AHB - SPI to AHB bridge

99.1 Overview

The SPI to AHB bridge is an SPI slave that provides a link between a SPI bus (that consists of two data signals, one clock signal and one select signal) and AMBA AHB. On the SPI bus the slave acts as an SPI memory device where accesses to the slave are translated to AMBA accesses. The core can translate SPI accesses to AMBA byte, half-word or word accesses. The access size to use is configurable via the SPI bus.

The core synchronizes the incoming clock and can operate in systems where other SPI devices are driven by asynchronous clocks.

GRLIB also contains a SPI master/slave controller core, without an AHB interface, where the transfer of each individual byte is controlled by software via an APB interface, see the SPICTRL core documentation for more information.

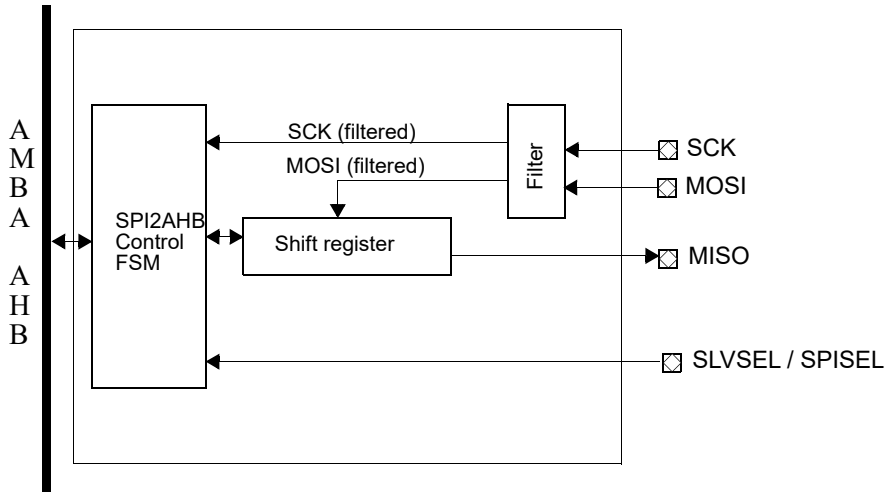


Figure 264. Block diagram, optional APB interface not shown

99.2 Transmission protocol

The SPI bus is a full-duplex synchronous serial bus. Transmission starts when a master selects a slave through the slave's Slave Select (SLVSEL) signal and the clock line SCK transitions from its idle state. Data is transferred from the master through the Master-Output-Slave-Input (MOSI) signal and from the slave through the Master-Input-Slave-Output (MISO) signal. In some systems with only one master and one slave, the Slave Select input of the slave may be always active and the master does not need to have a slave select output. This does not apply to this SPI to AHB bridge, the slave select signal must be used to mark the start and end of an operation.

During a transmission on the SPI bus data is either changed or read at a transition of SCK. If data has been read at edge n, data is changed at edge n+1. If data is read at the first transition of SCK the bus is said to have clock phase 0, and if data is changed at the first transition of SCK the bus has clock phase 1. The idle state of SCK may be either high or low. If the idle state of SCK is low, the bus has clock polarity 0 and if the idle state is high the clock polarity is 1. The combined values of clock polarity (CPOL) and clock phase (CPHA) determine the mode of the SPI bus. Figure 265 shows one byte (0x55) being transferred MSb first over the SPI bus under the four different modes. Note that the idle state of the MOSI line is '1' and that CPHA = 0 means that the devices must have data ready before the first transition of SCK. The figure does not include the MISO signal, the behavior of this line is the same as for the MOSI signal. However, due to synchronization the MISO signal will be delayed for a period of time that depends on the system clock frequency.

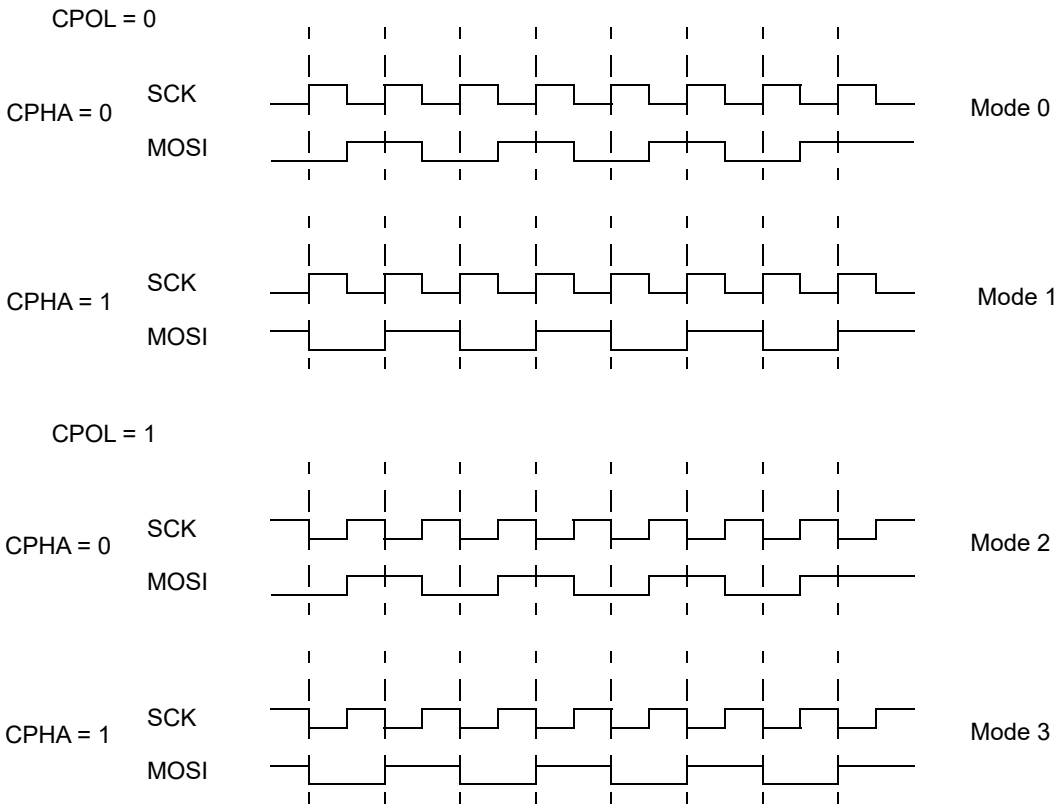


Figure 265. SPI transfer of byte 0x55 in all modes

The SPI to AHB bridge makes use of a protocol commonly used by SPI Flash memory devices. A master first selects the slave via the slave select signal and then issues a one-byte instruction. The instruction is then followed by additional bytes that contain address or data values. All instructions, addresses and data are transmitted with the most significant bit first. All AMBA accesses are done in big endian format. The first byte sent to or from the slave is the most significant byte.

99.3 System clock requirements and sampling

The core samples the incoming SPI SCK clock and does not introduce any additional clock domains into the system. Both the SCK and MOSI lines first pass through two stage synchronizers and are then filtered with a low pass filter.

The synchronizers and filters constrain the minimum system frequency. The core requires the SCK signal to be stable for at least two system clock cycles before the core accepts the SCK value as the new clock value. The core's reaction to transitions will be additionally delayed since both lines are taken through two-stage synchronizers before they are filtered. In order for the slave to be able to output data on the SCK 'change' transition and for this data to reach the master before the next edge the SCK frequency should not be higher than one tenth of the system frequency of core (with the standard VHDL generic *filter* setting of 2).

The slave select input should be asserted at least two system clock cycles before the SCK line starts transitioning.

99.4 SPI instructions

99.4.1 Overview

The core is controlled from the SPI bus by sending SPI instructions. Some commands require additional bytes in the form of address or data. The core makes use of the same instructions as commonly available SPI Flash devices. Table 1604 summarizes the available instructions.

*Table 1604.*SPI instructions

Instruction	Description	Instruction code	Additional bytes
RDSR	Read status/control register	0x05	Core responds with register value
WRSR	Write status/control register	0x01	New register value
READ	AHB read access	0x03	Four address bytes, after which core responds with data.
READD	AHB read access with dummy byte	0x0B	Four address bytes and one dummy byte, after which core responds with data
WRITE	AHB write access	0x02	Four address bytes followed by data to be written

All instructions, addresses and data are transmitted with the most significant bit first. All AMBA accesses are done in big endian format. The first byte sent to or from the slave is the most significant byte.

99.4.2 SPI status/control register accesses (RDSR/WRSR)

The RDSR and WRSR instructions access the core's SPI status/control register. The register is accessed by issuing the wanted instruction followed by the data byte to be written (WRSR) or any value on the byte in order to shift out the current value of the status/control register (RDSR). The fields available in the SPI status/control register are shown in table 1605.

*Table 1605.*SPI2AHB SPI status/control register

7	6	5	4	3	2	1	0
Reserved	RAHEAD	PROT	MEXC	DMAACT	MALF	HSIZE	

7 Reserved, always zero (read only)

6 Read ahead (RAHEAD) - When this bit is set the core will make a new access to fetch data as soon as the last current data bit has been moved. Otherwise the core will not attempt the new access until the 'change' transition on SCK. Setting this bit to '1' allows higher SCK frequencies to be used but will also result in a data fetch as soon as the current data has been read out. This means that RAHEAD may not be suitable when accessing FIFO interfaces. (read/write)

5 Memory protection triggered (PROT) - '1' if last AHB access was outside the allowed memory area. Updated after each AMBA access (read only). Note that since this bit is updated after each access the RAHEAD = '1' setting may hide errors.

4 Memory exception (MEXC) - '1' if core receives AMBA ERROR response. Updated after each AMBA access (read only). Note that since this bit is updated after each access the RAHEAD = '1' setting may hide errors.

3 DMA active (DMAACT) - '1' if core is currently performing a DMA operation.

2 Malfunction (MALF): This bit is set to one by the core is DMA is not finished when a new byte starts getting shifted. If this bit is set to '1' then the last AHB access was not successful.

1:0 AMBA access size (HSIZE) - Controls the access size that the core will use for AMBA accesses. 0: byte, 1: half-word, 2: word. HSIZE = "11" is illegal.

Reset value: 0x42

99.4.3 Read and write instructions (WRITE and READ/READD)

The READD is the same as the READ instruction with an additional dummy byte inserted after the four address bytes. To perform a read operation on AHB via the SPI bus the following sequence should be performed:

1. Assert slave select
2. Send READ instruction
3. Send four byte AMBA address, the most significant byte is transferred first

3a. Send dummy byte (if READD is used)

4. Read the wanted number of data bytes
5. De-assert slave select

To perform a write access on AHB via the SPI bus, use the following sequence:

1. Assert slave select
2. Send WRITE instruction
3. Send four byte AMBA address, the most significant byte is transferred first
4. Send the wanted number of data bytes
5. De-assert slave select

During consecutive read or write operations, the core will automatically increment the address. The access size (byte, halfword or word) used on AHB is set via the HSIZE field in the SPI status/control register.

The core always respects the access size specified via the HSIZE field. If a write operation writes fewer bytes than what is required to do an access of the specified HSIZE then the write data will be dropped, no access will be made on AHB. If a read operation reads fewer bytes than what is specified by HSIZE then the remaining read data will be dropped when slave select is de-asserted.

The core will not mask any address bits. Therefore it is important that the SPI master respects AMBA rules when performing half-word and word accesses. A half-word access must be aligned on a two byte address boundary (least significant bit of address must be zero) and a word access must be aligned on a four byte boundary (two least significant address bits must be zero).

The core can be configured to generate interrupt requests when an AHB access is performed if the core is implemented with the APB register interface, see the APB register documentation for details.

99.4.4 Memory protection

The core is configured at implementation time to only allow accesses to a specified AHB address range (which can be the full 4 GiB AMBA address range). If the core has been implemented with the optional APB register interface then the address range is soft configurable and the reset value is specified with VHDL generics.

The VHDL generics *ahbaddrh* and *ahbaddrl* define the base address for the allowed area. The VHDL generics *ahbmaskh* and *ahbmaskl* define the size of the area. The generics are used to assign the memory protection area's address and mask in the following way:

Protection address, bits 31:16 (*protaddr[31:16]*): ahbaddrh
Protection address, bits 15:0 (*protaddr[15:0]*): ahbaddrl
Protection mask, bits 31:16 (*protmask[31:16]*): ahbmaskh
Protection mask, bits 15:0 (*protmask[15:0]*): ahbmaskl

Before the core performs an AMBA access it will perform the check:

(((incoming address) xor (protaddr)) and protmask) /= 0x00000000

If the above expression is true (one or several bits in the incoming address differ from the protection address, and the corresponding mask bits are set to '1') then the access is inhibited. As an example, assume that *protaddr* is 0xA0000000 and *protmask* is 0xF0000000. Since *protmask* only has ones in the most significant nibble, the check above can only be triggered for these bits. The address range of allowed accessed will thus be 0xA0000000 - 0xAFFFFFFF..

The core will set the configuration register bit PROT if an access is attempted outside the allowed address range. This bit is updated on each AHB access and will be cleared by an access inside the allowed range. Note that the (optional) APB status register has a PROT field with a slightly different behavior.

99.5 Registers

The core can optionally be implemented with an APB interface that provides registers mapped into APB address space.

*Table 1606.*APB registers

APB address offset	Register
0x00	Control register
0x04	Status register
0x08	Protection address register
0x0C	Protection mask register

99.5.1 Control Register

*Table 1607.*0x00 - CTRL - Control register

31	2	1	0
RESERVED		IRQEN	EN
0		0	*
r		rw	rw

31 : 2 RESERVED

1 Interrupt enable (IRQEN) - When this bit is set to '1' the core will generate an interrupt each time the DMA field in the status register transitions from '0' to '1'.

0 Core enable (EN) - When this bit is set to '1' the core is enabled and will respond to SPI accesses. Otherwise the core will not react to SPI traffic.

99.5.2 Status Register

*Table 1608.*0x04 - STAT - Status register

31	3	2	1	0
RESERVED		PROT	WR	DMA
0		0	0	0
r		wc	r	wc

31 : 3 RESERVED

2 Protection triggered (PROT) - Set to '1' if an access has triggered the memory protection. This bit will remain set until cleared by writing '1' to this position. Note that the other fields in this register will be updated on each AHB access while the PROT bit will remain at '1' once set.

1 Write access (WR) - Last AHB access performed was a write access. This bit is read only.

0 Direct Memory Access (DMA) - This bit gets set to '1' each time the core attempts to perform an AHB access. By setting the IRQEN field in the control register this condition can generate an interrupt. This bit can be cleared by software by writing '1' to this position.

99.5.3 Protection Address Register

*Table 1609.*0x08 - PADDR - Protection address register

31	0
PROTADDR	
*	
rw	

31 : 0 Protection address (PROTADDR) - Defines the base address for the memory area where the core is allowed to make accesses.

99.5.4 Protection Mask Register

*Table 1610.*0x0C - PMASK - Protection mask register

31	0
PROTMASK	
*	
rw	

31 : 0 Protection mask (PROTMASK) - Selects which bits in the Protection address register that are used to define the protected memory area.

Reset value: Implementation dependent

99.6 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x05C. For a description of vendor and device identifiers see the GRLIB IP Library User's Manual.

99.7 Implementation

99.7.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

99.8 Configuration options

Table 1611 shows the configuration options of the core (VHDL generics). Two different top level entities for the core is available. One with the optional APB interface (spi2ahb_apb) and one without the APB interface (spi2ahb). The entity without the APB interface has fewer generics as indicated in the table below.

*Table 1611.*Configuration options

Generic name	Function	Allowed range	Default
hindex	AHB master index	0 - NAHBMST	0
ahbaddrh	Defines bits 31:16 of the address used for the memory protection area	0 - 16#FFFF#	0
ahbaddrl	Defines bits 15:0 of the address used for the memory protection area	0 - 16#FFFF#	0
ahbmaskh	Defines bits 31:16 of the mask used for the memory protection area	0 - 16#FFFF#	0
ahbmaskl	Defines bits 15:0 of the mask used for the memory protection area	0 - 16#FFFF#	0
resen	Reset value for core enable bit (only available on the spi2ahb_apb entity).	0 - 1	0
pindex	APB slave index (only available on the spi2ahb_apb entity).	0 - NAPBSLV-1	0
paddr	ADDR field of the APB BAR (only available on the spi2ahb_apb entity).	0 - 16#FFF#	0
pmask	MASK field of the APB BAR (only available on the spi2ahb_apb entity).	0 - 16#FFF#	16#FFF#
pirq	Interrupt line driven by APB interface (only available on the spi2ahb_apb entity).	0 - NAHBIRQ-1	0
oepol	Output enable polarity	0 - 1	0
filter	Low-pass filter length. This generic should specify, in number of system clock cycles plus one, the time of the shortest pulse on the SCK clock line to be registered as a valid value.	2 - 512	2
cpol	Clock polarity of SPI clock (SCK)	0 - 1	0
cpha	Clock phase of SPI communication	0 - 1	0

99.9 Signal descriptions

Table 1612 shows the interface signals of the core (VHDL ports).

*Table 1612.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
AHBI	*	Input	AHB master input signals	-
AHBO	*	Output	AHB master output signals	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
SPII	SCK	Input	SPI clock line input	-
	MOSI	Input	SPI data line input	-
	SPISEL	Input	SPI slave select input	
	Other fields	Input	Unused	
SPIO	MISO	Output	SPI data line output	-
	MISOOEN	Output	SPI data line output enable	Low**
	Other fields	Output	Unused	-

* see GRLIB IP Library User's Manual
** depends on value of OEPOL VHDL generic.

99.10 Signal definitions and reset values

The signals and their reset values are described in table 1613.

*Table 1613.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
sck	Input	SPI clock line	-	Hi-Z
miso	InputOutput	SPI master-input, slave-output line	-	Hi-Z
mosi	Input	SPI master-output, slave-input line	-	-
spisel	Input	SPI slave select	Low	-

99.11 Library dependencies

Table 1614 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1614.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	SPI	Component, signals	Component declaration, SPI signal definitions

99.12 Instantiation

The example below shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;
library grlib, techmap;
use grlib.amba.all;
use techmap.gencomp.all;
library gaisler;
```

```
use gaisler.misc.all;

entity spi2ahb_ex is
  port (
    clk  : in std_ulogic;
    rstn : in std_ulogic;

    -- SPI signals
    miso : inout std_logic;
    mosi : in    std_logic;
    sck  : in    std_logic;
    sel  : in    std_logic;
    );
end;

architecture rtl of spi2ahb_ex is
  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector;
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector;
  -- SPI signals
  signal spislvi : spi_in_type;
  signal spislvo : spi_out_type;
begin

  -- AMBA Components are instantiated here
  ...
  -- SPI to AHB bridge
  spibridge : if CFG_SPI2AHB /= 0 generate
    withapb : if CFG_SPI2AHB_APB /= 0 generate
      spi2ahb0 : spi2ahb_apb
        generic map(hindex => 10,
          ahbaddrh => CFG_SPI2AHB_ADDRH, ahbaddrl => CFG_SPI2AHB_ADDRL,
          ahbmaskh => CFG_SPI2AHB_MASKH, ahbmaskl => CFG_SPI2AHB_MASKL,
          resen => CFG_SPI2AHB_RESEN, pindex => 11, paddr => 11, pmask => 16#fff#,
          pirq => 11, filter => CFG_SPI2AHB_FILTER, cpol => CFG_SPI2AHB_CPOL,
          cpha => CFG_SPI2AHB_CPHA)
        port map (rstn, clkm, ahbmi, ahbmo(10),
                  apbi, apbo(11), spislvi, spislvo);
    end generate;
    woapb : if CFG_SPI2AHB_APB = 0 generate
      spi2ahb0 : spi2ahb
        generic map(hindex => 10,
          ahbaddrh => CFG_SPI2AHB_ADDRH, ahbaddrl => CFG_SPI2AHB_ADDRL,
          ahbmaskh => CFG_SPI2AHB_MASKH, ahbmaskl => CFG_SPI2AHB_MASKL,
          filter => CFG_SPI2AHB_FILTER,
          cpol => CFG_SPI2AHB_CPOL, cpha => CFG_SPI2AHB_CPHA)
        port map (rstn, clkm, ahbmi, ahbmo(10),
                  spislvi, spislvo);
    end generate;
    spislv_miso_pad : iopad generic map (tech => padtech)
      port map (miso, spislvo.miso, spislvo.misooen, spislvi.miso);
    spislvl_mosi_pad : inpad generic map (tech => padtech)
      port map (miso, spislvi.mosi);
    spislv_sck_pad  : inpad generic map (tech => padtech)
      port map (sck, spislvi.sck);
    spislv_slvsel_pad : iopad generic map (tech => padtech)
      port map (sel, spislvi.spisel);
  end generate;
  nospibridge : if CFG_SPI2AHB = 0 or CFG_SPI2AHB_APB = 0 generate
    apbo(11) <= apb_none;
  end generate;
end;
```

100 SPICTRL - SPI Controller

100.1 Overview

The core provides a link between the AMBA APB bus and the Serial Peripheral Interface (SPI) bus and can be dynamically configured to function either as a SPI master or a slave. The SPI bus parameters are highly configurable via registers. Core features also include configurable word length, bit ordering, clock gap insertion, automatic slave select and automatic periodic transfers of a specified length. All SPI modes are supported and optionally also dual SPI, quad SPI, and a 3-wire protocol where one bidirectional data line is used. In slave mode the core synchronizes the incoming clock and can operate in systems where other SPI devices are driven by asynchronous clocks.

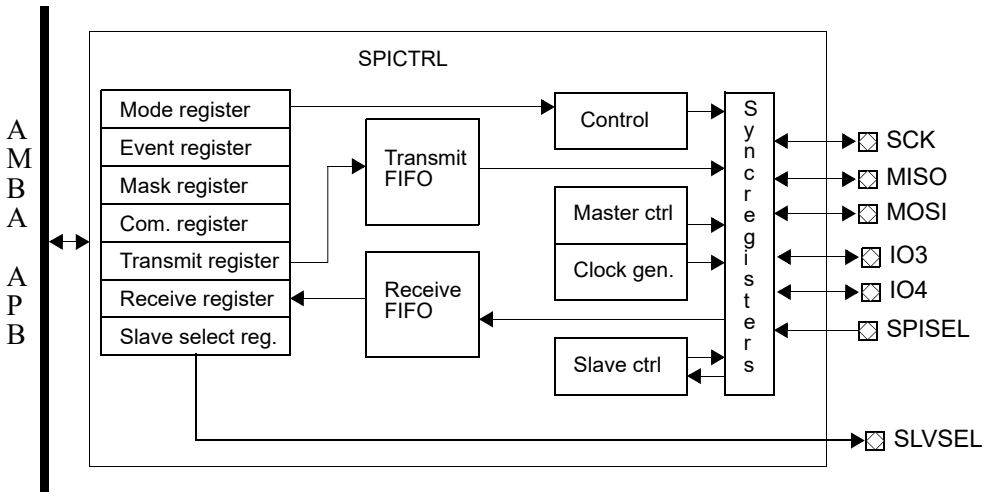


Figure 266. Block diagram

100.2 Operation

100.2.1 SPI transmission protocol

The SPI bus is a full-duplex synchronous serial bus. Transmission starts when a master selects a slave through the slave's Slave Select (SLVSEL) signal and the clock line SCK transitions from its idle state. Data is transferred from the master through the Master-Output-Slave-Input (MOSI) signal and from the slave through the Master-Input-Slave-Output (MISO) signal. In a system with only one master and one slave, the Slave Select input of the slave may be always active and the master does not need to have a slave select output. If the core is configured as a master it will monitor the SPISEL signal to detect collisions with other masters, if SPISEL is activated the master will be disabled.

During a transmission on the SPI bus data is either changed or read at a transition of SCK. If data has been read at edge n, data is changed at edge n+1. If data is read at the first transition of SCK the bus is said to have clock phase 0, and if data is changed at the first transition of SCK the bus has clock phase 1. The idle state of SCK may be either high or low. If the idle state of SCK is low, the bus has clock polarity 0 and if the idle state is high the clock polarity is 1. The combined values of clock polarity (CPOL) and clock phase (CPHA) determine the mode of the SPI bus. Figure 267 shows one byte (0x55) being transferred MSb first over the SPI bus under the four different modes. Note that the idle state of the MOSI line is '1' and that CPHA = 0 means that the devices must have data ready before the first transition of SCK. The figure does not include the MISO signal, the behavior of this line is the same as for the MOSI signal. However, due to synchronization issues the MISO signal will be delayed when the core is operating in slave mode, please see section 100.2.6 for details.

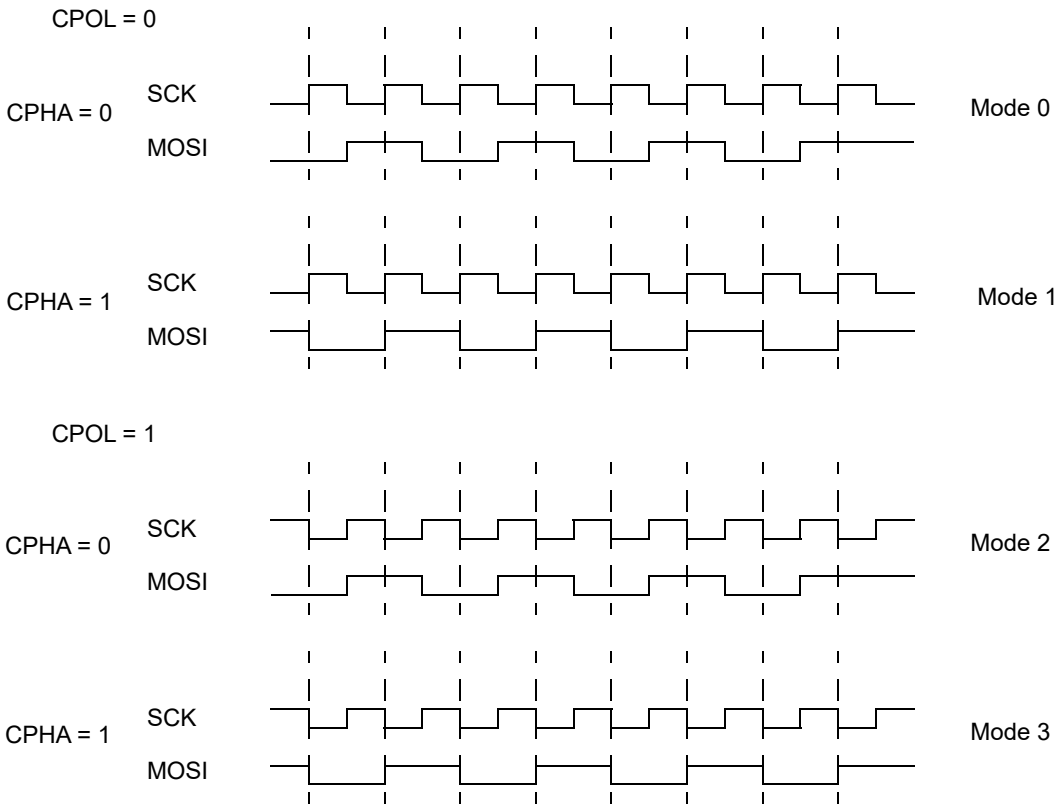


Figure 267. SPI transfer of byte 0x55 in all modes

100.2.2 3-wire transmission protocol

The core can be configured to use a 3-wire protocol if the TWEN field in the core's Capability register 0 is set to '1', where the controller uses a bidirectional dataline instead of separate data lines for input and output data. In 3-wire protocol the bus is thus a half-duplex synchronous serial bus. Transmission starts when a master selects a slave through the slave's Slave Select (SLVSEL) signal and the clock line SCK transitions from its idle state. Only the Master-Output-Slave-Input (MOSI) signal is used for data transfer in the 3-wire protocol. The MISO signal is not used.

The direction of the first data transfer is determined by the value of the 3-wire Transfer Order (TTO) field in the core's Mode register. If TTO is '0', data is first transferred from the master (through the MOSI signal). After a word has been transferred, the slave uses the same data line to transfer a word back to the master. If TTO is '1' data is first transferred from the slave to the master. After a word has been transferred, the master uses the MOSI line to transfer a word back to the slave.

The data line transitions depending on the clock polarity and clock phase in the same manner as in SPI mode. The aforementioned slave delay of the MISO signal in SPI mode will affect the MOSI signal when using 3-wire protocol, when the core operates as a slave.

100.2.3 Dual and quad transmission protocols

The core can be configured to use dual and quad SPI protocols if support for these protocols is indicated in the PROT field of the core's Capability register 1. The SPROT field of the core's Command register determines the protocol to use.

In standard SPI mode, a master always transmits on the MOSI line and receives on the MISO line and vice-versa for a slave. With dual SPI protocol the slave or master may use both of MISO and MOSI for reception or transmission. In quad SPI mode the slave or master will use MISO, MOSI, IO2 and IO3 for either transmission or reception. Since this all traffic in this controller is driven via the trans-

mit queue it becomes necessary to mark the words to be transmitted so that the controller knows which direction that should be used for the MISO, MOSI, IO2 and IO3 lines in the corresponding transfer. The direction associated with the transfer is determined by the setting of the DIR field in the core's Command register.

100.2.4 Receive and transmit queues

The core's transmit queue consists of the transmit register and the transmit FIFO. The receive queue consists of the receive register and the receive FIFO. The total number of words that can exist in each queue is thus the FIFO depth plus one. When the core has one or more free slots in the transmit queue it will assert the Not full (NF) bit in the event register. Software may only write to the transmit register when this bit is asserted. When the core has received a word, as defined by word length (LEN) in the Mode register, it will place the data in the receive queue. When the receive queue has one or more elements stored the Event register bit Not empty (NE) will be asserted. The receive register will only contain valid data if the Not empty bit is asserted and software should not access the receive register unless this bit is set. If the receive queue is full and the core receives a new word, an overrun condition will occur. The received data will be discarded and the Overrun (OV) bit in the Event register will be set.

The core will also detect underrun conditions. An underrun condition occurs when the core is selected, via SPISEL, and the SCK clock transitions while the transmit queue is empty. In this scenario the core will respond with all bits set to '1' and set the Underrun (UN) bit in the Event register. An underrun condition will never occur in master mode. When the master has an empty transmit queue the bus will go into an idle state.

100.2.5 Clock generation

The core only generates the clock in master mode, the generated frequency depends on the system clock frequency and the Mode register fields DIV16, FACT, and PM. Without DIV16 the SCK frequency is:

$$SCKFrequency = \frac{AMBAclockfrequency}{(4-(2 \cdot FACT)) \cdot (PM+1)}$$

With DIV16 enabled the frequency of SCK is derived through:

$$SCKFrequency = \frac{AMBAclockfrequency}{16 \cdot (4-(2 \cdot FACT)) \cdot (PM+1)}$$

Note that the fields of the Mode register, which includes DIV16, FACT and PM, should not be changed when the core is enabled. If the FACT field is set to 0 the core's register interface is compatible with the register interface found in MPC83xx SoCs. If the FACT field is set to 1, the core can generate an SCK clock with higher frequency.

100.2.6 Slave operation

When the core is configured for slave operation it does not drive any SPI signal until the core is selected, via the SPISEL input, by a master. If the core operates in SPI mode when SPISEL goes low the core configures MISO as an output and drives the value of the first bit scheduled for transfer. If the core is configured to use 3-wire protocol then the core will first listen to the MOSI line and when a word has been transferred drive the response on the MOSI line. If the core is selected when the transmit queue is empty it will transfer a word with all bits set to '1' and the core will report an underflow.

Since the core synchronizes the incoming clock it will not react to transitions on SCK until two system clock cycles have passed. This leads to a delay of three system clock cycles when the data output line should change as the result of a SCK transition. This constrains the maximum input SCK frequency of the slave to (system clock) / 8 or less. The controlling master must also allow the decreased setup time on the slave data out line.

The core can also filter the SCK input. The value of the PM field in the Mode register defines for how many system clock cycles the SCK input must be stable before the core accepts the new value. If the PM field is set to zero, then the maximum SCK frequency of the slave is, as stated above, (system clock) / 8 or less. For each increment of the PM field the clock period of SCK must be prolonged by two times the system clock period as the core will require longer time discover and respond to SCK transitions.

100.2.7 Master operation

When the core is configured for master operation it will transmit a word when there is data available in the transmit queue. When the transmit queue is empty the core will drive SCK to its idle state. If the SPISEL input goes low during master operation the core will abort any active transmission and the Multiple-master error (MME) bit will be asserted in the Event register. If a Multiple-master error occurs the core will be disabled. Note that the core will react to changes on SPISEL even if the core is operating in loop mode and that the core can be configured to ignore SPISEL by setting the IGSEL field in the Mode register.

100.2.8 Automated periodic transfers

The core supports automated periodic transfers if the AMODE field in the core's Capability register is '1'. In this mode the core will perform transfers with a specified period and length. The steps below outline how to set up automated transfers:

1. Configure the core's Mode register as a master and set the AMEN field (bit 31) to '1'. Possibly also configure the automatic slave select settings.
2. Write to the AM Mask registers to configure which parts of the AM transmit queue that will be used. The number of bits in the AM Mask registers that are set to one together with the word length (set in the Mode register) defines how long the transfer should be.
3. Write data to the AM transmit queue (AM Transmit registers). Only those registers that correspond to a bit that is set to one in the AM Mask registers need to be written.
4. Set the transfer period in the AM Period register.
5. Set the options for the automated transfers in the AM Configuration register
6. Set the ACT or EACT field in the AM Configuration register.
7. Wait for the Not Empty field to be set in the Event register
8. Read out the AM Receive queue (AM Receive registers). If lock bit (LOCK) in AM Configuration register is set then all registers which have a bit in the AM Mask registers set must be read. If the lock bit is not set software does not need to read out any data, the core can write new data to the AM Receive registers anyway.
9. Go back to step 7.

When an automated transfer is performed, data is not immediately placed in AM receive queue. Instead the data is placed in a temporary queue to ensure that a full transfer can be read out atomically without interference from incoming data.

The AM receive queue is filled with the data from the temporary queue if the AM receive queue is empty, or if it is full and Sequential transfers (SEQ) is disabled in the AM Configuration register. It is possible to configure the core not to place new data in the AM receive queue while software is reading

out data from the queue. This is done by setting the lock bit (LOCK) in the AM Configuration register.

If the AM Configuration register's SEQ bit is set the core will not move data from the temporary queue until the AM receive queue has been cleared. Demanding Sequential transfers means that the AM receive queue's data will never be overwritten. However, data may still be lost, depending on the settings that determine how the temporary queue handles overflow conditions.

The controller will attempt to place data into the temporary receive queue when the automated transfer period counter reaches zero. If the temporary queue is filled, which can occur if the controller is prevented from moving the data to the receive queue, the core's behavior will depend on the setting of the Strict Period (STRICT) field in the AM Configuration register:

If the value of STRICT is '0' the core will delay the transfer and wait until the temporary queue has been cleared.

If the value of STRICT is '1', and the contents of the temporary queue can not be moved to the AM receive queue, there will be an overflow condition in the temporary queue. The core's behavior on a temporary queue overflow is defined by the AM Configuration register fields Overflow Transfer Behavior (OVTB) and Overflow Data Behavior (OVDB). If there is a temporary queue overflow and OVTB is set, the transfer will be skipped and the core's internal period counter will be reloaded. If the OVTB bit is not set the transfer will be performed. If the transfer is performed and the OVDB bit is set the data will be disregarded. If the OVDB bit is not set the data will be placed in the temporary receive queue and the previous data will be overwritten.

A series of automated transfers can be started by an external event. If the AM Configuration register field EACT is set, the core will activate Automated transfers when its internal ASTART input signal goes high. When the core detects that EACT and ASTART are both set, it will set the AM Configuration register ACT bit and reset the EACT bit. Note that subsequent automated transfers will be started when the period counter reaches zero, if ERPT field of the AM Configuration register is set to zero. If the ERPT field is set to one then the ASTART input is used to start subsequent transfers instead.

When automated transfers are enabled by setting the AM Configuration register ACT bit, the core will send a pulse on its internal ASTART output signal. This means that several cores can be connected together and have their start event synchronized. To synchronize a start event, set the EACT bit in all cores, except in the last core which is activated by setting the AM Configuration register ACT field. The last core will then pulse its ASTART output and trigger the start event in all the other connected cores. When this has been done the cores' transfers will be synchronized. However this synchronization may be lost if a core's receive queues are filled and STRICT transfers are disabled, since this will lead to a delay in the start of the core's next transfer.

When the core operates in AM mode, the Receive and Transmit registers should not be accessed. Nor should the AM transmit registers be updated when automatic transfers are enabled.

100.3 Registers

The core is programmed through registers mapped into APB address space.

*Table 1615.*SPI controller registers

APB address offset	Register
0x00	Capability register 0
0x04	Capability register 1
0x08-0x1C	Reserved
0x20	Mode register
0x24	Event register
0x28	Mask register
0x2C	Command register
0x30	Transmit register
0x34	Receive register
0x38	Slave Select register (optional)
0x3C	Automatic slave select register*
0x40	AM Configuration register**
0x44	AM Period register**
0x48-0x4C	Reserved
0x50-0x5C	AM Mask register(s)***
0x200-0x3FC	AM Transmit register(s)****
0x400-0x5FC	AM Receive register(s)****

*Only available if ASEL (bit 17) in the SPI controller Capability register is set.
**Only available if AMODE (bit 18) in the SPI controller Capability register is set.

***Only available if AMODE (bit 18) in the SPI controller Capability register is set. Number of implemented registers depend on FDEPTH (bits 15:8) in the SPI controller Capability register in the following way: Number of registers = (FDEPTH-1)/32 + 1.

****Only available if AMODE (bit 18) in the SPI controller Capability register is set. Number of implemented registers equals FDEPTH (bits 15:8) in the SPI controller Capability register.

100.3.1 SPI Controller Capability Register 0

*Table 1616.*0x00 - CAP0 - SPI controller Capability register 0

31	24	23	20	19	18	17	16
SSSZ		MAXWLEN		TWEN	AMODE	ASELA	SSEN
*		*		*	*	*	‘
r		r		r	r	r	r

15	8	7	6	5	4	0
FDEPTH		SR	FT		REV	
*		*	*		5	
r		r	r		r	

31 : 24 Slave Select register size (SSSZ) - If the core has been configured with slave select signals this field contains the number of available signals. This field is only valid is the SSEN bit (bit 16) is ‘1

23 : 20 Maximum word Length (MAXWLEN) - The maximum word length supported by the core:
0b0000 - 4-16, and 32-bit word length
0b0011-0b1111 - Word length is MAXWLEN+1, allows words of length 4-16 bits.
The core must not be configured to use a word length greater than what is defined by this register.

19 3-wire Protocol Enable (TWEN) - If this bit is ‘1’ the core supports 3-wire protocol. See also the PROT field in Capability register 1.

18 Auto mode (AMODE) - If this bit is ‘1’ the core supports Automated transfers.

17 Automatic slave select available (ASELA) - If this bit is set, the core has support for setting slave select signals automatically.

16 Slave Select Enable (SSEN) - If the core has a slave select register, and corresponding slave select lines, the value of this field is one. Otherwise the value of this field is zero.

15 : 8 FIFO depth (FDEPTH) - This field contains the depth of the core’s internal FIFOs. The number of words the core can store in each queue is FDEPTH+1, since the transmit and receive registers can contain one word each.

7 SYNCRAM (SR) - If this field is ‘1’ the core has buffers implemented with SYNCRAM components.

6 : 5 Fault-tolerance (FT) - This field signals if the core has any fault-tolerant capabilities. “00” - No fault-tolerance. “01” - Parity DMR, “10” - TMR.

4 : 0 Core revision (REV) - This manual applies to core revision 5.

100.3.2 SPI Controller Capability Register 1

*Table 1617.*0x04 - CAP1 - SPI controller Capability register 1

31	2	1	0
R		PROT	
0		*	
r		r	

31 : 2 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

1 : 0 Protocols (PROT) - This field shows which SPI protocols that the core supports. Note that support for the 3-wire protocol is shown using a separate bit in Capability register 0. The values for the PROT field are decoded in the following way:
0 - Support for standard SPI protocol
1 - Support for standard and dual SPI protocols
2 - Support for standard, dual and quad SPI protocols

100.3.3 SPI Controller Mode Register

*Table 1618.*0x20 - MODE - SPI controller Mode register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AMEN	LOOP	CPOL	CPHA	DIV16	REV	MS	EN	LEN				PM			
0	0	0	0	0	0	0	0	0				0			
rw*	rw	rw	rw	rw	rw	rw	rw	rw				rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TWEN	ASEL	FACT	OD	CG					ASELDEL		TAC	TTO	IGSEL	CITE	R
0	0	0	0	0					0		0	0	0	*	0
rw*	rw*	rw	rw*	rw					rw*		rw	rw	rw	rw	r

31 Auto mode enable (AMEN) - When this bit is set to '1' the core will be able to perform automated periodic transfers. See the AM registers below. The core supports this mode if the AMODE field in the capability register is set to '1'. Otherwise writes to this field has no effect. When this bit is set to '1' the core can only perform automated transfers. Software is allowed to initialize the transmit queue and to read out the receive queue but no transfers except the automated periodic transfers may be performed. The core must be configured to act as a master (MS field set to '1') when performing automated transfers.

30 Loop mode (LOOP) - When this bit is set, and the core is enabled, the core's transmitter and receiver are interconnected and the core will operate in loopback mode. The core will still detect, and will be disabled, on Multiple-master errors.

29 Clock polarity (CPOL) - Determines the polarity (idle state) of the SCK clock.

28 Clock phase (CPHA) - When CPHA is '0' data will be read on the first transition of SCK. When CPHA is '1' data will be read on the second transition of SCK.

27 Divide by 16 (DIV16) - Divide system clock by 16, see description of PM field below and see section 100.2.5 on clock generation. This bit has no significance in slave mode.

26 Reverse data (REV) - When this bit is '0' data is transmitted LSB first, when this bit is '1' data is transmitted MSB first. This bit affects the layout of the transmit and receive registers.

25 Master/Slave (MS) - When this bit is set to '1' the core will act as a master, when this bit is set to '0' the core will operate in slave mode.

24 Enable core (EN) - When this bit is set to '1' the core is enabled. No fields in the mode register should be changed while the core is enabled. This can bit can be set to '0' by software, or by the core if a multiple-master error occurs.

23 : 20 Word length (LEN) - The value of this field determines the length in bits of a transfer on the SPI bus. Values are interpreted as:

0b0000 - 32-bit word length

0b0001-0b0010 - Illegal values

0b0011-0b1111 - Word length is LEN+1, allows words of length 4-16 bits.

The value of this field must never specify a word length that is greater than the maximum allowed word length specified by the MAXWLEN field in the Capability register.

19 : 16 Prescale modulus (PM) - This value is used in master mode to divide the system clock and generate the SPI SCK clock. The value in this field depends on the value of the FACT bit.

If bit 13 (FACT) is '0':The system clock is divided by 4*(PM+1) if the DIV16 field is '0' and 16*4*(PM+1) if the DIV16 field is set to '1'. The highest SCK frequency is attained when PM is set to 0b0000 and DIV16 to '0', this configuration will give a SCK frequency that is (system clock)/4. With this setting the core is compatible with the SPI register interface found in MPC83xx SoCs.

If bit 13 (FACT) is '1': The system clock is divided by 2*(PM+1) if the DIV16 field is '0' and 16*2*(PM+1) if the DIV16 field is set to '1'. The highest SCK frequency is attained when PM is set to 0b0000 and DIV16 to '0', this configuration will give a SCK frequency that is (system clock)/2.

In slave mode the value of this field defines the number of system clock cycles that the SCK input must be stable for the core to accept the state of the signal. See section 100.2.6.

15 3-wire protocol (TW) - If this bit is set to '1' the core will operate using 3-wire protocol. This bit can only be set if the TWEN field of the Capability register is set to '1'.

*Table 1618.*0x20 - MODE - SPI controller Mode register

14	Automatic slave select (ASEL) - If this bit is set to '1' the core will swap the contents in the Slave select register with the contents of the Automatic slave select register when a transfer is started and the core is in master mode. When the transmit queue is empty, the slave select register will be swapped back. Note that if the core is disabled (by writing to the core enable bit or due to a multiple-master-error (MME)) when a transfer is in progress, the registers may still be swapped when the core goes idle. This bit can only be set if the ASELA field of the Capability register is set to '1'. Also see the ASELDEL field which can be set to insert a delay between the slave select register swap and the start of a transfer.
13	PM factor (FACT) - If this bit is 1 the core's register interface is no longer compatible with the MPC83xx register interface. The value of this bit affects how the PM field is utilized to scale the SPI clock. See the description of the PM field.
12	Open drain mode (OD) - If this bit is set to '0', all pins are configured for operation in normal mode. If this bit is set to '1' all pins are set to open drain mode. The implementation of the core may or may not support open drain mode. If this bit can be set to '1' by writing to this location, the core supports open drain mode. The pins driven from the slave select register are not affected by the value of this bit.
11 : 7	Clock gap (CG) - The value of this field is only significant in master mode. The core will insert CG SCK clock cycles between each consecutive word. This only applies when the transmit queue is kept non-empty. After the last word of the transmit queue has been sent the core will go into an idle state and will continue to transmit data as soon as a new word is written to the transmit register, regardless of the value in CG. A value of 0b00000 in this field enables back-to-back transfers.
6 : 5	Automatic Slave Select Delay (ASELDEL) - If the core is configured to use automatic slave select (ASEL field set to '1') the core will insert a delay corresponding to ASELDEL*(SPI SCK cycle time)/2 between the swap of the slave select registers and the first toggle of the SCK clock. As an example, if this field is set to "10" the core will insert a delay corresponding to one SCK cycle between assigning the Automatic slave select register to the Slave select register and toggling SCK for the first time in the transfer. This field can only be set if the ASELA field of the Capability register is set to '1'.
4	Toggle Automatic slave select during Clock Gap (TAC) - If this bit is set, and the ASEL field is set, the core will perform the swap of the slave select registers at the start and end of each clock gap. The clock gap is defined by the CG field and must be set to a value >= 2 if this field is set. This field can only be set if the ASELA field of the Capability register is set to '1'.
3	3-wire Transfer Order (TTO) - This bit controls if the master or slave transmits a word first in 3-wire protocol. If this bit is '0', data is first transferred from the master to the slave. If this bit is '1', data is first transferred from the slave to the master. This bit can only be set if the TWEN field of the Capability register is set to '1'.
2	Ignore SPISEL input (IGSEL) - If this bit is set to '1' then the core will ignore the value of the SPISEL input.
1	Require Clock Idle for Transfer End (CITE) - If this bit is '0' the core will regard the transfer of a word as completed when the last bit has been sampled. If this bit is set to '1' the core will wait until it has set the SCK clock to its idle level (see CI field) before regarding a transfer as completed. This setting only affects the behavior of the TIP status bit, and automatic slave select toggling at the end of a transfer, when the clock phase (CP field) is '0'.
0	RESERVED (R) - Read as zero and should be written as zero to ensure forward compatibility.

100.3.4 SPI Controller Event Register

*Table 1619.*0x24 - EVENT - SPI controller Event register

31	30 16	15	14	13	12	11	10	9	8	7 0
TIP	R	AT	LT	R	OV	UN	MME	NE	NF	R
0	0	0	0	0	0	0	0	0	0	0
r	r	r	wc	r	wc	wc	wc	r	r	r

31 Transfer in progress (TIP) - This bit is ‘1’ when the core has a transfer in progress. Writes have no effect. This bit is set when the core starts a transfer and is reset to ‘0’ once the core considers the transfer to be finished. Behavior affected by setting of CITE field in Mode register.

30 : 16 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

15 Automated transfers (AT) - This bit is ‘1’ when the core has an automated transfer in progress. This bit is cleared automatically by the core. Writes have no effect.

14 Last character (LT) - This bit is set when a transfer completes if the transmit queue is empty and the LST bit in the Command register has been written. This bit is cleared by writing ‘1’, writes of ‘0’ have no effect.

13 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

12 Overrun (OV) - This bit gets set when the receive queue is full and the core receives new data. The core continues communicating over the SPI bus but discards the new data. This bit is cleared by writing ‘1’, writes of ‘0’ have no effect.

11 Underrun (UN) - This bit is only set when the core is operating in slave mode. The bit is set if the core’s transmit queue is empty when a master initiates a transfer. When this happens the core will respond with a word where all bits are set to ‘1’. This bit is cleared by writing ‘1’, writes of ‘0’ have no effect.

10 Multiple-master error (MME) - This bit is set when the core is operating in master mode and the SPISEL input goes active. In addition to setting this bit the core will be disabled. This bit is cleared by writing ‘1’, writes of ‘0’ have no effect.

9 Not empty (NE) - This bit is set when the receive queue contains one or more elements. It is cleared automatically by the core, writes have no effect.

8 Not full (NF) - This bit is set when the transmit queue has room for one or more words. It is cleared automatically by the core when the queue is full, writes have no effect. This bit is only updated when the core is enabled (EN field of Mode register is set to ‘1’).

7 : 0 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

100.3.5 SPI Controller Mask Register

*Table 1620.*0x28 - MASK - SPI controller Mask register

31	30 16	15	14	13	12	11	10	9	8	7 0
TIPE	R	AT	LTE	R	OVE	UNE	MMEE	NEE	NFE	R
0	0	0	0	0	0	0	0	0	0	0
rw	r	rw	rw	rw	rw	rw	rw	rw	rw	r

31 Transfer in progress enable (TIPE) - When this bit is set the core will generate an interrupt when the TIP bit in the Event register transitions from ‘0’ to ‘1’.

30 : 16 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

15 Automated transfers (AT) - When this bit is set, the core will generate an interrupt when an automated transfer is completed.

14 Last character enable (LTE) - When this bit is set the core will generate an interrupt when the LT bit in the Event register transitions from ‘0’ to ‘1’.

13 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

12 Overrun enable (OVE) - When this bit is set the core will generate an interrupt when the OV bit in the Event register transitions from ‘0’ to ‘1’.

11 Underrun enable (UNE) - When this bit is set the core will generate an interrupt when the UN bit in the Event register transitions from ‘0’ to ‘1’.

10 Multiple-master error enable (MMEE) - When this bit is set the core will generate an interrupt when the MME bit in the Event register transitions from ‘0’ to ‘1’.

9 Not empty enable (NEE) - When this bit is set the core will generate an interrupt when the NE bit in the Event register transitions from ‘0’ to ‘1’.

8 Not full enable (NFE) - When this bit is set the core will generate an interrupt when the NF bit in the Event register transitions from ‘0’ to ‘1’.

7 : 0 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

100.3.6 SPI Controller Command Register

*Table 1621.*0x2C - CMD - SPI controller Command register

31 23	22	21 4	3	2	1 0
R	LST	R	PGRD	DIR	SPROT
0	0	0	0	0	0
r	w*	r	w*	rw*	rw*

31 : 23 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

22 Last (LST) - After this bit has been written to '1' the core will set the Event register bit LT when a character has been transmitted and the transmit queue is empty. If the core uses the 3-wire protocol then the Event register bit is set when the whole transfer has completed. This bit is automatically cleared when the Event register bit has been set and is always read as zero.

As of revision 6 of this SPI controller the LST bit can only be set to '1'. Previous revisions of the core allowed the LST bit to be set to '0' by writing to this bit. As of revision 6, writes of zero do not affect the core's internal state of the LST bit.

21 : 4 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

3 Protocol guard (PGRD) - This field must be set to '1' to modify the IO and SPROT fields. If the value of this field is 0 for a write operation then no change will be made to IO and SPROT.

2 Direction (DIR) - This field determines the direction for transfers when the SPROT field is non-zero.
0 - Output
1 - Input
This field can only be modified when the PGRD field is set in the write data.

1 : 0 SPI protocol (SPROT) - This field selects between standard, dual and quad SPI mode. The settings are:

0b00 - Standard SPI mode
0bx1 - Dual SPI mode
0b10 - Quad SPI mode

Dual and quad SPI modes can only be enabled if they are supported by the implementation as indicated by the PROT field in Capability register 1. This field must not be changed while the core is transmitting or receiving data. The same protocol is also used for the words received while transmitting.

This field must be set to 0 when using 3-wire protocol (controlled via Mode register).

This field can only be modified when the PGRD field is set in the write data.

100.3.7 SPI Controller Transmit Register

*Table 1622.*0x30 - TX - SPI controller Transmit register

31 0
TDATA
0
w

31 : 0 Transmit data (TDATA) - Writing a word into this register places the word in the transmit queue. This register will only react to writes if the Not full (NF) bit in the Event register is set. The layout of this register depends on the value of the REV field in the Mode register:

Rev = '0': The word to transmit should be written with its least significant bit at bit 0.

Rev = '1': The word to transmit should be written with its most significant bit at bit 31.

100.3.8 SPI Controller Receive Register

*Table 1623.*0x34 - RXC - SPI controller Receive register

31	0
RDATA	
0	
r	

31 : 0 Receive data (RDATA) - This register contains valid receive data when the Not empty (NE) bit of the Event register is set. The placement of the received word depends on the Mode register fields LEN and REV:

For LEN = 0b0000 - The data is placed with its MSb in bit 31 and its LSb in bit 0.

For other lengths and REV = '0' - The data is placed with its MSB in bit 15.

For other lengths and REV = '1' - The data is placed with its LSB in bit 16.

To illustrate this, a transfer of a word with eight bits (LEN = 7) that are all set to one will have the following placement:

REV = '0' - 0x0000FF00

REV = '1' - 0x00FF0000

100.3.9 SPI Slave Select Register (optional)

*Table 1624.*0x38 - SLVSEL - SPI Slave select register (optional)

31 SSSZ	SSSZ-1 0
R	SLVSEL
0	all 1
r	rw

31 : SSSZ RESERVED (R) - The lower bound of this register is determined by the Capability register field SSSZ if the SSEN field is set to 1. If SSEN is zero bits 31:0 are reserved.

(SSSZ-1) : 0 Slave select (SLVSEL) - If SSEN in the Capability register is 1 the core's slave select signals are mapped to this register on bits (SSSZ-1):0. Software is solely responsible for activating the correct slave select signals, the core does not assert or deassert any slave select signal automatically.

100.3.10SPI Controller Automatic Slave Select Register

*Table 1625.*0x3C - ASLVSEL - SPI controller Automatic slave select register

31 SSSZ	SSSZ-1 0
R	ASLVSEL
0	0
r	rw

31 : SSSZ RESERVED (R) - The lower bound of this register is determined by the Capability register field SSSZ if the SSEN field is set to 1. If SSEN is zero bits 31:0 are reserved.

(SSSZ-1) : 0 Automatic Slave select (ASLVSEL) - If SSEN and ASELA in the Capability register are both '1' the core's slave select signals are assigned from this register when the core is about to perform a transfer and the ASEL field in the Mode register is set to '1'. After a transfer has been completed the core's slave select signals are assigned the original value in the slave select register.

Note: This register is only available if ASELA (bit 17) in the SPI controller Capability register is set

100.3.11SPI Controller AM Configuration Register

*Table 1626.*0x40 - AMCFG - SPI controller AM configuration register

31	30								16
RESERVED									
0									
r									

15	9	8	7	6	5	4	3	2	1	0
RESERVED		ECGC	LOCK	ERPT	SEQ	STRICT	OVTB	OVDB	ACT	EACT
0		0	0	0	0	0	0	0	0	0
r		rw	rw	rw	rw	rw	rw	rw	rw	rw

31 : 9 RESERVED - This field is reserved for future use and should always be written as zero.

8 External clock gap control (ECGC) - If software sets this bit to ‘1’ then the clock gap between individual transfers in a set of automated transfers is controller by the core’s CSTART input instead of the CG field in the Mode registers. Note that the requirement that the CG field must be set to a value >= 2 if the TAC bit is set still applies even if this bit is set. Reset value ‘0’.

7 Lock bit (LOCK) - If software sets this bit to ‘1’ then the core will not place new data in the AM Receive registers while software is reading out new data.

6 External repeat (ERPT) - When this bit is set the core will use the input signal astart to start a new periodic transfer. If this bit is cleared, the period counter will be used instead.

5 Sequential transfers (SEQ) - When this bit is set the core will not update the receive queue unless the queue has been emptied by reading out its contents. Note that the contents in the temporary FIFO may still be overwritten with incoming data, depending on the setting of the other fields in this register.

4 Strict period (STRICT) - When this bit is set the core will always try to perform a transfer when the period counter reaches zero, if this bit is not set the core will wait until the receive FIFO is empty before it tries to perform a new transfer.

3 Overflow Transfer Behavior (OVTB) - If this bit is set to ‘1’ the core will skip transfers that would result in data being overwritten in the temporary receive queue. Note that this bit only decides if the transfer is performed. If this bit is set to ‘0’ a transfer will be performed and the setting of the Overflow Data Behavior bit (OVDB) will decide if data is actually overwritten.

2 Overflow Data Behavior (OVDB) - If this bit is set to ‘1’ the core will skip incoming data that would overwrite data in the receive queues. If this bit is ‘0’ the core will overwrite data in the temporary queue.

1 Activate automated transfers (ACT) - When this bit is set to ‘1’ the core will start to decrement the AM period register and perform automated transfers. The system clock cycle after this bit has been written to ‘1’ there will be a pulse on the core’s ASTART output.

Automated transfers can be deactivated by writing this bit to ‘0’. The core will wait until any ongoing transfer has finished before deactivating automated transfers. Software should not perform any operation on the core before this bit has been read back as ‘0’. The data in the last transfer(s) will be lost if there is a transfer in progress when this bit is written to ‘0’. All words present in the transmit queue will also be dropped.

0 External activation of automated transfers (EACT) - When this bit is set to ‘1’ the core will activate automated transfers when the core’s ASTART input goes HIGH. When the core has been activated by the external signal this bit will be reset and the ACT field (bit 1 will be set).

Note: This register is only available if AMODE (bit 18) in the SPI controller Capability register is set

100.3.12SPI Controller AM Period Register

*Table 1627.*0x44 - AMPER - SPI controller AM period register

31	0
AMPER	
0	
rw	

31 : 0 AM Period (AMPER) - This field contains the period, in system clock cycles, of the automated transfers. The core has an internal counter that is decremented each system clock cycle. When the counter reaches zero the core will begin to transmit all data in the transmit queue and reload the internal counter, which will immediately begin to start count down again. If the core has a transfer in progress when the counter reaches zero, the core will stall and not start a new transfer, or reload the internal counter, before the ongoing transfer has completed.

The number of bits in this register is implementation dependent. Software should write this register with 0xFFFFFFFF and read back the value to see how many bits that are available.

Note: This register is only available if AMODE (bit 18) in the SPI controller Capability register is set

100.3.13SPI Controller AM Mask Register(s)

*Table 1628.*0x50-0x5C - AMMASK - SPI controller AM Mask register(s)

31	0
AM MASK	
0	
rw	

31 : 0 AM Mask - This field is used as a bit mask to determine which words in the AM Transmit / Receive queues to read from / write to. Bit 0 of the first mask register corresponds to the first position in the queues, bit 1 of the first mask register to the second position, bit 0 of the second mask register corresponds to the 33:d position, etc. The total number of bits implemented equals FDEPTH (bit 15:8) in the SPI controller Capability register. If a bit is set to one then the core will read / write the corresponding position in the queue, otherwise it will be skipped. Software can write these registers at all times. However if a automated transfer is in progress when the write occurs, then the core will save the new value in a temporary register until the transfer is complete. The reset value is all ones.

Note: This register is only available if AMODE (bit 18) in the SPI controller Capability register is set

100.3.14SPI Controller AM Transmit Register(s)

*Table 1629.*0x200-0x3FC - AMTX - SPI controller AM Transmit register(s)

31	0
TDATA	
0	
rw	

31 : 0 Transmit data (TDATA) - Writing a word into these register places the word in the AM Transmit queue. The address of the register determines the position in the queue. Address offset 0x200 corresponds to the first position, offset 0x204 to the second position etc.

The layout of the registers during write depends on the value of the REV field in the Mode register:
Rev = ‘0’: The word to transmit should be written with its least significant bit at bit 0.
Rev = ‘1’: The word to transmit should be written with its most significant bit at bit 31.

The layout of the registers during read is fixed, the word is read with its least significant bit at bit 0.

Note: This register is only available if AMODE (bit 18) in the SPI controller Capability register is set

100.3.15SPI Controller AM Receive Register

*Table 1630.*0x400-0x5FC - SPI controller AM Receive register(s)

31	0
RDATA	
0	
rw	

31 : 0 Receive data (RDATA) - The address of the register determines the position in the queue. Address offset 0x200 corresponds to the first position, offset 0x204 to the second position etc. The placement of the received word depends on the Mode register fields LEN and REV.

For LEN = 0b0000 - The data is placed with its MSb in bit 31 and its LSb in bit 0.

For other lengths and REV = '0' - The data is placed with its MSB in bit 15.

For other lengths and REV = '1' - The data is placed with its LSB in bit 16.

To illustrate this, a transfer of a word with eight bits (LEN = 7) that are all set to one will have the following placement:

REV = '0' - 0x0000FF00

REV = '1' - 0x00FF0000

Note: This register is only available if AMODE (bit 18) in the SPI controller Capability register is set

100.4 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x02D. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

100.5 Implementation

100.5.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core will use asynchronous reset for all registers, except synchronization registers, if the GRLIB config package setting *grlib_async_reset_enable* is set.

See also the documentation for the *syncrst* VHDL generic.

100.6 Configuration options

Table 1631 shows the configuration options of the core (VHDL generics).

*Table 1631.*Configuration options

Generic name	Function	Allowed range	Default
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	ADDR field of the APB BAR.	0 - 16#FFF#	0
pmask	MASK field of the APB BAR.	0 - 16#FFF#	16#FFF#
pirq	Interrupt line used by SPI controller	0 - NAHBIRQ-1	0

*Table 1631.*Configuration options

Generic name	Function	Allowed range	Default
fdepth	FIFO depth. The FIFO depth in the core is 2^{fdepth}. Note that the depth of the transmit and receive queues is FIFO depth + 1 since the Transmit and Receive registers can hold one word. The number of AM Transmit / Receive registers are however 2^{fdepth}.	1 - 7	1
slvselen	Enable Slave Select register. When this value is set to 1 the core will include a slave select register that controls slvselsz slave select signals.	0 - 1	0
slvselsz	Number of Slave Select (slvsel) signals that the core will generate. These signals can be controlled via the Slave select register if the generic slvselen has been set to 1, otherwise they are driven to '1'.	1 - 32	1
oepol	Selects output enable polarity	0 - 1	0
odmode	Open drain mode. If this generic is set to 1, the OD bit in the mode register can be set to 1 and the core must be connected to I/O or OD pads.	0 - 1	0
automode	Enable automated transfers. If this generic is set to 1 the core will include support to automatically perform periodic transfers. The core's receive and transmit queues must not contain more than 128 words if automode is enabled.	0 - 1	0
acntbits	Selects the number of bits used in the AM period counter. This generic is only of importance if the automode generic is set to 1.	1 - 32	32
aslvsel	Enable automatic slave select. If this generic is set to 1 the core will include support for automatically setting the slave select register from the automatic slave select register before a transfer, or queue of transfers, starts. This generic is only significant of the slvselen generic is set to 1.	0 - 1	0
twen	Enable 3-wire protocol. If this generic is set to 1 the core will include support for 3-wire protocol.	0 - 1	1
maxwlen	Determines the maximum supported word length. Values are defined as: 0 - Core will support lengths up to 32-bit words 0-3 - Illegal values 4-15 - Maximum word length is maxlen+1, allows words of length 4-16 bits. This generic sets the size of the slots in the transmit and receive queues. If the core will be used in an application that will never need to perform transfers with words as long as 32-bits, this setting can be used to save area.	0 - 15	0
netlist	If this generic is set to 0 (default) then the RTL version of the core will be used. If this generic is non-zero, the netlist version of the core will be used (if available) and the value of *netlist* will specify the target technology.	0 - NTECH	0
syncram	When this generic is set to 1 the core will instantiate SYNCRAM_2P components for the receive and transmit queues. The use of SYNCRAM_2P components can reduce area requirements, particularly when automode is enabled.	0 - 1	1
memtech	Selects memory technology for SYNCRAM_2P components.	0 - NTECH	0 (inferred)

*Table 1631.*Configuration options

Generic name	Function	Allowed range	Default
ft	Enables fault tolerance for receive and transmit queues. 0 - No fault tolerance, 1 - Parity DMR, 2 - TMR. This generic only has effect if generic syncram is non-zero.	0 - 2	0
scantest	Enable scan test support. Only applicable if generic syncram is /= 0.	0 - 1	0
syncrst	Use only synchronous reset. If this generic is 0 then the spio.sckoen, spio.misooen, spio.mosioen and slvsel output will have asynchronous reset. If synchronous reset for these registers is wanted then set this generic to 1. Note that if grlib_async_reset_enable in the GRLIB configuration package is enabled then this will override the syncrst setting ans all registers, except synchronization registers in the code will have asynchronous reset.	0 - 1	0
ignore	Enable AIGNORE/CIGNORE inputs (experimental)	0 - 1	0
prot	Selects what protocols (note that support for 3-wire protocol is selected by the *twen* generic). The value of prot has the following effect: 0 - Support for standard SPI protocol 1 - Support for standard and dual SPI protocols 2 - Support for standard, dual and quad SPI protocols	0 - 2	0

100.7 Signal descriptions

Table 1632 shows the interface signals of the core (VHDL ports).

*Table 1632.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-

*Table 1632.*Signal descriptions

Signal name	Field	Type	Function	Active
SPII	MISO	Input	Master-Input-Slave-Output data line, not used with 3-wire protocol.	-
	MOSI	Input	Master-Output-Slave-Input data line	-
	SCK	Input	Serial Clock. If the core is instantiated in a system where it will work only as a master then drive this signal constant Low to save some area.	-
	SPISEL	Input	Slave select input. This signal should be driven High if it is unused in the design.	Low
	ASTART	Input	Automated transfer start. The core can be programmed to use this signal to start a set of automated transfers. This signal should be driven low if it is unused in the design. This signal must be synchronous to the CLK input.	High
	CSTART	Input	Automated clock start. This signal can be used to control when an individual transfer in a set of automated transfers should start. This signal doesn't affect the start of the first transfer in the set. Also the core needs to be programmed to use the signal. This signal should be driven low if it is unused in the design. This signal must be synchronous to the CLK input.	High
	AIGNORE	Input	Ignore RX fifo adddress increment, ignore first TX fifo address increment	High
	CIGNORE	Input	Ignore TX fifo address increment	High
	IO2	Input	Data line 2, used with quad SPI protocol	-
	IO3	Input	Data line 3, used with quad SPI protocol	-
SPIO	MISO	Output	Master-Input-Slave-Output data line, not used in with 3-wire protocol.	-
	MISOOEN	Output	Master-Input-Slave-Output output enable, not used with 3-wire protocol.	-
	MOSI	Output	Master-Output-Slave-Input	-
	MOSIOEN	Output	Master-Output-Slave-Input output enable	-
	SCK	Output	Serial Clock	-
	SCKOEN	Output	Serial Clock output enable	-
	SSN	Output	Not used	-
	ASTART	Output	Automated transfer start indicator.	High
	AREADY	Output	Automated transfer ready indicator. Set each time an individual transfer in a set of automated transfers is completed.	High
	IO2	Output	Data line 2, used with quad SPI protocol	-
	IO2OEN	Output	Data line 2 output enable, used with quad SPI protocol	-
	IO3	Output	Data line 3, used with quad SPI protocol	-
	IO3OEN	Output	Data line 3output enable, used with quad SPI protocol	-
SLVSEL [SSSZ-1:0]	N/A	Output	Slave select output(s). Used if the *slvselen* VHDL generic is set to 1. The range of the vector is (slvselsz-1):0	-

* see GRLIB IP Library User's Manual

100.8 Signal definitions and reset values

The signals and their reset values are described in table 1633.

*Table 1633.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
sck	InputOutput	SPI clock	-	Hi-Z
miso	InputOutput	Master-Input-Slave-Output, not used with 3-wire protocol	-	Hi-Z
mosi	InputOutput	Master-Output-Slave-Input	-	Hi-Z
io2	InputOutput	Data line 2, used with quad SPI protocol	-	Hi-Z
io3	InputOutput	Data line 3, used with quad SPI protocol	-	Hi-Z
spisel	Input	Slave select input	Logical 0	-
slvsel[SSSZ-1:0]	Output	Slave select signals	Logical 0	Logical 1

100.9 Timing

The timing waveforms and timing parameters are shown in figure 268 and are defined in table 1634.

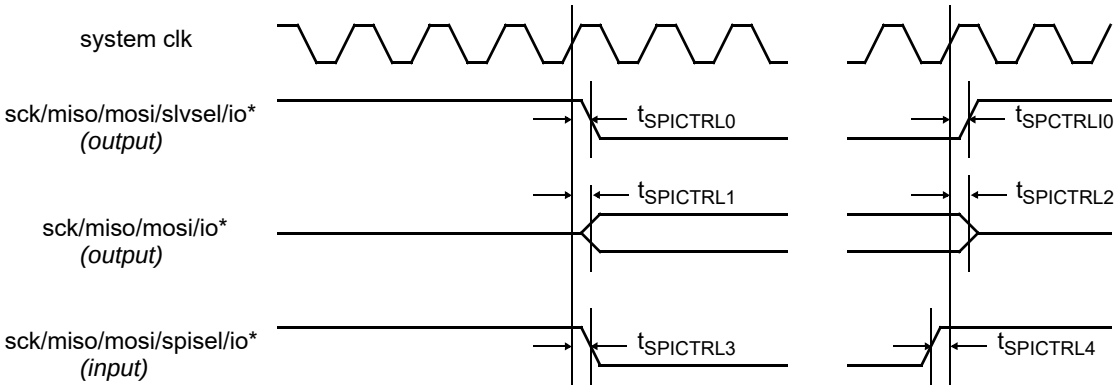


Figure 268. Timing waveforms

*Table 1634.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{SPICTRL0}$	clock to output delay	rising *clk* edge	TBD	TBD	ns
$t_{SPICTRL1}$	clock to non-tri-state delay	rising *clk* edge	TBD	TBD	ns
$t_{SPICTRL2}$	clock to tri-state delay	rising *clk* edge	TBD	TBD	ns
$t_{SPICTRL3}$	input to clock hold	rising *clk* edge	-	-	ns
$t_{SPICTRL4}$	input to clock setup	rising *clk* edge	-	-	ns

Note: The *sck/miso/mosi/io2/io3/spisel* inputs are re-synchronized internally. The signals do not have to meet any setup or hold requirements.

100.10 Library dependencies

Table 1635 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1635.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	SPI	Component, signals	SPI component and signal definitions.
TECHMAP	GENCOMP	Constant values	Technology constants
TECHMAP	NETCOMP	Component	Netlist component

100.11 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib, techmap;
use grlib.amba.all;
use techmap.gencomp.all;

library gaisler;
use gaisler.misc.all;

entity spi_ex is
  port (
    clk    : in std_ulogic;
    rstn   : in std_ulogic;

    -- SPI signals
    sck    : inout std_ulogic;
    miso   : inout std_ulogic;
    mosi   : inout std_ulogic;
    spisel : in std_ulogic
    );
end;

architecture rtl of spi_ex is

  -- AMBA signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);

  -- SPIsignals
  signal spii : spi_in_type;
  signal spio : spi_out_type;
begin

  -- AMBA Components are instantiated here
  ...

  -- SPI controller with FIFO depth 2 and no slave select register
  spictrl0 : spictrl generic map (pindex => 10, paddr => 10, pirq => 10,
                                  fdepth => 1, slvselen => 0, slvselsz => 1)
      port map (rstn, clkm, apbi, apbo(10), spii, spio, open);

    misopad : iopad generic map (tech => padtech)
      port map (miso, spio.miso, spio.misooen, spii.miso);
    mosipad : iopad generic map (tech => padtech)
      port map (mosi, spio.mosi, spio.mosioen, spii.mosi);
    sckpad : iopad generic map (tech => padtech)
      port map (sck, spio.sck, spio.sckoen, spii.sck);
    spiselpad : inpad generic map (tech => padtech)
      port map (spisel, spii.spisel);
end;
```

101 SPIMCTRL - SPI Memory Controller

101.1 Overview

The core maps a memory device connected via the Serial Peripheral Interface (SPI) into AMBA address space. Read accesses are performed by performing normal AMBA read operations in the mapped memory area. Other operations, such as writes, are performed by directly sending SPI commands to the memory device via the core's register interface. The core is highly configurable and supports most SPI Flash memory devices.

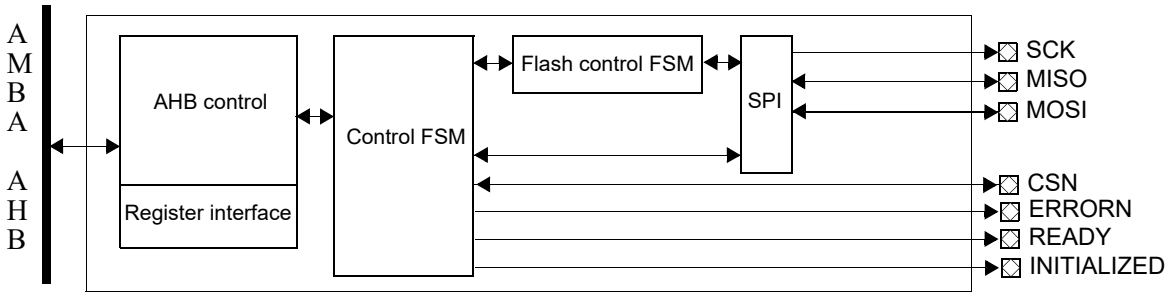


Figure 269. Block diagram

101.2 Operation

101.2.1 Operational model

The core has two memory areas that can be accessed via the AMBA bus; the I/O area and the ROM area. The ROM area maps the memory device into AMBA address space and the I/O area is utilized for status reporting and to issue user commands to the memory device.

When transmitting SPI commands directly to the device the ROM area should be left untouched. The core will issue an AMBA ERROR response if the ROM area is accessed when the core is busy performing an operation initiated via I/O registers.

Depending on the type of device attached the core may need to perform an initialization sequence. Accesses to the ROM area during the initialization sequence receive AMBA error responses. The core has successfully performed all necessary initialization when the Initialized bit in the core's status register is set, the value of this bit is also propagated to the core's output signal *spio.initialized*.

101.2.2 I/O area

The I/O area contains registers that are used when issuing commands directly to the memory device. By default, the core operates in System mode where it will perform read operations on the memory device when the core's ROM area is accessed. Before attempting to issue commands directly to the memory device, the core must be put into User mode. This is done by setting the User Control (USRC) bit in the core's Control register. Care should be taken to not enter User mode while the core is busy, as indicated by the bits in the Status register. The core should also have performed a successful initialization sequence before User mode accesses (INIT bit in the Status register should be set).

Note that a memory device may need to be clocked when there has been a change in the state of the chip select signal. It is recommended that software transmits a byte with the memory device deselected after entering and before leaving User mode.

The following steps are performed to issue a command to the memory device after the core has been put into User mode:

1. Check Status register and verify that the BUSY and DONE bits are cleared. Also verify that the core is initialized and not in error mode.

2. Optionally enable DONE interrupt by setting the Control register bit IEN.
3. Write command to Transmit register.
4. Wait for interrupt (if enabled) or poll DONE bit in Status register.
5. When the DONE bit is set the core has transferred the command and will have new data available in the Receive register.
6. Clear the Status register's DONE bit by writing one to its position.

The core should not be brought out of User mode until the transfer completes. Accesses to ROM address space will receive an AMBA ERROR response when the core is in User mode and when an operation initiated under User mode is active.

101.2.3 ROM area

The ROM area only supports AMBA read operations. Write operations will receive AMBA ERROR responses. When a read access is made to the ROM area the core will perform a read operation on the memory device. If the system has support for AMBA SPLIT responses the core will SPLIT the master until the read operation on the memory device has finished, unless the read operation is a locked access. A locked access never receives a SPLIT response and the core inserts wait states instead. If the system lacks AMBA SPLIT support the core will always insert wait states until the read operation on the memory device has finished. The core uses the value of the VHDL generic *spliten* to determine if the system has AMBA SPLIT support.

The ROM area is marked as cacheable and prefetchable. This must be taken into account if the data in the ROM area is modified via the I/O area.

101.2.4 SPI memory device address offset

An offset can be specified at implementation via the core's *offset* VHDL generic. This offset will be added to all accesses to the ROM area before the address is propagated to the SPI memory device. Specifying an offset can be useful when the SPI memory device contains, as an example, FPGA configuration data at the lower addresses. By specifying an offset, the top of the SPI memory device can be used to hold user data. The AMBA system is unaware of the offset being added. An access to address *n* in the ROM area will be automatically translated to an access to address *offset* + *n* on the SPI memory device.

The offset must be accounted for when accessing the SPI memory device via the core's register interface. If data is programmed to the SPI memory device then the data must be written starting at the offset specified by the VHDL generic *offset*.

101.2.5 Supported memory devices

The core supports a wide range of memory devices due to its configuration options of read instruction, dummy byte insertion and dual output. Table 1636 below lists configurations for some memory devices.

*Table 1636.*Configurations for some memory devices

		VHDL generic*		
Manufacturer	**Memory device**	**readcmd****	**dummybyte**	**dualoutput**
Spansion	S25FL-series	0x0B	1	0
Winbond	W25X-series	0x0B	1	0
	W25X-series with dual output read.	0x3B	1	1
* '-' means don't care ** Available in the core's Configuration register.				

The core is configured to issue the instruction defined by the VHDL generic *readcmd* to obtain data from the device. After an access to the ROM area the core will issue the read instruction followed by 24 address bits. If the VHDL generic *dummybyte* is set to 1 the core will issue a dummy byte following the address. After the possible dummy byte the core expects to receive data from the device. If the VHDL generic *dualoutput* is set to 1 the core will read data on both the MISO and MOSI data line. Otherwise the core will only use the MISO line for input data.

Many memory devices support both a READ and a FAST_READ instruction. The FAST_READ instruction can typically be issued with higher device clock frequency compared to the READ instruction, but requires a dummy byte to be present after the address. The most suitable choice of read instruction depends on the system frequency and on the memory device's characteristics.

101.2.6 Clock generation and power-up timing

The core generates the device clock by scaling the system clock. The VHDL generic *scaler* selects the divisor to use for the device clock that is used when issuing read instructions.

The alternate clock can be used for all communication by setting the Enable Alternate Scaler (EAS) bit in the Control register. When configuring the core for communication with a device in a system where the target frequency may change it is recommended to set the VHDL generic *scaler* to a conservative value and configure the alternate scaler to produce a faster clock. A boot loader can then set the Enable Alternate Scaler (EAS) bit early in the boot process when it has been determined that the system can use the memory device at a higher frequency.

If the external device needs power-up time before being accessed then this needs to be handled at the system level or by waiting to access the SPI memory controller until the power up time has passed.

101.3 Registers

The core is programmed through registers mapped into AHB address space.

*Table 1637.*SPIMCTRL registers

AHB address offset	Register
0x00	Configuration register
0x04	Control register
0x08	Status register
0x0C	Receive register
0x10	Transmit register

101.3.1 Configuration Register

*Table 1638.*0x00 - CONF - Configuration register

31 8	7 0
RESERVED	READCMD
0	*
r	r

31 :8 RESERVED

7:0 Read instruction (READCMD) - Read instruction that the core will use for reading from the memory device.

101.3.2 Control Register

*Table 1639.*0x04 - CTRL - Control register

31 5	4	3	2	1	0
RESERVED	RST	CSN	EAS	IEN	USRC
	0	1	0	0	0
	rw*	rw*	rw	rw	rw

31 :5 RESERVED

4 Reset core (RST) - By writing '1' to this bit the user can reset the core. This bit is automatically cleared when the core has been reset. Reset core should be used with care. Writing this bit has the same effect as system reset. Any ongoing transactions, both on AMBA and to the SPI device will be aborted.

3 Chip select (CSN) - Controls core chip select signal. This field always shows the level of the core's internal chip select signal. This bit is always automatically set to '1' when leaving User mode by writing USRC to '0'.

2 Enable Alternate Scaler (EAS) - When this bit is set the SPI clock is divided by using the alternate scaler.

1 Interrupt Enable (IEN) - When this bit is set the core will generate an interrupt when a User mode transfer completes.

0 User control (USRC) - When this bit is set to '1' the core will accept SPI data via the transmit register. Accesses to the memory mapped device area will return AMBA ERROR responses.

101.3.3 Status Register

*Table 1640.*0x08 - STAT - Status register

31 3	2	1	0
RESERVED	INIT	BUSY	DONE
0	0	0	0
r	r	r	wc

31:3 RESERVED

2 Initialized (INIT) - This read only bit is set to '1' when the SPI memory device has been initialized. Accesses to the ROM area should only be performed when this bit is set to '1'.

1 Core busy (BUSY) - This bit is set to '1' when the core is performing an SPI operation.

0 Operation done (DONE) - This bit is set to '1' when the core has transferred an SPI command in user mode.

Reset value: 0x00000000

101.3.4 Receive Register

*Table 1641.*0x0C - RX - Receive register

31 8	7 0
RESERVED	RDATA
0	nr
R	rw

31 :8 RESERVED

7:0 Receive data (RDATA) : Contains received data byte

Reset value: 0x000000UU, where U is undefined

101.3.5 Transmit Register

*Table 1642.*0X10 - TX - Transmit register

31 8	7 0
RESERVED	TDATA
0	0
r	rw

31 :8 RESERVED

7:0 Transmit data (TDATA) - Data byte to transmit

101.4 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x045. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

101.5 Implementation

101.5.1 Reset

The core changes reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual).

The core will add reset for all registers if the GRLIB config package setting *grlib_sync_reset_enable_all* is set.

The core does not support *grlib_async_reset_enable*. All registers that react on the reset signal will have a synchronous reset.

101.5.2 Technology mapping

The core does not instantiate any technology specific primitives.

101.5.3 RAM usage

The core does not use any RAM components.

101.6 Configuration options

Table 1643 shows the configuration options of the core (VHDL generics).

*Table 1643.*Configuration options

Generic name	Function	Allowed range	Default
hindex	AHB slave index	0 - (NAHBSLV-1)	0

*Table 1643.*Configuration options

Generic name	Function	Allowed range	Default
hirq	Interrupt line	0 - (NAHBIRQ-1)	0
faddr	ADDR field of the AHB BAR1 defining ROM address space.	0 - 16#FFF#	16#000#
fmask	MASK field of the AHB BAR1 defining ROM address space.	0 - 16#FFF#	16#FFF#
ioaddr	ADDR field of the AHB BAR0 defining register address space.	0 - 16#FFF#	16#000#
iomask	MASK field of the AHB BAR0 defining register space.	0 - 16#FFF#	16#FFF#
spliten	If this generic is set to 1 the core will issue AMBA SPLIT responses when it is busy performing an operation on the memory device. Otherwise the core will insert wait states until the operation completes.	0 - 1	0
oepol	Select polarity of output enable signals. 0 = active low.	0 - 1	0
sdcard	Set to 0	0 - 0	0
readcmd	Read instruction of memory device	0 - 16#FF#	16#0B#
dummybyte	Output dummy byte after address	0 - 1	0
dualoutput	Use dual output when reading data from device	0 - 1	0
scaler	Clock divisor used when generating device clock is 2^{scaler}	1 - 512	1
altscaler	Clock divisor used when generating alternate device clock is $2^{altscaler}$	1 - 512	1
pwrupcnt	Unused	N/A	0
maxahbaccsz	Maximum supported AHB access size. The core will support accesses ranging from 8-bit (BYTE) to the size set by maxahbaccsz. The maximum access size is 256 bits (8WORD).	32, 64, 128, 256	AHBDW
offset	Specifies offset that will be added to incoming AMBA address before address is propagated to SPI flash device. An access to memory position *n* in the core's ROM area will be translated to an access to SPI memory device address *n* + *offset*. Note that this only applies to accesses to the ROM area, accesses via the core's register interface are unaffected.	-	0

101.7 Signal descriptions

Table 1644 shows the interface signals of the core (VHDL ports).

*Table 1644.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
AHBSI	*	Input	AHB slave input signals	-
AHBSO	*	Output	AHB slave output signals	-
SPII	MISO	Input	Master-input slave-output data line	-
	MOSI	Input	Master-output slave-input data line	-
	CD	Input	Unused	-
SPIO	MOSI	Output	Master-output slave-input data line	-
	MOSIOEN	Output	Master-output slave-input output enable	-

*Table 1644.*Signal descriptions

Signal name	Field	Type	Function	Active
	SCK	Output	SPI clock	-
	CSN	Output	Chip select	Low
	CDCSNOEN	Output	Chip select output enable. This signal can be left unconnected and CSN should be connected to an output pad.	-
	READY	Output	When this signal is low the core is busy performing an operation.	High
	INITIALIZED	Output	This bit goes high when the SPI memory device has been initialized and can accept read accesses. This signal has the same value as the Initialized (INIT) bit in the core's Status register.	High

* see GRLIB IP Library User's Manual

101.8 Signal definitions and reset values

The signals and their reset values are described in table 1645.

*Table 1645.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
miso	Inout	Data into the master	-	-
mosi	Output	Data out of the master, can also serve as bi-directional signal if the core is configured to function with dual output memory devices.	-	Logical 1
sck	Output	SPI clock	Logical 1	Logical 0
csn	Output	Chip select, can also be used as a card detect signal in which case the signal is bi-directinal.	Logical 0	Logical 1
ready	Output	Core ready	Logial 1	Logical 0
initialized	Output	Memory device initialized	Logical 1	Logical 0

101.9 Library dependencies

Table 1646 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1646.*Library dependencies

Library	Package	Imported unit(s)	Description
GAISLER	SPI	Component, signals	Component and signal definitions
GRLIB	AMBA	Signals	AMBA signal definitions

101.10 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib, techmap;
use grlib.amba.all;
use techmap.gencomp.all;

library gaisler;
use gaisler.memctrl.all;

entity spimctrl_ex is
```

```
  port (
    clk       : in  std_ulogic;
    rstn      : in  std_ulogic;
    -- SPIMCTRL signals
    -- For SPI Flash
    spi_c     : out std_ulogic;
    spi_d     : out std_ulogic;
    spi_q     : in  std_ulogic;
    spi_sn    : out std_ulogic
    );
end;

architecture rtl of spimctrl_ex is
  -- AMBA signals
  signal ahbsi  : ahb_slv_in_type;
  signal ahbso  : ahb_slv_out_vector := (others => ahbs_none);
  ...
  -- SPIMCTRL signals
  signal spmi1 : spimctrl_in_type;
  signal spmo1 : spimctrl_out_type;
begin

  -- AMBA Components are instantiated here
  ...

  -- SPMCTRL core, configured for use with generic SPI Flash memory with read
  -- command 0x0B and a dummy byte following the address.
  spimctrl1 : spimctrl
      generic map (hindex => 4, hirq => 4, faddr => 16#b00#, fmask  => 16#fff#,
                   ioaddr => 16#200#, iomask => 16#fff#, spliten => CFG_SPLIT,
                   sdcard => 0, readcmd => 16#0B#, dummybyte => 1, dualoutput => 0,
                   scaler => 1, altscaler => 1)
      port map (rstn, clk, ahbsi, ahbso(4), spmi1, spmo1);

    spi_miso_pad : inpad generic map (tech => padtech)
      port map (spi_q, spmi1.miso);
    spi_mosi_pad : outpad generic map (tech => padtech)
      port map (spi_d, spmo1.mosi);
    spi_sck_pad  : outpad generic map (tech => padtech)
      port map (spi_c, spmo1.sck);
    spi_slvsel0_pad : outpad generic map (tech => padtech)
      port map (spi_sn, spmo1.csn);
end;
```

102 SPIMASTER - SPI Master Device

102.1 Overview

The core provides a link between the AMBA APB bus and the Serial Peripheral Interface (SPI) bus and function as a SPI master. Core features include configurable word length (4, 5, 6... 32 bits), bit ordering and all four SPI modes are supported. This IP is developed as part of ESA activity: Prototyping of space protocol(s) for SPI (Contract: 4000114112/15/NL/LF).

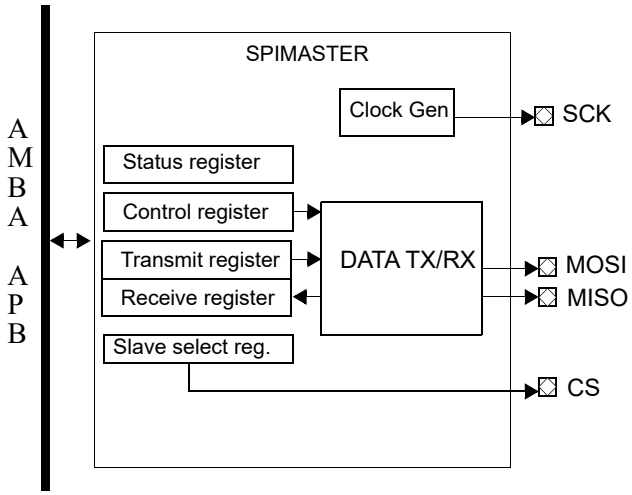


Figure 270. Block diagram

102.2 Transmission

The SPI bus is a full-duplex synchronous serial bus. Transmission starts when a master selects a slave through the slave's Slave Select (CS) signal and the clock line SCK transitions from its idle state. The clock line transition occurs when the EN bit in the Transmit Enable register is set to "high", the data need to be transferred must be written into the Transmit register before writing the transmit enable register. Data is transferred from the master through the Master-Output-Slave-Input (MOSI) signal and from the slave through the Master-Input-Slave-Output (MISO) signal. The SCK is only available during the data transfer and return to idle state after the transmission is completed.

During a transmission on the SPI bus data is either changed or read at a transition of SCK. If data has been read at edge n, data is changed at edge n+1. If data is read at the first transition of SCK the bus is said to have clock phase 0, and if data is changed at the first transition of SCK the bus has clock phase 1. The idle state of SCK may be either high or low. If the idle state of SCK is low, the bus has clock polarity 0 and if the idle state is high the clock polarity is 1. The combined values of clock polarity (CPOL) and clock phase (CPHA) determine the mode of the SPI bus. Figure below shows one byte (0x55) being transferred MSb first over the SPI bus under the four different modes. Note that the idle state of the MOSI line is '1' and that CPHA = 0 means that the devices must have data ready before the first transition of SCK. The figure does not include the MISO signal, the behavior of this line is the same as for the MOSI signal.

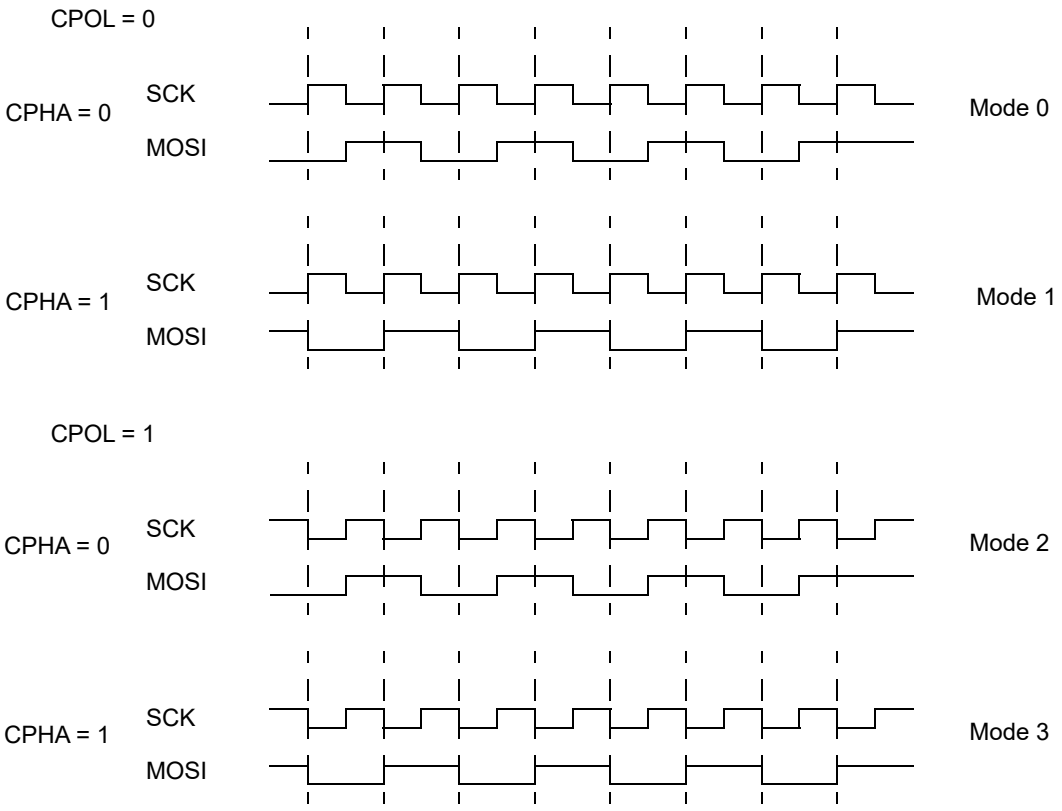


Figure 271. SPI transfer of byte 0x55 in all modes

102.3 Operation

The data transfer between this master and a slave device is performed using the registers mapped into APB address space. The data need to be transferred must be written into the Transmit register and the EN bit in the Transmit Enable register must be set “high” inorder to send and receive, the receive data is available when the transmission is completed. The EN bit will be set by the core to “low” when all the transmission is completed. It is also possible to generate an interrupt when all the transmission is completed using Transmission Done interrupt. The core’s control, polarity, chip select, clock registers must be appropriately set as per the requirements of the slave device. The SCK is only available during the data transfer and return to idle state after the transmission is completed.

The core can hold a data in addition to the one currently in transfer. The BC field in Status register specify the number of data available. If two words are written into the Transmit register the BC field show a value of 2, after the first transfer the value will be 1and finally when the transfer is completed the BC field will have value 0. The purpose of the hold register is to continuously transfer data to a slave device. In order to transfer continuously the software should perform the following, write two data to be transferred into the Transmit register and enable the transfer, after the first data is transferred (the software can learn about the data transfer either by polling the BC in Status register or using the RX Received data interrupt) the software can write the consecutive data into the Transmit register.

In order to receive a data the master should transmit a data. The Software should take care of clearing (reading) the data available in the received register before transmitting (receiving) an another data. The transmit buffer is maximum 32 bit (WLEN in Control register defines the Word length bit count), note also a transmit hold register is available which is also maximum 32 bit (also depends on the WLEN bit count). The Software controlling the master should take into account the response time of the slave (or by polling the EN bit in the Transmit Enable register, or by using the interrupt triggered

RX Received data interrupt) to determine when a transmission is completed, and also make sure the received data is read back before the next data is set to be transfered.

It is possible an overrun condition could occur if a received data is not read before the arrival of next data. If new data arrived before the Software could read the previously received data overrun condition is triggered. An Overrun interrupt is generated when overrun condition occurs for data reception.

102.4 Registers

The core is programmed through registers mapped into APB address space.

*Table 1647.*APB registers

APB address offset	Register
0x00	Control register
0x04	Status register
0x08	Clock divide register
0x0C	Chip select polarity register
0x10	Chip select register
0x14	Transmit register
0x18	Transmit enable register
0x1C	Receive register
0x20	Interrupt enable register
0x24	Interrupt register

102.4.1 Control Register

*Table 1648.*0x00 - CTRL - Control register

31 24	23-17	16	15-13	12 8	7	6	5	4	3	2	1	0
Key	R	OD	R	WLEN	IAMBA	CPHA	CPOL	REV	LOOP	RESET	R	R
0	0	0	0	0x0F	0	0	0	1	0	0	0	0
w	r	rw	r	rw	rw	rw	rw	rw	rw	rw	r	r

31 Safety code (KEY) - Must be 0x94 when writing, otherwise register write is ignored

23 : 17 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

16 Overrun detect (OD) - To detect overrun condition (also to trigger overrun interrupt) this bit must be enabled.

15 : 13 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

12 : 8 Word length (WLEN) - The value of this field determines the length in bits of a transfer on the SPI bus. Valid values are 0x03 to 0x1F

Word length is WLEN+1, allows words of length 4-32 bits.

7 AMBA Interrupt enable (IAMBA) - If set, AMBA interrupt generation is enabled for the events that are individually maskable by the Interrupt enable (INTE) register

6 Clock phase (CPHA) - When CPHA is '0' data will be read on the first transition of SCK. When CPHA is '1' data will be read on the second transition of SCK.

5 Clock polarity (CPOL) - Determines the polarity (idle state) of the SCK clock.

4 Reverse data (REV) - When this bit is '0' data is transmitted LSB first, when this bit is '1' data is transmitted MSB first.

3 Loop mode (LOOP) - When this bit is set, the core's transmitter and receiver are interconnected and the core will operate in loopback mode.

2 Reset (RESET) - Resets all the registers in the core.

1 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

0 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

102.4.2 Status Register

*Table 1649.*0x00 - CTRL - Control register

31 2	1 0
R	BC
	0
	r

31: 2 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

1:0 Buffer count BC - Transmit buffer count (maximum 2)

102.4.3 Clock Divide Register

*Table 1650.*0x08 - CDR - Clock divide register

31 24	23 0
Key	CD
0	0
w	rw

*Table 1650.*0x08 - CDR - Clock divide register

31	Safety code (KEY) - Must be 0x94 when writing, otherwise register write is ignored
23 : 0	Clock divide (CD) - This value is used to divide the system clock and generate the SPI SCK clock. If the value is '0' then the system clock is divided by two and the SCK frequency is half the system clock. Similarly if the value is '1' the SCK frequency is 1/4 the system clock. if the value is '2' the SCK frequency is 1/6 the system clock. if the value is '3' the SCK frequency is 1/8 the system clock. if the value is '4' the SCK frequency is 1/10 the system clock.

102.4.4 Chip Select Polarity Register

*Table 1651.*0x0C - CSP - Chip select polarity register

31 24	23 8	7 0
Key	R	CSP
0	0	0
w	r	rw

31 : 24	Safety code (KEY) - Must be 0x94 when writing, otherwise register write is ignored
23 : 8	RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.
7 : 0	Chip select polarity (CSP) - This register is provided in order to be able to communicate with devices having an active high chip select polarity. By default the polarity is active low.

102.4.5 Chip Select Register

*Table 1652.*0x10 - CS - Chip select register

31 24	23 8	7 0
Key	R	CS
0	0	0xFFFFFF
w	r	rw

31 : 24	Safety code (KEY) - Must be 0x94 when writing, otherwise register write is ignored
23 : 8	RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.
7 : 0	Chip select (CS) - The slave device must be selected before starting communication. Software is solely responsible for activating the correct chip select signal, the core does not assert or deassert any chip select signal automatically.

102.4.6 Transmit Register

*Table 1653.*0x14 - TDATA - Transmit register

31	0
TDATA	
0	
rw	

31 : 0 Transmit data (TDATA) - The written data is transferred to the slave device when appropriate conditions for CS and SCK are satisfied. The word to transmit should be written with its least significant bit at bit 0. Also note that only the number of bits need to be transferred from this register should match the word length register (WLEN).

102.4.7 Transmit Enable Register

*Table 1654.*0x18 - TE - Transmit enable register

31	24	23	1	0
Key		R		EN
0		0		0
w		r		rw

31 : 24 Safety code (KEY) - Must be 0x94 when writing, otherwise register write is ignored

23 : 1 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

0 Enable (EN) - The written data in the Transmit register is transferred to the slave device when EN bit is set. This bit will go low when the transmission is completed.

102.4.8 Receive Register

*Table 1655.*0x1C - RDATA - Receive register

31	0
RDATA	
0	
r	

31 : 0 Receive data (RDATA) - This register contains received data.

102.4.9 Interrupt Enable Register

*Table 1656.*0x20 - INTE- Interrupt enable register

31	24	23	3	2	1	0
Key		RESERVED		OVRE	RXE	TXDE
0		0		0	0	0
w		r		rw	rw	rw

31 : 24 Safety code (KEY) - Must be 0x94 when writing, otherwise register write is ignored.

23 : 3 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

2 Overrun interrupt enable (OVRE) - If enabled an interrupt will be generated when overrun condition occurs for data reception.

1 Received data enable (RXE) - If enabled an interrupt is generated when a data is received.

0 Transmission done interrupt enable (TXDE) - If enabled an interrupt is generated when a data transmission is completed.

102.4.10Interrupt Register

*Table 1657.*0x24 - INT- Interrupt register

31 24	23 2	1	0
Key	RESERVED	OVR	RX	TXD
0	0	0	0	0
w	r	wc	wc	wc

31 : 24	Safety code (KEY) - Must be 0x94 when writing, otherwise register write is ignored.
23 : 1	RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.
2	Overrun interrupt (OVR) - An interrupt is generated when overrun condition occurs for data reception. (a received data must be read before the arrival of next data, if new data arrived before the Software could read the previously received data overrun condition is triggered)
1	Received data (RX) - An interrupt is generated when a data is received.
0	Transmission done (TXD) - Data Transmission completed (when the transmit and hold buffer is empty after a transmission).

102.5 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x0A6. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

102.6 Implementation

102.6.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

102.7 Configuration options

Table 1658 shows the configuration options of the core (VHDL generics).

*Table 1658.*Configuration options

Generic name	Function	Allowed range	Default
gSLVSEL	Number of slave select signals that the core will generate.	1 - 24	1
gPINDEX	APB slave index	0 - NAPBSLV-1	0
gHINDEX	Unused	0	0
gPADDR	ADDR field of the APB BAR	0 - 16#FFF#	0
gPMASK	MASK field of the APB BAR.	0 - 16#FFF#	16#FFF#
gPIRQ	Interrupt line driven by APB interface.	0 - NAHBIRQ-1	1

102.8 Signal descriptions

Table 1659 shows the interface signals of the core (VHDL ports).

*Table 1659.*Signal descriptions

Signal name	Type	Function	Active
RSTN	Input	Reset	Low
CLK	Input	Clock	-
APBI	Input	APB slave input signals*	-
APBO	Output	APB slave output signals*	-
MISO	Input	SPI data line input	-
MOSI	Output	SPI data line output	-
SCK	Output	SPI clock line output	-
SLVSEL	Output	Slave select output(s). The range of the vector is (gSLVSEL-1):0	Low

* see GRLIB IP Library User's Manual

102.9 Library dependencies

Table 1660 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1660.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	SPICOMP	Component, signals	Component declaration, SPI signal definitions
GAISLER	GRSPICOMP	Component, signals	Component declaration, SPI signal definitions

102.10 Instantiation

```
library ieee;
use ieee.std_logic_1164.all;
library grlib;
use grlib.amba.all;
use grlib.devices.all;
use grlib.stdlib.all;
library gaisler;
use gaisler.spicomp.all;
use gaisler.grspicomp.all;

entity grspimaster_ex is
   generic (
      gSLVSEL    :    integer range 1 to 24 := 8);
   port (
     rstn        :    in  std_ulogic;
     clk         :    in  std_ulogic;
     apbi        :    in  APB_Slv_In_Type;
     apbo        :    out APB_Slv_Out_Type;
     -- SPI signals
     miso        :    in  std_ulogic;
     mosi        :    out std_ulogic;
     sck         :    out std_ulogic;
     slvsel      :    out std_logic_vector((gSLVSEL-1) downto 0));
end entity grspimaster_ex;

architecture rtl of grspimaster_ex is
  -- AMBA signals
```

```
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector;

  signal sck_mst        :       std_ulogic;
  signal miso_mst       :       std_ulogic;
  signal mosi_mst       :       std_ulogic;
  signal slvsel_mst     :       std_logic_vector(7 downto 0);

begin

   grspimaster0: grspimaster
      generic map (
         gSLVSEL         => gSLVSEL,
         gPINDEX         => 1,
         gPADDR          => 1,
         gPIRQ           => 1)
      port map (
        rstn             => rstn,
        clk              => clk,
        apbi             => apbi,
        apbo             => apbo(1),

        miso             => miso_mst,
        mosi             => mosi_mst,
        sck              => sck_mst,
        slvsel           => slvsel_mst);

   sck_m1pad: outpad generic map (tech => padtech)
      port map (sck, sck_mst);

   mosi_m1pad: outpad generic map (tech => padtech)
      port map (mosi, mosi_mst);

   miso_m1pad: inpad generic map (tech => padtech)
      port map (miso, miso_mst);

   cs_m1pad: outpadv generic map (width => 8, tech => padtech)
      port map (slvsel, slvsel_mst);

end architecture rtl;
```

103 SPISLAVE - Dual Port SPI Slave

103.1 Overview

This core is a Dual Port SPI Slave device that provides link between SPI and AMBA AHB and APB ports. Core features include configurable word length (4, 5, 6 ... 32 bits), bit ordering and all four SPI modes are supported. This core also has redundant SPI ports which can be interfaced using two different masters. The slave takes two sets of SPI interfaces (nominal and redundant each consists of two data signals, one clock signal and one chip select signal). This IP is developed as part of ESA activity: Prototyping of space protocol(s) for SPI (Contract: 4000114112/15/NL/LF).

103.2 Implementation of SPI protocols

This slave device is based on the protocols developed for SPI4SPACE activity. The following text explains the different protocols supported.

In order to support the SPI 0 protocol the slave provides configurable word length of 4, 5, 6 ... 32 bits transmission and reception. The Word bit ordering can be MSB first or LSB first transferred.

For SPI 1 protocol the word length of the transfer can be 8, 16 or 24 bits. The word bit ordering MSB transferred first and LSB transferred last is supported. The parity bit can be appended at the end of every word, the parity bit is not included by the SPI slave device, since the implementation supports 9, 17 and 25 bits of word transfer the parity bit can be appended by the software.

All control and data transfer for SPI protocol 0 and 1 are supported only through the APB registers.

The SPI protocol 2 uses a fixed word length of 16 bits. The word bit ordering is MSB transferred first and LSB transferred last. Also this core implements the network layer of the SPI protocol 2, the slave hardware itself can process the SPI protocol 2 commands and provide responses. The APB interface is only for control and status, all the data transfer to the AMBA is performed using the AHB Master.

:

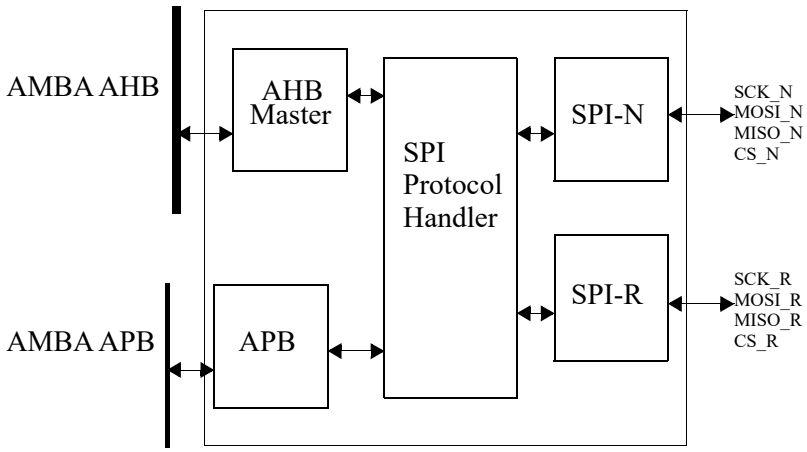


Figure 272. Block diagram

103.3 Transmission

The SPI bus is a full-duplex synchronous serial bus. Transmission starts when a master selects a slave through the slave's Slave Select (CS) signal and the clock line SCK transitions from its idle state. Data is transferred from the master through the Master-Output-Slave-Input (MOSI) signal and from the slave through the Master-Input-Slave-Output (MISO) signal. In some systems with only one master and one slave, the Slave Select input of the slave may be always active and the master does not need

to have a slave select output. This does not apply to this device, the slave select signal must be used to mark the start and end of an operation.

During a transmission on the SPI bus data is either changed or read at a transition of SCK. If data has been read at edge n, data is changed at edge n+1. If data is read at the first transition of SCK the bus is said to have clock phase 0, and if data is changed at the first transition of SCK the bus has clock phase 1. The idle state of SCK may be either high or low. If the idle state of SCK is low, the bus has clock polarity 0 and if the idle state is high the clock polarity is 1. The combined values of clock polarity (CPOL) and clock phase (CPHA) determine the mode of the SPI bus. Figure below shows one byte (0x55) being transferred MSb first over the SPI bus under the four different modes. Note that the idle state of the MOSI line is '1' and that CPHA = 0 means that the devices must have data ready before the first transition of SCK. The figure does not include the MISO signal, the behavior of this line is the same as for the MOSI signal.

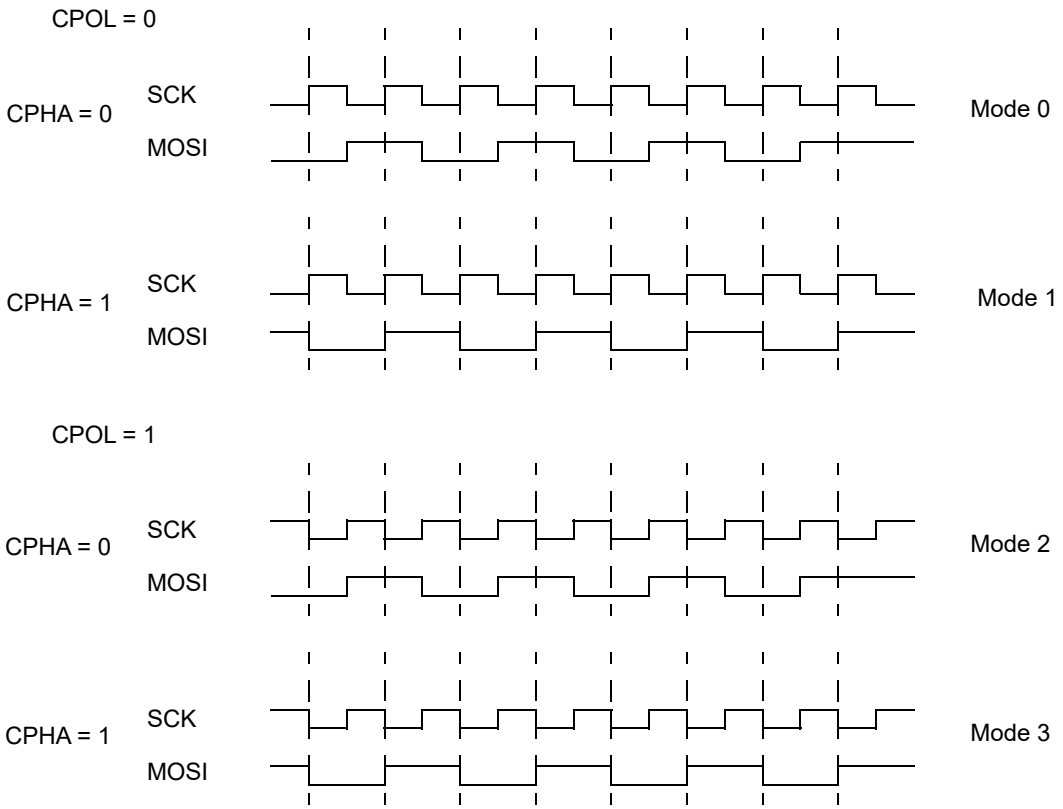


Figure 273. SPI transfer of byte 0x55 in all modes

103.4 Operation

The data transfer between the master and the slave is through APB registers or through command transfer from a master is determined by the EN bit in the SPI2 control register. When APB registers are used the data transferred by a master is available at receive registers (NRDATA or RRDATA depending on the port used) while during the same reception period the contents of the transmit registers (TDATA) are transferred to the master. When appropriate commands are transferred by a master SPI device and EN bit in the SPI2 control register is enabled then the commands are processed by the SPI 2 protocol handler available in this core. The SPI protocol 2 implementation is explained in detail in the following section.

103.5 SPI 2 Protocol Handler

The core is capable of handling the commands (based on SPI protocol 2) transferred by a SPI master and provide response. The message format transferred between a SPI master and SPI slave device is defined below.

*Table 1661.*Example message format (write data)

Signal	*Message Header*		*Payload*	*Payload CRC*
MOSI	*Command #1*	*Command #2*	*Data*	*CRC-16*
MISO	*Response #1*	*Response #2*	*0x0000*	*0x0000*

*Table 1662.*Example message format (read data)

Signal	*Message Header*		*Payload*	*Payload CRC*
MOSI	*Command #1*	*Command #2*	*0x0000*	*0x0000*
MISO	*Response #1*	*Response #2*	*Data*	*CRC-16*

The message header is composed of a Command token from the master and a Response token from the slave. The message also contains optional data words and CRC checksum appended at the end that are calculated for the data words transferred. The CRC is mandatory, if the message contains payload data then the message is always appended with one word of CRC. The received messages are processed by the SPI slave device and response and data are transferred as per the received command. Also note some of the status bits in the response token are status for the previously received command.

The SPI slave has the possibility to address incoming data with clock gaps (splitted) fashion. If the SPI master transfers the data with a clock gap the slave can accept the data and provide proper response. For example if the SPI master is software controlled and has a SPI controller with a word-width that is less than the full message then software needs to keep at least one word in the transmit queue at all times to avoid breaking the protocol. In order to provide a relaxed requirement on software, the SPI2 protocol allow gaps between clock periods (equivalent to stretching a clock period). The gaps must be at word level (16 bits) i.e. the clock gap can be between Command #1 and Command #2 not within the Command #1 16 bits.

103.5.1 Message Header - Command Token

The master transmits a message header that specifies the action need to be performed in slave. The command token sent by the master device consist of two 16 bit words. The message header content details are explained below.

*Table 1663.*Command word 1

MSB	*Command Token Word #1*															*LSB*
Prefix		*Command Code*						*Spare*		*Message Length*						
15	*14*	*13*	*12*	*11*	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*	
'0'	*'1'*	*C5*	*C4*	*C3*	*C2*	*C1*	*C0*	*'1'*	*'1'*	*L5*	*L4*	*L3*	*L2*	*L1*	*L0*	

*Table 1664.*Command word 2

MSB	*Command Token Word #2*															*LSB*
Prefix		*Sub-address*								*Spare*		*CRC-4*				
31	*30*	*29*	*28*	*27*	*26*	*25*	*24*	*23*	*22*	*21*	*20*	*19*	*18*	*17*	*16*	

'0'	*'1'*	*SA7*	*SA6*	*SA5*	*SA4*	*SA3*	*SA2*	*SA1*	*SA0*	*'1'*	*'1'*	*CRC3*	*CRC 2*	*CRC1*	*CRC0*

- Prefix and spare

The prefix bits are transmitted initially. In the command word#1 and #2 the prefix and spare bits have fixed value in the current implementation, these are reserved bits. The spislave receives them and use it for validating the token. If an invalid prefix and spare bits are received then Status illegal command (SIC) status bit is enabled and also transmitted to master as part of the next response token.

- Message Length

The number of payload words that will be transmitted in the current message. The number should not include the command token and the CRC checksum appended at the end of the message.

- Sub-address

This field provide additional sub-address location for write and read commands.

- CRC-4

The final four bits of the command token consist of a checksum for all the previous command token bits transmitted in this message. The CRC-4 should be computed for the following 28 bits, Command word #1 (16bits, MSB first sent to the CRC generator) and Command word #2 (excluding this CRC-4 field) (12bits, MSB first sent to the CRC generator). The Prefix and Spare fields are included in the CRC calculation. The generator polynomial used is $X^4 + X + 1$. In this SPI slave receiving end the CRC-4 is calculated internally for the received command token, if the calculated CRC-4 does not match the expected value (this field) the corresponding command token is discarded and message error status is enabled and transmitted to master as part of the next response token.

- Payload data

The payload consist of the data need to be transferred from the master to slave. Depending on the command executed the master must include valid data or dummy information in the form of string of zeros. For example the write command have the data to be written as the payload but the read command have dummy information in the form of string of zeros.

- Payload CRC

When a valid payload is delivered in the payload data section of the message a Payload CRC (CRC-16) must be included at the end of the message. The generator polynomial used is $x^{16} + x^{15} + x^2 + 1$. When dummy information in the form of string of zeros is included then no Payload CRC need to be attached then the payload CRC field must be all zero (0X0000). In the SPI slave receiving end the CRC-16 is calculated internally for the received payload data, if the calculated CRC-16 does not match the expected value (this field) the corresponding operation with respect to the command is not performed and message error status is enabled and transmitted to master as part of the next response token.

103.5.2 Command Code

The command code specify the operating instruction for the receiving slave. The detailed explanation of each command code and its implementation are explained in the table below.

- Reset command

Code	*Command*	*Length*	*Sub-address*	*Payload*	*Description*
0x00	*RESET_SPI*	*0x00*	*0x00*	*None*	*This command will reset all the spi slave device registers to the default value except the time registers (TIME1, TIME2) and core enable registers (ENN and ENR).*

The RESET_SPI command resets the SPI slave device to a power up initialized state. The SPI slave resets the system only if it received a valid command. If the prefix and spare bits does not match or if the calculated CRC-4 does not match the expected value then the RESET_SPI command is discarded.

- Time synchronization command

Code	*Command*	*Length*	*Sub-address*	*Payload*	*Description*
0x07	*SYNCH*	*0x04*	*0x00*	*MOSI:<SYNC1><SYNC2><SYNC3><SYNC4><CRC-16>* *MISO: <all zeros>*	*The master must transmit the SYNC command token followed by payload words containing synchronization information for it. These words are copied inside dedicated registers implemented in the SPI slave device after validation.*

The time register is of 64 bit in width, the most significant time is transferred first in SYNC1 followed by SYNC2, SYNC3 and SYNC4. The time register roll over when its maximum count is reached. The time is synchronised only when all the words are received and also the command token CRC-4 and data CRC-16 must be valid. All bits are zero at reset. The RESET_SPI does not reset the time register.

- Time increment command

Code	*Command*	*Length*	*Sub-address*	*Payload*	*Description*
0x08	*TICK*	*0x00*	*Used as index for increment.*	*None*	*This command is used to advance the timing synchronization register available in the SPI slave device (same register used for the SYNC command).*

A valid command increments the implemented time register. The sub address field specify from which bit the time register must increment.

- Read back sent command

Code	*Command*	*Length*	*Sub-address*	*Payload*	*Description*
0x0A	*READBACK_CMD*	*0x02*	*0x00*	*MOSI: <all zeros>* *MISO:<CMDTOKEN><CRC-16>*	*The command can be used to verify the correct reception of the previous command. Upon reception of the command the slave respond with the previous command token.*

The SPI slave device after receiving the READBACK_CMD send the previous command token transmitted by the SPI master. This command is useful only when some other command (other than RESET_SPI) was previously transmitted. If the previous command is RESET_SPI, the SPI master only receives zeros in the payload section of this command.

- Write command

Code	Command	Length	Sub-address	Payload	Description
0x0D	WRITE_SA	Number of words to be written, N	SA	MOSI:<DW1> <DW2> …<DWN> <CRC-16> MISO: <all zeros>	The command is used to write a certain number of data words into a slave specific Sub Address. Dedicated field of the command token select the payload length and the target SA.

When a valid WRITE_SA command is received the payload data is stored at the address specified. The address for writing the data is calculated by using the write address register (CONFIG_WRITE), and sub-address. The CRC-16 is calculated for received words and compared with the received payload CRC, if a data CRC error is detected then message error status is enabled and transmitted to master as part of the next response token.

- Read command

Code	Command	Length	Sub-address	Payload	Description
0x0E	READ_SA	Number of words to be read, N	SA	MOSI: <all zeros> MISO:<DW1> <DW2> …<DWN> <CRC-16>	The command is used to read a certain number of data words into a slave specific Sub Address. Dedicated field of the command token select the payload length and the target SA.

When a valid READ_SA command is received the payload data is transferred from the address specified. The address for reading the data is calculated by using the read address register (CONFIG_READ), and sub-address. The CRC-16 is calculated for transmitted words and sent as payload CRC by the slave device.

- Configure address commands

Code	Command	Length	Sub-address	Payload	Description
0x20	CONFIGWRITE_ADDR	0x02	0x00	MOSI:<CW1><CW2> <CRC-16> MISO: <all zeros>	The command can be used to notify the slave about the address to which the data from the master is written, used for WRITE_SA command.
0x21	CONFIG READ_ADDR	0x02	0x00	MOSI:<CR1> <CR2> <CRC-16> MISO: <all zeros>	The command can be used to notify the slave about the address from which the data to the master is read, used for READ_SA command.

Dedicated registers for write address and read address is implemented, these registers takes value from this command. The purpose of this register is to access upto 32 bits of address space. The most significant word CW1 (or CR1) contains the most significant bytes of the target address.

- Redundancy commands

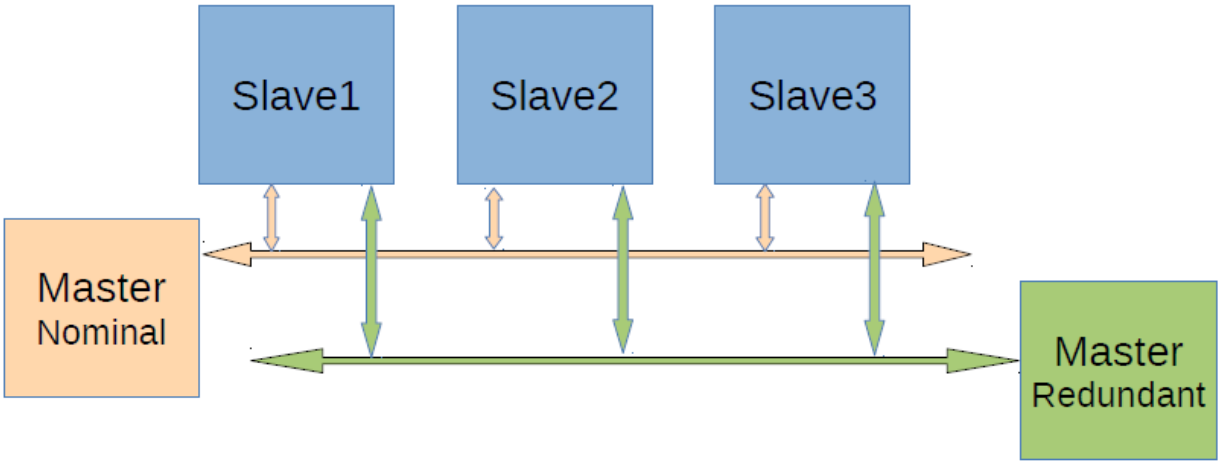


Figure 274. Redundant system

Code	*Command*	*Length*	*Sub-address*	*Payload*	*Description*
0x24	*ACTIVATE*	*0x00*	*0x00*	*None*	*The command is used to activate the other slave interface. This command cannot activate the interface in which it is receiving this command.*

Code	*Command*	*Length*	*Sub-address*	*Payload*	*Description*
0x25	*DEACTIVATE*	*0x00*	*0x00*	*None*	*The command is used to deactivate the other slave interface. This command cannot deactivate the interface in which it is receiving this command.*

The SPI Slave device has two dedicated interfaces for two masters. The masters can send to its corresponding slave interface to activate or deactivate the other SPI interface. The master device cannot activate or deactivate the same ports on which it is connected, it can only activate or deactivate the other ports.

Initially both the SPI port interfaces are enabled to receive commands, when the communication between the nominal master and slave interface fails then the redundant master can deactivate the nominal interface using its dedicated redundant interface. The redundant master can also activate the nominal interface.

An example switchover scenario from nominal to redundant interface is described in the following text.

The nominal master communicates with its dedicated interface to a slave device, a fault occurred can be detected by the master using several options,

The status received by the master have invalid values (using the response token),

The Read back command sent does not provide appropriate values in the received payload,

Error bits are enabled in the status received by the master (using the response token),

Based on any of the above mentioned fault detection methods the master can send deactivate command in the redundant interface to deactivate the nominal interface of the slave. The master can send Read back sent commands (using redundant) to check if the previous deactivate command was received by the slave and can check the status of the response token as well. After conforming a proper communication has been established the master can use the redundant interface to perform its normal operations.

- Others

Code	*Command*	*Length*	*Sub-address*	*Payload*	*Description*
All others	*N/A*	*0x00*			*These command codes are currently not implemented and their use is reserved for future. Upon reception of one of these codes the slave discard the incoming data.*

Any other commands which are not implemented is received then the command token is discarded and Status illegal command (SIC) bit is enabled and also transmitted to master as part of the next response token.

103.5.3 Message Header -Response Token

The slave transmits a message header which consist of status of module and details of error occurred. The message header sent by SPI slave device is called response token which consist of two 16 bit words. The message header content details are explained below.

MSB	*Response Token Word #1*														*LSB*
Prefix		*Status*					*Spare*					*Module State*			
15	*14*	*13*	*12*	*11*	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
'1'	*'0'*	*STF*	*ME*	*AR*	*IC*	*‘0’*	*'0'*	*'0'*	*'0'*	*'0'*	*'0'*	*MS3*	*MS2*	*MS1*	*MS0*

*Table 1665.*Response word #1

MSB	*Response Token Word #2*														*LSB*
Prefix		*Data*	*Spare*									*CRC-4*			
31	*30*	*29*	*28*	*27*	*26*	*25*	*24*	*23*	*22*	*21*	*20*	*19*	*18*	*17*	*16*
'1'	*'0'*	*DNA*	*'0'*	*'0'*	*'1'*	*'1'*	*'1 '*	*'1'*	*'0'*	*'0'*	*'0'*	*CRC 3*	*CRC 2*	*CRC1*	*CRC0*

*Table 1666.*Response word #2

- Status bits

Bit	*Identifier*	*Type*	*Value*	*Description*	*Clear Condition*
13	*SPI_TERMINAL_FAULT*	*Error*	*‘0’=no fault* *‘1’=fault*	*The bit flag a SPI terminal fault condition.*	*According to the module current state.*

In SPI slave device this bit is enabled or disabled by SPI2 control register (STF) using APB.

Bit	Identifier	Type	Value	Description	Clear Condition
12	MESSAGE_ERROR	Error	'0'=no fault '1'=fault	This bit is utilized to indicate that the previous message received from the bus master has failed to pass the validity tests.	Always related to the previous command. Reception of a valid command will clear it (with a delay of one command).

This status bit is enabled when the received message fails to pass the command token and payload data CRC checks. The next valid command clears this status bit.

Bit	Identifier	Type	Value	Description	Clear Condition
11	ADDRESS_ERROR	Error	'0'=no fault '1'=fault	This bit flag an AMBA error occured while performing the previous command.	Always related to the previous command. Reception of a valid command will clear it (with a delay of one command)

The SPI slave device uses an AHB master to perform the memory read and write, this bit is enabled when an AHB error is reported.

Bit	Identifier	Type	Value	Description	Clear Condition
10	ILLEGAL_COMMAND	Error	'0'=no fault '1'=fault	This bit flag that the previous received command was not compatible with the SPI slave device.	Always related to the previous command. Reception of a valid command will clear it (with a delay of one command)

When the prefix and spare bits in the received command token do not match the intended value or an unimplemented command is received this status bit is enabled. The next valid command clears this status bit.

- Module state:

In the SPI slave device these bits are enabled or disabled by SPI2 control register (MODSTAT) using APB. These bits can be used by Software controlling the slave device to provide additional status to the master.

103.6 Redundancy

The SPI slave has a two SPI ports which can be interfaced using two different masters. Two SPI master capable of communicating individually to the respective port must be available inorder to achieve redundancy using this Dual-port SPI slave.The slave takes two sets of SPI interfaces (nominal and

redundant). The configuration registers available in the device is used to enable which interface to communicate and it is possible to use dedicated commands (using SPI 2 protocol) to activate and deactivate ports.

While using configuration registers to activate or deactivate ports, the complete control of activation and deactivation must be performed by the external unit, only one port must active at any time. If both enabled then both the SPI ports are open for communication which is not supported while using external configuration for redundancy. The system which initiates the communication should take responsibility for which lane to take (there must be dedicated SPI Masters available in the system to communicate with the respective slave). If both are disabled then no communication is possible. The Master (driver) must have two dedicated SPI Master to perform communication on each lane of the SPI bus.

When commands are used to control the ports, the device can receive commands from both the interfaces. By receiving from both the interfaces the slave device can deactivate a non-working interface. The intention is to keep only one bus active for normal operation but using the redundant bus to achieve switchover. The SPI protocol 2 implementation supports dedicated commands to achieve the activation and deactivation of interfaces.

In normal working case the SPI masters Nominal and redundant (using HW or SW) should make sure not to write at the same time to both lanes of dual-port SPI Slave (for example to make a transfer). The SW or HW can command the Redundant master only when it detects problem with the Nominal communication. For worst case lets say, the SPI masters Nominal (in error state babelling some command repeatedly), using the redundant port the Nominal lane can be switched off (switch over command using redundant port or external configuration), the slave takes the redundant port input, the SPI slave is designed to take the redundant port inputs when it is available rather than nominal input.

103.7 Registers

The core is programmed through registers mapped into APB address space.

*Table 1667.*APB registers

APB address offset	Register
0x00	Control register
0x04	Status register
0x08	Transmit register
0x0C	Nominal receive register
0x10	Redundant receive register
0x14	Interrupt enable register
0x18	Interrupt register
0x1C	Reserved
0x20	SPI2 control register
0x24	SPI2 time1 register
0x28	SPI2 time2 register
0x2C	SPI2 config address write register
0x30	SPI2 config address read register

103.7.1 Control Register

*Table 1668.*0x00 - CTRL - Control register

31 24	23-17	16	15-13	12 8	7	6	5	4	3	2	1	0
Key	R	OD	R	WLEN	IAMBA	CPHA	CPOL	REV	R	RESET	ENR	ENN
0	0	0	0	0x0F	0	0	0	1	0	0	1	1
w	r	rw	r	rw	rw	rw	rw	rw	r	rw	rw	rw

31	Safety code (KEY) - Must be 0x68 when writing, otherwise register write is ignored
23 : 17	RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.
16	Overrun detect (OD) - To detect overrun condition (also to trigger overrun interrupt) this bit must be enabled. Valid only for SPI protocol 0 and 1.
15 : 13	RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.
12 : 8	Word length (WLEN) - The value of this field determines the length in bits of a transfer on the SPI bus. Valid values are 0x03 to 0x1F Word length is WLEN+1, allows words of length 4-32 bits.
7	AMBA Interrupt enable (IAMBA) - If set, AMBA interrupt generation is enabled for the events that are individually maskable by the Interrupt enable (INTE) register
6	Clock phase (CPHA) - When CPHA is ‘0’ data will be read on the first transition of SCK. When CPHA is ‘1’ data will be read on the second transition of SCK.
5	Clock polarity (CPOL) - Determines the polarity (idle state) of the SCK clock.
4	Reverse data (REV) - When this bit is ‘0’ data is transmitted LSB first, when this bit is ‘1’ data is transmitted MSB first.
3	RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.
2	Reset (RESET) - Resets all the registers in the core except time registers (TIME1, TIME2) and core enable registers (ENN and ENR).
1	Enable redundant port transfer (ENR) - Enable bit for redundant port transfer. See section 5.6 for more information.
0	Enable nominal port transfer (ENN)- Enable bit for nominal port transfer. See section 5.6 for more information.

103.7.2 Status Register

*Table 1669.*0x04 - STAT - Status register

31 8	7	6	5	4	3 2	1	0
RESERVED	ATR	ATN	SAR	SIC	R	RR	RN
0	0	1	0	0	0	0	0
r	r	r	r	r	r	r	r

31 : 3 RESERVED

7 Active transmission in redundant port (ATR) - This bit provides the status of the redundant transmission port. Set based on the incoming activate and deactivate commands (active '1' else '0'). Valid only for SPI protocol 2 implementation.

6 Active transmission in nominal port (ATN) - This bit provides the status of the nominal transmission port. Set based on the incoming activate and deactivate commands (active '1' else '0'). Valid only for SPI protocol 2 implementation.

5 Status address error (SAR) - This bit gets set to '1' when an AMBA write or read access resulted in a error. A valid new command clears this status bit. Valid only for SPI protocol 2 implementation.

4 Status illegal command (SIC) - This bit gets set to '1' when an illegal command is received. A valid new command clears this status bit. Valid only for SPI protocol 2 implementation.

3 : 2 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

1 Received data nominal (RR) - This bit gets set to '1' each time a data is received in the redundant port. The bit gets set to '0' when the Redundant receive register is read.

0 Received data nominal (RN) - This bit gets set to '1' each time a data is received in the nominal port. The bit gets set to '0' when the Nominal receive register is read.

103.7.3 Transmit Register

*Table 1670.*0x08 - TDATA - Transmit register

31 0
TDATA
0
rw

31 : 0 Transmit data (TDATA) - The written data is transferred to the master device when appropriate conditions for CS and SCK are satisfied. The word to transmit should be written with its least significant bit at bit 0. Also note that only the number of bits need to be transferred from this register should match the word length register (WLEN). Valid only for SPI protocol 0 and 1.

103.7.4 Nominal Receive Register

*Table 1671.*0x0C - NRDATA - Nominal receive register

31 0
NRDATA
0
r

31 : 0 Nominal Receive data (NRDATA) - This register contains received data from the nominal port. Valid only for SPI protocol 0 and 1.

103.7.5 Redundant Receive Register

*Table 1672.*0x10 - RRDATA - Redundant receive register

31 0
RRDATA
0

*Table 1672.*0x10 - RRDATA - Redundant receive register

r

31 : 0 Redundant Receive data (RRDATA) - This register contains received data from the redundant port. Valid only for SPI protocol 0 and 1.

103.7.6 Interrupt Enable Register

*Table 1673.*0x14 - INTE- Interrupt enable register

31 24	23 9	8	7	6	5	4	3	2	1	0
Key	RESERVED	OVRE	WDE	AE	CRE	CWE	TICKE	SYNCE	RXRE	RXNE
0	0	0	0	0	0	0	0	0	0	0
w	r	rw	rw	rw	rw	rw	rw	rw	rw	rw

31 : 24 Safety code (KEY) - Must be 0x68 when writing, otherwise register write is ignored.

23 : 9 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

8 Overrun interrupt enable (OVRE) - If enabled an interrupt will be generated when overrun condition occurs for data reception. Valid only for SPI protocol 0 and 1.

7 Write data interrupt enable (WDE). Valid only for SPI protocol 2.

6 AMBA access error interrupt enable (AE). Valid only for SPI protocol 2.

5 Change in config read address interrupt enable (CRE). Valid only for SPI protocol 2.

4 Change in config write address interrupt enable (CWE). Valid only for SPI protocol 2.

3 Tick command received interrupt enable (TICKE). Valid only for SPI protocol 2.

2 Sync command received interrupt enable (SYNCE). Valid only for SPI protocol 2.

1 Data received in redundant port interrupt enable (RXRE).Valid only for SPI protocol 0 and 1.

0 Data received in nominal port interrupt enable (RXNE). Valid only for SPI protocol 0 and 1.

103.7.7 Interrupt Register

*Table 1674.*0x18- INT- Interrupt register

31 24	23 9	8	7	6	5	4	3	2	1	0
Key	RESERVED	OVR	WD	AI	CR	CW	TICK	SYNC	RXR	RXN
0	0	0	0	0	0	0	0	0	0	0
w	r	wc	wc	wc	wc	wc	wc	wc	wc	wc

31 : 24 Safety code (KEY) - Must be 0x68 when writing, otherwise register write is ignored.

23 : 9 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

8 Overrun interrupt (OVR) - An interrupt is generated when overrun condition occurs for data reception. (a received data must be read before the arrival of next data, if new data arrived before the Software could read the previously received data overrun condition is triggered). Valid only for SPI protocol 0 and 1.

7 Write data interrupt (WD). Valid only for SPI protocol 2.

6 AMBA access error interrupt (AI). Valid only for SPI protocol 2.

5 Change in config read address interrupt (CR). Valid only for SPI protocol 2.

4 Change in config write address interrupt (CW). Valid only for SPI protocol 2.

3 Tick command received interrupt (TICK). Valid only for SPI protocol 2.

2 Sync command received interrupt (SYNC). Valid only for SPI protocol 2.

1 Data received in redundant port interrupt (RXR).Valid only for SPI protocol 0 and 1.

0 Data received in nominal port interrupt (RXN). Valid only for SPI protocol 0 and 1.

103.7.8 SPI2 Control Register

*Table 1675.*0x20- SPI2C- SPI2 control register

31 24	23 8	7	6	5	4	3	2	1	0
Key	RESERVED	MODSTAT				RESERVED		STF	EN
0	0	0	0	0	0	0	0	0	1
w	r	rw	rw	rw	rw	r	r	rw	rw

31 : 24 Safety code (KEY) - Must be 0x68 when writing, otherwise register write is ignored.

23 : 8 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

7: 4 Module state (MODSTAT). The values in these bits are sent to the master via the response token. These are user configurable registers which can be set to ‘1’ or ‘0’. Valid only for SPI protocol 2.

3: 2 RESERVED (R) - Read as zero and should be written to zero to ensure forward compatibility.

1 SPI terminal failure (STF). This value in this bit is sent to the master via the response token. In order to intimate a terminal failure this bit can be written to ‘1’ through software. Valid only for SPI protocol 2.

0 Enable (EN). SPI protocol 2 enable bit. If set to ‘1’ the commands received from master are handled by the SPI 2 protocol handler in the core. If set to ‘0’ the data received and transfered are using the APB registers.

103.7.9 SPI2 Time1 Register

*Table 1676.*0x24 - TIME1 - SPI2 time1 register

31 0
TIME1
0x00000000
r

31 : 0 Time 1 register (TIME1) - Provides the most significant 32 bits of the time register. This is a status (read only) register, the contents of this register is a reflection of the time modified/incremented using the sync and tick command respectively.

103.7.10SPI2 Time2 Register

*Table 1677.*0x28 - TIME2 - SPI2 time2 register

31	0
TIME2	
0x00000000	
r	

31 : 0 Time 2 register (TIME2) - Provides the lower 32 bits of the time register. This is a status (read only) register, the contents of this register is a reflection of the time modified/incremented using the sync and tick command respectively.

103.7.11SPI2 Config Address Write Register

*Table 1678.*0x2C - CONFW - SPI2 config address write register

31	0
CONFW	
0x40000000	
r	

31 : 0 Configuration read address (CONFW) - Defines the base address for the memory area where the core is allowed to make accesses. This is a status (read only) register, the contents of this register can be modified by the configuration write address command.

103.7.12SPI2 Config Address Read Register

*Table 1679.*0x30 - CONFR - SPI2 config address read register

31	0
CONFR	
0x40000000	
r	

31 : 0 Configuration read address (CONFR) - Defines the base address for the memory area where the core is allowed to make accesses. This is a status (read only) register, the contents of this register can be modified by the configuration read address command.

103.8 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x0A7. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

103.9 Implementation

103.9.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

103.10 Configuration options

Table 1680 shows the configuration options of the core (VHDL generics).

*Table 1680.*Configuration options

Generic name	Function	Allowed range	Default
gPINDEX	APB slave index	0 - NAPBSLV-1	0
gHINDEX	AHB master index	0 - NAHBMST	0
gPADDR	ADDR field of the APB BAR	0 - 16#FFF#	0
gPMASK	MASK field of the APB BAR.	0 - 16#FFF#	16#FFF#
gPIRQ	Interrupt line driven by APB interface.	0 - NAHBIRQ-1	1
gSPI2	Implement SPI protocol 2	0 - 1	1
gCONFW	Default value for config write address register	0 - 16#FFFFFF#	16#400000#
gCONFR	Default value for config read address register	0 - 16#FFFFFF#	16#400000#
gOEPOL	Output enable polarity	0 - 1	0

103.11 Signal descriptions

Table 1681 shows the interface signals of the core (VHDL ports).

*Table 1681.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
AHBI	*	Input	AHB master input signals	-
AHBO	*	Output	AHB master output signals	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
SCK_N	N/A	Input	SPI clock line input Nominal	-
MOSI_N	N/A	Input	SPI data line input Nominal	-
SLVSEL_N	N/A	Input	SPI slave select output Nominal	Low
MISO_N	N/A	Output	SPI data line output Nominal	-
MISO_EN_N	N/A	Output	SPI data line output enable Nominal	**
SCK_R	N/A	Input	SPI clock line input Redundant	-
MOSI_R	N/A	Input	SPI data line input Redundant	-
SLVSEL_R	N/A	Input	SPI slave select output Redundant	Low
MISO_R	N/A	Output	SPI data line output Redundant	-
MISO_EN_R	N/A	Output	SPI data line output enable Redundant	**

* see GRLIB IP Library User's Manual
** depends on value of OEPOL VHDL generic.

103.12 Library dependencies

Table 1682 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1682.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	SPICOMP	Component, signals	Component declaration, SPI signal definitions
GAISLER	GRSPICOMP	Component, signals	Component declaration, SPI signal definitions

103.13 Instantiation

```
library  ieee;
use      ieee.std_logic_1164.all;

library  grlib, techmap;
use      grlib.amba.all;
use      grlib.devices.all;
use      grlib.stdlib.all;
use techmap.gencomp.all;
library  gaisler;
use gaisler.spicomp.all;
use gaisler.grspicomp.all;

entity grspislave_ex is
   port (
     rstn        : in  std_ulogic;
     clk         : in  std_ulogic;
     ahbmi       : in  ahb_mst_in_type;
     ahbmo       : out ahb_mst_out_type;
     apbi        : in  APB_Slv_In_Type;
     apbo        : out APB_Slv_Out_Type;
     -- SPI signals
     miso_n      : out std_ulogic;
     miso_en_n   : out std_ulogic;
     mosi_n      : in  std_ulogic;
     sck_n       : in  std_ulogic;
     slvsel_n    : in  std_ulogic;

     miso_r      : out std_ulogic;
     miso_en_r   : out std_ulogic;
     mosi_r      : in  std_ulogic;
     sck_r       : in  std_ulogic;
     slvsel_r    : in  std_ulogic);
end entity grspislave_ex;

architecture rtl of grspislave_ex is

  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector;
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector;

  signal nom_sck        :       std_ulogic;
  signal nom_miso       :       std_ulogic;
  signal nom_miso_en    :       std_ulogic;
  signal nom_mosi       :       std_ulogic;
  signal nom_slvsel     :       std_ulogic;

  signal red_sck        :       std_ulogic;
  signal red_miso       :       std_ulogic;
```

```
  signal red_miso_en    :       std_ulogic;
  signal red_mosi       :       std_ulogic;
  signal red_slvsel     :       std_ulogic;
  constant OEPOL : integer := padoen_polarity(padtech);

begin

     grspislave0: grspislave
        generic map (
           gHINDEX         => 4,
           gPINDEX         => 6,
           gPADDR          => 6,
           gPIRQ           => 6,
           gSPI2           => 1,
           gCONFW          => 16#400000#,
           gCONFR          => 16#400000#,
           gOEPOL          => OEPOL)
        port map (
          rstn             => rstn,
          clk              => clk,
          ahbmi            => ahbmi,
          ahbmo            => ahbmo(4),
          apbi             => apbi,
          apbo             => apbo(6),

          miso_n           => nom_miso,
          miso_en_n        => nom_miso_en,
          mosi_n           => nom_mosi,
          sck_n            => nom_sck,
          slvsel_n         => nom_slvsel,

          miso_r           => red_miso,
          miso_en_r        => red_miso_en,
          mosi_r           => red_mosi,
          sck_r            => red_sck,
          slvsel_r         => red_slvsel);

 --Nominal
   sck_p1pad : inpad generic map (tech => padtech)
      port map (sck_n, nom_sck);

   mosi_p1pad : inpad generic map (tech => padtech)
      port map (mosi_n, nom_mosi);

   miso_p1pad : toutpad generic map (tech => padtech, oepol => OEPOL)
      port map (miso_n, nom_miso, nom_miso_en);

   cs_p1pad : inpad generic map (tech => padtech)
      port map (slvsel_n, nom_slvsel);

--Redundant
   sck_p2pad : inpad generic map (tech => padtech)
      port map (sck_r, red_sck);

   mosi_p2pad : inpad generic map (tech => padtech)
      port map (mosi_r, red_mosi);

   miso_p2pad : toutpad generic map (tech => padtech, oepol => OEPOL)
      port map (miso_r, red_miso, nom_miso_en);

   cs_p2pad : inpad generic map (tech => padtech)
      port map (slvsel_r, red_slvsel);
end architecture rtl;
```

104 SRCTRL- 8/32-bit PROM/SRAM Controller

104.1 Overview

SRCTRL is an 8/32-bit PROM/SRAM/IO controller that interfaces external asynchronous SRAM, PROM and I/O to the AMBA AHB bus. The controller can handle 32-bit wide SRAM and I/O, and either 8- or 32-bit PROM.

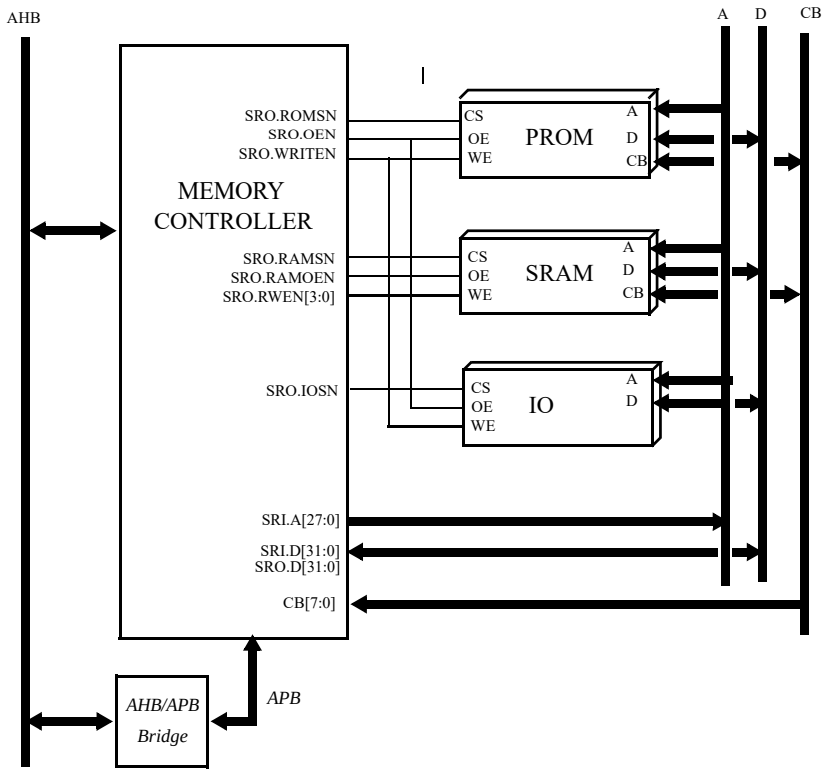


Figure 275. 8/32-bit PROM/SRAM/IO controller

The controller is configured through VHDL-generics to decode three address ranges: PROM, SRAM and I/O area. By default PROM area is mapped into address range 0x0 - 0x00FFFFFF, the SRAM area is mapped into address range 0x40000000 - 0x40FFFFFF, and the I/O area is mapped to 0x20000000 - 0x20FFFFFF.

One chip select is decoded for the I/O area, while SRAM and PROM can have up to four and two select signals respectively. The controller generates both a common write-enable signal (WRITEN) as well as four byte-write enable signals (WREN). If the SRAM uses a common write enable signal the controller can be configured to perform read-modify-write cycles for byte and half-word write accesses. Number of waitstates is separately configurable for the three address ranges.

A single write-enable signal is generated for the PROM area (WRITEN), while four byte-write enable signals (RWEN[3:0]) are provided for the SRAM area. If the external SRAM uses common write enable signal, the controller can be configured to perform read-modify-write cycles for byte and half-word write accesses.

Number of waitstates is configurable through VHDL generics for both PROM and SRAM areas.

A signal (BDRIVE) is provided for enabling the bidirectional pads to which the data signals are connected. The oepol generic is used for selecting the polarity of these enable signals. If output delay is an issue, a vectored output enable signal (VBDRIVE) can be used instead. In this case, each pad has

its own enable signal driven by a separate register. A directive is placed on these registers so that they will not be removed during synthesis (if the output they drive is used in the design).

104.1.1 Endianness

The core is designed for big-endian systems.

104.2 8-bit PROM access

The SRCTRL controller can be configured to access a 8-bit wide PROM. The data bus of external PROM should be connected to the upper byte of the 32-bit data bus, i.e. D[31:24]. The 8-bit mode is enabled with the prom8en VHDL generic. When enabled, read accesses to the PROM area will be done in four-byte bursts. The whole 32-bit word is then presented on the AHB data bus. Writes should be done one byte at a time and the byte should always be driven on bit 31-24 on the AHB data bus independent of the byte address.

It is possible to dynamically switch between 8- and 32-bit PROM mode using the BWIDTH[1:0] input signal. When BWIDTH is “00” then 8-bit mode is selected. If BWIDTH is “10” then 32-bit mode is selected. Other BWIDTH values are reserved for future use.

SRAM access is not affected by the 8-bit PROM mode.

104.3 PROM/SRAM waveform

Read accesses to 32-bit PROM and SRAM has the same timing, see figure below.

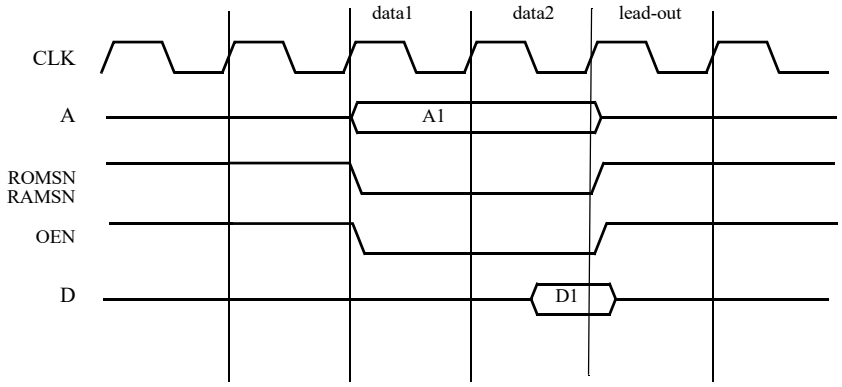


Figure 276. 32-bit PROM/SRAM/IO read cycle

The write access for 32-bit PROM and SRAM can be seen below.

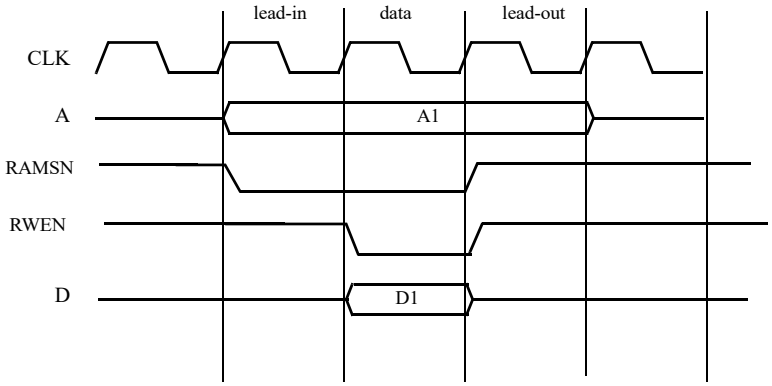


Figure 277. 32-bit PROM/SRAM/IO write cycle

If waitstates are configured through the VHDL generics, one extra data cycle will be inserted for each waitstate in both read and write cycles.

104.4 Burst cycles

To improve the bandwidth of the memory bus, accesses to consecutive addresses can be performed in burst mode. Burst transfers will be generated when the memory controller is accessed using an AHB burst request. These includes instruction cache-line fills and burst from DMA masters. The timing of a burst cycle is identical to the programmed basic cycle with the exception that during read cycles, the lead-out cycle will only occurs after the last transfer.

104.5 Registers

The core does not implement any user programmable registers.

All configuration is done through the VHDL generics.

104.6 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x008. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

104.7 Implementation

104.7.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers. The registers driving external chip select, output enable and output enables for the data bus have asynchronous reset.

104.8 Configuration options

Table 1684 shows the configuration options of the core (VHDL generics).

*Table 1683.*Configuration options

Generic	Function	Allowed range	Default
hindex	AHB slave index	1 - NAHBSLV-1	0
romaddr	ADDR field of the AHB BAR0 defining PROM address space. Default PROM area is 0x0 - 0xFFFFFF.	0 - 16#FFF#	16#000#
rommask	MASK field of the AHB BAR0 defining PROM address space.	0 - 16#FFF#	16#FF0#
ramaddr	ADDR field of the AHB BAR1 defining SRAM address space. Default SRAM area is 0x40000000-0x40FFFFFF.	0 - 16#FFF#	16#400#
rammask	MASK field of the AHB BAR1 defining SRAM address space.	0 -16#FFF#	16#FF0#
ioaddr	ADDR field of the AHB BAR2 defining IO address space. Default IO area is 0x20000000-0x20FFFFFF.	0 - 16#FFF#	16#200#
iomask	MASK field of the AHB BAR2 defining IO address space.	0 -16#FFF#	16#FF0#
ramws	Number of waitstates during access to SRAM area	0 - 15	0
romws	Number of waitstates during access to PROM area	0 - 15	2
iows	Number of waitstates during access to IO area	0 - 15	2
rmw	Enable read-modify-write cycles.	0 - 1	0
prom8en	Enable 8 - bit PROM accesses	0 - 1	0
oepol	Polarity of bdrive and vbdrive signals. 0=active low, 1=active high	0 - 1	0
srbanks	Set the number of SRAM banks	1 - 5	1
banksz	Set the size of bank 1 - 4. 0 = 8 Kbyte, 1 = 16 Kbyte, ... , 13 = 64Mbyte.	0 - 13	13
romasel	address bit used for PROM chip select.	0 - 27	19

104.9 Signal description

Table 1683 shows the interface signals of the core (VHDL ports).

*Table 1684.*Signal descriptions

Signal name	Field	Type	Function	Polarity
CLK	N/A	Input	Clock	-
RST	N/A	Input	Reset	Low
SRI	DATA[31:0]	Input	Memory data	High
	BRDYN	Input	Not used	-
	BEXCN	Input	Not used	-
	WRN[3:0]	Input	Not used	-
	BWIDTH[1:0]	Input	BWIDTH=”00” => 8-bit PROM mode BWIDTH=”10” => 32-bit PROM mode	-
	SD[31:0]	Input	Not used	-

*Table 1684.*Signal descriptions

Signal name	Field	Type	Function	Polarity
SRO	ADDRESS[27:0]	Output	Memory address	High
	DATA[31:0]	Output	Memory data	High
	RAMSN[4:0]	Output	SRAM chip-select	Low
	RAMOEN[4:0]	Output	SRAM output enable	Low
	IOSN	Output	Not used. Driven to '1' (inactive)	Low
	ROMSN[1:0]	Output	PROM chip-select	Low
	RAMN	Output	Common SRAM chip-select. Asserted when one of the RAMSN[4:0] signals is asserted.	Low
	ROMN	Output	Common PROM chip-select. Asserted when one of the ROMSN[1:0] signals is asserted.	Low
	OEN	Output	Output enable	Low
	WRITEN	Output	Write strobe	Low
	WRN[3:0]	Output	SRAM write enable: WRN[0] corresponds to DATA[31:24], WRN[1] corresponds to DATA[23:16], WRN[2] corresponds to DATA[15:8], WRN[3] corresponds to DATA[7:0].	Low
	MBEN[3:0]	Output	Byte enable: MBEN[0] corresponds to DATA[31:24], MBEN[1] corresponds to DATA[23:16], MBEN[2] corresponds to DATA[15:8], MBEN[3] corresponds to DATA[7:0].	Low
	BDRIVE[3:0]	Output	Drive byte lanes on external memory bus. Controls I/O-pads connected to external memory bus: BDRIVE[0] corresponds to DATA[31:24], BDRIVE[1] corresponds to DATA[23:16], BDRIVE[2] corresponds to DATA[15:8], BDRIVE[3] corresponds to DATA[7:0].	Low/High[2]
	VBDRIVE[31:0]	Output	Identical to BDRIVE but has one signal for each data bit. Every index is driven by its own register. This can be used to reduce the output delay.	Low/High[2]
	READ	Output	Read strobe	High
	SA[14:0]	Output	Not used	High
AHBSI	1)	Input	AHB slave input signals	-
AHBSO	1)	Output	AHB slave output signals	-
SDO	SDCASN	Output	Not used. All signals are driven to inactive state.	Low

1) See GRLIB IP Library User's Manual

2) Polarity is selected with the oepol generic

104.10 Library dependencies

Table 1685 shows libraries used when instantiating the core (VHDL libraries).

*Table 1685.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AHB signal definitions
GAISLER	MEMCTRL	Signals, component	Memory bus signals definitions, component declaration

104.11 Component declaration

The core has the following component declaration.

```
component srctrl
  generic (
    hindex  : integer := 0;
    romaddr : integer := 0;
    rommask : integer := 16#ff0#;
    ramaddr : integer := 16#400#;
    rammask : integer := 16#ff0#;;
    ioaddr  : integer := 16#200#;
    iomask  : integer := 16#ff0#;
    ramws   : integer := 0;
    romws   : integer := 2;
    iows    : integer := 2;
    rmw     : integer := 0;-- read-modify-write enable
    prom8en : integer := 0;
    oepol   : integer := 0;
    srbanks : integer range 1 to 5 := 1;
    banksz  : integer range 0 to 13:= 13;
    romasel : integer range 0 to 27:= 19
  );
  port (
    rst     : in  std_ulogic;
    clk     : in  std_ulogic;
    ahbsi   : in  ahb_slv_in_type;
    ahbso   : out ahb_slv_out_type;
    sri     : in  memory_in_type;
    sro     : out memory_out_type;
    sdo     : out sdctrl_out_type
  );
end component;
```

104.12 Instantiation

This example shows how the core can be instantiated.

The example design contains an AMBA bus with a number of AHB components connected to it including the memory controller. The external memory bus is defined on the example designs port map and connected to the memory controller. System clock and reset are generated by GR Clock Generator and Reset Generator.

Memory controller decodes default memory areas: PROM area is 0x0 - 0xFFFFFF and SRAM area is 0x40000000 - 0x40FFFFF. The 8-bit PROM mode is disabled. Two SRAM banks of size 64 Mbyte are used and the fifth chip select is disabled.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
use grlib.tech.all;
library gaisler;
use gaisler.memctrl.all;
```

```
use gaisler.pads.all;   -- used for I/O pads
use gaisler.misc.all;
library esa;
use esa.memoryctrl.all;

entity srctrl_ex is
  port (
    clk : in std_ulogic;
    resetn : in std_ulogic;
    pllref : in  std_ulogic;

    -- memory bus
    address  : out   std_logic_vector(27 downto 0); -- memory bus
    data     : inout std_logic_vector(31 downto 0);
    ramsn    : out   std_logic_vector(4 downto 0);
    ramoen   : out   std_logic_vector(4 downto 0);
    rwen     : inout std_logic_vector(3 downto 0);
    romsn    : out   std_logic_vector(1 downto 0);
    iosn     : out   std_logic;
    oen      : out   std_logic;
    read     : out   std_logic;
    writen   : inout std_logic;
    brdyn    : in    std_logic;
    bexcn    : in    std_logic;
    modesel  : in    std_logic; --PROM width select
-- sdram i/f
    sdcke    : out std_logic_vector ( 1 downto 0);  -- clk en
    sdcsn    : out std_logic_vector ( 1 downto 0);  -- chip sel
    sdwen    : out std_logic;                       -- write en
    sdrasn   : out std_logic;                       -- row addr stb
    sdcasn   : out std_logic;                       -- col addr stb
    sddqm    : out std_logic_vector (7 downto 0);  -- data i/o mask
    sdclk    : out std_logic;                       -- sdram clk output
    sa       : out std_logic_vector(14 downto 0); -- optional sdram address
    sd       : inout std_logic_vector(63 downto 0) -- optional sdram data
       );
end;

architecture rtl of srctrl_ex is

  -- AMBA bus (AHB and APB)
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);
  signal ahbsi : ahb_slv_in_type;
  signal ahbso : ahb_slv_out_vector := (others => ahbs_none);
  signal ahbmi : ahb_mst_in_type;
  signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);

  -- signals used to connect memory controller and memory bus
  signal memi : memory_in_type;
  signal memo : memory_out_type;

  signal sdo : sdctrl_out_type;

  signal wprot : wprot_out_type;  -- dummy signal, not used
  signal clkm, rstn : std_ulogic; -- system clock and reset

-- signals used by clock and reset generators
  signal cgi : clkgen_in_type;
  signal cgo : clkgen_out_type;

  signal gnd : std_ulogic;

begin

  -- AMBA Components are defined here ...


  -- Clock and reset generators
  clkgen0 : clkgen generic map (clk_mul => 2, clk_div => 2, sdramen => 1,
                                tech => virtex2, sdinvclk => 0)
```

```
  port map (clk, gnd, clkm, open, open, sdclk, open, cgi, cgo);

  cgi.pllctrl <= "00"; cgi.pllrst <= resetn; cgi.pllref <= pllref;

  rst0 : rstgen
  port map (resetn, clkm, cgo.clklock, rstn);


  -- Memory controller
srctrl0 : srctrl generic map (rmw => 1, prom8en => 0, srbanks => 2,
  banksz => 13, ramsel5 => 0)
    port map (rstn, clkm, ahbsi, ahbso(0), memi, memo, sdo);


  -- I/O pads driving data memory bus data signals
  datapads : for i in 0 to 3 generate
      data_pad : iopadv generic map (width => 8)
      port map (pad => data(31-i*8 downto 24-i*8),
                o => memi.data(31-i*8 downto 24-i*8),
                en => memo.bdrive(i),
                i => memo.data(31-i*8 downto 24-i*8));
  end generate;

  -- Alternative I/O pad instantiation with vectored enable instead
  datapads : for i in 0 to 3 generate
      data_pad : iopadvv generic map (width => 8)
      port map (pad => data(31-i*8 downto 24-i*8),
                o => memi.data(31-i*8 downto 24-i*8),
                en => memo.bdrive(31-i*8 downto 24-i*8),
                i => memo.data(31-i*8 downto 24-i*8));
  end generate;

  -- connect memory controller outputs to entity output signals
  address <= memo.address; ramsn <= memo.ramsn; romsn <= memo.romsn;
  oen <= memo.oen; rwen <= memo.wrn; ramoen <= memo.ramoen;
  writen <= memo.writen; read <= memo.read; iosn <= memo.iosn;
  sdcke <= sdo.sdcke; sdwen <= sdo.sdwen; sdcsn <= sdo.sdcsn;
  sdrasn <= sdo.rasn; sdcasn <= sdo.casn; sddqm <= sdo.dqm;

end;
```

105 SSRCTRL- 32-bit SSRAM/PROM Controller

105.1 Overview

The memory controller (SSRCTRL) is an 32-bit SSRAM/PROM/IO controller that interfaces external Synchronous pipelined SRAM, PROM, and I/O to the AMBA AHB bus. The controller acts as a slave on the AHB bus and has a configuration register accessible through an APB slave interface. Figure 278 illustrates the connection between the different devices.

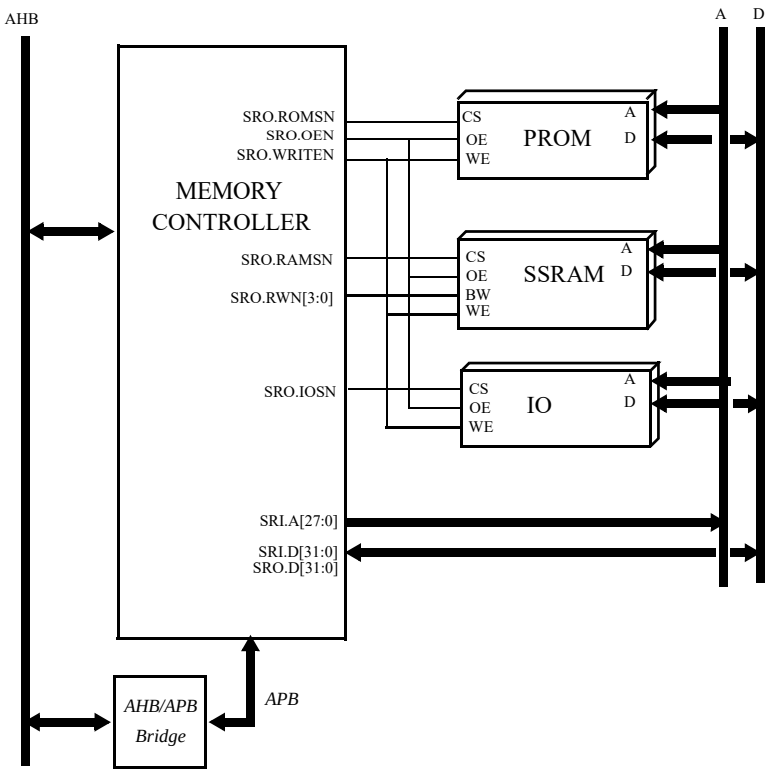


Figure 278. 32-bit SSRAM/PROM/IO controller

The controller is configured by VHDL-generics to decode three address ranges: PROM, SSRAM and I/O area. By default PROM area is mapped into address range 0x0 - 0x00FFFFFF; the SSRAM area is mapped into address range 0x40000000 - 0x40FFFFFF; and the I/O area is mapped to 0x20000000 - 0x20FFFFFF.

One chip select is generated for each of the address areas. The controller generates both a common write-enable signal (WRITEN) as well as four byte-write enable signals (WRN). The byte-write enable signal enables byte and half-word write access to the SSRAM.

A signal (BDRIVE) is provided for enabling the bidirectional pads to which the data signals are connected. The oepol generic is used to select the polarity of these enable signals. If output delay is an issue, a vectored output enable signal (VBDRIVE) can be used instead. In this case, each pad has its own enable signal driven by a separate register. A directive is placed on these registers so that they will not be removed during synthesis (in case the output they drive is used in the design).

The SSRCTRL conteoller can optionally support 16-bit PROM/IO devices. This is enabled through the BUS16 generic. A 32-bit access to the PROM or IO area will be translated into two 16-bit accesses with incrementing address.

105.1.1 Endianness

The core is designed for big-endian systems.

105.2 SSRAM/PROM waveform

Because the SSRAM (Synchronous pipelined SRAM) has a pipelined structure, the data output has a latency of three clock cycles. The pipelined structure enables a new memory operation to be issued each clock cycle. Figure 278 and figure 279 show timing diagrams for the SSRAM read and write accesses.

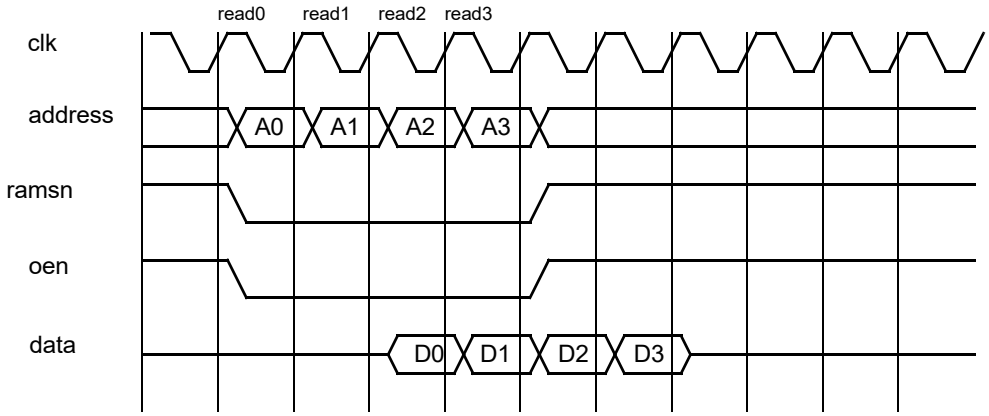


Figure 279. 32-bit SSRAM read cycle

As shown in the figure above, the controller always perform a burst read access to the memory. This eliminates all data output latency except for the first word when a burst read operation is executed.

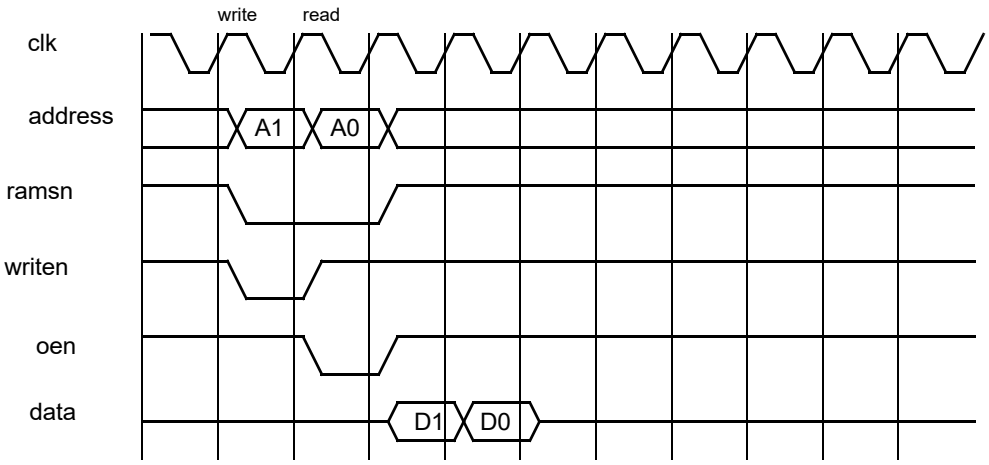


Figure 280. 32-bit SSRAM write cycle

A write operation takes three clock cycles. On the rising edge of the first clock cycle, the address and control signals are latched into the memory. On the next rising edge, the memory puts the data bus in high-impedance mode. On the third rising edge the data on the bus is latched into the memory and the write is complete. The controller can start a new memory (read or write) operation in the second clock cycle. In figure 280 this is illustrated by a read operation following the write operation.

Due to the memory automatically putting the data bus in high-impedance mode when a write operation is performed, the output-enable signal (OEN) is held active low during all SSRAM accesses (including write operations).

105.2.1 PROM and IO access

For the PROM and I/O operations, a number of waitstates can be inserted to increase the read and write cycle. The number of waitstates can be configured separately for the I/O and PROM address ranges, through a programmable register mapped into the APB address space. After a reset the wait-states for PROM area is set to its maximum (15). Figure 281 and figure 282 show timing diagrams for the PROM read and write accesses.

Read accesses to 32-bit PROM and I/O has the same timing, see figure 281

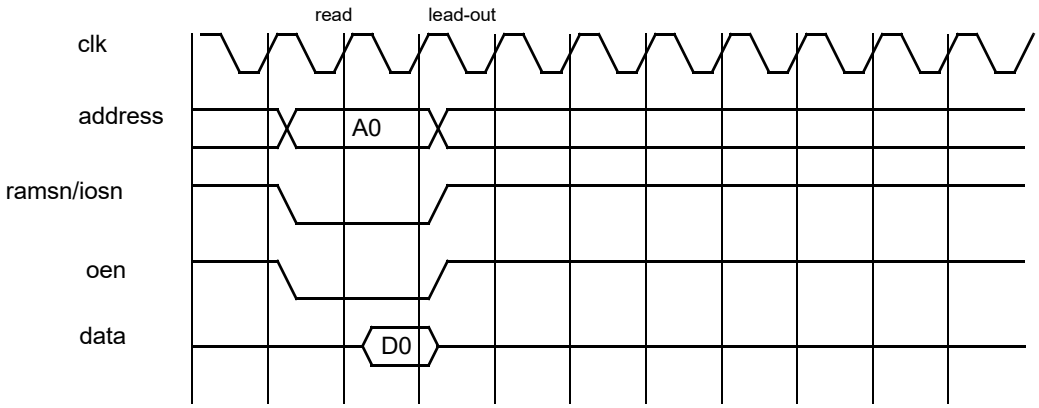


Figure 281. 32-bit PROM/IO read cycle

The write access for 32-bit PROM and I/O can be seen in figure 282

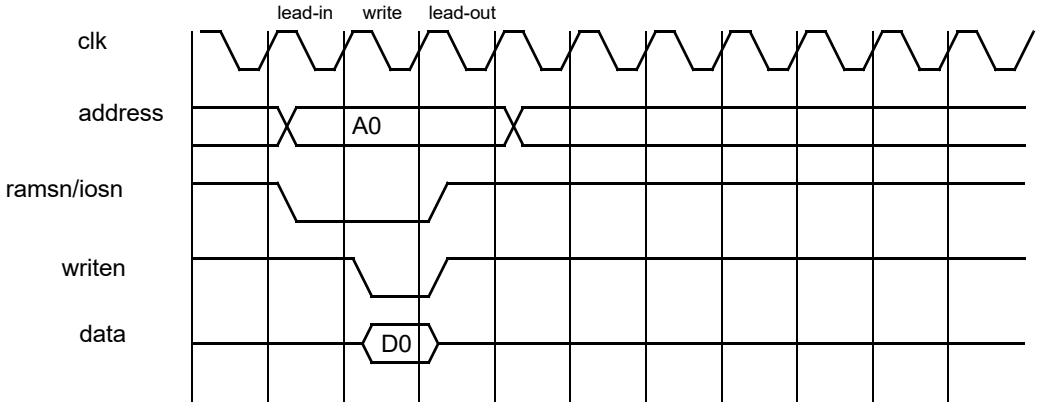


Figure 282. 32-bit PROM/IO write cycle

The SSRCTRL conteoller can optionally support 16-bit PROM/IO devices. This is enabled through the BUS16 generic. A 32-bit access to the PROM or IO area will be translated into two 16-bit accesses with incrementing address. A 16-bit access will result in one bus access only. 8-bit accesses are not allowed.

16-bit PROM/IO operation is enabled by writing “01” to the romwidth field in SSRAM control register. At reset, the romwidth field is set by the MEMI.BWIDTH input signal.

Read accesses to 16-bit PROM and I/O has the same timing, see figure 283

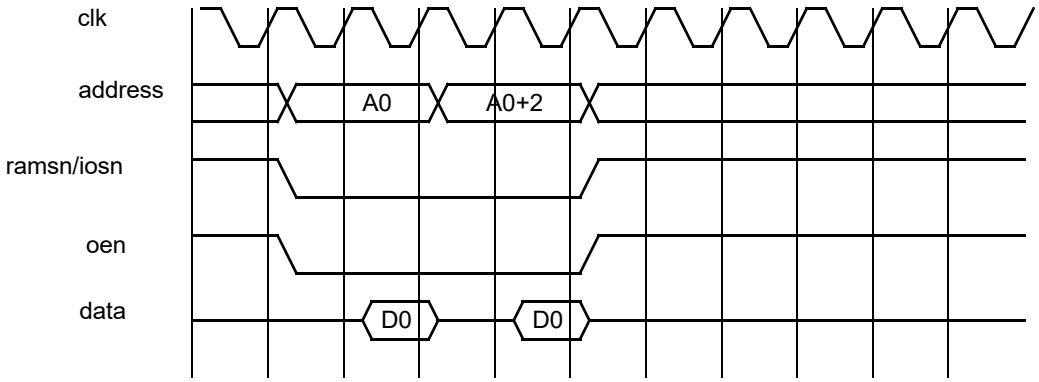


Figure 283. 32-bit PROM/IO read cycle in 16-bit mode

The write access for 32-bit PROM and I/O can be seen in figure 284

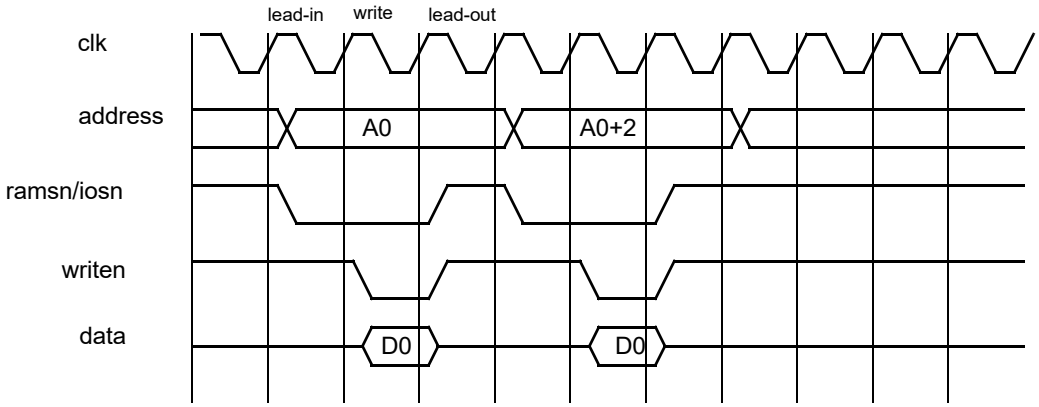


Figure 284. 32-bit PROM/IO write cycle in 16-bit mode

105.3 Registers

The core is programmed through registers mapped into APB address space.

*Table 1686.*SSRAM controller registers

APB address offset	Register
0x00	Memory configuration register

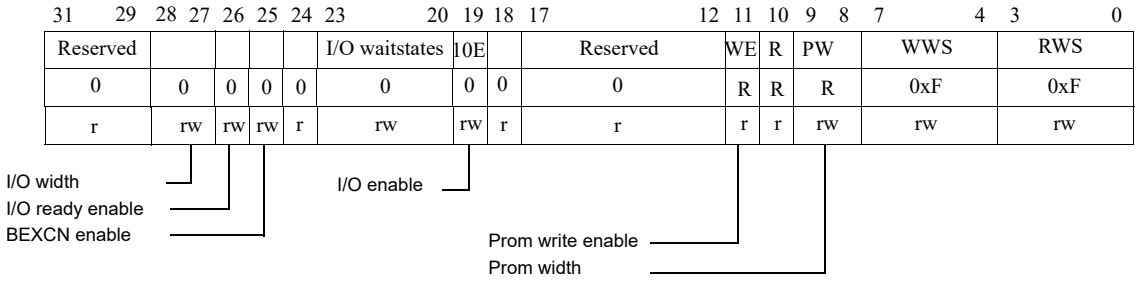


Figure 285. Memory configuration register

[3:0]: Prom read waitstates. Defines the number of waitstates during prom read cycles (“0000”=0, “0001”=1,... “1111”=15).
[7:4]: Prom write waitstates. Defines the number of waitstates during prom write cycles (“0000”=0, “0001”=1,... “1111”=15).
[9:8]: Prom width. Defines the data with of the prom area (“01”=16, “10”=32).
[10]: Reserved
[11]: Prom write enable. If set, enables write cycles to the prom area. NOT USED.
[17:12]: Reserved
[19]: I/O enable. If set, the access to the memory bus I/O area are enabled. NOT USED.
[23:20]: I/O waitstates. Defines the number of waitstates during I/O accesses (“0000”=0, “0001”=1, “0010”=2,..., “1111”=15).
[25]: Bus error (BEXCN) enable. NOT USED.
[26]: Bus ready (BRDYN) enable. NOT USED.
[28:27]: I/O bus width. Defines the data with of the I/O area (“01”=16, “10”=32).

During power-up (reset), the PROM waitstates fields are set to 15 (maximum) and the PROM bus width is set to the value of MEMI.BWIDTH. All other fields are initialized to zero.

105.4 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x00A. For description of vendor and device identifiers see GRLIB IP Library User’s Manual.

105.5 Configuration options

Table 1687 shows the configuration options of the core (VHDL generics).

*Table 1687.*Configuration options

Generic	Function	Allowed range	Default
hindex	AHB slave index	1 - NAHBSLV-1	0
pindex	APB slave index	0 - NAPBSLV-1	0
romaddr	ADDR field of the AHB BAR0 defining PROM address space. Default PROM area is 0x0 - 0xFFFFFF.	0 - 16#FFF#	16#000#
rommask	MASK field of the AHB BAR0 defining PROM address space.	0 - 16#FFF#	16#FF0#
ramaddr	ADDR field of the AHB BAR1 defining RAM address space. Default RAM area is 0x40000000-0x40FFFFFF.	0 - 16#FFF#	16#400#
rammask	MASK field of the AHB BAR1 defining RAM address space.	0 -16#FFF#	16#FF0#
ioaddr	ADDR field of the AHB BAR2 defining IO address space. Default IO area is 0x20000000-0x20FFFFFF.	0 - 16#FFF#	16#200#
iomask	MASK field of the AHB BAR2 defining IO address space.	0 -16#FFF#	16#FF0#
paddr	ADDR field of the APB BAR configuration registers address space.	0 - 16#FFF#	0
pmask	MASK field of the APB BAR configuration registers address space.	0 - 16#FFF#	16#FFF#
oepol	Polarity of bdrive and vbdrive signals. 0=active low, 1=active high	0 - 1	0
bus16	Enable support for 16-bit PROM/IO accesses	0 - 1	0

105.6 Signal descriptions

Table 1688 shows the interface signals of the core (VHDL ports).

*Table 1688.*Signal descriptions

Signal name	Field	Type	Function	Polarity
CLK	N/A	Input	Clock	-
RST	N/A	Input	Reset	Low
SRI	DATA[31:0]	Input	Memory data	High
	BRDYN	Input	Not used	-
	BEXCN	Input	Not used	-
	WRN[3:0]	Input	Not used	-
	BWIDTH[1:0]	Input	PROM bus width at reset	-
	SD[63:0]	Input	Not used	-
	CB[7:0]	Input	Not used	-
	SCB[7:0]	Input	Not used	-
	EDAC	Input	Not used	-

*Table 1688.*Signal descriptions

Signal name	Field	Type	Function	Polarity
SRO	ADDRESS[27:0]	Output	Memory address	High
	DATA[31:0]	Output	Memory data	High
	SDDATA[63:0]	Output	Not used	-
	RAMSN[7:0]	Output	SSRAM chip-select, only bit 0 is used	Low
	RAMOEN[7:0]	Output	Same as OEN	Low
	IOSN	Output	I/O chip-select	Low
	ROMSN[7:0]	Output	PROM chip-select, only bit 0 is used	Low
	OEN	Output	Output enable	Low
	WRITEN	Output	Write strobe	Low
	WRN[3:0]	Output	SSRAM byte write enable: WRN[0] corresponds to DATA[31:24], WRN[1] corresponds to DATA[23:16], WRN[2] corresponds to DATA[15:8], WRN[3] corresponds to DATA[7:0].	Low
	MBEN[3:0]	Output	Not used	Low
	BDRIVE[3:0]	Output	Drive byte lanes on external memory bus. Controls I/O-pads connected to external memory bus: BDRIVE[0] corresponds to DATA[31:24], BDRIVE[1] corresponds to DATA[23:16], BDRIVE[2] corresponds to DATA[15:8], BDRIVE[3] corresponds to DATA[7:0]. Any BDRIVE[ ] signal can be used for CB[ ].	Low/High[2]
	VBDRIVE[31:0]	Output	Identical to BDRIVE but has one signal for each data bit. Every index is driven by its own register. This can be used to reduce the output delay.	Low/High[2]
	SVBDRIVE	Output	Not used	-
	READ	Output	Not used	-
	SA[14:0]	Output	Not used	-
	CB[7:0]	Output	Not used	-
	SCB[7:0]	Output	Not used	-
	VCDRIVE[7:0]	Output	Not used	-
	SVCDRIVE[7:0]	Output	Not used	-
	CE	Output	Not used	-
AHBSI	1)	Input	AHB slave input signals	-
AHBSO	1)	Output	AHB slave output signals	-
APBI	1)	Input	APB slave input signals	-
APBO	1)	Output	APB slave output signals	-

1) See GRLIB IP Library User's Manual

2) Polarity is selected with the oepol generic

105.7 Library dependencies

Table 1689 shows libraries used when instantiating the core (VHDL libraries).

*Table 1689.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AHB signal definitions
GAISLER	MEMCTRL	Signals, component	Memory bus signals definitions, component declaration

105.8 Component declaration

The core has the following component declaration.

```
component ssrctrl
  generic (
    hindex  : integer := 0;
    pindex  : integer := 0;
    romaddr : integer := 0;
    rommask : integer := 16#ff0#;
    ramaddr : integer := 16#400#;
    rammask : integer := 16#ff0#;
    ioaddr  : integer := 16#200#;
    iomask  : integer := 16#ff0#;
    paddr   : integer := 0;
    pmask   : integer := 16#fff#;
     oepol   : integer := 0;
     bus16 : integer := 0
  );
  port (
    rst     : in  std_ulogic;
    clk     : in  std_ulogic;
    ahbsi   : in  ahb_slv_in_type;
    ahbso   : out ahb_slv_out_type;
    apbi    : in  apb_slv_in_type;
    apbo    : out apb_slv_out_type;
    sri     : in  memory_in_type;
    sro     : out memory_out_type

  );
end component;
```

105.9 Instantiation

This example shows how the core can be instantiated.

The example design contains an AMBA bus with a number of AHB components connected to it, including the memory controller. The external memory bus is defined in the example designs port map and connected to the memory controller. System clock and reset are generated by the Clkgen_ml401 Clock Generator and GR Reset Generator.

The memory controller decodes default memory areas: PROM area is 0x0 - 0x00FFFFFF, I/O-area is 0x20000000-0x20FFFFFF and RAM area is 0x40000000 - 0x40FFFFFF.

```
library ieee;
use ieee.std_logic_1164.all;
library grlib, techmap;
use grlib.amba.all;
use grlib.stdlib.all;
use techmap.gencomp.all;
library gaisler;
use gaisler.memctrl.all;
use gaisler.misc.all;

entity ssrctrl_ex is
```

```
 port (
    sys_rst_in: in  std_ulogic;
    sys_clk: in  std_ulogic; -- 100 MHz main clock
    sram_flash_addr : out std_logic_vector(22 downto 0);
    sram_flash_data : inout std_logic_vector(31 downto 0);
    sram_cen  : out std_logic;
    sram_bw   : out std_logic_vector (0 to 3);
    sram_flash_oe_n : out std_ulogic;
    sram_flash_we_n : out std_ulogic;
    flash_ce  : out std_logic;
    sram_clk  : out std_ulogic;
    sram_clk_fb: in  std_ulogic;
    sram_mode : out std_ulogic;
    sram_adv_ld_n : out std_ulogic;
    sram_zz : out std_ulogic;
    iosn    : out std_ulogic;
);
end;

architecture rtl of ssrctrl_ex is

-- Clock generator component
component clkgen_ml401
  generic (
    clk_mul  : integer := 1;
    clk_div  : integer := 1;
    freq     : integer := 100000);-- clock frequency in KHz
  port (
    clkin   : in  std_logic;
    clk     : out std_logic;-- main clock
    ddrclk  : out std_logic;-- DDR clock
    ddrclkfb: in  std_logic;-- DDR clock feedback
    ddrclk90  : out std_logic;-- DDR 90 clock
    ddrclk180 : out std_logic;-- 180 clock
    ddrclk270 : out std_logic;-- DDR clock
    ssrclk  : out std_logic;-- SSRAM clock
    ssrclkfb: in  std_logic;-- SSRAM clock feedback
    cgi     : in clkgen_in_type;
    cgo     : out clkgen_out_type);
end component;


-- signals used to connect memory controller and memory bus
signal memi  : memory_in_type;
signal memo  : memory_out_type;

-- AMBA bus (AHB and APB)
signal apbi  : apb_slv_in_type;
signal apbo  : apb_slv_out_vector := (others => apb_none);
signal ahbsi : ahb_slv_in_type;
signal ahbso : ahb_slv_out_vector := (others => ahbs_none);
signal ahbmi : ahb_mst_in_type;
signal ahbmo : ahb_mst_out_vector := (others => ahbm_none);

-- Signals used by clock and reset generators
signal clkm, rstn, rstraw, srclkl : std_ulogic;
signal cgi   : clkgen_in_type;
signal cgo   : clkgen_out_type;
signal ddrclkfb, ssrclkfb, ddr_clkl, ddr_clknl : std_ulogic;


begin

  clkgen0 : clkgen_ml401  -- clock generator
  port map (sys_clk, clkm, ddr_clkl, ddrclkfb, open, ddr_clknl, open, sram_clk,
      sram_clk_fb, cgi, cgo);

  rst0 : rstgen-- reset generator
  port map (sys_rst_in, clkm, cgo.clklock, rstn, rstraw);

  -- AMBA Components are defined here ...
```

```
  -- Memory controller
  mctrl0 : ssrctrl generic map (hindex => 0, pindex => 0)
  port map (rstn, clkm, ahbsi, ahbso(0), apbi, apbo(0), memi, memo);

  -- connect memory controller outputs to entity output signals
  sram_adv_ld_n <=  '0'; sram_mode <=  '0'; sram_zz <= '0';
  sram_flash_addr <= memo.address(24 downto 2); sram_cen <= memo.ramsn(0);
  flash_ce <= memo.romsn(0); sram_flash_oe_n <= memo.oen; iosn <= memo.iosn;
  sram_bw <= memo.wrn; sram_flash_we_n <= memo.writen;

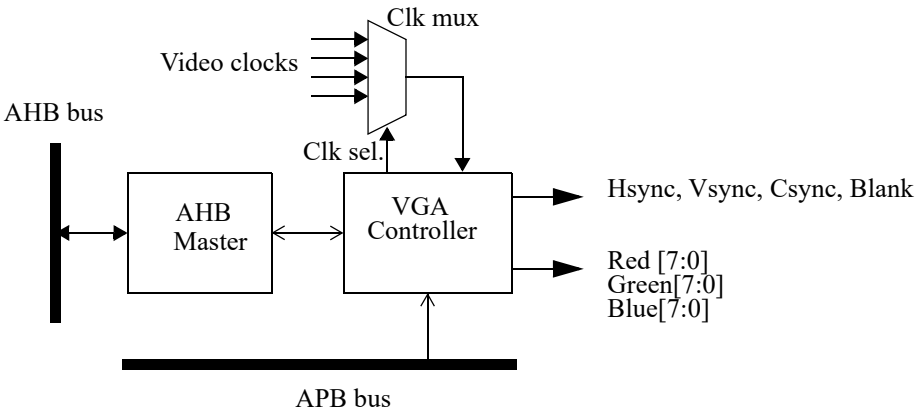
  -- I/O pad instantiation with vectored enable instead
  bdr : for i in 0 to 31 generate
      data_pad : iopad generic map (tech => padtech)
      port map (sram_flash_data(i), memo.data(i),
             memo.vbdrive(i), memi.data(i));
  end generate;

end;
```

106 SVGACTRL - VGA Controller Core

106.1 Overview

The core is a pixel based video controller (frame buffer), capable of displaying standard and custom resolutions with variable bit depth and refresh rates. The video controller consists of a synchronization unit, main control unit, FIFO unit and an AHB master as shown in the figure below.



106.2 Operation

The core uses external frame buffer memory located in the AHB address space. A frame on the display is created by fetching the pixel data from memory and sending it to the screen through an external DAC using three 8-bit color vectors. To hide the AHB bus latency, the pixel data is buffered in a FIFO inside the core. The start address of the frame buffer is specified in the Frame buffer Memory Position register, and can be anywhere in the AHB address space. In addition to the color vectors the video controller also generates HSYNC, VSYNC, CSYNC and BLANK signals control signals.

The video timing is programmable through the Video Length, Front Porch, Sync Length and Line Length registers. The bit depth selection and enabling of the controller is done through the status register. These values make it possible to display a wide range of resolutions and refresh rates.

The pixel clock can be either static or dynamic multiplexed. The frequency of the pixel clock is calculated as *Horizontal Line Length * Vertical Line Length * refresh rate*. When using a dynamically multiplexed clock, bits [5:4] in the status register are used to control the clock selector. The dynamic pixel clocks should be defined in the core's VHDL generics to allow software to read out the available pixel clock frequencies.

The core can use bit depths of 8, 16 and 32 bits. When using 32 bits, bits[23:0] are used, when 16 bits a [5,6,5] color scheme is used and when using 8 bits a color lookup table "CLUT" is used. The CLUT has 256 positions, each 24 bits wide, and the 8 bit values read from memory are used to index the CLUT to obtain the actual color.

106.3 DVI support

In order to initialize a DVI transmitter, an additional core such as the I^2C master is normally required. Additional glue logic may also be required since the interfaces of DVI transmitters differ between manufacturers and product lines. Examples on how to interface the core to a DVI transmitter are available in the GRLIB IP Library's template designs.

106.4 Registers

The core is programmed through registers mapped into APB address space.

*Table 1690.*VGA controller registers

APB address offset	Register
0x00	Status register
0x04	Video length register
0x08	Front Porch register
0x0C	Sync Length register
0x10	Line Length register
0x14	Framebuffer Memory Position register
0x18	Dynamic Clock 0 register
0x1C	Dynamic Clock 1 register
0x20	Dynamic Clock 2 register
0x24	Dynamic Clock 3 register
0x28	CLUT Access register

106.4.1 Status Register

*Table 1691.*0x00 -STAT - Status register

31 10	9	8	7 6	5 4	3	2	1	0
RESERVED	VPOL	HPOL	CLKSEL	BDSEL	VR	R	RST	EN
0	NR	NR	0	NR	0	0	0	0
r	rw	rw	rw	rw	r	r	rw	rw

31:10 RESERVED
9 V polarity (VPOL)- Sets the polarity for the vertical sync pulse.
8 H polarity (HPOL) - Sets the polarity for the horizontal sync pulse.
7:6 Clock Select (CLKSEL) Clock selector when using dynamic pixelclock
5:4 Bit depth selector (BDSEL) - “01” = 8-bit mode; “10” = 16-bit mode; “11” = 32-bit mode
3 Vertical refresh (VR) - High during vertical refresh
2 RESERVED
1 Reset (RST) - Resets the core
0 Enable (EN) - Enables the core

106.4.2 Video Length Register

*Table 1692.*0x04 - VLEN - Video Length register

31 16	15 0
VRES	HRES
0	0
rw	rw

31:16 Vertical screen resolution (VRES) - Vertical screen resolution in pixels -1
15:0 Horisontal screen resolution (HRES) - Horizontal screen resolution in pixels -1.

106.4.3 Front Porch Register

*Table 1693.*0x08 - FPORCH - Front porch register

31 16	15 0
VPORCH	HPORCH
0	0
rw	rw

31:16 Vertical front porch (VPORCH) - Vertical front porch in pixels.
15:0 Horisontal front porch (HPORCH) - Horizontal front porch in pixels.

106.4.4 Sync Length Register

*Table 1694.*0x0C - SYNLEN - Sync length register

31 16	15 0
VPLEN	HPLEN
0	0
rw	rw

31:16 Vertical sync pulse length (VPLEN) - Vertical sync pulse length in pixels.
15:0 Horisontal sync pulse length (HPLEN) - Horizontal sync pulse length in pixels.

106.4.5 Line Length Register

*Table 1695.*0x10 - LINLEN - Line Length register

31 16	15 0
VLLEN	HLLEN
0	0
rw	rw

31:16 Vertical line length (VLLEN) - The length of the total line with front and back porch, sync pulse length and vertical screen resolution.

15:0 Horisontal line length (HLLEN) - The length of the total line with front and back porch, sync pulse length and horizontal screen resolution,

106.4.6 Framebutter Memory Position Register

*Table 1696.*0x14 - FBUF - Framebuffer Memory Position register

31 0
FMEM
0
rw

31:0 Framebuffer memory position (FMEM) - Holds the memory position of the framebuffer, must be aligned on a 1 Kbyte boundary.

106.4.7 Dynamic Clock 0 Register

*Table 1697.*0x18 - DCLK0 - Dynamic clock 0 register

31 0
CLK0
*
r

31:0 Dynamic pixel clock 0 (CLK0) - Dynamic pixel clock defined in ps.

106.4.8 Dynamic Clock 1 Register

*Table 1698.*0x1C - DCLK1 - Dynamic clock 1 register

31 0
CLK1
*
r

31:0 Dynamic pixel clock 1 (CLK1) - Dynamic pixel clock defined in ps.

106.4.9 Dynamic Clock 2 Register

*Table 1699.*0x20 - DCLK2 - Dynamic clock 2 register

31 0
CLK2
*
r

31:0 Dynamic pixel clock 2 (CLK2) - Dynamic pixel clock defined in ps.

106.4.10Dynamic Clock 3 Register

*Table 1700.*0x24 - DCLK3 - Dynamic clock 3 register

31	0
CLK3	
*	
e	

31:0 Dynamic pixel clock 3 (CLK3) - Dynamic pixel clock defined in ps.

106.4.11CLUTA Access Register

*Table 1701.*0x28 - CLUT - CLUT Access register

31 24	23 16	15 8	7 0
CREG	RED	GREEN	BLUE
NR	NR	NR	NR
w	w	w	w

31:24 Color lookup table register (CREG) - Color lookup table register to set.

23:16 Red color data (RED) - Red color data to set in the specified register.

15:8 Green color data (GREEN) - Green color data to set in the specified register.

7:0 Blue color data (BLUE) - Blue color data to set in the specified register.

106.5 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x063. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

106.6 Implementation

106.6.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

See also the documentation for the *asyncrst* VHDL generic.

106.7 Configuration options

Table 1702 shows the configuration options of the core (VHDL generics).

*Table 1702.*Configuration options

Generic name	Function	Allowed range	Default
length	Size of the pixel FIFO	3 - 1008	384
part	Pixel FIFO part length	1 - 336	128
memtech	Memory technology	0 - NTECH	0
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	12-bit MSB APB address	0 - 16#FFF#	0
pmask	APB address mask	0 - 16#FFF#	16#FFF#
hindex	AHB master index	0 - NAHBMST-1	0
hirq	Interrupt line	0 - NAHBIRQ-1	0
clk0	Period of dynamic clock 0 in ps	0- 16#FFFFFFFF#	40000
clk1	Period of dynamic clock 1 in ps	0- 16#FFFFFFFF#	20000
clk2	Period of dynamic clock 2 in ps	0- 16#FFFFFFFF#	15385
clk3	Period of dynamic clock 3 in ps	0- 16#FFFFFFFF#	0
burstlen	AHB burst length. The core will burst $2^{burstlen}$ words.	2 - 8	8
ahbaccsz	Determines the size of the AMBA accesses that the core will use when fetching data from memory.	32 - AHBDW	32
asyncrst	Use asynchronous reset for the VGA clock domain. If this generic is set to 1 the core will use the *arst* input to reset part of the registers in the VGA domain. Asynchronous reset should be used if the VGA clock is not available during system reset. If this generic is 0 the *arst* input is not used.	0 - 1	0

106.8 Signal descriptions

Table 1703 shows the interface signals of the core (VHDL ports).

*Table 1703.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	System clock	-
VGACLK	N/A	Input	Pixel clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
VGAO	HSYNC	Output	Horizontal sync	-
	VSYNC	Output	Vertical sync	-
	COMP_SYNC	Output	Composite sync	-
	BLANK	Output	Blanking	-
	VIDEO_OUT_R[7:0]	Output	Video out, red.	-
	VIDEO_OUT_G[7:0]	Output	Video out, green.	-
	VIDEO_OUT_B[7:0]	Output	Video out, blue.	-
	BITDEPTH[1:0]	Output	Value of Status register's BDSEL field	-
AHBI	*	Input	AHB master input signals	-
AHBO	*	Output	AHB master output signals	-
CLK_SEL[1:0]	N/A	Output	2-bit clock selector	-
ARST	N/A	Input	Asynchronous reset input	Low

* see GRLIB IP Library User's Manual

106.9 Library dependencies

Table 1704 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1704.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
GAISLER	MISC	Component, signals	Component and signal definitions.

106.10 Instantiation

This example shows how the core can be instantiated.

```
library grlib;
use grlib.amba.all;
library Gaisler;
use gaiser.misc.all;
.
architecture rtl of test is
signal apbi : apb_slv_in_type;
signal apbo : apb_slv_out;
signal vgao : apbvga_out_type;
signal ahbi : ahb_mst_in_type;
signal ahbo : ahb_mst_out_type;
signal clk_sel :std_logic_vector(1 downto 0));
signal clkmvga : std_logic;
begin
.
.
```

```
-- VGA Controller
  vga0 : svgactrl
  generic map(memtech => memtech, pindex => 6, paddr => 6, hindex => 6,
    clk0 => 40000, clk1 => 20000, clk2 => 15385, clk3 => 0)
  port map(rstn,clkm,clkmvga, apbi, apbo(6), vgao,ahbmi,ahbmo(6),clk_sel);
end;
```

106.11 Linux 2.6 driver

A video driver for the core is provided Snapgear Linux (-p27 and later). The proper kernel command line options must be used for the driver to detect the core. Please see the SnapGear Linux for LEON manual for further information.

107 SYNCIOTEST - Test block for synchronous I/O interfaces

107.1 Overview

This IP core is a helper block for instantiation into other IP cores, in order to simplify clock-to-out and setup/hold production testing on ASICs. It needs to be embedded into the IP in order to use the same registers as is used in the functional mode in order to get relevant timing measurement.

It currently has a few conditions on its use for implementation reasons:

- Number of inputs+bidirs needs to be 8 or more.
- Number of outputs needs to be at least 1

107.2 Operation

The modes are:

- Idle
- Output pseudo-random sequence on outputs and bidirs (pattern repeats after 255 cycles)
- Output toggle values between all-ones and all-zeros
- Output toggle between all-one, tristate, all-zero, tristate, ...
- Output toggle each bit in sequence "00101010" with other values first as all-one and then again with other outputs as all-zero.
- Input same pseudo-random sequence as in output mode above. If the wrong data is received on a byte lane, one of the outputs is set to flag an error. The PRNG is re-seeded with the input data every cycle to make the test mode self synchronizing with the input stream.

The tmodeact output controls when the test mode is activated, when high the surrounding IP core should mux in the dataout vector to the output registers and the tmodeoe signal to bidir output-enable registers.

A simple safety scheme is implemented. An inverted copy of the mode vector must be supplied on the top bits of the tmode input, if this is incorrect then no mode is activated. If the tmode signal is mapped to a register in the IP core, it can scrub the field for accidental bit-flips by clearing it when the tmode-act signal is low.

107.3 Implementation

107.3.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

107.4 Configuration options

Table 1705 shows the configuration options of the core (VHDL generics).

*Table 1705.*Configuration options

Generic name	Function	Allowed range	Default
ninputs	Number of inputs		1
noutputs	Number of outputs		1
nbidir	Number of bidirectional signals		1
dirmode	Direction mode. 0=both, 1=in-only, 2=out-only		1

107.5 Signal descriptions

Table 1706 shows the interface signals of the core (VHDL ports).

*Table 1706.*Signal descriptions

Signal name	Field	Type	Function	Active
CLK	N/A	Input	Clock	-
RSTN	N/A	Input	Reset	Low
DATAIN	N/A	Input	Data input	-
DATAOUT	N/A	Output	Data output	-
TMODE	N/A	Input	Test mode	High
TMODEACT	N/A	Output	Test mode activated	High
TMODEOE	N/A	Output	Test mode output enable	High

* see GRLIB IP Library User's Manual

107.6 Library dependencies

Table 1707 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1707.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	DFTLIB	Component, signals	Component declaration

108 SYNCRAM - Single-port RAM generator

108.1 Overview

SYNCRAM is a single port RAM that maps on technology-specific RAM blocks. The core has a common address bus, and separate data-in and data-out buses. All inputs are latched on the on the rising edge of clk. The read data appears on dataout directly after the clk rising edge.

108.2 Configuration options

Table 1708 shows the configuration options of the core (VHDL generics).

*Table 1708.*Configuration options

Name	Function	Range	Default
tech	Technology selection	0 - NTECH	0
abits	Address bits. Depth of RAM is $2^{abits-1}$	see table below	-
dbits	Data width	see table below	-
testen	Enable bypass logic for scan testing	0 - 1	0
custombits	Bits used by custom interface		
pipeline	Adds pipeline register on data outputs. Adds one clock cycle latency	0 - 15	0

108.3 Scan test support

Scan test support will be enabled if the TESTEN generic is set to 1. This option will generate a register (flip-flops) connected between the DATAIN and DATAOUT of the syncram module. In test mode, DATAOUT is driven from the register rather then from the RAM outputs. This will allow both input and output paths around the syncram to be testable by scan. The address bus and control signals are xored with the DATAIN signal to also increase test coverage of those. Test mode is enabled by driving the TESTIN(3) signals to 1. This signal should typically be connected to the global test enable signals of the design.

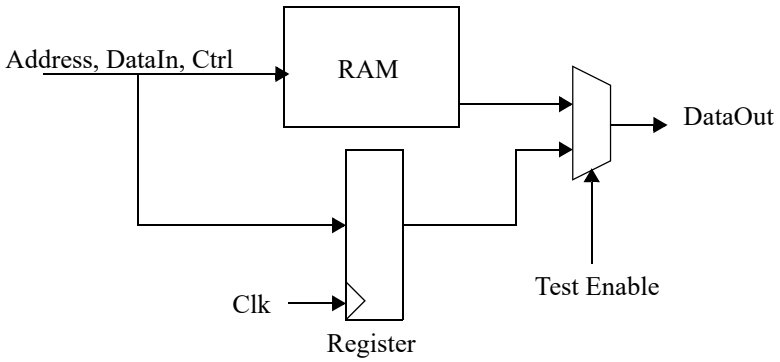


Figure 286. Scan test support

Table 1709 shows the supported technologies for the core.

*Table 1709.*Supported technologies

Tech name	Technology	RAM cell	abit range	dbit range
altera	All Altera devices	altsyncram	unlimited	unlimited
ihp15	IHP 0.25	sram2k (512x32)	2 - 9	unlimited
inferred	Behavioral description	Tool dependent	unlimited	unlimited
virtex	Xilinx Virtex, VirtexE, Spartan2	RAMB4_Sn	unlimited	unlimited
virtex2, virtex4, virtex5, spartan3, spartan6, virtex7, kintex7, artix7, zynq7000, kintexu	Xilinx Virtex2/4/5/6, Spartan3/3a/3e/6, 7-Series, Ultrascale	RAMB16_Sn	unlimited	unlimited
axcel / axdsp	Actel AX, RTAX and RTAX-DSP	RAM64K36	2 - 12	unlimited
proasic	Actel Proasic	RAM256x9SST	2 - 14	unlimited
proasic3	Actel Proasic3	ram4k9, ram512x18	2 - 12	unlimited
lattice	Lattice XP/EC/ECP	sp8ka	2 - 13	unlimited
memvirage	Virage ASIC RAM	hdss1_128x32cm4sw0 hdss1_256x32cm4sw0 hdss1_512x32cm4sw0 hdss1_1024x32cm8sw0	7 - 11	32
memartisan	Artisan ASIC RAM	sp_256x32m32 sp_512x32m32 sp_1kx32m32 sp_2kx32m32 sp_4kx32m32 sp_8kx32m32 sp_16kx32m32	8 - 14	32
memvirage90	Virage 90 nm ASIC RAM	SPRAM_HS_32x30 SPRAM_HS_128x32 SPRAM_HS_256x32 SPRAM_HS_1024x32	2 - 10	128
eclipse	Aeroflex/Quicklogic FPGA	RAM128x18_25um RAM256X9_25um RAM512X4_25um RAM1024X2_25um	2 - 10	unlimited
easic90	eASIC 90 nm Nextreme	eram, bram	2 - 15	unlimited
easic45	eASIC 45 nm Nextreme2	bRAM, rFile	unlimited	unlimited
igloo2 / smartfusion2	Microsemi IGLOO2 / SmartFusion2	RAM1K18	2 - 14	unlimited
rtg4	Microsemi RTG4	RAM1K18_RT	2 - 16	unlimited

108.4 Signal descriptions

Table 1710 shows the interface signals of the core (VHDL ports).

*Table 1710.*Signal descriptions

Signal name	Field	Type	Function	Active
CLK	N/A	Input	Clock. All input signals are latched on the rising edge of the clock.	-
ADDRESS	N/A	Input	Address bus. Used for both read and write access.	-
DATAIN	N/A	Input	Data inputs for write data	-
DATAOUT	N/A	Output	Data outputs for read data	-
ENABLE	N/A	Input	Chip select	High
WRITE	N/A	Input	Write enable	High
TESTIN		Input	Test inputs (see text)	High

108.5 Library dependencies

Table 1711 shows libraries used when instantiating the core (VHDL libraries).

*Table 1711.*Library dependencies

Library	Package	Imported unit(s)	Description
TECHMAP	GENCOMP	Constants	Technology contants

108.6 Component declaration

The core has the following component declaration.

```
library techmap;
use techmap.gencomp.all;

  component syncram
  generic (tech : integer := 0; abits : integer := 6; dbits : integer := 8);
  port (
    clk      : in std_ulogic;
    address  : in std_logic_vector((abits -1) downto 0);
    datain   : in std_logic_vector((dbits -1) downto 0);
    dataout  : out std_logic_vector((dbits -1) downto 0);
    enable   : in std_ulogic;
    write    : in std_ulogic;
    testin   : in std_logic_vector(3 downto 0) := "0000");
  end component;
```

108.7 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;
library techmap;
use techmap.gencomp.all;
.

clk      : std_ulogic;
address  : std_logic_vector((abits -1) downto 0);
datain   : std_logic_vector((dbits -1) downto 0);
dataout  : std_logic_vector((dbits -1) downto 0);
enable   : std_ulogic;
write    : std_ulogic);
```

```
ram0 : syncram generic map ( tech => tech, abits => addrbits, dbits => dbits)
      port map ( clk, addr, datain, dataout, enable, write);
```

109 SYNCRAMBW - Single-port RAM generator with byte enables

109.1 Overview

SYNCRAMBW implements a single port RAM with byte enables, using the GRLIB technology wrapping for different target technologies. The core operates identically to SYNCRAM, with the addition that each byte has a separate chip select (ENABLE) and write select (WRITE). The core is provided in a generic configuration and also in configurations of 128, 156 and 256 bits, and the corresponding entities are named SYNCRAMBW, SYNCRAM128BW, SYNCRAM156BW and SYNCRAM256BW. In the simplest case, the IP cores just instantiate several eight bit wide SYNCRAM components. SYNCRAM128BW, SYNCRAM156BW and SYNCRAM256BW, used in GRLIB's Level-2 cache core, contain specialized maps for several technologies to more efficiently utilize device resources.

Note that some SYNCRAM components may be missing from the library depending on the type of GRLIB distribution.

109.2 Configuration options

Table 1712 shows the configuration options of the core (VHDL generics).

*Table 1712.*Configuration options

Name	Function	Range	Default
tech	Technology selection	0 - NTECH	0
abits	Address bits. Depth of RAM is $2^{abits-1}$	see table below	-
testen	Enable bypass logic for scan testing	0 - 1	0
custombits	Bits used by custom interface		
pipeline	Adds pipeline register on data outputs. Adds one clock cycle latency	0 - 15	0

109.3 Scan test support

Scan test support will be enabled if the TESTEN generic is set to 1. This option will generate a register (flip-flops) connected between the DATAIN and DATAOUT of the syncram module. In test mode, DATAOUT is driven from the register rather then from the RAM outputs. This will allow both input and output paths around the syncram to be testable by scan. The address bus and control signals are xored with the DATAIN signal to also increase test coverage of those. Test mode is enaled by driving the TESTIN(3) signals to 1. This signal should typically be connected to the global test enable signals of the design.

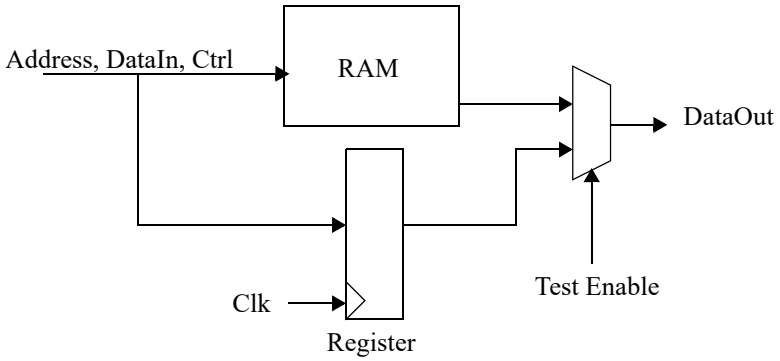


Figure 287. Scan test support

109.4 Technology support

Table 1713 shows the supported technologies for the core.

*Table 1713.*Supported technologies

Tech name	Technology	RAM cell	abit range	dbit range
altera	All Altera devices	altsyncram	unlimited	unlimited
inferred	Behavioral description	Tool dependent	unlimited	unlimited
virtex2, virtex4, virtex5, spartan3, spartan6, virtex7, kintex7, artix7, zynq7000, kintexu	Xilinx Virtex2/4/5/6, Spartan3/3a/3e/6, 7-Series, Ultrascale	RAMB16_Sn	unlimited	unlimited
all others	-	syncram core with dwidth=8	tech depend.	tech depend.

To add support for a new technology, the following steps should be taken:

- Add technology-specific version for the RAM core in lib/techmap/TECH
- Instantiate the technology-specific RAM core in lib/techmap/maps/syncram256bw.vhd, and set the has_sram256bw() constant to 1 for the specific technology:

```
constant has_sram256bw : tech_ability_type := (
virtex2 => 1, virtex4 => 1, virtex5 => 1, spartan3 => 1,
spartan3e => 1, spartan6 => 1, virtex6 => 1,
altera => 1, cyclone3 => 1, stratix2 => 1, stratix3 => 1,
tm65gpl => 0, others => 0);
```

See also syncrambw.vhd, syncram128bw.vhd and syncram156bw.vhd under lib/techmap/maps/ for the corresponding SYNCRAM BW IP cores.

109.5 Signal descriptions

Table 1714 shows the interface signals of the core (VHDL ports).

*Table 1714.*Signal descriptions

Signal name	Field	Type	Function	Active
CLK	N/A	Input	Clock. All input signals are latched on the rising edge of the clock.	-
ADDRESS	N/A	Input	Address bus. Used for both read and write access.	-
DATAIN	N/A	Input	Data inputs for write data	-
DATAOUT	N/A	Output	Data outputs for read data	-
ENABLE	N/A	Input	Byte Chip select	High
WRITE	N/A	Input	Byte Write enable	High
TESTIN		Input	Test inputs (see text)	High

109.6 Library dependencies

Table 1715 shows libraries used when instantiating the core (VHDL libraries).

*Table 1715.*Library dependencies

Library	Package	Imported unit(s)	Description
TECHMAP	GENCOMP	Constants	Technology contants

109.7 Component declaration

The core has the following component declaration.

```
library techmap;
use techmap.gencomp.all;

  component syncram_bw128
  generic (tech : integer := 0; abits : integer := 6);
  port (
    clk      : in std_ulogic;
    address  : in std_logic_vector((abits -1) downto 0);
    datain   : in std_logic_vector(127 downto 0);
    dataout  : out std_logic_vector(127 downto 0);
    enable   : in std_logic_vector(15 downto 0);
    write    : in std_logic_vector(15 downto 0);
    testin   : in std_logic_vector(3 downto 0) := "0000");
  end component;

  component syncram_bw256
  generic (tech : integer := 0; abits : integer := 6);
  port (
    clk      : in std_ulogic;
    address  : in std_logic_vector((abits -1) downto 0);
    datain   : in std_logic_vector(255 downto 0);
    dataout  : out std_logic_vector(255 downto 0);
    enable   : in std_logic_vector(31 downto 0);
    write    : in std_logic_vector(31 downto 0);
    testin   : in std_logic_vector(3 downto 0) := "0000");
  end component;
```

109.8 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
```

```
use ieee.std_logic_1164.all;
library techmap;
use techmap.gencomp.all;
.

clk      : std_ulogic;
address  : std_logic_vector(9 downto 0);
datain   : std_logic_vector(255 downto 0);
dataout  : std_logic_vector(255 downto 0);
enable   : std_logic_vector(31 downto 0);
write    : std_logic_vector(31 downto 0);

ram0 : syncram generic map ( tech => tech, abits => 10)
      port map ( clk, addr, datain, dataout, enable, write);
```

110 SYNCRAM_2P - Two-port RAM generator

110.1 Overview

The two-port RAM generator has a one read port and one write port. Each port has a separate address and data bus. All inputs are registered on the rising edge of clk. The read data appears on dataout directly after the clk rising edge. Address width, data width and target technology is parametrizable through generics.

110.2 Write-through operation

Write-through is supported if the function *syncram_2p_write_through(tech)* returns 1 for the target technology, or if the *wrfst* generic is set to 1. If *wrfst* = 1, additional logic will be generated to detect simultaneous read/write to the same memory location, and in that case bypass the written data to the data outputs.

110.3 Conflicts

Some technologies will produce unpredictable results when a read and write operation occurs simultaneously to the same memory location. The function *syncram_2p_dest_rw_collision(tech)* returns 1 for technologies that has this characteristic. If SYNCRAM_2P is implemented with *sepclk* = 0 then logic will be included that disables the read enable signal, if needed, when a collision is detected. If the core is implemented with *sepclk* = 1 (and *syncram_2p_dest_rw_collision(tech)* returns 1) then collision avoidance must be handled by external logic.

110.4 Scan test support

Scan test support will be enabled if the TESTEN generic is set to 1. This option will generate a register (flip-flops) connected between the DATAIN and DATAOUT of the syncram module. In test mode, DATAOUT is driven from the register rather then from the RAM outputs. This will allow both input and output paths around the syncram to be testable by scan. The address bus and control signals are xored with the DATAIN signal to also increase test coverage of those. Test mode is enaled by driving the TESTIN(3) signals to 1. This signal should typically be connected to the global test enable signals of the design.

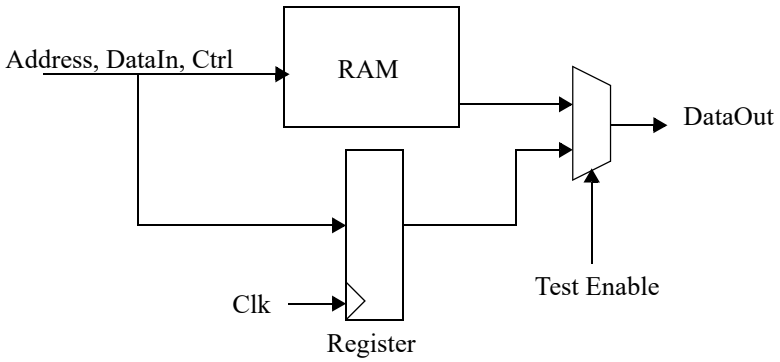


Figure 288. Scan test support

110.5 Configuration options

Table 1716 shows the configuration options of the core (VHDL generics).

*Table 1716.*Configuration options

Name	Function	Range	Default
tech	Technology selection	0 - NTECH	0
abits	Address bits. Depth of RAM is $2^{abits-1}$	see table below	-
dbits	Data width	see table below	-
sepclk	If 1, separate clocks (rclk/wclk) are used for the two ports. If 0, wclk is used for both ports.	0 - 1	0
wrfst	Enable bypass logic for write-through operation. Can only be enabled for sepclk = 0.	0 - 1	0
testen	Enable bypass logic for scan testing	0 - 1	0
pipeline	Adds pipeline registers on data outputs	0 - 15	0

Table 1717 shows the supported technologies for the core.

*Table 1717.*Supported technologies

Tech name	Technology	RAM cell	abit range	dbit range
Inferred	Behavioural description	Tool dependent	unlimited	unlimited
altera	All Altera devices	altsyncram	umlimited	unlimited
virtex	Xilinx Virtex, Virtex-E, Spartan-2	RAMB4_Sn	2 - 10	unlimited
virtex2, virtex4, virtex5, spartan3, spartan6, virtex7, kintex7, artix7, zynq7000, kintexu	Xilinx Virtex2/4/5/6, Spartan3/3a/3e/6, 7-Series, Ultrascale	RAMB16_Sn	2 - 14	unlimited
axcel / axdsp	Actel AX, RTAX and RTAX-DSP	RAM64K36	2 - 12	unlimited
proasic	Actel Proasic	RAM256x9SST	2 - 14	unlimited
proasic3	Actel Proasic3	ram4k9, ram512x18	2 - 12	unlimited
lattice	Lattice XP/EC/ECP	dp8ka	2 - 13	unlimited
memvirage	Virage ASIC RAM	hdss2_64x32cm4sw0 hdss2_128x32cm4sw0 hdss2_256x32cm4sw0 hdss2_512x32cm4sw0	6 - 9	32
memartisan	Artisan ASIC RAM	rf2_256x32m4 rf2_512x32m4	8 - 9	32
eclipse	Aeroflex/Quicklogic FPGA	RAM128x18_25um RAM256X9_25um RAM512X4_25um RAM1024X2_25um	2 - 10	unlimited
easic90	eASIC 90 nm Nextreme	eram	2 - 12	unlimited
easic45	eASIC 45 nm Nextreme2	bRAM, rFile	unlimited	unlimited
igloo2 / smartfusion2	Microsemi IGLOO2 / SmartFusion2	RAM1K18	2 - 14	unlimited
rtg4	Microsemi RTG4	RAM1K18_RT	2 - 16	unlimited

110.6 Signal descriptions

Table 1718 shows the interface signals of the core (VHDL ports).

*Table 1718.*Signal descriptions

Signal name	Type	Function	Active
RCLK	Input	Read port clock	-
RENABLE	Input	Read enable	High
RADDRESS	Input	Read address bus	-
DATAOUT	Output	Data outputs for read data	-
WCLK	Input	Write port clock	-
WRITE	Input	Write enable	High
WADDRESS	Input	Write address	-
DATAIN	Input	Write data	-
TESTEN	Input	Test inputs (see text)	High

110.7 Library dependencies

Table 1719 shows libraries used when instantiating the core (VHDL libraries).

*Table 1719.*Library dependencies

Library	Package	Imported unit(s)	Description
TECHMAP	GENCOMP	Constants	Technology contants

110.8 Component declaration

The core has the following component declaration.

```
library techmap;
use techmap.gencomp.all;

component syncram_2p
  generic (tech : integer := 0; abits : integer := 6; dbits : integer := 8; sepclk : integer
:= 0);
  port (
    rclk     : in std_ulogic;
    renable  : in std_ulogic;
    raddress : in std_logic_vector((abits -1) downto 0);
    dataout  : out std_logic_vector((dbits -1) downto 0);
    wclk     : in std_ulogic;
    write    : in std_ulogic;
    waddress : in std_logic_vector((abits -1) downto 0);
    datain   : in std_logic_vector((dbits -1) downto 0);
    testin   : in std_logic_vector(3 downto 0) := "0000");
  end component;
```

110.9 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;
library techmap;
use techmap.gencomp.all;

rclk     : in std_ulogic;
renable  : in std_ulogic;
raddress : in std_logic_vector((abits -1) downto 0);
```

```
dataout  : out std_logic_vector((dbits -1) downto 0);
wclk     : in std_ulogic;
write    : in std_ulogic;
waddress : in std_logic_vector((abits -1) downto 0);
datain   : in std_logic_vector((dbits -1) downto 0));

ram0 : syncram_2p generic map ( tech => tech, abits => addrbits, dbits => dbits)
      port map ( rclk, renable, raddress, dataout, wclk, write, waddress, datain, enable,
write);
```

111 SYNCRAM_DP - Dual-port RAM generator

111.1 Overview

The dual-port RAM generator has two independent read/write ports. Each port has a separate address and data bus. All inputs are latched on the on the rising edge of clk. The read data appears on dataout directly after the clk rising edge. Address width, data width and target technology is parametrizable through generics. Simultaneous write to the same address is technology dependent, and generally not allowed.

111.2 Configuration options

Table 1720 shows the configuration options of the core (VHDL generics).

*Table 1720.*Configuration options

Name	Function	Range	Default
tech	Technology selection	0 - NTECH	0
abits	Address bits. Depth of RAM is $2^{abits-1}$	see table below	-
dbits	Data width	see table below	-
testen	Enable bypass logic for scan testing	0 - 1	0
custombits	Bits used by custom interface		
sepclk	If 1, separate clocks are used for the two ports.	0 - 1	0
wrfst	Enable bypass logic for write-through operation. Can only be enabled for sepclk = 0.	0 - 1	0
pipeline	Adds pipeline registers on data outputs	0 - 15	0

Table 1721 shows the supported technologies for the core.

*Table 1721.*Supported technologies

Tech name	Technology	RAM cell	abit range	dbit range
altera	All altera devices	altsyncram	unlimited	unlimited
virtex	Xilinx Virtex, Virtex-E, Spartan-2	RAMB4_Sn	2 - 10	unlimited
virtex2, virtex4, virtex5, spartan3, spartan6, virtex7, kintex7, artix7, zynq7000, kintexu	Xilinx Virtex2/4/5/6, Spartan3/3a/3e/6, 7-Series, Ultrascale	RAMB16_Sn	2 - 14	unlimited
proasic3	Actel Proasic3	ram4k9	2 - 12	unlimited
lattice	Lattice XP/EC/ECP	dp8ka	2 - 13	unlimited
memvirage	Virage ASIC RAM	hdss2_64x32cm4sw0 hdss2_128x32cm4sw0 hdss2_256x32cm4sw0 hdss2_512x32cm4sw0	6 - 9	32
memartisan	Artisan ASIC RAM	dp_256x32m4 dp_512x32m4 dp_1kx32m4	8 - 10	32
memvirage90	Virage 90 nm ASIC RAM	DPRAM_HS_256x20 DPRAM_HS_256x32	2 - 8	128
easic45	eASIC 45 nm Nextreme2	bRAM	unlimited	unlimited
igloo2 / smartfusion2	Microsemi IGLOO2 / SmartFusion2	RAM1K18	2 - 14	unlimited
rtg4	Microsemi RTG4	RAM1K18_RT	2 - 16	unlimited

111.3 Signal descriptions

Table 1722 shows the interface signals of the core (VHDL ports).

*Table 1722.*Signal descriptions

Signal name	Field	Type	Function	Active
CLK1	N/A	Input	Port1 clock	-
ADDRESS1	N/A	Input	Port1 address	-
DATAIN1	N/A	Input	Port1 write data	-
DATAOUT1	N/A	Output	Port1 read data	-
ENABLE1	N/A	Input	Port1 chip select	High
WRITE1	N/A	Input	Port 1 write enable	High
CLK2	N/A	Input	Port2 clock	-
ADDRESS2	N/A	Input	Port2 address	-
DATAIN2	N/A	Input	Port2 write data	-
DATAOUT2	N/A	Output	Port2 read data	-
ENABLE2	N/A	Input	Port2 chip select	High
WRITE2	N/A	Input	Port 2 write enable	High

111.4 Library dependencies

Table 1723 shows libraries used when instantiating the core (VHDL libraries).

*Table 1723.*Library dependencies

Library	Package	Imported unit(s)	Description
TECHMAP	GENCOMP	Constants	Technology contants

111.5 Component declaration

The core has the following component declaration.

```
library techmap;
use techmap.gencomp.all;

component syncram_dp
  generic (tech : integer := 0; abits : integer := 6; dbits : integer := 8);
  port (
    clk1     : in std_ulogic;
    address1 : in std_logic_vector((abits -1) downto 0);
    datain1  : in std_logic_vector((dbits -1) downto 0);
    dataout1 : out std_logic_vector((dbits -1) downto 0);
    enable1  : in std_ulogic;
    write1   : in std_ulogic;
    clk2     : in std_ulogic;
    address2 : in std_logic_vector((abits -1) downto 0);
    datain2  : in std_logic_vector((dbits -1) downto 0);
    dataout2 : out std_logic_vector((dbits -1) downto 0);
    enable2  : in std_ulogic;
    write2   : in std_ulogic);
  end component;
```

111.6 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;
library techmap;
use techmap.gencomp.all;

clk1     : in std_ulogic;
address1 : in std_logic_vector((abits -1) downto 0);
datain1  : in std_logic_vector((dbits -1) downto 0);
dataout1 : out std_logic_vector((dbits -1) downto 0);
enable1  : in std_ulogic;
write1   : in std_ulogic;
clk2     : in std_ulogic;
address2 : in std_logic_vector((abits -1) downto 0);
datain2  : in std_logic_vector((dbits -1) downto 0);
dataout2 : out std_logic_vector((dbits -1) downto 0);
enable2  : in std_ulogic;
write2   : in std_ulogic);

ram0 : syncram_dp generic map ( tech => tech, abits => addrbits, dbits => dbits)
      port map ( clk1, address1, datain1, dataout1, enable1, write1, clk2, address2, datain2,
dataout2, enable2, write2);
```

112 SYNCRAMFT - Single-port RAM generator with EDAC

112.1 Overview

SYNCRAMFT is a single port RAM that maps on technology-specific RAM blocks. The core has a common address bus, and separate data-in and data-out buses. All inputs are latched on the on the rising edge of clk. The read data appears on dataout directly after the clk rising edge. SYNCRAMFT can be configured to include logic for error detection or error detection and correction. This protection is added either as logic connected to an internal SYNCRAM instantiation or by mapping directly to technology specific memory resources with SECDED EDAC.

112.2 Configuration options

Table 1724 shows the configuration options of the core (VHDL generics).

*Table 1724.*Configuration options

Name	Function	Range	Default
tech	Technology selection	0 - NTECH	0
abits	Address bits. Depth of RAM is $2^{abits-1}$	-	-
dbits	Data width	-	-
ft	Fault-tolerance 0: Standard SYNCRAM, no FT 1: byte parity DMR 2: true TMR 3: byte-parity, no DMR (only error detection) 4: SECDED - BCH 5: SECDED - target technology specific The option of target technology specific EDAC is currently supported for Xiliinx Virtex5, Virtex6 and 7-series FPGAs. It is also supported for Microsemi RTG4 FPGAs.	0 - 5	0
testen	Enable bypass logic for scan testing	0 - 1	0
custombits	Bits used by custom interface		
pipeline	Adds pipeline registers on data outputs. Bits 3:0 of is a field that adds registers to the data outputs of the RAM cell. This adds one additional clock cycle before the read data is available on the SYNCRAM data outputs. Bits 7:4 is a field that adds a register after the error correction logic. This adds one additional clock cycle before the read data is available on the data outputs. The error signals are delayed in the same way as the data. This has the following effect on data read latency Pipeline value: added latency 0 : 0 1 : 1 16: 1 17: 2	0 - 255	0

112.3 Scan test support

See SYNCRAM documentation.

112.4 Signal descriptions

Table 1725 shows the interface signals of the core (VHDL ports).

*Table 1725.*Signal descriptions

Signal name	Field	Type	Function	Active
CLK	N/A	Input	Clock. All input signals are latched on the rising edge of the clock.	-
ADDRESS	N/A	Input	Address bus. Used for both read and write access.	-
DATAIN	N/A	Input	Data inputs for write data	-
DATAOUT	N/A	Output	Data outputs for read data	-
ENABLE	N/A	Input	Chip select	High
WRITE	N/A	Input	Write enable	High
ERROR	N/A	Output	Different behaviour depending on setting of VHDL generic ft: 0 .. 3: Error output has one position per byte 4 .. 5: Error output has two positions: 0:CERR, 1: UCERR. CERR is asserted for correctable error. UCERR is asserted for uncorrectable errors and overrides CERR.	High
TESTIN	N/A	Input	Test inputs (see text)	High
ERRINJ	N/A	Input	Different behaviour depending on setting of VHDL generic ft: errinj bits (((dbits + 7)/8)*2-1 downto 0) are used for byte parity DMR (FT = 1) errinj cannot currently be used with FT = 2 (TMR) errinj bits (((dbits + 7)/8)-1 downto 0) are used for byte parity, no DMR (FT = 3) errinj bits 6 downto 0 are used for SECDED - BCH (FT = 4) errinj bits used for technology specific EDAC (FT = 5) depends on the target technology. For Xilinx, bits 1:0 are used. 0: inject correctable error. 1: inject uncorrectable error. For RTG4 only bit 0 is used and is used to disabled the EDAC logic.	High

112.5 Library dependencies

Table 1726 shows libraries used when instantiating the core (VHDL libraries).

*Table 1726.*Library dependencies

Library	Package	Imported unit(s)	Description
TECHMAP	GENCOMP	Constants	Technology constants

113 TAP - JTAG TAP Controller

113.1 Overview

JTAG TAP Controller provides an Test Access Port according to IEEE-1149 (JTAG) Standard. The core implements the Test Access Port signals, the synchronous TAP state-machine, a number of JTAG data registers (depending on the target technology) and an interface to user-defined JTAG data registers.

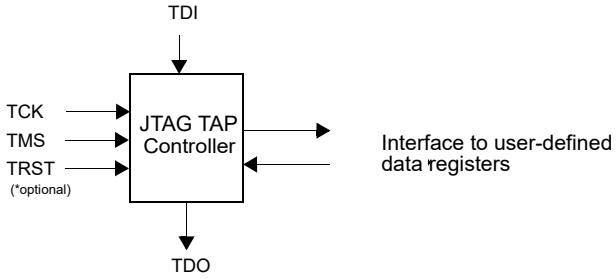


Figure 289. TAP controller block diagram

113.2 Operation

113.2.1 Generic TAP Controller

The generic TAP Controller implements JTAG Test Access Point interface with signals TCK, TMS, TDI and TDO, a synchronous state-machine compliant to the IEEE-1149 standard, JTAG instruction register and two JTAG data registers: bypass and device identification code register. The core is capable of shifting and updating the JTAG instruction register, putting the device into bypass mode (BYPASS instruction) and shifting out the devices identification number (IDCODE instruction). User-defined JTAG test registers are accessed through user-defined data register interface.

The access to the user-define test data registers is provided through the user-defined data register interface. The instruction in the TAP controller instruction register appears on the interface as well as shift-in data and signals indicating that the TAP controller is in Capture-Data-Register, Shift-Data-Register or Update-Data-Register state. Logic controlling user-defined data registers should observe value in the instruction register and TAP controller state signals in order to capture data, shift data or update data-registers.

JTAG test registers such as boundary-scan register can be interfaced to the TAP controller through the user data register interface.

113.3 Technology specific TAP controllers

The core instantiates technology specific TAP controller for Altera and Xilinx devices.

113.4 Registers

The core implements three JTAG registers: instruction, bypass and device identification code register.

113.5 Vendor and device identifiers

The core does not have vendor and device identifiers since it does not have AMBA interfaces.

113.6 Implementation

113.6.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). If the VHDL generic trsten is non-zero then the corer makes use of asynchronous reset. Otherwise synchronous reset is used.

113.7 Configuration options

Table 1727 shows the configuration options of the core (VHDL generics).

*Table 1727.*Configuration options

Generic	Function	Allowed range	Default
tech	Target technology	0 - NTECH	0
irlen	Instruction register length (generic tech only)	2 - 8	4
idcode	JTAG IDCODE instruction code(generic tech only)	0 - 255	9
manf	Manufacturer id. Appears as bits 11-1 in TAP controllers device identification register. Used only for generic technology. Default is Cobham Gaisler manufacturer id.	0 - 2047	804
part	Part number (generic tech only). Bits 27-12 in device id. reg.	0 - 65535	0
ver	Version number (generic tech only). Bits 31-28 in device id. reg.	0-15	0
trsten	Support optional TRST signal (generic tech only)	0 - 1	1
scantest	Enable scan test support	0 - 1	0
oepol	Polarity for TDOEN signal	0 - 1	1
tcknen	Support externally inverted TCK signal (generic tech only)	0 - 1	0

113.8 Signal descriptions

Table 1728 shows the interface signals of the core (VHDL ports).

*Table 1728.*Signal declarations

Signal name	Field	Type	Function	Active
TRST	N/A	Input	JTAG TRST signal*	Low
TCK	N/A	Input	JTAG clock*	-
TMS	N/A	Input	JTAG TMS signal*	High
TDI	N/A	Input	JTAG TDI signal*	High
TDO	N/A	Output	JTAG TDO signal*	High
User-defined data register interface				
TAPO_TCK	N/A	Output	TCK signal	High
TAPO_TDI	N/A	Output	TDI signal	High
TAPO_INST[7:0]	N/A	Output	Instruction in the TAP Ctrl instruction register	High
TAPO_RST	N/A	Output	TAP Controller in Test-Logic_Reset state	High
TAPO_CAPT	N/A	Output	TAP Controller in Capture-DR state	High
TAPO_SHFT	N/A	Output	TAP Controller in Shift-DR state	High
TAPO_UPD	N/A	Output	TAP Controller in Update-DR state	High
TAPO_XSEL1	N/A	Output	Xilinx User-defined Data Register 1 selected (Xilinx tech only)	High
TAPO_XSEL2	N/A	Output	Xilinx User-defined Data Register 2 selected (Xilinx tech only)	High
TAPI_EN1	N/A	Input	Enable shift-out data port 1 (TAPI_TDO1), when disabled data on port 2 is used	High
TAPI_TDO1	N/A	Input	Shift-out data from user-defined register port 1	High
TAPI_TDO2	N/A	Input	Shift-out data from user-defined register port 2	High
TAPO_NINST	N/A	Output	Instruction to be written into TAP Ctrl instruction register, only valid when TAPO_IUPD is high. (Generic tech only)	High
TAPO_IUPD	N/A	Output	TAP Controller in Update-IR state (Generic tech only)	High
TAPO_TCKN	N/A	Outpu	Inverted TCK signal	High
Additional signals				
TESTEN	N/A	Input	Test mode enable signal	High
TESTRST	N/A	Input	Test mode reset signal	Low
TESTOEN	N/A	Input	Test mode output-enable control	see oepol
TDOEN	N/A	Output	JTAG TDO enable signal*	see oepol
TCKN	N/A	Input	Inverted clock in (if tcknen generic is set)	

*) If the target technology is Xilinx or Altera the cores JTAG signals TCK, TCKN, TMS, TDI and TDO are not used. Instead the dedicated FPGA JTAG pins are used. These pins are implicitly made visible to the core through technology-specific TAP macro instantiation.

113.9 Library dependencies

Table 1729 shows libraries used when instantiating the core (VHDL libraries).

*Table 1729.*Library dependencies

Library	Package	Imported unit(s)	Description
TECHMAP	GENCOMP	Component	TAP Controller component declaration

113.10 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library techmap;
use gaisler.gencomp.all;

entity tap_ex is
  port (
    clk : in std_ulogic;
    rst : in std_ulogic;

    -- JTAG signals
    tck  : in std_ulogic;
    tms  : in std_ulogic;
    tdi  : in std_ulogic;
    tdo  : out std_ulogic
);
end;

architecture rtl of tap_ex is

signal gnd : std_ulogic;

signal tapo_tck, tapo_tdi, tapo_rst, tapo_capt : std_ulogic;
signal tapo_shft, tapo_upd : std_ulogic;
signal tapi_en1, tapi_tdo : std_ulogic;
signal tapo_inst : std_logic_vector(7 downto 0);


begin

 gnd <= '0';
 tckn <= not tck;


-- TAP Controller

  tap0 : tap (tech => 0)
    port map (rst, tck, tckn, tms, tdi, tdo, open, tapo_tck, tapo_tdi, tapo_inst,
      tapo_rst, tapo_capt, tapo_shft, tapo_upd, open, open,
       tapi_en1, tapi_tdo, gnd);


-- User-defined JTAG data registers

  ...


end;
```

114 GRTM - CCSDS/ECSS Telemetry Encoder

114.1 Overview

The CCSDS/ECSS/PSS Telemetry Encoder implements part of the Data Link Layer, covering the Protocol Sub-layer and the Frame Synchronization and Coding Sub-layer and part of the Physical Layer of the packet telemetry encoder protocol.

The operation of the Telemetry Encoder is highly programmable by means of control registers. The design of the Telemetry Encoder is highly configurable by means of VHDL generics.

The Telemetry Encoder comprises several encoders and modulators implementing the Consultative Committee for Space Data Systems (CCSDS) recommendations, European Cooperation on Space Standardization (ECSS) and the European Space Agency (ESA) Procedures, Standards and Specifications (PSS) for telemetry and channel coding. The Telemetry Encoder comprises the following:

- Packet Telemetry and/or Advanced Orbiting Systems (AOS) Encoder
- Reed-Solomon Encoder
- Turbo Encoder (future option)
- Pseudo-Randomiser (PSR)
- Non-Return-to-Zero Mark encoder (NRZ)
- Convolutional Encoder (CE)
- Split-Phase Level modulator (SP)
- Sub-Carrier modulator (SC)
- Clock Divider (CD)

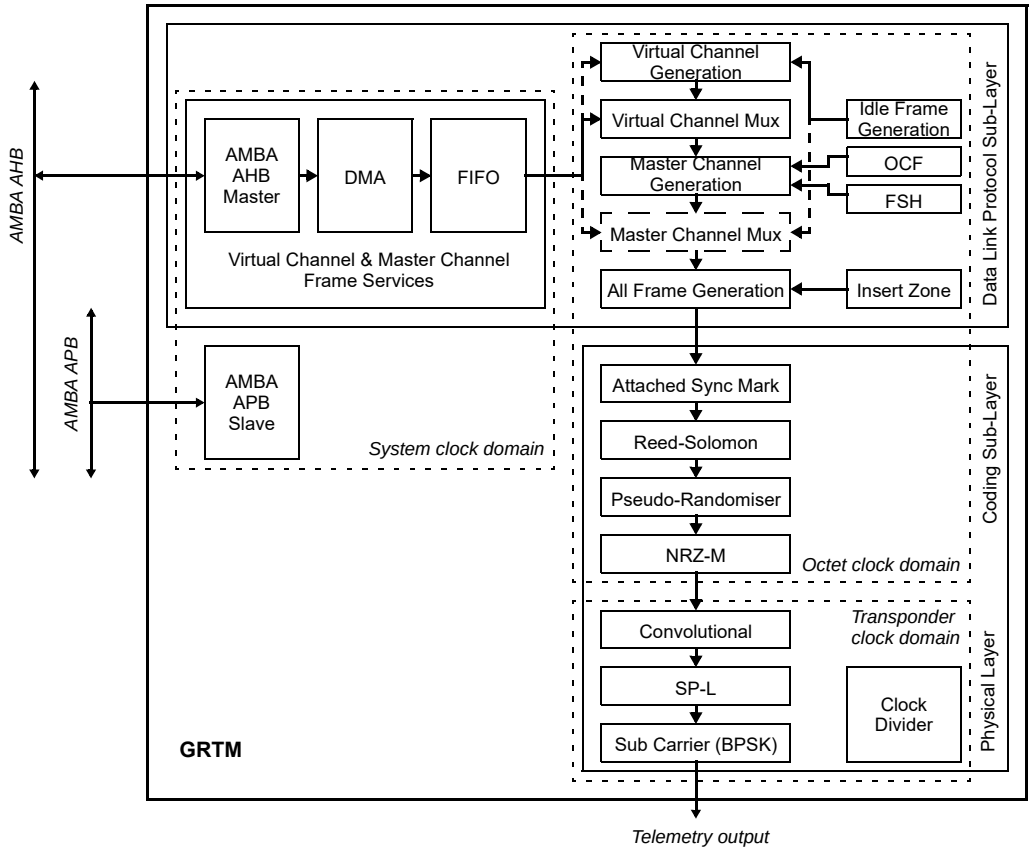


Figure 290. Block diagram

114.2 References

114.2.1 Documents

[CCSDS-131.0-B-2] TM Synchronization and Channel Coding

[CCSDS-132.0-B-1] TM Space Data Link Protocol

[CCSDS-133.0-B-1] Space Packet Protocol

[CCCSDS-732.0-B-2] AOS Space Data Link Protocol

[ECSS-E-ST-50-01C] Space engineering - Space data links - Telemetry synchronization and channel coding

[ECSS-E-ST-50-03C] Space engineering - Space data links - Telemetry transfer frame protocol

[ECSS-E-ST-50-05C] Space engineering - Radio frequency and modulation

[PSS-04-103] Telemetry channel coding standard

[PSS-04-105] Radio frequency and modulation standard

[PSS-04-106] Packet telemetry standard

114.2.2 Acronyms and abbreviations

AOS Advanced Orbiting Systems

ASM Attached Synchronization Marker

CCSDS Consultative Committee for Space Data Systems

CLCW Command Link Control Word

CRC Cyclic Redundancy Code

DMA Direct Memory Access

ECSS European Cooperation for Space Standardization

ESA European Space Agency

FECF Frame Error Control Field

FHEC Frame Header Error Control

FHP First Header Pointer

GF Galois Field

LFSR Linear Feedback Shift Register

MC Master Channel

NRZ Non Return to Zero

OCF Operational Control Field

PSR Pseudo Randomiser

PSS Procedures, Standards and Specifications

RS Reed-Solomon

SP Split-Phase

TE Turbo Encoder

TM Telemetry

VC Virtual Channel

114.3 Layers

114.3.1 Introduction

The Packet Telemetry (or simply Telemetry or TM) and Advanced Orbiting System (AOS) standards are similar in their format, with only some minor variations. The AOS part covered here is the down-link or transmitter, not the uplink or receiver.

The relationship between these standards and the Open Systems Interconnection (OSI) reference model is such that the OSI Data Link Layer corresponds to two separate layer, namely the Data Link Protocol Sub-layer and Synchronization and Channel Coding Sub-Layer. The OSI Data Link Layer is covered here.

The OSI Physical Layer is also covered here to some extended, as specified in [ECSS-E-ST-50-05C] and [PSS-04-105].

The OSI Network Layer or higher layers are not covered here.

114.3.2 Data Link Protocol Sub-layer

The Data Link Protocol Sub-layer differs somewhat between TM and AOS. Differences are pointed out where needed in the subsequent descriptions.

The following functionality is not implemented in the core:

- Packet Processing
- Bitstream Processing (applies to AOS only)

The following functionality is implemented in the core:

- Virtual Channel Generation (for Idle Frame generation only)
- Virtual Channel Multiplexing (for Idle Frame generation only)
- Master Channel Generation (applies to Packet Telemetry only)
- Master Channel Multiplexing (including Idle Frame generation)
- All Frame Generation

114.3.3 Synchronization and Channel Coding Sub-Layer

The Synchronization and Channel Coding Sub-Layer does not differ between TM and AOS.

The following functionality is implemented in the core:

- Attached Synchronization Marker
- Reed-Solomon coding
- Turbo coding (future option)
- Pseudo-Randomiser
- Convolutional coding

114.3.4 Physical Layer

The Physical Layer does not differ between TM and AOS.

The following functionality is implemented in the core:

- Non-Return-to-Zero modulation
- Split-Phase modulation
- Sub-Carrier modulation

114.4 Data Link Protocol Sub-Layer

114.4.1 Physical Channel

The configuration of a Physical Channel covers the following parameters:

- Transfer Frame Length (in number of octets)
- Transfer Frame Version Number

Note that there are other parameters that need to be configured for a Physical Channel, as listed in section 114.4.8, covering the All Frame Generation functionality.

The Transfer Frame Length can be programmed by means of the DMA length register.

The Transfer Frame Version Number can be programmed by means of a register, and can take one of two legal values: 00b for Telemetry and 01b for AOS.

114.4.2 Virtual Channel Frame Service

The Virtual Channel Frame Service is implemented by means of a DMA interface, providing the user with a means for inserting Transfer Frames into the Telemetry Encoder. Transfer Frames are automatically fetched from memory, for which the user configures a descriptor table with descriptors that point to each individual Transfer Frame. For each individual Transfer Frame the descriptor also provides means for bypassing functions in the Telemetry Encoder. This includes the following:

- Virtual Channel Counter generation can be enabled in the Virtual Channel Generation function (this function is normally only used for Idle Frame generation but can be used for the Virtual Channel Frame Service when sharing a Virtual Channel)
- Master Channel Counter generation can be bypassed in the Master Channel Generation function (TM only)
- Frame Secondary Header (FSH) generation can be bypassed in the Master Channel Generation function (TM only)
- Operational Control Field (OCF) generation can be bypassed in the Master Channel Generation function (TM only)
- Frame Error Header Control (FECH) generation can be bypassed in the All Frame Generation function (AOS only)
- Insert Zone (IZ) generation can be bypassed in the All Frame Generation function (AOS only)
- Frame Error Control Field (FECF) generation can be bypassed in the All Frame Generation function
- A Time Strobe can be generated for the Transfer Frame.

Note that the above features can only be bypassed for each Transfer Frame, the overall enabling of the features is done for the corresponding functions in the Telemetry Encoder, as described in the subsequent sections.

The detailed operation of the DMA interface is described in section 114.8.

114.4.3 Virtual Channel Generation

The Virtual Channel Generation function is used to generate the Virtual Channel Counter for Idle Frames as described hereafter. The function can however also be enabled for any Transfer Frame inserted via the Virtual Channel Frame Service described above, allowing a Virtual Channel to be shared between the two services. In this case the Virtual Channel Counter, the Extended Virtual Channel Counter (only for TM, as defined for ECSS and PSS, including the complete Transfer Frame Secondary Header) and the Virtual Channel Counter Cycle (only for AOS) fields will be inserted and incremented automatically when enabled as described hereafter.

114.4.4 Virtual Channel Multiplexing

The Virtual Channel Multiplexing Function is used to multiplex Transfer Frames of different Virtual Channels of a Master Channel. Virtual Channel Multiplexing in the core is performed between two sources: Transfer Frames provided through the Virtual Channel Frame Service and Idle Frames. Note that multiplexing between different Virtual Channels is assumed to be done as part of the Virtual Channel Frame Service outside the core.

The Virtual Channel Frame Service user interface is described above. The Idle Frame generation is described hereafter.

Idle Frame generation can be enabled and disabled by means of a register. The Spacecraft ID to be used for Idle Frames is programmable by means of a register. The Virtual Channel ID to be used for Idle Frames is programmable by means of a register.

Master Channel Counter generation for Idle Frames can be enabled and disabled by means of a register (only for TM). Note that it is also possible to generate the Master Channel Counter field as part of the Master Channel Generation function described in the next section. When Master Channel Counter generation is enabled for Idle Frames, then the generation in the Master Channel Generation function is bypassed.

The Virtual Channel Counter generation for Idle Frames is always enabled (both for TM and AOS) and generated in the Virtual Channel Generation function described above.

Extended Virtual Channel Counter generation for Idle Frames can be enabled and disabled by means of a register (only for TM, as defined for ECSS and PSS). This includes the complete Transfer Frame Secondary Header.

Virtual Channel Counter Cycle generation for Idle Frames can be enabled and disabled by means of a register (only for AOS).

If Frame Secondary Header generation is enabled in the Master Channel Generation function described in the next section, it can be bypassed for Idle Frames, programmable by means of a register. This allows VC_FSH or MC_FSH realization.

If Operation Control Field generation is enabled in the Master Channel Generation function described in the next section, it can be bypassed for Idle Frames, programmable by means of a register. This allows VC_OCF or MC_OCF realization.

114.4.5 Master Channel Generation

The Master Channel Counter can be generated for all frames on a master channel (only for TM). It can be can be enabled and disabled by means of a register. The generation can also be bypassed for Idle Frames or Transfer Frames provided via the DMA interface.

The Frame Secondary Header (FSH) can be generated from a 128-bit register (only for TM). This can be done for all frames on an master channel (MC_FSH) or be bypassed for Idle Frames or Transfer Frames provided via the DMA interface, effectively implementing FSH on a per virtual channel basis (VC_FSH). The FSH length is programmable by means of a register.

The Operational Control Field (OCF) can be generated from a 32-bit register. This can be done for all frames on an master channel (MC_OCF) or be bypassed for Idle Frames or Transfer Frames provided via the DMA interface, effectively implementing OCF on a per virtual channel basis (VC_OCF).

114.4.6 Master Channel Frame Service

The Master Channel Frame Service user interface is equivalent to the previously described Virtual Channel Frame Service user interface, using the same DMA interface. The interface can thus be used for inserting both Master Channel Transfer Frame and Virtual Channel Transfer Frames.

114.4.7 Master Channel Multiplexing

The Master Channel Multiplexing Function is used to multiplex Transfer Frames of different Master Channels of a Physical Channel. Master Channel Multiplexing is performed between three sources: Master Channel Generation Service, Master Channel Frame Service and Idle Frames.

Bypassing all the functionality of the Master Channel Generation functionality described above effectively establishes the master channel frame service. The same holds for the Idle Frame generation described above, allowing the core to generate Idle Frame on the level of the Physical Channel.

114.4.8 All Frame Generation

The All Frame Generation functionality operates on all transfer frames of a Physical Channel. Each of the individual functions can be bypassed for each frame coming from the DMA interface or idle frame generation functionality.

The Frame Header Error Control (FHEC) generation can be enabled and disabled by means of a register (AOS only).

The Insert Zone can be generated from a 128-bit register (only for AOS). This can be done for all frames on an physical channel (MC_FSH) or be bypassed for Idle Frames or Transfer Frames provided via the DMA interface. The Insert Zone length is programmable by means of a register. Note that the Insert Zone and Frame Secondary Header functionality share the same resources, since they cannot be used simultaneously for a Physical Channel.

Frame Error Control Field (FECF) generation can be enabled and disabled by means of a register.

114.5 Synchronization and Channel Coding Sub-Layer

114.5.1 Attached Synchronization Marker

The 32-bit Attached Synchronization Marker is placed in front of each Transfer Frame as per [CCSDS-131.0-B-2] and [ECSS-E-ST-50-03C].

An alternative Attached Synchronization Marker for embedded data streams can also be used, its enabling and bit pattern being programmable via a configuration register.

114.5.2 Reed-Solomon Encoder

The CCSDS recommendation [CCSDS-131.0-B-2] and ECSS standard [ECSS-E-ST-50-03C] specify Reed-Solomon codes, one (255, 223) code and one (255, 239) code. The ESA PSS standard [PSS013] only specifies the former code. Although the definition style differs between the documents, the (255, 223) code is the same in all three documents. The definition used in this document is based on the PSS standard [PSS013].

The Reed-Solomon Encoder implements both codes.

The Reed-Solomon encoder is compliant with the coding algorithms in [CCSDS-131.0-B-2] and [ECSS-E-ST-50-03C]:

- there are 8 bits per symbol;
- there are 255 symbols per codeword;
- the encoding is systematic:
- for E=8 or (255, 239), the first 239 symbols transmitted are information symbols, and the last 16 symbols transmitted are check symbols;
- for E=16 or (255, 223), the first 223 symbols transmitted are information symbols, and the last 32 symbols transmitted are check symbols;
- the E=8 code can correct up to 8 symbol errors per codeword;

- the E=16 code can correct up to 16 symbol errors per codeword;
- the field polynomial is

$$f_{esa}(x) = x^8 + x^6 + x^4 + x^3 + x^2 + x + 1$$

- the code generator polynomial for E=8 is

$$g_{esa}(x) = \prod_{i=120}^{135} (x + \alpha^i) = \sum_{j=0}^{16} g_j \cdot x^j$$

  for which the highest power of x is transmitted first;
- the code generator polynomial for E=16 is

$$g_{esa}(x) = \prod_{i=112}^{143} (x + \alpha^i) = \sum_{j=0}^{32} g_j \cdot x^j$$

  for which the highest power of x is transmitted first;
- interleaving is supported for depth I = {1 to 8}, where information symbols are encoded as I codewords with symbol numbers $i + j*I$ belonging to codeword i {where $0 \leq i < I$ and $0 \leq j < 255$};
- shortened codeword lengths are supported;
- the input and output data from the encoder are in the representation specified by the following transformation matrix T_{esa}, where i_0 is transferred first

$$\begin{bmatrix} \iota_0 & \iota_1 & \iota_2 & \iota_3 & \iota_4 & \iota_5 & \iota_6 & \iota_7 \end{bmatrix} = \begin{bmatrix} \alpha_7 & \alpha_6 & \alpha_5 & \alpha_4 & \alpha_3 & \alpha_2 & \alpha_1 & \alpha_0 \end{bmatrix} \times \begin{bmatrix} 0 & 0 & 1 & 1 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 \\ 0 & 0 & 1 & 0 & 1 & 0 & 1 & 1 \\ 0 & 1 & 1 & 1 & 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 1 & 1 & 0 & 1 & 1 \end{bmatrix}$$

- the following matrix T^{-1}_{esa} specifying the reverse transformation

$$\begin{bmatrix} \alpha_7 & \alpha_6 & \alpha_5 & \alpha_4 & \alpha_3 & \alpha_2 & \alpha_1 & \alpha_0 \end{bmatrix} = \begin{bmatrix} \iota_0 & \iota_1 & \iota_2 & \iota_3 & \iota_4 & \iota_5 & \iota_6 & \iota_7 \end{bmatrix} \times \begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 \end{bmatrix}$$

- the Reed-Solomon output is non-return-to-zero level encoded.

The Reed-Solomon Encoder encodes a bit stream from preceding encoders and the resulting symbol stream is output to subsequent encoder and modulators. The encoder generates codeblocks by receiving information symbols from the preceding encoders which are transmitted unmodified while calculating the corresponding check symbols which in turn are transmitted after the information symbols. The check symbol calculation is disabled during reception and transmission of unmodified data not

related to the encoding. The calculation is independent of any previous codeblock and is perform correctly on the reception of the first information symbol after a reset.

Each information symbol corresponds to an 8 bit symbol. The symbol is fed to a binary network in which parallel multiplication with the coefficients of a generator polynomial is performed. The products are added to the values contained in the check symbol memory and the sum is then fed back to the check symbol memory while shifted one step. This addition is performed octet wise per symbol. This cycle is repeated until all information symbols have been received. The contents of the check symbol memory are then output from the encoder. The encoder is based on a parallel architecture, including parallel multiplier and adder.

The encoder can be configured at compile time to support only the E=16 (255, 223) code, only the E=8 (255, 239) code, or both. This is done with the *reed* VHDL generic. Only the selected coding schemes are implemented. The choice between the E=16 and E=8 coding can be performed during operation by means of a configuration register.

The maximum number of supported interleave depths I_{max} is selected at compile time with the *reed-depth* VHDL generic, the range being 1 to 8. For a specific instantiation of the encoder, the choice of any interleave depth ranging from 1 to the chosen I_{max} is supported during operation. The area of the encoder is minimized, i.e. logic required for a greater interleave depth than I_{max} is not unnecessarily included.

The interleave depth is chosen during operation by means of a configuration register.

114.5.3 Pseudo-Randomiser

The Pseudo-Randomiser (PSR) generates a bit sequence according to [CCSDS-131.0-B-2] and [ECSS-E-ST-50-03C] which is xor-ed with the data output of preceding encoders. This function allows the required bit transition density to be obtained on a channel in order to permit the receiver on ground to maintain bit synchronization.

The polynomial for the Pseudo-Randomiser is $h(x) = x^8+x^7+x^5+x^3+1$ and is implemented as a Fibonacci version (many-to-one implementation) of a Linear Feedback Shift Register (LFSR). The registers of the LFSR are initialized to all ones between Transfer Frames. The Attached Synchronization Marker (ASM) is not effected by the encoding.

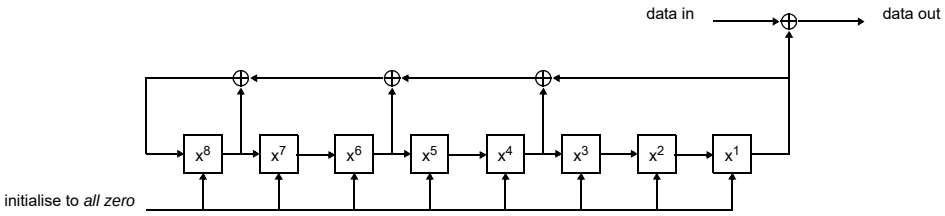


Figure 291. Pseudo-randomiser

114.5.4 Convolutional Encoder

The Convolutional Encoder (CE) implements two convolutional encoding schemes. The ESA PSS standard [PSS-04-103] specifies a basic convolutional code without puncturing. This basic convolutional code is also specified in the CCSDS recommendation [CCSDS-131.0-B-2] and ECSS standard [ECSS-E-ST-50-03C], which in addition specifies a punctured convolutional code.

The basic convolutional code has a code rate of 1/2, a constraint length of 7, and the connection vectors G1 = 1111001_b (171 octal) and G2 = 1011011_b (133 octal) with symbol inversion on output path, where G1 is associated with the first symbol output.

The punctured convolutional code has a code rate of 1/2 which is punctured to 2/3, 3/4, 5/6 or 7/8, a constraint length of 7, and the connection vectors G1 = 1111001_b (171 octal) and G2 = 1011011_b (133 octal) without any symbol inversion. The puncturing and output sequences are defined in [CCSDS-

131.0-B-2]. The encoder also supports rate 1/2 unpunctured coding with aforementioned connection vectors and no symbol inversion.

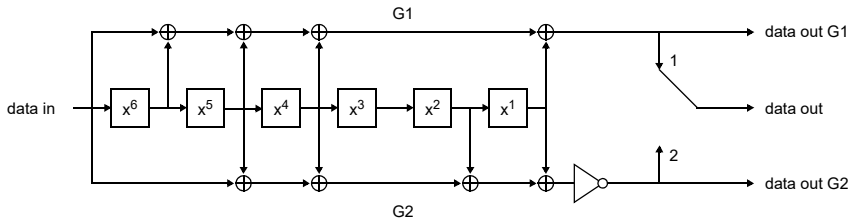


Figure 292. Unpuctured convolutional encoder

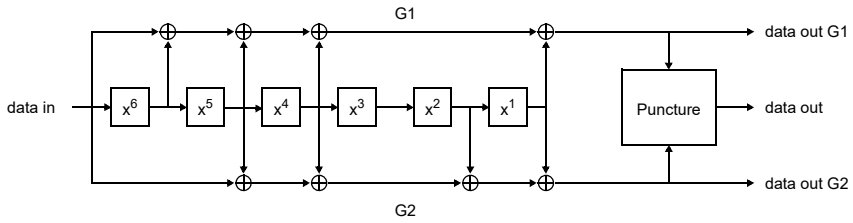


Figure 293. Punctured convolutional encoder

114.6 Physical Layer

114.6.1 Non-Return-to-Zero Mark encoder

The Non-Return-to-Zero Mark encoder (NRZ) encodes differentially a bit stream from preceding encoders according to [ECSS-E-ST-50-05C]. The waveform is shown in figure 294

Both data and the Attached Synchronization Marker (ASM) are affected by the coding. When the encoder is not enabled, the bit stream is by default non-return-to-zero level encoded.

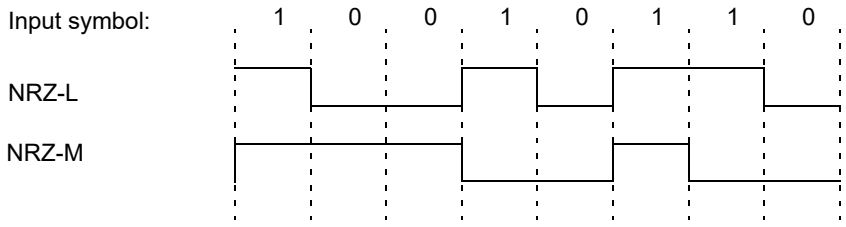


Figure 294. NRZ-L and NRZ-M waveform

114.6.2 Split-Phase Level modulator

The Split-Phase Level modulator (SP) modulates a bit stream (output symbols) from preceding encoders according (input symbols) to [ECSS-E-ST-50-05C]. The waveform is shown in figure 295.

Both data and the Attached Synchronization Marker (ASM) are effected by the modulator. The modulator will increase the output bit rate with a factor of two.

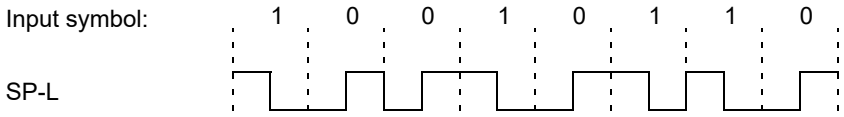


Figure 295. SP-L waveform

114.6.3 Sub-Carrier modulator

The Sub-Carrier modulator (SC) modulates a bit stream (output symbols) from preceding encoders according (input symbols) to [ECSS-E-ST-50-05C], which is Binary Phase Shift Key modulation (BPSK) or Phase Shift Key Square.

The sub-carrier modulation frequency is programmable. The symbol rate clock be divided to a degree 2^{15}. The divider can be configured during operation to divide the symbol rate clock frequency from 1/2 to $1/2^{15}$. The phase of the sub-carrier is programmable, selecting which phase 0^{o} or 180^{o} should correspond to a logical one on the input.

114.6.4 Clock Divider

The Clock Divider (CD) provides clock enable signals for the telemetry and channel encoding chain. The clock enable signals are used for controlling the bit rates of the different encoder and modulators.

The source for the bit rate frequency is the dedicated bit rate clock input. The bit rate clock input can be divided to a degree 2^{15}. The divider can be configured during operation to divide the bit rate clock frequency from 1/1 to $1/2^{15}$. In addition, the Sub-Carrier modulator can divide the above resulting clock frequency from 1/2 to $1/2^{15}$. The divider in the sub-carrier modulator can be used without enabling actual sub-carrier modulation, allowing division up to $1/2^{30}$.

The bit rate frequency is based on the output frequency of the last encoder in a coding chain, except for the sub-carrier modulator. No actual clock division is performed, since clock enable signals are used. No clock multiplexing is performed in the core.

The Clock Divider (CD) supports clock rate increases for the following encoders and rates:

- Convolutional Encoder (CE), 1/2, 2/3, 3/4, 5/6 and 7/8;
- Split-Phase Level modulator (SP-L), rate 1/2;
- Sub-Carrier modulator (SC), rate 1/2 to $1/2^{15}$.

The resulting symbol rate and telemetry rate are depended on what encoders and modulators are enabled. The following variables are used in the tables hereafter: f = input bit frequency, n = SYMBOLRATE+1 (GRTM physical layer register field +1), and m = SUBRATE+1 (physical layer register field +1), c = convolutional coding rate {1/2, 2/3, 3/4, 5/6, 7/8) (see CERATE field in GRTM coding sub-layer register).

*Table 1730.*Data rates without sub-carrier modulation (SUB=0)

Coding & Modulation	Telemetry rate	Convolutional rate	Split-Phase rate	Sub-carrier frequency	Output symbol rate	Output clock frequency
-	f / n / m	-	-	-	f / n / m	f / n / m
CE	(f / n / m) * c	f / n / m	-	-	f / n / m	f / n / m
SP-L	f / n / m / 2	-	f / n / m	-	f / n / m	f / n / m
CE + SP-L	(f / n / m / 2) * c	f / n / m / 2	f / n / m	-	f / n / m	f / n / m
For n = 1, no output symbol clock is generated, i.e. SYMBOLRATE register field equals 0. m should be an even number, i.e. SUBRATE register field should be uneven and > 0 to generate an output symbol clock with 50% duty cycle. If m > 1 then also n must be > 1, i.e. if SUBRATE register field is > 0 then SYMBOLRATE register field must be > 0.						

*Table 1731.*Data rates with sub-carrier modulation (SUB=1)

Coding & Modulation	Telemetry rate	Convolutional rate	Split-Phase rate	Sub-carrier frequency	Output symbol rate [1]	Output clock frequency
SC	f / n / m	-	-	f / n / 2	f / n	f / n
CE + SC	(f / n / m) * c	f / n / m	-	f / n / 2	f / n	f / n
SP-L+ SC	f / n / m / 2	-	f / n / m	f / n / 2	f / n	f / n
CE + SP-L + SC	(f / n / m / 2) * c	f / n / m / 2	f / n / m	f / n / 2	f / n	f / n

n = 1 or *m* = 1 are invalid settings for sub-carrier modulation, i.e SYMBOLRATE and SUBRATE register fields must be > 0.
m must be an even number, i.e. SUBRATE register field must be uneven and > 0.
m defines number of sub-carrier phases per input bit from preceding encoder or modulator.
Note 1: The output symbol rate for sub-carrier modulation corresponds to the rate of phases, not the frequency. Sub-carrier frequency is half the symbol rate.

114.7 Connectivity

The output from the Packet Telemetry and AOS encoder can be connected to:

- Reed-Solomon encoder
- Pseudo-Randomiser
- Non-Return-to-Zero Mark encoder
- Convolutional encoder
- Split-Phase Level modulator
- Sub-Carrier modulator

The input to the Reed-Solomon encoder can be connected to:

- Packet Telemetry and AOS encoder

The output from the Reed-Solomon encoder can be connected to:

- Pseudo-Randomiser
- Non-Return-to-Zero Mark modulator
- Convolutional encoder
- Split-Phase Level modulator
- Sub-Carrier modulator

The input to the Pseudo-Randomiser (PSR) can be connected to:

- Packet Telemetry and AOS encoder
- Reed-Solomon encoder

The output from the Pseudo-Randomiser (PSR) can be connected to:

- Non-Return-to-Zero Mark modulator
- Convolutional encoder
- Split-Phase Level modulator
- Sub-Carrier modulator

The input to the Non-Return-to-Zero Mark encoder (NRZ) can be connected to:

- Packet Telemetry and AOS encoder
- Reed-Solomon encoder
- Pseudo-Randomiser

The output from the Non-Return-to-Zero Mark encoder (NRZ) can be connected to:

- Convolutional encoder
- Split-Phase Level modulator
- Sub-Carrier modulator

The input to the Convolutional Encoder (CE) can be connected to:

- Packet Telemetry and AOS encoder
- Reed-Solomon encoder
- Pseudo-Randomiser
- Non-Return-to-Zero Mark encoder

The output from the Convolutional Encoder (CE) can be connected to:

- Split-Phase Level modulator
- Sub-Carrier modulator

The input to the Split-Phase Level modulator (SP) can be connected to:

- Packet Telemetry and AOS encoder
- Reed-Solomon encoder
- Pseudo-Randomiser
- Non-Return-to-Zero Mark encoder
- Convolutional encoder

The output from the Split-Phase Level modulator (SP) can be connected to:

- Sub-Carrier modulator

The input to the Sub-Carrier modulator (SC) can be connected to:

- Packet Telemetry and AOS encoder
- Reed-Solomon encoder
- Pseudo-Randomiser
- Non-Return-to-Zero Mark encode
- Convolutional encoder
- Split-Phase Level modulator

114.8 Operation

114.8.1 Introduction

The DMA interface provides a means for the user to insert Transfer Frames in the Packet Telemetry and AOS Encoder. Depending on which functions are enabled in the encoder, the various fields of the Transfer Frame are overwritten by the encoder. It is also possible to bypass some of these functions for each Transfer Frame by means of the control bits in the descriptor associated to each Transfer Frame. The DMA interface allows the implementation of Virtual Channel Frame Service and Master Channel Frame Service, or a mixture of both, depending on what functions are enabled or bypassed.

114.8.2 Descriptor setup

The transmitter DMA interface is used for transmitting transfer frames on the downlink. The transmission is done using descriptors located in memory.

A single descriptor is shown in table 1732 and 1733. The number of bytes to be sent is set globally for all transfer frames in the length field in register DMA length register. The the address field of the descriptor should point to the start of the transfer frame. The address must be word-aligned. If the interrupt enable (IE) bit is set, an interrupt will be generated when the transfer frame has been sent (this requires that the transmitter interrupt enable bit in the control register is also set). The interrupt will be generated regardless of whether the transfer frame was transmitted successfully or not. The wrap (WR) bit is also a control bit that should be set before transmission and it will be explained later in this section.

*Table 1732.*GRTM transmit descriptor word 0 (address offset 0x0)

31 16	15	14	13 10	9	8	7	6	5	4	3	2	1	0
RESERVED	UE	TS	0000	VCE	MCB	FSHB	OCFB	FHECB	IZB	FECFB	IE	WR	EN

31: 16	RESERVED
15	Underrun Error (UE) - underrun occurred while transmitting frame (status bit only)
14	Time Strobe (TS) - generate a time strobe for this frame
13: 10	RESERVED
9	Virtual Channel Counter Enable (VCE) - enable virtual channel counter generation (using the Idle Frame virtual channel counter)
8	Master Channel Counter Bypass (MCB) - bypass master channel counter generation (TM only)
7	Frame Secondary Header Bypass (FSHB) - bypass frame secondary header generation (TM only)
6	Operational Control Field Bypass (OCFB) - bypass operational control field generation
5	Frame Error Header Control Bypass (FECHB) - bypass frame error header control generation (AOS)
4	Insert Zone Bypass (IZB) - bypass insert zone generation (AOS)
3	Frame Error Control Field Bypass (FECFB) - bypass frame error control field generation
2	Interrupt Enable (IE) - an interrupt will be generated when the frame from this descriptor has been sent provided that the transmitter interrupt enable bit in the control register is set. The interrupt is generated regardless if the frame was transmitted successfully or if it terminated with an error.
1	Wrap (WR) - Set to one to make the descriptor pointer wrap to zero after this descriptor has been used. If this bit is not set the pointer will increment by 8. The pointer automatically wraps to zero when the 1 kB boundary of the descriptor table is reached.
0	Enable (EN) - Set to one to enable the descriptor. Should always be set last of all the descriptor fields.

*Table 1733.*GRTM transmit descriptor word 1 (address offset 0x4)

31 2	1 0
ADDRESS	RES

31: 2	Address (ADDRESS) - Pointer to the buffer area from where the packet data will be loaded.
1: 0	RESERVED

To enable a descriptor the enable (EN) bit should be set and after this is done, the descriptor should not be touched until the enable bit has been cleared by the core.

114.8.3 Starting transmissions

Enabling a descriptor is not enough to start a transmission. A pointer to the memory area holding the descriptors must first be set in the core. This is done in the transmitter descriptor pointer register. The address must be aligned to a 1 kByte boundary. Bits 31 to 10 hold the base address of descriptor area while bits 9 to 3 form a pointer to an individual descriptor.The first descriptor should be located at the base address and when it has been used by the core, the pointer field is incremented by 8 to point at

the next descriptor. The pointer will automatically wrap back to zero when the next 1 kByte boundary has been reached (the descriptor at address offset 0x3F8 has been used). The WR bit in the descriptors can be set to make the pointer wrap back to zero before the 1 kByte boundary.

The pointer field has also been made writable for maximum flexibility but care should be taken when writing to the descriptor pointer register. It should never be touched when a transmission is active.

The final step to activate the transmission is to set the transmit enable bit in the DMA control register. This tells the core that there are more active descriptors in the descriptor table. This bit should always be set when new descriptors are enabled, even if transmissions are already active. The descriptors must always be enabled before the transmit enable bit is set.

114.8.4 Descriptor handling after transmission

When a transmission of a frame has finished, status is written to the first word in the corresponding descriptor. The Underrun Error bit is set if the FIFO became empty before the frame was completely transmitted. The other bits in the first descriptor word are set to zero after transmission while the second word is left untouched. The enable bit should be used as the indicator when a descriptor can be used again, which is when it has been cleared by the core.

There are multiple bits in the DMA status register that hold transmission status.

The Transmitter Interrupt (TI) bit is set each time a DMA transmission of a transfer frame ended successfully. The Transmitter Error (TE) bit is set each time an DMA transmission of a transfer frame ended with an underrun error. For either event, an interrupt is generated for transfer frames for which the Interrupt Enable (IE) was set in the descriptor. The interrupt is maskable with the Interrupt Enable (IE) bit in the control register.

The Transmitter AMBA error (TA) bit is set when an AMBA AHB error was encountered either when reading a descriptor or when reading transfer frame data. Any active transmissions were aborted and the DMA channel was disabled. It is recommended that the Telemetry Encoder is reset after an AMBA AHB error. The interrupt is maskable with the Interrupt Enable (IE) bit in the control register.

The Transfer Frame Sent (TFS) bit is set whenever a transfer frame has been sent, independently if it was sent via the DMA interface or generated by the core. The interrupt is maskable with the Transfer Frame Interrupt Enable (TFIE) bit in the control register.

The Transfer Frame Failure (TFF) bit is set whenever a transfer frame has failed for other reasons, such as when Idle Frame generation is not enabled and no user Transfer Frame is ready for transmission, independently if it was sent via the DMA interface or generated by the core. The interrupt is maskable with the Transfer Frame Interrupt Enable (TFIE) bit in the control register.

The Transfer Frame Ongoing (TFO) bit is set when DMA transfers are enabled, and is not cleared until all DMA induced transfer frames have been transmitted after DMA transfers are disabled.

114.8.5 Interrupts

The Transfer Frame Sent (TFS) and Transfer Frame Failure (TFF) interrupts are maskable with the Transfer Frame Interrupt Enable (TFIE) bit in the DMA control register, and can be observed via the DMA status register.

The Transmitter Interrupt (TI), Transmitter Error (TE) and Transmitter AMBA Error (TA) interrupts are maskable with the Interrupt Enable (IE) bit in the DMA control register, and can be observed via the DMA status register.

The Time Strobe Interrupt (TSI) is maskable with the Transfer Frame Interrupt Enable (TFIE) bit in the DMA control register.

All interrupts except Time Strobe Interrupt (TSI) are output on interrupt number defined by *pirq* VHDL generic.

The Time Strobe Interrupt (TSI) is output on interrupt number defined by *pirq+1* VHDL generic.

114.9 Registers

The core is programmed through registers mapped into APB address space.

*Table 1734.*GRTM registers

APB address offset	Register
0x00	GRTM DMA Control register
0x04	GRTM DMA Status register
0x08	GRTM DMA Length register
0x0C	GRTM DMA Descriptor Pointer register
0x10	GRTM DMA Configuration register
0x14	GRTM DMA Revision register
0x20	GRTM DMA External VC Control & Status register
0x2C	GRTM DMA External VC Descriptor Pointer register
0x80	GRTM Control register
0x84	GRTM Status register (unused)
0x88	GRTM Configuration register
0x90	GRTM Physical Layer register
0x94	GRTM Coding Sub-Layer register
0x98	GRTM Attached Synchronization Marker
0xA0	GRTM All Frames Generation register
0xA4	GRTM Master Frame Generation register
0xA8	GRTM Idle Frame Generation register
0xC0	GRTM FSH/Insert Zone register 0
0xC4	GRTM FSH/Insert Zone register 1
0xC8	GRTM FSH/Insert Zone register 2
0xCC	GRTM FSH/Insert Zone register 3
0xD0	GRTM Operational Control Field register

114.9.1 GRTM DMA Control Register

*Table 1735.*0x00 - DCR - DMA control register

31 ... 5	4	3	2	1	0
RESERVED	TFIE	RST	TXRST	IE	EN
0	0	0	*	0	*
r	rw	rw	rw	rw	rw*

31: 5 RESERVED

4 Transfer Frame Interrupt Enable (TFIE) - enable telemetry frame sent (TFS) and failure (TFF) interrupt, and time strobe interrupt

3 Reset (RST) - reset DMA and telemetry transmitter

2 Reset Transmitter (TXRST) - reset telemetry transmitter

1 Interrupt Enable (IE) - enable DMA interrupt (TI), (TE) and (TA)

0 Enable (EN) - enable DMA transfers

114.9.2 GRTM DMA Status Register

*Table 1736.*0x04 - DSR - DMA status register

31 ... 8	7	6	5	4	3	2	1	0
RESERVED	TXSTAT	TXRDY	TFO	TFS	TFF	TA	TI	TE
0	0	0	*	0	0	0	*	*
r	r	r	r	wc	wc	wc	wc	wc

31: 8 RESERVED

7 Transmitter Reset Status (TXSTAT) - telemetry transmitter is in reset mode when set (read-only)

6 Transmitter Ready (TXRDY) - telemetry transmitter ready for operation after setting the TE bit in GRTM control register (read-only)

5 Transfer Frame Ongoing (TFO) - telemetry frames via DMA transfer are on-going (read-only)

4 Transfer Frame Sent (TFS) - telemetry frame interrupt, cleared by writing a logical 1

3 Transfer Frame Failure (TFF) - telemetry transmitter failure, cleared by writing a logical 1

2 Transmitter AMBA Error (TA) - DMA AMBA AHB error, cleared by writing a logical 1

1 Transmitter Interrupt (TI) - DMA interrupt, cleared by writing a logical 1

0 Transmitter Error (TE) - DMA transmitter underrun, cleared by writing a logical 1

114.9.3 GRTM DMA Length Register

Table 1737. 0x08 - DLR - DMA length register

31 ... 27	26 ... 16	15 ... 11	10 ... 0
RESERVED	LIMIT-1	RESERVED	LENGTH-1
0	*	0	*
r	rw	r	rw

31: 27 RESERVED

26: 16 Transfer Limit (LIMIT)- length-1 of data to be fetched by DMA before transfer starts.

Note: LIMIT must be equal to or less than LENGTH.

LIMIT must be equal to or less than FIFOSZ.

LIMIT must be equal to or larger than BLOCKSZ*2 for LENGTH > BLOCKSZ*2.

15: 11 RESERVED

10: 0 Transfer Length (LENGTH) - length-1 of data to be transferred by DMA

114.9.4 GRTM DMA Descriptor Pointer Register

Table 1738. 0x0C - DPR - DMA descriptor pointer register

31 10	9 3	2 0
BASE	INDEX	RESERVED
*	*	0
rw	rw	r

31: 10 Descriptor base (BASE) - base address of descriptor table

9: 3 Descriptor index (INDEX) - index of active descriptor in descriptor table

2: 0 Reserved - fixed to “00”

114.9.5 GRTM DMA Configuration Register (read-only)

Table 1739. 0x10 - DCF - DMA configuration register (read-only)

31 16	15 0
FIFOSZ	BLOCKSZ
*	*
r	r

31: 16 FIFO size (FIFOSZ) - size of FIFO memory in number of bytes (read-only)

15: 0 Block size (BLOCKSZ) - size of block in number of bytes (read-only)

114.9.6 GRTM DMA Revision Register (read-only)

Table 1740. 0x14 - DRR - DMA revision register (read-only)

31 22	21	20	19	18	17	16	15 8	7 0
RESERVED	AS	ASX	FIX	EX	IN	TIRQ	REVISION	SUB REVISION
0	-	-	*	*	*	*	*	0x04
r	r	r	r	r	r	r	r	r

31: 22 RESERVED

21 Autostart (AS) - Automatic start for telemetry

20 Autostart external (ASX) - Automatic start for external Virtual Channels

19 Fixed Frame Length (FIX) - Frame length fixed

18 External Virtual Channels (EX) - External Virtual Channels supported

17 Internal Virtual Channels (IN) - Internal Virtual Channels supported

16 Time Strobe Interrupt (TIRQ) - Separate time strobe interrupt supported

15: 8 REVISION - Main revision number

0x00: Initial release

7: 0 SUB REVISION - Sub revision number

0x00: Initial release

0x01: Added time interrupt, moved TXRDY bit, added TXSTAT bit, added this revision register

0x02: Added support for internal and external virtual channels

0x03: Added Master Channel Frame Counter value to master and idle frame generation registers

0x04: Added indicators for autostart of Telemetry and autostart of external Virtual Channels

114.9.7 GRTM DMA External VC Control & Status Register

*Table 1741.*0x20 - EUCS - DMA external VC control & status register

31 6	5	4 3	2	1	0
RESERVED	XTFO	RESERVED	XTI	XTE	XEN
0	*	0	*	*	*
r	r	r	wc	wc	rw

31: 6 RESERVED

5 External Transfer Frame Ongoing (XTFO) - telemetry frames via DMA transfer for external VC are on-going (read-only)

4: 3 RESERVED

2 External Transmitter Interrupt (XTI) - DMA interrupt for external VC, cleared by writing a logical 1

1 External Transmitter Error (XTE) - DMA transmitter underrun for external VC, cleared by writing a logical 1

0 External Enable (XEN) - enable DMA transfers for external VC (note that descriptor table is checked continuously till this bit is cleared).

114.9.8 GRTM DMA External VC Descriptor Pointer Register

Table 1742. 0x2C - EVDP - DMA external VC descriptor pointer register

31 10	9 3	2 0
BASE	INDEX	RESERVED
*	*	0
rw	rw	r

31: 10 Descriptor base (BASE) - base address of descriptor table

9: 3 Descriptor index (INDEX) - index of active descriptor in descriptor table

2: 0 Reserved - fixed to “00”

114.9.9 GRTM Control Register

Table 1743. 0x80 - CTRL - control register

31 1	0
RESERVED	TE
0	*
r	rw

31: 1 RESERVED

0: Transmitter Enable (TE) - enables telemetry transmitter (should be done after the complete configuration of the telemetry transmitter, including the LENGTH field in the GRTM DMA length register)

114.9.10GRTM Configuration Register (read-only)

Table 1744. 0x88 - CONF - configuration register (read-only)

31 23	22	21	20	19	18	17	16	15	14	13	12	11	10 9	8 6	5	4	3	2	1	0
RESERVED	OCFB	CIF	AOS	FHEC	IZ	MCG	FSH	IDLE	EVC	OCF	FECF	AASM	RS	RS DEPTH	TE	PSR	NRZ	CE	SP	SC
0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

31: 23	RESERVED
22	Operational Control Field Bypass (OCFB) - CLCW implemented externally, no OCF_SDU register
21	Encryption/Cipher Interface (CIF) - interface between protocol and channel coding sub-layers
20	Advanced Orbiting Systems (AOS) - AOS transfer frame generation implemented
19	Frame Header Error Control (FHEC) - frame header error control implemented, only if AOS also set
18	Insert Zone (IZ) - insert zone implemented, only if AOS also set
17	Master Channel Generation (MCG) - master channel counter generation implemented
16	Frame Secondary Header (FSH) - frame secondary header implemented
15	Idle Frame Generation (IDLE) - idle frame generation implemented
14	Extended VC Cntr (EVC) - extended virtual channel counter implemented (ECSS)
13	Operational Control Field (OCF) - CLCW implemented
12	Frame Error Control Field (FECF) - transfer frame CRC implemented
11	Alternative ASM (AASM) - alternative attached synchronization marker implemented
10: 9	Reed-Solomon (RS) - reed-solomon encoder implemented, “01” E=16, “10” E=8, “11” E=16 & 8
8: 6	Reed-Solomon Depth (RSDEPTH) - reed-solomon interleave depth -1 implemented
5	Turbo Encoder (TE) - turbo encoder implemented (reserved)
4	Pseudo-Randomiser (PSR) - pseudo-Randomiser implemented
3	Non-Return-to-Zero (NRZ) - non-return-to-zero - mark encoding implemented
2	Convolutional Encoding (CE) - convolutional encoding implemented
1	Split-Phase Level (SP) - split-phase level modulation implemented
0	Sub Carrier (SC) - sub carrier modulation implemented

114.9.11GRTM Physical Layer Register

Table 1745. 0x90 - PLR - physical layer register

31	30 16	15	14 0
SF	SYMBOLRATE	SCF	SUBRATE
‘*	*	*	*
rw	rw	rw	rw

31	Symbol Fall (SF) - symbol clock has a falling edge at start of symbol bit
30: 16	Symbol Rate (SYMBOLRATE) - symbol rate division factor - 1
15	Sub Carrier Fall (SCF) -sub carrier output start with a falling edge for logical 1
14: 0	Sub Carrier Rate (SUBRATE) - sub carrier division factor - 1

114.9.12GRTM Coding Sub-Layer Register

Table 1746. 0x94 - CSL - coding sub-layer register

31 20	19	18 17	16	15	14 12	11	10 8	7	6	5	4 2	1	0
RESERVED	CIF	CSEL	AASM	RS	RSDEPTH	RS8	RESERVED	PSR	NRZ	CE	CE RATE	SP	SC
0	*	*	*	*	*	*	0	*	*	*	*	*	*
r	rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw

31: 20	RESERVED
19	Encryption/Cipher Interface (CIF) - enable external encryption/cipher interface between sub-layers
18: 17	Clock Selection (CSEL) - selection of external telemetry clock source (application specific)
16	Alternative ASM (AASM) - alternative attached synchronization marker enable. When enabled the value from the GRTM Attached Synchronization Marker register is used, else the standardized ASM value 0x1ACFFC1D is used
15	Reed-Solomon (RS) - reed-solomon encoder enable
14: 12	Reed-Solomon Depth (RSDEPTH) - reed-solomon interleave depth -1
11	Reed-Solomon Rate (RS8) - ‘0’ E=16, ‘1’ E=8
10: 8	RESERVED
7	Pseudo-Randomiser (PSR) - pseudo-Randomiser enable
6	Non-Return-to-Zero (NRZ) - non-return-to-zero - mark encoding enable
5	Convolutional Encoding (CE) - convolutional encoding enable
4: 2	Convolutional Encoding Rate (CERATE): “00-” rate 1/2, no puncturing “01-” rate 1/2, punctured “100” rate 2/3, punctured “101” rate 3/4, punctured “110” rate 5/6, punctured “111” rate 7/8, punctured
1	Split-Phase Level (SP) - split-phase level modulation enable
0	Sub Carrier (SC) - sub carrier modulation enable

114.9.13GRTM Attached Synchronization Marker Register

Table 1747. 0x98 - ASM - attached synchronization marker register

31 0
ASM
*
rw

31: 0	Attached Synchronization Marker (ASM) - pattern for alternative ASM, (bit 31 MSB sent first, bit 0 LSB sent last) (The reset value is the standardized alternative ASM value 0x352EF853.)

114.9.14GRTM All Frames Generation Register

Table 1748. 0xA0 - AFGR - all frames generation register

31 22	21 17	16	15	14	13 12	11 0
RESERVED	FSH / IZ LENGTH	IZ	FECF	FHEC	VER	RESERVED
0	*	*	*	*	*	0
r	rw	rw	rw	rw	rw	r

31: 22 RESERVED
21: 17 Frame Secondary Header (TM) / Insert Zone (AOS) (FSH / IZ LENGTH) - length in bytes
16 Insert Zone (IZ) - insert zone enabled, only with AOS
15 Frame Error Control Field (FECF) - transfer frame CRC enabled
14 Frame Header Error Control (FHEC) - frame header error control enabled, only with AOS
13: 12 Version (VER) - Transfer Frame Version - “00” Packet Telemetry, “01” AOS
11: 0 RESERVED

114.9.15GRTM Master Frame Generation Register

Table 1749. 0xA4 - MFGR - master frame generation register

31 24	23 4	3	2	1	0
MCFC	RESERVED	MC	FSH	OCF	OW
*	0	*	*	*	*
r	r	rw	rw	rw	rw

31: 24 Master Channel Frame Counter (MCFC) - diagnostic read out (read only, TM only)
23: 4 RESERVED
3 Master Channel (MC) - enable master channel counter generation (TM only)
2 Frame Secondary Header (FSH) - enable MC_FSH for master channel (TM only)
1 Operation Control Field (OCF) - enable MC_OCF for master channel
0 Over Write OCF (OW) - overwrite OCF bits 16 and 17 when set

114.9.16GRTM Idle Frame Generation Register

Table 1750. 0xA8 - IFGR - idle frame generation register

31 24	23 22	21	20	19	18	17	16	15 10	9 0
IDLEMCFC	RESERVED	IDLE	OCF	EVC	FSH	VCC	MC	VCID	SCID
*	0	*	*	*	*	*	*	*	*
r	r	rw	rw	rw	rw	rw	rw	rw	rw

31: 24 Idle Master Channel Frame Counter (IDLEMCFC) - diagnostic read out (read only, TM only)

23: 22 RESERVED

21 Idle Frames (IDLE) - enable idle frame generation

20 Operation Control Field (OCF) - enable OCF for idle frames

19 Extended Virtual Channel Counter (EVC) - enable extended virtual channel counter generation for idle frames (TM only, ECSS)

18 Frame Secondary Header (FSH) - enable FSH for idle frames (TM only)

17 Virtual Channel Counter Cycle (VCC) - enable virtual channel counter cycle generation for idle frames (AOS only)

16 Master Channel (MC) - enable separate master channel counter generation for idle frames (TM only)

15: 10 Virtual Channel Identifier (VCID) - virtual channel identifier for idle frames

9: 0 Spacecraft Identifier (SCID) - spacecraft identifier for idle frames

114.9.17GRTM FSH / IZ Register 0, MSB

Table 1751. 0xC0 - FSH0 - FSH / IZ register 0, MSB

31 0
DATA
*
rw

31: 0 FSH / Insert Zone Data (DATA) - data (bit 31 MSB sent first)

Note: Writing to this register prevents the new FSH/Insert Zone data value to be transferred.

114.9.18GRTM FSH / IZ Register 1

Table 1752. 0xC4 - FSH1 - FSH / IZ register 1

31 0
DATA
*
rw

31: 0 FSH / Insert Zone Data (DATA) - data

114.9.19GRTM FSH / IZ Register 2

Table 1753. 0xC8 - FSH2 - FSH / IZ register 2

31 0
DATA
*
rw

31: 0 FSH / Insert Zone Data (DATA) - data

114.9.20GRTM FSH / IZ Register 3, LSB

Table 1754. 0xCC - FSH3 - FSH / IZ register 3, LSB

31	0
DATA	
*	
rw	

31: 0 FSH / Insert Zone Data (DATA) - data (bit 0 LSB sent last)

Note: Writing to this registers enables the new FSH/Insert Zone data value to be transferred.

114.9.21GRTM OCF Register

Table 1755. 0x00 - OCF - OCF register

31	0
CLCW	
*	
rw	

31: 0 Operational Control Field (OCF) - CLCW data (bit 31 MSB, bit 0 LSB)

114.10 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x030. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

114.11 Configuration options

Table 1756 shows the configuration options of the core (VHDL generics).

*Table 1756.*Configuration options

Generic name	Function	Allowed range	Default
hindex	AHB master index	0 - NAHBMST-1	0
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	ADDR field of the APB BAR	0 - 16#FFF#	0
pmask	MASK field of the APB BAR	0 - 16#FFF#	16#FFF#
pirq	Interrupt line used by core	0 - NAHBIRQ-1	0
memtech	Memory technology	0 to NTECH	0
ft	Enable fault-tolerance against SEU errors	0 - 2	0
blocksize	Block size (in number of bytes)	16 to 512	512
fifosize	FIFO size (in number of bytes)	32 to 4096	4096
fixedsize	Fixed Transfer Frame Length	0 - 1	0
framelength	Default Transfer Frame Length	0 - 4095	0
txlimit	Default Limit size	0 - 4095	0
nsync	Level of synchronization	1 - 2	2
exconf	External reset configuration	0 - 1	0
autostart	Automatic start of Telemetry	0 - 1	0
internal	Support for internal Virtual Channels	0 - 1	1

*Table 1756.*Configuration options

Generic name	Function	Allowed range	Default
external	Support for external Virtual Channels 1 = support external virtual channels 2 = support external virtual channels, autostart external virtual channels 3 = support external virtual channels, stand alone operation (autostart external virtual channels, never stop)	0 - 3	0
externaladdr	Default base address for external Virtual Channels	-	16#000#
resync	Resynchronization of internal constants	0 - 1	0
altasm	Alternative Attached Synchronization Marker	0 - 1	1
aos	Advanced Orbiting System (AOS)	0 - 1	1
fhec	Frame Header Error Control, AOS only	0 - 1	1
insertzone	Insert Zone, AOS only	0 - 1	1
mcgf	Master Channel Generation Function	0 - 1	1
fsh	Frame Secondary Header	0 - 1	1
idle	Idle Frame Generation	0 - 1	1
idleextvccntr	Extended Virtual Channel Counter, Idle Frames	0 - 1	1
ocf	Operation Control Field (2 equals external bypass)	0 - 2	1
fecf	Frame Error Control Field	0 - 1	1
cipher	Encryption / Cipher Interface	0-1	0
reed	Reed-Solomon, 1- E=16, 2 - E=8, 3 - E=8 & 16	0 - 3	3
reeddepth	Reed-Solomon Interleave Depth, maximum	1 - 8	8
turbo	Reserved	0	0
pseudo	Pseudo-Randomiser encoding	0 - 1	1
mark	Non-Return-to-Zero Mark modulation	0 - 1	1
conv	Convolutional coding	0 - 1	1
split	Split-Phase Level modulation	0 - 1	1
sub	Sub-Carrier modulation	0 - 1	1
timeirq	Separate time strobe interrupt	0 - 1	0
synchronous	0 = octet clock derived from transponder clock, separate clock domain 1 = octet clock equals the transponder clock, same clock domain	0 - 1	0
syncassert	0 = combinatorial (asynchronous) assertion of internal reset signal 1= sequential (synchronous) assertion of internal reset signal	0 - 1	0

114.12 Signal descriptions

Table 1757 shows the interface signals of the core (VHDL ports).

*Table 1757.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
TMI	BITLOCK	Input	Bit Lock	High
	RFAVAIL		RF Available	High
	OCF_SDU[0:31]		OCF_SDU Bypass	-
	CIPHER		Encryption/ Cipher Interface	-
	EXREQUEST		External VC Request	High
	CONF		External configuration	-
TMO	TIME	Output	Time strobe	High
	SYNC		ASM indicator	High
	FRAME		Frame indicator	High
	SERIAL		Serial bit data	High
	CLOCK		Serial bit data clock	High
	DATA [0:7]		Parallel data, octet	High
	STROBE		Parallel data strobe	High
	CLKSEL[0:1]		External clock selection	-
	FRAMELSB[0:1]		MC Counter least significant bits	-
	CIPHER		Encryption/ Cipher Interface	-
	SCID[0:9]		SCID setting	-
	OCF		OCF setting	High
	FECF		FECF setting	High
	EXENABLE		External VC enable	High
	EXGRANT		External VC grant	High
	EXREADY		External VC ready	High
TCLK	N/A	Input	Transponder clock	-
OCLKO	N/A	Output	Octet clock output	-
OCLKI	N/A	Input	Octet clock input	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
AHBMI	*	Input	AMB master input signals	-
AHBMO	*	Output	AHB master output signals	-

* see GRLIB IP Library User's Manual

114.13 Signal definitions and reset values

The signals and their reset values are described in table 1758.

*Table 1758.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
bitlock	Input	Bit Lock	High	-
rfavail	Input	RF Available	High	-
time	Output	Time strobe	High	Logical 0
sync	Output	ASM indicator	High	Logical 0
frame	Output	Frame indicator	High	Logical 0
serial	Output	Serial bit data	-	-
clock	Output	Serial bit data clock	High	Logical 0
data[0:7]	Output	Parallel data, octet	-	-
strobe	Output	Parallel data strobe	High	Logical 0

114.14 Timing

The timing waveforms and timing parameters are shown in figure 296 and are defined in table 1759.

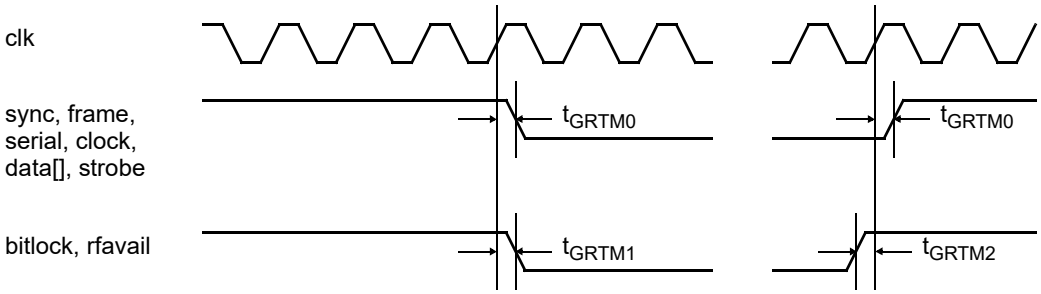


Figure 296. Timing waveforms

*Table 1759.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{GRTM0}	clock to output delay	rising *clk* edge	TBD	TBD	ns
t_{GRTM1}	input to clock hold	rising *clk* edge	-	-	ns
t_{GRTM2}	input to clock setup	rising *clk* edge	-	-	ns

Note: The inputs are re-synchronized inside the core. The signals do not have to meet any setup or hold requirements.

114.15 Library dependencies

Table 1760 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1760.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
TMTC	TMTC_TYPES	Signals, component	Component declaration

115 GRTM_DESC - CCSDS/ECSS Telemetry Encoder - Descriptor

115.1 Overview

The CCSDS/ECSS/PSS Telemetry Encoder Descriptor implements an automatic descriptor handler for external Telemetry Virtual Channels implemented in hardware (Telemetry Encoder Virtual Channel Generation function), not requiring software support.

115.2 Operation

115.2.1 Introduction

Warning: software should not read or write the descriptor table. All interaction is performed automatically by hardware.

The bandwidth is allocated equally between the external Telemetry Virtual Channels. Note that the descriptor table will be continuously checked by the Telemetry Encoder, even when all descriptors have their Enable (EN) bit cleared. This will go on until the External Enable (XEN) bit in the Telemetry Encoder is cleared by software.

115.2.2 Descriptor definition

A single descriptor is shown in table 1761 and 1762.

Table 1761. Transmit descriptor word 0 (address offset 0x0)

31 16	15	14	13 10	9	8	7	6	5	4	3	2	1	0
RESERVED	UE	TS	0000	VCE	MCB	FSHB	OCFB	FHECB	IZB	FECFB	IE	WR	EN

31: 16	RESERVED
15	Underrun Error (UE) - underrun occurred while transmitting frame (status bit only)
14	Time Strobe (TS) - generate a time strobe for this frame (static 0)
13: 10	RESERVED
9	Virtual Channel Counter Enable (VCE) - enable virtual channel counter generation (using the Idle Frame virtual channel counter) (static 0)
8	Master Channel Counter Bypass (MCB) - bypass master channel counter generation (TM only) (static 0)
7	Frame Secondary Header Bypass (FSHB) - bypass frame secondary header generation (TM only) (static 0)
6	Operational Control Field Bypass (OCFB) - bypass operational control field generation (static 0)
5	Frame Error Header Control Bypass (FECHB) - bypass frame error header control generation (AOS) (static 0)
4	Insert Zone Bypass (IZB) - bypass insert zone generation (AOS) (static 0)
3	Frame Error Control Field Bypass (FECFB) - bypass frame error control field generation (static 0)
2	Interrupt Enable (IE) - an interrupt will be generated when the frame from this descriptor has been sent provided that the transmitter interrupt enable bit in the control register is set. (static 0)
1	Wrap (WR) - Set to one to make the descriptor pointer wrap to zero after this descriptor has been used. If this bit is not set the pointer will increment by 8. The pointer automatically wraps to zero when the 1 kB boundary of the descriptor table is reached. (Set to 1 for last descriptor entry, otherwise static 0).
0	Enable (EN) - Set to one to enable the descriptor. Should always be set last of all the descriptor fields. (Automatically set an cleared by hardware)

Table 1762. Transmit descriptor word 1 (address offset 0x4)

31	2	1	0
ADDRESS			RES

31: 2 Address (ADDRESS) - Pointer to the buffer area from where the packet data will be loaded.

1: 0 RESERVED

115.3 Registers

None.

115.4 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x084. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

115.5 Configuration options

Table 1763 shows the configuration options of the core (VHDL generics).

*Table 1763.*Configuration options

Generic name	Function	Allowed range	Default
hindex	Selects which AHB select signal (HSEL) will be used to access the memory.	0 to NAHBMAX-1	0
haddr	ADDR field of the AHB BAR	0 to 16#FFF#	0
hmask	MASK field of the AHB BAR	0 to 16#FFF#	16#FFF#
channels	Number of Virtual Channels	power of 2	2
frames	Number of frames per Virtual Channel	2 -	2

115.6 Signal descriptions

Table 1764 shows the interface signals of the core (VHDL ports).

*Table 1764.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
VCRI	-	Input	Virtual Channel Request Interface	-
VCRO	-	Output		-
DI	-	Input	Descriptor Interface	-
DO	-	Output		-
AHBI	*	Input	AMB master input signals	-
AHBO	*	Output	AHB master output signals	-

* see GRLIB IP Library User's Manual

115.7 Signal definitions and reset values

None.

115.8 Timing

None.

115.9 Library dependencies

Table 1765 shows the libraries used when instantiating the core (VHDL libraries).

Table 1765. Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
TMTC	TMTC_TYPES	Signals, component	Component declaration
TMTC	GRTM_PKG	Signals, component	Component declaration

116 GRTM_VC - CCSDS/ECSS Telemetry Encoder - Virtual Channel Generation

116.1 Overview

The CCSDS/ECSS/PSS Telemetry Encoder Virtual Channel Generation function implements:

- Transfer Frame Primary Header insertion
- Transfer Frame Data Field insertion (with support for different lengths due to OCF and FECF)
- First Header Pointer (FHP) handling and insertion

The function keeps track of the number of octets received and the packet boundaries in order to calculated the First Header Pointer (FHP). The data are stored in pre-allocated slots in the buffer memory comprising complete Transfer Frames. The module fully supports the FHP generation and does not require any alignment of the packets with the Transfer Frame Data Field boundary.

The data input format can be CCSDS Space Packet [CCSDS-133.0-B-1] or any user-defined datablock. Data is input via a separate Virtual Channel Generation function input interface.

The function communicates with the Telemetry Encoder Virtual Channel Frame Service by means of a buffer memory space. The buffer memory space allocated to the Virtual Channel is treated as a circular buffer. The buffer memory space is accessed by means of a AMBA AHB master interface.

116.2 Registers

None.

116.3 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x085. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

116.4 Configuration options

Table 1766 shows the configuration options of the core (VHDL generics).

*Table 1766.*Configuration options

Generic name	Function	Allowed range	Default
hindex	Selects which AHB select signal (HSEL) will be used to access the memory.	0 to NAHBMAX-1	0
index	Channel index		0
id	0-7: Virtual Channel Identifier > 7: Virtual Channel Identifier is picked from the DYNVCID input.		0
roomsize	Packet size for ready signalling		0
frames	Number of frames		2
framepitch	Distance between consequtive frames		2048
frameoffset	Offset for all frames		4096
framelength	Frame length (transmitted)		1115
frameaddress	Start address of frames		16#000#

116.5 Signal descriptions

Table 1767 shows the interface signals of the core (VHDL ports).

*Table 1767.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
FECF	N/A	Input	Frame Error Control Field	High
OCF	N/A	Input	Operational Control Field	High
SCID	N/A	Input	Spacecraft Identifier	-
VCII	-	Input	Virtual Channel Input Interface	-
VCIO	-	Output		-
VCRI	-	Input	Virtual Channel Request Interface	-
VCRO	-	Output		-
AHBI	*	Input	AMB master input signals	-
AHBO	*	Output	AHB master output signals	-
DYNVCID	N/A	Input	Dynamic Virtual Channel Identifier to be used instead of the id generic in transfer frame generation if id > 7	-

* see GRLIB IP Library User's Manual

116.6 Signal definitions and reset values

None.

116.7 Timing

None.

116.8 Library dependencies

Table 1768 shows the libraries used when instantiating the core (VHDL libraries).

Table 1768. Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
TMTC	TMTC_TYPES	Signals, component	Component declaration
TMTC	GRTM_PKG	Signals, component	Component declaration

117 GRTM_PAHB - CCSDS/ECSS Telemetry Encoder - Virtual Channel Generation Input - AMBA

117.1 Overview

The Telemetry Encoder Virtual Channel Generation function input interface implements an interfaces towards the automatic Virtual Channel Generation function of the Telemetry Encoder (also called external Virtual Channels). Space Packets or any other user-defined data block can be input.

Data is transferred to the Virtual Channel Generation function by writing to the AMBA AHB slave interface, located in the AHB I/O area. Writing is only possible when the packet valid delimiter is asserted, else the access results in an AMBA access error. It is possible to transfer one, two or four bytes at a time, following the AMBA big-endian convention regarding send order. The last written data can be read back via the AMBA AHB slave interface. Data are output as octets to the Virtual Channel Generation function.

In the case the data from a previous write access has not been fully transferred over the interface, a new write access will result in an AMBA retry response. The progress of the interface can be monitored via the AMBA APB slave interface. An interrupt is generated when the data from the last write access has been transferred. An interrupt is also generated when the ready for input packet indicator is asserted.

The core incorporates status and monitoring functions accessible via the AMBA APB slave interface. This includes:

- Busy and ready signalling from Virtual Channel Generation function
- Interrupts on ready for new word, or ready for new packet (size 518 octets (set with *roomsize* VHDL generic))

117.2 Interrupts

Two interrupts are implemented by the interface:

Index:Name:Description:

0 NOT BUSYReady for a new data (word, half-word or byte)

1 READYReady for new packet

The interrupts are configured by means of the *pirq* VHDL generic.

117.3 Registers

The core is programmed through registers mapped into APB address space.

*Table 1769.*GRTM_PAHB registers

APB address offset	Register
16#004#	Status Register
16#008#	Control Register

117.3.1 Status Register (R)

*Table 1770.*0x04 - STAT - Status Register

31 2	1	0
RESERVED	BUSY	READY
0	*	*
r	r	r

1: BUSY Not ready for new input, busy with octet
0: READY Ready for new packet of maximum size

All bits are cleared to 0 at reset.

117.3.2 Control Register (R/W)

*Table 1771.*0x08 - CTRL - Control Register

31 10	9	8	7 3	2	1	0
RESERVED	BUSYEN	READYEN	RESERVED	VALID	RST	EN
0	0	0	0	0	0	0
r	rw	rw	r	rw*	rw	rw

8: BUSYEN
9: READYENEnable ready for packet interrupt when 1
2: VALID Packet valid delimiter, packet valid when 1, in-between packets when 0 (read-only)
1: RST Reset complete core when 1
0: EN Enable interface when 1

All bits are cleared to 0 at reset. Note that RST is read back as 0.

117.4 AHB I/O area

Data to be transferred to the Virtual Channel Generation function is written to the AMBA AHB slave interface which implements a AHB I/O area. See [GRLIB] for details.

Note that the address is not decoded by the core. Address decoding is only done by the AMBA AHB controller, for which the I/O area location and size is configured by means of the *ioaddr* and *iomask* VHDL generics. It is possible to transfer one, two or four bytes at a time, following the AMBA big-endian convention regarding send order. The last written data can be read back via the AMBA AHB slave interface. Data are output as octets on the Virtual Channel Generation interface.

*Table 1772.*AHB I/O area - data word definition

31 24	23 16	15 8	7 0
DATA [31:24]	DATA [23:16]	DATA [15:8]	DATA [7:0]

*Table 1773.*AHB I/O area - send order

Transfer size	Address offset	DATA [31:24]	DATA [23:16]	DATA [15:8]	DATA [7:0]	Comment
Word	0	first	second	third	last	Four bytes sent
Halfword	0	first	last	-	-	Two bytes sent
	2	-	-	first	last	Two bytes sent
Byte	0	first	-	-	-	One byte sent
	1	-	first	-	-	One byte sent
	2	-	-	first	-	One byte sent
	3	-	-	-	first	One byte sent

117.5 Vendor and device identifiers

The module has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x088. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

117.6 Configuration options

Table 1774 shows the configuration options of the core (VHDL generics).

*Table 1774.*Configuration options

Generic name	Function	Allowed range	Default
hindex	AHB master index.	1 - NAHBSLV-1	0
ioaddr	Addr field of the AHB IO bar.	0 - 16#FFF#	0
iomask	Mask field of the AHB IO bar.	0 - 16#FFF#	16#F00#
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	Addr field of the APB bar.	0 - 16#FFF#	0
pmask	Mask field of the APB bar.	0 - 16#FFF#	16#FFC#
pirq	Interrupt line used by the GRTM_PAHB.	0 - NAHBIRQ-1	0
syncrst	Only synchronous reset	0, 1	1
roomsize	Size of packet		518

117.7 Signal descriptions

Table 1775 shows the interface signals of the core (VHDL ports).

*Table 1775.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
AHBI	*	Input	AMB slave input signals	-
AHBO	*	Output	AHB slave output signals	-

* see GRLIB IP Library User's Manual

117.8 Library dependencies

Table 1776 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1776.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
TMTC	TMTC_Types	Signals, component	Component declarations, signals.
TMTC	GRTM_PKG	Signals, component	Component declaration

118 GRTM_PW - CCSDS/ECSS Telemetry Encoder - Virtual Channel Generation Input - PacketWire

The PacketWire (PW) interface to a telemetry encoder is a simple bit synchronous protocol. There is one PacketWire interface for each telemetry Virtual Channel.

The data can be any CCSDS supported packets. The interface comprises three input signals; bit data, bit clock and packet delimiter. There is an additional discrete signal provided for busy signalling.

Data should consist of multiples of eight bits otherwise the last bits will be lost. The input packet delimiter signal is used to delimit packets. It should be asserted while a packet is being input, and de-asserted in between. In addition, the input packet delimiter signal should define the octet boundaries in the input data stream, the first octet explicitly and the following octets each subsequent eight bit clock cycles.

The interface is based on the de facto standard PacketWire interface used by the *European Space Agency* (ESA). At the time of writing there were no relevant documents available from the *European Cooperation for Space Standardization* (ECSS).

118.1 Operation

The PacketWire interface accepts and generates the waveform format shown in figure 297.

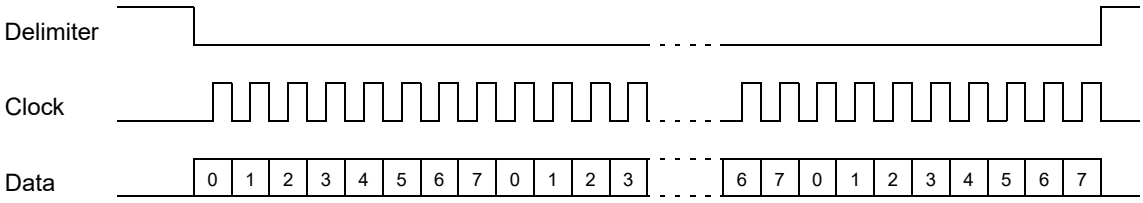


Figure 297. Synchronous bit serial waveform

The PacketWire protocol follows the CCSDS transmission convention, the most significant bit being sent first. Transmitted data should consist of multiples of eight bits otherwise the last bits will be lost. The input message delimiter port is used to delimit messages (packets). It should be asserted while a message is being input, and deasserted in between. In addition, the message delimiter port should define the octet boundaries in the data stream, the first octet explicitly and the following octets each subsequent eight bit clock cycles.

The maximum receiving input baud rate is defined as half the frequency of the system clock input. There is no lower limit for the input bit rate in the receiver.

The handshaking between the PacketWire links and the interface is implemented with a busy port. When a message is sent, the busy signal on the PacketWire input link will be asserted as soon as the input interface is not ready to receive more data, it will then be deasserted as soon as the interface is ready to receive the next octet. This gives the transmitter ample time to stop transmitting after the completion of an octet and wait for the busy signal deassertion before starting the transmission of the next octet. The handshaking is continued through out the message.

118.2 Signal definitions and reset values

The signals and their reset values are described in table 1777.

*Table 1777.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
*pw*valid_n*	Input	Delimiter: This input port is the message delimiter for the input interface. It should be deasserted between messages.	Low	-
*pw*clk*	Input	Bit clock: This input port is the PacketWire bit clock. The receiver registers are clocked on the rising edge.	Rising	-
*pw*data*	Input	Data: This input port is the serial data input for the interface. Data are sampled on the rising *pw*clk* edge when *pw*valid_n* is asserted.	-	-
*pw*busy*	Output	Not ready for octet: This port indicates whether the receiver is ready to receive one octet.	High	Logical 0

118.3 Timing

The timing waveforms and timing parameters are shown in figure 298 and are defined in table 1778.

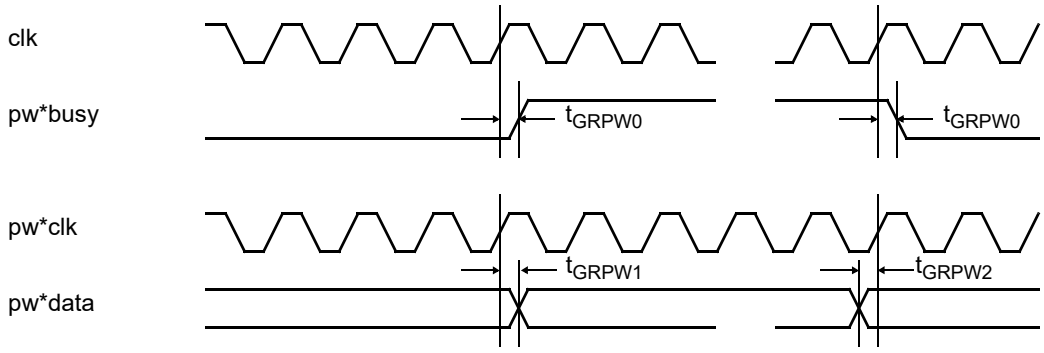


Figure 298. Timing waveforms

*Table 1778.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{GRPW0}	clock to output delay	rising *clk* edge	TBD	TBD	ns
t_{GRPW1}	input to clock hold	rising *pw*clk* edge	TBD	-	ns
t_{GRPW2}	input to clock setup	rising *pw*clk* edge	TBD	-	ns
t_{GRPW3}	*pw*valid_n* to *pw*clk* edge	rising *pw*clk* edge	TBD	-	ns
t_{GRPW3}	*pw*valid_n* de-asserted period	-	TBD		system clock periods

119 GRTM_UART - CCSDS/ECSS Telemetry Encoder - Virtual Channel Generation Input - UART

The PacketAsynchronous (PA) interface to a telemetry encoder is a simple bit asynchronous protocol. There can be one bit asynchronous interface per telemetry Virtual Channel.

The protocol has a fixed or programmable baud rate, 1 start bit, 8 data bits, optional odd parity, 1 or 2 stop bits, with a BREAK command for message delimiting (sending 13 bits of logical zero).

The data can be any CCSDS supported packet. The interface comprises one input signal with bit asynchronous data. There are two additional discrete signals provided for busy signalling.

119.1 Asynchronous bit serial data format

The asynchronous bit serial interface complies to the data format defined in [EIA 232]. It also complies to the data format and waveform shown in table 1779 and figure 299. The interface is independent of the transmitted data contents. Positive logic is considered for the data bits. The number of stop bits can optionally be either one or two. The parity bit can be optionally included.

Asynchronous bit serial format	start	D0	D1	D2	D3	D4	D5	D6	D7	parity	stop	stop
	first	*lsb*							*msb*			*last*
General data format $i = \{0, n\}$		8**i*+7	8**i*+6	8**i*+5	8**i*+4	8**i*+3	8**i*+2	8**i*+1	8**i*			
		last							*first*			

*Table 1779.*Asynchronous bit serial data format

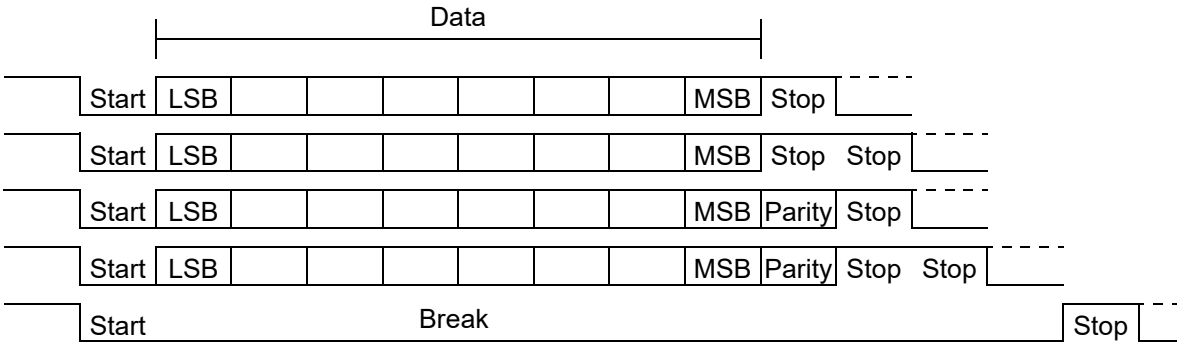


Figure 299. Asynchronous bit serial protocol / waveform

The handshaking for the bit asynchronous links is implemented with a busy signal. When a message is sent, the busy signal on the input link will be asserted as soon as the input interface is not ready to receive more data, it will then be deasserted as soon as the interface is ready to receive the next octet. The handshaking is continued through out the packet.

119.2 Registers

The core has not user accessible registers.

119.3 Vendor and device identifiers

The core has has neither a vendor identifier nor a device identifier.

119.4 Configuration options

Table 1780 shows the configuration options of the core (VHDL generics).

*Table 1780.*Configuration options

Generic	Function	Description	Allowed range	Default
gSystemClock	System frequency	[Hz]	Integer	8000000
gBaud	Baud rate	[Baud]	Integer	115200
gProgrammable	Baud rate	Enables programmable baud rate when 1	0 - 1	0
syncreset	Sync reset	Synchronous reset when 1	0 - 1	0

119.5 Signal descriptions

Table 1781 shows the interface signals of the core (VHDL ports).

*Table 1781.*Signal descriptions

Signal name	Field	Type	Function	Description	Active
RSTN	N/A	Input	Reset		Low
CLK	N/A	Input	Clock		-
IGNOREPARITY	N/A	Input		Generate odd parity, else none	High
TWOSTOPBITS	N/A	Input		Generate two stop bits, else one	High
BAUDTHRESH-OLD	N/A	Input		Sets baud rate, if gProgrammable is 1	-
VCIO	*	Output		Virtual Channel Interface	-
VCII	*	Input		Virtual Channel Interface	-
TMUART	N/A	Input		Data	-
TMBUSYN	N/A	Output		Not ready for octet	Low
TMRDY	N/A	Output		Ready for packet	High

119.6 Signal definitions and reset values

The signals and their reset values are described in table 1782.

*Table 1782.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
*tm*data*	Input	Data: This input port is the serial data input for the interface. Data are sampled on the rising *pw*clk* edge when *pw*valid_n* is asserted.	-	-
*tm*busyn*	Output	Not ready for octet: This port indicates whether the receiver is ready to receive one octet.	Low	Logical 1
*tm*ready*	Output	Not ready for octet: This port indicates whether the receiver is ready to receive one octet.	High	Logical 0

119.7 Timing

The timing waveforms and timing parameters are shown in figure 300 and are defined in table 1783.

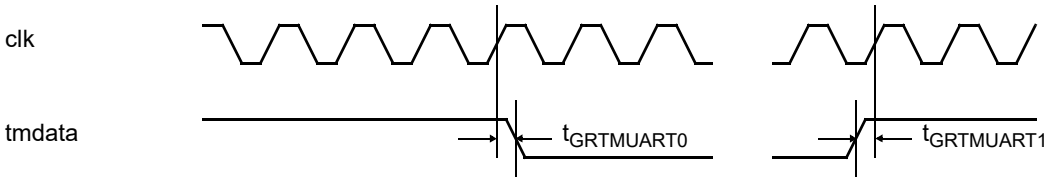


Figure 300. Timing waveforms

*Table 1783.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{GRTMUART0}$	hold from clock	rising *clk* edge	-	-	ns
$t_{GRTMUART1}$	setup to clock	rising *clk* edge	-	-	ns

Note: The inputs are re-synchronized internally. The signals do not have to meet any setup or hold requirements.

120 GEFFE - CCSDS/ECSS Telemetry Encoder - Geffe Generator

120.1 Overview

The Geffe Generator implements a simple stream based cipher to encrypt Telemetry Transfer Frames.

The Geffe generator acts as a keystream generator. It uses three Linear Feed-back Shift Registers (LFSR) combined in a nonlinear manner. Two of the LFSRs (LFSR1 and LFSR2) are inputs into a multiplexer, and the third LFSR (LFSR0) controls the output of the multiplexer. Suppose LFSR0, LFSR1, and LFSR2 are the outputs of the three LFSRs, then the generator output is as follows:

```
b(x) = (LFSR0 and LFSR1) xor (not LFSR0 and LFSR2)
```

The generator is programmable, in terms of the power of the polynomials used (i.e. stages or states), the polynomials (POLY0, POLY1 and POLY2) and the initialization values (INIT0, INIT1 and INIT2), individually for each of the three LFSRs.

The Geffe Generator interfaces with the GRTM CCSDS Telemetry Encoder via its external encryption/cipher interface located between the Data Link Protocol Sub-Layer and the Synchronization and Channel Coding Sub-Layer. This corresponds to Link Layer Security Option A according CCSDS definitions (see CCSDS 350.0-G-2 *"The application of CCSDS protocols to secure systems"*). This corresponds to Link Layer Security Option A according to CCSDS 350.0-G-2, i.e. between Logical Link Sublayer and Coding Sublayer.

The implementation of security services is below the Transfer Frame level. The full Transfer Frame is encrypted after any other necessary security services are applied. The generated keystream is XOR-ed bit wise with the Transfer Frame bit stream, starting with first bit transmitted. The LFSRs are only shifted when there is data to be encrypted. The shift is made after each bit has been encrypted.

The three LFSRs are initialized once when the generator is enabled, with the contents of the programmable INIT0, INIT1 and INIT2 register fields, respectively.

The LFSRs initialization value can be optionally XOR-ed with the Transfer Frame Master Channel Counter (only supported for hardware implemented Master Channel Counter in telemetry encoder), according to the following formula:

```
LFSR(31:24) = INIT(31:24) xor MCC(0:7),  LFSR(23:16) = INIT(23:16) xor MCC(0:7)
LFSR(15: 8) = INIT(15: 8) xor MCC(0:7),  LFSR( 7: 0) = INIT( 7: 0) xor MCC(0:7)
```

where INIT(31:0) is the programmable register field (bit 31 being the most significant), and MCC(0:7) is the Transfer Frame Master Channel Counter (bit 0 being the most significant).

The keystream is optionally restarted for each Transfer Frame, i.e. the LFSRs are re-initialized.

The Attached Synchronization Marker remains in plaintext to enable the ground systems to delimit the Channel Access Service Data Units. Also the Reed-Solomon check symbols are in plaintext, i.e. error detection & correction before decrypting begins.

Encryption for Idle Transfer Frames can be optionally disabled (only supported for hardware implemented Idle Transfer Frame generation in telemetry encoder).

A Cyclic Redundancy Code (CRC) can be optionally calculated over the encrypted data according to CCSDS/ECSS algorithm and replace the Frame Error Control Field (FECF) when transmitted in a Transfer Frame (only supported for hardware implemented CRC calculation in telemetry encoder).

The Geffe generator provides support for the following programmable functions:

- Enable/disable encryption on Transfer Frame boundaries
- Initialize LFSRs in-between Transfer Frames
- Initialize LFSRs taking Master Channel Counter value into account
- Skip encryption for Idle Transfer Frames
- Recalculate Cyclic Redundancy Code (CRC) and replace Frame Error Control Field (FECF)

120.2 Linear Feed-back Shift Registers

The three Linear Feed-back Shift Registers (LFSR) are Many-to-One implementation, i.e. Fibonacci version of LFRS. The One-to-Many implementation, i.e. Galois version of LFSR is not supported.

There are two mathematical representations for Fibonacci LFSR:

- output has the highest power, h(x)
- output has the lowest power, l(x)

The implementation of the Geffe Generator supports both representations. Note that both representations generate the same keystream.

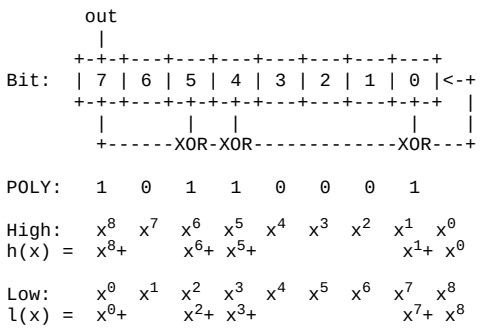
The LFSRs are always shifted to the left. The feedback is always entered to the right. The output bits corresponds to the leftmost set bits in the POLY fields in the polynomial configuration registers. The POLY field defined the feedback taps. The initialization values of the LFSRs is defined in the INIT fields in the polynomial initialization value configuration registers.

Note that the bit index of the configuration registers is not directly related to the polynomial powers. The interpretation of the bit index values depends on which of the above representations is assumed.

A first example of an LFSR configuration and the two possible interpretations is shown hereafter. The POLY field is set to 0x0000000B1. Since the leftmost bit set has index 7, the LFSR has 8 stages, and the output is taken from bit index 7, indicated with *out* in the figure.

Assuming that the output has the highest power, indicated with *High* and *h(x)*, the resulting polynomial is $h(x) = x^8 + x^6 + x^5 + x^1 + x^0$.

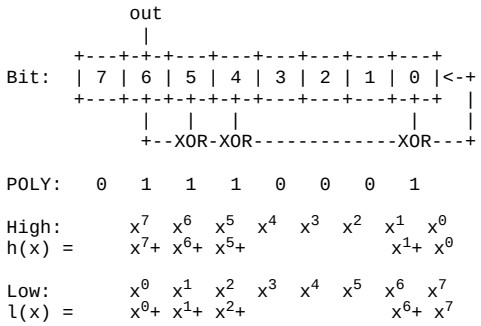
Assuming that the output has the highest power, indicated with *Low* and *l(x)*, the resulting polynomial is $l(x) = x^0 + x^2 + x^3 + x^7 + x^8$.



A second example of an LFSR configuration and the two possible interpretations is shown hereafter. The POLY field is set to 0x000000071. Since the leftmost bit set has index 6, the LFSR has 7 stages, and the output is taken from bit index 6, indicated with *out* in the figure.

Assuming that the output has the highest power, indicated with *High* and *h(x)*, the resulting polynomial is $h(x) = x^7 + x^6 + x^5 + x^1 + x^0$.

Assuming that the output has the highest power, indicated with *Low* and *l(x)*, the resulting polynomial is $l(x) = x^0 + x^1 + x^2 + x^6 + x^7$.



120.3 Connectivity

The connectivity of the Geffe Generator is tightly coupled to the functionality of the GRTM CCSDS Telemetry Encoder.

The input to the Geffe Generator can be connected to:

- Packet Telemetry and AOS encoder

The output from the Geffe Generator can be connected to:

- Reed-Solomon encoder
- Pseudo-Randomiser
- Non-Return-to-Zero Mark encoder
- Convolutional encoder
- Sub-Carrier modulator

120.4 Registers

The core is programmed through registers mapped into APB address space.

*Table 1784.*GEFFE registers

APB address offset	Register
0x00	GEFFE Control Register
0x10	GEFFE LFSR 0 Polynomial Configuration Register
0x14	GEFFE LFSR 1 Polynomial Configuration Register
0x18	GEFFE LFSR 2 Polynomial Configuration Register
0x20	GEFFE LFSR 0 Initialization Value Configuration Register
0x24	GEFFE LFSR 1 Initialization Value Configuration Register
0x28	GEFFE LFSR 2 Initialization Value Configuration Register

120.4.1 Control Register

*Table 1785.*0x00 - CTRL - GEFFE control register

31 13	12 8	7	6	5	4	3	2	1	0
RESERVED	LENGTH-1	ON	-	RI	MCC	IDLE	CRC	EN	RST
0	*	0		0	0	0	0	0	0
r	r	r		rw	rw	rw	rw	rw	rw

31: 13 RESERVED

12: 8 LFSR Length -1 (LENGTH-1) - the bit length of the implemented LFSR registers - 1 bit (read-only)

7 On-going (ON) - encryption of Transfer Frame is on-going when set, wait till cleared before changing ann configuration settings (read-only)

6 RESERVED

5 Re-initialize (RI) - when set, LFSRs are re-initialized in-between Transfer Frame (Reset value 0)

4 Master Channel Counter (MCC) - when set, LFSRs are initialized with the Transfer Frame Master Channel Counter value being XOR-ed with the INIT field values (Reset value 0)

3 Skip idle (IDLE) - when set, if an Idle Transfer Frame is transmitted, skip encryption (Reset value 0)

2 CRC replace (CRC) - when set, if FECF is transmitted in Transfer Frame, recalculates CRC value over encrypted data and replace FECF with the result (Reset value 0)

1 Enable (EN) - enable Geffe Generator when set (Reset value 0)

0 Reset (RST) - reset Geffe Generator when set. Does not reset configuration bits and polynomial and initialization registers. (Reset value 0)

120.4.2 LFSR Polymonial Configuration Registers 0 to 2

Table 1786. 0x10 - PcRn - GEFFE LFSR Polynomial Configuration Registers 0 to 2

31 0
POLY
0
rw

31: 0 LFSR Polynomial - Each bit in POLY corresponds to a tap in the LFSR. The LFSR is always shifted to the left. Feedback taps are always entered to the right, i.e. bit 0. The output bit corresponds to the leftmost set bit in POLY. Should not be changed while encryption is enabled. (Reset value all zero)

120.4.3 Initialization Value Configuration Registers 0 to 2

Table 1787. 0x20 - ICRn - GEFFE LFSR Initialization Value Configuration Registers 0 to 2

31 0
INIT
0
rw

31: 0 LFSR Initialization Value - The LFSR is initialized with this value, or optionally combined with the Transfer Frame Master Channel Counter value. Should not be changed while encryption is enabled. (Reset value all zero)

120.5 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x086. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

120.6 Configuration options

Table 1788 shows the configuration options of the core (VHDL generics).

*Table 1788.*Configuration options

Generic name	Function	Allowed range	Default
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	ADDR field of the APB BAR	0 - 16#FFF#	0
pmask	MASK field of the APB BAR	0 - 16#FFF#	16#FFF#
len	LFSR length	1 - 32	32

120.7 Signal descriptions

Table 1789 shows the interface signals of the core (VHDL ports).

*Table 1789.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
CI	CIPHER			
	ENABLE	Input	Encryption enabled from Telemetry Encoder	High
	DATA(0:7)		Parallel data, octet	-
	SYNC		ASM indicator	High
	FRAME		Frame indicator	High
	FECF		FECF/CRC indicator	High
	CHECK		Reed-Solomon checksymbol indicator	High
	TIME		Time strobe	High
	IDLE		Idle Transfer Frame indicator	High
	MCCNTR(0:7)		Transfer Frame Master Channel Counter	-
CO	CIPHER			
	ENABLE	Output	Unused	-
	DATA(0:7)		Parallel data, octet	-
	SYNC		ASM indicator	High
	FRAME		Frame indicator	High
	FECF		Unused	-
	CHECK		Reed-Solomon checksymbol indicator	High
	TIME		Time strobe	High
	IDLE		Unused	-
	MCCNTR(0:7)		Transfer Frame Master Channel Counter	-
OCLK	N/A	Input	Octet clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-

* see GRLIB IP Library User's Manual

120.8 Signal definitions and reset values

There are not external signals.

120.9 Timing

The are no external timing waveforms and timing parameters.

120.10 Library dependencies

Table 1790 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1790.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
TMTC	TMTC_TYPES	Signals, component	Component declaration

121 GRTMRX - CCSDS/ECSS Telemetry Receiver

121.1 Overview

The CCSDS/ECSS/PSS Telemetry Receiver implements part of the Data Link Layer, covering the Protocol Sub-layer and the Frame Synchronization and Coding Sub-layer and part of the Physical Layer of the packet telemetry protocol.

The operation of the Telemetry Receiver is highly programmable by means of control registers.

The Telemetry Receiver comprises several decoders and modulators implementing the Consultative Committee for Space Data Systems (CCSDS) recommendations, European Cooperation on Space Standardization (ECSS) and the European Space Agency (ESA) Procedures, Standards and Specifications (PSS) for telemetry and channel coding. The Telemetry Receiver comprises the following:

- Operation Control Field (OCF)
- Frame Error Control Field (FECF)
- Pseudo-De-Randomiser (PSR)
- Attached Sync Marker search (ASM)
- Non-Return-to-Zero Mark decoder (NRZ)
- Convolutional Quick-Look Decoder (CE)
- Split-Phase Level de-modulator (SP)
- Sub-Carrier de-modulator (SC)

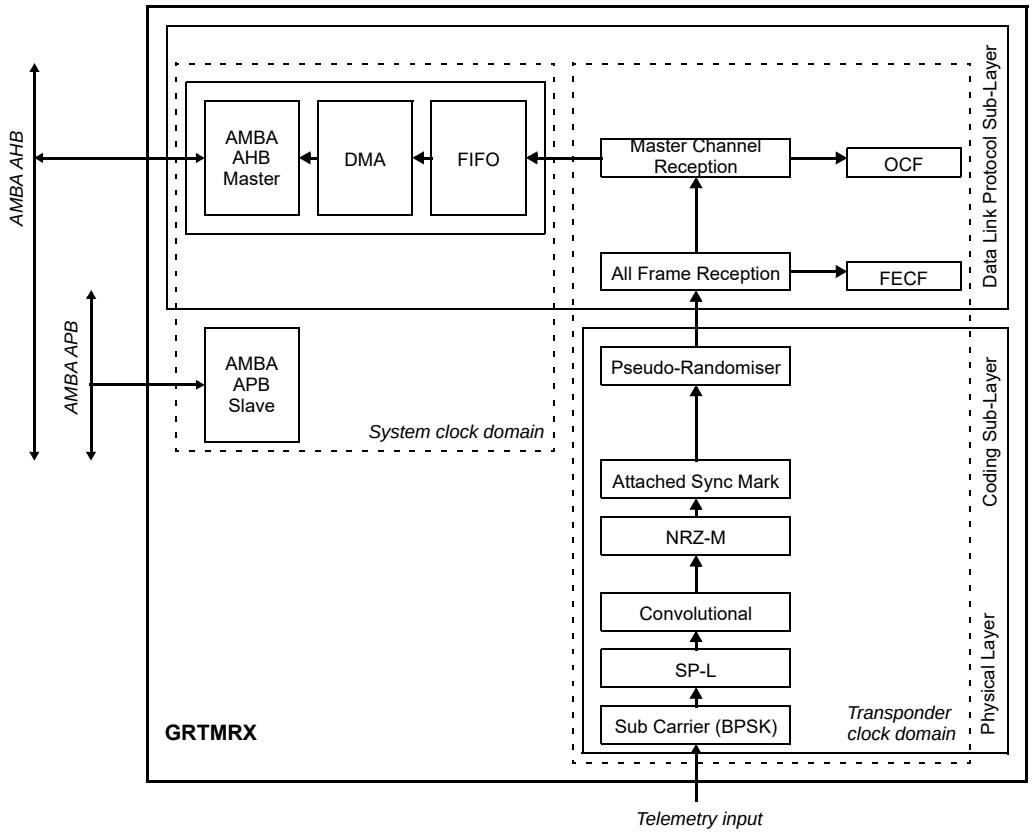


Figure 301. Block diagram

121.2 References

121.2.1 Documents

[C131] CCSDS 131.0-B-2 TM Synchronization and Channel Coding

[C132] CCSDS 132.0-B-1 TM Space Data Link Protocol

[C133] CCSDS 133.0-B-1 Space Packet Protocol

[C732] CCSDS 732.0-B-2 AOS Space Data Link Protocol

[ECSS01] ECSS-E-50-01C Space engineering - Space data links - Telemetry synchronization and channel coding

[ECSS03] ECSS-E-50-03C Space engineering - Space data links - Telemetry transfer frame protocol

[ECSS05] ECSS-E-50-05C Space engineering - Radio frequency and modulation

[PPS103] ESA PSS-04-103 Telemetry channel coding standard

[PPS105] ESA PSS-04-105 Radio frequency and modulation standard

[PPS106] ESA PSS-04-106 Packet telemetry standard

121.2.2 Acronyms and abbreviations

AOSAdvanced Orbiting Systems

ASMAttached Synchronization Marker

CCSDSConsultative Committee for Space Data Systems

CLCWCommand Link Control Word

CRCCyclic Redundancy Code

DMADirect Memory Access

ECSSEuropean Cooperation for Space Standardization

ESAEuropean Space Agency

FECFFrame Error Control Field

GF Galois Field

NRZNon Return to Zero

OCFOperational Control Field

PSR Pseudo Randomiser

PSS Procedures, Standards and Specifications

RS Reed-Solomon

SP Split-Phase

TE Turbo Encoder

TM Telemetry

121.3 Layers

121.3.1 Introduction

The Packet Telemetry (or simply Telemetry or TM) and Advanced Orbiting System (AOS) standards are similar in their format, with only some minor variations. The AOS part covered here is the down-link or transmitter, not the uplink or receiver.

The relationship between these standards and the Open Systems Interconnection (OSI) reference model is such that the OSI Data Link Layer corresponds to two separate layer, namely the Data Link Protocol Sub-layer and Synchronization and Channel Coding Sub-Layer. The OSI Data Link Layer is covered here.

The OSI Physical Layer is also covered here to some extended, as specified in [ECSS05] and [PPS105].

The OSI Network Layer or higher layers are not covered here.

121.3.2 Data Link Protocol Sub-layer

The following functionality is implemented in the core:

- Master Channel Reception / Virtual Channel Reception

  •Operation Control Field (OCF) extraction
- All Frame Reception:

  •Frame Error Control Field (FECF) extraction and check

  •Frame filtering on the four first received octets (of the Transfer Frame after ASM)

121.3.3 Synchronization and Channel Coding Sub-Layer

The following functionality is implemented in the core:

- Attached Synchronization Marker (ASM) search
- Pseudo de-randomiser
- Convolutional quick-look decoding

121.3.4 Physical Layer

The following functionality is implemented in the core:

- Non-Return-to-Zero de-modulation
- Split-Phase de-modulation
- Sub-Carrier de-modulation

121.4 Operation

121.4.1 Introduction

The DMA interface provides a means for the user to receive blocks of data of arbitrary length, normally this is Telemetry Transfer Frames, with ASM and optional Reed-Solomon checkbits.

121.4.2 Descriptor setup

The receiver DMA interface is used for receiving data on the downlink. The reception is done using descriptors located in memory.

A single descriptor is shown in tables 1791 through 1794.

The number of bits to be received is set globally. The the address field of the descriptor should point to the start of the transfer frame. The address must be word-aligned. If the interrupt enable (IE) bit is set, an interrupt will be generated when the transfer frame has been received (this requires that the interrupt enable bit in the control register is also set). The interrupt will be generated regardless of whether the transfer frame was received successfully or not. The wrap (WR) bit is also a control bit that should be set before reception and it will be explained later in this section.

*Table 1791.*GRTMRX descriptor word 0 (address offset 0x0)

31 16	15 11	10	9	8	7	6 3	2	1	0
LEN	RESERVED	ALOCK	INV	CERR	OV	RESERVED	WR	IE	EN

31: 16 (LEN) - received length in bytes (read only)

15: 11 RESERVED

10: ASM Lock (ALOCK) - (read only) Set to one when ASM search is in lock.

9: Inverted bit stream (INV) - (read only) Set to one when an inverted bit stream detected.

8: CRC Error (CERR) - (read only) Set to one when a CRC error was detected (speculative, only useful if FECF present in frame)

7: Overrun (OV) - (read only) Set to one when an overrun has occurred during reception.

6: 3 RESERVED

2: Wrap (WR) - Set to one to make the descriptor pointer wrap to zero after this descriptor has been used. If this bit is not set the pointer will increment by 16. The pointer automatically wraps to zero when the 16 kB boundary of the descriptor table is reached.

1: Interrupt Enable (IE) - an interrupt will be generated when the frame from this descriptor has been sent provided that the receiver interrupt enable bit in the control register is set. The interrupt is generated regardless if the frame was received successfully or if it terminated with an error.

0: Enable (EN) - Set to one to enable the descriptor. Should always be set last of all the descriptor fields.

*Table 1792.*GRTMRX descriptor word 1 (address offset 0x4)

31 2	1	0
ADDRESS	-	

31: 2 Address (ADDRESS) - Pointer to the buffer area to where data will be stored.

1: 0 RESERVED

*Table 1793.*GRTMRX descriptor word 2 (address offset 0x8)

31 0
STATUS0

31: 0 (STATUS0) - External status information

*Table 1794.*GRTMRX descriptor word 3 (address offset 0xC)

31 0
STATUS1

31: 0 (STATUS1) - External status information

To enable a descriptor the enable (EN) bit should be set and after this is done, the descriptor should not be touched until the enable bit has been cleared by the core.

121.4.3 Starting reception

Enabling a descriptor is not enough to start reception. A pointer to the memory area holding the descriptors must first be set in the core. This is done in the descriptor pointer register. The address must be aligned to a 16 kByte boundary. Bits 31 to 14 hold the base address of descriptor area while

bits 13 to 4 form a pointer to an individual descriptor. The first descriptor should be located at the base address and when it has been used by the core, the pointer field is incremented by 16 to point at the next descriptor. The pointer will automatically wrap back to zero when the next 16 kByte boundary has been reached. The WR bit in the descriptors can be set to make the pointer wrap back to zero before the 16 kByte boundary.

The pointer field has also been made writable for maximum flexibility but care should be taken when writing to the descriptor pointer register. It should never be touched when reception is active.

The final step to activate the reception is to set the enable bit in the DMA control register. This tells the core that there are more active descriptors in the descriptor table. This bit should always be set when new descriptors are enabled, even if reception is already active. The descriptors must always be enabled before the reception enable bit is set.

121.4.4 Descriptor handling after reception

When the reception of a frame has finished, status is written to the first word in the corresponding descriptor. The other bits in the first descriptor word are set to zero after reception. The enable bit should be used as the indicator when a descriptor can be used again, which is when it has been cleared by the core. Additionally, the last two words in the corresponding descriptor are written with external status information.

There are multiple bits in the DMA status register that hold status information.

The Receiver Interrupt (RI) bit is set each time a DMA reception ended successfully. The Receiver Error (RE) bit is set each time an DMA reception ended with an overrun error. For either event, an interrupt is generated for descriptor for which the Interrupt Enable (IE) was set. The interrupt is maskable with the Interrupt Enable (IE) bit in the control register.

The Receiver AMBA error (RA) bit is set when an AMBA AHB error was encountered either when reading a descriptor or when writing data. Any active reception was aborted and the DMA channel was disabled. It is recommended that the receiver is reset after an AMBA AHB error. The interrupt is maskable with the Interrupt Enable (IE) bit in the control register.

121.4.5 Demodulator clock recovery

Demodulators are provided, that support Split-Phase Level (SP) demodulation (SP), and Binary Phase Shift Key (BPSK) demodulation (or Phase Shift Key Square) as per [ECSS-E-ST-50-05C]. The demodulators can operate separately or in combination.

The demodulators can operate either with a bit serial clock input signal, or with just the bit serial data stream.

For the former, it is assumed that a bit serial clock input, which is synchronous with the bit serial data input, is provided. The demodulator can decode symbol rates up the system clock frequency.

For the latter, a bit serial clock signal can be re-generated locally for a bit serial data input that is Split-Phase-L (SP-L) and/or Sub-Carrier (SC) modulated. The clock recovery is enabled by setting the EN bit in the GRTMRX Demodulator register. With clock recovery, the demodulator can decode a bit serial data input where the symbol period has a duration of down to four times the system clock period. Note that when Sub Carrier (SC) modulation is used, a symbol corresponds to a single phase of the sub-carrier waveform, thus the sub-carrier frequency can be up to an eighth of the system clock frequency.

121.5 Registers

The core is programmed through registers mapped into APB address space.

*Table 1795.*GRTMRX registers

APB address offset	Register
0x00	GRTMRX DMA Control register
0x04	GRTMRX DMA Status register
0x08	GRTMRX DMA Descriptor Pointer register
0x80	GRTMRX Control register
0x84	GRTMRX Status register
0x88	GRTMRX Configuration register
0x8C	GRTMRX Size register
0x90	GRTMRX Physical Layer register
0x94	GRTMRX Coding Sub-Layer register
0x98	GRTMRX Attached Synchronization Marker register
0x9C	GRTMRX Attached Synchronization Marker Mask register
0xAC	GRTMRX Data Rate register
0xB0	GRTMRX Filter register
0xB4	GRTMRX Filter Mask register
0xD0	GRTMRX Operational Control Field register
0xD4	GRTMRX Frame Error Control Field register
0xD8	GRTMRX Demodulator register

121.5.1 GRTMRX DMA Control Register

*Table 1796.*0x00 - DCR - DMA control register

31	2	1	0
RESERVED		IE	EN
0		0	0
r		rw	rw

31: 2 RESERVED

1: Interrupt Enable (IE) - enable interrupts RA, RI, and RE

0: Enable (EN) - enable DMA transfers

121.5.2 GRTMRX DMA Status Register

*Table 1797.*0x04 - DSR - DMA status register

31	4	3	2	1	0
RESERVED		ACTIVE	RA	RI	RE
0		NR	0	0	0
r		r	wc	wc	wc

31: 4 RESERVED

3: Active (ACTIVE) - DMA access ongoing

2: Receiver AMBA Error (RA) - DMA AMBA AHB error, cleared by writing a logical 1

1: Receiver Interrupt (RI) - DMA interrupt, cleared by writing a logical 1

0: Receiver Error (RE) - DMA receiver error (e.g.underrun), cleared by writing a logical 1

121.5.3 GRTMRX DMA Descriptor Pointer Register

Table 1798. 0x08 - DPR - DMA descriptor pointer register

31	14	13	4	3	0
BASE		INDEX		RESERVED	
NR		NR		0	
rw		rw		r	

31: 14 Descriptor base (BASE) - base address of descriptor table

13: 4 Descriptor index (INDEX) - index of active descriptor in descriptor table

3: 0 Reserved - fixed to “0000”

121.5.4 GRTMRX Control Register

Table 1799. 0x80 - CTRL - control register

31	4	3	2	1	0
RESERVED		ScRST	RST	RxRST	RxEN
0		0	0	1	0
r		rw	rw	rw	rw

31: 4 RESERVED

3: Sub Carrier Reset (ScRST) - resets sub carrier receiver

2: Reset (RST) - resets complete core

1: Receiver Reset (RxRST) - resets telemetry receiver

0: Receiver Enable (RxEN) - enables telemetry receiver (should be done after the complete configuration of the telemetry receiver)

121.5.5 GRTMRX Status Register (read-only)

Table 1800. 0x84 - STAT - status register (read-only)

31 15	14	13 12	11	10	9	8	7	6	5	4	3	2	1 0
RESERVED	DEBUG	ASM Cntr	R	CRC Error	Invert	DLock	Sync Mark	Frame Mark	Frame Ready	ASM Free	ASM Lock	ASM Sync	State
0	*	0	0	0	0	1	*	*	0	0	0	0	0
r	r	r	r	r	r	r	r	r	r	r	r	r	r

31: 15 RESERVED

14: (DEBUG) - Indicates when set that additional debug information is available in bit 31:15.

13: 12 (ASMCTNR) - ASM counter (diagnostics)

11: RESERVED

10: (CRCERR) - CRC error (speculative, only useful if FECF present in frame) [1]

9: (INVERT) - Inverted bit stream (diagnostics)

8: (DLOCK) - Convolutional decoder in lock (diagnostics)

7: (SYNCMARK) - Sync Marker (external signal status, if available)

6: (FRAMEMARK) - Frame Marker (external signal status, if available)

5: (FRAMEREADY) - Frame ready (diagnostics)

4: (ASMFREE) - ASM free running (diagnostics) [1]

3: (ASMLOCK) - ASM in lock (diagnostics) [1]

2: (ASMSYNC) - ASM synchronized (diagnostics)[1]

1: 0 Receiver state (STATE) - 00=Idle, 01=Search, 10=Filter, 11=Receive (diagnostics)

121.5.6 GRTMRX Configuration Register

Table 1801. 0x88 - CONF - configuration register

31 24	23 8	7 3	2	1	0
REVISION	FIFOSIZE	RESERVED	Free Wheel	Raw	Endian
1	25b	0	0	0	0
r	r	r	rw	rw	rw

31: 24 (REVISION) - Revision number

23: 8 (FIFOSIZE) - FIFO size bytes

7: 3 RESERVED

2: (FREEWHEEL) - Free wheeling enabled when set (i.e. accepts missing ASM) (not to be used with RAW set or MATCH and IGNORE usage)

1: (RAW) - Raw data capture when set (no ASM search)

0: (ENDIAN) - Little Endian when set, Big Endian when cleared

121.5.7 GRTMRX Size Register

Table 1802. 0x8C - SIZE - size register

31 29	28 16	15 0
RESERVED	OCFINDEX	NOOFBITS
0	0xE3	0x718
r	rw	rw

31: 29 RESERVED

28: 16 (OCFINDEX) Defines the byte number of the last octet of OCF, counting from the ASM start [1]

Defines the byte number of the octet preceding FECF, counting from the ASM start [1]

15: 0 (NOOFBITS) - Number of bits for block to receive (e.g. including ASM, Reed-Solomon code, etc.)

121.5.8 GRTMRX Physical Layer Register

Table 1803. 0x90 - PLR - physical layer register

31	30 16	15	14 0
SF	SYMBOLRATE	SCF	SUBRATE
0	0	0	0
rw	r	rw	r

31 Symbol Fall (SF) - symbol clock has a falling edge at start of symbol bit

30: 16 Symbol Rate (SYMBOLRATE) - symbol rate division factor -1 (read-only) (diagnostics)

When Sub Carrier (SC) is disabled, this field corresponds to the lower 15 bits of the number of system clock periods -1 counted per incoming symbol clock period duration.

When Sub Carrier (SC) is enabled, this field corresponds to the number of system clock periods -1 counted per incoming symbol clock period duration.

15 Sub Carrier Fall (SCF) -sub carrier output start with a falling edge for logical 1

14: 0 Sub Carrier Rate (SUBRATE) - sub carrier division factor - 1 (read only) (diagnostics)

When Sub Carrier (SC) is disabled, this field corresponds to the upper 15 bits of the number of system clock periods -1 counted per incoming symbol clock period duration.

When Sub Carrier (SC) is enabled, this field corresponds to the number of sub-carrier clock phases - 1 counted per incoming symbol bit duration.

Telemetry Rate (TELEMTRY RATE) - is the bit rate after potential Sub Carrier (SC) demodulation, Split-Phase Level (S) demodulation and Convolutional Encoding (CE) decoding, and corresponds to the telemetry bit rate.

The following variables are used in the tables hereafter: f = system clock frequency, n = SYMBOLRATE+1 (GRTMRX physical layer register field +1), and m = SUBRATE+1 (GRTMRX physical layer register field +1).

When Sub Carrier (SC) is disabled, the telemetry rate equals

TELMETRY RATE = (SUBRATE * 2**15 + SYMBOLRATE+1) / (1+CE) / (1+SP) = m * n / (1+CE) / (1+SP)

When Sub Carrier (SC) is enabled, the telemetry rate equals

TELEMETRY RATE = (SUBRATE +1)* (SYMBOLRATE+1) / (1+CE) / (1+SP) = m * n / (1+CE) / (1+SP)

121.5.9 GRTMRX Coding Sub-Layer Register

Table 1804. 0x94 - CSL - coding sub-layer register

31 19	18 17	16 8	7	6	5	4 2	1	0
RESERVED	SEL	RESERVED	PSR	NRZ	CE	RESERVED	SP	SC
0	0	0	0	0	0	0	0	0
r	rw	r	rw	rw	rw	r	rw	rw

31: 19 RESERVED

18: 17 Selection (SEL) - selection of external telemetry clock and data source (application specific)

16: 8 RESERVED

7: Pseudo-Randomiser (PSR) - pseudo-de-randomiser enable [1]

6: Non-Return-to-Zero (NRZ) - non-return-to-zero - mark decoding enable

5: Convolutional Encoding (CE) - convolutional decoding enable

4: 2 RESERVED

1: Split-Phase Level (SP) - split-phase level de-modulation enable

0: Sub Carrier (SC) - sub carrier de-modulation enable

121.5.10GRTMRX Attached Synchronization Marker Register

Table 1805. 0x98 - ASM - attached synchronization marker register

31	0
ASM	
0xIACFFCID	
rw	

31: 0 Attached Synchronization Marker (ASM) - pattern for ASM, (bit 31 MSB sent first, bit 0 LSB sent last), reset values 0x1ACFFC1D [1]

121.5.11GRTMRX Attached Synchronization Mask Register

Table 1806. 0x9C - AMM - attached synchronization mask register

31	0
ASMMASK	
0xFFFFFFFF	
r	

31: 0 Attached Synchronization Marker Mask (ASMMASK) - mask for ASM pattern, bit used when set [1]

121.5.12GRTMRX Data Rate Register (read-only)

Table 1807. 0xAC - DRR - data rate register (read-only)

31	30	29	0
R		DATARATE	
0		0	
r		r	

31: 30 RESERVED

29: 0 (DATARATE) - data rate division factor -1 (read-only) (diagnostics)

This field corresponds to the number of system clock periods -1 counted per incoming telemetry bit period duration.

121.5.13GRTMRX Filter Register

Table 1808. 0xB0 - FLT - Filter register

31	16	15	0
MATCH		IGNORE	
0		0	
rw		rw	

31: 16 (MATCH) - Matching pattern for the first two received octets after ASM (bit 31 MSB, bit 16 LSB) [1]

15: 0 (IGNORE) - Non-matching pattern for the first two received octets after ASM (bit 15 MSB, bit 0 LSB) [1]

121.5.14GRTMRX Filter Mask Register

Table 1809. 0B4 - FLTM - Filter Mask register

31 16	15 0
MATCHMASK	IGNOREMASK
0	0
rw	rw

31: 16 (MATCHMASK) - Mask for matching pattern (bit 31 MSB, bit 16 LSB), bit used when set [1]

15: 0 (IGNOREMASK) - Mask for non-matching pattern (bit 15 MSB, bit 0 LSB), bit used when set [1]

121.5.15GRTMRX OCF Register (read-only)

*Table 1810.*0x00 - OCF - OCF register (read-only)

31 0
OCF
0xFFFFFFFF
r

31: 0 Operational Control Field (OCF) - OCF/CLCW data (bit 31 MSB, bit 0 LSB) [1]

121.5.16GRTMRX FECF Register (read-only)

Table 1811. 0x04 - FECF - FECF register (read-only)

31 16	15 0
RESERVED	FECF
0	0xFFFF
r	r

31: 16 RESERVED

15: 0 Frame Error Control Field (FECF) - FECF/CRC data (bit 15 MSB, bit 0 LSB) [1]

Note 1: This function does is not supported in raw capture mode, when the RAW register bit is set.

121.5.17GRTMRX Demodulator Register

*Table 1812.*0x08 - DEM - Demodulator register

31	30	29 0
EN	DM	SYMBOLRATE
0	1	*
rw	r	r

31: Enable (EN) - Enable clock recovery demodulator when logical 1

30: Demodulator (DM) - Clock recovery demodulator implemented if logical 1(read-only)

29: 0 Symbol Rate (SYMBOLRATE) - Symbol rate division factor -1 (read-only) (diagnostics)

This field corresponds to the number of system clock periods -1 counted per incoming symbol duration (i.e. locally generated symbol clock period). Note that when Sub Carrier (SC) modulation is used, a symbol corresponds to one phase of the sub-carrier clock.

121.6 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x082. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

121.7 Configuration options

Table 1813 shows the configuration options of the core (VHDL generics).

*Table 1813.*Configuration options

Generic name	Function	Allowed range	Default
hindex	AHB master index	0 - NAHBMST-1	0
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	ADDR field of the APB BAR	0 - 16#FFF#	0
pmask	MASK field of the APB BAR	0 - 16#FFF#	16#FFF#
pirq	Interrupt line used by core	0 - NAHBIRQ-1	0
memtech	Memory technology	0 to NTECH	0
clktech	Clock buffer technology	0 to NTECH	0
buftype	Clock buffer type	TBD	0
demod	Demodulator for local clock recovery	0 - 1	0

121.8 Signal descriptions

Table 1814 shows the interface signals of the core (VHDL ports).

*Table 1814.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
TMI	BITLOCK	Output	Bit Lock	High
	RFAVAIL		RF Available	High
	OCF_SDU[0:31]		OCF_SDU Bypass	-
	CIPHER		Encryption/ Cipher Interface	-
	EXREQUEST		External VC Request	High
	CONF		External configuration	-

*Table 1814.*Signal descriptions

Signal name	Field	Type	Function	Active
TMO	TIME	Input	Time strobe	High
	SYNC		ASM indicator	High
	FRAME		Frame indicator	High
	SERIAL		Serial bit data	High
	CLOCK		Serial bit data clock	High
	DATA [0:7]		Parallel data, octet	High
	STROBE		Parallel data strobe	High
	C1		C1 bit from convolutional encoder	-
	C2		C2 bit from convolutional encoder	-
	CLKSEL[0:1]		External clock selection	-
	FRAMELSB[0:1]		MC Counter least significant bits	-
	CIPHER		Encryption/ Cipher Interface	-
	SCID[0:9]		SCID setting	-
	OCF		OCF setting	High
	FECF		FECF setting	High
	EXENABLE		External VC enable	High
	EXGRANT		External VC grant	High
	EXREADY		External VC ready	High
	TIMESTAMP		Time Stamp	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
AHBMI	*	Input	AMB master input signals	-
AHBMO	*	Output	AHB master output signals	-

* see GRLIB IP Library User's Manual

121.9 Signal definitions and reset values

The signals and their reset values are described in table 1815.

*Table 1815.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
sync	Input	ASM indicator	High	-
frame	Input	Frame indicator	High	-
serial	Input	Serial bit data	-	-
clock	Input	Serial bit data clock	High	-

121.10 Timing

The timing waveforms and timing parameters are shown in figure 302 and are defined in table 1816.

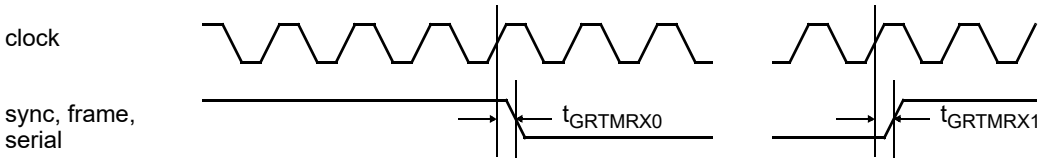


Figure 302. Timing waveforms

*Table 1816.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{GRTMRX0}$	input to clock hold	rising *clock* edge	TBD	TBD	ns
$t_{GRTMRX1}$	input to clock setup	rising *clock* edge	TBD	TBD	ns

121.11 Library dependencies

Table 1817 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1817.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
TMTC	TMTC_TYPES	Signals, component	Component declaration

122 GRCE/GRCD - CCSDS/ECSS Convolutional Encoder and Quicklook Decoder

The *Basic Convolutional Encoder* (GRCE) comprises a synchronous bit serial input and a synchronous bit serial output. The output frequency is twice the input frequency.

The *Basic Convolutional Quicklook Decoder* (GRCD) comprises a synchronous bit serial input and a synchronous bit serial output. The input frequency is twice the output frequency. The quicklook decoder decodes the incoming bit stream without correcting for bit errors.

The GRCE / GRCD models are based on the Basic Convolutional Code specified by *Consultative Committee for Space Data Systems* (CCSDS) and *European Cooperation for Space Standardization* (ECSS).

[CCSDS] TM Synchronization and Channel Coding, CCSDS 131.0-B-2

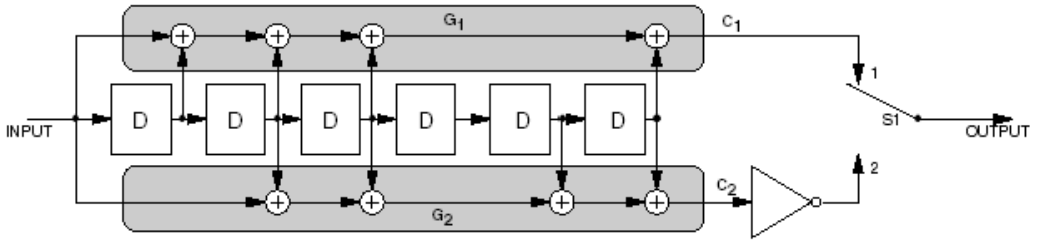
[PSS] Telemetry Channel Coding Standard, ESA PSS-04-103, Issue 1, September 1989

[ECSS] Telemetry synchronization and channel coding, ECSS-E-ST-50-01C

122.1 Protocol

The basic convolutional code is a rate 1/2, constraint-length 7 transparent code which is well suited for channels with predominantly Gaussian noise:

Nomenclature:	Convolutional code
Code rate:	1/2 bit per symbol.
Constraint length:	7 bits.
Connection vectors:	G1 = 1111001 (171 octal); G2 = 1011011 (133 octal).
Symbol inversion:	On output path of G2.



NOTES:

1. → D → = SINGLE BIT DELAY.
2. FOR EVERY INPUT BIT, TWO SYMBOLS ARE GENERATED BY COMPLETION OF A CYCLE FOR S1: POSITION 1, POSITION 2.
3. S1 IS IN THE POSITION SHOWN (1) FOR THE FIRST SYMBOL ASSOCIATED WITH AN INCOMING BIT.
4. ⊕ = MODULO-2 ADDER.
5. → ▷○ = INVERTER.

122.2 Configuration options

Table 1818 shows the configuration options of the cores (VHDL generics).

*Table 1818.*Configuration options

Generic name	Function	Allowed range	Default
syncreset	Synchronous reset when set, else asynchronous	0 - 1	0

122.3 Signal descriptions

Table 1820 shows the interface signals of the Basic Convolutional Encoder (GRCE) core (VHDL ports).

*Table 1819.*Signal descriptions - GRCE

Signal name	Field	Type	Function	Active
Rst_N	N/A	Input	This active low input port synchronously resets the model. The port is assumed to be deasserted synchronously with the ***Cout*** system clock.	Low
Cin	N/A	Input	This input port is the bit clock for the data input ***Din***. The port is sampled on the rising ***Cout*** edge. When *Cin* is sampled as asserted, a new bit is present on the ***Din*** port. ***Cin*** is assumed to have been generated from the rising ***Cout*** edge, normally with a delay, and ***Din*** is assumed to be stable after the falling ***Cin*** edge.	High
Din	N/A	Input	This input port is the serial data input for the interface. Data are sampled on the rising ***Cout*** edge when the ***Cin*** input is asserted. Input data ***Din*** is thus qualified by the input bit clock ***Cin***. For each input data bit on ***Din***, two bits are output on ***Dout***.	-
Cout	N/A	Output	This input port is the system clock for the model. All registers are clocked on the rising ***Cout*** edge. The port also acts as the bit clock for the data output ***Dout***.	Rising
Dout	N/A	Output	This output port is the serial data output for the interface. The output is clocked out on the rising ***Cout*** edge.	-

Table 1820 shows the interface signals of the GRCD core (VHDL ports).

*Table 1820.*Signal descriptions - GRCD

Signal name	Field	Type	Function	Active
Rst_N	N/A	Input	This active low input port synchronously resets the model. The port is assumed to be deasserted synchronously with the ***Cin*** system clock.	Low
Cin	N/A	Input	This input port is the system clock for the model. All registers are clocked on the falling ***Cin*** edge. The port also acts as the bit clock for the data input ***Din***.	Falling
Din	N/A	Input	This input port is the serial data input for the interface. Data are sampled on the falling ***Cin*** edge. For two input data bits on ***Din***, one bit is output on ***Dout***.	-
Cout	N/A	Output	This output port is the output bit clock. The output is clocked out on the falling ***Cin*** edge.	-
Dout	N/A	Output	This output port is the serial data output for the interface. The output is clocked out on the falling ***Cin*** edge. ***Dout*** is assumed to be sampled externally on the falling ***Cout*** edge.	-
Dlock	N/A	Output	This output port is asserted when the quick look decoder is in lock and producing decoded data. The output is clocked out on the falling ***Cin*** edge.	High

122.4 Signal definitions and reset values

The signals and their reset values for the Basic Convolutional Encoder (GRCE) are described in table 1821.

*Table 1821.*Signal definitions and reset values - GRCE

Signal name	Type	Function	Active	Reset value
cin	Input	Input data qualifier	High	-
din	Input	Input data	-	-
cout	Input	Bit clock	Rising	-
dout	Output	Output data	-	Logical 0

The signals and their reset values for the Basic Convolutional Quicklook Decoder (GRCD) are described in table 1821.

*Table 1822.*Signal definitions and reset values - GRCD

Signal name	Type	Function	Active	Reset value
cin	Input	Bit clock	Falling	-
din	Input	Input data	-	-
cout	Output	Output bit clock	High	Logical 0
dout	Output	Output data	-	Logical 0
dlock	Output	Decoder in lock	High	Logical 0

122.5 Timing

The timing waveforms and timing parameters for the Basic Convolutional Encoder (GRCE) are shown in figure 303 and are defined in table 1823.

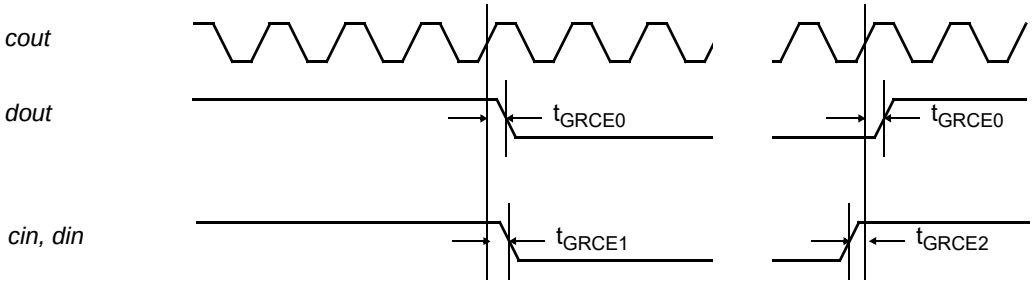


Figure 303. Timing waveforms - GRCE

*Table 1823.*Timing parameters - GRCE

Name	Parameter	Reference edge	Min	Max	Unit
t_{GRCE0}	clock to output delay	rising *cout* edge	TBD	TBD	ns
t_{GRCE1}	input to clock hold	rising *cout* edge	-	-	ns
t_{GRCE2}	input to clock setup	rising *cout* edge	-	-	ns

The timing waveforms and timing parameters for the Basic Convolutional Quicklook Decoder (GRCD) are shown in figure 303 and are defined in table 1823.

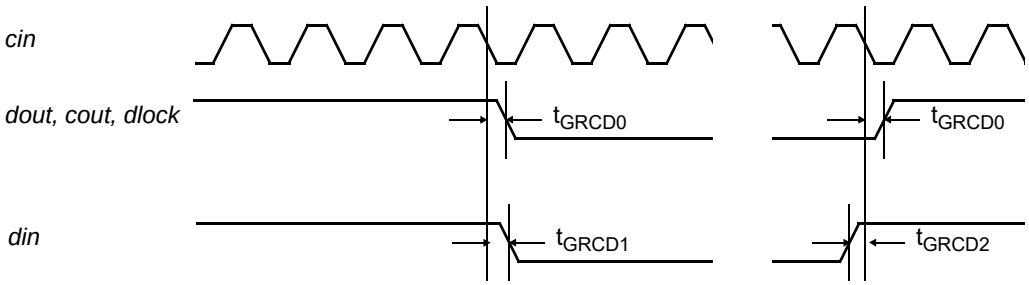


Figure 304. Timing waveforms - GRCD

*Table 1824.*Timing parameters - GRCD

Name	Parameter	Reference edge	Min	Max	Unit
t_{GRCD0}	clock to output delay	rising *cin* edge	TBD	TBD	ns
t_{GRCD1}	input to clock hold	rising *cin* edge	-	-	ns
t_{GRCd2}	input to clock setup	rising *cin* edge	-	-	ns

122.6 Library dependencies

Table 1825 shows the libraries used when instantiating the cores (VHDL libraries).

*Table 1825.*Library dependencies

Library	Package	Imported unit(s)	Description
TMTC	TMTC_Types	Component	Component declaration

122.7 Instantiation

The GRCE/ GRCD cores are fully synchronous designs based on a single clock strategy. All registers in the cores are reset synchronously or asynchronously, controlled by the syncrst VHDL generic. The reset input requires external synchronisation to avoid any setup and hold time violations.

This example shows how the cores can be instantiated.

```
   library  IEEE;
   use      IEEE.Std_Logic_1164.all;
   library  TMTC;

...

   component GRCE
   port(
      Rst_n:      in    Std_ULogic; -- Synchronous reset
      Cin:        in    Std_ULogic; -- Input  data clock
      Din:        in    Std_ULogic; -- Input  data
      Cout:       in    Std_ULogic; -- Output data clock
      Dout:       out   Std_ULogic);-- Output data
   end component GRCE;

   component GRCD
   port(
      Rst_N:      in    Std_ULogic; -- Synchronous reset
      Cin:        in    Std_ULogic; -- Input  data clock
      Din:        in    Std_ULogic; -- Input  data
      Cout:       out   Std_ULogic; -- Output data clock
      Dout:       out   Std_ULogic; -- Output data
      Dlock:      out   Std_ULogic);-- Output locked
   end component GRCD;
```

123 GRTC - CCSDS/ECSS Telecommand Decoder

123.1 Overview

The Telecommand Decoder (GRTC) is compliant with the Packet Telecommand protocol and specification defined by [ECSS-E-ST-50-04C]. The decoder is compatible with the [PSS-04-107] and [PSS-04-151] standards. The decoder is compatible with the CCSDS recommendations [CCSDS-231.0-B-2], [CCSDS-232.0-B-2] and [CCSDS-232.1-B-2]. The Telecommand Decoder (GRTC) only implements the Coding Layer (CL).

In the Coding Layer (CL), the telecommand decoder receives bit streams on multiple channel inputs. The streams are assumed to have been generated in accordance with the Physical Layer specifications. In the Coding Layer, the decoder searches all input streams simultaneously until a start sequence is detected. Only one of the channel inputs is selected for further reception. The selected stream is bit-error corrected and the resulting corrected information is passed to the user. The corrected information received in the CL is transfer by means of Direct Memory Access (DMA) to the on-board processor.

The Command Link Control Word (CLCW) and the Frame Analysis Report (FAR) can be read and written as registers via the AMBA AHB bus. Parts of the two registers are generated by the Coding Layer (CL). The CLCW can be automatically transmitted to the Telemetry Encoder (TM) for transmission to the ground. Note that most parts of the CLCW and FAR are not produced by the Telecommand Decoder (GRTC) hardware portion. This is instead done by the software portion of the decoder.

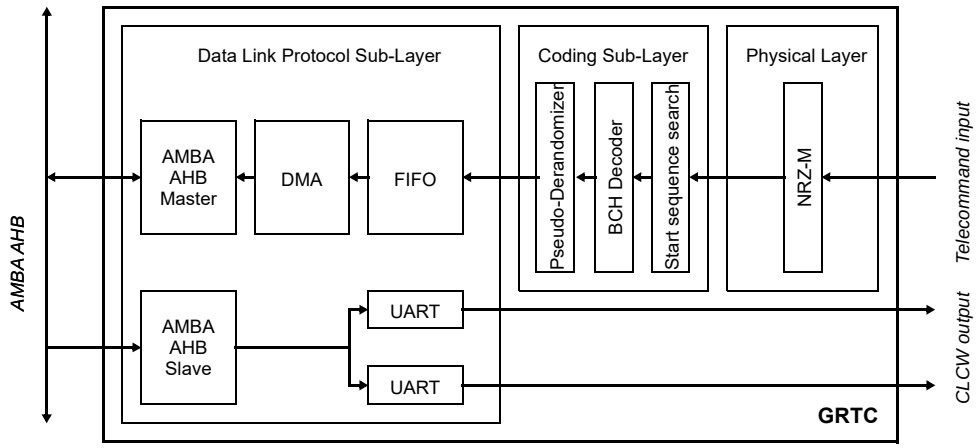


Figure 305. Block diagram

123.1.1 Concept

A telecommand decoder in this concept is mainly implemented by software in the on-board processor. The supporting hardware in the GRTC core implements the Coding Layer, which includes synchronisation pattern detection, channel selection, codeblock decoding, Direct Memory Access (DMA) capability and buffering of corrected codeblocks. The hardware also provides a register via which the Command Link Control Word (CLCW) is made available to a Telemetry Encoder. The CLCW is to be generated by the software.

The GRTC has been split into several clock domains to facilitate higher bit rates and partitioning. The two resulting sub-cores have been named Telecommand Channel Layer (TCC) and the Telecommand Interface (TCI). Note that TCI is called AHB2TCI. A complete CCSDS packet telecommand decoder can be realized at software level according to the latest available standards, staring from the Transfer Layer.

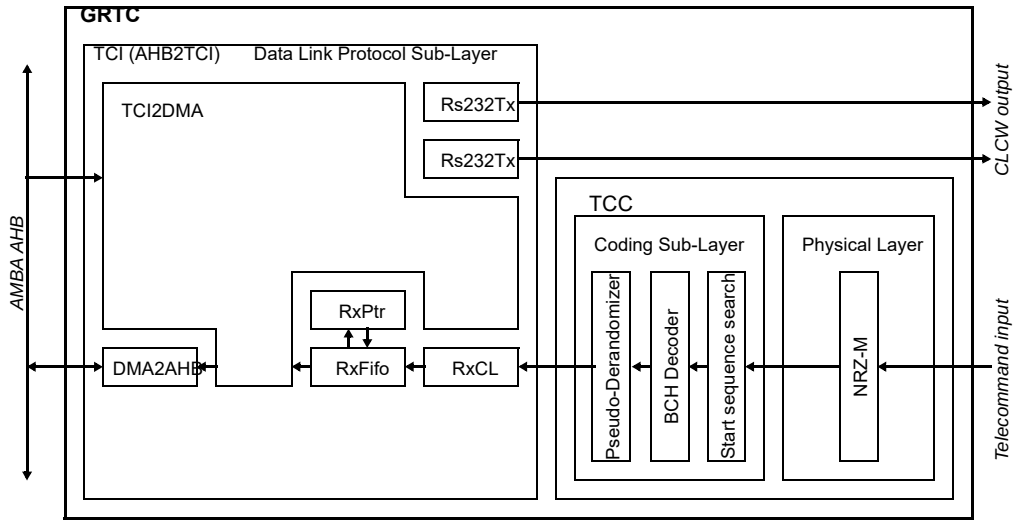


Figure 306. Detailed block diagram showing the internal structure

123.1.2 Functions and options

The Telecommand Decoder (GRTC) only implements the Coding Layer of the telecommand protocol standard [ECSS-E-ST-50-04C]. All other layers are to be implemented in software, e.g. Authentication Unit (AU). The Command Pulse Distribution Unit (CPDU) is not implemented.

The following functions of the GRTC are programmable by means of registers:

- Pseudo-De-Randomisation
- Non-Return-to-Zero – Mark decoding

The following functions of the GRTC are pin configurable:

- Polarity of RF Available and Bit Lock inputs
- Edge selection for input channel clock

123.2 Data formats

123.2.1 Reference documents

[PSS-04-107]	Packet Telecommand Standard, Issue 2
[PSS-04-151]	Telecommand Decoder Standard, Issue 1
[CCSDS 231.0-B-2]	TC Synchronization and Channel Coding
[CCSDS 232.0-B-2]	TC Space Data Link Protocol
[CCSDS 232.1-B-2]	Communications Operation Procedure-1
[ECSS-E-ST-50-04C]	Space engineering - Space data links - Telecommand protocols, synchronization and channel coding

123.2.2 Waveforms

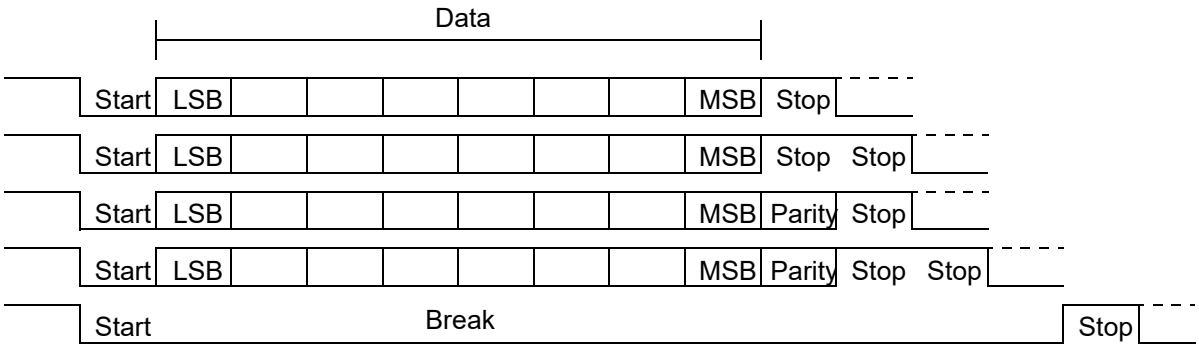


Figure 307. Bit asynchronous protocol versions

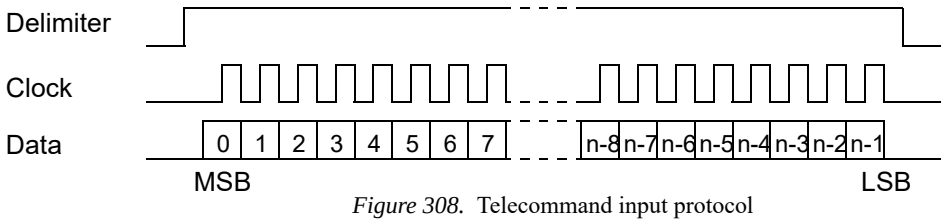


Figure 308. Telecommand input protocol

123.3 Coding Layer (CL)

The Coding Layer synchronises the incoming bit stream and provides an error correction capability for the Command Link Transmission Unit (CLTU). The Coding Layer receives a dirty bit stream together with control information on whether the physical channel is active or inactive for the multiple input channels.

The bit stream is assumed to be NRZ-L encoded, as the standards specify for the Physical Layer. As an option, it can also be NRZ-M encoded. There are no assumptions made regarding the periodicity or continuity of the input clock signal while an input channel is inactive. The most significant bit (Bit 0 according to [ECSS-E-ST-50-04C]) is received first.

Searching for the Start Sequence, the Coding Layer finds the beginning of a CLTU and decodes the subsequent codeblocks. As long as no errors are detected, or errors are detected and corrected, the Coding Layer passes clean blocks of data to the Transfer Layer which is implemented in software. When a codeblock with an uncorrectable error is encountered, it is considered as the Tail Sequence, its contents are discarded and the Coding Layer returns to the Start Sequence search mode.

The Coding Layer also provides status information for the FAR, and it is possible to enable an optional de-randomiser according to [ECSS-E-ST-50-04C].

123.3.1 Synchronisation and selection of input channel

Synchronisation is performed by means of bit-by-bit search for a Start Sequence on the channel inputs. The detection of the Start Sequence is tolerant to a single bit error anywhere in the Start Sequence pattern. The Coding Layer searches both for the specified pattern as well as the inverted pattern. When an inverted Start Sequence pattern is detected, the subsequent bit-stream is inverted till the detection of the Tail Sequence.

The detection is accomplished by a simultaneous search on all active channels. The first input channel where the Start Sequence is found is selected for the CLTU decoding. The selection mechanism is restarted on any of the following events:

- The input channel active signal is de-asserted, or
- a Tail Sequence is detected, or

- a Codeblock rejection is detected, or
- an abandoned CLTU is detected, or the clock time-out expires.

As a protection mechanism in case of input failure, a clock time-out is provided for all selection modes. The clock time-out expires when no edge on the bit clock input of the selected input channel in decode mode has been detected for a specified period. When the clock time-out has expired, the input channel in question is ignored (i.e. considered inactive) until its active signal is de-asserted (configurable with gTimeoutMask=1).

123.3.2 Codeblock decoding

The received Codeblocks are decoded using the standard (63,56) modified BCH code. Any single bit error in a received Codeblock is corrected. A Codeblock is rejected as a Tail Sequence if more than one bit error is detected. Information regarding Count of Single Error Corrections and Count of Accept Codeblocks is provided to the FAR. Information regarding Selected Channel Input is provided via a register.

123.3.3 De-Randomiser

In order to maintain bit synchronisation with the received telecommand signal, the incoming signal must have a minimum bit transition density. If a sufficient bit transition density is not ensured for the channel by other methods, the randomiser is required. Its use is optional otherwise. The presence or absence of randomisation is fixed for a physical channel and is managed (i.e., its presence or absence is not signalled but must be known a priori by the spacecraft and ground system). A random sequence is exclusively OR-ed with the input data to increase the frequency of bit transitions. On the receiving end, the same random sequence is exclusively OR-ed with the decoded data, restoring the original data form. At the receiving end, the de-randomisation is applied to the successfully decoded data. The de-randomiser remains in the “all-ones” state until the Start Sequence has been detected. The pattern is exclusively OR-ed, bit by bit, to the successfully decoded data (after the Error Control Bits have been removed). The de-randomiser is reset to the “all-ones” state following a failure of the decoder to successfully decode a codeblock or other loss of input channel.

123.3.4 Non-Return-to-Zero – Mark

An optional Non-Return-to-Zero – Mark decoder can be enabled by means of a register.

123.3.5 Design specifics

The coding layer is supporting 1 to 8 channel inputs ([PSS-04-151] requires at least 4).

A codeblock is fixed to 56 information bits (as per CCSDS/ECSS).

The CCSDS/ECSS (1024 octets) or [PSS-04-151] (256 octets) standard maximum frame lengths are supported, being programmable via bit PSS in the GCR register. The former allows more than 37 codeblocks to be received.

The Frame Analysis Report (FAR) interface supports 8 bit CAC field, as well as the 6 bit CAC field specified in [PSS-04-151]- When the PSS bit is cleared to '0', the two most significant bits of the CAC will spill over into the "LEGAL/ILLEGAL" FRAME QUALIFIER field in the FAR. These bits will however be all-zero when [PSS-04-151] compatible frame lengths are received or the PSS bit is set to '1'. The saturation is done at 6 bits when PSS bit is set to '1' and at 8 bits when PSS bit is cleared to '0'.

The Pseudo-Randomiser decoder is included (as per CCSDS/ECSS), its usage being input signal programmable.

The Physical Layer input can be NRZ-L or NRZ-M modulated, allowing for polarity ambiguity. NRZ-L/M selection is programmable. This is an extension to ECSS: Non-Return to Zero - Mark decoder added, with its internal state reset to zero when channel is deactivated.

Note: If input clock disappears, it will also affect the codeblock acquired immediately before the codeblock just being decoded (accepted by [PSS-04-151]).

In state S1, all active inputs are searched for start sequence, there is no priority search, only round robin search. The search for the start sequence is sequential over all inputs: maximum input frequency = system frequency /(gIn+2)

The [PSS-04-151] specified CASE-1 and CASE-2 actions are implemented according to aforementioned specification, not leading to aborted frames.

Extended E2 handling is implemented:

- E2b Channel Deactivation - selected input becomes inactive in S3
- E2c Channel Deactivation - too many codeblocks received in S3
- E2d Channel Deactivation - selected input is timed-out in S3
  (design choice being: S3 => S1, abandoned frame)

123.3.6 Direct Memory Access (DMA)

This interface provides Direct Memory Access (DMA) capability between the AMBA bus and the Coding Layer. The DMA operation is programmed via an AHB slave interface.

The DMA interface is an element in a communication concept that contains several levels of buffering. The first level is performed in the Coding Layer where a complete codeblock is received and kept until it can be corrected and sent to the next level of the decoding chain. This is done by inserting each correct information octet of the codeblock in an on-chip local First-In-First-Out (FIFO) memory which is used for providing improved burst capabilities. The data is then transferred from the FIFO to a system level ring buffer in the user memory (e.g. SRAM located in on-board processor board) which is accessed by means of DMA.

The following storage elements can thus be found in this design:

The shift and hold registers in the Coding Layer

The local FIFO (parallel; 32-bit; 4 words deep)

The system ring buffer (for example external SRAM; 32-bit; 1 to 256 kByte deep).

123.4 Transmission

The transmission of data from the Coding Layer to the system buffer is described hereafter.

The serial data is received and shifted in a shift register in the Coding Layer when the reception is enabled. After correction, the information content of the shift register is put into a hold register.

When space is available in the peripheral FIFO, the content of the hold register is transferred to the FIFO. The FIFO is of 32-bit width and the byte must thus be placed on the next free byte location in the word.

When the FIFO is filled for 50%, a request is done to transfer the available data towards the system level buffer.

If the system level ring buffer isn’t full, the data is transported from the FIFO, via the AHB master interface towards the main processor and stored in e.g. external SRAM. If no place is available in the system level ring buffer, the data is held in the FIFO.

When the GRTC keeps receiving data, the FIFO will fill up and when it reaches 100% of data, and the hold and shift registers are full, a receiver overrun interrupt will be generated (IRQ_RX_OVERRUN). All new incoming data is rejected until space is available in the peripheral FIFO.

When the receiving data stream is stopped (e.g. when a complete data block is received), and some bytes are still in the peripheral FIFO, then these bytes will be transmitted to the system level ring buf-

fer automatically. Received bytes in the shift and hold register are always directly transferred to the peripheral FIFO.

The FIFO is automatically emptied when a CLTU is either ready or has been abandoned. The reason for the latter can be codeblock error, time out etc. as described in CLTU decoding state diagram.

The operational state machine is shown in figure 309.

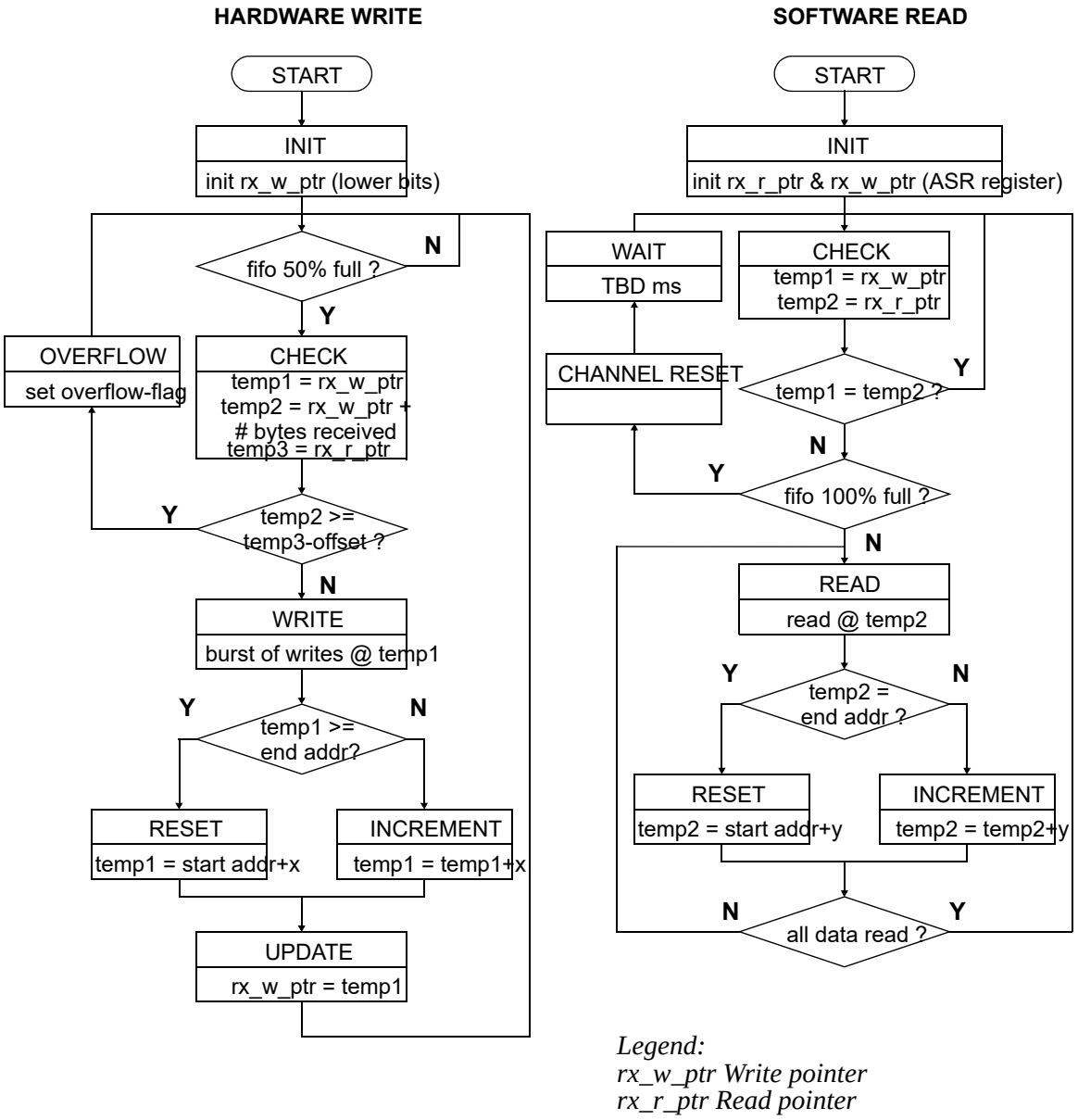


Figure 309. Direct Memory Access

123.4.1 Data formatting

When in the decode state, each candidate codeblock is decoded in single error correction mode as described hereafter.

123.4.2 CLTU Decoder State Diagram

Note that the diagram has been improved with explicit handling of different E2 events listed below.

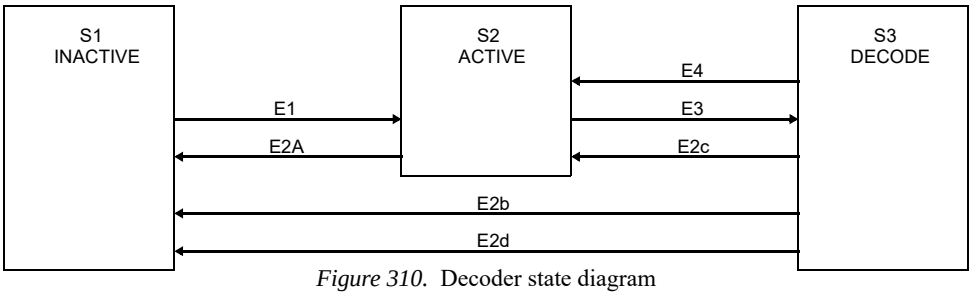


Figure 310. Decoder state diagram

State Definition:

- S1 Inactive
- S2 Search
- S3 Decode

Event Definition:

- E1 Channel Activation
- E2a Channel Deactivation - all inputs are inactive
- E2b Channel Deactivation - selected becomes inactive (CB=0 -> frame abandoned)
- E2c Channel Deactivation - too many codeblocks received (all -> frame abandoned)
- E2d Channel Deactivation - selected is timed-out (all -> frame abandoned)
- E3 Start Sequence Found
- E4 Codeblock Rejection (CB=0 -> frame abandoned)

123.4.3 Nominal

A: When the first “Candidate Codeblock” (i.e. “Candidate Codeblock” 0, which follows Event 3 (E3):START SEQUENCE FOUND) is found to be error free, or if it contained an error which has been corrected, its information octets are transferred to the remote ring buffer as shown in table 1826. At the same time, a “Start of Candidate Frame” flag is written to bit 0 or 16, indicating the beginning of a transfer of a block of octets that make up a “Candidate Frame”. There are two cases that are handled differently as described in the next sections.

*Table 1826.*Data format

	Bit[31……24]	**Bit[23……16]**	**Bit[15……8]**	**Bit[7……..……0]**
0x40000000	information octet0	0x01	information octet1	0x00
0x40000004	information octet2	0x00	information octet3	0x00
0x40000008	information octet4	0x00	end of frame	0x02
…	…		…	
0x400000xx	information octet6	0x01	information octet7	0x00
0x400000xx	information octet8	0x00	abandoned frame	0x03

Legend: Bit [17:16] or [1:0]:

“00” = continuing octet

“01” = Start of Candidate Frame

“10” = End of Candidate Frame

“11” = Candidate Frame Abandoned

123.4.4 CASE 1

When an Event 4 – (E4): CODEBLOCK REJECTION – occurs for any of the 37 possible “Candidate Codeblocks” that can follow Codeblock 0 (possibly the tail sequence), the decoder returns to the SEARCH state (S2), with the following actions:

- The codeblock is abandoned (erased)
- No information octets are transferred to the remote ring buffer
- An “End of Candidate Frame” flag is written, indicating the end of the transfer of a block of octets that make up a “Candidate Frame”.

123.4.5 CASE 2

When an Event 2 – (E2): CHANNEL DEACTIVATION – occurs which affects any of the 37 possible “Candidate Codeblocks” that can follow Codeblock 0, the decoder returns to the INACTIVE state (S1), with the following actions:

- The codeblock is abandoned (erased)
- No information octets are transferred to the remote ring buffer
- An “End of Candidate Frame” flag is written, indicating the end of the transfer of a block of octets that make up a “Candidate Frame”

123.4.6 Abandoned

- B: When an Event 4 (E4), or an Event 2 (E2), occurs which affects the first candidate codeblock 0, the CLTU shall be abandoned. No candidate frame octets have been transferred.
- C: If and when more than 37 Codeblocks have been accepted in one CLTU, the decoder returns to the SEARCH state (S2). The CLTU is effectively aborted and this is will be reported to the software by writing the “Candidate Frame Abandoned flag” to bit 1 or 17, indicating to the software to erase the “Candidate frame”.

123.5 Relationship between buffers and FIFOs

The conversion from the peripheral data width (8 bit for the coding layer receiver), to 32 bit system word width, is done in the peripheral FIFO.

All access towards the system ring buffer are 32-bit aligned. When the amount of received bytes is odd or not 32-bit aligned, the FIFO will keep track of this and automatically solve this problem. For the reception data path, the 32 bit aligned accesses could result in incomplete words being written to the ring buffer. This means that some bytes aren’t correct (because not yet received), but this is no problem due to the fact that the hardware write pointer (rx_w_ptr) always points to the last, correct, data byte.

The local FIFO ensures that DMA transfer on the AMBA AHB bus can be made by means of 2-word bursts. If the FIFO is not yet filled and no new data is being received this shall generate a combination of single accesses to the AMBA AHB bus if the last access was indicating an end of frame or an abandoned frame.

If the last single access is not 32-bit aligned, this shall generate a 32-bit access anyhow, but the receive-write-pointer shall only be incremented with the correct number of bytes. Also in case the previous access was not 32-bit aligned, then the start address to write to will also not be 32-bit aligned. Here the previous 32-bit access will be repeated including the bytes that were previously missing, in order to fill-up the 32-bit remote memory-controller without gaps between the bytes.

The receive-write-pointer shall be incremented according to the number of bytes being written to the remote memory controller.

123.5.1 Buffer full

The receiving buffer is full when the hardware has filled the complete buffer space while the software didn't read it out. Due to hardware implementation and safety, the buffer can't be filled completely without interaction of the software side. A space (offset) between the software read pointer (rx_r_ptr) and the hardware write pointer (rx_w_ptr) is used as safety buffer. When the write pointer (rx_w_ptr) would enter this region (due to a write request from the receiver), a buffer full signal is generated and all hardware writes to the buffer are suppressed. The offset is hard coded to 8 bytes.

Warning: If the software wants to receive a complete 1kbyte block (when RXLEN = 0), then it must read out at least 8 bytes of data from the buffer. In this case, the hardware can write the 1024 bytes without being stopped by the rx buffer full signal.

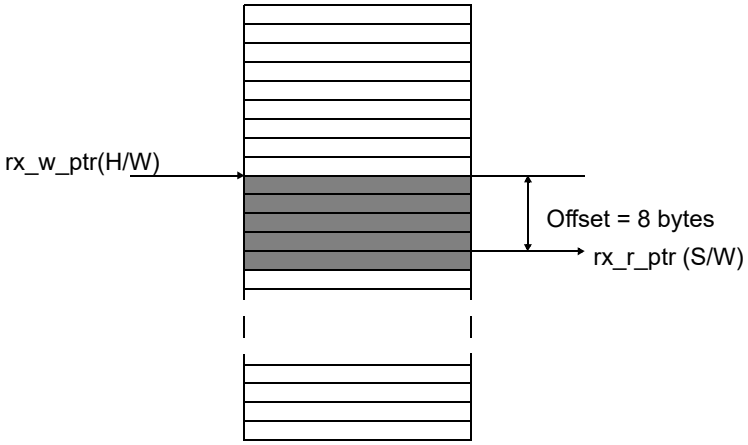


Figure 311. Buffer full situation

123.5.2 Buffer full interrupt

The buffer full interrupt is given when the difference between the hardware write pointer (rx_w_ptr) and the software read pointer (rx_r_ptr) is less than 1/8 of the buffer size. The way it works is the same as with the buffer full situation, only is the interrupt active when the security zone is entered. The buffer full interrupt is active for 1 system clock cycle. When the software reads out data from the buffer, the security zone shifts together with the read pointer (rx_r_ptr) pointer. Each time the hardware write pointer (rx_w_ptr) enters the security zone, a single interrupt is given.

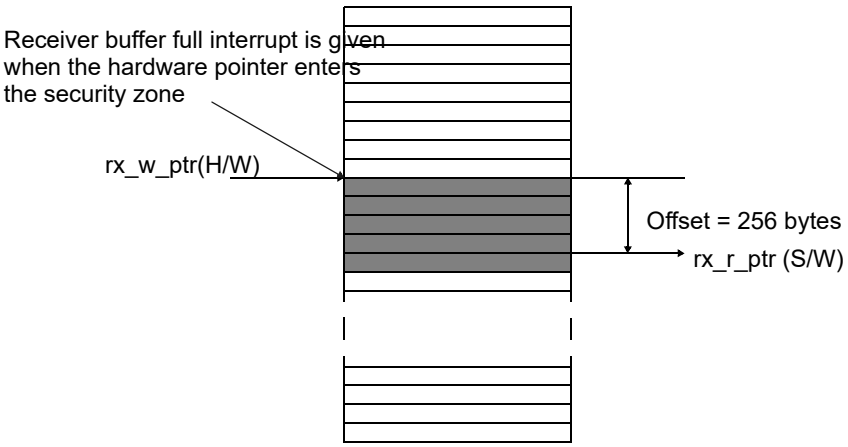


Figure 312. Buffer full interrupt (buffers size is 2kbyte in this example)

123.6 Command Link Control Word interface (CLCW)

The Command Link Control Word (CLCW) is inserted in the Telemetry Transfer Frame by the Telemetry Encoder (TM) when the Operation Control Field (OPCF) is present. The CLCW is created by the software part of the telecommand decoder. The telecommand decoder hardware provides two registers for this purpose which can be accessed via the AMBA AHB bus. Note that bit 16 (No RF Available) and 17 (No Bit Lock) of the CLCW are not possible to write by software. The information carried in these bits is based on discrete inputs.

Two PacketAsynchronous interfaces (PA) are used for the transmission of the CLCW from the telecommand decoder. The protocol is fixed to 115200 baud, 1 start bit, 8 data bits, 1 or 2 stop bits (configured by generics), with a BREAK command for message delimiting (sending 13 bits of logical zero).

The CLCWs are automatically transferred over the PA interface after reset, on each write access to the CLCW register and on each change of the bit 16 (No RF Available) and 17 (No Bit Lock).

*Table 1827.*CLCW transmission protocol

Byte Number	**CLCWR register bits**	**CLCW contents**						
First	[31:24]	Control Word Type	CLCW Version Number	Status Field	COP In Effect			
Second	[23:16]	Virtual Channel Id	Reserved Field					
Third	[15:8]	No RF Available	No Bit Lock	Lock Out	Wait	Retransmit	Farm B Counter	Report Type
Fourth	[7:0]	Report Value						
Fifth	N/A	[RS232 Break Command]						

123.7 Configuration Interface (AMBA AHB slave)

The AMBA AHB slave interface supports 32 bit wide data input and output. Since each access is a word access, the two least significant address bits are assumed always to be zero, address bits 23:0 are decoded. Note that address bits 31:24 are not decoded and should thus be handled by the AHB arbiter/decoder. The address input of the AHB slave interfaces is thus incompletely decoded. Misaligned addressing is not supported. For read accesses, unmapped bits are always driven to zero.

The AMBA AHB slave interface has been reduced in function to support only what is required for the TC. The following AMBA AHB features are constrained:

- Only supports HSIZE=WORD, HRESP_ERROR generated otherwise
- Only supports HMASTLOCK='0', HRESP_ERROR generated otherwise
- Only support HBURST=SINGLE or INCR, HRESP_ERROR generated otherwise
- No HPROT decoding
- No HSPLIT generated
- HRETRY is generated if a register is inaccessible due to an ongoing reset.
- HRESP_ERROR is generated for unmapped addresses, and for write accesses to register without any writeable bits
- Only big-endianness is supported.

During a channel reset the RRP and RWP registers are temporary unavailable. The duration of this reset-inactivity is 8 HCLK clock periods and the AHB-slave generates a HRETRY response during this period if an access is made to these registers.

If the channel reset is initiated by or during a burst-access the reset will execute correctly but a part of the burst could be answered with a HRETRY response. It is therefore not recommended to initiate write bursts to the register.

GRTC has interrupt outputs, that are asserted for at least two clock periods on the occurrence of one of the following events:

- 'CLTU stored' (generated when CLTU has been stored towards the AMBA bus, also issued for abandoned CLTUs)
- 'Receive buffer full' (generated when the buffer has less than 1/8 free) (note that this interrupt is issued on a static state of the buffer, and can thus be re-issued immediately after the corresponding register has been read out by software, it should be masked in the interrupt controller to avoid an immediate second interrupt).
- 'Receiver overrun' (generated when received data is dropped due to a reception overrun)
- 'CLTU ready' (note that this interrupt is also issued for abandoned CLTUs)
- FAR interrupt 'Status Survey Data'
- CLCW interrupt 'Bit Lock'
- CLCW interrupt 'RF Available'

123.7.1 Miscellaneous

The accuracy of the transmission or reception baud rate of the bit asynchronous serial interface is dependent on the selected system frequency and baud rate. The number of system clock periods used for sending or receiving a bit is directly proportional to the integer part of the division of the system frequency with the baud rate.

The BREAK command received on the bit asynchronous serial interface is a sequence of logical zeros that is at least one bit period longer than the normal byte frame, i.e. start bit, eight data bits, optional parity, one or two stop bits. When transmitted, it is always 13 bits.

123.8 Interrupts

The core generates the interrupts defined in table 1828.

*Table 1828.*Interrupts

Interrupt offset	Interrupt name	Description
1:st	RFA	RF Available changed
2:nd	BLO	Bit Lock changed
3:rd	FAR	FAR available
4:th	CR	CLTU ready/aborted
5:th	RBF	Output buffer full
6:th	OV	Input data overrun
7:th	CS	CLTU stored

123.9 Miscellaneous

123.9.1 Numbering and naming conventions

Convention according to the CCSDS recommendations, applying to time structures:

- The most significant bit of an array is located to the left, carrying index number zero.
- An octet comprises eight bits.

*Table 1829.*CCSDS n-bit field definition

CCSDS n-bit field		
most significant		least significant
0	1 to n-2	n-1

Convention according to AMBA specification, applying to the APB/AHB interfaces:

- Signal names are in upper case, except for the following:
- A lower case 'n' in the name indicates that the signal is active low.
- Constant names are in upper case.
- The least significant bit of an array is located to the right, carrying index number zero.
- Big-endian support.

*Table 1830.*AMBA n-bit field definition

AMBA n-bit field		
most significant		least significant
n-1	n-2 down to 1	0

General convention, applying to all other signals and interfaces:

- Signal names are in mixed case.
- An upper case '_N' suffix in the name indicates that the signal is active low.

123.9.2 Performance

The uplink bit rate is supported in the range of 1 kbits/s to 1 Mbits/s.

The bit rate is set to 115200 bit/s for the PacketAsynchronous (PA) interfaces.

123.10 Registers

The core is programmed through registers mapped into AHB I/O address space.

*Table 1831.*GRTC registers

AHB address offset	Register
0x00	Global Reset Register (GRR)
0x04	Global Control Register (GCR)
0x08	Physical Interface Mask Register (PMR)
0x0C	Spacecraft Identifier Register (SIR)
0x10	Frame Acceptance Report Register (FAR)
0x14	CLCW Register 1 (CLCWR1)
0x18	CLCW Register 2 (CLCWR2)
0x1C	Physical Interface Register (PHIR)
0x20	Control Register (COR)
0x24	Status Register (STR)
0x28	Address Space Register (ASR)
0x2C	Receive Read Pointer Register (RRP)
0x30	Receive Write Pointer Register (RWP)
0x60	Pending Interrupt Masked Status Register (PIMSR)
0x64	Pending Interrupt Masked Register (PIMR)
0x68	Pending Interrupt Status Register (PISR)
0x6C	Pending Interrupt Register (PIR)
0x70	Interrupt Mask Register (IMR)
0x74	Pending Interrupt Clear Register (PICR)

123.10.1Global Reset Register (GRR)

Table 1832. 0x00 - GRR - Global Reset Register

31 24	23 1	0
SEB	RESERVED	SRST
0	0	0
w	r	rw

31: 24 SEB (Security Byte):

Write: '0x55'= the write will have effect (the register will be updated).
Any other value= the write will have no effect on the register.

Read: All zero.

23: 1 RESERVED

Write: Don't care.

Read: All zero.

0 System reset (SRST): **[1]**

Write: '1'= initiate reset,'0'= do nothing

Read: '1'= unsuccessful reset, '0'= successful reset

123.10.2Global Control Register (GCR)

Table 1833. 0x04 - GCR - Global Control Register

31 24	23 13	12	11	10	9 0
SEB	RESERVED	PSS	NRZM	PSR	RESERVED
0	0	1	0	0	0
w	r	rw*	rw*	rw*	r

31: 24 SEB (Security Byte):

Write: '0x55'= the write will have effect (the register will be updated).
Any other value= the write will have no effect on the register.

Read: All zero.

23: 13 RESERVED

Write: Don't care.

Read: All zero.

12 PSS (ESA/PSS enable) [11]

Write/Read: '0'= disable, '1'= enable [Read-only when gHardware VHDL generic set.]

11 NRZM (Non-Return-to-Zero Mark Decoder enable)

Write/Read: '0'= disable, '1'= enable [Read-only when gHardware VHDL generic set.]

10 PSR (Pseudo-De-Randomiser enable)

Write/Read: '0'= disable, '1'= enable [Read-only when gHardware VHDL generic set.]

9: 0 RESERVED

Write: Don't care.

Read: All zero.

Power-up default: 0x00001000, The default value depends on the TCC_PSS, TCC_Mark, TCC_Pseudo inputs.

123.10.3Physical Interfice Mask Register (PMR)

Table 1834. 0x08 -PMR - Physical Interface Mask Register

31 8	7 0
RESERVED	MASK
0	0
r	rw

31: 8 RESERVED

Write: Don’t care.

Read: All zero.

7: 0 MASK

Write: Mask TC input when set, bit 0 corresponds to TC input 0

Read: Current mask

123.10.4Spacecraft Identifier Register (STR)

Table 1835. 0x0C - SIR - Spacecraft Identifier Register [7]

31 10	9 0
RESERVED	SCID
0	*
r	r

31: 10 RESERVED

Write: Don’t care.

Read: All zero.

9: 0 SCID (Spacecraft Identifier)

Write: Don’t care.

Read: Bit[9]=MSB, Bit[0]=LSB

Power-up default: Depends on SCID input configuration.

123.10.5Frame Acceptance Report Register (FAR)

Table 1836. 0x10 - FAR - Frame Acceptance Report Register [7]

31	30 25	24 19	18 16	15 14	13 11	10 0
SSD	RESERVED	CAC	CSEC	RESERVED	SCI	RESERVED
0	0	0	0	0	0b111	0
r	r	r	r	r	r	r

31 SSD (Status of Survey Data) (see [PSS-04-151])

- Write: Don't care.
- Read: Automatically cleared to 0 when any other field is updated by the coding layer. Automatically set to 1 upon a read.

30: 25 RESERVED

- Write: Don't care.
- Read: All zero.

24: 19 CAC (Count of Accept Codeblocks) (see [PSS-04-151])

- Write: Don't care.
- Read: Information obtained from coding layer. [2]

18: 16 CSEC (Count of Single Error Corrections) (see [PSS-04-151])

- Write: Don't care.
- Read: Information obtained from coding layer.

15: 14 RESERVED

- Write: Don't care.
- Read: All zero.

13: 11 SCI (Selected Channel Input) (see [PSS-04-151])

- Write: Don't care.
- Read: Information obtained from coding layer.

10: 0 RESERVED

- Write: Don't care.
- Read: All zero.

123.10.6CLCW Register (CLCWRx)

*Table 1837.*0x14 - CLCWRx - CLCW Register (see [PSS-04-107])

31	30 29	28 26	25 24	23 18	17 16	15	14	13	12	11	10 9	8	7 0
CWTY	VNUM	STAF	CIE	VCI	RESERVED	NRFA	NBLO	LOUT	WAIT	RTMI	FBCO	RTYPE	RVAL
0	0	0	0	0	0	0	0	0	0	0	0	0	0
rw	rw	rw	rw	rw	rw	r	r	rw	rw	rw	rw	rw	rw

31 CWTY (Control Word Type)

30: 29 VNUM (CLCW Version Number)

28: 26 STAF (Status Fields)

25: 24 CIE (COP In Effect)

23: 18 VCI (Virtual Channel Identifier)

17: 16 Reserved (PSS/ECSS requires “00”)

15 NRFA (No RF Available)

Write: Don’t care.

Read: Based on discrete inputs.

14 NBLO (No Bit Lock)

Write: Don’t care.

Read: Based on discrete inputs.

13 LOUT (Lock Out)

12 WAIT (Wait)

11 RTMI (Retransmit)

10: 9 FBCO (FARM-B Counter)

8 RTYPE (Report Type)

7: 0 RVAL (Report Value)

123.10.7Physical Interface Register (PHIR)

*Table 1838.*0x1C - PHIR - Physical Interface Register [7]

31 16	15 8	7 0
RESERVED	RFA	BLO
0	*	*
r	r	r

31: 16 RESERVED

Write: Don’t care.

Read: All zero.

15: 8 RFA (RF Available) [3]

Only implemented inputs are taken into account. All other bits are zero.

Write: Don’t care.

Read: Bit[8] = input 0, Bit[15] = input 7

7: 0 BLO (Bit Lock) [3]

Only implemented inputs are taken into account. All other bits are zero.

Write: Don’t care.

Read: Bit[0] = input 0, Bit[7] = input 7

123.10.8Control Register (COR)

*Table 1839.*0x20 - COR - Control Register

31 24	23 10	9	8 1	0
SEB	RESERVED	CRST	RESERVED	RE
0	0	0	0	*
w	r	rw	r	rw

31: 24 SEB (Security Byte):

Write: '0x55'= the write will have effect (the register will be updated). Any other value= the write will have no effect on the register.

Read: All zero.

23: 10 RESERVED

Write: Don't care.

Read: All zero.

9 CRST (Channel reset) [4]

Write: '1'= initiate channel reset,'0'= do nothing

Read: '1'= unsuccessful reset, '0'= successful reset

8: 1 RESERVED

Write: Don't care.

Read: All zero.

0 RE (Receiver Enable) [Always enabled when gHardware VHDL generic set.]

The TCActive input of the receiver are masked when the RE bit is disabled.

Read/Write: '0'= disabled, '1'= enabled

Power-up default: 0x00000000 [0x00000001 when gHardware VHDL generic set.]

123.10.9Status Register (STR)

*Table 1840.*0x24 - STR - Status Register [7]

31 11	10	9 8	7	6 5	4	3 1	0
RESERVED	RBF	RESERVED	RFF	RESERVED	OV	RESERVED	CR
0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r

31: 11 RESERVED

Write: Don’t care.

Read: All zero.

10 RBF (RX BUFFER Full)

Write: Don’t care.

Read: ‘0’ = Buffer not full,

‘1’= Buffer full (this bit is set if the buffer has less then 1/8 of free space)

9: 8 RESERVED

Write: Don’t care.

Read: All zero.

7 RFF (RX FIFO Full)

Write: Don’t care.

Read: ‘0’ = FIFO not full, ‘1’ = FIFO full

6: 5 RESERVED

Write: Don’t care.

Read: All zero.

4 OV (Overrun) [5]

Write: Don’t care.

Read: ‘0’= nominal, ‘1’= data lost

3: 1 RESERVED

Write: Don’t care.

Read: All zero.

0 CR (CLTU Ready) [5]

There is a worst case delay from the CR bit being asserted, until the data has actually been transferred from the receiver FIFO to the ring buffer. This depends on the PCI load etc.

Write: Don’t care.

Read: ‘1’= new CLTU in ring buffer. ‘0’= no new CLTU in ring buffer.

123.10.10 Address Space Register (ASR)

*Table 1841.*0x28 - ASR - Address Space Register [8]

31 10	9 8	7 0
BUFST	RESERVED	RXLEN
0	0	0
rw	r	rw

31: 10 BUFST (Buffer Start Address)

22-bit address pointer

This pointer contains the start address of the allocated buffer space for this channel.

Register has to be initialized by software before DMA capability can be enabled.

9: 8 RESERVED

Write: Don't care.

Read: All zero.

7: 0 RXLEN *(RX buffer length)*

Number of 1kB-blocks reserved for the RX buffer.
(Min. 1kByte = 0x00, Max. 256kByte = 0xFF)

123.10.11 Receive Read Pointer Register (RRP)

*Table 1842.*0x2C - RRP - Receive Read Pointer Register [6] [9][10]

31 24	23 0
RxRd Ptr Upper	RxRd Ptr Lower
0	0
r	rw

31: 24 10-bit upper address pointer

Write: Don't care.

Read: This pointer = ASR[31..24].

23: 0 24-bit lower address pointer.

This pointer contains the current RX read address. This register is to be incremented with the actual amount of bytes read.

123.10.12 Receive Write Pointer Register (RWP)

*Table 1843.*0x30 - RWP - Receive Write Pointer Register [6] [9]

31 24	23 0
RxWr Ptr Upper	RxWr Ptr Lower
0	0
r	r

31: 24 10-bit upper address pointer

Write: Don't care.

Read: This pointer = ASR[31..24].

23: 0 24-bit lower address pointer.

This pointer contains the current RX write address. This register is incremented with the actual amount of bytes written.

Legend:

[1] The global system reset caused by the SRST-bit in the GRR-register results in the following actions:

- Initiated by writing a '1", gives '0' on read-back when the reset was successful.

- No need to write a '0' to remove the reset.

- Unconditionally, means no need to check/disable something in order for this reset-function to correctly execute.
- Could of course lead to data-corruption coming/going from/to the reset core.
- Resets the complete core (all logic, buffers & register values)
- Behaviour is similar to a power-up.

[2] The FAR register supports the CCSDS/ECSS standard frame lengths (1024 octets), requiring an 8 bit CAC field instead of the 6 bits specified for PSS. The two most significant bits of the CAC will thus spill over into the "LEGAL/ILLEGAL" FRAME QUALIFIER field, Bit [26:25]. This is only the case when the PSS bit is set to '0'.

[3] The number of channels are controlled with the gRFAvailable and gBitLock VHDL generics, respectively.

[4] The channel reset caused by the CRST-bit in the COR-register results in the following actions:
- Initiated by writing a '1", gives '0' on read-back when the reset was successful.
- No need to write a '0' to remove the reset.
- All other bit's in the COR are neglected (not looked at) when the CRST-bit is set during a write, meaning that the value of these bits has no impact on the register-value after the reset.
- Unconditionally, means no need to check/disable something in order for this reset-function to correctly execute.
- Could of course lead to data-corruption coming/going from/to the reset channel.
- Resets the complete channel (all logic, buffers & register values)
- Except the ASR-register of that channel which remains it's value.
- All read- and write-pointers are automatically re-initialized and point to the start of the ASR-address.
- All registers of the channel (except the ones described above) get their power-up value.
- This reset shall not cause any spurious interrupts.

[5] These bits are sticky bits which means that they remain present until the register is read and that they are cleared automatically by reading the register.

[6] The value of the pointers depends on the content of the corresponding Address Space Register (ASR). During a system reset, a channel reset or a change of the ASR register, the pointers are recalculated based on the values in the ASR register.
The software has to take care (when programming the ASR register) that the pointers never have to cross a 16MByte boundary (because this would cause an overflow of the 24-bit pointers).
It is not possible to write an out of range value to the RRP register. Such access will be ignored with an HERROR.

[7] An AMBA AHB ERROR response is generated if a write access is attempted to a register without any writeable bits.

[8] The channel reset caused by a write to the ASR-register results in the following actions:
- Initiated by writing an updated value into the ASR-register.
- Unconditionally, means no need to check/disable something in order for this reset-function to correctly execute.
- Could of course lead to data-corruption coming/going from/to the reset channel.
- Resets the complete channel (all logic & buffers) but not all register values, only the following:
- COR-register, TE & RE bits get their power-up value, other bits remain their value.
- STR-register, all bits get their power-up value
- Other registers remain their value
- Updates the ASR-register of that channel with the written value
- All read- and write-pointers are automatically re-initialized and point to the start of the ASR-address.
- This reset shall not cause any spurious interrupts

[9] During a channel reset the register is temporarily unavailable and HRETRY response is generated if accessed.

[10] It is not possible to write an out of range value to the RRP register. Such access will be ignored without an error.

[11] The PSS bit usage is only supported if the gPSS generic is set on the TCC module.

123.10.13Interrupt registers

The interrupt registers give complete freedom to the software, by providing means to mask interrupts, clear interrupts, force interrupts and read interrupt status.

When an interrupt occurs the corresponding bit in the Pending Interrupt Register is set. The normal sequence to initialize and handle a module interrupt is:

- Set up the software interrupt-handler to accept an interrupt from the module.
- Read the Pending Interrupt Register to clear any spurious interrupts.
- Initialize the Interrupt Mask Register, unmasking each bit that should generate the module interrupt.
- When an interrupt occurs, read the Pending Interrupt Status Register in the software interrupt-handler to determine the causes of the interrupt.
- Handle the interrupt, taking into account all causes of the interrupt.
- Clear the handled interrupt using Pending Interrupt Clear Register.

Masking interrupts: After reset, all interrupt bits are masked, since the Interrupt Mask Register is zero. To enable generation of a module interrupt for an interrupt bit, set the corresponding bit in the Interrupt Mask Register.

Clearing interrupts: All bits of the Pending Interrupt Register are cleared when it is read or when the Pending Interrupt Masked Register is read. Reading the Pending Interrupt Masked Register yields the contents of the Pending Interrupt Register masked with the contents of the Interrupt Mask Register. Selected bits can be cleared by writing ones to the bits that shall be cleared to the Pending Interrupt Clear Register.

Forcing interrupts: When the Pending Interrupt Register is written, the resulting value is the original contents of the register logically OR-ed with the write data. This means that writing the register can force (set) an interrupt bit, but never clear it.

Reading interrupt status: Reading the Pending Interrupt Status Register yields the same data as a read of the Pending Interrupt Register, but without clearing the contents.

Reading interrupt status of unmasked bits: Reading the Pending Interrupt Masked Status Register yields the contents of the Pending Interrupt Register masked with the contents of the Interrupt Mask Register, but without clearing the contents.

The interrupt registers comprise the following:

*Table 1844.*Interrupt registers

Description	Name	Mode
Pending Interrupt Masked Status Register	PIMSR	r
Pending Interrupt Masked Register	PIMR	r
Pending Interrupt Status Register	PISR	r
Pending Interrupt Register	PIR	rw
Interrupt Mask Register	IMR	rw
Pending Interrupt Clear Register	PICR	w

*Table 1845.*Interrupt registers template

31 7	6	5	4	3	2	1	0
-	CS	OV	RBF	CR	FAR	BLO	RFA
	0	0	0	0	0	0	0
	*	*	*	*	‘	*	‘

6: CS CLTU stored*
5: OV Input data overrun*
4: RBF Output buffer full*
3: CR CLTU ready/aborted*

2: FAR FAR available*
1: BLO Bit Lock changed*
0: RFA RF Available Changed*

*See table 1844.

123.11 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x031. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

123.12 Configuration options

Table 1846 shows the configuration options of the core (VHDL generics).

*Table 1846.*Configuration options

Generic	Function	Description	Allowed range	Default
GRLIB AMBA plug&play settings				
hindex	AHB slave index		Integer	0
hirq	AHB slave interrupt		Integer	0
singleirq	Single interrupt	Enable interrupt registers	Integer	0
inputmask	Maskable input		Integer	0
ioaddr	IO area address		0 - 16#FFF#	0
iomask	IO area mask		0 - 16#FFF#	16#FFF#
syncrst	synchronous reset		0 - 1	0
gHardware	Hardware commands	Coding layer fixed configuration & enable	0 - 1	0
Features settings				
gIn	Number of channels	Number of TC channels	1 - 8	3
gPSS	PSS support enable	Enables PSS support	0 - 1	1
gTimeoutMask	Time out mask	Enables masking of input on time out	0 - 1	0
gTimeout	Time out period	2^n clock periods		24
gRFAvailable	Number of RF inputs	Minimum 1	1 - 8	3
gBitLock	Number of TC inputs	Minimum 1	1 - 8	3
gDepth	FIFO depth	words (2^x)		4
Asynchronous bit serial interface settings (CLCW interface)				
gSystemClock	System frequency	[Hz]	Integer	33333333
gBaud	Baud rate	[Baud]	Integer	115200
gOddParity	Odd parity	Odd parity generated, but not checked	0 - 1	0
gTwoStopBits	Number of stop bits	0=one stop bit, 1=two stop bits	0 - 1	0

123.13 Signal descriptions

Table 1847 shows the interface signals of the core (VHDL ports).

*Table 1847.*Signal descriptions

Signal name	Field	Type	Function	Description	Active
HRESETn	N/A	Input	Reset		Low
HCLK	N/A	Input	Clock		-
TCIN	TCC_SCID	Input	Spacecraft Identity	0 is MSB, 9 is LSB	-
	TCACTIVE		Active	Indicate that sub-carrier lock is achieved (or bit lock). Enable for the clock and data.	-
	TCCLK		Bit clock	Serve as the serial data input bit clocks.	-
	TCDATA		Data	Serve as the serial data input. Data are sampled on the TCCLK clock edges when the corresponding TCActive input is asserted.	-
	TCC_HIGH		Active high setting	1=active high delimiter, 0=active low	-
	TCC_RISE		Rising clock edge	1=rising, 0=falling	-
	PSEUDO		Pseudo-Derando-miser	1=enabled, 0=disabled	-
	MARK		NRZ-M decoder	1=NRZ-M, 0=NRZ-L	-
	PSS		PSS/ECSS mode	1=ESA PSS, 256 octet, fill bit aug-ment 0=ECSS, 1024 octet, no fill bit augment	-
	RFAVAILPOS		RF Available polarity	Active high=1 / low=0, used for CLCW	-
	BITLOCKPOS		Bit Lock polarity	Active high=1 / low=0, used for CLCW	-
	CLCWRFAVAIL-ABLE		RF Available	Used for CLCW	-
	CLCWBITLOCK		Bit Lock	Used for CLCW	-
TCOUT	CLCW1DATA	Output	CLCW Data	Bit serial asynchronous data for CLCW 1 interface.	-
	CLCW2DATA		CLCW Data	Bit serial asynchronous data for CLCW 2 interface.	-
AHBSIN	*	Input	AMB slave input signals		-
AHBSOUT	*	Output	AHB slave output signals		-
	HIRQ(hirq+6)		Interrupts (If *singleirq*=1 only one common interrupt will be generate using *hirq*.)	CLTU stored	Location on HIRQ bus depends on *hirq* generic. If *hirq*=0, no interrupt will be generated.
	HIRQ(hirq+5)			Input data overrun	
	HIRQ(hirq+4)			Output buffer full	
	HIRQ(hirq+3)			CLTU ready/aborted	
	HIRQ(hirq+2)			FAR available	
	HIRQ(hirq+1)			Bit Lock changed	
	HIRQ(hirq+0)			RF Available changed	
AHBMIN	*	Input	AMB master input signals		-
AHBMOUT	*	Output	AHB master output signals		-

* see GRLIB IP Library User's Manual

123.14 Signal definitions and reset values

The signals and their reset values are described in table 1848.

*Table 1848.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
tcc_scid	Input, static	Spacecraft Identity	-	-
tcc_high	Input, static	Active high setting	-	-
tcc_rise	Input, static	Rising clock edge	-	-
pseudo	Input, static	Pseudo-Derandomiser	-	-
mark	Input, static	NRZ-M decoder	-	-
pss	Input, static	PSS/ECSS mode	-	-
rfavailpos	Input, static	RF Available polarity	-	-
bitlockpos	Input, static	Bit Lock polarity	-	-
tcactive	Input, async	Active	-	-
tcclk	Input, async	Bit clock	-	-
tcdata	Input, async	Data	-	-
rfavailable	Input, async	RF Available for CLCW	-	-
bitlock	Input, async	Bit Lock for CLCW	-	-
clcw1data	Output	CLCW output data 1	-	Logical 1
clcw2data	Output	CLCW output data 2	-	Logical 1

123.15 Timing

The timing waveforms and timing parameters are shown in figure 313 and are defined in table 1849.

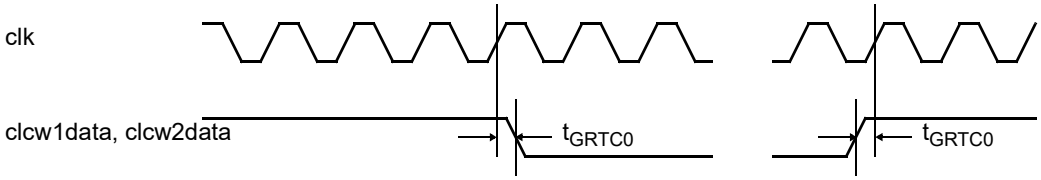


Figure 313. Timing waveforms

*Table 1849.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{GRTC0}	clock to output delay	rising *clk* edge	TBD	TBD	ns

Note: The inputs are re-synchronized internally. The signals do not have to meet any setup or hold requirements. Static signals should not change between resets.

123.16 Library dependencies

Table 1850 shows libraries used when instantiating the core (VHDL libraries).

*Table 1850.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
TMTC	TMTC_Types	Signals, component	Signals and component declaration

123.17 Instantiation

This example shows how the core can be instantiated.

```
library  IEEE;
   use      IEEE.Std_Logic_1164.all;
   library  GRLIB;
   use      GRLIB.AMBA.all;
   library  TMTC;
   use      TMTC.TMTC_Types.all;

...

   component GRTC is
   generic(
      hmstndx:       in    Integer                 := 0;
      hslvndx:       in    Integer                 := 0;
      ioaddr:        in    Integer                 := 0;
      iomask:        in    Integer                 := 16#fff#;
      hirq:          in    Integer                 := 0;
      syncrst:       in    Integer                 := 0;  -- synchronous reset
      gIn:           in    Integer range 1 to  8 := 3;   -- number of inputs
      gPSS:          in    Integer range 0 to  1 := 0;   -- enable PSS support
      gTimeoutMask:  in    Integer range 0 to  1 := 0;   -- timeout mask
      gTimeout:      in    Integer                 := 24;  -- timeout 2^n
      gSystemClock:  in    Natural := 333333333;         -- Hz
      gBaud:         in    Natural := 115200;            -- Baud rate setting
      gOddParity:    in    Natural := 0;                 -- Odd parity
      gTwoStopBits:  in    Natural := 0;                 -- Stop bit selection
      gRFAvailable:  in    Natural range 1 to  8 := 3;   -- No. of RF inputs
      gBitLock:      in    Natural range 1 to  8 := 3;   -- No. of BL inputs
      gDepth:        in    Natural := 4;                 -- words (2^x)
      gHardware:     in    Natural range 0 to 1 := 0);   -- enable hardware cmd
   port(
      -- AMBA AHB system signals
      HCLK:          in    Std_ULogic;                   -- System clock
      HRESETn:       in    Std_ULogic;                   -- Synchronised reset

      -- AMBA AHB slave Interface
      AHBSIn:        in    AHB_Slv_In_Type;              -- AHB slave input
      AHBSOut:       out   AHB_Slv_Out_Type;             -- AHB slave output

      -- AMBA AHB master Interface
      AHBMIn:        in    AHB_Mst_In_Type;              -- AHB master input
      AHBMOut:       out   AHB_Mst_Out_Type;             -- AHB master output

      -- Telecommand interfaces
      TCIn:          in    GRTC_In_Type;
      TCOut:         out   GRTC_Out_Type);
   end component GRTC;
```

124 TCAU - Telecommand Decoder Authentication Unit

124.1 Overview

The TCAU is compatible with the Telecommand Decoder Specification defined by [PSS-04-151] and implements authentication in accordance with [CCSDS-350.0] as defined by Option B, authentication of segment. The TCAU is placed between the Transfer Sublayer and the Segmentation Sublayer.

The TCAU authentication method is a plain text with appended signature. It is based on a one-way function called “hard knapsack”, which relies on a 40-bit digital signature generated by applying a secret key on the segment. The same algorithm is used for generating the signature in the transmitting end as in the receiving end.

124.2 Operation

The TCAU receives segments from the transfer sublayer octet by octet, starting with the segment header. By comparing the 5 LSBs of the segment header, the MAP address, with the configuration signal *aumap*, the TCAU determines if the segment is to be authenticated. If the *auenable* input signal is high, all segments where the MAP address is less than or equal to *aumap* will be sent to the Authentication Processor for authentication. Segments where the MAP address is higher than *aumap*, will be sent to the segmentation sublayer without processing. A special case exists for segments where the entire MAP ID equals 63. These are dedicated for the Control Command Processor of the TCAU and are always authenticated, see further section 124.9. The control commands are used to change the internal configuration of the TCAU and are always unsegmented, i.e. the segmentation flags are set to 11b.

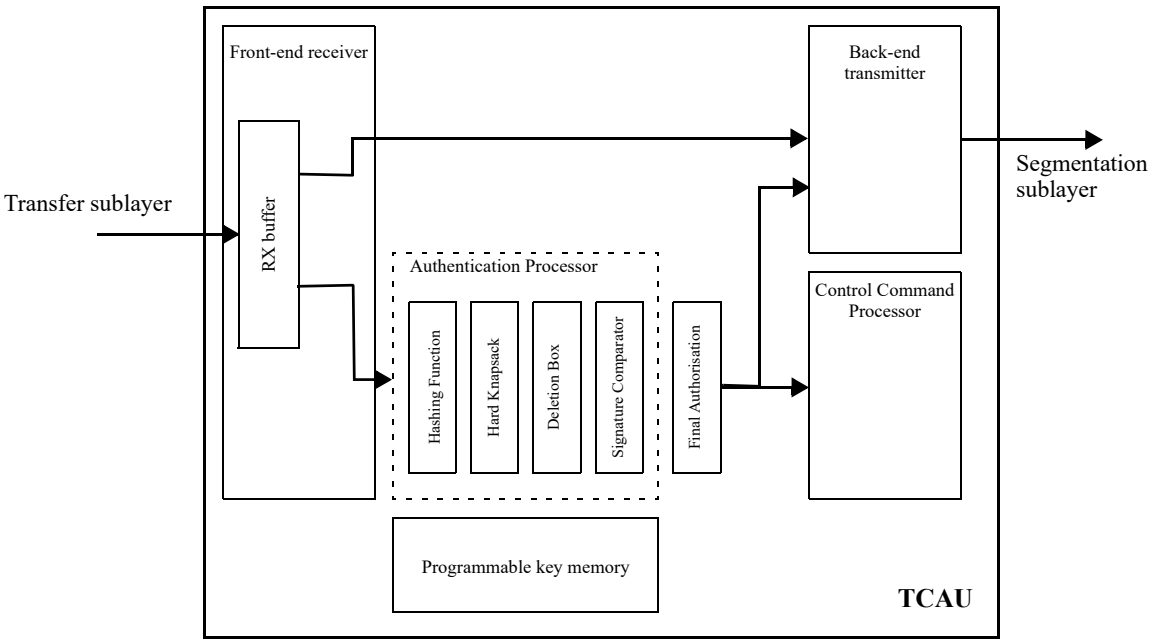


Figure 314. Block diagram

The TCAU contains the following major functions:

- Front-end receiver
- Authentication Processor
- Final Authorisation
- Control Command Processor

- Programmable key
- Back-end transmitter

124.3 References

[PSS-04-151] Telecommand Decoder Specification, ESA PSS-04-151, issue 1

[CCSDS-350.0] The Application of CCSDS Protocols to Secure Systems, CCSDS 350.0-G-2, issue 2

124.4 Data structures

Table 1851 shows the structure of a telecommand segment with the optional authentication tail used by the TCAU. The authentication tail is mandatory for all segments that are to be authenticated.

*Table 1851.*Telecommand segment with authentication tail

<table>
<tr><td colspan="7">Telecommand segment with optional tail</td></tr>
<tr><td colspan="3">Segment header</td><td rowspan="2">Segment data field</td><td colspan="3">Authentication tail (optional)</td></tr>
<tr><td rowspan="2">Sequence flags</td><td colspan="2">MAP identifier</td><td colspan="2">Logical authentication channel (LAC)</td><td rowspan="2">Signature</td></tr>
<tr><td>Control flag</td><td>MAP address</td><td>LAC ID</td><td>LAC count</td></tr>
<tr><td>2 bits</td><td>1 bit</td><td>5 bits</td><td>0 to 239 octets or</td><td>2 bits</td><td>30 bits</td><td>40 bits</td></tr>
<tr><td colspan="3">1 octet</td><td>0 to 248 octets</td><td colspan="3">0 or 9 octets</td></tr>
<tr><td colspan="7">1 to 249 octets</td></tr>
</table>

124.5 Front-end receiver

The front-end receiver handles reception of octets from the Transfer sublayer using a handshaking protocol. Octets are placed in a 10 octet buffer, in order to accommodate the entire authentication tail. The front-end receiver counts all octets received to determine the segment length. The octets are passed on to the Authentication Processor and the Back-end transmitter.

124.6 Authentication Processor

The Authentication Processor receives the entire segment from the Front-end receiver and calculates the 40-bit digital signature using one of two on-board keys: the fixed key or the programmable key. The 40-bit digital signature is compared to the signature in the authentication tail appended to the segment. The Authentication Processor comprises the following functions:

- Hashing Function
- Hard Knapsack
- Deletion Box
- Signature Comparator

124.6.1 Hashing Function

The Hashing Function generates i 60-bit pre-signature by shifting the extended message, x, into a linear feedback shift register (LFSR). The extended message comprises the segment header, segment data, received LAC from the authentication tail and finally filler bits, comprising 24 zeros, to ensure a minimum length of the extended message. The coefficients of the LFSR are part of the keys.

When a new segment is received, the LFSR is initialized to 1000...000, i.e. bit 0 is set to 1 and all other bits are set to zero. When the entire extended message has been shifted into the LFSR, it will contain the pre-signature, P.

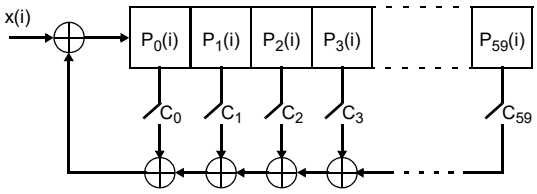


Figure 315. Hashing Function

124.6.2 Hard Knapsack

The purpose of the Hard Knapsack function is to make the overall system non-linear and to serve as a true one-way function, so that it is not possible to calculate the pre-signature from the signature. The Hard Knapsack consists of 60 weights, which are part of the two on-board keys, with each weight being 48 bits long. It is defined by the following transformation:

$$S' = \left(\sum_{j=0}^{59} P_j W_j \right) \; mod \; 2^{48}$$

Where P is the pre-signature calculated by the Hashing Function, i.e. each bit of the pre-signature selects the corresponding weight for the Hard Knapsack function.

The result of the Hard Knapsack function is the 48-bit knapsack sum, S'.

124.6.3 Deletion Box

The Deletion Box removes the 8 least significant bits, i.e. bits 40 to 47, from the knapsack sum, S', to form the authentication signature, S. It has been shown that the least significant bits are too weak from a cryptanalysis standpoint.

124.6.4 Signature Comparator

The Signature Comparator compares the received signature, s, with the calculated signature, S, and presents the result to the Final Authorisation function of the Supervisor.

124.7 Final Authorisation

When the received signature (s) and the calculated signature (S) are found to be identical, the Final Authorisation function checks that the received LAC count is identical to the LAC count of the counter indicated by the received LAC ID. If these match, the used LAC counter is incremented by 1. Note that the LAC counter is incremented even if the segment contains a control command which is found to be incorrect.

If the telecommand segment was transferred on MAP 63, it is transferred to the Control Command Processor.

The Final Authorisation also generates a report on the output *auana*, outputs the MAP on *lastmap* and pulses *auanavalid* for one clock cycle.

124.8 Control Command Processor

The Control Command Processor executes the control commands used for changing the internal configuration of the TCAU. Any commands not conforming to the specified formats are reported as non-executable.

124.9 Control Commands

Before being executed, the following checks are performed on the control commands:

- The sequence flags of the segment header are verified to be 11b (unsegmented)
- The segment is verified to contain a valid control command
- The length of the segment is verified to comply with the expected length of the command
- The LAC ID for a “Set new LAC count value” command is verified to be 00b, 01b or 10b
- The start address of a “Change programmable key block B” command is verified to be less than 112

If a segment is transferred to the Control Command Processor and fails any of these checks, it is discarded and reported in *auana*.

The control commands are listed in table 1852. Table 1853, 1854 and 1855 shows the layout of the three groups of control commands.

*Table 1852.*Authentication Unit Control Commands

Group	Control Command Identifier	Command name
1	0000 0000	Dummy segment
	0000 0101	Select fixed key
	0000 0110	Select programmable key
	0000 0111	Load fixed key in programmable key memory
2	0000 1001	Set new LAC count value
3	0000 1010	Change programmable key block A
	0000 1011	Change programmable key block B

*Table 1853.*Group 1 control commands

Segment header	Control command identifier	Authentication tail
0xFF	00000***	LAC + Signature
1 octet	1 octet	9 octets

*Table 1854.*Group 2 control commands

Segment header	Control command identifier	LAC value to be set		Authentication tail
0xFF	00001001	LAC ID	LAC count	LAC + Signature
1 octet	1 octet	2 bits	30 bits	9 octets

*Table 1855.*Group 3 control commands

Segment header	Control command identifier	Start address	Key-specific pattern	Authentication tail
0xFF	0000101*			LAC + Signature
1 octet	1 octet	1 octet	7 octets	9 octets

124.9.1 Dummy segment

This control command is provided for testing purposes. It has no side effects when executed, but since it is authenticated, the LAC counters will be updated and a new report will be generated.

This command is authenticated with the currently selected key.

124.9.2 Select fixed key

If authentication is successful, the result of the command is that the fixed key will be used for subsequent segments.

This control command is always authenticated using the fixed key.

124.9.3 Select programmable key

If authentication is successful, the result of the command is that the programmable key will be used for subsequent segments.

This control command is always authenticated using the programmable key.

124.9.4 Load fixed key in programmable key memory

This control command will copy the weights and the coefficients of the fixed key to the programmable key.

This command is authenticated with the currently selected key.

124.9.5 Set new LAC count value

This command sets the value of either of the three LAC counters, as determined by the LAC ID identifier in the segment data field. If authentication is successful, the selected LAC will be loaded with the value specified in the LAC count field in the segment data. The new LAC value is set after Final Authorisation, which means that if the same LAC is used for authentication, it will get it’s new value after being incremented.

This command is authenticated with the currently selected key.

124.9.6 Change programmable key block

There are two change programmable key commands:

- Command A is used to change blocks starting at the first 256 octets
- Command B is used to change blocks starting at the last 112 octets

These commands changes five octets of the programmable key, starting at the address defined by the start address field in the segment data.

Generation of the five octets to be written to the programmable key is accomplished as follows:

Once the segment has been authorised by the Final Authorisation, the segment except the signature is inverted and passed once more through the Authentication Processor. The 24 bits of virtual fill z are

inserted without being inverted. The resulting 40-bit pseudo-signature is then loaded into the programmable key memory as follows:

- Bits 32 through 39 of the “pseudo-signature” are loaded into the octet indicated by the start address field in Bank A or Bank B.
- Bits 24 through 31 of the “pseudo-signature” are loaded into the octet at the next higher address (i.e. at start address + 1)
- And so on, until bits 0 through 7 are loaded into the octet indicated by the (start address field + 4)

The organization of the programmable key for the purpose of this command is depicted in table 1856.

*Table 1856.*Programmable key organization

Bank	Address	Authentication key		
A	0	40	W0(40 to 47)	47
	1	32	W0(32 to 39)	39
	2	24	W0(24 to 31)	31
	3	16	W0(16 to 23)	23
	4	8	W0(8 to 15)	15
	5	0	W0(0 to 7)	7
	6	40	W1(40 to 47)	47
	7	32	W1(32 to 39)	39
	255	16	W42(16 to 23)	23
B	0	8	W42(8 to 15)	15
	103	0	W59(0 to 7)	7
	104		59 C(59 to 56)	56
	105	55	C(55 to 48)	48
	106	47	C(47 to 40)	40
	107	39	C(39 to 32)	32
	108	31	C(31 to 16)	24
	109	23	C(23 to 16)	16
	110	15	C(15 to 8)	8
	111	7	C(7 to 0)	0

124.10 Programmable Key Memory

The weights of the programmable key is stored in an internal memory in the TCAU, while the coefficients are stored in registers. The memory is protected by TMR, to avoid errors in the weights. To remove bit flips from the memories, the programmable key is scrubbed (cf. section 124.10.1)

124.10.1Scrubber

The TCAU contains a scrubber that scrubs the programmable key memory whenever the core is idle. The scrubber reads each octet from the memory and writes them back unconditionally, thereby ensuring that all three memories get the same value.

124.11 Fixed Key

The fixed key is provided to the TCAU by means of the input signal *fixedkey*.

124.12 Back-end transmitter

The Back-end transmitter is a serial output that can be connected to a Segmentation sublayer. The TCAU can function without connecting the Back-end transmitter, if the Segmentation sublayer receives the segment independently from the TCAU, e.g. reads them from a memory. In this case, the authentication result signals from the Final Authorisation is sufficient for the Segmentation sublayer to determine if the segment is to be processed.

The Back-end transmitter receives octets directly from the Front-end receiver buffer.

124.12.1Non-authenticated segments

Segments transmitted on non-authenticated MAPs or while the AU is disabled, are output independently of the Authentication Processor. In this case, the entire segment is transmitted on the serial link.

124.12.2Authenticated data segments

For authenticated data segments, the Back-end transmitter transmits the segment in parallel with the authentication process, to avoid having to buffer the entire segment. To be able to remove the authentication tail from the segment, the Back-end transmitter always waits until the Front-end receiver buffer contains at least 10 octets or the Front-end receiver has received the entire segment. When the entire segment has been received and the buffer contains less than 10 octets, all of these belong to the authentication tail.

When the entire segment has been received, the Back-end transmitter waits until the Final Authorisation function has completed before completing the transfer. If the authorisation fails, the transfer is aborted and if the authorisation succeeds, the transfer is completed.

124.12.3Control Commands

If a segment containing a control command is received, the Back-end transmitter consumes all data without transmitting any octets.

124.13 Cold start state

After reset, the TCAU is in the following state:

- Fixed key is in use
- Principal LAC and Auxiliary LAC are all ones
- Recovery LAC is *rlac_rstval_c*
- Programmable key is unknown

124.14 Registers

The core does not implement any memory mapped registers.

124.15 Implementation

124.15.1Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core implements a separate generic for selecting between synchronous and asynchronous reset and resets all registers in both configurations.

124.16 Configuration options

Table 1857 shows the configuration options of the core (VHDL generics).

*Table 1857.*Configuration options

Generic	Function	Allowed range	Default
tech	Selects technology for the programmable key memory.	0 - NTECH	inferred
syncrst	Enable synchronous reset.	0 - 1	0
ft	Enable fault-tolerance against SEU errors. The core can optionally be implemented with fault-tolerance against SEU errors in the programmable key memory. The fault-tolerance is enabled through the ft VHDL generic to 1. If ft is set to 1, TMR memories will be implemented.	0-1	0

124.17 Signal descriptions

Table 1858 shows the interface signals of the core (VHDL ports).

*Table 1858.*Signal descriptions

Signal name	Field	Type	Function	Description	Active
RST_N	N/A	Input	Synchronous reset		Low
ARST_N	N/A	Input	Asynchronous reset		Low
CLK	N/A	Input	Clock		-
TLCRI	BEGINS	Input	Data unit start	Pulses when a new segment is to be sent from the transfer sublayer.	High
	PROGRESSES		In progress	High throughout the segment transfer.	High
	COMPLETES		End of data	Pulses to indicate the successful completion of a segment transfer.	High
	ABORTS		Abort data unit	Pulses to indicate the erroneous completion of a segment transfer.	High
	REQUEST		Data valid strobe	Pulses to transmit a new octet to the TCAU from the transfer sublayer.	High
	DATA		8-bit data	Segment data	-
TLCRO	ACCEPTING	Output	Ready for segment	Indicates that the TCAU is idle and can accept a new segment. When this output transits from low to high, it indicates that a segment has been fully processed, including any control command processing.	High
	BUSY		Not ready for octet	Indicates that the TCAU is ready to receive a new octet in an ongoing segment.	High

*Table 1858.*Signal descriptions

Signal name	Field	Type	Function	Description	Active
AUCRI	BEGINS	Output	Data unit start	Pulses when a new segment is to be sent to the segmentation sub-layer.	High
	PROGRESSES		In progress	High throughout the segment transfer.	High
	COMPLETES		End of data	Pulses to indicate the successful completion of a segment transfer.	High
	ABORTS		Abort data unit	Pulses to indicate the erroneous completion of a segment transfer, i.e. either aborted from the transfer sublayer or from an unsuccessful authentication.	High
	REQUEST		Data valid strobe	Pulses to transmit a new octet from the TCAU to the segmentation sublayer.	High
	DATA		8-bit data	Segment data	-
AUCRO	ACCEPTING	Input	Ready for segment	Indicates that the segmentation sublayer is idle and can accept a new segment.	High
	BUSY		Not ready for octet	Indicates that the segmentation sublayer is ready to receive a new octet in an ongoing segment.	High
TCAUI	ENABLE	Input	Enable the TCAU	If set to '0', the TCAU will not perform any authentication, but will produce reports and forward segments to the segmentation sub-layer	High
	FIXEDKEY		Fixed key	Contains the weights and coefficients of the fixed key	-
	AUMAP		MAP selection for authentication	All segments where the 5 least significant bits of the segment header (the MAP address) are less than or equal to this input will be authenticated. All other segments (except control commands) will be forwarded to the segmentation sub-layer unaltered.	-
	RLAC_RSTVAL		Reset value for Recovery LAC	This value is read on the first clock cycle after reset is released and stored in the Recovery LAC as a start value.	-

*Table 1858.*Signal descriptions

Signal name	Field	Type	Function	Description	Active
TCAUO	AUANAVALID	Output	Analysis valid	Pulses whenever the AUANA and LASTMAP are updated with a new report. This is done when the TCAU has completed authentication or determined that a segment isn't to be authenticated.	High
	AUANA		Authentication analysis	Holds the TCAU report for the current segment when AUANAVALID is high.	-
	LASTMAP		Last addressed MAP	Holds the MAP ID of the current segment when AUANAVALID is high.	-
	PLAC		Principal LAC	Holds the 30-bit counter value of the Principal LAC.	-
	ALAC		Auxiliary LAC	Holds the 30-bit counter value of the Auxiliary LAC.	-
	RLAC		Recovery LAC	Holds the 8-bit counter value of the Recovery LAC.	-
	RLACWR		Recovery LAC write	Pulses when RLAC is updated.	High
	KEYINUSE		Currently selected key	0: fixed key is selected 1: programmable key is selected	-

124.18 Library dependencies

Table 1859 shows libraries used when instantiating the core (VHDL libraries).

*Table 1859.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	STDLIB	All	Common VHDL functions
TMTC	TMTC_TYPES	All	Signals and component declaration
TECHMAP	GENCOMP	All	Memory components

124.19 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib, techmap;
use grlib.stdlib.all;
use grlib.config.all;
use techmap.gencomp.all;

library tmtc;
use tmtc.tmtc_types.all;

entity authentication_example is
  generic (
    memtech : integer := CFG_MEMTECH
    ft      : integer range 0 to 1 := 1);
  port (
    clk   : in  std_logic;
    rst_n : in  std_logic;
    tlcri : in  oci_request_type;
```

```
    tlcro : out oci_response_type;
    aucri : out oci_request_type;
    aucro : in  oci_response_type;
    tcaui : in  tcau_in_type;
    tcauo : out tcau_out_type);
end entity authentication_example;

architecture rtl of authentication_example is
  constant tcau_syncrst_c : integer := 1 - grlib_config_array_type.grlib_async_reset_enable;

  tcau0: tcau
    generic map (
      syncrst => tcau_syncrst_c,
      tech    => memtech,
      ft      => ft)
    port map (
      clk    => clk,
      arst_n => '1',
      rst_n  => rst_n,
      tlcri  => tlcri,
      tlcro  => tlcro,
      aucro  => aucro,
      aucri  => aucri,
      tcaui  => tcaui,
      tcauo  => tcauo);
end architecture rtl;
```

125 GRTC_HW - CCSDS/ECSS Telecommand Decoder - Hardware Commands

125.1 Overview

125.1.1 Concept

The Telecommand Decoder - Hardware Commands provides access to an output port via telecommands.

The decoder implements the following layers:

- Application Layer:
  - Hardware command decoding and execution
- Space Packet Protocol:
  - Packet Extraction
  - Path Recovery
- Data Link - Protocol Sub-Layer:
  - Virtual Channel Packet Extraction
  - Virtual Channel Reception:
    - Support for Command Link Control Word (CLCW)
  - Virtual Channel Demultiplexing
  - Master Channel Demultiplexing

  •All Frames Reception
- D ata Link - Synchronization and Channel Coding Sub-Layer:

  •Pseudo-Derandomization
  - BCH codeblock decoding
  - Start Sequence Search
- Physical Layer:
  - Non-Return-to-Zero Level/Mark de-modulation (NRZ-L/M)

The Channel Coding Sub-Layer and the Physical Layer are shared with the Telecommand Decoder and are therefore not repeated here.

125.2 Operation

In the Application Layer and the Data Link - Protocol Sub-Layer, the information octets from the Channel Coding Sub-Layer are decoded as follows.

125.2.1 All Frames Reception

The All Frames Reception function performs two procedures:

- Frame Delimiting and Fill Removal Procedure; and
- Frame Validation Check Procedure, in this order.

The Frame Delimiting and Fill Removal Procedure is used to reconstitute Transfer Frames from the data stream provided by the Channel Coding Sub-Layer and to remove any Fill Data transferred from the Channel Coding Sub-Layer. The Frame Length field is checked to correspond to a fixed value as listed below. The number of information octets is checked to be a fixed number 21.

The Fill Data is checked to match the 0x55 pattern, or the corresponding pseudo-randomized pattern when pseudo-derandomization is enabled (pin configurable). Note that it is assumed that the Fill Data is not pseudo-randomized at the transmitting end.

The Frame Validation Checks procedure performs the following checks:

- Version Number is checked to be 0
- Bypass Flag is checked to be 1
- Control Command Flag is checked to be 0
- Reserved Spare bits are checked to be 0
- Spacecraft Identifier is compared with a pin configurable input value
- Virtual Channel identifier is compared with a pin configurable input value
- Frame Length field is checked to be a fixed value of 0000010011_b (i.e. 20-1)
- Frame Sequence Number is checked to be a fixed value of 0
- The Frame Error Control Field is checked to match the recomputed CRC value

125.2.2 Master Channel Demultiplexing

The Master Channel Demultiplexing is performed implicitly during the All Frames Reception procedure described above.

125.2.3 Virtual Channel Demultiplexing

The Virtual Channel Demultiplexing is performed implicitly during the All Frames Reception procedure described above.

125.2.4 Virtual Channel Reception

The Virtual Channel Reception supports Command Link Control Word (CLCW) generation and transfer to the Telemetry Encoder, according to the following field description.

- Control Word Type field is 0
- CLCW Version Number field is 0
- Status Field is 0
- COP in Effect field is 1
- Virtual Channel Identification is taken from pin configurable input value
- Reserved Spare field is 0
- No RF Available Flag is 0, but is overwritten by the Telemetry Encoder
- No Bit Lock Flag is 0, but is overwritten by the Telemetry Encoder
- Lockout Flag is 1
- Wait Flag is 0
- Retransmit Flag is 0
- FARM-B Counter is taken from the to least significant bits of a reception counter
- Reserved Spare field is 0
- Report Value field is 0

125.2.5 Virtual Channel Packet Extraction

The Virtual Channel Packet Extraction function extracts the Space Packet from the Frame Data Unit on the Virtual Channel, received from the Virtual Channel Reception function.

No blocking of Space Packets is permitted.

The Packet Version Number is checked to be 000, before delivered to the next function, else the Space Packet is discarded.

125.2.6 Path Recovery

The Path Recovery function receives and demultiplexes Space Packets received from the underlying subnetwork. The Path Recovery function receives Space Packets from the underlying subnetwork and demultiplex, if necessary, the received Space Packets on the basis of the Path Identifier of each Space Packet.

The Path Identifier is derived directly from the Application Identifier (APID) of the Space Packet, which is checked to be 00000000000, else the Space Packet is discarded.

Since the application layer uses the Octet String Service, the received Space Packets are delivered to the user through the Packet Extraction function described hereafter.

125.2.7 Packet Extraction

The Packet Extraction function extracts service data units from Space Packets. The Packet Extraction function extracts Octet Strings by stripping the Packet Primary Header, and the Packet Error Control field.

The following checks are performed before the Octet Strings (i.e. User Data Field) is forwarded to the Application Layer, else it is discarded:

- Packet Version field is 000_b
- Packet Type is 1_b
- Secondary Header Flagis 0_b
- Application Process identifer is compared with a pin configurable input value
- Sequence Flagsare 11_b
- Packet Data Length is 0000000000000110_b

The Packet Extraction Function does not check the continuity of the Packet Sequence Count, since Packet Name is used.

The Packet Extraction function verifies the correctness of the Packet Error Control field to match the recomputed CRC value (calculated over the complete Space Packet), if incorrect the Space Packet is not forwarded to the Application Layer, being discarded.

125.2.8 Application Layer

The Application Layer interprets only Transfer Frames that have successfully passed the Data Link Layer and Space Packet Protocol checks as described above.

The Application Layer interprets the Octet Strings (i.e. User Data Field) of the Packet Data Field.

The User Data Field consists of 5 octets comprising the hardware command, as defined in the bit order hereafter (MSB of first octet corresponds to OUTPUT(0), LSB of last octet corresponds to PULSE(7):

- OUTPUT(0 to 31) (32 bits in total)
- PULSE(0 to 7) (8 bits in total)

Before a hardware command is executed, the following is checked that:

- no hardware command is ongoing

The OUTPUT bits 0 to 31 correspond to the tcgpio[] bits 0 to 31.

The PULSE field has three interpretations: 0 to clear bits, 255 to set bits, 1 to 254 to generate pulses on bits:

- When PULSE field is 0, the corresponding bits that are not set in the OUTPUT field are cleared on the tcgpio outputs (AND function).
- When PULSE field is 255, the corresponding bits that are set in the OUTPUT field are set on the tcgpio outputs (OR function).
- When PULSE field is in the range 1 to 254, the corresponding bits that are set in the OUTPUT field are set on the tcgpio outputs for a duration of PULSE * 8192 system clock cycles, after which they are cleared again.

The tcgpio[0:31] outputs are cleared to logical 0 at reset.

125.3 Telecommand Transfer Frame format - Hardware Commands

The telecommand Transfer Frame for Hardware Commands has the following structures.

Transfer Frame				
Transfer Frame Primary Header	Transfer Frame Data Field			Frame Error Control Field (FECF)
	Space Packet			
	Packet Primary Header	Packet Data Field		
		User Data Field	Packet Error Control	
		Hardware Command		
0:39	40:87	88:127	128:143	144:159
5 octets	6 octets	5 octets	2 octets	2 octets
20 octets				

*Table 1860.*Telecommand Transfer Frame format

Transfer Frame Primary Header							
Version	Bypass Flag	Control Command Flag	Reserved Spare	S/C Id	Virtual Channel Id	Frame Length	Frame Sequence Number
00_b	1_b	0_b	00_b	PIN	PIN	0000010011_b	00000000_b
0:1	2	3	4:5	6:15	16:21	22:31	32:39
2 bits	1 bit	1 bit	2 bits	10 bits	6 bits	10 bits	8 bits
2 octets					2 octets		1 octet

*Table 1861.*Telecommand Transfer Frame Primary Header format

Space Packet								
Packet Primary Header							Packet Data Field	
Packet Version Number	Packet Identification			Packet Sequence Control		Packet Data Length	User Data Field	Packet Error Control
	Type	Secondary Header Flag	Application Process Id	Sequence Flags	Packet Name			
000_b	1_b	0_b	PIN	11_b	Don't care	0006_{16}	Hardware Command	CRC
40:42	43	44	45:55	56:57	58:71	72:87	88:127	128:143
3 bits	1 bit	1 bit	11 bits	2 bits	14 bits	16 bits	40 bits	16 bits
6 octets							5 octets	2 octets

*Table 1862.*CCSDS Space Packet format

Hardware Command	
OUTPUT (0:31)	PULSE (0:7)
88:119	120:127
32 bits	8 bits
4 octets	1 octet

*Table 1863.*Hardware Command format

125.4 Registers

The core has not user accessible registers.

125.5 Vendor and device identifiers

The core has has neither a vendor identifier nor a device identifier.

125.6 Configuration options

The core has no configuration options.

125.7 Signal descriptions

Table 1864 shows the interface signals of the core (VHDL ports).

*Table 1864.*Signal descriptions

Signal name	Field	Type	Function	Description	Active
RSTN	N/A	Input	Reset		Low
CLK	N/A	Input	Clock		-
TCI	SCID	Input	Spacecraft Identity	0 is MSB, 9 is LSB	-
	PSEUDO		Pseudo-Derando-miser	1=enabled, 0=disabled	-
	RFAVAILPOS		RF Available polarity	Active high=1 / low=0, used for CLCW	-
	BITLOCKPOS		Bit Lock polarity	Active high=1 / low=0, used for CLCW	-
	CLCWRFAVAIL-ABLE		RF Available	Used for CLCW	-
	CLCWBITLOCK		Bit Lock	Used for CLCW	-
TCO	CL_*	Input	Coding Layer	Coding Layer interface	-
TCVCID	N/A	Input	Virutal Channel Identifier		-
TCAPID	N/A	Input	Application Identifier		-
TCGPIO	N/A	Output	Hardware command		-
CLCW-DATA	N/A	Output	CLCW parallel data		-
CLCWEV-ENT	N/A	Output	CLCW changed		High

125.8 Signal definitions and reset values

The signals and their reset values are described in table 1865.

*Table 1865.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
tcgpio[0:31]	Output	Hardware command output	Logical 1	Logical 0

125.9 Timing

The timing waveforms and timing parameters are shown in figure 316 and are defined in table 1866.

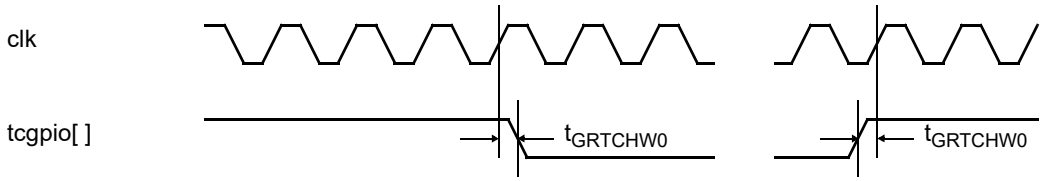


Figure 316. Timing waveforms

*Table 1866.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{GRTCHW0}$	clock to output delay	rising *clk* edge	TBD	TBD	ns

Note: The inputs are re-synchronized internally. The signals do not have to meet any setup or hold requirements. Static signals should not change between resets.

125.10 Library dependencies

Table 1867 shows libraries used when instantiating the core (VHDL libraries).

*Table 1867.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	StdLib	Functions	Operators
TMTC	TMTC_Types	Signals, component	Signals and component declaration

126 GRTC_UART - CCSDS/ECSS Telecommand Decoder - UART

126.1 Overview

A UART is used for the transmission of the CLTU from the telecommand decoder to the suer. The protocol has a fixed to baud rate, 1 star bit, 8 data bits, optional odd parity, 1 or 2 stop bits, with a BREAK command for message delimiting (sending 13 bits of logical zero).

The output contains the corrected information octets, which comprises the Telecommand Transfer Frame and any filler data octets. This is followed by the transmission of a BREAK command.

Note: The Telecommand Decoder Coding Layer does not inspect the contents of the corrected information octets. All corrected information octets are output on the UART interface.

126.2 Asynchronous bit serial data format

The asynchronous bit serial interface complies to the data format defined in [EIA 232]. It also complies to the data format and waveform shown in table 1868 and figure 317. The interface is independent of the transmitted data contents. Positive logic is considered for the data bits. The number of stop bits can optionally be either one or two. The parity bit can be optionally included.

Asynchronous bit serial format	start	D0	D1	D2	D3	D4	D5	D6	D7	parity	stop	stop
	first	*lsb*							*msb*			*last*
General data format $i = \{0, n\}$		8*i+7	8*i+6	8*i+5	8*i+4	8*i+3	8*i+2	8*i+1	8*i			
		last							*first*			

Table 1868. Asynchronous bit serial data format

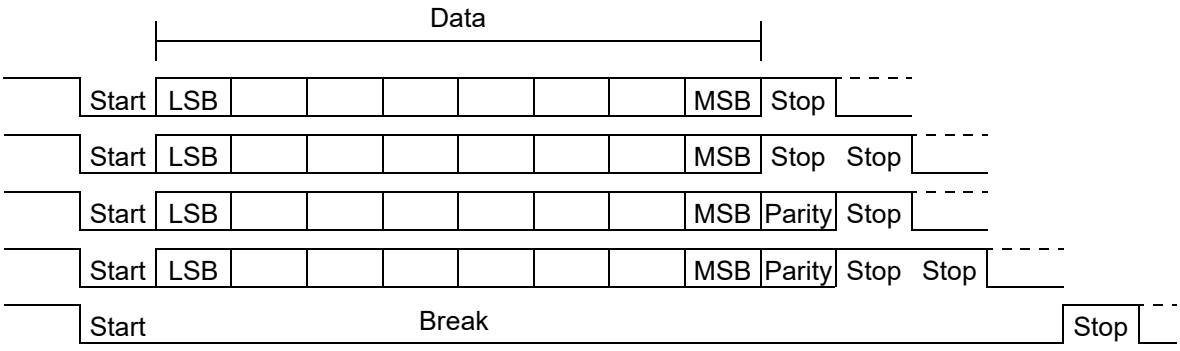


Figure 317. Asynchronous bit serial protocol / waveform

126.3 Registers

The core has not user accessible registers.

126.4 Vendor and device identifiers

The core has has neither a vendor identifier nor a device identifier.

126.5 Configuration options

Table 1869 shows the configuration options of the core (VHDL generics).

*Table 1869.*Configuration options

Generic	Function	Description	Allowed range	Default
gSystemClock	System frequency	[Hz]	Integer	33333333
gBaud	Baud rate	[Baud]	Integer	115200
syncreset	Sync reset	Synchronous reset when 1	0 - 1	0

126.6 Signal descriptions

Table 1870 shows the interface signals of the core (VHDL ports).

*Table 1870.*Signal descriptions

Signal name	Field	Type	Function	Description	Active
RSTN	N/A	Input	Reset		Low
CLK	N/A	Input	Clock		-
ODDPARITY	N/A	Input		Generate odd parity, else none	High
TWOSTOPBITS	N/A	Input		Generate two stop bits, else one	High
TCO	CL_*	Input	Coding Layer	Coding Layer interface	-
TCUART	N/A	Output		Telecommad UART output	-

126.7 Signal definitions and reset values

The signals and their reset values are described in table 1871.

*Table 1871.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
tcuart	Output	CLTU UART output	-	Logical 1

126.8 Timing

The timing waveforms and timing parameters are shown in figure 318 and are defined in table 1872.

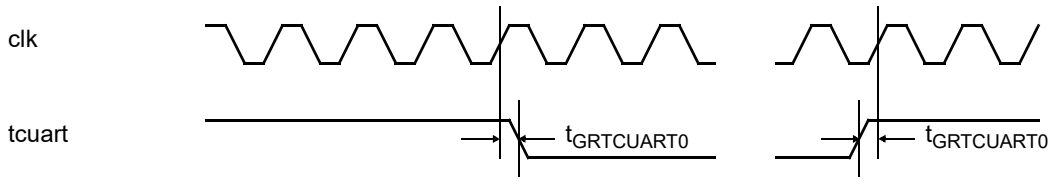


Figure 318. Timing waveforms

*Table 1872.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{GRTCUART0}$	clock to output delay	rising *clk* edge	TBD	TBD	ns

Note: The inputs are re-synchronized internally. The signals do not have to meet any setup or hold requirements. Static signals should not change between resets.

126.9 Library dependencies

Table 1873 shows libraries used when instantiating the core (VHDL libraries).

*Table 1873.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	StdLib	Functions	Operators
TMTC	TMTC_Types	Signals, component	Signals and component declaration

127 GRTCTX - CCSDS/ECSS Telecommand Transmitter

127.1 Overview

The CCSDS/ECSS/PSS Telecommand Transmitter implements part of the Data Link Layer, covering the Protocol Sub-layer and the Frame Synchronization and Coding Sub-layer and part of the Physical Layer of the packet telecommand protocol.

The operation of the Telecommand Transmitter is highly programmable by means of control registers.

The Telecommand Transmitter comprises several encoders and modulators implementing the Consultative Committee for Space Data Systems (CCSDS) recommendations, European Cooperation on Space Standardization (ECSS) and the European Space Agency (ESA) Procedures, Standards and Specifications (PSS) for telecommand and channel coding. The Telecommand Transmitter comprises the following:

- Frame Error Control Field (FECF)
- Pseudo-Randomiser (PSR) / Bit Transition Generator (BTG)
- Communications Link Transmission Unit (CLTU)
  - Start Sequence insertion
  - Bose-Chaudhuri-Hocquenghem (BCH)
  - Tail Sequence insertion
- Physical Layer Operations Procedures (PLOP-1, PLOP-2)
- Non-Return-to-Zero Mark/Level (NRZ)

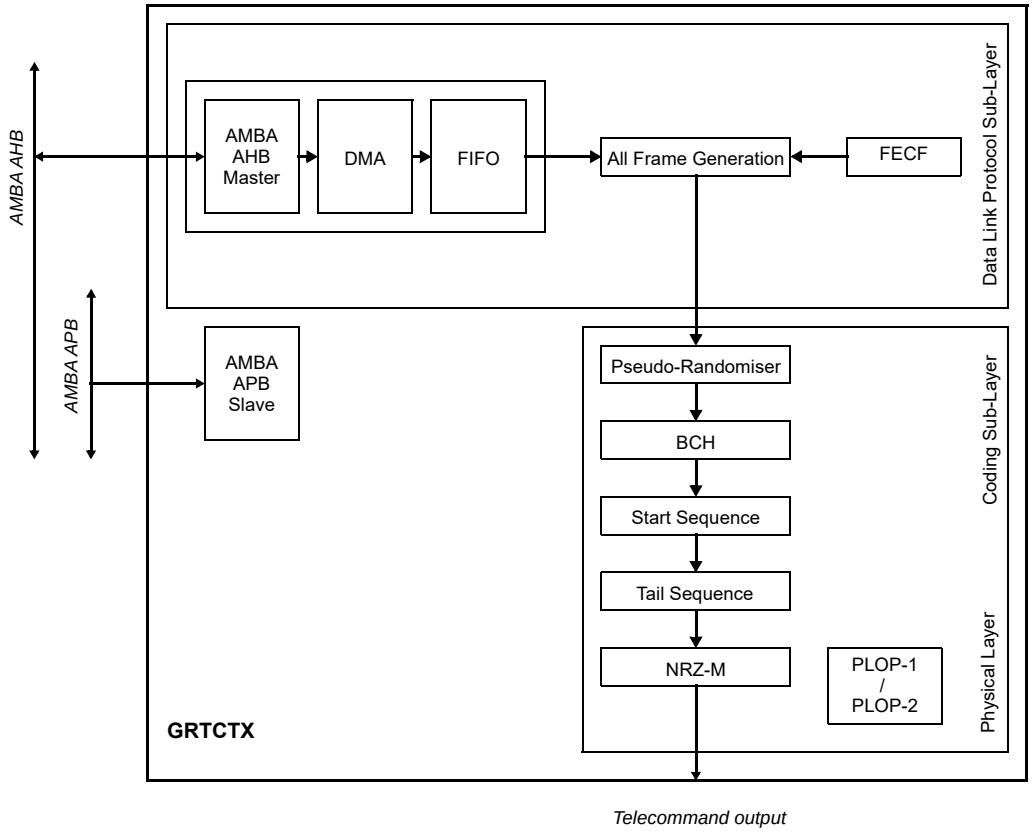


Figure 319. Block diagram

127.2 References

127.2.1 Documents

[C231] CCSDS 231.0-B-2 TC Synchronization and Channel Coding

[C232] CCSDS 232.0-B-2 TC Space Data Link Protocol

[ECSS04] ECSS-E-50-04C: Space engineering - Space data links - Telecommand protocols, synchronization and channel coding

[ECSS05] ECSS-E-50-05C: Space engineering - Radio frequency and modulation

[PPS107] PSS-04-107: Packet telecommand standard

[PPS105] PSS-04-105 Radio frequency and modulation standard

127.2.2 Acronyms and abbreviations

BTG Bit Transition Generator

CCSDS Consultative Committee for Space Data Systems

CLCW Command Link Control Word

CLTU Communications Link Transmission Unit

CMM Carrier Modulation Mode

CRC Cyclic Redundancy Code

DMA Direct Memory Access

ECSS European Cooperation for Space Standardization

ESA European Space Agency

FECF Frame Error Control Field

MSB Most Significant Bit

NRZ Non Return to Zero

OCF Operational Control Field

PLOP Physical Layer Operations Procedure

PSR Pseudo Randomiser

PSS Procedures, Standards and Specifications

TC Telecommand -- BCH Bose-Chaudhuri-Hocquenghem

127.3 Layers

127.3.1 Introduction

The relationship between Packet Telecommand (or simply Telecommand or TC) standard and the Open Systems Interconnection (OSI) reference model is such that the OSI Data Link Layer corresponds to two separate layer, namely the Data Link Protocol Sub-layer and Synchronization and Channel Coding Sub-Layer. The OSI Data Link Layer is covered here.

The OSI Physical Layer is also covered here to some extended, as specified in [ECSS04] and [PPS107]. The OSI Network Layer or higher layers are not covered here.

127.3.2 Data Link Protocol Sub-layer

The following functionality is implemented in the core:

- All Frame Generation:

•Frame Error Control Field (FECF) calculation and insertion

127.3.3 Synchronization and Channel Coding Sub-Layer

The following functionality is implemented in the core:

- Pseudo-Randomiser (PSR) / Bit Transition Generator (BTG)
- Communications Link Transmission Unit (CLTU)
  - Start Sequence insertion
  - Bose-Chaudhuri-Hocquenghem (BCH)
  - Tail Sequence insertion

127.3.4 Physical Layer

The following functionality is implemented in the core:

- Physical Layer Operations Procedures (PLOP-1, PLOP-2)
- Non-Return-to-Zero (NRZ) modulation

127.4 Operation

127.4.1 Introduction

The DMA interface provides a means for the user to send blocks of data of arbitrary length, normally this is Communications Link Transmission Units (CLTU).

127.4.2 Descriptor setup

The DMA interface is used for sending data on the uplink. The transmission is done using descriptors located in memory. A single descriptor is shown in tables 1874 through 1877. The address field of the descriptor should point to the start of the data to be sent. The address need not be word-aligned. If the interrupt enable (IE) bit is set, an interrupt will be generated when the transfer has completed (this requires that the interrupt enable bit in the control register is also set). The interrupt will be generated regardless of whether the transfer was successful or not. The wrap (WR) bit is also a control bit that should be set before transmission and it will be explained later in this section.

*Table 1874.*GRTCTX descriptor word 0 (address offset 0x0)

31 16	15 8	7	6 4	3	2	1	0
LEN	RESERVED	UR	SEL	-	WR	IE	EN

31: 16	(LEN) - Length in bytes (note that maxium length is limited to 2048 bytes, and minimum to 2 bytes)
15: 8	RESERVED
7:	Underrun (UR) - Underrun detected during transmission.
6: 4	Select output (SEL) - Select output for bit clock, bit lock and bit data (0 to 7)
3:	RESERVED
2:	Wrap (WR) - Set to one to make the descriptor pointer wrap to zero after this descriptor has been used. If this bit is not set the pointer will increment by 16. The pointer automatically wraps to zero when the 16 kB boundary of the descriptor table is reached.
1:	Interrupt Enable (IE) - an interrupt will be generated when the data for this descriptor has been sent provided that the transmitter interrupt enable bit in the control register is set. The interrupt is generated regardless if it was transferred successfully or if it terminated with an error.
0:	Enable (EN) - Set to one to enable the descriptor. Should always be set last of all the descriptor fields.

*Table 1875.*GRTCTX descriptor word 1 (address offset 0x4)

31	0
ADDRESS	

31: 0 Address (ADDRESS) - Pointer to the buffer area to where data will be fetched.

*Table 1876.*GRTCTX descriptor word 2 (address offset 0x8)

31	0
STATUS0	

31: 0 (STATUS0) - External status information

*Table 1877.*GRTCTX descriptor word 3 (address offset 0xC)

31	0
STATUS1	

31: 0 (STATUS1) - External status information

To enable a descriptor the enable (EN) bit should be set and after this is done, the descriptor should not be touched until the enable bit has been cleared by the core.

127.4.3 Starting transmission

Enabling a descriptor is not enough to start transmission. A pointer to the memory area holding the descriptors must first be set in the core. This is done in the descriptor pointer register. The address must be aligned to a 16 kByte boundary. Bits 31 to 14 hold the base address of descriptor area while bits 13 to 4 form a pointer to an individual descriptor. The first descriptor should be located at the base address and when it has been used by the core, the pointer field is incremented by 16 to point at the next descriptor. The pointer will automatically wrap back to zero when the next 16 kByte boundary has been reached. The WR bit in the descriptors can be set to make the pointer wrap back to zero before the 16 kByte boundary.

The pointer field has also been made writable for maximum flexibility but care should be taken when writing to the descriptor pointer register. It should never be touched when transmission is active.

The final step to activate the transmission is to set the enable bit in the DMA control register. This tells the core that there are more active descriptors in the descriptor table. This bit should always be set when new descriptors are enabled, even if transmission is already active. The descriptors must always be enabled before the transmission enable bit is set.

127.4.4 Descriptor handling after transmission

When the transmission has finished, status is written to the first word in the corresponding descriptor. The other bits in the first descriptor word are set to zero after transmission while the second word is left untouched. The enable bit should be used as the indicator when a descriptor can be used again, which is when it has been cleared by the core. Additionally, the last two words in the corresponding descriptor are written with external status information.

There are multiple bits in the DMA status register that hold status information.

The Transmitter Interrupt (TI) bit is set each time a DMA transmission ended successfully. The Transmitter Error (TE) bit is set each time an DMA transmission ended with an error. For either event, an interrupt is generated for descriptor for which the Interrupt Enable (IE) was set. The interrupt is maskable with the Interrupt Enable (IE) bit in the control register.

The Transmitter AMBA error (TA) bit is set when an AMBA AHB error was encountered either when reading a descriptor or when writing data. Any active transmission was aborted and the DMA channel was disabled. It is recommended that the Telecommand Transmitter is reset after an AMBA AHB error. The interrupt is maskable with the Interrupt Enable (IE) bit in the control register.

127.5 Registers

The core is programmed through registers mapped into APB address space.

*Table 1878.*GRTCTX registers

APB address offset	Register
0x00	GRTCTX DMA Control register
0x04	GRTCTX DMA Status register
0x08	GRTCTX DMA Descriptor Pointer register
0x80	GRTCTX Control register
0x88	GRTCTX Configuration register
0x90	GRTCTX Physical Layer register
0x94	GRTCTX Coding Sub-Layer register
0x98	GRTCTX Start and Tail register
0x9C	GRTCTX All Frames register

127.5.1 GRTCTXDMA Control Register

*Table 1879.*0x00 -DCR - DMA control register

31 2	1	0
RESERVED	IE	EN
0	0	0
r	rw	rw

31: 2 RESERVED

1: Interrupt Enable (IE) - enable interrupts TA, TI, and TE

0: Enable (EN) - enable DMA transfers

127.5.2 GRTCTX DMA Status Register

*Table 1880.*0x04 - DSR - DMA status register

31 4	3	2	1	0
RESERVED	ACTIVE	TA	TI	TE
0	NR	0	0	0
r	r	wc	wc	wc

31: 4 RESERVED

3: Active (ACTIVE) - DMA access ongoing

2: Transmitter AMBA Error (TA) - DMA AMBA AHB error, cleared by writing a logical 1

1: Transmitter Interrupt (TI) - DMA interrupt, cleared by writing a logical 1

0: Transmitter Error (TE) - DMA transmitter error, cleared by writing a logical 1

127.5.3 GRTCTXDMA Descriptor Pointer Register

Table 1881. 0x08 - DDP - DMA descriptor pointer register

31 14	13 4	3 0
BASE	INDEX	RESERVED
NR	NR	0
rw	rw	r

31: 14 Descriptor base (BASE) - base address of descriptor table

13: 4 Descriptor index (INDEX) - index of active descriptor in descriptor table

3: 0 Reserved - fixed to “0000”

127.5.4 GRTCTX Control Register

Table 1882. 0x80 - CTRL - control register

31 3	2	1	0
RESERVED	RST	R	TxEN
0	0	0	0
r	rw	r	rw

31: 3 RESERVED

2: Reset (RST) - resets complete core

1: RESERVED

0: Transmitter Enable (TxEN) - enables Telecommand Transmitter (should be done after the complete configuration of the Telecommand Transmitter)

127.5.5 GRTCTX Configuration Register

Table 1883. 0x88 - CONF - configuration register

31 24	23 8	7 0
REVISION	FIFOSIZE	RESERVED
*	*	0
r	r	r

31: 24 (REVISION) - Revision number

23: 8 (FIFOSIZE) - FIFO size in bytes

7: 0 RESERVED

127.5.6 GRTCTX Physical Layer Register

Table 1884. 0x90 - PLR - physical layer register

31 20	19 16	15 11	10	9	8	7	6	5	4	3 2	1	0
DIVIDE	UNMODU-LATED	RESERVED	IDLE ALL	IDLE PRE	IDLE POST	RF AVAIL	RF POS	BIT POS	CLK RISE	CLK MODE	PLOP	NRZM
1	0	0	0	0	0	0	1	1	1	0b01	0	0
rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

31: 20 (DIVIDE) - Clock divider (value 0 not used)

19: 16 (UNMODULATE) - Number of unmodulated octet counts (CMM-1)

15: 11 RESERVED

10: (IDLEALL) - Idle Sequence when unmodulate (CMM-1) or non-active, else all-zero output

9: (IDLEPRE) - Optional Idle Sequence before CLTU (CMM-4)

8: (IDLEPOST) - Optional Idle Sequence after CLTU (CMM-4)

7: (RFAVAIL) - RF available when unmodulate (CMM-1) or non-active

6: (RFPOS) - Positive polarity for RF available output signal

5: (BITPOS) - Positive polarity for bit lock output signal

4: Rising clock edge (CLKRISE) - Rising clock edge coinciding with serial data bit change

3: 2 Clock mode (MODE) - 00 = never generated,
01 = only generated when modulated,
10 = also generated when unmodulated (CMM-1),
11 = always generated

1: Physical Layer Operations Procedure (PLOP) - PLOP-1 (when cleared) or PLOP-2 (when set)

0: Non-Return-to-Zero-Mark (MARK) - non-return-to-zero - mark encoding enable

127.5.7 GRTCTX Coding Sub-layer Register

Table 1885. 0x94 - CSL - coding sub-layer register

31 24	23 16	15 8	7	6 5	4	3	2	1	0
RESERVED	IDLE	FILLDATA	FILLER BIT	R	PSEUDO ALL	PSEUDO	BCH	START SEQ	TAIL SEQ
0	0x55	0x55	0	0	0	0	0	0	0
r	rw	rw	rw	r	rw	rw	rw	rw	rw

31: 24 RESERVED
23: 16 (IDLE) - Idle/Acquisition Sequence (reset 0x55)
15: 8 (FILLDATA) - Fill Data for BCH coding (reset 0x55)
7: (FILLERBIT) - Filler Bit for BCH coding (reset 0)
6: 5 RESERVED
4: (PSEUDOALL) - Pseudo-Randomize BCH fill data (only with BCH and PSEUDO)
3: (PSEUDO) - Pseudo-Randomize (only with BCH)
2: (BCH) - BCH encoding
1: (STARTSEQ) - Start Sequence Generation
0: (TAILSEQ) - Tail Sequence Generation

127.5.8 GRTCTX Start And Tail Register

Table 1886. 0x98 - STR - start and tail register

31 16	15 8	7 0
START	TAIL	TAILLAST
0xEB90	0xC5	0x79
rw	rw	rw

31: 16 (START) - Start Sequence value (reset 0xEB90)
15: 8 (TAIL) - Tail Sequence value (reset 0xC5) (applies to first 7 octets:)
7: 0 (TAILLAST) - Tail Sequence, last (reset 0x79) (applies to the last octet only):

127.5.9 GRTCTX All Frames Register

Table 1887. 0x9C - AFR - all frames register

31 26	25 16	15 2	1	0
RESERVED	SCID	RESERVED	PSS	FECF
0	0	0	0	0
r	rw	r	rw	rw

31: 26 RESERVED
25: 16 (SCID) - Spacecraft Identifier (unsed)
15: 2 RESERVED
1: (PSS) - ESA PSS compatible mode (unsed)
0: (FECF) - Insert CRC/FECF, overwriting the two last octets of a transfer frame (only with BCH)

127.6 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x082. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

127.7 Configuration options

Table 1888 shows the configuration options of the core (VHDL generics).

*Table 1888.*Configuration options

Generic name	Function	Allowed range	Default
hindex	AHB master index	0 - NAHBMST-1	0
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	ADDR field of the APB BAR	0 - 16#FFF#	0
pmask	MASK field of the APB BAR	0 - 16#FFF#	16#FFF#
pirq	Interrupt line used by core	0 - NAHBIRQ-1	0
memtech	Memory technology	0 to NTECH	0
clktech	Clock buffer technology	0 to NTECH	0
buftype	Clock buffer type	TBD	0

127.8 Signal descriptions

Table 1889 shows the interface signals of the core (VHDL ports).

*Table 1889.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
TCI	TCACTIVE[]	Output	Bit Lock	-
	TCCLK[]		Bit clock	-
	TCDATA[]		Bit data	-
	CLCW-RFAVAILABLE[]		RF Available	-
	CLCW-BITLOCK[]		Bit Lock	-
TMO	TIMESTAMP	Input	Time Stamp	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
AHBMI	*	Input	AMB master input signals	-
AHBMO	*	Output	AHB master output signals	-

* see GRLIB IP Library User's Manual

127.9 Signal definitions and reset values

The signals and their reset values are described in table 1890.

*Table 1890.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
tcactive[]	Output	Bit lock	-	-
tcdata[]	Output	Serial bit data	-	-
tcclk[]	Output	Serial bit data clock	-	-
rfavailable[]	Output	RF available	-	-

127.10 Timing

The timing waveforms and timing parameters are shown in figure 320 and are defined in table 1891.

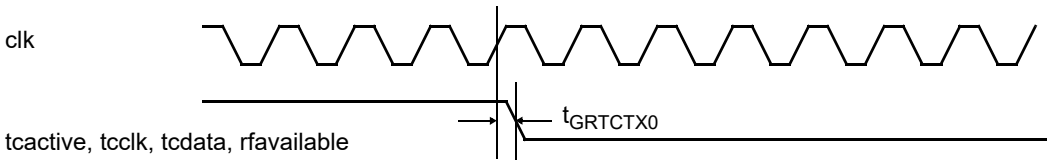


Figure 320. Timing waveforms

*Table 1891.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{GRTCTX0}$	clock to output	rising *clock* edge	TBD	TBD	ns

127.11 Library dependencies

Table 1892 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1892.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
TMTC	TMTC_TYPES	Signals, component	Component declaration

128 GRCTM - CCSDS Time Manager

128.1 Overview

The CCSDS Time Manager (GRCTM) provides basic time keeping functions such an Elapsed Time (ET) counter according to the Consultative Committee for Space Data Systems (CCSDS) Unsegmented Code specification, [CCSDS]. It comprises a Frequency Synthesizer (FS) by which a binary frequency is generated to drive the ET counter. The GRCTM provides support for setting the increment rate of the ET counter as well as of the FS counter.

The GRCTM provides datation services that sample the ET counter value on external events. It also provides generation of periodic pulses with cycle periods of less than one second. All services in the GRCTM core are accessible via an AMBA AHB slave interface.

The GRCTM provides a service for sampling the ET counter value on the occurrence of the time strobe generated by for example the Packet Telemetry Encoder (PTME), generating a Standard Spacecraft Time Source Packet according to the ESA Packet Telemetry Standard, [PSS]. The Time Source Packet can be read out via the AMBA AHB slave interface and is transmitted directly to a telemetry encoder via a serial interface.

The GRCTM can act as a master and/or a slave in a time distribution system. As a master only, the GRCTM distributes the ET to GRCTM slaves via a TimeWire (TW) interface. As a slave only, the GRCTM receives the ET via the TimeWire interface. When acting as a master and slave, the GRCTM receives the ET from a master GRCTM, but can also distribute the ET to other slaves.

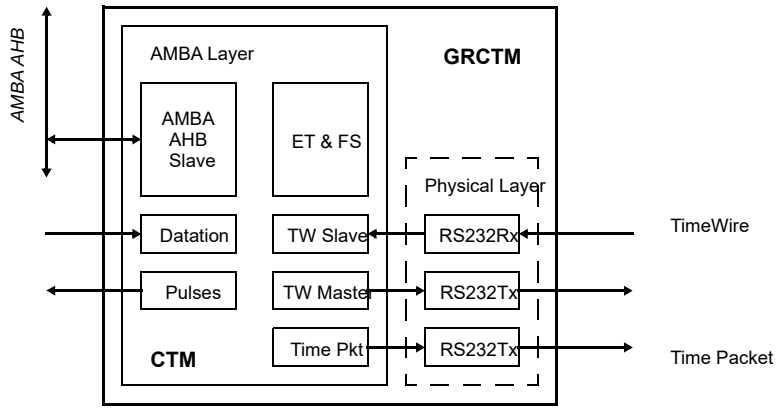


Figure 321. Block diagram

128.1.1 Foreseen usage of the core

On-board time maintenance and distribution is to be handled through a master CCSDS Time Manager (GRCTM) and one or more slave GRCTMs. Using a dedicated synchronisation line (TimeWire), the slave time manager can be synchronised with the master GRCTM. The slave GRCTM can further distribute the time to the payload. The GRCTM slaves will thus be slaved to the master GRCTM, but also act as masters for other modules. This isolates the master GRCTM from the payloads. The slave GRCTM provides four datation register into which the Elapsed Time (ET) counter can be latched on the occurrence of an external triggering event.

It is not possible to synchronise or set the ET counter in the master GRCTM. The ET counter can only be cleared by means of hardware or software reset.

128.1.2 Description of a general system using the core

The general approach to accurately maintaining on-board time is to have a central time reference measuring the elapsed time from an arbitrary epoch and to distribute regularly this time information to on-board applications by means of messages and synchronisation pulses. Another approach would be to have a centralised time system, where each application that needs to time stamp data could request the unit maintaining the central time reference to provide the relevant time information. Such an approach would have several inherent drawbacks, e.g. in systems with many users, the accuracy of a time stamp could be jeopardised due to long service latency and excessive bus traffic could degrade the overall performance of the data handling system.

The purpose of the GRCTM is to provide a building block for such time distribution services by providing the means for CCSDS compliant time keeping and a set of basic user time services. Most time distribution implementations have required support from the application processor to maintain synchronisation between the central and the local time references. Protocols and formats for distributing time information have differed between spacecraft and have sometimes only provided low resolution or poor accuracy. The purpose of the GRCTM is to provide an accurate time coherence throughout the spacecraft.

The correlation between the central time reference and ground has already been foreseen by providing a time strobe from the Packet Telemetry encoder. The time strobe has a deterministic relationship to the bit structure of the telemetry frame. This makes it possible to establish the time relation between the assertion of this time strobe on-board and the reception of the relevant frame on ground, taking into account the down link propagation delay. Each GRCTM instance maintains its own copy of the central elapsed time reference with which on-board applications can time stamp their data. This unbroken chain of time relationships on-board, and between the spacecraft and ground, provides a solution to the problem of knowing when an event took place on-board in any given space-time frame.

The GRCTM is foreseen to be used both as a central elapsed time reference in the spacecraft data management system, as well as the local elapsed time reference in an instrument or other subsystem. By using standardised AMBA interfaces, the integration of the GRCTM should be simple for most systems.

128.1.3 Functions not included

The GRCTM does not support alarm services.

The GRCTM does not support setting of an arbitrary epoch time.

128.2 Data formats

All Elapsed Time (ET) information handled by GRCTM is compliant with the CCSDS Unsegmented Code defined in [CCSDS] and repeated hereafter.

128.2.1 Reference documents

[CCSDS] Time Code Formats, CCSDS 301.0-B-4, www.ccsds.org

[PSS] Packet Telemetry Standard, ESA PSS-04-106, Issue 1, January 1988

128.2.2 CCSDS Unsegmented Code: Preamble Field (P-Field)

The time code preamble field (P-Field) may be either explicitly or implicitly conveyed. If it is implicitly conveyed (not present with T-Field), the code is not self-identified, and identification must be

obtained by other means. As presently defined, the explicit representation of the P-Field is limited to one octet whose format is described hereafter.

*Table 1893.*CCSDS Unsegmented Code P-Field definition

Bit	Value		Interpretation
0	0		Extension flag
1 - 3	“001”	1958 January 1 epoch (Level 1) [1]	Time code identification
	“010”	Agency-defined epoch (Level 2) [1]	
4 - 5	(number of octets of coarse time) - 1		Detail bits for information on the code
6 - 7	(number of octets of fine time)		

1 *For the Standard Spacecraft Time Source Packet defined in the ESA Packet Telemetry Standard, bits 1 to 3 must are set to* 010_b.

128.2.3 CCSDS Unsegmented Code: Time Field (T-Field)

For the unsegmented binary time codes described herein, the T-Field consists of a selected number of contiguous time elements, each element being one octet in length. An element represents the state of 8 consecutive bits of a binary counter, cascaded with the adjacent counters, which rolls over at a modulo of 256.

*Table 1894.*CCSDS Unsegmented Code T-Field definition

CCSDS Unsegmented Code												
Preamble Field	Time Field											
	Coarse time								Fine time			
-	2^{31}	2^{24}	2^{23}	2^{16}	2^{15}	2^{8}	2^{7}	2^{0}	2^{-1}	2^{-8}	2^{-9}	2^{-15}	2^{-16}	2^{-24}

The basic time unit is the second. The T-Field consists of 32 bits of coarse time (seconds) and 24 bits of fine time (sub seconds). The coarse time code elements are a count of the number of seconds elapsed from the epoch. The 32 bits of coarse time results in a maximum ambiguity period of approximately 136 years. Arbitrary epochs may be accommodated as a Level 2 code. The 24 bits of fine code elements result in a resolution of 2-24 second (about 60 nanoseconds). This code is not UTC-based and leap second corrections do not apply according to CCSDS.

128.2.4 Waveforms

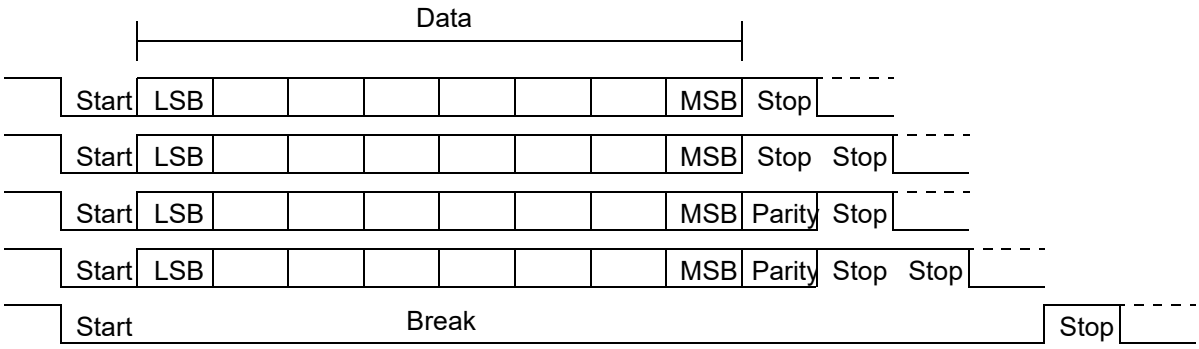


Figure 322. Bit asynchronous protocol

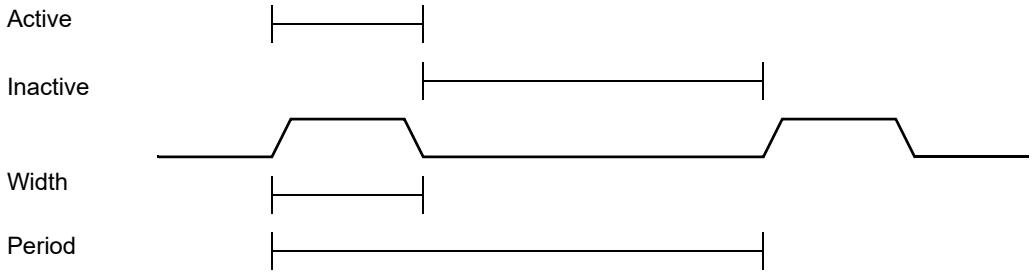


Figure 323. Pulse generation waveform

128.3 Operation

The CCSDS Time Manager (GRCTM) synthesizable core can be configured for various purposes. The different functions presented hereafter can be used to from a GRCTM to act as a master, slave, or master and slave.

128.3.1 Elapsed Time (ET)

The local Elapsed Time (ET) counter is based on a default 32 bit coarse time field and a 24 bit fine time field, complying to the CCSDS Unsegmented Code (CUC) T-Field. The width of the two time fields is fixed. The counter implementing the ET is incremented on the system clock only when enabled by the frequency synthesizer described below. The ET is incremented with a pre-calculated increment value, which matches the synthesised frequency. The local ET is output in the CUC format, P-Field and T-Field, to be used by an application embedding the GRCTM. The P-Field is static with the Time Code Identifier is set to 010b.

128.3.2 Frequency Synthesizer (FS)

The binary frequency required to determine the ET counter increment is derived from the system clock using a frequency synthesizer. The frequency synthesizer is incremented with a pre-calculated increment value, which matches the available system clock frequency. The FS simply generates a tick every time it wraps around, which makes the ET to step forward with the pre-calculated increment value. The output of the frequency synthesizer is used for enabling the increment of the local ET as described above. A 24 to 32 bit wide FS causes a systematic drift of less than 1 second/day.

128.3.3 TimeWire Interface (TW)

The GRCTM provides two TimeWire (TW) interfaces, one for the master function and one for the slave function. The TimeWire interface is used for distributing the Elapsed Time (ET) of a GRCTM master to one or more GRCTM slaves. The information carried in the synchronisation message comprises the Elapsed Time Field, which is 4 bytes, and a synchronisation pulse which is sent as a BREAK command. The synchronisation pulse is used for synchronising both the ET and the phase of the Frequency Synthesiser (FS) and is done once every second.

The GRCTM slave automatically synchronizes its ET with that of the GRCTM master without requiring any user support. A GRCTM that acts both as a master and a slave will be slaved to another master via a slave TimeWire interface, and will simultaneously distribute its own ET to other GRCTM slaves. The GRCTM slave will continue to work undisturbed in case a GRCTM master has failed. It is also possible to disable the synchronisation by means of a register further to avoid failure propagation. The TimeWire interface provides means for synchronising a GRCTM slave from a GRCTM that acts both as a master and a slave, which being synchronised in turn from another GRCTM master.

The message is sent just before the synchronisation instance. A BREAK command is sent just after the message to indicate the synchronisation pulse. The instance of the synchronisation actually depends on the reception of the BREAK command and the time it takes to generate an internal pulse

in the receiver on which the previously sent message is latched into the ET counter of the slave. The baseline is to send the synchronisation message and pulse to coincide with the wrap around of the sub-second bits in the ET. However, the time at which the message is sent out from the master is configurable by means of a generic (based on the fine part of the ET). An additional generic is provided for the fine tuning of the message start. On the slave side, a generic is provided to set the fine part of the ET at which the synchronisation pulse will occur. It is thus possible to synchronise the two units at any arbitrary point in time, provided it is done once a second.

To tolerate large skew and drift differences between the clocks driving the master and the slave GRCTM, a staged approach has been taken for the distribution of the synchronisation message and the synchronisation pulse. The first GRCTM master in a time chain synchronises its GRCTM slaves before it is time for these to act as masters and in turn send their synchronisation messages and pulses to their slaves. This is done to avoid that the first GRCTM master will synchronise the GRCTM slaves in such a way that no synchronisation messages are being sent out from these GRCTM due to clock drift. Since the synchronisation only occurs once a second, the first GRCTM master in a time chain has one second of time available to synchronise its GRCTM slaves before they synchronise their slaves in turn.

The TimeWire interface is based on a bit asynchronous interface (RS232/422) with the following programmable specification:

- 115200 baud (configured by generics/register bits)
- 1 start bit, 8 bit data, 1 or 2 stop bits (configured by generics/register bit)
- odd parity is generated in transmitter, but ignored in the receiver (configured by generics/register bit)
- no handshake
- message delimiting via BREAK command (13 bits when sent)
- synchronisation via BREAK command (13 bits when sent)

*Table 1895.*TimeWire transmission protocol

Byte Number	Elapsed Time Coarse Register (ETCR)	CCSDS Unsegmented Code Time Field Coarse Part	Comment
First	[31:24]	2^{31} 2^{24}	
Second	[23:16]	2^{23} 2^{16}	
Third	[15:8]	2^{15} 2^{8}	
Fourth	[7:0]	2^{7} 2^{0}	
Fifth	N/A	[RS232 Break Command]	Used as synchronisation pattern

Note that it is not possible for the TimeWire to carry sub-second phase information due to the usage of the above RS232/422 type of interface.

128.3.4 Datation

The GRCTM comprises three datation registers for the purpose of datation of user events relative the ET counter. The datation is triggered by three external edge sensitive inputs (programmable rising or falling edge).

A fourth datation register is provided for sampling the ET counter when generating a Standard Spacecraft Time Source Packet as described below.

Each of the three general datation services is automatically disabled after an occurrence and is not re-enabled until the corresponding fine time register is read. The format of all four datation registers is compliant to the CUC T-Field.

The ET counter can be accessed directly via the AMBA AHB interface. This can be used for direct datation from software.

128.3.5 Interrupts

The GRCTM provides individual interrupt lines for the incoming datation inputs, the time strobe input and the occurrence of the individual pulse outputs. The interrupt lines are asserted for at least two system clock cycles and can be connected to an external interrupt controller. The interrupts indicate that a new datation value can be read. The interrupts defined in table 1896 are generated.

*Table 1896.*Interrupts

Interrupt offset	Interrupt name	Description
1:st	DRL0	Datation Register 0 Latched
2:nd	DRL1	Datation Register 1 Latched
3:rd	DRL2	Datation Register 2 Latched
4:th	STL	Spacecraft Time Register Latched
5:th	PULSE0	Pulse 0 interrupt
6:th	PULSE1	Pulse 1 interrupt
7:th	PULSE2	Pulse 2 interrupt
8:th	PULSE3	Pulse 3 interrupt
9:th	PULSE4	Pulse 4 interrupt
10:th	PULSE5	Pulse 5 interrupt
11:th	PULSE6	Pulse 6 interrupt
12:th	PULSE7	Pulse 7 interrupt
13:th	ETSET	ET set (only when VHDL generic gSetET is 1)

128.3.6 Pulses

The GRCTM provides eight external outputs used for clock pulse distribution. The timing of each pulse output is individually derived from the Elapsed Time counter. It is possible to program for each pulse output individually the following parameters:

- periodicity pulse
- width of pulse
- polarity of pulse
- enable/disable pulse generation (reset status is disabled)

The pulse has two parts, the active and the inactive part. The active part always starts the pulse, followed by the inactive part. The polarity or logical level of the active part is programmable. The inactive part takes the logical inversion of the active pulse, and is the default output from the generator when the pulse is not issued or the overall generation is disabled. The leading edge of the active pulse part is aligned with the 1 second transition of the Elapsed Time counter.

The periodicity of the pulse corresponds to one of the ET bits that can be selected in the range 27 to 2-8 seconds, providing a range from 128 seconds to 3,91 ms, i.e. 0,0078 to 256 Hz frequency. See register definition for details.

The width of the active part of the pulse corresponds to one of the ET bits that can be selected in the range 26 to 2-9 seconds, providing a range from 64 seconds to 1,95 ms. See register definition for details.

It is possible to generate a pulse that has a duty cycle of 50%. It is also possible to generate a pulse for which the active part is as short as 2-9 seconds, and its period is as high as 27 seconds. The effective duty cycle can be as low as 2-9/27 for the longest period, up to 50% for the shortest period of 2-8 sec-

onds = 256 Hz. The duty cycle choice becomes more restricted as the frequency increases. Note that it is only possible to reduce the duty cycle in one direction: 50%/50%, 25%/75% ... 1%/99%. The active part of the pulse can thus never be more than 50% of the cycle. It should be noted that the active pulse width must be at most 50% of the pulse period. This is a requirement on the software usage.

The pulse outputs are guaranteed to be spike free. If the re-synchronisation of the GRCTM in slave mode occurs within 0,5 ms of the expected synchronisation instance, the ongoing pulse output width will be accurate to within 0,5 ms. Else, the pulse output will remain unchanged corresponding to up to four times the expected output width.

If a pulse output is disabled by means of writing to the corresponding register (PDRx) (i.e. writing a zero to the Pulse Enable bit (PE)), the pulse output will be immediately driven to the inversion of the Pulse Level bit (PL), which corresponds to the level of the inactive part of the pulse. It is thus possible to modify immediately the pulse output by disabling it using the PE bit and then changing the PL bit, since the output will always drive the inversion of the PL bit while disabled.

128.3.7 Standard Spacecraft Time Source Packet

As mentioned above, the GRCTM comprises one datation register for sampling the ET counter when generating a Standard Spacecraft Time Source Packet according to the ESA Packet Telemetry Standard, AD2, according to the following programmable bit asynchronous protocol specification:

- 115200 baud (configured by generics/register bit)
- 1 start bit, 8 bit data, 1 or 2 stop bits (configured by generics/register bit)
- odd parity is generated (configured by generics/register bit)
- no handshake (note that there is a BUSY signal for internal handshake, that can block the generation of additional packets)
- message delimiting via BREAK command (13 zero bits when sent)

The Spacecraft Time Coarse Register (STCR) and the Spacecraft Time Fine Register (STFR) are available for readout of the datation time from the software. The software cannot block or initiate a datation on these registers, since controlled from an external input pin. If multiple datation have

occurred since the registers were previously read, only the time at the first datation can be read from the registers.

*Table 1897.*Standard Spacecraft Time Source Packet

Octet number	Name	Value
0	Packet Header Octet 0	0x00
1	Packet Header Octet 1	0x00
2	Segment Flags & Sequence Count (0 to 5)	11_b & 14 bit counter
3	Sequence Count (6 to 13)	
4	Packet Length (0 to 7)	0x00
5	Packet Length (8 to 15)	0x00
6	Data Field & Sample Rate (0 to 3)	0000b & sampling rate
7	P-Field	0x2F
8	T-Field (2^{31} to 2^{24})	
9	T-Field (2^{23} to 2^{16})	
10	T-Field (2^{15} to 2^{8})	
11	T-Field (2^{7} to 2^{0})	
12	T-Field (2^{-1} to 2^{-8})	
13	T-Field (2^{-9} to 2^{-16})	
14	T-Field (2^{-17} to 2^{-24})	

*Table 1898.*Time sample rate

Bit	Rate (in frames)	Bit	Rate (in frames)
0000_b	1	0101_b	32
0001_b	2	0110_b	64
0010_b	4	0111_b	128
0011_b	8	1000_b	256
0100_b	16	others	undefined

128.3.8 AMBA AHB slave interface

All time services, including the Elapsed Time counter in the embedded GRCTM core, are clocked by the AMBA AHB clock HCLK. All input signals are assumed to be synchronous with the AMBA AHB interface clock HCLK. No input signal synchronisation is performed in the core. All outputs are synchronous with the AMBA AHB interface clock.

The AMBA AHB slave interface supports 32 bit wide data input and output. Since each access is a word access, the two least significant address bits are assumed always to be zero. Only address bits 23:0 are decoded. Note that address bits 31:24 are not decoded and should thus be handled by the AHB arbiter/decoder. The address input of the AHB slave interfaces is thus incompletely decoded. Misaligned addressing is not supported. One wait state is introduced for read and write accesses.

When the CCSDS field is narrower than the AMBA data width, zeros are padded to the right. Re-mapping between the opposing numbering conventions in the CCSDS and AMBA documentation is performed automatically. For read accesses, unmapped bits are always driven to zero.

The interface provides direct access to the T-Field of the ET counter.

The AMBA AHB interface has been reduced in function to support only what is required for the GRCTM. The following AMBA AHB features are constrained:

- Only supports HSIZE=WORD, HRESP_ERROR generated otherwise
- Only supports HMASTLOCK='0', HRESP_ERROR generated otherwise
- Only supports HBURST=SINGLE and INCR, HRESP_ERROR generated otherwise
- No HPROT decoding
- No HSPLIT generated
- No HRETRY generated
- HRESP_ERROR generated for unmapped addresses, and for write accesses to register without any writeable bits
- Only big-endianness is supported.
- Frequency synthesis and time increment configuration

The increment values for the ET and FS counters depend on the implemented width of each counter and the frequency of the available on the system clock.

128.3.9 Miscellaneous

The accuracy of the transmission or reception baud rate of the bit asynchronous serial interface is dependent on the selected system frequency and baud rate. The number of system clock periods used for sending or receiving a bit is directly proportional to the integer part of the division of the system frequency with the baud rate.

The BREAK command received on the bit asynchronous serial interface is a sequence of logical zeros that is at least one bit period longer than the normal byte frame, i.e. start bit, eight data bits, optional parity, one or two stop bits. When transmitted, it is always 13 bits.

128.3.10Numbering and naming conventions

Convention according to the CCSDS recommendations, applying to time structures:

- The most significant bit of an array is located to the left, carrying index number zero.
- An octet comprises eight bits.

*Table 1899.*CCSDS n-bit field definition

CCSDS n-bit field		
most significant		least significant
0	1 to n-2	n-1

Convention according to AMBA specification, applying to the APB/AHB interfaces:

- Signal names are in upper case, except for the following:
- A lower case 'n' in the name indicates that the signal is active low.
- Constant names are in upper case.
- The least significant bit of an array is located to the right, carrying index number zero.
- Big-endian support.

*Table 1900.*AMBA n-bit field definition

AMBA n-bit field		
most significant		least significant
n-1	n-2 down to 1	0

General convention, applying to all other signals and interfaces:

- Signal names are in mixed case.
- An upper case '_N' suffix in the name indicates that the signal is active low.

128.4 Registers

The core is programmed through registers mapped into AHB I/O address space.

*Table 1901.*GRCTM registers

AHB address offset	Register
0x00	Global Reset Register (GRR)
0x04	Global Control Register (GCR)
0x08	Global Status Register (GSR)
0x0C	N/A
0x10	N/A
0x14	Preamble Field Register (PFR)
0x18	Elapsed Time Coarse Register (ETCR)
0x1C	Elapsed Time Fine Register (ETFR)
0x20	Datation Coarse Register 0 (DCR0)
0x24	Datation Fine Register 0 (DFR0)
0x28	Datation Coarse Register 1 (DCR1)
0x2C	Datation Fine Register 1 (DFR1)

*Table 1901.*GRCTM registers

AHB address offset	Register
0x30	Datation Coarse Register 2 (DCR2)
0x34	Datation Fine Register 2 (DFR2)
0x38	Spacecraft Time Datation Coarse Register (STCR)
0x3C	Spacecraft Time Datation Fine Register (STFR)
0x40	Pulse Definition Register 0
0x44	Pulse Definition Register 1
0x48	Pulse Definition Register 2
0x4C	Pulse Definition Register 3
0x50	Pulse Definition Register 4
0x54	Pulse Definition Register 5
0x58	Pulse Definition Register 6
0x5C	Pulse Definition Register 7
0x60	Pending Interrupt Masked Status Register
0x64	Pending Interrupt Masked Register
0x68	Pending Interrupt Status Register
0x6C	Pending Interrupt Register
0x70	Interrupt Mask Register
0x74	Pending Interrupt Clear Register
0x78	N/A
0x7C	N/A
0x80	Elapsed Time Increment Register (ETIR)
0x84	Frequency Synthesizer Increment Register (FSIR)
0x88	Serial Configuration Register
0x8C	N/A
0x90	TimeWire Start Configuration Register
0x94	TimeWire Adjust Configuration Register
0x98	TimeWire Transmit Configuration Register
0x9C	TimeWire Receive Configuration Register
0xA0	Set Elapsed Time Coarse Register (SetETCR)
0xA4	Set Elapsed Time Fine Register (SetETFR)

128.4.1 Global Reset Register

Table 1902. 0x00 - GRR - Global Reset Register

31 24	23 1	0
SEB	RESERVED	SRST
0	0	0
w	r	rw

31: 24 SEB (Security Byte):

Write: '0x55'= the write will have effect (the register will be updated). Any other value= the write will have no effect on the register.

Read: All zero.

23: 1 RESERVED

Write: Don't care.

Read: All zero.

0 System reset (SRST): **[1]**

Write: '1'= initiate reset,'0'= do nothing

Read: '1'= unsuccessful reset, '0'= successful reset

128.4.2 Global Control Register

Table 1903. 0x04 - GCR - Global Control Register

31 24	23 13	12	11	10	9	8	7	6 0
SEB	RESERVED	DRE2	DRE1	DRE0	EXT	SYNC	FREQDIS	RESERVED
0	0	0	0	0	0	0	0	0
w	r	rw	rw	rw	rw	rw	rw	r

31: 24 SEB (Security Byte):

Write: '0x55'= the write will have effect (the register will be updated). Any other value= the write will have no effect on the register.

Read: All zero.

23: 13 RESERVED

Write: Don't care.

Read: All zero.

12 Datation Register2 Edge (DRE2)

Write/Read: '0'= falling, '1'= rising

11 Datation Register1 Edge (DRE1)

Write/Read: '0'= falling, '1'= rising

10 Datation Register0 Edge (DRE0)

Write/Read: '0'= falling, '1'= rising

9 External synchronisation (EXT) (through external synchronisation interface)

Write/Read: '0'= disabled, '1'= enable.

8 Synchronise slave (SYNC) (through TimeWire)

Write/Read: '0'= disabled, '1'= enabled

7 Disable frequency synthesizer from driving Elapsed Time counter (FREQDIS)

Write/Read: '1'= disabled, '0'= enabled

6: 0 RESERVED

Write: Don't care.

Read: All zero.

128.4.3 Global Status Register

Table 1904. 0x08 - GSR - Global Status Register [8]

31 5	4	3	2	1	0
RESERVED	SARM	STL	DRL2	DRL1	DRL0
0	0	0	0	0	0
r	r	r	r	r	r

31: 5 RESERVED
- Write: Don't care.
- Read: All zero.

4 Set Elapsed Time counter Arm (SARM): [9]
- Write: Don't care.
- Read: '1' = Ready to set ET, '0' = reset value, or already ET has been set

3 Spacecraft Time Register Latched (STL): [3]
- Write: Don't care.
- Read: '1' = Latched with new value, '0' = old value

2 Datation Register 2 Latched (DRL2): [4]
- Write: Don't care.
- Read: '1' = Latched with new value, '0' = old value

1 Datation Register 1 Latched (DRL1): [4]
- Write: Don't care.
- Read: '1' = Latched with new value, '0' = old value

0 Datation Register 0 Latched (DRL0): [4]
- Write: Don't care.
- Read: '1' = Latched with new value, '0' = old value

128.4.4 Preamble Field Register

Table 1905. 0x14 - PFR - Preamble Field Register [8]

31 8	7 0
RESERVED	P-FIELD
0	0x2E
r	r

31: 8 RESERVED
- Write: Don't care.
- Read: All zero.

7: 0 Preamble Field (P-Field):
- Write: Don't care.
- Read: Static P-Field

128.4.5 Elapsed Time Coarse Register

*Table 1906.*0x18 - ETCR - Elapsed Time Coarse Register [8]

31 0
T-FIELD, COARSE
0
r

31: 0 T-Field, coarse part [5]
- Write: Don't care.
- Read: T-Field, coarse part

128.4.6 Elapsed Time Fine Register

*Table 1907.*0x1C - ETFR - Elapsed Time Fine Register [8]

31 8	7 0
T-FIELD, FINE	RESERVED
0	0
r	r

31: 8 T-Field, fine part [5]
- Write: Don't care.
- Read: T-Field, fine part

7: 0 RESERVED
- Write: Don't care.
- Read: All zero.

128.4.7 Datation Time Coarse Register 0

*Table 1908.*0x20 - DCR0 - Datation Time Coarse Register 0 [8]

31 0
T-FIELD, COARSE
0
r

31: 0 T-Field, coarse part [6]
- Write: Don't care.
- Read: T-Field, coarse part

128.4.8 Datation Time Fine Register 0

*Table 1909.*0x24 - DFR0 - Datation Time Fine Register 0 [8]

31 8	7 0
T-FIELD, FINE	RESERVED
0	0
r	r

31: 8 T-Field, fine part [6]
- Write: Don't care.
- Read: T-Field, fine part

7: 0 RESERVED
- Write: Don't care.
- Read: All zero.

128.4.9 Datation Time Coarse Register 1

*Table 1910.*0x28 - DCR1 - Datation Time Coarse Register 1 [8]

31 0
T-FIELD, COARSE
0
r

31: 0 T-Field, coarse part [6]
- Write: Don't care.
- Read: T-Field, coarse part

128.4.10Datation Time Fine Register 1

*Table 1911.*0x2C - DFR1 - Datation Time Fine Register 1 [8]

31 8	7 0
T-FIELD, FINE	RESERVED
0	0
r	r

31: 8 T-Field, fine part [6]
- Write: Don't care.
- Read: T-Field, fine part

7: 0 RESERVED
- Write: Don't care.
- Read: All zero.

128.4.11Datation Time Coarse Register 2

*Table 1912.*0x30 - DCR2 - Datation Time Coarse Register 2 [8]

31 0
T-FIELD, COARSE
0
r

31: 0 T-Field, coarse part [6]
- Write: Don't care.
- Read: T-Field, coarse part

128.4.12Datation Time Fine Register 2

*Table 1913.*0x34 - DFR2 - Datation Time Fine Register 2 [8]

31 8	7 0
T-FIELD, FINE	RESERVED
0	0
r	r

31: 8 T-Field, fine part [6]
- Write: Don't care.
- Read: T-Field, fine part

7: 0 RESERVED
- Write: Don't care.
- Read: All zero.

128.4.13Spacecraft Time Datation Coarse Register

*Table 1914.*0x38 - STCR - Spacecraft Time Datation Coarse Register [8]

31 0
T-FIELD, COARSE
0
r

31: 0 T-Field, coarse part [7]
- Write: Don't care.
- Read: T-Field, coarse part

128.4.14Spacecraft Time Datation Fine Register

*Table 1915.*0x3C - STFR - Spacecraft Time Datation Fine Register [8]

31 8	7 0
T-FIELD, FINE	RESERVED
0	0
r	r

31: 8 T-Field, fine part [7]
- Write: Don't care.
- Read: T-Field, fine part

7: 0 RESERVED
- Write: Don't care.
- Read: All zero.

128.4.15Pulse Definition Register 0 to 7

*Table 1916.*0x40 - 0x5C - PDR0 to PDR7 - Pulse Definition Register 0 to 7

31 24	23 20	19 16	15 11	10	9 2	1	0
RESERVED	PP	PW	RESERVED	PL	RESERVED	PE	R
0	0	0	0	1	0	0	0
r	rw	rw	r	rw	r	rw	r

31: 24 RESERVED
- Write: Don't care.
- Read: All zero.

23: 20 Pulse Period (PP):
- Write/Read:
  - '0000' = 2^{7} seconds
  - '0001' = 2^{6} seconds
  - '0010' = 2^{5} seconds
  - ...
  - '1110' = 2^{-7} seconds
  - '1111' = 2^{-8} seconds
  - Period = $2^{(7-PP)}$
  - Frequency = $2^{-(7-PP)}$

19: 16 Pulse Width (PW):
- Write/Read:
  - '0000' = 2^{6} seconds
  - '0001' = 2^{5} seconds
  - '0010' = 2^{4} seconds
  - ...

*Table 1916.*0x40 - 0x5C - PDR0 to PDR7 - Pulse Definition Register 0 to 7

	'1110'	=	2^{-8} seconds
	'1111'	=	2^{-9} seconds
	Width	=	$2^{(6-PW)}$

15: 11 RESERVED
- Write: Don't care.
- Read: All zero.

10 Pulse Level (PL): Defines logical level of active part of pulse output.
- Write/Read: '0'= Low, '1'= High

9: 2 RESERVED
- Write: Don't care.
- Read: All zero.

1 Pulse Enable (PE):
- Write/Read: '0'= disabled, '1'= enabled

0 RESERVED
- Write: Don't care.
- Read: All zero.

128.4.16Elapsed Time Increment Register

*Table 1917.*0x80 - ETIR - Elapsed Time Increment Register

31	7	0
RESERVED	ETINC	
0	*	
r	rw*	

7: 0 ETINC

Write/Read: Increment, in number ET Fine Time LSB.

(Presence of ETIR can be discovered by read/write access, resulting in an error if not implemented.)

128.4.17Frequency Synthesizer Increment Register

*Table 1918.*0x84 - FSIR - Frequency Synthesizer Increment Register

31	0
FSINC	
*	
rw*	

31: 0 FSINC

Write/Read: Increment

(The number of implemented bits can be discovered by writing all ones and the reading them back.)

(Presence of ETIR can be discovered by read/write access, resulting in an error if not implemented.)

128.4.18Serial Configuration Register

*Table 1919.*0x88 - SCR - Serial Configuration Register

31	30	29	28	27	16	15	0
R		ODD	TWO	RESERVED		BAUDTHRESHOLD	
0		*	*	0		*	
r		rw	rw	r		rw	

31: 30 RESERVED

28 ODD: Send odd parity and ignore received parity when set.

28 TWO: Send and receive two stop bits when set.

27: 16 RESERVED

15: 0 BAUDTHRESHOLD: Set baud rate: system frequency / baud rate

128.4.19TimeWire Start Configuration Register

*Table 1920.*0x90 - TWSC - TimeWire Start Configuration Register

31	8	7	0
START		RESERVED	
*		0	
rw		r	

31: 8 START: Defines T-Field fine part value when to start sending TimeWire message.

7: 0 RESERVED

128.4.20TimeWire Adjust Configuration Register

*Table 1921.*0x94 - TWAC - TimeWire Adjust Configuration Register

31 8	7 0
RESERVED	ADJUST
0	*
r	rw

31: 1 RESERVED

7: 0 ADJUST: Delay in number of systems clock when to start sending TimeWire message.

128.4.21TimeWire Transmit Configuration Register

*Table 1922.*0x98 - TWTC - TimeWire Transmit Configuration Register

31 1	0
RESERVED	TRANSMIT
0	*
r	rw

31: 1 RESERVED

0 TRANSMIT: T-Field fine part value other than 0 assumed for sent TimeWire message.

128.4.22TimeWire Receive Configuration Register

*Table 1923.*0x9C - TWRC - TimeWire Receive Configuration Register

31 8	7 0
RECEIVE	RESERVED
*	0
rw	w

31: 8 RECEIVE: Defines T-Field fine part value corresponding to received TimeWire message time point.

7: 0 RESERVED

128.4.23Set Elapsed Time Coarse Register

*Table 1924.*0xA0 - SETCR - Set Elapsed Time Coarse Register [9]

31 0
T-FIELD, COARSE
0
rw

31: 0 T-Field, coarse part [9]

Write: T-Field, coarse part

Read: T-Field, coarse part

128.4.24Set Elapsed Time Fine Register

*Table 1925.*0xA4 - SETFR - Set Elapsed Time Fine Register [9]

31 8	7 0
T-FIELD, FINE	RESERVED
0	0
rw	r

31: 8 T-Field, fine part [9]
- Write: T-Field, fine part
- Read: T-Field, fine part

7: 0 RESERVED
- Write: Don't care.
- Read: All zero.

Legend:

[1] The global system reset caused by the SRST-bit in the GRR-register results in the following actions:

- Initiated by writing a '1", gives '0' on read-back when the reset was successful.
- No need to write a '0' to remove the reset.
- Unconditionally, means no need to check/disable something in order for this reset-function to correctly execute.
- Could of course lead to data-corruption coming/going from/to the reset core.

Behaviour:

- Resets the complete core (all logic, buffers & register values)

(except for the ET and FS counters which continue running undisturbed)

- Behaviour is similar to a power-up.
- This reset shall not cause any spurious interrupts

{Note that the above actions require that the HRESET signal is fed back inverted to HRESETn}

[2] The channel reset results in the following actions:

Not implemented in Global Configuration Register.

[3] This bit is sticky which means that it remains asserted until the corresponding STFR register is read at which time the bit is cleared. The corresponding registers should be read in the STCR – STFR order.

[4] This bit is sticky which means that it remains asserted until the corresponding Defraud register is read at which point the bit is cleared. The corresponding registers should be read in the DCRx – DFRx order.

[5] When ETCR is read, the ETFR register is latched and are not released until ETFR has been read. The registers should be read in the ETCR – ETFR order.

[6] The coarse and fine time part of the register pair is latched on an external event and is released on reading the corresponding fine time register. No new event is accepted until the corresponding fine time register has been read.

[7] The coarse and fine time part of the register pair is latched on an external event. No new event is accepted until the corresponding fine time register has been read. This does not prevent datations to occur and Standard Spacecraft Time Source Packet to be generated.

[8] An AMBA AHB ERROR response is generated if a write access is attempted to a register which does not have any writeable bits.

[9] The GSR.SARM bit is set when the SetETFR register is written to. It is cleared when an active high signal is detected on the CTMIN.SETET input, at which point the SetETCR and SetETFR contents are written to the ET counter (ETCR and ETFR) and the frequency synthesizer is reset. Only available when gSetET VHDL generic is set to 1.

128.4.25Interrupt registers

The interrupt registers give complete freedom to the software, by providing means to mask interrupts, clear interrupts, force interrupts and read interrupt status.

When an interrupt occurs the corresponding bit in the Pending Interrupt Register is set. The normal sequence to initialize and handle a module interrupt is:

- Set up the software interrupt-handler to accept an interrupt from the module.
- Read the Pending Interrupt Register to clear any spurious interrupts.
- Initialize the Interrupt Mask Register, unmasking each bit that should generate the module interrupt.
- When an interrupt occurs, read the Pending Interrupt Status Register in the software interrupt-handler to determine the causes of the interrupt.
- Handle the interrupt, taking into account all causes of the interrupt.
- Clear the handled interrupt using Pending Interrupt Clear Register.

Masking interrupts: After reset, all interrupt bits are masked, since the Interrupt Mask Register is zero. To enable generation of a module interrupt for an interrupt bit, set the corresponding bit in the Interrupt Mask Register.

Clearing interrupts: All bits of the Pending Interrupt Register are cleared when it is read or when the Pending Interrupt Masked Register is read. Reading the Pending Interrupt Masked Register yields the contents of the Pending Interrupt Register masked with the contents of the Interrupt Mask Register. Selected bits can be cleared by writing ones to the bits that shall be cleared to the Pending Interrupt Clear Register.

Forcing interrupts: When the Pending Interrupt Register is written, the resulting value is the original contents of the register logically OR-ed with the write data. This means that writing the register can force (set) an interrupt bit, but never clear it.

Reading interrupt status: Reading the Pending Interrupt Status Register yields the same data as a read of the Pending Interrupt Register, but without clearing the contents.

Reading interrupt status of unmasked bits: Reading the Pending Interrupt Masked Status Register yields the contents of the Pending Interrupt Register masked with the contents of the Interrupt Mask Register, but without clearing the contents.

The interrupt registers comprise the following:

- Pending Interrupt Masked Status Register[PIMSR]R
- Pending Interrupt Masked Register[PIMR]R
- Pending Interrupt Status Register[PISR]R
- Pending Interrupt Register[PIR]R/W
- Interrupt Mask Register[IMR]R/W
- Pending Interrupt Clear Register[PICR]W

*Table 1926.*0x60 - 0x74 - IR - Interrupt registers

31 13	12	11		4	3	2	1	0
R	ETSET	PULSE7	...	PULSE0	STL	DRL2	DRL1	DRL0
0	0	0	0	0	0	0	0	0
r	rw	rw	rw	rw	rw	rw	rw	rw

12: ETSET ET has been set from SetETCR and SetETFR registers (only when VHDL generic gSetET is 1)
11: PULSE7 Pulse 7 interrupt
10: PULSE6 Pulse 6 interrupt
9: PULSE5 Pulse 5 interrupt
8: PULSE4 Pulse 4 interrupt
7: PULSE3 Pulse 3 interrupt
6: PULSE2 Pulse 2 interrupt
5: PULSE1 Pulse 1 interrupt
4: PULSE0 Pulse 0 interrupt
3: STL Spacecraft Time Register Latched

2:	DRL2	Datation Register 2 Latched
1:	DRL1	Datation Register 1 Latched
0:	DRL0	Datation Register 0 Latched

All bits in all interrupt registers are reset to 0b after reset.

128.5 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x033. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

128.6 Configuration options

Table 1927 shows the configuration options of the core (VHDL generics).

*Table 1927.*Configuration options

Generic	Function	Description	Allowed range	Default
GRLIB AMBA plug&play settings				
hindex	AHB slave index		Integer	0
hirq	AHB slave interrupt		Integer	0
singleirq	Single interrupt	Enable interrupt registers	Integer	0
ioaddr	IO area address		0 - 16#FFF#	0
iomask	IO area mask		0 - 16#FFF#	16#FFF#
syncrst	synchronous reset		0 - 1	0
Features settings				
gProgrammable	Programmable	ET and FS increment, and TimeWire	0 - 1	0
gExternal	External support	Support for external synchronization input	0 - 1	0
gMaster	Master CTM support		0 - 1	0
gSlave	Slave CTM support		0 - 1	0
gDatation	Datation support		0 - 1	0
gPulse	Pulse support		0 - 1	0
gTimePacket	Time Packet support		0 - 1	0
gSetET	Set ET support	Register from which ET is set on next. input	0 - 1	0
Frequency synthesizer and Elapsed Time counter settings				
gFrequency	Frequency Synthesizer	Defines the accuracy of the synthesized reference time, the wider the synthesizer the less drift is induced.	2 - 32	30
gETIncrement	Increment of ET counter	Defines with what value the Elapsed Time counter is to be incremented each time when the Frequency Synthesizer wraps around. The ET increment needs to match the synthesized frequency.	Integer	4
gFSIncrement	Increment of FS counter	Defines increment value of the Frequency Synthesizer which is added to the counter every system clock cycle. It defines the frequency of the synthesized reference time. Should match ET increment.	Integer	135107990
TimeWire settings				
gTWStart	ETF at msg start	ET Fine at start of message [1]	Integer	16#FFE330#
gTWAdjust	Adjust phase of msg	System clock based tuning of message start	Integer	5
gTWTransmit	ETF at transmission	ET Fine at synchronisation (master) [1]	Integer	16#000000#
gTWRecieve	ETF at reception	ET Fine at synchronisation (slave) [1] [2]	Integer	16#FFE000#
gDebug	Debug when set	Only used for TW settings adjustments.	0 - 1	0
Asynchronous bit serial interface settings (TimeWire and Time Packet)				
gSystemClock	System frequency	System clock frequency [Hz]	Integer	33333333
gBaud	Baud rate	[Baud]	Integer	115200
gOddParity	Odd parity	Odd parity generated, but not checked	0 - 1	0
gTwoStopBits	Number of stop bits	0=one stop bit, 1=two stop bits	0 - 1	0

Legend:

[1] These generics are defined as 32 bit ET fine time values, thus 16#FFE000# corresponds to all the 24 implemented bits being all-ones.

[2] For proper mitigation of spikes on the Pulses[0:7] outputs, only the leftmost bits should be set.

128.7 Signal descriptions

Table 1928 shows the interface signals of the core (VHDL ports).

*Table 1928.*Signal descriptions

Signal name	Field	Type	Function	Description	Active
HRESETn	N/A	Input	Reset	Resets the ET & FS in the VHDL core. The signal is assumed synchronous with rising HCLK edge.	Low
CRESETn	N/A	Input	Reset	Resets all logic but the ET & FS in the VHDL core. The signal is assumed synchronous with rising HCLK edge.	Low
HCLK	N/A	Input	Clock		-

*Table 1928.*Signal descriptions

Signal name	Field	Type	Function	Description	Active
CTMIN	TWSLAVE	Input	TimeWire slave	TimeWire input	-
	DATATION		Datation input	The inputs are sampled on rising HCLK edge.	-
	TIMEMODE		Time rate select	Selects the rate of the time strobe periodicity	-
	TIMESTROBE		Time strobe input		-
	TIMEBUSY_N		Time packet busy		Low
	EXTERNALTIME		Elapsed Time	ET coarse [31:0] & ET fine [-1:-24]	-
	EXTERNALSYNC		Synchronization		High
	SETET		Set ET	Pulse to set ET from reg.	High
CTMOUT	TWMASTER	Output	TimeWire master	TimeWire output	
	PULSES		Pulse outputs	The outputs are driven on rising HCLK edge.	-
	TIMEPKT		Time packet data		-
	ELAPSEDTIME		Elapsed Time	ET coarse [31:0] & ET fine [-1:-24]	-
	ELAPSEDNEXT		Next Elapsed Time	ET coarse [31:0] & ET fine [-1:-24]	-
	ELAPSEDEVENT		ET increment		High
	ELAPSEDSYNC		Synchronisation		High
AHBIN	*	Input	AMB slave input signals		-
AHBOUT	*	Output	AHB slave output signals		-
	HIRQ(hirq+12)		Interrupts	ETSET output	Location on HIRQ bus depends on *hirq* generic. If *hirq*=0, no interrupt will be generated. If *singleirq*=1 only one common interrupt will be generate using *hirq*.
	HIRQ(hirq+11)			PULSES(7) output	
	HIRQ(hirq+10)			PULSES(6) output	
	HIRQ(hirq+9)			PULSES(5) output	
	HIRQ(hirq+8)			PULSES(4) output	
	HIRQ(hirq+7)			PULSES(3) output	
	HIRQ(hirq+6)			PULSES(2) output	
	HIRQ(hirq+5)			PULSES(1) output	
	HIRQ(hirq+4)			PULSES(0) output	
	HIRQ(hirq+3)			STL	
	HIRQ(hirq+2)			DRL2	
	HIRQ(hirq+1)			DRL1	
	HIRQ(hirq+0)			DRL0	

* see GRLIB IP Library User's Manual

128.8 Signal definitions and reset values

The signals and their reset values are described in table 1929.

*Table 1929.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
twmaster	Output	UART transmit data line	-	Logical 1
twslave	Input	UART receive data line	-	-
pulses	Output	Pulse output	-	Logical 0
datation	Input	Datation input	-	-
timemode	Input	Time rate select	-	-
timestrobe	Input	Time strobe input	-	-
timepkt	Output	Time packet data	-	Logical 0
timebusy_n	Input	Time packet busy	-	Low

128.9 Timing

The timing waveforms and timing parameters are shown in figure 324 and are defined in table 1930.

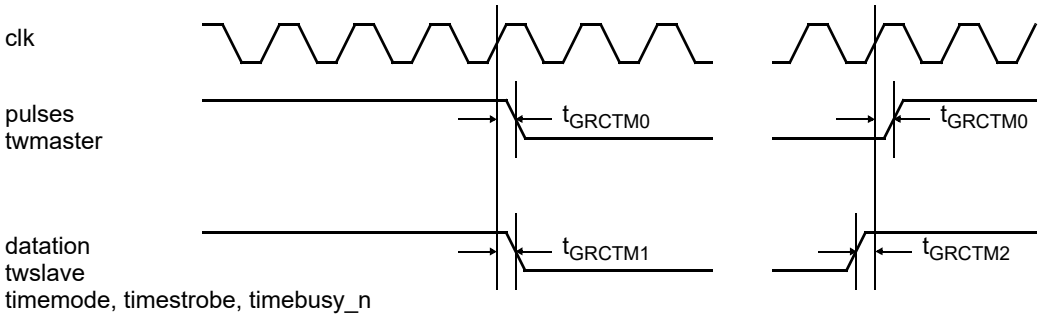


Figure 324. Timing waveforms

*Table 1930.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{GRCTM0}	clock to output delay	rising *clk* edge	TBD	TBD	ns
t_{GRCTM1}	input to clock hold	rising *clk* edge	-	-	ns
t_{GRCTM2}	input to clock setup	rising *clk* edge	-	-	ns

Note: The inputs are re-synchronized internally. The signals do not have to meet any setup or hold requirements.

128.10 Library dependencies

Table 1931 shows libraries used when instantiating the core (VHDL libraries).

*Table 1931.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
TMTC	TMTC_Types	Signals, component	Signals and component declaration

128.11 Instantiation

This example shows how the core can be instantiated.

```
   library  IEEE;
   use      IEEE.Std_Logic_1164.all;
   library  GRLIB;
   use      GRLIB.AMBA.all;
   library  TMTC;
   use      TMTC.TMTC_Types.all;

...

   component GRCTM is
   generic(
      hindex:        in    Integer                := 0;
      hirq:          in    Integer                := 0;
      ioaddr:        in    Integer                := 0;
      iomask:        in    Integer                := 16#fff#;
      syncrst:       in    Integer                := 0;
      gProgrammable: in    Integer                := 0;
      gExternal:     in    Natural range 0 to 1   := 0;  -- External sync
      gMaster:       in    Natural range 0 to 1   := 1;  -- Master CTM support
      gSlave:        in    Natural range 0 to 1   := 1;  -- Slave CTM support
      gDatation:     in    Natural range 0 to 1   := 1;  -- Datation support
      gPulse:        in    Natural range 0 to 1   := 1;  -- Pulse support
      gTimePacket:   in    Natural range 0 to 1   := 1;  -- Time Packet support

      gFrequency:    in    Positive               := 30; -- Frequency Synthesize
      gETIncrement:  in    Natural := 4;                 -- ET increment
      gFSIncrement:  in    Natural := 135107990;         -- FS increment

      gTWStart:      in    Natural := 16#FFE330#;        -- ETF at start of msg
      gTWAdjust:     in    Natural := 5;                 -- Adjust phase of msg
      gTWTransmit:   in    Natural := 16#000000#;        -- ETF at transmision
      gTWRecieve:    in    Natural := 16#FFE000#;        -- ETF at reception

      gSystemClock:  in    Natural := 33333333;          -- System frequency[Hz]
      gBaud:         in    Natural := 115200;            -- Baud rate
      gOddParity:    in    Natural range 0 to 1   := 0;  -- Odd parity
      gTwoStopBits:  in    Natural range 0 to 1   := 0;  -- Two stop bits
      gDebug:        in    Natural range 0 to 1   := 0); -- Debug mode when set
   port(
      -- AMBA AHB system signals
      HCLK:          in    Std_ULogic;                   -- System clock
      HRESETn:       in    Std_ULogic;                   -- Synchronised reset
      CRESETn:       in    Std_ULogic;                   -- Synchronised reset

      -- AMBA AHB slave interface
      AHBIn:         in    AHB_Slv_In_Type;              -- AHB slave input
      AHBOut:        out   AHB_Slv_Out_Type;             -- AHB slave output

      -- Time interfaces
      CTMIn:         in    GRCTM_In_Type;
      CTMOut:        out   GRCTM_Out_Type);
   end component GRCTM;
```

128.12 Configuration tuning

The gFrequency generic defines the width of the Frequency Synthesiser (FS). The greater the width, the smaller the drift induced. The gFSIncrement generic defines with what value the FS counter should be incremented to obtain a synthesized frequency that matches the least significant bit of the Elapsed Time (ET) counter, normally being 2**24 Hz. It is also possible to synthesize a frequency less than 2**24 Hz, which will require the gETIncrement generic to have a higher value than the default 1.

The gETIncrement generic defines with what value the ET counter should be incremented. The specified value is added to the current ET counter value. The addition is done to the least significant bit in the fine part of the ET counter, i.e. gETIncrement is multiplied with 2**-24 before the addition. The gETIncrement is normally set to 1, since the obtained synthesised frequency is normally 2**24 Hz.

For lower frequencies, the gETIncrement generic must be larger than 1. Note that the synthesized frequency must always be a power of two.

The following paragraphs define synchronization via the optional TimeWire master and slave interfaces.

The gTWStart generic defines at what time the transmission of the TimeWire message should start on the TWMaster output. The gTWStart value corresponds to the ET counter fine part assuming 24 bit resolution. E.g. 16#FFE330# corresponds to bit 2**-1 to 2**-24. The gTWAdjust generic defines the number of HCLK periods that should pass between the gTWStart time has occurred and the TimeWire message should be sent. This allows for fine grained adjustment of the starting point for the TimeWire message.

The gTWTransmit generic defines the ET fine part value that is transmitted virtually to the slave. Its only consequence is to decide whether the ET coarse part to be sent in the TimeWire message should be the same as the current ET in the master or be incremented by one second. The gTWRecieve generic defines the ET fine part value that should be loaded into the ET at synchronisation. Normally this will be 0 for slave only applications of the GRCTM.

When the gDebug generic is 1, the ET counter reset will be 0x000000 for the coarse part and 0xFF0000 for the fine part (assuming CUC 32 & 24 bit resolution). This achieves an ET synchronisation early in a simulation without the need to wait for a second of simulation time.

128.12.1Master configuration

The master configuration is used for the source of the time chain and supports the following features:

- Frequency Synthesizer (FS) and Elapsed Time (ET) counters
- Master TimeWire interface
- Datation by means of direct read out of the ET counter via AMBA AHB interface

The following register are available in this configuration: GRR, GCR, GSR, ETCR, ETFR.

Table 1927 shows the master configuration.

*Table 1932.*Master configuration

Generic	Function	Default
Features settings		
gMaster	Master CTM support	1
gSlave	Slave CTM support	0
gDatation	Datation support	0
gPulse	Pulse support	0
gTimePacket	Time Packet support	0
Frequency synthesizer and Elapsed Time counter settings		
gFrequency	Frequency Synthesizer	30
gETIncrement	Increment of ET counter (In this example a resolution is 2**-22 due to the slow system frequency.)	4
gFSIncrement	Increment of FS counter	135107990
TimeWire settings		
gTWStart	ETF at msg start	16#FFC3300#
gTWAdjust	Adjust phase of msg	5
gTWTransmit	ETF at transmission	16#FFE000#
gTWRecieve	ETF at reception	16#000000#
gDebug	Debug when set	0
Asynchronous bit serial interface settings (TimeWire and Time Packet)		
gSystemClock	System frequency	33333333
gBaud	Baud rate	115200
gOddParity	Odd parity	0
gTwoStopBits	Number of stop bits	0

128.12.2Master/Slave configuration

The master/slave configuration is used for an intermediate unit in the time chain, and supports all features.

All registers are available in this configuration.

Table 1927 shows the master/slave configuration.

*Table 1933.*Master/Slave configuration

Generic	Function	Default
Features settings		
gMaster	Master CTM support	1
gSlave	Slave CTM support	1
gDatation	Datation support	1
gPulse	Pulse support	1
gTimePacket	Time Packet support	1
Frequency synthesizer and Elapsed Time counter settings		
gFrequency	Frequency Synthesizer	30
gETIncrement	Increment of ET counter (In this example a resolution is 2**-22 due to the slow system frequency.)	4
gFSIncrement	Increment of FS counter	135107990
TimeWire settings		
gTWStart	ETF at msg start	16#FFE330#
gTWAdjust	Adjust phase of msg	5
gTWTransmit	ETF at transmission	16#0000000#
gTWRecieve	ETF at reception	16#FFE000#
gDebug	Debug when set	0
Asynchronous bit serial interface settings (TimeWire and Time Packet)		
gSystemClock	System frequency	33333333
gBaud	Baud rate	115200
gOddParity	Odd parity	0
gTwoStopBits	Number of stop bits	0

128.12.3Slave configuration

The slave configuration is used for a sink at the end of the time chain, e.g. in the payload, and supports the following features:

- Frequency Synthesizer (FS) and Elapsed Time (ET) counters
- Slave TimeWire interface
- Datation by means of direct read out of the ET counter via AMBA AHB interface

Note that the slave configuration can also support other features as required. Only those necessary for proper operation have been listed above.

The following register are available in this configuration: GRR, GCR, GSR, ETCR, ETFR.

Table 1927 shows the slave configuration.

*Table 1934.*Slave configuration

Generic	Function	Default
Features settings		
gMaster	Master CTM support	0
gSlave	Slave CTM support	1
gDatation	Datation support	0
gPulse	Pulse support	0
gTimePacket	Time Packet support	0
Frequency synthesizer and Elapsed Time counter settings		
gFrequency	Frequency Synthesizer	30
gETIncrement	Increment of ET counter (In this example a resolution is 2**-22 due to the slow system frequency.)	4
gFSIncrement	Increment of FS counter	135107990
TimeWire settings		
gTWStart	ETF at msg start	16#000000#
gTWAdjust	Adjust phase of msg	0
gTWTransmit	ETF at transmission	16#000000#
gTWRecieve	ETF at reception	16#000000#
gDebug	Debug when set	0
Asynchronous bit serial interface settings (TimeWire and Time Packet)		
gSystemClock	System frequency	33333333
gBaud	Baud rate	115200
gOddParity	Odd parity	0
gTwoStopBits	Number of stop bits	0

129 SPWCUC - SpaceWire - CCSDS Unsegmented Code Transfer Protocol

129.1 Overview

This interface implements the SpaceWire - CCSDS Unsegmented Code Transfer Protocol (CUCTP), providing automatic SpaceWire Time-Code transmission and reception, and automatic CUCTP packet reception. It also provides support for CUCTP packet transmission.

The SpaceWire - CCSDS Unsegmented Code Transfer Protocol interface (SPWCUC) is assumed to operate in an AMBA bus system where AMBA APB bus is present. The AMBA APB bus is used for configuration, control and status handling. The interface is tightly coupled with the CCSDS Time Manager (GRCTM) and the SpaceWire codec with AHB host Interface and RMAP target (GRSPW2).

129.2 Protocol

The SpaceWire - CCSDS Unsegmented Code Transfer Protocol (CUCTP) provides synchronization between Elapsed Time (ET) counters in the local node and remote nodes, by means of SpaceWire Time-Codes and SpaceWire packets. The time format conforms to the CCSDS Unsegmented Code format.

*Table 1935.*SpaceWire - CCSDS Unsegmented Code Transfer Protocol

Destination Logical Address	Protocol Identifier	CCSDS Unsegmented Code										CRC	EOP
		P-Field		T-Field									
		1st	2nd	Coarse Time				Fine Time					
				2^{31} 2^{24}	2^{23} 2^{16}	2^{15} 2^{8}	2^{7} 2^{0}	2^{-1} 2^{-8}	2^{-9} 2^{-16}	2^{-17} 2^{-24}			*weight*
		0 7	8 15	0 7	8 15	16 23	24 31	32 39	40 47	48 55			*index*
8 bits	8 bits	8 bits	8 bits	8 bits	8 bits	8 bits	8 bits	8 bits	8 bits	8 bits		8 bits	*no. of bits*

SpaceWire Time-Codes are continuously transmitted from a master node to all slave nodes. The transmission of the Time-Codes is synchronized with the local ET counter in the master node. The six bits of the Time-Code time information correspond to six bits of the local ET counter (its exact mapping being programmable by means of register access). The ET bits with lower weights than the size bits mapped to the Time-Code time information bits are all zero at time of Time-Code transmission.

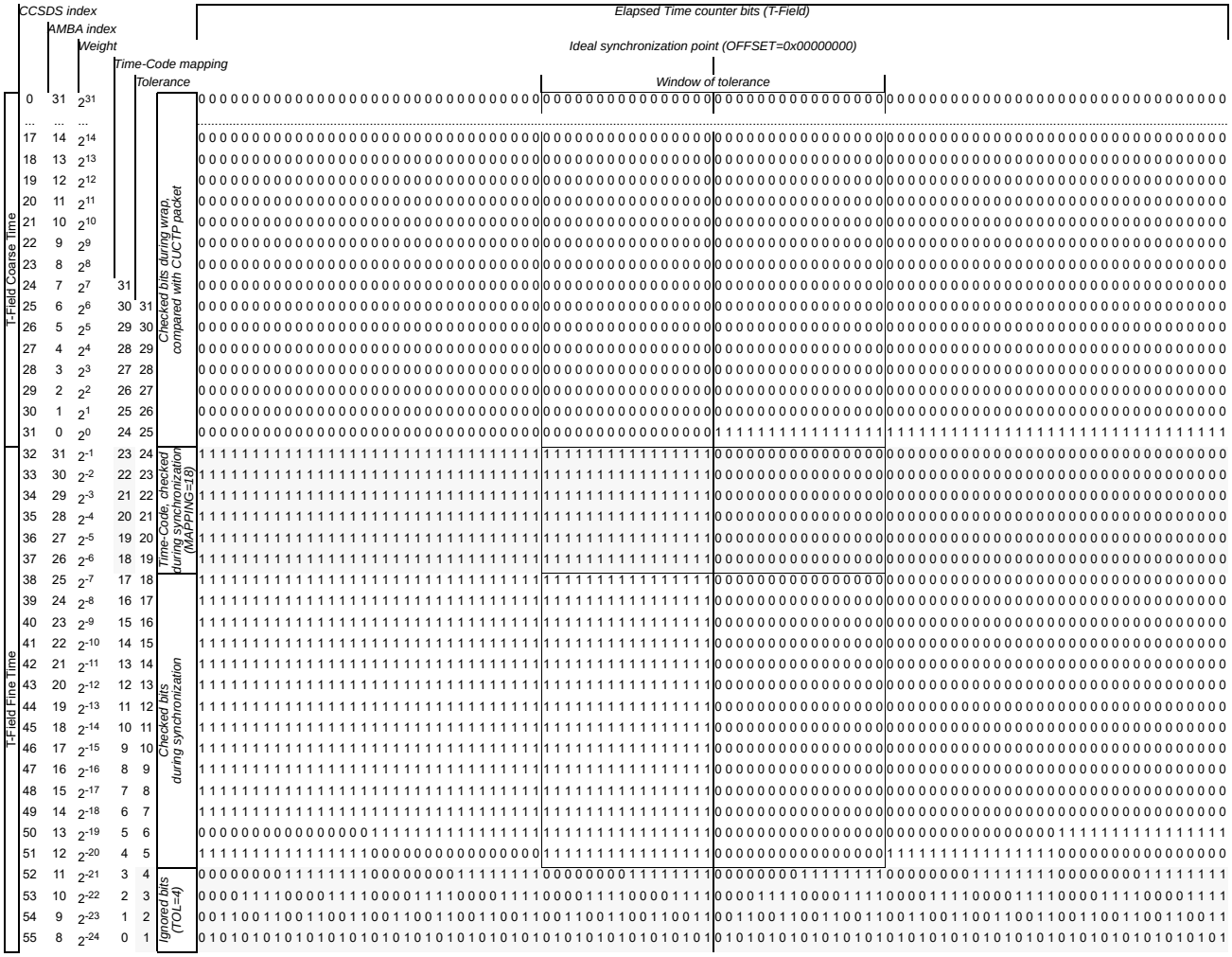
When a Time-Code is received in a slave node, the Time-Code time information is first verified to be an increment of the previously received time-information. The event of the Time-Code reception is assumed to occur synchronously with the local ET counter in the slave node. It is possible to allow a window of tolerance surrounding the exact time at which the reception event was expected. If the event was outside the window of tolerance a tolerance error has occurred and the no further synchronization is performed. Note that the check means that the ET counter bits with weights lower than the six ET bits mapped to the Time-Code time information are checked to have an expected value. This expected value is programmable by means of register access and should be seen as an offset from the all zero value (c.f. Time-Code transmission timing above). The check of the ET counter bits with the lower weights is done with respect to the expected value and the expected value -1 (see further down for the definition of -1). Thus, the ideal point at which a Time-Code can be received is just at the transition to the expected value. The window of tolerance means that a programmable number of ET bits with the lowest weights are ignored in the above comparisons. Note also that the window of tolerance is symmetrical around the expected value and that the -1 subtraction corresponds to the ET bit with the lowest weight that is not ignored due to the window of tolerance.

If the Time-Code reception event was within the window of tolerance, the time information is compared with the corresponding bits in the local ET counter. If there is a match then the two ET counters are considered to be synchronized. If there is a mismatch, then a synchronization error has occurred. Note that during synchronization only the six bits of the ET mapped to the Time-Code time information bits are considered for synchronization. If no Time-Code is received within the window, then the local ET is considered to still be in synchronization but it is freewheeling on Time-Code level.

Additionally, whenever the Time-Code time information wraps from 0x3F to 0x00 it is possible to synchronize the ET bits that have a higher weight than the bits mapped to the Time-Code time information bits. This is performed whenever a new CUCTP packet has been received preceding the reception of the Time-Code with the wrapping time information. If no such packet has been received, then the synchronization will be as described above, but with an increment of the ET bits with the higher weight. If a new and valid CUCTP packet has been received, then in addition to checking the six ET bits, the ET bits with a higher weight are compared with the corresponding ET bits received in the CUCTP packet. If there is a mismatch, then a wrapping error has occurred. If no packet has been received, then the local ET is considered to still be in synchronization but it is freewheeling on packet level.

To summarize, ET bits mapped to the Time-Code time information bits and ET bits with lower weight are checked for every Time-Code received; whilst ET bits with higher weight are checked when ever time information is wrapping. ET bits with lower weight can be offset from the all zero value. ET bits with the lowest weight can be ignored to form a window of tolerance.

*Table 1936.*Example of synchronization



129.3 Functionality

The interface implements the following functions:

- transmission of SpaceWire Time-Codes
- reception of SpaceWire Time-Codes
- reception of SpaceWire - CCSDS Unsegmented Code Transfer Protocol (CUCTP) packets
- verification of SpaceWire Time-Codes to be received within window of tolerance
- synchronization of SpaceWire Time-Codes time information with local Elapsed Time counter in CCSDS Time Manager (GRCTM) using its external synchronization interface
- synchronization of SpaceWire - CCSDS Unsegmented Code Transfer Protocol (CUCTP) packets with local Elapsed Time counter in CCSDS Time Manager (GRCTM) using its external synchronization interface, occurring on the wrapping of SpaceWire Time-Codes time information
- support for transmission of SpaceWire - CCSDS Unsegmented Code Transfer Protocol (CUCTP) packets

129.3.1 SpaceWire Time-Code transmission

SpaceWire Time-Code transmission is normally performed by a single master node in a system.

SpaceWire Time-Code transmission can be enabled by means of register access. SpaceWire Time-Codes can be transmitted simultaneously on one to four possible outputs, selectable by means of register access.

The six bits of the Time-Code time information are mapped to six bits of the local ET counter, by means of register access. The least significant time information bit [index 0] can be mapped to one of the 32 ET counter bits with the lowest weights.

When Time-Code time information is transmitted, an interrupt is generated (TickTx). If the Time-Code time information is wrapping from 0x3F to 0x00, an interrupt is generated (TickTxWrap).

129.3.2 SpaceWire Time-Code reception

SpaceWire Time-Code reception can be enabled by means of register access. SpaceWire Time-Codes can be received from one of four possible inputs, selectable by means of register access.

When SpaceWire Time-Code reception is enabled, the received Time-Code time information is checked to be an increment of the previously received Time-Code time information. If not, a Time-Code reception error interrupt is generated (TickRxError). If the received Time-Code time information is not an increment, then the received Time-Code time information is stored for the next comparison but is not used for further processing as described hereafter. If the received Time-Code time information is equal to the previously received Time-Code time information, then no action is taken and no interrupts are generated.

The Time-Code control flag can be checked to be “00”, selectable by means of register access. If checking is enabled, control flag differing from “00” will generate a Time-Code reception error interrupt (TickRxError).

If the expected Time-Code time information (and optionally control flags) is received, an interrupt is generated (TickRx). If the Time-Code time information is wrapping from 0x3F to 0x00, an interrupt is generated (TickRxWrap). Both events qualify the Time-Code time information for further processing as described hereafter.

129.3.3 CCSDS Unsegmented Code Transfer Protocol (CUCTP) packet reception

SpaceWire - CCSDS Unsegmented Code Transfer Protocol packets can be automatically received when enabled by means of register access. General SpaceWire communication is performed by the

GRSPW2 SpaceWire codec, which outputs received characters unfiltered to the SPWCUC interface. The SPWCUC interface implements the reception and checking of the CUCTP packet format.

Destination Logical Address (DLA) as per ECSS-E-ST-50-51C. Packets with non-matching DLA are discarded. The DLA is programmable in the range 0x00 to 0xFF by means of register access. The DLA can also be masked with a programmable mask pattern, by means of register access.

The Protocol Identifier as per ECSS-E-ST-50-51C. Packets with non-matching Protocol Identifier are discarded. The Protocol Identifier is programmable in the range 0x00 to 0xFF, as per ECSS-E-ST-50-51C, by means of register access.

Fixed and programmable bits of the P-Field are checked with expected values. The Detail bits for information on the code are fixed to “1111”. The Time code identification is optionally compared to a programmable value, accessible through register access. Reserved bits for future use are checked to be fixed to “000000”. If any of the bits of the received P-Field are incorrect, the packet is discarded and an error interrupt is generated (PktError).

The packet CRC is the same as for RMAP as per ECSS-E-ST-50-52C.

Packets with incorrect CRC are discarded and an error interrupt is generated (PktError).

Packet without an End-Of-Packet (EOP) or an Error-End-of-Packet (EEP) are discarded and an error interrupt is generated (PktError). Too long or too short packets are discarded and an error interrupt is generated (PktError).

A correctly received packet is considered for synchronization, and an interrupt is generated (PktRx). Note that the fully, partially or incorrectly received packet is accessible through register access.

129.3.4 Verification of Time-Codes to be received within tolerance

SpaceWire Time-Code reception can be enabled by means of register access.

The reception time offset is programmable by means of register access. The offset is always counted from the all zero value corresponding to the time at which the Time-Code transmission started. The programmable offset is 32 bit wide and corresponds to the ET bits with the lowest weight.

The window of tolerance is programmable by means of register access. Up to 31 least significant bits can be ignored during Time-Code event comparison with the local ET counter. Note that the window of tolerance is a binary coded window.

If a received Time-Code event is outside the window of tolerance an error interrupt is generated (ToleranceError) and no further synchronization check are attempted for this specific Time-Code. The status will indicate that the local ET is out of synchronization (InSync, FreeSync and FreePkt are cleared).

The window of tolerance should not have a larger width than half the offset. Note that bits in the offset can be masked and ignored by the window of tolerance and will then not be used in the comparison.

If no Time-Code is received within the window of tolerance, then the local ET is considered to still be in synchronization (InSync set) but it is freewheeling on Time-Code level (FreeSync set).

129.3.5 Synchronization via Time-Codes

Synchronization by means of Time-Code reception can be enabled by means of register access, and occurs on reception Time-Codes the window of tolerance as described above.

If the check passes, the status indicates that the local ET is in synchronization (InSync set) and an interrupt is generated (Sync).

If the check fails, an error interrupt is generated (SyncError). The status indicates that the local ET is out of synchronization (InSync, FreeSync and FreePkt are cleared).

If the received Time-Code time information was wrapping and no new CUCTP packet was previously received, then the status indicates that the local ET is freewheeling on packet level (FreePkt set).

129.3.6 Synchronization via CUCTP packets

Synchronization by means of CUCTP packets can be enabled by means of register access, and occurs on reception Time-Codes the window of tolerance as described above when the time information is wrapping. Only correctly received and checked CUCTP packet are considered for synchronization, which have bit 15 in the P-Field cleared (meaning synchronization).

If the check passes, the status indicates that the local ET is in synchronization (InSync set) and an interrupt is generated (Wrap).

If the check fails, an error interrupt is generated (WrapError). The status indicates that the local ET is out of synchronization (InSync, FreeSync and FreePkt are cleared).

129.3.7 Initialization via CUCTP packets

Initialization by means of CUCTP packets can be enabled by means of register access, and occurs on reception Time-Codes the window of tolerance as described above when the time information is wrapping. Only correctly received and checked CUCTP packet are considered for synchronization, which have bit 15 in the P-Field set (meaning initialization).

No other checks are performed. The status indicates that the local ET is in synchronization (InSync set) and an interrupt is generated (Init).

129.3.8 CCSDS Unsegmented Code Transfer Protocol (CUCTP) packet transmission support

CUCTP packet transmission is normally performed by a single master node in a system.

When a Time-Code has been transmitted with time information that is wrapping from 0x3F to 0x00, an interrupt is generated (TickTxWrap) which can be used as a starting point for software controlled generation and transmission of CUCTP packets. The next T-Field to be sent in the CUCTP packet can be read out by means of register access.

129.4 Data formats

All Elapsed Time (ET) information is compliant with the CCSDS Unsegmented Code defined in [CCSDS] and repeated hereafter.

129.4.1 Numbering and naming conventions

Convention according to the CCSDS recommendations, applying to time structures:

- The most significant bit of an array is located to the left, carrying index number zero.
- An octet comprises eight bits.

*Table 1937.*CCSDS n-bit field definition

CCSDS n-bit field		
most significant		least significant
0	1 to n-2	n-1

Convention according to AMBA specification:

- The least significant bit of an array is located to the right, carrying index number zero.
- Big-endian support.

*Table 1938.*AMBA n-bit field definition

AMBA n-bit field		
most significant		least significant
n-1	n-2 down to 1	0

129.4.2 Reference documents

[CCSDS] Time Code Formats, CCSDS 301.0-B-4, www.ccsds.org

[SPW] Space engineering: SpaceWire - Links, nodes, routers and networks, ECSS-E-ST-50-12C

[PID] Space engineering: SpaceWire protocol identification, ECSS-E-ST-50-51C

[RMAP] Space engineering: SpaceWire - Remote memory access protocol, ECSS-E-ST-50-52C

129.4.3 CCSDS Unsegmented Code: Preamble Field (P-Field)

The time code preamble field (P-Field) may be either explicitly or implicitly conveyed. If it is implicitly conveyed (not present with T-Field), the code is not self-identified, and identification must be obtained by other means. As presently defined, the explicit representation of the P-Field is limited to one octet whose format is described hereafter.

*Table 1939.*CCSDS Unsegmented Code P-Field definition

Bit	Value		Interpretation
0	“1”		Extension flag, P-Field extended with 2nd octet
1 - 3	“001”	1958 January 1 epoch (Level 1)	Time code identification
	“010”	Agency-defined epoch (Level 2)	
4 - 5	“11”	(number of octets of coarse time) - 1	Detail bits for information on the code
6 - 7	“11”	(number of octets of fine time)	
8	“0”		Extension flag, P-Field not extended with 3rd octet
9-14	“000000”	Don’t care	Reserved for future use
15	“1”=Initialize,”0”=Synchronize		Initialization

Note: Revision 0 of the core used bit 8 for Initialize/Synchronize selection. Bit 15 is used from Revision 1 and forward, since bit 8 has the meaning of an extension flag for a third octet.

129.4.4 CCSDS Unsegmented Code: Time Field (T-Field)

For the unsegmented binary time codes described herein, the T-Field consists of a selected number of contiguous time elements, each element being one octet in length. An element represents the state of 8 consecutive bits of a binary counter, cascaded with the adjacent counters, which rolls over at a modulo of 256.

*Table 1940.*CCSDS Unsegmented Code T-Field definition

CCSDS Unsegmented Code									
Preamble Field	Time Field								
	Coarse time						Fine time		
-	2^{31} 2^{24}	2^{23} 2^{16}	2^{15} 2^{8}	2^{7} 2^{0}			2^{-1} 2^{-8}	2^{-9} 2^{-15}	2^{-16} 2^{-24}
0:15	0			31			32		55

The basic time unit is the second. The T-Field consists of 32 bits of coarse time (seconds) and 24 bits of fine time (sub seconds). The coarse time code elements are a count of the number of seconds elapsed from the epoch. The 32 bits of coarse time results in a maximum ambiguity period of approximately 136 years. Arbitrary epochs may be accommodated as a Level 2 code. The 24 bits of fine code elements result in a resolution of 2-24 second (about 60 nanoseconds). This code is not UTC-based and leap second corrections do not apply according to CCSDS.

129.5 Registers

The core is programmed through registers mapped into APB address space.

*Table 1941.*Registers

APB address offset	Register
0x00	Configuration Register
0x04	Status Register
0x08	Control Register
0x10	Destination Logical Address and Mask Register
0x14	Protocol Identifier Register
0x18	Offset Register
0x20	T-Field Coarse Time Packet Register
0x24	T-Field Fine Time Packet Register
0x28	P-Field Packet and CRC Packet Register
0x30	Elapsed Time Coarse Register
0x34	Elapsed Time Fine Register
0x38	Next Elapsed Time Coarse Register
0x3C	Next Elapsed Time Fine Register
0x60	Pending Interrupt Masked Status Register
0x64	Pending Interrupt Masked Register
0x68	Pending Interrupt Status Register
0x6C	Pending Interrupt Register
0x70	Interrupt Mask Register
0x74	Pending Interrupt Clear Register

129.5.1 Various T-Field Mappings

Table 1942. Various T-Field mappings

T-Field Coarse Time Registers (AMBA index numbering)																																T-Field Fine Time Registers (AMBA index numbering)																				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8
Binary Weights (2**n)																																																							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	-1	-2	-3	-4	-5	-6	-7	-8	-9	-10	-11	-12	-13	-14	-15	-16	-17	-18	-19	-20	-21	-22	-23	-24
Integer seconds																																*Fractions of seconds*																				
CCSDS T-Field Index (CCSDS index numbering)																																																				
0	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*	*11*	*12*	*13*	*14*	*15*	*16*	*17*	*18*	*19*	*20*	*21*	*22*	*23*	*24*	*25*	*26*	*27*	*28*	*29*	*30*	*31*	*32*	*33*	*34*	*35*	*36*	*37*	*38*	*39*	*40*	*41*	*42*	*43*	*44*	*45*	*46*	*47*	*48*	*49*	*50*	*51*	*52*	*53*	*54*	*55*
Time-Code Mapping (position of bit [0], with bits [5:1] positioned left-of)																																																				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																						
Tolerance Mapping (index of left-most ignored bit)																																																			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1																							
Offset Mapping																																																			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																						

129.5.2 Various T-Field Mappings - Example (Time-Codes at 64 Hz, CUCTP Packets at 1 Hz)

Table 1943. Various T-Field mappings - example (Time-Codes at 64 Hz, CUCTP packets at 1 Hz)

T-Field Coarse Time Registers (AMBA index numbering)																																T-Field Fine Time Registers (AMBA index numbering)																				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8
Binary Weights (2**n)																																																						
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	-1	-2	-3	-4	-5	-6	-7	-8	-9	-10	-11	-12	-13	-14	-15	-16	-17	-18	-19	-20	-21	-22	-23	-24
Integer seconds																																*Fractions of seconds*																				
CCSDS T-Field Index (CCSDS index numbering)																																																			
0	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*	*11*	*12*	*13*	*14*	*15*	*16*	*17*	*18*	*19*	*20*	*21*	*22*	*23*	*24*	*25*	*26*	*27*	*28*	*29*	*30*	*31*	*32*	*33*	*34*	*35*	*36*	*37*	*38*	*39*	*40*	*41*	*42*	*43*	*44*	*45*	*46*	*47*	*48*	*49*	*50*	*51*	*52*	*53*	*54*	*55*
Time-Code Mapping (position of bit [0], with bits [5:1] positioned left-of)																																																			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																						
											5	4	3	2	1	0																																					
Tolerance Mapping (index of left-most ignored bit)																																																			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1																							
																								-	-	-	-	-	-	-																							
Offset Mapping																																																			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																						
														0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-																						
														1	1	1	1	1	1	1	1	1	-	-	-	-	-	-	-	-																							
														0	0	0	0	0	0	0	0	0	1	-	-	-	-	-	-	-	-																						
														0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-																						

MAPPING = 18 Time-Code:

TOL = 8 Ignored bits:

OFFSET = 0x00000000 Late match:
Early match:

OFFSET = 0x00000123 Late match:
Early match:

129.5.3 Configuration Register

*Table 1944.*0x00 - CONF - Configuration Register

31 28	27 26	25 24	23 21	20 16	15 13	12 8	7	6 4	3 2	1	0
SELOUT	R	SELIN	R	MAPPING	R	TOL	R	TID	R	CTF	CP
0	0	0	0	*	0	*	0	0b001	0	0	0
rw	r	rw	r	rw	r	rw	r	rw	r	rw	rw

31: 28	SELOUT	Select output(s) for SpaceWire time-code transmission, index 3 downto 0.
27: 26	RESERVED	
25: 24	SELIN	Select input for SpaceWire time-code and packet reception, one of 0 through 3.
23: 21	RESERVED	
20: 16	MAPPING	Defines mapping of Time-Code time information versus T-Field: T-Field definition [0 to 55], where 0 is MSB and 55 is LSB, 0 corresponds to 2**31 seconds, and 55 corresponds to 2**-24 seconds. MAPPING= 0 corresponds to Time-Code[5] mapped to T-Field[50] and Time-Code[0] mapped to T-Field[55], MAPPING= 1 corresponds to Time-Code[5] mapped to T-Field[49] and Time-Code[0] mapped to T-Field[54], ... MAPPING=30 corresponds to Time-Code[5] mapped to T-Field[20] and Time-Code[0] mapped to T-Field[25]. MAPPING=31 corresponds to Time-Code[5] mapped to T-Field[19] and Time-Code[0] mapped to T-Field[24].
15: 13	RESERVED	
12: 8	TOL	Defines SpaceWire Time-Code reception tolerance: T-Field definition [0 to 55], where 0 is MSB and 55 is LSB, 0 corresponds to 2**31 seconds, and 55 corresponds to 2**-24 seconds. TOL= 0 corresponds to zero tolerance, TOL= 1 corresponds to T-Field[55] being ignored, TOL= 2 corresponds to T-Field[54:55] being ignored, ... TOL=30 corresponds to T-Field[26:55] being ignored, TOL=31 corresponds to T-Field[25:55] being ignored.
7	RESERVED	
6: 4	TID	Defines CUC P-Field Time Code Identification: “001” 1958 January 1 epoch (Level 1) “010” Agency-defined epoch (Level 2)
3: 2	RESERVED	
1	CTF	Check SpaceWire Time-Code control flags to be all zero when set.
0	CP	Check CUC P-Field Time Code Identification to match TID field when set.

Power-up default: depends on configuration

129.5.4 Status Register

*Table 1945.*0x04 - STAT - Status Register

31 11	10	9	8	7 6	5 0
RESERVED	FREEPKT	FREESYNC	INSYNC	TIMEFLAG	TIMEINFO
0	0	0	0	0	0
r	r	r	r	r	r

31: 11	RESERVED	
10	FREEPKT	Time freewheeling on packet level
9	FREESYNC	Time freewheeling on time-code level
8	INSYNC	Synchronous time reception of packets and time-codes
7: 6	TIMEFLAG	Received SpaceWire Time-Code Control Flags
5: 0	TIMEINFO	Received SpaceWire Time-Code Time Information

129.5.5 Control Register

*Table 1946.*0x08 - CTRL - Control Register

31 6	5	4	3	2	1	0
RESERVED	PKTRXEN	PKTINITEN	PKTSYNCEN	RXEN	TXEN	RESET
0	0	0	0	0	0	0
r	rw	rw	rw	rw	rw	rw

31: 6	RESERVED	
5	PKTRXEN	Enable SpaceWire CUC packet reception
4	PKTINITEN	Enable SpaceWire CUC packet initialization
3	PKTSYNCEN	Enable SpaceWire CUC packet synchronization
2	RXEN	Enable SpaceWire Time-Code reception
1	TXEN	Enable SpaceWire Time-Code transmission
0	RESET	Reset core

Power-up default: 0x00000000

129.5.6 Destination Logical Address and Mask Register

*Table 1947.*0x10 - DLA - Destination Logical Address and Mask Register

31 16	15 8	7 0
RESERVED	MASK	DLA
0	0	*
r	rw	rw

31: 16	RESERVED	
15: 8	MASK	Destination Logical Address Mask, ignore bit when set. Zero at reset.
7: 0	DLA	Destination Logical Address

Power-up default: configuration dependent

129.5.7 Protocol Identifier Register

*Table 1948.*0x14 - PIR - Protocol Identifier Register

31	8	7	0
RESERVED		PID	
0		*	
r		rw	

31: 8 RESERVED

7: 0 PID Protocol Identifier

Power-up default: configuration dependent

129.5.8 Offset Register

*Table 1949.*0x18 - OFFS - Offset Register

31	24	23	0
OFFSET			
0			
rw			

2^{7} 2^{0} 2^{-1} 2^{-24}

24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55

31: 0 OFFSET Packet reception offset: 0 corresponds to LSB of T-Field.

Power-up default: 0x00000000

129.5.9 T-Field Coarse Time Packet Register

*Table 1950.*0x20 - TCTP - T-Field Coarse Time Packet Register

31	0
T-Field, Coarse Time	
0	
rw	

2^{31} 2^{0}

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

31: 0 COARSE T-Field of received packet

129.5.10T-Field Fine Time Packet Register

*Table 1951.*0x24 - TFTP - T-Field Fine Time Packet Register

31	8	7	0
T-Field, Fine Time		RESERVED	
0		0	
rw		r	

2^{-1} 2^{-24}

32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55

31: 8 FINE T-Field of received packet

7: 0 RESERVED

129.5.11P-Field Packet and CRC Packet Register

*Table 1952.*0x28 - PPCP - P-Field Packet and CRC Packet Register

31	30	29	28 24	23 16	15 0
NEW	INIT	FORCE	R	CRC	P-Field
0	0	0	0	0	0
rw	rw	rw	r	rw	rw

b7 b6 b5 b4 b3 b2 b1 b0 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

31	NEW	New packet received
30	INIT	Initialization bit set in received packet
29	FORCE	Force packet initialization at once, one shot (mostly for debug)
28: 24	RESERVED	
23: 16	CRC	CRC of received packet
15: 0	P-Field	P-Field of received packet

129.5.12Elapsed Coarse Time Register

*Table 1953.*0x30 - ECT - Elapsed Coarse Time Register

31 0
T-Field, Coarse Time
*
r

2^{31} 2^{0}

31: 0	COARSE	T-Field of current time (latches Fine Time when read)

129.5.13Elapsed Fine Time Register

*Table 1954.*0x34 - EFT - Elapsed Fine Time Register

31 8	7 0
T-Field, Fine Time	RESERVED
0	0
r	r

2^{-1} 2^{-24}

31: 8	FINE	T-Field of current time
7: 0	RESERVED	

129.5.14Next Elapsed Coarse Time Packet Register

*Table 1955.*0x38 - NECT - Next Elapsed Coarse Time Packet Register

31 0
T-Field, Coarse Time
*
r

2^{31} 2^{0}

31: 0	COARSE	T-Field of next packet to be sent

129.5.15Next Elapsed Fine Time Packet Register

*Table 1956.*0x3C - NEFT - Next Elapsed Fine Time Packet Register

31	8	7	0
T-Field, Fine Time		RESERVED	
*		0	
r		r	
2^{-1}	2^{-24}		

31: 8	FINE	T-Field of next packet to be sent
7: 0	RESERVED	

129.5.16

Interrupt registers

The interrupt registers give complete freedom to the software, by providing means to mask interrupts, clear interrupts, force interrupts and read interrupt status.

When an interrupt occurs the corresponding bit in the Pending Interrupt Register is set. The normal sequence to initialize and handle a module interrupt is:

- Set up the software interrupt-handler to accept an interrupt from the module.
- Read the Pending Interrupt Register to clear any spurious interrupts.
- Initialize the Interrupt Mask Register, unmasking each bit that should generate the interrupt.
- When an interrupt occurs, read the Pending Interrupt Status Register in the software interrupt-handler to determine the causes of the interrupt.
- Handle the interrupt, taking into account all causes of the interrupt.
- Clear the handled interrupt using Pending Interrupt Clear Register.

Masking interrupts: After reset, all interrupt bits are masked, since the Interrupt Mask Register is zero. To enable generation of a module interrupt for an interrupt bit, set the corresponding bit in the Interrupt Mask Register.

Clearing interrupts: All bits of the Pending Interrupt Register are cleared when it is read or when the Pending Interrupt Masked Register is read. Reading the Pending Interrupt Masked Register yields the contents of the Pending Interrupt Register masked with the contents of the Interrupt Mask Register. Selected bits can be cleared by writing ones to the bits that shall be cleared to the Pending Interrupt Clear Register.

Forcing interrupts: When the Pending Interrupt Register is written, the resulting value is the original contents of the register logically OR-ed with the write data. This means that writing the register can force (set) an interrupt bit, but never clear it.

Reading interrupt status: Reading the Pending Interrupt Status Register yields the same data as a read of the Pending Interrupt Register, but without clearing the contents.

Reading interrupt status of unmasked bits: Reading the Pending Interrupt Masked Status Register yields the contents of the Pending Interrupt Register masked with the contents of the Interrupt Mask Register, but without clearing the contents.

The interrupt registers comprise the following:

*Table 1957.*Interrupt registers

Description	Name	Mode
Pending Interrupt Masked Status Register	SPWCUCPIMSR	r
Pending Interrupt Masked Register	SPWCUCPIMR	r
Pending Interrupt Status Register	SPWCUCPISR	r
Pending Interrupt Register	SPWCUCPIR	w
Interrupt Mask Register	SPWCUCIMR	w
Pending Interrupt Clear Register	SPWCUCPICR	w

*Table 1958.*Interrupt registers template

31 13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	TickTX	TickTx Wrap	TickRx	TickRx Wrap	TickRx Error	Toler-ance Error	Sync	Sync Error	Wrap	Wrap Error	Pkt Rx	Pkt Error	Pkt Init
	0	0	0	0	0	0	0	0	0	0	0	0	0
	*	*	*	*	*	*	*	*	*	*	*	*	*

31: 13	RESERVED	
12	TickTx	Time-code transmission, incrementing time information*
11	TickTxWrap	Time-code transmission, wrapping time information*
10	TickRx	Time-code reception, incrementing time information*
9	TickRxWrap	Time-code reception, wrapping time information*
8	TickRxError	Error in received time-code time information*
7	ToleranceError	Time-code reception timing outside tolerance with respect to local Elapsed Time*
6	Sync	Time-information synchronized correctly with respect to local Elapsed Time*
5	SyncError	Error in time-information synchronization with respect to local Elapsed Time*
4	Wrap	Packet synchronized correctly with respect to local Elapsed Time*
3	WrapError	Error in packet synchronization with respect to local Elapsed Time*
2	PktRx	Packet received correctly*
1	PktError	Error in received packet (e.g. CRC, P-Field, EEP, etc.)*
0	PktInit	Initialization of local Elapsed Time through received packet or forced access*
	All bits in all interrupt registers are reset to 0b after reset	

*See table 1957.

129.6 Vendor and device identifiers

The module has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x089. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

129.7 Implementation

129.7.1 Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

129.8 Configuration options

Table 1959 shows the configuration options of the core (VHDL generics).

*Table 1959.*Configuration options

Generic name	Function	Allowed range	Default
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	Addr field of the APB bar.	0 - 16#FFF#	0
pmask	Mask field of the APB bar.	0 - 16#FFF#	16#FFF#
pirq	Interrupt line used by the core.	0 - NAHBIRQ-1	0
dlareset	Destination Logical Address reset value	0-255	254
pidreset	Protocol Identifier reset value	0-255	254
mapreset	Index of least significant bit for mapping in SpaceWire Time-Code Time information. LSB is marked as 0.	0-31	18
tolreset	Number of least significant bits that tolerate errors. LSB is marked as 1, whereas 0 allows no tolerance.	0-31	8

129.9 Signal descriptions

Table 1960 shows the interface signals of the core (VHDL ports).

*Table 1960.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
CUCI	TickInDone	Input	SpaceWire Time-Code input processed	High
	TickOutRaw		SpaceWire Time-Code output event	High
	TimeOut[7:0]		SpaceWire Time-Code output	-
	RxDAv		SpaceWire character event	High
	RxDataOut[8:0]		SpaceWire character	-
	ElapsedTime[0:55]		Elapsed Time	
	ElapsedNext[0:55]		Next Elapsed Time	
	ElapsedEvent		Elapsed Time counter event	High
	ElapsedSync		Elapsed Time counter synchronization event	High
CUCO	TickInRaw	Output	SpaceWire Time-Code input request	High
	TimeIn[7:0]		SpaceWire Time-Code input	-
	ExternalTime[0:55]		External Elapsed Time input	-
	ExternalSync		External Elapsed Time input synchronization	High

* see GRLIB IP Library User's Manual

129.10 Signal definitions and reset values

The core has no external signals.

129.11 Timing

The core has no external timing.

129.12 Library dependencies

Table 1961 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1961.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
TMTC	SPACEWIRECUC	Signals, component	Component declarations, signals.

130 GRPW - PacketWire Interface

The *PacketWire to AMBA AHB Interface* (GRPW) comprises a bi-directional PacketWire link and an AMBA AHB master interface. The purpose of the interface is to allow read and write accesses on an AMBA AHB bus to be initiated from the PacketWire interface. The protocol allows single or multiple reads per command, each command specifying a read or write access, the number of word transfers and the starting address. For a write access, word oriented data is transmitted to the interface, and for read accesses word oriented data is received from the interface.

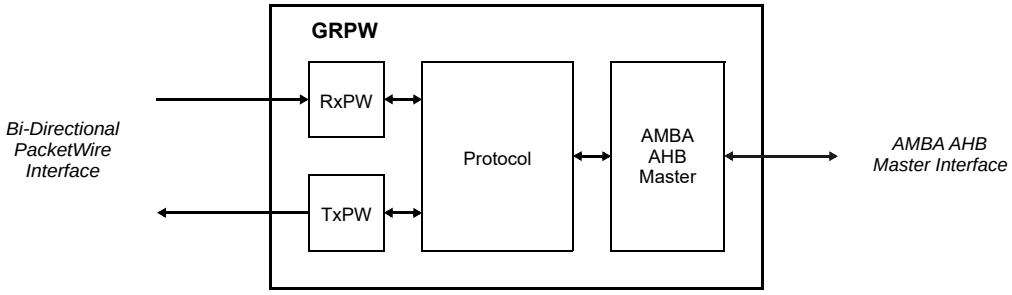


Figure 325. Block diagram

In a typical application, the PacketWire interface would be used as a remote control interface of a System-On-a-Chip device based around the AMBA AHB bus. An example could be a Packet Telemetry and Telecommand device which can be controlled remotely from a processor board via a PacketWire link. The link would provide both the capability to read and write registers, and to make block transfers to and from the target device and its memories.

This interface is based on the de facto standard PacketWire interface used by the *European Space Agency* (ESA). At the time of writing there were no relevant documents available from the *European Cooperation for Space Standardization* (ECSS).

130.1 Operation

130.1.1 Protocol

The communication protocol is based on the protocol used in the LEON processor. Commands are sent to the interface as messages over the bi-directional PacketWire interface. The protocol allows read and write accesses, as shown in table 1962. For each command, the number of 32-bit words to be transferred are specified, ranging from 1 to 64 words. For each command access, a 32-bit starting byte address is specified.

All transfers are assumed to be word aligned, effectively ignoring the two least significant bits of the address, assuming them to be both zero. There are no restrictions on the address, allowing a wrap around at the end of the address space during a transfer. The start address can thus be set to any position in the address space. The address is automatically incremented by 4 after each word access during

a transfer. The address and data bit numbering in table 1962 correspond to the AMBA AHB bit numbering conventions.

*Table 1962.*Protocol on PacketWire side

	Control	**Address**				**Data**												
						first word				**second word**				**...**	**last word**			
Cmd	Write																	
Octet	0	1	2	3	4	5	6	7	8	9	10	11	12	...	n-4	n-3	n-2	n-1
Send	11_b Length-1	31:24	23:16	15:8	7:0	31:24	23:16	15:8	7:0	31:24	23:16	15:8	7:0	...	31:24	23:16	15:8	7:0
Byte						0	1	2	3	4	5	6	7	...	n-4	n-3	n-2	n-1
Receive																		
Cmd	Read																	
Octet	0	1	2	3	4	5	6	7	8	9	10	11	12	...	n-4	n-3	n-2	n-1
Send	10_b Length-1	31:24	23:16	15:8	7:0													
Byte						0	1	2	3	4	5	6	7	...	n-4	n-3	n-2	n-1
Receive						31:24	23:16	15:8	7:0	31:24	23:16	15:8	7:0	...	31:24	23:16	15:8	7:0

130.1.2 Bi-directional PacketWire interface

The bi-directional PacketWire interface comprises two PacketWire links, one in each direction, the PacketWire input link and the PacketWire output link. Each link comprises three ports for transmitting the message delimiter, the bit clock and the serial bit data. Each link also comprises an additional port for busy signalling, indicating when the receiver is ready to receive the next octet.

The interface accepts and generates the waveform format shown in figure 326.

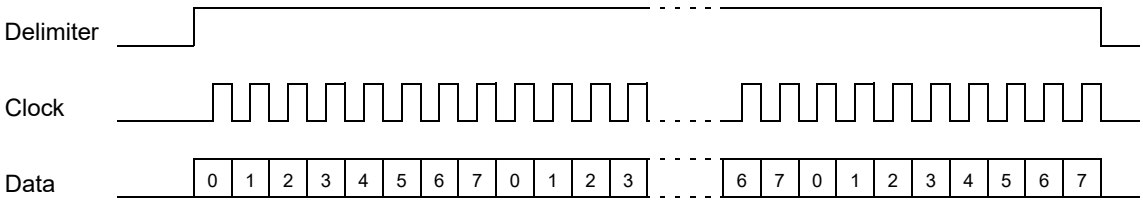


Figure 326. Synchronous bit serial waveform

The PacketWire protocol follows the CCSDS transmission convention, the most significant bit being sent first, both for octet transfers (control), and for word transfer (address or data). Transmitted data should consist of multiples of eight bits otherwise the last bits will be lost. The input message delimiter port is used to delimit messages (commands). It should be asserted while a message is being input, and deasserted in between. In addition, the message delimiter port should define the octet boundaries in the data stream, the first octet explicitly and the following octets each subsequent eight bit clock cycles.

The maximum receiving input baud rate is defined as twice the frequency of the system clock input (f_{HCLK}). The maximum receiving throughput is limited by the AMBA AHB system into which this core is integrated. There is no lower limit for the input baud rate in the receiver. Note however that there are constraints on the input baud rate related to the automatic baud rate detection, as described hereafter.

The output baud rate is automatically adjusted to the incoming baud rate, provided that the incoming baud rate is less than half the frequency of the system clock input (f_{HCLK}). The lower limit for the input baud rate detection is $f_{HCLK}/512$. If the input baud rate is less than this limit, the output baud rate will equal $f_{HCLK}/512$. The input baud rate is determined by measuring the width of the logical one phase of the input bit clock.

The handshaking between the PacketWire links and the interface is implemented with busy ports, one in each direction. When a message is sent, the busy signal on the PacketWire input link will be asserted as soon as the first data bit is detected, it will then be deasserted as soon as the interface is ready to receive the next octet. This gives the transmitter ample time to stop transmitting after the completion of the first octet and wait for the busy signal deassertion before starting the transmission of the next octet. The handshaking is continued through out the message. At the end of message, the busy signal will be asserted until the completion of the message. For a write command, the busy signal will be deasserted after the completion of the AMBA AHB write access of the last word. For a read command, the busy signal will be deasserted after the completion of the AMBA AHB read access of the last word and its transmission on the PacketWire output link. It is therefore not possible for the external transmitter to send a new command until the previous has been completed.

Illegal commands are prevented from being executed. An illegal command is defined as a control octet for which the two most significant bits are neither 11_b nor 10_b. No accesses to the AMBA AHB bus will be performed and no response will be generated on the PacketWire link for a read command. A new command will be accepted as soon as the input message delimiter has been deasserted and a new command is transmitted.

A command can be aborted by prematurely deasserting the message delimiter on the PacketWire input link. This can be done at any point of the message, e.g. during the control octet, during the address or during the data transfer for write accesses. An aborted message will immediately terminate the access on the AMBA AHB bus. Note that it is not possible to predict whether or not the last word write access to the AMBA AHB bus has been completed or not in the case the message is aborted.

It is not possible to determine whether or not an access has been successfully completed on the AMBA AHB bus. For read accesses, a data response will be generated on the PacketWire output link independently of whether the AMBA AHB access was terminated with an *OKAY* or *ERROR*.

In the case an AMBA AHB access is not terminated because of indefinite *RETRY* or *SPLIT* responses, the command will not be completed and the busy port on the PacketWire input link will not be deasserted. This locked state can be observed by monitoring the response on the PacketWire input link, for which the busy signal will not be deasserted. For read accesses, this locked state can also determine if no data is received on the PacketWire output link. To overcome this locked stated, the message delimiter should be firstly deasserted on the PacketWire input linked. The message delimiter should then be asserted and a new control octet should then be transmitted, even though the busy port is asserted on the PacketWire input link. This action will abort any AMBA AHB accesses and restore the state of the interface. The newly started message should then be completed using the handshake method previously described. Note that it is not possible to determine at what time instant the abort will occur, possibly ruining the on going access. This is however acceptable considering being a recovery from a locked state.

130.1.3 AMBA AHB master interface

The AMBA AHB master interface has been reduced in functionality to support only what is required for the core. The following AMBA AHB features are constrained:

- only generates ***HSIZE*** = *HSIZE_WORD*
- only generates ***HLOCK*** = 0_b
- only generates ***HPROT*** = 0000_b
- only generates ***HBURST*** = *HBURST_SINGLE*
- never generates ***HTRANS*** = *HTRANS_BUSY*
- both ***HRESP*** = *HRESP_OKAY* and ***HRESP*** = *HRESP_ERROR* are treated as a successfully completed access
- both ***HRESP*** = *HRESP_RETRY* and ***HRESP*** = *HRESP_SPLIT* will result in a rescheduling the previous access until terminated with *HRESP_OKAY* or *HRESP_ERROR*

- only big-endianness is supported

The interface can act as a default AHB master generating idle accesses when required. It only implements a single word access at a time, without bursts, to reduce complexity for retry and split handling, and not requiring the 1024 byte boundary imposed by the AMBA specification on burst transfers to be taken into account.

130.1.4 Advanced Microcontroller Bus Architecture

Convention according to the Advanced Microcontroller Bus Architecture (AMBA) Specification, applying to the AHB and APB interfaces:

- Signal and port names are in upper case, except for the following:
- A lower case '*n*' in the name indicates that the signal or port is active low.
- Constant names are in upper case.
- The *least* significant bit of an array is located to the *right*, carrying index number zero.

*Table 1963.*AMBA n-bit field definition

AMBA n-bit field		
most significant		least significant
n-1	n-2 down to 1	0

130.1.5 Consultative Committee for Space Data Systems

Convention according to the Consultative Committee for Space Data Systems (CCSDS) recommendations, applying to all relevant structures:

- The *most* significant bit of an array is located to the *left*, carrying index number zero, and is transmitted first.
- An octet comprises eight bits.

General convention, applying to signals, ports and interfaces:

- Signal or port names are in mixed case.
- An upper case '*_N*' suffix in the name indicates that the signal or port is active low.

*Table 1964.*CCSDS n-bit field definition

CCSDS n-bit field		
most significant		least significant
0	1 to n-2	n-1

130.2 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x032. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

130.3 Configuration options

Table 1965 shows the configuration options of the core (VHDL generics).

*Table 1965.*Configuration options

Generic name	Function	Allowed range	Default
hindex	AHB master index	0 - NAHBMST-1	0
syncreset	Synchronous reset when set, else asynchronous	0 - 1	0

130.4 Signal descriptions

Table 1966 shows the interface signals of the core (VHDL ports).

*Table 1966.*Signal descriptions

Signal name	Field	Type	Function	Comment	Active
HRESETn	N/A	Input	Reset		Low
HCLK	N/A	Input	Clock		-
PWI	VALID	Input	Delimiter	This input port is the message delimiter for the input interface. It should be deasserted between messages	High
	CLOCK		Bit clock	This input port is the PacketWire bit clock. The receiver registers are clocked on the rising ***PWI.Clk*** edge.	Rising
	DATA		Data	This input port is the serial data input for the interface. Data are sampled on the rising ***PWI.Clk*** edge when ***PWI.Valid*** is asserted.	-
	BUSY_N		Not ready for octet	This input port indicates whether the receiver is ready to receive one octet. The input is considered as asynchronous.	Low
PWO	VALID	Output	Delimiter	This output port is the packet delimiter for the output interface. It is deasserted between packets. The output is clocked out on the rising ***HCLK*** edge.	High
	CLOCK		Bit clock	This output port is the PackeWire output bit clock. The output is clocked out on the rising ***HCLK*** edge.	Rising
	DATA		Data	This output port is the serial data output for the interface. The output is clocked out on the rising ***HCLK*** edge.	-
	BUSY_N		Not ready for octet	This port indicates whether the receiver is ready to receive one octet. The output is clocked out on the rising ***HCLK*** edge.	Low
AHBI	*	Input	AMB master input signals		-
AHBO	*	Output	AHB master output signals		-

* see GRLIB IP Library User's Manual

130.5 Signal definitions and reset values

The signals and their reset values are described in table 1967.

*Table 1967.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
pwi_valid	Input	Delimiter	High	-
pwi_clock	Input	Bit clock	Rising	-
pwi_data	Input	Data	-	-
pwo_busy_n	Output	Not ready for octet	Low	Logical 0
pwo_valid	Output	Delimiter	High	Logical 0
pwo_clock	Output	Bit clock	Rising	Logical 0
pwo_data	Output	Data	-	Logical 0
pwi_busy_n	Input	Not ready for octet	Low	-

130.6 Timing

The timing waveforms and timing parameters are shown in figure 327 and are defined in table 1968.

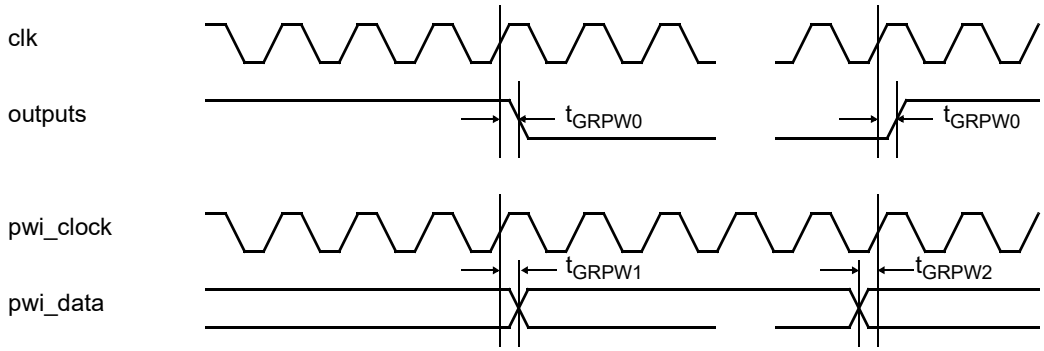


Figure 327. Timing waveforms

*Table 1968.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
t_{GRPW0}	clock to output delay	rising *clk* edge	TBD	TBD	ns
t_{GRPW1}	input to clock hold	rising *pwi_clock* edge	TBD	-	ns
t_{GRPW2}	input to clock setup	rising *pwi_clock* edge	TBD	-	ns
t_{GRPW3}	pwi_valid to pwi_clock edge	rising *pwi_clock* edge	TBD	-	ns
t_{GRPW3}	pwi_valid de-asserted period	-	TBD*t_{CLK}		periods

Note: The *pwi_busy_n* input is re-synchronized inside the core. The signal does not have to meet any setup or hold requirements.

130.7 Library dependencies

Table 1969 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1969.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
TMTC	TMTC_Types	Signals, component	Component declaration

130.8 Instantiation

The core is an almost fully synchronous design based on a single system clock strategy. The asynchronous part is related to the PacketWire (PW) input interface, for which the receiving shift register is implemented as a separate clock domain. All signals going between clock domains are clocked twice before being used to reduce the risk for metastability.

All registers in the core are reset asynchronously. The reset input can be asserted asynchronously, but requires synchronous deassertion to avoid any recovery time violations.

The ***PWI.Valid*** input should be deasserted for at least 4 ***HCLK*** clock periods between messages. The ***PWI.Data*** input is clocked into a receiving shift register on the rising ***PWI.Clk*** edge. The ***PWI.Clk*** input should have a 50% duty cycle.

The ***PWI.Busy_N*** should be asserted as soon as possible by the receiver, allowing the transmitter to halt the transmission between octets. The input is synchronised using two registers clocked on the rising ***HCLK*** edge.

This example shows how the core can be instantiated.

```
library  IEEE;
use      IEEE.Std_Logic_1164.all;
library  GRLIB;
use      GRLIB.AMBA.all;
library  TMTC;
use      TMTC.TMTC_Types.all;
..
   component GRPW is
      generic(
         hindex:           in    Integer := 0);
      port(
         -- AMBA AHB System Signals
         HCLK:             in    Std_ULogic; -- system clock
         HRESETn:          in    Std_ULogic; -- synchronised reset
         -- AMBA AHB Master Interface
         AHBOut:           out   AHB_Mst_Out_Type;
         AHBIn:            in    AHB_Mst_In_Type;
         -- PacketWire interface
         PWI:              in    GRPW_In_Type;
         PWO:              out   GRPW_Out_Type);
   end component GRPW;
```

131 GRPWRX - PacketWire Receiver

131.1 Overview

The PacketWire Receiver implements a receiver function with Direct Memory Access (DMA) support. Packets (or blocks of data, normally CCSDS Space Packets) are automatically stored to memory, for which the user configures a descriptor table with descriptors that point to each individual packet or one or more packets stored in a fixed length fields (framing mode).

The core provides the following external and internal interfaces:

- Packet Wire interface (serial bit data, bit clock, packet delimiter, abort, ready, busy)
- AMBA AHB master interface, with sideband signals as per [GRLIB]
- AMBA APB slave interface, with sideband signals as per [GRLIB]

The operation of the receiver is highly programmable by means of control registers.

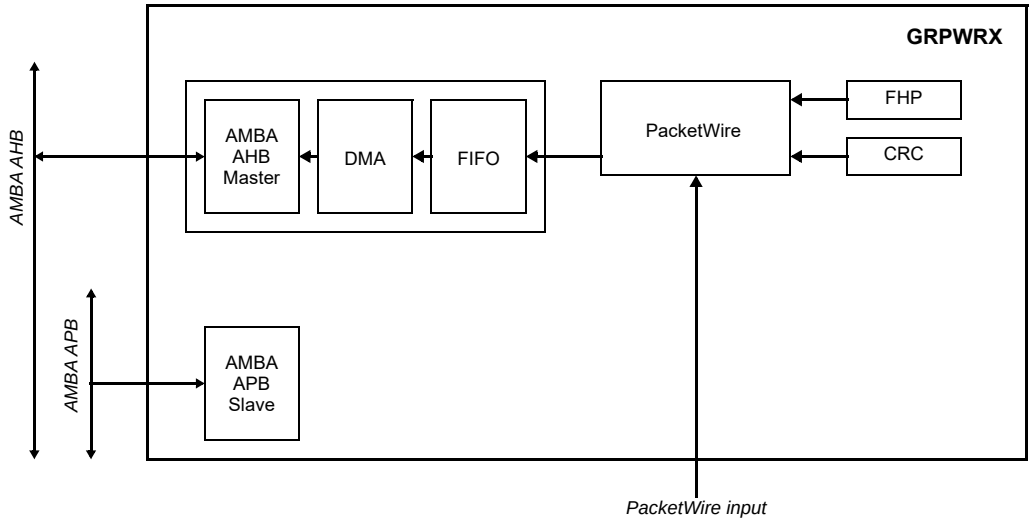


Figure 328. Block diagram

131.2 PacketWire interface

A PacketWire link comprises four ports for transmitting the message delimiter, the bit clock, the serial bit data and an abort signal. A link also comprises additional ports for busy signalling, indicating when the receiver is ready to receive the next octet, and for ready signalling, indicating that the receiver is ready to receive a complete packet. The waveform format shown in figure 329.

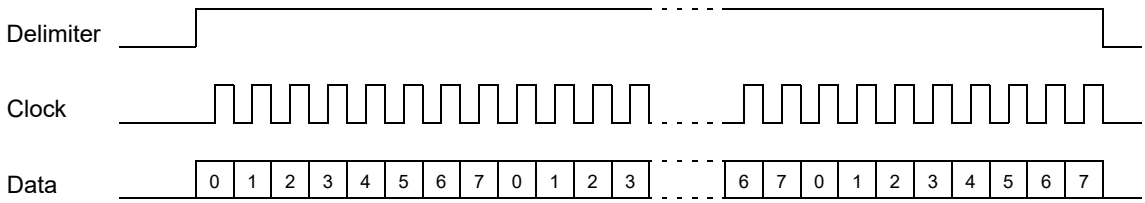


Figure 329. Synchronous bit serial waveform

The PacketWire protocol follows the CCSDS transmission convention, the most significant bit being sent first, both for octet transfers (control), and for word transfer (address or data). Transmitted data

should consist of multiples of eight bits otherwise the last bits will be lost. The message delimiter port is used to delimit messages (commands). It should be asserted while a message is being input, and deasserted in between. In addition, the message delimiter should define the octet boundaries in the data stream, the first octet explicitly and the following octets each subsequent eight bit clock cycles. The delimiter should be de-asserted for at least eight bit periods between messages.

The handshaking between the PacketWire link and the interface is implemented with a busy port. When a message is sent, the busy signal on the PacketWire link will be asserted as soon as the first data bit is detected, it will then be deasserted as soon as the interface is ready to receive the next octet. This gives the transmitter ample time to stop transmitting after the completion of the first octet and wait for the busy signal deassertion before starting the transmission of the next octet. The handshaking is continued through out the message. At the end of message, the busy signal will be asserted until the completion of the message.

131.3 Operation

131.3.1 Introduction

The DMA interface provides a means for the user to receive blocks of data of arbitrary length (maximum 65535 bytes), normally these are packet structures such as CCSDS Space Packets. It also supports reception of one or more blocks of data into a fixed length field such as a CCSDS Telemetry Transfer Frame Data Field (framing mode).

131.3.2 Descriptor setup

The DMA interface is used for receiving data. The reception is done using descriptors located in memory. A single descriptor is shown in tables 1970 through 1971. The address field of the descriptor should point to the start of where the received data is to be stored. The address need not be word-aligned. If the interrupt enable (IE) bit is set, an interrupt will be generated when the transfer has completed (this requires that the interrupt enable bit in the control register is also set). The interrupt will be generated regardless of whether the transfer was successful or not. The wrap (WR) bit is also a control bit that should be set before reception and it will be explained later in this section.

*Table 1970.*GRPWRX descriptor word 0 (address offset 0x0)

31 16	15 9	8	7	6 4	3	2	1	0
LEN	RESERVED	CERR	OV	RESERVED	FHP	WR	IE	EN

31: 16	(LEN) - Length in bytes (note that length is limited to 2048 bytes for framing mode) In packet mode, the LEN field is written by the hardware after the reception. In framing mode, the LEN field is written by the software before reception.
15: 9	RESERVED
8:	Cyclic Redundancy Code Error (CERR) - (read only) Set to one when a CRC error was detected in a packet (speculative, only useful if CRC is present in received packet)
7:	Overrun (OV) - (read only) Overrun detected during transmission.
6: 3	RESERVED
3:	First Header Pointer (FHP) - First Header Pointer to be stored (2 bytes)
2:	Wrap (WR) - Set to one to make the descriptor pointer wrap to zero after this descriptor has been used. If this bit is not set the pointer will increment by 16. The pointer automatically wraps to zero when the 16 kB boundary of the descriptor table is reached.
1:	Interrupt Enable (IE) - an interrupt will be generated when data for this descriptor has been received provided that the receive interrupt enable bit in the control register is set. The interrupt is generated regardless if the data was transferred successfully or if it terminated with an error.
0:	Enable (EN) - Set to one to enable the descriptor. Should always be set last of all the descriptor fields.

*Table 1971.*GRPWRX descriptor word 1 (address offset 0x4)

31	0
ADDRESS	

31: 0 Address (ADDRESS) - Pointer to the buffer area to where data will be stored.

To enable a descriptor the enable (EN) bit should be set and after this is done, the descriptor should not be touched until the enable bit has been cleared by the core.

131.3.3 Packet mode

In packet mode, each descriptor corresponds to one received packet. The maximum length of a packet can be 65535 bytes. There is no check for too long packets. Reception of any too long packet will result in indeterministic behavior. The length of the received packet is automatically written into descriptor word 0.

131.3.4 Framing mode

In framing mode, each pair of descriptors correspond to one fixed length field as the CCSDS Telemetry Transfer Frame Data Field. The first descriptor defines the length (fixed for a field) and position in memory where the data is to be stored. The second descriptor in a pair defines the fixed length (2 bytes) and position of the memory where the First Header Pointer (FHP) calculated for the data received in a field belonging to the previous descriptor is to be stored. The First Header Pointer is calculated according to CCSDS: if the first packet starts at the beginning of the field then it is all zeros, if no packet starts in the field then it is all ones, any other location of the start of the first packet in a field is its count from the start of the field minus one. The First Header Pointer write-back is enabled by setting the FHP bit in the descriptor word 0. Normally the start location of First Header Pointer is two bytes in front of the field when CCSDS Telemetry Transfer Frames are used.

131.3.5 Starting transmission

Enabling a descriptor is not enough to start transmission. A pointer to the memory area holding the descriptors must first be set in the core. This is done in the descriptor pointer register. The address must be aligned to a 16 kByte boundary. Bits 31 to 14 hold the base address of descriptor area while bits 13 to 4 form a pointer to an individual descriptor. The first descriptor should be located at the base address and when it has been used by the core, the pointer field is incremented by 16 to point at the next descriptor. The pointer will automatically wrap back to zero when the next 16 kByte boundary has been reached. The WR bit in the descriptors can be set to make the pointer wrap back to zero before the 16 kByte boundary.

The pointer field has also been made writable for maximum flexibility but care should be taken when writing to the descriptor pointer register. It should never be touched when reception is active.

The final step to activate the reception is to set the enable bit in the DMA control register. This tells the core that there are more active descriptors in the descriptor table. This bit should always be set when new descriptors are enabled, even if transmission is already active. The descriptors must always be enabled before the transmission enable bit is set.

131.3.6 Descriptor handling after transmission

When the reception of a packet (or field in framing mode) has finished, status is written to the first word in the corresponding descriptor, while the second word is left untouched. The other bits in the first descriptor word are set to zero after reception. The enable bit should be used as the indicator when a descriptor can be used again, which is when it has been cleared by the core.

If the Cyclic Redundancy Code (CRC) bit is set, a CRC calculated over all but the two last octets, will be checked and the results stored in the descriptor. The CRC is defined in CCSDS 132.0-B-1. This is not supported in framing mode.

There are multiple bits in the DMA status register that hold status information.

The Receiver Interrupt (RI) bit is set each time a DMA reception ended successfully. The Receiver Error (RE) bit is set each time an DMA reception ended with an error. For either event, an interrupt is generated for transfers for which the Interrupt Enable (IE) was set in the descriptor. The interrupt is maskable with the Interrupt Enable (IE) bit in the control register.

The Receiver AMBA error (RA) bit is set when an AMBA AHB error was encountered either when reading a descriptor or when writing data. Any active reception was aborted and the DMA channel was disabled. It is recommended that the receiver is reset after an AMBA AHB error. The interrupt is maskable with the Interrupt Enable (IE) bit in the control register.

131.4 Registers

The core is programmed through registers mapped into APB address space.

*Table 1972.*GRPWRX registers

APB address offset	Register
0x00	GRPWRX DMA Control register
0x04	GRPWRX DMA Status register
0x08	GRPWRX DMA Descriptor Pointer register
0x80	GRPWRX Control register
0x84	GRPWRX Status register
0x88	GRPWRX Configuration register
0x8C	GRPWRX Physical Layer register

131.4.1 DMA Control Register

*Table 1973.*0x00 - DCR - DMA control register

31 2	1	0
RESERVED	IE	EN
0	0	0
r	rw	rw

31: 2 RESERVED

1: Interrupt Enable (IE) - enable interrupts RA, RI, and RE

0: Enable (EN) - enable DMA transfers

131.4.2 DMA Status Register

*Table 1974.*0x04 - DSR - DMA status register

31 4	3	2	1	0
RESERVED	ACTIVE	RA	RI	RE
0	NR	0	0	0
r	r	wc	wc	wc

31: 4 RESERVED

3: Active (ACTIVE) - DMA access ongoing

2: Receiver AMBA Error (RA) - DMA AMBA AHB error, cleared by writing a logical 1

1: Receiver Interrupt (RI) - DMA interrupt, cleared by writing a logical 1

0: Receiver Error (RE) - DMA receiver error, cleared by writing a logical 1

131.4.3 DMA Descriptor Pointer Register

Table 1975. 0x08 - DDP - DMA descriptor pointer register

31 14	13 4	3 0
BASE	INDEX	RESERVED
NR	NR	0
rw	rw	r

31: 14 Descriptor base (BASE) - base address of descriptor table

13: 4 Descriptor index (INDEX) - index of active descriptor in descriptor table

3: 0 Reserved - fixed to “0000”

131.4.4 Control Register

Table 1976. 0x80 - CTRL - control register

31 3	2	1	0
RESERVED	RST	RES	RxEN
0	0	1	0
r	r	r	r

31: 3 RESERVED

2: Reset (RST) - resets complete core

1: RESERVED

0: Receiver Enable (RxEN) - enables receiver (should be done after the complete configuration of the receiver)

131.4.5 Status Register

Table 1977. 0x84 - STAT - Status register

31 ... 3	2	1	0
RESERVED	VALID	BUSY	READY
0	0	1	0
r	r	r	r

31: 3 RESERVED

2: Packet valid delimiter (VALID) - External valid signal

1: Busy with octet (BUSY) - External busy signal

0: Ready for packet (READY) - External ready signal

131.4.6 Configuration Register

Table 1978. 0x88 - CONF - configuration register

31 ... 24	23 ... 8	7 ... 1	0
REVISION	FIFOSIZE	RESERVED	MODE
*	*	0	0
r	r	r	rw

31: 24 (REVISION) - Revision number (read-only)

23: 8 (FIFOSIZE) - FIFO size in bytes (read-only)

23: 1 RESERVED

0: (MODE) - Enable framing mode when set, else packet mode when cleared

131.4.7 Physical Layer Register

Table 1979. 0x8C - PLR - physical layer register

31 ... 20	19 ... 8	7	6	5	4	3 ... 0
HALFBAUD	RESERVED	BUSY POS	READY POS	VALID POS	CLK RISE	RESERVED
0	0	0	1	1	1	0
r	r	rw	rw	rw	rw	r

31: 20 (HALFBAUD) - Received clock rate division factor with respect to the system clock - 1. Corresponds to the high phase of the incoming PacketWire bit clock. (read only)

19: 8 RESERVED

7: (BUSYPOS) - Positive polarity of busy input signal

6: (READYPOS) - Positive polarity of ready input signal

5: (VALIDPOS) - Positive polarity of valid output signal

4: (CLKRISE) - Rising clock edge in the middle of the serial data bit

3: 0 RESERVED

131.5 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x08E. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

131.6 Configuration options

Table 1980 shows the configuration options of the core (VHDL generics).

*Table 1980.*Configuration options

Generic name	Function	Allowed range	Default
hindex	AHB master index	0 - NAHBMST-1	0
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	ADDR field of the APB BAR	0 - 16#FFF#	0
pmask	MASK field of the APB BAR	0 - 16#FFF#	16#FFF#
pirq	Interrupt line used by core	0 - NAHBIRQ-1	0
memtech	Memory technology	0 to NTECH	0
clktech	Clock buffer technology	0 to NTECH	0
buftype	Clock buffer type	TBD	0
burstlength	Sets the AHB burst length used by the core	-	16

131.7 Signal descriptions

Table 1981 shows the interface signals of the core (VHDL ports).

*Table 1981.*Signal descriptions

Signal name	Field	Type	Function		Active
RSTN	N/A	Input	Reset		Low
CLK	N/A	Input	Clock		-
APBI	*	Input	APB slave input signals		-
APBO	*	Output	APB slave output signals		-
AHBI	*	Input	AMB master input signals		-
AHBO	*	Output	AHB master output signals		-
PWO	BUSY_N	Output	Not ready for octet	Port indicates whether the receiver is ready to receive one octet. The port is considered asynchronous.	Programmable
	READY		Ready for packet	Port indicates whether the receiver is ready to receive one packet. The port is considered asynchronous.	Programmable
PWI	VALID	Input	Delimiter	Port is the packet delimiter for the output interface. It is deasserted between packets. The output is clocked out on the rising CLK edge.	Programmable
	CLK		Bit clock	Port is the PacketWire output bit clock. The output is clocked out on the rising CLK edge.	Programmable
	DATA		Data	Port is the serial data output for the interface. The output is clocked out on the rising CLK edge.	-
	ABORT		Abort	Port is clocked out on the rising CLK edge.	High

* see GRLIB IP Library User's Manual

131.8 Signal definitions and reset values

The signals and their reset values are described in table 1982.

*Table 1982.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
pwi_valid	Input	Delimiter	High	-
pwi_clock	Input	Bit clock	Rising	-
pwi_data	Input	Data	-	-
pwi_aboart	Input	Abort (fixed output)	High	-
pwo_busy_n	Output	Not ready for octet	Low	Logical 1
pwo_ready	Output	Ready for packet	High	Logical 0

131.9 Timing

The timing waveforms and timing parameters are shown in figure 330 and are defined in table 1983.

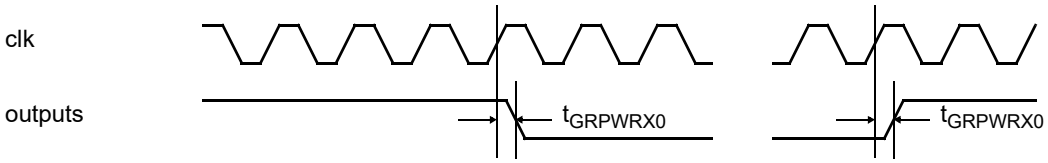


Figure 330. Timing waveforms

*Table 1983.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{GRPWRX0}$	clock to output delay	rising *clk* edge	TBD	TBD	ns

Note: The inputs are re-synchronized inside the core. The signals do not have to meet any setup or hold requirements.

131.10 Library dependencies

Table 1984 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1984.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
TMTC	TMTC_TYPES	Signals, component	Component declaration

132 GRPWTX - PacketWire Transmitter

132.1 Overview

The PacketWire Transmitter implements a transmit function with Direct Memory Access (DMA) suppport. Packets (or blocks of data, normally CCSDS Space Packets) are automatically fetched from memory, for which the user configures a descriptor table with descriptors that point to each individual packet.

The core provides the following external and internal interfaces:

- Packet Wire interface (serial bit data, bit clock, packet delimiter, abort, ready, busy)
- AMBA AHB master interface, with sideband signals as per [GRLIB]
- AMBA APB slave interface, with sideband signals as per [GRLIB]

The operation of the transmitter is highly programmable by means of control registers.

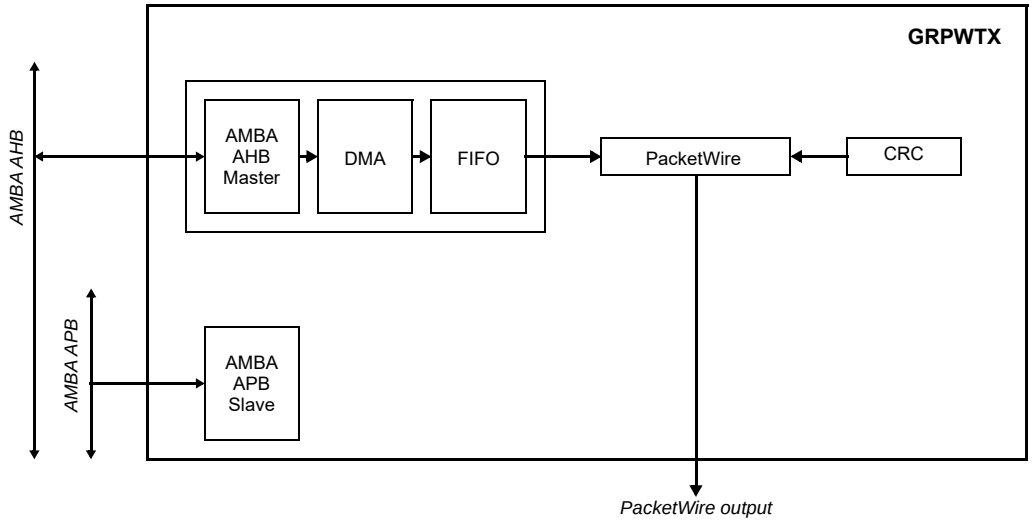


Figure 331. Block diagram

132.2 PacketWire interface

A PacketWire link comprises four ports for transmitting the message delimiter, the bit clock, the serial bit data and an abort signal. A link also comprises additional ports for busy signalling, indicating when the receiver is ready to receive the next octet, and for ready signalling, indicating that the receiver is ready to receive a complete packet. The waveform format shown in figure 332.

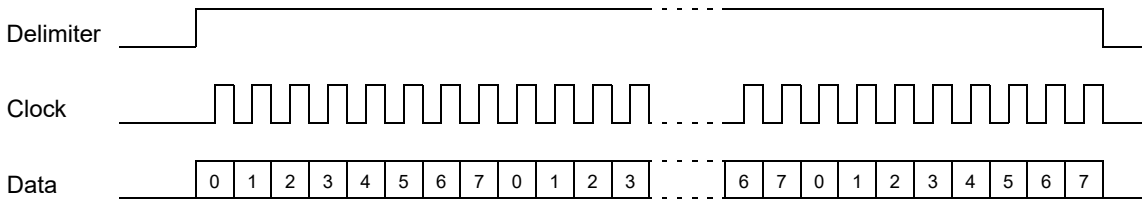


Figure 332. Synchronous bit serial waveform

The PacketWire protocol follows the CCSDS transmission convention, the most significant bit being sent first, both for octet transfers (control), and for word transfer (address or data). Transmitted data

should consist of multiples of eight bits otherwise the last bits will be lost. The message delimiter port is used to delimit messages (commands). It should be asserted while a message is being input, and deasserted in between. In addition, the message delimiter port should define the octet boundaries in the data stream, the first octet explicitly and the following octets each subsequent eight bit clock cycles.

The handshaking between the PacketWire link and the interface is implemented with a busy port. When a message is sent, the busy signal on the PacketWire link will be asserted as soon as the first data bit is detected, it will then be deasserted as soon as the interface is ready to receive the next octet. This gives the transmitter ample time to stop transmitting after the completion of the first octet and wait for the busy signal deassertion before starting the transmission of the next octet. The handshaking is continued through out the message. At the end of message, the busy signal will be asserted until the completion of the message.

132.3 Operation

132.3.1 Introduction

The DMA interface provides a means for the user to send blocks of data of arbitrary length, normally these are packet structures such as CCSDS Space Packets.

132.3.2 Descriptor setup

The DMA interface is used for sending data on the uplink. The transmission is done using descriptors located in memory. A single descriptor is shown in tables 1985 through 1986. The address field of the descriptor should point to the start of the data to be sent. The address need not be word-aligned. If the interrupt enable (IE) bit is set, an interrupt will be generated when the transfer has completed (this requires that the interrupt enable bit in the control register is also set). The interrupt will be generated regardless of whether the transfer was successful or not. The wrap (WR) bit is also a control bit that should be set before transmission and it will be explained later in this section.

*Table 1985.*GRPWTX descriptor word 0 (address offset 0x0)

31 16	15 8	7	6 4	3	2	1	0
LEN	RESERVED	UR	RESERVED	CRC	WR	IE	EN

31: 16	(LEN) - length in bytes
15: 8	RESERVED
7:	Underrun (UR) - Underrun detected during transmission.
6: 4	RESERVED
3:	Cyclic Redundancy Code (CRC) - Insert CRC, overwriting the two last octets of a data block
2:	Wrap (WR) - Set to one to make the descriptor pointer wrap to zero after this descriptor has been used. If this bit is not set the pointer will increment by 16. The pointer automatically wraps to zero when the 16 kB boundary of the descriptor table is reached.
1:	Interrupt Enable (IE) - an interrupt will be generated when the data from this descriptor has been sent provided that the transmitter interrupt enable bit in the control register is set. The interrupt is generated regardless if the data was transferred successfully or if it terminated with an error.
0:	Enable (EN) - Set to one to enable the descriptor. Should always be set last of all the descriptor fields.

*Table 1986.*GRPWTX descriptor word 1 (address offset 0x4)

31 0
ADDRESS

31: 0	Address (ADDRESS) - Pointer to the buffer area to where data will be fetched.

To enable a descriptor the enable (EN) bit should be set and after this is done, the descriptor should not be touched until the enable bit has been cleared by the core.

132.3.3 Starting transmission

Enabling a descriptor is not enough to start transmission. A pointer to the memory area holding the descriptors must first be set in the core. This is done in the descriptor pointer register. The address must be aligned to a 16 kByte boundary. Bits 31 to 14 hold the base address of descriptor area while bits 13 to 4 form a pointer to an individual descriptor. The first descriptor should be located at the base address and when it has been used by the core, the pointer field is incremented by 16 to point at the next descriptor. The pointer will automatically wrap back to zero when the next 16 kByte boundary has been reached. The WR bit in the descriptors can be set to make the pointer wrap back to zero before the 16 kByte boundary.

The pointer field has also been made writable for maximum flexibility but care should be taken when writing to the descriptor pointer register. It should never be touched when transmission is active.

If the Cyclic Redundancy Code (CRC) bit is set, a CRC calculated over all but the two last octets, will be inserted overwriting the two last octets of a data block. The CRC is defined in CCSDS 132.0-B-1.

The final step to activate the transmission is to set the enable bit in the DMA control register. This tells the core that there are more active descriptors in the descriptor table. This bit should always be set when new descriptors are enabled, even if transmission is already active. The descriptors must always be enabled before the transmission enable bit is set.

132.3.4 Descriptor handling after transmission

When the transmission has finished, status is written to the first word in the corresponding descriptor. The other bits in the first descriptor word are set to zero after transmission, while the second word is left untouched. The enable bit should be used as the indicator when a descriptor can be used again, which is when it has been cleared by the core.

There are multiple bits in the DMA status register that hold status information.

The Transmitter Interrupt (TI) bit is set each time a DMA transmission ended successfully. The Transmitter Error (TE) bit is set each time an DMA transmission ended with an error. For either event, an interrupt is generated for which the Interrupt Enable (IE) was set in the descriptor. The interrupt is maskable with the Interrupt Enable (IE) bit in the control register.

The Transmitter AMBA error (TA) bit is set when an AMBA AHB error was encountered either when reading a descriptor or data. Any active transmission was aborted and the DMA channel was disabled. It is recommended that the transmitter is reset after an AMBA AHB error. The interrupt is maskable with the Interrupt Enable (IE) bit in the control register.

132.4 Registers

The core is programmed through registers mapped into APB address space.

*Table 1987.*GRPWTX registers

APB address offset	Register
0x00	GRPWTX DMA Control register
0x04	GRPWTX DMA Status register
0x08	GRPWTX DMA Descriptor Pointer register
0x80	GRPWTX Control register
0x84	GRPWTX Status register
0x88	GRPWTX Configuration register
0x8C	GRPWTX Physical Layer register

132.4.1 DMA Control Register

*Table 1988.*0x00 - DCR - DMA control register

31	2	1	0
RESERVED		IE	EN
0		0	0
r		rw	rw

31: 2 RESERVED

1: Interrupt Enable (IE) - enable interrupts TA, TI, and TE

0: Enable (EN) - enable DMA transfers

132.4.2 DMA Status Register

*Table 1989.*0x04 - DSR - DMA status register

31	4	3	2	1	0
RESERVED		ACTIVE	TA	TI	TE

31: 4 RESERVED

3: Active (ACTIVE) - DMA access ongoing

2: Transmitter AMBA Error (TA) - DMA AMBA AHB error, cleared by writing a logical 1

1: Transmitter Interrupt (TI) - DMA interrupt, cleared by writing a logical 1

0: Transmitter Error (TE) - DMA transmitter error, cleared by writing a logical 1

132.4.3 DMA Descriptor Pointer Register

Table 1990. 0x08 - DDP - DMA descriptor pointer register

31	14	13	4	3	0
BASE		INDEX		RESERVED	
NR		NR		0	
rw		rw		r	

31: 14 Descriptor base (BASE) - base address of descriptor table

13: 4 Descriptor index (INDEX) - index of active descriptor in descriptor table

3: 0 Reserved - fixed to “0000”

132.4.4 Control Register

Table 1991. 0x80 - CTRL - control register

31	3	2	1	0
RESERVED		RST	R	TxEN
0		0	0	0
r		rw	r	rw

31: 3 RESERVED

2: Reset (RST) - resets complete core

1: RESERVED

0: Transmitter Enable (TxEN) - enables transmitter (should be done after the complete configuration of the transmitter)

132.4.5 Status Register

Table 1992. 0x84 - STAT - Status register (read-only)

31 … 2	1	0
RESERVED	BUSY	READY
0	1	0
r	r	r

31: 2 RESERVED

1: Busy with octet (BUSY) - External busy signal

0: Ready for packet (READY) - External ready signal

132.4.6 Configuration Register

Table 1993. 0x88 - CONF - configuration register (read-only)

31 … 24	23 … 8	7 … 0
REVISION	FIFOSIZE	RESERVED
*	*	0
r	r	r

31: 24 (REVISION) - Revision number (read-only)

23: 8 (FIFOSIZE) - FIFO size in bytes (read-only)

7: 0 RESERVED

132.4.7 Physical Layer Register

Table 1994. 0x8C - PLR - physical layer register

31 … 20	19 … 8	7	6	5	4	3	2 … 0
HALFBAUD	RESERVED	BUSY POS	READY POS	VALID POS	CLK RISE	CLK MODE	RESERVED
1	0	0	1	1	1	0	0
rw	r	rw	rw	rw	rw	rw	r

31: 20 (HALFBAUD) - System clock division factor (indicates the width of the high and low phases of the outgoing PacketWire bit clock in number of system clock periods -1)

19: 8 RESERVED

7: (BUSYPOS) - Positive polarity of busy input signal

6: (READYPOS) - Positive polarity of ready input signal

5: (VALIDPOS) - Positive polarity of valid output signal

4: (CLKRISE) - Rising clock edge in the middle of the serial data bit

3: (CLKMODE) - 0=when valid (default), 1=always (experimental)

2: 0 RESERVED

132.5 Vendor and device identifier

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x08D. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

132.6 Configuration options

Table 1995 shows the configuration options of the core (VHDL generics).

*Table 1995.*Configuration options

Generic name	Function	Allowed range	Default
hindex	AHB master index	0 - NAHBMST-1	0
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	ADDR field of the APB BAR	0 - 16#FFF#	0
pmask	MASK field of the APB BAR	0 - 16#FFF#	16#FFF#
pirq	Interrupt line used by core	0 - NAHBIRQ-1	0
memtech	Memory technology	0 to NTECH	0
burstlength	Sets the AHB burst length used by the core	-	16

132.7 Signal descriptions

Table 1996 shows the interface signals of the core (VHDL ports).

*Table 1996.*Signal descriptions

Signal name	Field	Type	Function		Active
RSTN	N/A	Input	Reset		Low
CLK	N/A	Input	Clock		-
APBI	*	Input	APB slave input signals		-
APBO	*	Output	APB slave output signals		-
AHBI	*	Input	AMB master input signals		-
AHBO	*	Output	AHB master output signals		-
PWI	BUSY_N	Input	Not ready for octet	Port indicates whether the receiver is ready to receive one octet. The port is considered asynchronous.	Programmable
	READY		Ready for packet	Port indicates whether the receiver is ready to receive one packet. The port is considered asynchronous.	Programmable
PWO	VALID	Output	Delimiter	Port is the packet delimiter for the output interface. It is deasserted between packets. The output is clocked out on the rising CLK edge.	Programmable
	CLK		Bit clock	Port is the PacketWire output bit clock. The output is clocked out on the rising CLK edge.	Programmable
	DATA		Data	Port is the serial data output for the interface. The output is clocked out on the rising CLK edge.	-
	ABORT		Abort	Port is clocked out on the rising CLK edge.	High

* see GRLIB IP Library User's Manual

132.8 Signal definitions and reset values

The signals and their reset values are described in table 1997.

*Table 1997.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
pwo_valid	Output	Delimiter	High	Logical 0
pwo_clock	Output	Bit clock	Rising	Logical 0
pwo_data	Output	Data	-	Logical 0
pwo_abort	Output	Abort (fixed output)	High	Logical 0
pwi_busy_n	Input	Not ready for octet	Low	-
pwi_ready	Input	Ready for packet	High	-

132.9 Timing

The timing waveforms and timing parameters are shown in figure 333 and are defined in table 1998.

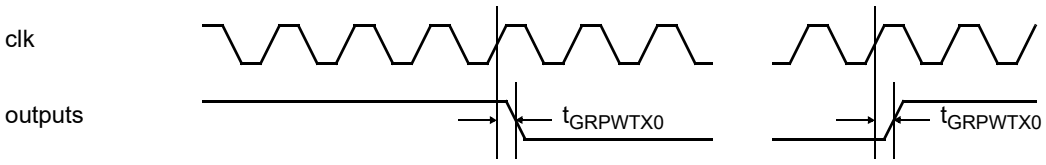


Figure 333. Timing waveforms

*Table 1998.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{GRPWTX0}$	clock to output delay	rising *clk* edge	TBD	TBD	ns

Note: The inputs are re-synchronized inside the core. The signals do not have to meet any setup or hold requirements.

132.10 Library dependencies

Table 1999 shows the libraries used when instantiating the core (VHDL libraries).

*Table 1999.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
TMTC	TMTC_TYPES	Signals, component	Component declaration

133 PW2APB - PacketWire receiver to AMBA APB Interface

133.1 Overview

The PacketWire to AMBA APB Interface implements the PacketWire protocol used by the Packet Telemetry Encoder (PTME) IP core and the Virtual Channel Assembler (VCA) device.

The core provides the following external and internal interfaces:

- Packet Wire interface (serial bit data, bit clock, packet delimiter, abort, ready, busy)
- AMBA APB slave interface, with sideband signals as per [GRLIB]

The core incorporates status and monitoring functions accessible via the AMBA APB slave interface. This includes:

- Valid and abort signalling from PacketWire interface
- Data overrun

Data is received on the PacketWire interface and read via the AMBA APB slave interface. It is possible to receive and read out one octet at a time.The packet delimiter and abort signals are observable via the control register, together with busy, ready and overrun signals. The baud rate is detected automatically and read via a configuration register.

133.2 PacketWire interface

A PacketWire link comprises four ports for transmitting the message delimiter, the bit clock, the serial bit data and an abort signal. A link also comprises additional ports for busy signalling, indicating when the receiver is ready to receive the next octet, and for ready signalling, indicating that the receiver is ready to receive a complete packet. The waveform format shown in figure 334.

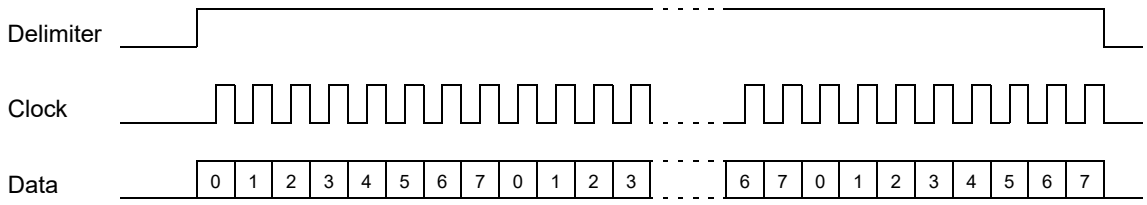


Figure 334. Synchronous bit serial waveform

The PacketWire protocol follows the CCSDS transmission convention, the most significant bit being sent first, both for octet transfers (control), and for word transfer (address or data). Transmitted data should consist of multiples of eight bits otherwise the last bits will be lost. The message delimiter port is used to delimit messages (commands). It should be asserted while a message is being input, and deasserted in between. In addition, the message delimiter port should define the octet boundaries in the data stream, the first octet explicitly and the following octets each subsequent eight bit clock cycles.

The maximum receiving input baud rate is defined as twice the frequency of the system clock input (f_{CLK}). The maximum receiving throughput is limited by the AMBA system into which this core is integrated. There is no lower limit for the input baud rate in the receiver.

The handshaking between the PacketWire link and the interface is implemented with a busy port. When a message is sent, the busy signal on the PacketWire link will be asserted as soon as the first data bit is detected, it will then be deasserted as soon as the interface is ready to receive the next octet. This gives the transmitter ample time to stop transmitting after the completion of the first octet and wait for the busy signal deassertion before starting the transmission of the next octet. The handshaking is continued through out the message.

To ensure that the receiver recognizes that the delimiter has been de-asserted, an application specific minimum time for the de-assertions should be imposed. Alternatively, ready signalling can be implemented in software, where the ready signal is asserted when the receiver software is ready to receive a packet, and is then immediately de-asserted when the first octet of a packet has been received. The transmitter software should thus only check the ready signal before starting to send a packet. This is illustrated in figure 335.

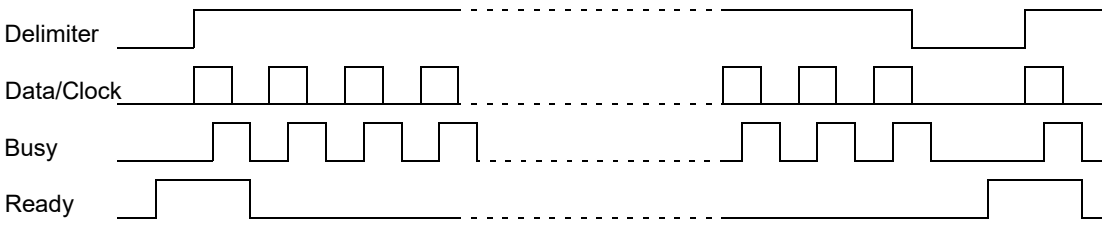


Figure 335. Handshake with ready signalling

To ensure that an abort is properly signalled, the abort signal should be de-asserted at the time the delimiter is asserted in the beginning of a packet, else the abort will be ignored. The abort signal should then be asserted while the delimiter is still asserted, to signal an abort to the receiver.

133.3 Registers

The core is programmed through registers mapped into APB address space.

*Table 2000.*PW2APB registers

APB address offset	Register
0x00	Control Register
0x04	Configuration Register
0x08	Data Reception Register

133.3.1 Control Register

*Table 2001.*0x00 - CTRL - Control Register

31 8	7	6	5	4	3	2	1 0
RESERVED	RESET	OV	READY	NEW	VALID	ABORT	SIZE
0	0	0	0	0	0	0	0
r	r	r	r	r	r	r	r

31: 8 RESERVED
- Write: Don't care.
- Read: All zero.

7 RESET
- Write: Write logical one to reset core
- Read: All zero

6 OV
- Write: Don't care.
- Read: Data input overrun, cleared on read.

  (Note that a received octet that results in an overrun does not overwrite the OCTET field.)

  (If there is a new octet available, as indicated by the NEW bit, it should be read out to free the receiver data reception register.)

5 READY
- Read/Write: Interface ready to receive a packet (only affects output signal)

4 NEW
- Write: Don't care.
- Read: Interface has received a new octet, ready for read-out (cleared when receiver data reception register has been read)

3 VALID
- Write: Don't care.
- Read: Packet delimiter when asserted (reflects input signal value)

2 ABORT
- Write: Don't care.
- Read: Abort current packet when asserted (only set when a valid abort takes place)

  (If there is a new octet available, as indicated by the NEW bit, it should be read to free the receiver data reception register.)

1: 0 SIZE — Reception size and order (left to right):
- Read/: `00 = 8 bit: 7:0`

133.3.2 Configuration Register

*Table 2002.*0x04 - CONF -Configuration Register

31 8	7 0
RESERVED	HALFBAUD
0	0
r	r

31: 8 RESERVED
- Write: Don't care.
- Read: All zero.

7: 0 HALFBAUD — System clock division factor (indicates the width of the high phase of the incoming PacketWire bit clock in number of system clock periods -1)
- Read:

```
0x00 = divide by 1
0xFF = divide by 256
```

133.3.3 Data Reception Register

*Table 2003.*0x08 - DRR - Data Reception Register

31 8	7 0
RESERVED	OCTET
0	0
r	rw

31: 8 RESERVED

Write: Don't care.

Read: All zero.

7: 0 OCTET

Write: Last octet correctly received. Note that a received octet that results in an overrun does not overwrite the OCTET field.

Read: All zero.

133.4 Vendor and device identifiers

The module has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x03C. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

133.5 Configuration options

Table 2004 shows the configuration options of the core (VHDL generics).

*Table 2004.*Configuration options

Generic name	Function	Allowed range	Default
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	Addr field of the APB bar.	0 - 16#FFF#	0
pmask	Mask field of the APB bar.	0 - 16#FFF#	16#FFC#
syncrst	Only synchronous reset	0, 1	1

133.6 Signal descriptions

Table 2005 shows the interface signals of the core (VHDL ports).

*Table 2005.*Signal descriptions

Signal name	Field	Type	Function		Active
RSTN	N/A	Input	Reset		Low
CLK	N/A	Input	Clock		-
APBI	*	Input	APB slave input signals		-
APBO	*	Output	APB slave output signals		-
PWO	BUSY_N	Input	Not ready for octet	This input port indicates whether the receiver is ready to receive one octet. The input is considered as asynchronous.	Low
	READY		Ready for packet	This input port indicates whether the receiver is ready to receive one packet. The input is considered as asynchronous.	High
PWI	VALID	Output	Delimiter	This output port is the packet delimiter for the output interface. It is deasserted between packets. The output is clocked out on the rising CLK edge.	High
	CLK		Bit clock	This output port is the PacketWire output bit clock. The output is clocked out on the rising CLK edge.	Rising
	DATA		Data	This output port is the serial data output for the interface. The output is clocked out on the rising CLK edge.	-
	ABORT		Abort	The output is clocked out on the rising CLK edge.	High

* see GRLIB IP Library User's Manual

133.7 Signal definitions and reset values

The signals and their reset values are described in table 2006.

*Table 2006.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
pwo_valid	Output	Delimiter	High	Logical 0
pwo_clock	Output	Bit clock	Rising	Logical 0
pwo_data	Output	Data	-	Logical 0
pwo_aboart	Output	Abort	High	Logical 0
pwi_busy_n	Input	Not ready for octet	Low	-
pwi_ready	Input	Ready for packet	High	-

133.8 Timing

The timing waveforms and timing parameters are shown in figure 336 and are defined in table 2007.

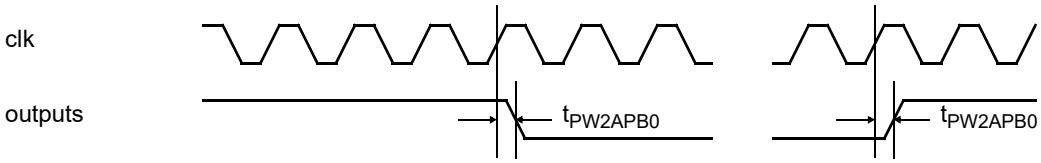


Figure 336. Timing waveforms

*Table 2007.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{PW2APB0}$	clock to output delay	rising *clk* edge	TBD	TBD	ns

Note: The inputs are re-synchronized inside the core. The signals do not have to meet any setup or hold requirements.

133.9 Library dependencies

Table 2008 shows the libraries used when instantiating the core (VHDL libraries).

*Table 2008.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
TMTC	TMTC_Types	Signals, component	Component declarations, signals.

134 APB2PW - AMBA APB to PacketWire Transmitter Interface

134.1 Overview

The AMBA APB to PacketWire Interface implements the PacketWire protocol used by the Packet Telemetry Encoder (PTME) IP core and the Virtual Channel Assembler (VCA) device.

The core provides the following external and internal interfaces:

- Packet Wire interface (serial bit data, bit clock, packet delimiter, abort, ready, busy)
- AMBA APB slave interface, with sideband signals as per [GRLIB]

The core incorporates status and monitoring functions accessible via the AMBA APB slave interface. This includes:

- Busy and ready signalling from PacketWire interface

Data are transferred to the PacketWire interface by writing to the AMBA APB slave interface. It is possible to transfer one, two or four bytes at a time, following the AMBA big-endian convention regarding send order. Data are output serially on the PacketWire interface.The packet delimiter and abort signals are controlled, together with the data size, through the control register. The progress of the interface can be monitored via the AMBA APB slave interface, through the control register. The baud rate is set via a configuration register.

134.2 PacketWire interface

A PacketWire link comprises four ports for transmitting the message delimiter, the bit clock, the serial bit data and an abort signal. A link also comprises additional ports for busy signalling, indicating when the receiver is ready to receive the next octet, and for ready signalling, indicating that the receiver is ready to receive a complete packet. The waveform format shown in figure 337.

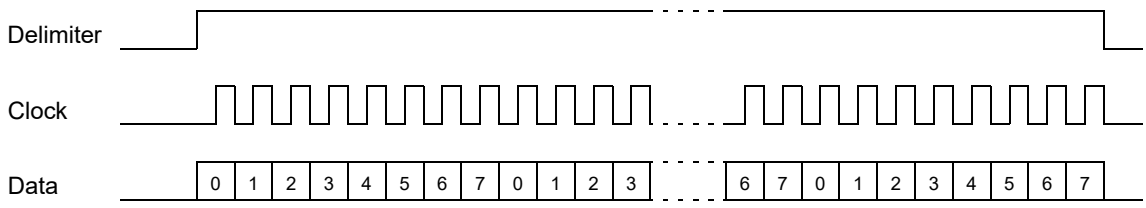


Figure 337. Synchronous bit serial waveform

The PacketWire protocol follows the CCSDS transmission convention, the most significant bit being sent first, both for octet transfers (control), and for word transfer (address or data). Transmitted data should consist of multiples of eight bits otherwise the last bits will be lost. The message delimiter port is used to delimit messages (commands). It should be asserted while a message is being input, and deasserted in between. In addition, the message delimiter port should define the octet boundaries in the data stream, the first octet explicitly and the following octets each subsequent eight bit clock cycles.

The handshaking between the PacketWire link and the interface is implemented with a busy port. When a message is sent, the busy signal on the PacketWire link will be asserted as soon as the first data bit is detected, it will then be deasserted as soon as the interface is ready to receive the next octet. This gives the transmitter ample time to stop transmitting after the completion of the first octet and wait for the busy signal deassertion before starting the transmission of the next octet. The handshaking is continued through out the message.

To ensure that the receiver recognizes that the delimiter has been de-asserted, an application specific minimum time for the de-assertions should be imposed. Alternatively, ready signalling can be implemented in software, where the ready signal is asserted when the receiver software is ready to receive a

packet, and is then immediately de-asserted when the first octet of a packet has been received. The transmitter software should thus only check the ready signal before starting to send a packet. This is illustrated in figure 338.

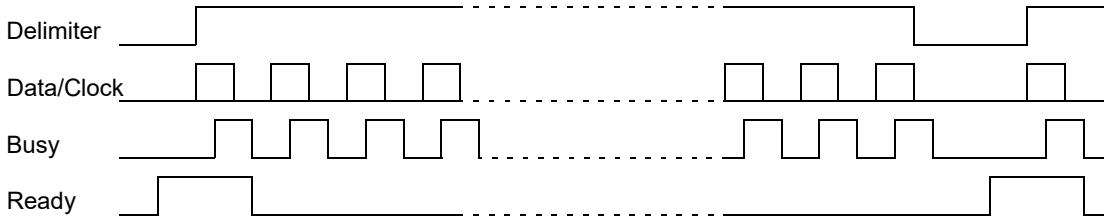


Figure 338. Handshake with ready signalling

To ensure that an abort is properly signalled, the abort signal should be de-asserted at the time the delimiter is asserted in the beginning of a packet, else the abort will be ignored. The abort signal should then be asserted while the delimiter is still asserted, to signal an abort to the receiver.

134.3 Registers

The core is programmed through registers mapped into APB address space.

Table 2009. APB2PW registers

APB address offset	Register
0x000	Control Register
0x004	Configuration Register
0x008	Data Transmission Register

134.3.1 Control Register

*Table 2010.*0x000 - CTRL - Control Register

31 8	7	6	5	4	3	2	1 0
RESERVED	RESET	R	READY	BUSY	VALID	ABORT	SIZE

31: 8 RESERVED
- Write: Don't care.
- Read: All zero.

7 RESET
- Write: Write logical one to reset core
- Read: All zero

6 RESERVED
- Write: Don't care.
- Read: All zero.

5 READY
- Write: Don't care.
- Read: Interface ready to receive a packet

4 BUSY
- Write: Don't care.
- Read: Interface busy with octet(s) when set, else ready for data input

3 VALID
- Read/Write: Packet delimiter when asserted (only affects output signal)

2 ABORT
- Read/Write: Abort current packet when asserted (only affects output signal)

1: 0 SIZE — Transfer size and order (left to right):
- Read/write: 00 = 8 bit: 7:0
- 01 = 16 bit: 15:8, 7:0
- 10 = 24 bit: 23:16, 15:8, 7:0
- 11 = 32 bit: 31:24, 23:16, 15:8, 7:0

Power-up default: 0x00000000

134.3.2 Configuration Register

*Table 2011.*0x004 - CONF - Configuration Register

31 8	7 0
RESERVED	HALFBAUD

31: 8 RESERVED
- Write: Don't care.
- Read: All zero.

7: 0 HALFBAUD — System clock division factor (indicates the width of the high and low phases of the outgoing PacketWire bit clock in number of system clock periods -1)
- Read/write: 0x00 = divide by 1
- 0xFF = divide by 256

Power-up default: 0x00000000

134.3.3 Data Transmission Register

*Table 2012.*0x008 - TX - Data Transmission Register

31 24	23 16	15 8	7 0
FIRST OCTET	SECOND OCTET	THIRD OCTET	LAST OCTET

31: 24 FIRST OCTET
- Write: First octet to be transmitted, if SIZE=11
- Read: All zero.

23: 16 SECOND OCTET
- Write: Second octet to be transmitted
- Read: All zero.

15: 8 THIRD OCTET
- Write: First octet to be transmitted
- Read: All zero.

7: 0 LAST OCTET
- Write: Last octet to be transmitted, any SIZE value
- Read: All zero.

Power-up default: 0x00000000

134.4 Vendor and device identifiers

The module has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x03B. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

134.5 Configuration options

Table 2013 shows the configuration options of the core (VHDL generics).

*Table 2013.*Configuration options

Generic name	Function	Allowed range	Default
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	Addr field of the APB bar.	0 - 16#FFF#	0
pmask	Mask field of the APB bar.	0 - 16#FFF#	16#FFC#
syncrst	Only synchronous reset	0, 1	1

134.6 Signal descriptions

Table 2014 shows the interface signals of the core (VHDL ports).

*Table 2014.*Signal descriptions

Signal name	Field	Type	Function		Active
RSTN	N/A	Input	Reset		Low
CLK	N/A	Input	Clock		-
APBI	*	Input	APB slave input signals		-
APBO	*	Output	APB slave output signals		-
PWI	BUSY_N	Input	Not ready for octet	This input port indicates whether the receiver is ready to receive one octet. The input is considered as asynchronous.	Low
	READY		Ready for packet	This input port indicates whether the receiver is ready to receive one packet. The input is considered as asynchronous.	High
PWO	VALID	Output	Delimiter	This output port is the packet delimiter for the output interface. It is deasserted between packets. The output is clocked out on the rising CLK edge.	High
	CLK		Bit clock	This output port is the PacketWire output bit clock. The output is clocked out on the rising CLK edge.	Rising
	DATA		Data	This output port is the serial data output for the interface. The output is clocked out on the rising CLK edge.	-
	ABORT		Abort	The output is clocked out on the rising CLK edge.	High

* see GRLIB IP Library User's Manual

134.7 Signal definitions and reset values

The signals and their reset values are described in table 2015.

*Table 2015.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
pwi_valid	Input	Delimiter	High	-
pwi_clock	Input	Bit clock	Rising	-
pwi_data	Input	Data	-	-
pwi_aboart	Input	Abort	High	-
pwo_busy_n	Output	Not ready for octet	Low	Logical 0
pwo_ready	Output	Ready for packet	High	Logical 0

134.8 Timing

The timing waveforms and timing parameters are shown in figure 339 and are defined in table 2016.

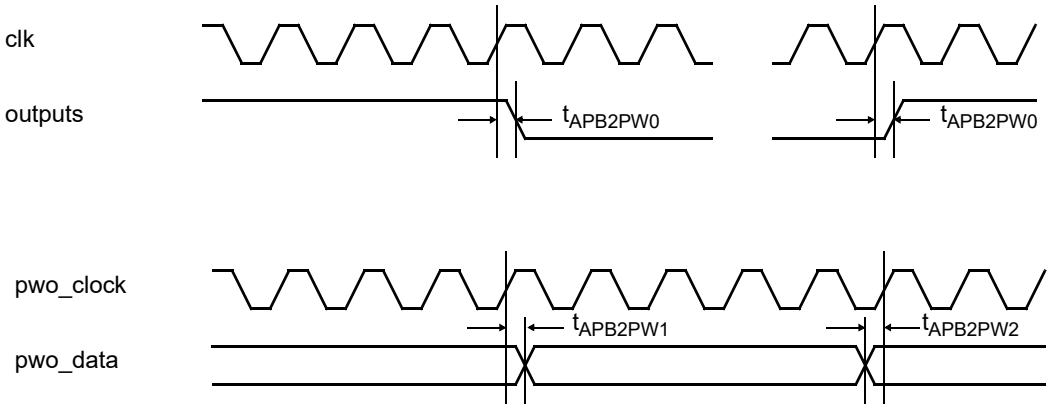


Figure 339. Timing waveforms

*Table 2016.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{APB2PW0}$	clock to output delay	rising *clk* edge	TBD	TBD	ns
$t_{APB2PW1}$	input to clock hold	rising *pwo_clock* edge	TBD	-	ns
$t_{APB2PW2}$	input to clock setup	rising *pwo_clock* edge	TBD	-	ns
$t_{APB2PW3}$	pwo_valid to pwo_clock edge	rising *pwo_clock* edge	TBD	-	ns
$t_{APB2PW4}$	pwo_valid de-asserted period	-	TBD*t_{CLK}		periods

Note: The inputs are re-synchronized inside the core. The signals do not have to meet any setup or hold requirements.

134.9 Library dependencies

Table 2017 shows the libraries used when instantiating the core (VHDL libraries).

*Table 2017.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
TMTC	TMTC_Types	Signals, component	Component declarations, signals.

135 AHB2PP - AMBA AHB to Packet Parallel Interface

135.1 Overview

The AMBA AHB to Packet Parallel Interface implements the PacketParallel protocol used by the Packet Telemetry Encoder (PTME) IP core and the Virtual Channel Assembler (VCA) device.

The core implements the following functions:

- Packet Parallel protocol
- General Purpose Input Output port

The core provides the following external and internal interfaces:

- Packet Parallel interface (octet data, packet delimiter, write strobe, abort, ready, busy)
- AMBA AHB slave interface, with sideband signals as per [GRLIB]
- AMBA APB slave interface, with sideband signals as per [GRLIB]

The core incorporates status and monitoring functions accessible via the AMBA APB slave interface. This includes:

- Busy and ready signalling from Packet Parallel interface
- Read back of output data
- Interrupts on ready for new word, or ready for new packet

Data is transferred to the Packet Parallel interface by writing to the AMBA AHB slave interface, located in the AHB I/O area. Writing is only possible when the Packet Parallel packet valid delimiter is asserted, else the access results in an AMBA access error. It is possible to transfer one, two or four bytes at a time, following the AMBA big-endian convention regarding send order. The last written data can be read back via the AMBA AHB slave interface. Data are output as octets on the Packet Parallel interface.

In the case the data from a previous write access has not been fully transferred over the Packet Parallel interface, a new write access will result in an AMBA retry response. The progress of the interface can be monitored via the AMBA APB slave interface. An interrupt is generated when the data from the last write access has been transferred. An interrupt is also generated when the Packet Parallel ready indicator is asserted.

135.2 Interrupts

Two interrupts are implemented by the Packet Parallel interface:

Index:Name:Description:

0 NOT BUSYReady for a new data (word, half-word or byte)

1 READYReady for new packet

The interrupts are configured by means of the *pirq* VHDL generic.

135.3 Registers

The core is programmed through registers mapped into APB address space.

*Table 2018.*AHB2PP registers

APB address offset	Register
0x000	Configuration Register
0x004	Status Register
0x008	Control Register
0x010	Data Input Register
0x014	Data Output Register
0x018	Data Direction Register

135.3.1 Configuration Register (R/W)

*Table 2019.*0x000 - CONF - Configuration Register

31	3	0
RESERVED	WS	
0	0	
r	rw	

3-0: WS Number of additional Wait States

All bits are cleared to 0 at reset.

The width of the write strobe can be extended by mean of the WS field. The nominal asserted width is one system clock period (corresponding to WS=0). The asserted period can be extended up to a total asserted width of 16 system clock periods.

The minimum gap between octet write accesses when the strobe is de-asserted is one system clock period when WS={0, 3}, two when WS={4, 7}, three when WS={8, 11}, and four when WS={12, 15}.

135.3.2 Status Register)

*Table 2020.*0x004 - STAT - Status register

31	3	2	1	0
RESERVED		BUSY	PP Busy	PP Ready
0		0	0	0
r		r	r	r

2: BUSY AHB2PP interface busy with data transfer
1: PP Busy Packet Parallel busy input
0: PP Ready Packet Parallel ready input

All bits are cleared to 0 at reset.

135.3.3 Control

*Table 2021.*0x008 - CTRL - Control Register

31 4	3	2	1	0
RESERVED	PP Abort	PP Valid	RST	EN
0	0	0	0	0
r	rw	rw	rw*	rw

3: PP Abort Packet Parallel abort output
2: PP Valid Packet Parallel valid output
1: RESET Reset complete core when 1
0: ENABLE Enable Packet Parallel interface when 1, else enable GPIO function

All bits are cleared to 0 at reset. Note that RESET is read back as 0b.

135.3.4 Data Input

*Table 2022.*0x010 - DIN - Data Input Register

31 8	7 0
RESERVED	DIN
0	0
r	r

7-0: DIN Input data *ppi.data[7:0]*

All bits are cleared to 0 at reset.

135.3.5 Data Output

*Table 2023.*0x014 - DOUT - Data Output Register

31 8	7 0
RESERVED	DOUT
0	0
r	rw

7-0: DOUT Output data *ppo.data[7:0]*

All bits are cleared to 0 at reset.

Note that the GPIO functionality can only be used when the Packet Parallel interface is disabled via the Control Register above.

135.3.6 Data Direction

*Table 2024.*0x018 - DIR - Data Direction Register

31 8	7 0
RESERVED	DDIR
0	0
r	r

7-0: DDIR Direction: *ppo.enable[7:0]*
0b = input = high impedance,

1b = output = driven

All bits are cleared to 0 at reset.

Note that the GPIO functionality can only be used when the Packet Parallel interface is disabled via the Control Register above.

135.4 AHB I/O area

Data to be transferred to the Packet Parallel interface is written to the AMBA AHB slave interface which implements a AHB I/O area. See [GRLIB] for details.

Note that the address is not decoded by the core. Address decoding is only done by the AMBA AHB controller, for which the I/O area location and size is configured by means of the *ioaddr* and *iomask* VHDL generics.

It is possible to transfer one, two or four bytes at a time, following the AMBA big-endian convention regarding send order. The last written data can be read back via the AMBA AHB slave interface. Data are output as octets on the Packet Parallel interface.

*Table 2025.*AHB I/O area - data word definition

31 24	23 16	15 8	7 0
DATA [31:24]	DATA [23:16]	DATA [15:8]	DATA [7:0]

*Table 2026.*AHB I/O area - send order

Transfer size	Address offset	DATA [31:24]	DATA [23:16]	DATA [15:8]	DATA [7:0]	Comment
Word	0	first	second	third	last	Four bytes sent
Halfword	0	first	last	-	-	Two bytes sent
	2	-	-	first	last	Two bytes sent
Byte	0	first	-	-	-	One byte sent
	1	-	first	-	-	One byte sent
	2	-	-	first	-	One byte sent
	3	-	-	-	first	One byte sent

135.5 Vendor and device identifiers

The module has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x039. For description of vendor and device identifiers see GRLIB IP Library User's Manual.

135.6 Configuration options

Table 2027 shows the configuration options of the core (VHDL generics).

*Table 2027.*Configuration options

Generic name	Function	Allowed range	Default
hindex	AHB master index.	1 - NAHBSLV-1	0
ioaddr	Addr field of the AHB IO bar.	0 - 16#FFF#	0
iomask	Mask field of the AHB IO bar.	0 - 16#FFF#	16#F00#
pindex	APB slave index	0 - NAPBSLV-1	0
paddr	Addr field of the APB bar.	0 - 16#FFF#	0
pmask	Mask field of the APB bar.	0 - 16#FFF#	16#FFC#
pirq	Interrupt line used by the AHB2PP.	0 - NAHBIRQ-1	0
syncrst	Only synchronous reset	0, 1	1
oepol	Output enable polarity	0, 1	1

135.7 Signal descriptions

Table 2028 shows the interface signals of the core (VHDL ports).

*Table 2028.*Signal descriptions

Signal name	Field	Type	Function	Active
RSTN	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
AHBI	*	Input	AMB slave input signals	-
AHBO	*	Output	AHB slave output signals	-
PPI	busy_n	Input	Packet Parallel busy signal	-
	ready		Packet Parallel ready signal	
	data[7:0]		Packet Parallel data (GPIO only)	
PPO	abort	Output	Packet Parallel abort signal	-
	valid_n		Packet Parallel packet delimiter signal	-
	wr_n		Packet Parallel octet write strobe	
	data[7:0]		Packet Parallel octet data	
	enable[7:0]		Enable/drive octet data output	

* see GRLIB IP Library User's Manual

135.8 Library dependencies

Table 2029 shows the libraries used when instantiating the core (VHDL libraries).

*Table 2029.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	AMBA signal definitions
TMTC	TMTC_Types	Signals, component	Component declarations, signals.

136 GRRM - Reconfiguration Module

136.1 Overview

The core processes different alarms and provides reconfiguration commands as outputs. When alarm conditions are matched the reconfiguration sequences are fetched from the external memory, these sequences are processed and output commands are provided specific to an alarm. The core operates in an AMBA bus system where both the AMBA AHB bus and the APB bus are present. The AMBA APB bus is used for configuration, control and status handling and the AMBA AHB Master is used to generate read and write access on the AMBA AHB bus.

136.2 Operation

According to the alarm activated and the current state of the core an alarm pattern is formed, the alarm pattern provides the address from which the reconfiguration sequences should be fetched. The AMBA AHB bus is used for retrieving the reconfiguration sequences in memory external to the core. The reconfiguration sequences consist of internal commands and external commands. The internal commands are processed by internal command processor which performs actions like masking the alarm that got activated and changing the state according to the internal commands. The external commands are formed into packets and sent to the command pulse distribution unit using PacketWire interface. The alarms can be logged to external memory along with the time instance at which the alarm is triggered. During initialization the core can configure itself or other systems available in the AHB bus.

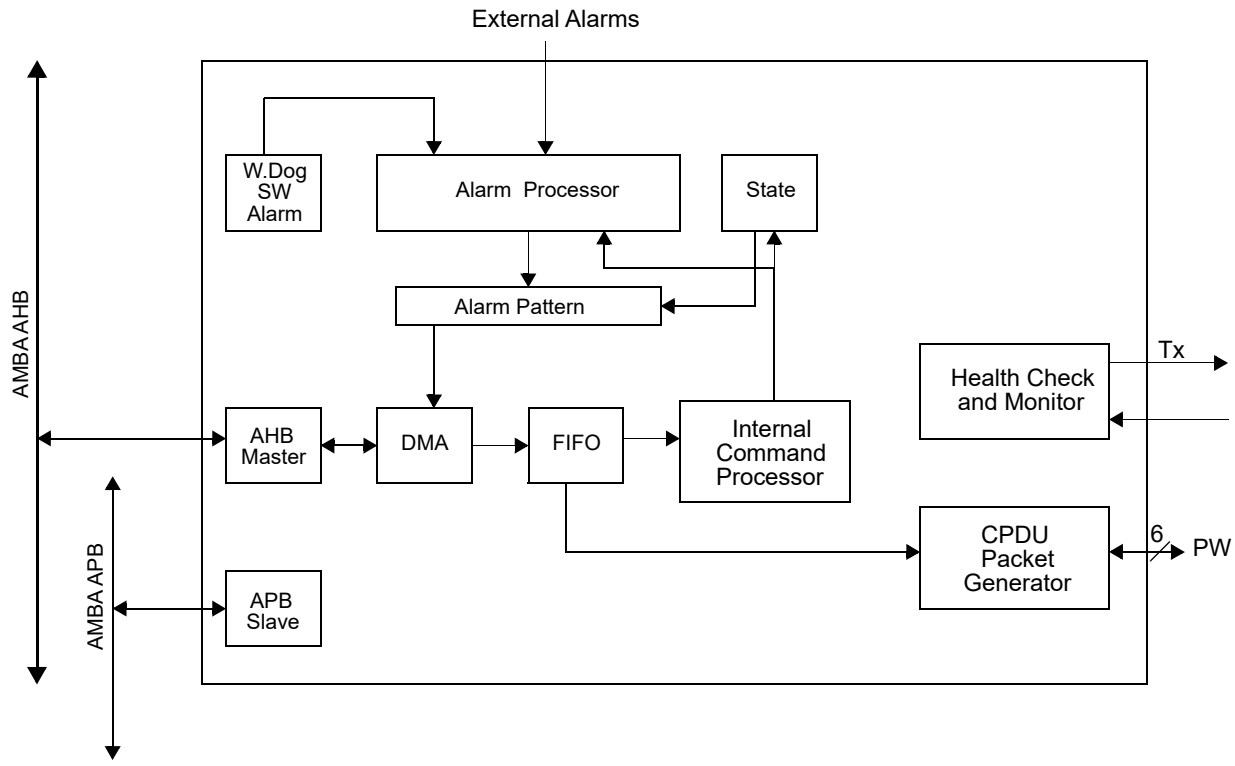


Figure 340. Block diagram

136.3 Alarms

External alarms (external discrete signal inputs), watchdog timeout and software alarms (alarm triggered by processors or any other unit capable of writing the APB register space) are the alarm inputs. Using watchdog and software alarms the core can monitor the processor module and using external

alarms the core can monitor high-level system alarms for example low battery indicator. All alarms are individually maskable using the alarm mask AM register.

136.3.1 External alarms

The external alarm inputs are processed and an alarm event is generated when the input matches the conditions specified in the alarm monitoring unit. For external alarms the monitoring unit consist of mask AM, polarity AP and delay AD registers, these registers must be configured according to the requirement for a particular external alarm. An external input should pass the above mentioned condition and produces the alarm event which is registered as a pending event in the alarm pending AP register.

136.3.2 Watchdog timeout

Watchdog timeout: it is a down-counter that must be cyclically reloaded upon by the processor. If it is not reloaded an alarm event is triggered which is registered as a pending event in the alarm pending AP register. The corresponding mask AM register must be enabled.

136.3.3 Software alarms

The processor can trigger a software alarm event by configuring the register SWNP. The SWNP.SWPM0 register bits can be configured with a value corresponds to a particular software alarm. The value 0b000 is reserved and all other values trigger an alarm respectively (seven software alarm). The SWNP.EN bit must also be set to trigger the alarm.

The software alarms can also be used to check the functionality of the core by allocating one of the alarms to be self check alarm, the processor can trigger that alarm and expect the reconfiguration sequences to clear that alarm pending event. The reconfiguration sequence must also be configured according to the need.

The software alarm 0b001 has the highest priority and 0b111 has the lowest priority.

136.4 Alarm Pattern

Alarm pending AP register memorizes any alarm that has triggered an alarm event. Each alarm becomes a pending event. The reconfiguration sequences are selected according to the highest priority pending alarm event and the current state of the state machine. The highest priority is given to external alarms, followed by watchdog alarms and finally software alarms.

Alarm pattern is formed by concatenation of the priority vector (LSB) and the state machine output (MSB). This vector is used as a pointer to the first address of the reconfiguration sequence to be executed. On this basis, the reconfiguration sequences are read from the external memory and stored in the internal buffers for processing.

The core includes a state machine STAT.STATE register of which the state can be modified by the reconfiguration sequences. The updates to the state machine by reconfiguration sequence allows another reconfiguration sequence to be executed for the same alarm if a previous reconfiguration attempt did not remedy the alarm situation.

136.5 Reconfiguration Log

After occurrence of every alarm event, the alarm pattern is stored in a circular buffer (available in the external memory area) allocated for reconfiguration log. Only previous 16 patterns (alarm events) can be stored. The alarm log address ALA register specify the location where the log must be stored. Each

log consist of 2 words. The log consist of time instance at which the alarm event occurred and the alarm pattern (state+alarm). The content of the log is shown in the table below.

Table 2030. Alarm Log Content

Word 1	Coarse Time (32 bits)	
Word 2	Fine Time (23 bits)	ALARM PATTERN (9 bits)

136.6 Reconfiguration Sequences

The reconfiguration sequences are fetched and stored into the internal buffers for an alarm event. The commands are processed one by one. Each reconfiguration sequence is made up of 64 Commands sent to Command Pulse Distribution Unit (CPDU) separated by delay and 64 commands for RM internal configuration (split into two - internal1 and internal2 of each containing 32 commands). The order of execution is internal1 commands, external commands followed by internal2 commands. The starting address of the initial (highest priority alarm) reconfiguration sequence location is provided by the RSA.SA register and for the other alarms the address from which the sequences are fetched is computed by the core itself using the particular alarm event and state of the alarm. A spreadsheet is provided along with this document to facilitate the configuration of these reconfiguration sequences, the output file from the spreadsheet can be used to load the reconfiguration sequences into an external memory.

136.6.1 Internal commands

The internal 64 commands are split into 2 blocks each containing 32 commands. The internal commands will perform internal control of the RM like masking the alarm currently in process, changing the state machine value (to try different pattern or reconfigure). The table below list the commands.

Table 2031. Internal Commands

Command	Parameter (maximum 24 bits)	Code	Purpose
Clear all pending	No	0x00	Clear all pending alarms
Clear current pending	No	0x01	Clear current pending alarm
Mask all	No	0x02	Mask all alarms
Mask current	No	0x03	Mask current pending alarms
Unmask all	No	0x04	Unmask all alarms
Unmask current	No	0x05	Unmask current alarm
Rearm Watchdog Nominal	Yes (24 bit value)	0x06	Rearm watchdog with the value in the parameter
Rearm Watchdog Redundant	Yes (24 bit value)	0x07	Rearm watchdog with the value in the parameter
Delay	Yes (16 bit value)	0x08	Perform delay of processing according to the parameter value. The prescaler for this delay is taken from the CP register
Set state	Yes (4 bit value)	0x09	Set state according to parameter
Set active SGM	Yes (3 bit value)	0x0A	Set which safe guard memory (SGM) contains the active content. According to this the GSC.CONT registers are updated
Check alarm	Yes (4 bit value)	0x0B	Check that the alarm is not triggered again after a reconfiguration, if triggered again increment the state and perform another reconfiguration sequence. This must be used in combination with other internal commands (delay, pending mask). For example: clear the corresponding pending alarm, unmask the processed alarm, provide a delay (if needed to check that the alarm happens again) and finally provide the Check alarm command, the state will be incremented only when the alarm is still pending.
Processor Write protect	Yes (4 bit value)	0x0C	According to this value the PSC.PMWP registers are updated. The registers are driven as output signals and connected to the write protection unit
End internal command	No	0xFE	After this the internal command execution moves to the next stage (to external command if internal command 1 was processed or end of command processing if internal 2 was processed)
Do nothing	No	0xFF	Skip a command execution

136.6.2 External commands

The External commands are sent as CPDU packets using PacketWire interface.

The format of each external command is shown below and the format of the final packet generated is explained in the next section. If all the external commands are not needed for processing the external command execution can be stopped by setting the delay section (see below table) of the reconfiguration sequence to be 0xFFFE.

Table 2032. External command format

31 16	15 4	3	2 0
Delay	PULSE	-	LEN
-			

31: 16	Delay - Delay needed in between different external commands (resolution of 1 ms and configurable using the CP register)
15: 4	PULSE - Pulse output number
3	Reserved
2: 0	LEN - Pulse Length

136.7 CPDU Packet Generator

The external commands (PULSE and LEN in the above table) in the reconfiguration sequences are formed into CPDU Packets that contain one Command Instruction. These are sent as output on a PacketWire interface as TeleCommand segments.

The block that generates the CPDU packets uses the flowing input data: 11-bit Application Process ID (programmable through CC.APID register), 12-bit pulse output number and 3-bit pulse length (PULSE and LEN in the above table). The Segment is illustrated in the table below.

*Table 2033.*CPDU Segment.

Telecommand Segment													
Segment Header		Packet Header							Packet Data Field				
Seq. Flags	MAP Id.	Packet ID				Packet Seq Control		Packet Length	Command Instruction				Packet Error Control
		Version Number	Type	Data Filed Header Flag	Application Process ID	Seq. Flags	Seq. Count		Output No. LSB	Output No. MSB	Reserved	Pulse Length	
3	0	0	1	0	Configurable	3	Auto Incr.	3	Configurable	Configurable	0	Configurable	Enabled
2	6	3	1	1	11	2	14	16	8	4	1	3	
8		16				16		16	16				16

The sequence counter is automatically incremented after each packet

136.8 Initial Core Configuration

During initialization the core can configure itself or other systems available in the AHB bus. The Initial configuration address ICA.CA register specify the initial configuration base address. Each configuration consist of four word of information described in the table below.

*Table 2034.*Initial Configuration

Commands	**Purpose**
Address Source	Source from where the data must be fetched
Address Destination	Destination to where the data must be stored
Length in words (4 bytes)	number of words to be transferred. Always one more than the number specified here. (Zero means 1 and 31 means 32, maximum 512 bytes i.e. 128 words)
Pointer	Next command base address. Least significant bit specify next command is available or not. If more configurations need to be performed set the least significant bit must be set to'1' other wise '0'

The configuration must be performed before the initial delay before start of alarm monitoring ID.DELAY register pass out. This delay is provided for the external units and processor to set the alarm inputs at their right nominal state and thus ensure that untimely reconfiguration are not executed because the system is still booting.

136.9 Health Communication

The RM can send its role and health informations to another RM if an health link is available in between them. By default one of the RM is set to be the master and the other Slave. The CTRL.ACTMST register specify whether the RM is active or inactive.

The active master will set itself to be in execute state (after the initial delay timeout) and the inactive slave set itself to be in the monitor state. The health state is available in the health status HSTAT.HSTATE register. The master RM can send active message to the slave RM using the communication link. The HCTRL.COMM, HCTRL.TXEN and HCTRL.RXEN must be set in both RM to properly send and receive. The interval of the message transfer is configurable using HMSG register, similarly the timeout to receive the message for slave is configurable using HMTO register. If the health send and health message timeout is enabled then when the message is not received by the slave after the timeout the slave set itself to be master. The previous master RM set itself to be in inactive state and mask all the alarms. The redundant RM will set itself to be master and process any pending alarm. The redundant RM move from monitor to execute state.

Similar to this the health alarm timeout HATO register can be configured, in this case when an alarm is not processed for a long time the active RM set itself to be inactive and send a message to the redundant RM to go active. If the health alarm timeout is enabled in the slave then redundant RM set itself to be active and set the other to be inactive.

By using the HCTRL.FORCE register the state of active and inactive RM can be changed. The force can move an RM from execute to inactive state and inactive to execute state. Using the HCTRL.FORCE the RM can also move from monitor to execute state.

136.10 RM Error

The following errors can occur in the RM unit which are updated in the RME register, Init error IER - the initial delay (before start of alarm monitoring) timed out before the configurations are completed, Log write error LOGER - error writing the alarm log, Initial configuration read error CRER, Initial configuration write error CWER and Sequence Read Error SEQER - Error in reading the reconfiguration sequences after an alarm event. RM Error (RMER) - This field will go high when any of the above error occurs. The errors can be cleared by writing ’1’ to the corresponding register. The errors must be rectified before it can be cleared otherwise the same errors will occur. For example the init error can be rectified by properly configuring the device before timeout (CTRL.CONFDONE is high before timeout) and clear the init error. Similarly the configuration read and write error can be cleared by configuring the RM unit using external unit and clear the corresponding error bits. The configuration read and write error can also be corrected by fixing the memory fetch in which the error occurs and making a core reset by activationg CTRLRESET.

It is possible to reconfigure (switch other RM to be active) because of an error, if the CTRL.EREC is enabled. The switchover can be based on any of the following critical error - Initial configuration read error CRER, Initial configuration write error CWER and Sequence Read Error SEQER. The Switchover can happen only when the health communication is available between the two RM. If no health communication is available it is possible to provide reset using the HCTRL.RESET register. By providing the HCTRL.RESET the RM will set itself to be in default init state and the RM registers must be configured properly by an external unit to start functioning again.

136.11 Registers

The core is programmed through registers mapped into APB address space.

*Table 2035.*Reconfiguration Module registers

APB address offset	Register
0x00	Control
0x04	Initial Configuration Address
0x08	Reconfiguration Sequence Address
0x0C	Alarm Log Address
0x10	Watchdog Prescaler
0x14	Common Prescaler
0x18	Initial Delay Before Start Of Alarm Monitoring
0x1C	CPDU Control
0x20	Health Control
0x24	Health Message Time-Out
0x28	Health Alarm Time-Out
0x2C	Health Send Message
0x40	Alarm Mask
0x44	Alarm Level
0x48	Alarm Edge
0x4C	Prescaler For Alarm Delay
0x50 - 0x8C	Alarm 0-15 Delay
0xB0	Status
0xB4	Alarm Status
0xB8	Alarm Pending
0xBC	Health Status
0xC0	RMerror
0xD0	Watchdog Counter Nominal PM
0xD4	Software Alarm Nominal PM
0xE0	Watchdog Counter Redundant PM
0xE4	Software Alarm Redundant PM
0xF0	PM-SGM Control
0xF4	Ground-SGM Control

Table 2036. 0x00 - CTRL - Control

31 24	23 18	17 16	15 14	13 12	11 6	5	4	3	2	1	0
KEY1	RESERVED		CXWDSW	CXEALARM	RESERVED	RESET	EREC	R	ACTMST	CONF-DONE	CON-FEN
0	0		0	0	0	0	0		-	0	1
w	r		rw	rw	r	rw	rw	r	rw	rw	rw

Table 2036. 0x00 - CTRL - Control

31: 24	KEY1 = 0x55
23: 16	RESERVED
15: 14	Cross strapped watch dog and SW alarms (CXWDSW) 0b00 = None Available 0b01 = Only Nominal 0b10 = Only External 0b11 = Both Available
13: 12	Cross strapped External alarms (CXEALARM) 0b00 = None Available 0b01 = Only Nominal 0b10 = Only External 0b11 = Both Available
11: 6	RESERVED
5	reset (RESET) - Resets all the registers in the core.
4	Error reconfigure (EREC) -- If this field is one then for every error mentioned in the RME register switch over to redundant reconfiguration module will occur.
3	RESERVED
2	ACTIVE - If this field is set to one then active master. By default an external input is provided to this field which specify the system is active or not, Connected to the signal master
1	Configuration done (CONFDONE) - If the CONFEN is set to one then if the initial configuration is successfully performed this field will go high. It is not mandatory to use the RM DMA for initial configuration, the initial configuration can be performed by some other unit and this field can be enabled by the external unit performing the initial configuration. This field must be enabled by any of the above specified option and also this must be enabled before the initial time out is configured in the ID register otherwise RM error is triggered (RME.IE register). Connected to the signal confdone
0	Configuration enable (CONFEN) - External units can write 1 to this field and start the initial configuration. This field is also controller by how the core is implemented, the reset value for this field is provided by an external input signal. If the initial configuration should be performed by the RM DMA after the system reset is disabled the external input should be 1, other option is by keeping the input zero and writing this field with 1 by some other unit to start the initialization process. Connected to the signal initconf

Table 2037. 0x04 - ICA - Initial Configuration Address

31 24	23 0
KEY1	CA
	0
w	rw

31: 24	KEY1= 0x55
23: 0	Configuration address CA - The initial configuration performed by the Reconfiguration module DMA fetches the starting configuration commands from this Address.

Table 2038. 0x08 - RSA - Reconfiguration Sequence Address

31 24	23 12	11 0
KEY1	RESERVED	SA
		0x001
w		rw

Table 2038. 0x08 - RSA - Reconfiguration Sequence Address

31: 24 KEY1= 0x55

23: 12 RESERVED

11: 0 Sequence Start Address - SA - The starting address of the first reconfiguration sequence.

Table 2039. 0x0C - ALA - Alarm Log Address

31 24	23 0
KEY1	ALA
	0X400000
w	rw

31: 24 KEY1= 0x55

23: 0 Alarm Log Address - ALA - The MSB address bits point to Alarm Log Area

Table 2040. 0x10 - WDP - Watchdog Prescaler

31 24	15 0
KEY1	WP
	0x00C350
w	rw

31: 24 KEY1= 0x55

23: 16 RESERVED

15: 0 Watchdog Prescaler - WP - Prescaler for the Watchdog counters.

Table 2041. 0x14 - CP - Common Prescaler

31 24	23 0
KEY1	CP
	0x00C350
w	rw

31: 24 KEY1= 0x55

23: 0 Common Prescaler - CP - Prescaler for the delay between external commands, initial delay before start of alarm monitoring, health message time-out and health alarm time-out

Table 2042. 0x18 - ID - Initial Delay Before Start Of Alarm Monitoring

31 24	23 17	16 0
KEY1	RESERVED	DELAY
	0	0xFA00
w	r	rw

31: 24 KEY1= 0x55

23: 16 RESERVED

15: 0 Initial Delay

Table 2043. 0x1C - CC - CPDU Control

31 24	23 18	8	7 0
KEY1	RESERVED	APID	DIVCTRL
	0	0x123	0x10
w	0	rw	rw

Table 2043. 0x1C - CC - CPDU Control

31: 24	KEY1= 0x55
23: 19	RESERVED
18: 8	Application Identifier - (APID) - Sets the Application Identified in transmitted CPDU packets.
7: 0	Transmitter clock divider control - (DIVCTRL)- Contains the System clock division factor (indicates the width of the high and low phases of the outgoing PacketWire bit clock in number of system clock periods -1)

Table 2044. 0x20 - HCTRL - Health Control

31 24	23 8	7 5	4	3	2	1	0
KEY1	BAUD	RESERVED	RESET	FORCE	-	RXEN	TXEN	COMEN
	0X1B2	0	0	0	r	0	0	0
w		r	rw	rw	0	rw	rw	rw

31: 24	KEY1= 0x55
23: 8	Baud required (BAUD) - This field must provide the value corresponding to the Baud rate required which can be calculated using the system clock and the baud rate required (SYSTEMCLK/BAUD rate) Default baud value if 50 MHz and 115200 baud rate.
5: 7	RESERVED
4	Reset (RESET) - RESET - This will cause all the health registers to be in reset state and set the RM inactive.
4	Force (FORCE) Forced Switchover
3	RESERVED
2	Receive Enable - RXEN - Enable message reception when 1
1	Transmit Enable - TXEN - Enable message transmission when 1
0	Communication Enable - COMEN - Enable Communication between Master and Slave when 1

Table 2045. 0x24 - HMTO - Health Message Time-Out

31 24	23	22 16	15 0
KEY1	EN	RESERVED	HMTO
	0	0	0x1F4
w	rw	r	rw

31: 24	KEY1= 0x55
23	Enable (EN)
22: 16	RESERVED
15: 0	Health Message Time-Out - HMTO - When message transmission is enabled between the two RM a message should be received before this time-out.

Table 2046. 0x28 - HATO - Health Alarm Time-Out

31 24	23	22 16	15 0
KEY1	EN	RESERVED	HATO
	0	0	0xFFF0
w	rw	r	rw

31: 24	KEY1= 0x55
23	Enable (EN)
23: 16	RESERVED
15: 0	Health Alarm Time-Out - HATO - An active Alarm should be processed before this time-out.

Table 2047. 0x2C - HSMS - Health Send Message

31 24	23	22 15	0
KEY1	EN	RESERVED	MSG
	0	0	0xFA
w	rw	r	rw

31: 24 KEY1= 0x55

23 Enable (EN)

23: 16 RESERVED

15: 0 Health Send Message (HSMS) - Send Health message at this time interval

Table 2048. 0x40 - AM - Alarm Mask

31 24	23 20	19 0
KEY2	RESERVED	Mask
	0	0
w	r	rw

31: 24 KEY2= 0xB6

23: 20 RESERVED

19: 0 Alarm Mask (Mask) - Each alarm is masked by writing 1 to respective bits.

Fields 15 to 0 are External alarms

Fields 16 Watchdog nominal

Fields 17 Watchdog redundant

Fields 18 Software alarm nominal

Fields 19 Software alarm redundant

Table 2049. 0x44 - AP - Alarm Polarity

31 24	23 15	0
KEY2	RESERVED	POL
	0	0
w	r	rw

31: 24 KEY2= 0xB6

23: 16 RESERVED

15: 0 Alarm Polarity - POL - When 1b corresponding alarm is active when rising edge or high level else falling edge or low level. (only for External Alarm)

Table 2050. 0x48 - AE - Alarm Edge

31 24	23 x	0
KEY2	RESERVED	EDGE
	0	0
w	r	rw

31: 24 KEY2= 0xB6

23: 16 RESERVED

15: 0 Alarm Edge (EDGE) - When 1 corresponding alarm is Edge triggered else Level. (only for External Alarm)

Table 2051. 0x4C - PFAD - Prescaler For Alarm Delay

31 24	23 16	15 0
KEY2	RESERVED	PFAD
	0	0xC350
w	r	rw

Table 2051. 0x4C - PFAD - Prescaler For Alarm Delay

31: 24	KEY2= 0xB6
23: 16	RESERVED
15: 0	Prescaler (PFAD) - Prescaler for external alarm delay

Table 2052. 0x50-0x8C - AD - Alarm 0-15 Delay

31 24	23	22 16	15 0
KEY2	PRE-SEL	RESERVED	DELAY
	0	0	0
w	rw	r	rw

31: 24	KEY2= 0xB6
23	Prescaler Select - (PRESEL) - If this field is one then the external alarm delay includes the prescaler (PFAD).
22: 16	RESERVED
15: 0	DELAY

Table 2053. 0xB0 - STAT - Status

31 12	11 8	7 4	3	2	1	0
RESERVED	LOGCOUNT	STATE	R	IDD	Master	CD
	0	0		0	-	
r	r	r	r	r	r	r

31: 8	RESERVED
11: 8	LOGCOUNT - All the alarm events are logged into an external memory, this register provides the location of the pointer at which the next alarm will be written.
7: 4	STATE - Current state of the an alarm.
3	RESERVED
2	Init delay done (IDD) - Initial delay before start of alarm monitoring timeout.
1	Master - initial configuration of the core after reset.
0	Configuration Done - CD - When initial configuration is completed.

Table 2054. 0xB4 - ASTAT - Alarm Status

31 16	15 0
RESERVED	EAIN
	0
r	r

31: 16	RESERVED
15: 0	External Alarm Input (EAIN) - Direct external alarm inputs

Table 2055. 0xB8 - AP - Alarm Pending

31 0
AP
0
r

Table 2055. 0xB8 - AP - Alarm Pending

31: x RESERVED

31: 0 Alarm Pending - (AP)

Fields 15 to 0 are External alarms

Fields 16 Watchdog nominal

Fields 17 Watchdog redundant

Fields 24 to 18 Software alarm nominal

Fields 31 to 25 Software alarm redundant

Table 2056. 0xBC - HSTAT - Health Status

31 17	16 15 8	7 0
RESERVED	HSTATE	RX	TX
	0	0	0
r	r	r	r

31: 18 RESERVED

17: 16 HSTATE - Current health monitor state

RESET = "00"

EXECUTE = "01"

MONITOR = "10"

INACTIVE = "11"

15: 8 RX - Received health message

7: 0 TX - Transmitted health message

Messages

MACTIVE: = 0x94

MGOACTIVE: = 0xa2

MGOINACTIVE = 0xb1

Table 2057. 0x00 - RME - RM Error

31 24	23 6	5	4	3	2	1	0
KEY3	RESERVED	IER	LOGER	CRER	CWER	SEQER	RMER
w	r	wc	wc	wc	wc	wc	wc

31: 24 KEY3=0x3E

23: 18 RESERVED

4 Init error (IER) - The initial delay before start of alarm monitoring timed out before the configurations are completed.

4 Log write error (LOGER) - Error writing the alarm log

3 Initial configuration read error (CRER)

2 Initial configuration read error (CWER)

1 Sequence Read Error (SEQER) - Error in reading the reconfiguration sequences after an alarm event.

0 RM Error (RMER) - This field will go high when any of the above error occurs.

Table 2058. 0xD0 - WDNP - Watchdog Counter Nominal PM

31 24	23 7	0
KEY4	RESERVED	WDPM0
	0	0xFA
w	r	rw

Table 2058. 0xD0 - WDNP - Watchdog Counter Nominal PM

31: 24 KEY4=0xC7

23: x RESERVED

x: 0 Watchdog Time-out PM 0 - WDPM0 -

Table 2059. 0xD4 - SWNP - Software Alarm Nominal PM

31 24	23 5	4	3	2 0
KEY5	RESERVED	R	EN	SWPM0
	0	0	0	0
w	r	r	rw	rw

31: 24 KEY5=0x2A

23: 5 RESERVED

4 RESERVED

3 Enable (EN) - Should be written with 1 when a software alarm needed to be triggered, (cleared internally)

2: 0 Software Alarm PM 0 (SWPM0) - Software alarm from the nominal processor module. (any value other than 0b000 trigger corresponding software alarm)

Table 2060. 0xE0 - WDRP - Watchdog Counter Redundant PM

31 24	23 7	0
KEY6	RESERVED	WDPM1
	0	0xFA
w	r	rw

31: 24 KEY6=0xD4

23: x RESERVED

x: 0 Watchdog Time-out PM 1 - WDPM1 -

Table 2061. 0xE4 - SWRP - Software Alarm Redundant PM

31 24	23 5	4	3	2 0
KEY7	RESERVED	R	EN	SWPM1
	0	0	0	0
w	r	r	rw	rw

31: 24 KEY7=0xEB

23: 5 RESERVED

4 RESERVED

3 Enable (EN) - Should be written with 1 when a software alarm needed to be triggered, (cleared internally)

2: 0 Software Alarm PM 1 (SWPM1) - Software alarm from the redundant processor module. (any value other than 0b000 trigger corresponding software alarm)

Table 2062. 0xF0 - GSC - Ground-SGM Control

31 24	23 6	4	3	2	1	0
KEY8	RESERVED	GNDP2	GNDP1	CONT3	CONT2	CONT1
		0	0	0	0	0
w	r	rw	rw	rw	rw	rw

Table 2062. 0xF0 - GSC - Ground-SGM Control

31: 24	KEY8=0x83
23: 5	RESERVED
4	Writeprotect Area 2 from Ground access (GNDP2) - Active when set 1
3	Writeprotect Area 1 from Ground access (GNDP1) - Active when set 1
2	Active Context 3 (Cont3) - When set SGM area #3 currently contains the active context
1	Active Context 2 (Cont2) - When set SGM area #2 currently contains the active context
0	Active Context 1 (Cont1) - When set SGM area #1 currently contains the active context

Table 2063. 0xF4 - PSC - PM-SGM Control

31 24	23 4	3	2	1	0
KEY9	RESERVED	PMwP4	PMWP3	PMWP2	PMWP1
		0	0	0	0
w	r	rw	rw	rw	rw

31: 24	KEY9=0x92
23: 2	RESERVED
3	Writeprotect Area 4 from PM access (PMP4) - Active when set 1
2	Writeprotect Area 3 from PM access (PMP3) - Active when set 1
1	Writeprotect Area 2 from PM access (PMP2) - Active when set 1
0	Writeprotect Area 1 from PM access (PMP1) - Active when set 1

136.12 Vendor and device identifiers

The core has vendor identifier 0x01 (Cobham Gaisler) and device identifier 0x09A. For a description of vendor and device identifiers see GRLIB IP Library User's Manual.

136.13 Implementation

136.13.1Reset

The core does not change reset behaviour depending on settings in the GRLIB configuration package (see GRLIB User's Manual). The core makes use of synchronous reset and resets a subset of its internal registers.

136.14 Configuration options

Table 2064 shows the configuration options of the core (VHDL generics).

*Table 2064.*Configuration options

Generic	Function	Allowed range	Default
gCONFADDR	Starting address location for the initial configuration commands	0 - 16#FFFFFF#	16#100000#0
gSEQADDR	Starting address location for the reconfiguration sequence	0 - 16#FFF#	16#300#
gLOGADDR	Starting address location for the alarm logs	0 - 16#FFFFFF#	16#400000#0
gNOEXT	Number of external alarms	2 - 16	16
gALARMPRE	Alarm delay preamble bits	1 - 24	16
gALARMDLY	Alarm delay timeout bits	1 - 23	8
gWATCHDOG	Watchdog availability (0- No watchdog alarm, 1- only nominal, 2- both nominal and redundant)	0 - 2	2
gWDOGPRE	Watchdog preamble bits	1 - 24	16
gWDOGDLY	Watchdog timeout bits	1 - 24	8
gSWALARM	Software alarm available (0- No software alarm, 1- only nominal, 2- both nominal and redundant)	0 - 2	2
gNOSW	Number of software alarms	1 - 7	7
gCOMPRE	Common preamble bits	1 - 24	24
gINITDLY	Initial timeout bits	1 - 16	16
gSYSTEMCLK	System clock frequency [Hz]	Integer	50000000
gBAUD	UART baud rate	Integer	115200
gPROG	Programmable baud rate when 1	0 - 1	1
gHEALTH	Health communication availability	0 - 1	1
gHTHBITS	Health timeout bits	1 - 23	16
gBUFTYPE	Type of RAM used (0 - Generic RAM interface selected, 1 - Gaisler RAM interface selected)	0	0
gPINDEX	APB slave index	0 - NAPBSLV-1	0
gHINDEX	AHB master index	0 - NAHBMST-1	0
gPADDR	ADDR field of the APB BAR	0 - 16#FFF#	0
gPMASK	MASK field of the APB BAR	0 - 16#FFF#	16#FFF#
gPIRQ	Not implemented	0 - NAPBIRQ	1

136.15 Signal descriptions

Table 2065 shows the interface signals of the core (VHDL ports).

*Table 2065.*Signal descriptions

Signal name	Field	Type	Function	Active
RST	N/A	Input	Reset	Low
CLK	N/A	Input	Clock	-
APBI	*	Input	APB slave input signals	-
APBO	*	Output	APB slave output signals	-
AHBMI	*	Input	AHB master input signals	-
AHBMO	*	Output	AHB master output signals	-
EXTALARM	N/A	Input	External alarm input signals	-
EXTTIME	N/A	Input	External time input signals	-
PKTWREADY	N/A	Input	Ready for packet	High
PKTWBUSY_N	N/A	Input	Not ready for octet	Low
PKTWCLK	N/A	Output	Bit clock	-
PKTWDATA	N/A	Output	Data	-
PKTWVALID	N/A	Output	Delimiter	High
PKTWABORT	N/A	Output	Abort	High
HEALTHRX	N/A	Input	UART receiver data	-
HEALTHTX	N/A	Output	UART transmit data	-
MASTER	N/A	Input	Select RM master or slave	High
INITCONF	N/A	Input	To enable initial configuration externally	High
CONFDONE	N/A	Input	If initial configuration not required tie this signal to active High	High
ALARM_EVT	N/A	Output	AHB master output signals	-
ALARMLOG	N/A	Output	AHB master input signals	High
RMERROR	N/A	Output	AHB master output signals	High
GNDWPRT2	N/A	Output	This signal reflects the contents of the GSC.GNDP2 register	High
GNDWPRT1	N/A	Output	This signal reflects the contents of the GSC.GNDP1 register	High
PMWPRT4	N/A	Output	This signal reflects the contents of the PSC.PMWP4 register	High
PMWPRT3	N/A	Output	This signal reflects the contents of the PSC.PMWP3 register	High
PMWPRT2	N/A	Output	This signal reflects the contents of the PSC.PMWP2 register	High
PMWPRT1	N/A	Output	This signal reflects the contents of the PSC.PMWP1 register	High

* see GRLIB IP Library User's Manual

136.16 Signal definitions and reset values

The signals and their reset values are described in table 2066.

*Table 2066.*Signal definitions and reset values

Signal name	Type	Function	Active	Reset value
txd[]	Output	UART transmit data line	-	Logical 1
rtsn[]	Output	Ready To Send	Low	Logical 1
rxd[]	Input	UART receive data line	-	-
ctsn[]	Input	Clear To Send	Low	-

136.17 Timing

The timing waveforms and timing parameters are shown in figure 341 and are defined in table 2067.

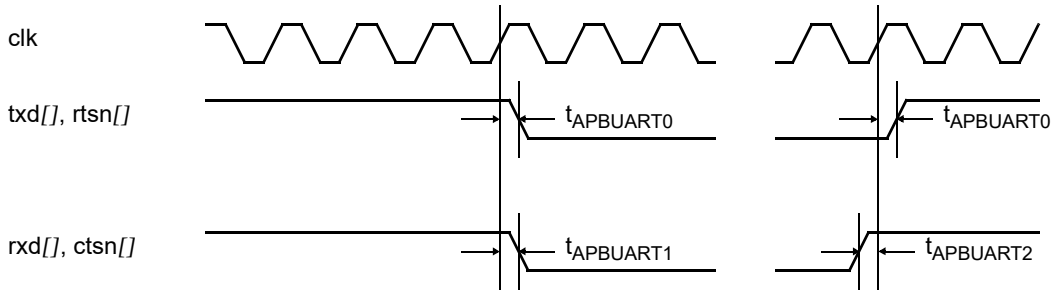


Figure 341. Timing waveforms

*Table 2067.*Timing parameters

Name	Parameter	Reference edge	Min	Max	Unit
$t_{APBUART0}$	clock to output delay	rising *clk* edge	TBD	TBD	ns
$t_{APBUART1}$	input to clock hold	rising *clk* edge	-	-	ns
$t_{APBUART2}$	input to clock setup	rising *clk* edge	-	-	ns

Note: The *ctsn[]* and *rxd[]* inputs are re-synchronized internally. These signals do not have to meet any setup or hold requirements.

136.18 Library dependencies

Table 2068 shows libraries that should be used when instantiating the core.

*Table 2068.*Library dependencies

Library	Package	Imported unit(s)	Description
GRLIB	AMBA	Signals	APB signal definitions
TMTC	GRRM	Signals, component	Signal and component declaration

136.19 Instantiation

This example shows how the core can be instantiated.

```
library ieee;
use ieee.std_logic_1164.all;

library grlib;
use grlib.amba.all;
```

```
library gaisler;
use gaisler.grreconfigmodule.all;
entity grrm_ex is
  port (
    clk : in std_ulogic;
    rstn : in std_ulogic;

    -- external alarms
    extalarm:   in std_logic_vector(gNOEXT-1 downto 0);
    -- external time
    exttime:    in std_logic_vector(54 downto 0);

    -- packetwire interface
    pktwready:  in  std_logic;
    pktwbusy_n: in  std_logic;
    pktwclk:    out std_logic;
    pktwdata:   out std_logic;
    pktwvalid:  out std_logic;
    pktwabort:  out std_logic;
    -- health communication
    healthrx:   in  std_logic;
    healthtx:   out std_logic;
    );
end;

architecture rtl of apbuart_ex is

  -- APB signals
  signal apbi  : apb_slv_in_type;
  signal apbo  : apb_slv_out_vector := (others => apb_none);

begin

  -- AMBA Components are instantiated here
   ...
rm0: grrm
      generic map (
         gCONFADDR       => 16#000400#,
         gSEQADDR        => 16#000#,
         gLOGADDR        => 16#400001#,
         gNOEXT          => 16,
         gALARMPRE       => 16,
         gALARMDLY       => 16,
         gWATCHDOG       => 2,
         gWDOGPRE        => 16,
         gWDOGDLY        => 8,
         gSWALARM        => 2,
         gNOSW           => 7,
         gCOMPRE         => 24,
         gINITDLY        => 16,
         gSYSTEMCLK      => 50000000,
         gBAUD           => 115200,
         gPROG           => 1,
         gHEALTH         => 1,
         gHTHBITS        => 16,
         gBUFTYPE        => 0,
         gPINDEX         => 10,
         gHINDEX         => 5,
         gPADDR          => 10,
         gPMASK          => 16#FFF#,
         gPIRQ           => 10)
      port map (
        rstn             => rstn,
        clk              => clk,
        apbi             => apbi,
        apbo             => apbo(10),
        ahbmi            => ahbmi,
        ahbmo            => ahbmo(5),
        extalarm         => extalarm,
        exttime          => exttime,
        pktwclk          => pktwclk,
```

```
pktwdata         => pktwdata,
pktwvalid        => pktwvalid,
pktwabort        => pktwabort,
pktwready        => pktwready,
pktwbusy_n       => pktwbusy_n,
healthrx         => healthrx,
healthtx         => healthtx,
master           => dipsw(6),
initconf         => dipsw(7),
confdone         => '0',
alarm_evt        => open,
alarmlog         => alarmlog,
rmerror          => rmerror,
gndwprt2         => gndwprt2,
gndwprt1         => gndwprt1,
pmwprt4          => pmwprt4,
pmwprt3          => pmwprt3,
pmwprt2          => pmwprt2,
pmwprt1          => pmwprt1);
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