

**Project Name: PecosII  
(IDX80)**

**PCB Serial Number:  
LA-3291**


# PecosII Schematics Document

**Intel Merom Dual Core LV1.33G&1.5G  
/Yonah Single Core ULV 1.06G&1.2G + Calistoga GM + ICH7-M**

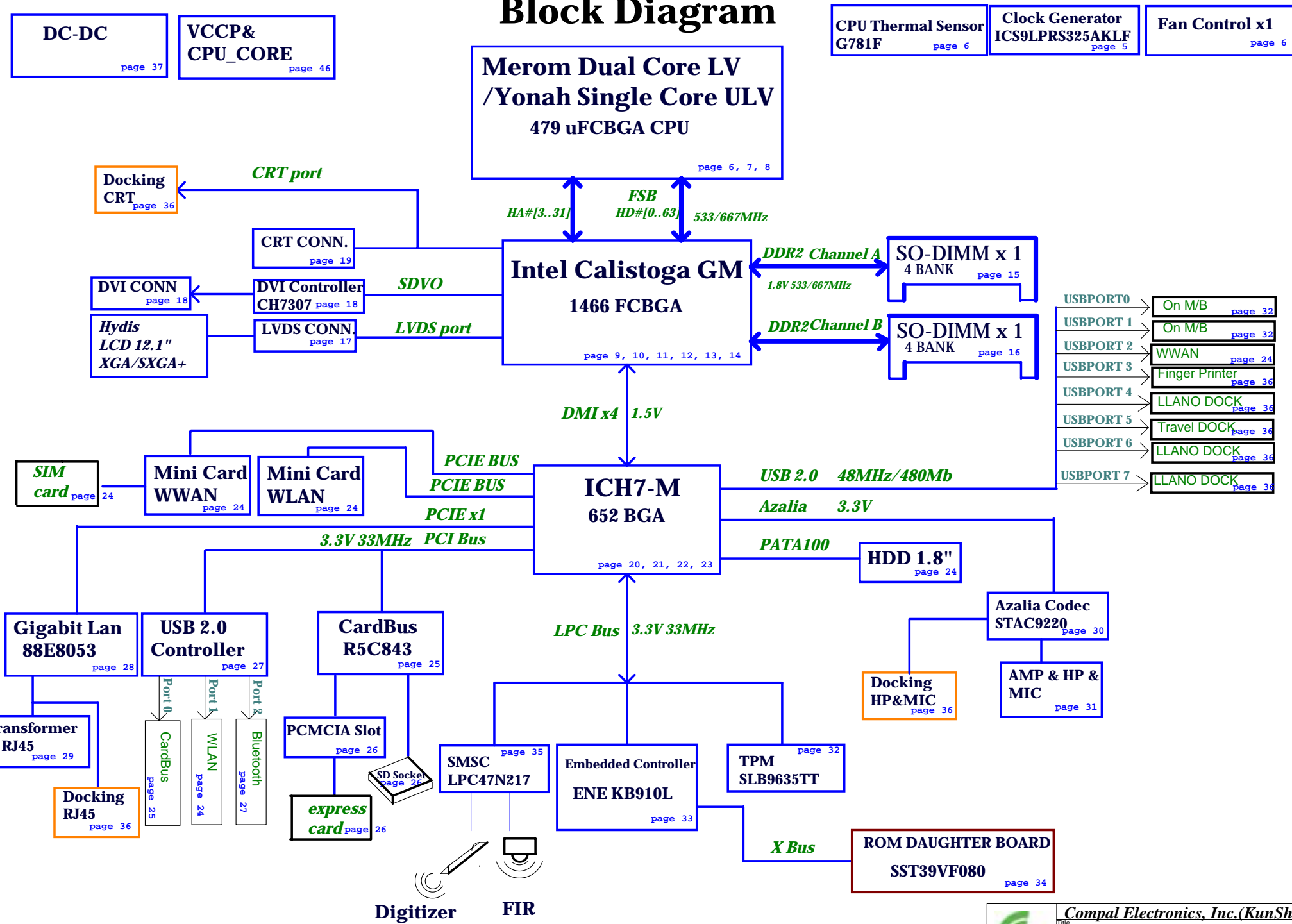
**2007-01-08**

**REV: X0.5**


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	Title <b>Cover Sheet</b>	
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# Block Diagram



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		Title Block Diagram	Document Number PecosII-JDX80-LA 3291
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## External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
CARD BUS	AD20	2	A,B
USB controller	AD21	0	E,F,G

### Symbol Note

 : means Digital Ground

 : means Analog Ground

 : Question Area Mark.(Wait check)

@: means don't stuff, just reserve

DB@: means jsut stuff when Mini-PCI E Debug card function enable

DVI\_7307@: means just stuff when use CH7307 controller

DVI\_1362@: means just stuff when use S11362 controller

9220@: means just populate when mount 9220 on board;  
depopulate when mount 9228 on board

9228@: means just populate when mount 9228 on board;  
depopulate when mount 9220 on board

LV@: means just populate when mount Merom/Yonah LV DC CPU on board;  
depopulate when mount Yonah ULV SC CPU on board

Buffer@: means just populate when buffer generate V\_DDR\_MCH\_REF;  
depopulate when 1.8V divider generate V\_DDR\_MCH\_REF

1.8\_divider@: means just populate when 1.8V divider generate V\_DDR\_MCH\_REF;  
depopulate when buffer generate V\_DDR\_MCH\_REF

1@: means just populate 0ohm resistors on board;

2@: means just populate MAX9890 & related components on board;

3220@: means populate 0ohm resistors when mount Agilent 3220,unpopulate 0ohm resistors when mount other

Power Management table

Signal \ State	+12VALW +5VALW +3VALW +3V_LAN	+1.8V	+5VS +3VS +1.8VS +2.5VS +1.5VS +0.9VS +VCCP +CPU_CORE
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON notel	ON	OFF
S5 S4/AC	ON notel	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF


Note1 : +3V\_LAN is ON only with AC power available, otherwise it is OFF.

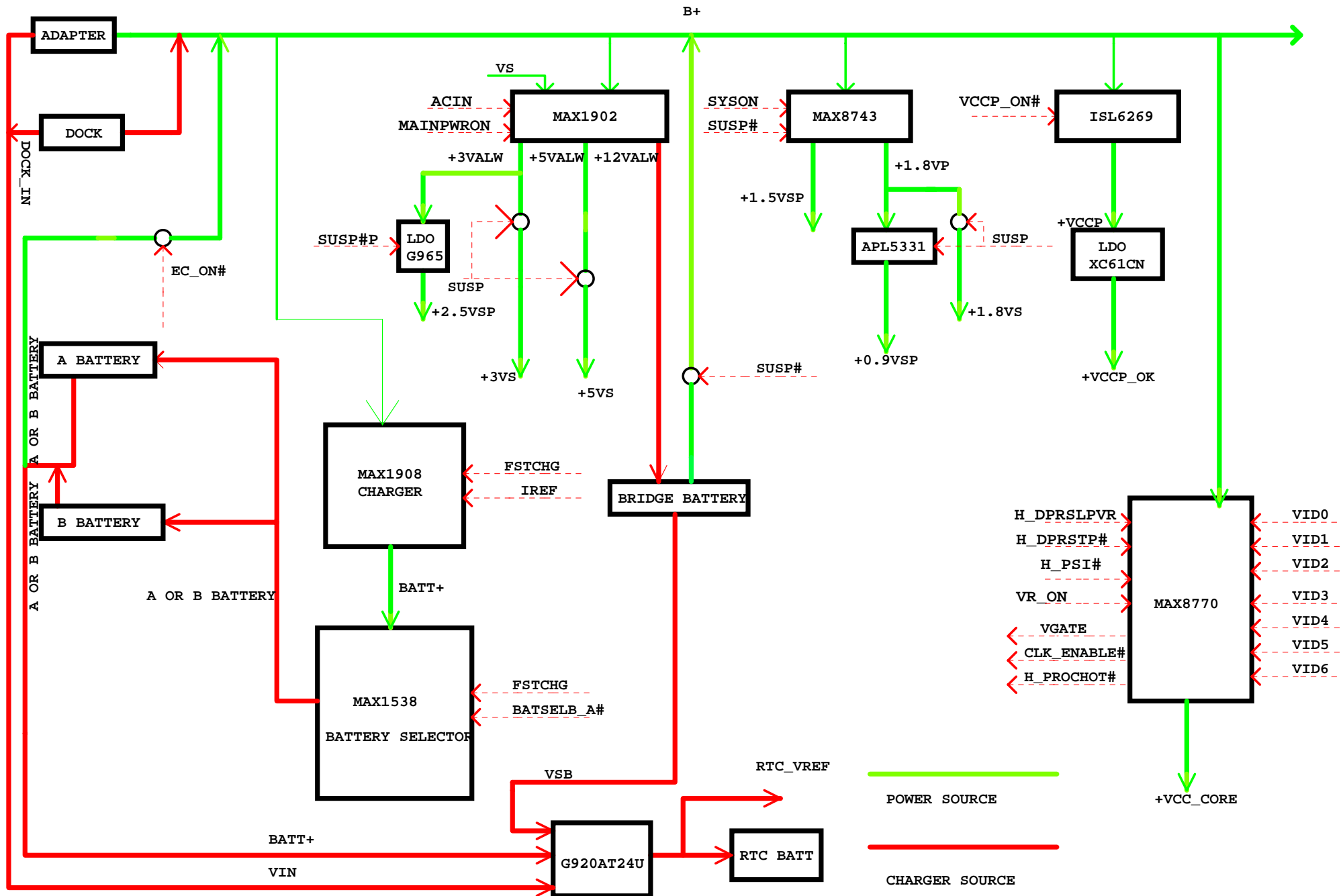
### Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V power rail for Processor I/O and MCH core power	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDRII Vtt	ON	OFF	OFF
+1.5VS	1.5V switched power rail for PCI-E interface	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail for MCH video PLL	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON
+3V_LAN	3.3V LAN power rail	ON	ON*	ON*


Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

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	Notes&Revision		
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Cust.ord	<b>PecosII-IDX80-LA3291</b>	X 0.5	
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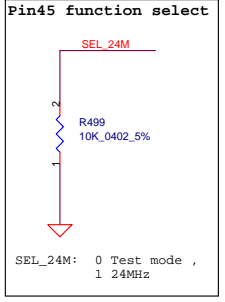
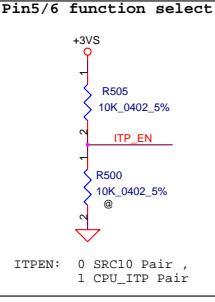
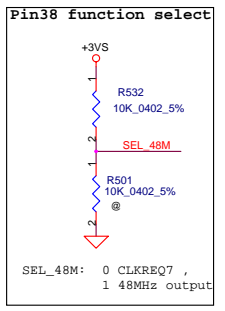
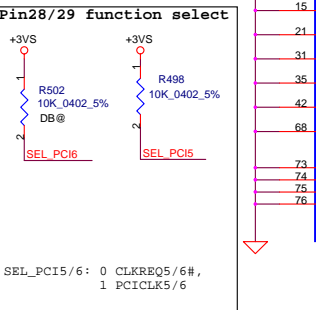
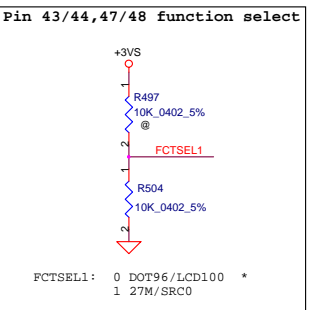
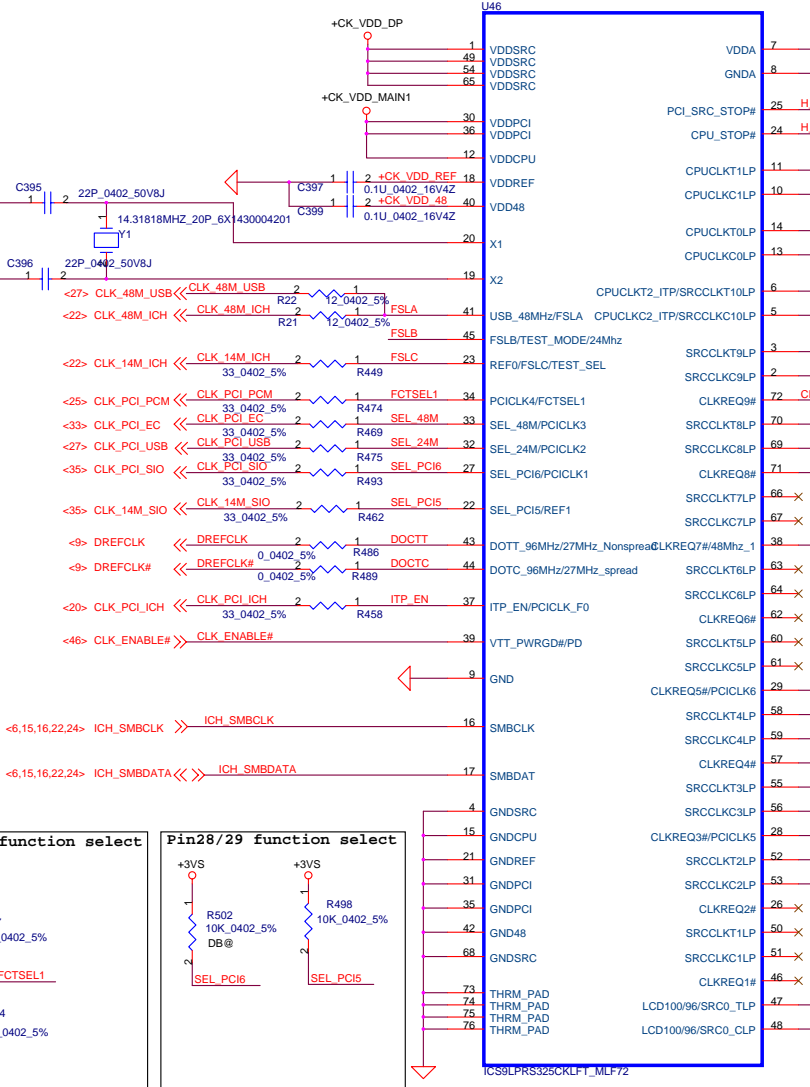
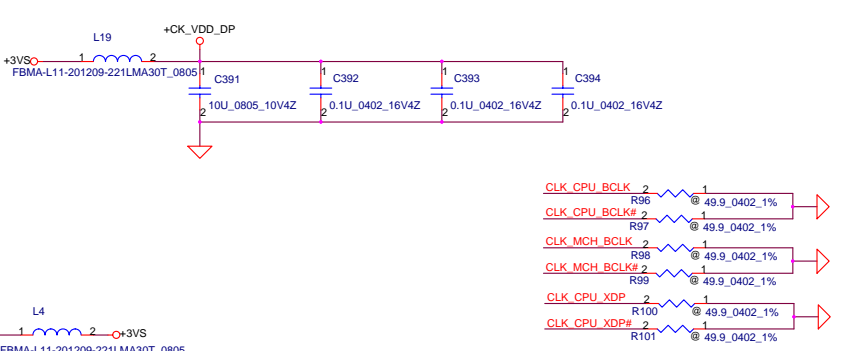
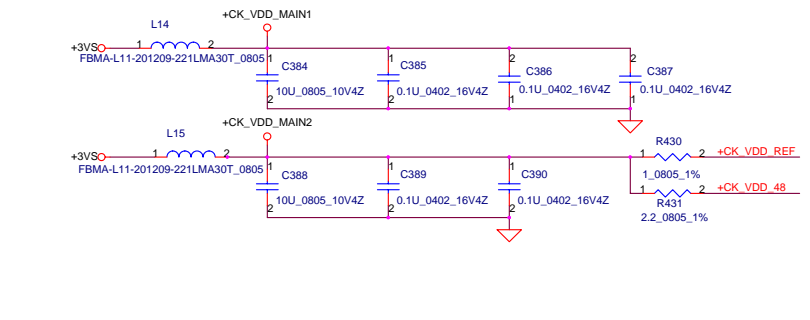
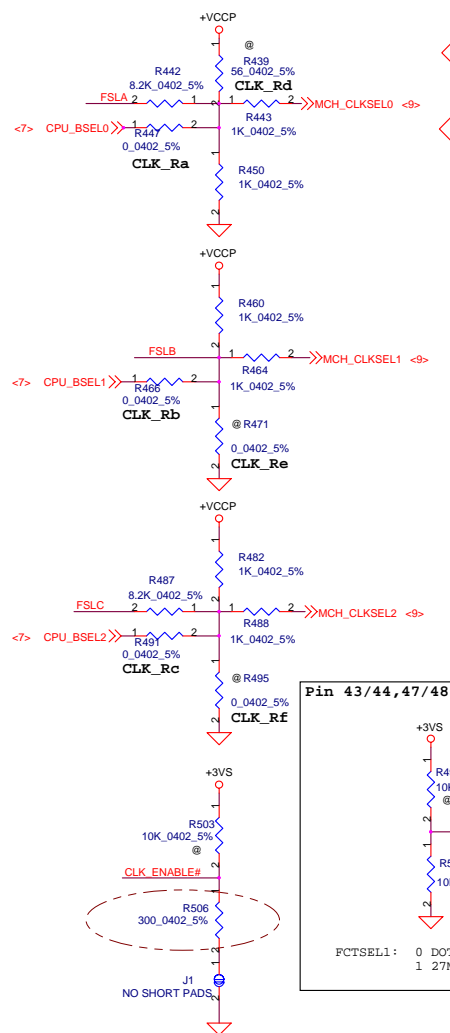
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	<b>Compal Electronics, Inc. (KunShan)</b>		
	Title <b>Power rail</b>	Document Number <b>PecosII-IDX80-LA3291</b>	
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FSLC	FSLB	FSLA	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

**FSB Frequency Select:**

CPU Driven	Stuff	CLK_Ra	CLK_Rb	CLK_Rc
*(Default)	No Stuff	CLK_Rd	CLK_Re	CLK_Rf
	533MHz	CLK_Ra	CLK_Rb	CLK_Rc
667MHz	Stuff	CLK_Rd	CLK_Rf	
	No Stuff	CLK_Ra	CLK_Rb	CLK_Rc



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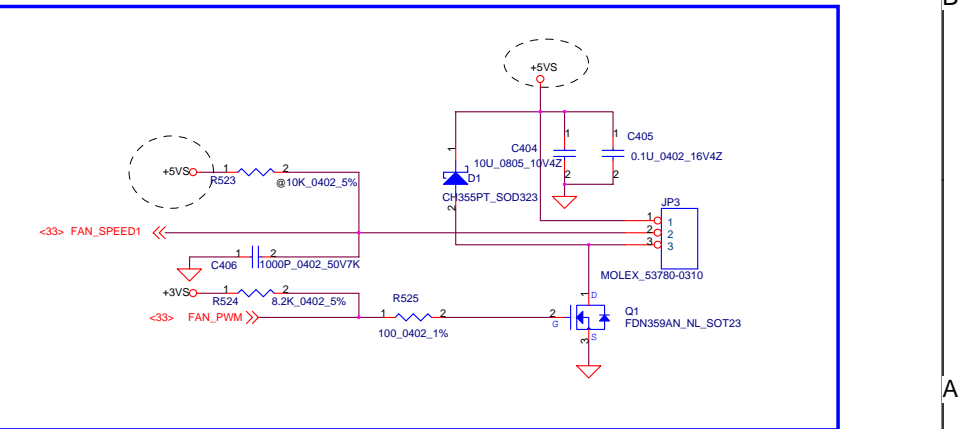
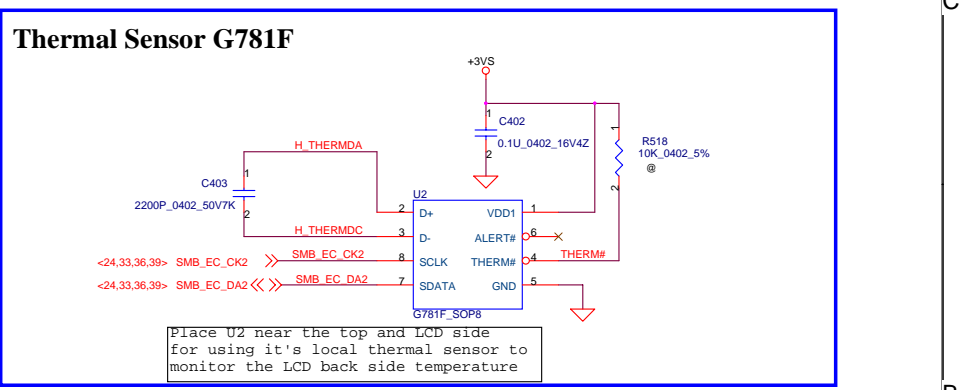
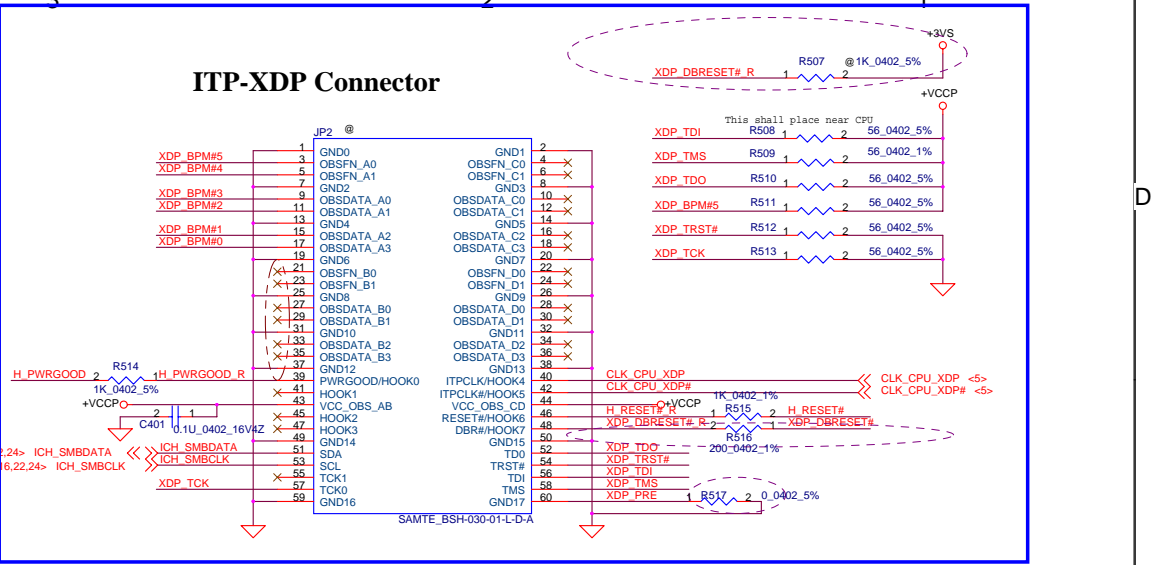
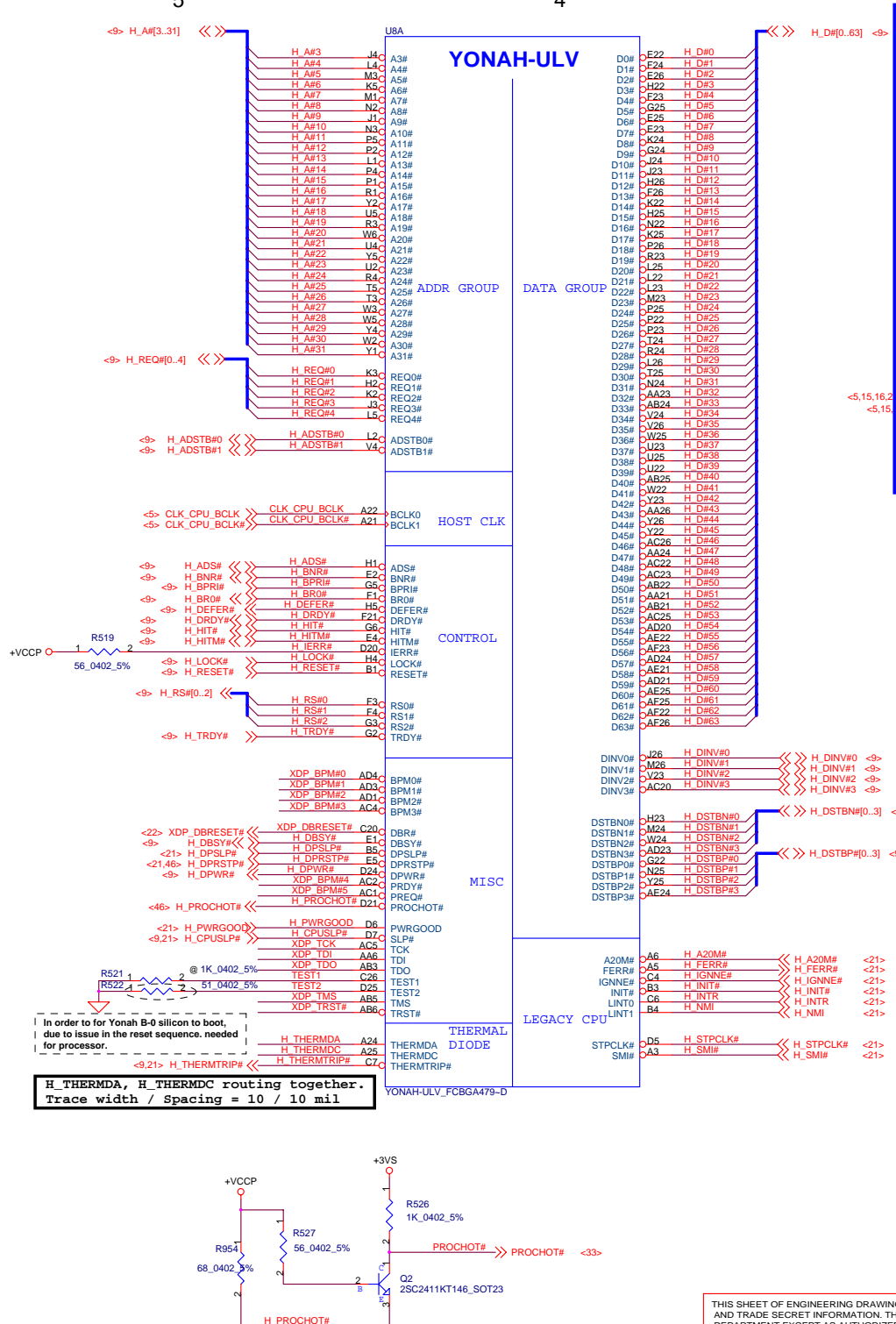
**Clock Generator**

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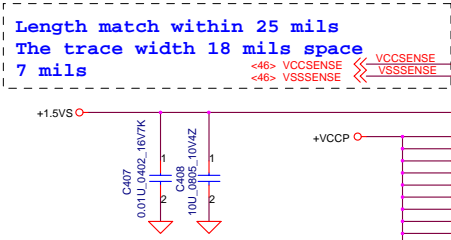
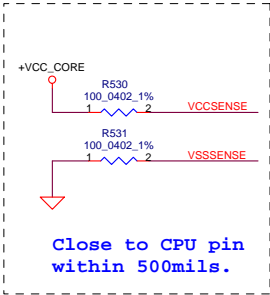
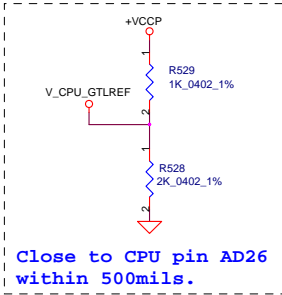
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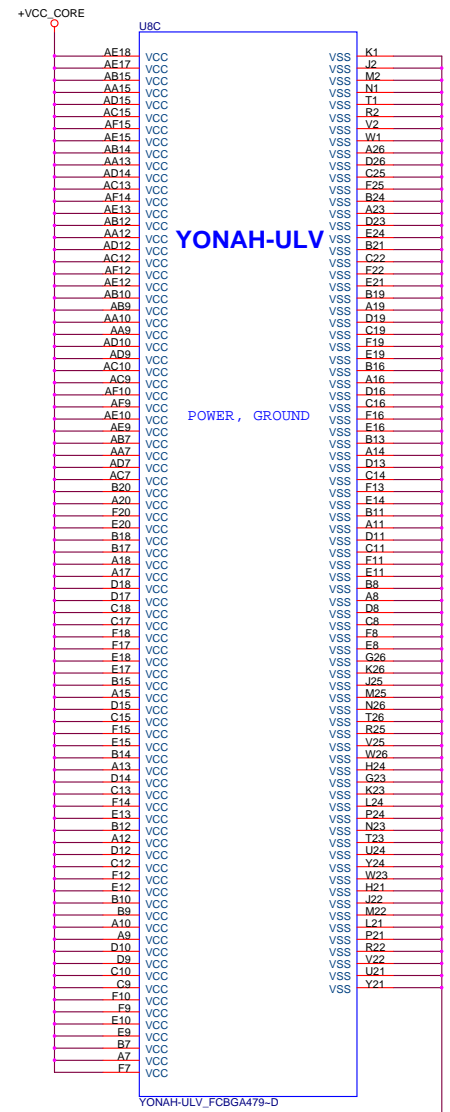
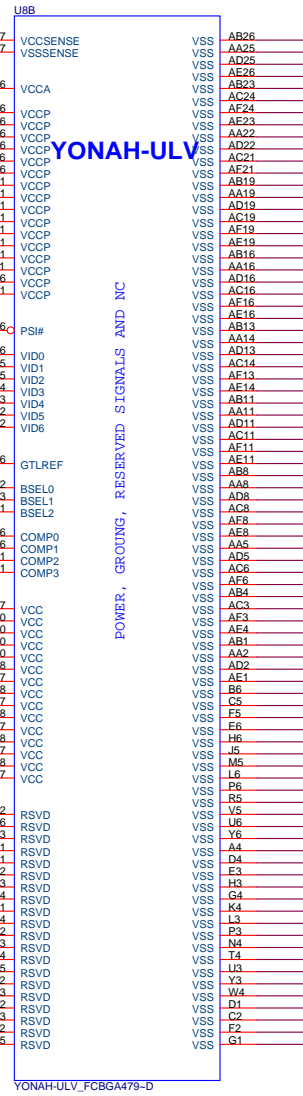
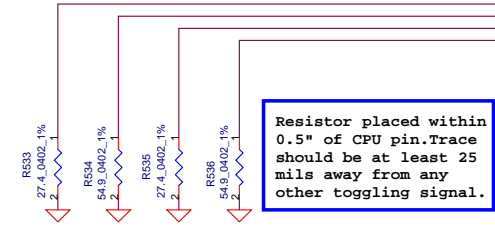


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CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

- <<46> H\_PSI# << H\_PSI# << AE6 << PSI#
- <<46> CPU\_VID0 << CPU\_VID0 << AD6 << VID0
- <<46> CPU\_VID1 << CPU\_VID1 << AE5 << VID1
- <<46> CPU\_VID2 << CPU\_VID2 << AE4 << VID2
- <<46> CPU\_VID3 << CPU\_VID3 << AE3 << VID3
- <<46> CPU\_VID4 << CPU\_VID4 << AE2 << VID4
- <<46> CPU\_VID5 << CPU\_VID5 << AE1 << VID5
- <<46> CPU\_VID6 << CPU\_VID6 << AE2 << VID6
- V\_CPU\_GTLREF << AD26 << GTLREF
- <<5> CPU\_BSEL0 << CPU\_BSEL0 << B22 << BSEL0
- <<5> CPU\_BSEL1 << CPU\_BSEL1 << B23 << BSEL1
- <<5> CPU\_BSEL2 << CPU\_BSEL2 << C21 << BSEL2
- COMP0 << R26 << COMP0
- COMP1 << U26 << COMP1
- COMP2 << U11 << COMP2
- COMP3 << V1 << COMP3



YONAH-ULV\_FCBGA479-D

YONAH-ULV\_FCBGA479-D

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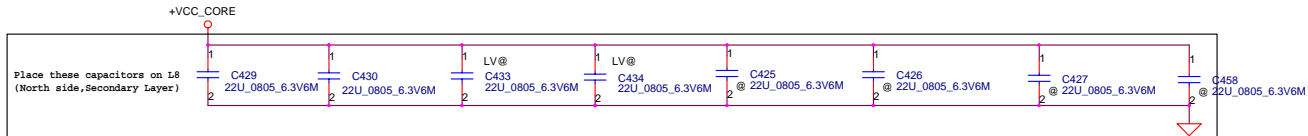
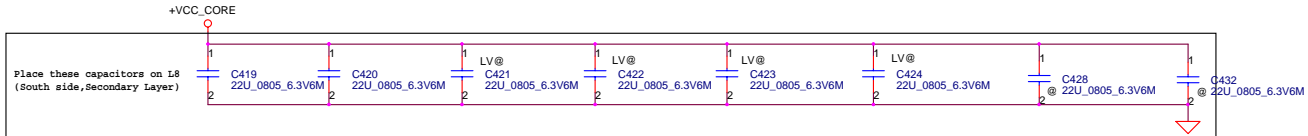
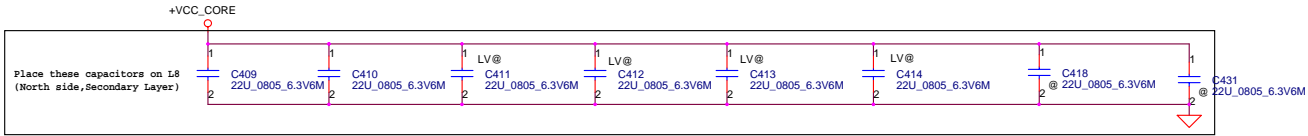
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**PecosII-IDX80-LA3291**

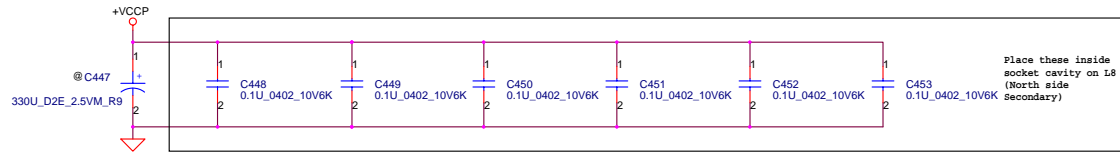
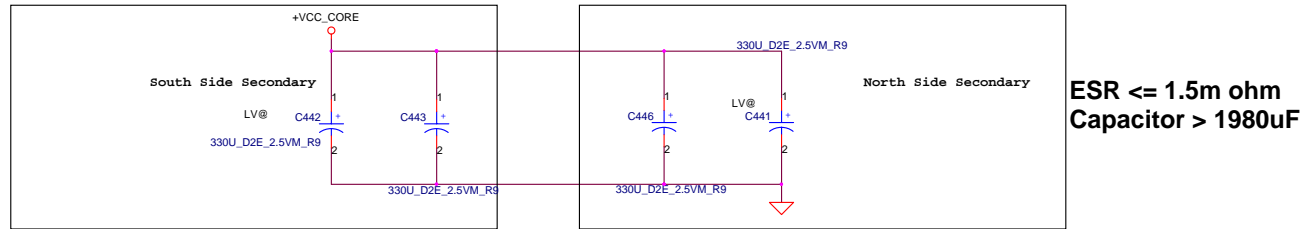
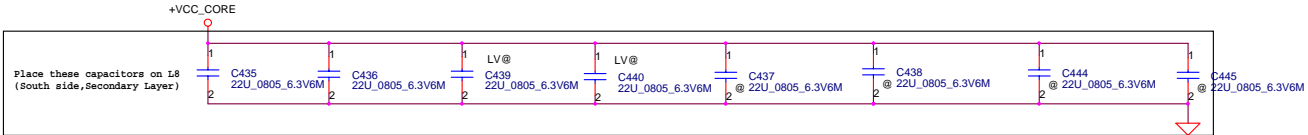
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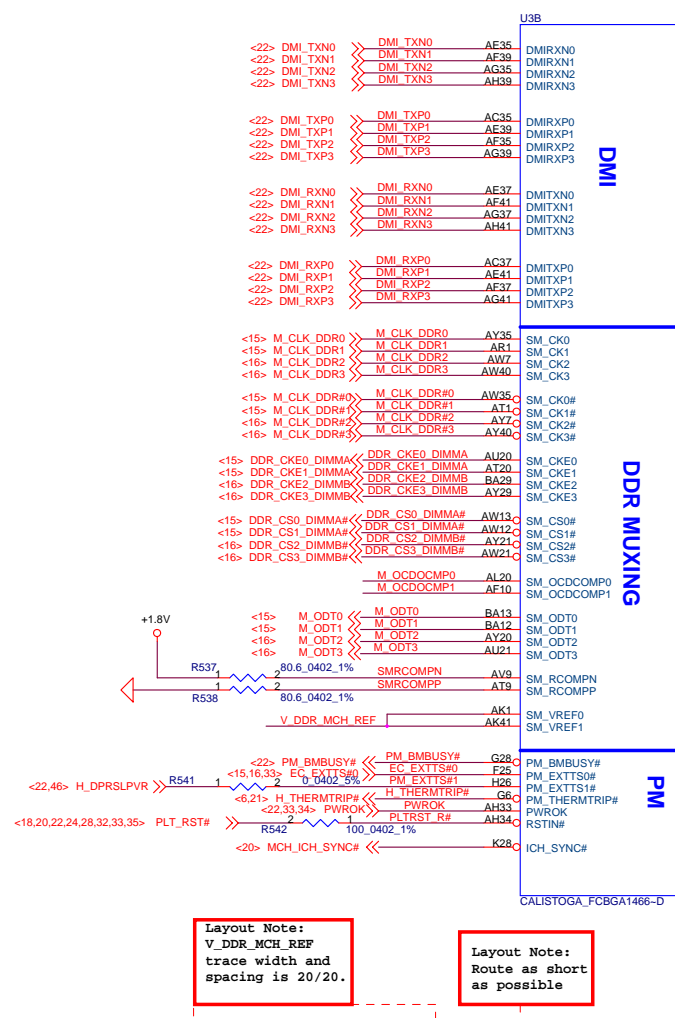
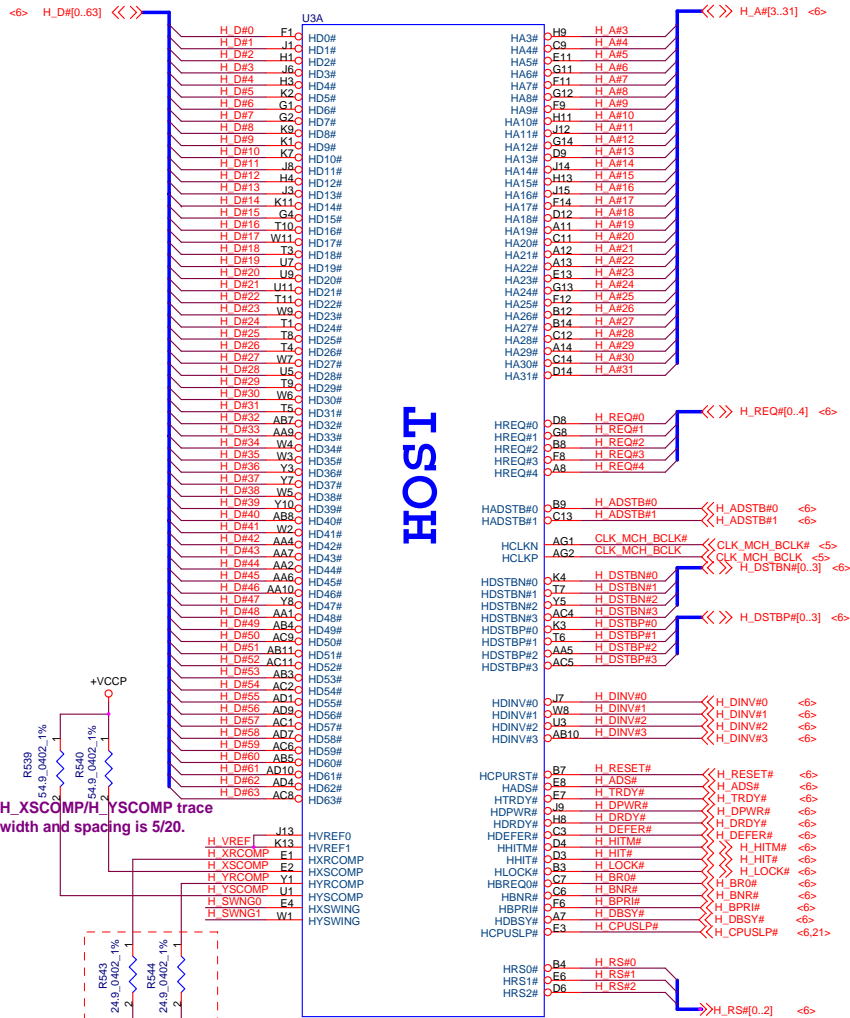
**Mid Frequency Decoupling**



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	Yonah bypass	
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H\_XSCOMP/H\_YSCOMP trace width and spacing is 5/20.

Layout Note:  
H\_XRCOMP / H\_YRCOMP / H\_VREF / H\_SWNG0 / H\_SWNG1 trace width and spacing is 10/20.

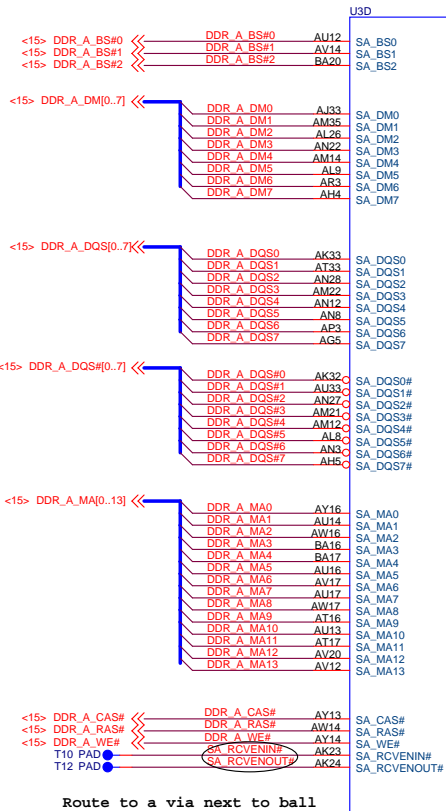
Layout Note:  
V\_DDR\_MCH\_REF trace width and spacing is 20/20.

Layout Note:  
Route as short as possible

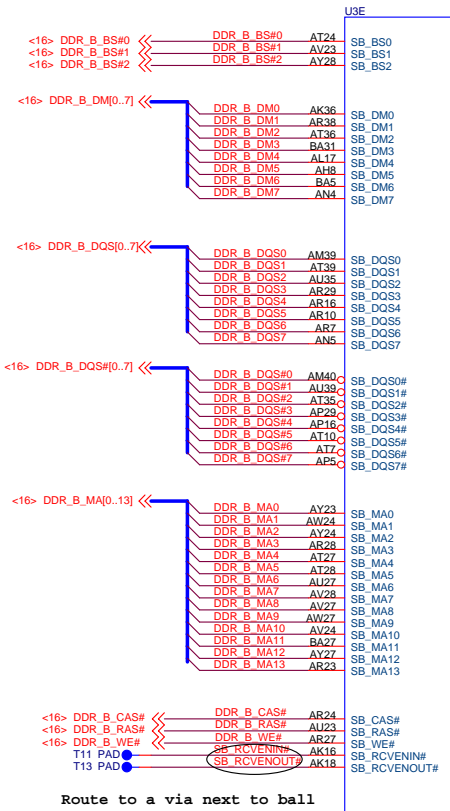
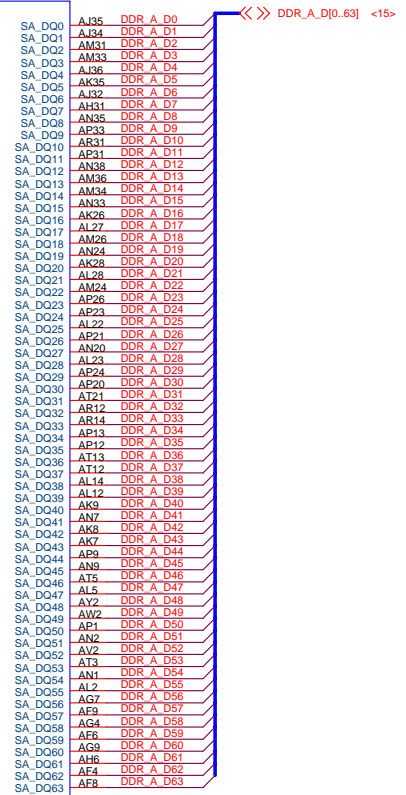
Stuff R546 & R547 for A1 Calistoga

Use +1.8V divide voltage for V\_DDR\_MCH\_REF, R545/R548 use 100\_0402\_1%  
Use buffer to generate V\_DDR\_MCH\_REF, R545/R548 use 1K\_0402\_1%

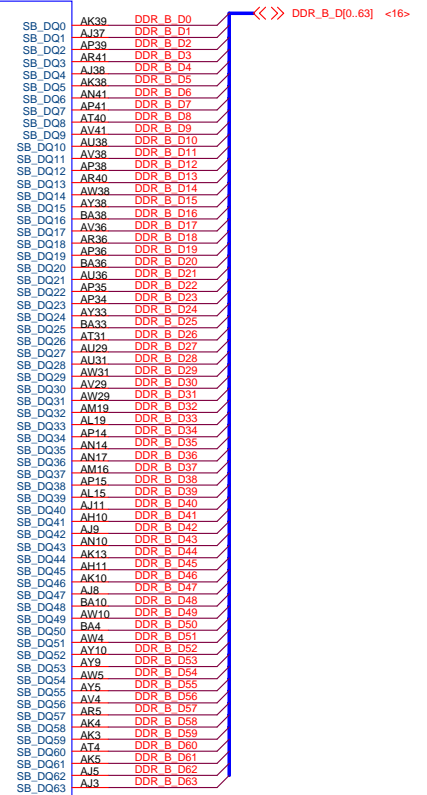




DDR SYS MEMORY A



DDR SYS MEMORY B



CALISTOGA\_FCBGA1466-D

CALISTOGA\_FCBGA1466-D

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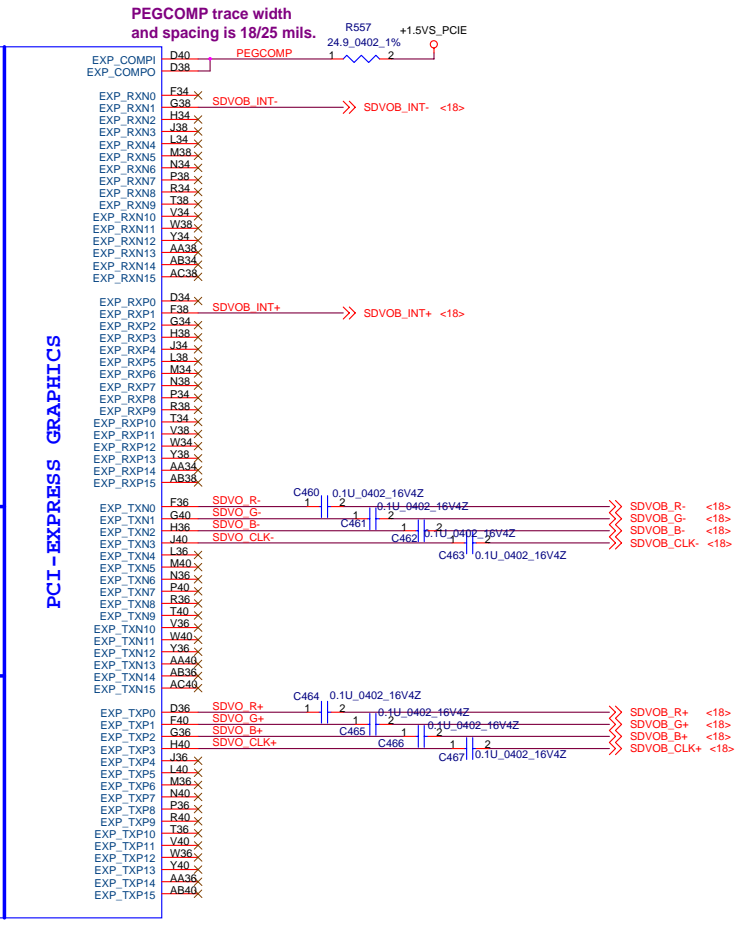
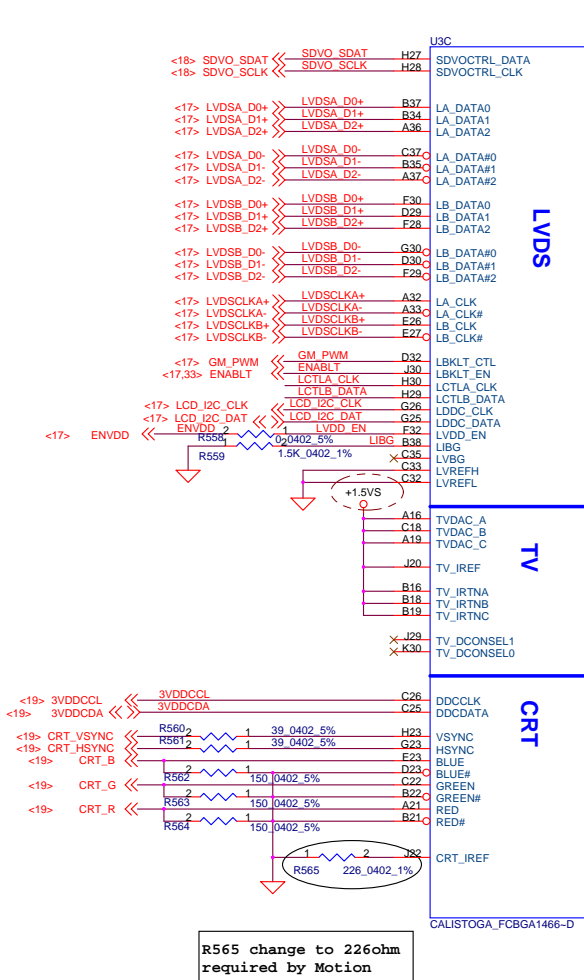
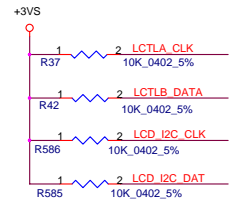
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Title: Calistoga2/6-DDRA&B

Size: X 0.5

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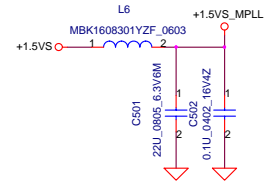
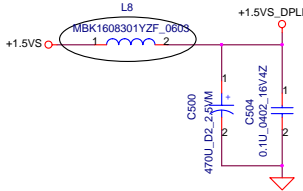
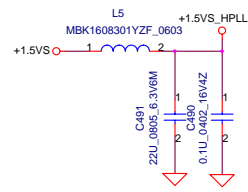
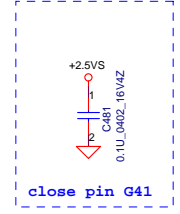
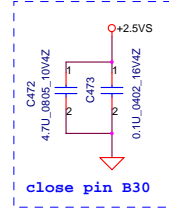
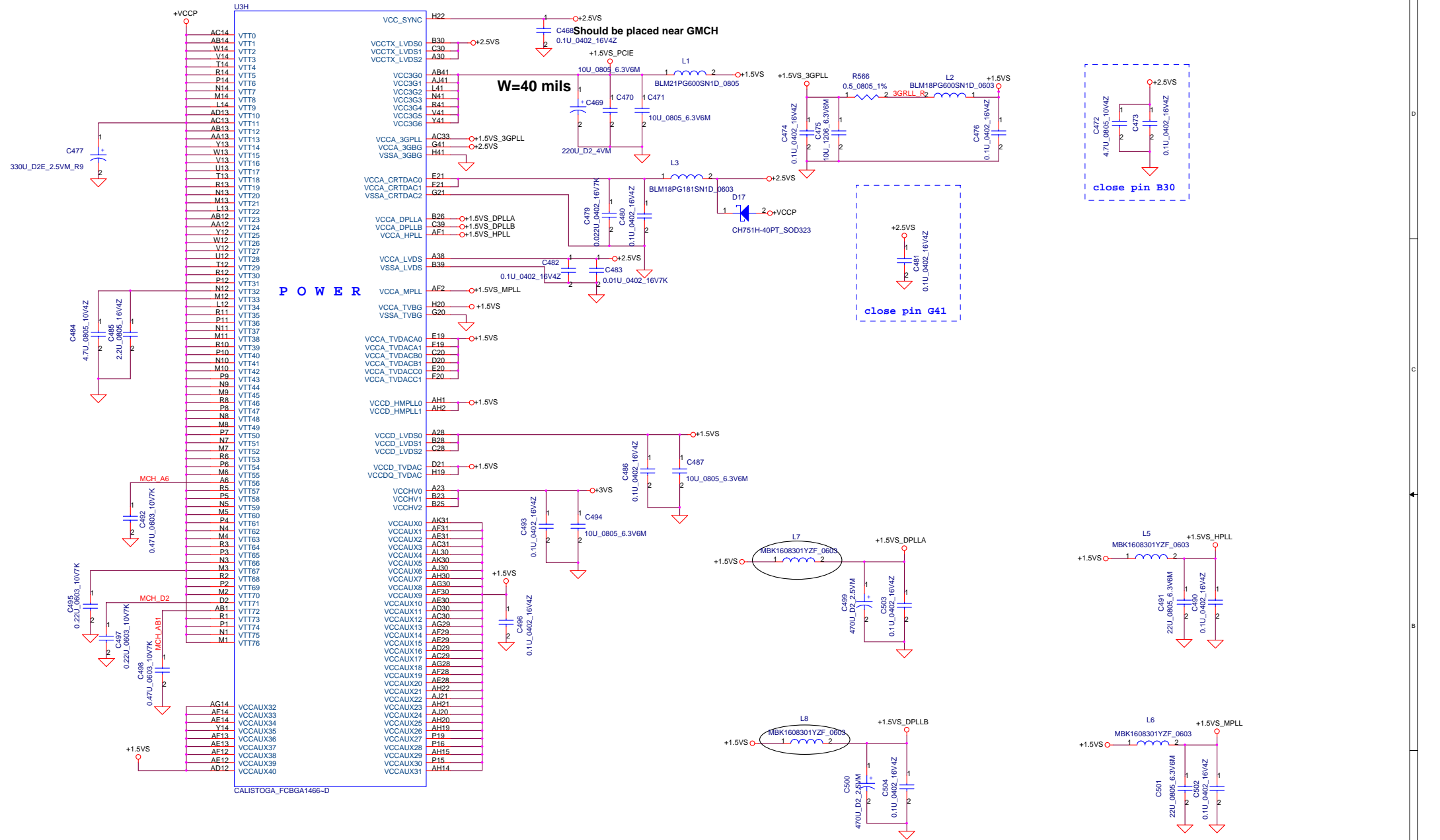
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PEGCOMP trace width and spacing is 18/25 mils.

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Title <b>Calistoga3/6-VGA/LVDS</b>			
Size	Document Number	Date	Rev
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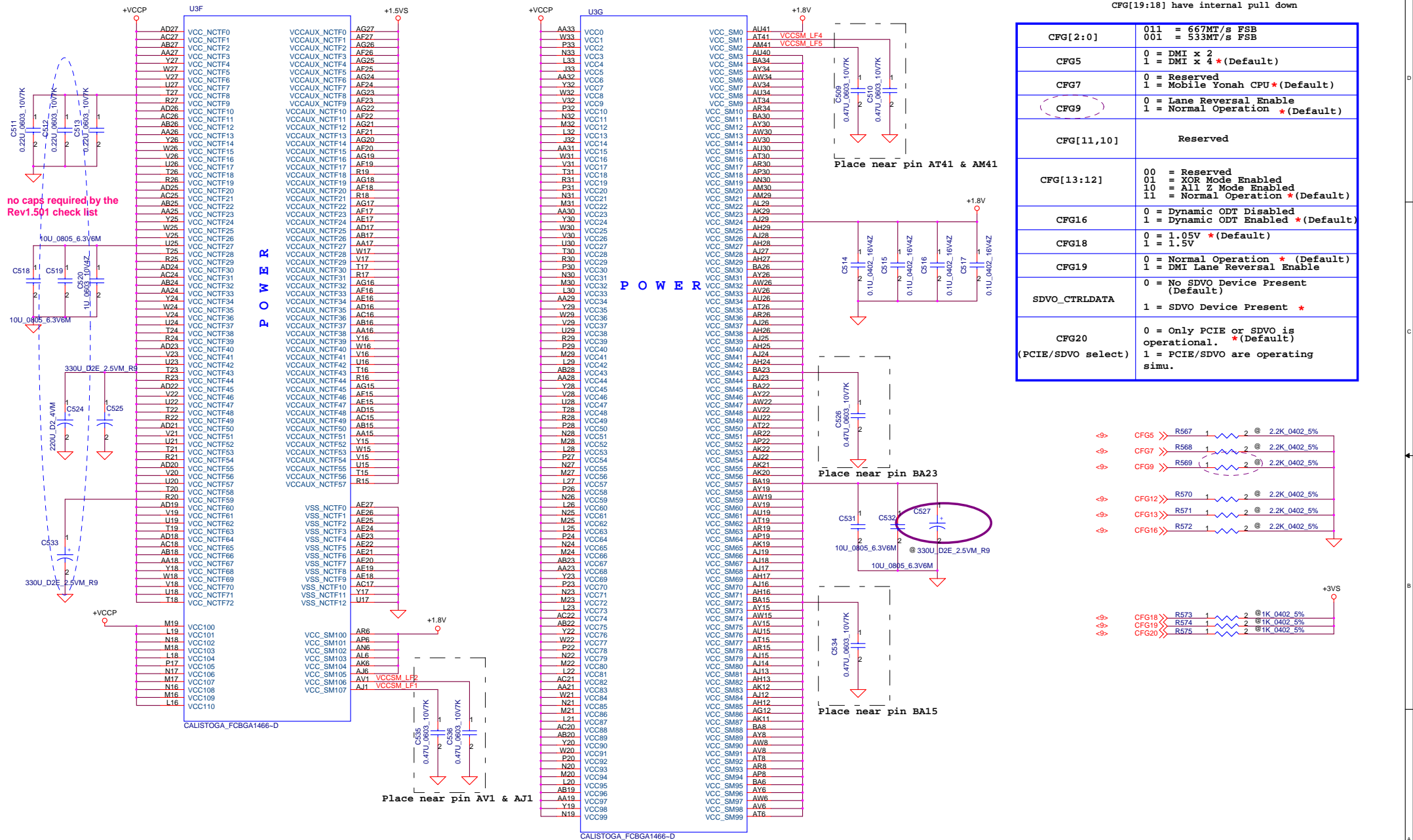
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	Calistoga/4/6-PWR	
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# Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG[11,10]	Reserved
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.05V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present (Default) 1 = SDVO Device Present *
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



no caps required by the Rev1.501 check list

## POWER

Place near pin AT41 & AM41

Place near pin BA23

Place near pin BA15

- <-> CFG5 >> R567 1 2 @ 2.2K 0402 5%
- <-> CFG7 >> R568 1 2 @ 2.2K 0402 5%
- <-> CFG9 >> R569 1 2 @ 2.2K 0402 5%
- <-> CFG12 >> R570 1 2 @ 2.2K 0402 5%
- <-> CFG13 >> R571 1 2 @ 2.2K 0402 5%
- <-> CFG16 >> R572 1 2 @ 2.2K 0402 5%
- <-> CFG18 >> R573 1 2 @ 1K 0402 5%
- <-> CFG19 >> R574 1 2 @ 1K 0402 5%
- <-> CFG20 >> R575 1 2 @ 1K 0402 5%

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**Compal Electronics, Inc. (KunShan)**

Title: Calistoga5/6-PWR/GND

Size: Document Number

Customer: PecosII-JDX80-LA3291

Date: Monday, January 08, 2007

Rev: X.0.5

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U3I		AE34	
AC41	VSS0	VSS100	G32
AA41	VSS1	VSS101	AC34
V41	VSS2	VSS102	C34
T41	VSS3	VSS103	YV33
P41	VSS4	VSS104	AV33
M41	VSS5	VSS105	AR33
J41	VSS6	VSS106	AE33
F41	VSS7	VSS107	H33
AV40	VSS8	VSS108	Y33
AP40	VSS9	VSS109	V33
AN40	VSS10	VSS110	T33
AK40	VSS11	VSS111	R33
A40	VSS12	VSS112	M33
AH40	VSS13	VSS113	H33
AG40	VSS14	VSS114	G33
AE40	VSS15	VSS115	F33
E40	VSS16	VSS116	D33
B40	VSS17	VSS117	B33
AY39	VSS18	VSS118	AH32
AV39	VSS19	VSS119	AG32
AR39	VSS20	VSS120	AF32
AN39	VSS21	VSS121	AE32
AK39	VSS22	VSS122	AC32
AC39	VSS23	VSS123	AB32
AB39	VSS24	VSS124	G32
AA39	VSS25	VSS125	B32
Y39	VSS26	VSS126	AY31
W39	VSS27	VSS127	AV31
V39	VSS28	VSS128	AJ31
T39	VSS29	VSS129	AI31
R39	VSS30	VSS130	AG31
P39	VSS31	VSS131	AB31
N39	VSS32	VSS132	Y31
M39	VSS33	VSS133	AB30
J39	VSS34	VSS134	E30
H39	VSS35	VSS135	AT29
G39	VSS36	VSS136	AM29
F39	VSS37	VSS137	AB29
E39	VSS38	VSS138	T29
D39	VSS39	VSS139	N29
AT38	VSS40	VSS140	K29
AM38	VSS41	VSS141	G29
AH38	VSS42	VSS142	E29
AG38	VSS43	VSS143	C29
AE38	VSS44	VSS144	B29
E38	VSS45	VSS145	A29
C38	VSS46	VSS146	BA28
AK37	VSS47	VSS147	AW28
AH37	VSS48	VSS148	AU28
AB37	VSS49	VSS149	AD28
AA37	VSS50	VSS150	AM28
Y37	VSS51	VSS151	U14
W37	VSS52	VSS152	AC28
V37	VSS53	VSS153	W28
T37	VSS54	VSS154	J28
R37	VSS55	VSS155	E28
P37	VSS56	VSS156	AP27
N37	VSS57	VSS157	AM27
M37	VSS58	VSS158	AK27
L37	VSS59	VSS159	J27
J37	VSS60	VSS160	G27
H37	VSS61	VSS161	F27
G37	VSS62	VSS162	C27
F37	VSS63	VSS163	B27
E37	VSS64	VSS164	AN26
D37	VSS65	VSS165	M26
AY36	VSS66	VSS166	K26
AV36	VSS67	VSS167	F26
AR36	VSS68	VSS168	D26
AN36	VSS69	VSS169	AK25
AK36	VSS70	VSS170	K25
AC36	VSS71	VSS171	H25
E36	VSS72	VSS172	H25
C36	VSS73	VSS173	E25
B36	VSS74	VSS174	D25
BA35	VSS75	VSS175	A25
AV35	VSS76	VSS176	BA24
AR35	VSS77	VSS177	AU24
AH35	VSS78	VSS178	AW23
AB35	VSS79	VSS179	AT23
AA35	VSS80	VSS180	AN23
Y35	VSS81	VSS181	AM23
W35	VSS82	VSS182	AI23
V35	VSS83	VSS183	AC23
T35	VSS84	VSS184	W23
R35	VSS85	VSS185	K23
P35	VSS86	VSS186	J23
N35	VSS87	VSS187	F23
M35	VSS88	VSS188	C23
J35	VSS89	VSS189	AA22
H35	VSS90	VSS190	K22
G35	VSS91	VSS191	G22
F35	VSS92	VSS192	F22
E35	VSS93	VSS193	E22
D35	VSS94	VSS194	D22
AK34	VSS95	VSS195	A22
AG34	VSS96	VSS196	BA21
AF34	VSS97	VSS197	AV21
	VSS98	VSS198	AR21
	VSS99	VSS199	


POWER

U3J		AG10	
AN21	VSS200	VSS280	AG10
AL21	VSS201	VSS281	AC10
AB21	VSS202	VSS282	LW10
Y21	VSS203	VSS283	L110
P21	VSS204	VSS284	BA9
K21	VSS205	VSS285	AW9
J21	VSS206	VSS286	AB9
H21	VSS207	VSS287	AH9
C21	VSS208	VSS288	AB9
AW20	VSS209	VSS289	Y9
AR20	VSS210	VSS290	R9
AM20	VSS211	VSS291	G9
AK20	VSS212	VSS292	E9
K20	VSS213	VSS293	A9
B20	VSS214	VSS294	AG8
A20	VSS215	VSS295	AD8
AC19	VSS216	VSS296	AA8
W19	VSS217	VSS297	U8
K19	VSS218	VSS298	K8
C19	VSS219	VSS299	CA
AM19	VSS220	VSS300	BA7
AH18	VSS221	VSS301	AV7
P18	VSS222	VSS302	AF7
H18	VSS223	VSS303	AL7
D18	VSS224	VSS304	AH7
A18	VSS225	VSS305	AF7
AY17	VSS226	VSS306	AC7
AR17	VSS227	VSS307	R7
AP17	VSS228	VSS308	G7
AM17	VSS229	VSS309	D7
AK17	VSS230	VSS310	AG6
Y16	VSS231	VSS311	AD6
AN16	VSS232	VSS312	AB6
AL16	VSS233	VSS313	Y6
J16	VSS234	VSS314	U6
F16	VSS235	VSS315	NE
C16	VSS236	VSS316	K6
AN15	VSS237	VSS317	H6
AM15	VSS238	VSS318	B6
AK15	VSS239	VSS319	AV5
N15	VSS240	VSS320	AF5
M15	VSS241	VSS321	AD5
L15	VSS242	VSS322	AY4
B15	VSS243	VSS323	AR4
A15	VSS244	VSS324	AP4
BA14	VSS245	VSS325	AL4
AT14	VSS246	VSS326	AJ4
AK14	VSS247	VSS327	Y4
AD14	VSS248	VSS328	U4
AA14	VSS249	VSS329	R4
U14	VSS250	VSS330	J4
K14	VSS251	VSS331	F4
H14	VSS252	VSS332	C4
E14	VSS253	VSS333	AV3
AV13	VSS254	VSS334	AW3
AR13	VSS255	VSS335	AV3
AN13	VSS256	VSS336	AL3
AM13	VSS257	VSS337	AH3
AK13	VSS258	VSS338	AG3
N13	VSS259	VSS339	AF3
AG13	VSS260	VSS340	AD3
P13	VSS261	VSS341	AC3
F13	VSS262	VSS342	AA3
D13	VSS263	VSS343	G3
B13	VSS264	VSS344	AT2
AY12	VSS265	VSS345	AR2
K12	VSS266	VSS346	AP2
H12	VSS267	VSS347	AK2
E12	VSS268	VSS348	AJ2
AD12	VSS269	VSS349	AD2
AA12	VSS270	VSS350	AB2
Y11	VSS271	VSS351	Y2
J11	VSS272	VSS352	U2
D11	VSS273	VSS353	T2
V11	VSS274	VSS354	N2
B11	VSS275	VSS355	J2
AV10	VSS276	VSS356	H2
AP10	VSS277	VSS357	F2
AL10	VSS278	VSS358	C2
AJ10	VSS279	VSS359	AL1
		VSS360	

POWER

CALISTOGA\_FCBGA1466-D

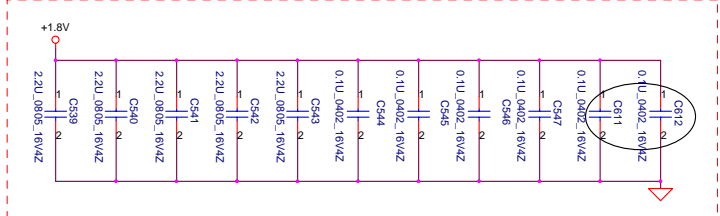
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	Calistoga6/6-GND	
	Size: 14	Document Number: PecosII-IDX80-LA3291
	Date: Monday, January 08, 2007	Sheet: 14 of 53

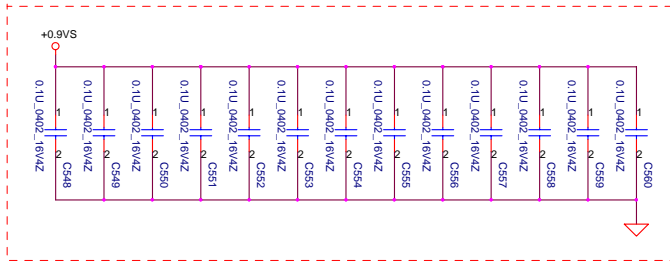
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 <10> DDR\_A\_D[0..63] <<>  
 <10> DDR\_A\_DM[0..7] <<>  
 <10> DDR\_A\_DQS[0..7] <<>  
 <10> DDR\_A\_MA[0..13] <<>

**Layout Note:**  
Place near JP4

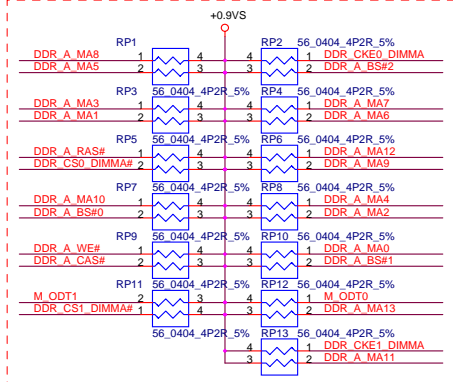
Add C611, C612 follow Motion's request



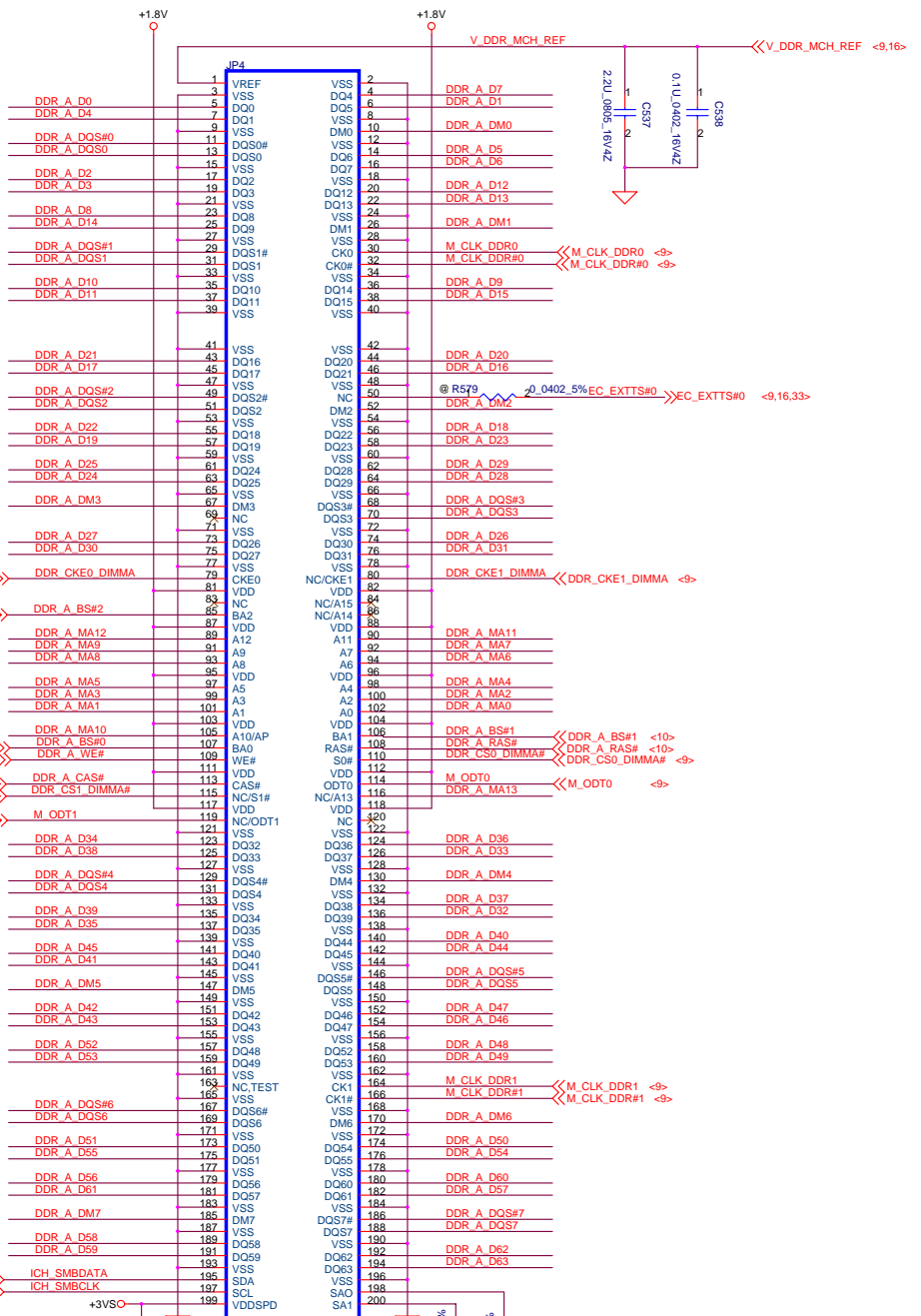
**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V



**Layout Note:**  
Place these resistor closely JP4, all trace length Max=1.5"



<5,6,16,22,24> ICH\_SMBDATA <<>  
 <5,6,16,22,24> ICH\_SMBCLK <<>



**SO-DIMM A REVERSE**



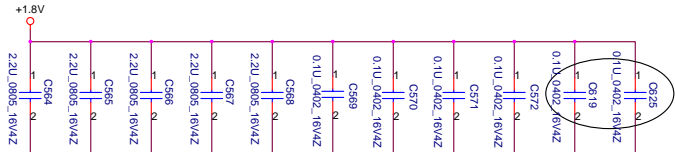
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 Title: **DDRII SO-DIMM A**  
 Size: Document Number  
 Cust. no: **PecosII-IDX80-LA3291**  
 Date: Monday, January 06, 2007 Sheet 15 of 53

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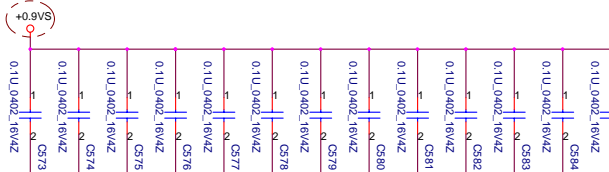
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 <10> DDR\_B\_D[0..63] <<>>  
 <10> DDR\_B\_DM[0..7] <<>>  
 <10> DDR\_B\_DQS[0..7] <<>>  
 <10> DDR\_B\_MA[0..13] <<>>

**Layout Note:**  
Place near JP5

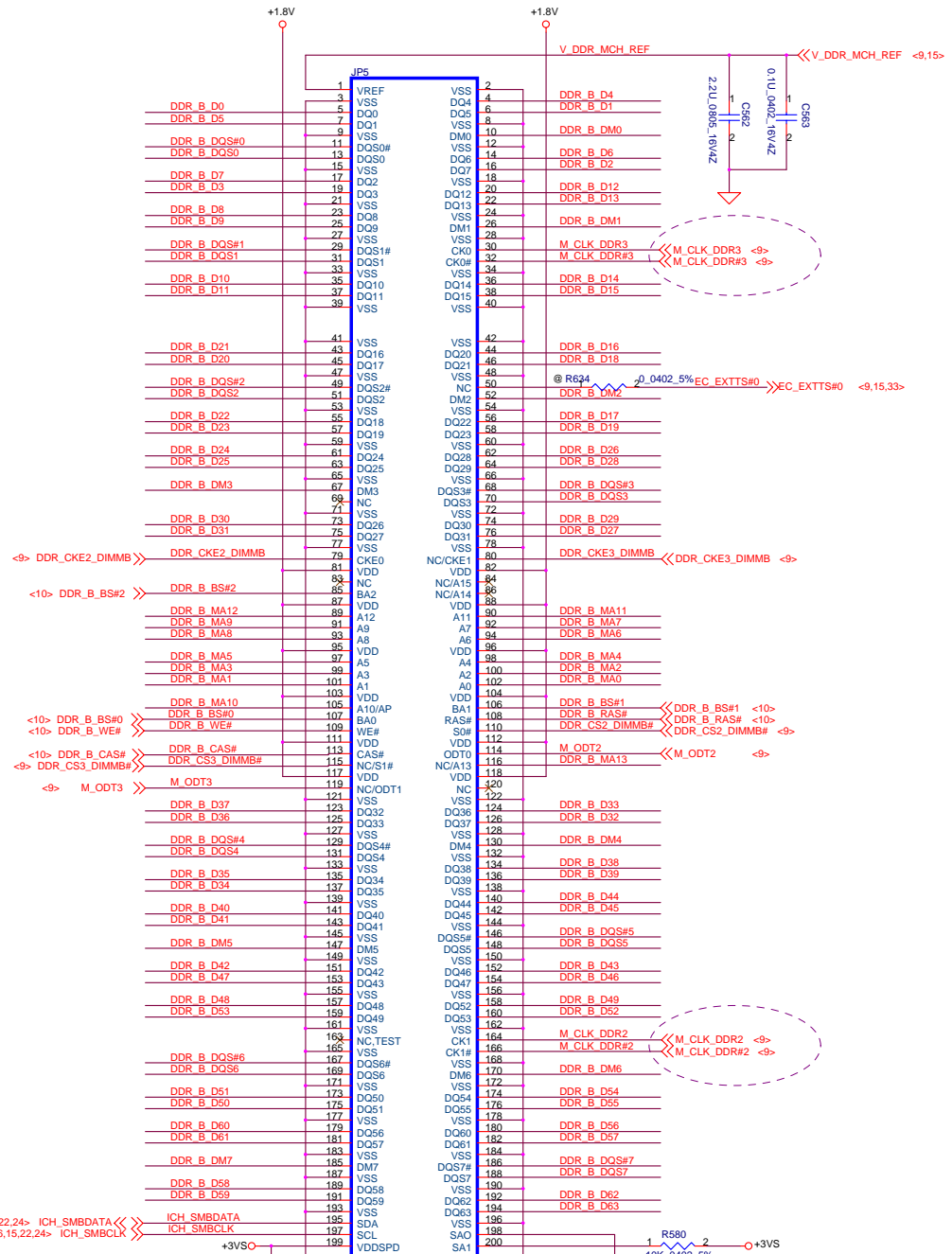
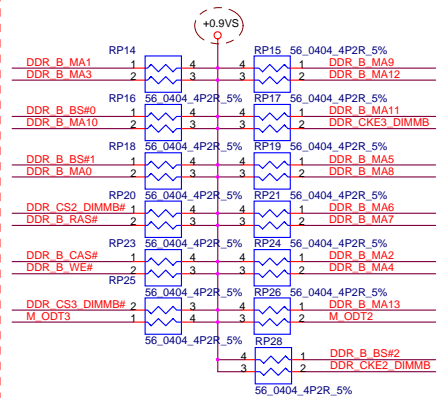
Add C619, C625 follow Motion's request



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V



**Layout Note:**  
Place these resistor closely JP10, all trace length Max<1.5"

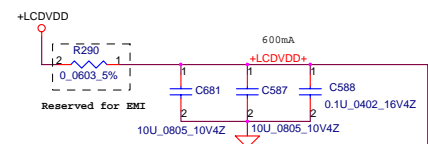
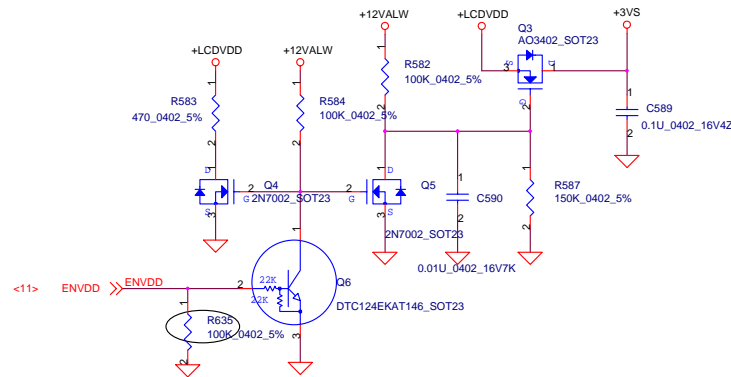


**SO-DIMM B STANDARD**

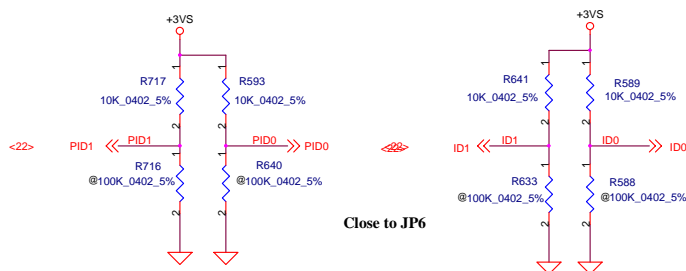
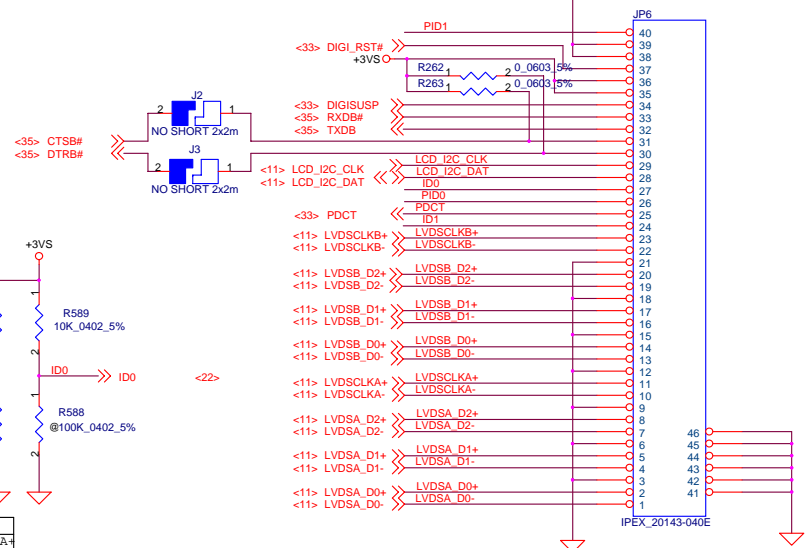
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 Title: **DDRII SO-DIMM B**  
 Size: Document Number  
 PecosII-JDX80-LA3291  
 Date: Monday, January 06, 2007  
 Sheet 16 of 53

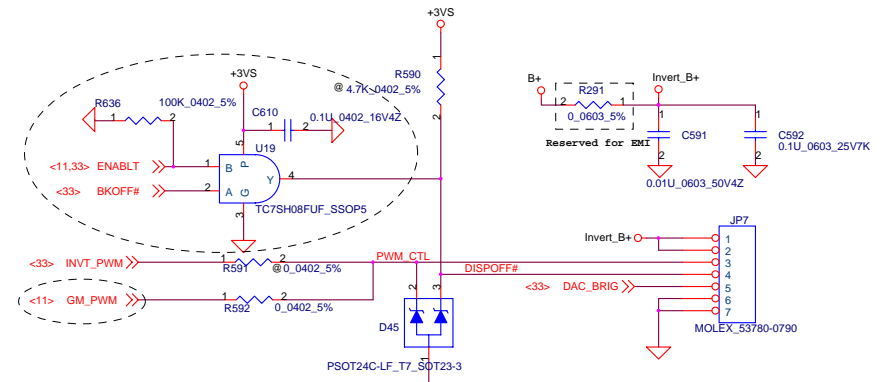
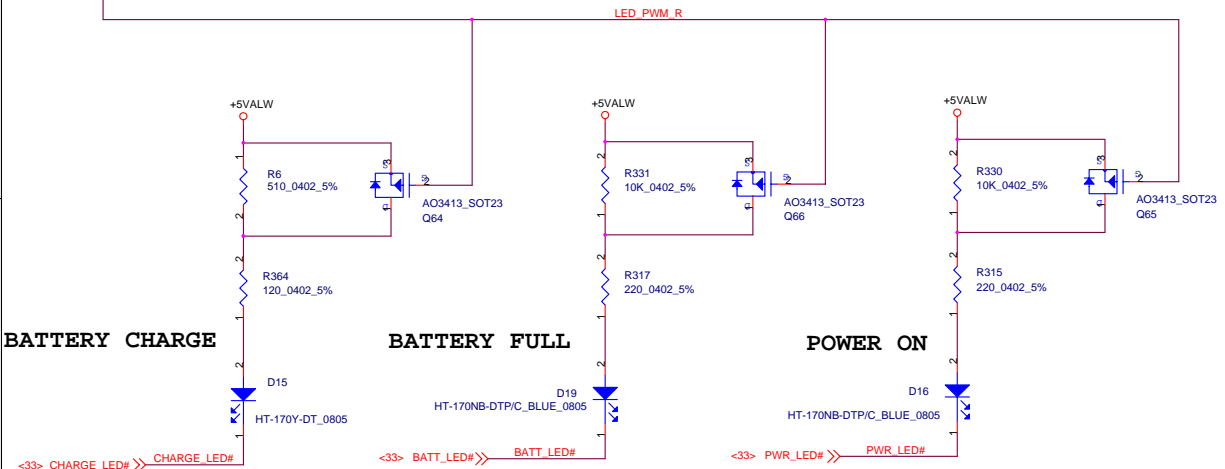
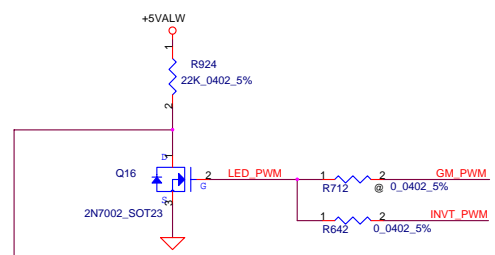




**LCD CONN.**



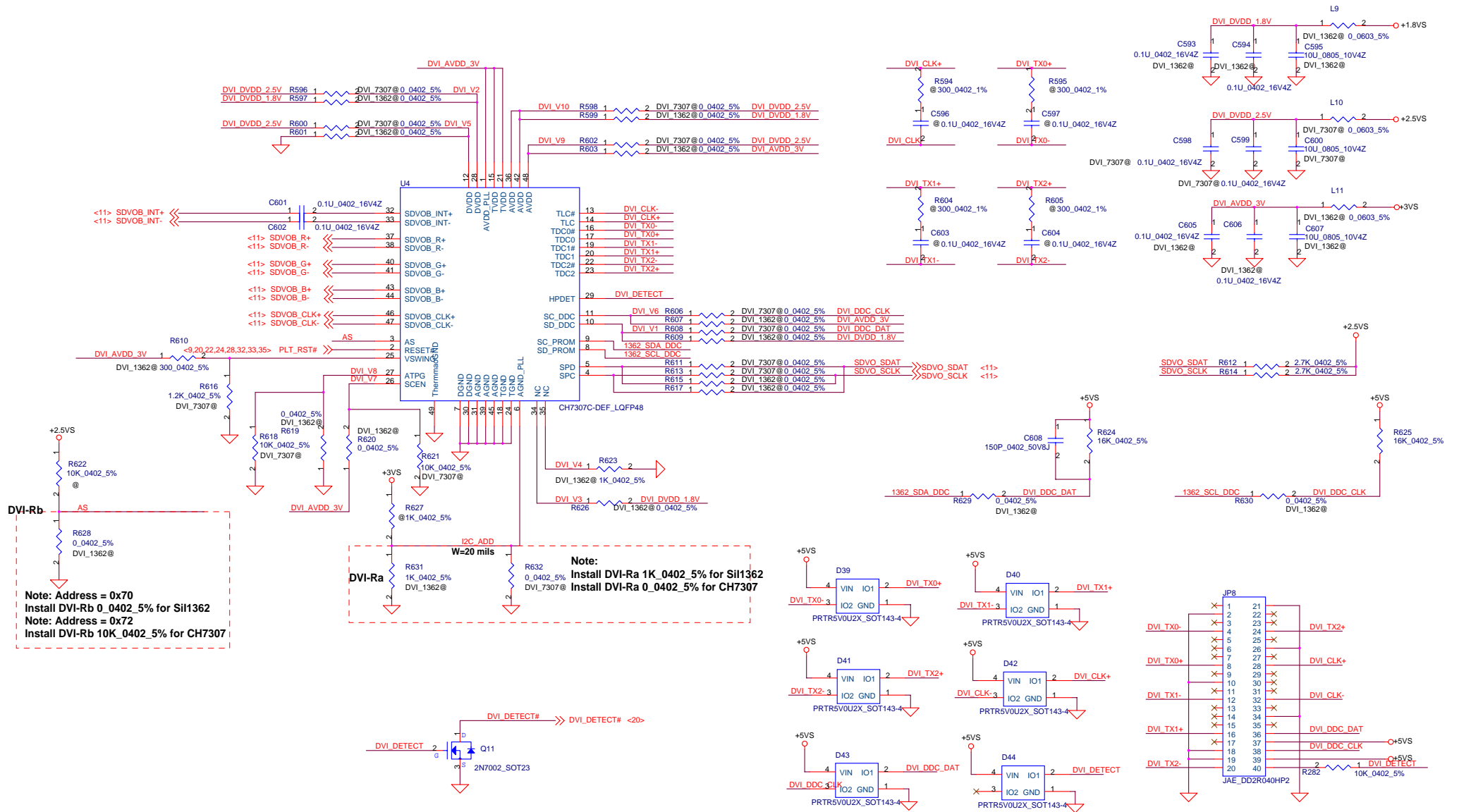
ID1	ID0	config	FID1	FID0	config
0	0	Reserve	0	0	Toshiba SXGA+
0	1	N-Trig	0	1	Toshiba XGA
1	0	TouchPanel	1	0	Hydis SXGA+
1	1	Digitizer	1	1	Hydis XGA



**Compal Electronics, Inc. (KunShan)**  
**LCD Conn&Inverter /LED dimming control**  
 Document Number: **PecosII-IDX80-LA3291**  
 Date: Monday, January 06, 2007 Sheet 17 of 53

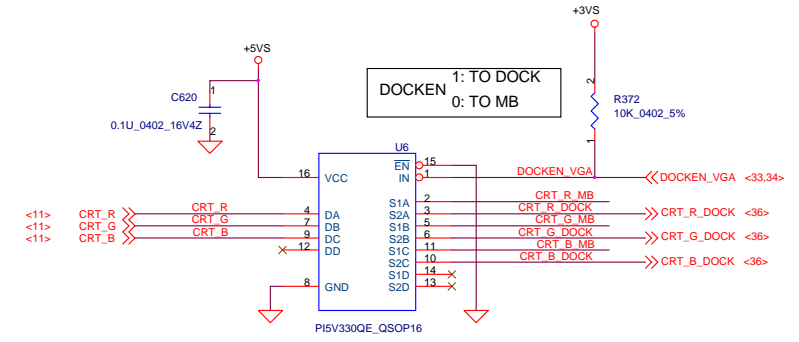
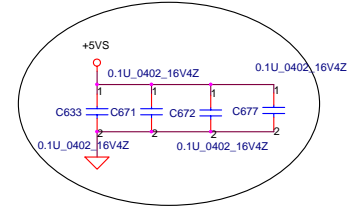
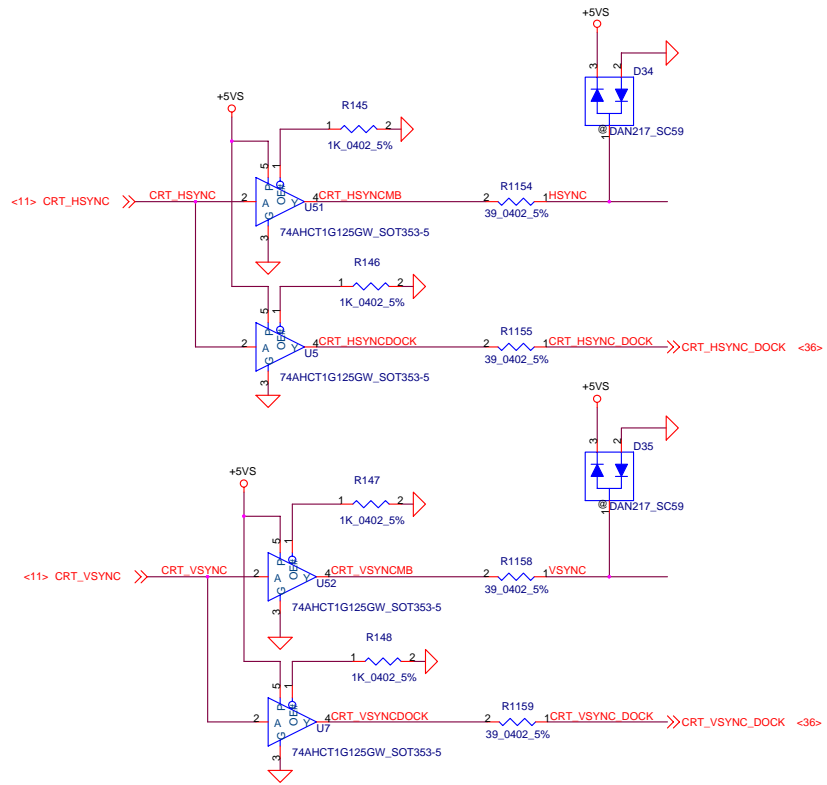
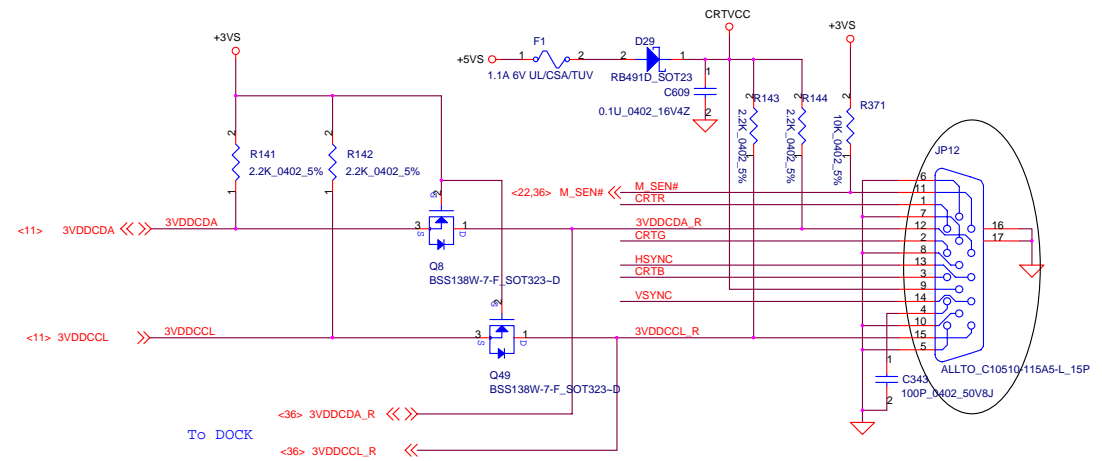
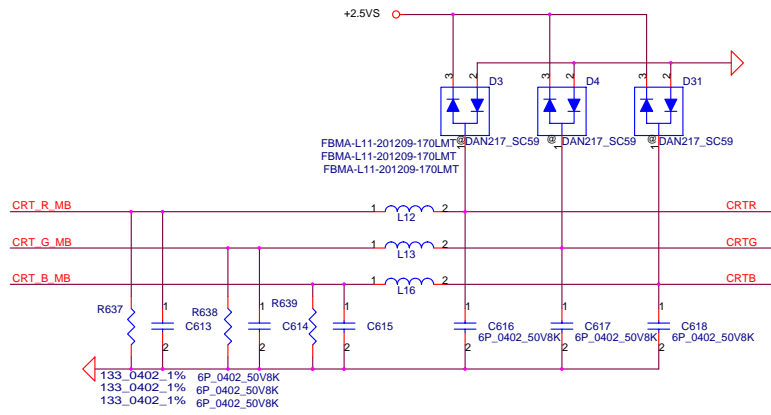
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# DVI CONTROLLER



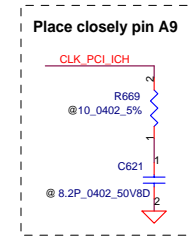
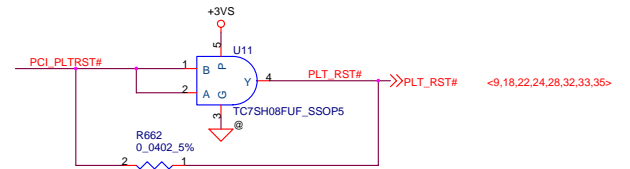
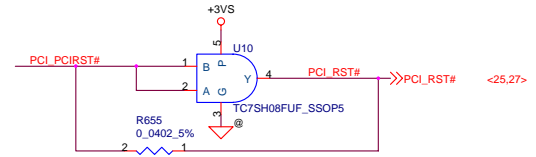
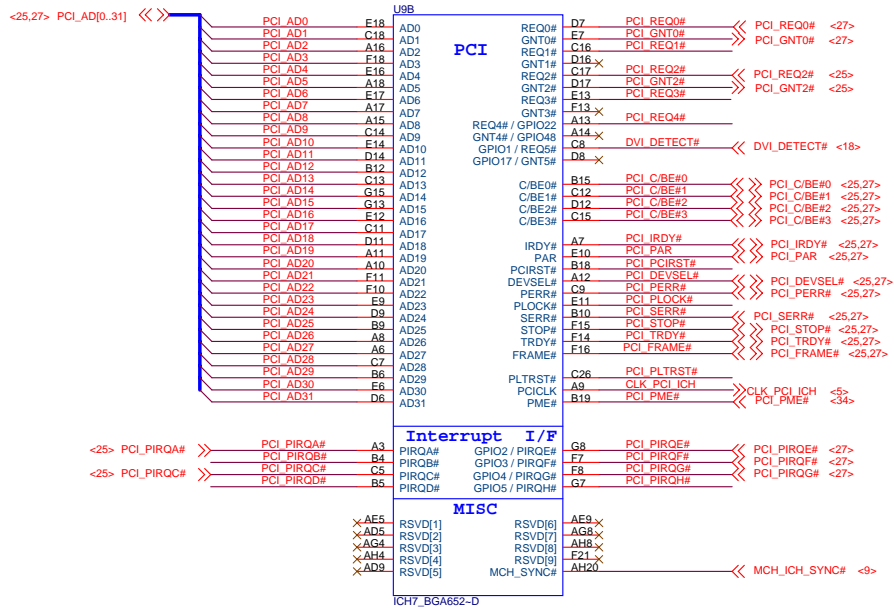
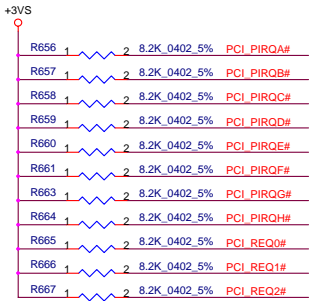
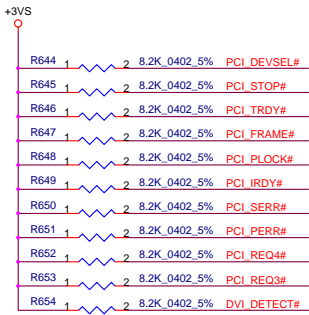
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	<b>DVI CONN</b>	
Size	Document Number	Rev
Customer	<b>PecosII-IDX80-LA3291</b>	X 0.5
Date	Monday, January 08, 2007	Sheet 18 of 53

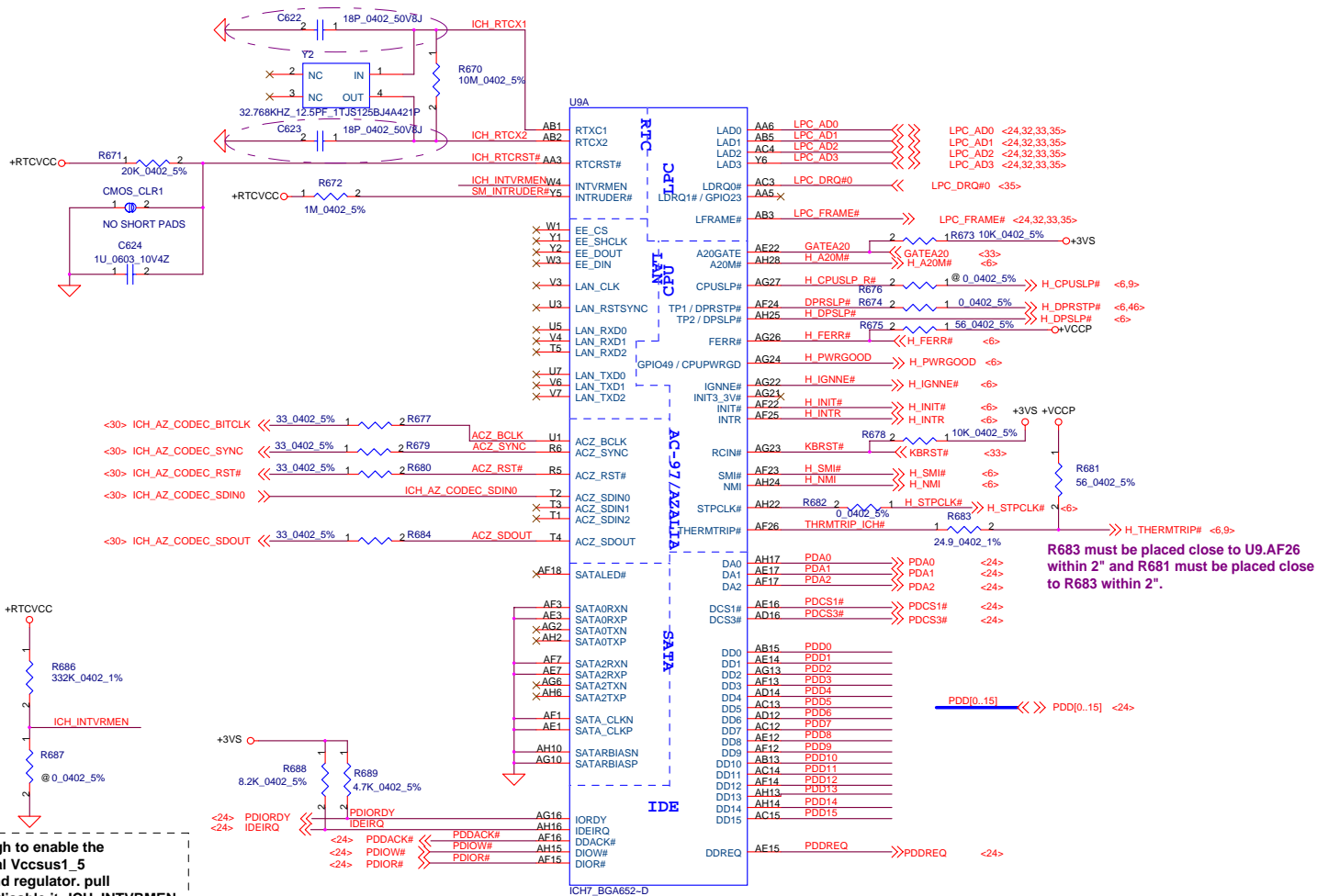


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		<b>CRT CONN</b>	
Size	Document Number	<b>PecosII-IDX80-LA3291</b>	
Date	Monday, January 06, 2007	Sheet	19 of 53

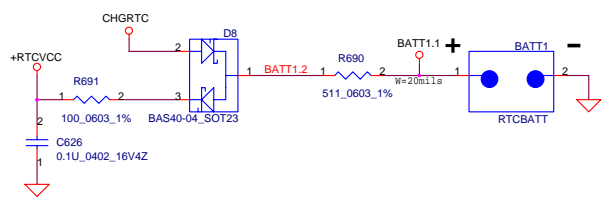


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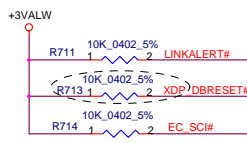
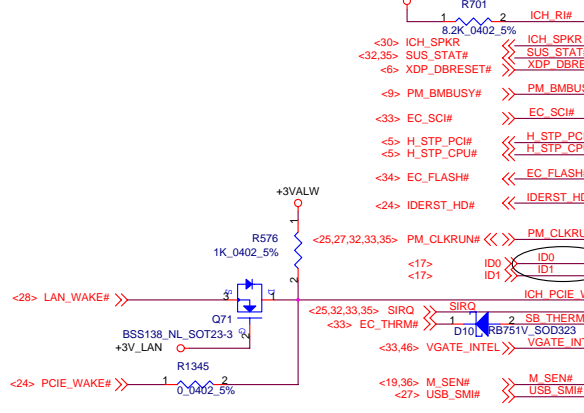
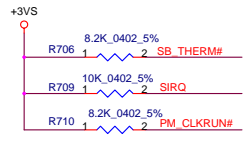
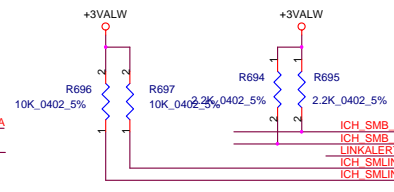
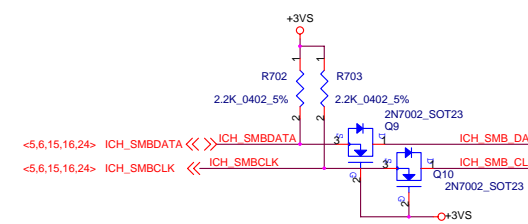
R683 must be placed close to U9.AF26 within 2" and R681 must be placed close to R683 within 2".

Pull high to enable the internal Vccsus1.5 suspend regulator. pull low to disable it--ICH\_INTVRMEN



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	<b>Compal Electronics, Inc. (KunShan)</b>	
	Title ICH7M2/4-RTC/LPC/IDE/Azalia	
	Size Cust. no.	Document Number <b>PecosII-IDX80-LA329I</b>
Date:	Monday, January 06, 2007	Sheet 21 of 53



U9C

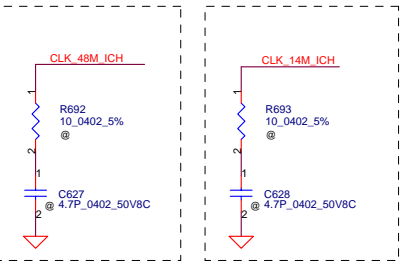
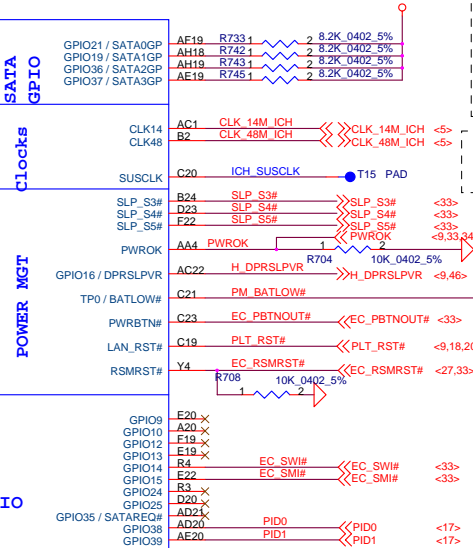
SMBCLK	B22
SMBDATA	B25
LINKALERT#	A26
ICH_SMLINK0	B25
ICH_SMLINK1	A25
RI#	A28
SPKR	A19
SUS_STAT#	A27
XDP_DBRESET#	A22
GPIO0 / BM_BUSY#	B23
GPIO11 / SMBALERT#	B23
GPIO18 / STPPCI#	AC20
GPIO20 / STPCPU#	AE21
GPIO26	A21
GPIO27	B21
GPIO28	E23
GPIO32 / CLKRUN#	AG18
GPIO33 / AZ_DOCK_EN#	AC19
GPIO34 / AZ_DOCK_RST#	U2
WAKE#	AH21
SERIRQ	AE20
THRM#	AH21
VRMPWRGD	AD22
GPIO6	AC21
GPIO7	AC18
GPIO8	E21

USD

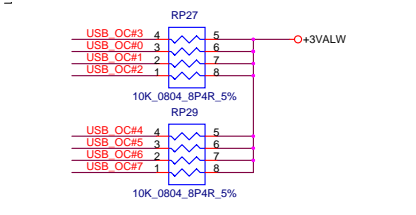
PCIE_RXN1	F26	PERn1
PCIE_RXP1	F25	PERp1
PCIE_TXN1	E28	PETn1
PCIE_TXP1	E27	PETp1
PCIE_RXN2	H26	PERn2
PCIE_RXP2	H25	PERp2
PCIE_TXN2	G28	PETn2
PCIE_TXP2	G27	PETp2
PCIE_RXN3	K26	PERn3
PCIE_RXP3	K25	PERp3
PCIE_TXN3	J28	PETn3
PCIE_TXP3	J27	PETp3
M26		PERn4
M25		PERp4
L28		PETn4
L27		PETp4
N26		PERn5
N25		PERp5
N28		PETn5
N27		PETp5
T25		PERn6
T24		PERp6
R28		PETn6
R27		PETp6
R2		SPI_CLK
P6		SPI_CS#
P1		SPI_ARB
P5		SPI_MOSI
P2		SPI_MISO
OC#0	D3	OC#0
OC#1	C4	OC#1
OC#2	D5	OC#2
OC#3	D4	OC#3
OC#4	C3	OC#4
OC#5	A2	OC#5
OC#6	A2	OC#6
OC#7	B3	OC#7
OC#8 / GPIO29		OC#8
OC#9 / GPIO30		OC#9
OC#10 / GPIO31		OC#10

USD

DMIORXN	V26	DMI_RXN0	<-9>
DMIOFXP	V25	DMI_RXP0	<-9>
DMIOTXN	U28	DMI_TXN0	<-9>
DMIOFXP	U27	DMI_TXP0	<-9>
DMI1RXN	Y26	DMI_RXN1	<-9>
DMI1FXP	Y25	DMI_RXP1	<-9>
DMI1TXN	W28	DMI_TXN1	<-9>
DMI1FXP	W27	DMI_TXP1	<-9>
DMI2RXN	AB26	DMI_RXN2	<-9>
DMI2FXP	AB25	DMI_RXP2	<-9>
DMI2TXN	AA28	DMI_TXN2	<-9>
DMI2FXP	AA27	DMI_TXP2	<-9>
DMI3RXN	AD25	DMI_RXN3	<-9>
DMI3FXP	AD24	DMI_RXP3	<-9>
DMI3TXN	AC28	DMI_TXN3	<-9>
DMI3FXP	AC27	DMI_TXP3	<-9>
DMI_CLKN	AE28	CLK_PCIE_ICH#	<-5>
DMI_CLKP	AE27	CLK_PCIE_ICH	<-5>
DMI_ZCOMP	C25	DMI_IRCOMP	<-9>
DMI_IRCOMP	D25	DMI_IRCOMP	<-9>
USBP0N	F1	USBP0-	<-32>
USBP0P	F2	USBP0+	<-32>
USBP1N	G4	USBP1-	<-32>
USBP1P	G3	USBP1+	<-32>
USBP2N	H1	USBP2-	<-24>
USBP2P	H2	USBP2+	<-24>
USBP3N	J4	USBP3-	<-36>
USBP3P	J3	USBP3+	<-36>
USBP4N	K1	USBP4-	<-36>
USBP4P	K2	USBP4+	<-36>
USBP5N	L4	USBP5-	<-36>
USBP5P	L5	USBP5+	<-36>
USBP6N	M1	USBP6-	<-36>
USBP6P	M2	USBP6+	<-36>
USBP7N	N4	USBP7-	<-36>
USBP7P	N3	USBP7+	<-36>
USBRBIAS	D2	USBRBIAS	<-9>
USBRBIAS	D1	USBRBIAS	<-9>

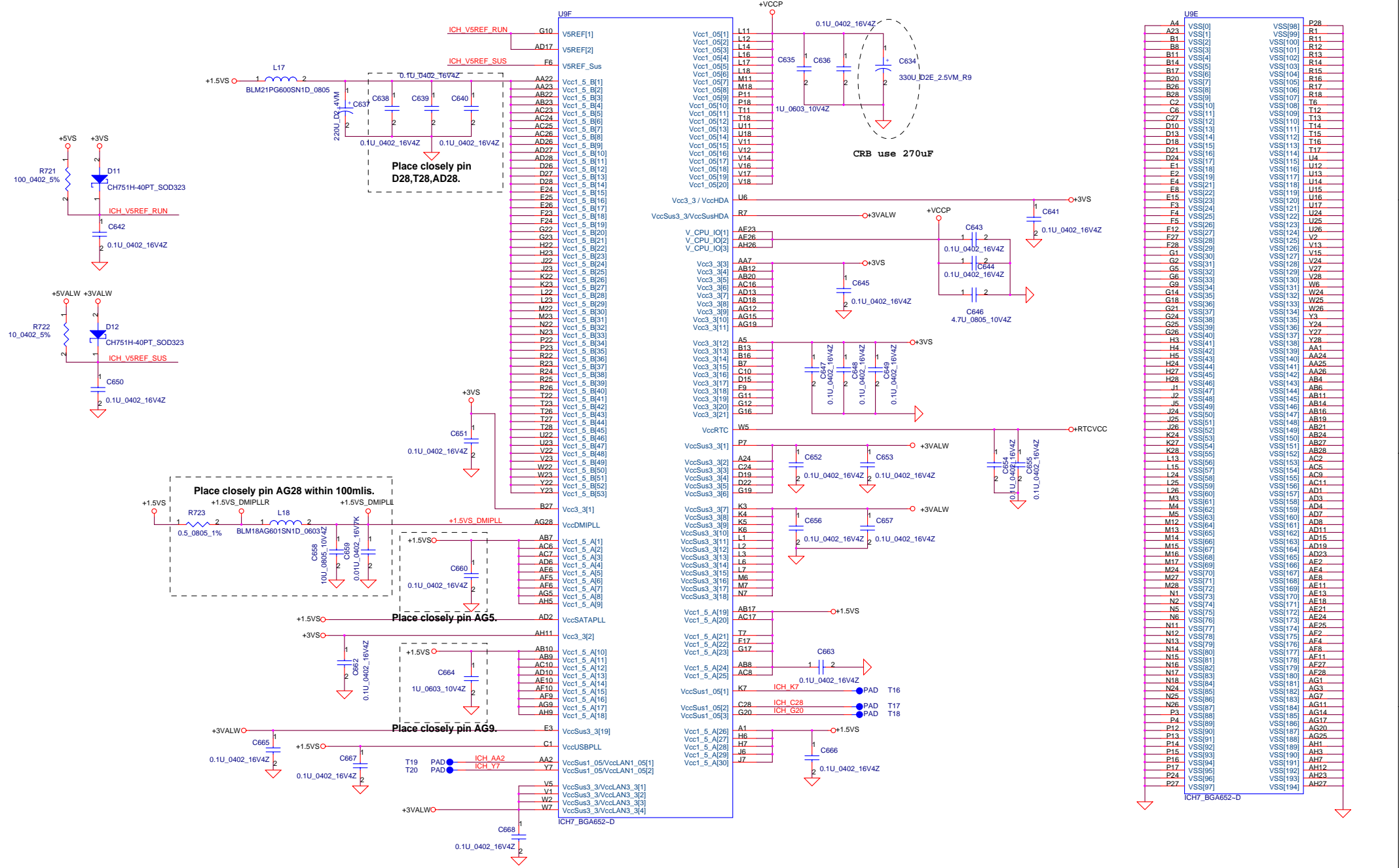


If the susclk duty cycle is beyond the 30-70% range, it indicate a poor oscillation signal



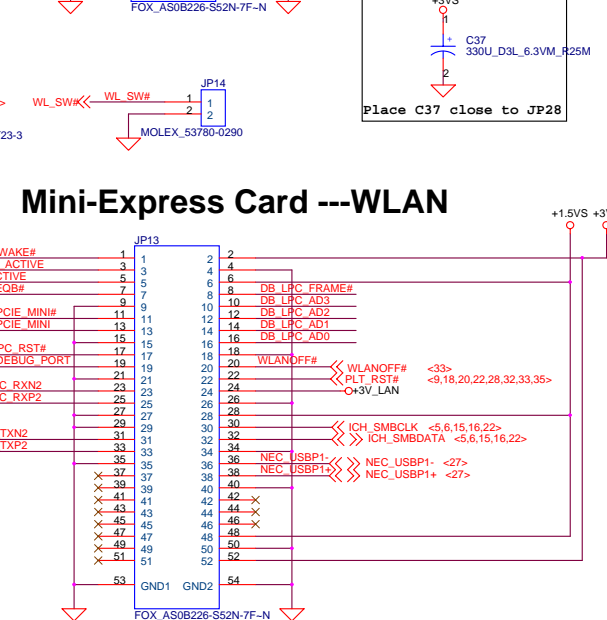
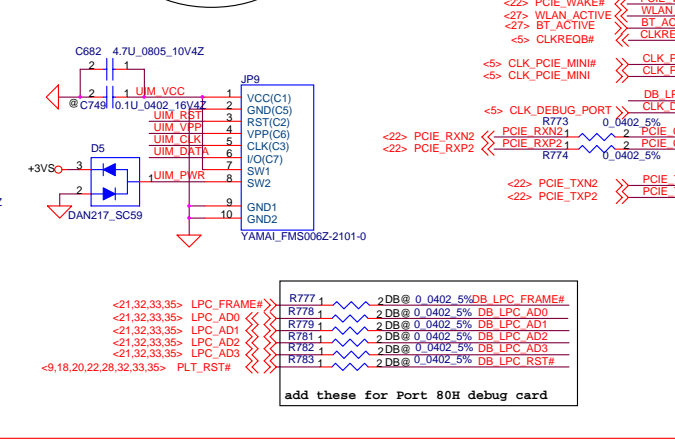
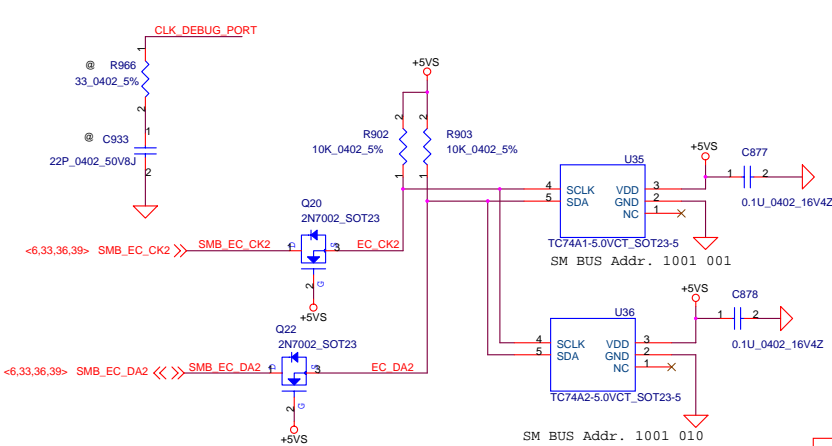
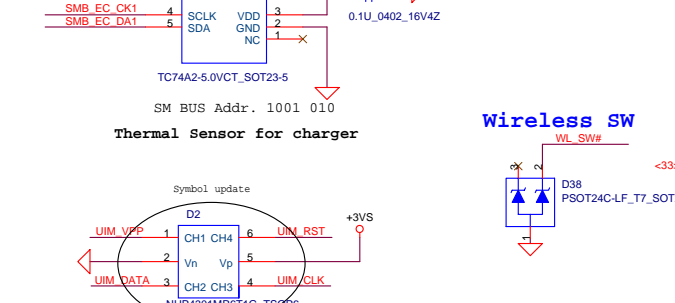
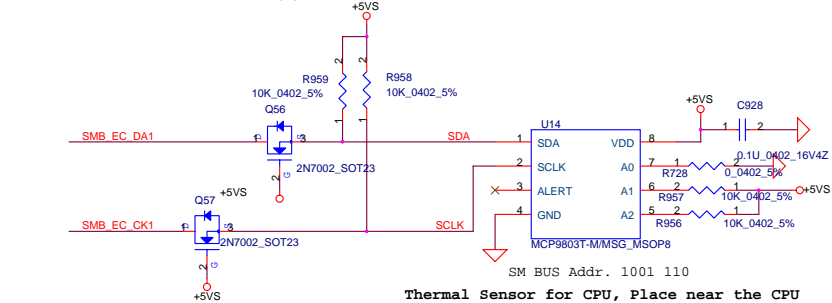
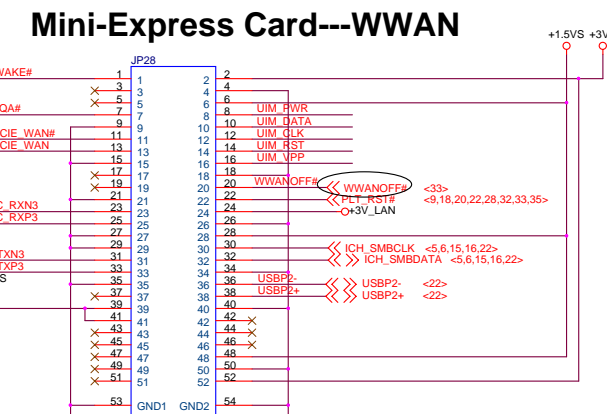
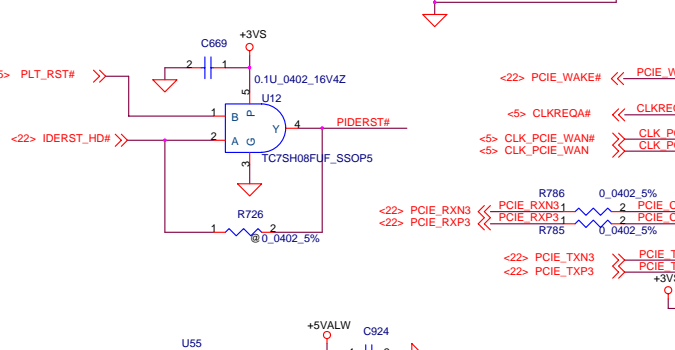
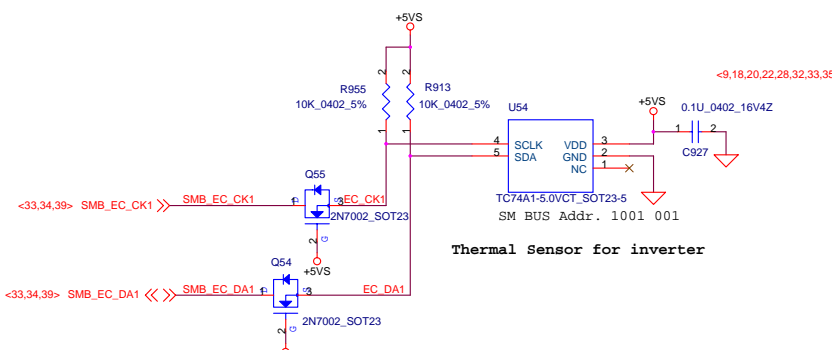
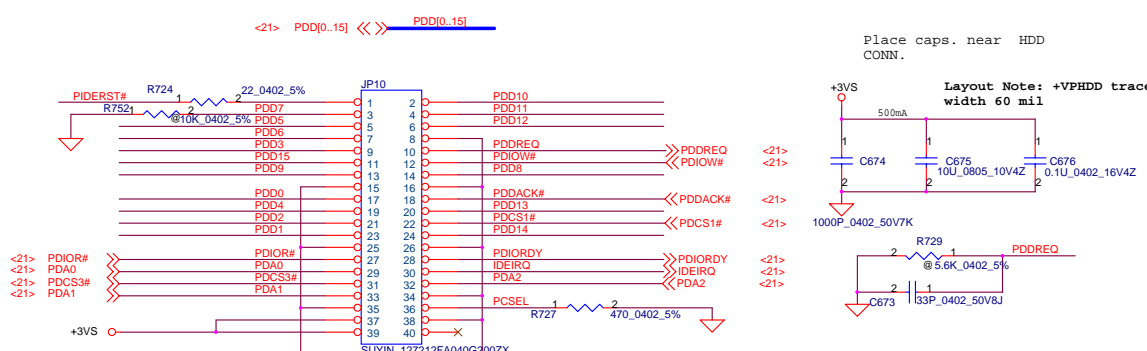
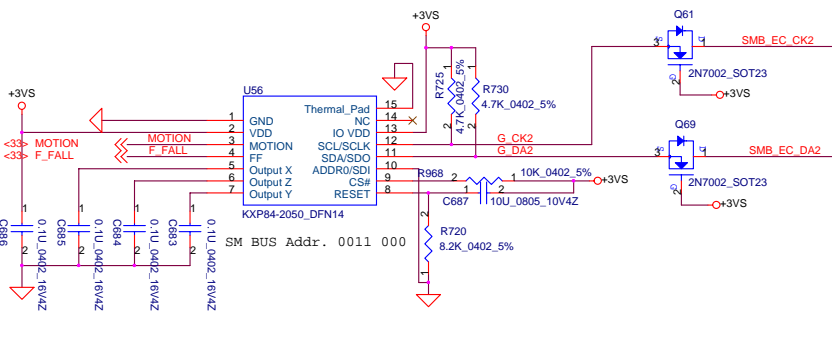
Within 500 mils

This is only supported USBRBIAS value for the Intel 82801GM and is required to properly configure the USB interface drive strength.



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		<b>Compal Electronics, Inc. (KunShan)</b> Title	
		ICH7M4/GNR/GND	
Size Cust. no.	Document Number <b>PecosII-IDX80-LA3291</b>	Date: Monday, January 06, 2007	Rev X.0.3
		Sheet 23	of 53

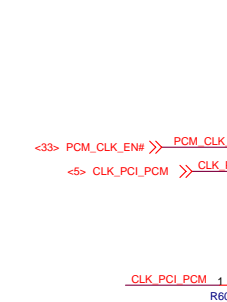
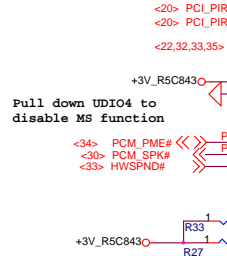
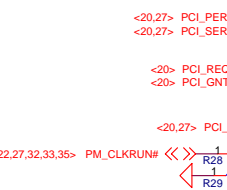
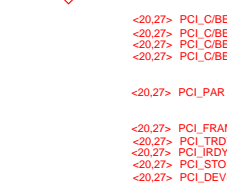
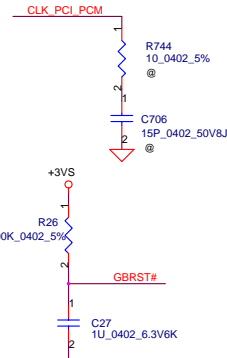


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**Compal Electronics, Inc. (KunShan)**  
**MINI Card Slot/PIDE&Thermal sensor**  
 PecosII-IDX80-LA3291  
 Date: Monday, January 06, 2007 Sheet 24 of 53



Layout notice:  
apply shield GND  
for CLK\_PCI\_PCM to  
reduce external noise.



U15A	Pin	Signal	Internal Pin
PCI AD31	M2	AD31	CAD31/CDATA10
PCI AD30	M3	AD30	CAD30/CDATA9
PCI AD29	N5	AD29	CAD29/CDATA8
PCI AD28	N4	AD28	CAD28/CDATA7
PCI AD27	N2	AD27	CAD27/CDATA6
PCI AD26	N1	AD26	CAD26/CDATA5
PCI AD25	P5	AD25	CAD25/CDATA4
PCI AD24	P4	AD24	CAD24/CDATA3
PCI AD23	R4	AD23	CAD23/CDATA2
PCI AD22	R2	AD22	CAD22/CDATA1
PCI AD21	R1	AD21	CAD21/CDATA0
PCI AD20	T2	AD20	CAD20/CDATA0
PCI AD19	T1	AD19	CAD19/CDADR25
PCI AD18	U2	AD18	CAD18/CDADR24
PCI AD17	U1	AD17	CAD17/CDADR23
PCI AD16	V4	AD16	CAD16/CDADR22
PCI AD15	T7	AD15	CAD15/CDADR21
PCI AD14	V7	AD14	CAD14/CDADR20
PCI AD13	W7	AD13	CAD13/CDADR19
PCI AD12	R8	AD12	CAD12/CDADR18
PCI AD11	T8	AD11	CAD11/CDADR17
PCI AD10	W8	AD10	CAD10/CDADR16
PCI AD9	V8	AD9	CAD9/CDADR15
PCI AD8	R9	AD8	CAD8/CDADR14
PCI AD7	V9	AD7	CAD7/CDADR13
PCI AD6	W9	AD6	CAD6/CDADR12
PCI AD5	T11	AD5	CAD5/CDADR11
PCI AD4	V11	AD4	CAD4/CDADR10
PCI AD3	W11	AD3	CAD3/CDADR9
PCI AD2	T12	AD2	CAD2/CDADR8
PCI AD1	V12	AD1	CAD1/CDADR7
PCI AD0	W12	AD0	CAD0/CDADR6

Pin	Signal	Internal Pin
B13	S1 D10	S1_D10
C18	S1 D9	S1_D9
D19	S1 D1	S1_D1
D18	S1 D8	S1_D8
E19	S1 D0	S1_D0
E16	S1 A0	S1_A0
F18	S1 A1	S1_A1
F15	S1 A2	S1_A2
G18	S1 A3	S1_A3
G15	S1 A4	S1_A4
H18	S1 A5	S1_A5
H15	S1 A6	S1_A6
J16	S1 A7	S1_A7
J15	S1 A24	S1_A24
K16	S1 A17	S1_A17
K15	S1 A8	S1_A8
L19	S1 IOWR#	S1_IOWR#
L18	S1 A9	S1_A9
M19	S1 IORD#	S1_IORD#
M18	S1 A11	S1_A11
N19	S1 OE#	S1_OE#
N18	S1 CE2#	S1_CE2#
O18	S1 A10	S1_A10
O15	S1 D15	S1_D15
P17	S1 D7	S1_D7
P17	S1 D13	S1_D13
Q16	S1 D6	S1_D6
Q16	S1 D12	S1_D12
R15	S1 D5	S1_D5
R15	S1 D11	S1_D11
T15	S1 D4	S1_D4
T15	S1 D3	S1_D3

USB signals, impedance 90 ohm  
 >>>S1\_IOWR# <<<  
 >>>S1\_IORD# <<<  
 >>>S1\_OE# <<<  
 >>>S1\_CE2# <<<

>>>S1\_REG# <<<  
 >>>S1\_CE1# <<<

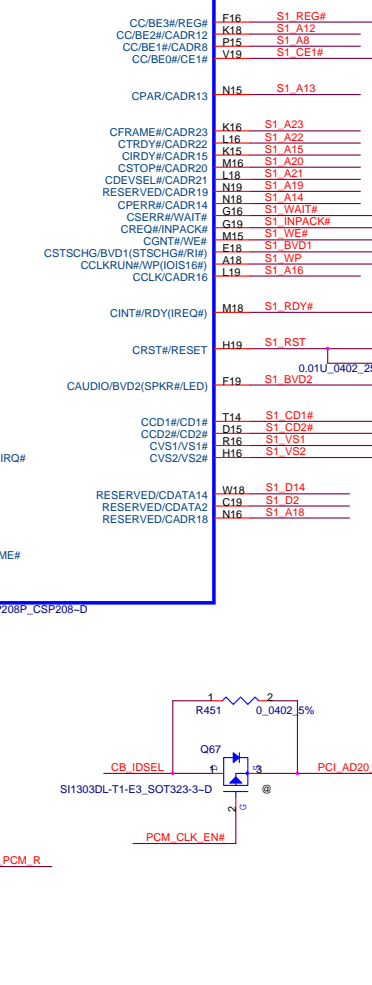
>>>S1\_WAIT# <<<  
 >>>S1\_INPACK# <<<  
 >>>S1\_WE# <<<  
 >>>S1\_BVD1 <<<  
 >>>S1\_WP <<<  
 >>>S1\_RDY# <<<

>>>S1\_RST <<<  
 >>>S1\_BVD2 <<<

>>>S1\_CD1# <<<  
 >>>S1\_CD2# <<<

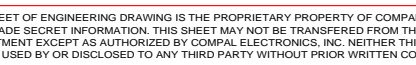
>>>S1\_VS1 <<<  
 >>>S1\_VS2 <<<

>>>S1\_D14 <<<  
 >>>S1\_D2 <<<  
 >>>S1\_A18 <<<

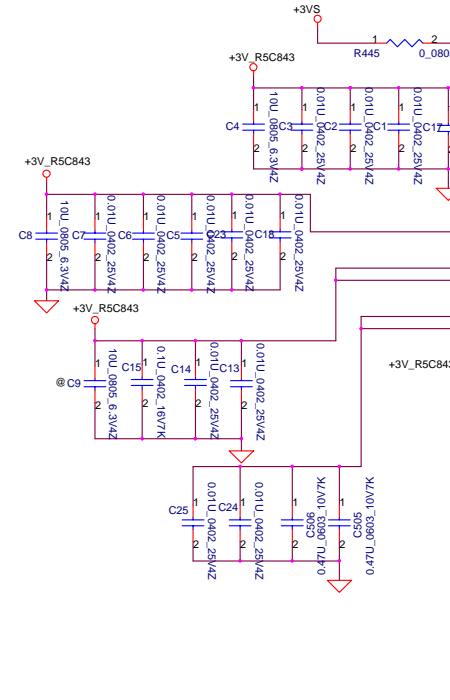
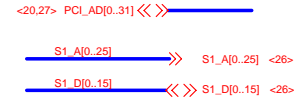


Layout notice: apply Shield GND  
for L19 signal s1\_A16

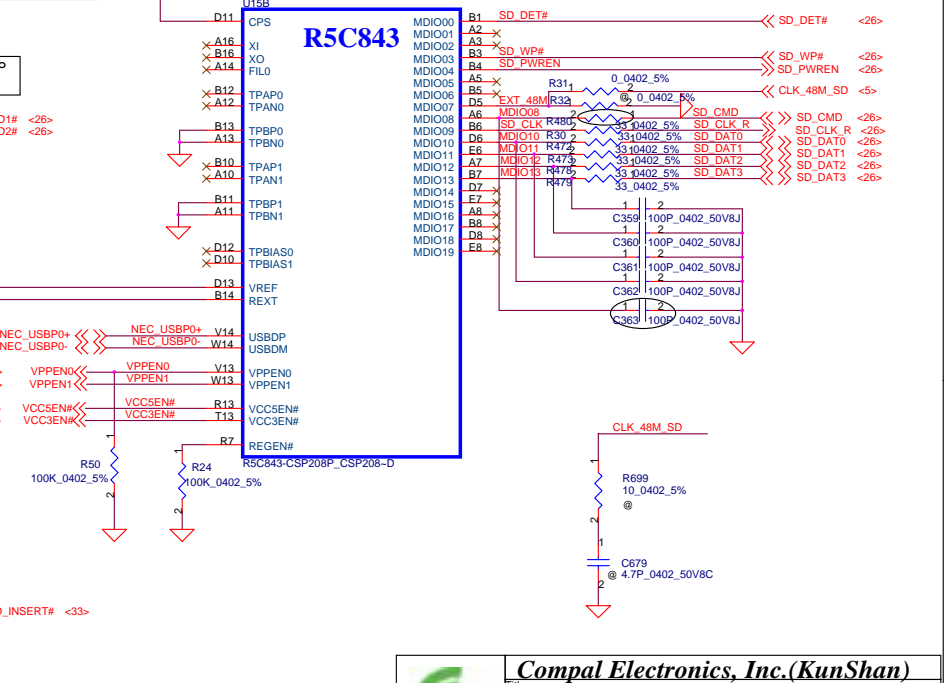
C71, C188, C208 close to  
JP33 cardbus connector



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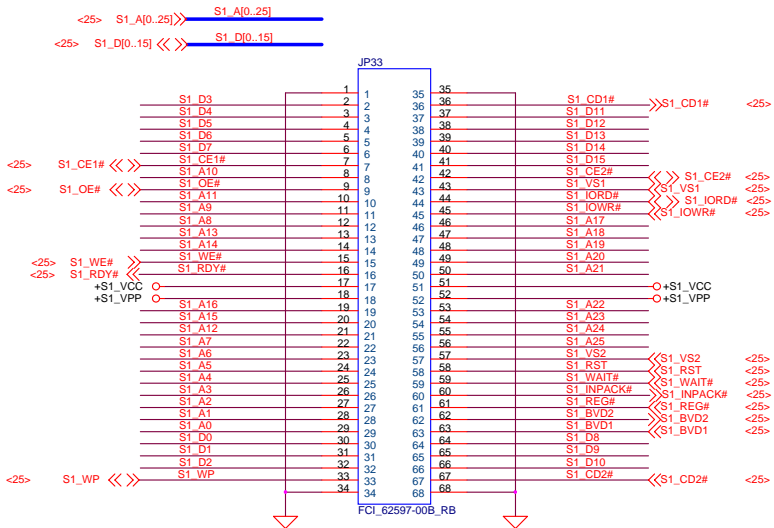


### R5C843

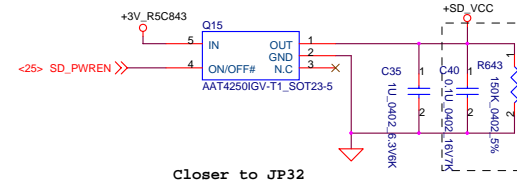
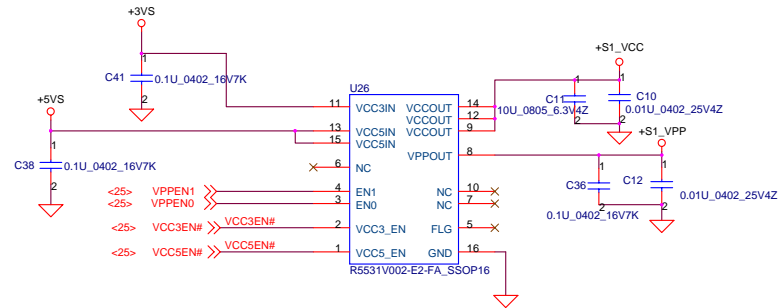


Compal Electronics, Inc. (KunShan)	
Title: CARBUS_R5C843	
Size: Document Number	Rev: X 0.5
Date: Monday, January 08, 2007	Sheet: 25 of 53

# CARDBUS SOCKET

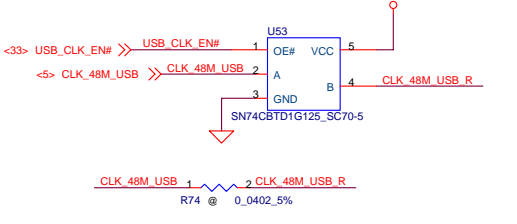
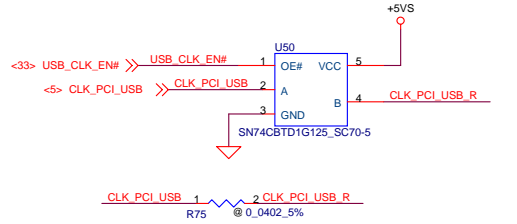
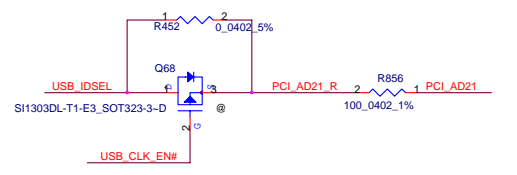
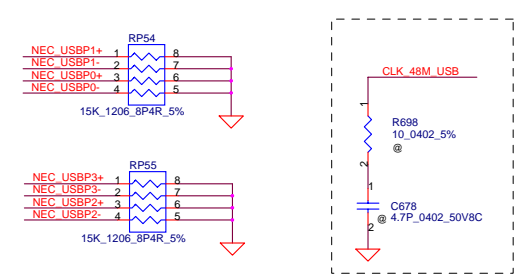


# SD SOCKET

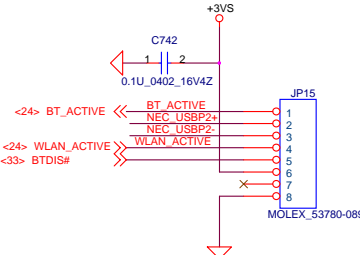


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	<b>Compal Electronics, Inc. (KunShan)</b>	
	Title <b>PCMCIA Slot/SD</b>	Document Number <b>PecosII-IDX80-LA3291</b>
Size Cust.com	Date: Monday, January 08, 2007	Rev X 0.5 Sheet 26 of 53

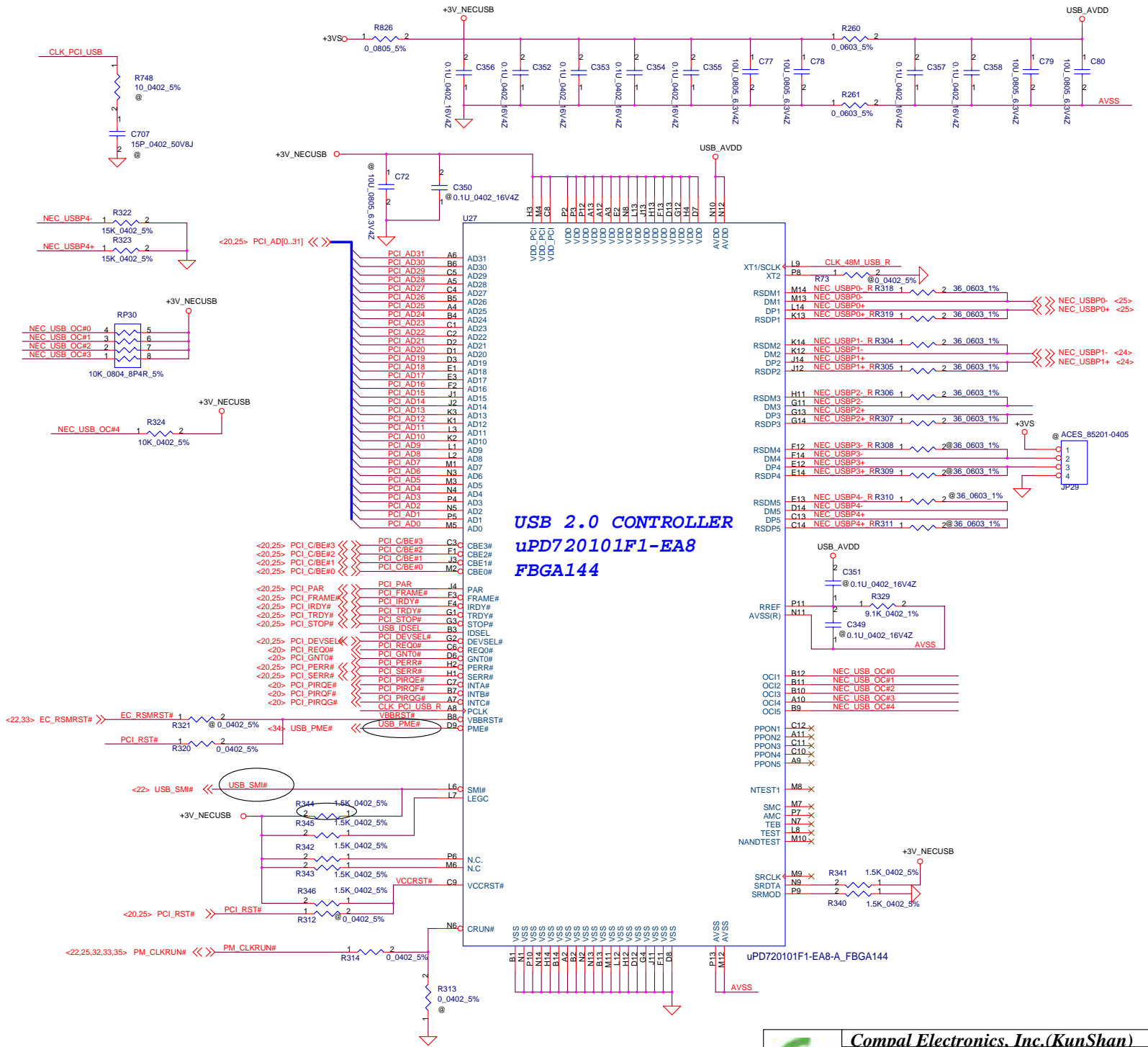


### BT MODULE CONN



**Bluetooth Cable**

Mini Card Pin5	BT_ACTIVE JP27.1
Mini Card Pin3	WLAN_ACTIVE JP27.4

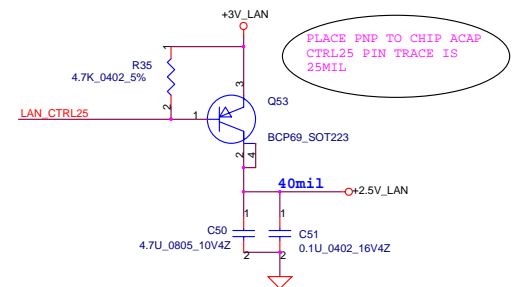
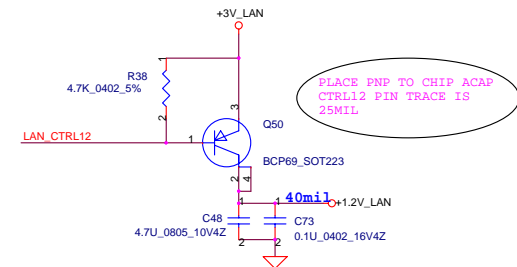
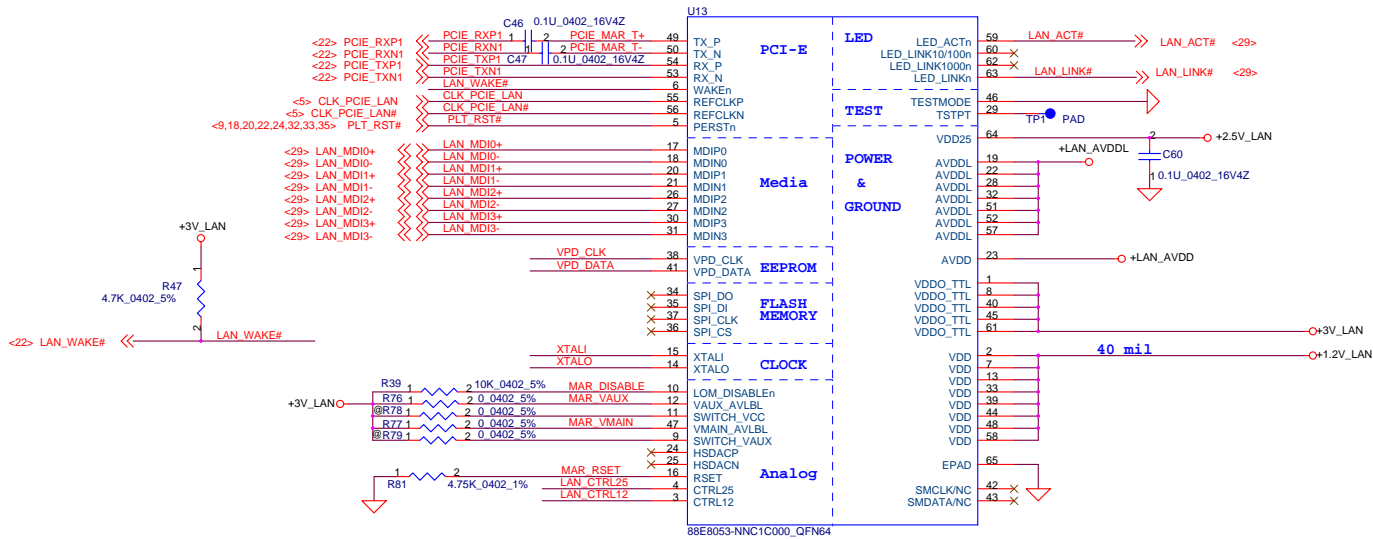


### USB 2.0 CONTROLLER uPD720101F1-EA8 FBGA144

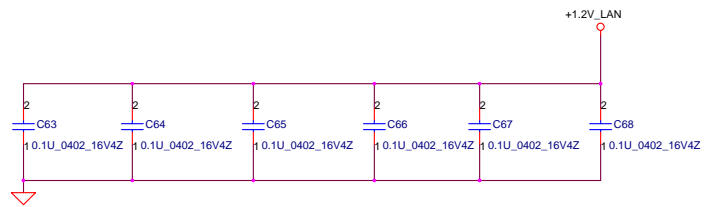
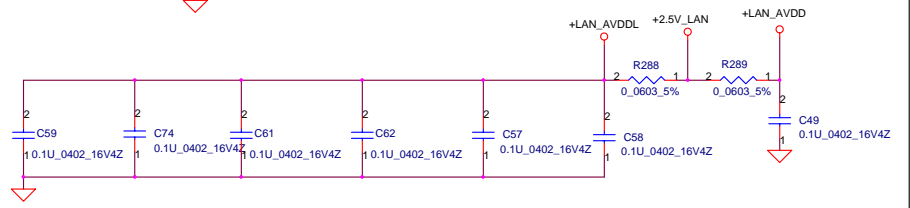
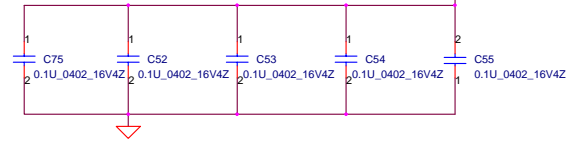
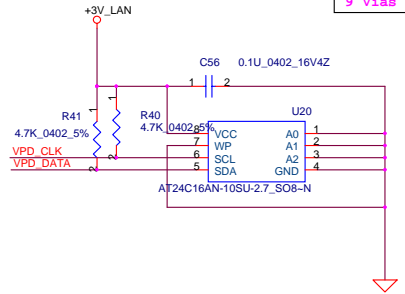
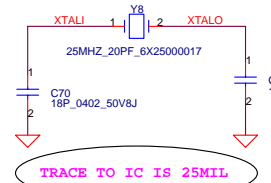
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**Compal Electronics, Inc. (KunShan)**  
**BT&USB CONTROLLER**

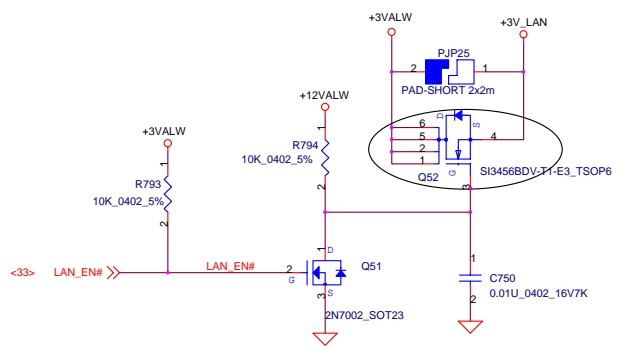
File	Document Number	Rev
Size	PecosII-IDX80-LA3291	X.0.5
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9 Vias to Ground at least.



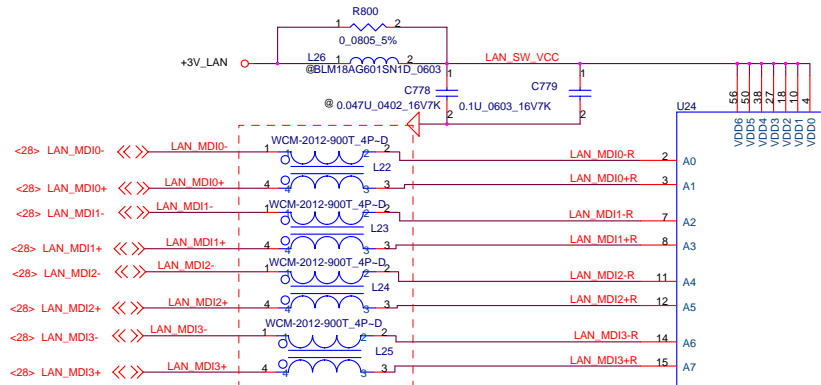
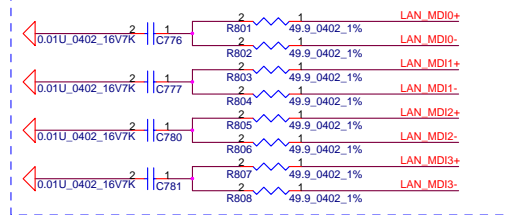
Note: Place Bypass Cap. with every power pin ACAP.



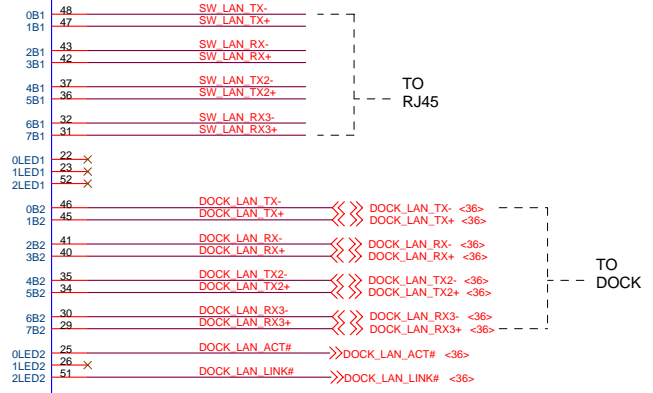
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	<b>Compal Electronics, Inc. (KunShan)</b>	
	88E8053	
Size	Document Number	Rev
Custom	<b>PecosII-IDX80-LA3291</b>	X 0.5
Date:	Monday, January 06, 2007	Sheet 28 of 53

**Close to Chip side**

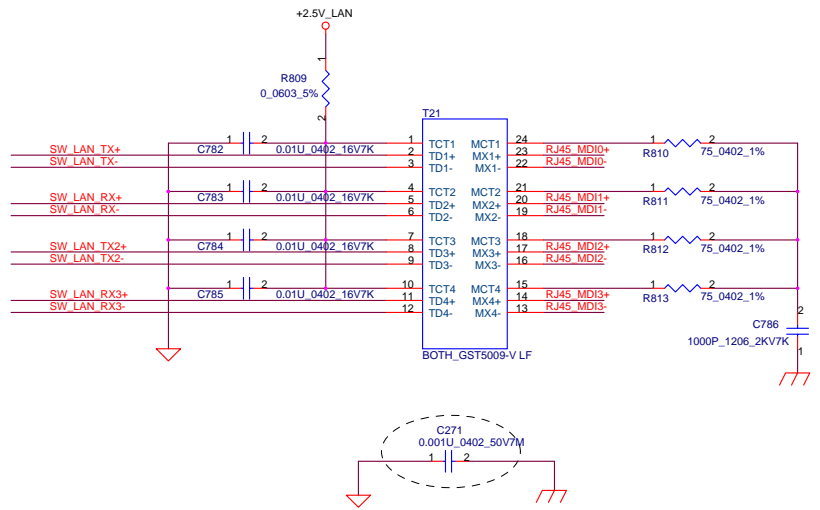
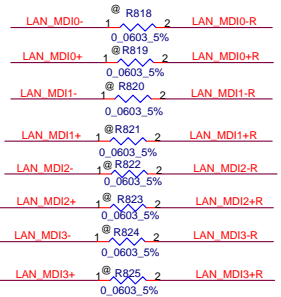


**LAN ANALOG SWITCH**

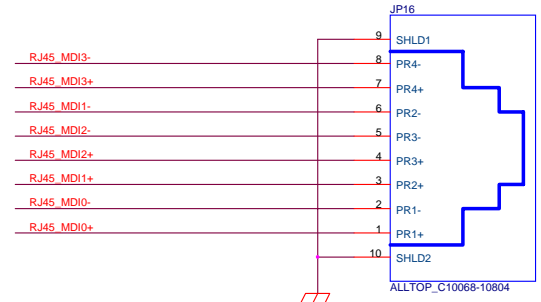


**DOCKEN 1: TO DOCK  
0: TO RJ45**

**Layout Notice : Place ckeoke as close P13L500 as possible**

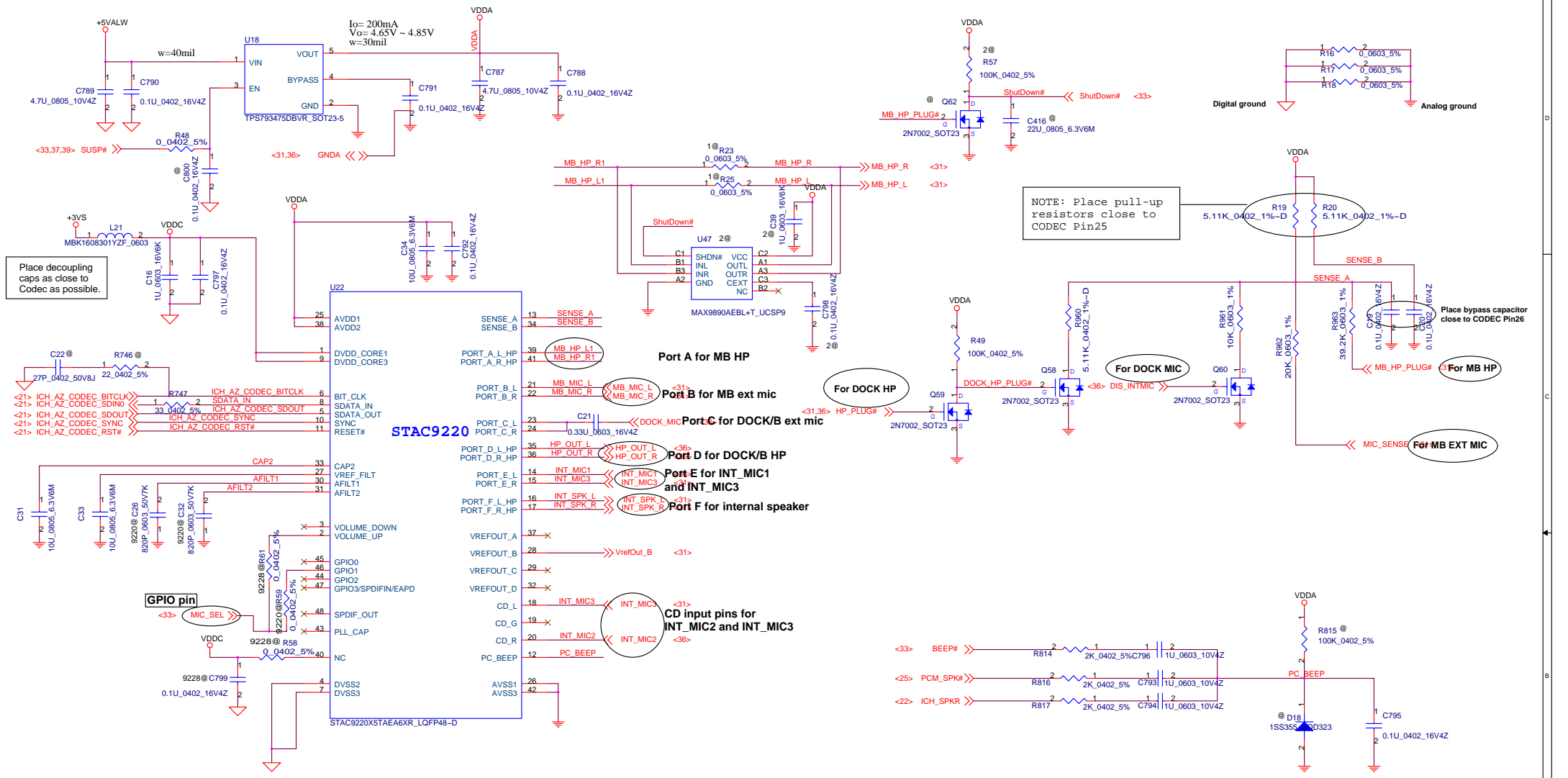


**FROM NIC**



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**Compal Electronics, Inc. (KunShan)**  
**Magnetics & RJ45**  
 Size: Document Number  
 Date: Monday, January 06, 2007 Sheet 29 of 53  
 Rev: X 0.5  
**PecosII-IDX80-LA3291**



Place decoupling caps as close to Codec as possible.

NOTE: Place pull-up resistors close to CODEC pin25

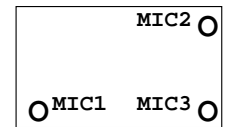
Place bypass capacitor close to CODEC Pin26

Item	STAC9220	STAC9228
C26, C32	POP	DE_POP
R58, C799	DE_POP	POP
R59	POP	DE_POP
R61	DE_POP	POP

	DIS_INTMIC	INT_MIC1 INT_MIC2 INT_MIC3	DOCK_MIC (PIN 23/24)
H	DISABLE	ENABLE	ENABLE
L	ENABLE	ENABLE	DISABLE

	MB_HP_PLUG# (EAPD function)	INT_SPK_L INT_SPK_R	PIN16 PIN17
H	ENABLE	ENABLE	
L	DISABLE	DISABLE	

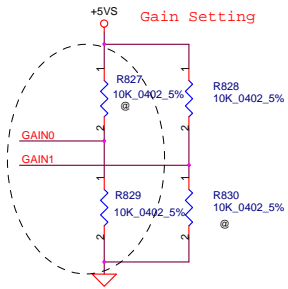
	MIC_SEL (PIN 46)	INT_MIC1 (PIN 14)	INT_MIC2 (PIN 20)	INT_MIC3 (PIN 15, 18)
L (Landscape)	ENABLE	ENABLE	DISABLE	ENABLE
H (Portrait)	DISABLE	DISABLE	ENABLE	ENABLE



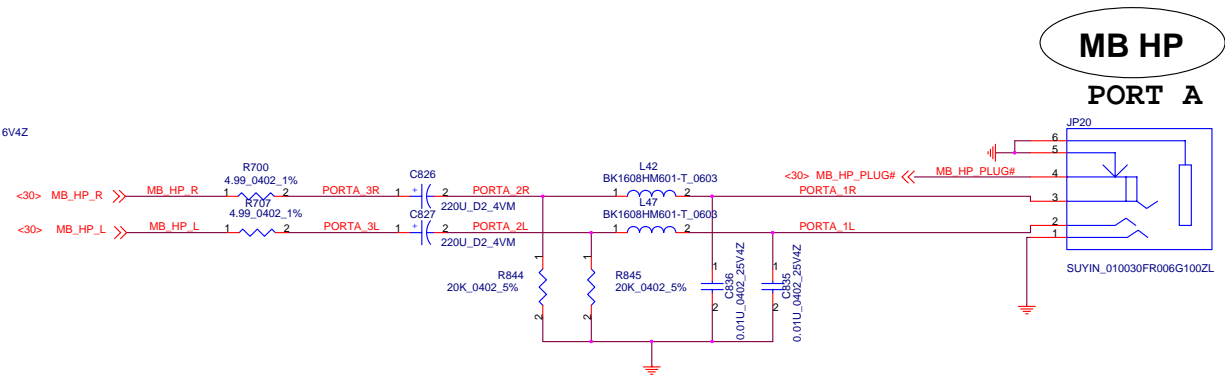
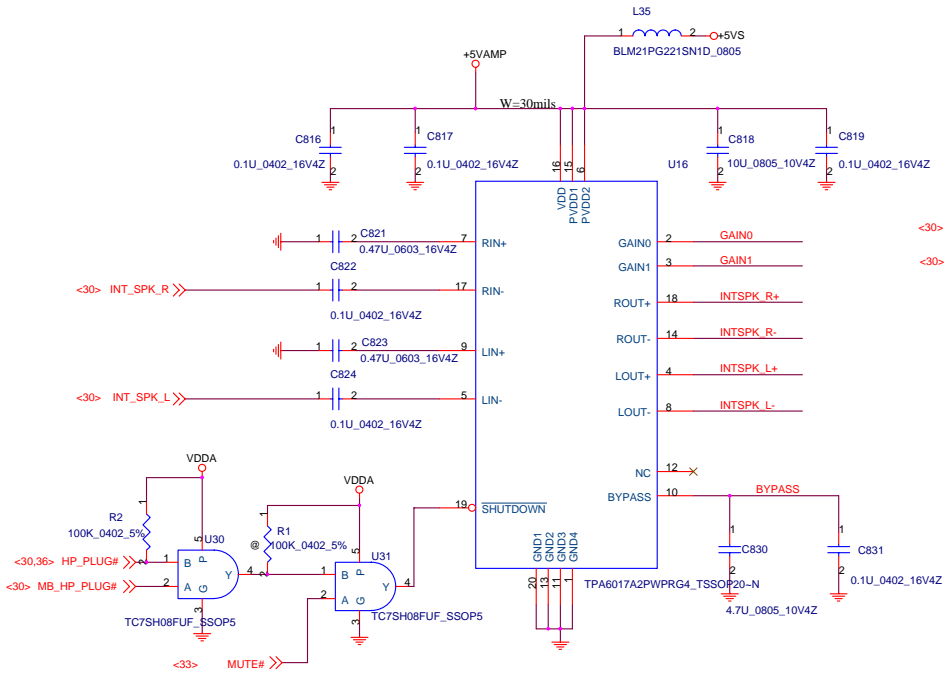
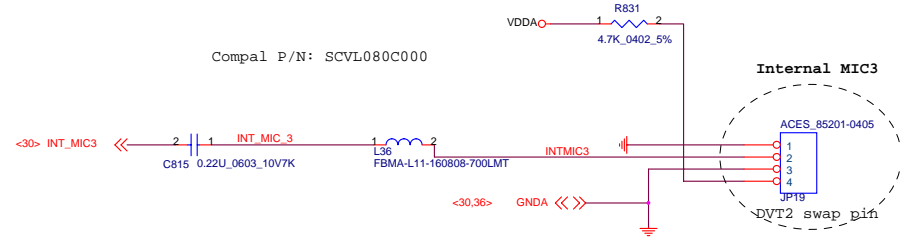
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**Compal Electronics, Inc. (KunShan)**  
 Title: Azalia Codec STAC9220  
 Size: Document Number  
 Date: Monday, January 08, 2007  
 Sheet: 30 of 53

Rev: X.05  
**Pecos II-IDX80-LA 3291**

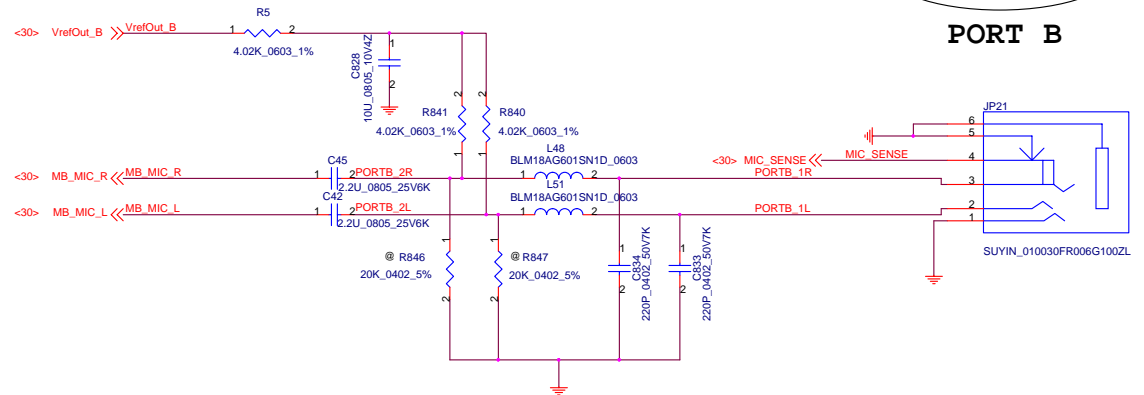


GAIN0	GAIN1	AV(inv)	INPUT IMPEDANCE
0	0	6dB	90K ohm
0	1	10dB	70K ohm
1	0	15.6dB	45K ohm
1	1	21.6dB	25K ohm

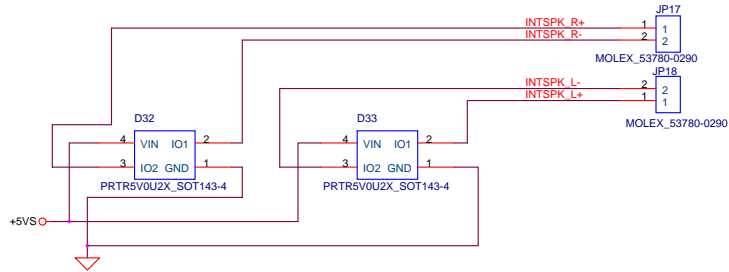


**MB HP  
PORT A**

**MB ext MIC  
PORT B**



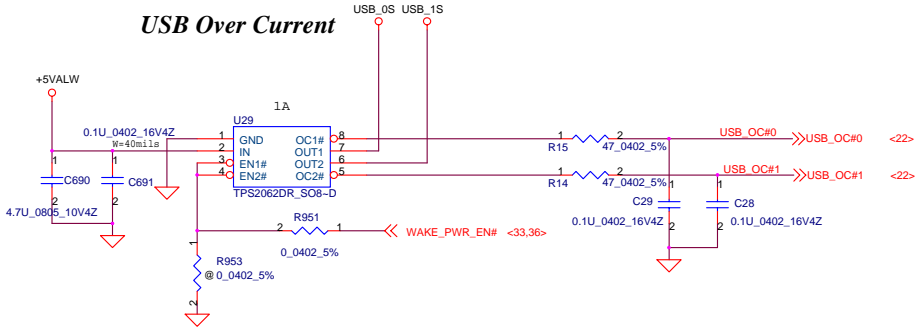
**Speaker**



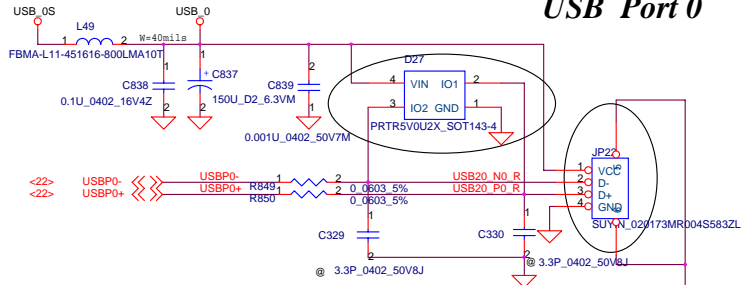
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	<b>AMP &amp; Audio JACK</b>	
	Size: Custom	Document Number: <b>PecosII-IDX80-LA329I</b>
	Date: Monday, January 08, 2007	Sheet: 31 of 53

### USB Over Current

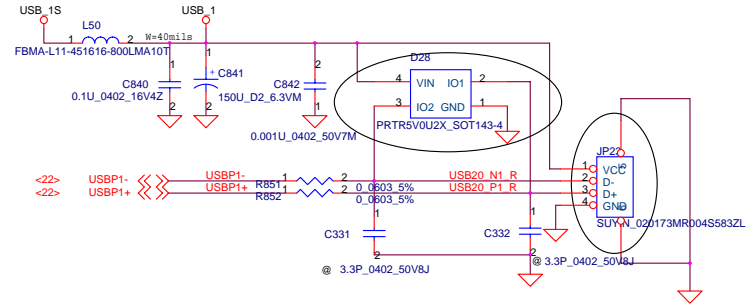


### USB Port 0

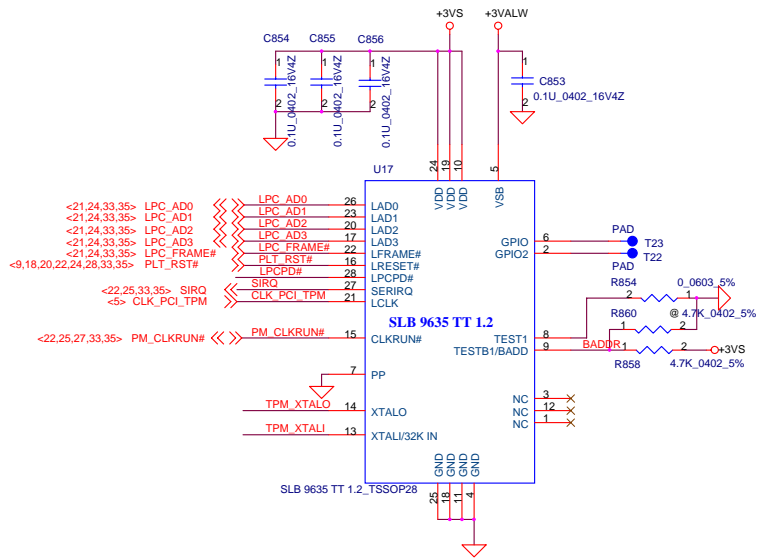


Required by Motion for ESD protect

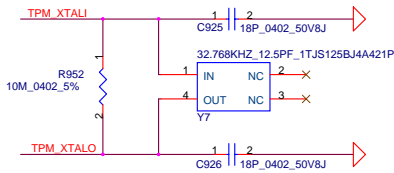
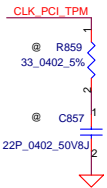
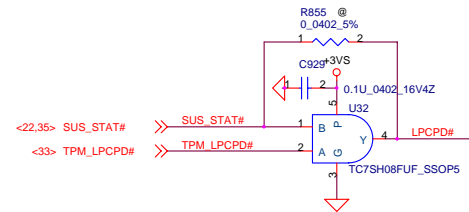
### USB Port 1



### TPM



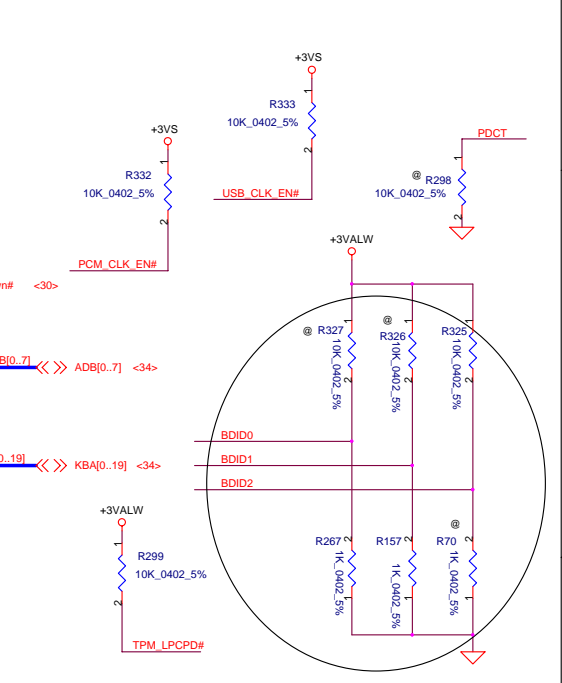
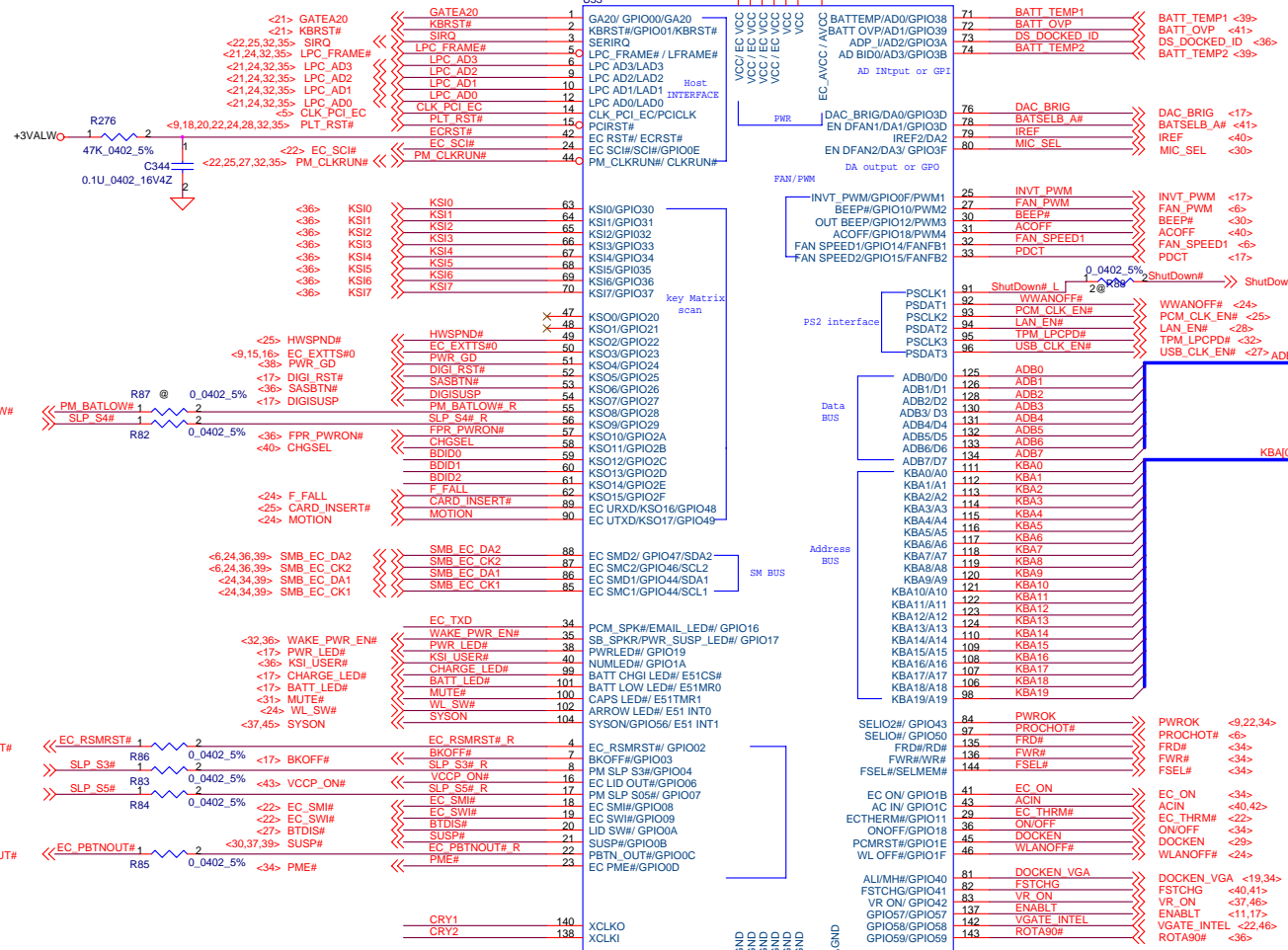
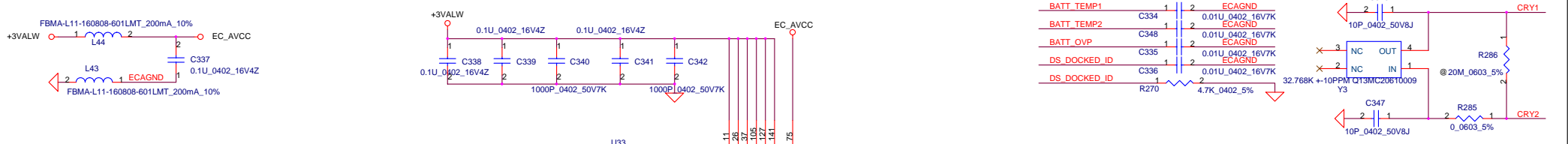
Base I/O Address  
 0 = 02Eh  
 +1 = 04Eh(Default)



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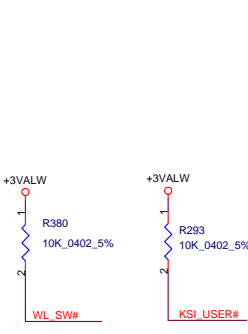
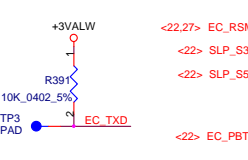
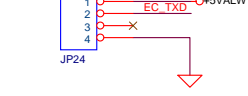
	<b>Compal Electronics, Inc. (KunShan)</b>	
	TPM/USB Port x2	
Size	Document Number	Rev
Custom	<b>PecosII-IDX80-LA329I</b>	X 0.5
Date:	Monday, January 06, 2007	Sheet 32 of 53





**SBBTN: User button as, ALT+CTL+Delete**

@ ACES\_85201-0405



BDID2	BDID1	BDID0	Version	Phase
0	0	0	0.1	EVT1
0	0	0	0.2	EVT2
0	0	0	0.3	DVT1
0	0	1	0.4	Reswork DVT2
0	1	0		Reserve
1	0	0	0.5	PVT
1	0	1	1.0	MP
1	1	0		Reserve
1	1	1		Reserve

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**Compal Electronics, Inc. (KunShan)**

File: **ENE KB910**

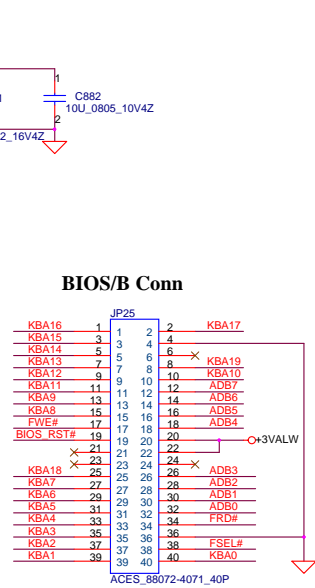
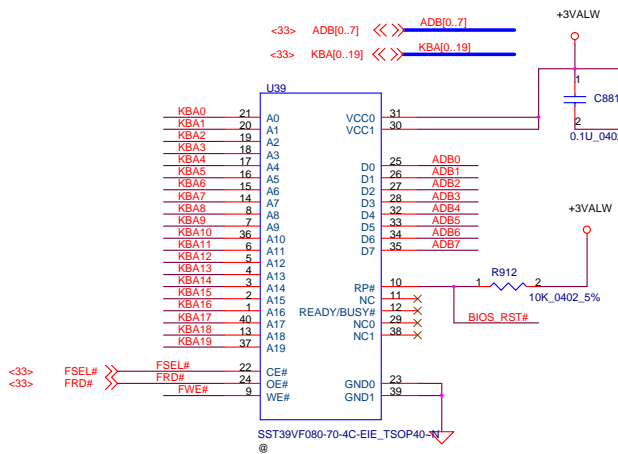
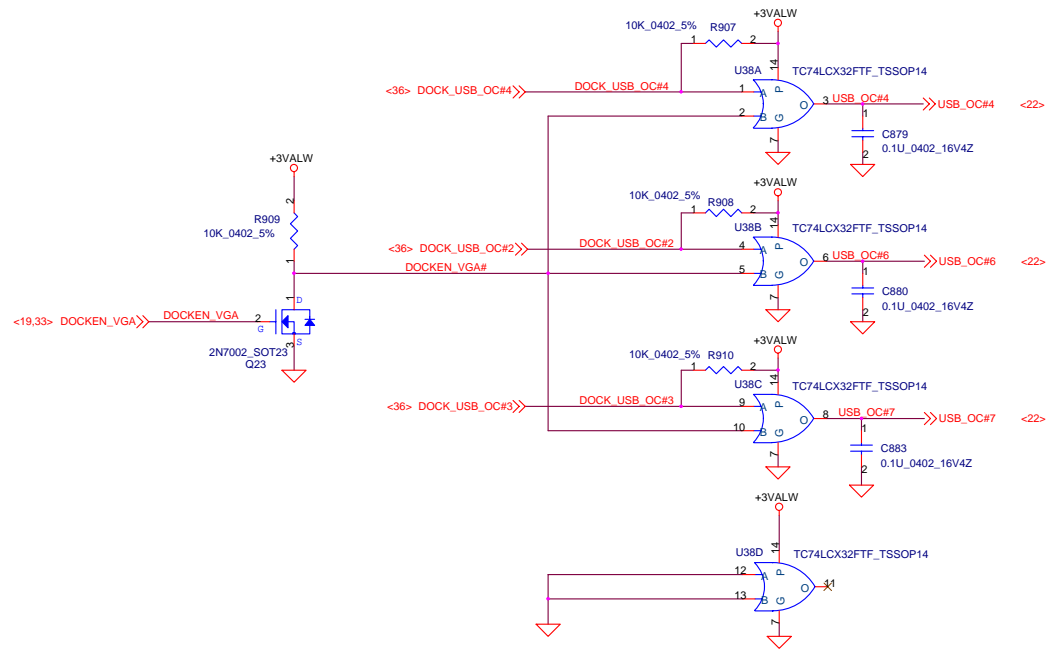
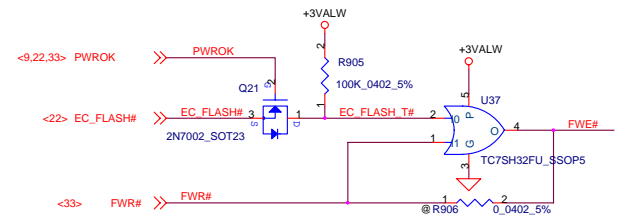
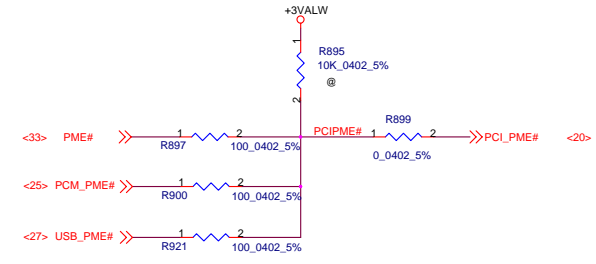
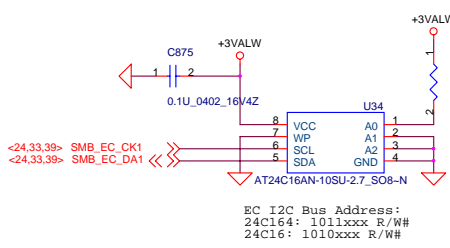
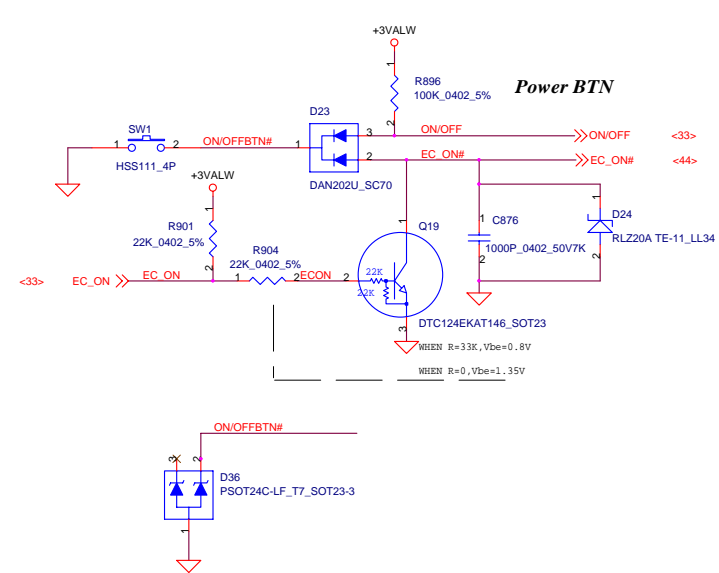
Size: Document Number

Customer: **PecosII-IDX80-LA3291**

Date: Monday, January 06, 2007

Rev: X.0.5

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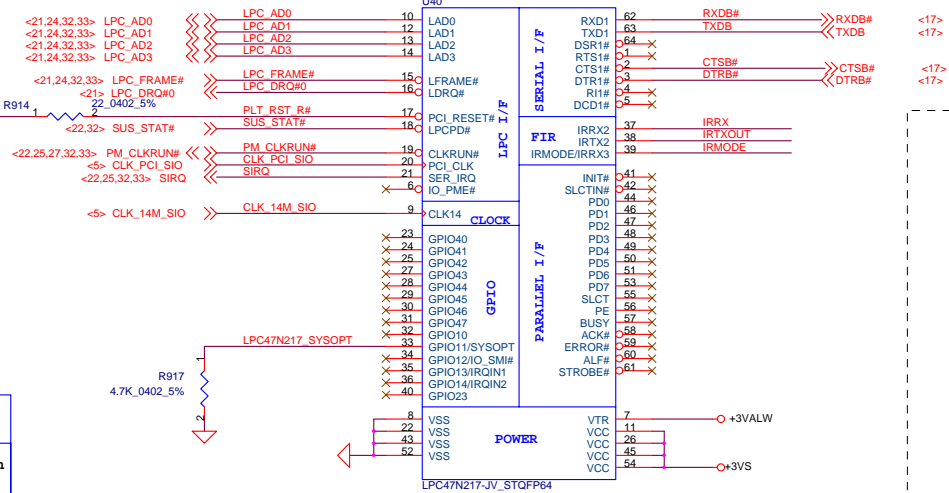
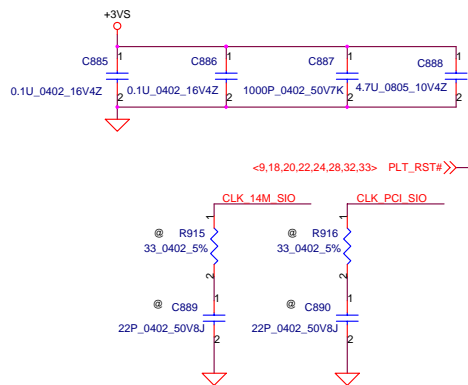
**Compal Electronics, Inc. (KunShan)**

EC Extend I/O&BIOS

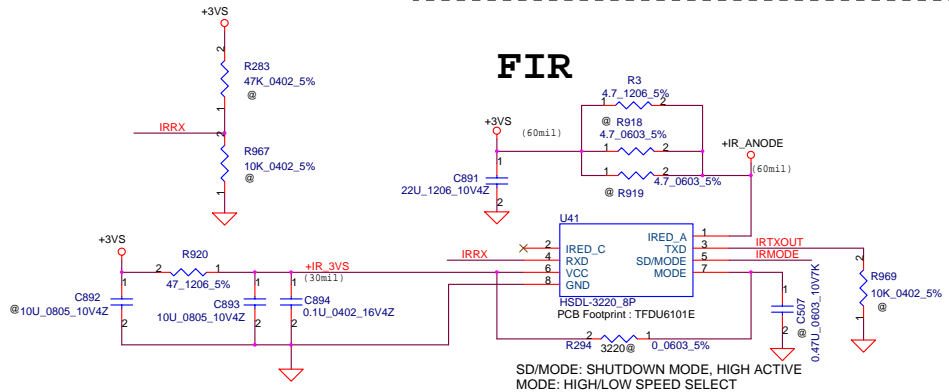
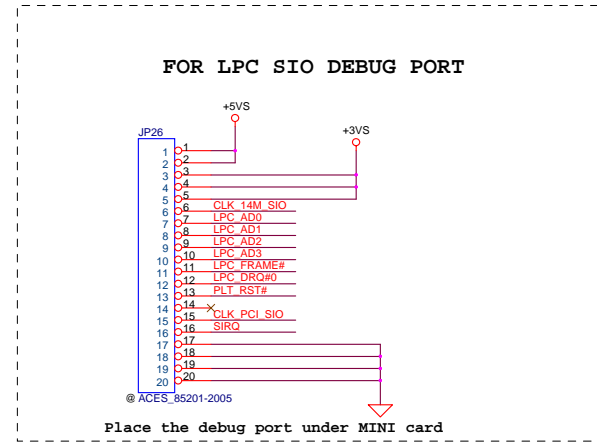
Size: Document Number  
 Date: Monday, January 06, 2007 Sheet 34 of 53

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PecosII-IDX80-LA3291



Strap pin	Pin #	Description
BADDR	33	BASE Address Selection "0": 2E-2F (Default) "1": 4E-4F



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File: **SMSC LPC47N217/FIR**

Size: Document Number

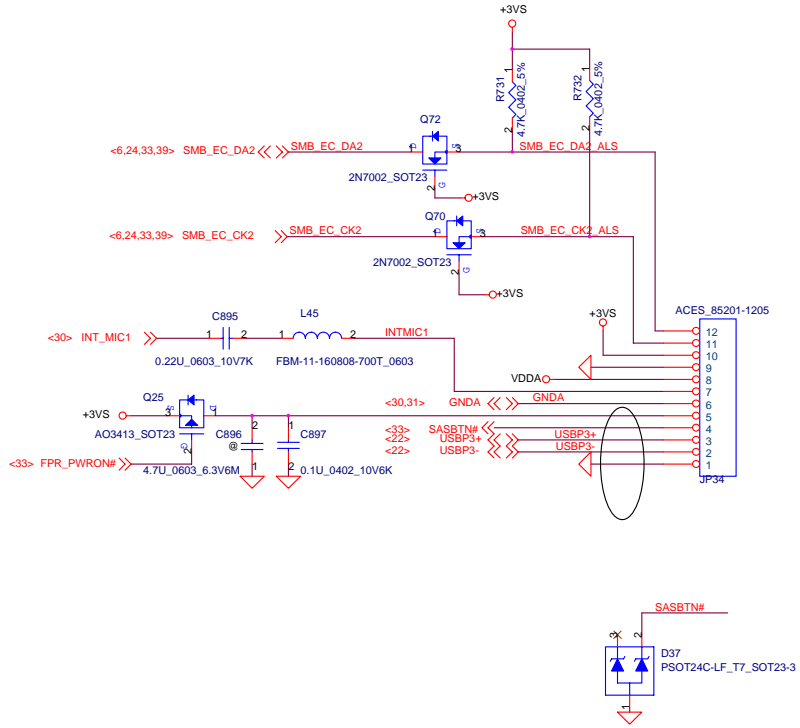
Cust. on: **PecosII-IDX80-LA3291**

Date: Monday, January 06, 2007

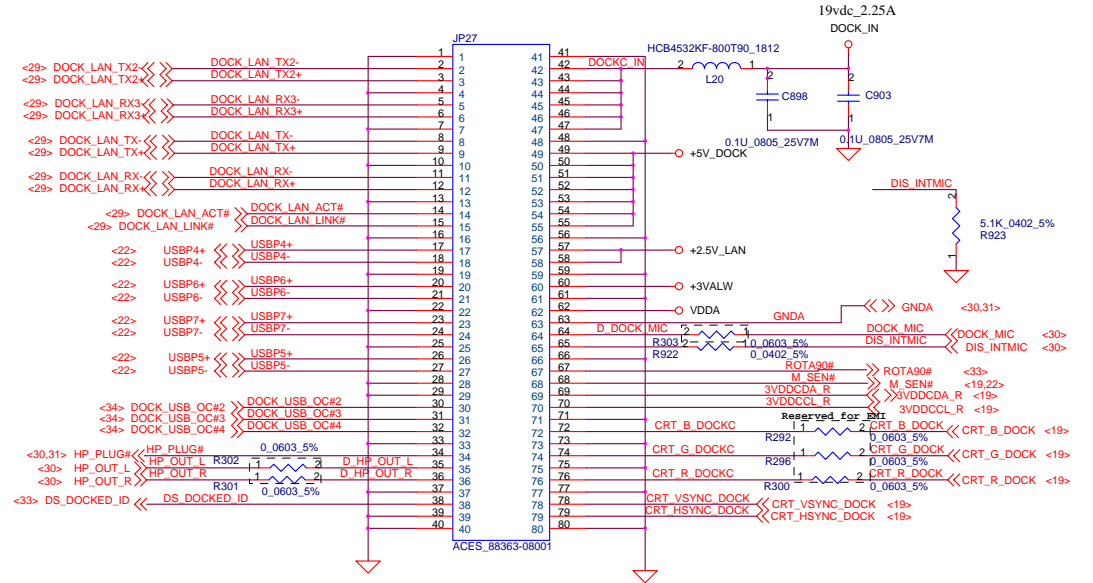
Rev: X 0.5

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# ALS/MIC & Finger Print combine CONN

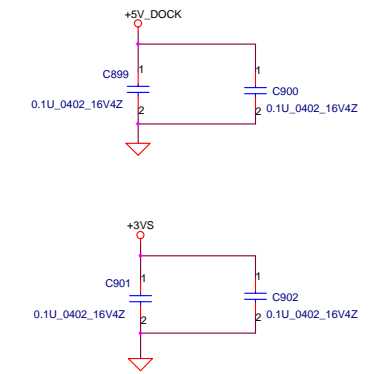
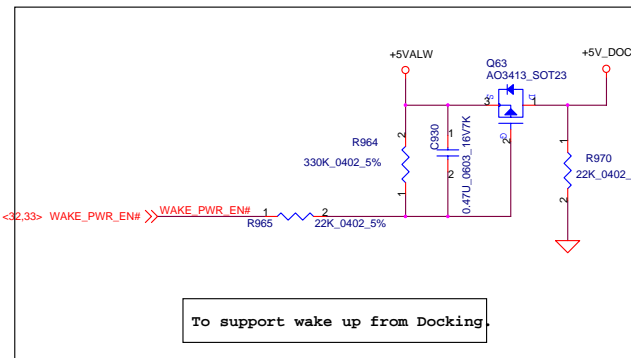
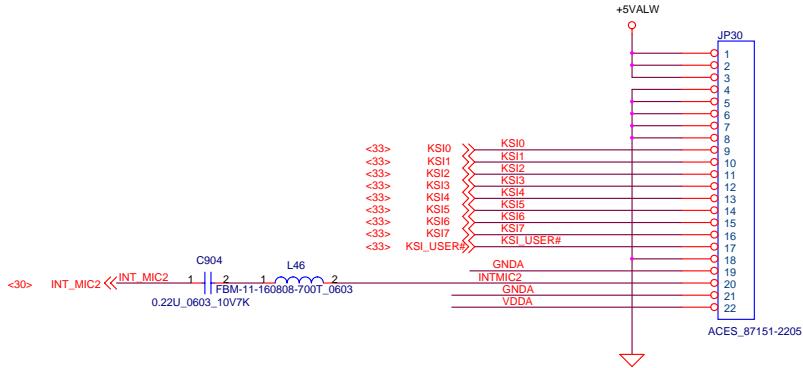


# DOCKING BD.



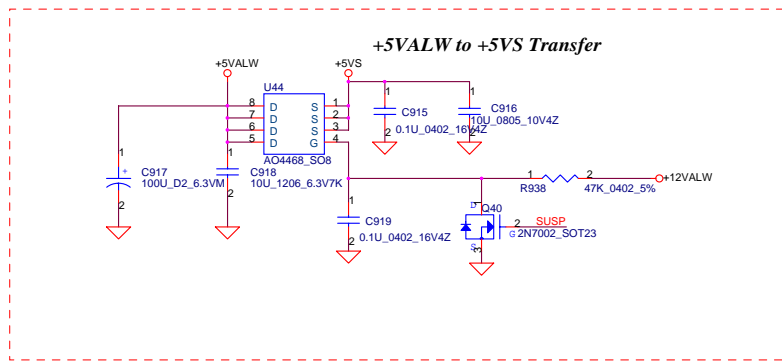
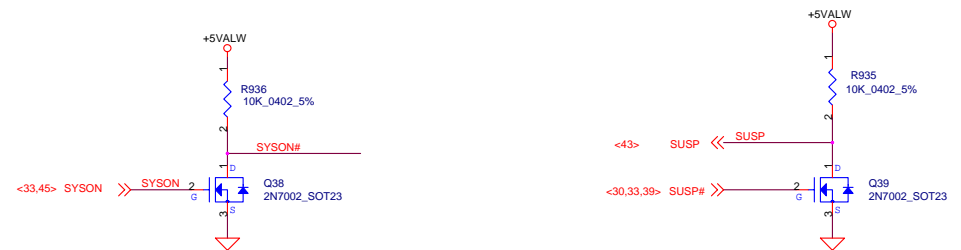
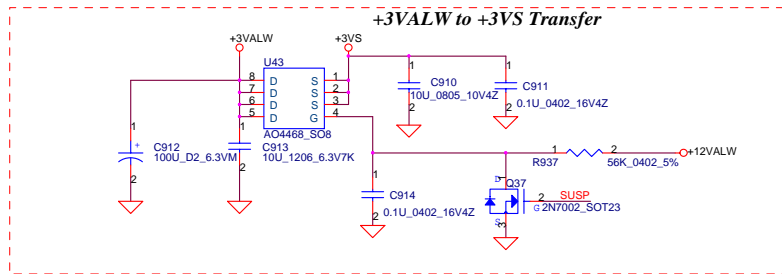
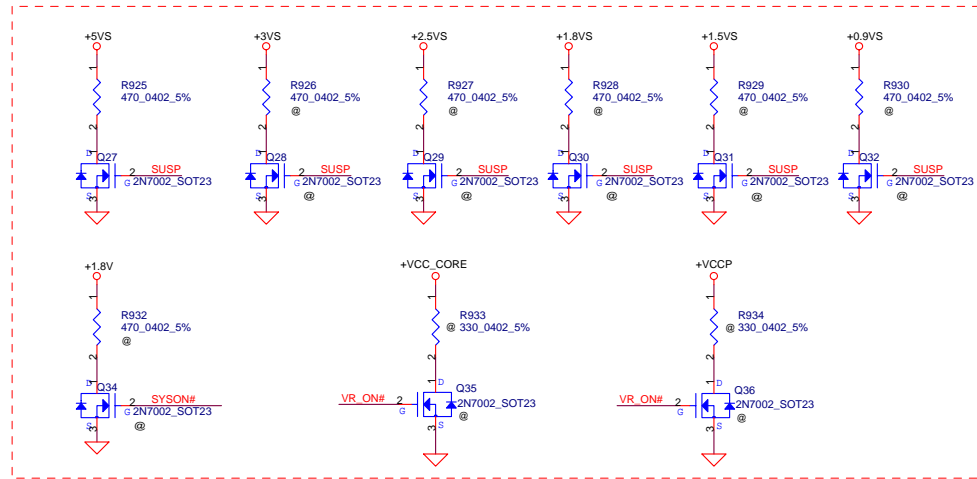
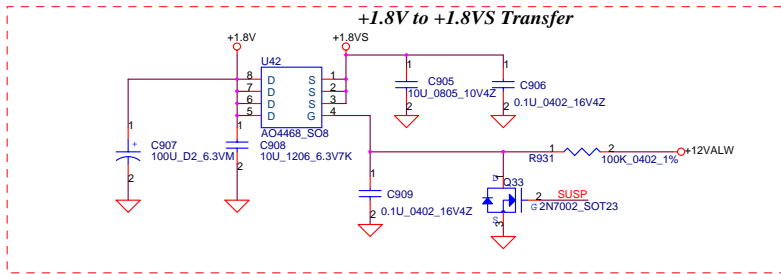
Need to update the Symbol

# To BTN Board



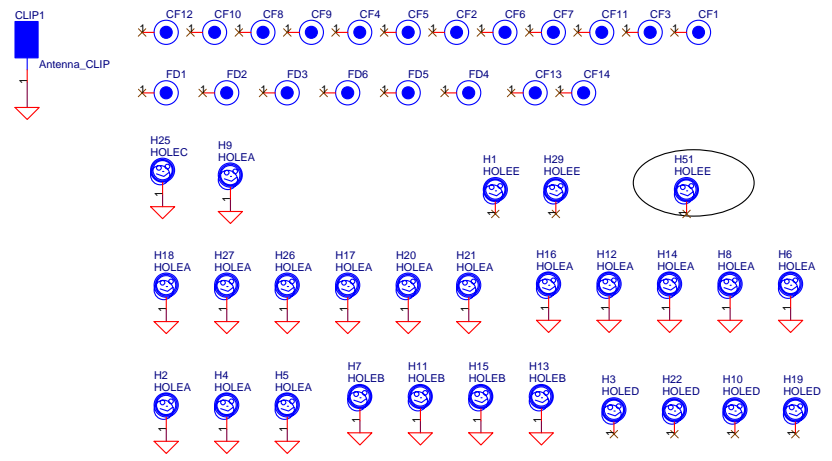
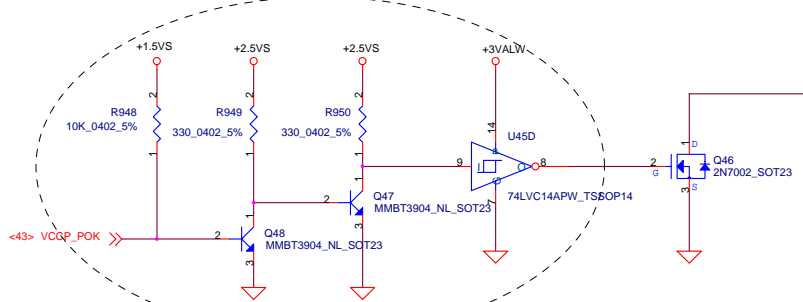
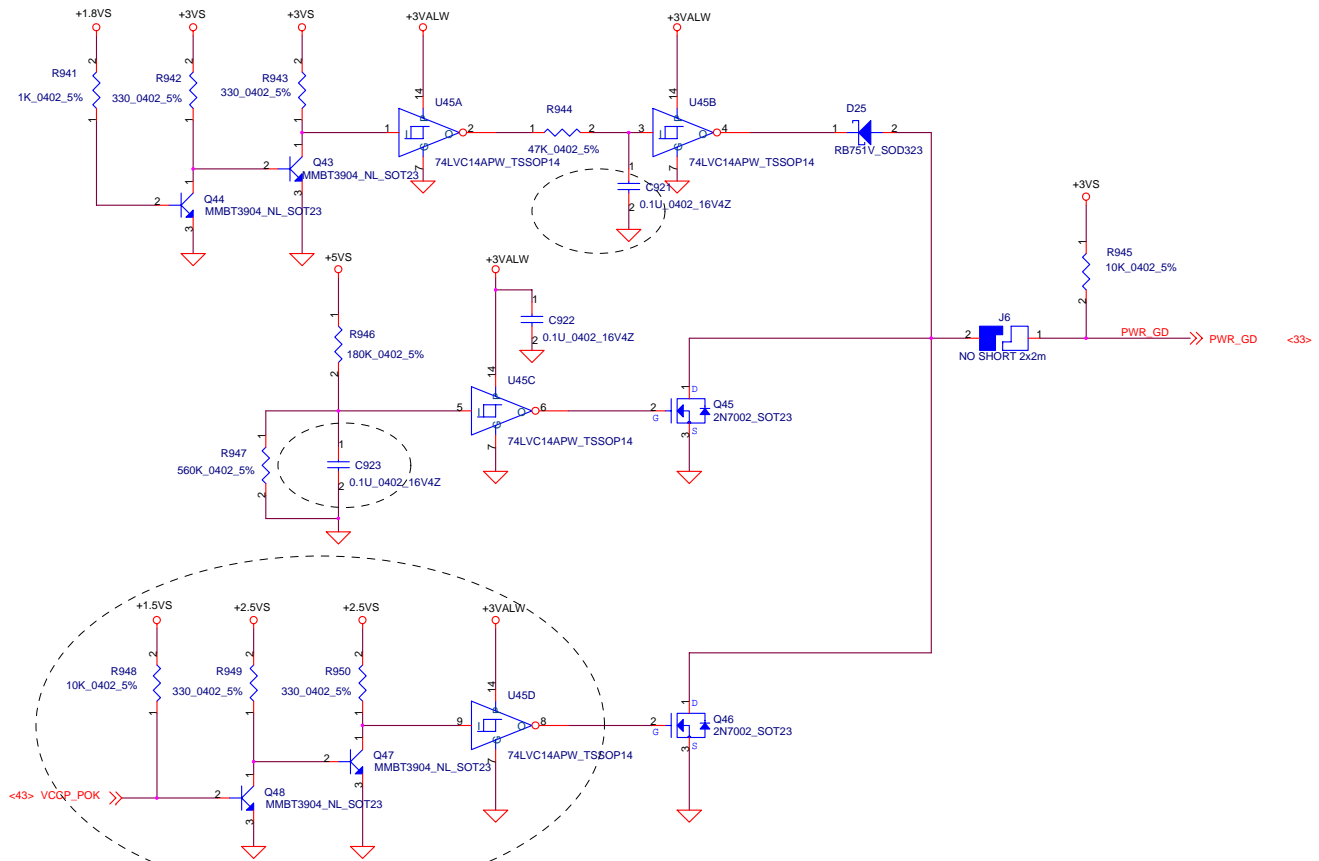
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	Title <b>Docking Conn /FingerPrinter /Button board Conn</b>	
	Size	Document Number
	<b>PecosII-IDX80-LA329I</b>	
Date:	Monday, January 08, 2007	Sheet 36 of 53



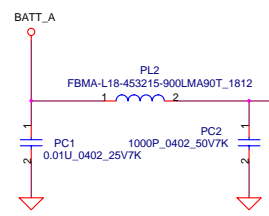
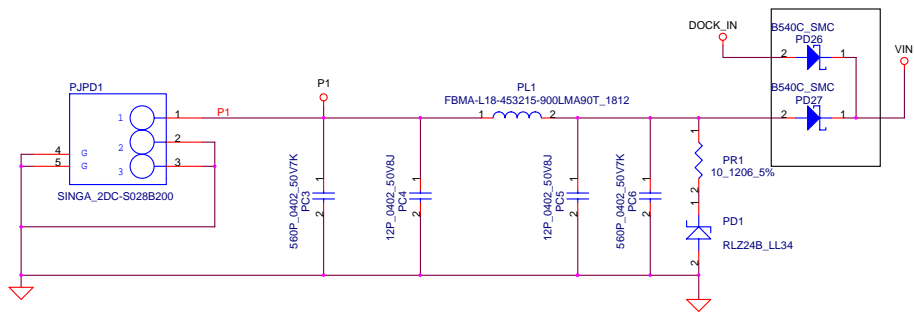
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	<b>Compal Electronics, Inc. (KunShan)</b>	
	DC-DC interface	
Size	Document Number	Rev
Custom	<b>PecosII-IDX80-LA329I</b>	X 0.5
Date:	Monday, January 06, 2007	Sheet 37 of 53

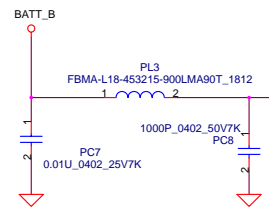
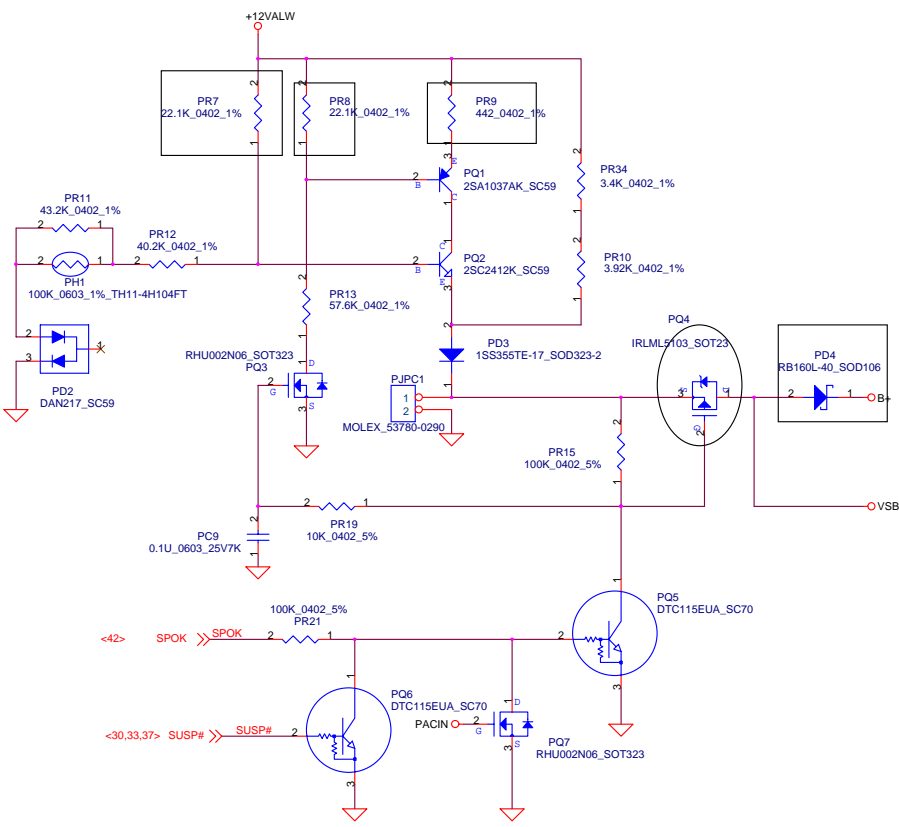
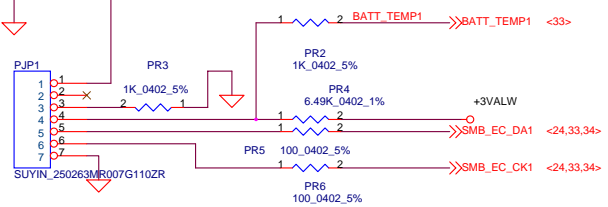


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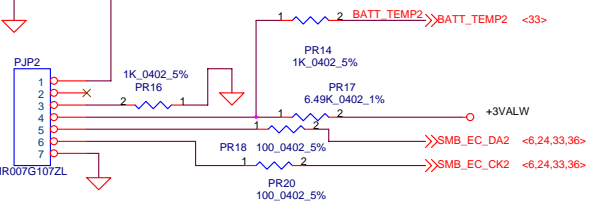
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	<b>POWER OK CKT</b>		
	Size	Document Number	Rev
Date:	<b>PecosII-IDX80-LA3291</b>		X 0.5
	Monday, January 06, 2007	Sheet 36	of 53



**PJP1 battery connector**  
**SMART Battery:**  
 1.BAT+  
 2.ID  
 3.B/I  
 4.TS  
 5.SMD  
 6.SMC  
 7.GND



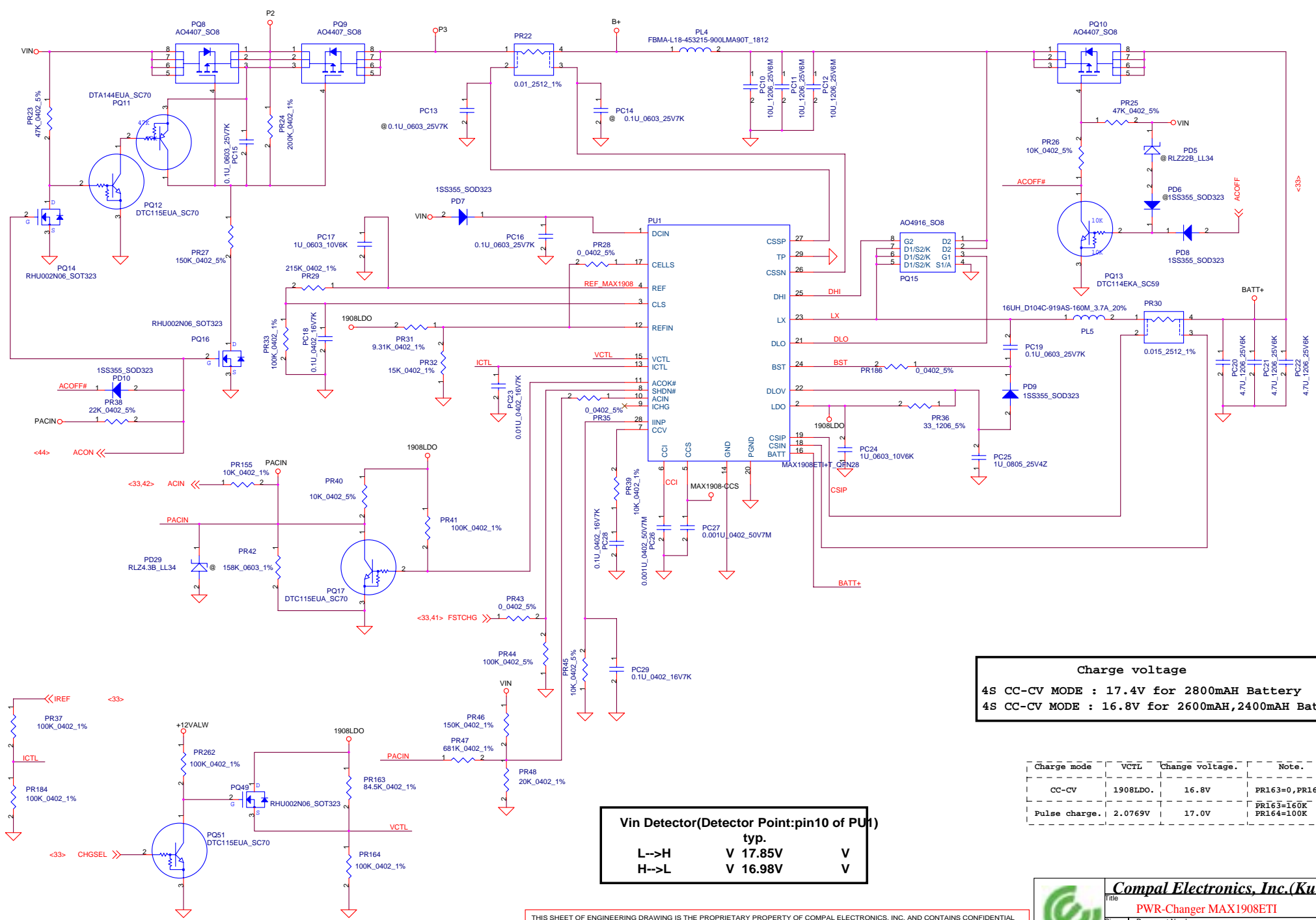
**PJP2 battery connector**  
**SMART Battery:**  
 1.BAT+  
 2.ID  
 3.B/I  
 4.TS  
 5.SMD  
 6.SMC  
 7.GND



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	<b>Compal Electronics, Inc.(KunShan)</b>	
	Title <b>PWR-Vin/bridge Batt/RTC</b>	
	Size Custom	Document Number <b>PecosII-IDX80-LA329J</b>
Date: Monday, January 08, 2007	Sheet 39 of 53	Rev X 0.5

I<sub>adp</sub>=0~2.38A (45.23W)



**Charge voltage**  
 4S CC-CV MODE : 17.4V for 2800mAH Battery  
 4S CC-CV MODE : 16.8V for 2600mAH,2400mAH Battery

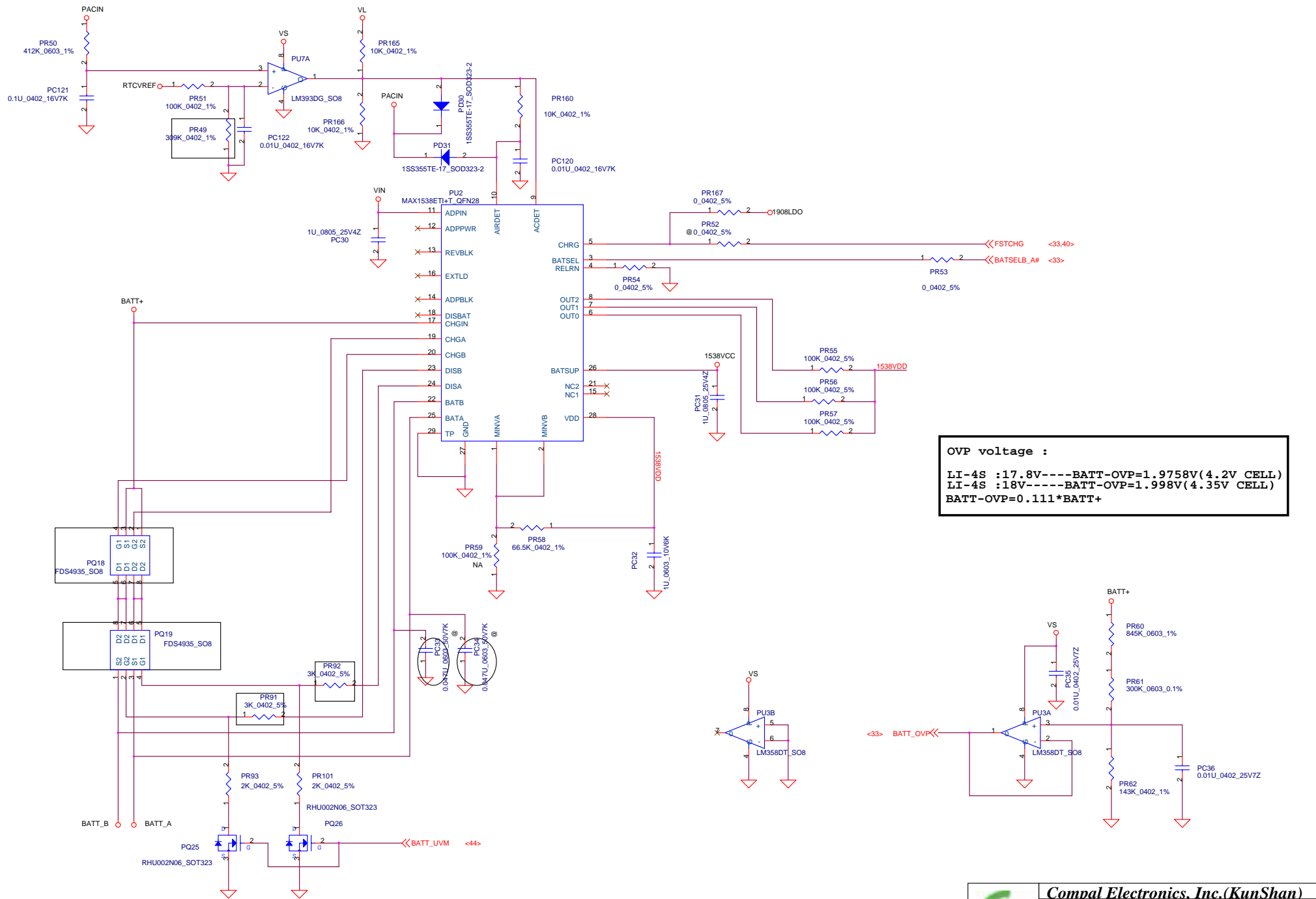
Charge mode	VCTL	Change voltage	Note
CC-CV	1908LDO.	16.8V	PR163=0,PR164=#
Pulse charge	2.0769V	17.0V	PR163=160K PR164=100K

**Vin Detector(Detector Point:pin10 of PU1)**  
 typ.  
 L-->H      V 17.85V      V  
 H-->L      V 16.98V      V

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**Compal Electronics, Inc. (KunShan)**  
 PWR-Changer MAX1908ETI  
 Document Number  
**PecosII-IDX80-LA329I**  
 Date: Monday, January 06, 2007 Sheet 40 of 53






OVP voltage :

LI-4S : 17.8V---BATT-OVP=1.9758V(4.2V CELL)

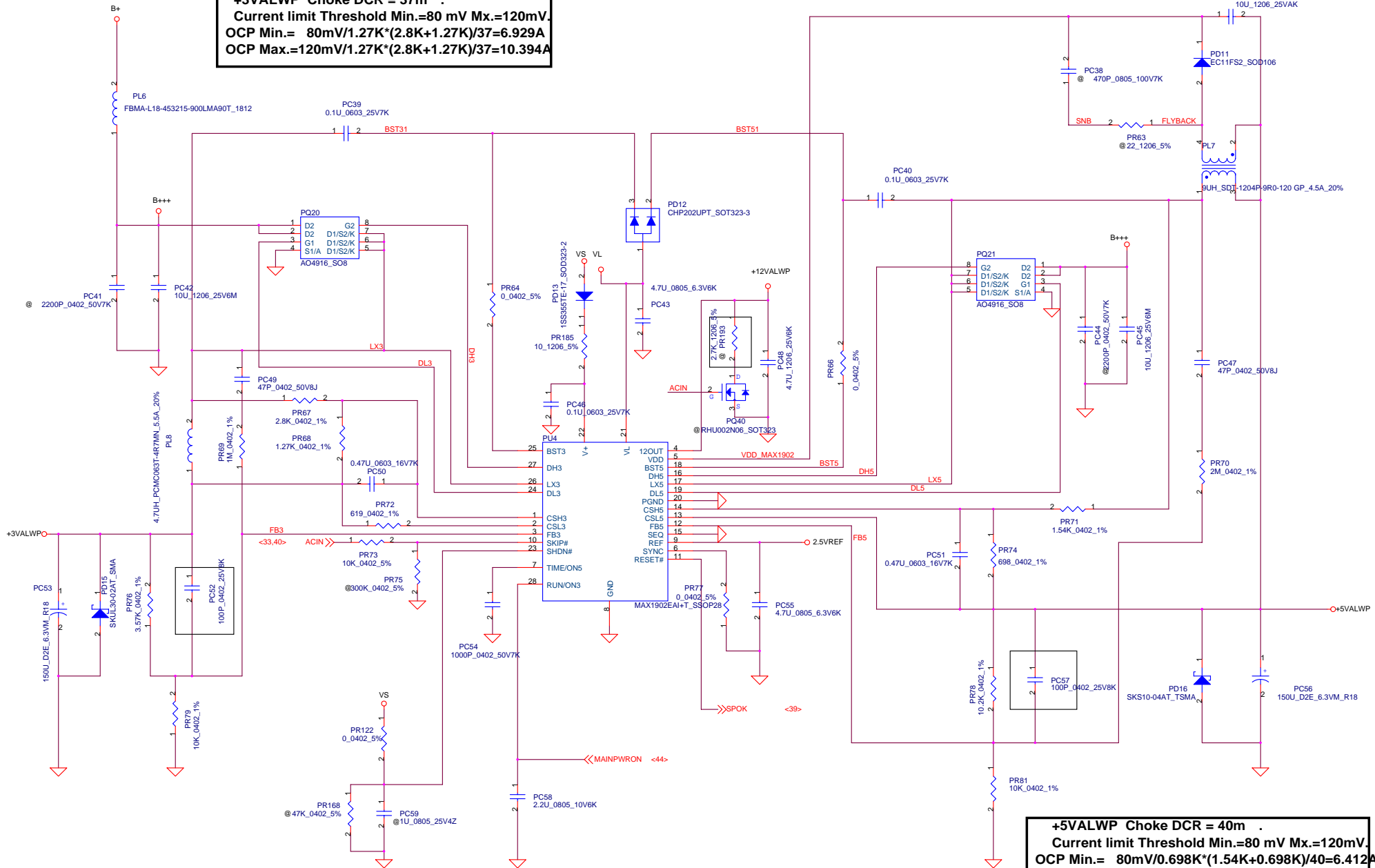
LI-4S : 18V-----BATT-OVP=1.998V(4.35V CELL)

BATT-OVP=0.111\*BATT+

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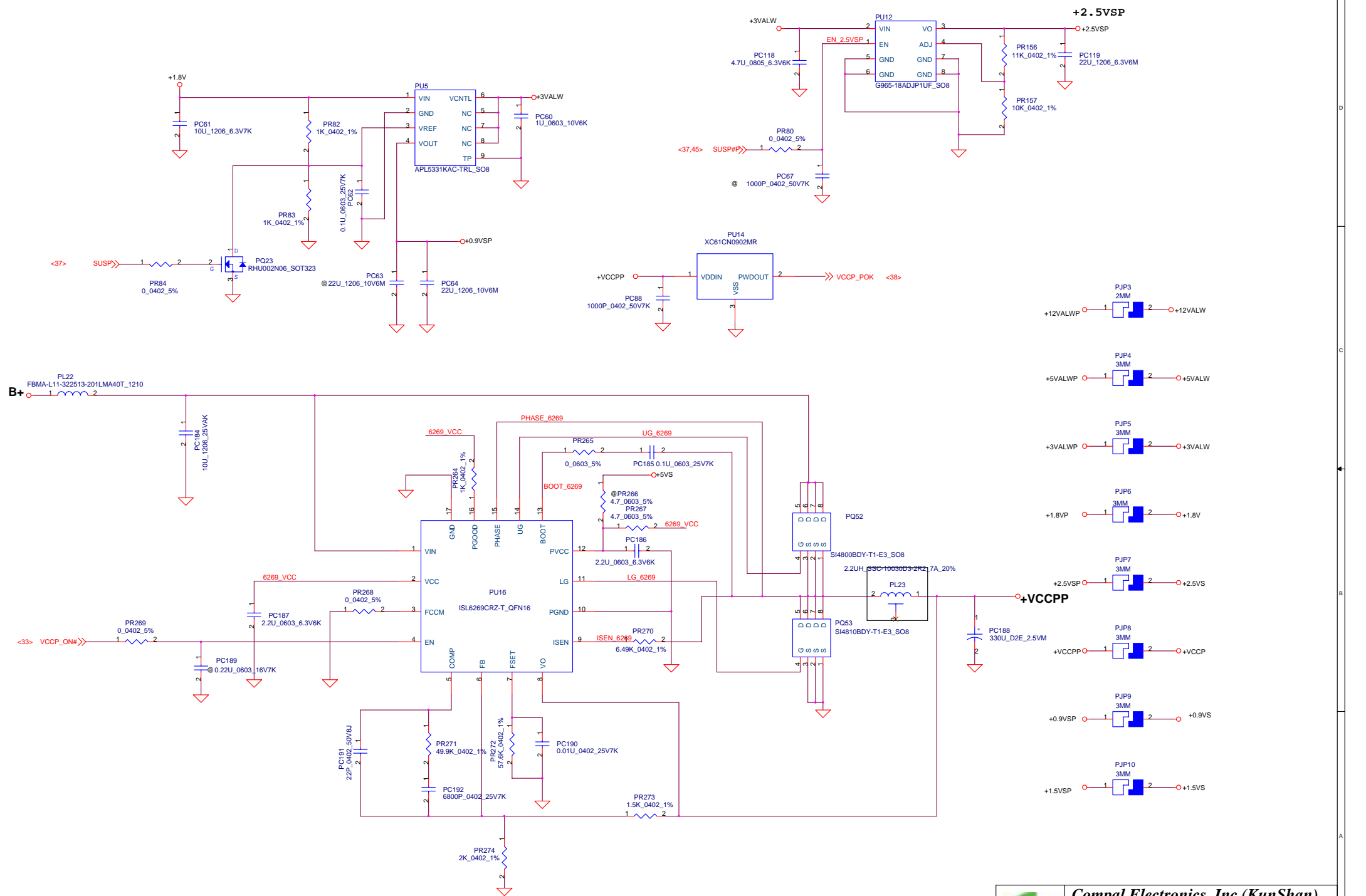
	<b>Compal Electronics, Inc.(KunShan)</b>	
	<b>PWR-Batt Select &amp; OVP</b>	
Size	Document Number	Rev
Cust. or	<b>PecosII-IDX80-LA329I</b>	X 0.5
Date:	Monday, January 06, 2007	Sheet 41 of 53

**+3VALWP Choke DCR = 37m .  
Current limit Threshold Min.=80 mV Mx.=120mV,  
OCP Min.= 80mV/1.27K\*(2.8K+1.27K)/37=6.929A  
OCP Max.=120mV/1.27K\*(2.8K+1.27K)/37=10.394A**




**$RS2(PR64)=RS1(PR58)*RS3(PR61)/(RS1+RS3)$   
 $L/RL(DCR)=RS1*RS3(PR61)/(RS1+RS3)*Cs(PC56)$**

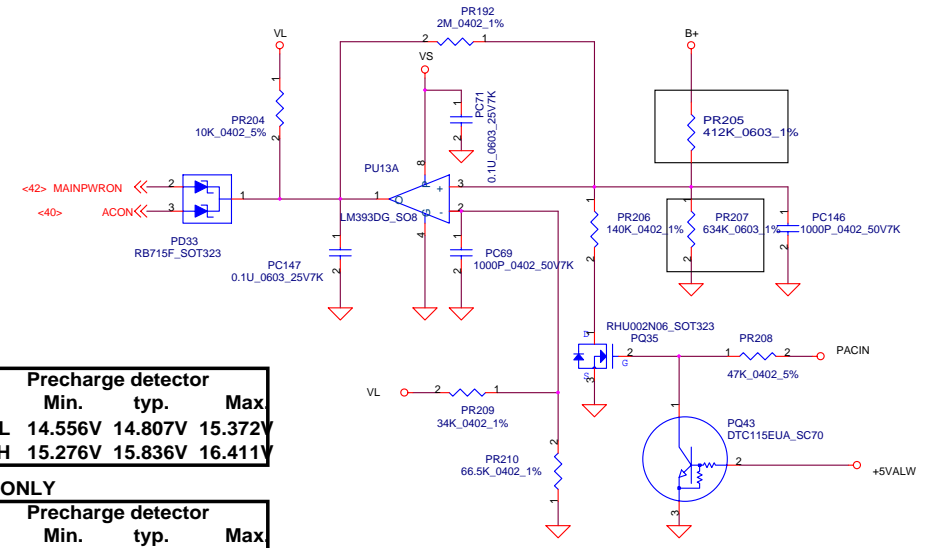
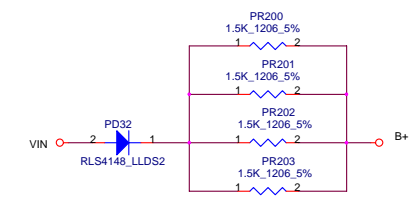
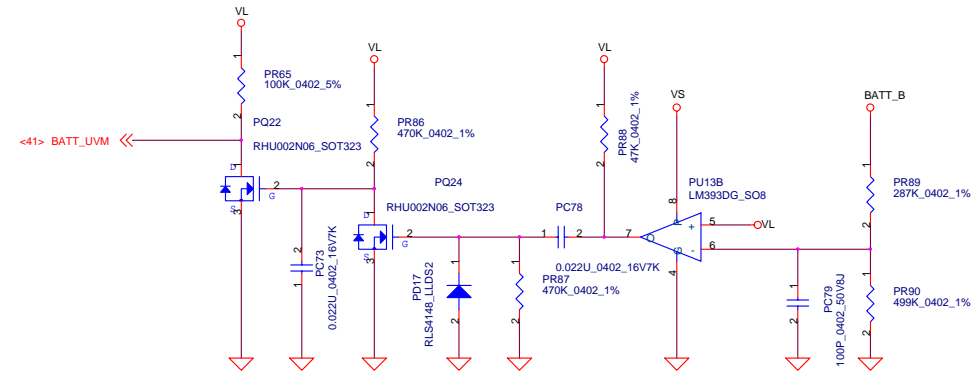
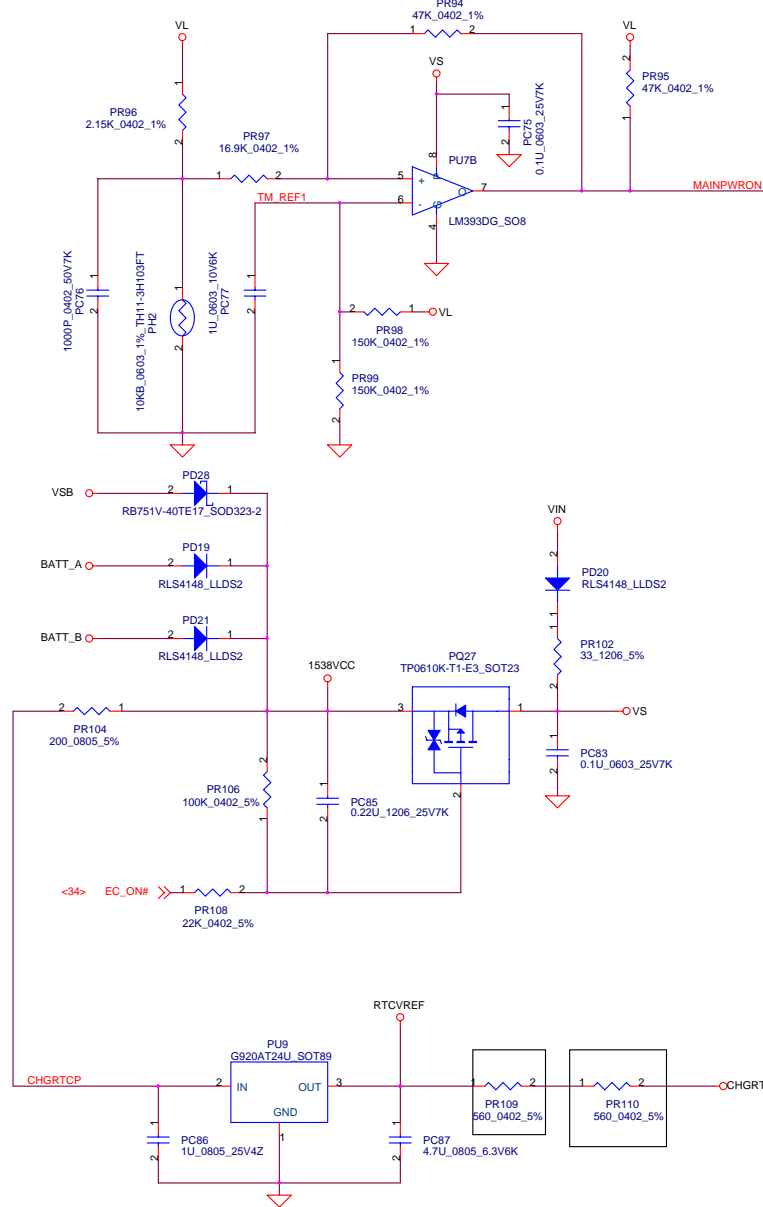
**+5VALWP Choke DCR = 40m .  
Current limit Threshold Min.=80 mV Mx.=120mV,  
OCP Min.= 80mV/0.698K\*(1.54K+0.698K)/40=6.412A  
OCP Max.=120mV/0.698K\*(0.698K+1.54K)/40=9.593A**



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	<b>Compal Electronics, Inc. (KunShan)</b>		
	<b>+0.9VSP&amp;VCCP&amp;+2.5</b>		
	Size	Document Number	Rev
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PH2 under CPU botten side :  
 CPU thermal protection at 80 degree C  
 Recovery at 44(45) degree C




**ACIN**

	Precharge detector	Min.	typ.	Max
H-->L	14.556V	14.807V	15.372V	
L-->H	15.276V	15.836V	16.411V	

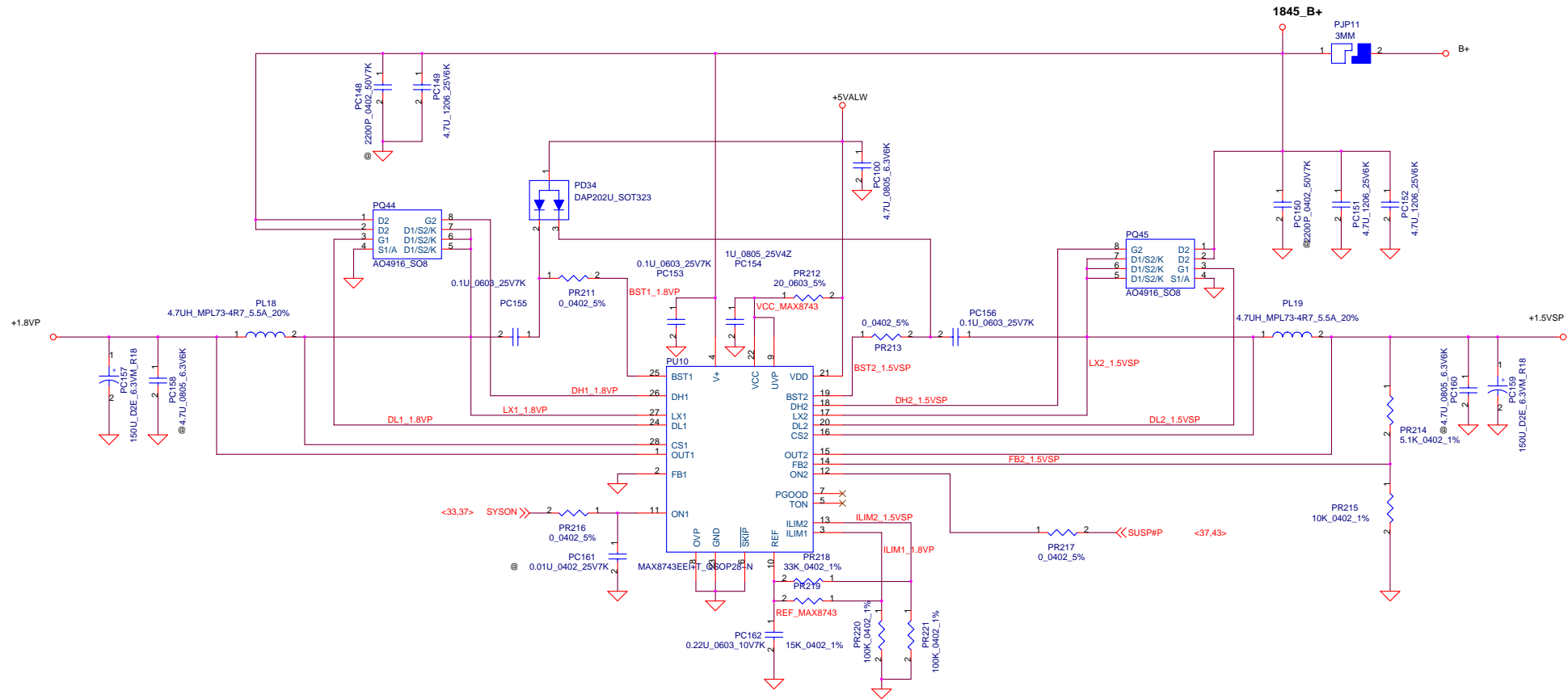
**BATT ONLY**

	Precharge detector	Min.	typ.	Max
H-->L	5.044V	5.096V	5.205V	
L-->H	6.008V	6.124V	6.243V	


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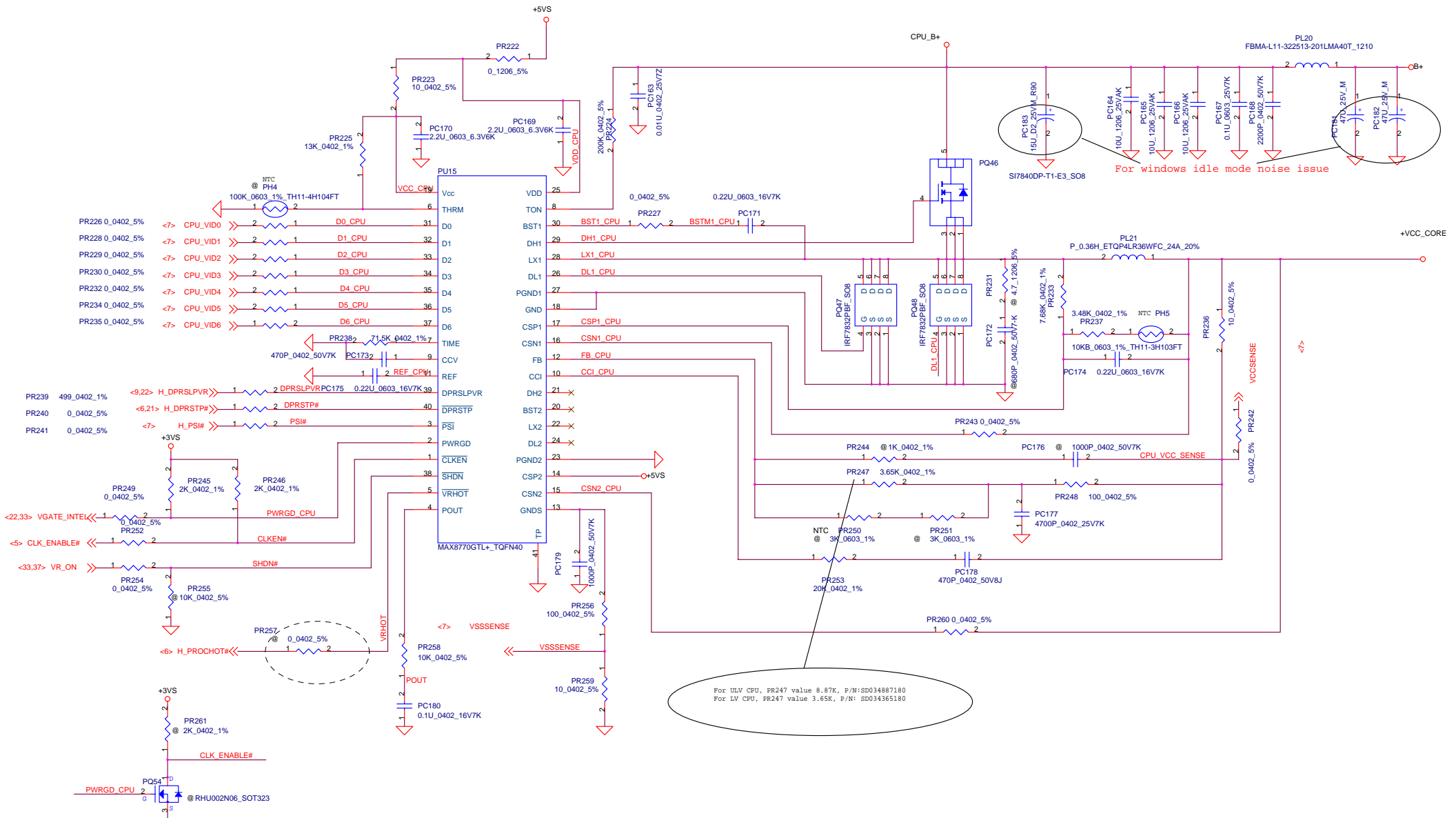


**Compal Electronics, Inc. (KunShan)**  
 Title: RTC Batt&OTP&Pre-charge  
 Size: Document Number  
 Date: Monday, January 06, 2007  
 Sheet: 44 of 53  
 Rev: X 0.5  
 PecosII-IDX80-LA3291



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	<b>Compal Electronics, Inc. (KunShan)</b>	
	<b>+1.5VSP &amp; +1.8VP</b>	
File	Document Number	Rev
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For windows idle mode noise issue

For ULV CPU, PR247 value 8.87K, P/N:SD034887180  
 For LV CPU, PR247 value 3.65K, P/N: SD034365180

$$Tsw = Cton(Rton + 6.5k) \quad Cton = 16.26pf$$

$$f = 1 / Tsw = 1 / Cton(Rton + 6.5K)$$

$$= 1 / 16.26pf(200k + 6.5k) = 297.824khz$$

$$Rton = PR224$$


PR261, PQ54 will be populated when MAX8870 Rev0.2 is used.

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	<b>Compal Electronics, Inc. (KunShan)</b>	
	<b>PWR-CPU-CORE</b>	
Size	Document Number	Rev
Cust. no.	<b>PecosII-IDX80-LA329I</b>	X 0.5
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	<b>Compal Electronics, Inc. (KunShan)</b>		
	Title <b>Power up Sequence</b>		
Size	Document Number	Rev	
Cust. no.	<b>PecosII-IDX80-LA329I</b>	X 0.5	
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# HW P.I.R LIST

Change item	Change reason	Page#	Date	Revision
1. ADD 100K ohm pull-down resistor on ENVDD	Follow Intel suggestions	P18	9/05/05	X0.1
2. ADD one more Panel ID, PID0 to support more panel	Required by Mothion	P18	9/05/05	X0.1
3. Add R791, Del R877	Use LED signal from Minicard to control RF LED directly, Required by Mothion	P28, P34	9/28/05	X0.1
4. Add R46,R31,R32,JP32 and Q12, Del JP31	Support SD card function and cancel the Smart card function	P25, P26	1/11/06	X0.1
5. Change the net of R22 pin 2 from CLK_48M_SC to CLK_48M_SD	Support SD card function and cancel the Smart card function	P5	1/12/06	X0.1
6. Add R37,R42 to pull high LCTLA_CLK & LCTLB_DATA	Follow Intel Rev 1.601 design check list	P11	1/12/06	X0.1
7. Add U19, C610, Delete D26,D30 and populate R636	Follow Intel Rev 1.601 design check list to pull down ENABL7	P17	1/12/06	X0.1
8. Delete R668,R732	No need these pull high resistor for setting the Boot BIOS destination	P20	1/12/06	X0.1
9. Add an unpopulated resistor R676	Reserved for the future.	P21	1/12/06	X0.1
10. Unpopulate R895	Use the internal pull high of ICH7	P34	1/12/06	X0.1
11. Swap the USB port 3 and port 4 to the docking connector JP27	Follow Motion's request	P36	1/12/06	X0.1
12. Add R48 and C800	Tune regulator power sequence to insure AVDD rail should come up after the DVDD rail	P30	1/14/06	X0.1
13. C26,C32,R59,R60 only populate for 9220; R59,C798,R58,C799,R61 populate for 9204	For 9220 and 9204 co-layout	P30	1/14/06	X0.1
14. change C826/827 from 47uF to 220 uF	Follow Sigmatel suggestions	P31	1/14/06	X0.1
15. Depopulate C846/C847	Follow Sigmatel suggestions	P31	1/14/06	X0.1
16. Change cardbus signals SPKROUT and HWSPND# pull high power to +3V_R5C843 from +3VALW	Follow FAE check list request	P25	1/16/06	X0.1
17. Add JP31,U19 and related components; delete JP32,Q12 and related components	Follow Motion change: add SC, delete SD	P26	1/17/06	X0.1
18. Add layout notice for CCLK/CARD16	Follow FAE check list request	P25	1/19/06	X0.1
19. Add C71	Follow FAE check list request	P25	1/19/06	X0.1
20. Pull cardbus signals TPBP0/TPBN0/TPBP1/TPBN1 to ground	Follow FAE check list request	P25	1/19/06	X0.1
21. Remove U28 and add R1/Q12	Follow motion request: shutdown amplifier to save power in S3 state	P31	1/24/06	X0.1
22. Signal mute# change into mute	Match Item 21 request	P31,P33	1/24/06	X0.1
23. Delete R879, R880 and cancel the net of DDR_ID0, DDR_ID1	Delete the unused DDR_ID0 and DDR_ID1	P33	2/13/06	X0.1
24. JP1 and Add U8	Update the package of CPU from uFCPGA to uFCBGA	P33	2/13/06	X0.1
25. Delete U21, ADD U27	Change the USB HUB to USB controller	P27	2/21/06	X0.1
26. Delete U1, Add U46	Change the clock Gen to compal part	P5	2/21/06	X0.1
27. Move the net ACOFF from U33 pin31 to U33 pin80 Add the net LED_PWM	Use the PMW signals from EC to control the brightness of LED	P33,P36	2/21/06	X0.1
28. Delete the R953	Follow Intel USA suggestions	P22	3/01/06	X0.1
29. Delete the R951, R853	Follow Motion's request	P32	3/02/06	X0.1
30. update the Docking connector's symbol	Change the Docking con from 100 pins to 80pins	P36	3/02/06	X0.1
31. Del U23 and relative components, add U47 and relative components	Change the Smart card controller from O2 to Omnikey	P26	3/03/06	X0.1
32. Del U27&JP31 and relative components	Remove the Smart card function	P26	3/07/06	X0.1

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	Hardware PIR list		
Title	Document Number		Rev
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Date	Monday, January 06, 2007		
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# HW P.I.R LIST

Change item	Change reason	Page#	Date	Revision
33.Add Q15, JP32 and relative components	Follow Motion's request add SD card feature	P26	3/07/06	X0.1
34.Del LED_PWM, Add PWM_CTL to Q14 pin 2	Follow Motion's solution for LED dimming control	P17	3/09/06	X0.1
35. Add the location for R775,R777,R778,R782,R781,R783 and R476	Reserve the locations for Port 80H debug card when debugging	P24, P5	3/09/06	X0.1
36. Reassign the pin net of Docking	Put the anlog power and analog GND together to get get better placement and return loop.	P36	3/13/06	X0.1
37. Add CF13,CF14 and Del H23, H24,H28,CL2,CL3	New PCB and new feature requirement	P38	3/13/06	X0.1
38. Add the locations for C431,C432,C425,C426,C427 C458,C437,C438C444,C445	Reserve the locations for 10uF caps in case of world wide shortage of 22uF caps	P8	3/13/06	X0.1
39. Change the net of R747.2 from ICH_AZ_CODEC_SDIN0 to SDATA_IN	Correct the net error	P30	3/15/06	X0.1
40. Add C271	Connect GND and LAN shield	P29	3/15/06	X0.1
41. change +0.9V to +0.9VS for VTT of DDR	Power net error	P16	3/21/06	X0.1
42.Populate R918	follow Vishay's suggestion	P35	3/21/06	X0.1
43.Delete Q12, add U31 and unpopulate R1, change MUTE to MUTE#	to avoid the current leakage when MUTE ative and no Headphone plugging in S0	P31	3/22/06	X0.1
44.Add R73, R74	For debug use only	P27	3/24/06	X0.1
45. Update JP24 symbol	Use small footprint for layout space saving	P33	3/24/06	X0.1
46.ADD D34,D35,D36,D37,D38,D39,D40,D41,D42,D43,D44	Add the location of ESD protection Diode for HSYNC, VSYNC, ON/OFFBTN#, WL_SW# and DVI signal lines.	P19,P34,P36, P24,P18	3/30/06	X0.1
47.Delete R772	remove the dual pull-up resistors for WL_SW#	P24	3/31/06	X0.1
48.Delete Q7, Add D45	update symbol	P17	4/07/06	X0.1
49.Add R472,R473,R478,R479,C359,C360,C361,C362	Add these components for signal quality of SD.	P25	4/10/06	X0.1
50.Add R951, R953, R964, R965, C930 and Q63	To support usb wake up from docking and wake up function can be selected by user.	P32,P36	5/12/06	X0.2
51.Delete R775 ;pin10,pin12,pin14,pin16 of JP13 net swap	Delete the useless power and change error the LPC nets for port 80H debug card	P24	5/12/06	X0.2
52.Add R2	To pull high HP_PLUG# to give it a stable status.	P31	5/12/06	X0.2
53.Add R480, C363	To reduce the SD_CMD's overshoot and undershoot	P25	5/15/06	X0.2
54.Add C611, C612,C619,C625	Follow Motion's request	P15,P16	5/15/06	X0.2
55.Add H51, JP12,JP22,JP23	Add a hole to fix HDD FPC, symbols of VGA connentor and usb connectors update for ME requirement	P38,P19,P32	5/24/06	X0.2
56.Add C633,C671,C672,C677	Follow motion's request	P49,P17	5/24/06	X0.2
57.unpopulate R73	To solve the issue of system hangup when enable NEC controller	P49,P27	5/26/06	X0.2
58.reassign the docking usb ports to ICH7	To support DOS mode for all docking ports	P22,P36	5/26/06	X0.2
59.Delete Q62,Q13,R776,R780,R791,R924	Remove LEDs for HDD,B/T and WWAN,WLAN	P17,P27,P24	5/26/06	X0.2
60.Add D6,D9,D13,R4,R7,R8	Support the LEDs change to M/B	P17	5/29/06	X0.2
61.Add two nets of WLAN_SW_EN, WWAN_SW_EN on U33,JP30	Follow SED request for supprting antenna's switching	P33,P36	5/29/06	X0.2
62.Change nets of JP6.24, JP6.36 from GND to +3vs, add R263,R262	follow motion's request of reserving 4 power wires for N-trig	P17	6/01/06	X0.2
63.Change Q52, from AO3402 to SI3456, JP13&JP28 pin24 from+3VALW to +3V_LAN	To support WOWLAN & WOL in AC only mode	P28,P24	6/06/06	X0.2
64.Change +3VALW of U27 to +3VS,Del R315, change USB_SMI# from U9.E21 to U9.AC18, populate R346,R320, unpopulate R312,R321	For more power saving and extendeng the life of bridge batter in S3 mode	P27,P22	6/06/06	X0.2
65.Swap the nets of U46.16&U46.17	modify the wrongly connected SMBus of clock Gen, to solve the issue of C3 hang up	P5	6/06/06	X0.2
66.Add R641, R633, change the net of PID1 to ID0	add ID0, ID1 two hw strap pins to identify the N-Trig Wacom or TouchKo	P17,P22	6/07/06	X0.2


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	<b>Compal Electronics, Inc. (KunShan)</b>		
	Title Hardware PIR list		
Size	Document Number	Rev	
Substom	<b>PecosII-IDX80-LA329I</b>		X 0.5
Date:	Monday, January 08, 2007		
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# HW P.I.R LIST

Change item	Change reason	Page#	Date	Revision
67.Change R8 from 150ohm to 2.2K	Solve LED no light issue	P17	7/17/06	X0.3
68.Swap cardbus controller U15B pinV14/W14 net names	Solve new card can not be detected issue	P25	7/17/06	X0.3
69.Change H26/H27 size from 110 to 165	Solve standoff too big & hole too small to dock-MB/B can not fix well issue	P38	7/17/06	X0.3
70.Add PID and ID table; change LCD connector symbol	Be beneficial to look at schematic; connect NC pin for EMI providing	P17	7/17/06	X0.3
71.Delete H50	No use	P38	7/17/06	X0.3
72.Change block diagram	Follow Motion requirement	P2	7/27/06	X0.3
73.Add R3, unpopulate R918/R919	Solving Irda communication information occur error issue	P35	7/31/06	X0.3
74.Populate R17/R18	Follow EMI requirement	P30	7/31/06	X0.3
75.Change R11 to L21	Follow EMI requirement	P30	7/31/06	X0.3
76.Change U42/U43/U44 from AO4422 to AO4468	AO4422 will EOL, AO4468 will substitute it	P37	7/31/06	X0.3
77.Add new JP34, delete old JP29/JP34	Solving DFX issue	P36	7/31/06	X0.3
78. Add mark LV@ on +VCC_CORE 12*22U & 2*330U decoupling capacitors	For Motion requirement	P8	7/31/06	X0.3
79. Add unpopulate R698/C678	Following Motion requirement for providing EMI	P27	8/1/06	X0.3
80. Add unpopulate R699/C679	Following Motion requirement for providing EMI	P25	8/1/06	X0.3
81. Add series resistors R700/R707	Following Sigmatel requirement	P31	8/1/06	X0.3
82. Change C835/C836 from 220pF to 0.01U	Following Sigmatel requirement	P31	8/1/06	X0.3
83. Change L27/L28/L29/L30/L31/L32/L33/L34 to L22/L23/L24/L25 co-layout with R818/R819/R820/R821/R822/R823/R824/R825	Follow EMI requirement	P29	8/1/06	X0.3
84. Add unpopulate JP29 on side of NEC controller	For Motion requirement	P27	8/2/06	X0.3
85.Change H18 size from C276D110 to C197D110	For ME change requirement	P38	8/2/06	X0.3
86. Add C74/C75	Following Motion requirement	P28	8/2/06	X0.3
87. Delete R57,R69,C798	Co-layout Trinity and delete co-layout Colorado with STAC9220	P30	8/4/06	X0.3
88. Add U1/C680/C931/C932/R446	Adding buffer to generate V_DDR_MCH_REF to solve SODIM sometime can not boot issue	P9	8/7/06	X0.3
89. Change R81 from 4.87K to 4.75K	Following Marvell requirement to optimize LAN chip usage	P28	8/14/06	X0.3
90. Change C69/C70 from 27pF to 18pF	Following Marvell requirement to optimize LAN chip usage	P28	8/14/06	X0.3
91. Change transformer T21 from GST5009-LF to GST5009-V	Following Marvell requirement to optimize LAN chip usage	P29	8/14/06	X0.3
92. Change U16/U31 power supply from +5VALW to +5VS	Save power in S3 state and reduce speakers output noise	P31	8/14/06	X0.3
93.Add R23/R25/U47/C39/C798/R57/Q62 footprint on board	Reserve for reduce headphone pop noise	P30	8/16/06	X0.3
94. Delete Q61, R685, R668, Q14, D6, D9, D13, R7, R8, R4. Add R924, Q16, R712, R642, R6, Q64, R364, D15, R331, Q66, R317, D19, R330, Q65, R315, D16.	As Motion requirement. Add LED brightness control function.	P17	9/29/06	X0.4
95. Change J2, J3 size, change J6 to Jump type.	Follow factory DFX requirement.	P17	9/29/06	X0.4
96. Add C681, R717, R716. Change JP6.40 from GND to PID1. Add signal PID1 to ICH7.AE20.	Follow Motion requirement. Add one pin to support panel ID.	P17 P22	9/29/06	X0.4
97. Add R718, Q11. Add signal DVI_DETECT# to ICH7. AD21.	Follow Motion requirement. Add DVI plug detect function to ICH.	P18 P22	9/29/06	X0.4
98. Change R34 from un-mounted to mounted. Add U48, R60, R451, Q67, U49.	Follow Motion requirement. Add power saving function for Ricoh controller.	P25	9/29/06	X0.4


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99. Add R826, R452, Q68, U50, R75, U53. Change U27 power supply from +3VS to +3V_NECUSB.	Follow Motion requirement. Add power saving function for NEC controller.	P27	9/29/06	X0.4
100. Delete R287. Add R87, R82, R86, R83, R84, R85.	For debug.	P33	9/29/06	X0.4
101. Add R333, R332. Add signal PCM_CLK_EN#, USB_CLK_EN#, Card_Insert#.	Follow Motion requirement. Add power saving function for NEC controller and Ricoh controller.	P33	9/29/06	X0.4
102. Add location CLIP1	For deal with antenna routing conveniently	P38	10/16/06	X0.4
103. Add R294	FIR part change	P35	10/17/06	X0.4
104. Add U56, C686, C685, C684, C683, R725, R730, R720, R968, C687, Q61, Q69, U57. Add signal G_SENSOR to EC.	Add G-Sensor function	P24	10/17/06	X0.4
105. Swap EC U33 pin35 and pin80	Solve +5V_DOCK turn on/off condition validity	P36	11/01/06	X0.4
106. Delete EC U33 pin62 project_ID net name	No use	P33	11/01/06	X0.4
107. Delete U57,change U33 pin62/pin90 net name	Follow vender review result to change	P24, P33	11/01/06	X0.4
108. Delete EC U33 pin91/pin92 net name	No use	P33	11/01/06	X0.4
109. JP30 pin4 and pin6 pull down to ground	No use	P36	11/01/06	X0.4
110. Buletooth USBP2+/- change into NEC_USBP2+/-; JP28 NEC_USBP2+/- change into USBP2+/-	Swap WWAN and BT, ensure WWAN to be used under DOS mode	P24, P27	11/01/06	X0.4
111. Change U33 pin46 net name from RFOFF# to WLANOFF# Change U33 pin92 net name from WWAN_SW_EN to WWANOFF# Change JP13 net name from RFOFF# to WLANOFF# Change JP28 net name from RFOFF# to WWANOFF#	Separate WLAN and WWAN on/off control signal	P24, P33	11/01/06	X0.4
112. H9 connect to digital ground from analog ground	Antenna pass through H9 area, provide signal being interfere	P38	11/01/06	X0.4
113. Add C416	Delay shutdown ramp up time to solve headphone pop-noise	P30	11/01/06	X0.4
114. Add unpopulate C507	For HSDL-3220 FIR reserve capacitor	P35	11/01/06	X0.4
115. Delete R328,R316, project_ID related table	No use	P33	11/01/06	X0.4
116. R327/R326 populate, R267/r157 unpopulate	Correct BDID configuration	P33	11/01/06	X0.4
117. Add unpopulate R966/C933	Add AC termination for EMI providing	P24	11/01/06	X0.4
118. Change BIOS/B connector from E&T_1009-E40L-00R to ACES_88072-4071_40P	Solving BIOS/B connect stably with MB	P34	11/06/06	X0.4
119. Change USB connector from SUYIN_020173MR004S500ZL to SUYIN_020173MR004S583ZL	Solving USB connector stability when inserting USB device	P32	11/06/06	X0.4
120. JP19, change Pin1 to GNDA; change Pin2 to INTMIC3; change Pin3 to GNDA;	Solve the MIC(3rd) noise issue;	P36	11/08/06	X0.4
121. JP34; Move Pin11 --> Pin9 Move Pin10 --> Pin11 Move Pin9 --> Pin10	Solve the MIC(Mic2) 'click' noise issue;	P31	11/08/06	X0.4
122. Change H26/H27 size form C276D165 to C276D173	Solve the docking CRT signal instability issue	P38	11/14/06	X0.4
123. Add unpopulate R283/R967 and R969	Follow SMSC schematics review	P35	11/14/06	X0.4
124. Change L42/L47 from BLM18AG601SND1 to BK1608HM601-T	Follow IDT AP test feedback result	P31	12/27/06	X0.5
125. Swap EC U33 pin27 and pin30	Solving fan noise, pin30 PWM can not be programming to 30KHz	P33	12/27/06	X0.5
126. Delete R718, delete U9 pinAD21 net to NC the pin , change net PCI_REQ5# into DVI_DETECT#	Solving DVI can be automatically detected by system when inserting	P18, P20,P22	12/28/06	X0.5


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127. Redefine BID	For reviewing	P33	12/28/06	X0.5
128. Add Q70, Q72, R731, R732	Providing ALS/B leak current to +3VS	P36	12/29/06	X0.5
129. Re-assign MB ALS/B connector JP34 pin	Solving the 1st array mic noise issue	P36	12/29/06	X0.5
130. unpopulate Q62/C416, add R88, when use MAX9890, use U33 pin91 control shutdown pin with R88	Reduce HP pop noise	P33,P30	12/29/06	X0.5
131. Change PCIE 0.1u capacitor C631/C632/C629/C630/C661/C670 part number	Solving PCIE capacitor temperature characteristic unstable issue	P22	12/29/06	X0.5
132. Change FIR module U41 to agilent HSDL-3220	Use agilent FIR module to solve FIR tranmsition and receive fail issue	P35	12/29/06	X0.5
133. Change JP30 pin19 GND to GNDA	Solving 2nd array mic noise issue	P36	12/29/06	X0.5
134. Change R965 form 100 to 22K; change C930 from 0.1U to 0.47U and re-connect; change R964 from 100K to 330K; add R970	Solving vibration issue when S3 wake up only battery supply power	P36	12/29/06	X0.5
135. change JP34 pin assignment	Avoid record noise in internal MIC1	P36	01/08/07	X0.5
136. delete signal "Blanco_USB_OC#"	Avoid ESD fail on this pin	P34	01/08/07	X0.5

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