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IM88-0481-02
HARDWARE INSTRUCTION MANUAL
ND812 TELETYPE/AUTO LOADER INTERFACE

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TABLE OF CONTENTS

<u>SECTION</u>	<u>TITLE</u>	<u>PAGE</u>
I	INTRODUCTION	1-1
	1-1. General Description	1-1
	1-3. Specifications	1-1
II	EQUIPMENT PREPARATION	2-1
	2-1. General	2-1
	2-3. Preparation for Use	2-1
	2-4. Unpacking and Inspection	2-1
	2-7. System Installation and Interconnections	2-1
	2-9. Preliminary Check-Out	2-2
III	OPERATING INSTRUCTIONS	3-1
	3-1. General	3-1
	3-3. Control and Indicator Functions	3-1
	3-6. Specific Software Considerations	3-1
	3-8. Operating Procedures	3-3
IV	FUNCTIONAL DESCRIPTION	4-1
	4-1. General	4-1
	4-3. General Information	4-1
	4-8. General Functional Description	4-4
	4-10. Keyboard/Reader Logic	4-4
	4-12. Printer/Punch Logic	4-5
	4-18. Detailed Functional Description	4-7
	4-21. Instruction Decode	4-7
	4-24. Keyboard/Reader Circuitry	4-8
	4-27. Printer/Punch Circuitry	4-9

<u>SECTION</u>	<u>TITLE</u>	<u>PAGE</u>
	4-29. Auto Loader Circuitry	4-9
	4-34. I/O Signal Description.	4-11
V	MAINTENANCE	5-1
	5-1. General	5-1
	5-3. Equipment Required For Maintenance	5-1
	5-5. Preventive Maintenance	5-2
	5-8. Corrective Maintenance	5-2
VI	REPLACEABLE PARTS LIST	6-1
	6-1. General	6-1
VII	DIAGRAMS	7-1
	7-1. General	7-1

LIST OF ILLUSTRATIONS

<u>FIGURE</u>	<u>TITLE</u>	<u>PAGE</u>
2-1	ND812 Teletype/Auto Loader Interconnection Diagram	2-2
4-1	ASCII Format	4-3
4-2	Address Format	4-3
4-3	Keyboard/Reader Block Diagram	4-4
4-4	Teletype Print/Punch Block Diagram	4-5
4-5	Auto Loader Block Diagram	4-6
4-6	ND812 I/O Instruction Format	4-8
4-7	Teletype Keyboard/Reader Timing Diagram (For Letter Z = 332)	4-8
4-8	Teletype Print/Punch Timing Diagram (For Letter Z = 332)	4-9
4-9	Auto Loader Data or Address Timing Diagram	4-10
4-10	Auto Loader ASCII or Field Change Character Timing Diagram	4-11

LIST OF TABLES

<u>TABLE</u>	<u>TITLE</u>	<u>PAGE</u>
1-1	Physical and Electrical Characteristics	1-1
3-1	ND812 Teletype I/O Instructions	3-2
3-2	Memory Field Selections	3-3
3-3	Punched Paper Tape Field Change Character Format	3-4
4-1	ASCII Coded Characters	4-1
4-2	Auto Loader Data Sequence	4-10

<u>TABLE</u>	<u>TITLE</u>	<u>PAGE</u>
4-3	ND812 Teletype/Auto Loader I/O Signals	4-11
5-1	Required Tools and Test Equipment	5-1
6-1	Replaceable Parts List	6-1
7-1	Diagram Index	7-1

SECTION I INTRODUCTION

1-1. GENERAL INFORMATION

1-2. The ND812 Teletype/Auto Loader Interface (88-0481) is designed to drive any standard Teletype Model ASR33 Automatic Send/Receive Set strapped for 20 mA full duplex operation. Serial input from the Teletype is assembled into a parallel eight bit word and transferred to the ND812 Central Processor. Parallel output from the processor is assembled into serial data and punched on paper tape in an eight-level ASCII code.

1-3. Auto Loader Interface is a hardware loader that reads binary formatted paper tape and loads the data into a memory field selected by the processor's front panel Memory Field switches or by the detection of a field change character formatted on the binary tape being read. This convenient feature permits loading programs into the ND812 via teletype without the Software Binary Loader (ND41-0005).

1-4. SPECIFICATIONS

1-5. Complete physical and electrical characteristics including specifications for the ND812 Teletype/Auto Loader Interface are listed in Table 1-1.

Table 1-1. Physical and Electrical Characteristics

Characteristics	Specifications
<u>Electrical Characteristics</u>	
Power Consumption	+5 Vdc at 1A -24 Vdc at 20 mA
<u>Functional Characteristics</u>	
Read-In Speed	10 characters/s
Readout Speed	10 characters/s

Table 1-1. Physical and Electrical Characteristics (Cont'd)

Characteristics	Specifications
Input/Output Format	Serial eight-level ASCII code
Operating Temperature Range	0-50°C (32-122°F)
Operating Humidity Range	15-95%, non-condensing

SECTION II EQUIPMENT PREPARATION

2-1. GENERAL

2-2. This section contains instructions for preparation for use, system installation and interconnection, and preliminary check-out.

2-3. PREPARATION FOR USE

2-4. UNPACKING AND INSPECTION

2-5. If ordered separately, carefully unpack the ND812 Teletype/Auto Loader Interface, saving the shipping cartons for possible re-shipment. Thoroughly inspect the equipment for damage and if damage is apparent, notify either the nearest Nuclear Data sales office or the Nuclear Data home office for prompt adjustment.

2-6. Normal heat generated by this interface will not hamper operation, however, this interface should not be placed over radiators or other devices utilizing vacuum tubes.

2-7. SYSTEM INSTALLATION AND INTERCONNECTIONS

2-8. ND812 Teletype/Auto Loader Interface consists of an ND-TAL-B board and is intended for mounting in the I/O cage of ND812 Central Processor. Refer to Figure 2-1 and perform the following operations:

- a. Remove rear panel from ND812 Central Processor.
- b. Insert ND-TAL-B board into ND812 Central Processor connector W30.
- c. Connect the gray ribbon cable and 16 pin integrated circuit connector originating from ASR33 Teletype to the integrated circuit socket labeled "TTY" (A09) on ND-TAL-B board.

d. Connect ASR33 Teletype line cord to the 117 Vac outlet provided on the rear panel of ND812 Central Processor.

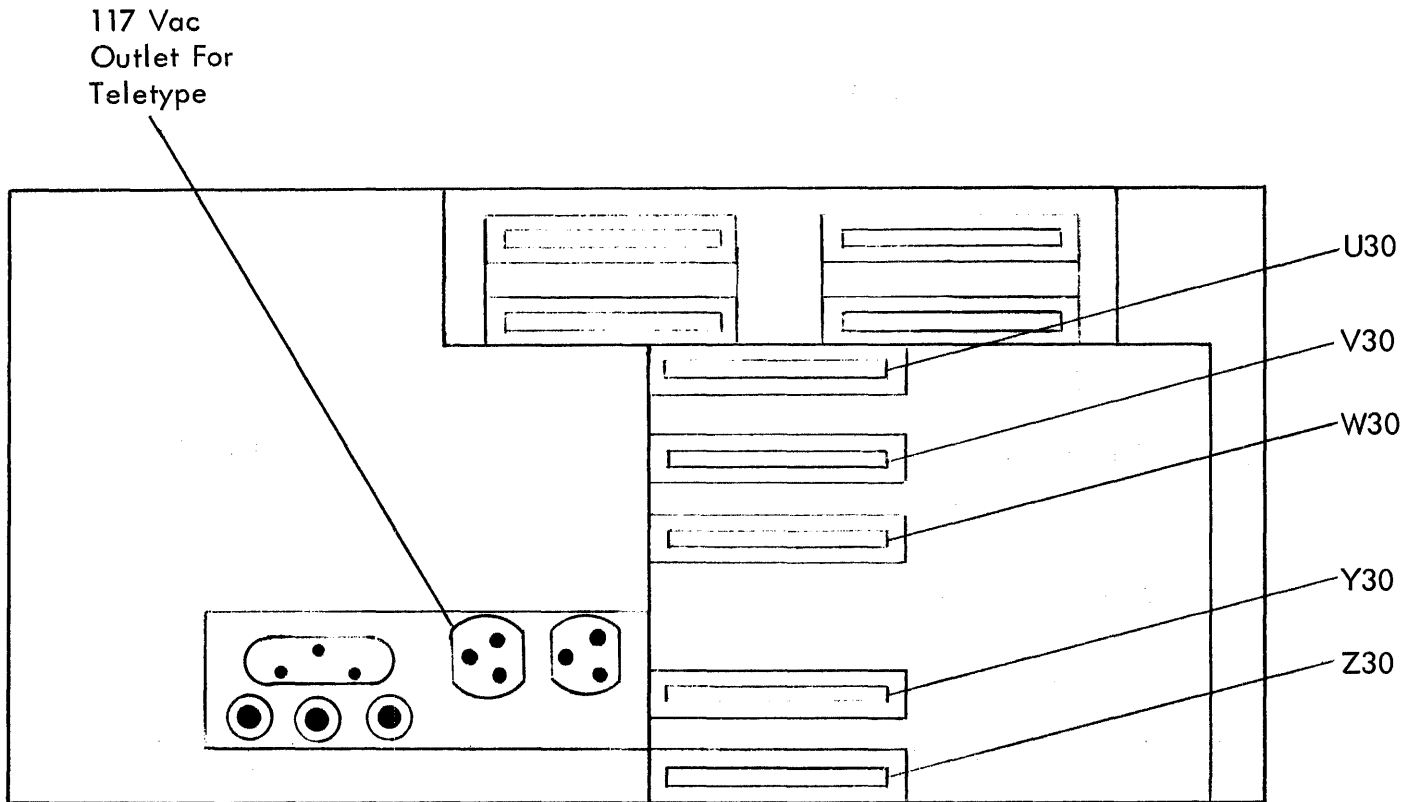


Figure 2-1. ND812 Teletype/Auto Loader Interconnection Diagram

2-9. PRELIMINARY CHECK-OUT

2-10. As a rapid and accurate method of checking ND812 Teletype/Auto Loader Interface operating status, a High/Low Speed Reader Test (ND41-8005) and Low Speed Punch Test (ND41-8006) are available. The reader test reads a sequence of 0 to 255 ramps from a tape loop, and continues to read the loop until an error is detected, or the reader test is manually terminated by depressing the processor STOP switch. The punch test punches a series of 0 to 255 ramps and verifies the punched tape. For a detailed description of these tests refer to the ND812 Diagnostics Software Instruction Manual.

SECTION III OPERATING INSTRUCTIONS

3-1. GENERAL

3-2. This section contains instructions for the ND812 Teletype/Auto Loader. Instructions include control and indicator functions, specific software considerations, and operating procedures.

3-3. CONTROL AND INDICATOR FUNCTIONS

3-4. ND812 Teletype I/O Instructions are utilized to execute a data transfer to/from the Teletype. These instructions must be incorporated within a core resident program to read or punch binary formatted paper tapes via the ASR33 Teletype. When instructed, interface read logic converts the 11 bit train of data from the keyboard or reader to an eight bit ASCII character. The punch logic conversely converts the eight bit ASCII character from the ND812 Central Processor to an 11 bit train of data. At the completion of either a read or punched character, an interrupt request is issued to the ND812 Central Processor.

3-5. The controls necessary to operate the ND812 Auto Loader are located on the ND812 Central Processor front panel. Simplicity and operational ease of the Auto Loader are of primary interest. Once the binary tape is inserted in the Teletype Reader with leader under reader head, momentarily depressing ND812 front panel NEXT WORD and LOAD AR switches initiates the Auto Loader.

3-6. SPECIFIC SOFTWARE CONSIDERATIONS

3-7. Table 3-1 lists all ND812 Teletype I/O Instructions. Instructions include Teletype Keyboard/Reader Instructions and Teletype Printer/Punch Instructions. The first column contains instruction names and the second column contains the associated mnemonic. Column three lists the instruction octal codes and the fourth column describes instruction operation.

Table 3-1. ND812 Teletype I/O Instructions

Instruction Name	Mnemonic	Octal Code	Operation
<u>TELETYPE KEYBOARD/READER INSTRUCTIONS</u>			
Teletype Input Skip	TIS	7404	Skips next logical instruction when keyboard/reader flag is set to "1".
Teletype Input Read	TIR	7402	Clears keyboard/reader flag and loads J register from keyboard/reader buffer.
Teletype Input Fetch	TIF	7401	^{KFLG} Clears keyboard/reader flag and fetches next character from keyboard/reader buffer.
Teletype Read Fetch	TRF	7403	Combines TIR and TIF.
<u>TELETYPE PRINTER/PUNCH INSTRUCTIONS</u>			
Teletype Output Skip	TOS	7414	Skip next logical instruction when printer/punch flag is set to "1".
Teletype Output Punch	TOP	7412	Clears printer/punch flag, loads printer/punch buffer from J register and prints/punches character.
Teletype Output Clear	TOC	7411	Clears printer/punch flag.
Teletype Clear Punch	TCP	7413	Combines TOP and TOC.

3-8. OPERATING INSTRUCTIONS

3-9. AUTO LOADER

3-10. ND812 Teletype Auto Loader reads binary formatted paper tape and loads the program into a selected memory field. Below is a detailed step-by-step paper tape loading procedure.

- a. Depress ND812 STOP key.
- b. Set Teletype START/STOP/FREE switch to FREE. Set Teletype LOCAL/OFF/LINE switch to LINE.
- c. Insert binary tape into Teletype Reader with leader (8th level punch only, 200_g) under the reader head.
- d. Set ND812 MEMORY FIELD switch to desired memory field. Binary tape is loaded into selected memory field. Refer to Table 3-2 for memory field selections.

Table 3-2. Memory Field Selections

Selected Memory Field	ND812 MEMORY FIELD Switches	
	∅∅	∅1
Memory Field ∅∅ (MF∅∅)	∅ (down)	∅ (down)
Memory Field ∅1 (MF∅1)	∅ (down)	1 (up)
Memory Field ∅2 (MF∅2)	1 (up)	∅ (down)
Memory Field ∅3 (MF∅3)	1 (up)	1 (up)

NOTE

If binary tape contains field change characters, set ND812 MEMORY FIELD switches to "∅" down. Field change characters are punched on paper tape in particular format which is depicted by Table 3-3. Paper tape levels three and eight indicate a field change character and levels one and two determine the memory field. Levels four through seven must not be punched.

Table 3-3. Punched Paper Tape Field Change Character Format

Selected Memory Field	Punched Paper Tape Levels*								8-Bit Octal Code
	1	2	3	4	5	6	7	8	
Memory Field 00 (MF00)	0	0	1	0	0	0	0	1	204
Memory Field 01 (MF01)	1	0	1	0	0	0	0	1	205
Memory Field 02 (MF02)	0	1	1	0	0	0	0	1	206
Memory Field 03 (MF03)	1	1	1	0	0	0	0	1	207

*A "1" indicates a punched level, "0" indicates a non-punched level.

- e. Set Teletype START/STOP/FREE switch to START.
- f. Simultaneously depress ND812 LOAD AR and NEXT WORD switches.
- g. The paper tape will be read into memory and stop on trailer (8th level punch only 200g).

NOTE

Any ASCII characters read by the Auto Loader will be echoed (printed). Data punched on paper tape is represented by 0XX (levels 1 through 6) and address information is 1XX (level 7 always punched and 1 through 6 contains address data).

h. Set ND812 SELECT REGISTER switch to J. Read contents of ND812 SELECTED REGISTER indicator lamps. An octal 0000 (all lamps out) indicates a valid load. If any lamps are on, the loading procedure was erroneous. Re-load tape starting from Step a.

3-11. TELETYPE

3-12. Teletype I/O Instructions control all operations performed by the Teletype. Selected instructions will read from the keyboard or reader, punch or print data from the processor, and/or clear the punch or reader flags. Instructions must be core resident before execution and programmed in a logical order.

3-13. Before executing any Teletype I/O Instructions, ascertain that Teletype START/STOP/FREE switch is in START (if tape is to be read), Teletype punch ON switch is depressed (if tape is to be punched), and LOCAL/OFF/LINE switch is in LINE.

SECTION IV FUNCTIONAL DESCRIPTION

4-1. GENERAL

4-2. This section contains theory of operation for the ND812 Teletype/Auto Loader Interface. Theory of operation includes general information, general functional description, and detailed functional description.

4-3. GENERAL INFORMATION

4-4. Table 4-1 lists standard ASCII coded characters and the corresponding eight bit octal code.

Table 4-1. ASCII Coded Characters

ASCII Character	8-Bit Octal Code	ASCII Character	8-Bit Octal Code
A	301	!	241
B	302	"	242
C	303	#	243
D	304	\$	244
E	305	%	245
F	306	&	246
G	307	'	247
H	310	(250
I	311)	251
J	312	*	252
K	313	+	253
L	314	,	254
M	315	-	255
N	316	.	256
O	317	/	257
P	320	:	272

Table 4-1. ASCII Coded Characters (Cont'd)

ASCII Character	8-Bit Octal Code	ASCII Character	8-Bit Octal Code
Q	321	;	273
R	322	<	274
S	323	=	275
T	324	>	276
U	325	?	277
V	326	@	300
W	327	□	333
X	330	\	334
Y	331	⌋	335
Z	332	↑	336
0	260	←	337
1	261	Leader/Trailer	200
2	262	LINE FEED	212
3	263	Carriage RETURN	215
4	264	SPACE	240
5	265	RUBOUT	377
6	266	Blank	000
7	267	BELL	207
8	270	TAB	211
9	271	FORM	214

4-5. Data to/from the Teletype is an ASCII coded 11 bit serial train. Each of the data trains can represent a single ASCII character or a binary number. All ASCII characters have the 8th level set to one, and the 8th level only is used for leader/trailer in binary tapes. Figure 4-1 illustrates the bit assignment and weighting of an ASCII character.

4-6. A start bit is brought low for approximately nine ms to signal the start of a character. The next eight intervals of nine ms are eight levels of the ASCII character. Levels are weighted 1, 2, 4, 10, 20, 40, 100 and 200 for levels 1 through 8 respectively. These eight levels are followed by two intervals during which the data line is high.

4-7. Binary tapes are assembled with the lower 6 bits of two frames as a 12 bit word. If the 7th level of the first frame is high, the assembled 12 bit word is an address and is placed into the program counter and address register (refer to Figure 4-2). If not, the 12 bit words are loaded into memory in successive locations until the next frame containing a 7th level is detected.

ASCII 261

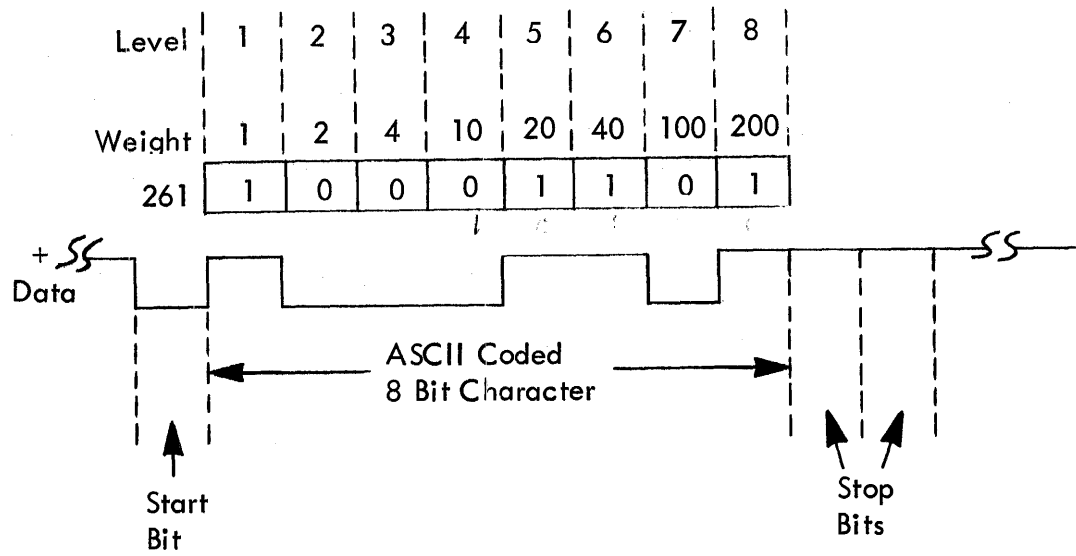


Figure 4-1. ASCII Format

Address 7777₈

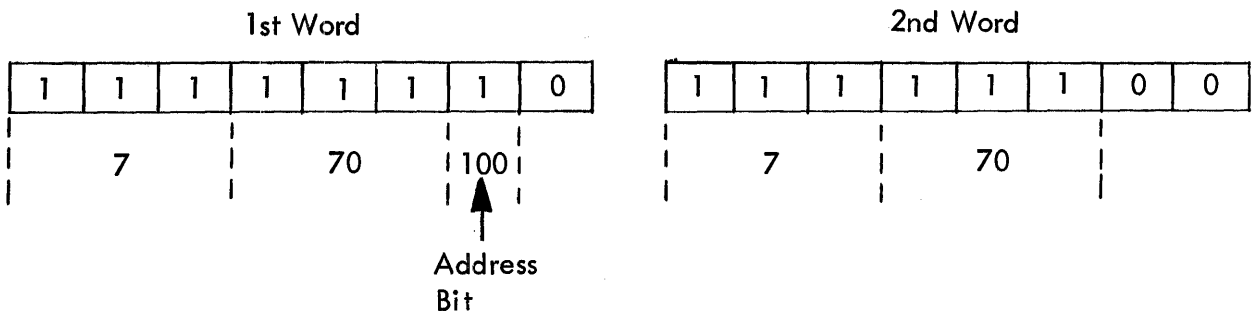


Figure 4-2. Address Format

4-8. GENERAL FUNCTIONAL DESCRIPTION

4-9. This section contains detailed block diagrams of the ND812 Teletype/Auto Loader Interface keyboard/reader logic, printer/punch logic, and auto loader logic.

4-10. KEYBOARD/READER LOGIC (Figure 4-3)

4-11. The 11 bit train of data from the keyboard/reader is converted to an eight bit ASCII character by the 8-bit Shift Register. Data is then transferred to ND812 Central Processor via signals EXT04* through EXT11*. EXT11 corresponds to level one on the paper tape. The normally high line from the Teletype (TTK) drops low for approximately 9 ms, signaling the start of a character. At the end of read character sequence Reader/Keyboard Control Logic sets a bistable (keyboard/reader flag) to a one, indicating the reception of a character by the interface. This flag is sensed or reset by the processor and will cause a trap to location 0001g if the low level interrupt (IONN) is enabled and the flag is set. Each character converted by the interface disables the reader until a "fetch" instruction (TIF) is issued by the ND812 (or auto loader logic). Signal RDRDR* advances Teletype read relay to next character.

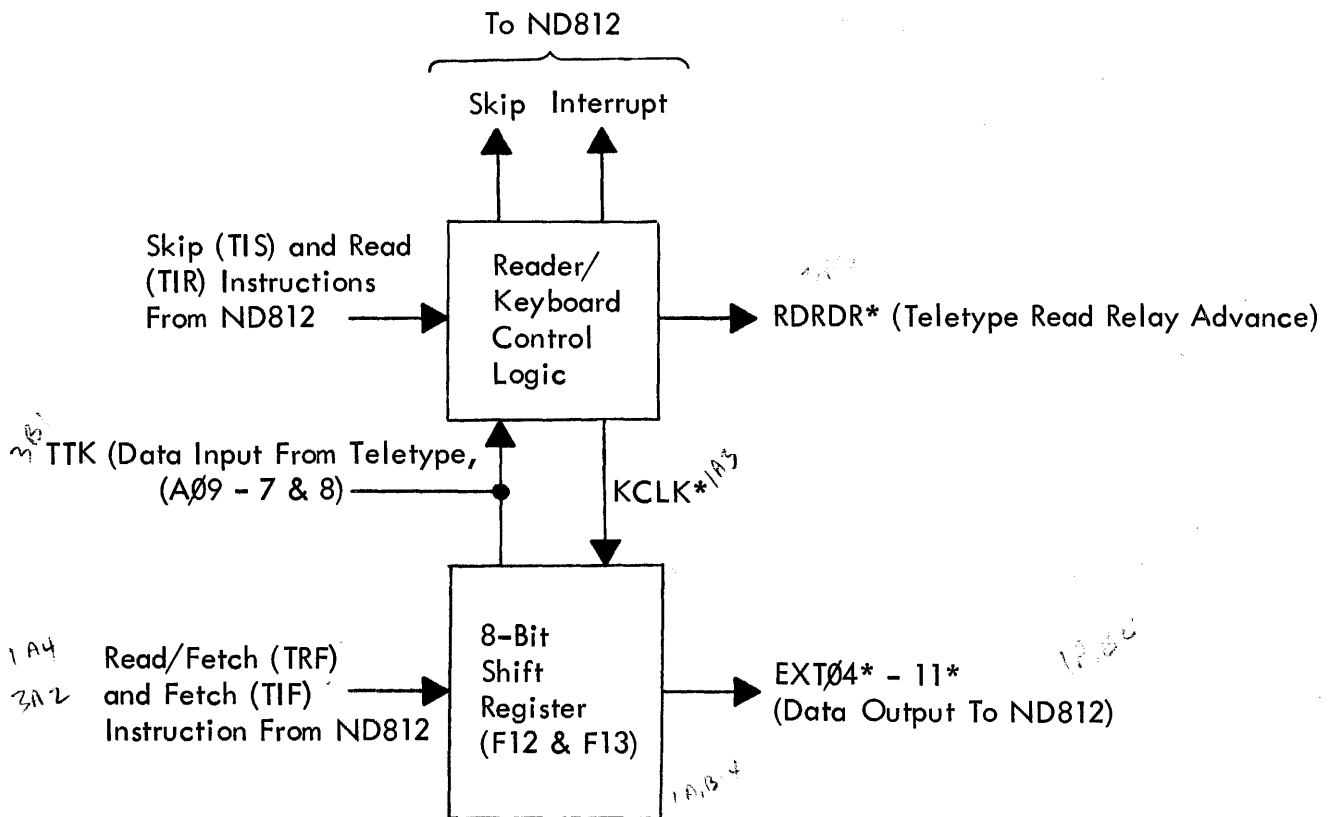


Figure 4-3. Teletype Keyboard/Reader Block Diagram

4-12. PRINTER/PUNCH LOGIC (Figure 4-4)

4-13. The 12-Bit Shift Register converts an eight bit ASCII character originating from the ND812 J Register into an 11 bit train of data. Input data is transferred from the ND812 to the interface via signals OUT04* through OUT11*. OUT11 corresponds to level one on the paper tape. On receipt of a TOP or TCP Instruction, the normally low drive lines to the Teletype (TTYDR*) goes high for approximately 9 ms, signaling the start of a character. At the end of the punch character sequence Print/Punch Control Logic sets a bistable (printer/punch flag) to a one, indicating that a character has been printed/punched. This flag is sensed or reset by the processor and will cause a trap to location 0001_g if the low level interrupt (IONN) is enabled and the flag is set.

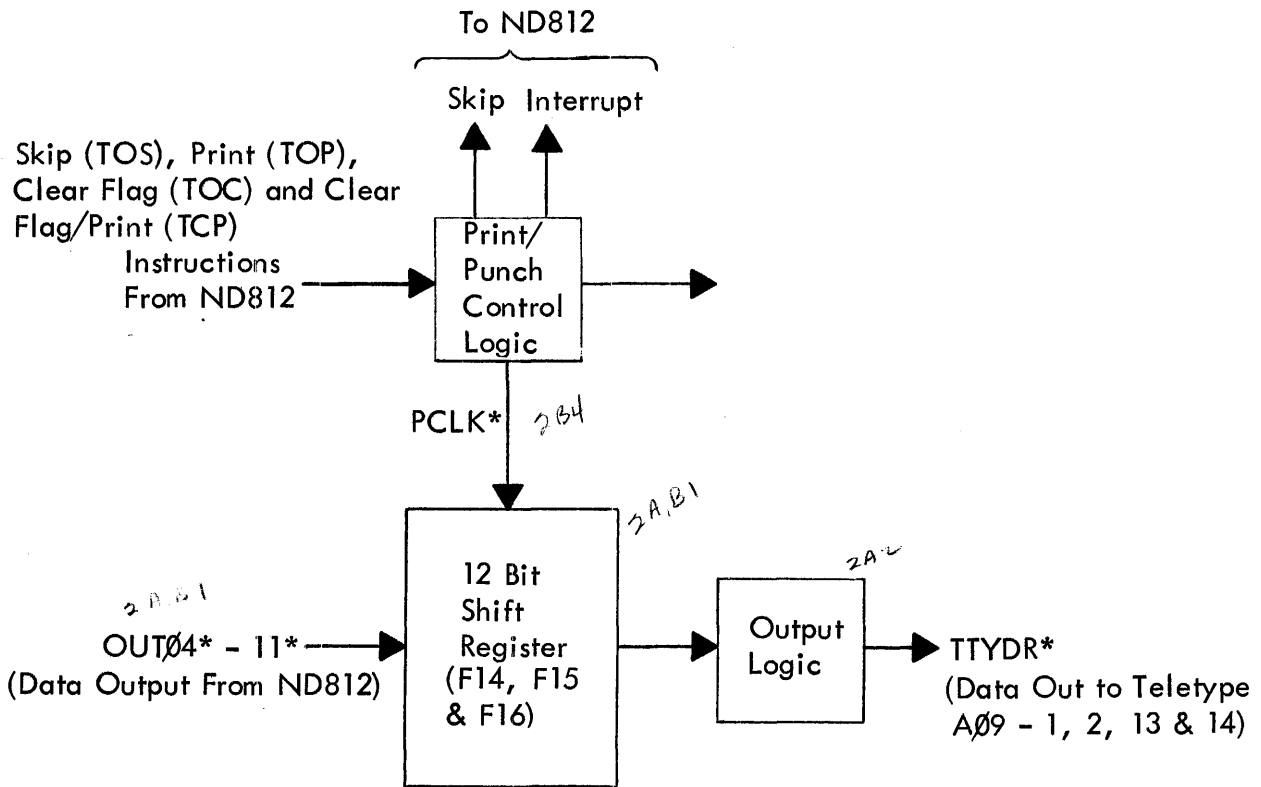


Figure 4-4. Teletype Print/Punch Block Diagram

4-14. AUTO LOADER LOGIC (Figure 4-5)

4-15. ND812 Auto loader reads binary formatted paper tape from and loads the Teletype Reader data into the memory field selected by ND812 front panel MEMORY FIELD switches or field characters present on the binary tape being loaded. ASCII characters punched on the paper tape will be printed by Teletype and will not be loaded into the ND812 Memory.

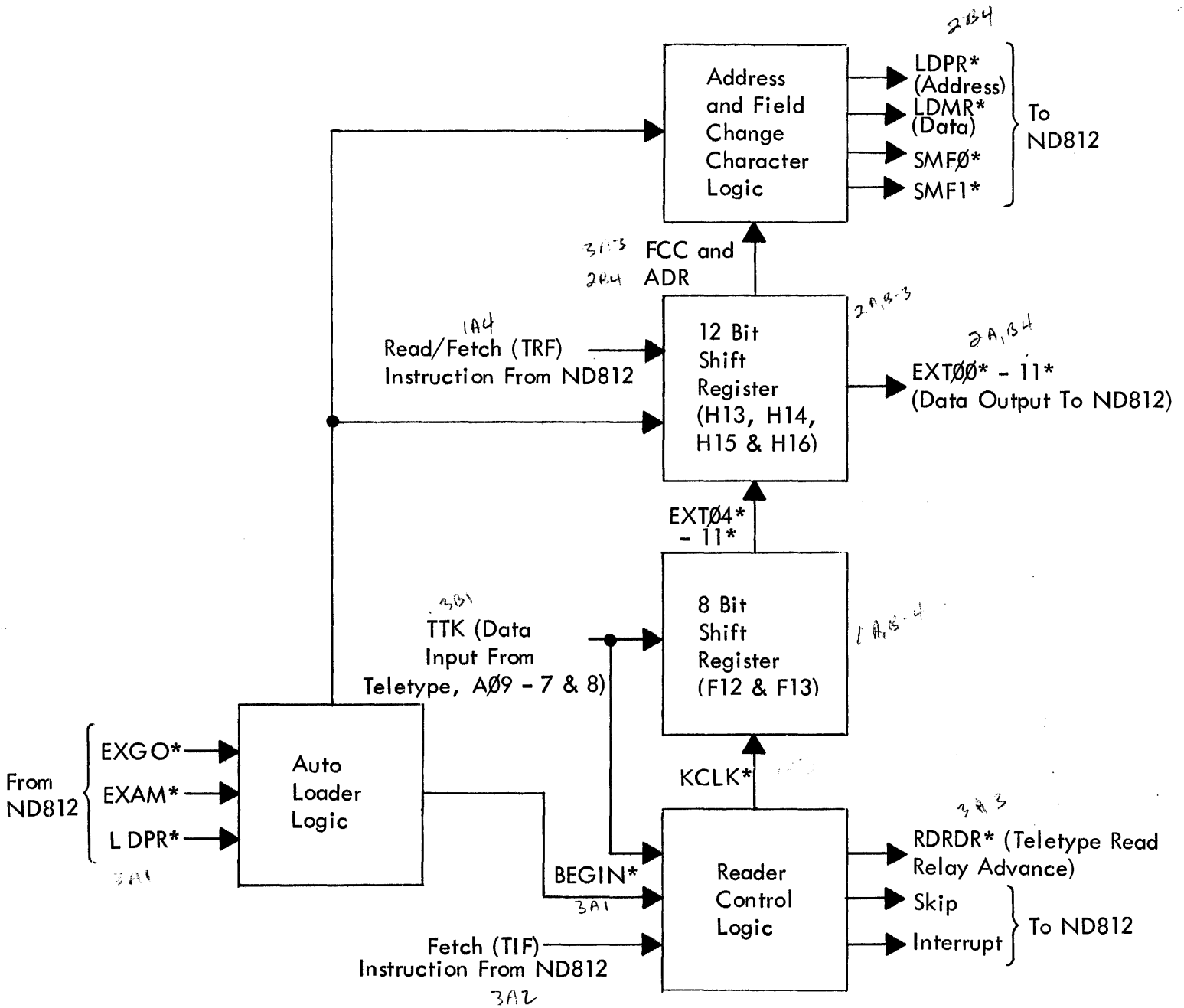


Figure 4-5. Auto Loader Block Diagram

4-16. The 8-Bit Shift Register assembles Teletype input data (TTK) into a 6-bit word then transfers the data into the 12-Bit Shift Register.

4-17. Logic assembles the lower 6 bits of each pair of frames from the Teletype into a 12 bit word, and if the 7th level of the first frame is a one, address and Field Change character logic places the output data (EXT00*-11*) into the Program Counter and Address Registers via signal LDPR*. If the 7th level of the first frame is zero, the 12 bit word is loaded into memory in successive locations (via LDMR*) until the next frame containing a 7th level is read. Field Change characters are also identified and transferred to ND812 via SMF0* and SMF1*. The J register is cleared during initial leader and each assembled 12 bit word is added to it throughout the loading process. The last pair of frames on the binary tape before the trailing 8 levels contains the check sum accompanied by a 7 level in the first frame of the two. This 12 bit number is the negated sum of all the 12 bit words added to the J register. Reader Control Logic provides skip and interrupt request outputs, advances the Teletype read relay, and clocks the 8-bit Shift Register. Auto Loader Logic decodes signals EXGO*, EXAM*, and LDPR* and initializes an auto load operation.

4-18. DETAILED FUNCTIONAL DESCRIPTION

4-19. This section is an expansion of the General Functional Description and includes descriptions of instruction decode circuitry, keyboard/reader circuitry, printer/punch circuitry, auto loader circuitry, and I/O signals.

4-20. Nuclear Data's system diagrams provide a convenient method for locating component and signal references. Each logic sheet is divided into four horizontal coordinates (1,2,3 and 4) and two vertical coordinates (A and B). Also every sheet is numbered, sheet 1 of XX, sheet 2 of XX, etc. The following detailed functional description utilizes parenthetical expressions following signal names for reference to location coordinates of that signal on a specific logic diagram in section VII. Reference to a specific circuit or signal is accomplished by locating the sheet number and coordinates. As an example, STCLR* (1B2) refers to sheet 1, vertical coordinate B, and horizontal coordinate 2.

4-21. INSTRUCTION DECODE

4-22. Signals IOM00* through IOM08* and PCP1* through PCP3* (1A1 and 1B1) originate in the ND812 Central Processor and are decoded by the instruction decoding circuitry initializing the associated operation. The eight Teletype I/O Instructions are described in Table 3-1.

4-23. Figure 4-6 illustrates ND812 I/O instruction format and associated bit weight assignments. For example, a TIF (7401) is represented by IOM00*, IOM01*, IOM02*, IOM03* and PCP3* being 0 Vdc (3A2) and the remaining signals being +5 Vdc.

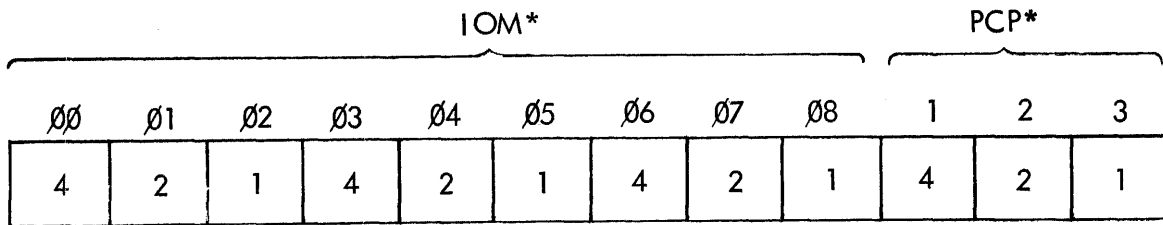


Figure 4-6. ND812 I/O Instruction Format

4-24. KEYBOARD/READER CIRCUITRY

4-25. A 7403 instruction issued by the processor is decoded to initiate a keyboard read/fetch cycle. Two signals control the output character from the Teletype; ACTIV* when low indicates that the keyboard/reader is active, and RDRDR* which is the reader relay advance signal. Referring to Figure 4-7, signal TIF* (fetch) goes low initiating a keyboard reader cycle. Signal TTI is the output data line from the Teletype and is presented to the interface after signal TIF* goes low. Signal ACTIV is brought high on detection of the first TTI and enables the keyboard/reader clock (1A2) via signal CLKEN. The keyboard/reader clock runs at a 110 Hz rate and is derived from a 28.16 kHz oscillator (EØ9 and B14, 3B2). Signal OSC* is the 28.16 kHz rate which is then divided by circuit F1Ø (1B2) providing a 1.76 kHz master clock (MCLK*). The free running master clock is then applied to another divider circuit (F11, 1A2) and the clock enable flip-flop (C13, 1A2). When signal ACTIV is brought high, the next MCLK* pulse causes signal CLKEN to go high presetting the keyboard/reader clock circuit to eight (half of normal divider) and enabling signal KCLK*. The first clock pulse is a short start pulse (due to preset of eight) followed by eight normal 9.09 ms clocks (KCLK) that shift the data into the eight bit shift register (F12 and F13, 1A4).

4-26. Detection of the last (eighth) data bit resets ACTIV which disables the clock (CLKEN high). The keyboard flag (KFLG) is then set by signal KB11* (1A4). When the ND812 Central Processor issues a TRF instruction, data is presented to the processor via signals EXTØ4* through 11*, and the keyboard flag is reset indicating that the interface is ready for the next character.

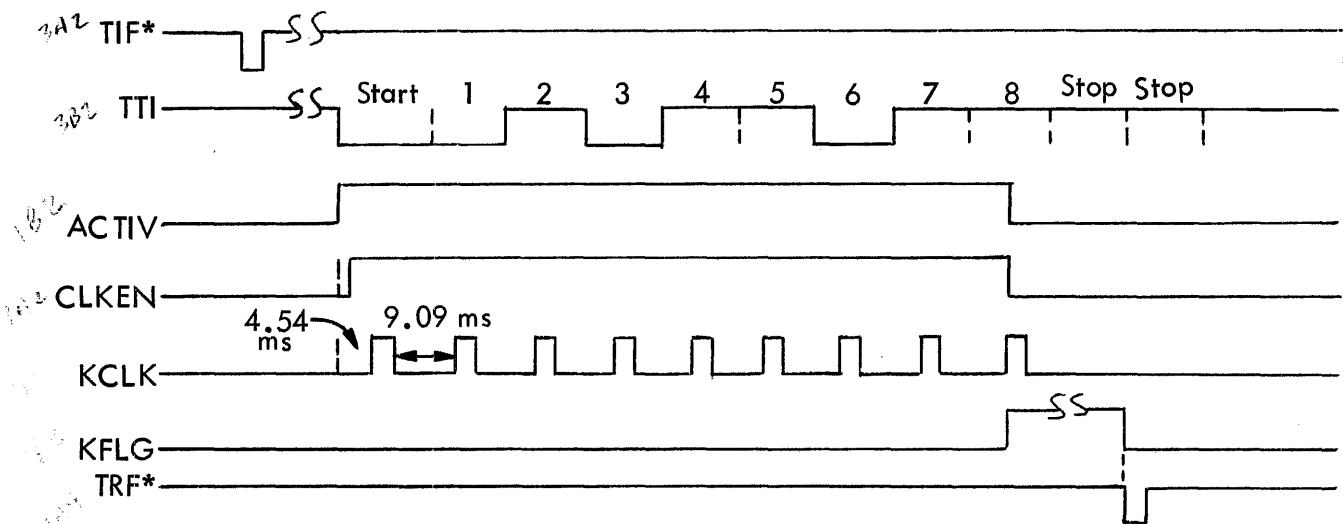


Figure 4-7. Teletype Keyboard/Reader Timing Diagram (For Letter Z = 332)

4-27. PRINTER/PUNCH CIRCUITRY

4-28. A 7413 instruction issued by the processor is decoded to initiate a clear flag, print/punch cycle. Referring to Figure 4-8, signal TCP resets the print/punch flag, enables the print/punch clock (PCLK), and sets the PRUN flip-flop. The print/punch clock runs at a 110 Hz rate and is derived from a 28.16 kHz oscillator (E09 and B14, 3B2). Signal OSC* is the 28.16 kHz rate which is then divided by circuit F10 (1B2) providing a 1.76 kHz master clock (MCLK*). The free running master clock is then applied to another divider circuit (H11 - 2B3) and is enabled by a 7412 instruction providing the print/punch clock (PCLK). The first TTYDR pulse is a start pulse followed by the 8 level ASCII coded word. Data is obtained from the processor via signals OUT04* through OUT11* and serially shifted to the teletype with signal PCLK. Detection of the first stop bit (10th PCLK) causes the EOC signal (end of character) to go high. The next PCLK pulse (11th) resets the punch flag and punch run flip-flops ending the print/punch cycle. Output data is then printed/punched and the interface is ready for the next character.

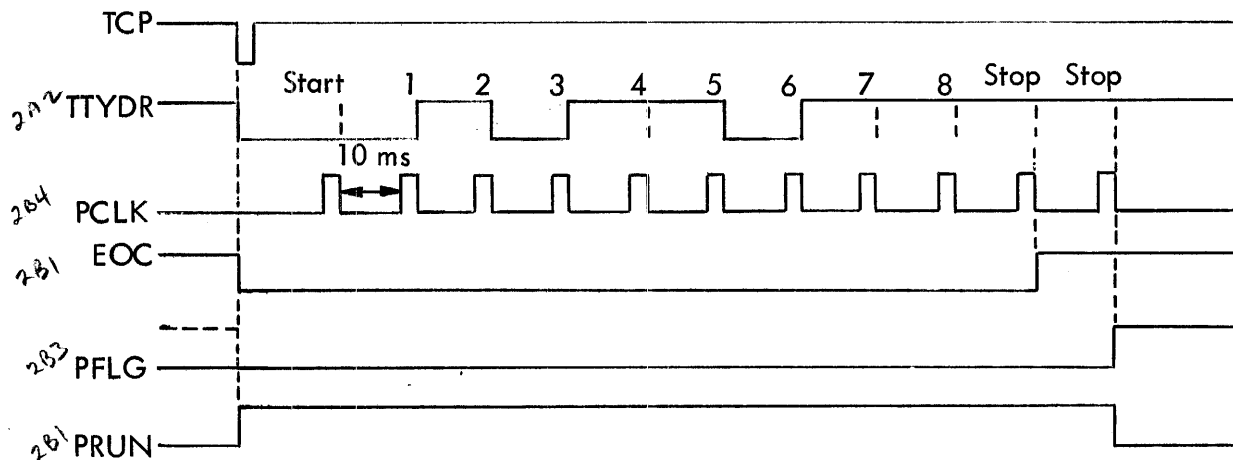


Figure 4-8. Teletype Print/Punch Timing Diagram (For Letter Z = 332)

4-29. AUTO LOADER CIRCUITRY

4-30. Binary formatted data is loaded into memory with the auto loader. An ASCII character is indicated when the tape is not at leader (LEADR* high), an 8th level punch is present on tape (EXT04 high), and it is not a field change character (FCC* high).

4-31. Figure 4-9 illustrates major signal timing for a single 12 bit data word (2 tape frames) loaded into memory. Signals EXAM* and LDPR* (low), and GO (high) (3A1) will set the auto load bistable (C11, 3A2) causing AUTO to go high initiating the auto loader.

Signal BEGIN* (3A1) is also generated which clears the keyboard flag (KFLG) (1B3) via signal TIF* (clear keyboard and advance reader). State zero (ST0) of the five state auto loader process is initiated and will stay high when KFLG is high. ST1 is a fetch character state generated when KFLG is high which reads/fetches a character (TRF*) from the teletype. The most significant six bits of 12-bit data word is loaded into the 12 bit shift register (H13, H14, H15 - 2A3) by TRF* and ST2 is initialized. ST2 will remain high until the keyboard flag is raised again. At this time another TRF* is generated and the least significant 6 bits are loaded into the 12 bit shift register. Upon completion of ST3, signal ST4 is generated loading the 12-bit data word into the ND812 Central Processor via EXT00* through EXT11*. In summary, Table 4-2 lists the sequence followed for every data loading procedure.

Table 4-2. Auto Loader Data Sequence

Signal	Action
BEGIN*	Clear reader flag.
ST0	Wait for reader flag.
ST1	Fetch half-character (6-bits).
ST2	Wait for reader flag.
ST3	Fetch half-character (6 bits).
ST4	Load word into ND812.

4-32. Signals LDPR* LDMR* distinguish data from address information by monitoring EXT05* and EXT04*. If an origin (7th level punch) is detected, the 12 bit word contains addressing information and is loaded into the program and address registers.

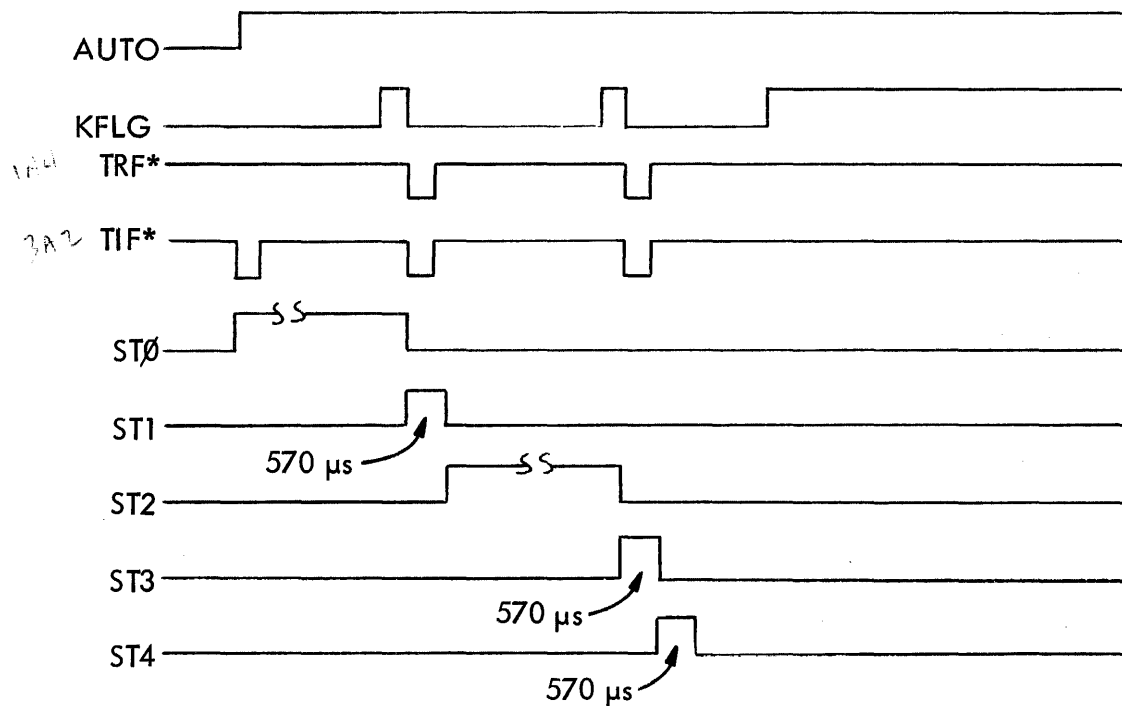


Figure 4-9. Auto Loader Data or Address Timing Diagram

4-33. Auto loader sequence for ASCII characters or field change character differs from data. Figure 4-10 illustrates this difference. Detection of an eighth level punch (EXT04 high) indicates a ASCII or field change character and causes the auto loader sequence to terminate after ST1 and return to ST0.

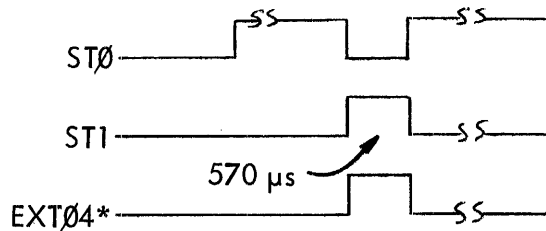


Figure 4-10. Auto Loader ASCII or Field Change Character Timing Diagram

4-34. I/O SIGNAL DESCRIPTION

4-35. Table 4-3 lists the ND812 Teletype/Auto Loader integrated circuit connector A09 I/O signals. The first column lists signal name, second lists A09 pin connection, and the third column describes the signal.

Table 4-3. ND812 Teletype/Auto Loader I/O Signals

Signal	A09 Pin	Description
TTYDR*	1	Teletype Drive
TTYDR*	2	These signals are the serial 11 bit ASCII coded output from ND812 Central Processor.
TTYDR*	13	
TTYDR*	14	
P5V05	3 4 11 12	
RDRDR*	5	Read Relay Drive
RDRDR*	6	
	9	
	10	
TTK*	7	Keyboard Signal Input
	8	
TTK*		These signals are the serial 11 bit ASCII coded input from the ASR33 Teletype.

Table 4-3. ND812 Teletype/Auto Loader I/O Signals (Cont'd)

Signal	AØ9 Pin	Description
	15 16	Not used.

SECTION V MAINTENANCE

5-1. GENERAL

5-2. This section contains instructions required to maintain ND812 Teletype/Auto Loader Interface. Instructions include preventive maintenance and corrective maintenance. Preventive maintenance includes periodic inspection of the equipment. Corrective maintenance includes alignment and adjustment, and test procedures.

5-3. EQUIPMENT REQUIRED FOR MAINTENANCE

5-4. Table 5-1 provides a list of tools and test equipment required for maintenance.

Table 5-1. Required Tools and Test Equipment

Nomenclature	Manufacturer's Model or Part No.	Manufacturer
Digital Voltmeter	3440B	Hewlett Packard*
Multimeter	630-A	Triplet*
Oscilloscope	454	Tektronics*
Standard Technicians Tool Kit	— —	— —
NIM Bin Power Extender Dable (42-pin)	75-0189	Nuclear Data
Module Card Edge Extender Card (62-pin)	75-0219	Nuclear Data
I/O Cage Extender Cable (86-pin)	75-9202	Nuclear Data

* Or Equivalent

5-5. PREVENTIVE MAINTENANCE

5-6. PERIODIC INSPECTION

5-7. Periodic inspection of the equipment is necessary to detect potential trouble before a malfunction occurs. Items such as condition of connectors and cables, proper operation of controls and indicators, and cleanliness of equipment, should be monitored and corrected as required prior to each use.

5-8. CORRECTIVE MAINTENANCE

5-9. ALIGNMENT AND ADJUSTMENT

5-10. This interface does not require alignment or adjustment.

5-11. TEST PROCEDURES

5-12. Either the High/Low Speed Reader Test (ND41-8005) or the Low Speed Reader Test (ND41-8006) can be run to test the operational status of ND812 Teletype/Auto Loader Interface. Refer to ND812 Diagnostic Software Instruction Manual for a detailed description of these tests.

SECTION VI REPLACEABLE PARTS LIST

6-1. GENERAL

6-2. Table 6-1 provides a non-illustrated list of replaceable parts for ND812 Teletype/ Auto Loader Interface. The first column lists the manufacturer part number in numerical order, and the second column provides an abbreviated part description.

Table 6-1. Replaceable Parts List

Part Number	Description
21-0024	RES MG QW 5% 51 OHM
21-0041	RES MG QW 5% 270 OHM
21-0071	RES MG QW 5% 4.7K
21-0079	RES MG QW 5% 10K
26-1037	CAP MY 250WV .1MFD
26-4005	CAP CR 150WV .01MFD
31-0005	DO ZR 1N 4734A
35-0006	DTL-944 DIP 14 G
35-0008	DTL-946 DIP 14 G
35-0017	DTL-936 DIP 14 HXVT
35-0034	IC MC858P DIP 14 G
35-0039	TTL 9300 DIP 16 SFTR
35-0053	IC SN747N DIP 14 FF
35-0059	IC9003 DIP 16 SFTR
35-0063	IC 9007 DIP 14 G
35-0066	IC 9016 DIP 14 HXVT
35-0083	IC MSI 9316 DIP CTR
35-0149	IC SN7413 DIP 14 TRG
70-1895	COMPLETE ND-TAL-B BOARD

SECTION VII DIAGRAMS

7-1. GENERAL

7-2. This section contains schematic diagrams and logic diagrams to be used for troubleshooting equipment covered by this publication. Table 7-1 provides an index for diagrams contained in this section.

Table 7-1. Diagram Index

Figure No.	Description	Page No.
7-1	Logic Diagram General Notes	7-2
7-2	ND812 Teletype/Auto Loader Interface ND-TAL-B Logic Diagram (Sheet 1 of 5)	7-3/7-4
7-2	ND812 Teletype/Auto Loader Interface ND-TAL-B Logic Diagram (Sheet 2 of 5)	7-5/7-6
7-2	ND812 Teletype/Auto Loader Interface ND-TAL-B Logic Diagram (Sheet 3 of 5)	7-7/7-8
7-2	ND812 Teletype/Auto Loader Interface ND-REL-A Logic Diagram (Sheet 4 of 5)	7-9/7-10
7-2	ND812 Teletype/Auto Loader Interface Loading Diagram (Sheet 5 of 5)	7-11/7-12

NOTES:

- 1 - ALL DIODES ARE G964 OR EQUIVALENT, EXCEPT AS NOTED.
- 2 - ALL RESISTORS ARE 1/4W, ±5%, EXCEPT AS NOTED.
- 3 - ALL CAPACITORS ARE pf, EXCEPT AS NOTED.
- 4 - I.C. VOLTAGES, EXCEPT AS NOTED:
 - 14 PIN DIP, PIN (7) GND: PIN (14) +5V
 - 16 PIN DIP, PIN (8) GND: PIN (16) +5V
 - 24 PIN DIP, PIN (12) GND: PIN (24) +5V
- 5 - THE FOLLOWING SYMBOLS/NOTATIONS ARE USED ON THE DIAGRAM AND/OR PRINTED CIRCUIT BOARD ASSEMBLY.

IC - INTEGRATED CIRCUIT

Q - TRANSISTOR

() - IC PIN DESIGNATION

→ - CONNECTOR DESIGNATION

NC - NO CONNECTION

SAT - SELECT AT TEST

(P1) - PRECISION RESISTORS 100PPM
1/8W, ±1% METAL FILM

⊕ - DC COMMON

FB - FERRITE BEAD

↯ - GERMANIUM DIODE

▷ - SILICON DIODE

⊕ - ZENER DIODE

▷ - TUNNEL DIODE

⊕ - SELENIUM DIODE

7-2

ADC* — SIGNAL NAME

[4A2] — SIGNAL SOURCE DRAWING LOCATION, OR

(4A2) — SIGNAL LOAD DRAWING LOCATION

┌ ZONE LOCATION
└ SHEET NUMBER

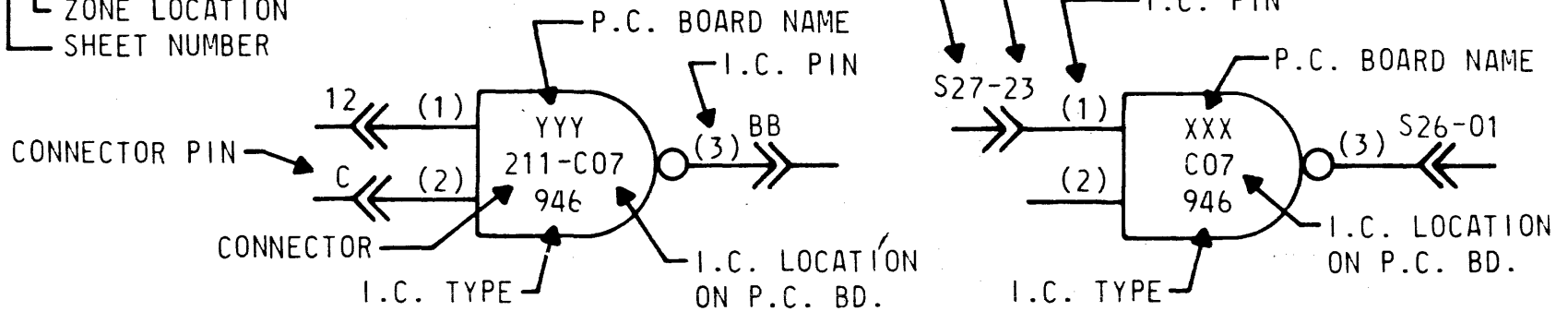


Figure 7-1. Logic Diagram General Notes

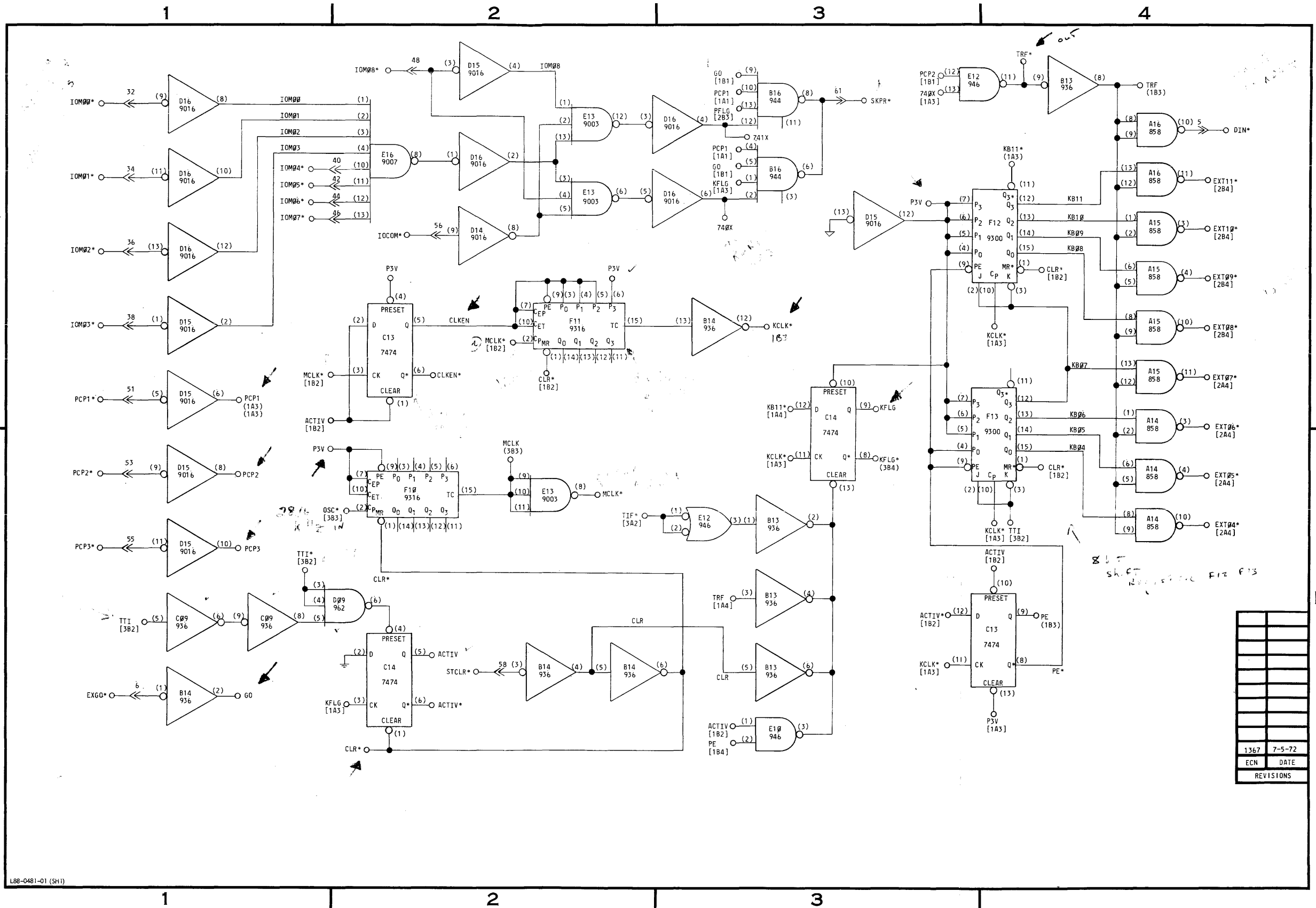


Figure 7-2. ND812 Teletype/Auto Loader Interface ND-TAL-B Logic Diagram (Sheet 1 of 5)

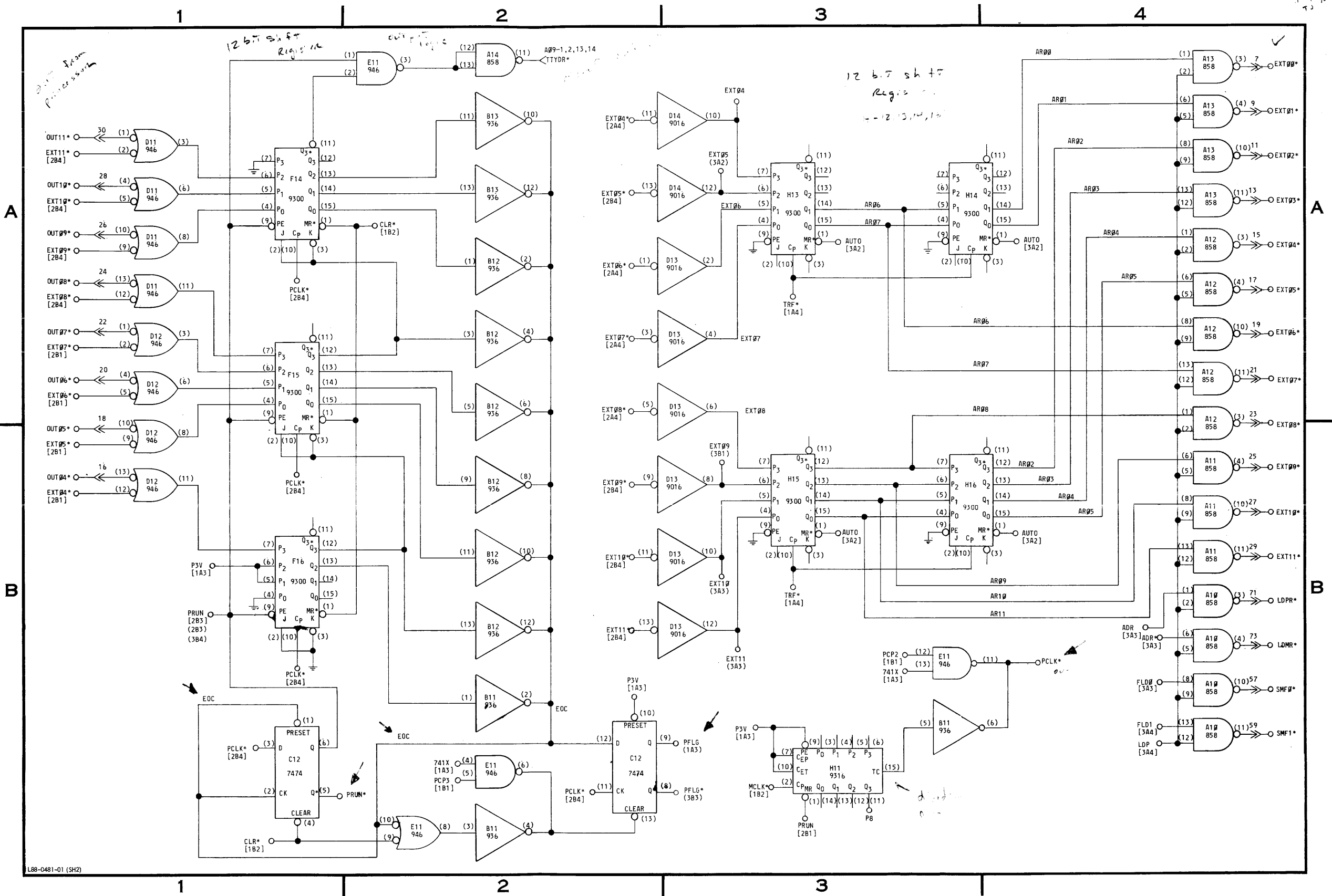


Figure 7-2. ND812 Teletype/Auto Loader Interface ND-TAL-B Logic Diagram (Sheet 2 of 5)

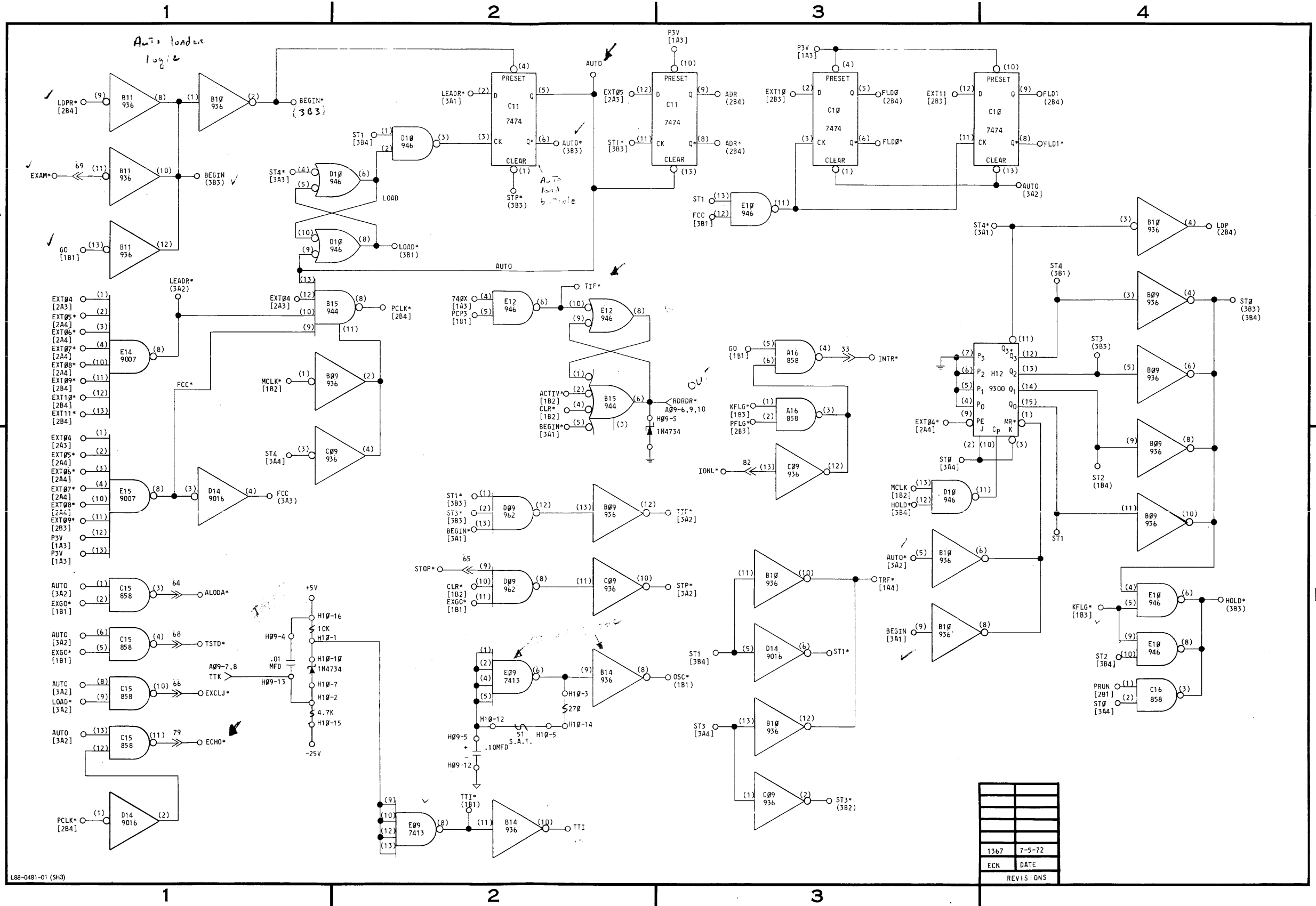


Figure 7-2. ND812 Teletype/Auto Loader Interface ND-TAL-B Logic Diagram (Sheet 3 of 5)

1

2

3

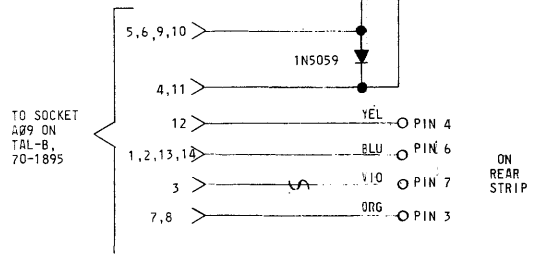
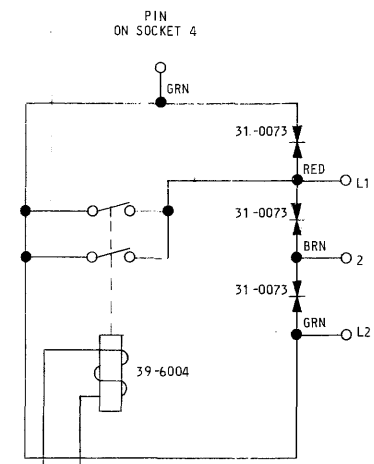
4

REFERENCE TABLE

INTERNAL SIGNALS		EXTERNAL SIGNALS					
SIGNAL	LOCATION	SIGNAL	LOCATION	SIGNAL	LOCATION	SIGNAL	LOCATION
ACTIV	[1B2] (1A1) (1B3) (1B4)	ALTER*	[T18-41]	IOM07*	[1A1]	START*	[T18-63]
ACTIV*	[1B2] (1B3) (3A2)	ARMX*	[T18-76]	IOM08*	[2A2]	STCLR*	[1B2]
	[3A2] (3B1) (3B1) (3B1) (3B1) (2A3) (2A4) (2B3) (2B4) (3A4)	CSMRZ	[T18-45]	IOM09*	[T18-50]	STOP*	[3B2]
BEGIN*	[3A1] (3A2) (3B2)	CSP*	[T18-39]	IOM10*	[T18-52]	TSTD*	[3B1]
CLR*	[1B2] (1A2) (1A4) (1B4) (2A2) (3B2) (3A2)	CSR*	[T18-37]	IOM11*	[T18-54]		
EXT04*	[2A3] (3A1) (3B1) (3A1)	DIN*	[1A4]	IONA*	[T18-78]		
GO	[1B1] (1A3) (1A3) (3A1) (3A3)	ECHO*	[3B1]	IONB*	[T18-80]		
	[1A3] (1B3) (1B3) (1A4) (1B4)	EXAM*	[3A1]	IONL*	[T18-82]		
KFLG	[1A3] (1B1) (1A3)	EXCLJ*	[3B1]	LDMR*	[2B4]		
MCLK*	[1B3] (1A2) (1A1) (2B3) (3A1)	EXG0*	[1B1] (3B1) (3B1) (3B2)	LDPR*	[2B4] (3A1)		
	[2B4] (2A1) (2B1) (2B1) (2B1) (2B2) (3A2) (3B1)	EXTK*	[T18-31]	MRDY*	[T18-47]		
PCP2	[1B1] (1A3) (2B3)	EXT00*	[2A4]	MXS0*	[T18-70]		
PCP3	[1B1] (2B2) (3A2)	EXT01*	[2A4]	MXS1*	[T18-72]		
		EXT02*	[2A4]	MXS2*	[T18-74]		
		EXT03*	[2A4]	OUT00*	[T18-8]		
		EXT04*	[2A4] (2B1) (2A2) (1B4) (3B3)	OUT01*	[T18-10]		
ST1	[3B4] (3B3) (3A2) (3A3)	EXT05*	[2A4] (2A2) (2B1) (1B4) (3A1) (3B1)	OUT02*	[T18-12]		
TIF*	[3A2] (1B2) (3B3)	EXT06*	[2A4] (2A2) (2A1) (1A4) (3A1) (3B1)	OUT03*	[T18-14]		
TRF*	[1A4] (2A3) (2B3) (3B3)	EXT07*	[2A4] (2A2) (2A1) (1A4) (3A1) (3B1)	OUT04*	[2B1]		
TTI	[3B2] (1B1) (1B4)	EXT08*	[2A4] (2A2) (2A1) (1A4) (3A1) (3B1)	OUT06*	[2A1]		
740X	[1A3] (3A2) (1A3)	EXT09*	[2B4] (2B2) (2A1) (1A4) (3A1)	OUT07*	[2A1]		
741X	[1A3] (2B2) (2B3)	EXT10*	[2B4] (2B3) (2A1) (1A4) (3A1)	OUT08*	[2A1]		
		EXT11*	[2B4] (2B3) (2A1) (1A4) (3A1)	OUT09*	[2A1]		
		INTP*	[T18-35]	OUT10*	[2A1]		
		INTR*	[3A3]	OUT11*	[2A1]		
		IOCOM*	[1A2]	PCPST*	[T18-62]		
		IOM00*	[1A1]	PCP0*	[T18-49]		
		IOM01*	[1A1]	PCP1*	[1A1]		
		IOM02*	[1A1]	PCP2*	[2B2]		
		IOM03*	[1A1]	PCP3*	[2B2]		
		IOM04*	[1A1]	SDCS*	[T18-43]		
		IOM05*	[1A1]	SI*S	[T18-75]		
		IOM06*	[1A1]	SKPR*	[1A3]		
				SMF0*	[2B4]		
				SMF1*	[2B4]		

CONNECTOR T18			
PIN	SIGNAL	PIN	SIGNAL
1	GND	2	GND
3	+5V	4	+5V
5	DIN*	6	EXG0*
7	EXT00*	8	
9	EXT01*	10	
11	EXT02*	12	
13	EXT03*	14	
15	EXT04*	16	OUT04*
17	EXT05*	18	OUT05*
19	EXT06*	20	OUT06*
21	EXT07*	22	OUT07*
23	EXT08*	24	OUT08*
25	EXT09*	26	OUT09*
27	EXT10*	28	OUT10*
29	EXT11*	30	OUT11*
31		32	IOM00*
33	INTR*	34	IOM01*
35		36	IOM02*
37		38	IOM03*
39		40	IOM04*
41		42	IOM05*
43		44	IOM06*
45		46	IOM07*
47		48	IOM08*
49		50	
51	PCP1*	52	
53	PCP2*	54	
55	PCP3*	56	IOCOM*
57	SMF0*	58	STCLR*
59	SMF1*	60	-25V
61	SKPR*	62	
63		64	ALODA*
65	STOP*	66	EXCLJ*
67		68	TSTD*
69	EXAM*	70	
71	LDPR*	72	
73	LDMR*	74	
75		76	
77		78	
79	ECHO*	80	
81		82	IONL*
83	+5V	84	+5V
85	GND	86	GND

CONNECTOR A09			
PIN	SIGNAL	PIN	SIGNAL
1	TTYDR*	14	TTYDR*
2	TTYDR*	15	TTYDR*
3	+5V	12	+5V
4	IC042	11	+5V
5	IC043	10	RDRDR*
6	RDRDR*	9	RDRDR*
7	TTK	8	TTK



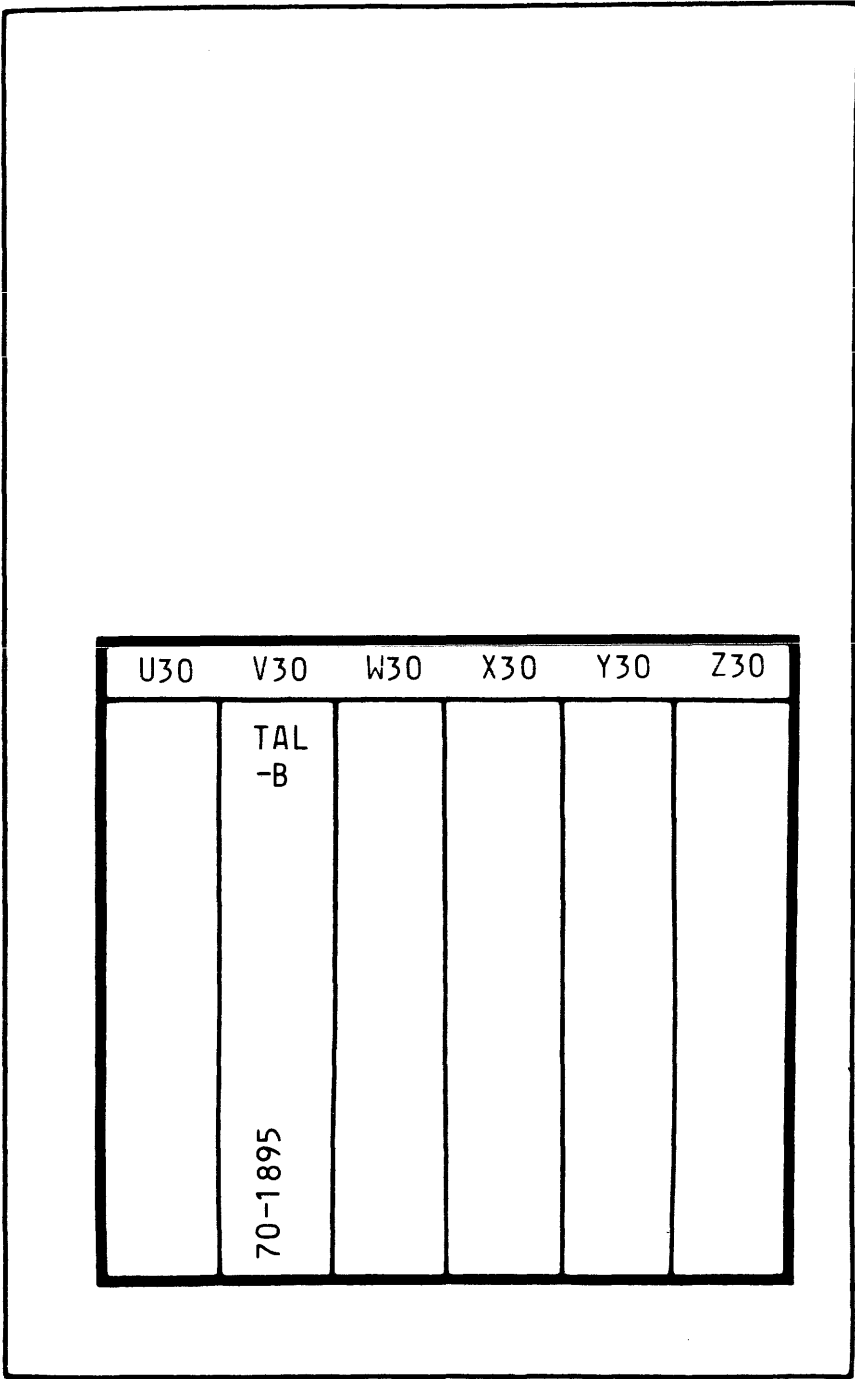
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ECN	DATE
REVISIONS	

L88-0481-02 (SH4)

Figure 7-2. ND812 Teletype/Auto Loader Interface ND-REL-A Logic Diagram (Sheet 4 of 5)

7-9/7-10

FRONT VIEW



L88-0481-00 (SH5)

Figure 7-2. ND812 Teletype/Auto Loader Interface Loading Diagram (Sheet 5 of 5)