# INSTALLATION INSTRUCTIONS <br> 1BM 7090 <br> DATA PROCESSING SYSTEM 

C. E. Installation Publications

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This publication is intended to serve as a guide for installing the IBM 7090 Data Processing System. It presents mechanical data and preliminary test procedures relevant to making the equipment operational in the customer's office.

For detailed maintenance and test procedures, refer to 7090 Reference Manual.
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All Custome $r$ Engineers are thoroughly indoctrinated in IBM Safety practices during the early phases of their training. It is expected that this training has become a part of routine practice. However, personnel safety cannot be over-emphasized. Follow the safety practices outlined in the C.E. Safety Practices card, IBM Form 124-0002-1, issued to all Customer Engineers.

Specific safety items for this system are:
A. Make sure that $\mathrm{CO}_{2}$ fire extinguishers are available in each room where frames of the system are set up.
B. In order to prevent pinching of fingers between the gate and slide frame members, keep fingers clear of gate slides when sliding a gate into the module.
C. Use caution when lowering a tailgate. When unlatched, the tailgate will free-fall to the stop limit.
D. When sliding a gate in or out, alternately observe each side to avoid hitting the laminar bus conne ctions.
E. Turn DC power off when removing or inserting an SMS card. It is possible to cause component damage by shorting to an adjacent card during this process.
F. Make sure that capacitors are completely discharged before working on DC power supplies.
G. Always turn off power before replacing any fuse.

## 1. GENERAL

This manual has been prepared to provide the necessary instructions for installing a typical IBM 7090 system configuration, Figure $1-1$, rather than a special set of instructions for each system configuration which may be installed. It will therefore be the installer's responsibility to become familiar with the machine types and quantities which will be provided for a particular installation. By becoming familiar with the system configuration the CE can take exception to information provided in this manual which is not applicable to his installation.

The CE should also be aware of special features ordered for the system to be installed as information on items such as this may required special attention that has not been specifically covered in this manual.

The main objective of the manual is to provide the necessary instructions to enable efficient and safe installation of the equipment. To accomplish this objective, however, it is necessary for the CE to read the manual very carefully before any supplies or equipment is received, so that full understanding of the information and the sequence of the installation process is achieved.

The overall content and organization of the manual with respect to the installation process is summarized in Table 1-1, Relative Sequence of Installation Process - IBM 7090. This table is not intended to show the length of time required to perform a particular operation since the time requirement is dependent upon the number of men assigned to a particular

## 1 INTRODUCTION



FIGURE 1-1. TYPICAL 7090 SYSTEM LAYOUT

TABLE 1-1 RELATIVE SEQUENCE OF INSTALLATION PROCESS - IBM 7090

| MANUAL SECTION | OPERATION | REMARKS | OPER. COMPLETE |
| :---: | :---: | :---: | :---: |
| SECTION 2 | Check Facilities <br> Set Up CE Room | 1 |  |
|  |  | 2 |  |
| Preparation of Machine Area | 3 Inventory and Store Spare Parts <br> 4 Inventory and Store Test Equip. \& Tools <br> 5 Check and Calibrate Test Equip. <br> 6  <br> 2  | 3 |  |
|  |  | 4 |  |
|  |  | 5 |  |
|  |  | 6 |  |
|  |  | 7 |  |
| SECTION 3 <br> Cable Installation And Connection |  | 1 |  |
|  |  | 2 |  |
|  |  | 3 |  |
|  |  | 4 |  |
|  |  | 5 |  |
|  |  | 6 |  |
|  |  | 7 |  |
| SECTION 4 <br> System Placement And Assembly |  | 1 |  |
|  |  | 2 |  |
|  |  | 3 |  |
|  |  | 4 |  |
|  |  | 5 |  |
|  |  | 6 |  |
|  |  | 7 |  |
|  |  | 8 |  |
|  |  | 9 |  |
| SECTION 5 <br> Testing | Testing Started <br> System Testing <br> NOTE: <br> Chart shows relative permissive starting point and possible overlap for various operations, but does not reflect lenght of time for various operations since time is dependent upon number of men assigned to a particular operation. |  |  |
|  |  | 1 |  |
|  |  |  |  |

task. The table is intended to assist the CEs in assigning manpower to the various operations by showing permissive starting times for various operations with respect to other operations and the posisible over-lap which can exist. As may be seen from the table, many operations can be performed simultaneously. It should also be pointed out that a particular operation in some cases need not be performed on all units before proceeding to another operation if a more efficient installation can be accomplished in this way. For example, corner brackets and trim must be installed on the front bottom corners of units that are butted together before final placement of the units. This operation could be deferred on units that are not butted together until final testing is in process. This has not been recommended in the table but does illustrate that all possible overlap is not indicated in the table. It may be noted from the table that cabling of the tape area is recommended before many of the assembly operations have been completed.

In the final analysis, an efficient installation is dependent on sound judgement of the CE in using the instructions provided.

## 2. EMERGENCY OPERATION

The continued operation of a customer's computer is dependent on information stored on cards, tape, disks, drums, etc. Also, equipment must be available to process the information. (Duplicate or master records should be maintained and stored in a remote area.) Make arrangements for emergency use of other equipment, transportation of personnel data, and supplies to temporary locations.

Where the continuity of operation is essential, a stand-by power source must be available.
3. GENERAL PRECAUTIONS AND PERSONNEL TRAINING

Arrange for monitoring of the computer room, air conditioning equipment room, and data storage room during non-operating hours.

Inspect steampipes and waterpipes running above the false ceilings to guard against possible damage due to accidental breakage, leakage, or condensation.

Check location of emergency exit doors in the computer area. The number of doors is dependent upon the size and location of the area.

Train personnel in such emergency measures as:
A. Proper method and sequence of shutting off all electrical power.
B. Shutting off air conditioning system.
C. Handling fire extinguishers in the approved manner.
D. Properly operating a small-diameter fire hose.
E. Evacuating records.
F. Evacuating personnel.
G. Calling fire company.
H. First Aid procedures.

## 4. RESPONSIBILITY ASSIGNMENTS

It is recommended that certain organizational assignments be made and rotated on a regular basis. This should result in increased individual responsibility and acquaint each Customer Engineer with all phases of operation.

Some suggested assignments are Preventive Maintenance Scheduling, Engineering Change Records, Stock Maintenance, and Diagnostics, Test Tapes and Test Equipment.
5. CUSTOMER ENGINEERING PARTS, TOOLS, TEST EQUIPMENT, AND FURNITURE

See letter from C.E. Department, Poughkeepsie, to local Customer Engineering Managers regarding the ordering of subject material. Furniture Is ordered through your Regional office. All spare parts, tools and test equipment are to be ordered through Mechanicsburg no later than 60 days before scheduled arrival of the machine units. For new systems, spare parts are ordered by description, e.g., "Spare Parts for 7090 System".

Order spare parts for each new unit in the system using a separate Code 01 P \& S Requisition Card for each type if parts are to be shipped to the Branch Office - or - list all machine dtypes on a MES form Code 50 if parts are to be shipped directly to the installation. Under description designate "Initial Spare Parts, type $\qquad$ ".

For replacement of systems and/or additional new type units the Branch Office should request a deck of pre-punched Parts Requisition Cards from Mechanicsburg PDC. Review these parts against your present inventory and then use the pre-punched cards as your new spare parts order for the items you want.

Customer Engineers must make an effort to keep the area clean and of good appearance. Customers cannot be expected to maintain a policy of
continual cleanliness on tape operation or within the computing room if we do not set an example.

Any shortages regarding furniture should be reported to the Local Office Manager. Check all parts immediately as they arrive at the installation and locate them in the parts cabinet.

Set up the spare parts tub file and establish proper ordering points for all parts. If required, obtain assistance in this activity from the Branch Office stock personnel. Notify the Parts Order Department, Mechanicsburg Parts Depot, immediately whenever any parts shortage oŕdiscrepancies are noted. A complete stock control procedure and parts section is included under separate cover (C.E. Basic Instruction Material).

## 6. STOCK

Stock should be maintained as described in the Basic Instruction Material. Instructions for ordering parts on an eme rgency basis are included in the introduction, to the Eme rgency Parts Center Manual. Parts are to be ordered through normal Branch Office procedures.

## 7. ASSISTANC E

7000 Series Technical Specialists exist in Local, District or Regional areas. These sources should be investigated for assistance when an emergency situation exists.

Poughkeepsie Customer Engineering should not be contacted for assistance without the prior approval of District and Regional Customer Engineering.

# 2 PREPARATION OF 

MACHINE AREA

## 1. GENERAL

The minimum physical requirements of an area for installation of an IBM 7090 are specified in 7090 Physical Planning Manual, Form No. X22-1209-1. The C.E. in charge should obtain (at least a week before cable delivery) a copy of the Physical Planning Manual and a copy of the scaled floor plan from the branch office or local sales representative. A check of the facility will be made by branch office personnel or the sales engineering representative before machine delivery. The C.E. is reminded, however, of the safety requirements specified in the Preface of this manual and of the following:
A. One week before machine delivery, all air conditioning equipment shall have been installed, tested, and ready for operation. Electrical facilities, lighting, floor ramps, painting, plastering, and decorating should also be completed at this time.
B. Cleanlines of the area must be maintained once the air conditioning equipment is ready for operation.
C. The supply air ducts and filters should be checked for cleanliness before the machine is installed. If the area under the raised floor is used as an air plenum it should be free from dust and dirt.
D. The power receptacles should be checked to determine that proper receptacles have been installed at the customers socket in accordance with the Physical Planning Manual.
E. Three-phase power receptacle should be checked for proper phasing in accordance with the Physical Planning Manual.

It should be realized that the custome $r$ is responsible for the above items and the C.E. should advise C.E. Management if discrepancies are observed.

## 2. RECEIVING SPECIAL MATERIALS

If proper ordering requirements have been observed (Ordering Instructions for 700-7000 Series Customer Engineering Materials), office equipment, test equipment, and other ordered items should arrive approximately $t$ wo weeks before machine delivery. External cables should also be received at this time. All capital items should be checked at the time of delivery and any damage reported, on the spot, to the carrier's representative and the branch office.

## 3. PREPARATION OF C.E. ROOM

The furniture and fixtures should be placed in the C.E. room in accordance with the layout obtained from the local sales engineering representative. Assemble and position the spare parts cabinet. Inventory and store spare parts in the cabinets; notify Mechanicsburgh imme diately on shortages. Label cabinets so that parts may be readily located when needed.

Keep the C.E. room clean and orderly at all times.
4. TOOLS AND TEST EQUIPMENT

Inventory and store all tools and test equipment. Test equipment should be checked over carefully, including a calibration check, as soon as possible.
NOTE
Initial calibration of scopes will be
checked against the oscillator of the 7090 before assuming the scopes to be correct. This is to avoid possible adjustment to the 7090 which might later be traced to a poorly calibrated scope.
Refer to manufacturer's instruction and/or latest C.E. procedure for repair and calibration of test equipment.

## 5. RECORD KEEPING

Many records must be prepared and maintained on the 7090. Read, and thoroughly understand, instructions that accompany the record forms. These record forms and instructions should arrive approximately two weeks before machine delivery.

The C.E. is required to set up or prepare and/or maintain the following:
A. Set up spare parts tub file and re-order points.
B. Fill out Machine Serial Number Record and forward it to Poughkeepsie.
C. Prepare and maintain an Engineering Change History Gard for each machine.
D. Maintain the C.E. Systems Performance Log which provides a permanent record of on-the-site history of the 7090. In addition to recording day-to-day events, a properly prepared log provides IBM with essential information for improving the reliability and operational life of future systems. The Poughkeepsie C.E. Department also contains duplicates of these logs from selected installations to improve service information which is sent to the field.
E. File diagnostic program writeups.

## 6. PREPARATION OF FLOOR FOR CABLE INSTALLATION AND MACHINE PLACEMENT

Holes should have been cut in the floor in accordance with the scaled lay-out of the system at least two weeks before system arrival. The hole locations with respect to the unit placement are specified in the Physical Planning Manual.

The floor should be clearly marked in accordance with the floor plan and Figure 2-1. Marking which will not be concealed by the unit when finally positioned should be placed on removable tape or other suitable means which will not deface the floor. If the floor holes are not cut as indicated in Figure 2-1, the Physical Planning Manual and floor lay-out should be checked, the reason for the discrepancy determined, and adjustments made as required by the situation, such as replacing floor



panels or slight adjustment in the location of the unit. These changes are the responsibility of the customer.

Marking should include corner location marks, machine type number, and frame number.

## 7. WALL BOXES

Wall boxes should be of a type that can be locked or held in an open position and can serve as a disconnect. Cripple any device which can lock the disconnect in the on position. Comme rcially available colored metal clips can be used to hold a CB switch open. All Customer Engineers should be familiar with the location of the main line and wall box switches and the machines they service. WHILE CABLING THE 7090, MAKE SURE THAT THE WALL BOX IS LOCKED OR HELD IN THE OPEN POSITION.

## 8. PREPARING CABLE DUCTS

Inspect all cable ducts. Correct any condition such as sharp edges in cable ducts, which might injure the cables or personnel. All ducts should be completely vacuum cleaned at the time the cables are put in place. WEAR HEAVY WORK GLOVES WHILE WORKING IN DUCTS THAT ARE METAL LINED. These gloves may be obtained locally.

1. GENERAL

The cable installation process consists of the following basic operations:
A. Placement of external cables in the raised floor.
B. Connecting external cables after machine placement.

The cables should arrive at the installation site approximately two weeks before the system arrives, permitting all cables to be placed in the floor before arrival of the system. The remaining operations are accomplished during various stages of the mechanical assembly process to permit testing of parts of the system to proceed before all assembly operations and cabling have been completed.

The detailed requirements and information for accomplishing these operations are provided in this part.

In addition, this part contains information of a general nature to assist the installer in identification of cables and locating cable connectors on the machines.
2. CABLE IDENTIFICATION

Cables are classified into the following groups:
External Cables - Power and signal cables which are usually installed below a raised floor.

Interframe Cables-Cables which are routed within a frame. A few of the se cables are disconnected for shipment; to permit a unit to be shipped in more than one section.

External cables are labeled as shown in the following illustration:


## Cable Labels

The tag with "Key No.'", at the left, is used on external cables and the key number is the same number used in the 7090 Physical Planning Manual to identify cables. The Key No. also appears in the customer cable order.

A typical "from" or "to" designation might read 02E02D, which would mean: frame 02 tailgate E , connector location 02D.

## 3. CABLES, TERMINATORS AND JUMPERS

All signal and power cables should arrive approximately two weeks before the machines and must be laid in the ducts in their proper location (as per " 7090 Physical Planning Installation Manual"), before machines arrive.

## NOTE

The above paragraph does not apply
to the central computer cables listed
in paragraph 3-2.

The heads of the cables must be below the floor level temporarily, to prevent the possibility of damage to the cables as the machines are being located. Refer to the 7090 Physical Planning Installation Manual for a description of cables.

Contact the Physical Planning Engineer if more cables are required in the installation or if any of the cables are the wrong length.

All power outlets should conform to those as stated in the " 7090 Physical Planning Installation Manual". Check the se outlets to insure that when connected, the power cables will lie beneath the floor without interference with duct covers, hoods etc.

Power cables have a male connector on one end and female connector on the other. These cables are not interchangeable end for end.

The power cables are listed in paragraph 3-1 indicating the male and female ends. See Figure3-15for addtional references.
3.1 Power Cables

|  | MALE CONNECTUR |  | FEMALE CUNNECTOR |
| :---: | :---: | :---: | :---: |
| Key Number | From | Connecto Number | To |
| $31 \%$ | Custorrer |  | - - |
|  | Receptacle | Q | 7618 |
| 32 | 7618 | R | 7608 |
| 33 | 7608 | T | 7618 |
| 34 | 7618 | S | 7608 |
| 35. | Customer |  |  |
|  | Receptacle |  | 7607 |
| $35 a$ | Customer |  |  |
|  | Receptacle |  | 7607 |
| 36 | 729 (Neare | to Chann | 729 |
| 37. | 7618 | 13 | 7151 |
| 37 a | 7618 | 1 | 7607 |
| 37 b / | 7618 | 2 | 7507 |
| 37 c | 7618 | 3 | 7607 |
| 37 d | 7618 | 4 | 7607 |
| 37 e | 7618 | 5 | 7607 |
| 37 f | 7618 | 6 | 7607 |
| 37g | 7618 | 7 | 7607 |
| 37 h | 7618 | 8 | 7607 |

3 CABLE INSTALLATION

|  | MALE CONNECTOR |  | FEMALE CONNECTOR |
| :---: | :---: | :---: | :---: |
| Key Number | From | Connector Number | To |
| $371 / 37 i$ | 7618 | 12 | 7302 |
| $37 \mathrm{j} /$ | 7618 | 9 | 7606 |
| 37 k | 7618 | 11 | $7100 \mathrm{GPU}-1$ |
| 37 m | 7618 | 10 | $7100 \mathrm{CPU}-2$ |
| 38a | 7618 | A | 7607 |
| 38 b , | 7618 | B | 7607 |
| 38 c | 7618 | C | 7607 |
| 38d | 7618 | D | 7607 |
| 38 e | 7618 | E | 7607 |
| 38 f | 7618 | F | 7607 |
| 38 g | 7618 | G | 7607 |
| 38 h | 7618 | H | 7607 |
| 38j | 7618 | J | 7606 |
| 38k | 7618 | L | $7100 \mathrm{CPU-1}$ |
| $38 \mathrm{~m} \sqrt{ }$ | 7618 | K | $7100 \mathrm{CPU}-2$ |
| 40 | 716 (T | inal Board) | 721 (Terminal Board) |
| 41 | 716 (T | inal Board) | 711 (Terminal Board) |
| 42 V | 7618 | N | 7151 |
| 43 V | 7618 | P | 7151 |
| 44 V | 7607 |  | 729 |


|  | MALE CONNECTOR |  | FEMALE CONNECTOR |
| :---: | :---: | :---: | :---: |
| Key Number | From | Connector Number | To |
| 44a $\sqrt{ }$ | 7607 |  | 729 |
| $45 \sqrt{ }$ | 716 (Te | inal Board) | 7607 |
| $46 \checkmark$ | 7618 | M | 7302 |
| * 47 | 7618 | U | 7302 |
| * Not required with | $\begin{aligned} & 7618 \\ & 22 \mathrm{~A} . \end{aligned}$ | \% | 776 |

### 3.2 Central Computer Cables

The signal line for the last tape unit in each bank is terminated with terminator block 529285.

Connect cables to the tailgate locations shown below. These cables connect tailgates " $E$ " in frames 01, 02, 03 and MEM. These cables do not drop into the duct below the floor, but go directly from tailgate to tailgate through the sides of the frames.

NOTE
Cables are marked with "from" and
"to" destinations.

| FRAME | FROM | TO |
| :---: | :---: | :---: |
| Frame 01 | $01 E-25 G$ | $03 E-37 E$ |
|  | $01 E-25 C$ | $03 E-25 E$ |
| Frame 02 | $02 E-33 G$ | $01 E-37 F$ |


| FRAME | FROM | TO |
| :---: | :---: | :---: |
| Frame 02 (Continued) | 02E-37G | 01E-37G |
|  | 02E-21F | 01E-25D |
|  | 02E-37F | 01E-37D |
|  | 02E-37E | 01E-37C |
|  | 02E-37C | 01E-37E |
|  | 02E-21G | 03E-21F |
|  | 02E-37D | 03E-21E |
| Frame 03 | 03E-17G | MEM-E-29F |
|  | 03E-21G | MEM-E-25F |
|  | 03E-25G | MEM-E-21F 7302 Oil Memory |
|  | 03E-25F | MEM-E-17E |
|  | 03E-33D | MEM-E-21E |
| 3.3 Other Cables |  |  |

The remainder of the cables will go from the tailgate to the floor and up to the tailgate in another frame. These cables will feed through the comb at the bottom of the frame.

## NOTE

No specific comb assignments will be made; however, the cables should be given comb assignments in a position relative to the tailgate connector location. Lower tailgate cables

NOTE (cont)
should feed thr ough outer comb sections. Upper tailgate cables should drop through center comb sections. The cables are listed below in order from bottom to top in each frame. The destination of each cable will be listed for
reference.

| FRAME | FROM | TO |
| :---: | :---: | :---: |
| FRAME 01 (CPU 1) | $01 F-21 C$ | $02 E-33 E$ |
|  | $01 F-21 D$ | $02 E-33 F$ |
| $01 F-21 E$ | $03 F-45 E$ |  |
|  | $01 F-21 F$ | $03 E-29 E$ |
|  | $01 F-21 G$ | $03 F-21 G$ |
|  | $01 F-25 C$ | $03 F-37 E$ |
|  | $01 F-25 D$ | $02 E-29 G$ |
|  | $01 F-25 G$ | $03 E-33 E$ |
|  | $01 F-29 C$ | $02 F-25 C$ |
|  | $01 F-29 D$ | $02 F-25 F$ |
|  | $01 F-29 G$ | $02 F-25 E$ |
|  |  | $02 E-29 F$ |


| FR.AME | FROM | TO |
| :---: | :---: | :---: |
| FRAME 01: (CPU 1) (Continued) | 01F-33C | 02F-25G |
|  | 01F-33E | 02F-29E |
|  | 01F-37F | 08H-05A |
|  | 01F-37G | 08H-09B |
|  | 01F-45C | 08H-05B |
|  | 01E-21C | 08H-09A |
|  | 01E-21D | 08H-01B |
|  | 01E-21E | 08H-05C |
|  | 01E-21F | 08H-01A |
|  | 01E-21G | 08H-01C |
|  | 01E-25F | 03F-25G |
|  | 01E-29C | 02F-21D |
|  | 01E-29D | 02F-21F |
|  | 01E-29F | 02F-21G |
| FRAME 02 (CPU 2) | 02F-21C | 03F-45G |
|  | 02F-21D | 01E-29C |
|  | 02F-21E | 03F-29F |
|  | 02E-21F | 01E-29D |
|  | 02F-21G | 01E-29F |
|  | 02F-25C | 01F-29C |
|  | 02F-25D | 03F-41G |
|  | 02F-25E | 01F-29E |

3 CABLE INSTALLATION

| FRAME | FROM | TO |
| :---: | :---: | :---: |
| FRAME 02(CPU 2) <br> (Continued) | $\begin{aligned} & 02 F-25 F \\ & 02 F-25 G \\ & 02 F-29 E \\ & 02 F-33 G \\ & 02 E-25 C \\ & 02 E-25 D \\ & 02 E-29 F \\ & 02 E-29 G \\ & 02 E-33 D \\ & 02 E-33 E \\ & 02 E-33 F \end{aligned}$ | $\begin{aligned} & 01 F-29 D \\ & 01 F-33 C \\ & 01 F-33 E \\ & 08 H-09 D \\ & 08 H-01 D \\ & 08 H-05 D \\ & 01 F-29 G \\ & 01 F-25 D \\ & 03 F-33 F \\ & 01 F-21 C \\ & 01 F-21 D \end{aligned}$ |
| FRAME 03 <br> (Multiplexor) | NOTE: Conn shown in this usesthis chan to add these. $\begin{aligned} & 03 F-21 E \\ & 03 F-21 F \\ & 03 F-21 G \\ & 03 F-25 E \\ & 03 F-25 G \\ & 03 F-29 E \\ & 03 F-29 D \\ & 03 F-29 G \\ & 03 F-33 E \end{aligned}$ | $\begin{aligned} & \text { rs to channel N are not } \\ & \text { If your installation } \\ & \text { see drawing of tailgate } \\ & 06 E-13 F \\ & 06 E-21 C \\ & 01 F-21 G \\ & 06 E-17 F \\ & 01 E-25 F \\ & M E M-E-37 F \\ & 02 F-21 E \\ & M E M-E-05 F \\ & 06 E-17 C \end{aligned}$ |


| FRAME | FROM | TO |
| :---: | :---: | :---: |
| FRAME 03 (Multiplexor) (Continued) | 03F-33F | 02E-33D |
|  | 03F-33G | MEM-E-01F |
|  | 03F-37E | 01F-25C |
|  | 03F-37F | 06F-41F |
|  | 03F-37G | 08H-09C |
|  | 03F-41E | 06F-33E |
|  | 03F-41F | 06F-37F |
|  | 03F-41G | 02F-25D |
|  | 03F-45E | 01F-21E |
|  | 03F-45F | 01F-25E |
|  | 03F-45G | 02F-21C |
|  | 03F-49D to 49G | 06F-25C |
|  | 03F-53D to 53G | For channel assignment, see tailgate drawing. |
|  | 03E-29E | 01F-21F |
|  | 03E-29G | 06E-05D |
|  | 03E-33E | 01F-25G |
|  | 03E-33G | 06E-17D |
|  | 03E-37G | 06E-21D |
| FRAME MEM (Memory) Oil | MEM-E-17F | 03E-25F |
|  | MEM-E-21F | 03E-25G |
|  | MEM-E-29F | 03E-17G |
|  | MEM-E-01F | 03F-33G |


| FRAME | FROM | TO |
| :---: | :---: | :---: |
| 7302 (Oil) Cont. | MEM-E-05F | $03 F-29 \mathrm{G}$ |
|  | MEM-E-21E | $03 F-33 D$ |
|  | MEM-E-37F | $03 F-29 E$ |

The list below includes connectors from channel N to $\mathrm{N}+1$. Check tailgate drawings if your configuration is different. This list does not
include tape or card machine connectors.

| FRAME |
| :---: | :--- | :--- |
| FRAME 06 |
| (Channel N) |$\quad$ FROM $\quad$ TO

3 CABLE INSTALLATION

| FRAME | FROM | TO |
| :---: | :---: | :---: |
| FRAME 06 (Channel N) (Continued) | 06E-09C | 06*E-21C |
|  | 06E-09D | 06*E-21D |
|  | 06E-13C | 06*E-17C |
|  | 06E-13D | 06*E-17D |
|  | 06E-13E | 06*E-13F |
|  | 06E-13F | 03F-21E |
|  | 06E-17C | 03F-33E |
|  | 06E-17D | 03E-33G |
|  | 06E-17E | 06*E-17F |
|  | 06E-17F | 03F-25E |
|  | 06E-21C | 03F-21F |
|  | 06E-21D | 03E-37G |
|  | 06E-29D | 09-29D |
|  | 06E-33C | 09-33C |
|  | 06E-33D | 09-33D |
|  | 06E-37C | 09-37C |
|  | 06E-37D | 09-37D |

The 729 II \& IV DO NOT use a power cable terminator in the last tape unit.
3.4 Tailgate E to F Jumpers And Terminators

Install the following tailgate $E$ to tailgate $F$ jumpers and terminating blocks.

3 CABLE INSTALLATION

| FRAME | FROM | TO |
| :---: | :---: | :--- |
| FRAME 01 (CPU 1) | $01 E-29 G$ | $01 F-37 D$ |
| $01 E-33 C$ | $01 F-25 F$ |  |
| $01 E-33 D$ | $01 F-41 C$ |  |
| FRAME 02 (CPU 2) | $01 E-33 E$ | $01 F-29 F$ |
| $01 E-33 F$ | $01 F-37 G$ |  |
| FRAME 03 (7607) | $01 E-33 G$ | $01 F-33 D$ |

3 CABLE INSTALLATION


## 4. COMPONENT LOCATION DRAWINGS

Figures 3-1 through3-13 show the unit connector layout and location numbers, to which external cables will be connected.




FIGURE 3-2. FRAME 02 CPU 2 WIRING

GATE F (BOTTOM)



FRAME


06* IS DATA CHAN NEL N + I. (SEE DWG. ${ }^{3}$ 532148.

NOTE 2: 06F 25C CON- ${ }^{29}$ NECTS TO 03F-53D, E, F, G; 49D, E, F, OR G. 25 (SEE TAILGATE 03).

NOTE 3: THE LAST 21 CHANNEL HAS TER MINATOR HASTER-06E-13C 130, 09C 09D. O6F-4IC, 37 C
33G.


9

5

I
23.

| $\begin{aligned} & 06 * E \\ & 17 C \end{aligned}$ | $\begin{aligned} & 06 * E 1 \\ & 170 \end{aligned}$ | $\begin{aligned} & 06 * E . \\ & 13 F^{\circ} \end{aligned}$ | $\begin{aligned} & 03 F \\ & 21 E, \end{aligned}$ | $\mathrm{R}^{2}$ |
| :---: | :---: | :---: | :---: | :---: |
|  | $\begin{array}{\|c\|} \hline \text { NOTE } \\ 06 * F \\ 21 D^{5} \end{array}$ | $\begin{aligned} & 06 \mathrm{~F} \\ & 45 \mathrm{E} \end{aligned}$ |  | ${ }^{\text {PR2 }} \sqrt{ }$ |
| $\begin{aligned} & \text { O6*E } \\ & \text { 05D. } \end{aligned}$ | $\begin{aligned} & 03 E \\ & 29 G \end{aligned}$ | $\begin{aligned} & 06 F \\ & 49 E \end{aligned}$ | $\begin{aligned} & 06 F^{\prime} \\ & 49 F^{\prime} \end{aligned}$ | PR2 |
|  |  |  | ${ }^{06 F} \mathbf{F} \mathrm{~F}^{\prime}$ |  |

GATE E (TOP)





FRAME
08
CONSOLE
7151

| $29 D$ | $33 C$ | $33 D$ | $37 C$ | $37 D$ | $45 C$ | $45 D$ | $49 C$ | 490 | $53 C$ | $53 D$ |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $06 E$ | $06 E$ | $06 E$ | $06 E$ | $06 E$ | $06 F$ | $06 F$ | $06 F$ | $06 F$ | $06 F$ | $06 F$ |  |
| $29 D$ | $33 C$ | $33 D$ | $37 C$ | $37 D$ | $45 C$ | $45 D$ | $49 C$ | 490 | $53 C$ | $53 D$ |  |

7617


FIGURE 3-8. FRAME 08 CONSOLE, 09 CHANNEL CONSOLE AND 09* CHANNEL +1 CONSOLE

NOTE

## Terminal Plugs

*P/N 532138 connects at G02A for $N$ lines P/N 532137 at H14A and H18A for P lines
**H17A to H08A
Hl3A to H04A Jumpers (32K)


FIGURE 3-9 CABLE CONNECTOR LOCATIONS -7302A


| $\begin{gathered} \text { CABLE } \\ \text { ASSY } \\ \text { PART NO. } \end{gathered}$ | $\begin{aligned} & \text { BLE CONNECTOR } \\ & \text { LOCATIDNS } \end{aligned}$ | $\begin{gathered} \text { REF } \\ \text { NO } \end{gathered}$ | $\begin{aligned} & \text { CABLE } \\ & \text { ASSY } \\ & \text { PARTNO. } \end{aligned}$ | $\begin{aligned} & \text { CABLE CONNECTOR } \\ & \text { LOCATIONS } \end{aligned}$ |  | $\left\lvert\, \begin{aligned} & \text { REF } \\ & N O \end{aligned}\right.$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | FROM : TO |  |  | FROM | TO |  |
| 587334 | OIE-33D OIF.4IC | 59 | 587343 | OIF-33C | O2F-256 | 57 d |
| 587335 | OIE-33F OIF-37C | 59 | 587344 | OfF-290 | O2F-25F | 57 c |
| 587335 | OIE-33G OIF-33D | 59 | 587345 | OFF-33E | O2F29E | 57b |
| 587335 | DIE.29G OIF:37D | 59 | 587345 | OFF-29E | O2F 25E | 57 |
| 587335 | OiE-33E DIF-29F | 59 | 587345 | OFF-29C | C2F-25C | 57 |
| 58733 | OIE-33C OIF-25 | 59 | 587 | O1F-21C | O2E-33E | 53 |
| 587337 | OLE-25D O2E-21F | 50 | 587347 | OFF-250 | O2E-29G | 53 c |
| 587339 | OEE-37D O2E-37F | 50 | 587347 | OEE-29C | 02F 210 | 55 |
| 537339 | OIE.37F O2E-33G | 50 | 587347 | CIE-29D | C2F-21F | 55 a |
| 587340 | OIE-37G O2E-37G | 50 | 587347 | OIE-29F | O2F-2IG | 55b |
| 587341 | OIE-37E O2E-37C | 50 | 587348 | OIF-210 | O2E.33F | 53 |
| 587341 | CIE-37C D2E-37E | 500 | 587349 | CIF-29G | O2E-29F | $53 a$ |



NOTEX- EACH END OF A CABLE ASSEMBLY MUST BE TAGGED WITH THE PART NO REF NQ AND FROM $\xi T O$ INFORMATION LISTED ABOVE ...

| $\begin{aligned} & \text { CABLE } \\ & \text { ASS'Y } \\ & \text { PART NO } \end{aligned}$ | $\begin{aligned} & \text { CABLE CONN. } \\ & \text { LOCATIONS } \end{aligned}$ |  | $\begin{aligned} & \text { REF } \\ & \text { No. } \end{aligned}$ |
| :---: | :---: | :---: | :---: |
|  | FROM | TO |  |
| 587334 | 02E-29E | 02F-29D | $54 a$ |
| 587334 | 02E-256 | 02F-29F | 54c |
| 587335 | 02E-25F | 02F-29C | 54b |
| 587336 | 02E-33C | I2F-296 | 54 |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |


NOTE

XI 7302A MEMORY MAY BEUSED INPLACE OF 7302

FIGURE 3-11: CABLE ROUTING AND IDENTIFICATION; 7109 ARITHMETIC SEQUENCE UNIT


4
$\frac{3}{5}$
2 2


NOTE-CABLES BETWEEN ANY TWO UPPER TAILGATES FOLIOW THE DIRECT ROUTINS INDICATED. AU


NOTEX- EACH END OF A CABLE ASSEMBIY MUST BE TAGGED WITH THE PART NO. REF NO., AND FROM \& TO. INFORMATION LISTED ${ }^{\dagger}$ ABOVE.

PART NO 587333
REF NO 65
FROM O3E-37D
TO 03F-53C
TYPICAL TAG OTHER FRAME TO FRAME CABLES ENTER AND EXIT AT THE BASE OF THE FRAME
NOTE $\because$ THESE CABLES ARE NOT REQUIRED WITH 7302 A(AR). USED ONLY WITH 7302 II 7302 A MAY BE USED $\mathbb{N}$ PLACE OF 7302 MEMORY.
 IDENTIFICATION


NOTE X- EACH END OF A CABLE ASSEMBLY MUST
BE TAGGED WITH THE, PART NO: REF. NO., AND FROM \& TO INFORMATION
LISTED_ABOVE…-


CABLE ROUTING

IYPICA TAG

AOMCDEFGHS


刻


IDENTIFICATION

## 5. CABLE PLACEMENT - EXTERNAL CABLES

Generally these cables will be routed under a raised floor. The cables are labeled with a tag as previously indicated; at one end of the cable the tag is red and at the other end the tag is white. There is also a one-inch band of tape near each end of the cable, this band, when placed at floor level, will provide sufficient cable to reach the connector. IMPORTANT

Check each cable with the installation sequence charts to determine which unit the RED label is associated with. The information in the installation sequence tables has been arranged for an efficient installation sequence and the red label does not necessarily indicate the "From" end of the cable.

Figures 3-14 and 3-15 summarize the cable installation sequence for the external power and signal cables.

The cabling information in this manual refers to a standard 7090 system. Certain cabling or terminator assignments may be different for a 7090 system on which special features are installed. Therefore, in cases where a system has special features on it, the $B / M$ instructions for these special features should be reviewed by the local C.E.'s before installation to determine if any changes are necessary in the cabling or terminator block assignments.

If these $B / M$ instructions are not received they can be procured by contacting:

Plant Customer Engineering<br>Department 910<br>IBM Corporation<br>Poughkeepsie, New York



FIGURE 3-14. EXTERNAL SIGNAL CABLES


[^0]| SEE FIGURE 3-14 |  |  | FROM |  | TO |  | Y | Z | PART NUMBER |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{gathered} \mathrm{CABLE} \\ \mathrm{GR} \end{gathered}$ | $\begin{array}{\|l\|} \mathrm{KEY} \\ \mathrm{NO} . \end{array}$ | NAME | FRAME \& GATE | CABLE CONN | FRAME \& GATE | $\begin{gathered} \hline \text { CABLE } \\ \text { CONN } \end{gathered}$ |  |  |  |
| 8 | 8 | CE CONSOLE $\rightarrow$ DATA CHANNEL | CONSOLE PNL | $37 \mathrm{C}$ | 06E | 37C | 18 | 64 | 587323 |
|  | 8 a |  |  | 33 C |  | 33 C |  | 62 |  |
|  | 8 b |  |  | 37D |  | 37D |  | 64 |  |
|  | 8 c |  |  | 33D |  | 33D |  | 62 |  |
|  | 8d |  |  | 29D |  | 29D |  | 60 |  |
| 9 | 9 | CE CONSOLE $\rightarrow$ DATA CHANNEL | $\begin{gathered} \text { CONSOLE } \\ \text { PNL \| } \end{gathered}$ | $53 \mathrm{C}$ | 06F | 53C |  | 38 | 587323 |
|  | 9 a |  |  | 53D |  | 53D |  | 38 |  |
|  | 9 b |  |  | 49C |  | 49 C |  | 36 |  |
|  | 9 c |  |  | 49D |  | 49D |  | 36 |  |
|  | 9d |  |  | 45C |  | 45C |  | 34 |  |
|  | 9 e |  |  | 45D |  | 45D |  | 34 |  |
| $10$ | $\text { (10) }=$ | MULTIPLEXOR $\rightarrow$ DATA <br> CHANNEL | 03F | 53D | 06F | 25C | 38 | 24 | 587314 |
|  | 10 aV |  |  | 53E |  | 25C | 38 | 24 |  |
|  | 10 b |  |  | 53 F |  | 25C | 38 | 24 |  |
|  | 10c |  |  | 53G |  | 25C | 38 | 24 |  |
|  | 10d |  |  | 49D |  | 25C | 36 | 24 |  |


| SEE FIGURE 3-14 |  |  | FROM |  | TO |  | Y | Z | PART <br> NUMBER |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{gathered} \mathrm{CABLE} \\ \mathrm{GR} \end{gathered}$ | $\begin{aligned} & \mathrm{KEY} \\ & \text { NO. } \end{aligned}$ | NAME | FRAME \& GATE | $\begin{aligned} & \text { CABLE } \\ & \text { CONN } \end{aligned}$ | FRAME \&GATE | $\begin{aligned} & \text { CABLE } \\ & \text { CONN } \end{aligned}$ |  |  |  |
| 10 | ${ }_{10 \mathrm{e}}^{10 \mathrm{f}} 10 \mathrm{~g}$ | MULTIPLEXOR CHANNEL $\rightarrow$ DATA | 03F | 49E <br> 49F <br> 49G | 06F | $25 \mathrm{C}$ <br> 25C <br> 25C | $36$ <br> 36 $36$ | 24 <br> 24 <br> 24 | 587314 |
| (11) | $\begin{array}{\|c\|} \hline 11 \checkmark \\ 11 a^{\prime} \\ 11 \mathrm{bV} \end{array}$ | MULTIPLEXOR $\rightarrow$ DATA CHANNEL N (BANK 2) | 03E | $\begin{aligned} & 37 G \\ & 33 G \\ & 29 G \end{aligned}$ | 06E | $\begin{aligned} & 21 \mathrm{D} \\ & 17 \mathrm{D} \\ & 05 \mathrm{D} \end{aligned}$ | 64 <br> 62 <br> 60 | 56 <br> 54 $48$ | $587314$ |
| (12) | $\begin{aligned} & 12 \\ & 12 a \\ & 12 b \\ & 12 c \end{aligned}$ | MULTIPLEXOR $\rightarrow$ DATA. CHANNEL (BANK 2) | 03F | 21E <br> 25E <br> $21 F$ <br> $33 E$ | 06E | 13F <br> 17F <br> 21 C <br> 17C | 22 <br> 24 <br> 22 <br> 28 | 52 <br> 54 <br> 56 <br> 54 | 587314 |
| (13) | 13 <br> $13 a$ <br> 13b | MULTIPLEXOR $\rightarrow$ DAT A <br> CHANNEL (BANK 2) | 03F | $\begin{aligned} & 37 F \\ & 41 E \\ & 41 F \end{aligned}$ | 06F | $41 F$ <br> 33 E $37 F$ | 30 <br> 32 $34$ | 32 <br> 28 <br> 30 | $587314$ $531641$ $587314$ |
| 14 | $14{ }^{14} 4$ | ```DATA CHANNEL N }->\mathrm{ DATA CHANNEL N + 1 DATA CHANNEL N'->DATA CHANNEL N' + l``` | 06E | $\begin{aligned} & 17 \mathrm{E} \\ & 13 \mathrm{E} \end{aligned}$ | 06E | $\begin{aligned} & 17 \mathrm{~F} \\ & 13 \mathrm{~F} \end{aligned}$ | 54 52 | 54 52 | $\begin{gathered} 587314 \text { NO } \\ \text { XII } \end{gathered}$ |

[^1]SEE FIGURE 3-14




FIGURE 3-15. EXTERNAL POWER CABLES
3. CABLE INSTALLATION

SEE FIGURE 3-15

| $\begin{aligned} & \text { CABLE } \\ & \text { GROUP } \end{aligned}$ | $\begin{aligned} & \text { KEY } \\ & \text { NO. } \end{aligned}$ | NAME | Y | Z | PART NUMBER |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 31 V | 31 | CUSTOMER RECEPTACLE $\rightarrow$ PCU | - | 24 | 532969 |
| 32 | 32 | PCU $\rightarrow$ POWER CONVERTER | 20 | *19 | 332967 |
| $33 \sqrt{ }$ | 33 | PCU POWER CONVER TER | 20 | *34 | 532970 |
| $34 \sqrt{ }$ | 34 | PCU $\rightarrow$ POWER CONVERTER | 27 | 23 | 532542 |
| 35 | 35 | CUSTOMER RECEPTACLE $\longrightarrow$ DATA CHANNEL | - | 13 | 532953 |
| 35 | 35 a | CUSTOMER RECEPTACLE $\rightarrow$ DATA | - | 21 | 532953 |
| 36 | 36 | TAPE DRIVE - TAPE DRIVE | 7 | 7 | 535098 |
| 37 | 37 37 a 37 b 37 c 37 d 37 e 37 f 37 g 37 h 37 i 37 j 37 k 37 m |  | 6 <br> 44 <br> 44 <br> 44 <br> 44 <br> 44 <br> 44 <br> 44 <br> 44 <br> 70 <br> 44 <br> 44 <br> $44 \sqrt{ }$ | 33 <br> 62 <br> 62 <br> 56 <br> 56 <br> 50 <br> 50 <br> 44 <br> 44 <br> 34 <br> 34 <br> 39 <br> 39 | 532542 <br> 532542 |
| 38 | 38a | DATA CHANNEL 1 PCU 60 <br> CYCLE   | 42 | 61 | 532973 |

SEE FIGURE 3-15

| CABLE GROUP | $\begin{aligned} & \text { KEY } \\ & \text { NO. } \end{aligned}$ | NAME | Y | Z | PART <br> NUMBER. |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | 38b <br> 38c <br> 38d <br> $38 e$ <br> $38 f$ <br> 38g <br> 38h <br> 38j <br> $38 k$ <br> 38 m |  | 42 42 42 42 42 42 42 42 42 42 | 61 <br> 55 <br> 55 <br> 49 <br> 49 <br> 43 <br> 43 <br> 33 <br> 38 <br> 38 | 532973 5 532973 |
| 40 | 40 | PRINTER $\longrightarrow$ PUNCH | 51 | 39 | 320187 |
| 41 | 41 | PRINTER $\longrightarrow$ READER | 55 | 29 | 513320 |
| 42 | 42 | $\mathrm{CONSOLE} \longrightarrow \mathrm{PCU}$ | 5 | 33 | 532553 |
| 43 | 43 | CONSOLE $\longrightarrow \mathrm{PCU}$ | 7 | 31 | 532554 |
| 44 | 44 | DATA CHANNEL $\longrightarrow$ TAPE DRIVE | 11 | 10 | 532536 |
| 44 | 44a | DATA CHANNEL $\longrightarrow$ TAPE DRIVE | 17 | 10 | 532536 |
| 45 | 45 | PRINTER $\longrightarrow$ DATA GHANNEL | -3 | 40 | 532535 |
| 46 | 46 | MEMORY $\longrightarrow \mathrm{PCU}$ | 67 | 33 | 532554 |
| 47 | 47 | ME MORY HEATER INPUT $\longrightarrow$ PCU | 162 | 20 | 532537 |
| 48 | 48 | PCU $\longrightarrow$ PRINTER | 23 | 40 | 535575 |
| NOTES <br> X CUSTOMER RECEPTACLE <br> * APPLIES ONLY TO THE FIRST 7 SYSTEMS |  |  |  |  |  |

## SEE FIGURE 3-15

DIMENSION Z WILL BE AS FOLLOWS AFTER FIRST 7 MACHINES KEY NO. 25 - 000 INCHES
KEY NOS. 33, 27 - 000 INCHES
INDICATES DIMENSION FROM BASE LINE TO FIRST FORK IN CABLE EACH CABLE SHOULD BE TAGGED WITH KEY NUMBERS ON BOTH ENDS ALL DIMENSIONS IN INCHES
XI 7302 A MAY BE USED IN PLACE OF 7302 CABLE KEY NO. 47 IS REQUIRED WITH 7302 ONLY.

## 6. GROUNDING CHECK

The ground system in the 7090 provides for tieing together electronic ground and frame ground at only one point in the system. This tie point is in the 7607 unit at $\mathrm{CH}-\mathrm{A}$.

The units are checked during mechanical assembly operations to determine that no short circuits exist between electronic and frame ground prior to any cable connecting. (Does not apply to 729 Tapes.)

It is possible that a defective cable could cause an electronic ground to frame ground loop which would be difficult to isolate if not detected immediately upon plugging the cable. Connect an ohmmeter between electronic ground and the frame while plugging cables, if a short occurs, locate the cause of trouble before continuing cabling.

## NOTE

Cables between the 7607 and 7606 should be the last ones connected, to prevent reading a short condition. If power is on the system and the 7607 is not grounded, a warning sign should be tied to the 7618 , indicating the jumper is disconnected. The 729 Tape Drives should also be left disconnected during cabling.

## 7. CABLE CONNECTION SEQUENCE

The tape system should be connected as soon as possible to prevent delays in testing of the rest of the system. The tape system must be operating to load diagnostic programs in memory.

Connect all cables in the tape system except these from the 7606 .
The rest of the external cables in the system may be connected as soon as units are in place and the required Laminar Bus Short Check has been made.

## 8. FINAL GROUND CHECK

When all units have been cabled together and the ground eircuit has been completed, the following circuits shall be common:

1. 400 Cycle AC Neutral
2. 60 Cycle Convenience Outlet Neutral
3. Frame Bond
4. Electronic Ground

Check these points at each unit by connecting between each neutral and the frame with a test light. Items 1, 2 and 3 are physically tied together in the 7618 . Within the 7618 the common point on the two relays in the 48 volt ground sensing circuit, and building ground shall be common with these circuits.
1.

GENE RAL
This section contains complete instructions for receiving, physical placement, unpacking, and mechanically assembling the system. The information is arranged in the basic order for the various operations from an overall systems standpoint, with special instructions provided for specific units as required. Table 4-1 lists all operations contained in this section with a column for each machine type number. The check marks in the column indicate which operations must be performed on each of the units. The installer should be cautioned however that it is not necessary to perform each operation on all units before proceeding to the next operation. One of the main considerations is the efficient use of manower.

It is recommended that cabling of the tape system be started as soon as the operations indicated for the 7607 and 729's have been completed. This will permit power testing of the tape area and tape sub systems testing to commence while cabling of other units is in process.

TABLE 4-1

|  | M ACHINE UNITS |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Operations | $\begin{aligned} & 7 \\ & 3 \\ & 0 \\ & 2 \end{aligned}$ | $\begin{gathered} 7 \\ 1 \\ 0 \\ 8 \end{gathered}$ | $\begin{aligned} & 7 \\ & 6 \\ & 0 \\ & 6 \end{aligned}$ | $\begin{aligned} & 7 \\ & 6 \\ & 0 \\ & 7 \end{aligned}$ | $\begin{aligned} & 7 \\ & 6 \\ & 1 \\ & 8 \end{aligned}$ | 7 6 0 8 | 7 1 5 1 | 7 6 1 7 | 7 2 9 | 7 1 0 9 |
| Receiving and Placement | X | X | X | X | X | X | X | X | X | X |
| Removal of Packing Material | X | X | X | X | X | X | X | X | X | X |
| Loosen Tower Locking Screws | X | X | X | X |  |  |  |  |  | X |
| Install Casters and Leveling Pads | x | X | X | X | x |  |  |  |  | X |
| Install Corner Bracket and TRIM | X | X | x | X | X |  |  |  |  | x |
| Level Units | x | X | x | x |  |  |  |  |  | X |
| Bolt Main Frame | X | X | X | x |  |  | X |  |  | X |
| Install Kick Plates | X | X | x | X | x |  |  |  |  | X |
| Laminar Bus Short Check | X | $\mathbf{x}$ | X | X |  |  | X |  |  | X |
| Assemble Console |  |  |  |  |  |  | X |  |  | X |

## 2. UNLOADING AND MOVEMENT OF UNITS

The carrier will normally provide movers to unload the units from the van and move them into the machine area. The C.E.'s should make sure that the carrier is informed of the following requirements for handling the equipment, to prevent injury to personnel, damage to equipment and damage to the installation.

## CAUTION

A. All machine movements are to be made on tempered masonite or ply wood to prevent damage to customer floors. Tnese units may each weigh in excess of one ton and considerable damage to flooring could occur.
B. Sufficient manpower must be used in handling and moving the units to prevent injury to personnel and damage to equipment. It is particularly important to be extra careful when moving the units on ramps or where obstructions such as cables and cable floor holes exist. It a caster should drop into a floor opening or off the side of a ramp it would be very difficult because of the height and weight of the unit to prevent it from tipping over, causing serious injury to personnel and damage to the unit.
C. Avoid twisting of units during moving on their casters. When approaching or leaving a ramp the unit must be aligned squarely with the ramp to prevent a twisting force on the tower casters, which do not swivel. The wieight of the machine may also be absorbed on only three casters if the unit is not aligned with the ramp, causing caster damage.
D. Che ck each unit as it is being unloaded for an sign of physical damage. A thorough check cannot be made until packing materials have been removed.

## 3. PLACEMENT OF UNITS

All units may be moved into their finallocation, except those which are to be butted together in their final position. SMS units which are butted together must be temporarily positioned to allow adequate space to install trim extensions.

The final placement of units should be in accordance with the custome $r$ floor plan and the instructions contained in Section II - Preparation of Machine Area. If these instructions have been followed, immediate positioning and/or alignment of units can be accomplished, by aligning the units with the marking on floors.

## 4. REMOVAL OF PACKAGING MA TERIAL

Most of the protective coverings and packing materials are easily seen and require no special instructions for removal.

The tape units are shipped with a rubber or plastic shim on the capstan as shown in Figure 4-1. To remove these shims it is necessary to manually ope rate the head take-up motor to raise the read-write head.

When packaging materials have been removed, carefully inspect all units for possible damage and check the following specific items.

NOTE
Gates on SMS Units cannot be opened until gate casters have been installed, tower casters adjusted, and the tower locking screw loosened.
A. Check power and signal connectors for bent or broken pins, loose wires and mechanical tightness.
B. Check gates for bent pins, broken wiring, loosened cards and connectors.
C. Check lubrication of the 7608. See C.E. Reference Manual for lubrication instructions.


FIGURE 4-1 CAPSi AN SHIMS - 729's

## 5. TOWER LOCKING SCREWS

Loosen the lock nut on the tower locking screw and lower the locking screw. See Figure 4-2 for location of tower locking screws on 29-1/2" frames.

## NOTE

Tower casters should be lowered sufficiently to prevent the tower from bottoming on the frame cross member when loosening the locking screw. Use special tool \#461136 when unlocking the tower screw. Final adjustment of the tower caster will be made when units have been leveled.
$29-1 / 2^{\prime \prime}$


FIGURE 4-2. TOWER 1OCKING SCREWS -
29 I/ $\mathbf{2}^{\text {" }}$ FRAMES


FIGURE 4-3. CASTER ORIENTATION

## 7. INSTALLING CORNER BRACKETS AND TRIM

The installation requirements for corner brackets and trim are shown in Figure 4-4. These parts should be carefully installed to present a neat trim line on the units. Final adjustments must be made before butting units together.


FIGURE 4-4 COHNER BRACKET AND TRIM

## 4 SYSTEM PLACEMENT AND ASSEMBLY

## 8. LEVELING UNITS

Leveling of units is required to improve the appearance of units and to permit proper tracking of the sliding gates wh en they are moved in and out.

### 8.1 7607 Leveling

To level the 7607 ichold a carpenters level on the top of the frame ( (do not rest level on covers as improper level may be obtained) checking level in both directions. Raise the leveling pad at the lowest corner sufficiently to permit adjustment of remaining pads. All casters except the tower caster should be off the floor when leveling is complete.

When the 7607 has been leveled, the tower should be moved in and out to check tower and caster adjustment as follows:

1. Observe wiring sides of gates closely, checking for possible contact with the vertical frame members on front of the unit. 2. Tower caster should be adjusted so that the tower will not bind with top frame members.
2. Gate casters should be adjusted to clear the floor by approximately $1 / 4^{\prime \prime}$ while sliding the tower in and out.
3. The gate casters are lifted off the floor when they are locked to the tower by an adjustable eccentric roller as it rides on a cam; see Figures 4-5, 4-6 and 4-7. It may be necessary to adjust the roller to obtain sufficient lift on the gates, and also to obtain a straight top cover line with respect to adjoining gates.


FIGURE 4-5. TOWER AND GATE LEVELING


FIGURE 4-6. GAJF んHIKING AOHETMENK - SMS FRAMES

11/64" Max. clearance between tower and frame when tower is tracked in and out. Adjust tower guides (two places) for free travel and equal space between sides of frames and sides of gates.


CE Fancl Cuver
line shall be even through out leng! of butted frames
1/8' vertical spacing between covers and between covers and frame

## NOTE: C.E. Panel Adjustable in tiree directions for proper alignment

Covers Parallel with Sides of Frame

Gate Casters adjusted to clear
floor by $1 / 16^{\prime \prime}$ at iniginest point of floor when sliding tower in and out
8. 2 Main Frame Leveling

When all units have been located in approximate final position, locate the highest unit and the highest point on this unit. Level this unit to a point about $1 / 2^{\prime \prime}$ to $3 / 8^{\prime \prime}$ above its highest point. Continue leveling each adjoining unit, keeping the units closely butted. Check trim line at the front and top of the unit. It may be necessary to adjust the position of the unit slightly for proper front alignment.

NOTE

The leveling pads will permit an adjustment of one inch in the height of unit. If the floor level in an installation seems to vary conside erably, the floor level should be checked. The differences in level should be noted before leveling CPU and multiplexor to make sure that the true ma chine high point with respect to floor level is obtained prior to leveling.

Tower and gate adjustments are made in the same manner as indicated for the 7607.

## 4 SYSTEM PLACEMENT AND ASSEMBLY

## 9. BOLTING MAIN FRAME

Bolting main frame units together is accomplished with two sets of clamps at the rear of a butted assembly. See Figure 4-9 for part number selection and proper placement of clamps.


FIGURE 4-8. TIE BRACKETS - MA IN FRAME

## 10. KICK PLATE ASSEMBLY

Kickplates made of expanded metal extend the cover line at the base of SMS units and permit air flow to the blowers. Kickplates must be installed on all exposed sides and the front and back of SMS units.

The method of attaching kickplates is dependent upon the type of channel used in the SMS frame, type of brackets supplied, and location of the kickplate to be installed.

The assembly requirements for the various kickplate assemblies are shown in Figures 4-9 and 4-10.


FIGURE 4-9. KICK PLATE MOUN'ING - FRONT AND REAR SMS FRAMES


FIGURE 4-10.KICK PLATE MOUNTING - SIDES SMS FRAMES

## 11. LAMINAR BUS - SHORT CHECK

This test is performed to check for possible shorts which may have occurred as a result of shipment. On each gate, use an ohmmeter to check for possible shorts between each segment of the laminar bus and all other segments. Also, check between each bus segment and frame. If any shorts are located, take corrective action and record the location of trouble.
12. ASSEMB LE AIR ME MORY UNIT, 7302A

To facilitate shipment, the Air Memory Unit is disassembled into two separate sections by removing four attaching bolts and associated electrical connectors.

The Air Memory Unit should be reassembled in accordance with Figures 4-11 through 4-24. Refer to Figures 4-11 and 4-12 as a guide to locations of units to be reassembled.

Table 4-2 lists the sequence of installation, operation performed and figure reference necessary to reassemble equipment that has been disassembled for shipment.

|  | OPERATION PERFORMED | FIGURE REFERENCE |
| :---: | :---: | :---: |
| A. | Reassembly of Power and Logic Frames | 4-13 |
| B. | Local Power Panel | 4-14 |
| C. | Cable Connections | 4-15 through 4-18 |
| D. | Blower Mounting | 4419 through 4-20 |
| E. | End Cover Mounting | 4-21 |
| F. | Front Base Cover Mounting | 4-22 |
| G. | Rear Base Cover Mounting | 4-23 |
| H. | Step Cover Mounting | 4-24 |

TABLE 4-2 AIR MEMORY INSTALLATION


FIGURE 4-11. AIR MEMORY UNIT - FRONT VIEW


FIGURE 4-12. AIR MEMORY UNIT - REAR VIEW



POWER SECTION (FRONT VIEW)

FIGURE 4-13. REASSEMBLY OF POWER AND LOGIC FRAMES (SHEET I OF 2)


FIGURE 4-13. REASSEMBLY OF POWER AND LOGIC FRAMES (SHEET 2 OF 2)


FIGURE 4-14. LOCAL POWER PANEL MOUNTING AND BLOWER CABLE CONNECTION


FIGURE 4-15. CABLE CONNECTION - TERMINAL BOARD


FIGURE 4-16. CABLE CONNECTION - TERMINAL BOARD


FIGURE 4-17. CABLE CONNECTIONS - UPPER TERMINAL BOARD


FIGURE 4-18. CABLE CONNECTORS


FIGURE 4-19. BLOWER MOUNTING - POWER MODULE


FIGURE 4-20. BLOWER MOUNTING - (EXCEPT POWER MODULE)


FIGURE 4-21.END COVER MOUNTING



CENTER SUPPORT


END SUPPORT

BASE SUPPORT
Spring \# 353580
Screw \# 383380
Lock Washer \# 9092

Spring \# 353580
Screw \# 383380
Speed Nut \# 353611


FIGURE 4-24. STEP COVER MOUNTING

## 13. SERVICING OIL MEMORY, 7302

Service the oil memory unit as follows:
A. Use an ohmmeter to check the test points on top of the array for open or shorted windings.

CAUTION
The oil is safe if handled properly. However, a thin film of oil (which may exist on an oily rag or on an oil spot on your clothes) will burn. An oil vapor will also burn. Do not smoke or light a match while working around the oil. Men working with the array and oil must have coveralls. (purchase locally).
B. Turn off power at wall box. Replace the 6 he at exchanger fuses removed earlier.
C. Disconnect the suction line at the pump and connect oil line from suction side of the pump to the pipe which will be inserted in the barrel. (See Figure 4-25.)
D. Turn power on at wall box. Depress power-on reset (7618) to energize 7302 heat exchanger. LEAVE 7302 "POWER ON" SWITCH OFF.
E. Check 208 volts 3 phase at the heat exchanger for proper phasing.
F. Fill the tank to the fill line on the gage. Do not fill higher than this line. Allow 15 minutes for air to rise from oil and recheck oil level.

## 4 SYSTEM PLACEMENT AND ASSEMBLY

G. Replace the oil line between the tank and pump. These connections should be hand tight.


## 1. GENERAL

This section contains instructions for checking and determining proper operation of the 7090 system. The information is arranged in the basic order for the various operations from an overall systems standpoint, with special instructions provided for specific units as required.
2. POWER TESTING

### 2.1 Phasing Check

The input voltages on the 7618 may be incorrectly phased which will cause blowers on the system to run in reverse. The blowers should be checked as soon as power is received on the system. Check the blower rotation as follows:
A. The blowers on all gates must rotate in a clockwise direction when viewed from the hinged end of the gate.
B. Check blower rotation by holding a strip of heavy paper or IBM card stock lightly against the rotating shaft and observe direction in which the paper is moved.

## NOTE

To change phasing that is incorrect, change any two input connections in the 7618.

### 2.2 Power-On Check

The power distribution system should be checked thoroughly in accordance with the following procedure:
A. Set all power switches to the "Off" position.
B. Set all circuit breakers to the "ON" position.
C. Set all emergency off switches to the "ON" position.
D. Set test area main power circuit breaker to the "ON" position.
E. Depress the 7618 unit power on reset switch.

NOTE
The 60 cycle power is available in the 7618 and the 48 V supply is energized when the power on reset switch is energized in the 7618 unit.
F. Set the 7608 unit circuit breaker to the "OFF" position, and then to the "ON" position.
G. Depress the 7618 unit power on switch to start the 7608 unit and/or initiate D-C power on sequence.
H. Observe the volt meter on the 7618 unit indicates a voltage when the meter selector switch is set to positions Phase 1 and 2, Phase 2 and 3 and Phase 3 and 1.
I. Set the power switches on the 7606, 7108, 7109, 7607, 7302A, 7151, 711, 716 and 721 to the "ON" position and observe power indicator lights are lit.

### 2.3 Emergency Off Switch Check

A. With power up on the system, pull the emergency off switch on the 7151 console to the "OFF" position.
B. Observe that all power is removed from the system and all indicator lights turn off and all blowers stop.

## NOTE

Power will still be present in the 7618 unit.
C. Depress emergency off switch on the 7151 console.
D. Depress the power on reset $s$ witch on the 7618 unit.
E. Set the circuit breaker on the 7608 unit to the "OFF" position and then to the "ON" position.
F. Depress the power on switch on the 7618 unit and observer that power comes up on the system.
G. Pull the emergency off switch on the 7618 unit and observe that all power is removed from the system.

## NOTE

All power will be present in the 7618 hot box.
H. Depress the emergency off switch and the power on reset switch on the 7618 unit.
I. Set the circuit breaker on the 7608 to the "OFF" position and then to the "ON" position.
J. Depress the power on $s$ witch on the 7618 unit and observe that power comes up on the system.

### 2.4 Convenience Outlet Checks

The following procedure will be used to check all convenience outlets in the system.
A. Plug a test lamp into any convenience outlet on the 7607 ,

7606, 7108, 7109, 711, 716, 721, 7151, 7618 or 7302A unit and do the following:

1. Set the test lamp switch to the "ON" position and observe the test lamp lights.
2. Unplug the test lamp from the convenience outlet and plug a polarity tester into the convenience outlet and observe the polarity tester lights.
3. Unplug the polarity tester from convenience outlet.

### 2.5 Reference Voltage Check - 7618

The output of the 7618 shall be set initially at 148 volts, with the M.G. under full load. The output voltage shall be me asured with a $1 / 4 \%$ deviation meter at the meter jacks on the control panel of the 7618. Adjust the output to 148 volts by rotating the control knob (located below the meter jacks). The final voltage setting will be made after measuring, recording and analyzing the logic voltages on the various units in the system; and determining that further adjustment of output voltage will make it possible to reduce the number of power supply adjustments which would be required to bring all logic voltages within tolerance.

### 2.6 Bias Check

The meters on the operators console are across the input of the marginal supplies; it is possible to have an indication that voltages are being varied on a particular unit without actually varying the voltage on
the gates. It is therefore necessary to check the bias voltages at the gates during the first occasion of diagnostic bias runs.

## 2. 7 Thermal and Fuse Check

These checks may be made at the convenience of the installer. With system power up, perform the checks listed in paragraphs 2.7.1 and 2.7.2.

### 2.7.1 Thermal Switch Check

Check the operation of each thermal switch listed by holding a hot soldering iron near the switch. Power should drop if switches and control, circuits are operating properly. Unit Thermal Switch Location

7108
7109
7606

7607
$\left\{\begin{array}{l}\text { Top of Gates - Row A }\end{array}\right.$
CAUTION: Insert a piece of asbestos between soldering iron and adjoining card to prevent damage to components.

### 2.7.2 Fuse Check

Che ck the fuse protection circuitry in each SMS module by removal of a fuse. Power should drop on all units in the power group.

### 2.8 Service Voltage Check

Measure and record the following voltages with a $1 / 4 \%$ deviation meter on the load side of fuses:

| Unit | $+6 \mid \%$ <br> Volt\|Dev. | $\begin{array}{c:c} +6 & * \% \\ \text { V.M. } & \text { Dev. } \end{array}$ | $\begin{array}{\|c\|c} -6 & * \% \\ \text { V.M. } & \text { Dev. } \end{array}$ | $\begin{aligned} & -12 * \% \\ & \text { Volt Dev. } \end{aligned}$ | $\begin{array}{\|c:c} -12 & * \% \\ \text { V.M. } & \text { Dev. } \end{array}$ | $\begin{aligned} & +30 * \% \\ & \text { Volt } \begin{array}{l} \text { Dev. } \end{array} \end{aligned}$ | $\begin{array}{\|l\|l\|} \hline-36 \mid * \% \\ \text { Volt } & \text { Dev. } \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 7108 |  | 1 | 1 | ! | 1 | T | 1 |
| 7109 | , | 1 | 1 | 1 | 1 | 1 | 1 |
| 7606 | 1 | 1 | 1 | 1 | i | 1 | 1 |
| 7618 |  | 1 | 1 | 1 |  | 1 | 1 |
| 7302 | 1 | 1 | 1 |  |  |  | 7 |
| 7608 |  |  |  |  | 1 |  |  |
| 7151 | 1 | $1$ | 1 | , | 1 | 1 | 1 |

[^2]
## NOTE

Loose contact pressure between fuse and fuse clips or a loose connection at the wire lug on fuse clip may cause low voltage. If any low voltages are observed, tighten these contacts and recheck voltage. A low voltage could also be caused by oxidation between fuse and fuse clip; burnishing with crocus cloth will correct this condition.

Analyze recorded voltages and determine whether or not an adjustment of the output voltage from the 7618 will bring high or low voltages within the allowable $2 \%$ deviation or reduce the number of
2. 8 Service Voltage Check (Continued)
supplies which wøuld require adjustment. If 7618 is readjusted, recheck voltages which were out of adjustments and any others which may have been driven out of tolerance.

If voltages are still out of tolerance, adjust the supplies in accordance with procedures in reference manual.

## NOT E

If all voltages on a particular supply are either high or low, adjustment of the basic voltage ( 9 volts) should be made before adjusting individual voltages.

## 3. 7302A MEMORY CHECKS

### 3.1 Write Ones and Zeros Check

A. Depress memory test key and observe memory test indicator lights.
B. Depress check reset key and observe me mory address register indicators 3 through 17 ripple on and off.
C. Depress write ones key and observe me mory data register indicators 0 through 71 ripple on and off.
D. Depress check ones key and observe check ones indicator lights and memory data register and memory address indicators continue to ripple.
E. Depress check ones key and observe check ones indicator light turns off.
F. Depress write zeros key and observe that memory data register indicators 0 through 71 turn off, while memory address register indicators ripple.
G. Depress check zeros key and observe check zeros indicator lights and the data registers 0 through 71 stay off, while the memory address registers continue to ripple.
H. Depress check zeros key and observe check zeros indicator turns off.
I. Depress memory test key and observe memory test indicator turns off and me mory address register stops rippling.

### 3.2 Store and Readout Checks

A. Set the AUTO/MANUAL key to the manual position.
B. Load all ones into all $M Q$ positions.
C. Store $M Q$ at memory address 77777 .
D. Display memory location 77777 and observe all ones.
E. Store MQ at memory address 00000 .
F. Display memory location 00000 and observe all ones.

### 3.3 Data - In - Timing Check

During final check at the customer's installation 7302 access time must be checked. There must be at least 80 nanoseconds overlap of the data-in-gate and the "MDBI" inputs while storing the following bits and scoping the data register input in the 7302 and 7302A.

| Operation | Bit | Address 00000 |  | Address 40000 |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Dig | MDBI | Dig | MDBI |
| STQ | MQ 17 |  |  |  |  |
| *SCHn | Chan LC 17 | 01A2J11-C | 01A2J11-E | 01A1J24-5 | 01A1J24-3 |
| *CSR1 | Chan DR 17 | Systems | 18.01.1 | Systems | .18.06.1 |
| STQ | MQ 35 |  |  |  |  |
| *SCHn | Chan AC 35 | 01A2J11-5 | 01A2J11-3 | 01A1J24-C | 01AlJ24-E |
| *CSRI | Chan DR 35 | Systems | 18.03.1 | Systems | 18.04.1 |
| * This must be checked on all channels installed. |  |  |  |  |  |

3.3.2 Air Memory Program

| Operation | Bit | Address 00000 |  | Address 40000 |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Dig | MDBI | Dig | MDBI |
| STQ | MQ 17 |  |  |  |  |
| SCHn* | Chan LC 17 | 01 A 6 A08-P | 01A6A08-X | 01A4A20-P | 01A4A20-X |
| CSRI* | Chan DR 17 | (Systems 01.19.03.1) |  | (Systems 01.19.09.1) |  |
| STQ | MQ 35 |  |  |  |  |
| SCHn* | Chan ADR 17 | 01A5A14-P | 01A5A14-X | 01A4A02-P | $01 \mathrm{~A} 4 \mathrm{~A} 02-\mathrm{X}$ |
| CSRI* | Chan DR 35 | (Systems 01.19.06.1) |  | $\text { (Systems } 01.19 .12 .1 \text { ) }$ |  |

Adjust - If the MDBI line is late for an entire channel (all eight conditions) the Data-In Gate may be delayed by changing the timing of the D6** at 01A5D22. The nominal delays for 7090 use is 150 nanoseconds The maximum permissible delay occurs when the rise (or end) of -DATA-IN GATE 7090. 01A5C18-Q on System 01.20.01.1, occurs no later than 1.05 microseconds after the rise (or beginning) of +N MEM SLECT, measured at 01B3J14F on Systems 01.10.01.1.
4. 7100 CENTRAL PROCESSING UNIT, 7606 MILTIPLEXOR
4.1 Waveforms and Variable Delays
A. The CP Set Pulses, Systems Diagram 02.05.05.1 should meet all requirements specified in Figure 5-1 when observed at 02A2F22G.
B. Odd and Even Clock Drive Line Pulses, Systems Diagram 08.00.44.1 should conform to the configuration shown on Figure 5-2 when observed at 03 A 4 Cl 5 F .
C. To insure proper machine functioning on all instructions, the CP SET must be aligned as follows:

1. The oscilloscope being used must contain probes of the same length.
2. Synchronize the scope on a +N Al Dl - 02A2Cl5F on systems 2.15.11.1. The other clock pulses to be mentioned are also on this system page. With respect to the Sync. Pulse, check the following:

| +N A2 Dl | No. 1 | $02 \mathrm{~A} 2 \mathrm{Cl3B}$ |
| :--- | :--- | :--- |
| +N A3 D1 |  | 02 A 2 D 20 C |
| +N A4 D1 +P |  | $02 \mathrm{~A} 3 \mathrm{Fl3B}$ |

a) These clock pulses should be approximately $182+15$ or -45 nanoseconds in duration and should repeat themselves every 2.18 microseconds. The time between the A2Dl rising through ground potential and the A3Dl rising through ground potential must be


FIGURE 5-1 CP SET PULSES


FIGURE 5.-2 EVEN CLOCK DRIVE LINE PULSES

## 5 SYSTEM TESTING

### 4.1 Waveforms and Variable Delays (Continued)

$182 \pm 40 \mathrm{nsec}$. This must also be true between the A3Dl and A4Dl. The time between the rise (at reference voltage) of the A2Dl and A4Dl must be $365 \pm 40$ nsec.
b). The distance between the leading edges of any two Dl pulses in 02Al and 02A2 (at the point of distribution to logic blocks) should be within 50 nsec . of multiples of 182 nsec. This need not be checked for all clock pulses.
3. With this accomplished the scope should be synchronized with I Time 02A2D03D with a Continuous Enter Instruction of LDQ (+0560). The following MQ test points should be checked with the CP SET being wholly contained within the gate for each set of points given. This should be accomplished by varying the delay line located in the 03D3 panel. It should be noted that negative going pulses will be viewed.

|  | CP SET |  | GATE |
| :---: | :---: | :---: | :---: |
| 1. | 02 A 2 H 18 C | - | 02A2H18D |
| 2. | 02A2H18E | - | 02A2H18F |
| 3. | 02A2H25C | - | 02A2H25D |
| 4. | 02A2H25E | - | 02A2H25F |

4. Once again synchronize the oscilloscope with I Time. Change the instruction in Continuous Enter Instruction from LDQ to

### 4.1 Waveforms and Variable Delays (Continued)

to CLA (+0500). The following AC test points should be checked with the CP SET being wholly contained within the GATE for each set of points given. This should be accomplished by varying the same delay line mentioned in Step 3. Negative going pulses will also be viewed.

|  | CPSET |  | GATE |
| :--- | :---: | :---: | :---: |
| 1. | 02 A 2 J 18 C | - | 02 A 2 J 18 D |
| 2. | 02 A 2 J 18 E | - | 02 A 2 J 18 F |
| 3. | $02 \mathrm{~A} 2 \mathrm{~J} 2 \$ \mathrm{C}$ | - | 02 A 2 J 2 DD |
| 4. | 02 A 2 J 2 ZE | - | $02 \mathrm{~A} 2 \mathrm{~J} 2 \$ \mathrm{~F}$ |
|  | 3 | 3 |  |

5. The final setting of the delay line should satisfy both steps:

3 and 4 ; that is the CP SET must be wholly contained within the duration of the gate at all eight sets of points.

## 4. 2 Delay Adjustments in Multiply Circuits

A. The delay card (EE) on Systems Diagram 02.09.54.1 at location 02A3C08 which is set 78 nanoseconds is not at all critical and will not require any adjustment. The delay card on Systems Diagram 02.09.55.1 at location 02A3D09 which is set at 52 nanoseconds delay prevents taking a MPY-ADD CYCLE before MQ35 is a One. This can be checked by the following program.

| 00000 | LDQ | 00003 |
| :--- | :--- | :--- |
| 00001 | MPY | 00004 |
| $00002 \quad$ TRA | 00000 |  |
| $00003+125252525252$ |  |  |
| $00004+$ | 000000000001 |  |

### 4.2 Delay Adjustments in Multiply Circuits (Continued)

B. Synchronize the scope on L Time Systems Diagram (02.15.13.1 at location 02AlC18H) and look at Systems Diagram (02.09.54.1 at locations 02A3E10E and E10F) El0E can be varied with respect to ElOF if necessary. The pulse on ElOE (Pre-sensed MQ-35) should gate alternate pulses on El0F (AO, A4, A8) and must not sliver with those pulses it does not gate. Other points to check are the SET and HOLD of both the AC and MQ. Using the same program and sync. pulse point compare Systems Diagram 02.05.04.1 at location 02A2H18D and H18C. H18C can be varied if necessary to gate a full SET pulse at H18D. Adjustment should also be checked to see that the gating on Systems Diagram 02.05.02.1 at location 02A2J23C and J23D is correct. The pulse on 02A2J23D should gate a full SET pulse on 02A2J23C.
4.3 Setting the Variable Delay Line in the 7090 for Floating Point Operations

The following is the approved method of obtaining exact setting for Tally Counter Delay.

1. Key in Program:

| 00000 CLA | 00003 |
| :--- | ---: |
| 00001 FAD | 00004 |
| 00002 TRA | 00000 |
| $00003+200$ | .700000000 |
| $00004+203$ | .007000000 |

2. Synchronize the scope on POD 30 Systems Diagram 02.10.30.1 at location 02D3G10C using delayed sweep. The normal time

### 4.3 Setting the Variable Delay Line in the 7090 for Floating Point Operations (Continued) <br> base should be 20 nanoseconds per CM (0.1 us magnified 5X).

3. Check the rise of FP ADD 1st step (02.10.30.1-02D1F18C). FP ADD 3rd step (02.10.31.l-02DlF18F) and FP ADD 4th step (02.10.33.1 - 02D1H23C) in relation to AllD1 (02.15.04.1

- 02D1B21G) and an AOD1 at (02.15.02.1-02D1G17C). The earliest step should start its rise at a point where the AllDl pulse reaches its most negative point. All steps should start their rise in the valley caused by the fall of AllDl and the rise of an AODl.

4. Floating Add Second and Fifth Step - Using same program the 2 nd and 5th steps should be adjusted as follows: The delay to be varied is on systems (02.10.31.1-02D3F20). The scope should be synchronized negatively on systems (02.05.05.1 - 02A2J28B -N FP ADD-SUB 2nd Step). The delay should be set such that the fall of the -O systems (02.05.02.1 02A2J22G) coincides with a peak of the -P CP SET GATED LN $2(02.05 .02 .1-02 \mathrm{~A} 2 \mathrm{~J} 23 \mathrm{C})$ in such a way that there are three distinct pulses on the output of - AND circuit systems (02.05.02.1-02A2J23A).

### 4.3 Setting the Variable Delay Line in the 7090 for Floating Point

Operations (Continued)
5. The delay to be varied for the 5th step is on systems
(02.10.34.1-02D3B14). The scope should be synchronized negatively on system (02.05.05.1-02A2J27G-N 5th step SHIFT LT). The delay should then be set in the exact same manner as described for 2nd step.
4.4 Timing on Manual Controls Single Shots
A. Systems 04.20.04.1 "Minus on any Switch":

Loc. 02ClC04 VRPF (EJVK) $\quad 1$ usec $\pm 10 \%$
Loc. 02C1D03 HL -- $\quad 30 \mathrm{msec} \pm 10 \%$
Loc. 02C1D06 AW -- 350 usec $\pm 10 \%$
B. Systems 04.20.12.1 "Clear Single Shot":

Loc. 02C2G02 VRPF (EJVK) 1 usec $\pm 10 \%$
C. Systems 04.20.17.1 "Multi Step Single Shots":
$\begin{array}{lll}\text { Loc. 02C2G13 } & \text { HL -- } & 12 \mathrm{msec} \pm 10 \% \\ \text { Loc. 02C2G10 } & \text { HL -- } & 12 \mathrm{msec} \pm 10 \% \\ \text { Loc. 02C2G15 } & \text { HL -- } & 40 \mathrm{msec} \pm 10 \% \\ \text { Loc. 02C2G16 } & \text { HL -- } & 40 \mathrm{msec} \pm 10 \%\end{array}$

## 5. 7151 CENTRAL PROCESSING UNIT CONSOLE

### 5.1 Operator's Panel

5.1.1 Enter MQ

With the machine in Manual and by use of the ENTER MQ and Operator's Panel Entry Keys, it should be possible to enter any 36 bit binary number into the $M Q$ register. The $M Q$ register indicators should always show that information which is containe d in the MQ. The ENTER MQ button should be inoperative when the machine is in automatic status.
5.1.2 Enter Instruction

With the machine in Manual and the automatic light off, depressing the Enter Instruction button should perform completely and correctly any legitimate instruction entered on Operator's Panel Entry keys. The contents of the Instruction Counter should remain unchanged when any but a transfer or skip type of instruction is executed. The button should not be effective with the machine in automatic status.
5.1.3 Display Storage

The Display Storage button should be capable of displaying in the Storage Register, the contents of any address in core storage regardless of what the contents may be. Under no circumstances should the Display Storage button be capable of modifying the contents of any storage location. This button should be effective only when

### 5.1.3 Display Storage (Continued)

the machine is in Manual and the automatic light is off. If a tag and/or indirect addressing is specified, the contents of the effective address will be displayed. Addresses from 40 K and up will not be displayed when in the storage nullification mode, (simulate).
5.1.4 Display Indicators

Pushing this button should, when the 7090 is in Manual status and automatic light is off, display contents of the Indicator Register (0-35) in the Storage Register indicators (S-35). The information should remain displayed until another operation involving the Storage Register is performed, or the Reset button is pressed. The contents of the Indicator Register should in no way influence the accuracy of the display nor should depressing the display indicators button in any way change the contents of the Indicator Register.
5.1.5 Display Effective Address

Depressing this button will modify the address portion of the Storage Register by the contents of the index register tagged in the Storage Register and replace the contents of the Storage Register with this "effective address". Storage Register positions S, 1-20 are cleared. This button operates only in Manual status with the automatic light off.

### 5.1.6 Single Step

Depressing the Single Step key results in executing the instruction whose address appears in the instruction counter previous

### 5.1.6 Single Step (Continued)

to depressing key. The Instruction Counter will be advanced or altered under control of the instruction executed. If an I/O operation is executed the machine will continue to execute instructions at high speed until the end of the I/O operation (although this feature may be suppressed by the I/O Interlock Switch, paragraph 6.1. Operation of the Single Step key is identical to the Enter Instruction key (5.1.2) if the Continuous Enter Instruction switch (6.2) is on. This key will not operate if either the Automatic or Program Stop lights are on.

### 5.1.7 Multiple Step

Holding the Multiple Step key down should result in a series of single step instruction executions. All specifications for single step operation should apply except that the machine should not stop, until either the Multiple Step key is released or a program or check stop occurs. The frequency of instruction execution is specified in paragraph 6.7.
5.1.8 Normal Off

Depressing the Normal Off button should start the following sequence of events; immediate removal of 60 cycle power from the MG set, MG blower, and all frame blowers; immediate removal of 400 cycle power from the $30-60$ volt me mory power supply; after $5 \pm 1$ second 400 cycle power removal from the standard memory

### 5.1.8 Normal Off (Continued)

supply and, after $3 \pm .5$ minutes, power should be off the memory blowers. The machine is then in normal off status with 60 cycle power still present in the PDF and at all convenience outlets. 5.1.9 Power On

If the system is in the Normal Off status pushing the Power On button will restore power. The ready status should be reached in $20 \pm 6$ seconds. A clear operation must occur as power is applied. Refer to paragraph 5.1.12.
5.1.10 Emergency Off

When this switch is pulled it should immediately remove all power from the 7090 with the exception of lines inside the "hotbox" in the PCU.
5.1.11 Reset

The Reset button should be capable of turning off any register or trigger whose indicator appears on the Operator's console. The automatic light should be off as a result of the reset. This Reset should affect neither the contents of core storage nor the machine clock. The Reset should not change the contents of the Indicator Register. Reset will also reset all channels that are not in manual status (See 7607 Reset).
5.1.12 Clear

With the machine in Automatic, the Clear button should perform all the functions of the Reset button and should, in addition,

### 5.1.12 Clear (Continued)

reset the machine Clock and Reset all core storage locations to zeros. This button should not be effective when the machine is in Manual. The Clear button should also reset the Indicator Register. The Clear button will also reset all channels that are not in manual status.
5.1.13 Load Cards and Load Tape

Depression of one of these buttons results in storing the first three words from either the Card Reader or Tape Unit \#l on Channel A; into memory addresses 0,1 and 2 providing Data Channel A with the first word as an I/O command; and starting the CPU with the second word stored as its first instruction. The machine must be in automatic status and the Ready light should be on for proper performance. Depression of a Load button will then:
A. Reset the Instruction Counter, Address Register, Program Stop light, Simulate light and all indicators and registers in all channels in Automatic status.
B. Set Card Reader Select (or Tape Read Select and Unit Select 1), Ind. $S$ and Word Counter indicators 16 and 17 , in Channel $A$ (if Channel A is attached and in Automatic status).
C. Channel A will normally store three words and then read a command from Memory address 00000.

### 5.1.13 Load Cards and Load Tape (Continued)

D. As Channel A reads out its command, the Master Stop trigger in the CPU should go off and Address Register position 17 should be set on, thus starting the CPU with the instruction at address 00001.

### 5.1.14 Start

The Start button should be capable of resetting the Program Stop trigger. This resetting function should be effective any time regardless of the status of the Automatic Manual Switch. When the Auto/ Manual switch is in Automatic, the Start button should also be capable of resetting the Master Stop trigger.

### 5.1.15 Auto/Manual Switch

The switch must operate in a manner described in paragraphs 5.1.6 and 5.1.13, in addition, switching from automatic to manual while running a program should cause the machine to stop. If an I/O program is running, this-stop will not occur until whatever units were selected have disconnected. The PROGRAM STOP light is not affected by this switch.

### 5.1.16 Sense Switches

The Sense switches shall operate in the proper manner when consulted by the appropriate sense instruction, skipping when the switch is down, not skipping when the switch is up.

### 5.1.17 Sense Lights

The Sense lights shall operate in the proper manner when turned on or off by appropriate Sense instructions, skipping when the light is turned on, not skipping when the light is off.
5.1.18 Operator's Panel Entry Keys

The contents of these keys may be entered into the Storage Register and Multiplier-Quotient using the Enter MQ button or the ENK instruction. The contents of these keys will be set into the Storage Register, Instruction Register and the Tag Register when using the Enter Instruction Key, or when using the Continuous Enter Instruction switch and Start, Single-Step, Machine Cycle or Multiple Step keys. An Entry Key being down represents a "one" or "Minus". 5.1.19 Operator's Panel Entry Keys Reset Pressing this key shall restore all OP PNL keys to the zero position. This operation shall take a maximum of two seconds and must not affect the machine in any way other than resetting the keys.

### 5.2 C.E. Test Panel

### 5.2.1 I/O Interlock Switch

This switch is effective when the Automatic/Manual switch is set to Manual. With both switches set to Manual positions the machine will stop after executing each instruction. With the I/O Interlock switch set on Automatic, the machine will not stop is an I/O device is in operation. This normal setting (Automatic) allows the computer to continue at high speed after I/O selection to provide instructions to serve the I/O device. The machine will stop after each instruction providing that no I/O device or Data Channel is in use.

### 5.2.2 Continuous Enter Instruction

This switch is effective in Automatic or Manual status. With this switch on, all instructions are obtained from the Operator's Panel Entry keys rather than from memory. The Instruction Counter does not advance for each instruction, and the Instruction Counter's contents will not be altered unless a skip, trap, or transfer results from the instruction in the Entry keys.

### 5.2.3 DC On

This switch controls the 400 cycle power supplied to the
7151. Putting it in the off position will immediately remove all power except that to the convenience outlets and reset motor. All voltages should be normal in the console within $10+6$ seconds of putting this switch on.

### 5.2.4 B Cycle Controls

All these switches allow the machine to operate normally when they are down. Any of these switches in the up position will turn off the ready light and modify operation as follows:
A. Interrupt - Prevents the 7606 from obtaining a B cycle by inter rupting a convert instruction.
B. Share - Denies the 7606 access to core storage during MFL Cycles.
C. End OPN - Prevents the 7606 from taking a B cycle when a MF instruction ends operation.

### 5.2.5 Machine Cycle Jack

When the machine cycle key is inserted in this plug depressing the key once should cause the machine to execute one and only one cycle. When the machine cycle key is not plugged in, a plug shorting pins 1 and 3 of the jack must be inserted.

### 5.2.6 Auxiliary Start and Reset Jack

When the Auxiliary Start and Reset buttons are plugged
into this jack they should operate in the same way that the operator's panel start and reset buttons work. See paragraph 5.2.5 for condition when buttons are unplugged.

### 5.2.7 Multiple Step

If this switch is in the ihigh speed position, the 7090 should when the multiple step key is depressed, execute $50 \pm 10$ instructions per second. The rate when the switch is in the low speed position should be $10+2$ instructions per second.

## 6. 7607 DATA CHANNEL

6. 1 Single Shot Multivibrator Timings
A. Each of the single shot multivibrator or variable-delay circuits
listed below must meet the specified timing duration:

| Systems | Name | Nominal Duration | Acceptable Duration |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 60.36.02.2 | Backspace Interlock | 10.0 us | 9.0 | - | 11.0 us |
| 60.36.02.2 | EOR Pulse | 10.0 us | 9.0 | - | 11.0 us |
| 60.40.12.1 | Manual Switch | 3.0 ms | 2.7 | - | 3.3 ms |
| 60.40.12.1 | Manual Switch | 118.0 us | 105.0 | - | 130.0 us |
| 60.50.10.1 | Tape Selected | 3.0 us | 2.8 | - | 3.2 us |
| 80.40.01.1 | Manual Pulse | 215.0 us | 212.0 | - | 218.0 us |
| 80.50.04.1 | Select Pulse | 4.0 us | 3.5 | - | $\therefore 4.5$ us |
| 80.60.01.1 | Disconnect Pulse | 4.0 us | 3.5 | - | 4.5 us |
| 80.80.01.2 | Card Sample Pulse | 4.0 us | 3.5 | - | 4.5 us |
| 60.36.05.1 | Select and Ready | 3.0 us | 2.8 | - | 3.2 us |
| 80.50 .03 .1 | Card EOR Pulse | 4.0 us | 3.5 | - | 4.5 us |
| 61.60.50.1 | Select and Rewind DLYD | 3.5 us | 3.2 | - | 4.0 us |

### 6.2 Channel Error Circuits

A. Check write compare circuits by:

1. Removing one at a time the cards in the following positions, and writing Tape all ones, with Data Channel in Manual OffLine status. The cards listed are located on page 61.40.10.1 of TAU manual.

| 6B4G15 | 6B4G22 |
| :--- | :--- |
| 6B4G16 | 6B4G23 |
| 6B4G17 | 6B4G24 |
| 6B4G18 | 6B4G25 |
| 6B4G19 | 6B4G26 |
| 6B4G20 | 6B4G27 |
| 6B4G21 | 6B4G28 |

NOTE
The channel should be reset after each card is pulled and re-inserted.

### 6.2 Channel Error Circuits (Continued)

2. Error Trigger should come on for each card pulled.
B. Test R/W VRC Trigger
3. From the Data Channel Console manually write a record containing all ones.
4. With each of the following pairs of cards removed the error trigger and RW/VRC triggers should be turned on when the above mentioned record is read:

$$
\begin{array}{lll}
\text { 6B4G15 } & \& & 16 \\
\text { 6B4G17 \& } & 18 \\
\text { 6B4G19 } & \& 20 \\
\text { 6B4G21 } & \& 22 \\
6 B 4 G 23 & \& & 24 \\
\text { 6B4G25 } & \& 26 \\
6 B 4 G 27 & \& & 28
\end{array}
$$

C. Test Gating of Skew Reg $B$ to $R / W$ Register when Register $A$ is redundant.

1. Fill memory with all ones.
2. Manually rewind Drive and load a control word of 77777 Address 00000.
3. Write Tape and Rewind.
4. Remove card 06 B 4 G 28 .
5. Clear Memory.
6. Load same control word mentioned above and read tape.
7. Give a memory test (Ones). Only one position in memory should be zero. Address 77777.

## 6. 2 Channel Error Circuits (Continued)

8. Re-insert card 06B4G28.
D. Test LRCR Error Gating Error Trigger
9. Manually write record containing all ones and rewind.
10. Remove card 06B2Kl8.
11. Remove the following cards, one at a time and read the record mentioned above.

| 6 B 4 C 09 | 6 B 4 C 17 |
| :--- | :--- |
| 6 B 4 C 11 | 6 B 4 C 19 |
| 6 B 4 C 13 | 6 B 4 C 21 |
| 6 B 4 C 15 |  |

4. The Error Trigger should come on for each card removed. The above mentioned cards are located on page 61.50.40.1 of the TAU manual.
E. Test Echo Check Circuit
5. Jumper 6B2K10E and 6B2K10F.
6. Write a record on tape.
7. The NO EGHO, ECHO ERROR, and ERROR triggers should come on.

## F. Test TWI Error Circuit

1. Write Cycle one word records in binary (bit 2 in first five characters and bit 1 in 6th character) from Data Channel Console.
2. Rewind and remove final amp card for track one (06B4J27).

### 6.2 Channel Error Cirguits (Continued)

3. Read from Data Channel Console in binary mode, not cycle, and TWI switch on (down).
4. The TWI indicator and Register A ERR TGR should turn on.
5. Turn TWI switch to off position (up).
6. Read in binary mode, not cycle.
7. TWI indicator should not turn on, there will be Register A ERR.
8. Read in BCD mode, not cycle, and TWI switch on.
9. TWI indicator should not turn on, Reg. A ERR and R/W VRC will be on.
10. Replace card 06B4J27.
G. Test WD NOISE Error Circuits
11. Write a long record of all bits (from Data Channel Console).
12. Backspace and reset channel when backspace is approximate in the middle of the record.
13. Write an End of File.
14. WD NOISE indicator should turn on, WR COMP and Register A Error may also turn on.
H. Test WR SKEW - Error Circuits
15. Remove ABZW location 06B4D12, and place ANZZ in the same location.
16. Write tape continuously all bits from Data Channel Console.

## 6. 2 Channel Error Circuits (Continued)

3. Write Skew Error indicator should turn on.
4. Remove ANZZ (06B4D12) and insert original ABZW.
I. Test Error Retention Logic (Baby Sitters)
5. From CPU write approximately $1 / 4$ reel of 1 word records of all bits in Binary.
6. Rewind tape and put channel in automatic and off line operation.
7. From CPU read one word record in BCD, loop program to continue reading.
8. Channel tape error triggers Reg. A and RW/VRC should turn on and remain on.
9. Perform following steps while reading tape from CPU.
10. Depress channel reset button, error triggers should be reset and remain reset while button is held depressed.
11. Lift channel "On/Off Line" switch to place channel in "On Line Operation".
12. Error triggers should not remain on, reset being accomplished by logical reset at beginning of each read operation.
J. To Insure Gating of Skew Register B with Read Clock Gate During Reg. A Error.
13. Write cycle several one word records (1,2, and B bit in lst, 2nd, 3rd characters) from channel console in Binary Mode).

## 5 SYSTEM TESTUNG

## 6. 2 Channel Error Circuits (Continued)

2. Remove Hi clip C Skew Register. A amp card (06B4H16).
3. Read in not cycle and in Binary Mode the above records with T WI Switch turned on. Records should be read without TWI error, Register A error will turn on.
4. Execute steps 1, 2, and 3 for Model H , IV, V and VI (Hi and Lo Density).
K. 7607 Models LI and IV, Data Channels ( 800 BPI ) will have a binary trigger used for switching the read clipping levels when rereading a redundancy. The trigger should be tested as follows:
5. With the Data Channel reset measure the voltage ( 20,000 ohms / voltmeter as a minimum) at 06B4J27A with respect to -12 volts. Adjust the potentiometer on the ARF card at 06B4F13 to read -0.6 V .
6. Manually write several one word records in the Binary Mode. Rewind the tape unit and read two records then read the next record in the BCD Mode. The TAU error trigger should signal a redundancy. Backspace record and read forward (BCD) and the clipping voltage at 06B4J27A should drop to 0.0 volts. The voltage at 06 B 4 J 27 D should remain at +1.8 V . Another backspace and read forward should change the low clip level at 06B4J27A to -0.6 V . The clipping level should change alternately when a redundancy is re-read. At the zero

## 5 SYSTEM TESTING

## 6. 2 Channel Error Circuits (Continued)

clipping level, first bit off register B is inoperative.
3. Backspace record and read forward (BCD) the low clip level should change to 0.0 volts. With the TAU error trigger still on read forward the next record and the low clip level should go to -0.6 volts with the rise of read delay.
4. Measure 06B4J27A as before and backspace several records to be sure that the low clip level remains at -0.6 volts while backspacing.

## 7. 7617 DATA CHANNEL CONSOLE

The 7617 Data Channel Console is a combined operator's console and C.E. Test Panel. The Operator's Panel on the 7617 Data Channel Console is checked as listed in paragraphs 7-1 through 1-14 and the CE Test Panel on the 7617 Data Channel Console is checked as listed in paragraphs 7-15 through 7-21. 7. 1 Auto/Manual Switch

In automatic, this switch permits normal operation of the machine while also isolating the entry keys and manual control switches in the channel. It also permits all resets initiated by the 7090 to reset the channels.

## 7. 2 Reset Switch

This button is operative only if the Auto Manual switch is in the manual status. If in manual status, depression of the reset button will reset all indicators, registers, and counters in the channel except the WC-zero indicator. When the channel is in automatic, all resets are under control of the 7090. (Refer to paragraph 7.8)

## 7. 3 Load Data Register

Depression of this button gates the entry keys to the data register if the channel is in manual. This button has no effect if the channel is in automatic.

### 7.4 Store Data Register

Depression of this button will cause the contents of the data register, if the channel is in manual status, to be stored in magnetic core storage

## 7. 4 Store Data Register (Continued)

at the address set up in the Address Counter. This button has no effect if the channel is in automatic status.

## 7. 5 Display Storage

Depression of this button will cause the contents of the storage location whose address is set up in the Address Counter to be displayed in the data register if the channel is in manual status. This button has no effect if the channel is in automatic status. Each time the button is pressed, the address counter is stepped once, displaying the next successive memory location. 7. 6 Load Command

Depression of this button causes information set up on the entry keys to be entered into the indicators, word counter, and address counter. Entry keys $S, 1,2$, and 19 are gated to the corresponding indicators entry keys 3 thru 17 are gated to the word counter and entry keys 21 thru 35 are gated to the address counter. The data register is cleared by this operation.

## 7. 7 Load Location Counter

Depression of this button causes the information set up in the entry keys 21 thru 35 to be entered into the location counter if the channel is in manual status.

## 7. 8 ON/OFF Line

In manual and with the On/ Off Line switch in the On Line position, data may be transmitted to or from core storage. In manual and switch in the Off Line position, no information will be transmitted to or from core storage

### 7.8 ON/OFF Line (Continued)

except by using CSRI or CSRO switches or display storage or store data register keys. When writing manually in the Off Line position, the contents of the data register will be written repeatedly. With the channel in automatic operation and the switch in "on-line" position, tape error triggers will be reset logically at the beginning of each operation. With channel in automatic and the switch in the "off line" position, the tape error triggers will remain on until the channel reset button is depressed. The tape "Master Error" trigger which turns on channel "tape check" is not affected.

## 7. 9 BCD Select

This is a latching type of switch. When in the latched position, tapes will be read and written in the BCD Mode when selected. The BCD SELECT switch is effective only if the channel is in manual status. 7.10 Stop Write

This switch is effective only if the channel is in manual status. The Stop Write switch is primarily a service tool but is located with the manual select switches because it is used in conjunction with the Write Tape Switch. The Stop Write switch is used to stop write tape test operations. 7. 11 Read Tape, Write Tape, Read Card Reader, Write Printer, Write Punch

The operations of each of these switches is similar in that each one may be used to initiate some type of data transmission operation subject to the effect of the On/Off Line switch and the requirements that the channel be
7.11 Read Tape, Write Tape ... (Continued)
in manual status. If a command is loaded prior to the selection of the I/O operation, while On-Line, the operation is basically the same as if a select instruction and the RCH instruction were executed by the Central Processing Unit. 7. 12 WEOF Select, Rewind Select, Backspace Record, and Backspace File

Each of these switches may be used to initiate the appropriate non data select operation when the channel is in manual status.
7. 13 Unit Select (Rotary Switch)

The rotary unit select switch is effective only if the channel is in manual status. For tape operations, the Unit Select switch determines which tape drive is to be selected. For manual printer and punch operations, the switch setting may be used to select Sense Exits.

## 7. 14 Tape Density Selection Switch (Rotary Switch)

This three position switch, determines which pair of densities may be selected in the 7607 Model III and IV Data Channel.
Switch Setting Density (BPI)

| A | $800-556$ |
| :--- | :--- |
| B | $800-200$ |
| C | $556-200$ |

### 7.15 Print Binary/TWI

For Printer Test - In the ON position (up), if the channel is in manual and the write printer switch is depressed, the printer will be selected and print out the contents of memory locations as selected by the address

## 7. 15 Print Binary/TWI (Continued)

counter. Ones will be printed for each binary bit in a memory location. Two binary words will be printed per line. The print binary test feature is inoperative with channel in automatic.

The TWI function of this switch is as follows: either in automatic or manual read tape operation; with the switch in the down position (TWI) and Binary Mode selected, tape circuitry will test at the end of record to see that a multiple of six characters have been read. If the tape group counter is at a position other than group six, a "Tape Word Incomplete" error will be selected. With this switch in the up position (not TWI) the tape word incomplete circuits are deconditioned to permit reading special tapes which do not have multiples of six characters per word.

## 7. 16 Tape Cycle Switch

This switch, when used in conjunction with the Read Tape switch will permit reading until a "tape Mark Record" is sensed and then force a rewind and re-read operation. When used in conjunction with the Write Tape switch this switch will cause a series of one word records from the Data Register to be written until the Stop Write switch is depressed. Cycle Backspace Record and Backspace File is also possible. The Reset key should be used between different select operations. The Tape Cycle switch is used only with the On/Off Line switch in the Off Line status. 7.17 Card Cycle Switch

This switch provides a gate for the Hand key for the simulation of card machine CB operations. (Refer to paragraph 7.18).

### 7.18 Card Hand Key Plug

This plug is used to connect a portable Hand key. When the card Cycle switch is in the OFF position, holding the Hand key depressed will cause continuous stepping of the card ring and CB counter.

When the Card Cycle switch is in the ON position, each depression generates only one write or read pulse and the CB counter is stepped after each group of four depressions. The actual read or write pulses will not be generated unless a card machine has been selected, but the card ring and $C B$ counter will advance with or without a card machine selected. The selected card machine must not be in ready status.

### 7.19 Continuous Storage Read - In Switch

In manual operation, the contents of the Data Register of the channel in manual is continuously stored at the address in the channels address counter. In automatic operation, the address counter and word counter are stepped until the word count equals zero. The data is stored in sequential addresses in memory. A me mory cycle should be requested once every fourth cycle.

### 7.20 Continuous Storage Read - Out Switch

The contents of the storage location specified in the address counter is continuously set into the Data Register, with the address counter being stepped in automatic and prevented from being stepped if the channel is in manual. In automatic, the word counter is stepped down until it reaches zero and stops operation.

## 5SYSTEM TESTING

### 7.21 Stop On Error

This switch is effective only in manual and Off-Line status. When in the ON position, tape writting will stop whenever the tape error trigger goes on. When reading tape, the tape will stop at the end of the record in which a tape error occurs.
8. TAPE ADAPTER UNIT (62.5 KC) FOR MODEL I AND II DATA CHANNEL

### 8.1 Tape Adapter Oscillators

There are ten different Oscillator Cards necessary to supply timing reference pulses for six different character rates. Three oscillators are gated for use with a given tape unit and density.

| Oscillator | Type | Tape <br> Machine | Frequency <br> Accuracy | Function |
| :--- | :--- | :--- | :--- | :--- |
| 6.67 KC | Crystal | 729 II | $\pm 1 \%$ | DC MS Control |
| 10.0 KC | Crystal | 729 IV | $\pm 1 \%$ | DC MS Control |
| 240 KC | Crystal | 729 II | $\pm 1 \%$ | DC US Control \& WC Drive 200 bpi |
| 240 KC | Clamped | 729 II | $\pm 5 \%$ | RC Drive 200 bpi |
| 360 KC | Crystal | 729 IV | $\pm 1 \%$ | DC US Control \& WC Drive 200 bpi |
| 360 KC | Clamped | 729 IV | $\pm 5 \%$ | RC Drive 200 bpi |
| 667 KC | Crystal | 729 II | $\pm 1 \%$ | DC US Control \& WC Drive 555.5 bpi |
| 667 KC | Clamped | 729 II | $\pm 5 \%$ | RC Drive 555.5 bpi |
| 1 MC | Crystal | 729 IV | $\pm 1 \%$ | DC US Control \& WC Drive 555.5 bpi |
| 1 MC | Clamped | 729 IV | $\pm 5 \%$ | RC Drive 555.5 bpi |

### 8.2 Tape Adapter Clocks

Both a read and a write clock are used. Their limitationsare as follows:
8.2.1 Read Clock (RC)

The read clock consists of four binary triggers separated
by a 400 milli-micro second timing pulse derived from a clamped oscillator and a SS. The trigger outputs are used as read timing control and their limitations are as follows:

### 8.2.1 Read Clock (RC) (Continued)

| Read Clock Output | 729 II Lo | 729 LI Hi | 729 IV Lo | 729 IV Hi |
| :---: | :---: | :---: | :---: | :---: |
| RC-3 | 13.0 usec | 5.0 usec | 8.8 usec | 3.5 usec |
| RC-4 | 17.2 usec | 6.5 usec | 11.6 usec | 4.5 usec |
| RC-7 (WR) | 21.4 usec | 8.0 usec | 14.4 usec | 5.5 usec |
| RC-6 | 25.6 usec | 9.5 usec | 17.2 usec | 6.5 usec |
| RC-7 (RD) | 29.8 usec | 11.0 usec | 19.9 usec | 7.5 usec |
| RC-7 Reset (RD) | 30.6 usec | 11.8 usec | 20.7 usec | 8.3 usec |
| RC-7Reset (WR) | 22.2 usec | 8.8 usec | 15.2 usec | 6.3 usec |

All read clock timings are $\pm 5 \%$ and are measured with respect to the rise of the first bit line.
8.2.2 Write Clock (WC)

The write clock consists of four binary triggers separated
by 400 millimicro second delay lines. These triggers are driven in parallel by a 400 milli-micro second timing pulse derived from a crystal oscillator. The trigger outputs are used as write timing control and the limitations are as follows:

| Write Clock Output | 729 II Lo | 729 II Hi | 729 IV Lo | 729 IV Hi |
| :---: | :---: | :---: | :---: | :---: |
| WC-1 | Reference | Reference | Reference | Reference |
| WC-3 | 8.32 usec | 3.00 usec | 5.56 usec | 2.00 usec |
| WC-5 | 16.60 usec | 6.00 usec | 11.10 usec | 4.00 usec |
| WC-9 | 31.50 usec | 11.50 usec | 21.10 usec | 7.75 usec |
| WC-14 | 54.10 usec | 19.50 usec | 36.10 usec | 13.00 usec |
| WC-1 | 66.60 usec | 24.00 usec | 44.50 usec | 16.00 usec |
| All write clock pulses are $\pm 1 \%$ with respect to the turn on of |  |  |  |  |
| the WC 1 Timing Pulse. |  |  |  |  |

8.3 Delay Counter (DC)

The delay counter consists of ten binary triggers. The DC 1 Trigger is driven directly from the Oscillator forming the Drive timing pulse and the Sample Pulse. The next four are driven in parallel by a 400 millimicrosecond timing pulse while the next five are driven in series by the output of the previous trigger. The purpose of this circuit is to control tape motion and data flow timings. Delay counter timings are named according to the agte lines and the count that the AND circuit totals.

### 8.3.1 Micro Second Control

Read Disconnect Delay (RDD) and Write Disconnect Delay
(WDD).

| Micro Second Control | 729 II Lo | 729 II Hi 729 IV Lo | 729 IV Hi |
| :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { RDD - } 36 \\ & R D D-128 \\ & R D D-136 \\ & R D D-144 \\ & R D D-144 \\ & \text { WDD - } 60 \\ & \text { *Read Clock Gate } \end{aligned}$ | 150 usec <br> 532 usec <br> 566 usec <br> 600 usec <br> 600 usec <br> 250 usec <br> 33.3 to 41.6 us | 54.0 usec  <br> 192.0 usec  <br> 204.0 usec 100 usec <br> 216.0 usec 355 usec <br> 216.0 usec 400 usec <br> 90.0 usec  <br> 12.0 to 15.0 us 22.2 to 27.8 us  | 36.0 usec <br> 128.0 usec <br> 136.0 usec <br> 144.0 usec <br> 144.0 usec <br> 60.0 usec <br> 8.0 to 10.0 us |
| All delay counter microsecond timings are $\pm 1 \%$ except <br> RDD- 36 which is $\pm 2 \%$ and Read Clock Gate which is $\pm 6 \%$. All timings are measured in respect to the turn on of RDD or WDD trigger control. |  |  |  |

*To measure Read Clock Gate cycle write one word records with bits 1 \& 2 in first character and bit $l$ in following characters, remove Hi clip card (06B4G28) and cycle read; Rewind and cycle Read, measure timings during Read.
8.3.2 Milli Second Control - Read Delay (RD), Write Delay (WD)
(RDD), (WDD), and Backspace Timings.

| MilliSe cond Control | 729 II | 729 IV | Tolerance |
| :---: | :---: | :---: | :---: |
| RDD - 16 | 2.4 ms | 1.6 ms | $\pm 12 \%$ |
| RDD - 22 RDD 38 | $5.7 \mathrm{~ms} \pm 1 \%$ | 2.2 ms | $\pm 2 \%$ |
| RDD - 64 | 9.6 ms | 6.4 ms | $\pm 1 \%$ |
| RDD - 152 | 22.8 ms | 15.2 ms | $\pm 1 \%$ |
| WDD - 20 | 3.0 ms | 2.0 ms | $\pm 3 \%$ |
| RD - 30 | 4.5 ms | 3.0 ms | $\pm 2 \%$ |
| RD-160 | 24.0 ms | 16.0 ms | $\pm 1 \%$ |
| WD - 320 | 48.0 ms | 32.0 ms | $\pm 1 \%$ |
| D - 50 | 7.5 ms | 5.0 ms | $\pm 1 \%$ |
| D-96 | 14.4 ms | 9.6 ms | $\pm \quad 1 \%$ |
| D - 160 | 24.0 ms | 16.0 ms | $\pm 1 \%$ |
| Backspace - 180 | 27.0 ms | 18.0 ms | $\pm 1 \%$ |

All Delay Counter Millisecond timings are measured in respect to the rise of the Millisecond Control Gate, except Backspace. Timings are referenced to the rise of RDD.

### 8.4 Final Amplifier

The basic TAU Final Amplifier consists of three SMS cards. Each card serves a specific function in the chain of events between the read bus signal and the ultimate -N current mode pulse which sets the read register. To the basic final amplifier, two more cards for each track are added to form the B Channel of the Dual Channel System. The tolerance of these acceptance levels and the respective card outputs follows:

Adjust the D. C. Voltage pin'A"for "Read".

1. A high impedance meter must be used ( 20,000 ohms per volt).

### 8.4 Final Amplifier (Continued)

2. Adjust pot. on card - 06B4Fl3 to set voltage on pin "A" of AFC -
(amp card) to -0.6 v with respect to -12 v . Channel must be in reset condition.
8.4.1 DC Measurements

$$
\begin{aligned}
& \text { AFC - Input Pin A (common - 12V DC Ref.) } \\
& \text { Write - } 1.74 \mathrm{~V} \text { DC } \leq \mathrm{Va}_{\mathrm{a}} \leq-2.17 \mathrm{~V} \mathrm{DC} \\
& \text { Read }-0.40 \mathrm{~V} \mathrm{DC} \leq \mathrm{Va}_{\mathrm{a}} \leq-0.77 \mathrm{~V} \mathrm{DC} \\
& \\
& \text { AFC - Output Pin } \mathrm{D}(-12 \mathrm{~V} \text { DC Ref.) } \\
& \text { Write }+0.65 \leq \mathrm{V}_{\mathrm{d}} \leq+0.89 \mathrm{~V} \mathrm{DC} \\
& \text { Read }+1.57 \leq \mathrm{V}_{\mathrm{d}} \leq+1.87 \mathrm{~V} \text { DC }
\end{aligned}
$$

These measurements must be made without AC signal on the
arnplifier system using a $20,000 \mathrm{ohm} /$ volt meter.
8.4.2 AC Measurements

AFC - Input Pin B
Write 8.35 V PP $\leq \mathrm{V}_{\mathrm{b}} \leq 9.25 \mathrm{VPP}$
AFC - Output Pin F (-12 V DC Ref.)
Write 7.05 VP $\leq \mathrm{V}_{\mathrm{f}} \leq 8.81 \mathrm{VP}$ (Average base to peak)
AFC - Output Pin D (-12 V DC Ref.)
Write 5. $74 \mathrm{VP} \leq \mathrm{V}_{\mathrm{d}} \leq 7.70 \mathrm{VP}$ (Average base to peak)
FC -- Output Pin G (-12 V DC Ref.)
The following must hold with the same input as previously
applied.

6.9 us $\leq \mathrm{T}_{\mathrm{r}} \leq 8.6 \mathrm{us}$ $+1.20 \mathrm{VDC} \leq \mathrm{V}_{\mathrm{on}} \leq+1.80 \mathrm{VDC}$
$+0.4 \mathrm{VDC} \leq \mathrm{V}_{\text {off }} \leq+0.9$

### 8.4.2 AC Measurements (Continued) <br> FD -- Output Pin D (Ground Ref.)

The following must hold with the same input as previously applied.


Sensing Delay
0.3 us $\leq \mathrm{T}_{\mathrm{p}} \leq 0.8$ usec.

The time from the most negative portion of the input peak at Pin B on the AFC - to the output slope of Pin D of the FD ... follows:

$$
3.75 \mathrm{us} \leq \mathrm{s}_{\mathrm{d}} \leq 4.25 \mathrm{us}
$$

### 8.5 Integrator (Level Measurements)

A. With reference to ground, measure $-12 \mathrm{~V}+.5 \mathrm{~V}$ at pin 06 B 4 H 28 D with Channel in Reset status.
B. Measure $-6 \mathrm{~V}+.3 \mathrm{~V}$ at 06 B 4 H 28 D while reading a 729 IV tape unit.
C. Measure $-8 \mathrm{~V}+.3 \mathrm{~V}$ at 06 B 4 H 28 D while reading a 729 II tape unit.
9. TAPE ADAPTER UNIT (90K. ) FOR THE 7607 MODEL IL AND IV DATA

## CHANNELS

### 9.1 Oscillators

The Oscillators listed provide the drive pulses to operate the TAU clocks through a range of character rates from 15 KC to 90 KC and provide motion control for 75 IPS and 112.5 IPS tape units - all crystal type are $\pm 1.0 \%$ gated are $\pm 5 \%$.

| Oscillator | Type | Tape Unit | Density Control |  |
| :---: | :---: | :---: | :---: | :---: |
| 6.67 KC | XTAL | 729 II, V |  | DC MS Control |
| 10.00 KC | XTAL | 729 IV, VI |  | DC MS Control |
| 240.00 KC | XTAL | 729 II, V | B Lo, C Lo | WC \& DC us Control 200 BPI |
| 240.00 KC | Gated | 729 II, V | B Lo, C Lo | RC 200 BPI |
| 360.00 KC | XTAL | 729 IV | B Lo, C Lo | WC \& DC us Control 200 BPI |
| 360.00 KC | Gated | 729 IV | B Lo, C Lo | RC 200 BPI |
| 667.00 KC | XTAL | 729 II, V | A Lo, C Hi | WC \& DC us Control 556 BPI |
| 667.00 KC | Gated | 729 II, V | A Lo, C Hi | RC 556 BPI |
| 960.00 KC | XTAL | 729 V | A $\mathrm{Hi}, \mathrm{BHi}$ | WC \& DC us Control 800 BPI |
| 1000.00 KC | Gated | 729 V | A $\mathrm{Hi}, \mathrm{BHi}$ | RC 800 BPI |
|  |  | 729 IV, VI | A Lo, C Hi | RC 556 BPI |
| 1000.00 KC | XTAL | 729 IV, VI | A Lo, C Hi | WC \& DC us Control 556 BPI |
| 1440.00 KC | XTAL | 729 VI | A $\mathrm{Hi}, \mathrm{BHi}$ | WC \& DC us Control 800 BPI |
| 1600.00 KC | Gated | 729 VI | A Hi, B Hi | RC 800 BPI |
| 360.00 KC | Gated |  | A, B, C | RD Check Character |

### 9.2 Tape Adapter Clocks

9.2.1 Read Clock (RD)

The Read Clock consists of 4 Binary Triggers. The RC 1
trigger is a high speed drift circuit capable of operating with a 2
MC drive pulse. A 400 mus pulse is generated on the fall of RC 1 and this drives the remaining triggers in Binary fashion. The

### 9.2.1 Read Clock (RD) (Continued)

output of RCl is used as a sample pulse for the read clock gating.
The limitations for these gates follows:

|  |  | BPI | 556 | PI | 800 | BPI |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 729 II-V | 729 IV-VI | 729 II-V | 729 IV-VI | 729V | 72.9 VI |
| RC2 | 8.4 | 5.8 us | 3.2 | 2.2 us | 2.2 | 1.6 us |
| RC4* | 16.9 | 11.3 us | 6.2 | 4.2 us | 4.2 | 2.7 us |
| RC5** | ---- | ------- | ---- | ------ | 5.2 | --- |
| RC6*** | 25.2 | 16.9 us | 9.2 | 6.3 us | 6.3 | 4.0 us |
| RC7 | 29.4 | 19.7 us | 10.8 | 7.5 us | 7.3 | 4.7 us |
| RC7 dly | 29.9 | 20.3 us | 11.3 | 8.0 us | 8.0 | 5.2 us |
| RC7 Reset | 30.3 | 20.7 us | 11.6 | 8.3 us | 8.3 | 5.6 us |
| RC Reset (RD) | 30.3 | 20.7 us | 11.7 | 8.3 us | 8.3 | 5.6 us |
| RC Reset (WR) ***** | 41.8 | 28.2 us | 15.5 | 10.5 us | 10.5 | 5.6 us |
| * Skew gate set pulse for $200 \mathrm{BPI} \& 556$ BPI <br> ** Skew gate set pulse for 800 BPI for 729 V <br> *** Skew gate set pulse for 800 BPI for 729 VI ***** Skew gate reset pulse |  |  |  |  |  |  |

All timings are $\pm 5 \%$ with reference to +N start read clock.

### 9.2.2 Write Clock (WC)

The Write Clock is a 16 step Binary Counter consisting of
4 Binary Triggers. The WC 1 trigger is a high speed drift circuit capable of drive frequencies to 2 MC . The turn off of WC 1 generates a 400 mus pulse which drives the remaining triggers. The write clock gates are sampled with the output of WC 1. The limitations for these gates follow:
9.2.2 Write Clock (WC) (Continued)


All write clock timings are $\pm 1,0 \%$ to reference when measured at similar logic points.

### 9.3 Delay Counter (DC)

The Delay Counter consists of 9 Binary Operated Triggers. The DC 1 trigger is a high speed drift circuit capable of operating with drive frequencies to 2 MC . The fall of this trigger generates a 400 mus pulse which drives the next four triggers in binary fashion. The output of DC 16 drives the next binary stage direct without DC 1 drive pulse reference. This mode of operation continues to the DC 256 trigger. The DC 1 output serves as the sample pulse for delay counter gating. The limitations of these gates follow:
9.3.1 Microsecond Control*

|  | $729 \mathrm{II}, \mathrm{V}$ | $729 \mathrm{IV}, \mathrm{VI}$ | $729 \mathrm{II}, \mathrm{V}$ | $729 \mathrm{IV}, \mathrm{VI}$ | 729 V | 729 VI |
| :--- | :---: | :---: | ---: | ---: | ---: | ---: |
| RDD36 | 150.4 | 100 us | 54.6 | 36.6 us | 37.5 | 25.6 us |
| RDD88 | 366.0 | 244 us | 132.0 | 88.6 us | 91.5 | 61.2 us |
| RDD128 | 532.0 | 355 us | 192.6 | 128.6 us | 133.0 | 89.6 us |
| RDD136 | 566.0 | 377 us | 204.0 | 136.6 us | 142.0 | 95.1 us |
| RDD144 | 600.0 | 400 us | 216.0 | 144.6 us | 150.0 | 100.7 us |
| WDD60 | 250.0 | 166 us | 90.6 | $60.6 . \mathrm{us}$ | 63.0 | 42.3 us |

### 9.3.1 Microsecond Control* (Continued)

* Delay counter timings are in reference to turn on of us
control. All Delay counter microsecond timings are $\pm 1 \%$, except RDD36 which is $\pm 2 \%$.


### 9.3.2 Read Clock Gates*

200 BPI
$729 \mathrm{II}, \mathrm{V}$
$729 \mathrm{IV}, \mathrm{VI}$$\quad \begin{aligned} & 33.3 \text { to } 41.6 \mathrm{us} \\ & 22.2 \text { to } 27.8 \text { us }\end{aligned}$

729 II, V
729 IV, VI
800 BPI
729 V
8.12 to 10.4 us

729 VI
5.6 to 7.0 us

* To measure Read Clock Gate cycle write one word records with bits 1 and 2 in first character and bit 1 in following characters. Rewind and remove Hi clip card (06B4G28) and cycle read. Measure timings during Read. Read clock gate tolerance is $\pm 6 \%$.
9.3.3 MilliSecond Control

|  | $729 \mathrm{II}, \mathrm{V}$ | $729 \mathrm{IV}, \mathrm{VI}$ | Tolerance |
| :--- | :---: | :---: | :---: |
|  | 2.4 ms |  |  |
| RDD-16 | $5.7 \mathrm{~ms} \pm 1 \%$ | 2.2 ms | $\pm 3 \%$ |
| RDD-22+RDD-38 | 9.6 ms | $\pm 2 \%$ |  |
| RDD-64 | 22.5 ms | 15.2 ms | $\pm 1 \%$ |
| RDD-152 | 3.0 ms | 2.0 ms | $\pm 1 \%$ |
| WDD-20 |  | $\pm 3 \%$ |  |

### 9.3.3 MilliSe cond Control (Continued)

| RD-30 | 4.5 ms | 3.0 ms | $\pm 2 \%$ |
| :--- | ---: | ---: | ---: |
| RD-160 | 24.0 ms | 16.0 ms | $\pm 1 \%$ |
| WD-52 | 7.8 ms | 5.2 ms | $\pm 1 \%$ |
| WD-80 | 12.0 ms | 8.0 ms | $\pm 1 \%$ |
| WD-320 | 48.0 ms | 32.0 ms | $\pm 1 \%$ |
| D-50 | 7.5 ms | 5.0 ms | $\pm 1 \%$ |
| D-96 | 14.4 ms | 9.6 ms | $\pm 1 \%$ |
| D-160 | 24.0 ms | 16.0 ms | $\pm 1 \%$ |
| Backspace-180 | 27.0 ms | 18.0 ms | $\pm 1 \%$ |
| St. Read Condition -32 | 4.8 ms | 3.2 ms | $\pm 2 \%$ |

All Delay Counter Millisecond Timings are measured in respect to the rise of MilliSecond Control Gate, except Backspace Timings which are referenced to the rise of RDD.

### 9.4 Final Amplifier

All measurements are to be made at 800 BPI . The basic TAU Final Amplifier consists of three SMS cards. Each card serves a specific function in the chain of events between the read bus signal and the ultimate -N current mode pulse which sets the read register. To the basic final amplifier, two more cards for each track are added to form the B Channel of the Dual Channel System. The sensitivity of the A and B Channels is independently controlled by four common clipping level cards. The tolerance of these acceptance levels and the respective card outputs follows:
9.4.1 D.C. Measurements

ARA - Input Pin A (7 common - 12 V DC Ref.)
Write - $1.74 \leq \mathrm{V}_{\mathrm{a}} \leq-2.17 \mathrm{~V}$ DC
Read $-0.40 \leq \mathrm{V}_{\mathrm{a}} \leq-0.77 \mathrm{~V} \mathrm{DC}$

### 9.4.1 D.C. Measurements (Continued)

ARA - Output Pin D (-12 V DC Ref.) Write $+0.65 \leq \mathrm{V}_{\mathrm{d}} \leq+0.89 \mathrm{~V}$ DC
Read $+1.57 \leq \mathrm{V}_{\mathrm{d}} \leq+1.87 \mathrm{~V} \mathrm{DC}$
These measurements must be made without AC signal on the amplifier system using a $20,000 \mathrm{ohm} /$ volt meter as a minimum.

### 9.4.2 Acceptance Levels

The minimum peak to peak read buss signal to insure an output from the Final Amplifier for each channel with the above DC voltage is as follows:

Channel B
Write 1.37 V
Read . 595 V
Channel A
Write 1.86 V
Read 1.63 V
9.4.3 AC Measurements

ARA - Input Pin B
Write $9.5 \mathrm{~V} \mathrm{PP} \leq \mathrm{V}_{\mathrm{b}} \leq 10.5 \mathrm{VPP}$
ARA - Output Pin F (-12 V DC Ref.)
Write 7.33 VP $\leq \mathrm{V}_{\mathrm{f}} \leq 8.76 \mathrm{VP}$ (Average base to peak) Output Pin D (-12 V DC Ref.)
Write 6.44 VP $\leq \mathrm{V}_{\mathrm{d}} \leq 8.11 \mathrm{VP}$ (Average base to peak)
FC - Output Pin G (-12 V DC Ref.)
The following must hold with the same input as previously
applied.

### 9.4.3 AC Measurements (Continued)


$+1.20 \mathrm{~V} \mathrm{DC} \leq \mathrm{V}_{\mathrm{on}} \leq+1.80 \mathrm{~V} \mathrm{DC}$
$+0.4 \mathrm{VDC} \leq \mathrm{V}_{\mathrm{off}} \leq+0.9 \mathrm{~V} \mathrm{DC}$
FD - Output Pin D (Ground Reference)
The following must hold with the same input as previously applied.


$$
0.3 \mathrm{us} \leq \mathrm{T}_{\mathrm{p}} \leq 0.6 \mathrm{us}
$$

9.4.4 Time Asymmetry
A. TAU Final Amplifier Symmetry alignment for 90 KP

1. Measure the asymmetry in track 1 in the usual manner as follows:
a. Write all one's at 800 BPI
9.1.4 Time Asymmetry (Continued)
b. Connect scope to TAU Read Register Atrigger output (pin G)c. Set sweep for five microsecond per cm
d. Sync negative internal
e. With proper sync, asymmetry results in thesecond negative slope appearing double
f. Turn on 5X multiplier
g. Move horizontal position to view the doublesecond slope
h. Measure the time difference between the doublepulses.
2. Invert the track 1 read signal by adding the last twopre-amp stages of track 2 as follows:a. Connect track 2 read delay line jumper to track1 output (LO1H)
b. Interchange track 1 and track 2 read bus coax
(EC 55a and EC 55b)
3. Measure the track 1 inverted signal asymmetry asin Step 1.
a. If both readings are zero, both tape and finalamp are properly set, go to Step 9.

### 9.4.4 Time Asymmetry (Continued)

b. If the two readings are different, (both tape and final amp have asymmetry) go to Step 4.
c. If the two readings are the same (either tape or final asymmetry is zero).

1. Adjust the tape unit track l asymmetry pot for zero asymmetry.
2. Restore the normal signal by restoring track 1 and 2 read bus coaxes to their proper respective places (EC 55a and EC 55b) and measuxe asymmetry.
3. If zero, go to Step 9.
4. If the two readings are different, go to Step 4.
5. Using the condition (normal or inverted signal) that produced the laxgest asymmetry, decrease the amount by one-half the difference (between normal and inverted) by adjusting the potentiometer in the track 1 final amplifier ARA card.
6. Set up the other condition and measure asymmetry.
7. Repeat until the inverted signal asymmetry equals the normal signal asymmetry, this asymmetry should then be due entirely to the tape unit.
8. Restore the read bus coaxes to normal.

### 9.4.4 Time Asymmetry (Continued)

8. Adjust the tape unit track 1 asymmetry to zero.
9. Use the cor rected tape unit track l signal to adjust the final amplifiers as follows:
a. With track 2 read delay line jumper still connected to track 1 output, adjust track 2 final amplifier potentiometer for zero asymmetry, as observed at the track 2 TAU Read Register A output.
b. Successively connect the remaining read delay line jumpers to track 1 output (L01H) and adjust the respective final amplifier potentiometer.

### 9.4.5 Sensing Asymmetry

The time difference between successive negative slopes on Pin G of the Read Register A Trigger must not exceed 0.25 usec. with a symmetrical input wave.

$\mathrm{T}_{\mathrm{a} 1}-\mathrm{T}_{\mathrm{a} 2} \leq 0.25 \mathrm{usec}$.

### 9.4.6 Sensing Skew

The time difference between the setting of all Read Register A triggers with a common input to the read buss must not exceed 0.25 usec.

### 9.5 Integrator Level Measurements

A. With reference to ground, measure $-12 \mathrm{~V} \pm 5 \mathrm{~V}$ at pin 06B4H28D with channel in reset status.
B. Measure $-6.0 \mathrm{~V} \pm .3 \mathrm{~V}$ at 06 B 4 H 28 D while reading a 729 II or V Tape Transport.
C. Measure nominal -2.4 V (-2.38 to -2.6) at 06B4H28D while reading a 729 IV or VI Tape Transport.
10. DIAGNOSTIC TESTING
10.1 List of Diagnostics

| Identification | Description | No. of Cards |
| :---: | :---: | :---: |
| 9M10A | Instruction Ctr. Test | One Card |
| 9M05B | Floating Point Diagnostic | 000-192 |
| 9M51A \& 9M56A | Mainframe Diag. and Reliability Program | $\begin{aligned} & 0000-1352 \\ & 000-633 \end{aligned}$ |
| 9P51A | On Line Printer Diag, and Reliability Test | 000-250 |
| 9R51A | Cd. Pu. Test Using Special Ripple and Random Numbers | 000-114 |
| 9 C 51 A | Cd. Rd. Timing and Reliability Test Mod. 250 | 000-419 |
| $\begin{aligned} & 9 \mathrm{~S} 04 \mathrm{H} \\ & \& \\ & 9 \mathrm{~S} 04 \mathrm{~L} \end{aligned}$ | Half Select Beat Test - 738 Core Str. | $\begin{aligned} & 00-47 \\ & 00-49 \end{aligned}$ |
|  | Zero - One Test - 738 Core Str. | $00-43$ <br> 00-45 |
| $\begin{gathered} 9 \mathrm{~S} 54 \mathrm{~A}-\mathrm{H} \\ \& \\ 9 \mathrm{~S} 54 \mathrm{~A}-\mathrm{L} \end{gathered}$ | Comprehensive Memory Test for the 7302 AirCooled Memory | 00-99 |
| 9T51B | Tape Frame and Channel Test - 729 LI, IV | 000-374 |
| 9T55B | Tape Inter-Record Gap and Creep Test 729 II, IV | 000-190; |
| 9T53A | 729 Multi-Channel Test | 000-161 |
| 9T54A | 729 Tape Frame Inter changeability Test | 000-076 |
| 9T56A | Data Channel Trap | 000-201 |
| 9T58A | Data Channel Reg. and Multi Dr. Tape Tests | 000-363 |


| Identification | Description | No. of Cards |
| :---: | :---: | :---: |
| 9T60B | Dual Density Feature Diag. Prog. | 000-219 |
| 9B51A | Cd. Mach. Data Transmission and Channel Ctr'l Test | 000-157 |
| 9B53B | Worst Case B Time Test | 000-144 |
| TR03A | Tape Reliability Test | 000-139 |
| 9Y51A | Six Channel Test with Cd. Machines on A C or E | 000-319 |
| 9Y52B | Concurrent I/O Oper. and Main Frame Exec. Diag | 0000-1412 |
| XCOMB | Compatibility Diagnostic Programs | 000-230 |
| 10.2 | Special Diagnostics |  |
| Identification | Description | No. of Cards |
| DEPREX | Sense Sw. Interrogation and Diag, Prt. Subrouting | 001-032 |
| 9T61A | Tape Generation Program Cd. to Tape | 00-36 |
| 9CNPB | Consecutive Numbering Punch Test | 000-007 |
| 9FT9 | C. E. Fortran Test | 000-114 |
| 910CA | I/O Instruction Routine Modifications | None |
| 9LD01 \& 2A | Program Loader | None |
| 9PACC | Program Accounting Clock Test | 000-056 |
| 9ST9 | C. E. Sort Test | 000-013 |
| 9FTRA | Fortran Tracer Test | 00-05 |

### 10.3 Vibration Testing

A. Program

9M51

9S51L*
9T51
9B51

Area to be Vibrated
CPU I, II MULTIPLEXOR
MEMORY
DATA CHANNEL (Except Panels A1, A2, A4)
DATA CHANNEL, MOD. I or III (Panels Al, A2, A4) (Printer Section)
B. Procedure

1. With power down, ripple all voltage jumpers and repair any loose connections.
2. With power on and the above programs operating, vibrate all SMS cards lightly using a blank SMS Card.
3. Ripple all pins on panel wherecoaxis extremely dense. Ripple coax itself.
4. Using a soft faced plastic hammer, vibrate all tailgates.
5. Push tower in and out (TAILGATE).
6. Open and close each gate several times.
C. The specified diagnostics shall run error free, while each of the above mentioned steps except \#1 is being performed.

### 10.4 Marginal Voltage Requirements

Paragraphs 10.1 and 10.2 contain a list of those programs to be marginal tested. The latest level of these programs should be run error

## 10. 4 Marginal Voltage Requirements (Continued)

free as instructed in the program operating procedures in paragraphs 10.6 and 10.7. Any adjustments made during or after these tests will invalidate previous results for areas of the machine affected by the adjustments.
A. The $7100,7606,7607$ and 7302 (Oil Cooled) marginal voltages will be varied as follows: when performing bias tests.

$$
\begin{array}{rrr}
+6 \mathrm{M} & 5.5 \mathrm{~V} \text { Low } & 6.5 \mathrm{~V} \mathrm{High} \\
-12 \mathrm{M} & -11.0 \mathrm{~V} \text { Low } & -13.0 \mathrm{~V} \mathrm{High}
\end{array}
$$

B. The 7302A (Air Cooled) core storage

1. The +6 M bias limits do not apply to the 7302 A since the voltage is not present.
2. $-12 \mathrm{M}-10.0 \mathrm{~V}$ Low -14.0V High
10.5 Reliability Requirements

Paragraphs 10.1 and 10.2 contain a list of those programs to be run. The latest level of each of these programs must operate error free for the specified time with all power supply voltages at normal. Machine adjustments invalidate these tests in the maner specified in paragraph 10.4 . 10.6 Diagnostic Testing
10.6.1 9M10-Checks instruction counter operation
A. Bias Test - Vary voltages 7100,7302 , and 7606 simultaneously for one minute at each voltage limit.
B. Reliability Run - Run for 0.5 hours.
10.6.2 9M05-Further tests of floating point operations
A. Bias Test - Vary voltages on 7100,7606 , and 7302 simultaneously for 100 passes at each voltage limit.
B. Reliability Run

1. Run for 1 hour.
2. Run program with CP SET rotated $180^{\circ}$ each side of mid-point.
10.6.3 9M51 - Test arithmetic ope rations and establishes long time reliability requirements.
A. Bias Test - Vary voltages on 7100,7302 , and 7606 simultaneously and for each voltage limit:
3. Load with Sense Switch 6 down and run for 100 passes, the first pass shall include the long index test.
4. With Sense Switches 5 and 6 down, verify the series of 14 halts and enter key operations as defined by the program listing.
5. Continue with Sense Switches 5 and 6 down for 100 passes.
B. Run program with C.P. set rotated $180^{\circ}$ from mid-point.
C. Reliability Run
6. Change the program as instructed in the listing for reliability test purposes.
10.6.3 9M51 - Tests arithmetic operations ... (Continued)
7. Run program for 10 consecutive hours using long adder test for minimum of 2 hours and maximum of 5 hours.
8. With 9M51 loaded and running, place 2 channels (or one if only one is installed) in Manual Status and Continuous Storage Read Out. Run for 4 passes. 9M56 - Provides easy method of loading - CPU diagnostic
A. Bias Test - None required.
B. Reliability Run - None required.

### 10.6.4 9P51 - Test Printer

A. Bias Test - Successful completion of this test requires four successive successful passes at the four marginal limits. Location 4141 may be changed to HTR 31 in order to change the bias voltage between passes. For each voltage limit, and each 716 printer run one pass varying the marginal voltages on the $7100,7302,7606$ and the 7607 I or III simultaneously.
B. Reliability Run - None required.
10.6.5 9R51 - Tests Card Recorder
A. Bias Test- None required.
B. Reliability Run - Run with Sense Switch 5 up.
10.6.5 9R51 - Test Card Recorder (Continued)

1. Two passes with right corner cut cards.
2. Two passes with left corner cut cards.
10.6.6 9C51 - Tests the operation of the Card Reader
A. Bias Test - None required.
B. Reliability Run - One pass with Sense Switch 5 up using

Entry keys 1 through 6 to check timings.

1. Card Cycle $235-245 \mathrm{~ms}$
2. Select to RCH

70 - 80 ms
3. Between Words
$360-440$ us
4. Between Rows 10.6 - 11.6 ms
5. Between EOR and 9L $95-102 \mathrm{~ms}$
6. Between 12R and EOR
7. Between 12R and Select 38 - 45 ms
8. One pass with Sense Switch 5 down
10.6.7 9S04L - Insures that half selected me mory cores will retain their original state while a read in or read out is performed on other cores. Tests addresses 00000 to 75777.
A. Bias Test - Vary voltages on 7100,7302 , and 7606
simultaneously for 1 minute at each voltage limit.
B. Reliability Run - None required.

9S04H - Same as above, except tests address 02000 to 77777.
Reliability Run and Bias Test - Same as steps A \& B.
10.6.8 9S05L - Memory Tests for noise generation on sense lines and checks ability to store ones and zeros. Tests addresses 00000 to 75777.
10.6.8 9S05L - Memory Tests for noise ... (Continued)
A. Bias Test - Vary voltages on 7100,7302 , and 7606 simultaneously for one minute at each voltage limit.
B. Reliability Run - None required.

9S05H - Same as above, except tests addresses 02000 to
77777. Reliability Run and Bias test - Same as steps A \& B.
10.6.9 9S54L - Tests operation of the memory area (air cooled)
A. Bias Test -

1. Run one pass at each voltage limit varying the 7100 , 7302A, 7606 simultaneously.
2. With all logic voltages normal and the memory driver voltages avried separately by 5\% above and below their operating points, run one pass at each driver voltage limit.
B. Reliability Run - Run for 1 hour.

9S54H - Same as above.
10.6.10 9T51-A reliability test of the channel tape circuits and each of the tape drives on the system.
A. Bias Test - two passes for each voltage limit on each channel. Use Model IV at 556 BPI or VI Tape Transports at 800 BPI if available. Vary voltages on 7100,7302 , 7606 and 7607 simultaneously.
10.6.10 9T51-A reliability test of ... (Continued)
B. Reliability Run

1. For each tape drive - run 15 minutes at 200 BPI .
2. Manually set at high density.
3. For each tape drive run 45 minutes at 556 BPI for Model II and IV and 800 BPI for Model V and VI.
4. Execute unit selects 0 thru 9 on each channel. One pass is sufficient for any one unit selection.
5. Reliability runs shall be spread equally across all the channels of the system and between tape drive banks on each channel. One reliability run must be made on each channel and Tape Drive Bank.
10.6.11 9T55-Tests Tape drive motion controls
A. Bias Test - None required.
B. Reliability Run - One pass on each drive with no single line error print outs. Model II, IV, V and VI Tape Transports will be tested at 556 and 200 BPI.
10.6.12 9T53-Tests multi-channel data flow with tape operation.
A. Requirements - At least one tape drive on each available channel Run at 556 BPI for the Model II and IV's and 800 BPI for the Model V and VI's.
B. Bias Test - two passes for each voltage limit. Use Model IV or VI Tape Transports if available. Vary
10.6.12 9T53 - Tests multi-channel ... (Continued)
voltages on the 7100, 7302, 7606 and all 7607's simultaneously.
C. Reliability Run -
6. Run for one hour using all channels
7. Five minute run for each tape drive not used in the one hour run.
8. If Sense Switch 5 is up and LOC 1016 is changed to TRA 35, each tape drive will rewind after each pass.
10.6.13 9T54-Tests tape interchangeability within the system.
A. Bias Test - None required.
B. Reliability Run - All operations will be performed at 556 BPI for the Model II and IV's and 800 BPI for the Model V and VI's. Write once with each Tape Drive in the system, read each of the written tapes on three pther tape drives. The interchange will be:
9. Between all channels.
10. Between both banks on each channel.
11. Among all Tape Drives in the system.
10.6.14.9T56-Check data channel trap operation.
A. Bias Test - Nary voltages on $7100,7302,7606$ and all 7607's simultaneously and run two passes at each
10.6.14 9T56-Check data channel... (Continued)

Marginal Voltage limit. Use 729 IV at 556 BPI or VI
Tape Transports at 800 BPI if available.

1. Manually TRA to 00141 to repeat halt tests after first pass.
B. Reliability Run
2. Run for one hour using all channels on system, using Model II and IV Tape Transports at 556 BPI or Model V and VI Tape Transports at 800 BPI .
3. Run one pass on one channel while performing continuous storage read out in manual on the other channel.
4. Error points which can be expected when running $9 T 56$ with other channels taking CSRO cycles are listed as follows:

LOC

| 00167 | T COA* | 00170 |
| :---: | :---: | :---: |
| 00216 | T COA* | 00167 |
| 00264 |  | 00217 |
|  | T COA* | 00216 |
| 00314 |  | 00265 |
|  | T COA* | 00264 |
|  |  | 02315 |
|  |  | 02314 |

10.6.15 9T58 - Data Channel Register and Multiple Tape Drive Test
A. Bias Test - Run two minutes at each marginal voltage limit on each channel at 556 BPI - 200 BPI. Vary voltages
10.6.159T58 - Data Channel Register ... (Continued)
on 7100, 7302, 7606 and all 7607's simultaneously.
B. Reliability Run - Determine running time for each channel by multiplying the number of drives by 3 minutes. Operate Model II, IV, V and VI Tape Transports at 556200 BPI.
10.6.16 9T60 - Multiple Density Feature Test
A. Bias Test - Vary voltages on the 7100, 7302, 7606, and 7607's simultaneously.

1. Run two passes at each marginal voltage limit on each 7607 Model I or II Data Channel.
2. Run one pass for each density switch setting, (A, B, and C) at each marginal voltage limit, on each 7607 Model III or IV Data Channel. 729 Model V or VI Tape Transport must be used.
B. Reliability Run
3. Run error free on each Model II and IV Tape Transport for 5 minutes at 556-200 BPI.
4. Run error free on each Model V and VI Tape Transport for 5 minutes per density switch setting for the 7607 Model III and IV Data Channels.
(a) $800-556 \mathrm{BPI}$
(b) $800-200 \mathrm{BPI}$
(c) $556-200 \mathrm{BPI}$
10.6.179B51-Tests the operation of all the control word indicators on all types of I/O operation and indirect addressing of control words.
A. Bias Test - Vary voltages on 7100,7606 , and 7607 simultaneously and at each voltage limit use the Reader, Printer and Punch.
5. Load with Sense Switch 6 down.
6. While Section I of Program is running ready the Card Reader with the pre-punched deck for Section II.
7. Put Sense Switch 5 down and repeat the program. Read the punched decks at normal voltage after successful bias runs.
B. Reliability Run - Two passes using Reader and Printer only (no Punch).
10.6.18 9B53-Tests multi-channel operation checking for worst case B time and priority.
A. Bias Test - Vary voltages on $7100,7302,7606$ and 7607 simultaneously. For each voltage limit run two passes on each channel of the system using 729 IV's at 556 BPI or 729 VI's at 800 BPI , if available.
B. Reliability Run - Use one tape drive on each channel for a period of time equal to the number of channels on the system times 15 minutes.
10.6.18 9B53 - Tests multi-channel operation ... (Continued)
8. 556 BPI for Model II and IV
9. 800 BPI for Model V and VI
10.6.19 9TR03 - Tape Reliability
A. Bias Test - None required.
B. Reliability Run
10. Run one full reel pass wirte and then read on each Tape Transport at the following density.
a) 15 write redundancies
b) 8 temporary read redundancies
c) no permanent read errors (99 rereads and still in error)
10.6.20 9Y5l - General Systems Operation Test
A. Bias Test - None required.
B. Reliability Run - Run for a period of time equal to the product of the number of channels installed times ten minutes. Set Sénse Switch 5 down.
10.6.21 9Y52-Tests the concurrent operations of I/O and arithmetic sections.
A. Bias Test - Repeat reliability runs at each of the following voltage limits, biasing all frames in the system - 7100, 7607, 7606 and 7302.
10.6.21 9Y52-Tests the concurrent operations ... (Continued)
B. Reliability Run
11. Run one pass on all channels at the highest density, using Model IV or VI Tape Transports if available.
12. Run one pass using all printers and at the lowest density Model II or V Tape Transports if available.
10.6.22 XCOM - Tests the compatibility with 704 type programming.
A. Bias Test - Vary voltages on 7100,7302 , and 7606 simultaneously.
16K Mode 100 Passes *24K Mode 100 Passes

NOTE: Setting Sense switch 5 down stops the program for setting mode.

16K Operation - Set to 16 K with Sign key up * 24 K Operation - Set to 24 K with Sign key down
B. Reliability Run

16K Mode - $1 / 2$ hour *24K Mode - $1 / 2$ hour
10.7 Special Diagnostic Testing
10.7.1 9FT9-CE FORTRAN TEST
A. Bias Test - None required.
B. Reliability Run - Run to successful completion at 800 BPI.
10.7.2 9ST9-CE IB9 Sort Test
A. Bias Test - None required.

### 10.7.2 9ST9-CE IB9 Sort Test (Continued)

B. Reliability Run - One complete sort to a successful completion at 800 BPI .

Other special diagnostics tests may be obtained by contacting:

Plant Custome $r$ Engineering Department 910
IBM Corporation
Poughkeepsie, N. Y.


[^0]:    $2 \varepsilon-\varepsilon$

[^1]:    $\stackrel{\omega}{\omega}$

[^2]:    * Allowable Deviation $\pm 2 \%$

