OEM PRODUCT DESIGN GUIDE

NVIDIA Jetson Xavier

Abstract

This document contains recommendations and guidelines for Engineers to follow to create a product that is optimized to achieve the best performance from the common interfaces supported by the NVIDIA® Jetson Xavier™ System-on-Module (SOM).

Document Change History

Date	Description
August 29, 2018	Initial release

Table of Contents

1.0 INTRODUCTION

1.1 References

Refer to the documents or models listed in Table 1 for more information. Use the latest revision of all documents at all times.

Table 1. List of Related Documents

Document
Jetson Xavier Module Data Sheet
Xavier Series Processors Technical Reference Manual
Jetson Xavier Developer Kit Carrier Board Specification
Jetson Xavier Module Pinmux
Jetson Xavier Thermal Design Guide
Jetson Xavier Developer Kit Carrier Board Design Files
Jetson Xavier Developer Kit Carrier Board BOM
Jetson Xavier Supported Component List

1.2 Abbreviations and Definitions

Table 2 lists abbreviations that may be used throughout this document and their definitions.

Table 2. Abbreviations and Definitions

Abbreviation	Definition
CEC	Consumer Electronic Control
CAN	Controller Area Network
DP	Display Port
eDP	Embedded Display Port
eMMC	Embedded MMC
HDMI	High Definition Multimedia Interface
I2C	Inter IC
I2S	Inter IC Sound Interface
LDO	Low Dropout (voltage regulator)
LPDDR4x	Low Power Double Data Rate DRAM, Fourth-generation
PCIe (PEX)	Peripheral Component Interconnect Express interface
PCM	Pulse Code Modulation
PHY	Physical Layer
PMIC	Power Management IC
RTC	Real Time Clock
SDIO	Secure Digital I/O Interface
SLVS	Scalable Low Voltage Signaling
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver-Transmitter
UFS	Universal Flash Storage
USB	Universal Serial Bus

2.0 JETSON XAVIER

2.1 Overview

Jetson Xavier resides at the center of the embedded system solution and includes:

Power (PMIC/Regulators, etc.)	DRAM (LPDDR4x)	eMMC
Power & Voltage Monitors	Thermal Sensor	

In addition, a range of interfaces are available at the main connector for use on the carrier board as shown in the following table.

Table 3. Jetson Xavier Interfaces

Catagory	Function		Catagory	Function
USB	USB 2.0 (x4)		**Audio**	I2S (x4), control & clock
	USB 3.1 (Up to x3)			Digital Mic & Speaker IFs
PCIe	Control (x5)		**CAN**	x2
	5 root ports		**I2C**	x7
Camera	CSI (6x2 or 4x4) D-PHY & C-PHY		**UART**	x4
Display	HDMI (up to x3) see note		**SPI**	x3
	DP (up to x3) see note		**Fan**	PWM & TACH
	HPD x3, CEC x1, DP_AUX/DDC x3		**Debug**	JTAG & UART
LAN	Gigabit Ethernet RGMII I/F		**System**	Power control, Reset, Alerts
SD Card	SD card or SDIO		**Power**	Main Inputs (HV & MV)

Note: HDMI & DP share the same pins. See the Display chapter for details.

Figure 1. System Block Diagram

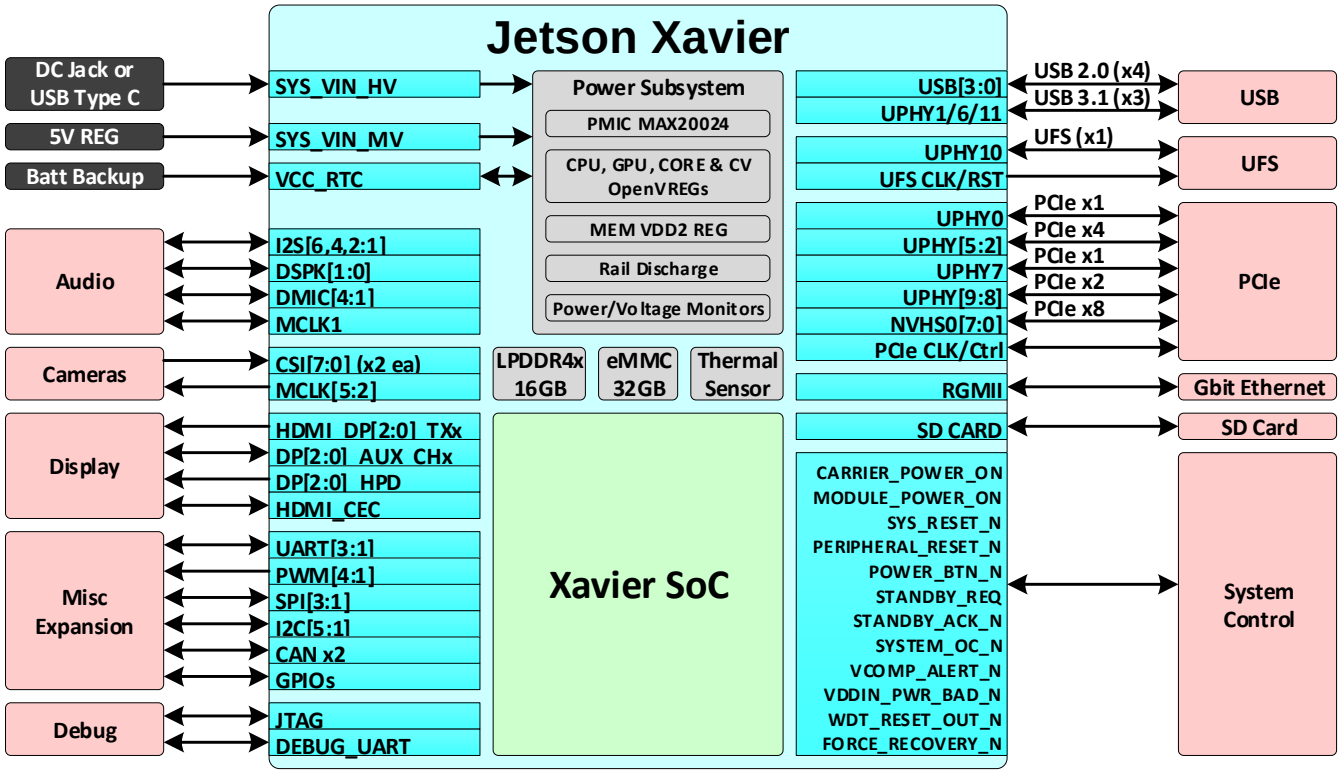


Table 4. Jetson Xavier Connector Pin Out Matrix (Part 1: Columns A-F)

	A	B	C	D	E	F
01			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV
02			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV
03	PRSNT0	SYS_VIN_HV	GND	SYS_VIN_HV	GND	SYS_VIN_HV
04	SDCARD_D2	GND	RGMII_RD0	GND	I2S2_FS	GND
05	SDCARD_CMD	RGMII_TXC	RGMII_RXC	RGMII_RX_CTL	RGMII_RD3	I2S2_DOUT
06	UFS0_REF_CLK	SDCARD_CLK	UFS0_RST_N	SDCARD_D3	RGMII_SMA_MDC	I2S2_DIN
07	GPIO29	GND	I2S1_SDOUT	GND	RGMII_SMA_MDIO	GND
08	PEX_WAKE_N	GPIO11	PEX_L5_CLKREQ_N	I2S1_FS	SDCARD_D0	SDCARD_D1
09	GND	PEX_L1_RST_N	GND	PEX_L1_CLKREQ_N	GND	GPIO16
10	USB2_P	RSVD	USB1_N	PEX_L0_RST_N	GPIO12	GPIO15
11	USB2_N	GND	USB1_P	GND	PEX_L0_CLKREQ_N	GND
12	GND	UPHY_RX10_P	GND	UPHY_RX11_P	GND	USB0_P
13	GND	UPHY_RX10_N	GND	UPHY_RX11_N	GND	USB0_N
14	UPHY_RX8_N	GND	UPHY_RX9_N	GND	PEX_CLK0_N	GND
15	UPHY_RX8_P	GND	UPHY_RX9_P	GND	PEX_CLK0_P	GND
16	GND	UPHY_RX6_P	GND	UPHY_RX7_P	GND	PEX_CLK1_P
17	GND	UPHY_RX6_N	GND	UPHY_RX7_N	GND	PEX_CLK1_N
18	UPHY_RX4_P	GND	UPHY_RX5_N	GND	RSVD	GND
19	UPHY_RX4_N	GND	UPHY_RX5_P	GND	RSVD	GND
20	GND	UPHY_RX2_N	GND	UPHY_RX3_P	GND	PEX_CLK3_P
21	GND	UPHY_RX2_P	GND	UPHY_RX3_N	GND	PEX_CLK3_N
22	UPHY_RX0_P	GND	UPHY_RX1_N	GND	PEX_CLK4_N	GND
23	UPHY_RX0_N	GND	UPHY_RX1_P	GND	PEX_CLK4_P	GND
24	GND	NVHS0_SLVS_RX1_N	GND	NVHS0_SLVS_RX0_P	GND	PEX_CLK5_P
25	GND	NVHS0_SLVS_RX1_P	GND	NVHS0_SLVS_RX0_N	GND	PEX_CLK5_N
26	NVHS0_SLVS_RX3_P	GND	NVHS0_SLVS_RX2_N	GND	UPHY_REFCLK1_N	GND
27	NVHS0_SLVS_RX3_N	GND	NVHS0_SLVS_RX2_P	GND	UPHY_REFCLK1_P	GND
28	GND	NVHS0_SLVS_RX5_N	GND	NVHS0_SLVS_RX4_P	GND	RSVD
29	GND	NVHS0_SLVS_RX5_P	GND	NVHS0_SLVS_RX4_N	GND	RSVD
30	NVHS0_SLVS_RX7_P	GND	NVHS0_SLVS_RX6_N	GND	NVHS0_SLVS_REFCLK0_P	GND
31	NVHS0_SLVS_RX7_N	GND	NVHS0_SLVS_RX6_P	GND	NVHS0_SLVS_REFCLK0_N	GND
32	GND	RSVD	GND	RSVD	GND	RSVD
33	GND	RSVD	GND	RSVD	GND	RSVD
34	RSVD	GND	RSVD	GND	RSVD	GND
35	RSVD	GND	RSVD	GND	RSVD	GND
36	GND	RSVD	GND	RSVD	GND	RSVD
37	GND	RSVD	GND	RSVD	GND	RSVD
38	RSVD	GND	RSVD	GND	CSI0_D1_N	GND
39	RSVD	GND	RSVD	GND	CSI0_D1_P	GND
40	GND	MID4	GND	MID3	GND	MID2
41	CSI2_D0_P	GND	CSI2_D1_N	GND	CSI0_D0_N	GND
42	CSI2_D0_N	CSI2_CLK_N	CSI2_D1_P	CSI5_D0_P	CSI0_D0_P	CSI0_CLK_N
43	GND	CSI2_CLK_P	GND	CSI5_D0_N	GND	CSI0_CLK_P
44	CSI7_D0_P	GND	CSI5_CLK_P	GND	CSI3_D0_N	GND
45	CSI7_D0_N	CSI7_CLK_P	CSI5_CLK_N	CSI5_D1_N	CSI3_D0_P	CSI3_CLK_N
46	GND	CSI7_CLK_N	GND	CSI5_D1_P	GND	CSI3_CLK_P
47	HDMI_DP1_TX0_P	GND	CSI7_D1_P	GND	CSI4_D1_P	GND
48	HDMI_DP1_TX0_N	HDMI_DP1_TX1_N	CSI7_D1_N	HDMI_DP1_TX2_N	CSI4_D1_N	CSI4_CLK_P
49	GND	HDMI_DP1_TX1_P	GND	HDMI_DP1_TX2_P	GND	CSI4_CLK_N
50	HDMI_DP2_TX2_N	GND	HDMI_DP2_TX3_N	GND	HDMI_DP1_TX3_P	GND
51	HDMI_DP2_TX2_P	HDMI_DP2_TX1_P	HDMI_DP2_TX3_P	HDMI_DP2_TX0_P	HDMI_DP1_TX3_N	DP0_AUX_CH_N
52	GND	HDMI_DP2_TX1_N	GND	HDMI_DP2_TX0_N	GND	DP0_AUX_CH_P
53	I2C5_CLK	GND	I2C5_DAT	GND	I2C3_DAT	I2C3_CLK
54	GPIO17	WDT_RESET_OUT_N	GPIO33	GPIO03	FAN_TACH	GPIO22
55	GPIO34	GPIO30	GPIO18	SPI1_MOSI	SPI1_CS0_N	SPI3_CLK
56	SPI1_MISO	SPI1_CS1_N	UART2_RX	SPI3_MISO	SPI3_CS1_N	GPIO36
57	UART2_CTS	GND	SPI3_CS0_N	GND	GND	GND
58	GPIO20	GPIO21	UART2_TX	JTAG_TDO	JTAG_TMS	CAN0_DIN
59	GPIO05	GPIO04	I2S3_SCLK	CAN0_DOUT	GPIO06	GPIO07
60	JTAG_TCK	JTAG_TDI	I2S3_FS	SPI2_CS0_N	I2C4_DAT	SPI2_MOSI
61	SYSTEM_OC_N	CAN1_DIN	GPIO09	I2C4_CLK	SPI2_CLK	VCOMP_ALERT_N
62	GPIO10	GPIO08	GND	SPI2_MISO	GND	GND
63	GND	SYS_VIN_HV	SYS_VIN_HV	GND	SYS_VIN_HV	SYS_VIN_HV
64			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV
65			SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV

Legend

Ground	Power	Reserved – Must be left unconnected unless otherwise directed.

Table 5. Jetson Xavier Connector Pin Out Matrix (Part 2: Columns G-L)

	G	H	J	K	L
01	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		
02	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		
03	GND	SYS_VIN_HV	GND	SYS_VIN_HV	GND
04	I2S2_CLK	GND	GPIO01	GND	UART4_RTS
05	RGMII_TD1	ENET_RST_N	ENET_INT	I2C1_CLK	UART4_TX
06	RGMII_TD3	RGMII_RD2	RGMII_TD0	RGMII_RD1	GPIO02
07	GPIO13	GND	RGMII_TD2	RGMII_TX_CTL	GND
08	PEX_L4_CLKREQ_N	I2S1_SDIN	GND	GND	I2C1_DAT
09	GND	MCLK01	PEX_L4_RST_N	PEX_L3_RST_N	GPIO28
10	USB3_N	PEX_L5_RST_N	PEX_L3_CLKREQ_N	RSVD	FORCE_RECOVERY_N
11	USB3_P	GND	RSVD	GND	STANDBY_REQ_N
12	GND	UPHY_TX11_P	GND	UPHY_TX10_N	GND
13	GND	UPHY_TX11_N	GND	UPHY_TX10_P	GND
14	UPHY_RX9_N	GND	UPHY_TX8_P	GND	I2S1_CLK
15	UPHY_RX9_P	GND	UPHY_TX8_N	GND	GPIO14
16	GND	UPHY_TX7_P	GND	UPHY_TX6_N	GND
17	GND	UPHY_TX7_N	GND	UPHY_TX6_P	GND
18	UPHY_TX5_N	GND	UPHY_TX4_P	GND	RSVD
19	UPHY_TX5_P	GND	UPHY_TX4_N	GND	RSVD
20	GND	UPHY_TX3_P	GND	UPHY_TX2_N	GND
21	GND	UPHY_TX3_N	GND	UPHY_TX2_P	GND
22	UPHY_TX1_N	GND	UPHY_TX0_P	GND	SYS_VIN_MV
23	UPHY_TX1_P	GND	UPHY_TX0_N	GND	SYS_VIN_MV
24	GND	NVHS0_TX0_P	GND	NVHS0_TX1_N	GND
25	GND	NVHS0_TX0_N	GND	NVHS0_TX1_P	GND
26	NVHS0_TX2_N	GND	NVHS0_TX3_P	GND	SYS_VIN_MV
27	NVHS0_TX2_P	GND	NVHS0_TX3_N	GND	SYS_VIN_MV
28	GND	NVHS0_TX4_P	GND	NVHS0_TX5_N	GND
29	GND	NVHS0_TX4_N	GND	NVHS0_TX5_P	GND
30	NVHS0_TX6_N	GND	NVHS0_TX7_P	GND	SYS_VIN_MV
31	NVHS0_TX6_P	GND	NVHS0_TX7_N	GND	SYS_VIN_MV
32	GND	RSVD	GND	RSVD	GND
33	GND	RSVD	GND	RSVD	GND
34	RSVD	GND	RSVD	GND	SYS_VIN_MV
35	RSVD	GND	RSVD	GND	SYS_VIN_MV
36	GND	RSVD	GND	RSVD	GND
37	GND	RSVD	GND	RSVD	GND
38	RSVD	GND	RSVD	GND	SYS_VIN_MV
39	RSVD	GND	RSVD	GND	SYS_VIN_MV
40	GND	MID1	GND	MID0	GND
41	CSI1_D0_P	GND	CSI1_D1_P	GND	VM_EN1_N
42	CSI1_D0_N	CSI1_CLK_N	CSI1_D1_N	GND	VM_EN0_N
43	GND	CSI1_CLK_P	GND	CSI6_D0_N	GND
44	CSI3_D1_P	GND	CSI6_CLK_P	CSI6_D0_P	VM_I2C_SCK
45	CSI3_D1_N	CSI6_D1_N	CSI6_CLK_N	GND	VM_I2C_DAT
46	GND	CSI6_D1_P	GND	HDMI_DP0_TX3_P	GND
47	CSI4_D0_N	GND	HDMI_DP0_TX2_P	HDMI_DP0_TX3_N	VM_INT_N
48	CSI4_D0_P	HDMI_DP0_TX0_N	HDMI_DP0_TX2_N	GND	UART4_RX
49	GND	HDMI_DP0_TX0_P	GND	GPIO25	UART4_CTS
50	HDMI_DP0_TX1_N	GND	HDMI_CEC	DP2_HPD	GPIO35
51	HDMI_DP0_TX1_P	GPIO26	GPIO24	DP1_HPD	UART1_RTS
52	GND	GPIO27	DP1_AUX_CH_P	DP0_HPD	OVERTEMP_N
53	DP2_AUX_CH_P	MCLK03	DP1_AUX_CH_N	UART1_TX	VCC_RTC
54	DP2_AUX_CH_N	UART1_CTS	MCLK02	UART1_RX	MODULE_POWER_ON
55	GPIO23	MCLK04	GPIO32	GND	VDDIN_PWR_BAD_N
56	SPI3_MOSI	GND	GND	GPIO19	TEMP_ALERT_N
57	GND	UART5_CTS	SPI1_CLK	PWM01	MCLK05
58	UART2_RTS	UART5_RX	UART5_TX	UART5_RTS	PERIPHERAL_RESET_N
59	NC_03	NVJTAG_SEL	I2S3_DIN	I2S3_DOUT	SAFETY_PROCESSOR_GPIO
60	NVDBG_SEL	GPIO31	STANDBY_ACK_N	UART3_RX_DEBUG	SYS_RESET_N
61	JTAG_TRST_N	CAN1_DOUT	I2C2_CLK	I2C2_DAT	POWER_BTN_N
62	GND	UART3_TX_DEBUG	GND	FAN_PWM	CARRIER_POWER_ON
63	SYS_VIN_HV	GND	SYS_VIN_HV	GND	PRSNT1
64	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		
65	SYS_VIN_HV	SYS_VIN_HV	SYS_VIN_HV		

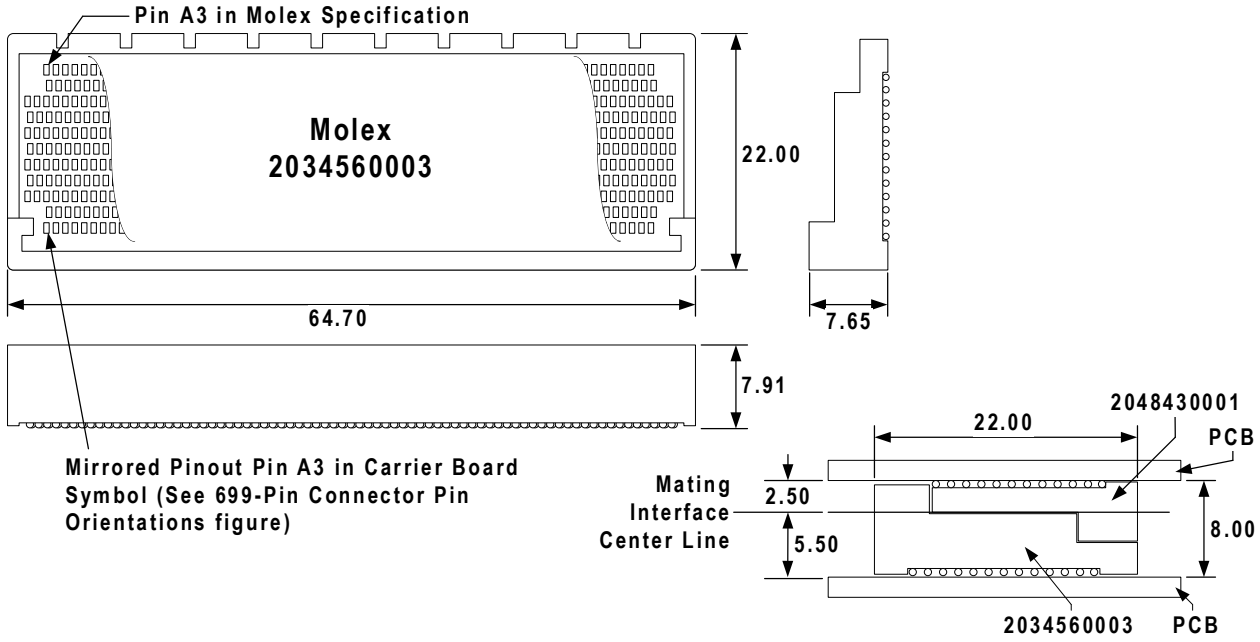
Legend

Ground	Power	Reserved – Must be left unconnected unless otherwise directed. See UART section for UART4_RX handling.

3.0 JETSON XAVIER MAIN 699-PIN CONNECTOR DETAILS

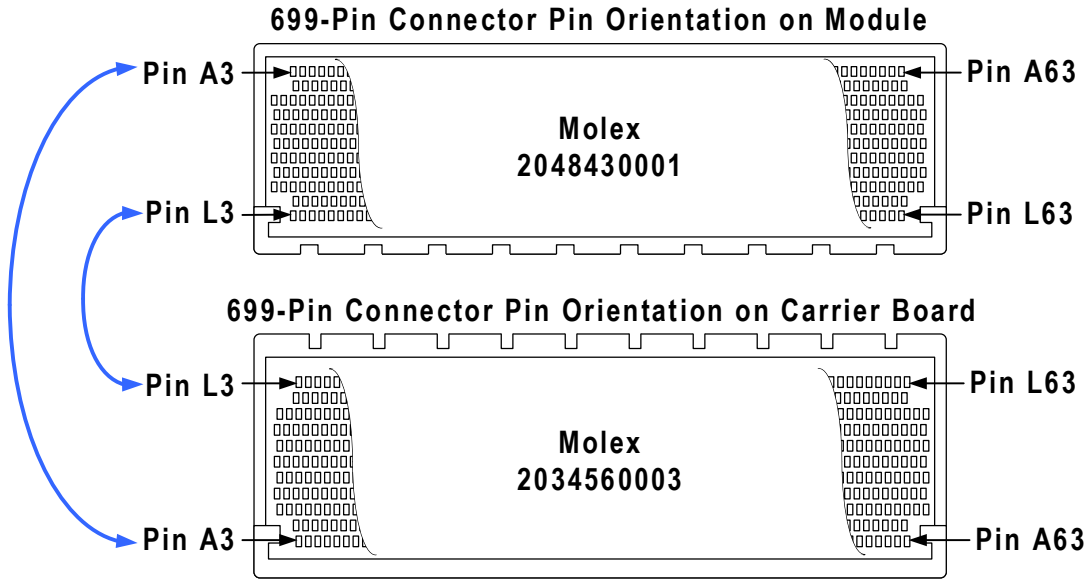
The main 699-pin connector on the Jetson Xavier module is from the Molex Mirror Mezz family and the part # is 2048430001. This mates with the Molex 2034560003 (shown in figure below) on the carrier board. Refer to the Molex Mirror Mezz connector specification for details.

Figure 2. 699-pin Connector Dimensions.



The symbol pinout for the 699-pin connector on the carrier board is mirrored such that the pin #s match when the module and carrier board connectors are mated. See the figure below. The orientation shown matches the carrier board in the upright position as well as the layout file.

Figure 3. 699-pin Connector Pin Orientations.



4.0 POWER

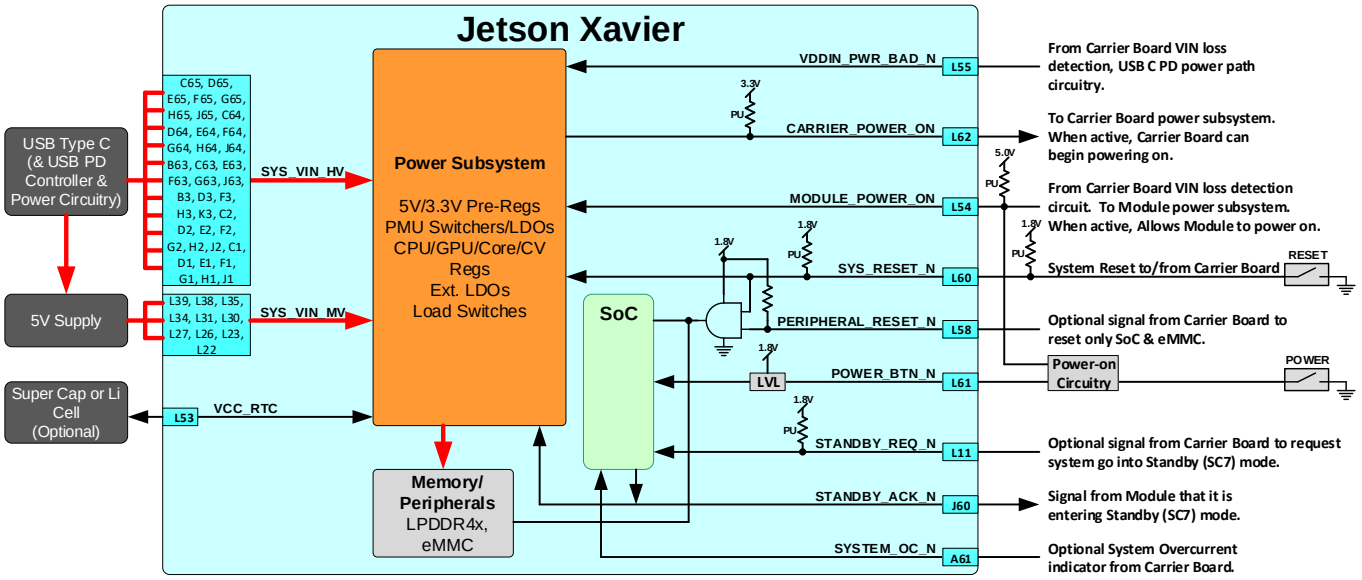
Caution *Jetson Xavier is not hot-pluggable. Before installing or removing the module, the main power supply (to SYS_VIN_HV & SYS_VIN_MV pins) must be disconnected and adequate time (recommended > 1 minute) must be allowed for the various power rails to fully discharge.*

Table 6. Jetson Xavier Power & System Pin Descriptions

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
Note 1	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
Note 2	SYS_VIN_MV	–	System Voltage Input - Medium	Main Medium Voltage DC Input	Input	Power: 5.0V
L53	VCC_RTC	–	Real-Time-Clock. Optionally used to provide back-up power for RTC. Connects to Lithium Cell or super capacitor on Carrier Board. PMIC is supply when charging cap or coin cell. Super cap or coin cell is source when system is disconnected from power.	Battery Back-up using Super-capacitor	Bidir	Power: 1.65V-5.5V
L62	CARRIER_POWER_ON	–	Carrier Power On. Used as part of the power up sequence. When asserted, it is safe for the carrier board to power up.	System	Output	Pulled to 3.3V on Module
L10	FORCE_RECOVERY_N	SOC_GPIO00	Force Recovery strap pin	System	Input	CMOS – 1.8V
L54	MODULE_POWER_ON	–	Module Power On	System	Input	5.0V Open-Drain or CMOS – 3.3V
L58	PERIPHERAL_RESET_N	–	Peripheral Reset. Driven from carrier board to force reset of SoC & eMMC & QSPI (not PMIC).	Not used	Input	CMOS – 1.8V
L61	POWER_BTN_N	POWER_ON	Power Button. Used to initiate a system power-on & to enter/exit SC7.	System	Input	CMOS – 1.8V
J60	STANDBY_ACK_N	SOC_PWR_REQ	Standby Acknowledge	System	Output	CMOS – 1.8V
L11	STANDBY_REQ_N	SOC_GPIO01	Standby Request	System	Input	CMOS – 1.8V
L60	SYS_RESET_N	SYS_RESET_N	System Reset: Connected to NRST_IO of PMIC. Bidirectional reset driven from PMIC to carrier board for devices requiring full system reset. Can also be driven from carrier board to module to initiate full system reset (including PMIC) (i.e. From RESET button). A pull-up is present on module.	System	Output	CMOS – 1.8V
A61	SYSTEM_OC_N	BATT_OC	Battery Over-current (& Thermal) warning	Not used	Input	CMOS – 1.8V
F61	VCOMP_ALERT_N	VCOMP_ALERT	TBD	Not used	Input	CMOS – 1.8V
L55	VDDIN_PWR_BAD_N	–	VDD_IN Power Bad. Carrier board indication to the module that the VDD_IN power is not valid. Carrier board should de-assert this (drive high) only when SYS_VIN_HV/MV have reached the required voltage levels and are stable. This prevents SoC from powering up until the main input supply voltages are stable.	System	Input	5.0V Open-Drain
L52	OVERTEMP_N	SOC_GPIO55	Force Power Off Request	System	Output	CMOS – 1.8V
B54	WDT_RESET_OUT_N	SOC_GPIO23	Watchdog Timeout	Not used	Output	CMOS – 1.8V

Note:
1. SYS_VIN_HV pin #s: C65, D65, E65, F65, G65, H65, J65, C64, D64, E64, F64, G64, H64, J64, B63, C63, E63, F63, G63, J63, B3, D3, F3, H3, K3, C2, D2, E2, F2, G2, H2, J2, C1, D1, E1, F1, G1, H1, J1
2. SYS_VIN_MV pin #s: L39, L38, L35, L34, L31, L30, L27, L26, L23, L22

Figure 4. Power Block Diagram



4.1 Supply Allocation

Table 7 Jetson Xavier Internal Power Subsystem Allocation

Power Rails	Usage	(V)	Power Supply	Source
VDD_CPU	SoC CPU rail	Variable	NCP81276 & FDMF5833 (x2)	**SYS_VIN_HV**
VDD_GPU	SoC GPU rail	Variable	NCP81276 & FDMF5833 (x2)	**SYS_VIN_HV**
VDD_CORE (SOC)	SoC Core rail	Variable	NCP81276 & FDMF5833 (x2)	**SYS_VIN_HV**
VDD_CV	SoC CV rail	Variable	NCP81276 & FDMF5833 (x2)	**SYS_VIN_HV**
VDDIO_SYS_1V0	SoC AVDDIO_HDMI_DP[3:0], PEX_DVDD, NVHS0_DVDD rails	1.0	PMIC Switcher SD0	**SYS_VIN_MV**
VDDIO_SYS_1V8HS	See note 1	1.8	PMIC Switcher SD1	**SYS_VIN_MV**
VDDIO_SYS_1V8LS	See note 2	1.8	PMIC Switcher SD2	**SYS_VIN_MV**
AVDD_CSI_1V2	SoC AVDD_CSI & VDDIO_UFS rails (See note 3)	1.2	PMIC LDO7	**SYS_VIN_MV**
EN_VDD_1V0	Enable for FETs gating discharge of VDDIO_SYS_1V0 rail (See note 3)	na	PMIC LDO8	**SYS_VIN_MV**
VDDIO_AO_1V8	See note 4	1.8	PMIC Switcher SD3	**SYS_VIN_MV**
DDR_AP_1V1	SoC VDDIO_DDRx rail	1.1	PMIC Switcher SD4	**SYS_VIN_MV**
VDD_RTC	SoC RTC rail	Variable	PMIC LDO0	**SYS_VIN_MV**
DDR_VDD2_1V1_EN	See note 5	Na	PMIC LDO1	**SYS_VIN_MV**
VDDIO_AO_3V3	SoC VDDIO_AUDIO_HV & VDDIO_AO_HV rails	3.3	PMIC LDO2	**SYS_VIN_MV**
VDD_EMMC_3V3	eMMC device 3.3V rail	3.3	PMIC LDO3	**SYS_VIN_MV**
VDD_USB_3V3	SoC AVDD_USB rail	3.3	PMIC LDO5	**SYS_VIN_MV**
VDD_SDIO_3V3	SoC VDDIO_SDMMC[3:1]_HV rails	3.3	PMIC LDO6	**SYS_VIN_MV**
DDR_VDD2_1.1V	SoC VDDIO_VDD2_DDRx & DRAM VDD2 rails.	1.1	LTC3636	**SYS_VIN_HV**
VDD_DDRQ	VDDIO_DDRxLV & LPDDR4x VDDQ rails	0.6 LPDDR4x	LTC3636	**SYS_VIN_HV**

Note:
1. SoC AVDD_PLL_NVHS_EUTMIP, VDD_HDMI_DP_PLL_0_1/1_3, PEX_HVDD, NVHS0_HVDD & NVHS0_PLL0_HVDD rails
2. SoC VDDIO_UART/AUDIO/SDMMC4/DMMC3_HV_VCLAMP/ VDDIO_SDMMC1_HV_VCLAMP/CONN/EQOS/QSPI/, AVDD_PLL_AA1_CV_ADC/DD2D3D4DPHBCS/CC2C3PADC_BPMP/C4_REFE, eMMC device VCCQ & QSPI device VDD rails.
3. These rails are sourced from the PMIC Switcher SD2 used for VDDIO_SYS_1V8LS which is sourced from SYS_VIN_MV.
4. SoC VDDIO_EDP/PEX_CTL/DEBUG/CAM/AO/VREFR0/ SYS, VPP_FUSE, AVDD_PLL_AON/MSC/GADC_M/MSD/XADC_MSB, VCLAMP_USB, AVDD_OSC, LPDDR4x device VDD1, Temp Sensor VDD
5. Enable (RUN2 pin) for VDD_DDRQ supply & Enable for discharge of DDR_VDD2_1.1V, VDDIO_SYS_1V8HS/SYS_1V8LS/AO_1V8 rails.

4.2 Power Sequencing

Figure 5. Power Up Sequence

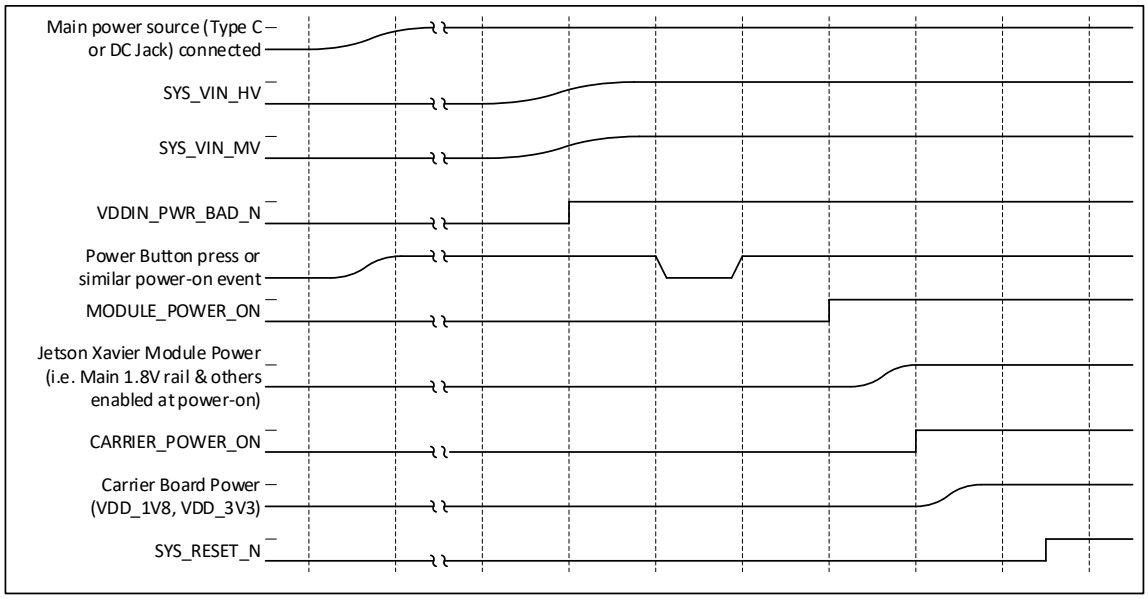


Figure 6. Power Down Sequence (Controlled Case)

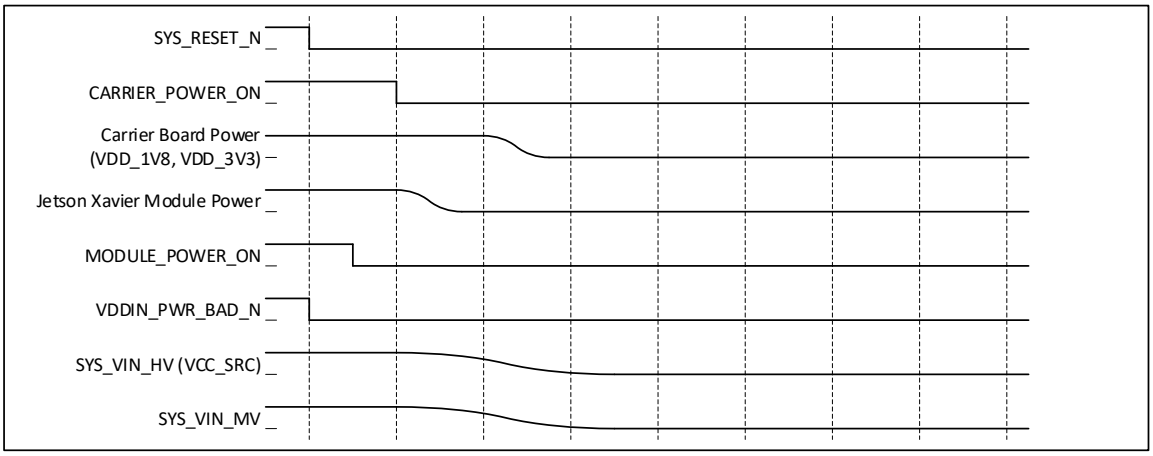
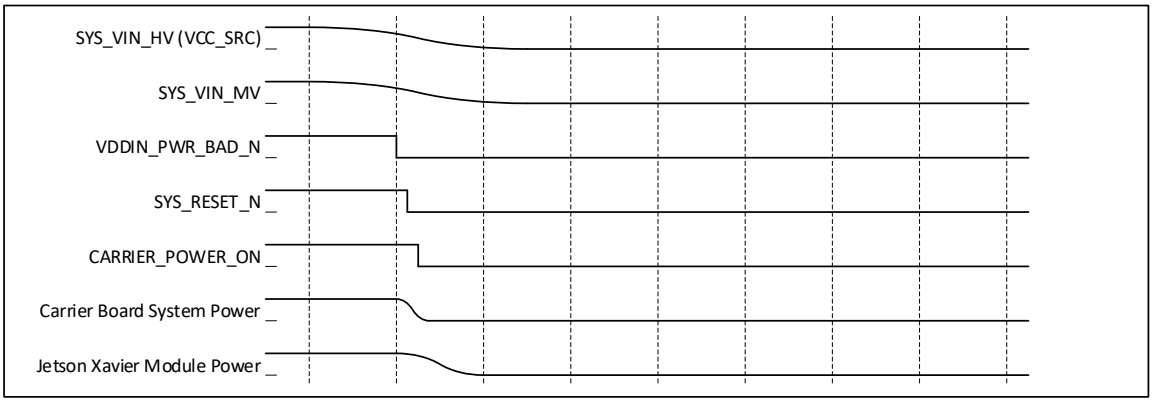


Figure 7. Power Down Sequence (Uncontrolled Power Removal Case)



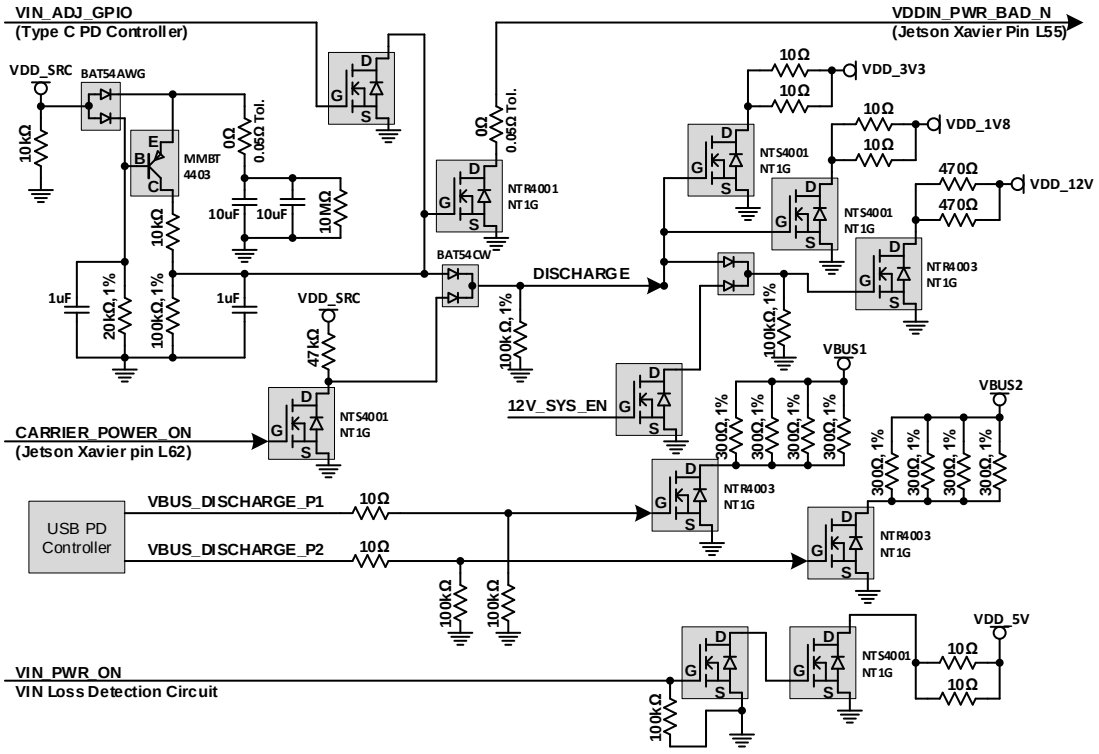
4.3 Auto-Power-On Option

For designs that will not have a power button but should power on when the main power supply is connected, MODULE_POWER_ON can be pulled up to an available 5V source. On the Nvidia carrier board, this would be 5V_AO. The Nvidia carrier board power solution has the signal VIN_PWR_ON which keeps the system from powering on if a module is not installed. This is to protect against accidently hot-plugging the module and possibly damaging the module or carrier board. If the equivalent of VIN_PWR_ON is implemented, this would also need to be active (driven by 3.3V push-pull device).

4.4 Power Discharge

To meet the Power Down requirements, discharge circuitry is required. In the figure, which is based on the P2822 Jetson Xavier Carrier Board, the DISCHARGE signal is generated, based on a transition of the CARRIER_POWER_ON signal or the removal of the main supply (VDD_SRC). When DISCHARGE is asserted, VDD_1V8, VDD_3V3, VDD_5V & VDD_12V are forced to GND in a controlled manner. Removal of the VDD_SRC supply also causes VDDIN_PWR_BAD_N to go active which causes Jetson Xavier to initiate a controlled shut down. In addition, the main VBUS[2:1] rails are discharged. The discharge for these is controlled by the USB PD Controller which generates the VBUS_DISCHARGE_P[2:1] signals shown below. These signals go active when the USB Type C supply turns off (cable disconnected, or upstream power source removed). When these signals go active, the VBUS[2:1] rails are forced to GND in a controlled manner as well.

Figure 8. Power Discharge



4.5 Power Button Supervisor

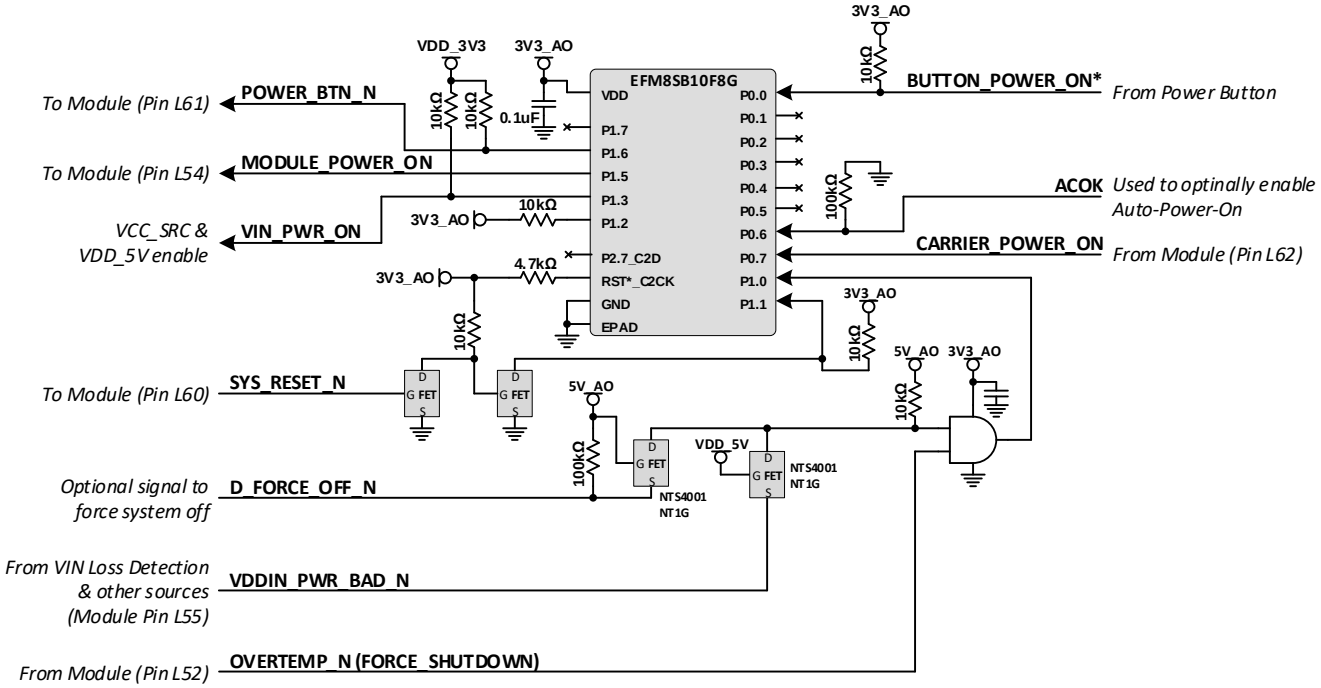
The Nvidia Jetson Xavier carrier board implements a power button supervisor. This supervisor is a low power device meant to intercept push-button (momentary) switches to control ON/Enable signals to the module PMIC and main processor. This supervisor is always powered and allows close to complete system power OFF while providing proper timing for ON/OFF signals to the system. The selected MCU to perform this function is the EFM8SB10F8G-A-QFN20_ from Silicon Labs.

Table 8 Jetson Xavier Internal Power Subsystem Allocation

Signal Name	Associated Jetson Xavier Pin #	I/O Type	Trigger Level	Drive Mode	Description	MCU Pin
BUTTON_POWER_ON*		Input (debounced)	Level	OD (HiZ)	Power Button	P0.0
ACOK		Input (debounced)	Edge	OD (HiZ)	Determine when USB power is supplied	P0.6
CARRIER_POWER_ON	L62	Input	Level	OD (HiZ)	Closed loop on power output	P0.7
RESET_N (SYS_RESET_N)	L60	Input	Edge	OD (HiZ)	Monitor / Power Good mask	P1.1
FORCE_SHUTDOWN_N (OVERTEMP_N)	L52	Input	Edge	OD (HiZ)	Triggers shutdown sequence	P1.0
BRD_SEL		Input		OD (HiZ)	Strap pin for board selection	P1.2
VIN_PWR_ON		Output		PP	Enable power to module	P1.3
MODULE_POWER_ON	L54	Output		PP	Enable input to PMIC	P1.5
POWER_BTN_N	L61	Output		OD	Buffered output of power button signal	P1.6

Note: OD – Open-drain. PP = Push-pull

Figure 9. Power-On Button Circuit



Defined behaviors

For all actions triggered by BUTTON_POWER_ON*, there will be a de-bounce time before triggering any output signal. All timings below are referenced from AFTER the de-bouncing. Therefore, a “0 ms” value indicates that the signal should start right after de-bounce. De-bounce time is 20ms.

Power OFF -> Power ON (Power Button Case)

Power button press use case: User presses the Power Button briefly, and the MCU sends the power enable signals to the module (VIN_PWR_ON) and to the PMIC on the module (MODULE_POWER_ON). The signal representing the Power Button to Jetson Xavier (POWER_BTN_N), will have the same (brief) duration of the Power Button input to the MCU. Once the power button is pressed, the power OK input (ACOK) is ignored, as the power ON sequence is already initiated by the power button.

Figure 10. Power-OFF to On Sequence (Power Button Case)

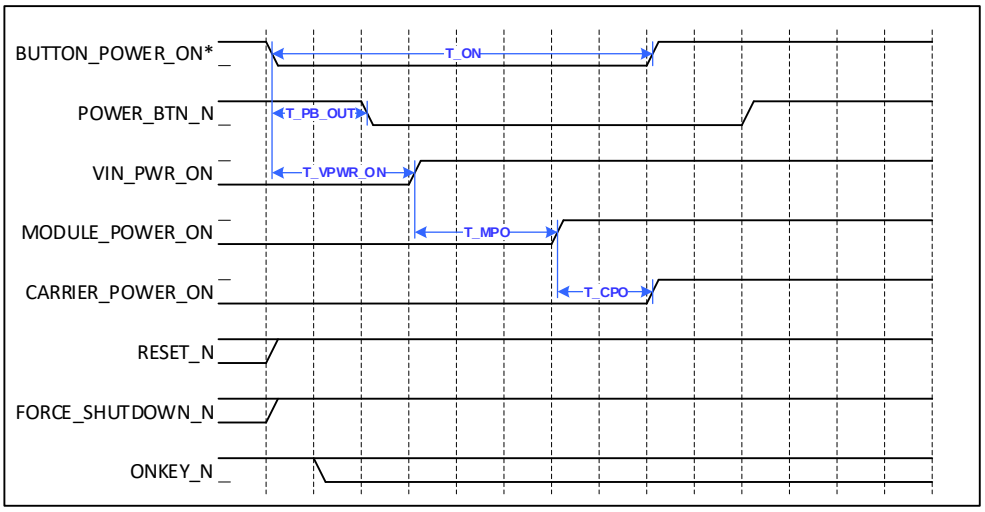


Table 9 Power-OFF to On Timing (Power Button Case)

Timing	Parameter	Typical	Units
T_ON	Power button active duration	>20	ms
T_PB_OUT	Delay to POWER_BTN_N assertion	20	ms
T_VPWR_ON	Delay to first rail ON	20	ms
T_MPO	MODULE_POWER_ON (module PMIC enable) delay from power VIN_PWR_ON rising edge	80	ms
T_CPO	Expected delay to CARRIER_POWER_ON assertion	10	ms

Power OFF -> Power ON (Auto-Power-On Case)

When the user connects the main power source, the MCU sends the power enable signals to the module (VIN_PWR_ON) and enables MODULE_POWER_ON. This is accomplished by having the ACOK signal driven high instead of pulled to GND.

The signal representing the Power Button to Jetson Xavier (POWER_BTN_N) will continue following the power button (BUTTON_POWER_ON*) behavior. However, once the power ON sequence is initiated by the connection of the main power source, and ACOK is driven high (by push-pull driver powered from 3V3_AO), the power button signals will not affect the MCU behavior until the PWR_GOOD signal verification is complete.

Figure 11. Power-OFF to On Sequence (Auto-Power-On Case)

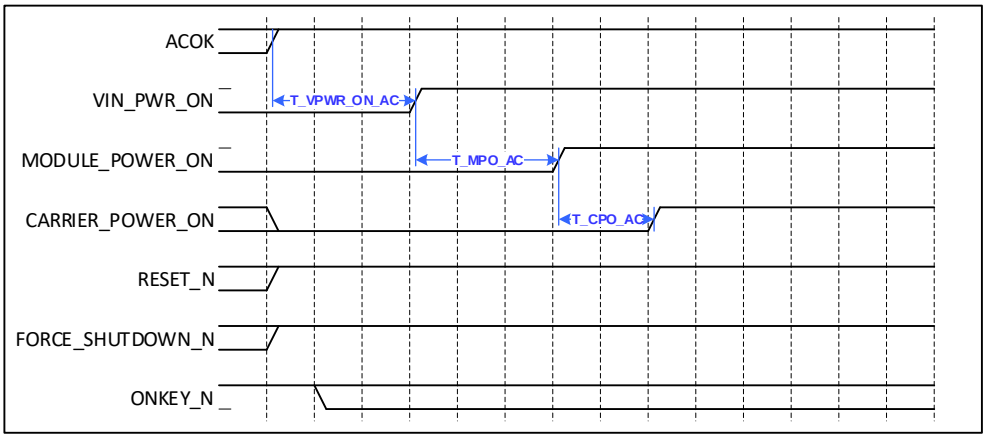


Table 10 Power-OFF to On Timing (Auto-Power-On Case)

Timing	Parameter	Typical	Units
T_VPWR_ON_AC	Delay from ACOK detected high with main power source applied to first rail ON	20	ms
T_MPO_AC	MODULE_POWER_ON active delay from VIN_PWR_ON rising edge	80	ms
T_CPO_AC	Expected delay to CARRIER_POWER_ON active	10	ms

Power ON -> Power OFF (Power Button Held Low > 10 Seconds)

With the system in power ON state, the user holds the power button for more than 10 seconds. The same button signal is relayed to Jetson Xavier through the buffered signal POWER_BTN_N. The system is forced to shut down at the 10 seconds mark.

Figure 12. Power-ON to OFF Sequence (Power Button Held Low > 10 Seconds)

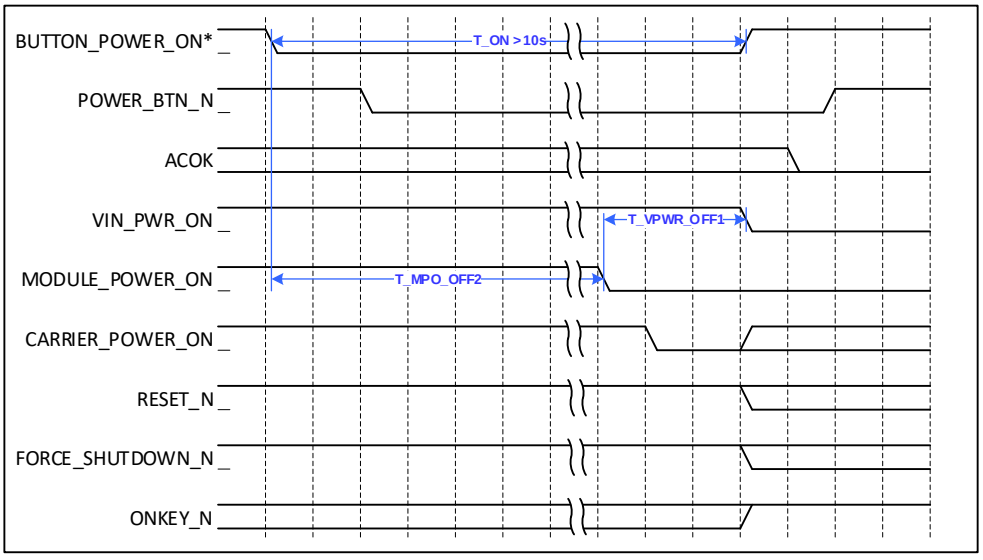


Table 11 Power-ON to OFF Timing (Power Button Held Low > 10 Seconds)

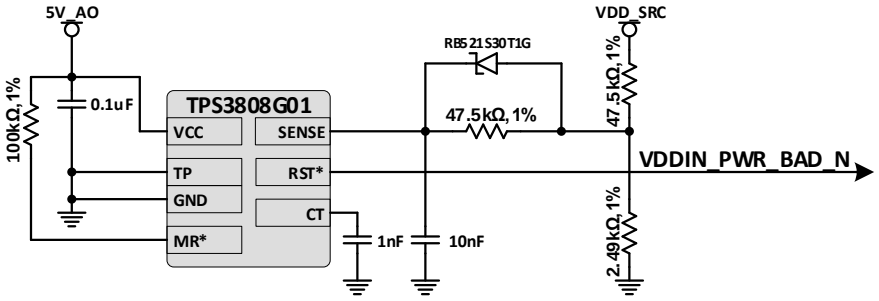
Timing	Parameter	Typical	Units
T_ON	Power button active duration for forced OFF	> 10	s
T_VPWR_OFF1	Delay to first rail off	10	ms
T_MPO_OFF2	Wait time to force MODULE_POWER_ON disable	10	s

4.6 Power & Voltage Monitoring

4.6.1 Power Loss Detection

The circuit below is implemented on the Nvidia Jetson Xavier carrier board to detect a loss or unacceptable droop on the main power input (VCC_SRC).

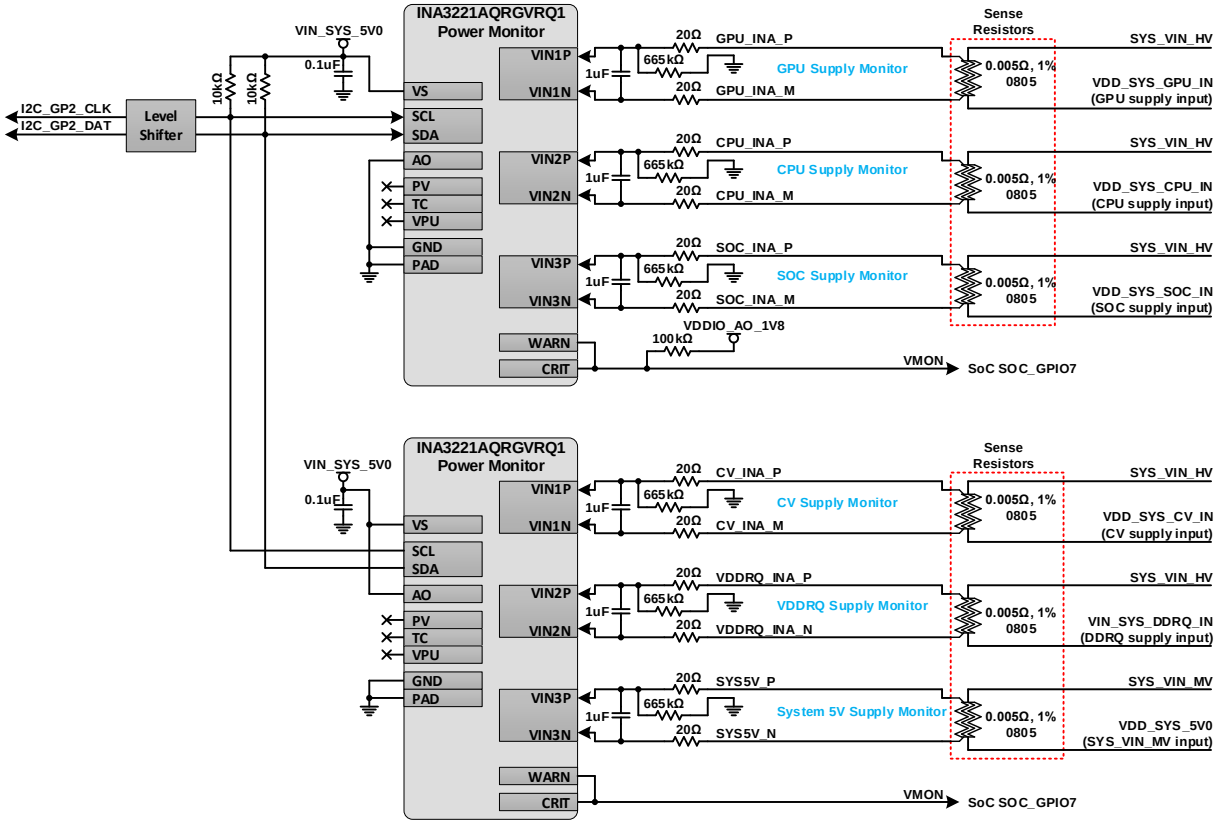
Figure 13. VIN Loss Detection Circuit



4.6.2 Power Monitor

Power monitors are provided on Jetson Xavier. These monitor the VDD_GPU, VDD_CPU, VDD_SOC (Core), VDD_CV, VDD_DDRQ & SYS_VIN_MV Supplies. The monitors will Toggle a WARN (Warning) or CRIT (Critical) output, depending on the power "seen" at the sense resistors and the thresholds set for each supply. This output is connected to the SOC_GPIO7 pin. The I2C address for the top Power Monitor (GPU/CPU/SOC) is 7'H40, and for the bottom Power Monitor (CV, VDDRQ, SYS_VIN_MV) is 7'H41).

Figure 14. Power Monitor



4.7 Deep Sleep (SC7)

Jetson Xavier supports a low power state called Deep Sleep or SC7. This can be entered under software control, and exited using various mechanisms, including wake capable pins that are listed in the table below.

Table 12. Jetson Xavier Signal Wake Events

Potential Wake Event (Reference Design Signal)	Jetson Xavier Pin Assigned	Wake #
PCIe Wake Request (PEX_WAKE_N)	PEX_WAKE_N	Wake01
SD Card Data 1 (SDCARD_D1)	SDCARD_D1	Wake03
Backlight PWM (BKLIGHT_PWM)	GPIO27	Wake04
GPIO 0 (CVB_GPIO0)	GPIO02	Wake08
System Overcurrent Control (SYSTEM_OC#)	SYSTEM_OC_N	Wake10
GPIO 1 (CVB_GPIO1)	GPIO11	Wake12
GPIO 3 (GPIO3/SD_WP)	GPIO29	Wake13
GPIO 2(CVB_GPIO2)	GPIO12	Wake15
Ethernet SMA MDIO (RGMII_SMA_MDIO)	RGMII_SMA_MDIO	Wake17
Ethernet Interrupt (ENET_INT)	ENET_INT	Wake20
I2C General Purpose 3 Data (I2C_GP3_DAT)	I2C3_DAT	Wake21
I2C General Purpose 4 Data (I2C_GP4_DAT)	I2C4_DAT	Wake22
Safe State (SAFE_STATE)	GPIO31	Wake25
Voltage Monitor (VMON)	VCOMP_ALERT_N	Wake26
Ethernet RX Control (RGMII_RX_CTL)	RGMII_RX_CTL	Wake28
Power On (POWER_ON)	POWER_BTN_N	Wake29
GPU Fault (GPU_FAULT)	GPIO01	Wake30
I2C General Purpose 1 Data (I2C_GP1_DAT)	I2C1_DAT	Wake31
PCIe L5 Clock Request (PEX_L5_CLKREQ_N)	PEX_L5_CLKREQ_N	Wake32
Board Identification 1 (BOARD_ID1)	UART1_CTS	Wake33
GPIO Expander 0 Interrupt (GPIO_EXP0_INT)	GPIO32	Wake34
USB OTG Identification (USB_OTG_ID)	GPIO30	Wake35
GPIO Expander 1 Interrupt (GPIO_EXP1_INT)	GPIO33	Wake36
GPIO Expander 2 Interrupt (GPIO_EXP2_INT)	GPIO34	Wake37
Watchdog Timer Reset Output (WDT_RESET_OUT)	WDT_RESET_OUT_N	Wake38
SPI 2 Chip Select 0 (SPI2_CS0#)	SPI2_CS0_N	Wake39
GPIO 5(CVB_GPIO5)	GPIO17	Wake40
I2C General Purpose 2 Data (I2C_GP4_DAT)	I2C2_DAT	Wake41
CAN 1 Data Input (CAN1_DIN)	CAN1_DIN	Wake42
CAN 0 Data Input (CAN0_DIN)	CAN0_DIN	Wake43
SPI 3 Clock (SPI3_CLK)	SPI3_CLK	Wake44
SPI 1 Chip Select 0 (SPI1_CS0#)	SPI1_CS0_N	Wake45
CAN 0 GPIO 1 (CAN0_GPIO1)	GPIO07	Wake46
CAN1 GPIO 1 (CAN1_GPIO1)	GPIO10	Wake48
SPI 1 Chip Select 1 (SPI1_CS1#)	SPI1_CS1_N	Wake50
Fan Tachometer (FAN_TACH)	FAN_TACH	Wake51
UART 1 Clear to Send (UART1_CTS)	UART2_CTS	Wake52
UART 2 Clear to Send (UART2_CTS)	UART5_CTS	Wake53
PCIe L1 Clock Request (PEX_L1_CLKREQ_N)	PEX_L1_CLKREQ_N	Wake54
SPI 3 Chip Select 0 (SPI3_CS0#)	SPI3_CS0_N	Wake56
SPI 3 Chip Select 1 (SPI3_CS1#)	SPI3_CS1_N	Wake58
Discrete GPU Alert (DGPU_ALERT)	GPIO03	Wake59
DP 0 Hot-Plug-Detect (DP0_HPD)	DP0_HPD	Wake60
USB VBUS Enable 0 (USB_VBUS_EN0)	GPIO22	Wake61
USB VBUS Enable 1 (USB_VBUS_EN1)	GPIO23	Wake62
DP 1 Hot-Plug-Detect (DP1_HPD)	DP1_HPD	Wake63
PCIe L3 Clock Request (PEX_L3_CLKREQ_N)	PEX_L3_CLKREQ_N	Wake65
GPIO 6(CVB_GPIO6)	GPIO24	Wake66
Force Recovery (FORCE_RECOVERY)	FORCE_RECOVERY_N	Wake67
Sleep (SLEEP#)	STANDBY_REQ_N	Wake68
Battery Low (BATLOW#)	GPIO28	Wake69
HDMI Consumer Electronics Control (HDMI_CEC)	HDMI_CEC	Wake70
DP 2 Hot-Plug-Detect (DP2_HPD)	DP2_HPD	Wake71

5.0 GENERAL ROUTING GUIDELINES

Signal Name Conventions

The following conventions are used in describing the signals for Jetson Xavier:

- Signal names use a mnemonic to represent the function of the signal. For example, Secure Digital Interface #3 Command signal is represented as **SDCARD_CMD**, written in bold to distinguish it from other text. All active low signals are identified by a # or an underscore followed by capital N (_N) after the signal name. For example, **RESET_IN#** indicates an active low signal. Active high signals do not have the underscore-N (_N) after the signal names. For example, **SDCARD_CMD** indicates an active high signal. Differential signals are identified as a pair with the same names that end with _P & _N, just P & N or + & - (for positive and negative, respectively). For example, **USB1_DP** and **USB1_DN** indicate a differential signal pair.
- I/O Type The signal I/O type is represented as a code to indicate the operational characteristics of the signal. The table below lists the I/O codes used in the signal description tables.

Table 13. Signal Type Codes

Code	Definition
A	Analog
DIFF I/O	Bidirectional Differential Input/Output
DIFF IN	Differential Input
DIFF OUT	Differential Output
I/O	Bidirectional Input/Output
I	Input
O	Output
OD	Open Drain Output
I/OD	Bidirectional Input / Open Drain Output
P	Power

Routing Guideline Format

The routing guidelines have the following format to specify how a signal should be routed.

- Breakout traces are traces routed from a BGA or other pin array, either to a point beyond the array, or to another layer where full normal spacing guidelines can be met. Breakout trace delay limited to 500 mils unless otherwise specified.
- After breakout, signal should be routed according to specified impedance for differential, single-ended, or both (for example: HDMI). Trace spacing to other signals also specified.
- Follow max & min trace delays where specified. Trace delays are typically shown in mm or in terms of signal delay in pico-seconds (ps) or both.
  - For differential signals, trace spacing to other signals must be larger of specified × dielectric height or inter-pair spacing
  - Spacing to other signals/pairs cannot be smaller than spacing between complementary signals (intra-pair).
  - Total trace delay depends on signal velocity which is different between outer (microstrip) & inner (stripline) layers of a PCB.

Signal Routing Conventions

Throughout this document, the following signal routing conventions are used:

SE Impedance (/ Diff Impedance) at x Dielectric Height Spacing

- Single-ended (SE) impedance of trace (along with differential impedance for diff pairs) is achieved by spacing requirement. Spacing is multiple of dielectric height. Dielectric height is typically different for microstrip & stripline. Note: 1 mil = 1/1000th of an inch.

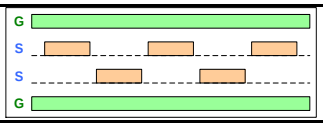
Note: Trace spacing requirement applies to SE traces or differential pairs to other SE traces or differential pairs. It does not apply to traces making up a differential pair. For this case, spacing/trace widths are chosen to meet differential impedance requirement.

General Routing Guidelines

Pay close attention when routing high speed interfaces, such as HDMI/DP, USB 3.1, PCIe or DSI/CSI. Each of these interfaces has strict routing rules for the trace impedance, width, spacing, total delay, and delay/flight time matching. The following guidelines provide an overview of the routing guidelines and notations used in this document.

- **Controlled Impedance**
  Each interface has different trace impedance requirements & spacing to other traces. It is up to designer to calculate trace width & spacing required to achieve specified single-ended (SE) & differential (Diff) impedances. Unless otherwise noted, trace impedance values are ±15%.
- **Max Trace Lengths/Delays**
  Trace lengths/delays should include main PCB routing and any additional routing on a Flex/ secondary PCB segment connected to main PCB. The max length/delay should be from Jetson Xavier to the actual connector (i.e. USB, HDMI, SD Card, etc.) or device (i.e. onboard USB device, Display driver IC, camera imager IC, etc.)
- **Trace Delay/Flight Time Matching**
  Signal flight time is the time it takes for a signal to propagate from one end (driver) to other end (receiver). One way to get same flight time for signal within signal group is to match trace lengths within specified delay in the signal group.
  - Total trace delay = Carrier PCB trace delay only. Do not exceed maximum trace delay specified.
  - For six layers or more, it is recommended to match trace delays based on flight time of signals. For example, outer-layer signal velocity could be 150psi (ps/inch) & inner-layer 175psi. If one signal is routed 10 inches on outer layer & second signal is routed 10 inches in inner layer, difference in flight time between two signals will be 300ps! That is a big difference if required matching is 15ps (trace delay matching). To fix this, inner trace needs to be 1.7 inches shorter or outer trace needs to be 2 inches longer.
  - In this design guide, terms such as intra-pair & inter-pair are used when describing differential pair delay. Intra-pair refers to matching traces within differential pair (for example, true to complement trace matching). Inter-pair matching refers to matching differential pairs average delays to other differential pairs average delays.

General PCB Routing Guidelines

For GSSG stack-up to minimize crosstalk, signal should be routed in such a way that they are not on top of each other in two routing layers (see diagram to right)	
Do not route other signals or power traces/areas directly under or over critical high-speed interface signals.	

Note: *The requirements detailed in the Interface Signal Routing Requirements tables must be met for all interfaces implemented or proper operation cannot be guaranteed.*

6.0 USB, PCIE, UFS

Jetson Xavier allows multiple USB 3.1 & PCIe interfaces & UFS to be brought out on the module. The table following the Pin Description tables shows the configurations allowed for these interfaces.

Table 14. Jetson Xavier USB 2.0 Pin Descriptions

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
F13	USB0_N	USB0_DN	USB 2.0 Port 0 Data–	UART-USB Bridge or USB Type C Connector (J7)	Bidir	USB2 Diff pair
F12	USB0_P	USB0_DP	USB 2.0 Port 0 Data+	UART-USB Bridge or USB Type C Connector (J7)	Bidir	USB2 Diff pair
C10	USB1_N	USB1_DN	USB 2.0, Port 1 Data–	USB Type C Connector (J8)	Bidir	USB2 Diff pair
C11	USB1_P	USB1_DP	USB 2.0, Port 1 Data+	USB Type C Connector (J8)	Bidir	USB2 Diff pair
A11	USB2_N	USB2_DN	USB 2.0, Port 2 Data–	M.2 Key E Connector	Bidir	USB2 Diff pair
A10	USB2_P	USB2_DP	USB 2.0, Port 2 Data+	M.2 Key E Connector	Bidir	USB2 Diff pair
G10	USB3_N	USB3_DN	USB 2.0, Port 3 Data–	USB / eSATA Connector (USB 2.0)	Bidir	USB2 Diff pair
G11	USB3_P	USB3_DP	USB 2.0, Port 3 Data+	USB / eSATA Connector (USB 2.0)	Bidir	USB2 Diff pair

Table 15. Jetson Xavier UPHY Pin Descriptions (Used for USB 3.1, PCIe & UFS)

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
E26	UPHY_REFCLK1_N	PEX_REFCLK1_N	UPHY Reference Clock 1- used when Jetson Xavier is an Endpoint	Unused	Input	PCIe Diff Pair
E27	UPHY_REFCLK1_P	PEX_REFCLK1_P	UPHY Reference Clock 1+ used when Jetson Xavier is an Endpoint		Input	
A23	UPHY_RX0_N	PEX_RX0_N	UPHY Receive 0-	eSATA Bridge	Input	PCIe Diff Pair, - TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
A22	UPHY_RX0_P	PEX_RX0_P	UPHY Receive 0+		Input	
J23	UPHY_TX0_N	PEX_TX0_N	UPHY Transmit 0-		Output	
J22	UPHY_TX0_P	PEX_TX0_P	UPHY Transmit 0+		Output	
C22	UPHY_RX1_N	PEX_RX1_N	UPHY Receive 1-	USB Type C Alt Mode SW (for J7)	Input	USB3 Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
C23	UPHY_RX1_P	PEX_RX1_P	UPHY Receive 1+		Input	
G22	UPHY_TX1_N	PEX_TX1_N	UPHY Transmit 1-		Output	
G23	UPHY_TX1_P	PEX_TX1_P	UPHY Transmit 1+		Output	
B20	UPHY_RX2_N	PEX_RX2_N	UPHY Receive 2-	M.2 Key M Connector	Input	PCIe Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
B21	UPHY_RX2_P	PEX_RX2_P	UPHY Receive 2+		Input	
K20	UPHY_TX2_N	PEX_TX2_N	UPHY Transmit 2-		Output	
K21	UPHY_TX2_P	PEX_TX2_P	UPHY Transmit 2+		Output	
D21	UPHY_RX3_N	PEX_RX3_N	UPHY Receive 3-		Input	
D20	UPHY_RX3_P	PEX_RX3_P	UPHY Receive 3+		Input	
H21	UPHY_TX3_N	PEX_TX3_N	UPHY Transmit 3-		Output	
H20	UPHY_TX3_P	PEX_TX3_P	UPHY Transmit 3+		Output	
A19	UPHY_RX4_N	PEX_RX4_N	UPHY Receive 4-		Input	
A18	UPHY_RX4_P	PEX_RX4_P	UPHY Receive 4+		Input	
J19	UPHY_TX4_N	PEX_TX4_N	UPHY Transmit 4-		Output	
J18	UPHY_TX4_P	PEX_TX4_P	UPHY Transmit 4+		Output	
C18	UPHY_RX5_N	PEX_RX5_N	UPHY Receive 5-		Input	
C19	UPHY_RX5_P	PEX_RX5_P	UPHY Receive 5+		Input	
G18	UPHY_TX5_N	PEX_TX5_N	UPHY Transmit 5-		Output	
G19	UPHY_TX5_P	PEX_TX5_P	UPHY Transmit 5+		Output	
B17	UPHY_RX6_N	PEX_RX6_N	UPHY Receive 6-	USB Type C Alt Mode SW (for J8)	Input	USB3 Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
B16	UPHY_RX6_P	PEX_RX6_P	UPHY Receive 6+		Input	
K16	UPHY_TX6_N	PEX_TX6_N	UPHY Transmit 6-		Output	
K17	UPHY_TX6_P	PEX_TX6_P	UPHY Transmit 6+		Output	
D17	UPHY_RX7_N	PEX_RX7_N	UPHY Receive 7-	M.2 Key E Connector	Input	PCIe Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
D16	UPHY_RX7_P	PEX_RX7_P	UPHY Receive 7+		Input	
H17	UPHY_TX7_N	PEX_TX7_N	UPHY Transmit 7-		Output	
H16	UPHY_TX7_P	PEX_TX7_P	UPHY Transmit 7+		Output	
A14	UPHY_RX8_N	PEX_RX8_N	UPHY Receive 8-	Unused	Input	PCIe Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier
A15	UPHY_RX8_P	PEX_RX8_P	UPHY Receive 8+		Input	
J15	UPHY_TX8_N	PEX_TX8_N	UPHY Transmit 8-		Output	

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
J14	UPHY_TX8_P	PEX_TX8_P	UPHY Transmit 8+		Output	board if direct connect to device.
C14	UPHY_RX9_N	PEX_RX9_N	UPHY Receive 9-		Input	PCIe Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
C15	UPHY_RX9_P	PEX_RX9_P	UPHY Receive 9+		Input	
G14	UPHY_TX9_N	PEX_TX9_N	UPHY Transmit 9-		Output	
G15	UPHY_TX9_P	PEX_TX9_P	UPHY Transmit 9+		Output	
B13	UPHY_RX10_N	PEX_RX10_N	UPHY Receive 10-	Micro SD / UFS Card Socket	Input	UFS Diff Pair
B12	UPHY_RX10_P	PEX_RX10_P	UPHY Receive 10+		Input	
K12	UPHY_TX10_N	PEX_TX10_N	UPHY Transmit 10-		Output	
K13	UPHY_TX10_P	PEX_TX10_P	UPHY Transmit 10+		Output	
D13	UPHY_RX11_N	PEX_RX11_N	UPHY Receive 11-	USB / eSATA Connector (USB 3.1)	Input	USB3 Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
D12	UPHY_RX11_P	PEX_RX11_P	UPHY Receive 11+		Input	
H13	UPHY_TX11_N	PEX_TX11_N	UPHY Transmit 11-		Output	
H12	UPHY_TX11_P	PEX_TX11_P	UPHY Transmit 11+		Output	

Table 16. Jetson Xavier NVHS (for PCIe x8) Pin Descriptions

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
E31	NVHS0_SLVS_REFCLK0_N	NVHS0_REFCLK_N	NVHS Reference Clock 0- used when Jetson Xavier is an Endpoint	PCIe x16 Connector after mux	Input	PCIe Diff Pair
E30	NVHS0_SLVS_REFCLK0_P	NVHS0_REFCLK_P	NVHS Reference Clock 0+ used when Jetson Xavier is an Endpoint			
D25	NVHS0_SLVS_RX0_N	NVHS0_RX0_N	NVHS (PCIe x8) Receive 0-	PCIe x16 Connector	Input	PCIe/SLVS Diff Pair, AC-Coupled on carrier board if PCIe & direct connect to device.
D24	NVHS0_SLVS_RX0_P	NVHS0_RX0_P	NVHS (PCIe x8) Receive 0+			
H25	NVHS0_TX0_N	NVHS0_TX0_N	NVHS (PCIe x8) Transmit 0-		Output	PCIe Diff Pair, AC-Coupled on carrier board
H24	NVHS0_TX0_P	NVHS0_TX0_P	NVHS (PCIe x8) Transmit 0+			
B24	NVHS0_SLVS_RX1_N	NVHS0_RX1_N	NVHS (PCIe x8) Receive 1-		Input	PCIe/SLVS Diff Pair, AC-Coupled on carrier board if PCIe & direct connect to device.
B25	NVHS0_SLVS_RX1_P	NVHS0_RX1_P	NVHS (PCIe x8) Receive 1+			
K24	NVHS0_TX1_N	NVHS0_TX1_N	NVHS (PCIe x8) Transmit 1-		Output	PCIe Diff Pair, AC-Coupled on carrier board
K25	NVHS0_TX1_P	NVHS0_TX1_P	NVHS (PCIe x8) Transmit 1+			
C26	NVHS0_SLVS_RX2_N	NVHS0_RX2_N	NVHS (PCIe x8) Receive 2-		Input	PCIe/SLVS Diff Pair, AC-Coupled on carrier board if PCIe & direct connect to device.
C27	NVHS0_SLVS_RX2_P	NVHS0_RX2_P	NVHS (PCIe x8) Receive 2+			
G26	NVHS0_TX2_N	NVHS0_TX2_N	NVHS (PCIe x8) Transmit 2-		Output	PCIe Diff Pair, AC-Coupled on carrier board
G27	NVHS0_TX2_P	NVHS0_TX2_P	NVHS (PCIe x8) Transmit 2+			
A27	NVHS0_SLVS_RX3_N	NVHS0_RX3_N	NVHS (PCIe x8) Receive 3-		Input	PCIe/SLVS Diff Pair, AC-Coupled on carrier board if PCIe & direct connect to device.
A26	NVHS0_SLVS_RX3_P	NVHS0_RX3_P	NVHS (PCIe x8) Receive 3+			
J27	NVHS0_TX3_N	NVHS0_TX3_N	NVHS (PCIe x8) Transmit 3-		Output	PCIe Diff Pair, AC-Coupled on carrier board
J26	NVHS0_TX3_P	NVHS0_TX3_P	NVHS (PCIe x8) Transmit 3+			
D29	NVHS0_SLVS_RX4_N	NVHS0_RX4_N	NVHS (PCIe x8) Receive 4-		Input	PCIe/SLVS Diff Pair, AC-Coupled on carrier board if PCIe & direct connect to device.
D28	NVHS0_SLVS_RX4_P	NVHS0_RX4_P	NVHS (PCIe x8) Receive 4+			
H29	NVHS0_TX4_N	NVHS0_TX4_N	NVHS (PCIe x8) Transmit 4-		Output	PCIe Diff Pair, AC-Coupled on carrier board
H28	NVHS0_TX4_P	NVHS0_TX4_P	NVHS (PCIe x8) Transmit 4+			
B28	NVHS0_SLVS_RX5_N	NVHS0_RX5_N	NVHS (PCIe x8) Receive 5-		Input	PCIe/SLVS Diff Pair, AC-Coupled on carrier board if PCIe & direct connect to device.
B29	NVHS0_SLVS_RX5_P	NVHS0_RX5_P	NVHS (PCIe x8) Receive 5+			
K28	NVHS0_TX5_N	NVHS0_TX5_N	NVHS (PCIe x8) Transmit 5-		Output	PCIe Diff Pair, AC-Coupled on carrier board
K29	NVHS0_TX5_P	NVHS0_TX5_P	NVHS (PCIe x8) Transmit 5+			
C30	NVHS0_SLVS_RX6_N	NVHS0_RX6_N	NVHS (PCIe x8) Receive 6-		Input	PCIe/SLVS Diff Pair, AC-Coupled on carrier board if PCIe & direct connect to device.
C31	NVHS0_SLVS_RX6_P	NVHS0_RX6_P	NVHS (PCIe x8) Receive 6+			
G30	NVHS0_TX6_N	NVHS0_TX6_N	NVHS (PCIe x8) Transmit 6-		Output	PCIe Diff Pair, AC-Coupled on carrier board
G31	NVHS0_TX6_P	NVHS0_TX6_P	NVHS (PCIe x8) Transmit 6+			

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
A31	NVHS0_SLVS_RX7_N	NVHS0_RX7_N	NVHS (PCIe x8) Receive 7-		Input	PCIe/SLVS Diff Pair, AC-Coupled on carrier board if PCIe & direct connect to device.
A30	NVHS0_SLVS_RX7_P	NVHS0_RX7_P	NVHS (PCIe x8) Receive 7+			
J31	NVHS0_TX7_N	NVHS0_TX7_N	NVHS (PCIe x8) Transmit 7-		Output	PCIe Diff Pair, AC-Coupled on carrier board
J30	NVHS0_TX7_P	NVHS0_TX7_P	NVHS (PCIe x8) Transmit 7+			

Table 17. Jetson Xavier PCIe Clock/Control Pin Descriptions

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
E14	PEX_CLK0_N	PEX_CLK0N	PCIe 0 Reference Clock– when Jetson Xavier is Root Port. Unused when Jetson Xavier used as Endpoint.	M.2 Key M Connector	Output	PCIe Diff Pair
E15	PEX_CLK0_P	PEX_CLK0P	PCIe 0 Reference Clock+ when Jetson Xavier is Root Port. Unused when used as Endpoint.		Output	
E11	PEX_L0_CLKREQ_N	PEX_L0_CLKREQ_N	PCIe 0 Clock Request. Input when Jetson Xavier is Root Port. Output when Jetson Xavier is Endpoint.		Input Output	CMOS – 1.8V
D10	PEX_L0_RST_N	PEX_L0_RST_N	PCIe 0 Reset. Output when Jetson Xavier is Root Port. Input when Jetson Xavier is Endpoint.		Output Input	CMOS – 1.8V
F17	PEX_CLK1_N	PEX_CLK1N	PCIe 1 Reference Clock–	eSATA Bridge	Output	PCIe Diff Pair
F16	PEX_CLK1_P	PEX_CLK1P	PCIe 1 Reference Clock+		Output	
D9	PEX_L1_CLKREQ_N	PEX_L1_CLKREQ_N	PCIe 1 Clock Request	Unused	Input	CMOS – 1.8V
B9	PEX_L1_RST_N	PEX_L1_RST_N	PCIe 1 Reset	eSATA Bridge	Output	CMOS – 1.8V
F21	PEX_CLK3_N	PEX_CLK3N	PCIe 3 Reference Clock–	M.2 Key E Connector	Output	Diff pair
F20	PEX_CLK3_P	PEX_CLK3P	PCIe 3 Reference Clock+		Output	
J10	PEX_L3_CLKREQ_N	PEX_L3_CLKREQ_N	PCIe 3 Clock Request		Input	CMOS – 1.8V
K9	PEX_L3_RST_N	PEX_L3_RST_N	PCIe 3 Reset		Output	CMOS – 1.8V
E22	PEX_CLK4_N	PEX_CLK4N	PCIe 4 Reference Clock–/+ when Jetson Xavier is Root Port. Unused when Jetson Xavier used as Endpoint.	Unused	Output	Diff pair
E23	PEX_CLK4_P	PEX_CLK4P			Output	
G8	PEX_L4_CLKREQ_N	PEX_L4_CLKREQ_N	PCIe 4 Clock Request. Input when Jetson Xavier is Root Port. Output when Jetson Xavier is Endpoint.		Input	CMOS – 1.8V
J9	PEX_L4_RST_N	PEX_L4_RST_N	PCIe 4 Reset. Output when Jetson Xavier is Root Port. Input when Jetson Xavier is Endpoint.		Output	CMOS – 1.8V
F25	PEX_CLK5_N	PEX_CLK5N	PCIe 5 Reference Clock–/+ when Jetson Xavier is Root Port. Unused when Jetson Xavier used as Endpoint.	PCIe x16 Connector	Output	Diff pair
F24	PEX_CLK5_P	PEX_CLK5P			Output	
C8	PEX_L5_CLKREQ_N	PEX_L5_CLKREQ_N	PCIe 5 Clock Request. Input when Jetson Xavier is Root Port. Output when Jetson Xavier is Endpoint.		Input	CMOS – 1.8V
H10	PEX_L5_RST_N	PEX_L5_RST_N	PCIe 5 Reset. Output when Jetson Xavier is Root Port. Input when Jetson Xavier is Endpoint.		Output	CMOS – 1.8V
A8	PEX_WAKE_N	PEX_WAKE_N	PCIe Wake	PCIe x16 Connector, M.2 Key E & M Conn.	Input	CMOS – 1.8V

Table 18. Jetson Xavier UFS & Miscellaneous USB Control Pin Descriptions

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
A6	UFS0_REF_CLK	UFS0_REF_CLK	UFS Reference Clock	Micro SD / UFS Card Socket	Output	CMOS – 1.2V
C6	UFS0_RST_N	UFS0_RST	UFS Reset	Micro SD / UFS Card Socket	Output	CMOS – 1.2V
A62	GPIO10	CAN1_WAKE	GPIO	USB PD Controller Interrupt	Bidir	CMOS – 3.3V
F54	GPIO22	USB_VBUS_EN0	GPIO	VDD_5V_SATA Load Switch Enable	Output	CMOS – 1.8V

Table 19. Xavier Module USB 3.1, PCIe & UFS Lane Mapping Configurations

Jetson Xavier Lanes			UPHY0	UPHY1	UPHY[5:2]	UPHY6	UPHY7	UPHY[9:8]	UPHY10	UPHY11	NVHS[7:0]
Avail. Outputs from Jetson Xavier											
USB 3.1	PCIe	UFS									
3	2 x1, 1 x2, 1 x4 & 1 x8	1 x1	PCIe x1 (C1)	USB 3.1 (P2)	PCIe x4 (C0)	USB 3.1 (P0)	PCIe x1 (C3)	PCIe x2 (C4)	UFS x1 (0)	USB 3.1 (P3)	PCIe x8 (C5)

6.1 USB

Figure 15 Simple USB Type A Connection Example

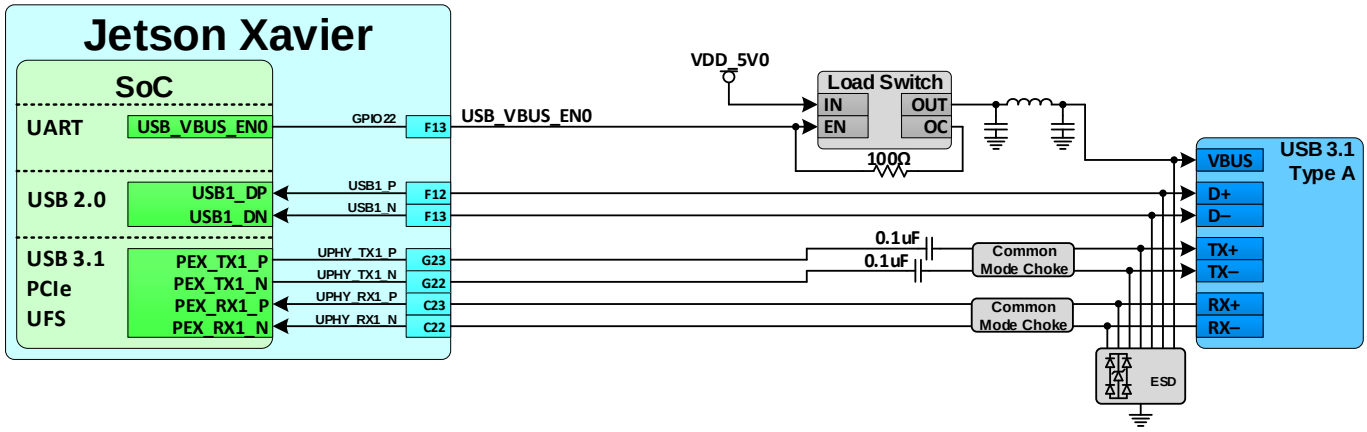
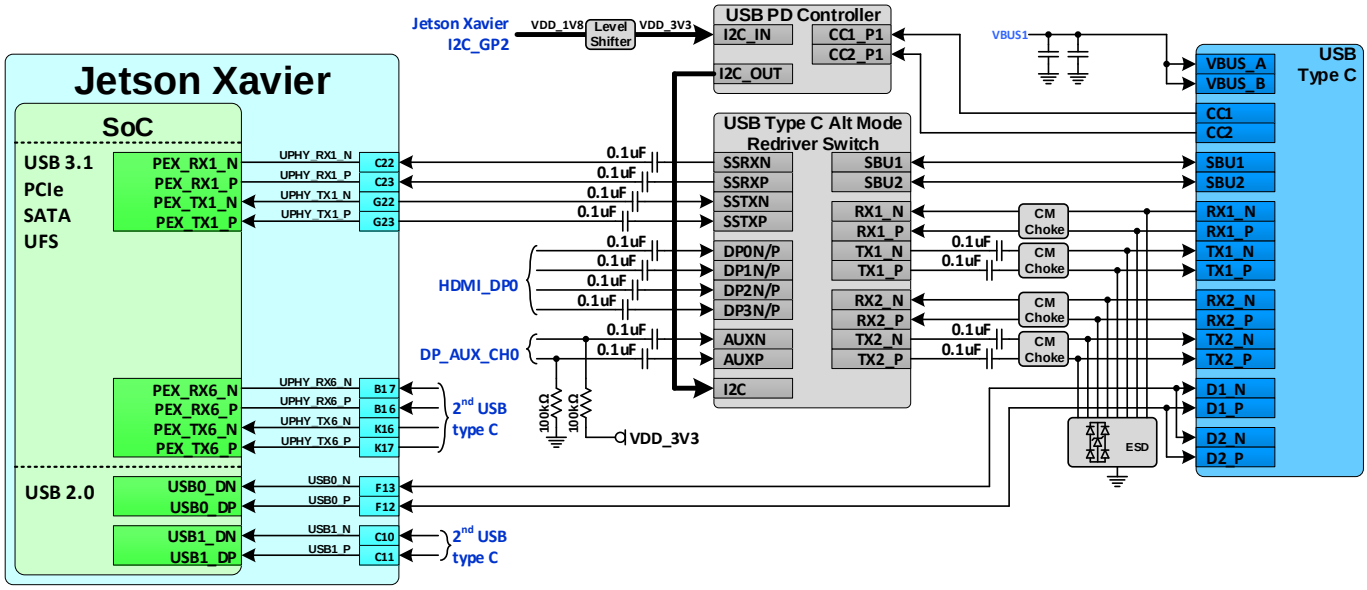
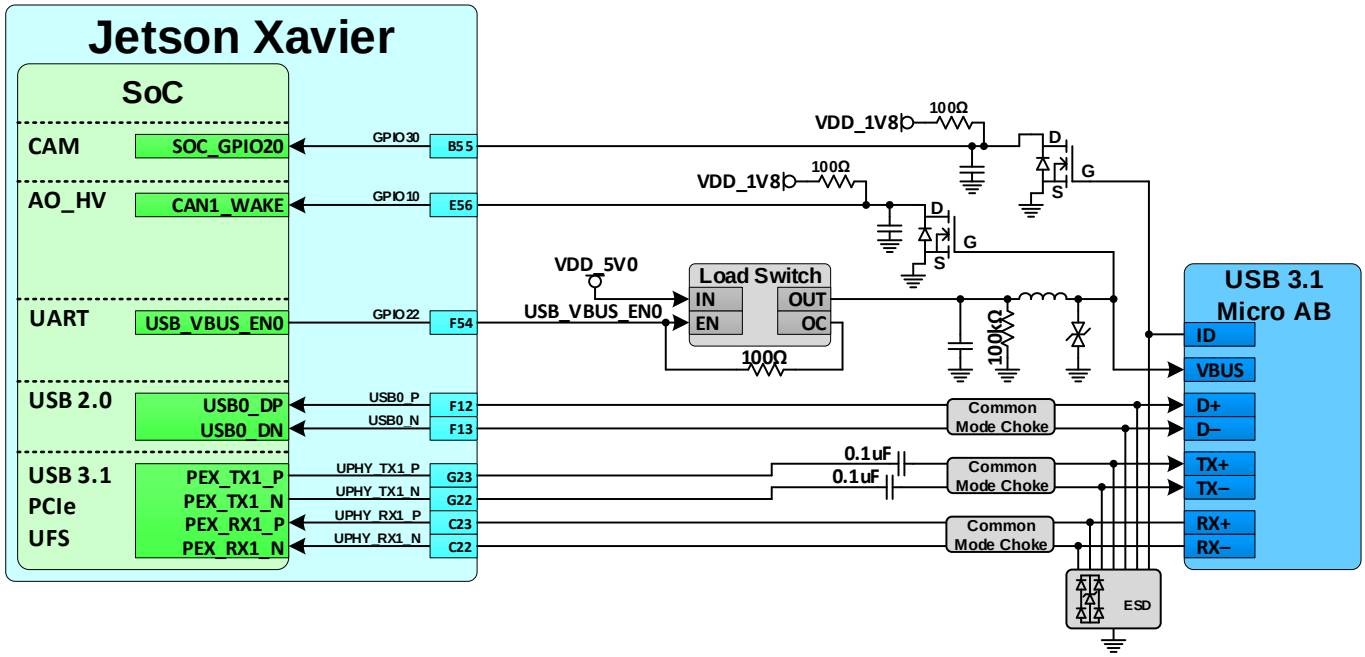


Figure 16 USB Type C Connection Example (from Jetson Xavier carrier board design)



Note: Type C connections are based on the Nvidia carrier board design. Additional interface assignments shown are also based on the carrier board usage.

Figure 17 USB 3.1 USB Micro AB Connection Example Supporting Device & Host Modes & USB 2.0 Recovery Mode.



USB 2.0 Design Guidelines

These requirements apply to the USB 2.0 controller PHY interfaces: **USB[3:0]_N/P**

Table 20. USB 2.0 Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Max Frequency (High Speed)	Bit Rate/UI period/Frequency	480/2.083/240	Mbps/ns/MHz	
Max Loading	High Speed / Full Speed / Low Speed	10 / 150 / 600	pF	
Reference plane		**GND**		
Trace Impedance	Diff pair / Single Ended	90 / 50	Ω	±15%
Via proximity (Signal to reference)		< 3.8 (24)	mm (ps)	See Note 2
Max Trace Delay	With CMC or SW (Microstrip / Stripline) Without CMC or SW (Microstrip / Stripline)	900/1050 (6) 1350/1575 (9)	ps (in)	Prop delay assumption: 175ps/in. for stripline, 150ps/in. for microstrip). See Note 3
Max Intra-Pair Skew between **USBx_D+** & **USBx_D–**		7.5	ps	

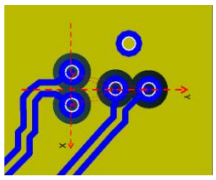
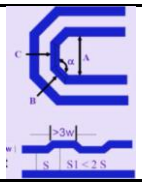
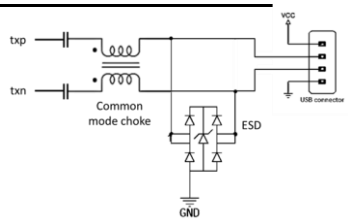
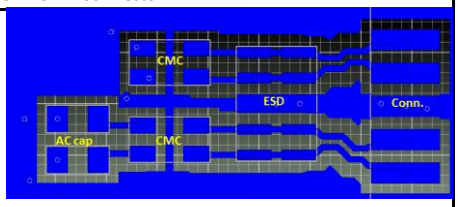
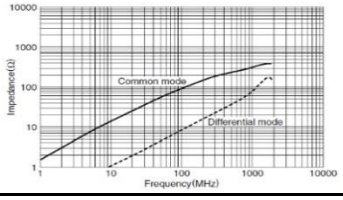
Note:
1. If portion of route is over a flex cable this length should be included in the Max Trace Delay/Length calculation & 85Ω Differential pair trace impedance is recommended.
2. Up to 4 signal Vias can share a single **GND** return Via.
3. CMC = Common-Mode-Choke. SW = Analog Switch
4. Adjustments to the USB drive strength, slew rate, termination value settings should not be necessary, but if any are made, they MUST be done as an offset to default values instead of overwriting those values.

USB 3.1 Design Guidelines

The following requirements apply to the USB 3.1 PHY interfaces

Table 21. USB 3.1 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI period GEN1 GEN2	5.0 / 200 10.0 / 100	Gbps / ps	Device mode supports GEN1 speed only.
Max Number of Loads	1	load	
Termination	90 differential	Ω	On-die termination at TX & RX
Electrical Specification			
Insertion Loss (IL)			
Host			
GEN1 (Type C)	≤ 2	dB	@ 2.5GHz
GEN1 (Type A)	≤ 7		@ 2.5GHz
GEN2 (Single role host mode)	TBD		@ 5GHz
Device			
GEN1 (Type C)	TBD		@ 2.5GHz
GEN1 (Micro AB)	≤ 1		@ 2.5GHz
GEN2 Host/GEN1 Device (dual role mode)	TBD		@ 5GHz (Host) / 2.5GHz (Device)
Resonance Dip Frequency	> 8	GHz	The resonance dip could be caused by a via stub for layer transition or trace stub for co-layout.
Time-domain Reflectometer (TDR) Dip GEN1 GEN2	75 75	Ω	@ Tr = 200ps (10%-90%) @ Tr = 61ps (10%-90%)
Near End Crosstalk (NEXT)	≤ −45	dB	DC – 5GHz per each TX-RX NEXT
Impedance			
Trace Impedance Diff pair / Single Ended	85 / 43	Ω	±15%. Intrinsic Zdf, does not account for coupling from other trace pairs
Reference plane	**GND**		
Trace Length/Skew			
Trace loss characteristic: GEN1 GEN2	< 0.7 TBD	dB/in	@ 2.5GHz. The following max length is derived based on this characteristic. The length constraint must be re-defined if loss characteristic is changed.
Breakout Region – Max length GEN1 GEN2	11 3	mm	Minimum trace width & spacing
Max Trace Length (Host)	152 (1014)	mm (ps)	
Max Trace Length (Device)	TBD		
Max Intra-Pair Skew (**RX/TX_N** to **RX/TX_P**)	0.15 (1)	mm (ps)	Do not perform length matching within breakout region. Trace length matching should be done before discontinuities. See Note 2
Differential pair uncoupled length	6.29 (41.9)	mm (ps)	
Trace Spacing for TX/RX Interleaving			
Trace Spacing (Microstrip / Stripline) Pair-Pair To Ref plane & SMT pad To unrelated high-speed signals	4x / 3x 4x / 3x 4x / 3x	Dielectric height	
Trace Spacing for TX/RX Non-interleaving			
TX-RX Xtalk is very critical in PCB trace routing. The ideal solution is to route TX and RX on different layers.			
If routing on the same layer, strongly recommend not interleaving TX and RX lanes			
If have to have interleaving routing in breakout, all the inter-pair spacing should follow the rule of inter-S_{NEXT} (between TX/RX pair spacing)			
The breakout trace width is suggested to be the minimum to increase inter-pair spacing			
Do not perform serpentine routing for intra-pair skew compensation in the breakout region			
Min Inter-S_{NEXT} (between TX/RX) Breakout Main-route	4.85x 3x	Dielectric height	This is the recommended dimensions for meeting the NEXT requirement. Stripline structure in a GSSG structure is assumed (holds in broadside-coupled stripline structure)
Max length Breakout Main-route	11 Max trace length - L_{BRK}	mm	
Via			
Via proximity (Signal via to GND return via)	< 3.8 (24)	mm (ps)	**See note 1**

Parameter		Requirement	Units	Notes
Topology		- Y-pattern is recommended - Keep symmetry		Y-pattern helps with Xtalk suppression. It can also reduce the limit of the pair-pair distance. Review needed (NEXT/FEXT check) if via placement does not use Y-pattern. 
GND via		Place **GND** via as symmetrically as possible to data pair vias. Up to 4 signal vias (2 diff pairs) can share a single **GND** return via		**GND** via is used to maintain return path, while its Xtalk suppression is limited
Max # of Vias	PTH vias Micro Vias	4 if all vias are PTH via Not limited as long as total channel loss meets IL spec		
Max Via Stub Length		0.4	mm	long via stub requires review (IL & resonance dip check)
Serpentine				
Min bend angle		135	deg (a)	
Dimension	Min A Spacing Min B, C Length Min Jog Width	4x 1.5x 3x	Trace width	S1 must be taken care in order to consider Xtalk to adjacent pair 
Additional Component Placement Order				
		Chip – AC capacitor (TX only) – common mode choke – ESD – Connector		
				
AC Cap				
Value	Min/Max	0.075 / 0.2	uF	Only required for TX pair when routed to connector
Location (max length to adjacent discontinuity)		8	mm	Discontinuity is connector, via, or component pad
Voiding		**GND/PWR** void under/above cap is preferred		Voiding is required if AC cap size is 0603 or larger
ESD				
Max Junction capacitance (IO to GND)		0.8	pF	e.g. SEMTECH RClamp0524p
Footprint		Pad should be on the net – not trace stub		
Location (max length to adjacent discontinuity)		8	mm	Discontinuity is connector, via, or component pad
Common-Mode Choke				
Common-mode impedance @ 100MHz Min/Max		65/90	Ω	TDK ACM2012D-900-2P
Max Rdc		0.3	Ω	
Differential TDR impedance		90	Ω @T_R-200ps (10%-90%)	
Min Sdd21 @ 2.5GHz		2.22	dB	
Max Scc21 @ 2.5GHz		19.2	dB	
Location		8	mm	Discontinuity is connector, via, or component pad
FPC (Additional length of Flexible Printed Circuit Board)				
The FPC routing should be included for PCB trace calculations (max length, etc.)				
Characteristic Impedance		Same as PCB		
Loss characteristic		Strongly recommend to be same as PCB or better		If worse than PCB, the PCB & FPC length must be re-estimated
Connector				
SMT Connector **GND** Voiding		**GND** plane under signal pad should be voided. Size of void should be the same size as the pad.		

Parameter	Requirement	Units	Notes
Connector used must be USB-IF certified			

Note:
1. Up to 4 signal Vias can share a single **GND** return Via
2. Include only PCB trace lengths/delays for Differential P/N matching. The SoC package delays for differential signal pairs are adequately matched.
3. Recommend trace length matching to <1ps before Vias or any discontinuity to minimize common mode conversion.
4. Place **GND** Vias as symmetrically as possible to data pair Vias.

Common USB Routing Guidelines

Guideline
If routing to USB device or USB connector includes a flex or 2nd PCB, the total routing including all PCBs/flexes must be used for the max trace & skew calculations.
Keep critical USB related traces away from other signal traces or unrelated power traces/areas or power supply components

Table 22. Jetson Xavier USB 2.0 Signal Connections

Jetson Xavier Ball Name	Type	Termination	Description
USB[3:0]_P **USB[3:0]_N**	DIFF I/O	90Ω common-mode chokes close to connector. ESD Protection between choke & connector on each line to GND	**USB Differential Data Pair:** Connect to USB connector, Mini-Card Socket, Hub or other device on the PCB.

Table 23. Jetson Xavier USB 3.1 Signal Connections

Jetson Xavier Pin Name	Type	Termination	Description
UPHY_TX6_N/P (USB 3.1 Port #0) **UPHY_TX1_N/P (USB 3.1 Port #2)** **UPHY_TX11_N/P (USB 3.1 Port #3)**	DIFF Out	Series 0.1uF caps. Common-mode chokes & ESD protection if these are used.	**USB 3.1 Differential Transmit Data Pairs:** Connect to USB 3.1 connectors, hubs or other devices on the PCB.
UPHY_RX6_N/P (USB 3.1 Port #0) **UPHY_RX1_N/P (USB 3.1 Port #2)** **UPHY_RX11_N/P (USB 3.1 Port #3)**	DIFF In	If routed directly to a peripheral on the board, AC caps are needed for the peripheral TX lines. Common-mode chokes & ESD protection, if these are used.	**USB 3.1 Differential Receive Data Pairs:** Connect to USB 3.1 connectors, hubs or other devices on the PCB.

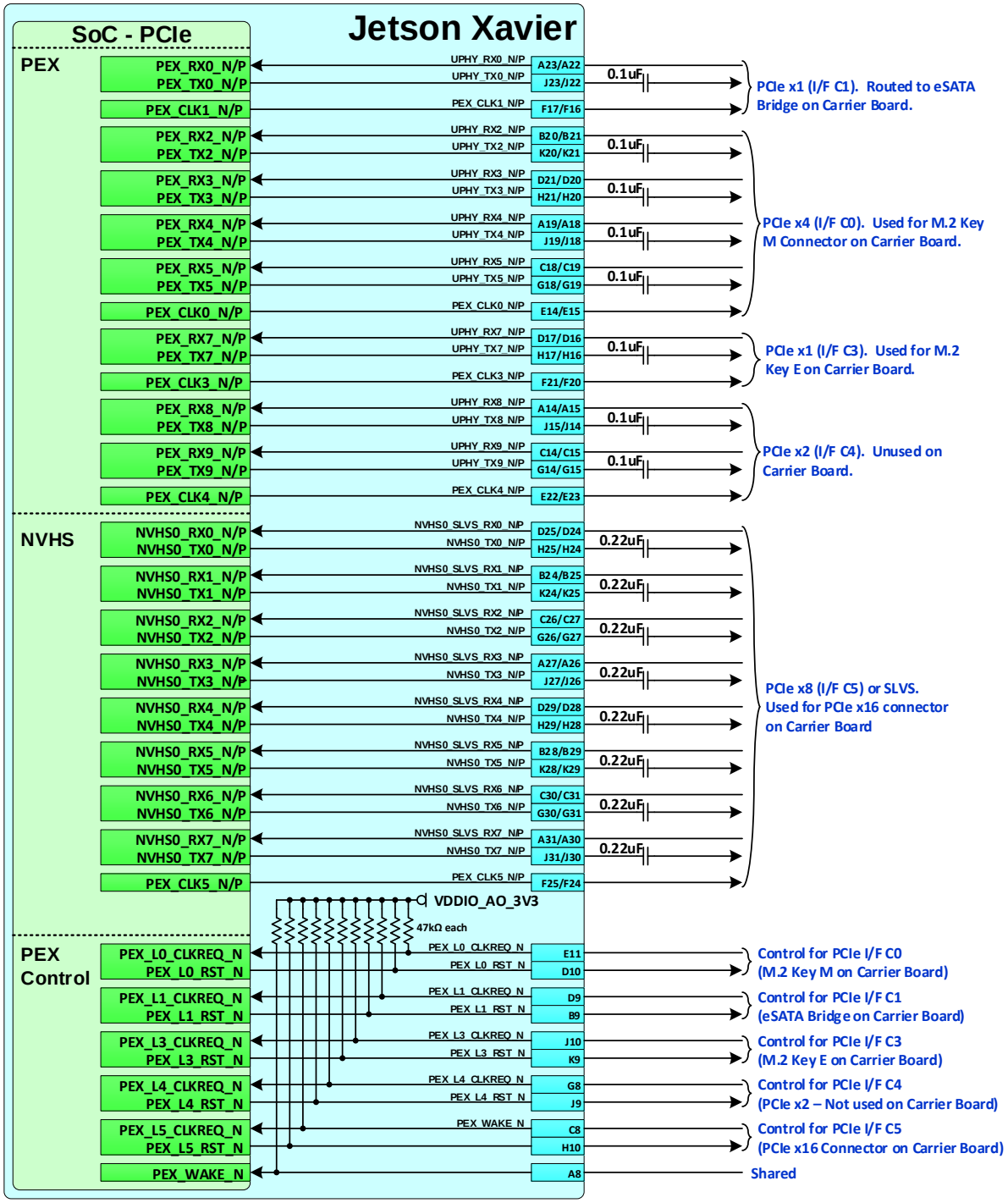
Table 24. Recommended USB observation (test) points for initial boards

Test Points Recommended	Location
One for each of the USB 2.0 data lines (**D+/-**)	Near Jetson Xavier connector & USB device. USB connector pins can serve as test points.
One for each of the USB 3.1 output lines used (**TXn_+/-**)	Near USB device. USB connector pins can serve as test points
One for each of the USB 3.1 input lines (**RX_+/-**)	Near Jetson Xavier connector.

6.2 PCIe

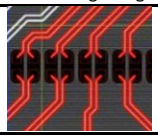
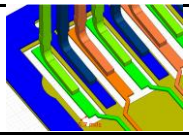
Jetson Xavier provides 16 lanes that can be used for PCIe, USB 3.1 & UFS. See the Jetson Xavier USB 3.1, PCIe & UFS Lane Mapping Configurations table for details on which are available for PCIe use. Root port is supported on all PCIe interfaces. End Point mode is supported on Interfaces C0, C4 & C5 only.

Figure 18. PCIe Connection Example



PCIe Design Guidelines (Up to GEN3)

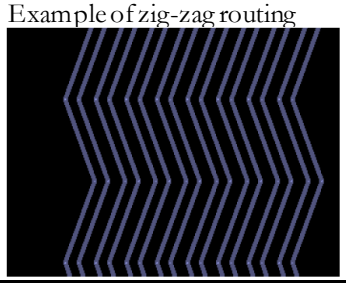
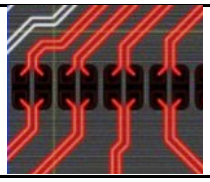
Table 25. PCIe Interface Signal Routing Requirements (Up to GEN3)

Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI Period	5.0 / 200	Gbps / ps	2.5GHz, half-rate architecture
Configuration / Device Organization	1	Load	
Topology	Point-point		Unidirectional, differential
Termination	50	Ω	To **GND** Single Ended for P & N
Impedance			
Trace Impedance differential / Single Ended	85 / 50	Ω	±15%. See note 1
Reference plane	**GND**		
Spacing			
Trace Spacing (Stripline/Microstrip) Pair – Pair To plane & capacitor pad To unrelated high-speed signals	3x / 4x 3x / 4x 3x / 4x	Dielectric	
Length/Skew			
Breakout region (Max Length)	41.9	ps	Minimum width and spacing. 4x or wider dielectric height spacing is preferred
Max trace length To PCIe Connector Stripline Microstrip Direct to PCIe Device Stripline Microstrip	 5.5 (979) 5.5 (825) 9 (1602) 9 (1250)	in (ps)	Assumption used is 178ps/in for Stripline routing & 150ps/in for Microstrip.
Max PCB via distance from the BGA	41.9	ps	Max distance from BGA ball to first PCB via.
PCB within pair (intra-pair) skew	0.15 (0.5)	mm (ps)	Do trace length matching before hitting discontinuities
Within pair (intra-pair) matching between subsequent discontinuities	0.15 (0.5)	mm (ps)	
Differential pair uncoupled length	41.9	ps	
Via			
Via placement	Place **GND** vias as symmetrically as possible to data pair vias. **GND** via distance should be placed less than 1x the diff pair via pitch		
Max # of Vias PTH Vias Micro-Vias	2 for TX traces & 2 for RX trace No requirement		
Max Via stub length	0.4	mm	Longer via stubs would require review
Routing signals over antipads	Not allowed		
AC Cap			
Value Min/Max	0.075 / 0.22	uF	Only required for TX pair when routed to connector
Location (max length to adjacent discontinuity)	8	mm	Discontinuity such as edge finger, component pad
Voiding	Voiding the plane directly under the pad 3-4 mils larger than the pad size is recommended.		
Serpentine (See USB 3.1 Guidelines)			
Connector			
Voiding	Voiding the plane directly under the pad 5.7 mils larger than the pad size is recommended.		
Keep critical PCIe traces such as PEX_TX/RX, TERMP etc. away from other signal traces or unrelated power traces/areas or power supply components			

Note:
1. The PCIe spec. has 40-60Ω absolute min/max trace impedance, which can be used instead of the 50Ω, ±15%.
2. If routing in the same layer is necessary, route group TX & RX separately without mixing RX/TX routes & keep distance between nearest TX/RX trace & RX to other signals 3x RX-RX separation.
3. For trace loss >= 0.7dB/in @ 2.5GHz, the max trace length should be 7 inches. To reduce trace loss, ensure the loss tangent of the dielectric material & roughness of the metal are tightly controlled.
4. The average of the differential signals is used for length matching.
5. Do length matching before Via transitions to different layers or any discontinuity to minimize common mode conversion.

PCIe GEN 4 Design Guidelines

Table 26. PCIe GEN 4 Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Data Rate / UI Period	16.0 / 62.5	Gbps / ps	8.0GHz, half-rate architecture
Topology	Point-point		Unidirectional, differential. Driven by 100MHz common reference clock
Termination	43	Ω	To **GND** Single Ended for P & N
Impedance			
Trace Impedance differential / Single Ended	85 / 50	Ω	±15%
Reference plane	**GND**		
Fiber-weave effect	- Use spread-glass (denser weave) instead of regular-glass (sparse weave) to minimize intra-pair skew - Use zig-zag route instead of straight to minimize skew, this is a mandatory for PCIe gen4 design		Example of zig-zag routing 
Spacing			
Trace Spacing (Stripline) Pair – Pair To plane & capacitor pad To unrelated high-speed signals	4x 4x 4x	Dielectric	
Length/Skew			
Breakout region (Max Length)	41.9	ps	Minimum width and spacing. 4x or wider dielectric height spacing is preferred
Max trace length To PCIe Connector Stripline Microstrip Direct to PCIe Device Stripline Microstrip	 4 (712) 4 (600) 9 (1602) 9 (1250)	in (ps)	Assumption used is 178ps/in for Stripline routing & 150ps/in for Microstrip.
Max PCB via distance from the Device/Connector	41.9	ps	Max distance from Device ball or Connector pin to first PCB via.
PCB within pair (intra-pair) skew	0.15 (0.5)	mm (ps)	Do trace length matching before hitting discontinuities.
Within pair (intra-pair) matching between subsequent discontinuities	0.15 (0.5)	mm (ps)	
Differential pair uncoupled length	41.9	ps	
Via			
Via placement	Place **GND** vias as symmetrically as possible to data pair vias. **GND** via distance should be placed less than 1x the diff pair via pitch		
Max # of Vias	4		Use micro via or back drilled via - no via stub allowed.
Max Via stub length	na		Not Allowed
AC Cap			
Value Min/Max	0.22	uF	20%, 0402 X5R or better. Only required for TX pair when routed to connector. Place close to TX side.
Voiding	Voiding the plane directly under the pad 3-4 mils larger than the pad size is required.		
Serpentine (See USB 3.1 Guidelines)			
Serpentine			
Min bend angle	135	deg (a)	

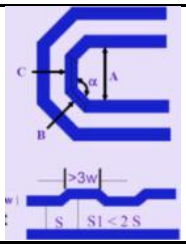
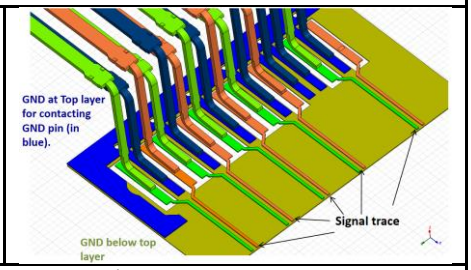
Dimension	Min A Spacing Min B, C Length Min Jog Width	4x 1.5x 3x	Trace width	S1 must be taken care in order to consider Xtalk to adjacent pair 
MIsc.				
GND fill rule		Remove unwanted GND fill that is either floating or act like antenna		
Connector				
Voiding		Void all layers of golden finger area under the pad 5.7 mils larger than the pad size is recommended.		
Keep critical PCIe traces such as PEX_TX/RX, TERMP etc. away from other signal traces or unrelated power traces/areas or power supply components				

Table 27. PCIe Signal Connections

Jetson Xavier Pin Name	Type	Termination	Description
PCIe Interface #C0 (x4 used for M.2 Key M on Carrier Board)			
UPHY_TX[5:2]_P/N	DIFF OUT	Series 0.1uF Capacitor	**Differential Transmit Data Pairs:** Connect to **TX_P/N** pins of PCIe connector or **RX_P/N** pin of PCIe device through AC caps.
UPHY_RX[5:2]_P/N	DIFF IN	Series 0.1uF capacitors if device on main PCB.	**Differential Receive Data Pairs:** Connect to **RX_P/N** pins of PCIe connector or **TX_P/N** pin of PCIe device through AC caps.
PEX_CLK0_P/N	DIFF OUT		**Differential Reference Clock Output:** Connect to **REFCLK_P/N** pins of PCIe device/connector
PEX_L0_CLKREQ_N	I/O	47KΩ pullups to **VDDIO_AO_3V3** on Jetson Xavier.	**PEX Clock Request for PEX_CLK0:** Connect to **CLKREQ** pin on device/connector.
PEX_L0_RST_N	O		**PEX Reset:** Connect to **PERST** pin on device/connector.
PCIe Interface #C1 (x1 used for eSATA bridge on Carrier Board)			
UPHY_TX0_P/N	DIFF OUT	Series 0.1uF Capacitor	**Differential Transmit Data Pairs:** Connect to **TX+/–** pins of PCIe connector or **RX_+/–** pin of PCIe device through AC caps.
UPHY_RX0_P/N	DIFF IN	Series 0.1uF capacitors if device on main PCB.	**Differential Receive Data Pairs:** Connect to **RX_+/–** pins of PCIe connector or **TX_+/–** pin of PCIe device through AC caps.
PEX_CLK1_P/N	DIFF OUT		**Differential Reference Clock Output**: Connect to **REFCLK_**+/– pins of PCIe device/connector.
PEX_L1_CLKREQ_N	I/O	47KΩ pullups to **VDDIO_AO_3V3** on Jetson Xavier.	**PEX Clock Request for PEX_CLK1:** Connect to **CLKREQ** pin on device/connector(s)
PEX_L1_RST_N	O		**PEX Reset:** Connect to **PERST** pin on device/connector.
PCIe Interface #C3 (x1 used for M.2 Key E on Carrier Board)			
UPHY_TX7_P/N	DIFF OUT	Series 0.1uF Capacitor	**Differential Transmit Data Pairs:** Connect to **TX_P/N** pins of PCIe connector or **RX_P/N** pin of PCIe device through AC caps.
UPHY_RX7_P/N	DIFF IN	Series 0.1uF capacitors if device on main PCB.	**Differential Receive Data Pairs:** Connect to **RX_P/N** pins of PCIe connector or **TX_P/N** pin of PCIe device through AC caps.
PEX_CLK3_P/N	DIFF OUT		**Differential Reference Clock Output:** Connect to **REFCLK_P/N** pins of PCIe device/connector
PEX_L3_CLKREQ_N	I/O	47KΩ pullups to **VDDIO_AO_3V3** on Jetson Xavier.	**PEX Clock Request for PEX_CLK3:** Connect to **CLKREQ** pin on device/connector.
PEX_L3_RST_N	O		**PEX Reset:** Connect to **PERST** pin on device/connector.
PCIe Interface #C4 (x2 – Not used on Carrier Board)			
UPHY_TX[9:8]_P/N	DIFF OUT	Series 0.1uF Capacitor	**Differential Transmit Data Pairs:** Connect to **TX_P/N** pins of PCIe connector or **RX_P/N** pin of PCIe device through AC caps.
UPHY_RX[9:8]_P/N	DIFF IN	Series 0.1uF capacitors if device on main PCB.	**Differential Receive Data Pairs:** Connect to **RX_P/N** pins of PCIe connector or **TX_P/N** pin of PCIe device through AC caps.
PEX_CLK4_P/N	DIFF OUT		**Differential Reference Clock Output:** Connect to **REFCLK_P/N** pins of PCIe device/connector.

PEX_L4_CLKREQ_N	I/O	47KΩ pullups to **VDDIO_AO_3V3** on Jetson Xavier.	**PEX Clock Request for PEX_CLK4:** Connect to **CLKREQ** pin on device/connector.
PEX_L4_RST_N	O		**PEX Reset:** Connect to **PERST** pin on device/connector.
PCIe Interface #C5 (x8 – Routed to lower 8 lanes of PCIe x16 connector)			
NVHS0_TX[7:0]_P/N	DIFF OUT	Series 0.1uF Capacitor	**Differential Transmit Data Pairs:** Connect to **TX_P/N** pins of PCIe connector or **RX_P/N** pin of PCIe device through AC caps.
NVHS0_SLVS_RX[7:0]_P/N	DIFF IN	Series 0.1uF capacitors if device on main PCB.	**Differential Receive Data Pairs:** Connect to **RX_P/N** pins of PCIe connector or **TX_P/N** pin of PCIe device through AC caps.
PEX_CLK5_P/N	DIFF OUT		**Differential Reference Clock Output:** Connect to **REFCLK_P/N** pins of PCIe device/connector.
PEX_L5_CLKREQ_N	I/O	47KΩ pullups to **VDDIO_AO_3V3** on Jetson Xavier.	**PEX Clock Request for PEX_CLK5:** Connect to **CLKREQ** pin on device/connector.
PEX_L5_RST_N	O		**PEX Reset:** Connect to **PERST** pin on device/connector.
PEX_WAKE_N	I	47KΩ pullup to **VDDIO_AO_3V3** on Jetson Xavier.	**PEX Wake:** Connect to **WAKE** pins on devices or connectors

Note: Check "Supported USB 3.1, PEX & UFS Interface Mappings" tables earlier in this section for PCIe IF mapping options.

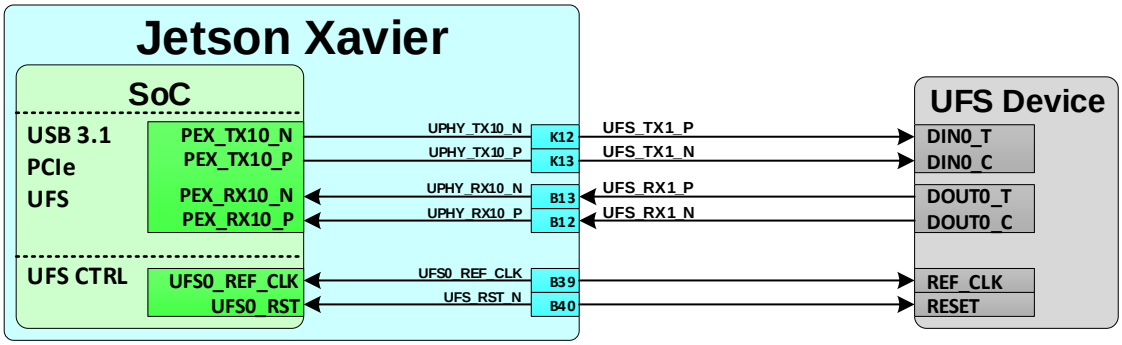
Table 28. Recommended PCIe observation (test) points for initial boards

Test Points Recommended	Location
One for each of the PCIe **TX_+/–** output lines used.	Near PCIe device. Connector pins may serve as test points if accessible.
One for each of the PCIe **RX_+/–** input lines used.	Near Jetson Xavier connector.

6.3 UFS

Jetson Xavier supports a x1 lane UFS interface.

Figure 19. UFS Connections Example



UFS Design Guidelines

Table 29. UFS Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Specification				
Max Rate	HS-GEAR1 (A-Series/B-Series) HS-GEAR2(A-Series/B-Series) HS-GEAR3(A-Series/B-Series)	1248 / 1457.6 2496 / 2915.2 4992 / 5830.4	Mbps	
Topology		Point-to-Point		Unidirectional, 100 ohm Differential
Max number of loads		1	Load	
Termination		100	Ω	Differential on die termination at TX/RX
Trace impedance				
Trace Impedance	differential / Single Ended	100 / 50	Ω	±15%
Reference plane		**GND**		
Spacing				
Trace Spacing (Stripline/Microstrip)	Pair – Pair To plane & capacitor pad To unrelated high-speed signals	3x / 4x 3x / 4x 3x / 4x	Dielectric	

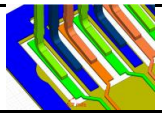
Parameter	Requirement	Units	Notes
Length/Width/Skew			
Breakout region (Max Length)	41.9	ps	Minimum width and spacing. 4x or wider dielectric height spacing is preferred
Max trace length Stripline Microstrip	4 (700) 4 (600)	In (ps)	PCB delays only.
Max PCB within pair (intra-pair) skew	0.15 (0.5)	mm (ps)	
Max Pair to Pair skew Tightly coupled case Nominally coupled case	33 100	ps	
Within pair (intra-pair) matching between subsequent discontinuities	0.15 (0.5)	mm (ps)	Do trace length matching before hitting discontinuities
Differential pair uncoupled length	41.9	ps	
Via			
Via placement	Place **GND** vias as symmetrically as possible to data pair vias. **GND** via distance should be placed less than 1x the diff pair via pitch		
Max # of Vias	2 for Through-Hole Vias		
Max Via stub length	0.4	mm	Longer via stubs would require review
Discontinuity			
Connector Voiding	Voiding the plane directly under the pad 5.7 mils larger than the pad size is recommended.		

Table 30. UFS Signal Connections

Ball Name (Function)	Type	Termination	Description
UPHY_TX10_P/N (UFS_TX0_P/N)	DIFF OUT		**Differential Transmit Data Pairs:** Connect to **DIN0_T/C** pins of UFS device
UFS0_REF_CLK	O		**UFS Reference Clock:** Connect to **REF_CLK** pin on device.
UFS0_RST	O		**UFS Reset:** Connect to **RST** pin on device

Note: Due to the power connections on the module, the SoC UFS sideband signal interface (UFS0_REF_CLK & UFS0_RST) supports 1.2V operation only. If higher voltage is required by the connected UFS device, level shifters will be needed.

7.0 GIGABIT ETHERNET

Jetson Xavier provides an RGMII interface to support GBit Ethernet functionality. The Ethernet PHY, magnetics & RJ45 connector are implemented on the Carrier board.

Table 31. Jetson Xavier Gigabit Ethernet Pin Descriptions

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
J5	ENET_INT	SOC_GPIO08	Ethernet Interrupt	Ethernet PHY	Input	CMOS – 1.8V
H5	ENET_RST_N	SOC_GPIO09	Ethernet Reset	Ethernet PHY	Output	CMOS – 1.8V
C4	RGMII_RD0	EQOS_RD0	Ethernet Receive data bit 0	Ethernet PHY	Input	CMOS – 1.8V
K6	RGMII_RD1	EQOS_RD1	Ethernet Receive data bit 1	Ethernet PHY	Input	CMOS – 1.8V
H6	RGMII_RD2	EQOS_RD2	Ethernet Receive data bit 2	Ethernet PHY	Input	CMOS – 1.8V
E5	RGMII_RD3	EQOS_RD3	Ethernet Receive data bit 3	Ethernet PHY	Input	CMOS – 1.8V
D5	RGMII_RX_CTL	EQOS_RX_CTL	Ethernet Receive Control	Ethernet PHY	Input	CMOS – 1.8V
C5	RGMII_RXC	EQOS_RXC	Ethernet Receive Clock	Ethernet PHY	Input	CMOS – 1.8V
E6	RGMII_SMA_MDC	EQOS_SMA_MDC	Ethernet Management Clock	Ethernet PHY	Output	CMOS – 1.8V
E7	RGMII_SMA_MDIO	EQOS_SMA_MDIO	Ethernet Management Data	Ethernet PHY	Bidir	CMOS – 1.8V
J6	RGMII_TD0	EQOS_TD0	Ethernet Transmit data bit 0	Ethernet PHY	Output	CMOS – 1.8V
G5	RGMII_TD1	EQOS_TD1	Ethernet Transmit data bit 1	Ethernet PHY	Output	CMOS – 1.8V
J7	RGMII_TD2	EQOS_TD2	Ethernet Transmit data bit 2	Ethernet PHY	Output	CMOS – 1.8V
G6	RGMII_TD3	EQOS_TD3	Ethernet Transmit data bit 3	Ethernet PHY	Output	CMOS – 1.8V
K7	RGMII_TX_CTL	EQOS_TX_CTL	Ethernet Transmit Control	Ethernet PHY	Output	CMOS – 1.8V
B5	RGMII_TXC	EQOS_TXC	Ethernet Transmit Clock	Ethernet PHY	Output	CMOS – 1.8V

Figure 20. Ethernet Connections

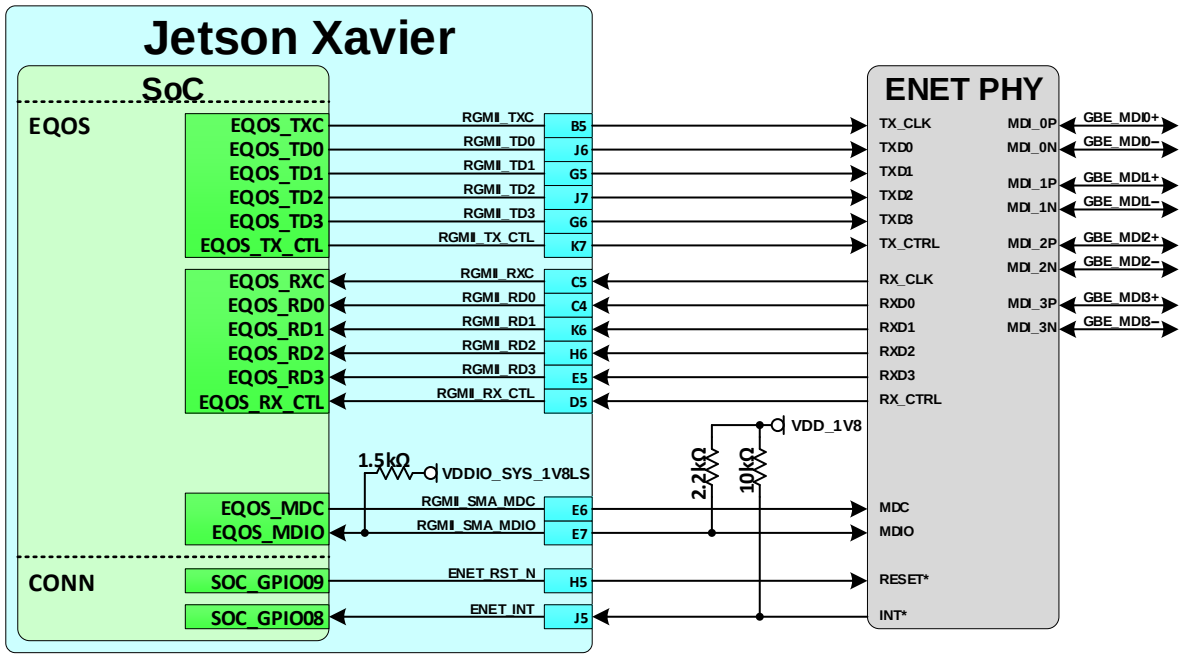
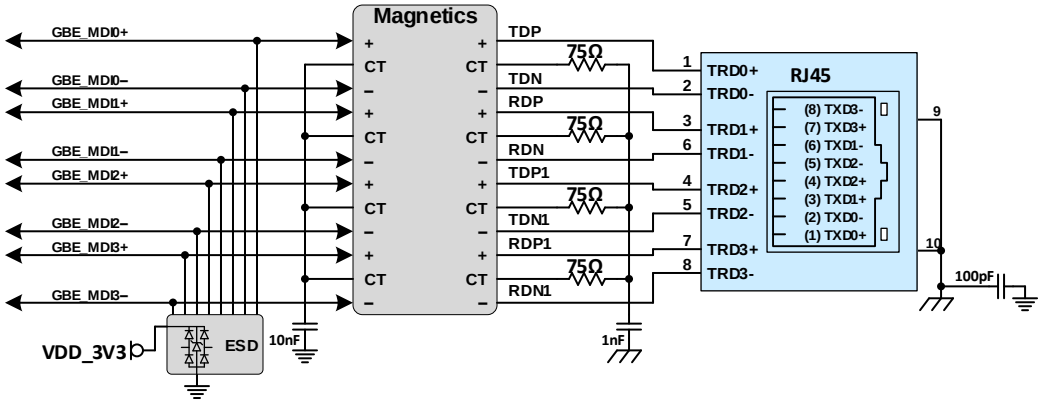


Figure 21. Gigabit Ethernet Magnetics & RJ45 Connections



Note: The connections above match those used on the carrier board and are shown for reference.

Table 32. RGMII Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency	125	MHz	
Topology	Point to point		Unidirectional, source terminated, source synchronous
Reference plane	**GND** or **PWR**		See note 1
Max PCB breakout delay	5 (30)	mm (ps)	
Trace Impedance	45-50	Ω	±15%
Via proximity (Signal via to GND return via)	< 3.8 (24)	mm (ps)	See note 2
Trace spacing Microstrip / Stripline	4x / 3x	dielectric	
Max Trace Length/Delay	175 (1200)	mm (ps)	See Note 3
Max Trace Delay Skew Between Clock & Data	4.8 (30)	mm (ps)	See Note 3
Isolation of TX and RX CLK signals	One of the following options for **TX_CLK** and **RX_CLK** signals: 1. **GND** shielding from each other and any other signal, or 2. >5x spacing from each other and any other signal, or 3. Routed on separate layers from each other and any other signal		
Isolation of TX and RX groups	One of the following options for **TX** signal and **RX** signal groups: 1. **GND** shielding from each other, or 2. >5x spacing from each other, or 3. Routed on separate layers from each other		
Noise Coupling Avoidance	Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components		

Notes:
1. If **PWR**, add 2x 0201 100nF & 2x 0402 4.7uF decoupling capacitors between **PWR** & **GND** for return current
2. Up to 4 signal Vias can share a single **GND** return Via
3. Include Package & PCB routing delays for Max trace delays and max trace delay skew parameters.

Table 33. Ethernet MDI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Reference plane	**GND**		
Trace Impedance Diff pair / Single Ended	100 / 50	Ω	±15%. Differential impedance target is 100Ω. 90Ω can be used if 100Ω is not achievable
Min Trace Spacing (Pair-Pair)	0.763	mm	
Max Trace Length	109 (690)	mm (ps)	
Max Within Pair (Intra-Pair) Skew	0.15 (1)	mm (ps)	
Number of Vias	minimum		Ideally there should be no vias, but if required for breakout to Ethernet controller or magnetics, keep very close to either device.

Table 34. Ethernet Signal Connections

Jetson Xavier Pin Name	Type	Termination	Description
RGMII_TXC	O		**RGMI Transmit Clock: Connect to TXCLK pin on GbE Transceiver.**
RGMII_TD[3:0]	O		**RGMI Transmit Data: Connect to TXD[3:0] pins on GbE Transceiver.**
RGMII_TX_CTL	O		**RGMI Transmit Control: Connect to TXEN pin on GbE Transceiver.**
RGMII_RXC	I		**RGMI Receive Clock: Connect to RXCLK pin on GbE Transceiver.**
RGMII_RD[3:0]	I		**RGMI Receive Data: Connect to RXD[3:0] pins on GbE Transceiver.**
RGMII_RX_CTL	I		**RGMI Receive Control: Connect to RXDV pin on GbE Transceiver.**
RGMII_MDC	O		**MDC: Connect to MDC pin on GbE Transceiver.**
RGMII_MDIO	I/O	2.2kΩ pull-up to VDD_1V8	**MDIO: Connect to MDIO pin on GbE Transceiver.**
ENET_RST_N	O		**Ethernet Reset: Connect to Reset input on Ethernet PHY.**
ENET_INT	I	10kΩ pull-up to VDD_1V8	**Ethernet Interrupt: Connect to Interrupt output on Ethernet PHY.**
GBE_MDI[3:0]+/–	DIFF I/O	ESD device to GND per signal	**Gigabit Ethernet MDI IF Pairs:** Connect to Magnetics +/– pins

Table 35. Recommended Gigabit Ethernet observation (test) points for initial boards

Test Points Recommended	Location
One for each of the RGMII lines.	
One for each of the **MDI[3:0]+/–** lines.	Near Jetson Xavier connector & Magnetics device.

8.0 DISPLAY

Jetson Xavier includes three interfaces (HDMI_DP[2:0]). Each can support eDP / DP or HDMI. See the Jetson Xavier Data Sheet for the maximum resolutions supported.

Table 36. Jetson Xavier HDMI / eDP / DP Pin Descriptions

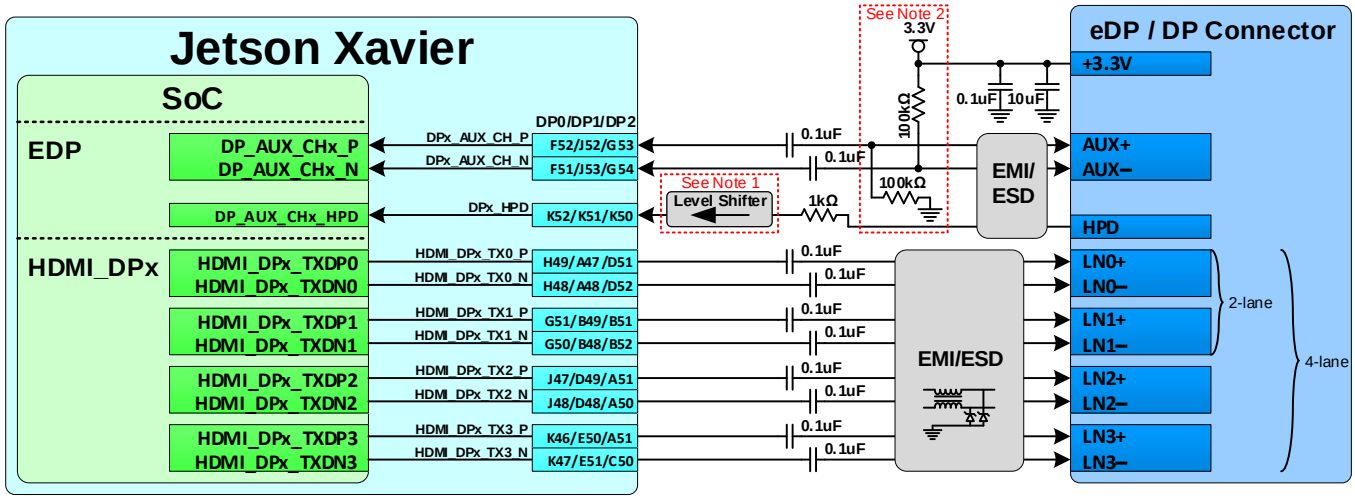
Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
H48	HDMI_DP0_TX0_N	HDMI_DP0_TXDN0	DisplayPort 0 Lane 0– or HDMI Lane 2–	USB Type C Conn. J512 (via Alt Mode Switch)	Output	Diff pair, AC-Coupled on carrier board
H49	HDMI_DP0_TX0_P	HDMI_DP0_TXDP0	DisplayPort 0 Lane 0+ or HDMI Lane 2+		Output	
G50	HDMI_DP0_TX1_N	HDMI_DP0_TXDN1	DisplayPort 0 Lane 1– or HDMI Lane 1–		Output	Diff pair, AC-Coupled on carrier board
G51	HDMI_DP0_TX1_P	HDMI_DP0_TXDP1	DisplayPort 0 Lane 1+or HDMI Lane 1+		Output	
J48	HDMI_DP0_TX2_N	HDMI_DP0_TXDN2	DisplayPort 0 Lane 2– or HDMI Lane 0–		Output	Diff pair, AC-Coupled on carrier board
J47	HDMI_DP0_TX2_P	HDMI_DP0_TXDP2	DisplayPort 0 Lane 2+ or HDMI Lane 0+		Output	
K47	HDMI_DP0_TX3_N	HDMI_DP0_TXDN3	DisplayPort 0 Lane 3– or HDMI Clk Lane–		Output	Diff pair, AC-Coupled on carrier board
K46	HDMI_DP0_TX3_P	HDMI_DP0_TXDP3	DisplayPort 0 Lane 3+ or HDMI Clk Lane+		Output	
F51	DP0_AUX_CH_N	DP_AUX_CH0_N	Display Port 0 Aux– or HDMI DDC SDA		Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC/I2C)
F52	DP0_AUX_CH_P	DP_AUX_CH0_P	Display Port 0 Aux+ or HDMI DDC SCL		Bidir	
K52	DP0_HPD	DP_AUX_CH0_HPD	Display Port/HDMI 0 Hot Plug Detect		Input	CMOS – 1.8V
A48	HDMI_DP1_TX0_N	HDMI_DP1_TXDN0	DisplayPort 1 Lane 0– or HDMI Lane 2–	USB Type C Conn. J513 (via Alt Mode Switch)	Output	Diff pair, AC-Coupled on carrier board
A47	HDMI_DP1_TX0_P	HDMI_DP1_TXDP0	DisplayPort 1 Lane 0+ or HDMI Lane 2+		Output	
B48	HDMI_DP1_TX1_N	HDMI_DP1_TXDN1	DisplayPort 1 Lane 1– or HDMI Lane 1–		Output	Diff pair, AC-Coupled on carrier board
B49	HDMI_DP1_TX1_P	HDMI_DP1_TXDP1	DisplayPort 1 Lane 1+ or HDMI Lane 1+		Output	
D48	HDMI_DP1_TX2_N	HDMI_DP1_TXDN2	DisplayPort 1 Lane 2– or HDMI Lane 0–		Output	Diff pair, AC-Coupled on carrier board
D49	HDMI_DP1_TX2_P	HDMI_DP1_TXDP2	DisplayPort 1 Lane 2+ or HDMI Lane 0+		Output	
E51	HDMI_DP1_TX3_N	HDMI_DP1_TXDN3	DisplayPort 1 Lane 3– or HDMI Clk Lane–		Output	Diff pair, AC-Coupled on carrier board
E50	HDMI_DP1_TX3_P	HDMI_DP1_TXDP3	DisplayPort 1 Lane 3+ or HDMI Clk Lane+		Output	
J53	DP1_AUX_CH_N	DP_AUX_CH1_N	Display Port 1 Aux– or HDMI DDC SDA		Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC/I2C)
J52	DP1_AUX_CH_P	DP_AUX_CH1_P	Display Port 1 Aux+ or HDMI DDC SCL		Bidir	
K51	DP1_HPD	DP_AUX_CH1_HPD	Display Port/HDMI 1 Hot Plug Detect		Input	CMOS – 1.8V
D52	HDMI_DP2_TX0_N	HDMI_DP2_TXDN0	DisplayPort 2 Lane 0– or HDMI Lane 2–	HDMI Connector	Output	Diff pair, AC-Coupled on carrier board
D51	HDMI_DP2_TX0_P	HDMI_DP2_TXDP0	DisplayPort 2 Lane 0+ or HDMI Lane 2+		Output	
B52	HDMI_DP2_TX1_N	HDMI_DP2_TXDN1	DisplayPort 2 Lane 1– or HDMI Lane 1–		Output	Diff pair, AC-Coupled on carrier board
B51	HDMI_DP2_TX1_P	HDMI_DP2_TXDP1	DisplayPort 2 Lane 1+ or HDMI Lane 1+		Output	
A50	HDMI_DP2_TX2_N	HDMI_DP2_TXDN2	DisplayPort 2 Lane 2– or HDMI Lane 0–		Output	Diff pair, AC-Coupled on carrier board
A51	HDMI_DP2_TX2_P	HDMI_DP2_TXDP2	DisplayPort 2 Lane 2+ or HDMI Lane 0+		Output	
C50	HDMI_DP2_TX3_N	HDMI_DP2_TXDN3	DisplayPort 2 Lane 3– or HDMI Clk Lane–		Output	Diff pair, AC-Coupled on carrier board
C51	HDMI_DP2_TX3_P	HDMI_DP2_TXDP3	DisplayPort 2 Lane 3+ or HDMI Clk Lane+		Output	
G54	DP2_AUX_CH_N	DP_AUX_CH2_N	Display Port 2 Aux– or HDMI DDC SDA		Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC/I2C)
G53	DP2_AUX_CH_P	DP_AUX_CH2_P	Display Port 2 Aux+ or HDMI DDC SCL		Bidir	
K50	DP2_HPD	DP_AUX_CH2_HPD	Display Port/HDMI 2 Hot Plug Detect		Input	CMOS – 1.8V
J50	HDMI_CEC	HDMI_CEC	HDMI CEC		Bidir	Open Drain, 1.8V

Table 37. DP/HDMI Pin Mapping

Jetson Xavier Pin Name	Jetson Xavier Pin #s	SoC Pin Name	SoC Pin #s	HDMI	DP
HDMI_DP0					
HDMI_DP0_TX0_P HDMI_DP0_TX0_N	H49 H48	HDMI_DP0_TXDP0 HDMI_DP0_TXDN0	C44 D44	TXD2_P TXD2_N	TXD0_P TXD0_N
HDMI_DP0_TX1_P HDMI_DP0_TX1_N	G51 G50	HDMI_DP0_TXDP1 HDMI_DP0_TXDN1	D43 E43	TXD1_P TXD1_N	TXD1_P TXD1_N
HDMI_DP0_TX2_P HDMI_DP0_TX2_N	J47 J48	HDMI_DP0_TXDP2 HDMI_DP0_TXDN2	C42 D42	TXD0_P TXD0_N	TXD2_P TXD2_N
HDMI_DP0_TX3_P HDMI_DP0_TX3_N	K46 K47	HDMI_DP0_TXDP3 HDMI_DP0_TXDN3	A41 A42	TXC_P TXC_N	TXD3_P TXD3_N
HDMI_DP1					
HDMI_DP1_TX0_P HDMI_DP1_TX0_N	A47 A48	HDMI_DP1_TXDP0 HDMI_DP1_TXDN0	F41 G41	TXD2_P TXD2_N	TXD0_P TXD0_N
HDMI_DP1_TX1_P HDMI_DP1_TX1_N	B49 B48	HDMI_DP1_TXDP1 HDMI_DP1_TXDN1	H40 G40	TXD1_P TXD1_N	TXD1_P TXD1_N
HDMI_DP1_TX2_P HDMI_DP1_TX2_N	D49 D48	HDMI_DP1_TXDP2 HDMI_DP1_TXDN2	J41 K41	TXD0_P TXD0_N	TXD2_P TXD2_N
HDMI_DP1_TX3_P HDMI_DP1_TX3_N	E50 E51	HDMI_DP1_TXDP3 HDMI_DP1_TXDN3	H42 J42	TXC_P TXC_N	TXD3_P TXD3_N
HDMI_DP2					
HDMI_DP2_TX0_P HDMI_DP2_TX0_N	D51 D52	HDMI_DP2_TXDP0 HDMI_DP2_TXDN0	F45 G45	TXD2_P TXD2_N	TXD0_P TXD0_N
HDMI_DP2_TX1_P HDMI_DP2_TX1_N	B51 B52	HDMI_DP2_TXDP1 HDMI_DP2_TXDN1	F44 G44	TXD1_P TXD1_N	TXD1_P TXD1_N
HDMI_DP2_TX2_P HDMI_DP2_TX2_N	A51 A50	HDMI_DP2_TXDP2 HDMI_DP2_TXDN2	H43 G43	TXD0_P TXD0_N	TXD2_P TXD2_N
HDMI_DP2_TX3_P HDMI_DP2_TX3_N	C51 C50	HDMI_DP2_TXDP3 HDMI_DP2_TXDN3	G42 F42	TXC_P TXC_N	TXD3_P TXD3_N

8.1.1 DP/eDP

Figure 22: DP / eDP Connection Example



Note:
1. A Level shifter is required on HPD to avoid the pin from being driven when Jetson Xavier is off. The level shifter must be non-inverting (preserve the polarity of the HPD signal from the display).
2. Pull-up/down only required for DP – not for eDP.
3. If EMI devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing & electrical requirements of the DisplayPort specification for the modes to be supported. Any ESD solution must also maintain signal integrity & meet the DisplayPort requirements for the modes to be supported.

DP / eDP Routing Guidelines

Figure 23: DP / eDP (Differential Main Link) Topology

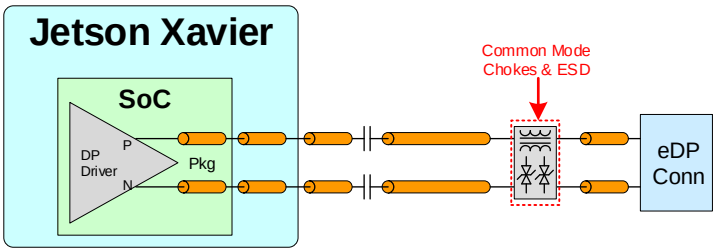
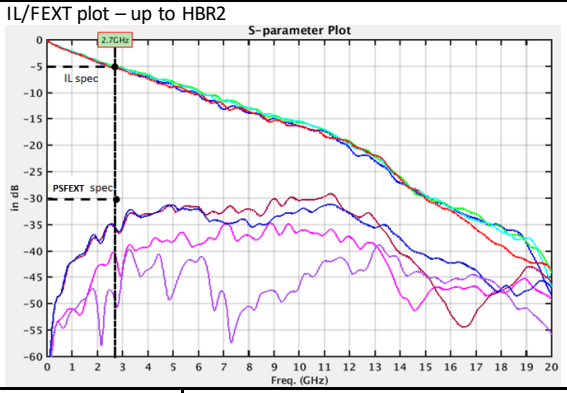
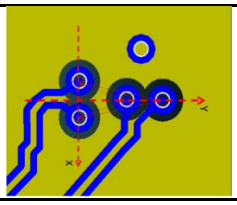
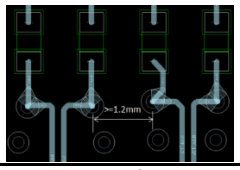


Table 38. DP/ eDP Main Link Signal Routing Requirements (Including DP_AUX)

Parameter		Requirement	Units	Notes
Specification				
Max Data Rate / Min UI	HBR2 HBR RBR	5.4 / 185 2.7 / 370 1.62 / 617	Gbps / ps	Per data lane
Number of Loads / Topology		1	load	Point-Point, Differential, Unidirectional
Termination		100	Ω	On die at TX/RX
Electrical Spec				
Insertion Loss	**E-HBR** @ 0.675GHz **PBR** 0.68GHz **HBR** 1.35GHz **HBR2** @ 2.7GHz	<=0.7 <=0.7 <=1.2 <=2.4	dB dB dB dB	
Resonance dip frequency		>8	GHz	
TDR dip		>85	Ω	@ Tr-200ps (10%-90%)
FEXT	@ DC @ 2.7GHz	<= -40dB <= -30dB	IL/FEXT plot – up to HBR2 	
Impedance				
Trace Impedance	Diff pair	100 90 85	Ω (±10%)	- 100Ω is the spec. target. 95/85Ω are implementation options (Zdiff does not account for trace coupling) - 95Ω should be used to support DP-HDMI co-lay out as HDMI 2.0 requires 100Ω impedance (see HDMI section for addition of series resistor R_S). - 85Ω can be used if eDP/DP only & is preferable as it can provide better trace loss characteristic performance. See Note 1.
Reference Plane		**GND**		
Trace Length, Spacing & Skew				
Trace loss characteristic @ 2.7GHz		< 0.81	dB/in	The following max length is derived based on this characteristic. The length constraint must be re-defined if loss characteristic is changed.
Max PCB Via dist. from module conn.	**RBR/HBR** **HBR2**	No requirement 7.63 (0.3)	mm (in)	
Max trace length from module to connector	**RBR/HBR** (Stripline / Microstrip) **HBR2** (Stripline)	215 (1137.5)/(975) 101.6 (700)	mm (ps)	175ps/inch assumption for Stripline, 150ps/inch for Microstrip.

Parameter		Requirement	Units	Notes
HBR2 (Microstrip, 5x / 7x)		89 (525) / 101.6 (600)		
Trace spacing (Pair-Pair)	Stripline	3x	dielectric	
	Microstrip (**HBR/RBR**)	4x		
	Microstrip (**HBR2**)	5x to 7x		
Trace spacing (Main Link to AUX)	Stripline/Microstrip	3x / 5x	dielectric	
Max Intra-pair (within pair) Skew		0.15 (1)	mm (ps)	- Do not perform length matching within breakout region - Do trace length matching before hitting discontinuity (i.e. matching to <1ps before the vias or any discontinuity to minimize common mode conversion).
Max Inter-pair (pair-pair) Skew		150	ps	
Via				
Max **GND** transition Via distance		< 1x	diff pair pitch	For signals switching reference layers, add symmetrical **GND** stitching Via near signal Vias.
Via Structure				
Impedance dip		≥97 ≥92	Ω @ 200ps Ω @ 35ps	The via dimension must be required for the HDMI-DP co-layout condition.
Recommended via dimension for impedance control	Drill/Pad	200/400	um	
	Antipad	>840	um	
	Via pitch	≥880	um	
Topology		- Y-pattern is recommended - keep symmetry Xtalk suppression is best using the Y-pattern. It can also reduce the limit of pair-pair distance.		
		For in-line via, the distance from a via of one lane to the adjacent via from other lane >= 1.2mm center-center.		
GND via		Place **GND** via as symmetrically as possible to data pair vias. Up to 4 signal vias (2 diff pairs) can share a single **GND** return via		**GND** via is used to maintain return path, while its Xtalk suppression is limited
Max # of Vias	PTH vias	4 if all vias are PTH via		
	Micro Vias	Not limited as long as total channel loss meets IL spec		
Max Via Stub Length		0.4	mm	
Serpentine (See USB 3.1 Guidelines)				
AC Cap				
Value		0.1	uF	Discrete 0402
Max Dist. from AC cap to connector	**RBR/HBR**	No requirement		
	HBR2	0.5	in	
Voiding	**RBR/HBR**	No requirement		**HBR2**: Voiding the plane directly under the pad 3-4 mils larger than the pad size is recommended.
	HBR2	Voiding required		
Connector				
Voiding	**RBR/HBR**	No requirement		**HBR2:** Standard DP Connector: Voiding requirement is stack-up dependent. For typical stack-ups, voiding on the layer under the connector pad is required to be 5.7mil larger than the connector pad.
	HBR2	Voiding required		
Keep critical eDP related traces including differential clock/data traces & **RSET** trace away from other signal traces or unrelated power traces/areas or power supply components				

Notes: 1. For eDP/DP, the spec puts a higher priority on the trace loss characteristic than on the impedance. However, before selecting 85Ω for impedance, it is important to make sure the selected stack-up, material & trace dimension can achieve the needed low loss characteristic.

2. The average of the differential signals is used for length matching.
3. Do not perform length matching within breakout region. Recommend doing trace length matching to <1ps before Vias or any discontinuity to minimize common mode conversion

Table 39. DP/eDP Signal Connections

Jetson Xavier Pin Name	Type	Termination	Description
HDMI_DPx_TX[3:0]_P/N	O	Series 0.1uF capacitors on all lines	**DP/eDP Differential CLK/Data Lanes:** Connect to matching pins on display connector. See DP/HDMI Pin Mapping & connection diagram for details.
DPx_AUX_CH_P/N	I/OD	Series 0.1uF capacitors	**DP/eDP: Auxiliary Channels**: Connect to **AUX_CH**+/– on display connector.
DPx_HPD	I		**DP/eDP: Hot Plug Detect**: Connect to **HPD** pin on display connector.

Table 40. Recommended eDP/DP observation (test) points for initial boards

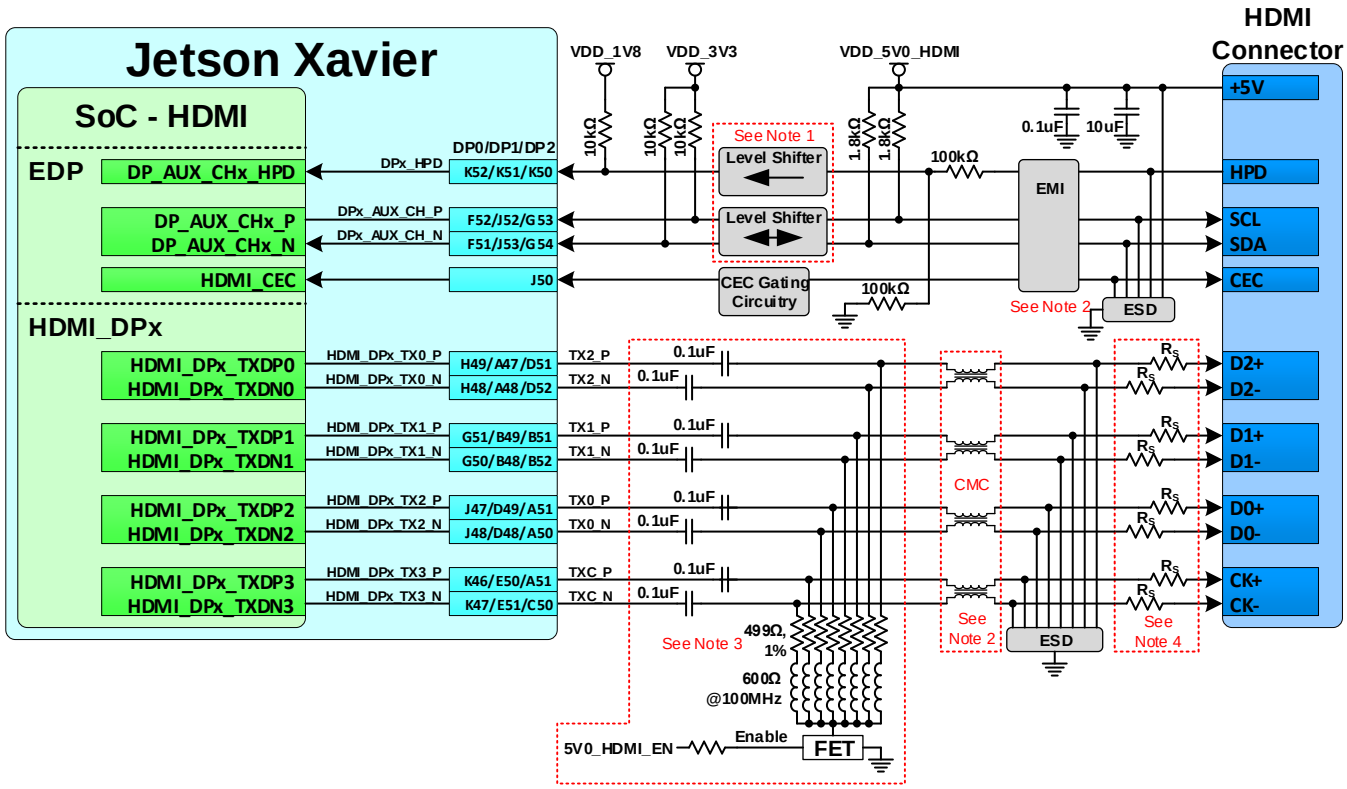
Test Points Recommended	Location
One for each signal line.	Near display connector. Connector pins can be used if accessible.

Note: Test points must be done carefully to minimize signal integrity impact. Avoid stubs & keep pads small & near signal traces

8.1.2 HDMI

A standard DP 1.2a or HDMI V2.0 interface is supported. These share the same set of interface pins, so either Display Port or HDMI can be supported natively. Dual-Mode DisplayPort(DP++) can be supported, in which the DisplayPort connector logically outputs TMDS signaling to a DP-to-HDMI dongle.

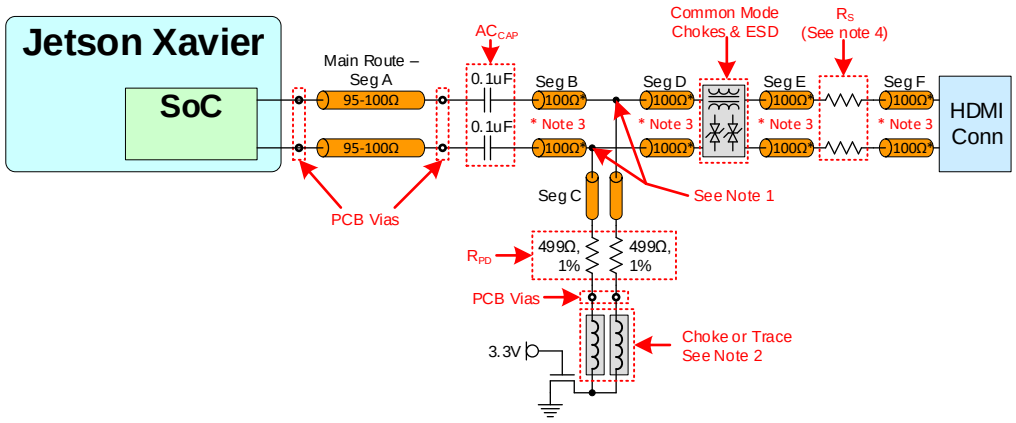
Figure 24: HDMI Connection Example



Note: 1. Level shifters required on DDC/HPD. Jetson Xavier pads are not 5V tolerant & cannot directly meet HDMI V_{IL}/V_{IH} requirements. HPD level shifter can be non-inverting or inverting.

2. If EMI/ESD devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing & electrical requirements of the HDMI specification for the modes to be supported. See requirements & recommendations in the related sections of the HDMI Interface Signal Routing Requirements table.
3. The HDMI_DP_TXx pads are native DP pads & require series AC capacitors (AC_{CAP}) & pull-downs (R_{PD}) to be HDMI compliant. The 499Ω, 1% pull-downs must be disabled when SoC is off to meet the HDMI V_{OFF} requirement. The enable to the FET, enables the pull-downs when the HDMI interface is to be used. Chokes between pull-downs & FET are required for Standard Technology designs and recommended for HDI designs.
4. Series resistors R_S are required. See the R_S section of the HDMI Interface Signal Routing Requirements table for details.

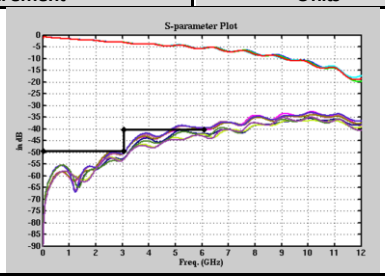
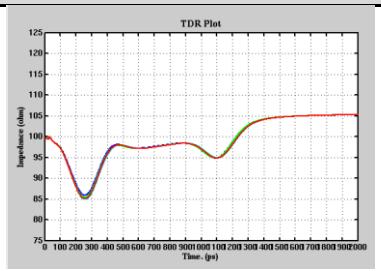
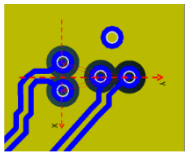
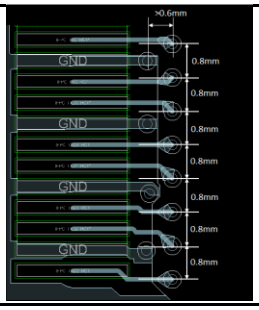
Figure 25: HDMI Clk/Data Topology

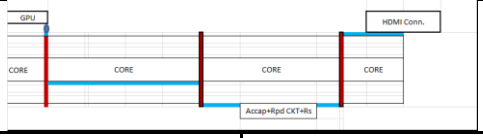
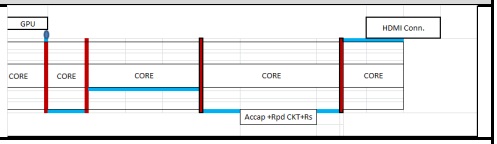
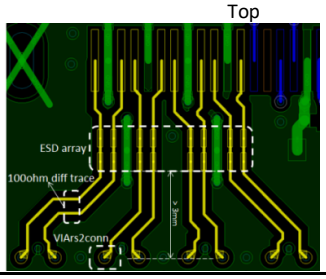
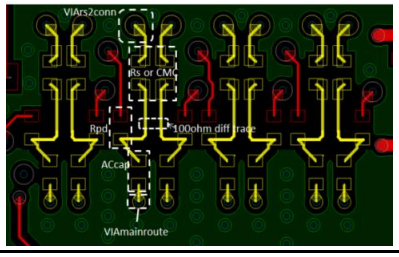
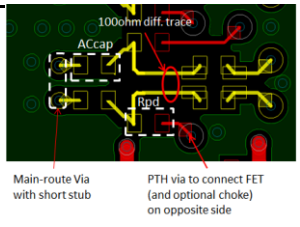


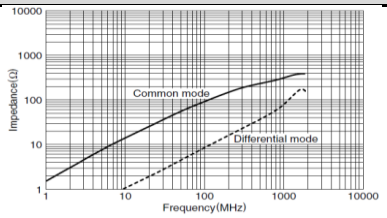
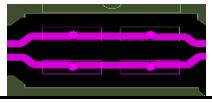
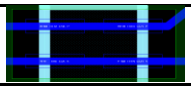
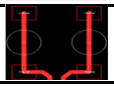
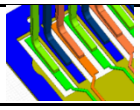
Note:
1. R_{PD} pad must be on the main trace. R_{PD} & AC_{CAP} must be on same layer.
2. Chokes (600Ω@100MHz) or narrow traces (1uH@DC-100MHz) between pull-downs & FET are required for Standard Technology (through-hole) designs and recommended for HDI designs.
3. The trace after the main-route via should be routed on the Top or Bottom layer of the PCB, and either with 100ohm differential impedance, or as uncoupled 50ohm Single Ended traces.
4. R_S series resistor is required. See the R_S section of the HDMI Interface Signal Routing Requirements table for details.

Table 41. HDMI Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Specification			
Max Frequency / UI	5.94 / 168	Gbps / ps	Per lane – not total link bandwidth
Topology	Point to point		Unidirectional, Differential
Termination At Receiver On-board	100 500	Ω	Differential To **3.3V** at receiver To **GND** near connector
Electrical Specification			
IL resonance dip frequency	<= 1.7 <= 2 <= 3 < 6 > 12	dB @ 1GHz dB @ 1.5GHz dB @ 3GHz dB @ 6GHz GHz	
TDR dip	>= 85	Ω @ Tr=200ps	10%-90%. If TDR dip is 75~85ohm that dip width should < 250ps
FEXT (PSFEXT)	<= -50 <= -40 <= -40	dB at DC dB at 3GHz dB at 6GHz	PSNEXT is derived from an algebraic summation of the individual NEXT effects on each pair by the other pairs
	IL/FEXT plot		TDR plot

Parameter	Requirement	Units	Notes
			
Impedance			
Trace Impedance Diff pair	100	Ω	±10%. Target is 100Ω. 95Ω for the breakout & main route is an implementation option.
Reference plane	**GND**		
Trace spacing/Length/Skew			
Trace loss characteristic:	< 0.8 < 0.4	dB/in. @ 3GHz dB/in. @ 1.5GHz	The max length is derived based on this characteristic. The length constraint must be re-defined if the loss characteristic is changed.
Trace spacing (Pair-Pair) Stripline Microstrip: pre 1.4b Microstrip: 1.4b/2.0	3x 4x 5x to 7x	dielectric	For Stripline, this is 3x of the thinner of above and below.
Trace spacing Stripline (Main Link to DDC) Microstrip	3x 5x	dielectric	For Stripline, this is 3x of the thinner of above and below.
Max Total Delay (1.4b/2.0 - up to 5.94Gbps) Stripline Microstrip (5x spacing) Microstrip (7x spacing)	 63.5/2.5 (437) 50.8/2.0 (300) 63.5/2.5 (375)	 mm/in (ps)	Propagation delay: 175ps/in. for stripline, 150ps/in. for microstrip).
Max Intra-Pair (within pair) Skew	0.15 (1)	Mm (ps)	See Notes 1, 2 & 3
Max Inter-Pair (pair to pair) Skew	150	ps	See Notes 1, 2 & 3
Max **GND** transition Via distance	1x	Diff pair via pitch	For signals switching reference layers, add one or two ground stitching vias. It is recommended they be symmetrical to signal vias.
Via			
Topology	4. Y-pattern is recommended 5. keep symmetry		Xtalk suppression is the best by Y-pattern. Also it can reduce the limit of pair-pair distance. Need review (NEXT/FEXT check) if via placement is not Y-pattern. 
Minimum Impedance Dip	97 92	Ω@200ps Ω@35ps	
Recommended Via Dimension drill/pad Antipad Via pitch	 200/400 840 880	 uM	
GND via	Place **GND** via as symmetrically as possible to data pair vias. Up to 4 signal vias (2 diff pairs) can share a single **GND** return via		**GND** via is used to maintain return path, while its Xtalk suppression is limited
Connector pin via	- The break-in trace to the connector pin via should be routed on the BOTTOM in order to avoid via stub effect - Equal spacing (0.8mm) between adjacent signal vias. - The x-axis distance between signal and GND via should be > 0.6mm		
Max # of Vias PTH via u-via	4 if all vias are PTH via Not limited as long as total channel loss meets IL spec.		
	No breakout: ≤ 3 vias		breakout on the same layer as main trunk: ≤ 4 vias

Parameter	Requirement	Units	Notes
			
Max Via Stub Length	0.4	mm	long via stub requires review (IL & resonance dip check)
Serpentine (See USB 3.1 Guidelines)			
Topology			
The main-route via dimensions should comply with the via structure rules (See Via section)			See topology figure above table
For the connector pin vias, follow the rules for the connector pin vias (See Via section)			
The traces after main-route via should be routed as 100Ω differential or as uncoupled 50ohm Single-ended traces on PCB Top or Bottom.			
Max distance from R_{PD} to main trace (seg B)	1	mm	
Max distance from AC cap to RPD stubbing point (seg A)	~0	mm	
Max distance between ESD and signal via	3	mm	
Add-on Components			
Example of a case where space is limited for placing components.	Top 		Bottom 
AC Cap			
Value	0.1	uF	
Max via distance from BGA	7.62 (52.5)	mm (ps)	
Location	must be placed before pull-down resistor		The distance between the AC cap and the HDMI connector is not restricted.
Placement PTH design Micro-Via design	Place cap on bottom layer if main-route above core Place cap on top layer if main-route below core Not Restricted		
Void	GND (or PWR) void under/above the cap is needed. Void size = SMT area + 1x dielectric height keepout distance		
Pull-down Resistor (R_{PD}), choke/FET			
Value	500	Ω	
Location.	Must be placed after AC cap		
Layer of placement	Same layer as AC cap. The FET & choke can be placed on the opposite layer thru a PTH via		
Choke between R_{PD} & FET Choke Max Trace Rdc Max Trace length	600 or 1 ≤20 4	Ω@100MHz uH@DC-100MHz mΩ mm	Can be choke or Trace. Recommended option for HDMI2.0 HF1-9 improvement.
Void	**GND/PWR** void under/above cap is preferred		
Common-Mode Choke (Stuffing option – not added unless EMI issue is seen)			TDK ACM2012D-900-2P
Common-mode impedance @ 100MHz Min Max	65 90	Ω	
R_{DC}	<=0.3ohm		
Differential TDR impedance	90ohm +/-15% @ Tr=200ps (10%-90%)		
Min Sdd21 @ 2.5GHz	2.22	dB	

Parameter	Requirement	Units	Notes
Max Scc21 @ 2.5GHz	19.2	dB	
Location	Close to any adjacent discontinuity (< 8mm) – such as connector, via, etc.		
ESD (On-chip protection diode is able to withstand 2kV HMM. External ESD is optional. Designs should include ESD footprint as a stuffing option)			
Max junction capacitance (IO to **GND**)	0.35	pF	e.g. ON-semiconductor ESD8040
Footprint	Pad right on the net instead of trace stub		 
Location	After pull-down resistor/CMC and before R_S		
Void	**GND/PWR** void under/above the cap is needed. Void size = 1mm x 2mm for 1 pair		
Series Resistor (R_S) – Series resistor on P/N path for HDMI 2.0 (Mandatory)			
Value	≤ 6	Ω	± 10%. 0ohm is acceptable if the design passes the HDMI2.0 HF1-9 test. Otherwise, adjust the R_S value to ensure the HDMI2.0 tests pass: Eye diagram, Vlow test and HF1-9 TDR test
Location	After all components and before HDMI connector		
Void	**GND/PWR** void under/above the R_S device is needed. Void size = SMT area + 1x dielectric height keepout distance.		
Trace at Component Region			
Value	100	Ω	± 10%
Location	At component region (Microstrip)		
Trace entering the SMT pad	One 45°		
Trace between components	Uncoupled structure		
HDMI Connector			
Connector Voiding	Voiding the ground below the signal lanes 0.1448(5.7mil) larger than the pin itself		
General			
Routing over Voids	Routing over voids not allowed except void around device ball/pin the signal is routed to.		
Noise Coupling	Keep critical HDMI related traces including differential clock/data traces & RSET trace away from other signal traces or unrelated power traces/areas or power supply components		

Note:
1. The average of the differential signals is used for length matching.
2. Do not perform length matching within breakout region. Recommend doing trace length matching to <1ps before vias or any discontinuity to minimize common mode conversion
3. If routing includes a flex or 2nd PCB, the max trace delay & skew calculations must include all the PCBs/flex routing. Solutions with flex/2nd PCB may not achieve maximum frequency operation.

Table 42. HDMI Signal Connections

Jetson Xavier Pin Name	Type	Termination (see note on ESD)	Description
HDMI_DPx_TX3_N/P	DIFF OUT	0.1uF series AC_{CAP} → 500Ω R_{PD} (controlled by FET) → EMI/ESD (if required),.≤6Ω R_S (series resistor)	**HDMI Differential Clock:** Connect to **C–/C+** & pins on HDMI Connector
HDMI_DPx_TX[2:0]_N/P	DIFF OUT		**HDMI Differential Data:** Connect to **D[2:0]+/–** pins. See DP/HDMI Pin Mapping table and connection diagram.

DPx_HPD	I	Jetson Xavier to Connector: 10kΩ PU to 1.8V → level shifter → 100kΩ series resistor. 100kΩ to **GND** on connector side.	**HDMI Hot Plug Detect:** Connect to **HPD** pin on HDMI Connector
HDMI_CEC	I/OD	Gating circuitry, See connection figure or reference schematics for details.	**HDMI Consumer Electronics Control:** Connect to **CEC** on HDMI Connector through circuitry.
DPx_AUX_CH_N/P	I/OD	From Jetson Xavier to Connector: 10kΩ PU to 3.3V → level shifter → 1.8kΩ PU to 5V → connector pin	**HDMI: DDC Interface – Clock and Data**: Connect **DPx_AUX_CH+** to **SCL** & **DPx_AUX_CH–** to **SDA** on HDMI Connector
HDMI 5V Supply	P	Adequate decoupling (0.1uF & 10uF recommended) on supply near connector.	**HDMI 5V supply to connector:** Connect to **+5V** on HDMI Connector.

Note: Any ESD and/or EMI solutions must support targeted modes (frequencies).

Table 43. Recommended HDMI / DP observation (test) points for initial boards

Test Points Recommended	Location
One for each signal line.	Near display connector. Connector pins can be used if accessible.

Note: Test points must be done carefully to minimize signal integrity impact. Avoid stubs & keep pads small & near signal traces

9.0 VIDEO INPUT

Jetson Xavier provides multiple MIPI CSI D-PHY or C-PHY interfaces for cameras. In addition, an 8-lane SLVS camera interface. SLVS will be covered in a later version of this design guide.

9.1 MIPI CSI

Jetson Xavier supports four MIPI CSI x4 bricks, allowing a variety of device types and combinations to be supported. Up to 4 quad lane cameras or four dual lane cameras plus two quad lane cameras or 6 dual lane cameras (total of 6 in any configuration) are available. Both MIPI D-PHY & C-PHY modes are supported. In D-PHY mode, each data channel has peak bandwidth of up to 2.5Gbps. For C-PHY, each lane (Trio) supports up to 2.5Gsps..

Note: Maximum data rate may be limited by use case / memory bandwidth.

Table 44. Jetson Xavier CSI Pin Descriptions

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
F42	CSI0_CLK_N	CSI_A_CLK_N	Camera, CSI 0 Clock–	Camera Connector	Input	MIPI D-PHY/C-PHY
F43	CSI0_CLK_P	CSI_A_CLK_P	Camera, CSI 0 Clock+		Input	
E41	CSI0_D0_N	CSI_A_D0_N	Camera, CSI 0 Data 0–		Input	
E42	CSI0_D0_P	CSI_A_D0_P	Camera, CSI 0 Data 0+		Input	
E38	CSI0_D1_N	CSI_A_D1_N	Camera, CSI 0 Data 1–		Input	
E39	CSI0_D1_P	CSI_A_D1_P	Camera, CSI 0 Data 1+		Input	
H42	CSI1_CLK_N	CSI_B_CLK_N	Camera, CSI 1 Clock–		Input	
H43	CSI1_CLK_P	CSI_B_CLK_P	Camera, CSI 1 Clock+		Input	
G42	CSI1_D0_N	CSI_B_D0_N	Camera, CSI 1 Data 0–		Input	
G41	CSI1_D0_P	CSI_B_D0_P	Camera, CSI 1 Data 0+		Input	
J42	CSI1_D1_N	CSI_B_D1_N	Camera, CSI 1 Data 1–		Input	
J41	CSI1_D1_P	CSI_B_D1_P	Camera, CSI 1 Data 1+		Input	
B42	CSI2_CLK_N	CSI_C_CLK_N	Camera, CSI 2 Clock–		Input	
B43	CSI2_CLK_P	CSI_C_CLK_P	Camera, CSI 2 Clock+		Input	
A42	CSI2_D0_N	CSI_C_D0_N	Camera, CSI 2 Data 0–		Input	
A41	CSI2_D0_P	CSI_C_D0_P	Camera, CSI 2 Data 0+		Input	
C41	CSI2_D1_N	CSI_C_D1_N	Camera, CSI 2 Data 1–		Input	
C42	CSI2_D1_P	CSI_C_D1_P	Camera, CSI 2 Data 1+		Input	
F45	CSI3_CLK_N	CSI_D_CLK_N	Camera, CSI 3 Clock–		Input	
F46	CSI3_CLK_P	CSI_D_CLK_P	Camera, CSI 3 Clock+		Input	
E44	CSI3_D0_N	CSI_D_D0_N	Camera, CSI 3 Data 0–		Input	
E45	CSI3_D0_P	CSI_D_D0_P	Camera, CSI 3 Data 0+		Input	
G45	CSI3_D1_N	CSI_D_D1_N	Camera, CSI 3 Data 1–		Input	
G44	CSI3_D1_P	CSI_D_D1_P	Camera, CSI 3 Data 1+		Input	
F49	CSI4_CLK_N	CSI_E_CLK_N	Camera, CSI 4 Clock–		Input	
F48	CSI4_CLK_P	CSI_E_CLK_P	Camera, CSI 4 Clock+		Input	
G47	CSI4_D0_N	CSI_E_D0_N	Camera, CSI 4 Data 0–		Input	
G48	CSI4_D0_P	CSI_E_D0_P	Camera, CSI 4 Data 0+		Input	
E48	CSI4_D1_N	CSI_E_D1_N	Camera, CSI 4 Data 1–		Input	
E47	CSI4_D1_P	CSI_E_D1_P	Camera, CSI 4 Data 1+		Input	
C45	CSI5_CLK_N	CSI_F_CLK_N	Camera, CSI 5 Clock–		Input	
C44	CSI5_CLK_P	CSI_F_CLK_P	Camera, CSI 5 Clock+		Input	
D43	CSI5_D0_N	CSI_F_D0_N	Camera, CSI 5 Data 0–		Input	
D42	CSI5_D0_P	CSI_F_D0_P	Camera, CSI 5 Data 0+		Input	
D45	CSI5_D1_N	CSI_F_D1_N	Camera, CSI 5 Data 1–		Input	
D46	CSI5_D1_P	CSI_F_D1_P	Camera, CSI 5 Data 1+		Input	
J45	CSI6_CLK_N	CSI_G_CLK_N	Camera, CSI 5 Clock–		Input	
J44	CSI6_CLK_P	CSI_G_CLK_P	Camera, CSI_6 Clock+		Input	
K43	CSI6_D0_N	CSI_G_D0_N	Camera, CSI_6 Data 0–		Input	
K44	CSI6_D0_P	CSI_G_D0_P	Camera, CSI_6 Data 0+		Input	
H45	CSI6_D1_N	CSI_G_D1_N	Camera, CSI_6 Data 1–		Input	
H46	CSI6_D1_P	CSI_G_D1_P	Camera, CSI_6 Data 1+		Input	
B46	CSI7_CLK_N	CSI_H_CLK_N	Camera, CSI_7 Clock–		Input	
B45	CSI7_CLK_P	CSI_H_CLK_P	Camera, CSI_7 Clock+		Input	

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
A45	CSI7_D0_N	CSI_H_D0_N	Camera, CSI_7 Data 0–		Input	
A44	CSI7_D0_P	CSI_H_D0_P	Camera, CSI_7 Data 0+		Input	
C48	CSI7_D1_N	CSI_H_D1_N	Camera, CSI_7 Data 1–		Input	
C47	CSI7_D1_P	CSI_H_D1_P	Camera, CSI_7 Data 1+		Input	

Table 45. Jetson Xavier Camera Miscellaneous Pin Descriptions

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
J54	MCLK02	EXTPERIPH1_CLK	Camera 0 Master Clock	Camera Connector	Output	CMOS – 1.8V
H53	MCLK03	EXTPERIPH2_CLK	Camera 1 Master Clock	Camera Connector	Output	CMOS – 1.8V
H55	MCLK04	SOC_GPIO41	Camera 2 Master Clock	Camera Connector	Output	CMOS – 1.8V
L57	MCLK05	SOC_GPIO42	Camera 2 Master Clock	Expansion Connector	Output	CMOS – 1.8V
F53	I2C3_CLK	CAM_I2C_SCL	General I2C 3 Clock	Camera Connector	Bidir	CMOS – 1.8V
E53	I2C3_DAT	CAM_I2C_SDA	General I2C 3 Data	Camera Connector	Bidir	CMOS – 1.8V
F10	GPIO15	DAP5_SCLK	GPIO / Digital Speaker Output Clock	Camera Connector (Camera 1 Powerdown)	Output	CMOS – 1.8V
F9	GPIO16	DAP5_DOUT	GPIO / Digital Speaker Output Data	Camera Connector (Camera 1 Reset)	Output	CMOS – 1.8V
K49	GPIO25	SOC_GPIO50	GPIO	Camera Connector (VDD_SYS Enable)	Output	CMOS – 1.8V
F56	GPIO36	SOC_GPIO53	GPIO	Camera AVDD Enable	Output	CMOS – 1.8V
L49	UART4_CTS	UART4_CTS	UART 4 Clear to Send	Camera Connector (Camera 0 Powerdown)	Output	CMOS – 1.8V
L5	UART4_TX	UART4_TX	UART 4 Transmit	Camera Connector (Camera 0 Reset)	Output	CMOS – 1.8V

Table 46. CSI Configurations (D-PHY Mode)

Signal Name	x2 Configurations						x4 Configurations			
	#1	#2	#3	#4	#5	#6	#1	#2	#3	#4
CSI_0_D0_P/N	Data						Data			
CSI_0_D1_P/N										
CSI_1_D0_P/N		Data								
CSI_1_D1_P/N										
CSI_2_D0_P/N			Data					Data		
CSI_2_D1_P/N										
CSI_3_D0_P/N				Data						
CSI_3_D1_P/N										
CSI_4_D0_P/N					Data				Data	
CSI_4_D1_P/N										
CSI_5_D0_P/N										
CSI_5_D1_P/N										
CSI_6_D0_P/N						Data				Data
CSI_6_D1_P/N										
CSI_7_D0_P/N										
CSI_7_D1_P/N										
CSI_0_CLK_P/N	Clk						Clk			
CSI_1_CLK_P/N		Clk								
CSI_2_CLK_P/N			Clk					Clk		
CSI_3_CLK_P/N				Clk						
CSI_4_CLK_P/N					Clk				Clk	
CSI_5_CLK_P/N										
CSI_6_CLK_P/N[1]						Clk				Clk
CSI_7_CLK_P/N[1]										

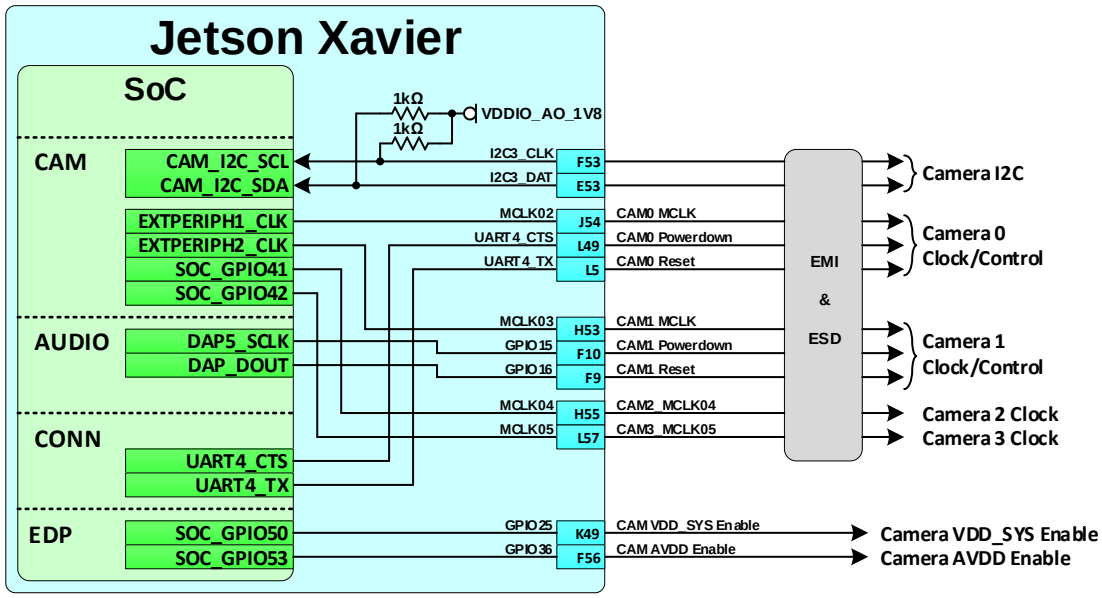
Note: 1. Each 2-lane option shown above can also be used for one single lane camera as well
2. Combinations of 1, 2 & 4-lane cameras are supported, as long as any 4-lane cameras match one of the four configurations above

Table 47. CSI Configurations (C-PHY Mode)

		2-Trio Configs						4-Trio Configs			
Camera # / SoC Balls	C-PHY Lanes	#1	#2	#3	#4	#5	#6	#1	#2	#3	#4
CSI_0_CLK_P, CSI_0_D0_P/N	0:0	√						√			
CSI_0_CLK_N, CSI_0_D1_P/N	0:1	√						√			
CSI_1_CLK_P. CSI_1_D0_P/N	1:0		√					√			
CSI_1_CLK_N, CSI_1_D1_P/N	1:1		√					√			
CSI_2_CLK_P, CSI_2_D0_P/N	2:0			√					√		
CSI_2_CLK_N, CSI_2_D1_P/N	2:1			√					√		
CSI_3_CLK_P, CSI_3_D0_P/N	3:0				√				√		
CSI_3_CLK_N, CSI_3_D1_P/N	3:1				√				√		
CSI_4_CLK_P, CSI_4_D0_P/N	4:0					√				√	
CSI_4_CLK_N, CSI_4_D1_P/N	4:1					√				√	
CSI_5_CLK_P, CSI_5_D0_P/N	5:0									√	
CSI_5_CLK_N, CSI_5_D1_P/N	5:1									√	
CSI_6_CLK_P, CSI_6_D0_P/N	6:0						√				√
CSI_6_CLK_N, CSI_6_D1_P/N	6:1						√				√
CSI_7_CLK_P, CSI_7_D0_P/N	7:0										√
CSI_7_CLK_N, CSI_7_D1_P/N	7:1										√

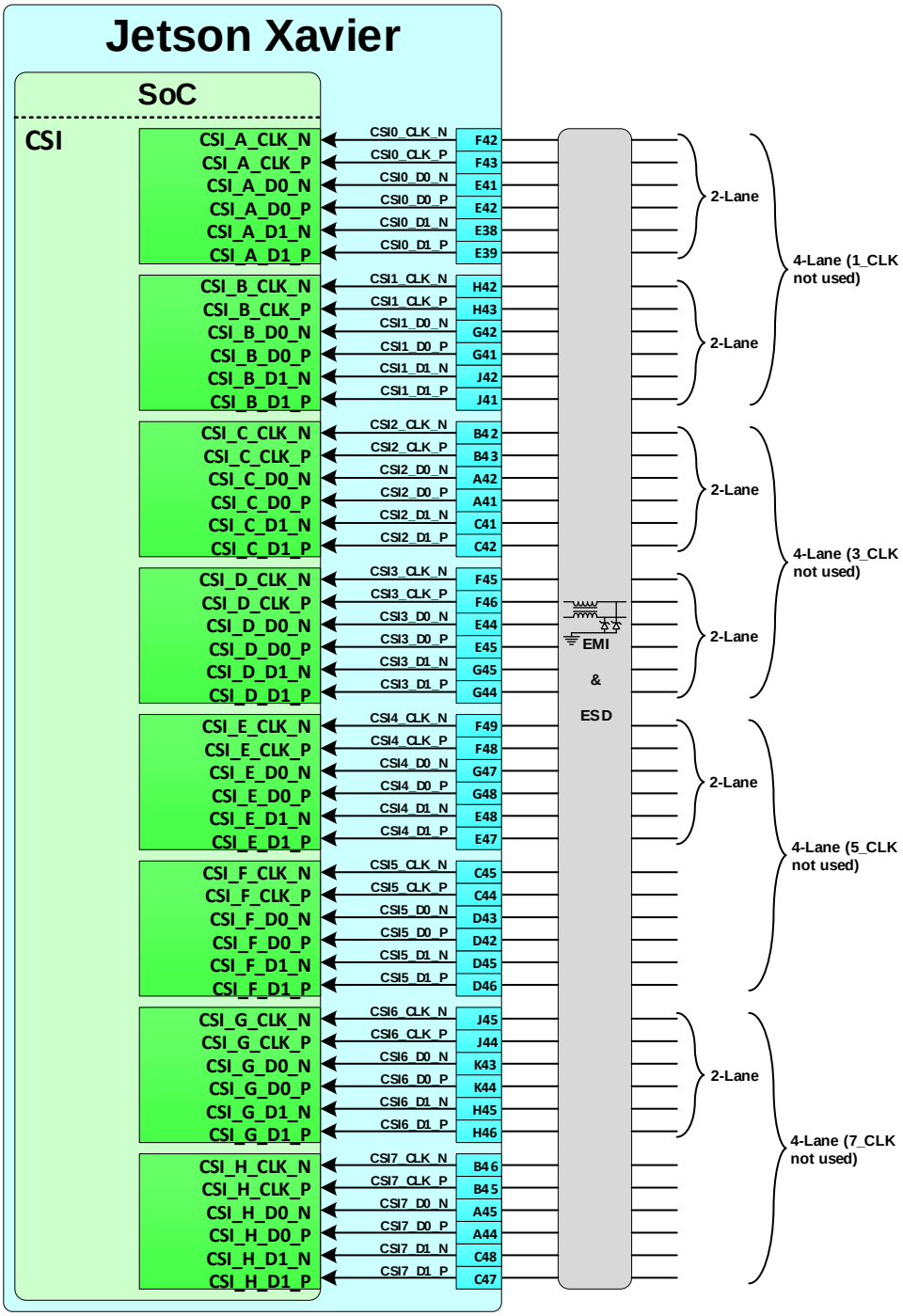
Note: Each x2 configurations can also be used for one single lane camera (x1 configuration) as well.
Configurations can coexist to support a mix of x1, x2 & x4 lanes, as long as each signal is not shared between multiple configurations.

Figure 26: Camera Control Connections



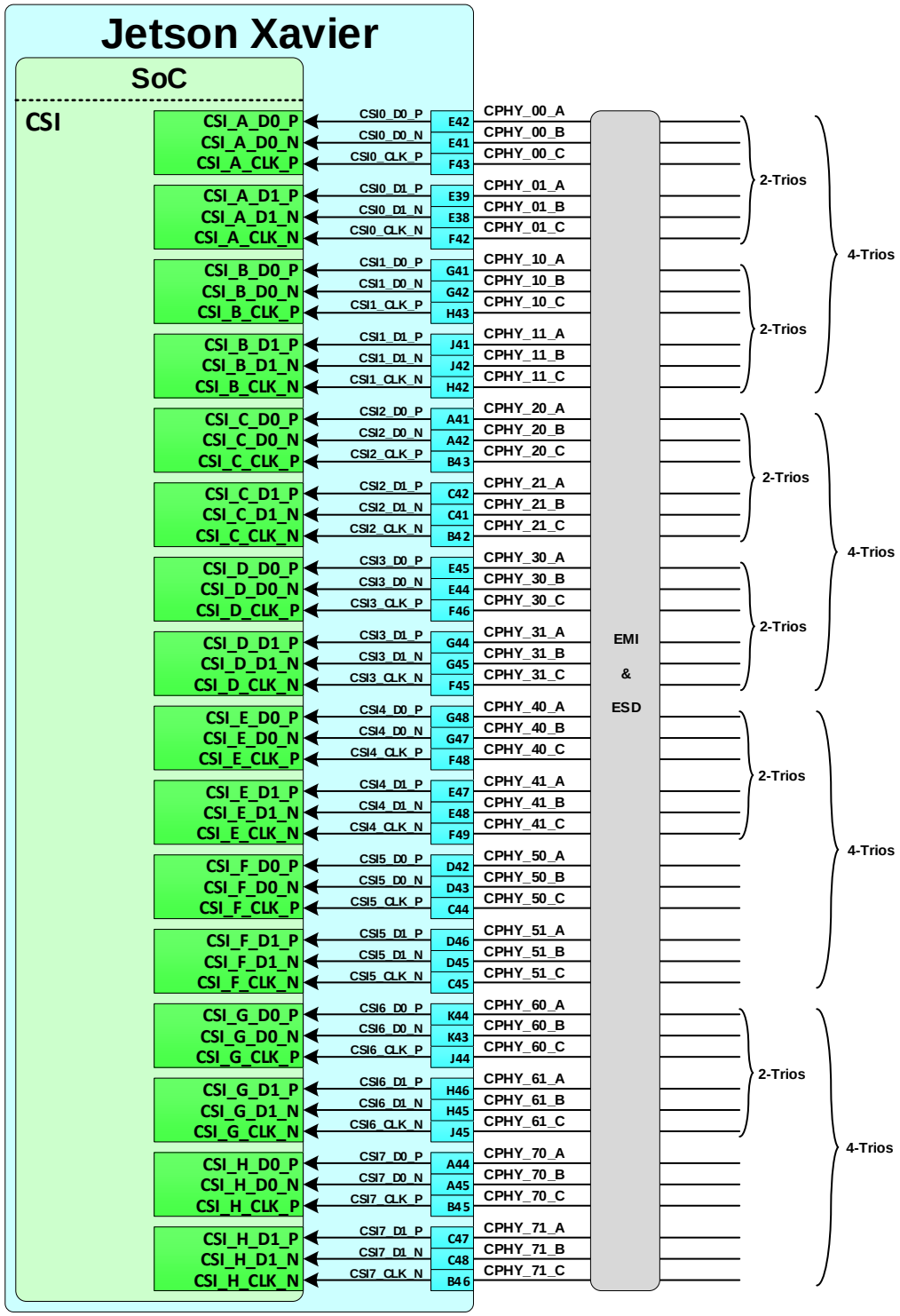
Note: Any EMI/ESD devices must be tuned to minimize impact to signal quality and meet the timing & Vil/Vih requirements at the receiver & maintain signal quality and meet requirements for the frequencies supported by the design.

Figure 27: Camera CSI D-PHY Connections



Note: Any EMI/ESD devices must be tuned to minimize impact to signal quality and meet the timing & Vil/Vih requirements at the receiver & maintain signal quality and meet requirements for the frequencies supported by the design .

Figure 28: Camera CSI C-PHY Connections



CSI D-PHY Design Guidelines

Table 48. MIPI CSI D-Phy Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate (per data lane) for High-Speed mode Max Frequency (for Low Power mode)	2.5 10	Gbps MHz	
Number of Loads	1	load	
Max Loading (per pin)	10	pF	
Reference plane	**GND**		
Breakout Region Impedance (Single Ended)	45-50	Ω	±15%
Max PCB breakout delay	48	ps	
Trace Impedance Diff pair / Single Ended	90-100 / 45-50	Ω	
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 1
Trace spacing Microstrip / Stripline	2x / 2x	dielectric	
Max Trace Delay 1 / 1.5 / 2.5 Gbps	1100 / 800 / 350	ps	See Note 2
Max Intra-pair Skew	1	ps	See Note 2
Max Trace Delay Skew between **DQ** & **CLK**	5	ps	See Note 2
Keep critical DSI/CSI related traces including DSI/CSI clock/data traces & RDN/RUP traces away from other signal traces or unrelated power traces/areas or power supply components			

Note:
1. Up to 4 signal Vias can share a single **GND** return Via
2. If routing to device includes a flex or 2nd PCB, the max trace & skew calculations must include all the PCBs/flex routing

CSI C-PHY Mode Design Guidelines

Table 49. MIPI CSI C-PHY Mode Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate (per trio)	2.5	Gsps	See note 1 & 2
Topology	Point-Point		With RX Common Mode cap to GND
Termination	Fully ODT (on-die)		50ohms SE to common mode cap
Max Loading (per pin)	2	pF	Single ended
Trace Impedance Differential / Single Ended	90-100 / 45-50	Ω	±15%
Reference Plane	**GND**		
Max PCB breakout Length/Delay	5 (30)	mm (ps)	
Via proximity (Signal via to GND return via)	< 2	mm	
Intra Trio Trace spacing Microstrip / Stripline	2x / 2x	dielectric	Recommendation
Inter Trio Trace spacing Microstrip / Stripline	150	ps	Recommend routing with loosely coupled differential impedance.
Max Trace Length/Delay Microstrip Stripline	51 (300) 51 (350)	mm (ps)	See Note 3
Max Intra-Trio Skew (Within Trios)	6	ps	A or B pin to C pin skew. See Note 3
Max Inter-Trio Skew (between Trios)	55	ps	See Note 3
Routing Layer Restrictions	A trio must route completely on the same layer. This means that both Trio0 and Trio1 would need to route on the same layer due to DPHY Compatibility (e.g. D0P/D0N must route on the same layer as CLKP/CLKN and thus so must D1P/D1N)		
Keep critical CSI C-PHY related traces including CSI Trio traces & RDN/RUP traces away from other signal traces or unrelated power traces/areas or power supply components			

Notes:
1. Bit rate in bps is 2.286 * Gsps.
2. Maximum data rate may be limited by use case / memory bandwidth.
3. If routing to DSI or CSI device includes a flex or 2nd PCB, the max trace & skew calculations must include all the PCBs/flex routing

Table 50. MIPI CSI Signal Connections

Jetson Xavier Pin Name	Type	Termination	Description
CSI[7:0]_CLK+/–	DIFF IN	See note	**CSI Differential Clocks:** Connect to clock pins of camera. See the CSI Configurations tables for details
CSI[7:0]_D[1:0]+/–	DIFF IN	See note	**CSI Differential Data Lanes:** Connect to data pins of camera. See the CSI Configurations tables for details

Note: Depending on the mechanical design of the platform and camera modules, ESD protection may be necessary. In addition, EMI control may be needed. Both are shown in the Camera Connection Example diagram. Any EMI/ESD solution must be compatible with the frequency required by the design.

Table 51. Miscellaneous MIPI Camera Connections

Jetson Xavier Pin Name (Camera Function)	Type	Termination	Description
I2C3_CLK **I2C3_DAT**	O I/O	1kΩ Pull-ups **VDD_1V8** (on Jetson Xavier). See note related to EMI/ESD under MIPI CSI Signal Connections tables.	**Camera I2C Interface:** Connect to I2C **SCL & SDA** pins of imager
MCLK02 (CAM0 MCLK) **MCLK03 (CAM1 MCLK)** **MCLK04 (CAM2 MCLK)** **MCLK05 (CAM3 MCLK)**	O	See note related to EMI/ESD under MIPI CSI Signal Connections tables.	**Camera Master Clocks:** Connect to Camera reference clock inputs.
GPIO15 (CAM1 PWDN) **UART4_CTS (CAM0 PWDN)**	I/O		**Camera Power Control signals (or GPIOs [1:0])**: Connect to powerdown pins on camera(s).
GPIO16 (CAM1 RST) **UART4_TX (CAM0 RST)**	O		**Camera Resets:** Connect to reset pin on any cameras with this function.
GPIO25 (VDD_SYS Enable)	O		**Camera VDD_SYS Enable:** Connect to appropriate camera supply.
GPIO36 (AVDD Enable)	O		**Camera AVDD Enable:** Connect to appropriate analog camera supply.

Table 52. Recommended CSI observation (test) points for initial boards

Test Points Recommended	Location
One per signal line.	Near Jetson Xavier pins

Note: Test points must be done carefully to minimize signal integrity impact. Avoid stubs & keep pads small & near signal traces

10.0 SDIO/SDCARD

Jetson Xavier has two SD/MMC interfaces. One is used on Jetson Xavier for eMMC for boot & storage and one is brought to the connector pins for SD Card or SDIO use.

Table 53. SDIO / SD Card / eMMC Interface Mapping

Jetson Xavier Pins	SoC Interface	Width	Usage
SDCARD_CLK	SDMMC1	4-bit	Micro SD / UFS Card socket
na	SDMMC4	8-bit	eMMC device on Module

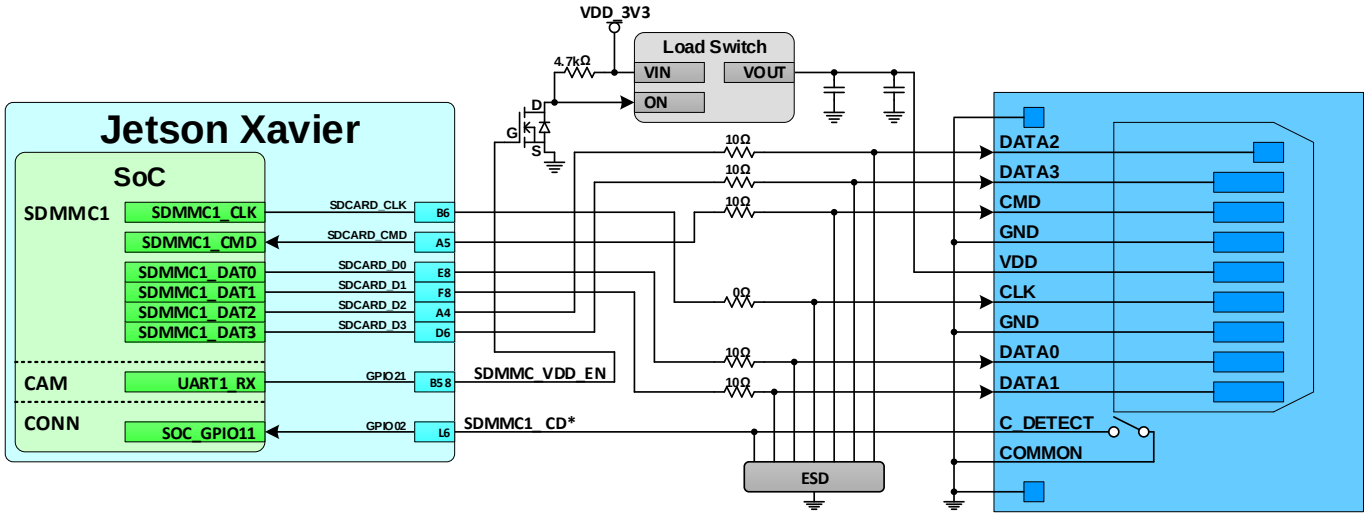
Table 54. Jetson Xavier SDMMC Pin Descriptions

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
B6	SDCARD_CLK	SDMMC1_CLK	SD Card (or SDIO) Clock	Micro SD / UFS Card Socket	Output	CMOS – 3.3V/1.8V
A5	SDCARD_CMD	SDMMC1_CMD	SD Card (or SDIO) Command		Bidir	CMOS – 3.3V/1.8V
E8	SDCARD_D0	SDMMC1_DAT0	SD Card (or SDIO) Data 0		Bidir	CMOS – 3.3V/1.8V
F8	SDCARD_D1	SDMMC1_DAT1	SD Card (or SDIO) Data 1		Bidir	CMOS – 3.3V/1.8V
A4	SDCARD_D2	SDMMC1_DAT2	SD Card (or SDIO) Data 2		Bidir	CMOS – 3.3V/1.8V
D6	SDCARD_D3	SDMMC1_DAT3	SD Card (or SDIO) Data 3		Bidir	CMOS – 3.3V/1.8V
B58	GPIO21	DAP6_SCLK	GPIO	SD Power Switch On	Output	CMOS – 3.3V
L6	GPIO02	SOC_GPIO11	GPIO	SD Card socket (SD Detect)	Bidir	CMOS – 1.8V

10.1 SD Card

The Figure shows a Micro SD card socket connection example. Internal pull-up resistors are used for SDCARD Data/CMD lines. External pull-ups are not required and cannot be used due to the internal pad voltage selection.

Figure 29. Micro SD Card Socket Connection Example



Notes:
1. If EMI and/or ESD devices are necessary, they must be tuned to minimize the impact to signal quality, which must meet the timing & Vil/Vih requirements at the receiver & maintain signal quality and meet requirements for the frequencies supported by the design.
2. Supply (load switch, etc) used to provide power to the SD Card must be current limited if the supply is shorted to GND.

Table 55. SDCARD Interface Signal Routing Requirements

Parameter			Requirement	Units	Notes
Max Frequency	3.3V Signaling	DS	25 (12.5)	MHz (MB/s)	See Note 1
		HS	50 (25)		
	1.8V Signaling	SDR12	25 (12.5)		

Parameter		Requirement	Units	Notes
	SDR25	50 (25)		
	SDR50	100 (50)		
	SDR104	208 (104)		
	DDR50	50 (50)		
Topology		Point to point		
Reference plane		**GND** or **PWR**		See Note 2
Trace Impedance		50	Ω	±15%. 45Ω optional depending on stack-up
Max Via Count	PTH	**4**		Independand of stackup layers
	HDI	**10**		Depends on stackup layers
Via proximity (Signal to reference)		< 3.8 (24)	mm (ps)	Up to 4 signal Vias can share 1 **GND** return Via
Trace spacing	Microstrip / Stripline	4x / 3x	dielectric	
Trace length				
SDR50 / SDR25 / SDR12 / HS / DS	Min	**16 (100)**	mm (ps)	
	Max	**139 (876)**		
SDR104 / DDR50	Min	**16 (100)**		
	Max	**83 (521)**		
Max Trace Delay Skew in/between **CLK** & **CMD/DAT**				**See Note 3**
	SDR50 / SDR25 / SDR12 / HS / DS	14 (87.5)	**Mm (ps)**	
	SDR104 / DDR50	2 (12.5)		
Keep CLK, CMD & DATA traces away from other signal traces or unrelated power traces/areas or power supply components				

Note:
1. Actual frequencies may be lower due to clock source/divider limitations.
2. If PWR, 0.01uF decoupling cap required for return current.
3. If routing to SD Card socket includes a flex or 2nd PCB, max trace & skew calculations must include PCB & flex routing.

Table 56. SD Card Loading vs Drive Type

General SD Card Compliance	Parameter	Value	Units	Notes
C_{CARD} (C_{DIE}+C_{PKG})	Min	5	pF	Spec best case value
	Max	10	pF	Spec worst case value
Drive Type	A	33	Ω	UHS50 Card = optional, UHS104 Card = mandatory
	B	50	Ω	UHS50 Card = mandatory, UHS104 Card = mandatory
	C	66	Ω	UHS50 Card = optional, UHS104 Card = mandatory
	D	100	Ω	UHS50 Card = optional, UHS104 Card = mandatory
F_{MAX} (CLK base frequency)	SDR104	208	MHz	Single data rate up to 104MB/sec
	DDR50	50	MHz	Double data rate up to 50MB/sec
	SDR50	100	MHz	Single data rate up to 50MB/sec
	SDR25	50	MHz	Single data rate up to 25MB/sec
	SDR12	25	MHz	Single data rate up to 12.5MB/sec
	HS	50	MHz	Single data rate up to 25MB/sec
	DS	25	MHz	Single data rate up to 12.5MB/sec
C_{LOAD} (C_{CARD}+C_{EQ}) (CLK freq = 208MHz)	Drive Type = A	21	pF	Total load capacitance supported
	Drive Type = B	15	pF	Total load capacitance supported
	Drive Type = C	11	pF	Total load capacitance supported
	Drive Type = D	22	pF	Possibly 22pF+ depending on host system
C_{LOAD} (C_{CARD}+C_{EQ}) (CLK freq = 100/50/25MHz)	Drive Type = A	43	pF	Total load capacitance supported
	Drive Type = B	30	pF	Total load capacitance supported
	Drive Type = C	23	pF	Total load capacitance supported
	Drive Type = D	22	pF	Possibly 22pF+ depending on host system

Table 57. SDCARD Signal Connections

Function Signal Name	Type	Termination	Description
SDCARD_CLK	O	See note for EMI/ESD	**SDIO/SD Card Clock:** Connect to **CLK** pin of device or socket
SDCARD_CMD	I/O	See note for EMI/ESD	**SDIO/SDMMC Command:** Connect to **CMD** pin of device/socket
SDCARD_D[3:0]	I/O		**SDIO/SDMMC Data:** Connect to **Data** pins of device or socket
GPIO02 (SDCARD_CD#)	I		**SDIO Card Detect:** Connect to **CD/C_DETECT** pin on socket if required.
GPIO21 (SDCARD_VDD_EN)	O		**SDIO Supply/Load Switch Enable:** Connect to enable of supply/load switch supplying **VDD** on SD Card socket.

Note: EMI/ESD may be required for SDIO when used as the SD Card socket interface. Any EMI/ESD device used must be able to meet signal timing/quality requirements.

Table 58. Recommended SDCARD observation (test) points for initial boards

Test Points Recommended	Location
One for **SDCARD_CLK** line.	Near Device/Connector pin. SD connector pin can be used for device end if accessible.
One **SDCARD_DATx** line & one for **SDCARD_CMD.**	Near Jetson Xavier & Device pins. SD connector pin can be used for device end if accessible.

11.0 AUDIO

Jetson Xavier brings TBD PCM/I2S audio interfaces to the module pins & includes a flexible audio-port switching architecture. In addition, digital microphone & speaker interfaces are provided.

Table 59. Jetson Xavier Audio Pin Descriptions

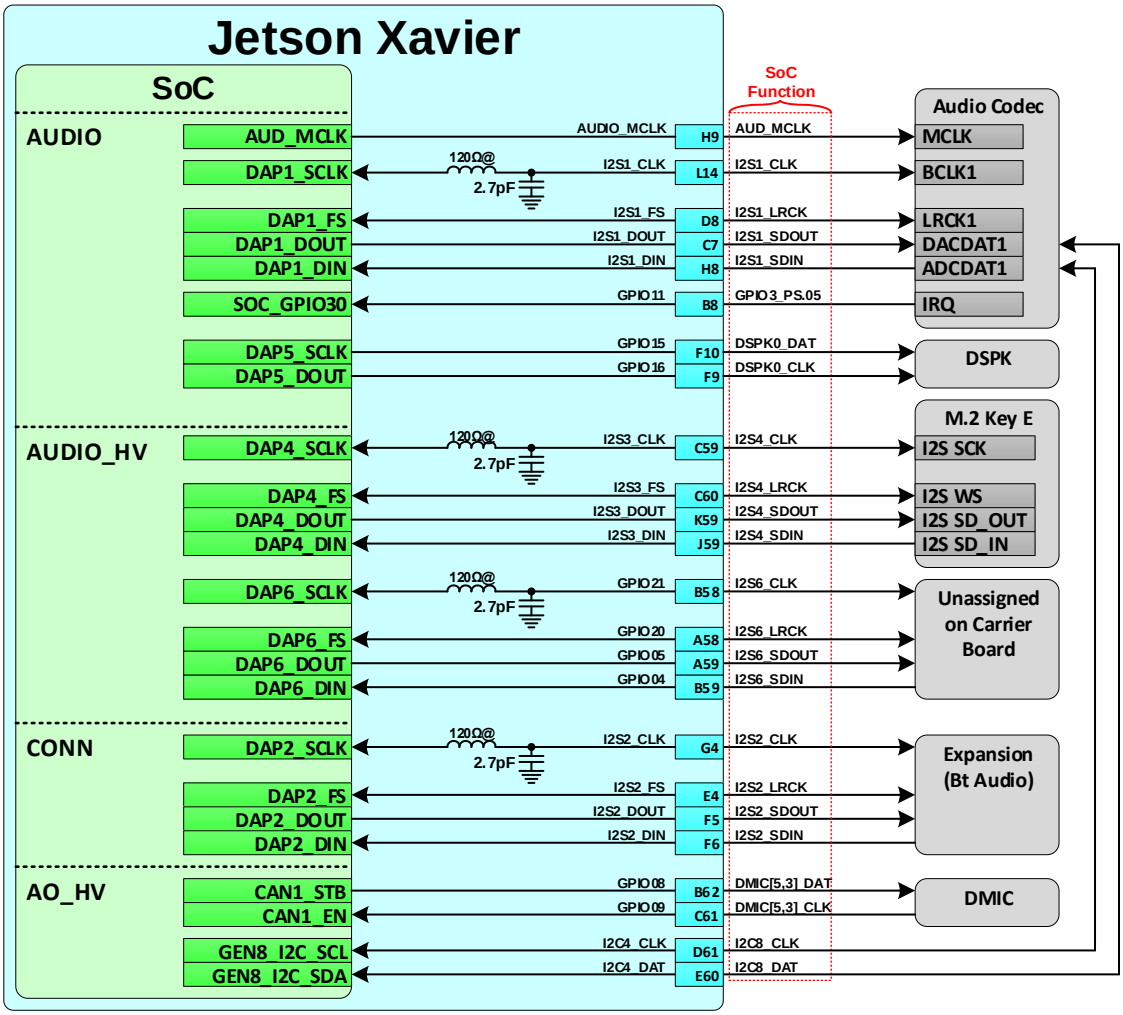
Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
H9	MCLK01	AUD_MCLK	Audio Codec Master Clock	Audio Codec	Output	CMOS – 1.8V
D61	I2C4_CLK	GEN8_I2C_SCL	General I2C 4 Clock	Audio Codec & Camera Connector	Bidir	CMOS – 1.8V
E60	I2C4_DAT	GEN8_I2C_SDA	General I2C 4 Data	Audio Codec & Camera Connector	Bidir	CMOS – 1.8V
L14	I2S1_CLK	DAP1_SCLK	I2S Audio Port 1 Clock	Audio Codec	Bidir	CMOS – 1.8V
D8	I2S1_FS	DAP1_DIN	I2S Audio Port 1 Data In	Audio Codec	Input	CMOS – 1.8V
H8	I2S1_SDIN	DAP1_DOUT	I2S Audio Port 1 Data Out	Audio Codec	Output	CMOS – 1.8V
C7	I2S1_SDOUT	DAP1_FS	I2S Audio Port 1 Left/Right Clock	Audio Codec	Bidir	CMOS – 1.8V
G4	I2S2_CLK	DAP2_SCLK	I2S Audio Port 2 Clock	BT Audio	Bidir	CMOS – 1.8V
F6	I2S2_DIN	DAP2_DIN	I2S Audio Port 2 Data In	BT Audio	Input	CMOS – 1.8V
F5	I2S2_DOUT	DAP2_DOUT	I2S Audio Port 2 Data Out	BT Audio	Output	CMOS – 1.8V
E4	I2S2_FS	DAP2_FS	I2S Audio Port 2 Left/Right Clock	BT Audio	Bidir	CMOS – 1.8V
J59	I2S3_DIN	DAP4_DIN	I2S Audio Port 3 Data In	M.2 Key E	Input	CMOS – 3.3V
K59	I2S3_DOUT	DAP4_DOUT	I2S Audio Port 3 Data Out	M.2 Key E	Output	CMOS – 3.3V
C60	I2S3_FS	DAP4_FS	I2S Audio Port 3 Left/Right Clock	M.2 Key E	Bidir	CMOS – 3.3V
C59	I2S3_SCLK	DAP4_SCLK	I2S Audio Port 3 Clock	M.2 Key E	Bidir	CMOS – 3.3V
B58	GPIO21	DAP6_SCLK	I2S Audio Port 6 Clock	Not assigned	Bidir	CMOS – 3.3V
A58	GPIO20	DAP6_FS	I2S Audio Port 6 Left/Right Clock	Not assigned	Bidir	CMOS – 3.3V
A59	GPIO05	DAP6_DOUT	I2S Audio Port 6 Data Out	Not assigned	Output	CMOS – 3.3V
B59	GPIO04	DAP6_DIN	I2S Audio Port 6 Data In	Not assigned	Input	CMOS – 3.3V
B8	GPIO11	SOC_GPIO30	GPIO	Audio Codec Interrupt	Bidir	CMOS – 1.8V
B62	GPIO08	CAN1_STB	GPIO / Digital Mic Input Data	Expansion Connector (AO DMIC In Data)	Bidir	CMOS – 3.3V
C61	GPIO09	CAN1_EN	GPIO / Digital Mic Input Clock	Expansion Connector (AO DMIC In Clock)	Bidir	CMOS – 3.3V
F10	GPIO15	DAP5_SCLK	GPIO / Digital Speaker Output Clock	Camera Connector (Camera 1 Powerdown)	Bidir	CMOS – 1.8V
F9	GPIO16	DAP5_DOUT	GPIO / Digital Speaker Output Data	Camera Connector (Camera 1 Reset)	Output	CMOS – 1.8V

When possible, the following assignments should be used for the I2Sx interfaces.

Table 60. I2S Interface Mapping

Jetson Xavier Pins (SoC Functions)	Xavier I/O Block	Typical Usage (Usage on Nvidia Carrier Board)
I2S1 (I2S1)	AUDIO	Audio Codec
I2S2 (I2S2)	CONN	Bt Audio
I2S3 (I2S4)	AUDIO_HV	M.2 Key E
GPIO[21:20,05:04] (I2S6)	AUDIO_HV	Unassigned

Figure 30. Audio Device Connections



Note:
- The I2S interfaces can be used in either Master or Slave mode.
- A capacitor from DAPn_FS to GND should be included if SoC an I2S slave & the edge_cntrl configuration = 1 (SDATA driven on positive edge of SCLK). The value of the capacitor should be chosen to provide a minimum of 2ns hold time for the DAPn_FS edge after the rising edge of DAPn_SCLK.

I2S Design Guidelines

Table 61. I2S Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Configuration / Device Organization	1	load	
Max Loading	8	pF	
Reference plane	**GND**		
Breakout Region Impedance	Min width/spacing		
Trace Impedance	50	Ω	±20%
Via proximity (Signal to reference)	< 3.8 (24)	mm (ps)	See Note 1
Trace spacing Microstrip or Stripline	2x	dielectric	
Max Trace Delay	3600 (~22)	ps (in)	
Max Trace Delay Skew between **SCLK** & **SDATA_OUT/IN**	250 (~1.6")	ps (in)	

Note: Up to 4 signal Vias can share a single GND return Via

Table 62. I2S & Miscellaneous Codec Signal Connections

Jetson Xavier Pin Name (Xavier Function)	Type	Termination	Description
I2S1_SCLK (I2S1_CLK) **I2S2_SCLK (I2S2_CLK)** **I2S3_SCLK (I2S4_CLK)** **GPIO21 (I2S6_CLK)**	I/O	120Ω Bead in series & 2.7pF capacitor to GND (on Jetson Xavier).	**I2S Serial Clock:** Connect to I2S/PCM **CLK** pin of audio device.
I2S1_FS (I2S1_LRCK) **I2S2_FS (I2S2_LRCK)** **I2S3_FS (I2S4_LRCK)** **GPIO20 (I2S6_LRCK)**	I/O		**I2S Left/Right Clock:** Connect to Left/Right Clock pin of audio device.
I2S1_DOUT (I2S1_SDOUT) **I2S2_DOUT (I2S2_SDOUT)** **I2S3_DOUT (I2S4_SDOUT)** **GPIO05 (I2S6_SDOUT)**	I/O		**I2S Data Output:** Connect to Data Input pin of audio device.
I2S1_DIN (I2S1_SDIN) **I2S2_DIN (I2S2_SDIN)** **I2S3_DIN (I2S4_SDIN)** **GPIO04 (I2S6_SDIN)**	I		**I2S Data Input:** Connect to Data Output pin of audio device.
AUD_MCLK	O		**Audio Codec Master Clock:** Connect to clock pin of Audio Codec.
GPIO20_AUD_INT	I		**Audio Interrupt:** Connect to interrupt pin of Audio Codec.

DMIC Design Guidelines

Table 63. DMIC Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Clock Frequency/Period	12/83.33	MHz/ns	
Data Bit-rate/Period (DDR24)	24/41.66	Mbps/ns	
Configuration / Device Organization	1	load	
Topology	Point to Point		
Reference plane	**GND**		
Trace Impedance	45-50	Ω	±20%
Via proximity (Signal via to GND return via)	< 3.8 (24)	mm (ps)	See Note
Trace spacing Microstrip / Stripline	2x / 2x	dielectric	
Max Trace Delay	1280	ps	
Max Trace Delay Skew between **CLK** & **DAT**	150	ps	

Notes: Up to 4 signal Vias can share a single GND return Via

Table 64. DMIC Signal Connections

Jetson Xavier Pin Name (Xavier Function)	Type	Termination	Description
GPIO09 (DMIC[5 or 3]_CLK)	O		**Digital Microphone Clock:** Connect to clock pin of DMIC device
GPIO08 (DMIC[5 or 3]_DAT)	I		**Digital Microphone Data:** Connect to data pin of DMIC device

12.0 MISCELLANEOUS INTERFACES

12.1 I2C

The SoC has nine I2C controllers. Jetson Xavier brings eight of the I2C interfaces out, which are shown in the tables below. The assignments in Table 66 should be used for the I2C interfaces:

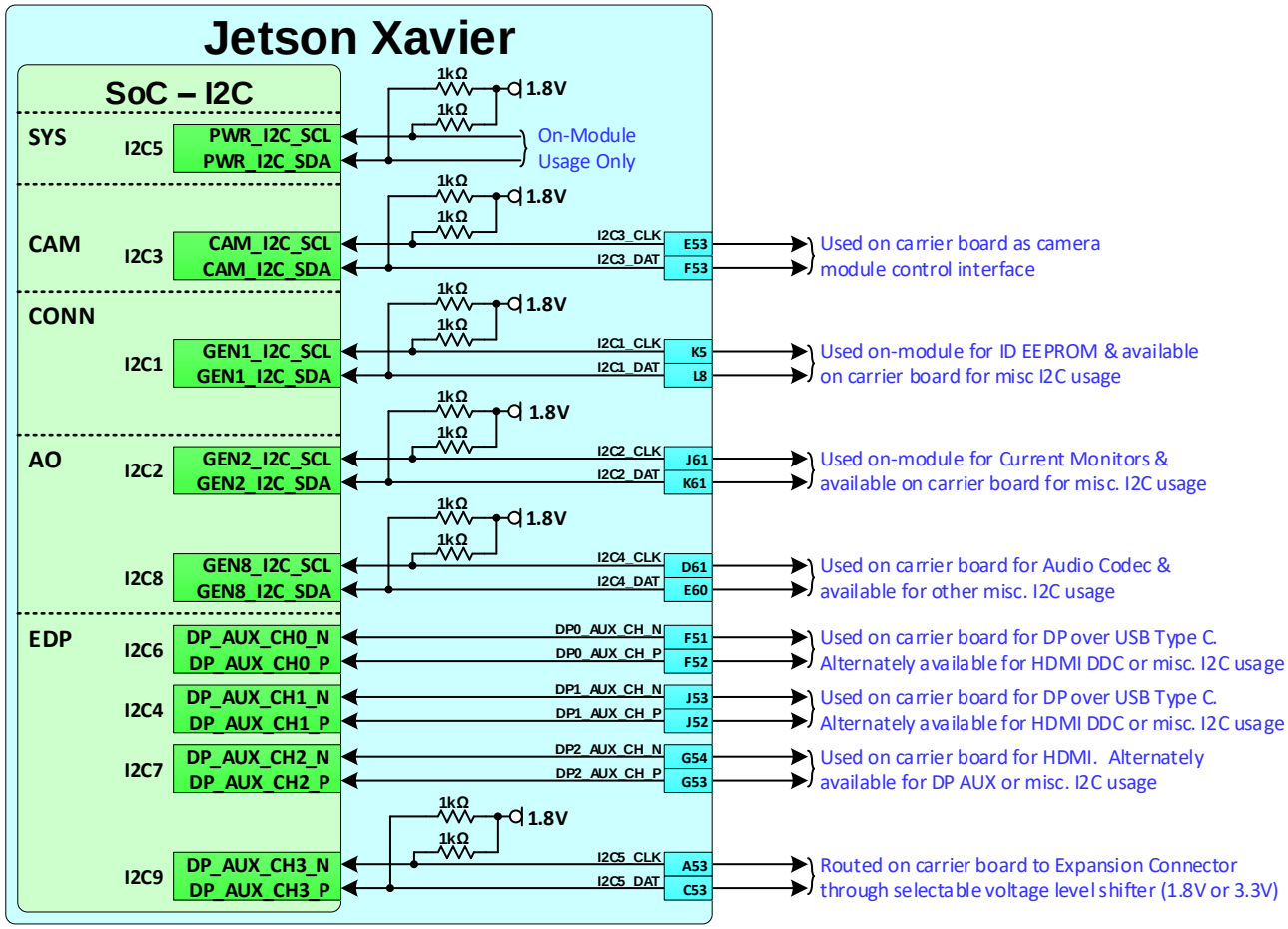
Table 65. Jetson Xavier I2C Pin Descriptions

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
K5	I2C1_CLK	GEN1_I2C_SCL	General I2C 1 Clock	ID EEPROM	Bidir	Open-Drain – 1.8V
L8	I2C1_DAT	GEN1_I2C_SDA	General I2C 1 Data		Bidir	Open-Drain – 1.8V
J61	I2C2_CLK	GEN2_I2C_SCL	General I2C 2 Clock	Various	Bidir	Open-Drain – 1.8V
K61	I2C2_DAT	GEN2_I2C_SDA	General I2C 2 Data	Various	Bidir	Open-Drain – 1.8V
F53	I2C3_CLK	CAM_I2C_SCL	General I2C 3 Clock	Camera Connector	Bidir	Open-Drain – 1.8V
E53	I2C3_DAT	CAM_I2C_SDA	General I2C 3 Data		Bidir	Open-Drain – 1.8V
D61	I2C4_CLK	GEN8_I2C_SCL	General I2C 4 Clock	Audio Codec & Camera Connector	Bidir	Open-Drain – 1.8V
E60	I2C4_DAT	GEN8_I2C_SDA	General I2C 4 Data		Bidir	Open-Drain – 1.8V
A53	I2C5_CLK	DP_AUX_CH3_P	General I2C 5 Clock	Expansion Connector	Bidir	Open-Drain – 1.8V
C53	I2C5_DAT	DP_AUX_CH3_N	General I2C 5 Data		Bidir	Open-Drain – 1.8V
F51	DP0_AUX_CH_N	DP_AUX_CH0_N	Display Port 0 Aux– or HDMI DDC SDA	USB Type C Conn. J512 (via Alt Mode Switch)	Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC/I2C)
F52	DP0_AUX_CH_P	DP_AUX_CH0_P	Display Port 0 Aux+ or HDMI DDC SCL		Bidir	
J53	DP1_AUX_CH_N	DP_AUX_CH1_N	Display Port 1 Aux– or HDMI DDC SDA	USB Type C Conn. J513 (via Alt Mode Switch)	Bidir	
J52	DP1_AUX_CH_P	DP_AUX_CH1_P	Display Port 1 Aux+ or HDMI DDC SCL		Bidir	
G54	DP2_AUX_CH_N	DP_AUX_CH2_N	Display Port 2 Aux– or HDMI DDC SDA	HDMI Connector	Bidir	
G53	DP2_AUX_CH_P	DP_AUX_CH2_P	Display Port 2 Aux+ or HDMI DDC SCL		Bidir	

Table 66. I2C Interface Mapping

Ctrlr	Jetson Xavier Pin Names (Xavier Pins)	Usage on Jetson Xavier	Xavier Block	On-Jetson Xavier Pull-up/voltage
I2C1	I2C1_CLK/DAT	ID EEPROM (7h4C)	CONN	1KΩ to 1.8V
I2C2	I2C2_CLK/DAT	Current Monitors (7H40 & 7H41)	AO	1KΩ to 1.8V (also Current Monitors via 1.8V-5V level shifters w/10k pull-ups to 5V)
I2C3	I2C3_CLK/DAT		CAM	1KΩ to 1.8V
I2C4	DP1_AUX_CH_N/P		EDP	1KΩ to 1.8V
I2C5	(PWR_I2C_SCL/SDA) On-module only	PMIC (7H3C), GPU VREG (0X50), CPU VREG (0X40), SOC VREG (0X20), CV VREG (0X30) & Temp Sensor (7H50)	SYS	1KΩ to 1.8V (VREGs via 1.8V-5V level shifters – 10k pull-ups to 5V)
I2C6	DP0_AUX_CH_N/P		EDP	None
I2C7	DP2_AUX_CH_N/P		EDP	None
I2C8	I2C4_CLK/DAT		AO	1KΩ to 1.8V
I2C9	I2C5_CLK/DAT		EDP	1KΩ to 1.8V

Figure 31. I2C Connections



I2C Design Guidelines

Care must be taken to ensure I2C peripherals on same I2C bus connected to Jetson Xavier do not have duplicate addresses. Addresses can be in two forms: 7-bit, with the Read/Write bit removed or 8-bit including the Read/Write bit. Be sure to compare I2C device addresses using the same form (all 7-bit or all 8-bit format).

Table 67. I2C Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Max Frequency	Standard-mode / Fm / Fm+	100 / 400 / 1000	kHz	See Note 1
Topology		Single ended, bi-directional, multiple masters/slaves		
Max Loading	Standard-mode / Fm / Fm+	400	pF	Total of all loads
Reference plane		**GND** or **PWR**		
Trace Impedance		50 – 60	Ω	±15%
Trace Spacing		1x	dielectric	
Max Trace Delay	Standard Mode Fm & Fm+	3400 (~20) 1700 (~10)	ps (in)	

Note:
1. Fm = Fast-mode, Fm+ = Fast-mode Plus
2. Avoid routing I2C signals near noisy traces, supplies or components such as a switching power regulator.
3. No requirement for decoupling caps for **PWR** reference

Table 68. I2C Signal Connections

Jetson Xavier Pin Name	Type	Termination	Description
I2C1_CLK/DAT	I/OD	1kΩ pull-ups to 1.8V on Jetson Xavier	**General I2C 1 Clock\Data.** Connect to **CLK/Data** pins of 1.8V devices
I2C2_CLK/DAT	I/OD	1kΩ pull-ups to 1.8V on Jetson Xavier	**General I2C 2 Clock\Data.** Connect to **CLK/Data** pins of 1.8V devices.
I2C3_CLK/DAT	I/OD	1kΩ pull-ups to 1.8V on Jetson Xavier	**General I2C 3 Clock\Data.** Connect to **CLK/Data** pins of 1.8V devices
I2C4_CLK/DAT	I/OD	1kΩ pull-ups to 1.8V on Jetson Xavier	**General I2C 4 Clock\Data.** Connect to **CLK/Data** pins of 1.8V devices.
I2C5_CLK/DAT	I/OD	1kΩ pull-ups to 1.8V on Jetson Xavier	**General I2C 5 Clock\Data.** Connect to **CLK/Data** pins of 1.8V devices.
DP0_AUX_CH_P/N	I/OD	See eDP/HDMI/DP sections for correct termination	**DP_AUX Channel (eDP/DP) or DDC I2C 2 Clock & Data (HDMI).** Connect to **AUX_CH_P/N** (DP) or **SCL/SDA** (HDMI). Alternately available as I2C IF.
DP1_AUX_CH_P/N	I/OD	See eDP/HDMI/DP sections for correct termination	**DP_AUX Channel (eDP/DP) or DDC I2C 2 Clock & Data (HDMI).** Connect to **AUX_CH_P/N** (DP) or **SCL/SDA** (HDMI). Alternately available as I2C IF.
DP2_AUX_CH_P/N	I/OD	See eDP/HDMI/DP sections for correct termination	**DP_AUX Channel (eDP/DP) or DDC I2C 2 Clock & Data (HDMI).** Connect to **AUX_CH_P/N** (DP) or **SCL/SDA** (HDMI). Alternately available as I2C IF.

Note: 1. If some devices require a different voltage level than others connected to the same I2C bus, level shifters are required.
2. For I2C interfaces that are pulled up to 1.8V, disable the E_IO_HV option for these pads. For I2C interfaces that are pulled up to 3.3V, enable the E_IO_HV option. The E_IO_HV option is selected in the Pinmux registers.

De-bounce

The tables below contain the allowable De-bounce settings for the various I2C Modes.

Table 69. De-bounce Settings (Fast Mode Plus, Fast Mode & Standard Mode)

I2C Mode	Clock Source	Source Clock Freq	I2C Source Divisor	Sm/Fm Divisor	De-bounce Value	I2C SCL Freq
Fm+	PLLP_OUT0	408MHz	5 (0x04)	10 (0x9)	0	1016KHz
					5:1	905.8KHz
					7:6	816KHz
Fm	PLLP_OUT0	408MHz	5 (0x4)	26 (0x19)	7:0	392KHz
Sm	PLLP_OUT0	408MHz	20 (0x13)	26 (0x19)	7:0	98KHz

Note: Sm = Standard Mode.

12.2 SPI

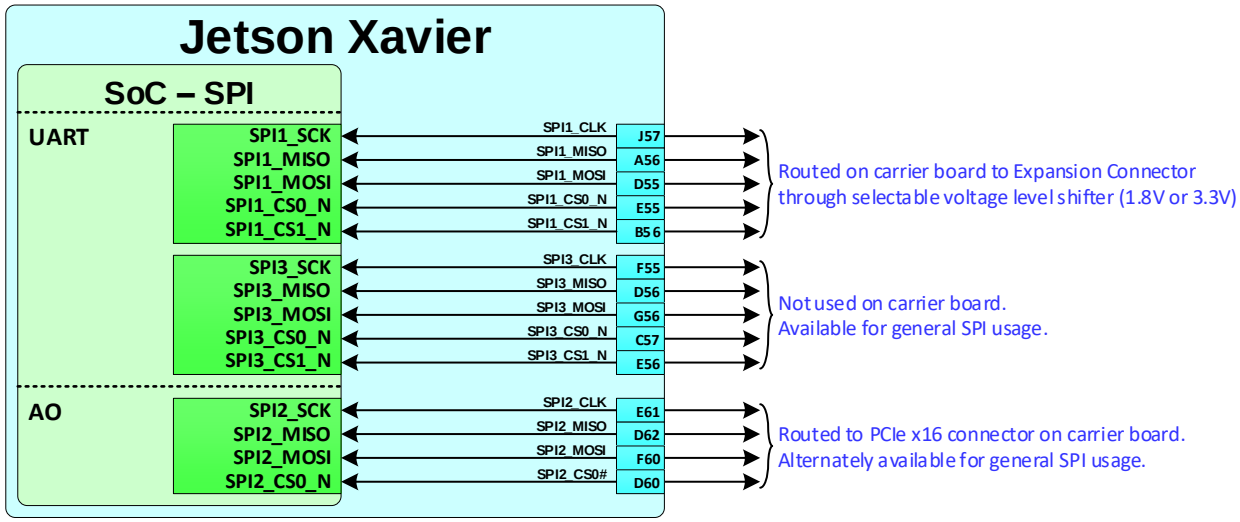
Jetson Xavier brings out three of the SoC SPI interfaces.

Table 70. Jetson Xavier SPI Pin Descriptions

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
J57	SPI1_CLK	SPI1_SCK	SPI 1 Clock	Expansion Connector	Bidir	CMOS – 1.8V
E55	SPI1_CS0_N	SPI1_CS0	SPI 1 Chip Select 0		Bidir	CMOS – 1.8V
B56	SPI1_CS1_N	SPI1_CS1	SPI 1 Chip Select 1		Bidir	CMOS – 1.8V
A56	SPI1_MISO	SPI1_MISO	SPI 1 Master In / Slave Out		Bidir	CMOS – 1.8V
D55	SPI1_MOSI	SPI1_MOSI	SPI 1 Master Out / Slave In		Bidir	CMOS – 1.8V
E61	SPI2_CLK	SPI2_SCK	SPI 2 Clock	PCIe x16 Connector	Bidir	CMOS – 1.8V
D60	SPI2_CS0_N	SPI2_CS0	SPI 2 Chip Select 0		Bidir	CMOS – 1.8V
D62	SPI2_MISO	SPI2_MISO	SPI 2 Master In / Slave Out		Bidir	CMOS – 1.8V
F60	SPI2_MOSI	SPI2_MOSI	SPI 2 Master Out / Slave In		Bidir	CMOS – 1.8V
F55	SPI3_CLK	SPI3_SCK	SPI 3 Clock	Not used	Bidir	CMOS – 1.8V
C57	SPI3_CS0_N	SPI3_CS0	SPI 3 Chip Select 0	Not used	Bidir	CMOS – 1.8V
E56	SPI3_CS1_N	SPI3_CS1	SPI 3 Chip Select 1	Not used	Bidir	CMOS – 1.8V
D56	SPI3_MISO	SPI3_MISO	SPI 3 Master In / Slave Out	PCIe x16 Connector (SLVS_XCLR)	Bidir	CMOS – 1.8V
G56	SPI3_MOSI	SPI3_MOSI	SPI 3 Master Out / Slave In	PCIe x16 Connector (SLVS_XCE)	Bidir	CMOS – 1.8V

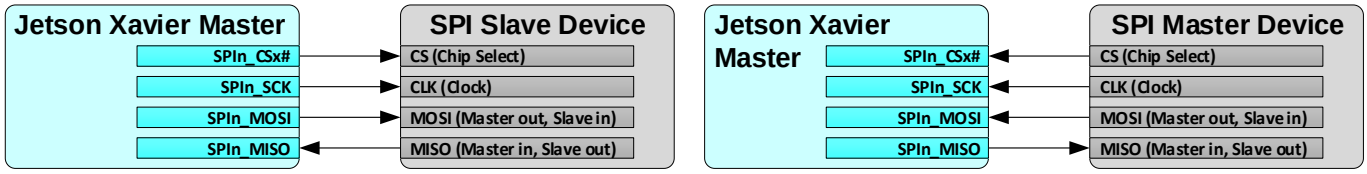
Note: The Direction depends on whether Xavier is the master or slave. If Xavier is master, the clock, chip select & MOSI are outputs and MISO is an input. If Xavier is slave, the clock, chip select & MOSI are inputs and MISO is an output.

Figure 32. SPI Connections



The figure below shows the basic SPI connections.

Figure 33. Basic SPI Master/Slave Connections



SPI Design Guidelines

Figure 34. SPI Point-Point Topology

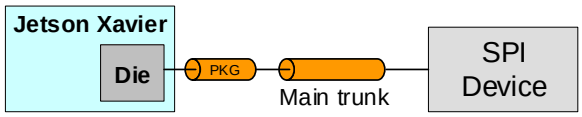


Figure 35. SPI Star Topologies

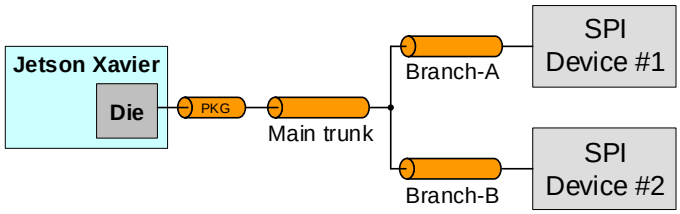


Figure 36. SPI Daisy Topologies

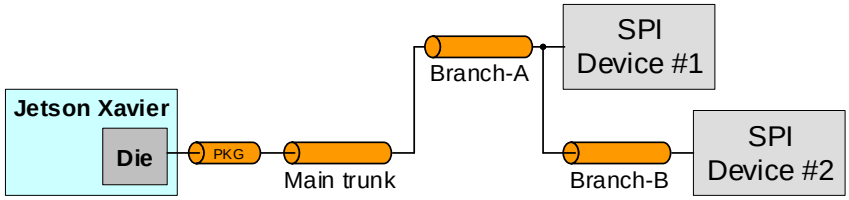


Table 71. SPI Interface Signal Routing Requirements

Parameter		Requirement	Units	Notes
Max Frequency		65	MHz	
Configuration / Device Organization		3	load	
Max Loading (total of all loads)		15	pF	
Reference plane		**GND**		
Breakout Region Impedance		Minimum width & spacing		
Max PCB breakout delay		75	ps	
Trace Impedance		50 – 60	Ω	±15%
Via proximity (Signal to reference)		< 3.8 (24)	mm (ps)	See Note 1
Trace spacing	Microstrip / Stripline	4x / 3x	dielectric	
Max Trace Length/Delay (PCB Main Trunk)	Point-Point	195 (1228)	mm (ps)	
For **MOSI, MISO, SCK** & **CS**	2x-Load Star/Daisy	120 (756)		
Max Trace Length/Delay (Branch-A) for **MOSI, MISO, SCK** & **CS**	2x-Load Star/Daisy	75 (472)	mm (ps)	
Max Trace Length/Delay (Branch-B) for **MOSI, MISO, SCK** & **CS**	2x-Load Star/Daisy	75 (472)	mm (ps)	
Max Trace Length/Delay Skew from **MOSI, MISO** & **CS** to **SCK**		16 (100)	mm (ps)	At any point

Note: Up to 4 signal Vias can share a single GND return Via

Table 72. SPI Signal Connections

Jetson Xavier Pin Names	Type	Termination	Description
SPI[3:1]_CLK	I/O		**SPI Clock.:** Connect to Peripheral **CLK** pin(s)
SPI[3:1]_MOSI	I/O		**SPI Data Output:** Connect to Slave Peripheral **MOSI** pin(s)
SPI[3:1]_MISO	I/O		**SPI Data Input:** Connect to Slave Peripheral **MISO** pin(s)
SPI[3:1]_CS[1:0]_N SPI2_CS0_N	I/O		**SPI Chip Selects.:** Connect one **CS_N** pin per SPI IF to each Slave Peripheral **CS** pin on the interface

Table 73. Recommended SPI observation (test) points for initial boards

Test Points Recommended	Location
One for each SPI signal line used	Near Jetson Xavier & Device pins.

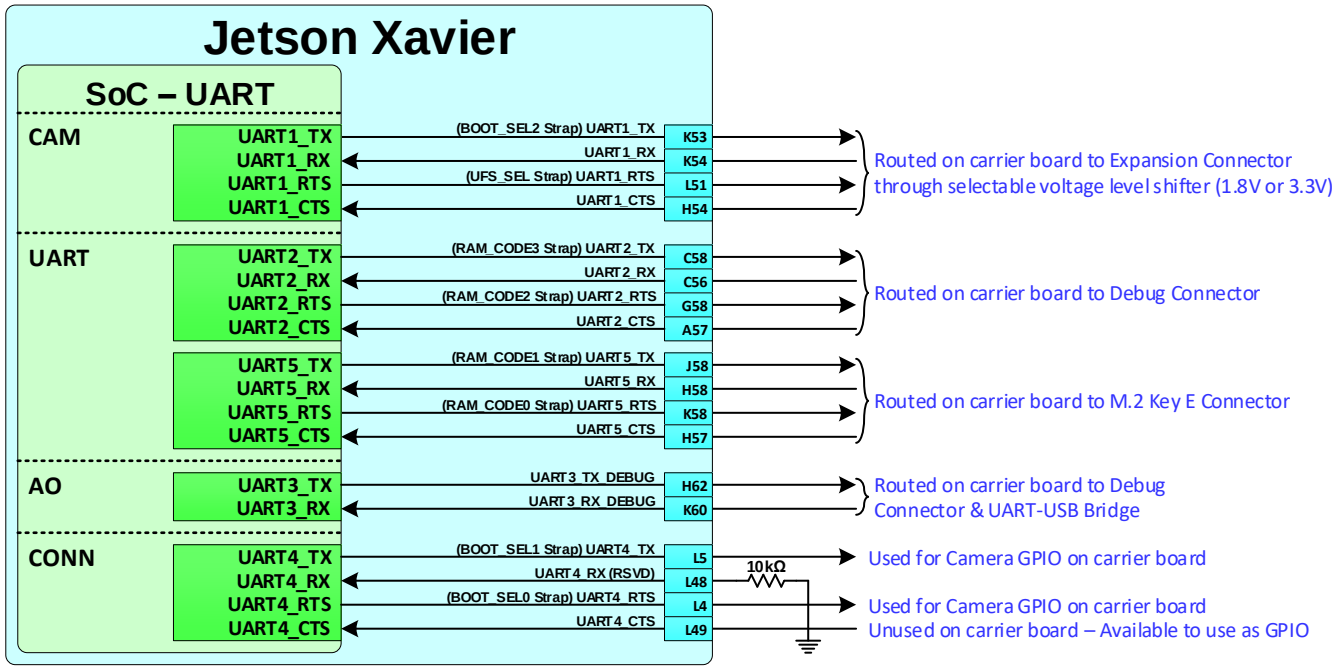
12.3 UART

Jetson Xavier brings five UARTs out to the main connector. See the Jetson Xavier UART Connections figure or typical assignments of the UARTs.

Table 74. Jetson Xavier UART Pin Descriptions

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
K54	UART1_RX	UART1_RX	UART 1 Receive	Expansion Connector via level shifter	Input	CMOS – 1.8V
K53	UART1_TX	UART1_TX	UART 1 Transmit		Output	CMOS – 1.8V
H54	UART1_CTS	UART1_CTS	UART 1 Clear to Send		Input	CMOS – 1.8V
L51	UART1_RTS	UART1_RTS	UART 1 Request to Send		Output	CMOS – 1.8V
C56	UART2_RX	UART2_RX	UART 2 Receive	UART-USB (MicroB) Bridge for Debug	Input	CMOS – 1.8V
C58	UART2_TX	UART2_TX	UART 2 Transmit		Output	CMOS – 1.8V
A57	UART2_CTS	UART2_CTS	UART 2 Clear to Send		Input	CMOS – 1.8V
G58	UART2_RTS	UART2_RTS	UART 2 Request to Send		Output	CMOS – 1.8V
K60	UART3_RX_DEBUG	UART3_RX	Debug UART Receive		Input	CMOS – 1.8V
H62	UART3_TX_DEBUG	UART3_TX	Debug UART Transmit		Output	CMOS – 1.8V
H58	UART5_RX	UART5_RX	UART 5 Receive	M.2 Key E Connector	Input	CMOS – 1.8V
J58	UART5_TX	UART5_TX	UART 5 Transmit		Output	CMOS – 1.8V
H57	UART5_CTS	UART5_CTS	UART 5 Clear to Send		Input	CMOS – 1.8V
K58	UART5_RTS	UART5_RTS	UART 5 Request to Send		Output	CMOS – 1.8V

Figure 37. Jetson Xavier UART Connections



Note:
- Note that UART4 pins do not support UART functionality and UART4_RX pin is reserved and must be tied to GND through a 10kΩ resistor. See the routing requirements in the "Reserved UART4_RX Routing Requirements" table. UART4_TX, UART4_RTS & UART4_CTS are available for use as GPIOs.
- Care must be taken that any of the UART pins with straps associated with them are not pulled up/down or driven up/down by connected devices that would affect the strap level at power-on.

Table 75. UART Signal Connections

Ball Name	Type	Termination	Description
UART[5,2:1]_TX **UART3_TX_DEBUG**	O		**UART Transmit:** Connect to Peripheral **RXD** pin of device
UART[5,2:1]_RX **UART3_RX_DEBUG**	I		**UART Receive:** Connect to Peripheral **TXD** pin of device
UART[5,2:1]_CTS	I		**UART Clear to Send:** Connect to Peripheral **RTS_N** pin of device
UART[5,2:1]_RTS	O		**UART Request to Send:** Connect to Peripheral **CTS** pin of device

The requirements for the routing if the trace from the UART4_RX pin to the resistor to GND are listed in the table below.

Table 76. Reserved UART4_RX Routing Requirements

Parameter	Requirement	Units	Notes
Minimum Trace spacing to other signals	3x (4x preferred)	dielectric	
Minimum distance from UART4_RX Plated-through hole (PTH) and other signal PTHs.	1.5	mm	
Trace Length to resistor to GND	5-15	mm	

12.4 CAN

Jetson Xavier brings two CAN (Controller Area Network) interfaces out to the main connector.

Table 77. Jetson Xavier CAN Pin Descriptions

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
F58	CAN0_DIN	CAN0_DIN	CAN 0 Receive	Expansion Header	Input	CMOS 3.3V
D59	CAN0_DOUT	CAN0_DOUT	CAN 0 Transmit		Output	CMOS 3.3V
B61	CAN1_DIN	CAN1_DIN	CAN 1 Receive		Input	CMOS 3.3V
H61	CAN1_DOUT	CAN1_DOUT	CAN 1 Transmit		Output	CMOS 3.3V
B62	GPIO08	CAN1_STB	GPIO / Digital Mic Input Data		Input	CMOS 3.3V
C61	GPIO09	CAN1_EN	GPIO / Digital Mic Input Clock		Output	CMOS 3.3V
E59	GPIO06	CAN0_EN	GPIO	PCIe REFCLK mux Select	Output	CMOS 3.3V
F59	GPIO07	CAN0_WAKE	GPIO	Unused	Input	CMOS 3.3V
A62	GPIO10	CAN1_WAKE	GPIO	USB PD Controller Interrupt	Input	CMOS 3.3V

Figure 38. Jetson Xavier CAN Connections

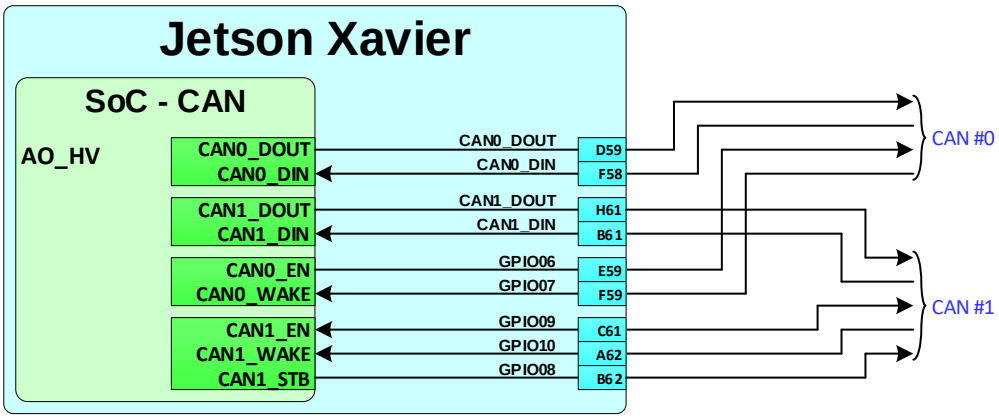


Table 78. CAN Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Data Rate / Frequency	1	Mbps / MHz	
Configuration / Device Organization	1	load	
Reference plane	**GND**		
Trace Impedance	50	Ω	±15%
Via proximity (Signal via to **GND** return via)	< 3.8 (24)	mm (ps)	See Note 1
Trace spacing Microstrip / Stripline	4x / 3x	dielectric	
Max Trace Length (for **RX** & **TX** only)	223 (1360)	mm (ps)	See Note 2
Max Trace Length/Delay Skew from **RX** to **TX**	8 (50)	mm (ps)	See Note 2

Table 79. CAN Signal Connections

Jetson Xavier Pin Name (Function)	Type	Termination	Description
CANx_DOUT	O		**CAN Data Output:** Connect to matching pin of device
CANx_DIN	I		**CAN Input:** Connect to Peripheral pin of device
GPIO06 (CAN0_EN) **GPIO09 (CAN1_EN)**	O		**CAN Enable:** Connect to matching pin of device
GPIO08 (CAN1_STB)	O		**CAN 1 Standby:** Connect to matching pin of device
GPIO07 (CAN0_WAKE) **GPIO10 (CAN1_WAKE)**	I		**CAN Wake:** Connect to matching pin of device

13.0 FAN

Jetson Xavier provides PWM and Tachometer functionality for controlling a fan as part of the thermal solution. Information on the PWM and Tachometer pins/functions can be found in the following locations:

Jetson Xavier Module Pin Mux:

- This is used to configure the FAN_PWM & FAN_TACH pins. The FAN_PWM pin is configured as GP_PWM4. The FAN_TACH pin is configured as NV_THERM_FAN_TACH.

Xavier Technical Reference Manual:

- Functional descriptions and related registers can be found in the TRM for the FAN_PWM (PWM chapter) & FAN_TACH (Tachometer chapter) functions.

Jetson Xavier Developer Kit Carrier Board Specification:

- The document contains the maximum current capability of the VDD_5V supply in the Interface Power chapter. The fan is powered by this supply on the Jetson Xavier Developer Kit carrier board.

Table 80. Jetson Xavier Fan Pin Descriptions

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
K62	FAN_PWM	TOUCH_CLK	Fan Pulse Width Modulation signal	Fan Circuit/Connector	Output	CMOS – 1.8V
E54	FAN_TACH	SOC_GPIO22	Fan Tachometer signal	Fan Circuit/Connector	Input	CMOS – 1.8V

Figure 39. Jetson Xavier Fan Connection Example

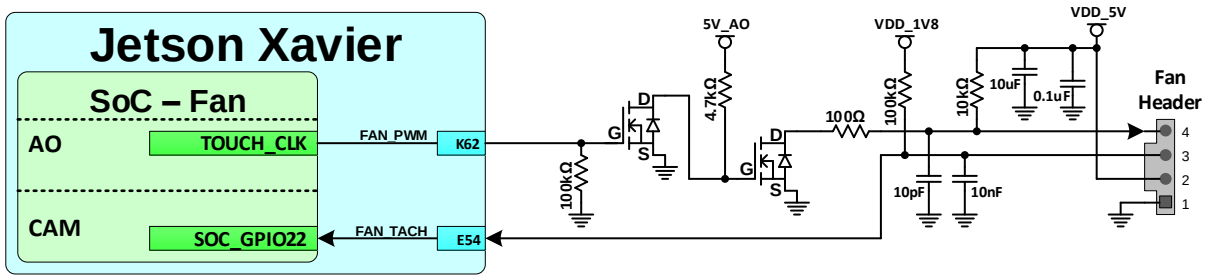
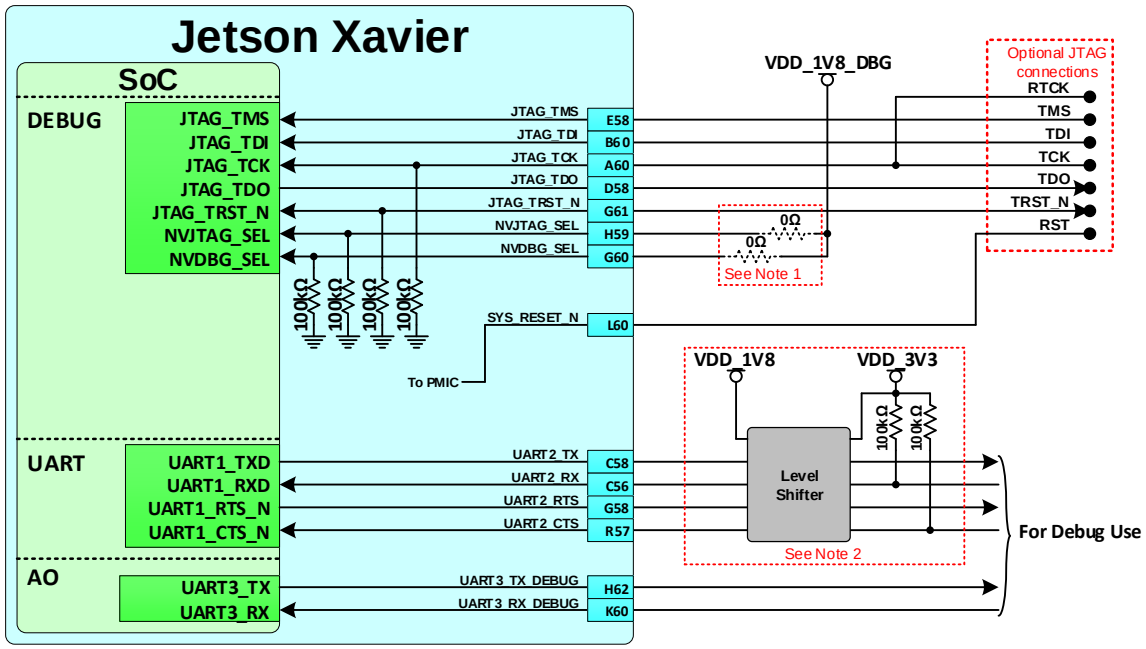


Table 81. Fan Signal Connections

Jetson Xavier Pin Name	Type	Termination	Description
FAN_PWM	O	100kΩ pulldown to GND.	**Fan Pulse Width Modulation:** Connect through FET as shown in the Jetson Xavier Fan Connections figure.
FAN_TACH	I	100kohm pullup to VDD_1V8	**Fan Tachometer:** Connect to TACH pin on fan connector.

14.0 DEBUG & STRAPPING

Figure 40. JTAG/UART Debug Connections



Notes:
1. NVJTAG_SEL is left unconnected (pulled down on module) for normal operation and pulled to 1.8V for Boundary Scan Mode.
2. NVDBG is left unconnected (pulled down on module) for normal operation and pulled to 1.8V for alternate debug modes (debug over USB, etc.).
3. If level shifter is implemented, pull-ups are required the RX & CTS lines on the non-SoC side of the level shifter. This is required to keep the inputs from floating and toggling when no device is connected to the debug UART.
4. Check preferred JTAG debugger documentation for JTAG PU/PD recommendations.

14.1 JTAG

JTAG is not required but may be useful for new design bring-up or for Boundary Scan.

Table 82. Jetson Xavier JTAG Pin Descriptions

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
A60	JTAG_TCK	JTAG_TCK	JTAG Test Clock	JTAG Connector	Input	CMOS – 1.8V
B60	JTAG_TDI	JTAG_TDI	JTAG Test Data In		Input	CMOS – 1.8V
D58	JTAG_TDO	JTAG_TDO	JTAG Test Data Out		Output	CMOS – 1.8V
E58	JTAG_TMS	JTAG_TMS	JTAG Test Mode Select		Input	CMOS – 1.8V
G61	JTAG_TRST_N	JTAG_TRST_N	JTAG Test Reset		Input	CMOS – 1.8V
G60	NVDBG_SEL	NVDBG_SEL	NVIDIA Debug Select	Unused – Driven to GND	Input	CMOS – 1.8V
H59	NVJTAG_SEL	NVJTAG_SEL	NVIDIA JTAG Select		Input	CMOS – 1.8V

Table 83. JTAG Signal Connections

Jetson Xavier Pin Name (other)	Type	Termination	Description
JTAG_TMS	I		**JTAG Mode Select:** Connect to **TMS** pin of connector
JTAG_TCK	I	100kΩ to **GND** (on Jetson Xavier)	**JTAG Clock:** Connect to **TCK** pin of connector
JTAG_TDO	O		**JTAG Data Out:** Connect to **TDO** pin of connector
JTAG_TDI	I		**JTAG Data In:** Connect to **TDI** pin of connector
JTAG_RTCK	I		**JTAG Return Clock:** Connect to **RTCK** pin of connector
JTAG_TRST_N	I	100kΩ to **GND** & 0.1uF to **GND** (on Jetson Xavier)	**JTAG General Purpose Pin #0:** Connect to **TRST** pin of connector

NVJTAG_SEL		100kΩ to **GND** (on Jetson Xavier)	**NVIDIA JTAG Select:** Used as select - Normal operation: Leave series resistor from **NVJTAG_SEL** not stuffed. - Scan test mode: Connect **NVJTAG_SEL** to **VDD_1V8** (install 0Ω resistor as shown).
NVDBG_SEL		100kΩ to **GND** (on Jetson Xavier)	**NVIDIA Debug Select:** Used as select - Normal operation: Leave series resistor from **NVDBG_SEL** not stuffed. - Advanced Debug modes: Connect **NVDBG_SEL** to **VDD_1V8** (install 0Ω resistor as shown).

14.2 Debug UART

Jetson Xavier provides UART2 & UART3_DEBUG for debug purposes. The connections are shown in Figure 40 and described in the table below.

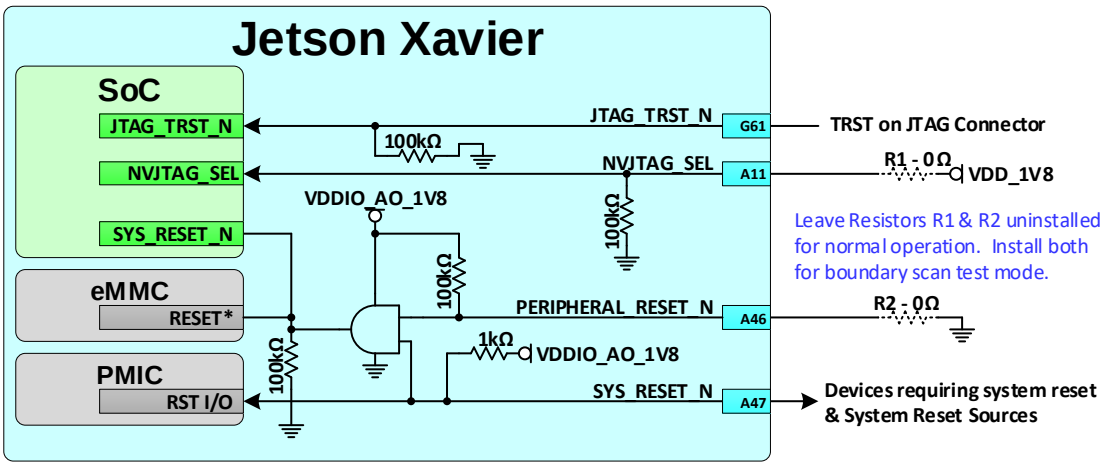
Table 84. Debug UART Connections

Jetson Xavier Pin Name	Type	Termination	Description
UART2_TX **UART3_TX_DEBUG**	O		**UART Transmit:** Connect to **RX** pin of serial device
UART2_RX **UART3_RX_DEBUG**	I	If level shifter implemented, 100kΩ to supply on the non-Jetson Xavier side of the device.	**UART Receive:** Connect to **TX** pin of serial device
UART2_RTS	O		**UART Request to Send:** Connect to **CTS** pin of serial device
UART2_CTS	I	If level shifter implemented, 100kΩ to supply on the non-Jetson Xavier side of the device.	**UART Clear to Send:** Connect to **RTS** pin of serial device

14.3 Boundary Scan Test Mode

To support Boundary Scan Test mode, the SoC NVJTAG_SEL pin must be pulled high and The SoC must be held in reset without resetting the PMIC. This is done using the PERIPHERAL_RESET_N pin on the module. The figure below illustrates this. Other requirements related to supporting Boundary Scan Test mode are described in the "Xavier Boundary Scan Requirements & Usage" document.

Figure 41. Boundary Scan Connections



14.4 Strapping Pins

Jetson Xavier has one strap (FORCE_RECOV#) that is intended to be used on the carrier board. That strap is used to enter Force Recovery mode. The other straps mentioned in this section are for use on the module by Nvidia only. They are included here as their state at power-on must be kept at the level selected on the module.

Figure 42. Jetson Xavier Strap Connections

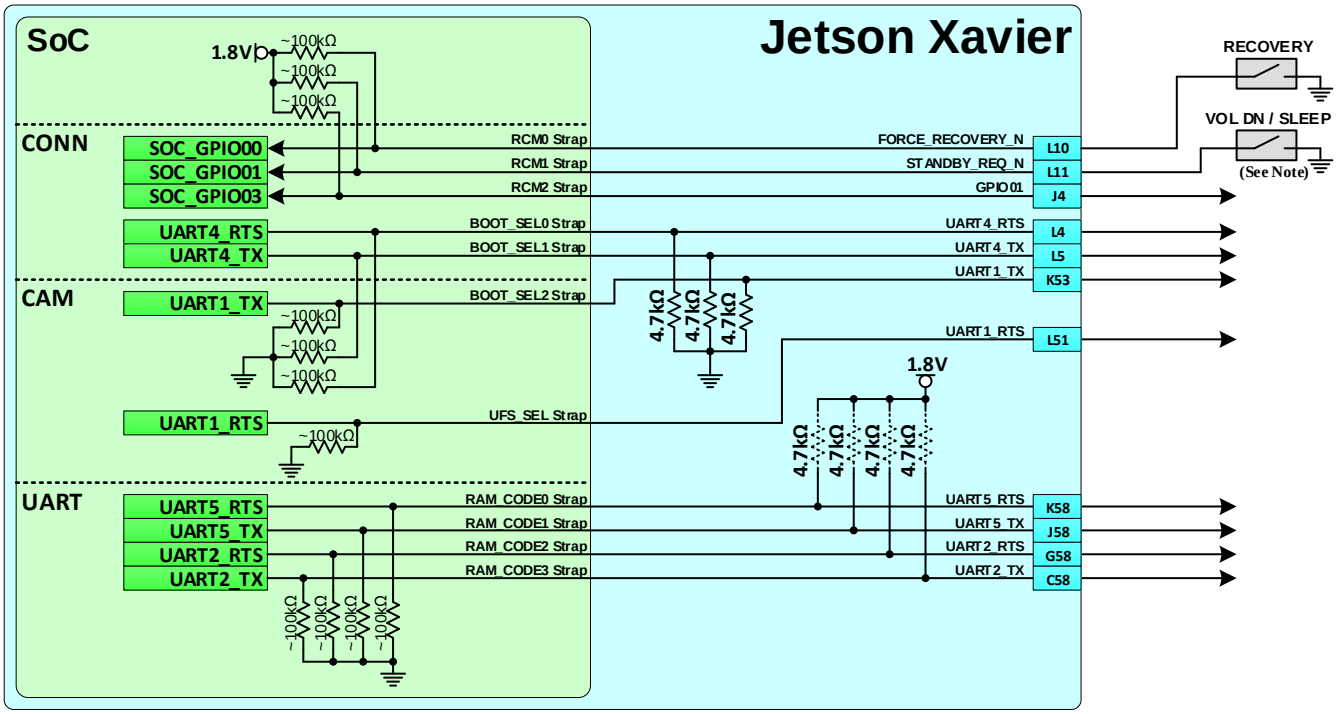


Table 85. Power-on Strapping Breakdown

Jetson Xavier Pin Name	SoC Ball Name	Strap Options	SoC Internal PU/PD	Jetson Xavier PU/PD	Description
FORCE_RECOVERY_N	**SOC_GPIO00**	RCM0	~100kΩ PU	na	Recovery Mode [1:0] x1: Normal boot from secondary device 10: Forced Recovery Mode 00: Reserved ***See critical warning in note 1***
STANDBY_REQ_N	**SOC_GPIO01**	RCM1	~100kΩ PU	na	
UART2_TX	**UART2_TX**	RAM_CODE3	~100kΩ PD	4.7KΩ PU or PD	[3:2] Selects secondary boot device configuration set within the BCT. For Nvidia use only. [1:0] Selects DRAM configuration set within the BCT. For Nvidia use only. ***See critical warning in Note 2***.
UART2_RTS	**UART2_RTS**	RAM_CODE2	~100kΩ PD	4.7KΩ PU or PD	
UART5_TX	**UART5_TX**	RAM_CODE1	~100kΩ PD	4.7KΩ PU or PD	
UART5_RTS	**UART5_RTS**	RAM_CODE0	~100kΩ PD	4.7KΩ PU or PD	
UART1_TX	**UART1_TX**	BOOT_SELECT2	~100kΩ PD	4.7kΩ PD	Software reads value and determines Boot device to be configured and used 000 = eMMC x8 BootModeOFF, 512-byte page. Maps to SDMMC w/config=0x0001 size. 26MHz 001 – 111 Reserved ***See Note 3 & 5. See critical warning in Note 4.***
UART4_TX	**UART4_TX**	BOOT_SELECT1	~100kΩ PD	4.7kΩ PD	
UART4_RTS	**UART4_RTS**	BOOT_SELECT0	~100kΩ PD	4.7kΩ PD	
UART1_RTS	**UART1_RTS**	UFS_SEL	~100kΩ PD	na	Indicates whether UFS sideband signals (REFCLK & RST) logic level will be 1.2V or 1.8V. 0 = 1.2V (Required strap setting – See note 5) 1 – 1.8V (not allowed)

Note:

1. If the STANDBY_REQ_N pin is used in a design, it must not be driven or pulled low during power-on at the same time as FORCE_RECOVERY_N is pulled low for Recovery Mode as this would change the strapping and select a reserved mode. ***Violating this requirement will prevent the system from entering Recovery Mode.***
2. If UART5_RTS, UART5_TX, UART2_RTS or UART2_TX are used in a design, they must not be driven or pulled high or low during power-on. ***Violating this requirement can change the RAM_CODE strapping & result in functional failures.***
3. The above BOOT_SELECT option is only in effect in "regular boot" conditions i.e. coldboot. If "Forced Recovery" mode is detected (FORCE_RECOVERY_N low at boot), that mode takes precedence over the eMMC boot device choice.
4. If UART4_RTS, UART4_TX or UART1_TX are used in a design, they must not be driven or pulled high during power-on as this would affect the BOOT_SELECT strapping. ***Violating this requirement will likely prevent the system from booting.***
5. The UFS_SEL strap is intended to select 1.2V or 1.8V operation on the REFSLK/RST sideband signals. Since the power tree default for VDDIO_UFS is 1.2V, the strap should always be low. If UART1_RTS is used in a design, it must not be driven or pulled high during power-on. ***Violating this requirement can change the UFS_SEL strapping & result in UFS functional failures.***
6. eMMC boot does not use either the normal boot mode or alternate boot mode supported by the eMMC spec. The SoC BootROM uses the Card Identification mode for booting from eMMC.

15.0 PADS

15.1 MPIO Pad Behavior when Associated Power Rail is Enabled

Jetson Xavier CZ (see note) type MPIOs pins may glitch when the associated power rail is enabled or disabled. Designers should take this into account. MPIOs of this type that must maintain a low state even while the power rail is being ramped up or down may require special handling. The Pin Descriptions section of Jetson Xavier Data Sheet includes the pin type information.

15.2 Schmitt Trigger Usage

The MPIO pins have an option to enable or disable Schmitt Trigger mode on a per-pin basis. This mode is recommended for pins used for edge-sensitive functions such as input clocks, or other functions where each edge detected will affect the operation of a device. Schmitt Trigger mode provides better noise immunity, and can help avoid extra edges from being "seen" by the SoC inputs. Input clocks include the I2S & SPI clocks (TBD) when SoC is in slave mode. The TBD pin is another input that could be affected by noise on the signal edges. The TBD pin (SoC TBD CLK function), while used to output the SD clock, also samples the clock at the input to help with read timing. Therefore, the TBD pin may benefit from enabling Schmitt Trigger mode. Care should be taken if the Schmitt Trigger mode setting is changed from the default initialization mode as this can have an effect on interface timing.

15.3 Pins Pulled/Driven High During Power-on

Jetson Xavier is powered up before the carrier board (See Power Sequencing section). Some of the pins are pulled or driven high either by The SoC or by pull-up resistors on the module. The pins on Jetson Xavier that are pulled/driven high by The SoC can be found in the Module Pinmux spreadsheet. The pins that have pull-up resistors on the module are listed in the Jetson Xavier Signal Terminations section of the Design Checklist chapter. Care must be taken on the carrier board design to ensure that any of these pins that connect to devices on the carrier board (or devices connected to the carrier board) do not cause damage or excessive leakage to those devices. Some of the ways to avoid issues with sensitive devices are:

- External pull-downs on the carrier board that are strong enough to keep the signals low are one solution, given that this does not affect the function of the pin. This will not work pins actively driven high by default.
- Buffers or level shifters can be used to separate the signals from devices that may be affected. The buffer/shifter should be disabled until the device power is enabled.

15.4 Pad Drive Strength

The table below provides the maximum MPIO pad output drive current when the pad is configured for the maximum DRVUP/DRVDN values (11111b). The MPIO pad types include the ST, DD, CZ and LV_CZ type pads. The pad types can be found in the Jetson Xavier Module Data Sheet.

Table 86. MPIO Maximum Output Drive Current

IOL/IOH	Pad Type	VOL	VOH
+/- 1mA	ST	0.15*VDD	0.825*VDD
+/- 1mA	DD	0.15*VDD	0.8*VDD
+/- 1mA	CZ (1.8V mode)	0.15*VDD	0.85*VDD
+/- 1mA	CZ (3.3V mode)	0.15*VDD	0.85*VDD
+/- 1mA	LV_CZ	0.15*VDD	0.85*VDD
+/- 2mA	ST	0.15*VDD	0.7*VDD
+/- 2mA	DD	0.175*VDD	0.7*VDD
+/- 2mA	CZ (1.8V mode)	0.25*VDD	0.75*VDD
+/- 2mA	CZ (3.3V mode)	0.15*VDD	0.75*VDD
+/- 2mA	LV_CZ	0.25*VDD	0.75*VDD

16.0 UNUSED INTERFACE TERMINATIONS

16.1 Unused MPIO Interfaces

The following Jetson Xavier pins (& groups of pins) are Jetson Xavier MPIO (Multi-purpose Standard CMOS Pad) pins that support either special function IOs (SFIO) and/or GPIO capabilities. Any unused pins or portions of pin groups listed below that are not used can be left unconnected.

Table 87. Unused MPIO pins / Pin Groups

Jetson Xavier Pins / Pin Groups		Jetson Xavier Pins / Pin Groups
I2Sx, AUD_MCLK, DSPKx, DMICx		GP_PWMx
SDMMCx		CCLAx
MIPI_TRC_x		SCE_SAFE_STATE
EQOSx		SOC_THERMx
QSPIx		PMICINTR
Ux3_x		GPIO_AO_RET
I2Cx		WDT_RESET_x
SPIx		TOUCH_x
CANx		EXTPERIPHx
VGPx		IGPUx
SLVSx		SATA_LED_ACTIVE
IQCx		NV_THERMx
UFSx		ISTCTRLx
PEx, PEX_CLKx		DCx
DP_AUXx		DGPU_x

16.2 Unused SFIO Interface Pins

See the Unused SFIO (Special Function I/O) interface pins section in the Checklist at the end of this document.

17.0 DESIGN CHECKLIST

The checklist below is intended to help ensure that the correct connections have been made in a design. The check items describe connections for the various interfaces and the "Same/Diff/NA" column is intended to be used to indicate whether the design matches the check item description, is different, or is not applicable to the design.

Table 88. Checklist

Check Item Description			Same/Diff/NA
Jetson Xavier Signal Terminations (Present on the module - shown for reference only) Note: Internal refers to SoC internal Pull-up/down resistors (value shown is default at Power-on). External refers to resistors added on the module.			
	Parallel Termination	Series Termination	
PCIe			
PEX_L0_CLKREQ_N	External 47KΩ pull-up to 3.3V		
PEX_L0_RST_N	External 47KΩ pull-up to 3.3V		
PEX_L1_CLKREQ_N	External 47KΩ pull-up to 3.3V		
PEX_L1_RST_N	External 47KΩ pull-up to 3.3V		
PEX_L3_CLKREQ_N	External 47KΩ pull-up to 3.3V		
PEX_L3_RST_N	External 47KΩ pull-up to 3.3V		
PEX_L4_CLKREQ_N	External 47KΩ pull-up to 3.3V		
PEX_L4_RST_N	External 47KΩ pull-up to 3.3V		
PEX_L5_CLKREQ_N	External 47KΩ pull-up to 3.3V		
PEX_L5_RST_N	External 47KΩ pull-up to 3.3V		
PEX_WAKE_N	External 47KΩ pull-up to 3.3V		
HDMI/DP/eDP			
DP0_HPD	Internal ~100KΩ pulldown		
DP1_HPD	Internal ~100KΩ pulldown		
DP2_HPD	Internal ~100KΩ pulldown		
I2C			
I2C1_CLK/DAT	External 1KΩ pull-up to 1.8V		
I2C2_CLK/DAT	External 1KΩ pull-up to 1.8V		
I2C3_CLK/DAT	External 1KΩ pull-up to 1.8V		
I2C4_CLK/DAT	External 1KΩ pull-up to 1.8V		
I2C5_CLK/DAT	External 1KΩ pull-up to 1.8V		
SPI			
SPI1_CLK	Internal pull-down		
SPI1_CS0_N	Internal pull-up to 1.8V		
SPI1_CS1_N	Internal pull-up to 1.8V		
SPI1_MISO	Internal pull-up to 1.8V		
SPI1_MOSI	Internal pull-up to 1.8V		
SPI2_CLK	Internal pull-down		
SPI2_MISO	Internal pull-down		
SPI2_MOSI	Internal pull-down		
SPI3_CLK	Internal pull-down		
SPI3_MISO	Internal pull-down		
SPI3_MOSI	Internal pull-down		
SD Card			
SDCARD_CLK	Internal pull-down (~19.5kΩ)		
SDCARD_CMD	Internal pull-down (~19.5kΩ)		
SDCARD_D[3:0]	Internal pull-down (~19.5kΩ)		
GPIO02 (SDCARD_CD#)	Internal pull-down (~100kΩ)		
Ethernet			
RGMII_SMA_MDIO	External 1.5KΩ pull-up to 1.8V		
GPIOs			
GPIO01	Internal pull-up to 1.8V (~100kΩ)		
GPIO02	Internal pull-down (~100kΩ)		
GPIO03	Internal pull-down (~100kΩ)		
GPIO04	Internal pull-down (~100kΩ)		

GPIO05	Internal pull-down (~100kΩ)		
GPIO06	na		
GPIO07	na		
GPIO08	Internal pull-down (~19.5kΩ)		
GPIO09	na		
GPIO10	na		
GPIO11	Internal pull-down (~100kΩ)		
GPIO12	Internal pull-up to 1.8V (~100kΩ)		
GPIO13	Internal pull-down (~100kΩ)		
GPIO14	Internal pull-down (~100kΩ)		
GPIO15	Internal pull-down (~100kΩ)		
GPIO16	Internal pull-down (~100kΩ)		
GPIO17	Internal pull-down (~100kΩ)		
GPIO18	Internal pull-down (~100kΩ)		
GPIO19	Internal pull-down (~100kΩ)		
GPIO20	Internal pull-down (~100kΩ)		
GPIO21	Internal pull-down (~100kΩ)		
GPIO22	Drive low		
GPIO23	Drive low		
GPIO24	Internal pull-down (~100kΩ)		
GPIO25	Internal pull-down (~100kΩ)		
GPIO26	Internal pull-down (~100kΩ)		
GPIO27	Internal pull-down (~100kΩ)		
GPIO28	Internal pull-down (~100kΩ)		
GPIO29	Internal pull-down (~100kΩ)		
GPIO30	Internal pull-down (~100kΩ)		
GPIO31	na		
GPIO32	Internal pull-down (~100kΩ)		
GPIO33	Internal pull-down (~100kΩ)		
GPIO34	Internal pull-down (~100kΩ)		
GPIO35	na		
GPIO36	Internal pull-down (~100kΩ)		
System Control			
FORCE_RECOVERY	External 10kΩ Pull-up to 1.8V		
STANDBY_REQ_N	External 10kΩ Pull-up to 1.8V		
SYS_RESET_N	External 1kΩ Pull-up to 1.8V		
PERIPHERAL_RESET_N	External 100kΩ Pull-up to 1.8V		
CARRIER_POWER_ON	External 10kΩ Pull-up to 3.3V		
JTAG			
JTAG_TCK	External 100kΩ Pull-down	–	
JTAG_TRST_N	External 100kΩ Pull-down	–	
NVJTAG_SEL	External 100kΩ Pull-down		
NVDBG_SEL	External 100kΩ Pull-down		
Pins used for Xavier Straps			
FORCE_RECOVERY_N (RCM0)	Internal 10kΩ Pull-up to 1.8V		
STANDBY_REQ_N (RCM1)	Internal 10kΩ Pull-up to 1.8V		
GPIO01 (RCM2)	Internal 100kΩ Pull-up to 1.8V		
UART2_TX (RAM_CODE3)	Internal 100kΩ Pull-down & External 4.7kΩ Pull-down or Pull-up to 1.8V		
UART2_RTS (RAM_CODE2)	Internal 100kΩ Pull-down & External 4.7kΩ Pull-down or Pull-up to 1.8V		
UART5_TX (RAM_CODE1)	Internal 100kΩ Pull-down & External 4.7kΩ Pull-down or Pull-up to 1.8V		
UART5_RTS (RAM_CODE0)	Internal 100kΩ Pull-down & External 4.7kΩ Pull-down or Pull-up to 1.8V		
UART1_TX (BOOT_SELECT2)	External 100kΩ Pull-down		
UART4_TX (BOOT_SELECT1)	External 100kΩ Pull-down		
UART4_RTS (BOOT_SELECT0)	External 100kΩ Pull-down		

Carrier Board Signal Terminations (To be implemented on the carrier board for interfaces that are used)						
	Parallel Termination			Series Termination		
USB/PCIe/UFS						
UPHY_TX[11:0]_N/P **NVHS0_TX[7:0]_N/P**				USB_SS/PCIe (GEN2): 0.1uF capacitors UFS: 0.01uF AC capacitors PCIe GEN4: 0.22uF capacitors		
UPHY_RX[11:0]_N/P **NVHS0_SLVS_RX[7:0]_N/P**				USB_SS/PCIe (GEN2): 0.1uF capacitors if directly connected UFS: 0.01uF AC capacitors PCIe GEN4: 0.22uF capacitors if directly connected.		
Ethernet						
RGMII_SMA_MDIO	External 2.2KΩ pull-up to 1.8V					
eDP/DP						
HDMI_DPx_TXDP/N[3:0]				0.1uF capacitors		
DPx_AUX_CH_N/P				0.1uF capacitors		
DPx_HPD	External 1Mohm go **GND** before level shifter (module side) & 100kΩ to **GND** after level shifter (connector side). 220pf capacitor to **GND** after series resistor.			Module pin to 1.8V-5.0V level shifter to 100kΩ series resistor to connector		
HDMI						
HDMI_DPx_TXDP/N[3:0]	499Ω, 1% resistors to 600Ω (@100MHz) beads on each together to FET to **GND**			0.1uF capacitors then 6.04Ω, 1% series resistors (to be tuned to meet signal requirements)		
DPx_AUX_CH_N/P	10kΩ pull-ups to **VDD_3V3** on module side of level shifters. 2kohm pull-ups to VDD_5V0_HDMI_CON on connector side of level shifters			Module to 3.3V-5.0V level shifters to connector		
DPx_HPD	10kΩ pull-ups **to VDD_1V8** before level shifter (module side) & 100kΩ to GND after level shifter (connector side). 220pf capacitor to **GND** after series resistor.			Module pin to 1.8V-5.0V level shifter to 100kΩ series resistor to connector		
HDMI_CEC	See carrier board reference schematics					
GPIOs						
GPIO02	External 100kΩ Pull-up to VDD_1V8					
GPIO07	External 10kΩ Pull-up to VAUX_3V3					
GPIO10	External 2.2kΩ Pull-up to VDD_3V3					
GPIO20	External 100kΩ Pull-down					
GPIO22	External 100kΩ Pull-up to VDD_1V8					
GPIO23	External 100kΩ Pull-up to VDD_1V8					
GPIO26	External 47kΩ Pull-up to VDD_1V8					
GPIO28	External 10kΩ Pull-up to VDD_1V8_DBG					
GPIO30	External 47kΩ Pull-up to VDD_1V8					
GPIO33	External 2.2kΩ Pull-up to VDD_1V8					
GPIO34	External 47kΩ Pull-up to VDD_1V8					
GPIO36	External 47kΩ Pull-down					
System						
MODULE_POWER_ON	External 100kΩ Pull-up to 5V					
SYS_RESET_N	External 47kΩ Pull-up to VDD_1V8					
FAN						
FAN_PWM	External 100kΩ Pull-down					
FAN_TACH	External 100kΩ Pull-up to VDD_1V8					
JTAG						
JTAG_TMS	External 47kΩ Pull-up to VDD_1V8					
JTAG_TCK	External 47kΩ Pull-down					
JTAG_TDO	External 47kΩ Pull-down					
JTAG_TDI	External 47kΩ Pull-up to VDD_1V8					
Power						
Jetson Xavier Power Supplies						
Supply (Carrier Board)	Usage		(V)	Supply Type	Source	Enable

SYS_VIN_HV	Main High Voltage Supply	9-20	USB Type C or AC/DC Adapter	**SYS_VIN_HV** over Module pins.	Power-on	
SYS_VIN_MV	Main 5.0V Supply	5.0	DC-DC	**SYS_VIN_MV** over module pins.	Power-on	
VCC_RTC	Real-time clock supply	1.65-5.5	PMIC is supply when charging cap or coin cell	Super cap or coin cell is source when system power removed	na	
Carrier Board Supplies						
VCC_SRC_FET	Main High Voltage supply	9-20	USB Type C or AC/DC Adapter	**SYS_VIN_HV** over Module pins.	Power-on	
VDD_5V	Main 5V supply from Module	5.0	DC-DC	**SYS_VIN_MV** over module pins	Power-on	
5V_AO	Main 5V Always-on supply	5.0	DC/DC	**VCC_SRC_FET**	Power-on	
V5V_P1	USB Type C PD Cont. P1 rail	5.0	Load Switch	**VDD_5V0**	**VDD_5V0**	
V5V_P2	USB Type C PD Cont. P1 rail	5.0	Load Switch	**VDD_5V0**	**VDD_5V0**	
VDD_SRC	Main supply from USB type C	9-20	FETs	**VBUS[2:1]**	**PD Controller**	
VCC_USBPD	USB C PD controller rail	9-20	DC-DC	**VCC_SRC**	**PD Controller**	
VDD_3V3	Main system 3.3V rail	3.3	DC-DC	**VCC_SRC**	**CARRIER_POWER_ON**	
VDD_1V8	Main system 1.8V rail	1.8	DC-DC	**VCC_SRC**	**CARRIER_POWER_ON**	
VDD_12V	Main system 12V rail	12	DC-DC	**VCC_SRC**	**VDD_5V0**	
AVDD_CAM_2V8	High voltage rail for cameras	2.8	LDO	**VDD_3V3**	**GPIO36**	
EPB_1V0	Ethernet PHY DVDD rail	1.0	LDO	**VDD_3V3**	**VDD_3V3**	
VDD_1V_SATA_PHY	ESATA PHY VDD rail	1.0	LDO	**VDD_1V8**	**VDD_1V8**	
VDD_5V0_HDMI_CON	5V rail for HDMI connector	5.0	Load Switch	**VDD_5V**	**GPIO20**	
VDD_1V8_SD	UFS 1.8V rail	1.8V	Load Switch	**VDD_1V8**	**GPIO21**	
VDD_3V3_SD	UFS/SDIO 3.3V rail	3.3V	Load Switch	**VDD_3V3**	**GPIO21**	
Power Control						
VDDIN_PWR_BAD_N connects to Carrier Board main power input & discharge circuit. Inactive when main supply is stable						
CARRIER_POWER_ON used as enable for Carrier Board main 5V supply & discharge circuit						
MODULE_POWER_ON: Used as enable by module to power on.						
SYS_RESET_IN_N to/from carrier board connects to devices requiring full system reset, and to system reset sources (reset button, etc.)						
PERIPHERAL_RESET_N to the module from Carrier Board when a force reset is required (as for Boundary Scan test mode)						
POWER_BTN_N is used to put system into sleep mode if active or wake system if in sleep mode.						
OVERTEMP_N (FORCE_SHUTDOWN_N) connects to power subsystem to cause system to power off if asserted by module.						
STANDBY_REQ_N from carrier board to module to request that module to enter SC7 low power mode.						
STANDBY_ACK_N from module to carrier board to indicate module will enter SC7 low power mode.						
Power Discharge						
DISCHARGE signal activated when main power source removed						
VDD_3V3 Discharge implemented: FET enabled by **DISCHARGE** w/Source **GND**'d & 2x10Ω to **VDD_3V3**						
VDD_1V8 Discharge implemented: FET enabled by **DISCHARGE** w/Source **GND**'d & 2x10Ω to **VDD_1V8**						
VDD_12V Discharge implemented: FET enabled by **DISCHARGE** w/Source **GND**'d & 2x470Ω to **VDD_12V**						
VDD_5V Discharge implemented: FET enabled by **VIN_PWR_ON** going inactive w/Source **GND**'d & 2x10Ω to **VDD_5V**						
VBUS1 & VBUS2 Discharge implemented: FETs enabled by **VBUS_DISCHARGE_P[2:1]** from USB PD Controller w/Source **GND**'d & 4x300Ω to **VBUS[2:1]** (separate circuits for each)						
Wake Event Pins						
If wake pin is required, use appropriate pin from Jetson Xavier Signal Wake Events table in the Power chapter.						
USB/PEX/UFS Connections						
USB 2.0						
USB0 available to be used as device for USB recovery at a minimum						
USB[3:0]_N/P connected to D-/D+ pins on USB 2.0 connector/device.						
Any EMI/ESD devices used are suitable for USB High-speed						
USB 3.1						
UPHY_RX1/RX6/RX11_N/P connected to RX+/- pins on USB 3.1 connector, Device, Hub, etc. (through 0.1uF series capacitors if USB device is on the main PCB).						
UPHY_TX1/TX6/TX11_N/P connected to TX+/- pins on USB 3.1 connector, Device, Hub, etc. through 0.1uF series capacitors						
See USB 3.1 section for Common Mode Choke requirements if this is required. TDK ACM2012D-900-2P device is recommended						
See USB 3.1 section for ESD requirements. SEMTECH ESD Rclamp0524p device is recommended						
PCIe						

PCIe Interface #C0 (x4 used for M.2 Key M on Carrier Board)	
UPHY2 used for single-lane device/connector (lane 0 of M.2 Key M connector on reference Carrier Board)	
UPHY[3:2] used for 2-lane device/connector	
UPHY[5:2] used for 4-lane device/connector	
TXx_P/N connected to corresponding pins on connector, or RX+/– on device on the carrier board (See Signal Terminations)	
RXx_P/N connected to corresponding pins on connector, or TX+/– on device on the carrier board	
AC caps are provided for device TX pins (those connected to the module RX_P/N) if device is on the carrier board (See Signal Terminations)	
Reference clock used for PCIe Interface #C0 (Up to x4 lane PCIe interface) is **PEX_CLK0_P/N**	
Clock Request & Reset for PCIe Interface #C0 are **PEX_L0_CLKREQ_N & PEX_L0_RST_N**	
PCIe Interface #C1 (x1 used for eSATA bridge on Carrier Board)	
UPHY0 used for single-lane device/connector	
TX0_P/N connected to corresponding pins on connector, or RX+/– on device on the carrier board (See Signal Terminations)	
RX0_P/N connected to corresponding pins on connector, or TX+/– on device on the carrier board	
AC caps are provided for device TX pins (those connected to the module RX_P/N) if device is on the carrier board (See Signal Terminations)	
Reference clock used for PCIe Interface #C1 (Up to x4 lane PCIe interface) is **PEX_CLK1_P/N**	
Clock Request & Reset for PCIe Interface #C1 are **PEX_L1_CLKREQ_N & PEX_L1_RST_N**	
PCIe Interface #C3 (x1 used for M.2 Key E on Carrier Board)	
UPHY7 used for single-lane device/connector	
TX7_P/N connected to corresponding pins on connector, or RX+/– on device on the carrier board (See Signal Terminations)	
RX7_P/N connected to corresponding pins on connector, or TX+/– on device on the carrier board	
AC caps are provided for device TX pins (those connected to the module RX_P/N) if device is on the carrier board (See Signal Terminations)	
Reference clock used for PCIe Interface #C3 (Up to x4 lane PCIe interface) is **PEX_CLK3_P/N**	
Clock Request & Reset for PCIe Interface #C3 are **PEX_L3_CLKREQ_N & PEX_L3_RST_N**	
PCIe Interface #C4 (x2 – Not used on Carrier Board)	
UPHY8 used for single-lane device/connector	
UPHY[9:8] used for 2-lane device/connector	
AC caps are provided for device TX pins (those connected to the module RX_P/N) if device is on the carrier board (See Signal Terminations)	
Reference clock used for PCIe Interface #C4 (Up to x4 lane PCIe interface) is **PEX_CLK4_P/N**	
Clock Request & Reset for PCIe Interface #C4 are **PEX_L4_CLKREQ_N & PEX_L4_RST_N**	
PCIe Interface #C5 (x8 – Routed to lower 8 lanes of PCIe x16 connector)	
NVHS[0] used for single-lane device/connector (lane 0 of PCIe x16 connector on reference Carrier Board)	
UPHY[1:0] used for 2-lane device/connector	
UPHY[3:0] used for 4-lane device/connector	
UPHY[7:0] used for 8-lane device/connector	
NVHSx_TXx_P/N connected to corresponding pins on connector, or RX+/– on device on the carrier board (See Signal Terminations)	
NVHS_SLVS_RXx_P/N connected to corresponding pins on connector, or TX+/– on device on the carrier board	
AC caps are provided for device TX pins (those connected to the module RX_P/N) if device is on the carrier board (See Signal Terminations)	
Reference clock used for PCIe Interface #C5 (Up to x4 lane PCIe interface) is **PEX_CLK5_P/N**	
Clock Request & Reset for PCIe Interface #C5 are **PEX_L5_CLKREQ_N & PEX_L5_RST_N**	
Common	
PEX_WAKE# connected to WAKE pins on devices/connectors (See Signal Terminations)	
UFS	
UPHY10_TX_P/N connected to DIN0_T/C pins on UFS device (single lane UFS)	
UPHY10_RX_P/N connected to DOUT0_T/C pins on UFS device (single lane UFS)	
UFS0_REF_CLK connected to REF_CLK pin of UFS device	
UFS0_RST_N connected to RESET pin of UFS device	
Ethernet	
RGMII_TXC connected to TXCLK pin on GbE Transceiver	
RGMII_TD[3:0] connected to TXD[3:0] pins on GbE Transceiver	
RGMII_TX_CTL connected to TXEN pin on GbE Transceiver	
RGMII_RXC connected to RXCLK pin on GbE Transceiver	
RGMII_RD[3:0] connected to RXD[3:0] pins on GbE Transceiver.	
RGMII_RX_CTL connected to RXDV pin on GbE Transceiver	
RGMII_MDC connect to MDC pin on GbE Transceiver	
RGMII_MDIO connected to MDIO pin on GbE Transceiver with 2.2kΩ pull-up to VDD_1V8	
ENET_RST_N connected to Reset input on Ethernet PHY	
ENET_INT connected to Interrupt output on Ethernet PHY with 10kΩ pull-up to VDD_1V8	

GBE_MDI[3:0]+/ – connected to equivalent pins on magnetics device (See Signal Terminations)	
SDMMC Connections	
SD Card	
SDCARD_CLK connected to CLK pin of socket/device	
SDCARD_CMD connected to CMD pin of socket/device. (See Signal Terminations)	
SDCARD_D[3:0] connected to DATA[3:0] pins of socket/device. (See Signal Terminations)	
GPIO02 (SDCARD_CD_N) connected to the SD Card Detect pin on socket	
GPIO21 (SDCARD_VDD_EN) connected to SD Card VDD supply/load switch enable pin	
Adequate bypass caps provided on SD Card VDD rail	
Any EMI/ESD devices used are suitable for highest frequencies supported (low capacitive load: <1pf recommended).	
Display Connections	
eDP / DP	
HDMI_DPx_TX[3:0]_P/N connected to D[3:0]+/– pins on eDP/DP connector (See DP/HDMI Pin Mapping table & Signal Terminations)	
DPx_AUX_CH_P/N connected to Aux Lane of panel/connector (See Signal Terminations)	
DPx_HPD connected to HPD pin of panel/connector	
Any EMI/ESD devices used are suitable for highest frequencies supported (low capacitive load: <1pf recommended)	
HDMI	
HDMI_DPx_TX3_P/N connected to C–/C+ & pins on HDMI Connector (See Signal Terminations)	
HDMI_DPx_TX[2:0]_P/N connected to D[0:2]+/– pins (See DP/HDMI Pin Mapping table) (See Signal Terminations)	
DPx_HPD connected to HPD pin on HDMI Connector (See Signal Terminations)	
HDMI_CEC connected to CEC on HDMI Connector through gating circuitry (see carrier board reference schematics).	
DPx_AUX_CH_P connected to SCL & **DPx_AUX_CH_N** to SDA on HDMI Connector (See Signal Terminations)	
HDMI 5V Supply connected to +5V on HDMI Connector.	
See HDMI section for Common Mode Choke requirements if this is required (not recommended unless EMI issues seen)	
See HDMI section for ESD requirements. ON-Semiconductor ESD8040 device is recommended	
Video Input	
Camera (CSI – D-PHY)	
CSI[7:0]_CLK_P/N connected to clock pins of camera. See CSI D-PHY Configurations table for details	
CSI[7:0]_D[1:0]_P/N connected to data pins of camera. See CSI D-PHY Configurations table for details	
Camera (CSI – C-PHY)	
CSI0_D0P (A), D0N (B), CLKP (C) connected to first trio of C-PHY camera & **CSI0_D1P (A), D1N (B), CLKN (C)** of second trio of 2-lane C-PHY camera or lower 2-lanes of 4-lane C-PHY camera	
CSI1_D0P (A), D0N (B), CLKP (C) connected to first trio of C-PHY camera & **CSI1_D1P (A), D1N (B), CLKN (C)** of second trio of 2-lane C-PHY camera or upper 2-lanes of 4-lane C-PHY camera	
CSI2_D0P (A), D0N (B), CLKP (C) connected to first trio of C-PHY camera & **CSI2_D1P (A), D1N (B), CLKN (C)** of second trio of 2-lane C-PHY camera or lower 2-lanes of 4-lane C-PHY camera	
CSI3_D0P (A), D0N (B), CLKP (C) connected to first trio of C-PHY camera & **CSI3_D1P (A), D1N (B), CLKN (C)** of second trio of 2-lane C-PHY camera or upper 2-lanes of 4-lane C-PHY camera	
CSI4_D0P (A), D0N (B), CLKP (C) connected to first trio of C-PHY camera & **CSI4_D1P (A), D1N (B), CLKN (C)** of second trio of 2-lane C-PHY camera or lower 2-lanes of 4-lane C-PHY camera	
CSI5_D0P (A), D0N (B), CLKP (C) connected to first trio of C-PHY camera & **CSI5_D1P (A), D1N (B), CLKN (C)** of second trio of 2-lane C-PHY camera or upper 2-lanes of 4-lane C-PHY camera	
CSI6_D0P (A), D0N (B), CLKP (C) connected to first trio of C-PHY camera & **CSI6_D1P (A), D1N (B), CLKN (C)** of second trio of 2-lane C-PHY camera or lower 2-lanes of 4-lane C-PHY camera	
CSI7_D0P (A), D0N (B), CLKP (C) connected to first trio of C-PHY camera & **CSI7_D1P (A), D1N (B), CLKN (C)** of second trio of 2-lane C-PHY camera or upper 2-lanes of 4-lane C-PHY camera	
Camera (Common)	
Any EMI/ESD devices used are suitable for highest frequencies supported (low capacitive load: <1pf recommended)	
Control	
I2C4_CLK/DAT connected to I2C SCL & SDA pins of imager (See Signal Terminations).	
MCLK[4:2]_MCLK connected to Camera reference clock inputs for cameras [2:0].	
GPIO15 (CAM1 PWDN)/ **UART4_CTS** (CAM0 PWDN) connected to powerdown pins on camera(s).	
GPIO16 (CAM1 RST)/ **UART4_TX** (CAM0 RST) connected to reset pin on any cameras with this function.	
GPIO26 (VDD_SYS Enable) connected to appropriate camera supply enable	
GPIO36 (AVDD Enable) connected to appropriate camera supply enable	
Audio	
Codec/I2S/DMIC/DSPK	
I2S1 used for Audio Codec if present in design	
I2S2 used for secondary BT if present in design	

I2S3 used for M.2 Key E (Primary BT) if present in design	
I2Sx_CLK Connected to I2S/PCM CLK pin of audio device.	
I2Sx_LRCK Connected to Left/Right Clock pin of audio device.	
I2Sx_SDATA_OUT Connected to Data Input pin of audio device.	
I2Sx_SDATA_IN Connected to Data Output pin of audio device.	
AUDIO_MCLK Connected to clock pin of Audio Codec.	
GPIO11 Connected to interrupt pin of Audio Codec.	
GPIO09 (DMIC_CLK) & **GPIO08 (DMIC_DAT)** connected to CLK/DAT pins of digital mic	
GPIO16 (DSPK_CLK) & **GPIO15 (DSPK_DAT)** connected to CLK/DAT pins of digital speaker driver	
I2C/SPI/UART	
I2C	
I2C devices on same I2C interface do not have address conflicts (comparisons are done 7-bit to 7-bit format or 8-bit to 8-bit format)	
I2C1, I2C2, I2C3, I2C4 & I2C5 (See Signal Terminations). Additional external pull-ups are not added unless stronger pull-up than on module required. Devices on bus are 1.8V or level shifter is used.	
Pull-up resistors are provided on the non-module side of any level shifters.	
Pull-up resistor values based on frequency/load (check I2C Spec)	
I2C1_CLK/DAT, I2C2_CLK/DAT, I2C3_CLK/DAT, I2C4_CLK/DAT & I2C5_CLK/DAT connect to SCL/SDA pins of devices	
SPI	
SPI[3:1]_CLK connected to Peripheral CLK pin(s)	
SPI[3:1]_MOSI connected to Slave Peripheral MOSI pin(s)	
SPI[3:1]_MISO connected to Slave Peripheral MISO pin(s)	
SPI[3,1]_CS[1:0]_N / **SPI2_CS0_N** connected one CS# pin per SPI IF to each Slave Peripheral CS pin on the interface	
CAN	
CAN[1:0]_DOUT connected to input data (DIN/RX) pins of respective CAN device	
CAN[1:0]_DIN connected to output data (DOUT/TX) pin of respective CAN device	
GPIO08 (CAN1_STBY) connected to Standby pin of respective CAN device	
GPIO09 (**CAN1_EN**) & **GPIO06** (**CAN0_EN**) connected to Error pin of respective CAN device	
GPIO10 (**CAN_WAKE**) connected to Wake pin of CAN devices	
UART	
UARTx_TX connects to Peripheral RX pin of device	
UARTx_RX connects to Peripheral TX pin of device	
UARTx_CTS connects to Peripheral RTS# pin of device	
UARTx_RTS connects to Peripheral CTS# pin of device	
Miscellaneous	
JTAG	
JTAG_TMS Connect to **TMS** pin of connector	
JTAG_TCK Connect to **TCK** pin of connector (See Signal Terminations).	
JTAG_TDO Connect to **TDO** pin of connector	
JTAG_TDI Connect to **TDI** pin of connector	
JTAG_RTCLK Connect to **RTCK** pin of connector	
JTAG_TRST_N: Connect to **TRST** pin of connector	
NVJTAG_SEL: For normal operation, **NVJTAG_SEL** is pulled down. (See Signal Terminations).	
NVJTAG_SEL: For Boundary Scan test mode, **NVJTAG_SEL** is connected to **VDD_1V8**. (See Signal Terminations).	
NVDBG_SEL: For normal operation, **NVJTAG_SEL** is pulled down. (See Signal Terminations).	
Strapping	
FORCE_RECOVERY_N: To enter Forced Recovery mode, pin is connected to **GND** when system is powered on.	
All other module pins associated with strapping on Xavier: Ensure any devices connected to module pins associated with Xavier straps do not affect the level of the straps at power-on. Module pins affected are: **STANDBY_REQ_N, GPIO01, UART2_TX, UART2_RTS, UART5_TX, UART5_RTS, UART1_TX, UART4_TX, UART4_RTS, UART1_RTS**.	
Pin Selection	
Pinmux completed including GPIO usage (direction, initial state, Ext. PU/PD resistors, Deep Sleep state).	
SFIO usage matches reference platform where possible.	
Each SFIO function assigned to only one pin, even if function selected in Pinmux registers is not used or pin used as GPIO	
GPIO usage matches reference platform where possible.	
Unused SFIO (Special Function I/O) Interface Pins	
Ball Name | **Termination**	
USB 2.0	
USB[3:1]_P/N | Leave NC any unused pins	
USB 3.1 / PCIe / UFS	

UPHY_[11:0]_TX_P/N **NVHS0_TX[7:0]_N/P**	Leave NC any unused TX lines	
UPHY[11:0]_RX_P/N **NVHS0_SLVS_RX[7:0]_N/P**	Leave NC or connect to **GND** through 10kΩ resistor any unused RX lines	
PEX_CLK[5:3,1,0]_N/P	Leave NC if not used	
CSI		
CSI[7:0]_CK+/–	Leave NC any unused CSI Clock lanes	
CSI[7:0]_D[1:0] +/–	Leave NC any unused CSI Data lanes	
RGMII (Ethernet)		
RGMII_TDC, RGMII_TD[1:0], RGMII_TX_CTL	Leave NC if RGMII interface not used	
RGMII_RDC, RGMII_RD[1:0], RGMII_RX_CTL	Leave NC if RGMII interface not used	
RGMII_SMA_MDIO, RBMII_SMA_MDC	Leave NC if RGMII interface not used	
eDP/DP/HDMI		
HDMI_DPx_TX[3:0]_N/P	Leave NC any unused lanes	
DPx_AUX_CH_N/P	Leave NC if not used	
DPx_HPD	Leave NC if not used	

18.0 APPENDIX A: GENERAL LAYOUT GUIDELINES

18.1 Overview

Trace and via characteristics play an important role in signal integrity and power distribution on Jetson Xavier. Vias can have a strong impact on power distribution and signal noise, so careful planning must take place to ensure designs meet NVIDIA's via requirements. Trace length and impedance determine signal propagation time and reflections, both of which can greatly improve or reduce the performance of Jetson Xavier. Trace and via requirements for each signal type can be found in the corresponding chapter; this appendix provides general guidelines for via and trace placement.

18.2 Via Guidelines

The number of vias in the path of a given signal, power supply line, or ground line can greatly affect the performance of the trace. Via placement can make differences in current carrying capability, signal integrity (due to reflections and attenuation), and noise generation, all of which can impact the overall performance of the trace. The following guidelines provide basic advice for proper use of vias.

18.2.1 Via Count and Trace Width

As a general rule, each ampere of current requires at least two micro-vias.

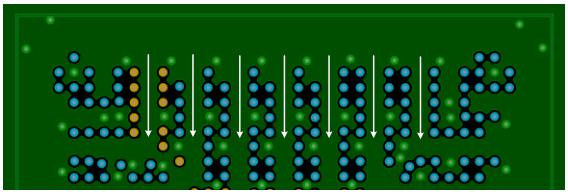
18.2.2 Via Placement

If vias are not placed carefully, they can severely degrade the robustness of a board's power plane. In standard deigns that don't use blind or buried vias, construction of a via entails drilling a hole that cuts into the power and ground planes. Thus, incorrect via placement affects the amount of copper available to carry current to the power balls of the IC.

18.2.3 Via Placement and Power/Ground Corridors

Vias should be placed so that sufficiently wide power corridors are created for good power distribution, as show in Figure 43.

Figure 43. Via Placement for Good Power Distribution



Care should also be taken to avoid use of "thermal spokes" (also referred to as "thermal relief") on power and ground vias. Thermal spokes are not necessary for surface-mount components, and the narrow spoke widths contribute to increased inductance. The metal on the inner layers between vias may not be flooded with copper if sufficient spacing is not provided. The diminished spacing creates a blockage and forces the current to find another path due to lack of copper, as shown in Figure 44 and Figure 45. This leads to power delivery issues and impedance discontinuities when traces are routed over these plane voids.

Figure 44. Good Current Flow Resulting from Correct Via Placement

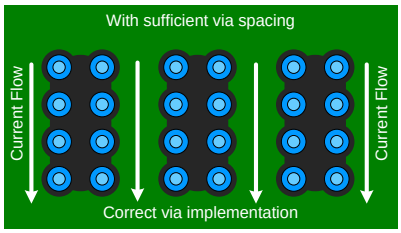
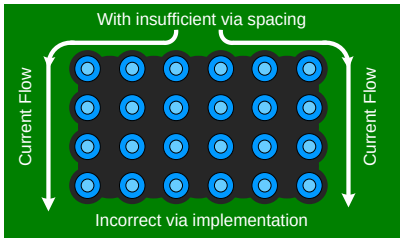


Figure 45. Poor Current Flow Resulting from Incorrect via Placement



In general, a dense via population should be avoided and good PCB design principles and analysis should be applied.

18.3 Connecting Vias

To be effective, vias must be connected properly to the signal and power planes. Poor via connections make the capacitor and power planes less effective, leading to increased cost due to the need for additional capacitors to achieve equivalent performance. This not only impacts the BOM (Bill of Material) cost of the design, but it can greatly impact quality and reliability of the design.

18.4 Trace Guidelines

Trace length and impedance play a critical role in signal integrity between the driver and the receiver on Jetson Xavier. Signal trace requirements are determined by the driver characteristics, source characteristics, and signal frequency of the propagating signal.

18.4.1 Layer Stack-Up

The number of layers required is determined by the number of memory signal layers needed to achieve the desired performance, and the number of power rails required to achieve the optimum power delivery/noise floor. For example, high-performance boards require four memory signal routing layers, with at least two GND planes for reference. This comes to six layers; add another two for power, which gives eight layers minimum. Reduction from eight to six layers starts the trade-off of cost versus performance.

Power and GND planes usually serve two purposes in PCB design: power distribution and providing a signal reference for high-speed signals.

Either the power or the ground planes can be used for high-speed signal reference; this is particularly common for low-cost designs with a low layer count. When both power and GND are used for signal reference, make sure you minimize the reference plane transition for all high-speed signals. Decoupling caps or transition vias should be added close to the reference plane transitions.

18.4.2 Trace Length

The maximum trace length for a given signal is determined by the maximum allowable propagation delay and impedance for the signal. Higher frequency signals must be treated as transmission lines (see “Appendix C – Transmission Line Primer”) to determine proper trace characteristics for a signal.

All signals on the graphics card maintain different trace guidelines; please refer to the corresponding signal chapter in the Design Guide to determine the guidelines for the signal.

19.0 APPENDIX B: STACK-UPS

19.1 Reference Design Stack-Ups

19.1.1 Importance of Stack-Up Definition

Stack-ups define the number and order of Board layers. Stack-up definition is critical to the following design:

- Circuit routability
- Signal quality
- Cost

19.1.2 Impact of Stack-Up Definition on Design

Stack-Up Impact on Circuit Routability

If there are insufficient layers to maintain proper signal spacing, prevent discontinuities in reference planes, obstruct flow of sufficient current, or avoid extra vias, circuit routing can become unnecessarily complex. Layer count must be minimally appropriate for the circuit.

Stack-Up Impact on Signal Quality

Both layer count and layer order impact signal integrity. Proper inter-signal spacing must be achievable. Via count for critical signals must be minimized. Current commensurate with the performance of the board must be carried. Critical signals must be adjacent to major and minor reference planes and adhere to proximity constraints with respect to those planes. The recommended NVIDIA stack-ups achieve these requirements for the signal speeds supported by the board.

Stack-Up Impact on Cost

While defining extra layers can facilitate excellent signal integrity, current handling capability and routability, extra layers can impede the goal of hitting cost targets. The art of stack-up definition is achieving all technical and reliability circuit requirements in a cost efficient manner. The recommended NVIDIA stack-ups achieve these requirements with efficient use of board layers.

20.0 APPENDIX C: TRANSMISSION LINE PRIMER

20.1 Background

NVIDIA maintains strict guidelines for high-frequency PCB transmission lines to ensure optimal signal integrity for data transmission. This section provides a brief primer into basic board-level transmission line theory.

Characteristics

The most important PCB transmission line characteristics are listed in the following bullets:

- Trace width/height, PCB height and dielectric constant, and layer stack-up affect the characteristic trace impedance of a transmission line.

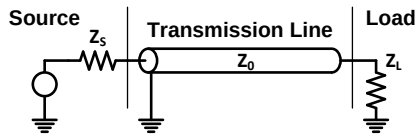
$$Z_0 \cong \left(\frac{L}{C}\right)^{1/2}$$

- Signal rise time is proportional to the transmission line impedance and load capacitance.

$$RiseTime \cong \left(\frac{Z_0 * R_{Term}}{Z_0 + R_{Term}}\right) * C_{Load}$$

- Real transmission lines (Figure 46) have non-zero resistances that lead to attenuation and distortion, creating signal integrity issues.

Figure 46. Typical Transmission Line Circuit



Transmission lines are used to "transmit" the source signal to the load or destination with as little signal degradation or reflection as possible. For this reason it is important to design the high-speed signal transmission line to fall within characteristic guidelines based on the signal speed and type.

20.2 Physical Transmission Line Types

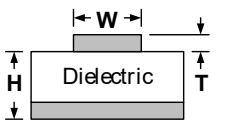
The two primary transmission line types often used for Jetson Xavier board designs are:

- Microstrip transmission line (Figure 47)
- Stripline transmission line (Figure 48)

The following sections describe each type of transmission.

Microstrip Transmission Line

Figure 47. Microstrip Transmission Line

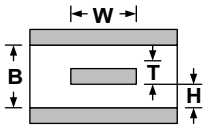


$$Z_0 = \left(\frac{87}{\sqrt{Er + 1.414}}\right) \ln\left(\frac{5.98H}{0.8W + T}\right)$$

- Z_0: Impedance
- W: Trace width (inches)
- T: Trace thickness (inches)
- Er: Dielectric constant of substrate
- H: Distance between signal and reference plane

Stripline Transmission Line

Figure 48. Stripline Transmission Line



$$Z_0 = \left(\frac{60}{\sqrt{Er}}\right) \ln\left(\frac{4H}{0.67\pi W\left(0.8 + \frac{T}{W}\right)}\right)$$

- Z_0: Impedance
- W: Trace width (inches)
- T: Trace thickness (inches)
- Er: Dielectric constant of substrate
- H: Distance between signal and reference plane

20.3 Driver Characteristics

Driver characteristics are important to the integrity and maximum speed of the signal. The following points identify key driver equations and concepts used to improve signal integrity and transmission speed.

- The driver (source) has resistive output impedance Z_S, which causes only a fraction of the signal voltage to propagate down the transmission line to the receiver (load).
  - • Transfer function at source:

$$T1 = \frac{Z_0}{Z_S + Z_0}$$

  - • Driver strength is inversely proportional to the source impedance, Z_S.
- Z_S also acts as the source termination, which helps dampen reflection.
  - Source reflection coefficient:

$$R1 = \frac{(Z_S - Z_0)}{(Z_S + Z_0)}$$

20.4 Receiver Characteristics

Receiver characteristics are important to the integrity and detectability of the signal. The following points identify key receiver concepts and equations for optimum signal integrity at the final destination.

- The receiver acts as a capacitive load and often has a high load impedance, Z_L.
- Unterminated transmission lines cause overshoot and reflection at the receiver, which can cause data corruption.
  - Output transfer function at load:

$$T2 = \frac{2 * Z_L}{Z_L + Z_0}$$

  - Load reflection coefficient:

$$R2 = \frac{(Z_L - Z_0)}{(Z_L + Z_0)}$$

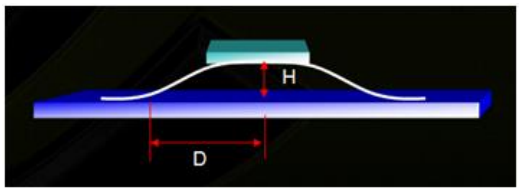
- Load impedance can be lowered with a termination resistor (R_{Term}) placed at the end of the transmission line.
  - Reflection is minimized when Z_L matches Z_0

20.5 Transmission Lines & Reference Planes

Defining an appropriate reference plane is vital to transmission line performance due to crosstalk and EMI issues. The following points explore appropriate reference plane identification and characteristics for optimal signal integrity:

- Transmission line return current (Figure 49)
  - High-speed return current follows the path of least inductance.
  - The lowest inductance path for a transmission line is right underneath the transmission line; i(D) is proportional to:

Figure 49. Transmission Line Height



- Transmission line return current:
  - High-speed return current follows the path of least inductance.
  - The lowest inductance path for a transmission line is the portion of the line closest to the dielectric surface; i(D) is proportional to

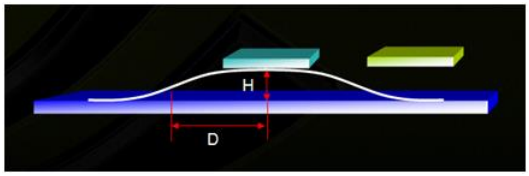
$$\frac{1}{\left(1+\left(\frac{D}{H}\right)^2\right)}$$

- Crosstalk on solid reference plane (Figure 50):
  - Crosstalk is caused by the mutual inductance of two parallel traces.
  - Crosstalk at the second trace is proportional to

$$\frac{1}{\left(1+\left(\frac{D}{H}\right)^2\right)}$$

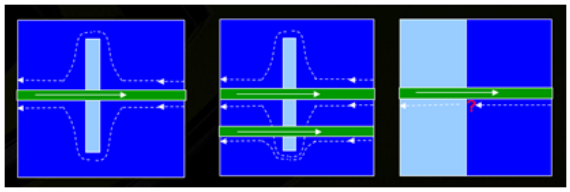
  - The signals need to be properly spaced to minimize crosstalk.

Figure 50. Crosstalk on Reference Plane



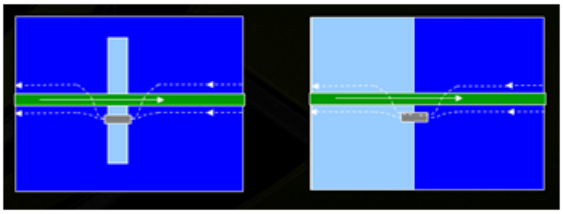
- Reference plane selection
  - Solid ground is preferred as reference plane.
  - Solid power can be used as reference plane with decoupling capacitors near driver and receiver.
  - Reference plane cuts and layer changes need to be avoided.
- Power plane cut example (Figure 51)
  - Power plane cuts will cause EMI issues.
  - Power plane cuts also induce crosstalk to adjacent signals.

Figure 51. Example of Power Plane Cuts



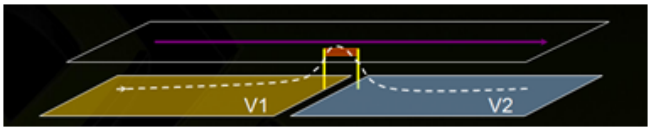
- When cut is unavoidable:
  - • Place decoupling capacitors near transition.
  - • Place transition near source or receiver when decoupling capacitors are abundant (Figure 52).

Figure 52. Another Example of Power Plane Cuts



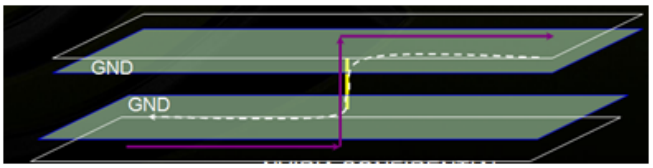
- When signal changes plane:
  - Try not to change the reference plane, if possible.
  - When a reference plane switches to different power rail, a stitching capacitor is required (Figure 53).

Figure 53. Switching Reference Planes



  - When the same ground/power reference plane changes to a different layer, a stitching via is required (Figure 54).

Figure 54. Reference Plane Switch Using VIA



21.0 APPENDIX D: DESIGN GUIDELINE GLOSSARY

The Design Guidelines include various terms. The descriptions in the table below are intended to show what these terms mean and how they should be applied to a design.

Table 89 Layout Guideline Tutorial

Trace Delays
Max Breakout Delay - Routing on Component layer: Maximum Trace Delay from module connector pin to point beyond pin array where normal trace spacing/impedance can be met. Routing passes to layer other than Component layer: Beyond this, normal trace spacing/impedance must be met. **Max Total Trace Delay** - Trace from module connector pin to Device pin. This must include routing on the main PCB & any other Flex or secondary PCB. Delay is from Module connector to the final connector/device.
Intra/Inter Pair Skews
Intra Pair Skew (within pair) - Difference in delay between two traces in differential pair: Shorter routes may require indirect path to equalize delays **Inter Pair Skew (pair to pair)** - Difference between two (or possibly more) differential pairs
Impedance/Spacing
Microstrip vs Stripline - Microstrip: Traces next to single ref. plane. Stripline: Traces between two ref planes **Trace Impedance** - Impedance of trace determined by width & height of trace, distance from ref. plane & dielectric constant of PCB material. For differential traces, space between pair of traces is also a factor **Board trace spacing / Spacing to other nets** - Minimum distance between two traces. Usually specified in terms of dielectric height which is distance from trace to reference layers. **Pair to pair spacing** - Spacing between differential traces **Breakout spacing** - Possible exception to board trace spacing where different spacing rules are allowed under module connector pin in order to escape from the pin array. Outside device boundary, normal spacing rules apply
Reference Return

Ground Reference Return Via & Via proximity (signal to reference)
- Signals changing layers & reference GND planes need similar return current path
- Accomplished by adding via, tying both GND layers together
Via proximity (sig to ref) is distance between signal & reference return vias
- GND reference via for Differential Pair
- Where a differential pair changes GND reference layers, return via should be placed close to & between signal vias (example to right)
Signal to return via ratio
- Number of Ground Return vias per Signal vias. For critical IFs, ratio is usually 1:1. For less critical IFs, several trace vias can share fewer return vias (i.e. 3:2 – 3 trace vias & 2 return vias).
Slots in Ground Reference Layer
- When traces cross slots in adjacent power or ground plane
- Return current has longer path around slot
- Longer slots result in larger loop areas
- Avoid slots in GND planes or do not route across them
Routing over Split Power Layer Reference Layers
- When traces cross different power areas on power plane
  - Return current must find longer path - usually a distant bypass cap
  - If possible, route traces w/solid plane (GND or PWR) or keep routes across single area
- If traces must cross two or more power areas, use stitching capacitors
  - Placing one cap across two PWR areas near where traces cross area boundaries provides high-frequency path for return current
  - Cap value typically 0.1uF & should ideally be within 0.1" of crossing

22.0 APPENDIX E: JETSON XAVIER PIN DESCRIPTIONS

Table 90. Jetson Xavier Connector (8x50) Pin Descriptions

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
A3	PRSNT0	–		Tied to GND	–	–
A4	SDCARD_D2	SDMMC1_DAT2	SD Card (or SDIO) Data 2	Micro SD / UFS Card Socket	Bidir	CMOS – 3.3V/1.8V
A5	SDCARD_CMD	SDMMC1_CMD	SD Card (or SDIO) Command	Micro SD / UFS Card Socket	Bidir	CMOS – 3.3V/1.8V
A6	UFS0_REF_CLK	UFS0_REF_CLK	UFS Reference Clock	Micro SD / UFS Card Socket	Output	CMOS – 1.2V
A7	GPIO29	SOC_GPIO31	GPIO	M.2 Key M PEWAKE#	Bidir	CMOS – 1.8V
A8	PEX_WAKE_N	PEX_WAKE_N	PCIe Wake	PCIe x16 Connector, M.2 Key E & M Conn.	Input	CMOS – 1.8V
A9	GND	–	GND	GND	–	GND
A10	USB2_P	USB2_DP	USB 2.0, Port 2 Data+	M.2 Key E Connector	Bidir	USB2 Diff pair
A11	USB2_N	USB2_DN	USB 2.0, Port 2 Data–	M.2 Key E Connector	Bidir	USB2 Diff pair
A12	GND	–	GND	GND	–	GND
A13	GND	–	GND	GND	–	GND
A14	UPHY_RX8_N	PEX_RX8_N	UPHY Receive 8-	–	Input	PCIe/USB3/UFS Diff Pair, AC-Coupled on carrier board
A15	UPHY_RX8_P	PEX_RX8_P	UPHY Receive 8+	–	Input	
A16	GND	–	GND	GND	–	GND
A17	GND	–	GND	GND	–	GND
A18	UPHY_RX4_P	PEX_RX4_P	UPHY Receive 4+	M.2 Key M Connector	Input	PCIe Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
A19	UPHY_RX4_N	PEX_RX4_N	UPHY Receive 4-	M.2 Key M Connector	Input	
A20	GND	–	GND	GND	–	GND
A21	GND	–	GND	GND	–	GND
A22	UPHY_RX0_P	PEX_RX0_P	UPHY Receive 0+	eSATA Bridge	Input	PCIe Diff Pair, - TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
A23	UPHY_RX0_N	PEX_RX0_N	UPHY Receive 0-	eSATA Bridge	Input	
A24	GND	–	GND	GND	–	GND
A25	GND	–	GND	GND	–	GND
A26	NVHS0_SLVS_RX3_P	NVHS0_RX3_P	NVHS/PCIe/SLVS 0 Receive 3+	PCIe x16 Connector	Input	PCIe/SLVS Diff Pair, AC-Coupled on carrier board if PCIe & direct connect to device.
A27	NVHS0_SLVS_RX3_N	NVHS0_RX3_N	NVHS/PCIe/SLVS 0 Receive 3-	PCIe x16 Connector	Input	
A28	GND	–	GND	GND	–	GND
A29	GND	–	GND	GND	–	GND
A30	NVHS0_SLVS_RX7_P	NVHS0_RX7_P	NVHS/PCIe/SLVS 0 Receive 7+	PCIe x16 Connector	Input	PCIe/SLVS Diff Pair, AC-Coupled on carrier board if PCIe & direct connect to device.
A31	NVHS0_SLVS_RX7_N	NVHS0_RX7_N	NVHS/PCIe/SLVS 0 Receive 7-	PCIe x16 Connector	Input	
A32	GND	–	GND	GND	–	GND
A33	GND	–	GND	GND	–	GND
A34	RSVD	–	–	–	–	–
A35	RSVD	–	–	–	–	–
A36	GND	–	GND	GND	–	GND
A37	GND	–	GND	GND	–	GND
A38	RSVD	–	–	–	–	–
A39	RSVD	–	–	–	–	–
A40	GND	–	GND	GND	–	GND
A41	CSI2_D0_P	CSI_C_D0_P	Camera, CSI 2 Data 0+	Camera Connector	Input	MIPI D-PHY/C-PHY
A42	CSI2_D0_N	CSI_C_D0_N	Camera, CSI 2 Data 0–	Camera Connector	Input	MIPI D-PHY/C-PHY
A43	GND	–	GND	GND	–	GND
A44	CSI7_D0_P	CSI_H_D0_P	Camera, CSI_7 Data 0+	Camera Connector	Input	MIPI D-PHY/C-PHY
A45	CSI7_D0_N	CSI_H_D0_N	Camera, CSI_7 Data 0–	Camera Connector	Input	MIPI D-PHY/C-PHY
A46	GND	–	GND	GND	–	GND
A47	HDMI_DP1_TX0_P	HDMI_DP1_TXDP0	DisplayPort 1 Lane 0+ or HDMI Lane 2+	USB Type C Conn. J8 (via Alt Mode Switch)	Output	Diff pair, AC-Coupled on carrier board
A48	HDMI_DP1_TX0_N	HDMI_DP1_TXDN0	DisplayPort 1 Lane 0– or HDMI Lane 2–	USB Type C Conn. J8 (via Alt Mode Switch)	Output	

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
A49	GND	–	GND	GND	–	GND
A50	HDMI_DP2_TX2_N	HDMI_DP2_TXDN2	DisplayPort 2 Lane 2– or HDMI Lane 0–	HDMI Connector	Output	Diff pair, AC-Coupled on carrier board
A51	HDMI_DP2_TX2_P	HDMI_DP2_TXDP2	DisplayPort 2 Lane 2+ or HDMI Lane 0+	HDMI Connector	Output	
A52	GND	–	GND	GND	–	GND
A53	I2C5_CLK	DP_AUX_CH3_P	General I2C 5 Clock	Expansion Connector	Bidir	Open-Drain – 1.8V
A54	GPIO17	SOC_GPIO21	GPIO	Expansion Connector (GMSI Interrupt 0)	Bidir	CMOS – 1.8V
A55	GPIO34	SOC_GPIO06	GPIO	M.2 Key M Alert	Bidir	CMOS – 1.8V
A56	SPI1_MISO	SPI1_MISO	SPI 1 Master In / Slave Out	Expansion Connector	Bidir	CMOS – 1.8V
A57	UART2_CTS	UART2_CTS	UART 2 Clear to Send	UART-USB (MicroB) Bridge	Bidir	CMOS – 1.8V
A58	GPIO20	DAP6_FS	GPIO	HDMI 5V Enable	Output	CMOS – 3.3V
A59	GPIO05	DAP6_DOUT	GPIO	12V Supply Enable	Output	CMOS – 3.3V
A60	JTAG_TCK	JTAG_TCK	JTAG Test Clock	JTAG Connector	Input	CMOS – 1.8V
A61	SYSTEM_OC_N	BATT_OC	Battery Over-current (& Thermal) warning	Not used	Input	CMOS – 1.8V
A62	GPIO10	CAN1_WAKE	GPIO	USB PD Controller Interrupt	Bidir	CMOS – 3.3V
A63	GND	–	GND	GND	–	GND
B3	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
B4	GND	–	GND	GND	–	GND
B5	RGMII_TXC	EQOS_TXC	Ethernet Transmit Clock	Ethernet PHY	Output	CMOS – 1.8V
B6	SDCARD_CLK	SDMMC1_CLK	SD Card (or SDIO) Clock	Micro SD / UFS Card Socket	Output	CMOS – 3.3V/1.8V
B7	GND	–	GND	GND	–	GND
B8	GPIO11	SOC_GPIO30	GPIO	Audio Codec Interrupt	Bidir	CMOS – 1.8V
B9	PEX_L1_RST_N	PEX_L1_RST_N	PCIe 1 Reset	–	Output	CMOS – 1.8V
B10	RSVD	–	–	–	–	–
B11	GND	–	GND	GND	–	GND
B12	UPHY_RX10_P	PEX_RX10_P	UPHY Receive 10+	Micro SD / UFS Card Socket	Input	UFS Diff Pair
B13	UPHY_RX10_N	PEX_RX10_N	UPHY Receive 10-	Micro SD / UFS Card Socket	Input	UFS Diff Pair
B14	GND	–	GND	GND	–	GND
B15	GND	–	GND	GND	–	GND
B16	UPHY_RX6_P	PEX_RX6_P	UPHY Receive 6+	USB Type C Alt Mode Switch (for J8)	Input	USB3 Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
B17	UPHY_RX6_N	PEX_RX6_N	UPHY Receive 6-	USB Type C Alt Mode Switch (for J8)	Input	
B18	GND	–	GND	GND	–	GND
B19	GND	–	GND	GND	–	GND
B20	UPHY_RX2_N	PEX_RX2_N	UPHY Receive 2-	M.2 Key M Connector	Input	PCIe Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
B21	UPHY_RX2_P	PEX_RX2_P	UPHY Receive 2+	M.2 Key M Connector	Input	
B22	GND	–	GND	GND	–	GND
B23	GND	–	GND	GND	–	GND
B24	NVHS0_SLVS_RX1_N	NVHS0_RX1_N	NVHS/PCIe/SLVS 0 Receive 1-	PCIe x16 Connector	Input	PCIe/SLVS Diff Pair, AC-Coupled on carrier board if PCIe & direct connect to device.
B25	NVHS0_SLVS_RX1_P	NVHS0_RX1_P	NVHS/PCIe/SLVS 0 Receive 1+	PCIe x16 Connector	Input	
B26	GND	–	GND	GND	–	GND
B27	GND	–	GND	GND	–	GND
B28	NVHS0_SLVS_RX5_N	NVHS0_RX5_N	NVHS/PCIe/SLVS 0 Receive 5-	PCIe x16 Connector	Input	PCIe/SLVS Diff Pair, AC-Coupled on carrier board if PCIe & direct connect to device.
B29	NVHS0_SLVS_RX5_P	NVHS0_RX5_P	NVHS/PCIe/SLVS 0 Receive 5+	PCIe x16 Connector	Input	
B30	GND	–	GND	GND	–	GND
B31	GND	–	GND	GND	–	GND
B32	RSVD	–	–	–	–	–
B33	RSVD	–	–	–	–	–
B34	GND	–	GND	GND	–	GND
B35	GND	–	GND	GND	–	GND
B36	RSVD	–	–	–	–	–
B37	RSVD	–	–	–	–	–
B38	GND	–	GND	GND	–	GND
B39	GND	–	GND	GND	–	GND

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
B40	MID4	–	Module ID #4	–	–	–
B41	GND	–	GND	GND	–	GND
B42	CSI2_CLK_N	CSI_C_CLK_N	Camera, CSI 2 Clock–	Camera Connector	Input	MIPI D-PHY/C-PHY
B43	CSI2_CLK_P	CSI_C_CLK_P	Camera, CSI 2 Clock+	Camera Connector	Input	MIPI D-PHY/C-PHY
B44	GND	–	GND	GND	–	GND
B45	CSI7_CLK_P	CSI_H_CLK_P	Camera, CSI_7 Clock+	Camera Connector	Input	MIPI D-PHY/C-PHY
B46	CSI7_CLK_N	CSI_H_CLK_N	Camera, CSI_7 Clock–	Camera Connector	Input	MIPI D-PHY/C-PHY
B47	GND	–	GND	GND	–	GND
B48	HDMI_DP1_TX1_N	HDMI_DP1_TXDN1	DisplayPort 1 Lane 1– or HDMI Lane 1–	USB Type C Conn. J8 (via Alt Mode Switch)	Output	Diff pair, AC-Coupled on carrier board
B49	HDMI_DP1_TX1_P	HDMI_DP1_TXDP1	DisplayPort 1 Lane 1+ or HDMI Lane 1+	USB Type C Conn. J8 (via Alt Mode Switch)	Output	
B50	GND	–	GND	GND	–	GND
B51	HDMI_DP2_TX1_P	HDMI_DP2_TXDP1	DisplayPort 2 Lane 1+ or HDMI Lane 1+	HDMI Connector	Output	Diff pair, AC-Coupled on carrier board
B52	HDMI_DP2_TX1_N	HDMI_DP2_TXDN1	DisplayPort 2 Lane 1– or HDMI Lane 1–	HDMI Connector	Output	
B53	GND	–	GND	GND	–	GND
B54	WDT_RESET_OUT_N	SOC_GPIO23	Watchdog Timeout	Not used	Output	CMOS – 1.8V
B55	GPIO30	SOC_GPIO20	GPIO	M.2 Key M Connector (Alert)	Bidir	CMOS – 1.8V
B56	SPI1_CS1_N	SPI1_CS1	SPI 1 Chip Select 1	Expansion Connector	Bidir	CMOS – 1.8V
B57	GND	–	GND	GND	–	GND
B58	GPIO21	DAP6_SCLK	GPIO	SD Power Switch On	Output	CMOS – 3.3V
B59	GPIO04	DAP6_DIN	GPIO	–	Output	CMOS – 3.3V
B60	JTAG_TDI	JTAG_TDI	JTAG Test Data In	JTAG Connector	Input	CMOS – 1.8V
B61	CAN1_DIN	CAN1_DIN	CAN 1 Receive	CAN (40-pin Expansion Header)	Bidir	CMOS 3.3V
B62	GPIO08	CAN1_STB	GPIO / Digital Mic Input Data	Expansion Connector (AO DMIC In Data)	Input	CMOS 3.3V
B63	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
C1	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
C2	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
C3	GND	–	GND	GND	–	GND
C4	RGMII_RD0	EQOS_RD0	Ethernet Receive data bit 0	Ethernet PHY	Input	CMOS – 1.8V
C5	RGMII_RXC	EQOS_RXC	Ethernet Receive Clock	Ethernet PHY	Input	CMOS – 1.8V
C6	UFS0_RST_N	UFS0_RST	UFS Reset	Micro SD / UFS Card Socket	Output	CMOS – 1.2V
C7	I2S1_SDOUT	DAP1_FS	I2S Audio Port 1 Left/Right Clock	Audio Codec	Bidir	CMOS – 1.8V
C8	PEX_L5_CLKREQ_N	PEX_L5_CLKREQ_N	PCIe 5 Clock Request. Input when Jetson Xavier is Root Port. Output when Jetson Xavier is Endpoint.	PCIe x16 Connector	Input	CMOS – 1.8V
C9	GND	–	GND	GND	–	GND
C10	USB1_N	USB1_DN	USB 2.0, Port 1 Data–	USB Type C Connector (J8)	Bidir	USB2 Diff pair
C11	USB1_P	USB1_DP	USB 2.0, Port 1 Data+	USB Type C Connector (J8)	Bidir	USB2 Diff pair
C12	GND	–	GND	GND	–	GND
C13	GND	–	GND	GND	–	GND
C14	UPHY_RX9_N	PEX_RX9_N	UPHY Receive 9-	–	Input	PCIe/USB3/UFS Diff Pair, AC-Coupled on carrier board
C15	UPHY_RX9_P	PEX_RX9_P	UPHY Receive 9+	–	Input	
C16	GND	–	GND	GND	–	GND
C17	GND	–	GND	GND	–	GND
C18	UPHY_RX5_N	PEX_RX5_N	UPHY Receive 5-	M.2 Key M Connector	Input	PCIe Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
C19	UPHY_RX5_P	PEX_RX5_P	UPHY Receive 5+	M.2 Key M Connector	Input	
C20	GND	–	GND	GND	–	GND
C21	GND	–	GND	GND	–	GND
C22	UPHY_RX1_N	PEX_RX1_N	UPHY Receive 1-	USB Type C Alt Mode Switch	Input	USB3 Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
C23	UPHY_RX1_P	PEX_RX1_P	UPHY Receive 1+	USB Type C Alt Mode Switch	Input	
C24	GND	–	GND	GND	–	GND
C25	GND	–	GND	GND	–	GND
C26	NVHS0_SLVS_RX2_N	NVHS0_RX2_N	NVHS/PCIe/SLVS 0 Receive 2-	PCIe x16 Connector	Input	PCIe/SLVS Diff Pair, AC-Coupled on carrier board if
C27	NVHS0_SLVS_RX2_P	NVHS0_RX2_P	NVHS/PCIe/SLVS 0 Receive 2+	PCIe x16 Connector	Input	

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
						PCIe & direct connect to device.
C28	GND	–	GND	GND	–	GND
C29	GND	–	GND	GND	–	GND
C30	NVHS0_SLVS_RX6_N	NVHS0_RX6_N	NVHS/PCIe/SLVS 0 Receive 6-	PCIe x16 Connector	Input	PCIe/SLVS Diff Pair, AC-Coupled on carrier board if PCIe & direct connect to device.
C31	NVHS0_SLVS_RX6_P	NVHS0_RX6_P	NVHS/PCIe/SLVS 0 Receive 6+	PCIe x16 Connector	Input	
C32	GND	–	GND	GND	–	GND
C33	GND	–	GND	GND	–	GND
C34	RSVD	–	–	–	–	–
C35	RSVD	–	–	–	–	–
C36	GND	–	GND	GND	–	GND
C37	GND	–	GND	GND	–	GND
C38	RSVD	–	–	–	–	–
C39	RSVD	–	–	–	–	–
C40	GND	–	GND	GND	–	GND
C41	CSI2_D1_N	CSI_C_D1_N	Camera, CSI 2 Data 1–	Camera Connector	Input	MIPI D-PHY/C-PHY
C42	CSI2_D1_P	CSI_C_D1_P	Camera, CSI 2 Data 1+	Camera Connector	Input	MIPI D-PHY/C-PHY
C43	GND	–	GND	GND	–	GND
C44	CSI5_CLK_P	CSI_F_CLK_P	Camera, CSI 5 Clock+	Camera Connector	Input	MIPI D-PHY/C-PHY
C45	CSI5_CLK_N	CSI_F_CLK_N	Camera, CSI 5 Clock–	Camera Connector	Input	MIPI D-PHY/C-PHY
C46	GND	–	GND	GND	–	GND
C47	CSI7_D1_P	CSI_H_D1_P	Camera, CSI_7 Data 1+	Camera Connector	Input	MIPI D-PHY/C-PHY
C48	CSI7_D1_N	CSI_H_D1_N	Camera, CSI_7 Data 1–	Camera Connector	Input	MIPI D-PHY/C-PHY
C49	GND	–	GND	GND	–	GND
C50	HDMI_DP2_TX3_N	HDMI_DP2_TXDN3	DisplayPort 2 Lane 3– or HDMI Clk Lane–	HDMI Connector	Output	Diff pair, AC-Coupled on carrier board
C51	HDMI_DP2_TX3_P	HDMI_DP2_TXDP3	DisplayPort 2 Lane 3+ or HDMI Clk Lane+	HDMI Connector	Output	Diff pair, AC-Coupled on carrier board
C52	GND	–	GND	GND	–	GND
C53	I2C5_DAT	DP_AUX_CH3_N	General I2C 5 Data	Expansion Connector	Bidir	Open-Drain – 1.8V
C54	GPIO33	SOC_GPIO05	GPIO	–	Bidir	CMOS – 1.8V
C55	GPIO18	SOC_GPIO40	GPIO	PCIe x16 Connector (SLVS HSYNC)	Bidir	CMOS – 1.8V
C56	UART2_RX	UART2_RX	UART 2 Receive	UART-USB (MicroB) Bridge	Bidir	CMOS – 1.8V
C57	SPI3_CS0_N	SPI3_CS0	SPI 3 Chip Select 0	Not used	Bidir	CMOS – 1.8V
C58	UART2_TX	UART2_TX	UART 2 Transmit	UART-USB (MicroB) Bridge	Bidir	CMOS – 1.8V
C59	I2S3_SCLK	DAP4_SCLK	I2S Audio Port 3 Clock	M.2 Key E (through level shifter)	Bidir	CMOS – 3.3V
C60	I2S3_FS	DAP4_FS	I2S Audio Port 3 Left/Right Clock		Bidir	CMOS – 3.3V
C61	GPIO09	CAN1_EN	GPIO / Digital Mic Input Clock	Expansion Connector (AO DMIC In Clock)	OUtput	CMOS – 3.3V
C62	GND	–	GND	GND	–	GND
C63	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
C64	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
C65	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
D1	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
D2	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
D3	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
D4	GND	–	GND	GND	–	GND
D5	RGMII_RX_CTL	EQOS_RX_CTL	Ethernet Receive Control	Ethernet PHY	Input	CMOS – 1.8V
D6	SDCARD_D3	SDMMC1_DAT3	SD Card (or SDIO) Data 3	Micro SD / UFS Card Socket	Bidir	CMOS – 3.3V/1.8V
D7	GND	–	GND	GND	–	GND
D8	I2S1_FS	DAP1_DIN	I2S Audio Port 1 Data In	Audio Codec	Input	CMOS – 1.8V
D9	PEX_L1_CLKREQ_N	PEX_L1_CLKREQ_N	PCIe 1 Clock Request	–	Input	CMOS – 1.8V
D10	PEX_L0_RST_N	PEX_L0_RST_N	PCIe 0 Reset. Output when Jetson Xavier is Root Port. Input when Jetson Xavier is Endpoint.	M.2 Key M Connector	Output	CMOS – 1.8V
D11	GND	–	GND	GND	–	GND
D12	UPHY_RX11_P	PEX_RX11_P	UPHY Receive 11+	USB / eSATA Connector (USB 3.1)	Input	USB3 Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
D13	UPHY_RX11_N	PEX_RX11_N	UPHY Receive 11-	USB / eSATA Connector (USB 3.1)	Input	

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
D14	GND	–	GND	GND	–	GND
D15	GND	–	GND	GND	–	GND
D16	UPHY_RX7_P	PEX_RX7_P	UPHY Receive 7+	M.2 Key E Connector	Input	PCIe Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
D17	UPHY_RX7_N	PEX_RX7_N	UPHY Receive 7-	M.2 Key E Connector	Input	
D18	GND	–	GND	GND	–	GND
D19	GND	–	GND	GND	–	GND
D20	UPHY_RX3_P	PEX_RX3_P	UPHY Receive 3+	M.2 Key M Connector	Input	PCIe Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
D21	UPHY_RX3_N	PEX_RX3_N	UPHY Receive 3-	M.2 Key M Connector	Input	
D22	GND	–	GND	GND	–	GND
D23	GND	–	GND	GND	–	GND
D24	NVHS0_SLVS_RX0_P	NVHS0_RX0_P	NVHS/PCIe/SLVS 0 Receive 0+	PCIe x16 Connector	Input	PCIe/SLVS Diff Pair, AC-Coupled on carrier board if PCIe & direct connect to device.
D25	NVHS0_SLVS_RX0_N	NVHS0_RX0_N	NVHS/PCIe/SLVS 0 Receive 0-	PCIe x16 Connector	Input	
D26	GND	–	GND	GND	–	GND
D27	GND	–	GND	GND	–	GND
D28	NVHS0_SLVS_RX4_P	NVHS0_RX4_P	NVHS/PCIe/SLVS 0 Receive 4+	PCIe x16 Connector	Input	PCIe/SLVS Diff Pair, AC-Coupled on carrier board if PCIe & direct connect to device.
D29	NVHS0_SLVS_RX4_N	NVHS0_RX4_N	NVHS/PCIe/SLVS 0 Receive 4-	PCIe x16 Connector	Input	
D30	GND	–	GND	GND	–	GND
D31	GND	–	GND	GND	–	GND
D32	RSVD	–	–	–	–	–
D33	RSVD	–	–	–	–	–
D34	GND	–	GND	GND	–	GND
D35	GND	–	GND	GND	–	GND
D36	RSVD	–	–	–	–	–
D37	RSVD	–	–	–	–	–
D38	GND	–	GND	GND	–	GND
D39	GND	–	GND	GND	–	GND
D40	MID3	–	Module ID #3	–	–	–
D41	GND	–	GND	GND	–	GND
D42	CSI5_D0_P	CSI_F_D0_P	Camera, CSI 5 Data 0+	Camera Connector	Input	MIPI D-PHY/C-PHY
D43	CSI5_D0_N	CSI_F_D0_N	Camera, CSI 5 Data 0–	Camera Connector	Input	MIPI D-PHY/C-PHY
D44	GND	–	GND	GND	–	GND
D45	CSI5_D1_N	CSI_F_D1_N	Camera, CSI 5 Data 1–	Camera Connector	Input	MIPI D-PHY/C-PHY
D46	CSI5_D1_P	CSI_F_D1_P	Camera, CSI 5 Data 1+	Camera Connector	Input	MIPI D-PHY/C-PHY
D47	GND	–	GND	GND	–	GND
D48	HDMI_DP1_TX2_N	HDMI_DP1_TXDN2	DisplayPort 1 Lane 2– or HDMI Lane 0–	USB Type C Conn. J8 (via Alt Mode Switch)	Output	Diff pair, AC-Coupled on carrier board
D49	HDMI_DP1_TX2_P	HDMI_DP1_TXDP2	DisplayPort 1 Lane 2+ or HDMI Lane 0+	USB Type C Conn. J8 (via Alt Mode Switch)	Output	
D50	GND	–	GND	GND	–	GND
D51	HDMI_DP2_TX0_P	HDMI_DP2_TXDP0	DisplayPort 2 Lane 0+ or HDMI Lane 2+	HDMI Connector	Output	Diff pair, AC-Coupled on carrier board
D52	HDMI_DP2_TX0_N	HDMI_DP2_TXDN0	DisplayPort 2 Lane 0– or HDMI Lane 2–	HDMI Connector	Output	
D53	GND	–	GND	GND	–	GND
D54	GPIO03	SOC_GPIO52	GPIO	M.2 Key E Connector (AP Wake BT)	Bidir	CMOS – 1.8V
D55	SPI1_MOSI	SPI1_MOSI	SPI 1 Master Out / Slave In	Expansion Connector	Bidir	CMOS – 1.8V
D56	SPI3_MISO	SPI3_MISO	SPI 3 Master In / Slave Out	PCIe x16 Connector (SLVS_XCLR)	Bidir	CMOS – 1.8V
D57	GND	–	GND	GND	–	GND
D58	JTAG_TDO	JTAG_TDO	JTAG Test Data Out	JTAG Connector	Output	CMOS – 1.8V
D59	CAN0_DOUT	CAN0_DOUT	CAN 0 Transmit	CAN (40-pin Expansion Header)	Bidir	CMOS 3.3V
D60	SPI2_CS0_N	SPI2_CS0	SPI 2 Chip Select 0	PCIe x16 Connector	Bidir	CMOS – 1.8V
D61	I2C4_CLK	GEN8_I2C_SCL	General I2C 4 Clock	Audio Codec & Camera Connector	Bidir	Open-Drain – 1.8V
D62	SPI2_MISO	SPI2_MISO	SPI 2 Master In / Slave Out	PCIe x16 Connector	Bidir	CMOS – 1.8V

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
D63	GND	–	GND	GND	–	GND
D64	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
D65	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
E1	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
E2	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
E3	GND	–	GND	GND	–	GND
E4	I2S2_FS	DAP2_FS	I2S Audio Port 2 Left/Right Clock	BT Audio	Bidir	CMOS – 1.8V
E5	RGMII_RD3	EQOS_RD3	Ethernet Receive data bit 3	Ethernet PHY	Input	CMOS – 1.8V
E6	RGMII_SMA_MDC	EQOS_SMA_MDC	Ethernet Management Clock	Ethernet PHY	Output	CMOS – 1.8V
E7	RGMII_SMA_MDIO	EQOS_SMA_MDIO	Ethernet Management Data	Ethernet PHY	Bidir	CMOS – 1.8V
E8	SDCARD_D0	SDMMC1_DAT0	SD Card (or SDIO) Data 0	Micro SD / UFS Card Socket	Bidir	CMOS – 3.3V/1.8V
E9	GND	–	GND	GND	–	GND
E10	GPIO12	SOC_GPIO33	GPIO	M.2 Key E Connector (M2 Wake AP)	Bidir	CMOS – 1.8V
E11	PEX_L0_CLKREQ_N	PEX_L0_CLKREQ_N	PCIe 0 Clock Request. Input when Jetson Xavier is Root Port. Output when Jetson Xavier is Endpoint.	M.2 Key M Connector	Input	CMOS – 1.8V
E12	GND	–	GND	GND	–	GND
E13	GND	–	GND	GND	–	GND
E14	PEX_CLK0_N	PEX_CLK0N	PCIe 0 Reference Clock– when Jetson Xavier is Root Port. Unused when Jetson Xavier used as Endpoint.	M.2 Key M Connector	Output	PCIe Diff Pair
E15	PEX_CLK0_P	PEX_CLK0P	PCIe 0 Reference Clock+ when Jetson Xavier is Root Port. Unused when used as Endpoint.	M.2 Key M Connector	Output	PCIe Diff Pair
E16	GND	–	GND	GND	–	GND
E17	GND	–	GND	GND	–	GND
E18	RSVD	–	–	–	–	–
E19	RSVD	–	–	–	–	–
E20	GND	–	GND	GND	–	GND
E21	GND	–	GND	GND	–	GND
E22	PEX_CLK4_N	PEX_CLK4N	PCIe 4 Reference Clock– when Jetson Xavier is Root Port. Unused when Jetson Xavier used as Endpoint.	–	Output	Diff pair
E23	PEX_CLK4_P	PEX_CLK4P	PCIe 4 Reference Clock+ when Jetson Xavier is Root Port. Unused when used as Endpoint.	–	Output	
E24	GND	–	GND	GND	–	GND
E25	GND	–	GND	GND	–	GND
E26	UPHY_REFCLK1_N	PEX_REFCLK1_N	UPHY Reference Clock 1-	Unused	Input	PCIe Diff Pair
E27	UPHY_REFCLK1_P	PEX_REFCLK1_P	UPHY Reference Clock 1+	Unused	Input	PCIe Diff Pair
E28	GND	–	GND	GND	–	GND
E29	GND	–	GND	GND	–	GND
E30	NVHS0_SLVS_REFCLK0_P	NVHS0_REFCLK_P	NVHS Reference Clock 0+ used when Jetson Xavier is an Endpoint	PCIe x16 Connector	Input	PCIe Diff Pair
E31	NVHS0_SLVS_REFCLK0_N	NVHS0_REFCLK_N	NVHS Reference Clock 0- used when Jetson Xavier is an Endpoint	PCIe x16 Connector	Input	PCIe Diff Pair
E32	GND	–	GND	GND	–	GND
E33	GND	–	GND	GND	–	GND
E34	RSVD	–	–	–	–	–
E35	RSVD	–	–	–	–	–
E36	GND	–	GND	GND	–	GND
E37	GND	–	GND	GND	–	GND
E38	CSI0_D1_N	CSI_A_D1_N	Camera, CSI 0 Data 1–	Camera Connector	Input	MIPI D-PHY/C-PHY
E39	CSI0_D1_P	CSI_A_D1_P	Camera, CSI 0 Data 1+	Camera Connector	Input	MIPI D-PHY/C-PHY
E40	GND	–	GND	GND	–	GND
E41	CSI0_D0_N	CSI_A_D0_N	Camera, CSI 0 Data 0–	Camera Connector	Input	MIPI D-PHY/C-PHY
E42	CSI0_D0_P	CSI_A_D0_P	Camera, CSI 0 Data 0+	Camera Connector	Input	MIPI D-PHY/C-PHY
E43	GND	–	GND	GND	–	GND
E44	CSI3_D0_N	CSI_D_D0_N	Camera, CSI 3 Data 0–	Camera Connector	Input	MIPI D-PHY/C-PHY
E45	CSI3_D0_P	CSI_D_D0_P	Camera, CSI 3 Data 0+	Camera Connector	Input	MIPI D-PHY/C-PHY
E46	GND	–	GND	GND	–	GND
E47	CSI4_D1_P	CSI_E_D1_P	Camera, CSI 4 Data 1+	Camera Connector	Input	MIPI D-PHY/C-PHY
E48	CSI4_D1_N	CSI_E_D1_N	Camera, CSI 4 Data 1–	Camera Connector	Input	MIPI D-PHY/C-PHY

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
E49	GND	–	GND	GND	–	GND
E50	HDMI_DP1_TX3_P	HDMI_DP1_TXDP3	DisplayPort 1 Lane 3+ or HDMI Clk Lane+	USB Type C Conn. J8 (via Alt Mode Switch)	Output	Diff pair, AC-Coupled on carrier board
E51	HDMI_DP1_TX3_N	HDMI_DP1_TXDN3	DisplayPort 1 Lane 3– or HDMI Clk Lane–	USB Type C Conn. J8 (via Alt Mode Switch)	Output	
E52	GND	–	GND	GND	–	GND
E53	I2C3_DAT	CAM_I2C_SDA	General I2C 3 Data	Camera Connector	Bidir	Open-Drain – 1.8V
E54	FAN_TACH	SOC_GPIO22	Fan Tachometer signal	Fan Circuit/Connector	Input	CMOS – 1.8V
E55	SPI1_CS0_N	SPI1_CS0	SPI 1 Chip Select 0	Expansion Connector	Bidir	CMOS – 1.8V
E56	SPI3_CS1_N	SPI3_CS1	SPI 3 Chip Select 1	Not used	Bidir	CMOS – 1.8V
E57	GND	–	GND	GND	–	GND
E58	JTAG_TMS	JTAG_TMS	JTAG Test Mode Select	JTAG Connector	Input	CMOS – 1.8V
E59	GPIO06	CAN0_EN	GPIO	PCIe REFCLK mux Select	Bidir	CMOS – 3.3V
E60	I2C4_DAT	GEN8_I2C_SDA	General I2C 4 Data	Audio Codec & Camera Connector	Bidir	Open-Drain – 1.8V
E61	SPI2_CLK	SPI2_SCK	SPI 2 Clock	PCIe x16 Connector	Bidir	CMOS – 1.8V
E62	GND	–	GND	GND	–	GND
E63	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
E64	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
E65	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
F1	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
F2	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
F3	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
F4	GND	–	GND	GND	–	GND
F5	I2S2_DOUT	DAP2_DOUT	I2S Audio Port 2 Data Out	BT Audio	Output	CMOS – 1.8V
F6	I2S2_DIN	DAP2_DIN	I2S Audio Port 2 Data In	BT Audio	Input	CMOS – 1.8V
F7	GND	–	GND	GND	–	GND
F8	SDCARD_D1	SDMMC1_DAT1	SD Card (or SDIO) Data 1	Micro SD / UFS Card Socket	Bidir	CMOS – 3.3V/1.8V
F9	GPIO16	DAP5_DOUT	GPIO / Digital Speaker Output Data	Camera Connector (Camera 1 Reset)	Output	CMOS – 1.8V
F10	GPIO15	DAP5_SCLK	GPIO / Digital Speaker Output Clock	Camera Connector (Camera 1 Powerdown)	Bidir	CMOS – 1.8V
F11	GND	–	GND	GND	–	GND
F12	USB0_P	USB0_DP	USB 2.0 Port 0 Data+	UART-USB Bridge or USB Type C Connector (J7)	Bidir	USB2 Diff pair
F13	USB0_N	USB0_DN	USB 2.0 Port 0 Data–	UART-USB Bridge or USB Type C Connector (J7)	Bidir	USB2 Diff pair
F14	GND	–	GND	GND	–	GND
F15	GND	–	GND	GND	–	GND
F16	PEX_CLK1_P	PEX_CLK1P	PCIe 1 Reference Clock–	–	Output	PCIe Diff Pair
F17	PEX_CLK1_N	PEX_CLK1N	PCIe 1 Reference Clock+	–	Output	PCIe Diff Pair
F18	GND	–	GND	GND	–	GND
F19	GND	–	GND	GND	–	GND
F20	PEX_CLK3_P	PEX_CLK3P	PCIe 3 Reference Clock–	M.2 Key E Connector	Output	Diff pair
F21	PEX_CLK3_N	PEX_CLK3N	PCIe 3 Reference Clock+	M.2 Key E Connector	Output	Diff pair
F22	GND	–	GND	GND	–	GND
F23	GND	–	GND	GND	–	GND
F24	PEX_CLK5_P	PEX_CLK5P	PCIe 5 Reference Clock+ when Jetson Xavier is Root Port. Unused when used as Endpoint.	PCIe x16 Connector	Output	Diff pair
F25	PEX_CLK5_N	PEX_CLK5N	PCIe 5 Reference Clock– when Jetson Xavier is Root Port. Unused when Jetson Xavier used as Endpoint.	PCIe x16 Connector	Output	Diff pair
F26	GND	–	GND	GND	–	GND
F27	GND	–	GND	GND	–	GND
F28	RSVD	–	–	–	–	–
F29	RSVD	–	–	–	–	–
F30	GND	–	GND	GND	–	GND
F31	GND	–	GND	GND	–	GND
F32	RSVD	–	–	–	–	–
F33	RSVD	–	–	–	–	–
F34	GND	–	GND	GND	–	GND
F35	GND	–	GND	GND	–	GND
F36	RSVD	–	–	–	–	–

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
F37	RSVD	–	–	–	–	–
F38	GND	–	GND	GND	–	GND
F39	GND	–	GND	GND	–	GND
F40	MID2	–	Module ID #2	–	–	–
F41	GND	–	GND	GND	–	GND
F42	CSI0_CLK_N	CSI_A_CLK_N	Camera, CSI 0 Clock–	Camera Connector	Input	MIPI D-PHY/C-PHY
F43	CSI0_CLK_P	CSI_A_CLK_P	Camera, CSI 0 Clock+	Camera Connector	Input	MIPI D-PHY/C-PHY
F44	GND	–	GND	GND	–	GND
F45	CSI3_CLK_N	CSI_D_CLK_N	Camera, CSI 3 Clock–	Camera Connector	Input	MIPI D-PHY/C-PHY
F46	CSI3_CLK_P	CSI_D_CLK_P	Camera, CSI 3 Clock+	Camera Connector	Input	MIPI D-PHY/C-PHY
F47	GND	–	GND	GND	–	GND
F48	CSI4_CLK_P	CSI_E_CLK_P	Camera CSI 4 Clock+	Camera Connector	Input	MIPI D-PHY/C-PHY
F49	CSI4_CLK_N	CSI_E_CLK_N	Camera, CSI 4 Clock–	Camera Connector	Input	MIPI D-PHY/C-PHY
F50	GND	–	GND	GND	–	GND
F51	DP0_AUX_CH_N	DP_AUX_CH0_N	Display Port 0 Aux– or HDMI DDC SDA	USB Type C Conn. J7 (via Alt Mode Switch)	Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC/I2C)
F52	DP0_AUX_CH_P	DP_AUX_CH0_P	Display Port 0 Aux+ or HDMI DDC SCL	USB Type C Conn. J7 (via Alt Mode Switch)	Bidir	
F53	I2C3_CLK	CAM_I2C_SCL	General I2C 3 Clock	Camera Connector	Bidir	Open-Drain – 1.8V
F54	GPIO22	USB_VBUS_EN0	GPIO	VDD_5V_SATA Load Switch Enable	Output	CMOS – 1.8V
F55	SPI3_CLK	SPI3_SCK	SPI 3 Clock	Not used	Bidir	CMOS – 1.8V
F56	GPIO36	SOC_GPIO53	GPIO	AVDD_CAM_2V8 LDO Enable	Output	CMOS – 1.8V
F57	GND	–	GND	GND	–	GND
F58	CAN0_DIN	CAN0_DIN	CAN 0 Receive	CAN (40-pin Expansion Header)	Bidir	CMOS 3.3V
F59	GPIO07	CAN0_WAKE	GPIO	Not Used	Bidir	CMOS – 3.3V
F60	SPI2_MOSI	SPI2_MOSI	SPI 2 Master Out / Slave In	PCIe x16 Connector	Bidir	CMOS – 1.8V
F61	VCOMP_ALERT_N	VCOMP_ALERT	TBD	Not used	Input	CMOS – 1.8V
F62	GND	–	GND	GND	–	GND
F63	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
F64	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
F65	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
G1	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
G2	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
G3	GND	–	GND	GND	–	GND
G4	I2S2_CLK	DAP2_SCLK	I2S Audio Port 2 Clock	BT Audio	Bidir	CMOS – 1.8V
G5	RGMII_TD1	EQOS_TD1	Ethernet Transmit data bit 1	Ethernet PHY	Output	CMOS – 1.8V
G6	RGMII_TD3	EQOS_TD3	Ethernet Transmit data bit 3	Ethernet PHY	Output	CMOS – 1.8V
G7	GPIO13	DAP3_DIN	GPIO	M.2 Key E Connector (BT Wake AP)	Input	CMOS – 1.8V
G8	PEX_L4_CLKREQ_N	PEX_L4_CLKREQ_N	PCIe 4 Clock Request. Input when Jetson Xavier is Root Port. Output when Jetson Xavier is Endpoint.	–	Input	CMOS – 1.8V
G9	GND	–	GND	GND	–	GND
G10	USB3_N	USB3_DN	USB 2.0, Port 3 Data–	USB / eSATA Connector (USB 2.0)	Bidir	USB2 Diff pair
G11	USB3_P	USB3_DP	USB 2.0, Port 3 Data+	USB / eSATA Connector (USB 2.0)	Bidir	USB2 Diff pair
G12	GND	–	GND	GND	–	GND
G13	GND	–	GND	GND	–	GND
G14	UPHY_TX9_N	PEX_TX9_N	UPHY Transmit 9-	–	Output	PCIe/USB3/UFS Diff Pair, AC-Coupled on carrier board
G15	UPHY_TX9_P	PEX_TX9_P	UPHY Transmit 9+	–	Output	
G16	GND	–	GND	GND	–	GND
G17	GND	–	GND	GND	–	GND
G18	UPHY_TX5_N	PEX_TX5_N	UPHY Transmit 5-	M.2 Key M Connector	Output	PCIe Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
G19	UPHY_TX5_P	PEX_TX5_P	UPHY Transmit 5+	M.2 Key M Connector	Output	
G20	GND	–	GND	GND	–	GND
G21	GND	–	GND	GND	–	GND

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
G22	UPHY_TX1_N	PEX_TX1_N	UPHY Transmit 1-	USB Type C Alt Mode Switch (for J7)	Output	USB3 Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
G23	UPHY_TX1_P	PEX_TX1_P	UPHY Transmit 1+	USB Type C Alt Mode Switch (for J7)	Output	
G24	GND	–	GND	GND	–	GND
G25	GND	–	GND	GND	–	GND
G26	NVHS0_TX2_N	NVHS0_TX2_N	NVHS/PCIe/SLVS 0 Transmit 2-	PCIe x16 Connector	Output	PCIe Diff Pair, AC-Coupled on carrier board
G27	NVHS0_TX2_P	NVHS0_TX2_P	NVHS/PCIe/SLVS 0 Transmit 2+	PCIe x16 Connector	Output	
G28	GND	–	GND	GND	–	GND
G29	GND	–	GND	GND	–	GND
G30	NVHS0_TX6_N	NVHS0_TX6_N	NVHS/PCIe/SLVS 0 Transmit 6-	PCIe x16 Connector	Output	PCIe Diff Pair, AC-Coupled on carrier board
G31	NVHS0_TX6_P	NVHS0_TX6_P	NVHS/PCIe/SLVS 0 Transmit 6+	PCIe x16 Connector	Output	
G32	GND	–	GND	GND	–	GND
G33	GND	–	GND	GND	–	GND
G34	RSVD	–	–	–	–	–
G35	RSVD	–	–	–	–	–
G36	GND	–	GND	GND	–	GND
G37	GND	–	GND	GND	–	GND
G38	RSVD	–	–	–	–	–
G39	RSVD	–	–	–	–	–
G40	GND	–	GND	GND	–	GND
G41	CSI1_D0_P	CSI_B_D0_P	Camera, CSI 1 Data 0+	Camera Connector	Input	MIPI D-PHY/C-PHY
G42	CSI1_D0_N	CSI_B_D0_N	Camera, CSI 1 Data 0–	Camera Connector	Input	MIPI D-PHY/C-PHY
G43	GND	–	GND	GND	–	GND
G44	CSI3_D1_P	CSI_D_D1_P	Camera, CSI 3 Data 1+	Camera Connector	Input	MIPI D-PHY/C-PHY
G45	CSI3_D1_N	CSI_D_D1_N	Camera, CSI 3 Data 1–	Camera Connector	Input	MIPI D-PHY/C-PHY
G46	GND	–	GND	GND	–	GND
G47	CSI4_D0_N	CSI_E_D0_N	Camera, CSI 4 Data 0–	Camera Connector	Input	MIPI D-PHY/C-PHY
G48	CSI4_D0_P	CSI_E_D0_P	Camera, CSI 4 Data 0+	Camera Connector	Input	MIPI D-PHY/C-PHY
G49	GND	–	GND	GND	–	GND
G50	HDMI_DP0_TX1_N	HDMI_DP0_TXDN1	DisplayPort 0 Lane 1– or HDMI Lane 1–	USB Type C Conn. J7 (via Alt Mode Switch)	Output	Diff pair, AC-Coupled on carrier board
G51	HDMI_DP0_TX1_P	HDMI_DP0_TXDP1	DisplayPort 0 Lane 1+or HDMI Lane 1+	USB Type C Conn. J7 (via Alt Mode Switch)	Output	Diff pair, AC-Coupled on carrier board
G52	GND	–	GND	GND	–	GND
G53	DP2_AUX_CH_P	DP_AUX_CH2_P	Display Port 2 Aux+ or HDMI DDC SCL	HDMI Connector	Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC/I2C)
G54	DP2_AUX_CH_N	DP_AUX_CH2_N	Display Port 2 Aux– or HDMI DDC SDA	HDMI Connector	Bidir	
G55	GPIO23	USB_VBUS_EN1	GPIO	PCIe x16 Conn. 3.3V Load Switch Enable	Output	CMOS – 1.8V
G56	SPI3_MOSI	SPI3_MOSI	SPI 3 Master Out / Slave In	PCIe x16 Connector (SLVS_XCE)	Bidir	CMOS – 1.8V
G57	GND	–	GND	GND	–	GND
G58	UART2_RTS	UART2_RTS	UART 2 Request to Send	UART-USB (MicroB) Bridge	Bidir	CMOS – 1.8V
G59	RSVD	–	–	–	–	–
G60	NVDBG_SEL	NVDBG_SEL	NVIDIA Debug Select	Driven low	Input	CMOS – 1.8V
G61	JTAG_TRST_N	JTAG_TRST_N	JTAG Test Reset	JTAG Connector	Input	CMOS – 1.8V
G62	GND	–	GND	GND	–	GND
G63	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
G64	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
G65	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
H1	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
H2	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
H3	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
H4	GND	–	GND	GND	–	GND
H5	ENET_RST_N	SOC_GPIO09	Ethernet Reset	Ethernet PHY	Output	CMOS – 1.8V
H6	RGMII_RD2	EQOS_RD2	Ethernet Receive data bit 2	Ethernet PHY	Input	CMOS – 1.8V
H7	GND	–	GND	GND	–	GND
H8	I2S1_SDIN	DAP1_DOUT	I2S Audio Port 1 Data Out	Audio Codec	Output	CMOS – 1.8V
H9	MCLK01	AUD_MCLK	Audio Codec Master Clock	Audio Codec	Output	CMOS – 1.8V

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
H10	PEX_L5_RST_N	PEX_L5_RST_N	PCIe 5 Reset. Output when Jetson Xavier is Root Port. Input when Jetson Xavier is Endpoint.	PCIe x16 Connector	Output	CMOS – 1.8V
H11	GND	–	GND	GND	–	GND
H12	UPHY_TX11_P	PEX_TX11_P	UPHY Transmit 11+	USB / eSATA Connector (USB 3.1)	Output	USB3 Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
H13	UPHY_TX11_N	PEX_TX11_N	UPHY Transmit 11-	USB / eSATA Connector (USB 3.1)	Output	
H14	GND	–	GND	GND	–	GND
H15	GND	–	GND	GND	–	GND
H16	UPHY_TX7_P	PEX_TX7_P	UPHY Transmit 7+	M.2 Key E Connector	Output	PCIe Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
H17	UPHY_TX7_N	PEX_TX7_N	UPHY Transmit 7-	M.2 Key E Connector	Output	
H18	GND	–	GND	GND	–	GND
H19	GND	–	GND	GND	–	GND
H20	UPHY_TX3_P	PEX_TX3_P	UPHY Transmit 3+	M.2 Key M Connector	Output	PCIe Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
H21	UPHY_TX3_N	PEX_TX3_N	UPHY Transmit 3-	M.2 Key M Connector	Output	
H22	GND	–	GND	GND	–	GND
H23	GND	–	GND	GND	–	GND
H24	NVHS0_TX0_P	NVHS0_TX0_P	NVHS/PCIe/SLVS 0 Transmit 0+	PCIe x16 Connector	Output	PCIe Diff Pair, AC-Coupled on carrier board
H25	NVHS0_TX0_N	NVHS0_TX0_N	NVHS/PCIe/SLVS 0 Transmit 0-	PCIe x16 Connector	Output	
H26	GND	–	GND	GND	–	GND
H27	GND	–	GND	GND	–	GND
H28	NVHS0_TX4_P	NVHS0_TX4_P	NVHS/PCIe/SLVS 0 Transmit 4+	PCIe x16 Connector	Output	PCIe Diff Pair, AC-Coupled on carrier board
H29	NVHS0_TX4_N	NVHS0_TX4_N	NVHS/PCIe/SLVS 0 Transmit 4-	PCIe x16 Connector	Output	
H30	GND	–	GND	GND	–	GND
H31	GND	–	GND	GND	–	GND
H32	RSVD	–	–	–	–	–
H33	RSVD	–	–	–	–	–
H34	GND	–	GND	GND	–	GND
H35	GND	–	GND	GND	–	GND
H36	RSVD	–	–	–	–	–
H37	RSVD	–	–	–	–	–
H38	GND	–	GND	GND	–	GND
H39	GND	–	GND	GND	–	GND
H40	MID1	–	Module ID #1	–	–	–
H41	GND	–	GND	GND	–	GND
H42	CSI1_CLK_N	CSI_B_CLK_N	Camera, CSI 1 Clock–	Camera Connector	Input	MIPI D-PHY/C-PHY
H43	CSI1_CLK_P	CSI_B_CLK_P	Camera, CSI 1 Clock+	Camera Connector	Input	MIPI D-PHY/C-PHY
H44	GND	–	GND	GND	–	GND
H45	CSI6_D1_N	CSI_G_D1_N	Camera, CSI_6 Data 1–	Camera Connector	Input	MIPI D-PHY/C-PHY
H46	CSI6_D1_P	CSI_G_D1_P	Camera, CSI_6 Data 1+	Camera Connector	Input	MIPI D-PHY/C-PHY
H47	GND	–	GND	GND	–	GND
H48	HDMI_DP0_TX0_N	HDMI_DP0_TXDN0	DisplayPort 0 Lane 0– or HDMI Lane 2–	USB Type C Conn. J7 (via Alt Mode Switch)	Output	Diff pair, AC-Coupled on carrier board
H49	HDMI_DP0_TX0_P	HDMI_DP0_TXDP0	DisplayPort 0 Lane 0+ or HDMI Lane 2+	USB Type C Conn. J7 (via Alt Mode Switch)	Output	
H50	GND	–	GND	GND	–	GND
H51	GPIO26	SOC_GPIO51	GPIO	M.2 Key E Connector (BT Reset)	Output	CMOS – 1.8V
H52	GPIO27	SOC_GPIO54	GPIO	PWM2 (40-pin Expansion Header)	Output	CMOS – 1.8V
H53	MCLK03	EXTPERIPH2_CLK	Camera 1 Master Clock	Camera Connector	Output	CMOS – 1.8V
H54	UART1_CTS	UART1_CTS	UART 1 Clear to Send	Expansion Connector via level shifter	Input	CMOS – 1.8V
H55	MCLK04	SOC_GPIO41	Camera 2 Master Clock	Camera Connector	Output	CMOS – 1.8V
H56	GND	–	GND	GND	–	GND
H57	UART5_CTS	UART5_CTS	UART 5 Clear to Send	M.2 Key E Connector	Bidir	CMOS – 1.8V
H58	UART5_RX	UART5_RX	UART 5 Receive	M.2 Key E Connector	Bidir	CMOS – 1.8V

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
H59	NVJTAG_SEL	NVJTAG_SEL	NVIDIA JTAG Select	Driven low	Input	CMOS – 1.8V
H60	GPIO31	SAFE_STATE	GPIO	Micro SD / UFS Card Socket (UFS Detect)	Input	CMOS – 1.8V
H61	CAN1_DOUT	CAN1_DOUT	CAN 1 Transmit	CAN (40-pin Expansion Header)	Bidir	CMOS 3.3V
H62	UART3_TX_DEBUG	UART3_TX	Debug UART Transmit	UART-USB (MicroB) Bridge	Input	CMOS – 1.8V
H63	GND	–	GND	GND	–	GND
H64	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
H65	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
J1	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
J2	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
J3	GND	–	GND	GND	–	GND
J4	GPIO01	SOC_GPIO03	GPIO	M.2 Key E Connector (WiFi Disable)	Output	CMOS – 1.8V
J5	ENET_INT	SOC_GPIO08	Ethernet Interrupt	Ethernet PHY	Input	CMOS – 1.8V
J6	RGMII_TD0	EQOS_TD0	Ethernet Transmit data bit 0	Ethernet PHY	Output	CMOS – 1.8V
J7	RGMII_TD2	EQOS_TD2	Ethernet Transmit data bit 2	Ethernet PHY	Output	CMOS – 1.8V
J8	GND	–	GND	GND	–	GND
J9	PEX_L4_RST_N	PEX_L4_RST_N	PCIe 4 Reset. Output when Jetson Xavier is Root Port. Input when Jetson Xavier is Endpoint.	–	Output	CMOS – 1.8V
J10	PEX_L3_CLKREQ_N	PEX_L3_CLKREQ_N	PCIe 3 Clock Request	M.2 Key E Connector	Input	CMOS – 1.8V
J11	RSVD	–	–	–	–	–
J12	GND	–	GND	GND	–	GND
J13	GND	–	GND	GND	–	GND
J14	UPHY_TX8_P	PEX_TX8_P	UPHY Transmit 8+	–	Output	PCIe/USB3/UFS Diff Pair, AC-Coupled on carrier board
J15	UPHY_TX8_N	PEX_TX8_N	UPHY Transmit 8-	–	Output	
J16	GND	–	GND	GND	–	GND
J17	GND	–	GND	GND	–	GND
J18	UPHY_TX4_P	PEX_TX4_P	UPHY Transmit 4+	M.2 Key M Connector	Output	PCIe Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
J19	UPHY_TX4_N	PEX_TX4_N	UPHY Transmit 4-	M.2 Key M Connector	Output	
J20	GND	–	GND	GND	–	GND
J21	GND	–	GND	GND	–	GND
J22	UPHY_TX0_P	PEX_TX0_P	UPHY Transmit 0+	eSATA Bridge	Output	PCIe Diff Pair, - TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
J23	UPHY_TX0_N	PEX_TX0_N	UPHY Transmit 0-	eSATA Bridge	Output	
J24	GND	–	GND	GND	–	GND
J25	GND	–	GND	GND	–	GND
J26	NVHS0_TX3_P	NVHS0_TX3_P	NVHS/PCIe/SLVS 0 Transmit 3+	PCIe x16 Connector	Output	PCIe Diff Pair, AC-Coupled on carrier board
J27	NVHS0_TX3_N	NVHS0_TX3_N	NVHS/PCIe/SLVS 0 Transmit 3-	PCIe x16 Connector	Output	
J28	GND	–	GND	GND	–	GND
J29	GND	–	GND	GND	–	GND
J30	NVHS0_TX7_P	NVHS0_TX7_P	NVHS/PCIe/SLVS 0 Transmit 7+	PCIe x16 Connector	Output	PCIe Diff Pair, AC-Coupled on carrier board
J31	NVHS0_TX7_N	NVHS0_TX7_N	NVHS/PCIe/SLVS 0 Transmit 7-	PCIe x16 Connector	Output	
J32	GND	–	GND	GND	–	GND
J33	GND	–	GND	GND	–	GND
J34	RSVD	–	–	–	–	–
J35	RSVD	–	–	–	–	–
J36	GND	–	GND	GND	–	GND
J37	GND	–	GND	GND	–	GND
J38	RSVD	–	–	–	–	–
J39	RSVD	–	–	–	–	–
J40	GND	–	GND	GND	–	GND
J41	CSI1_D1_P	CSI_B_D1_P	Camera, CSI 1 Data 1+	Camera Connector	Input	MIPI D-PHY/C-PHY
J42	CSI1_D1_N	CSI_B_D1_N	Camera, CSI 1 Data 1–	Camera Connector	Input	MIPI D-PHY/C-PHY
J43	GND	–	GND	GND	–	GND
J44	CSI6_CLK_P	CSI_G_CLK_P	Camera, CSI_6 Clock+	Camera Connector	Input	MIPI D-PHY/C-PHY
J45	CSI6_CLK_N	CSI_G_CLK_N	Camera, CSI 5 Clock–	Camera Connector	Input	MIPI D-PHY/C-PHY

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
J46	GND	–	GND	GND	–	GND
J47	HDMI_DP0_TX2_P	HDMI_DP0_TXDP2	DisplayPort 0 Lane 2+ or HDMI Lane 0+	USB Type C Conn. J7 (via Alt Mode Switch)	Output	Diff pair, AC-Coupled on carrier board
J48	HDMI_DP0_TX2_N	HDMI_DP0_TXDN2	DisplayPort 0 Lane 2– or HDMI Lane 0–	USB Type C Conn. J7 (via Alt Mode Switch)	Output	
J49	GND	–	GND	GND	–	GND
J50	HDMI_CEC	HDMI_CEC	HDMI CEC	HDMI Connector	Bidir	Open Drain, 1.8V
J51	GPIO24	DP_AUX_CH3_HPD	GPIO	M.2 Key E Connector (SAR TOUT)	Output	CMOS – 1.8V
J52	DP1_AUX_CH_P	DP_AUX_CH1_P	Display Port 1 Aux+ or HDMI DDC SCL	USB Type C Conn. J8 (via Alt Mode Switch)	Bidir	AC-Coupled on Carrier Board (eDP/DP) or Open-Drain, 1.8V (3.3V tolerant - DDC/I2C)
J53	DP1_AUX_CH_N	DP_AUX_CH1_N	Display Port 1 Aux– or HDMI DDC SDA	USB Type C Conn. J8 (via Alt Mode Switch)	Bidir	
J54	MCLK02	EXTPERIPH1_CLK	Camera 0 Master Clock	Camera Connector	Output	CMOS – 1.8V
J55	GPIO32	SOC_GPIO04	GPIO	–	Bidir	CMOS – 1.8V
J56	GND	–	GND	GND	–	GND
J57	SPI1_CLK	SPI1_SCK	SPI 1 Clock	Expansion Connector	Bidir	CMOS – 1.8V
J58	UART5_TX	UART5_TX	UART 5 Transmit	M.2 Key E Connector	Bidir	CMOS – 1.8V
J59	I2S3_DIN	DAP4_DIN	I2S Audio Port 3 Data In	M.2 Key E	Input	CMOS – 3.3V
J60	STANDBY_ACK_N	SOC_PWR_REQ	Standby Acknowledge	System	Output	CMOS – 1.8V
J61	I2C2_CLK	GEN2_I2C_SCL	General I2C 2 Clock	Various	Bidir	Open-Drain – 1.8V
J62	GND	–	GND	GND	–	GND
J63	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
J64	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
J65	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
K3	SYS_VIN_HV	–	System Voltage Input - High	Main High Voltage DC Input	Input	Power: 9V to 20V
K4	GND	–	GND	GND	–	GND
K5	I2C1_CLK	GEN1_I2C_SCL	General I2C 1 Clock	ID EEPROM	Bidir	Open-Drain – 1.8V
K6	RGMII_RD1	EQOS_RD1	Ethernet Receive data bit 1	Ethernet PHY	Input	CMOS – 1.8V
K7	RGMII_TX_CTL	EQOS_TX_CTL	Ethernet Transmit Control	Ethernet PHY	Output	CMOS – 1.8V
K8	GND	–	GND	GND	–	GND
K9	PEX_L3_RST_N	PEX_L3_RST_N	PCIe 3 Reset	M.2 Key E Connector	Output	CMOS – 1.8V
K10	RSVD	–	–	–	–	–
K11	GND	–	GND	GND	–	GND
K12	UPHY_TX10_N	PEX_TX10_N	UPHY Transmit 10-	Micro SD / UFS Card Socket	Output	UFS Diff Pair
K13	UPHY_TX10_P	PEX_TX10_P	UPHY Transmit 10+	Micro SD / UFS Card Socket	Output	UFS Diff Pair
K14	GND	–	GND	GND	–	GND
K15	GND	–	GND	GND	–	GND
K16	UPHY_TX6_N	PEX_TX6_N	UPHY Transmit 6-	USB Type C Alt Mode Switch (for J8)	Output	USB3 Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
K17	UPHY_TX6_P	PEX_TX6_P	UPHY Transmit 6+	USB Type C Alt Mode Switch (for J8)	Output	
K18	GND	–	GND	GND	–	GND
K19	GND	–	GND	GND	–	GND
K20	UPHY_TX2_N	PEX_TX2_N	UPHY Transmit 2-	M.2 Key M Connector	Output	PCIe Diff Pair, TX AC Coupled on carrier board. RX AC Coupled on carrier board if direct connect to device.
K21	UPHY_TX2_P	PEX_TX2_P	UPHY Transmit 2+	M.2 Key M Connector	Output	
K22	GND	–	GND	GND	–	GND
K23	GND	–	GND	GND	–	GND
K24	NVHS0_TX1_N	NVHS0_TX1_N	NVHS/PCIe/SLVS 0 Transmit 1-	PCIe x16 Connector	Output	PCIe Diff Pair, AC-Coupled on carrier board
K25	NVHS0_TX1_P	NVHS0_TX1_P	NVHS/PCIe/SLVS 0 Transmit 1+	PCIe x16 Connector	Output	
K26	GND	–	GND	GND	–	GND
K27	GND	–	GND	GND	–	GND
K28	NVHS0_TX5_N	NVHS0_TX5_N	NVHS/PCIe/SLVS 0 Transmit 5-	PCIe x16 Connector	Output	PCIe Diff Pair, AC-Coupled on carrier board
K29	NVHS0_TX5_P	NVHS0_TX5_P	NVHS/PCIe/SLVS 0 Transmit 5+	PCIe x16 Connector	Output	
K30	GND	–	GND	GND	–	GND
K31	GND	–	GND	GND	–	GND
K32	RSVD	–	–	–	–	–
K33	RSVD	–	–	–	–	–
K34	GND	–	GND	GND	–	GND
K35	GND	–	GND	GND	–	GND

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
K36	RSVD	–	–	–	–	–
K37	RSVD	–	–	–	–	–
K38	GND	–	GND	GND	–	GND
K39	GND	–	GND	GND	–	GND
K40	MID0	–	Module ID #0	–	–	–
K41	GND	–	GND	GND	–	GND
K42	GND	–	GND	GND	–	GND
K43	CSI6_D0_N	CSI_G_D0_N	Camera, CSI_6 Data 0–	Camera Connector	Input	MIPI D-PHY/C-PHY
K44	CSI6_D0_P	CSI_G_D0_P	Camera, CSI_6 Data 0+	Camera Connector	Input	MIPI D-PHY/C-PHY
K45	GND	–	GND	GND	–	GND
K46	HDMI_DP0_TX3_P	HDMI_DP0_TXDP3	DisplayPort 0 Lane 3+ or HDMI Clk Lane+	USB Type C Conn. J7 (via Alt Mode Switch)	Output	Diff pair, AC-Coupled on carrier board
K47	HDMI_DP0_TX3_N	HDMI_DP0_TXDN3	DisplayPort 0 Lane 3– or HDMI Clk Lane–	USB Type C Conn. J7 (via Alt Mode Switch)	Output	
K48	GND	–	GND	GND	–	GND
K49	GPIO25	SOC_GPIO50	GPIO	Camera Connector (VDD_SYS_EN)	Output	CMOS – 1.8V
K50	DP2_HPD	DP_AUX_CH2_HPD	Display Port/HDMI 2 Hot Plug Detect	HDMI Connector	Input	CMOS – 1.8V
K51	DP1_HPD	DP_AUX_CH1_HPD	Display Port/HDMI 1 Hot Plug Detect	USB Type C Conn. J8 (via Alt Mode Switch)	Input	CMOS – 1.8V
K52	DP0_HPD	DP_AUX_CH0_HPD	Display Port/HDMI 0 Hot Plug Detect	USB Type C Conn. J7 (via Alt Mode Switch)	Input	CMOS – 1.8V
K53	UART1_TX	UART1_TX	UART 1 Transmit	Expansion Connector via level shifter	Bidir	CMOS – 1.8V
K54	UART1_RX	UART1_RX	UART 1 Receive	Expansion Connector via level shifter	Bidir	CMOS – 1.8V
K55	GND	–	GND	GND	–	GND
K56	GPIO19	SOC_GPIO43	GPIO	PCIe x16 Connector (SLVS VSYNC)	Bidir	CMOS – 1.8V
K57	PWM01	SOC_GPIO44		Expansion Connector (PWM 1)	Output	CMOS – 1.8V
K58	UART5_RTS	UART5_RTS	UART 5 Request to Send	M.2 Key E Connector	Bidir	CMOS – 1.8V
K59	I2S3_DOUT	DAP4_DOUT	I2S Audio Port 3 Data Out	M.2 Key E	Output	CMOS – 3.3V
K60	UART3_RX_DEBUG	UART3_RX	Debug UART Receive	UART-USB (MicroB) Bridge	Input	CMOS – 1.8V
K61	I2C2_DAT	GEN2_I2C_SDA	General I2C 2 Data	Various	Bidir	Open-Drain – 1.8V
K62	FAN_PWM	TOUCH_CLK	Fan Pulse Width Modulation signal	Fan Circuit/Connector	Output	CMOS – 1.8V
K63	GND	–	GND	GND	–	GND
L3	GND	–	GND	GND	–	GND
L4	UART4_RTS	UART4_RTS	GPIO	Not used	Bidir	CMOS – 1.8V
L5	UART4_TX	UART4_TX	GPIO	Camera Conn. (CAM0_RST)	Output	CMOS – 1.8V
L6	GPIO02	SOC_GPIO11	GPIO	SD Card socket (SD Detect)	Bidir	CMOS – 1.8V
L7	GND	–	GND	GND	–	GND
L8	I2C1_DAT	GEN1_I2C_SDA	General I2C 1 Data	ID EEPROM	Bidir	Open-Drain – 1.8V
L9	GPIO28	SOC_GPIO02	GPIO	Not Used	Input	CMOS – 1.8V
L10	FORCE_RECOVERY_N	SOC_GPIO00	Force Recovery strap pin	System	Input	CMOS – 1.8V
L11	STANDBY_REQ_N	SOC_GPIO01	Standby Request	System	Input	CMOS – 1.8V
L12	GND	–	GND	GND	–	GND
L13	GND	–	GND	GND	–	GND
L14	I2S1_CLK	DAP1_SCLK	I2S Audio Port 1 Clock	Audio Codec	Bidir	CMOS – 1.8V
L15	GPIO14	DAP3_FS	GPIO	M.2 Key E Connector (M2 Enable)	Bidir	CMOS – 1.8V
L16	GND	–	GND	GND	–	GND
L17	GND	–	GND	GND	–	GND
L18	RSVD	–	–	–	–	–
L19	RSVD	–	–	–	–	–
L20	GND	–	GND	GND	–	GND
L21	GND	–	GND	GND	–	GND
L22	SYS_VIN_MV_10	–	System Voltage Input - Medium	Main Medium Voltage DC Input	Input	Power: 5.0V
L23	SYS_VIN_MV_9	–	System Voltage Input - Medium	Main Medium Voltage DC Input	Input	Power: 5.0V
L24	GND	–	GND	GND	–	GND
L25	GND	–	GND	GND	–	GND
L26	SYS_VIN_MV_8	–	System Voltage Input - Medium	Main Medium Voltage DC Input	Input	Power: 5.0V

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
L27	SYS_VIN_MV_7	–	System Voltage Input - Medium	Main Medium Voltage DC Input	Input	Power: 5.0V
L28	GND	–	GND	GND	–	GND
L29	GND	–	GND	GND	–	GND
L30	SYS_VIN_MV_6	–	System Voltage Input - Medium	Main Medium Voltage DC Input	Input	Power: 5.0V
L31	SYS_VIN_MV_5	–	System Voltage Input - Medium	Main Medium Voltage DC Input	Input	Power: 5.0V
L32	GND	–	GND	GND	–	GND
L33	GND	–	GND	GND	–	GND
L34	SYS_VIN_MV_4	–	System Voltage Input - Medium	Main Medium Voltage DC Input	Input	Power: 5.0V
L35	SYS_VIN_MV_3	–	System Voltage Input - Medium	Main Medium Voltage DC Input	Input	Power: 5.0V
L36	GND	–	GND	GND	–	GND
L37	GND	–	GND	GND	–	GND
L38	SYS_VIN_MV_2	–	System Voltage Input - Medium	Main Medium Voltage DC Input	Input	Power: 5.0V
L39	SYS_VIN_MV_1	–	System Voltage Input - Medium	Main Medium Voltage DC Input	Input	Power: 5.0V
L40	GND	–	GND	GND	–	GND
L41	RSVD	–	–	–	–	–
L42	RSVD	–	–	–	–	–
L43	GND	–	GND	GND	–	GND
L44	RSVD	–	–	–	–	–
L45	RSVD	–	–	–	–	–
L46	GND	–	GND	GND	–	GND
L47	RSVD	–	–	–	–	–
L48	UART4	–	Reserved – Must be pulled to GND through 10kΩ resistor	–	–	–
L49	UART4_CTS	UART4_CTS	GPIO	Camera Connector (Camera 0 Powerdown)	Output	CMOS – 1.8V
L50	GPIO35	SOC_GPIO12	GPIO	40-pin Header (PWM3)	Output	CMOS – 1.8V
L51	UART1_RTS	UART1_RTS	UART 1 Request to Send	Expansion Connector via level shifter	Bidir	CMOS – 1.8V
L52	OVERTEMP_N	SOC_GPIO55	Force Power Off Request	System	Output	CMOS – 1.8V
L53	VCC_RTC	–	Real-Time-Clock. Optionally used to provide back-up power for RTC. Connects to Lithium Cell or super capacitor on Carrier Board. PMIC is supply when charging cap or coin cell. Super cap or coin cell is source when system is disconnected from power.	Battery Back-up using Super-capacitor	Bidir	Power: 1.65V-5.5V
L54	MODULE_POWER_ON	–	Module Power On	System	Input	Open-drain – 5.0V or CMOS – 3.3V
L55	VDDIN_PWR_BAD_N	–	VDD_IN Power Bad. Carrier board indication to the module that the VDD_IN power is not valid. Carrier board should de-assert this (drive high) only when SYS_VIN_HV/MV have reached the required voltage levels and are stable. This prevents SoC from powering up until the main input supply voltages are stable.	System	Input	Open-drain – 5.0V
L56	TEMP_ALERT_N	–	–	–	–	–
L57	MCLK05	SOC_GPIO42	Peripheral Master Clock	–	Output	CMOS – 1.8V
L58	PERIPHERAL_RESET_N	–	Peripheral Reset. Driven from carrier board to force reset of SoC & eMMC & QSPI (not PMIC).	Not used	Input	CMOS – 1.8V
L59	RSVD	–	–	–	–	–
L60	SYS_RESET_N	SYS_RESET_N	System Reset: Connected to NRST_IO of PMIC. Bidirectional reset driven from PMIC to carrier board for devices requiring full system reset. Can also be driven from carrier board to module to initiate full system reset (including	System	Output	CMOS – 1.8V

Pin #	Jetson Xavier Pin Name	SoC Signal	Usage/Description	Usage on the Nvidia Carrier Board	Direction	Pin Type
			PMIC) (i.e. From RESET button). A pull-up is present on module.			
L61	POWER_BTN_N	POWER_ON	Used to enter/exit SC7 (sleep).	System	Input	CMOS – 1.8V
L62	CARRIER_POWER_ON	–	Carrier Power On. Used as part of the power up sequence. When asserted, it is safe for the carrier board to power up.	System	Output	Pulled to 3.3V on module
L63	PRSNT1	–		Connected to Power Switch	–	–

Legend	Ground	Power	Reserved – Must be left unconnected unless otherwise directed.

Notes:

1. The Usage/Description column uses the Jetson Xavier port/lane/interface references.
2. In the Type/Dir column, Output is from Jetson Xavier. Input is to Jetson Xavier. Bidir is for Bidirectional signals.
3. These pins are handled as Open-Drain on the carrier board

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