

LongBeach 100

LA-2451 REV 0.4 Schematic

Desktop LGA-775 Package

RXC400M(RU400M)+SB400+ATI M22P/M24P(64/128MB VRAM)

2004-11-08<A>

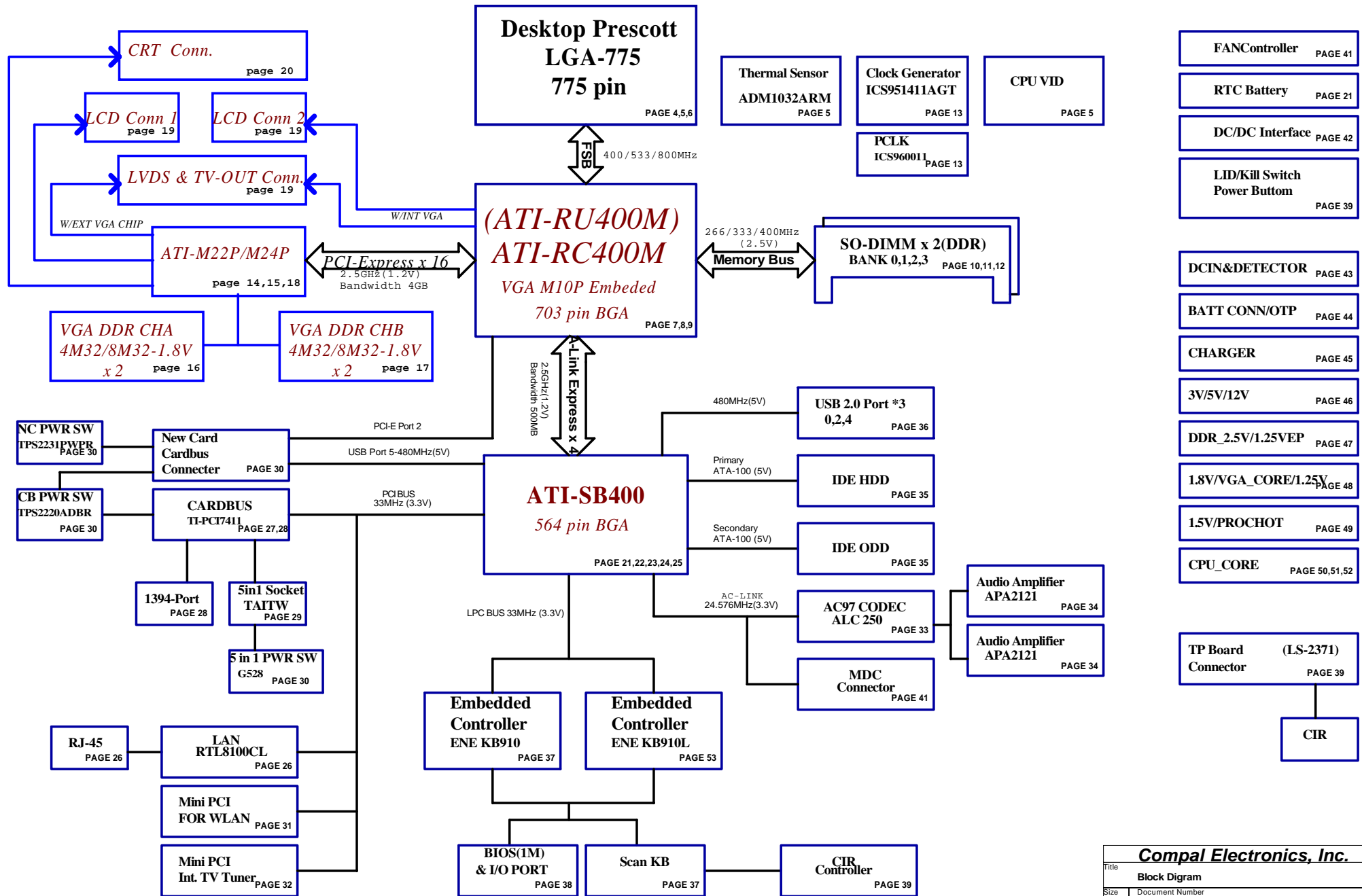
Compal Electronics, Inc.

Title		
Cover Page		
Size	Document Number	Rev
Custom		0.1
Date:	星期一, 十一月 08, 2004	Sheet 1 of 53

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EAQ11 LA-2451

FUNCTION BLOCK DIAGRAM



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPUVID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VGA_CORE	1.0V/1.2V switched power rail for VGA chip	ON	OFF	OFF
+1.2VS	1.2VS for PCI-Express	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 8X	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(PCI7411)	AD20	2	PIRQE/PIRQF/PIRQG/PIRQH
LAN	AD22	1	PIRQG/PIRQC
Mini-PCI(WLAN)	AD18	3	PIRQF:PIRQG/PIRQC:PIRQD
Mini-PCI(TV-Tuner)	AD23	4	PIRQH:PIRQE/PIRQD:PIRQA

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02) (24C04)	1010 000X b 1011 000Xb	ICS960011	1101 110X b

EC SM Bus2 address

SB400 SM Bus address

Device	Address
Clock Generator (ICS951411BGLFT)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 001Xb

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

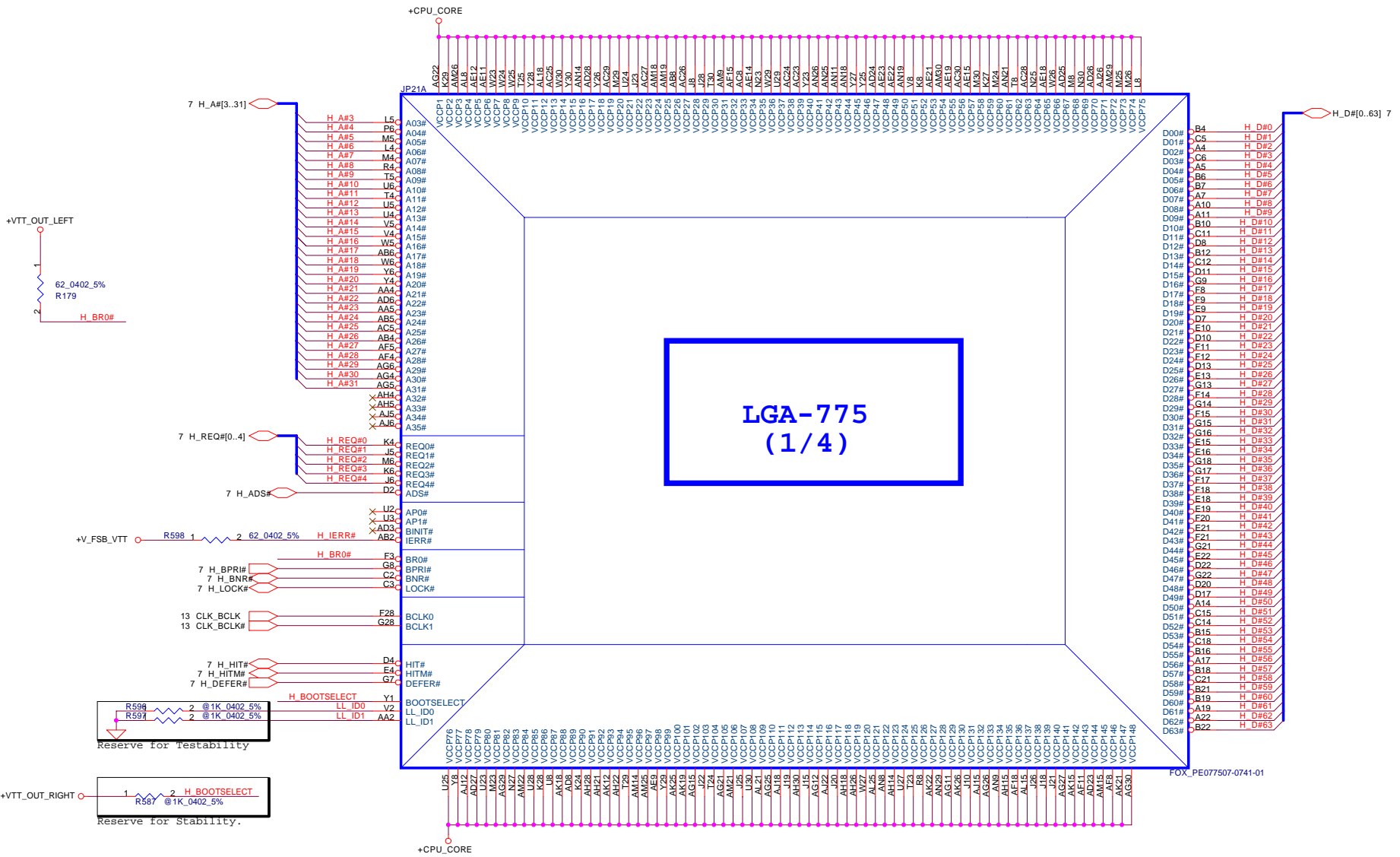
Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

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Title		Notes	
Size	Document Number	Rev	
Custom	Longbeach 100 <LA-2451>	0.1	
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LGA-775
(1/4)

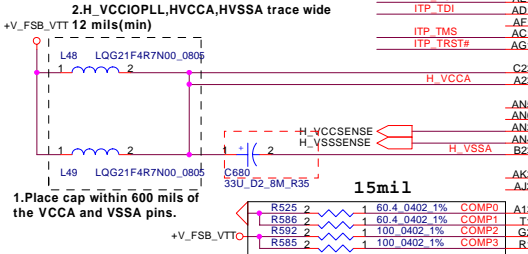
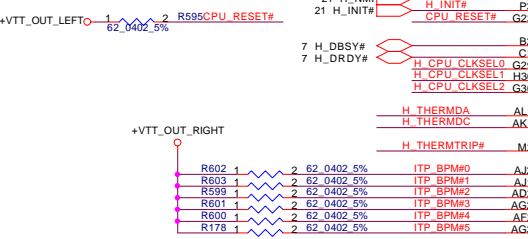
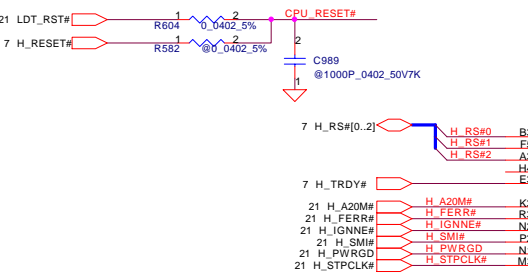
In Intel CPU datasheet:
LL_ID[1:0], VTT_SEL, GTLREF_SEL and VID_SELECT are signals that are implement on the processor package.
That is they are either connected directly to Vss or open lands.

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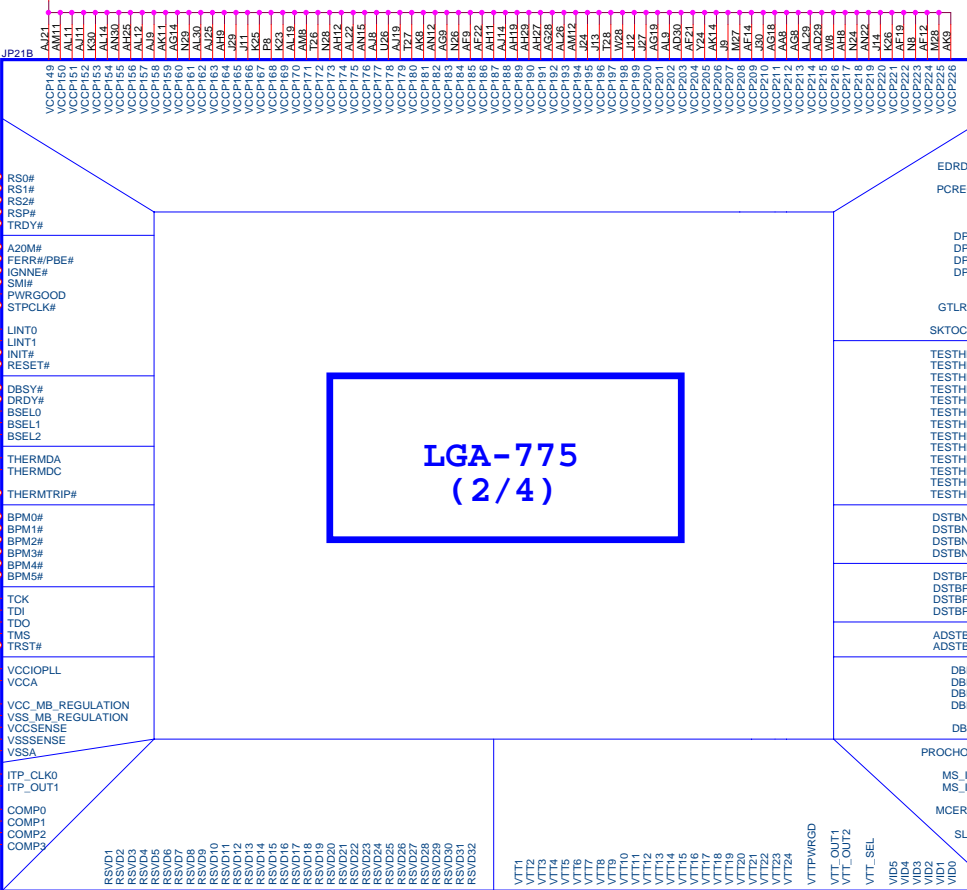
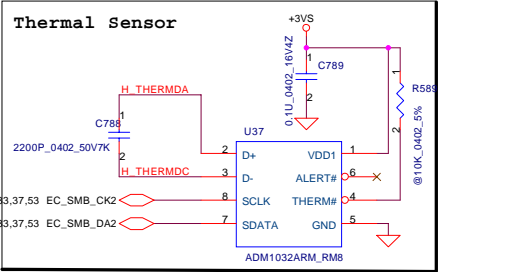
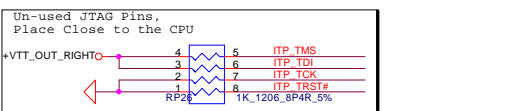
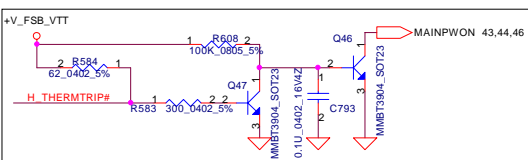
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Title	LGA-775(1/3)	
Size	Document Number	Rev
Customer	Longbeach 100 <LA-2451>	0.1
Date:	星期六, 十二月 06, 2004	Sheet 4 of 53

+CPU_CORE

GTLREF Voltage should be 0.63*VTT=0.75V

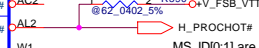
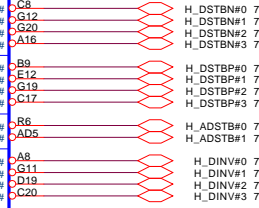
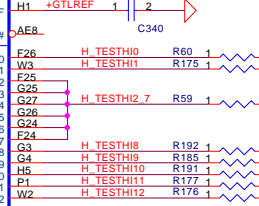
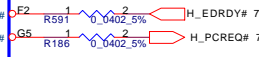


Note: Please change to 10uH, DC current of 120mA parts and close to cap DC Voltage drop from VTT to VCCA should be < 70mV

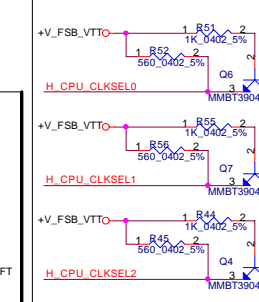
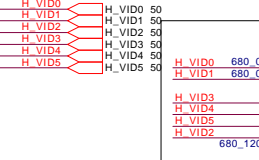
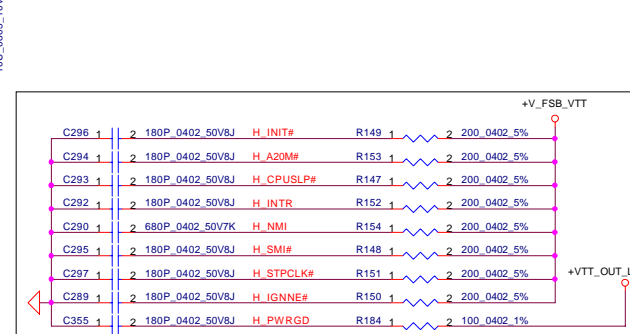
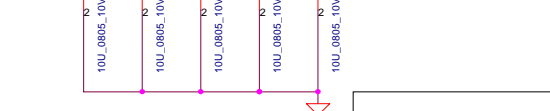
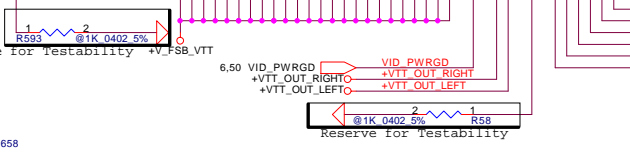
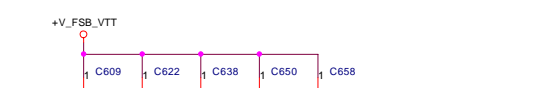
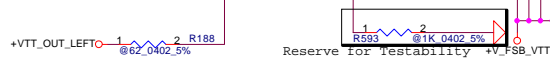


LGA-775 (2/4)

EDRDY#_H_PCREQ# is not a feature of the Pentium 4 processor in the 775-land package.



MS_ID[0:1] are provided to indicate the Market Segment for the processor and may be used for future processor compatibility.



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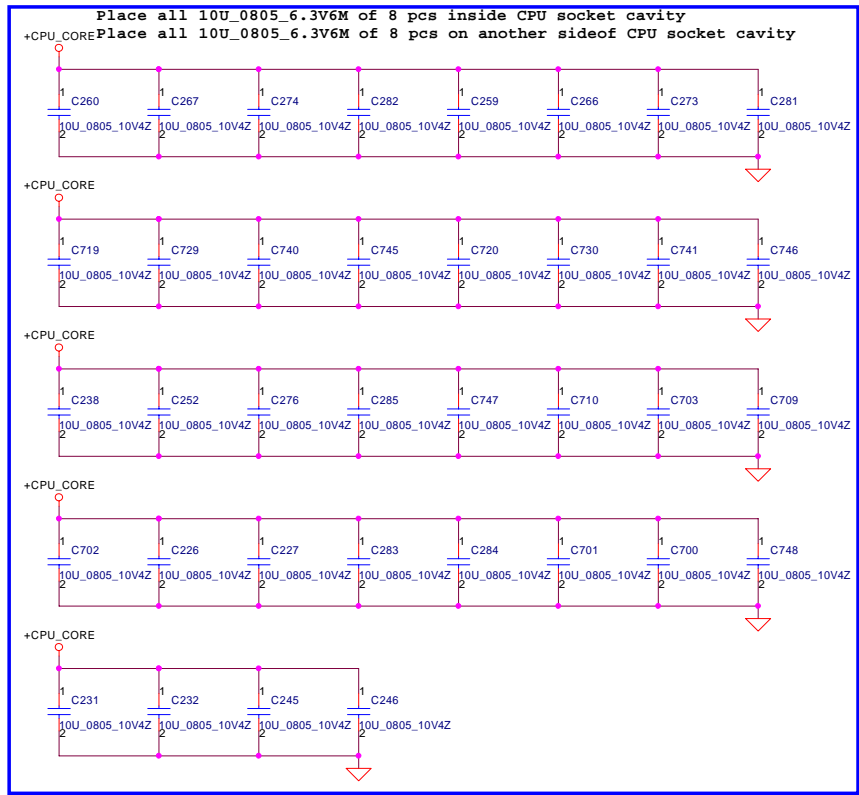
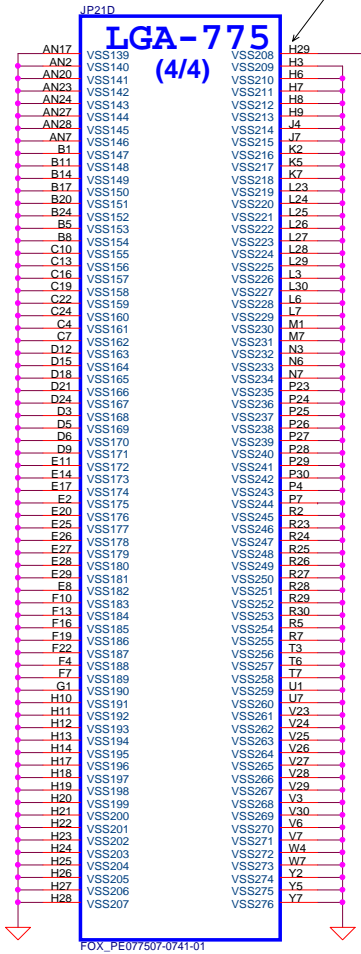
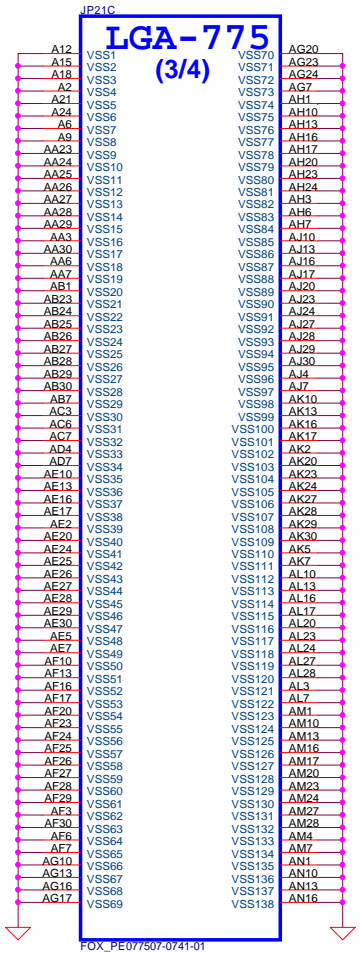
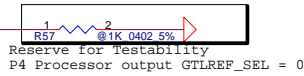
LGA-775(2/3)

Size: Document Number Longbeach 100 <LA-2451>

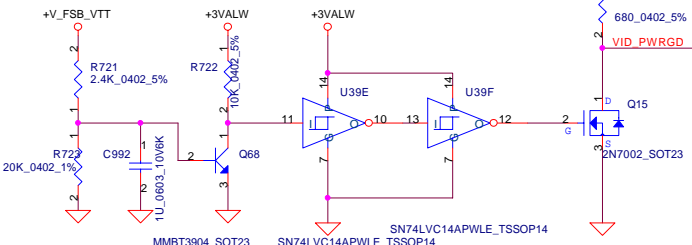
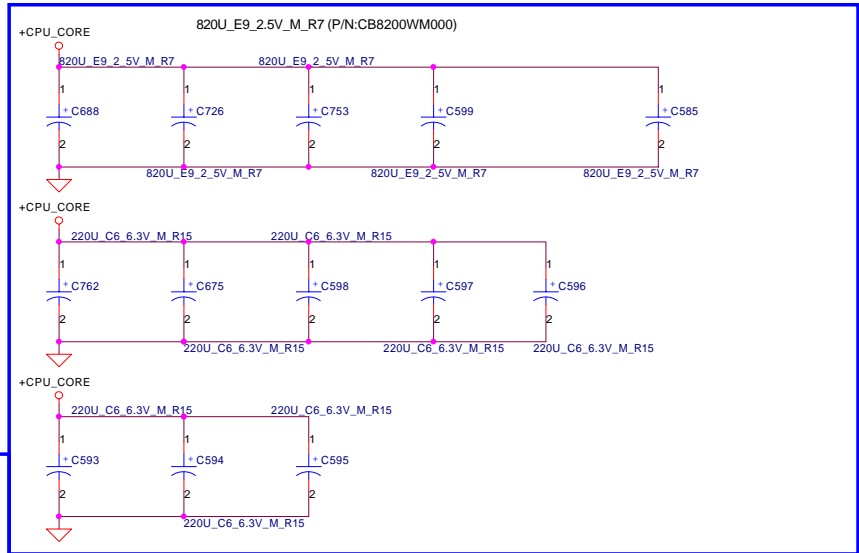
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H29 This pin in CPU is GTLREF_SEL, but not VSS.

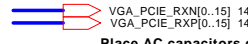
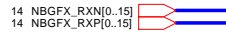
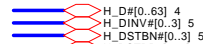
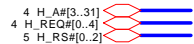


SANYO OS-CON 820uF_ERS7m ohm* 6
SANYO OS-CON 220uF_ERS13m ohm* 8

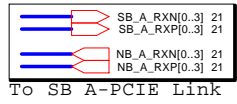
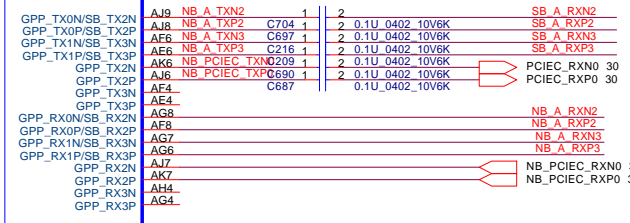
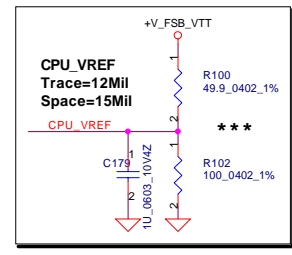
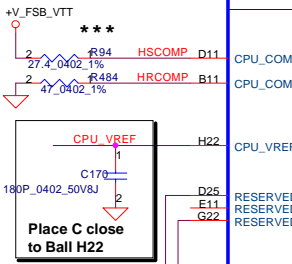
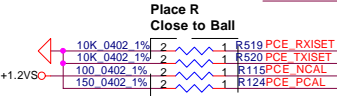
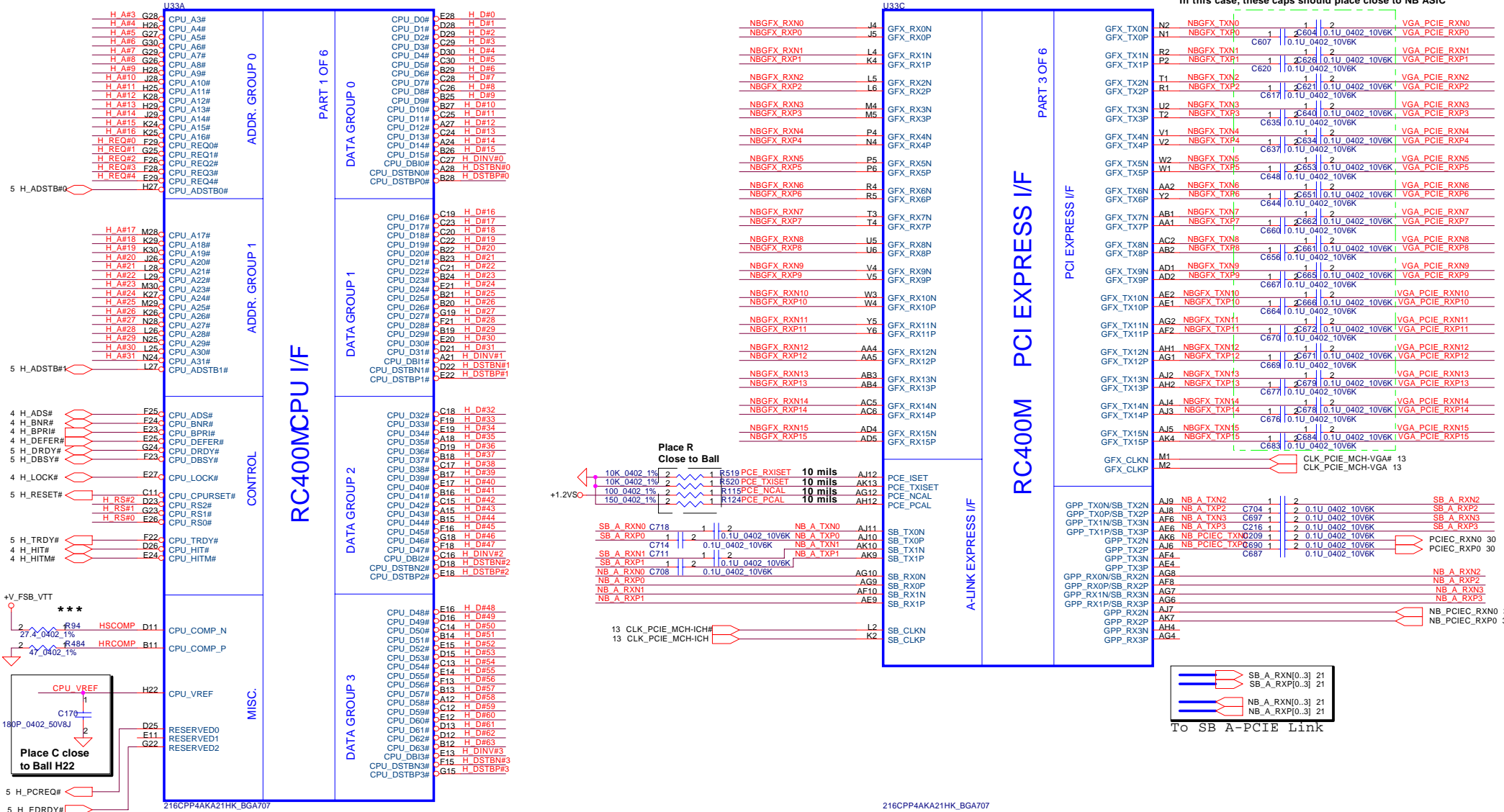


Decoupling Reference Document:
Grantsdale Chipset Platform Design guide Rev1.2 (15434) Page263

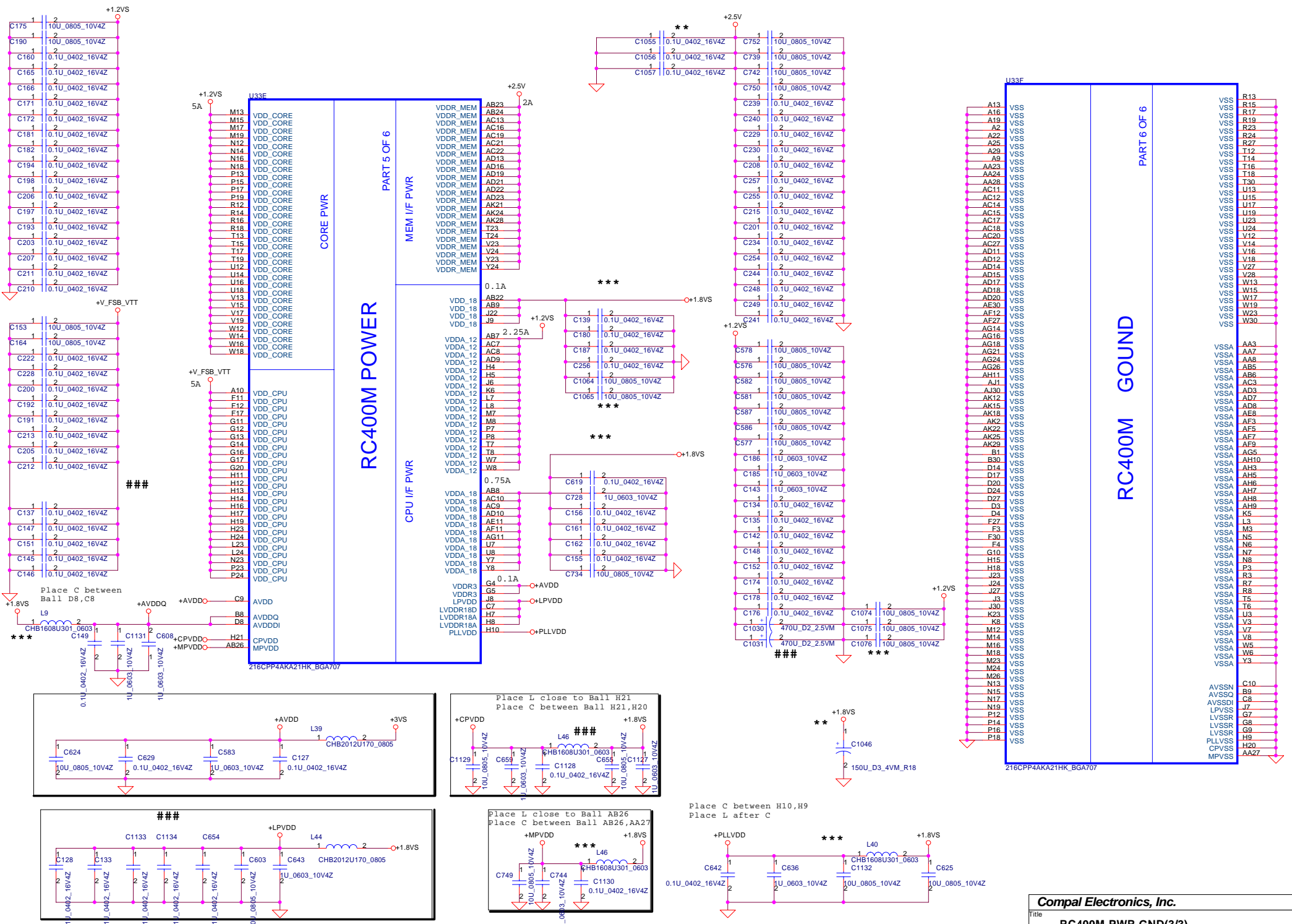
Decoupling Reference Requirement:
560uF Polymer, ESR:6m ohm(each) * 10
22uF X5R * 8
10uF X5R * 10



Place AC capacitors close to transmitter
In this case, these caps should place close to NB ASIC



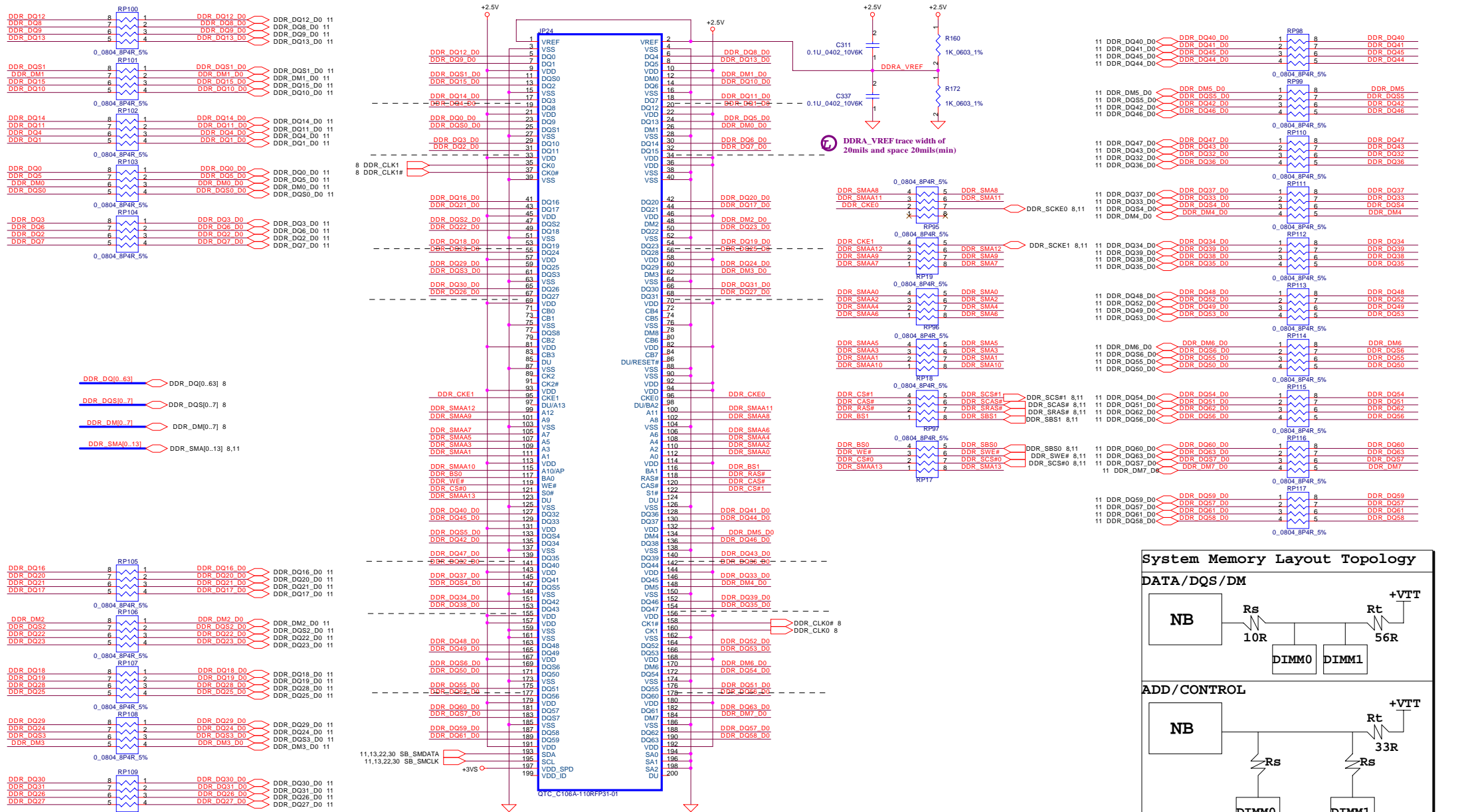
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RC400M POWER
PART 5 OF 6
PART 6 OF 6

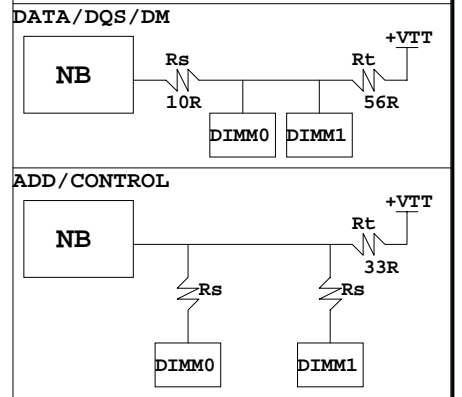
RC400M GROUND
PART 6 OF 6

Compal Electronics, Inc.
 Title: **RC400M-PWR,GND(3/3)**
 Size: Document Number
 Customer: **Longbeach 100 <LA-2451>**
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Layout note
Place Add/Command resistors
Close to Pin, max L = 300 mils

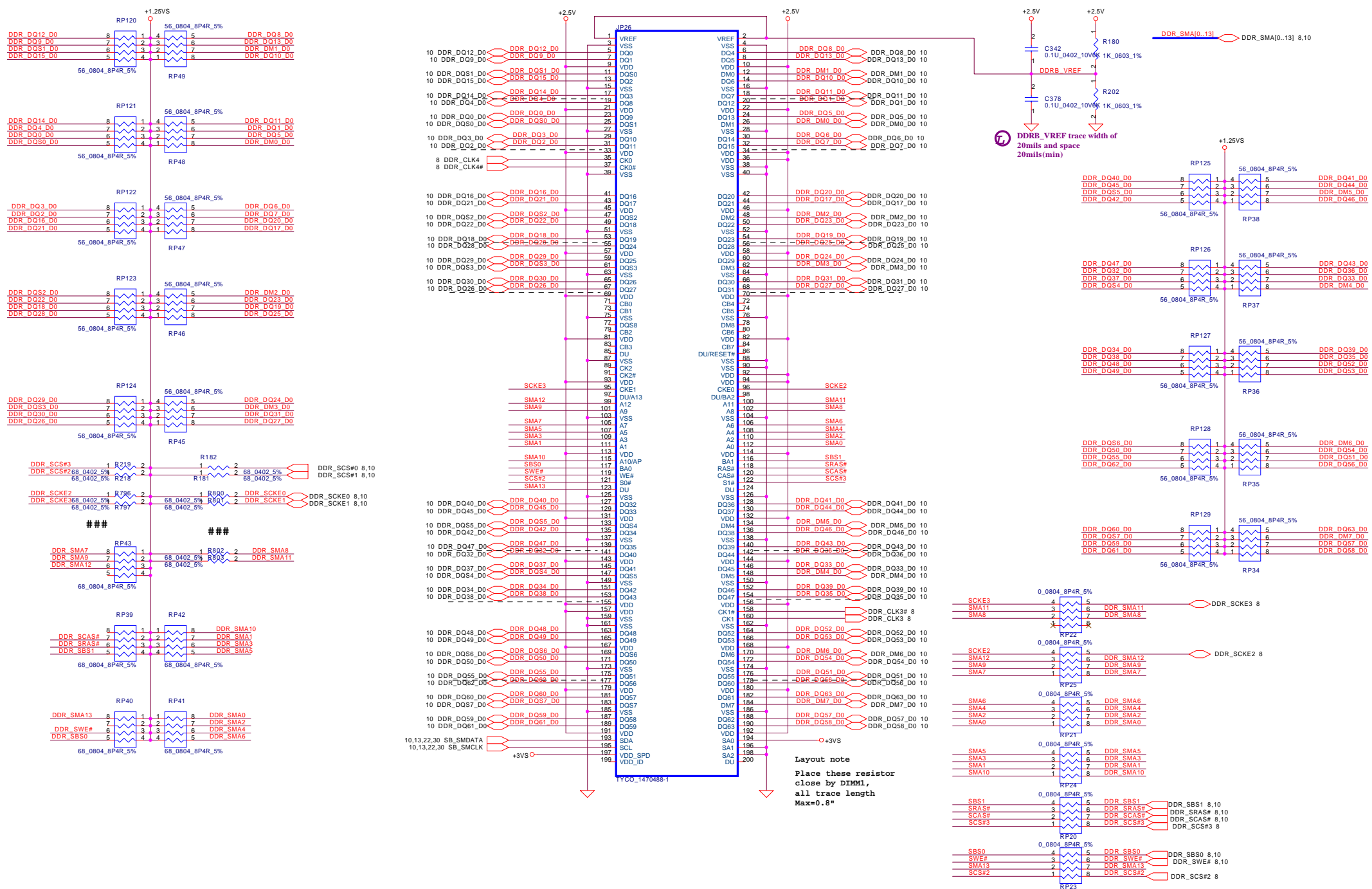
System Memory Layout Topology



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Title: DDR-SODIMMSLOT0

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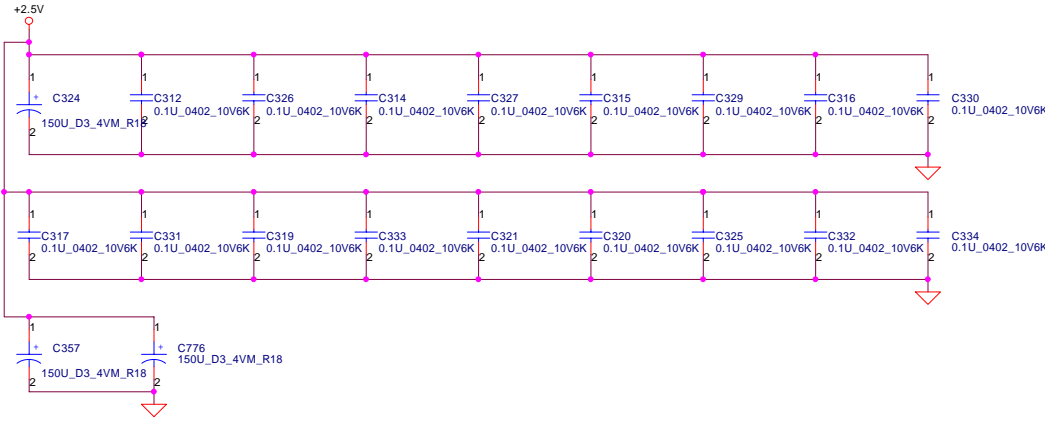


Layout note
Place these resistor
close by DIMM1,
all trace length
Max=0.8"

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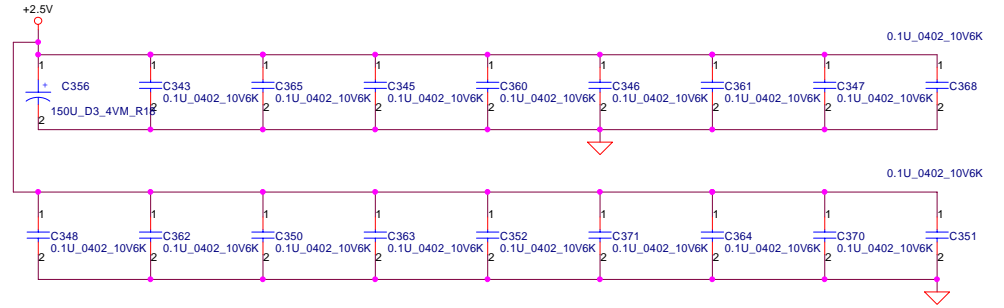
Layout note :

Distribute as close as possible to DDR-SODIMM0.



Layout note :

Distribute as close as possible to DDR-SODIMM1.

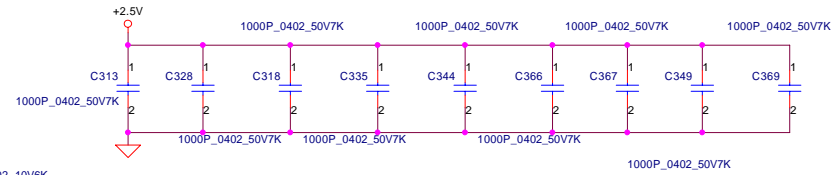


Layout note :

Place one cap close to every 2 pull up resistors termination to +1.25VS



Layout note :
for EMI solution

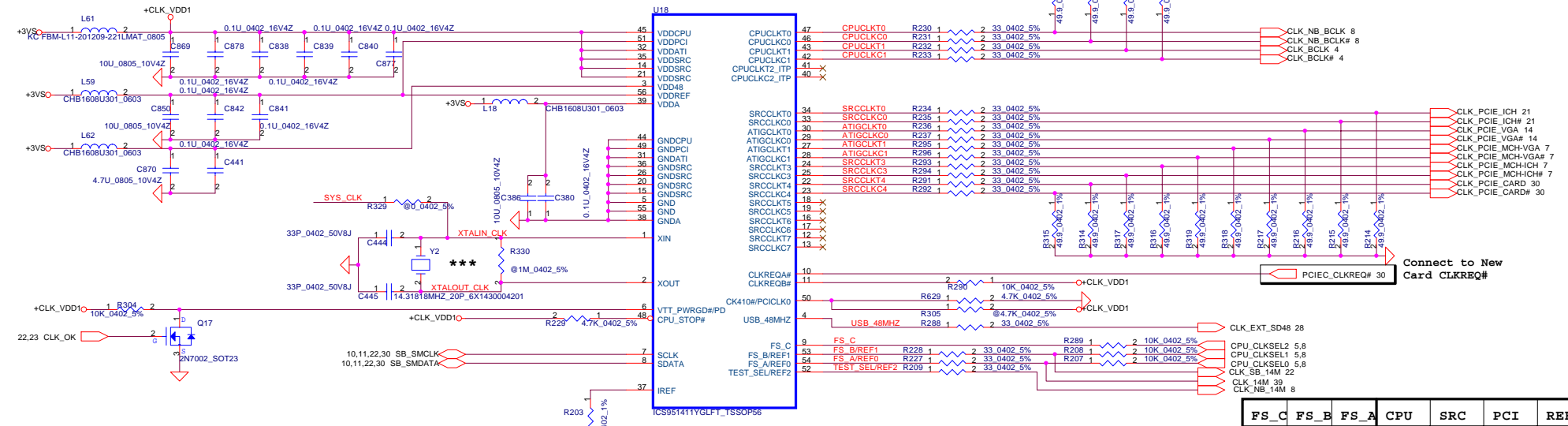


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DDR SODIMM Decoupling		
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Clock Generator

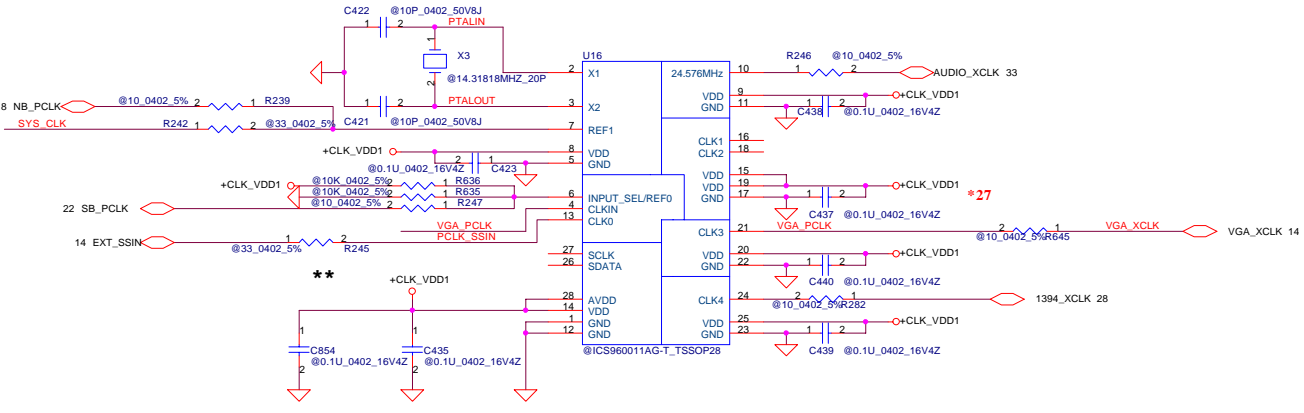
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO CLOCK GEN AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBCLK/#, ITPCLK/# AND SCR/# ,AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN



ICS951411 AND CY28RS400 ARE FULLY PIN COMPATIBLE AND CAN BE INTERCHANGED WITHOUT ANY HARDWARE MODIFICATION.

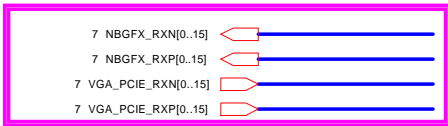
FS_C	FS_B	FS_A	CPU	SRC	PCI	REF	USB
0	0	0	266.66	100.00	33.33	14.318	48.000
		1	133.33	100.00	33.33	14.318	48.000
	1	0	200.00	100.00	33.33	14.318	48.000
1	0	1	166.66	100.00	33.33	14.318	48.000
	1	0	100.00	100.00	33.33	14.318	48.000
		1	400.00	100.00	33.33	14.318	48.000
						RESERVED	14.318 48.000

CLOCK OF IC



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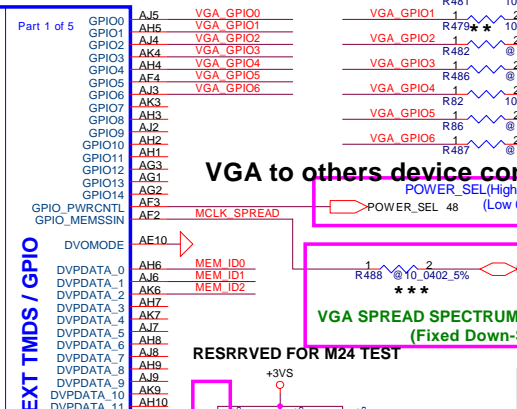
VGA to others device connection



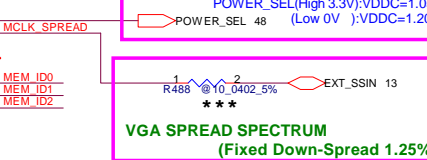
Place AC capacitors close to transmitter
In this case, these caps should place close to VGA ASIC

NBGFX_RXP15	1	2	VGA_PCIE_TXP15	AF26	PCIE_TX0P
NBGFX_RXN15	C58	0.1U_0402_10V6K	VGA_PCIE_TXN15	AE26	PCIE_TX0N
NBGFX_RXP14	C51	0.1U_0402_10V6K	VGA_PCIE_TXP14	AC25	PCIE_TX1P
NBGFX_RXN14	C51	0.1U_0402_10V6K	VGA_PCIE_TXN14	AE25	PCIE_TX1N
NBGFX_RXP13	1	2	VGA_PCIE_TXP13	AC27	PCIE_TX1N
NBGFX_RXN13	C44	0.1U_0402_10V6K	VGA_PCIE_TXN13	AE27	PCIE_TX1P
NBGFX_RXP12	1	2	VGA_PCIE_TXP12	AC26	PCIE_TX2P
NBGFX_RXN12	C46	0.1U_0402_10V6K	VGA_PCIE_TXN12	AE26	PCIE_TX2N
NBGFX_RXP11	1	2	VGA_PCIE_TXP11	Y25	PCIE_TX3P
NBGFX_RXN11	C15	0.1U_0402_10V6K	VGA_PCIE_TXN11	W25	PCIE_TX3N
NBGFX_RXP10	1	2	VGA_PCIE_TXP10	Y27	PCIE_TX4P
NBGFX_RXN10	C17	0.1U_0402_10V6K	VGA_PCIE_TXN10	W27	PCIE_TX4N
NBGFX_RXP9	1	2	VGA_PCIE_TXP9	Y26	PCIE_TX5P
NBGFX_RXN9	C19	0.1U_0402_10V6K	VGA_PCIE_TXN9	W26	PCIE_TX5N
NBGFX_RXP8	1	2	VGA_PCIE_TXP8	U25	PCIE_TX6P
NBGFX_RXN8	C21	0.1U_0402_10V6K	VGA_PCIE_TXN8	T25	PCIE_TX6N
NBGFX_RXP7	1	2	VGA_PCIE_TXP7	U27	PCIE_TX7P
NBGFX_RXN7	C23	0.1U_0402_10V6K	VGA_PCIE_TXN7	T27	PCIE_TX7N
NBGFX_RXP6	1	2	VGA_PCIE_TXP6	U26	PCIE_TX8P
NBGFX_RXN6	C25	0.1U_0402_10V6K	VGA_PCIE_TXN6	T26	PCIE_TX8N
NBGFX_RXP5	1	2	VGA_PCIE_TXP5	P25	PCIE_TX9P
NBGFX_RXN5	C27	0.1U_0402_10V6K	VGA_PCIE_TXN5	N25	PCIE_TX9N
NBGFX_RXP4	1	2	VGA_PCIE_TXP4	N26	PCIE_TX10P
NBGFX_RXN4	C29	0.1U_0402_10V6K	VGA_PCIE_TXN4	N27	PCIE_TX10N
NBGFX_RXP3	1	2	VGA_PCIE_TXP3	P26	PCIE_TX11P
NBGFX_RXN3	C31	0.1U_0402_10V6K	VGA_PCIE_TXN3	N26	PCIE_TX11N
NBGFX_RXP2	1	2	VGA_PCIE_TXP2	N25	PCIE_TX12P
NBGFX_RXN2	C37	0.1U_0402_10V6K	VGA_PCIE_TXN2	K25	PCIE_TX12N
NBGFX_RXP1	1	2	VGA_PCIE_TXP1	L27	PCIE_TX13P
NBGFX_RXN1	C35	0.1U_0402_10V6K	VGA_PCIE_TXN1	K27	PCIE_TX13N
NBGFX_RXP0	1	2	VGA_PCIE_TXP0	L26	PCIE_TX14P
NBGFX_RXN0	C33	0.1U_0402_10V6K	VGA_PCIE_TXN0	K26	PCIE_TX14N
					PCIE_TX15N

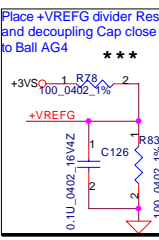
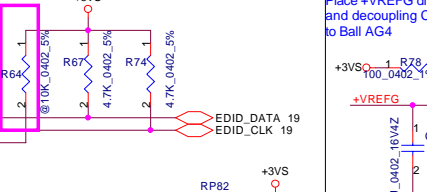
VGA_PCIE_RXP15	AH30	PCIE_RX0P
VGA_PCIE_RXN15	AG30	PCIE_RX0N
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VGA_PCIE_RXN14	AE29	PCIE_RX1N
VGA_PCIE_RXP13	AE28	PCIE_RX2P
VGA_PCIE_RXN13	AE30	PCIE_RX2N
VGA_PCIE_RXP12	AD30	PCIE_RX3P
VGA_PCIE_RXN12	AD29	PCIE_RX3N
VGA_PCIE_RXP11	AC29	PCIE_RX4P
VGA_PCIE_RXN11	AB29	PCIE_RX4N
VGA_PCIE_RXP10	AB30	PCIE_RX5P
VGA_PCIE_RXN10	AA30	PCIE_RX5N
VGA_PCIE_RXP9	AA29	PCIE_RX6P
VGA_PCIE_RXN9	W29	PCIE_RX6N
VGA_PCIE_RXP8	W30	PCIE_RX7N
VGA_PCIE_RXN8	W30	PCIE_RX8P
VGA_PCIE_RXP7	V30	PCIE_RX8P
VGA_PCIE_RXN7	V29	PCIE_RX8N
VGA_PCIE_RXN6	U29	PCIE_RX9P
VGA_PCIE_RXN5	T29	PCIE_RX9N
VGA_PCIE_RXN4	T30	PCIE_RX10P
VGA_PCIE_RXN3	R29	PCIE_RX10N
VGA_PCIE_RXN2	P29	PCIE_RX11P
VGA_PCIE_RXN1	P30	PCIE_RX11N
VGA_PCIE_RXN0	N30	PCIE_RX12P
VGA_PCIE_RXN0	M30	PCIE_RX12N
VGA_PCIE_RXN0	M30	PCIE_RX13P
VGA_PCIE_RXN0	L29	PCIE_RX13N
VGA_PCIE_RXN0	L29	PCIE_RX14P
VGA_PCIE_RXN0	K29	PCIE_RX14N
VGA_PCIE_RXN0	K30	PCIE_RX15P
VGA_PCIE_RXN0	J30	PCIE_RX15N



VGA to others device connection



RESRRVED FOR M24 TEST



General Strapping (VGA Internal PD) 0:Disable, 1:Enable		
GPIO0	Full Transmitter Output Swing Power	DEFAULT : 1
GPIO1	Transmitter De-emphasis Enable	DEFAULT : 1
GPIO(3:2)	00: PCI Express 1.0A mode 01: Kyrene-compatible mode 10: PCI Express 1.0 mode 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	DEFAULT : 00
GPIO4	Transmitter Extra Current PCI-E Lane Reversal Enable	DEFAULT : 1
GPIO5	Force chip to go to compliance state quickly for test purposes	DEFAULT : 0
GPIO6	Reduced PLL bandwidth	DEFAULT : 0

Vedio Memory Config. (VGA Internal PD)					
MEM_ID0	MEM_ID1		Size	Vendor	
0	0	Default	64MB	4Mx32	Samsung
0	1		64MB	4Mx32	Hynix
1	0		128MB	8Mx32	Samsung
1	1		128MB	8Mx32	Hynix

MEM_ID2	0	1
MEM Voltage	2.5V	1.8V

PCI EXPRESS

DVO / EXT TMS / GPIO

LVD5

TMDS

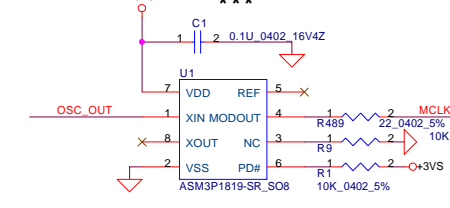
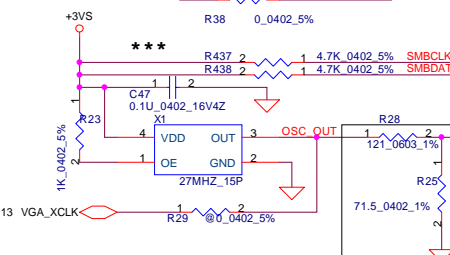
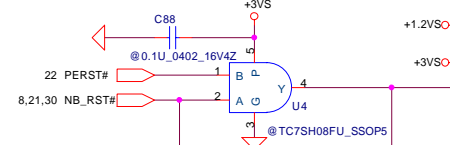
CLK SS DAC2

CLM SS DAC1

THERM DAC1

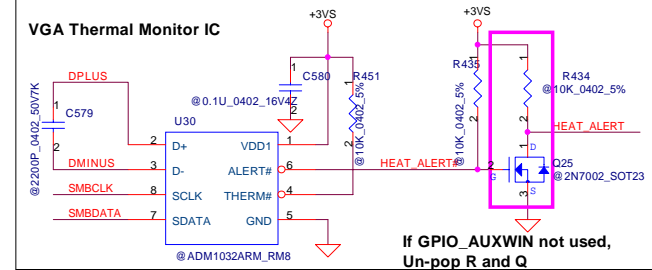
GPIO

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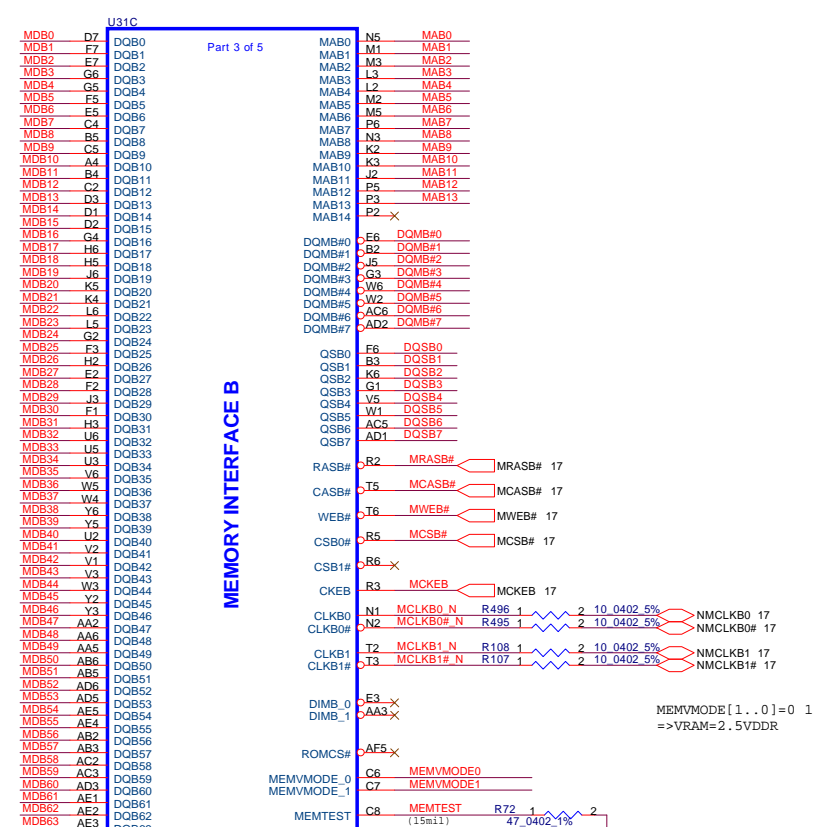
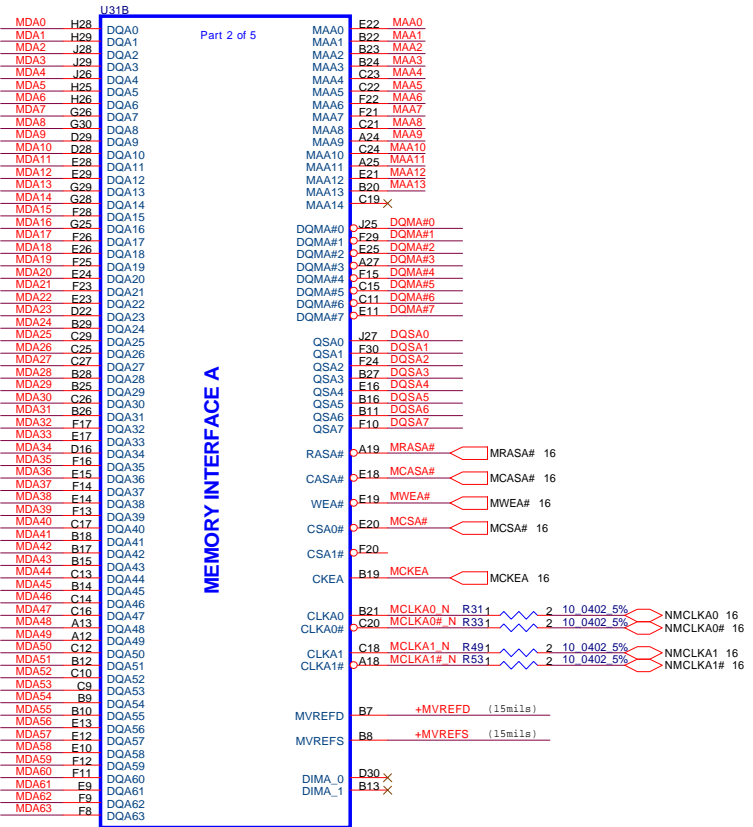
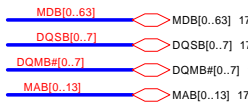
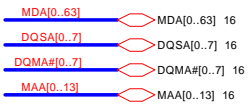


Voltage divider
Reduce Voltage from 3.3V to 1.2V

If GPIO_AUXWIN not used,
pulled it to GND.

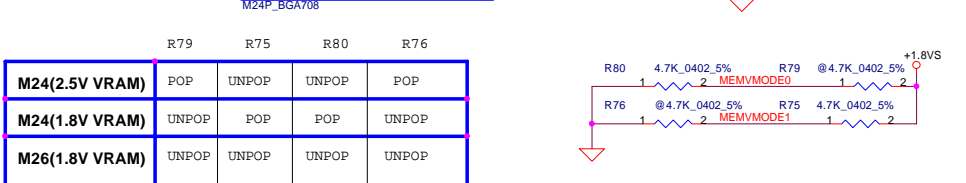
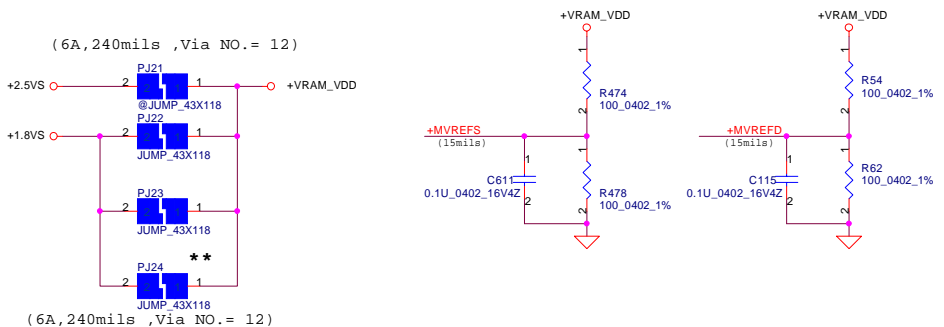


Compal Electronics, Inc.			
M24-P PCIE, DISP, GPIO			
Size	Document Number	Rev 0.1	
Customer	Longbeach 100 <LA-2451>		
Date:	星期六, 十一月 06, 2004	Sheet	14 of 53

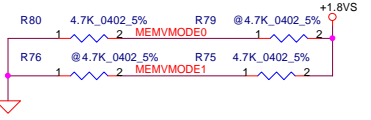


MEMORY INTERFACE A

MEMORY INTERFACE B



M24(2.5V VRAM)	POP	UNPOP	UNPOP	POP
M24(1.8V VRAM)	UNPOP	POP	POP	UNPOP
M26(1.8V VRAM)	UNPOP	UNPOP	UNPOP	UNPOP



For Uni-directional signals, series resistors should be placed close to the VGA ASIC.
Such as MDQMA[0..7], MAA[0..13], MRASA#, MCASA#, MWEA#, MCSA#[0..1]

For Bi-directional signals, series resistors should be placed close to the memory.
Such as MDA[0..63] and MDQSA[0..7]

For Uni-directional signals, series resistors should be placed close to the VGA ASIC.
Such as MDQMB[0..7], MAB[0..13], MRASB#, MCASB#, MWEB#, MCSB#[0..1]

For Bi-directional signals, series resistors should be placed close to the memory.
Such as MDB[0..63] and MDQSB[0..7]

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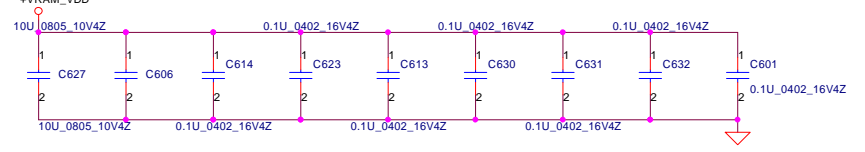
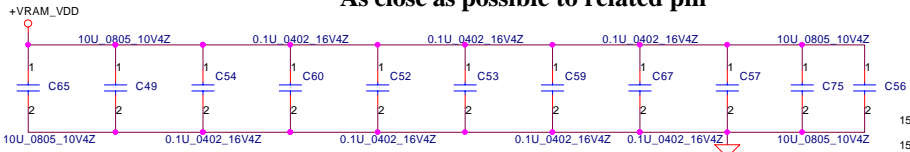
Compal Electronics, Inc.

Title: **M24-P VRAM INTERFACE**

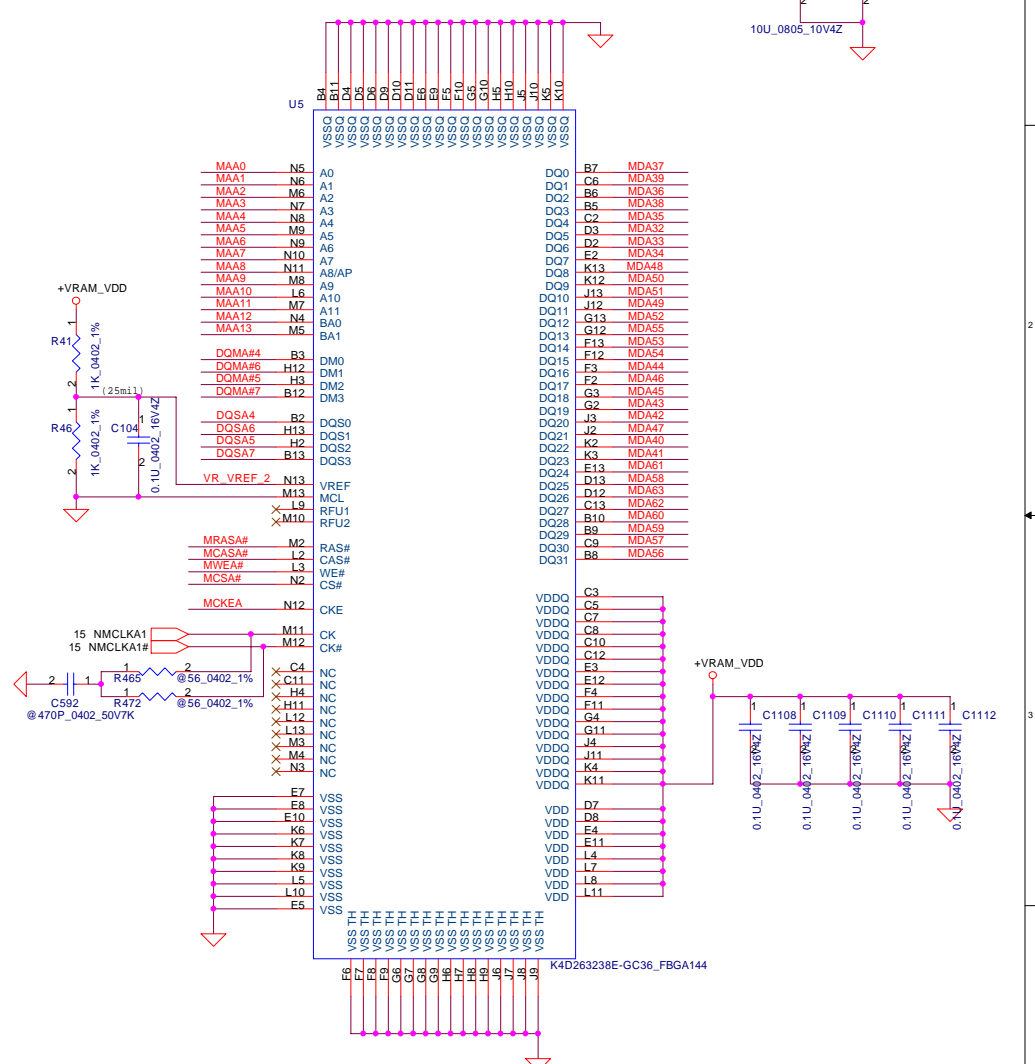
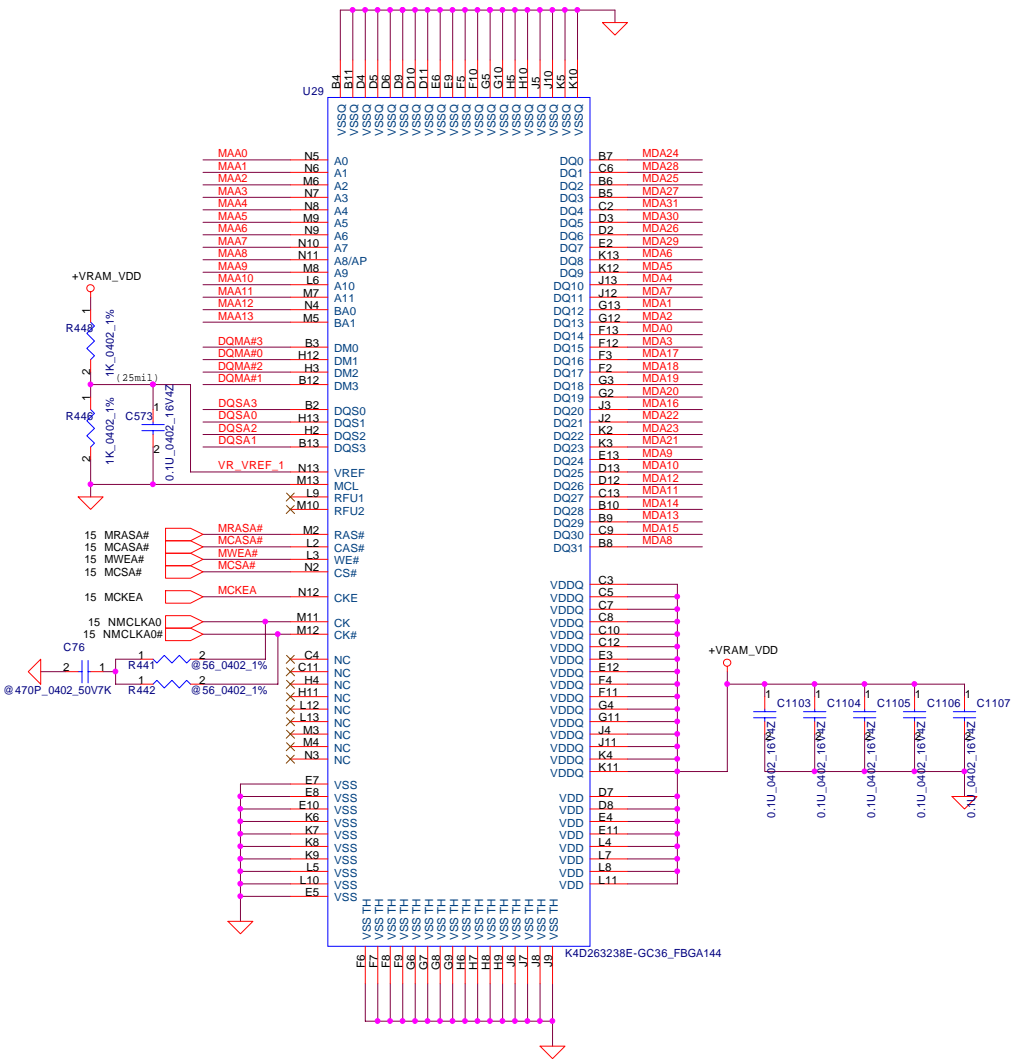
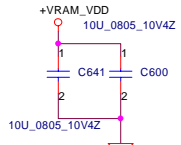
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Customer: **Longbeach 100 <LA-2451>**

Date: 星期六, 十一月 06, 2004 Sheet 15 of 53

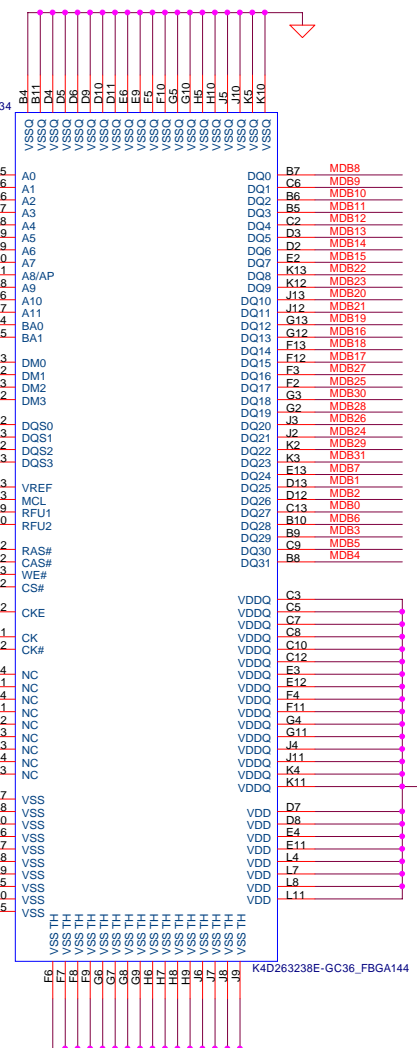
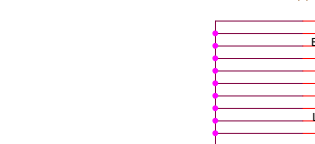
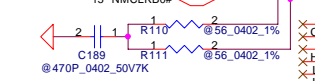
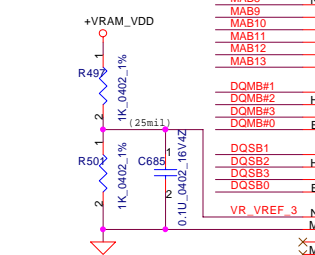
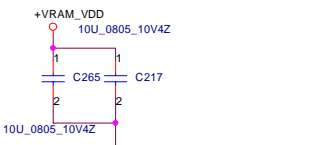
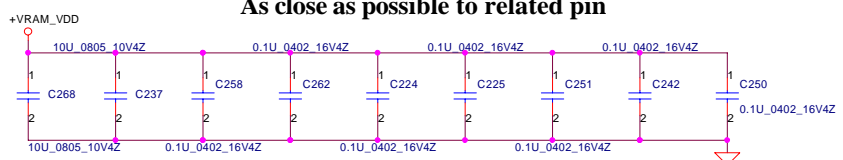
As close as possible to related pin



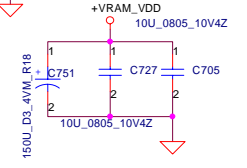
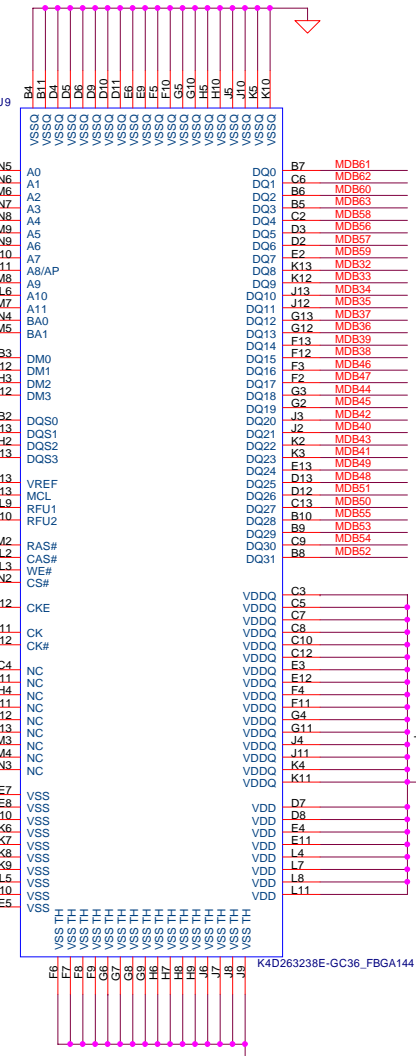
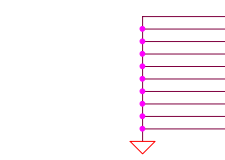
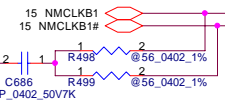
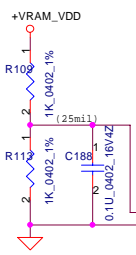
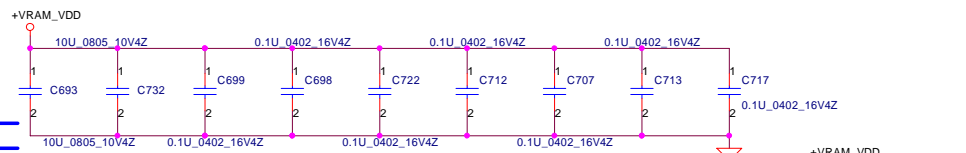
- 15 DQMA#[0..7] DQMA#[0..7]
- 15 MAA#[0..13] MAA#[0..13]
- 15 MDA#[0..63] MDA#[0..63]
- 15 DQSA#[0..7] DQSA#[0..7]



As close as possible to related pin



- 15 DQSB[0..7] DQSB[0..7]
- 15 MDB[0..63] MDB[0..63]
- 15 DQMB#[0..7] DQMB#[0..7]
- 15 MAB[0..13] MAB[0..13]



Compal Electronics, Inc.

Title: **VRAM DDR CHANNEL B**

Size: Document Number

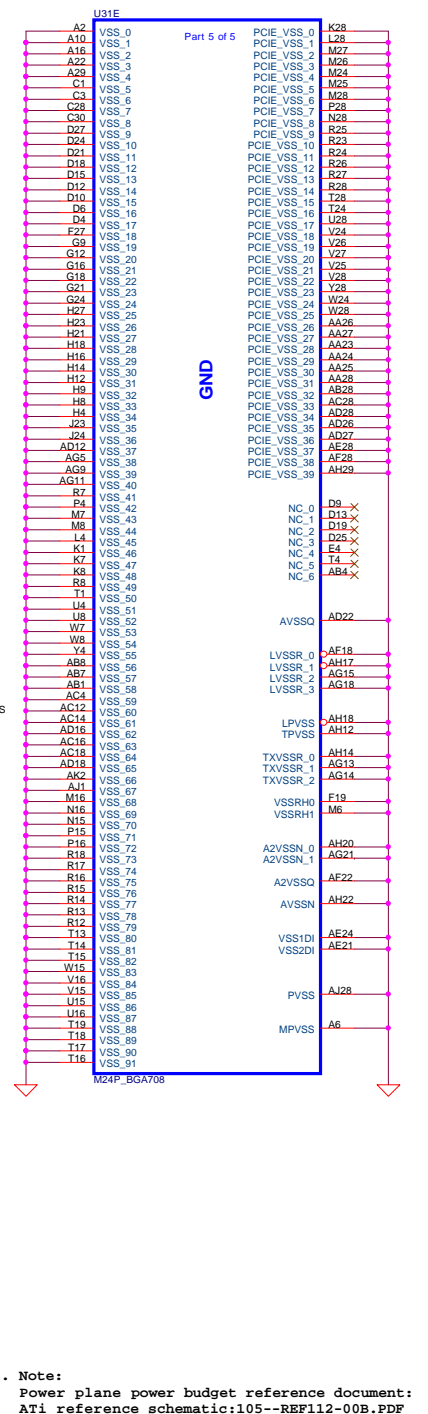
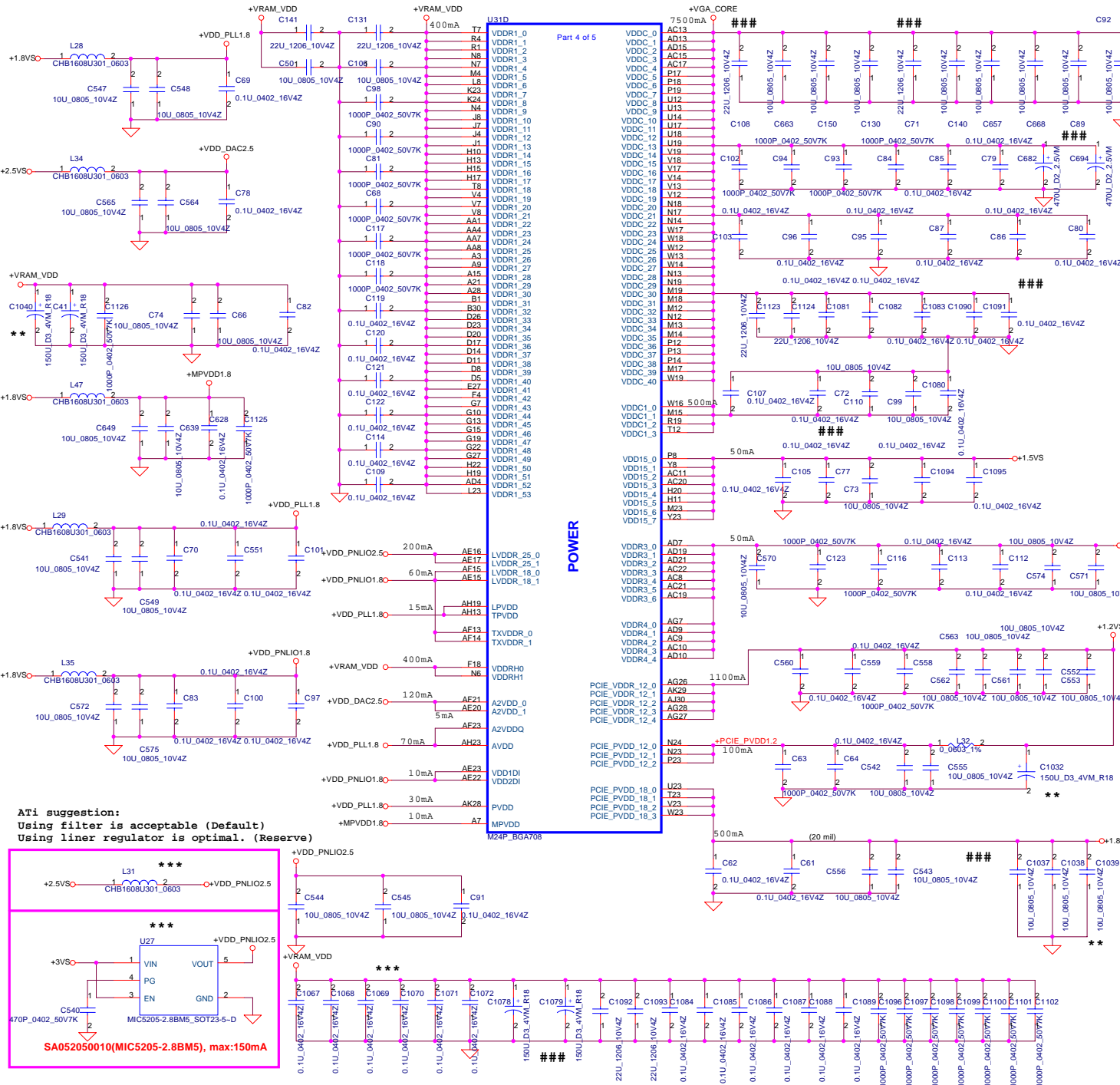
Customer: **Longbeach 100 <LA-2451>**

Date: 星期六, 十一月 06, 2004

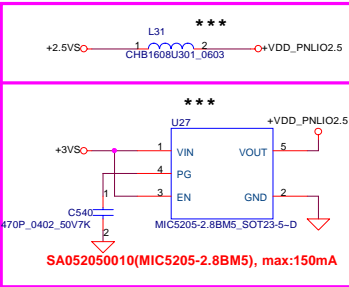
Sheet: 17 of 53

Rev: 0.1

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Ati suggestion:
Using filter is acceptable (Default)
Using liner regulator is optimal. (Reserve)



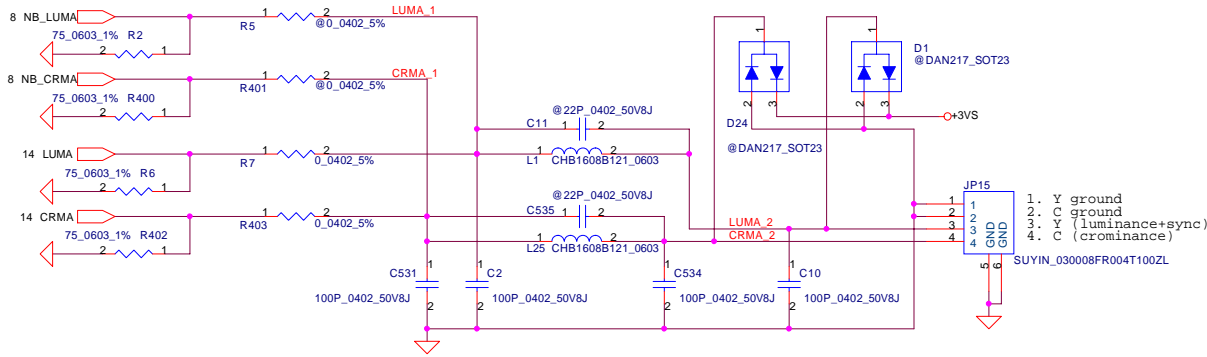
1. Note:
Power plane power budget reference document:
Ati reference schematic:105--REF112-00B.PDF
Ati Power Estimate: PM_M24_A1.pdf

Compal Electronics, Inc.			
Title: M24-P POWER			
Size: Document Number	Customer: Longbeach 100 <LA-2451>	Rev: 0.1	
Date: 星期六,十一月06,2004	Sheet: 18	of 53	

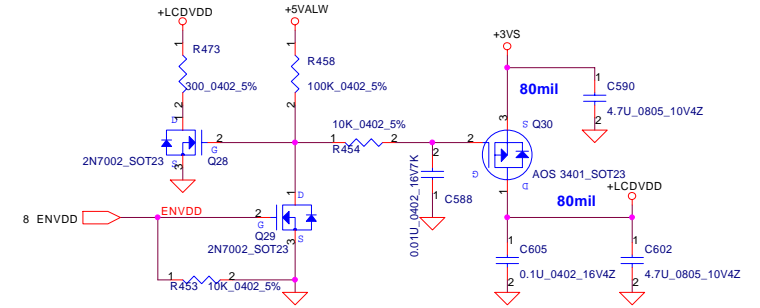
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TV-OUT CONNECTOR

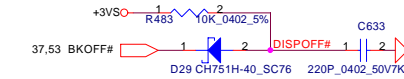
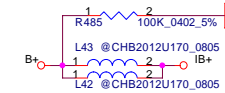
Reduce LUMA_1 and CRMA_1 length
As short as possible



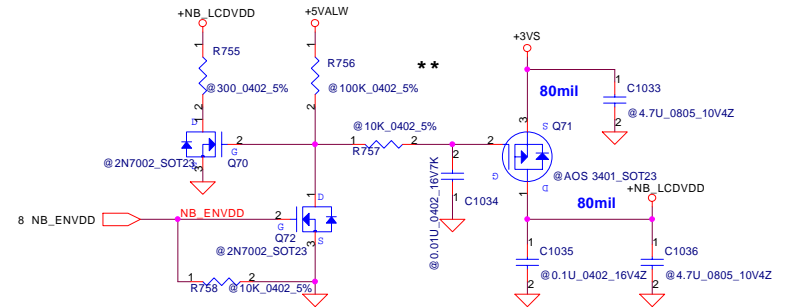
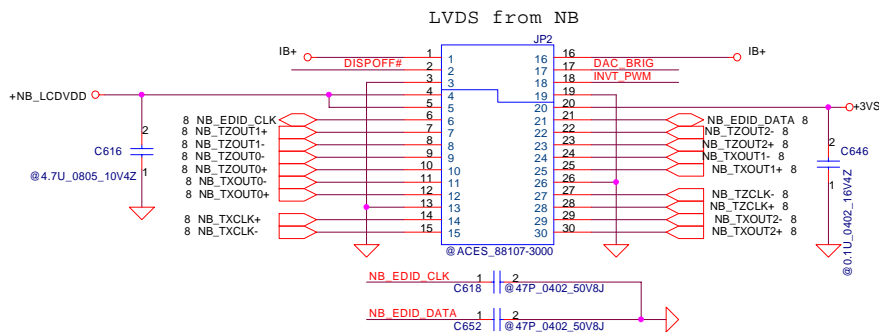
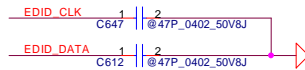
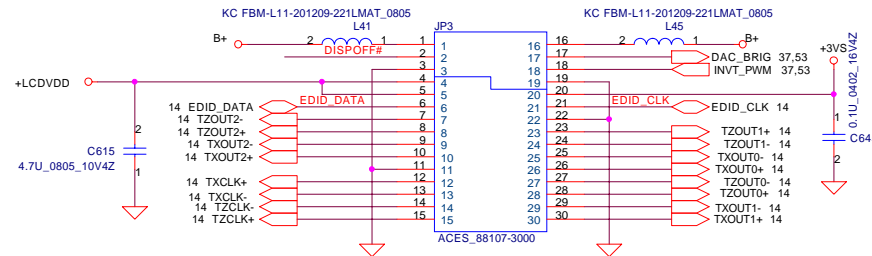
PANEL +LCDVDD CTRL CKT



+LCDVDD Width: 40mils
Place below parts between JP6 and JP7



LCD CONNECTOR



Compal Electronics, Inc.

Title: CRT,TV-OUT,LVDS

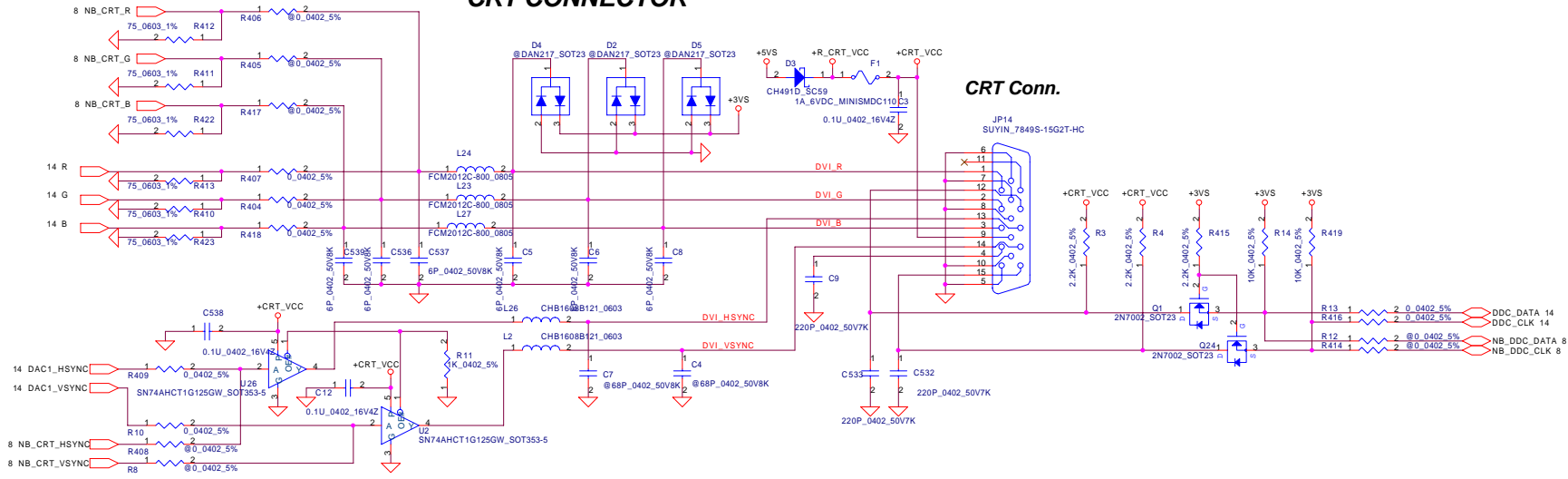
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Customer: Longbeach 100 <LA-2451>

Date: 星期六,十一月06,2004 Sheet 19 of 53

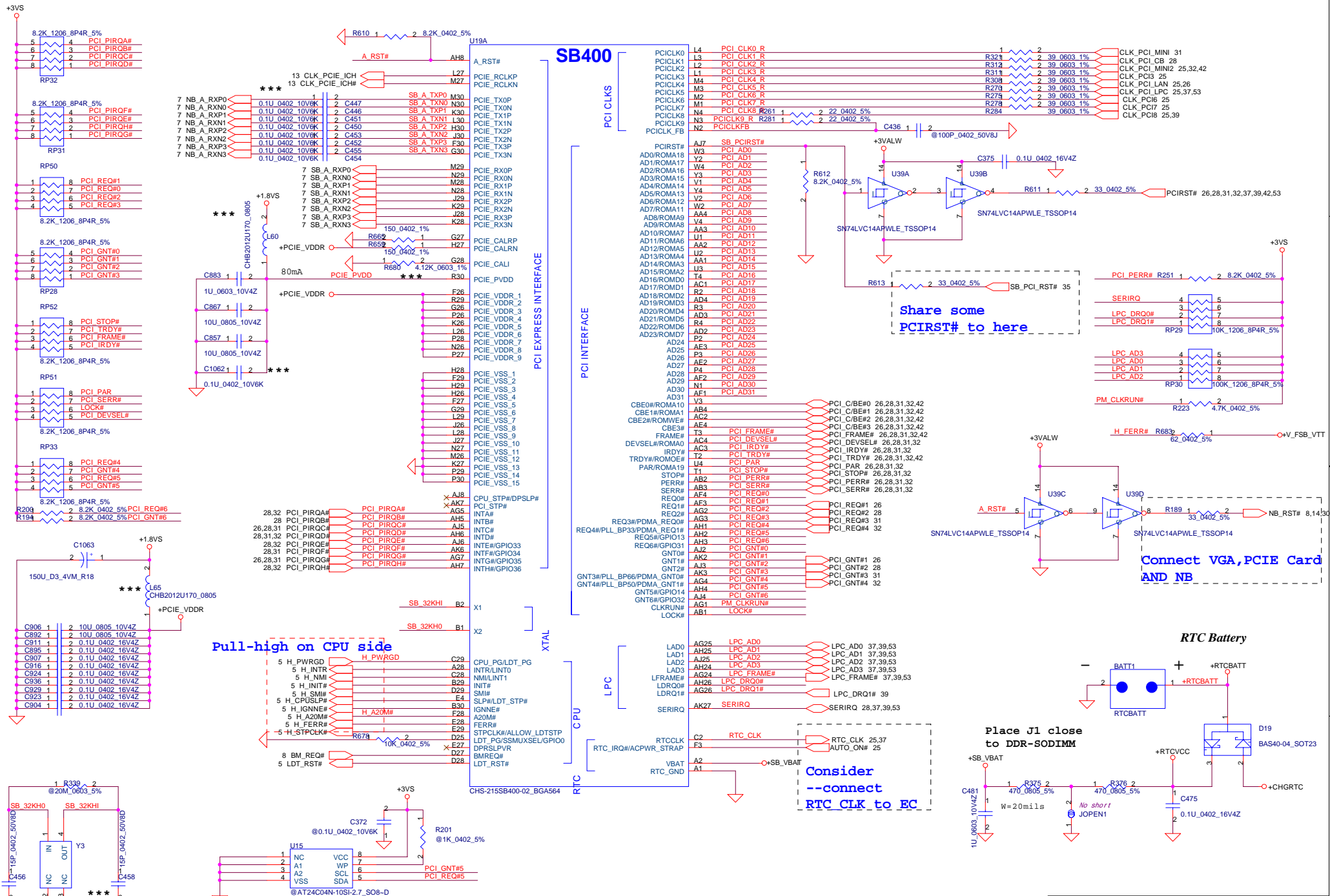
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CRT CONNECTOR



Compal Electronics, Inc.		
Title		
CRT_DVI/SII1362		
Size	Document Number	Rev
C	Longbeach 100 <LA-2451>	0.1
Date:	日期	Sheet
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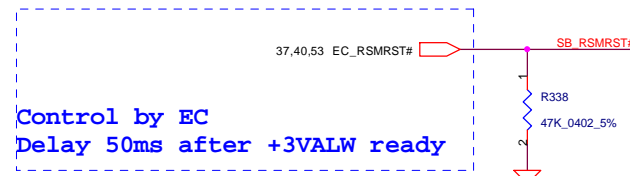
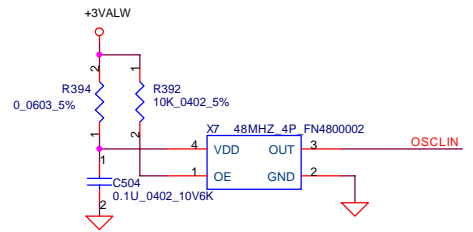
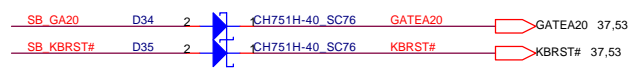
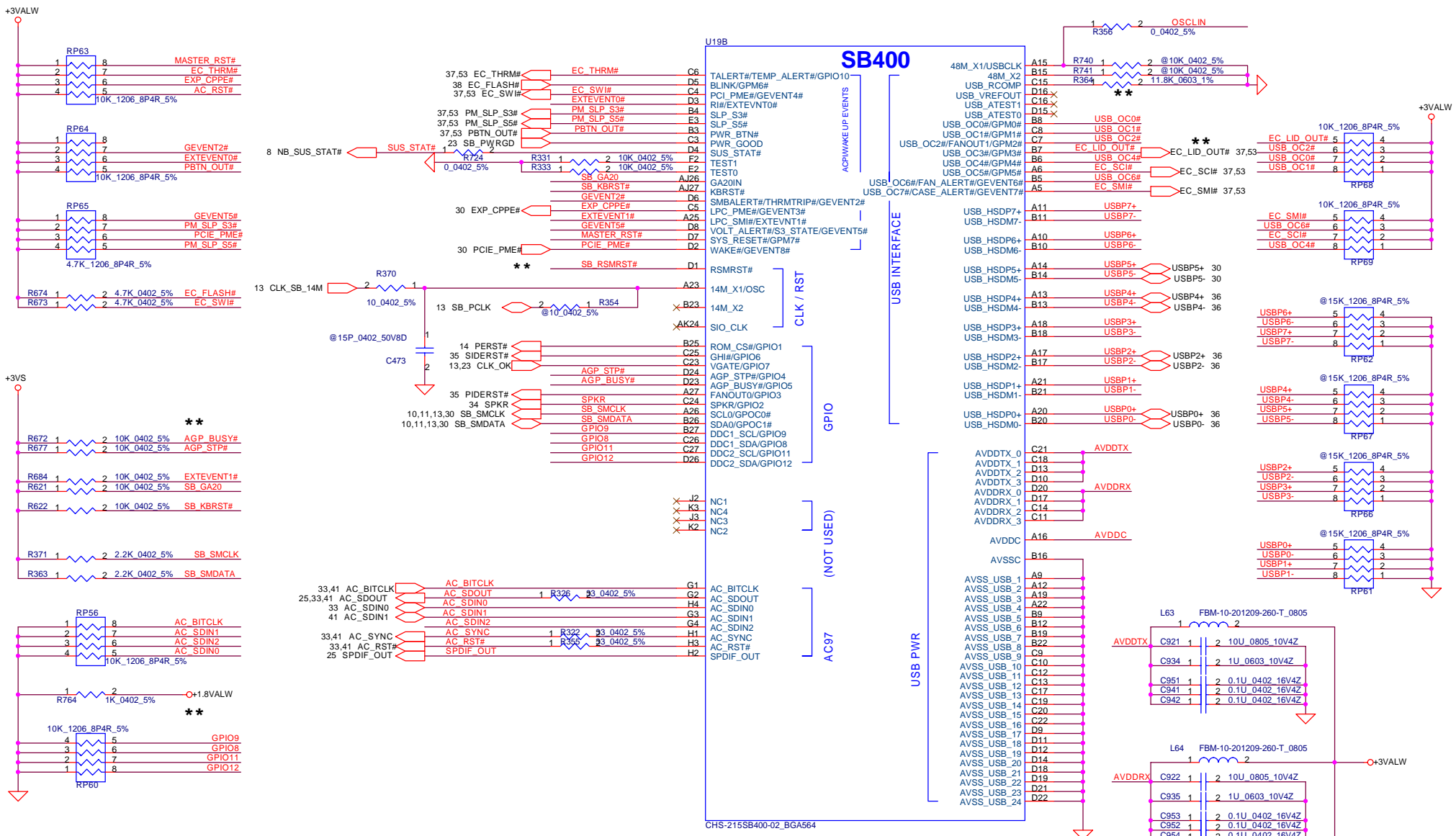
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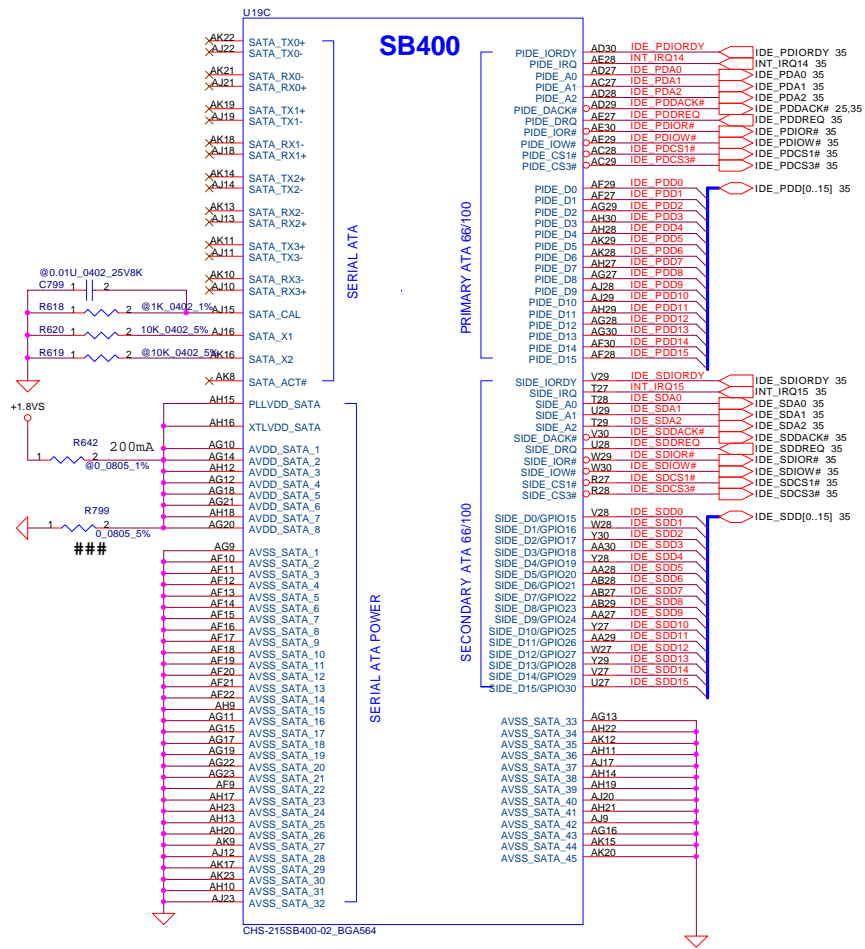
Title		
Compal Electronics, Inc.		
MUTOL/CPU/PM/RTC		
Size	Document Number	Rev
	Longbeach 100 -LA-2451>	0.1
Date:	星期六, 十一月 7, 2006, 2004	Sheet 21 of 53



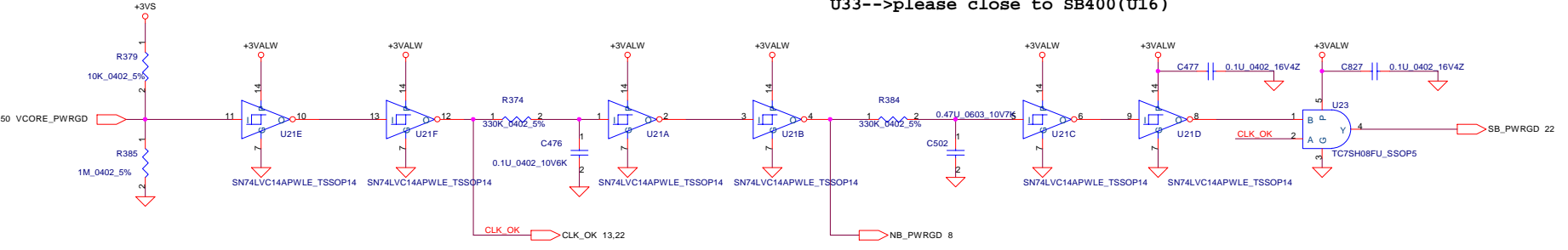
Control by EC
Delay 50ms after +3VALW ready

Compal Electronics, Inc.			
Title	USB/LPC/AC97/MAC		
Size	Document Number	Rev	
	Longbeach 100 <LA-2451>	0.1	
Date:	~P期六, 十一月 06, 2004	Sheet	22 of 53

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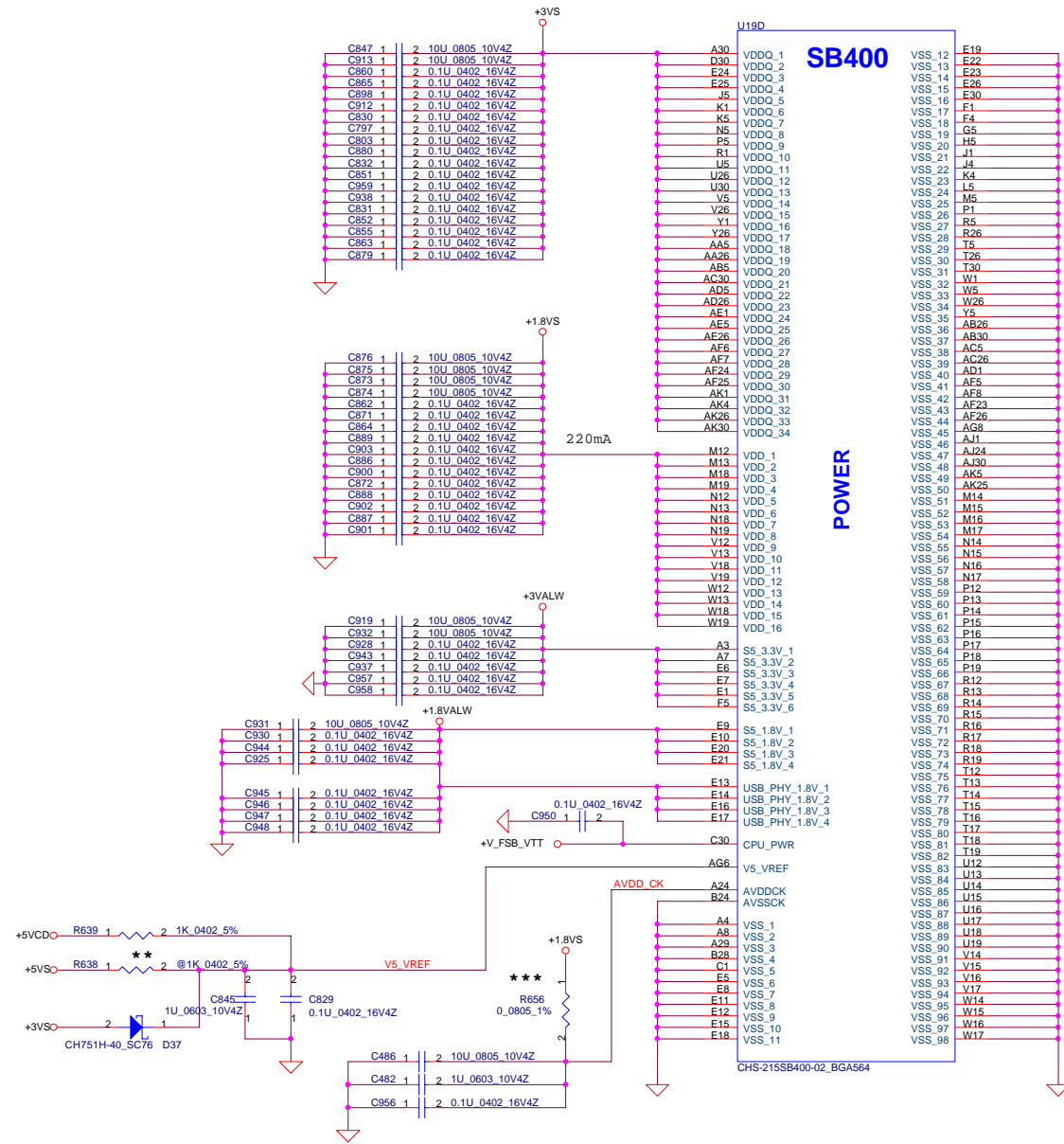
U33-->please close to SB400(U16)



Compal Electronics, Inc.

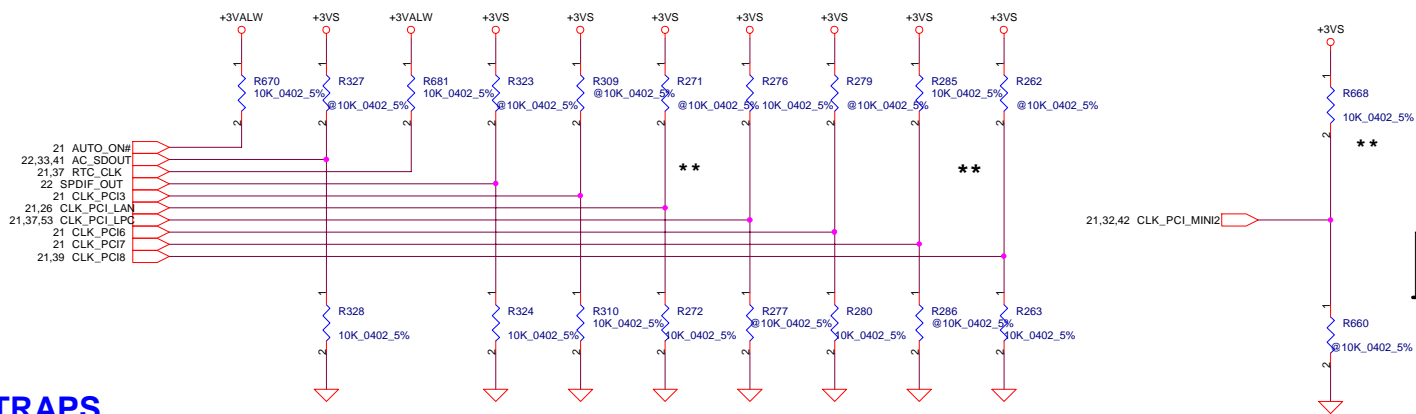
Title		IDE/SATA	
Size	Document Number	Longbeach 100 <LA-2451>	
Date:	2003年11月06日	Sheet	23 of 53
Rev	0.1		

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Compal Electronics, Inc.		
Title Power/GND		
Size	Document Number Longbeach 100 <LA-2451>	Rev 0.1
Date	日期六, 十一, 2006, 2004	Sheet 24 of 53

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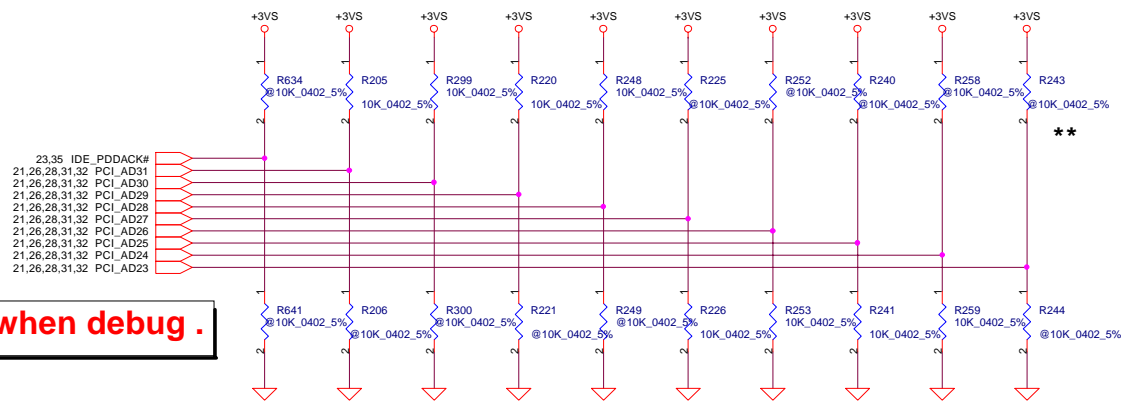


Selects type of 48MHz clock pad

REQUIRED STRAPS



	AUTO_ON#	AC97_SDOOUT	RTC_CLK	SPDIF_OUT	CLK_PCI3	CLK_PCI_LAN	CLK_PCI_LPC	PCI_CLK6	PCI_CLK7	PCI_CLK8	CLK_PCI_MINI2
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS DEFAULT	INTERNAL RTC DEFAULT	SIO 24MHz DEFAULT	USB PHY PWRDOWN DISABLE DEFAULT	Internal PLL DEFAULT	14MHz OSC MODE DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = LPC ROM I		Clock input buffer DEFAULT
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	USB PHY PWRDOWN ENABLE DEFAULT	External Clock DEFAULT	14MHz XTAL MODE	CPU I/F = P4 DEFAULT	L,H = LPC ROM II L,L = FWH ROM		Crystal Pad



Pop R634 when debug .

DEBUG STRAPS

	IDE_PDDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24
PULL HIGH	USE LONG RESET DEFAULT	PLL CHARGE PUMP CTRL BIT 1 HI DEFAULT	PLL CHARGE PUMP CTRL BIT 0 HI DEFAULT	PLL VCO CTRL BIT 1 HI DEFAULT	PLL VCO CTRL BIT 0 HI DEFAULT	BYPASS PCI PLL	BYPASS ACPI BCLK DEFAULT	BYPASS IDE PLL	USE EEPROM PCIE STRAPS
PULL LOW	USE SHORT RESET	PLL CHARGE PUMP CTRL BIT 1 LO	PLL CHARGE PUMP CTRL BIT 0 LO	PLL VCO CTRL BIT 1 LO	PLL VCO CTRL BIT 0 LO	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT

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Compal Electronics, Inc.

Hardware Trap

Title		
Size	Document Number	Rev
	Longbeach 100 <LA-2451>	0.1
Date:	星期六, 十一月 7 2006, 2004	Sheet 25 of 53

21,25,28,31,32,42 PCI_AD[0..31]

28,31 PCI_PIRQC#

28,31 PCI_PIRQC#

21,28,31,32,42 PCI_C/BE#0

21,28,31,32,42 PCI_C/BE#1

21,28,31,32,42 PCI_C/BE#2

21,28,31,32,42 PCI_C/BE#3

21,28,31,32 PCI_PAR

21,28,31,32,42 PCI_FRAME#

21,28,31,32 PCI_IRDY#

21,28,31,32,42 PCI_TRDY#

21,28,31,32 PCI_DEVSEL#

21,28,31,32 PCI_STOP#

21,28,31,32 PCI_PERR#

21,28,31,32 PCI_SERR#

21 PCI_REQ#1

21 PCI_GNT#1

31,37,53 LAN_PME#

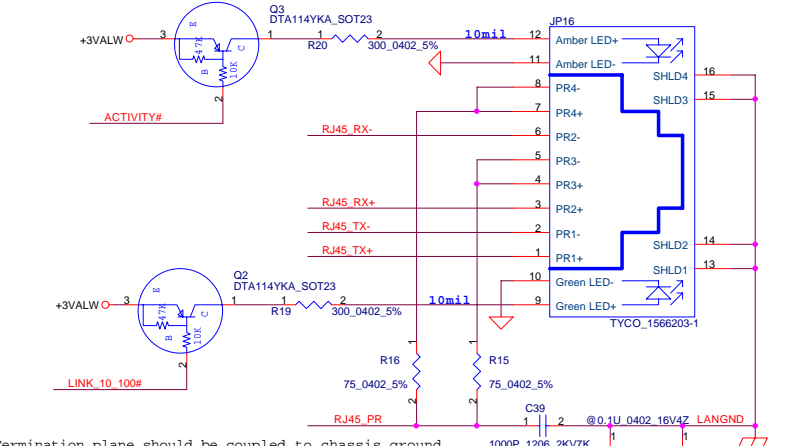
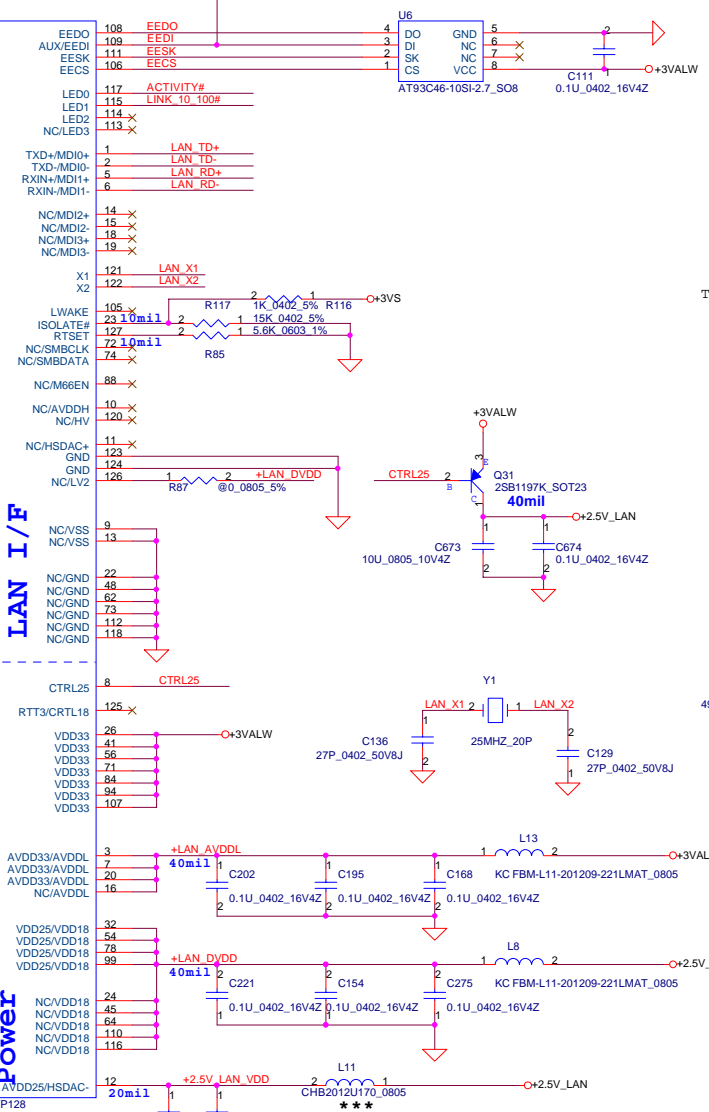
21,28,31,32,37,39,42,53 PCIRST#

21,25 CLK_PCI_LAN

PCI_AD0	104	AD0
PCI_AD1	102	AD1
PCI_AD2	102	AD2
PCI_AD3	98	AD3
PCI_AD4	97	AD4
PCI_AD5	96	AD5
PCI_AD6	95	AD6
PCI_AD7	93	AD7
PCI_AD8	90	AD8
PCI_AD9	89	AD9
PCI_AD10	87	AD10
PCI_AD11	86	AD11
PCI_AD12	85	AD12
PCI_AD13	83	AD13
PCI_AD14	82	AD14
PCI_AD15	79	AD15
PCI_AD16	59	AD16
PCI_AD17	58	AD17
PCI_AD18	57	AD18
PCI_AD19	55	AD19
PCI_AD20	53	AD20
PCI_AD21	49	AD21
PCI_AD22	47	AD22
PCI_AD23	46	AD23
PCI_AD24	43	AD24
PCI_AD25	42	AD25
PCI_AD26	40	AD26
PCI_AD27	39	AD27
PCI_AD28	37	AD28
PCI_AD29	36	AD29
PCI_AD30	34	AD30
PCI_AD31	33	AD31

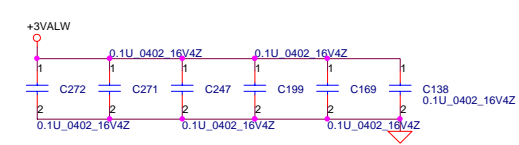
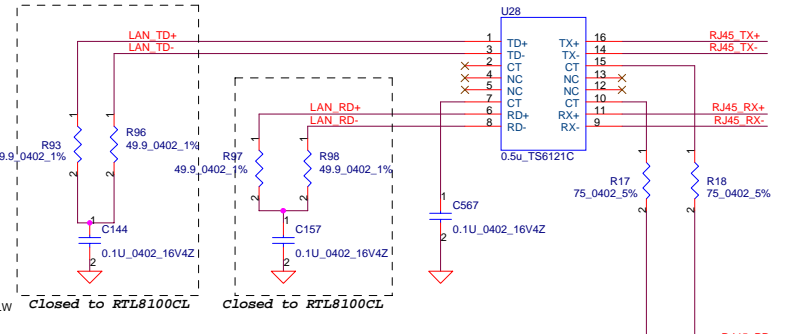
C/BE#0	92	C/BE#0
C/BE#1	77	C/BE#1
C/BE#2	80	C/BE#2
C/BE#3	44	C/BE#3
IDSEL	48	IDSEL
PAR	78	PAR
FRAME#	61	FRAME#
IRDY#	63	IRDY#
TRDY#	67	TRDY#
DEVSEL#	68	DEVSEL#
STOP#	69	STOP#
PERR#	75	PERR#
SERR#	75	SERR#
REQ#	30	REQ#
GNT#	29	GNT#
INTA#	25	INTA#
PME#	31	PME#
RST#	27	RST#
CLK	28	CLK
CLKRUN#	65	CLKRUN#
GND/VSS	4	GND/VSS
GND/VSS	17	GND/VSS
GND/VSS	128	GND/VSS
GND/VSSPST	21	GND/VSSPST
GND/VSSPST	38	GND/VSSPST
GND/VSSPST	51	GND/VSSPST
GND/VSSPST	66	GND/VSSPST
GND/VSSPST	81	GND/VSSPST
GND/VSSPST	91	GND/VSSPST
GND/VSSPST	101	GND/VSSPST
GND/VSSPST	119	GND/VSSPST
GND	35	GND
GND	52	GND
GND	80	GND
GND	100	GND

AVDD25/HSADC	12	AVDD25/HSADC
NC/VDD18	24	NC/VDD18
NC/VDD18	45	NC/VDD18
NC/VDD18	64	NC/VDD18
NC/VDD18	110	NC/VDD18
NC/VDD18	116	NC/VDD18



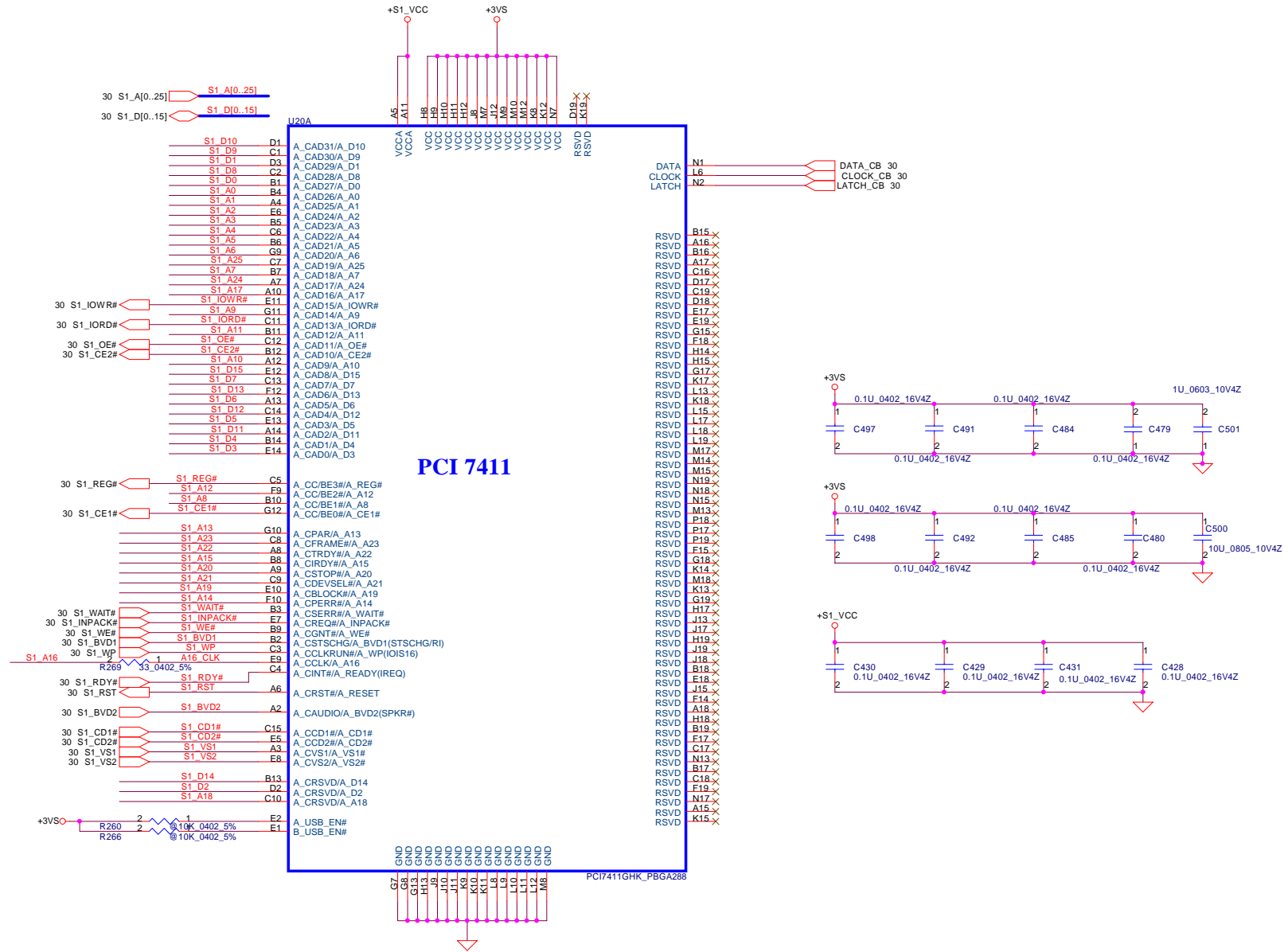
Termination plane should be coupled to chassis ground

Layout Note
TS6121 pls close to conn.



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Compal Electronics, Inc.			
Ethernet RTL8100CL			
Title	Document Number	Rev	0.1
Date	星期六, 十一月 706, 2004	Sheet	26 of 53

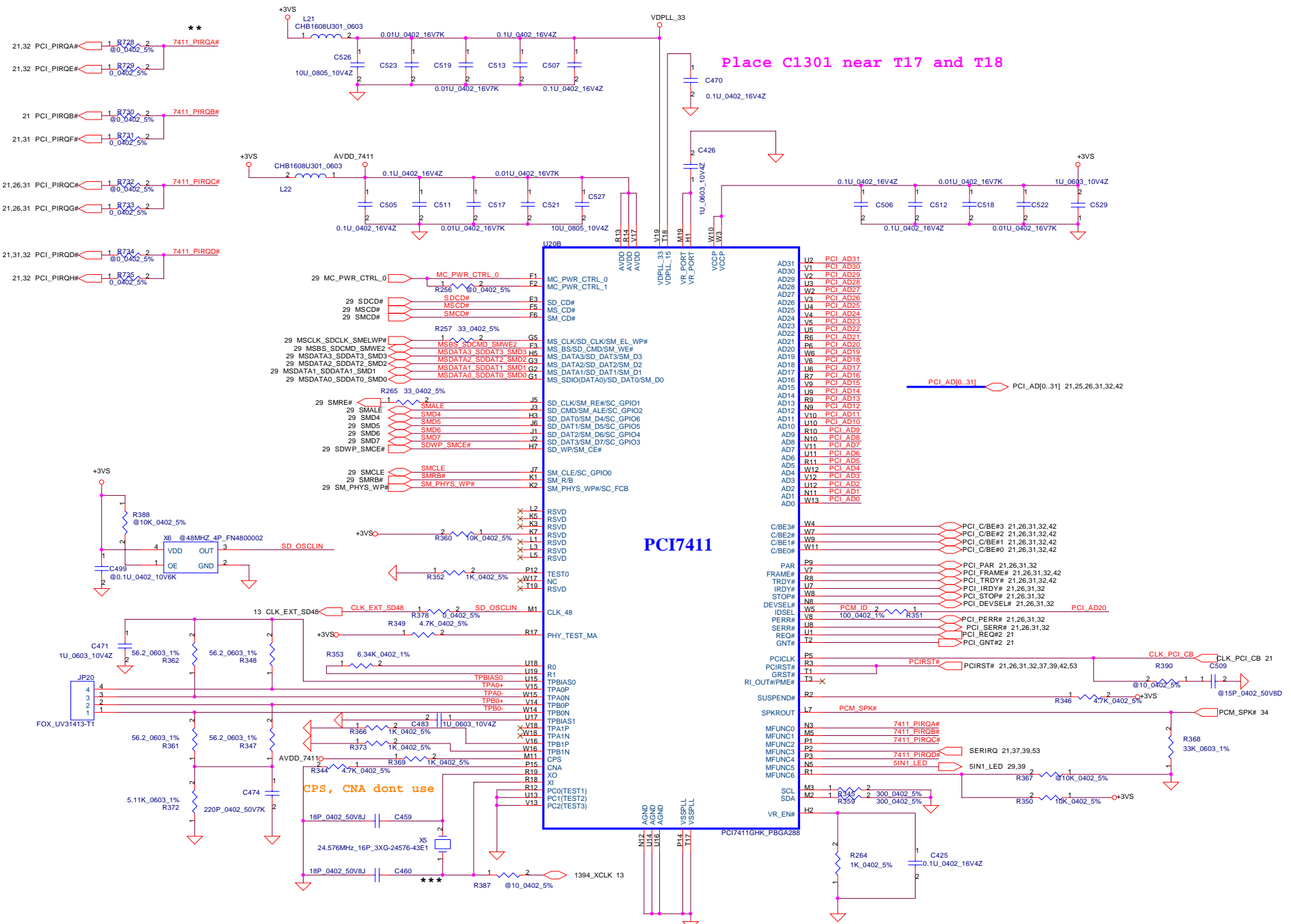


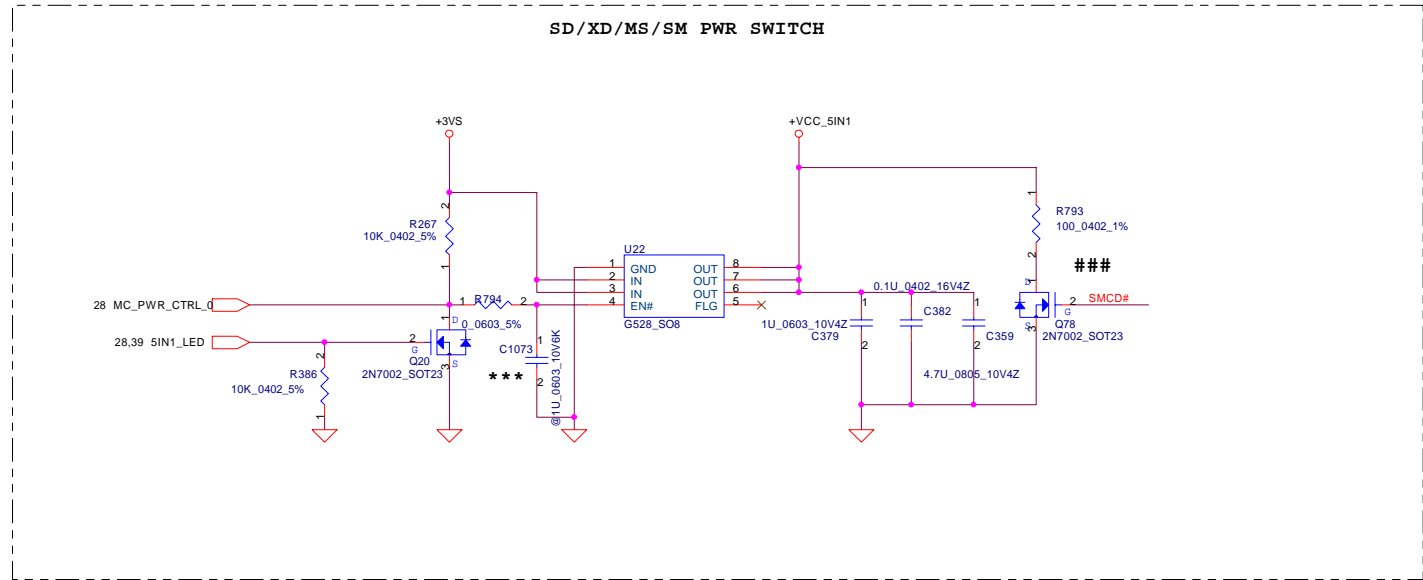
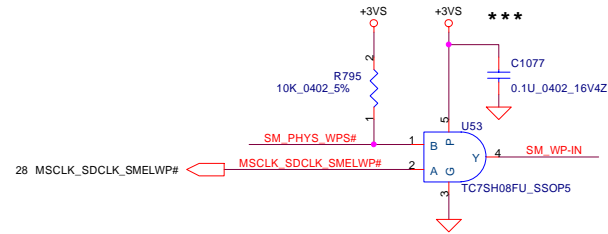
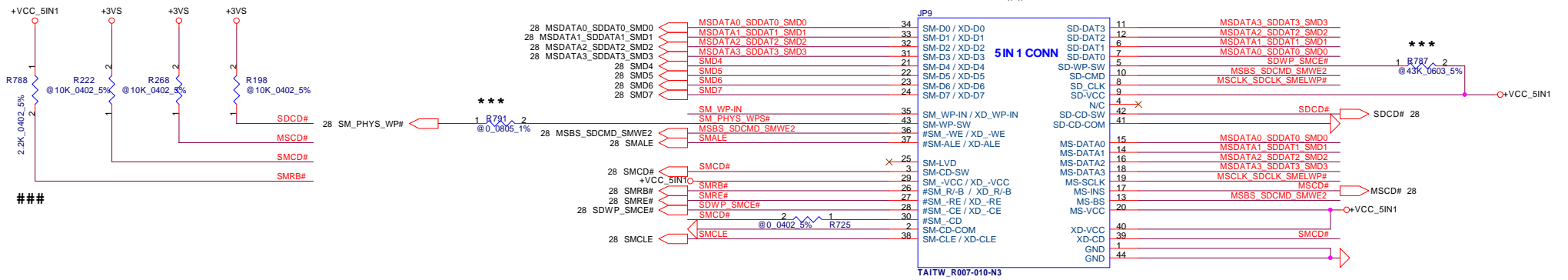
PCI 7411

PCI7411GHK_PBGA288

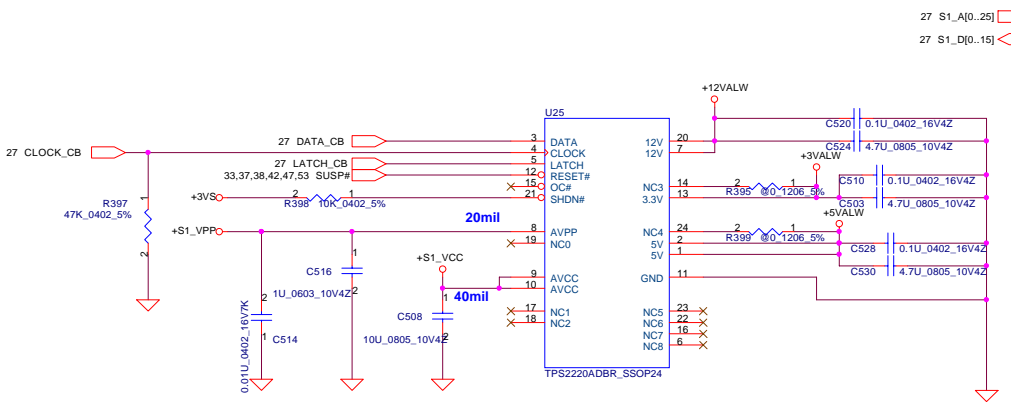
Title PCI7411-1		
Size Custom	Document Number Longbeach 100 <LA-2451>	Rev 0.1
Date: 星期六, 十一月 06, 2004	Sheet 27	of 53

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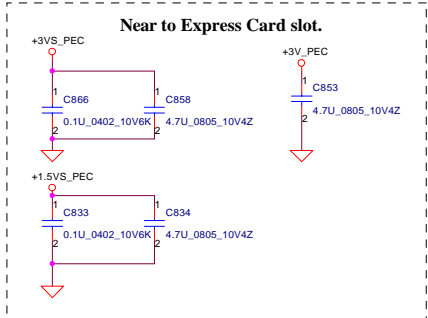
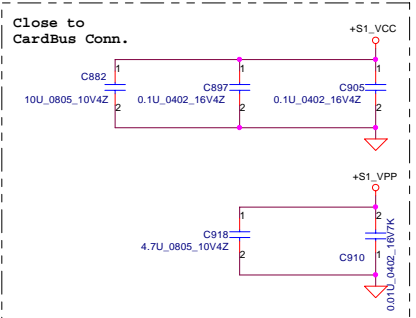
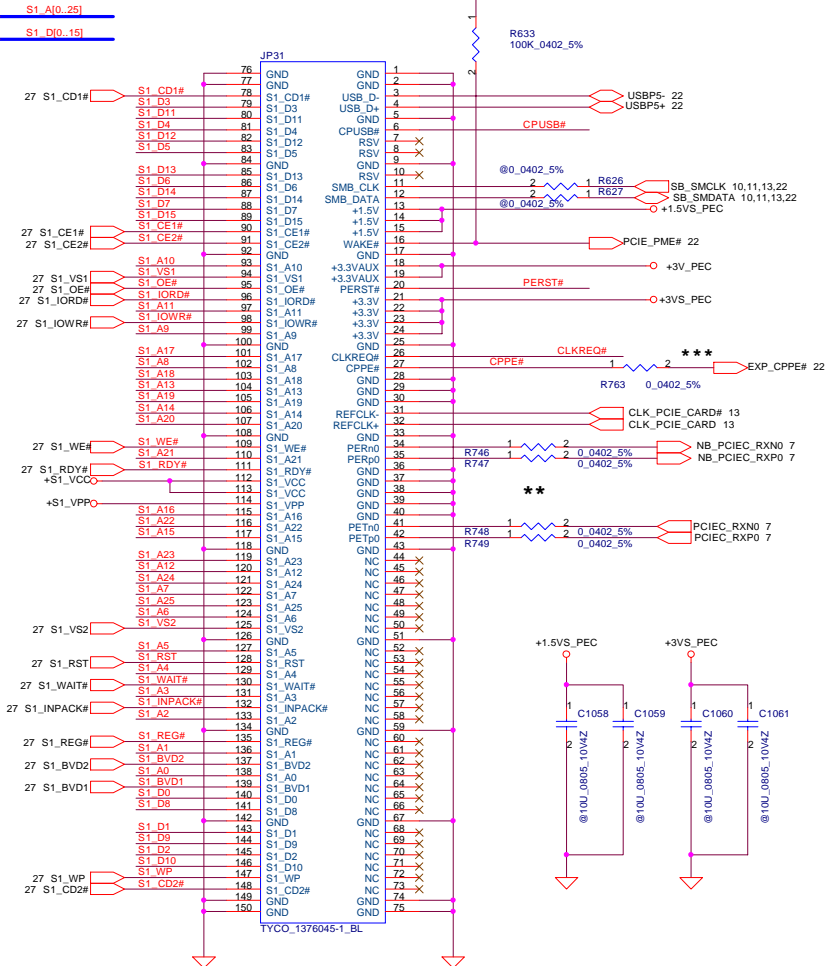




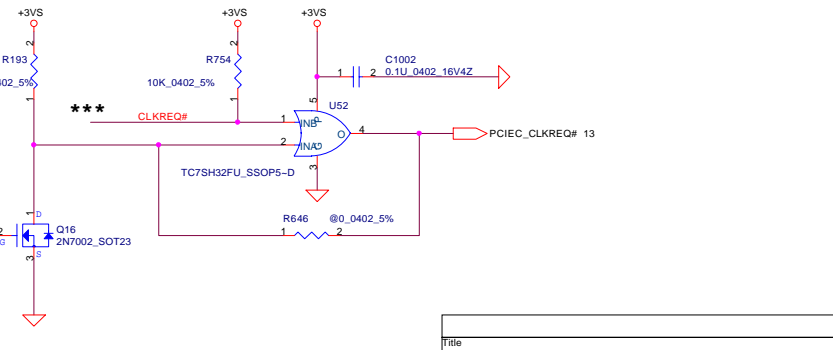
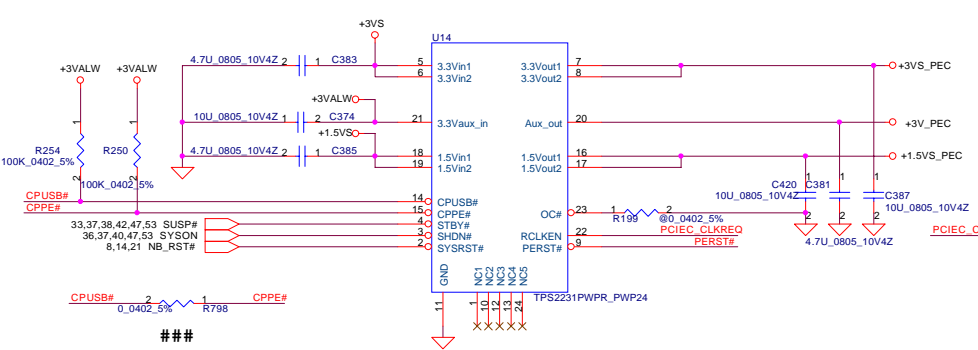
Power Switch for PCMCIA



CardBus & PCI-E Socket

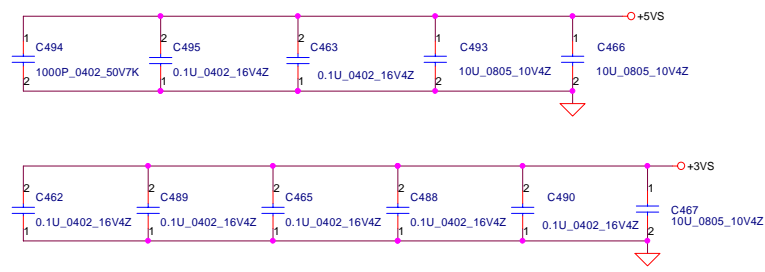
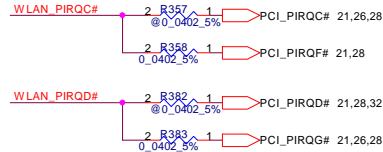
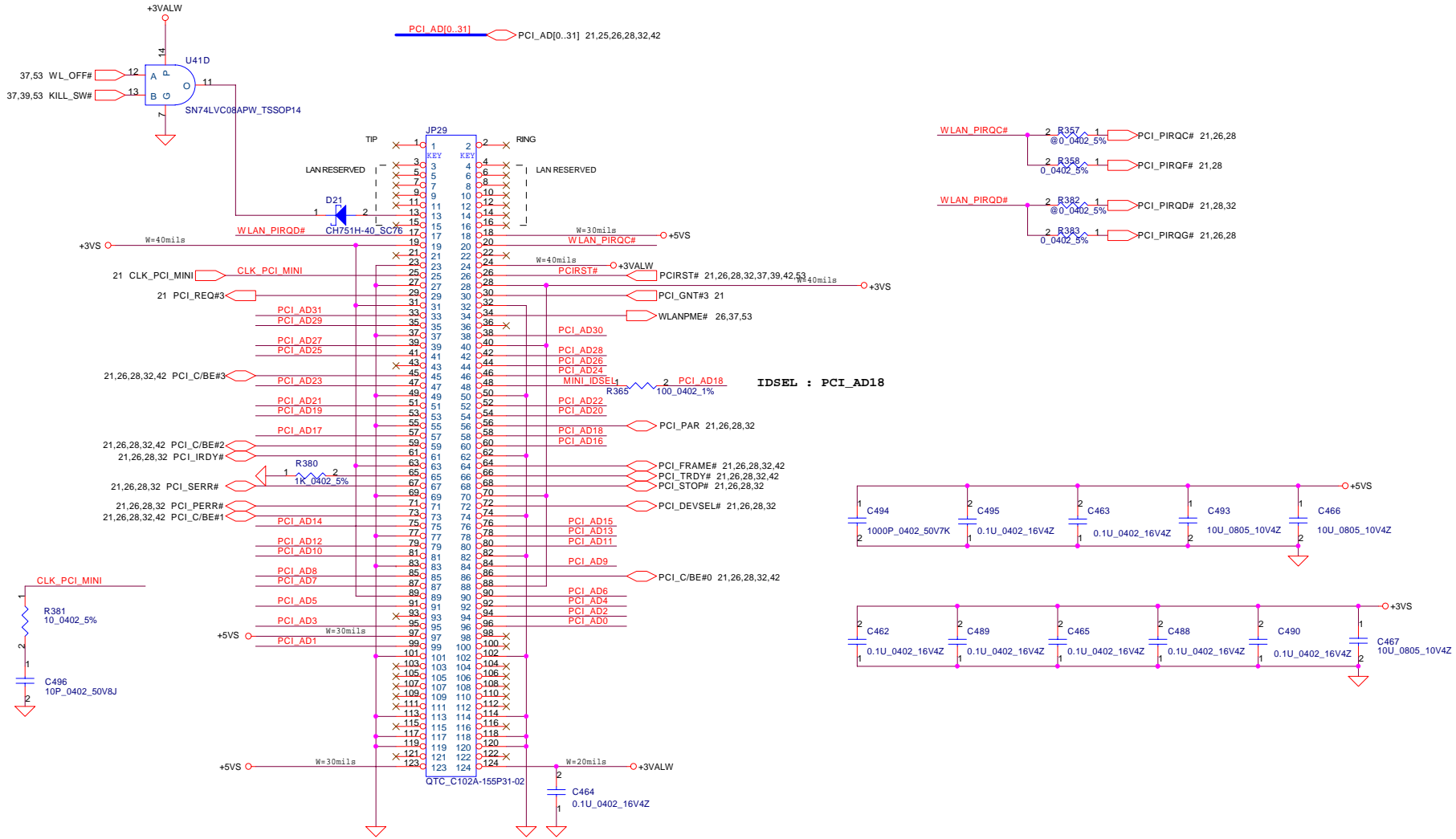


Power Switch for PCI-E



Title PCMCIA Socket		
Size Document Number	Customer Longbeach 100 <LA-2451>	
Rev 0.1	Date 2004.06.11	Sheet 30 of 53

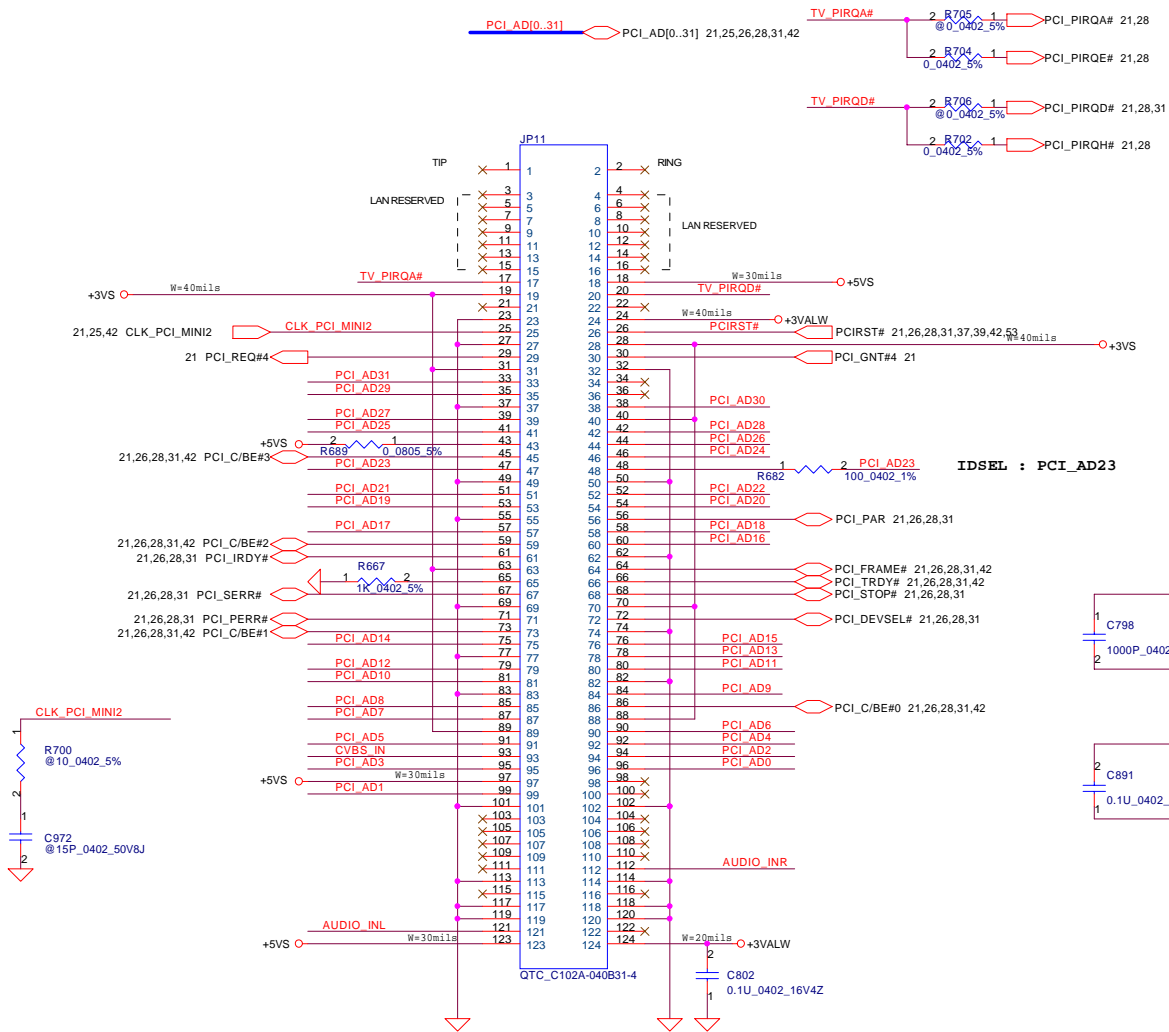
MINI_PCI 1 SOCKET FOR WLAN (BOTTOM)



Compal Electronics, Inc.		
Title MINI_PCI-WLAN		
Size	Document Number	Rev
Customer	Longbeach 100 <LA-2451>	0.1
Date:	星期六, 十一月 06, 2004	Sheet 31 of 53

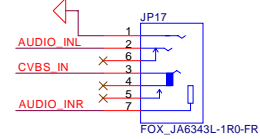
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MINI_PCI 2 SOCKET FOR TV TURNER (TOP)

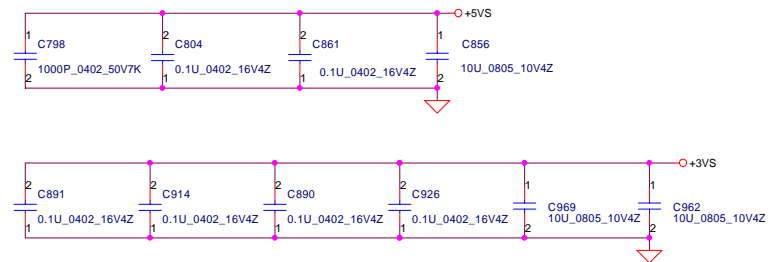
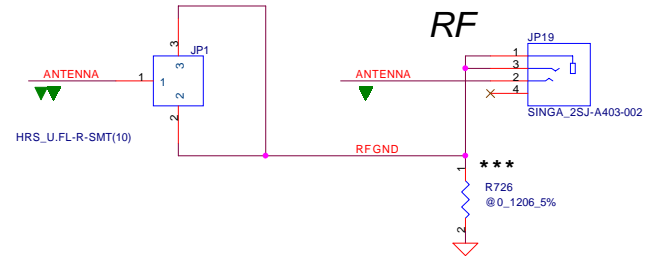


TV-Tuner

AV IN



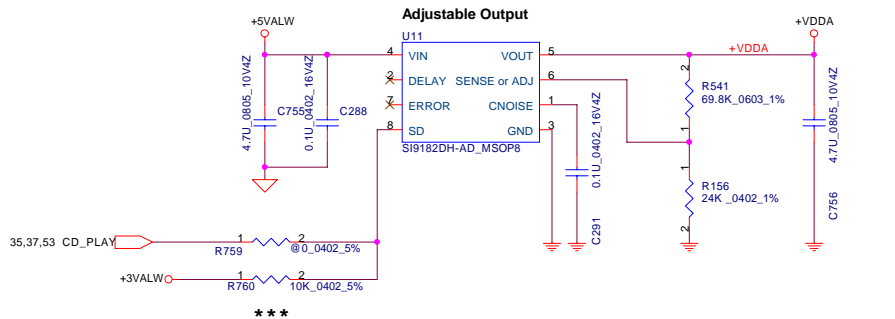
RF



Compal Electronics, Inc.

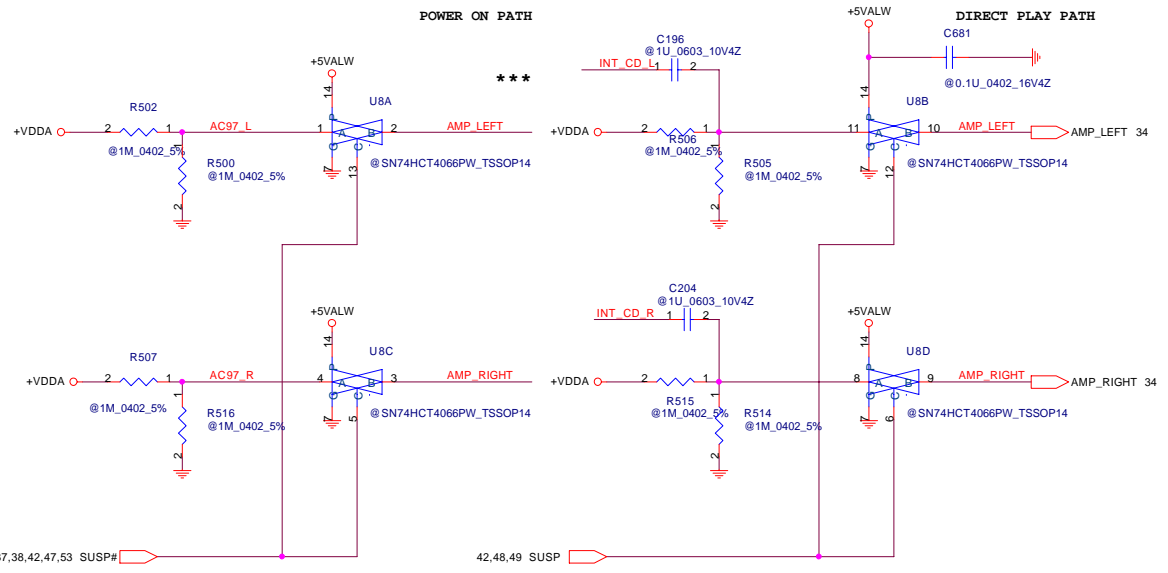
Title MINI_PCI-TV Tuner		
Size	Document Number	Rev
Customer	Longbeach 100 <LA-2451>	0.1
Date:	星期六, 十一月 06, 2004	Sheet 32 of 53

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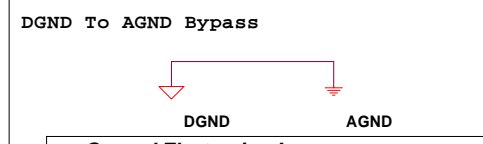
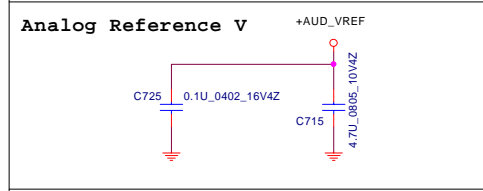
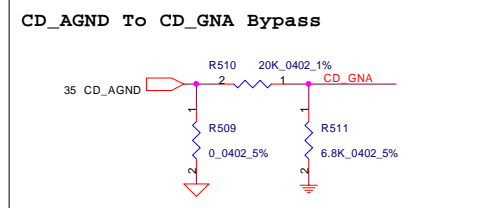
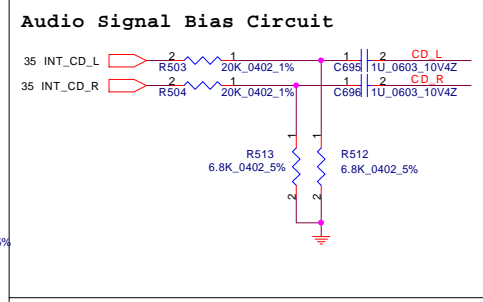
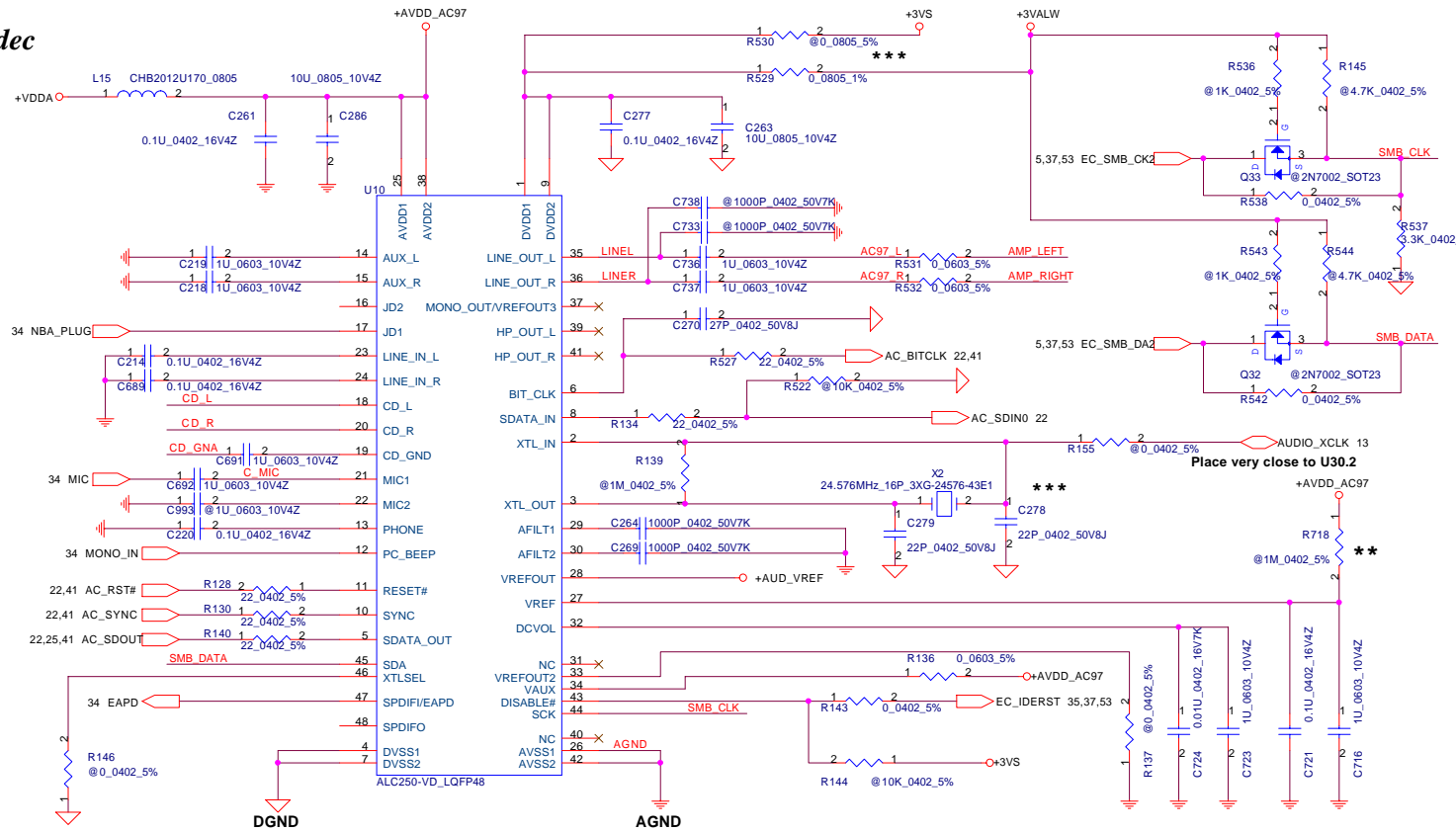


DEFAULT (WITH 4066)
 U0 R0 R7 R8 R9 R10 R11 R12 R13 R14 C1 C2 C3 POP
 Q1 Q2 R1 R2 R3 R4 R5 R6 DEPOP

S3 (WITHOUT 4066)
 Q1 Q2 R1 R2 R3 R4 R5 R6 POP
 U1 R0 R7 R8 R9 R10 R11 R12 R13 R14 C1 C2 C3 DEPOP



AC97 Codec



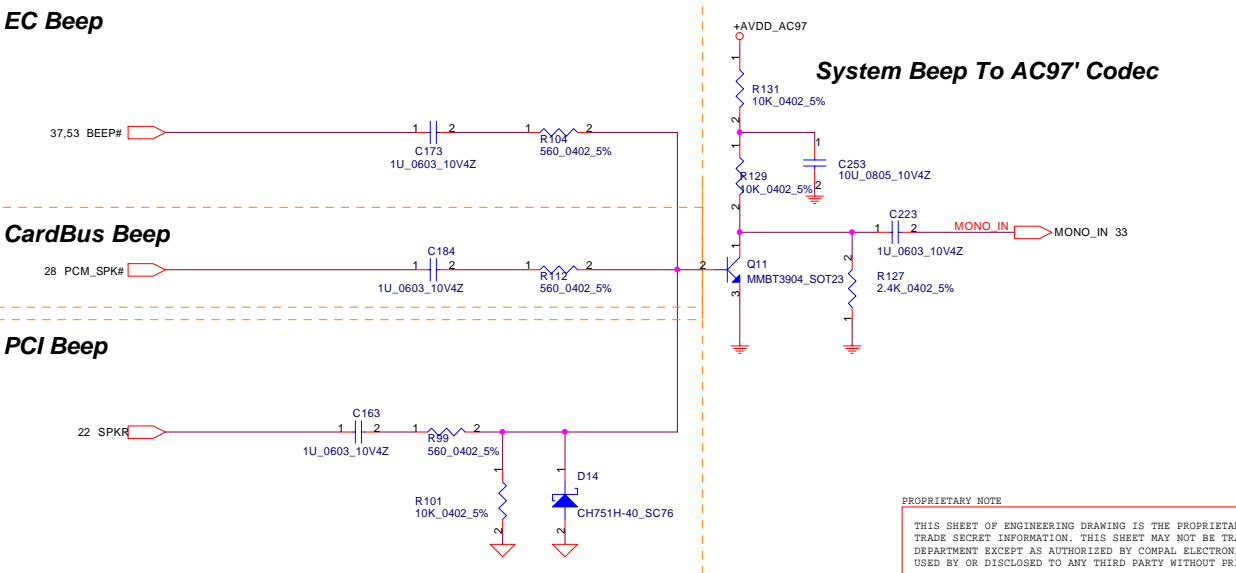
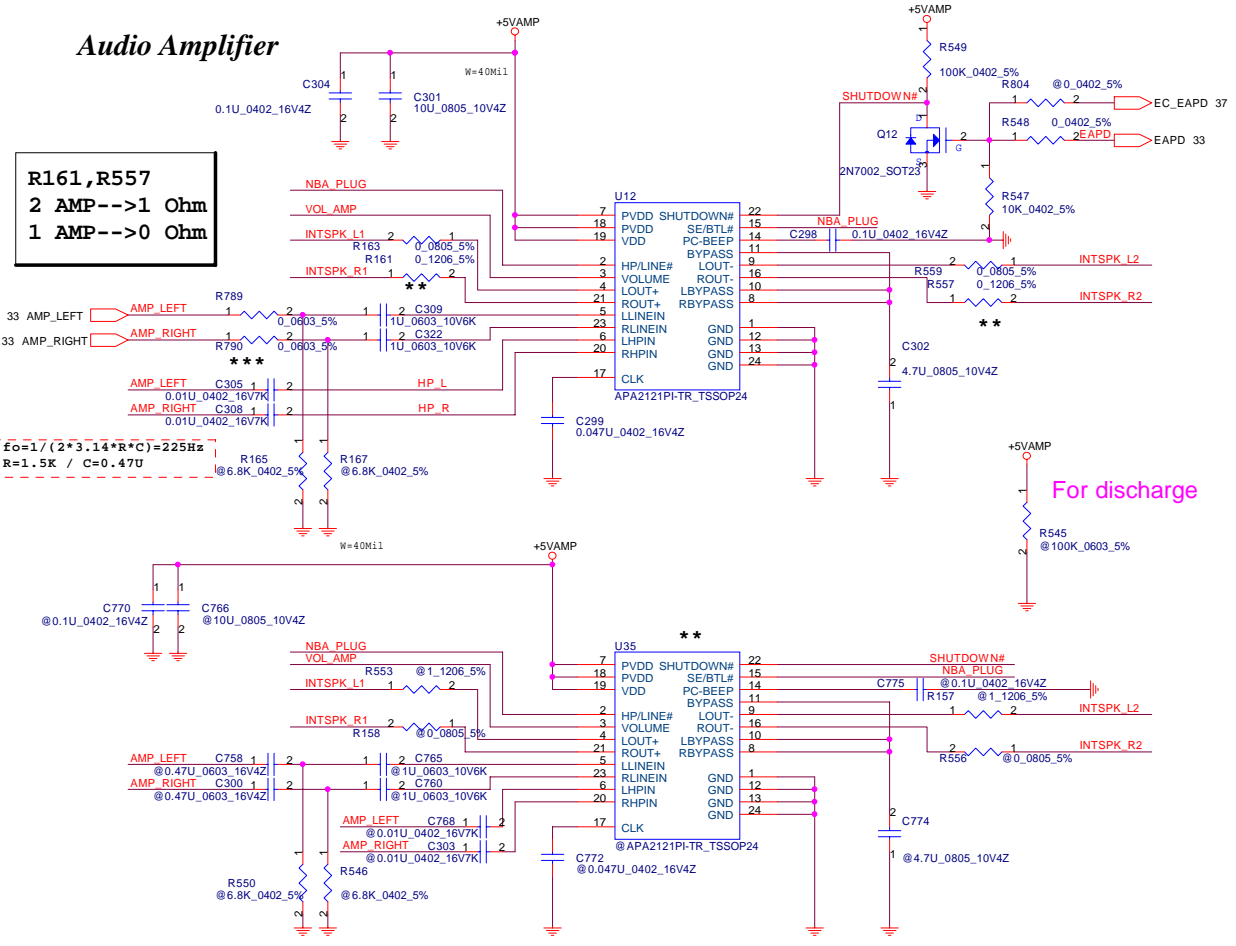
WITH 14.318MHz : Rxxx POP
 WITH 24.576MHz : Rxxx DEPOP

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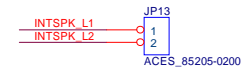
Compal Electronics, Inc.		
Title: AC97 Codec		
Size: Document Number	Customer: Longbeach 100 <LA-2451>	Rev: 0.1
Date: 星期六, 十一月 06, 2004	Sheet: 33	of 53

Audio Amplifier

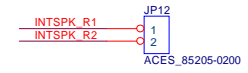
R161, R557
2 AMP-->1 Ohm
1 AMP-->0 Ohm



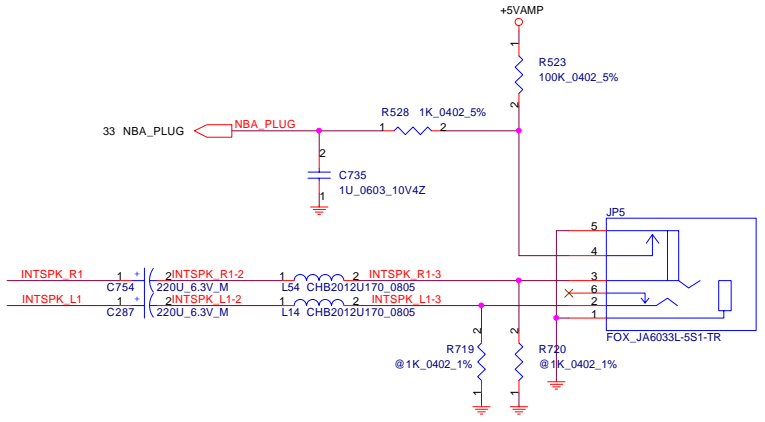
Left Speaker Connector



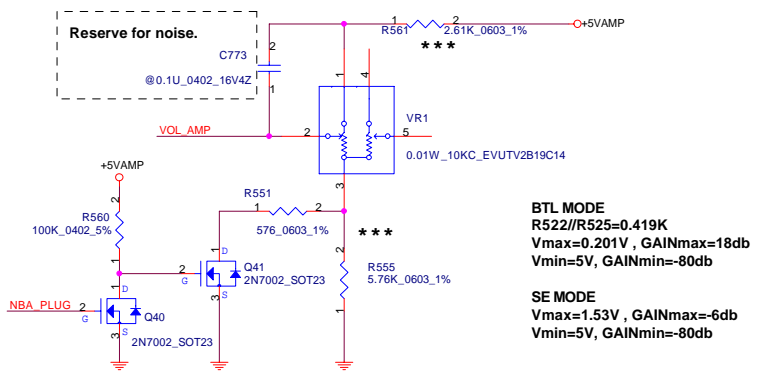
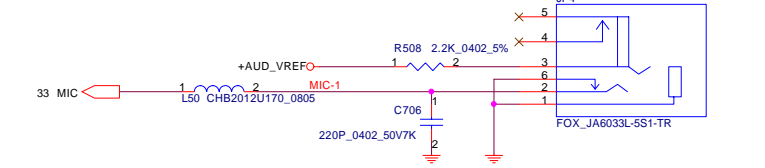
Right Speaker Connector



HEADPHONE OUT JACK



MICROPHONE IN JACK

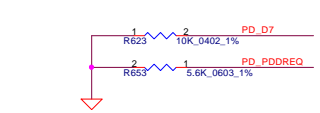
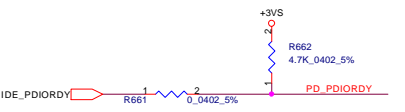
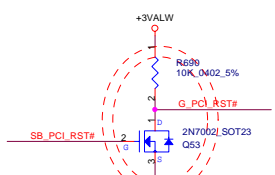
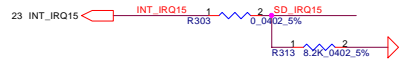
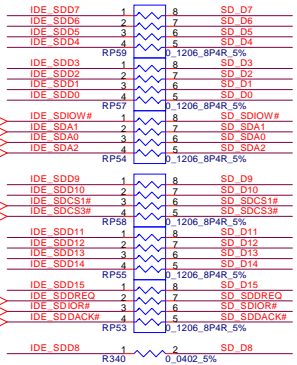
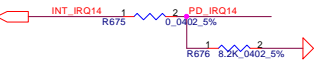
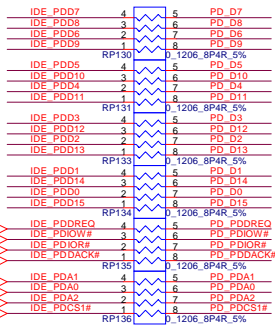


BTL MODE
R522/R525=0.419K
Vmax=0.201V , GAINmax=18db
Vmin=5V, GAINmin=-80db

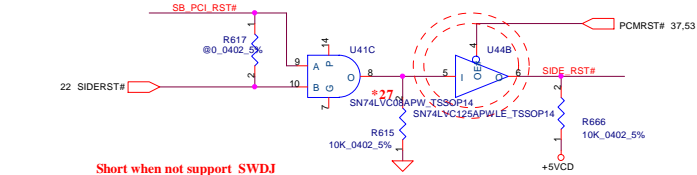
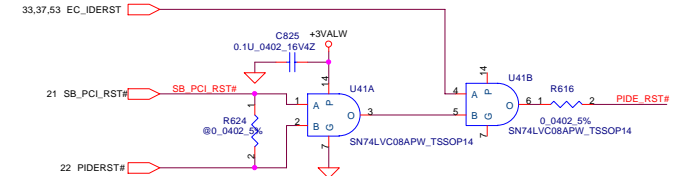
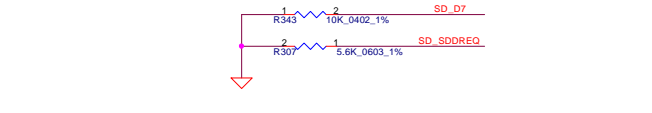
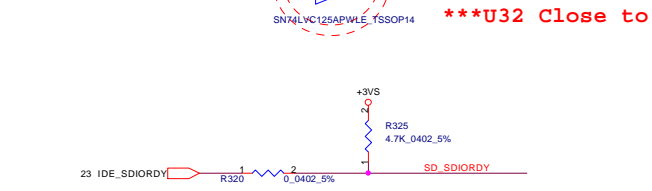
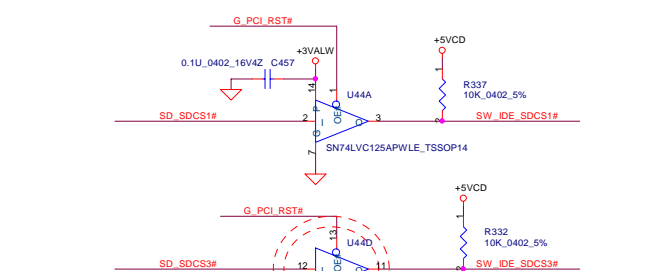
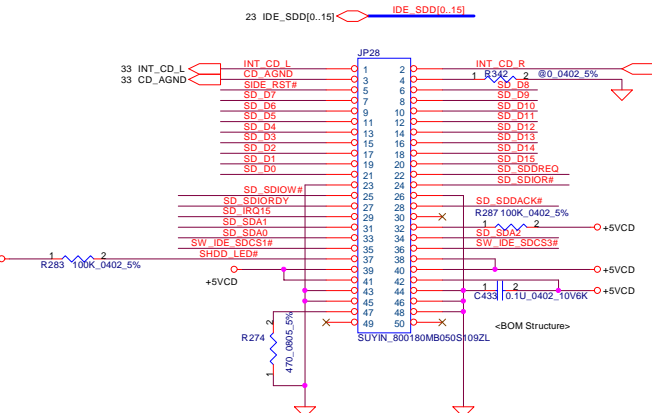
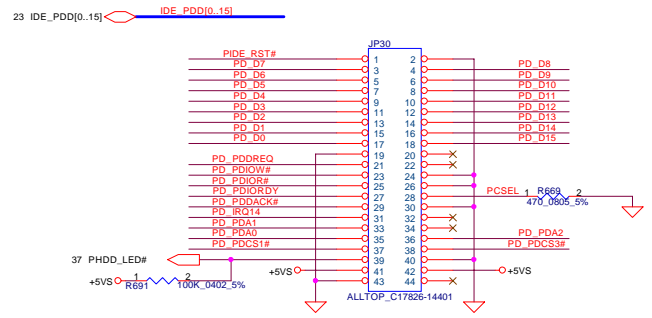
SE MODE
Vmax=1.53V , GAINmax=-6db
Vmin=5V, GAINmin=-80db

Compal Electronics, Inc.			
AMP & Audio Jack			
Title	Document Number		Rev
Size	Customer		0.1
Longbeach 100 <LA-2451>			
Date:	星期六, 十一月 06, 2004	Sheet	34 of 53

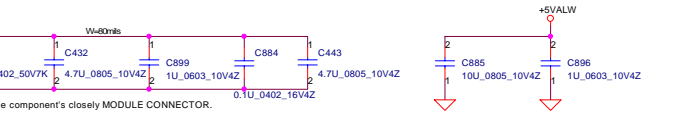
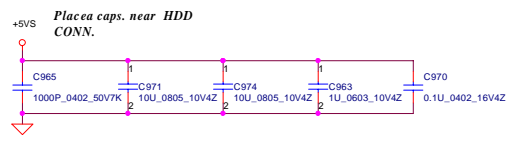
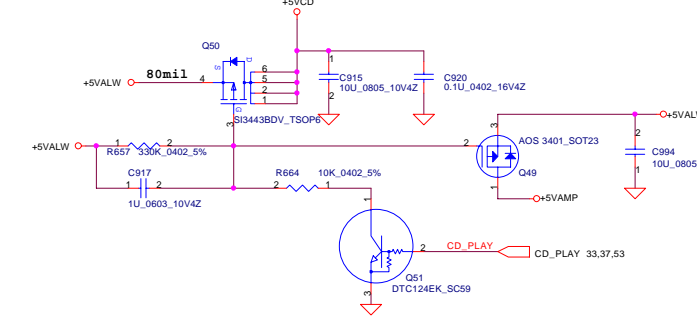
PROPRIETARY NOTE
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HDD CONNECTOR



Short when not support SWJD
Net width should be 60mil wide



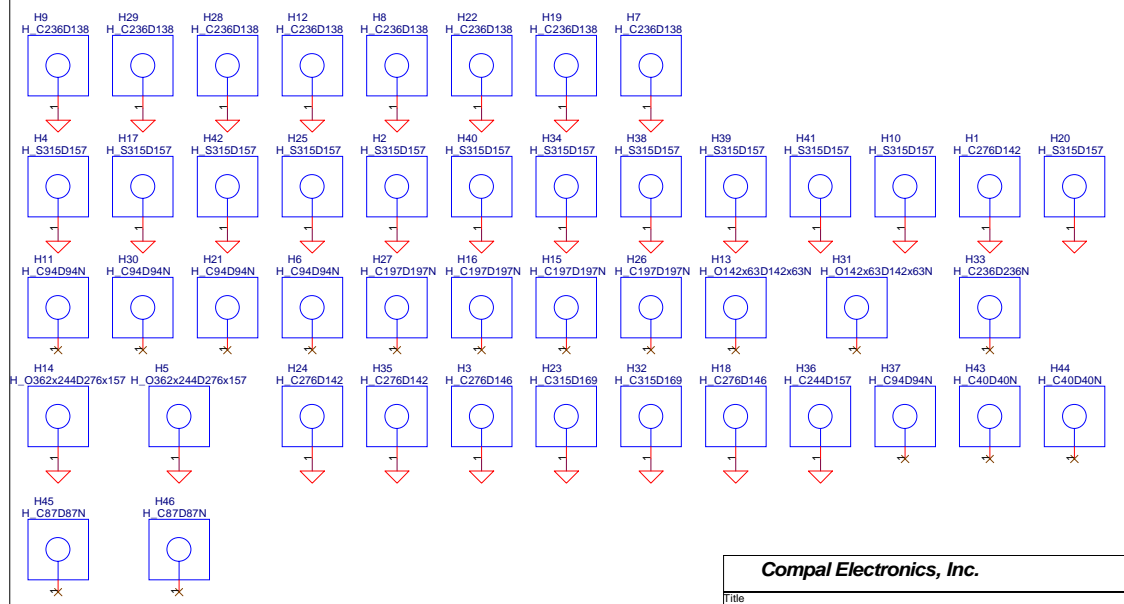
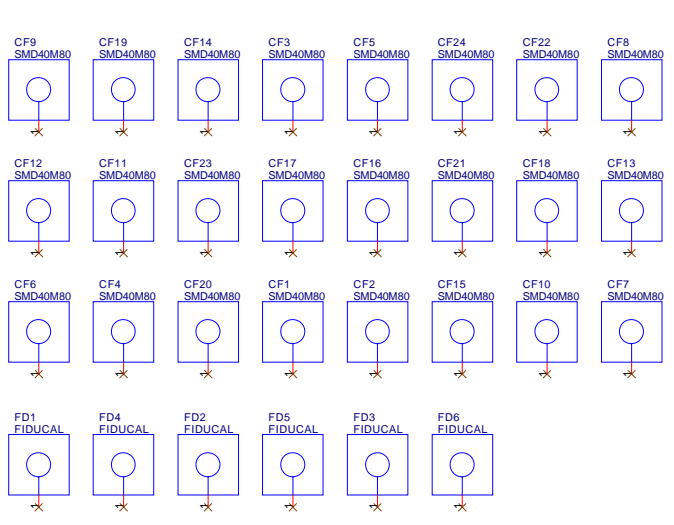
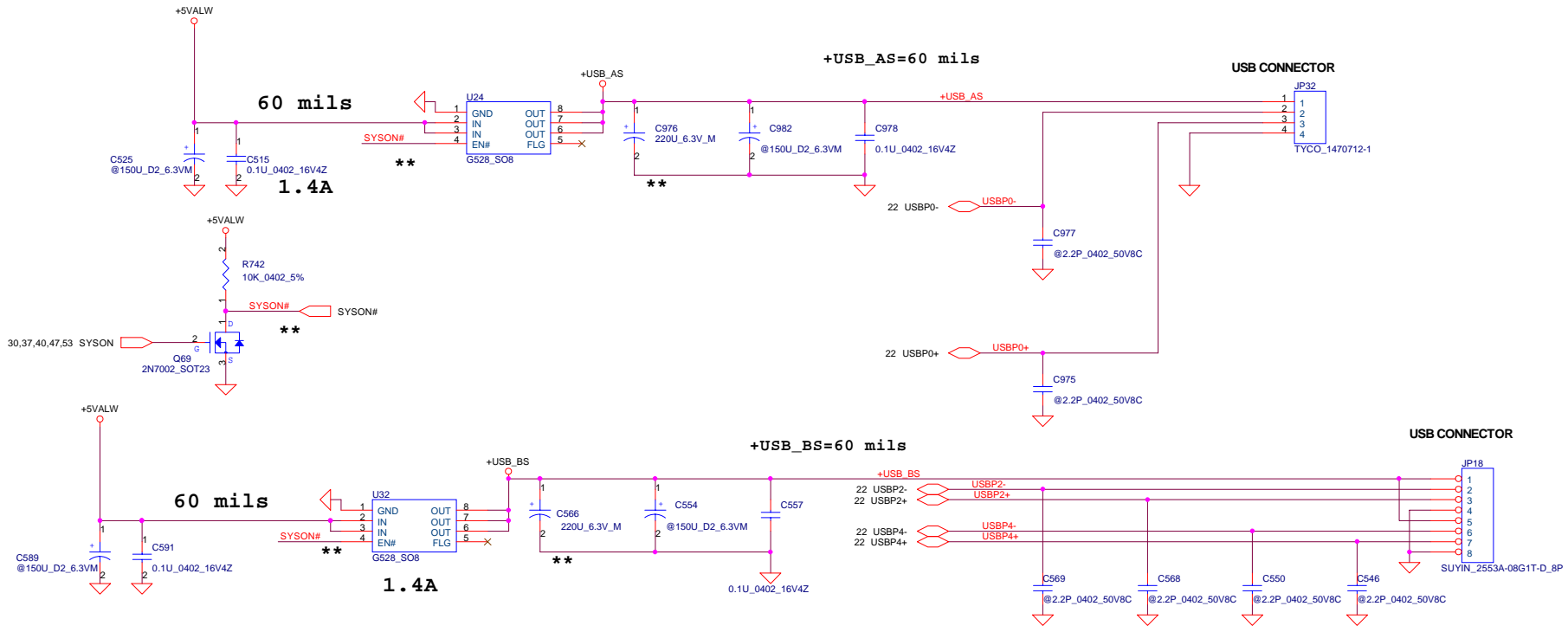
Place components closely MODULE CONNECTOR.

***U32 Close to CD-ROM Side

Compal Electronics, Inc.

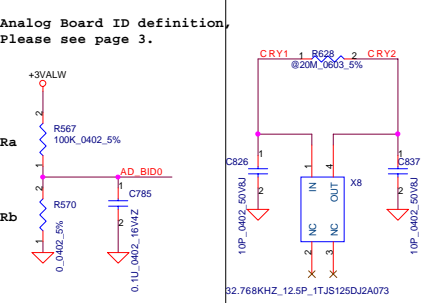
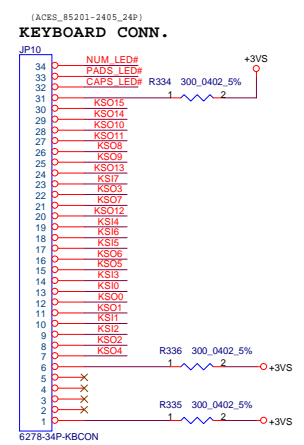
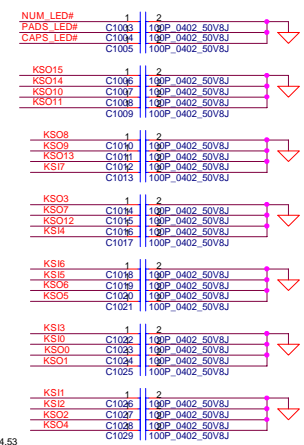
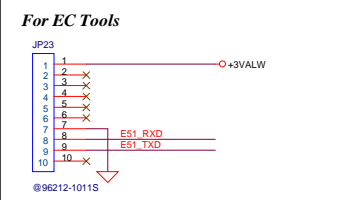
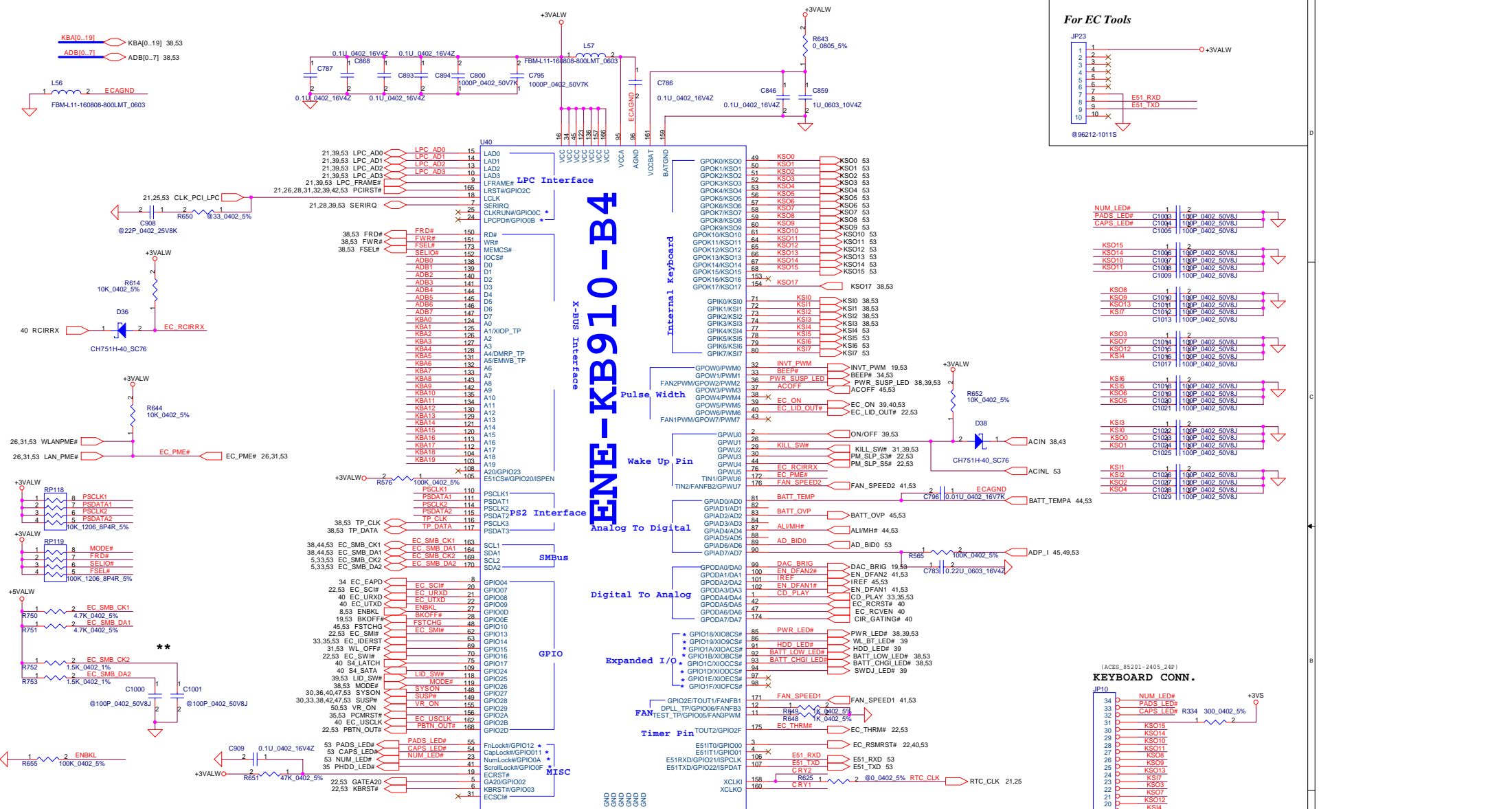
Title IDE/FDD MODULE CONN.		
Size Customer	Document Number Longbeach 100 <LA-2451>	Rev 0.1
Date: 星期六, 十一月 08, 2004	Sheet 35	of 53

Keep 20 mils minimum spacing between
USB signals and others signals

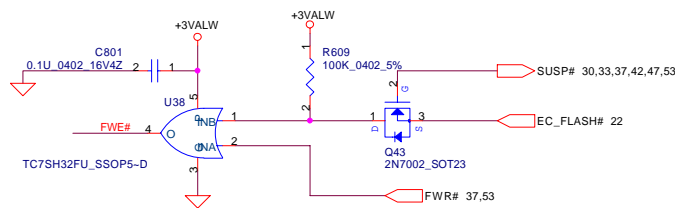
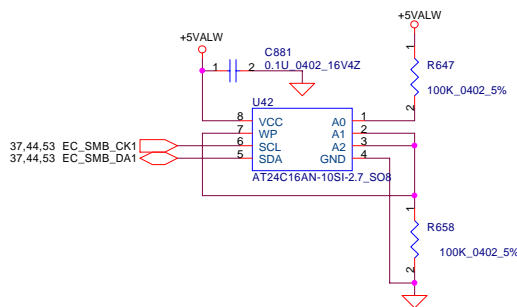


Compal Electronics, Inc.		
Title: USB Conn.		
Size: Longbeach 100 <LA-2451>	Document Number:	Rev: 0.1
Date: 星期六 十一月 706, 2004	Sheet: 36	of 53

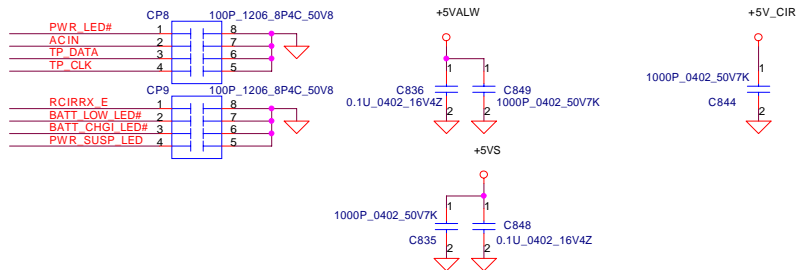
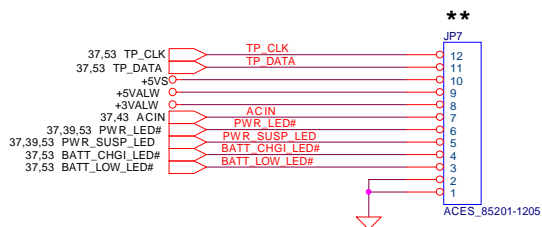
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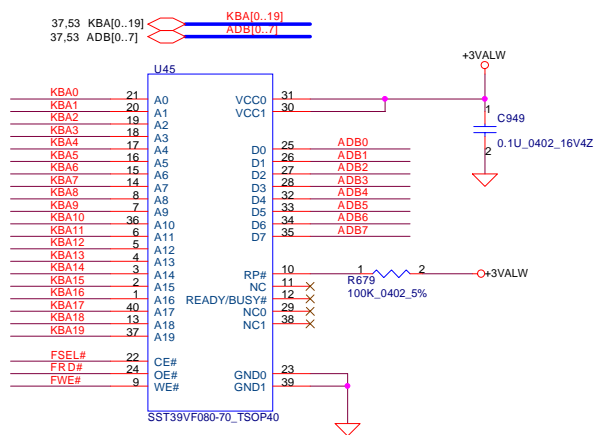
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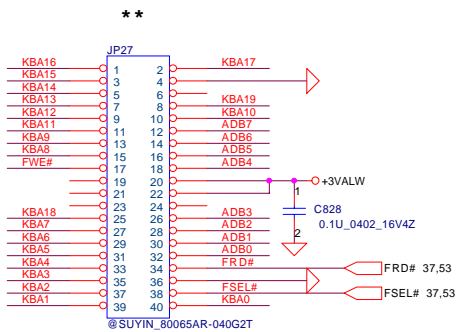
Touch Pad Connector



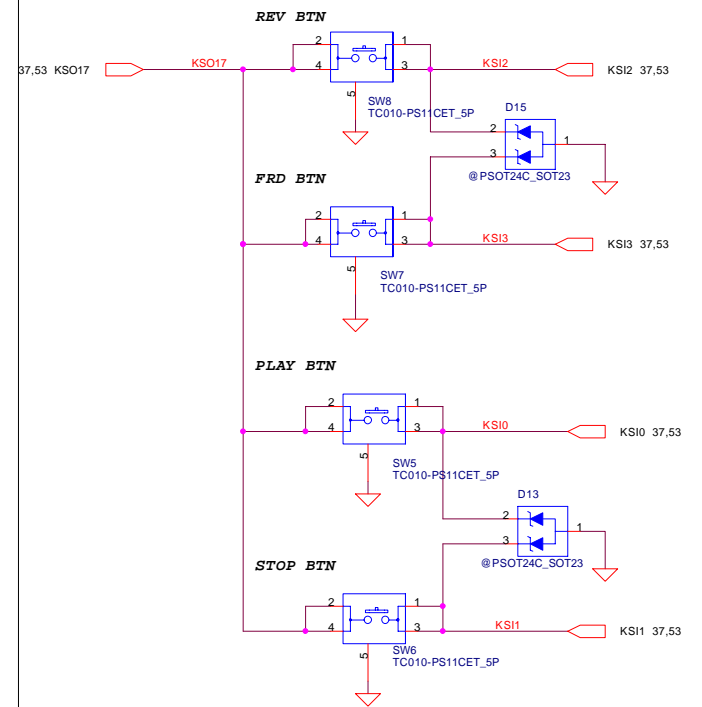
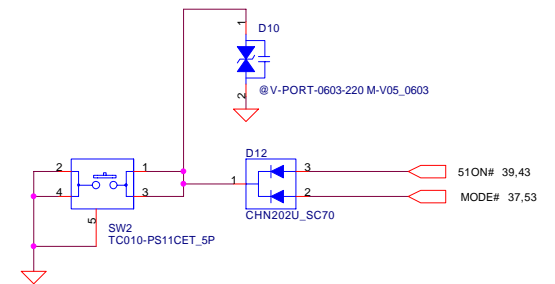
1MB Flash ROM



1MB BIOS Connector



Direct CD button

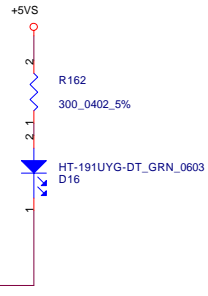


Compal Electronics, Inc.

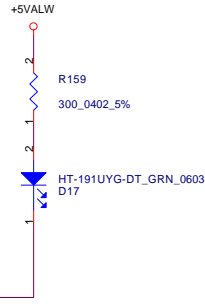
Title		
BIOS & EXT. I/O PORT		
Size	Document Number	Rev
Custom	Longbeach 100 <LA-2451>	0.1
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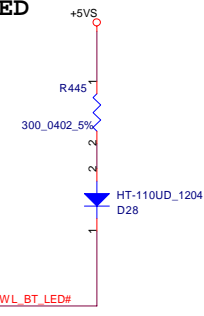
HDD LED



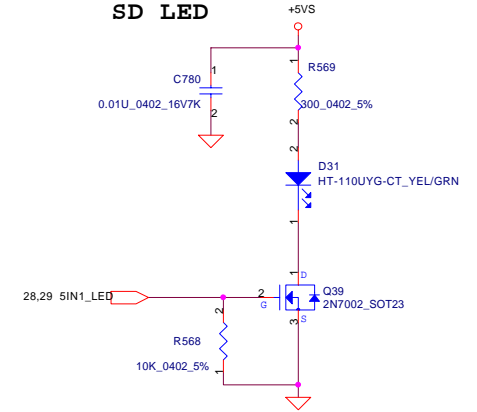
SWDJ LED



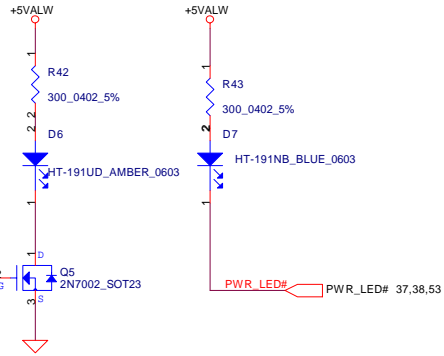
Wireless LED



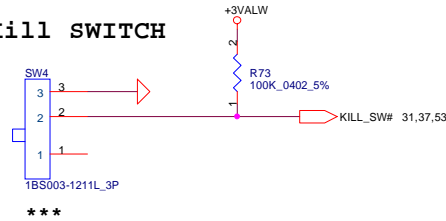
SD LED



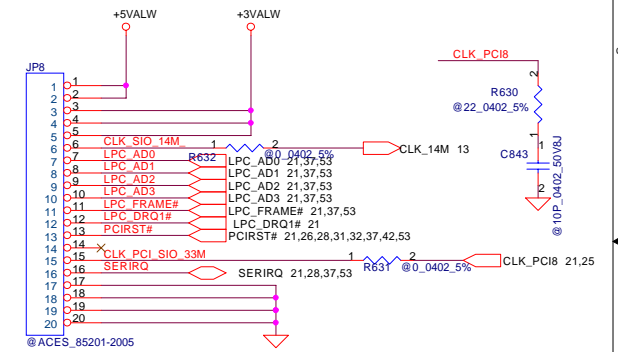
POWER LED



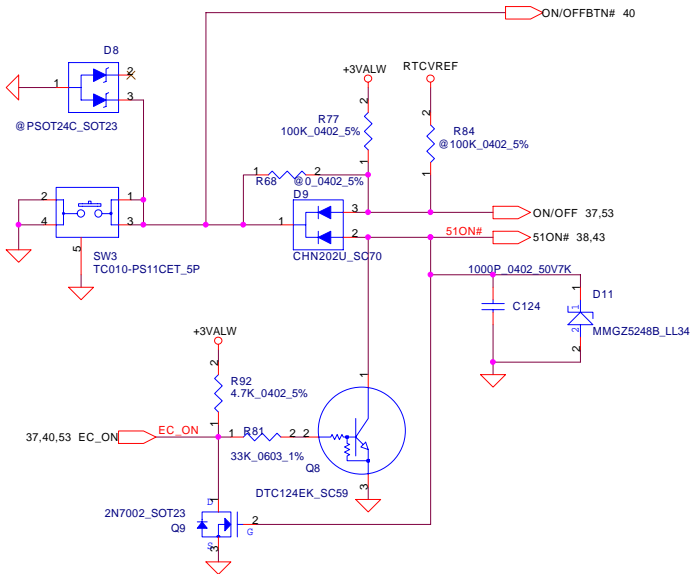
Kill SWITCH



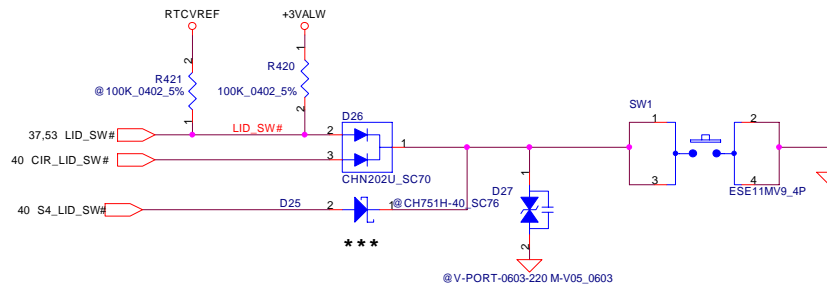
LPC Debug Port



Power Button



LID Switch

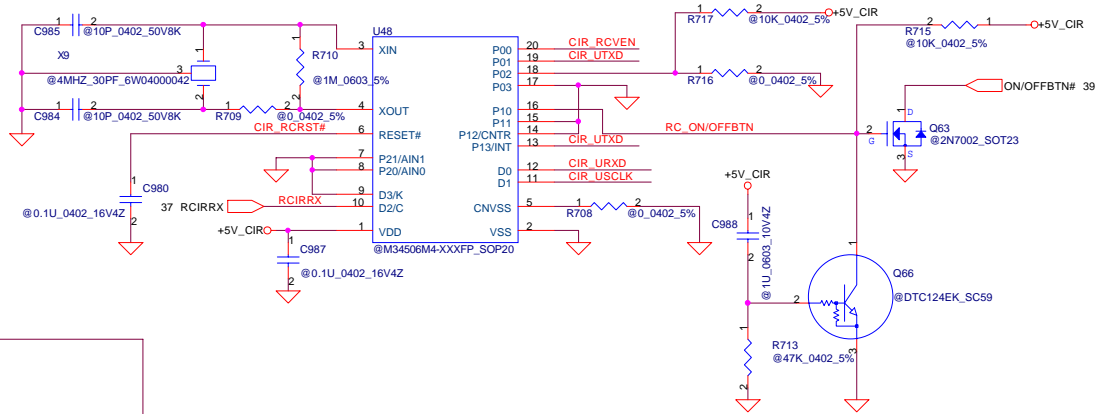
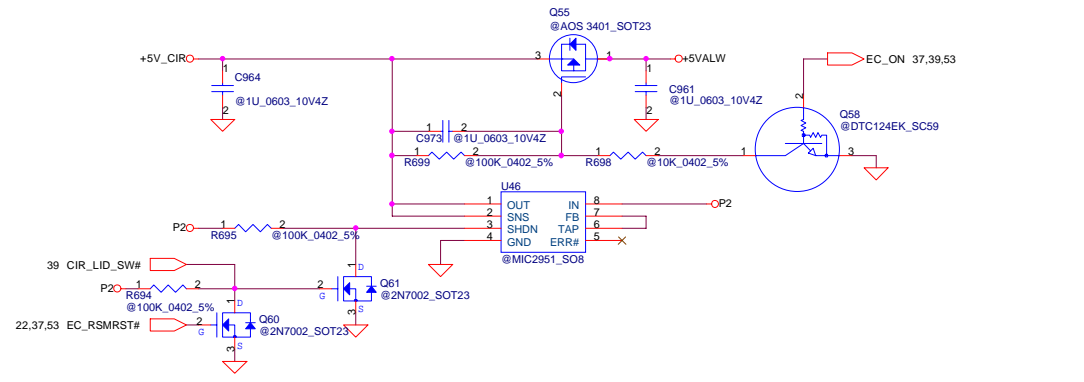
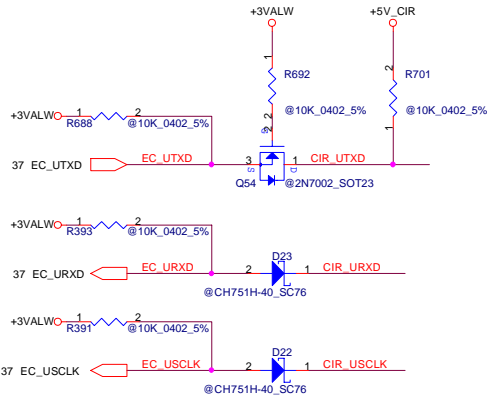


Compal Electronics, Inc.

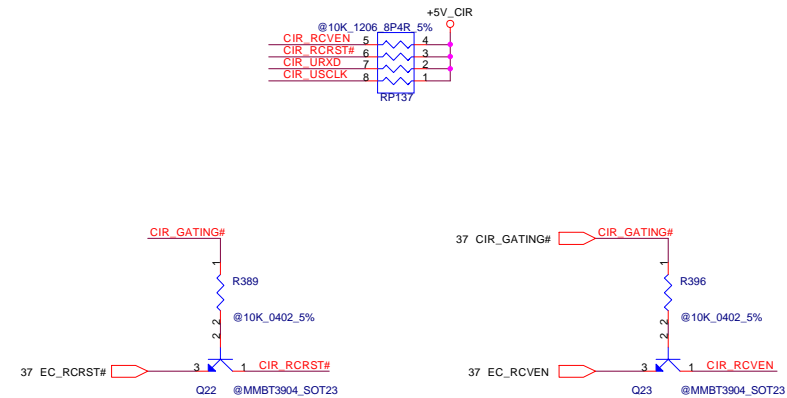
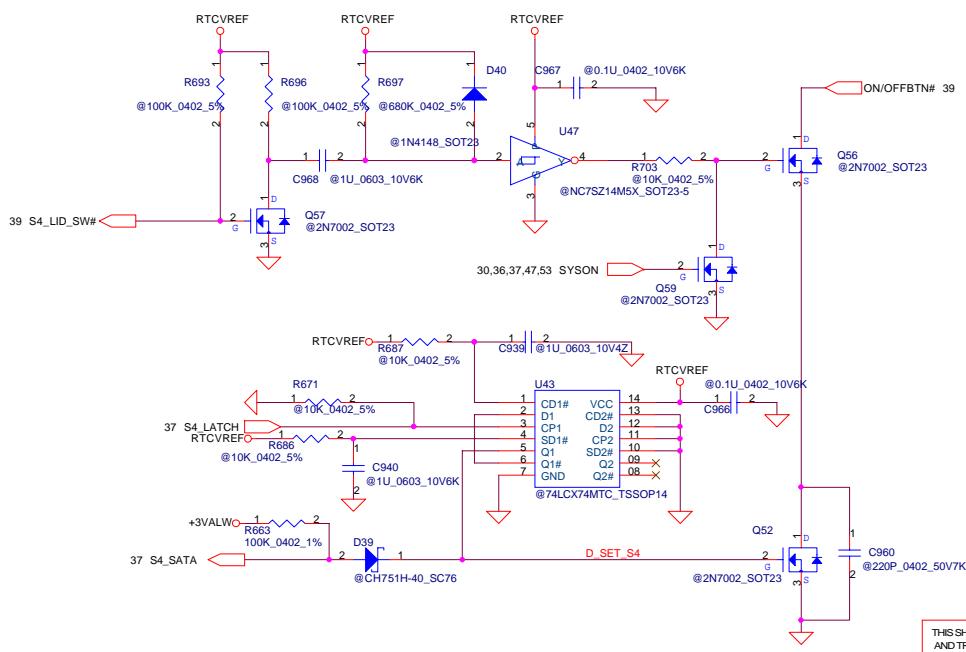
Switches & Connectors

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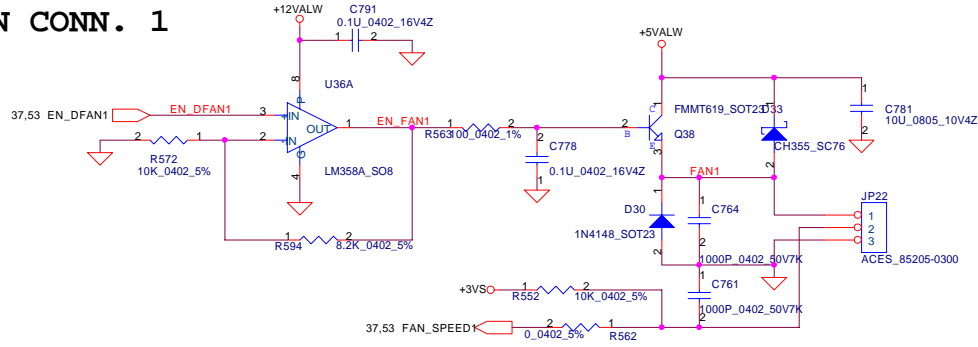
Battery mode Hibernation



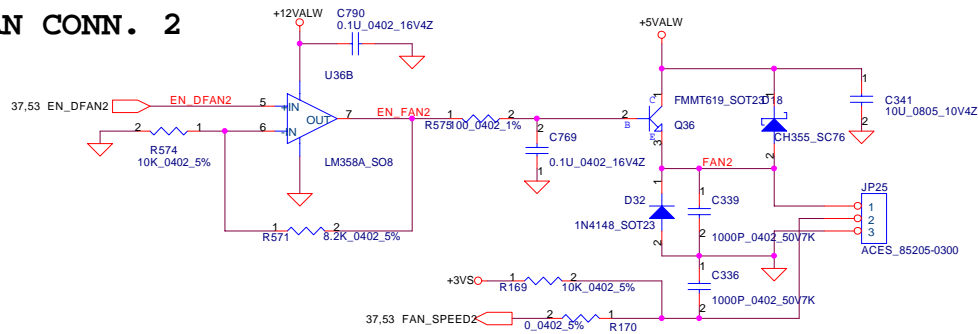
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Compal Electronics, Inc.			
Title: CIR & MDC			
Size: Cusontongbeach 100 <LA-2451>	Document Number: 220P_0402_51V7K	Rev: 0.1	
Date: 星期六, 十一月 06, 2004	Sheet: 40	of 53	

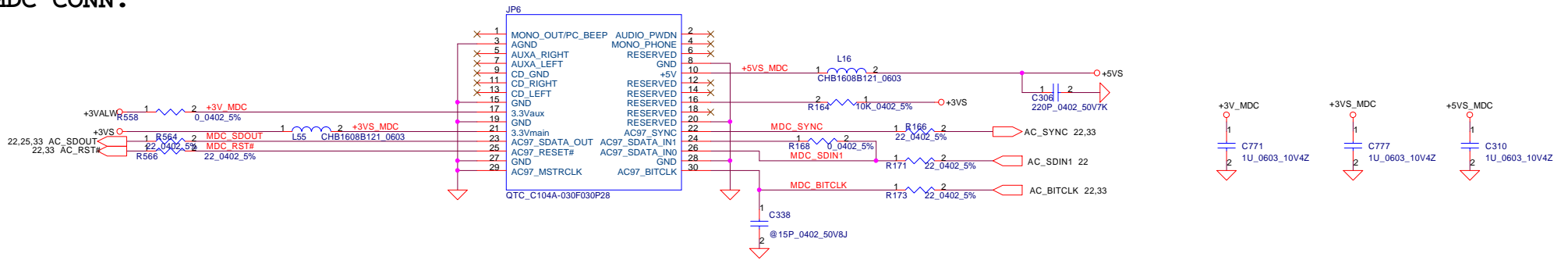
FAN CONN. 1



FAN CONN. 2



MDC CONN.



Compal Electronics, Inc.

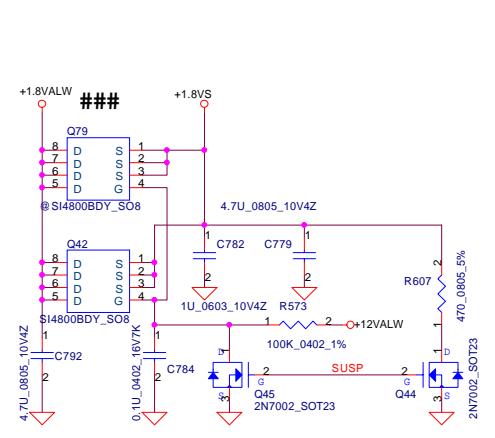
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Size: Document Number: Longbeach 100 <LA-2451> Rev: 0.1

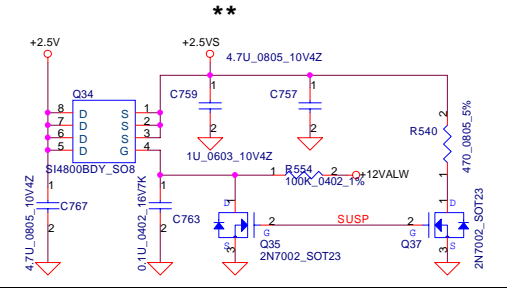
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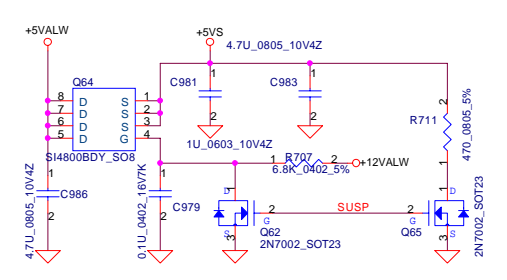
+1.8VALW TO +1.8VS



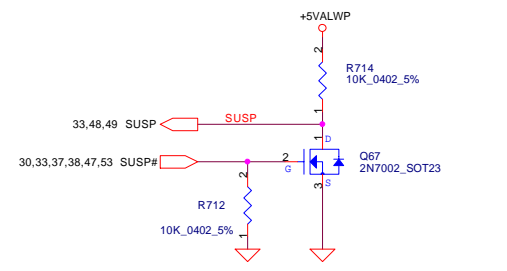
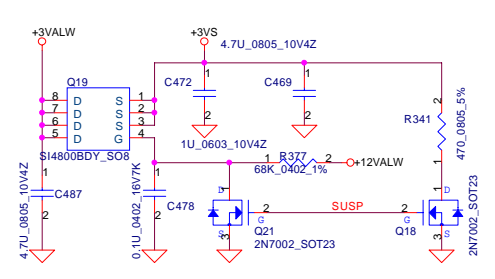
+2.5V TO +2.5VS



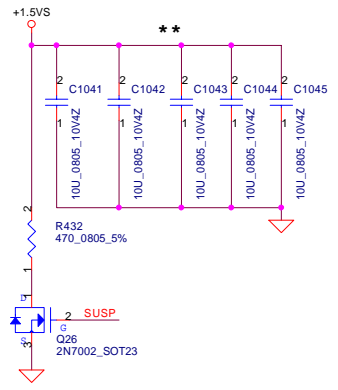
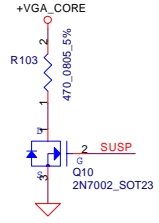
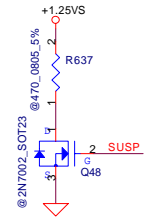
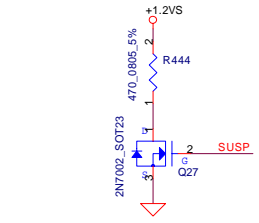
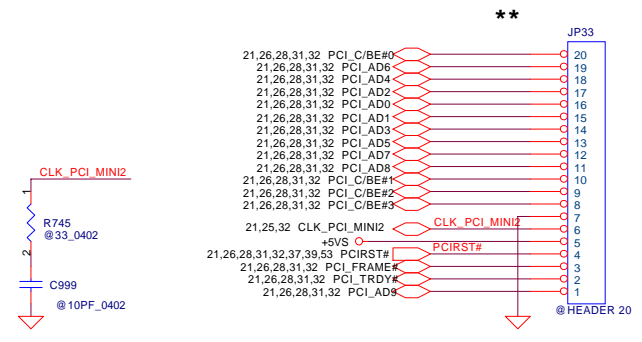
+5VALW TO +5VS

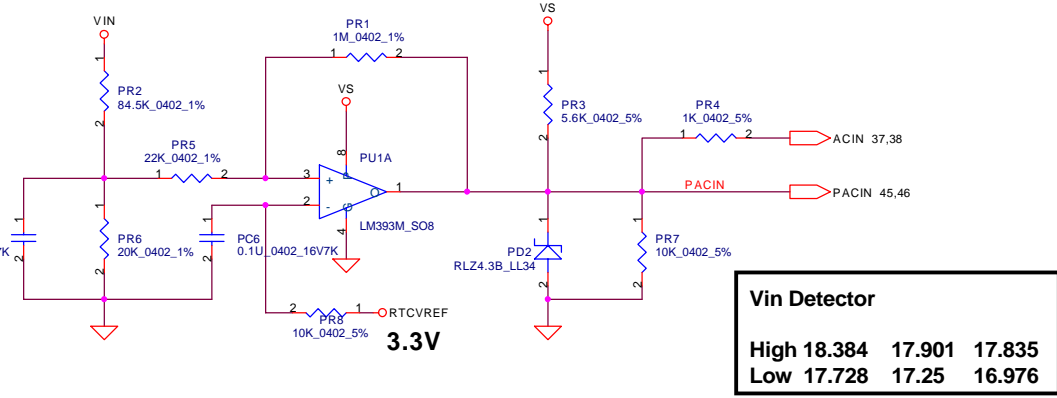
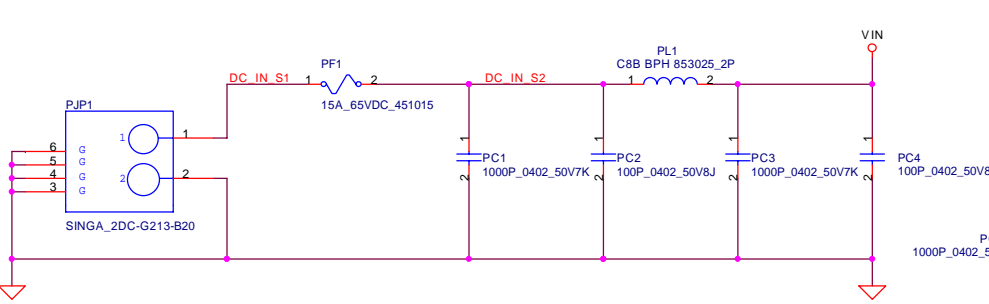


+3VALW TO +3VS

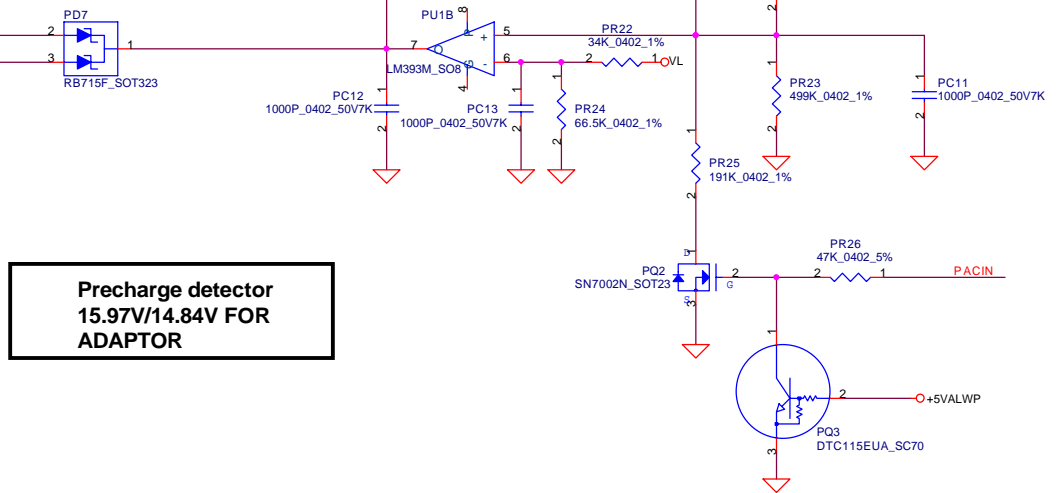
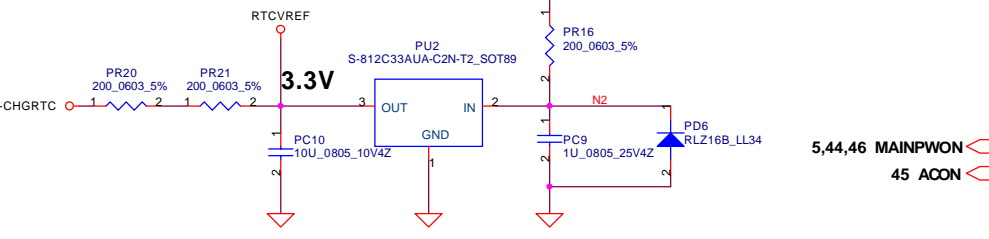
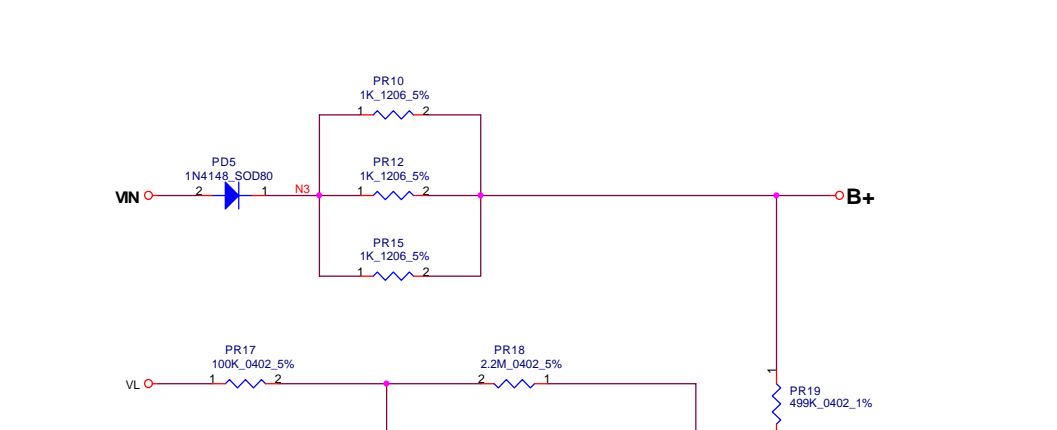
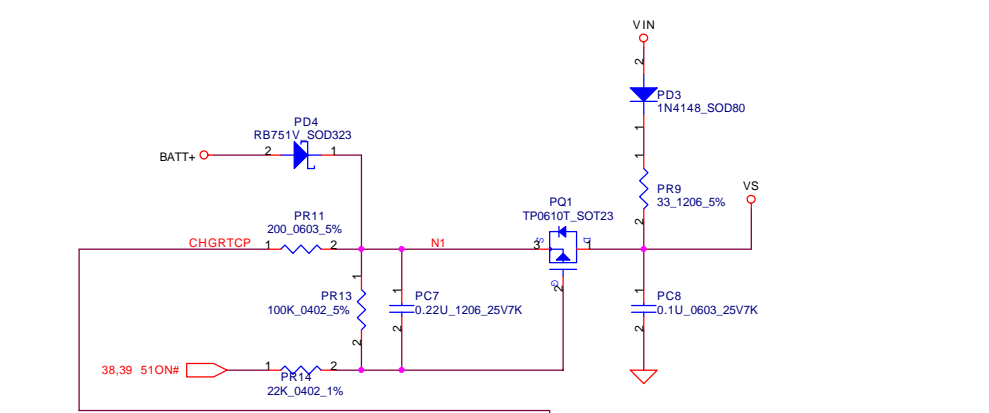


Port 80 Debug Card Connector

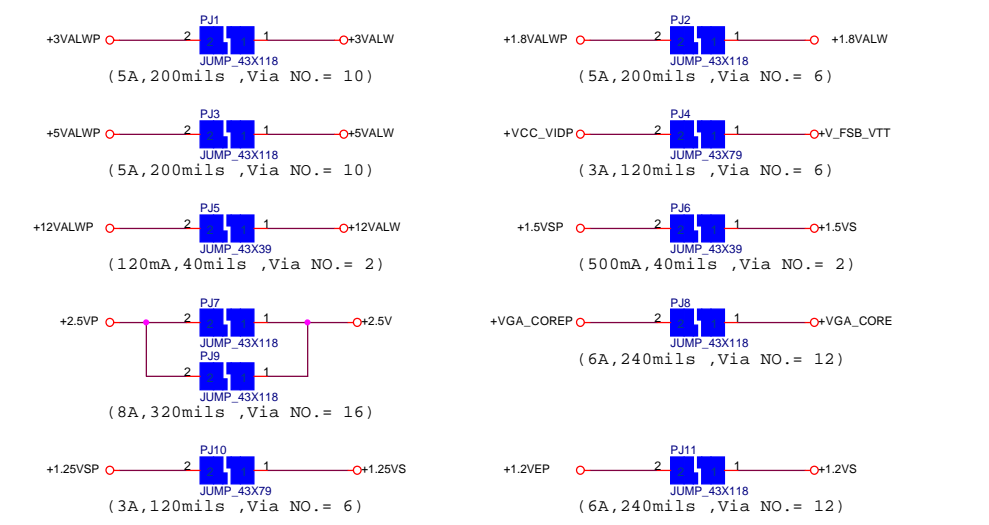




Vin Detector
High 18.384 17.901 17.835
Low 17.728 17.25 16.976



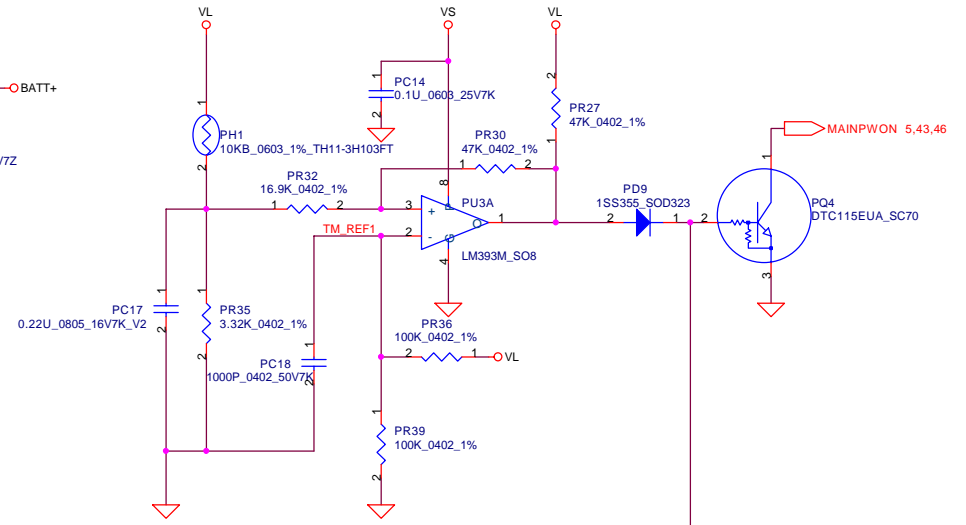
Precharge detector
15.97V/14.84V FOR
ADAPTOR



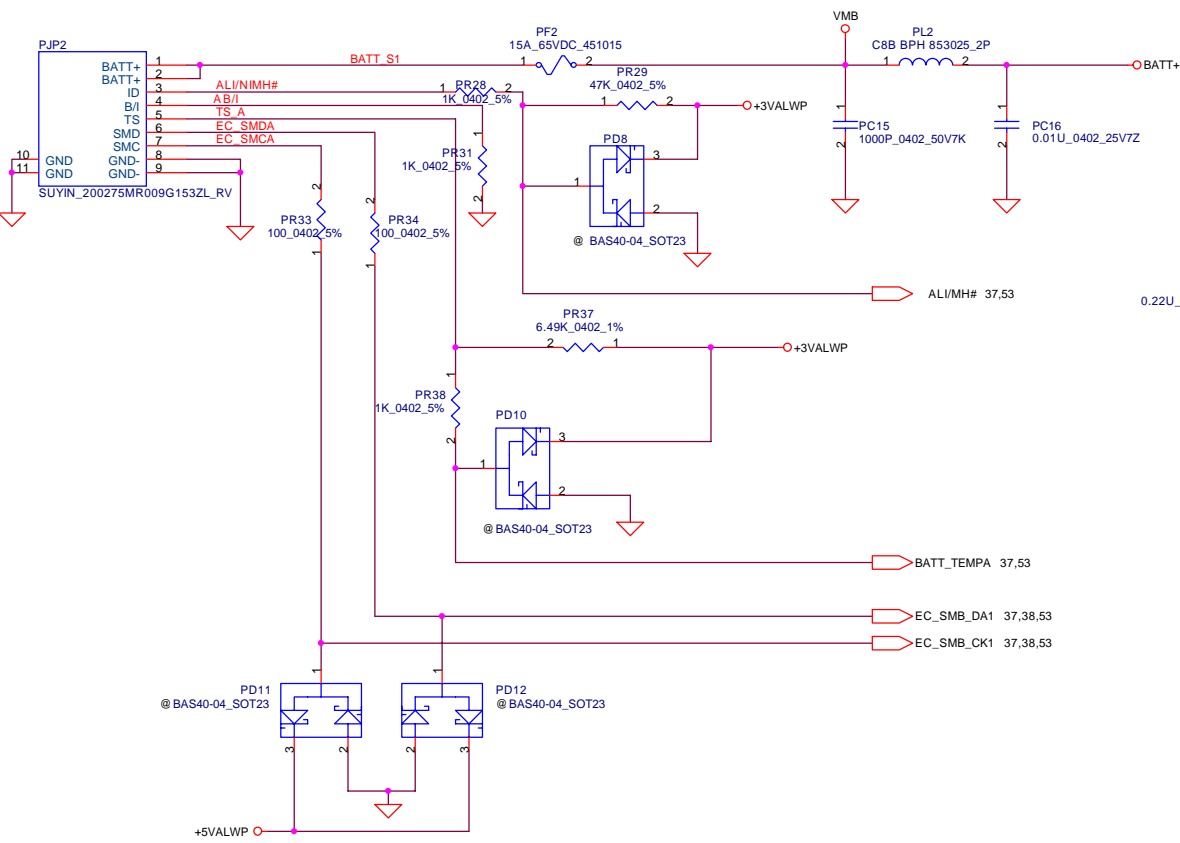
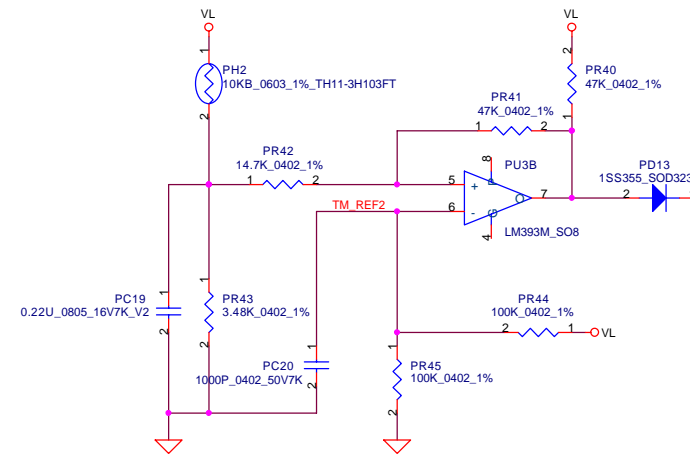
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Compal Electronics, Inc.		
DCIN & DETECTOR		
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PH1 under CPU bottom side :
 CPU thermal protection at 84 degree C
 Recovery at 45 degree C

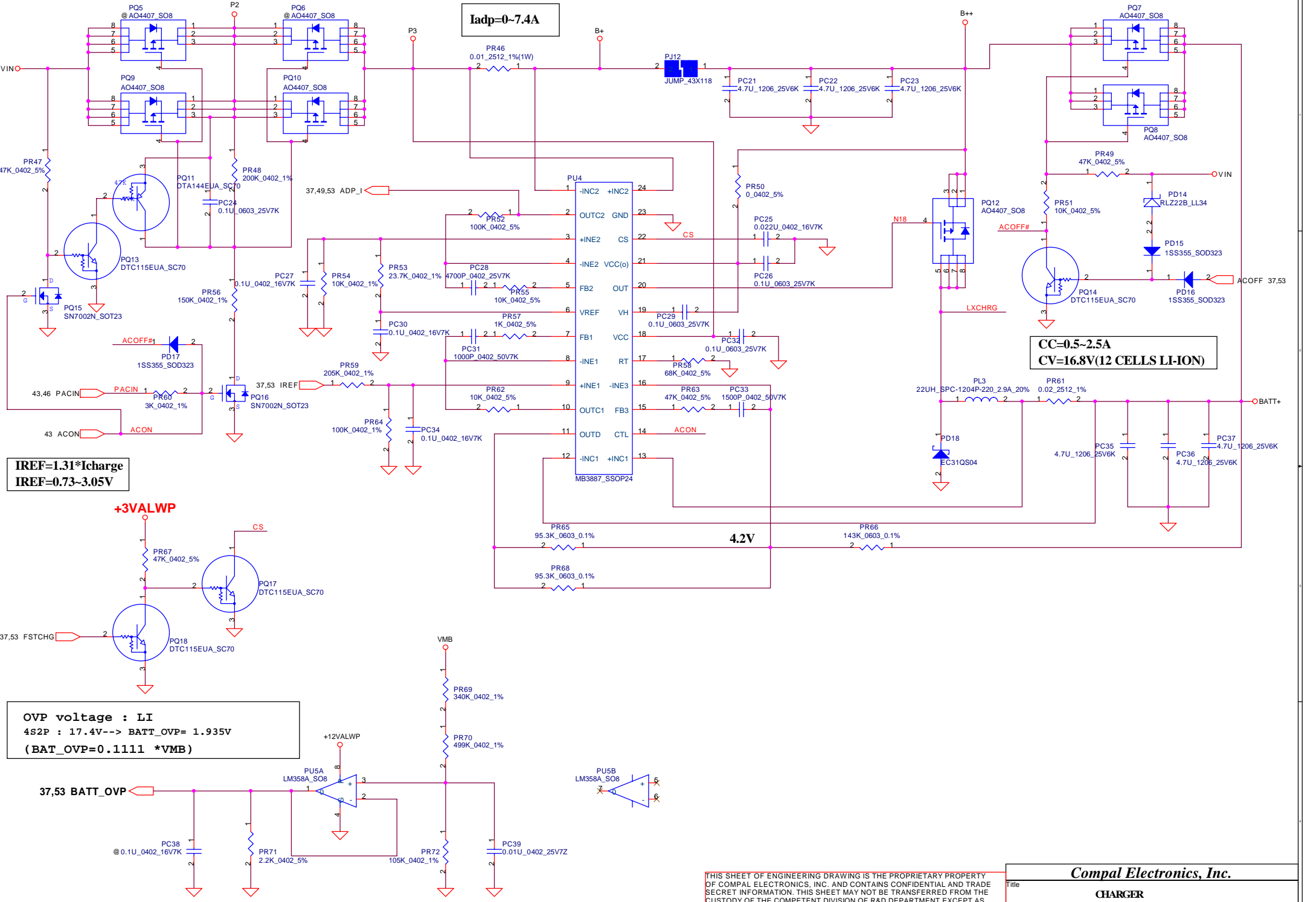


PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 45 degree C



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Compal Electronics, Inc.		
BATTERY CONN/OTP		
Size	Document Number	R ev
	Longbeach100	0.1
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I_{adp}=0~7.4A

**CC=0.5~2.5A
CV=16.8V(12 CELLS LI-ION)**

**I_{REF}=1.31*I_{charge}
I_{REF}=0.73~3.05V**

+3VALWP

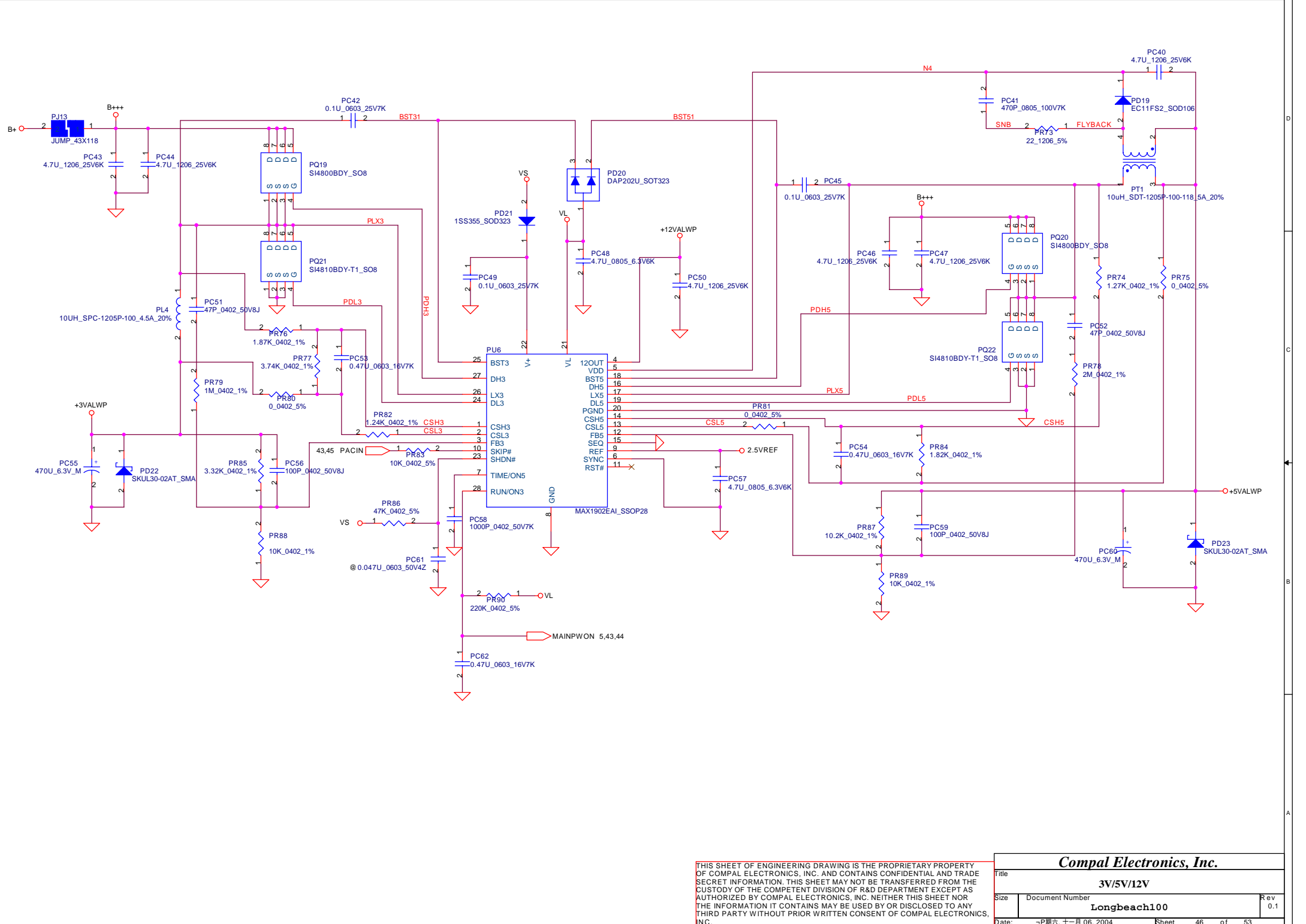
4.2V

**OVP voltage : LI
4S2P : 17.4V--> BATT_OVP = 1.935V
(BATT_OVP=0.1111 *VMB)**

37,53 BATT_OVP

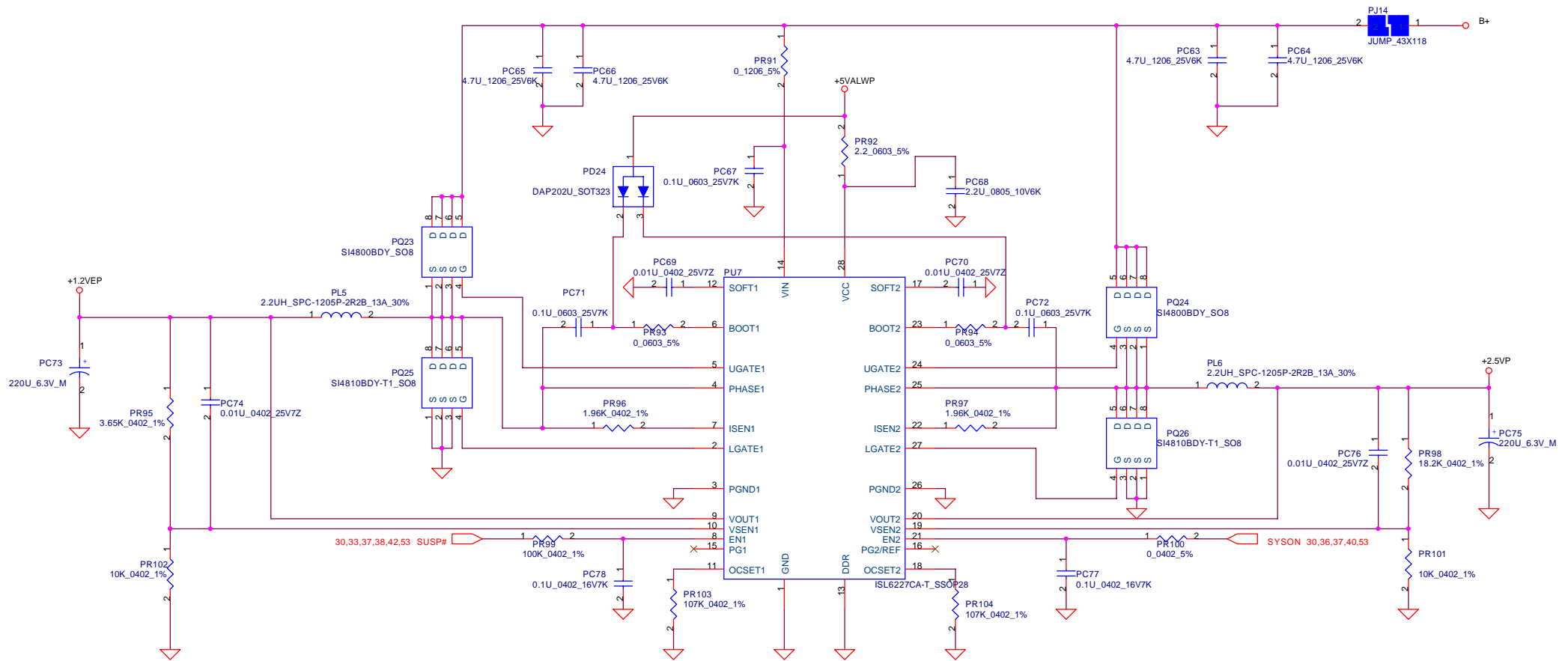
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Compal Electronics, Inc.		
CHARGER		
Size	Document Number	Rev
	Longbeach100	0.1
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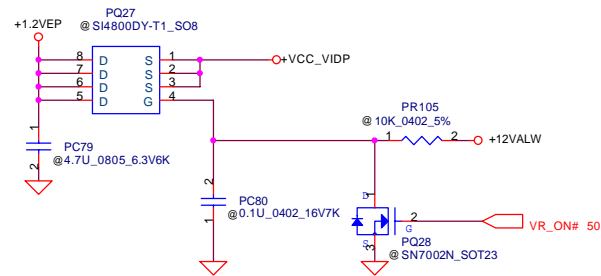


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Title 3V/5V/12V		
Size	Document Number Longbeach100	Rev 0.1
Date:	~P期六, 十一月 06, 2004	Sheet 46 of 53

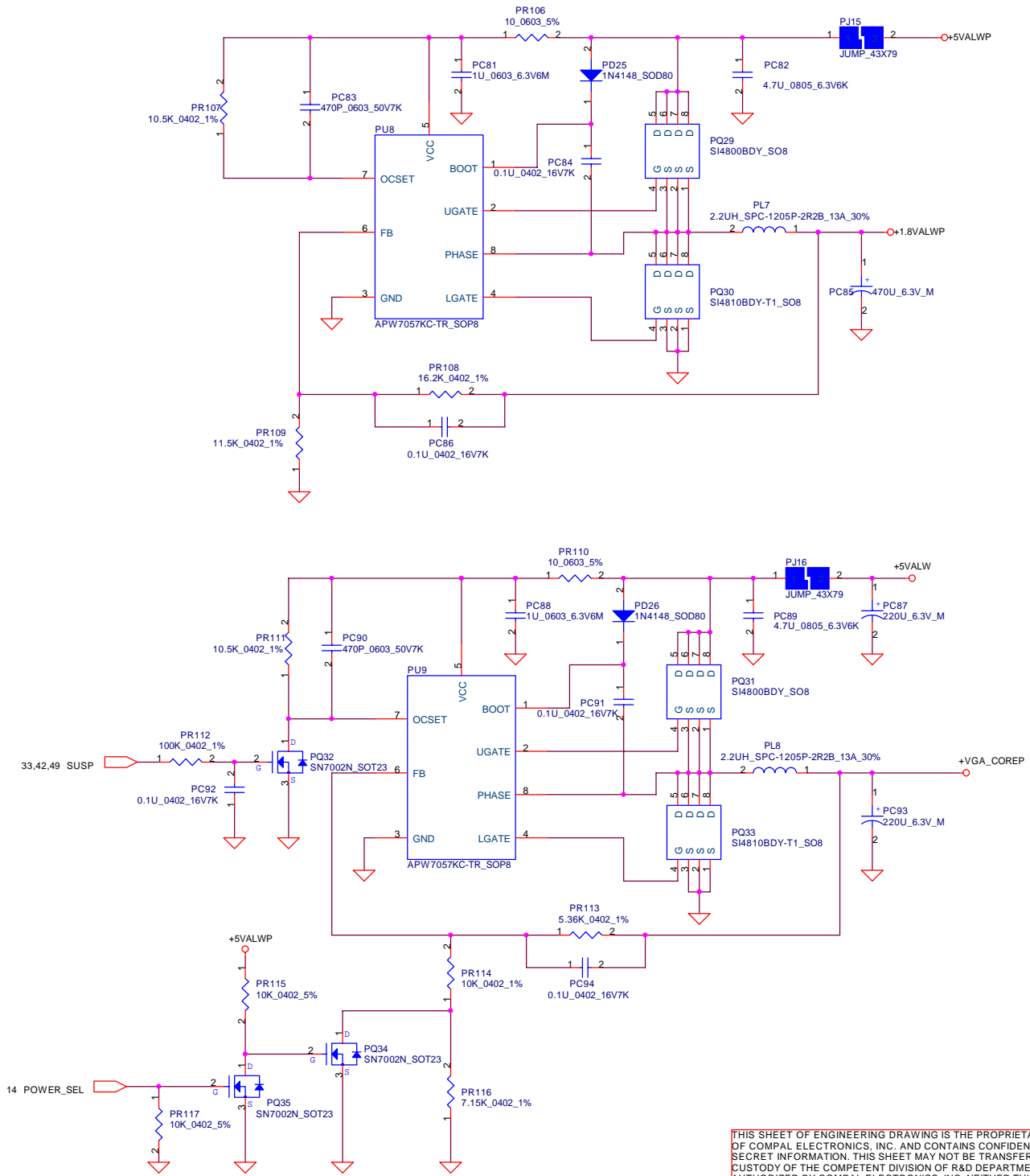


+1.2VEP TO +VCC_VIDP



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Compal Electronics, Inc.		
Title DDR_2.5V/1.2VEP		
Size	Document Number Longbeach100	R ev 0.1
Date	-P 翻六, 十一月 06, 2004	Sheet 47 of 53

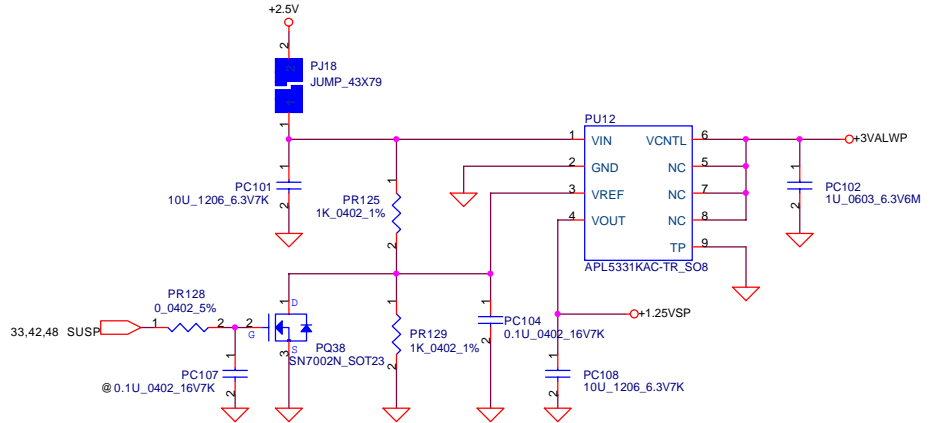
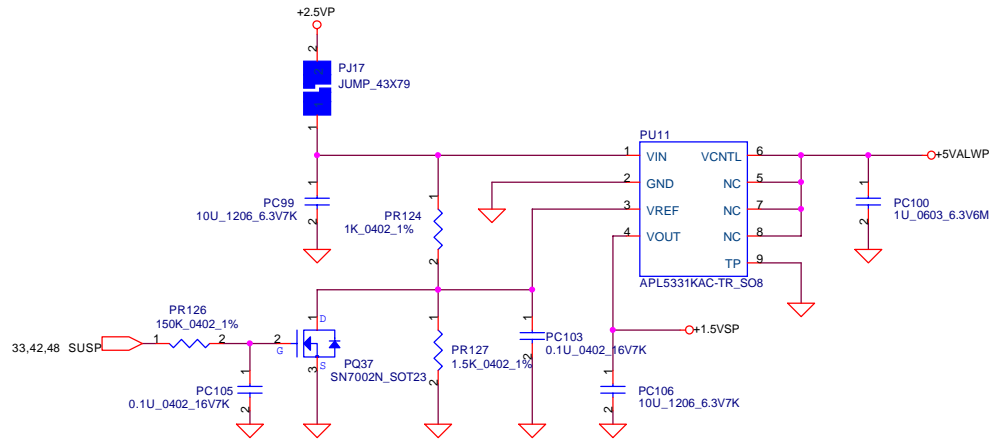
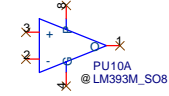
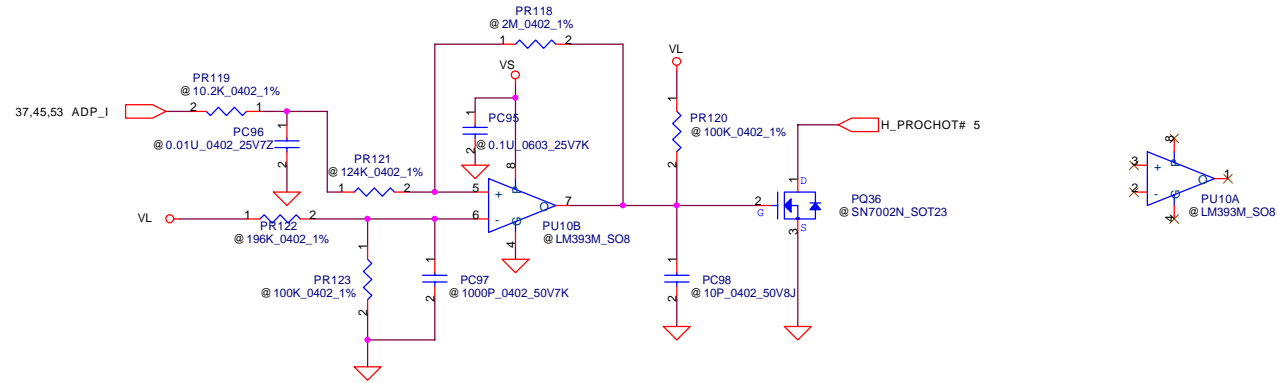


	M24/1.2V	M22/1.15V
PR113	5.36K	3.92K
PR114	10K	8.87K
PR116	7.15K	6.81K

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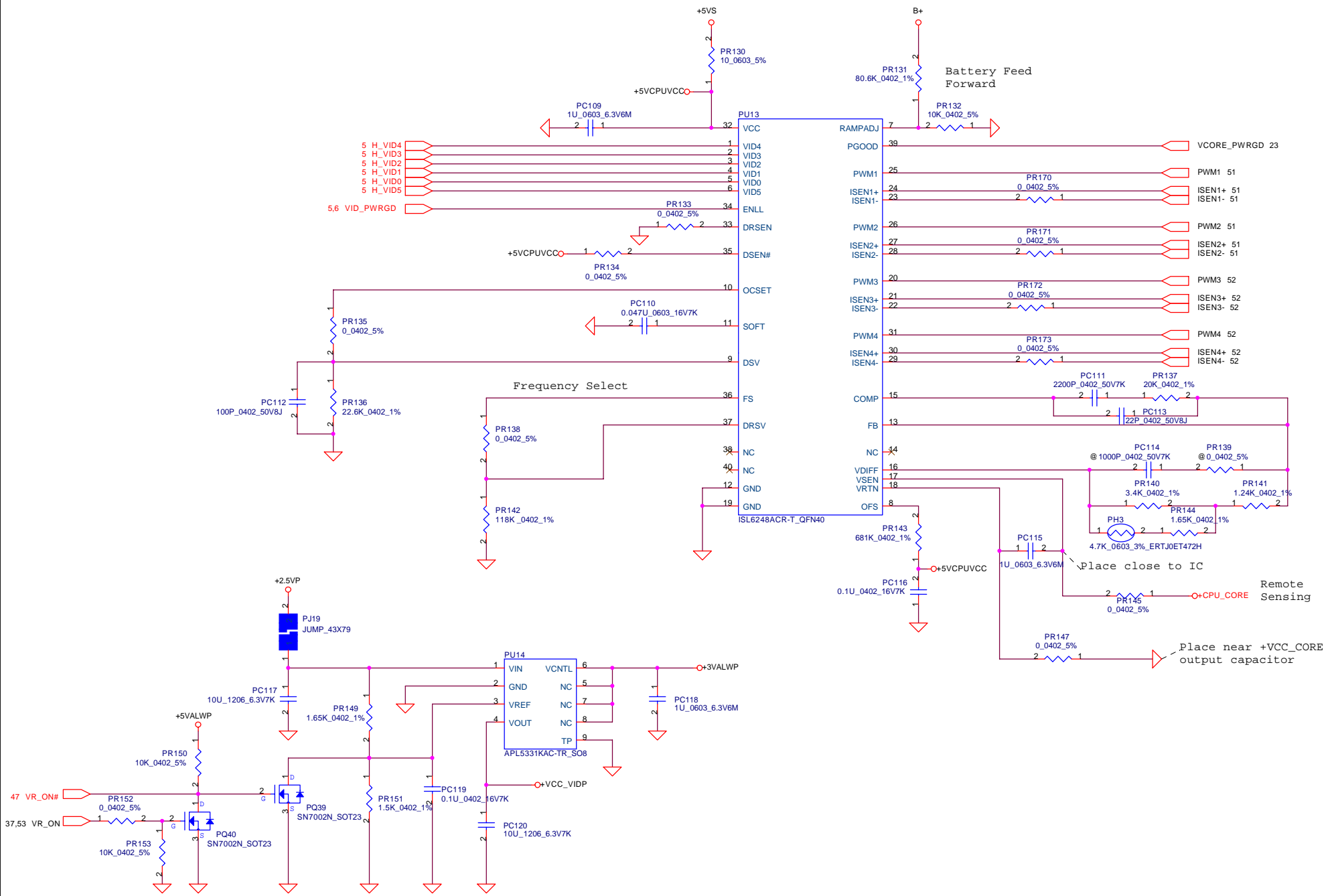
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Title		18V/VGA	
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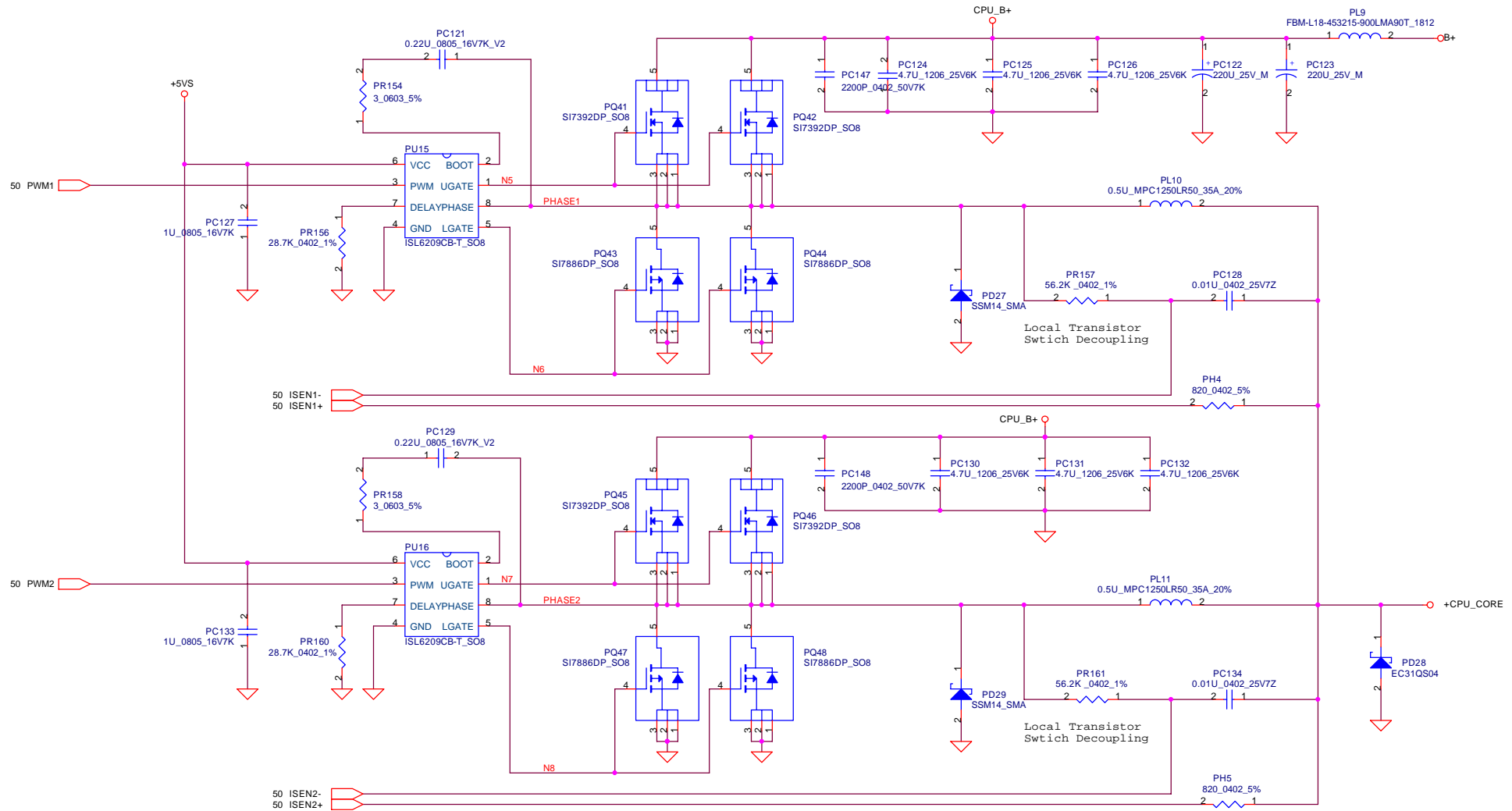
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Compal Electronics, Inc.		
Title 1.5V/1.25V/PROCHOT		
Size	Document Number Longbeach100	Rev 0.1
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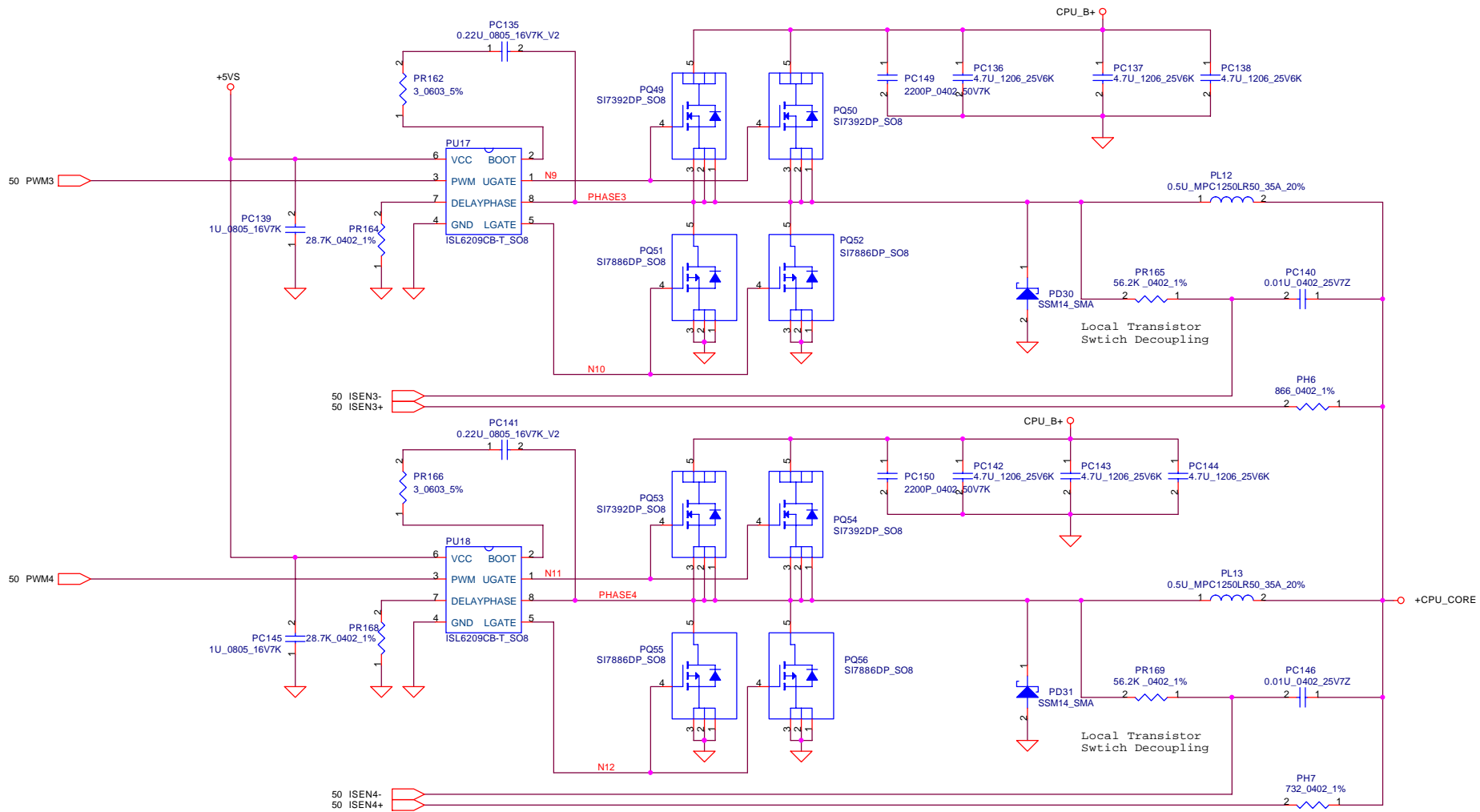
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Compal Electronics, Inc.		
Title		
CPU_CORE (1)		
Size	Document Number	Rev
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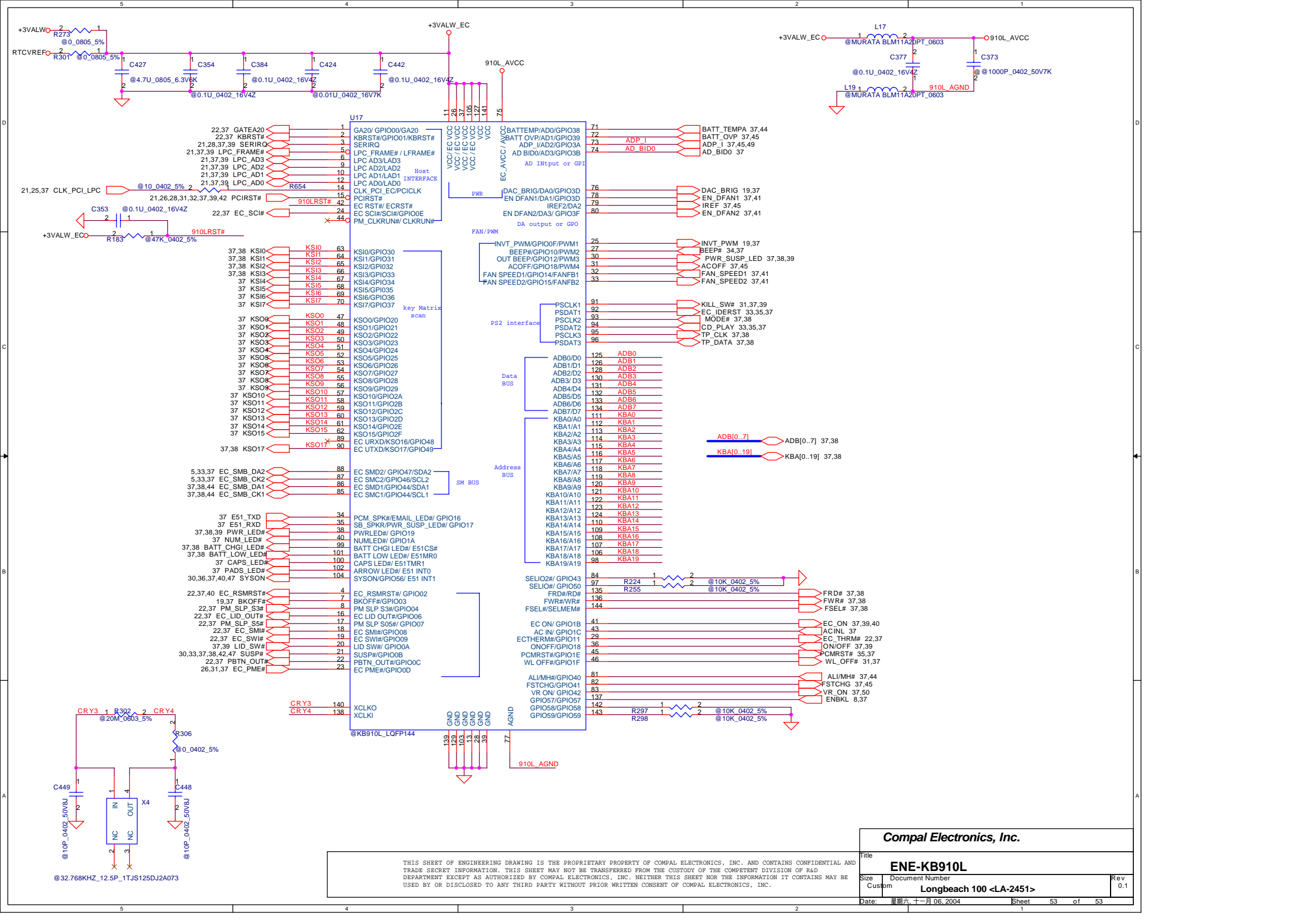
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Title		
CPU_CORE (1)		
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Compal Electronics, Inc.		
Title CPU_CORE (2)		
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Compal Electronics, Inc.		
Title ENE-KB910L		
Size Custom	Document Number Longbeach 100 <LA-2451>	Rev 0.1
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