1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
16	0001345356	ENGINEERING RELEASED	2012-01-19

D7i MLB

LAST_MODIFIED=Thu Jan 19 17:56:04 2012

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-9179	1	SCH,MLB,K70I	SCH	CRITICAL	
820-3172	1	PCBF,MLB,K70I	PCB	CRITICAL	

DRAWING
TITLE=K22
ABBREV=DRAWING
LAST_MODIFIED=Thu Jan 19 17:56:04 2012

DRAWING TITLE: SCH,D7i,MLB

Apple Inc.

DRAWING NUMBER: 051-9179 | SIZE: D
REVISION: 16.0.0
BRANCH:
PAGE: 1 OF 113
SHEET: 1 OF 90

System Block diagram can be found on Kismet

PATH: Kismet > K70/72 > Block Diagrams > K70 Block Diagram

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE: System Block Diagram

Apple Inc.

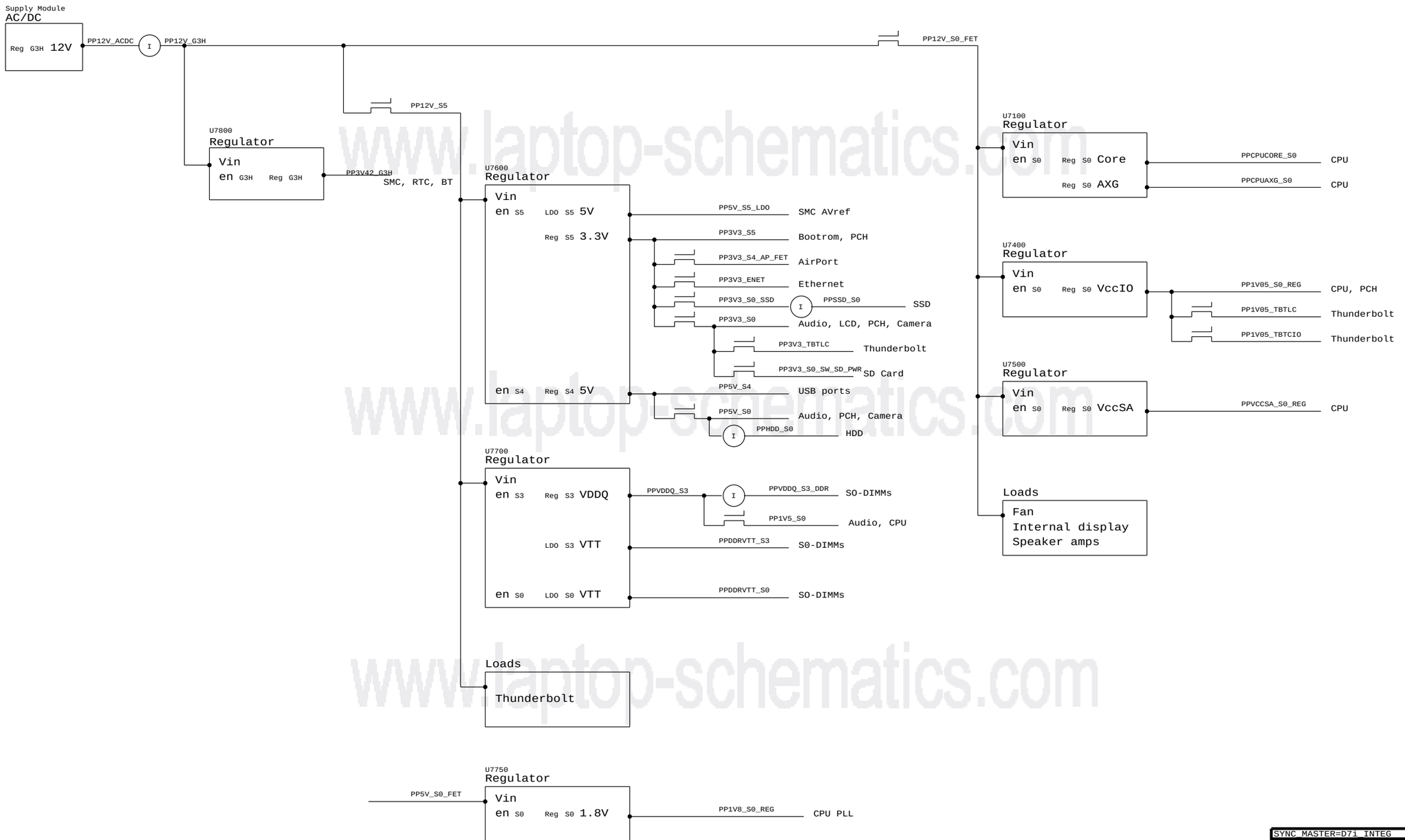
DRAWING NUMBER: 051-9179 SIZE: D

REVISION: 16.0.0

BRANCH:

PAGE: 2 OF 113

SHEET: 2 OF 90



SYNC_MASTER=D71 INTEG SYNC_DATE=N/A

PAGE TITLE
Power Block Diagram

Apple Inc.

DRAWING NUMBER 051-9179 SIZE D
REVISION 16.0.0
BRANCH
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-2676	PCBA,MLB,D7I	D7_COMMON,CPU:4C_2P9GHZ_GFX2C,EEEE:DPQ5
085-3567	PCBA,MLB,DEV,D7I	DEVELOPMENT,D7_DEVEL,SSD:Y

Bar Code Labels / EEEE #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7122	1	MLB LABEL,48.0X4.8	EEEE_DPQ5	CRITICAL	EEEE:DPQ5

BOM Groups

BOM GROUP	BOM OPTIONS
D7_COMMON	COMMON,ALTERNATE,D7_COMMON1,D7_COMMON2,D7_PROGPARTS
D7_COMMON1	XDP,RSMRST:SMC,SPEAKERID,TBTHV:P12V
D7_COMMON2	SNS_CPUCORE:3PHASE,CPUCOREDRV:ISL6612,IG:Y,SNS_VDDQS3_DDR:Y
D7_PROGPARTS	SMC:PROG,BOOTROM:PROG,T29ROM:PROG,CIVROM:PROG,CAMROM:PROG
D7_DEVEL	XDP_CONN,LPCPLUS,VREFMRGN:EXT,BKLT_PWM,DEVEL_SENSORS,DEVEL_AUDIO
DEVEL_SENSORS	TEMPSNSDEV
D7_PRODUCTION	VREFMRGN:N,SSD:N

Add 'D7_PRODUCTION' at RevA release

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
337S4189	1	IVB,QBQ1,ES2,K0,2.4G,65W,2+2,0.9,3M,LGA	CPU	CRITICAL	CPU:2C_2P4GHZ_GFX2C	Old POR was 2C CPU
337S4258	1	IVB,QC48,QS,E1,2.9G,65W,4+2,1.10,6M,LGA	CPU	CRITICAL	CPU:4C_2P9GHZ_GFX2C	Temporary until a better 4C GT2 part is pulled

Module Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4277	1	IC,PANTHER POINT,C1,SLJC7,PRQ,BD82Z77	U1800	CRITICAL	
338S1047	1	IC,TBT,CR-4C,ES1,288 FCBGA,12X12MM	U3600	CRITICAL	
343S0592	1	IC,BCM57766,ENET&SD,a0,8X8	U3900	CRITICAL	

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
341S3493	1	IC,CR,V24.2,D7/D7I	U3690	CRITICAL	T29ROM:PROG	
335S0865	1	IC,EEPROM,SERIAL,8KB,MLP8	U3690	CRITICAL	T29ROM:BLANK	
335S0807	1	IC,SPI SRL 50MHZ FLASH, 64MBT,8SOP,FLSE=1	U5110	CRITICAL	BOOTROM:BLANK	Alternate: 335S0812
341S3507	1	IC,EFI,PROTO 1,D7/D7I	U5110	CRITICAL	BOOTROM:PROG	
335S0862	1	IC,SERIAL FLASH, 2MBIT, 2.7V, REV F	U3990	CRITICAL	CIVROM:BLANK	Alternate:335S0854
341S3487	1	IC,PRGRMD,ENET SPI ROM,PROTO,D7/D7I/D8	U3990	CRITICAL	CIVROM:PROG	
338S1098	1	IC,SMC12_A3, BLANK,D7	U4900	CRITICAL	SMC:BLANK	
341S3485	1	IC,SMC,EXTERNAL-PROTO 1,V2.1A94,AC,D7I	U4900	CRITICAL	SMC:PROG	
341S3506	1	IC,CAMERA FLASH,D7/D7I/D8	U4202	CRITICAL	CAMROM:PROG	
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK	

Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0107	377S0126		ALL	USB diodes
157S0055	157S0058		ALL	Enet magnetics
376S1081	376S0975		ALL	P/NCh dual FET
341S3486	341S3487		ALL	C-IV ROM ALT
128S0298	128S0293		ALL	330 UF AL POLY
155S0578	155S0367		ALL	120OHM EMI BEAD
138S0681	138S0638		ALL	Taiyo 10uf 805 alt
377S0124	377S0057		ALL	TVS

CPU Socket

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0073	1	SOCKET,MOLEX,LGA1156,CPU-LF	U1000	CRITICAL	

CPU Socket Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
511S0071	511S0073		ALL	TYCO SOCKET
511S0072	511S0073		ALL	FOXCONN SOCKET

SYNC_MASTER=D7i_INTEG SYNC_DATE=N/A

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-9179 SIZE: D

REVISION: 16.0.0

BRANCH:

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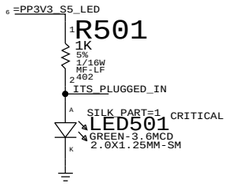
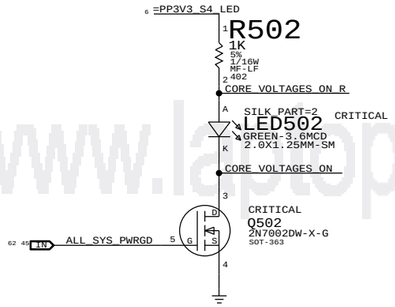
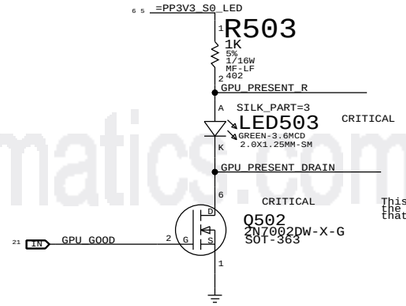
S5 Led



ALL_SYS_PWRGD Led

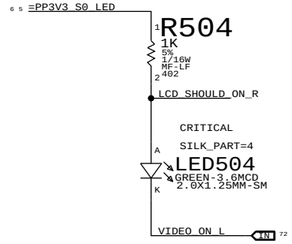


GPU GOOD Led



This LED is a GPIO driven from the southbridge that indicates that chipset has enumerated graphics

VIDEO ON Led



SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE: DEBUG LEDS

Apple Inc.

DRAWING NUMBER: 051-9179 SIZE: D

REVISION: 16.0.0

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MLB to AC-DC Supplemental Signal Connector

SILK_PART=PwrSig
CRITICAL
J601
53780-8606
M-RT-SM

PWR_BTN (OUT) 46
R606 0 5% 1/16W MF-LF 402
NOSTUFF C600 1UF 10% 6.3V CERM 402
D600 6.8V-100PF 402
PWR_BTN_R
SNS_ACDC_N (OUT) 85 51
SNS_ACDC_P (OUT) 85 51
BURSTMODE_EN_L (IN) 68 46
SMC_ACDC_ID (OUT) 46 6
=PP3V3_S0_VRD 69 67 66 63 62 6
R601 10K 5% 1/16W MF-LF 402
SMC_ACDC_ID 46 6

MLB to AC-DC Connector

CRITICAL
J600
43650-0603
F-RT-TH

PP12V_G3H_ACDC 6
J600.6:3mm C601 10UF 10% 25V X5R 805
EMC J600.7:3mm C602 1000PF 5% 25V NP0-C0G 402
EMC J600.8:3mm C603 1000PF 5% 25V NP0-C0G 402

G3 Rails

Always on: Keeps the PCH RTC alive

PP3V3_G3
MAKE_BASE=TRUE
VOLTAGE=3.3V
NET_SPACING_TYPE=POWER
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
MAX_NECK_LENGTH=3MM
- PP3V3_G3H_RTC 22 26
- =PP3V3_G3_PCH 18 19

G3H Rails

PP12V_ACDC (88) MAKE_BASE=TRUE
- PP12V_G3H_ACDC 6
- =PP12V_G3H_SNS_R 49

PP12V_G3H (88) MAKE_BASE=TRUE
- PP12V_G3H_SNS 49
- =PP12V_G3H_REG_3V42_G3H 70
- =PP12V_G3H_FET_P12V_S5 70
- =PP12V_G3H_FET_P12V_S0 71

PP3V42_G3H (88) MAKE_BASE=TRUE
- PP3V42_G3H_REG 70
- =PP3V3_G3H_BT 33
- =PP3V3_G3H_SMC 45 46
- =PP3V3_RTC_D 26
- =PPVIN_G3H_SMCVREF 46
- =PP3V3_G3H_SMC_USBMUX 43

S5 Rails

Enabled when system has AC and is in S5

PP12V_S5 (88) MAKE_BASE=TRUE
- PP12V_S5_FET 70
- =PP12V_S5_REG_P3V3P5V_S5 68
- =PP12V_S5_REG_VDDQ_S3 69
- =PP12V_S5_PWRCTL 61 62 71
- =PPHV_SW_TBTAPWRSW 75
- =PPHV_SW_TBTBPWRSW 76
- =PP12V_S5_SNS 49

PP5V_S5 (88) MAKE_BASE=TRUE
- PP5V_S5_LDO 68
- =PP5V_S5_PWRCTL 68 71
- =PP5V_S5_PCH 24

PP3V3_S5 (88) MAKE_BASE=TRUE
- PP3V3_S5_REG 68
- =PP3V3_S5_LDO_P1V05_S5
- =PP3V3_S5_FET_P3V3_S4 71
- =PP3V3_S5_FET_P3V3_S0 71
- =PP3V3_S5_PWRCTL 61 62 71
- =PP3V3_S5_VRD 68 69
- =PP3V3_S5_LED 5
- =PP3V3_S5_LPCPLUS 47
- =PP3V3_S5_PCH 19 24 26
- =PP3V3_S5_PCH_STRAPS 15
- =PP3V3_S5_PCH_VCC_DSW 22 24
- =PP3V3_S5_PCH_VCC_SPI 22 24
- =PP3V3_S5_PCH_VCCSUS_HDA 22 24
- =PP3V3_S5_PCH_VCCSUS_USB 22 24
- =PP3V3_S5_ROM 47
- =PP3V3_S5_SENSE 49
- =PP3V3_S5_SMC 46
- =PP3V3_S5_USBMUX 43 44
- =PP3V3_S5_XDP 25

S4 Rails

Enabled when system has AC and is in run or sleep

PP5V_S4 (88) MAKE_BASE=TRUE
- PP5V_S4_REG 68
- =PP5V_S4_REG_VDDQ_S3 69
- =PP5V_S4_FET_P5V_S0 71
- =PP5V_S4_MEMRESET 28
- =PP5V_S4_PWRCTL 71
- =PP5V_S4_USB 43 44
- =PP5V_S4_CAMERA 40

PP3V3_S4 (88) MAKE_BASE=TRUE
- PP3V3_S4_FET 71
- =PP3V3_S4_FET_ENET 38
- =PP3V3_S4_PWRCTL 71
- =PP3V3_S4_ALS 40
- =PP3V3_S4_AP 33
- =PP3V3_S4_LED 5
- =PP3V3_S4_MEMRESET 28
- =PP3V3_S4_PCH 15
- =PP3V3_S4_PM 28
- =PP3V3_S4_SDCARD 15 39
- =PP3V3_S4_SMC 46
- =PP3V3_S4_SMBUS_SMC_2 48
- =PP3V3_S4_TBT 34 35 36 75 76
- =PP3V3_S4_TBTAPWRSW 46 75
- =PP3V3_S4_TBTBPWRSW 46 76
- =PP3V3_S4_USB_HUB 27
- =PP3V3_S4_VREFMRGN 32
- =PP3V3_S4_CAMERA 40 41

S3 Rails

Enabled when system is in run or sleep

PP3V3_ENET (88) MAKE_BASE=TRUE
- PP3V3_ENET_FET 38
- =PP3V3_ENET_PHY 37 38
- =PP3V3_ENET_SYSCLK 26
- =PPVDDIO_ENET_CLK 26

PPVDDQ_S3 (86) MAKE_BASE=TRUE
- PPVDDQ_S3_REG 69
- =PPVDDQ_S3_FET_VDDQ_S0 71
- =PPVDDQ_S3_LDO_DDRVTT 69
- =PPVDDQ_S3_SNS_DDR_R 50
- =PPVDDQ_S3_VSNS

PPVDDQ_S3_DDR (86) MAKE_BASE=TRUE
- PPVDDQ_S3_SNS_DDR 50
- =PPVDDQ_S3_DDR_VREF 32
- =PPVDDQ_S3_MEM_A 29
- =PPVDDQ_S3_MEM_B 30
- =PPVDDQ_S3_MEMRESET 28

PPDDRVTT_S3 (86) MAKE_BASE=TRUE
- PPDDRVTT_S3_LDO 69
- =PPDDRVTT_S3_VREFCA 32

S0 Rails

Enabled when system is in run

PP12V_S0 (88) MAKE_BASE=TRUE
- PP12V_S0_FET 71
- =PP12V_S0_REG_CPUCORE_S0 64
- =PP12V_S0_REG_VCCSA_S0 67
- =PP12V_S0_REG_P1V05_S0 66
- =PP12V_S0_AUDIO_SPKRAMP 55 56
- =PP12V_S0_BKLT 77
- =PP12V_S0_FAN 52
- =PP12V_S0_LCD 72

PPHDD_S0 (88) MAKE_BASE=TRUE
- PPHDD_S0_SNS 49
- =PP5V_S0_FET_P5V_HDD 71

PP5V_S0_HDD (88) MAKE_BASE=TRUE
- PP5V_S0_HDD_FET 71
- =PP5V_S0_SATA 42

PP5V_S0 (88) MAKE_BASE=TRUE
- PP5V_S0_FET 71
- =PP5V_S0_REG_CPUCORE_S0 63
- =PP5V_S0_REG_VCCSA_S0 67
- =PP5V_S0_REG_P1V05_S0 66
- =PP5V_S0_REG_GPU_P1V05_S0
- =PP5V_S0_REG_P1V8_S0 69
- =PP5V_S0_REG_GPUCORE_S0
- =PP5V_S0_REG_GPU_VDDQ_S0
- =PP5V_S0_VRD 69
- =PP5V_S0_AUDIO 53 60
- =PP5V_S0_CAMERA
- =PP5V_S0_ISENSE 49
- =PP5V_S0_LPCPLUS 47
- =PP5V_S0_PCH 24
- =PP5V_S0_BKLT 77
- =PPHDD_S0_SNS_R 49

PP3V3_S0 (88) MAKE_BASE=TRUE
- PP3V3_S0_FET 71
- =PP3V3_S0_P3V3TBTFET 36
- =PP3V3_S0_PWRCTL 71
- =PP3V3_S0_VRD 6 62 63 66 67 69
- =PP3V3_S0_AUDIO 40 53 55 56 59
- =PP3V3_S0_AUDIO_DIG 57
- =PP3V3_S0_BT 33
- =PP3V3_S0_CAMERA
- =PP3V3_S0_DP 9 48 72 74
- =PP3V3_S0_ENET 37
- =PP3V3_S0_FAN 52
- =PP3V3_S0_INTDPMUX 73
- =PP3V3_S0_LED 5
- =PP3V3_S0_LED_SATA 15 42
- =PP3V3_S0_PCH 18 21 24
- =PP3V3_S0_PCH_GPIO 15 19 20 36
- =PP3V3_S0_PCH_PM 26
- =PP3V3_S0_PCH_STRAPS 15
- =PP3V3_S0_PCH_VCC 22 24
- =PP3V3_S0_PCH_VCC_ADAC 17
- =PP3V3_S0_PCH_VCC_GPIO 22 24
- =PP3V3_S0_PCH_VCC_HVCMOS 22 24
- =PP3V3_S0_PCH_VCC_PCI 22 24
- =PP3V3_S0_RSTBUF 26
- =PP3V3_S0_SDCARD 39
- =PP3V3_S0_SENSE 42 50 51
- =PP3V3_S0_SMBUS 48
- =PP3V3_S0_SMBUS_SMC_0 48
- =PP3V3_S0_SMBUS_SMC_1 48
- =PP3V3_S0_SMBUS_SMC_3 48
- =PP3V3_S0_SMC 9 46
- =PP3V3_S0_TBTPWRCTL 36
- =PP3V3_S0_BKLT_VDDIO 77
- =PPSPD_S0_MEM_A 29
- =PPSPD_S0_MEM_B 30

PP3V3_S0_SSD (88) MAKE_BASE=TRUE
- PP3V3_S0_SSD_FET 71
- =PPSSD_S0_SNS_R 50

PPSSD_S0 (88) MAKE_BASE=TRUE
- PPSSD_S0_SNS 50
- =PP3V3_S0_SSD 42
- =PP3V3_S0_SATAMUX 42

PP1V8_S0 (88) MAKE_BASE=TRUE
- PP1V8_S0_REG 69
- =PP1V8_S0_CAMERA
- =PP1V8_S0_CPU_PLL 13 16
- =PP1V8_S0_PCH 19
- =PP1V8_S0_PCH_VCC_DFTERM 22 24
- =PP1V8_S0_PCH_VCC_VRM 24
- =PPVDDIO_S0_SBCLK 26
- =PP1V8_S0_GPUVID
- =PP1V8_S0_ENET 38

PP1V5_S0 (86) MAKE_BASE=TRUE
- PP1V5_S0_FET 71
- =PP1V5_S0_CPU_MEM 11 13 16
- =PP1V5_S0_AUD_DIG 53
- =PP1V5_S0_SENSE 42

PPDDRVTT_S0 (86) MAKE_BASE=TRUE
- PPDDRVTT_S0_LDO 69
- =PPDDRVTT_S0_CLAMP 28
- =PPDDRVTT_S0_MEM_A 29
- =PPDDRVTT_S0_MEM_B 30

PPDDRVREF_DQ_MEM_A_S3 (88) MAKE_BASE=TRUE
- PPDDRVREF_DQ_MEM_A 32
- =PPDDRVREF_DQ_MEM_A 29

PPDDRVREF_CA_MEM_A_S3 (88) MAKE_BASE=TRUE
- PPDDRVREF_CA_MEM_A 32
- =PPDDRVREF_CA_MEM_A 29

PPDDRVREF_DQ_MEM_B_S3 (88) MAKE_BASE=TRUE
- PPDDRVREF_DQ_MEM_B 32
- =PPDDRVREF_DQ_MEM_B 30

PPDDRVREF_CA_MEM_B_S3 (88) MAKE_BASE=TRUE
- PPDDRVREF_CA_MEM_B 32
- =PPDDRVREF_CA_MEM_B 30

PP1V05_S0 (86) MAKE_BASE=TRUE
- PP1V05_S0_REG 66
- =PP1V05_S0_DP
- =PP1V05_S0_P1V05TBTFET 36
- =PP1V05_S0_PCH 18 24
- =PP1V05_S0_PCH_VCC_ADPLL 17
- =PP1V05_S0_PCH_VCC_ASW 22 24
- =PP1V05_S0_PCH_VCC_CORE 22 24
- =PP1V05_S0_PCH_VCC_DMI 22 24
- =PP1V05_S0_PCH_VCC_DIFFCLK 22
- =PP1V05_S0_PCH_VCC_SSC 22
- =PP1V05_S0_PCH_VCCIO_DMI 22
- =PP1V05_S0_PCH_VCCIO_PCIE 18 19 22
- =PP1V05_S0_PCH_VCCIO_SATA 18 22 24
- =PP1V05_S0_PCH_VCCIO_USB 22
- =PP1V05_S0_PCH_V_PROC_IO 22 24
- =PPVCCIO_S0_CPU 10 11 13 16 63
- =PPVCCIO_S0_SMC 46
- =PPVCCIO_S0_XDP 25

PPVCORE_S0_CPU (87) MAKE_BASE=TRUE
- PPCPUCORE_S0_REG 64
- =PPVCORE_S0_CPU 13 16 49 63

PPVAXG_S0 (87) MAKE_BASE=TRUE
- PPCPUAXG_S0_REG 65
- =PPVAXG_S0_CPU 13 17 49 63

PPVCCSA_S0 (86) MAKE_BASE=TRUE
- PPVCCSA_S0_REG 67
- =PPVCCSA_S0_CPU 13 16

Thunderbolt Rails (S0)

Enabled when Thunderbolt cable is plugged in

PP3V3_TBTLC (88) MAKE_BASE=TRUE
- =PP3V3_TBTLC_FET 36
- =PP3V3_TBT_PCH_GPIO 15
- =PP3V3_TBTLC_RTR 34 35 36
- =PPVDDIO_TBT_CLK 26

PP1V05_TBTLC (86) MAKE_BASE=TRUE
- =PP1V05_TBTLC_FET 36
- =PP1V05_TBTLC_RTR 35 36

PP1V05_TBTCIO (86) MAKE_BASE=TRUE
- =PP1V05_TBTCIO_FET 36
- =PP1V05_TBTCIO_RTR 35

Ground/Common

GND
MAKE_BASE=TRUE

SYNC_MASTER=D7I_NICK SYNC_DATE=01/11/2012

PAGE TITLE
Power Connectors/Aliases

Apple Inc.

DRAWING NUMBER 051-9179 SIZE D
REVISION 16.0.0
BRANCH
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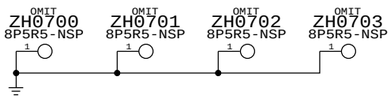
CPU Heatsink

4mm Plated Holes (998-0850)

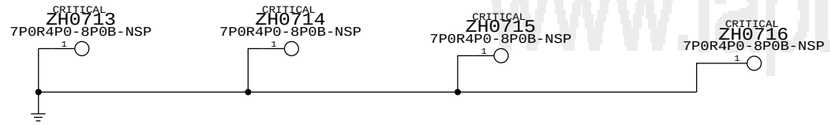


WIRELESS CARD MTG HOLES

998-4560 (Plated holes, 2.3mm inner diameter, 4.3mm pad)

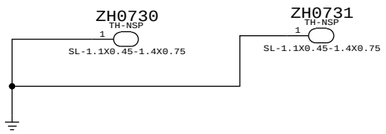
Rear Cover

998-4559 (Plated holes, 4mm inner diameter, 8mm pad)



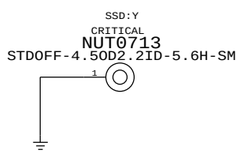
USB Can holes

998-3975 (Plated slot holes, 1.10mm x 0.45mm)



SSD STANDOFF

APN: 860-1461



SYNC_MASTER=D7i_INTEG SYNC_DATE=N/A

PAGE TITLE: Holes/PD parts

Apple Inc.

DRAWING NUMBER: 051-9179 SIZE: D

REVISION: 16.0.0

BRANCH:

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CPU Reserved

10	TP_CPU_RSVD<16..1>	NC_CPU_RSVD<16..1>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_RSVD<46..19>	NC_CPU_RSVD<46..19>	MAKE_BASE=TRUE NO_TEST=TRUE
82 10	CPU_CFG<15..12>	TP_CPU_CFG<15..12>	MAKE_BASE=TRUE

CPU Memory

12	TP_MEM_A_DQ_CB<7..0>	NC_MEM_A_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_A_DQS_N<8>	NC_MEM_A_DQSN<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_A_DQS_P<8>	NC_MEM_A_DQSP<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQ_CB<7..0>	NC_MEM_B_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQS_N<8>	NC_MEM_B_DQSN<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQS_P<8>	NC_MEM_B_DQSP<8>	MAKE_BASE=TRUE NO_TEST=TRUE
79 12	MEM_A_CLK_N<2..3>	NC_MEM_A_CLKN<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
79 12	MEM_A_CLK_P<2..3>	NC_MEM_A_CLKP<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
79 12	MEM_A_CS_L<2..3>	NC_MEM_A_CS_L<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
79 12	MEM_A_CKE<2..3>	NC_MEM_A_CKE<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
79 12	MEM_B_CLK_N<2..3>	NC_MEM_B_CLKN<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
79 12	MEM_B_CLK_P<2..3>	NC_MEM_B_CLKP<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
79 12	MEM_B_CS_L<2..3>	NC_MEM_B_CS_L<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
79 12	MEM_B_CKE<2..3>	NC_MEM_B_CKE<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
79 12	MEM_A_ODT<2..3>	NC_MEM_A_ODT<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE
79 12	MEM_B_ODT<2..3>	NC_MEM_B_ODT<2..3>	MAKE_BASE=TRUE NO_TEST=TRUE

PCH USB

20	USB_PCH_4_N	NC_USB_PCH_4_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_4_P	NC_USB_PCH_4_P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_5_N	NC_USB_PCH_5_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_5_P	NC_USB_PCH_5_P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_6_N	NC_USB_PCH_6_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_6_P	NC_USB_PCH_6_P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_11_N	NC_USB_PCH_11_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_11_P	NC_USB_PCH_11_P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_12_N	NC_USB_PCH_12_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_12_P	NC_USB_PCH_12_P	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_13_N	NC_USB_PCH_13_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_13_P	NC_USB_PCH_13_P	MAKE_BASE=TRUE NO_TEST=TRUE

PCH PLL

22	PP1V05_S0_PCH_VCCAPLLDMI2	NC_PP1V05_S0_PCH_VCCAPLLDMI2	MAKE_BASE=TRUE NO_TEST=TRUE
22	PP1V05_S0_PCH_VCCAPLL_EXP	NC_PP1V05_S0_PCH_VCCAPLL_EXP	MAKE_BASE=TRUE NO_TEST=TRUE
22	PP1V05_S0_PCH_VCCAPLL_SATA	NC_PP1V05_S0_PCH_VCCAPLL_SATA	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Clocks

18	TP_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE6N	NC_PCIE_CLK100M_PE6N	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE7N	NC_PCIE_CLK100M_PE7N	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE7P	NC_PCIE_CLK100M_PE7P	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_TX_N<3..0>	NC_PE_TXN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_TX_P<3..0>	NC_PE_TXP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_RX_N<3..0>	NC_PE_RXN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_RX_P<3..0>	NC_PE_RXP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
18	DMI_MIDBUS_CLK100M_N	NC_DMI_MIDBUS_CLK100N	MAKE_BASE=TRUE NO_TEST=TRUE
18	DMI_MIDBUS_CLK100M_P	NC_DMI_MIDBUS_CLK100P	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_CLKOUT_PEG_A_N	NC_CLKOUT_PEG_AN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_CLKOUT_PEG_A_P	NC_CLKOUT_PEG_AP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CLKOUT_DPN	NC_PCH_CLKOUT_DPN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CLKOUT_DPP	NC_PCH_CLKOUT_DPP	MAKE_BASE=TRUE NO_TEST=TRUE
18	PCH_CLK25M_XTALOUT	NC_PCH_CLK25M_XTALOUT	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO64_CLKOUTFLEX0	NC_PCH_GPIO64_CLKOUTFLEX0	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO65_CLKOUTFLEX1	NC_PCH_GPIO65_CLKOUTFLEX1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO66_CLKOUTFLEX2	NC_PCH_GPIO66_CLKOUTFLEX2	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO67_CLKOUTFLEX3	NC_PCH_GPIO67_CLKOUTFLEX3	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Unused Display

19	TP_CRT_IG_RED	NC_CRT_IG_RED	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_GREEN	NC_CRT_IG_GREEN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_BLUE	NC_CRT_IG_BLUE	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_HSYNC	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_VSYNC	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_DDC_CLK	NC_CRT_IG_DDC_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_DDC_DATA	NC_CRT_IG_DDC_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINN	NC_SDVO_TVCLKINN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINP	NC_SDVO_TVCLKINP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLN	NC_SDVO_STALLN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLP	NC_SDVO_STALLP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTN	NC_SDVO_INTN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTP	NC_SDVO_INTP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_BKLTEN	NC_PCH_L_BKLTEN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_VDD_EN	NC_PCH_L_VDD_EN	MAKE_BASE=TRUE NO_TEST=TRUE

UNUSED GRAPHICS ALIASES

TP_DVPCNTL_M<0..1>	NC_DVPCNTL_M<0..1>	MAKE_BASE=TRUE NO_TEST=TRUE
TP_DVPCNTL<0..2>	NC_DVPCNTL<0..2>	MAKE_BASE=TRUE NO_TEST=TRUE
TP_DVPCLK	NC_DVPCLK	MAKE_BASE=TRUE NO_TEST=TRUE
TP_DVPDATA<4..23>	NC_DVPDATA<4..23>	MAKE_BASE=TRUE NO_TEST=TRUE
HDMI_EG_CLK_C_P	NC_HDMI_EG_CLK_C_P	MAKE_BASE=TRUE NO_TEST=TRUE
HDMI_EG_CLK_C_N	NC_HDMI_EG_CLK_C_N	MAKE_BASE=TRUE NO_TEST=TRUE
HDMI_EG_DDC_CLK	NC_HDMI_EG_DDC_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
HDMI_EG_DDC_DATA	NC_HDMI_EG_DDC_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
HDMI_EG_DATA_C_P<0..2>	NC_HDMI_EG_DATA_C_P<0..2>	MAKE_BASE=TRUE NO_TEST=TRUE
HDMI_EG_DATA_C_N<0..2>	NC_HDMI_EG_DATA_C_N<0..2>	MAKE_BASE=TRUE NO_TEST=TRUE
GPU_TDIODE_P	NC_GPU_TDIODE_P	MAKE_BASE=TRUE NO_TEST=TRUE
GPU_TDIODE_N	NC_GPU_TDIODE_N	MAKE_BASE=TRUE NO_TEST=TRUE
EG_LCD_PWR_EN	NC_EG_LCD_PWR_EN	MAKE_BASE=TRUE NO_TEST=TRUE

PCH SATA

18	TP_SATA_C_R2D_CN	NC_SATA_C_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_C_R2D_CP	NC_SATA_C_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_C_D2RN	NC_SATA_C_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_C_D2RP	NC_SATA_C_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_R2D_CN	NC_SATA_D_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_R2D_CP	NC_SATA_D_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_D2RN	NC_SATA_D_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_D2RP	NC_SATA_D_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_R2D_CN	NC_SATA_E_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_R2D_CP	NC_SATA_E_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_D2RN	NC_SATA_E_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_D2RP	NC_SATA_E_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_R2D_CN	NC_SATA_F_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_R2D_CP	NC_SATA_F_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_D2RN	NC_SATA_F_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_D2RP	NC_SATA_F_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Reserved

19	TP_PCH_RESERVE_0	NC_PCH_RESERVE_0	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_1	NC_PCH_RESERVE_1	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_2	NC_PCH_RESERVE_2	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_3	NC_PCH_RESERVE_3	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_4	NC_PCH_RESERVE_4	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_5	NC_PCH_RESERVE_5	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_6	NC_PCH_RESERVE_6	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_7	NC_PCH_RESERVE_7	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_8	NC_PCH_RESERVE_8	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_9	NC_PCH_RESERVE_9	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_10	NC_PCH_RESERVE_10	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_11	NC_PCH_RESERVE_11	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_12	NC_PCH_RESERVE_12	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_13	NC_PCH_RESERVE_13	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_14	NC_PCH_RESERVE_14	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_15	NC_PCH_RESERVE_15	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_16	NC_PCH_RESERVE_16	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_17	NC_PCH_RESERVE_17	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_18	NC_PCH_RESERVE_18	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_19	NC_PCH_RESERVE_19	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_20	NC_PCH_RESERVE_20	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_21	NC_PCH_RESERVE_21	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_22	NC_PCH_RESERVE_22	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_23	NC_PCH_RESERVE_23	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_24	NC_PCH_RESERVE_24	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_25	NC_PCH_RESERVE_25	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_26	NC_PCH_RESERVE_26	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_27	NC_PCH_RESERVE_27	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_28	NC_PCH_RESERVE_28	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Test Points

21	TP_PCH_TP1	NC_PCH_TP1	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP2	NC_PCH_TP2	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP3	NC_PCH_TP3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP4	NC_PCH_TP4	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP5	NC_PCH_TP5	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP6	NC_PCH_TP6	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP7	NC_PCH_TP7	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP8	NC_PCH_TP8	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP9	NC_PCH_TP9	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP10	NC_PCH_TP10	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP11	NC_PCH_TP11	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP12	NC_PCH_TP12	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP13	NC_PCH_TP13	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP14	NC_PCH_TP14	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP15	NC_PCH_TP15	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP16	NC_PCH_TP16	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP17	NC_PCH_TP17	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP18	NC_PCH_TP18	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP19	NC_PCH_TP19	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP20	NC_PCH_TP20	MAKE_BASE=TRUE NO_TEST=TRUE

PCH PCI

20	TP_PCI_AD<31..0>	NC_PCI_AD<31..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_C_BE_L<3..0>	NC_PCI_C_BE_L<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_PAR	NC_PCI_PAR	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_RESET_L	NC_PCI_RESET_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_INIT3V3_L	NC_PCH_INIT3V3_L	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_LPC_DREQ0_L	NC_LPC_DREQ0_L	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Miscellaneous

18	TP_HDA_SDIN1	NC_HDA_SDIN1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN2	NC_HDA_SDIN2	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN3	NC_HDA_SDIN3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM0	NC_PCH_PWM0	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM1	NC_PCH_PWM1	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM2	NC_PCH_PWM2	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM3	NC_PCH_PWM3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_SST	NC_PCH_SST	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_CLK1	NC_PCH_CL_CLK1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_DATA1	NC_PCH_CL_DATA1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_RST1	NC_PCH_CL_RST1	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_CLK33M_OUT2	NC_PCI_CLK33M_OUT2	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_CLK33M_OUT3	NC_PCI_CLK33M_OUT3	MAKE_BASE=TRUE NO_TEST=TRUE
22	PP1V05_S0_PCH_FDIPLL	NC_PP1V05_S0_PCH_FDIPLL	MAKE_BASE=TRUE NO_TEST=TRUE
22	PP1V05_S0_PCH_VCC_A_CLK	NC_PP1V05_S0_PCH_VCC_A_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
22	TP_PPVOUT_PCH_DCPSUSBYP	NC_PPVOUT_PCH_DCPSUSBYP	MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=D7i_INTEG SYNC_DATE=N/A

PAGE TITLE: Unused Signal Aliases

Apple Inc.

DRAWING NUMBER: 051-9179 SIZE: D

REVISION: 16.0.0

BRANCH:

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unused GPU aliases

10 =PEG_D2R_N<0..15> — NC_PEG_D2R_N<0..15> — MAKE_BASE=TRUE NO_TEST=TRUE
10 =PEG_D2R_P<0..15> — NC_PEG_D2R_P<0..15> — MAKE_BASE=TRUE NO_TEST=TRUE
10 =PEG_R2D_C_N<0..15> — NC_PEG_R2D_C_N<0..15> — MAKE_BASE=TRUE NO_TEST=TRUE
10 =PEG_R2D_C_P<0..15> — NC_PEG_R2D_C_P<0..15> — MAKE_BASE=TRUE NO_TEST=TRUE

CPU PCH FDI BUS

82 10 CPU_FDI_TX_N<7..0> — PCH_FDI_RX_N<7..0> 19 — MAKE_BASE=TRUE
82 10 CPU_FDI_TX_P<7..0> — PCH_FDI_RX_P<7..0> 19 — MAKE_BASE=TRUE
82 10 CPU_FDI_FSYNC<1..0> — PCH_FDI_FSYNC<1..0> 19 — MAKE_BASE=TRUE
82 10 CPU_FDI_LSYNC<1..0> — PCH_FDI_LSYNC<1..0> 19 — MAKE_BASE=TRUE
82 10 CPU_FDI_INT — PCH_FDI_INT 19 — MAKE_BASE=TRUE

PCH DP ALIAS

19 DP_IG_C_MLN<3..0> — DP_TBTSNK0_ML_C_N<3:0> 34 89 — MAKE_BASE=TRUE
19 DP_IG_C_MLP<3..0> — DP_TBTSNK0_ML_C_P<3:0> 34 89 — MAKE_BASE=TRUE
19 DP_IG_C_AUX_N — DP_TBTSNK0_AUXCH_C_N 34 89 — MAKE_BASE=TRUE
19 DP_IG_C_AUX_P — DP_TBTSNK0_AUXCH_C_P 34 89 — MAKE_BASE=TRUE
19 DP_IG_C_HPD — DP_TBTSNK0_HPD 34 — MAKE_BASE=TRUE
19 9 DP_IG_C_CTRL_CLK — DP_TBTSNK0_DDC_CLK 74 — MAKE_BASE=TRUE
19 9 DP_IG_C_CTRL_DATA — DP_TBTSNK0_DDC_DATA 74 — MAKE_BASE=TRUE

19 DP_IG_D_MLN<3..0> — DP_TBTSNK1_ML_C_N<3:0> 34 89 — MAKE_BASE=TRUE
19 DP_IG_D_MLP<3..0> — DP_TBTSNK1_ML_C_P<3:0> 34 89 — MAKE_BASE=TRUE
19 DP_IG_D_AUXN — DP_TBTSNK1_AUXCH_C_N 34 89 — MAKE_BASE=TRUE
19 DP_IG_D_AUXP — DP_TBTSNK1_AUXCH_C_P 34 89 — MAKE_BASE=TRUE
19 DP_IG_D_HPD — DP_TBTSNK1_HPD 34 — MAKE_BASE=TRUE
19 9 DP_IG_D_CTRL_CLK — DP_TBTSNK1_DDC_CLK 74 — MAKE_BASE=TRUE
19 9 DP_IG_D_CTRL_DATA — DP_TBTSNK1_DDC_DATA 74 — MAKE_BASE=TRUE

19 DP_IG_B_MLN<3..0> — DP_INT_EG_ML_N<3:0> 73 89 — MAKE_BASE=TRUE
19 DP_IG_B_MLP<3..0> — DP_INT_EG_ML_P<3:0> 73 89 — MAKE_BASE=TRUE
19 DP_IG_B_AUX_N — DP_INT_EG_AUX_N 73 89 — MAKE_BASE=TRUE
19 DP_IG_B_AUX_P — DP_INT_EG_AUX_P 73 89 — MAKE_BASE=TRUE
19 DP_IG_B_HPD — DP_INT_EG_HPD 73 — MAKE_BASE=TRUE

18 TP_PCH_L_BKLTCTL — GPU_LCD_BKLT_PWM 73 — MAKE_BASE=TRUE

74 72 48 9 6 =PP3V3_S0_DP
R0900[1] 2.2K 5% 1/16W MF-LF 402 2
R0901[1] 2.2K 5% 1/16W MF-LF 402 2
19 DP_IG_B_DDC_CLK
19 DP_IG_B_DDC_DATA

74 72 48 9 6 =PP3V3_S0_DP
R0902[1] 2.2K 5% 1/16W MF-LF 402 2
R0903[1] 2.2K 5% 1/16W MF-LF 402 2
19 9 DP_IG_C_CTRL_CLK
19 9 DP_IG_C_CTRL_DATA

74 72 48 9 6 =PP3V3_S0_DP
R0904[1] 2.2K 5% 1/16W MF-LF 402 2
R0905[1] 2.2K 5% 1/16W MF-LF 402 2
19 9 DP_IG_D_CTRL_CLK
19 9 DP_IG_D_CTRL_DATA

26 GPU_RESET_L — NC_GPU_RESET_L — MAKE_BASE=TRUE NO_TEST=TRUE
80 18 PEG_CLK100M_P — NC_PEG_CLK100M_P — MAKE_BASE=TRUE NO_TEST=TRUE
80 18 PEG_CLK100M_N — NC_PEG_CLK100M_N — MAKE_BASE=TRUE NO_TEST=TRUE

SMC-EG pull up and pull down

the pull up and down should be deleted if SMC ignore those two signals

46 6 =PP3V3_S0_SMC
R0906[1] 10K 5% 1/20W MF 201 2
R0907[1] 10K 5% 1/20W MF 201 2
SMC_GFX_THROTTLE_R_L — R0909 0 5% 1/16W MF-LF 402 — SMC_GFX_THROTTLE_L — IN 45
SMC_GFX_OVERTEMP_R_L — R0908 0 5% 1/16W MF-LF 402 — SMC_GFX_OVERTEMP — OUT 45 46
NOSTUFF
R0910[1] 10K 5% 1/20W MF 201 2

SYNC_MASTER=D7i_INTEG SYNC_DATE=N/A
PAGE TITLE: Signal Aliases
Apple Inc.
DRAWING NUMBER: 051-9179 SIZE: D
REVISION: 16.0.0
BRANCH:
PAGE: 9 OF 113
SHEET: 9 OF 90

DMI_S2N_P/N<1> swapped for D7i layout

SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4 MIL TRACE TO R1010.1
ROUTE B5 TO R1010.1 AS A SEPERATE 10 MIL TRACE.

OMIT TABLE
U1000
IVY-BRIDGE
BGA-SKT-K70
SYM 1 OF 10

DMI
DMI_S2N_N<0> W4 DMI_RX_0*
DMI_S2N_N<1> V4 DMI_RX_1*
DMI_S2N_N<2> Y4 DMI_RX_2*
DMI_S2N_N<3> AA5 DMI_RX_3*
DMI_S2N_P<0> W5 DMI_RX_0
DMI_S2N_P<1> V3 DMI_RX_1
DMI_S2N_P<2> Y3 DMI_RX_2
DMI_S2N_P<3> AA4 DMI_RX_3
DMI_N2S_N<0> V6 DMI_TX_0*
DMI_N2S_N<1> W8 DMI_TX_1*
DMI_N2S_N<2> Y7 DMI_TX_2*
DMI_N2S_N<3> AA8 DMI_TX_3*
DMI_N2S_P<0> V7 DMI_TX_0
DMI_N2S_P<1> W7 DMI_TX_1
DMI_N2S_P<2> Y6 DMI_TX_2
DMI_N2S_P<3> AA7 DMI_TX_3

FLEXIBLE DISPLAY INTERFACE
CPU_FDI_TX_N<0> AC7 FDI_TX_0*
CPU_FDI_TX_N<1> AC3 FDI_TX_1*
CPU_FDI_TX_N<2> AD1 FDI_TX_2*
CPU_FDI_TX_N<3> AD3 FDI_TX_3*
CPU_FDI_TX_N<4> AD6 FDI_TX_4*
CPU_FDI_TX_N<5> AE8 FDI_TX_5*
CPU_FDI_TX_N<6> AF2 FDI_TX_6*
CPU_FDI_TX_N<7> AG1 FDI_TX_7*
CPU_FDI_TX_P<0> AC8 FDI_TX_0
CPU_FDI_TX_P<1> AC2 FDI_TX_1
CPU_FDI_TX_P<2> AD2 FDI_TX_2
CPU_FDI_TX_P<3> AD4 FDI_TX_3
CPU_FDI_TX_P<4> AD7 FDI_TX_4
CPU_FDI_TX_P<5> AE7 FDI_TX_5
CPU_FDI_TX_P<6> AF3 FDI_TX_6
CPU_FDI_TX_P<7> AG2 FDI_TX_7
CPU_FDI_FSYNC<0> AC5 FDI_FSYNC_0
CPU_FDI_FSYNC<1> AE5 FDI_FSYNC_1
CPU_FDI_INT AG3 FDI_INT
CPU_FDI_LSYNC<0> AC4 FDI_LSYNC_0
CPU_FDI_LSYNC<1> AE4 FDI_LSYNC_1
CPU_FDI_COMPIO AE2 FDI_COMPIO
AE1 FDI_ICOMPO

=PPVCCIO_S0_CPU
R1011 24.9 1% 1/10W MF-LF 402

(Unused)

PCI EXPRESS -- GRAPHICS
(Available for Workstation only)
PCI EXPRESS
TP_PE_RX_N<0> P4 PE_RX_0*
TP_PE_RX_N<1> R1 PE_RX_1*
TP_PE_RX_N<2> T3 PE_RX_2*
TP_PE_RX_N<3> U1 PE_RX_3*
TP_PE_RX_P<0> P3 PE_RX_0
TP_PE_RX_P<1> R2 PE_RX_1
TP_PE_RX_P<2> T4 PE_RX_2
TP_PE_RX_P<3> U2 PE_RX_3
TP_PE_TX_N<0> P7 PE_TX_0*
TP_PE_TX_N<1> T8 PE_TX_1*
TP_PE_TX_N<2> R5 PE_TX_2*
TP_PE_TX_N<3> U6 PE_TX_3*
TP_PE_TX_P<0> P8 PE_TX_0
TP_PE_TX_P<1> T7 PE_TX_1
TP_PE_TX_P<2> R6 PE_TX_2
TP_PE_TX_P<3> U5 PE_TX_3

PEG_COMPI B4
PEG_ICOMPO B5
PEG_RCOMPO C4
CPU_PEG_COMP

PLACE_NEAR=U1000.B4:12.7mm
R1010 24.9 1% 1/10W MF-LF 402
=PPVCCIO_S0_CPU

PEG_RX_0* B12 =PEG_D2R_N<0>
PEG_RX_1* D11 =PEG_D2R_N<1>
PEG_RX_2* C9 =PEG_D2R_N<2>
PEG_RX_3* E9 =PEG_D2R_N<3>
PEG_RX_4* B7 =PEG_D2R_N<4>
PEG_RX_5* C5 =PEG_D2R_N<5>
PEG_RX_6* A6 =PEG_D2R_N<6>
PEG_RX_7* E1 =PEG_D2R_N<7>
PEG_RX_8* F3 =PEG_D2R_N<8>
PEG_RX_9* G1 =PEG_D2R_N<9>
PEG_RX_10* H4 =PEG_D2R_N<10>
PEG_RX_11* J2 =PEG_D2R_N<11>
PEG_RX_12* K4 =PEG_D2R_N<12>
PEG_RX_13* L2 =PEG_D2R_N<13>
PEG_RX_14* M4 =PEG_D2R_N<14>
PEG_RX_15* N2 =PEG_D2R_N<15>
PEG_RX_0 B11 =PEG_D2R_P<0>
PEG_RX_1 D12 =PEG_D2R_P<1>
PEG_RX_2 C10 =PEG_D2R_P<2>
PEG_RX_3 E10 =PEG_D2R_P<3>
PEG_RX_4 B8 =PEG_D2R_P<4>
PEG_RX_5 C6 =PEG_D2R_P<5>
PEG_RX_6 A5 =PEG_D2R_P<6>
PEG_RX_7 E2 =PEG_D2R_P<7>
PEG_RX_8 F4 =PEG_D2R_P<8>
PEG_RX_9 G2 =PEG_D2R_P<9>
PEG_RX_10 H3 =PEG_D2R_P<10>
PEG_RX_11 J1 =PEG_D2R_P<11>
PEG_RX_12 K3 =PEG_D2R_P<12>
PEG_RX_13 L1 =PEG_D2R_P<13>
PEG_RX_14 M3 =PEG_D2R_P<14>
PEG_RX_15 N1 =PEG_D2R_P<15>
PEG_TX_0* C14 =PEG_R2D_C_N<0>
PEG_TX_1* E13 =PEG_R2D_C_N<1>
PEG_TX_2* G13 =PEG_R2D_C_N<2>
PEG_TX_3* F11 =PEG_R2D_C_N<3>
PEG_TX_4* J13 =PEG_R2D_C_N<4>
PEG_TX_5* D7 =PEG_R2D_C_N<5>
PEG_TX_6* C3 =PEG_R2D_C_N<6>
PEG_TX_7* E5 =PEG_R2D_C_N<7>
PEG_TX_8* F7 =PEG_R2D_C_N<8>
PEG_TX_9* G9 =PEG_R2D_C_N<9>
PEG_TX_10* G6 =PEG_R2D_C_N<10>
PEG_TX_11* K8 =PEG_R2D_C_N<11>
PEG_TX_12* J6 =PEG_R2D_C_N<12>
PEG_TX_13* M7 =PEG_R2D_C_N<13>
PEG_TX_14* L5 =PEG_R2D_C_N<14>
PEG_TX_15* N6 =PEG_R2D_C_N<15>
PEG_TX_0 C13 =PEG_R2D_C_P<0>
PEG_TX_1 E14 =PEG_R2D_C_P<1>
PEG_TX_2 G14 =PEG_R2D_C_P<2>
PEG_TX_3 F12 =PEG_R2D_C_P<3>
PEG_TX_4 J14 =PEG_R2D_C_P<4>
PEG_TX_5 D8 =PEG_R2D_C_P<5>
PEG_TX_6 D3 =PEG_R2D_C_P<6>
PEG_TX_7 E6 =PEG_R2D_C_P<7>
PEG_TX_8 F8 =PEG_R2D_C_P<8>
PEG_TX_9 G10 =PEG_R2D_C_P<9>
PEG_TX_10 G5 =PEG_R2D_C_P<10>
PEG_TX_11 K7 =PEG_R2D_C_P<11>
PEG_TX_12 J5 =PEG_R2D_C_P<12>
PEG_TX_13 M8 =PEG_R2D_C_P<13>
PEG_TX_14 L6 =PEG_R2D_C_P<14>
PEG_TX_15 N5 =PEG_R2D_C_P<15>

OMIT TABLE
U1000
IVY-BRIDGE
BGA-SKT-K70
SYM 5 OF 10

RESERVED
TP_CPU_RSVD<1> C38 RSVD_C38
TP_CPU_RSVD<2> C39 RSVD_C39
TP_CPU_RSVD<3> D38 RSVD_D38
TP_CPU_RSVD<4> H7 RSVD_H7
TP_CPU_RSVD<5> H8 RSVD_H8
TP_CPU_RSVD<6> J9 RSVD_J9
TP_CPU_RSVD<7> J31 RSVD_J31
TP_CPU_RSVD<8> J33 RSVD_J33
TP_CPU_RSVD<9> J34 RSVD_J34
TP_CPU_RSVD<10> K9 RSVD_K9
TP_CPU_RSVD<11> K31 RSVD_K31
TP_CPU_RSVD<12> K34 RSVD_K34
TP_CPU_RSVD<13> L9 RSVD_L9
TP_CPU_RSVD<14> L31 RSVD_L31
TP_CPU_RSVD<15> L33 RSVD_L33
TP_CPU_RSVD<16> L34 RSVD_L34
NC_SNS_CPU_THERMDN M34 RSVD_M34 ThermDC
NO TEST=TRUE
NC_SNS_CPU_THERMDP N33 RSVD_N33 ThermDA
NO TEST=TRUE
TP_CPU_RSVD<19> N34 RSVD_N34
RSVD_P35 P35 TP_CPU_RSVD<20>
RSVD_P37 P37 TP_CPU_RSVD<21>
RSVD_P39 P39 TP_CPU_RSVD<22>
RSVD_R34 R34 TP_CPU_RSVD<23>
RSVD_R36 R36 TP_CPU_RSVD<24>
RSVD_R38 R38 TP_CPU_RSVD<25>
RSVD_R40 R40 TP_CPU_RSVD<26>
RSVD_AB6 AB6 TP_CPU_RSVD<27>
RSVD_AB7 AB7 TP_CPU_RSVD<28>
RSVD_AD34 AD34 TP_CPU_RSVD<29>
RSVD_AD35 AD35 TP_CPU_RSVD<30>
RSVD_AD37 AD37 TP_CPU_RSVD<31>
RSVD_AE6 AE6 TP_CPU_RSVD<32>
RSVD_AF4 AF4 TP_CPU_RSVD<33>
RSVD_AG4 AG4 TP_CPU_RSVD<34>
RSVD_AJ11 AJ11 TP_CPU_RSVD<35>
RSVD_AJ29 AJ29 TP_CPU_RSVD<36>
RSVD_AJ30 AJ30 TP_CPU_RSVD<37>
RSVD_AJ31 AJ31 TP_CPU_RSVD<38>
RSVD_AN20 AN20 TP_CPU_RSVD<39>
RSVD_AP20 AP20 TP_CPU_RSVD<40>
RSVD_AT11 AT11 TP_CPU_RSVD<41>
RSVD_AT14 AT14 TP_CPU_RSVD<42>
RSVD_AU10 AU10 TP_CPU_RSVD<43>
RSVD_AV34 AV34 TP_CPU_RSVD<44>
RSVD_AW34 AW34 TP_CPU_RSVD<45>
RSVD_AY10 AY10 TP_CPU_RSVD<46>

CPU_CFG<0> H36 CFG_0
CPU_CFG<1> J36 CFG_1
CPU_CFG<2> J37 CFG_2
CPU_CFG<3> K36 CFG_3
CPU_CFG<4> L36 CFG_4
CPU_CFG<5> N35 CFG_5
CPU_CFG<6> L37 CFG_6
CPU_CFG<7> M36 CFG_7
CPU_CFG<8> J38 CFG_8
CPU_CFG<9> L35 CFG_9
CPU_CFG<10> M38 CFG_10
CPU_CFG<11> N36 CFG_11
CPU_CFG<12> N38 CFG_12
CPU_CFG<13> N39 CFG_13
CPU_CFG<14> N37 CFG_14
CPU_CFG<15> N40 CFG_15
CPU_CFG<16> G37 CFG_16
CPU_CFG<17> G36 CFG_17

RSVD_NCTF_AV1 AV1 TP_CPU_RSVD_NCTF<1>
RSVD_NCTF_AW2 AW2 TP_CPU_RSVD_NCTF<2>
RSVD_NCTF_AY3 AY3 TP_CPU_RSVD_NCTF<3>
RSVD_NCTF_B39 B39 TP_CPU_RSVD_NCTF<4>
NCTF_A38 A38 TP_CPU_NCTF<1>
NCTF_C2 C2 TP_CPU_NCTF<2>
NCTF_D1 D1 TP_CPU_NCTF<3>
NCTF_AU40 AU40 TP_CPU_NCTF<4>
NCTF_AW38 AW38 TP_CPU_NCTF<5>

INTEL SUGGESTS TO KEEP THESE TPS

CFG[1:0] Reserved config lane
CFG[2] PCIe Static x16 lane reversal; Refer to page 15 for more info
CFG[3] PCIe Static x4 lane reversal; Refer to page 15 for more info
CFG[4] Reserved config lane
CFG[6:5] PCIe bifurcation; Refer to page 15 for more info
CFG[17:7] Reserved config lanes

SYNC_MASTER=D7i_MLB SYNC_DATE=N/A
PAGE TITLE
CPU DMI/PEG/FDI/RSVD
Apple Inc.
DRAWING NUMBER 051-9179
SIZE D
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PAGE 10 OF 113
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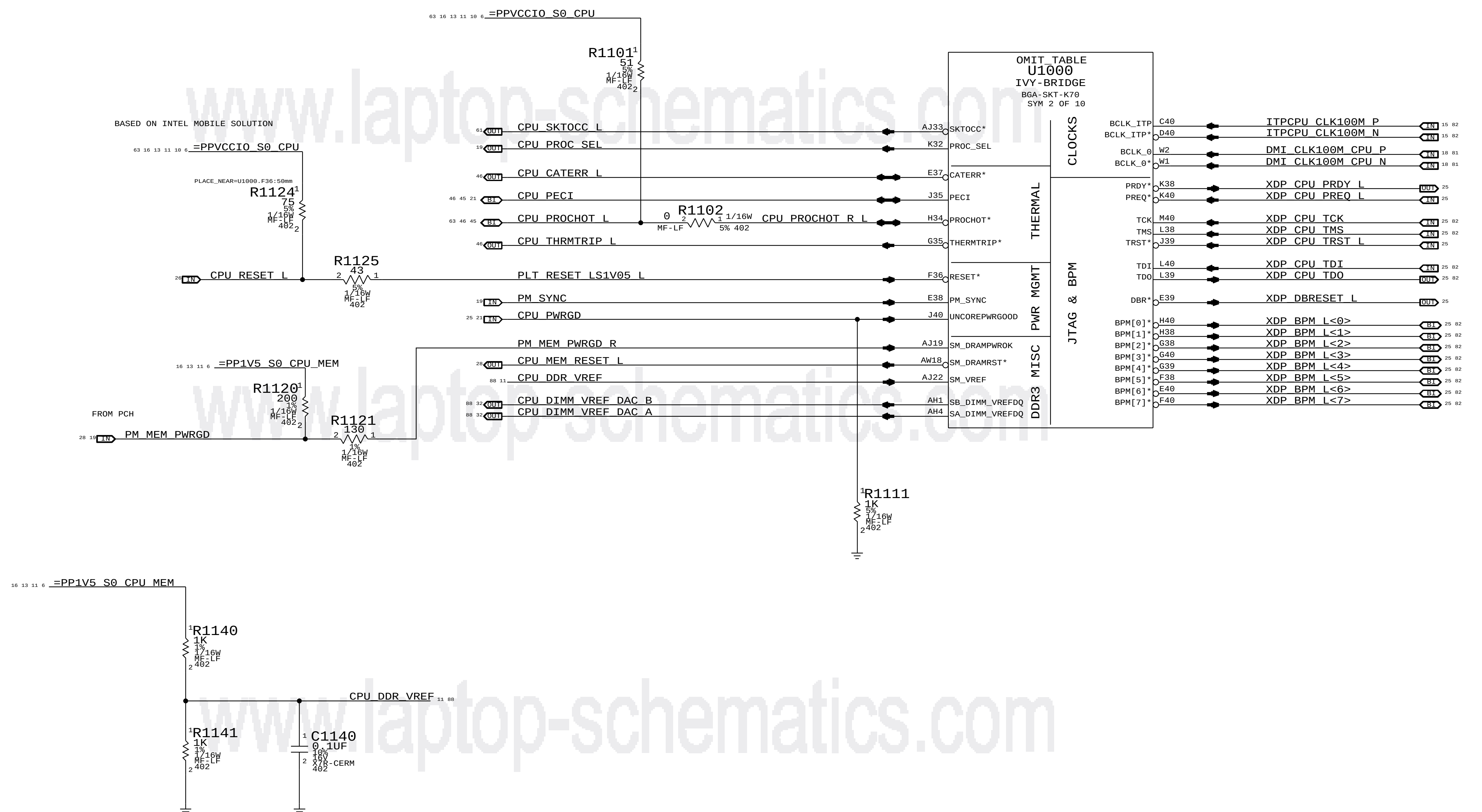
=PPVCCIO_S0_CPU
R1101
51
5%
1/16W
MF-LF
402
BASED ON INTEL MOBILE SOLUTION
PLACE_NEAR=U1000.F36:50mm
R1124
75
CPU_RESET_L
R1125
43
PLT_RESET_LS1V05_L
CPU_SKTOCC_L
CPU_PROC_SEL
CPU_CATERR_L
CPU_PECI
CPU_PROCHOT_L
R1102
CPU_PROCHOT_R_L
CPU_THRMTRIP_L
PM_SYNC
CPU_PWRGD
PM_MEM_PWRGD_R
CPU_MEM_RESET_L
CPU_DDR_VREF
CPU_DIMM_VREF_DAC_B
CPU_DIMM_VREF_DAC_A
=PP1V5_S0_CPU_MEM
R1120
200
FROM PCH
PM_MEM_PWRGD
R1121
130
R1111
1K
OMIT_TABLE
U1000
IVY-BRIDGE
BGA-SKT-K70
SYM 2 OF 10
CLOCKS
THERMAL
PWR MGMT
DDR3 MISC
JTAG & BPM
SKTOCC*
PROC_SEL
CATERR*
PECI
PROCHOT*
THERMTRIP*
RESET*
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
SM_DRAMRST*
SM_VREF
SB_DIMM_VREFDQ
SA_DIMM_VREFDQ
BCLK_ITP
BCLK_ITP*
BCLK_0
BCLK_0*
PRDY*
PREQ*
TCK
TMS
TRST*
TDI
TDO
DBR*
BPM[0]*
BPM[1]*
BPM[2]*
BPM[3]*
BPM[4]*
BPM[5]*
BPM[6]*
BPM[7]*
ITPCPU_CLK100M_P
ITPCPU_CLK100M_N
DMI_CLK100M_CPU_P
DMI_CLK100M_CPU_N
XDP_CPU_PRDY_L
XDP_CPU_PREQ_L
XDP_CPU_TCK
XDP_CPU_TMS
XDP_CPU_TRST_L
XDP_CPU_TDI
XDP_CPU_TDO
XDP_DBRESET_L
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_BPM_L<6>
XDP_BPM_L<7>
=PP1V5_S0_CPU_MEM
R1140
1K
CPU_DDR_VREF
R1141
1K
C1140
0.1UF
X7R-CERM
402

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE
CPU CLOCK/MISC/JTAG

Apple Inc.

DRAWING NUMBER 051-9179 SIZE D

REVISION 16.0.0

BRANCH

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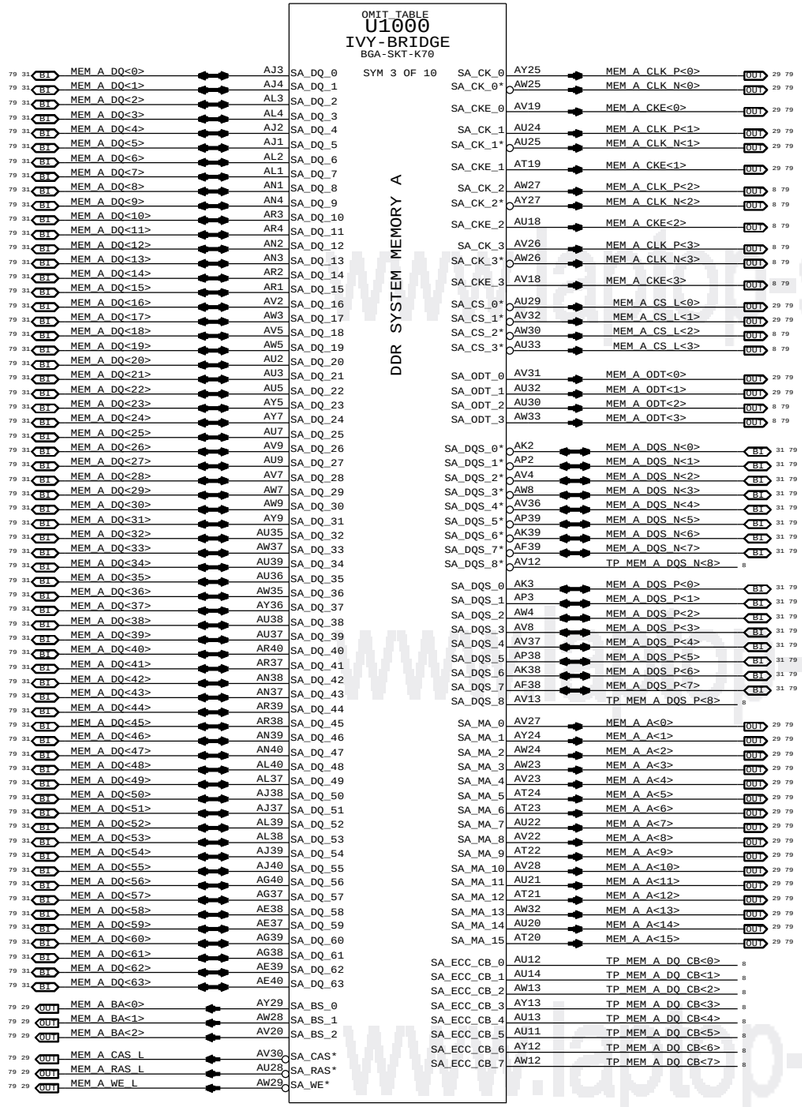

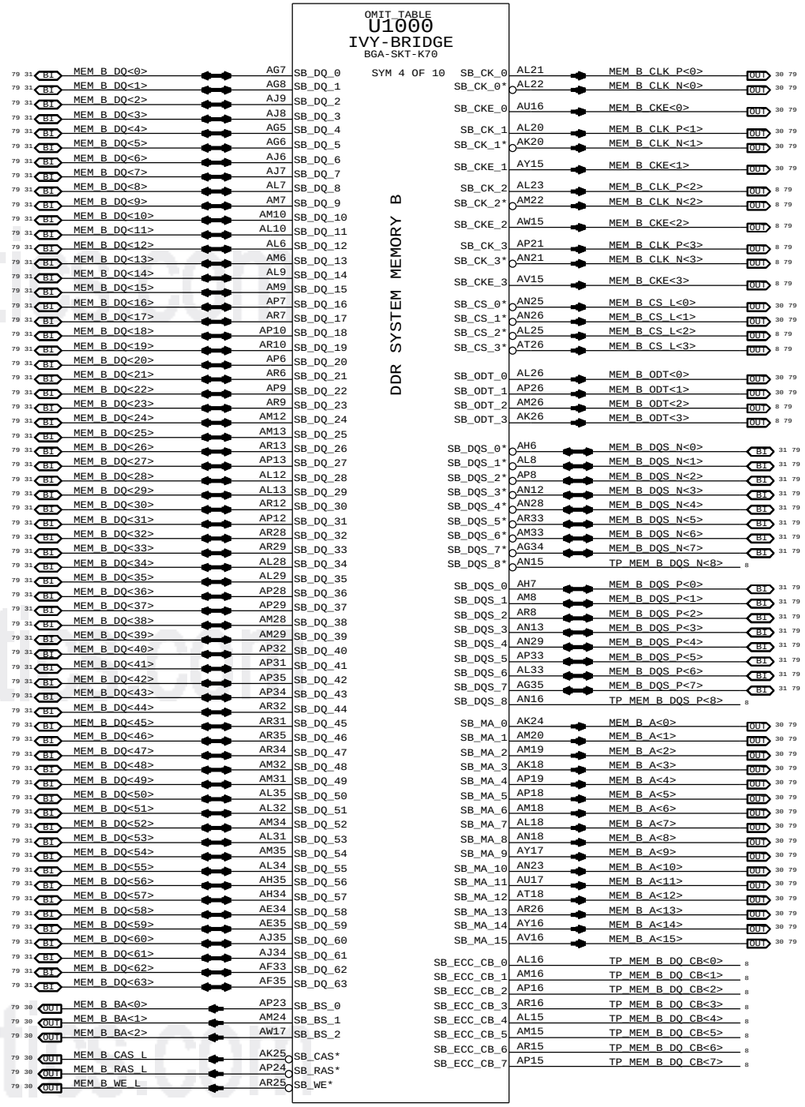

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

DRAWING NUMBER 051-9179 SIZE D

REVISION 16.0.0

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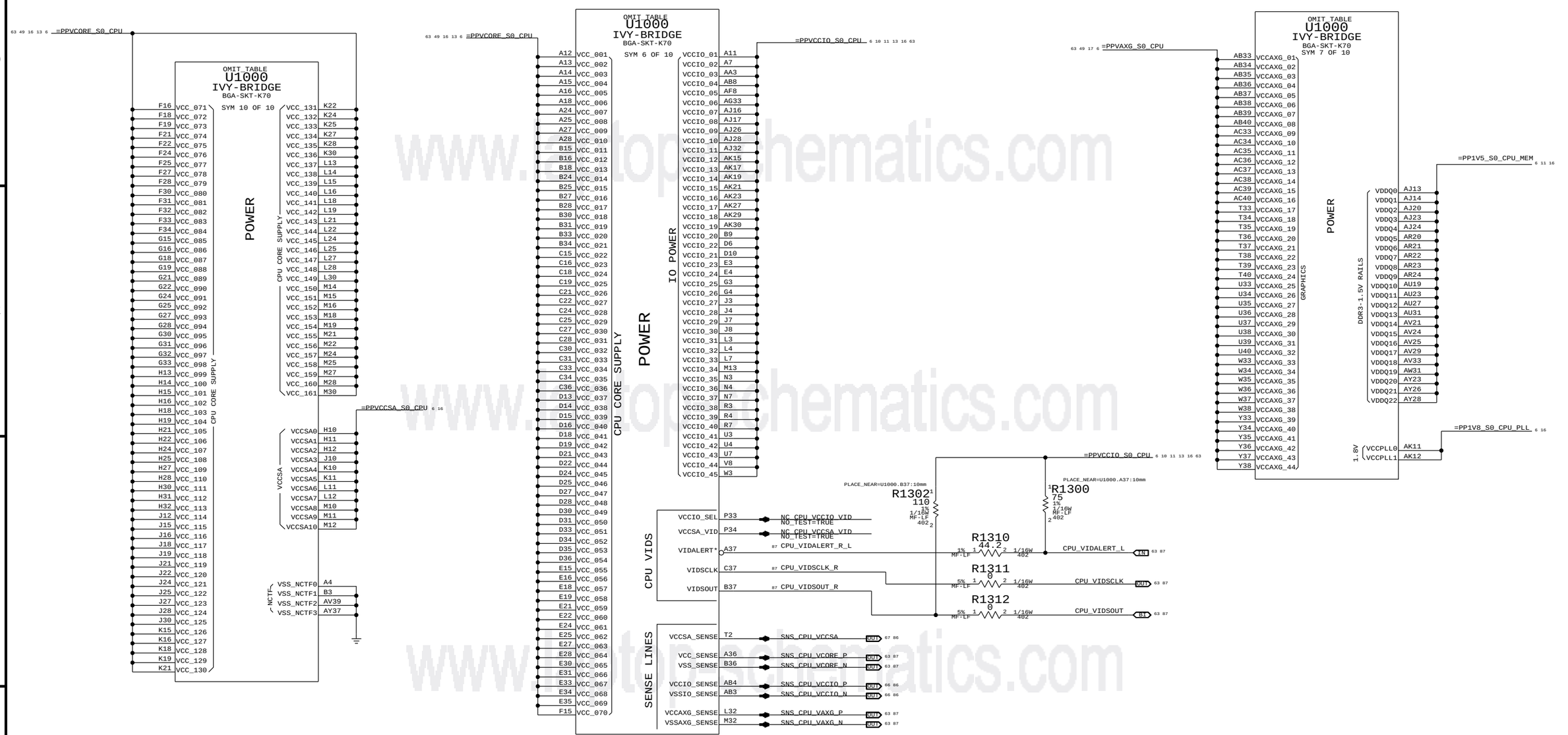

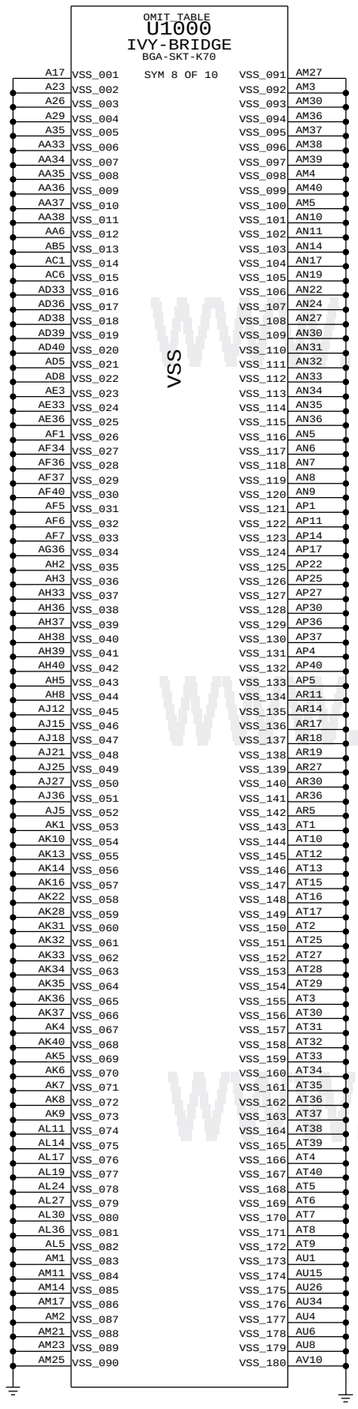

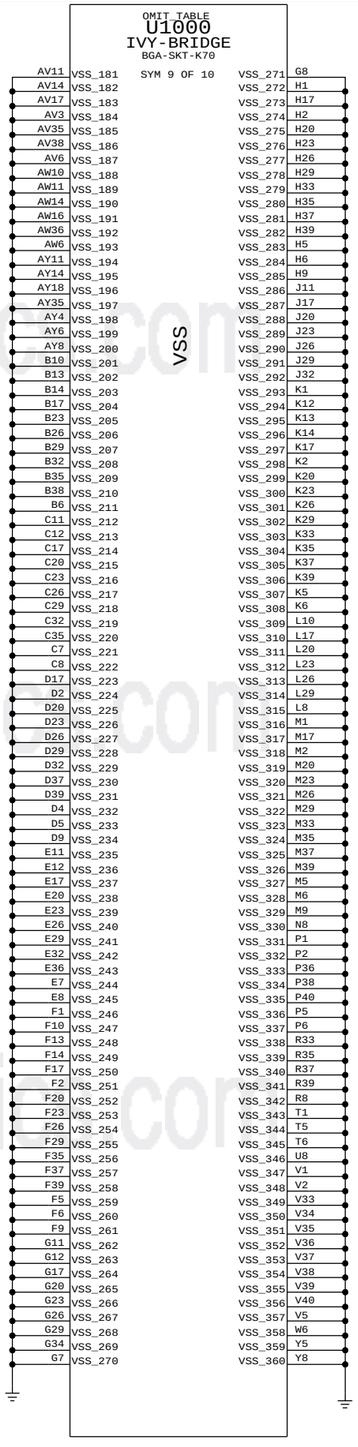

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE

CPU GROUNDS

Apple Inc.

DRAWING NUMBER 051-9179 SIZE D

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=PP3V3_S5_PCH_STRAPS
R1501 10K 5% 1/16W MF-LF 402 — SMC_WAKE_SCI_L
R1502 10K 5% 1/16W MF-LF 402 — TBT_GO2SX_BIDIR
R1504 10K 5% 1/16W MF-LF 402 — PCH_SUSWARN_L
R1563 10K 5% 1/16W MF-LF 402 — PCH_GPIO72
R1564 1K 5% 1/16W MF-LF 402 — PM_PWRBTN_L
R1590 10K 5% 1/16W MF-LF 402 — PCH_SMBALERT_L

=PP3V3_S5_PCH_STRAPS
R1519 10K 5% 1/16W MF-LF 402 — USB_EXTA_OC_L
R1518 10K 5% 1/16W MF-LF 402 — USB_EXTB_OC_L
R1517 10K 5% 1/16W MF-LF 402 — USB_EXTC_OC_L
R1516 10K 5% 1/16W MF-LF 402 — USB_EXTD_OC_L
R1536 1K 5% 1/16W MF-LF 402 — USB_EXTB_OC_EHCI_L
R1537 1K 5% 1/16W MF-LF 402 — USB_EXTD_OC_EHCI_L

=PP3V3_S4_SDCARD
R1520 10K 5% 1/16W MF-LF 402 — SDCONN_STATE_CHANGE

NOSTUFF R1553 0 5% 1/16W MF-LF 402 — ITPXDP_CLK100M_N — ITPCPU_CLK100M_N
NOSTUFF R1554 0 5% 1/16W MF-LF 402 — ITPXDP_CLK100M_P — ITPCPU_CLK100M_P

=PP3V3_S0_LED_SATA
R1556 10K 5% 1/16W MF-LF 402 — PCH_SATALED_L

=PP3V3_S4_PCH
R1505 10K 5% 1/16W MF-LF 402 — AP_PWR_EN

=PP3V3_S5_PCH_STRAPS
SPI_DESCRIPTOR_OVERRIDE_L
CRITICAL Q1500 SOT23-3_MF NTR1P02L
PLACE_NEAR=R1805.4:3mm
SPI_DESCRIPTOR_OVERRIDE_R — 330 5% 1/16W MF-LF 402 R1552 — HDA_SDOUT_R

=PP3V3_S0_PCH_GPIO
R1558 10K 5% 1/16W MF-LF 402 — BT_PWR_RST_L
R1557 10K 5% 1/16W MF-LF 402 — TBT_PWR_REQ_L

=PP3V3_S0_PCH_STRAPS
R1509 10K 5% 1/16W MF-LF 402 — DP_AUXCH_ISOL
R1510 10K 5% 1/16W MF-LF 402 — PCH_GPIO1
R1511 10K 5% 1/16W MF-LF 402 — PCH_GPIO48

DP_AUXIO_EN Inversion

Inverts PCH GPIO DP_AUXCH_ISOL to drive DP_AUXIO_EN for external DP

=PP3V3_S0_PCH_STRAPS
R1507 10K 5% 1/16W MF-LF 402 — DP_AUXIO_EN (OUT)
CRITICAL Q1509 SSM3K15AMFVAPE VESM
DP_AUXCH_ISOL

=PP3V3_S0_PCH_STRAPS
NOSTUFF R1529 4.7K 5% 1/16W MF-LF 402 — PCH_SPKR
R1528 10K 5% 1/16W MF-LF 402 — SATARDRVR_EN
R1525 10K 5% 1/16W MF-LF 402 — MLB_RAM_CFG1
R1524 10K 5% 1/16W MF-LF 402 — MLB_RAM_CFG0
R1542 10K 5% 1/16W MF-LF 402 — SMC_RUNTIME_SCI_L
R1526 10K 5% 1/16W MF-LF 402 — PCH_CAM_RESET
R1527 10K 5% 1/16W MF-LF 402 — PCH_CAM_EXT_BOOT

=PP3V3_S0_PCH_STRAPS
R1540 10K 5% 1/16W MF-LF 402 — TBT_CLKREQ_L
R1539 10K 5% 1/16W MF-LF 402 — ENET_CLKREQ_L
R1538 10K 5% 1/16W MF-LF 402 — AP_CLKREQ_L
R1541 10K 5% 1/16W MF-LF 402 — SSD_CLKREQ_L
R1508 10K 5% 1/16W MF-LF 402 — PEG_CLKREQ_L

=PP3V3_TBT_PCH_GPIO
R1562 10K 5% 1/16W MF-LF 402 — JTAG_TBT_TDO
R1561 10K 5% 1/16W MF-LF 402 — JTAG_TBT_TDI
R1560 10K 5% 1/16W MF-LF 402 — JTAG_TBT_TMS
NOSTUFF R1559 10K 5% 1/16W MF-LF 402 — TBT_SW_RESET_R_L
R1567 10K 5% 1/16W MF-LF 402 — JTAG_TBT_TCK

HDA_SYNC — 1K 5% 1/16W MF-LF 402 R1514

IVB PCIe Straps configuration:

CFG[5:6] = Sel PCIe Cfg
11 = 1x16 (default)
10 = 2x8
00 = 1x8,2x4

CFG[3]=Direct/Rev for X4
1 = DIR
0 = REV

CFG[2]= Direct/Rev for x16
1 = DIR
0 = REV

CPU_CFG<5> — 1K NOSTUFF R1512 5% 1/16W MF-LF 402
CPU_CFG<6> — 1K NOSTUFF R1513 5% 1/16W MF-LF 402
CPU_CFG<3> — 1K NOSTUFF R1523 5% 1/16W MF-LF 402
U1000.18:3mm
CPU_CFG<2> — 1K R1522 5% 1/16W MF-LF 402

PM_SLP_S5_L — 100K R1570 5% 1/16W MF-LF 402
PM_SLP_S4_L — 100K R1571 5% 1/16W MF-LF 402
PM_SLP_S3_L — 100K R1572 5% 1/16W MF-LF 402
PCH_GPIO22 — 10K R1533 5% 1/16W MF-LF 402
PCH_GPIO6 — 20K R1532 5% 1/16W MF-LF 402
ENET_MEDIA_SENSE — 10K R1531 5% 1/16W MF-LF 402
WOL_EN — 10K R1530 5% 1/16W MF-LF 402
PCH_GPIO29 — 10K R1555 5% 1/16W MF-LF 402
TBT_CIO_PLUG_EVENT — 10K R1521 5% 1/16W MF-LF 402
ENET_LOW_PWR_PCH — 10K R1503 5% 1/16W MF-LF 402

UNUSED clock terminations for FCIM MODE

PCH_CLKIN_GND1 — 10K R1551 5% 1/16W MF-LF 402
PCH_CLKIN_GND0 — 10K R1550 5% 1/16W MF-LF 402
PCH_CLK14P3M_REFCLK — 10K R1549 5% 1/16W MF-LF 402
PCH_CLK100M_DMIN — 10K R1548 5% 1/16W MF-LF 402 PLACE_NEAR=U1800.P33:5mm
PCH_CLK100M_DMIP — 10K R1547 5% 1/16W MF-LF 402 PLACE_NEAR=U1800.R33:5mm
PCH_CLK100M_SATAN — 10K R1546 5% 1/16W MF-LF 402 PLACE_NEAR=U1800.AF55:5mm
PCH_CLK100M_SATAP — 10K R1545 5% 1/16W MF-LF 402 PLACE_NEAR=U1800.AG56:5mm
PCH_CLK96M_DOTN — 10K R1544 5% 1/16W MF-LF 402 PLACE_NEAR=U1800.BD38:5mm
PCH_CLK96M_DOTP — 10K R1543 5% 1/16W MF-LF 402 PLACE_NEAR=U1800.BF38:5mm

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012
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CPU VCORE DECOUPLING

14x 22UF,0805 INTEL RECOMMENDATION 18X 22UF 0805 (14 Inside cavity and 4 North of processor)

PLACEMENT_NOTE (C1600-C1613): REPALCED WITH 603 PER RDAR://10700439

16 13 6 63 49 =PPVCORE_S0_CPU

C1600 22UF 20% 6.3V X5R-CERM2 0603
C1601 22UF 20% 6.3V X5R-CERM2 0603
C1602 22UF 20% 6.3V X5R-CERM2 0603
C1603 22UF 20% 6.3V X5R-CERM2 0603
C1604 22UF 20% 6.3V X5R-CERM2 0603
C1605 22UF 20% 6.3V X5R-CERM2 0603
C1606 22UF 20% 6.3V X5R-CERM2 0603
C1607 22UF 20% 6.3V X5R-CERM2 0603
C1608 22UF 20% 6.3V X5R-CERM2 0603
C1609 22UF 20% 6.3V X5R-CERM2 0603
C1610 22UF 20% 6.3V X5R-CERM2 0603
C1611 22UF 20% 6.3V X5R-CERM2 0603
C1612 22UF 20% 6.3V X5R-CERM2 0603
C1613 22UF 20% 6.3V X5R-CERM2 0603

BULK CAPS ON CPU VREG PAGE 72

63 49 16 13 6 =PPVCORE_S0_CPU

10x 10UF and 10x 1UF CAPACITORS

Place inside socket cavity

C1620 10UF 20% 6.3V X5R 603
C1621 10UF 20% 6.3V X5R 603
C1622 10UF 20% 6.3V X5R 603
C1623 10UF 20% 6.3V X5R 603
C1624 10UF 20% 6.3V X5R 603
C1625 10UF 20% 6.3V X5R 603
C1626 10UF 20% 6.3V X5R 603
C1627 10UF 20% 6.3V X5R 603
C1628 10UF 20% 6.3V X5R 603
C1629 10UF 20% 6.3V X5R 603
C1630 1UF 10% 16V X5R 402
C1631 1UF 10% 16V X5R 402
C1632 1UF 10% 16V X5R 402
C1633 1UF 10% 16V X5R 402
C1634 1UF 10% 16V X5R 402
C1635 1UF 10% 16V X5R 402
C1636 1UF 10% 16V X5R 402
C1637 1UF 10% 16V X5R 402
C1638 1UF 10% 16V X5R 402
C1639 1UF 10% 16V X5R 402

CPU VCCIO DECOUPLING

8X 22UF 0805, 6X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805,16X 0805 placeholders

13 11 10 6 63 =PPVCCIO_S0_CPU

PLACEMENT_NOTE (C1650-C1657):

C1650 22UF 20% 6.3V X5R-CERM2 0603
C1651 22UF 20% 6.3V X5R-CERM2 0603
C1652 22UF 20% 6.3V X5R-CERM2 0603
C1653 22UF 20% 6.3V X5R-CERM2 0603
C1654 22UF 20% 6.3V X5R-CERM2 0603
C1655 22UF 20% 6.3V X5R-CERM2 0603
C1656 22UF 20% 6.3V X5R-CERM2 0603
C1657 22UF 20% 6.3V X5R-CERM2 0603

PLACEMENT_NOTE (C1660-C1665):

Place at edge of socket.

C1660 10UF 20% 6.3V X5R 603
C1661 10UF 20% 6.3V X5R 603
C1662 10UF 20% 6.3V X5R 603
C1663 10UF 20% 6.3V X5R 603
C1664 10UF 20% 6.3V X5R 603
C1665 10UF 20% 6.3V X5R 603

BULK CAPS ON CPU VREG PAGE 74

CRITICAL
C1670 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

CPU VCCSA DECOUPLING

2x 10uF 0603. INTEL RECOMMENDATION 2X 10uF 0805

13 6 =PPVCCSA_S0_CPU

C1666 10UF 20% 6.3V X5R 603
C1667 10UF 20% 6.3V X5R 603

Bulk decoupling is on VCCSA reg page 75

Memory (CPU VCCDDR) DECOUPLING

13 11 6 =PP1V5_S0_CPU_MEM

C1676 22UF 20% 6.3V X5R-CERM2 0603
C1677 22UF 20% 6.3V X5R-CERM2 0603
C1678 22UF 20% 6.3V X5R-CERM2 0603
C1679 22UF 20% 6.3V X5R-CERM2 0603
C1680 22UF 20% 6.3V X5R-CERM2 0603
C1681 22UF 20% 6.3V X5R-CERM2 0603
C1682 1UF 20% 6.3V X5R 0201
C1683 1UF 20% 6.3V X5R 0201
C1684 1UF 20% 6.3V X5R 0201
C1685 1UF 20% 6.3V X5R 0201
C1686 1UF 20% 6.3V X5R 0201

NOSTUFF
CRITICAL
C1687 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

PLL (CPU VCCSFR) DECOUPLING

2x 47uF, 1x 22uF 0805, 1x 10uF 0603, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402. INTEL RECOMMENDATION 1x 10uF 0805

13 6 =PP1V8_S0_CPU_PLL

C1693 1UF 10% 16V X5R 402
C1694 1UF 10% 16V X5R 402
C1692 2.2UF 10% 6.3V X5R 402
C1691 4.7UF 10% 6.3V X5R-CERM 603
C1695 10UF 20% 6.3V X5R 603
C1690 22UF 20% 6.3V X5R-CERM2 0603
C1696 47UF 20% 6.3V X5R 0805
C1697 47UF 20% 6.3V X5R 0805

BULK CAPS ON VTT REG PAGE 77

SYNC_MASTER=D7 MLB SYNC_DATE=01/19/2012

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CPU NON-GFX DECOUPLING

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VAXG DECOUPLING

INTEL RECOMMENDATION 4X22UF 0805,3X 4.7UF

PLACEMENT_NOTE (C1704-C1709):

Place inside socket cavity

63 49 13 6 =PPVAXG_S0_CPU

C1704 22UF 20% 6.3V X5R-CERM2 0603
C1705 22UF 20% 6.3V X5R-CERM2 0603
C1706 22UF 20% 6.3V X5R-CERM2 0603
C1707 22UF 20% 6.3V X5R-CERM2 0603
C1708 22UF 20% 6.3V X5R-CERM2 0603
C1709 22UF 20% 6.3V X5R-CERM2 0603

C1710 4.7UF 10% 6.3V X5R-CERM 603
C1711 4.7UF 10% 6.3V X5R-CERM 603
C1712 4.7UF 10% 6.3V X5R-CERM 603

BULK CAPS ON CPU VREG PAGE 73

6 =PP3V3_S0_PCH_VCC_ADAC — R1720 0 5% 1/16W MF-LF 402 — PP3V3_S0_PCH_VCCA_DAC_F 22
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

CRITICAL IG:Y C1720 10UF 20% 6.3V X5R 603
IG:Y C1721 0.1UF 10% 16V X5R 402
IG:Y C1722 0.01UF 10% 16V CERM 402

6 =PP1V05_S0_PCH_VCC_ADPLL — R1730 0 5% 1/16W MF-LF 402 — PP1V05_S0_PCH_VCCADPLLA_R
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V

OMIT_TABLE
CRITICAL
L1730 10UH-0.12A-0.36OHM 0603

CRITICAL IG:Y C1730 220UF 20% 2.5V TANT B16
NOSTUFF C1731 1UF 10% 6.3V CERM 402

PP1V05_S0_PCH_VCCADPLLA_F 22 24
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V

R1740 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCCADPLLB_R
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V

OMIT_TABLE
CRITICAL
L1740 10UH-0.12A-0.36OHM 0603

CRITICAL IG:Y C1740 220UF 20% 2.5V TANT B16
NOSTUFF C1741 1UF 10% 6.3V CERM 402

PP1V05_S0_PCH_VCCADPLLB_F 22 24
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1070	2	IND,WW,10UH,20%.120MA,0.36OHMS	L1730,L1740	CRITICAL	IG:Y
113S0022	2	RES,MF,1/10W,0OHM,5,0603,SMD,LF	L1730,L1740		IG:N

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

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PCIE_SSD_D2R_N<0> … PCIE_SSD_R2D_C_P<0>

PCIE_SSD_D2R_N<0>	IN	J20	PERN1
PCIE_SSD_D2R_P<0>	IN	J20	PERP1
PCIE_SSD_R2D_C_N<0>	OUT	E25	PETN1
PCIE_SSD_R2D_C_P<0>	OUT	E23	PETP1
PCIE_SSD_D2R_N<1>	IN	P20	PERN2
PCIE_SSD_D2R_P<1>	IN	N20	PERP2
PCIE_SSD_R2D_C_N<1>	OUT	E22	PETN2
PCIE_SSD_R2D_C_P<1>	OUT	A22	PETP2
PCIE_ENET_D2R_N	IN	H17	PERN3
PCIE_ENET_D2R_P	IN	J17	PERP3
PCIE_ENET_R2D_C_N	OUT	E21	PETN3
PCIE_ENET_R2D_C_P	OUT	B21	PETP3
PCIE_AP_D2R_N	IN	B17	PERN4
PCIE_AP_D2R_P	IN	A17	PERP4
PCIE_AP_R2D_C_N	OUT	E18	PETN4
PCIE_AP_R2D_C_P	OUT	E17	PETP4
PCIE_TBT_D2R_N<0>	IN	N15	PERN5
PCIE_TBT_D2R_P<0>	IN	M15	PERP5
PCIE_TBT_R2D_C_N<0>	OUT	B17	PETN5
PCIE_TBT_R2D_C_P<0>	OUT	C16	PETP5
PCIE_TBT_D2R_N<1>	IN	J15	PERN6
PCIE_TBT_D2R_P<1>	IN	J15	PERP6
PCIE_TBT_R2D_C_N<1>	OUT	A16	PETN6
PCIE_TBT_R2D_C_P<1>	OUT	B15	PETP6
PCIE_TBT_D2R_N<2>	IN	J12	PERN7
PCIE_TBT_D2R_P<2>	IN	H12	PERP7
PCIE_TBT_R2D_C_N<2>	OUT	E15	PETN7
PCIE_TBT_R2D_C_P<2>	OUT	E13	PETP7
PCIE_TBT_D2R_N<3>	IN	H10	PERN8
PCIE_TBT_D2R_P<3>	IN	J10	PERP8
PCIE_TBT_R2D_C_N<3>	OUT	B13	PETN8
PCIE_TBT_R2D_C_P<3>	OUT	D13	PETP8

PCIE_CLK100M_SSD_N … PCIE_CLK100M_TBT_P

PCIE_CLK100M_SSD_N	OUT	AE6	CLKOUT_PCIE0N
PCIE_CLK100M_SSD_P	OUT	AC6	CLKOUT_PCIE0P
PCIE_CLK100M_AP_N	OUT	AA5	CLKOUT_PCIE1N
PCIE_CLK100M_AP_P	OUT	W5	CLKOUT_PCIE1P
PCIE_CLK100M_TBT_N	OUT	AB12	CLKOUT_PCIE2N
PCIE_CLK100M_TBT_P	OUT	AB14	CLKOUT_PCIE2P
PEG_CLKREQ_L	IN	AV43	PCIECLKRQ2*/GPIO20/SMI*
PCIE_CLK100M_ENET_N	OUT	AB9	CLKOUT_PCIE3N
PCIE_CLK100M_ENET_P	OUT	AB8	CLKOUT_PCIE3P
TP_PCIE_CLK100M_PE4N	OUT	Y9	CLKOUT_PCIE4N
TP_PCIE_CLK100M_PE4P	OUT	Y8	CLKOUT_PCIE4P
PEG_CLK100M_N	OUT	AF3	CLKOUT_PCIE5N
PEG_CLK100M_P	OUT	AG2	CLKOUT_PCIE5P
PCIE_CLKREQ5_GPIO44_L	IN	BL54	PCIECLKRQ5*/GPIO44
DMI_MIDBUS_CLK100M_N	OUT	AE12	CLKOUT_PEG_B_N
DMI_MIDBUS_CLK100M_P	OUT	AE11	CLKOUT_PEG_B_P

OMIT TABLE
U1800
PANTHER-POINT
FCBGA
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SMBUS

SMBALERT*/GPIO11	BN49	PCH_SMBALERT_L	15
SMBCLK	BT47	SMBUS_PCH_CLK	OUT 48 85
SMBDATA	BR49	SMBUS_PCH_DATA	BI 48 85
SML0ALERT*/GPIO60	BU49	USB_EXTB_SEL_XHCI	OUT 43
SML0CLK	BT51	SML_PCH_0_CLK	OUT 48 85
SML0DATA	BM50	SML_PCH_0_DATA	BI 48 85
SML1ALERT*/PCHHOT*/GPIO74	BR46	USB_EXTD_SEL_XHCI	OUT 44
SML1CLK/GPIO58	BJ46	SML_PCH_1_CLK	OUT 48
SML1DATA/GPIO75	BK46	SML_PCH_1_DATA	BI 48

PEG

CLKOUT_PEG_A_N	AG8	TP_CLKOUT_PEG_A_N	OUT 8
CLKOUT_PEG_A_P	AG9	TP_CLKOUT_PEG_A_P	OUT 8
CLKOUT_DMI_N	P31	DMI_CLK100M_CPU_N	OUT 11 81
CLKOUT_DMI_P	R31	DMI_CLK100M_CPU_P	OUT 11 81

PCI-E* FROM CLK BUFFER

CLKOUT_DP_N	N56	TP_PCH_CLKOUT_DPN	OUT 8
CLKOUT_DP_P	M55	TP_PCH_CLKOUT_DPP	OUT 8
CLKIN_DMI_N	P33	PCH_CLK100M_DMIN	IN 15
CLKIN_DMI_P	R33	PCH_CLK100M_DMIP	IN 15
CLKIN_DOT_96N	BD38	PCH_CLK96M_DOTN	IN 15
CLKIN_DOT_96P	BF38	PCH_CLK96M_DOTP	IN 15
CLKIN_SATA_N	AF55	PCH_CLK100M_SATAN	IN 15
CLKIN_SATA_P	AG56	PCH_CLK100M_SATAP	IN 15
REFCLK14IN	AN8	PCH_CLK14P3M_REFCLK	IN 15
CLKIN_PCILOOPBACK	BD15	PCH_CLK33M_PCIIN (DOES THIS NEED LENGTH MATCH???)	IN 26 83
XTAL25_IN	AJ3	PCH_CLK25M_XTALIN	IN 26 83
XTAL25_OUT	AJ5	PCH_CLK25M_XTALOUT	8
XCLK_RCOMP	AL2	PCH_XCLK_RCOMP	83

=PP1V05_S0_PCH_VCCIO_PCIE 6 19 22
PLACE_NEAR=U1800.AL2:2mm
R1890 90.9 1% MF-LF 1/16W 402

CLOCK FLEX

CLKOUTFLEX0/GPIO64	AT9	TP_PCH_GPIO64_CLKOUTFLEX0	8
CLKOUTFLEX1/GPIO65	BA5	TP_PCH_GPIO65_CLKOUTFLEX1	8
CLKOUTFLEX2/GPIO66	AW5	TP_PCH_GPIO66_CLKOUTFLEX2	8
CLKOUTFLEX3/GPIO67	BA2	TP_PCH_GPIO67_CLKOUTFLEX3	8
CLKOUT_ITPXDP_N	R52	ITPXDP_CLK100M_N	15 25 82
CLKOUT_ITPXDP_P	N52	ITPXDP_CLK100M_P	15 25 82
CLKIN_GND0_N	W53	PCH_CLKIN_GND0	15
CLKIN_GND0_P	V52		
CLKIN_GND1_N	R27	PCH_CLKIN_GND1	15
CLKIN_GND1_P	P27		
CL_CLK1	BA50	TP_PCH_CL_CLK1	8
CL_DATA1	BF50	TP_PCH_CL_DATA1	8
CL_RST1*	BF49	TP_PCH_CL_RST1	8

R1851 0 5% 1/16W MF-LF 402
SSD_CLKREQ_L (42 15) — 1
NOSTUFF
R1852 0 5% 1/16W MF-LF 402
ENET_CLKREQ_L (37 15) — 1
2 — PCIE_CLKREQ5_GPIO44_L (18)

PCH_CLK32K_RTCX1	IN	BR39	RTCX1
PCH_CLK32K_RTCX2	OUT	BN39	RTCX2
RTC_RESET_L		BT41	RTCRST*
PCH_SRTCRST_L		BN37	SRTCRST*
PCH_INTRUDER_L		BM38	INTRUDER*
PCH_INTVRMEN		BN41	INTVRMEN
HDA_BIT_CLK_R		BU22	HDA_BCLK
HDA_SYNC_R		BP23	HDA_SYNC
PCH_SPKR		BE56	SPKR
HDA_RST_R_L		BC22	HDA_RST*
HDA_SDIN0	IN	BD22	HDA_SDIN0
TP_HDA_SDIN1		BF22	HDA_SDIN1
TP_HDA_SDIN2		BK22	HDA_SDIN2
TP_HDA_SDIN3		BJ22	HDA_SDIN3
HDA_SDOUT_R		BT23	HDA_SDO
JTAG_TBT_TMS		BC25	GPIO33
ENET_MEDIA_SENSE		BA25	GPIO13
XDP_PCH_TCK		BA43	JTAG_TCK
XDP_PCH_TMS		BC50	JTAG_TMS
XDP_PCH_TDI		BC52	JTAG_TDI
XDP_PCH_TDO		BF47	JTAG_TDO
SPI_CLK_R	OUT	AR54	SPI_CLK
SPI_CS0_R_L	OUT	AT57	SPI_CS0*
NC_SPI_CS1_L NO_TEST=TRUE		AR56	SPI_CS1*
SPI_MOSI_R	OUT	AU53	SPI_MOSI
SPI_MISO	IN	AT55	SPI_MISO

OMIT TABLE
U1800
PANTHER-POINT
FCBGA
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RTC / LPC

FWH0/LAD0	BK15	LPC_R_AD<0> — R1860 33 1/16W — LPC_AD<0>	BI 45 47 83
FWH1/LAD1	BJ17	LPC_R_AD<1> — R1861 33 1/16W — LPC_AD<1>	BI 45 47 83
FWH2/LAD2	BJ20	LPC_R_AD<2> — R1862 33 1/16W — LPC_AD<2>	BI 45 47 83
FWH3/LAD3	BG20	LPC_R_AD<3> — R1863 33 1/16W — LPC_AD<3>	BI 45 47 83
FWH4/LFRAME*	BG17	LFRAME_L — R1864 33 1/16W — LPC_FRAME_L	OUT 45 47 83
LDRQ0*	BK17	TP_LPC_DREQ0_L	8
LDRQ1*/GPIO23	BA20	TBT_PWR_EN_PCH	26
SERIRQ	AV52	LPC_SERIRQ	BI 45 47

=PP3V3_S0_PCH 6 21 24
R1820 10K 5% 1/16W MF-LF 402

SATA

SATA0RXN	AC56	SATA_HDD_D2R_N	IN 42 82
SATA0RXP	AB55	SATA_HDD_D2R_P	IN 42 82
SATA0TXN	AE46	SATA_HDD_R2D_C_N	OUT 42 82
SATA0TXP	AE44	SATA_HDD_R2D_C_P	OUT 42 82
SATA1RXN	AA53	SATA_SSD_D2R_N	IN 42 82
SATA1RXP	AA56	SATA_SSD_D2R_P	IN 42 82
SATA1TXN	AG49	SATA_SSD_R2D_C_N	OUT 42 82
SATA1TXP	AG47	SATA_SSD_R2D_C_P	OUT 42 82
SATA2RXN	AL50	TP_SATA_C_D2RN	8
SATA2RXP	AL49	TP_SATA_C_D2RP	8
SATA2TXN	AL56	TP_SATA_C_R2D_CN	8
SATA2TXP	AL53	TP_SATA_C_R2D_CP	8
SATA3RXN	AN46	TP_SATA_D_D2RN	8
SATA3RXP	AN44	TP_SATA_D_D2RP	8
SATA3TXN	AN56	TP_SATA_D_R2D_CN	8
SATA3TXP	AM55	TP_SATA_D_R2D_CP	8
SATA4RXN	AN49	TP_SATA_E_D2RN	8
SATA4RXP	AN50	TP_SATA_E_D2RP	8
SATA4TXN	AT50	TP_SATA_E_R2D_CN	8
SATA4TXP	AT49	TP_SATA_E_R2D_CP	8
SATA5RXN	AT46	TP_SATA_F_D2RN	8
SATA5RXP	AT44	TP_SATA_F_D2RP	8
SATA5TXN	AV50	TP_SATA_F_R2D_CN	8
SATA5TXP	AV49	TP_SATA_F_R2D_CP	8
SATAICOMPO	AJ53	PCH_SATAICOMP	82
SATAICOMPI	AJ55	TIE THEM TOGETHER VERY CLOSE TO PINS. PLACE THE RESISTOR LESS THAN 200MILS FROM THE PINS	
SATALED*	BF57	PCH_SATALED_L	15 42
SATA0GP/GPIO21	BC54	DP_AUXCH_ISOL_R — R1841 0 5% 1/20W MF 201 — DP_AUXCH_ISOL	OUT 15
SATA1GP/GPIO19	AV52	SATARDRVR_EN_R — R1842 0 5% 1/20W MF 201 — SATARDRVR_EN	OUT 15
SATA3COMPI	AE54		
SATA3RCOMPO	AE52	PCH_SATA3COMP	82
SATA3RBIAS	AC52	PCH_SATA3RBIAS	82

=PP1V05_S0_PCH_VCCIO_SATA 6 22 24
PLACE_NEAR=U1800.AJ53:2mm
R1830 37.4 1% 1/16W MF-LF 402

=PP1V05_S0_PCH 6 24
PLACE_NEAR=U1800.AE52:2mm
R1831 49.9 1% 1/16W MF-LF 402

PLACE_NEAR=U1800.AC52:2mm
R1832 750 1% 1/16W MF-LF 402

IHDA

L_BKLTCTL	AG12	TP_PCH_L_BKLTCTL	9
L_BKLTEN	AG18	TP_PCH_L_BKLTEN	8
L_VDD_EN	AG17	TP_PCH_L_VDD_EN	8

R1805 33 5% 1/16W SM-LF

HDA_SDOUT_R	83 18 15	HDA_SDOUT	OUT 53 83
HDA_BIT_CLK_R	83 18	HDA_BIT_CLK	OUT 53 83
HDA_SYNC_R	83 18	HDA_SYNC	OUT 15 53 83
HDA_RST_R_L	83 18	HDA_RST_L	OUT 53 83

PLACE THIS RESISTOR PACK CLOSE TO PCH (MIN 500MIL)

=PP3V3_G3_PCH 19 6
R1800 390K 5% 1/16W MF-LF 402
R1801 1M 5% 1/16W MF-LF 402
R1802 20K 5% 1/16W MF-LF 402
R1803 20K 5% 1/16W MF-LF 402

RTC_RESET_L	18 46
PCH_SRTCRST_L	18
PCH_INTRUDER_L	
PCH_INTVRMEN	

C1802 1UF 10% 6V X5R 402
C1803 1UF 10% 16V X5R 402

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012
PAGE TITLE
PCH SATA/PCIE/CLK/LPC/SPI

Apple Inc.

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U1800 PANTHER-POINT (3 OF 10) FCBGA

OMIT TABLE

DMI_N2S_N<0>	D33	DMI0RXN	
DMI_N2S_N<1>	A36	DMI1RXN	
DMI_N2S_N<2>	B37	DMI2RXN	
DMI_N2S_N<3>	E37	DMI3RXN	
DMI_N2S_P<0>	B33	DMI0RXP	
DMI_N2S_P<1>	B35	DMI1RXP	
DMI_N2S_P<2>	C36	DMI2RXP	
DMI_N2S_P<3>	F38	DMI3RXP	
DMI_S2N_N<0>	J36	DMI0TXN	
DMI_S2N_N<1>	P38	DMI1TXN	
DMI_S2N_N<2>	H38	DMI2TXN	
DMI_S2N_N<3>	M41	DMI3TXN	
DMI_S2N_P<0>	H36	DMI0TXP	
DMI_S2N_P<1>	R38	DMI1TXP	
DMI_S2N_P<2>	J38	DMI2TXP	
DMI_S2N_P<3>	P41	DMI3TXP	
PCH_DMI2RBIAS	A32	DMI2RBIAS	
PCH_DMI_COMP	E31	DMI_ZCOMP	
	B31	DMI_IRCOMP	

DMI / FDI

FDI_RXN0	C42	PCH_FDI_RX_N<0>	9
FDI_RXN1	F45	PCH_FDI_RX_N<1>	9
FDI_RXN2	H41	PCH_FDI_RX_N<2>	9
FDI_RXN3	C46	PCH_FDI_RX_N<3>	9
FDI_RXN4	B45	PCH_FDI_RX_N<4>	9
FDI_RXN5	B47	PCH_FDI_RX_N<5>	9
FDI_RXN6	J43	PCH_FDI_RX_N<6>	9
FDI_RXN7	M43	PCH_FDI_RX_N<7>	9
FDI_RXP0	B43	PCH_FDI_RX_P<0>	9
FDI_RXP1	F43	PCH_FDI_RX_P<1>	9
FDI_RXP2	J41	PCH_FDI_RX_P<2>	9
FDI_RXP3	D47	PCH_FDI_RX_P<3>	9
FDI_RXP4	A46	PCH_FDI_RX_P<4>	9
FDI_RXP5	C49	PCH_FDI_RX_P<5>	9
FDI_RXP6	H43	PCH_FDI_RX_P<6>	9
FDI_RXP7	P43	PCH_FDI_RX_P<7>	9
FDI_INT	H46	PCH_FDI_INT	OUT 9
FDI_FSYNC0	B51	PCH_FDI_FSYNC<0>	OUT 9
FDI_FSYNC1	C52	PCH_FDI_FSYNC<1>	OUT 9
FDI_LSYNC0	E49	PCH_FDI_LSYNC<0>	OUT 9
FDI_LSYNC1	D51	PCH_FDI_LSYNC<1>	OUT 9

=PP3V3_S0_PCH_GPIO 6 15 20 36 — R1998 10K 5% 1/16W MF-LF 402

SYSTEM POWER MANAGEMENT

PM_SYSRST_L	BE52	SYS_RESET*	
PM_PCH_SYS_PWROK	BJ53	SYS_PWROK	
PM_PCH_PWROK	BJ38	PWROK	
PM_MEM_PWRGD	BG46	DRAMPWROK	
	BT37	DPWROK	
PM_PCH_APWROK	BC46	APWROK	
PM_RSMRST_PCH_L	BK38	RSMRST*	
PCH_SUSWARN_L	BU46	SUSWARN*/GPIO30	
PM_PWRBTN_L	BT43	PWRBTN*	
PCH_GPIO31_ACPRESENT	BG43	GPIO31	
PCH_GPIO72	AV46	GPIO72	
PCH_RI_L	BJ48	RI*	
TP_PCH_INIT3V3_L	BN56	INIT3_3V*	

WAKE*	BC44	PCIE_WAKE_L	IN 19 33 38
GPIO32	BC56	PCH_GPIO32	
SUS_STAT*/GPIO61	BN54	LPC_PWRDWN_L	OUT 26 45 47
SUSCLK/GPIO62	BA47	PM_CLK32K_SUSCLK_R	OUT 46 83
SLP_S5*/GPIO63	BH50	PM_SLP_S5_L	OUT 15 33 45 61
SLP_S4*	BN52	PM_SLP_S4_L	OUT 15 45 61
SLP_S3*	BM53	PM_SLP_S3_L	OUT 15 28 38 45 46 61
SLP_A*	BC41	TP_PM_SLP_A_L (KEEPING TP, IF NEED TO USE IT LATER)	
PMSYNCH	F55	PM_SYNC	OUT 11
SLP_LAN*/GPIO29	BH49	PCH_GPIO29	15
DF_TVS	R47	PCH_DF_TVS	19
DSWVRMEN	BR42	PCH_DSWVRMEN	19
SLP_SUS*	BD43	TP_PCH_SLP_SUS_L	
SUSACK*	BP45	TP_PCH_SUSACK_L	

R1900 49.9 1% 1/16W MF-LF 402 — =PP1V05_S0_PCH_VCCIO_PCIE 22 18 6 — PLACE_NEAR=U1800.E31:2mm

R1920 750 1% 1/16W MF-LF 402 — PLACE_NEAR=U1800.A32:2mm

PCH_DMI_COMP: SHORT THESE TWO PINS VERY NEAR THE PINS. PLACE THE RESISTOR VERY CLOSE TO COMMON POINT

R1999 10K 5% 1/16W MF-LF 402 — =PP3V3_S5_PCH 26 24 19 6

R1905 10K 5% 1/16W MF-LF 402

R1909 10K 5% 1/16W MF-LF 402

U1800 PANTHER-POINT (4 OF 10) FCBGA

OMIT TABLE

TP_PCH_RESERVE_0	J57	RESERVED	
TP_PCH_RESERVE_1	U43		
TP_PCH_RESERVE_2	M49		
TP_PCH_RESERVE_3	M50		
TP_PCH_RESERVE_4	R50		
TP_PCH_RESERVE_5	Y41		
TP_PCH_RESERVE_6	H50		
TP_PCH_RESERVE_7	U44		
TP_PCH_RESERVE_8	U46		
TP_PCH_RESERVE_9	U50		
TP_PCH_RESERVE_10	R44		
TP_PCH_RESERVE_11	U49		
TP_PCH_RESERVE_12	AB44		
TP_PCH_RESERVE_13	AB49		
TP_PCH_RESERVE_14	E52		
TP_PCH_RESERVE_15	H52		
TP_PCH_RESERVE_16	F53		
TP_PCH_RESERVE_17	J55		
TP_PCH_RESERVE_18	L56		
TP_PCH_RESERVE_19	K46		
TP_PCH_RESERVE_20	Y50		
TP_PCH_RESERVE_21	AB50		
TP_PCH_RESERVE_22	L53		
TP_PCH_RESERVE_23	Y44		
TP_PCH_RESERVE_24	G56		
TP_PCH_RESERVE_25	AB46		
TP_PCH_RESERVE_26	K49		
TP_PCH_RESERVE_27	K50		
TP_PCH_RESERVE_28	M48		

DIGITAL DISPLAY INTERFACE

CRT

TP_CRT_IG_BLUE	AM1	CRT_BLUE	
TP_CRT_IG_GREEN	AN2	CRT_GREEN	
TP_CRT_IG_RED	AN6	CRT_RED	
TP_CRT_IG_DDC_CLK	AW3	CRT_DDC_CLK	
TP_CRT_IG_DDC_DATA	AW1	CRT_DDC_DATA	
TP_CRT_IG_HSYNC	AR4	CRT_HSYNC	
TP_CRT_IG_VSYNC	AR2	CRT_VSYNC	
PCH_DAC_IREF	AT3	DAC_IREF	
	AM6	CRT_IRTN	

R1951 1K 5% 1/16W MF-LF 402 — PLACE_NEAR=U1800.AT3:3mm — PLACE CLOSE TO U1800 PIN

SDVO_TVCLKINN	U9	TP_SDVO_TVCLKINN	
SDVO_TVCLKINP	U8	TP_SDVO_TVCLKINP	
SDVO_STALLN	U5	TP_SDVO_STALLN	
SDVO_STALLP	W3	TP_SDVO_STALLP	
SDVO_INTN	T3	TP_SDVO_INTN	
SDVO_INTP	U2	TP_SDVO_INTP	
SDVO_CTRLCLK	AL15	DP_IG_B_DDC_CLK	
SDVO_CTRLDATA	AL17	DP_IG_B_DDC_DATA	
DDPB_AUXN	R9	DP_IG_B_AUX_N	
DDPB_AUXP	R8	DP_IG_B_AUX_P	
DDPB_HPD	T1	DP_IG_B_HPD	
DDPB_0N	R12	DP_IG_B_MLN<0>	
DDPB_0P	R14	DP_IG_B_MLP<0>	
DDPB_1N	M12	DP_IG_B_MLN<1>	
DDPB_1P	M11	DP_IG_B_MLP<1>	
DDPB_2N	K8	DP_IG_B_MLN<2>	
DDPB_2P	H8	DP_IG_B_MLP<2>	
DDPB_3N	M3	DP_IG_B_MLN<3>	
DDPB_3P	L5	DP_IG_B_MLP<3>	
DDPC_CTRLCLK	AL12	DP_IG_C_CTRL_CLK	
DDPC_CTRLDATA	AL14	DP_IG_C_CTRL_DATA	
DDPC_AUXN	U12	DP_IG_C_AUX_N	
DDPC_AUXP	U14	DP_IG_C_AUX_P	
DDPC_HPD	N2	DP_IG_C_HPD	
DDPC_0N	J3	DP_IG_C_MLN<0>	
DDPC_0P	L2	DP_IG_C_MLP<0>	
DDPC_1N	G4	DP_IG_C_MLN<1>	
DDPC_1P	G2	DP_IG_C_MLP<1>	
DDPC_2N	F5	DP_IG_C_MLN<2>	
DDPC_2P	F3	DP_IG_C_MLP<2>	
DDPC_3N	E2	DP_IG_C_MLN<3>	
DDPC_3P	E4	DP_IG_C_MLP<3>	
DDPD_CTRLCLK	AL9	DP_IG_D_CTRL_CLK	
DDPD_CTRLDATA	AL8	DP_IG_D_CTRL_DATA	
DDPD_AUXN	R6	DP_IG_D_AUXN	
DDPD_AUXP	N6	DP_IG_D_AUXP	
DDPD_HPD	M1	DP_IG_D_HPD	
DDPD_0N	B5	DP_IG_D_MLN<0>	
DDPD_0P	D5	DP_IG_D_MLP<0>	
DDPD_1N	D7	DP_IG_D_MLN<1>	
DDPD_1P	C6	DP_IG_D_MLP<1>	
DDPD_2N	C9	DP_IG_D_MLN<2>	
DDPD_2P	B7	DP_IG_D_MLP<2>	
DDPD_3N	B11	DP_IG_D_MLN<3>	
DDPD_3P	E11	DP_IG_D_MLP<3>	

R1915 390K 5% 1/16W MF-LF 402 — =PP3V3_G3_PCH 6 18 — PCH_DSWVRMEN 19

R1925 1K 1% 1/16W MF-LF 402 — =PP3V3_S5_PCH 6 19 24 26 — 38 33 19 PCIE_WAKE_L — MAKE_BASE=TRUE — =TBT_WAKE_L 34

R1981 2.2K 5% 1/16W MF-LF 402 — =PP1V8_S0_PCH 6

R1980 4.7K 5% 1/16W MF-LF 402 — 19 PCH_DF_TVS — CPU_PROC_SEL 11

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE: PCH DMI/FDI/GRAPHICS

Apple Inc.

DRAWING NUMBER: 051-9179 SIZE: D

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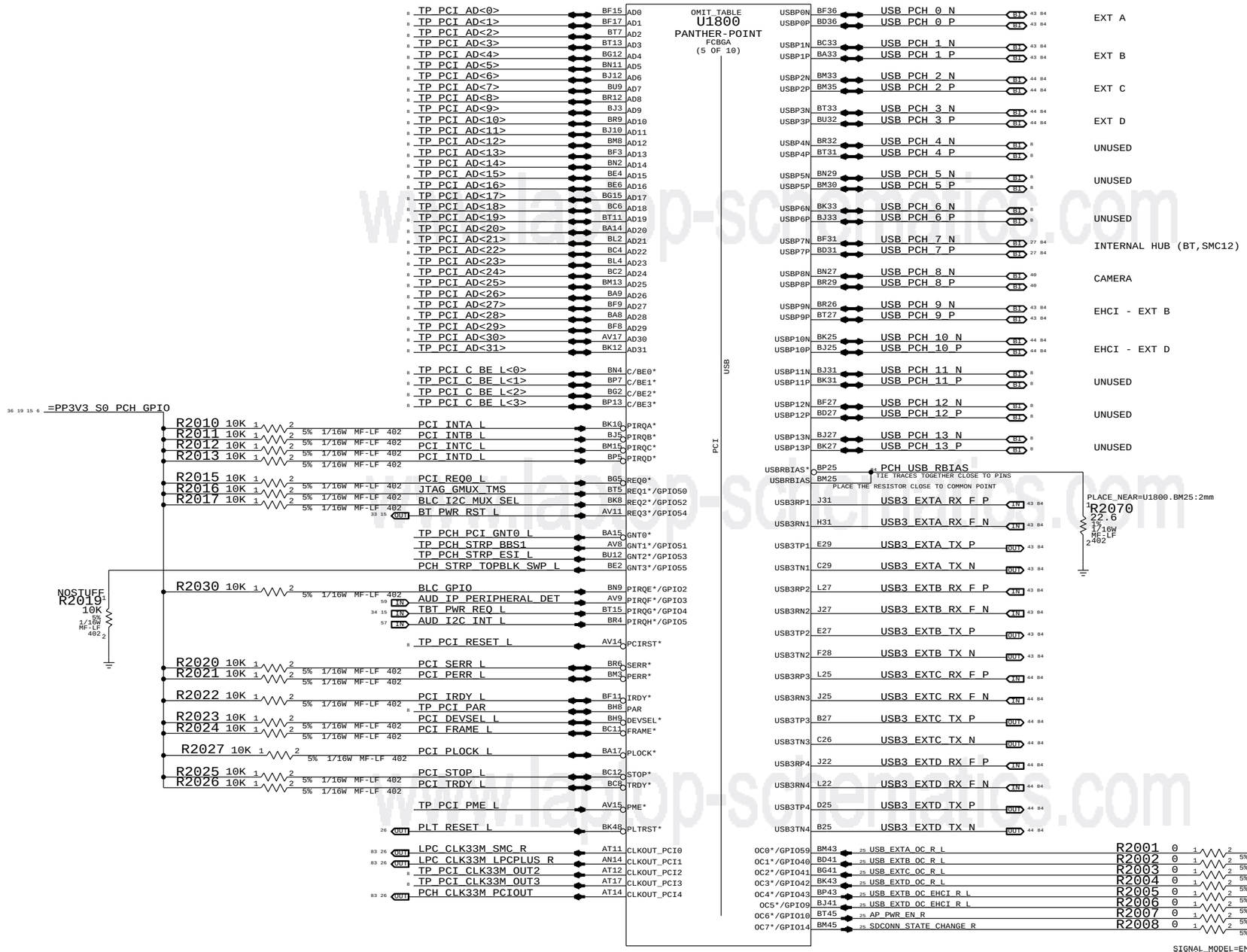

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE

PCH PCI/USB

Apple Inc.

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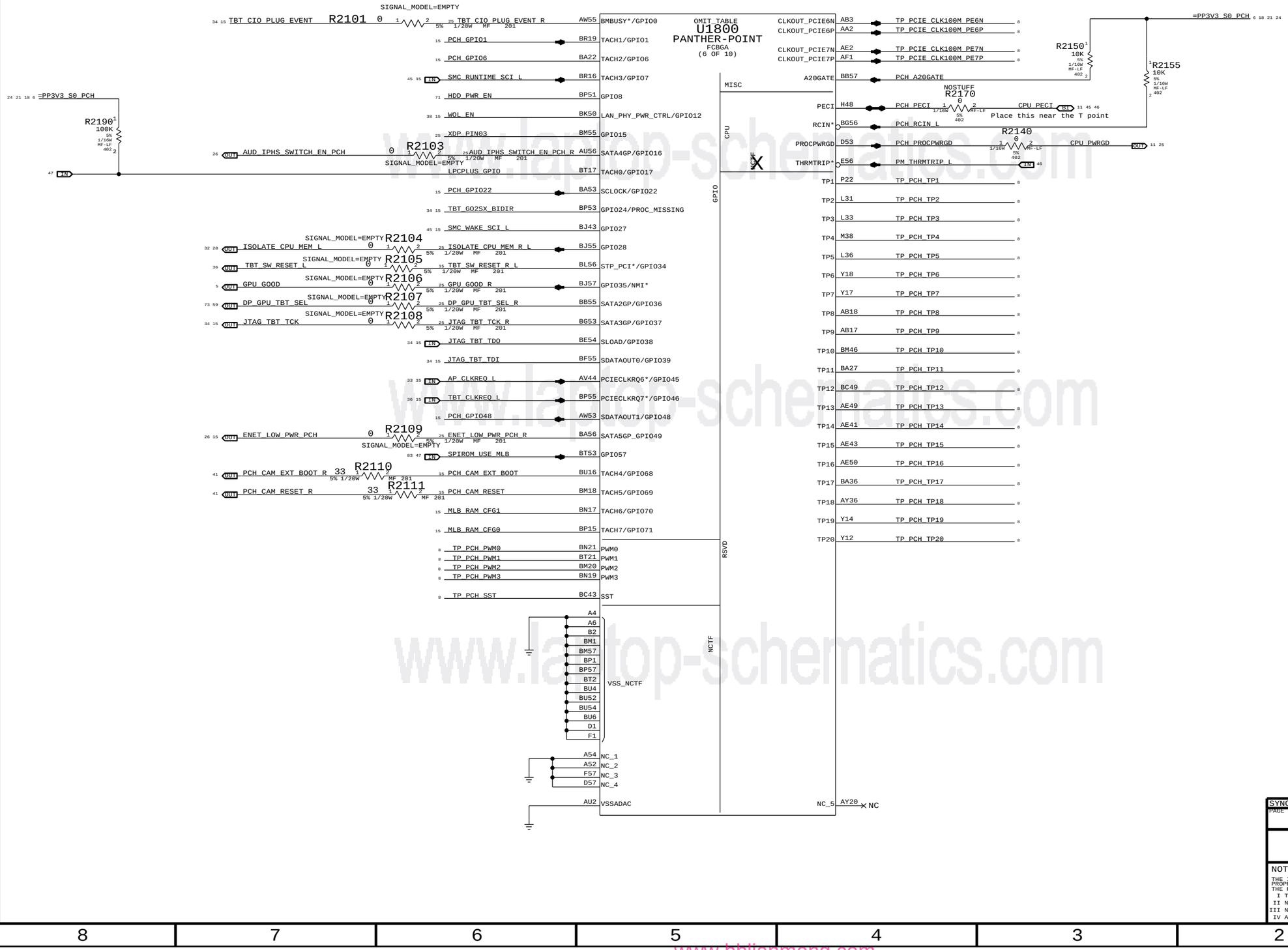

SYNC_MASTER=D7_MLB	SYNC_DATE=01/19/2012
PAGE TITLE	PCH MISC
Apple Inc.	DRAWING NUMBER 051-9179 SIZE D
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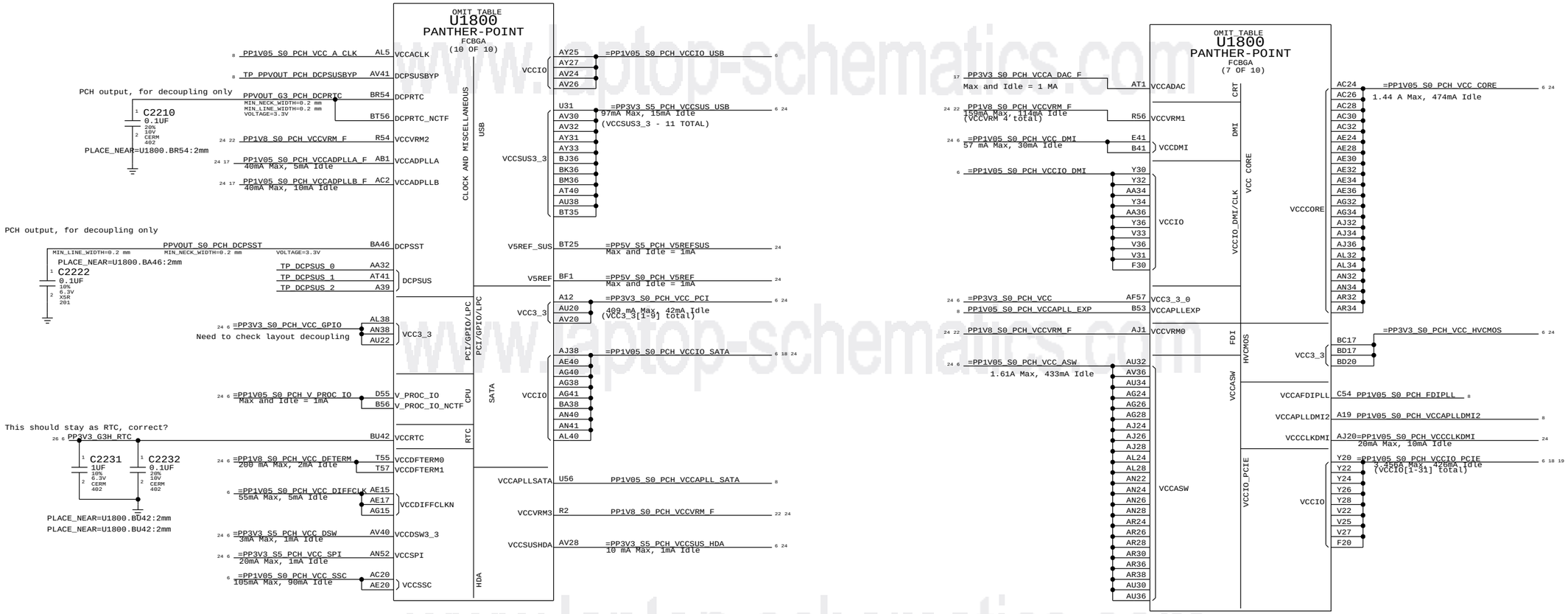

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE

PCH POWER

Apple Inc.

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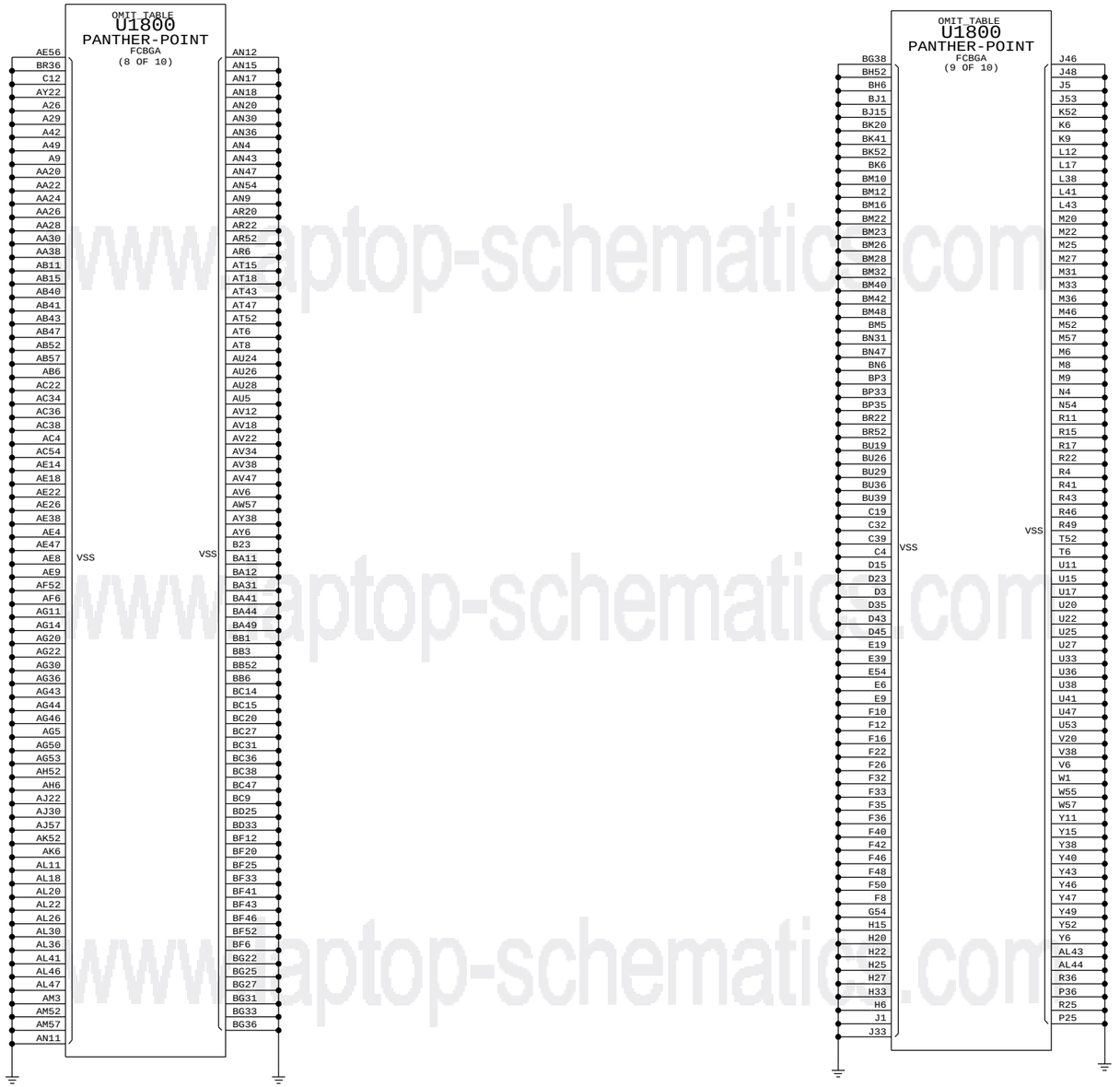

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE

PCH GROUNDS

Apple Inc.

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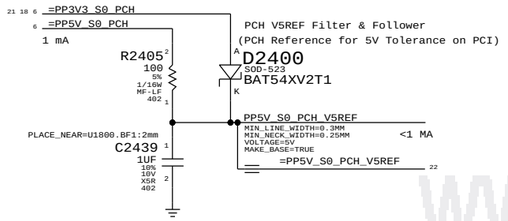
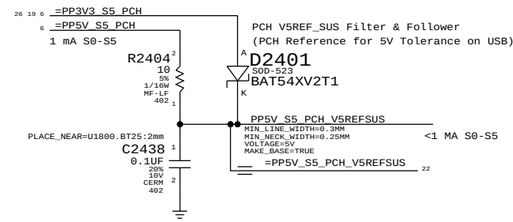
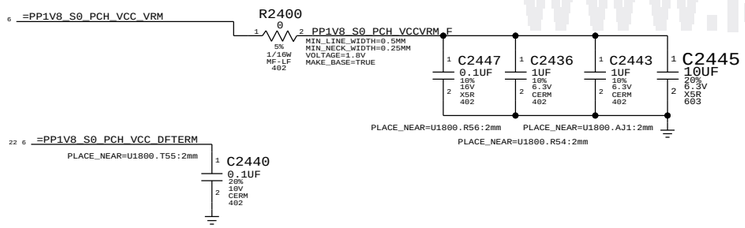
Power Sequencing

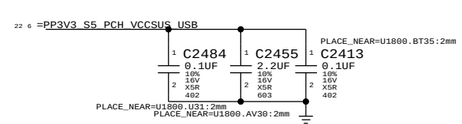


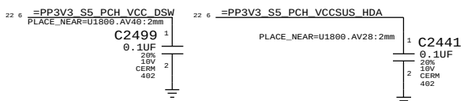


1V8 S0 Rails

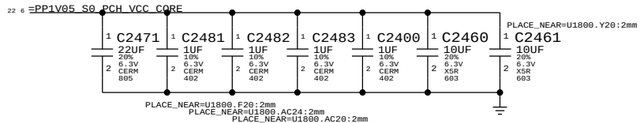


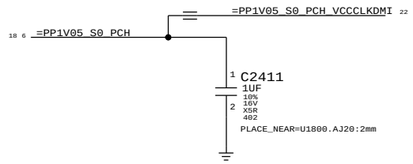
3V3 S5 Rails

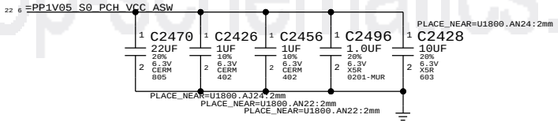


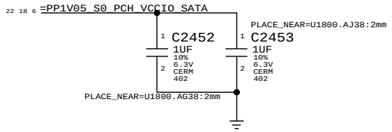


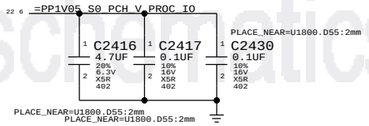
1V05 S0 Rails

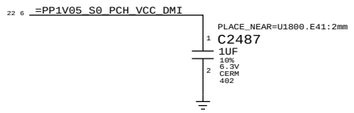




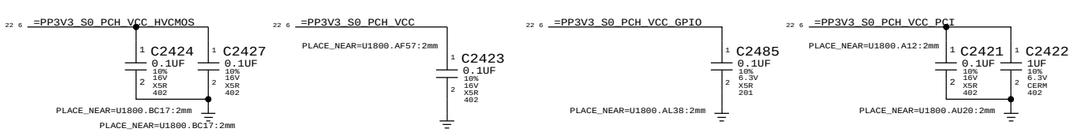








3V3 S0 Rails



SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE: PCH DECOUPLING

Apple Inc.

DRAWING NUMBER: 051-9179 SIZE: D

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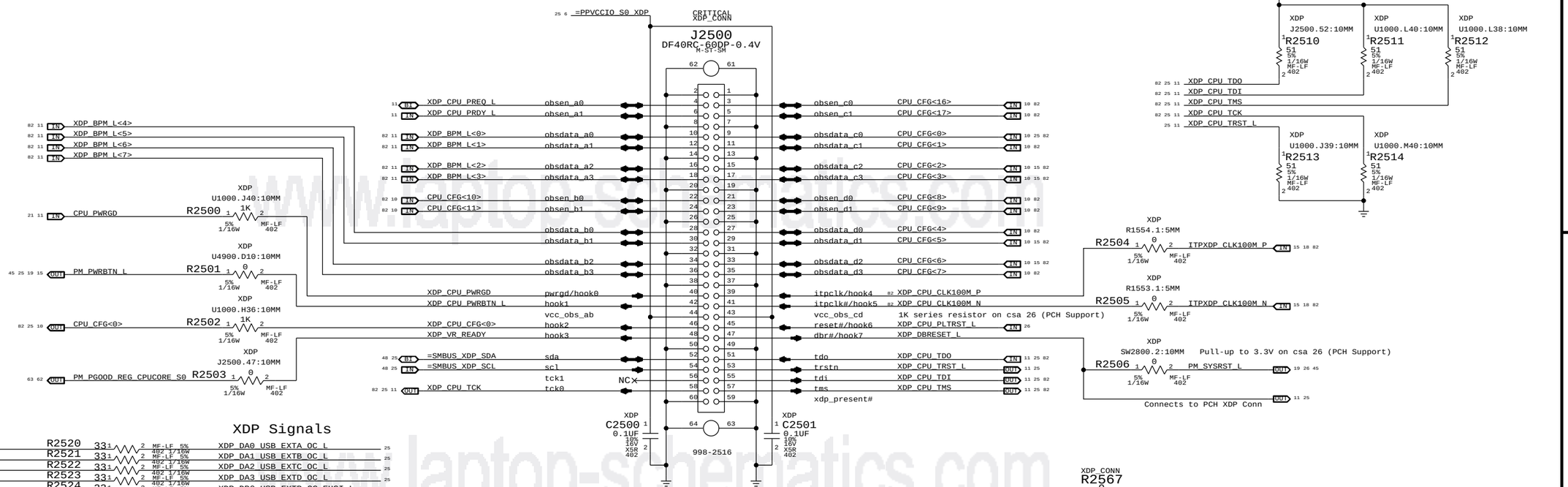
CPU Micro2-XDP

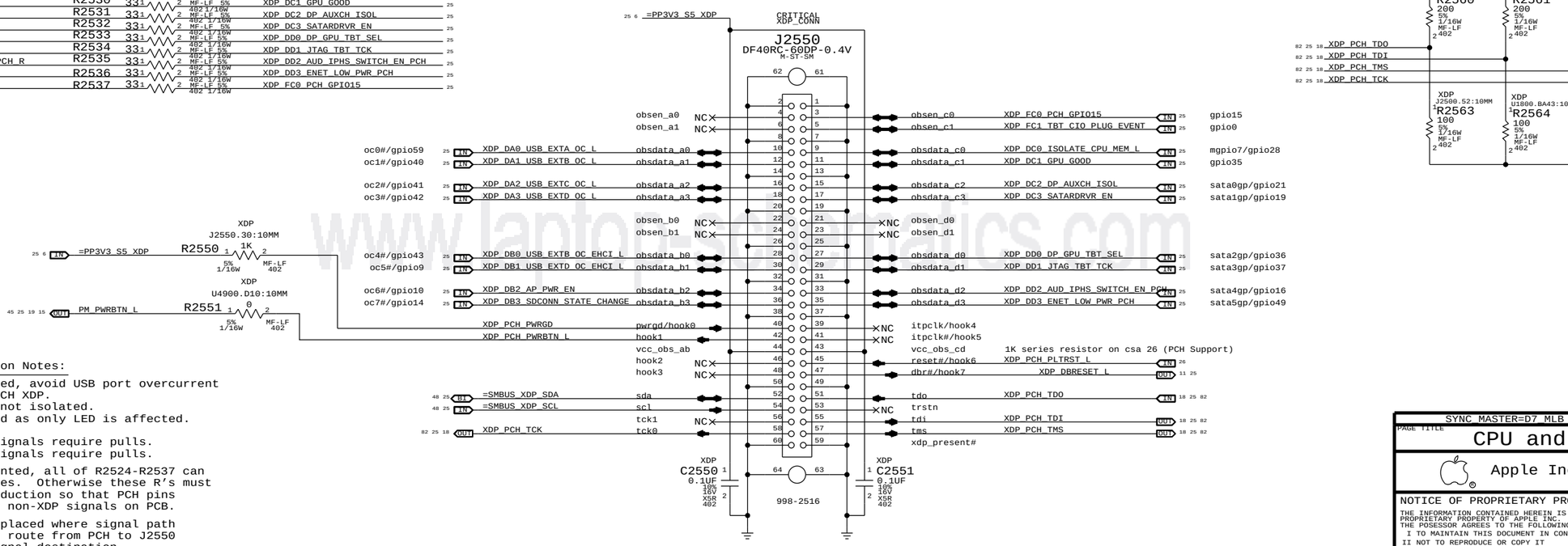


PCH Signals

USB_EXTA_OC_R_L	R2520	33	XDP_DA0_USB_EXTA_OC_L
USB_EXTB_OC_R_L	R2521	33	XDP_DA1_USB_EXTB_OC_L
USB_EXTC_OC_R_L	R2522	33	XDP_DA2_USB_EXTC_OC_L
USB_EXTD_OC_R_L	R2523	33	XDP_DA3_USB_EXTD_OC_L
USB_EXTB_OC_EHCI_R_L	R2524	33	XDP_DB0_USB_EXTB_OC_EHCI_L
USB_EXTD_OC_EHCI_R_L	R2525	33	XDP_DB1_USB_EXTD_OC_EHCI_L
AP_PWR_EN_R	R2526	33	XDP_DB2_AP_PWR_EN
SDCONN_STATE_CHANGE_R	R2527	33	XDP_DB3_SDCONN_STATE_CHANGE
TBT_CIO_PLUG_EVENT_R	R2528	33	XDP_FC1_TBT_CIO_PLUG_EVENT
ISOLATE_CPU_MEM_R_L	R2529	33	XDP_DC0_ISOLATE_CPU_MEM_L
GPU_GOOD_R	R2530	33	XDP_DC1_GPU_GOOD
DP_AUXCH_ISOL_R	R2531	33	XDP_DC2_DP_AUXCH_ISOL
SATARDRVR_EN_R	R2532	33	XDP_DC3_SATARDRVR_EN
DP_GPU_TBT_SEL_R	R2533	33	XDP_DD0_DP_GPU_TBT_SEL
JTAG_TBT_TCK_R	R2534	33	XDP_DD1_JTAG_TBT_TCK
AUD_IPHS_SWITCH_EN_PCH_R	R2535	33	XDP_DD2_AUD_IPHS_SWITCH_EN_PCH
ENET_LOW_PWR_PCH_R	R2536	33	XDP_DD3_ENET_LOW_PWR_PCH
XDP_PIN03	R2537	33	XDP_FC0_PCH_GPIO15

XDP Signals

PCH Micro2-XDP



PCH/XDP Signal Isolation Notes:

- USB OC#'s not isolated, avoid USB port overcurrent events while using PCH XDP.
- Unused GPIOs 0 & 15 not isolated.
- MXM_GOOD not isolated as only LED is affected.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

If PCH XDP not implemented, all of R2524-R2537 can be replaced with aliases. Otherwise these R's must be stuffed even in production so that PCH pins connect to appropriate non-XDP signals on PCB.

R2524-R2537 should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

SYNC_MASTER=D7 MLB SYNC_DATE=01/19/2012

PAGE TITLE: CPU and PCH XDP

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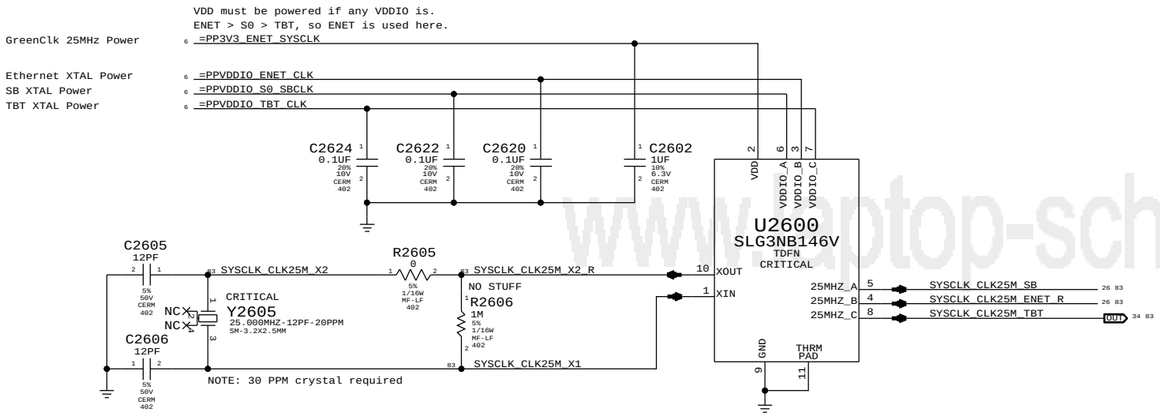
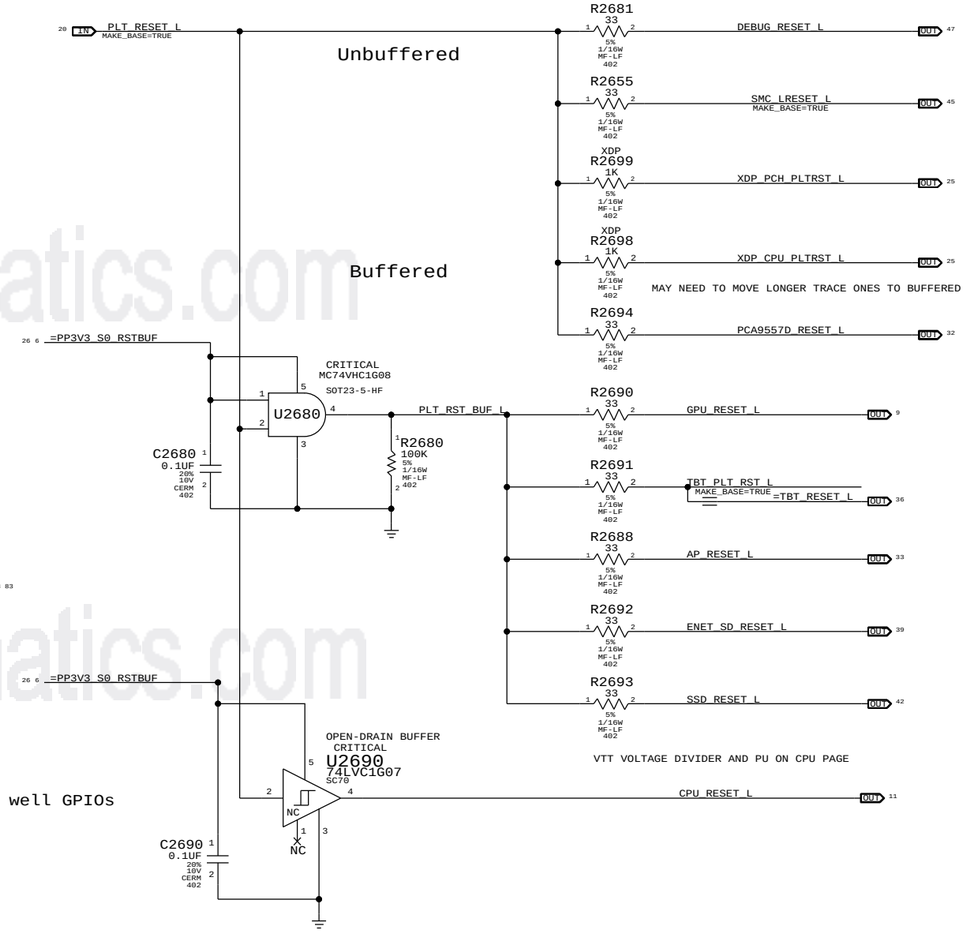
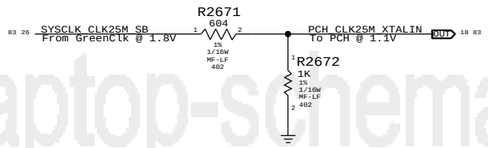
System 25MHz Clock Generator



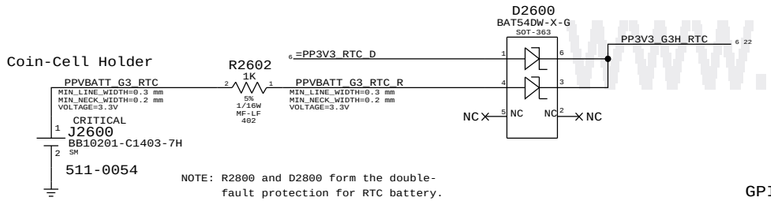
Platform Reset Connections



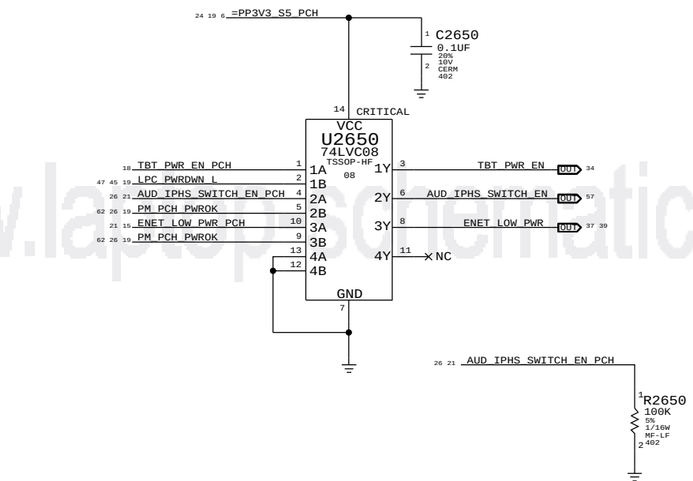
PCH 25MHZ CLOCK



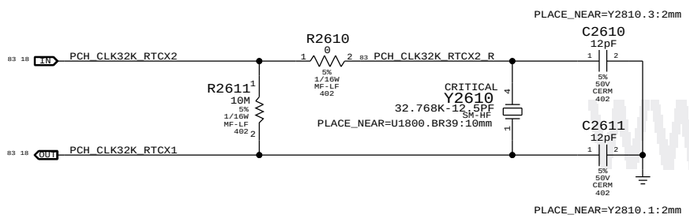
RTC Power Sources



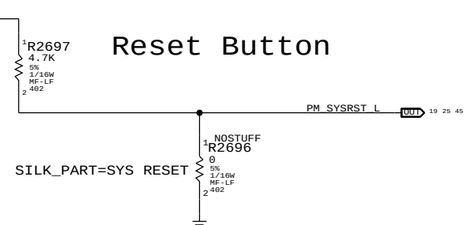
GPIO Isolation to prevent glitches on critical core well GPIOs



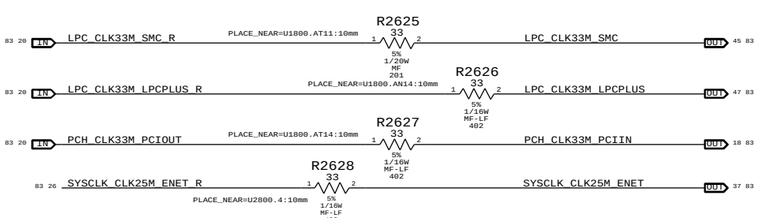
PCH RTC Crystal



Reset Button



Clock series termination



SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE: CHIPSET SUPPORT

Apple Inc.

DRAWING NUMBER: 051-9179 SIZE: D
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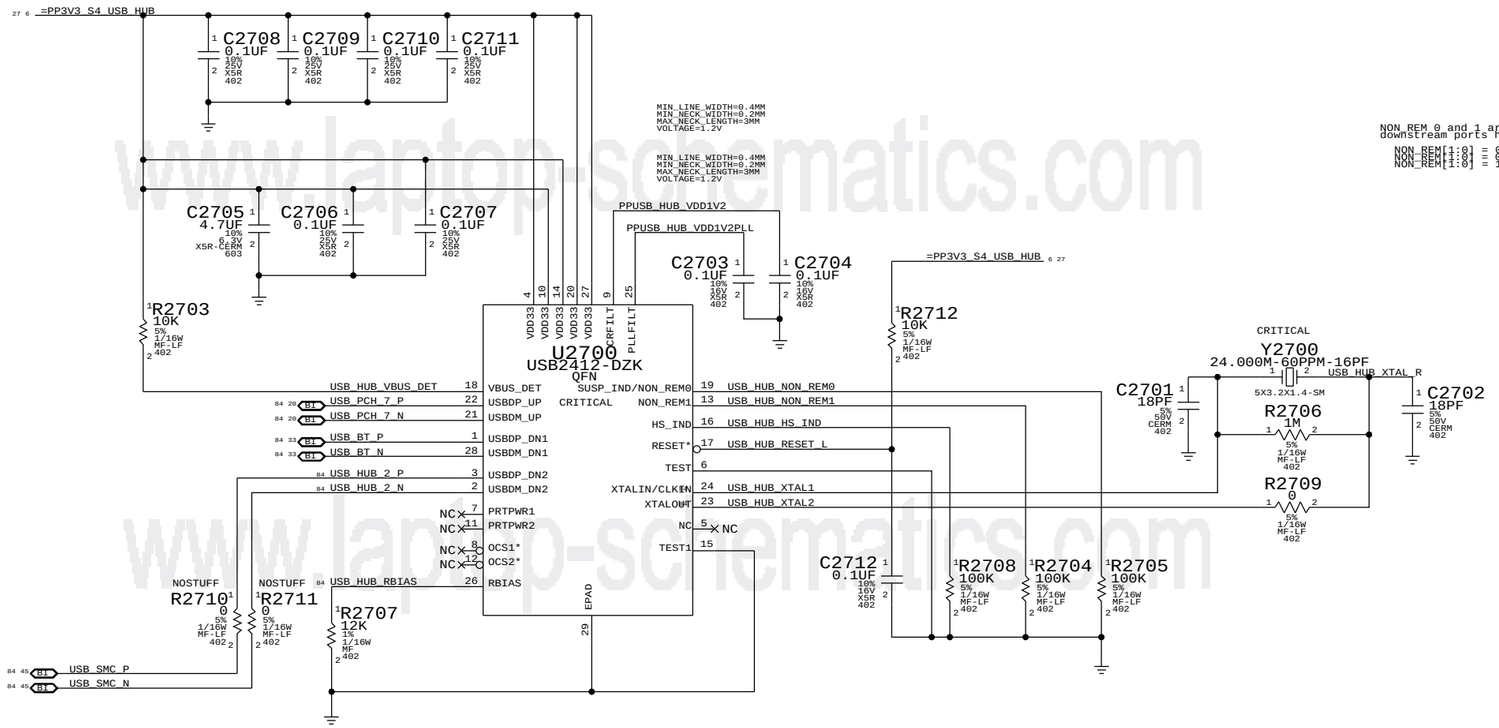

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

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USB HUB

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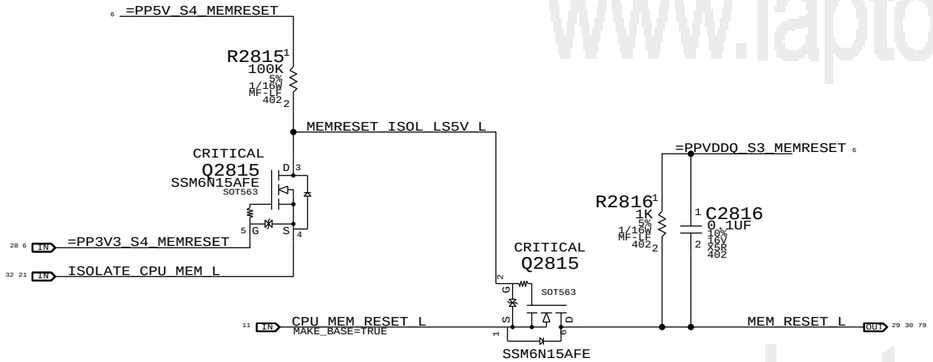
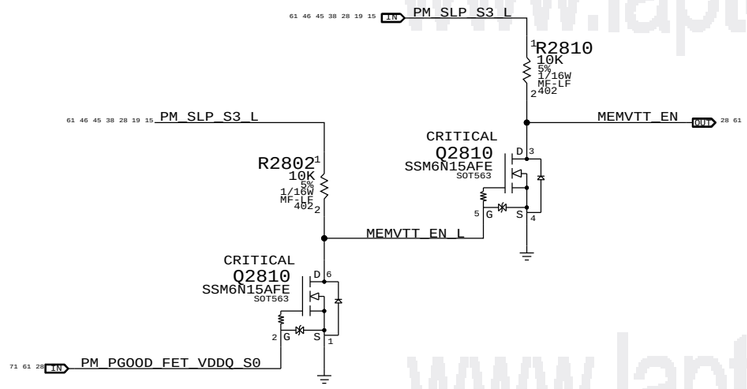
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

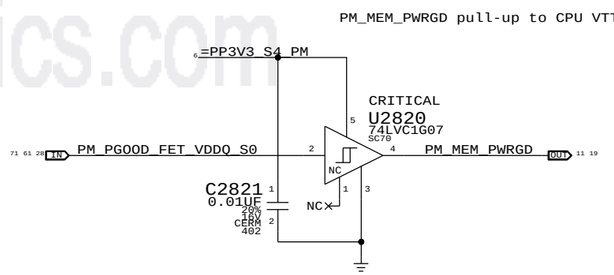
MEMVTT_EN = PM_PGOOD_FET_VDDQ_S0 * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L





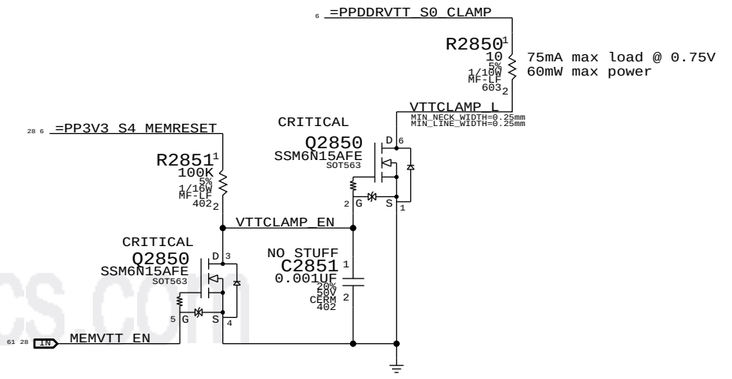
1V5 S0 "PGOOD" for CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1
to	1	0	1	1	1	1	1
S3	2	0	0	1	1	1	0
	3	0	0	0	X	1	0
	4	0	0	1	X	1	0
to	5	0	1	1	0 (*)	1	1
S0	6	0	1	1	1	1	1
	7	1	1	1	1	CPU_MEM_RESET_L	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must de-assert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

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CPU Memory S3 Support

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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPDDRVREF_DQ_MEM_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

J2900 CRITICAL F-RT-SM 2013311

1	VREFDQ	VSS_0	2
3	VSS_1	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS_2	8
9	VSS_3	DQS0*	10
11	DM0	DQS0	12
13	VSS_4	VSS_5	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS_6	VSS_7	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS_8	VSS_9	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS_10	VSS_11	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS_12	VSS_13	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS_14	VSS_15	44
45	DQS2*	DM2	46
47	DQS2	VSS_16	48
49	VSS_17	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS_18	54
55	VSS_19	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS_20	60
61	VSS_21	DQS3*	62
63	DM3	DQS3	64
65	VSS_22	VSS_23	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS_24	VSS_25	72
	KEY		
73	CKE0	CKE1	74
75	VDD_0	VDD_1	76
77	NC_0	A15	78
79	BA2	A14	80
81	VDD_2	VDD_3	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD_4	VDD_5	88
89	A8	A6	90
91	A5	A4	92
93	VDD_6	VDD_7	94
95	A3	A2	96
97	A1	A0	98
99	VDD_8	VDD_9	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD_10	VDD_11	106
107	A10_AP	BA1	108
109	BA0	RAS*	110
111	VDD_12	VDD_13	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD_14	VDD_15	118
119	A13	ODT1	120
121	S1*	NC_1	122
123	VDD_16	VDD_17	124
125	TEST	VREFCA	126
127	VSS_26	VSS_27	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS_28	VSS_29	134
135	DQS4*	DM4	136
137	DQS4	VSS_30	138
139	VSS_31	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS_32	144
145	VSS_33	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS_34	150
151	VSS_35	DQS5*	152
153	DM5	DQS5	154
155	VSS_36	VSS_37	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS_38	VSS_39	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS_40	VSS_41	168
169	DQS6*	DM6	170
171	DQS6	VSS_42	172
173	VSS_43	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS_44	178
179	VSS_45	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS_46	184
185	VSS_47	DQS7*	186
187	DM7	DQS7	188
189	VSS_48	VSS_49	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS_50	VSS_51	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT_0	VTT_1	204
205	MTG_PIN	MTG_PIN	206

NC
NC

=MEM_A_DQ<0>
=MEM_A_DQ<1>
=MEM_A_DQ<2>
=MEM_A_DQ<3>
=MEM_A_DQ<8>
=MEM_A_DQ<9>
=MEM_A_DQS_N<1>
=MEM_A_DQS_P<1>
=MEM_A_DQ<10>
=MEM_A_DQ<11>
=MEM_A_DQ<16>
=MEM_A_DQ<17>
=MEM_A_DQS_N<2>
=MEM_A_DQS_P<2>
=MEM_A_DQ<18>
=MEM_A_DQ<19>
=MEM_A_DQ<24>
=MEM_A_DQ<25>
=MEM_A_DQ<26>
=MEM_A_DQ<27>
=MEM_A_DQ<32>
=MEM_A_DQ<33>
=MEM_A_DQS_N<4>
=MEM_A_DQS_P<4>
=MEM_A_DQ<34>
=MEM_A_DQ<35>
=MEM_A_DQ<40>
=MEM_A_DQ<41>
=MEM_A_DQ<42>
=MEM_A_DQ<43>
=MEM_A_DQ<48>
=MEM_A_DQ<49>
=MEM_A_DQS_N<6>
=MEM_A_DQS_P<6>
=MEM_A_DQ<50>
=MEM_A_DQ<51>
=MEM_A_DQ<56>
=MEM_A_DQ<57>
=MEM_A_DQ<58>
=MEM_A_DQ<59>
=MEM_A_DQ<4>
=MEM_A_DQ<5>
=MEM_A_DQS_N<0>
=MEM_A_DQS_P<0>
=MEM_A_DQ<6>
=MEM_A_DQ<7>
=MEM_A_DQ<12>
=MEM_A_DQ<13>
MEM_RESET_L
=MEM_A_DQ<14>
=MEM_A_DQ<15>
=MEM_A_DQ<20>
=MEM_A_DQ<21>
=MEM_A_DQ<22>
=MEM_A_DQ<23>
=MEM_A_DQ<28>
=MEM_A_DQ<29>
=MEM_A_DQS_N<3>
=MEM_A_DQS_P<3>
=MEM_A_DQ<30>
=MEM_A_DQ<31>
=MEM_A_DQ<36>
=MEM_A_DQ<37>
=MEM_A_DQ<38>
=MEM_A_DQ<39>
=MEM_A_DQ<44>
=MEM_A_DQ<45>
=MEM_A_DQS_N<5>
=MEM_A_DQS_P<5>
=MEM_A_DQ<46>
=MEM_A_DQ<47>
=MEM_A_DQ<52>
=MEM_A_DQ<53>
=MEM_A_DQ<54>
=MEM_A_DQ<55>
=MEM_A_DQ<60>
=MEM_A_DQ<61>
=MEM_A_DQS_N<7>
=MEM_A_DQS_P<7>
=MEM_A_DQ<62>
=MEM_A_DQ<63>
MEM_EVENT_L
=I2C_SODIMMA_SDA
=I2C_SODIMMA_SCL

MEM_A_CKE<0>
MEM_A_CKE<1>
MEM_A_BA<2>
MEM_A_A<12>
MEM_A_A<9>
MEM_A_A<8>
MEM_A_A<5>
MEM_A_A<3>
MEM_A_A<1>
MEM_A_CLK_P<0>
MEM_A_CLK_N<0>
MEM_A_A<10>
MEM_A_BA<0>
MEM_A_WE_L
MEM_A_CAS_L
MEM_A_A<13>
MEM_A_CS_L<1>
MEM_A_A<15>
MEM_A_A<14>
MEM_A_A<11>
MEM_A_A<7>
MEM_A_A<6>
MEM_A_A<4>
MEM_A_A<2>
MEM_A_A<0>
MEM_A_CLK_P<1>
MEM_A_CLK_N<1>
MEM_A_BA<1>
MEM_A_RAS_L
MEM_A_CS_L<0>
MEM_A_ODT<0>
MEM_A_ODT<1>
MEM_A_SA<0>
MEM_A_SA<1>

=PPVDDQ_S3_MEM_A

C2910 0.1UF 20% 10V CERM 402
C2911 0.1UF 20% 10V CERM 402
C2912 0.1UF 20% 10V CERM 402
C2913 0.1UF 20% 10V CERM 402
C2914 0.1UF 20% 10V CERM 402
C2915 0.1UF 20% 10V CERM 402
C2916 0.1UF 20% 10V CERM 402
C2917 0.1UF 20% 10V CERM 402
C2902 0.1UF 20% 10V CERM 402

C2900 10UF 20% 6.3V X5R 603
C2901 10UF 20% 6.3V X5R 603
C2918 0.1UF 20% 10V CERM 402
C2919 0.1UF 20% 10V CERM 402
C2920 0.1UF 20% 10V CERM 402
C2921 0.1UF 20% 10V CERM 402
C2922 0.1UF 20% 10V CERM 402
C2923 0.1UF 20% 10V CERM 402
C2924 0.1UF 20% 10V CERM 402

=PPSPD_S0_MEM_A

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

=PPDDRVTT_S0_MEM_A

=PPDDRVREF_CA_MEM_A

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

C2950 1UF 10% 10V X5R 402
C2951 1UF 10% 10V X5R 402
C2952 1UF 10% 10V X5R 402
C2953 1UF 10% 10V X5R 402

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE: DDR3 SO-DIMM Connector A

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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPDDRVREF_DQ_MEM_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 CRITICAL F-RT-SM 2013290

1	VREFDQ		2	VSS_0			
3	VSS_1		4	DQ4	=MEM_B_DQ<4>	B1	31
5	DQ0	=MEM_B_DQ<0> B1 31	6	DQ5	=MEM_B_DQ<5>	B1	31
7	DQ1	=MEM_B_DQ<1> B1 31	8	VSS_2			
9	VSS_3		10	DQS0*	=MEM_B_DQS_N<0>	B1	31
11	DM0		12	DQS0	=MEM_B_DQS_P<0>	B1	31
13	VSS_4		14	VSS_5			
15	DQ2	=MEM_B_DQ<2> B1 31	16	DQ6	=MEM_B_DQ<6>	B1	31
17	DQ3	=MEM_B_DQ<3> B1 31	18	DQ7	=MEM_B_DQ<7>	B1	31
19	VSS_6		20	VSS_7			
21	DQ8	=MEM_B_DQ<8> B1 31	22	DQ12	=MEM_B_DQ<12>	B1	31
23	DQ9	=MEM_B_DQ<9> B1 31	24	DQ13	=MEM_B_DQ<13>	B1	31
25	VSS_8		26	VSS_9			
27	DQS1*	=MEM_B_DQS_N<1> B1 31	28	DM1			
29	DQS1	=MEM_B_DQS_P<1> B1 31	30	RESET*	MEM_RESET_L IN 28 29 79		
31	VSS_10		32	VSS_11			
33	DQ10	=MEM_B_DQ<10> B1 31	34	DQ14	=MEM_B_DQ<14>	B1	31
35	DQ11	=MEM_B_DQ<11> B1 31	36	DQ15	=MEM_B_DQ<15>	B1	31
37	VSS_12		38	VSS_13			
39	DQ16	=MEM_B_DQ<16> B1 31	40	DQ20	=MEM_B_DQ<20>	B1	31
41	DQ17	=MEM_B_DQ<17> B1 31	42	DQ21	=MEM_B_DQ<21>	B1	31
43	VSS_14		44	VSS_15			
45	DQS2*	=MEM_B_DQS_N<2> B1 31	46	DM2			
47	DQS2	=MEM_B_DQS_P<2> B1 31	48	VSS_16			
49	VSS_17		50	DQ22	=MEM_B_DQ<22>	B1	31
51	DQ18	=MEM_B_DQ<18> B1 31	52	DQ23	=MEM_B_DQ<23>	B1	31
53	DQ19	=MEM_B_DQ<19> B1 31	54	VSS_18			
55	VSS_19		56	DQ28	=MEM_B_DQ<28>	B1	31
57	DQ24	=MEM_B_DQ<24> B1 31	58	DQ29	=MEM_B_DQ<29>	B1	31
59	DQ25	=MEM_B_DQ<25> B1 31	60	VSS_20			
61	VSS_21		62	DQS3*	=MEM_B_DQS_N<3>	B1	31
63	DM3		64	DQS3	=MEM_B_DQS_P<3>	B1	31
65	VSS_22		66	VSS_23			
67	DQ26	=MEM_B_DQ<26> B1 31	68	DQ30	=MEM_B_DQ<30>	B1	31
69	DQ27	=MEM_B_DQ<27> B1 31	70	DQ31	=MEM_B_DQ<31>	B1	31
71	VSS_24		72	VSS_25			
	KEY						
73	CKE0	MEM_B_CKE<0> IN 79 12	74	CKE1	MEM_B_CKE<1>	IN	12 79
75	VDD_0		76	VDD_1			
77	NC_0	NC	78	A15	MEM_B_A<15>	IN	12 79
79	BA2	MEM_B_BA<2> IN 79 12	80	A14	MEM_B_A<14>	IN	12 79
81	VDD_2		82	VDD_3			
83	A12/BC*	MEM_B_A<12> IN 79 12	84	A11	MEM_B_A<11>	IN	12 79
85	A9	MEM_B_A<9> IN 79 12	86	A7	MEM_B_A<7>	IN	12 79
87	VDD_4		88	VDD_5			
89	A8	MEM_B_A<8> IN 79 12	90	A6	MEM_B_A<6>	IN	12 79
91	A5	MEM_B_A<5> IN 79 12	92	A4	MEM_B_A<4>	IN	12 79
93	VDD_6		94	VDD_7			
95	A3	MEM_B_A<3> IN 79 12	96	A2	MEM_B_A<2>	IN	12 79
97	A1	MEM_B_A<1> IN 79 12	98	A0	MEM_B_A<0>	IN	12 79
99	VDD_8		100	VDD_9			
101	CK0	MEM_B_CLK_P<0> IN 79 12	102	CK1	MEM_B_CLK_P<1>	IN	12 79
103	CK0*	MEM_B_CLK_N<0> IN 79 12	104	CK1*	MEM_B_CLK_N<1>	IN	12 79
105	VDD_10		106	VDD_11			
107	A10_AP	MEM_B_A<10> IN 79 12	108	BA1	MEM_B_BA<1>	IN	12 79
109	BA0	MEM_B_BA<0> IN 79 12	110	RAS*	MEM_B_RAS_L	IN	12 79
111	VDD_12		112	VDD_13			
113	WE*	MEM_B_WE_L IN 79 12	114	S0*	MEM_B_CS_L<0>	IN	12 79
115	CAS*	MEM_B_CAS_L IN 79 12	116	ODT0	MEM_B_ODT<0>	IN	12 79
117	VDD_14		118	VDD_15			
119	A13	MEM_B_A<13> IN 79 12	120	ODT1	MEM_B_ODT<1>	IN	12 79
121	S1*	MEM_B_CS_L<1> IN 79 12	122	NC_1	NC		
123	VDD_16		124	VDD_17			
125	TEST	NC	126	VREFCA	=PPDDRVREF_CA_MEM_B 6		
127	VSS_26		128	VSS_27			
129	DQ32	=MEM_B_DQ<32> B1 31	130	DQ36	=MEM_B_DQ<36>	B1	31
131	DQ33	=MEM_B_DQ<33> B1 31	132	DQ37	=MEM_B_DQ<37>	B1	31
133	VSS_28		134	VSS_29			
135	DQS4*	=MEM_B_DQS_N<4> B1 31	136	DM4			
137	DQS4	=MEM_B_DQS_P<4> B1 31	138	VSS_30			
139	VSS_31		140	DQ38	=MEM_B_DQ<38>	B1	31
141	DQ34	=MEM_B_DQ<34> B1 31	142	DQ39	=MEM_B_DQ<39>	B1	31
143	DQ35	=MEM_B_DQ<35> B1 31	144	VSS_32			
145	VSS_33		146	DQ44	=MEM_B_DQ<44>	B1	31
147	DQ40	=MEM_B_DQ<40> B1 31	148	DQ45	=MEM_B_DQ<45>	B1	31
149	DQ41	=MEM_B_DQ<41> B1 31	150	VSS_34			
151	VSS_35		152	DQS5*	=MEM_B_DQS_N<5>	B1	31
153	DM5		154	DQS5	=MEM_B_DQS_P<5>	B1	31
155	VSS_36		156	VSS_37			
157	DQ42	=MEM_B_DQ<42> B1 31	158	DQ46	=MEM_B_DQ<46>	B1	31
159	DQ43	=MEM_B_DQ<43> B1 31	160	DQ47	=MEM_B_DQ<47>	B1	31
161	VSS_38		162	VSS_39			
163	DQ48	=MEM_B_DQ<48> B1 31	164	DQ52	=MEM_B_DQ<52>	B1	31
165	DQ49	=MEM_B_DQ<49> B1 31	166	DQ53	=MEM_B_DQ<53>	B1	31
167	VSS_40		168	VSS_41			
169	DQS6*	=MEM_B_DQS_N<6> B1 31	170	DM6			
171	DQS6	=MEM_B_DQS_P<6> B1 31	172	VSS_42			
173	VSS_43		174	DQ54	=MEM_B_DQ<54>	B1	31
175	DQ50	=MEM_B_DQ<50> B1 31	176	DQ55	=MEM_B_DQ<55>	B1	31
177	DQ51	=MEM_B_DQ<51> B1 31	178	VSS_44			
179	VSS_45		180	DQ60	=MEM_B_DQ<60>	B1	31
181	DQ56	=MEM_B_DQ<56> B1 31	182	DQ61	=MEM_B_DQ<61>	B1	31
183	DQ57	=MEM_B_DQ<57> B1 31	184	VSS_46			
185	VSS_47		186	DQS7*	=MEM_B_DQS_N<7>	B1	31
187	DM7		188	DQS7	=MEM_B_DQS_P<7>	B1	31
189	VSS_48		190	VSS_49			
191	DQ58	=MEM_B_DQ<58> B1 31	192	DQ62	=MEM_B_DQ<62>	B1	31
193	DQ59	=MEM_B_DQ<59> B1 31	194	DQ63	=MEM_B_DQ<63>	B1	31
195	VSS_50		196	VSS_51			
197	SA0	MEM_B_SA<0> 30	198	EVENT*	MEM_EVENT_L OUT 29 45 46		
199	VDDSPD	=PPSPD_S0_MEM_B 30 6	200	SDA	=I2C_SODIMMB_SDA	B1	48
201	SA1	MEM_B_SA<1> 30	202	SCL	=I2C_SODIMMB_SCL	IN	48
203	VTT_0		204	VTT_1			
205	MTG_PIN		206	MTG_PIN			

=PPVDDQ_S3_MEM_B 30 6

C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402
C3102 0.1UF 20% 10V CERM 402

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
C3118 0.1UF 20% 10V CERM 402
C3119 0.1UF 20% 10V CERM 402
C3120 0.1UF 20% 10V CERM 402
C3121 0.1UF 20% 10V CERM 402
C3122 0.1UF 20% 10V CERM 402
C3123 0.1UF 20% 10V CERM 402
C3124 0.1UF 20% 10V CERM 402

=PPSPD_S0_MEM_B 30 6

R3141 10K 5% 1/16W MF-LF 402
R3140 10K 5% 1/16W MF-LF 402

=PPSPD_S0_MEM_B 30 6

C3140 2.2UF 20% 6.3V CERM 402-LF

=PPDDRVREF_CA_MEM_B 6

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

=PPDDRVTT_S0_MEM_B 30 6

C3150 1UF 10% 10V X5R 402
C3151 1UF 10% 10V X5R 402
C3152 1UF 10% 10V X5R 402
C3153 1UF 10% 10V X5R 402

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE: DDR3 SO-DIMM CONNECTOR B

Apple Inc.

DRAWING NUMBER: 051-9179 SIZE: D
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8	7	6	5	4	3	2	1

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>	29
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>	29
MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<7>	29
MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<6>	29
MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<5>	29
MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<4>	29
MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<3>	29
MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<2>	29
MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<1>	29
MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<0>	29
MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>	29
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>	29
MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<15>	29
MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<14>	29
MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<13>	29
MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<12>	29
MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<11>	29
MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<10>	29
MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<9>	29
MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<8>	29
MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>	29
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>	29
MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<23>	29
MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<22>	29
MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<21>	29
MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<20>	29
MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<19>	29
MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<18>	29
MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<17>	29
MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<16>	29
MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>	29
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>	29
MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<31>	29
MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<30>	29
MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<29>	29
MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<28>	29
MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<27>	29
MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<26>	29
MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<25>	29
MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<24>	29
MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>	29
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>	29
MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<39>	29
MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<38>	29
MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<37>	29
MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<36>	29
MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<35>	29
MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<34>	29
MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<33>	29
MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<32>	29
MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	29
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	29
MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<47>	29
MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<46>	29
MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	29
MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	29
MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	29
MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	29
MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	29
MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	29
MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>	29
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>	29
MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<55>	29
MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	29
MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	29
MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	29
MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<51>	29
MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	29
MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	29
MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	29
MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	29
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	29
MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	29
MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	29
MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	29
MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	29
MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	29
MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<58>	29
MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	29
MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	29

MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>	30
MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>	30
MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<7>	30
MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<6>	30
MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<5>	30
MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<4>	30
MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<3>	30
MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<2>	30
MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<1>	30
MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<0>	30
MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>	30
MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>	30
MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<15>	30
MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<14>	30
MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<13>	30
MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<12>	30
MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<11>	30
MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<10>	30
MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<9>	30
MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<8>	30
MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>	30
MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>	30
MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<23>	30
MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<22>	30
MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<21>	30
MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<20>	30
MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<19>	30
MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<18>	30
MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<17>	30
MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<16>	30
MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>	30
MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>	30
MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<31>	30
MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<30>	30
MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<29>	30
MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<28>	30
MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<27>	30
MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<26>	30
MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<25>	30
MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<24>	30
MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>	30
MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>	30
MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<39>	30
MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<38>	30
MEM_B_DQ<37>	MAKE_BASE=TRUE	=MEM_B_DQ<37>	30
MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<36>	30
MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<35>	30
MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<34>	30
MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<33>	30
MEM_B_DQ<32>	MAKE_BASE=TRUE	=MEM_B_DQ<32>	30
MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>	30
MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>	30
MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<47>	30
MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<46>	30
MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<45>	30
MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<44>	30
MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<43>	30
MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<42>	30
MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<41>	30
MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<40>	30
MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=MEM_B_DQS_N<6>	30
MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=MEM_B_DQS_P<6>	30
MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<55>	30
MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<54>	30
MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<53>	30
MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<52>	30
MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<51>	30
MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<50>	30
MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<49>	30
MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<48>	30
MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>	30
MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>	30
MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<63>	30
MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<62>	30
MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<61>	30
MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<60>	30
MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<59>	30
MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<58>	30
MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<57>	30
MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<56>	30

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE
DDR3 ALIASES AND BITSWAPS

Apple Inc.

DRAWING NUMBER 051-9179 SIZE D

REVISION 16.0.0

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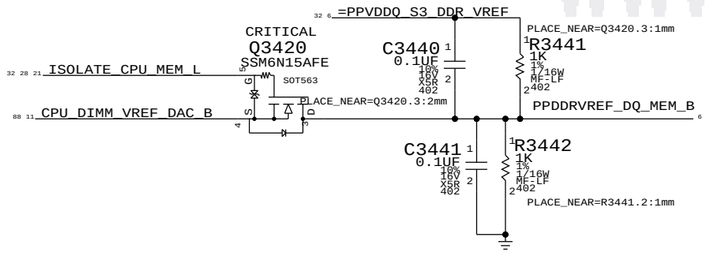
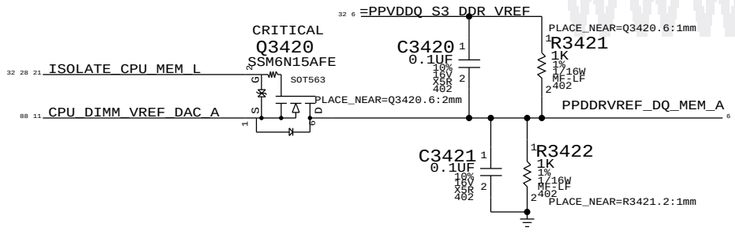
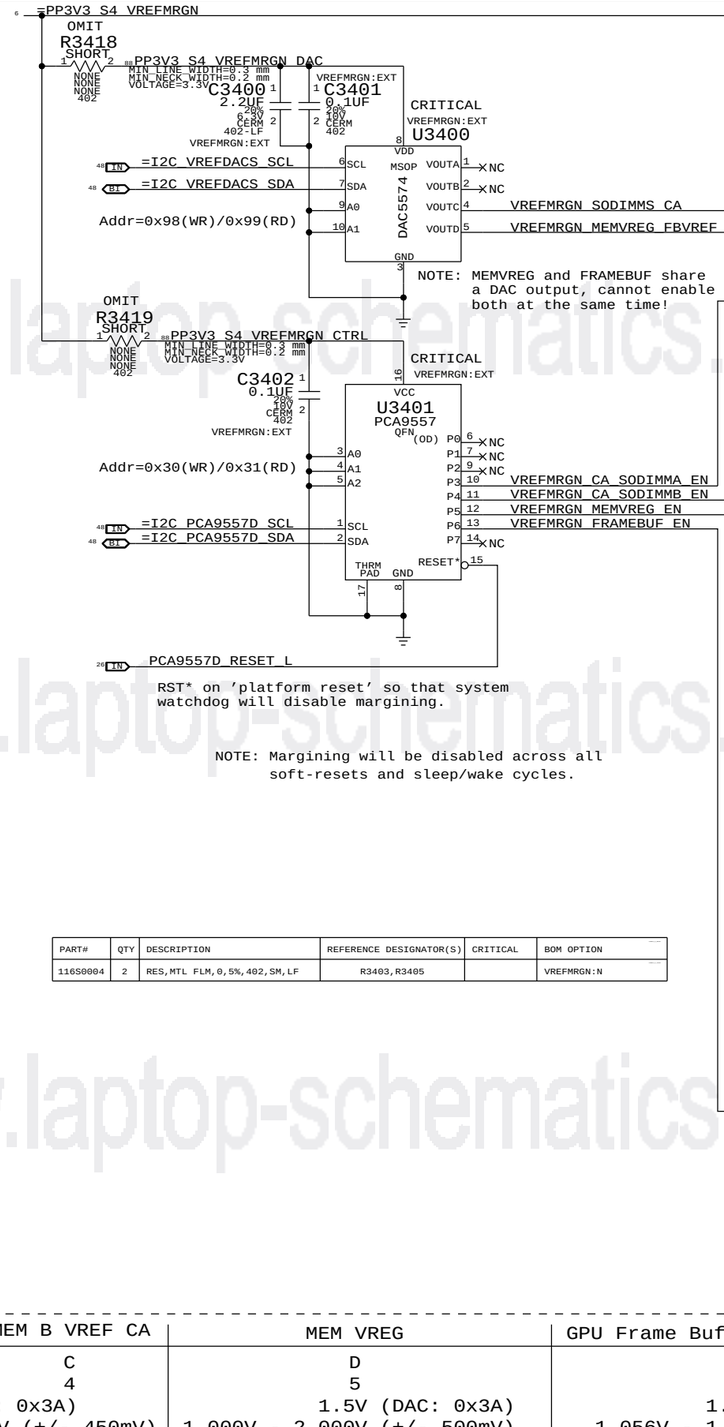
VRef DQ

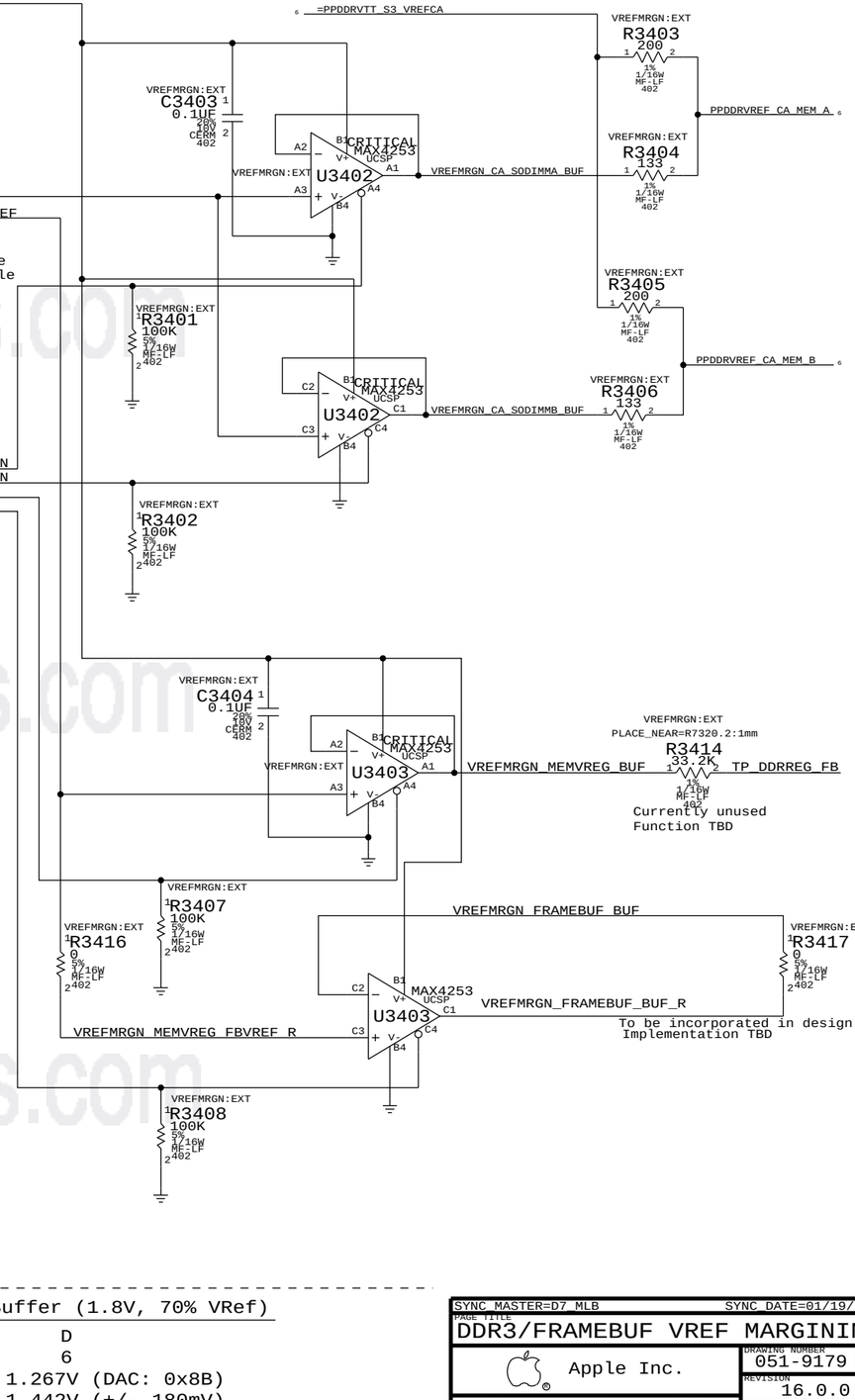
Driven by CPU

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step









PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FLM,0,5%,402,SM,LF	R3403,R3405		VREFMRGN:N

	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	C	C	D	D
PCA9557D Pin:	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)		1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)		1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)		0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)		+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output		8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE
DDR3/FRAMEBUF VREF MARGINING

Apple Inc.

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AIRPORT BLUETOOTH

AP & BT Load Switch

SWITCH	TPS22924B
CHANNEL	N-TYPE
RDS(ON)	18.4 MOHM @3.3V
LOADING	2 A (EDP)

CRITICAL
U3510 TPS22924B CSP
=PP3V3_S4_AP → A2, B2 VIN; VOUT A1, B1 → PP3V3_S4_AP_FET
MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
AP_PWR_EN → C2 ON; GND; C1
L3502 CRITICAL 220-OHM-1.4A 0603 → PP3V3_S4_AP_FLT
C3502 0.1UF 10% 16V X5R 402
C3503 0.1UF 10% 16V X5R 402
C3504 10UF 20% 6.3V X5R 603
MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
C3505 0.1UF 10% X5R 6.3V 201 PLACE_NEAR=J3500.4:3mm
C3506 0.1UF 10% X5R 6.3V 201 PLACE_NEAR=J3500.5:3mm
PCIE_AP_R2D_C_N, PCIE_AP_R2D_C_P
514S0335 CRITICAL
J3500 SSD-K99 F-RT-SM1
AP_EVENT_L
PCIE_AP_R2D_N, PCIE_AP_R2D_P
PCIE_CLK100M_AP_N, PCIE_CLK100M_AP_P
PCIE_AP_D2R_P, PCIE_AP_D2R_N
AP_WAKE_L
AP_RESET_CONN_L
AP_CLKREQ_O_L
USB_BT_MUX_N
USB_BT_MUX_P

CRITICAL
U3540 TPS22924B CSP
=PP3V3_G3H_BT → A2, B2 VIN; VOUT A1, B1 → PP3V3_G3H_BT_FET
VOLTAGE=3.3V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM
SMC_S4_WAKESRC_EN → C2 ON; GND; C1
L3501 CRITICAL 220-OHM-1.4A 0603 → PP3V3_G3H_BT_FLT
VOLTAGE=3.3V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM
C3507 0.1UF 10% 16V X5R 402
C3508 10UF 20% 6.3V X5R 603

CRITICAL
Q3540 SSM6L36FE SOT563 P-CH N-CH
BT_PWR_RST_L → G
=PP3V3_S0_BT → S
D → BT_PWR_RST
R3542 10K 5% 1/16W MF-LF 402
BT_PWR_EN
BT_PWR_RST → G
S → R3543 10K 5% 1/16W MF-LF 402

Wake from BT in G3H circuit

SMC_PME_S4_WAKE_L
CRITICAL Q3501 SSM3K15FV SOD-VESM-HF
R3500 15K 1% 1/20W MF 201
PP3V3_G3H_BT_FET
C3500 0.1UF 20% 16V CERM 402
U3501 USB3740 DFN CRITICAL
USB_BT_N, USB_BT_P
USB_BT_WAKEN, USB_BT_WAKEP
DP → USB_BT_MUX_N
DM → USB_BT_MUX_P
PM_SLP_S5_L → R3502 0 5% 1/16W MF-LF 402 → USB_BT_EN
NOSTUFF C3501 0.1UF 20% 16V CERM 402
R3501 15K 1% 1/20W MF 201
SIGNAL_MODEL=SWI_USB3740_DFN_USB3740_MOJO

Supervisor & CLKFREG # Isolation
Delay = 60 ms +/- 20%

PP3V3_S4_AP_FLT → R3530 100K 1% 1/16W MF-LF 402
R3531 232K 1% 1/16W MF-LF 402
=PP3V3_S4_AP
CRITICAL U3530 SLG4AP016V TDFN
P3V3AP_VMON → SENSE 0.7V
DLY
AP_RESET_CONN_L → RESET* → MR* → AP_RESET_L
AP_CLKREQ_O_L → IN → OUT (60) → AP_PWR_EN, AP_CLKREQ_L
THRM PAD GND
C3530 0.1UF 20% 16V CERM 402
R3532 100K 1% 1/16W MF-LF 402

PP3V3_S4_AP_FLT
CRITICAL Q3570 SSM3K15FV SOD-VESM-HF
R3570 10K 5% 1/16W MF-LF 402
PCIE_WAKE_L → AP_WAKE_L

SYNC_MASTER=D7_MLB	SYNC_DATE=01/19/2012
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PCIE Polarity swapped for D7i layout
R2D<0>
R2D<3>
D2R<1>
D2R<3>

CRITICAL
OMIT_TABLE
U3600
CACTUSRIDGE4C
FCBGA
(SYM 1 OF 2)

PCIE GEN2

RECEIVE

PCIE_TBT_R2D_C_N<0>	C3600 0.1UF	PCIE_TBT_R2D_P<0>	AB9
		PCIE_TBT_R2D_N<0>	AA10
PCIE_TBT_R2D_C_P<0>	C3601 0.1UF		
PCIE_TBT_R2D_C_P<1>	C3602 0.1UF	PCIE_TBT_R2D_P<1>	AA12
		PCIE_TBT_R2D_N<1>	AB13
PCIE_TBT_R2D_C_N<1>	C3603 0.1UF		
PCIE_TBT_R2D_C_P<2>	C3604 0.1UF	PCIE_TBT_R2D_P<2>	AB15
		PCIE_TBT_R2D_N<2>	AA16
PCIE_TBT_R2D_C_N<2>	C3605 0.1UF		
PCIE_TBT_R2D_C_N<3>	C3606 0.1UF	PCIE_TBT_R2D_P<3>	AA18
		PCIE_TBT_R2D_N<3>	AB19
PCIE_TBT_R2D_C_P<3>	C3607 0.1UF		

PERP_0, PERN_0, PERP_1, PERN_1, PERP_2, PERN_2, PERP_3, PERN_3

TRANSMIT

PCIE_TBT_D2R_C_P<0>	C3640 0.1UF	PCIE_TBT_D2R_P<0>	AD5
PCIE_TBT_D2R_C_N<0>	C3641 0.1UF	PCIE_TBT_D2R_N<0>	AD7
PCIE_TBT_D2R_C_P<1>	C3642 0.1UF	PCIE_TBT_D2R_N<1>	AD9
PCIE_TBT_D2R_C_N<1>	C3643 0.1UF	PCIE_TBT_D2R_P<1>	AD11
PCIE_TBT_D2R_C_P<2>	C3644 0.1UF	PCIE_TBT_D2R_P<2>	AD13
PCIE_TBT_D2R_C_N<2>	C3645 0.1UF	PCIE_TBT_D2R_N<2>	AD15
PCIE_TBT_D2R_C_P<3>	C3646 0.1UF	PCIE_TBT_D2R_N<3>	AD17
PCIE_TBT_D2R_C_N<3>	C3647 0.1UF	PCIE_TBT_D2R_P<3>	AD19

PETP_0, PETN_0, PETP_1, PETN_1, PETP_2, PETN_2, PETP_3, PETN_3

=PP3V3_S4_TBT
R3610 47K 5% 1/16W MF-LF 402

TBT_PCIE_RESET_L → R6 PERST_N
TBT_PWR_ON_POC_RST_L → J2 PWR_ON_POC_RSTN

NO STUFF
C3610 0.1UF 10% 16V X5R 402

OMIT
R3615 NOSTUFF NONE 402

DEBUG: For monitoring current/voltage
TBT_MONOBSP → W18 MONOBS_P
TBT_MONOBSN → W16 MONOBS_N
DEBUG: For monitoring clock
TP_TBT_THERM_DP (Use AA8 GND ball for THERM_DN) → Y7 THERMDA

MISC

RSENSE U20 TBT_RSENSE
RBIAS W20 TBT_RBIAS
R3655 1K 1% 1/20W MF 201
NC U4 NC

NOTE: The following pins require testpoints:

0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_LSTX
7 - PCIE_RST_3_N	15 - PB_LSRX

PCIE RESET

Not used in host mode.

PCIE_RST_0_N N6	TP_TBT_PCIE_RESET0_L
PCIE_RST_1_N T1	TP_TBT_PCIE_RESET1_L
PCIE_RST_2_N Y5	TP_TBT_PCIE_RESET2_L
PCIE_RST_3_N U2	TP_TBT_PCIE_RESET3_L
PCIE_CLKREQ_OD_N W6	=TBT_CLKREQ_L → OUT 36
EN_LC_PWR K5	TBT_EN_LC_PWR → OUT 36

CLOCKS

REFCLK_100_IN_P AB21	PCIE_CLK100M_TBT_P ← IN 18 81
REFCLK_100_IN_N AD21	PCIE_CLK100M_TBT_N ← IN 18 81
XTAL_25_IN AA24	SYSCLK_CLK25M_TBT_R 83
XTAL_25_OUT AB23	TP_TBT_XTAL25OUT
TMU_CLK_OUT AA4	TBT_TMU_CLK_OUT
TMU_CLK_IN Y3	TBT_TMU_CLK_IN

=PP3V3_TBTLC_RTR
R3698 10K 5% 1/16W MF-LF 402
R3695 806 1% 1/16W MF-LF 402 — SYSCLK_CLK25M_TBT ← IN 25 83
Divides 3.3V to 1.8V

=PP3V3_TBTLC_RTR
R3697 100K 5% 1/16W MF-LF 402
NO STUFF
R3699 10K 5% 1/16W MF-LF 402
R3696 1K 5% 1/16W MF-LF 402
R3680 10K 5% 1/16W MF-LF 402

TBT_DDC_XBAR_EN_L
TBT_GO2SX_BIDIR
R3681 for CYA, allows separation of GPIO_2/GPIO_9 if necessary. Stuff one of R3861/2.
R3681 0 5% 1/16W MF-LF 402
TBT_GPIO_9
TBT_GPIO_14
NO STUFF
R3683 10K 5% 1/16W MF-LF 402
R3682 10K 5% 1/16W MF-LF 402

=PP3V3_S4_TBT
R3685 10K 5% 1/16W MF-LF 402
R3686 10K 5% 1/16W MF-LF 402
TBT_A_DP_PWRDN
TBT_B_DP_PWRDN
TBT_A_HV_EN
TBT_B_HV_EN
R3688 10K 5% 1/16W MF-LF 402
R3687 10K 5% 1/16W MF-LF 402

=PP3V3_TBTLC_RTR
R3690 3.3K 5% 1/16W MF-LF 402
R3691 3.3K 5% 1/16W MF-LF 402
C3690 1UF 10% 6.3V CERM 402
R3692 3.3K 5% 1/16W MF-LF 402
R3693 3.3K 5% 1/16W MF-LF 402

CRITICAL
OMIT_TABLE
U3690 M95256-RMC6XG MLP
VCC, VSS, THM PAD

(TBT_SPI_MOSI) D
(TBT_SPI_CLK) C
(TBT_SPI_CS_L) S*
TBTROM_WP_L W*
TBTROM_HOLD_L HOLD*
Q (TBT_SPI_MISO)

EEPROM

TBT_SPI_MOSI	R4 EE_DI
TBT_SPI_MISO	P5 EE_DO
TBT_SPI_CS_L	AD3 EE_CS_N
TBT_SPI_CLK	W4 EE_CLK

JTAG/TEST PORT

JTAG_TBT_TDI	V1 TDI
JTAG_TBT_TMS	AB3 TMS
JTAG_TBT_TCK	AA6 TCK
JTAG_TBT_TDO	R2 TDO
TBT_TEST_EN	N4 TEST_EN
TBT_TEST_PWR_GOOD	AB5 TEST_PWR_GOOD

R3625 0 5% 1/16W MF-LF 402
R3629 0 5% 1/16W MF-LF 402

DISPLAYPORT

SINK PORT 0

DP_TBTSNK0_ML_P<3>	E14 DPSNK0_3_P
DP_TBTSNK0_ML_N<3>	D13 DPSNK0_3_N
DP_TBTSNK0_ML_P<2>	E16 DPSNK0_2_P
DP_TBTSNK0_ML_N<2>	D15 DPSNK0_2_N
DP_TBTSNK0_ML_P<1>	E18 DPSNK0_1_P
DP_TBTSNK0_ML_N<1>	D17 DPSNK0_1_N
DP_TBTSNK0_ML_P<0>	E20 DPSNK0_0_P
DP_TBTSNK0_ML_N<0>	D19 DPSNK0_0_N
DP_TBTSNK0_AUXCH_P	A6 DPSNK0_AUX_P
DP_TBTSNK0_AUXCH_N	B5 DPSNK0_AUX_N
DP_TBTSNK0_HPD	U6 DPSNK0_HPD

R3630 100K 5% 1/16W MF-LF 402

SINK PORT 1

DP_TBTSNK1_ML_P<3>	E6 DPSNK1_3_P
DP_TBTSNK1_ML_N<3>	D5 DPSNK1_3_N
DP_TBTSNK1_ML_P<2>	E8 DPSNK1_2_P
DP_TBTSNK1_ML_N<2>	D7 DPSNK1_2_N
DP_TBTSNK1_ML_P<1>	E10 DPSNK1_1_P
DP_TBTSNK1_ML_N<1>	D9 DPSNK1_1_N
DP_TBTSNK1_ML_P<0>	E12 DPSNK1_0_P
DP_TBTSNK1_ML_N<0>	D11 DPSNK1_0_N
DP_TBTSNK1_AUXCH_P	A4 DPSNK1_AUX_P
DP_TBTSNK1_AUXCH_N	B3 DPSNK1_AUX_N
DP_TBTSNK1_HPD	T5 DPSNK1_HPD

R3631 100K 5% 1/16W MF-LF 402

SOURCE PORT 0

DPSRC_3_P	A14 TP_DP_TBTSRC_ML_CP<3>
DPSRC_3_N	B15 TP_DP_TBTSRC_ML_CN<3>
DPSRC_2_P	A12 TP_DP_TBTSRC_ML_CP<2>
DPSRC_2_N	B13 TP_DP_TBTSRC_ML_CN<2>
DPSRC_1_P	A10 TP_DP_TBTSRC_ML_CP<1>
DPSRC_1_N	B11 TP_DP_TBTSRC_ML_CN<1>
DPSRC_0_P	A8 TP_DP_TBTSRC_ML_CP<0>
DPSRC_0_N	B9 TP_DP_TBTSRC_ML_CN<0>
DPSRC_AUX_P	C2 TP_DP_TBTSRC_AUXCH_CP
DPSRC_AUX_N	D3 TP_DP_TBTSRC_AUXCH_CN
DPSRC_HPD_OD	V3 DP_TBTSRC_HPD → 73

R3632 100K 5% 1/16W MF-LF 402

GPIO_2/GO2SX	Y1 TBT_GO2SX_BIDIR ↔ BI 15 21 34
(FORCE_PWR) GPIO_3	W2 TBT_PWR_EN ← IN 26
GPIO_4/WAKE_N_OD	J4 =TBT_WAKE_L → OUT 19
GPIO_5/CIO_PLUG_EVENT	AA2 TBT_CIO_PLUG_EVENT → OUT 15 21
GPIO_6/CIO_SDA_OD	AB1 =I2C_TBTRTR_SDA ↔ BI 48 89
GPIO_7/CIO_SCL_OD	AC2 =I2C_TBTRTR_SCL ← IN 48 89
GPIO_8/EN_CIO_PWR_OD*	P3 (TBT_EN_CIO_PWR_L)
GPIO_9/OK2GO2SX_OD*	M5 TBT_GPIO_9 34
GPIO_14	T3 TBT_GPIO_14 34
GPIO_15	V5 TBT_DDC_XBAR_EN_L → OUT 34 74

TBT_PWR_REQ_L → OUT 15 20
TBT_EN_CIO_PWR_L → OUT 36
MAKE_BASE=TRUE

PORT0

TBT_A_R2D_C_P<0>	G24 PA_CIO0_TX_P/DP_SRC_0_P
TBT_A_R2D_C_N<0>	E24 PA_CIO0_TX_N/DP_SRC_0_N
TBT_A_D2R_P<0>	G22 PA_CIO0_RX_P
TBT_A_D2R_N<0>	E22 PA_CIO0_RX_N
TBT_A_CONFIG1_BUF	K1 PA_CONFIG1/CIO_0_LSEO
TBT_A_CONFIG2_RC	G4 PA_CONFIG2/CIO_0_LSOE

PORT2

PB_CIO2_TX_P/DP_SRC_0_P	R24 TBT_B_R2D_C_P<0> → OUT 76 89
PB_CIO2_TX_N/DP_SRC_0_N	N24 TBT_B_R2D_C_N<0> → OUT 76 89
PB_CIO2_RX_P	R22 TBT_B_D2R_P<0> ← IN 76 89
PB_CIO2_RX_N	N22 TBT_B_D2R_N<0> ← IN 76 89
PB_CONFIG1/CIO_2_LSEO	P1 TBT_B_CONFIG1_BUF → OUT 76
PB_CONFIG2/CIO_2_LSOE	H5 TBT_B_CONFIG2_RC ← IN 76

PORT1

TBT_A_R2D_C_P<1>	L24 PA_CIO1_TX_P/DP_SRC_2_P
TBT_A_R2D_C_N<1>	J24 PA_CIO1_TX_N/DP_SRC_2_N
TBT_A_D2R_P<1>	L22 PA_CIO1_RX_P
TBT_A_D2R_N<1>	J22 PA_CIO1_RX_N
TBT_A_LSTX	N2 PA_LSTX/CIO_1_LSEO
TBT_A_LSRX	J6 PA_LSRX/CIO_1_LSOE

PORT3

PB_CIO3_TX_P/DP_SRC_2_P	W24 TBT_B_R2D_C_P<1> → OUT 76 89
PB_CIO3_TX_N/DP_SRC_2_N	U24 TBT_B_R2D_C_N<1> → OUT 76 89
PB_CIO3_RX_P	W22 TBT_B_D2R_P<1> ← IN 76 89
PB_CIO3_RX_N	U22 TBT_B_D2R_N<1> ← IN 76 89
PB_LSTX/CIO_3_LSEO	L6 TBT_B_LSTX → OUT 76
PB_LSRX/CIO_3_LSOE	G6 TBT_B_LSRX ← IN 76

PORTS

DP_TBTPA_ML_C_P<1>	A16 PA_DPSRC_1_P
DP_TBTPA_ML_C_N<1>	B17 PA_DPSRC_1_N
DP_TBTPA_ML_C_P<3>	A18 PA_DPSRC_3_P
DP_TBTPA_ML_C_N<3>	B19 PA_DPSRC_3_N
DP_TBTPA_AUXCH_C_P	F3 PA_AUX_P
DP_TBTPA_AUXCH_C_N	F1 PA_AUX_N
DP_TBTPA_HPD	H1 PA_DPSRC_HPD
TBT_A_HV_EN	G2 GPIO_0/PA_HV_EN/BYP0
TBT_A_CIO_SEL	M3 GPIO_10/PA_CIO_SEL/BYP1
TBT_A_DP_PWRDN	H3 GPIO_12/PA_DP_PWRDN/BYP2

DP_TBTPB_ML_C_P<1>	A20 PB_DPSRC_1_P
DP_TBTPB_ML_C_N<1>	B21 PB_DPSRC_1_N
DP_TBTPB_ML_C_P<3>	A22 PB_DPSRC_3_P
DP_TBTPB_ML_C_N<3>	B23 PB_DPSRC_3_N
DP_TBTPB_AUXCH_C_P	D1 PB_AUX_P
DP_TBTPB_AUXCH_C_N	E2 PB_AUX_N
DP_TBTPB_HPD	K3 PB_DPSRC_HPD
TBT_B_HV_EN	M1 GPIO_1/PB_HV_EN/BYP0
TBT_B_CIO_SEL	L2 GPIO_11/PB_CIO_SEL/BYP1
TBT_B_DP_PWRDN	L4 GPIO_13/PB_DP_PWRDN/BYP2

SNK0 AC Coupling

DP_TBTSNK0_ML_C_P<0>	C3620 0.1UF	DP_TBTSNK0_ML_P<0>
DP_TBTSNK0_ML_C_N<0>	C3621 0.1UF	DP_TBTSNK0_ML_N<0>
DP_TBTSNK0_ML_C_P<1>	C3622 0.1UF	DP_TBTSNK0_ML_P<1>
DP_TBTSNK0_ML_C_N<1>	C3623 0.1UF	DP_TBTSNK0_ML_N<1>
DP_TBTSNK0_ML_C_P<2>	C3624 0.1UF	DP_TBTSNK0_ML_P<2>
DP_TBTSNK0_ML_C_N<2>	C3625 0.1UF	DP_TBTSNK0_ML_N<2>
DP_TBTSNK0_ML_C_P<3>	C3626 0.1UF	DP_TBTSNK0_ML_P<3>
DP_TBTSNK0_ML_C_N<3>	C3627 0.1UF	DP_TBTSNK0_ML_N<3>
DP_TBTSNK0_AUXCH_C_P	C3628 0.1UF	DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_C_N	C3629 0.1UF	DP_TBTSNK0_AUXCH_N

SNK1 AC Coupling

DP_TBTSNK1_ML_C_P<0>	C3630 0.1UF	DP_TBTSNK1_ML_P<0>
DP_TBTSNK1_ML_C_N<0>	C3631 0.1UF	DP_TBTSNK1_ML_N<0>
DP_TBTSNK1_ML_C_P<1>	C3632 0.1UF	DP_TBTSNK1_ML_P<1>
DP_TBTSNK1_ML_C_N<1>	C3633 0.1UF	DP_TBTSNK1_ML_N<1>
DP_TBTSNK1_ML_C_P<2>	C3634 0.1UF	DP_TBTSNK1_ML_P<2>
DP_TBTSNK1_ML_C_N<2>	C3635 0.1UF	DP_TBTSNK1_ML_N<2>
DP_TBTSNK1_ML_C_P<3>	C3636 0.1UF	DP_TBTSNK1_ML_P<3>
DP_TBTSNK1_ML_C_N<3>	C3637 0.1UF	DP_TBTSNK1_ML_N<3>
DP_TBTSNK1_AUXCH_C_P	C3638 0.1UF	DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_C_N	C3639 0.1UF	DP_TBTSNK1_AUXCH_N

For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.

SYNC_MASTER=D7i_MLB SYNC_DATE=N/A
PAGE TITLE: Thunderbolt Host (1 of 2)

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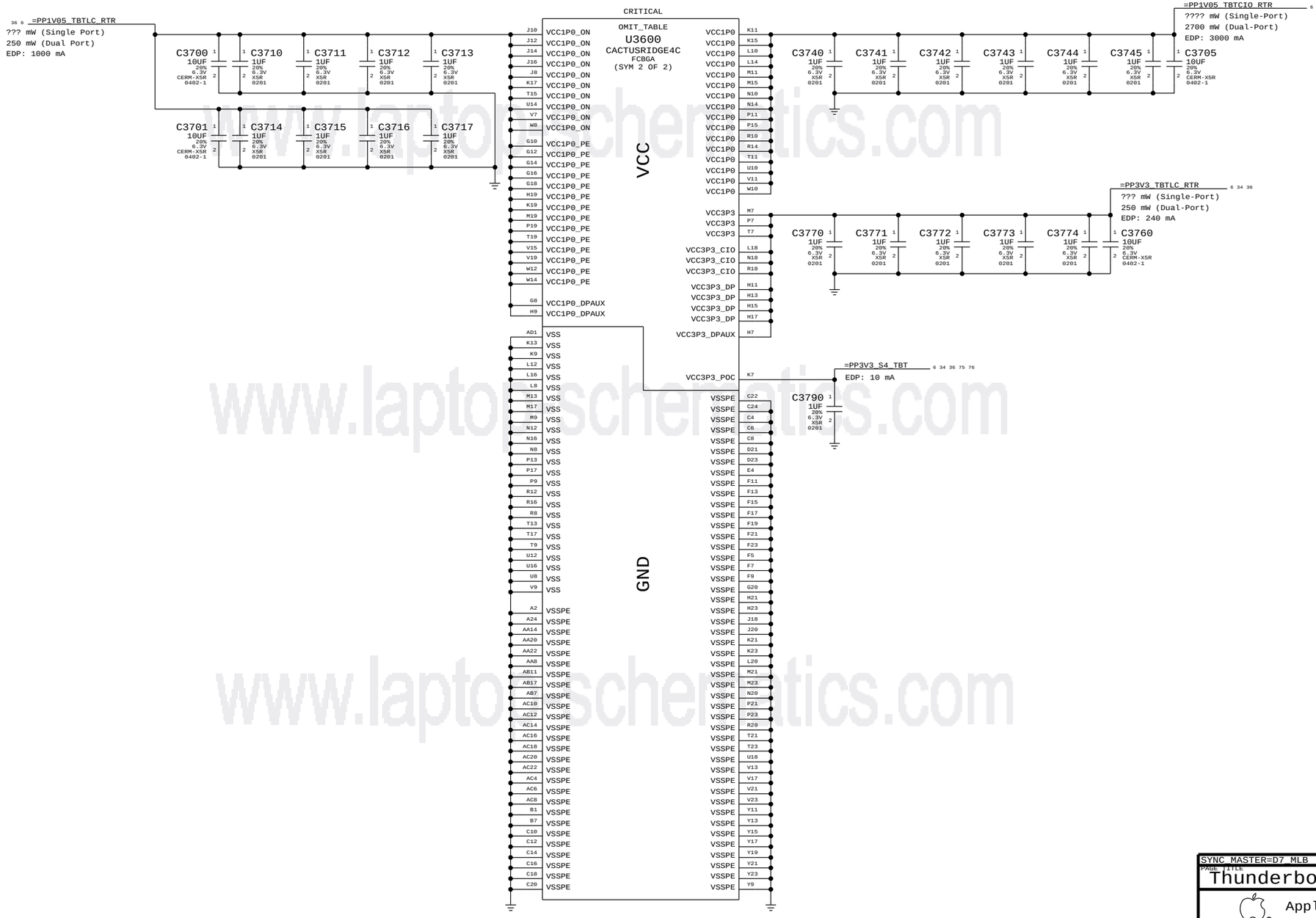

EDP current / power consumption figures from CR DG v0.57, IBL doc #472455.

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

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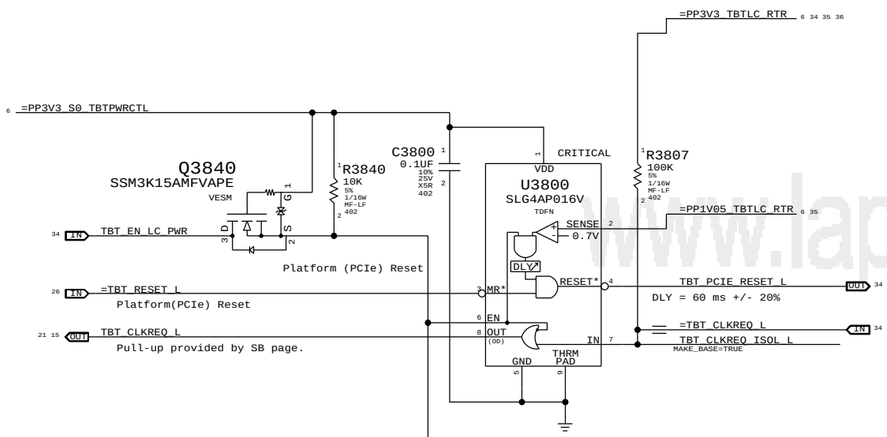
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

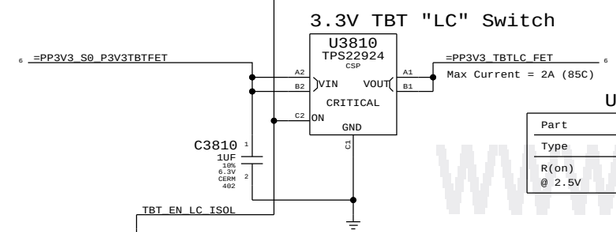
Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

Supervisor & CLKREQ# Isolation



3.3V TBT "LC" Switch



U3810

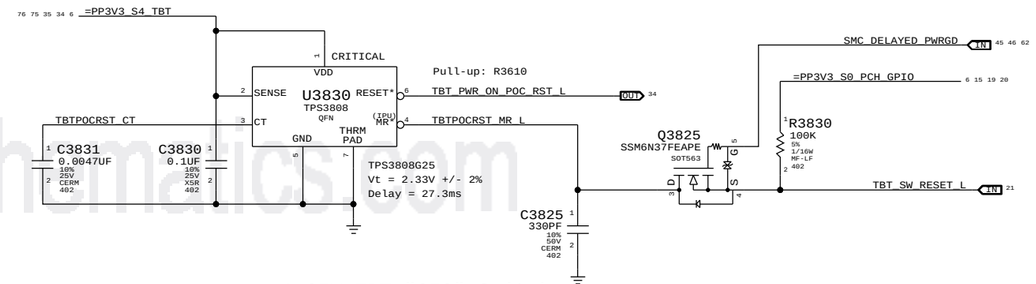
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

U3815

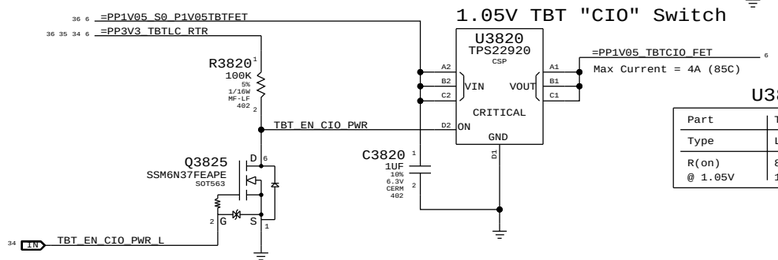
Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ 28.6 mOhm Max

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.



1.05V TBT "CIO" Switch



U3820

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

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Thunderbolt Power Support

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

=PP3V3_ENET_PHY
281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
PP3V3R1V8_CR_VDDIO
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.15 mm
VOLTAGE=3.3V

ENET_SR_LX
ENET_SR_VFB
Internal 1.2V Switching Regulator pins.

=PP1V2_ENET_PHY
396mA (1000base-T, Caesar II)

CRITICAL L3900 FERR-600-OHM-300MA-0.85OHM 0402
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
C3900 0.1UF 10% 16V X5R-CERM 0201
ENET_XTALVDDH MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

CRITICAL L3905 FERR-600-OHM-300MA-0.85OHM 0402
PP3V3_ENET_PHY_BIASVDDH MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
C3905 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3910 FERR-600-OHM-300MA-0.85OHM 0402
PP3V3_ENET_PHY_AVDDH MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X5R-CERM 0201
C3911 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3920 FERR-600-OHM-300MA-0.85OHM 0402
PP1V2_ENET_PHY_AVDDL MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
C3921 0.1UF 10% 16V X5R-CERM 0201
C3920 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3925 FERR-600-OHM-0.5A SM
PP1V2_ENET_PHY_PCIEPLL MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
C3926 0.1UF 10% 16V X5R-CERM 0201
C3925 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3930 FERR-600-OHM-300MA-0.85OHM 0402
PP1V2_ENET_PHY_GPHYPLL MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.15 mm VOLTAGE=1.2V
C3931 0.1UF 10% 16V X5R-CERM 0201
C3930 4.7UF 20% 6.3V X5R-CERM1 402

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 20% 6.3V X5R-CERM1 402
C3916 0.1UF 10% 16V X5R-CERM 0201
C3936 0.1UF 10% 16V X5R-CERM 0201
C3935 10UF 20% 6.3V X5R 603

AVDDH BIASVDDH XTALVDDH VDDO SR_VDD SR_VDDP SR_LX SR_VFB AVDDL PCIE_PLLVDDL GPHY_PLLVDDL VDDC

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

=PP3V3_S0_ENET
R3942 1K 5% 1/16W MF-LF 402 Current Limiting Resistor

C3950 0.1UF 10% 16V X5R-CERM 0201
C3951 0.1UF 10% 16V X5R-CERM 0201
C3955 0.1UF 10% 16V X5R-CERM 0201
C3956 0.1UF 10% 16V X5R-CERM 0201

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N

=ENET_WAKE_L
(See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

OMIT_TABLE
U3900
BCM57766C0KMLG
QFN-8X8

ENET_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
ENET_RESET_L
ENET_CLKREQ_L
ENET_LOW_PWR
SMB_ENET_SCL
SMB_ENET_SDA
ENET_SCLK
ENET_MISO
ENET_MOSI
ENET_CS_L
ENET_CR_3V3_EN_L
ENET_TRAFFICLED_L
SYSCLK_CLK25M_ENET
ENET_RDAC

VMAIN_PRSNT (IPD-ENET)
PCIE_TXD_N
PCIE_TXD_P
PCIE_RXD_P
PCIE_RXD_N
PCIE_REFCLK_P
PCIE_REFCLK_N
PERST* (IPD)
CLKREQ* (OD)
WAKE* (OD)
LOW_PWR (IPD)
SMB_CLK
SMB_DATA (IPD-ENETM)
SCLK_SPD1000LED*
SI/EEDATA
SO_LINKLED*
CS*/EECLK
SPD100LED*/SERIAL_DO (OD)
TRAFFICLED*/SERIAL_DI (OD)
XTALI
XTALO
RDAC
THRM_PAD

NC

R3965 1.24K 1% 1/16W MF-LF 402

GPIO_0/CR_ACT_LED* (IPD)
GPIO_1/LR_OUT
GPIO_2/MEDIA_SENSE
SD_DETECT* (IPx-ENET)
CR_CMD
CR_CLK
CR_DATA0
CR_DATA1
CR_DATA2
CR_DATA3
CR_DATA4
CR_DATA5
CR_DATA6
CR_DATA7
MS_INS*
CR_LED*/CR_BUS_PWR (IPU-ENET)
CR_WP* (IPU-ENET)
SR_DISABLE (NO IPU OR IPD-ENET)

NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.

TRD0_P TRD0_N TRD1_P TRD1_N TRD2_P TRD2_N TRD3_P TRD3_N
ENETCONN_MDI P<0> N<0> P<1> N<1> P<2> N<2> P<3> N<3>

ENET_CR_1V8_EN
ENET_MEDIA_SENSE
ENET_SD_DETECT_L
ENET_SD_CMD
ENET_SD_CLK
ENET_CR_DATA<0> ... ENET_CR_DATA<7>
ENET_CR_PWREN
ENET_SR_DISABLE

R3961 33 5% 1/20W MF 201 SDCONN_CMD
R3979 33 5% 1/20W MF 201 SDCONN_CLK
R3971 33 5% 1/20W MF 201 SDCONN_DATA<0>
R3972 33 5% 1/20W MF 201 SDCONN_DATA<1>
R3973 33 5% 1/20W MF 201 SDCONN_DATA<2>
R3974 33 5% 1/20W MF 201 SDCONN_DATA<3>
R3975 33 5% 1/20W MF 201 SDCONN_DATA<4>
R3976 33 5% 1/20W MF 201 SDCONN_DATA<5>
R3977 33 5% 1/20W MF 201 SDCONN_DATA<6>
R3978 33 5% 1/20W MF 201 SDCONN_DATA<7>
No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

R3981 1K 5% 1/16W MF-LF 402

PP3V3R1V8_ENET_LR_OUT
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.15 mm
VOLTAGE=3.3V

SDCONN_CMD
SDCONN_CLK
SDCONN_DATA<0> ... SDCONN_DATA<7>
SDCONN_WP

ENET supports both active-levels for WP.

ENET 1.2V SR IS ENABLED IF FLOATING.
(See note)

ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE
If ENET switching regulator is used, this pin can float (alias to TP_). If not used, must be pulled to 3.3V ENET via 1K resistor (not provided on this page).

PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900
PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900
PLACEMENT_NOTE=PLACE R3975 NEAR U3900
PLACEMENT_NOTE=PLACE R3976 NEAR U3900
PLACEMENT_NOTE=PLACE R3977 NEAR U3900
PLACEMENT_NOTE=PLACE R3978 NEAR U3900

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

=PP3V3_ENET_PHY
C3990 0.1UF 10% 16V X5R-CERM 0201
U3990 AT45DB011D SOIC-8S1 OMIT_TABLE
VCC SCK CS* WP* RESET* SI SO GND
ENET_SCLK ENET_CS_L ENET_MOSI ENET_MISO
NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012
PAGE TITLE: ETHERNET PHY (CAESAR IV)
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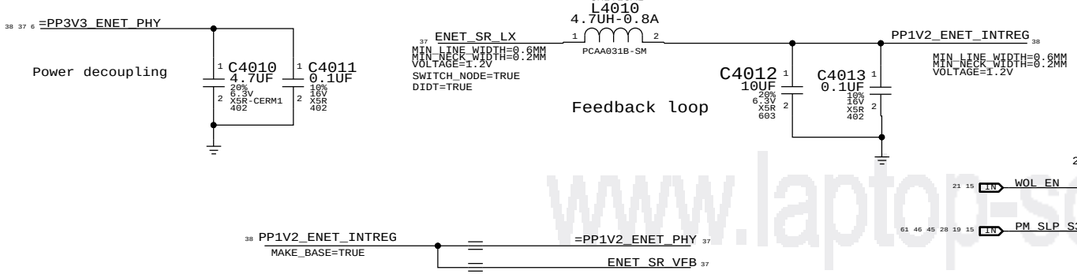
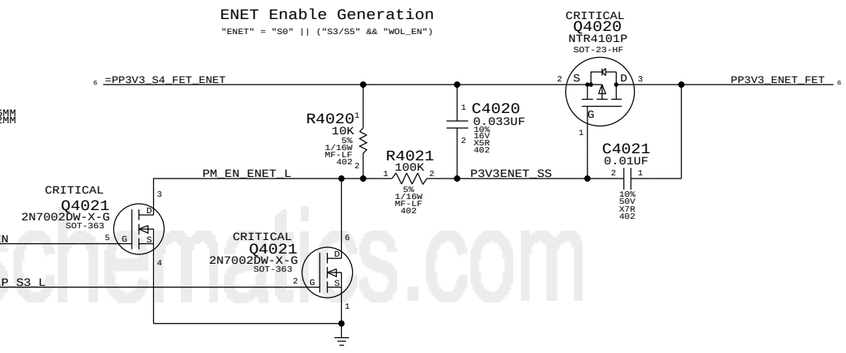
CAESAR IV 1.2V INT.VR CMPTS

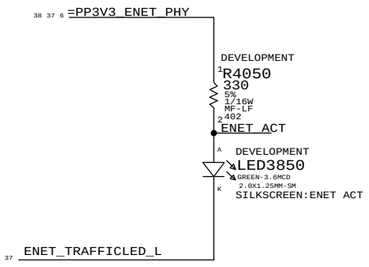


ENET Enable Generation

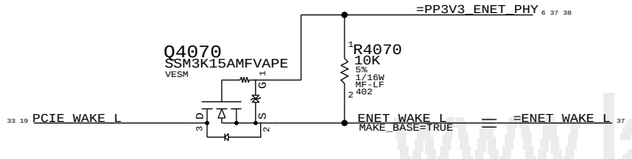
"ENET" = "S0" || ("S3/S5" && "WOL_EN")

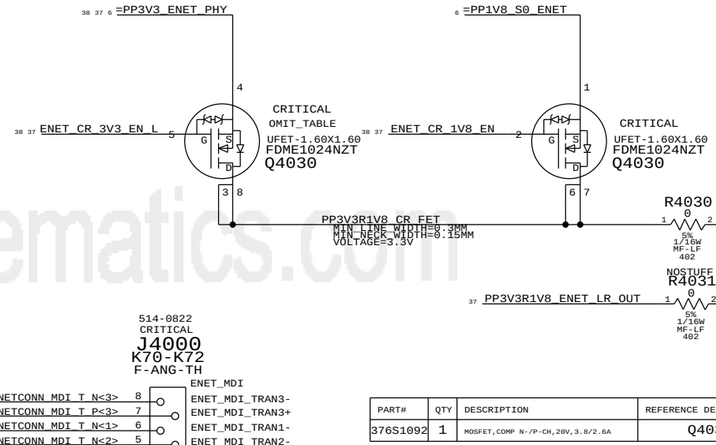


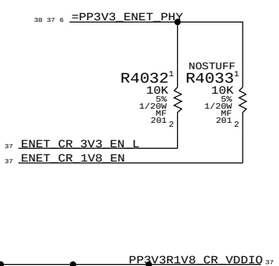
CAESAR IV ACTIVITY LED

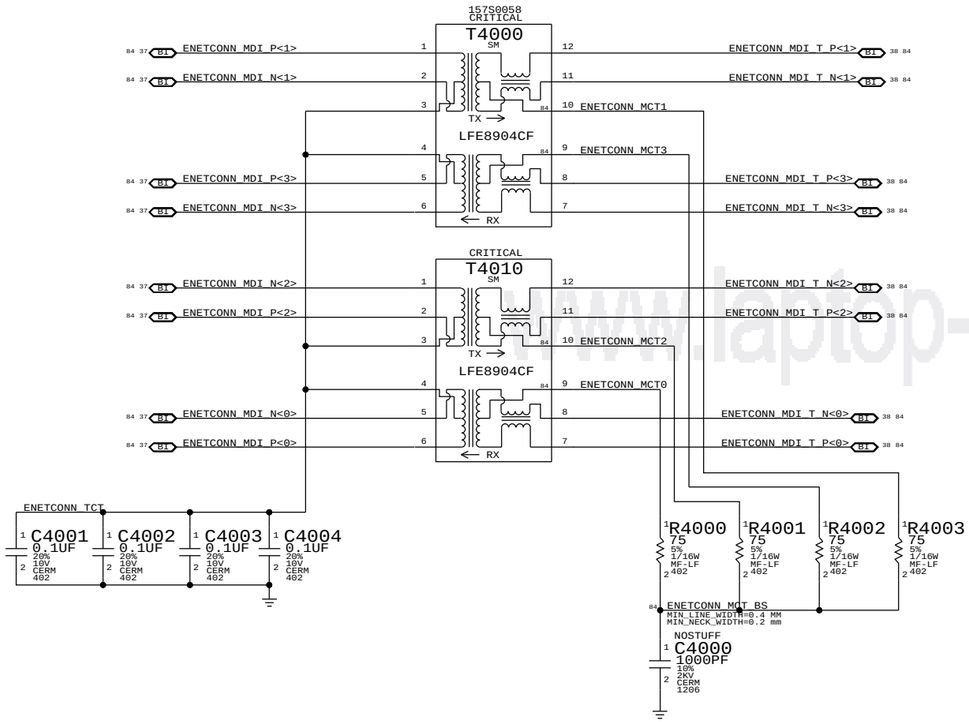


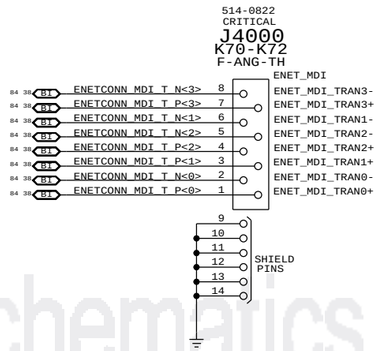
CAESAR IV WAKE# ISOLATION











PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
376S1092	1	MOSFET,COMP N-/P-CH,20V,3.8/2.6A	Q4030	CRITICAL	

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE
Ethernet Support & Connector

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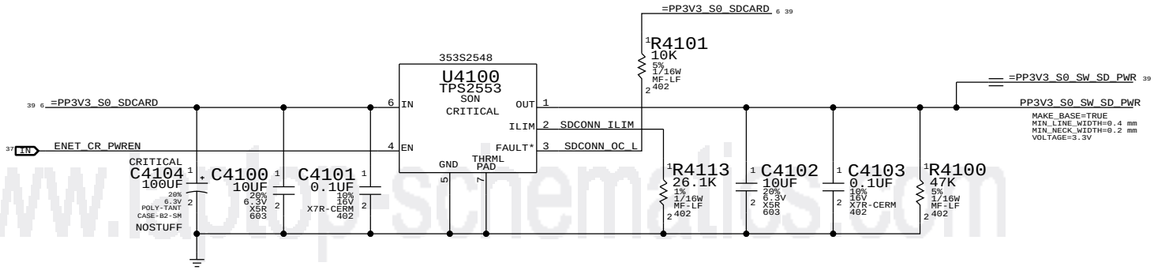
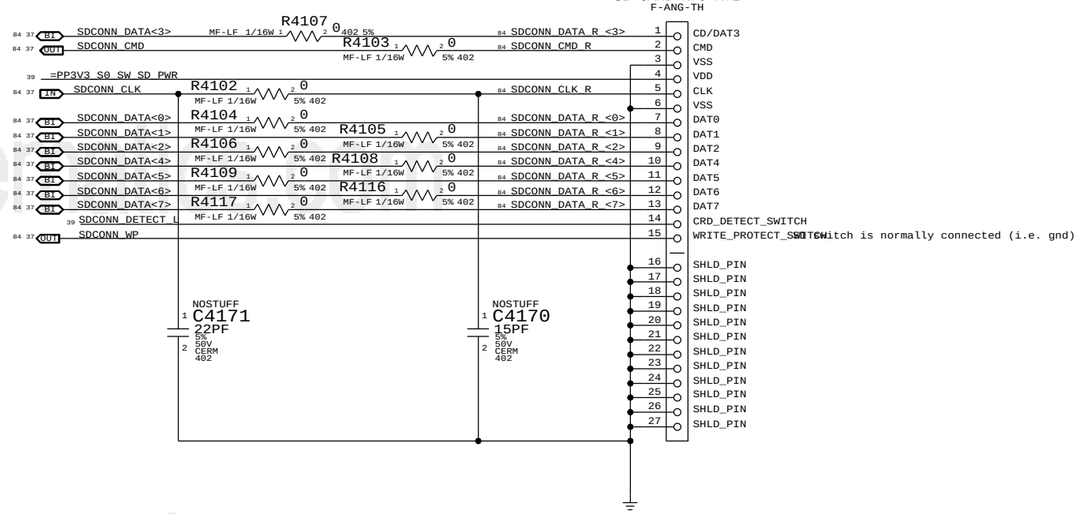
SD CARD 3.3V OVERCURRENT PROTECTION CHIP



CRITICAL
516-0249

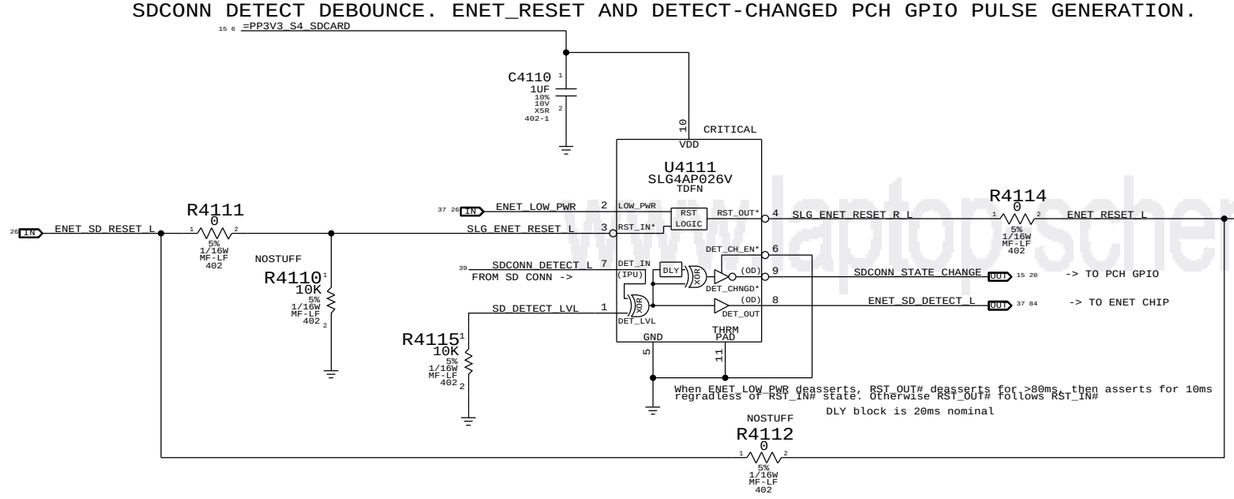
SD CARD CONNECTOR

J4100
SD-CARD-K70-K72
F-ANG-TH



SWITCH is normally connected (i.e. gnd)

SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

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SD READER CONNECTOR

Apple Inc.

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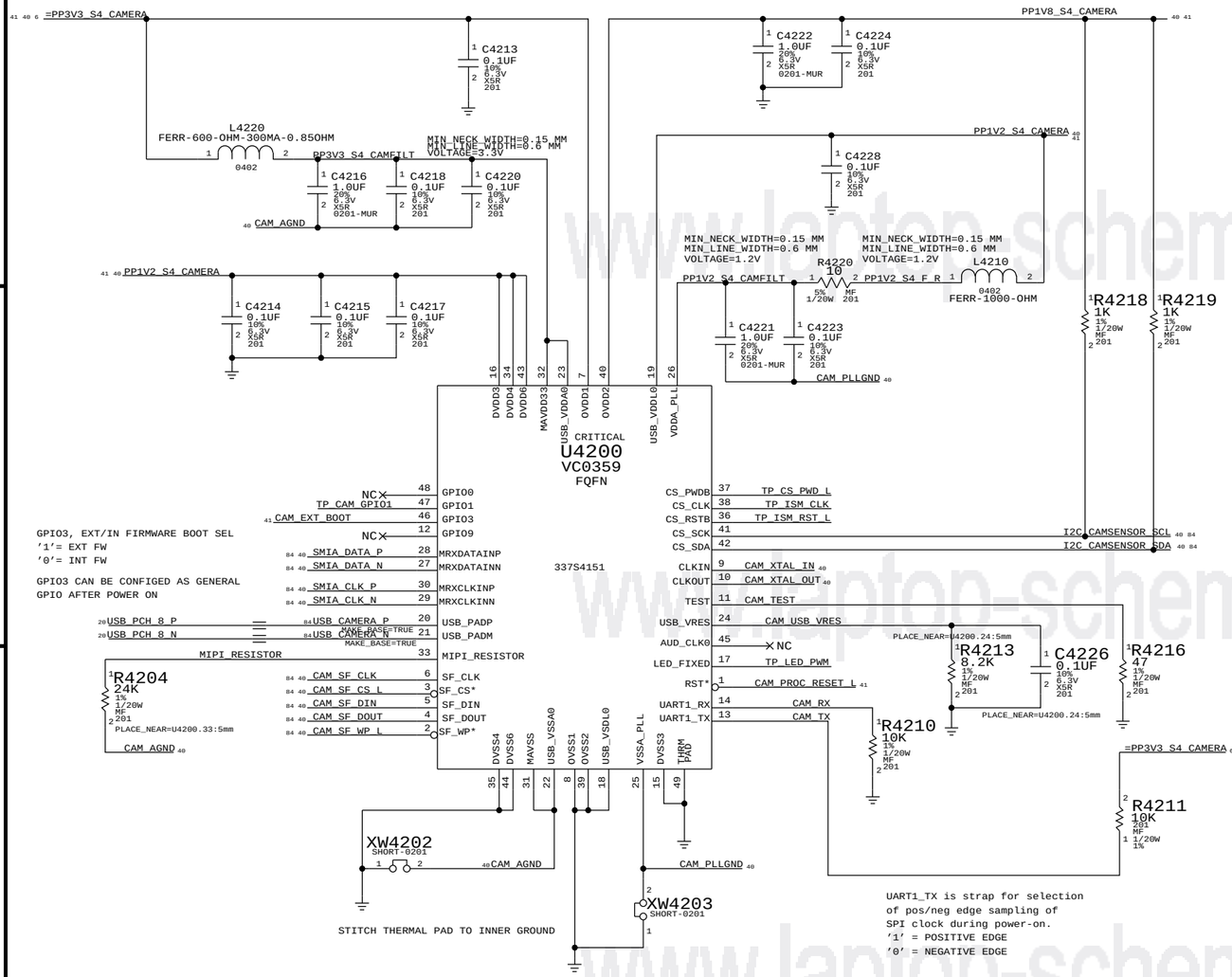
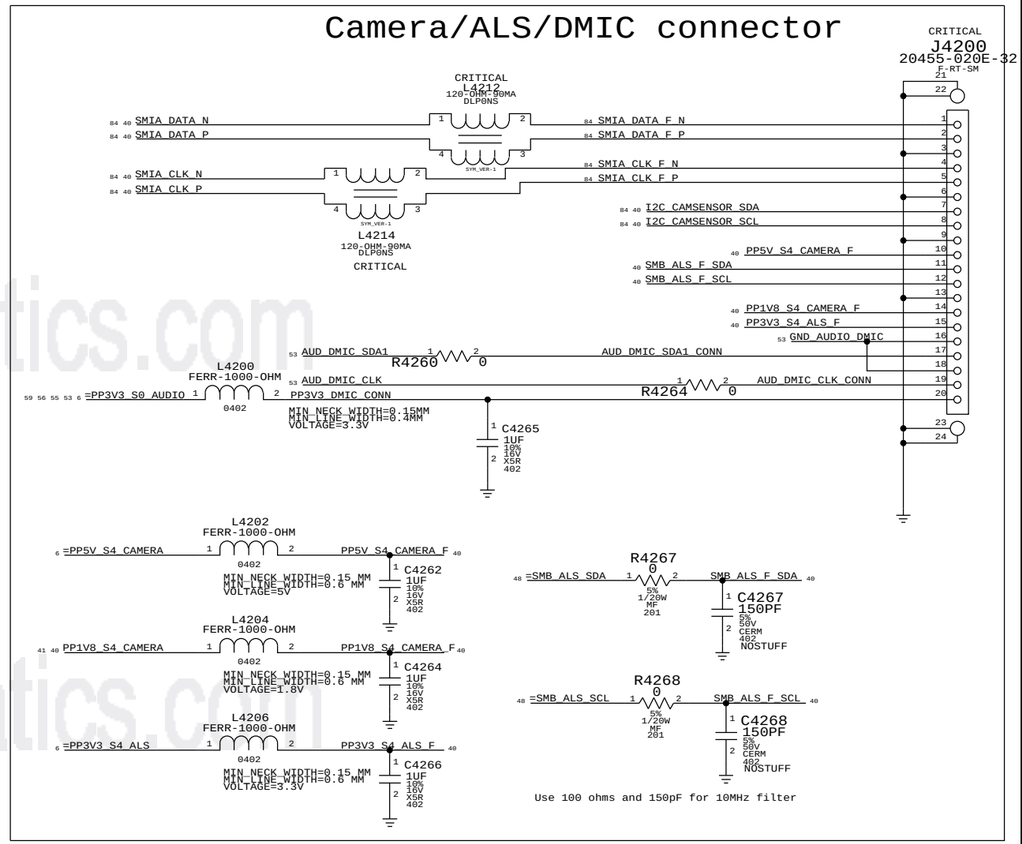
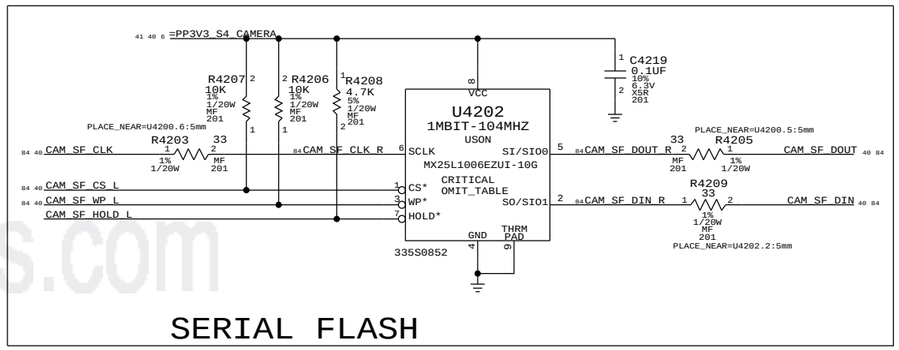
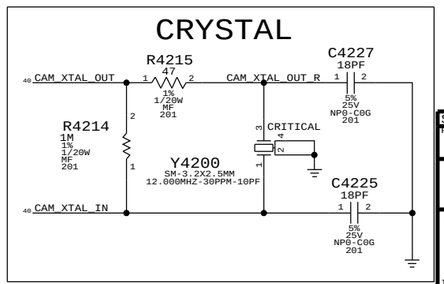
USB CAMERA CONTROLLER



Camera/ALS/DMIC connector







SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE: Camera Controller

Apple Inc.

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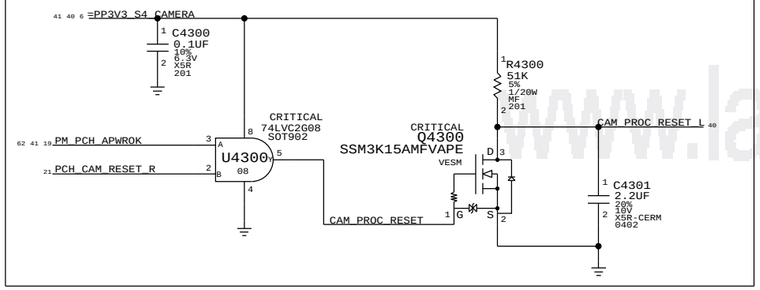
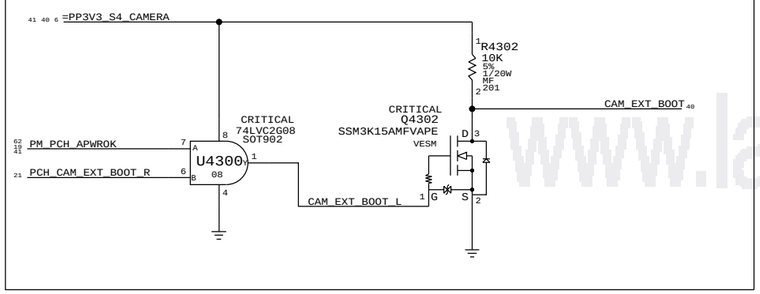
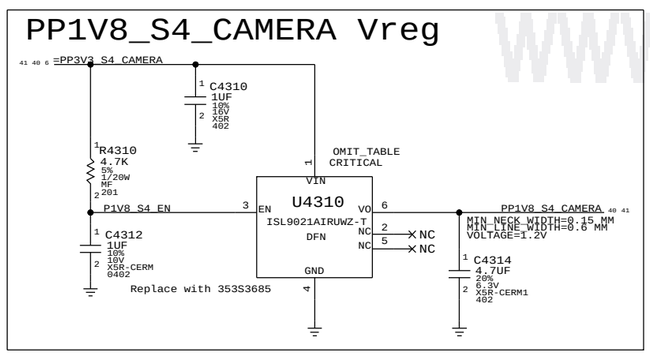
Camera Processor Reset



Camera Processor ExtBoot Cntl

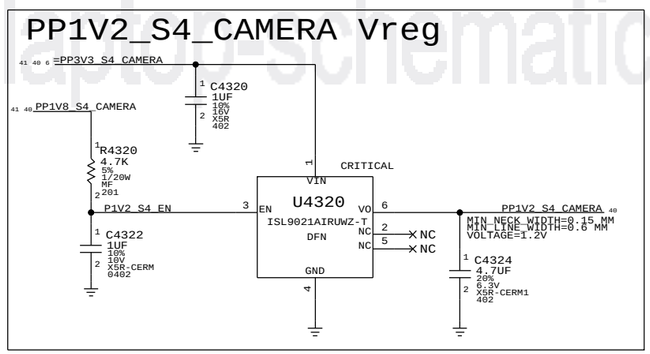


PP1V8_S4_CAMERA Vreg



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S3685	1	IC,ISL9021A,LDO REG,1.8V,250MA,DFN6	U4310	CRITICAL	

PP1V2_S4_CAMERA Vreg



PAGE TITLE
Camera Controller Support

Apple Inc.

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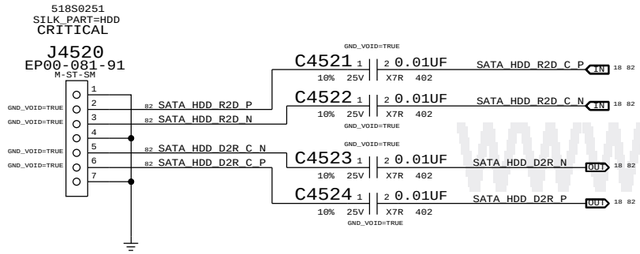
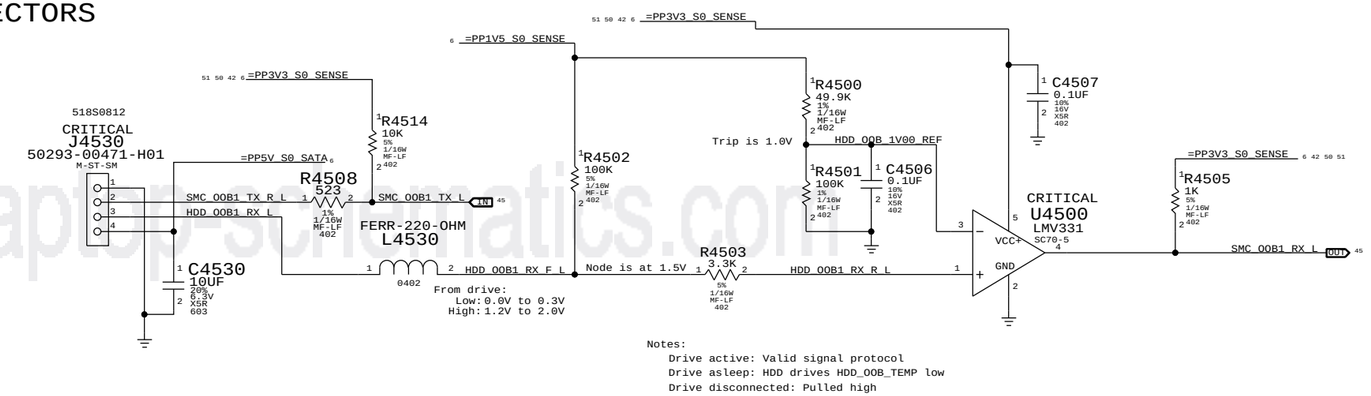
HDD CONNECTORS



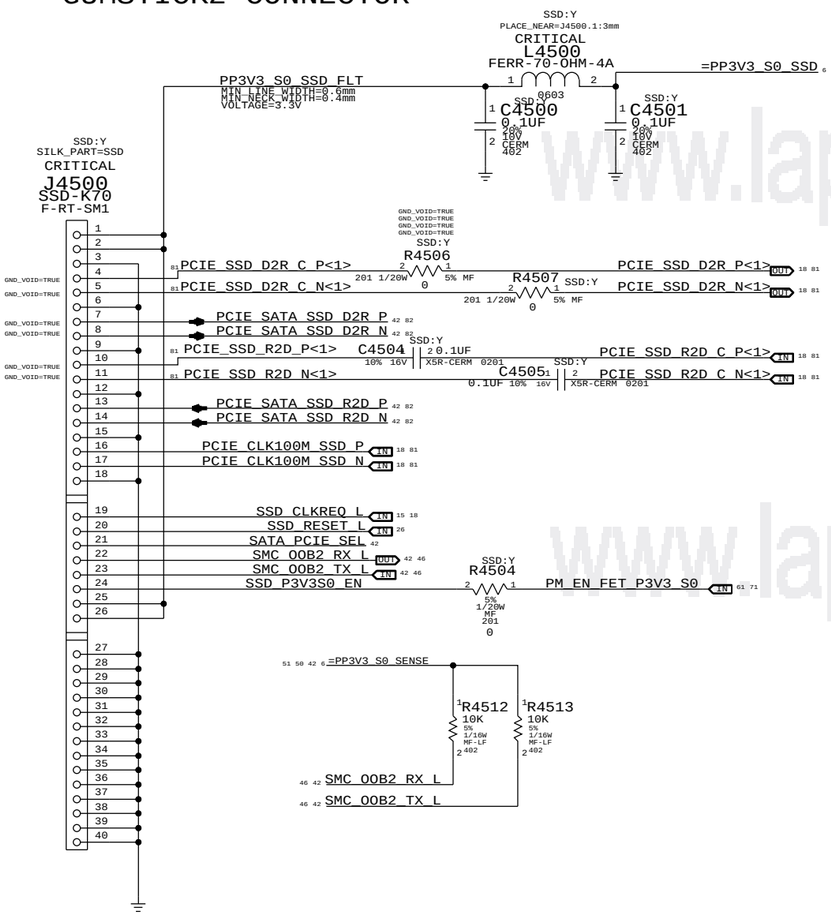
HDD Out-of-Band Temperature Sensing

Temperature read from SATA power connecter pin 11

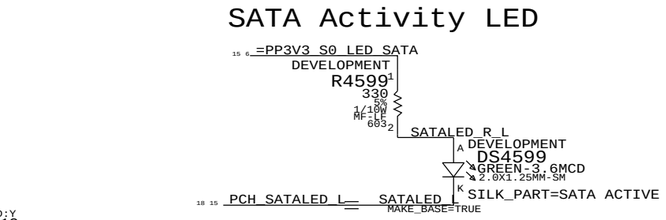


Notes:
- Drive active: Valid signal protocol
- Drive asleep: HDD drives HDD_OOB_TEMP low
- Drive disconnected: Pulled high

GUMSTICK2 CONNECTOR



SATA Activity LED



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S0002	2	RES,MF,1/20W,0.0OHM,5,0201,SMD	C4515,C4516		SSD:Y

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

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Apple Inc.

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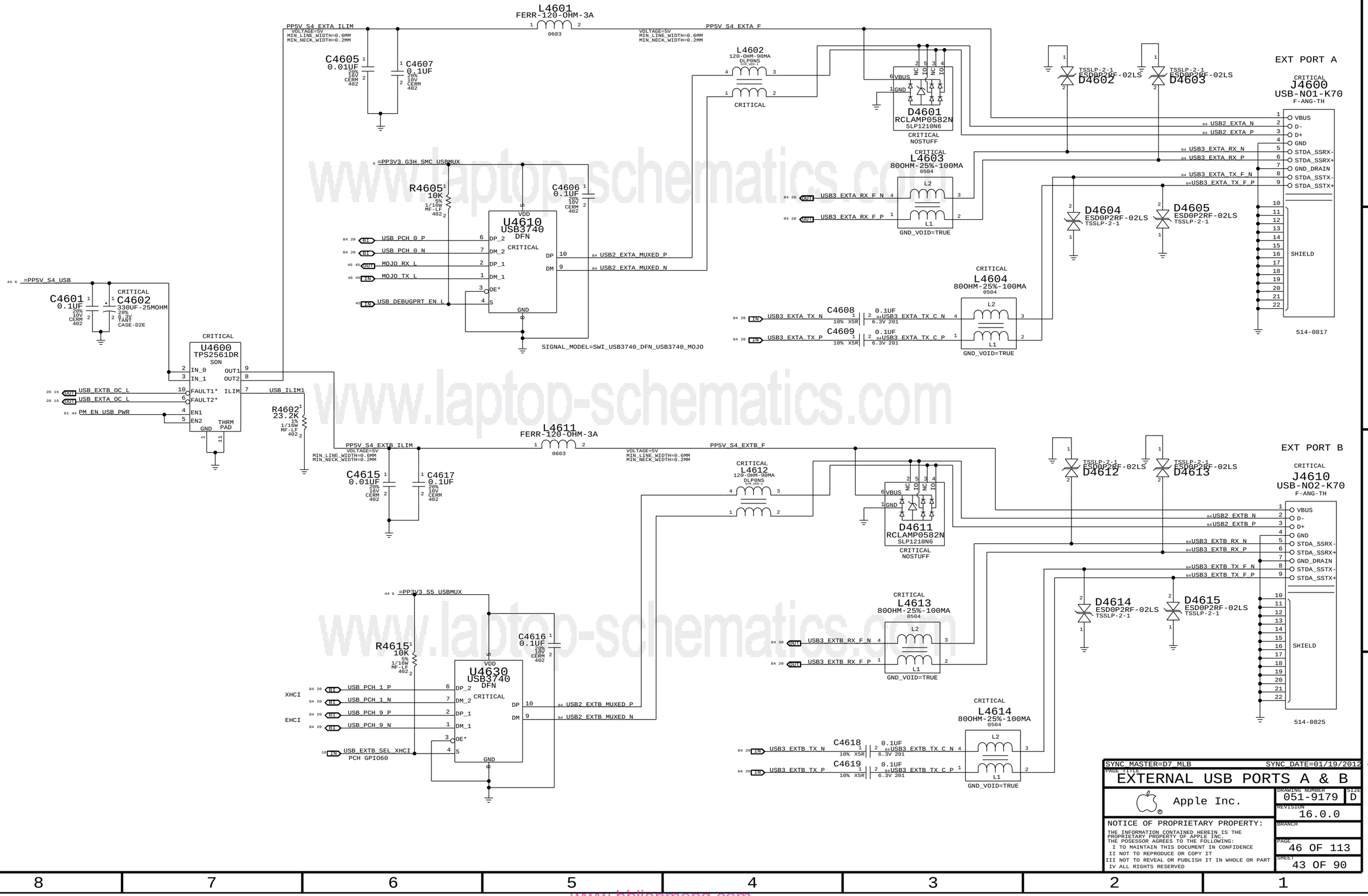
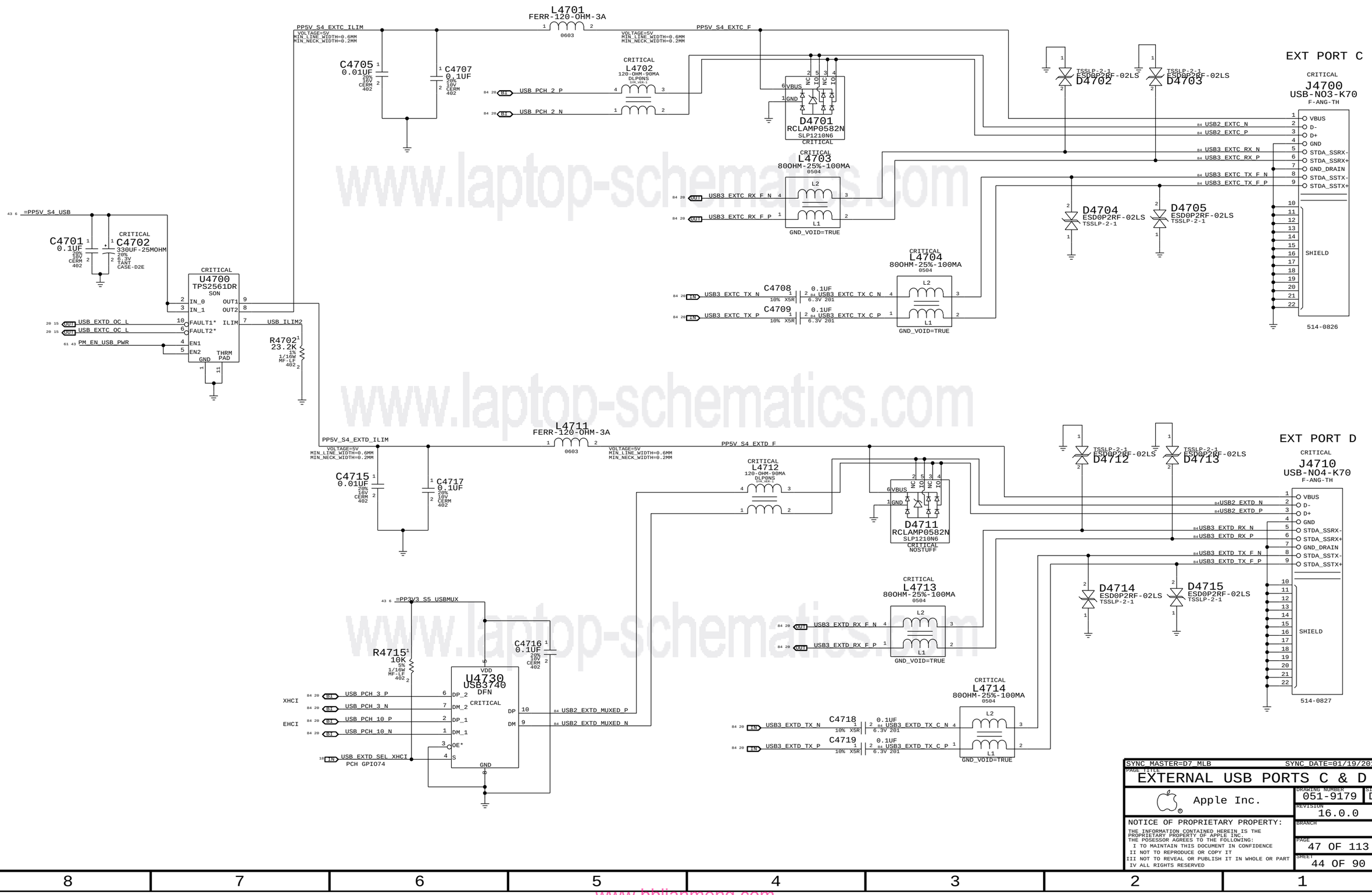
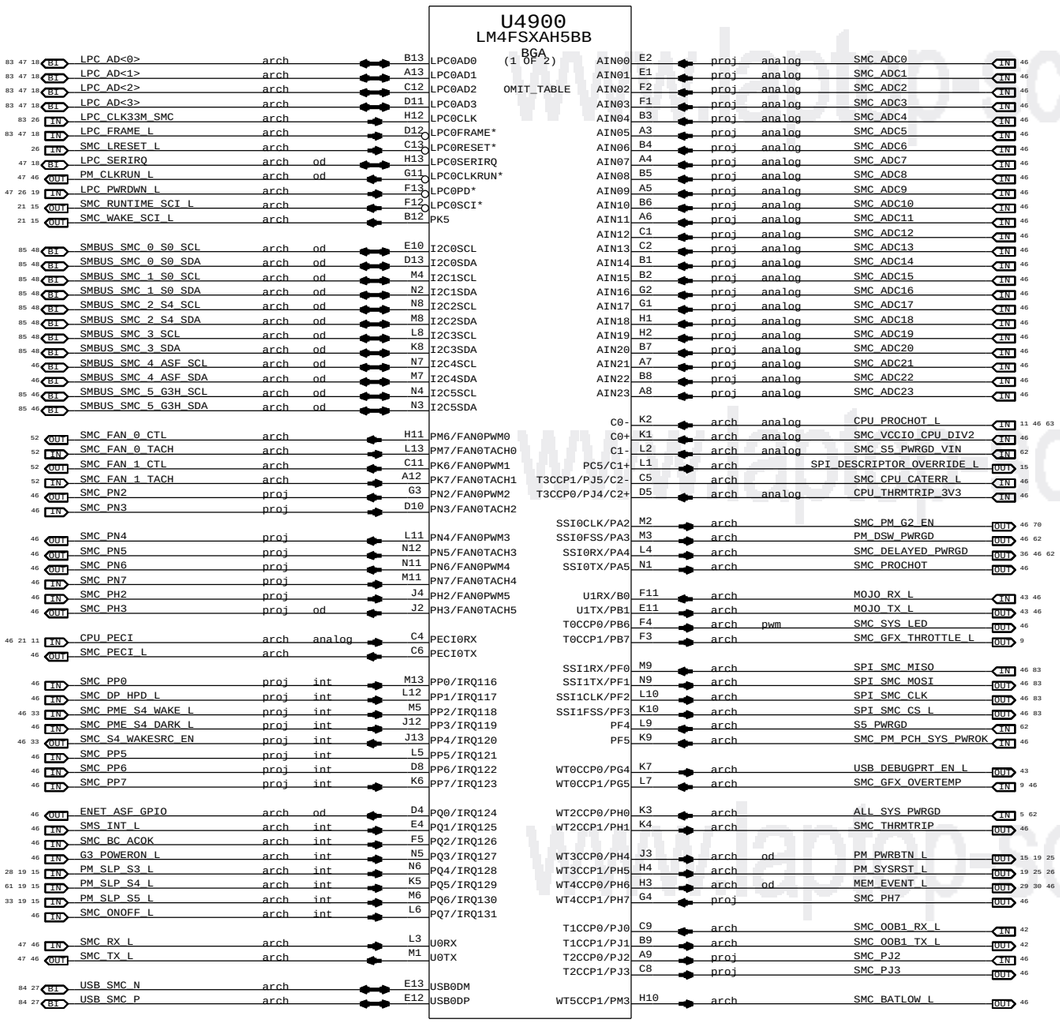
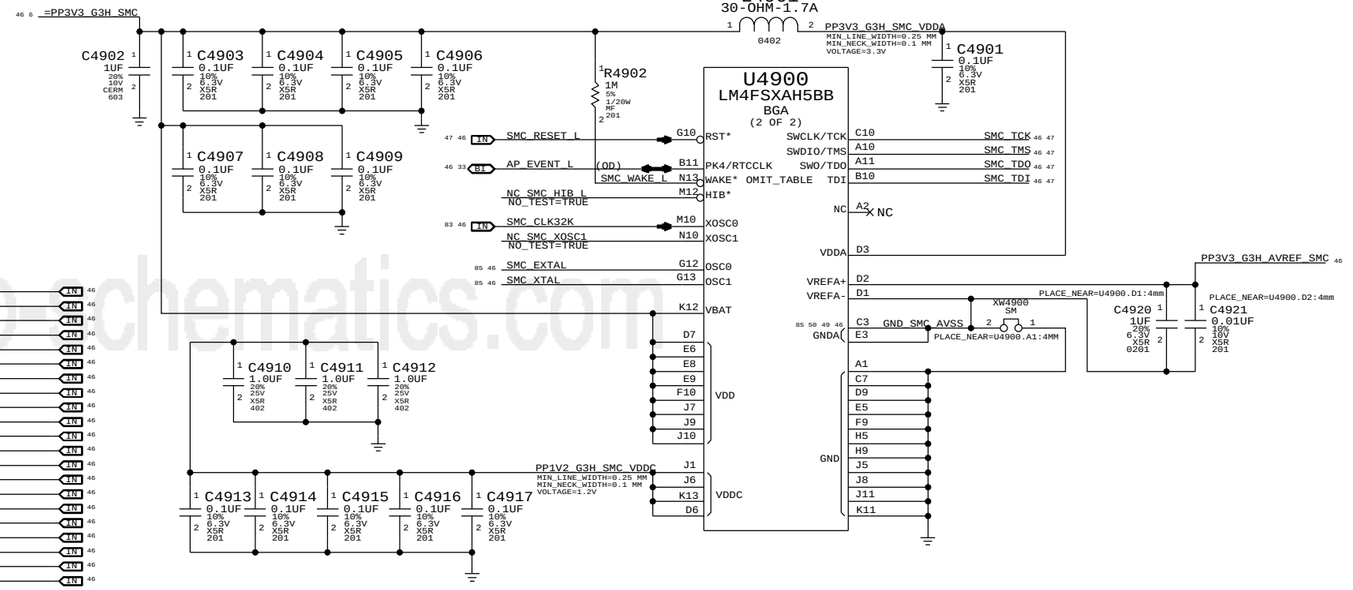




NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





SYNC_MASTER=D7_MLB	SYNC_DATE=01/19/2012
PAGE TITLE: SMC	
Apple Inc.	DRAWING NUMBER: 051-9179 SIZE: D
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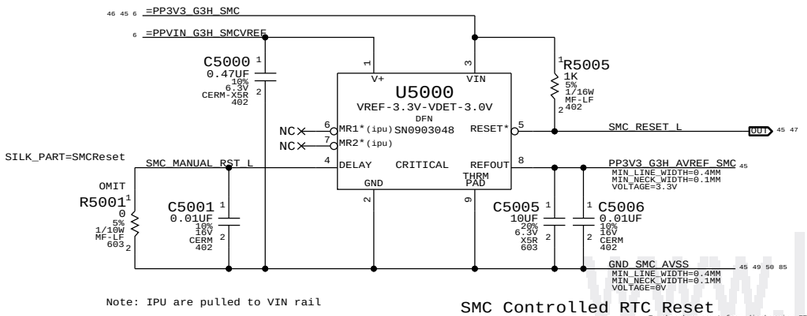
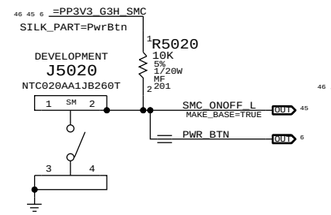
SMC Supervisor and AVREF Supply



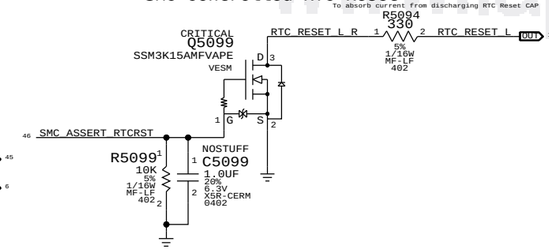
Note: IPU are pulled to VIN rail

Power Button



SMC Controlled RTC Reset

To absorb current from discharging RTC Reset CAP

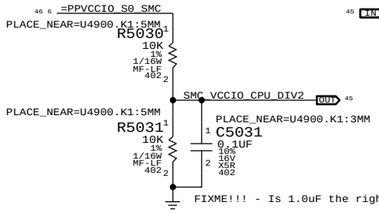


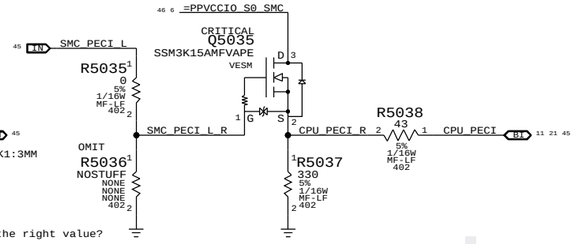
Enable TBT S4 Wake Sources

PECI Support

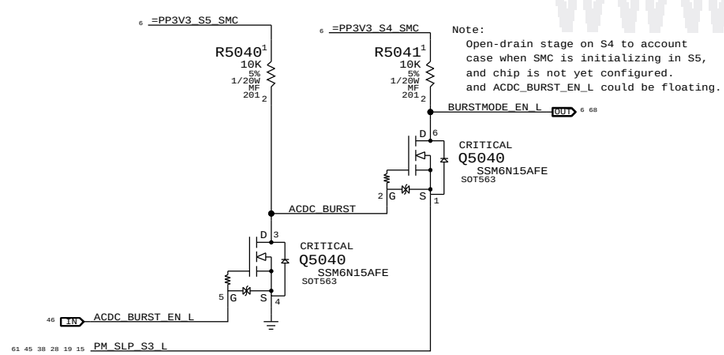
Level-shifter that allows SMC to drive PECI
Place this circuit near the Tee point to minimize reflections

Comparator Reference





AC/DC Burst Mode Enable



Note:
Open-drain stage on S4 to account
case when SMC is initializing in S5,
and chip is not yet configured.
and ACDC_BURST_EN_L could be floating.

ADC Channel Aliases

SMC_ADC0	VSNS_P12VG3H	MAKE_BASE=TRUE
SMC_ADC1	ISNS_P12VG3H	MAKE_BASE=TRUE
SMC_ADC2	VSNS_P12VS0_GPUCORE	MAKE_BASE=TRUE
SMC_ADC3	ISNS_P12VS0_GPUCORE	MAKE_BASE=TRUE
SMC_ADC6	VSNS_VDDQS3_DDR	MAKE_BASE=TRUE
SMC_ADC7	ISNS_VDDQS3_DDR	MAKE_BASE=TRUE
SMC_ADC8	VSNS_P12VS0_GPUUNCORE	MAKE_BASE=TRUE
SMC_ADC9	ISNS_P12VS0_GPUUNCORE	MAKE_BASE=TRUE
SMC_ADC10	VSNS_CPUCORE	MAKE_BASE=TRUE
SMC_ADC11	ISNS_CPUCORE	MAKE_BASE=TRUE
SMC_ADC12	VSNS_CPUAXG	MAKE_BASE=TRUE
SMC_ADC13	ISNS_CPUAXG	MAKE_BASE=TRUE
SMC_ADC14	VSNS_HDDS0	MAKE_BASE=TRUE
SMC_ADC15	ISNS_HDDS0	MAKE_BASE=TRUE
SMC_ADC16	VSNS_SSDS0	MAKE_BASE=TRUE
SMC_ADC17	ISNS_SSDS0	MAKE_BASE=TRUE

Project-specific Aliases

SMC_PH3	BDV_BKL_PWM	MAKE_BASE=TRUE
SMC_PN5	ACDC_BURST_EN_L	MAKE_BASE=TRUE
SMC_PJ3	SMC_OOB2_TX_L	MAKE_BASE=TRUE
SMC_PJ2	SMC_OOB2_RX_L	MAKE_BASE=TRUE
SMC_PP0	SMC_ACDC_ID	MAKE_BASE=TRUE
SMC_PH2	SMC_ASSERT_RTCRST	MAKE_BASE=TRUE

Unused ADC Channels

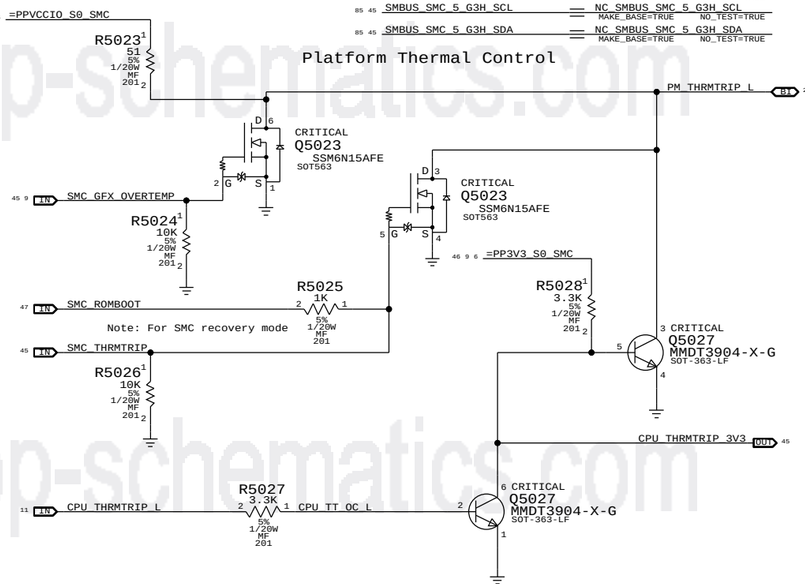
SMC_ADC4	NC_SMC_ADC4	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC5	NC_SMC_ADC5	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC18	NC_SMC_ADC18	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC19	NC_SMC_ADC19	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC20	NC_SMC_ADC20	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC21	NC_SMC_ADC21	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC22	NC_SMC_ADC22	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_ADC23	NC_SMC_ADC23	MAKE_BASE=TRUE NO_TEST=TRUE

Unused Project-specific

SMC_PN2	NC_SMC_PN2	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PN3	NC_SMC_PN3	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PN4	NC_SMC_PN4	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PN6	NC_SMC_PN6	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PN7	NC_SMC_PN7	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PP5	NC_SMC_PP5	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PP6	NC_SMC_PP6	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PP7	NC_SMC_PP7	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PME_S4_DARK_L	NC_SMC_PME_S4_DARK_L	MAKE_BASE=TRUE NO_TEST=TRUE
SMC_PH7	TP_SMC_PH7	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_5_G3H_SCL	NC_SMBUS_SMC_5_G3H_SCL	MAKE_BASE=TRUE NO_TEST=TRUE
SMBUS_SMC_5_G3H_SDA	NC_SMBUS_SMC_5_G3H_SDA	MAKE_BASE=TRUE NO_TEST=TRUE

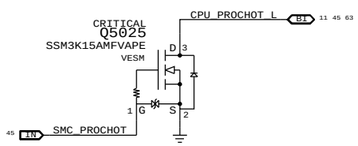
TP for access if ZPB re-intstated

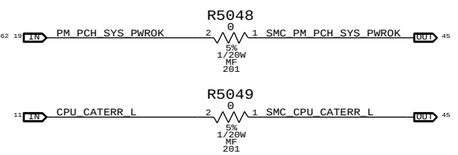
Platform Thermal Control



PROCHOT Support

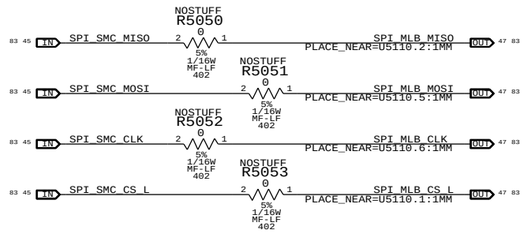
Level-shifter that allows SMC to drive PROCHOT





SMC SPI Support

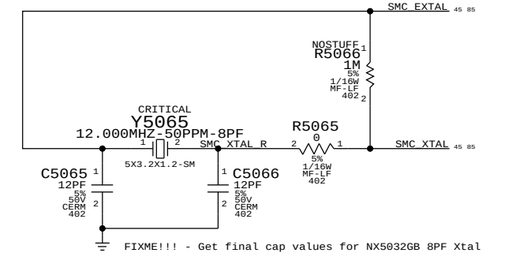
Series R are NOSTUFF until topology of 2 SPI masters is verified



SMC 32KHz Clock

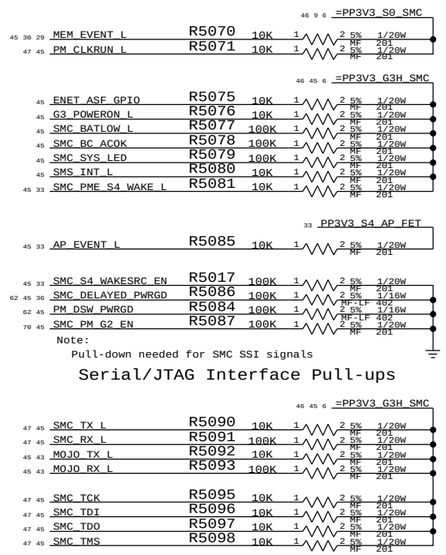
SMC Crystal

NOTE: SMC team wants 12MHz for this Xtal



FIXME!!! - Get final cap values for NX5032GB 8PF Xtal

Arch Pull Up/Down



SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

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Apple Inc.

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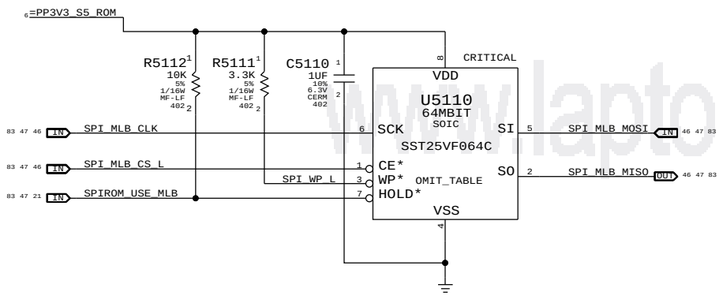
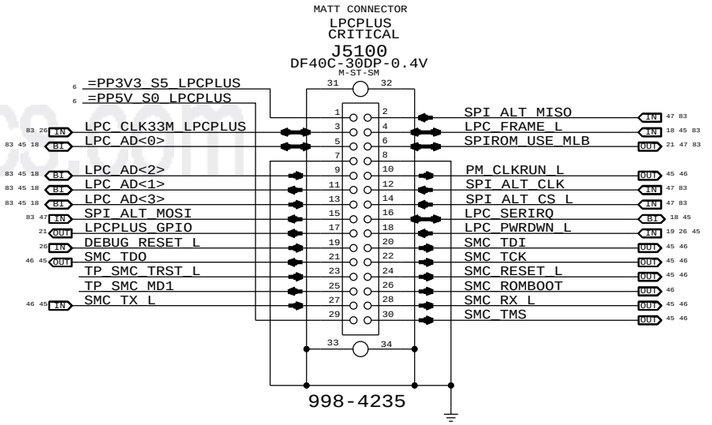
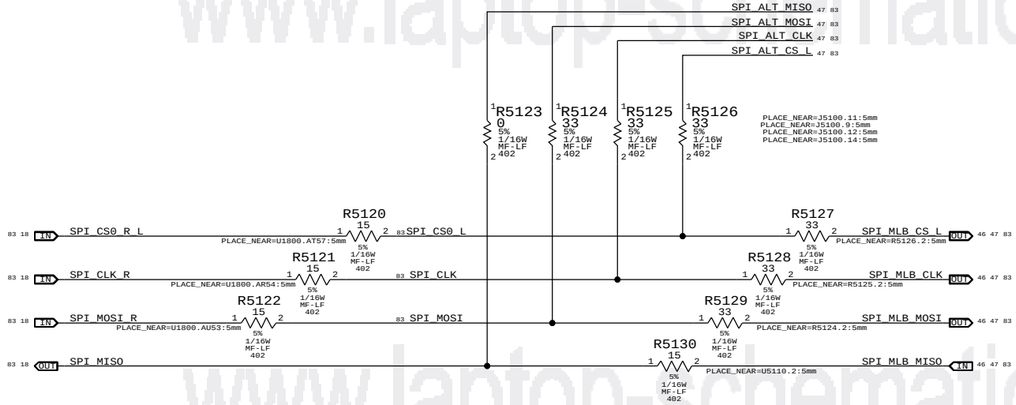
SPI BootROM



LPC+SPI Connector



SPI Series Termination



SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE: SPI and Debug Connector

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Line Legend

- Master
- Slave
- Mux

PCH (SMBus)

48 6 =PP3V3_S0_SMBUS

R5260 2.2K 5% 1/16W MF-LF 402
R5261 2.2K 5% 1/16W MF-LF 402

18 85	SMBUS_PCH_CLK (MAKE_BASE=TRUE)	
18 85	SMBUS_PCH_DATA (MAKE_BASE=TRUE)	

Memory Channel A

J3100 A/B

=I2C_SODIMMA_SCL	29	DIMM 0: 0xA0 Write 0xA1 Read
=I2C_SODIMMA_SDA	29	DIMM 2: 0xA2 Write 0xA3 Read

Memory Channel B

J3200 A/B

=I2C_SODIMMB_SCL	30	DIMM 1: 0xA4 Write 0xA5 Read
=I2C_SODIMMB_SDA	30	DIMM 3: 0xA6 Write 0xA7 Read

VRef DAC

U3400

=I2C_VREFDACS_SCL	32	0x98 Write 0x99 Read
=I2C_VREFDACS_SDA	32	

Vref Control

U3401

=I2C_PCA9557D_SCL	32	0x30 Write 0x31 Read
=I2C_PCA9557D_SDA	32	

Backlight Control

U9700

=I2C_BKLT_SCL	77	0x22 Write 0x?? Read
=I2C_BKLT_SDA	77	

CHS

U6550

=I2C_CHS_SCL	57	0x76 Write 0x77 Read
=I2C_CHS_SDA	57	

Mikey

U6551

=I2C_MIKEY_SCL	57	0x72 Write 0x73 Read
=I2C_MIKEY_SDA	57	

XDP

J2550

=SMBUS_XDP_SCL	25	0x94 Write 0x95 Read
=SMBUS_XDP_SDA	25	

TBT

U3600

=I2C_TBTRTR_SCL	34 89	0x?? Write 0x?? Read
=I2C_TBTRTR_SDA	34 89	

NOSTUFF R5262 0 5% 1/16W MF-LF 402
NOSTUFF R5263 0 5% 1/16W MF-LF 402

SMC (SMBus 3)

U4900

=SMBUS_PCH_SCL	48	
=SMBUS_PCH_SDA	48	

SMC (SMBus 0)

6 =PP3V3_S0_SMBUS_SMC_0

R5200 2.2K 5% 1/16W MF-LF 402
R5201 2.2K 5% 1/16W MF-LF 402

U4900

SMB_0_S0_CLK (MAKE_BASE=TRUE)	85 45 SMBUS_SMC_0_S0_SCL	
SMB_0_S0_DATA (MAKE_BASE=TRUE)	85 45 SMBUS_SMC_0_S0_SDA	

GPU Die Temp

U8000

GPU_SMB_CLK_R		0x9E Write 0x9F Read
GPU_SMB_DAT_R		

Temp Sensors (Prod)

U5500

=SMB_SNS1_SCL	51	EMC1414 (Prod): 0x98 Write 0x99 Read
=SMB_SNS1_SDA	51	

PCH (SML 1)

U1800

SML_PCH_1_CLK	18	0x88 Write 0x89 Read
SML_PCH_1_DATA	18	

LCD Temp IRemote (Dev4Now)

U5590

=SMB_SNS3_SCL	51	TMP006 (Prod): 0x8A Write 0x8B Read
=SMB_SNS3_SDA	51	

SMC (SMBus 1)

6 =PP3V3_S0_SMBUS_SMC_1

R5210 4.7K 5% 1/16W MF-LF 402
R5211 4.7K 5% 1/16W MF-LF 402

U4900

SMB_1_S0_CLK (MAKE_BASE=TRUE)	85 45 SMBUS_SMC_1_S0_SCL	
SMB_1_S0_DATA (MAKE_BASE=TRUE)	85 45 SMBUS_SMC_1_S0_SDA	

Temp Sensors (Dev)

U5550

=SMB_SNS2_SCL	51	TMP423B (Dev): 0x9A Write 0x9B Read
=SMB_SNS2_SDA	51	

Display TCon

J9100

SMB_DP_TCON_SLA_SCL	72	TMB421: 0x5E Write 0x5F Read
SMB_DP_TCON_SLA_SDA	72	Panel/Vendor ID: 0x1A Write 0x1B Read

SMC (SMBus 2)

6 =PP3V3_S4_SMBUS_SMC_2

R5220 4.7K 5% 1/16W MF-LF 402
R5221 4.7K 5% 1/16W MF-LF 402

U4900

SMB_2_S4_CLK (MAKE_BASE=TRUE)	85 45 SMBUS_SMC_2_S4_SCL	
SMB_2_S4_DATA (MAKE_BASE=TRUE)	85 45 SMBUS_SMC_2_S4_SDA	

ALS

J3510

=SMB_ALS_SCL	40	0x52 Write 0x53 Read
=SMB_ALS_SDA	40	

SMC (SMBus 3)

6 =PP3V3_S0_SMBUS_SMC_3

R5230 4.7K 5% 1/16W MF-LF 402
R5231 4.7K 5% 1/16W MF-LF 402

U4900

SMB_3_CLK (MAKE_BASE=TRUE)	85 45 SMBUS_SMC_3_SCL	
SMB_3_DATA (MAKE_BASE=TRUE)	85 45 SMBUS_SMC_3_SDA	

SMC multi-master experiment

PCH (SML 1)

U1800

R5264 8.2K 5% 1/16W MF-LF 402
R5265 8.2K 5% 1/16W MF-LF 402

18 85	SML_PCH_0_CLK (MAKE_BASE=TRUE)	
18 85	SML_PCH_0_DATA (MAKE_BASE=TRUE)	

Unused PCH SM Link

Display TCon

74 72 9 6 =PP3V3_S0_DP

K60 Panel Requires these pullups - Can NOSTUFF when we get K70 panels

R5290 2.2K 5% 1/16W MF-LF 402
R5291 2.2K 5% 1/16W MF-LF 402

J9100

72 85	SMB_DP_TCON_SCL (MAKE_BASE=TRUE)	
72 85	SMB_DP_TCON_SDA (MAKE_BASE=TRUE)	

TCon has 4.7K pullup

BLC Control from TCon

U9700

=SMB_DP_BLC_SCL	77	0x?? Write 0x??+01 Read
=SMB_DP_BLC_SDA	77	

SYNC_MASTER	D7 MLB
SYNC_DATE	01/19/2012
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	Apple Inc.
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BRANCH	
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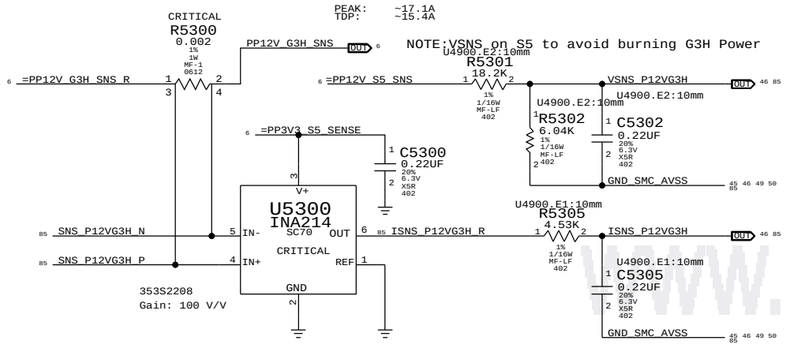
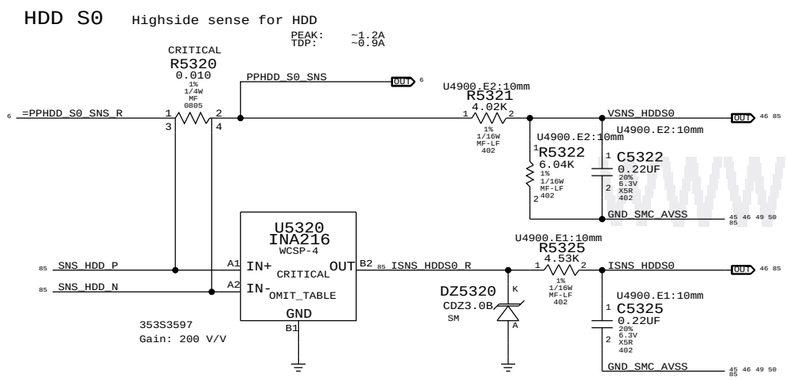
12V G3H AC/DC lowside sense (System total)

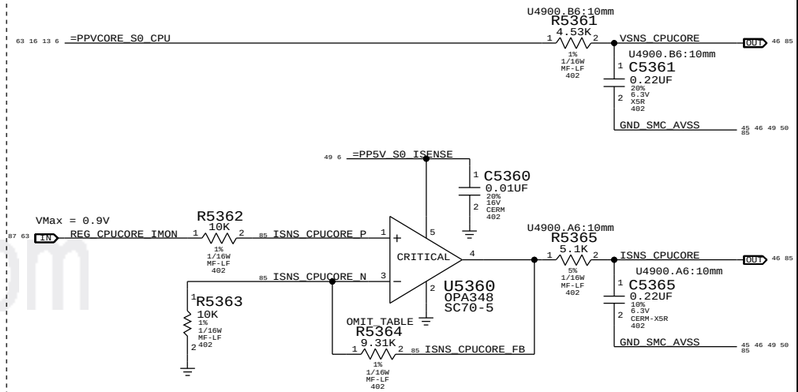


HDD S0 Highside sense for HDD



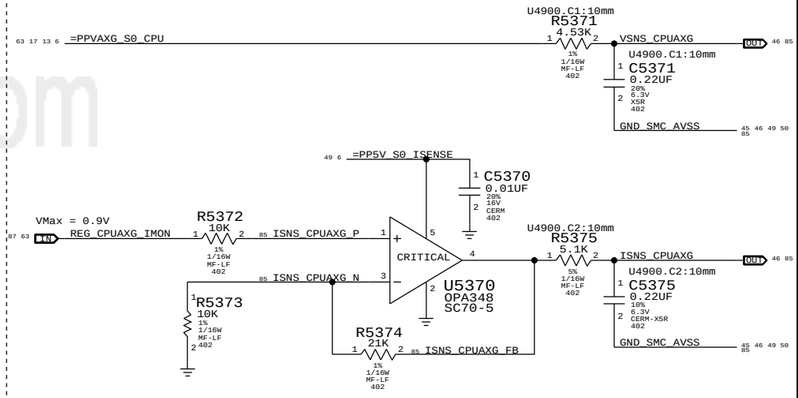
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S3597	1	INA216A4 200V/V Current Sense	U5320	

CPU Core Voltage sense and IMON amp (VC0C, IC0C)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0312	1	RES,MTL FILM,1/16W,9.31K,0402	R5364	SNS_CPUCORE:3PHASE
114S0345	1	RES,MTL FILM,1/16W,21K,0402	R5364	SNS_CPUCORE:4PHASE

CPU AXG Voltage sense and IMON amp (VC0G, IC0G)



SYNC_MASTER=D7_MLB SYNC_DATE=01/10/2012

PAGE TITLE
I and V Sense(Production)

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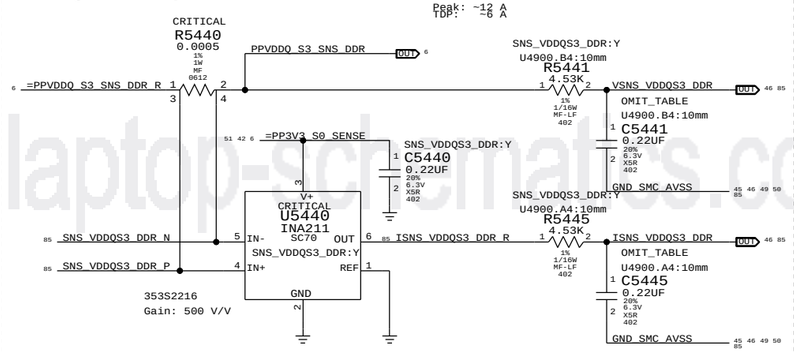
VDDQ S3

VDDQ lowside sense for SO-DIMM modules

Peak: ~12 A
TDP: ~6 A

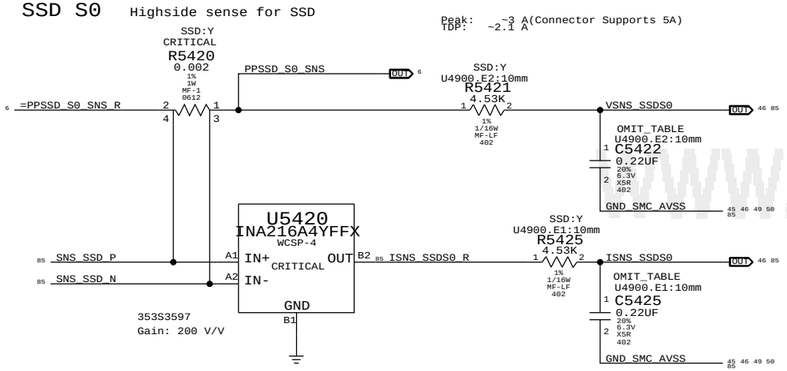


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP,0.22UF,402	C5441,C5445	SNS_VDDQS3_DDR:Y
116S0004	2	RES,0 OHM,402	C5441,C5445	SNS_VDDQS3_DDR:N

SSD S0

Highside sense for SSD

Peak: ~3 A(Connector Supports 5A)
TDP: ~2.1 A



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP,0.22UF,402	C5422,C5425	SSD:Y
116S0004	2	RES,0 OHM,402	C5422,C5425	SSD:N

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE
I and V Sense(Development)

Apple Inc.

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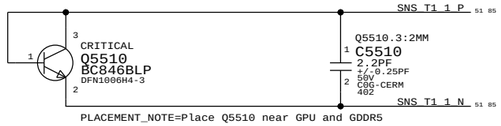
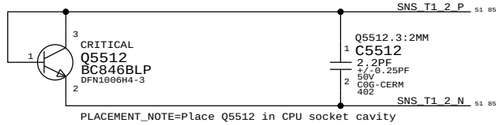
Temperature Sensor T1: Production Bound

GPU Proximity



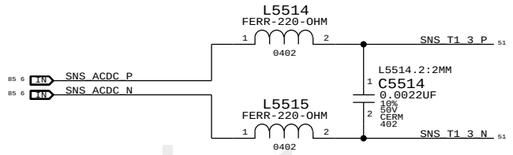
PLACEMENT_NOTE=Place Q5510 near GPU and GDDR5

CPU Proximity

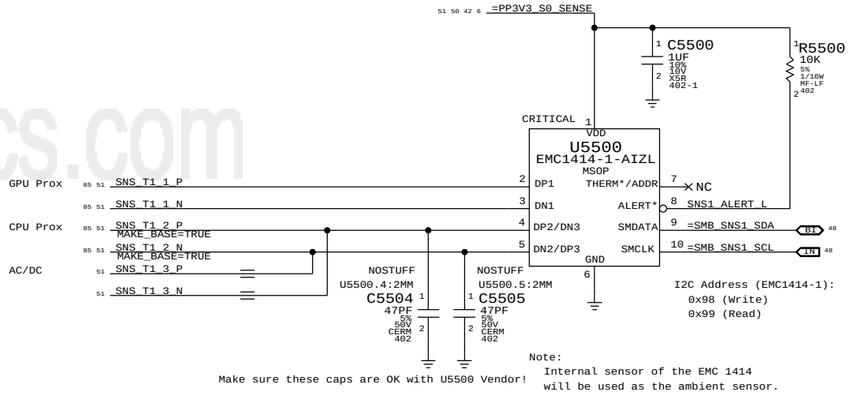


PLACEMENT_NOTE=Place Q5512 in CPU socket cavity

AC/DC Diode on supply

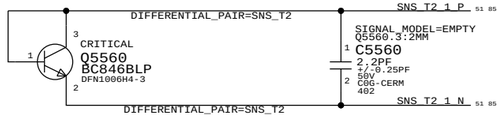


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode



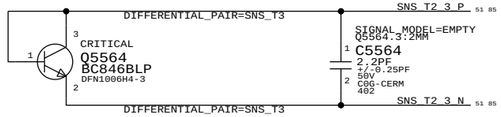
Temperature Sensor T2: Development Only

SO-DIMM Proximity



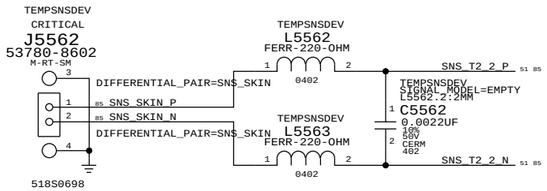
PLACEMENT_NOTE=Place Q5550 near SO-DIMM connectors

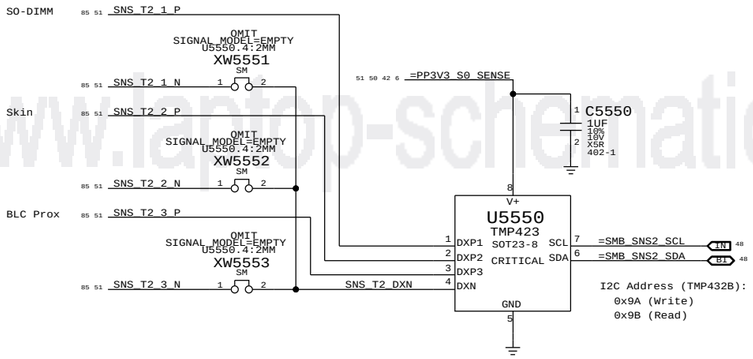
BLC Proximity



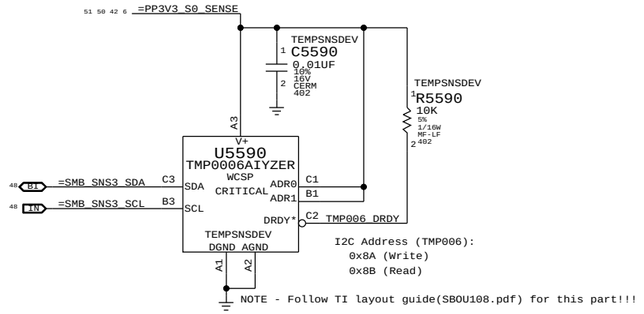
PLACEMENT_NOTE=Place Q5554 near BLC controller

Skin





Temperature Sensor T3: LCD Remote Sensor(Dev4Now)



SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

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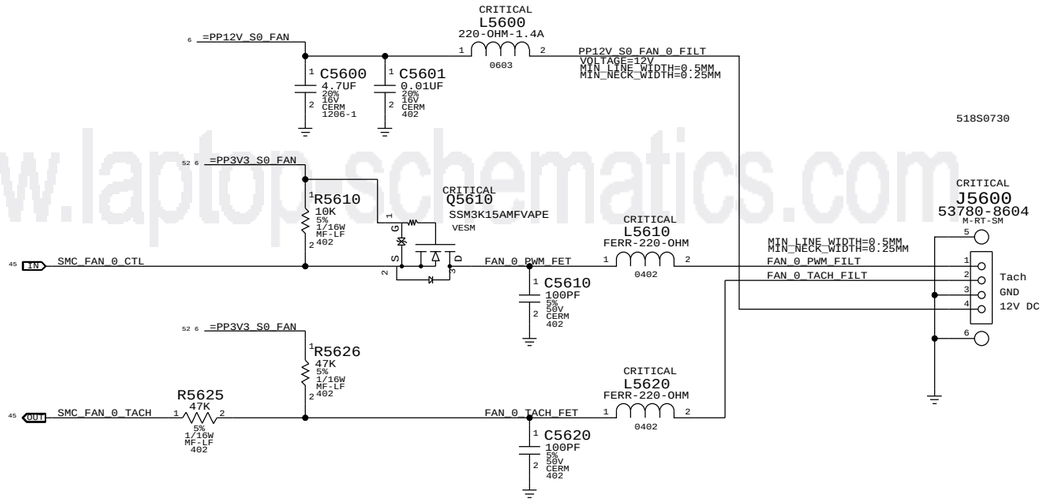
SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q5610 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q5610 is at common and the SMC sinks current when Q5610 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.



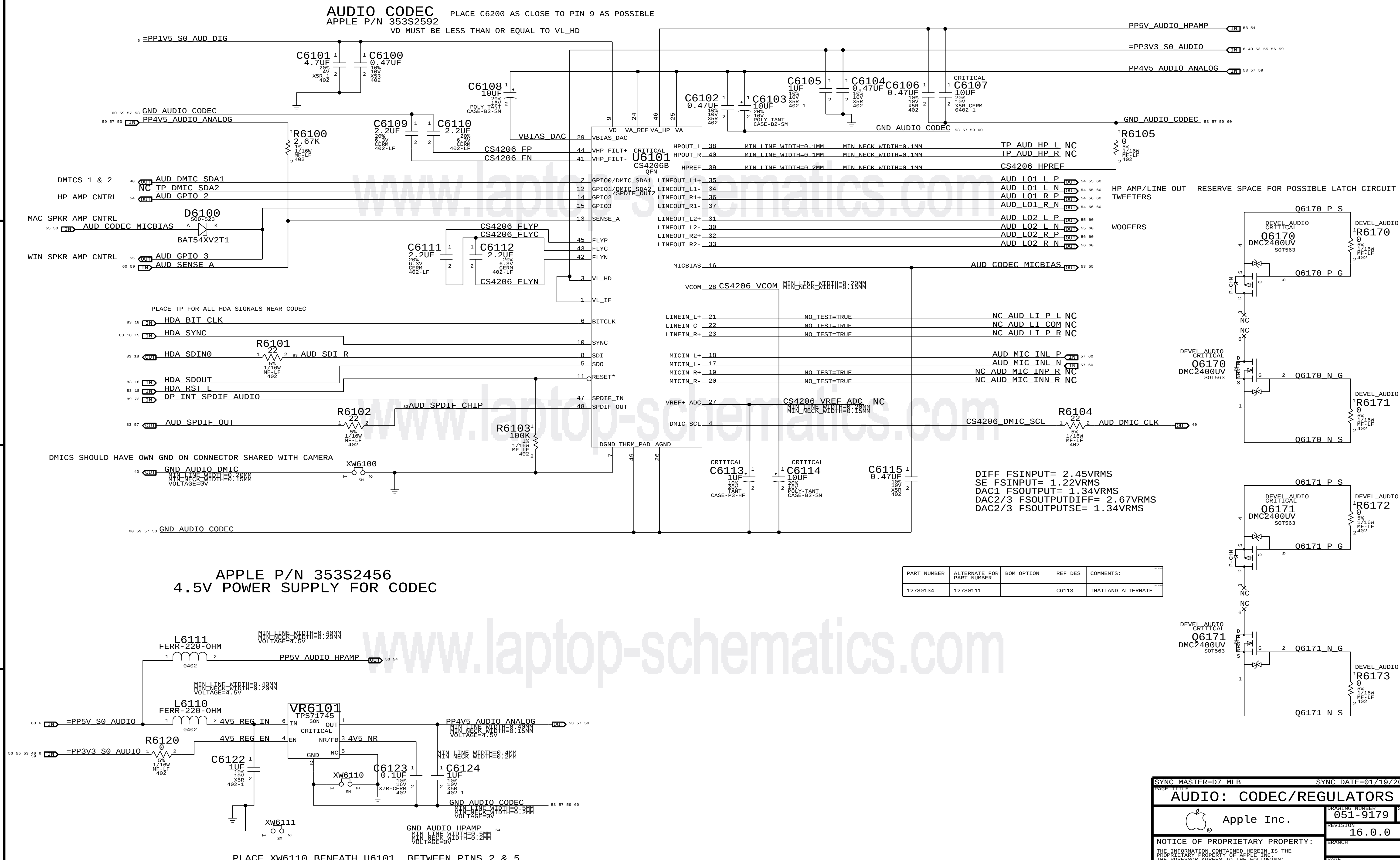
SMC Fan 1 (Unused)

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE: System Fan

Apple Inc.

DRAWING NUMBER: 051-9179 SIZE: D
REVISION: 16.0.0
BRANCH:
PAGE: 56 OF 113
SHEET: 52 OF 90



AUDIO CODEC
APPLE P/N 353S2592
PLACE C6200 AS CLOSE TO PIN 9 AS POSSIBLE
VD MUST BE LESS THAN OR EQUAL TO VL_HD
=PP1V5_S0_AUD_DIG
C6101 4.7UF 20% 4V X5R-1 402
C6100 0.47UF 10% 10V X5R 402
C6108 10UF 20% 16V POLY-TANT CASE-B2-SM
GND_AUDIO_CODEC
PP4V5_AUDIO_ANALOG
R6100 2.67K 1% 1/16W MF-LF 402
C6109 2.2UF 20% 6.3V CERM 402-LF
C6110 2.2UF 20% 6.3V CERM 402-LF
VBIAS_DAC
CS4206_FP
CS4206_FN
DMICS 1 & 2
AUD_DMIC_SDA1
TP_DMIC_SDA2
HP AMP CNTRL
AUD_GPIO_2
MAC SPKR AMP CNTRL
AUD_CODEC_MICBIAS
D6100 SOD-523
BAT54XV2T1
WIN SPKR AMP CNTRL
AUD_GPIO_3
AUD_SENSE_A
CS4206_FLYP
CS4206_FLYC
CS4206_FLYN
C6111 2.2UF 20% 6.3V CERM 402-LF
C6112 2.2UF 20% 6.3V CERM 402-LF
U6101 CS4206B QFN CRITICAL
VD VA_REF VA_HP VA
VBIAS_DAC VHP_FILT+ VHP_FILT- GPIO0/DMIC_SDA1 GPIO1/DMIC_SDA2 /SPDIF_OUT2 GPIO2 GPIO3 SENSE_A FLYP FLYC FLYN VL_HD VL_IF BITCLK SYNC SDI SDO RESET* SPDIF_IN SPDIF_OUT
HPOUT_L HPOUT_R HPREF LINEOUT_L1+ LINEOUT_L1- LINEOUT_R1+ LINEOUT_R1- LINEOUT_L2+ LINEOUT_L2- LINEOUT_R2+ LINEOUT_R2- MICBIAS VCOM LINEIN_L+ LINEIN_C- LINEIN_R+ MICIN_L+ MICIN_L- MICIN_R+ MICIN_R- VREF+_ADC DMIC_SCL
DGND THRM_PAD AGND
PLACE TP FOR ALL HDA SIGNALS NEAR CODEC
HDA_BIT_CLK
HDA_SYNC
HDA_SDIN0
R6101 22 5% 1/16W MF-LF 402
AUD_SDI_R
HDA_SDOUT
HDA_RST_L
DP_INT_SPDIF_AUDIO
AUD_SPDIF_CHIP
AUD_SPDIF_OUT
R6102 22 5% 1/16W MF-LF 402
R6103 100K 1% 1/16W MF-LF 402
DMICS SHOULD HAVE OWN GND ON CONNECTOR SHARED WITH CAMERA
XW6100 SM
GND_AUDIO_DMIC
MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM VOLTAGE=0V
PP5V_AUDIO_HPAMP
=PP3V3_S0_AUDIO
PP4V5_AUDIO_ANALOG
C6102 0.47UF 10% 10V X5R 402
C6103 10UF 20% 16V POLY-TANT CASE-B2-SM
C6105 1UF 10% 10V X5R 402-1
C6104 0.47UF 10% 10V X5R 402
C6106 0.47UF 10% 10V X5R 402
C6107 CRITICAL 10UF 20% 10V X5R-CERM 0402-1
R6105 0 5% 1/16W MF-LF 402
MIN_LINE_WIDTH=0.1MM MIN_NECK_WIDTH=0.1MM
MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM
TP_AUD_HP_L NC
TP_AUD_HP_R NC
CS4206_HPREF
AUD_LO1_L_P
AUD_LO1_L_N
AUD_LO1_R_P
AUD_LO1_R_N
HP AMP/LINE OUT TWEETERS
AUD_LO2_L_P
AUD_LO2_L_N
AUD_LO2_R_P
AUD_LO2_R_N
WOOFERS
AUD_CODEC_MICBIAS
CS4206_VCOM
MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM
NO_TEST=TRUE
NC_AUD_LI_P_L NC
NC_AUD_LI_COM NC
NC_AUD_LI_P_R NC
AUD_MIC_INL_P
AUD_MIC_INL_N
NC_AUD_MIC_INP_R NC
NC_AUD_MIC_INN_R NC
CS4206_VREF_ADC NC
CS4206_DMIC_SCL
R6104 22 5% 1/16W MF-LF 402
AUD_DMIC_CLK
C6113 CRITICAL 1UF 10% 20V TANT CASE-P3-HF
C6114 CRITICAL 10UF 20% 16V POLY-TANT CASE-B2-SM
C6115 0.47UF 10% 10V X5R 402
DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS
RESERVE SPACE FOR POSSIBLE LATCH CIRCUIT
Q6170_P_S
Q6170 DEVEL_AUDIO CRITICAL DMC2400UV SOT563
R6170 DEVEL_AUDIO 0 5% 1/16W MF-LF 402
Q6170_P_G
Q6170_N_G
R6171 DEVEL_AUDIO 0 5% 1/16W MF-LF 402
Q6170_N_S
Q6171_P_S
Q6171 DEVEL_AUDIO CRITICAL DMC2400UV SOT563
R6172 DEVEL_AUDIO 0 5% 1/16W MF-LF 402
Q6171_P_G
Q6171_N_G
R6173 DEVEL_AUDIO 0 5% 1/16W MF-LF 402
Q6171_N_S
P-CHN
N-CHN
NC
APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC
L6111 FERR-220-OHM 0402
MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM VOLTAGE=4.5V
PP5V_AUDIO_HPAMP
L6110 FERR-220-OHM 0402
=PP5V_S0_AUDIO
=PP3V3_S0_AUDIO
R6120 0 5% 1/16W MF-LF 402
4V5_REG_IN
4V5_REG_EN
VR6101 TPS71745 SON CRITICAL
IN OUT EN NR/FB GND NC
4V5_NR
PP4V5_AUDIO_ANALOG
MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.15MM VOLTAGE=4.5V
MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM
C6122 1UF 10% 10V X5R 402-1
C6123 0.1UF 10% 16V X7R-CERM 402
C6124 1UF 10% 10V X5R 402-1
XW6110 SM
XW6111 SM
GND_AUDIO_CODEC
MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V
GND_AUDIO_HPAMP
MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V
PLACE XW6110 BENEATH U6101, BETWEEN PINS 2 & 5

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
127S0134	127S0111		C6113	THAILAND ALTERNATE

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE
AUDIO: CODEC/REGULATORS

Apple Inc.

DRAWING NUMBER 051-9179 SIZE D

REVISION 16.0.0

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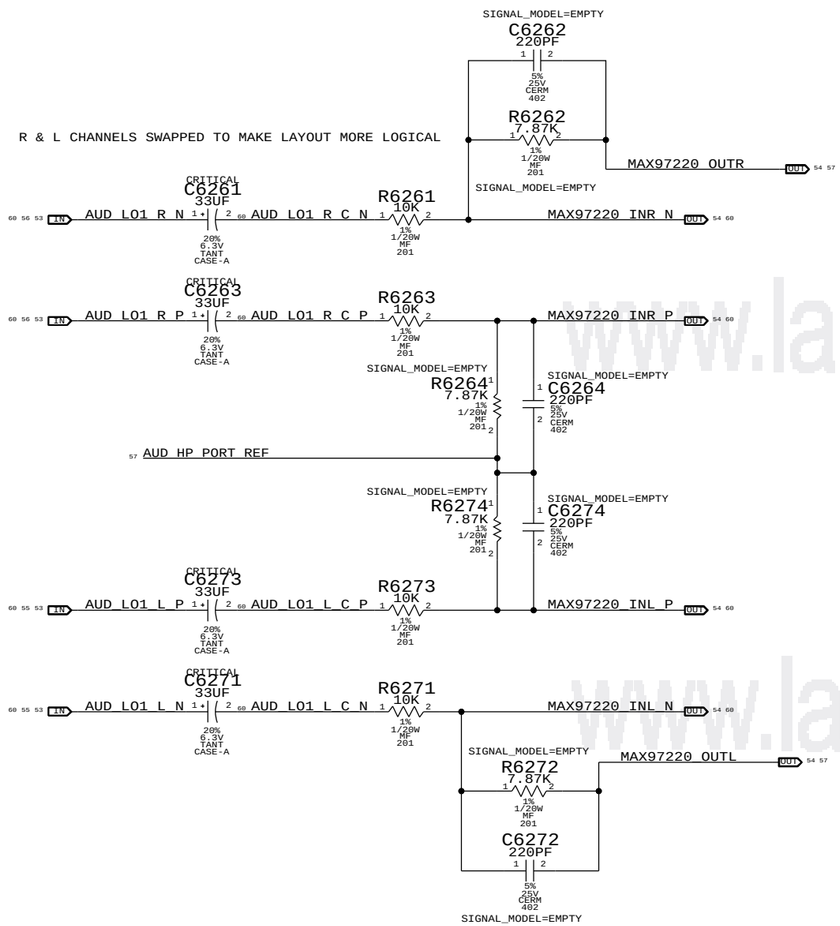

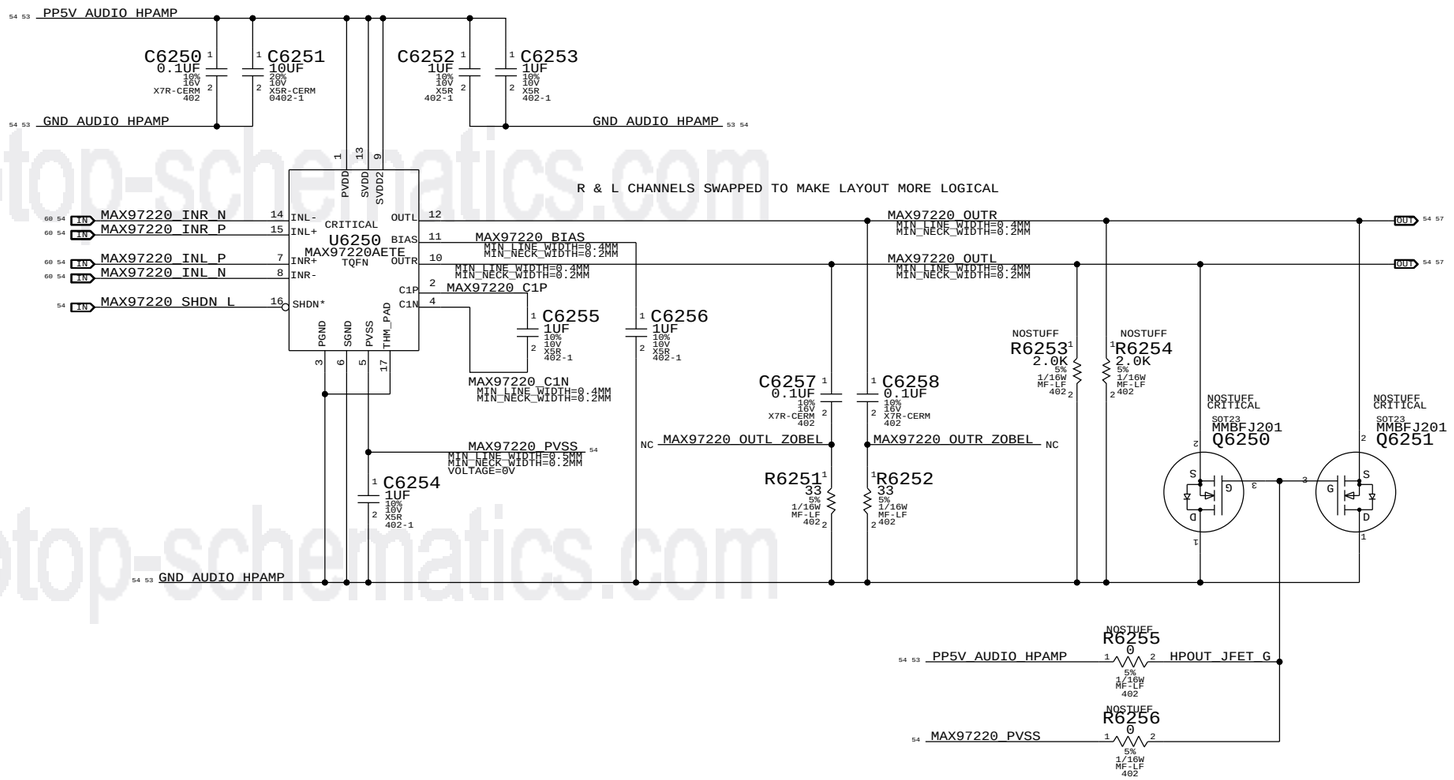

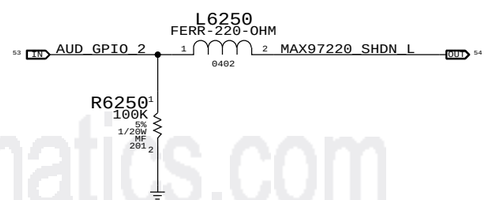

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
127S0135	127S0120		C6261	THAILAND ALTERNATE
127S0135	127S0120		C6263	THAILAND ALTERNATE
127S0135	127S0120		C6271	THAILAND ALTERNATE
127S0135	127S0120		C6273	THAILAND ALTERNATE

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE
AUDIO: HEADPHONE AMP

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LEFT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~18 HZ (0.22 UF)

=PP12V_S0_AUDIO_SPKRAMP

C6300 10UF 10% 25V X5R 805
C6301 10UF 10% 25V X5R 805
C6302 0.1UF 10% 25V X5R 402
C6303 1UF 10% 25V X5R 603-1
C6304 0.1UF 10% 25V X5R 402
C6305 1UF 10% 25V X5R 603-1
CRITICAL C6306 470UF 20% 16V POLY SM

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

L6303 FERR-1000-OHM 0402 — AUD_LO1_L_N — AUD_LAMP_RINC_P — C6308 4700PF 5% 50V NPO-C0G 805 — AUD_LAMP_RIN_P
L6302 FERR-1000-OHM 0402 — AUD_LO1_L_P — AUD_LAMP_RINC_N — C6309 4700PF 5% 50V NPO-C0G 805 — AUD_LAMP_RIN_N
L6300 FERR-1000-OHM 0402 — AUD_LO2_L_N — AUD_LAMP_LINC_P — C6310 0.22UF 10% 16V CERM 402 — AUD_LAMP_LIN_P
L6301 FERR-1000-OHM 0402 — AUD_LO2_L_P — AUD_LAMP_LINC_N — C6311 0.22UF 10% 16V CERM 402 — AUD_LAMP_LIN_N

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

=PP3V3_S0_AUDIO

PVDD (34, 35, 36, 37)

CRITICAL U6300 SSM3302 LFCSP

20	INR+	
19	INR-	
22	STDNR*	AUD_SPKRAMP_MAC_SHDN_L
16	MONO	AUD_LAMP_MONO
9	STDNL*	AUD_SPKRAMP_WIN_SHDN_L
11	INL+	
12	INL-	
21	GAIN	AUD_LAMP_GAIN
8	VREG/AVDD	AUD_LAMP_AVDD (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM, VOLTAGE=5V)
23	REGEN	
17	THERM	TP_AUD_LAMP_THERM — NC
30	BOOTR+	C6313 0.22UF 20% 25V X5R 603 — AUD_LAMP_BOOTRP (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
28, 29	OUTR+	AUD_LAMP_OUTPR (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
26, 27	OUTR-	AUD_LAMP_OUTNR (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
25	BOOTR-	C6314 0.22UF 20% 25V X5R 603 — AUD_LAMP_BOOTRN (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
10	EDGE	AUD_LAMP_EDGE
1	BOOTL+	C6315 0.22UF 20% 25V X5R 603 — AUD_LAMP_BOOTLP (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
2, 3	OUTL+	AUD_LAMP_OUTPL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
4, 5	OUTL-	AUD_LAMP_OUTNL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
6	BOOTL-	C6316 0.22UF 20% 25V X5R 603 — AUD_LAMP_BOOTLN (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
18	NC	NC
13	NC	NC
14	NC	NC
15	NC	NC
7, 24, 41	AGND	
31, 32, 33, 38, 39, 40	PGND	

WOOFERS & TWEETERS ON UNDER MAC OS
ONLY WOOFERS ON UNDER WINDOWS

C6317 2.2UF 20% 10V X5R-CERM 402

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

AUD_LAMP_OUTPR — L6305 CRITICAL 110-OHM-3A DLY5ATN111SQ2 — AUD_SPKR_LTWT_OUT_P — C6323 CRITICAL 1000PF 5% 25V NP0-C0G 402 — AUD_SPKR_LTWT_OUT_N
AUD_LAMP_OUTNR

AUD_LAMP_OUTPL — L6307 CRITICAL 110-OHM-3A DLY5ATN111SQ2 — AUD_SPKR_LWFR_OUT_N — C6324 CRITICAL 1000PF 5% 25V NP0-C0G 402 — AUD_SPKR_LWFR_OUT_P
AUD_LAMP_OUTNL

SIGNAL_MODEL=EMPTY

C6320 CRITICAL 1000PF 5% 25V NP0-C0G 402
C6322 CRITICAL 1000PF 5% 25V NP0-C0G 402
C6319 CRITICAL 1000PF 5% 25V NP0-C0G 402
C6321 CRITICAL 1000PF 5% 25V NP0-C0G 402

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

L6308 FERR-1000-OHM 0402 — AUD_CODEC_MICBIAS — AUD_SPKRAMP_MAC_SHDN_L
R6301 100K 5% 1/16W MF-LF 402 — NOSTUFF C6312 100PF 5% 50V CERM 402

R6308 0 5% 1/16W MF-LF 402 — AUD_GPIO_3 — AUD_SPKRAMP_WIN_SHDN_L
R6309 100K 5% 1/16W MF-LF 402 — NOSTUFF C6318 100PF 5% 50V CERM 402

EDGE RATE CONTROL

	R6304	R6305
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6306	R6307
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	NOSTUFF
+15 DB	0 OHM	NOSTUFF
+18 DB	NOSTUFF	47 KOHM
+24 DB	47 KOHM	NOSTUFF

AUD_LAMP_AVDD
R6304 0 5% 1/16W MF-LF 402 — NOSTUFF
R6306 0 5% 1/16W MF-LF 402 — NOSTUFF
AUD_LAMP_EDGE
AUD_LAMP_MONO
AUD_LAMP_GAIN
R6305 0 5% 1/16W MF-LF 402 — NOSTUFF
R6303 0 5% 1/16W MF-LF 402
R6307 0 5% 1/16W MF-LF 402 — NOSTUFF

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012
PAGE TITLE: AUDIO: LEFT SPKR AMP

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RIGHT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~18 HZ (0.22 UF)

55 6 =PP12V_S0_AUDIO_SPKRAMP

C6400 10UF 10% 25V X5R 805
C6401 10UF 10% 25V X5R 805

C6402 0.1UF 10% 25V X5R 402
C6403 1UF 10% 25V X5R 603-1
C6404 0.1UF 10% 25V X5R 402
C6405 1UF 10% 25V X5R 603-1
CRITICAL
C6406 470UF 20% 16V POLY SM

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

L6400 FERR-1000-OHM 0402
C6408 0.22UF 10% 16V CERM 402
60 53 AUD_LO2_R_N — AUD_RAMP_RINC_P — AUD_RAMP_RIN_P

L6401 FERR-1000-OHM 0402
C6409 0.22UF 10% 16V CERM 402
60 53 AUD_LO2_R_P — AUD_RAMP_RINC_N — AUD_RAMP_RIN_N

L6402 FERR-1000-OHM 0402
C6410 4700PF 5% 50V NP0-C0G 805
60 54 53 AUD_LO1_R_P — AUD_RAMP_LINC_P — AUD_RAMP_LIN_P

L6403 FERR-1000-OHM 0402
C6411 4700PF 5% 50V NP0-C0G 805
60 54 53 AUD_LO1_R_N — AUD_RAMP_LINC_N — AUD_RAMP_LIN_N

59 55 53 40 6 =PP3V3_S0_AUDIO

34 35 36 37 PVDD

CRITICAL
U6400
SSM3302
LFCSP

20	INR+	
19	INR-	
55	AUD_SPKRAMP_WIN_SHDN_L	STDNR*
56	AUD_RAMP_MONO	MONO
55	AUD_SPKRAMP_MAC_SHDN_L	STDNL*
11	INL+	
12	INL-	
56	AUD_RAMP_GAIN	GAIN
56	AUD_RAMP_AVDD (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM, VOLTAGE=5V)	VREG/AVDD
23	REGEN	

ONLY WOOFERS ON UNDER WINDOWS
WOOFERS & TWEETERS ON UNDER MAC OS

C6417 2.2UF 20% 10V X5R-CERM 402

7 24 41 AGND THRM_PAD
31 32 33 38 39 40 PGND

17	THERM	TP_AUD_RAMP_THERM NC
30	BOOTR+	C6413 0.22UF 20% 25V X5R 603 — AUD_RAMP_BOOTRP (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
28 29	OUTR+	AUD_RAMP_OUTPR (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM) OUT 56
26 27	OUTR-	AUD_RAMP_OUTNR (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM) OUT 56
25	BOOTR-	C6414 0.22UF 20% 25V X5R 603 — AUD_RAMP_BOOTRN (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
10	EDGE	AUD_RAMP_EDGE IN 56
1	BOOTL+	C6415 0.22UF 20% 25V X5R 603 — AUD_RAMP_BOOTLP (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
2 3	OUTL+	AUD_RAMP_OUTPL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
4 5	OUTL-	AUD_RAMP_OUTNL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
6	BOOTL-	C6416 0.22UF 20% 25V X5R 603 — AUD_RAMP_BOOTLN (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM)
18	NC	NC
13	NC	NC
14	NC	
15	NC	

PINS 14 & 15 ARE TEST PINS AND
SHOULD BE TIED TO GND

OUTPUT POLARITY FLIP TO
MAKE LAYOUT MORE LOGICAL

SIGNAL_MODEL=EMPTY
CRITICAL
L6405 110-OHM-3A DLY5ATN111SQ2
AUD_SPKR_RWFR_OUT_P — OUT 58 60
SIGNAL_MODEL=EMPTY CRITICAL C6423 1000PF 5% 25V NP0-C0G 402
AUD_SPKR_RWFR_OUT_N — OUT 58 60

SIGNAL_MODEL=EMPTY
CRITICAL
L6407 110-OHM-3A DLY5ATN111SQ2
AUD_SPKR_RTWT_OUT_P — OUT 58 60
SIGNAL_MODEL=EMPTY CRITICAL C6424 1000PF 5% 25V NP0-C0G 402
AUD_SPKR_RTWT_OUT_N — OUT 58 60

SIGNAL_MODEL=EMPTY — CRITICAL C6420 1000PF 5% 25V NP0-C0G 402 — CRITICAL C6422 1000PF 5% 25V NP0-C0G 402 — SIGNAL_MODEL=EMPTY
SIGNAL_MODEL=EMPTY — CRITICAL C6419 1000PF 5% 25V NP0-C0G 402 — CRITICAL C6421 1000PF 5% 25V NP0-C0G 402 — SIGNAL_MODEL=EMPTY

EDGE RATE CONTROL

	R6404	R6405
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6406	R6407
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	NOSTUFF
+15 DB	0 OHM	NOSTUFF
+18 DB	NOSTUFF	47 KOHM
+24 DB	47 KOHM	NOSTUFF

56 AUD_RAMP_AVDD

R6404 0 5% 1/16W MF-LF 402 — AUD_RAMP_EDGE OUT 56
NOSTUFF R6405 0 5% 1/16W MF-LF 402
R6403 0 5% 1/16W MF-LF 402 — AUD_RAMP_MONO OUT 56
NOSTUFF R6406 0 5% 1/16W MF-LF 402 — AUD_RAMP_GAIN OUT 56
R6407 0 5% 1/16W MF-LF 402

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012
PAGE TITLE
AUDIO: RIGHT SPKR AMP

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MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S2640

PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=10.63KHZ

MIKEY 1A
APN:353S2640
MIKEY ADDRESS: WRITE=72H, READ=73H

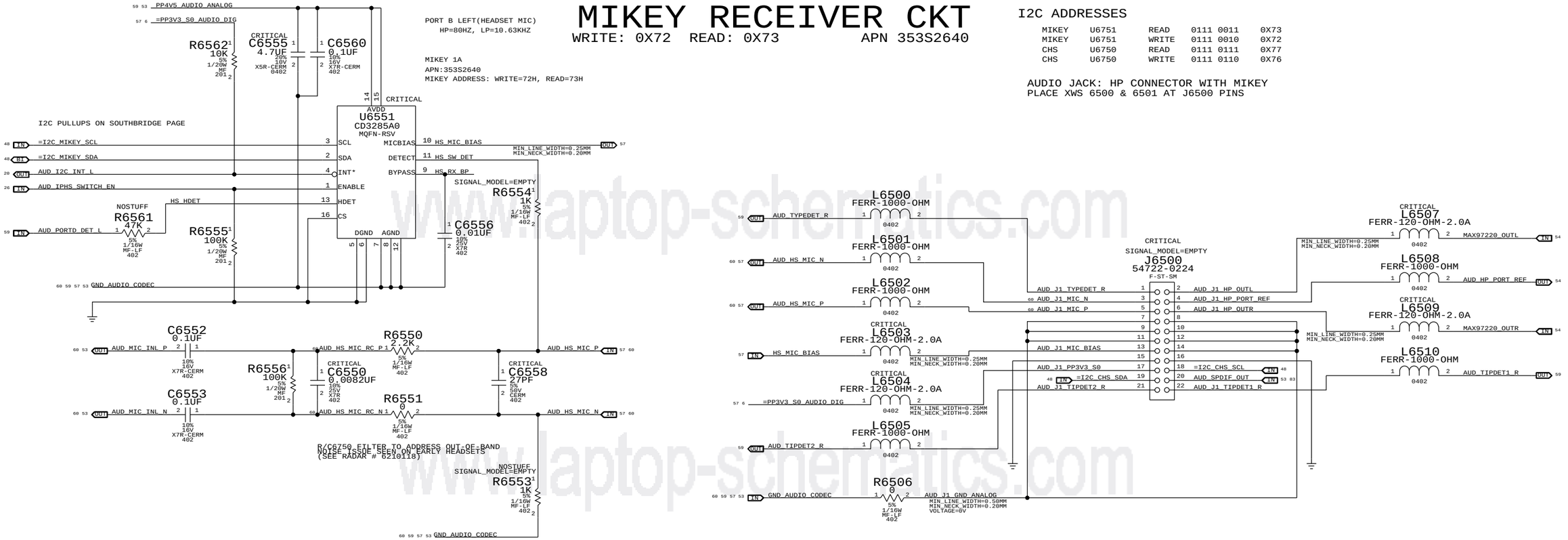
I2C ADDRESSES

MIKEY	U6751	READ	0111 0011	0X73
MIKEY	U6751	WRITE	0111 0010	0X72
CHS	U6750	READ	0111 0111	0X77
CHS	U6750	WRITE	0111 0110	0X76

AUDIO JACK: HP CONNECTOR WITH MIKEY
PLACE XWS 6500 & 6501 AT J6500 PINS

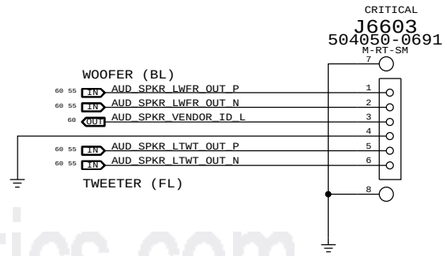
I2C PULLUPS ON SOUTHBRIDGE PAGE

R/C6750 FILTER TO ADDRESS OUT-OF-BAND NOISE ISSUE SEEN ON EARLY HEADSETS (SEE RADAR # 6210118)

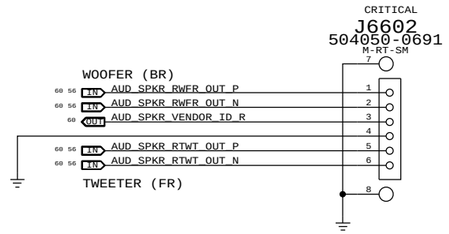


SPEAKER CABLE CONNECTORS

APPLE P/N 998-4119



APPLE P/N 998-4119



SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE
Audio: Spkr/Mic Conn.

Apple Inc.

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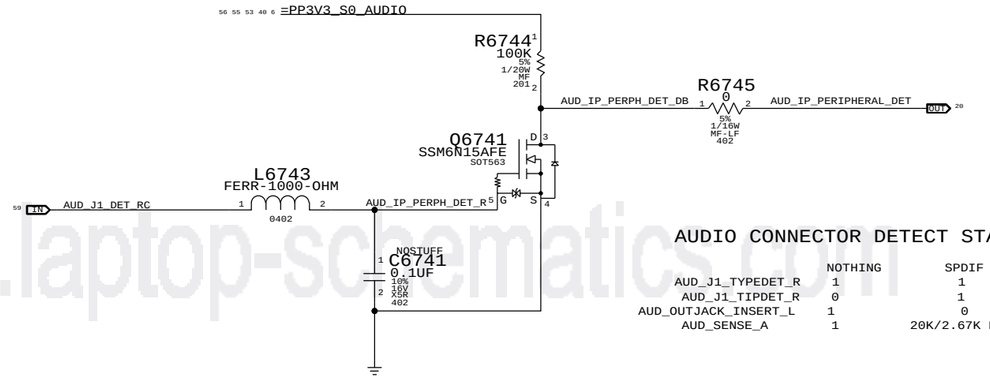
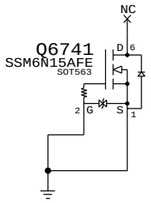
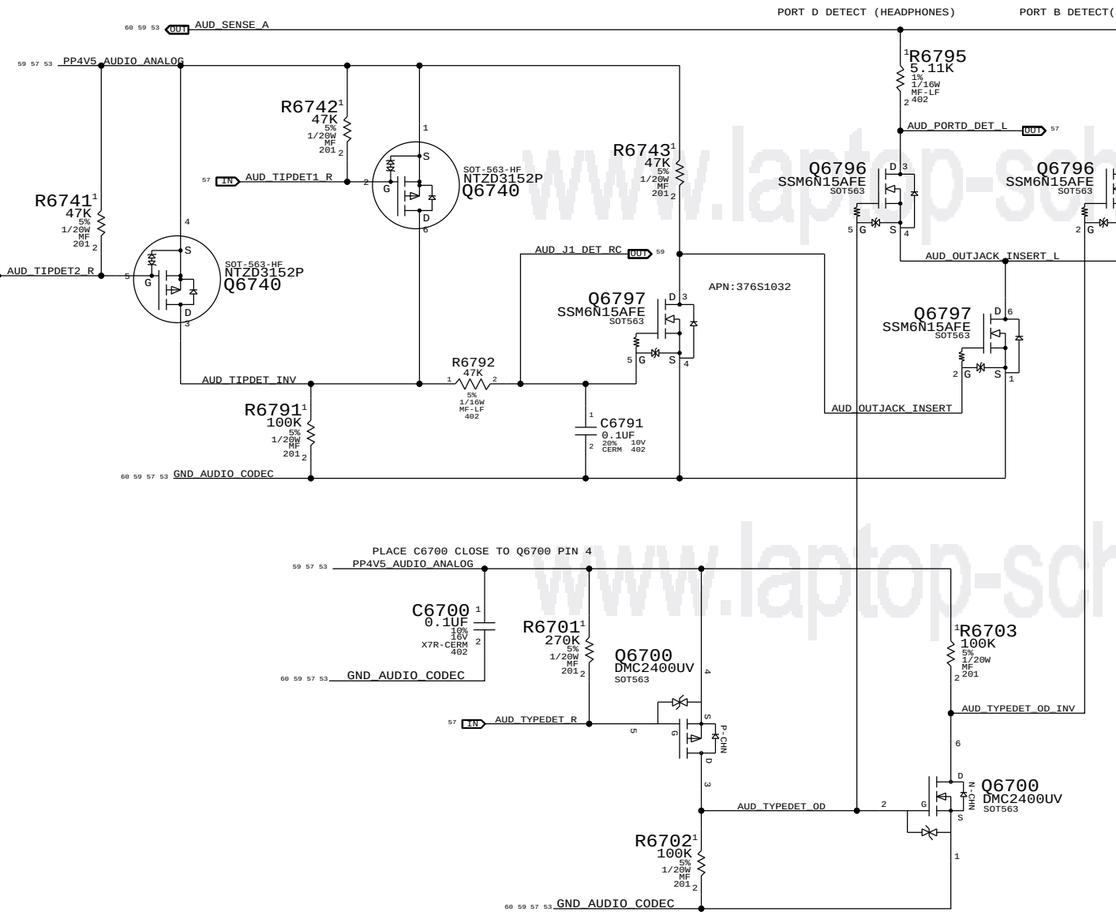
IPHS HS Detect Debounce CKT



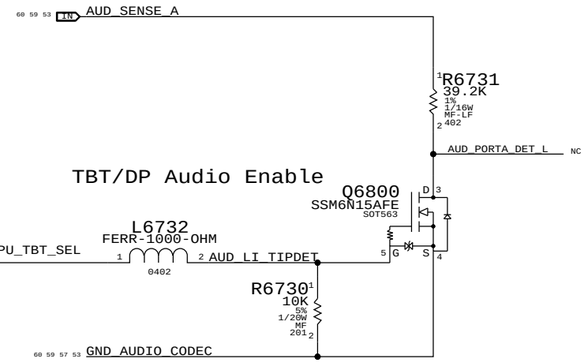
AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_J1_TYPEDET_R	1	1	0
AUD_J1_TIPDET_R	0	1	1
AUD_OUTJACK_INSERT_L	1	0	0
AUD_SENSE_A	1	20K/2.67K RDIV	39.2K/2.67K RDIV





LI Insert Detect (DETECT A)



TBT/DP Audio Enable

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE: AUDIO: Detects/Grounding

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0X0E (14,LEFT & RIGHT) 0X12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	PANTHER POINT GPIO 16	PANTHER POINT GPIO 5 (RCV0 INT) PANTHER POINT GPIO 3 (PERIPH DET)

OTHER DETECT

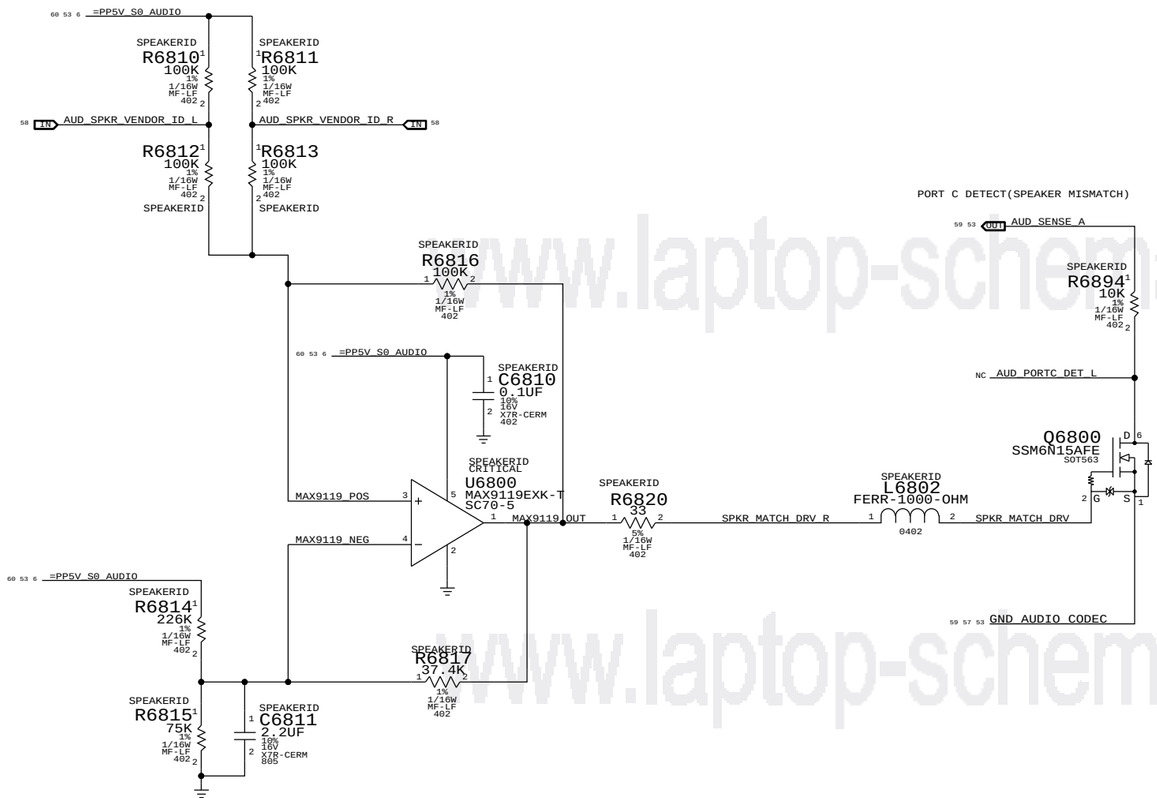
FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
1515 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	53 54 55
1516 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	53 54 55
1517 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_P	54
1518 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_N	54
1519 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	53 54 56
1520 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	53 54 56
1521 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_P	54
1522 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_N	54
1523 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	53 55
1524 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	53 55
1525 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	53 56
1526 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	53 56
1527 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_P	56
1528 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_N	56
1529 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_P	56
1530 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_N	56
1531 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_P	56
1532 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_N	56
1533 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_P	56
1534 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_N	56
1535 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_P	55
1536 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_N	55
1537 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_P	55
1538 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_N	55
1539 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_P	55
1540 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_N	55
1541 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_P	55
1542 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_N	55
1543 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INL_P	54
1544 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INL_N	54
1545 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INR_P	54
1546 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INR_N	54
1547 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	56 58
1548 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_N	56 58
1549 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	56 58
1550 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_N	56 58
1551 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	55 58
1552 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_N	55 58
1553 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	55 58
1554 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_N	55 58
1555 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	53 57
1556 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	53 57
1557 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_P	57
1558 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_N	57
1559 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_P	57
1560 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_N	57
1561 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_P	57
1562 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_N	57



SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE: AUDIO: Speaker ID

Apple Inc.

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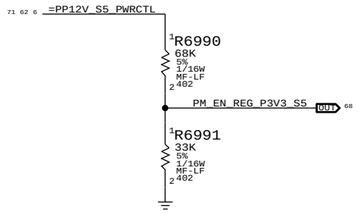
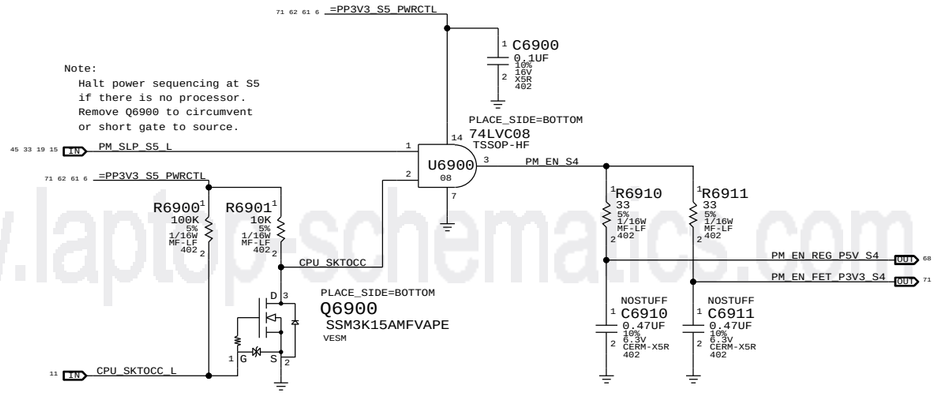
S5 Soft Enable

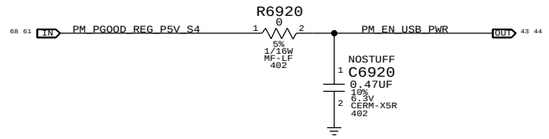


S4 Enables

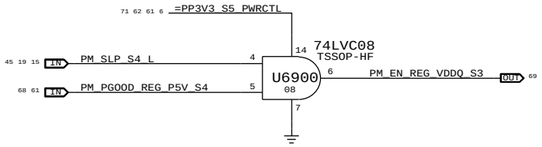


tau (RC delay, ms): 0.0 0.0

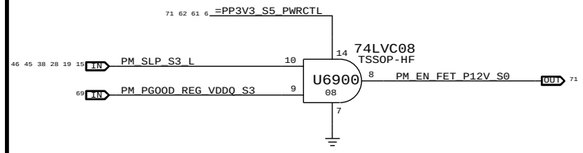
S4 USB Enable

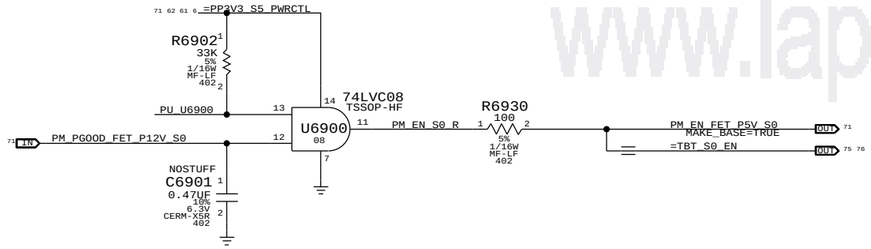


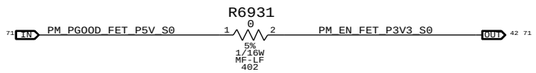
S3 VDDQ Enable



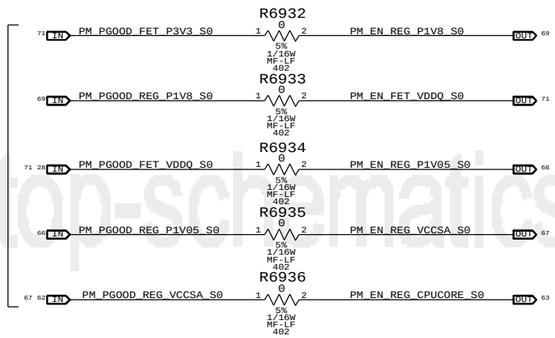
S0 Enables







CPU/PCH Sequencing



Rail definitions

Platform: All processor non-Core and non-Graphics (5 V, 3.3 V, 1.8 V 1.5 V, PCH Core/PLL/VRM)
Uncore: VccSA, VDDQ, VccA (1.8 V), VccIO (VccSA, VccA, and VccIO must ramp within 50 ms of each other)

Notes on sequencing requirements

Intel:
1. No hard specification on platform rails
2. SMC guarantees timing on PCH DPWROK and PWROK

NVIDIA:
1. 3V3_S0 must ramp first
2. IFPA/B_IOVDD (1.8 V) can ramp simultaneously or after 3V3_S0 (unused)
3. NVVDD (GPU_CORE) must ramp after IFPA/B_IOVDD
4. VDDQ must ramp after CPU_CORE
5. PEX_VDD with IFPC/D/E/F_IOVDD (1.05V) must ramp after VDDQ
6. All rails must reach their target voltages in more than 40 uS

SYNC_MASTER=D7i_INTEG SYNC_DATE=N/A

PAGE TITLE: PM Regulator Enables

Apple Inc.

DRAWING NUMBER: 051-9179 SIZE: D
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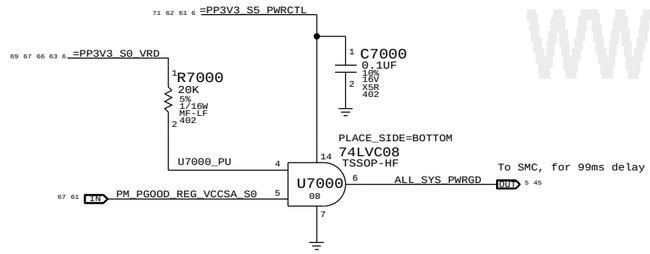
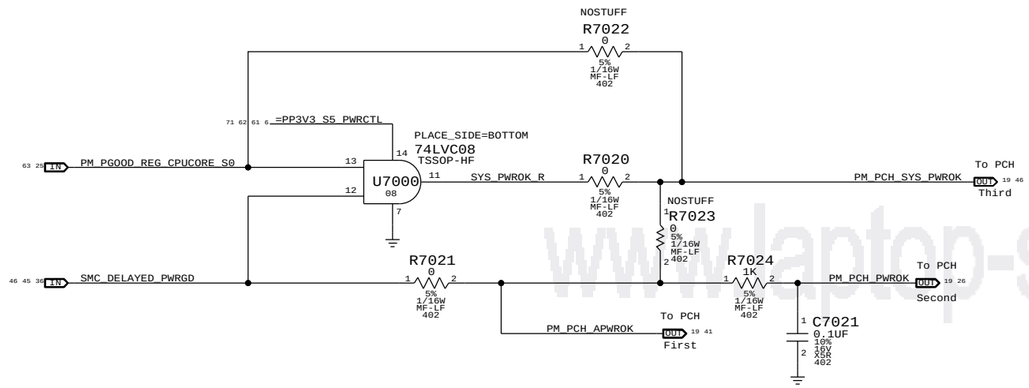
Platform and UnCore Power Good

Derive SMC ALL_SYS_PWRGD

Note: GPU power goods are implicitly included because the power goods for VDDQ, DPVDDC, and GPU Core are wired-or together



PCH Power Goods



Resume Reset

Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

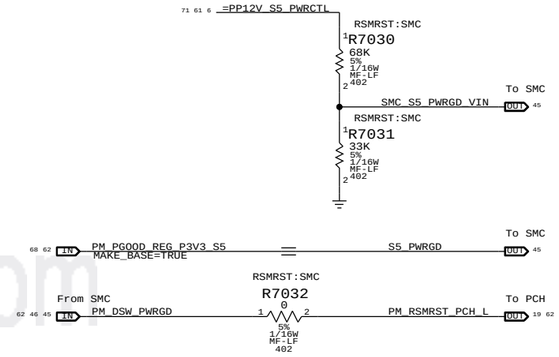
Note:
The iMac K70K72 designs does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V to allow PCH to switch suspend well to battery without excessive loading

Primary method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation.

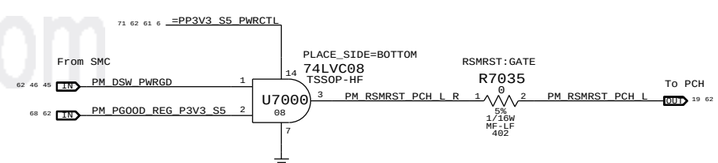
SMC de-asserts RSMRST# (PM_DSW_PWRGD) when S5_PWRGD input is asserted and SMC_S5_PWRGD_VIN input is above comparator input level of 1.5 V.

SMC asserts RSMRST# (PM_DSW_PWRGD) when SMC_S5_PWRGD_VIN input drops from 1.8 V to 1.5 V (as implemented) when 12 V S5 rail drops to 10 V.



Secondary method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



SYNC_MASTER=D7i_INTEG SYNC_DATE=N/A

PAGE TITLE
PM Power Good

Apple Inc.

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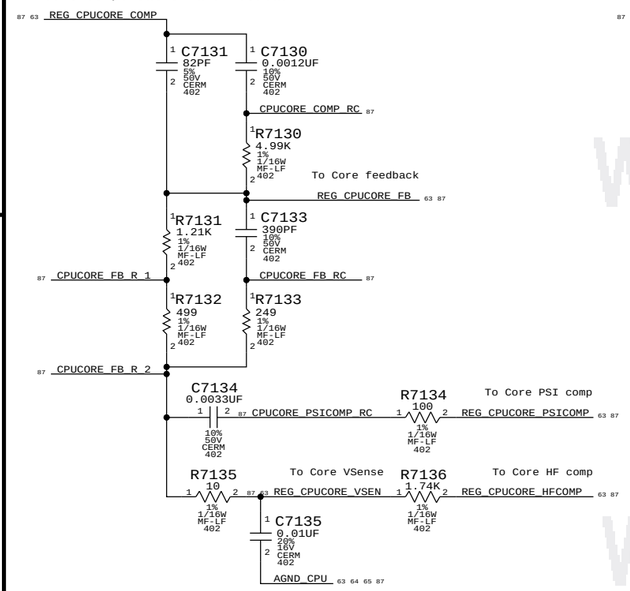
CPU Core S0 Regulator

Max avg current: ? A (design)/ 41.05 A (budget)
Max peak current: ? A (design)/75.05 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 290 kHz

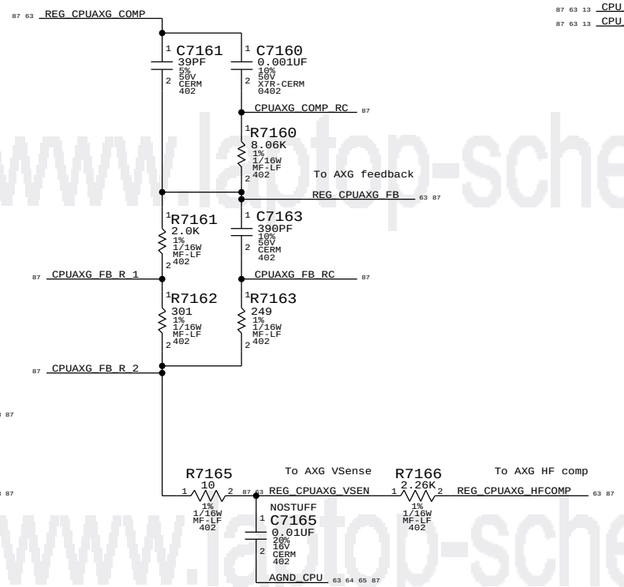
Core compensation and feedback



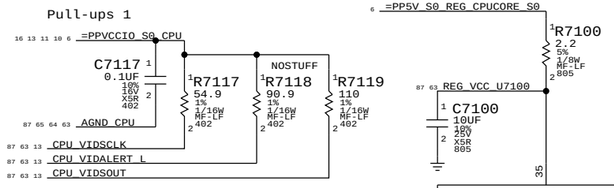
CPU AXG S0 Regulator

Max avg current: ? A (design)/ 10 A (budget)
Max peak current: ? A (design)/ 30 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 290 kHz

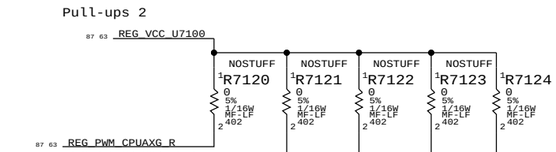
AXG compensation and feedback

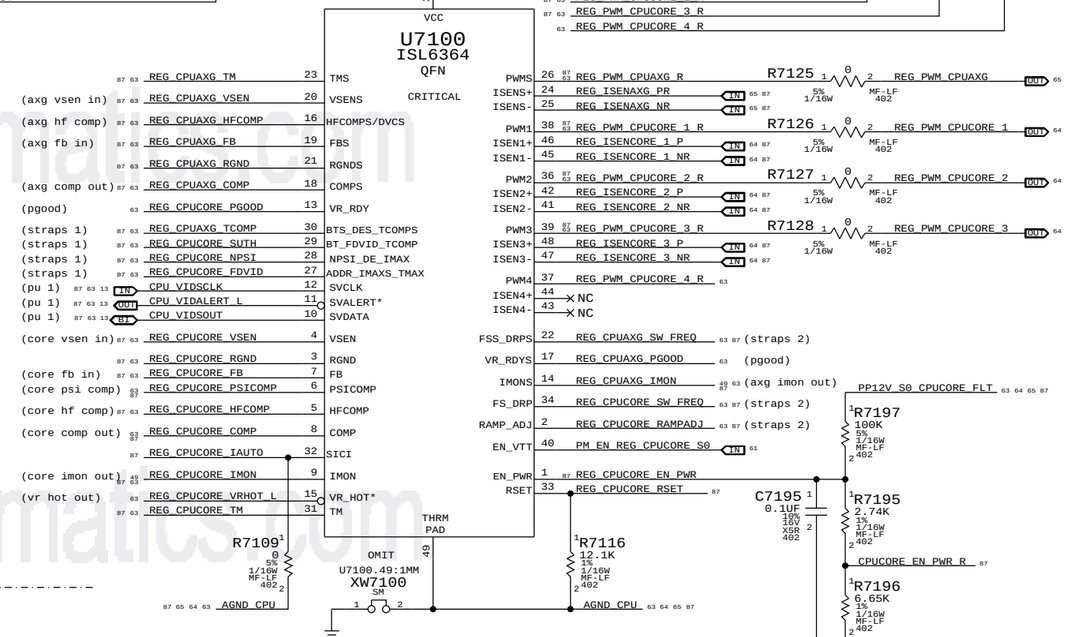


Pull-ups 1

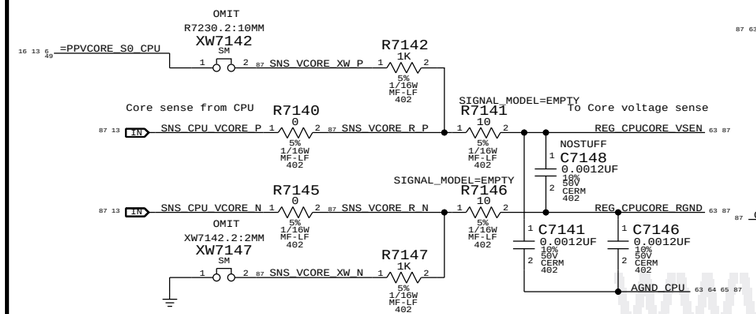


Pull-ups 2

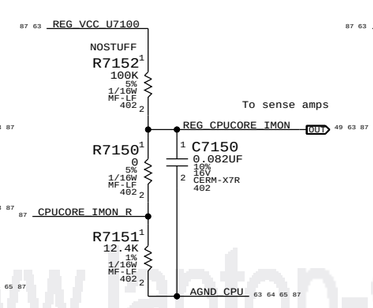




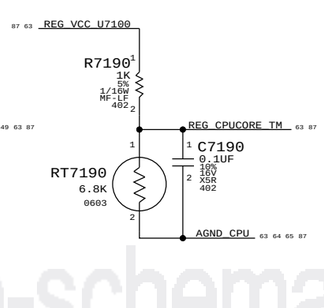
Core voltage sense input



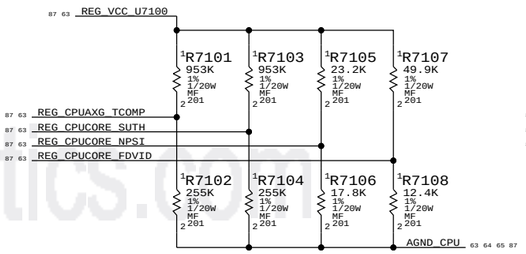
Core IMON output



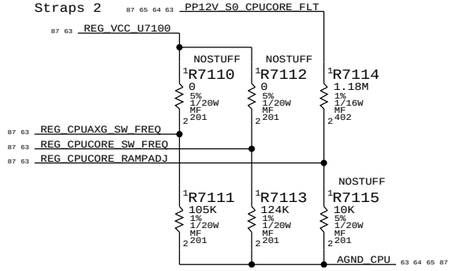
Core temp measurement



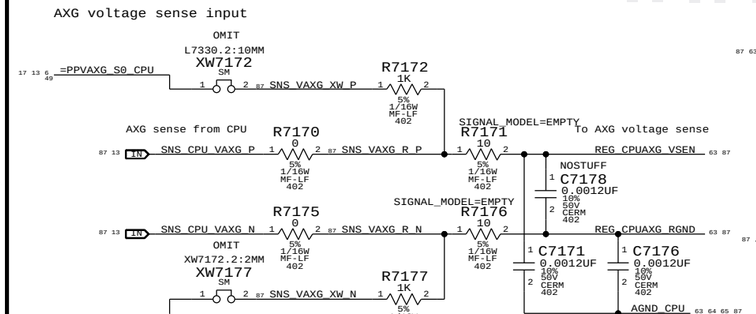
Straps 1



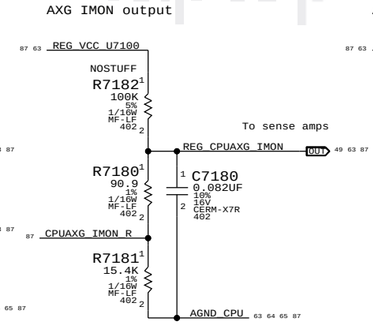
Straps 2



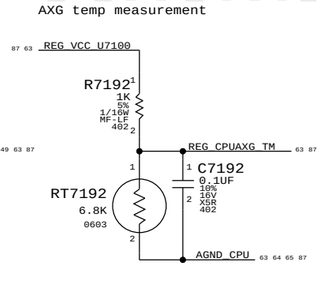
AXG voltage sense input



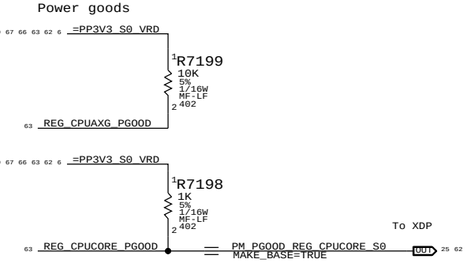
AXG IMON output



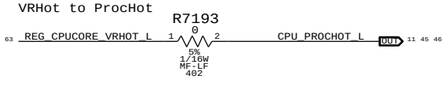
AXG temp measurement



Power goods



VRHot to ProcHot



SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE
VReg CPU Core/AXG Cntl

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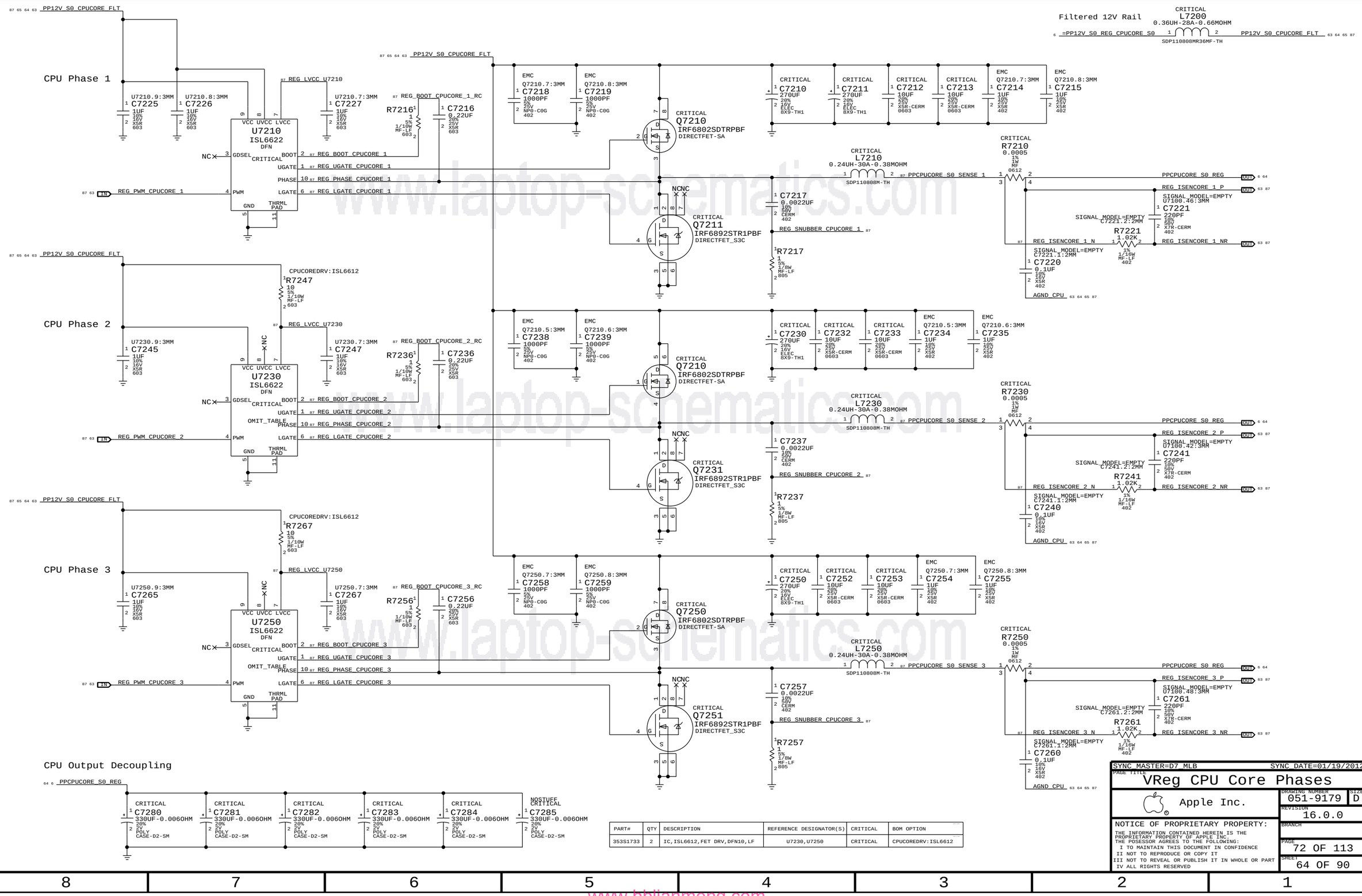

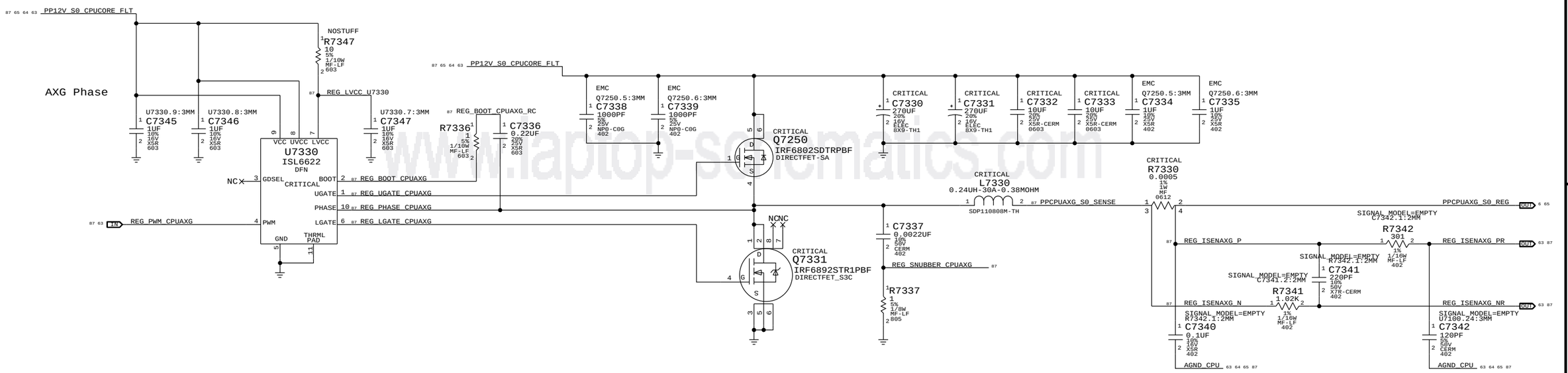

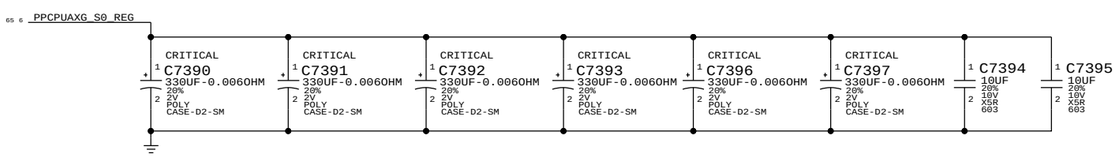

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE
VReg CPU AXG Phases

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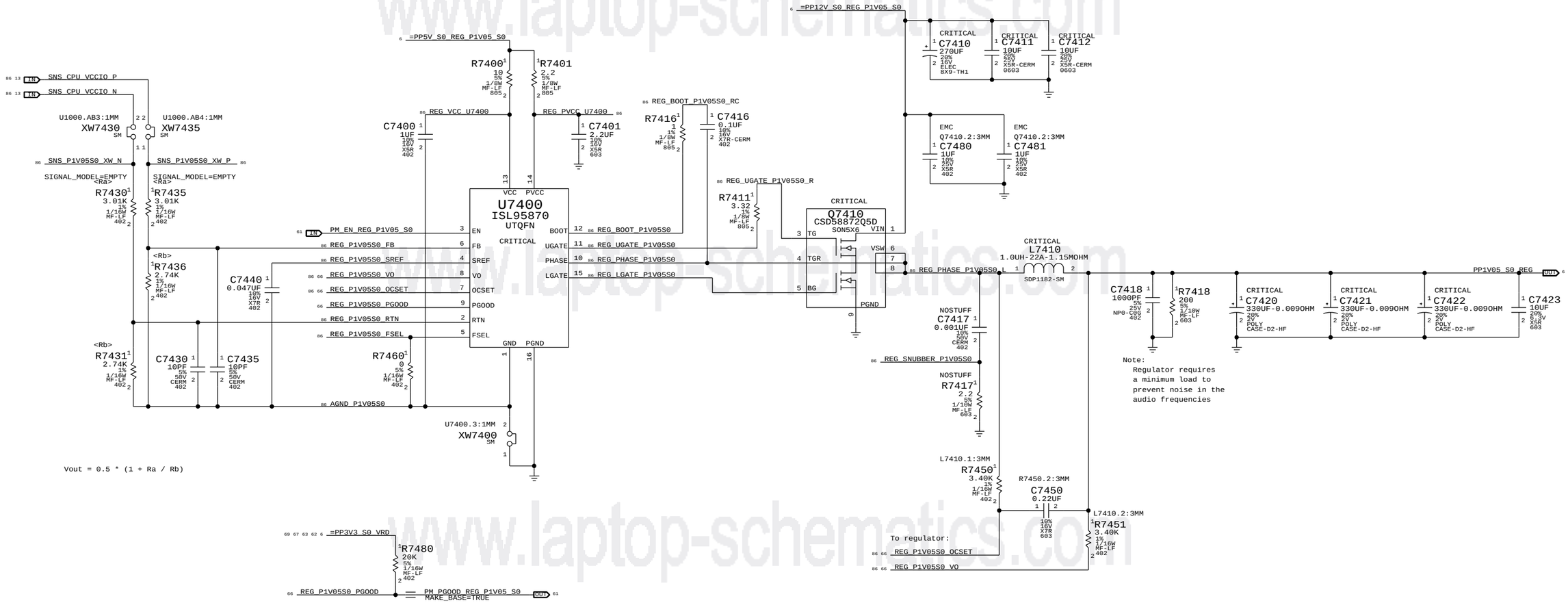
CPU VccIO/PCH (1.05V) S0 Regulator

Max avg current: ? A (design)/ 14.38 A (budget)
Max peak current: ? A (design)/ 18.38 A (budget)
OC trip point: ? A (min)/? A (max)
Switching freq: 500 kHz



SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE
VReg CPU/PCH 1.05V S0

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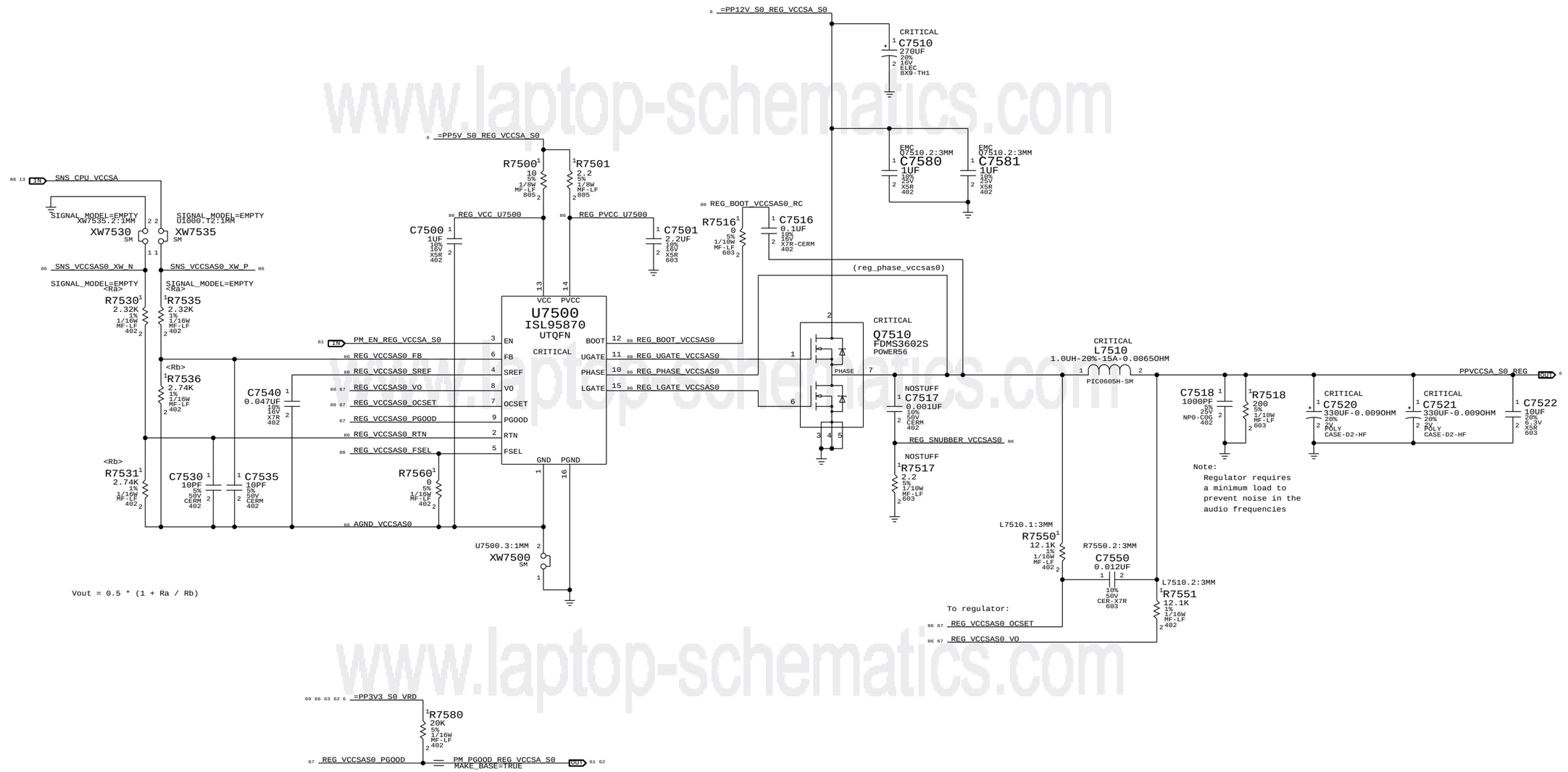
CPU VccSA (0.925V) S0 Regulator

Max avg current: ? A (design)/ 1.51 A (budget)
Max peak current: ? A (design)/ 8.76 A (budget)
OC trip point: ? A (min)/? A (max)
Switching freq: 500 kHz



SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE
VReg CPU VccSA S0

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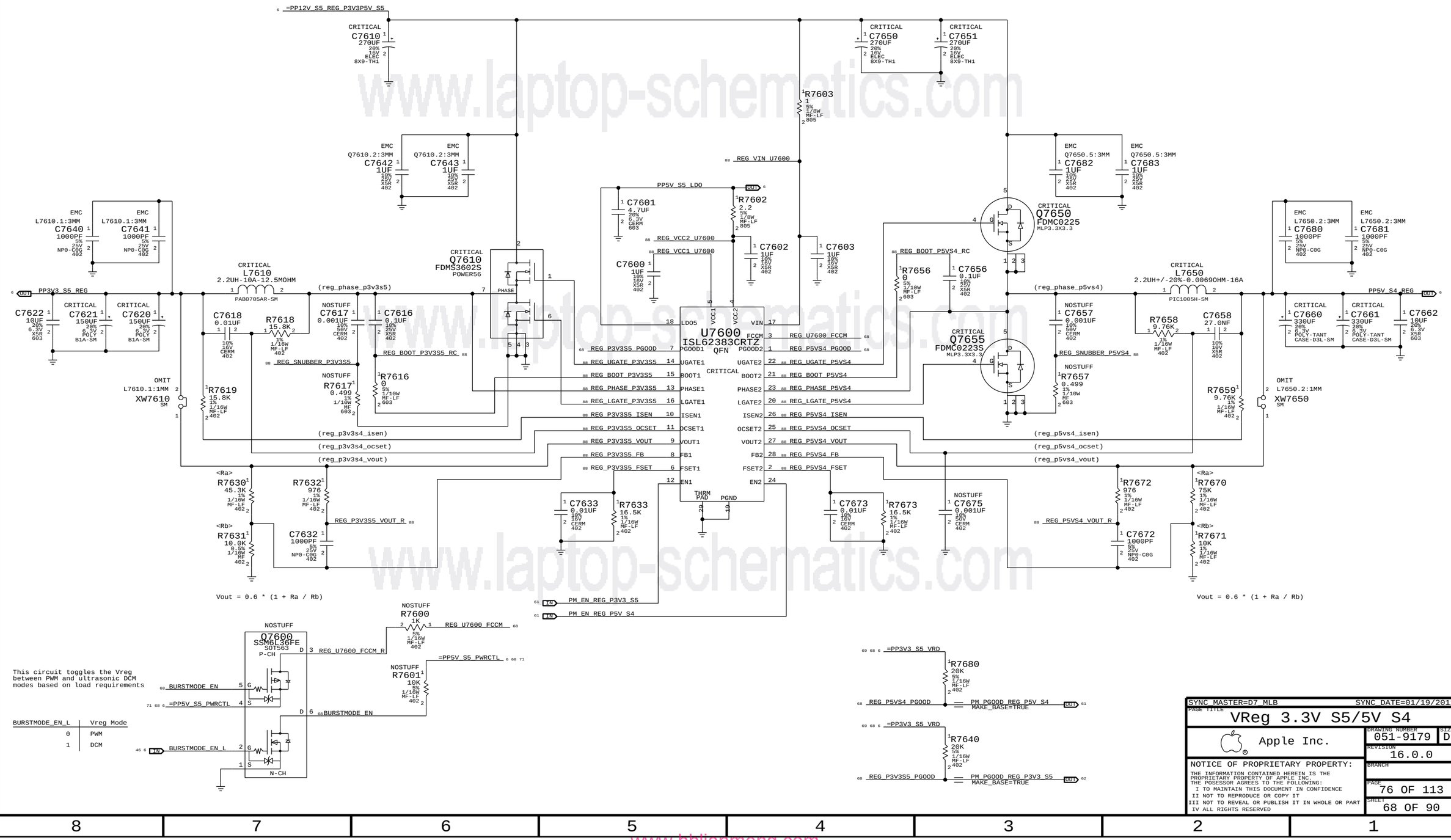
3.3V S5 Regulator

Max avg current: 6 A (design)/ 4.85 A (budget)
Max peak current: ? A (design)/ 6.6 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 350 kHz

5V S4 Regulator

Max avg current: 10 A (design)/ 6.08 A (budget)
Max peak current: ? A (design)/ 6.9 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 350 kHz



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PAGE TITLE: VReg 3.3V S5/5V S4

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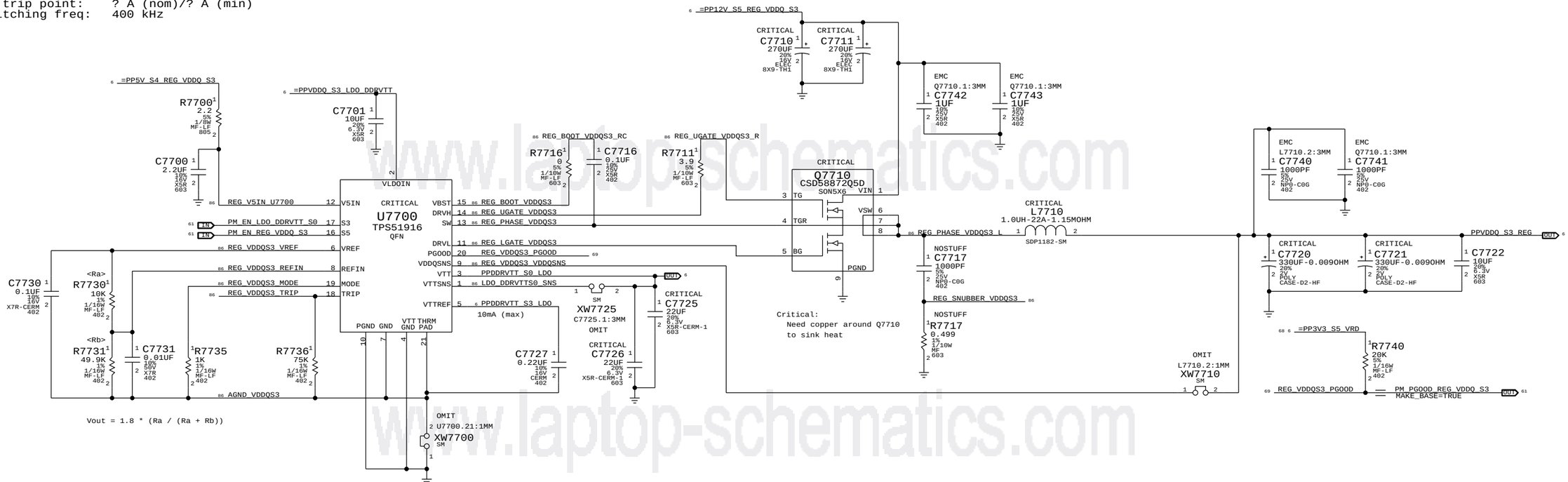
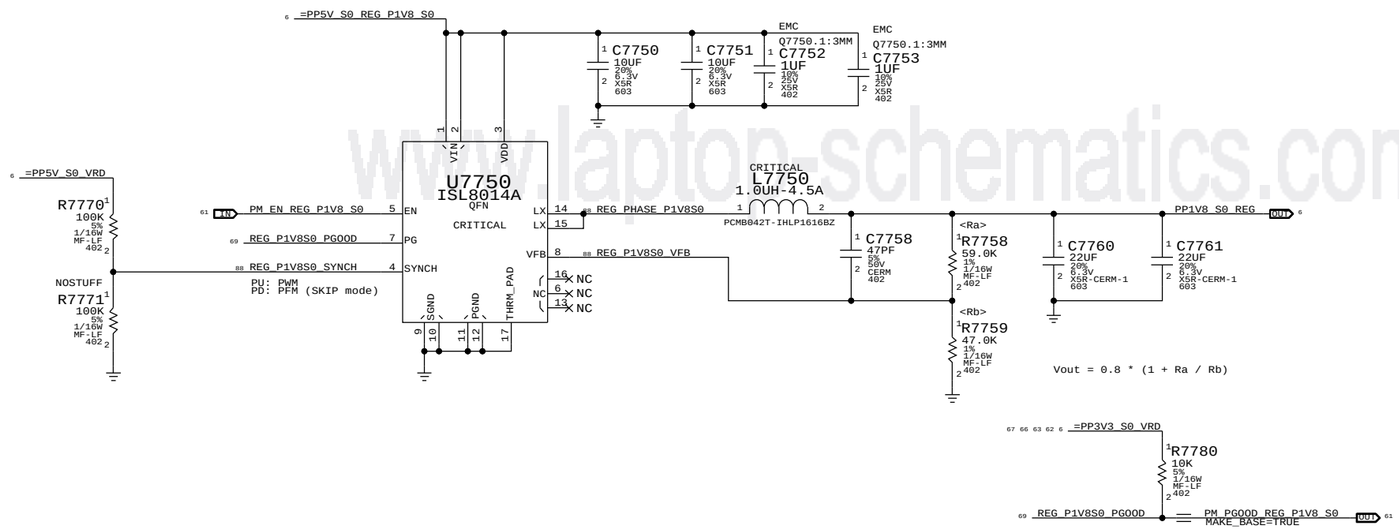
VDDQ (1.5V) S3 Regulator

Max avg current: ? A (design)/ 8 A (budget)
Max peak current: ? A (design)/ 17.8 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 400 kHz



1.8V S0 Regulator

Max avg current: 3 A (design)/ 0.61 A (budget)
Max peak current: ? A (design)/ 1.83 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: ? kHz



SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE: VReg VDDQ and 1.8V S0

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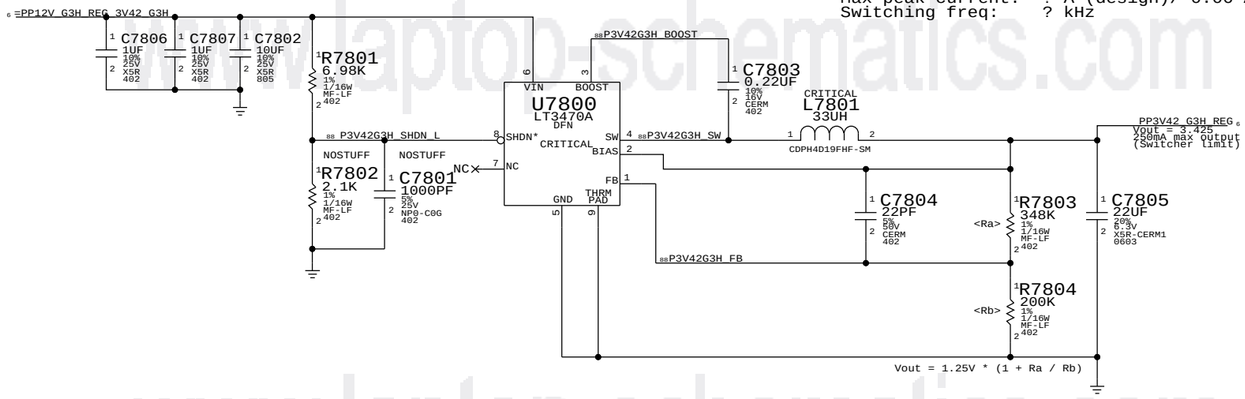
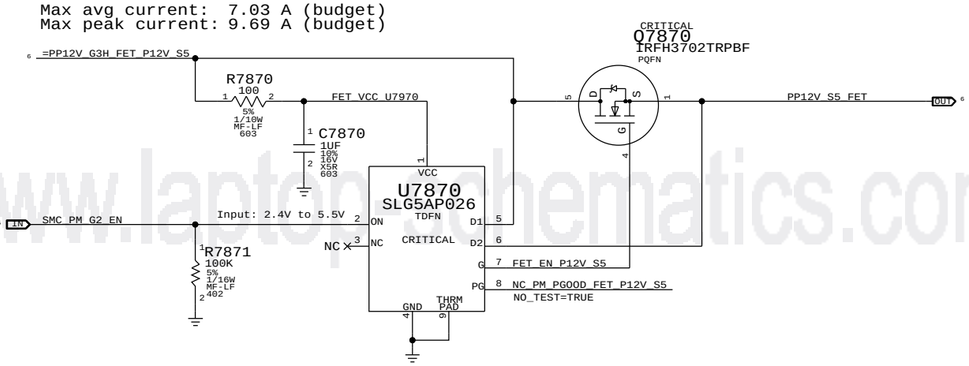
3.425V "G3Hot" Regulator

Max avg current: ? A (design)/ 0 A (budget)
Max peak current: ? A (design)/ 0.06 A (budget)
Switching freq: ? kHz



12V S5 FET

Max avg current: 7.03 A (budget)
Max peak current: 9.69 A (budget)



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PAGE TITLE: VReg G3Hot

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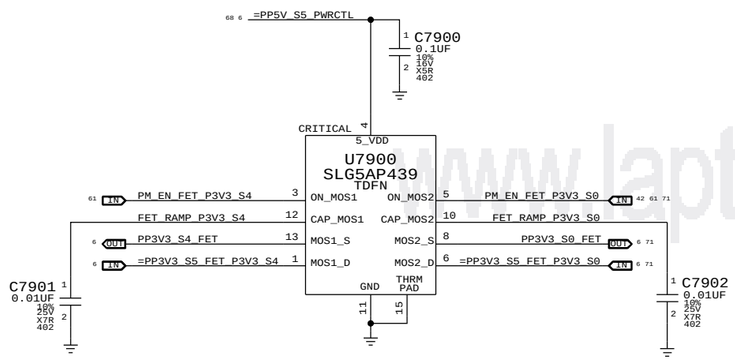
3.3V S4 FET

Max avg current: 0.85 A (budget)
Max peak current: 1.48 A (budget)

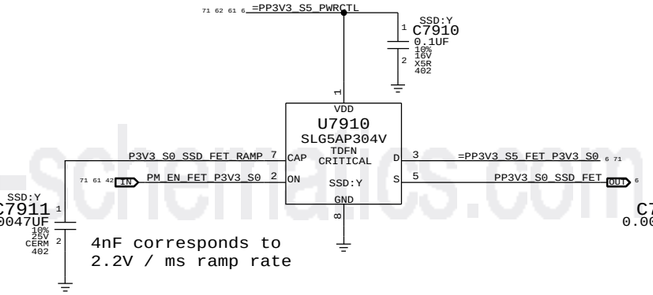


3.3V S0 FET

Max avg current: 1.7 A (budget)
Max peak current: 1.82 A (budget)

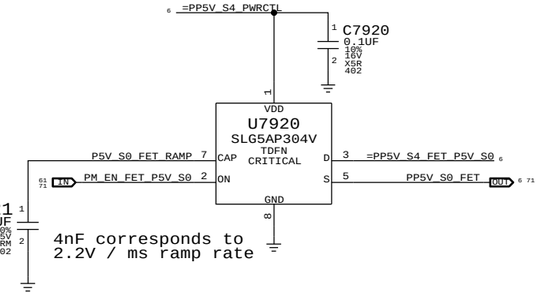
3V3 S0 SSD

Max avg current: 2.12 A (budget)
Max peak current: 3.03 A (budget)

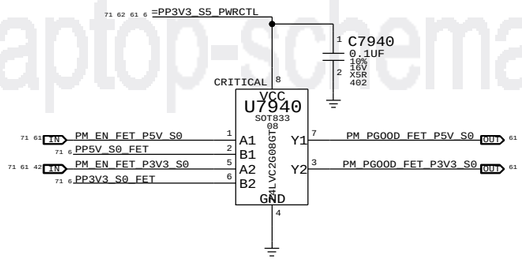


5V S0 FET

Max avg current: 1.26 A (budget)
Max peak current: 2.08 A (budget)

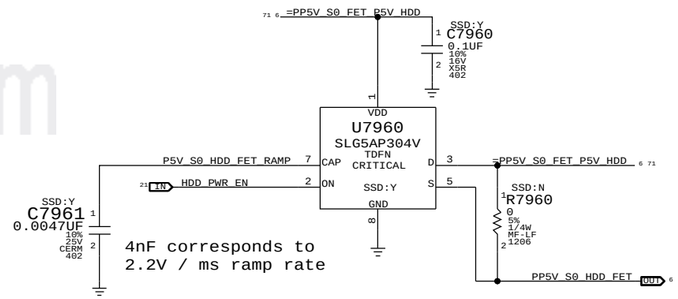


5V / 3V3 S0 PGOODs



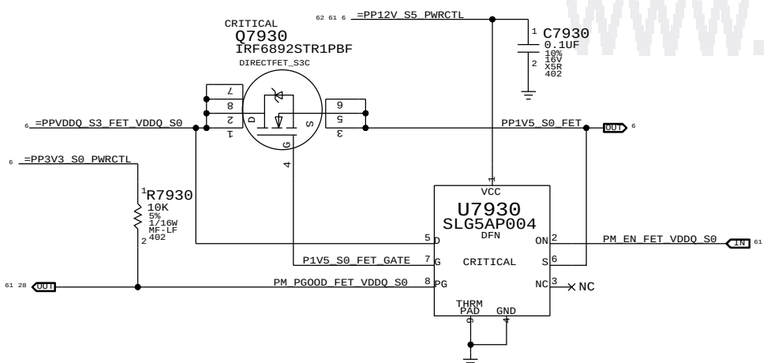
5V HDD FET

Max avg current: ? A (budget)
Max peak current: ? A (budget)



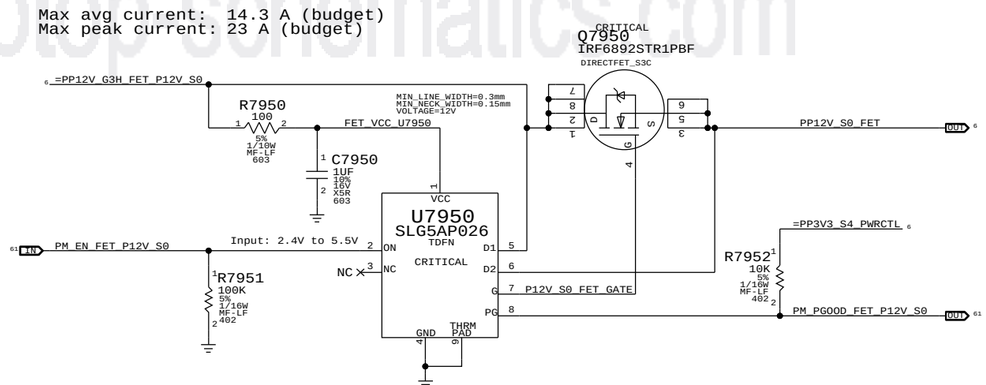
1.5V S0 FET

Max avg current: 1.27 A (budget)
Max peak current: 4.8 A (budget)



12V S0 FET

Max avg current: 14.3 A (budget)
Max peak current: 23 A (budget)



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Internal DP Connector

518S0829

CRITICAL

J9100
20525-130E-01
F-RT-SM

L9100
FERR-250-OHM
SM

=PP12V_S0_LCD → PP12V_LCD
VOLTAGE=12V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm

C9120 10UF 10% 16V X5R-CERM 0805
C9101 0.001UF 20% 50V CERM 402

Display TCon Master	OUT	SMB_DP_TCON_SDA
	OUT	SMB_DP_TCON_SCL
Display TCon Slave	BI	SMB_DP_TCON_SLA_SDA
	IN	SMB_DP_TCON_SLA_SCL
	OUT	DP_INT_SPDIF_AUDIO
	OUT	DP_INTPNL_HPD
	BI	DP_INTPNL_AUX_N
	BI	DP_INTPNL_AUX_P
	IN	DP_INTPNL_ML_P<0>
	IN	DP_INTPNL_ML_N<0>
	IN	DP_INTPNL_ML_P<1>
	IN	DP_INTPNL_ML_N<1>
	OUT	VIDEO_ON
	OUT	BKLT_VSYNC

Backlight Control

U9000 output Y2 is a non-inverted, delayed version of input A
The delay applies only on a L->H transition on A. This guarantees video is valid before the backlight is enabled.
On a H->L transition of A, Y2 follows with standard logic propagation delay. This ensures the backlight is off immediately after loss of video
Y1 is simply an inverted version of A, with no delay

=PP3V3_S0_DP

C9106 0.1UF 20% 10V CERM 402

U9100
SN1105002
SC70
VCC
CRITICAL
GND

VIDEO_ON → A
NC → NC
Y1 → VIDEO_ON_L → To Diag LED
Y2 → BKLT_EN → To BLC

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Internal DP Support

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TP to DP aliases

TP_DP_TBTSRC_ML_CP<0> = DP_TBTSRC_ML_P<0> (MAKE_BASE=TRUE)
TP_DP_TBTSRC_ML_CN<0> = DP_TBTSRC_ML_N<0> (MAKE_BASE=TRUE)
TP_DP_TBTSRC_ML_CP<1> = DP_TBTSRC_ML_P<1> (MAKE_BASE=TRUE)
TP_DP_TBTSRC_ML_CN<1> = DP_TBTSRC_ML_N<1> (MAKE_BASE=TRUE)
TP_DP_TBTSRC_AUXCH_CP = DP_TBTSRC_AUXCH_P (MAKE_BASE=TRUE)
TP_DP_TBTSRC_AUXCH_CN = DP_TBTSRC_AUXCH_N (MAKE_BASE=TRUE)

NC aliases

TP_DP_TBTSRC_ML_CP<2> = NC_DP_TBTSRC_ML_P<2> (NO_TEST=TRUE, MAKE_BASE=TRUE)
TP_DP_TBTSRC_ML_CN<2> = NC_DP_TBTSRC_ML_N<2> (NO_TEST=TRUE, MAKE_BASE=TRUE)
TP_DP_TBTSRC_ML_CP<3> = NC_DP_TBTSRC_ML_P<3> (NO_TEST=TRUE, MAKE_BASE=TRUE)
TP_DP_TBTSRC_ML_CN<3> = NC_DP_TBTSRC_ML_N<3> (NO_TEST=TRUE, MAKE_BASE=TRUE)
DP_INT_EG_ML_P<2> = NC_DP_INT_EG_ML_P<2> (NO_TEST=TRUE, MAKE_BASE=TRUE)
DP_INT_EG_ML_N<2> = NC_DP_INT_EG_ML_N<2> (NO_TEST=TRUE, MAKE_BASE=TRUE)
DP_INT_EG_ML_P<3> = NC_DP_INT_EG_ML_P<3> (NO_TEST=TRUE, MAKE_BASE=TRUE)
DP_INT_EG_ML_N<3> = NC_DP_INT_EG_ML_N<3> (NO_TEST=TRUE, MAKE_BASE=TRUE)

=PP3V3_S0_INTDPMUX
C9268 0.1UF 10% 6.3V X5R 201
C9269 0.1UF 10% 6.3V X5R 201

U9200 PI3VEDP212 TQFN CRITICAL
VDD pins: 29, 20, 16, 12, 9, 3

DP_INT_EG_ML_P<0>	31	D0+A	
DP_INT_EG_ML_N<0>	30	D0-A	
DP_INT_EG_ML_P<1>	27	D1+A	
DP_INT_EG_ML_N<1>	26	D1-A	
DP_INT_EG_AUX_P (C9208 0.1UF)	19	AUX+A	
DP_INT_EG_AUX_N (C9209 0.1UF)	18	AUX-A	
DP_INT_EG_HPD	17	HPD_A	
DP_TBTSRC_ML_C_P<0>	25	D0+B	
DP_TBTSRC_ML_C_N<0>	24	D0-B	
DP_TBTSRC_ML_C_P<1>	23	D1+B	
DP_TBTSRC_ML_C_N<1>	22	D1-B	
DP_TBTSRC_AUXCH_P (C9210 0.1UF)	15	AUX+B	
DP_TBTSRC_AUXCH_N (C9211 0.1UF)	14	AUX-B	
DP_TBTSRC_HPD	13	HPD_B	
DP_GPU_TBT_SEL	10	SEL	
	32	AUX_SEL	
	11	HPD_SEL	
	33, 28, 21	THMPAD_GND	

PD is on the CR page

R9201 10K 5% 1/20W MF 201
R9200 100K 5% 1/20W MF 201

DP_INTPNL_ML_C_P<0> → C9200 0.1UF → DP_INTPNL_ML_P<0>
DP_INTPNL_ML_C_N<0> → C9201 0.1UF → DP_INTPNL_ML_N<0>
DP_INTPNL_ML_C_P<1> → C9202 0.1UF → DP_INTPNL_ML_P<1>
DP_INTPNL_ML_C_N<1> → C9203 0.1UF → DP_INTPNL_ML_N<1>
DP_INTPNL_AUX_P / DP_INTPNL_AUX_N
DP_INTPNL_HPD
R9202 100K 5% 1/20W MF 201
R9203 100K 5% 1/20W MF 201 → =PP3V3_S0_INTDPMUX

DP_TBTSRC_ML_P<0> → C9212 0.1UF → DP_TBTSRC_ML_C_P<0>
DP_TBTSRC_ML_N<0> → C9213 0.1UF → DP_TBTSRC_ML_C_N<0>
DP_TBTSRC_ML_P<1> → C9214 0.1UF → DP_TBTSRC_ML_C_P<1>
DP_TBTSRC_ML_N<1> → C9215 0.1UF → DP_TBTSRC_ML_C_N<1>
R9212 2.7K, R9213 2.7K, R9214 2.7K, R9215 2.7K — 5% 1/20W MF 201

=PP3V3_S0_INTDPMUX
C9270 0.1uF 10% 16V X5R 402
U9220 74LVC1G157 SOT487 (BKLT_PWM)
BDV_BKL_PWM, GPU_LCD_BKLT_PWM, DP_GPU_TBT_SEL
LCD_BKLT_PWM
R9222 47 5% 1/10W MF-LF 402
L9201 FERR-220-OHM 0402
LCD_BKLT_FILT → LCD_BKLT_PWM

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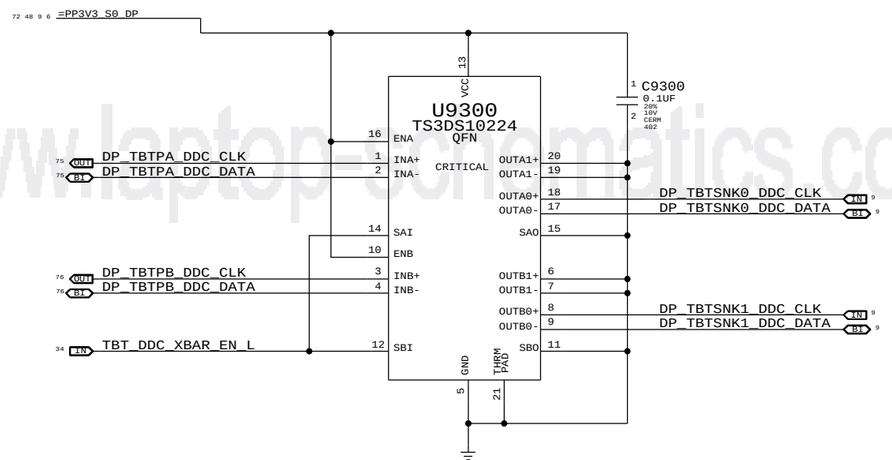
Dual-Port Host DDC Crossbar



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TBT DDC Crossbar

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

=PP3V3_S4_TBTAPWRSW
CRITICAL C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM
CRITICAL C9480 22UF 20% 6.3V X5R-CERM-1 603
C9481 0.1UF 20% 10V CERM 402
=PPHV_SW_TBTAPWRSW
18.9V Max
C9415 4.7UF 10% 25V X5R-CERM 0603
C9410 0.1UF 10% 50V X7R 603-1
CRITICAL U9410 CD3210A0RGP QFN
V3P3 V3P3OUT NC
VHV OUT
RSVD RSVD
EN ISET_V3P3
HV_EN ISET_S0
S0 ISET_S3
GND THRM PAD
=TBTAPWRSW_EN
TBT_A_HV_EN
=TBT_S0_EN
PPHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
C9411 0.1UF 10% 50V X7R 603-1
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
TBTHV:P15V
12V: See below
R9410 22.6K 1% 1/16W MF-LF 402
R9411 22.6K 1% 1/16W MF-LF 402
R9412 36.5K 1% 1/16W MF-LF 402
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
R9413 22.6K 1% 1/16W MF-LF 402
R9414 22.6K 1% 1/16W MF-LF 402
Two Rs in series required by CD3210 for single-fault protection(S0,S3 only)

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9410,R9413		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9411,R9414		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector A

=PP3V3_S4_TBT
C9420 0.1UF 10% 6.3V X5R 201
C9421 0.1UF 10% 6.3V X5R 201
R9427 10K 5% 1/20W MF 201
R9429 100K 5% 1/20W MF 201
VDD
CRITICAL U9420 CBTL05023 HVQFN
TBT_A_BIAS VOLTAGE=3.3V
C9425 0.1UF 10% 6.3V X5R 201
TBT_A_CIO_SEL
DP_AUXIO_EN
DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
C9430 0.1UF 10% 6.3V X5R 201
C9431 0.1UF 10% 6.3V X5R 201
DP_TBTPA_AUXCH_N
DP_TBTPA_AUXCH_P
DP_TBTPA_DDC_DATA
DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
C9432 0.22UF 20% 6.3V X5R 0201
C9433 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_P<1>
DP_TBTPA_ML_N<1>
TBT_A_LSTX
TBT_A_LSRX_UNBUF
TBT_A_DP_PWRDN
DP_TBTPA_HPD
BIASIN BIASOUT
AUXIO_EN
AUX- AUXIO-
AUX+ AUXIO+
DDC_DAT CA_DETOUT CA_DET
DDC_CLK
DP+ DPMLO+
DP- DPMLO-
LSTX
LSRX
DP_PD
HPDOUT HPD
GND THMPAD
DP_A_AUXCH_DDC_N
DP_A_AUXCH_DDC_P
TBT: RX_1 Bias Sink
TBT_A_CONFIG1_RC
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_A_HPD
R9426 1M 5% 1/20W MF 201
R9428 100K 5% 1/20W MF 201
CRITICAL U9460 74AUP1T97 SOT891
C9460 0.1UF 10% 16V X5R-CERM 0201

L9400 FERR-120-OHM-3A 0603
PP3V3RHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
C9400 0.01UF 10% 50V X7R 402
R9401 12 5% 1/20W MF 201
TBTACONN_20_RC
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
C9401 0.01UF 10% 50V X7R 402

C9405 0.01UF 10% 25V X5R-CERM 0201
TBTACONN_1_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
DP Dir TBT Dir
TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
TBT: TX_0
C9470 0.22UF 20% 6.3V X5R 0201
C9471 0.22UF 20% 6.3V X5R 0201
GND_VOID=TRUE (Both C's)
R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201

C9406 0.01UF 10% 25V X5R-CERM 0201
TBTACONN_7_C
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.9V
(0-18.9V)
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_R2P/P2R (P/N)

CRITICAL J9400 DUAL-MDP-K70 F-ANG-TH
SHLD
HPD CONFIG1 CONFIG2 GND2 ML_LANE3P ML_LANE3N GND4 AUX_CHP AUX_CHN DP_PWR
ML_LANE0P ML_LANE0N GND1 ML_LANE1P ML_LANE1N GND3 ML_LANE2P ML_LANE2N RETURN
PORT A SHLD
514-0824

GND_VOID=TRUE (Both C's)
C9474 0.22UF 20% 6.3V XSR 0201
C9475 0.22UF 20% 6.3V XSR 0201
TBT_A_D2R_N<0>
TBT_A_D2R_P<0>
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
NOTE: Polarity Swapped for layout!
R9494 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY
R9495 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY
C9478 0.22UF 20% 6.3V XSR 0201
C9479 0.22UF 20% 6.3V XSR 0201
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
TBT: Terminated
R9478 470K 5% 1/20W MF 201
R9479 470K 5% 1/20W MF 201
TBT_A_BIAS
R9498 2.2K 5% 1/20W MF 201
R9499 2.2K 5% 1/20W MF 201
GND_VOID=TRUE (Both C's)
C9476 0.22UF 20% 6.3V XSR 0201
C9477 0.22UF 20% 6.3V XSR 0201
TBT_A_D2R_N<1>
TBT_A_D2R_P<1>
TBT_A_D2R_C_P<1>
TBT_A_D2R_C_N<1>
NOTE: Polarity Swapped for layout!
CRITICAL GND_VOID=TRUE (Both D's)
D9498 BAR90-02LRH TSLP-2-7
D9499 BAR90-02LRH TSLP-2-7
TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N
CRITICAL L9498 650NH-5%-0.430MA-0.52OHM 0603 SIGNAL_MODEL=EMPTY
CRITICAL L9499 650NH-5%-0.430MA-0.52OHM 0603 SIGNAL_MODEL=EMPTY
DP_A_AUXCH_DDC_P
DP_A_AUXCH_DDC_N
C9498 30PF 5% 50V CERM 402
C9499 30PF 5% 50V CERM 402
TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R9452 1M 5% 1/20W MF 201
R9451 1M 5% 1/20W MF 201
C9494 330PF 10% 16V X7R 201
C9495 330PF 10% 16V X7R 201
R9441 100K 5% 1/20W MF 201
C9402 0.01UF 10% 25V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
TBT: TX_1
C9472 0.22UF 20% 6.3V XSR 0201
C9473 0.22UF 20% 6.3V XSR 0201
GND_VOID=TRUE (Both C's)
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201
NOTE: Polarity Swapped for layout!
470k R's for ESD protection on AC-coupled signals.

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

=PP3V3_S4_TBTBPWRSW
CRITICAL C9687 100UF 20% 6.3V POLY-TANT CASE-B2-SM
CRITICAL C9680 22UF 20% 6.3V X5R-CERM-1 603
C9681 0.1UF 20% 10V CERM 402
=PPHV_SW_TBTBPWRSW
18.9V Max
C9615 4.7UF 10% 25V X5R-CERM 0603
C9610 0.1UF 10% 50V X7R 603-1
CRITICAL U9610 CD3210A0RGP QFN
V3P3 V3P3OUT NC
VHV OUT
RSVD RSVD
EN ISET_V3P3
HV_EN ISET_S0
S0 ISET_S3
GND THRM PAD
PPHV_SW_TBTBPWR
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=15V
C9611 0.1UF 10% 50V X7R 603-1
=TBTBPWRSW_EN
TBT_B_HV_EN
=TBT_S0_EN
TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3
12V: See below
TBTHV:P15V
R9610 22.6K 1% 1/16W MF-LF 402
R9611 22.6K 1% 1/16W MF-LF 402
R9612 36.5K 1% 1/16W MF-LF 402
TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R
R9613 22.6K 1% 1/16W MF-LF 402
R9614 22.6K 1% 1/16W MF-LF 402
Two Rs in series required by CD3210 for single-fault protection(S0,S3 only)

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9610,R9613		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9611,R9614		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

NOTE: Polarity Swapped for Layout!

NOTE: Polarity Swapped for Layout!

TBT: Terminated

Thunderbolt Connector B

=PP3V3_S4_TBT
C9620 0.1UF 10% 6.3V X5R 201
C9621 0.1UF 10% 6.3V X5R 201
R9627 10K 5% 1/20W MF 201
R9629 100K 5% 1/20W MF 201
CRITICAL U9620 CBTL05023 HVQFN VDD
TBT_B_BIAS VOLTAGE=3.3V
C9625 0.1UF 10% 6.3V X5R 201
TBT_B_CIO_SEL
DP_AUXIO_EN
DP_TBTPB_AUXCH_C_N
DP_TBTPB_AUXCH_C_P
C9630 0.1UF 10% 6.3V X5R 201
C9631 0.1UF 10% 6.3V X5R 201
BIASIN BIASOUT
AUXIO_EN
AUX- AUX+
DDC_DAT DDC_CLK
CA_DETOUT CA_DET
DP+ DP-
LSTX LSRX
DP_PD
HPDOUT HPD
AUXIO- AUXIO+
DPMLO+ DPMLO-
DP_B_AUXCH_DDC_N
DP_B_AUXCH_DDC_P
TBT: RX_1 Bias Sink
TBT_B_CONFIG1_BUF
TBT_B_CONFIG1_RC
DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
C9632 0.22UF 20% 6.3V X5R 0201
C9633 0.22UF 20% 6.3V X5R 0201
DP_TBTPB_ML_P<1>
DP_TBTPB_ML_N<1>
DP_B_LSX_ML_P<1>
DP_B_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_B_LSTX
TBT_B_LSRX_UNBUF
TBT_B_DP_PWRDN
DP_TBTPB_HPD
TBT_B_HPD
=PP3V3_S4_TBT
CRITICAL U9660 74AUP1T97 SOT891
TBT_B_LSRX
C9660 0.1UF 10% 16V X5R-CERM 0201
R9626 1M 5% 1/20W MF 201
R9628 100K 5% 1/20W MF 201
GND_THMPAD

L9600 FERR-120-OHM-3A 0603
PP3V3RHV_SW_TBTBPWR
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=15V
C9600 0.01UF 10% 50V X7R 402
C9601 0.01UF 10% 50V X7R 402
TBTBCONN_20_RC
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
R9601 12 5% 1/20W MF 201
TBT Dir DP Dir
CRITICAL J9400 DUAL-MDP-K70 F-ANG-TH
SHLD
HPD CONFIG1 CONFIG2 GND2 ML_LANE3P ML_LANE3N GND4 AUX_CHP AUX_CHN DP_PWR
GND0 ML_LANE0P ML_LANE0N GND1 ML_LANE1P ML_LANE1N GND3 ML_LANE2P ML_LANE2N RETURN
PORT B SHLD
514-0824
C9602 0.01UF 10% 25V X5R-CERM 0201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

C9605 0.01UF
TBTBCONN_1_C
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
(0-18.9V)
DP Dir TBT Dir
TBT: TX_0
C9606 0.01UF
TBTBCONN_7_C
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
(0-18.9V)
TBT: LSX_R2P/P2R (P/N)
TBT: TX_1
C9670 0.22UF
C9671 0.22UF
R9670 470K 5% 1/20W MF 201
R9671 470K 5% 1/20W MF 201
TBT_B_R2D_C_P<0>
TBT_B_R2D_C_N<0>
C9672 0.22UF
C9673 0.22UF
R9672 470K 5% 1/20W MF 201
R9673 470K 5% 1/20W MF 201
TBT_B_R2D_C_N<1>
TBT_B_R2D_C_P<1>
470k R's for ESD protection on AC-coupled signals.

C9674 0.22UF
C9675 0.22UF
TBT_B_D2R_N<0>
TBT_B_D2R_P<0>
TBT_B_D2R_C_P<0>
TBT_B_D2R_C_N<0>
R9694 1K 5% 1/20W MF 201
R9695 1K 5% 1/20W MF 201
SIGNAL_MODEL=EMPTY
C9678 0.22UF
C9679 0.22UF
DP_TBTPB_ML_C_P<3>
DP_TBTPB_ML_C_N<3>
R9678 470K 5% 1/20W MF 201
R9679 470K 5% 1/20W MF 201
C9676 0.22UF
C9677 0.22UF
TBT_B_D2R_N<1>
TBT_B_D2R_P<1>
TBT_B_D2R_C_P<1>
TBT_B_D2R_C_N<1>
R9698 2.2K 5% 1/20W MF 201
R9699 2.2K 5% 1/20W MF 201
D9698 BAR90-02LRH TSLP-2-7
D9699 BAR90-02LRH TSLP-2-7
TBT_B_D2R1_AUXDDC_P
TBT_B_D2R1_AUXDDC_N
CRITICAL L9698 650NH-5%-0.430MA-0.52OHM 0603
CRITICAL L9699 650NH-5%-0.430MA-0.52OHM 0603
SIGNAL_MODEL=EMPTY
DP_B_AUXCH_DDC_P
DP_B_AUXCH_DDC_N
C9698 30PF 5% 50V CERM 402
C9699 30PF 5% 50V CERM 402
TBT_B_HPD
TBT_B_CONFIG1_RC
TBT_B_CONFIG2_RC
R9652 1M 5% 1/20W MF 201
R9651 1M 5% 1/20W MF 201
C9694 330PF 10% 16V X7R 201
C9695 330PF 10% 16V X7R 201
R9641 100K 5% 1/20W MF 201

GND_VOID=TRUE (Both C's)
GND_VOID=TRUE (Both D's)
GND_VOID=TRUE

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0745	138S0743		BLC_CAP	BLC Ouput Cap

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1592	152S1591		L9700	BLC Switch Inductor
371S0648	371S0694		D9700	BLC Switch Diode

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1054	376S1022		Q9700	BLC Switch FET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S3665	1	IC,LP8561,LED BKLT CTRLR,LLP24,B0	U9700	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1071	376S1073		ALL	Short Protection FET

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0845	376S1067		Q9702	BLC Inrush FET

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE: LCD Backlight Driver (LP8545)

Apple Inc.

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K70 Board Specific Physical and Spacing Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OF MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA	MM	16.2

General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	*	Y	0.215 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	TOP,BOTTOM	Y	0.215 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	*	Y	0.170 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	*	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	0.138 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.138 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.110 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	Y	0.180 MM	0.085 MM	=STANDARD	0.140 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.180 MM	0.085 MM	=STANDARD	0.140 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.135 MM	0.085 MM	=STANDARD	0.160 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD	0.160 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.089 MM	0.085 MM	=STANDARD	0.220 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.085 MM	=STANDARD	0.220 MM	0.1 MM

General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	*	0.076 MM	?
1X_DIELECTRIC	TOP,BOTTOM	0.071 MM	?

BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1100

BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

Board Stack-up

Finished board thickness: 1.58 mm

Top	Signal	0.5 oz (Cu plated)	
	Prepreg	0.071 mm	
2	Plane	1 oz	
	Prepreg	0.076 mm	
3	Signal	0.5 oz	
	Prepreg	0.435 mm	
4	Plane	1 oz	
	Core	0.127 mm	
5	Plane	1 oz	
	Prepreg	0.435 mm	
6	Signal	0.5 oz	
	Prepreg	0.076 mm	
2	Plane	1 oz	
	Prepreg	0.071 mm	
Btm	Signal	0.5 oz (Cu plated)	

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

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DDR3

DDR3-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_34S	*	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=STANDARD	=STANDARD
DDR_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
DDR_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
DDR_42S_D	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	0.1016 MM	0.1016 MM
DDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
DDR_68D	*	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF

Minimum diff spacing is 4 mil
Table 3-5, Intel Doc# 473718

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
POWER_DDR_P4MM	*	Y	0.400 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_DDR	*	POWER_DDR_P4MM
DDR_CLK_PHY	*	DDR_68D
DDR_CTRL_PHY	*	DDR_39S
DDR_CMD_PHY	*	DDR_34S
DDR_DQ_PHY	*	DDR_42S
DDR_DQS_PHY	*	DDR_42S_D

DDR3 Power-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_DDR	*	=2:1_SPACING	?

DDR3-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DDR_CLK_ISO	*	=5:1_SPACING	?
DDR_CTRL_ISO	*	=3.5:1_SPACING	?
DDR_CTRL2CTRL	*	=2.5:1_SPACING	?
DDR_CMD_ISO	*	=3.5:1_SPACING	?
DDR_CMD2CMD	*	=2:1_SPACING	?
DDR_DATA_ISO	*	=3:1_SPACING	?
DDR_DQ2DQ	*	=2:1_SPACING	900
DDR_DQ2DQS	*	=3:1_SPACING	?
DDR_BL2BL	*	=3:1_SPACING	?
DDR_CH2CH	*	=6.5:1_SPACING	?

Main Segment Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Table	Trace	Design	Iso	Design	Comments
3-2	4	(diff)	15	19.69	CLK trace spacing controlled by =68_OHM_DIFF
3-3	8	9.84	12	13.78	
3-4	6	7.87	12	13.78	
3-5	8.5	7.87	12	11.81	DQ or DQS to other signals not in the same bytelane (but not ch)
					DQ to DQ in the same bytelane of the same channel
			10	11.81	DQ to DQS in the same bytelane of the same channel
			12	11.81	DQ or DQS in different bytelanes of the same channel
			25	25.59	DQ or DQS in different channels
			-	25.59	DDR3 to any other signal not DDR3

Constraints

Clocks: CK[3:0], CK#[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CLK	*	*	DDR_CLK_ISO

Control: CS#[3:0], CKE[3:0], ODT[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CTRL	*	*	DDR_CTRL_ISO
DDR_CTRL	DDR_CTRL	*	DDR_CTRL2CTRL

Command: MA[15:0], RAS#, CAS#, WE# BS[2:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CMD	*	*	DDR_CMD_ISO
DDR_CMD	DDR_CMD	*	DDR_CMD2CMD

Data: DQS[7:0], DQS#[7:0], DQ[63:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
DDR_A_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_A_DQS*	*	*	DDR_DATA_ISO	
DDR_B_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_B_DQS*	*	*	DDR_DATA_ISO	
DDR_*_DQ_BYTE*	=SAME	*	DDR_DQ2DQ	See Note (3)
DDR_A_DQ_BYTE*	DDR_A_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_A_DQ_BYTE*	DDR_A_DQ_BYTE*	*	DDR_BL2BL	See Note (3)
DDR_B_DQ_BYTE*	DDR_B_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_B_DQ_BYTE*	DDR_B_DQ_BYTE*	*	DDR_BL2BL	
DDR_A_*	DDR_B_*	*	DDR_CH2CH	See Note (2)

Note (1):
Deliberately set DQ to DQS spacing to 3:1 to avoid adding complexity to contraints, even though it can be less. Only one rule per channel is needed by trading off a little space.

Note (2):
Intel suggests 25 mil (0.65 mm) spacing for via to channel, and via to pad to two different channels. DDR3 draws about 20 mA per trace with edge rates in the 100s of ps. The main coupling mechanism is capacitive. A 0.65 mm spacing is used for power nets, which draw far more current (inductive coupling however). These rules are far too conservative. To meet these rules, the spacing must be applied to the net.

Note (3):
In order for the constraints DDR_*_DQ_BYTE* to =SAME to win out over DDR_{A,B}_DQ_BYTE* to DDR_{A,B}_DQ_BYTE* so that the small intra-bytelane spacing is used, the spacing rule DDR_DQ2DQ must have a weight greater than DDR_BL2BL.

DDR3

Electrical Contraint Set	Physical	Spacing		
Channel A				
I17 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<1..0>	12 29
I17 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<1..0>	12 29
I25 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<3..2>	8 12
I25 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<3..2>	8 12
I18 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<1..0>	12 29
I18 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<1..0>	12 29
I18 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<1..0>	12 29
I24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<3..2>	8 12
I24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<3..2>	8 12
I24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<3..2>	8 12
I18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_A<15..0>	12 29
I18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_BA<2..0>	12 29
I18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_RAS_L	12 29
I18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_CAS_L	12 29
I18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_WE_L	12 29
I19 DDR_A_DQ_BYTE0	DDR_DQ_PHY	DDR_A_DQ_BYTE0	MEM_A_DQ<7..0>	12 31
I19 DDR_A_DQ_BYTE1	DDR_DQ_PHY	DDR_A_DQ_BYTE1	MEM_A_DQ<15..8>	12 31
I19 DDR_A_DQ_BYTE2	DDR_DQ_PHY	DDR_A_DQ_BYTE2	MEM_A_DQ<23..16>	12 31
I19 DDR_A_DQ_BYTE3	DDR_DQ_PHY	DDR_A_DQ_BYTE3	MEM_A_DQ<31..24>	12 31
I19 DDR_A_DQ_BYTE4	DDR_DQ_PHY	DDR_A_DQ_BYTE4	MEM_A_DQ<39..32>	12 31
I19 DDR_A_DQ_BYTE5	DDR_DQ_PHY	DDR_A_DQ_BYTE5	MEM_A_DQ<47..40>	12 31
I19 DDR_A_DQ_BYTE6	DDR_DQ_PHY	DDR_A_DQ_BYTE6	MEM_A_DQ<55..48>	12 31
I19 DDR_A_DQ_BYTE7	DDR_DQ_PHY	DDR_A_DQ_BYTE7	MEM_A_DQ<63..56>	12 31
I19 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_P<0>	12 31
I19 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_N<0>	12 31
I19 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_P<1>	12 31
I19 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_N<1>	12 31
I20 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_P<2>	12 31
I20 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_N<2>	12 31
I20 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_P<3>	12 31
I20 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_N<3>	12 31
I23 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_P<4>	12 31
I23 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_N<4>	12 31
I23 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_P<5>	12 31
I23 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_N<5>	12 31
I23 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_P<6>	12 31
I23 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_N<6>	12 31
I23 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_P<7>	12 31
I23 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_N<7>	12 31
Channel B				
I21 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<1..0>	12 30
I21 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<1..0>	12 30
I25 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<3..2>	8 12
I25 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<3..2>	8 12
I21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<1..0>	12 30
I21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<1..0>	12 30
I21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<1..0>	12 30
I26 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<3..2>	8 12
I26 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<3..2>	8 12
I26 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<3..2>	8 12
I21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_A<15..0>	12 30
I21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_BA<2..0>	12 30
I21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_RAS_L	12 30
I22 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_CAS_L	12 30
I22 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_WE_L	12 30
I22 DDR_B_DQ_BYTE0	DDR_DQ_PHY	DDR_B_DQ_BYTE0	MEM_B_DQ<7..0>	12 31
I22 DDR_B_DQ_BYTE1	DDR_DQ_PHY	DDR_B_DQ_BYTE1	MEM_B_DQ<15..8>	12 31
I22 DDR_B_DQ_BYTE2	DDR_DQ_PHY	DDR_B_DQ_BYTE2	MEM_B_DQ<23..16>	12 31
I22 DDR_B_DQ_BYTE3	DDR_DQ_PHY	DDR_B_DQ_BYTE3	MEM_B_DQ<31..24>	12 31
I22 DDR_B_DQ_BYTE4	DDR_DQ_PHY	DDR_B_DQ_BYTE4	MEM_B_DQ<39..32>	12 31
I22 DDR_B_DQ_BYTE5	DDR_DQ_PHY	DDR_B_DQ_BYTE5	MEM_B_DQ<47..40>	12 31
I22 DDR_B_DQ_BYTE6	DDR_DQ_PHY	DDR_B_DQ_BYTE6	MEM_B_DQ<55..48>	12 31
I22 DDR_B_DQ_BYTE7	DDR_DQ_PHY	DDR_B_DQ_BYTE7	MEM_B_DQ<63..56>	12 31
I23 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_P<0>	12 31
I23 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_N<0>	12 31
I23 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_P<1>	12 31
I23 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_N<1>	12 31
I23 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_P<2>	12 31
I23 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_N<2>	12 31
I23 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_P<3>	12 31
I23 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_N<3>	12 31
I23 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_P<4>	12 31
I23 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_N<4>	12 31
I24 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_P<5>	12 31
I24 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_N<5>	12 31
I24 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_P<6>	12 31
I24 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_N<6>	12 31
I24 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_P<7>	12 31
I24 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_N<7>	12 31
Reset				
I24	DDR_50S		MEM_RESET_L	28 29 30

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE: DDR3 Constraints

Apple Inc.

DRAWING NUMBER: 051-9179 SIZE: D
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BRANCH:
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PCI Express/DMI

PCIe-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
PCIE_COMP	*	Y	0.305 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE3_PHY	*	PCIE_80D
CLK_PCIE_PHY	*	PCIE_90D
COMP_PCIE_PHY	*	PCIE_COMP

PCIe and DMI Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
4-5	50	50	15	15.75	PCIe. Impedance inferred from Table 4-7.
4-7	50	50	8	15.75	DMI. Numbers based on Intel stack-up.

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_ISO	*	=5:1_SPACING	?
COMP_PCIE_ISO	*	=4:1_SPACING	?

Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	*	*	CLK_PCIE_ISO
COMP_PCIE	*	*	COMP_PCIE_ISO
PEG_R2D	PEG_R2D	*	PEG_SAME_DIR
PEG_D2R	PEG_D2R	*	PEG_SAME_DIR
PEG_D2R	PEG_R2D	*	PEG_ALT_DIR
PEG_D2R	*	*	PEG_ISO
PEG_R2D	*	*	PEG_ISO

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
PEG_SAME_DIR	*	=3.5X_DIELECTRIC	?
PEG_ALT_DIR	*	=7X_DIELECTRIC	?
PEG_ISO	*	=4:1_SPACING	?

PEG Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
4.2.1	80	80	16	15.75	PCIe Gen3. Allow looser spacing for same direction on stripline per Anil

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing	
x16 Graphics			
144D PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<15>
144J PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<15>
144J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<15>
144J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<15>
144C PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<15>
144G PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<15>
144G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<15>
144G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<15>
144D PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<14>
144E PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<14>
145C	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<14>
145C	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<14>
145D PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<14>
145C PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<14>
145C	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<14>
145C	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<14>
145F PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<13>
145G PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<13>
145G	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<13>
146G	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<13>
145G PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<13>
146G PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<13>
146G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<13>
146G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<13>
146C PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<12>
146G PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<12>
146J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<12>
146G	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<12>
146G PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<12>
147C PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<12>
146G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<12>
147A	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<12>
147J PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<11>
147J PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<11>
147J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<11>
147J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<11>
147J PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<11>
147J PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<11>
147J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<11>
147J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<11>
148C PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<10>
148E PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<10>
148J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<10>
148J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<10>
148C PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<10>
148E PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<10>
148J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<10>
148J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<10>
148F PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<9>
148G PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<9>
149J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<9>
149J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<9>
149F PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<9>
149G PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<9>
149J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<9>
149J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<9>
149C PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<8>
149E PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<8>
149J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<8>
149J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<8>
149C PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<8>
149E PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<8>
149J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<8>
149J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<8>

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing	
x16 Graphics			
150D PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<7>
150E PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<7>
150J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<7>
150J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<7>
150F PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<7>
150G PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<7>
151J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<7>
151J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<7>
151D PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<6>
151E PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<6>
151J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<6>
151J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<6>
151D PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<6>
151E PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<6>
151J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<6>
151J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<6>
152F PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<5>
152G PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<5>
152J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<5>
152J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<5>
152F PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<5>
152G PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<5>
152J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<5>
152J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<5>
152C PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<4>
152E PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<4>
153J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<4>
153J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<4>
153C PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<4>
153E PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<4>
153J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<4>
153J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<4>
153D PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<3>
153E PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<3>
153J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<3>
153J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<3>
154D PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<3>
154E PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<3>
154J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<3>
154J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<3>
154C PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<2>
154E PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<2>
154J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<2>
154J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<2>
154C PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<2>
154E PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<2>
154J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<2>
154J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<2>
155C PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<1>
155E PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<1>
155J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<1>
155J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<1>
155C PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<1>
155E PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<1>
155J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<1>
155J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<1>
156F PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<0>
156G PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<0>
156J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<0>
156J	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<0>
156F PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<0>
156G PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<0>
156J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<0>
156J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<0>
CPU PCIe Clocks			
166D PEG_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_P 9 18
166C PEG_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_N 9 18
CPU PCIe Compensation			
167K	COMP_PCIE_PHY	COMP_PCIE	CPU_PEG_COMP 10

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Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_PHY	*	PCIE_85D
COMP_DMI_PHY	*	50_OHM_SE

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_SAME_DIR	*	=3.5X_DIELECTRIC	?
PCIE_ALT_DIR	*	=7X_DIELECTRIC	?
PCIE_ISO	*	=4:1_SPACING	?

TBT x4 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_TBT_R2D	PCIE_TBT_R2D	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_D2R	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_R2D	*	PCIE_ALT_DIR
PCIE_TBT_D2R	*	*	PCIE_ISO
PCIE_TBT_R2D	*	*	PCIE_ISO

SSD x2 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_SSD_R2D	PCIE_SSD_R2D	*	PCIE_SAME_DIR
PCIE_SSD_D2R	PCIE_SSD_D2R	*	PCIE_SAME_DIR
PCIE_SSD_D2R	PCIE_SSD_R2D	*	PCIE_ALT_DIR
PCIE_SSD_D2R	*	*	PCIE_ISO
PCIE_SSD_R2D	*	*	PCIE_ISO

PCH x1 PCIE Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	PCIE_ISO

DMI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
DMI_SAME_DIR	*	=4X_DIELECTRIC	?
DMI_ALT_DIR	*	=5X_DIELECTRIC	?
DMI_ISO	*	=4X_DIELECTRIC	?

DMI x4 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_N2S	DMI_N2S	*	DMI_SAME_DIR
DMI_S2N	DMI_S2N	*	DMI_SAME_DIR
DMI_N2S	DMI_S2N	*	DMI_ALT_DIR
DMI_N2S	*	*	DMI_ISO
DMI_S2N	*	*	DMI_ISO

PCIe (PCH)

Electrical Contraint Set	Physical	Spacing		
x4 Thunderbolt				
PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_P<3..0>	34
PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_N<3..0>	34
	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_P<3..0>	18 34
	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_N<3..0>	18 34
PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_P<3..0>	18 34
PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_N<3..0>	18 34
	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_P<3..0>	34
	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_N<3..0>	34
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_P	18 34
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_N	18 34
x2 SSD				
PCIE_GEN2_R2D_CONN_SSD	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_P<1>	42
PCIE_GEN2_R2D_CONN_SSD	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_N<1>	42
	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_C_P<1>	18 42
	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_C_N<1>	18 42
PCIE_GEN2_D2R_CONN_SSD	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_P<1>	18 42
PCIE_GEN2_D2R_CONN_SSD	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_N<1>	18 42
	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_C_P<1>	42
	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_C_N<1>	42
PCIE_GEN2_R2D_MUX_SSD	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_P<0>	42
PCIE_GEN2_R2D_MUX_SSD	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_N<0>	42
	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_C_P<0>	18 42
	PCIE_PHY	PCIE_SSD_R2D	PCIE_SSD_R2D_C_N<0>	18 42
PCIE_GEN2_D2R_MUX_SSD	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_P<0>	18 42
PCIE_GEN2_D2R_MUX_SSD	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_N<0>	18 42
	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_C_P<0>	42
	PCIE_PHY	PCIE_SSD_D2R	PCIE_SSD_D2R_C_N<0>	42
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_P	18 42
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_N	18 42
x1 AirPort				
PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_P	33
PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_N	33
	PCIE_PHY	PCIE	PCIE_AP_R2D_C_P	18 33
	PCIE_PHY	PCIE	PCIE_AP_R2D_C_N	18 33
PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_P	18 33
PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_N	18 33
	PCIE_PHY	PCIE	PCIE_AP_D2R_C_P	
	PCIE_PHY	PCIE	PCIE_AP_D2R_C_N	
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_P	18 33
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_N	18 33
x1 Caesar IV				
PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_P	37
PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_N	37
	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_P	18 37
	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_N	18 37
PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_P	18 37
PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_N	18 37
	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_P	37
	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_N	37
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_P	18 37
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_N	18 37

DMI

Electrical Contraint Set	Physical	Spacing		
DMI				
DMI_N2S	PCIE_PHY	DMI_N2S	DMI_N2S_P<3..0>	10 19
DMI_N2S	PCIE_PHY	DMI_N2S	DMI_N2S_N<3..0>	10 19
DMI_S2N	PCIE_PHY	DMI_S2N	DMI_S2N_P<3..0>	10 19
DMI_S2N	PCIE_PHY	DMI_S2N	DMI_S2N_N<3..0>	10 19
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_P	11 18
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_N	11 18
DMI Compensation				
	COMP_DMI_PHY	COMP_PCIE	PCH_DMI_COMP	19

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SATA

SATA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SATA_PHY	*	SATA_90D
COMP_SATA_PHY	*	SATA_50S

SATA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ISO	*	=6:1_SPACING	?
COMP_SATA_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA	*	*	SATA_ISO
COMP_SATA	*	*	COMP_SATA_ISO

SATA Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
15.2.1	90	95	20	23.62	SATA Gen2, SATA Gen3

SATA Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
15-3	50	50	15	15.75	SATA Gen2, SATA Gen3

FDI

FDI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FDI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
COMP_FDI	*	Y	0.25 MM	0.25 MM	3 MM	=STANDARD	=STANDARD
FDI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
FDI_DIFF_PHY	*	FDI_85D
FDI_SE_PHY	*	FDI_50S
COMP_FDI_PHY	*	COMP_FDI

FDI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FDI_ISO	*	=3:1_SPACING	?
COMP_FDI_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FDI	*	*	FDI_ISO
COMP_FDI	*	*	COMP_FDI_ISO

FDI Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Table	Imp	Design	Iso	Design	Comments
6-1/6-2	85	85	12	11.81	FDI main length

FDI Compensation Rules (mils)

Table	Trace	Design	Iso	Design	Comments
6-4	10	11.81	-	15.75	Using PCIe guidelines

XDP

XDP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
XDP_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
XDP_PHY	*	XDP_55S

XDP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XDP_ISO	*	=2:1_SPACING	?
CLK_JTAG_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XDP	*	*	XDP_ISO
CLK_JTAG	*	*	CLK_JTAG_ISO

Desktop Debug Design Guide (Intel Doc# 430883)

Section	Imp	Design	Iso	Design	Comments
1.5	45-65	55	-	15.75	Isolation is for JTAG clocks. All signals default are 50 Ohm SE.

SATA

Electrical Contraint Set	Physical	Spacing		
PCH SATA Port 0 (HDD)				
T90 SATA_R2D	SATA_PHY	SATA	SATA_HDD_R2D_P	42
T92 SATA_R2D	SATA_PHY	SATA	SATA_HDD_R2D_N	42
T89	SATA_PHY	SATA	SATA_HDD_R2D_C_P	18 42
T91	SATA_PHY	SATA	SATA_HDD_R2D_C_N	18 42
T94 SATA_D2R	SATA_PHY	SATA	SATA_HDD_D2R_P	18 42
T95 SATA_D2R	SATA_PHY	SATA	SATA_HDD_D2R_N	18 42
T93	SATA_PHY	SATA	SATA_HDD_D2R_C_P	42
T93	SATA_PHY	SATA	SATA_HDD_D2R_C_N	42
PCH SATA Port 1 (SSD)				
T97 SATA_R2D_MUX_SSD	SATA_PHY	SATA	SATA_SSD_R2D_P	42
T99 SATA_R2D_MUX_SSD	SATA_PHY	SATA	SATA_SSD_R2D_N	42
T96	SATA_PHY	SATA	SATA_SSD_R2D_C_P	18 42
T98	SATA_PHY	SATA	SATA_SSD_R2D_C_N	18 42
T100 SATA_D2R_MUX_SSD	SATA_PHY	SATA	SATA_SSD_D2R_P	18 42
T102 SATA_D2R_MUX_SSD	SATA_PHY	SATA	SATA_SSD_D2R_N	18 42
T106	SATA_PHY	SATA	SATA_SSD_D2R_C_P	42
T104	SATA_PHY	SATA	SATA_SSD_D2R_C_N	42
SSD PCIe/SATA Mux Output				
T111 PCIE_SATA_R2D_MUX_CONN	SATA_PHY	SATA	PCIE_SATA_SSD_R2D_P	42
T110 PCIE_SATA_R2D_MUX_CONN	SATA_PHY	SATA	PCIE_SATA_SSD_R2D_N	42
T117 PCIE_SATA_D2R_MUX_CONN	SATA_PHY	SATA	PCIE_SATA_SSD_D2R_P	42
T116 PCIE_SATA_D2R_MUX_CONN	SATA_PHY	SATA	PCIE_SATA_SSD_D2R_N	42
PCH SATA Compensation				
T120	COMP_SATA_PHY	COMP_SATA	PCH_SATAICOMP	18
T109	COMP_SATA_PHY	COMP_SATA	PCH_SATA3COMP	18
T108	COMP_SATA_PHY	COMP_SATA	PCH_SATA3RBIAS	18

FDI

Electrical Contraint Set	Physical	Spacing		
FDI				
T120 FDI_TX	FDI_DIFF_PHY	FDI	CPU_FDI_TX_P<7..0>	9 10
T119 FDI_TX	FDI_DIFF_PHY	FDI	CPU_FDI_TX_N<7..0>	9 10
T113	FDI_SE_PHY	FDI	CPU_FDI_FSYNC<1..0>	9 10
T112	FDI_SE_PHY	FDI	CPU_FDI_LSYNC<1..0>	9 10
T115	FDI_SE_PHY	FDI	CPU_FDI_INT	9 10
FDI Compensation				
T121	COMP_FDI_PHY	COMP_FDI	CPU_FDI_COMPIO	10

XDP

Electrical Contraint Set	Physical	Spacing		
CPU XDP				
T37	XDP_PHY	XDP	XDP_BPM_L<7..0>	11 25
T38	XDP_PHY	XDP	CPU_CFG<17..0>	8 10 15 25
T39 ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_P	11 15
T40 ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_N	11 15
T41	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_P	15 18 25
T43	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_N	15 18 25
T42	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_P	25
T44	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_N	25
T45	XDP_PHY	CLK_JTAG	XDP_CPU_TCK	11 25
T46	XDP_PHY	XDP	XDP_CPU_TMS	11 25
T47	XDP_PHY	XDP	XDP_CPU_TDI	11 25
T48	XDP_PHY	XDP	XDP_CPU_TDO	11 25
PCH XDP				
T49	XDP_PHY	CLK_JTAG	XDP_PCH_TCK	18 25
T50	XDP_PHY	XDP	XDP_PCH_TMS	18 25
T51	XDP_PHY	XDP	XDP_PCH_TDI	18 25
T52	XDP_PHY	XDP	XDP_PCH_TDO	18 25

SYNC_MASTER=D7_MLB SYNC_DATE=01/19/2012

PAGE TITLE: SATA/FDI/XDP Constraints

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PCH

PCH-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

PCH-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	=4:1_SPACING	?
COMP_PCH	*	=2:1_SPACING	?

PCI

PCI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

PCI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCI	*	=2:1_SPACING	?

LPC

LPC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

LPC-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5:1_SPACING	?
CLK_LPC	*	=2:1_SPACING	?

HDA

HDA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

HDA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

Crystal

Crystal-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

Crystal-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

SPI

SPI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=2:1_SPACING	?

PCI

Electrical Contraint Set	Physical	Spacing		
PCI Clock				
H33J	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIIN	18 26
H32J	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIOUT	20 26

LPC

Electrical Contraint Set	Physical	Spacing		
LPC				
H33D	LPC_55S	LPC	LPC_AD<3..0>	18 45 47
H33B	LPC_55S	LPC	LPC_R_AD<3..0>	18
H33J	LPC_55S	LPC	LPC_FRAME_L	18 45 47
H33F	LPC_55S	LPC	LFRAME_L	18
LPC Clocks				
H33C	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	26 47
H34C	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	20 26
H34J	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	26 45
H34F	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	20 26

PCH Clocks

Electrical Contraint Set	Physical	Spacing		
PCH Reference Clock				
H38D	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_SB	26
H40D	CLK_PCH_55S	CLK_PCH	PCH_CLK25M_XTALIN	18 26
PCH Ref Clock Comp				
H34C	PCH_55S	COMP_PCH	PCH_XCLK_RCOMP	18
PCH RTC 32K				
H44J	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	18 26
H43J	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	18 26
H52J	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2_R	26
SMC 32K				
H24D	CLK_PCH_55S	CLK_PCH	PM_CLK32K_SUSCLK_R	19 46
H45D	CLK_PCH_55S	CLK_PCH	SMC_CLK32K	45 46

25 MHz Reference Clocks

Electrical Contraint Set	Physical	Spacing		
25M Reference Crystal				
H47J	CLK_XTAL	XTAL	SYSCLK_CLK25M_X1	26
H48D	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2	26
H48J	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2_R	26
25M Reference Clocks				
H48C	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_ENET	26 37
H48C	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_ENET_R	26
H49D	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_TBT	26 34
H49F	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_TBT_R	34

HDA

Electrical Contraint Set	Physical	Spacing		
HDA				
H35C	HDA_55S	HDA	HDA_BIT_CLK	18 53
H34C	HDA_55S	HDA	HDA_BIT_CLK_R	18
H36C	HDA_55S	HDA	HDA_RST_L	18 53
H36C	HDA_55S	HDA	HDA_RST_R_L	18
H46C	HDA_55S	HDA	HDA_SDOUT	18 53
H46C	HDA_55S	HDA	HDA_SDOUT_R	15 18
H60C	HDA_55S	HDA	HDA_SYNC	15 18 53
H60C	HDA_55S	HDA	HDA_SYNC_R	18
H60C	HDA_55S	HDA	HDA_SDIN0	18 53
H60C	HDA_55S	HDA	AUD_SDI_R	53
SPDIF				
H47C		HDA	AUD_SPDIF_CHIP	53
H47C		HDA	AUD_SPDIF_OUT	53 57

SPI Bootrom

Electrical Contraint Set	Physical	Spacing		
SPI ROM				
H49J	SPI_50S	SPI	SPI_CLK_R	18 47
H49C	SPI_50S	SPI	SPI_CLK	47
H49C	SPI_50S	SPI	SPI_ALT_CLK	47
H48C	SPI_50S	SPI	SPI_SMC_CLK	45 46
H48C	SPI_50S	SPI	SPI_MLB_CLK	46 47
H39C	SPI_50S	SPI	SPI_CS0_R_L	18 47
H39C	SPI_50S	SPI	SPI_CS0_L	47
H39C	SPI_50S	SPI	SPI_ALT_CS_L	47
H40C	SPI_50S	SPI	SPI_SMC_CS_L	45 46
H39J	SPI_50S	SPI	SPI_MLB_CS_L	46 47
H39C	SPI_50S	SPI	SPI_MOSI_R	18 47
H40C	SPI_50S	SPI	SPI_MOSI	47
H40J	SPI_50S	SPI	SPI_ALT_MOSI	47
H43C	SPI_50S	SPI	SPI_SMC_MOSI	45 46
H43J	SPI_50S	SPI	SPI_MLB_MOSI	46 47
H40C	SPI_50S	SPI	SPI_MISO	18 47
H40C	SPI_50S	SPI	SPI_ALT_MISO	47
H43C	SPI_50S	SPI	SPI_SMC_MISO	45 46
H43J	SPI_50S	SPI	SPI_MLB_MISO	46 47
H49C	SPI_50S	SPI	SPIROM_USE_MLB	21 47

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USB

USB-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB2_PHY	*	USB_90D
USB3_PHY	*	USB_85D

USB-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2_ISO	*	=3:1_SPACING	?
USB2_ISO	TOP,BOTTOM	=3:1_SPACING	?
USB3_ISO	*	=5.5:1_SPACING	?
USB3_ISO	TOP,BOTTOM	=5.5:1_SPACING	?

USB Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
12.2.1	90	90	12	11.81	USB 2.0
13.3.1	85	85	20	21.65	USB 3.0

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB2	*	*	USB2_ISO
USB3	*	*	USB3_ISO

Caesar IV (Ethernet/SD)

CIV-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_COMP_PHY	*	ENET_50S
ENET_DIFF_PHY	*	ENET_100D
SD_PHY	*	SD_50S
CIV_SPI	*	SPI_55S

CIV-specific Spacing Definitions
Ethernet

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF_ISO	*	=6:1_SPACING	?
ENET_DIFF2DIFF	*	=3:1_SPACING	?
ENET_TRANS_ISO	*	1.27 MM	?
COMP_ENET_ISO	*	=4:1_SPACING	?

Constraints
Ethernet

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	*	*	ENET_DIFF_ISO
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_TRANS	*	*	ENET_TRANS_ISO
COMP_ENET	*	*	COMP_ENET_ISO
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF

2 kV isolation

SD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_ISO	*	=3:1_SPACING	?

SD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SD	*	*	SD_ISO

Camera Processor-to-Camera Sensor I/F (SMIA/MIPI)

Camera Processor's SMIA Interface Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMIA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMIA_DIFF_PHY	*	SMIA_100D

Camera Processor's SMIA Interface Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMIA_DIFF_ISO	*	=6:1_SPACING	?
SMIA_DIFF2DIFF	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMIA_DIFF	*	*	SMIA_DIFF_ISO
SMIA_DIFF	SMIA_DIFF	*	SMIA_DIFF2DIFF

USB 3.0 and USB 2.0 Trixies Muxing

Electrical Contraint Set	Physical	Spacing		
External Port A (J4600)				
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_P	43
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_N	43
	USB3_PHY	USB3	USB3_EXTA_RX_F_P	20 43
	USB3_PHY	USB3	USB3_EXTA_RX_F_N	20 43
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_P	20 43
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_N	20 43
	USB3_PHY	USB3	USB3_EXTA_TX_F_P	43
	USB3_PHY	USB3	USB3_EXTA_TX_F_N	43
	USB3_PHY	USB3	USB3_EXTA_TX_C_P	43
	USB3_PHY	USB3	USB3_EXTA_TX_C_N	43
USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_PCH_0_P	20 43
USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_PCH_0_N	20 43
	USB2_PHY	USB2	USB2_EXTA_MUXED_P	43
	USB2_PHY	USB2	USB2_EXTA_MUXED_N	43
	USB2_PHY	USB2	USB2_EXTA_P	43
	USB2_PHY	USB2	USB2_EXTA_N	43
External Port B (J4610)				
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_P	43
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_N	43
	USB3_PHY	USB3	USB3_EXTB_RX_F_P	20 43
	USB3_PHY	USB3	USB3_EXTB_RX_F_N	20 43
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_P	20 43
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_N	20 43
	USB3_PHY	USB3	USB3_EXTB_TX_F_P	43
	USB3_PHY	USB3	USB3_EXTB_TX_F_N	43
	USB3_PHY	USB3	USB3_EXTB_TX_C_P	43
	USB3_PHY	USB3	USB3_EXTB_TX_C_N	43
USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_1_P	20 43
USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_1_N	20 43
	USB2_PHY	USB2	USB_PCH_9_P	20 43
	USB2_PHY	USB2	USB_PCH_9_N	20 43
	USB2_PHY	USB2	USB2_EXTB_MUXED_P	43
	USB2_PHY	USB2	USB2_EXTB_MUXED_N	43
	USB2_PHY	USB2	USB2_EXTB_P	43
	USB2_PHY	USB2	USB2_EXTB_N	43
External Port C (J4700)				
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_P	44
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_N	44
	USB3_PHY	USB3	USB3_EXTC_RX_F_P	20 44
	USB3_PHY	USB3	USB3_EXTC_RX_F_N	20 44
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_P	20 44
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_N	20 44
	USB3_PHY	USB3	USB3_EXTC_TX_F_P	44
	USB3_PHY	USB3	USB3_EXTC_TX_F_N	44
	USB3_PHY	USB3	USB3_EXTC_TX_C_P	44
	USB3_PHY	USB3	USB3_EXTC_TX_C_N	44
USB2_CONN	USB2_PHY	USB2	USB_PCH_2_P	20 44
USB2_CONN	USB2_PHY	USB2	USB_PCH_2_N	20 44
	USB2_PHY	USB2	USB2_EXTC_P	44
	USB2_PHY	USB2	USB2_EXTC_N	44
External Port D (J4710)				
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_P	44
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_N	44
	USB3_PHY	USB3	USB3_EXTD_RX_F_P	20 44
	USB3_PHY	USB3	USB3_EXTD_RX_F_N	20 44
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_P	20 44
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_N	20 44
	USB3_PHY	USB3	USB3_EXTD_TX_F_P	44
	USB3_PHY	USB3	USB3_EXTD_TX_F_N	44
	USB3_PHY	USB3	USB3_EXTD_TX_C_P	44
	USB3_PHY	USB3	USB3_EXTD_TX_C_N	44
USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_3_P	20 44
USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_3_N	20 44
	USB2_PHY	USB2	USB_PCH_10_P	20 44
	USB2_PHY	USB2	USB_PCH_10_N	20 44
	USB2_PHY	USB2	USB2_EXTD_MUXED_P	44
	USB2_PHY	USB2	USB2_EXTD_MUXED_N	44
	USB2_PHY	USB2	USB2_EXTD_P	44
	USB2_PHY	USB2	USB2_EXTD_N	44
Camera (J3510)				
USB2_CONN_TNT	USB2_PHY	USB2	USB_CAMERA_P	40
USB2_CONN_TNT	USB2_PHY	USB2	USB_CAMERA_N	40
PCH USB Compensation				
	PCH_55S	COMP_PCH	PCH_USB_RBIAS	20

RMH Love

Electrical Contraint Set	Physical	Spacing		
USB 2.0 Hub				
USB2_HUB	USB2_PHY	USB2	USB_PCH_7_P	20 27
USB2_HUB	USB2_PHY	USB2	USB_PCH_7_N	20 27
USB2_HUB_CONN	USB2_PHY	USB2	USB_BT_P	27 33
USB2_HUB_CONN	USB2_PHY	USB2	USB_BT_N	27 33
USB2_HUB_CONN	USB2_PHY	USB2	USB_BT_MUX_P	33
USB2_HUB_CONN	USB2_PHY	USB2	USB_BT_MUX_N	33
USB2_HUB_RES	USB2_PHY	USB2	USB_SMC_P	27 45
USB2_HUB_RES	USB2_PHY	USB2	USB_SMC_N	27 45
	USB2_PHY	USB2	USB_HUB_2_P	27
	USB2_PHY	USB2	USB_HUB_2_N	27
USB 2.0 Hub Compensation				
	PCH_55S	COMP_PCH	USB_HUB_RBIAS	27
USB 2.0 Hub Crystal				
	CLK_XTAL	XTAL	USB_HUB_XTAL1	27
	CLK_XTAL	XTAL	USB_HUB_XTAL2	27

Et tu Brute?

Electrical Contraint Set	Physical	Spacing		
Ethernet				
ENET_MDI	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_P<3..0>	37 38
ENET_MDI	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_N<3..0>	37 38
	ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_P<3..0>	38
	ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_N<3..0>	38
		ENET_TRANS	ENETCONN_MCT0	38
		ENET_TRANS	ENETCONN_MCT1	38
		ENET_TRANS	ENETCONN_MCT2	38
		ENET_TRANS	ENETCONN_MCT3	38
		ENET_TRANS	ENETCONN_MCT_BS	38
	ENET_COMP_PHY	COMP_ENET	ENET_RDAC	37
SD				
SD_DATA	SD_PHY	SD	ENET_CR_DATA<7..0>	37
	SD_PHY	SD	SDCONN_DATA<7..0>	37 39
	SD_PHY	SD	SDCONN_DATA_R <7..0>	39
SD_CMD	SD_PHY	SD	ENET_SD_CMD	37
	SD_PHY	SD	SDCONN_CMD	37 39
	SD_PHY	SD	SDCONN_CMD_R	39
SD_CLK	SD_PHY	SD	ENET_SD_CLK	37
	SD_PHY	SD	SDCONN_CLK	37 39
	SD_PHY	SD	SDCONN_CLK_R	39
	SD_PHY	SD	ENET_MEDIA_SENSE	15 18 37
	SD_PHY	SD	ENET_SD_DETECT_L	37 39
	SD_PHY	SD	SDCONN_WP	37 39
CIV SPI				
	CIV_SPI	SPI	ENET_SCLK	37
	CIV_SPI	SPI	ENET_MISO	37
	CIV_SPI	SPI	ENET_MOSI	37
	CIV_SPI	SPI	ENET_CS_L	37

Camera Processor-Camera Sensor I/F

Electrical Contraint Set	Physical	Spacing		
SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_P	40
SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_N	40
SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_F_P	40
SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_F_N	40
SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_P	40
SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_N	40
SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_F_P	40
SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_F_N	40
	SPI_50S	SPI	CAM_SF_CLK	40
	SPI_50S	SPI	CAM_SF_CLK_R	40
	SPI_50S	SPI	CAM_SF_DIN	40
	SPI_50S	SPI	CAM_SF_DIN_R	40
	SPI_50S	SPI	CAM_SF_CS_L	40
	SPI_50S	SPI	CAM_SF_WP_L	40
	SPI_50S	SPI	CAM_SF_DOUT	40
	SPI_50S	SPI	CAM_SF_DOUT_R	40
	SMB_PHY	SMB	I2C_CAMSENSOR_SDA	40
	SMB_PHY	SMB	I2C_CAMSENSOR_SCL	40

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SMBus

SMBus-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_PHY	*	SMB_55S

SMBus-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB_ISO	*	=2x_DIELECTRIC	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SMB_ISO

Sensor

Sensor-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_DIFF_PHY	*	1:1_DIFFPAIR

Sensor-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SENSE	*	*	SENSE_ISO
SENSE	POWER	*	PWR_P2MM
SENSE	GND	*	GND_P2MM

SMBus

Electrical Contraint Set	Physical	Spacing		
SMC				
I10	SMB_PHY	SMB	SMBUS_SMC_0_S0_SCL	45 48
I9	SMB_PHY	SMB	SMBUS_SMC_0_S0_SDA	45 48
I11	SMB_PHY	SMB	SMBUS_SMC_1_S0_SCL	45 48
I12	SMB_PHY	SMB	SMBUS_SMC_1_S0_SDA	45 48
I13	SMB_PHY	SMB	SMBUS_SMC_2_S4_SCL	45 48
I14	SMB_PHY	SMB	SMBUS_SMC_2_S4_SDA	45 48
I15	SMB_PHY	SMB	SMBUS_SMC_3_SCL	45 48
I16	SMB_PHY	SMB	SMBUS_SMC_3_SDA	45 48
I19	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SCL	45 46
I20	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SDA	45 46
PCH				
I51	TBT_I2C_5SS	TBT_I2C	SMBUS_PCH_CLK	18 48
I52	TBT_I2C_5SS	TBT_I2C	SMBUS_PCH_DATA	18 48
I53	SMB_PHY	SMB	SML_PCH_0_CLK	18 48
I54	SMB_PHY	SMB	SML_PCH_0_DATA	18 48
Display TCon				
I55	SMB_PHY	SMB	SMB_DP_TCON_SCL	48 72
I66	SMB_PHY	SMB	SMB_DP_TCON_SDA	48 72

Temperature Sense

Electrical Contraint Set	Physical	Spacing		
EMC1414-1 (Production)				
I57 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_1_P	51
I58 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_1_N	51
I59 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_2_P	51
I60 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_2_N	51
I65 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_P	6 51
I66 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_N	6 51
TMP423 (Development)				
I67 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_1_P	51
I68 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_1_N	51
I69 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_2_P	51
I70 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_2_N	51
I61 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_SKIN_P	51
I62 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_SKIN_N	51
I71 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_3_P	51
I72 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_3_N	51
HDD Out-of-Band				
I73		SENSE	SMC_HDD_OOB_TEMP	
I74		SENSE	HDD_OOB_TEMP_CONN	
I75		SENSE	HDD_OOB_TEMP_FILT	
I76		SENSE	HDD_OOB_TEMP_R	
SSD Out-of-Band				
I77		SENSE	SMC_SSD_OOB_TEMP	
I78		SENSE	SMC_SSD_TEMP_CTL	
I79		SENSE	SSD_OOB_TEMP	

SMC

Electrical Contraint Set	Physical	Spacing		
SMC				
I1	CLK_XTAL	XTAL	SMC_XTAL	45 46
I2	CLK_XTAL	XTAL	SMC_EXTAL	45 46

Current/Voltage Sense

Electrical Contraint Set	Physical	Spacing		
Common				
I3		SENSE	GND_SMC_AVSS	45 46 49 50
12V S5 (System Total)				
I4 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_P	49
I5 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_N	49
I6		SENSE	ISNS_P12VG3H_R	49
I7		SENSE	ISNS_P12VG3H	46 49
I8		SENSE	VSNS_P12VG3H	46 49
12V S0 (GPU Core)				
I22 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUCORE_P	
I23 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUCORE_N	
I24		SENSE	ISNS_P12VS0_GPUCORE_R	
I25		SENSE	ISNS_P12VS0_GPUCORE	46
I26		SENSE	VSNS_P12VS0_GPUCORE	46
HDD				
I80 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_HDD_P	49
I82 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_HDD_N	49
I83		SENSE	ISNS_HDDS0_R	49
I89		SENSE	ISNS_HDDS0	46 49
I84		SENSE	VSNS_HDDS0	46 49
SSD				
I85 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_P	50
I87 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_N	50
I86		SENSE	ISNS_SSDS0_R	50
I88		SENSE	ISNS_SSDS0	46 50
I89		SENSE	VSNS_SSDS0	46 50
VDDQ S3 (DDR)				
I33 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_VDDQS3_DDR_P	50
I32 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_VDDQS3_DDR_N	50
I35		SENSE	ISNS_VDDQS3_DDR_R	50
I34		SENSE	ISNS_VDDQS3_DDR	46 50
I36		SENSE	VSNS_VDDQS3_DDR	46 50
VDDQ S0 (GPU Uncore)				
I37 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUUC_P	
I38 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUUC_N	
I39		SENSE	ISNS_P12VS0_GPUUC_R	
I40		SENSE	ISNS_P12VS0_GPUUNCORE	46
I41		SENSE	VSNS_P12VS0_GPUUNCORE	46
CPU Core				
I42 SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_CPUCORE_P	49
I43 SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_CPUCORE_N	49
I44		SENSE	ISNS_CPUCORE_FB	49
I45		SENSE	ISNS_CPUCORE	46 49
I46		SENSE	VSNS_CPUCORE	46 49
CPU AXG				
I47 SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_CPUAXG_P	49
I48 SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_CPUAXG_N	49
I49		SENSE	ISNS_CPUAXG_FB	49
I50		SENSE	ISNS_CPUAXG	46 49
I51		SENSE	VSNS_CPUAXG	46 49

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DC-DC

Power-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GND_P3MM	*	Y	0.300 MM	0.150 MM	3.0 MM	=STANDARD	=STANDARD
GND_P5MM	*	Y	0.500 MM	0.150 MM	3.0 MM	=STANDARD	=STANDARD
POWER_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
POWER_P3MM	*	Y	0.300 MM	0.150 MM	3.0 MM	=STANDARD	=STANDARD
POWER_P6MM	*	Y	0.600 MM	0.150 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND	*	GND_P5MM
GND	BGA	GND_P3MM
POWER	*	POWER_P6MM
POWER	BGA	POWER_P3MM
VR_CTL_PHY	*	POWER_P3MM
VR_CTL_PHY	BGA	STANDARD
VR_VID_PHY	*	POWER_50S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VR_DIDT_PHY	*	POWER_P6MM
VR_DIDT_PHY	BGA	STANDARD

Power-specific Spacing Definitions
Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_ISO	*	=STANDARD	?
GND_ISO	*	=STANDARD	?

Constraints
Power and Common

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	POWER_ISO
GND	*	*	GND_ISO

DC-DC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SWNODE_ISO	*	=8:1_SPACING	1000
SWNODE_SW2SW	*	=1:1_SPACING	?
SWNODE_SW2PWR	*	=2:1_SPACING	?
SWNODE_SW2GND	*	=2:1_SPACING	?

DC-DC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_SWITCH	*	*	SWNODE_ISO
VR_SWITCH	*	BGA	BGA_P1MM
VR_SWITCH	VR_SWITCH	*	SWNODE_SW2SW
VR_SWITCH	POWER	*	SWNODE_SW2PWR
VR_SWITCH	GND	*	SWNODE_SW2GND

DC-DC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_ISO	*	=3:1_SPACING	?
VR_VID_ISO	*	=4X_DIELECTRIC	?

DC-DC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CTL	*	*	VR_CTL_ISO
VR_VID	*	*	VR_VID_ISO

VDDQ S3 (1.5V)/VTT S0

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
143	POWER	POWER	5V			REG_V5IN_U7700	69
Local Ground							
144	GND	GND	0V			AGND_VDDQS3	69
VDDQ S3							
145	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3	69
146	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3_L	69
147	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_VDDQS3	69
148	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_VDDQS3_RC	69
149	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3	69
150	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3_R	69
152	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_VDDQS3	69
151	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_VDDQS3	69
154	POWER	POWER	1.5V			PPVDDQ_S3_SENSE	
153	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VDDQSNS	69
155	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VREF	69
156	VR_CTL_PHY	VR_CTL				REG_VDDQS3_REFIN	69
157	VR_CTL_PHY	VR_CTL				REG_VDDQS3_MODE	69
158	VR_CTL_PHY	VR_CTL				REG_VDDQS3_TRIP	69
160	VR_CTL_PHY	VR_CTL				LDO_DDRVTTS0_SNS	69
Output Bus							
162	POWER	POWER	1.5V			PPVDDQ_S3	6
161	POWER_DDR	POWER_DDR	0.75V			PPDDRVTT_S3	6
163	POWER_DDR	POWER_DDR	0.75V			PPDDRVTT_S0	6
FET Switched							
164	POWER	POWER	1.5V			PP1V5_S0	6
Sensed							
165	POWER	POWER	1.5V			PPVDDQ_S3_DDR	6

CPU VccIO/ PCH 1.05V S0

	Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus								
I1		POWER	POWER	5V			REG_VCC_U7400	66
I2		POWER	POWER	5V			REG_PVCC_U7400	66
Local Ground								
I3		GND	GND	0V			AGND_P1V05S0	66
1.05V S0								
I5		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0	66
I4		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0_L	66
I7		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V05S0	66
I6		VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P1V05S0_RC	66
I8		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0	66
I9		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0_R	66
I10		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P1V05S0	66
I12		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P1V05S0	66
I11		VR_CTL_PHY	VR_CTL				REG_P1V05S0_OCSET	66
I14		VR_CTL_PHY	VR_CTL				REG_P1V05S0_VO	66
I13	VSNS_CPU_VCCIO	SNS_DIFF_PHY	SENSE				SNS_CPU_VCCIO_P	13 66
I15	VSNS_CPU_VCCIO	SNS_DIFF_PHY	SENSE				SNS_CPU_VCCIO_N	13 66
I16		SNS_DIFF_PHY	SENSE				SNS_P1V05S0_XW_P	66
I17		SNS_DIFF_PHY	SENSE				SNS_P1V05S0_XW_N	66
I19			SENSE				REG_P1V05S0_FB	66
I18			SENSE				REG_P1V05S0_RTN	66
I21		VR_CTL_PHY	VR_CTL				REG_P1V05S0_SREF	66
I20		VR_CTL_PHY	VR_CTL				REG_P1V05S0_FSEL	66
Output Bus								
I22		POWER	POWER	1.05V			PP1V05_S0	6
FET Switched								
I23		POWER	POWER	1.05V			PP1V05_TBTLC	6
I66		POWER	POWER	1.05V			PP1V05_TBTCIO	6

CPU VccSA

	Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus								
I24		POWER	POWER	5V			REG_VCC_U7500	67
I25		POWER	POWER	5V			REG_PVCC_U7500	67
Local Ground								
I26		GND	GND	0V			AGND_VCCSAS0	67
VCCIO								
I27		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VCCSAS0	67
I28		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_VCCSAS0	67
I29		VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_VCCSAS0_RC	67
I31		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VCCSAS0	67
I30		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_VCCSAS0	67
I33		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_VCCSAS0	67
I32		VR_CTL_PHY	VR_CTL				REG_VCCSAS0_OCSET	67
I35		VR_CTL_PHY	VR_CTL				REG_VCCSAS0_VO	67
I34			SENSE				SNS_CPU_VCCSA	13 67
I37	VSNS_CPU_VCCSA	SNS_DIFF_PHY	SENSE				SNS_VCCSAS0_XW_P	67
I36	VSNS_CPU_VCCSA	SNS_DIFF_PHY	SENSE				SNS_VCCSAS0_XW_N	67
I38			SENSE				REG_VCCSAS0_FB	67
I39			SENSE				REG_VCCSAS0_RTN	67
I40		VR_CTL_PHY	VR_CTL				REG_VCCSAS0_SREF	67
I41		VR_CTL_PHY	VR_CTL				REG_VCCSAS0_FSEL	67
Output Bus								
I42		POWER	POWER	0.925V			PPVCCSA_S0	6

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CPU Core Phases

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
H10	POWER	POWER	12V			PP12V_S0_CPUCORE_FLT	63 64 65
H11	POWER	POWER	5V			REG_VCC_U7100	63
Local Ground							
H20	GND	GND	0V			AGND_CPU	63 64 65
Phase 1							
H35	POWER	POWER	12V			REG_LVCC_U7210	64
H36	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_1	63 64
H38	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_1_R	63
H37	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_1	64
H39	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_1	64
H40	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_1_RC	64
H38	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_1	64
H39	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUCORE_1	64
H42	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUCORE_1	64
H43	POWER	POWER	1.1V			PPCPUCORE_S0_SENSE_1	64
H44	SNS_DIFF_PHY	SENSE				REG_ISENCORE_1_P	63 64
H45	SNS_DIFF_PHY	SENSE				REG_ISENCORE_1_N	64
H46		SENSE				REG_ISENCORE_1_NR	63 64
Phase 2							
H48	POWER	POWER	12V			REG_LVCC_U7230	64
H49	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_2	63 64
H51	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_2_R	63
H50	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_2	64
H52	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_2	64
H53	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_2_RC	64
H54	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_2	64
H55	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUCORE_2	64
H56	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUCORE_2	64
H57	POWER	POWER	1.1V			PPCPUCORE_S0_SENSE_2	64
H58	SNS_DIFF_PHY	SENSE				REG_ISENCORE_2_P	63 64
H59	SNS_DIFF_PHY	SENSE				REG_ISENCORE_2_N	64
H60		SENSE				REG_ISENCORE_2_NR	63 64
Phase 3							
H62	POWER	POWER	12V			REG_LVCC_U7250	64
H63	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_3	63 64
H64	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_3_R	63
H65	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_3	64
H66	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_3	64
H67	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_3_RC	64
H68	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_3	64
H69	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUCORE_3	64
H70	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUCORE_3	64
H71	POWER	POWER	1.1V			PPCPUCORE_S0_SENSE_3	64
H72	SNS_DIFF_PHY	SENSE				REG_ISENCORE_3_P	63 64
H73	SNS_DIFF_PHY	SENSE				REG_ISENCORE_3_N	64
H74		SENSE				REG_ISENCORE_3_NR	63 64

CPU AXG Phase and Core Controller

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
AXG							
H11	POWER	POWER	12V			REG_LVCC_U7330	65
H13	VR_CTL_PHY	VR_CTL				REG_PWM_CPUAXG	63 65
H14	VR_CTL_PHY	VR_CTL				REG_PWM_CPUAXG_R	63
H15	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUAXG	65
H16	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUAXG	65
H17	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUAXG_RC	65
H18	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUAXG	65
H19	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUAXG	65
H21	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUAXG	65
H22	POWER	POWER	1.1V			PPCPUAXG_S0_SENSE	65
H23 TSNS_CPU_AXG	SNS_DIFF_PHY	SENSE				REG_ISENAXG_P	65
H24 TSNS_CPU_AXG	SNS_DIFF_PHY	SENSE				REG_ISENAXG_N	65
H25		SENSE				REG_ISENAXG_PR	63 65
H26		SENSE				REG_ISENAXG_NR	63 65
ISL6364							
H92	VR_CTL_PHY	VR_CTL				REG_CPUCORE_COMP	63
H93	VR_CTL_PHY	VR_CTL				CPUCORE_COMP_RC	63
H94	VR_CTL_PHY	VR_CTL				REG_CPUCORE_FB	63
H95	VR_CTL_PHY	VR_CTL				CPUCORE_FB_RC	63
H96	VR_CTL_PHY	VR_CTL				CPUCORE_FB_R_1	63
H97	VR_CTL_PHY	VR_CTL				CPUCORE_FB_R_2	63
H98	VR_CTL_PHY	VR_CTL				CPUCORE_PSICOMP_RC	63
H99	VR_CTL_PHY	VR_CTL				REG_CPUCORE_PSICOMP	63
H100	VR_CTL_PHY	VR_CTL				REG_CPUCORE_HFCOMP	63
H101 VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VCORE_P	13 63
H102 VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VCORE_N	13 63
H103	SNS_DIFF_PHY	SENSE				SNS_VCORE_R_P	63
H104	SNS_DIFF_PHY	SENSE				SNS_VCORE_R_N	63
H105	SNS_DIFF_PHY	SENSE	1.1V			SNS_VCORE_XW_P	63
H106	SNS_DIFF_PHY	SENSE	0V			SNS_VCORE_XW_N	63
H107		SENSE				REG_CPUCORE_VSEN	63
H108		SENSE				REG_CPUCORE_RGND	63
H109	VR_CTL_PHY	VR_CTL				REG_CPUCORE_IMON	49 63
H110	VR_CTL_PHY	VR_CTL				CPUCORE_IMON_R	63
H111	VR_CTL_PHY	VR_CTL				REG_CPUCORE_TM	63
H112	VR_CTL_PHY	VR_CTL				REG_CPUCORE_SUTH	63
H113	VR_CTL_PHY	VR_CTL				REG_CPUCORE_NPSI	63
H114	VR_CTL_PHY	VR_CTL				REG_CPUCORE_FDVID	63
H115	VR_CTL_PHY	VR_CTL				REG_CPUCORE_IAUTO	63
H116	VR_CTL_PHY	VR_CTL				REG_CPUCORE_SW_FREQ	63
H117	VR_CTL_PHY	VR_CTL				REG_CPUCORE_RAMPADJ	63
H118	VR_CTL_PHY	VR_CTL				REG_CPUCORE_EN_PWR	63
H119	VR_CTL_PHY	VR_CTL				CPUCORE_EN_PWR_R	63
H120	VR_CTL_PHY	VR_CTL				REG_CPUCORE_RSET	63
H121	VR_CTL_PHY	VR_CTL				REG_CPUAXG_COMP	63
H122	VR_CTL_PHY	VR_CTL				CPUAXG_COMP_RC	63
H123	VR_CTL_PHY	VR_CTL				REG_CPUAXG_FB	63
H124	VR_CTL_PHY	VR_CTL				CPUAXG_FB_RC	63
H125	VR_CTL_PHY	VR_CTL				CPUAXG_FB_R_1	63
H126	VR_CTL_PHY	VR_CTL				CPUAXG_FB_R_2	63
H127	VR_CTL_PHY	VR_CTL				REG_CPUAXG_HFCOMP	63
H128 VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VAXG_P	13 63
H129 VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VAXG_N	13 63
H130	SNS_DIFF_PHY	SENSE				SNS_VAXG_R_P	63
H131	SNS_DIFF_PHY	SENSE				SNS_VAXG_R_N	63
H132	SNS_DIFF_PHY	SENSE	1.1V			SNS_VAXG_XW_P	63
H133	SNS_DIFF_PHY	SENSE	0V			SNS_VAXG_XW_N	63
H134		SENSE				REG_CPUAXG_VSEN	63
H135		SENSE				REG_CPUAXG_RGND	63
H136	VR_CTL_PHY	VR_CTL				REG_CPUAXG_IMON	49 63
H137	VR_CTL_PHY	VR_CTL				CPUAXG_IMON_R	63
H138	VR_CTL_PHY	VR_CTL				REG_CPUAXG_TM	63
H139	VR_CTL_PHY	VR_CTL				REG_CPUAXG_TCOMP	63
H140	VR_CTL_PHY	VR_CTL				REG_CPUAXG_SW_FREQ	63
H141	VR_VID_PHY	VR_VID				CPU_VIDSCLK	13 63
H142	VR_VID_PHY	VR_VID				CPU_VIDSCLK_R	13
H143	VR_VID_PHY	VR_VID				CPU_VIDALERT_L	13 63
H144	VR_VID_PHY	VR_VID				CPU_VIDALERT_R_L	13
H145	VR_VID_PHY	VR_VID				CPU_VIDSOUT	13 63
H146	VR_VID_PHY	VR_VID				CPU_VIDSOUT_R	13
Output Bus							
H147	POWER	POWER	1.1V			PPVCORE_S0_CPU	6
H148	POWER	POWER	1.1V			PPVAXG_S0	6

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GPU Core Phases and Controller

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
U120	POWER	POWER	12V			REG_PVCC_U8900
U120	POWER	POWER	5V			REG_VCC_U8900
Phase 1						
U127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_1
U127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_1
U127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_1_RC
U127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_1
U127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_1
U127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_ISEN_GPUCORE_1
U127	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_GPUCORE_1
Phase 2						
U120	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_2
U120	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_2
U130	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_2_RC
U130	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_2
U130	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_2
U130	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_ISEN_GPUCORE_2
U130	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_GPUCORE_2
ISL6568						
U127	VR_CTL_PHY	VR_CTL				REG_GPUCORE_ICOMP
U127	VR_CTL_PHY	VR_CTL				REG_GPUCORE_OCSET
U120	VR_CTL_PHY	VR_CTL				GPUCORE_ICOMP_R
U120	VR_CTL_PHY	VR_CTL				REG_GPUCORE_IREF
U120	VR_CTL_PHY	VR_CTL				REG_GPUCORE_ISUM
U120	VR_CTL_PHY	VR_CTL				REG_GPUCORE_COMP
U120	VR_CTL_PHY	VR_CTL				GPUCORE_COMP_RC
U120	VR_CTL_PHY	VR_CTL				REG_GPUCORE_VDIFF
U131	VR_CTL_PHY	VR_CTL				GPUCORE_VDIFF_R
U131	VR_CTL_PHY	VR_CTL				GPUCORE_VDIFF_RC
U131	VR_CTL_PHY	VR_CTL				REG_GPUCORE_FB
U130 VSNS_GPU_CORE	SNS_DIFF_PHY	SENSE				SNS_GPU_CORE_P
U130 VSNS_GPU_CORE	SNS_DIFF_PHY	SENSE				SNS_GPU_CORE_N
U131		SENSE				REG_GPUCORE_VSEN
U131		SENSE				REG_GPUCORE_RGND
U131	VR_VID_PHY	VR_VID				REG_GPUCORE_VID4
U131	VR_VID_PHY	VR_VID				REG_GPUCORE_VID3
U131	VR_VID_PHY	VR_VID				REG_GPUCORE_VID2
U131	VR_VID_PHY	VR_VID				REG_GPUCORE_VID1
U132	VR_VID_PHY	VR_VID				REG_GPUCORE_VID0
U132	VR_CTL_PHY	VR_CTL				REG_GPUCORE_MODE
U132	VR_CTL_PHY	VR_CTL				REG_GPUCORE_REF
U132	VR_CTL_PHY	VR_CTL				REG_GPUCORE_OFS
U132	VR_CTL_PHY	VR_CTL				REG_GPUCORE_FS
Output Bus						
U120	POWER	POWER	1.0V			PPVCORE_S0_GPU

GPU 1.05V S0

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
U139	POWER	POWER	5V			REG_VCC_U8300
Local Ground						
U139	GND	GND	0V			P1V05_GPU_AGND
1.05V S0						
U138	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPU_P1V05S0
U138	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPU_P1V05S0_L
U140	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPU_P1V05S0
U140	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPU_P1V05S0_RC
U140	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPU_P1V05S0
U140	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPU_P1V05S0_R
U140	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPU_P1V05S0
U141	VR_CTL_PHY	VR_CTL				REG_GPU_P1V05S0_OCSET_R
U141	VR_CTL_PHY	VR_CTL				REG_GPU_P1V05S0_VO_R
U140	VR_CTL_PHY	VR_CTL				REG_GPU_P1V05S0_OCSET
U140	VR_CTL_PHY	VR_CTL				REG_GPU_P1V05S0_VO
U140 VSNS_GPU_P1V05	SNS_DIFF_PHY	SENSE				SNS_GPU_PEX_IOVDD_P
U140 VSNS_GPU_P1V05	SNS_DIFF_PHY	SENSE				SNS_GPU_PEX_IOVDD_N
U141		SENSE				REG_GPU_P1V05S0_FB
U141		SENSE				REG_GPU_P1V05S0_RTN
U141	VR_CTL_PHY	VR_CTL				REG_GPU_P1V05S0_SREF
U141	VR_CTL_PHY	VR_CTL				REG_GPU_P1V05S0_FSEL
Output Bus						
U141	POWER	POWER	1.05V			PP1V05_S0_GPU

GPU VDDQ

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
U143	POWER	POWER	5V			REG_VCC_U8350
U143	POWER	POWER	5V			REG_PVCC_U8350
Local Ground						
U143	GND	GND	0V			AGND_GPUVDDQ
GPU VDDQ						
U142	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUVDDQ
U142	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUVDDQ
U142	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUVDDQ_RC
U142	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUVDDQ
U142	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUVDDQ
U142	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_OCSET
U142	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_VO
U143 VSNS_GPU_VDDQ	SNS_DIFF_PHY	SENSE				SNS_GPUVDDQ_P
U143 VSNS_GPU_VDDQ	SNS_DIFF_PHY	SENSE				SNS_GPUVDDQ_N
U143		SENSE				REG_GPUVDDQ_FB
U143		SENSE				REG_GPUVDDQ_RTN
U144	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_SREF
U144	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_FSEL
U144	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_SET0
U144	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_SET1
U144	VR_CTL_PHY	VR_CTL				REG_GPUVDDQ_SET1_R
Output Bus						
U142	POWER	POWER	1.5V			PPVDDQ_S0_GPU

3.3V S5/5V S4

Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus						
U144 POWER	POWER	12V			REG_VIN_U7600	68
U120 POWER	POWER	5V			REG_VCC1_U7600	68
U120 POWER	POWER	5V			REG_VCC2_U7600	68
3.3V S5						
U140 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P3V3S5	68
U140 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P3V3S5	68
U140 VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P3V3S5_RC	68
U140 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P3V3S5	68
U140 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P3V3S5	68
U140 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P3V3S5	68
U107 VR_CTL_PHY	VR_CTL				REG_P3V3S5_ISEN	68
U107 VR_CTL_PHY	VR_CTL				REG_P3V3S5_OCSET	68
U141 VR_CTL_PHY	VR_CTL				REG_P3V3S5_FSET	68
U106 VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT	68
U107 VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT_R	68
U107 VR_CTL_PHY	VR_CTL				REG_P3V3S5_FB	68
5V S3						
U113 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P5VS4	68
U113 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P5VS4	68
U113 VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P5VS4_RC	68
U114 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P5VS4	68
U114 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P5VS4	68
U114 VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P5VS4	68
U114 VR_CTL_PHY	VR_CTL				REG_P5VS4_ISEN	68
U114 VR_CTL_PHY	VR_CTL				REG_P5VS4_OCSET	68
U114 VR_CTL_PHY	VR_CTL				REG_P5VS4_FSET	68
U115 VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT	68
U115 VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT_R	68
U115 VR_CTL_PHY	VR_CTL				REG_P5VS4_FB	68
Output Bus						
U115 POWER	POWER	5V			PP5V_S5	6
U115 POWER	POWER	5V			PP5V_S4	6
U114 POWER	POWER	3.3V			PP3V3_S5	6
FET Switched						
U42 POWER	POWER	5V			PP5V_S0	6
U42 POWER	POWER	3.3V			PP3V3_S4	6
U42 POWER	POWER	3.3V			PP3V3_S0	6
U45 POWER	POWER	3.3V			PP3V3_S0_SSD	6
U21 POWER	POWER	3.3V			PP3V3_ENET	6
U30 POWER	POWER	3.3V			PP3V3_TBTLC	6
Sensed						
U145 POWER	POWER	3.3V			PPSSD_S0	6

DDR3 Vref

Physical	Spacing	Voltage	DIDT	NO_TEST		
Memory Vref						
U130 POWER	POWER	3.3V			PP3V3_S4_VREFMRGN_DAC	32
U130 POWER	POWER	3.3V			PP3V3_S4_VREFMRGN_CTRL	32
U130 POWER_DDR	POWER_DDR	0.75V			PPDDRVREF_DQ_MEM_A_S3	6
U130 POWER_DDR	POWER_DDR	0.75V			PPDDRVREF_DQ_MEM_B_S3	6
U130 POWER_DDR	POWER_DDR	0.75V			PPDDRVREF_CA_MEM_A_S3	6
U130 POWER_DDR	POWER_DDR	0.75V			PPDDRVREF_CA_MEM_B_S3	6
U144 POWER_DDR	POWER_DDR	0.75V			CPU_DIMM_VREF_DAC_A	11 32
U144 POWER_DDR	POWER_DDR	0.75V			CPU_DIMM_VREF_DAC_B	11 32
U130 POWER_DDR	POWER_DDR	0.75V			CPU_DDR_VREF	11

3.42V G3H

Physical	Spacing	Voltage	DIDT	NO_TEST		
3.42V G3H						
U144 POWER	VR_SWITCH	12V			P3V42G3H_BOOST	70
U144 POWER	VR_SWITCH	12V			P3V42G3H_SW	70
U144 VR_CTL_PHY	VR_CTL				P3V42G3H_FB	70
U144 VR_CTL_PHY	VR_CTL				P3V42G3H_SHDN_L	70
Output Bus						
U144 POWER	POWER	3.425V			PP3V42_G3H	6

1.8V S0

Physical	Spacing	Voltage	DIDT	NO_TEST		
1.8V S0						
U116 POWER	VR_SWITCH	5V			REG_PHASE_P1V8S0	69
U116 VR_CTL_PHY	VR_CTL				REG_P1V8S0_VFB	69
U116 VR_CTL_PHY	VR_CTL				REG_P1V8S0_SYNCH	69
Output Bus						
U116 POWER	POWER	1.8V			PP1V8_S0	6

HDD S0

Physical	Spacing	Voltage	DIDT	NO_TEST		
U130 POWER	POWER	5V			PPHDD_S0	6
U140 POWER	POWER	5V			PP5V_S0_HDD	6

12V

Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus						
U144 POWER	POWER	12V			PP12V_ACDC	6
FET Switched						
U144 POWER	POWER	12V			PP12V_S5	6
U144 POWER	POWER	12V			PP12V_S0	6
Sensed						
U144 POWER	POWER	12V			PP12V_G3H	6
U145 POWER	POWER	12V			PP12V_S0_GPUCORE	
U145 POWER	POWER	12V			PP12V_S0_GPUUNCORE	

Ground/Common

Physical	Spacing	Voltage	DIDT	NO_TEST	
Common					
U130 GND	GND	0V			GND

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Thunderbolt

Thunderbolt-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBTDP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Thunderbolt-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_I2C	*	=2x_DIELECTRIC	?
TBT_SPI	*	=2x_DIELECTRIC	?
TBTDP	*	=5x_DIELECTRIC	?
TBTDP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

DisplayPort

DP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

DP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	?

Pairs should be within 100 mils of clock length.
Max length of DisplayPort traces: 12 inches

DisplayPort intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DisplayPort AUX channel intra-pair matching should be 5 ps. No relationship to other signals.

TBT IC Net Properties

Electrical Contraint Set	Physical	Spacing		
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	9 34
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	9 34
DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	34
DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	34
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	9 34
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	9 34
DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	34
DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	34
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	9 34
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	9 34
DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	34
DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	34
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	9 34
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	9 34
DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	34
DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	34
DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_P<3..0>	73
DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_N<3..0>	73
DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	73
DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	73
DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_P	73
DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_N	73
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_P	73
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_N	73
	TBT_I2C_55S	TBT_I2C	=I2C_TBTRTR_SCL	34 48
	TBT_I2C_55S	TBT_I2C	=I2C_TBTRTR_SDA	34 48
TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK	34
TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI	34
TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO	34
TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L	34

*: Only used on hosts supporting T29 video-in

DisplayPort

Electrical Contraint Set	Physical	Spacing		
Graphics Source				
DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<1..0>	9 73
DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<1..0>	9 73
DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_P	9 73
DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_N	9 73
	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_P	73
	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_N	73
Internal Panel				
	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_P<3..0>	73
	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_N<3..0>	73
DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_P<3..0>	72 73
DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_N<3..0>	72 73
DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_P	72 73
DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_N	72 73
Internal DP SPDIF				
		HDA	DP_INT_SPDIF_AUDIO	53 72

TBT/DP Net Properties

Electrical Contraint Set	Physical	Spacing		
Port A				
TBT_A_R2D1	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<1>	34 75
TBT_A_R2D1	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<1>	34 75
TBT_A_R2D0	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<0>	34 75
TBT_A_R2D0	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<0>	34 75
	TBTDP_90D	TBTDP	TBT_A_R2D_P<1..0>	75
	TBTDP_90D	TBTDP	TBT_A_R2D_N<1..0>	75
DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	34 75
DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	34 75
DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	34 75
DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	34 75
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	75
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	75
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	75
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	75
DP_A_LSX	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	75
DP_A_LSX	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	75
	TBTDP_90D	TBTDP	TBT_A_D2R_C_P<1..0>	75
	TBTDP_90D	TBTDP	TBT_A_D2R_C_N<1..0>	75
TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_P<1>	34 75
TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_N<1>	34 75
TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_P<0>	34 75
TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_N<0>	34 75
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	34 75
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	34 75
	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P	75
	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N	75
DP_A_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_P	75
DP_A_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_N	75
	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_P	75
	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_N	75
Port B				
TBT_B_R2D1	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<1>	34 76
TBT_B_R2D1	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<1>	34 76
TBT_B_R2D0	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<0>	34 76
TBT_B_R2D0	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<0>	34 76
	TBTDP_90D	TBTDP	TBT_B_R2D_P<1..0>	76
	TBTDP_90D	TBTDP	TBT_B_R2D_N<1..0>	76
DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	34 76
DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	34 76
DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	34 76
DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	34 76
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	76
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	76
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	76
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	76
DP_B_LSX	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	76
DP_B_LSX	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	76
	TBTDP_90D	TBTDP	TBT_B_D2R_C_P<1..0>	76
	TBTDP_90D	TBTDP	TBT_B_D2R_C_N<1..0>	76
TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_P<1>	34 76
TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_N<1>	34 76
TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_P<0>	34 76
TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_N<0>	34 76
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	34 76
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	34 76
	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P	76
	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N	76
DP_B_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_P	76
DP_B_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_N	76
	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_P	76
	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_N	76

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Backlight Controller

BLC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BLC_P6MM	*	Y	0.600 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD
BLC_P3MM	*	Y	0.300 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_BLC	*	BLC_P6MM
POWER_BLC_RET	*	BLC_P3MM
BLC_CTL_PHY	*	BLC_P3MM

BLC-specific Spacing Definitions
BLC High Voltage Output

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_HV_ISO	*	0.45mm	1000

Constraints
BLC High Voltage Output

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_HV	BLC_CTL	*	BLC_CTL_ISO
BLC_HV	BLC_HV	*	BLC_CTL_ISO
BLC_HV	*	*	BLC_HV_ISO

BLC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PHASE_ISO	*	=8:1_SPACING	2000
PHASE_SW2SW	*	=1:1_SPACING	?
PHASE_SW2PWR	*	=2:1_SPACING	?
PHASE_SW2GND	*	=2:1_SPACING	?

BLC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_PHASE	*	*	PHASE_ISO
BLC_PHASE	BLC_PHASE	*	PHASE_SW2SW
BLC_PHASE	POWER	*	PHASE_SW2PWR
BLC_PHASE	GND	*	PHASE_SW2GND

BLC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_CTL_ISO	*	=3:1_SPACING	?

BLC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_CTL	*	*	BLC_CTL_ISO

Is it chel'oh or sel'oh?

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
H38	POWER	POWER	12V			PP12V_BKLT_SNS 77
H40	POWER	POWER	12V			PP12V_BKLT_FUSED 77
H46	POWER	POWER	12V			PP12V_S0_BKLT_FILT 77
H72	POWER	POWER	12V			PP12V_S0_BKLT_PWR 77
H94	POWER	POWER	12V			PP12V_S0_BKLT_PWR_R 77
H96	POWER	POWER	5V			PP5V_S0_BKLT_R 77
H48	POWER	POWER	3.3V			PP3V3_S0_BKLT_VDDIO_R 77
Local Ground						
H80	BLC_CTL_PHY	BLC_PHASE	0V			GND_BKLT 77
H34	BLC_CTL_PHY	BLC_PHASE	0V			PGND_BKLT 77
H70	BLC_CTL_PHY	BLC_PHASE	0V			DGND_BKLT 77
H88	BLC_CTL_PHY	BLC_PHASE	0V			LGND_BKLT 77
Backlight						
H76	POWER_BLC	BLC_PHASE	80V	TRUE		BKLT_PHASE 77
H36	BLC_CTL_PHY	BLC_PHASE	80V	TRUE		BKLT_GATE 77
H54	BLC_CTL_PHY	BLC_PHASE	80V	TRUE		BKLT_GATE_R 77
H78	BLC_CTL_PHY	BLC_PHASE	80V	TRUE	TRUE	BKLT_SNUBBER 77
H52	BLC_CTL_PHY	BLC_PHASE	12V	TRUE		BKLT_SW_R 77
H50	BLC_CTL_PHY	BLC_CTL				BKLT_ISET 77
H42	BLC_CTL_PHY	BLC_CTL				BKLT_FLT 77
H44	BLC_CTL_PHY	BLC_CTL				BKLT_FLT_RC 77
H74	SNS_DIFF_PHY	SENSE				BKLT_SW_P 77
H32	SNS_DIFF_PHY	SENSE				BKLT_SW_N 77
H62		SENSE				BKLT_FB 77
H60		BLC_HV	67V			BKLT_FB_XW 77
H64		BLC_HV	67V			BKLT_FB_R 77
H77	POWER_BLC_RET	BLC_CTL				BKLT_ISEN1 77
H79	POWER_BLC_RET	BLC_CTL				BKLT_ISEN2 77
H75	POWER_BLC_RET	BLC_CTL				BKLT_ISEN3 77
H37	POWER_BLC_RET	BLC_CTL				BKLT_ISEN4 77
H35	POWER_BLC_RET	BLC_CTL				BKLT_ISEN5 77
H33	POWER_BLC_RET	BLC_CTL				BKLT_ISEN6 77
H73	POWER_BLC_RET	BLC_HV				BKLT_ISEN1_R 77
H81	POWER_BLC_RET	BLC_HV				BKLT_ISEN2_R 77
H95	POWER_BLC_RET	BLC_HV				BKLT_ISEN3_R 77
H97	POWER_BLC_RET	BLC_HV				BKLT_ISEN4_R 77
H93	POWER_BLC_RET	BLC_HV				BKLT_ISEN5_R 77
H91	POWER_BLC_RET	BLC_HV				BKLT_ISEN6_R 77
H39	POWER_BLC_RET	BLC_HV				LED_RETURN_1 77
H41	POWER_BLC_RET	BLC_HV				LED_RETURN_2 77
H45	POWER_BLC_RET	BLC_HV				LED_RETURN_3 77
H43	POWER_BLC_RET	BLC_HV				LED_RETURN_4 77
H89	POWER_BLC_RET	BLC_HV				LED_RETURN_5 77
H87	POWER_BLC_RET	BLC_HV				LED_RETURN_6 77
Output Bus						
H71	POWER_BLC	BLC_HV	67V			BKLT_BOOST 77
H69	POWER_BLC	BLC_HV	67V			BKLT_BOOST_1 77
H67	POWER_BLC	BLC_HV	67V			BKLT_BOOST_2 77

Cello Miscellaneous

Electrical Contraint Set	Physical	Spacing	
SPI			
H56	SMB_PHY	SMB	BKLT_SCL 77
H58	SMB_PHY	SMB	BKLT_SDA 77

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