MAJOR ICs INFORMATION

1. General ICs Information

XD890WJ (MAIN UNIT):

· **IC1905** : HDMI RECEIVER
Part number: Sii9021
Sharp code: VHISII9021+-1Q
The Sii9021 is a second generation panel link cinema receiver that is compatible with the HDMI 1.1 (High Definition Multimedia Interface) specification. The Sii9021 is capable of receiving and outputting two channel digital audio signals at up to 192 kHz— an excellent solution for digital TVs.
This IC features the following.
1) Digital video interface supports video processors.
2) Analog RGB and YPbPr output: 10-bit DAC.
3) Digital audio interface supports high-end audio systems.

· **IC1901**: NVM OF HDMI (E-EDID)
Part number: 24LC2BIN
Sharp code: VHI24LC2BIN-1Y
This IC is a 2-wire (I2C bus type) serial EEPROM this is electrically programmable. This EEPROM chip stores the data structure used to carry configuration information for optimal use of a display (EDID data).

· **IC2701** : SYNC SELECT
Part number: TVHC153T
Sharp code: VHITVHC153T-1Y
This VHC153 is a high-speed Dual 4-input multiplexer with common select inputs and individual enable inputs for each section.

IC2704 : HDMI & RGB SOUND MULTIPLEXER
Part number: CD4052BP
Sharp code: VHICD4052BP-1Y
The TC74HC4052A is a high-speed CMOS analog multiplexer/demultiplexer backed by silicon gate CMOS technology. The multiplexer function includes the selection and mixing of analog and digital signals. The chip consists of 4 channels (x 2). A digital signal through the control terminal turns on the switch of a corresponding channel.

· **IC3002 :** VIDEO PROCESSOR
Part number: VCTP
Sharp code: RH-IXB624WJN1Q
The VCT 6wxyP family is dedicated to high-quality FPD and double-scan TV sets. The memory and program ROM are integrated in the IC. Modular design and deep submicron technology allow the integration of audio, video, teletext, OSD, and controller-related functionalities. They cover the whole range of flat-panel display TVs. The IC is based on proven functional blocks of existing products like VCT 49xxI, VSP 94x5B, and DPS 94xxB.
Each member of the IC family contains the entire audio, video, upconversion processing for 4:3 and 16:9 50/60 Hz progressive or 100/120 Hz interlaced stereo TV sets plus the control/data interface for flat-panel displays. The integrated microcontroller is supported by a powerful OSD and graphics generator with integrated teletext acquisition.
The VCT 6wxyP family provides a front-end video processing unit with 4 CVBS-Y/C or component inputs for HDTV, EDTV, and SDTV. A VBI slicer, support of 1000 pages of teletext, and a 3-D comb filter for PAL and NTSC (in certain versions) are also available. The front-end unit further allows to process an SD and an HD source in parallel, thus enabling PiP and PaP functionality. Motion-adaptive de-interlacing, temporal noise reduction, and film mode detection are based on a unified memory technology.
Post-scaling in the display processing block ensures the desired output format. Display processing is supported by an 8-bit 8051-compatible controller. By means of powerful alpha-blending, the graphics mixer composes the output image from following image layers: the video layer, the OSD layer and the pixel graphics layer.
The audio part consists of a multistandard sound IF demodulator and a baseband processor supporting all desired sound features in this range.
A connection for additional features, such as advanced motion compensation via -Micronas' FRC 94xyA, is also provided.

· **IC3001 :** NVM 64Kb-E2PROM
Part number: BR24L64F
Sharp code: VHIBR24L64F-1Y
The BR24L64F is a 2-wire (I2C bus type) serial EEPROM that is electrically programmable. This IC stores the control data of system contents (last memory, for example) for the main microprocessor's AV PWB and main PWB. The data is given out by commands from the main microprocessor.

· **IC3003 :** PIC MICROCONTROLLER
Part number: PIC16F913
Sharp code: RH-IXB664WJZZY
28 Pin Flash-Based, 8 bit CMOS Microcontrollers with LCD Driver and nanoWatt Technology.
This IC is controlled via I2C and works how expander of ports. This IC has led control and include A/D converter.

· **IC2301 :** RS-232 TRANSMITTERS/RECEIVERS
Part number: ISL83220
Sharp code: VHIISL83220-1Y
The ISL83220E is a 3.0V to 5.5V powered RS-232 transmitter/receiver,+/-15kV ESD protected, minimum data rate 250 kpbs.

· **IC2303 :** NVM OF PC MODE (EDID)
Part number: BR24C21F
Sharp code: VHIBR24C21F-1Y
This IC is a 2-wire (I2C bus type) serial EEPROM this is electrically programmable. This EEPROM chip stores the data structure used to carry configuration information for optimal use of a display (EDID data).

· **IC1701:** POWER RESET OF +BU1.8V
Part number: BU4239G
Sharp code: VHIBU4239G+-1Y
Low voltage detector IC with adjustable output delay. Standard Detection Voltage = 3.9V

· **IC1702:** BU+3.3V (VOLTAGE INPUT: BU+5V)
Part number: PQ20WZ11
Sharp code: VHIPQ20WZ11-1Y
Low power-loss voltage regulators. Variable Output. Output current 1A. Built-in overcurrent, overheat protection functions, ASO protection circuit.

· **IC1703:** S+8V (VOLTAGE INPUT: POW+12V)
Part number: PQ20WZ11
Sharp code: VHIPQ20WZ11-1Y
Low power-loss voltage regulators. Variable Output. Output current 1A. Built-in overcurrent, overheat protection functions, ASO protection circuit.

· **IC1707:** +3.3V (VOLTAGE INPUT: POW+5V)
Part number: PQ20WZ11
Sharp code: VHIPQ20WZ11-1Y
Low power-loss voltage regulators. Variable Output. Output current 1A. Built-in overcurrent, overheat protection functions, ASO protection circuit.

· **IC1708:** +1.8V (VOLTAGE INPUT: POW+5V)
Part number: MP1410
Sharp code: VHIMP1410ES-1Y
DC to DC Converter. 2A Step down switch mode regulator with a built in internal Power Mosfet. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

· **IC1706:** BU+1.8V (VOLTAGE INPUT: BU+5V)
Part number: MP1410
Sharp code: VHIMP1410ES-1Y
DC to DC Converter. 2A Step down switch mode regulator with a built in internal Power Mosfet. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

· **IC1710:** CPLD
Part number: EPM240T
Sharp code: RH-IXB823WJZZQ
This IC is a CPLD of Altera and use CMOS EEPROM cells to implement logic functions with 64 Macrocells. This device controls ON/OFF power supply and signals for inverter unit.

FD604WJ (AV UNIT):

· **IC301 & IC302** : AUDIO AMPLIFIER
Part number: TDA8931T
Sharp code: VHITDA893T-1Y
The TDA8931 is a switching power stage for high efficiency class-D audio power amplifier systems. The IC has a high efficiency so that a heat sink is not required up to 20W (RMS).

· **IC303** : HEADPHONE AMPLIFIER
Part number: NJM4558M
Sharp code: VHINJM4558M-1Y
The NJM4558 is a dual high-gain operational amplifier internally compensated and constructed on a single silicon chip using an advanced epitaxial process.

· **IC1101 & IC1102:** VIDEO OUTPUT
Part number: MM1506XN
Sharp code: VHIMM1506XN-1Y
This IC extends the series of ICs for video/audio signal switching, with a 2-input 1-output single video switch with 75W driver and input bias (6dB gain).

· **IC1201:** VIDEO INPUT
Part number: MM1507XN
Sharp code: VHIMM1506XN-1Y
This IC extends the series of ICs for video/audio signal switching, with a 2-input 1-output single video switch with 75W driver and input clamp.

FD605WJ (POWER SUPPLY UNIT):

· **IC708:**
Part number: NJM2904M
Sharp code: VHINJM2904M-1Y
The IC consists of two independent, high gain internally frequency compensated operation amplifiers which were designed specifically to operate from single power supply.

· **IC706 & IC707:** FEEDBACK CONTROL
Part number: TA76431R
Sharp code: VHITA76431R-1Y
Adjustable precision shunt regulator for feedback control for driving an optocoupler in power supplies

· **IC705:** POWER SUPPLY CONTROLLER FOR INVERTER
Part number: MR4020
Sharp code: VHIMR4020++-1
A high speed 900V IGBT makes ideal partial resonance operation which ensures high efficiency and low noise.
Very low power consumption at micro-loads (burst mode).
Start-up circuit eliminates the need for start-up resistor.
Excess current protection (ON period limitation, primary current limitation), excess voltage protection, and thermal shut-down function are incorporated.

· **IC704:** POWER SUPPLY CONTROLLER FOR SIGNAL BOARD
Part number: MR4030
Sharp code: VHIMR4030++-1
A high speed 900V IGBT makes ideal partial resonance operation which ensures high efficiency and low noise.
Very low power consumption at micro-loads (burst mode).
Start-up circuit eliminates the need for start-up resistor.
Excess current protection (ON period limitation, primary current limitation), excess voltage protection, and thermal shut-down function are incorporated.

FD607WJ (RC/LED UNIT):

· **IC101 :** OPC
Part number: TPS850
Sharp code: VHITPS850++-1Y
The TPS850 is a linear-output photo-IC which incorporates a photodiode and current amp circuit in a single chip. This photo-IC is current output type, so can set up output voltage freely by arbitrary load resistance.

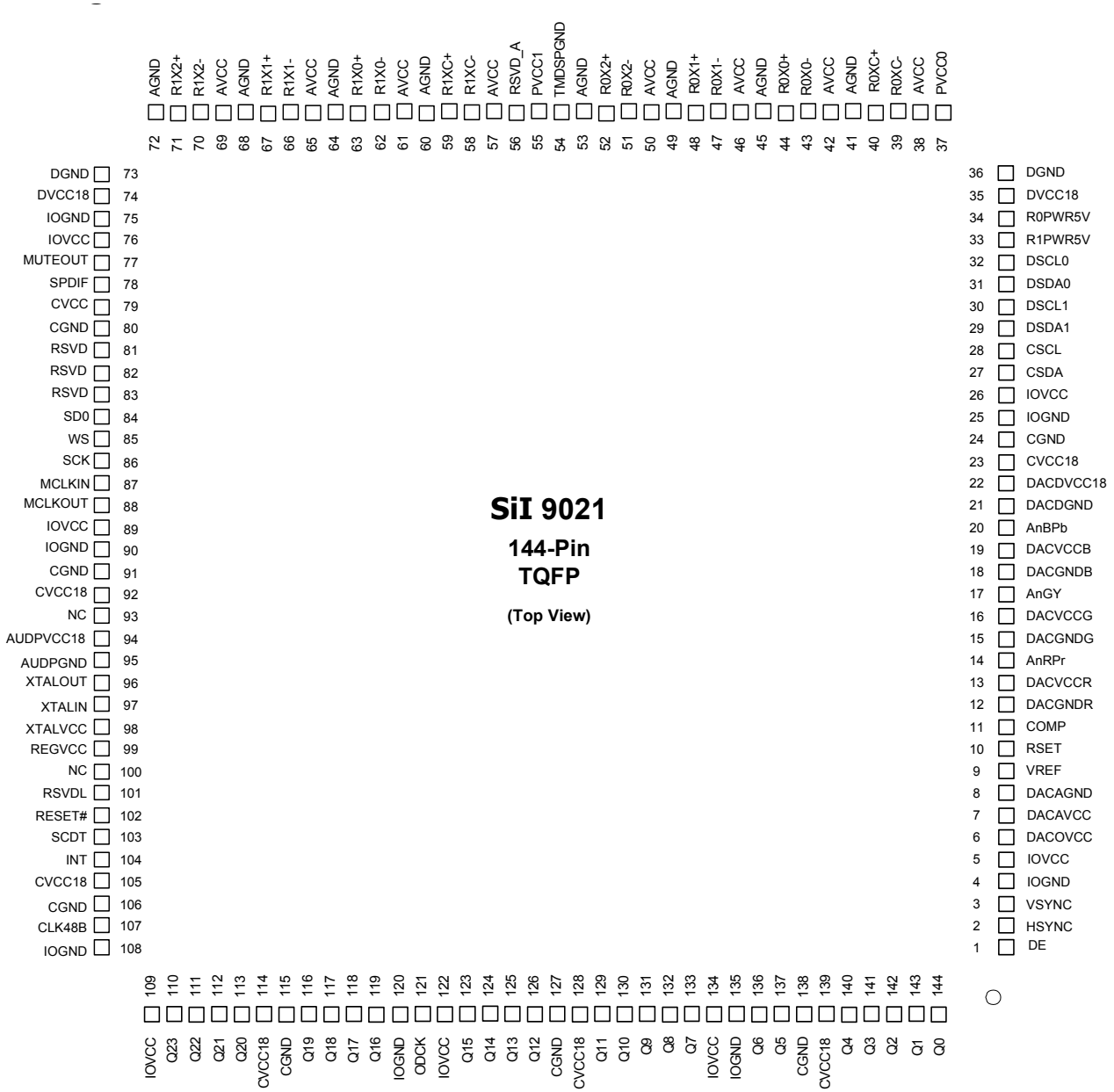
FD608WJ (TUNER UNIT):

· **IC201 :** IF-Demodulator/PLL
Part number: TDA9886
Sharp code: VHITDA9886+-1Y
The TDA9886 is an alignment-free multi-standard (PAL, SECAM and NTSC) vision and sound IF signal PLL demodulator for positive and negative modulation including sound AM and FM processing.
This IC features the following.
* Gain controlled wide-band vision intermediate frequency (VIF) amplifier (AC-coupled).
* Multi-standard true synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures reduced harmonics, excellent pulse response).
* Gate phase detector for L/L accent standard.
* Fully integrated VIF Voltage Controlled Oscillator (VCO), alignment-free; frequencies switchable for all negative modulated standards via I2C bus.
* 4MHz reference frequency input [signal from phase-locked loop (PLL) tuning system] or operating as crystal oscillator.
* VIF Automatic Gain Control (AGC) detector for gain control operating as a peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals.

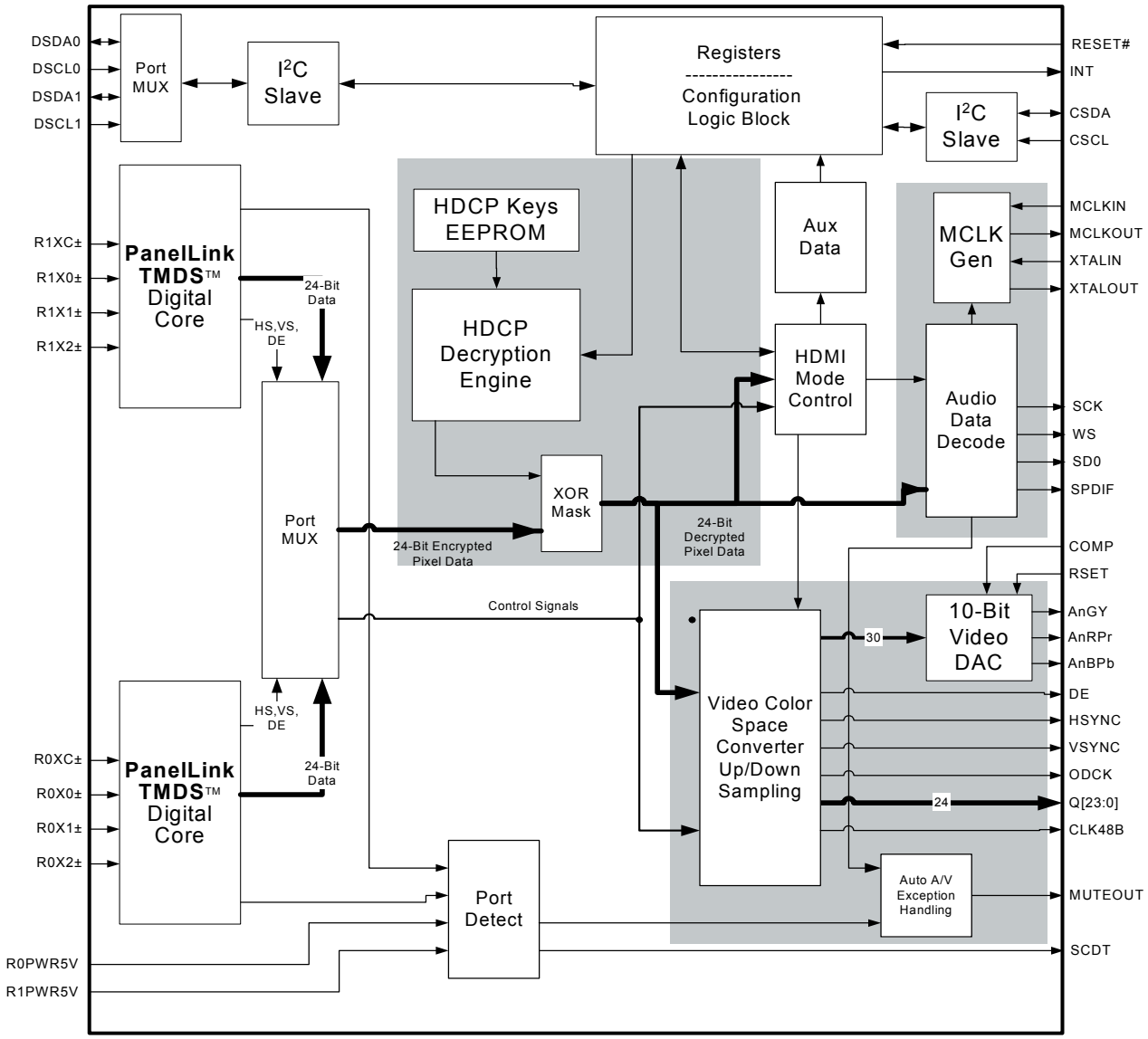
2. Detailed ICs Information

2.1. IC1905 (VHISII9021+-1Q)

2.1.1. Pinning



2.1.2. Block Diagram



The SiI 9021 supports two HDMI input ports. Only one port may be active at any time.

2.2. IC3002 (RH-IXB624WJN1Q)

2.2.1. Pin Connections and Short Description

IN = Input Pin
ANA = Analog Pin
OUT = Output Pin
SUPPLY = Supply Pin

NC = not connected
LV = if not used, leave vacant
OBL = obligatory; connect as described in circuit diagram

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
1		656O6 P4_6 TDOFW	IN/OUT	LV	Digital 656 Bit 6 Output Port 4, Bit 6 Input/Output JTAG Interface Data Output (firmw. Controler)
2		656O5 P4_5 TDIFW	IN/OUT	LV	Digital 656 Bit 5 Output Port 4, Bit 5 Input/Output JTAG Interface Data Input (firmw. Controler)
3		656O4 P4_4 TMSFW	IN/OUT	LV	Digital 656 Bit 4 Output Port 4, Bit 4 Input/Output JTAG Interface Mode Select Input (fw. Contr.)
4		656O3 P4_3 TCLK	IN/OUT	LV	Digital 656 Bit 3 Output Port 4, Bit 3 Input/Output JTAG Interface Clock Input (TV Controler)
5		656O2 P4_2 TDO	IN/OUT	LV	Digital 656 Bit 2 Output Port 4, Bit 2 Input/Output JTAG Interface Data Output (TV Controler)
6		656O1 P4_1 TDI	IN/OUT	LV	Digital 656 Bit 1 Output Port 4, Bit 1 Input/Output JTAG Interface Data Input (TV Controler)
7		656O0 P4_0 TMS	IN/OUT	LV	Digital 656 Bit 0 Output (LSB) Port 4, Bit 0 Input/Output JTAG Interface Mode Select Input (TV Contr.)
8		RESETQ	IN/OUT	OBL	$\overline{\text{Reset}}$ Input/Output
9		AIN1R	IN	GND	Analog Audio 1 Input, Right
10		AIN1L	IN	GND	Analog Audio 1 Input, Left
11		AIN2R	IN	GND	Analog Audio 2 Input, Right
12		AIN2L	IN	GND	Analog Audio 2 Input, Left
13		AIN3R	IN	GND	Analog Audio 3 Input, Right
14		AIN3L	IN	GND	Analog Audio 3 Input, Left
15		AIN4R	IN	GND	Analog Audio 4 Input, Right
16		AIN4L	IN	GND	Analog Audio 4 Input, Left
17		VREFAU	ANA	OBL	Reference Voltage, Audio
18		VSUP8.0AU	SUPPLY	OBL	Supply Voltage Analog Audio, 8.0 V
19		GNDA	SUPPLY	OBL	Ground Analog Audio, Platform Ground
20		SGND	ANA	OBL	Analog Signal GND

2.2.1. Pin Connections and Short Description (Continued)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
21		AOUT2R AIN5R	IN/OUT	LV	Analog Audio 2 Output, Right Analog Audio 5 Input, Right
22		AOUT2L AIN5L	IN/OUT	LV	Analog Audio 2 Output, Left Analog Audio 5 Input, Left
23		AOUT1R	OUT	LV	Analog Audio 1 Output, Right
24		AOUT1L	OUT	LV	Analog Audio 1 Output, Left
25		HEADPHONER	OUT	LV	Analog Headphone Output, Right
26		HEADPHONEL	OUT	LV	Analog Headphone Output, Left
27		SPEAKERR	OUT	LV	Analog Loudspeaker Output, Right
28		SPEAKERL	OUT	LV	Analog Loudspeaker Output, Left
29		SUBWOOFER TEST	IN/OUT	LV	Analog SUBWOOFER Output Test Input
30		VREFSIF	ANA	OBL	Reference Voltage, Audio SIF
31		SIFIN+	IN	$VREF_{IF}$	Differential IF Input
32		SIFIN-	IN	$VREF_{IF}$	Differential IF Input
33		VSUP5.0SIF	SUPPLY	OBL	Supply Voltage Analog SIF, 5.0 V
34		GNDA	SUPPLY	OBL	Ground Analog SIF, Platform Ground
35		GND3.3DIG	SUPPLY	OBL	Ground Digital Audio Core
36		VSUP3.3DIG	SUPPLY	OBL	Supply Voltage Digital Audio Core, 3.3 V
37		SPDIF_OUT	OUT	LV	SPDIF Output
38		I2S_DA_IN	IN	LV	Audio Bus Data Input
39		I2S_CL	IN	LV	Audio Bus Clock Input
40		I2S_WS	IN	LV	Audio Bus Word Strobe Input
41		I2S_DEL_OUT	OUT	LV	Audio Delay Line Bus Data Output
42		I2S_DEL_IN	IN	LV	Audio Delay Line Bus Data Input
43		I2S_DEL_CL	OUT	LV	Audio Delay Line Bus Clock Output
44		I2S_DEL_WS	OUT	LV	Audio Delay Line Bus Word Strobe Output
45		VSUP3.3RAM	SUPPLY	OBL	Supply Voltage Ram, 3.3 V
46		GND3.3RAM	SUPPLY	OBL	Ground Ram
47		DVS	IN	LV	Digital or Analog Video VSYNC HD Input
48		DEN	IN	LV	Digital Video Enable Input
49		DCLK	IN	LV	Digital Video Clock Input
50		DRI7	IN	LV	Digital Video Red 7 Input

2.2.1. Pin Connections and Short Description (Continued)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
51		DRI6	IN	LV	Digital Video Red 6 Input
52		DRI5	IN	LV	Digital Video Red 5 Input
53		DRI4	IN	LV	Digital Video Red 4 Input
54		DRI3	IN	LV	Digital Video Red 3 Input
55		DRI2	IN	LV	Digital Video Red 2 Input
56		DRI1	IN	LV	Digital Video Red 1 Input
57		DRI0	IN	LV	Digital Video Red 0 Input (LSB)
58		DGI7	IN	LV	Digital Video Green 7 Input
59		DGI6	IN	LV	Digital Video Green 6 Input
60		DGI5	IN	LV	Digital Video Green 5 Input
61		DGI4	IN	LV	Digital Video Green 4 Input
62		DGI3	IN	LV	Digital Video Green 3 Input
63		DGI2	IN	LV	Digital Video Green 2 Input
64		DGI1	IN	LV	Digital Video Green 1 Input
65		DGI0	IN	LV	Digital Video Green 0 Input (LSB)
66		DBI7	IN	LV	Digital Video Blue 7 Input
67		DBI6	IN	LV	Digital Video Blue 6 Input
68		DBI5	IN	LV	Digital Video Blue 5 Input
69		DBI4	IN	LV	Digital Video Blue 4 Input
70		DBI3	IN	LV	Digital Video Blue 3 Input
71		DBI2	IN	LV	Digital Video Blue 2 Input
72		DBI1	IN	LV	Digital Video Blue 1 Input
73		DBI0	IN	LV	Digital Video Blue 0 Input (LSB)
74		GND3.3DRI	SUPPLY	OBL	Ground Digital Ram Interface
75		VSUP3.3DRI	SUPPLY	OBL	Supply Voltage Digital Ram Interface, 3.3 V
76		GND3.3COM	SUPPLY	OBL	Ground Common
77		VSUP3.3COM	SUPPLY	OBL	Supply Voltage Common, 3.3V
78		XTALIN	IN	OBL	Analog Crystal Input
79		XTALOUT	OUT	OBL	Analog Crystal Output
80		CLKOUT	OUT	LV	Digital 20MHz Clock Output
81		VSO	OUT	LV	Vertical Sync Output, Frontend

2.2.1. Pin Connections and Short Description (Continued)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
82		HSO	OUT	LV	Horizontal Sync Output, Frontend
83		SCL	IN/OUT	OBL	I^2C Bus Clock Input/Output
84		SDA	IN/OUT	OBL	I^2C Bus Data Input/Output
85		GND3.3FL	SUPPLY	OBL	Ground Flash
86		VSUP3.3FL	SUPPLY	OBL	Supply Voltage Flash, 3.3 V
87		P2_0	IN/OUT	LV	Port 2, Bit 0 Input/Output
88		P2_1	IN/OUT	LV	Port 2, Bit 1 Input/Output
89		P2_2	IN/OUT	LV	Port 2, Bit 2 Input/Output
90		P2_3	IN/OUT	LV	Port 2, Bit 3 Input/Output
91		P2_4 TDI	IN/OUT	LV	Port 2, Bit 4 Input/Output JTAG Interface Data Input
92		P2_5 TMS	IN/OUT	LV	Port 2, Bit 5 Input/Output JTAG Interface Mode Select Input
93		OSDV DBO2_0	IN/OUT	LV	Graphic Vertical Sync Input/Output Channel 2 Digital 0 Blue Output (LSB)
94		OSDH DBO2_1	IN/OUT	LV	Graphic Horizontal Sync Input/Output Channel 2 Digital 1 Blue Output
95		GND3.3IO1	SUPPLY	OBL	Ground Digital Input/Output Port 1
96		VSUP3.3IO1	SUPPLY	OBL	Supply Voltage Input/Output Port 1, 3.3 V
97		OSDCLK DBO2_2	IN/OUT	LV	Graphic Clock Input/Output Channel 2 Digital 2 Blue Output
98		OSDFSW DBO2_3	IN/OUT	LV	Graphic Fast Switch Input/Output Channel 2 Digital 3 Blue Output
99		OSDHCS1 P3_7 DBO2_4	IN/OUT	LV	Graphic Half Contrast 1 Input/Output Port 3, Bit 7 Input/Output Channel 2 Digital 4 Blue Output
100		OSDHCS0 P3_6 DBO2_5	IN/OUT	LV	Graphic Half Contrast 0 Input/Output (LSB) Port 3, Bit 6 Input/Output Channel 2 Digital 5 Blue Output
101		OSDB3 P3_5 DBO2_6	IN/OUT	LV	Graphic Blue 3 Input/Output (MSB) Port 3, Bit 5 Input/Output Channel 2 Digital 6 Blue Output
102		OSDB2 P3_4 DBO2_7	IN/OUT	LV	Graphic Blue 2 Input/Output Port 3, Bit 4 Input/Output Channel 2 Digital 7 Blue Output (MSB)
103		OSDB1 DGO2_0	IN/OUT	LV	Graphic Blue 1 Input/Output Channel 2 Digital 0 Green Output (LSB)
104		OSDB0 DGO2_1	IN/OUT	LV	Graphic Blue 0 Input/Output Channel 2 Digital 1 Green Output

2.2.1. Pin Connections and Short Description (Continued)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
105		OSDG3 P3_3 DGO2_2	IN/OUT	LV	Graphic Green 3 Input/Output (MSB) Port 3, Bit 3 Input/Output Channel 2 Digital 2 Green Output
106		OSDG2 P3_2 DGO2_3	IN/OUT	LV	Graphic Green 2 Input/Output Port 3, Bit 2 Input/Output Channel 2 Digital 3 Green Output
107		OSDG1 DGO2_4	IN/OUT	LV	Graphic Green 1 Input/Output Channel 2 Digital 4 Green Output
108		OSDG0 DGO2_5	IN/OUT	LV	Graphic Green 0 Input/Output Channel 2 Digital 5 Green Output
109		OSDR3 P3_1 DGO2_6	IN/OUT	LV	Graphic Red 3 Input/Output (MSB) Port 3, Bit 1 Input/Output Channel 2 Digital 6 Green Output
110		OSDR2 P3_0 DGO2_7	IN/OUT	LV	Graphic Red 2 Input/Output Port 3, Bit 0 Input/Output Channel 2 Digital 7 Green Output (MSB)
111		OSDR1 DRO2_0	IN/OUT	LV	Graphic Red 1 Input/Output Channel 2 Digital 0 Red Output (LSB)
112		OSDR0 DRO2_1	IN/OUT	LV	Graphic Red 0 Input/Output (LSB) Channel 2 Digital 1 Red Output
113		GND3.3IO1	SUPPLY	OBL	Ground Digital Input/Output Port 1
114		VSUP3.3IO1	SUPPLY	OBL	Supply Voltage Input/Output Port 1, 3.3 V
115		PCS5 P2_6	IN/OUT	LV	Flat Panel Control Select 5 PWM Output Port 2, Bit 6 Input/Output
116		PCS4 P2_7	IN/OUT	LV	Flat Panel Control Select 4 REV Output Port 2, Bit 7 Input/Output
117		PCS3 P4_0	IN/OUT	LV	Flat Panel Control Select 3 DE2 Output Port 4, Bit 0 Input/Output
118		PCS2 P4_1	IN/OUT	LV	Flat Panel Control Select 2 DE1 Output Port 4, Bit 1 Input/Output
119		PCS1 P4_2	IN/OUT	LV	Flat Panel Control Select 1 V Output Port 4, Bit 2 Input/Output
120		PCS0 P4_3	IN/OUT	LV	Flat Panel Control Select 0 H Output Port 4, Bit 3 Input/Output
121		PCLK2	OUT	LV	Flat Panel Control Clock 2 Output
122		PCLK1	OUT	LV	Flat Panel Control Clock 1 Output
123		GND1.8DIG	SUPPLY	OBL	Ground Digital Core
124		VSUP1.8DIG	SUPPLY	OBL	Supply Voltage Digital Core, 1.8 V
125		DBO1_0 DRO2_2 LVDSA_4P	OUT	LV	Channel 1 Digital 0 Blue Output[1)] (LSB) Channel 2 Digital 2 Red Output[1)] LVDS Channel 1 bit 4 Positive Output[2)]

2.2.1. Pin Connections and Short Description (Continued)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
126		DBO1_1 DRO2_3 LVDSA_4N	OUT	LV	Channel 1 Digital 1 Blue Output[1)] Channel 2 Digital 3 Red Output[1)] LVDS Channel 1 bit 4 Negative Output[2)]
127		DBO1_2 DRO2_4 VSUP3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 2 Blue Output[1)] Channel 2 Digital 4 Red Output[1)] Supply Digital Voltage LVDS[2)] Port, 3.3 V
128		DBO1_3 DRO2_5 LVDSA_3P	OUT	LV	Channel 1 Digital 3 Blue Output[1)] Channel 2 Digital 5 Red Output[1)] LVDS Channel 1 bit 3 Positive Output[2)]
129		DBO1_4 DRO2_6 LVDSA_3N	OUT	LV	Channel 1 Digital 4 Blue Output[1)] Channel 2 Digital 6 Red Output[1)] LVDS Channel 1 bit 3 Negative Output[2)]
130		DBO1_5 DRO2_7 GND3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 5 Blue Output[1)] Channel 2 Digital 7 Red Output[1)] (MSB) Ground Digital LVDS[2)], 3.3 V
131		DBO1_6 DBO1_0 LVDSA_CLKP	OUT	LV	Channel 1 Digital 6 Blue Output[1)] Channel 1 Digital 0 Blue Output[1)] (LSB) LVDS Channel 1 Clock Positive Output[2)]
132		DBO1_7 DBO1_1 LVDSA_CLKN	OUT	LV	Channel 1 Digital 7 Blue Output[1)] Channel 1 Digital 1 Blue Output[1)] LVDS Channel 1 Clock Negative Output[2)]
133		VSUP3.3IO2 VSUP3.3LVDS	SUPPLY	OBL	Supply Digital Output[1)] Port 2 Supply Digital Voltage LVDS[2)], 3.3 V
134		GND3.3IO2 LVDSA_2P	SUPPLY OUT	OBL LV	Ground Voltage Output[1)] Port 2, 3.3 V LVDS Channel 1 bit 2 Positive Output[2)]
135		DBO1_8 DBO1_2 LVDSA_2N	OUT	LV	Channel 1 Digital 8 Blue Output[1)] Channel 1 Digital 2 Blue Output[1)] LVDS Channel 1 bit 2 Negative Output[2)]
136		DBO1_9 DBO1_3 GND3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 9 Blue Output[1)] (MSB) Channel 1 Digital 3 Blue Output[1)] Ground Digital LVDS[2)], 3.3 V
137		DGO1_0 DBO1_4 LVDSA_1P	OUT	LV	Channel 1 Digital 0 Green Output[1)] (LSB) Channel 1 Digital 4 Blue Output[1)] LVDS Channel 1 bit 1 Positive Output[2)]
138		DGO1_1 DBO1_5 LVDSA_1N	OUT	LV	Channel 1 Digital 1 Green Output[1)] Channel 1 Digital 5 Blue Output[1)] LVDS Channel 1 bit 1 Negative Output[2)]
139		DGO1_2 DBO1_6 VSUP3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 2 Green Output[1)] Channel 1 Digital 6 Blue Output[1)] Supply Digital Voltage LVDS[2)], 3.3 V
140		DGO1_3 DBO1_7 LVDSA_0P	OUT	LV	Channel 1 Digital 3 Green Output[1)] Channel 1 Digital 7 Blue Output[1)] (MSB) LVDS Channel 1 bit 0 Positive Output[2)]

2.2.1. Pin Connections and Short Description (Continued)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
141		DGO1_4 DGO1_0 LVDSA_0N	OUT	LV	Channel 1 Digital 4 Green Output[1)] Channel 1 Digital 0 Green Output[1)] (LSB) LVDS Channel 1 bit 0 Negative Output[2)]
142		DGO1_5 DGO1_1 VSUP1.8LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 5 Green Output[1)] Channel 1 Digital 1 Green Output[1)] Supply Analog Voltage LVDS[2)], 1.8 V
143		DGO1_6 DGO1_2 REXT	OUT ANA	LV OBL	Channel 1 Digital 6 Green Output[1)] Channel 1 Digital 2 Green Output[1)] LVDS External Resistor[2)]
144		DGO1_7 DGO1_3 GND1.8LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 7 Green Output[1)] Channel 1 Digital 3 Green Output[1)] Ground Analog LVDS[2)], 1.8 V
145		DGO1_8 DGO1_4 LVDSB_3P	OUT	LV	Channel 1 Digital 8 Green Output[1)] Channel 1 Digital 4 Green Output[1)] Dual-LVDS Channel 2 bit 3 Positive Output[2)]
146		DGO1_9 DGO1_5 LVDSB_3N	OUT	LV	Channel 1 Digital 9 Green Output[1)] (MSB) Channel 1 Digital 5 Green Output[1)] Dual-LVDS Channel 2 bit 3 Negative Output[2)]
147		DRO1_0 DGO1_6 GND3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 0 Red Output[1)] (LSB) Channel 1 Digital 6 Green Output[1)] Ground Digital LVDS[2)], 3.3 V
148		DRO1_1 DGO1_7 LVDSBCLKP	OUT	LV	Channel 1 Digital 1 Red Output[1)] Channel 1 Digital 7 Green Output[1)] (MSB) Dual-LVDS Channel 2 Clock Positive Output[2)]
149		GND3.3IO2 LVDSBCLKN	SUPPLY OUT	OBL LV	Ground Digital Output[1)] Port 2 Dual-LVDS Channel 2 Clock Negative Output[2)]
150		VSUP3.3IO2 VSUP3.3LVDS	SUPPLY	OBL	Supply Voltage Output[1)] Port 2, 3.3 V Supply Digital Voltage LVDS[2)], 3.3 V
151		DRO1_2 DRO1_0 LVDSB_2P	OUT	LV	Channel 1 Digital 2 Red Output[1)] Channel 1 Digital 0 Red Output[1)] (LSB) Dual-LVDS Channel 2 bit 2 Positive Output[2)]
152		DRO1_3 DRO1_1 LVDSB_2N	OUT	LV	Channel 1 Digital 3 Red Output[1)] Channel 1 Digital 1 Red Output[1)] Dual-LVDS Channel 2 bit 2 Negative Output[2)]
153		DRO1_4 DRO1_2 GND3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 4 Red Output[1)] Channel 1 Digital 2 Red Output[1)] Ground Digital LVDS[2)], 3.3 V
154		DRO1_5 DRO1_3 LVDSB_1P	OUT	LV	Channel 1 Digital 5 Red Output[1)] Channel 1 Digital 3 Red Output[1)] Dual-LVDS Channel 2 bit 1 Positive Output[2)]
155		DRO1_6 DRO1_4 LVDSB_1N	OUT	LV	Channel 1 Digital 6 Red Output[1)] Channel 1 Digital 4 Red Output[1)] Dual-LVDS Channel 2 bit 1 Negative Output[2)]

2.2.1. Pin Connections and Short Description (Continued)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
156		DRO1_7 DRO1_5 VSUP3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 7 Red Output[1)] Channel 1 Digital 5 Red Output[1)] Supply Digital Voltage LVDS[2)], 3.3 V
157		DRO1_8 DRO1_6 LVDSB_0P	OUT	LV	Channel 1 Digital 8 Red Output[1)] Channel 1 Digital 6 Red Output[1)] Dual-LVDS Channel 2 bit 0 Positive Output[2)]
158		DRO1_9 DRO1_7 LVDSB_0N	OUT	LV	Channel 1 Digital 9 Red Output[1)] (MSB) Channel 1 Digital 7 Red Output[1)] (MSB) Dual-LVDS Channel 2 bit 0 Negative Output[2)]
159		P1_7 TDO	IN/OUT	OBL	Port 1, Bit 7 Input/Output JTAG Interface Data Output
160		P1_6 TCLK	IN/OUT	OBL	Port 1, Bit 6 Input/Output JTAG Interface Clock Input
161		P1_5	IN/OUT	LV	Port 1, Bit 5 Input/Output
162		P1_4	IN/OUT	LV	Port 1, Bit 4 Input/Output
163		GND3.3DAC	SUPPLY	OBL	Ground DAC
164		VSUP3.3DAC	SUPPLY	OBL	Supply Voltage DAC, 3.3V
165		P1_3 ROUT	IN/OUT	LV	Port 1, Bit 3 Input/Output Analog Red Output
166		P1_2 GOUT	IN/OUT	LV	Port 1, Bit 2 Input/Output Analog Green Output
167		P1_1 BOUT	IN/OUT	LV	Port 1, Bit 1 Input/Output Analog Blue Output
168		P1_0 SVMOUT	IN/OUT	LV	Port 1, Bit 0 Input/Output Scan Velocity Modulation Output
169		VSUP1.8FE	SUPPLY	OBL	Supply Voltage Analog Video Frontend, 1.8 V
170		VSUP3.3FE	SUPPLY	OBL	Supply Voltage Analog Video Frontend, 3.3 V
171		VIN22 DHS	IN	GND	Analog Video 22 H-Sync Input Digital Video H-Sync Input
172		VIN21	IN	GND	Analog Video 21 B HD Input
173		VIN20	IN	GND	Analog Video 20 G HD Input
174		VIN19	IN	GND	Analog Video 19 R HD Input
175		VIN18	IN	GND	Analog Video 18 Fast Blank 2 Input
176		VIN17	IN	GND	Analog Video 17 B HD Input
177		VIN16	IN	GND	Analog Video 16 G HD Input
178		VIN15	IN	GND	Analog Video 15 R HD Input
179		VIN13	IN	GND	Analog Video 13 B HD Input

2.2.1. Pin Connections and Short Description (Continued)

VCTP Pin No.		Pin Name	Type	Connection	Short Description
PLQFP 208-1				(If not used)	
180		VIN12	IN	GND	Analog Video 12 G HD Input
181		VIN11	IN	GND	Analog Video 11 R HD Input
182		VIN9	IN	GND	Analog Video 9 Y or B SD Input
183		VIN8	IN	GND	Analog Video 8 C or Fast Blank 1 Input
184		VIN7	IN	GND	Analog Video 7 Y or G SD Input
185		VSUP1.8FE	SUPPLY	OBL	Supply Voltage Analog Video Frontend, 1.8 V
186		GNDA	SUPPLY	OBL	Analog Video Frontend, Platform Ground
187		VIN6	IN	GND	Analog Video 6 C or R SD Input
188		VIN5	IN	GND	Analog Video 5 Y/CVBS Input
189		VIN3	IN	GND	Analog Video 3 CVBS Input
190		VIN2	IN	GND	Analog Video 2 CVBS Input
191		VIN1	IN	GND	Analog Video 1 CVBS Input
192		VSUP3.3VO	SUPPLY	OBL	Supply Voltage Analog Video Output, 3.3 V
193		VOUT3	OUT	LV	Analog cvbs Video 3 Output
194		VOUT2	OUT	OBL	Analog cvbs Video 2 Output
195		VOUT1	OUT	OBL	Analog cvbs Video 1 Output
196		GND3.3IO3	SUPPLY	OBL	Ground Digital Input/Output Port 1
197		VSUP3.3IO3	SUPPLY	OBL	Supply Voltage Input/Output Port 1, 3.3 V
198		656I0 P3_0	IN/OUT	LV	Digital 656 Bit 0 Input (LSB) Port 3, Bit 0 Input/Output
199		656I1 P3_1	IN/OUT	LV	Digital 656 Bit 1 Input Port 3, Bit 1 Input/Output
200		656I2 P3_2	IN/OUT	LV	Digital 656 Bit 2 Input Port 3, Bit 2 Input/Output
201		656I3 P3_3	IN/OUT	LV	Digital 656 Bit 3 Input Port 3, Bit 3 Input/Output
202		656I4 P3_4	IN/OUT	LV	Digital 656 Bit 4 Input Port 3, Bit 4 Input/Output
203		656I5 P3_5	IN/OUT	LV	Digital 656 Bit 5 Input Port 3, Bit 5 Input/Output
204		656I6 P3_6	IN/OUT	LV	Digital 656 Bit 6 Input Port 3, Bit 6 Input/Output
205		656I7 P3_7	IN/OUT	LV	Digital 656 Bit 7 Input Port 3, Bit 7 Input/Output
206		656CLKI	IN/OUT	GND	Digital 656 Clock Input

2.2.1. Pin Connections and Short Description (Continued)

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
207		656CLKO	OUT	LV	Digital 656 Clock Output
208		656O7 P4_7 TCLKFW	IN/OUT	LV	Digital 656 Bit 7 Output Port 4, Bit 7 Input/Output JTAG Interface Clock Input (firmw. Controler)

1) only in RGB output version
2) only in LVDS output version

Display	CRT								FPD											
Application	Analog RGB + SVMOUT + H + V								TTL (Single RGB), LVDS (Dual or Single)								TTL (Dual RGB)			
Panel control									X	X	X	X	X	X	X	X	X	X	X	X
656IN	X	X	X		X	X			X	X	X		X	X			X		X	
656OUT	X	X	X	X					X	X	X	X					X	X		
OSD444	X			X	X		X		X			X	X		X					
OSD222		X				X				X				X						
Port 1	4	4	4	4	4	4	4	4	8	8	8	8	8	8	8	8	8	8	8	8
Port 2	8	8	8	8	8	8	8	8	6	6	6	6	6	6	6	6	6	6	6	6
Port 3		6	8	8		6	8	8		6	6	8		6	8	8		8		8
Port 4	2	2	2	2	8	8	8	8					8	8	8	8			8	8
Max Number of Ports	14	20	22	22	20	26	28	28	14	20	20	22	22	28	30	30	14	22	22	30

Note: 24bit RGB input is always available

Maximum Number of Ports

2.2.2. Pin Descriptions

2.2.2.1. Supply Pins

VSUP1.8DIG – Supply Voltage 1.8 V
This pin is main and standby supply for the digital core logic of controller, video and display processing.

VSUP1.8FE – Supply Voltage 1.8 V
This pin is main and standby supply for the analog video frontend.

VSUP3.3FE – Supply Voltage 3.3 V
This pin is main and standby supply for the analog video frontend.

VSUP3.3VO – Supply Voltage 3.3 V
This pin is main and standby supply for the analog video outputs.

VSUP1.8LVDS – Supply Voltage 1.8 V
This pin is main and standby supply for the analog LVDS core.

VSUP3.3LVDS – Supply Voltage 3.3 V
This pin is main and standby supply for the Digital LVDS port.

VSUP3.3FL – Supply Voltage 3.3 V
This pin is main and standby supply for the Flash device.

VSUP3.3DRI – Supply Voltage 3.3 V
This pin is main supply for the digital RAM interface.

VSUP3.3RAM – Supply Voltage 3.3 V
This pin is main supply for the RAM device

VSUP3.3IO 1-3 – Supply Voltage 3.3 V
This 3 pins are main and standby supply for the digital I/O-ports.

VSUP3.3COM – Supply Voltage 3.3 V
This pin is main and standby supply for the digital Input ports and common digital logic.

VSUP3.3DIG – Supply Voltage 3.3 V
This pin is main supply for the digital core logic of IF and audio processing and digital video backend.

VSUP8.0AU – Supply Voltage 8.0 V
This pin is main supply for the analog audio processing.

VSUP5.0SIF – Supply Voltage 5.0 V
This pin is main supply for the SIF processing.

VSUP3.3DAC – Supply Voltage 3.3 V
This pin is main and standby supply for the Analog DAC.

GND* – Ground
This pin are main ground for all digital analog and port supplies.

Application Note:

All GND pins must be connected to a low-resistive ground plane underneath the IC. All supply pins must be connected separately with short and low-resistive lines to the power supply. Decoupling capacitors from VSUPxx to GND have to be placed as closely as possible to these pins. It is recommended to use more than one capacitor. By choosing different values, the frequency range of active decoupling can be extended.

2.2.2.2 Audio Pins

VREFAU – Reference Voltage for Analog Audio
This pin serves as the internal ground connection for the analog audio circuitry. It must be connected to the **GND** pin with a 3.3 µF and a 100 nF capacitor in parallel.

SGND – Analog Reference Input
This is the reference ground Analog Audio part.

AIN1 R/L – Audio 1 Inputs
The analog input signal for audio 1 is fed to this pin. Analog input connection must be AC coupled.

AIN2 R/L – Audio 2 Inputs
The analog input signal for audio 2 is fed to this pin. Analog input connection must be AC coupled.

AIN3 R/L – Audio 3 Inputs
The analog input signal for audio 3 is fed to this pin. Analog input connection must be AC coupled.

AIN4 R/L – Audio 4 Inputs
The analog input signal for audio 4 is fed to this pin. Analog input connection must be AC coupled.

AIN5 R/L – Audio 5 Inputs
The analog input signal for audio 5 is fed to this pin. Analog input connection must be AC coupled.

AOUT1 R/L – Audio 1 Outputs
Output of the analog audio 1 signal. Connections to these pins are intended to be AC coupled.

AOUT2 R/L – Audio 2 Outputs
Output of the analog audio 2 signal. Connections to these pins are intended to be AC coupled.

SPEAKER R/L – Loudspeaker Outputs
Output of the loudspeaker signal.

HEADPHONES R/L – Headphones Outputs
Output of the headphones signal.

2.2.2. Pin Descriptions (Continued)

SUBWOOFER – Subwoofer Outputs
Output of the subwoofer signal

I2S_DEL_WS - Delay Line Bus Word Strobe
This is the word strobe signal of the delay line bus.

I2S_DEL_CL - Delay Line Bus Clock
This is the Clock signal of the delay line bus.

I2S_DEL_IN - Delay Line Bus Data Input
This is the data input signal of the delay line bus.

I2S_DEL_OUT - Delay Line Bus Data Output
This is the data output signal of the delay line bus.

I2S_WS - I2S Word Strobe
This is the word strobe signal of I2S bus.

I2S_DA_IN - I2S Data Input
This is the data input signal of I2S bus.

I2S_CL - I2S Clock
This is the Clock signal of I2S bus.

SPDIF_OUT -
This is an SPDIF output signal to connect to an A/V receiver.

SIF –/+ – Sound IF Input
This is the SIF input to connect to an external DRX.

VREFSIF – Reference Voltage for SIF
This pin serves as the internal ground connection for the analog audio circuitry.

2.2.2.3 Video Pins

656I 0-7 – Digital 656 Data Input
These are the 8 bits digital 656 video inputs.

656CLKI – Digital 656 Input clock
This is the clock for the digital 656 video inputs.

656O 0-7 – Digital 656 Data Output
These are the 8 bits digital 656 video outputs.

656CLKO– Digital 656 output clock
This is the clock for the digital 656 video outputs.

OSDR 0-3 – Graphic Data input/output
These are the 2 or 4 bit graphic input/output

OSDG 0-3 – Graphic Data input/output
These are the 2 or 4 bit graphic input/output

OSDB 0-3 – Graphic Data input/output
These are the 2 or 4 bit graphic input/output

OSDHCS 0-1 – Graphic Half Contrast Input/Output
This is the half contrast for the graphic input/output

OSDFSW – Graphic Fast Switch Input/Output
This is the fast switch for the graphic input/output

OSDCLK – Graphic clock Input/Output
This is the clock for the graphic video input/output

OSDV – Graphic vertical sync Input/Output
This is the vertical sync for the graphic input/output

OSDH – Graphic horizontal sync Input/Output
This is the horizontal sync signal for the graphic I/O

DRO1_ 0-9 - Digital Red Outputs
This are 10 bits digital signals for red outputs, for dual RGB use bits (0-7).

DGO1_ 0-9 - Digital Green Output
This are 10 bits digital signals for green outputs, for dual RGB use bits (0-7).

DBO1_ 0-9 - Digital Blue Outputs
This are 10 bits digital signals for blue outputs, for dual RGB use bits (0-7).

DRO2_ 0-7 - Digital dual Red Outputs
This are 8 bits digital signals for red outputs.

DGO2_ 0-7 - Digital dual Green Output
This are 8 bits digital signals for green outputs.

DBO2_ 0-7 - Digital dual Blue Outputs
This are 8 bits digital signals for blue outputs.

PCS 0-5 - LCD Panel Control Select Outputs
This are 6 control select signals for LCD outputs.
For CRT application use PCS_0 as H sync and PCS_1 as V sync Back End.

PCLK1,2 - LCD Panel Clock Outputs
This are the clock signals for LCD/RGB outputs.

LVDSA_* - LCD Panel LVDS Outputs
This are 12 signals and clocks for LVDS single or dual output.

LVDSB_* - LCD Panel LVDS Outputs
This are 10 signals and clocks for LVDS dual output.

REXT - LVDS External Resistor
This pin is connected to the external LVDS resistor. (6.2 kOhm to gnd)

DRI 0-7 - Digital video inputs for Red
This are 8 bits digital inputs for red signal

DGI 0-7- Digital video inputs for Green
This are 8 bits digital inputs for green signal

DBI 0-7- Digital video inputs for Blue
This are 8 bits digital inputs for blue signal.

DEN - Digital video inputs Enable
This is the enable signal for the Digital Video Inputs.

DHS - Digital video inputs Horizontal Sync
This is the H Sync signal for the Digital RGB input bus or for the VGA Video Inputs.

DVS - Digital video inputs Vertical Sync
This is the V Sync signal for the Digital RGB input bus or for the VGA Video Inputs.

DCLK - Digital video inputs Clock
This is the Clock signal for the Digital Video Inputs.

CLKOUT – Digital Output clock
This is a 20MHz clock for the external video ICs.

VIN 1–22 – Analog Video Input
These are the 19 analog video inputs.
(Vin 4,10 and 14 are missing)
A CVBS, S-VHS, YCrCb or RGB signal is converted using the luma, chroma and component AD converter.
Vin 8,18 are fast blank inputs. Vin22 is an Hsync input.
The input signals must be AC-coupled.

VOUT 1-3 – Analog Video Output
The analog video inputs that are selected by the video matrix are output at these pins.

ROUT, GOUT, BOUT – Analog RGB Output
These pins are the analog Red/Green/Blue outputs of the back-end.

SVMOUT – Scan Velocity Modulation Output
This output delivers the analog SVM signal. The D/A converter is a current sink like the RGB D/A converters. At zero signal the output current is 50% of the maximum output current.

2.2.2.4 Controller Pins

XTALIN Crystal Input and **XTALOUT** Crystal Output
These pins are connected to an 20.25 MHz crystal oscillator. An external clock can be fed into XTALIN.

RESETQ – Reset Input/Output
A low level on this pin resets the VCT 69xyP. The internal CPU can pull down this pin to reset external devices connected to this pin.

TEST – Test Input
This pin enables factory test modes. For normal operation, it must be connected to ground.

SCL – I^2C Bus Clock
This pin delivers the I^2C bus clock line. The signal can be pulled down by external slave ICs to slow down data transfer.

SDA – I^2C Bus Data
This pin delivers the I^2C bus data line.

P1_0–**P1_3** – I/O Port
These pins provide CPU controlled I/O ports.

P1_4–**P1_7** – I/O Port
These pins provide CPU controlled I/O ports.
Also used as **CADC1**–**4** – Controller A/D inputs 1 to 4.
This 4 pins are analog/digital converters from the controller

P2_0–**P2_7** – I/O Port
These pins provide CPU controlled I/O ports.

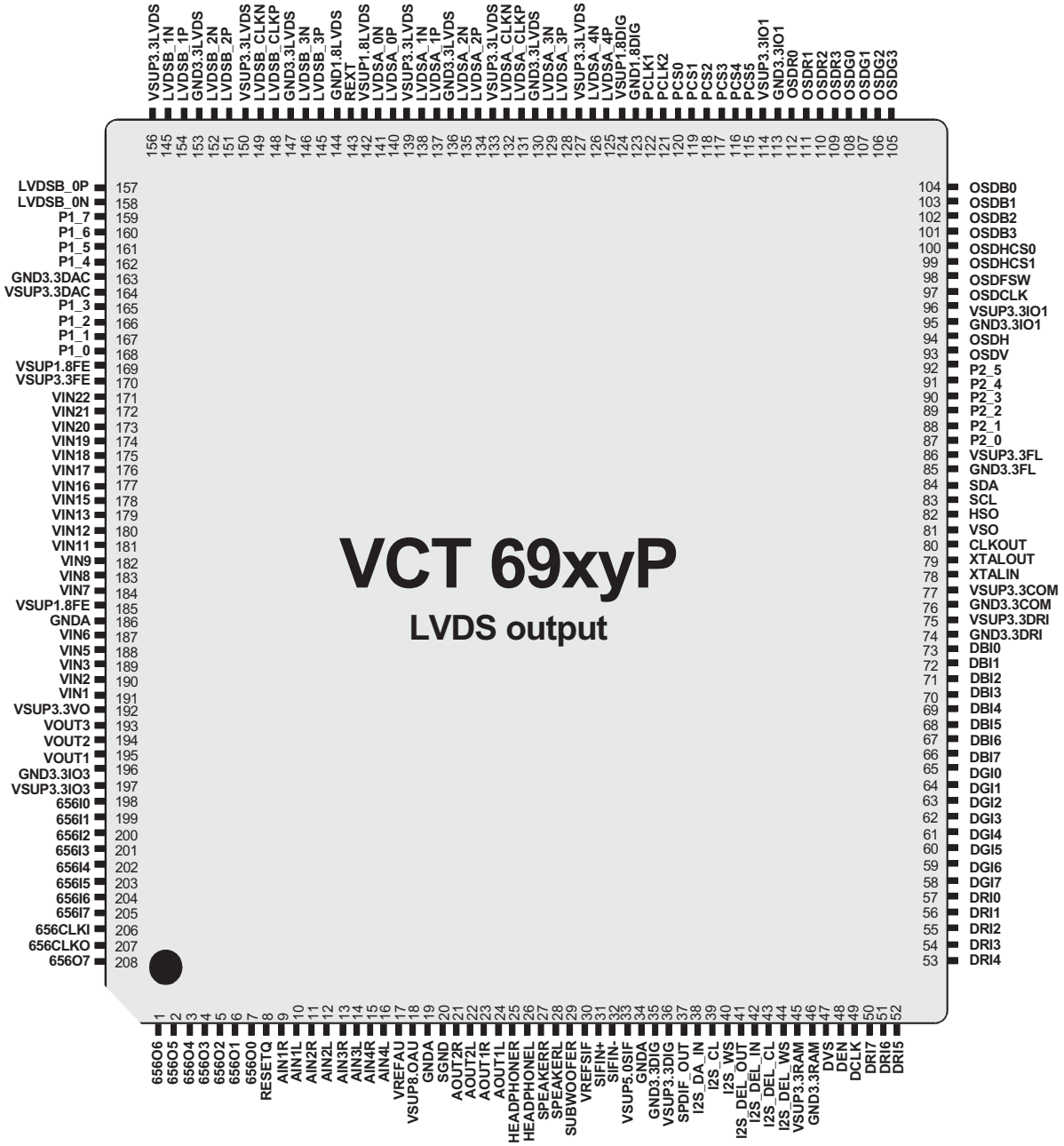
P3_0–**P3_7** – I/O Port
These pins provide CPU controlled I/O ports.

P4_0–**P4_7** – I/O Port
These pins provide CPU controlled I/O ports.

TDO-TCLK-TDI-TMS -JTAG Interface Pins for TV controler.
TCLK at pin 4 (656O3) has during reset an internal pull up: (TCLK=0) at end of reset enables the JTAG mode at 656 LSB's, this can also be done via I2C.
This JTAG is also available at Port(1 and 2) but only via I2C.

TDOFW-TCLKFW-TDIFW-TMSFW -JTAG Interface Pins for firmware controler.
TCLKFW at pin 208 (656O7) has during reset an internal pull up: (TCLKFW=0) at end of reset enables the JTAG mode, this can also be done via I2C.

2.2.3. Pinning



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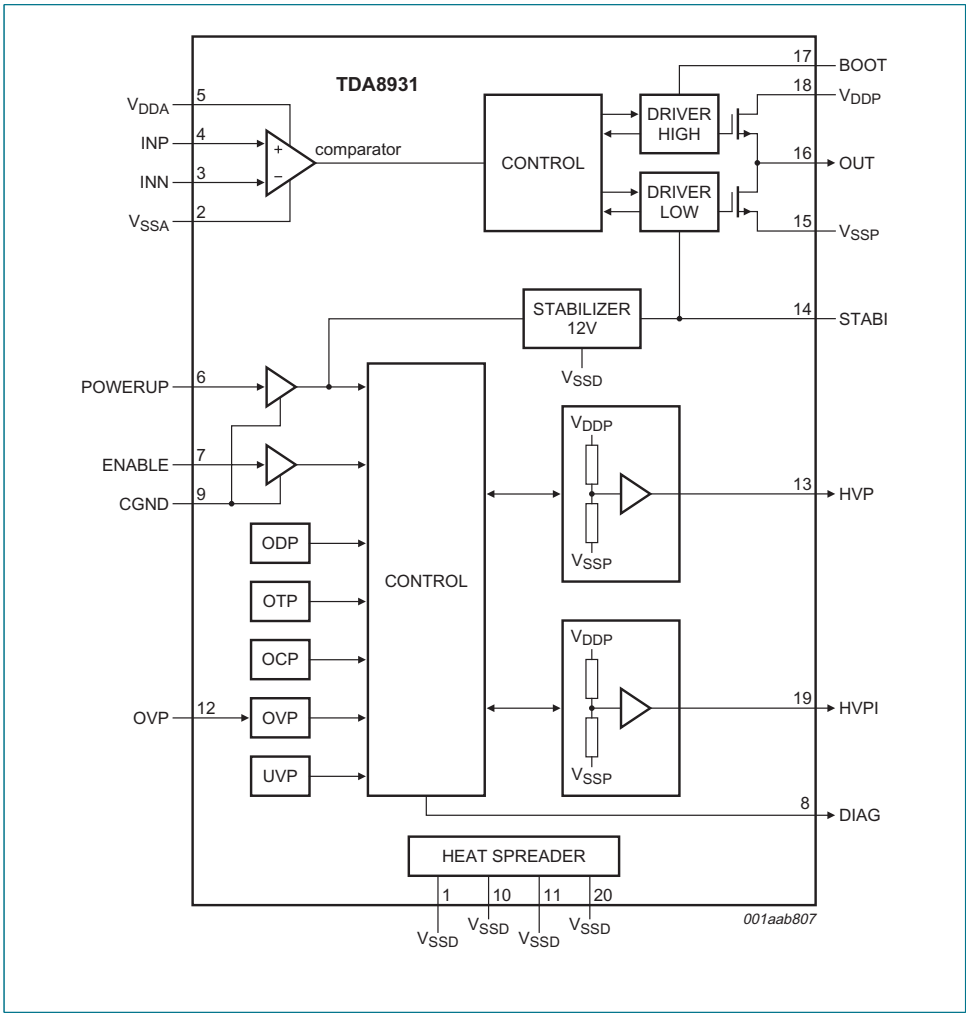
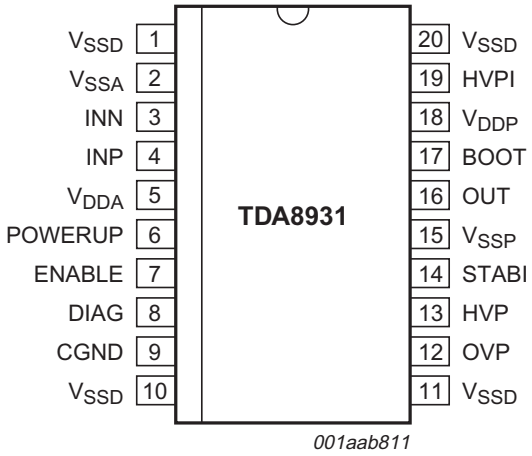
2.3. IC301, IC302 (VHITDA8931T-1Y)

2.3.1. Block Diagram

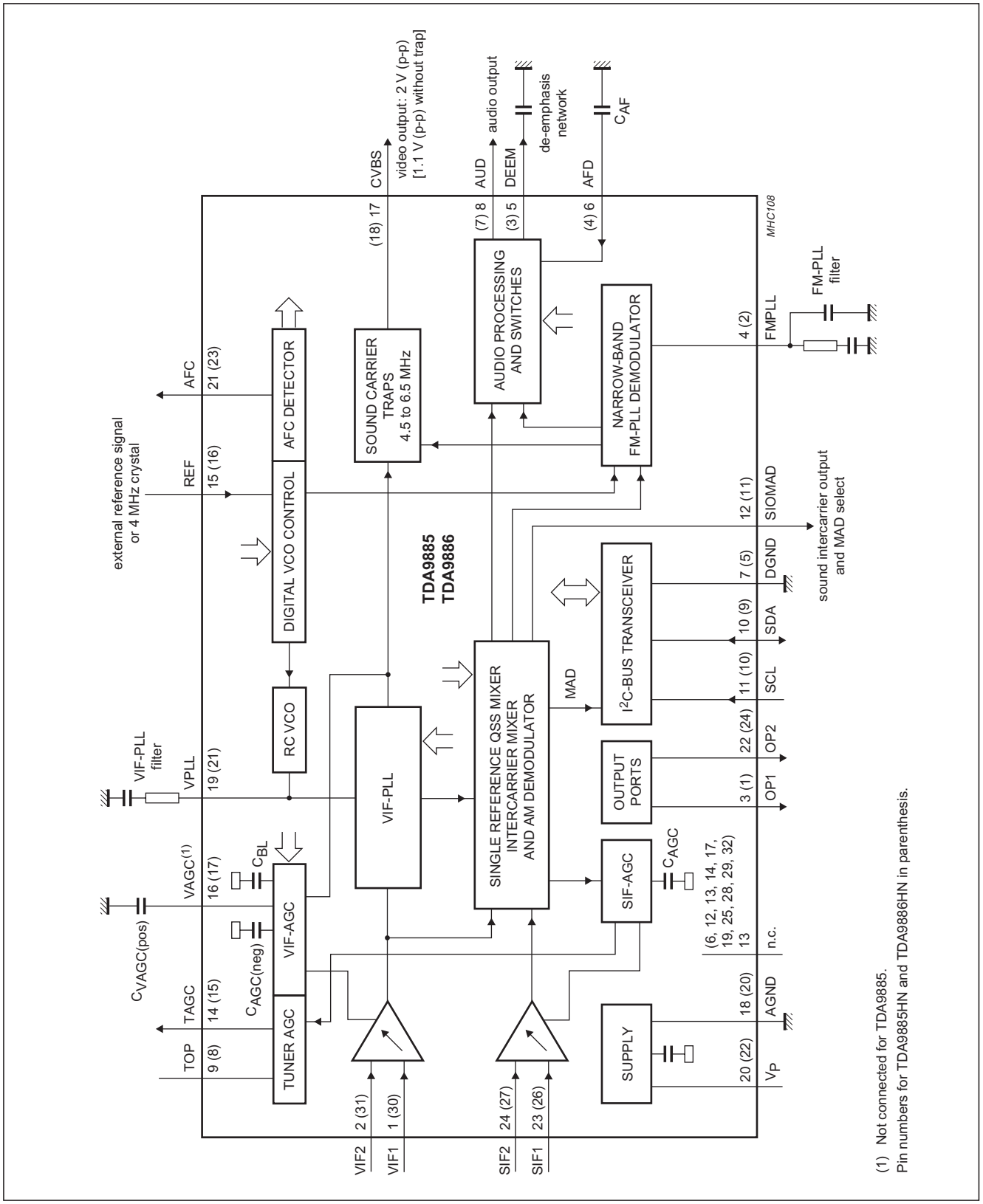


2.3.2. Pinning



2.4. IC201 (VHITDA9886+-1Y)

2.4.1. Block Diagram

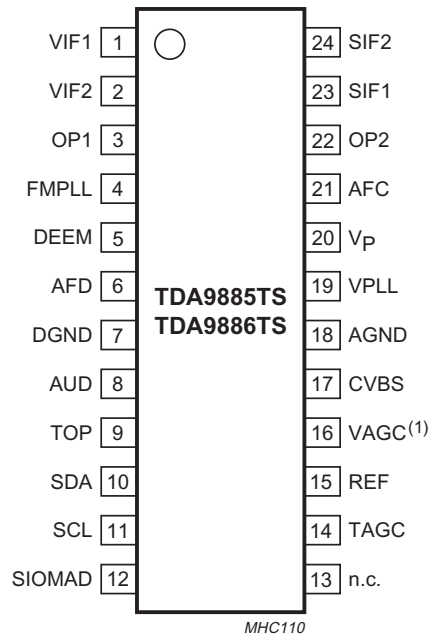


(1) Not connected for TDA9885.
Pin numbers for TDA9885HN and TDA9886HN in parenthesis.

2.4.2. Pinning

SYMBOL	PIN				DESCRIPTION
	TDA9885T TDA9885TS	TDA9886T TDA9886TS	TDA9885HN	TDA9886HN	
VIF1	1	1	30	30	VIF differential input 1
VIF2	2	2	31	31	VIF differential input 2
n.c.	–	–	32	32	not connected
OP1	3	3	1	1	output port 1; open-collector
FMPLL	4	4	2	2	FM-PLL for loop filter
DEEM	5	5	3	3	de-emphasis output for capacitor
AFD	6	6	4	4	AF decoupling input for capacitor
DGND	7	7	5	5	digital ground
n.c.	–	–	6	6	not connected
AUD	8	8	7	7	audio output
TOP	9	9	8	8	tuner AGC TakeOver Point (TOP) for resistor adjustment
SDA	10	10	9	9	I^2C-bus data input and output
SCL	11	11	10	10	I^2C-bus clock input
SIOMAD	12	12	11	11	sound intercarrier output and MAD select with resistor
n.c.	–	–	12	12	not connected
n.c.	13	13	13	13	not connected
n.c.	–	–	14	14	not connected
TAGC	14	14	15	15	tuner AGC output
REF	15	15	16	16	4 MHz crystal or reference signal input
VAGC	–	16	–	17	VIF-AGC for capacitor
n.c.	16	–	17	–	not connected
CVBS	17	17	18	18	composite video output
n.c.	–	–	19	19	not connected
AGND	18	18	20	20	analog ground
VPLL	19	19	21	21	VIF-PLL for loop filter
V_P	20	20	22	22	supply voltage
AFC	21	21	23	23	AFC output
OP2	22	22	24	24	output port 2; open-collector
n.c.	–	–	25	25	not connected
SIF1	23	23	26	26	SIF differential input 1 and MAD select with resistor
SIF2	24	24	27	27	SIF differential input 2 and MAD select with resistor
n.c.	–	–	28	28	not connected
n.c.	–	–	29	29	not connected

2.4.2. Pinning (Continued)



(1) Not connected for TDA9885TS.

Fig.3 Pin configuration for SSOP24.

SOURCE OF DOCUMENTATION

IC1905 SiI9021.

SILICON IMAGE Data Sheet:
SiI9021 HDMI PanelLink Cinema Receiver
Doc: SiL-DS-0117-A . August 2004.

IC201 TDA9886.

PHILIPS Semiconductors Product Specification:
TDA9885;TDA9886 I2C-bus controlled single and multistandard alignment-free IF-PLL demodulators. 2003 Oct 02
http://www.semiconductors.philips.com/acrobat_download/datasheets/TDA9885_TDA9886_2.pdf

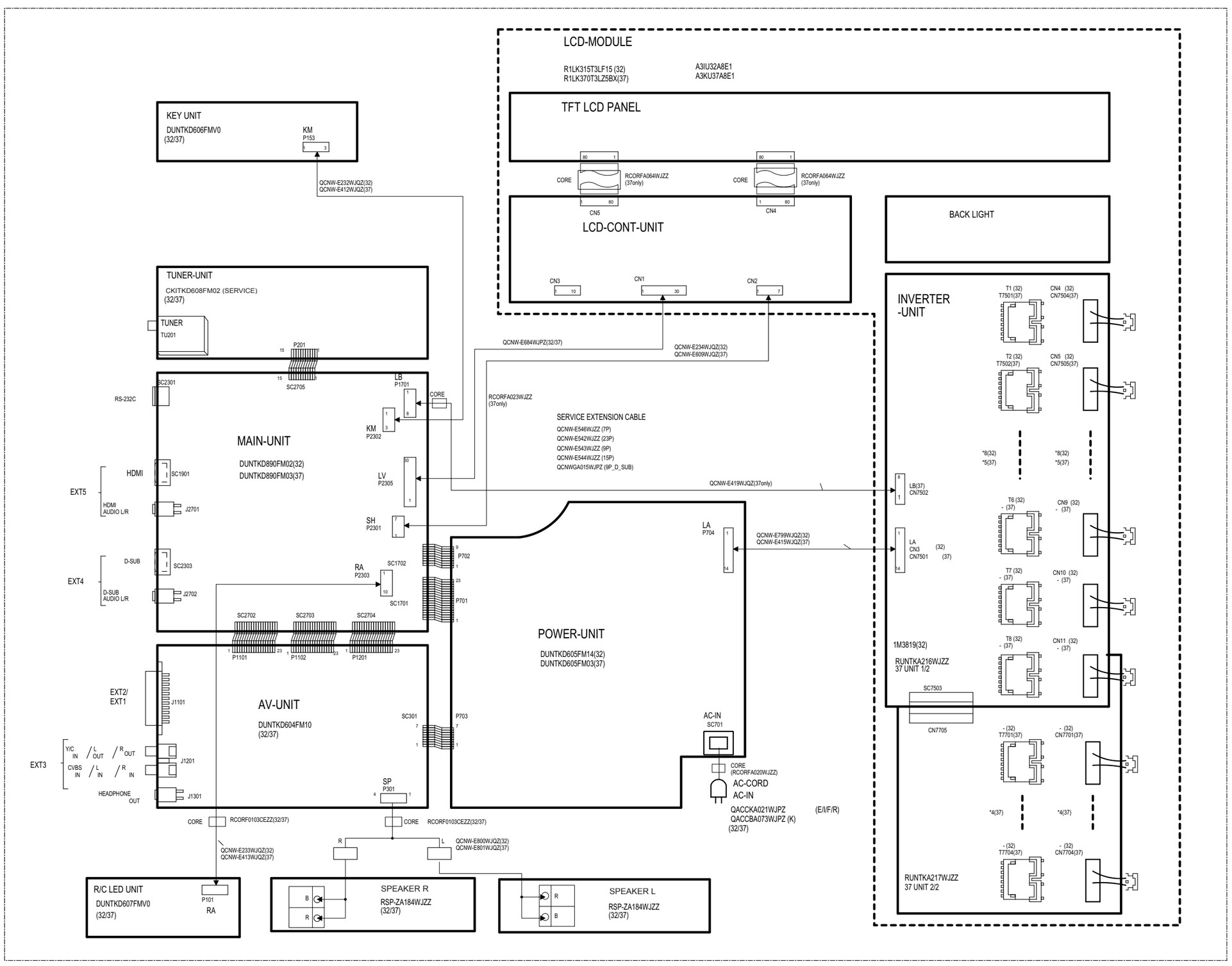
IC301, IC302 TDA8931.

PHILIPS Semiconductors Preliminary Data Sheet:
TDA8931 Power Comparator 1x20W
Doc: 9397 750 13847 Rev.01. 14 January 2004
http://www.semiconductors.philips.com/acrobat_download/datasheets/TDA8931_1.pdf

IC3002 VCT69xyP.

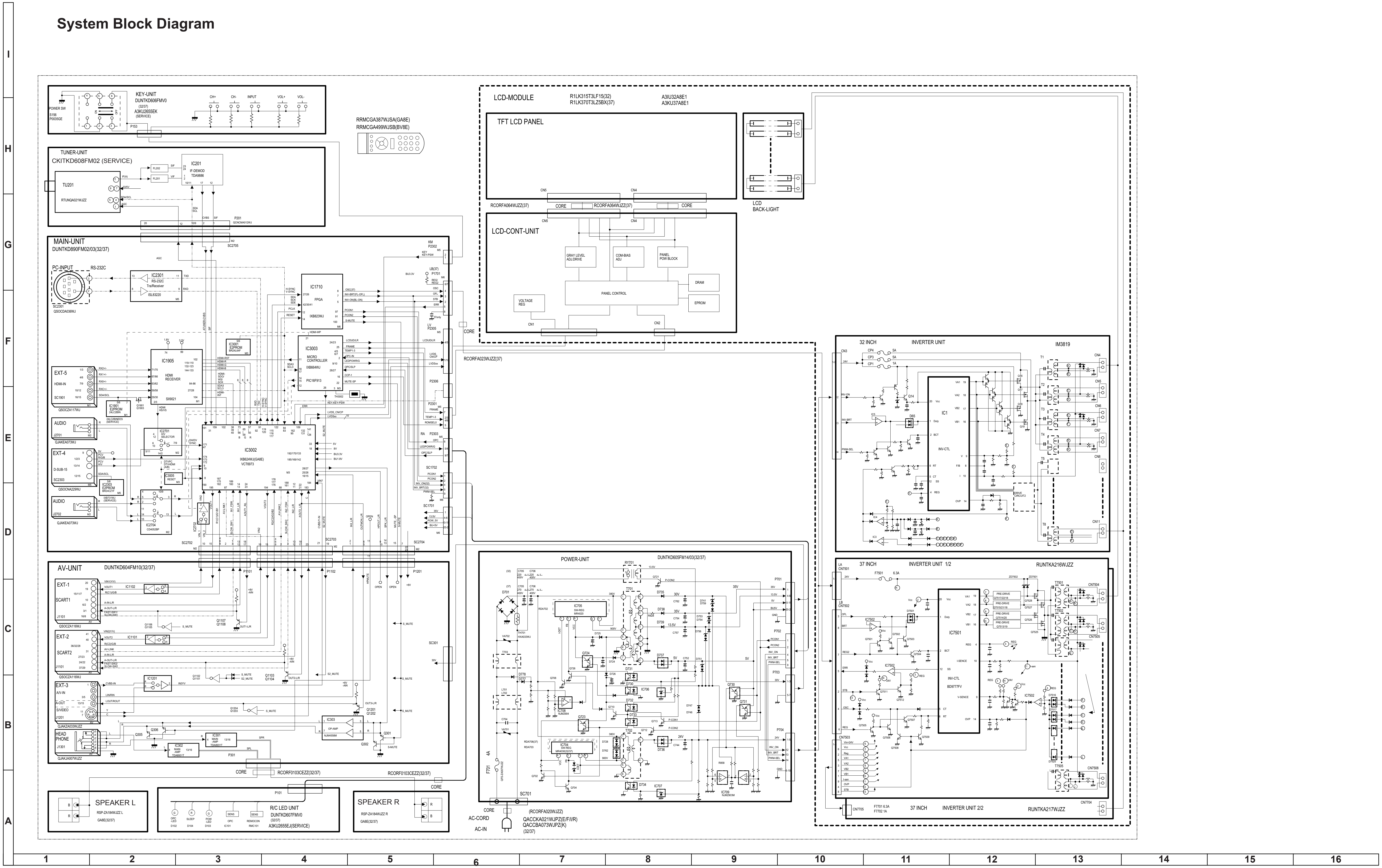
MICRONAS Avance Information:
VCT69xyP Video-Controller-Text-Audio IC Family for DoubleScan and FPD TV
Doc: 6251-644-1-1AI. November 3, 2004

OVERALL WIRING DIAGRAM

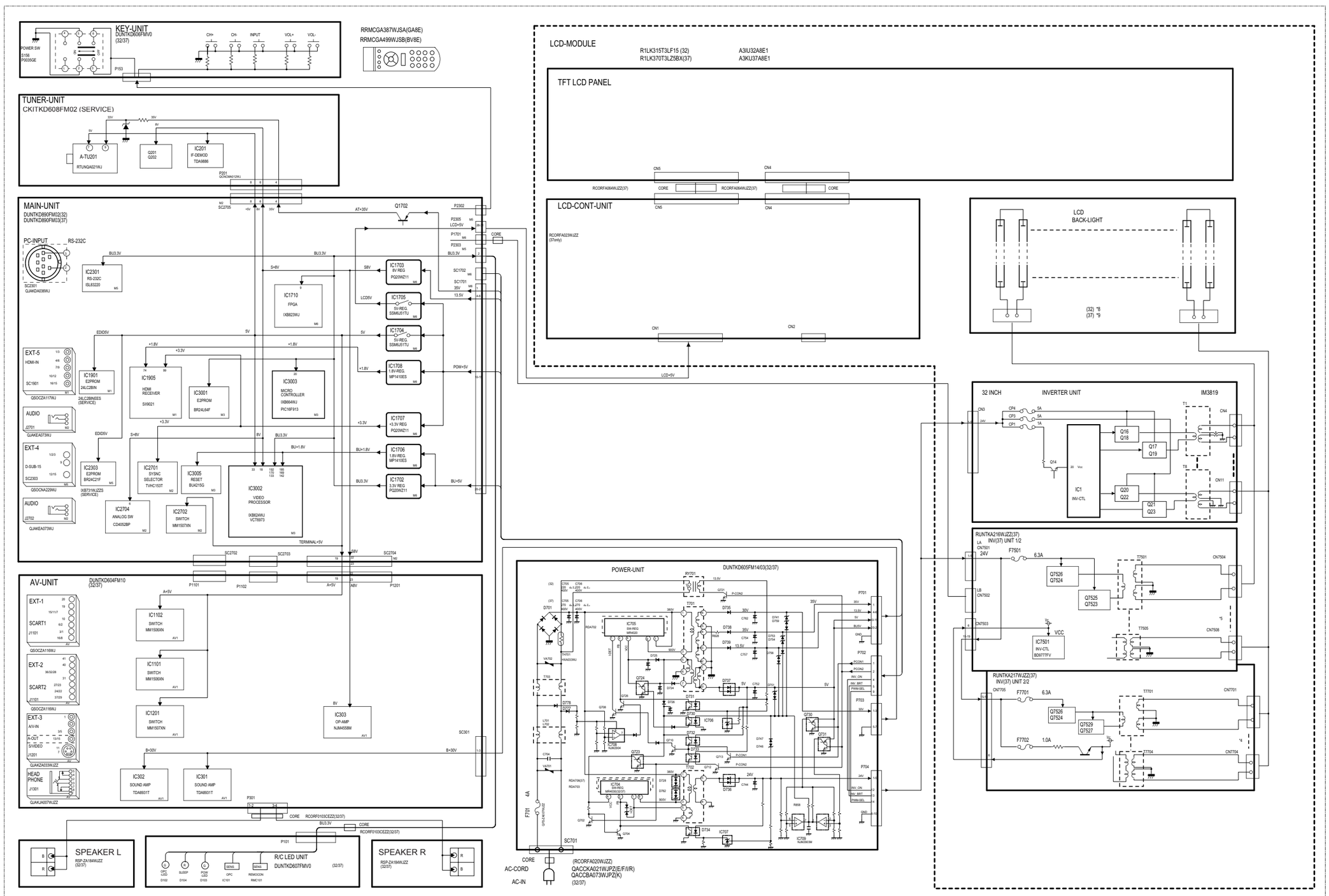


BLOCK DIAGRAM

System Block Diagram



Power-Source Block Diagram



SCHEMATIC DIAGRAMS

Description:

VOLTAGE MEASUREMENT CONDITION:

1. The voltages at test points are measured on exclusive AC adaptor and the stable supply voltage of AC 230V. Signals are fed by a color bar signal generator for servicing purpose and the above voltages are measured with a 20k ohm/V tester.

INDICATION OF RESISTOR & CAPACITOR:

RESISTOR

1. The unit of resistance "Ω" is omitted. (K=kΩ=1000 Ω, M=MΩ).
2. All resistors are ± 5%, unless otherwise noted. (J= ± 5%, F= ± 1%, D= ± 0.5%)
3. All resistors are 1/16W, unless otherwise noted.
4. All resistors are Carbon type, unless otherwise noted.

Ⓒ: Solid Ⓦ: Cement
Ⓢ: Oxide Film Ⓣ: Special
Ⓝ: Metal Coating

CAPACITOR

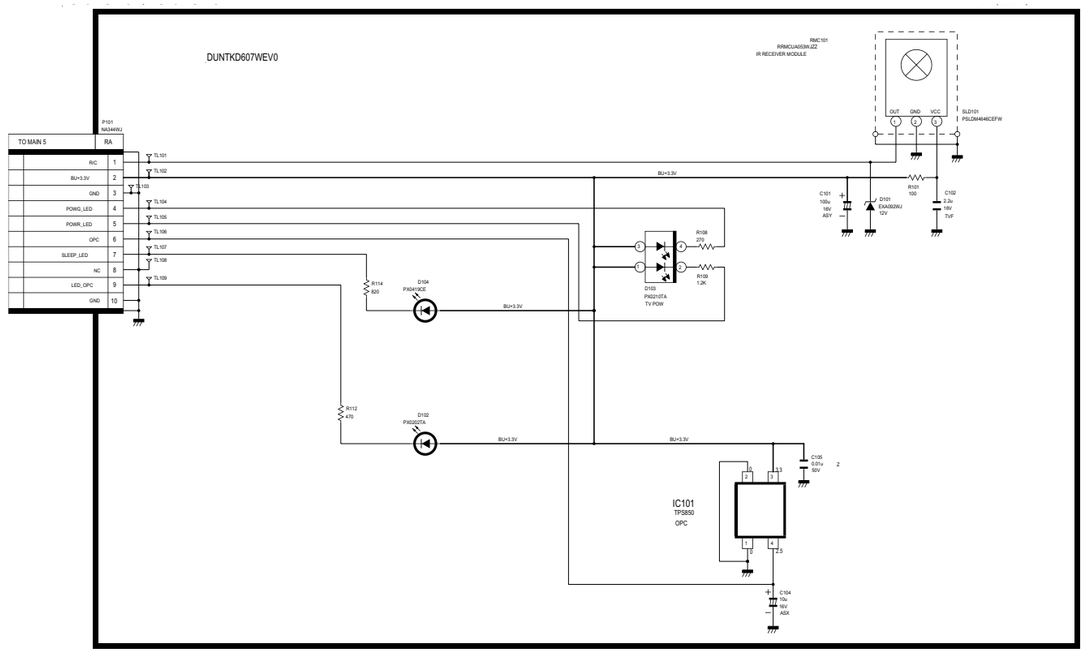
1. All capacitors are μF, unless otherwise noted. (P=pF=μμ F).
2. All capacitors are 50V, unless otherwise noted.
3. All capacitors are Ceramic type, unless otherwise noted.

(ML): Mylar (TA): Tantalum
(PF): Polypro Film (ST): Styrol

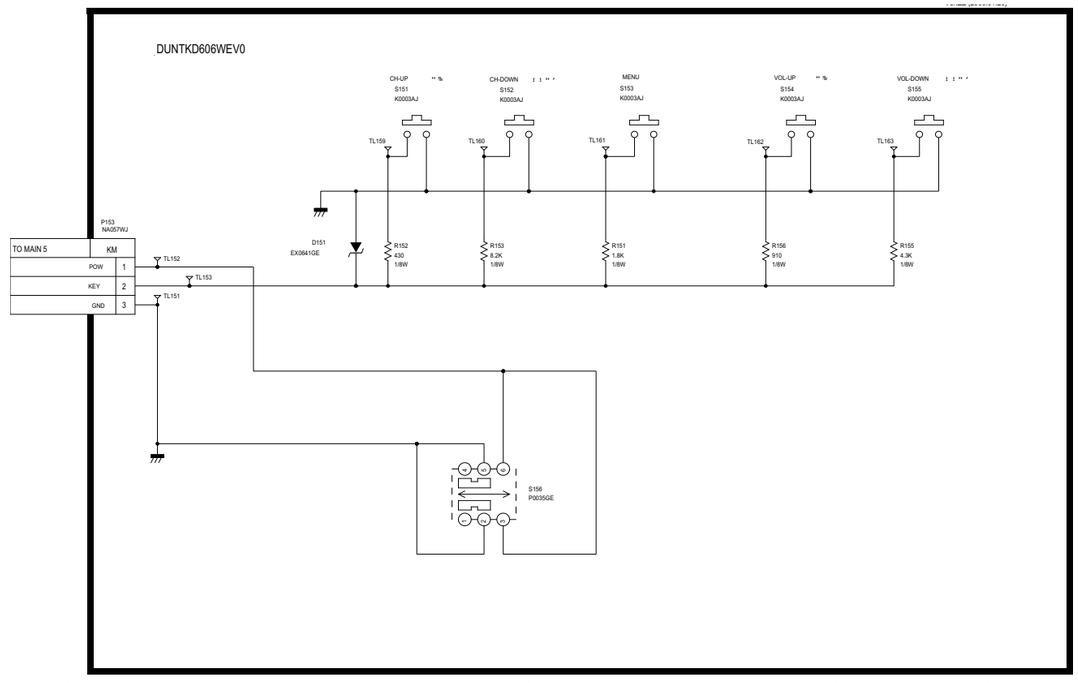
CAUTION:
This circuit diagram is original one, therefore there may be a slight difference from yours.

IMPORTANT SAFETY NOTICE:
PARTS MARKED WITH "⚠" ( ) ARE IMPORTANT FOR MAINTAINING THE SAFETY OF THE SET. BE SURE TO REPLACE THESE PARTS WITH SPECIFIED ONES FOR MAINTAINING THE SAFETY AND PERFORMANCE OF THE SET.

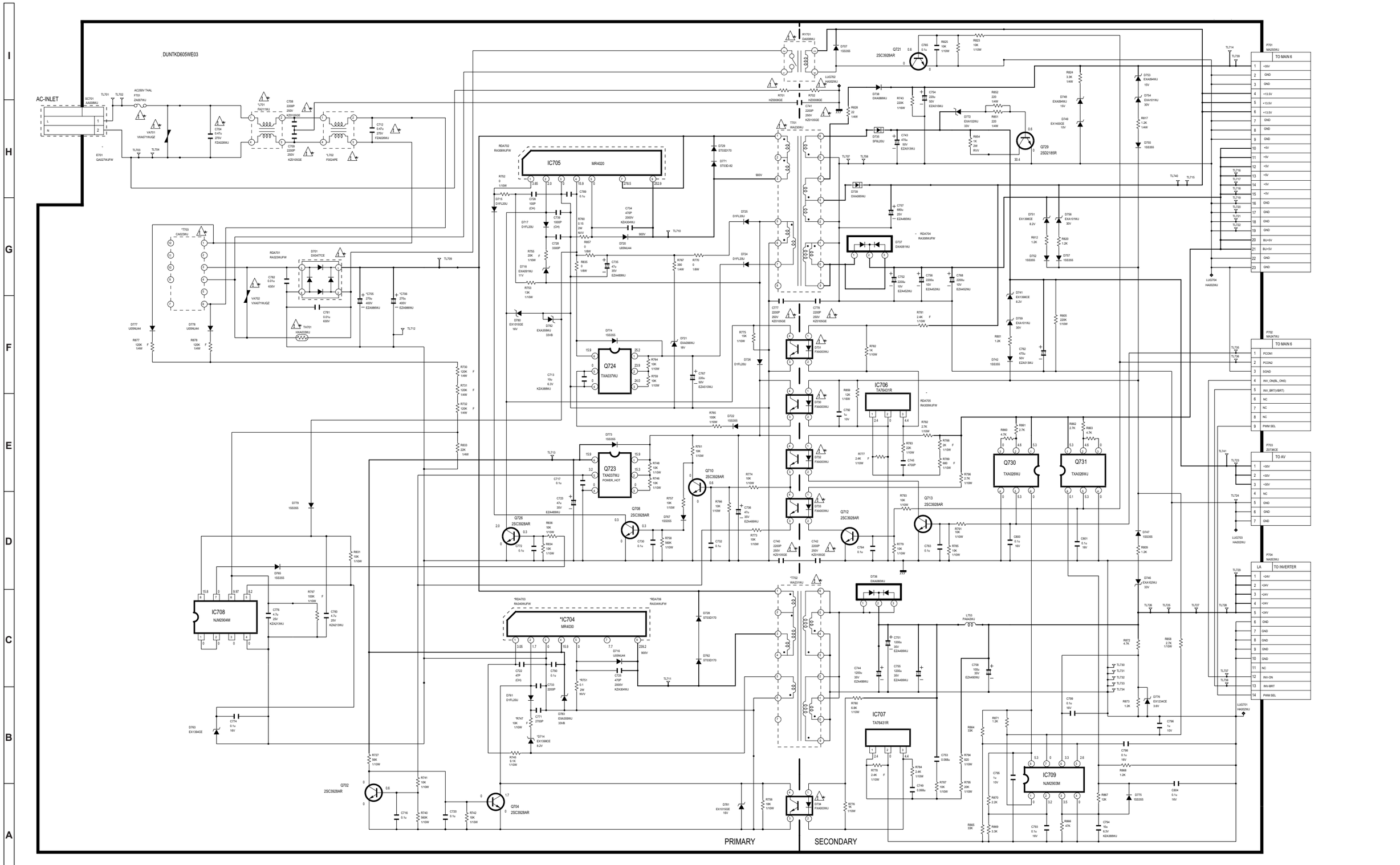
LC-32/37GA8E RC/LED Unit Diagram



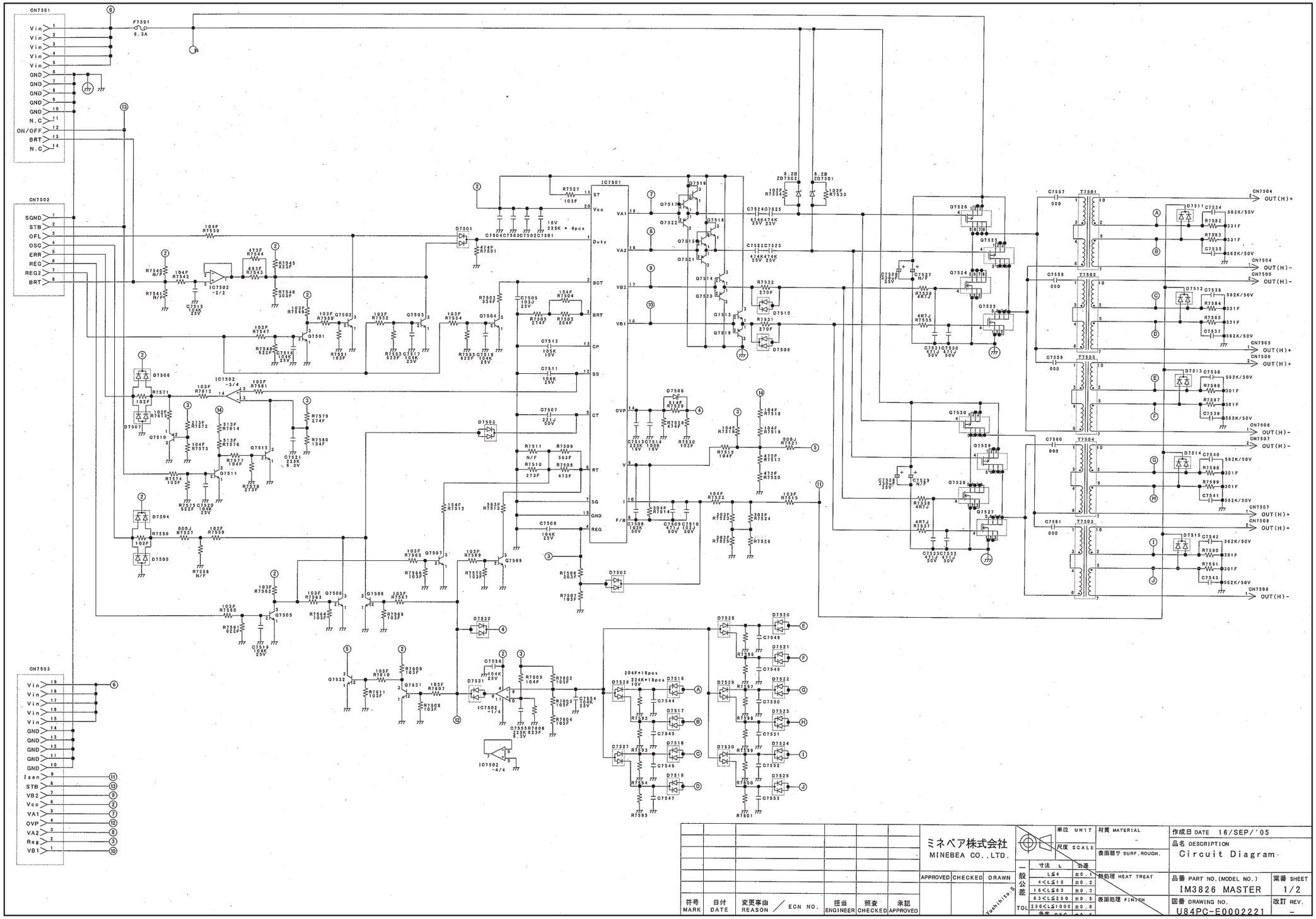
LC-32/37GA8E KEY Unit Diagram



LC-37GA8E POWER SUPPLY Unit Diagram



LC-37GA8E INVERTER Unit Diagram (RUNTKA216WJZZ)



符号 MARK	日付 DATE	変更事由 REASON / ECN NO.	担当 ENGINEER	照査 CHECKED	承認 APPROVED

ミネベア株式会社
MINEBEA CO.,LTD.

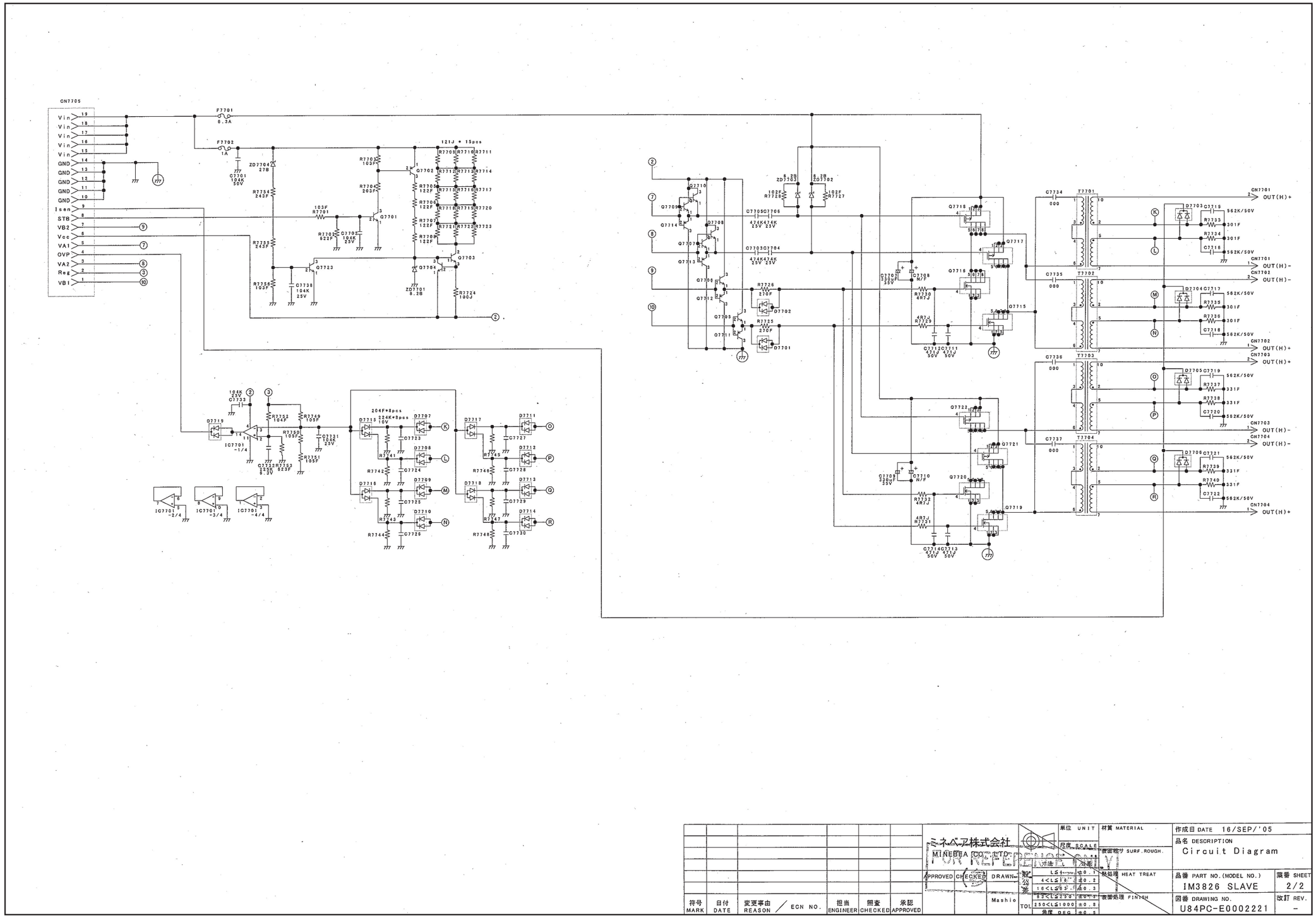
APPROVED	CHECKED	DRAWN
		Yoshito.S

単位 UNIT	材質 MATERIAL	作成日 DATE 16/SEP/'05
尺度 SCALE	表面粗さ SURF.ROUGH.	品名 DESCRIPTION Circuit Diagram

一般公差 寸法 L	公差
L≦4	±0.1
4<L≦16	±0.2
16<L≦63	±0.3
63<L≦250	±0.5
250<L≦1000	±0.8

熱処理 HEAT TREAT	品番 PART NO.(MODEL NO.) IM3826 MASTER	葉番 SHEET 1/2
表面処理 FINISH	図番 DRAWING NO. U84PG-E0002221	改訂 REV. -

LC-37GA8E INVERTER Unit Diagram (RUNTKA217WJZZ)



符号 MARK	日付 DATE	変更事由 REASON / ECN NO.	担当 ENGINEER	照査 CHECKED	承認 APPROVED

ミネベア株式会社
MINEBEA CO., LTD.

APPROVED	CHECKED	DRAWN
		Mashio

単位 UNIT | 材質 MATERIAL | 作成日 DATE 16/SEP/'05

尺度 SCALE | 表面粗さ SURF. ROUGH. | 品名 DESCRIPTION Circuit Diagram

寸法 | 公差

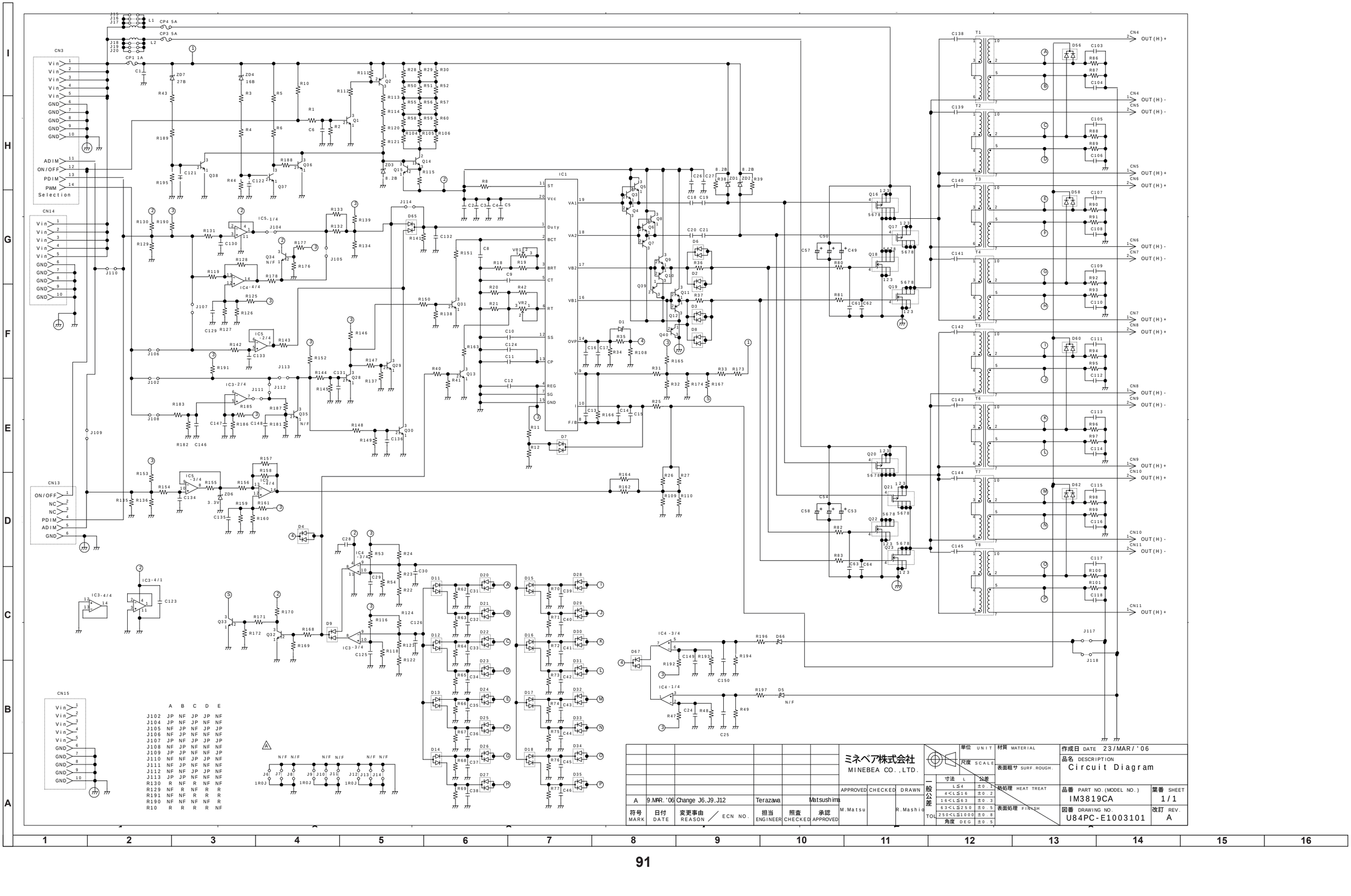
寸法	公差
L≦4	±0.1
4<L≦18	±0.2
18<L≦63	±0.3
63<L≦250	±0.5
250<L≦1000	±0.8
角度 DEG	±0.5

熱処理 HEAT TREAT | 表面処理 FINISH

品番 PART NO.(MODEL NO.) IM3826 SLAVE | 葉番 SHEET 2/2

図番 DRAWING NO. U84PC-E0002221 | 改訂 REV. -

LC-32GA8E INVERTER Unit Diagram (RDENC2266TPZC)



	A	B	C	D	E
J102	JP	NF	JP	JP	NF
J104	JP	NF	JP	NF	NF
J105	NF	JP	NF	JP	JP
J106	NF	JP	NF	NF	NF
J107	JP	NF	JP	JP	JP
J108	NF	JP	NF	NF	NF
J109	JP	JP	NF	NF	JP
J110	NF	NF	JP	JP	NF
J111	NF	JP	NF	NF	NF
J112	NF	NF	JP	JP	NF
J113	JP	JP	NF	NF	NF
R130	R	NF	R	NF	NF
R129	NF	R	NF	R	R
R191	NF	NF	R	R	R
R190	NF	NF	NF	NF	R
R10	R	R	R	R	NF

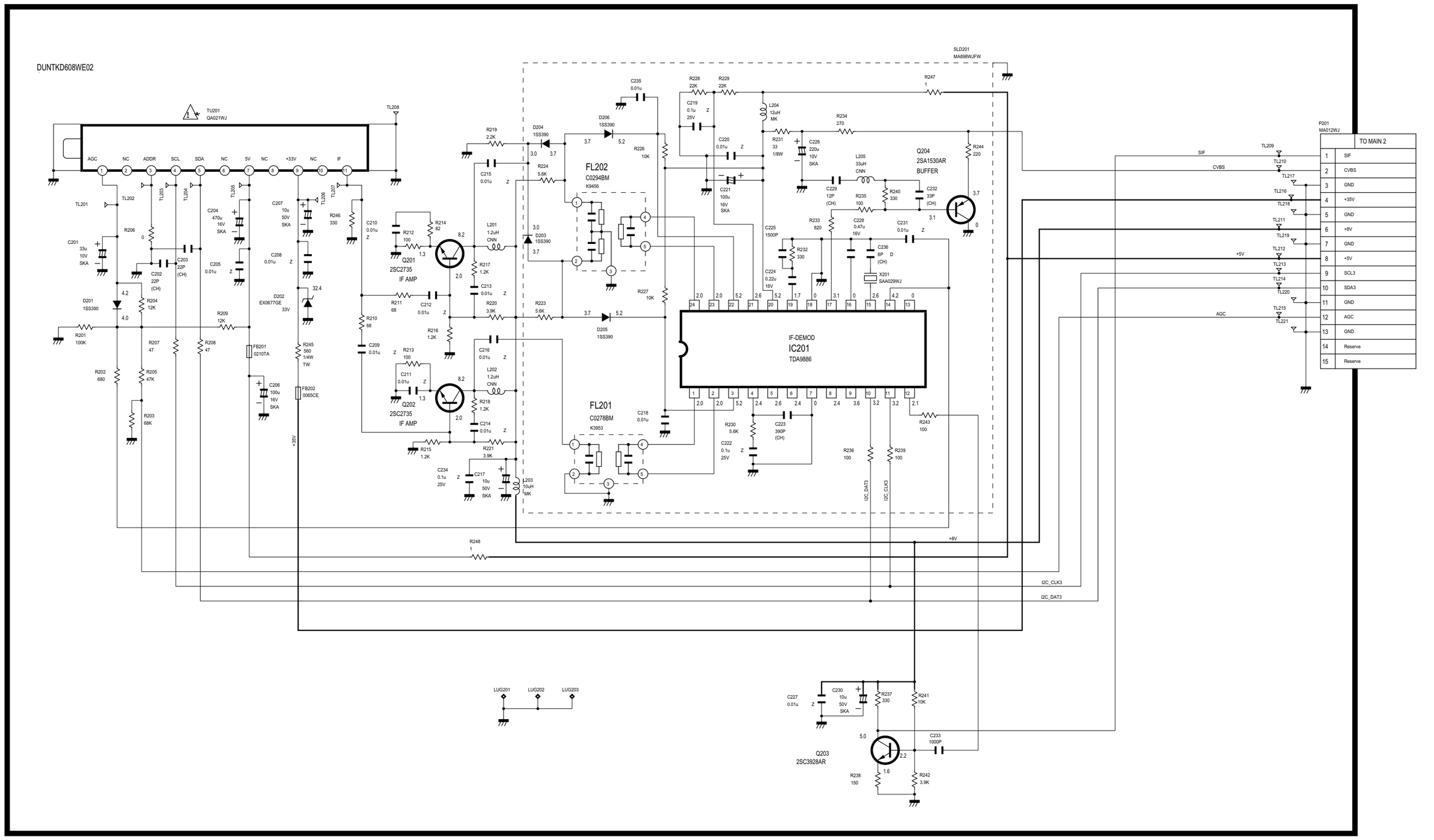
MARK	DATE	REASON / ECN NO.	ENGINEER	CHECKED	APPROVED
A	9.MAR.'06	Change J6,J9,J12			

APPROVED	CHECKED	DRAWN
M.Matsu		R.Mashio

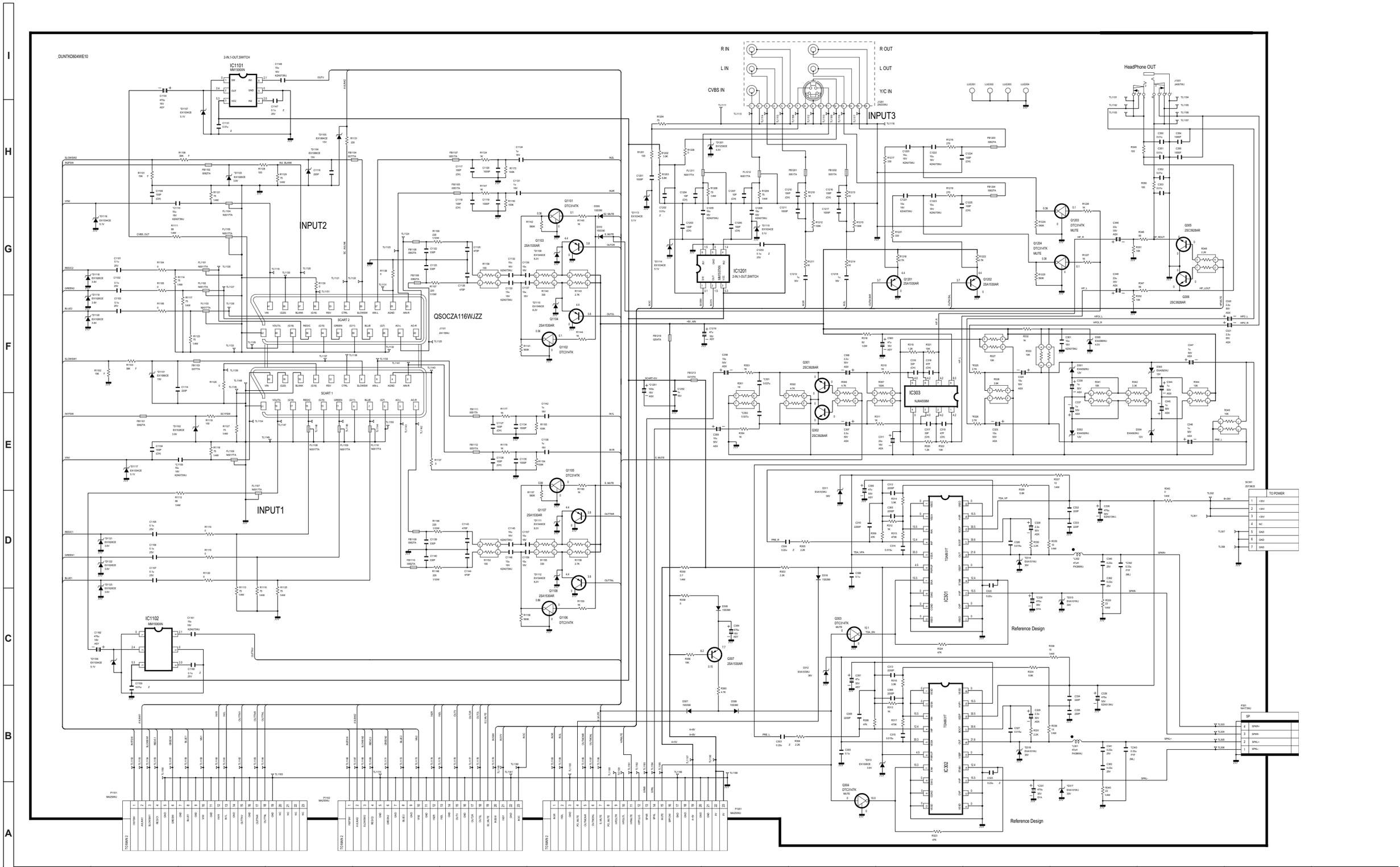
一般公差 TOL	寸法 L	公差
	L≦4	±0.1
	4<L≦16	±0.2
	16<L≦63	±0.3
	63<L≦250	±0.5
	250<L≦1000	±0.8
	角度 DEG	±0.5

単位 UNIT	
尺度 SCALE	
材質 MATERIAL	
表面粗サ SURF.ROUGH.	
熱処理 HEAT TREAT	
表面処理 FINISH	
作成日 DATE	23/MAR/'06
品名 DESCRIPTION	Circuit Diagram
品番 PART NO.(MODEL NO.)	IM3819CA
葉番 SHEET	1/1
図番 DRAWING NO.	U84PC-E1003101
改訂 REV.	A

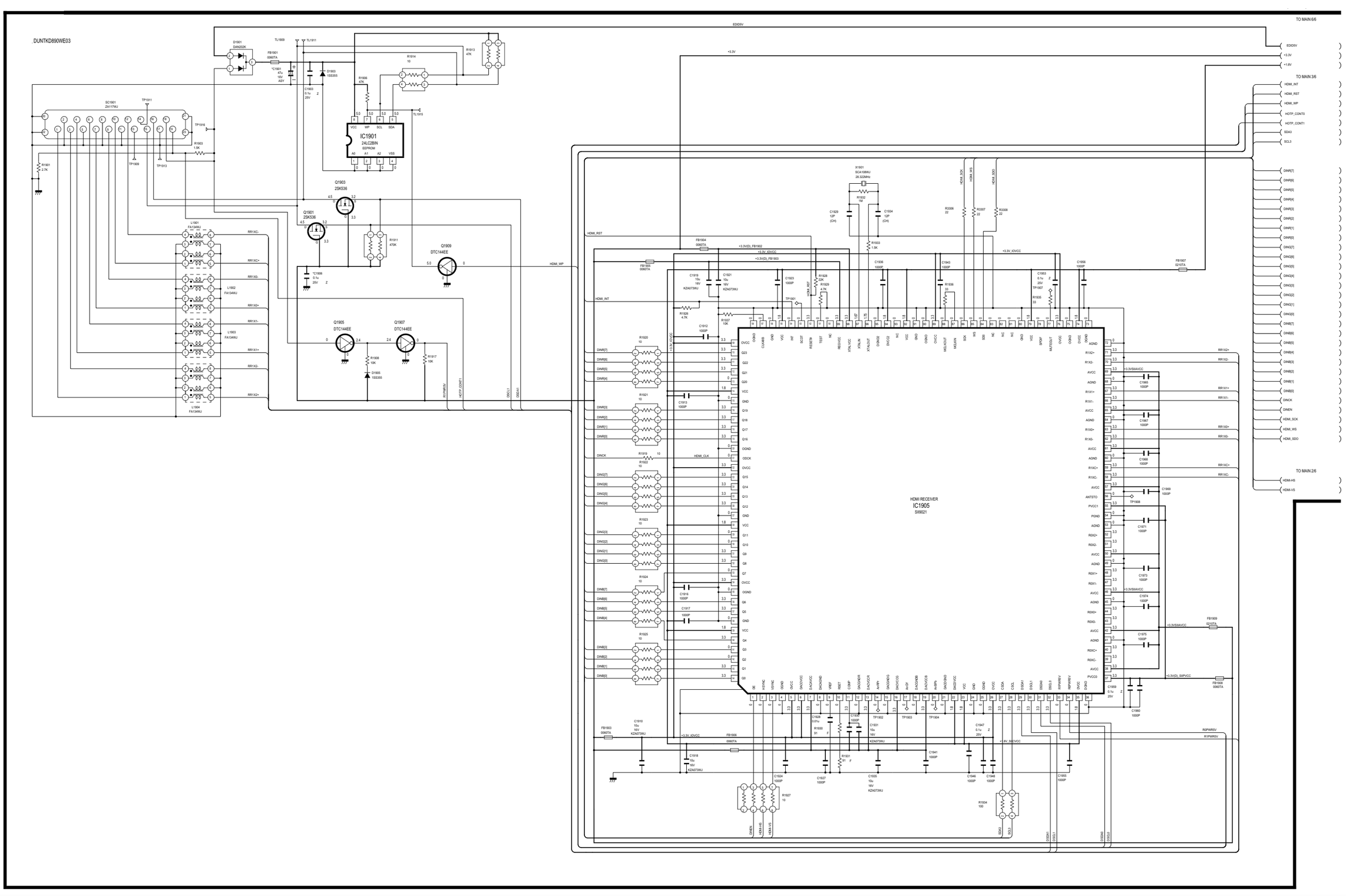
LC-32/37GA8E TUNER Unit Diagram



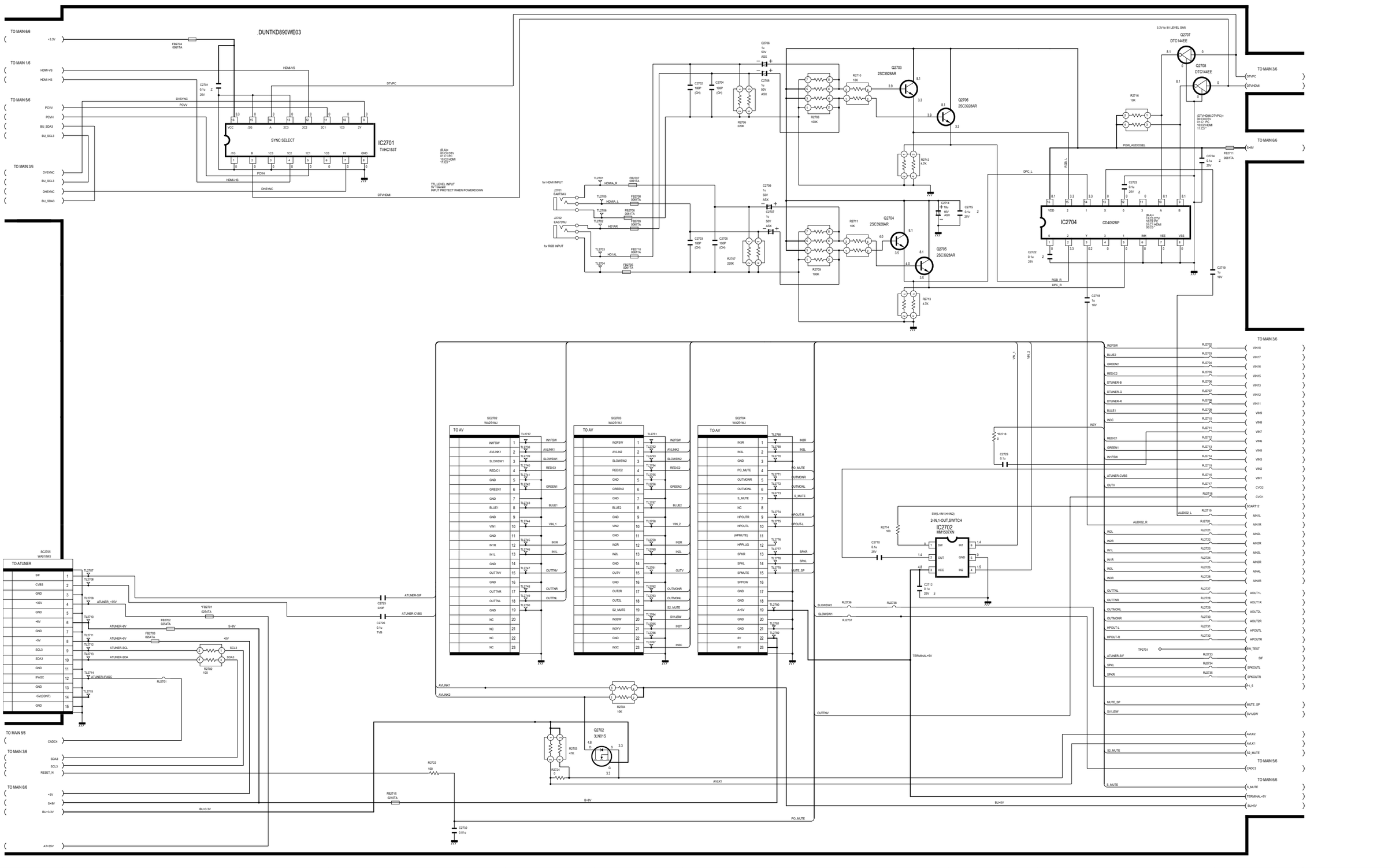
LC-32/37GA8E AV Unit Diagram



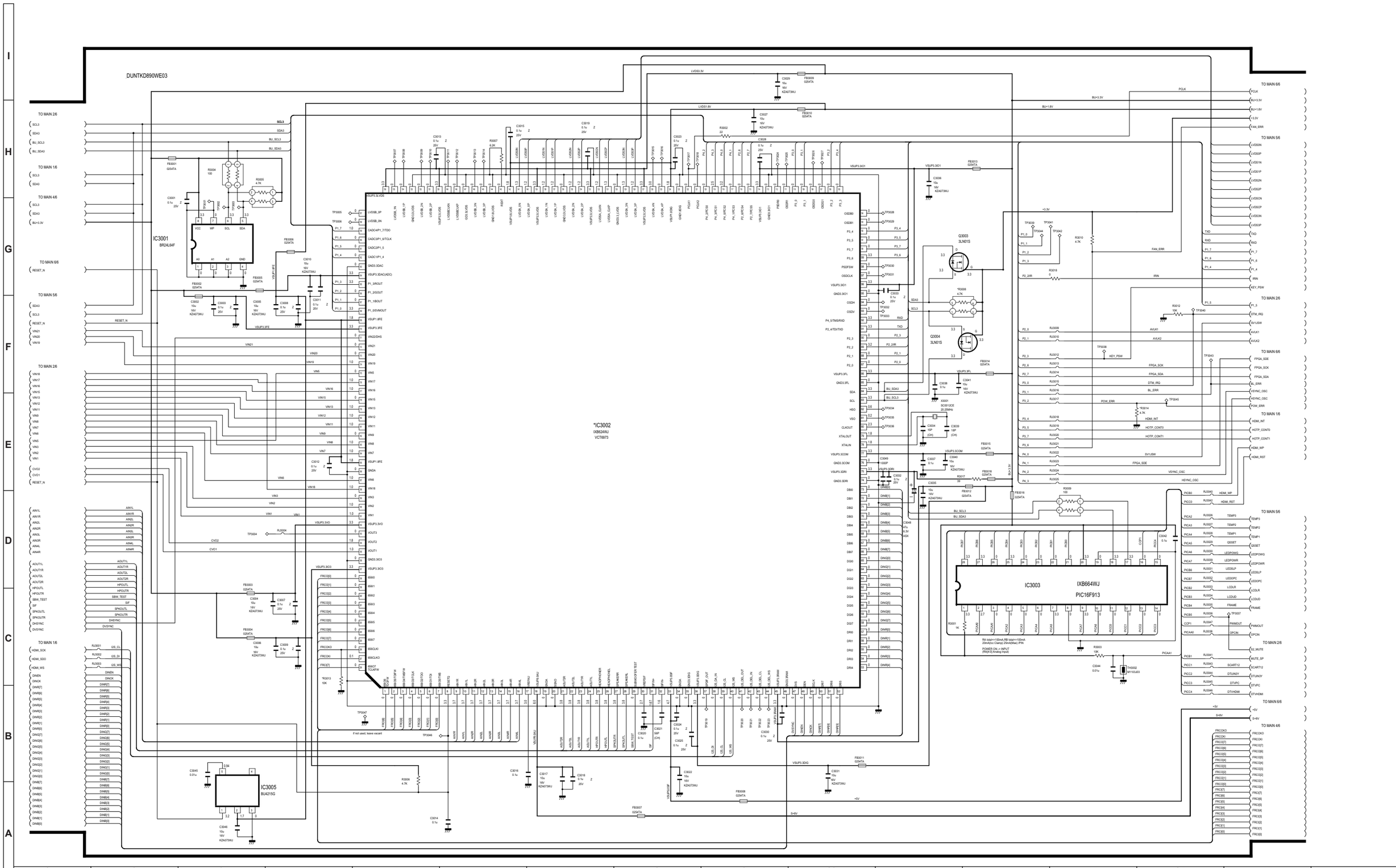
LC-37GA8E Main Unit Diagram (HDMI)



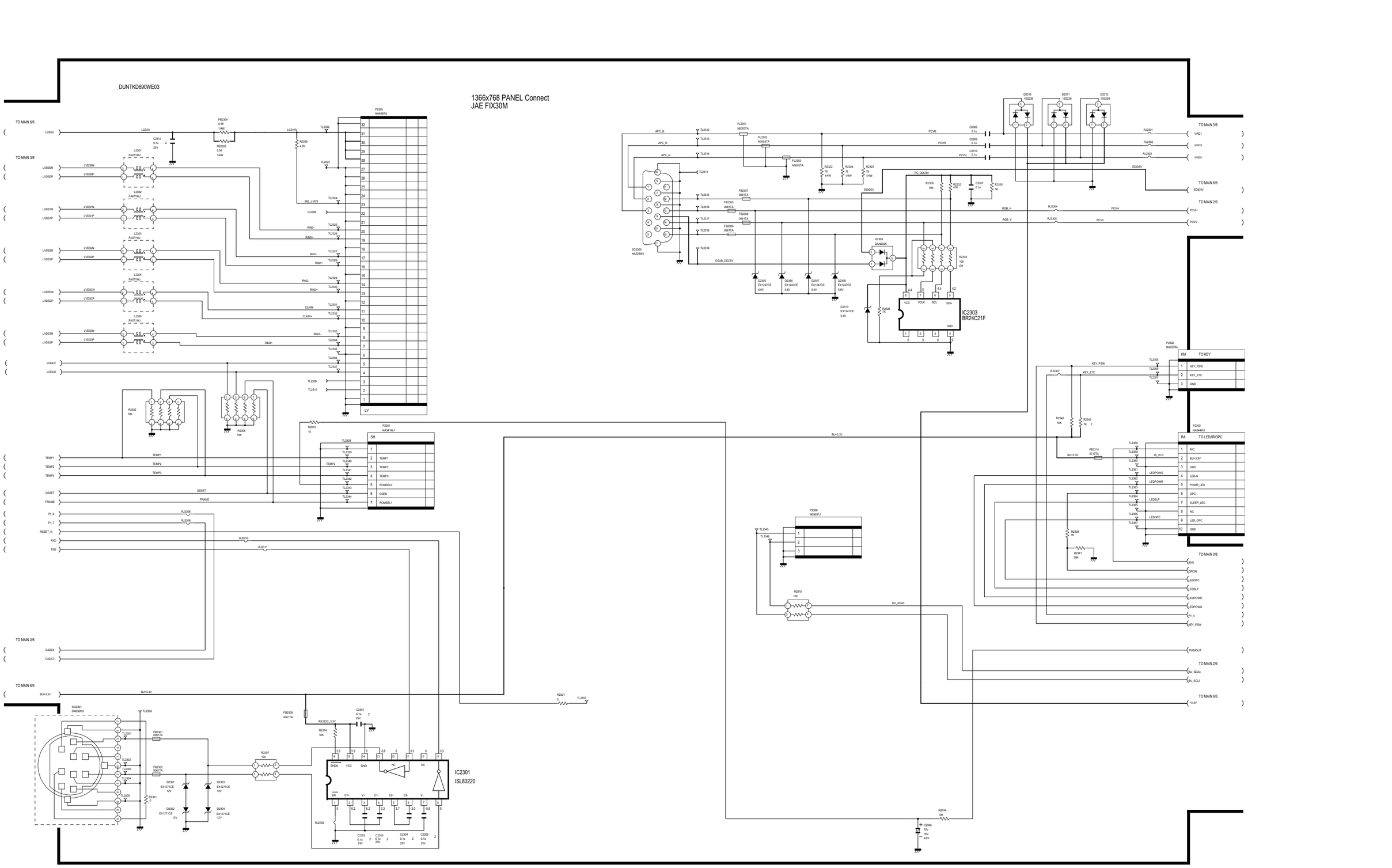
LC-37GA8E Main Unit Diagram (SIGNAL INOUT)



LC-37GA8E Main Unit Diagram (VCTP)



LC-37GA8E Main Unit Diagram (MISC)



LC-37GA8E Main Unit Diagram (POWER DC-DC)