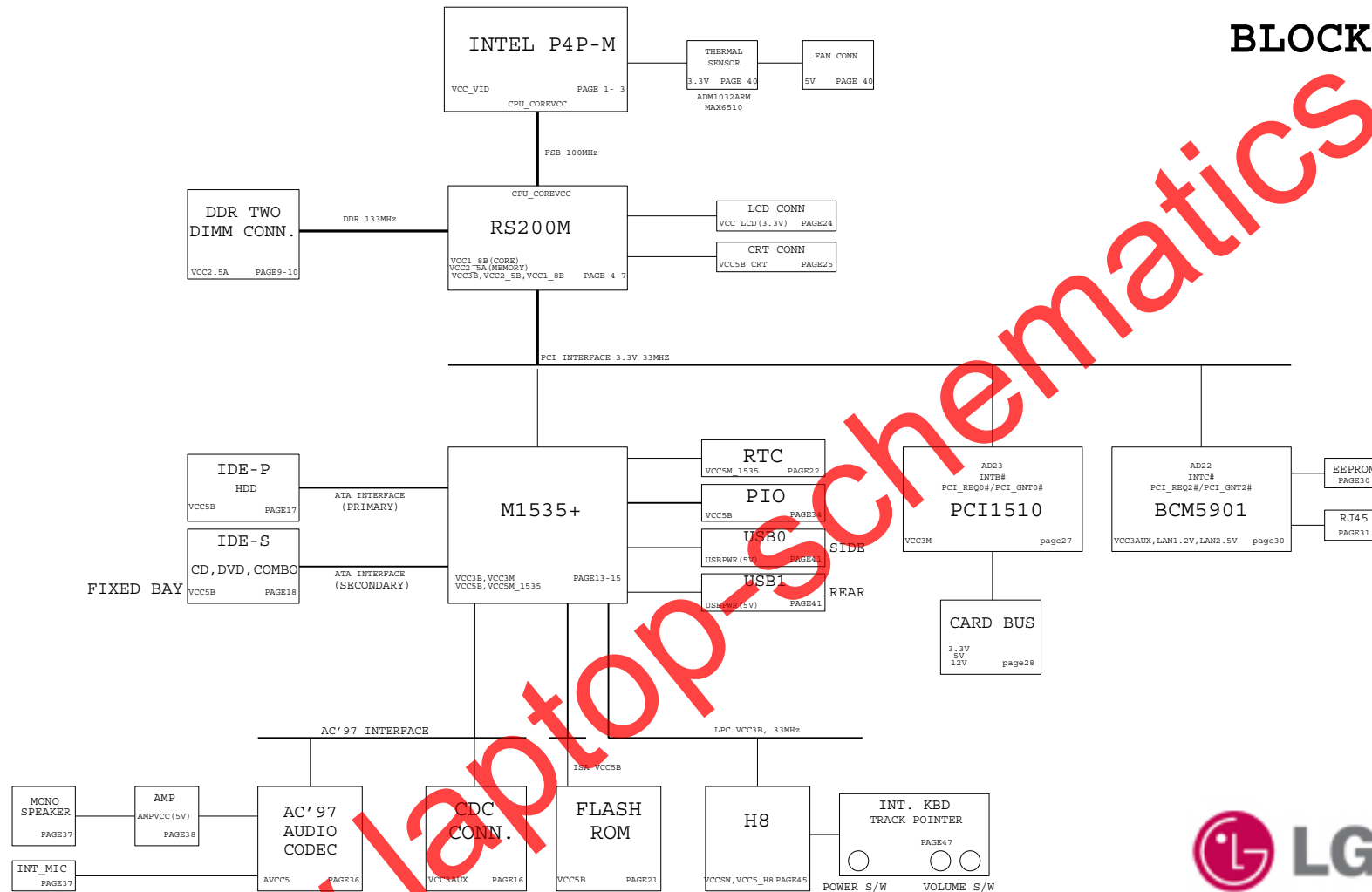
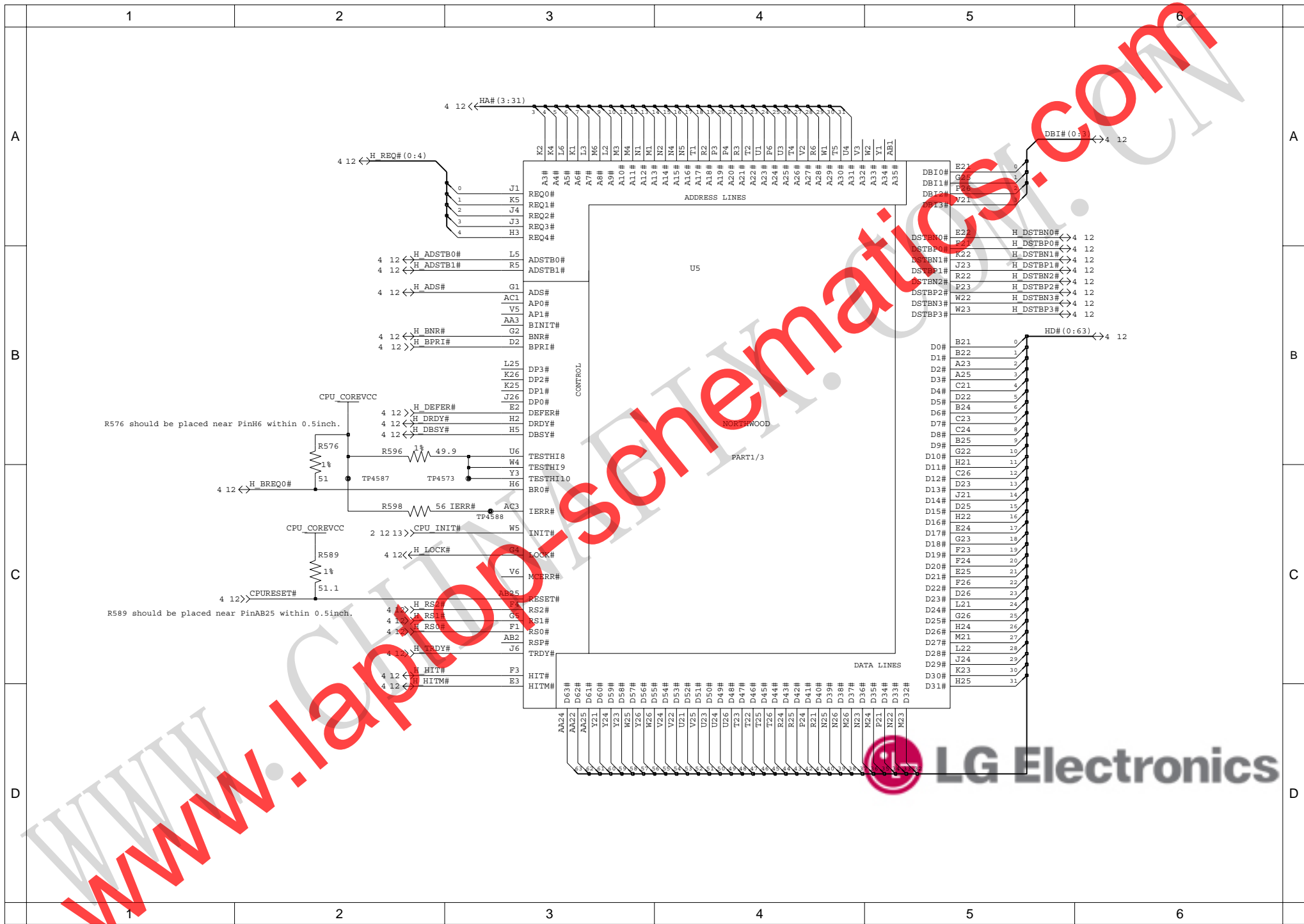
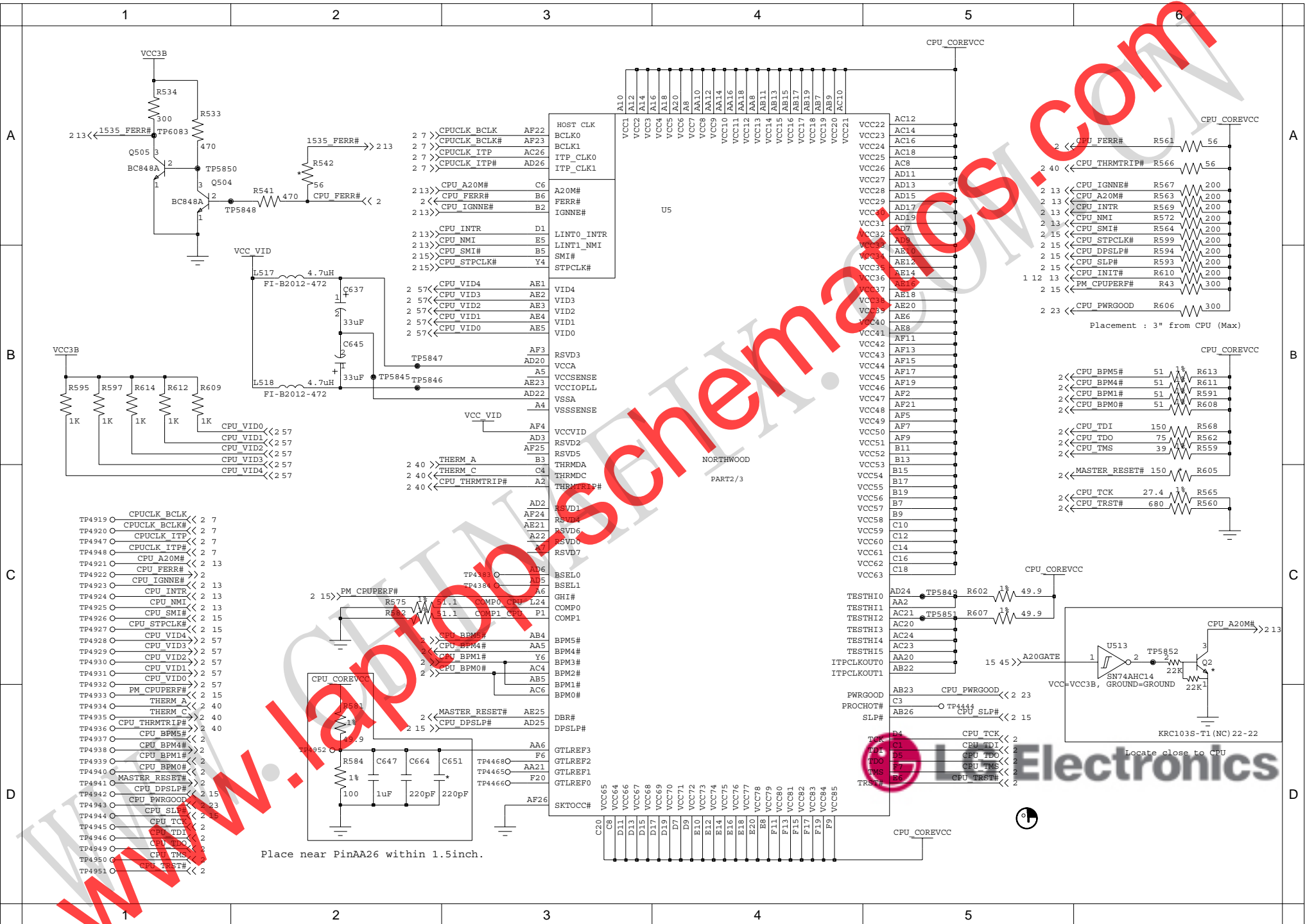


BLOCK DIAGRAM



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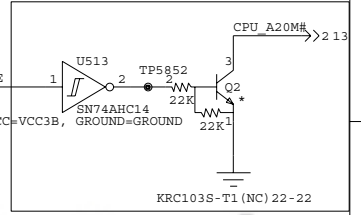
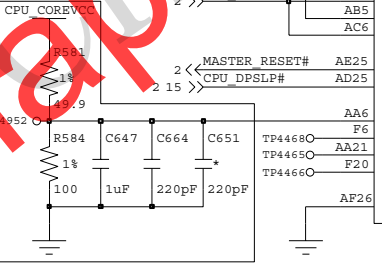


Place near PinAA26 within 1.5inch.

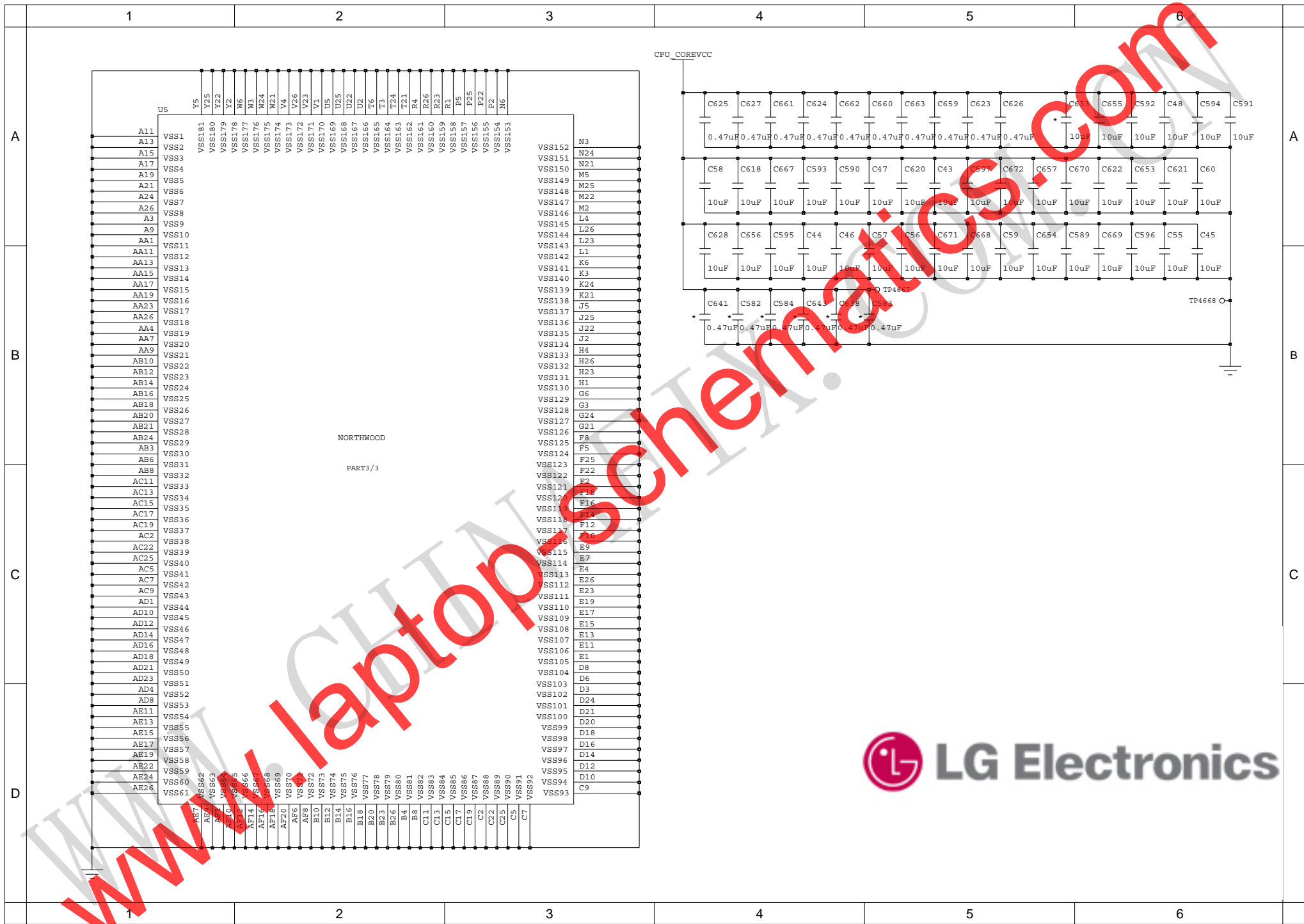
Locate close to CPU

Placement : 3" from CPU (Max)

- TP4919 CPUCLK_BCLK << 2 7
- TP4920 CPUCLK_BCLK# << 2 7
- TP4947 CPUCLK_ITP << 2 7
- TP4948 CPUCLK_ITP# << 2 7
- TP4921 CPU A20M# << 2 13
- TP4922 CPU FERR# << 2
- TP4923 CPU IGNNE# << 2 13
- TP4924 CPU INTR << 2 13
- TP4925 CPU NMI << 2 13
- TP4926 CPU SMI# << 2 15
- TP4927 CPU STPCLK# << 2 15
- TP4928 CPU VID4 << 2 57
- TP4928 CPU VID3 << 2 57
- TP4929 CPU VID2 << 2 57
- TP4930 CPU VID1 << 2 57
- TP4931 CPU VID0 << 2 57
- TP4932 PM CPUPERF# << 2 15
- TP4933 THERM A << 2 40
- TP4934 THERM C << 2 40
- TP4935 CPU THRMTRIP# << 2 40
- TP4936 CPU BPM5# << 2 40
- TP4937 CPU BPM4# << 2 40
- TP4938 CPU BPM3# << 2 40
- TP4939 CPU BPM2# << 2 40
- TP4940 MASTER RESET# << 2
- TP4941 CPU DPSLP# << 2
- TP4942 CPU PWRGOOD << 2 15
- TP4943 CPU SLP# << 2 15
- TP4944 CPU TCK << 2 40
- TP4945 CPU TDI << 2 40
- TP4946 CPU TDO << 2 40
- TP4949 CPU TMS << 2 40
- TP4950 CPU TRST# << 2 40
- TP4951 CPU TEST# << 2



- C20 VCC65
- D13 VCC66
- D14 VCC67
- D15 VCC68
- D16 VCC69
- D17 VCC70
- D18 VCC71
- D19 VCC72
- E10 VCC73
- E12 VCC74
- E14 VCC75
- E16 VCC76
- E18 VCC77
- E20 VCC78
- F11 VCC79
- F12 VCC80
- F13 VCC81
- F14 VCC82
- F15 VCC83
- F16 VCC84
- F17 VCC85
- F18 VCC86
- F19 VCC87
- F20 VCC88
- F21 VCC89
- F22 VCC90
- F23 VCC91
- F24 VCC92
- F25 VCC93
- F26 VCC94
- F27 VCC95
- F28 VCC96
- F29 VCC97
- F30 VCC98
- F31 VCC99
- F32 VCC100
- F33 VCC101
- F34 VCC102
- F35 VCC103
- F36 VCC104
- F37 VCC105
- F38 VCC106
- F39 VCC107
- F40 VCC108
- F41 VCC109
- F42 VCC110
- F43 VCC111
- F44 VCC112
- F45 VCC113
- F46 VCC114
- F47 VCC115
- F48 VCC116
- F49 VCC117
- F50 VCC118
- F51 VCC119
- F52 VCC120
- F53 VCC121
- F54 VCC122
- F55 VCC123
- F56 VCC124
- F57 VCC125
- F58 VCC126
- F59 VCC127
- F60 VCC128
- F61 VCC129
- F62 VCC130
- F63 VCC131
- F64 VCC132
- F65 VCC133
- F66 VCC134
- F67 VCC135
- F68 VCC136
- F69 VCC137
- F70 VCC138
- F71 VCC139
- F72 VCC140
- F73 VCC141
- F74 VCC142
- F75 VCC143
- F76 VCC144
- F77 VCC145
- F78 VCC146
- F79 VCC147
- F80 VCC148
- F81 VCC149
- F82 VCC150
- F83 VCC151
- F84 VCC152
- F85 VCC153
- F86 VCC154
- F87 VCC155
- F88 VCC156
- F89 VCC157
- F90 VCC158
- F91 VCC159
- F92 VCC160
- F93 VCC161
- F94 VCC162
- F95 VCC163
- F96 VCC164
- F97 VCC165
- F98 VCC166
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- F100 VCC168
- F101 VCC169
- F102 VCC170
- F103 VCC171
- F104 VCC172
- F105 VCC173
- F106 VCC174
- F107 VCC175
- F108 VCC176
- F109 VCC177
- F110 VCC178
- F111 VCC179
- F112 VCC180
- F113 VCC181
- F114 VCC182
- F115 VCC183
- F116 VCC184
- F117 VCC185
- F118 VCC186
- F119 VCC187
- F120 VCC188
- F121 VCC189
- F122 VCC190
- F123 VCC191
- F124 VCC192
- F125 VCC193
- F126 VCC194
- F127 VCC195
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- F130 VCC198
- F131 VCC199
- F132 VCC200
- F133 VCC201
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- F179 VCC247
- F180 VCC248
- F181 VCC249
- F182 VCC250
- F183 VCC251
- F184 VCC252
- F185 VCC253
- F186 VCC254
- F187 VCC255
- F188 VCC256
- F189 VCC257
- F190 VCC258
- F191 VCC259
- F192 VCC260
- F193 VCC261
- F194 VCC262
- F195 VCC263



A

B

C

D

A

B

C

HA# (3:31) U510 HD# (0:63)

3	M24	P4_A3#	J24	0	P4_D0#
4	P22	P4_A4#	H23	1	P4_D1#
5	M23	P4_A5#	H26	2	P4_D2#
6	N26	P4_A6#	H25	3	P4_D3#
7	N25	P4_A7#	J25	4	P4_D4#
8	M22	P4_A8#	J26	5	P4_D5#
9	P25	P4_A9#	G25	6	P4_D6#
10	P24	P4_A10#	H24	7	P4_D7#
11	P21	P4_A11#	F25	8	P4_D8#
12	R26	P4_A12#	G26	9	P4_D8#
13	P26	P4_A13#	G21	10	P4_D9#
14	R25	P4_A13#	F23	11	P4_D10#
15	N22	P4_A14#	F24	12	P4_D11#
16	N21	P4_A15#	H22	13	P4_D12#
17	T24	P4_A16#	F22	14	P4_D13#
18	T26	P4_A17#	F26	15	P4_D14#
19	R24	P4_A18#	F21	16	P4_D15#
20	R22	P4_A19#	E25	17	P4_D16#
21	R23	P4_A20#	B25	18	P4_D17#
22	T25	P4_A21#	E23	19	P4_D18#
23	U26	P4_A22#	L24	20	P4_D19#
24	T21	P4_A23#	L24	20	P4_D20#
25	U25	P4_A24#	E26	21	P4_D21#
26	U22	P4_A25#	D22	22	P4_D22#
27	U24	P4_A26#	E24	23	P4_D23#
28	T22	P4_A27#	D22	24	P4_D24#
29	V25	P4_A28#	B26	25	P4_D25#
30	U21	P4_A29#	B24	26	P4_D26#
31	V21	P4_A30#	C23	27	P4_D27#
		P4_A31#	A24	28	P4_D28#
			A25	29	P4_D29#
			D23	30	P4_D30#
			A26	31	P4_D31#
			E21	32	P4_D32#
			E20	33	P4_D33#
			F18	34	P4_D34#
			F20	35	P4_D35#
			D20	36	P4_D36#
			D21	37	P4_D37#
			A23	38	P4_D38#
			F19	39	P4_D39#
			E18	40	P4_D40#
			A22	41	P4_D41#
			C22	42	P4_D42#
			C21	43	P4_D43#
			B21	44	P4_D44#
			A21	45	P4_D45#
			D18	46	P4_D46#
			F17	47	P4_D47#
			C19	48	P4_D48#
			A20	49	P4_D49#
			B20	50	P4_D50#
			B19	51	P4_D51#
			E17	52	P4_D52#
			F15	53	P4_D53#
			A19	54	P4_D54#
			B18	55	P4_D55#
			B17	56	P4_D56#
			C18	57	P4_D57#
			A18	58	P4_D58#
			C17	59	P4_D59#
			E15	60	P4_D60#
			C16	61	P4_D61#
			F14	62	P4_D62#
			B16	63	P4_D63#

1 12	H ADSTB0#	P23	P4_ADSTB0#	CPU
1 12	H ADSTB1#	U23	P4_ADSTB1#	CPU
1 12	H DSTBN0#	G22	P4_DSTBN0#	CPU
1 12	H DSTBN1#	C25	P4_DSTBN1#	CPU
1 12	H DSTBN2#	E19	P4_DSTBN2#	CPU
1 12	H DSTBN3#	D16	P4_DSTBN3#	CPU
1 12	H DSTBP0#	G23	P4_DSTBP0#	CPU
1 12	H DSTBP1#	C24	P4_DSTBP1#	CPU
1 12	H DSTBP2#	D19	P4_DSTBP2#	CPU
1 12	H DSTBP3#	E16	P4_DSTBP3#	CPU

1 12	H RS0#	M21	P4_RS0#	CPU
1 12	H RS1#	K21	P4_RS1#	CPU
1 12	H RS2#	K22	P4_RS2#	CPU
4 23 45	NB EWRGD	D6	POWERGOOD	CPU
1 12	CPURSET#	E14	P4_CPURST#	CPU

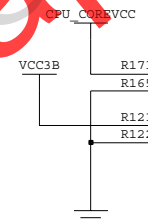
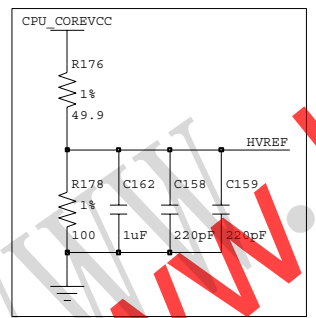
1 12	H ADS#	K24	P4_ADS#	CPU
1 12	H BPRI#	L21	P4_BPRI#	CPU
1 12	H BREQ0#	J22	P4_BR0#	CPU
1 12	H BNR#	K25	P4_BNR#	CPU
1 12	H LOCK#	L24	P4_LOCK#	CPU
1 12	H DEFER#	L23	P4_DEFER#	CPU
1 12	H HIT#	K26	P4_HIT#	CPU
1 12	H HITM#	L22	P4_HITM#	CPU
1 12	H DBSY#	J23	P4_DBSY#	CPU
1 12	H DRDY#	L25	P4_DRDY#	CPU
1 12	H TRDY#	J21	P4_TRDY#	CPU

	HVREF	TP4673	V24	P4_VREF
		TP4672	V23	COMPVDD
		TP4671	V22	COMPVSS
		TP4670	C15	COMPCLKVDD
		TP4669	D15	COMPCLKVSS

M25	P4_REQ0#
N23	P4_REQ1#
R21	P4_REQ2#
M26	P4_REQ3#
L26	P4_REQ4#
H21	P4_DBT0#
C26	P4_DBT1#
B22	P4_DBT2#
F16	P4_DBT3#

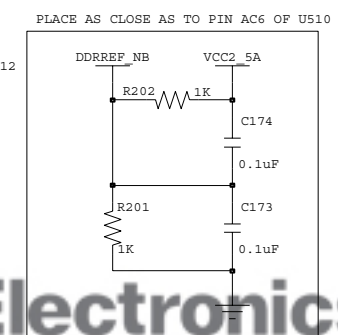
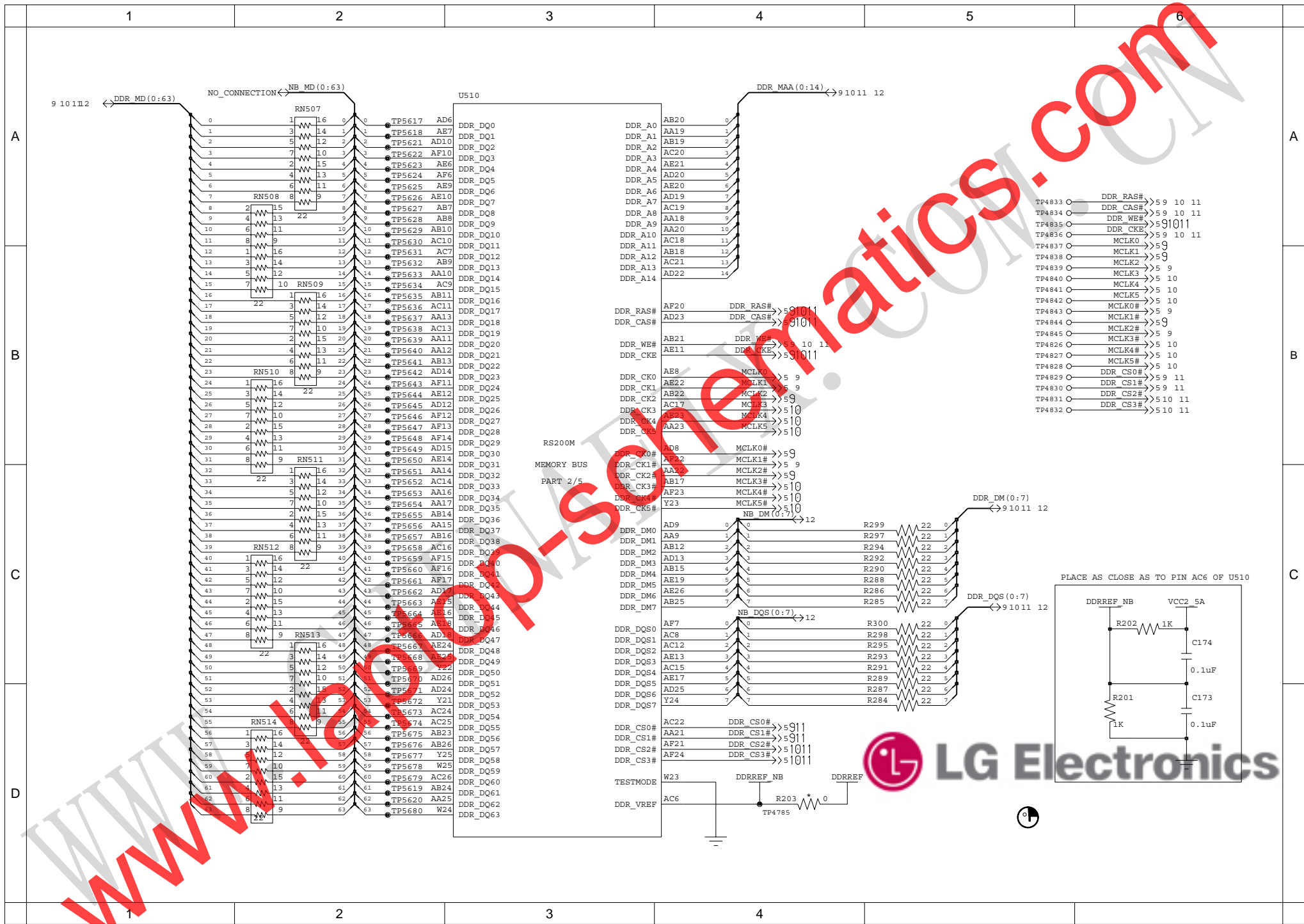
SUSSTAT#	AA8	SUSTAT#
PCIRST# PCI	AB6	PCIRST# PCI
SYSRST#		

TP4825	NB_PWRGD	<<4	23 45
TP4823	SUSTAT#	<<4	15 45
TP4822	PCIRST# PCI	<<4	13 27 29 30

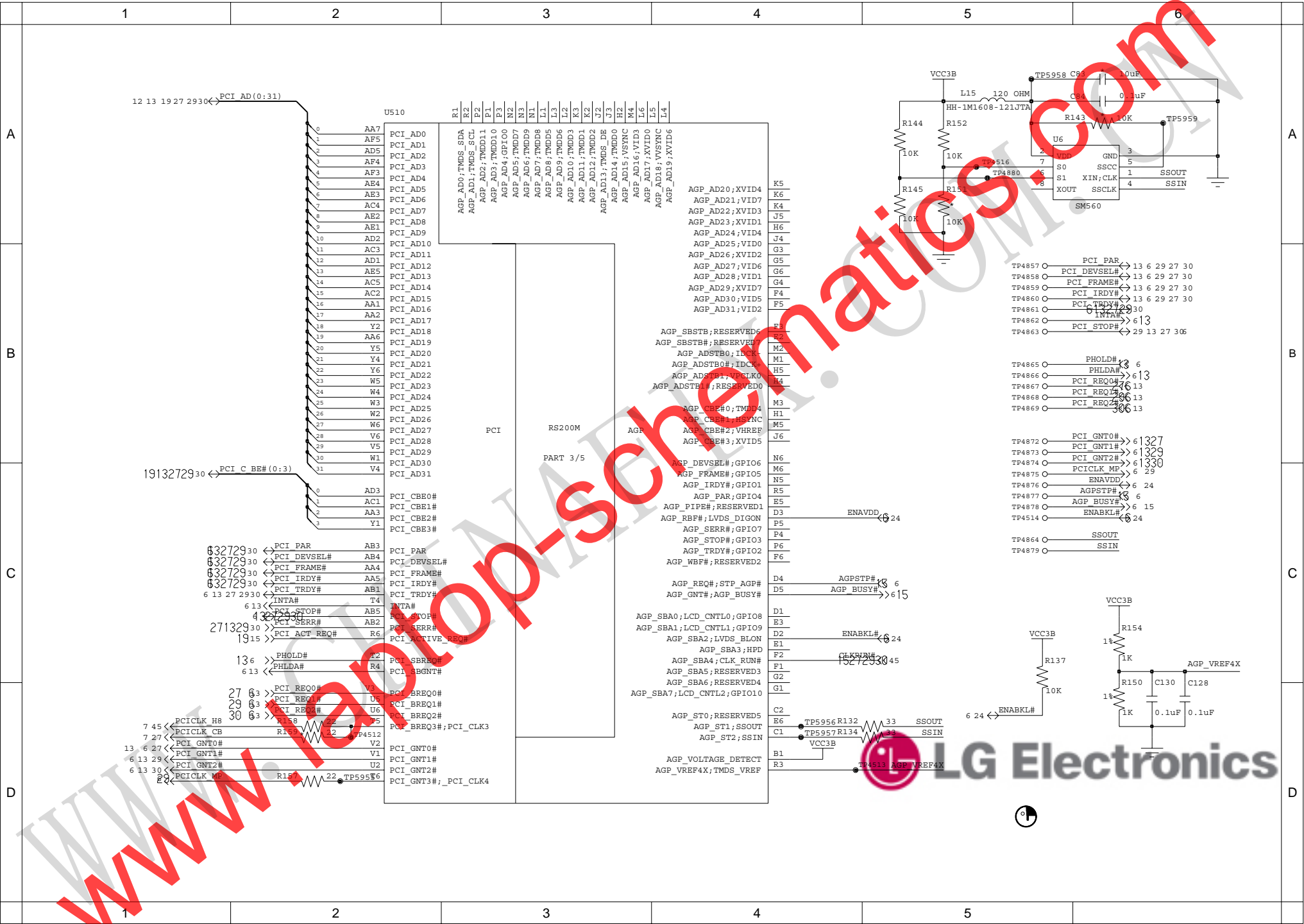


1 12 H REQ# (0:4) DBI# (0:3)



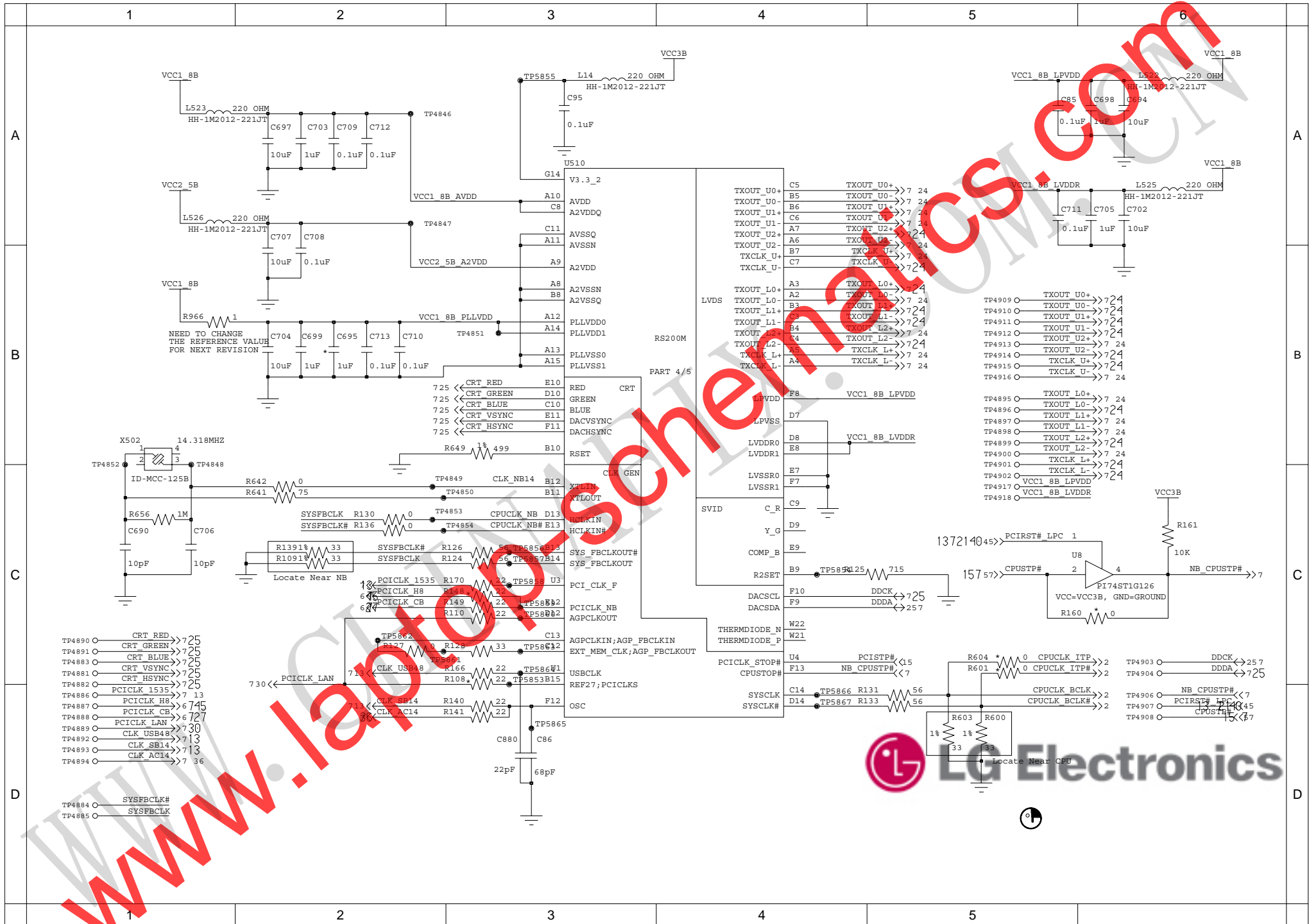


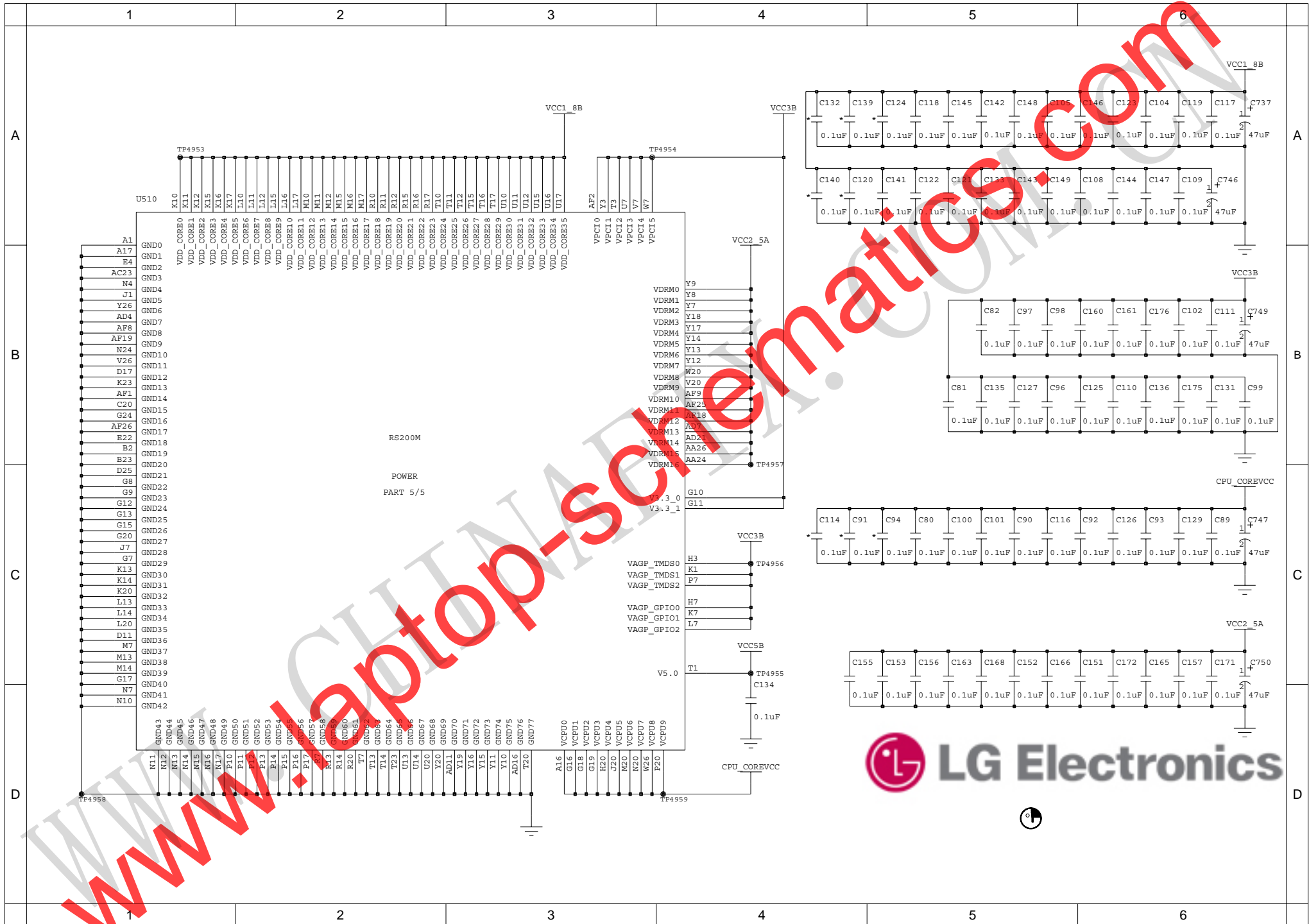
www.lg-electronics.com

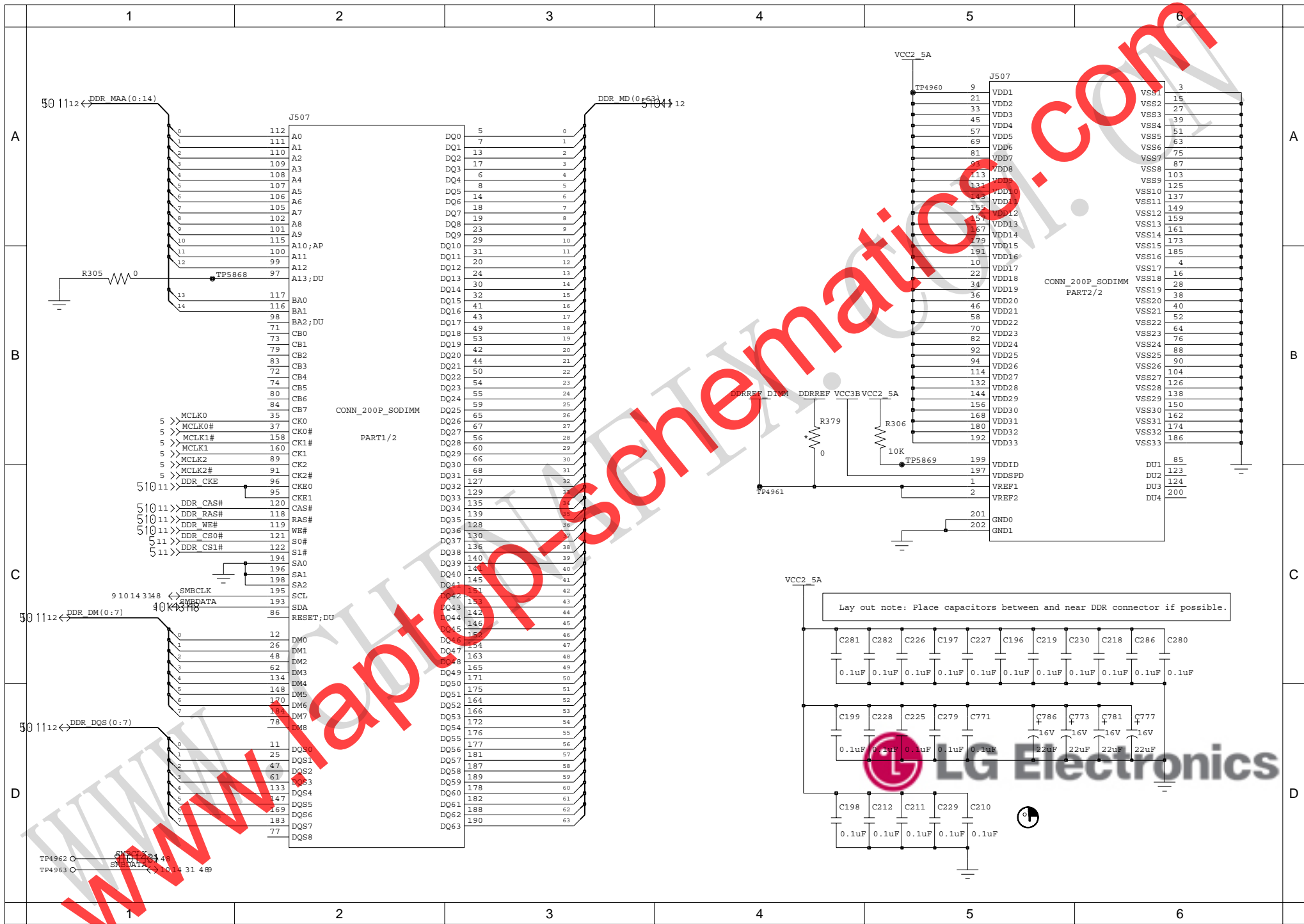


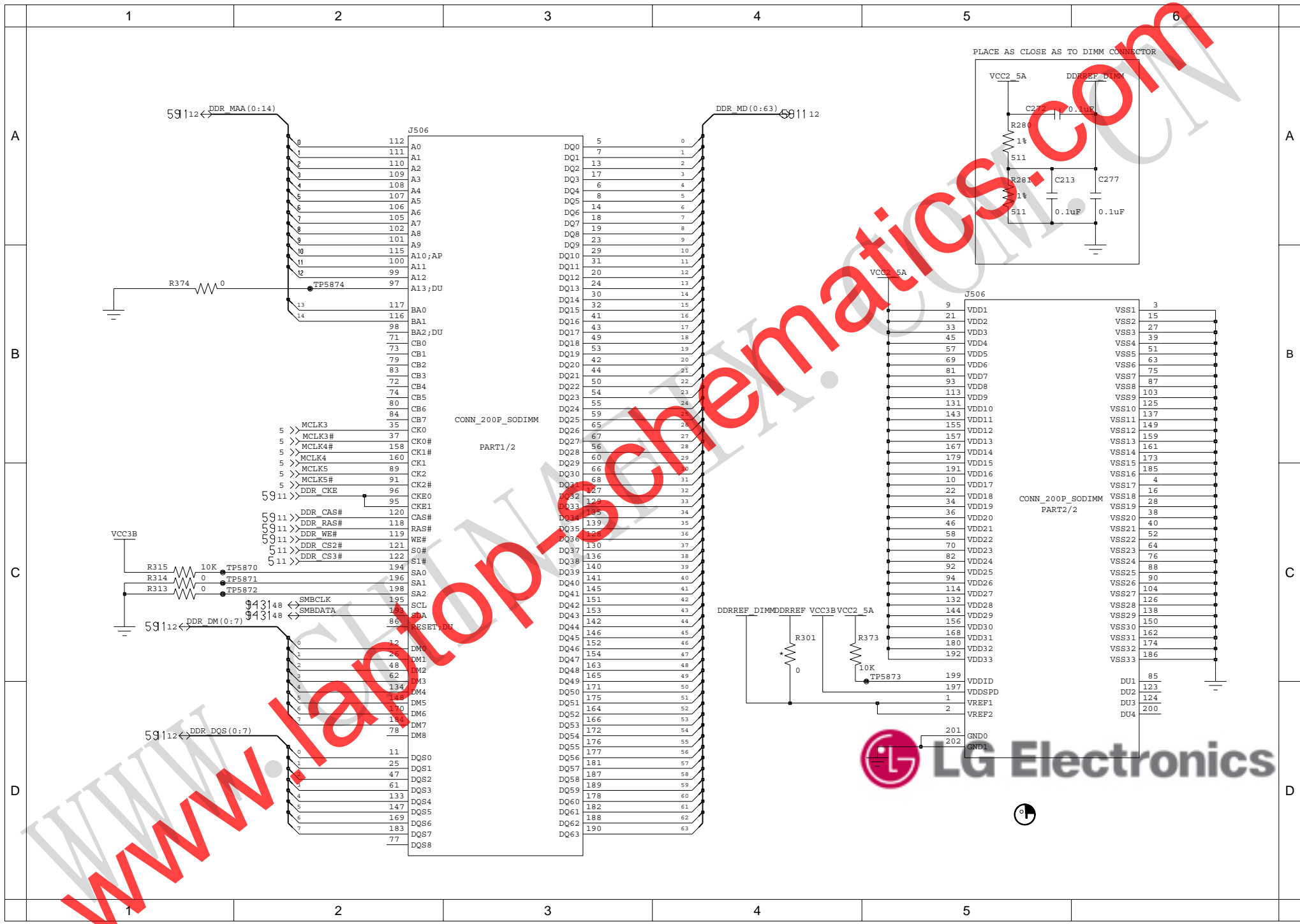
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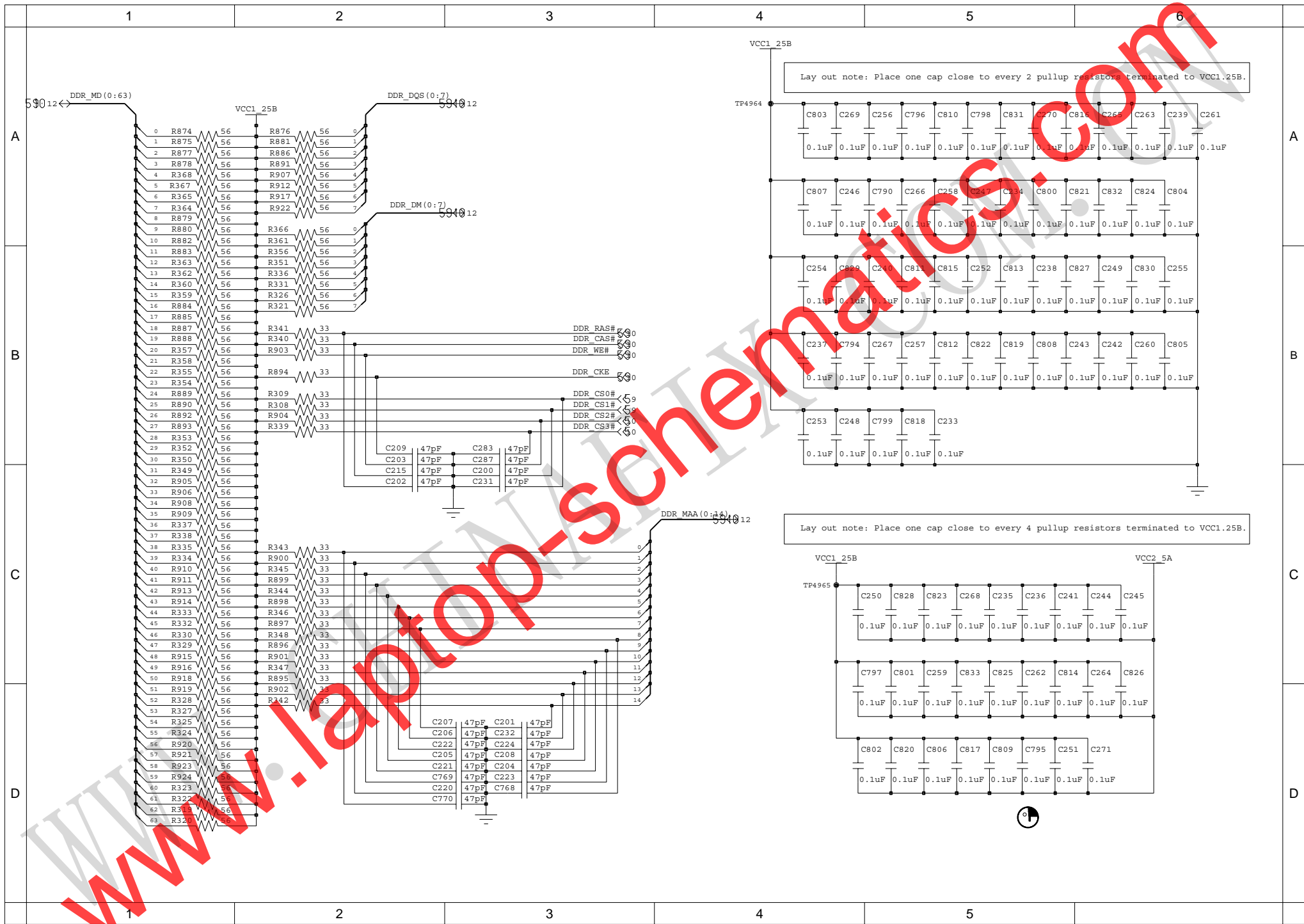


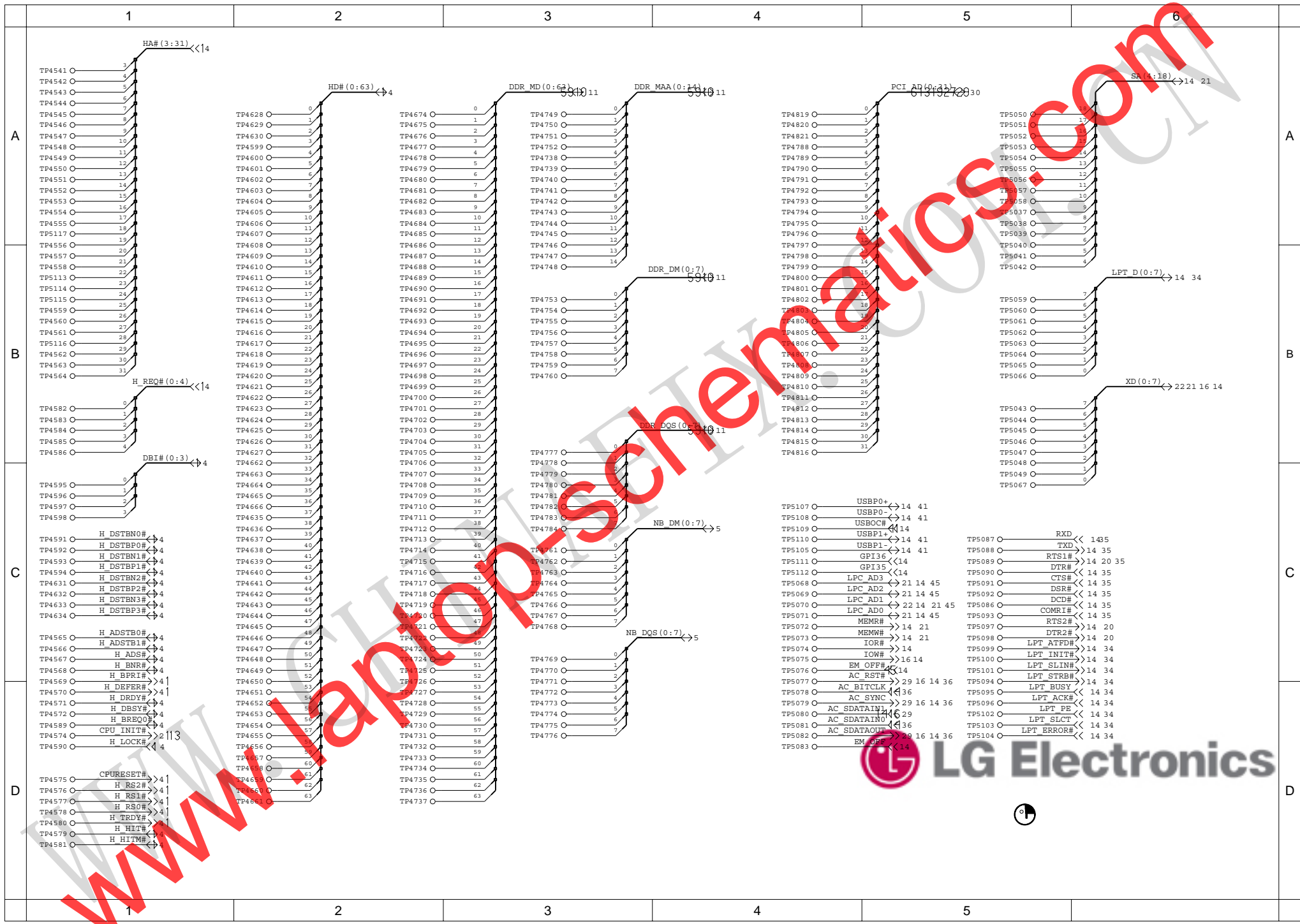




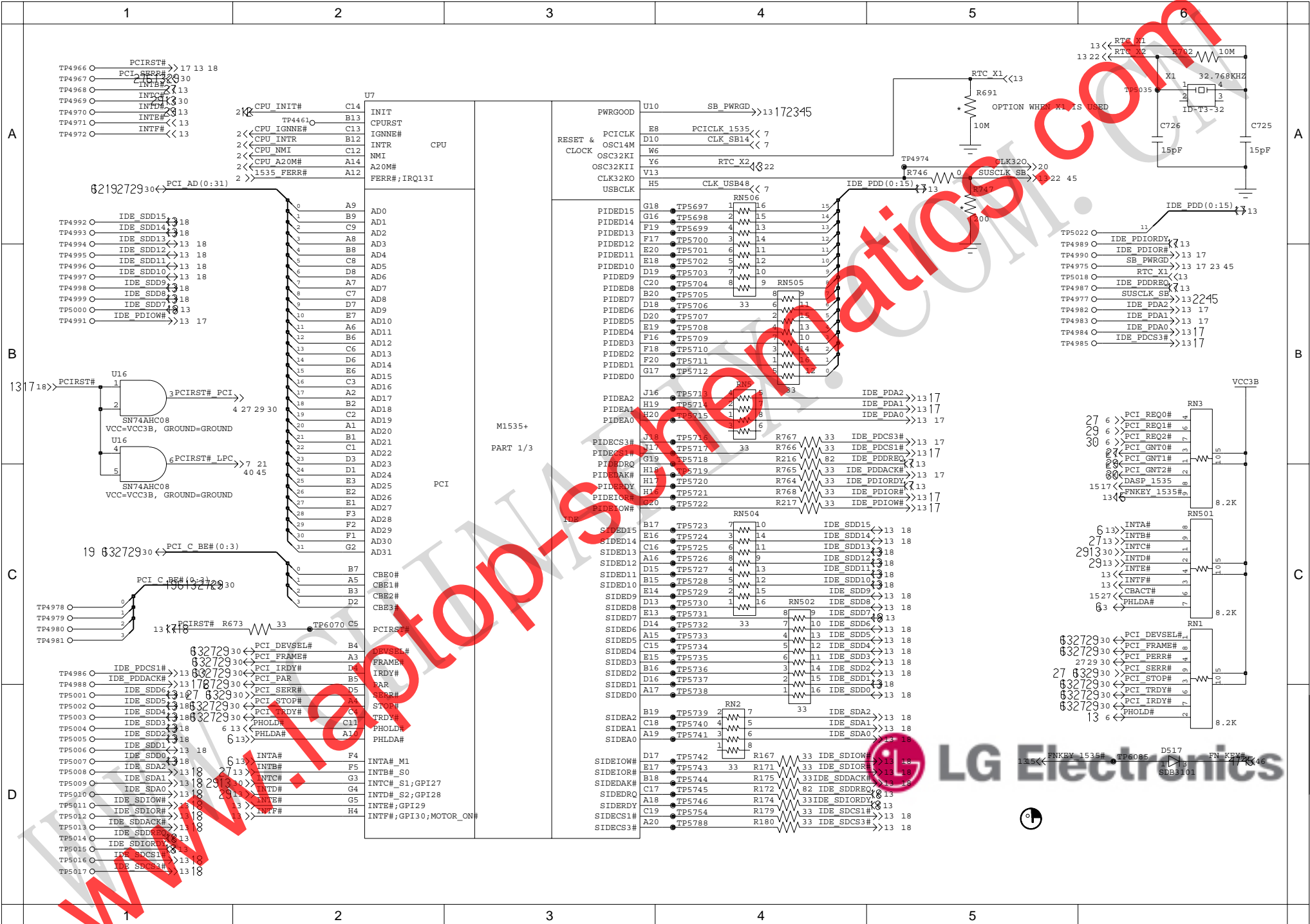


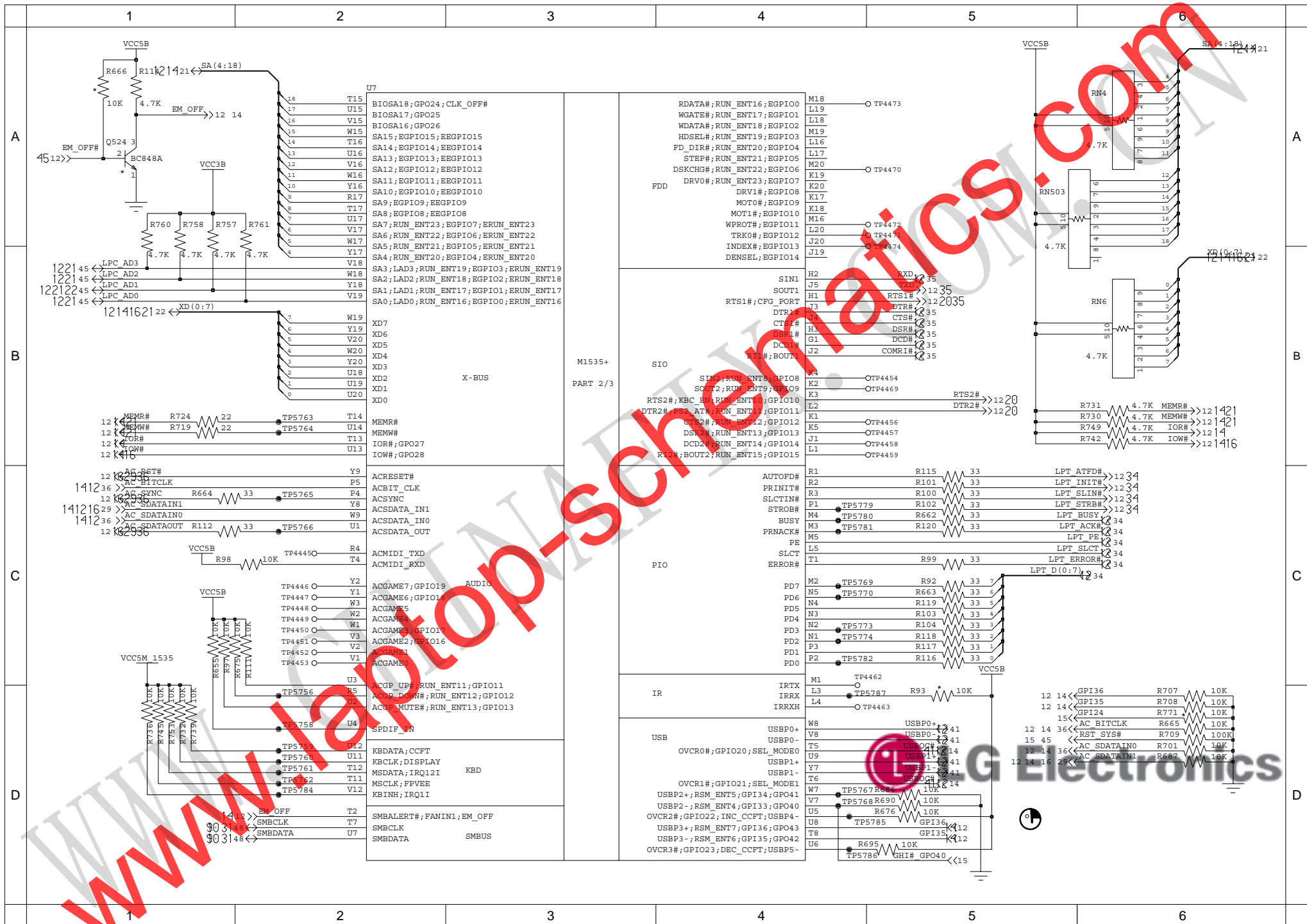
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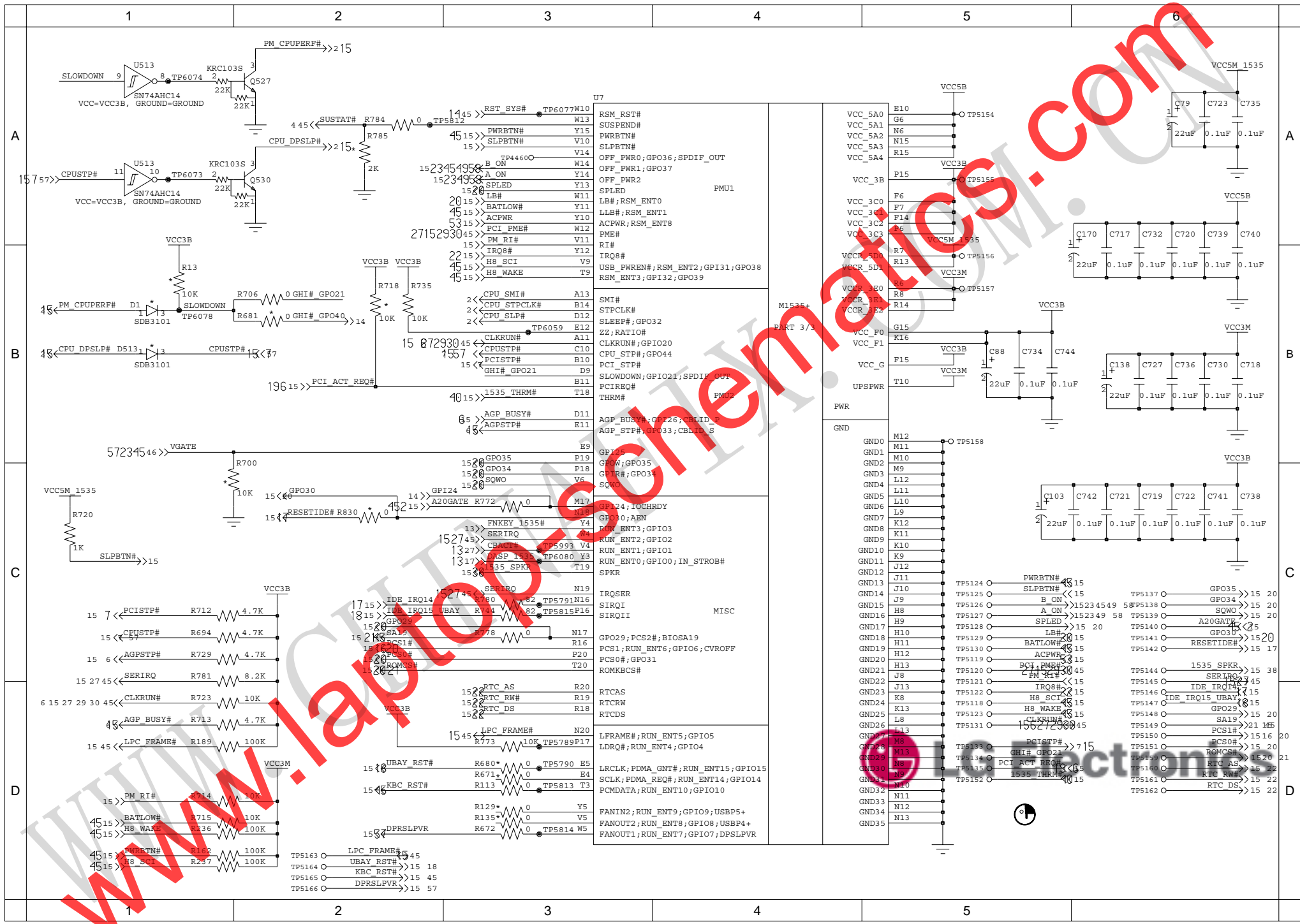




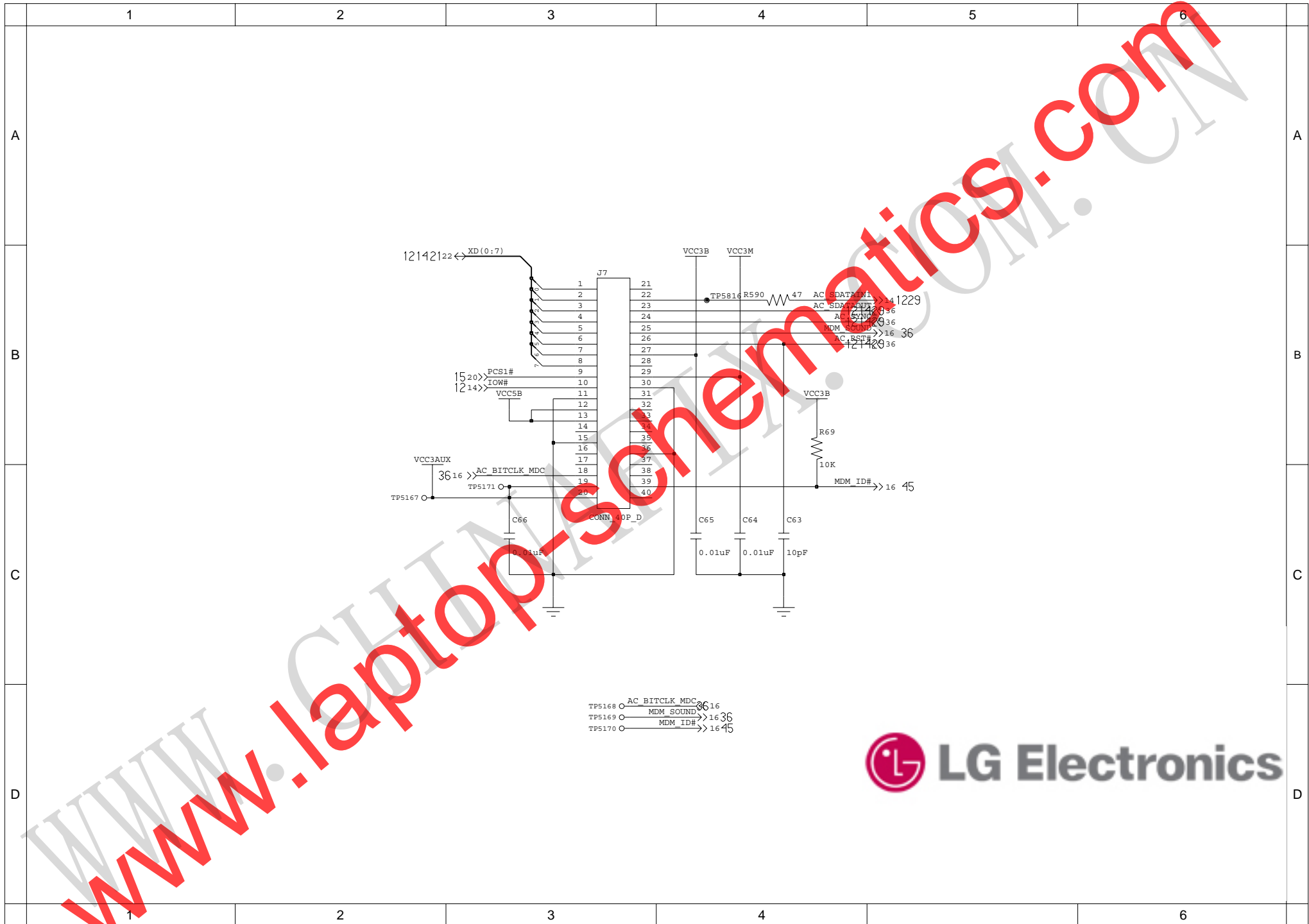
www.Top-Scholar.com

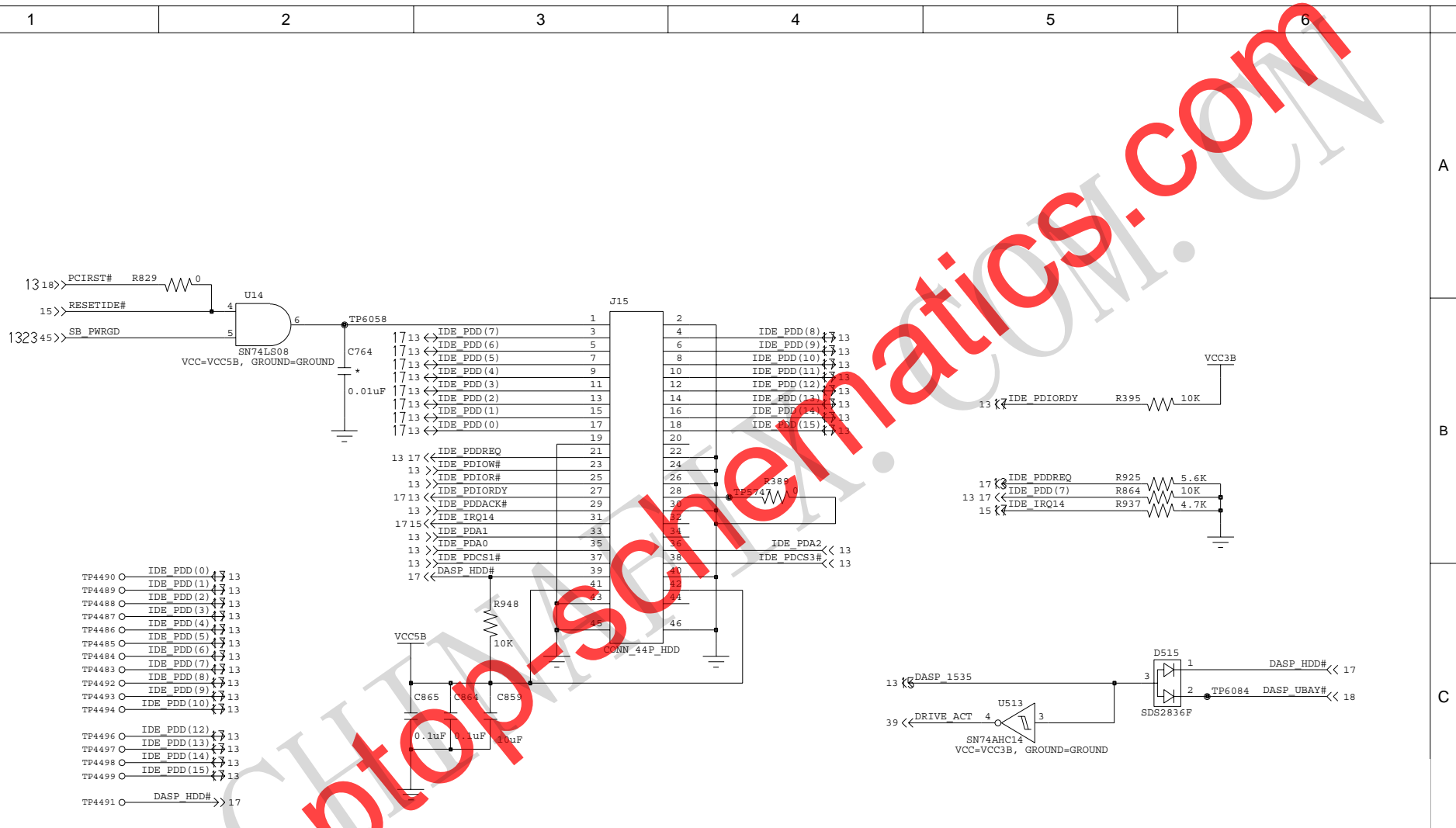


G Electronics

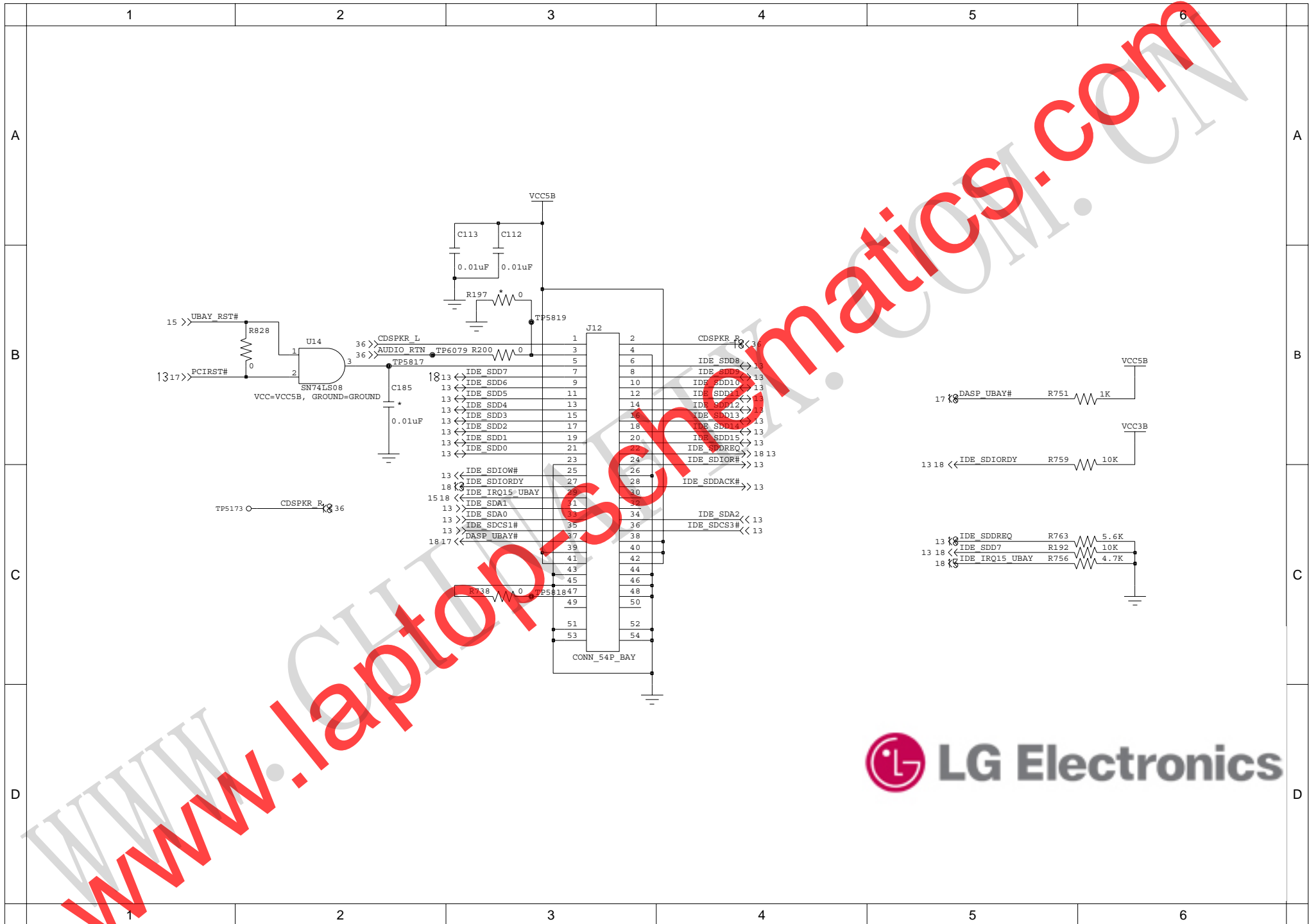


www.laptronics.com



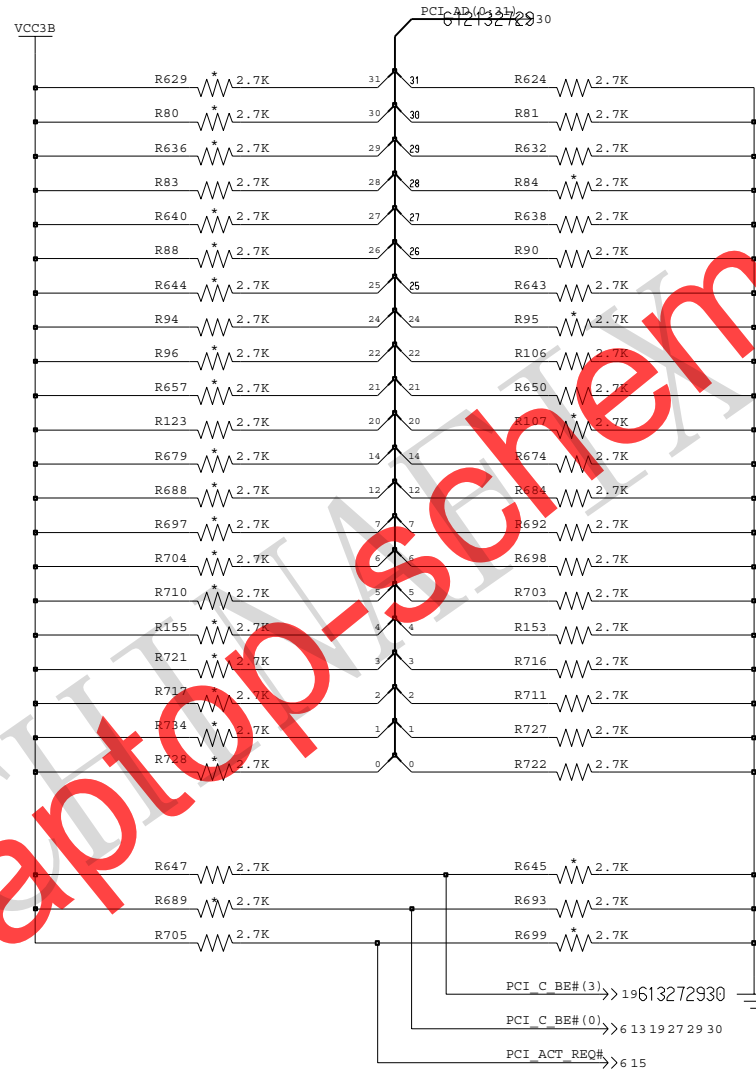


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RS200M Strapping Options

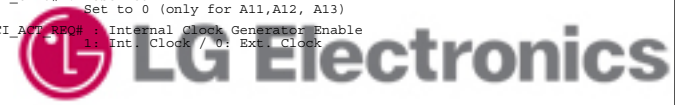


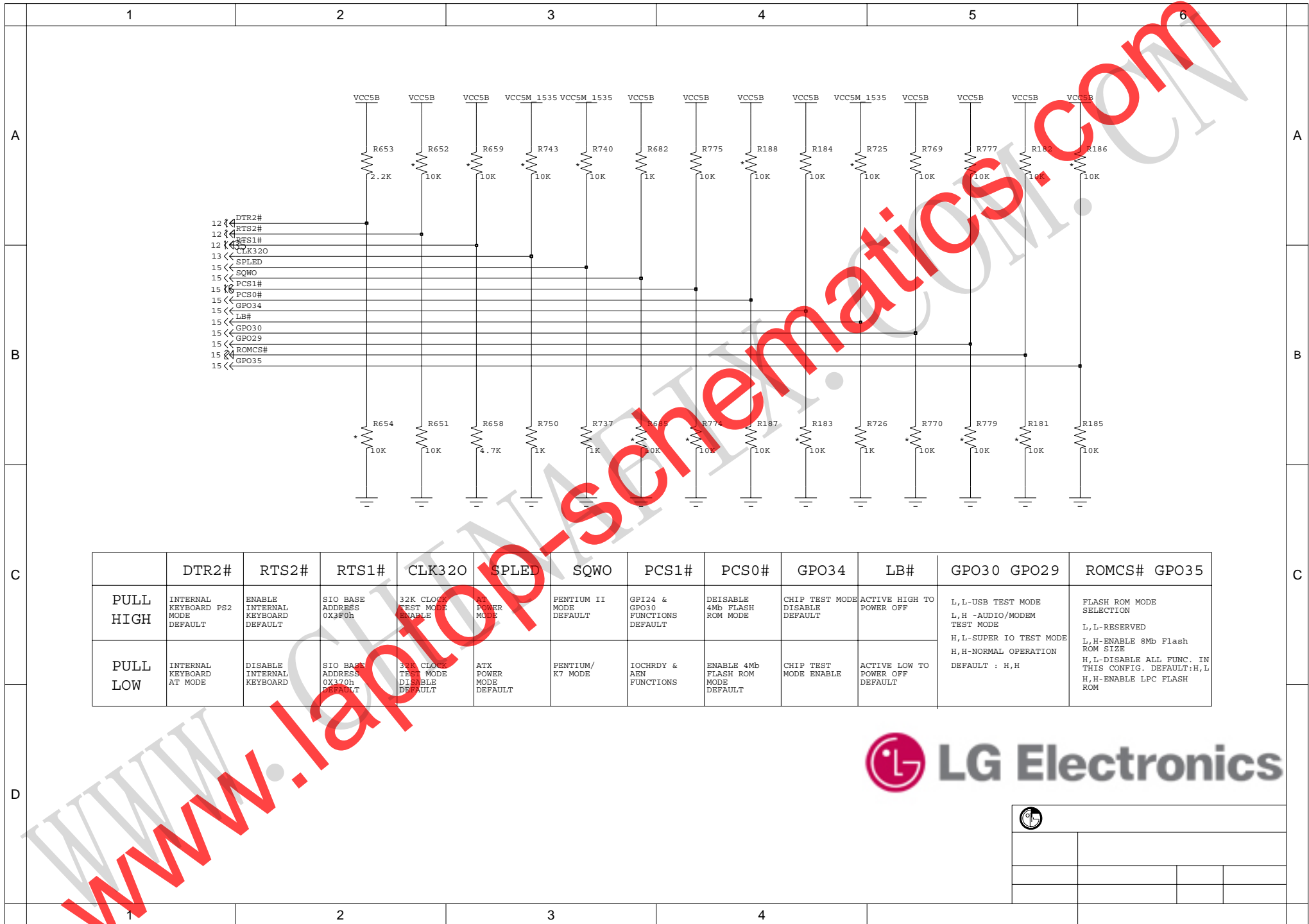
AD(31:30) FSB Speed	
00	100 MHz
01	133 MHz
10	166 MHz
11	86 MHz

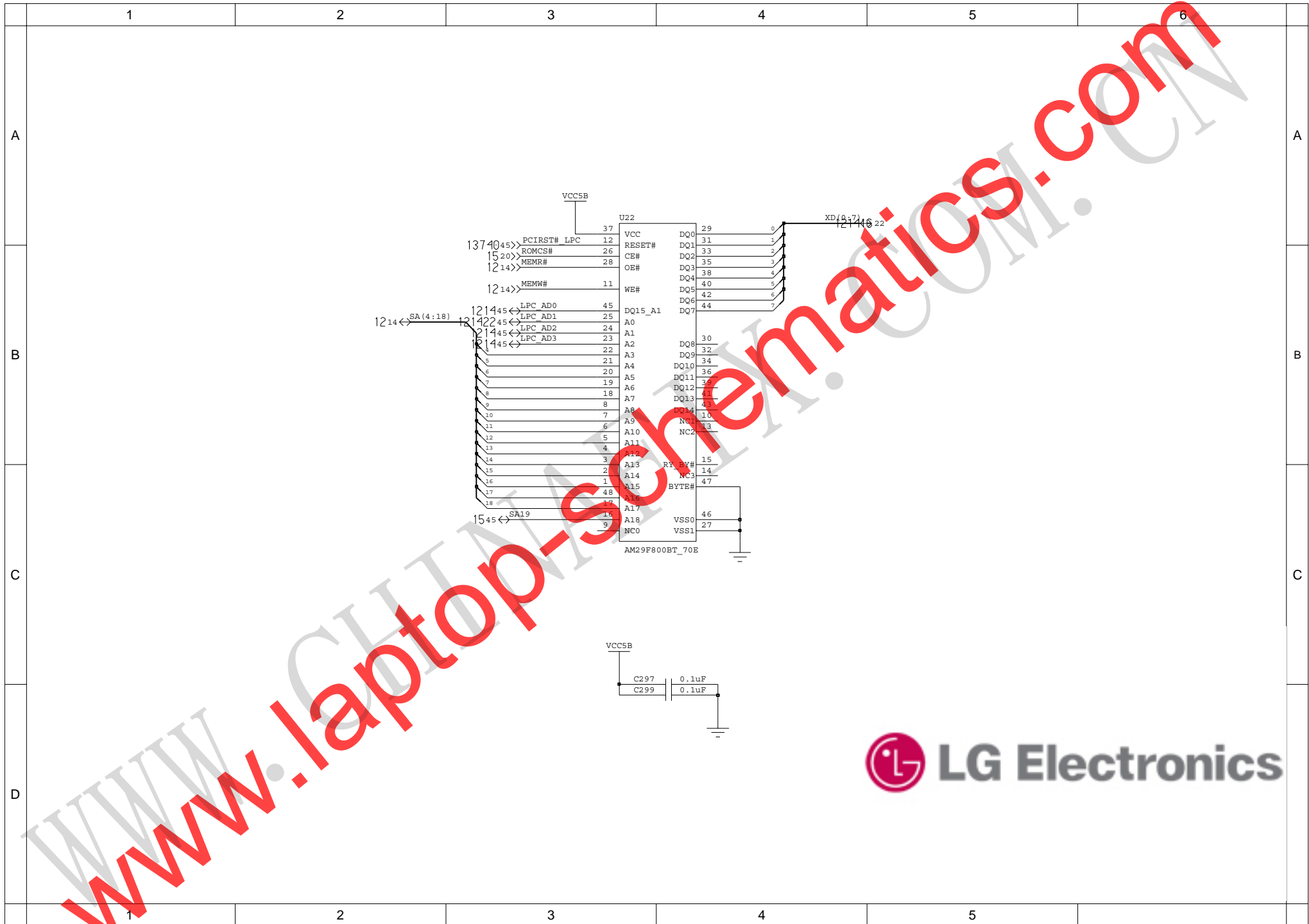
- AD(31:30) FSB Clock Speed
- AD29 : Strap Configuration
1: Reduced Set / 0: Full Set
- AD28 : Enable Spread Spectrum
1: Enable SS / 0: Disable SS
- AD27 : Disable MCERR# Observations
1: Disable / 0: Enable
- AD26 : Disable Bus Parking
1: Disable / 0: Enable
- AD25 : Disable BINIT# Observations
1: Disable / 0: Enable
- AD24 : Enable IOQ Pipelining
1: IOQ=12 / 0: IOQ=1
- AD22 : REF27 Function
1: 27MHz REF Input / 0: PCICLK5 Output
- AD21 : Clock Bypass
1: Test Mode / 0: Normal Mode
- AD20 : PCI Clock Expansion (REQ3# & GNT3#)
1: PCICLK3 & PCICLK4 / 0: REQ & GNT Pair
- AD14 : P4 Voltage Detection
1: 1.7V DT CPU / 0: 1.2V NT CPU
- AD12 : Flat Panel ID4
FP_ID4
- AD11 : Flat Panel ID3
FP_ID3
- AD10 : Flat Panel ID2
FP_ID2
- AD5 : Flat Panel ID1
FP_ID1
- AD4 : Flat Panel ID0
FP_ID0
- AD3 : A-Link Enable
1: A-Link / 0: PCI-33
- AD2 : Auto Calibration Enable
1: Disable / 0: Enable
- AD1 : CPU Reset Forced to Be Shortened
1: Test Mode / 0: Normal Mode
- AD0 : Default CFG for GC Enable bit & AGPCLKOUT
1: '0' & 66MHz AGP / 0: '0' & 33MHz PCI

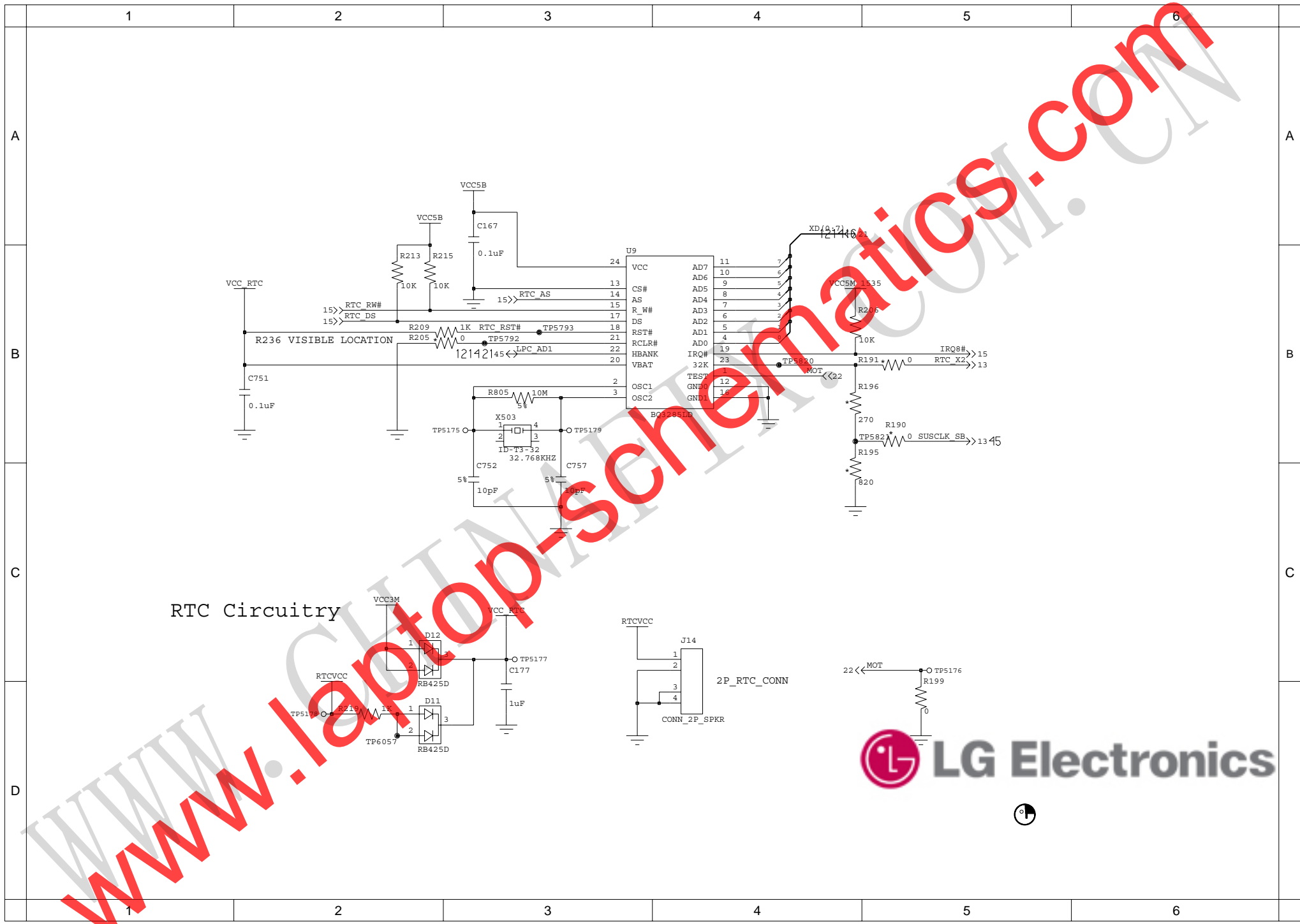
- PCI_CBE3# : Production Test
1: Normal / 0: Production Test
- PCI_CBE0# : Reserved
Set to 0 (only for A11,A12, A13)
- PCI_ACT_REQ# : Internal Clock Generator Enable
1: Int. Clock / 0: Ext. Clock

FP_ID(0:4)

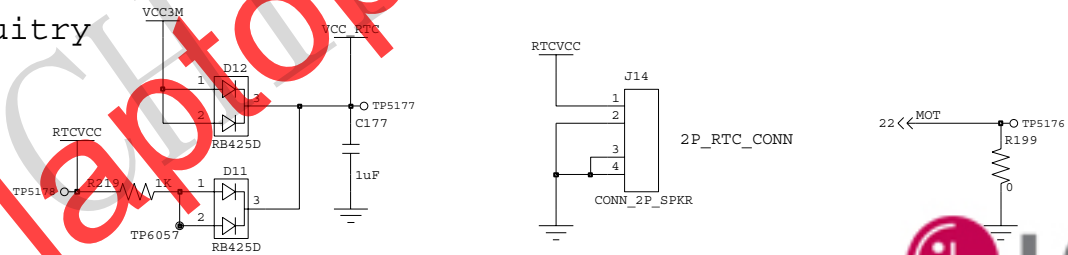


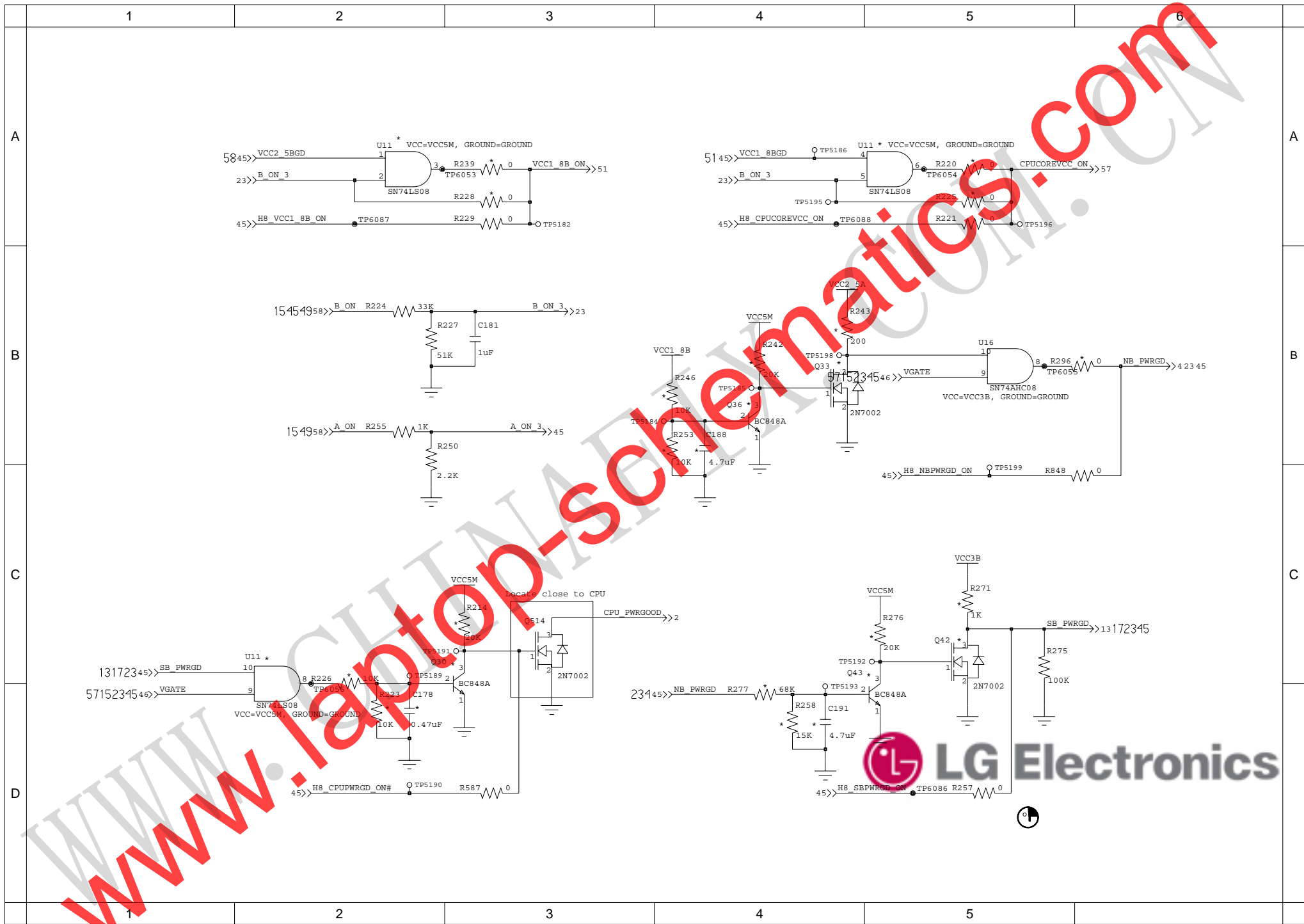




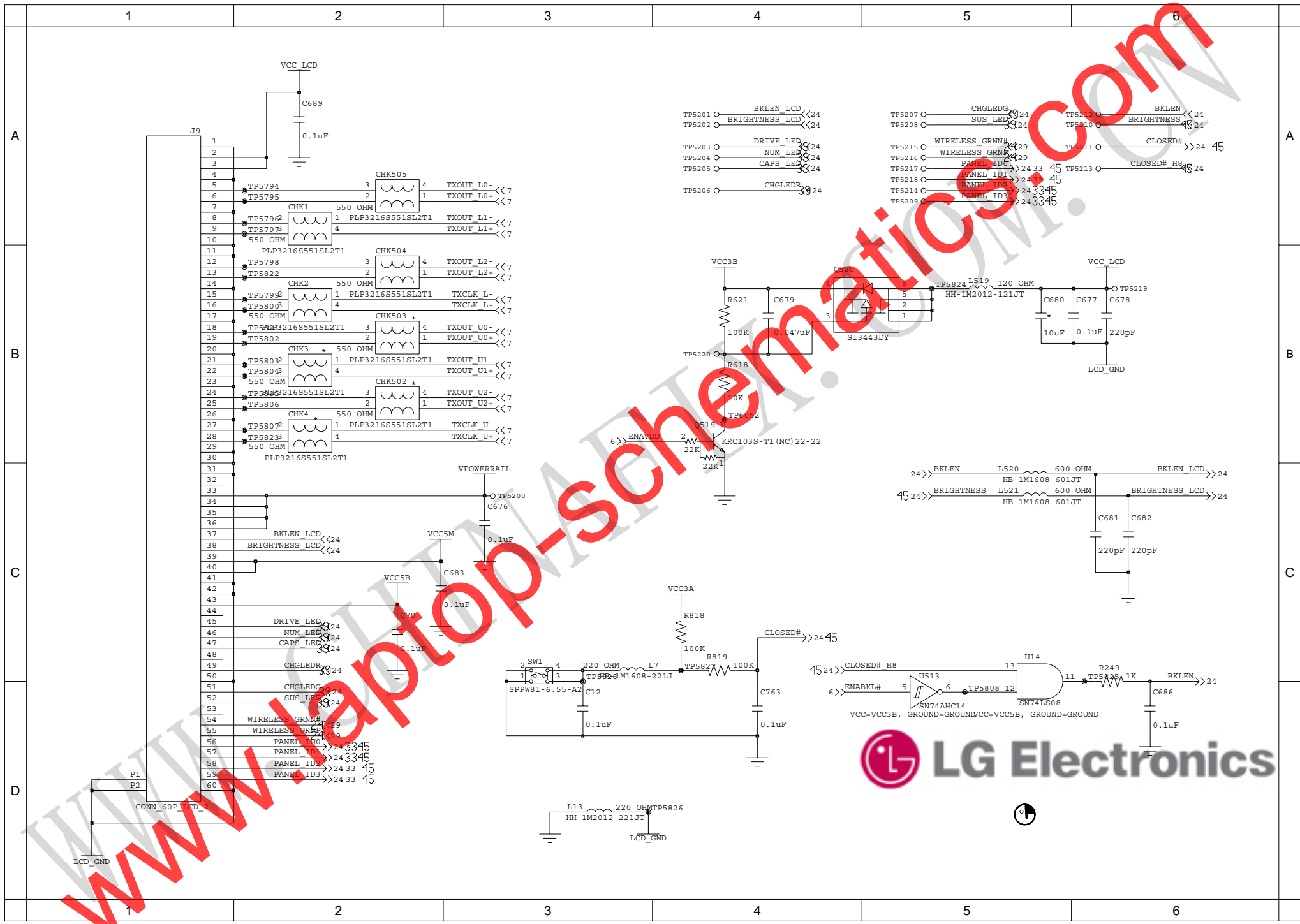


RTC Circuitry

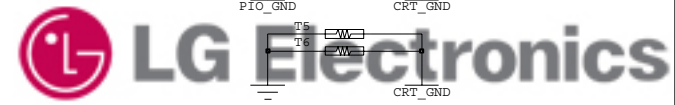
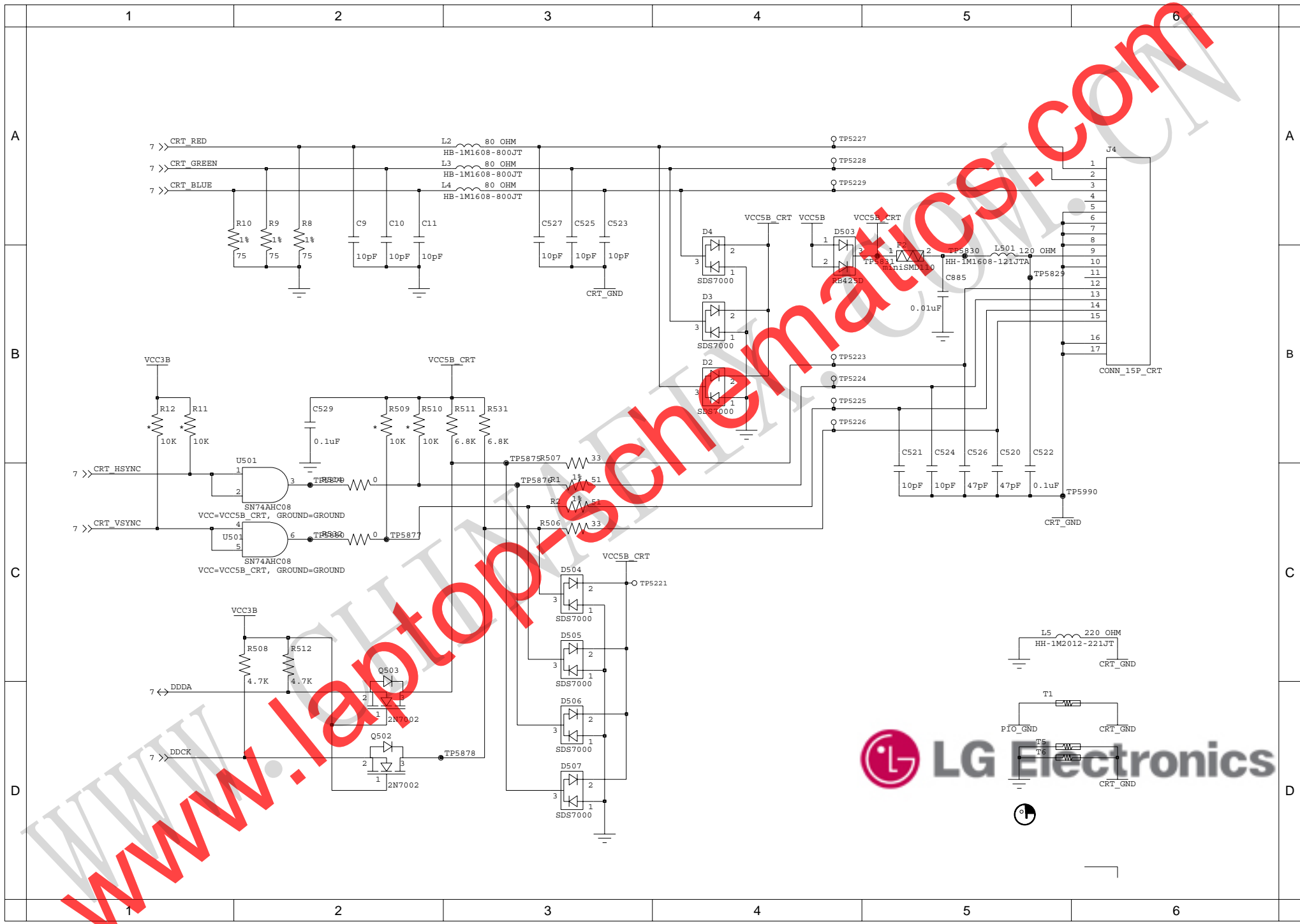


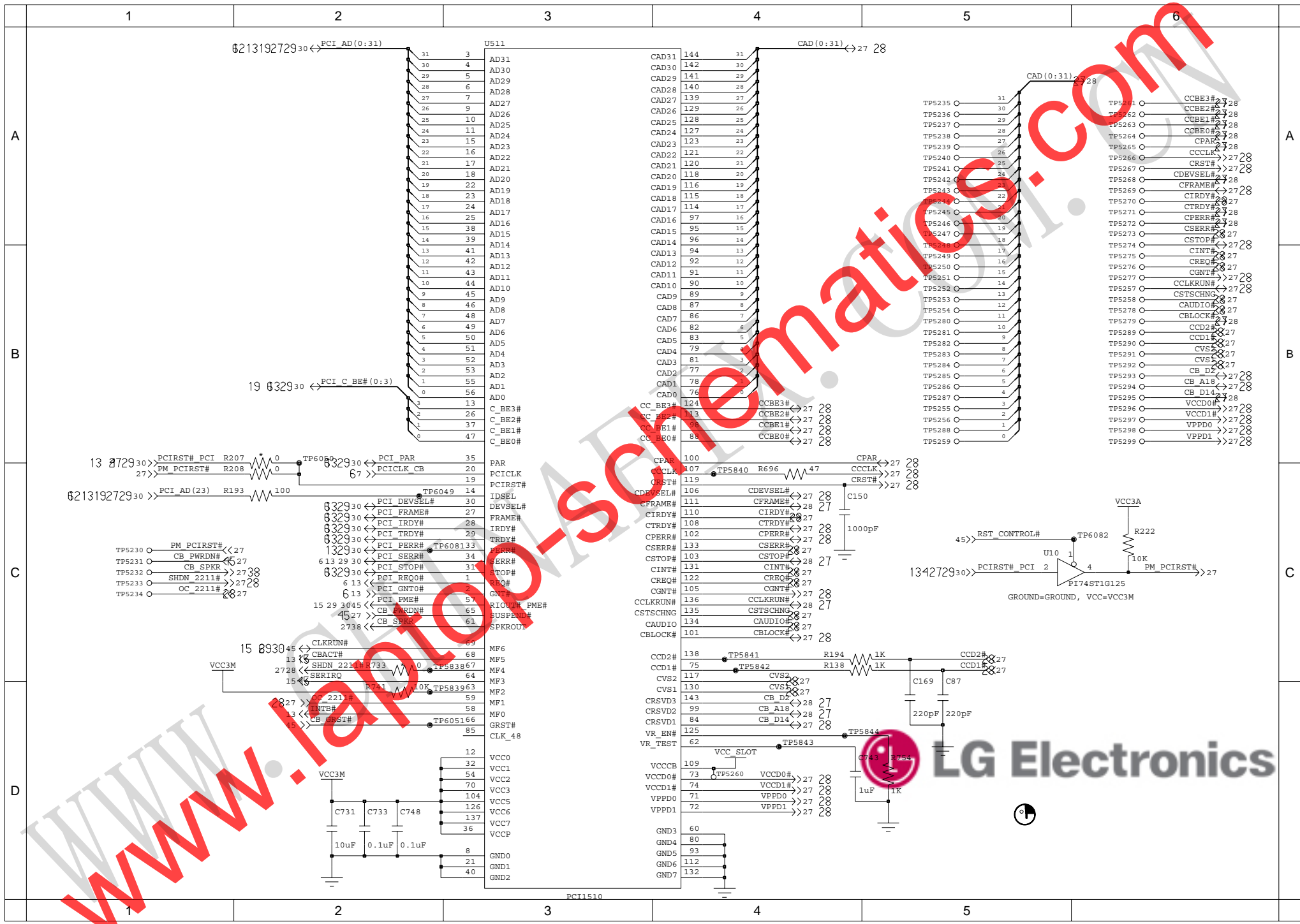


www.taptop-schematics.com

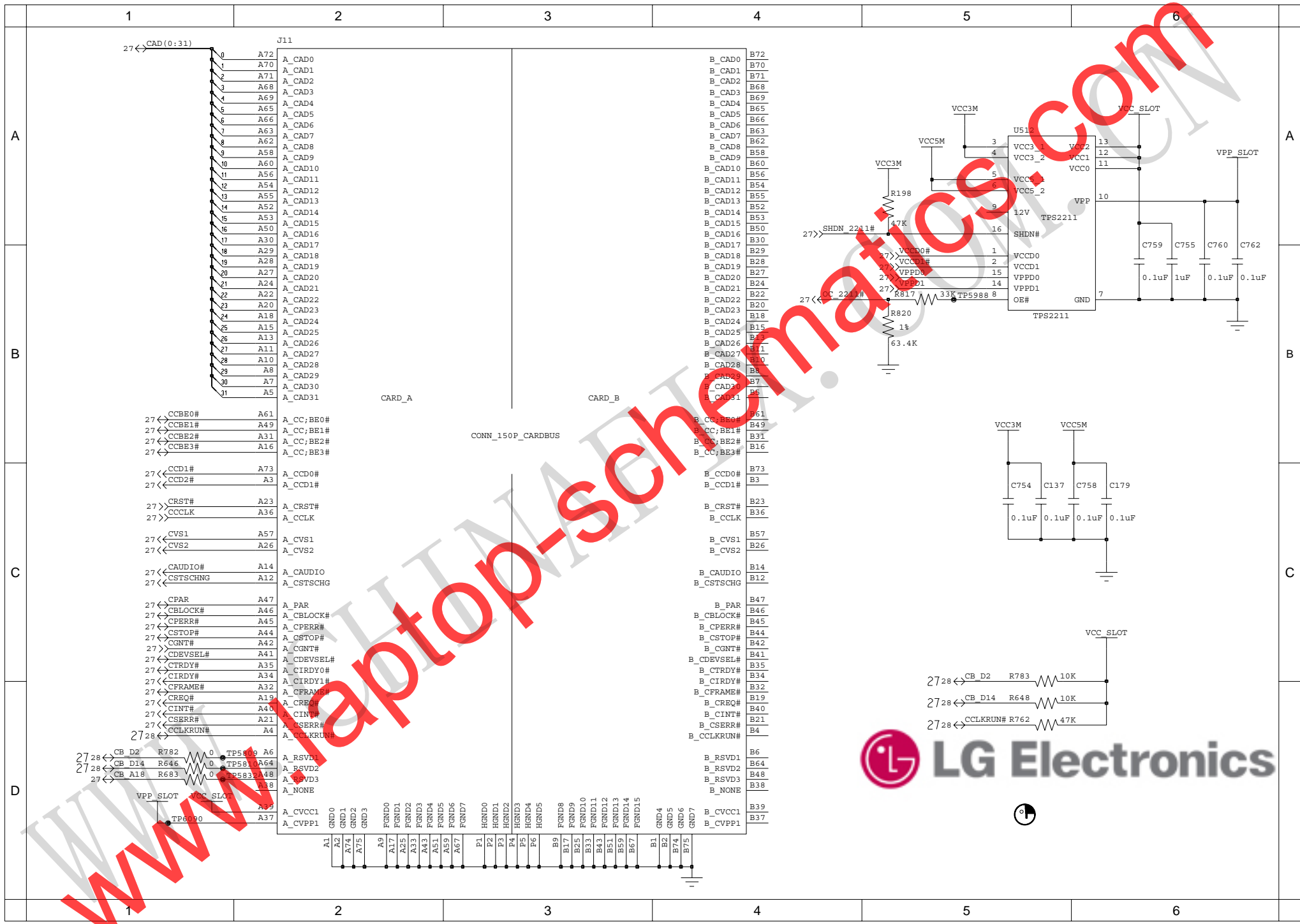


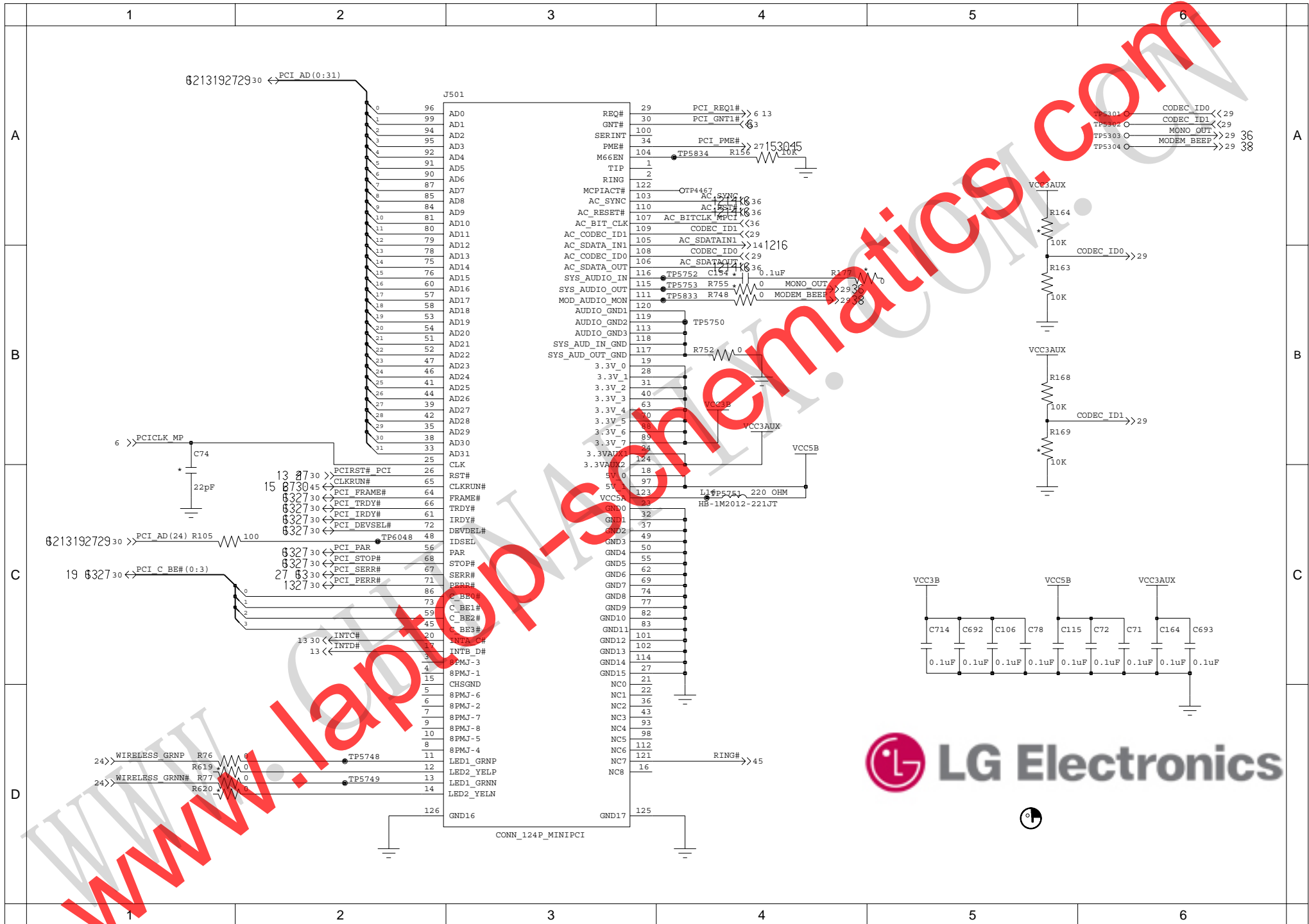
www.tropicschematic.com

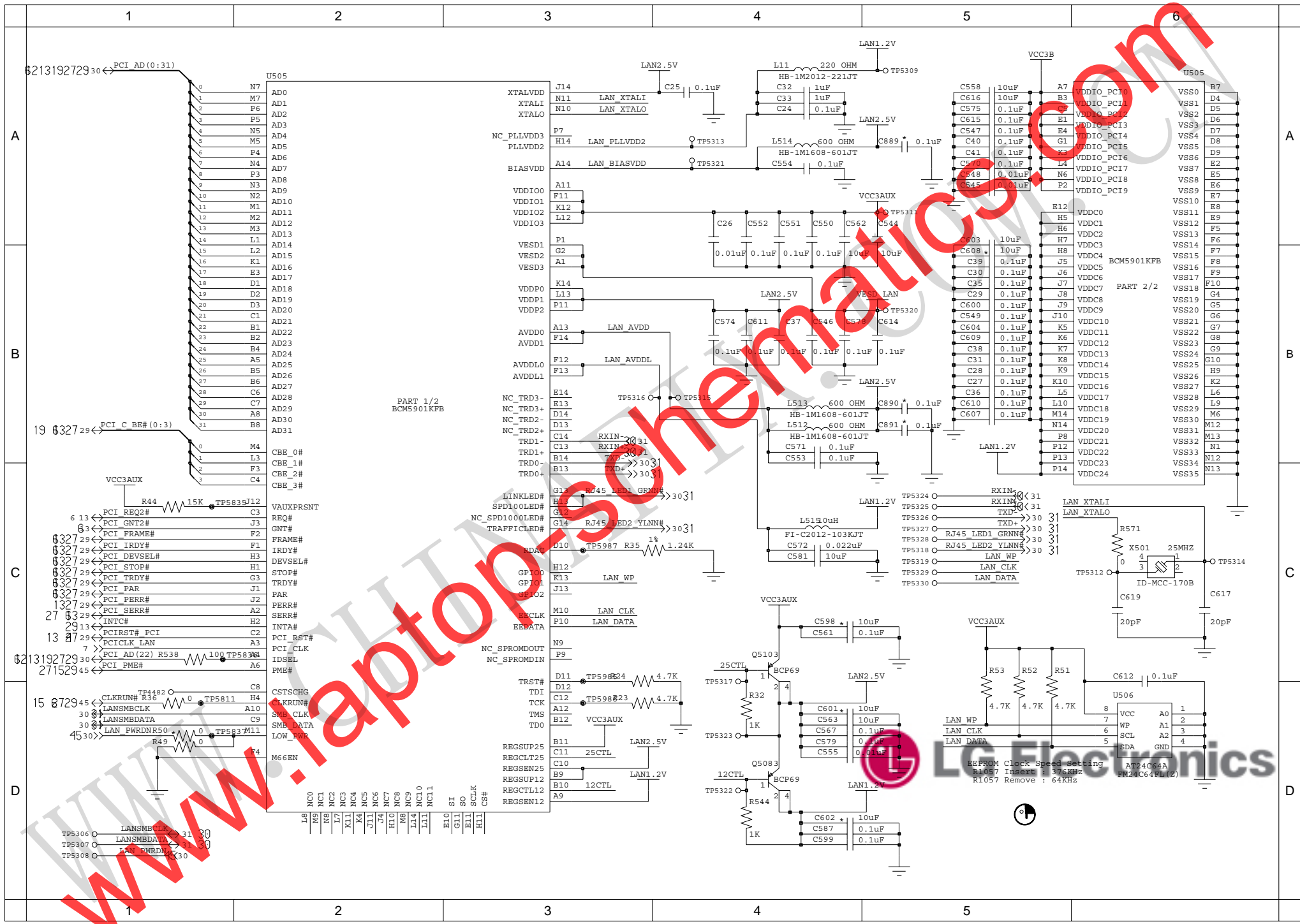




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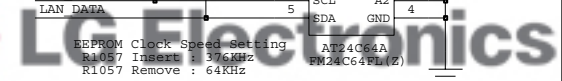




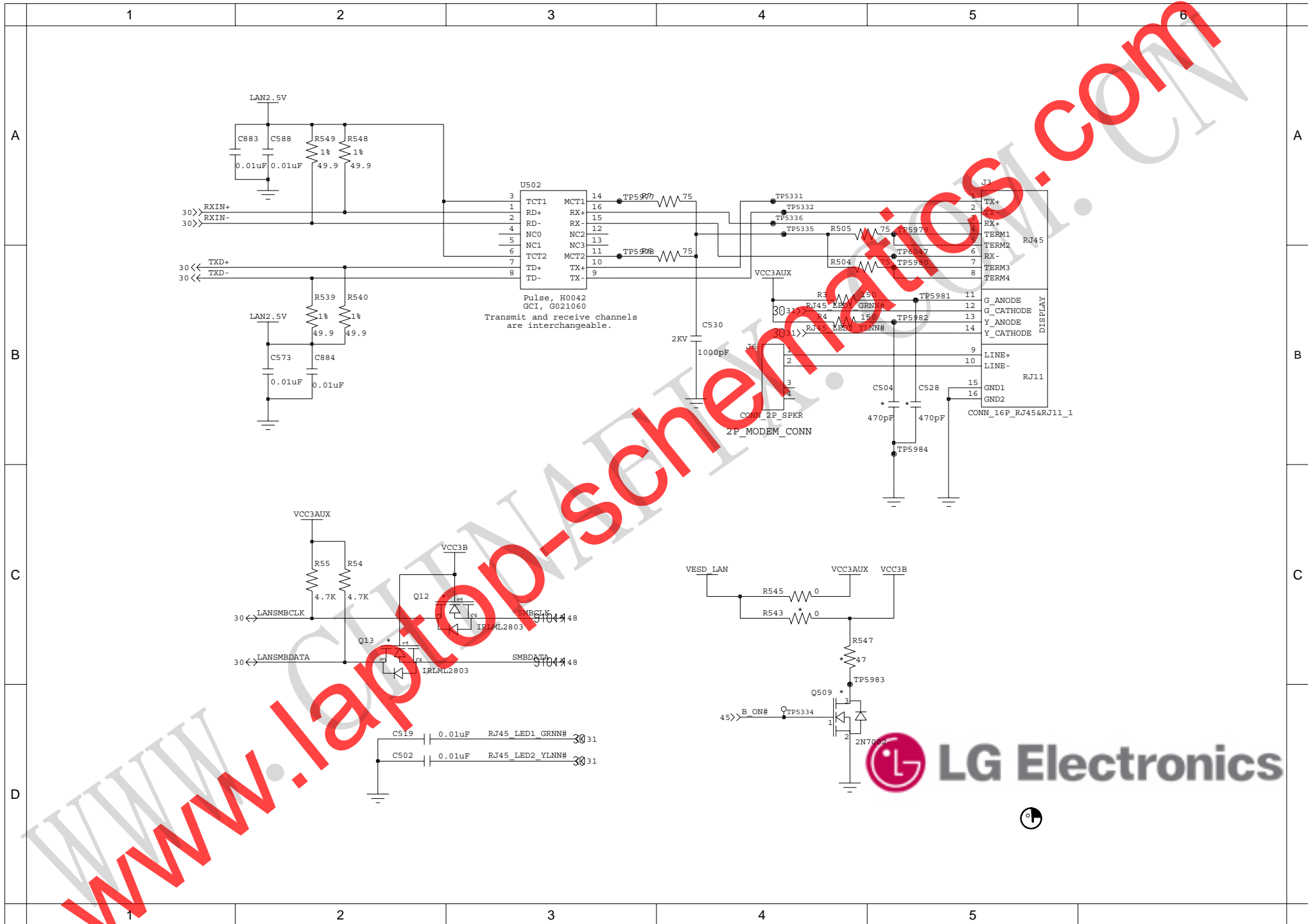


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EEPROM Clock Speed Setting
 R1057 Insert : 376KHz
 R1057 Remove : 64KHz



AT24C64A
 FM24C64FL(Z)

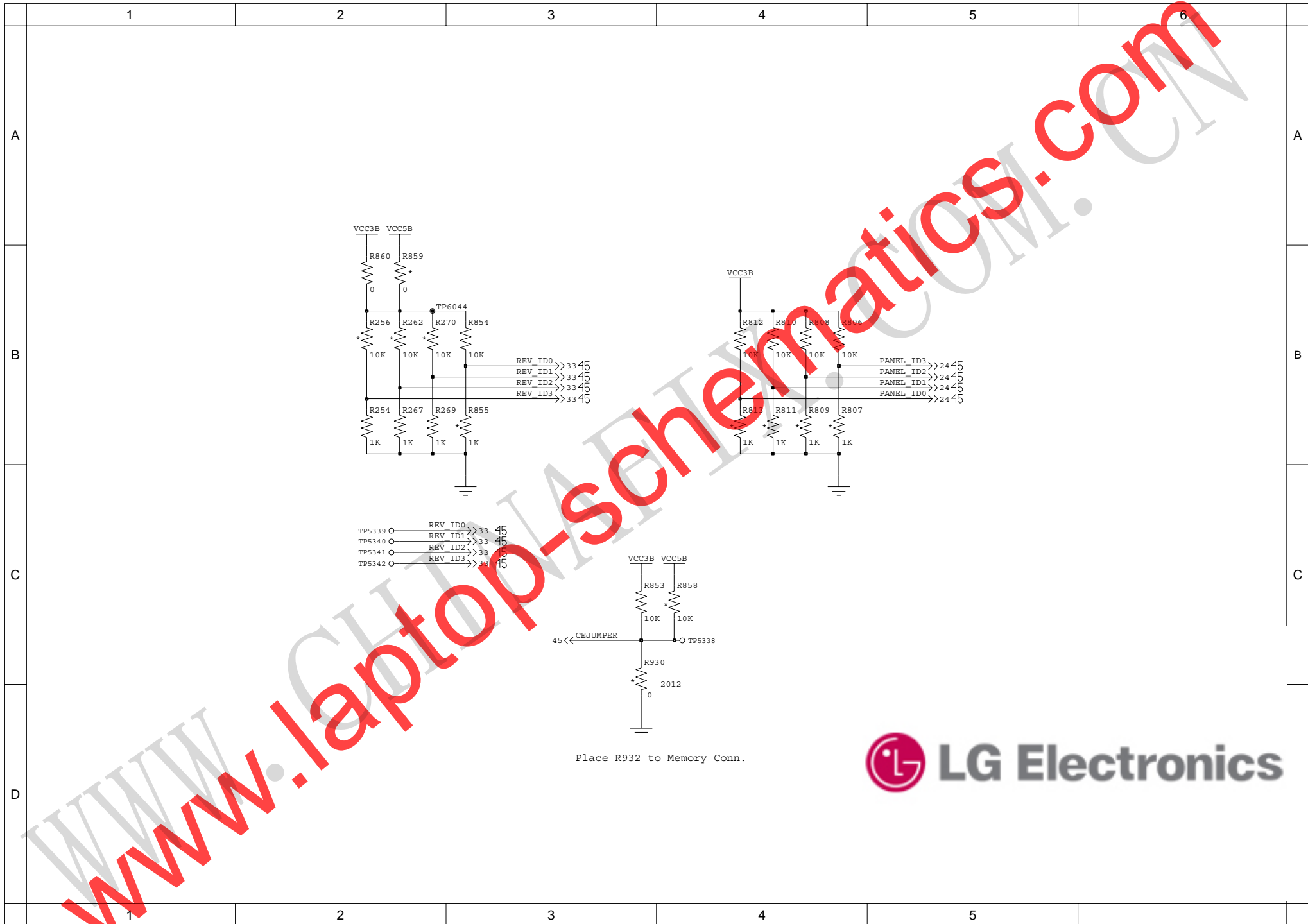


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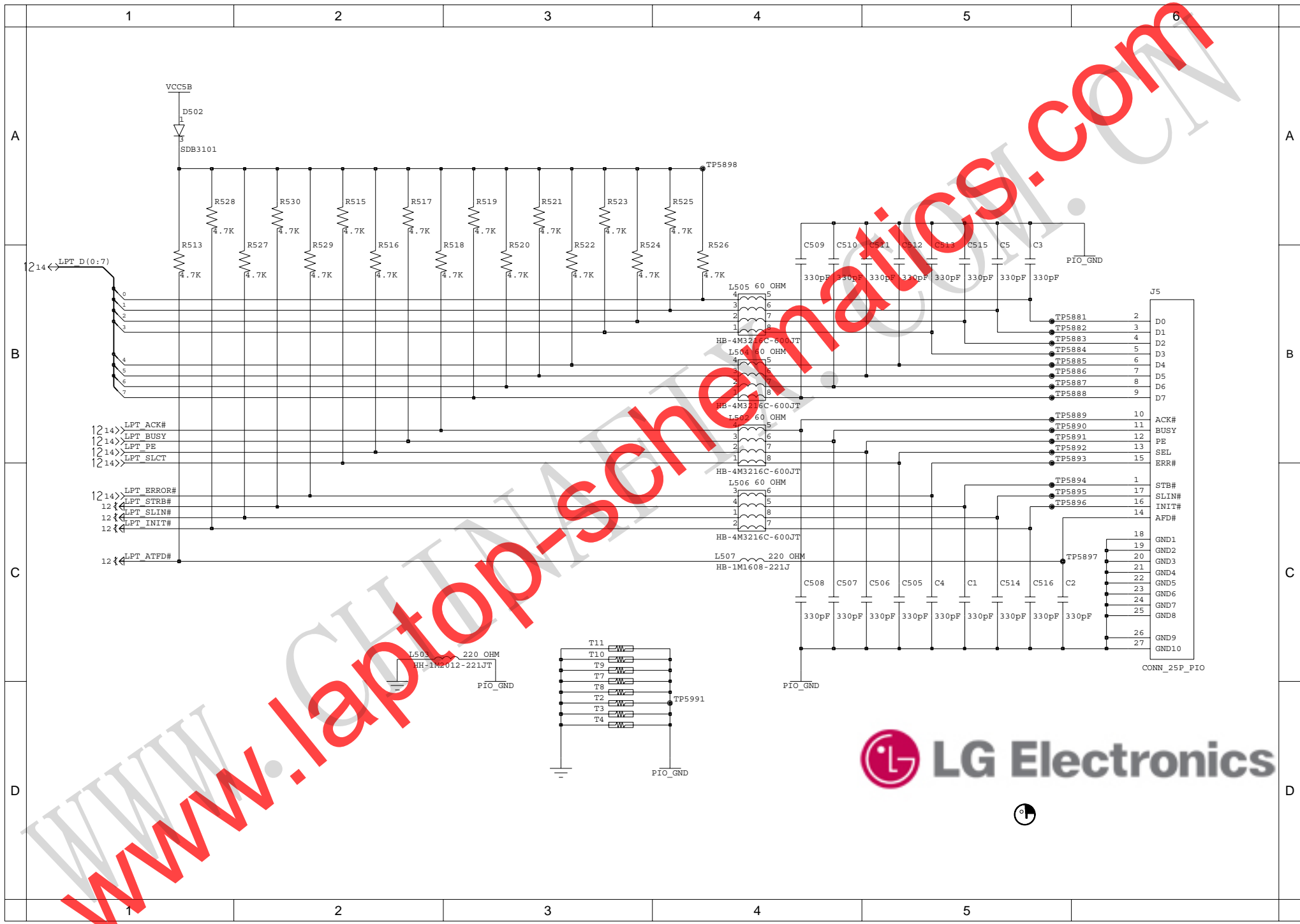


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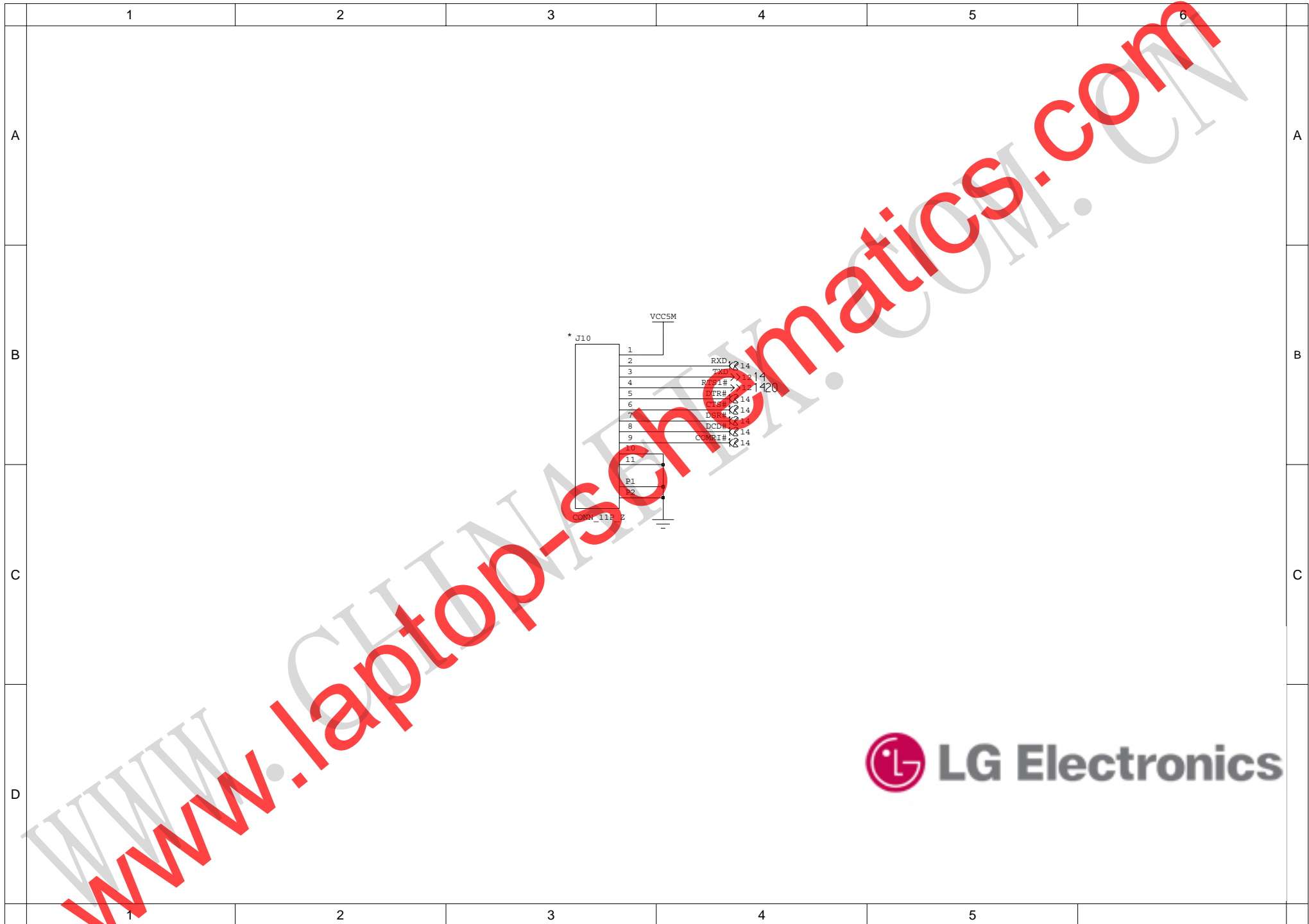
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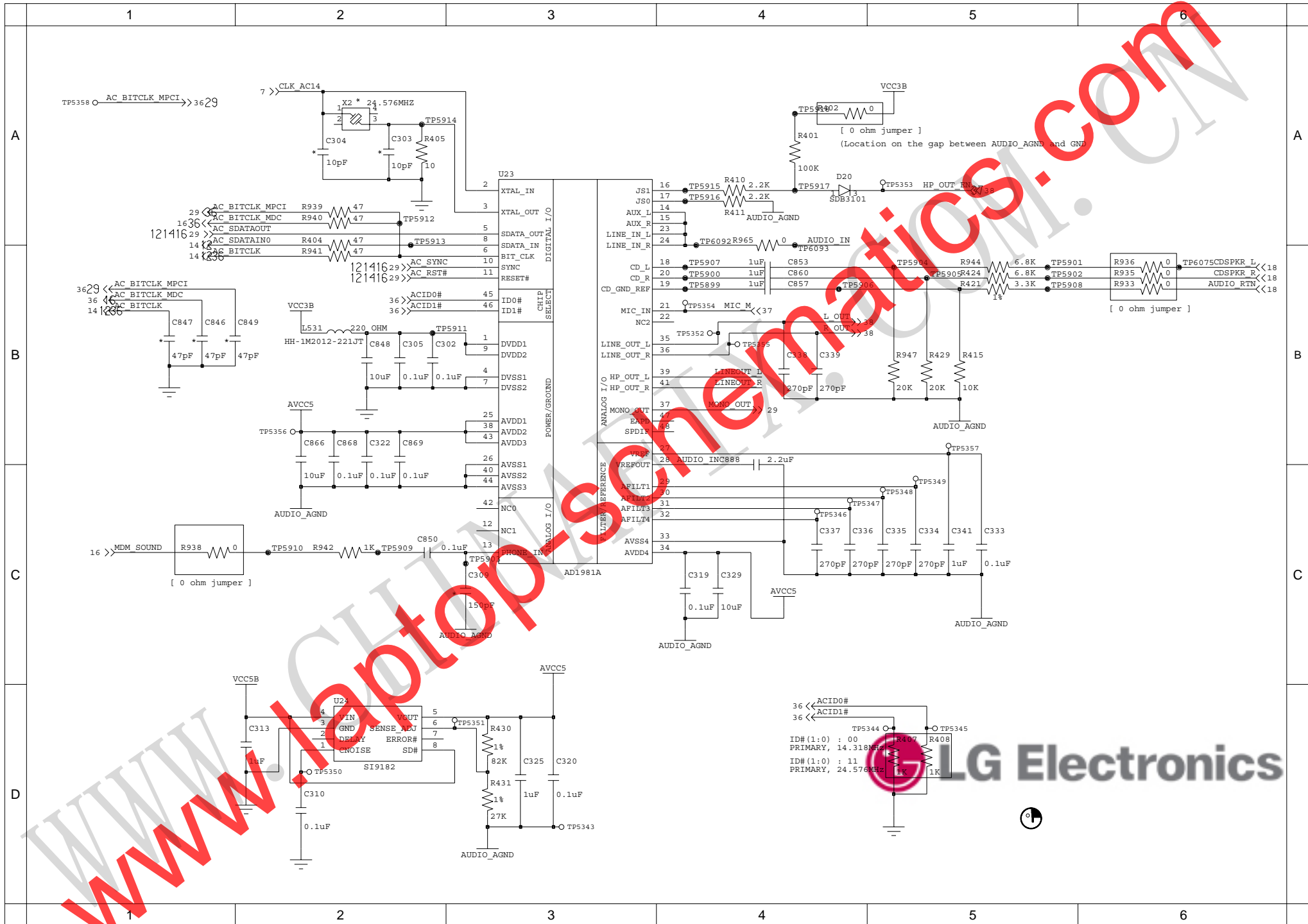


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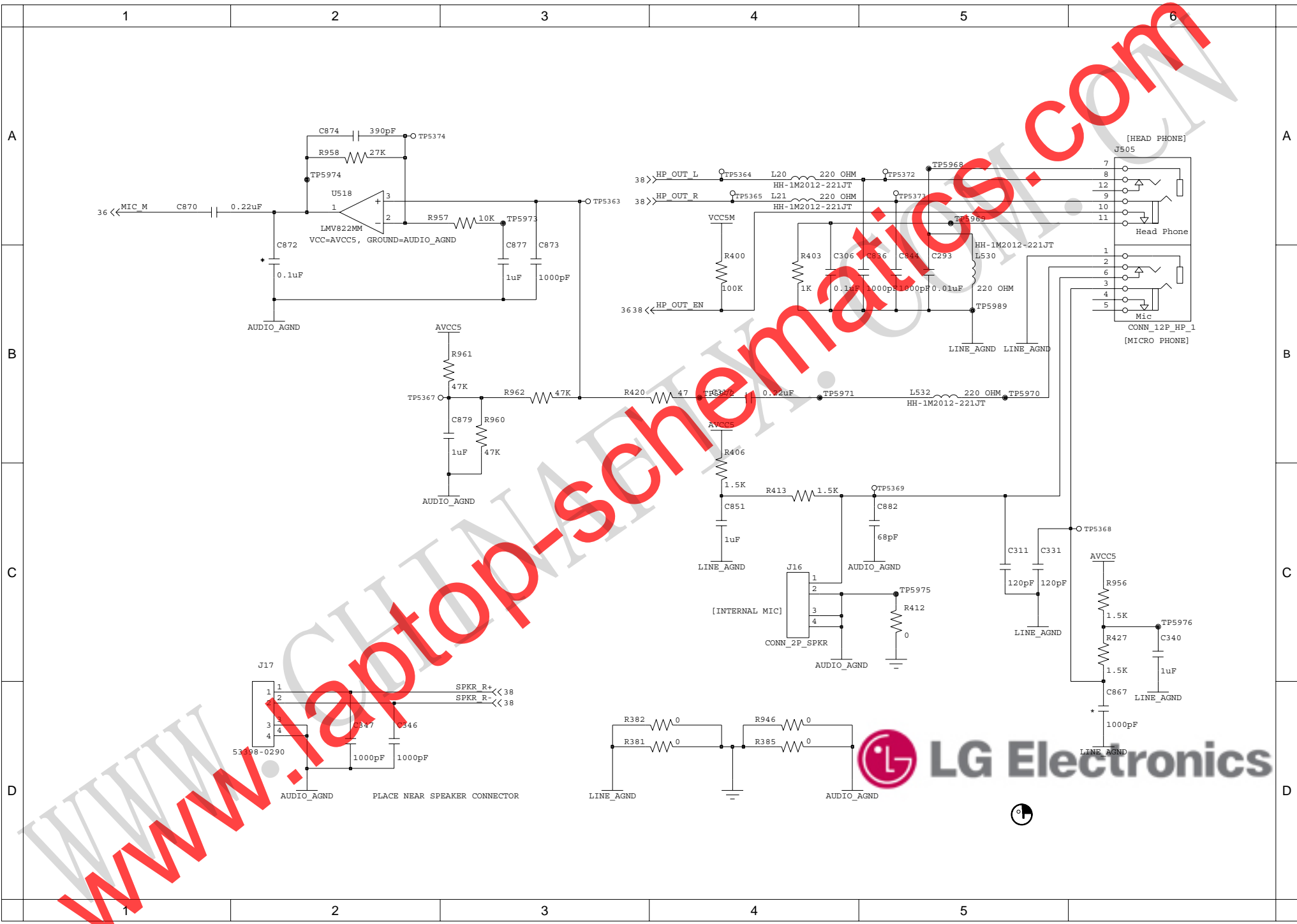


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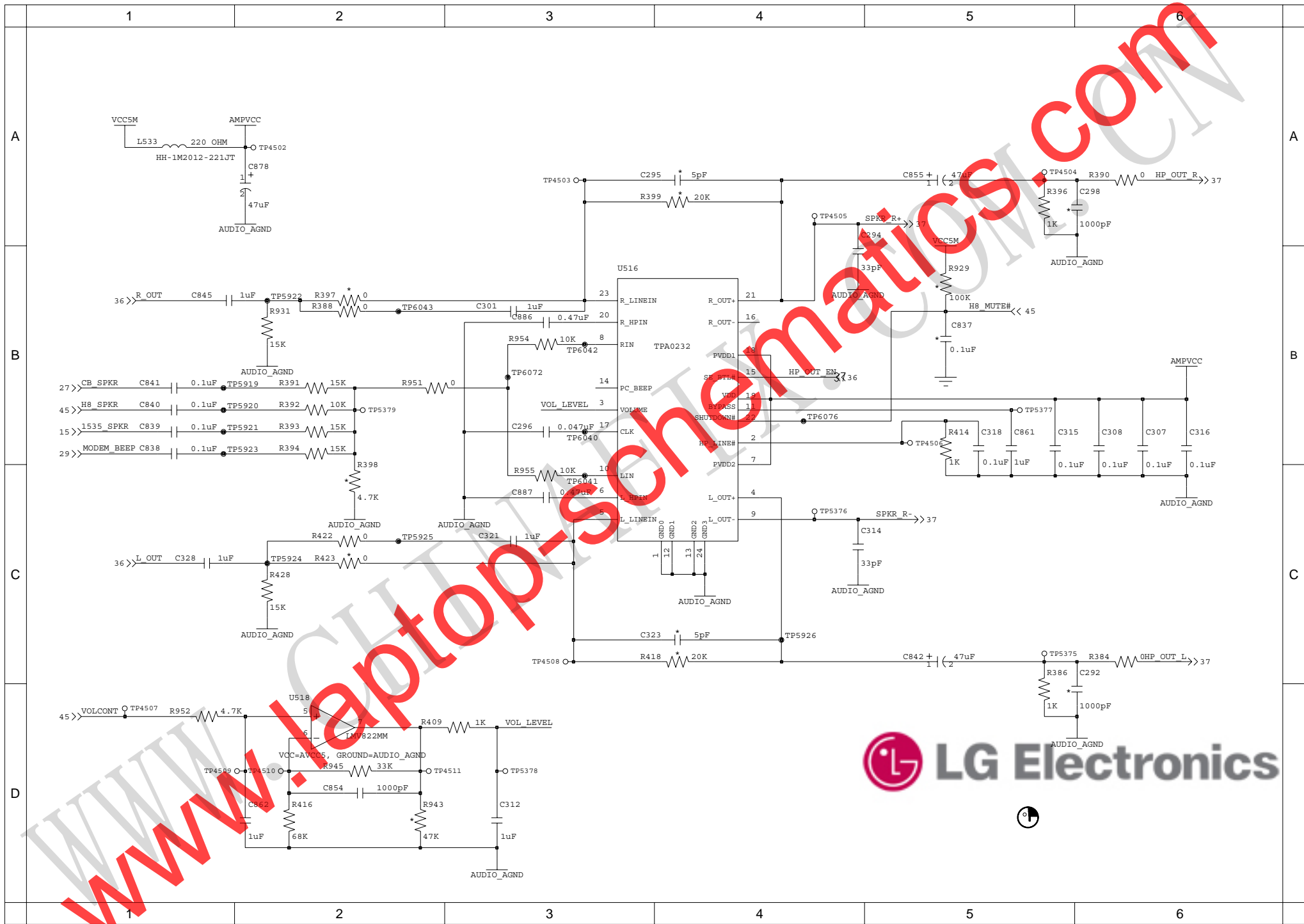


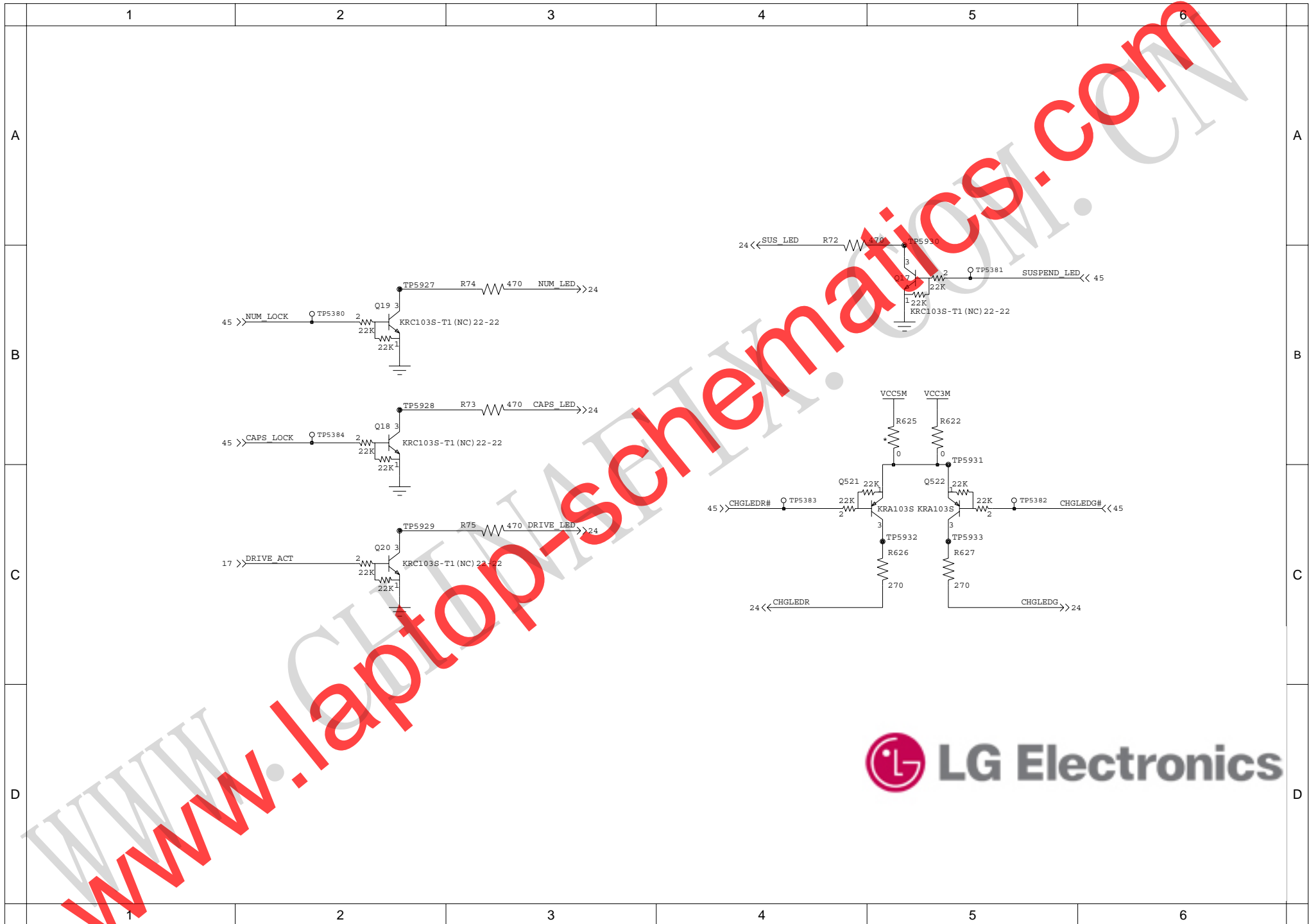


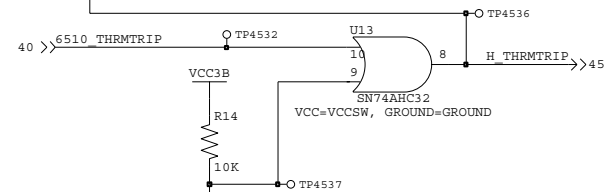
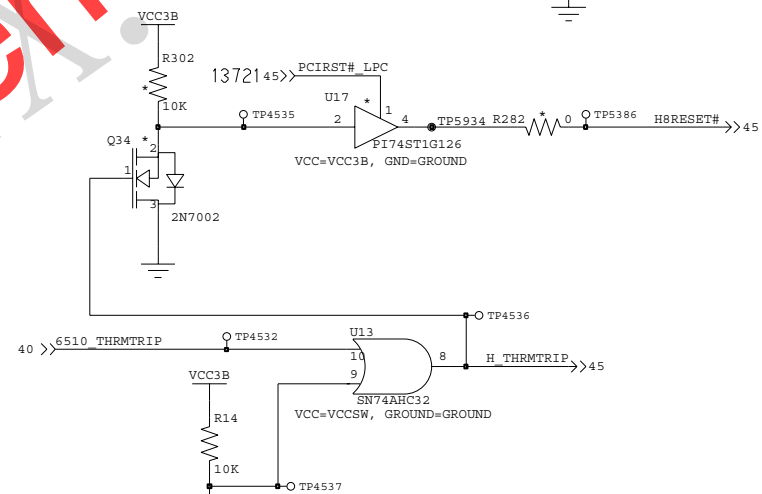
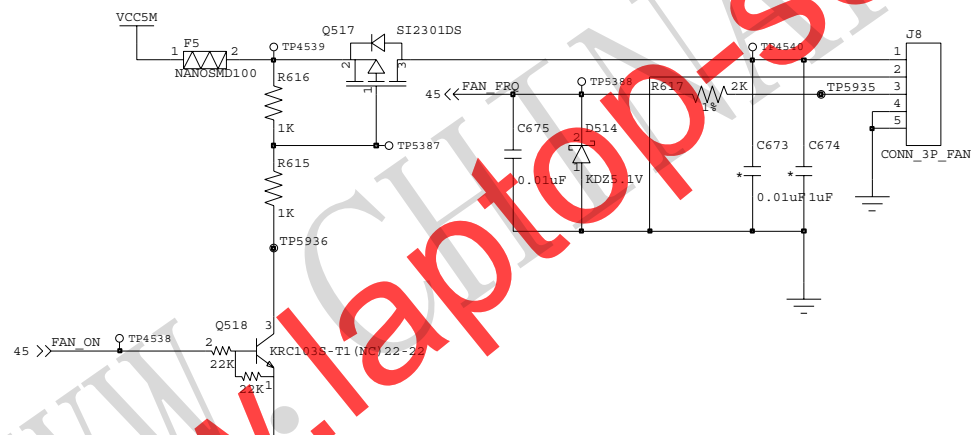
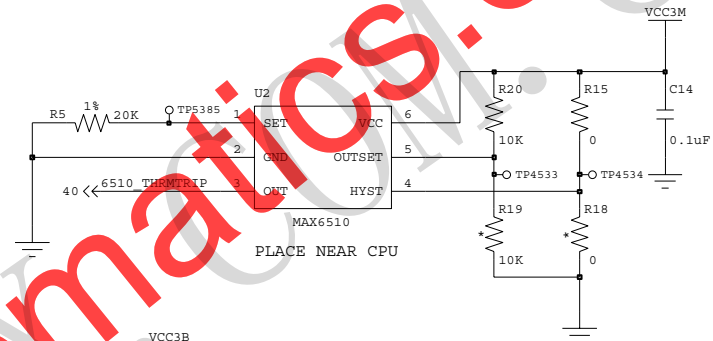
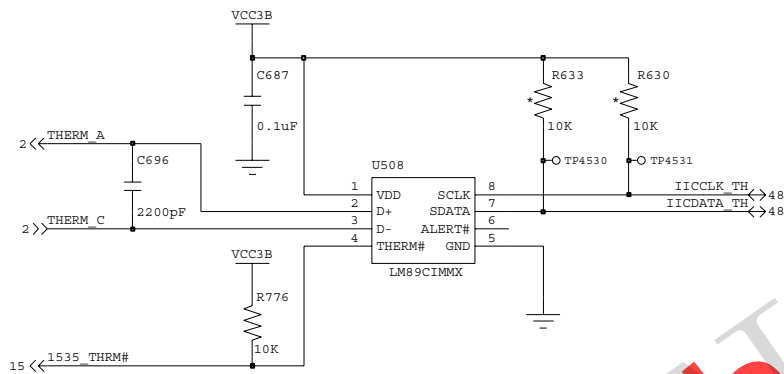
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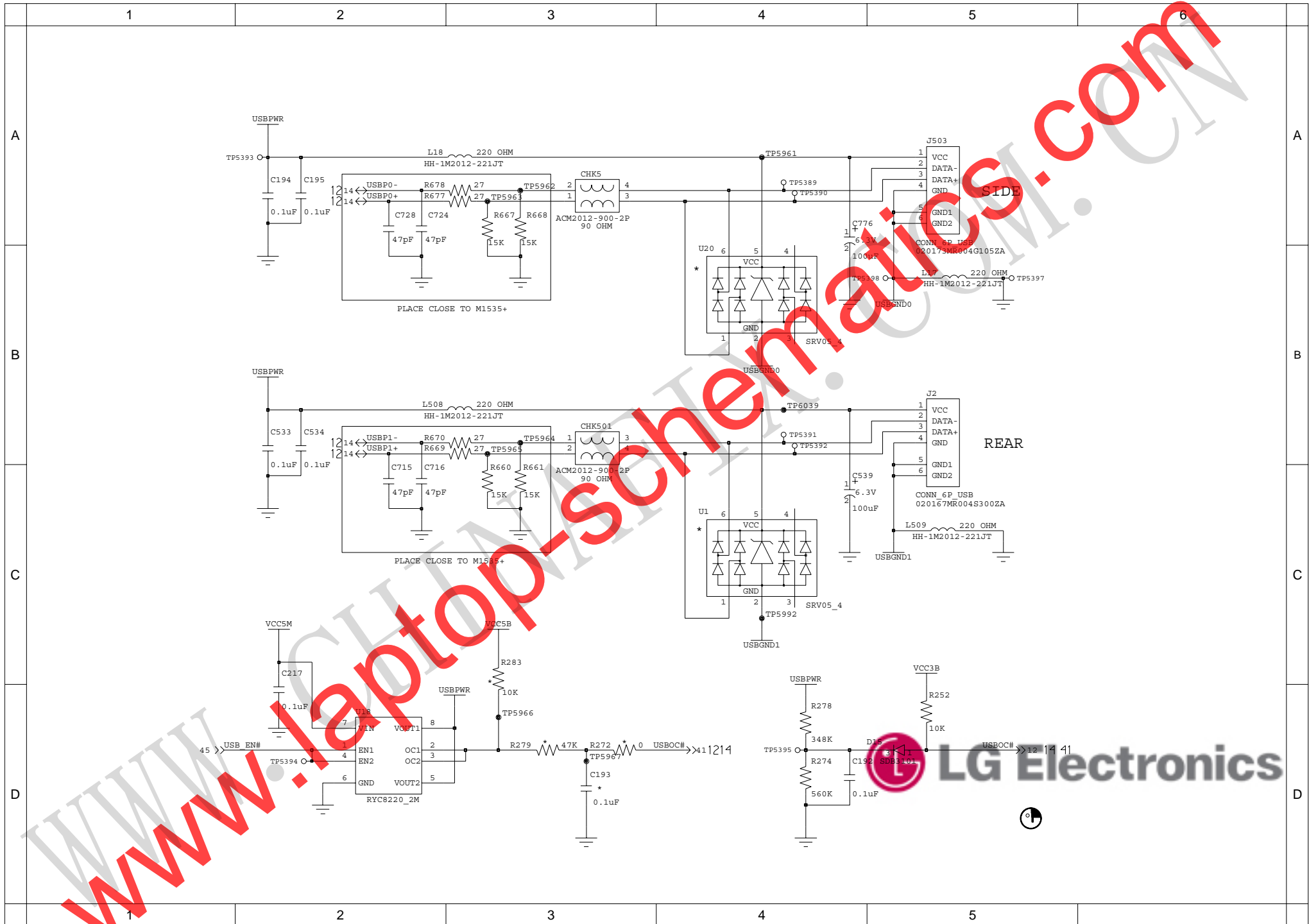
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C							C
D							D
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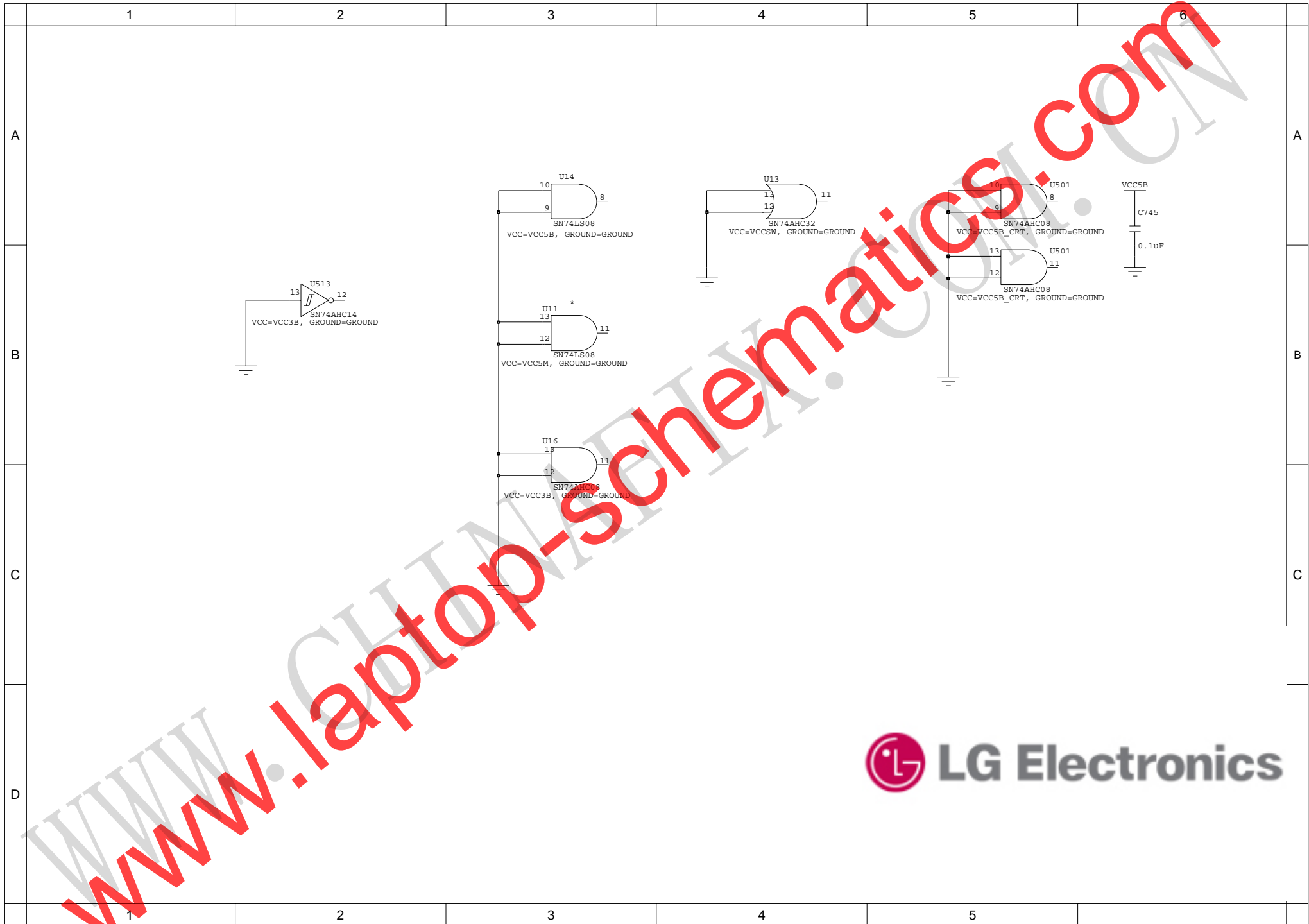


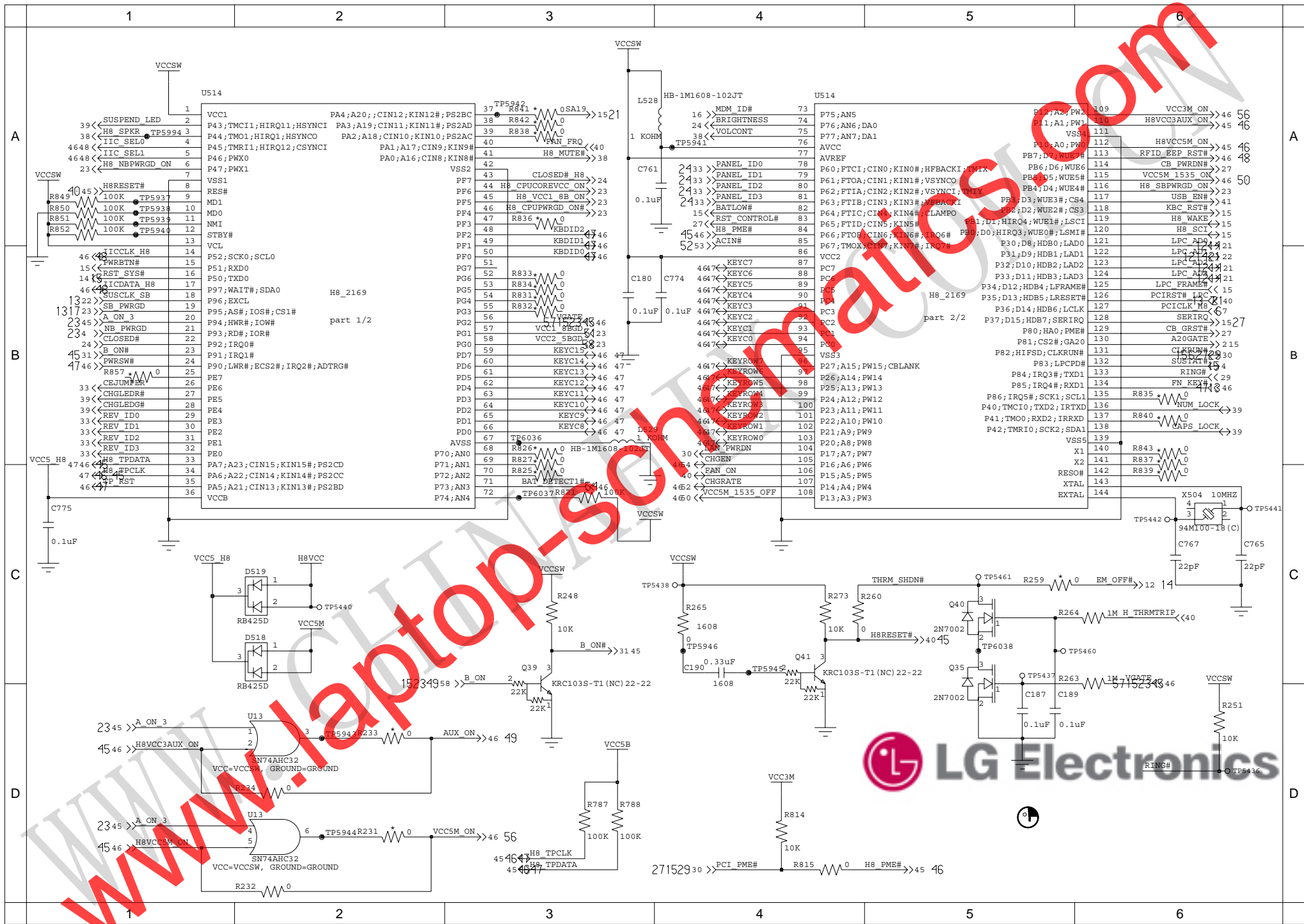
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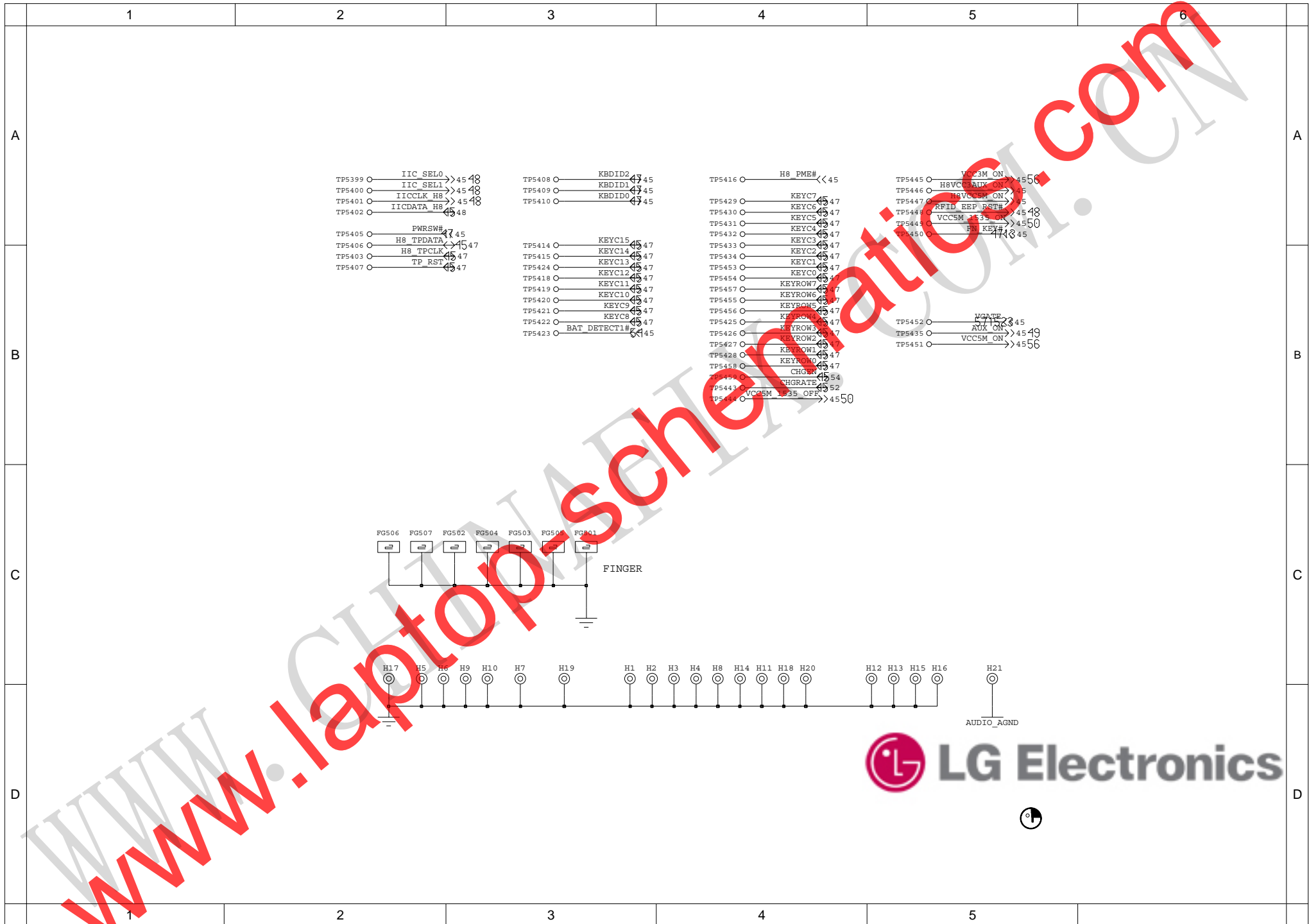
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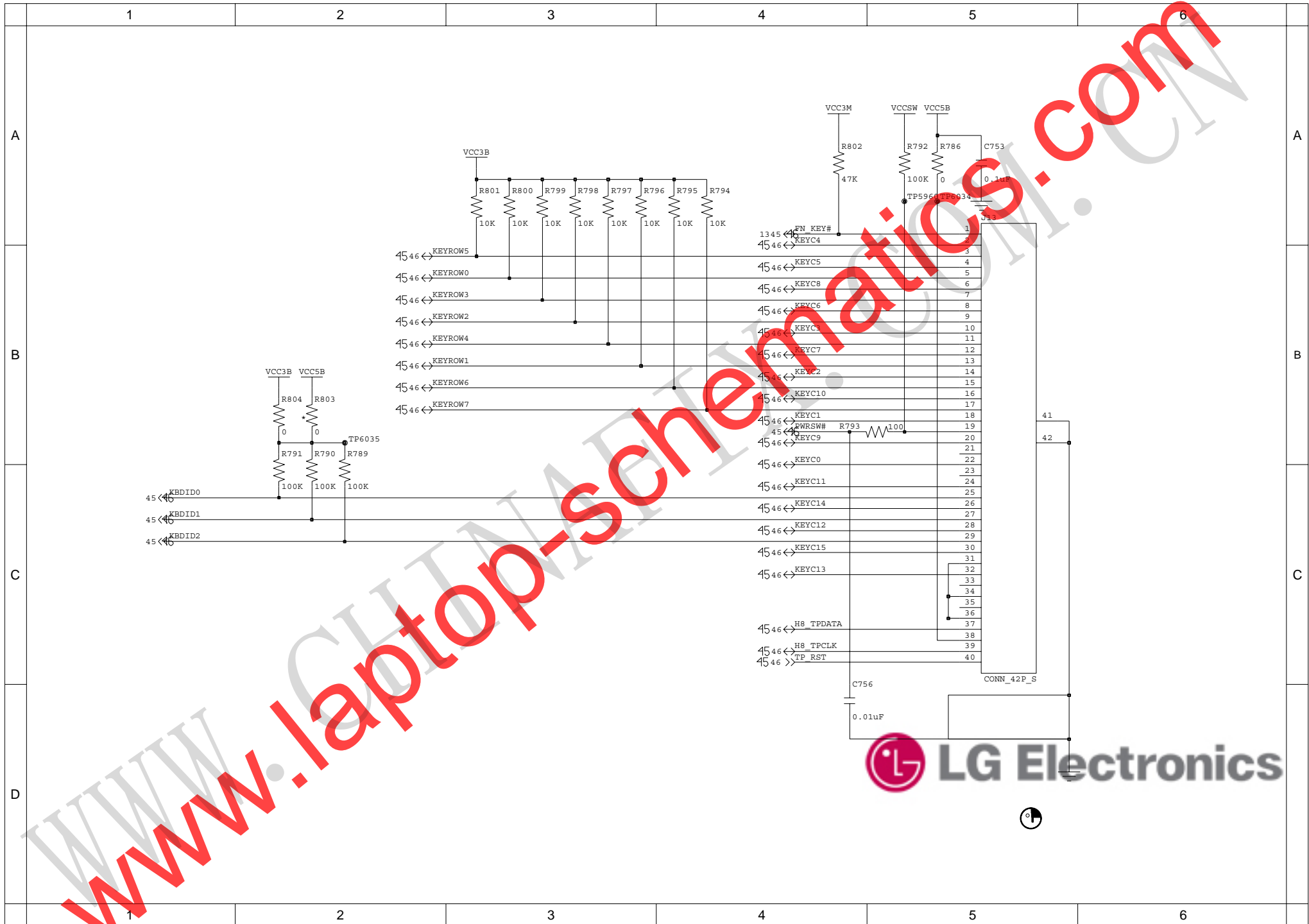


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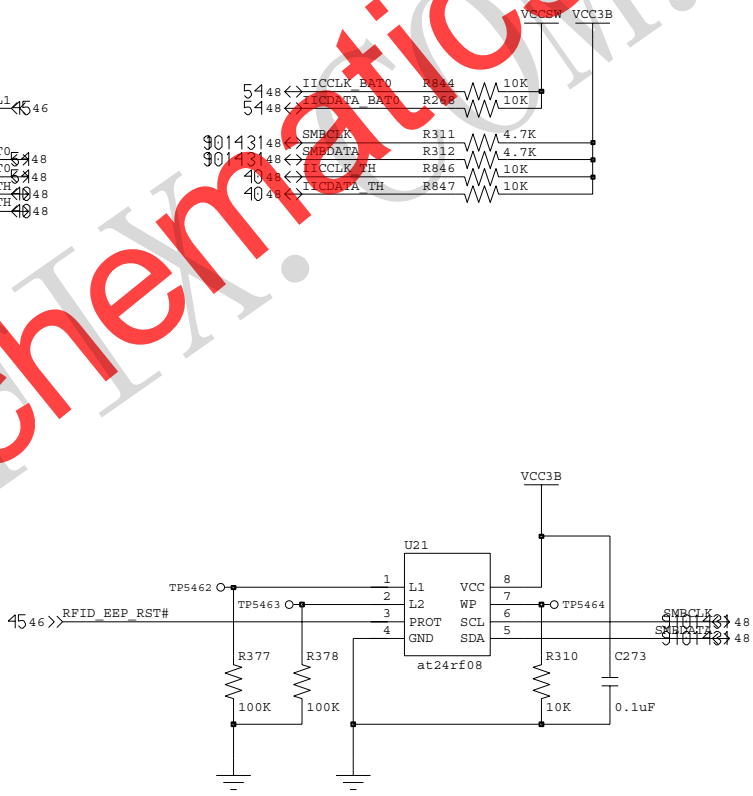
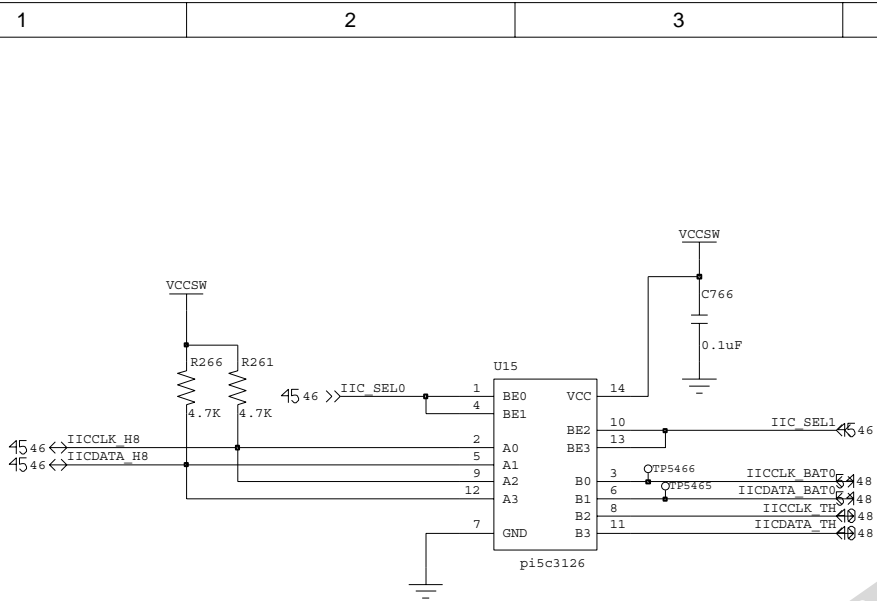






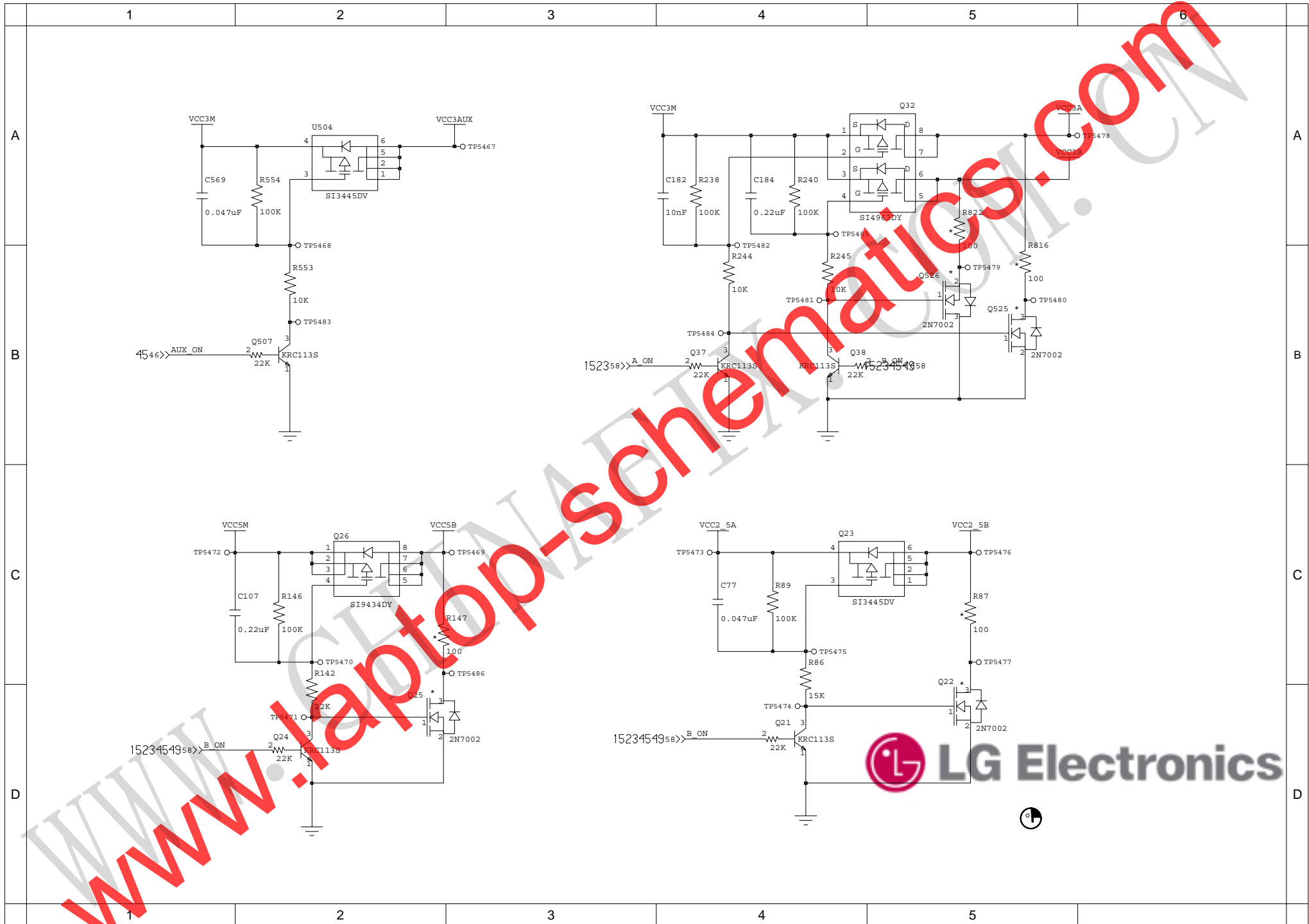


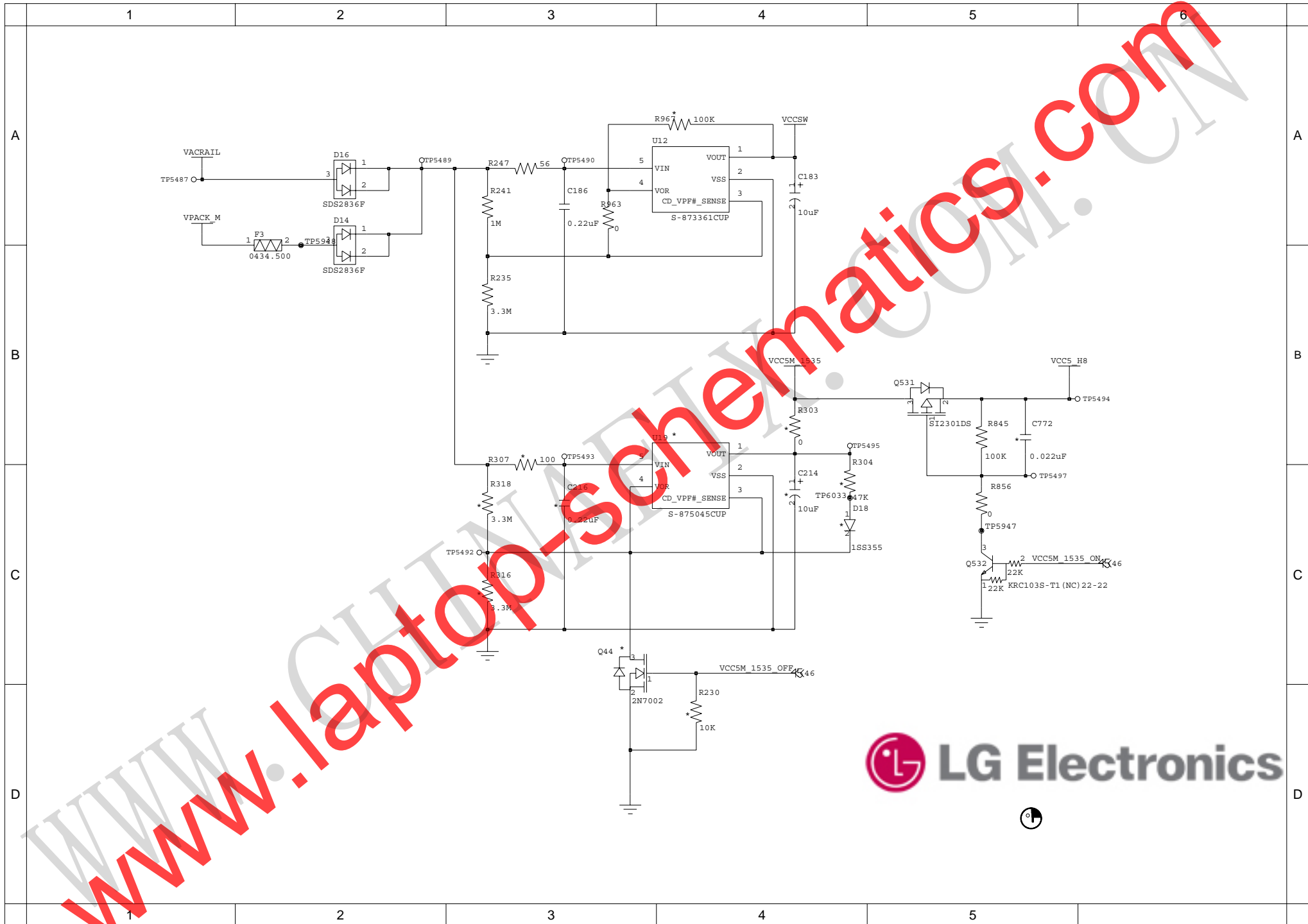
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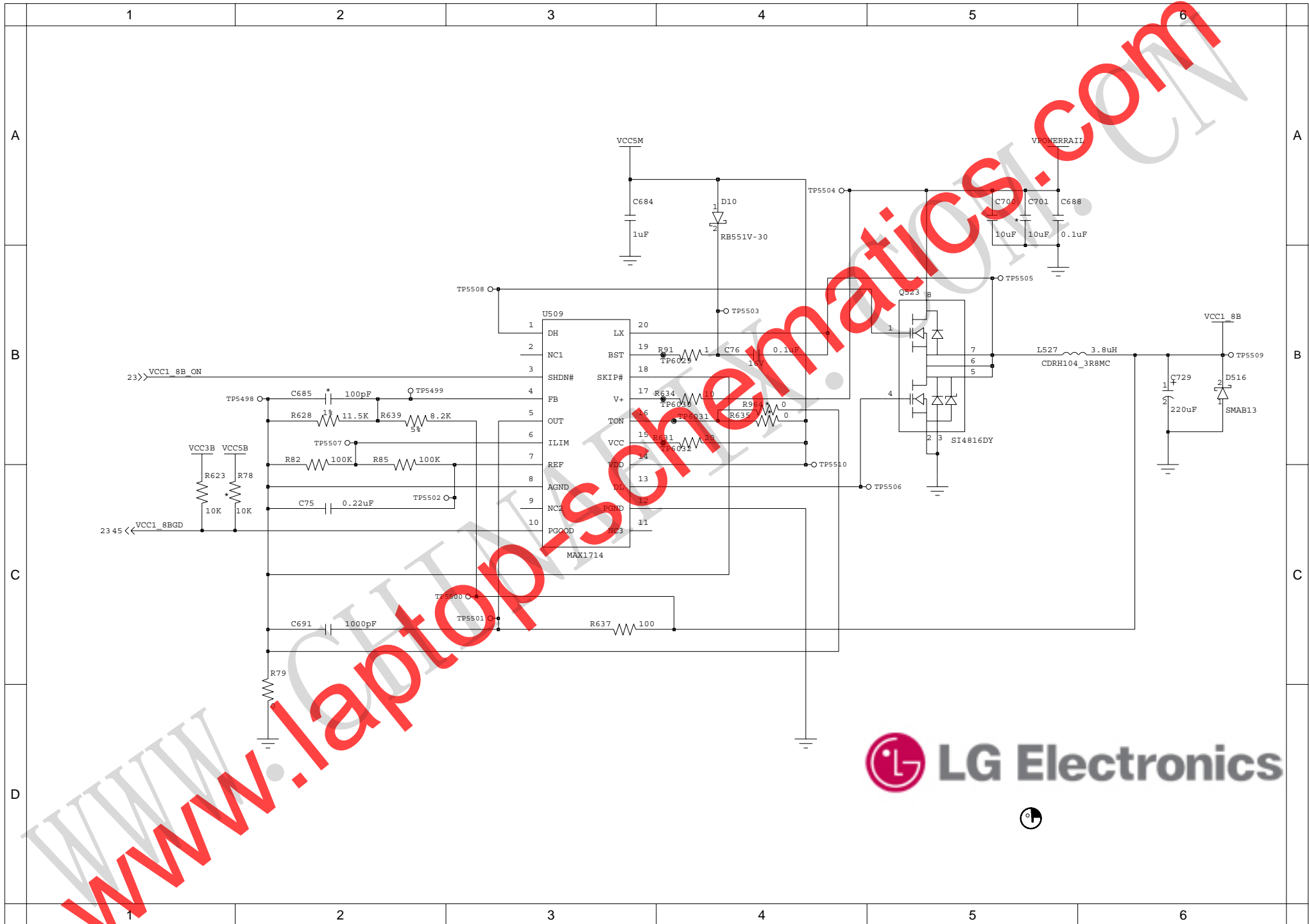


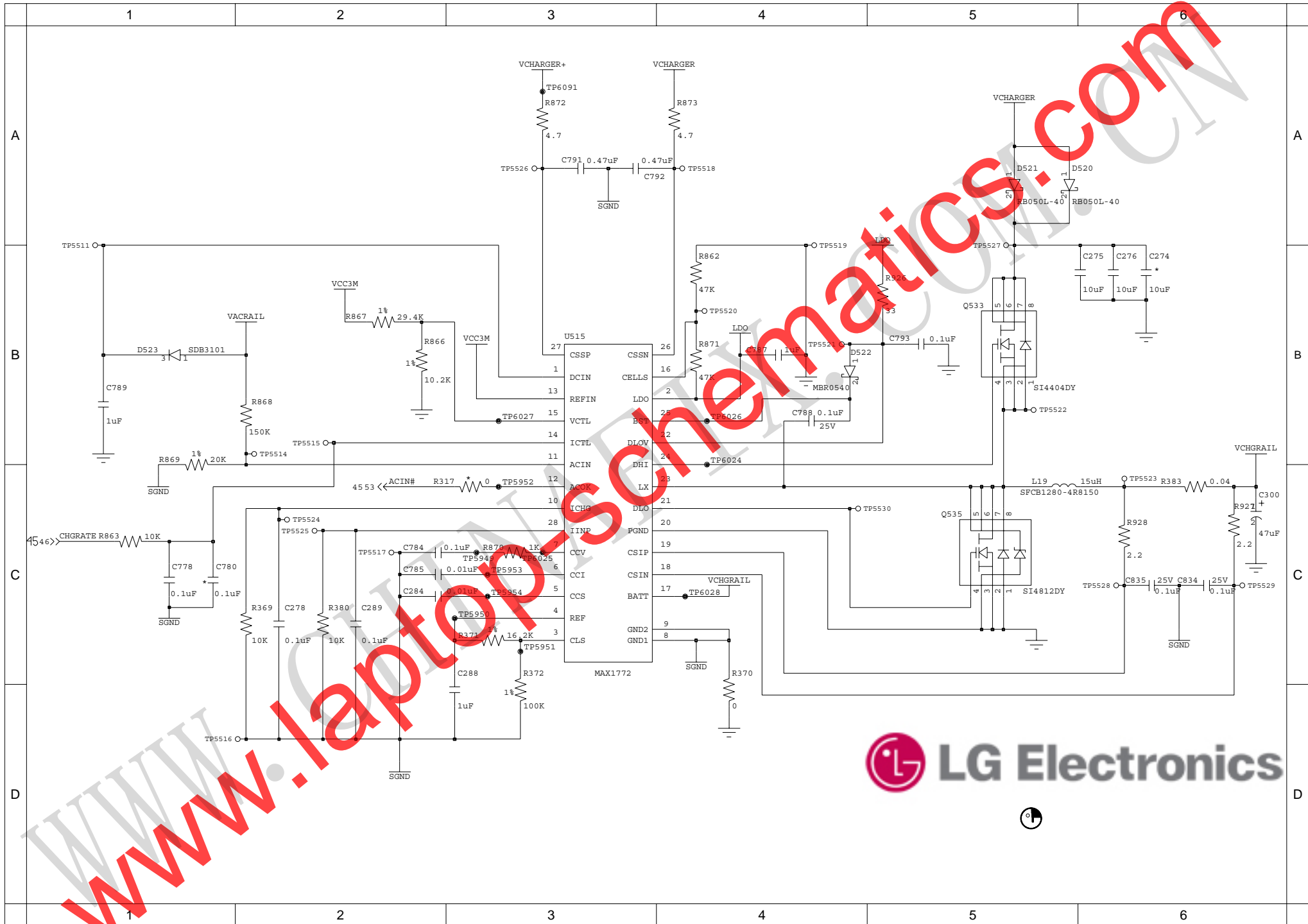
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HIGH	LOW	IICCLK_BATO	IICDATA_BATO
LOW	HIGH	IICCLK_TH	IICDATA_TH

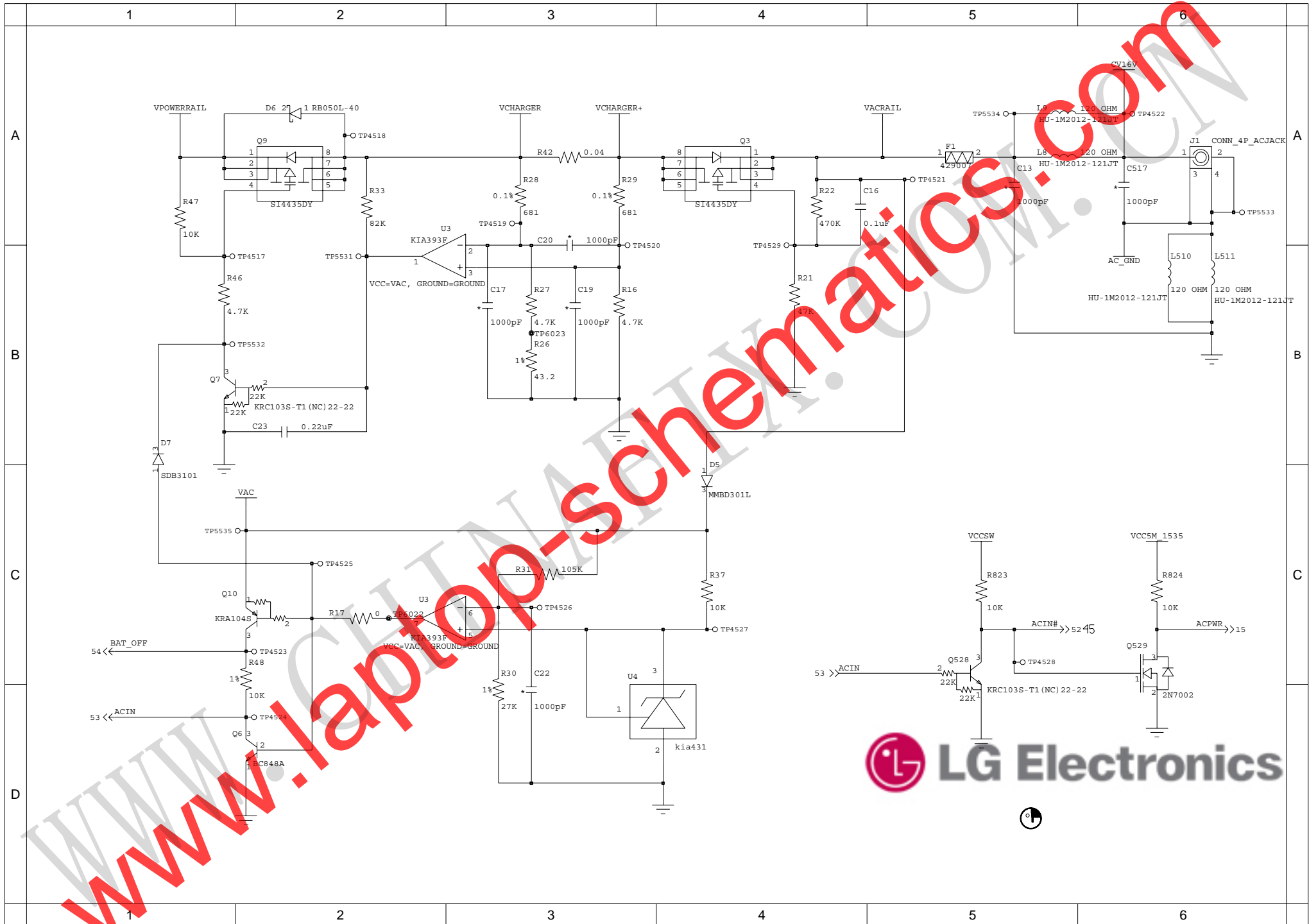


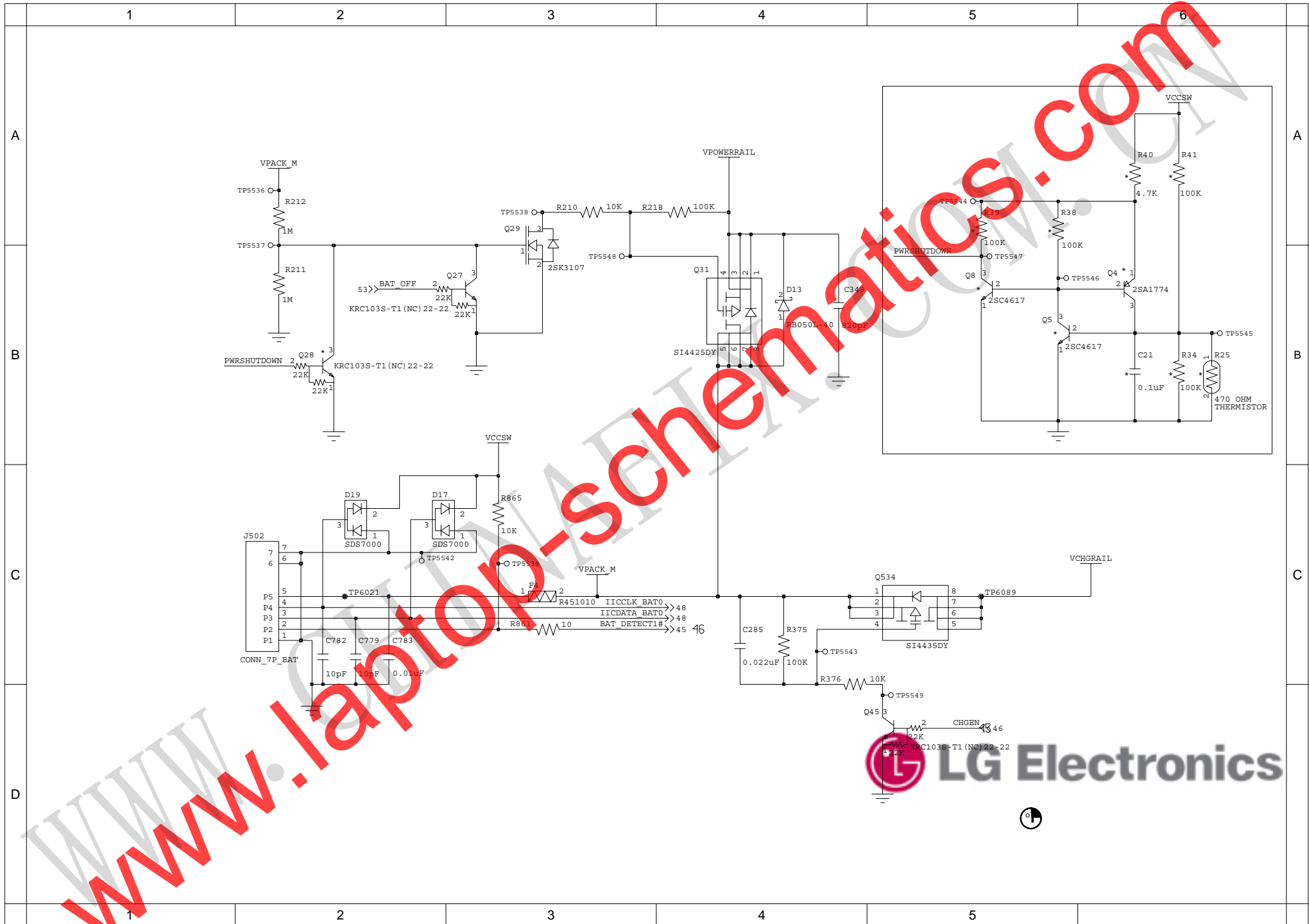


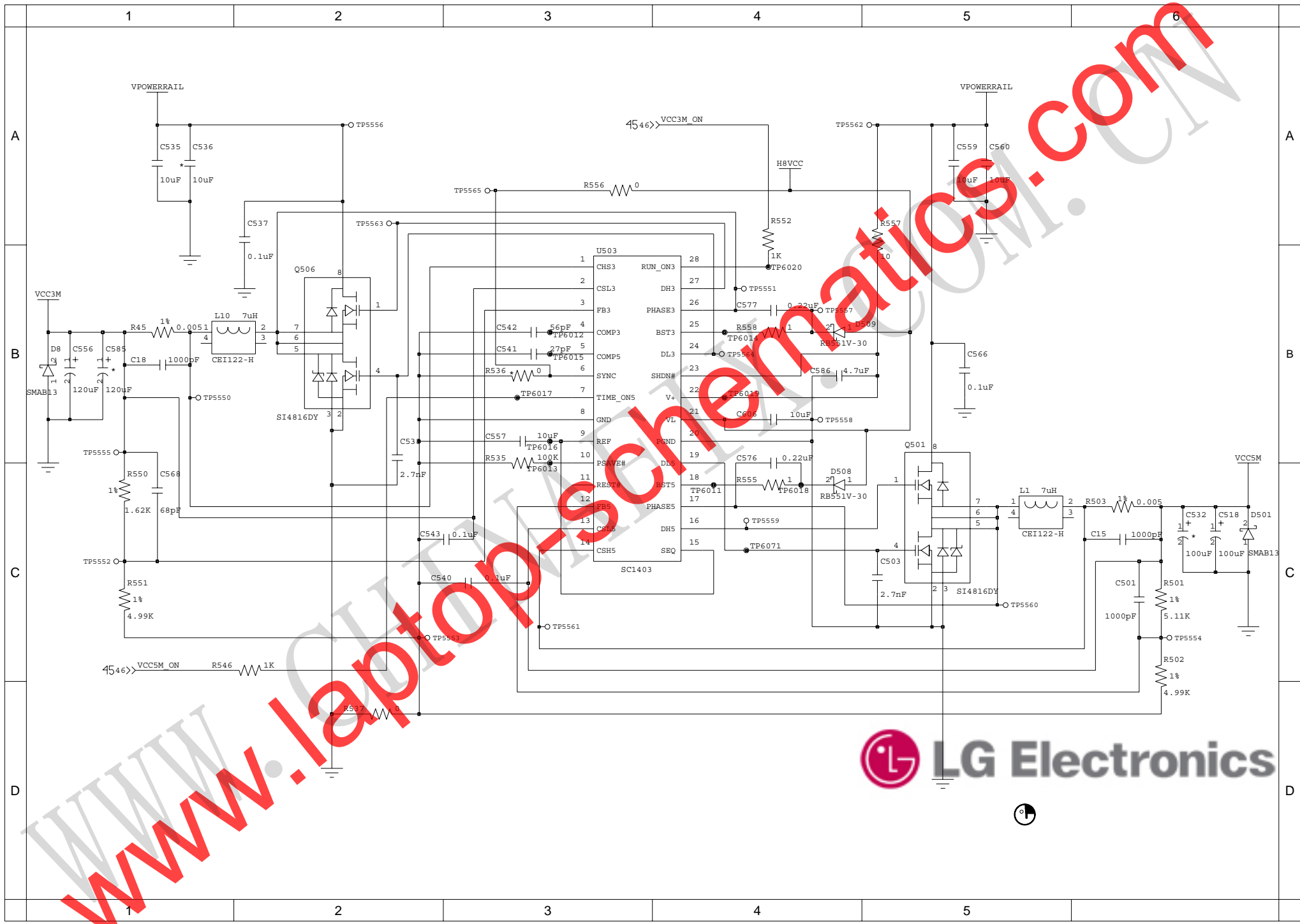




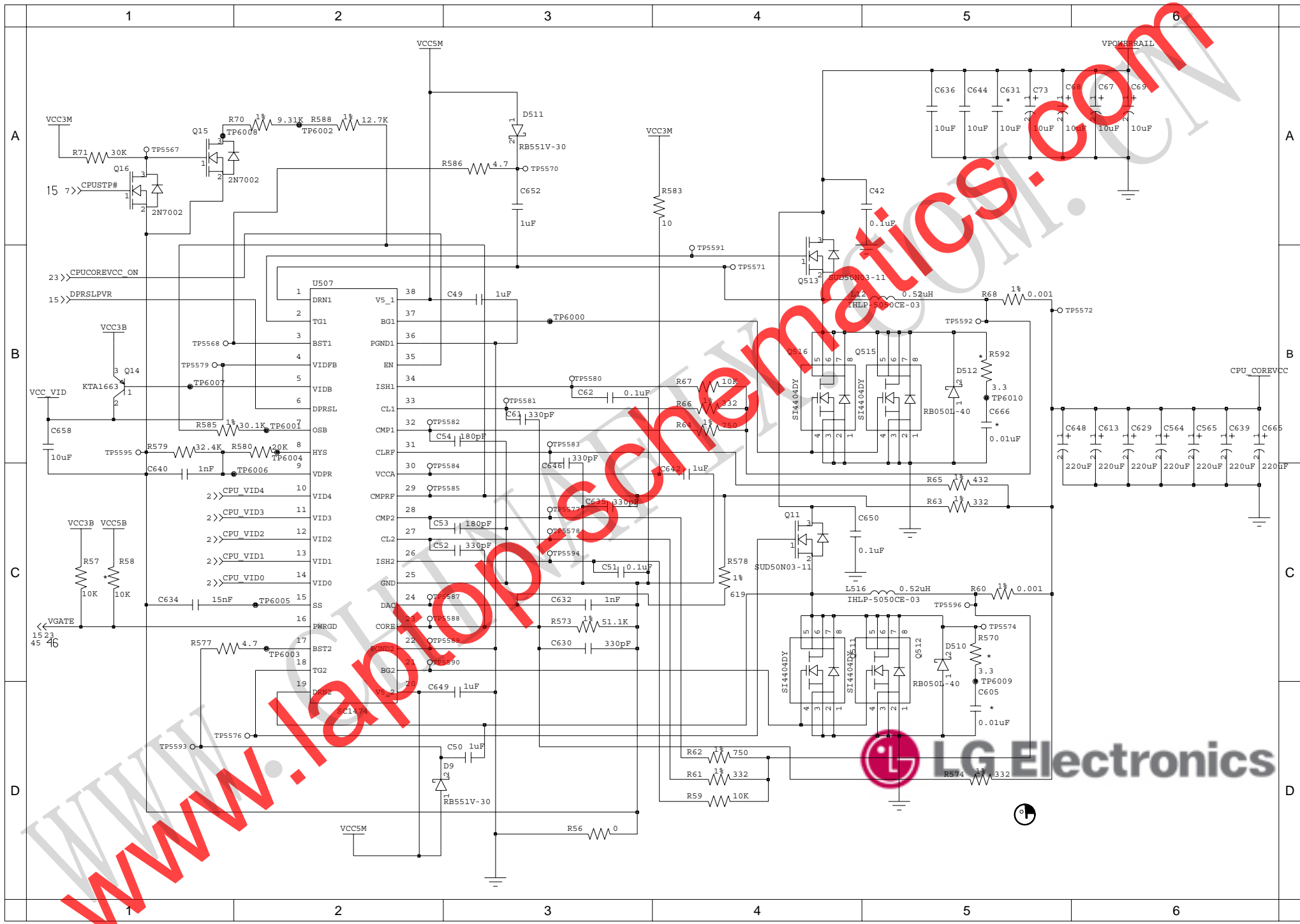






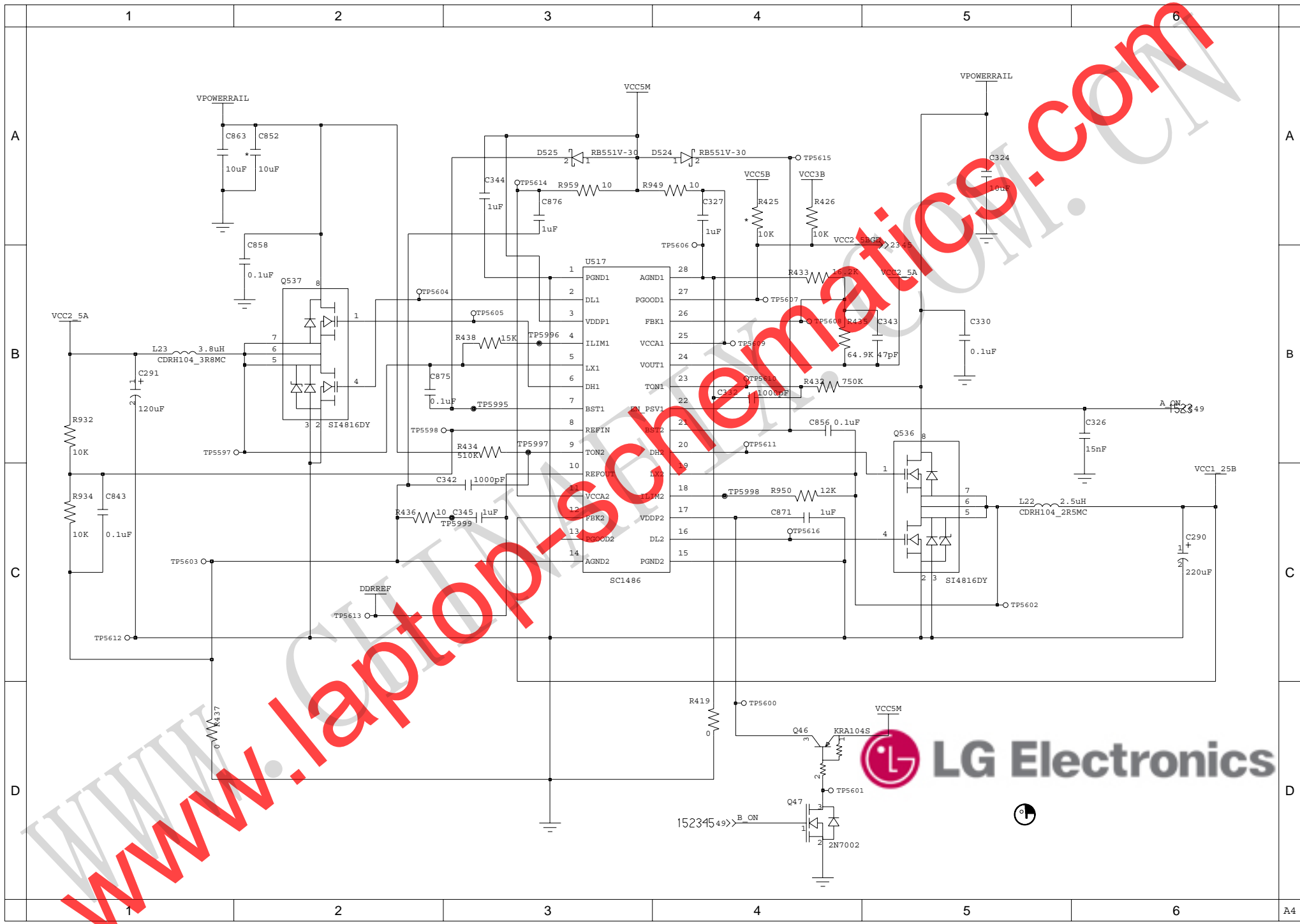


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	1	2	3	4	5	6	
A							A
B							B
C							C
D							D
	1	2	3	4	5	6	



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