Discrete/UMA Schematics Document

Sandy Bridge

Intel PCH

2011-01-19

REV : XXX

DY :None Installed
UMA:UMA platform installed
PARK:DIS PARK platform installed
MADISON:DIS MADISON platform installed
Colay :Manual modify BOM
MUX : PX

BOM

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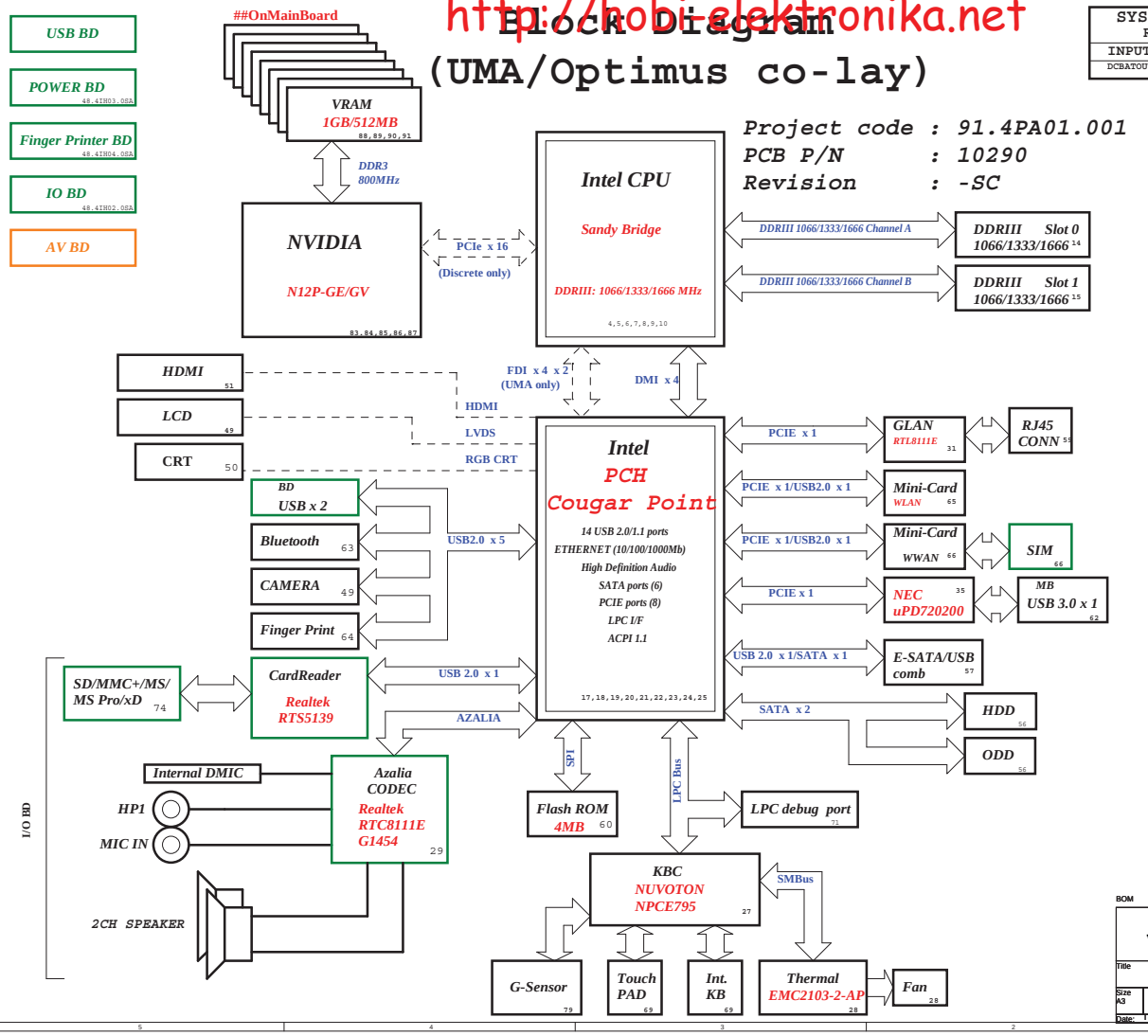
Title: Cover Page

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 1 of 102

Block Diagram (UMA/Optimus co-lay)

Project code : 91.4PA01.001
PCB P/N : 10290
Revision : -SC



SYSTEM DC/DC RT8208B 48	
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0

CPU DC/DC NCP6131 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6111CQHC 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183AQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6111C 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 DDR_VREF_S3

SYSTEM DC/DC NCP5911 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA RT8208B 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

LDO RT9025 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC G9091-180T11U 24,93	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S5
3D3V_S0	1D8V_VGA_S0

LDO RT9026 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0

PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Signal

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Title: Block Diagram

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 2 of 102

PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ ~~~~8.2 kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	 CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I2 C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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Title: Table of Content

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 3 of 102

SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

delete R404&RN 401 @20100630

62.10055.321

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Title: CPU (PCIE/DMI/FDI)		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 4 of 102	

SSID = CPU

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

20100722 SA confirm.

Connect EC to PROCHOT# through inverting OD buffer.

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

20100722 follow Astro add buffer

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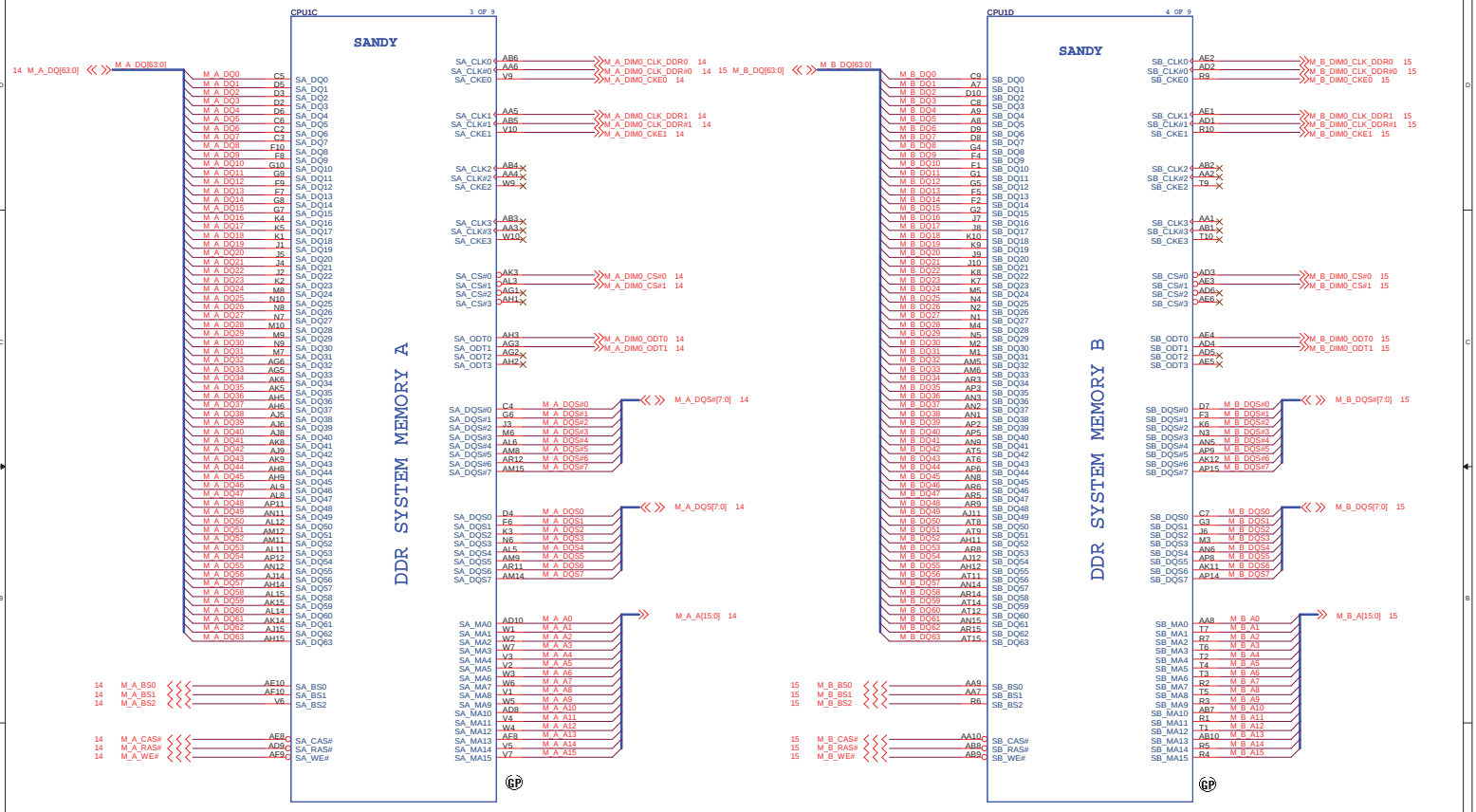
Title: CPU (THERMAL/CLOCK/PM)	
Size: A3	Document Number: LZ57
Rev: -1	
Date: Tuesday, March 29, 2011	Sheet 5 of 102

SSID = CPU



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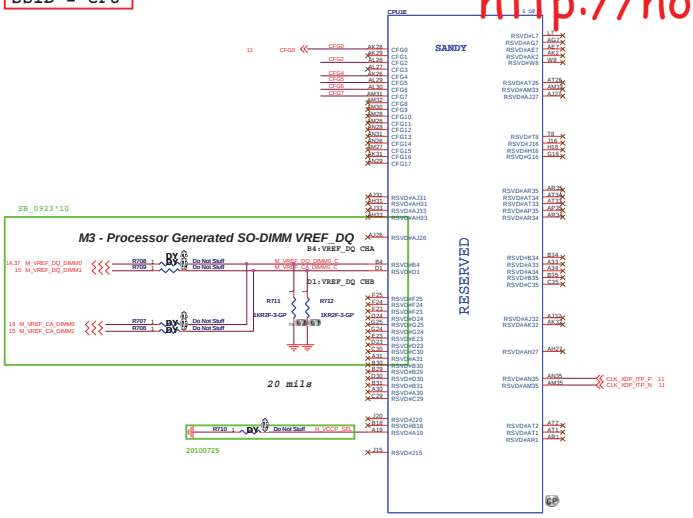
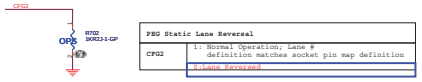
Title: CPU (DDR)

Size	Document Number	Rev
A3	LZ57	-1

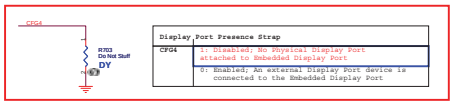
Date: Tuesday, March 29, 2011 Sheet 6 of 102

SSID = CPU

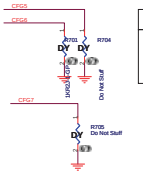




PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display_Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: CPU (RESERVED)

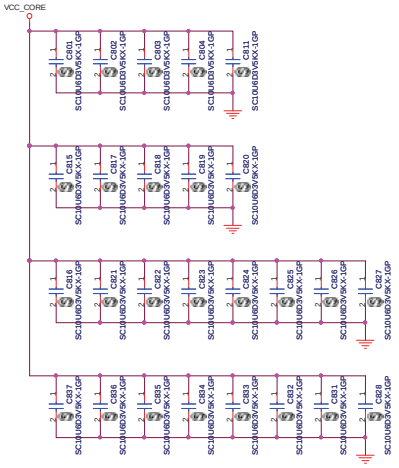
Size	Document Number	Rev
D	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 7 of 102

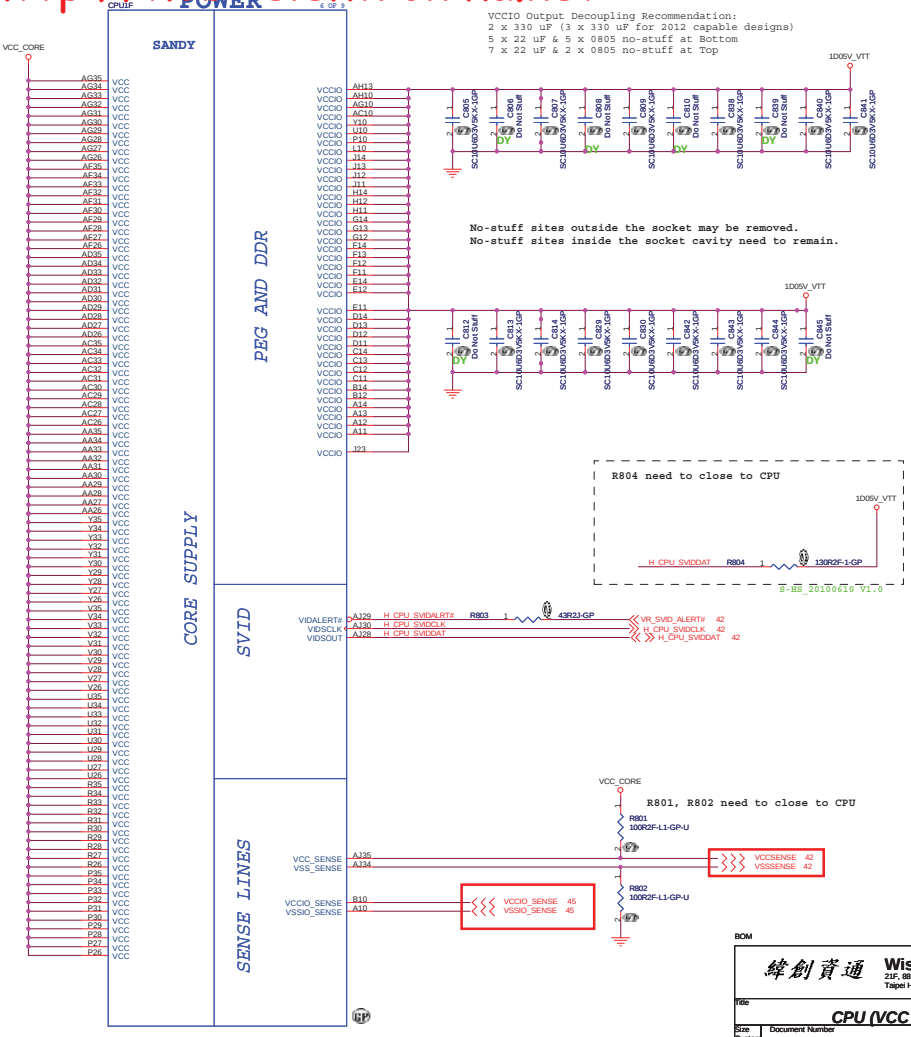
SSID = CPU

PROCESSOR CORE POWER

53A



VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity



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Title: CPU (VCC_CORE)

Size: Custom | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 8 of 102

SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

POWER

CPU1G — SANDY — GRAPHICS

SENSE LINES
VAXG_SENSE (AK35) → VCC_AXG_SENSE 42
VSSAXG_SENSE (AK34) → VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF
SM_VREF (AL1) ← +V_SM_VREF_CNT ← +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

DDR3 -1.5V RAILS
VDDQ: AE7, AF4, AF1, AC7, AC4, AC1, Y7, Y4, Y1, U7, U4, U1, P7, P4, P1

SA RAIL
VCCSA: M27, M26, L26, J26, J25, J24, H26, H25

MISC
VCCSA_SENSE (H23) → VCCSA_SENSE 48
FC_C22 (C22) → H_FC_C22 48
VCCSA_VID1 (C24) → VCCSA_SEL 48

1.8V RAIL
VCCPLL: B6, A6, A2

Close to CPU
VCC_GFXCORE
R906 100R2F-L1-GP-U
VCC_AXG_SENSE
VSS_AXG_SENSE
R907 100R2F-L1-GP-U
S-HR_20100609 V1.0

VCC_GFXCORE

PROCESSOR VAXG: 24A
C901 Do Not Stuff
C902
C903 Do Not Stuff
C904
C905
C906
C907
C908
C918
C919
C920
C921
SC10U6D3V5KX-1GP

PROCESSOR VDDQ: 10A
1D5V_DDR_S0
C909
C910
C911
C912 Do Not Stuff
C913 Do Not Stuff
C914
SC10U6D3V5KX-1GP

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

PROCESSOR VCCSA: 6A
0D85V_S0
C916 Do Not Stuff
C915
C917
TC903 ST330U2VDM-4-GP
SC10U6D3V5KX-1GP

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

0D85V_S0
R902 100R2F-L1-GP-U Notice:pull-high 100k or 10k

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

1D8V_S0
PROCESSOR VCCPLL: 1.2A
TC902 ST330U2VDM-4-GP
C923
C922
C924 Do Not Stuff
SC10U6D3V5KX-1GP

RN901 SRN1KJ-7-GP

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

20100721 standard schematic update

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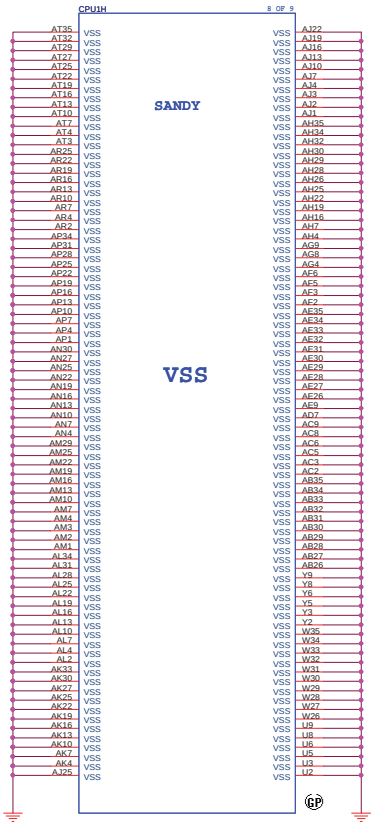
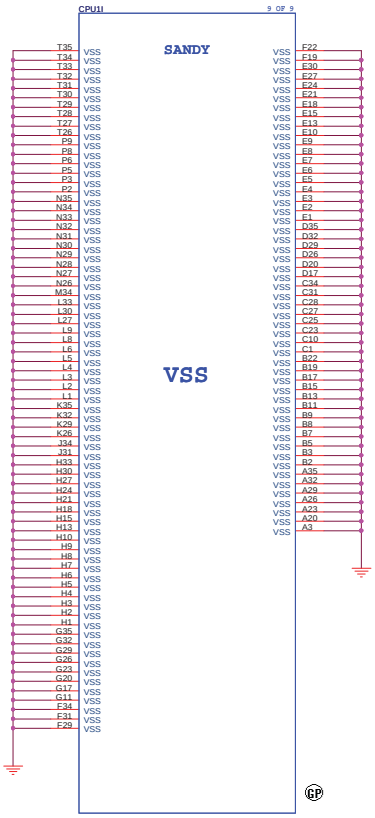
Title: CPU (VCC_GFXCORE)		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 9 of 102	

SSID = CPU





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Title: CPU (VSS)

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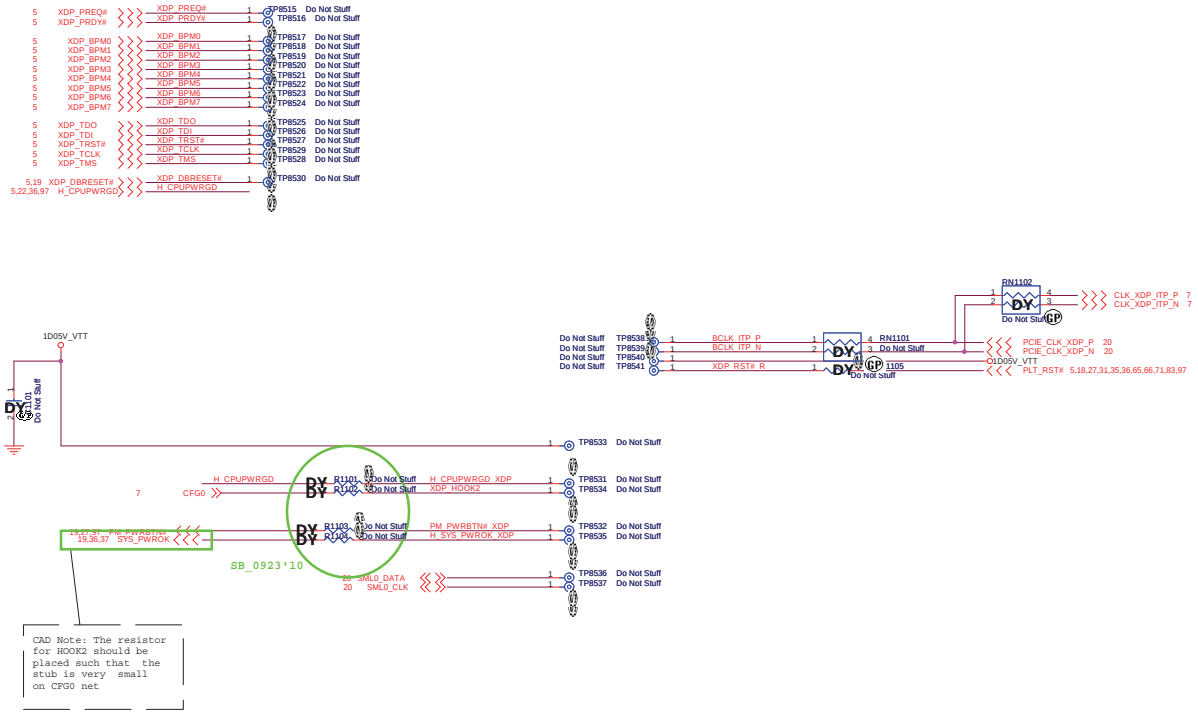
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 10 of 102



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Title: XDP		
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Title: *Reserved*

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 12 of 102

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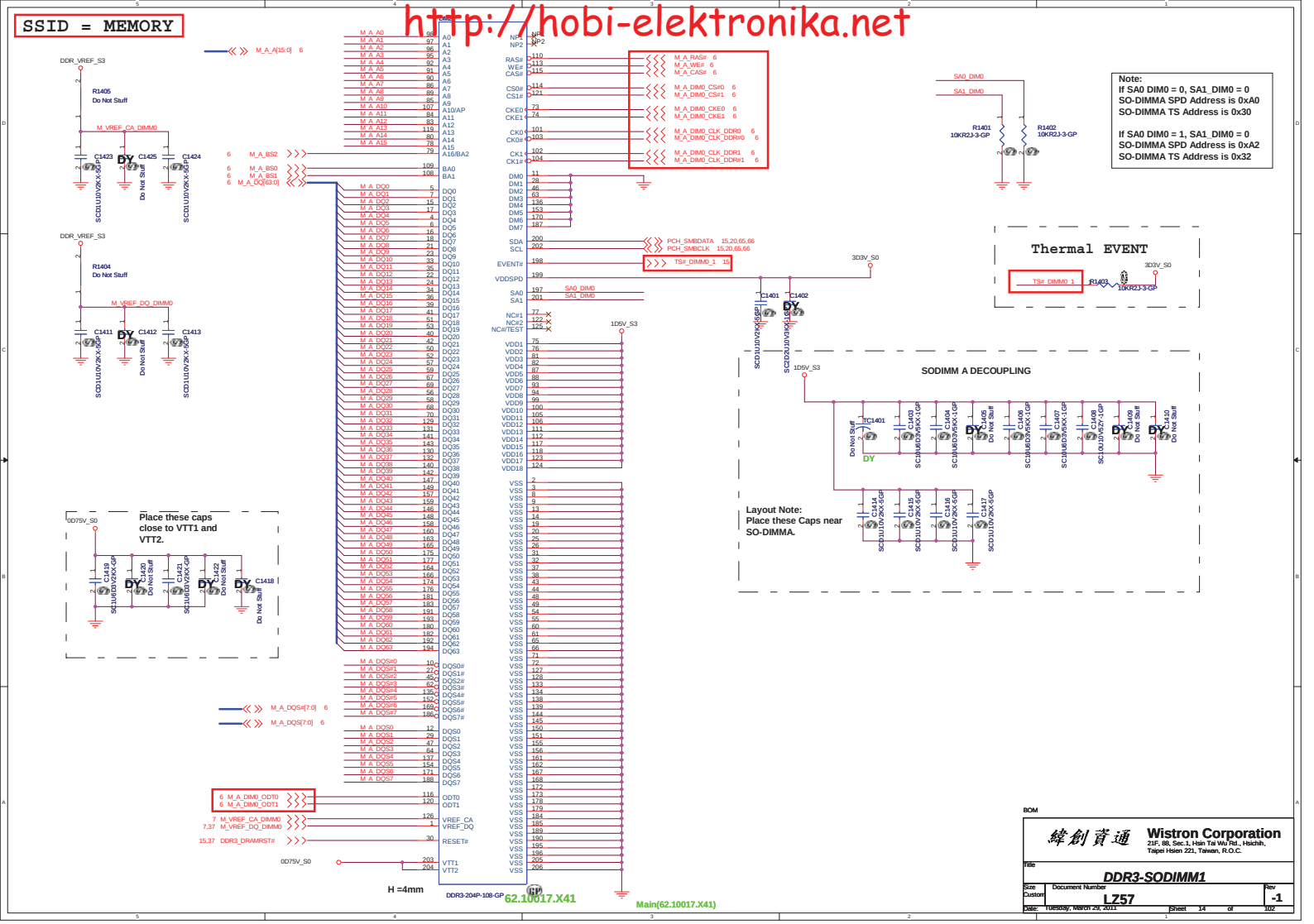
Title: *Reserved*

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 13 of 102

SSID = MEMORY



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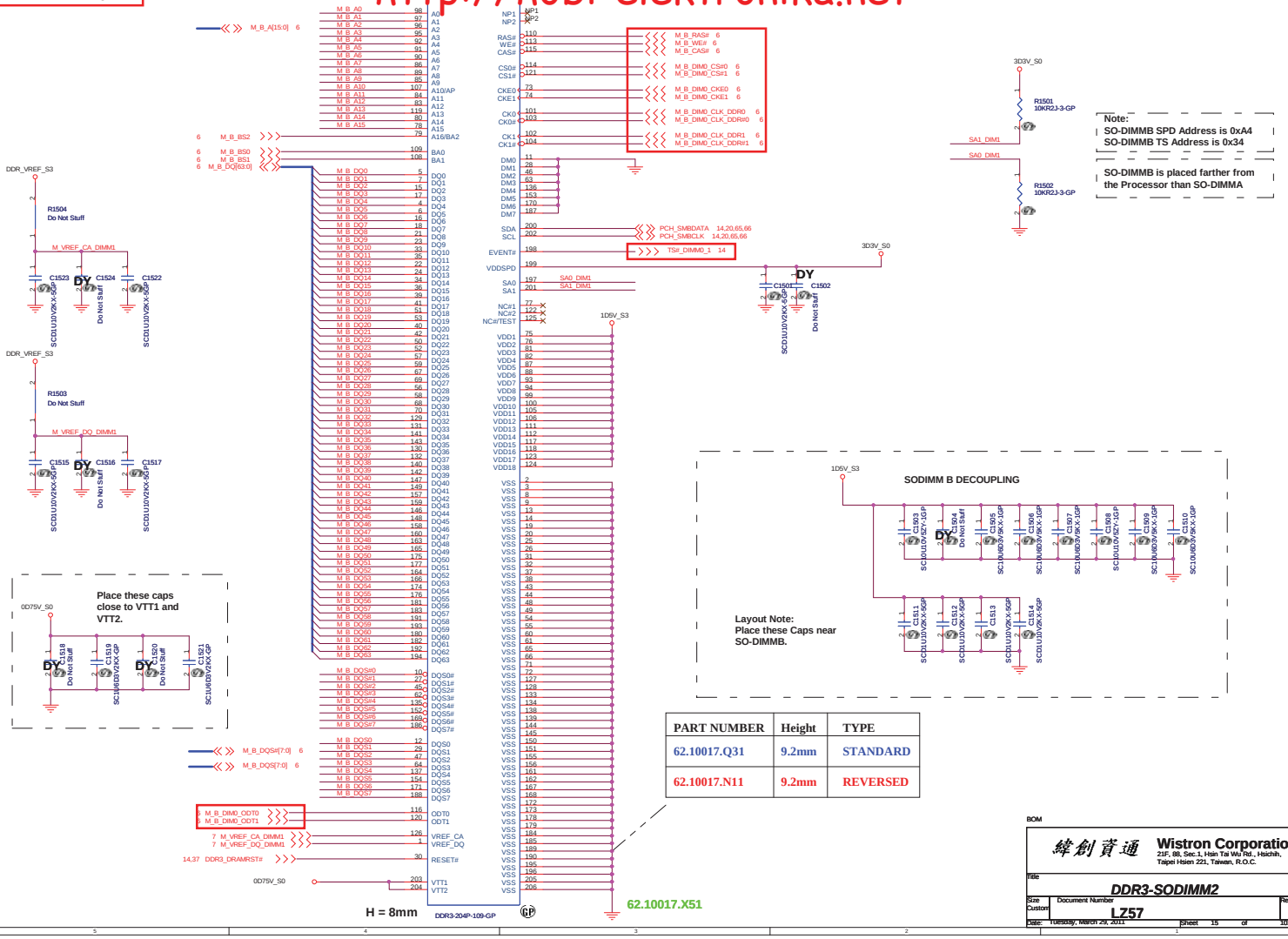
Title: **DDR3-SODIMM1**

Size	Document Number	Rev
Custom	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 14 of 102

SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

Place these caps close to VTT1 and VTT2.

Layout Note:
Place these Caps near SO-DIMMB.

PART NUMBER	Height	TYPE
62.10017.Q31	9.2mm	STANDARD
62.10017.N11	9.2mm	REVERSED

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Title: DDR3-SODIMM2

Size	Document Number	Rev
Custom	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 15 of 102

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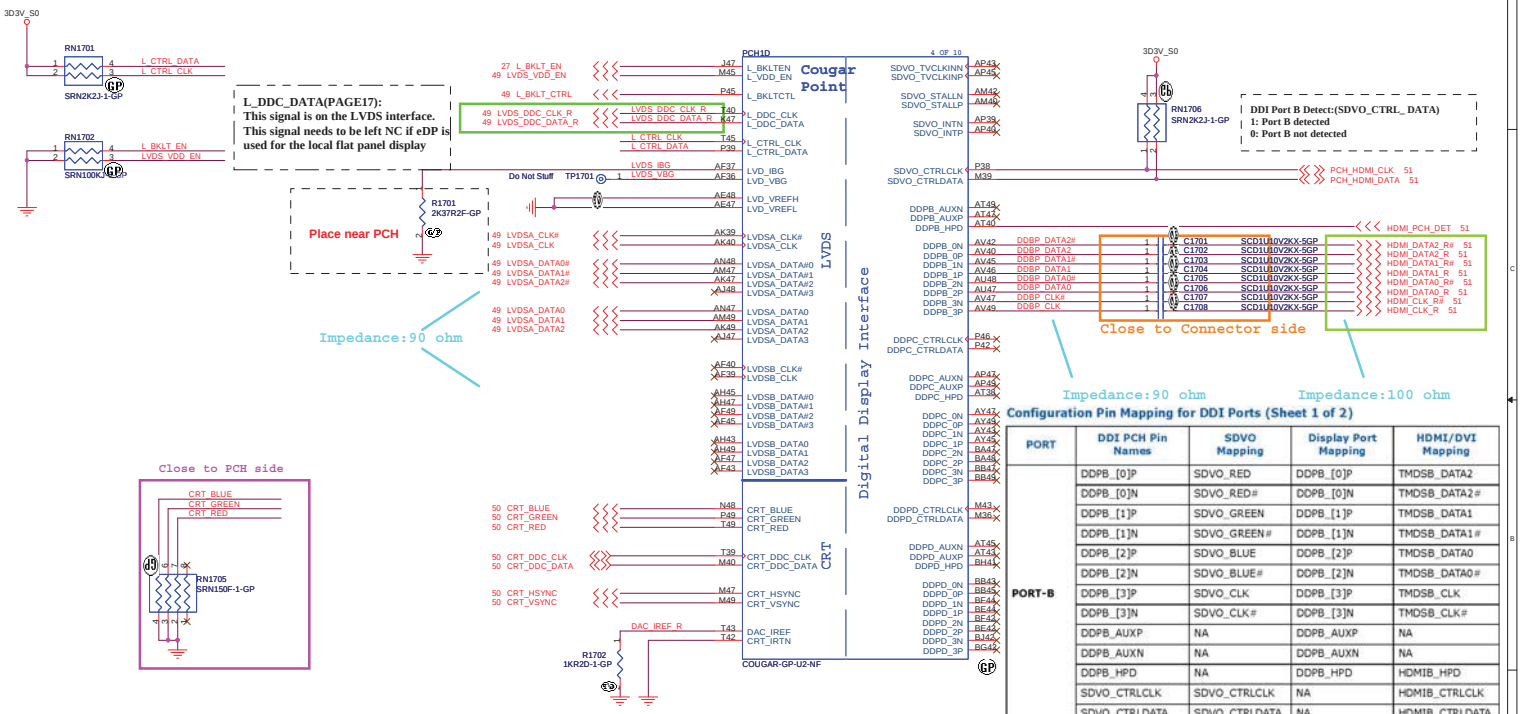
Title: DDR3-SODIMM2

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 16 of 102



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

BOM

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 17 of 102

SSID = PCH

20100725 Annie modify

CRB : 2.2K
CEKLT: 1K

DMI & PDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB Table

Pair	Device
0	X
1	USB Ext. port 1 (Left Side)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	E-SATA /USB Ext. port 4
9	USB Ext. port 2(CardReader BD
10	USB Ext. port 3(RJ45_BD)
11	Mini Card1 (WLAN)
12	CAMERA
13	X

SW programing USB_OC#12_13 for USB 9

KBC CLK EMI

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

Danbury Technology:
Disabled when Low.
Enable when High.

BOM			
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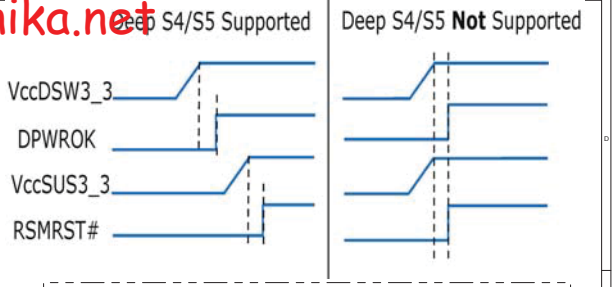
Title: PCH (PCI/USB/NVRAM)			
Size: A3	Document Number: LZ57		Rev: -1
Date: Tuesday, March 29, 2011		Sheet 18 of 102	

20100629

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

PCH1C — Cougar Point — COUGAR-GP-U2-NF

DMI: DMI0RXN/DMI1RXN/DMI2RXN/DMI3RXN, DMI0RXP/DMI1RXP/DMI2RXP/DMI3RXP, DMI0TXN/DMI1TXN/DMI2TXN/DMI3TXN, DMI0TXP/DMI1TXP/DMI2TXP/DMI3TXP

FDI: FDI_RXN0–7, FDI_RXP0–7, FDI_INT, FDI_FSYNC0, FDI_FSYNC1, FDI_LSYNC0, FDI_LSYNC1

DMI_ZCOMP — R1901 49D9R2F-GP — 1D05V_VTT
DMI_IRCOMP — R1902 750R2F-GP — RBIAS_CPY
DMI2RBIAS

System Power Management:
DSWVRMEN — DSWODVREN
DPWROK — PCH_DPWROK — R1910 0R2J-2-GP DY — R1911 Do Not Stuff — PM_RSMRST# — RTC_AUX_S5
WAKE# — PCIE_WAKE# 31,35,65,66
CLKRUN#/GPIO32 — PM_CLKRUN# 27
SUS_STAT#/GPIO61 — PM_SUS_STAT# — TP1901 Do Not Stuff
SUSCLK/GPIO62 — SUS_CLK — R1913 Do Not Stuff — PCH_SUSCLK_KBC 27
SLP_S5#/GPIO63 — PM_SLP_S5# — TP1902 Do Not Stuff
SLP_S4# — SLP_S4# R — R1914 Do Not Stuff — PM_SLP_S4# 27,46
SLP_S3# — SLP_S3# R — R1915 Do Not Stuff — PM_SLP_S3# 27,36,37,47,92
SLP_A# — PM_SLP_A# — TP1903 Do Not Stuff
SLP_SUS# — PM_SLP_SUS# — TP1904 Do Not Stuff
PMSYNCH — H_PM_SYNC — H_PM_SYNC 5
SLP_LAN#/GPIO29 — PM_SLP_LAN# — TP1905 Do Not Stuff

SUSACK# — R1903 Do Not Stuff — SUS_PWR_ACK — SUSACK# C12
SYS_RESET# — R1902 Do Not Stuff — 5,11 XDP_DBRESET# — SYS_RESET# K3
SYS_PWROK — R1905 10KR2J-3-GP — R1923 Do Not Stuff — 3D3V_S0 — 11,36,37 SYS_PWROK — SYS_PWROK P12
PWROK — R1924 0R2J-2-GP — 27,36 S0_PWR_GOOD — PWROK L22
APWROK — R1906 0R2J-2-GP — R1907 Do Not Stuff — MEPWROK — 36,37,45,46,47 RUNPWROK — APWROK L10
DRAMPWROK — 5,37 PM_DRAM_PWRGD — DRAMPWROK B13
RSMRST# — PM_RSMRST# — RSMRST# C21
SUSWARN#/SUSPWRDNACK/GPIO30 — 20,27 SUS_PWR_ACK — SUSWARN#/SUSPWRDNACK/GPIO30 K16
PWRBTN# — 11,27,97 PM_PWRBTN# — PWRBTN# E20
ACPRESENT/GPIO31 — 27 AC_PRESENT — ACPRESENT/GPIO31 H20
BATLOW#/GPIO72 — 20 BATLOW# — BATLOW#/GPIO72 E10
RI# — PM_RI# — RI# A10

R1926 SYS_PWROK — R1904 PWROK — 100KR2J-1-GP DY Do Not Stuff

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

DSWODVREN - On Die DSW VR Enable

HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5 — R1917 330KR2J-L1-GP — DSWODVREN — R1918 DY Do Not Stuff

3D3V_S0 — PM_CLKRUN# — R1919 8K2R2J-3-GP

3D3V_S5 — RN1901 SRN10KJ-6-GP — PCIE_CLK_LAN_RQ1# — AC_PRESENT — PM_RI# — PCIE_CLK_LAN_RQ1# 20,31

R1921 10KR2J-3-GP — PCIE_WAKE# — DY

R1922 10KR2J-3-GP — PM_PWRBTN# — R1926 10KR2J-3-GP — PM_SLP_LAN# — DY Do Not Stuff

20100729

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PWRBTN#
This signal has an internal pull-up resistor

R1908 — PM_RSMRST# — 10KR2J-3-GP

3D3V_AUX_S5 — R1909 10KR2J-1-GP — R1916 10KR2J-3-GP — Q1901 2N7002KDW-GP — R1912 1KR2J-1-GP — PM_RSMRST# — RSMRST#_KBC 27 — 3V_5V_POK # — 3V_5V_POK 41

84.2N702.A3F
2nd = 84.DM601.03F

BOM

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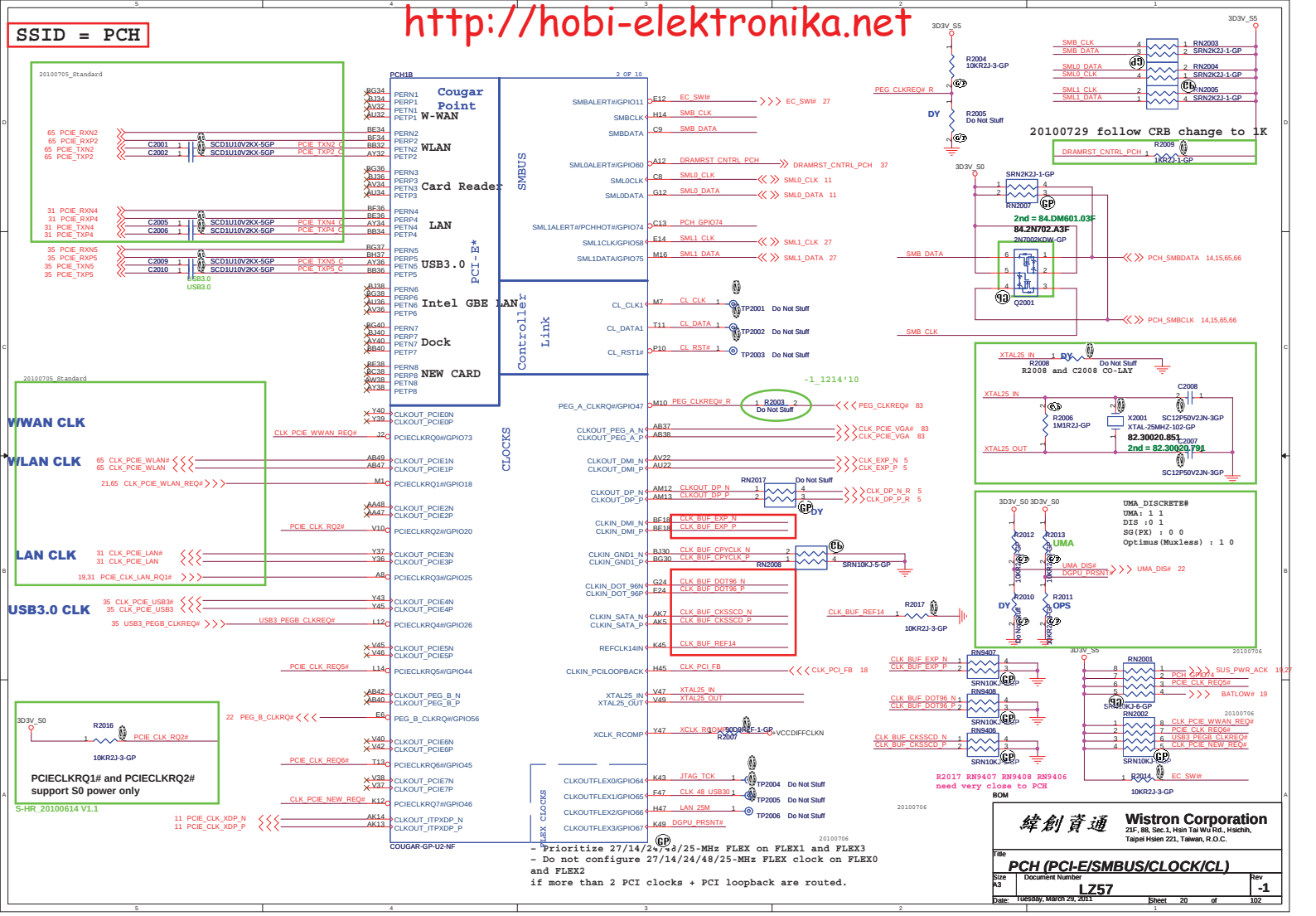
Title: **PCH (DM I/FDI/PM)**
Size: A3 | Document Number: LZ57 | Rev: -1
Date: Tuesday, March 29, 2011 | Sheet 19 of 102

SSID = PCH



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Title	PCH (PCI-E/SMBUS/CLOCK/CL)
Size A3	Document Number LZ57 Rev -1
Date: Tuesday, March 29, 2011	Sheet 20 of 102

SSID = PCH

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

NO REBOOT STRAP

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

20100629 SA

Move Cap close to Connector.

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Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 21 of 102

SSID = PCH

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

Note:
For PCH debug with XDP, need to NO STUFF R2218

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

20100720 SW

SB 0923'10

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

20100729 follow Annie CRB

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

[VRAM_SIZE1:VRAM_SIZE2]
LL=512M / HL=1G / LH=2G

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

BOM

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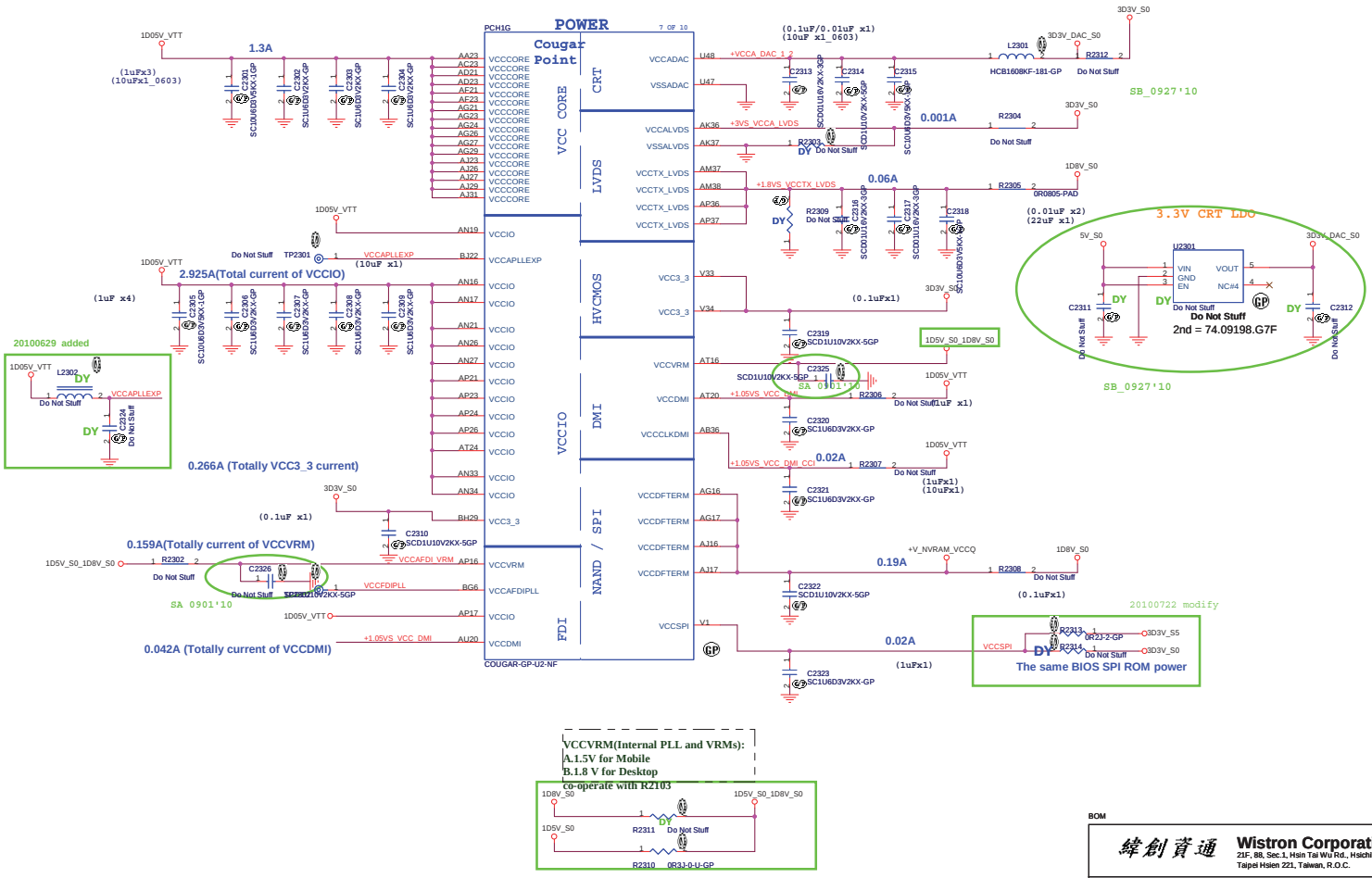
Title: PCH (GPIO/CPU)

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 22 of 102

SSID = PCH 6A



VCCVRM(Internal PLL and VRMs):
A.1.5V for Mobile
B.1.8 V for Desktop
co-operate with RZ103

BOM

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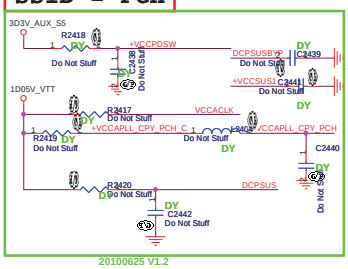
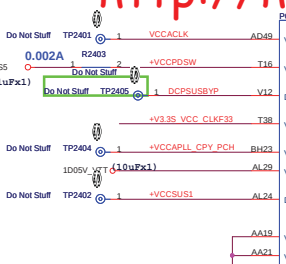
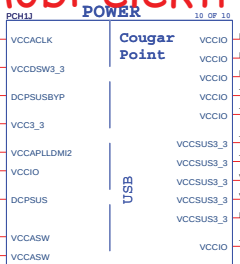
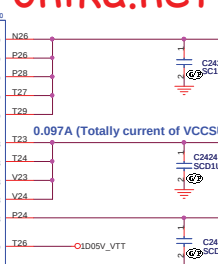
Title: PCH (POWER1)		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 23 of 102	

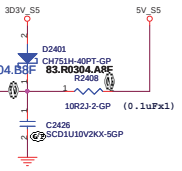
SSID = PCH

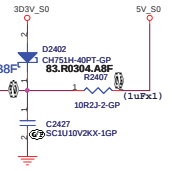


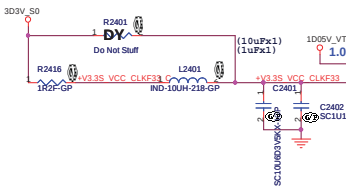


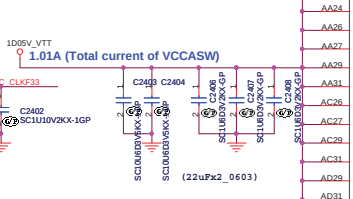


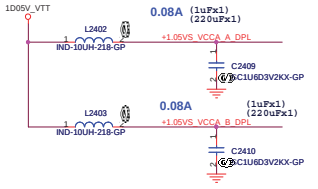


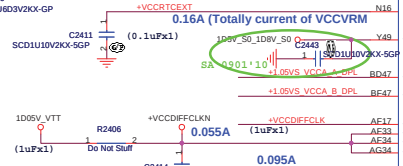


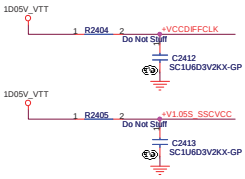


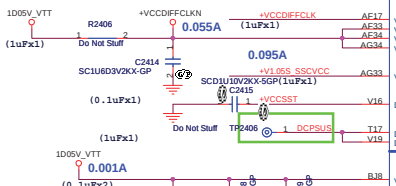


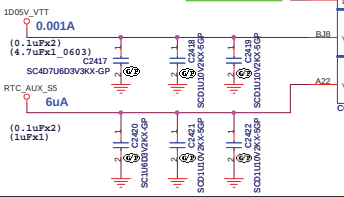


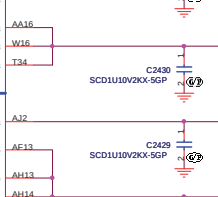


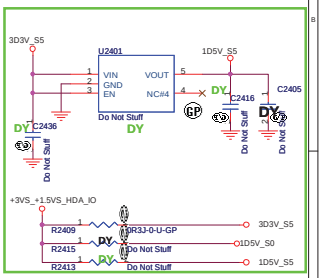












BOM

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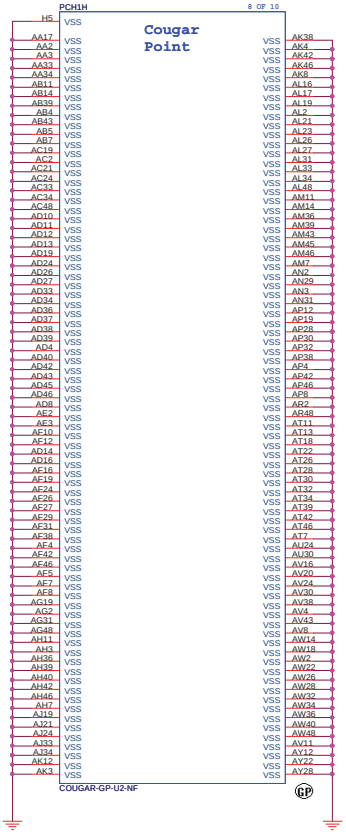
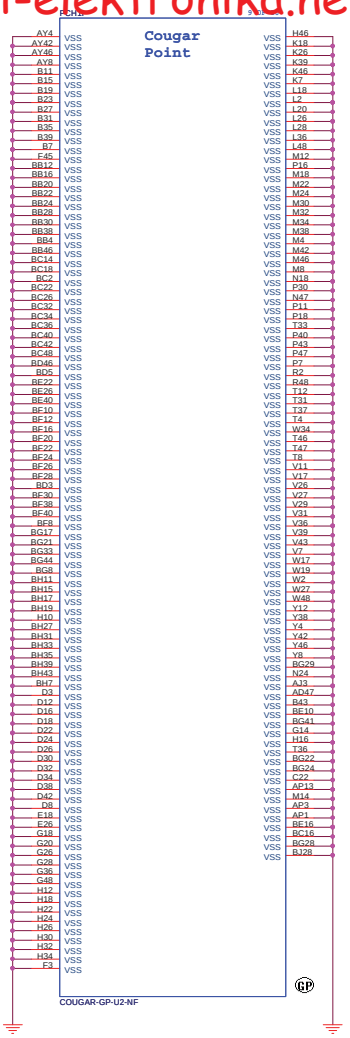
Title: **PCH (POWER2)**

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 24 of 102

SSID = PCH





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Title: PCH (VSS)

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 25 of 102

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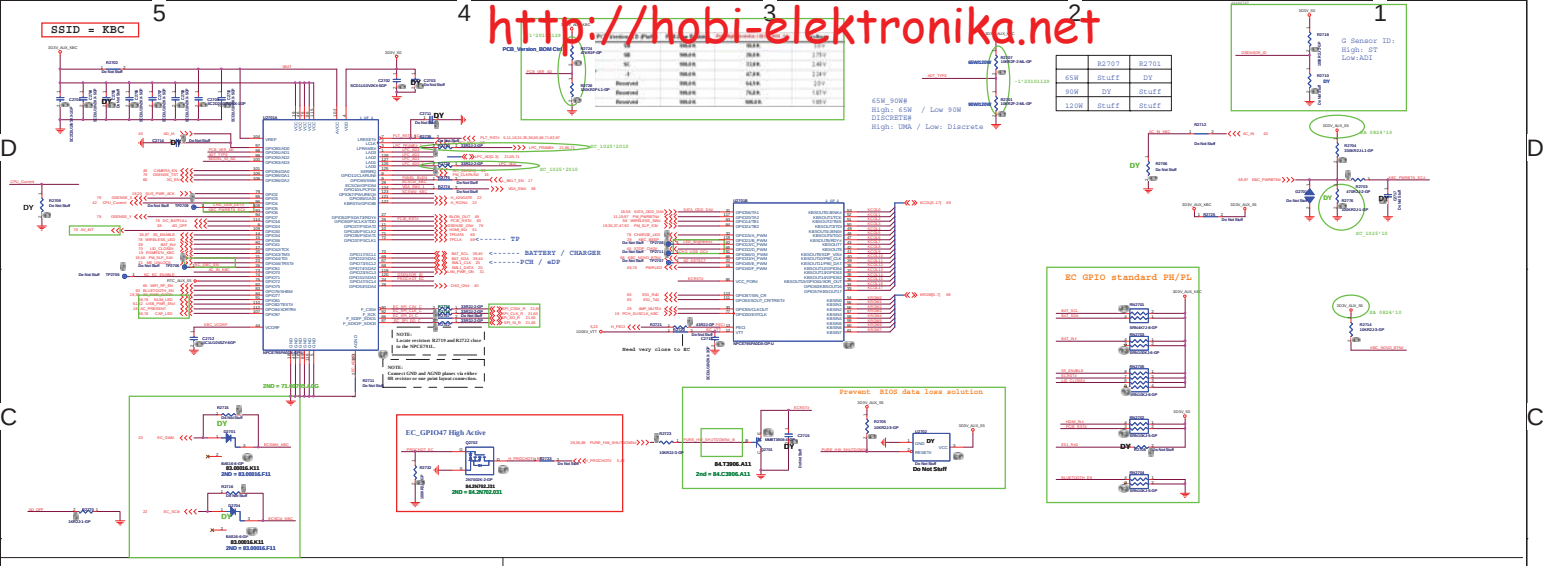
Title: *Reserved*

Size	Document Number	Rev
A4	LZ57	-1

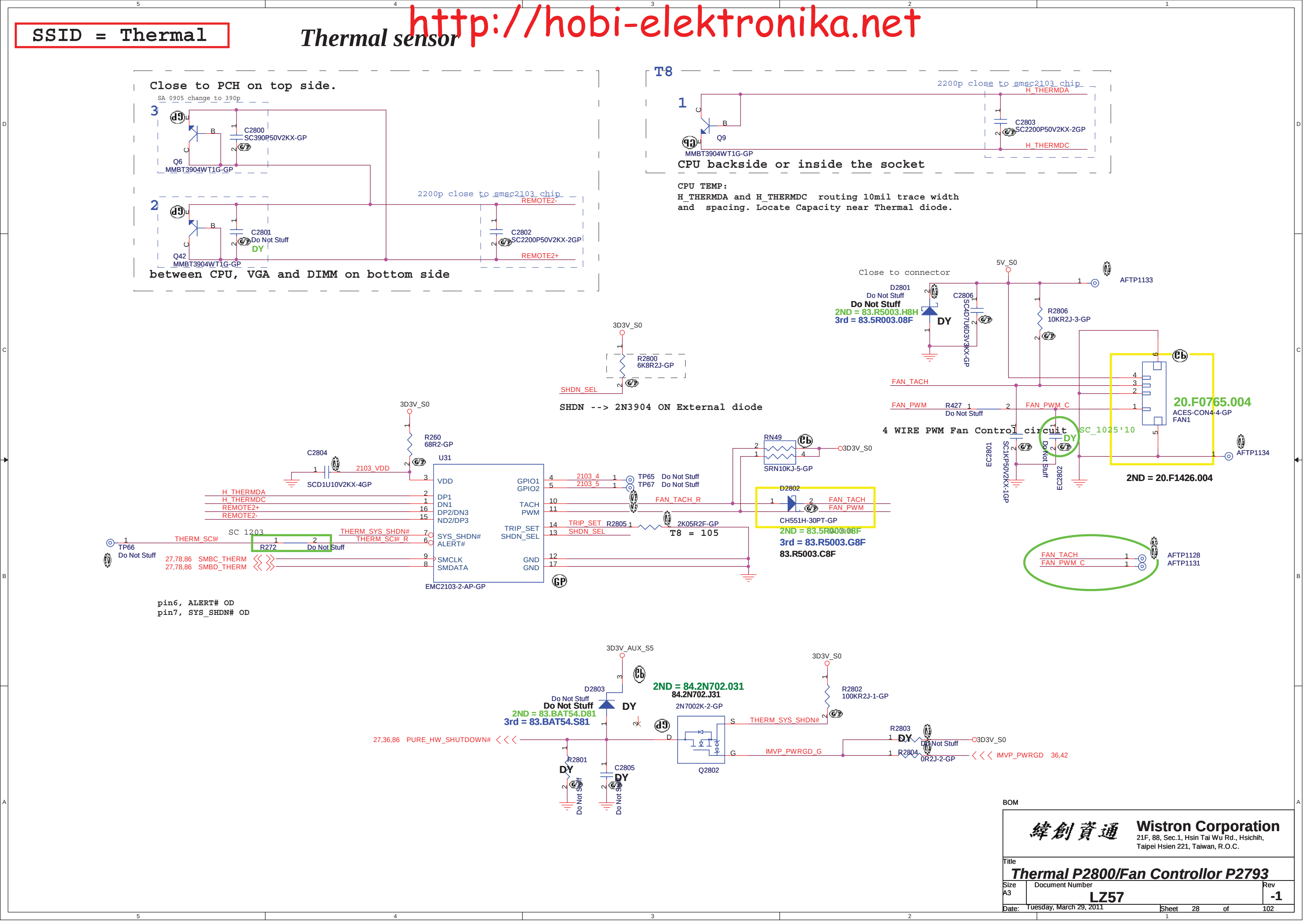
Date: Tuesday, March 29, 2011 Sheet 26 of 102



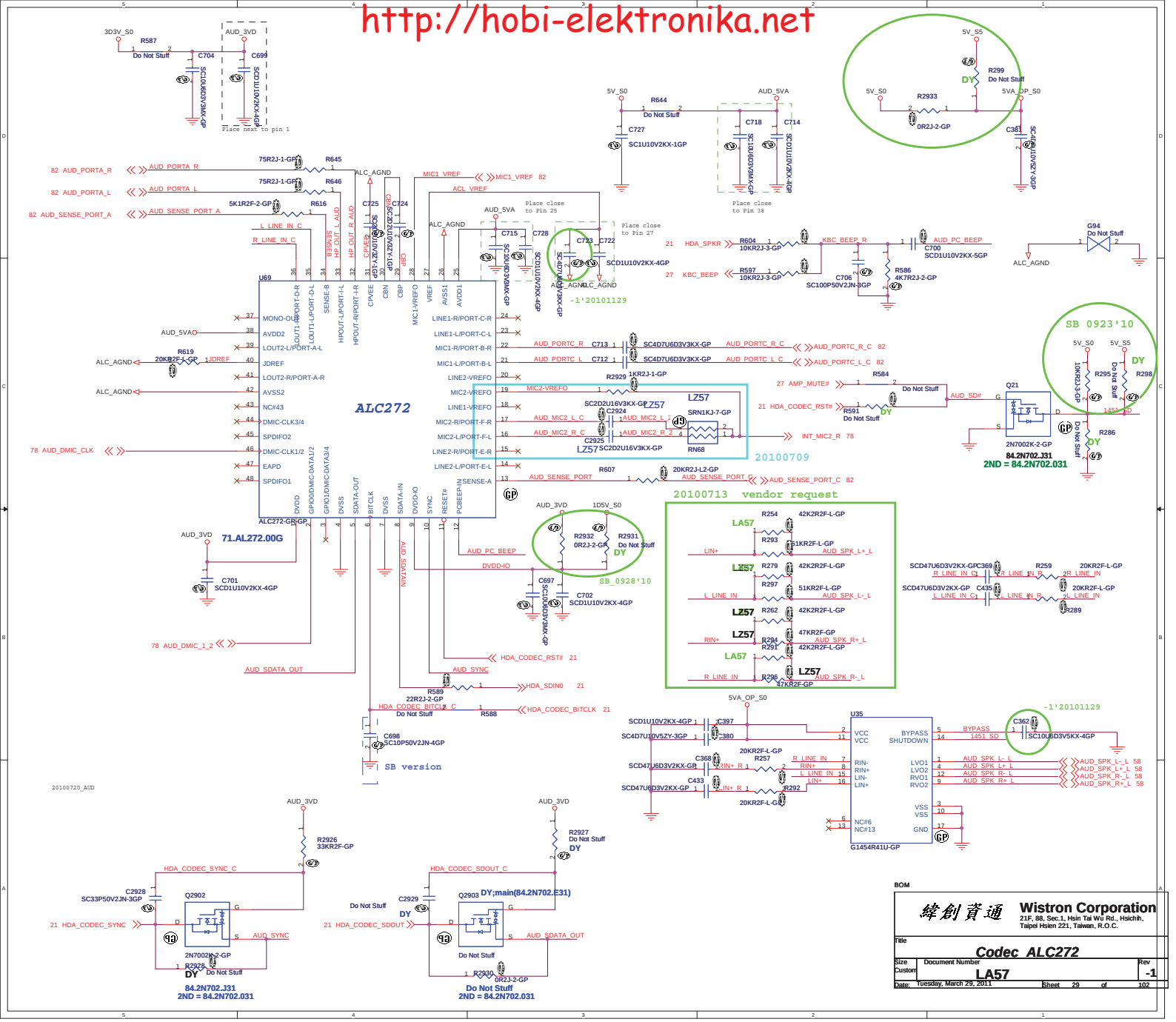
	R2707	R2701
65W	Stuff	DY
90W	DY	Stuff
120W	Stuff	Stuff

MODEL_ID_AD(Pin100)	Full-Low Register	Full-High Register	Voltage
V/W 57 UMA	100.0 K	64.9 K	2.001 V
V/W 57 OPTIMUS	100.0 K	76.8 K	1.867 V
Z 57 UMA	100.0 K	100.0 K	1.650 V
Z 57 OPTIMUS	100.0 K	143.0 K(64.14335.L01)	1.32 V

Wistron Corporation
KBC Nuvoton NPCE795
L757



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: Thermal P2800/Fan Controllor P2793
Size A3 Document Number LZ57 Rev -1
Date: Tuesday, March 29, 2011 Sheet 28 of 102



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BOM

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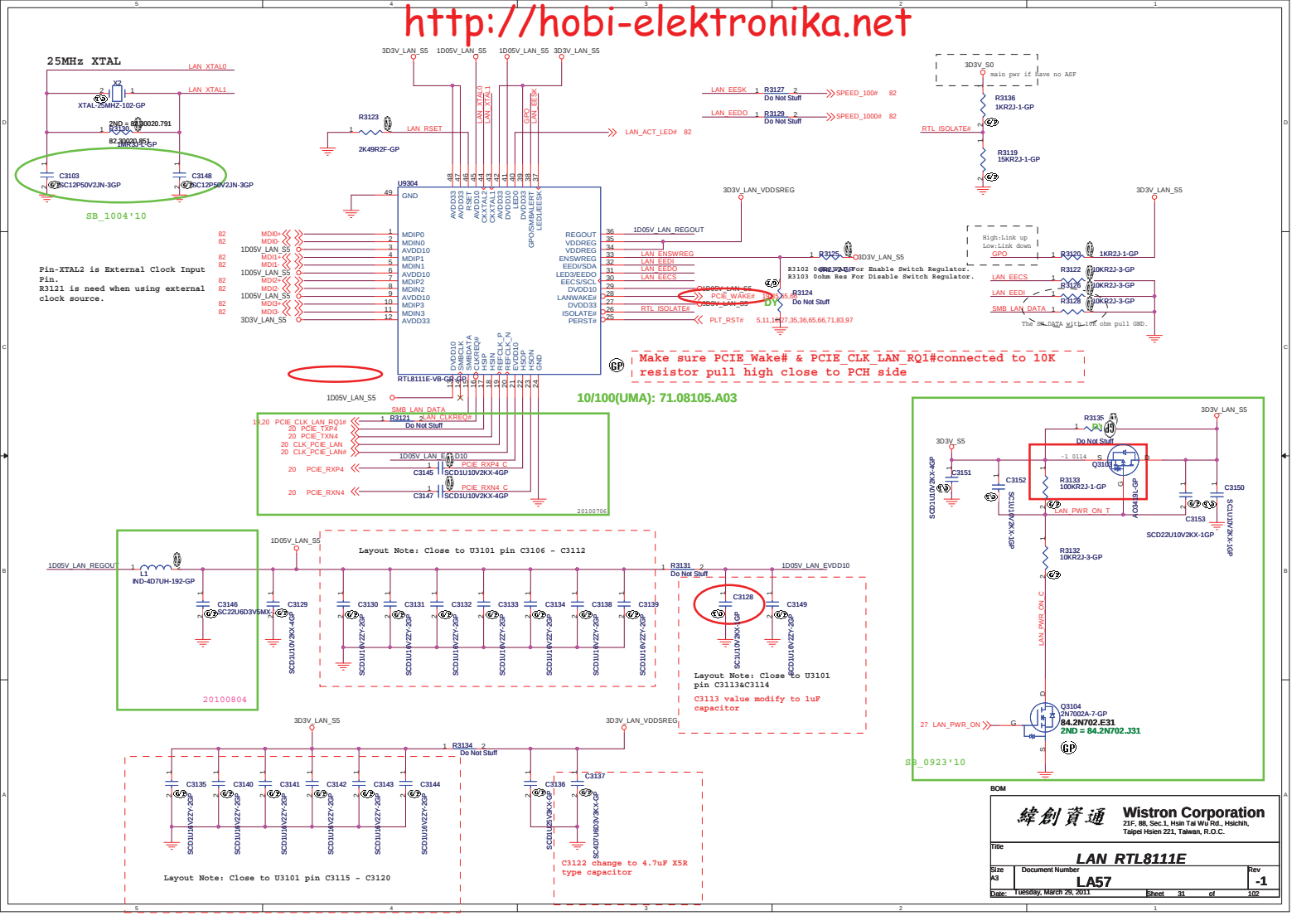
Taipei Hsien 221, Taiwan, R.O.C.

Title: reserved

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 30 of 102



BOM

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RTS5159 (CARD READER)

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 32 of 102

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BOM

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 33 of 102

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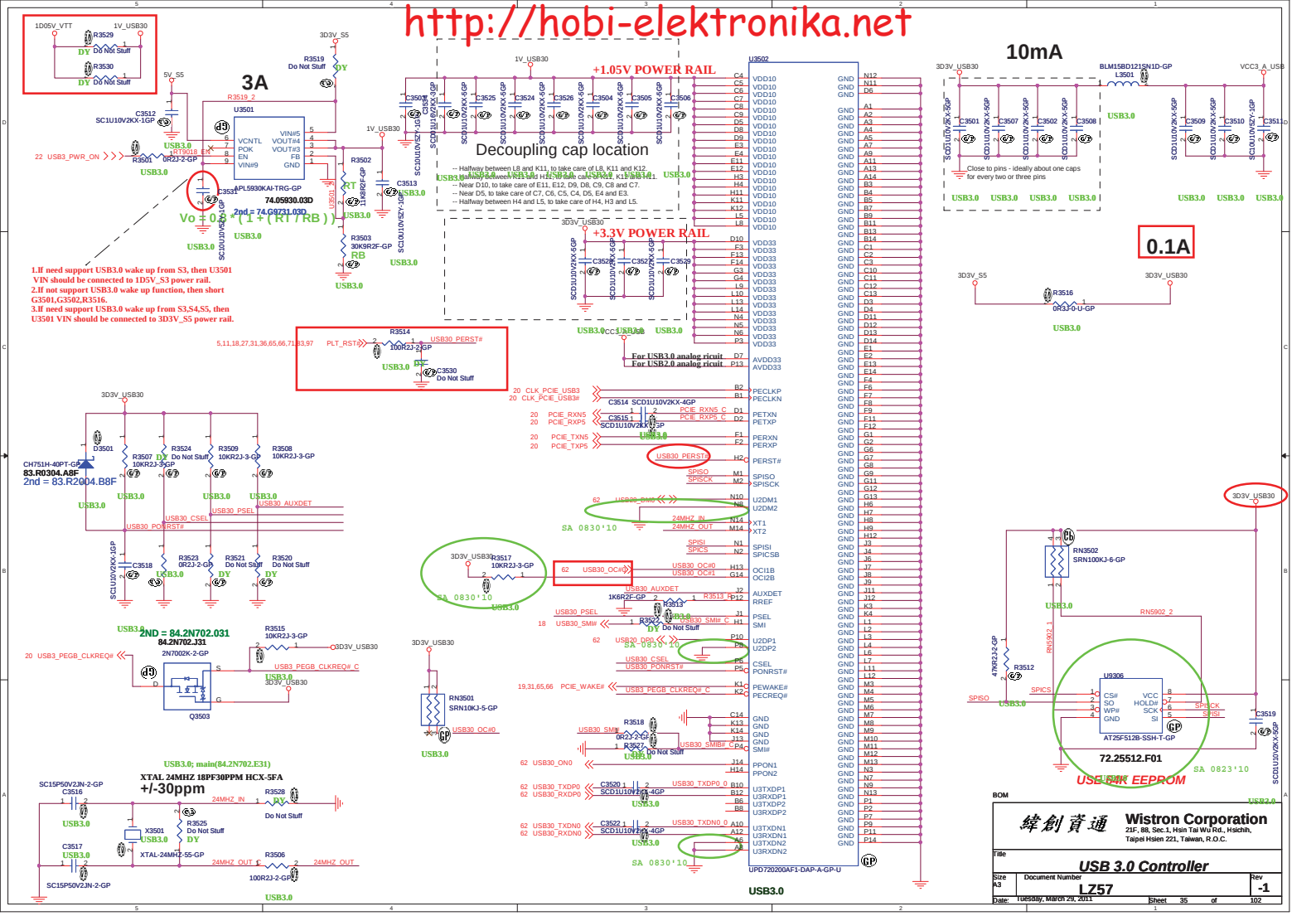
Taipei Hsien 221, Taiwan, R.O.C.

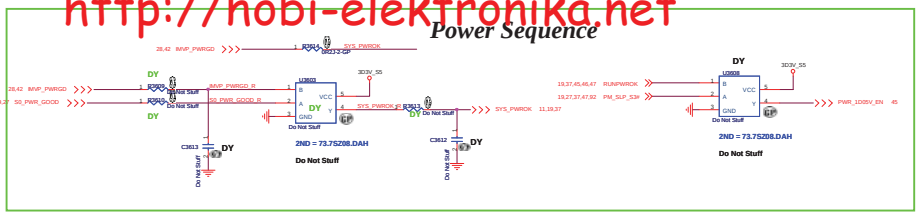
Title: *Reserved*

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 34 of 102

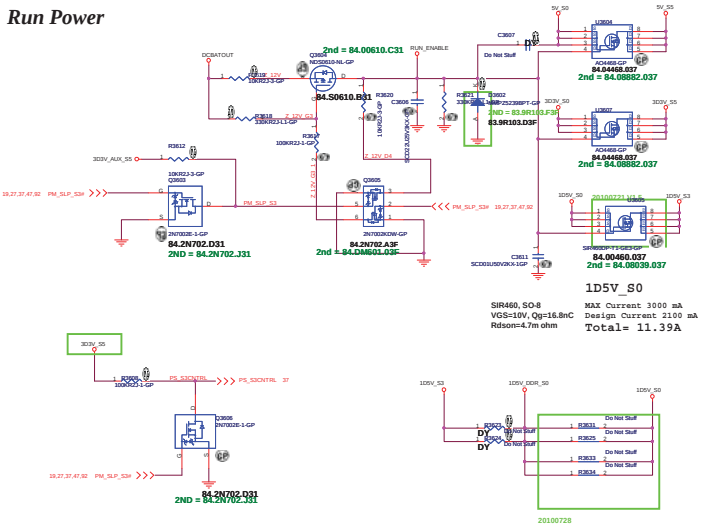


Power Sequence

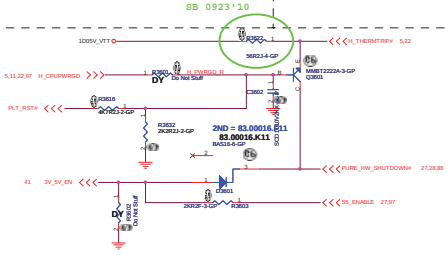


SSID = Reset.Suspend

Run Power



SB 0923'10



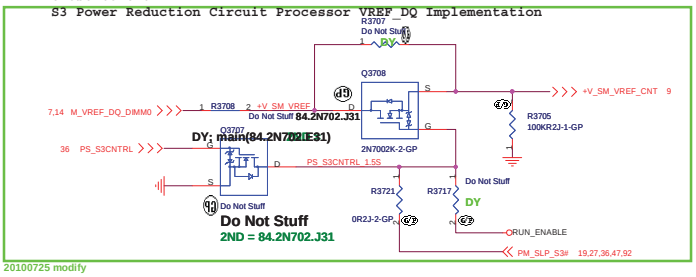
BOM

蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

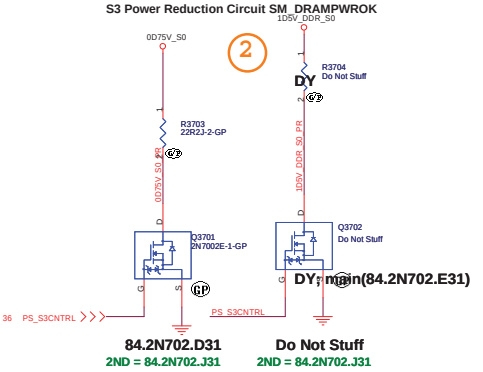
Size	Document Number	Rev
A2	LZ57	-1
Date: Tuesday, March 29, 2011	Sheet 38 of 102	

Close to CPU
S3 Power Reduction Circuit Processor VREF DQ Implementation

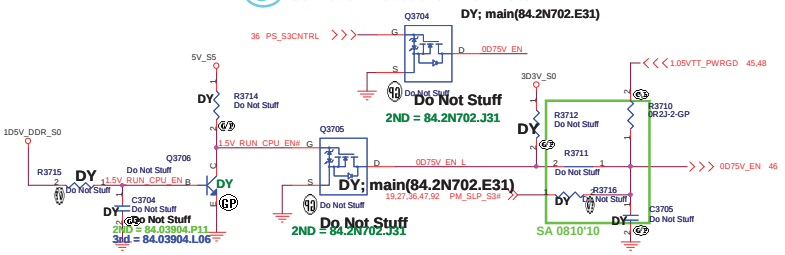


20100725 modify

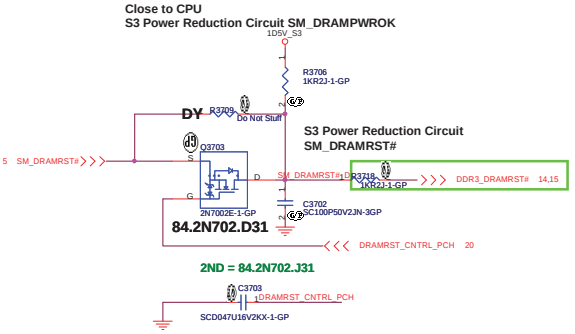
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



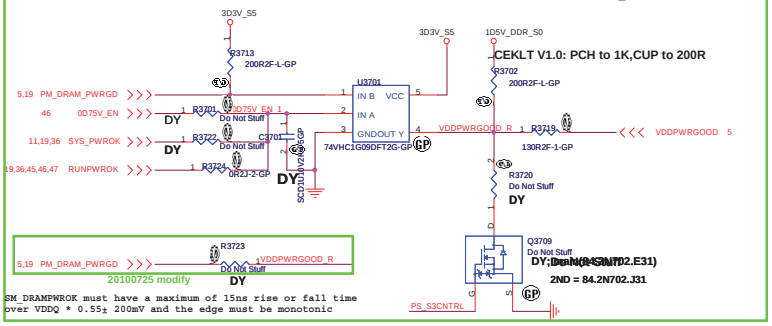
5 S3 Power Reduction X01 20091111



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



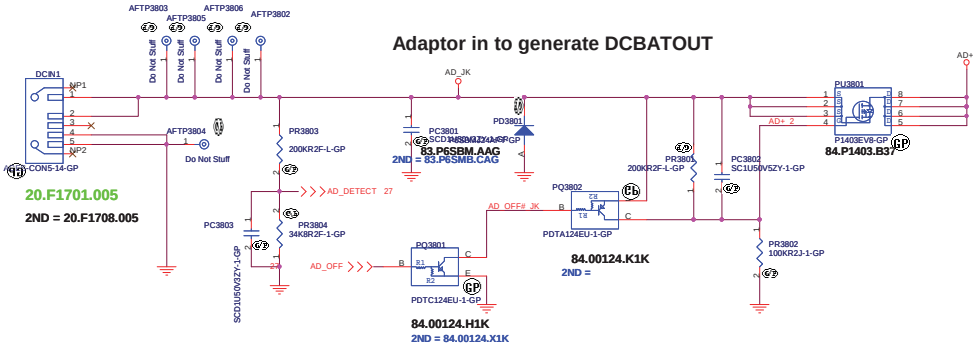
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



BOM

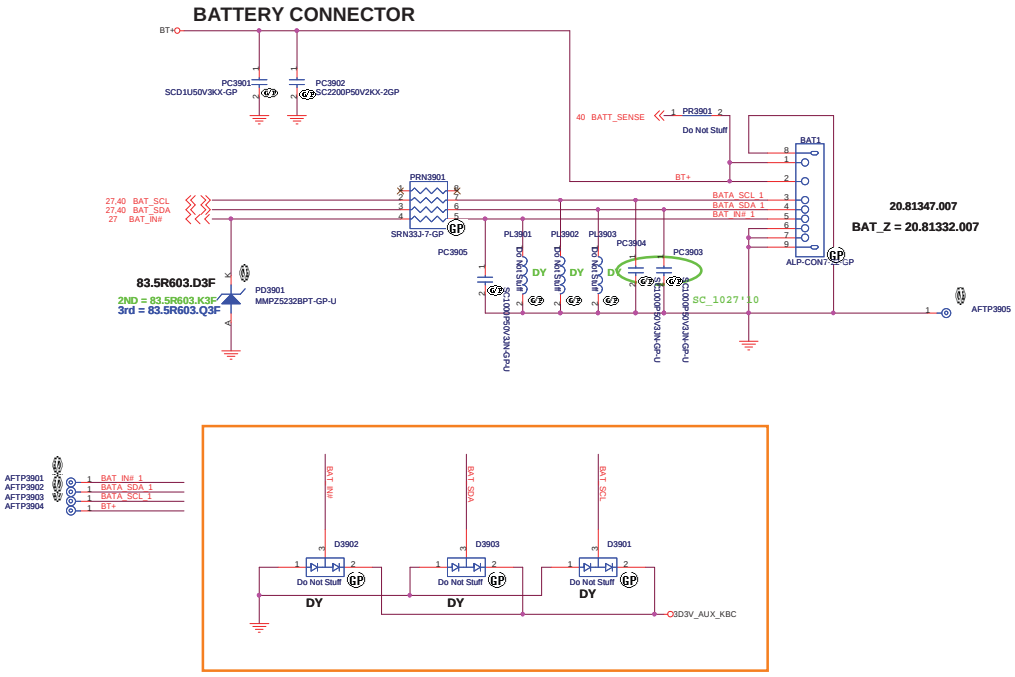
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ADAPTER		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 37 of 102	

Adaptor in to generate DCBATOUT



BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DCIN_JACK		
Size	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 38 of 102	



BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	BATT_CONN	
Size	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 39 of 102	

AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k (64.18735.6DL)	49.9k	80w	137k	49.9k
90w	121k (64.12135.6DL)	49.9k	120w	76.8k (64.76825.6DL)	49.9k

NEAR

20100518 WAYNE

STOP_CHG# connects to KBC

SC_1026'10

79.10712.L02

SC_1028'10

20100518 WAYNE

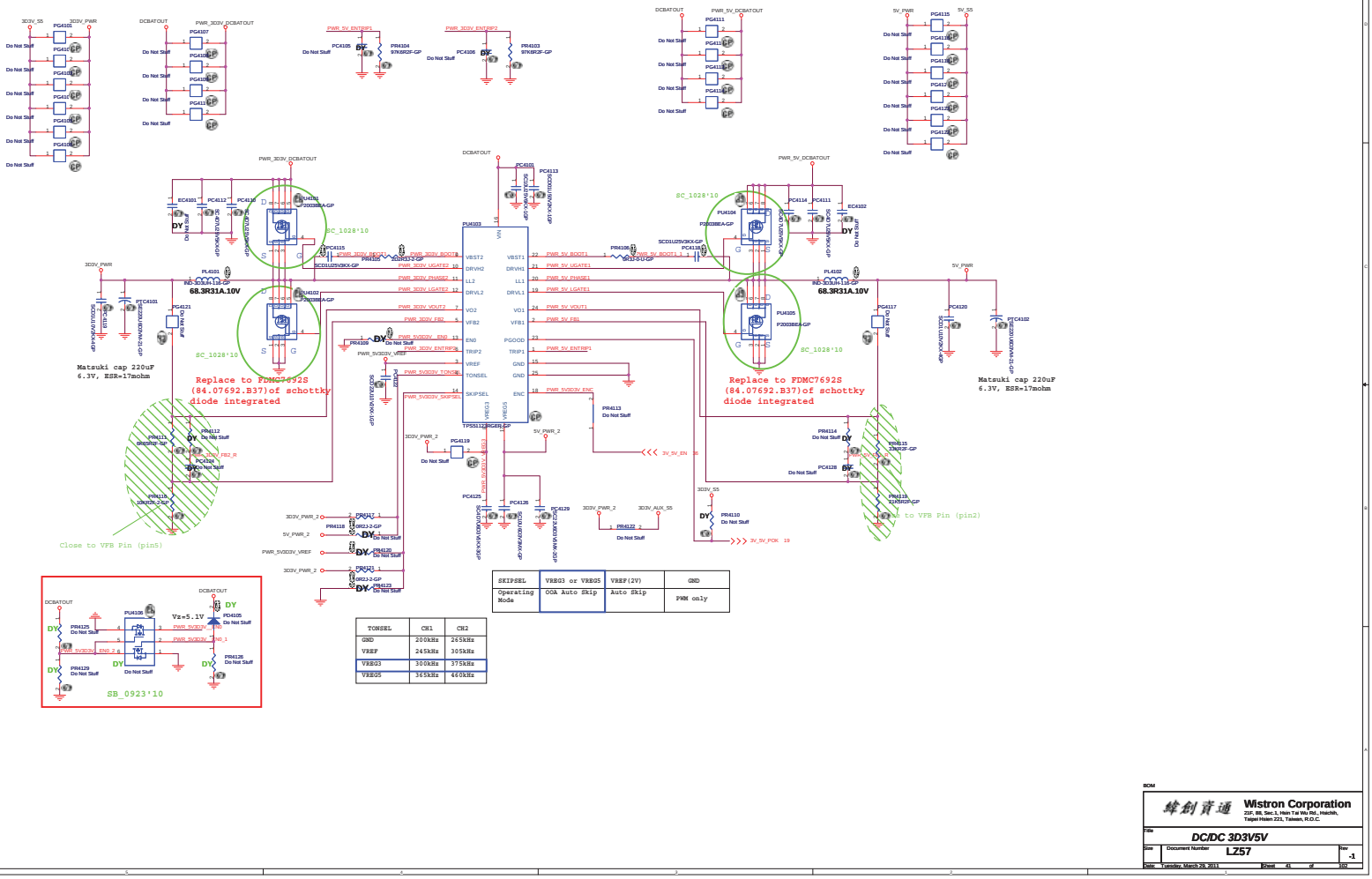
BOM_CTRL

2ND = 84.2N702.031

AC_IN to KBC

Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: Charger_BQ24745	
Size:	Document Number: LZ57 Rev: -1
Date: Tuesday, March 29, 2011	Sheet 40 of 102

SSID = PWR.Plane.Regulator_5v3p3v



TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

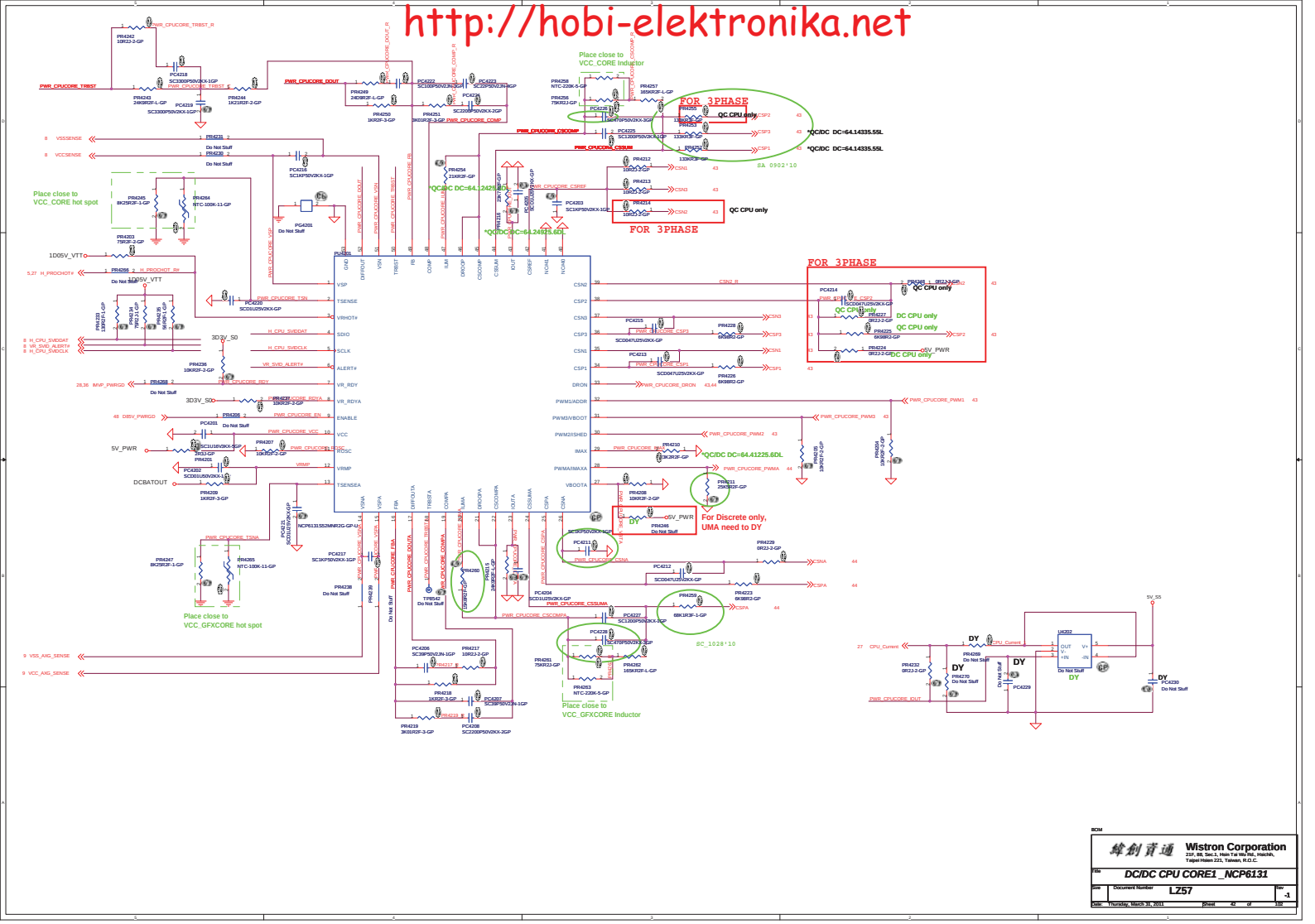
BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

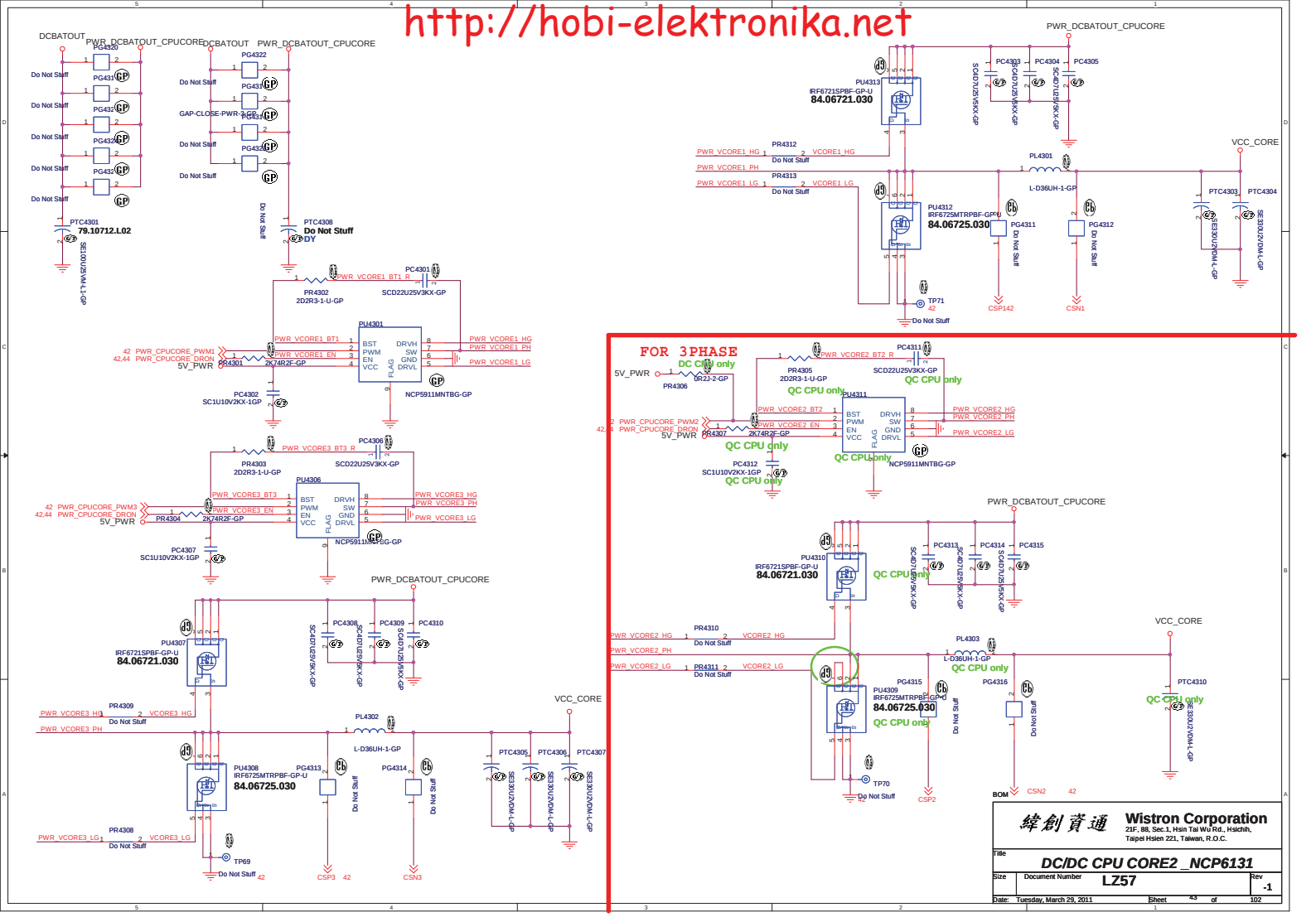
Title: DC/DC 3D3V5V

Size	Document Number	Rev
	LZ57	-1

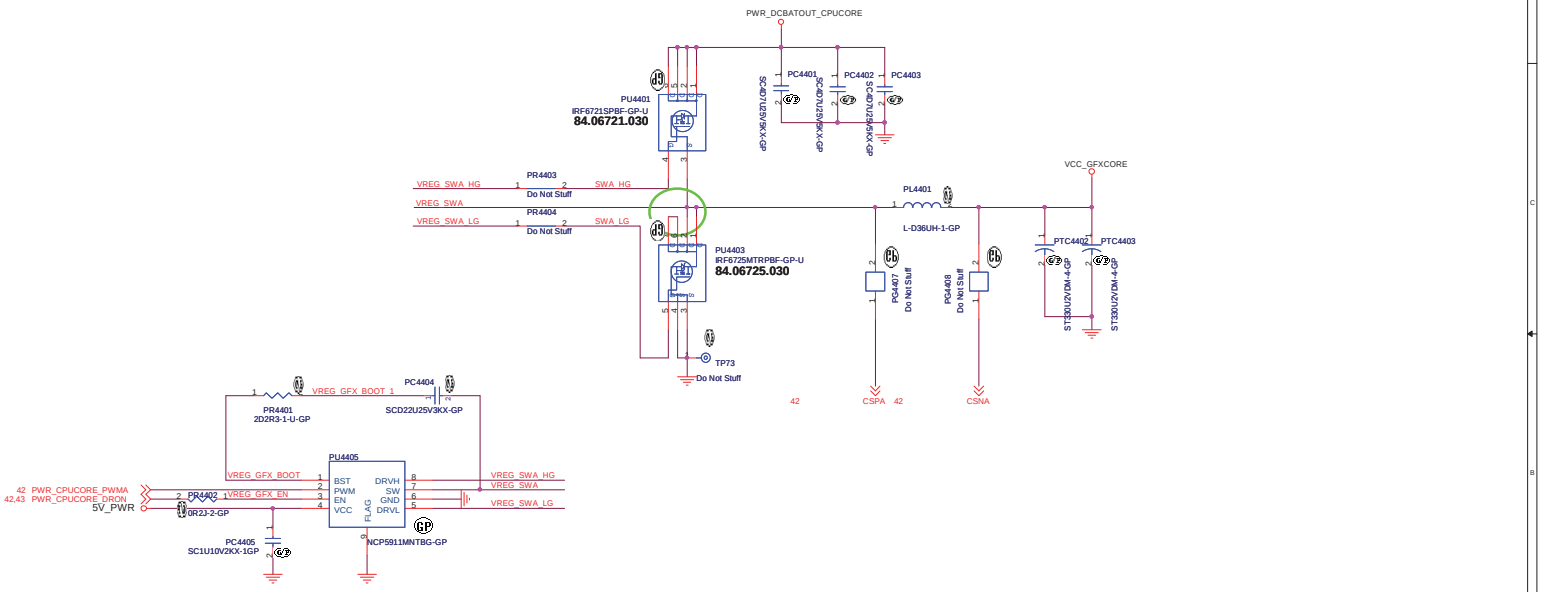
Date: Tuesday, March 29, 2011 Sheet 41 of 102



BOM	
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DC/DC CPU CORE1_NCP6131
Size	Document Number: LZ57
Rev	-1
Date: Thursday, March 31, 2011	Sheet 42 of 102

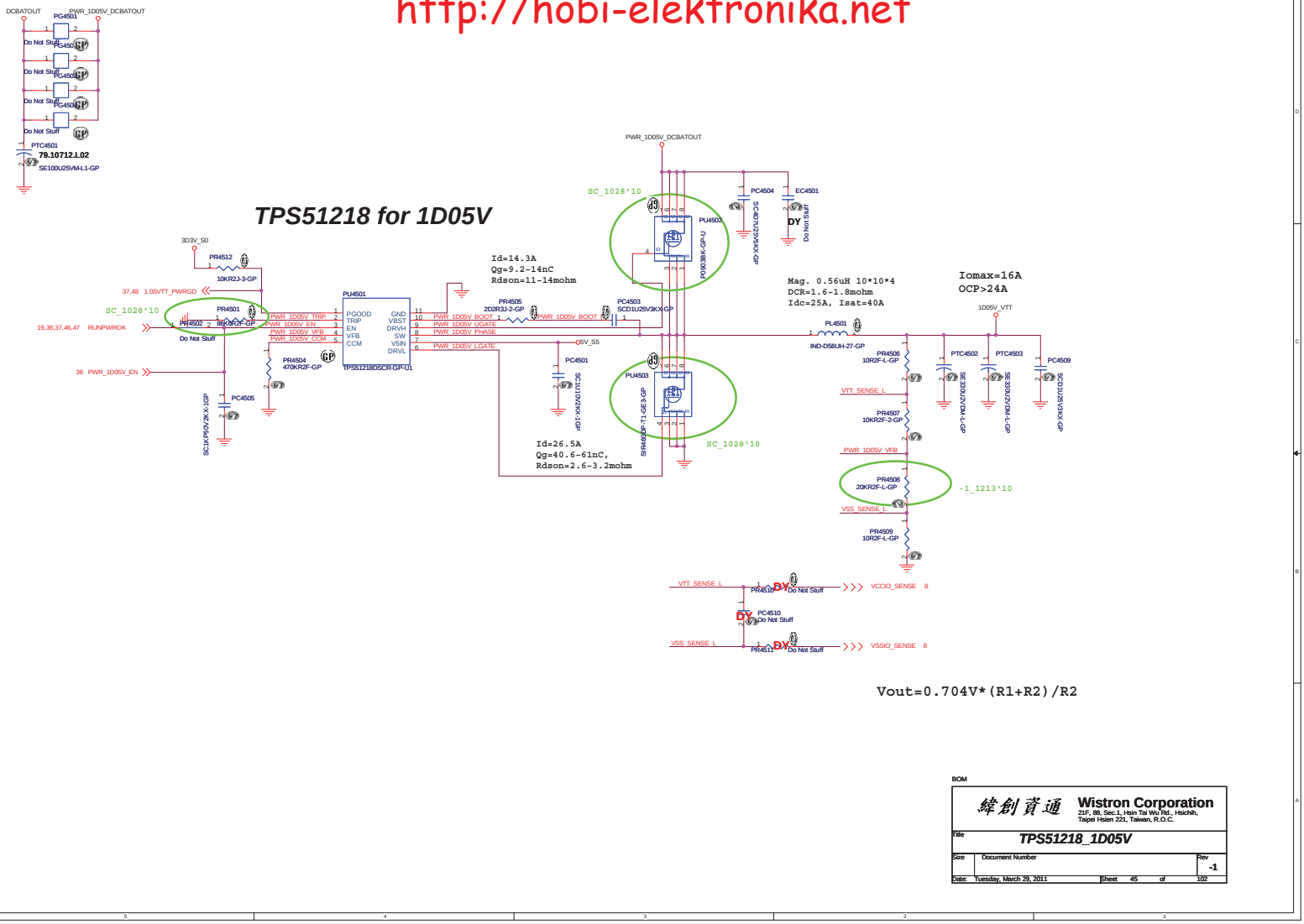


緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DC/DC CPU CORE2 _NCP6131	
Size	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 43 of 102	



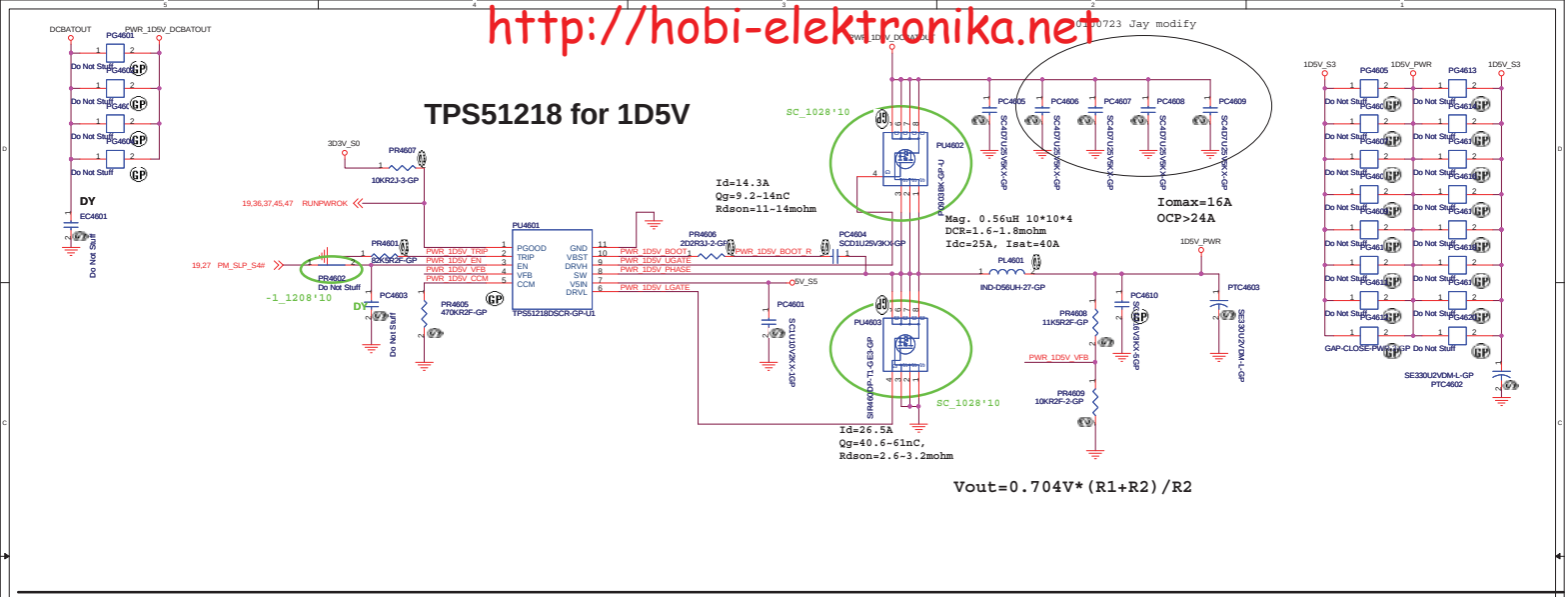
BOM

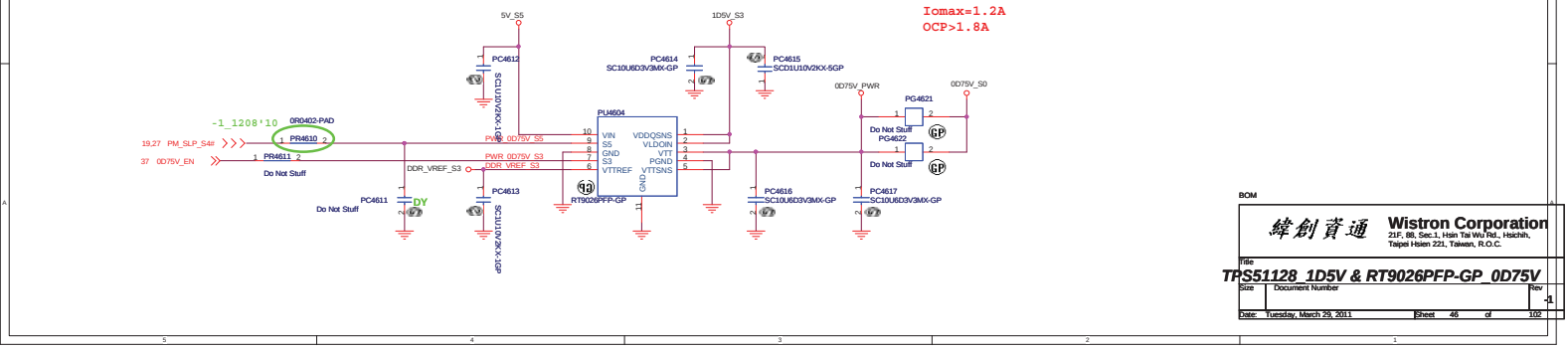
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***DC/DC CPU CORE3 _NCP6131***
Size / Document Number	LZ57
Rev	-1
Date: Tuesday, March 29, 2011	Sheet 44 of 102



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***TPS51218_1D05V***	
Size	Document Number	Rev -1
Date: Tuesday, March 29, 2011	Sheet 45 of 102	

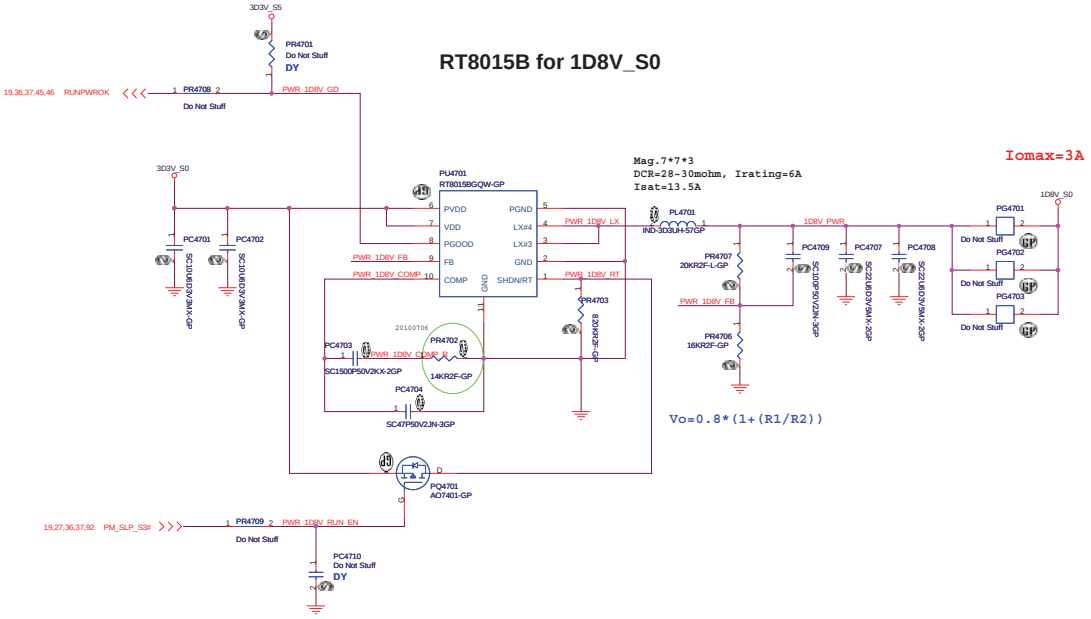




BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: TPS51128_1D5V & RT9026PFP-GP_0D75V		
Size	Document Number	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 46 of 102	

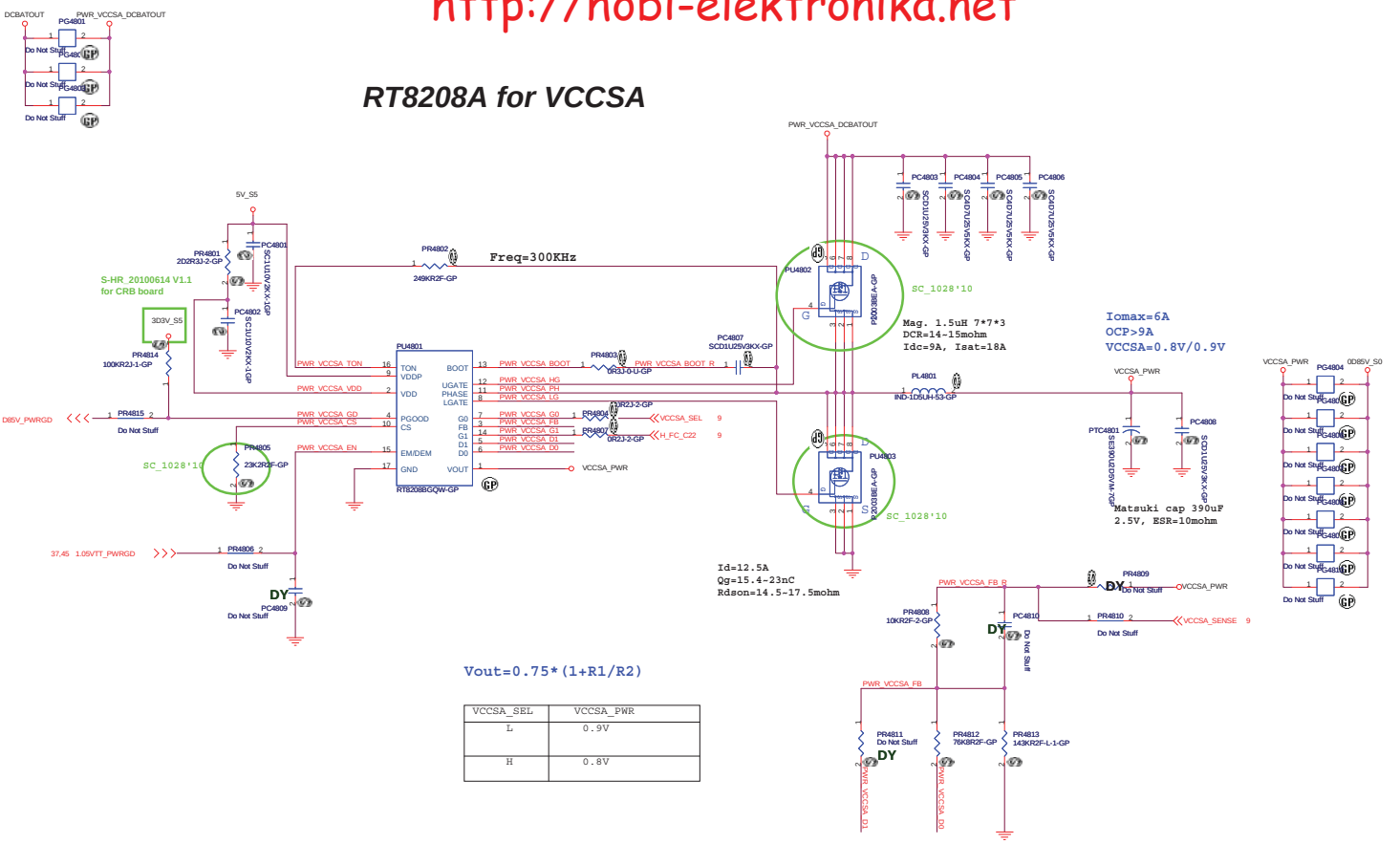
RT9025 for 1D8V_S0



BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 1D8V_RT9025		
Size	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 47 of 102	

RT8208A for VCCSA



Vout=0.75*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

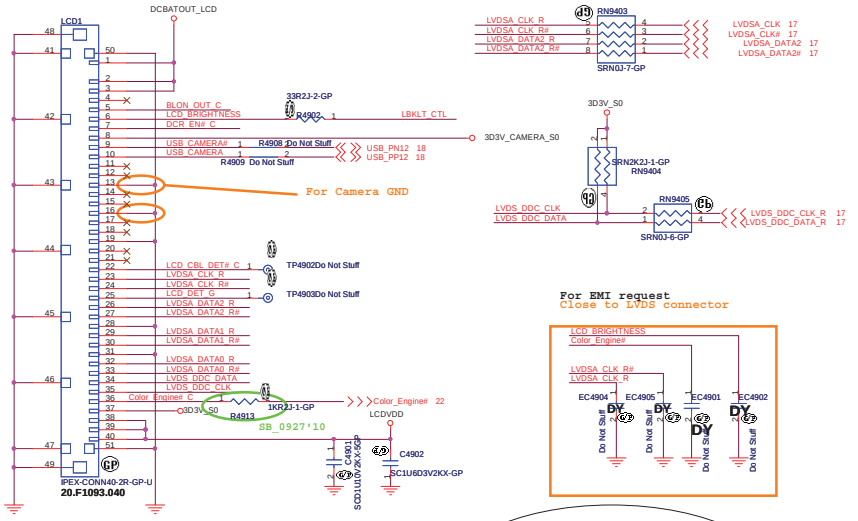
Title: *RT8208B_VCCSA*

Size	Document Number	Rev
	LZ57	-1

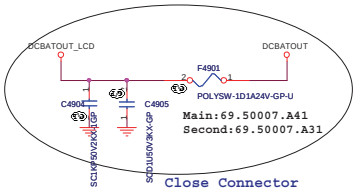
Date: Tuesday, March 29, 2011 Sheet 48 of 102

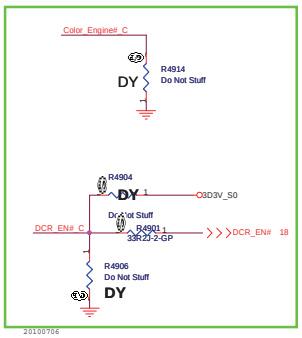
SSID = VIDEO

LVDS CONNECTOR

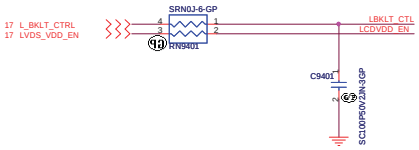


For EMI request
Close to LVDS connector

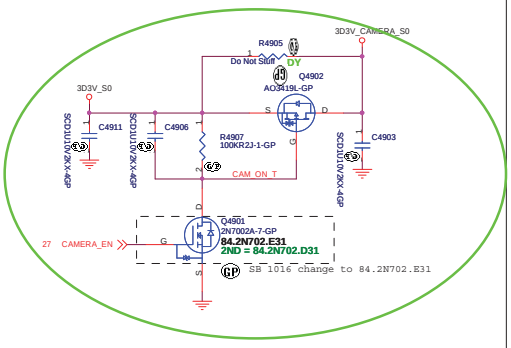




Panel BL brightness/Power En/BL En

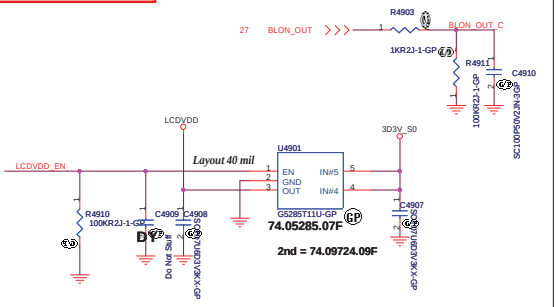


CAMERA POWER



SB 0923'10

SSID = VIDEO



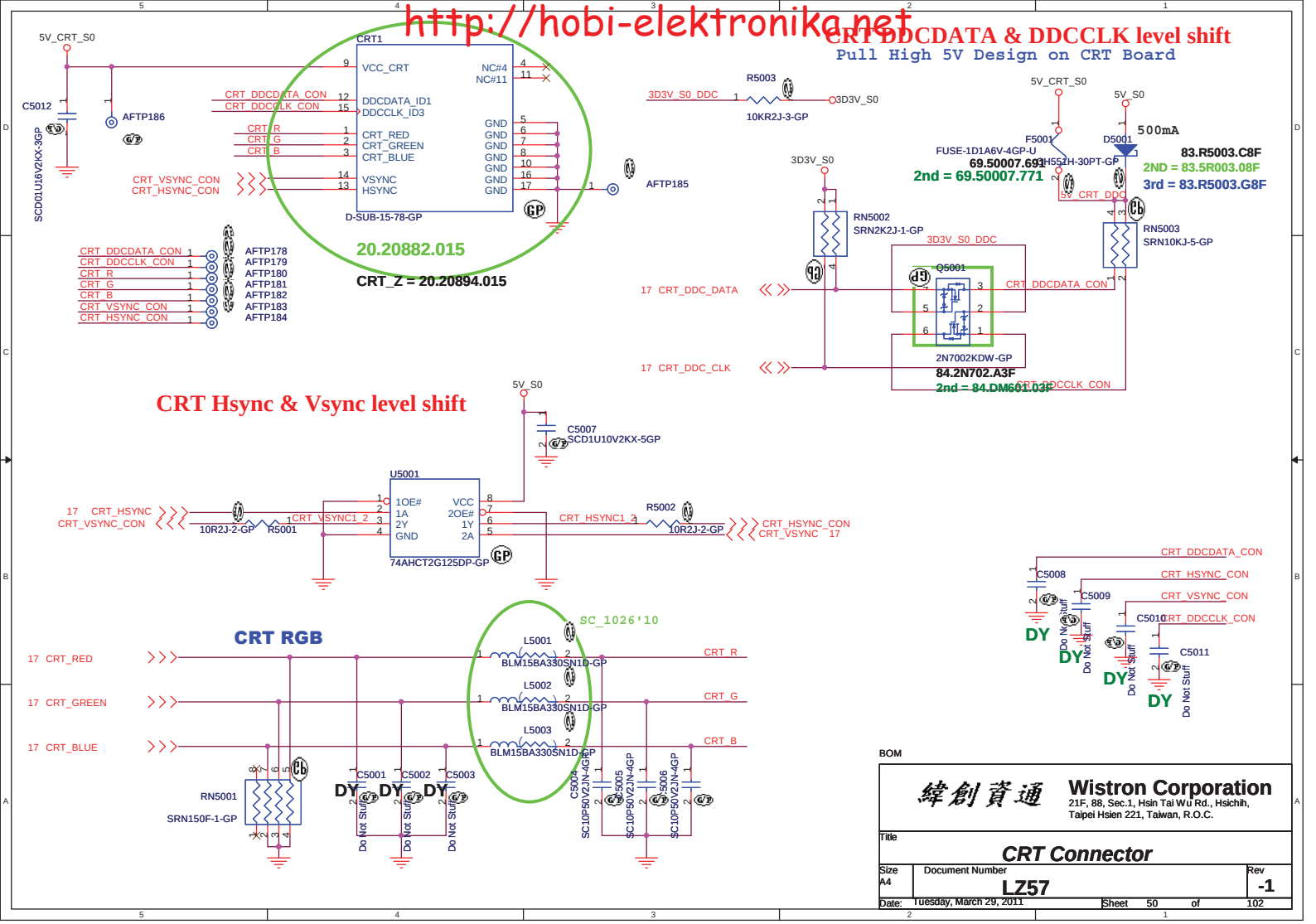
BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 49 of 102



BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size	Document Number	Rev
A4	LZ57	-1

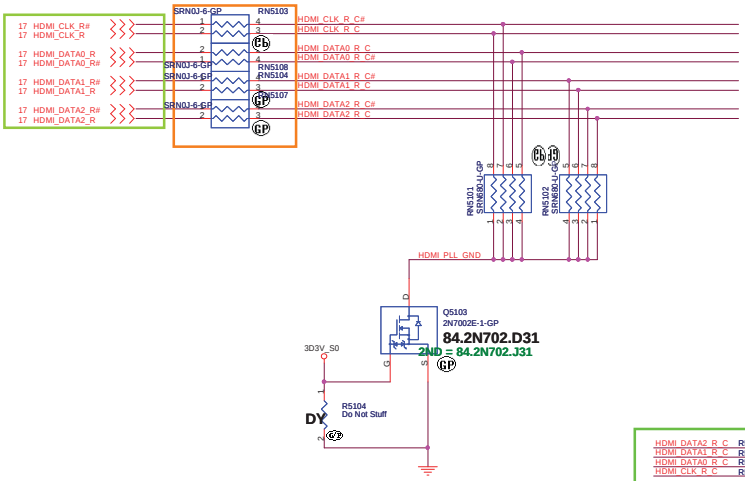
Date: Tuesday, March 29, 2011 Sheet 50 of 102

SSID = VIDEO

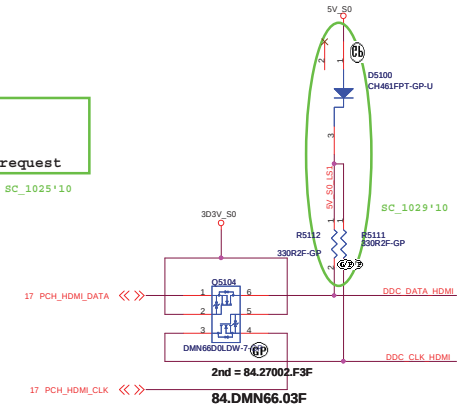
HDMI CONNECTOR

HDMI Passive Level Shifter

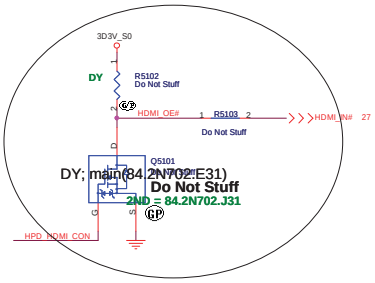
Close to HDMI Connector



HDMI DDC Passive Level Shifter

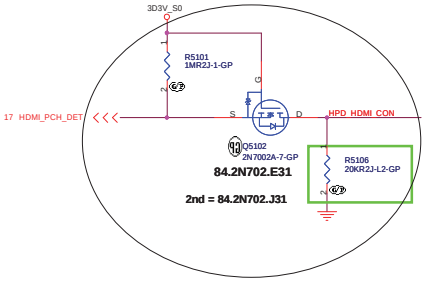


20100727 modify, KBC isn't use.



DY; main(84.2N702.E31)

20100727 follow intel design guide



BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 51 of 102

(Blanking)

Wistron Corporation
6QP
1.2SZ

(Blanking)

BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: S-VIDEO

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 53 of 102

(Blanking)

BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

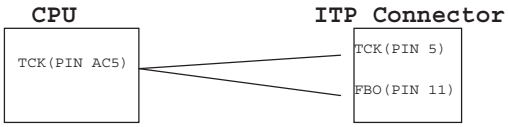
Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 54 of 102

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



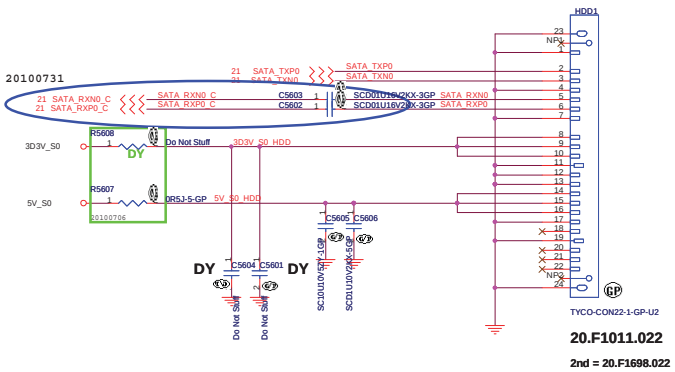
BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP		
Size: A4	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 55 of 102	

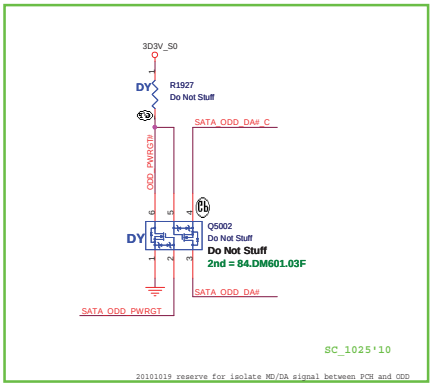
SSID = SATA

SATA HDD Connector



20.F1011.022

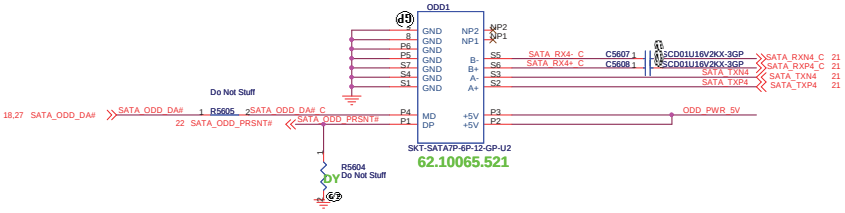
2nd = 20.F1698.022

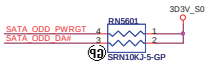


ODD Connector

SATA_RX- and SATA_RX+ Trace Length match within 20 mil

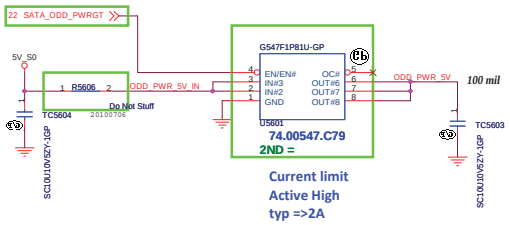
Mars:
Exchange ODD and ESATA differential pair each other.





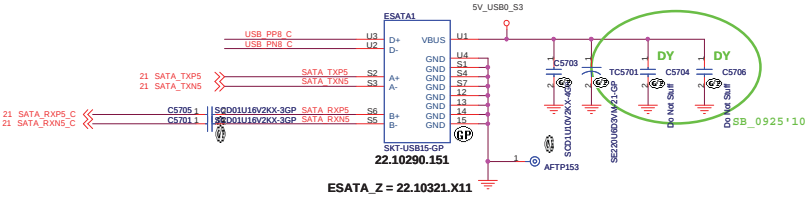
SUPPORT ZERO SATA ODD

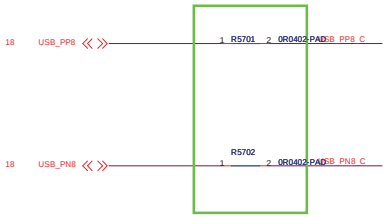
SATA Zero Power ODD

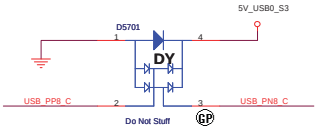


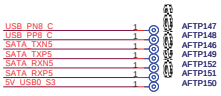
BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD/ODD		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 56 of 102	





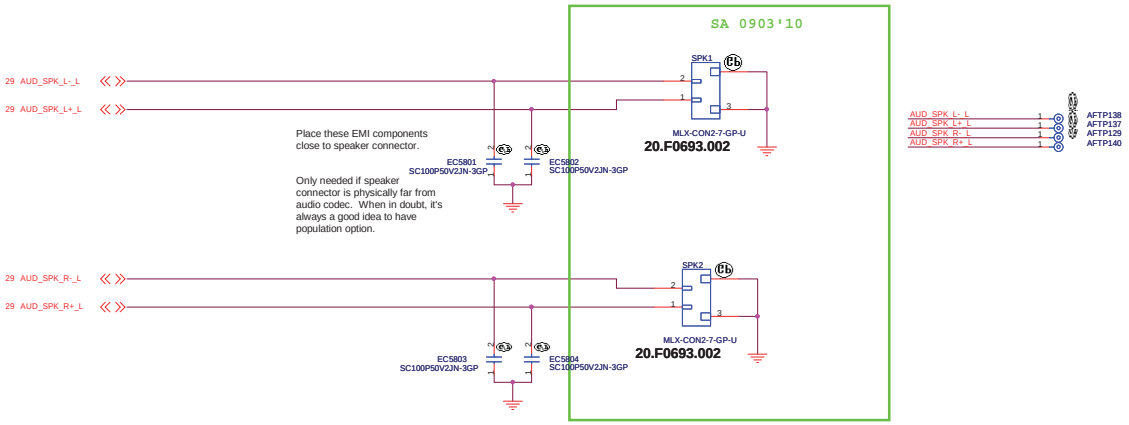




BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: E-SATA/USB		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 57 of 102	

INTERNAL STEREO SPEAKERS



BOM

緯創資通 Wistron Corporation 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MIC/SPEAKER/AUDIO JACK		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 58 of 102	

Reserved

BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

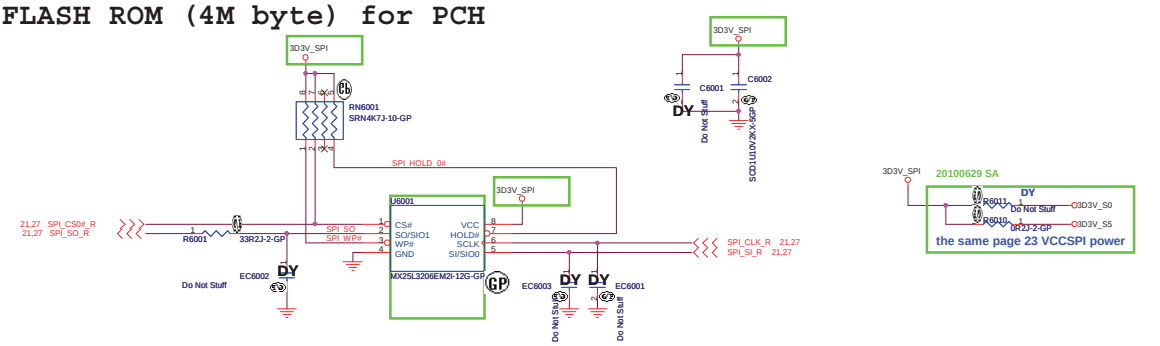
Title: Reserved

Size	Document Number	Rev
A3	LZ57	-1

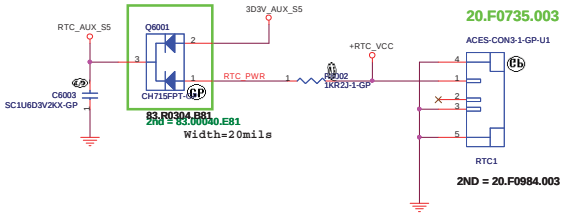
Date: Tuesday, March 29, 2011 Sheet 59 of 102

SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH



SSID = RBATT

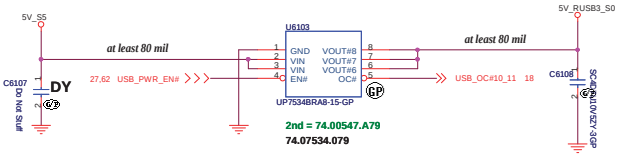


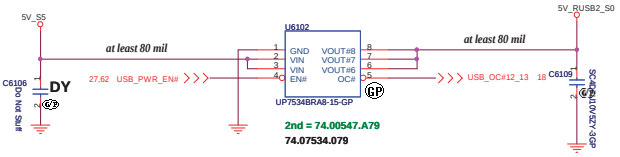
BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Flash/RTC		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 60 of 102	

SSID = USB

RJ45_USB Board USB Power





I/O Board USB Power

BOM

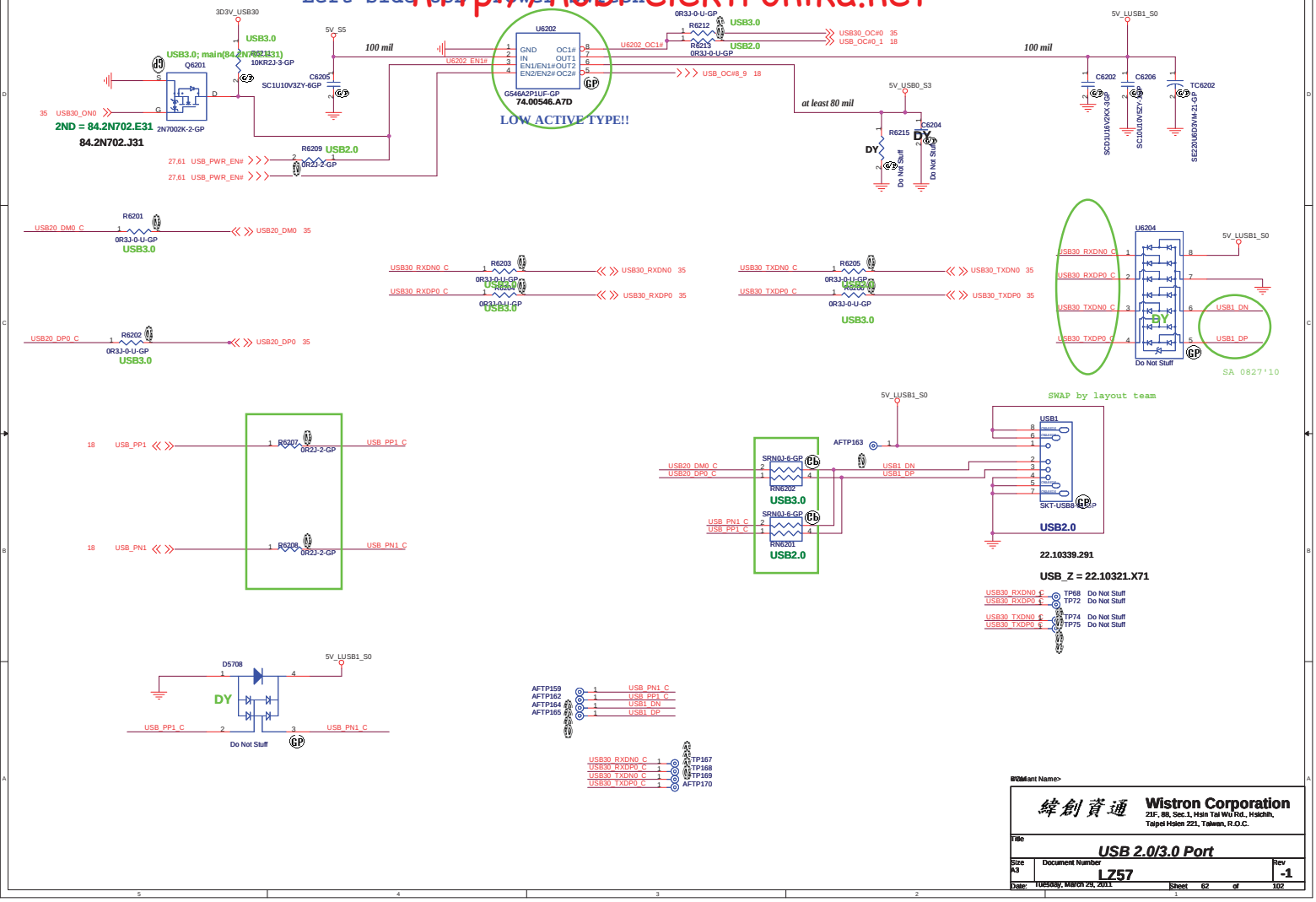
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Power SW

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 61 of 102

Left Side USB Power Switch



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB 2.0/3.0 Port

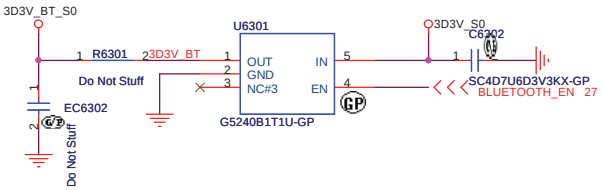
Size: A3 | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 62 of 102

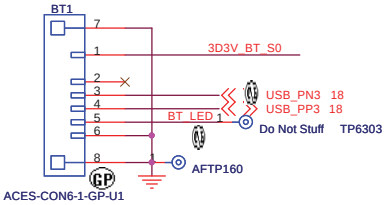
SSID = User.Interface

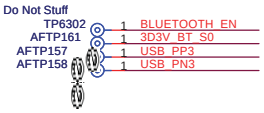
Bluetooth Module conn.

Bluetooth Module



EC6302 put near BLUE1 / all USB put one choke near connector by EMI request





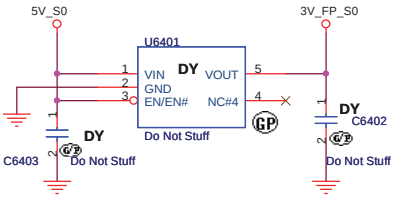
20.F0772.006

2ND = 20.F1804.006

BOM

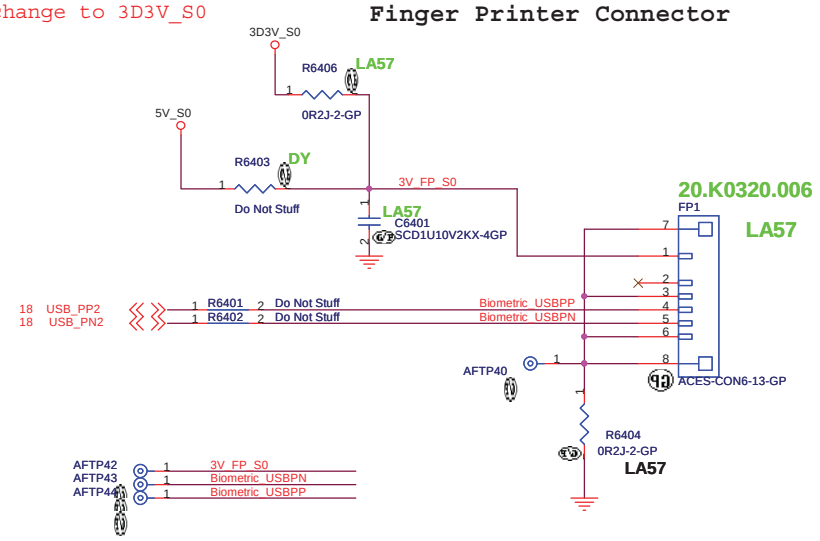
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Bluetooth		
Size: A4	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 63 of 102	



LA47 change to 3D3V_S0

Finger Printer Connector

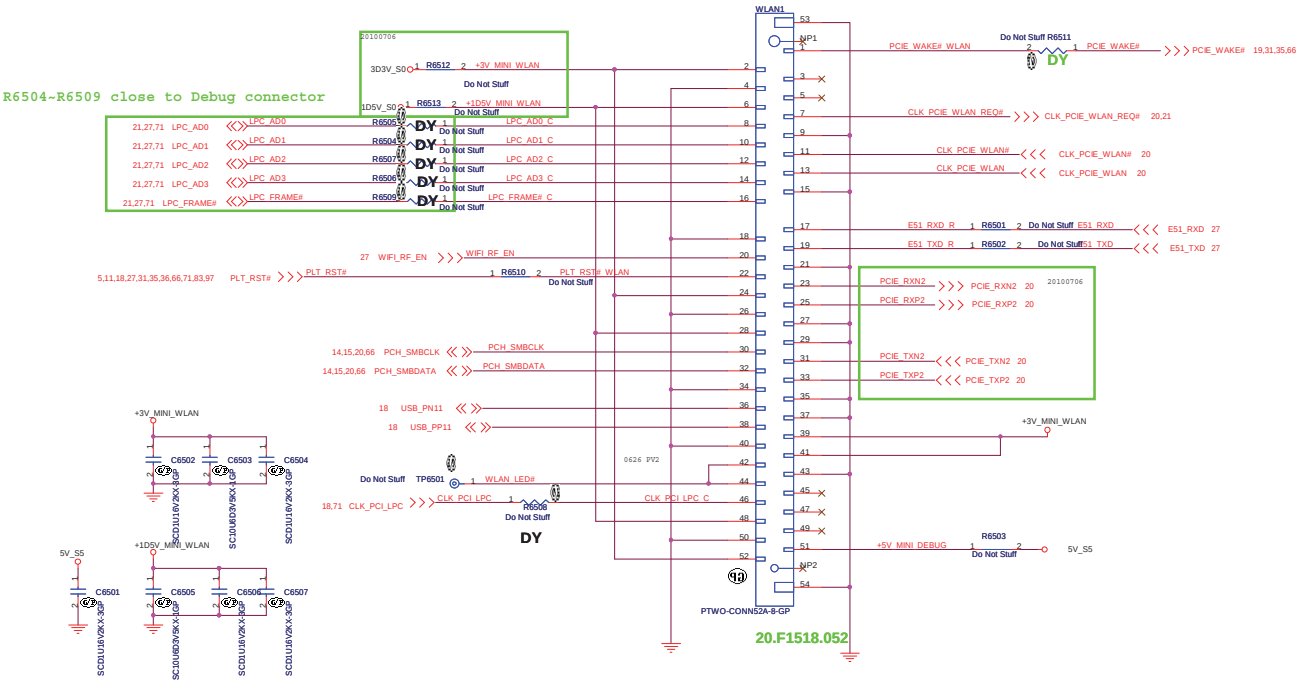


BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RESERVED		
Size: A4	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 64 of 102	

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

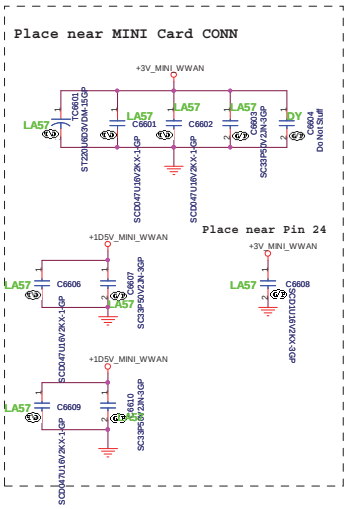


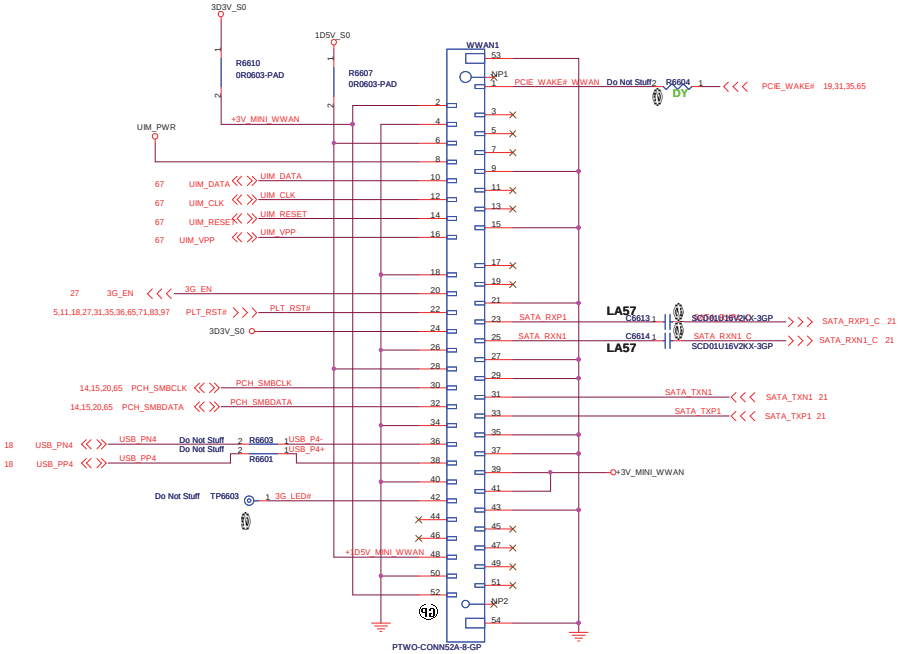
BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINICARD(WLAN)/ITP CONN		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 65 of 102	

SSID = Wireless

Mini Card Connector(WWAN)

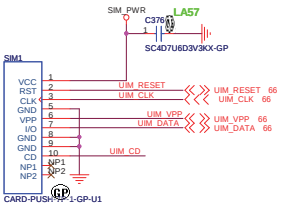


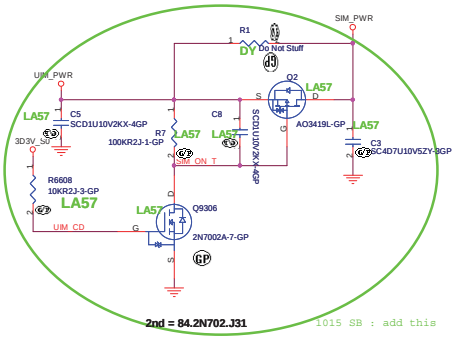


LA5720.F1518.052

BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: WWAN Connector		
Size: A3	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 66 of 102	





LA57

20.I0073.001

2nd = 84.2N702.J31

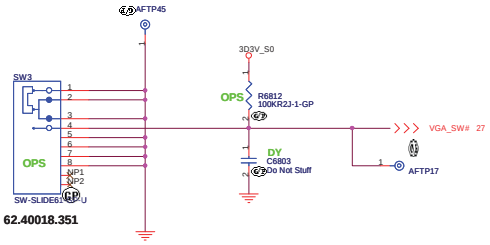
1015 SB : add this

84.2N702.E31

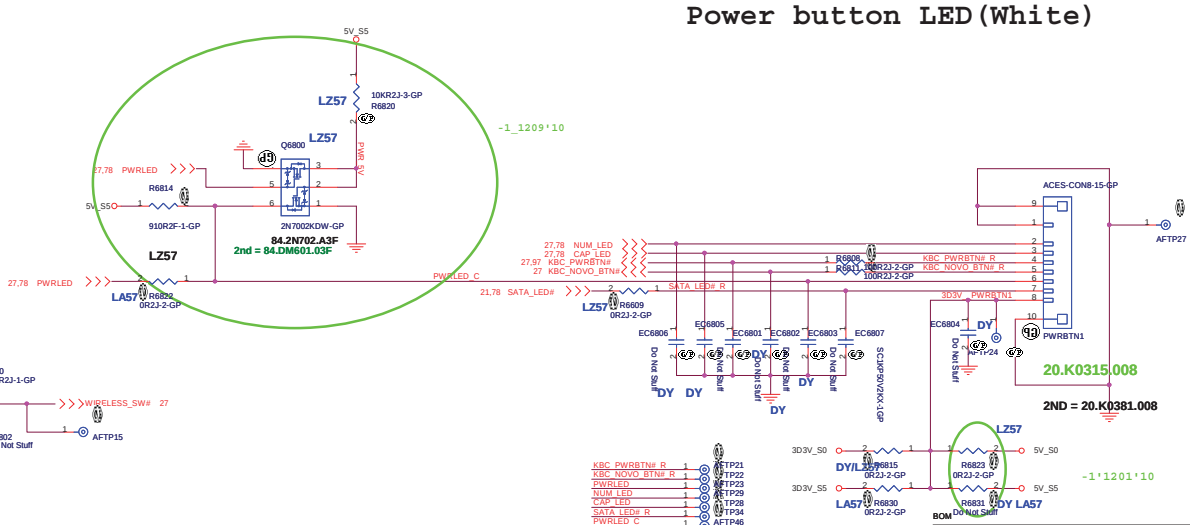
BOM

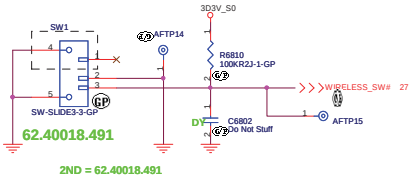
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***SIM CARD***	
Size: A3	Document Number: **LZ57**	Rev: **-1**
Date: Tuesday, March 29, 2011	Sheet 67 of 102	

SSID = User.Interface



Power button LED(White)



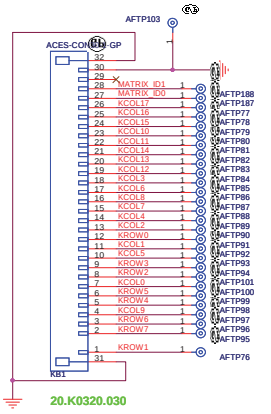


緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LED Bard/Power Button	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 68 of 102	

SSID = KBC

SSID = Touch.Pad

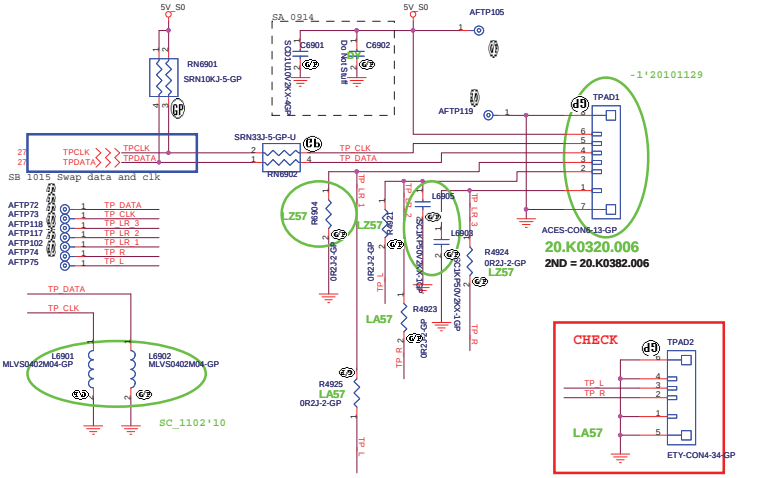
Internal KeyBoard Connector

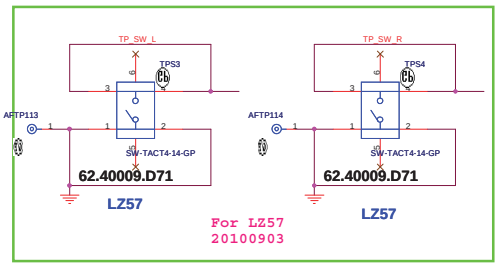


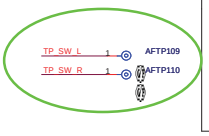
ID KEY MATRIX	SENSE			
	27	28	29	30
	IDO	ID1	ID2	GND
US	GND	GND	X	GND
GB	GND	X	X	GND
JP	X	GND	X	GND

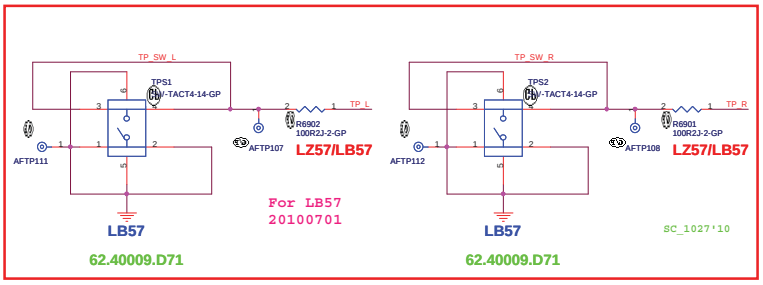
KROW[0..7] 27

KCOL[0..17] 27









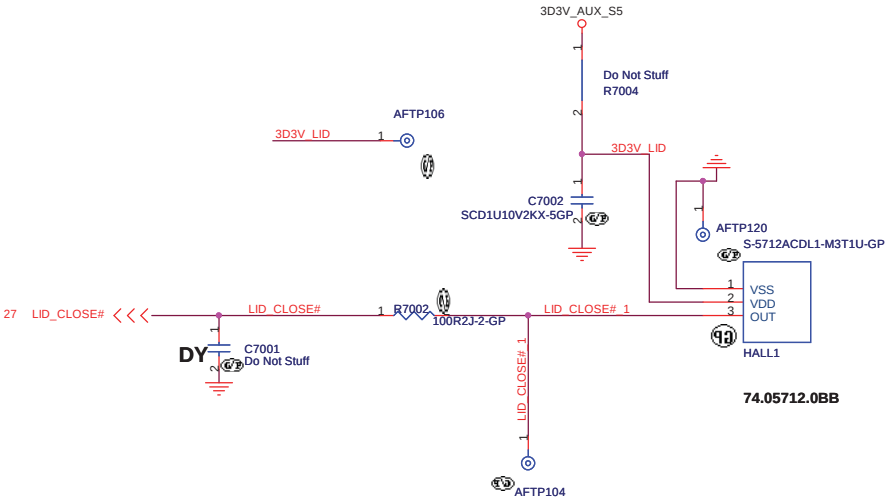
BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 69 of 102



74.05712.0BB

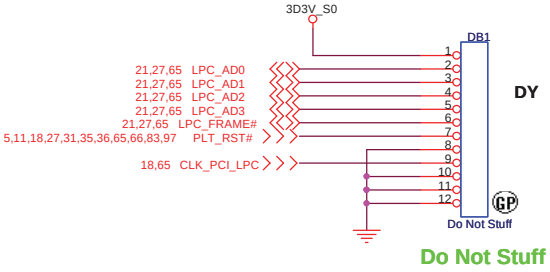
BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 70 of 102



Do Not Stuff

BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Dubug connector		
Size: A4	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 71 of 102	

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BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 72 of 102

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BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 73 of 102

BOM

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader CONN**

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 74 of 102

BOM

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***New Card***

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 75 of 102

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BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 76 of 102

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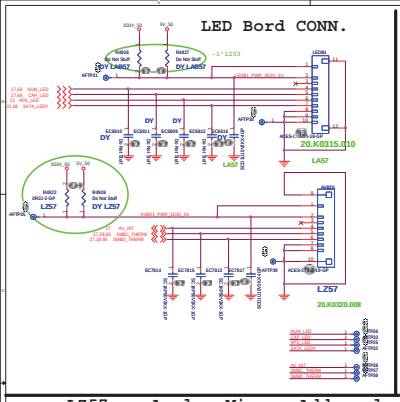
BOM

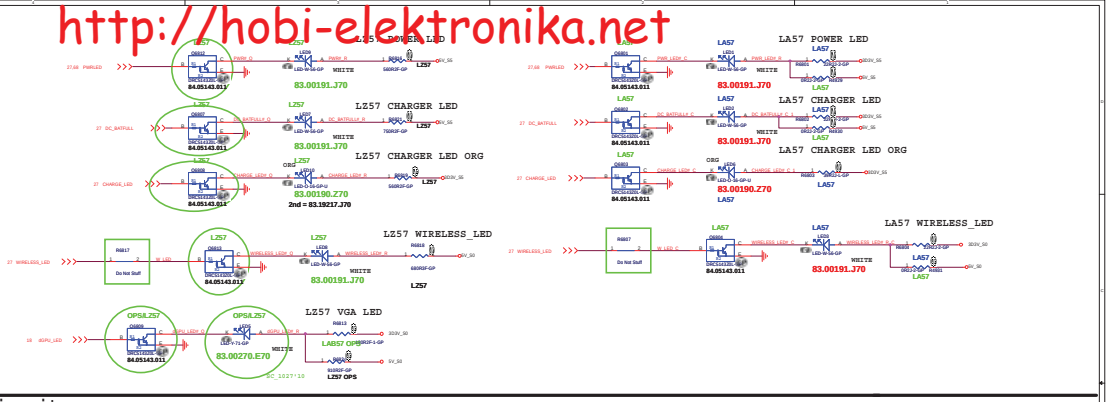
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

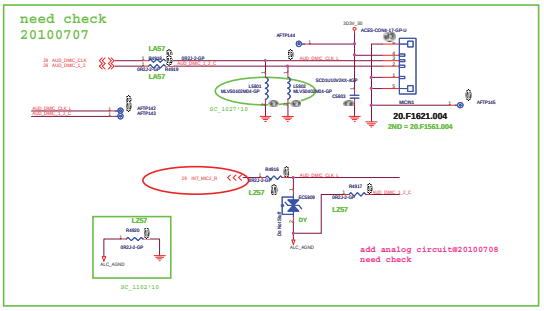
Size	Document Number	Rev
A4	LZ57	-1

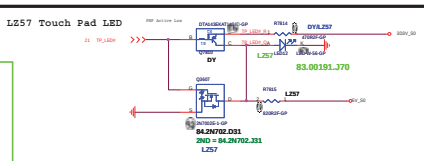
Date: Tuesday, March 29, 2011 Sheet 77 of 102

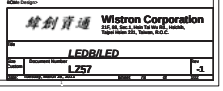




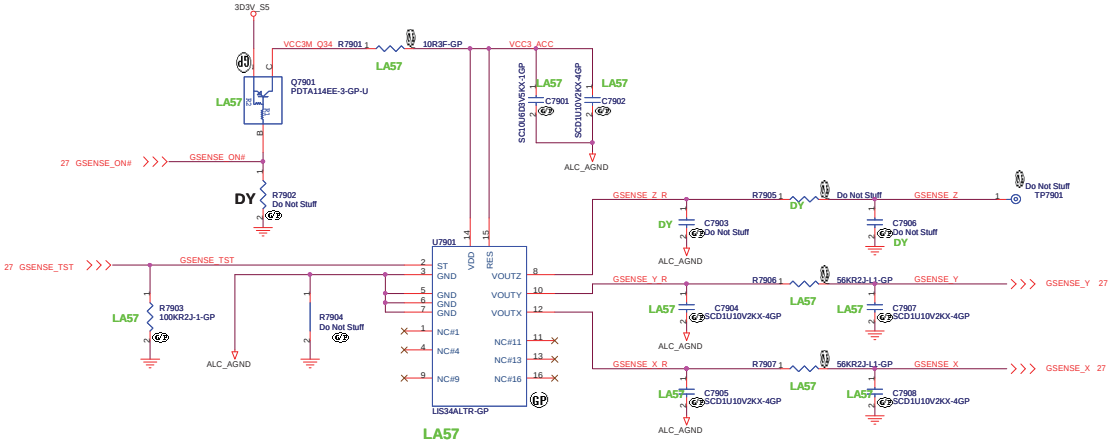
LZ57 => Analog Mic => Add analog circuit.
LA57 => Digital Mic







G-Sensor



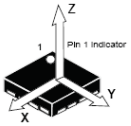
STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00335.0BZ

	ADXL322 LIS244AL LIS34AL	No Accel
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	G-Sensor	
Size: Custom	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 79 of 102	

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BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 80 of 102

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BOM

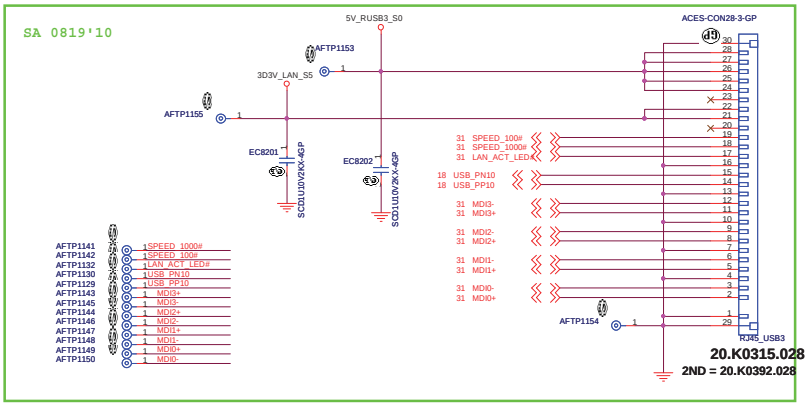
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

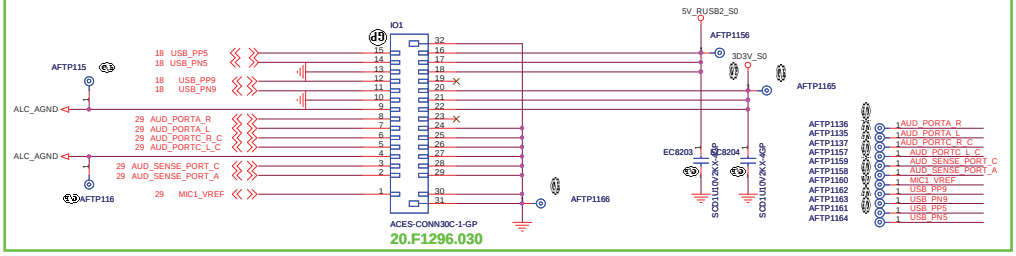
Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 81 of 102

RJ45_USB CONN.



Card Reader Board CONN.



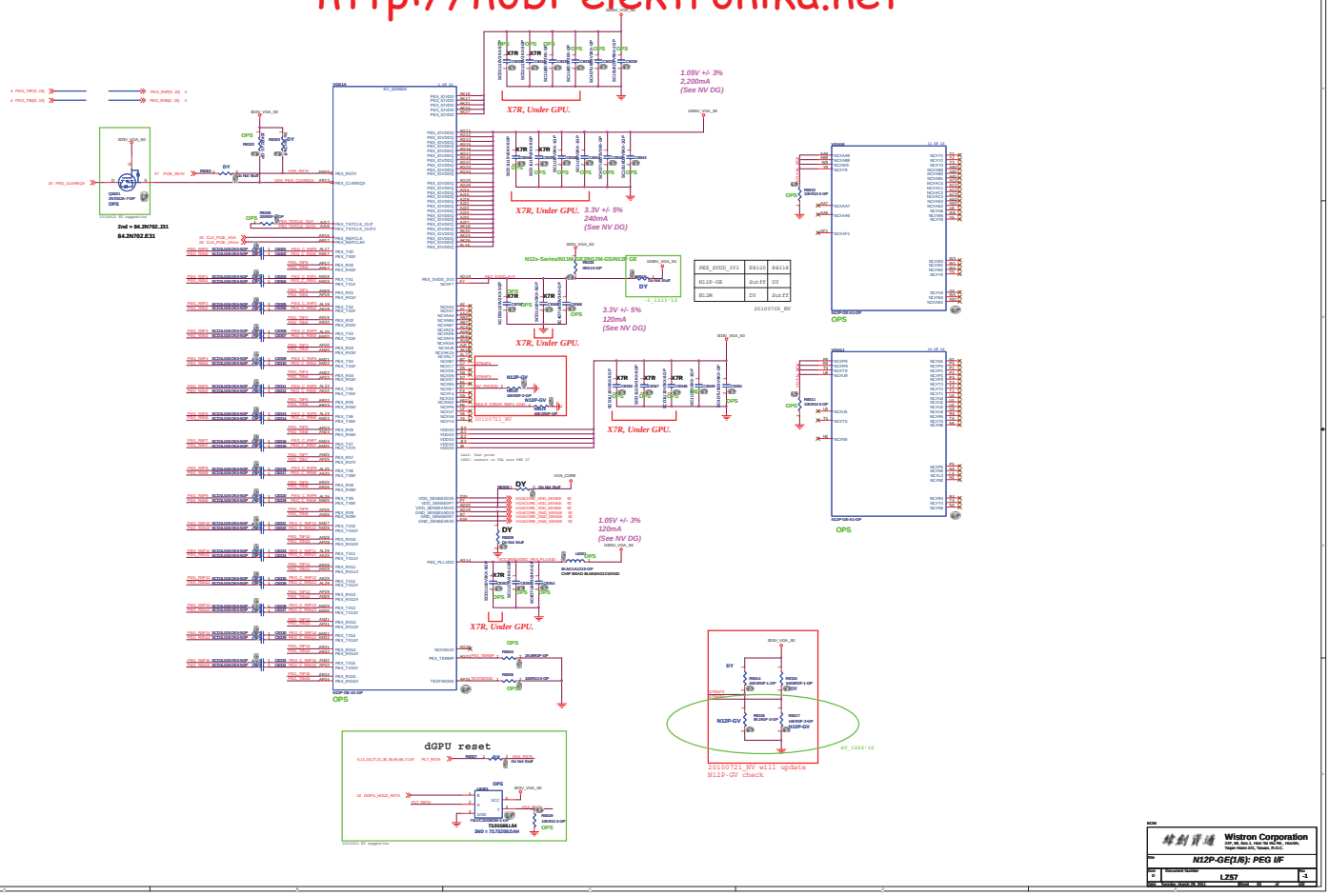
BOM

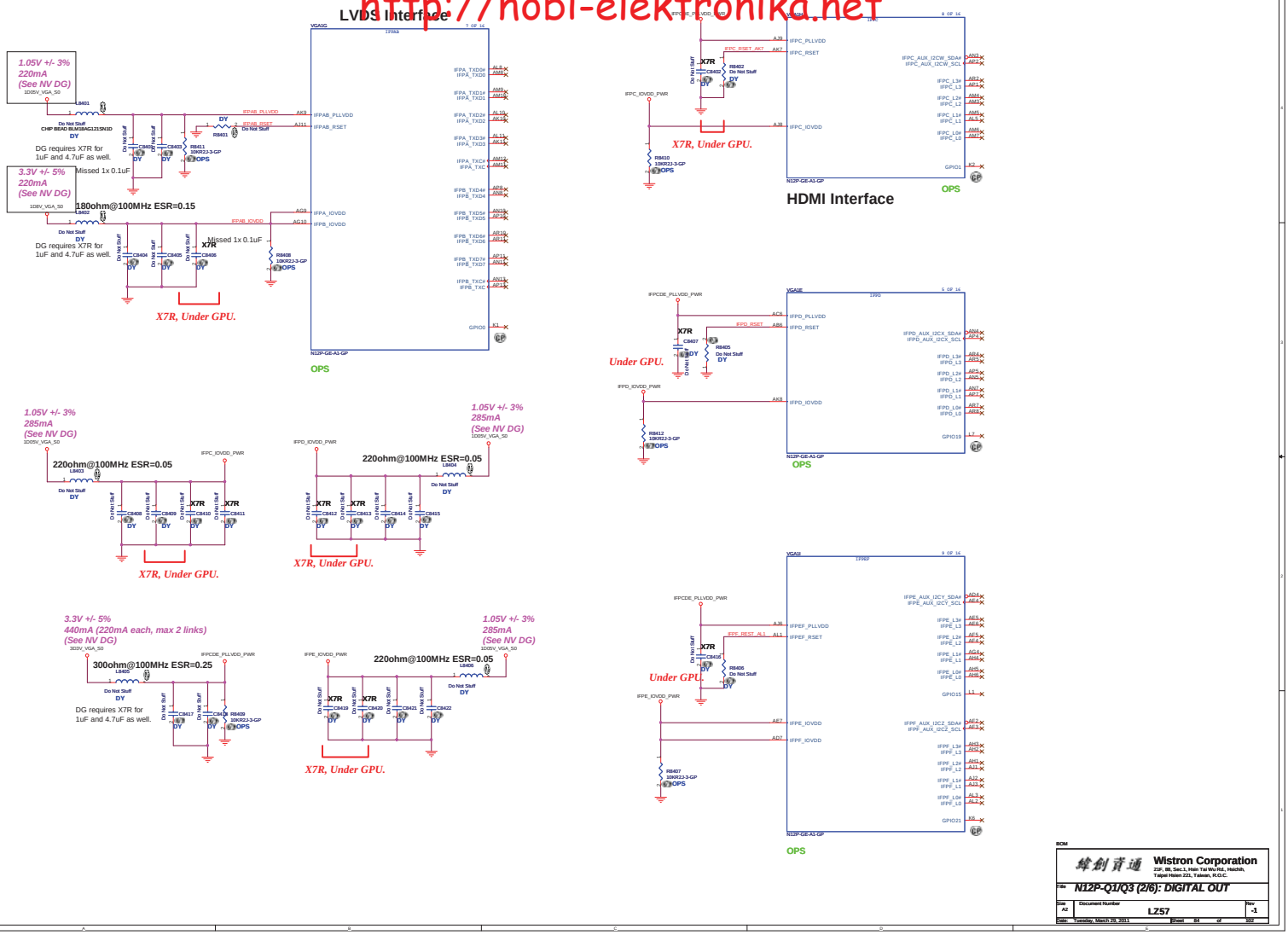
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***IO Board Connector***

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 82 of 102





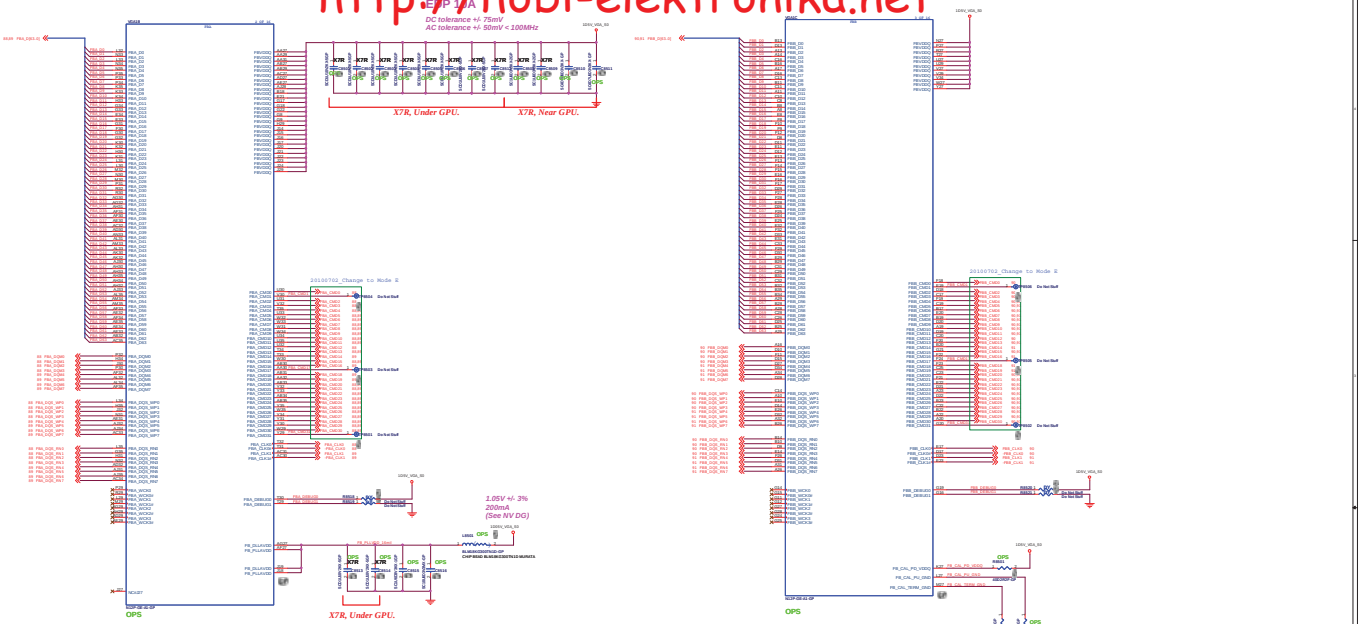
BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

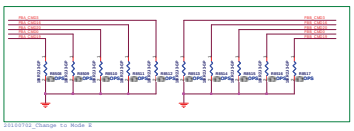
Title: N12P-Q1/Q3 (2/6): DIGITAL OUT

Size	Document Number	Rev
A2	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 84 of 102



FBCLK Termination place on VRAM side



FBCLK Termination place on VRAM side

Wistron Corporation	
N12P-Q1/Q3 (3/6): VRAM I/F	
Document Number	Rev
L257	A
Date: Monday, March 29, 2010	Sheet 46 of 47

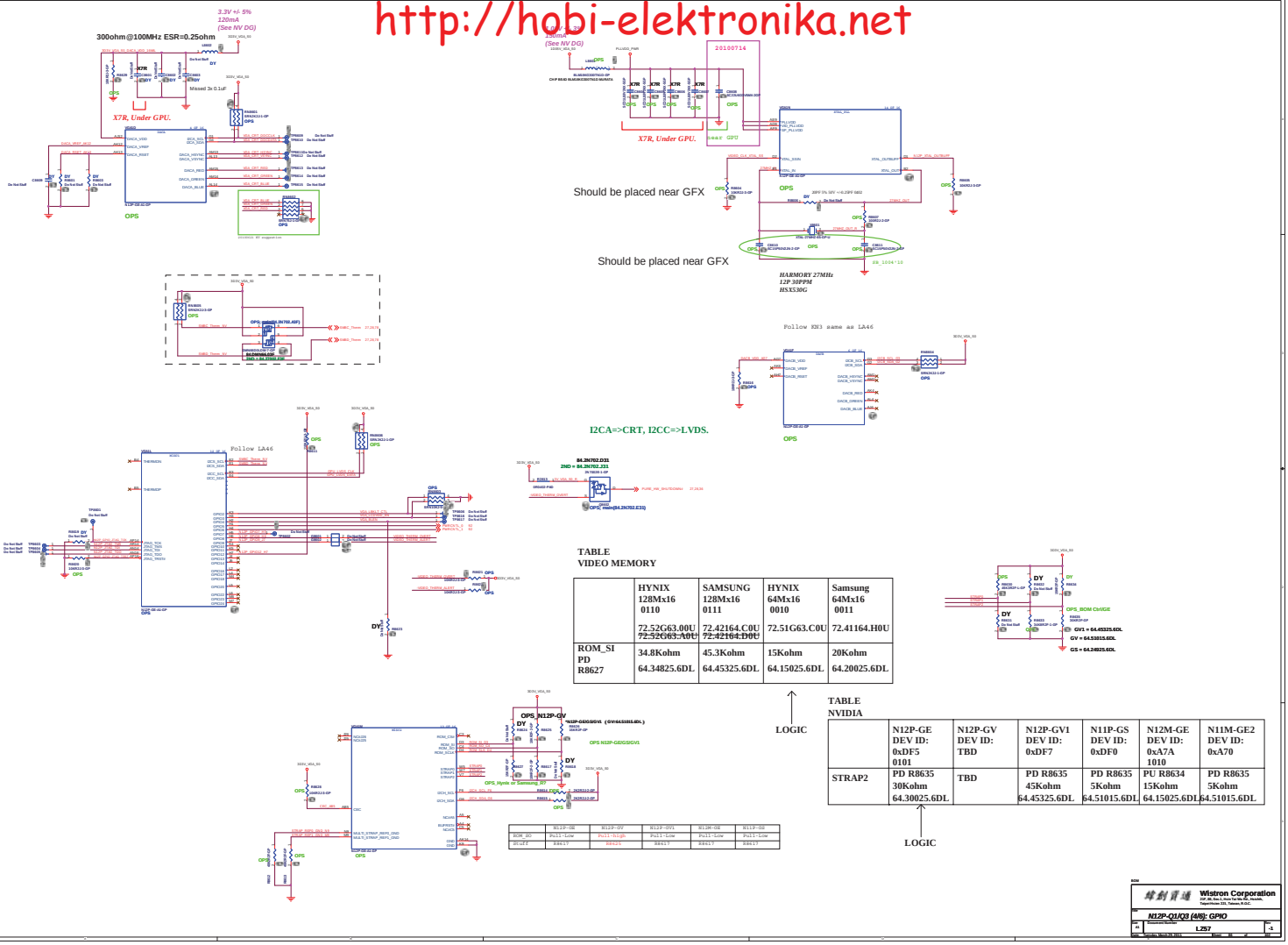


TABLE
VIDEO MEMORY

	HYNIX 128Mx16 0110 72.52G63.00U ~~72.52G63.A0U~~	SAMSUNG 128Mx16 0111 72.42164.C0U ~~72.42164.D0U~~	HYNIX 64Mx16 0010 72.51G63.C0U	Samsung 64Mx16 0011 72.41164.H0U
ROM_SI PD R8627	34.8Kohm 64.34825.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL

LOGIC

TABLE
NVIDIA

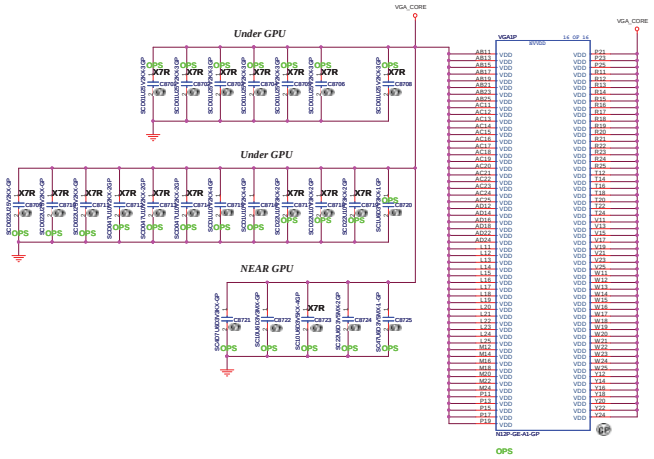
	N12P-GE DEV ID: 0xDF5 0101	N12P-GV DEV ID: TBD	N12P-GV1 DEV ID: 0xDF7	N11P-GS DEV ID: 0xDF0	N12M-GE DEV ID: 0xA7A 1010	N11M-GE2 DEV ID: 0xA70
STRAP2	PD R8635 30Kohm 64.30025.6DL	TBD	PD R8635 45Kohm 64.45325.6DL	PD R8635 5Kohm 64.51015.6DL	PU R8634 15Kohm 64.15025.6DL	PD R8635 5Kohm 64.51015.6DL

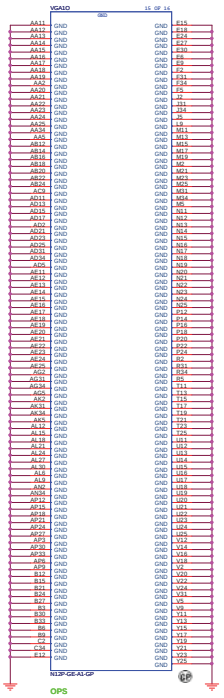
LOGIC

	N12P-GE	N12P-GV	N12P-GV1	N12M-GE	N11P-GS
ROM_SO	Pull-Low	Pull-High	Pull-Low	Pull-Low	Pull-Low
Stuff	R8617	R8625	R8617	R8617	R8617

Wistron Corporation
N12P-Q1/Q3 (4/6): GPIO
LZ57

EDP 50A
(TDP 37W)





BOM

蜂創資通 Wistron Corporation
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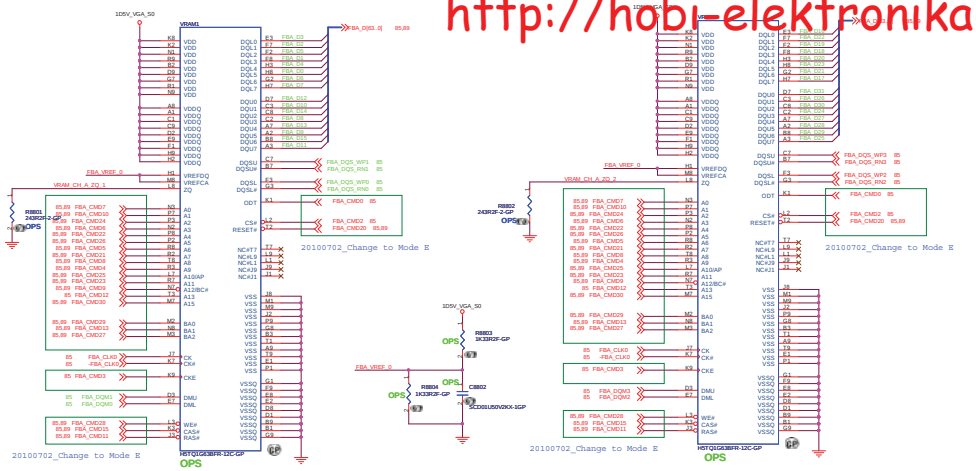
Title: N12P-Q1/Q3 (5/6): POWER

Size	Document Number	Rev
A0	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 87 of 102



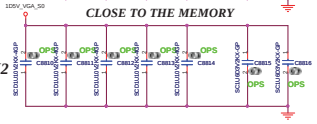
FB CMD mapping Mode D-N12x

DG requires 4x0.1uF and 8x1.0uF per VRAM chip

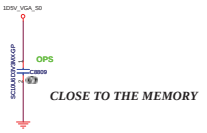
FOR VRAM1

CLOSE TO THE MEMORY

FOR VRAM2



CLOSE TO THE MEMORY

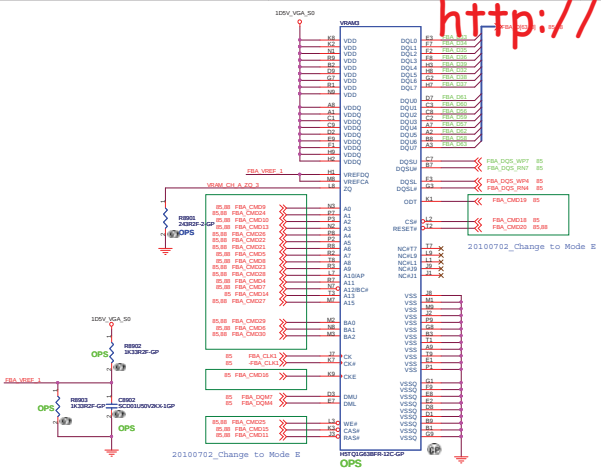


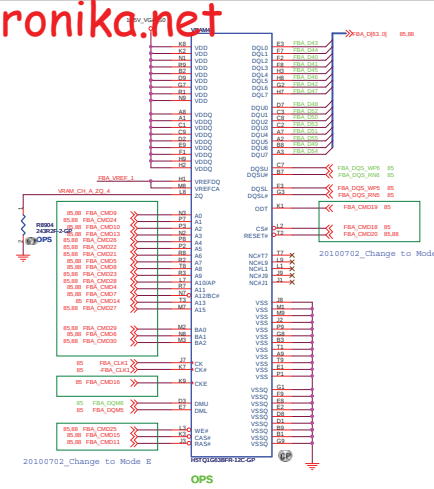
CLOSE TO THE MEMORY

VIDEO FRAME BUFFER PORT A

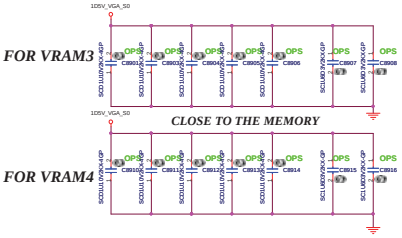
BOM

蜂創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: VRAM CHANNEL-A		
Size: A2	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 88 of 102	





FB CMD mapping Mode D-N12x



VIDEO FRAME BUFFER PORT A

BOM

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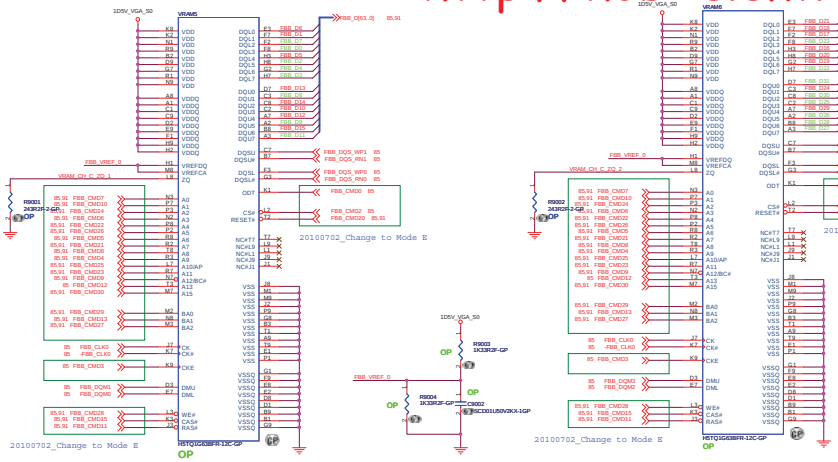
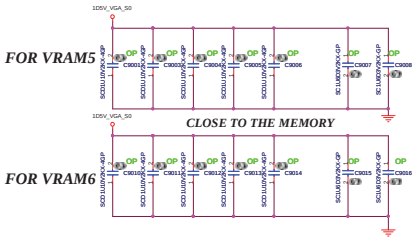
File: VRAM CHANNEL-A

Size	Document Number	Rev
A2	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 89 of 102



DG requires 4x0.1uF and 8x1.0uF per VRAM chip



VIDEO FRAME BUFFER PORT C

BOM

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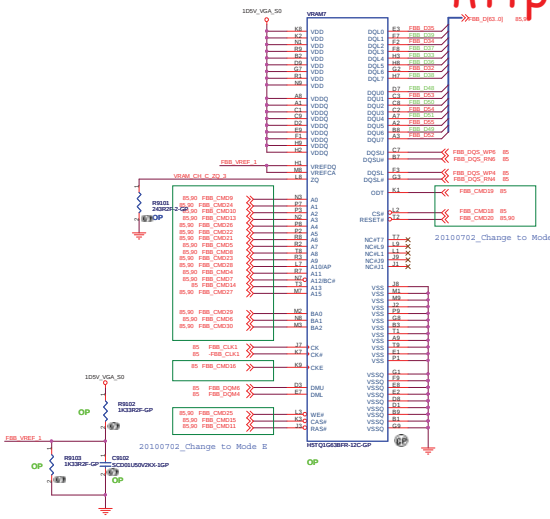
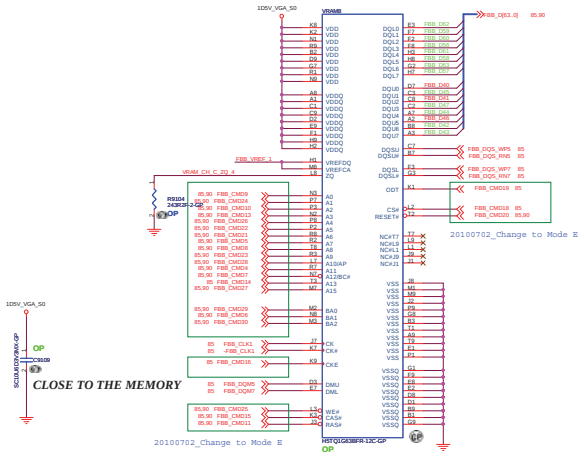
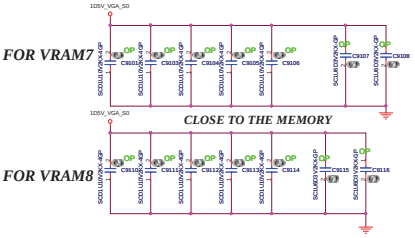
File: **VRAM CHANNEL-C**

Size	Document Number	Rev
A2	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 90 of 302



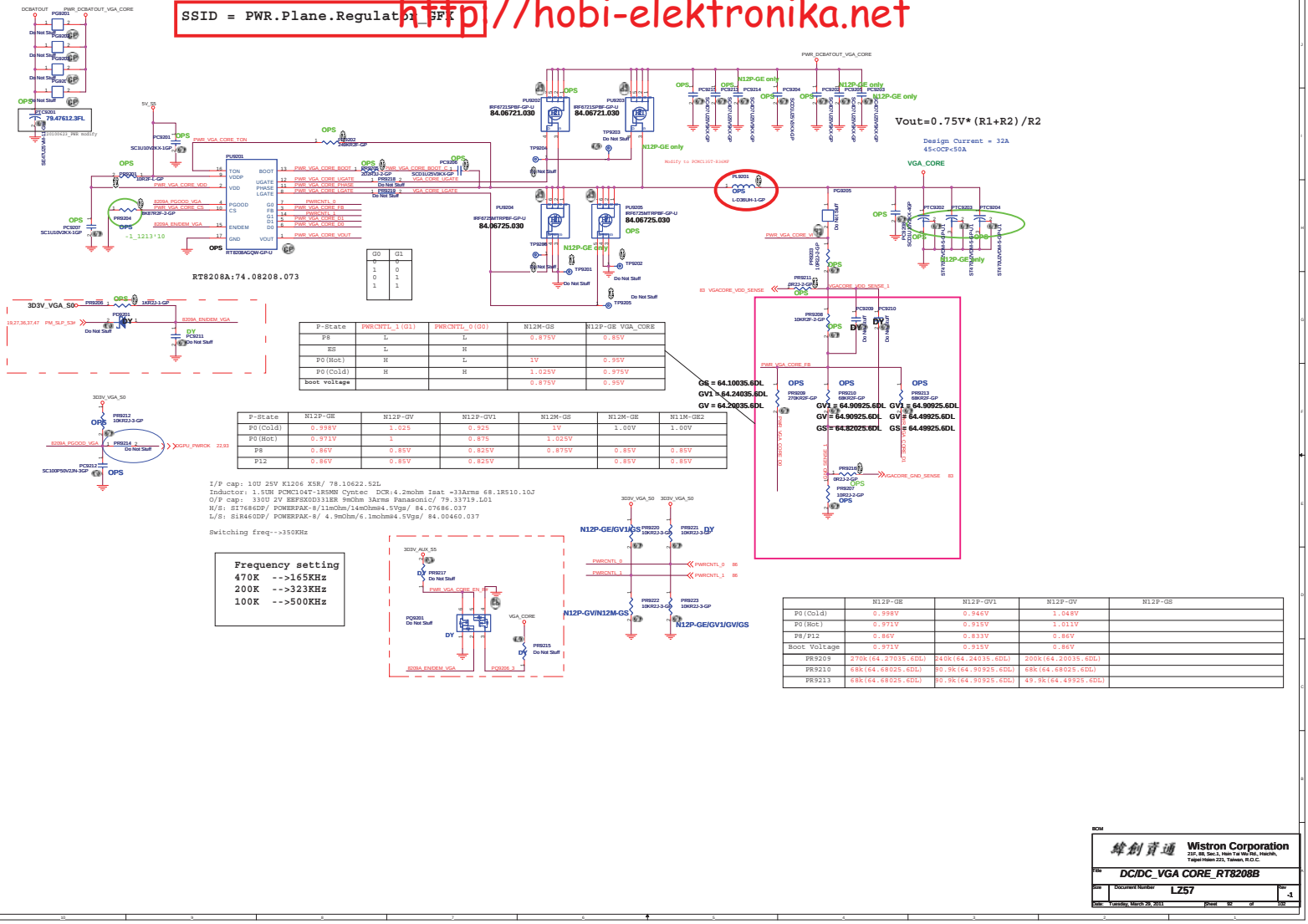




VIDEO FRAME BUFFER PORT C

BOM

緯創資通	Wistron Corporation 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	VRAM CHANNEL-C	
Size: A2	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 91 of 102	



P-State	PWRCNTL_1 (G1)	PWRCNTL_0 (G0)	N12M-GS	N12P-GE VGA_CORE
P8	L	L	0.875V	0.85V
ES	L	H		
P0(Hot)	H	L	1V	0.95V
P0(Cold)	H	H	1.025V	0.975V
boot voltage			0.875V	0.95V

P-State	N12P-GE	N12P-GV	N12P-GV1	N12M-GS	N12M-GE	N11M-GE2
P0(Cold)	0.998V	1.025	0.925	1V	1.00V	1.00V
P0(Hot)	0.971V	1	0.875	1.025V		
P8	0.86V	0.85V	0.825V	0.875V	0.85V	0.85V
P12	0.86V	0.85V	0.825V		0.85V	0.85V

I/P cap: 10U 25V K1206 XSR/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SIR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

Switching freq--350KHz

Frequency setting
470K -->165KHz
200K -->323KHz
100K -->500KHz

	N12P-GE	N12P-GV1	N12P-GV	N12P-GS
P0(Cold)	0.998V	0.946V	1.048V	
P0(Hot)	0.971V	0.915V	1.011V	
P8/P12	0.86V	0.833V	0.86V	
Boot Voltage	0.971V	0.915V	0.86V	
PR9209	270K(64.27035.6DL)	240K(64.24035.6DL)	200K(64.20035.6DL)	
PR9210	68K(64.68025.6DL)	80.9K(64.90925.6DL)	68K(64.68025.6DL)	
PR9213	68K(64.68025.6DL)	80.9K(64.90925.6DL)	49.9K(64.49925.6DL)	

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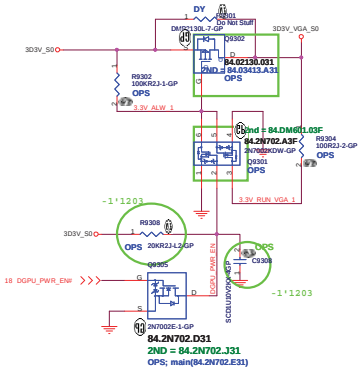
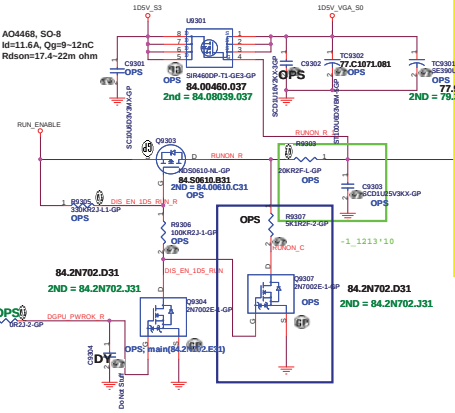
Title	DC/DC_VGA CORE_RT8208B	
Size	Document Number	Rev
	LZ57	-1
Date: Tuesday, March 29, 2011	Sheet 82 of 102	

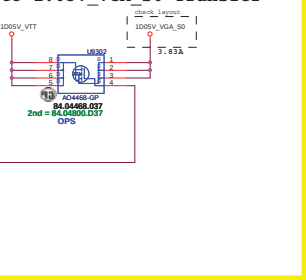
+3VS to 3.3V_DELAY Transfer



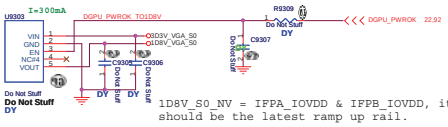
1D5V_VGA_S0



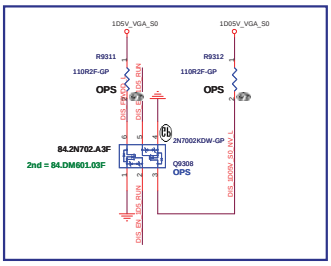
1.05V to 1.05V_VGA_S0 Transfer



+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.



BOM

鋒創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DISCRETE VGA POWER	
Size	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 83 of 102	

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BOM

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Taipei Hsien 221, Taiwan, R.O.C.

Title

LVDS_Switch

Size	Document Number	Rev
A2	LZ57	-1

Date: Tuesday, March 26, 2013 Sheet 94 of 102

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BOM

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Switch

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 95 of 102

BOM

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Title

TOUCH PANEL

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 96 of 102

CPU Plate

H13 Do Not Stuff
H14 Do Not Stuff
H15 Do Not Stuff

Do Not Stuff Do Not Stuff Do Not Stuff

VGA Std-Off

H10 STF237R128H42-GP
H11 STF237R128H42-GP

OPS

34.4GD01.101 34.4GD01.101

Check test point

3D3V_S0		TP8507	Do Not Stuff
3D3V_AUX_S5		TP8508	Do Not Stuff
3D3V_S5		TP8509	Do Not Stuff
5V_S5		TP8510	Do Not Stuff
11,19,27	PM_PWRBTN#	TP8511	Do Not Stuff
5,11,22,36	H_CPUPWRGD	TP8512	Do Not Stuff
27,36	S5_ENABLE	TP8513	Do Not Stuff
5,11,18,27,31,35,36,65,66,71,83	PLT_RST#	TP8514	Do Not Stuff

Test Point放在Dimm Door打開可量測處

Structure boss

H1 Do Not Stuff
H2 Do Not Stuff
H3 Do Not Stuff
H5 Do Not Stuff
H6 Do Not Stuff
H12 Do Not Stuff
H7 Do Not Stuff
H8 Do Not Stuff

Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff Do Not Stuff

MiniPCI Std-Off

H4 STF237R113H63-GP

34.44P03.101

Do Not Stuff
H16

Do Not Stuff

H17 Do Not Stuff

Do Not Stuff

S1 SPRING-71-GP
S2 SPRING-63-GP
S3 SPRING-63-GP

DY

34.4Y806.001 34.4Y806.001

SC_1101'10

POWER TESTING POINT--TOP

27,68 KBC_PWRBTN#
TP9701 Do Not Stuff
TP9700 Do Not Stuff

POWER TESTING POINT--Bottom

27,68 KBC_PWRBTN#
TP9702 Do Not Stuff
TP9703 Do Not Stuff

AD+
EC9708 EC9709 EC9710 EC9711 EC9712 EC9713
DY Do Not Stuff
SCD1U25V2KX-GP

DCBATOUT
AD_JK
EC9720 EC9719 EC9718 EC9717 EC9716 EC9715
DY Do Not Stuff
SCD1U25V2KX-GP

SA 0904'10

DCBATOUT
EC9714
SCD1U25V2KX-GP

SA 0809'10

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Title: UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 97 of 102

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Title: Change History

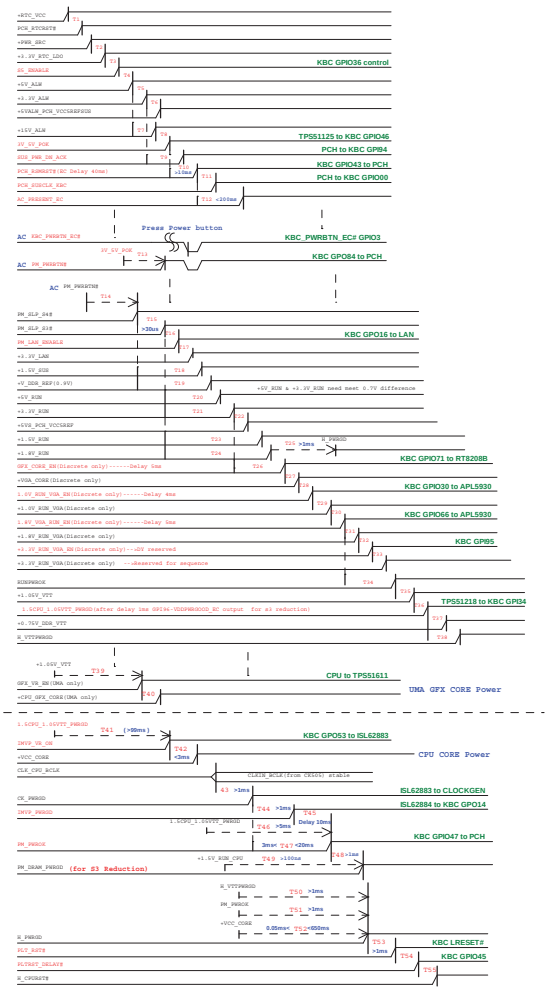
Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 98 of 102

Intel-Power Up Sequence

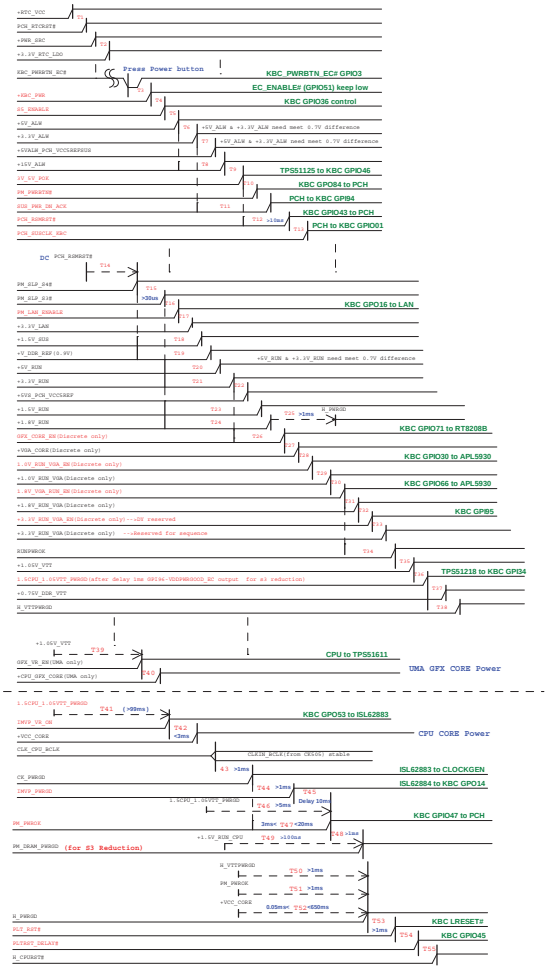
(AC mode)

red word: KBC GPIO

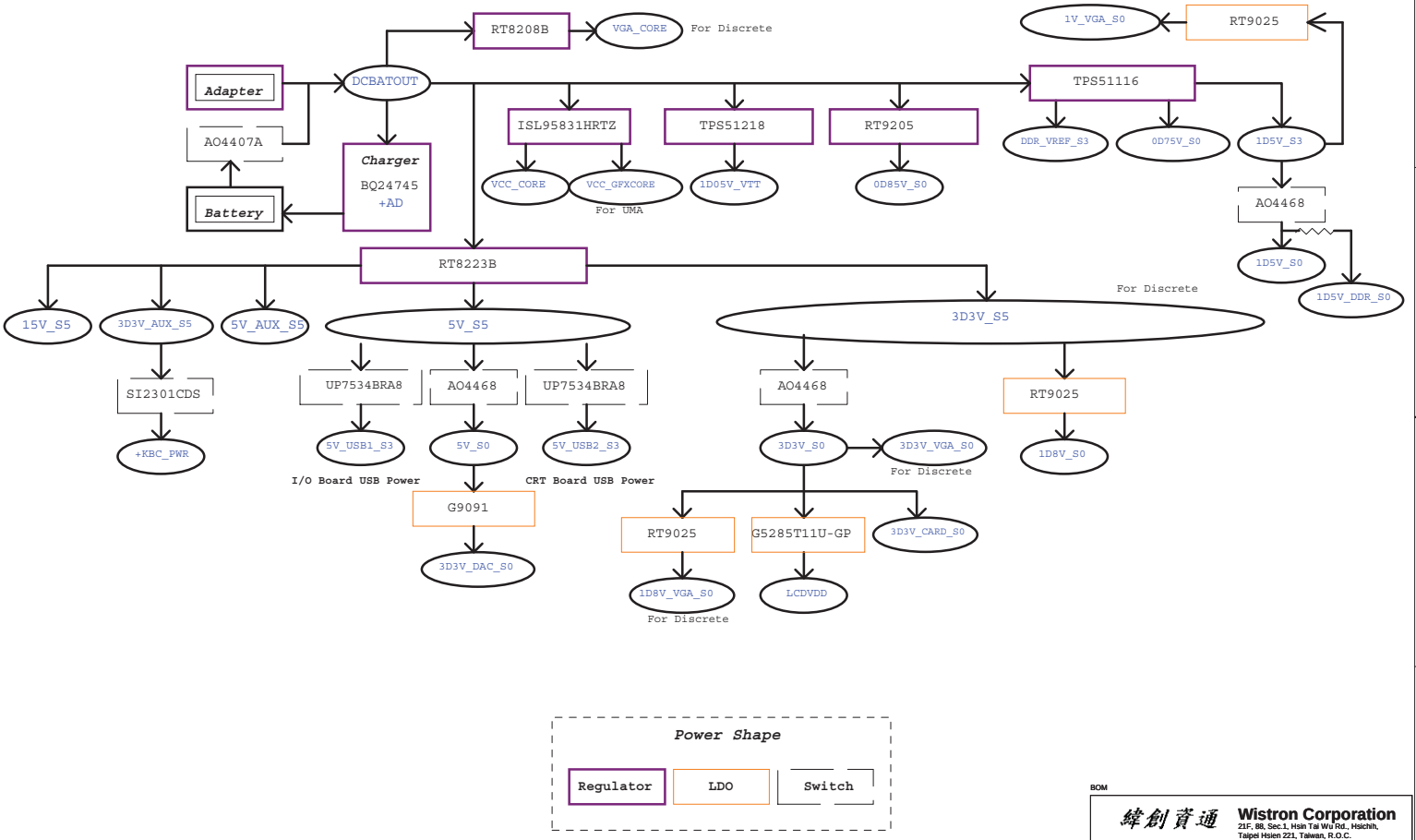


(DC mode)

red word: KBC GPIO



Wistron Corporation			
Power Sequence			
Size	Document Number		Rev
	LZ57		-3
Date:	Sheet	of	



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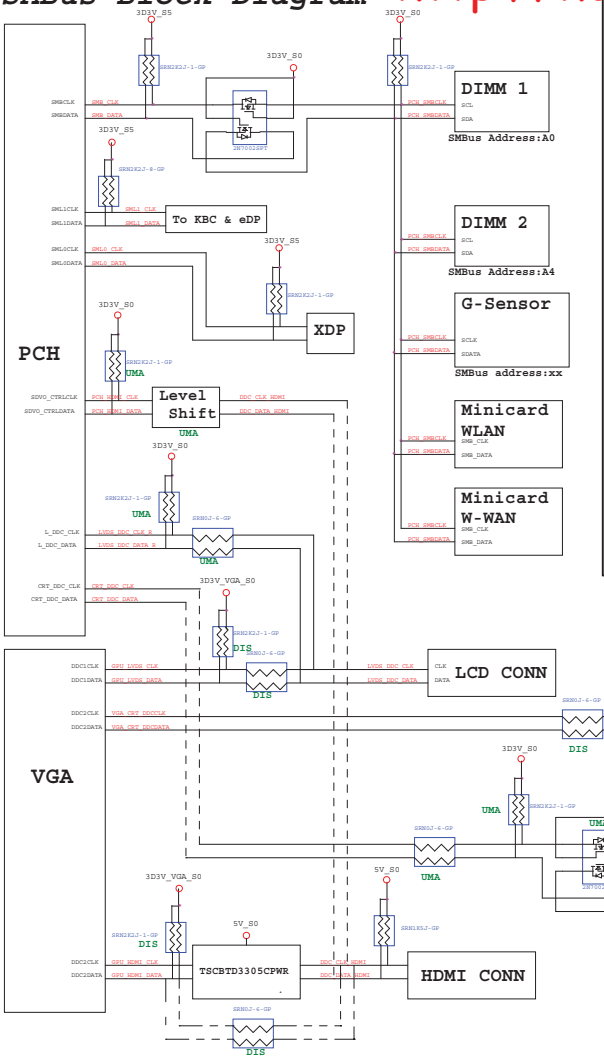
Title: **Power Block Diagram**

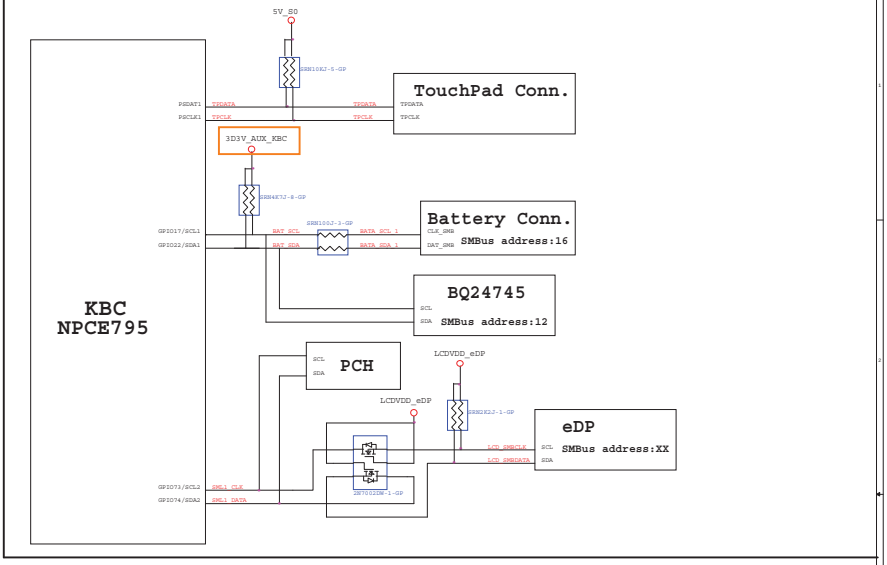
Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 100 of 102

PCH SMBus Block Diagram

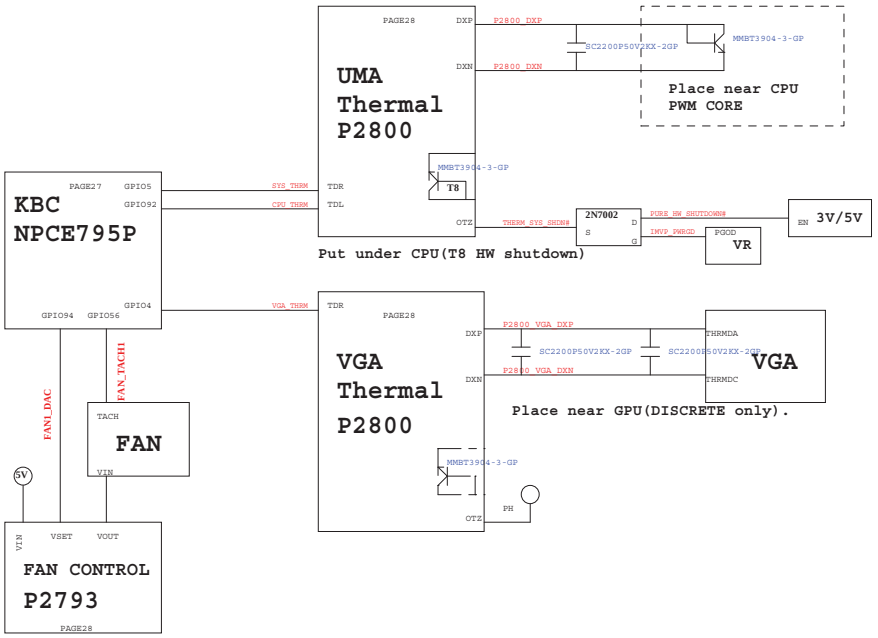


KBC SMBus Block Diagram

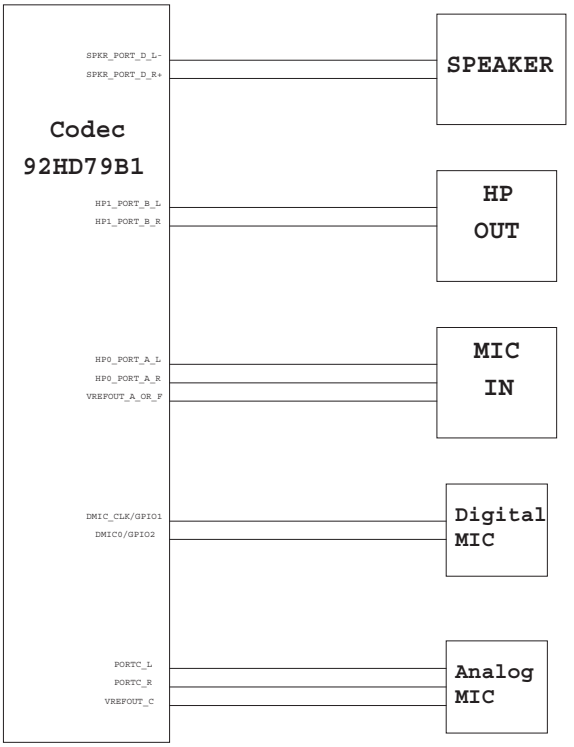


Wistron Corporation	SMBUS Block Diagram	
Size: A2	Document Number: LZ57	Rev: -1
Date: Tuesday, March 26, 2013	Sheet 1 of 1	

Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
Custom	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 102 of 102