intel®

PRELIMINARY

MCS™ 40 MICROCOMPUTER SET ADVANCE SPECIFICATIONS

Intel will soon introduce four new integrated circuits to further enhance the low-cost advantages of using the MCS-40 Microcomputer Set and allow its use in applications not before possible. These devices are both functionally and electrically compatible with current MCS-4 devices. The accompanying pages present a functional description of these new devices. Electrical specifications will be published as soon as the devices are fully characterized.

4040 — Central Processor Unit

- Functionally and electrically identical to 4004 CPU
- 14 new instuctions (60 total) including Logical Operations and Read Program Memory
- Interrupt capability
- Single step operation
- 8K byte memory addressing capability
- 24 index registers
- Subroutine nesting to 7 levels

4201 — Clock Generator

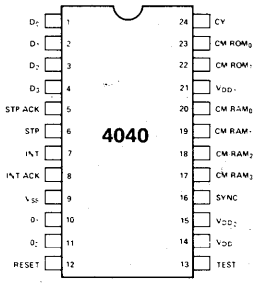
- Crystal controlled oscillator
- Directly drives MCS-4 set
- Generates power on reset for MCS-4
- Provides single step circuit for 4040

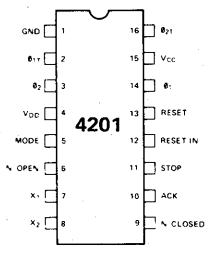
4308 — Mask Programmable ROM

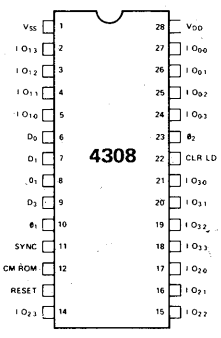
- Equivalent of (4) 4001 ROM's
- 1K x 8 program storage
- Four independent 4-bit I/O ports

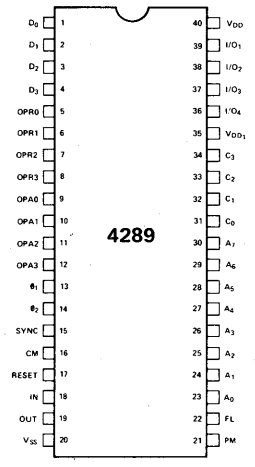
4289 — Standard Memory Interface

- Single package equivalent of 4008/4009
- Allows use of 2 μsec memories with MCS-4
- Direct interface to all standard memories: TTL, NMOS, PMOS, CMOS









THE MCS-4 USER'S MANUAL SHOULD
BE REFERENCED FOR A MORE BASIC
UNDERSTANDING OF THE SYSTEM.

4040 CENTRAL PROCESSOR UNIT

1. Introduction

The 4040 is a single chip 4-bit parallel MOS central processor. It is intended as an enhanced version of the 4004 and as such retains all of the functional capability of that device. It does, however, provide several significant improvements in hardware and software. These are listed briefly here and will be described in detail in the body of this preliminary specification.

1.1 Extended Instruction Set

The 4040 software contains all of the 4004 instruction set and includes an additional 14 instructions, providing:

- HALT
- Logical operations between accumulator and a designated index register.
- INTERRUPT DISABLE, ENABLE FUNCTIONS
- ROM BANK switching
- Index register bank switching

This instruction set is described in detail in Section 4.

1.2 Hardware Interrupt Logic

The 4040 contains the necessary hardware to accept and process single level interrupts. To facilitate this, the address stack has been increased from 4 x 12 bits to 8 x 12 bits, allowing up to seven levels of subroutine nesting. In addition, the index register array has been increased

from sixteen 4-bit registers to twenty-four 4-bit registers. The interrupt logic is explained in detail in Section 3.2.

1.3. Hardware STOP Logic

The 4040 is provided with a STOP control which allows the user to halt the processor at any instruction cycle. This feature allows the implementation of a 'single step' operation for program debugging (see Section 3.1 and Appendix II for detailed descriptions).

1.4 Expanded ROM Capacity

The 4040 can directly address up to 8K x 8 words of ROM with no external logic required.

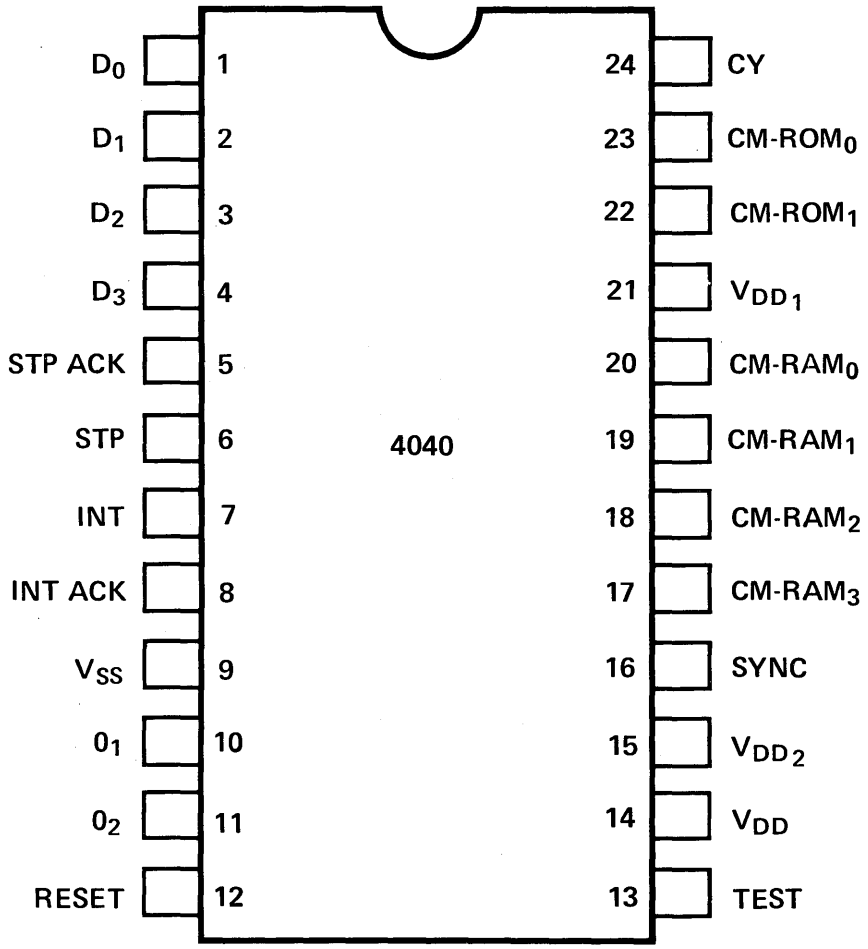
1.5 More Flexible Interface and System Configurations

The 4040 is provided with separate power supply pins for the timing circuitry and for the output buffers. These features allow a low-power standby mode by shutting off the main power supply and operating only the timing. Since the output buffers have a separate supply they can be directly interfaced to other circuit types such as N-channel MOS or CMOS. For single-supply systems all three power supply pins can be tied together.

2. General Description of Hardware

The 4040 is packaged in a 24 pin ceramic DIP. The pin configuration is shown in the following figure. A brief functional description of each pin is given in Section 2.1.

4040 PIN CONFIGURATION



2.1 Pin Description

Pin #	Designation	Description of Function
1 - 4	D_0 - D_3	Bidirectional data bus. All address and data communication between the processor and the RAM and ROM chips is handled by way of these 4 lines.
5	STPA	STOP ACKNOWLEDGE ouput. This signal acknowledges receipt that the machine has stopped. Output is "open drain" requiring pull-down resistor to V_{DD}.
6	STP	STOP input signal. A logic "1" level at this input causes the processor to enter the STOP mode.
7	INT	INTERRUPT input signal. A logic "1" level at this input causes the processor to enter the INTERRUPT mode.
8	INTA	INTERRUPT ACKNOWLEDGE output. This signal acknowledges receipt of an INTERRUPT command and prevents additional INTERRUPTs from entering the processor. INTERRUPT ACKNOWLEDGE remains active until cleared by the execution of the new BRANCH BACK and SRC (BBS) instruction. The output is "open drain", requiring a pull-down resistor to V_{DD}.

Pin #	Designation	Description of Function
9	V_{SS}	Circuit GND potential - most positive supply voltage.
10,11	ϕ_1, ϕ_2	Non-overlapping clock signals which determine processor timing.
12	RESET	RESET input. A "1" level applied to this pin clears all flag and status flip-flops and forces the program counter to 0. To completely clear all of the address and index registers, RESET must be applied for 96 clock cycles (12 machine cycles).
13	TEST	TEST input. The logical state of this input can be examined with the JCN instruction.
14	V_{DD}	Main supply voltage to the processor. Value must be V_{SS} -15.0V $\pm$ 5%.
15	V_{DD2}	Supply voltage for output buffers. May be varied depending on interface conditions.
16	SYNC	SYNC output. Synchronization signal generated by the processor and sent to ROM and RAM chips. Indicates beginning of instruction cycle.

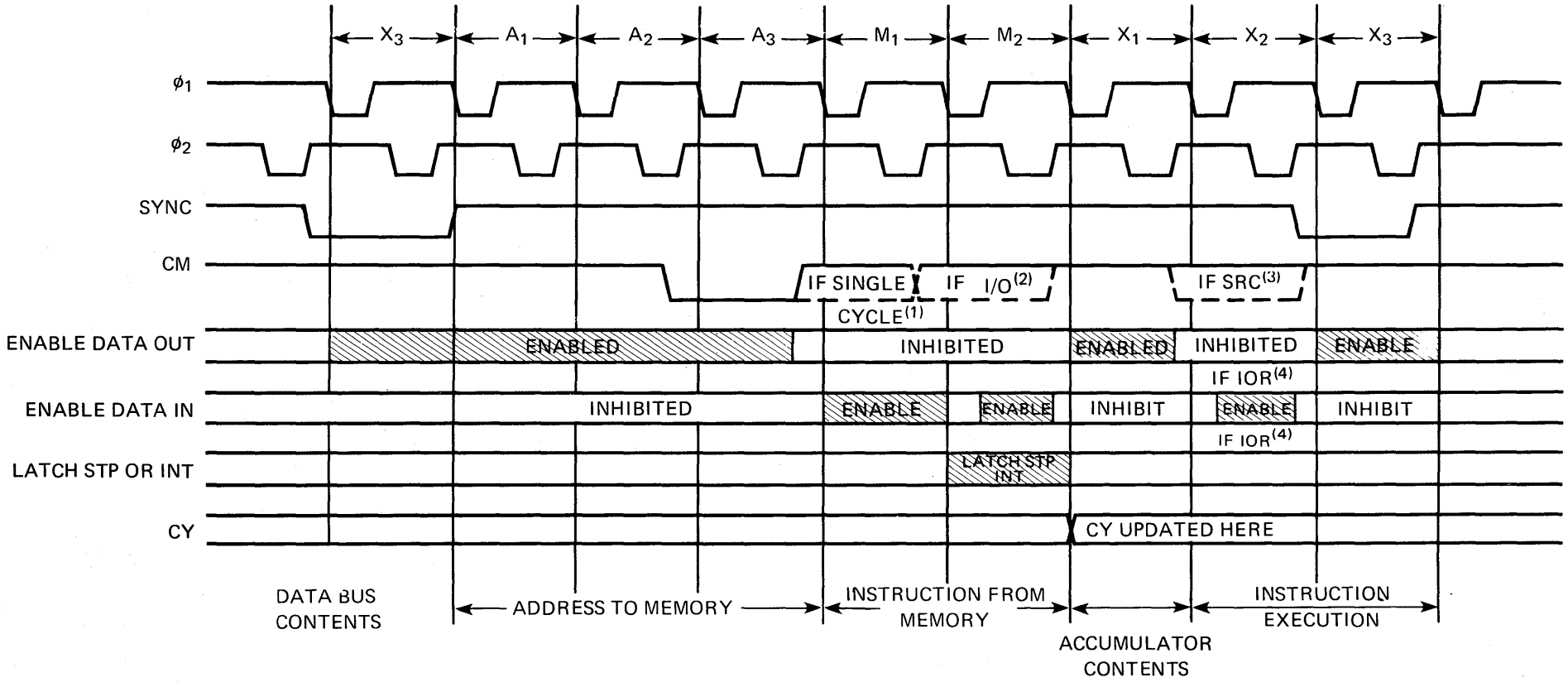
Pin #	Designation	Description of Function
17 - 20	$CM\text{-}RAM_0$ - $CM\text{-}RAM_3$	CM-RAM outputs. These outputs act as bank select signals for the 4002 RAM chips in the system.
21	V_{DD1}	Supply voltage for timing circuit. Value must be V_{SS} -15.0V $\pm$ 5%. Allows low power standby operation.
22,23	$CM\text{-}ROM_0$ - $CM\text{-}ROM_1$	CM-ROM outputs. These outputs act as bank select signals for the ROM chips in the system.
24	CY	CARRY output buffer. The state of the CY flip-flop is presented at this output and is updated at X_1. The output is "open drain" requiring a pull-down resistor to V_{DD}.

2.2 Basic Circuit Timing

The basic system timing for the 4040 is identical to that used for the 4004, as shown in the following figure. Two non-overlapping clock signals, ϕ_1 and ϕ_2, are used to define the basic timing. The start of an instruction cycle is indicated by the SYNC signal, which is generated by the processor and sent to the various ROM and RAM or peripheral chips in the system. An instruction cycle consists of the following operations:

1. The 12-bit content of the program counter is sent out to the ROM chips in three 4-bit groups during A_1, A_2, A_3.
2. The 8-bit instruction or data from the addressed ROM loca-

4040 TIMING



NOTES:

1. CM-ROM, RAM SIGNALS WILL BE PRESENT AT M_1 FOR ANY SINGLE CYCLE INSTRUCTION OR FOR THE FIRST CYCLE OF A DOUBLE CYCLE INSTRUCTION.
2. CM-ROM, RAM SIGNALS WILL BE PRESENT AT M_2 FOR ANY OF THE SIXTEEN I/O GROUP INSTRUCTIONS.
3. CM-ROM, RAM SIGNALS WILL BE PRESENT AT X_2 DURING EXECUTION OF AN SRC INSTRUCTION.
4. IOR MEANS ONE OF THE I/O READ INSTRUCTIONS: SBM, ROM, RDR, ADM, RDø, RD1, RD2, RD3.

tion is received by the processor at M_1 and M_2 at which time the instruction is decoded.

3. Instruction execution occurs during X_1, X_2, and X_3. Data or address information may be sent to output ports or RAM chips; data may be received from input ports or RAM chips; or data may be operated on within the processor.

The data bus contents at the various times of the instruction cycle are defined just as for the 4004 with the exception of the data at X_1. The 4040 outputs the contents of the accumulator at X_1 for program debugging purposes, whereas the 4004 simply copies the data which it received at M_2. The data bus contents at X_2 and X_3 depend on the instruction being executed; a listing for each individual instruction is contained in Appendix III.

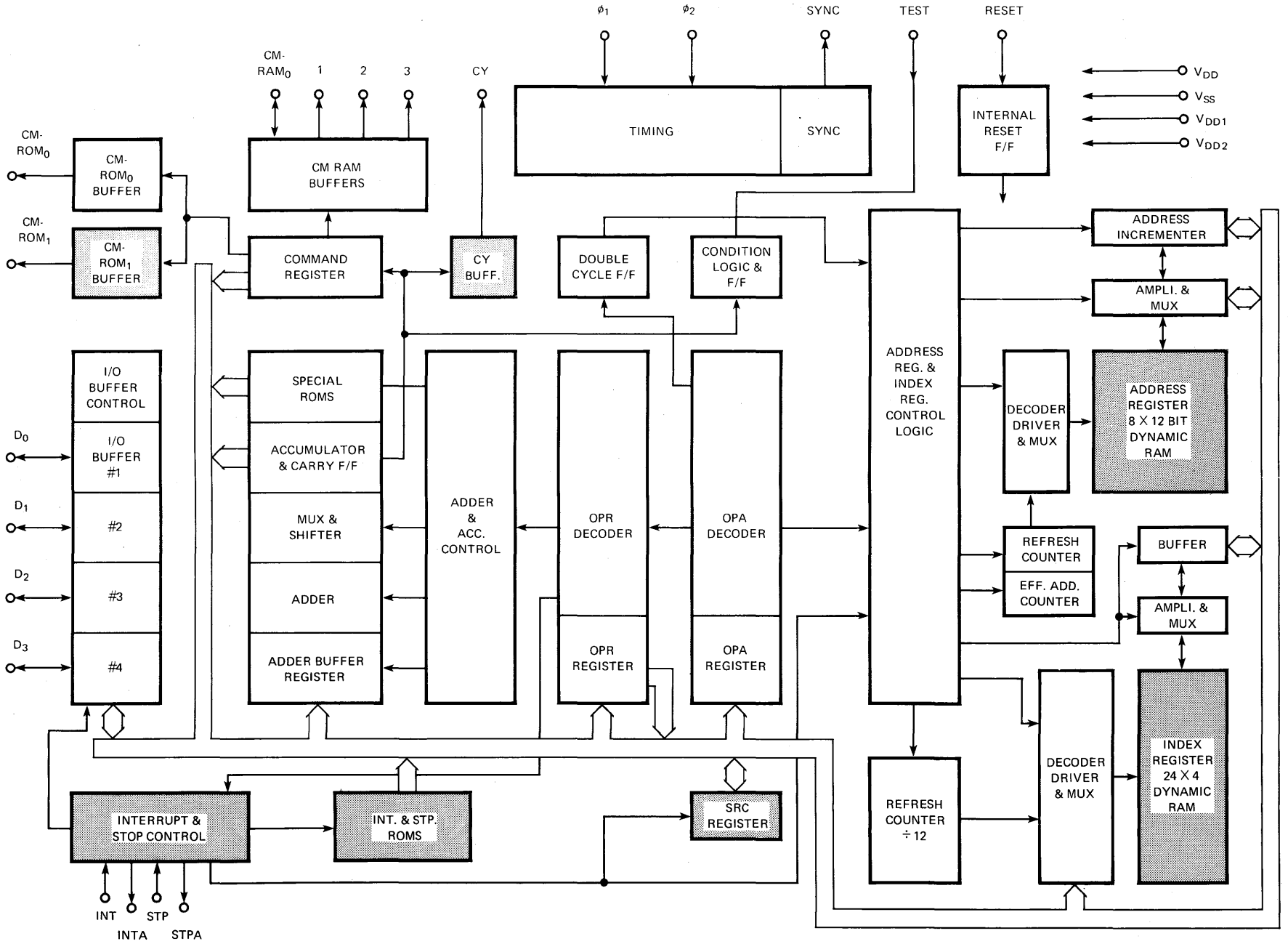
An additional change to the basic timing occurs with the generation of the CM-ROM, CM-RAM signals at M_1. This will occur for all single cycle instructions and for the first cycle of all double cycle instructions. This feature allows external logic to distinguish between instruction information and address or data at M_1 and M_2 time.

2.3 Basic Description of Major Circuit Blocks

The following figure is a block diagram of the 4040 indicating the major circuit blocks and their interconnections. The following major functional blocks are contained in the 4040:

1. Address register stack and address incrementer.
2. Index register array.
3. 4-bit adder/accumulator.

4040 BLOCK DIAGRAM



4. Instruction register/decoder and control logic.
5. Hardware interrupt and stop control.
6. Peripheral circuits for controlling timing and external communication.

A brief functional description of each of these major elements is given below.

2.3.1 Address Register and Address Incrementer

The address register is a dynamic RAM array of 8 x 12 bits operating as a push-down stack. One level of the stack is used to store the effective address, leaving seven levels available for subroutine calls and interrupt processing. The stack address is provided by the effective address counter to the decoder.

The contents of the selected address register are stored in the address buffer and multiplexed to the internal bus during A_1, A_2, and A_3 in 4-bit slices. The contents of the address buffer are incremented by a 4-bit carry-look-ahead circuit following the outputting of each 4-bit slice. The incremented value is transferred back to the address buffer and written back into the selected address register.

Since the array is dynamic, provision is made for refreshing the stored data. A 3-bit refresh counter is multiplexed to the stack decoder for this purpose.

2.3.2 Index Register Array

The index register is a dynamic RAM array of 12 x 8 bits organized as three banks of 4 x 8 bits. Two of

the banks have identical address locations and so must be individually selected with the SIBØ, 1 instructions. The third bank is always available for use. Section 3.2.1.1 describes the index register array organization in detail.

Two modes of operation are possible for the index register array. In one mode the array provides 24 directly addressable 4-bit storage locations for intermediate computation or control purposes. In the second mode the array provides 12 pairs of register locations for addressing RAM and ROM or for storing data fetched from ROM.

Index register addressing is provided by the internal bus for normal read/write operations and by a refresh counter for refresh operation. The addresses are multiplexed to the array decoder.

The content of the selected register is stored in a temporary register and multiplexed to the internal bus. During write operations the internal bus contents are transferred to the temporary register and then to the selected index register.

2.3.3 SRC Register

The SRC register is an 8-bit dynamic latch which stores the contents of the designated index register pair during the execution of the SRC instruction. This 8-bit value is sent to the ROM and RAM chips as an address

for a succeeding I/O instruction (see detailed description in Sec. 4.) The SRC register is used to hold this value in the case that an interrupt should occur, thus allowing the value to be restored when a return from interrupt is made. The SRC register is not loadable during an interrupt routine.

2.3.4 4-Bit Adder/Accumulator

The 4-bit adder is of the ripple-through carry type. One term of the addition comes from the "Adder Buffer" register which communicates with the internal bus on one side and can transfer to the adder data or $\overline{\text{data}}$. The other term of the addition comes from the accumulator and carry flip-flop. Both data and $\overline{\text{data}}$ can be transferred. The output of the adder is transferred to the accumulator and carry FF. The accumulator is provided with a shifter to implement shift right and shift left instructions. The accumulator communicates also with the command register, with special ROMs, with the condition logic, and with the internal bus. The command register holds a 3-bit code used for CM-RAM line switching. The special ROMs perform a code conversion for DAA (decimal adjust accumulator) and KBP (process keyboard) instructions. The special ROMs communicate with the internal bus. The condition logic senses ADD = 0 and ACC = 0 conditions, the state of the carry FF, and the state of an external signal (TEST) to implement JCN (jump on condition) and ISZ (increment index register skip if zero) instructions.

2.3.5 Instruction Register/Decoder and Control Logic

The instruction register is loaded with the content of the internal bus at M_1 and M_2 through a multiplexer and holds the instruction fetched from ROM. The instructions are decoded in the instruction decoder and appropriately gated with timing signals to provide the control signals for the various functional blocks. A single cycle FF is reset from one of 5 double-length instructions. Double-length instructions are instructions that need two system cycles (16 clock cycles) for their execution. A condition FF controls JCN and ISZ instruction and is set by the condition logic.

2.3.6 INTERRUPT and STOP Control Logic

The 4040 is provided with hardware INTERRUPT and STOP controls which override the normal processor operation. The INTERRUPT logic detects and acknowledges the presence of an INTERRUPT signal and forces the processor to execute a JMS instruction to location 003. Section 3.2 discusses in detail the timing and operation of the INTERRUPT control as well as the additional 4040 features which enhance its use. Examples of INTERRUPT processing routines are given in Appendix 1B.

The STOP control logic behaves in a similar manner by detecting and acknowledging the presence of a STOP signal. The processor is forced to execute a NOP instruction and will remain in the STOP condition

until the STOP signal is removed. Section 3.1 presents a detailed description of the STOP/HALT operating mode.

2.3.7 Peripheral Circuits

This includes:

a. The data bus input-output buffers communicating between data pads and internal bus.

b. Timing and SYNC generator.

c. 2 CM-ROM and 4 CM-RAM output buffers.

d. POWER-ON-CLEAR flip-flop.

During RESET, all RAMs and static FF's are cleared, and the data bus is set to "0". After RESET, program control will start from "0" and $CM\text{-}ROM_{\emptyset}$, $CM\text{-}RAM_{\emptyset}$ will be selected. In addition, the INTERRUPT logic will be disabled and INDEX register bank $\emptyset$ will be selected.

3. 4040 New Operating Features

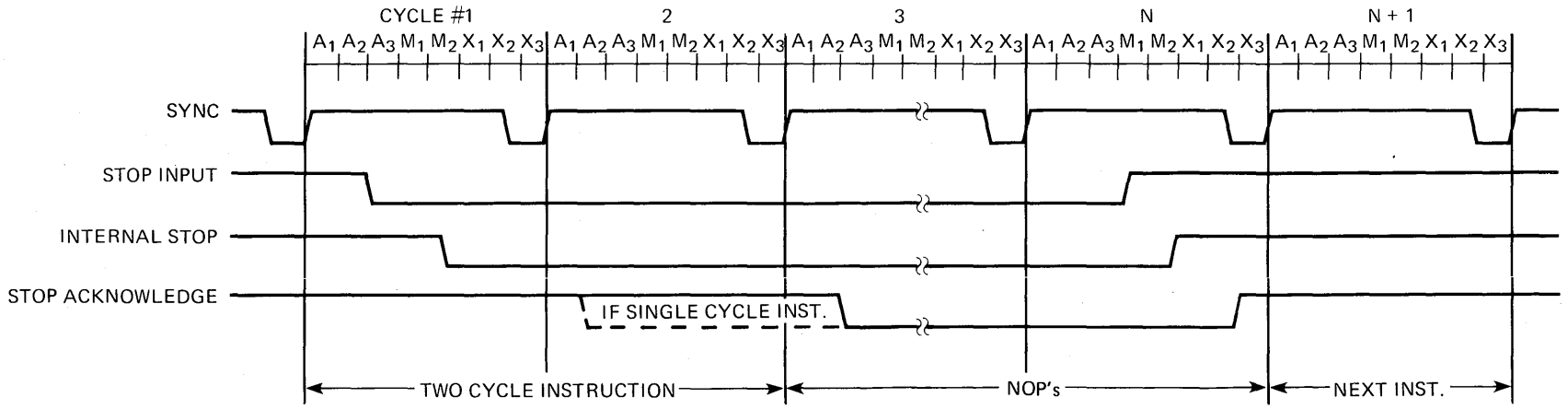
The following features will be described in detail:

- STOP/HALT mode logic
- INTERRUPT mode logic
- Extended ROM addressing capability

3.1 STOP/HALT Mode Operation

The normal processor cycle of the 4040 may be "stopped" at any point in an instruction sequence by one of two methods. A logic "1" level may be applied to the STOP input pin, in which case the processor will complete the current instruction and then enter the STOP mode. The timing for this operation is shown in the following figure and the sequence of events is outlined below:

STOP TIMING


CYCLE #1
2
3
N
N + 1
A1 A2 A3 M1 M2 X1 X2 X3
SYNC
STOP INPUT
INTERNAL STOP
STOP ACKNOWLEDGE
IF SINGLE CYCLE INST.
TWO CYCLE INSTRUCTION
NOP's
NEXT INST.

a. During instruction cycle #1 the state of the STOP pin is gated into the internal STOP latch at M_2.

b. At A_1 of the next single cycle instruction the STOP flip-flop will be set. In the example shown, the processor was executing a double cycle instruction when the STOP signal was first applied. It was allowed to complete the full instruction, hence the STOP flip-flop was not set until A_1 of instruction cycle #3. The buffered output of the STOP flip-flop is used as a STOP ACKNOWLEDGE signal.

c. During instruction cycle #3 and all succeeding instruction cycles, the content of the program counter is sent out at A_1, A_2, and A_3. The program counter is not allowed to increment, however, effectively "stopping" the processor at a give location. In addition the data bus input buffers are prevented from receiving information at M_1 and M_2 times and a NOP instruction is forced on the internal data bus.

d. The processor remains in this NOP loop until the external STOP signal is returned to a logic "0" level during instruction cycle N. The new information is gated into the STOP latch at M_2, allowing the STOP flip-flop to reset at X_3 of the instruction cycle N. Normal processor operation resumes at instruction cycle N + 1.

3.1.1 HALT Mode

Entry to the STOP mode may also be gained through the use of the HALT (HLT) instruction as shown in the following figure. In this case the processor executes

the HLT instruction and causes the HALT and STOP flip-flops to be set at X_3 of instruction cycle #1. The processor is forced to execute NOP's at instruction cycle #2 and all successive cycle times until removed from the HALT mode.

Exit from the HALT mode can be gained in two ways, one of which is also shown in the following figure. At instruction cycle #N, a logic "1" level is applied to the STOP input and is in turn latched by the STOP latch at M_2. A logic "1" in the STOP latch causes the HALT flip-flop to be reset at A_1 of cycle #n + 1. The processor is now in the normal STOP mode and can be released as described in (d) above.

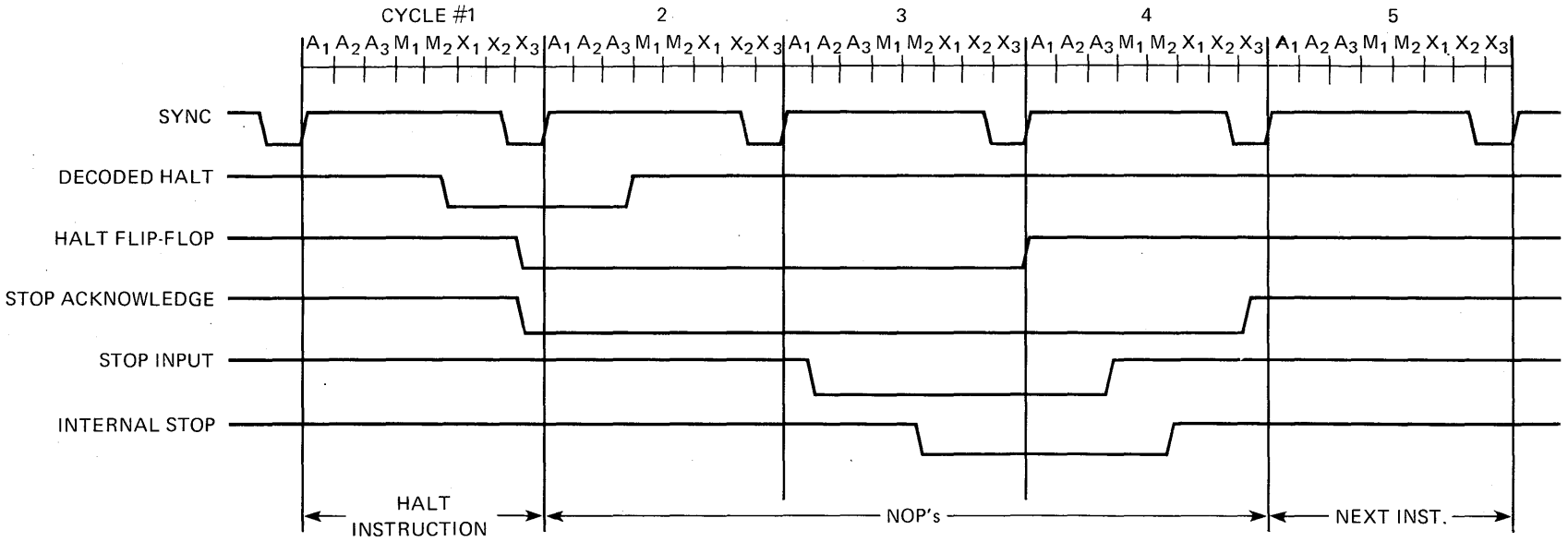
The second means of exiting from the HALT condition is by way of the INTERRUPT input and will be described in Section 3.2.

3.1.2 DATA BUS Contents

The data bus contents during STOP/HALT mode are shown. For program debugging purposes the following information is available:

A_1, A_2, A_3	12-bit address from internal program counter.
M_1, M_2	8-bit instruction from addressed ROM location. Internally the processor executes NOP.
X_1	4-bit contents of ACCUMULATOR.
X_2, X_3	8-bit contents of internal SRC register

HALT TIMING
(EXIT USING STOP INPUT)



which stores the value of the last SRC address. CM-ROM and CM-RAM signals are not present at X_2 in this case. (See Section 3.2 for complete description of operation of SRC register.)

3.1.3 Single Step Operation

The STOP control provides a convenient means of program debugging by allowing a "single step" operation. Appendix II describes the necessary hardware and timing.

3.2 INTERRUPT Mode

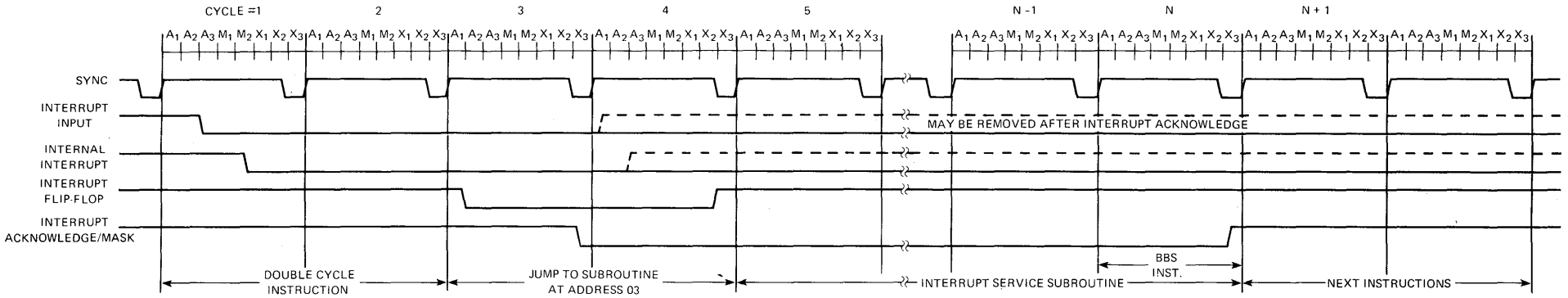
The 4040 is provided with an asynchronous INTERRUPT input and an INTERRUPT ACKNOWLEDGE output. The following figure presents the basic timing for the INTERRUPT mode. The sequence of events is as follows:

a. During instruction cycle #1 an INTERRUPT occurs and is gated into the INTERRUPT LATCH during M_2.

b. At A_1 of the next single cycle instruction the INTERRUPT flip-flop is set. As in the case of the STOP example, if the processor is executing a double cycle instruction it is allowed to complete it.

c. During instruction cycle #3 the program counter is prevented from incrementing and the data input buffers are inhibited at M_1 and M_2. A JUMP TO SUBROUTINE (JMS) instruction is forced on the internal data bus. The subroutine address is forced to be page 0, location 3. At X_3 the INTERRUPT ACKNOWLEDGE flip-flop is set and its

INTERRUPT TIMING



buffered output is available on the INTERRUPT ACKNOWLEDGE pin. The instruction at location 0, 3 begins the interrupt processing routine.

d. The INTERRUPT ACKNOWLEDGE flip-flop remains set until the interrupt has been processed and the new BRANCH BACK & SRC (BBS) instruction has been executed (instruction cycle #N). No new INTERRUPT can be entered while INTERRUPT ACKNOWLEDGE is active. Note that the INTERRUPT signal may be removed after INTERRUPT ACKNOWLEDGE occurs.

3.2.1 Saving and Restoring Processor Status

To have an effective interrupt handling capability the processor must be capable of saving current program and status register values and restoring same when the interrupt processing is complete. In the 4040 the following values must be saved:

a. Content of ACCUMULATOR and CARRY flip-flop.
b. Content of COMMAND REGISTER.
c. Content of as many INDEX REGISTERS as required.
d. The value of the last SRC address sent out prior to interrupt.
e. Content of the PROGRAM COUNTER.
f. The current ROM bank ($CM\text{-}ROM_0$ + $CM\text{-}ROM_1$).

To facilitate the items listed, a number of new hardware features have been included in the 4040 and are described in the following paragraphs.

3.2.1.1 Expanded Index Register Array

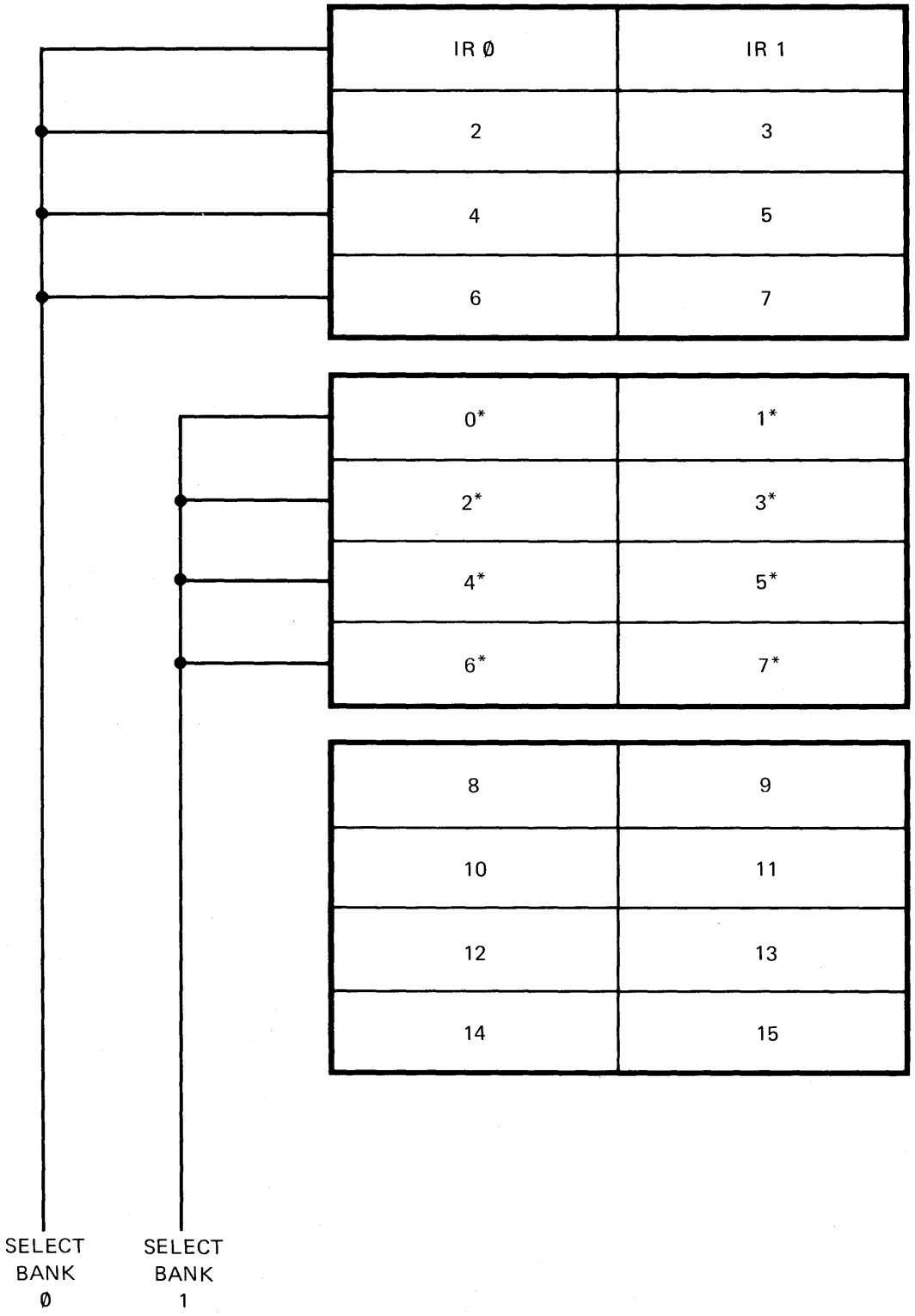
Saving status values requires having temporary storage locations available in the index

register array. For this reason the 4040 is provided with 8 additional index registers (4 register pairs) providing a total of 24 4-bit registers (12 8-bit register pairs). The array is organized into three 8 register banks. Bank Ø and Bank 1 are individually selectable by using the SELECT INDEX BANK (SBØ, SB1) instructions. The upper bank, that one containing registers 8 - 15, is always available for storage. Appendix I.b provides examples of interrupt routines and demonstrates the use of the index register banks as well as all other features listed here.

Note that both Bank Ø and Bank 1 contain the same individual address locations. This feature allows those instructions which reference specific register locations to be executed from either index register bank. Thus the JUMP INDIRECT (JIN) instruction and the logical instructions OR4, OR5, AN6, AN7 reference two different sets of registers, e.g. a JIN instruction can reference register pair #0 in Bank Ø or in Bank 1.

The BANK SELECT flip-flop is automatically saved and restored during interrupts. Thus a user may wish to operate

INDEX REGISTER ORGANIZATION



in Bank Ø until interrupted then switch to Bank 1. When the BBS instruction is executed to return from interrupt, previous Bank will automatically be selected for the next instruction.

After application of a RESET signal, Bank Ø will be selected.

3.2.1.2 SRC Register

When the 4040 executes an SRC instruction, the 4-bit values sent out at X_2 and X_3 are stored internally in the 8-bit SRC register. The SRC register is locked out during the interrupt routine by the INTERRUPT ACKNOWLEDGE flip-flop. Thus, any SRC instruction executed during an interrupt routine will not affect the value in the SRC register. The last instruction in the interrupt routine must be a BRANCH BACK and SRC (BBS), another new instruction which restores the program counter (see below) and sends out the contents of the SRC register at X_2 and X_3, and generates the appropriate CM-ROM and CM-RAM at X_2. This restores the ROM and RAM select logic to their pre-interrupt conditions.

3.2.1.3 Extended Address Register Stack

The address stack of the 4040 is an 8 x 12 bit array (compared to 4 x 12 bits in the 4004). One level of the stack is required for the

program counter; hence seven levels of subroutines may be nested using the 4040.

When an interrupt occurs the program counter is not incremented, but is stored down one level in the stack by the execution of the forced JMS instruction. This value is restored by the execution of the BBS instruction at the end of the interrupt routine.

3.2.1.4 General Information Applying to Interrupt

- The 4040 is capable of servicing one interrupt at a time. The INTERRUPT ACKNOWLEDGE signal is used internally to prevent a second interrupt from being entered until the first is completely serviced.

- Two instructions, INTERRUPT ENABLE (EIN) and INTERRUPT DISABLE (DIN) are provided for protecting sequences of instructions from being interrupted. These are described in detail in Section 4.

- The RESET signal serves to disable interrupt. If the processor is started from a RESET condition an EIN instruction must be performed before an interrupt will be recognized.

- If an INTERRUPT and STOP signal occur such that they are both latched at M_2 of the same instruction cycle, the STOP logic will have

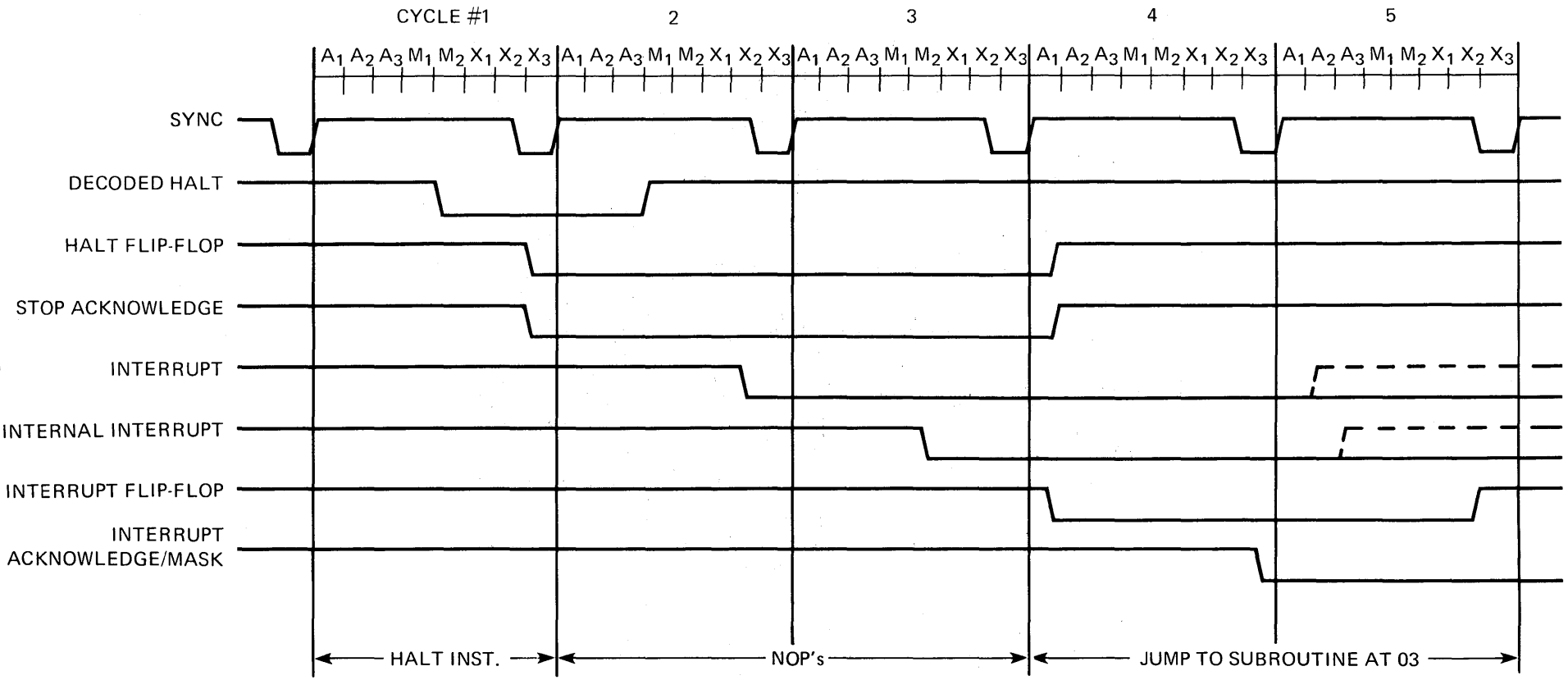
priority, and must be cleared before the interrupt can be recognized.

As mentioned in Section 3.1.2 the INTERRUPT control may be used to exit from a HALT condition. The timing for this is shown. The processor enters the HALT mode at instruction cycle #1 and remains in that mode until the INTERRUPT signal is recognized at instruction cycle #4. When the INTERRUPT flip-flop is set, it causes the HALT flip-flop to be reset. The processor is then in the INTERRUPT mode. In this way a processor could be used in a completely asynchronous control application in which the INTERRUPT signal would begin the processing routine. When the routine was complete the processor would execute the HLT instruction and wait for a new INTERRUPT.

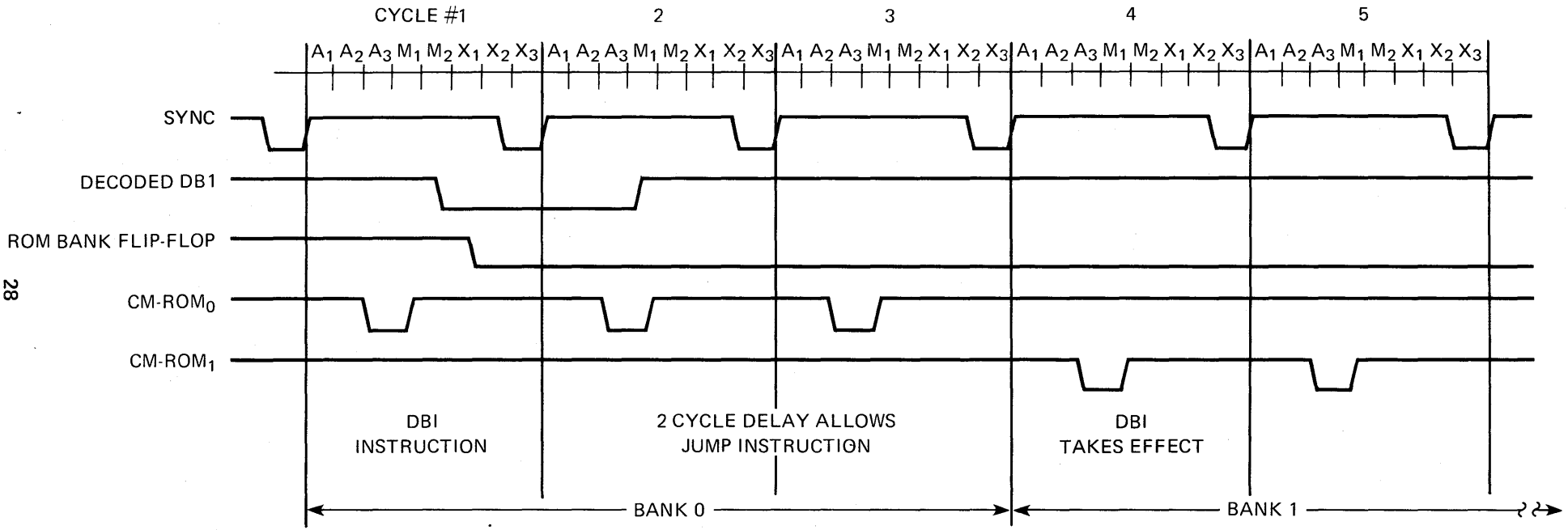
3.3 Extended ROM Addressing Capability

The 4040 is equipped with two CM-ROM output buffers, each of which can be used to select a bank of sixteen 256 x 8 ROMs. A total of 8K x 8-bit words can be directly addressed. Bank switching is accomplished through the use of two new instructions, DESIGNATE BANK Ø (DBØ) and DESIGNATE BANK 1 (DB1). Both of these instructions take effect on the third cycle following their execution. Appendix I.a provides example

HALT TIMING
(EXIT USING INTERRUPT)



ROM BANK SWITCHING



uses of the DBØ, 1 instructions.

Since the INTERRUPT control logic will force a JMS to page Ø, location 3, the first few instructions of the interrupt routine will have to be duplicated in both ROM banks (see Appendix I.b).

The fact that the bank switching operation requires three instruction cycles to be completed means that an INTERRUPT cannot occur during those three cycles. For this reason the INTERRUPT logic is internally disabled during the execution of DBØ or DB1.

4. Definition of Instruction Set

The 4040 is functionally compatible with the 4004 and therefore recognizes all 46 instructions valid for the 4004. In addition, the 4040 recognizes 14 new instructions giving a total of 60 instructions in the set. The instruction format is, of course, identical to that used in the 4004.

Four groups of instructions can be defined as follows:

a. Machine Instructions - This group of 16 instructions are designated by an OPR code of 0000 - 1101. Within this group is contained a second group which is designated supplemental group.

b. Supplemental Group - This group of 14 instructions is designated by an OPR code of 0000 and an OPA code of 0001 - 1110. These are the new instructions which have been added to the 4040.

c. I/O Group - Designated by an OPR code of 1110, this group of 16 instructions is used for transferring data between the processor and the RAM chips or I/O circuits.

d. Accumulator Group - This group of 14 instructions is designated by an OPR code of 1111 and operates only on the accumulator/carry flip-flop, the special ROMs and the command register.

The 4004 instruction set is well documented elsewhere (see MCS-4 Users' Manual) and therefore will not be described here.
The new supplemental group will be described in detail below:

4.1 New Instructions for 4040 - Detailed Description

MNEMONIC	OPR	OPA	DESCRIPTION
HLT	0000	0001	The processor sets the HALT and STOP flip-flops. Program counter incrementer and data input buffers are inhibited. The processor executes NOP continuously; continuation can occur by means of STOP or INTERRUPT control.
BBS	0000	0010	This instruction is a combination of BRANCH BACK and SRC. The effective address counter is decremented and program control is returned to the location saved by the forced JMS which occurred during the interrupt routine. In addition, the content of the SRC register is sent out at X_2 and X_3 of the instruction cycle, thus restoring

MNEMONIC	OPR	OPA	DESCRIPTION
			the I/O port or RAM location address.
LCR	0000	0011	The 4-bit contents of the COMMAND REGISTER are transferred to the ACCUMULATOR. This allows saving the command register values before processing the interrupt.
OR4	0000	0100	The 4-bit contents of index register #4 are logically "OR-ed" with the ACCUMULATOR. The result is placed in the ACCUMULATOR and the CARRY flip-flop is unaffected. Logically the result is : $ACC_n \leftarrow ACC_n + IR4_n$
OR5	0000	0101	The 4-bit contents of index register #5 are logically "OR-ed" with the ACCUMULATOR.
AN6	0000	0110	The 4-bit contents of index register #6 are logically "AND-ed" with the ACCUMULATOR. The result is placed in the ACCUMULATOR and the CARRY IS unaffected. Logically the result is: $A_{CCn} \leftarrow ACC_n \cdot IR6_n$

MNEMONIC	OPR	OPA	DESCRIPTION
AN7	0000	0111	The 4-bit contents of index register #7 are logically "AND-ed" with the ACCUMULATOR.
DBØ	0000	1000	DESIGNATE ROM BANK Ø. The most significant bit of the COMMAND REGISTER, CR_3, is reset. On the third instruction cycle following its execution,it causes CM-ROMØ to be activated.
DB1	0000	1001	DESIGNATE ROM BANK 1. The most significant bit of the COMMAND REGISTER, CR_3, is set. On the third instruction cycle following its execution, it causes CM-ROM1 to be activated.
SBØ	0000	1010	SELECT INDEX REGISTER BANK Ø. The index register bank select flip-flop is reset. Index registers 0 - 7, 8 - 15 will be available for program use.
SB1	0000	1011	SELECT INDEX REGISTER BANK 1. The index register bank select flip-flop is set. Index registers 0* - 7*, 8 - 15 will be available for program use.

MNEMONIC	OPR	OPA	DESCRIPTION
EIN	0000	1100	ENABLE INTERRUPT. Internal interrupt detection logic is enabled.
DIN	0000	1101	DISABLE INTERRUPT. Internal interrupt detection logic is disabled.
RPM	0000	1110	READ PROGRAM MEMORY. This instruction can be used only with the 4289 Standard Memory and I/O Interface Chip. The contents of the previously selected half-byte of program memory are transferred to the 4040 and loaded to the ACCUMULATOR. A First/Last sequence flip-flop regulates the transfer. Two RPMs are required for instruction fetch.

APPENDIX I

PROGRAMMING EXAMPLES

I. USE OF DBØ AND DB1

The DB instructions present a convenient method of switching from one ROM bank to another. As shown in the following examples the bank switch is delayed until the 3rd instruction cycle after the DB is executed.

EXAMPLE A

ROM Location* Bank / Page / Word			Instruction	Comment
0	2	107	X X X	
0	2	108	DB1	Designate Bank 1.
0	2	109	JUN 1	
0	2	110	27	During this instruction cycle a "1" is loaded in bit #3 of the command register.
1	1	27	X X X	JUN occurred to Bank 1 because $CM\text{-}ROM_1$ has been activated.
.			.	
.			.	
.			.	
1	1	63	DBØ	Designate Bank Ø.
1	1	64	ISZ 3	
1	1	65	151	
0	1	66	X X X	Program jumps here if $(IR_3) = 0$.
0	1	151	X X X	Program jumps here if $(IR_3) \neq 0$.

* Bank # 0, 1
Page # 0 - 15
Word # 0 - 255

EXAMPLE B

ROM Location Bank / Page / Word			Instruction	Comment
0	7	131	X X X	
0	7	132	DB1	Designate Bank 1.
0	7	133	JMS 2	
0	7	134	96	Address 7, 135 saved in stack.
1	2	96	X X X	JMS occurs to 1, 2, 96 since
.		.	.	CM-ROM, is activated at this
.		.	.	instruction cycle.
.		.	.	
1	2	170	DBØ	Designate Bank Ø.
1	2	171	XCH 7	
1	2	172	BBL	Address 7, 135 pulled from stack and placed in PC; branch back
0	7	135	X X X	occurs to 7, 135 in Bank Ø because $CM\text{-}ROM_0$ is activated during this instruction cycle.

II. INTERRUPT PROCESSING

An interrupt processing routine is, in general, composed of three parts:

a) The instructions required to save the current processor status.

b) A portion which determines and services the interrupting device.

c) The instructions required to restore program control to the pre-interrupt conditions.

In the first example, the processor is used with a single ROM bank, and index register Bank 1 is used to save status (accumulator/carry, command register). The six remaining registers in IR Bank 1 are available for interrupt servicing. In addition to being relatively simple, this scheme has the advantage of saving processor status with the fewest number of instructions. Note that since only one ROM bank is available, it is only necessary to save the lower three bits of CR. This allows saving the CR and CY in the same register location.

In Example B, both ROM banks are used and all eight registers of IR Bank 1 are required to service the interrupt. Since the forced JMS instruction can occur in either ROM bank, the instructions

required to save ACC and CR must be located in each bank. If more than eight register locations are required for interrupt servicing, additional instructions will be required to save the values of the upper eight IR.

EXAMPLE A

ROM Location Bank	Page	Word	Instruction	Comment
0	6	82	SRC 4	(IR 8,9) sent to ROM & RAM, Load SRC Reg.
0	6	83	INC 9	Interrupt occurs here.
0	6	84	(JMS Ø)	Interrupt acknowledged, 6,84
0	6	84	(3)	saved in stack; instruction at 6,84 ignored.
0	0	3	SB1	Select IR Bank 1.
0	0	4	XCH 7	(ACC)→IR7* - ACC saved.
0	0	5	LCR	(CR)→ACC
0	0	6	RAL	(CY)→Acc_0, Acc_0→Acc_1...Acc_3→CY
0	0	7	XCH 6	(ACC)→IR6* CY, ^{0}CR saved.
0	0	8		
0	0	9	.	Routine for determing and
	.		.	servicing interrupt is executed
	.		.	here.
	.		.	
0	P	n	XCH 6	(IR6*)→ACC
		n+1	RAR	ACC_0→CY - CY restored
		n+2	DCL	ACC_0→CR_0, ACC_1→CR_1, ACC_2→CR_2, CR restored.
		n+3	XCH 7	(IR7*)→ACC
		n+4	SBØ	Select IR Bank Ø.
		n+5	BBS	Address 6,84 loaded into PC; contents of SRC register sent out;
0	6	84	WRM	program restored.
			.	
			.	
			.	

APPENDIX II

SINGLE STEP MODE

Fig. C1 shows a possible circuit configuration for operating in single step mode. The circuit uses the positive going (turn-off) edge of STOP ACKNOWLEDGE to generate a new STP signal. Operation is as follows:

(a) With the toggle switch in the SINGLE-STEP position, the line STP is at a logic "1" level and the processor is in the STOP mode.

(b) Depressing the single-step push button causes a negative going pulse to be generated at point (A), in turn causing STP to return to a positive level. The duration of this pulse is determined by the R/C combination and must be greater than one instruction cycle.

(c) The processor will cause STPA to return to a logic "0" level indicating that it is no longer in STOP mode. This signal is inverted and then used to reset the O/S causing STP to return to logic "1".

(d) The "new" STP signal will be latched up and acknowledged after one instruction has been executed.

SUGGESTED SINGLE STEP FEATURE IMPLIMENTATION

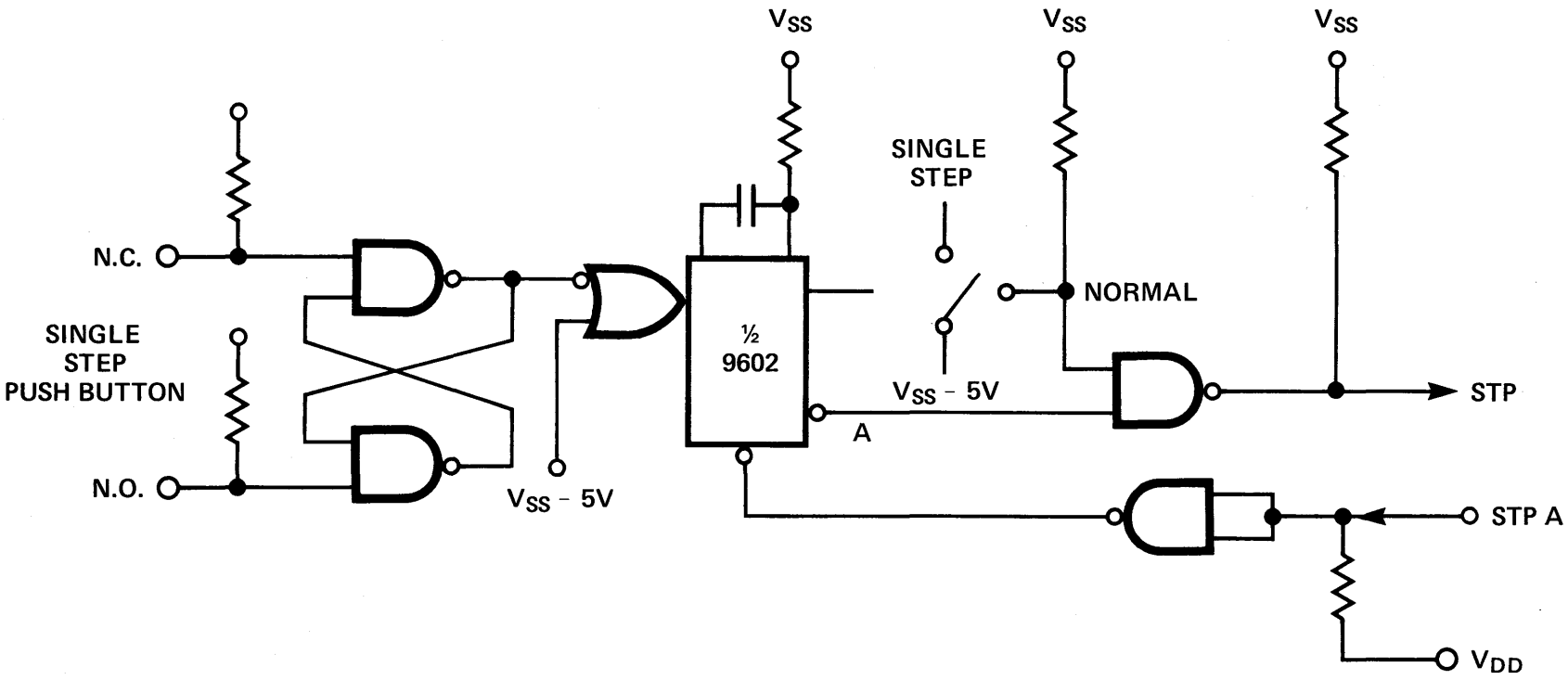


Figure C1

APPENDIX III

INSTRUCTION	DATA @ X_2 D_3 D_2 D_1 $D_\emptyset$	DATA @ X_3 D_3 D_2 D_1 $D_\emptyset$	COMMENTS
NOP	1 1 1 1	1 1 1 1	
HLT	1 1 1 1	1 1 1 1	After execution of HLT, processor enters STOP mode.
BBS	(SRCH)	(SRCL)	(SRCH) means contents of 4 high order bits of SRC register.
LCR	(COM. REG)	1 1 1 1	
OR4	(0100)	1 1 1 1	
OR5	(0101)	1 1 1 1	
AN6	(0110)	1 1 1 1	
AN7	(0111)	1 1 1 1	
DBØ	1 1 1 1	1 1 1 1	
DB1	1 1 1 1	1 1 1 1	
SBØ	1 1 1 1	1 1 1 1	
SB1	1 1 1 1	1 1 1 1	
E1N	1 1 1 1	1 1 1 1	
D1N	1 1 1 1	1 1 1 1	
RPM	(P.M.)	(P.M.)	Program memory content

4201 CLOCK GENERATOR

1.0 Introduction

The 4201 is a CMOS MSI integrated circuit designed to fill the clock requirements of the MCS-4 microcomputer set. The 4201 contains a crystal controlled oscillator (XTAL external), clock generation circuitry, and both MOS and TTL level clock driver circuits.

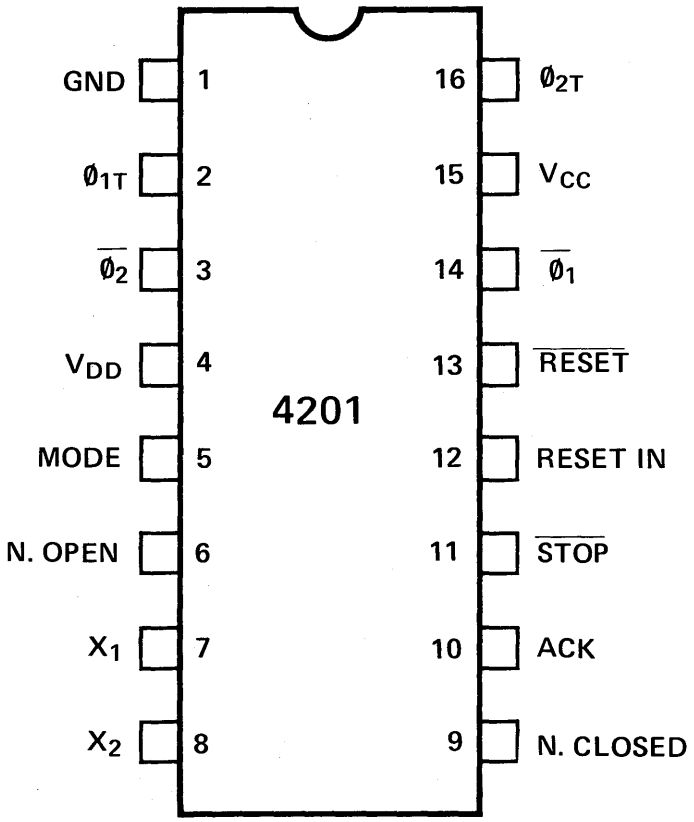
The 4201 also performs the power on reset function required by MCS-4 components and provides the logic necessary to implement the single-step function of the 4040 central processor unit.

2.0 Hardware Description

The 4201 is packaged in a 16-pin plastic DIP. The pin configuration is shown in the following figure, and a functional description of each pin is given below:

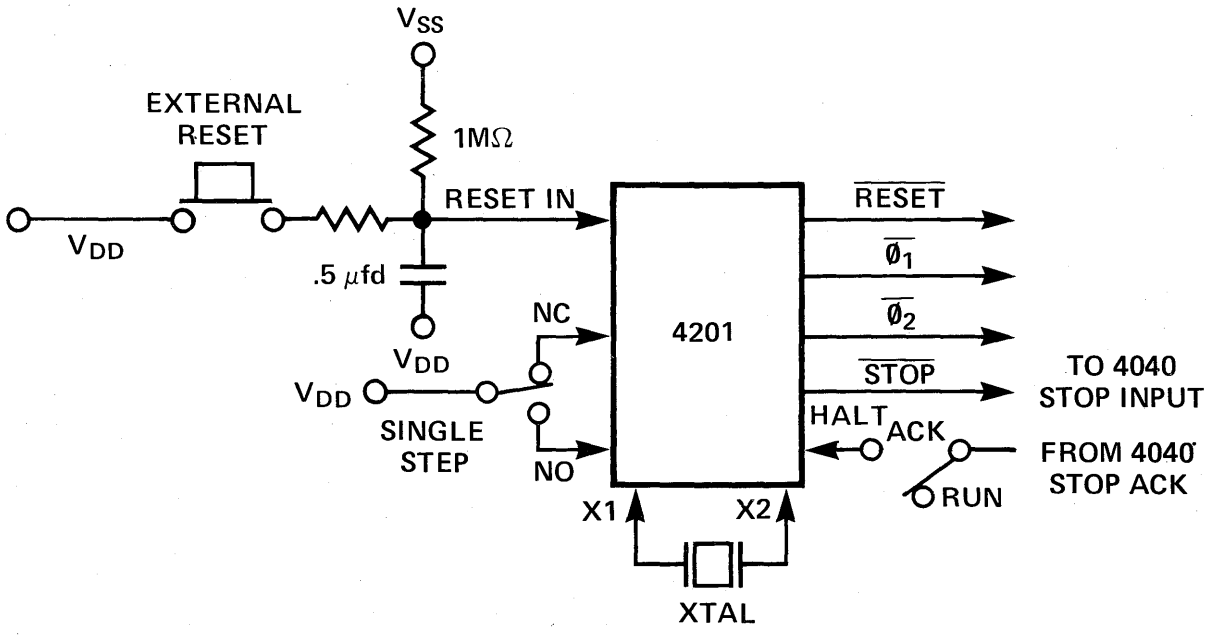
Pin #	Designation	Description
1	GND	Circuit ground potential
2	Ø1T	Phase 1 TTL level clock output (2ma-sink).
3	$\overline{Ø2}$	Phase 2 MOS level clock output. Directly drives all MCS-4 components (up to 250pf).
4	V_{DD}	Main Power Supply Pin. $V_{DD} = V_{SS}$-15V±5%
5	MODE	Counter mode control pin. Determines whether counter divides basic frequency by 4 or 7. Model 1 = V_{SS} Model 2 = V_{DD}

4201 PIN CONFIGURATION



6	N. OPEN	Input of single step circuitry to which normally open contact of SPDT switch is connected.
7	X1	External Crystal Connection
8	X2	External Crystal Connection
9	N. CLOSED	Input of single step circuitry to which normally closed contact of SPDT switch is connected.
10	ACK	Acknowledge input to single step circuitry normally connected to stop acknowledge output of 4040.
11	$\overline{\text{STOP}}$	Stop output of single step circuitry normally connected to stop input of 4040.
12	RESET IN	Input to which RC network is connected to provide power-on reset timing.
13	$\overline{\text{RESET}}$	Reset signal output which directly connects to all MCS-4 reset inputs.
14	$\overline{\text{Ø1}}$	Phase 1 MOS level clock output. Directly drives all MCS-4 clock inputs (up to 250pf).
15	V_{CC}	Circuit reference potential--most positive supply voltage.
16	Ø2T	Phase 1 TTL level clock output (2ma-sink).

4201 IMPLEMENTATION



3.0 Functional Description

The 4201 consists of the following functional blocks:

3.1 Crystal Oscillator

The oscillator is a simple series mode crystal-type circuit consisting of two inverters biased in the active region, and a series crystal element.

3.2 Programmable Shift Register

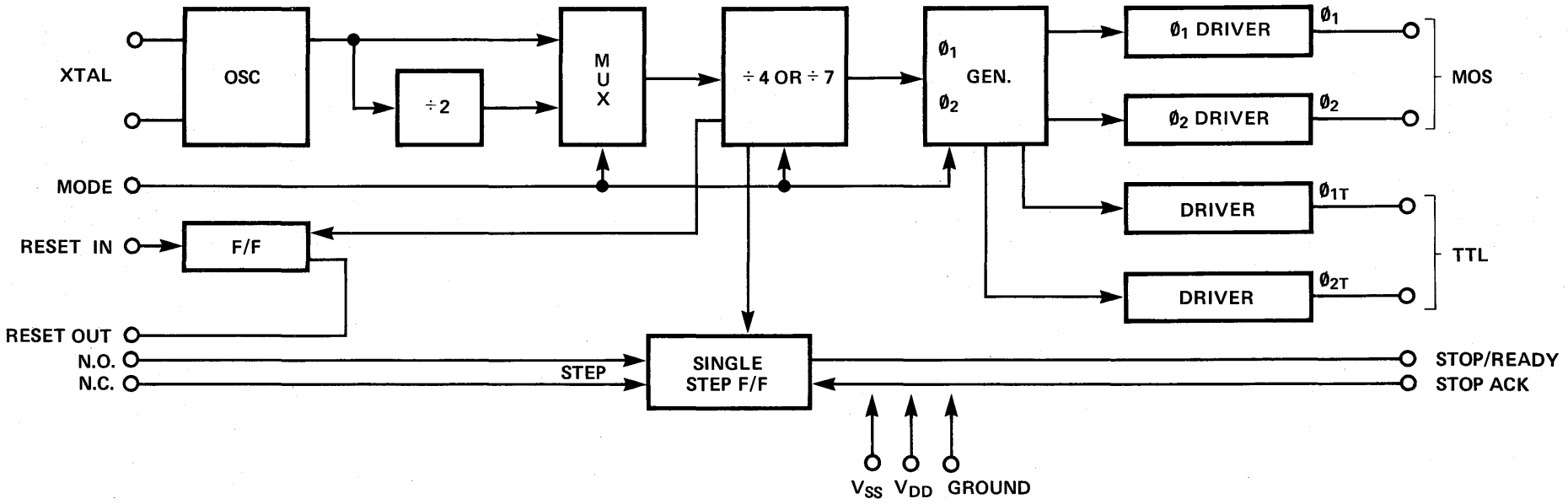
The shift register in the 4201 divides the master clock and generates the proper states for generating the desired two-phase clock. The circuit is a seven-bit dynamic device which circulates a logical "1" through a field of zeroes. The output of the various stages are then combined to provide the proper clock waveforms.

In order to maintain the proper clock timing over the full operating frequency range of the MCS-4, the shift register is programmable (using mode pin) as either a 7-bit or 4-bit device. When in the 4-bit mode the clock is divided by 2 and the relationship between the phases is equal; that is, ϕ_1 pulse width, ϕ_2 pulse width, ϕ_1 to ϕ_2 and ϕ_2 to ϕ_1 times are all equal.

3.3 Phase Decoder

A simple gate complex is used to decode the shift register outputs to provide phase 1 and phase 2 clock waveforms. This circuitry is controlled by the mode input to achieve the two sets of timing discussed in the previous section.

4201 BLOCK DIAGRAM



3.4 Output Buffers

There are two sets of output buffers for the 2 phase clock. One set is the MOS level drivers designed to directly drive a full complement of MCS-4 components. These outputs can drive approximately 250pf loads with transition times of less than 50ns. The second set provides TTL compatible outputs which can drive one standard TTL load.

3.5 Reset Circuit

The reset circuit is simply a level detector and driver stage. An external RC netword connected between V_{DD} and V_{SS} at the reset input pin of the 4201 provides the required power-on delay. A 1MΩ/.5μfd combination will insure a 300ms reset pulse.

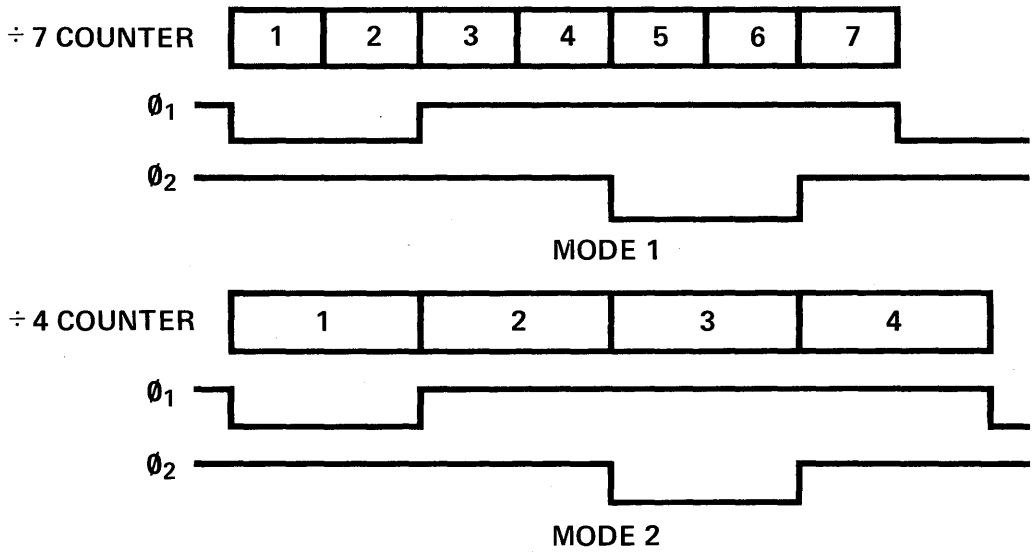
A reset pulse can be generated externally by discharging the external capacitor.

In addition to driving members of the MCS-4 externally, the reset pulse is used internally for initializing the single step circuitry.

3.6 Single Step Control

The 4201 contains the necessary circuitry for allowing the 4040 CPU to execute instructions one at a time. Using the stop input and stop acknowledge output of the 4040, the 4201 generates a pulse that allows the 4040 to perform only one instruction. The stop command can be provided by a SPDT pushbutton directly since bebouncing is provided by the 4201. A SPST toggle switch, in series with the ACK line, provides th the Run/Halt feature.

4201 SHIFT REGISTER MODES



4308 READ ONLY MEMORY

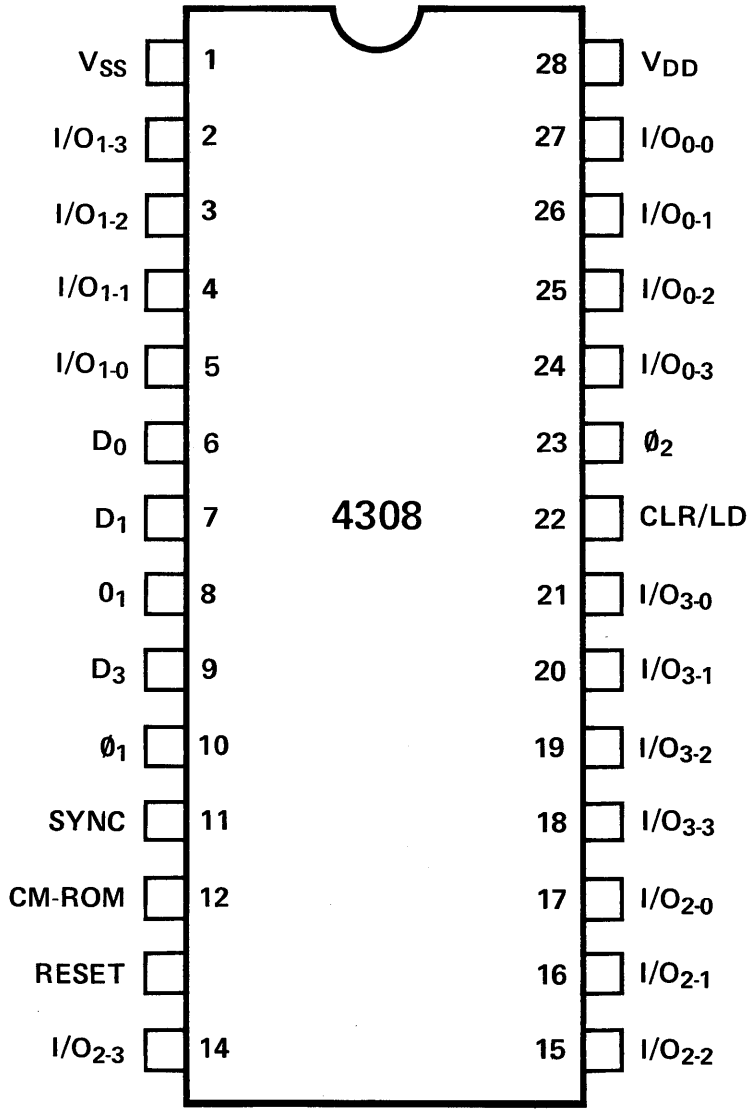
1.0 Introduction

The 4308 is a 1024 x 8-bit word ROM memory with four I/O ports. It is designed for the MCS-4 system, and is operationally compatible with all existing MCS-4 elements. The 4308 is functionally identical to four 4001 chips. It has 16 I/O lines arranged in four groups of four lines. Port selection and accessibility is accomplished as previously, with the 4001. In addition, 4308 has input I/O buffer storage, and is packaged in a 28-pin DIP. A substitution of four 4001 programs can be incorporated in one 4308, including I/O, with no other consideration.

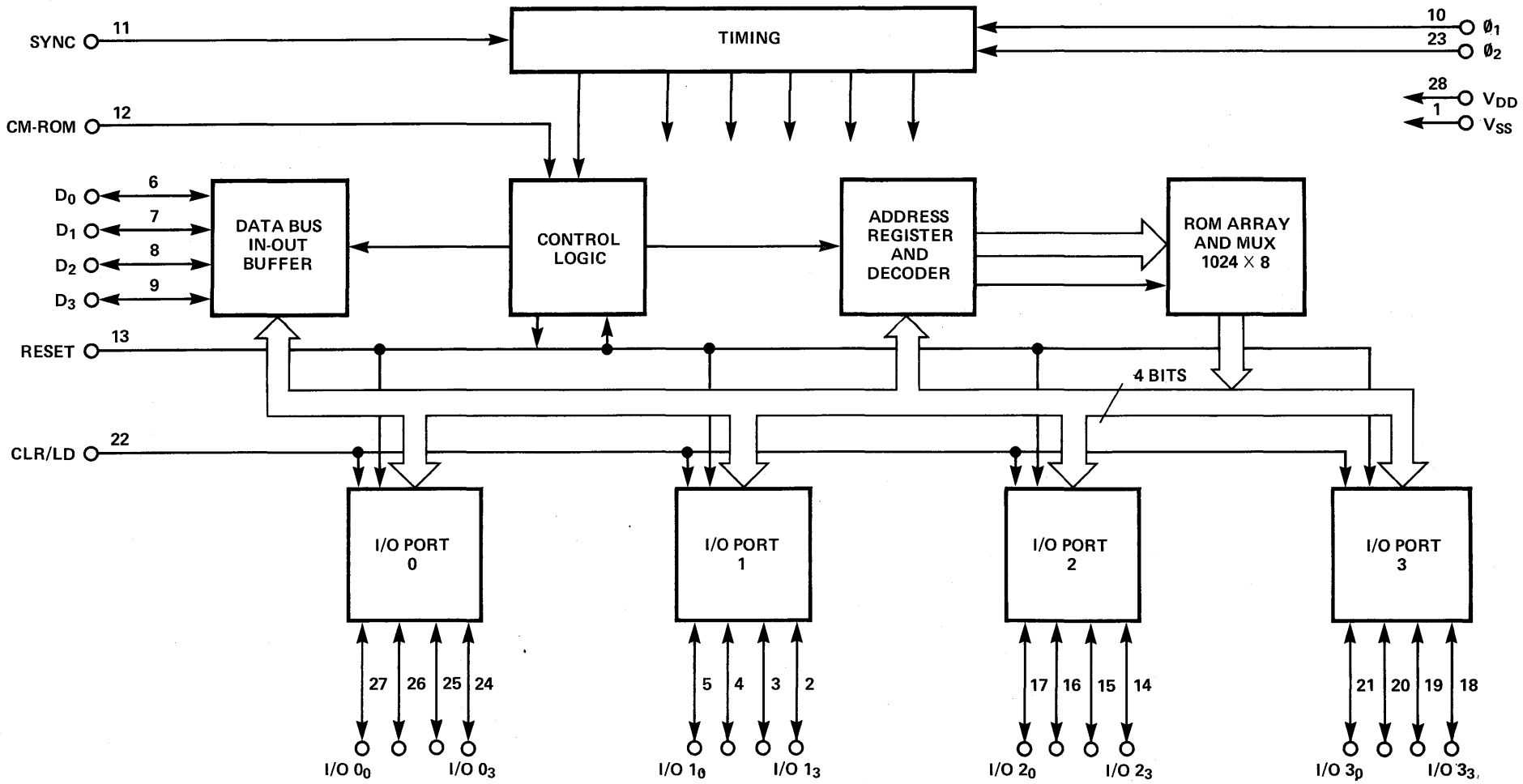
2.0 General Description

The 4308 ROM memory is arrayed 1024 x 8-bit words. As in the 4001, the A1 - A3 time periods are used to address the ROM contents. The 4308 decodes the first ten bits of the address to select 1 out of 1024 words, 8-bits wide. The remaining two bit selects a package number, one of four combinations are possible per ROM bank. The package (chip select) number is selected by a metal mask option. As with the 4001, instruction information is available in two 4-bit segments during M_1 and M_2 time periods. A 4004 system can accommodate up to four 4308's while a 4040 system can utilize up to eight devices. Since the 4308 is compatible with all components of the MCS-4 system, 4308 and 4001 can be mixed on one memory bank as long as the chip select addresses are mutually exclusive.

4308 PIN CONFIGURATION



4308
1024 × 8 BIT MASK PROGRAMMABLE ROM AND 4 I/O PORT, 4 BITS EACH

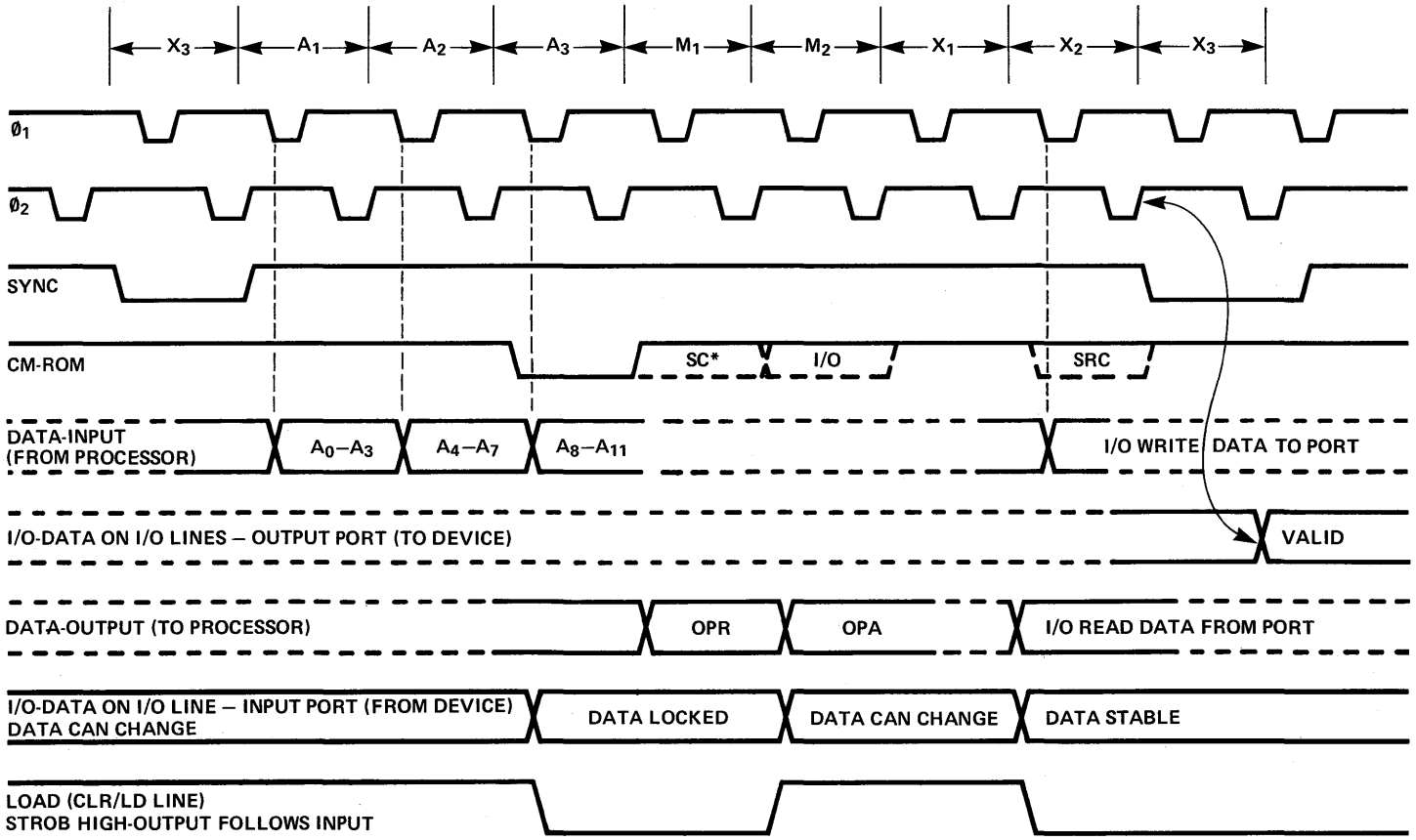


As an I/O device, the 4308 ROM recognizes the same class of I/O instructions (SRC, WRR, and RDR) as that of the 4001 ROM. Each of the four I/O ports are program selectable. Each of the four lines can be specified as either inputs or outputs. This is done via the metal mask option. A complete description of the I/O option capabilities are given in Section 3.0. The 4308 has an input storage buffer for utilization with those I/O pins designated as inputs. A common strobe line allows the asynchronous loading of data from the I/O lines. This same strobe line can also serve as a clear to the I/O output port buffers when designated. This line is common to all ports on a 4308 and when toggled, will effect those I/O lines connected by the metal mask option. For an input line, if the strobe line is left unconnected, or if it is pulled up (V_{SS}), then the output of the buffer will follow the input.

2.1 Pin Description

Pin #	Designators	Description of Function
1	VSS	Circuit GND potential--most positive supply voltage.
2 - 5	$I/O1_3$ - $I/O1_\emptyset$	Four I/O ports consisting of 4 bi-directional and selectable lines which are selectively compatible to a host of logic families.
14 - 17	$I/O2_3$ - $I/O2_\emptyset$	
18 - 21	$I/O3_3$ - $I/O3_\emptyset$	
24 - 27	$I/O\emptyset_3$ - $I/O\emptyset_\emptyset$	
10, 23	ø1, ø2	Non-overlapped clock signals which determine device timing.

4308 EXTERNAL TIMING



*REFER TO MCS 4040 SPECIFICATION

Pin#	Designators	Description of Function
11	SYNC	System synchronization signal generated by processor.
12	CM-ROM	Chip enable generated by the processor.
13	RESET	Reset input. A "1" level on this pin will clear internal flip-flops and buffers. The input buffers are not cleared by this signal.
22	CLR/LD	Clear/Load input. When this option is selected, a "1" to "0" state change will cause the output buffer to clear or the input buffer to load the contents of I/O bus. This bus is common to all I/O ports and is TTL compatible.
28	V_{DD}	Main supply voltage value must be V_{SS} - 15.0V $\pm$ 5%.

2.2 Basic Timing

Referring to the timing diagrams, at the beginning of each instruction sequence, a SYNC pulse is generated externally to synchronize the processor with the various components of the system. This pulse, along with the clock inputs $\emptyset_1$ and $\emptyset_2$, is used in the 4308 as an input to a timing register.

During time A1, A2, and A3 the address is sequentially

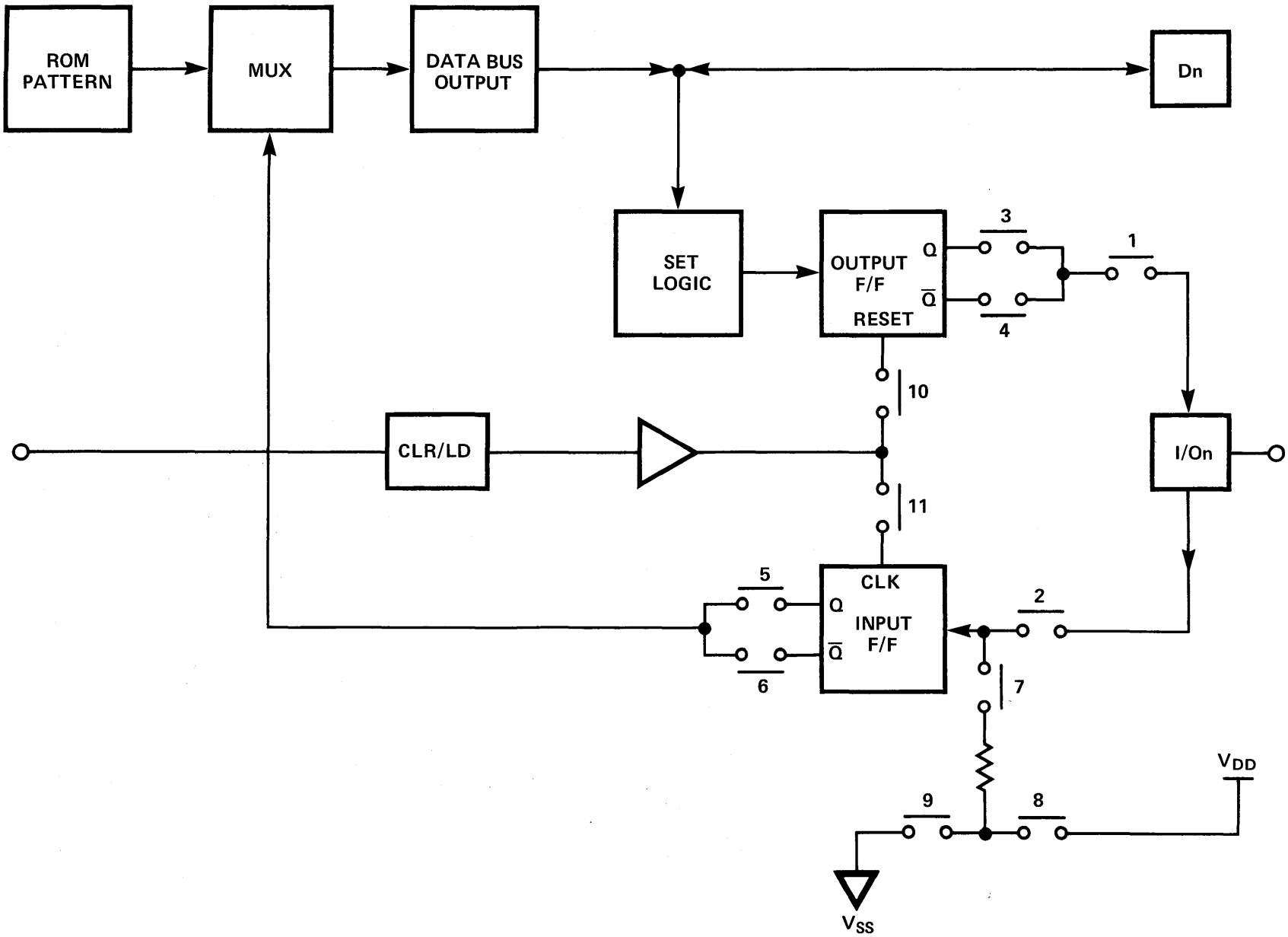
accepted from the data bus and decoded. During time A3, the CM-ROM line will be active, and if the 2-bit (highest order) chip select matches the metal pre-programmed chip select option, the ROM will respond to the current address.

At time M1, M2, the instruction OPR, OPA will be placed on the data bus for the processor. The 4308 responds to 3 I/O instructions in the 4004/4040 instruction set - SRC, RDR, and WRR.

The SRC or Send Register Control instruction is used to designate a set of 4 I/O lines (1 port) on a particular ROM which are to be used for subsequent ROM I/O operations. When this instruction is executed by the processor, the processor sends a 4-bit code to the ROM during X_2, and CM-ROM goes to a "1". The first two bits (D_3, D_4) of this code select a group of 1 out of 4 possible 4308, and the last two bits select a particular port (1 of 4 ports). This port remains selected until the next SRC instruction is executed.

As in the 4001, the WRR (write to ROM port) instruction will cause the contents of the accumulator to be transferred to a previously selected ROM port. As in both the RDR and WRR operations, the CM-ROM line will become active during time M2, and if the ROM has a previously selected I/O port it will respond to the I/O in two ways. For a WRR accumulator, data will be transferred to an internal ROM selected output port flip-flops during X2. Data will be available

4308 I/O PIN OPTIONS



on the I/O line from time X3 · $\overline{\phi}_2$. The data will remain on the bus until a new WRR occurs, a reset occurs, or a clear (CLR/LD line) is generated. The RDR instruction will transfer information from the input port flip-flops of a previously selected port. Prior to RDR instruction the user should insure that the input flip-flops have been loaded via the CLR/LD strobe if the load strobe is specified. If the load strobe is not specified, information on the input lines will be loaded into the accumulator at the time of the RDR. Input ports or lines are TTL compatible as well as the CLR/LD line. Outputs require external pull-up and +5V, -10V supply.

3.0 I/O Options

The 4308 offers all of the feasibilities found in the 4001. In addition, there are enhancements over the 4001:

1. The user can programmably clear any or all output ports with the CL/LD signal.
2. When operated as an input port, both the inverting and non-inverting inputs paths are TTL compatible.
3. By selecting the LD option, the input buffer becomes an input flip-flop and the CL/LD signal becomes an asynchronous clock for loading data.

Referring to the block diagram of the single I/O pin illustrating the various options, it should be noted that the option numbering differs from that of 4001. Certain pin combination are mutually exclusive and should not be specified together. There are also certain invalid combinations. The following combinations should

be avoided:

8, 9

5, 6

3, 4

10, 11

Examples of some common desired option/connections are:

(a) I/O pin inputs*

non-inverting 11, 2, 5, 7, 9 (TTL) - 2, 5, 7, 8

inverting 11, 2, 6, 7, 9 (TTL) - 2, 6, 7, 8

(b) I/O pin outputs

non-inverting 3, 1 (10 optional)

inverting 4, 1 (10 optional)

Other combinations exist and should be used with caution.

For TTL compatibility on the I/O lines, the supply voltage should be V_{DD} = -10V ± 5%, V_{SS} = +5V ± 5%, V_{DD1} = GND. External pull-up is required for outputs.

All 4308 metal masked ROM orders must be submitted on forms provided by Intel. Programming information should be provided in the form of computer punched cards or punched tape. In either case, a print-out of the truth table must accompany the order. Refer to the Appendix for complete pattern specification and a sample 4308 ROM form.

*NOTE: Option 11 need not be specified if an unbuffered input is desired. This is equivalent to a 4001 input.

4308 INPUT FORMAT

The 4308 programming information should be provided in the form of computer punched cards or punched paper tape. The input format is found in the Intel General Component Catalog, and reproduced here for your convenience. The following enhancement has been added to assist in the preparation of programs. These features are optional:

A. The character "X" to be included with "P" and "N" in data word, where "X" indicates "don't care". The bit will be assigned a value which will have the least impact on the dynamic operation of the ROM. A fully assigned listing will be returned to the customer for approval.

B. The use of a format; B*nnnnF to indicate that the preceding word should be repeated nnnnn times, (where "nnn" is a decimal number). It should be noted that "nnnnn" can be no greater than 1023 for the 4308.

The above two options permits the user to default the last "nnn" ROM words to a "don't care" value.

Due to the I/O customizing option of the 4308, the following header information should be appended to the usual programming input. This information provided on a header is optional. The 4308 custom ROM order form should accompany the program whether the header is used or not.

Each tape should start with a device identifier

"I4308-"

where the "I" and the "-" serve as delimiters, just as "B" and "F" do for data words. This could be preceded by any data not containing

an "I".

This should be followed by the chip select information encoded as a decimal number and enclosed by "C" and "S", as in:

"CdS" = Ø - 3

Finally, the I/O options would be specified on a port-by-port basis (refer to ROM form) with the connections to be made separated by commas, and enclosed in parenthesis:

"(n1, n2, n3...n11)".

Example:

"( )"	indicates no connection
"(1)"	indicates only #1
"(2, 5, 7, 9)"	indicates connections 2, 5, 7, and 9

So, a 4308 tape might be:

I4308-CØ3S (1,3) (2,7,5,9)...(1,4) B . . F . .

4308 CUSTOM ROM ORDER FORM

4308 Metal Masked ROM

All custom ROM orders must be submitted on forms provided by Intel. Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a print-out of the truth table must accompany the order. Refer to the 4308 Data Catalog for complete pattern specifications. Additional forms are available from Intel.

CUSTOMER _____	Intel use
ADDRESS _____	S# _____ PPPP _____
_____	STD _____ ZZ _____
P.O. NUMBER _____	APP _____ DD _____
DATE _____	DATE _____ I/O _____

INTEL STANDARD MARKING

The marking as shown at right must contain the Intel logo, the product type (P4308), the four digit Intel pattern number (PPPP), a date code (XXXX), and the two digit chip number (DD). An optional customer identification number may be substituted for the chip number (ZZ). _____

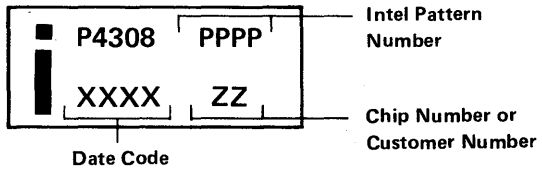
Optional Customer Number (Maximum 6 characters or spaces)

ROM DESCRIPTION

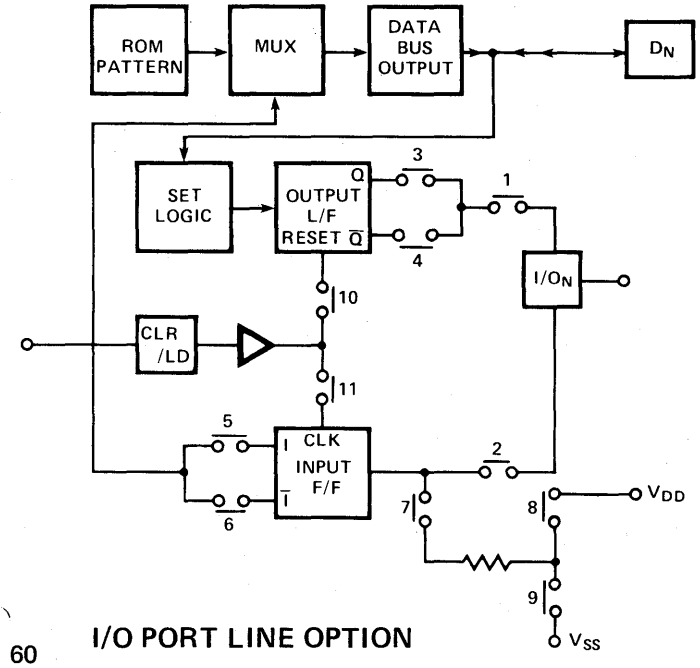
Chip Select Value (0–3) _____ (Must be specified.)

In the table below, select the connections which should be made for each of the 16 I/O port input lines. Avoid the use of illegal options—refer to the 4308 Data Catalog.

Mark the appropriate box for an option connection. Leave blank for a no connection.



PIN		OPTION										
I/O 0_0	27	1	2	3	4	5	6	7	8	9	10	11
I/O 0_1	26	1	2	3	4	5	6	7	8	9	10	11
I/O 0_2	25	1	2	3	4	5	6	7	8	9	10	11
I/O 0_3	24	1	2	3	4	5	6	7	8	9	10	11
I/O 1_0	5	1	2	3	4	5	6	7	8	9	10	11
I/O 1_1	4	1	2	3	4	5	6	7	8	9	10	11
I/O 1_2	3	1	2	3	4	5	6	7	8	9	10	11
I/O 1_3	2	1	2	3	4	5	6	7	8	9	10	11
I/O 2_0	17	1	2	3	4	5	6	7	8	9	10	11
I/O 2_1	16	1	2	3	4	5	6	7	8	9	10	11
I/O 2_2	15	1	2	3	4	5	6	7	8	9	10	11
I/O 2_3	14	1	2	3	4	5	6	7	8	9	10	11
I/O 3_0	21	1	2	3	4	5	6	7	8	9	10	11
I/O 3_1	20	1	2	3	4	5	6	7	8	9	10	11
I/O 3_2	19	1	2	3	4	5	6	7	8	9	10	11
I/O 3_3	18	1	2	3	4	5	6	7	8	9	10	11



I/O PORT LINE OPTION

Input Format

I. ROM and PROM Truth Table Format

Programming information should be sent in the form of computer punched cards or punched paper tape. When using the 7600C or MCS programmers (see Section II), punched paper tape should be used. In all cases, a printout of the truth table should be accompanied with the order.

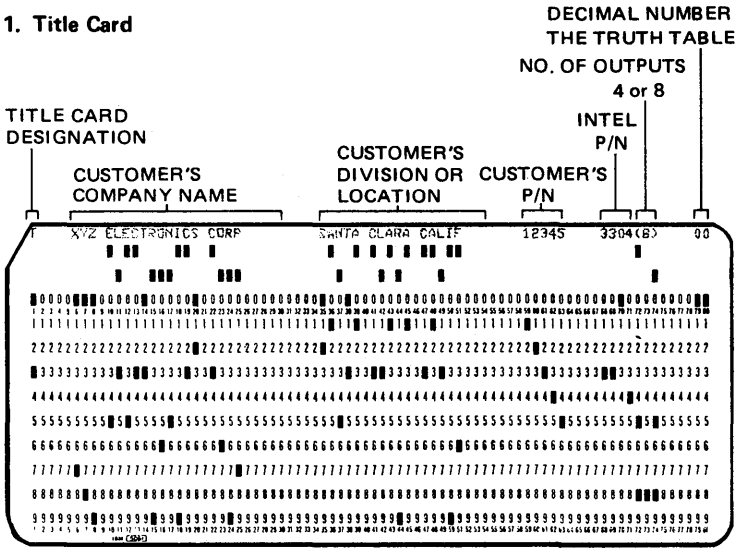
The following general format is applicable to the programming information sent to Intel:

1. A data field should start with the most significant bit and end with the least significant bit.
2. The data field should consist of P's and N's. A P is to indicate a high level output (most positive) and an N a low level output (most negative). If the programming information is sent on a punched paper tape, then a start character, B, and an end character, F, must be used in the data field.

A. Punched Card Format

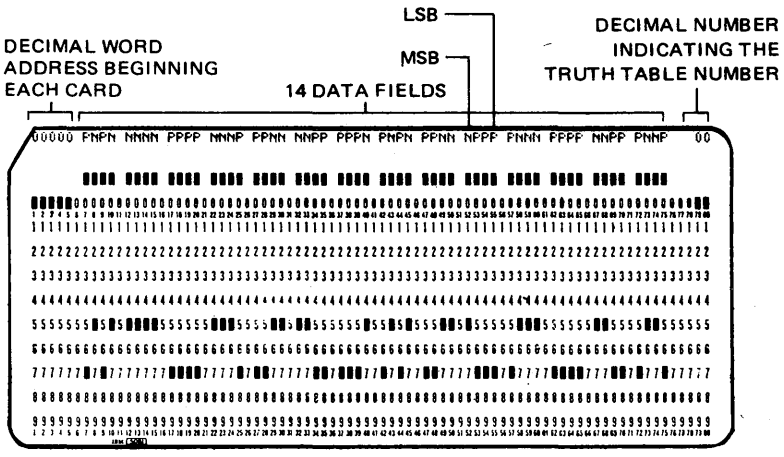
An 80 column Hollerith card (preferably interpreted) punched by an IBM 026 or 029 keypunch should be submitted. The first card will be a title card. The format is as follows:

1. Title Card



Column	Data
1	Punch a T
2-5	Blank
6-30	Customer Company Name
31-34	Blank
35-54	Customer's Company Division or location
55-58	Blank
59-63	Customer Part Number
64-67	Blank
68-74	Punch the Intel 4 digit basic part number and in () the number of output bits, e.g. 1702 (8), 3304 (8), 3301 (4), or 3601 (4).
75-78	Blank
79-80	Punch a 2 digit decimal number to identify the truth table number. The first truth table will be ØØ, second Ø1, third Ø3, etc.

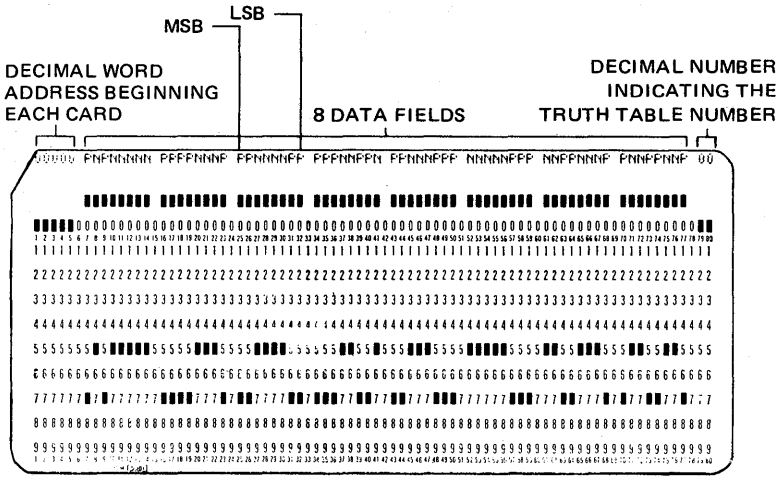
2. For a N words x 4 bit organization only, cards 2 and the following cards should be punched as shown: Each card specifies the 4 bit output of 14 words.



Column	Data
1-5	Punch the 5 digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., ØØØØØ, ØØØ14, ØØØ28, etc.
6	Blank
7-10	Data Field
11	Blank
12-15	Data Field
16	Blank
17-20	Data Field
21	Blank
22-25	Data Field
26	Blank
27-30	Data Field
31	Blank
32-35	Data Field
36	Blank
37-40	Data Field
41	Blank
42-45	Data Field
46	Blank
47-50	Data Field
51	Blank
52-55	Data Field
56	Blank
57-60	Data Field
61	Blank
62-65	Data Field
66	Blank
67-70	Data Field
71	Blank
72-75	Data Field
76-78	Blank
79-80	Punch same 2 digit decimal number as in title card.

Input Format

3. **For a N words x 8 bit organization only, cards 2 and the following cards should be punched as shown. Each card specifies the 8 bit output of 8 words.**



Column	Data
1-5	Punch the 5 digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., ØØØØØ, ØØØØ8, ØØØ16, etc.
6	Blank
7-14	Data Field
15	Blank
16-23	Data Field
24	Blank
25-32	Data Field
33	Blank
34-41	Data Field
42	Blank
43-50	Data Field
51	Blank
52-59	Data Field
60	Blank
61-68	Data Field
69	Blank
70-77	Data Field
78	Blank
79-80	Punch same 2 digit decimal number as in title card.

B. Paper Tape Format

The paper tapes which should be used are the:

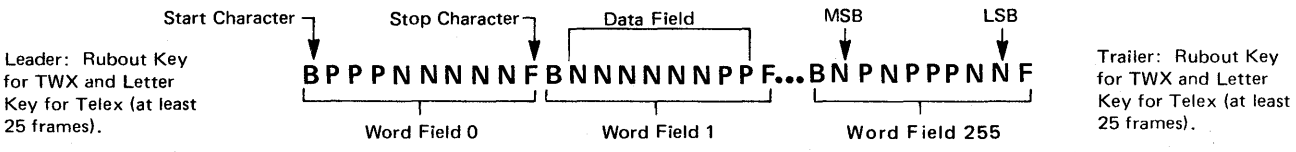
1. 1" wide paper tape using 7 or 8 bit ASCII code, such as a model 33 ASR teletype produces, or the
2. 11/16" wide paper tape using 5 bit Baudot code, such as a Telex produces.

The format requirements are as follows:

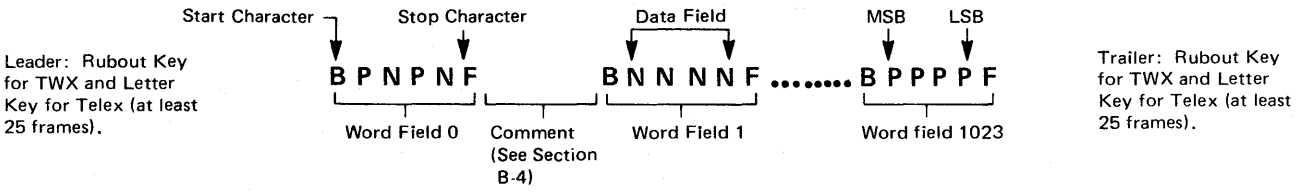
1. All word fields are to be punched in consecutive order, starting with word field Ø (all addresses low). There must be exactly N word fields for the N x 8 or N x 4 ROM organization.
2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 or 4 data characters between the B and F for the N x 8 or N x 4 organization respectively.

   NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A WORD FIELD. If in preparing a tape, an error is made, the entire word field, including the B and F must be rubbed out. Within the word field, a P results in a high level output, and an N results in a low level output.
3. Preceding the first word field and following the last word field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes)
4. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc. are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every four word fields.
5. Included in the tape before the leader should be the customer's complete Telex or TWX number and if more than one pattern is being transmitted, the ROM pattern number.
6. MSB and LSB are the most and least significant bit of the device outputs. Refer to the data sheet for the pin numbers.

Example of 256 x 8 format (N = 256):



Example of 1024 x 4 format (N = 1024):



4289 STANDARD MEMORY INTERFACE

1.0 Introduction

The 4289 is a single chip replacement for the 4008/4009 STANDARD MEMORY and I/O INTERFACE set. Like that set, it enables the 4-bit microprocessor chip (4004 or 4040) to be used with "standard" memory components such as 1702 PROM's or 2102 RAM's and general purpose input/output devices.

A number of improvements as well as additions have been incorporated into the 4289 aside from the single chip package. These are listed here and described in detail in Sections 2 and 3.

1.1 A change in internal timing has been made which will allow using PROGRAM MEMORY components with access times as great as 2.1μseconds (address to output).

1.2 A new instruction, READ PROGRAM MEMORY (RPM) which is included in the 4040 instruction set, is recognized by the 4289. Section 3.3 provides a detailed description of RPM.

1.3 A separate supply voltage, V_{DD1}, has been provided for the ADDRESS and CHIP SELECT buffers. This simplifies the problem of interfacing to n-channel/TTL-compatible memories. See Appendix for examples.

1.4 A RESET pin has been added which simplifies control over the FIRST/LAST flip-flop (see Section 3.3). It is not necessary to power down the chip to perform the reset function.

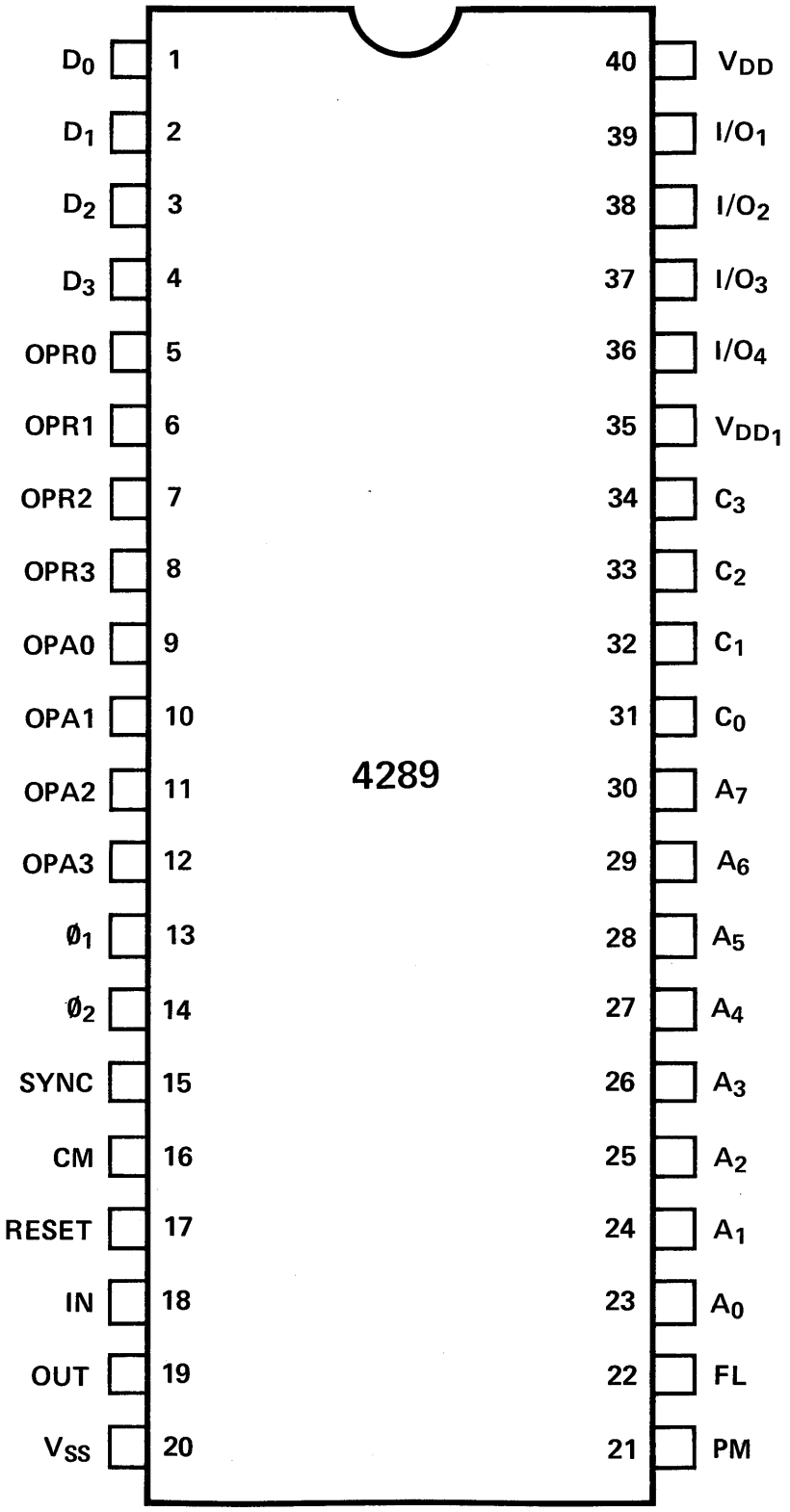
2.0 Description of Basic Hardware

The 4289 is packaged in a 40-pin plastic DIP. The pin configuration and a brief functional description of each pin is given in Section 2.1.

2.1 Pin Function Description

Pin #	Designation	Description
1 - 4	$D_{\emptyset}$-D_3	Bidirectional data bus. All address, instruction and data communication between processor and the PROGRAM MEMORY or I/O ports is transmitted on these 4 pins.
5 - 8	$OPR_{\emptyset}$-OPR_3	The high order 4 bits (OPR) of the instruction from the PROGRAM MEMORY are transferred to the 4289 on these pins. Same as D_5'-D_8' on 4009.
9 - 12	$OPA_{\emptyset}$-OPA_3	The low order 4 bits (OPA) of the instruction are transferred to the 4289. Same as D_1'-D_4' on 4009.
13 - 14	$\emptyset_1$-$\emptyset_2$	Non-overlapping clock signals which are used to generate the basic chip timing.

4289 PIN CONFIGURATION



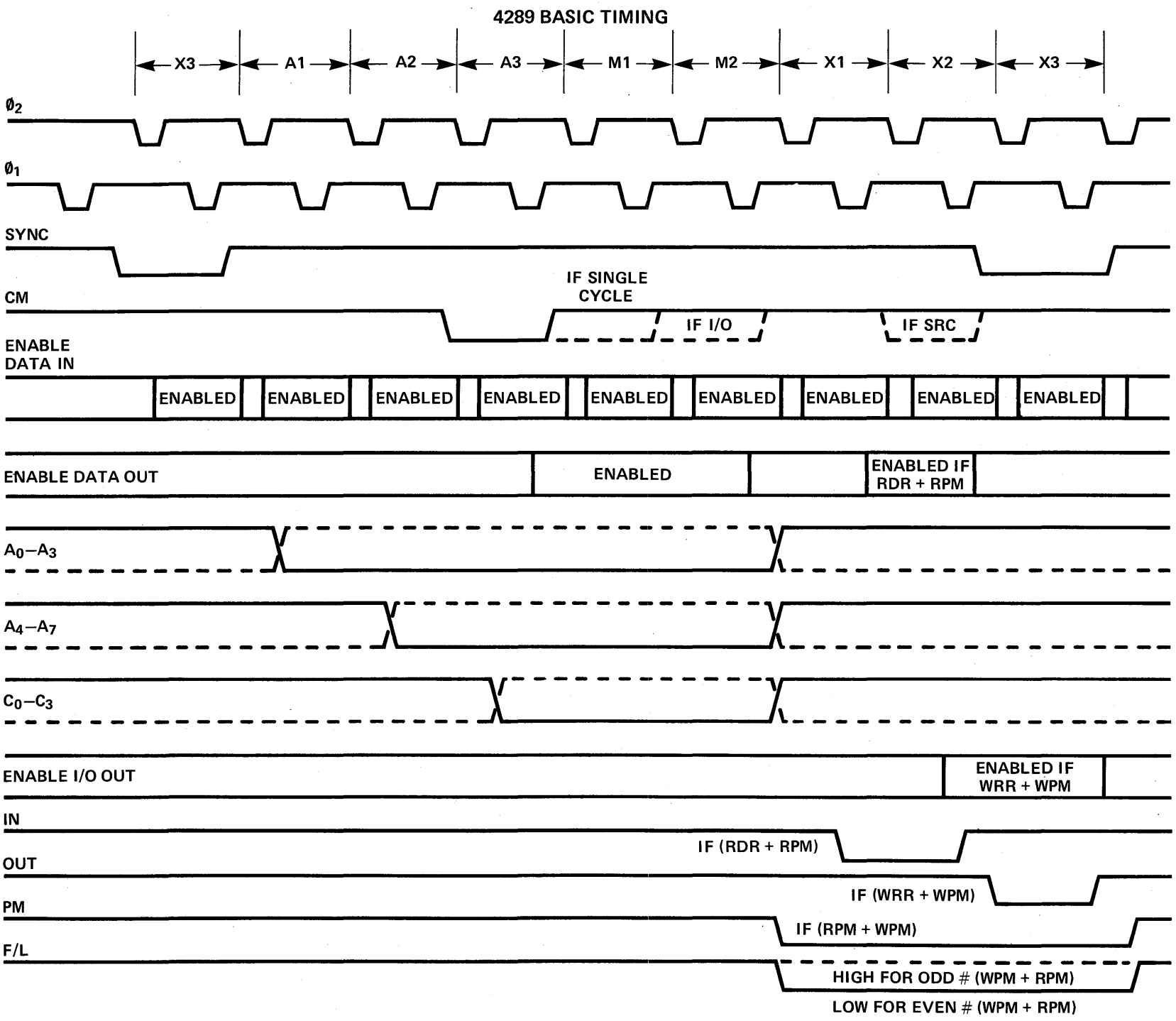
Pin #	Designation	Description
15	SYNC	Synchronization input signal driven by SYNC output of processor.
16	CM	Command input driven by CM-ROM output of processor. Used for decoding SRC and I/O instructions.
17	RESET	RESET input. A logic "1" level applied to this input resets the CM flip-flop and FIRST/LAST flip-flop.
18	IN	Output signal generated by 4289 when the processor executes an RDR or RPM instruction.
19	OUT	Output signal generated by the 4289 when the processor executes a WRR or WPM instruction.
20	V_{SS}	Circuit GND potential; most positive supply voltage.
21	PM	Output signal generated by the 4289 when the processor executes an RPM or WPM instruction.
22	F/L	Output signal generated by the 4289 to indicate which half-byte of PROGRAM MEMORY is to be operated on.

Pin #	Designation	Description
23 - 30	$A_\emptyset$-A_7	Address output buffers. The demultiplexed address values generated by the 4289 from the address data supplied by the processor at A_1 and A_2.
31 - 34	$C_\emptyset$-C_3	Chip select output buffers. The address data generated by the processor at A_3, or during an SRC are transferred here.
35	V_{DD1}	Supply voltage for address and chip select buffers.
36 - 39	$I/O_\emptyset$-I/O_3	Bidirectional I/O data bus. Data to and from I/O ports or data to R/W PROGRAM MEMORY are transferred via these pins.
40	V_{DD}	Main power supply pin. Value must be V_{SS} - 15V $\pm$ 5%.

2.2 Basic Circuit Timing

The basic timing of the 4289 which is generated by the two non-overlapping clock pulses $\emptyset_1$ and $\emptyset_2$. The 4289 is synchronized to the processor by the SYNC signal generated by the processor and sent out at the beginning of each instruction cycle.

During a typical instruction cycle, the 4289 follows the sequence of events outlined below:


4289 BASIC TIMING
X3
A1
A2
A3
M1
M2
X1
X2
X3
Ø2
Ø1
SYNC
CM
IF SINGLE CYCLE
IF I/O
IF SRC
ENABLE DATA IN
ENABLED
ENABLED
ENABLED
ENABLED
ENABLED
ENABLED
ENABLED
ENABLED
ENABLED
ENABLE DATA OUT
ENABLED
ENABLED IF RDR + RPM
A0–A3
A4–A7
C0–C3
ENABLE I/O OUT
ENABLED IF WRR + WPM
IN
IF (RDR + RPM)
OUT
IF (WRR + WPM)
PM
IF (RPM + WPM)
F/L
HIGH FOR ODD # (WPM + RPM)
LOW FOR EVEN # (WPM + RPM)

a. The device latches the address information sent by the processor at A_1, A_2, and A_3, and presents the 12-bit parallel address on pins $A_\emptyset$-A_7 and $C_\emptyset$-C_3. $A_\emptyset$-A_7 select 1 out of 256 eight-bit words and $C_\emptyset$-C_3 enable 1 out of 16 pages of PROGRAM MEMORY.

b. The 8-bit contents of the selected memory location are transferred to the 4289 on pins $OPR_\emptyset$-OPR_3 and $OPA_\emptyset$-OPA_3. They are then multiplexed and transferred to the processor in two 4-bit groups at M_1 and M_2.

c. The 8-bit contents of the internal SRC register are transferred to the ADDRESS and CHIP SELECT buffers at X_1. This value is used as an address for an ensuing I/O or PROGRAM MEMORY operation (see Section 3.2 for detailed description).

d. The special control signals IN, OUT, PROGRAM MEMORY and FIRST/LAST are generated by the 4289 as shown in Figure 2. They are required for performing the I/O and PROGRAM MEMORY operations and are described in detail in Section 3.

2.3 Major Circuit Blocks

The major functional blocks which make up the chip are:

a. Data bus input-output buffer and multiplex circuitry.

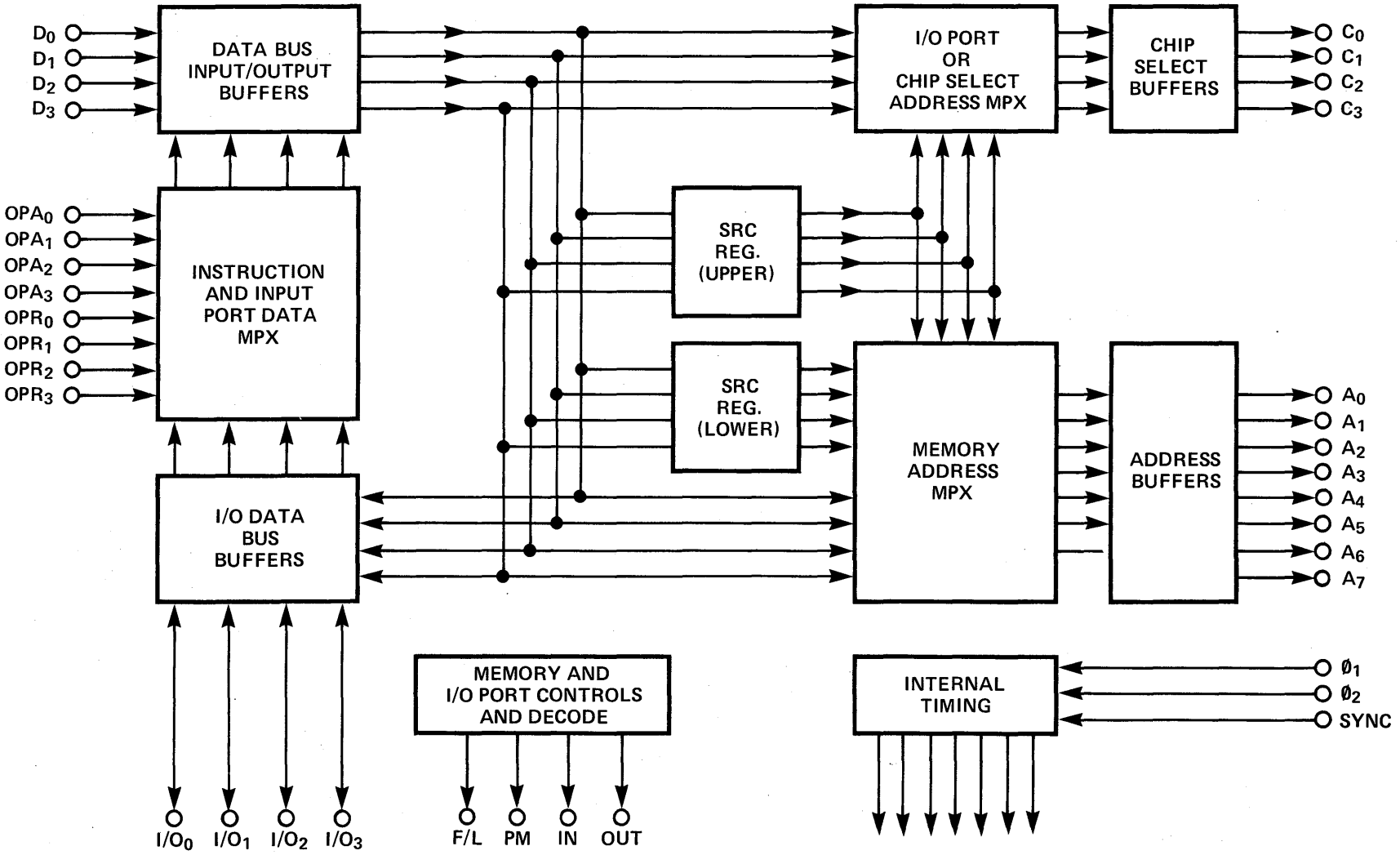
b. Address and chip select output buffers and multiplex circuitry.

c. 8-bit SRC register.

d. I/O input-output buffers.

e. Timing and control logic.

4289 BLOCK DIAGRAM



A brief description of each of these major circuit blocks is given below.

2.3.1 Data Bus Input-Output Buffer

The bidirectional data bus buffers provide a communication channel to the processor. The associated multiplex circuitry allows the 4289 to send PROGRAM MEMORY or I/O port information to the processor.

2.3.2 Address and Chip Select Output Buffers

The address and chip select output buffers provide a 12-bit parallel address to the PROGRAM MEMORY for instruction fetch operations. At X_1 the contents of the internal SRC register is transferred to the address and chip select buffers to be used as an address for an I/O or PROGRAM MEMORY operation. The high order 4 bits (SRCRH) are transferred to $C_\emptyset$-C_3 and to A_4-A_7. The low order 4 bits ($SRCR_2$) are transferred to $A_\emptyset$-A_3.

2.3.3 SRC Register

The 8-bit SRC register stores the address value sent out by the processor at X_2 and X_3 of an SRC instruction. The contents of this register is transferred to the address and chip select buffers at X_1 of every instruction cycle, as described above.

2.3.4 I/O Input-Output Buffers

The I/O buffers are used to transfer data between the processor and the input/output ports or from the

processor to the PROGRAM MEMORY in the case of a WRITE PROGRAM MEMORY (WPM) instruction.

2.3.5 Timing and Control Circuitry

This includes:

a. The internal timing register.

b. Instruction decoding for the following instructions: WRR, RDR, WPM, RPM.

c. FIRST/LAST flip-flop.

d. The logic required for generating the external control signals, IN, OUT, PM, and F/L.

3.0 Detailed Description of Operating Modes

As stated in the Introduction, the 4289 enables the 4-bit microprocessor chip (4004 or 4040) to interface to standard memory components. This allows construction of prototype or small volume systems using electrically programmable ROM's or RAM's in place of 4001 mask programmable ROM's. Since 4001's also contain mask programmable I/O ports, the 4289 has provisions for directly addressing 16 channels of 4-bit I/O ports. In its role as a Memory and I/O interface device, the 4289 provides three different types of operation, namely;

a. Interface to Program Memory for instruction fetch operations.

b. Interface to Input/Output ports for storing or fetching data using WRR, RDR instructions.

c. Interface to R/W Program Memory for storing or fetching data or for program alteration using WPM, RPM instructions. This last feature allows the use of standard R/W RAM to be used

for data storage.

These three basic operations will be discussed in detail in the following paragraphs.

3.1 Instruction Fetch Operation

The contents of the data bus at A_1, A_2, and A_3 are latched by the 4289 and transferred to the address and chip select output buffers as shown in Figure 2. The low order address at A_1 is transferred to $A_\emptyset$-A_3 outputs, the middle order address at A_2 is transferred to A_4-A_7 outputs and the high order address at A_3 is transferred to $C_\emptyset$-C_3 outputs. These 12 output lines provide the necessary address and chip select signals to interface to a 4K x 8-bit Program Memory (see Appendix for examples of Program Memory configurations).

The 8-bit word selected by $A_\emptyset$-A_7 and $C_\emptyset$-C_3 is transferred to the processor via the $OPR_{\emptyset-3}$, $OPA_{\emptyset-3}$ input lines and the data output buffer. The high order bits (OPR) are transferred at M_1 and the low order 4 bits (OPA) are transferred at M_2. The $OPR_\emptyset$-OPR_3 input lines correspond to the D_5'-D_8' lines of the 4009 and the $OPA_\emptyset$-OPA_3 lines correspond to the D_1'-D_4' lines.

The 4289 has been designed to work equally well with either the 4004 or 4040 processor elements. Since the 4040 is provided with two CM-ROM controls which allow it to directly address up to 8K x 8-bits of Program Memory (4K x 8-bits selected by each CM-ROM control), two 4289's would be required for full memory capability. In this case, one 4289 would be

controlled by CM-ROM$_{\emptyset}$ and the other by CM-ROM$_1$. The 4289 which receives CM at A_3 would be enabled to transfer data at M_1 and M_2.

In should be noted that the two CM-ROM controls permit the simultaneous use of 4001, 4308, and 4289 in the same system. The ROM's 4001 and 4308 can be mixed and assigned to one CM-ROM control line while a single 4289 can be assigned to the other. Within one CM-ROM control line, 4289, 4001, and 4308 cannot be mixed. The reason being that bus contention will arise between the devices.

3.2 I/O Port Operation

When the processor executes an I/O port instruction (WRR or RDR), a previously selected I/O port is enabled to receive or transmit 4 bits of data. In the case of WRR, the selected output port receives the 4-bit contents of the processor accumulator, and in the case of RDR, the selected input port transmits 4 bits of data to the processor accumulator. In either case, the port selection must be made by means of a previous SRC instruction. The 4-bit value sent out at X_2 is used as the port address. The 4289 must therefore be capable of storing the SRC address sent by the processor and presenting that address to the I/O port selection logic. To accomplish this, the 4289 behaves as follows:

a. When the processor executes an SRC instruction, the 4289 stores the address sent out by the processor at X_2 and X_3. The contents of this SRC register are transferred during

every X_1 time to the address and chip select are available for subsequent I/O instructions. The high order 4 bits are presented at $C_\emptyset$-C_3 and will select the I/O port.

b. When the processor then executes a WRR instruction, the 4289 latches the data sent out by the processor at X_2 and transfers this data to the I/O output buffer. This buffer is enabled during X_3 and transmits the data to the selected output port. So that external port logic may be enabled to receive the data, the 4289 generates the OUT strobe signal.

c. When the processor executes an RDR instruction, the 4289 generates the IN strobe. This enables the selected input port to transmit its data to the I/O bus, where it is latched by the 4289 and transferred to the processor at X_2.

The system configurations given in the Appendix provide several examples of I/O port connections.

3.3 Read/Write Program Memory Operations

The 4008/4009 combination provides the WRITE PROGRAM MEMORY (WPM) function which allows standard random access memory chips to be used for program or data storage. Reading locations in this memory, however, require dedicating an input port for the purpose. However, if the 4289 is used in conjunction with the 4040, both the WRITE and READ PROGRAM MEMORY (RPM) functions are directly available. To accomplish these operations, the following are required:

a. A program memory address.

b. The proper control signals.

c. A means of transmitting the data to be stored or fetched.

The 4289 provides all of these as described in the following paragraphs.

3.3.1 Program Memory Address

The address for an RPM or WPM operation is provided by the 8-bit contents of the SRC register. At X_1 of every instruction cycle this 8-bit value is transferred to the address output buffers $A_\emptyset$-A_7. These addresses will select 1 out of 256 program memory words. During execution of WPM or RPM, the 4289 does not transfer the high order 4 bits of the SRC register to $C_\emptyset$-C_3. Instead, it forces all 4 chip select output buffers to a logic "1" state (positive true logic). If only one page of R/W memory is required the 1111 condition on $C_\emptyset$-C_3 can be used to enable that page. If more than one page is required, an output port will be necessary to store the 1 out of 16 page select address.

Since the program memory is organized as 8-bit words, and since RPM and WPM are transmitting only 4-bit words, it is also necessary to specify either the upper or lower half-byte of program memory.

This is done automatically by the FIRST/LAST flip-flop in the 4289. The state of this flip-flop is used

to generate the control signal F/L which determines the proper half-byte of program memory. If F/L is a logic "1" state, the first or lower half-byte is selected, and when F/L is a logic "Ø", the last or upper half-byte is selected.

Unlike the F/L control in the 4008, the user can directly reset the FIRST/LAST flip-flop in the 4289 by applying a RESET signal.

Starting from a "reset" condition the FIRST/LAST flip-flop automatically toggles after executing either an RPM or WPM instruction. Hence, odd numbered program memory operations select the 'first' half-byte and even numbered program memory operations select the 'last' half-byte.

3.3.2 Program Memory Control Signals

When the processor executes either WPM or RPM, the 4289 generates the following control signals:

a. F/L - As indicated in 3.3.1.

b. PM - This output signal is generated as shown in Figure 2 whenever a program memory operation is to be performed. This signal allows external logic to differentiate between a program memory operation and an I/O operation.

c. OUT - This strobe signal is generated only during WPM and WRR instructions. The combination of PM

and OUT is used as a WRITE ENABLE signal for the program memory.

The system examples shown in the Appendix demonstrate the use of these control signals.

3.3.3 Program Memory Data Paths

When the processor executes the WPM instruction, the 4289 latches the data sent out at X_2 by the processor and transfers it via the I/O output buffers to the I/O bus. The I/O bus must be connected to the data input pins of the R/W memory chips (see Figure A3 in the Appendix).

If the processor (4040) executes the RPM instruction, then the entire 8-bit program memory word is transferred to the $OPR_\emptyset$-OPR_3 and $OPA_\emptyset$-OPA_3 inputs of the 4289. Depending on the state of F/L either the first (OPA) or last (OPR) half-byte is automatically selected by the 4289.

APPENDIX

The 4289 can be used to form systems of widely varying complexity. Simple systems containing only one page (256 x 8) of PROGRAM MEMORY and few I/O ports, or more complex systems requiring as many as 32 pages (8K x 8) of memory and 32 I/O ports can readily be implemented. Several examples will be described here. Refer to the listed Figure.

A. Figure A1 - SIM4-01 Equivalent. This system contains:

- 1K x 8 bits of PROGRAM MEMORY (1702A ROM)
- 1280 bits of DATA MEMORY (4002 RAM) organized as 16 20-character registers
- 4 RAM output ports (4002)
- 4 I/O ports

This system used 3205's to decode the IN and OUT strobes for the I/O ports. Since the I/O buffers of the 4289 can sink one full TTL load, no additional buffering is required (3404 input current = 250A max.)

B. Figure A2 - This system again contains 4 pages of PROM storage but, in addition, has one page of RAM storage which can be used for either PROGRAM or DATA storage by using the WPM/RPM instructions. (The RPM instruction is valid only with the 4040). The RAM storage has been implemented with 2101's (256 x 4 version of 2102). Notice that separate WRITE ENABLE signals must be generated for the upper and lower half-bytes of RAM.

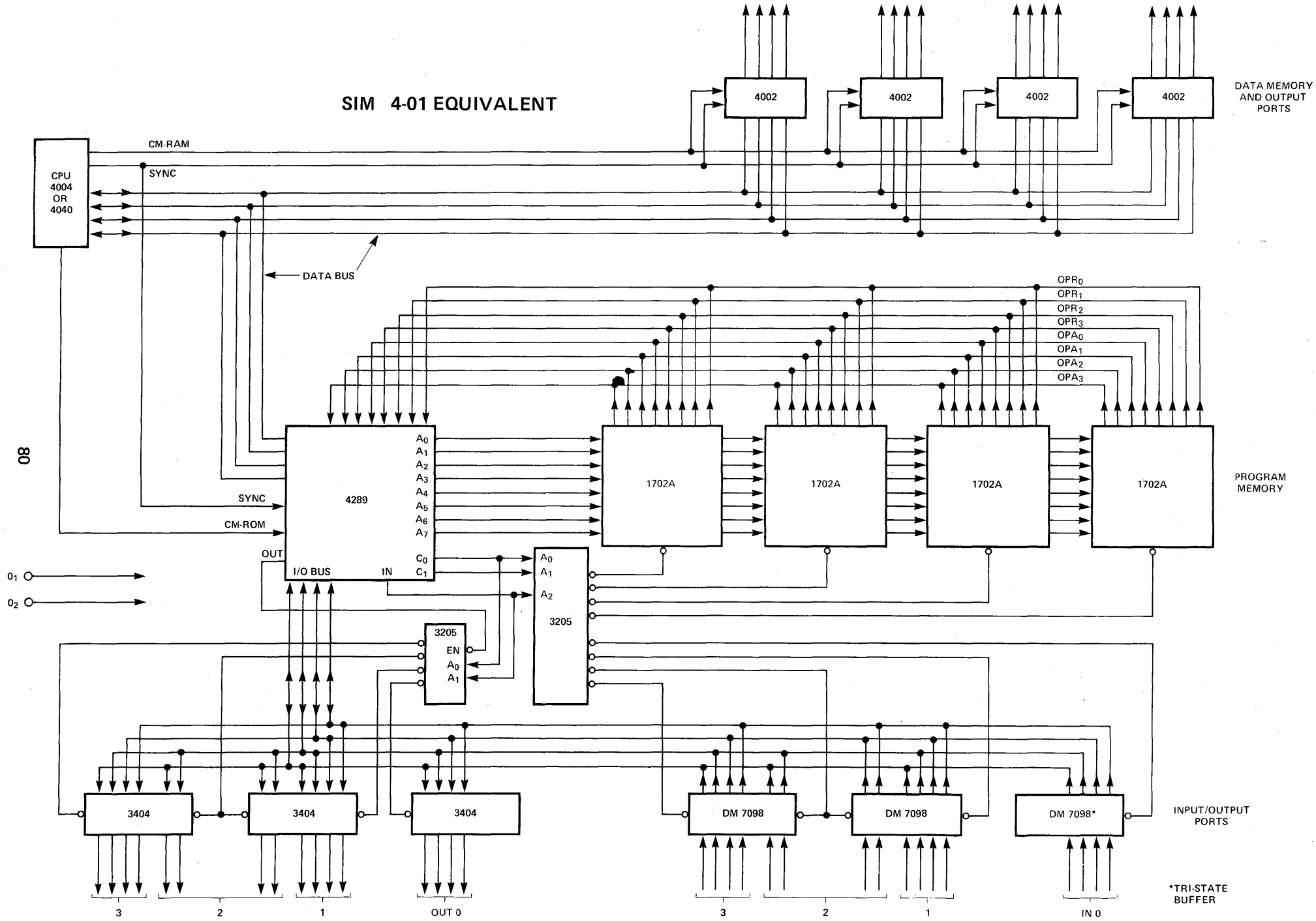
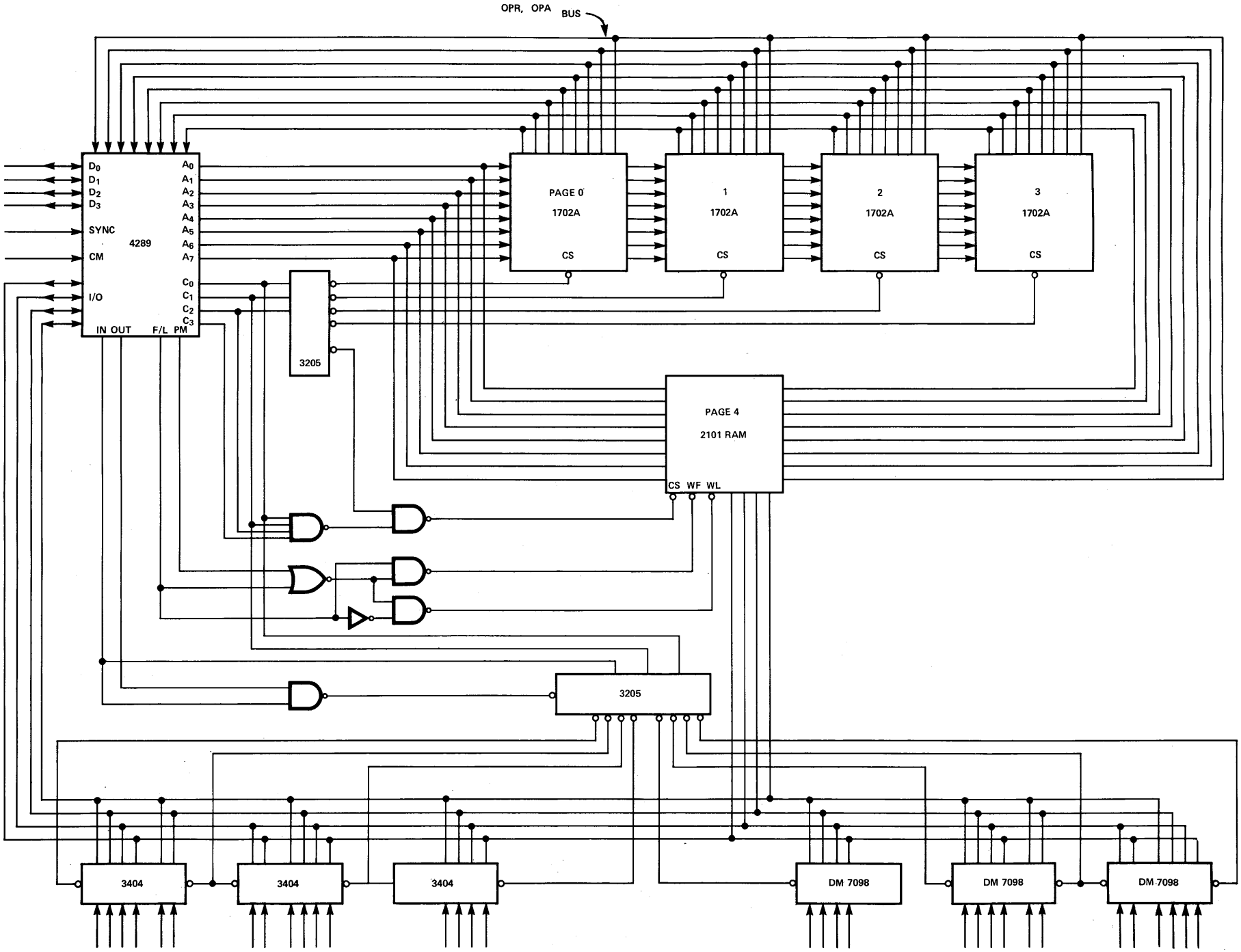

SIM 4-01 EQUIVALENT
CPU 4004 OR 4040
CM-RAM
SYNC
DATA BUS
4002
4002
4002
4002
DATA MEMORY AND OUTPUT PORTS
OPR0
OPR1
OPR2
OPR3
OPA0
OPA1
OPA2
OPA3
4289
SYNC
CM-ROM
OUT
I/O BUS
IN
A0
A1
A2
A3
A4
A5
A6
A7
C0
C1
1702A
1702A
1702A
1702A
PROGRAM MEMORY
01
02
3205
EN
A0
A1
3205
A0
A1
A2
3404
3404
3404
DM 7098
DM 7098
DM 7098*
INPUT/OUTPUT PORTS
*TRI-STATE BUFFER
3
2
1
OUT 0
3
2
1
IN 0

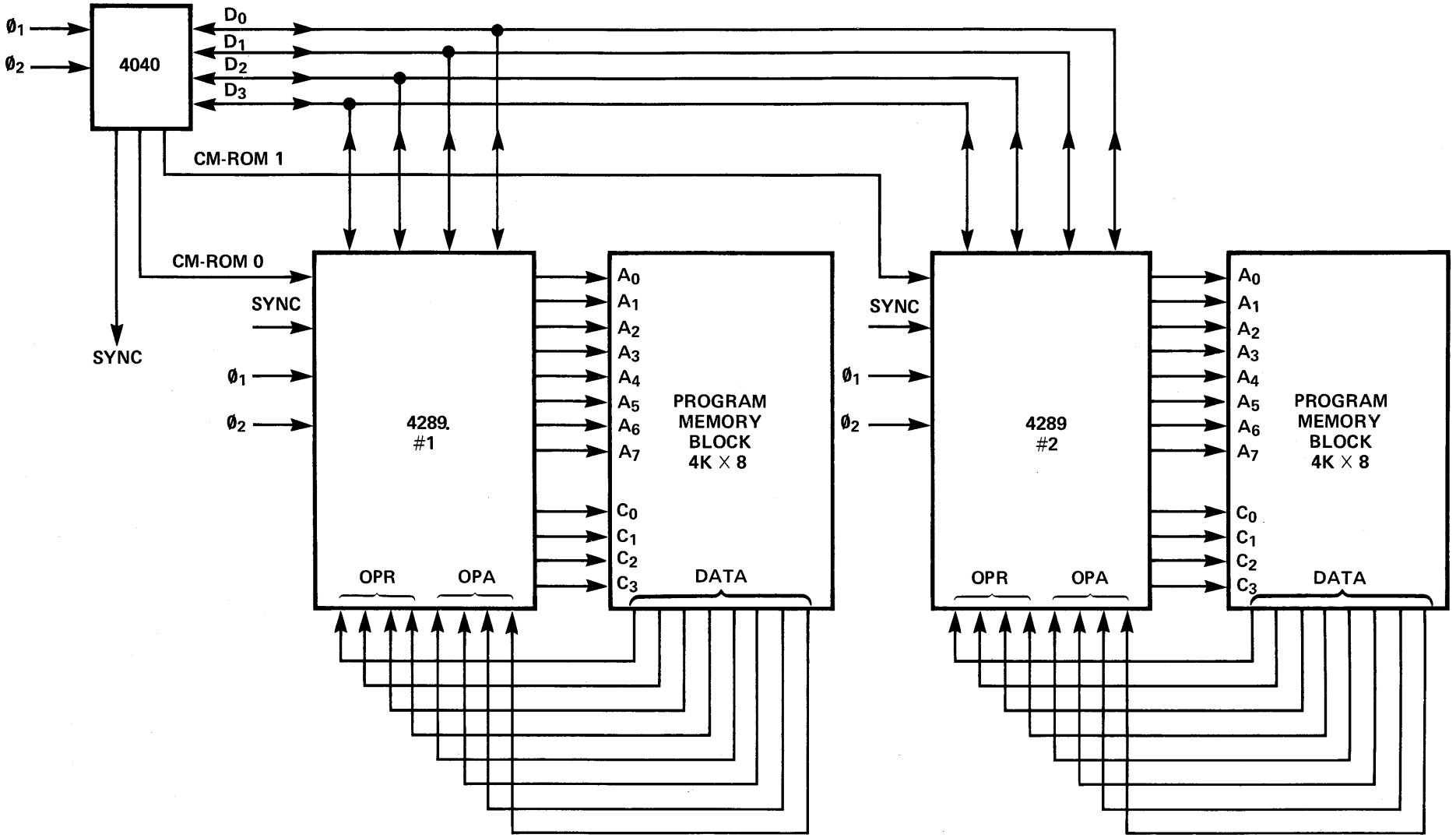
FIGURE A2 RA[redacted]ROM Program Memory Organization



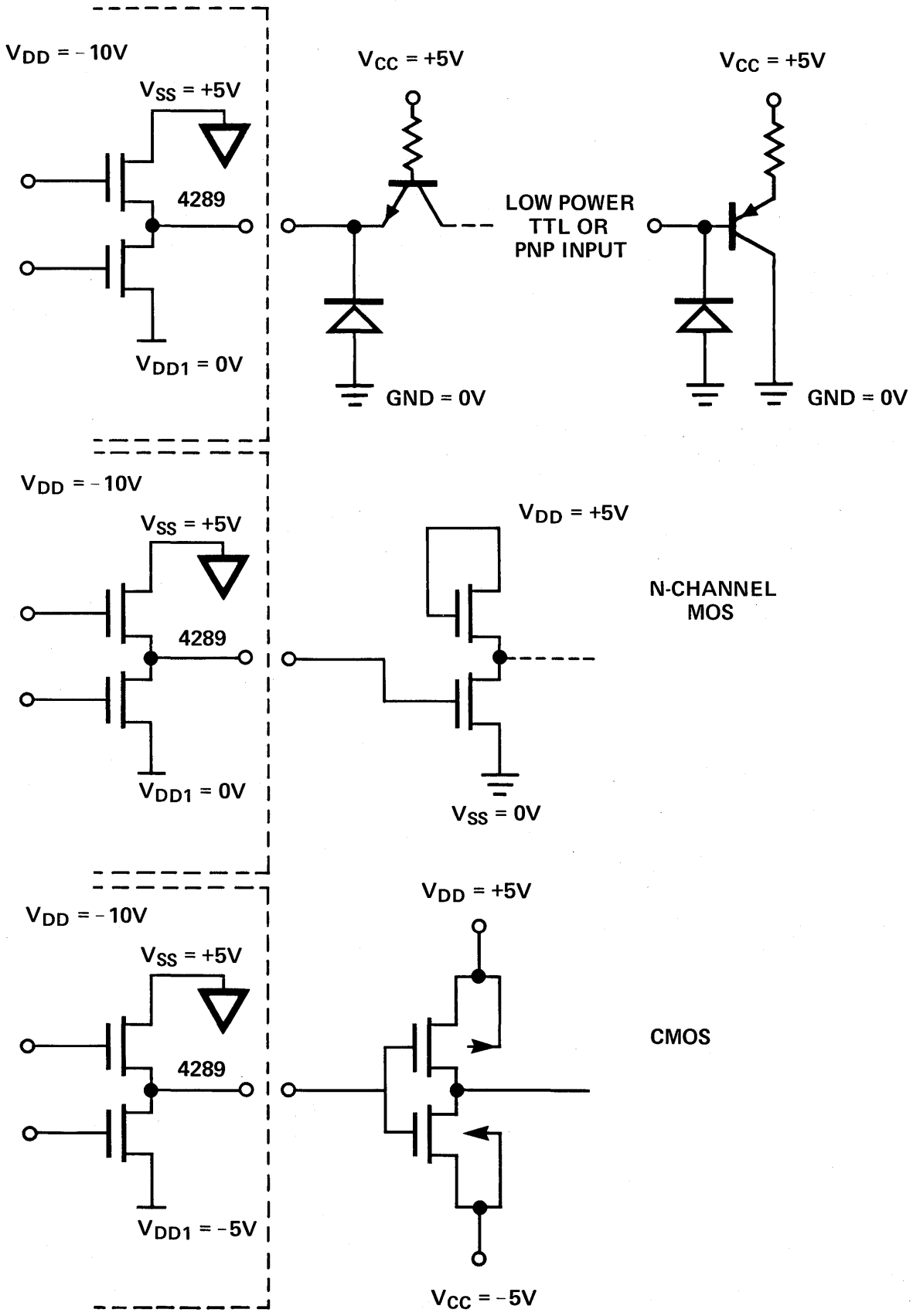
C. Figure A3 - Systems using two 4289's can be designed as shown here. In this case each 4289 is controlled from a separate CM-ROM control signal. The CM-ROMØ and CM-ROM1 lines are generated by the 4040. This system cannot be implemented with the 4004.

As mentioned in 1.3 of the Introduction, a separate supply pin, V_{DD1}, has been provided for the ADDRESS and CHIP SELECT output buffers. Figure 4 shows examples of the use of V_{DD1} when interconnecting the 4289 with other circuit forms.

4040 8K MEMORY SYSTEM



4289 INTERFACE METHOD



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