SERVICE MANUAL FOR

9270D

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1. Hardware Engineering Specification

1.1 Introduction

The 9270D motherboard implements Intel's Calpella platform with Arrandale mobile processor. Arrandale is the next generation of 64-bit, multi-core mobile processors built on 32-nanometer process technology. Throughout this document, Arrandale may be referredto as simply the processor. Based on the low-power/high-performance Nehalem microarchitecture, the processor is designed for a two-chip platform as opposed to the traditional three-chip platforms (processor, GMCH, and ICH). The two-chip platform consists of a processor and the Platform Controller Hub (PCH) and enables higher performance, lower cost, easier validation, and improved x-y footprint.

Included in this family of processors is an integrated memory controller (IMC) and integrated I/O (IIO) (such as PCI Express* and DMI) on a single-silicon die. This singledie solution is known as a monolithic processor.

The Ibex Peak provides extensive I/O support. Functions and capabilities include:

- PCI Express* Base Specification, Revision 2.0 support for up to eight ports.
- PCI Local Bus Specification, Revision 2.3 support for 33 MHz PCI operations (supports up to four Req/Gnt pairs).
- ACPI Power Management Logic Support, Revision 3.0b
- Enhanced DMA controller, interrupt controller, and timer functions

- Integrated Serial ATA host controllers with independent DMA operation on up to six ports.
- FIS-based Port Multiplier support on SATA Ports 4 and 5 in AHCI/RAID mode.
- USB host interface with support for up to fourteen USB ports; two EHCI high-speed USB 2.0 Host controllers, 2 rate matching hubs, seven UHCI host controllers;
- Integrated 10/100/1000 Gigabit Ethernet MAC with System Defense
- System Management Bus (SMBus) Specification, Version 2.0 with additional support for I2C devices
- Supports Intel® High Definition Audio
- Supports Intel® Matrix Storage Technology
- Supports Intel® Trusted Execution Technology
- Analog and Digital Display ports

— Analog CRT

— HDMI

— DVI

— DisplayPort 1.1

— SDVO

— LVDS (Mobile Only)

- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support
- Serial Peripheral Interface (SPI) support
- Intel® Quiet System Technology (Desktop only)
- Intel® Anti-Theft Technology

User expendable peripheral interface built on 9270D system are 3 USB + 1 combo E-SATA ports. 9270D system provides a New Card / Express Card and Mini PCI-E Card. User interface includes internal keyboard, touch pad. Realtek ALC663 High Definition (Azalia) Audio Codec based multimedia interface includes Built-in stereo speaker and woofer, Microphone-in and headphone-out audio jacks. There is one communication the RGMII Giga Ethernet PHY to support RJ-45 LAN jack.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows Vista to take full advantage of the hardware capabilities. Features such as bus mastering IDE, Plug and Play, Advanced Configuration Power Interface (ACPI) with application restart, software-controlled power shutdown.

1.2 System Hardware Parts-1

Basic Function		Spec	Remark
CPU			
	Type	Intel Arrandale CPU	
	TDP	45/35W (Processor/chipset SOC)	
Display		18.4 SWXGA + Glare/Non Glare	1680x945 HD+
		-Max Brightness :TBD	1920x1080 FHD
Chipset		Ibex Peak Chipset	
Memory		0 MB on board	
	Type	DDRIII SO-DIMM 1066/1333 MHz	
	Slot	2 SO-DIMM	
	Max Size	8GB	
Graphic		ATI M96-XT	
	VRAM	1GB	
	No. chips	64x16x8	
	Function	Display	
Audio			
	Interface	Azalia	ALC633, Vista Criteria
	Speaker	2.5 W speak x2 3Wx1	
	Int. Mic	1	
	Other	Dolby Home Theater Logo	

1.2 System Hardware Parts-2

Basic Function		Spec	Remark
Express Card			
	Slot Type	Express 54 x1	USB & PCI-E
	Function	Wake on ring support	X
		To be able to disable by BIOS	X
Card Reader		4 in 1 Card Reader	
	Slot Type	MS / MS PRO / SD / MMC	
	Access LED	N/A	
	Function	SDHC Support	
Storage Device		Spec	Remark
HDD		SATA I/F,2.5” 9.5mm height HDD	
	Function		
	Structure	CBB Compliant	
ODD		SATA I/F,12.7mm height ODD	
	Type	Super Multi/BD	
	Structure	CBB Compliant	
	Bezel	G-BASE	

1.2.1 Intel Arrandale CPU Processor

1.2.1.1 CPU – Intel Arrandale

Arrandale Processor Introduction

Arrandale is the next generation of 64-bit, multi-core mobile processor built on 32- nanometer process technology. Throughout this document, Auburndale may be referred to as simply the processor. Based on the low-power/high-performance Nehalem micro-architecture, the processor is designed for a two-chip platform as opposed to the traditional three-chip platforms (processor, GMCH, and ICH). The two-chip platform consists of a processor and the Platform Controller Hub (PCH) and enables higher performance, lower cost, easier validation, and improved x-y footprint. The PCH may also be referred to as Mobile Intel® 5 Series Chipset (formerly Ibex Peak- M). Auburndale is designed for the Calpella platform and is offered in an rPGA988A or a BGA1288 package. Included in this family of processors is an integrated graphics and memory controller die on the same package as the processor core die. This two-chip solution of a processor core die with an integrated graphics and memory controller die is known as a multi-chip package (MCP) processor.

Note: Integrated graphics and memory controller die is built on 32-nanometer process technology

Processor Feature Details

- Four execution cores
- A 32-KB instruction and 32-KB data first-level cache (L1) for each core
- A 256-KB shared instruction/data second-level cache (L2) for each core

- Up to 8-MB shared instruction/data last-level cache (L3), shared among all cores
- Intel® Virtualization Technology (Intel® VT-x)
- Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
- Intel® Trusted Execution Technology (Intel® TXT)
- Intel® Streaming SIMD Extensions 4.1 (Intel® SSE4.1)
- Supplemental Streaming SIMD Extensions 4.2 (Intel® SSE4.2)
- Intel® Hyper-Threading Technology (Intel® HT Technology)
- Intel® 64 architecture
- Execute Disable Bit
- Intel® Turbo Boost Technology

1.2.1.2 Mobile Intel Arrandale system memory support

The Integrated Memory Controller (IMC) supports DDR3 protocols with two, independent, 64-bit wide channels each accessing one SO-DIMM. It supports a maximum of one, unbuffered non-ECC DDR3 SO-DIMM per-channel thus allowing up to two device ranks per-channel. DDR3 Data Transfer Rates: — 800 MT/s (PC3-6400), and 1066 MT/s (PC3-8500)

➢DDR3 SO-DIMM Modules:

— Raw Card A – double-sided x16 unbuffered non-ECC

— Raw Card B – single-sided x8 unbuffered non-ECC

— Raw Card C – single-sided x16 unbuffered non-ECC

— Raw Card D – double-sided x8 (stacked) unbuffered non-ECC

— Raw Card F – double-sided x8 (planar) unbuffered non-ECC

➢ DDR3 DRAM Device Technology:

— Standard 1-Gb, and 2-Gb technologies and addressing are supported for x16 and x8 devices. There is no support for memory modules with different technologies or capacities on opposite sides of the same memory module. If one side of a memory module is populated, the other side is either identical or empty.

System Memory Timing Support

The IMC supports the following DDR3 Speed Bin, CAS Write Latency (CWL), and command signal mode timings on the main memory interface:

- tCL = CAS Latency
- tRCD = Activate Command to READ or WRITE Command delay
- tRP = PRECHARGE Command Period
- CWL = CAS Write Latency
- Command Signal modes = 1n indicates a new command may be issued every clock and 2n indicates a new command may be issued every 2 clocks. Command launch mode programming depends on the transfer rate and memory configuration.

System Memory Organization Modes

The IMC supports two memory organization modes, single-channel and dual-channel. Depending upon how the SO-DIMM Modules are populated in each memory channel, a number of different configurations can exist.

Rules for Populating Memory Slots

In all modes, the frequency of system memory is the lowest frequency of all memory modules placed in the system, as determined through the SPD registers on the memory modules. The system memory controller supports only one SO-DIMM connector per channel. For dual-channel modes both channels must have an SO DIMM connector populated. For single-channel mode, only a single-channel can have an SO-DIMM connector populated.

1.2.2 Intel Platform control HUB Ibex Peak chipset

1.2.2.1 Introduction

- Direct Media Interface

—10 Gb/s each direction, full duplex

—Transparent to software

- PCI Express*

—NEW: 8 PCI Express root ports

—NEW: PCI Express 2.0 specification running at 2.5GT/s.

—NEW: Ports 1-4 and 5-8 can independently be configured to support eight x1s, two x4s, two x2s and four x1s, or one x4 and four x1 port widths.

—Support for full 2.5 Gb/s bandwidth in each direction per x1 lane

—Module based Hot-Plug supported (e.g., ExpressCard*)

- PCI Bus Interface

—Supports PCI Rev 2.3 Specification at 33 MHz

—Four available PCI REQ/GNT pairs

—Support for 64-bit addressing on PCI using DAC protocol

- Integrated Serial ATA Host Controller

—Up to six SATA ports

—Data transfer rates up to 3.0 Gb/s (300 MB/s).

—Integrated AHCI controller

- External SATA support

—NEW: Port Disable Capability

- Intel®High Definition Audio Interface

—PCI Express endpoint

—Independent Bus Master logic for eight general purpose streams: four input and four output

—Support four external Codecs

—Supports variable length stream slots

—Supports multichannel, 32-bit sample depth, 192 kHz sample rate output

—Provides mic array support

—Allows for non-48 kHz sampling output

—Support for ACPI Device

- USB 2.0

—NEW: Two USB 2.0 Rate Matching Hubs to replace functionality of UHCI controllers

—Two EHCI Host Controllers, supporting up to fourteen external ports

—Per-Port-Disable Capability

—Includes up to two USB 2.0 High-speed Debug Ports

—Supports wake-up from sleeping states S1-S4

—Supports legacy Keyboard/Mouse software

- Integrated Gigabit LAN Controller

—NEW: PCI Express* connection

—Integrated ASF Management Controller

—Network security with System Defense

—Supports IEEE 802.3

—10/100/1000 Mbps Ethernet Support

—Jumbo Frame Support

- Power Management Logic

—Supports ACPI 3.0b

—ACPI-defined power states (processor driven C states)

—ACPI Power Management Timer

—SMI# generation

—All registers readable/restorable for proper resume from 0 V suspend states

—Support for APM-based legacy power management for non-ACPI implementations

- Enhanced DMA Controller

—Two cascaded 8237 DMA controllers

—Supports LPC DMA

- SMBus

—Faster speed, up to 100 kbps

—Flexible SMBus/SMLink architecture to optimize for ASF

—Provides independent manageability bus through SMLink interface

—Supports SMBus 2.0 Specification

—Host interface allows processor to communicate via SMBus

—Slave interface allows an internal or external Microcontroller to access system resources

—Compatible with most two-wire components that are also I2C compatible

- High Precision Event Timers

—Advanced operating system interrupt scheduling

- Real-Time Clock

—256-byte battery-backed CMOS RAM

—Integrated oscillator components

—Lower Power DC/DC Converter implementation

- Serial Peripheral Interface (SPI)

—Supports up to two SPI devices

—Supports 20 MHz, 33 MHz SPI devices

—Support up to two different erase granularities

- Interrupt Controller

—Supports up to eight PCI interrupt pins

—Supports PCI 2.3 Message Signaled Interrupts

—Two cascaded 82C59 with 15 interrupts

—Integrated I/O APIC capability with 24 interrupts

—Supports Processor System Bus interrupt delivery

- Firmware Hub I/F supports BIOS Memory size up to 8 MBytes
- Low Pin Count (LPC) I/F

—Supports two Master/DMA devices.

—Support for Security Device (Trusted Platform Module) connected to LPC.

- Package

—27 mm x 27 mm FCBGA (Desktop Only)

—27 mm x 25 mm FCBGA (Mobile Only)

—22 mm x 20 mm FCBGA (Mobile SFF Only)

- Analog Display Port
- Digital Display

—Three Digital Display ports capable of supporting HDMI/DVI and Display port

—One Digital Display port supporting SDVO

—LVDS

1.2.2.2 Features and Functions

Digital Media Interface (DMI)

Digital Media Interface (DMI) is the chip-to-chip connection between the processor and Ibex Peak chipset. This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities. Base functionality is completely software-transparent, permitting current and legacy software to operate normally.

PCI Express Interface*

The Ibex Peak provides up to 8 PCI Express Root Ports, supporting the *PCI Express Base Specification*, Revision 2.0. Each Root Port supports 2.5 GB/s bandwidth in each direction (5 GB/s concurrent). PCI Express Root Ports 1-4 can be statically configured as four x1 Ports or ganged together to form one x4 port. Ports 5 and 6 can only be used as two x1 ports.

Serial ATA (SATA) Controller

The Ibex Peak has two integrated SATA host controllers that support independent DMA operation on up to six ports and supports data transfer rates of up to 3.0 GB/s (300 MB/s). The SATA controller contains two modes of operation – a legacy mode using I/O space, and an AHCI mode using memory space. Software that uses legacy mode will not have AHCI capabilities. The Ibex Peak supports the Serial ATA Specification, Revision 1.0a. The Ibex Peak also supports several optional sections of the Serial ATA II: Extensions to Serial ATA 1.0 Specification, Revision 1.0 (AHCI support is required for some elements).

PCI Interface

The Ibex Peak PCI interface provides a 33 MHz, Revision 2.3 implementation. The Ibex Peak integrates a PCI arbiter that supports up to four external PCI bus masters in addition to the internal Ibex Peak requests. This allows for combinations of up to four PCI down devices and PCI slots.

Low Pin Count (LPC) Interface

The Ibex Peak implements an LPC Interface as described in the LPC 1.1 Specification. The Low Pin Count (LPC) bridge function of the Ibex Peak resides in PCI Device 31:Function 0. In addition to the LPC bridge interface function, D31:F0 contains other functional units including DMA, interrupt controllers, timers, power management, system management, GPIO, and RTC.

Serial Peripheral Interface (SPI)

The Ibex Peak implements an SPI Interface as an alternative interface for the BIOS flash device. An SPI flash device can be used as a replacement for the FWH, and is required to support Gigabit Ethernet, Intel® Active Management Technology and integrated Intel® Quiet System Technology. The Ibex Peak supports up to two SPI flash devices with speed up to 33 MHz utilizing two chip select pins.

Universal Serial Bus (USB) Controllers

The Ibex Peak contains up to two Enhanced Host Controller Interface (EHCI) host controllers that support USB high-speed signaling. High-speed USB 2.0 allows data transfers up to 480 Mb/s which is 40 times faster than full-speed USB. The Ibex Peak also contains up to seven Universal Host Controller Interface (UHCI) controllers that support USB full-speed and low-speed signaling.

Note: UHCI's are for debug purposes only and not a production feature.

The Ibex Peak supports up to fourteen USB 2.0 ports. All fourteen ports are highspeed, full-speed, and low-speed capable. Ibex Peak's port-routing logic determines whether a USB port is controlled by one of the UHCI or EHCI controllers. See Section 5.18 and Section 5.19 for details.PBGA

Gigabit Ethernet Controller

The Gigabit Ethernet Controller provides a system interface via a PCI function. The controller provides a full memory-mapped or IO mapped interface along with a 64 bit address master support for systems using more than 4 GB of physical memory and DMA (Direct Memory Addressing) mechanisms for high performance data transfers. Its bus master capabilities enable the component to process high-level commands and perform multiple operations; this lowers processor utilization by off-loading communication tasks from the processor. Two large configurable transmit and receive FIFOs (up to 20 KB each) help prevent data underruns and overruns while waiting for bus accesses. This enables the integrated LAN controller to transmit data with minimum interframe spacing (IFS). The LAN controller can operate at multiple speeds (10/100/1000 MB/s) and in either full duplex or half duplex mode. In full duplex mode the LAN controller adheres with the IEEE 802.3x Flow Control Specification. Half duplex performance is enhanced by a proprietary collision reduction mechanism. See Section 5.3 for details..

RTC

The Ibex Peak contains a Motorola MC146818A-compatible real-time clock with 256 bytes of battery-backed RAM. The real-time clock performs two key functions: keeping track of the time of day and storing system data, even when the system is powered down. The RTC operates on a 32.768 KHz crystal and a 3 V battery. The RTC also supports two lockable memory ranges. By setting bits in the configuration space, two 8-byte ranges can be locked to

read and write accesses. This prevents unauthorized reading of passwords or other system security information. The RTC also supports a date alarm that allows for scheduling a wake up event up to 30 days in advance, rather than just24 hours in advance.

Intel® High Definition Audio Controller

The Intel® High Definition Audio Specification defines a digital interface that can be used to attach different types of codecs, such as audio and modem codecs. The Ibex Peak Intel® HD Audio controller supports up to 4 codecs. The link can operate at either 3.3 V or 1.5 V. With the support of multi-channel audio stream, 32-bit sample depth, and sample rate up to 192 kHz, the Intel® HD Audio controller provides audio quality that can deliver CE levels of audio experience. On the input side, the Ibex Peak adds support for an array of microphones.

System Management Bus (SMBus 2.0)

The Ibex Peak contains an SMBus Host interface that allows the processor to communicate with SMBus slaves. This interface is compatible with most I2C devices. Special I2C commands are implemented. The Ibex Peak's SMBus host controller provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves). Also, the Ibex Peak supports slave functionality, including the Host Notify protocol. Hence, the host controller supports eight command protocols of the SMBus interface (see System Management Bus (SMBus) Specification, Version 2.0): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, Block Read/Write, and Host Notify. Ibex Peak's SMBus also implements hardware-based Packet Error Checking for data robustness and the Address Resolution Protocol (ARP) to dynamically provide address to all SMBus devices.

1.2.3 ATI M96 series GDDR3 1Gb (64Mx16) – K4W1G1646E

- VDD/VDDQ= 1.5V ± 0.075V at 1066/1333/1600/1800/2000
- 533MHz fCK for 1066Mb/sec/pin, 667MHz fCK for 1333Mb/sec/pin, 800MHz fCK for 1600Mb/sec/pin 900MHz fCK for 1800Mb/sec/pin,1000MHz fCK for 2000Mb/sec/pin
- 8 Banks
- Posted CAS
- Programmable CAS Latency(posted CAS): 7,9,11,12,13
- Programmable Additive Latency: 0, CL-2 or CL-1 clock
- Programmable CAS Write Latency: (CWL) =6 (1066Mbps), 7(1333Mbps), 8(1600Mbps), 9(1800Mbps),10(2000Mbps)
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address “000” only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data-Strobe
- Internal(self) calibration : Internal self calibration through ZQ pin(RZQ : 240 ohm ± 1%)
- On Die Termination using ODT pin

• Average Refresh Period: 7.8us at lower than TCASE 85°C, 3.9us at 85°C < TCASE < 95 °C

• Asynchronous Reset

• Package : 96 balls FBGA - x16

• All of Lead-Free products are compliant for RoHS

• All of products are Halogen-Freetr

1.2.4 Realtek ALC633 High Definition Audio System

The ALC663 is a 5.1 Channel High Definition Audio Codec designed for Windows system. Its performance and functionality meet the latest Microsoft® WLP (Windows Logo Program) 3.10 and future requirement date of June 01,2008.

Featuring three stereo DACs, two stereo ADCs, legacy analog input to analog output mixing, one stereo digital microphone converter and two independent S/PDIF output converters to provide a fully integrated audio solution for multimedia desktop and mobile PCs, and ultra mobile devices.

Two stereo ADCs and one stereo digital microphone converter support analog microphone recording and digital microphone recording simultaneously with Realtek proprietary Acoustic Echo Cancellation (AEC), Beam Forming (BF), and Noise Suppression (NS) technologies, to improve user experience for VoIP and voice recognition such as applications relay on good voice quality.

Multiple analog IO (except MONO, PCBEEP and HP-OUT) are input and output capable with headphone amplifiers. Four linear headphone amplifiers are integrated to drive earphones on port-A, port-D, port-E and port-F. The fifth headphone amplifier on port-I (HPOUT) is designed to drive earphone without external DC blocking capacitors, reducing pop noise caused by the DC blocking capacitors.

ALC663 provides two independent S/PDIF output and supports 16/20/24-bit S/PDIF output function and a sampling rate of up to 192kHz. The primary S/PDIF output offers connection of PCs to high quality consumer electronic products such as digital decoders and speakers. The secondary S/PDIF output is used to output digital stream to HDMI transmitter is getting more popular in high-end multimedia PC.

Addition to the audio functions, ALC663 supports enhanced power management. Its power management design is compliant to the latest Intel low power ECR, saves more power consumption when audio function is not being used, offering wake up for jack detection when system is in power down state, which can extend battery life for mobile system without sacrificing audio features.

The ALC663 supports host audio from the Intel ICH series chipset, and also from any other HAD compatible audio controller. With software utilities like Karaoke mode, environment emulation, multi-band software equalizer, dynamic range compressor and extender, optional Dolby® Digital Live, DTS® CONNECT™, Dolby® Home Theater, and SRS® programs, ALC663 provides an excellent home entertainment package and game experience.

1.2.5 APA2031 Audio Amplifier and APA3010 subwoofer

APA2031

APA2030/1 is a monolithic integrated circuit, which provides internal gain control, and a stereo bridged audio power amplifiers capable of producing 2.6W (1.9W) into 3Ω with less than 10% (1.0%) THD+N. By control the two gain setting pins, Gain0 and Gain1, The amplifier can provide 6dB, 10dB, 15.6dB, and 21.6dB gain settings. The advantage of internal gain setting can be less components and PCB area. Both of the depop circuitry and the thermal shutdown protection circuitry are integrated in APA2030/1, that reduces pops and clicks noise during power up or shutdown mode operation. It also improved the power off pop noise and protects the chip from being destroyed by over temperature and short current failure. To simplify the audio system design APA2030 combines a stereo bridge-tied loads (BTL) mode for speaker drive and a stereo single-end (SE) mode for headphone drive into a single chip, where both modes are easily switched by the SE/BTL input control pin signal. Besides the multiple input selections is used for portable audio system. APA2031 eliminates both input selection and single-end (SE) mode function to simplifying the design and save the PCB space.

APA3010

- Operating Voltage : 2.5V-5.5V
- Bridge-Tied Load (BTL) Mode Operation
- Supply Current – IDD=7mA at VDD=5V
- Low Shutdown Current – IDD=0.1mA

- Low Distortion

–2.5W, at VDD=5V, BTL, RL=3W

THD+N=0.1%

–2.1W, at VDD=5V, BTL, RL=4W

THD+N=0.1%

- Output Power

at 1% THD+N

–2.6W, at VDD=5V, BTL, RL=3W

–2.3W, at VDD=5V, BTL, RL=4W

at 10% THD+N

–3.3W at VDD=5V, BTL, RL=3W

–2.7W at VDD=5V, BTL, RL=4W

- Depop Circuitry Integrated
- Thermal shutdown protection and over current protection circuitry

- High supply voltage ripple rejection
- Surface-Mount Packaging

–MSOP-8-P (with enhanced thermal pad)

–SOP-8-P (with enhanced thermal pad)

- Lead Free Available (RoHS Compliant)

1.2.6 Keyboard System – IT8512 Universal Keyboard Controller

- 8032 Embedded Controller

- Twin Turbo version/3-stage pipeline

- 9.2 MHz for EC domain and 8032 internal timer

- Variable frequency range to gain the maximum 8032 code-fetch performance

-Instruction set compatible with standard 8051/2

- LPC Bus Interface

- Compatible with the LPC specification v1.1

- Supports I/O read/write

- Supports Memory read/write

- Supports FWH read/write

-Serial IRQ

➢ Flash Interface

- Behaves as a LPC/FWH memory device

(HLPC) to the host SouthBridge

- Supports external serial flash with 32.3~64.5

MHz

- Up to 16M bytes Flash space shared by the host

and EC side (serial flash)

➢ SM Bus Controller

- SM Bus spec. 2.0

- 3 SM Bus masters

- 3 SM Bus channels

- System Wake Up Control

- Modem RI# wake up

- Telephone RING# wake up

- IRQ/SMI routing

- EC Wake Up Control

- 40 external/internal wake up events

- Interrupt Controller

- 48 interrupt events to EC

- Fixed priority

- Timer / Watch Dog Timer

- 3 16-bit multi-function timers inside 8032, which

is based on EC clock

- 1 watch dog timer inside 8032, which is based

on EC clock

- 1 external WDT in ETWD module, which is

based on 32.768 k clock source

- UART

-1 full duplex UART inside 8032

- ACPI Power Management Channel

- 2 Power management channels

- Compatible and enhanced mode

- Battery-backed SRAM

- Supports 64-byte battery-backed memory

space

- Supports power-switch circuit

- GPIO

- Supports 73-port GPIO with serial flash

- Programmable pull up/pull down

- Schmitt trigger for input

- External GPIO Controller (EGPC)

- Communicate with 4 IT8301 chips

-Each IT8301 supports 38 GPIO ports

- KBC Interface

- 8042 style KBC interface

- Legacy IRQ1 and IRQ12

- Fast A20G and KB reset

- ADC

- 12 ADC channels (8 external)

- 10-bit resolution (+/- 4LSB)

- Digital filter for noise reduction

- DAC

- 6 DAC channels

- 8-bit DAC

- PWM

- 8 PWM channels

- Base clock frequency is 32.768 kHz

- 8 duty cycle resolution

- 8/16-bit common input clock prescaler

- 4 prescalers for 8 PWM output used for devices

with different frequencies

- 2 Tachometers for measuring fan speed

- Complete resolution 256 PWM output

supported. (CR256)

- PS/2 Interface

- 3 PS/2 interface

- Hardware/Software mode selection

- KB Matrix Scan

- Hardware keyboard scan

- 18x8 keyboard matrix scan

1.2.7 System SPI Flash Memory (BIOS) –EN25F16

The EN25F16 is a 16M-bit (2048K-byte) Serial Flash memory, with advanced write protection mechanisms, accessed by a high speed SPI-compatible bus. The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction. The EN25F16 is designed to allow either single Sector at a time or full chip erase operation. The EN25F16 can be configured to protect part of the memory as the software protected mode. The device can sustain a minimum of 100K program/erase cycles on each sector.

- Single power supply operation

- Full voltage range: 2.7-3.6 volt

- 16 Mbit Serial Flash

- 16 M-bit/2048 K-byte/8192 pages

- 256 bytes per programmable page

- High performance

- 100MHz clock rate

- Low power consumption

- 5 mA typical active current

- 1 μA typical power down current

- Uniform Sector Architecture:

- 512 sectors of 4-Kbyte

- 32 blocks of 64-Kbyte

- Any sector or block can be erased individually

- Software and Hardware Write Protection:

- Write Protect all or portion of memory viasoftware

- Enable/Disable protection with WP# pin

- High performance program/erase speed

- Page program time: 1.5ms typical

- Sector erase time: 150ms typical

- Block erase time 800ms typical

- Chip erase time: 18 Seconds typical

- Lockable 256 byte OTP security sector
- Minimum 100K endurance cycle
- Package Options

- 8 pins SOP 200mil body width

- 8 contact VDFN

- 8 pins PDIP

- 16 pin SOP 300mil body width

- All Pb-free packages are RoHS compliant

1.2.8 Card Reader - RTS5159

The RTS5159 is an ultimate throughput USB 2.0 compliant card reader controller that integrates USB 2.0 Transceiver, MCU, SIE, regulators and memory card access units into a single chip. The RTS5159 can support Memory Stick TM, Memory Stick Pro TM, Memory Stick PRO-HG Duo TM, Secure Digital TM, Multi-Media Card TM and xD-Picture Card TM, but only 1-LUN configuration, i.e. only one of these memory cards can be inserted into RTS5159 system at the same time.

A serial EEPROM interface is provided here that could store the desired pre-configuration information.

The RTS5159 integrates 3.3V-to-1.8V regulator, clock generation circuitry and MOSFET, and could dramatically reduce the system BOM cost.

- Compliant with Universal Serial Bus Specification Revision 2.0
- Compliant with USB Mass Storage Class Bulk only Transport Specification Rev. 1.0
- Support High-speed (480Mbps) and Full-speed (12Mbps) Data Transfer
- USB bus power operation
- Support Control, Bulk IN / OUT data pipes
- Support the following memory card interfaces:

-Secure Digital TM (SD), MultiMediaCard TM (MMC), Mini-SD, Micro-SD (T-flash), RS-MMC, Mobile-MMC and MMC-micro

-Memory Stick TM (MS), Memory Stick PROTM (MS-PRO), MS Duo, MS-PRO Duo and Micro-MS (M2)

-MSPRO-HG Duo 8-bit mode

-xD-Picture Card TM (xD) including Type M and Type H

- Support hardware ECC (Error Correction Code) function

- Support hardware CRC (Cyclic Redundancy Check) function
- Programmable clock rate for flash memory card interfaces
- Support MS-PRO v1.02
- Support MS v1.43
- Support MS PRO-HG Duo v1.01
- Support SD version 2.0
- Support MMC version 4.2

1.2.10 RGMII LAN PHY - RTL8111D

The Realtek RTL8111D-GR/RTL811DL-GR Gigabit Ethernet controller combines a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, PCI Express bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8111D/RTL8111DL offers high-speed transmission over CAT5 UTP cable or CAT3 UTP (10Mbps only) cable. Functions such as Crossover Detection and Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The RTL8111D-GR/RTL811DL supports Receive Side Scaling (RSS) to hash incoming TCP connections and load-balance received data processing across multiple CPUs. RSS improves the number of transactions per second and number of connections per second, for increased network throughput.

The device also features inter-connect PCI Express technology. PCI Express is a high-bandwidth, low pin count, serial, interconnect technology that offers significant improvements in performance over conventional PCI and also maintains software compatibility with existing PCI infrastructure. The device embeds an adaptive equalizer in the PCIe PHY for ease of system integration and excellent link quality. The equalizer enables the length of the PCB traces to reach 40 inches.Other Functions

1.3 Other Function

1.3.1 Hot Key Function

Keys Combination	Feature	Meaning
Fn + F1	Wireless LAN ON/OFF	Enable or Disable Wireless LAN Function
Fn + F2	Bluetooth ON/OFF	Enable or Disable Bluetooth Function
Fn + F3	Volume down	Audio Volume down
Fn + F4	Volume up	Audio Volume up
Fn + F5	LCD/external CRT switching	Rotate display mode in LCD only, CRT only, and simultaneously display.
Fn + F6	Brightness down (8 levels)	Decreases the LCD brightness
Fn + F7	Brightness up (8 levels)	Increases the LCD brightness
Fn + F8		
Fn + F9		
Fn + F10	Mute ON/OFF	Toggle Mute on/off
Fn + F11	Panel ON/OFF	Toggle Panel on/off
Fn + F12	Suspend to DRAM / HDD	Force the computer into either Suspend to HDD or Suspend to DRAM mode depending on BIOS Setup.

1.3.2 Power on/off/Suspend/Resume Button

1.3.2.1 APM Mode

At APM mode, Power button is on/off system power.

1.3.2.2 ACPI Mode

At ACPI mode, Windows power management control panel set power button behavior.

You could set "standby", "power off" or "hibernate"(must enable hibernate function in power Management) to power button function.

Continue pushing power button over 4 seconds will force system off at ACPI mode.

1.3.3 Cover Switch (Hall Sensor)

System automatically provides power saving by monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover.

At ACPI mode there are three functions to be chosen at Windows XP power management control panel.

1. None

2. Standby

3. Off

4. Hibernate (must enable hibernate function in power management

1.3.4 LED Indicators

System has six status LED indicators to display system activity, which include six above Front Bezel and MMB LED indicators.

1.3.4.1 Six LED Indicators

LED Indicators Definition		System State				
		S1/S2	S3	S4	S5	Location
LED	**function status**					Front Bezel
Battery Charge LED	Battery Full Charged	Off	Off	Off	Off	Left 1
	Battery charging	Blue	Blue	Blue	Blue	
	Battery Critical Low	Blue Blink	Blue Blink	Blue Blink	Blue Blink	
Wlan	WLAN Enable	Blue	Off	Off	Off	Left 2
	WLAN Disable	Off	Off	Off	Off	
BT	BT Enable	Blue	Off	Off	Off	Left 3
	BT Disable	Off	Off	Off	Off	
CAP	CAP Enable	Blue	Off	Off	Off	Left 4
	CAP Disable	Off	Off	Off	Off	
Num Lock	Num lock Enable	Blue	Off	Off	Off	Left 5
	Num lock Disable	Off	Off	Off	Off	
HDD/ODD lock	HDD/ODD Enable	Blue	Off	Off	Off	Left 6
	HDD/ODD Disable	Off	Off	Off	Off	
Power Status		Blue	Blue Blink	Off	Off	Power Button

1.3.5 Battery status

1.3.5.1 Battery Warning

System also provides Battery capacity monitoring and gives user a warning so that users have chance to save his data before battery dead. Also, this function protects system from mal-function while battery capacity is low. Battery Warning: Capacity below 10%, Battery Capacity LED flashes per second, system beeps per 2 seconds. System will suspend to HDD after 2 Minutes to protect user’s data.

1.3.5.2 Battery Low State

After Battery Warning State, and battery capacity is below 5%, system will generate beep sound for twice per second.

1.3.5.3 Battery Dead State

When the battery voltage level reaches 7.4 volts, system will shut down automatically in order to extend the battery packs' life.

1.3.6 Fan Power on/off Management

1.3.6.1 CPU Fan

FAN is controlled by W83L951AD embedded controller-using F75385 to sense CPU temperature and W83L951AD PWM control fan speed. Fan speed is depended on CPU temperature. Higher CPU temperature will get faster Fan Speed.

1.3.7 CMOS Battery

There is a Standard CR2032 3V 220mAh lithium coin battery to supply RTC power. When AC in or system main battery inside, CMOS battery consumes no power to save coin battery’s life cycle.

1.4 Peripheral Components

1.4.1 LCD Panel

- 18.4 SWXGA + Glare/Non Glare

1.4.2 HDD

- SATA I/F, 2.5” 9.5mm height HDD
- 80/100/120/160 GB, CBB

1.4.3 ODD

- SATA I/F, 12.7mm height ODD
- Super Multi/BlueRay

1.4.4 DDR SO-DIMM

- 0MB DDRII SDRAM memory on board
- 2 SO- DIMM slots for memory expansion
- 200pin DDRIII 800 1/2/4GB SDRAM SO-DIMM Memory Module

1.4.5 Keyboard

- European keyboard layout
- 18.45mm key pitch / 2.6mm stroke

1.5 Power Management

The 9270D system has built in several power saving modes to prolong the battery usage. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key). Following are the descriptions of the power management modes supported.

1.5.1 System Management Mode

- Full on mode

  In this mode, each device is running with the maximal speed. CPU clock is up to its maximum.

- Doze Mode

  In this mode, CPU will be toggling between on & stop grant mode either. The technology is clock throttling. This can save battery power without loosing much computing capability.

  The CPU power consumption and temperature is lower in this mode.

- Standby Mode

  For more power saving, it turns of the peripheral components. In this mode, the following is the status of each device:

  - CPU: Stop grant

- LCD: backlight off

- HDD: spin down

- Suspend to DRAM

The most chipset of the system is entering power down mode for more power saving. In this mode, the following is the status of each device:

-- CPU: off

-- Twister K: Partial off

-- VGA: Suspend

-- New Card: Suspend

-- Audio: off

-- SDRAM: self refresh

- Suspend to HDD

-- All devices are stopped clock and power-down

-- System status is saved in HDD

-- All system status will be restored when powered on again

1.5.2 Battery Only Power off Mode

The 9270D system has built in Battery only power off mode to prolong the battery usage. In this mode, Universal Keyboard Controller (KBC) will be power off. In addition, the system leakage current shall be less than 0.5mA; therefore system power consumption is lower in this mode.

1.6 Appendix

1.6.1 IBEX PEAK-M GPIO Setting Table-1

Name	Pin	Type	Power well	Tolerance	Default	Original Define	HW Function
GPIO0	Y3	I/O	Core	3V	GPI	BMBUSY#/GPIO0	GPIO0
GPIO1	C38	I/O	Core	3V	GPI	TACH1/GPIO1	EXTSMI#
GPIO2	B41	I/OD	Core	5V	GPI	PIRQE#/GPIO2	PCI_INTPIRQE#
GPIO3	K53	I/OD	Core	5V	GPI	PIRQF#/GPIO3	PCI_INTPIRQF#
GPIO4	A36	I/OD	Core	5V	GPI	PIRQG#/GPIO4	PCI_INTPIRQG#
GPIO5	A48	I/OD	Core	5V	GPI	PIRQH#/GPIO5	PCI_INTPIRQH#
GPIO6	D37	I/O	Core	3V	GPI	TACH2/GPIO6	WLAN_PD#
GPIO7	J32	I/O	Core	3V	GPI	TACH3/GPIO7	SCI#
GPIO8	F10	I/O	Resume	3V	GPO	GPIO8	GPIO8
GPIO9	G16	I/O	Resume	3V	Native	USB_OC5#/GPIO9	Reserve
GPIO10	F12	I/O	Resume	3V	Native	USB_OC6#/GPIO10	Reserve
GPIO11	B9	I/O	Resume	3V	Native	SMBALERT#/GPIO11	GPIO11
GPIO12	K9	I/O	Resume	3V	GPI	LAN_PHY_PWR_CTRL/GPIO12	GPIO12
GPIO13	J30	I/O	Resume	3V	GPI	HAD_DOCK_RST#/GPIO13	Reserve
GPIO14	T15	I/O	Resume	3V	Native	OC7#/GPIO14	Reserve
GPIO15	T7	I/O	Resume	3V	GPO	GPIO15	GPIO15
GPIO16	AA2	I/O	Core	3V	GPI	SATA4GP/GPIO16	LAN_ISOLATEB
GPIO17	F38	I/O	Core	3V	GPI	TACH0/GPIO17	SPI_WP#
GPIO18	U4	I/O	Core	3V	Native	PCIECLKRQ1#/GPIO18	PEC_CLKREQ_MINI#

1.6.1 IBEX PEAK-M GPIO Setting Table-2

Name	Pin	Type	Power well	Tolerance	Default	Original Define	HW Function
GPIO19	V1	I/O	Core	3V	GPI	SATA1GP/GPIO19	GPIO19
GPIO20	N4	I/O	Core	3V	Native	PCIECLKRQ2#/GPIO20	PEB_CLKREQ_NEWCARD#
GPIO21	Y9	I/O	Core	3V	GPI	SATA0GP/GPIO21	BT_ON#
GPIO22	Y7	I/O	Core	3V	GPI	SCLOCK/GPIO22	BIOS_REC
GPIO23	F34	I/O	Core	3V	Native	LDRQ1#/GPIO23	Reserve
GPIO24	H10	I/O	Resume	3V	GPO	GPIO24	SB_MUTE#
GPIO25	A8	I/O	Resume	3V	Native	PCIECLKRQ3#/GPIO25	PCIECLKRQ3
GPIO26	M9	I/O	Resume	3V	Native	PCIECLKRQ4#/GPIO26	PCIECLKRQ4
GPIO27	AB12	I/O	Resume	3V	GPO	GPIO27	GPIO27
GPIO28	V13	I/O	Resume	3V	GPI	GPIO28	GPIO28
GPIO29	F6	I/O	Resume	3V	GPO	SLP_LAN#/GPIO29	PM_SLP_LAN# (no connection)
GPIO30	M1	I/O	Resume	3V	GPI	SUS_PWR_DN_ACK/GPIO30	SUS_PWR_ACK
GPIO31	P7	I/O	Resume	3V	GPI	ACPRESENT/GPIO31	AC_PRESENT (no connection)
GPIO32	Y1	I/O	Core	3V	GPO/Native	CLKRUN#/GPIO32	PM_CLKRUN#
GPIO33	H32	I/O	Core	3V	GPO	HDA_DOCK_EN#/GPIO33	HDA_DOCK_EN#
GPIO34	M11	I/O	Core	3V	GPI	STP_PCI#/GPIO34	GPIO34
GPIO35	V6	I/O	Core	3V	GPO	GPIO35	SB_MB_ID0
GPIO36	AB7	I/O	Core	3V	GPI	SATA2GP/GPIO36	SB_MB_ID1
GPIO37	AB13	I/O	Core	3V	GPI	SATA3GP/GPIO37	SB_MB_ID2

1.6.1 IBEX PEAK-M GPIO Setting Table-3

Name	Pin	Type	Power well	Tolerance	Default	Original Define	HW Function
GPIO38	V3	I/O	Core	3V	GPI	SLOAD/GPIO38	MFG_MODE
GPIO39	P3	I/O	Core	3V	GPI	SDATAOUT0/GPIO39	CRB_SV_DET
GPIO40	J16	I/O	Resume	3V	Native	USB_OC#1/GPIO40	Reserve
GPIO41	F16	I/O	Resume	3V	Native	USB_OC#2/GPIO41	USB_OC#2
GPIO42	L16	I/O	Resume	3V	Native	USB_OC#3/GPIO42	USB_OC3#
GPIO43	F14	I/O	Resume	3V	Native	USB_OC#4/GPIO43	USB_OC3#
GPIO44	H6	I/O	Resume	3V	Native	PCIECLKRQ5#/GPIO44	PCIECLKRQ5
GPIO45	H3	I/O	Resume	3V	Native	PCIECLKRQ6#/GPIO45	PCIECLKRQ6
GPIO46	F1	I/O	Resume	3V	Native	PCIECLKRQ7#/GPIO46	PCIECLKRQ7
GPIO47	H1	I/O	Resume	3V	Native	PEG_A_CLKRQ#/GPIO47	M96_CLKREQ#
GPIO48	AB6	I/O	Core	3V	GPI	SDATAOUT1/GPIO48	GPIO48
GPIO49	AA4	I/O	Core	3V	GPI	SATA5GP/GPIO49/TEMP/ALERT#	Temp_ALERT#
GPIO50	A46	I/O	Core	5V	Native	REQ1#/GPIO50	PCI_REQ1 (no connection)
GPIO51	K45	I/O	Core	3V	Native	GNT1#/GPIO51	PCI_GNT#1 (no connection)
GPIO52	B45	I/O	Core	5V	Native	REQ2#/GPIO52	PCI_REQ2 (no connection)
GPIO53	F36	I/O	Core	3V	Native	GNT2#/GPIO53	Reserve
GPIO54	M53	I/O	Core	5V	Native	REQ3#/GPIO54	PCI_REQ3 (no connection)
GPIO55	H53	I/O	Core	3V	Native	GNT3#/GPIO55	PCI_GNT#3 (no connection)
GPIO56	P13	I/O	Resume	3V	Native	PEG_B_CLKRQ#/GPIO56	LAN_CLKREQ#

1.6.1 IBEX PEAK-M GPIO Setting Table-4

Name	Pin	Type	Power well	Tolerance	Default	Original Define	HW Function
GPIO57	F8	I/O	Resume	3V	GPI	GPIO57	GPIO57
GPIO58	E10	I/O	Resume	3V	Native	SML1CLK/GPIO58	SMBCLK_PCH_KBC
GPIO59	N16	I/O	Resume	3V	Native	USB_OC#0/GPIO59	USB_OC0#
GPIO60	J14	I/O	Resume	3V	Native	SML0ALERT#/GPIO60	GPIO60
GPIO61	P8	I/O	Resume	3V	Native	SUS_STAT#/GPIO61	LPC_PD#
GPIO62	E3	I/O	Resume	3V	Native	SUSCLK/GPIO62	GPIO62
GPIO63	E4	I/O	Resume	3V	Native	SLP_S5#/GPIO63	SLP_S5#
GPIO64	T45	I/O	Core	3V	Native	CLKOUTFLEX0/GPIO64	Reserve
GPIO65	P43	I/O	Core	3V	Native	CLKOUTFLEX1/GPIO65	Reserve
GPIO66	T42	I/O	Core	3V	Native	CLKOUTFLEX2/GPIO66	Reserve
GPIO67	N50	I/O	Core	3V	Native	CLKOUTFLEX3/GPIO67	Reserve
GPIO72	A6	I/O	Resume	3V	Native	BATLOW#/GPIO72	PM_BATLOW(no connection)
GPIO73	P9	I/O	Resume	3V	Native	PCIECLKRQ0#/GPIO73	PCIECLKRQ0
GPIO74	M14	I/O	Resume	3V	Native	SML1ALERT#/GPIO74	GPIO74
GPIO75	G12	I/O	Resume	3V	Native	SML1DATA/GPIO75	SMBDATA_PCH_KBC

1.6.2 KBC IT8512 GPIO Setting Table-1

Pin no	Signal	9270D
24	PWM0/GPA0	LED_CAP#
25	PWM1/GPA1	LED_NUM#
28	PWM2/GPA2	LED_CHARGER#
29	PWM3/GPA3	LED_BATT_R#
30	PWM4/GPA4	RESERVE
31	PWM5/GPA5	KBC_BEEP
32	PWM6/GPA6	FAN_ON
34	PWM7/GPA7	KBC_BLADJ
108	RXD/GPB0	KBC_RX
109	TXD/GPB1	KBC_TX
123	CTX0/GPB2	SUSB_1.8VS
110	SMCLK0/GPB3	BAT_CLK
111	SMDAT0/GPB4	BAT_DATA
126	GA20/GPB5	KBC_A20GATE
4	KBRST#/GPB6	KBC_RCIN#
112	RING#/PWRFAIL#/LPCRST#/GPB7	IRQ#
119	CRX0/GPC0	SUSB_1.05VS
115	SMCLK1/GPC1	SMBCLK_PCH
116	SMDAT1/GPC2	SMBDATA_PCH
56	KSO16/GPC3	KBC_SB_PWRBTN#
120	TMRI0/WUI2/GPC4	SUSB#
57	KSO17/GPC5	SB_RSMRST#
124	TMRI1/WUI3/GPC6	RESERVE
16	PWUREQ#/GPC7	KBC_WAKE_UP#
18	RI1#/WUI0/GPD0	SUSC#
21	RI2#/WUI1/GPD1	ADEN#

1.6.2 KBC IT8512 GPIO Setting Table-2

Pin no	Signal	9270D
22	LPCRST#/WUI4/GPD2	BUF_PLT_RST#
23	ECSCI#/GPD3	KBC_SCI#
15	ECSMI#/GPD4	KBC_EXTSMI#
33	GINT/GPD5	KBC_ENABKL
47	TACH0/GPD6	FAN_SPD
48	TACH1/GPD7	SB_PWRGD_KBC
19	L80HLAT/GPE0	SW_VDD3
82	EGAD/GPE1	PWRON_VDD3S
83	EGCS#/GPE2	SUSB_0.75VS
84	EGCLK/GPE3	SUSC_3V
125	PWRSW/GPE4	PWRBTN#
35	WUI5/GPE5	BAT_TEMP
17	LPCPD#/WUI6/GPE6	LPC_PD#
20	L80LLAT/WUI7/GPE7	RESERVE
85	PS2CLK0/GPF0	TP_CLK
86	PS2DAT0/GPF1	TP_DATA
87	PS2CLK1/GPF2	VCCP_PWRGD
88	PS2DAT1/GPF3	KBD_US/JP#
89	PS2CLK2/WUI20/GPF4	LCD_ENABKL
90	PS2DAT2/WUI21/GPF5	CRT_IN#
117	SMCLK2/WUI22/GPF6	SMBCLK_KBC
118	SMDAT2/WUI23/GPF7	SMBDATA_KBC
106	GPG0	SUSB_1.5VS
107	GPG1/ID7	KBC_MUTE#
100	GPG2	SUSB_5VS
104	GPG6	SUSC_5V

1.6.2 KBC IT8512 GPIO Setting Table-3

Pin no	Signal	9270D
93	CLKRUN#/WUI16/GPH0/ID0	PM_CLKRUN#
94	CRX1/WU117/GPH1/ID1	LID_SW#
95	CTX1/WUI18/GPH2/ID2	SUSC_1.5V
96	WUI19/GPH3/ID3	SUSB_VGA
97	GPH4/ID4	CHARGING
98	GPH5/ID5	SUSB_CPU_CORE
99	GPH6/ID6	LEARNING
66	ADC0/GPI0	BAT_VOLT
67	ADC1/GPI1	GND
68	ADC2/GPI2	GND
69	ADC3/GPI3	I-LIMIT
70	ADC4/GPI4	KBC_MB_ID_0
71	ADC5/GPI5	KBC_MB_ID_1
72	ADC6/GPI6	+KBC_CPUCORE
73	ADC7/GPI7	GND
76	DAC0/GPJ0	I_CTRL
77	DAC1/GPJ1	SUS_PWR_ACK
78	DAC2/GPJ2	PWR_BTN_LED
79	DAC3/GPJ3	DAC_BRIG
80	DAC4/GPJ4	SUSB_VCCP
81	DAC5/GPJ5	SUSB_3VS
1	VSS	GND
2	CK32KE	CK32KE
3	VBAT	GND
5	SERIRQ	SERIRQ
6	LFRAME#	LPC_FRAME#

1.6.2 KBC IT8512 GPIO Setting Table-4

Pin no	Signal	9270D
7	LAD3	LPC_AD3
8	LAD2	LPC_AD2
9	LAD1	LPC_AD1
10	LAD0	LPC_AD0
11	VCC	+3VS
12	VSS	GND
13	LPCCLK	CLK_PCI_KBC
14	WRST#	KBC_RESET#
26	VSTBY	+VDD3
27	VSS	GND
36	KSO0/PD0	KO0
37	KSO1/PD1	KO1
38	KSO2/PD2	KO2
39	KSO3/PD3	KO3
40	KSO4/PD4	KO4
41	KSO5/PD5	KO5
42	KSO6/PD6	KO6
43	KSO7/PD7	KO7
44	KSO8/ACK#	KO8
45	KSO9/BUSY	KO9
46	KSO10/PE	KO10
49	VSS	GND
50	VSTBY	+VDD3
51	KSO11/ERR#	KO11
52	KSO12/SLCT	KO12
53	KSO13	KO13

1.6.2 KBC IT8512 GPIO Setting Table-5

Pin no	Signal	9270D
54	KSO14	KO14
55	KSO15	KO15
58	KSI0/STB#	KI0
59	KSI1/AFD#	KI1
60	KSI2/INIT#	KI2
61	KSI3/SLIN#	KI3
62	KSI4	KI4
63	KSI5	KI5
64	KSI6	KI6
65	KSI7	KI7
74	AVCC	+VDD3_ALW
75	AVSS	ITE_GND
91	VSS	GND
92	VSTBY	+VDD3
101	FSCE#	KBC_SPI_SCSI#
102	FMOSI	KBC_SPI_MOSI
103	FMISO	KBC_SPI_MISO
105	FSCK	KBC_SPI_SCK
113	VSS	GND
114	VSTBY	+VDD3
121	VSTBY	+VDD3
122	VSS	GND
127	VSTBY	VDD3
128	CK32K	CK32KE

1.6.3 9270D Product Spec-1

ITEM	CATEGORY	DESCRIPTION
CPU	Type	Intel Capella PM
	Package	
	TDP	45/35W (Processor/chipset SOC)
	Socket	Socket-P
	FSB	
	Speed	
	Others	
	Assembling Capability	Distribution configurable
System BIOS	Brand	Phoenix
	Size of EEPROM	TBD
	BIOS Architecture	
	Others	
Chipset	Brand & Model Name: North Bridge	None
	Brand & Model Name: South Bridge	Ibex Peak Chipset
	Others	
Memory	Module Type	DDRIII SO-DIMM
	Module Size	1G/2G
	Number of Pins	200
	Speed	800/1066 MHz
	On Board Memory Size	0
	Number of Slot	2
	Form Factor	1.25 inch height
	Maximum Capacity	8GB
	Assembling Capability	Distribution configurable

1.6.3 9270D Product Spec-2

ITEM	CATEGORY	DESCRIPTION
VIDEO CONTROLLER	Type (UMA or Discrete)	Discrete
	Interface	PCI-E
	Brand & Model Name	ATI M96-M2 Pro+
	Marketing Name	ATI Mobility Radeon™ HD 4650
	Others	128bit memory bus/ No TV Out
VRAM	Type	gDDRIII
	No. of Vram Chips	8 pcs
	Local VRAM Size	1GB (64 x 16 x 8pc)
	UMA VRAM Size	
	Others	
Optical Disk Drive	Interface	SATA
	Height	12.7mm
	Type	Super Multi/BD
	Bezel Type	G-BASE
	Others	CBB Compliant
	Assembling Capability	Distribution configurable
Hard Disk Drive	Interface	SATA
	Height & Diameter	9.5mm & 2.5″
	RPM	5400
	Capacity	
	Others	CBB Compliant
	Assembling Capability	Able to assemble at distribution center

1.6.3 9270D Product Spec-3

ITEM	CATEGORY	DESCRIPTION
DISPLAY	Size	18.4″W
	Type	TFT
	Resolution	1680x945 HD+
		1920x1080 FHD
	Others	
KEYBOARD	Height	5.6mm
	Pitch	18.45mm
	Stroke	2.6mm
	Width	339mm
	Layout	US/UI
	Others	
POINTING DEVICE	Type	Underplastic touchpad without scroll bar
	Number of Button	2
	Others	(Gesture version)
PC Card slot	Type	New Card Type II 54mm
	Interface	PCIE/USB
	Number of Slot	1
Audio System	Interface	Azalia
	Output Channels	5.1 analog output
	Speaker	Two 2.5W stereo speaker
	Subwoofer	3W
	Volume Control	keyboard function key
	Internal Microphone	x 1
	Others	

1.6.3 9270D Product Spec-4

ITEM	CATEGORY	DESCRIPTION
Memory Card Reader	Ejection Type	
	Type of Card Support	SD/MS/MS Pro/MMC
	Others	
I/O Port	USB	3 (USB 2.0)
	USB/e-SATA	1
	RJ-11	N/A
	RJ-45	1
	Headphone	1
	S/PDIF	1
	Microphone	1
	Line In	N/A
	DC Input	1
	Analog VGA Port	1
	DVI-D	N/A
	DVI-I	N/A
	S-Video Out	N/A
	S-Video In	N/A
	IEEE1394	N/A
	TV in Connector	N/A
	IrDA	N/A
	CIR	N/A
	HDMI	1
	Kensington Lock	1
	Others	N/A

1.6.3 9270D Product Spec-5

ITEM	CATEGORY	DESCRIPTION
Quick Key	Number of Quick Key	
	Definition	
Indicator	Number of Indicator	7
	Definition	WLAN/BT/power/battery charge/cap lock/num lock/HDD & ODD
Modem	Interface	N/A
	Type & Speed	
	Form Factor	
	Assembling Capability	
	Others	
LAN	Interface	LAN Phy
	Speed	10/100/1000 Mbps
Wireless LAN	Interface	PCIE/USB
	Form Factor	Mini PCIE half size
	Type	B/G/N
	Others	
	Assembling Capability	
TV Card	Form Factor	N/A
	Interface	
	Tuner	
	Others	
Bluetooth	Interface	USB
	Version	2.1(EDR)
	Others	

1.6.3 9270D Product Spec-6

ITEM	CATEGORY	DESCRIPTION
Battery	Type	Li-Ion Cylinder
	Number of Cell	9 cell
	Pack Capacity	6600mAH/11.1V (9 cell)
	Battery Life	
	Assembling Capability	user Swappable
AC Adapter	Type	Universal AC adaptor
	Wattage	90W/120W
	Input Voltage	100V ~ 240V
	Output Voltage	19V
	number of Pin	2/3
	D/C jack Dimension	2.5mm*5.5MM*11.5~12.5mm
	Others	2.5mm*5.5MM*11.5~12.5mm
Dimensions	L x W x D mm	W441 x D298.5 x H 25~39mm
Weight	Kg	3.7KG
Other Specifications (a)	Webcam	USB 2.0 interface 1.3M
Other Specifications (b)	MMB module	6 touch sense buttons (TBD), Media , Stop, Play, FF, BF
Other Specifications (C)	RF Receiver	option (USB interface)

1.6.3 9270D Product Spec-7

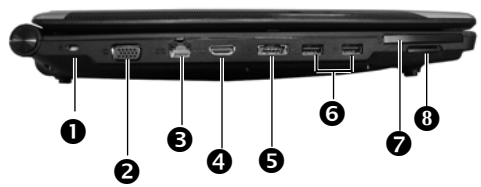
ITEM	CATEGORY	DESCRIPTION
Microsoft LOGO	Windows Logo	Vista Premium SP1
		Windows 7
Regulation	EMC	CE
	Safety	CB
Green Product Coverage	ROHS	Yes

2. System View and Disassembly

2.1 System View

2.1.1 Left-side View

❶ Kensington Lock
❷ CRT Connector
❸ RJ45 Connector
❹ HDMI Connector
❺ ESATA+USB Connector
❻ USB Ports
❼ Card Reader Connector
❽ Express Card Connector



2.1.2 Right-side View

❶ Headphone out

❷ MIC In

❸ SPDIF Connector

❹ ODD

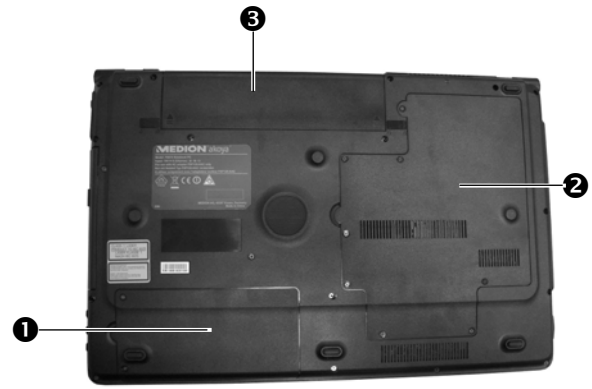
❺ USB Port

❻ Power Jack

2.1.3 Rear View

❶ Ventilation Openings

2.1.4 Bottom View

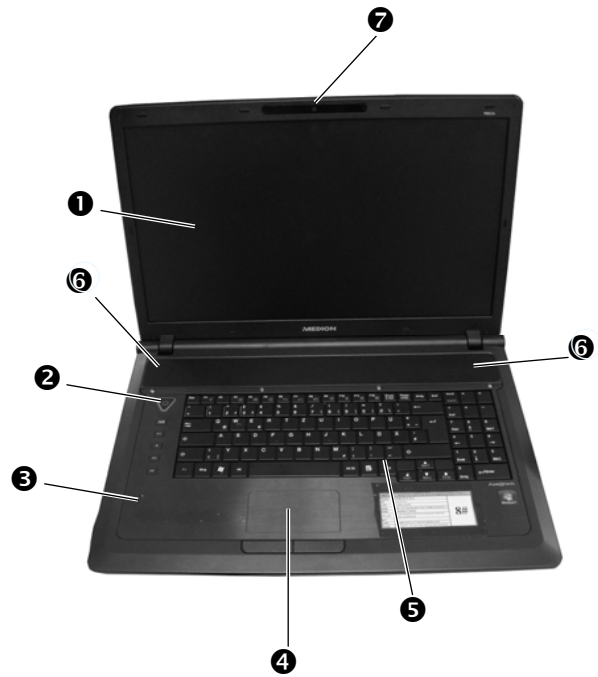


❶ HDD

❷ CPU & DDR3 SO-DIMM & Mini Express Card

❸ Battery Park

2.1.5 Top-open View



❶ LCD Screen

❷ Power Button

❸ Internal MIC

❹ Touch Pad

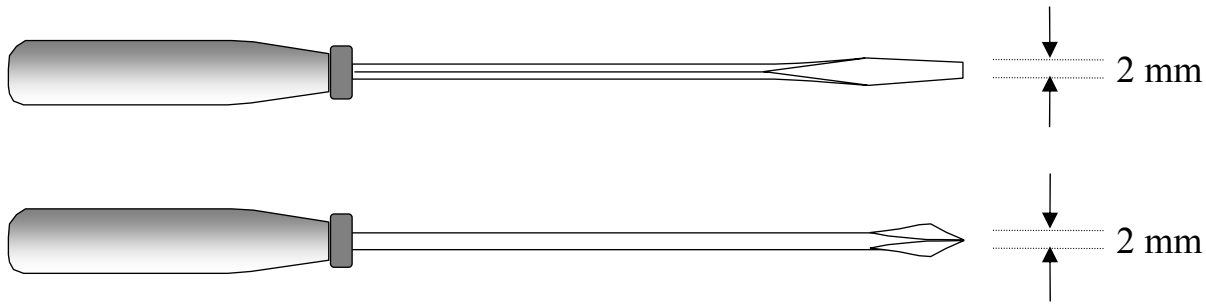
❺ Keyboard

❻ Speaker

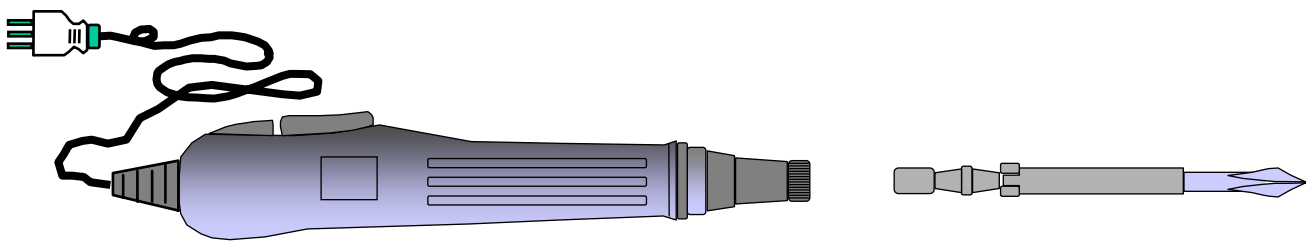
❼ Web Camera

2.2 Tools Introduction

1. Minus screw driver for notebook assembly & disassembly.



2. Auto screw driver for notebook assembly & disassembly.



Bit Size

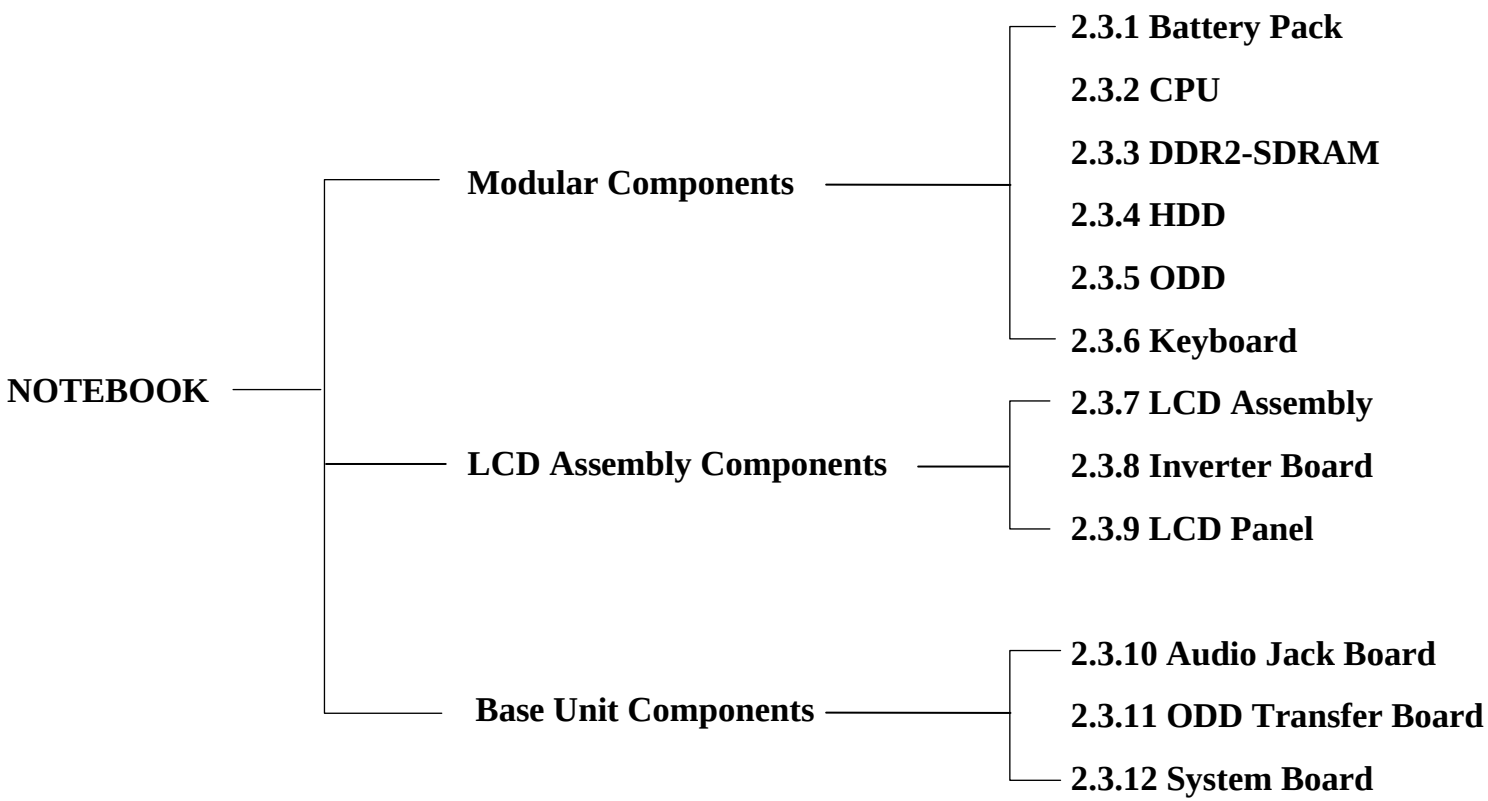
#0

Screw Size	Tooling	Tor.	Bit Size
1. M2.0	Auto-Screw driver	2.0-2.5 kg/cm^2	#0

2.3 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations.Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



2.3.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide two release lever outwards to the “unlock” ( ) position (❶), while take the battery pack out of the compartment (❷). (Figure 2-1)

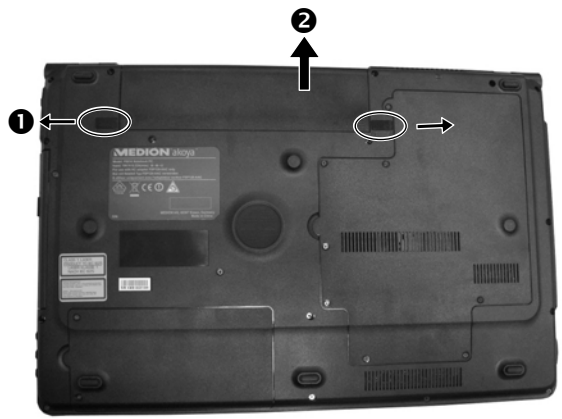


Figure 2-1 Remove the battery pack

Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the “lock” ( ) position.

2.3.2 CPU

Disassembly

1. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove eight screws fastening the CPU cover. (Figure 2-2)
3. Remove six spring screws that secure the heatsink upon the CPU and remove three screws fastening the fan, then disconnect the fan's power cord from system board. (Figure 2-3)

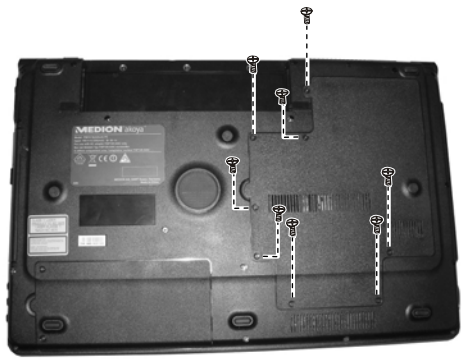


Figure 2-2 Remove eight screws

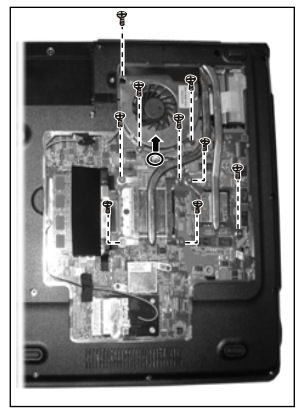


Figure 2-3 Free the heatsink

4. To remove the existing CPU, loosen the screw by a flat screwdriver,upraise the CPU socket to unlock the CPU. (Figure 2-4)

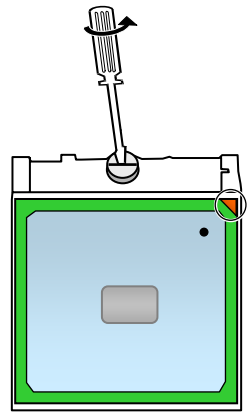


Figure 2-4 Remove the CPU

Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Tighten the screw by a flat screwdriver to locking the CPU.
2. Connect the fan's power cord to the system board, fit the fan and heatsink upon the CPU and secure with nine screws.
3. Replace the CPU cover and secure with eight screws.
4. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.3 DDR3-SDRAM

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (See section 2.3.1 Disassembly)
2. Remove eight screws fastening the CPU cover. (Refer to step 2 of section 2.3.2 Disassembly)

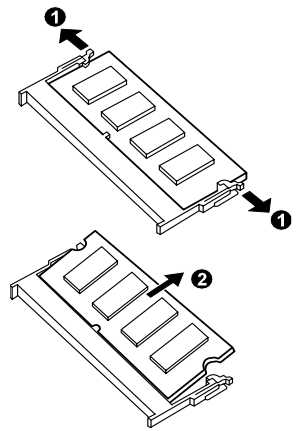


Figure 2-5 Remove the SO-DIMM

3. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-5)

Reassembly

1. To install the DDR3, match the DDR3's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the DDR3 into position.
2. Replace the CPU cover and secure with eight screws. (Refer to step 3 of section 2.3.3 Reassembly)
3. Replace the battery pack. (See section 2.3.1 Reassembly)

2.3.4 HDD

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack and . (Refer to section 2.3.1 Disassembly)
2. Remove two screws fastening the HDD cover. (Figure 2-6)
3. Lift the HDD module out and disconnect the HDD connector. (Figure 2-7)

Figure 2-6 Remove HDD cover

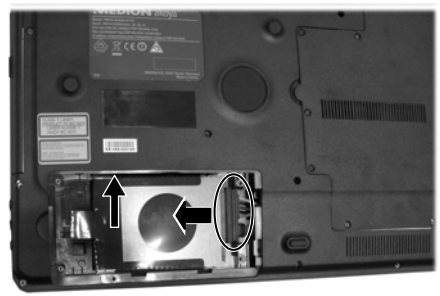


Figure 2-7 Remove HDD module

Reassembly

1. Reconnect the HDD connector and replace the HDD module to the HDD shielding.
2. Replace the HDD compartment cover and secure with two screws.
3. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.5 ODD

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove one screw fastening the ODD. (Figure 2-9)
3. Insert a small rod, such as a straightened paper clip, into ODD's manual eject hole (❶) and push firmly to release the tray. Then gently pull out the ODD by holding the tray that pops out (❷). (Figure 2-9)

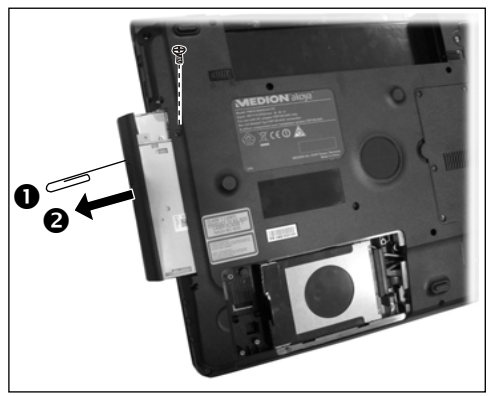


Figure 2-9 Remove the ODD

Reassembly

1. Push the ODD into the compartment and secure with one screw.
2. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.6 Keyboard

Disassembly

1. Remove the battery pack. (Refer to section 2.3.1 Disassembly)
2. Remove four screws fastening the keyboard cover, then remove the keyboard cover. (figure 2-10)
3. Remove three screws fastening the keyboard. (Figure 2-11)

Figure 2-10 Remove the keyboard cover

Figure 2-11 Remove four screws

4. Slightly turn over the keyboard and disconnect the cable from the system board to detach the keyboard. (Figure 2-12)

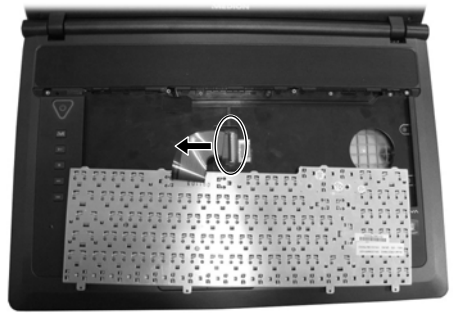


Figure 2-12 Remove the keyboard

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place, then secure the keyboard with three screws..
2. Replace the keyboard cover and secure with four screws.
3. Replace the battery pack. (Refer to section 2.3.1 Reassembly)

2.3.7 LCD ASSY

Disassembly

1. Remove the battery pack, CPU, DDR3, HDD, ODD and keyboard. (See sections 2.3.1~2.3.6 Disassembly)
2. Remove twenty-seven screws and disconnect one cable. (Figure 2-13)
3. Turn over the unit, remove nine screws and disconnect the touch pad cable, then remove the top cover. (Figure 2-14)

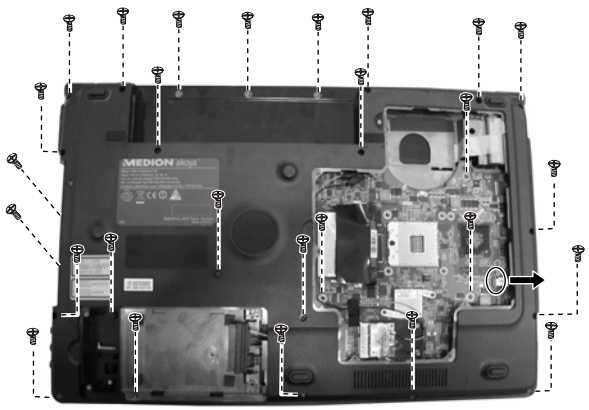


Figure 2-13 Remove twenty-seven screws and disconnect one cable

Figure 2-14 Remove the top cover

4. Remove nine screws and carefully pull the antenna wire and two cables out. Then free the LCD assembly. (Figure 2-15)

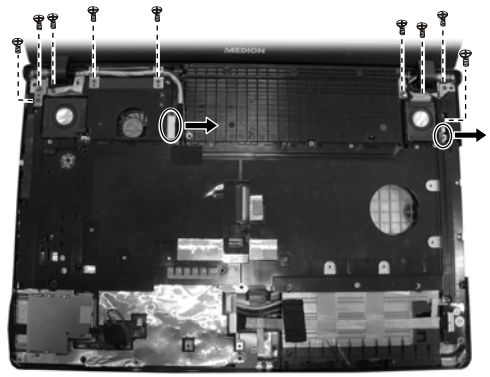


Figure 2-15 Free the LCD assembly

Reassembly

1. Attach the LCD assembly to the base unit and secure with nine screws. Reconnect the antenna wires and two cables.
2. Reconnect the antenna wires and two cables.
3. Replace the top cover and reconnect the touchpad cable, secure with nine screws.
4. Turn over the unit, reconnect one cable and secure with twenty-seven screws.
3. Replace the keyboard, ODD, HDD, DDR3, CPU and battery pack. (Refer to sections 2.3.6~2.3.1 Reassembly)

2.3.8 Inverter Board

Disassembly

1. Remove the LCD assembly. (Refer to section 2.3.7 Disassembly)
2. Remove six screws fastening the LCD cover. (Figure 2-16)
3. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the frame out. Repeat the process as figure 1-20 arrowhead hints until the cover is completely separated from the housing.
4. Remove nine screws, then separate panel from LCD housing. (Figure 2-17)

Figure 2-16 Remove LCD cover

Figure 2-17 Remove nine screws

5. Disconnect two cables, then remove the inverter board. (Figure 2-18)

Figure 2-18 Remove the inverter board

Reassembly

1. Replace the inverter board and reconnect two cables.
2. Replace the LCD panel and inverter board into the LCD housing, then secure with nine screws.
3. Fit the LCD cover and secure with six screws.
4. Replace the LCD assembly. (See sections 2.3.7 Reassembly)

2.3.9 LCD Panel

Disassembly

1. Remove the LCD assembly and inverter board. (Refer to section 2.3.7 and 2.3.8 Disassembly)
2. Remove eight screws that secure the LCD brackets. (Figure 2-19)
3. Disconnect LCD cable to free the panel. (Figure 2-20)

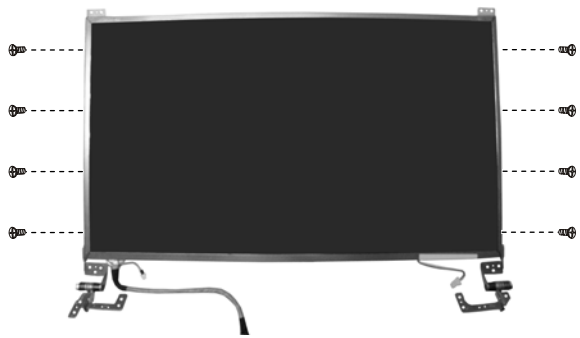


Figure 2-19 Remove eight screws

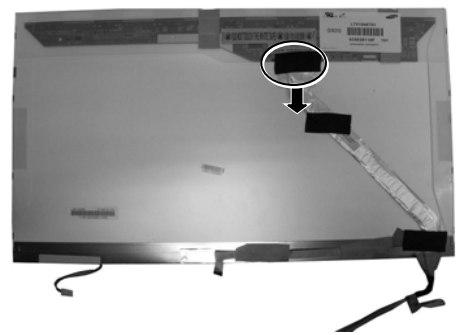


Figure 2-20 Free the LCD panel

Reassembly

1. Replace the cable to the LCD panel.
2. Attach the LCD panel's brackets back to LCD panel and secure with eight screws.
3. Replace the inverter board and LCD assembly. (See sections 2.3.8 and 2.3.7 Reassembly)

2.3.10 Audio Jack Board

Disassembly

1. Remove the LCD assembly. (Refer to sections 2.3.7 Disassembly)
2. Remove six screws fastening the shielding. Then remove the shielding. (Figure 2-21)
3. Remove one screw and disconnect two cables, then remove the audio jack board. (Figure 2-22)

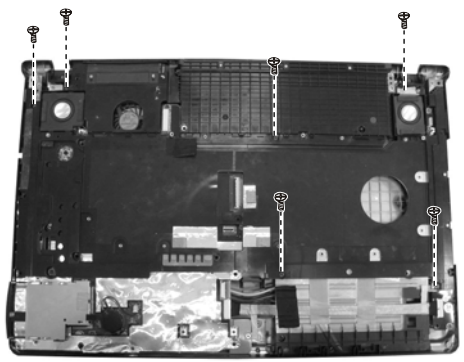


Figure 2-21 Remove the shielding

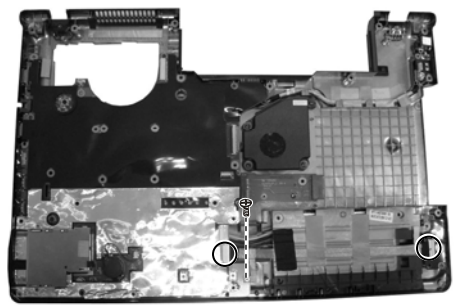


Figure 2-22 Remove the audio jack board

Reassembly

1. Replace the audio jack board and reconnect two cables, then secure with one screw.
2. Replace the shielding and secure with six screws.
3. Replace the LCD assembly. (See sections 2.3.7 Reassembly)

2.3.11 ODD Transfer Board

Disassembly

1. Remove the LCD assembly. (Refer to sections 2.3.7 Disassembly)
2. Remove the shielding. (See step 2 of section 2.3.10 Disassembly)
3. Remove one screw fastening the ODD transfer board, the remove it flatly. (Figure 2-23)

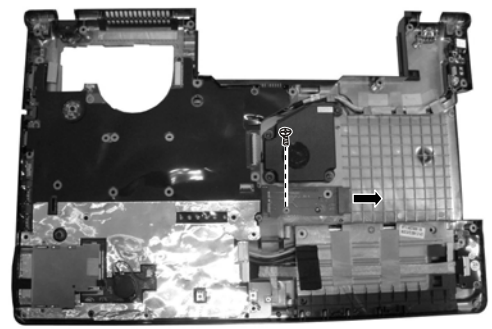


Figure 2-23 Remove the ODD transfer board

Reassembly

1. Replace the ODD transfer board flatly and secure with one screw.
2. Replace the shielding. (See step 2 of section 2.3.10 Reassembly)
3. Replace the LCD assembly. (See sections 2.3.7 Reassembly)

2.3.12 System Board

Disassembly

1. Remove the LCD assembly, audio jack board and ODD transfer board. (Refer to sections 2.3.7, 2.3.10&2.3.11 Disassembly)
2. Remove three screws fastening the system board. (Figure 2-24)
3. Remove two screws fastening the HDD cable and disconnect two cables, the free the system board. (Figure 2-25)

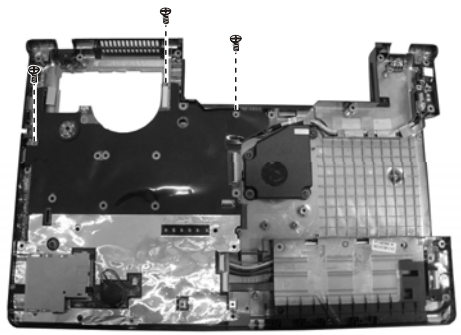


Figure 2-24 Remove five screws

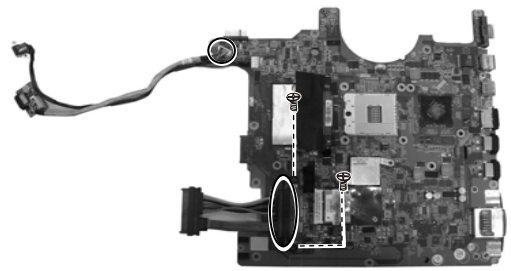


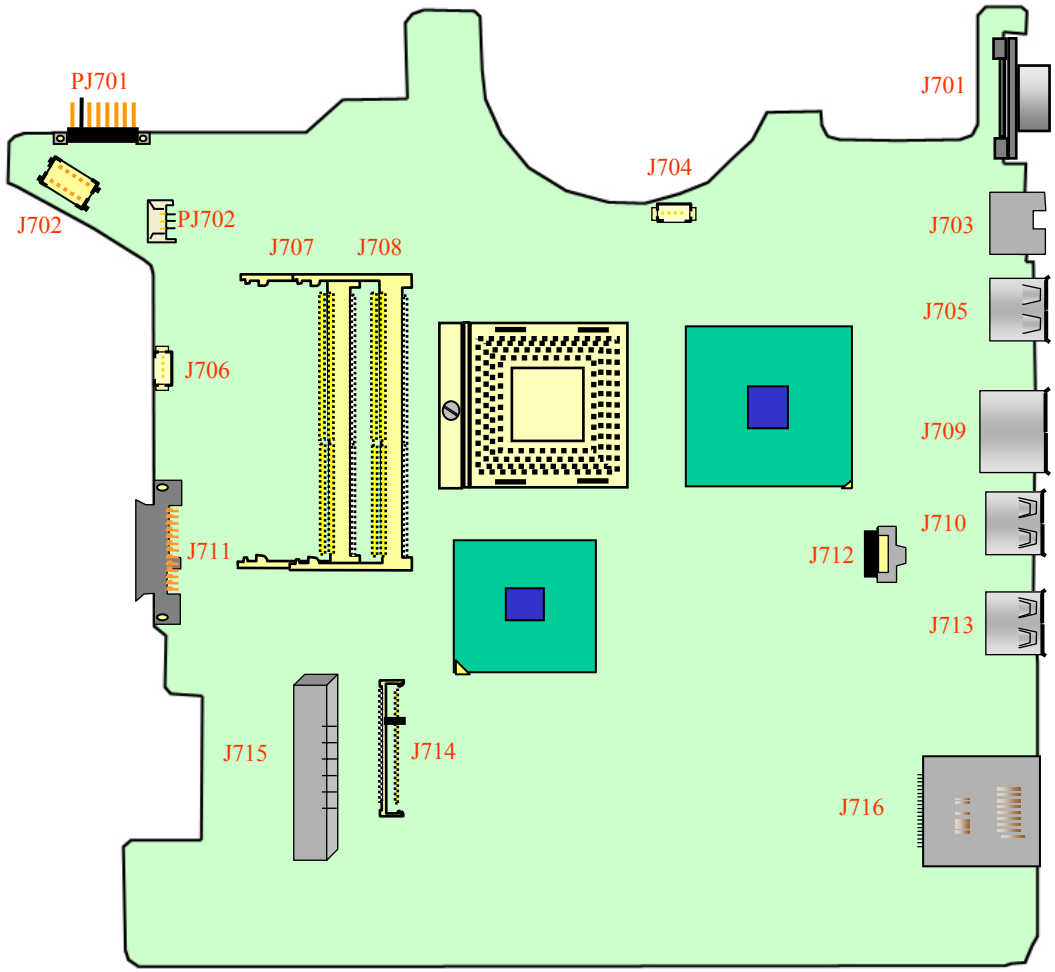
Figure 2-25 Free the system board

Reassembly

1. Replace the system board and reconnect two cables, then secure the HDD cable with two screws.
2. Replace the system board into the housing and secure with three screws.
3. Replace the ODD transfer board, audio jack board and LCD assembly. (See sections 2.3.11, 2.3.10&2.3.7 Reassembly)

3. Definition & Location of Major Components

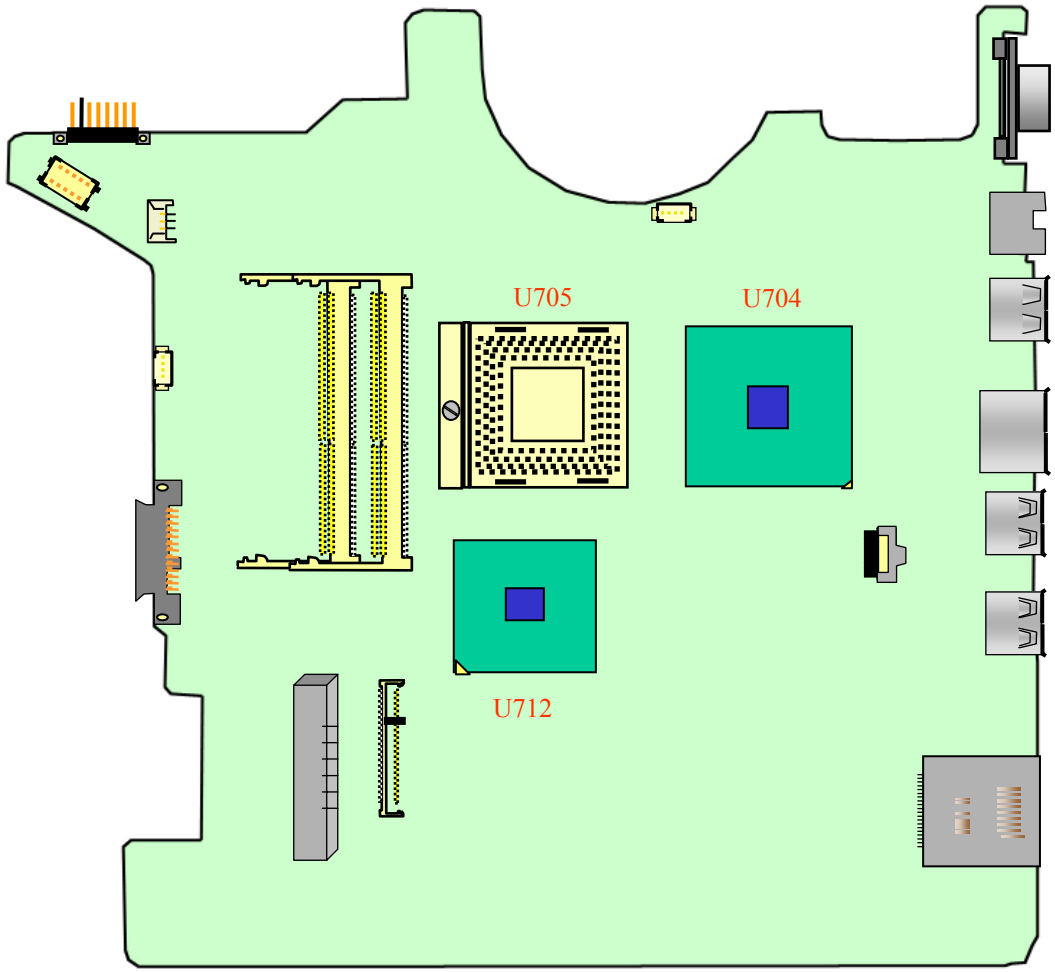
3.1 Mother Board (Side A) -1



- PJ701: Battery Connector
- PJ702: Power Jack Connector
- J701: External VGA Connector
- J702: Mother Board to USB Board Connector
- J703: RJ45 Connector
- J704: CPU Fan Connector
- J705: HDMI Connector
- J706: Internal Subwoofer Connector
- J707, J708 : DDR3 Sockets
- J709: E-SATA+USB Connector
- J710, J713: USB Ports
- J711: SATA ODD Connector
- J712: MMB Board Connector
- J714: MINI Wireless LAN Socket
- J715: SATA HDD Connector
- J716: Cardreader Connector

3. Definition & Location of Major Components

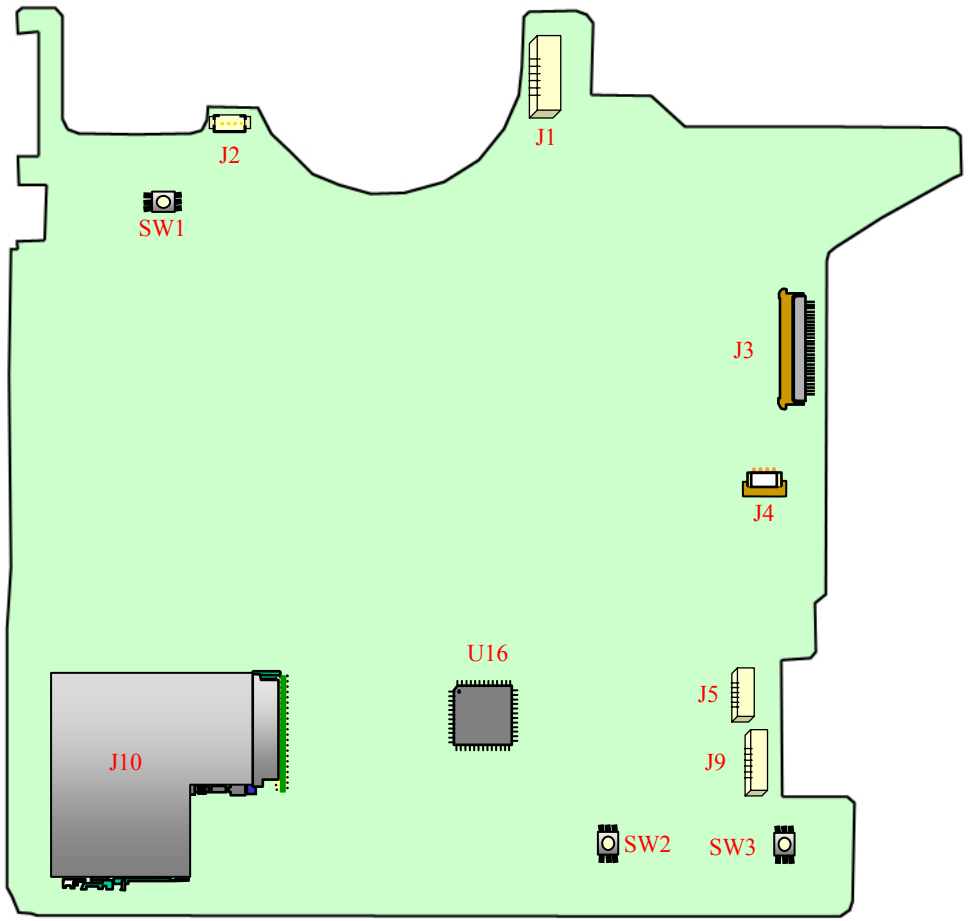
3.1 Mother Board (Side A) -2



- **U704: NVIDIA M96-PRO+**
- **U705: Intel Arrandle CPU Socket**
- **U712: IBEX PEAK-M PM55**

3. Definition & Location of Connectors/Switches

3.1 Mother Board (Side B)



- **J1: LCD Cable Connector**
- **J2: Internal Speaker Connector**
- **J3: Internal Keyboard Connector**
- **J4: Internal Touch-pad Connector**
- **J5: Bluetooth Board Connector**
- **J9: Audio Board Connector**
- **J10: Express Card Slot**

- **SW1: Power Button**
- **SW2: Touch-pad Left Button**
- **SW3: Touch-pad Right Button**

- **U16: KBC IT8502J**

4. Pin Descriptions of Ibex Peak-M

4.1 Digital Media Interface Signals

Name	Type	Description
DMI0TXP, DMI0TXN	O	**Digital Media Interface Differential Transmit Pair 0**
DMI0RXP, DMI0RXN	I	**Digital Media Interface Differential Receive Pair 0**
DMI0RXP, DMI1RXN	O	**Digital Media Interface Differential Transmit Pair 1**
DMI0RXP, DMI2RXN	I	**Digital Media Interface Differential Receive Pair 1**
DMI0RXP, DMI3RXN	O	**Digital Media Interface Differential Transmit Pair 2**
DMI0RXP, DMI4RXN	I	**Digital Media Interface Differential Receive Pair 2**
DMI0RXP, DMI5RXN	O	**Digital Media Interface Differential Transmit Pair 3**
DMI0RXP, DMI6RXN	I	**Digital Media Interface Differential Receive Pair 3**
DMI0RXP, DMI7RXN	I	**Impedance Compensation Input:** Determines DMI input impedance.
DMI0RXP, DMI8RXN	O	**Impedance/Current Compensation Output:** Determines DMI output impedance and bias current.

4.2 PCI Express* Signals –Table 1

Name	Type	Description
PETp1, PETn1	O	**PCI Express* Differential Transmit Pair 1**
PERp1, PERn1	I	**PCI Express Differential Receive Pair 1**
PETp2, PETn2	O	**PCI Express Differential Transmit Pair 2**
PERp2, PERn2	I	**PCI Express Differential Receive Pair 2**
PETp3, PETn3	O	**PCI Express Differential Transmit Pair 3**
PERp3, PERn3	I	**PCI Express Differential Receive Pair 3**
PETp4, PETn4	O	**PCI Express Differential Transmit Pair 4**
PERp4, PERn4	I	**PCI Express Differential Receive Pair 4**

4.2 PCI Express* Signals –Table 2

Name	Type	Description
PETp5, PETn5	O	**PCI Express Differential Transmit Pair 5**
PERp5, PERn5	I	**PCI Express Differential Receive Pair 5**
PETp6, PETn6	O	**PCI Express Differential Transmit Pair 6**
PERp6, PERn6	I	**PCI Express Differential Receive Pair 6**
PERp6, PERn7	O	**PCI Express Differential Transmit Pair 7** NOTE: Port 7 may not be available in all Ibex Peak SKUs.
PERp6, PERn8	I	**PCI Express Differential Receive Pair 7** **NOTE:** Port 7 may not be available in all Ibex Peak SKUs.
PERp6, PERn9	O	**PCI Express Differential Transmit Pair 8** **NOTE:** Port 7 may not be available in all Ibex Peak SKUs.
PERp6, PERn10	I	**PCI Express Differential Receive Pair 8** **NOTE:** Port 7 may not be available in all Ibex Peak SKUs.

4.3 Firmware Hub Interface Signals

Name	Type	Description
FWH[3:0] / LAD[3:0]	I/O	**Firmware Hub Signals.** These signals are multiplexed with the LPC address signals.
FWH4 / LFRAME#	O	**Firmware Hub Signals.** This signal is multiplexed with the LPC LFRAME# signal.
INIT3_3V#	O	**Initialization 3.3 V:** INIT3_3V# is asserted by the Ibex Peak for 16 PCI clocks to reset the processor. This signal is intended for Firmware Hub.

4.4 PCI Interface Signals –Table 1

Name	Type	Description
AD[31:0]	I/O	**PCI Address/Data:** AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical address (32 bits). During subsequent clocks, AD[31:0] contain data. The Ibex Peakwill drive all 0s on AD[31:0] during the address phase of all PCI Special Cycles.
C/BE[3:0]#	I/O	**Bus Command and Byte Enables:** The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# define the Byte Enables. **C/BE[3:0]# Command Type** 0000b Interrupt Acknowledge 0001b Special Cycle 0010b I/O Read 0011b I/O Write 0110b Memory Read 0111b Memory Write 1010b Configuration Read 1011b Configuration Write 1100b Memory Read Multiple 1110b Memory Read Line 1111b Memory Write and Invalidate All command encodings not shown are reserved. The Ibex Peak does not decode reserved values, and therefore will not respond if a PCI master generates a cycle using one of the reserved values.

4.4 PCI Interface Signals –Table 2

Name	Type	Description
DEVSEL#	I/O	**Device Select:** The Ibex Peak asserts DEVSEL# to claim a PCI transaction. As an output, the Ibex Peak asserts DEVSEL# when a PCI master peripheral attempts an access to an internal Ibex Peak address or an address destined for DMI (main memory or graphics). As an input, DEVSEL# indicates the response to an Ibex Peak-initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PLTRST#. DEVSEL# remains tri-stated by the Ibex Peak until driven by a target device.
FRAME#	I/O	**Cycle Frame:** The current initiator drives FRAME# to indicate the beginning and duration of a PCI transaction. While the initiator asserts FRAME#, data transfers continue. When the initiator negates FRAME#, the transaction is in the final data phase. FRAME# is an input to the Ibex Peak when the Ibex Peak is the target, and FRAME# is an output from the Ibex Peak when the Ibex Peak is the initiator. FRAME# remains tri-stated by the Ibex Peak until driven by an initiator.

4.4 PCI Interface Signals –Table 3

Name	Type	Description
IRDY#	I/O	**Initiator Ready:** IRDY# indicates the Ibex Peak's ability, as an initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the Ibex Peak has valid data present on AD[31:0]. During a read, it indicates the Ibex Peak is prepared to latch data. IRDY# is an input to the Ibex Peak when the Ibex Peak is the target and an output from the Ibex Peak when the Ibex Peak is an initiator. IRDY# remains tri-stated by the Ibex Peak until driven by an initiator.
TRDY#	I/O	**Target Ready:** TRDY# indicates the Ibex Peak's ability as a target to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the Ibex Peak, as a target, has placed valid data on AD[31:0]. During a write, TRDY# indicates the Ibex Peak, as a target is prepared to latch data. TRDY# is an input to the Ibex Peak when the Ibex Peak is the initiator and an output from the Ibex Peak when the Ibex Peak is a target. TRDY# is tri-stated from the leading edge of PLTRST#. TRDY# remains tri-stated by the Ibex Peak until driven by a target.

4.4 PCI Interface Signals –Table 4

Name	Type	Description
STOP#	I/O	**Stop:** STOP# indicates that the Ibex Peak, as a target, is requesting the initiator to stop the current transaction. STOP# causes the Ibex Peak, as an initiator, to stop the current transaction. STOP# is an output when the Ibex Peak is a target and an input when the Ibex Peak is an initiator.
PAR	I/O	**Calculated/Checked Parity:** PAR uses “even” parity calculated on 36 bits, AD[31:0] plus C/BE[3:0]#. “Even” parity means that the Ibex Peak counts the number of ones within the 36 bits plus PAR and the sum is always even. The Ibex Peak always calculates PAR on 36 bits regardless of the valid byte enables. The Ibex Peak generates PAR for address and data phases and only guarantees PAR to be valid one PCI clock after the corresponding address or data phase. The Ibex Peak drives and tri-states PAR identically to the AD[31:0] lines except that the Ibex Peak delays PAR by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all Ibex Peak initiated transactions. PAR is an output during the data phase (delayed one clock) when the Ibex Peak is the initiator of a PCI write transaction, and when it is the target of a read transaction. Ibex Peak checks parity when it is the target of a PCI write transaction. If a parity error is detected, the Ibex Peak will set the appropriate internal status bits, and has the option to generate an NMI# or SMI#.

4.4 PCI Interface Signals –Table 5

Name	Type	Description
PERR#	I/O	**Parity Error:** An external PCI device drives PERR# when it receives data that has a parity error. The Ibex Peak drives PERR# when it detects a parity error. The Ibex Peak can either generate an NMI# or SMI# upon detecting a parity error (either detected internally or reported via the PERR# signal).
REQ0# **REQ1#/** GPIO50 **REQ2#/** GPIO52 **REQ3#/**GPIO54	I	**PCI Requests:** The Ibex Peak supports up to 4 masters on the PCI bus. REQ[3:1]# pins can instead be used as GPIO.
GNT0# **GNT1#/** GPIO51 **GNT2#/** GPIO53 **GNT3#/**GPIO55	O	**PCI Grants:** The Ibex Peak supports up to 4 masters on the PCI bus. GNT[3:1]# pins can instead be used as GPIO. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail. **NOTE:** GNT[3:0]# are sampled as a functional strap. See Section 4.30 for details.
CLKIN_PCILOO PBACK	I	**PCI Clock:** This is a 33 MHz clock feedback input to reduce skew between PCH PCI clock and clock observed by connected PCI devices. This signal must be connected to one of the pins in the group CLKOUT_PCI[4:0]

4.4 PCI Interface Signals –Table 6

Name	Type	Description
PCIRST#	O	**PCI Reset:** This is the Secondary PCI Bus reset signal. It is a logical OR of the primary interface PLTRST# signal and the state of the Secondary Bus Reset bit of the Bridge Control register (D30:F0:3Eh, bit 6).
PLOCK#	I/O	**PCI Lock:** This signal indicates an exclusive bus operation and may require multiple transactions to complete. Ibex Peak asserts PLOCK# when it performs non-exclusive transactions on the PCI bus. PLOCK# is ignored when PCI masters are granted the bus.
SERR#	I/OD	**System Error:** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the Ibex Peak has the ability to generate an NMI, SMI#, or interrupt.
PME#	I/OD	**PCI Power Management Event:** PCI peripherals drive PME# to wake the system from low-power states S1–S5. PME# assertion can also be enabled to generate an SCI from the S0 state. In some cases the Ibex Peak may drive PME# active due to an internal wake event. The Ibex Peak will not drive PME# high, but it will be pulled up to VccSus3_3 by an internal pull-up resistor.

4.5 Serial ATA Interface Signals–Table 1

Name	Type	Description
SATA0TXP **SATA0TXN**	O	**Serial ATA 0 Differential Transmit Pairs:** These are outbound high-speed differential signals to Port 0. In compatible mode, SATA Port 0 is the primary master of SATA Controller 1.
SATA0RXP **SATA0RXN**	I	**Serial ATA 0 Differential Receive Pair:** These are inbound high-speed differential signals from Port 0. In compatible mode, SATA Port 0 is the primary master of SATA Controller 1.
SATA1TXP **SATA1TXN**	O	**Serial ATA 1 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 1. In compatible mode, SATA Port 1 is the secondary master of SATA Controller 1.
SATA1RXP **SATA1RXN**	I	**Serial ATA 1 Differential Receive Pair:** These are inbound high-speed differential signals from Port 1. In compatible mode, SATA Port 1 is the secondary master of SATA Controller 1
SATA2TXP **SATA2TXN**	O	**Serial ATA 2 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 2. In compatible mode, SATA Port 2 is the primary slave of SATA Controller 1. NOTE: SATA Port 2 may not be available in all PCH SKUs.

4.5 Serial ATA Interface Signals–Table 2

Name	Type	Description
SATA2RXP **SATA2RXN**	I	**Serial ATA 2 Differential Receive Pair:** These are inbound high-speed differential signals from Port 2. In compatible mode, SATA Port 2 is the primary slave of SATA Controller 1 NOTE: SATA Port 2 may not be available in all PCH SKUs.
SATA3TXP **SATA3TXN**	O	**Serial ATA 3 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 3 In compatible mode, SATA Port 3 is the secondary slave of SATA Controller 1 NOTE: SATA Port 3 may not be available in all PCH SKUs.
SATA3RXP **SATA3RXN**	I	**Serial ATA 3 Differential Receive Pair:** These are inbound high-speed differential signals from Port 3 In compatible mode, SATA Port 3 is the secondary slave of SATA Controller 1 NOTE: SATA Port 3 may not be available in all PCH SKUs.
SATA4TXP **SATA4TXN**	O	**Serial ATA 4 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 4. In compatible mode, SATA Port 4 is the primary master of SATA Controller 2
SATA4RXP **SATA4RXN**	I	**Serial ATA 4 Differential Receive Pair:** These are inbound high-speed differential signals from Port 4. In compatible mode, SATA Port 4 is the primary master of SATA Controller 2

4.5 Serial ATA Interface Signals–Table 3

Name	Type	Description
SATA5TXP SATA5TXN	O	**Serial ATA 5 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 5. In compatible mode, SATA Port 5 is the secondary master of SATA Controller 2
SATA5RXP SATA5RXN	I	**Serial ATA 5 Differential Receive Pair:** These are inbound high-speed differential signals from Port 5. In compatible mode, SATA Port 5 is the secondary master of SATA Controller 2
SATAICOMPO	O	**Serial ATA Compensation Output:** Connected to the external precision (TBD) resistor to VccCore. Must be connected to SATAICOMPI on the board.
SATAICOMPI	I	**Serial ATA Compensation Input:** Connected to SATAICOMPO on the board.
SATA0GP / GPIO21	I	**Serial ATA 0 General Purpose:** This is an input pin which can be configured as an interlock switch corresponding to SATA Port 0. When used as an interlock switch status indication, this signal should be drive to ‘0’ to indicate that the switch is closed and to ‘1’ to indicate that the switch is open. If interlock switches are not required, this pin can be configured as GPIO21.
SATA1GP / GPIO19	I	**Serial ATA 1 General Purpose:** Same function as SATA0GP, except for SATA Port 1. If interlock switches are not required, this pin can be configured as GPIO19.
SATA2GP / GPIO36	I	**Serial ATA 2 General Purpose:** Same function as SATA0GP, except for SATA Port 2. If interlock switches are not required, this pin can be configured as GPIO36. NOTE: This signal can also be used as GPIO36.

4.5 Serial ATA Interface Signals–Table 4

Name	Type	Description
SATA3GP / GPIO37	I	**Serial ATA 3 General Purpose:** Same function as SATA0GP, except for SATA Port 3. If interlock switches are not required, this pin can be configured as GPIO37. NOTE: This signal can also be used as GPIO37.
SATA4GP / GPIO16	I	**Serial ATA 4 General Purpose:** Same function as SATA0GP, except for SATA Port 4.
SATA5GP / GPIO49	I	**Serial ATA 5 General Purpose:** Same function as SATA0GP, except for SATA Port 5.
SATALED#	OD O	**Serial ATA LED:** This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc3_3 is required.
SCLOCK/ GPIO22	OD O	**SGPIO Reference Clock:** The SATA controller uses rising edges of this clock to transmit serial data, and the target uses the falling edge of this clock to latch data. If SGPIO interface is not used, this signal can be used as a GPIO.
SLOAD/GPIO38	OD O	**SGPIO Load:** The controller drives a ‘1’ at the rising edge of SCLOCK to indicate either the start or end of a bit stream. A 4-bit vendor specific pattern will be transmitted right after the signal assertion. If SGPIO interface is not used, this signal can be used as a GPIO.
SDATAOUT0/ GPIO39 SDATAOUT1/ GPIO48	OD O	**SGPIO Dataout:** Driven by the controller to indicate the drive status in the following sequence: drive 0, 1, 2, 3, 4, 5, 0, 1, 2... If SGPIO interface is not used, the signals can be used as GPIO.

4.6 LPC Interface Signals

Name	Type	Description
LAD[3:0] / FWH[3:0]	I/O	**LPC Multiplexed Command, Address, Data:** For LAD[3:0], internal pull-ups are provided.
LFRAME# / FWH4	O	**LPC Frame:** LFRAME# indicates the start of an LPC cycle, or an abort.
LDRQ0#, LDRQ1# / GPIO23	I	**LPC Serial DMA/Master Request Inputs:** LDRQ[1:0]# are used to request DMA or bus master access. These signals are typically connected to an external Super I/O device. An internal pull-up resistor is provided on these signals. LDRQ1# may optionally be used as GPIO.

4.7 Interrupt Signals

Name	Type	Description
SERIRQ	I/OD	**Serial Interrupt Request:** This pin implements the serial interrupt protocol.
PIRQ[D:A]#	I/OD	**PCI Interrupt Requests:** In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQA# is connected to IRQ16, PIRQB# to IRQ17, PIRQC# to IRQ18, and PIRQD# to IRQ19. This frees the legacy interrupts.
PIRQ[H:E]# / GPIO[5:2]	I/OD	**PCI Interrupt Requests:** In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQE# is connected to IRQ20, PIRQF# to IRQ21, PIRQG# to IRQ22, and PIRQH# to IRQ23. This frees the legacy interrupts. If not needed for interrupts, these signals can be used as GPIO.

4.8 USB Interface Signals –Table 1

Name	Type	Description
USBP0P, USBP0N, USBP1P, USBP1N	I/O	**Universal Serial Bus Port [1:0] Differential:** These differential pairs are used to transmit Data/Address/Command signals for ports 0 and 1. These ports can be routed to UHCI controller #1 or the EHCI controller #1. **NOTE:** No external resistors are required on these signals. The Ibex Peak integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP2P, USBP2N, USBP3P, USBP3N	I/O	**Universal Serial Bus Port [3:2] Differential:** These differential pairs are used to transmit data/address/command signals for ports 2 and 3. These ports can be routed to UHCI controller #2 or the EHCI controller #1. **NOTE:** No external resistors are required on these signals. The Ibex Peak integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP4P, USBP4N, USBP5P, USBP5N	I/O	**Universal Serial Bus Port [5:4] Differential:** These differential pairs are used to transmit Data/Address/Command signals for ports 4 and 5. These ports can be routed to UHCI controller #3 or the EHCI controller #1. **NOTE:** No external resistors are required on these signals. The Ibex Peak integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.

4.8 USB Interface Signals –Table 2

Name	Type	Description
USBP6P, USBP6N, USBP7P, USBP7N	I/O	**Universal Serial Bus Port [7:6] Differential:** These differential pairs are used to transmit Data/Address/Command signals for ports 6 and 7. These ports can be routed to UHCI controller #4 or the EHCI controller #2. **NOTE:** No external resistors are required on these signals. The Ibex Peak integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP8P, USBP8N, USBP9P, USBP9N	I/O	**Universal Serial Bus Port [9:8] Differential:** These differential pairs are used to transmit Data/Address/Command signals for ports 8 and 9. These ports can be routed to UHCI controller #5 or the EHCI controller #2. **NOTE:** No external resistors are required on these signals. The Ibex Peak integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
USBP10P, USBP10N, USBP11P, USBP11N	I/O	**Universal Serial Bus Port [11:10] Differential:** These differential pairs are used to transmit Data/Address/Command signals for ports 10 and 11. These ports can be routed to UHCI controller #6 or the EHCI controller #2. **NOTE:** No external resistors are required on these signals. The Ibex Peak integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.

4.8 USB Interface Signals –Table 3

Name	Type	Description
USBP12P, USBP12N, USBP13P, USBP13N	I/O	**Universal Serial Bus Port [13:12] Differential:** These differential pairs are used to transmit Data/Address/Command signals for ports 13 and 12. These ports can be routed to UHCI controller #7 or the EHCI controller #2. **NOTE:** No external resistors are required on these signals. The Ibex Peak integrates 15 kΩ pull-downs and provides an output driver impedance of 45 Ω which requires no external series resistor.
OC0# / GPIO59 **OC1# /** GPIO40 **OC2# /** GPIO41 **OC3# /** GPIO42 **OC4# /** GPIO43 **OC5# /** GPIO9 **OC6# /** GPIO10 **OC7# /** GPIO14	I	**Overcurrent Indicators:** These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred. OC[7:0]# may optionally be used as GPIOs. **NOTES:** 1. OC# pins are not 5 V tolerant. 2. OC# pins must be shared between ports 3. OC#[3:0] can only be used for EHCI controller #1 4. OC#[4:7] can only be used for EHCI controller #2
USBRBIAS	O	**USB Resistor Bias:** Analog connection point for an external resistor. Used to set transmit currents and internal load resistors.
USBRBIAS#	I	**USB Resistor Bias Complement:** Analog connection point for an external resistor. Used to set transmit currents and internal load resistors.

4.9 Power Management Interface Signals –Table 1

Name	Type	Description
PLTRST#	O	**Platform Reset:** The Ibex Peak asserts PLTRST# to reset devices on the platform (e.g., SIO, FWH, LAN, Processor, etc.). The Ibex Peak asserts PLTRST# during power-up and when S/W initiates a hard reset sequence through the Reset Control register (I/O Register CF9h). The Ibex Peak drives PLTRST# inactive a minimum of 1 ms after both PWROK and VGATE are driven high. The Ibex Peak drives PLTRST# active a minimum of 1 ms when initiated through the Reset Control register (I/O Register CF9h). **NOTE:** PLTRST# is in the VccSus3_3 well.
THRMTRIP#	I	**Thermal Trip:** When low, this signal indicates that a thermal trip from the processor occurred, and the Ibex Peak will immediately transition to a S5 state. The Ibex Peak will not wait for the processor stop grant cycle since the processor has overheated.
SLP_S3#	O	**S3 Sleep Control:** SLP_S3# is for power plane control. This signal shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S4#	O	**S4 Sleep Control:** SLP_S4# is for power plane control. This signal shuts power to all non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state. **NOTE:** This pin must be used to control the DRAM power in order to use the Ibex Peak's DRAM power-cycling feature.

4.9 Power Management Interface Signals –Table 2

Name	Type	Description
SLP_S5# / GPIO63	O	**S5 Sleep Control:** SLP_S5# is for power plane control. This signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states. Pin may also be used as GPIO63
SLP_M#	O	**Manageability Sleep State Control:** This signal is used to control power planes to the Intel® AMT sub-system. If no Management Engine firmware is present, SLP_M# will have the same timings as SLP_S3#.
SLP_LAN# / GPIO29	O	**LAN Sub-System Sleep Control:** When SLP_LAN# is deasserted it indicates that the Hanksville PHY device must be powered. When SLP_LAN# is asserted power can be shut off to the Hanksville PHY device. SLP_LAN# will always be deasserted in S0 and anytime SLP_M# is deasserted. SLP_LAN# behavior in Sx/Moff can be configured by ME FW. If ME FW is not configuring SLP_LAN#, host can control the signal behavior by configuring GPIO29 as an output. If neither ME FW nor host BIOS configure the pin as an output, SLP_LAN# behavior will be based on the setting of the RTC backed SLP_LAN# Default Bit (D31:F0:A4h:bit 8). **NOTE:** The SLP_LAN# Default Value Bit will always determine SLP_LAN# behavior when in S4/S5/Moff after a G3, when in S5/Moff after a host partition reset with power down and when in S5/Moff due to an unconditional power down.

4.9 Power Management Interface Signals –Table 3

Name	Type	Description
PWROK	I	**Power OK:** When asserted, PWROK is an indication to the Ibex Peak that all of its core power rails have been stable for 10 ms. PWROK can be driven asynchronously. When PWROK is negated, the Ibex Peak asserts PLTRST#. **NOTE:** It is required that the power rails associated with PCI/PCIe typically the 3.3V, 5V, and 12V core well rails) have been valid for 99ms prior to PCH_PWROK assertion in order to comply with the 100ms PCI 2.3/PCIe 1.1 specification on PLTRST# deassertion. PWROK must not glitch, even if RSMRST# is low.
MEPWROK	I	**Management Engine Power OK:** When asserted, indicates that power to the ME subsystem is stable.
PWRBTN#	I	**Power Button:** The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S1-S4 states. This signal has an internal pull-up resistor and has an internal 16 ms de-bounce on the input.
RI#	I	**Ring Indicate:** This signal is an input from a modem. It can be enabled as a wake event, and this is preserved across power failures.

4.9 Power Management Interface Signals –Table 4

Name	Type	Description
SYS_RESET#	I	**System Reset:** This pin forces an internal reset after being debounced. The Ibex Peak will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms ± 2 ms for the SMBus to idle before forcing a reset on the system.
RSMRST#	I	**Resume Well Reset:** This signal is used for resetting the resume power plane logic. This signal must be asserted for at least 10 ms after the suspend power wells are valid. When deasserted, this signal is an indication that the suspend power wells are stable.
LAN_RST#	I	**LAN Reset:** When asserted, the internal LAN controller is in reset. This signal must remain asserted until at least 1 ms after the LAN power well (VccLAN) and ME power well (VccME3_3) are valid. Also, LAN_RST# must assert a minimum of 40 ns before the LAN power rails become inactive. When deasserted, this signal is an indication that LAN power wells are stable. Note: 1. If Intel LAN is enabled LAN_RST# must be connected to the same source as MEPWROK. 2. If Intel LAN is not used or disabled LAN_RST# must be grounded through an external pull-down resistor.
LAN_PHY_PWR_CTRL / GPIO12	O	**LAN PHY Power Control:** LAN_PHY_PWR_CTRL should be connected to LAN_DISABLE_N on the Hanksville PHY. Ibex Peak will drive LAN_PHY_PWR_CTRL low to put the PHY into a low power state when functionality is not needed. **NOTES:** LAN_PHY_PWR_CTRL can only be driven low if SLP_LAN# is deasserted. Signal can instead be used as GPIO12.

4.9 Power Management Interface Signals –Table 5

Name	Type	Description
WAKE#	I	**PCI Express* Wake Event:** Sideband wake signal on PCI Express asserted by components requesting wake up.
SUS_STAT# / GPIO61	O	**Suspend Status:** This signal is asserted by the Ibex Peak to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. Pin may also be used as GPIO61.
SUSCLK / GPIO62	O	**Suspend Clock:** This clock is an output of the RTC generator circuit to use by other chips for refresh clock. Pin may also be used as GPIO62.
DRAMPWROK	O	**DRAM Power OK:** This signal should connect to the Processor's SM_DRAMPWROK pin. The PCH asserts this pin to indicate when DRAM power is on. **NOTES:** 1. This pin should have External pull-up to the an always on Voltage level of 1.05 V / 1.1 V
PMSYNC#	O	**Power Management Sync:** Provides state information from the PCH to the Processor relevant to C-state transitions.
CLKRUN# / GPIO32 (Desktop Only)	I/O	**PCI Clock Run:** Used to support PCI CLKRUN protocol. Connects to peripherals that need to request clock restart or prevention of clock stopping.

4.9 Power Management Interface Signals –Table 6

Name	Type	Description
BATLOW# (Mobile Only) / GPIO72 (Desktop Only)	I	**Battery Low:** Mobile only signal is an input from the battery to indicate that there is insufficient power to boot the system. Assertion will prevent wake from S3–S5 state. This signal can also be enabled to cause an SMI# when asserted. **Note:** Desktop requires a weak external pull-up
SYS_PWROK	I	**System Power OK:** This generic power good input to the Ibex Peak is driven and utilized in a platform-specific manner. While PWROK always indicates that the CORE well of the Ibex Peak is stable, SYS_PWROK is used to inform the Ibex Peak that power is stable to some other system component(s) and the system is ready to start the exit from reset. The particular component(s) associated with SYS_PWROK can vary across platform types supported by the same generation of Ibex Peak. Depending on the platform, the Ibex Peak may expect (and wait) for SYS_PWROK at different stages of the boot flow before continuing. **NOTE:** Consult the platform design guide for instructions on how to connect SYS_PWROK for that platform.
STP_PCI# (Mobile Only) / **GPIO34** (Desktop Only)	O	**Stop PCI Clock:** This signal is an output to the external clock generator for it to turn off the PCI clock. Mobile: Can be configured as STP_PCI# Desktop: Hardware to GPIO mode.

4.10 Processor Interface Signals

Name	Type	Description
RCIN#	I	**Keyboard Controller Reset CPU:** The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the PCH's other sources of INIT#. When the PCH detects the assertion of this signal, INIT# is generated for 16 PCI clocks. **NOTE:** The PCH will ignore RCIN# assertion during transitions to the S3, S4, and S5 states.
A20GATE	I	**A20 Gate:** A20GATE is from the keyboard controller. The signal acts as an alternative method to force the A20M# signal active. It saves the external OR gate needed with various other copyists.
PROCPWRGD	O	**Processor Power Good:** This signal should be connected to the processor's VCCPWRGOOD_1 and VCCPWRGOOD_0 input to indicate when the processor power is valid.

4.1.11 SM Bus Interface Signals

Name	Type	Description
SMBDATA	I/OD	**SMBus Data:** External pull-up resistor is required.
SMBCLK	I/OD	**SMBus Clock:** External pull-up resistor is required.
SMBALERT# / GPIO11	I	**SMBus Alert:** This signal is used to wake the system or generate SMI#. This signal may be used as GPIO11

4.12 System Management Interface Signals

Name	Type	Description
INTRUDER#	I	**Intruder Detect:** This signal can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPI if the Intruder Detection is not needed.
SML0DATA	I/OD	**System Management Link 0 Data:** SMBus link to external PHY. External pull-up is required.
SML0CLK	I/OD	**System Management Link 0 Clock:** SMBus link to external PHY. External pull-up is required.
SML0ALERT# / GPIO60 /	O OD	**SMLink Alert 0:** Output of the integrated LAN controller to external PHY. External pull-up resistor is required. This signal can instead be used as a GPIO60.
SML1ALERT# / GPIO74	O OD	**SMLink Alert 1:** Alert for the ME SMBus controller to optional Embedded Controller or BMC. External pull-up resistor is required. This signal can instead be used as a GPIO74
SML1CLK / GPIO58	I/OD	**System Management Link 1 Clock:** SMBus link to optional Embedded Controller or BMC. External pull-up resistor is required.
SML1DATA / GP75	I/OD	**System Management Link 1 Data:** SMBus link to optional Embedded Controller or BMC. External pull-up resistor is required.

4.13 Real Time Clock Interface

Name	Type	Description
RTCX1	Special	**Crystal Input 1:** This signal is connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX1 can be driven with the desired clock rate.
RTCX2	Special	**Crystal Input 2:** This signal is connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX2 should be left floating.

4.14 Miscellaneous Signals

Name	Type	Description
INTVRMEN	I	**Internal Voltage Regulator Enable:** This signal enables the internal 1.05 V regulators. This signal must be always pulled-up to VccRTC.
SPKR	O	**Speaker:** The SPKR signal is the output of counter 2 and is internally "ANDed" with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon PLTRST#, its output state is 0. **NOTE:** SPKR is sampled as a functional strap. See Section 4.30 for more details. There is a weak integrated pull-down resistor on SPKR pin.
RTCRST#	I	**RTC Reset:** When asserted, this signal resets register bits in the RTC well. **NOTES:** 1. Unless CMOS is being cleared (only to be done in the G3 power state), the RTCRST# input must always be high when all other RTC power planes are on. 2. In the case where the RTC battery is dead or missing on the platform, the RTCRST# pin must rise before the RSMRST# pin.
SRTCRST#	I	**Secondary RTC Reset:** This signal resets the manageability register bits in the RTC well when the RTC battery is removed. **NOTES:** 1. The SRTCRST# input must always be high when all other RTC power planes are on. 2. In the case where the RTC battery is dead or missing on the platform, the SRTCRST# pin must rise before the RSMRST# pin.

4.15 Intel® High Definition Audio Link Signals –Table 1

Name	Type	Description
HDA_RST#	O	**Intel® High Definition Audio Reset:** Master hardware reset to external codec(s).
HDA_SYNC	O	**Intel High Definition Audio Sync:** 48 kHz fixed rate sample sync to the codec(s). Also used to encode the stream number. **NOTE:** This signal is sampled as a functional strap. See Section 4.30 for more details.There is a weak integrated pull-down resistor on this pin.
HDA_BCLK	O	**Intel High Definition Audio Bit Clock Output:** 24.000 MHz serial data clock generated by the Intel High Definition Audio controller (the Ibex Peak). This signal has a weak internal pull-down resistor.
HDA_SDO	O	**Intel High Definition Audio Serial Data Out:** Serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel High Definition Audio. **NOTE:** This signal is sampled as a functional strap. See Section 4.30 for more details.There is a weak integrated pull-down resistor on this pin.
HDA_SDIN [3:0]	I	**Intel High Definition Audio Serial Data In [3:0]:** Serial TDM data inputs from the codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel® High Definition Audio. These signals have integrated pull-down resistors, which are always enabled. **NOTE:** During enumeration, the Ibex Peak will drive this signal. During normal operation, the CODEC will drive it.

4.15 Intel® High Definition Audio Link Signals –Table 2

Name	Type	Description
HDA_DOCK_EN# /*GPIO33*	O	**High Definition Audio Dock Enable:** This signal controls the external Intel HD Audio docking isolation logic. This is an active low signal. When deasserted the external docking switch is in isolate mode. When asserted the external docking switch electrically connects the Intel HD Audio dock signals to the corresponding Ibex Peak signals. This signal can instead be used as GPIO33. **NOTE:** This signal is sampled as a functional strap. See Section 4.30for more details.
HDA_DOCK_RST# / GPIO13	O	**High Definition Audio Dock Reset:** This signal is a dedicated HDA_RST# signal for the codec(s) in the docking station. Aside from operating independently from the normal HDA_RST# signal, it otherwise works similarly to the HDA_RST# signal. This signal can instead be used as GPIO13.

4.16 Controller Link Signals

Name	Type	Description
CL_RST1# (Mobile Only) / TP20 (Desktop Only)	O	**Controller Link Reset 1:** Controller Link reset that connects to a Wireless LAN Device supporting Intel® Active Management Technology.
CL_CLK1 (Mobile Only) / TP18 (Desktop Only)	I/O	**Controller Link Clock 1:** bi-directional clock that connects to a Wireless LAN Device supporting Intel® Active Management Technology.
CL_DATA1 (Mobile Only) / TP19 (Desktop Only)	I/O	**Controller Link Data 1:** bi-directional data that connects to a Wireless LAN Device supporting Intel® Active Management Technology.

4.1.17 Serial Peripheral Interface (SPI) Signals

Name	Type	Description
SPI_CS0#	O	**SPI Chip Select 0:** Used as the SPI bus request signal.
SPI_CS1#	O	**SPI Chip Select 1:** Used as the SPI bus request signal.
SPI_MISO	I	**SPI Master IN Slave OUT:** Data input pin for Ibex Peak.
SPI_MOSI	O	**SPI Master OUT Slave IN:** Data output pin for Ibex Peak. **NOTE:** This signal is sampled as a functional strap. See Section 4.30 for more details.There is a weak integrated pull-down resistor on this pin.
SPI_CLK	O	**SPI Clock:** SPI clock signal, during idle the bus owner will drive the clock signal low. 17.86 MHz and 31.25.

4.18 Intel® Quiet System Technology Signals

Name	Type	Description
PWM[3:0] (Desktop Only) / TP[12:9] (Mobile Only)	OD O	**Fan Pulse Width Modulation Outputs:** Pulse Width Modulated duty cycle output signal that is used for Intel® Quiet System Technology. When controlling a 3-wire fan, this signal controls a power transistor that, in turn, controls power to the fan. When controlling a 4-wire fan, this signal is connected to the “ Control” signal on the fan. The polarity of this signal is programmable. The output default is low. These signals are 5V tolerant.
TACH0 (Desktop Only) / GPIO17 TACH1 (Desktop Only) / GPIO1 TACH2 (Desktop Only) / GPIO6 TACH3(Desktop Only) / GPIO7	I	**Fan Tachometer Inputs:** Tachometer pulse input signal that is used to measure fan speed. This signal is connected to the “ Sense” signal on the fan. Can instead be used as a GPIO.
SST	I/O	**Simple Serial Transport:** Single-wire, serial bus. Connect to SST compliant devices such as SST thermal sensors or voltage sensors.
PECI	I/O	**Platform Environment Control Interface:** Single-wire, serial bus. Connect to corresponding pin of the processor for accessing processor digital thermometer.

4.19 JTAG Signals

Name	Type	Description
JTAG_TCK	I/O	**Test Clock Input (TCK):** The test clock input provides the clock for the JTAG test logic.
JTAG_TMS	I/O	**Test Mode Select (TMS):** The signal is decoded by the Test Access Port (TAP) controller to control test operations.
JTAG_TDI	I/O	**Test Data Input (TDI):** Serial test instructions and data are received by the test logic at TDI.
JTAG_TDO	I/O	**Test Data Output (TDO):** TDO is the serial output for test instructions and data from the test logic defined in this standard.
TRST#	I/O	**Test Reset (RST):** RST is an active low asynchronous signal that can reset the Test Access Port (TAP) controller. **Note:** The RST signal is optional per the IEEE 1149.1 specification, and is not functional for Boundary Scan Testing

NOTE: JTAG Pin definitions are from IEEE Standard Test Access Port and Boundary-Scan Architecture (IEEE Std. 1149.1-2001)

4.20 Dual Channel NAND Interface –Table 1

Name	Type	Description
NV_DQ[15:0] / NV_IO[15:0]	I/O	**Data Input/Output:** The bidirectional I/O used to transfer command, address and data to and from NAND device. Data is output during write operations and input during read operations. Source sychronous mode: NV_DQ - default mode of operation Asynchronous mode: NV_IO - only supported to identify flash at power on as per ONFI* 2.0 standard.
NV_DQS[1:0]	I/O	**Data Strobe[1:0]:** The data strobe signal indicates the data valid window for source synchronous mode. During read operations, NAND controller latches input data from NV_IO on the rising and falling edges of NV_DQS. During write operations, NAND controller outputs data on NV_DQ, edge-aligned to the rising and falling edges of NV_DQS. NV_DQS[0] is the data strobe for the lower data byte NV_DQ[7:0]. NV_DQS[1] is the data strobe for the upper data byte NV_DQ[15:8]. **NOTE:** These signals are unused in asynchronous mode.
NV_CE#[3:0]	O	**Chip Enable [3:0]#:**Selects one or more logical units (LUN) on the NAND device.
NV_CLE	O	**Command Latch Enable:** Indicates command is driven valid by NAND controller on the NV_DQ / NV_IO bus.
NV_ALE	O	**Address Latch Enable:** Indicates address is driven valid by IBX NAND controller on the NV_DQ / NV_IO bus.

4.20 Dual Channel NAND Interface –Table 2

Name	Type	Description
NV_WR#[1:0] /NV_RE#[1:0]	O	**Source Synchronous Mode:** **Write Read[1:0]# Indicates owner of the NV_DQ / NV_IO and NV_DQS signals.** '1', NV_DQ / NV_IO and NV_DQS are driven by IBX NAND Controller. '0', NV_DQ / NV_IO and NV_DQS are driven by the NAND device. **Asynchronous Mode:** **Read Enable [1:0]#:**Controls when NAND device will drive input data on the NV_IO bus during read operations
NV_CK[1:0]/ NV_WE[1:0]#	O	**Clock or Write Enable #:** **Source Synchronous Interface:** Provides the clock for the source synchronous interface. The clock is free-running when any Chip Enable NV_CE[3:0]# is asserted. **Asynchronous Interface:** Write Enable #: The active low signal indicates command, address or data are driven valid by the PCH NAND controller on the NV_IO bus.
NV_RB#	I	**Ready/Busy #:** Indicates the status of the NAND device. Ready/ Busy# signals from multiple NAND devices must be wired-OR together to provide a single Ready/Busy# input to NAND controller.
NV_RCOMP	I/O	**NAND Buffer Impedance Compensation:** This pin is connected to an external precision resistor (TBD) for impedance compensation of the NAND buffer drivers.

NOTE: Asynchronous Mode is included only for compliance to ONFi* 2.0. The Ibex Peak DC NAND I/F solutions will only support in source synchronous mode.

4.21 Clock Interface Signals –Table 1

Name	Type	Description
CLKIN_BCLK_P, CLKIN_BCLK_N	I	133 MHz differential reference clock from a clock chip in Buffer-Through Mode. Unused when Integrated Clock Generation is enabled.
CLKOUT_BCLK0_P / CLKOUT_PCIE8_P, CLKOUT_BCLK0_N / CLKOUT_PCIE8_N	O	133MHz Differential output to Processor or 100 MHz PCIe* Gen 1.1 specification differential output to PCI Express devices.
CLKOUT_DP_P / CLKOUT_BCLK1_P, CLKOUT_DP_N / CLKOUT_BCLK1_N	O	120 MHz Differential output for DisplayPort reference or 133MHz Differential output to Processor
CLKIN_DMI_P, CLKIN_DMI_N	I	100 MHz differential reference clock from a clock chip in Buffer-Through Mode. **Note:** This input clock is required to be PCIe 2.0 jitter spec compliant from a clock chip, for PCIe 2.0 discrete Graphics platforms.
CLKOUT_DMI_P, CLKOUT_DMI_N	O	100MHz Gen2 specification jitter tolerant differential output to processor.
CLKIN_SATA_P / CKSSCD_P, CLKIN_SATA_N / CKSSCD_N	I	100MHz differential reference clock from a clock chip, provided separately from CLKIN_DMI, for use only as a 100MHz source for SATA.

4.21 Clock Interface Signals –Table 2

Name	Type	Description
CLKIN_DOT96P, CLKIN_DOT96N	I	96MHz differential reference clock from a clock chip.
XTAL25_IN	I	Connection for 25MHz crystal to Ibex Peak oscillator circuit.
XTAL25_OUT	O	Connection for 25MHz crystal to Ibex Peak oscillator circuit.
REFCLK14IN	I	Single-ended 14.31818MHz reference clock driven by a clock chip.
CLKOUT_PEG_A_P, CLKOUT_PEG_A_N	O	100MHz Gen2 specification differential output to PCI-Express Graphics device
CLKOUT_PEG_B_P, CLKOUT_PEG_B_N	O	100MHz Gen2 specification differential output to a second PCI-Express Graphics device
PEG_A_CLKRQ# / GPIO47, PEG_B_CLKRQ# / GPIO56	I	Clock Request Signals for PEG SLOTS Can instead by used as GPIOs
CLKOUT_PCIE[7:0]P, CLKOUT_PCIE[7:0]N	O	100MHz PCIe* Gen1.1 specification differential output to PCI Express* devices

4.21 Clock Interface Signals –Table 3

Name	Type	Description
PCIECLKRQ0# / GPIO73, PCIECLKRQ1# / GPIO18, PCIECLKRQ2# / GPIO20, PCIECLKRQ3# / GPIO25, PCIECLKRQ4# / GPIO26, PCIECLKRQ5# / GPIO44, PCIECLKRQ6# / GPIO45, PCIECLKRQ7# / GPIO46	I	Clock Request Signals for PCI Express 100 MHz Clocks Can instead by used as GPIOs **NOTE:** External Pull-up Resistor required if used for CLKREQ# functionality
CLKOUT_PCI[4:0]	O	Single Ended 33.3MHz outputs to PCI connectors/devices. One of these signals must be connected to **CLKIN_PCILOOPBACK** to function as a PCI clock loopback. This allows skew control for variable lengths of **CLKOUT_PCI[4:0].**

4.21 Clock Interface Signals –Table 4

Name	Type	Description
CLKOUTFLEX0 / GPIO64	I/O	Configurable as a GPIO or as an Intel Management Firmware programmable output clock which can be configured as one of the following: -33 MHz -14.31818 MHz -DC Output logic ‘0’ - (Default) **NOTE:** Default clock setting requires no ME FW configuration.
CLKOUTFLEX1 / GPIO65	O	Configurable as a GPIO or as an Intel Management Firmware programmable output clock which can be configured as one of the following: Non functional and unsupported clock output value (Default) -33 MHz -14.31818 MHz output to SIO -DC Output logic ‘0’ **NOTE:** Default clock setting requires no ME FW configuration.
CLKOUTFLEX2 / GPIO66	O	Configurable as a GPIO or as an Intel Management Firmware programmable output clock which can be configured as one of the following: -33 MHz -14.31818 MHz (Default) -DC Output logic ‘0’ **NOTE:** Default clock setting requires no ME FW configuration.
CLKOUTFLEX3 / GPIO67	O	Configurable as a GPIO or as an Intel Management Firmware programmable output clock which can be configured as one of the following: -48 MHz (Default) -33 MHz -14.31818 MHz output to SIO -DC Output logic ‘0’ **NOTE:** Default clock setting requires no ME FW configuration.
XCLK_RCOMP	I/O	**Differential clock buffer Impedance Compensation:** Connected to an external precision resistor (90.9 ohms +/- 1%) to VccIO

4.22 LVDS Interface Signals –Table 1

Name	Type	Description
LVDSA_DATA [3:0]	O	LVDS Channel A differential data output - positive
LVDSA_DATA #[3:0]	O	LVDS Channel A differential data output -negative
LVDSA_CLK	O	LVDS Channel A differential clock output - positive
LVDSA_CLK#	O	LVDS Channel A differential clock output - negative
LVDSB_DATA [3:0]	O	LVDS Channel B differential data output - positive
LVDSB_DATA #[3:0]	O	LVDS Channel B differential data output -negative
LVDSB_CLK	O	LVDS Channel B differential clock output - positive
LVDSB_CLK#	O	LVDS Channel B differential clock output - negative
L_DDC_CLK	I/O	EDID support for flat panel display

4.22 LVDS Interface Signals –Table 2

Name	Type	Description
L_DDC_DATA	I/O	EDID support for flat panel display
L_CTRL_CLK	I/O	Control signal (clock) for external SSC clock chip control – optional
L_CTRL_DATA	I/O	Control signal (data) for external SSC clock chip control – optional
L_VDD_EN	I/O	**LVDS Panel Power Enable:** Panel power control enable control for LVDS. This signal is also called VDD_DBL in the CPIS specification and is used to control the VDC source to the panel logic.
L_BKLTEN	I/O	**LVDS Backlight Enable:** Panel backlight enable control for LVDS. This signal is also called ENA_BL in the CPIS specification and is used to gate power into the backlight circuitry.
L_BKLTCTL	I/O	**Panel Backlight Brightness Control:** Panel brightness control for LVDS. This signal is also called VARY_BL in the CPIS specification and is used as the PWM Clock input signal.

4.23 Analog Display Interface Signals

Name	Type	Description
CRT_RED	O A	**RED Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC.
CRT_GREEN	O A	**GREEN Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC.
CRT_BLUE	O A	**BLUE Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC.
DAC_IREF	I/O A	**Resistor Set:** Set point resistor for the internal color palette DAC. A 1 kohm 1% resistor is required between DAC_IREF and motherboard ground.
CRT_HSYNC	O HVCMOS	**CRT Horizontal Synchronization:** This signal is used as the horizontal sync (polarity is programmable) or “sync interval”. 2.5 V output
CRT_VSYNC	O HVCMOS	**CRT Vertical Synchronization:** This signal is used as the vertical sync (polarity is programmable). 2.5V output.
CRT_DDC_CLK	I/O COD	**Monitor Control Clock**
CRT_DDC_DATA	I/O COD	**Monitor Control Data**
CRT_IRTN	I/O COD	**Monitor Interrupt Return**

4.24 Intel Flexible Display Interface Signals

Name	Type	Description
FDI_RXP[3:0]	I	Display Link 1 positive data in
FDI_RXN[3:0]	I	Display Link 1 negative data in
FDI_FSYNC[0]	O	Display link 1 Frame sync
FDI_LSYNC[0]	O	Display link 1 Line sync
FDI_RXP[7:4]	I	Display Link 2 positive data in
FDI_RXN[7:4]	I	Display Link 2 negative data in
FDI_FSYNC[1]	O	Display link 2 Frame sync
FDI_LSYNC[1]	O	Display link 2 Line sync
FDI_INT	O	Used for Display interrupts from Ibex Peak to processor.

4.1.25 Misc HV Display Signals

Name	Type	Description
L_CLKCTLA	I/O	Can be used to control external clock chip for SSC - optional - SMBus clk signal
L_CLKCTLB	I/O	Can be used to control external clock chip for SSC - optional - SMBus data signal

4.26 Digital Display Interface Signals –Table 1

Name	Type	Description
DDPB_[3:0]P	O	**Port B: Capable of SDVO / HDMI / DVI / DisplayPort** SDVO DDPB_[0]P: red DDPB_[1]P: green DDPB_[2]P: blue DDPB_[3]P: clock **HDMI / DVI Port B Data and Clock Lines** DDPB_[0]P: TMDSB_DATA2 DDPB_[1]P: TMDSB_DATA1 DDPB_[2]P: TMDSB_DATA0 DDPB_[3]P: TMDSB_CLK **DisplayPort Port B** DDPB_[0]P: Display Port Lane 0 DDPB_[1]P: Display Port Lane 1 DDPB_[2]P: Display Port Lane 2 DDPB_[3]P: Display Port Lane 3

4.26 Digital Display Interface Signals –Table 2

Name	Type	Description
DDPB_[3:0]N	O	**Port B: Capable of SDVO / HDMI / DVI / DisplayPort SDVO** DDPB_[0]N: red complement DDPB_[1]N: green complement DDPB_[2]N: blue complement DDPB_[3]N: clock complement **HDMI / DVI Port B Data and Clock Line Complements** DDPB_[0]N: TMDSB_DATA2B DDPB_[1]N: TMDSB_DATA1B DDPB_[2]N: TMDSB_DATA0B DDPB_[3]N: TMDSB_CLKB DisplayPort **Port B** DDPB_[0]N: Display Port Lane 0 complement DDPB_[1]N: Display Port Lane 1 complement DDPB_[2]N: Display Port Lane 2 complement DDPB_[3]N: Display Port Lane 3 complement
DDPB_AUXP	I/O	**Port B:** Display Port Aux
DDPB_AUXN	I/O	**Port B:** Display Port Aux Complement
DDPB_HPD	I	**Port B:** TMDSB_HPD Hot Plug Detect
SDVO_CTRLCLK	I/O	**Port B:** HDMI Control Clock. Shared with port B SDVO
SDVO_CTRLDATA	I/O	**Port B:** HDMI Control Data. Shared with port B SDVO

4.26 Digital Display Interface Signals –Table 3

Name	Type	Description
SDVO_INTP	I	**SDVO_INTP:** Serial Digital Video Input Interrupt
SDVO_INTN	I	**SDVO_INTN:** Serial Digital Video Input Interrupt Complement.
SDVO_TVCLKINP	I	**SDVO_TVCLKINP:** Serial Digital Video TVOUT Synchronization Clock.
SDVO_TVCLKINN	I	**SDVO_TVCLKINN:** Serial Digital Video TVOUT Synchronization Clock Complement.
SDVO_STALLP	I	**SDVO_STALLP:** Serial Digital Video Field Stall.
SDVO_STALLN	I	**SDVO_STALLN:** Serial Digital Video Field Stall Complement.
DDPC_[3:0]P	O	**Port C: Capable of HDMI / DVI / DP** **HDMI / DVI Port C Data and Clock Lines** DDPC_[0]P: TMDSC_DATA2 DDPC_[1]P: TMDSC_DATA1 DDPC_[2]P: TMDSC_DATA0 DDPC_[3]P: TMDSC_CLK **DisplayPort Port C** DDPC_[0]P: Display Port Lane 0 DDPC_[1]P: Display Port Lane 1 DDPC_[2]P: Display Port Lane 2 DDPC_[3]P: Display Port Lane 3

4.26 Digital Display Interface Signals –Table 4

Name	Type	Description
DDPC_[3:0]N	O	**Port C: Capable of HDMI / DVI / DisplayPort** **HDMI / DVI Port C Data and Clock Line Complements** DDPC_[0]N: TMDSC_DATA2B DDPC_[1]N: TMDSC_DATA1B DDPC_[2]N: TMDSC_DATA0B DDPC_[3]N: TMDSC_CLKB **DisplayPort Port C Complements** DDPC_[0]N: Lane 0 complement DDPC_[1]N: Lane 1 complement DDPC_[2]N: Lane 2 complement DDPC_[3]N: Lane 3 complement
DDPC_AUXP	I/O	**Port C:** Display Port Aux
DDPC_AUXN	I/O	**Port C:** Display Port Aux Complement
DDPC_HPD	I	**Port C:** TMDSC_HPD Hot Plug Detect
DDPC_CTRLCLK	I/O	HDMI port C Control Clock
DDPC_CTRLDATA	I/O	HDMI port C Control Data

4.26 Digital Display Interface Signals –Table 5

Name	Type	Description
DDPD_[3:0]P	O	**Port D: Capable of HDMI / DVI / DP** **HDMI / DVI Port D Data and Clock Lines** DDPD_[0]P: TMDSC_DATA2 DDPD_[1]P: TMDSC_DATA1 DDPD_[2]P: TMDSC_DATA0 DDPD_[3]P: TMDSC_CLK **DisplayPort Port D** DDPD_[0]P: Display Port Lane 0 DDPD_[1]P: Display Port Lane 1 DDPD_[2]P: Display Port Lane 2 DDPD_[3]P: Display Port Lane 3
DDPD_[3:0]N	O	**Port D: Capable of HDMI / DVI / DisplayPort** **HDMI / DVI Port D Data and Clock Line Complements** DDPD_[0]N: TMDSC_DATA2B DDPD_[1]N: TMDSC_DATA1B DDPD_[2]N: TMDSC_DATA0B DDPD_[3]N: TMDSC_CLKB **DisplayPort Port D Complements** DDPD_[0]N: Lane 0 complement DDPD_[1]N: Lane 1 complement DDPD_[2]N: Lane 2 complement DDPD_[3]N: Lane 3 complement
DDPD_AUXP	I/O	**Port D:** Display Port Aux
DDPD_AUXN	I/O	**Port D:** Display Port Aux Complement
DDPD_HPD	I	**Port D:** TMDSD_HPD Hot Plug Detect
DDPD_CTRLCLK	I/O	HDMI port D Control Clock
DDPD_CTRLDATA	I/O	HDMI port D Control Data

4.27 General Purpose I/O Signals –Table 1

Note:
1. GPIO Configuration registers within the Core Well are reset whenever PWROK is deasserted.
2. GPIO Configuration registers within the Suspend Well are reset when RSMRST# is asserted, CF9h reset (06h or 0Eh) event occurs, or SYS_RST# is asserted.
3. GPIO24 is an exception to the other GPIO Signals in the Suspend Well and is not reset by CF9h reset (06h or 0Eh)

Name	Type	Tolerance	Power Well	Default	Blink Capability	Description
GPIO75	I/O	3.3 V	Suspend	Native	No	Multiplexed with SML1DATA (Note 12)
GPIO74	I/O	3.3 V	Suspend	Native	No	Multiplexed with SML1ALERT# (Note 12)
GPIO73	I/O	3.3 V	Suspend	Native	No	Multiplexed with PCIECLKRQ0#
GPIO72	I/O	3.3 V	Suspend	Native (Mobile Only)	No	Mobile: Multiplexed with BATLOW#. Desktop: Unmultiplexed (Note 4)
GPIO67	I/O	3.3 V	Core	Native	No	Multiplexed with CLKOUTFLEX3
GPIO66	I/O	3.3 V	Core	Native	No	Multiplexed with CLKOUTFLEX2
GPIO65	I/O	3.3 V	Core	Native	No	Multiplexed with CLKOUTFLEX1
GPIO64	I/O	3.3 V	Core	Native	No	Multiplexed with CLKOUTFLEX0
GPIO63	I/O	3.3 V	Suspend	Native	No	Multiplexed with SLP_S5#
GPIO62	I/O	3.3 V	Suspend	Native	No	Multiplexed with SUSCLK
GPIO61	I/O	3.3 V	Suspend	Native	No	Multiplexed with SUS_STAT#
GPIO60	I/O	3.3 V	Suspend	Native	No	Multiplexed with SML0ALERT#

4.27 General Purpose I/O Signals –Table 2

Name	Type	Tolerance	Power Well	Default	Blink Capability	Description
GPIO59	I/O	3.3 V	Suspend	Native	No	Multiplexed with OC[0]# (Note 12)
GPIO58	I/O	3.3 V	Suspend	Native	No	Multiplexed with SML1CLK
GPIO57	I/O	3.3 V	Suspend	GPI	No	Unmultiplexed
GPIO56	I/O	3.3 V	Suspend	Native	No	Multiplexed with PEG_B_CLKRQ#
GPIO55	I/O	3.3 V	Core	Native	No	Multiplexed with GNT3#
GPIO54	I/O	5.0 V	Core	Native	No	Multiplexed with REQ3#. (Note 12)
GPIO53	I/O	3.3 V	Core	Native	No	Multiplexed with GNT2#
GPIO52	I/O	5.0 V	Core	Native	No	Multiplexed with REQ2#. (Note 12)
GPIO51	I/O	3.3 V	Core	Native	No	Multiplexed with GNT1#
GPIO50	I/O	5.0 V	Core	Native	No	Multiplexed with REQ1#. (Note 12)
GPIO49	I/O	3.3V	Core	GPI	No	Multiplexed with SATA5GP
GPIO48	I/O	3.3 V	Core	GPI	No	Multiplexed with SDATAOUT1.
GPIO47	I/O	3.3V	Suspend	Native	No	Multiplexed with PEG_A_CLKRQ#
GPIO46	I/O	3.3V	Suspend	Native	No	Multiplexed with PCIECLKRQ7#
GPIO45	I/O	3.3V	Suspend	Native	No	Multiplexed with PCIECLKRQ6#
GPIO44	I/O	3.3V	Suspend	Native	No	Multiplexed with PCIECLKRQ5#
GPIO[43:40]	I/O	3.3 V	Suspend	Native	No	Multiplexed with OC[4:1]#. (Note 12)
GPIO39	I/O	3.3 V	Core	GPI	No	Multiplexed with SDATAOUT0.
GPIO38	I/O	3.3 V	Core	GPI	No	Multiplexed with SLOAD.
GPIO37	I/O	3.3 V	Core	GPI	No	Multiplexed with SATA3GP.
GPIO36	I/O	3.3 V	Core	GPI	No	Multiplexed with SATA2GP.

4.27 General Purpose I/O Signals –Table 3

Name	Type	Tolerance	Power Well	Default	Blink Capability	Description
GPIO35	I/O	3.3 V	Core	GPO	No	Unmultiplexed.
GPIO34	I/O	3.3 V	Core	GPI	No	Multiplexed with STP_PCI#
GPIO33	I/O	3.3 V	Core	GPO	No	Multiplexed with HDA_DOCK_EN# (Mobile Only) (Note 4)
GPIO32	I/O	3.3 V	Core	GPO, Native (Mobile only)	No	Unmultiplexed (Desktop Only) Mobile Only: Used as CLKRUN#, unavailable as GPIO (Note 4)
GPIO31	I/O	3.3 V	Suspend	GPI	Yes	Multiplexed with ACPRESENT (Note 7)
GPIO30	I/O	3.3 V	Suspend	GPI	Yes	Multiplexed with SUS_PWR_DN_ACK Desktop: Cannot be used for native function. Used as GPIO30 only. Mobile: Used as SUS_PWR_DN_ACK or GPIO30
GPIO29	I/O	3.3 V	Suspend	GPO	No	Multiplexed with SLP_LAN# (Note 11)
GPIO28	I/O	3.3 V	Suspend	GPI	Yes	Unmultiplexed
GPIO27	I/O	3.3 V	Suspend	GPO	Yes	Unmultiplexed
GPIO26	I/O	3.3 V	Suspend	Native	Yes	Multiplexed with PCIECLKRQ4#
GPIO25	I/O	3.3 V	Suspend	Native	Yes	Multiplexed with PCIECLKRQ3#
GPIO24	I/O	3.3 V	Suspend	GPO	Yes	Unmultiplexed NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.
GPIO23	I/O	3.3 V	Core	Native	Yes	Multiplexed with LDRQ1#.
GPIO22	I/O	3.3 V	Core	GPI	Yes	Multiplexed with SCLOCK
GPIO21	I/O	3.3 V	Core	GPI	Yes	Multiplexed with SATA0GP

4.27 General Purpose I/O Signals –Table 4

Name	Type	Tolerance	Power Well	Default	Blink Capability	Description
GPIO20	I/O	3.3 V	Core	Native	Yes	Multiplexed with PCIECLKRQ2#
GPIO19	I/O	3.3 V	Core	GPI	Yes	Multiplexed with SATA1GP
GPIO18	I/O	3.3 V	Core	Native	Yes (Note 6)	Multiplexed with PCIECLKRQ1#
GPIO17	I/O	3.3 V	Core	GPI	Yes	Multiplexed with TACH0. Mobile: Used as GPIO17 only.
GPIO16	I/O	3.3 V	Core	GPI	Yes	Multiplexed with SATA4GP.
GPIO15	I/O	3.3 V	Suspend	GPO	Yes	Unmultiplexed
GPIO14	I/O	3.3 V	Suspend	Native	Yes	Multiplexed with OC7#
GPIO13	I/O	3.3 V	Suspend	GPI	Yes	Multiplexed with HDA_DOCK_RST# (Mobile Only) (Note 4)
GPIO12	I/O	3.3 V	Suspend	GPI	Yes	Multiplexed with LAN_PHY_PWR_CTRL. GPIO / Native functionality controlled via soft strap (Note 9)
GPIO11	I/O	3.3 V	Suspend	Native	Yes	Multiplexed with SMBALERT#. (Note 12)
GPIO10	I/O	3.3 V	Suspend	Native	Yes	Multiplexed with OC6# (Note 12)
GPIO9	I/O	3.3 V	Suspend	Native	Yes	Multiplexed with OC5# (Note 12)
GPIO8	I/O	3.3 V	Suspend	GPO	Yes	Unmultiplexed
GPIO[7:6]	I/O	3.3 V	Core	GPI	Yes	Multiplexed with TACH[3:2]. Mobile: Used as GPIO[7:6] only.
GPIO[5:2]	I/OD	5 V	Core	GPI	Yes	Multiplexed with PIRQ[H:E]# (Note 5).
GPIO1	I/O	3.3 V	Core	GPI	Yes	Multiplexed with TACH1. Mobile: Used as GPIO1 only.
GPIO0	I/O	3.3 V	Core	GPI	Yes	Unmultiplexed

4.27 General Purpose I/O Signals

NOTES:

1. All GPIOs can be configured as either input or output.

2. GPI[15:0] can be configured to cause a SMI# or SCI. Note that a GPI can be routed to either an SMI# or an SCI, but not both.

3. Some GPIOs exist in the VccSus3_3 power plane. Care must be taken to make sure GPIO signals are not driven high into powered-down planes. Also, external devices should not be driving powered down GPIOs high. Some GPIOs may be connected to pins on devices that exist in the core well. If these GPIOs are outputs, there is a danger that a loss of core power (PWROK low) or a Power Button Override event will result in the Ibex Peak driving a pin to a logic 1 to another device that is powered down.

4. The functionality that is multiplexed with the GPIO may not be utilized in desktop configuration.

5. When this signal is configured as GPO the output stage is an open drain.

6. GPIO18’s blink capability defaults to enabled; therefore, it will toggle at a frequency of approximately 1 Hz when the Ibex Peak comes out of reset.

7. In a ME disabled system, GPIO31 may be used as ACPRESENT from the EC.

8. GPIO18 will toggle at a frequency of approximately 1 Hz when the Ibex Peak comes out of reset

4.27 General Purpose I/O Signals

NOTES:

9. For GPIOs where GPIO vs. Native Mode is configured via SPI Soft Strap, the corresponding GPIO_USE_SEL bits for these GPIOs have no effect. The GPIO_USE_SEL bits for these GPIOs may change to reflect the Soft-Strap configuration even though GPIO Lockdown Enable (GLE) bit is set.

10. This pins are used as Functional straps. See Section 4.30 for more detail

11. GPIO29 functionality is only enabled in Sx/Moff when ME FW has not configured the signal as SLP_LAN#. GPIO29 must never be used for any purpose other than in association with it muxed native SLP_LAN# functionality.

12. When the multiplexed GPIO is used as GPIO functionality, care should be taken to ensure the signal is stable in its inactive state of the native functionality, immediately after reset until it is initialized to GPIO functionality.

4.28 Manageability Signals -1

The following signals can be optionally utilized by Ibex Peak Management engine supported applications and appropriately configured by Management Engine firmware. When configured and utilized as a Manageability function, the associated host GPIO functionality is no longer available. If the Manageability function is not utilized in a platform, the signal can be used as a host General Purpose I/O or a native function.

Name	Type	Description
GPIO30/ **PROC_MISSING** (Desktop Only)	I	Used to indicate Processor Missing to Ibex Peak Management Engine.
GPIO24 / **FP_PWR_EN#** (Mobile Only)	O	Ibex Peak Management Engine drives signal to enable/disable power to the Finger-Print Sensor device.
SML0ALERT# / GPIO60 / **FP_INT** (Mobile Only)	I	Used by Finger-Print Sensor device to indicate an interrupt to the Ibex Peak Management Engine.
GPIO57/**TPM_PP**	I	Used to indicate TPM Physical Presence to the Management Engine, when pulled high.

4.28 Manageability Signals -2

Name	Type	Description
SATA5GP / GPIO49 / **TEMP_ALERT#**	O	Used as an alert (active low) to indicate to the external controller (e.g EC or SIO) that temperatures are out of range for the PCH or Graphics/Memory Controller or the Processor Core.
ACPRESENT / GPIO31 (Mobile Only)	I	Used in Mobile systems. Input signal from the Embedded Controller to indicate AC power source or the system battery. Active High indicates AC power. **Note:** This signal is required by Management Engine in M3 supporting platforms. Signal usage is optional otherwise.
SUS_PWR_DN_ACK / GPIO30 (Mobile Only)	O	Active High output signal asserted by the Intel ME to the Embedded Controller, when it does not require the PCH Suspend well to be powered. Note: This signal is required by Management Engine in all platforms.

NOTE: SLP_LAN#/GPIO29 may also be configured by ME FW in Sx/Moff. Please refer to SLP_LAN#/GPIO29 signal description for details.

4.29 Power and Ground Signals –Table 1

Name	Description
DcpRTC	**Decoupling:** This signal is for RTC decoupling only. This signal requires decoupling.
DcpSST	**Decoupling:** Internally generated 1.5V powered off of Suspend Well. This signal requires decoupling. Decoupling is required even if this feature is not used.
DcpSus	**Decoupling:** 1.05 V Suspend well supply that is supplied internally by Internal VRs. This signal requires decoupling.
DcpSusByp	**Decoupling:** This signal may require decoupling. Leave no connect if coupling is not required.
V5REF	Reference for 5 V tolerance on core well inputs. This power may be shut off in S3, S4, S5 or G3 states.
V5REF_Sus	Reference for 5 V tolerance on suspend well inputs. This power is not expected to be shut off unless the system is unplugged.
VccCore	1.05 V supply for core well logic. This power may be shut off in S3, S4, S5 or G3 states.
Vcc3_3	3.3 V supply for core well I/O buffers. This power may be shut off in S3, S4, S5 or G3 states.
VccME	1.05 V supply for the Intel Management Engine. This plane must be on in S0 and other times the Intel Management Engine is used.
VccME3_3	3.3V supply for the Intel Management Engine I/O and SPI I/O. This is a separate power plane that may or may not be powered in S3–S5 states. This plane must be on in S0 and other times the Intel Management Engine is used.

4.29 Power and Ground Signals –Table 1

Name	Description
DcpRTC	**Decoupling:** This signal is for RTC decoupling only. This signal requires decoupling.
DcpSST	**Decoupling:** Internally generated 1.5V powered off of Suspend Well. This signal requires decoupling. Decoupling is required even if this feature is not used.
DcpSus	**Decoupling:** 1.05 V Suspend well supply that is supplied internally by Internal VRs. This signal requires decoupling.
DcpSusByp	**Decoupling:** This signal may require decoupling. Leave no connect if coupling is not required.
V5REF	Reference for 5 V tolerance on core well inputs. This power may be shut off in S3, S4, S5 or G3 states.
V5REF_Sus	Reference for 5 V tolerance on suspend well inputs. This power is not expected to be shut off unless the system is unplugged.
VccCore	1.05 V supply for core well logic. This power may be shut off in S3, S4, S5 or G3 states.
Vcc3_3	3.3 V supply for core well I/O buffers. This power may be shut off in S3, S4, S5 or G3 states.
VccME	1.05 V supply for the Intel Management Engine. This plane must be on in S0 and other times the Intel Management Engine is used.
VccME3_3	3.3V supply for the Intel Management Engine I/O and SPI I/O. This is a separate power plane that may or may not be powered in S3–S5 states. This plane must be on in S0 and other times the Intel Management Engine is used.

4.29 Power and Ground Signals –Table 2

Name	Description
VccDMI	Power supply for DMI. 1.1 V or 1.05 V based on the processor used. Please refer to the respective processor documentation to find the appropriate voltage level.
VccLAN	1.05 V supply for LAN controller logic. This is a separate power plane that may or may not be powered in S3–S5 states. **NOTE:** VccLAN may be grounded if Intel LAN is disabled.
VccRTC	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well. This power is not expected to be shut off unless the RTC battery is removed or completely drained. **NOTE:** Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS in an Ibex Peak-based platform can be done by using a jumper on RTCRST# or GPI.
VccIO	1.05 V supply for core well I/O buffers. This power may be shut off in S3, S4, S5 or G3 states.
VccSus3_3	3.3 V supply for suspend well I/O buffers. This power is not expected to be shut off unless the system is unplugged.
VccSusHDA	Suspend supply for Intel® High Definition Audio. This pin can be either 1.5 or 3.3 V.
VccVRM	1.5V / 1.8 V supply for internal PLL and VRMs
VccpNAND	1.8 V supply for Dual Channel NAND interface. This power is supplied by core well. If unused, this pin can be left as no connect.

4.29 Power and Ground Signals –Table 3

Name	Description
VccADPLLA	1.05 V supply for Display PLL A Analog Power. This power is supplied by the core well.
VccADPLLB	1.05 V supply for Display PLL B Analog Power. This power is supplied by the core well.
VccADAC	3.3 V supply for Display DAC Analog Power. This power is supplied by the core well.
Vss	Grounds.
VSS_NCTF	**Non-Critical To Function.** These pins are for package mechanical reliability. **Note:** These pins should be connected to Ground.
Vcc3_3_NCTF	**Non-Critical To Function.** These pins are for package mechanical reliability. **Note:** These pins should be connected the same as the Vcc3_3 pins.
VccRTC_NCTF	**Non-Critical To Function.** These pins are for package mechanical reliability. **Note:** These pins should be connected the same as the VccRTC pins.
VccSUS3_3_N CTF	**Non-Critical To Function.** These pins are for package mechanical reliability. **Note:** These pins should be connected the same as the VccSUS3_3 pins.
V_CPU_IO_N CTF	**Non-Critical To Function.** These pins are for package mechanical reliability. **Note:** These pins should be connected the same as the V_CPU_IO pins.

4.29 Power and Ground Signals –Table 4

Name	Description
TP22_NCTF	**Non-Critical To Function.** These pins are for package mechanical reliability. **Note:** These pins should be connected to Ground.
VccAClk	1.05 V Analog power supply for internal clock PLL. This requires a filter and power is supplied by the core well. **NOTE:** This pin can be left as no connect in On-Die VR enabled mode (default).
VccSATAPLL	1.05 V Analog power supply for SATA. This signal is used for the analog power for SATA. This requires an LC filter and is supplied by the core well. Must be powered even if SATA is not used. **NOTE:** This pin can be left as no connect in On-Die VR enabled mode (default).
VccAPLLEXP	1.05 V Analog Power for DMI. This power is supplied by the core well. This requires an LC filter. NOTE: This pin can be left as no connect in On-Die VR enabled mode (default).
VccFDIPLL	1.05 V analog power supply for the FDI PLL. This power is supplied with core well. This requires an LC filter. **NOTE:** This pin can be left as no connect in On-Die VR enabled mode (default).
VccALVDS	3.3 V Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8 V I/O power supply for LVDS. (Mobile Only) This power is supplied by core well.
V_CPU_IO	Powered by the same supply as the processor I/O voltage. This supply is used to drive the processor interface signals. Please refer to the respective processor documentation to find the appropriate voltage level.

4.30 Functional Strap Definitions –Table 1

The following signals are used for static configuration. They are sampled at the rising edge of PWROK to select configurations (except as noted), and then revert later to their normal usage. To invoke the associated mode, the signal should be driven at least four PCI clocks prior to the time it is sampled.

Ibex Peak has implemented Soft Straps. Soft Straps are used to configure specific functions within the Ibex Peak and processor very early in the boot process before BIOS or SW intervention. When Descriptor Mode is enabled, the Ibex Peak will read Soft Strap data out of the SPI device prior to the de-assertion of reset to both the Management Engine and the Host system.

Name	Usage	When Sampled	Comment
SPKR	No Reboot	Rising edge of PWROK	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# de-asserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Ibex Peak will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers: Offset 3410h:bit 5).
INIT3_3V#	Reserved	Rising edge of PWROK	This signal has a weak internal pull up. **Note:** the internal pull-up is disabled after PLTRST# de-asserts. **NOTE:** This signal should not be pulled low

4.30 Functional Strap Definitions –Table 2

The following signals are used for static configuration. They are sampled at the rising edge of PWROK to select configurations (except as noted), and then revert later to their normal usage. To invoke the associated mode, the signal should be driven at least four PCI clocks prior to the time it is sampled.

Ibex Peak has implemented Soft Straps. Soft Straps are used to configure specific functions within the Ibex Peak and processor very early in the boot process before BIOS or SW intervention. When Descriptor Mode is enabled, the Ibex Peak will read Soft Strap data out of the SPI device prior to the de-assertion of reset to both the Management Engine and the Host system.

Name	Usage	When Sampled	Comment
SPKR	No Reboot	Rising edge of PWROK	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# de-asserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Ibex Peak will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers: Offset 3410h:bit 5).
INIT3_3V#	Reserved	Rising edge of PWROK	This signal has a weak internal pull up. **Note:** the internal pull-up is disabled after PLTRST# de-asserts. **NOTE:** This signal should not be pulled low

4.30 Functional Strap Definitions –Table 3

Name	Usage	When Sampled	Comment
GNT[3]#/ GPIO[55]	Top-Block Swap Override	Rising edge of PWROK	The signal has a weak internal pull-up. **Note: the internal pull-up is disabled after PCIRST# de-asserts.** If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode (Ibex Peak inverts A16 for all cycles targeting BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Config Registers:Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
INTVRMEN	Integrated 1.05 V VRM Enable / Disable	Always	Integrated 1.05 V VRMs is enabled when high **NOTE:** This signal should always be pulled high

4.30 Functional Strap Definitions –Table 4

<table>
<tr><th>Name</th><th>Usage</th><th>When Sampled</th><th>Comment</th></tr>
<tr><td>GNT1# / GPIO51</td><td>Boot BIOS Strap bit [1] BBS[1]</td><td>Rising edge of PWROK</td><td>This Signal has a weak internal pull-up.
Note: the internal pull-up is disabled after PCIRST# de-asserts.
This field determines the destination of accesses to the BIOS memory range. Also controllable via Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.
Bit11 Bit 10 Boot BIOS Destination
0 1 Reserved
1 0 PCI
1 1 SPI
0 0 LPC
NOTE: If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Ibex Peak require SPI flash connected directly to the Ibex Peak's SPI bus with a valid descriptor in order to boot.
NOTE: Booting to PCI is intended for debut/testing only.
Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel Management Engine or Integrated GbE LAN.</td></tr>
</table>

4.30 Functional Strap Definitions –Table 5

Name	Usage	When Sampled	Comment
GNT[0]#	Boot BIOS Strap bit[0] BBS[0]	Rising edge of PWROK	This Signal has a weak internal pull-up. Note: the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also controllable via Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC **NOTE:** If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Ibex Peak require SPI flash connected directly to the Ibex Peak's SPI bus with a valid descriptor in order to boot. **NOTE:** Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.

4.30 Functional Strap Definitions –Table 6

Name	Usage	When Sampled	Comment
GNT[0]#	Boot BIOS Strap bit[0] BBS[0]	Rising edge of PWROK	This Signal has a weak internal pull-up. Note: the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also controllable via Boot BIOS Destination bit (Chipset Config Registers:Offset 3410h:bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC **NOTE:** If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Ibex Peak require SPI flash connected directly to the Ibex Peak's SPI bus with a valid descriptor in order to boot. **NOTE:** Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.

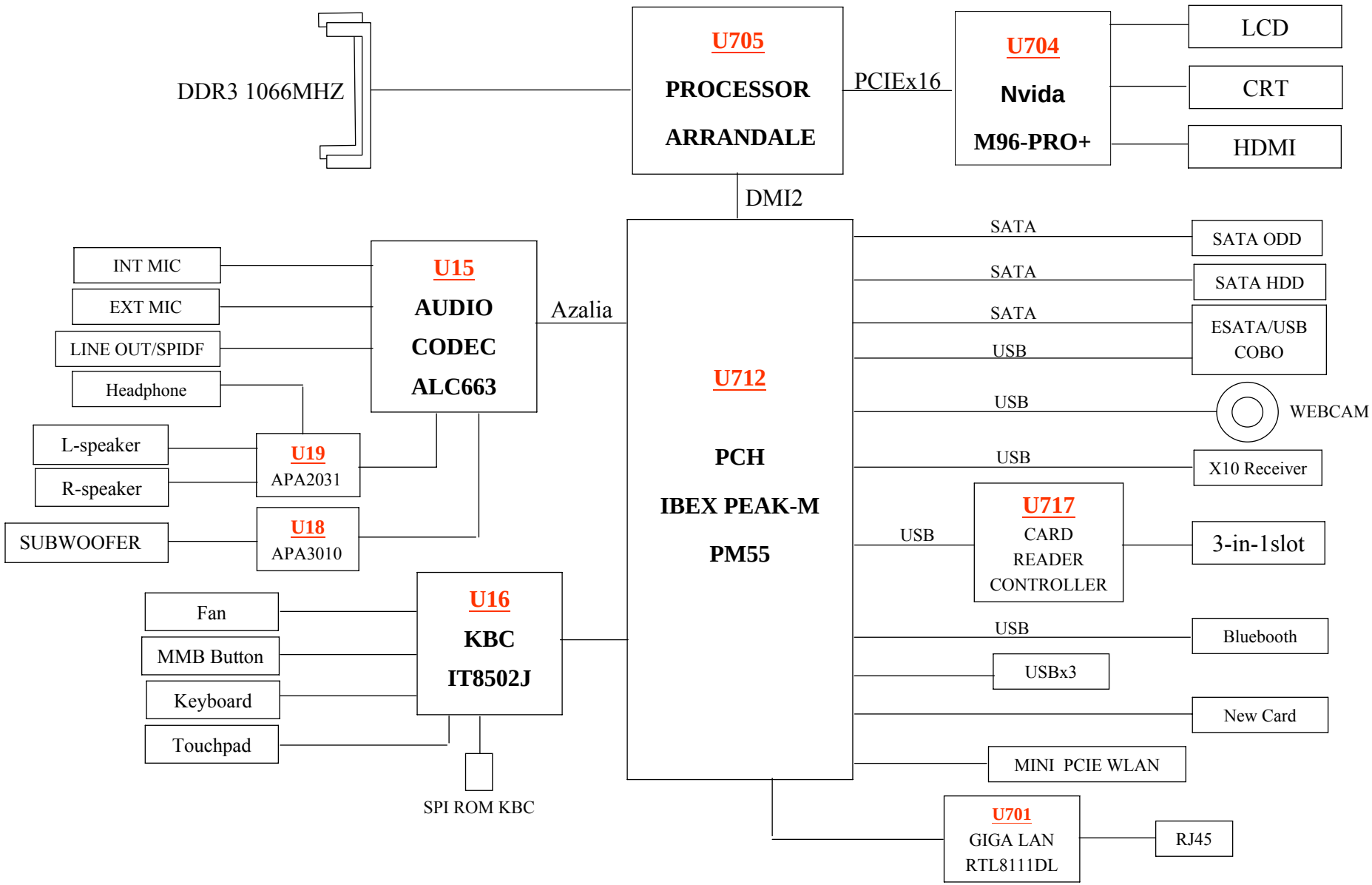
4.30 Functional Strap Definitions –Table 7

Name	Usage	When Sampled	Comment
GNT2#/ GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	This Signal has a weak internal pull-up. **Note:** the internal pull-up is disabled after PCIRST# de-asserts.Tying this strap low configures DMI for ESI compatible operation. **NOTE:** ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
NV_ALE	Intel® Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	Rising edge of PWROK	Signal has internal pull-down. Intel AT-d is disabled when sampled low (default). Intel AT-d is capable of being enabled when sampled high. **NOTE:** This strap, softstrap AT-d_DIS in Section 22.2.5.1, softstrap VE Enabled in Section 22.2.5.11and Ibex Peak SKU capable of AT-D are necessary to enable this functionality.
HDA_DOCK_EN#/GPIO[33]	Flash Descriptor Security Override/ ME Debug Mode	Rising edge of PWROK	Signal has a weak internal pull-up. If strap is sampled high, the security measures defined in the Flash Descriptor will be in effect (default) If sampled low, the Flash Descriptor Security will be overridden. This strap should only be asserted low via external pull down in manufacturing/debug environments ONLY. **NOTE:** Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel Management Engine after chipset bringup and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manfacturing/ debug.

4.30 Functional Strap Definitions –Table 8

Name	Usage	When Sampled	Comment
SPI_MOSI	TPM Functionality Disable	Rising edge of MEPWROK	This signal has a weak internal pull-down resistor. This signal must be sampled low.
NV_CLE	DMI Termination Voltage	Rising edge of PWROK	This signal has a weak internal pull-down.
HDA_SDO	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull down. NOTE: This signal should not be pulled high
GPIO8	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull up. **Note:** the weak internal pull-up is disabled after RSMRST# de-asserts. **NOTE:** This signal should not be pulled low
GPIO27	On-Die PLL Voltage Regulator	Rising edge of RSMRST# pin	This signal has a weak internal pull-up. Note: the internal pull-up is disabled after RSMRST# de-asserts. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	This signal has a weak internal pull down. On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.
GPIO15	Reserved	Rising edge of RSMRST# pin	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality This signal has a weak internal pull down. **NOTE:** A strong pull up may be needed for GPIO functionality

5. System Block Diagram



6. Trouble Shooting

- **6.1 No Power (*1)**
- **6.2 No Display (*2)**
- **6.3 Graphics Controller Failure LCD No Display**
- **6.4 External Monitor No Display**
- **6.5 Memory Failure**
- **6.6 Keyboard (K/B) or Touch-Pad (T/P) Failure**
- **6.7 Hard Disk Drive Failure**
- **6.8 ODD Failure**
- **6.9 USB Ports Failure**
- **6.10 Audio Failure**
- **6.11 LAN Failure**
- **6.12 Card Reader Slot Failure**
- **6.13 Mini Express (Wireless) Socket Failure**
- **6.14 Express Card Socket Failure**

*1: No Power Definition

Base on ACPI Spec. We define the no power as while we press the power button, the system can't leave S5 status or none the PG signal send out from power supply.

Judge condition:

- Check whether there are any voltage feedback control to turn off the power.
- Check whether no CPU power will cause system can't leave S5 status.

If there are not any diagram match these condition, we should stop analyzing the schematic in power supply sending out the PG signal. If yes, we should add the effected analysis into no power chapter.

*2: No Display Definition

Base on the digital IC three basic working conditions: working power, reset, Clock. We define the no display as while system leave S5 status but can't get into S0 status.

Judge condition:

- Check which power will cause no display.
- Check which reset signal will cause no display.
- Check which Clock signal will cause no display.

Base on these three conditions to analyze the schematic and edit the no display chapter.

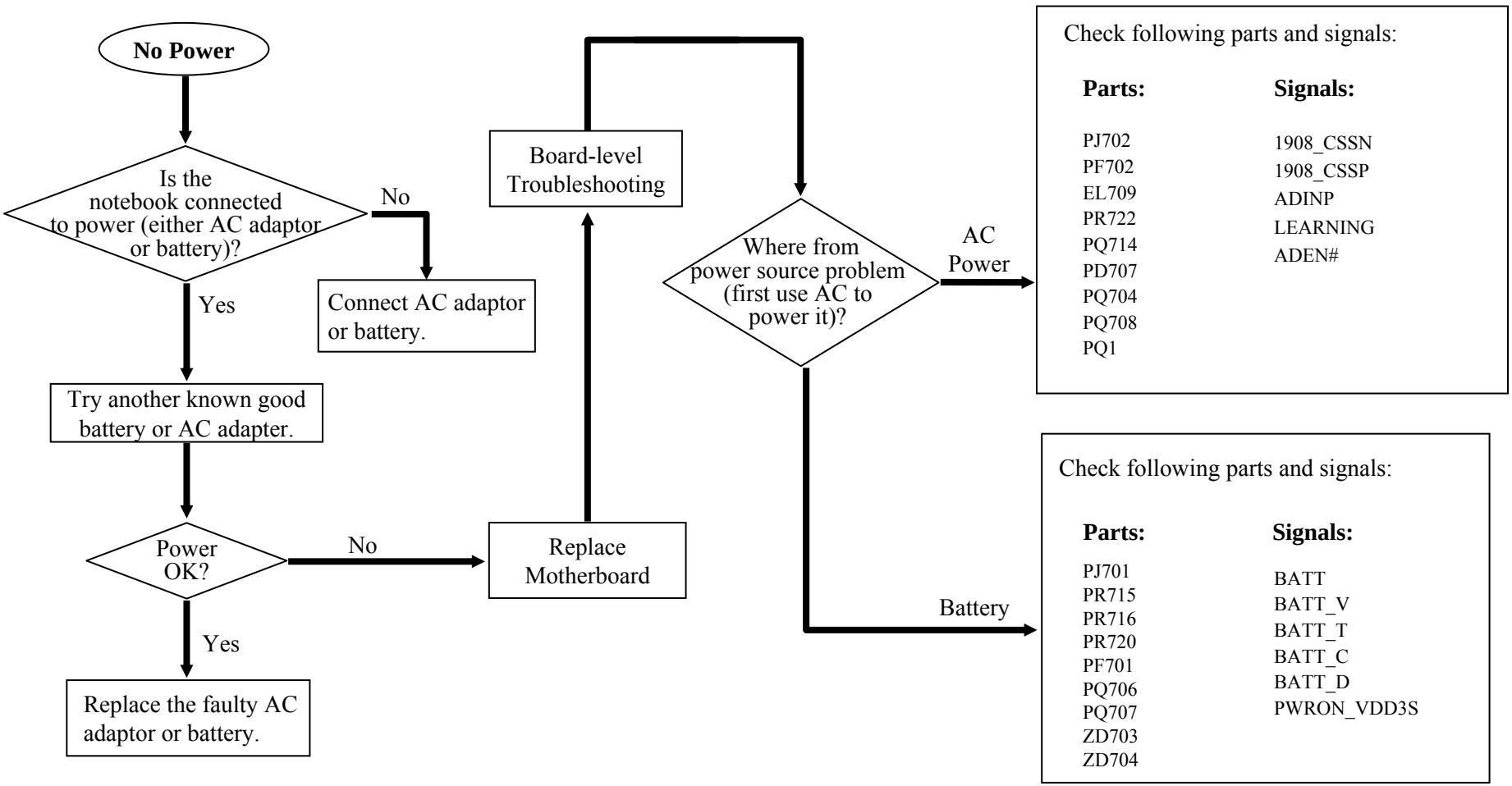
Keyword:

- S5: *Soft Off*
- S0: *Working*

For detail please refer the ACPI specification.

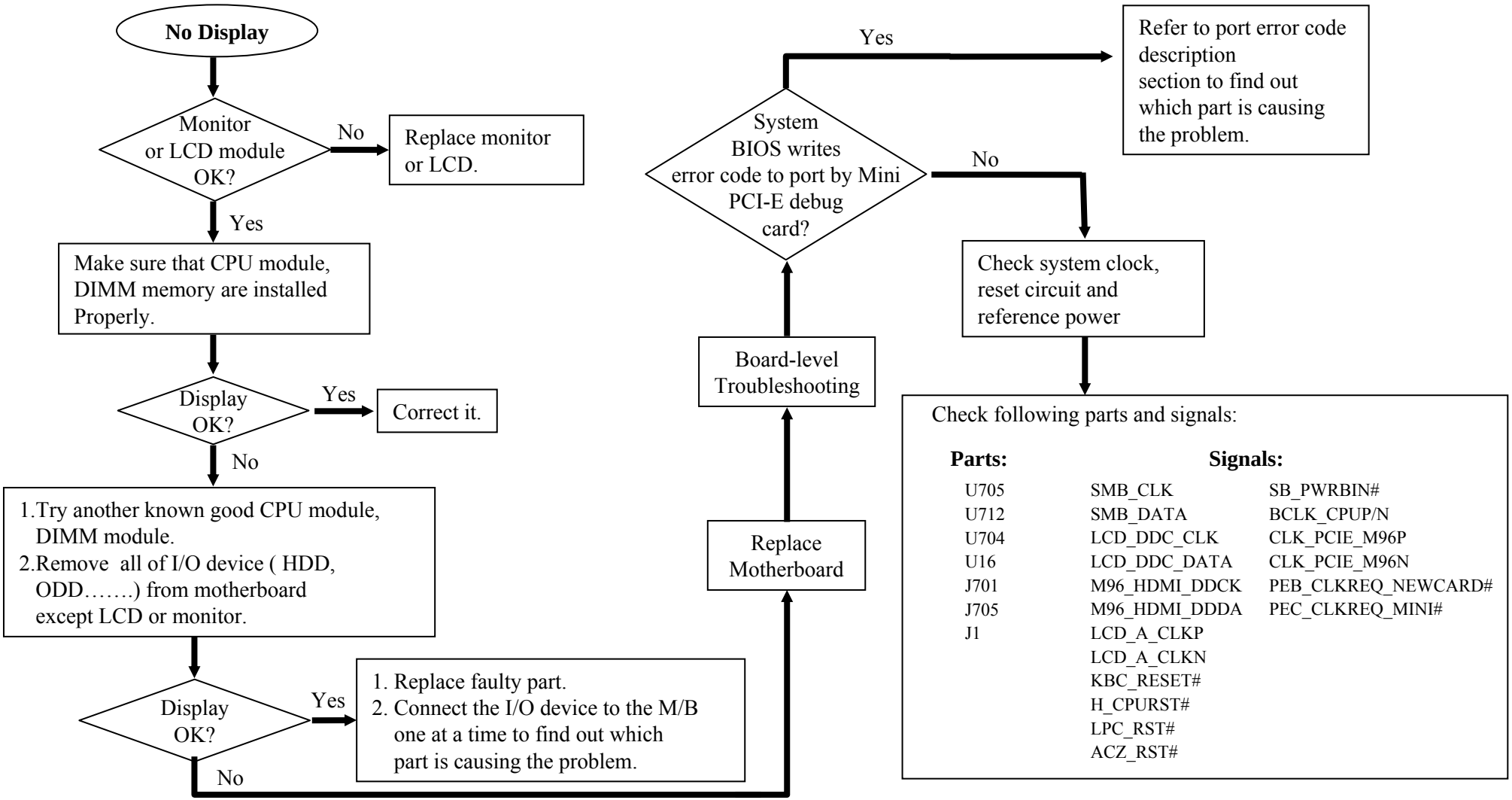
6.1 No Power

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



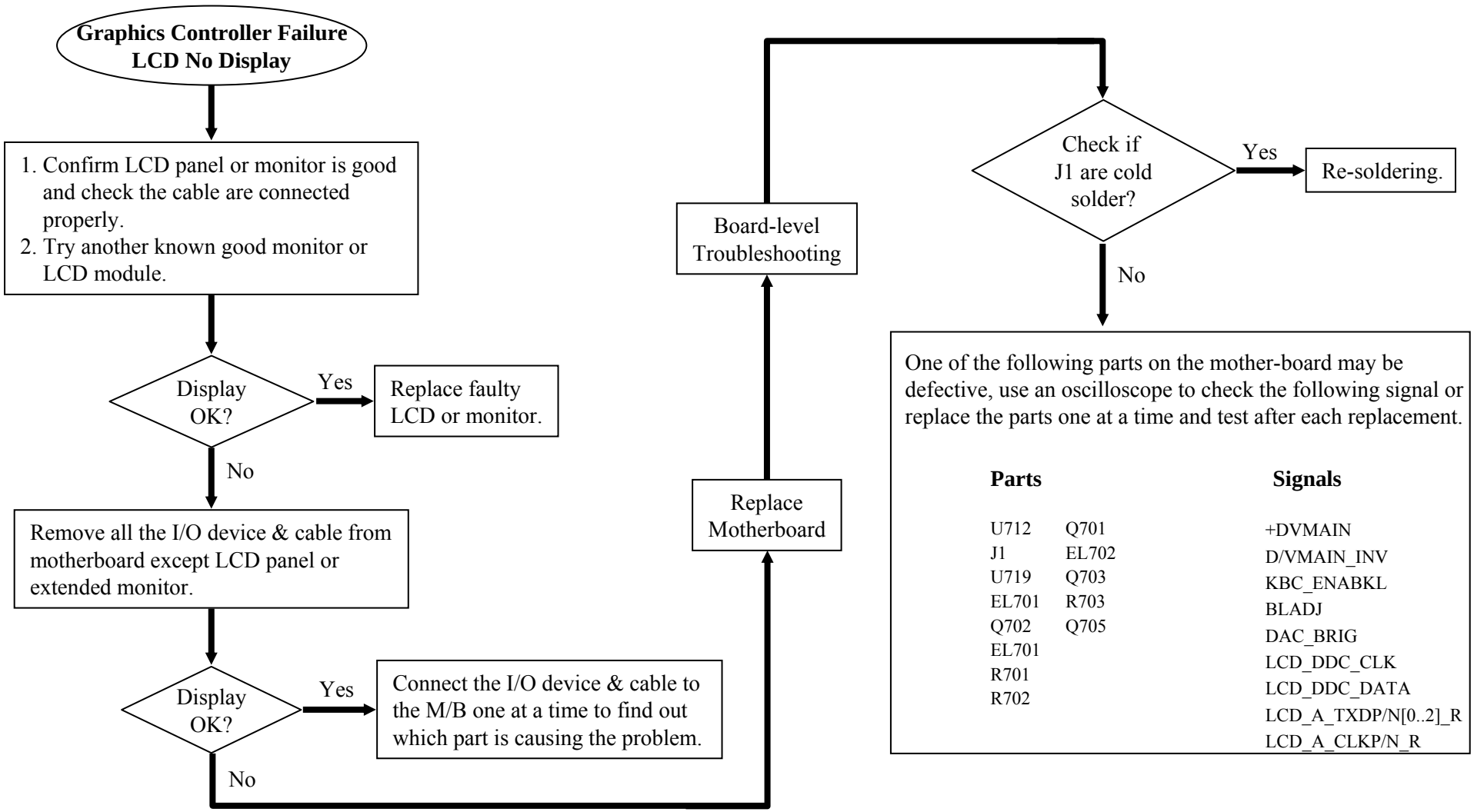
6.2 No Display

There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



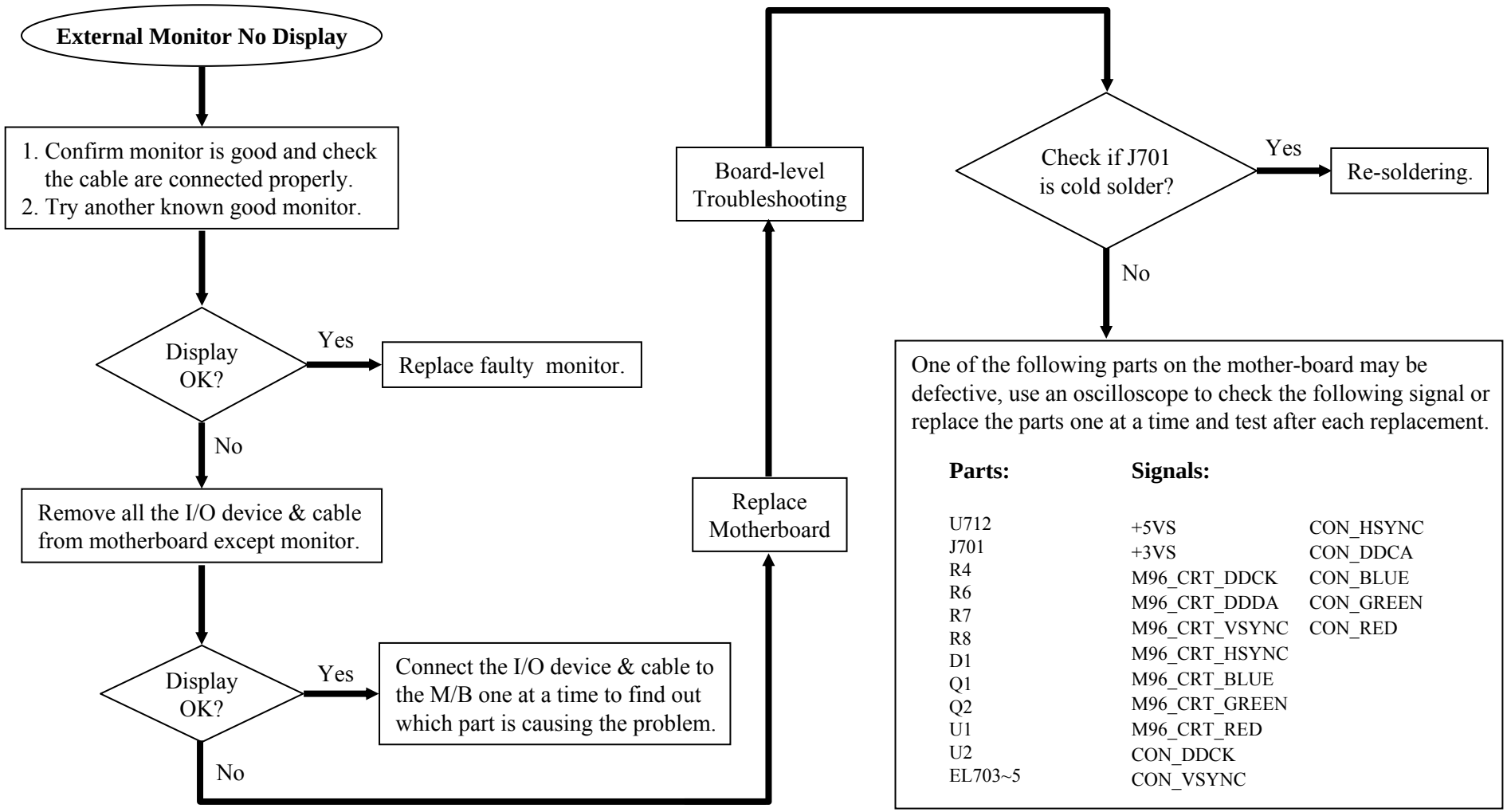
6.3 Graphics Controller Failure LCD No Display

There is no display or picture abnormal on LCD although power-on-self-test is passed.



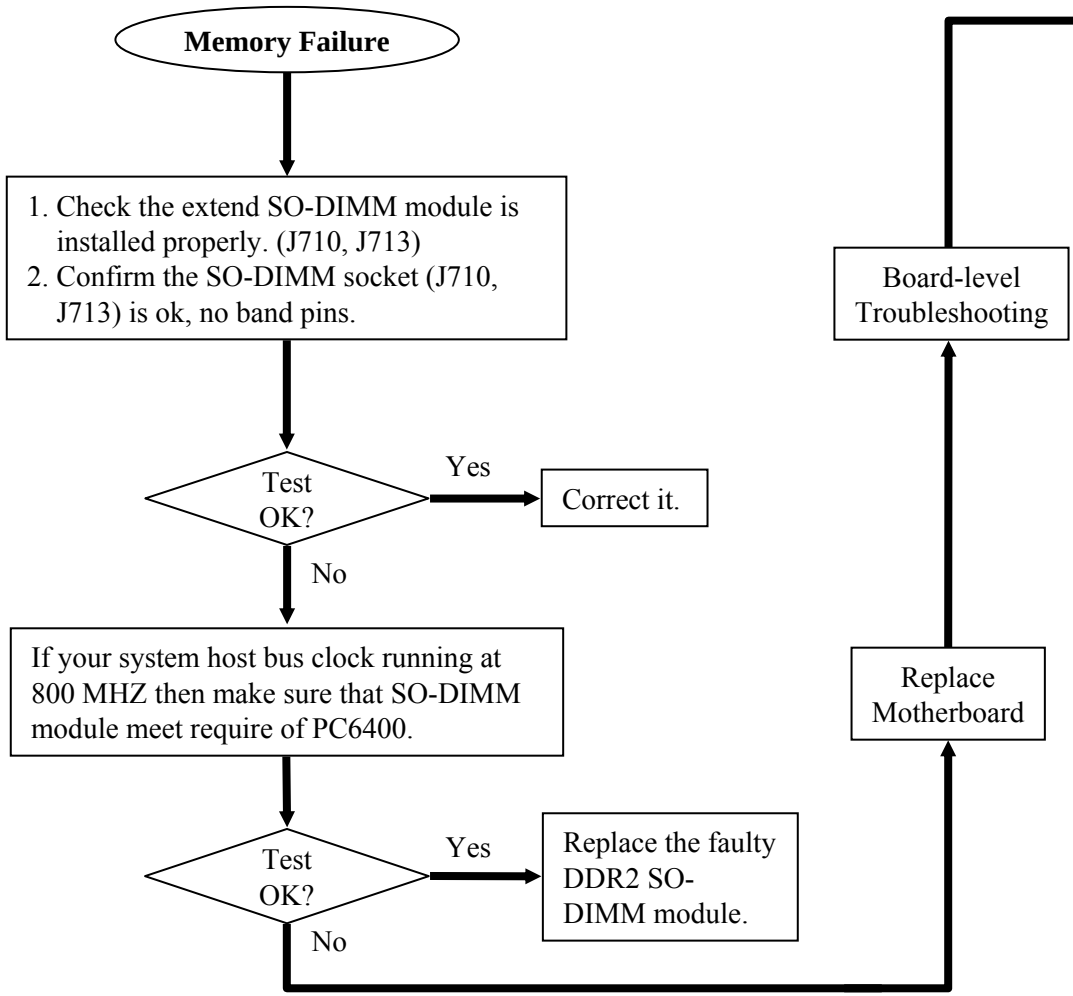
6.4 External Monitor No Display

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



6.5 Memory Failure

Extend DDR2 SO-DIMM is failure or system hangs up.

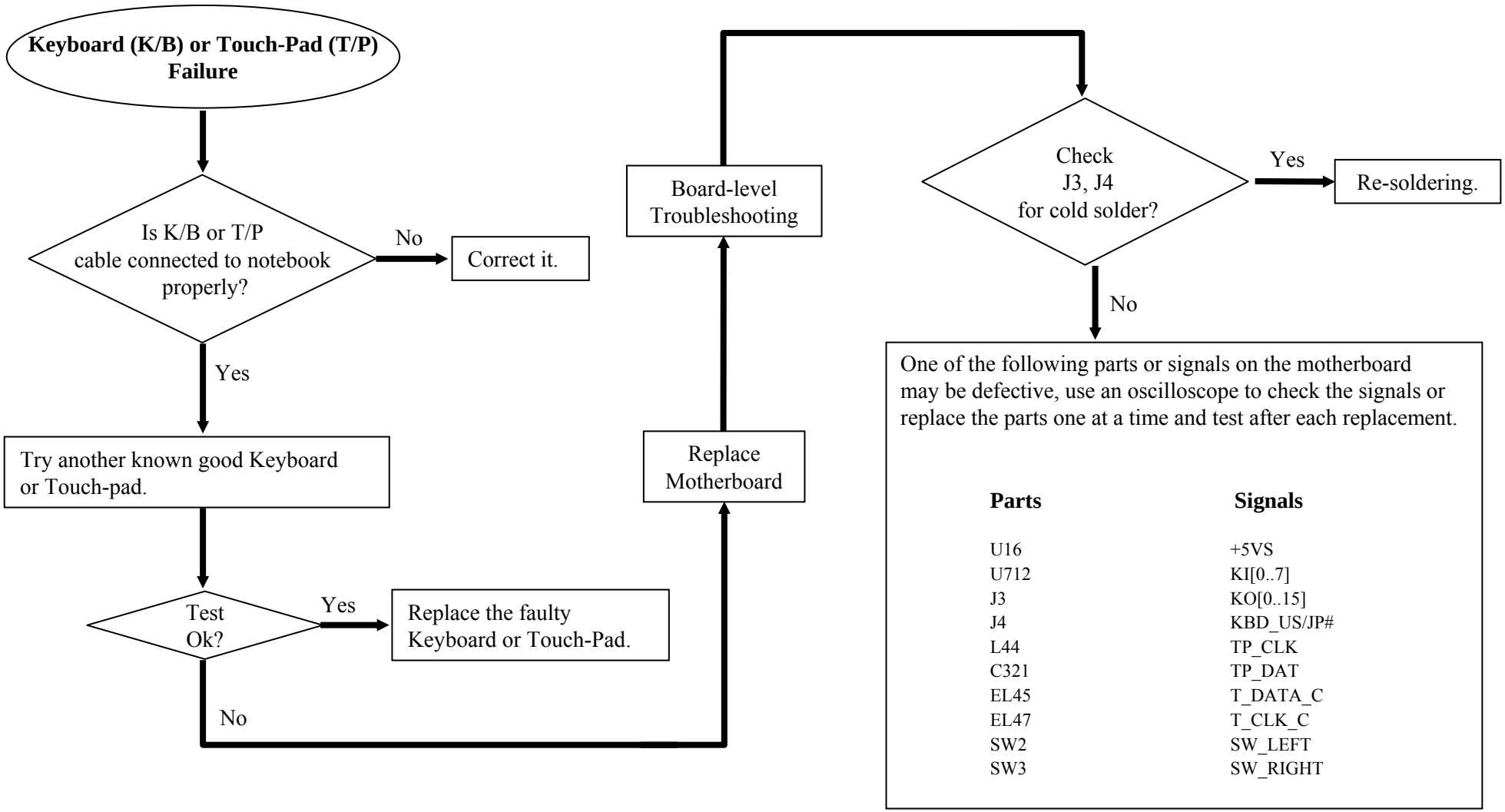


One of the following components or signals on the motherboard may be defective ,Use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**	
U712	M_VREF_DQ_DIMM0	DDR_A/B_RAS#
J708	DDR_A/B_DQ[0..63]	
J707	DDR_A/B_DQSN[0..7]	
EL48	DDR_A/B_DQSP[0..7]	
R797	DDR_A/B_DM[0..7]	
R798	DDR_CKE[0..3]	
EL722	DDR_A/B_BS[0..2]	
R711	DDR_A/B_MA[0..15]	
R759	DDR_A/B_WE#	
R176	DDR_A/B_CAS#	
R178	DDR_CS#[0..3]	
R774	DDR_ODT[0..3]	
R795	SMBDATA_DDR3	
	SMB_CLK_DDR3	

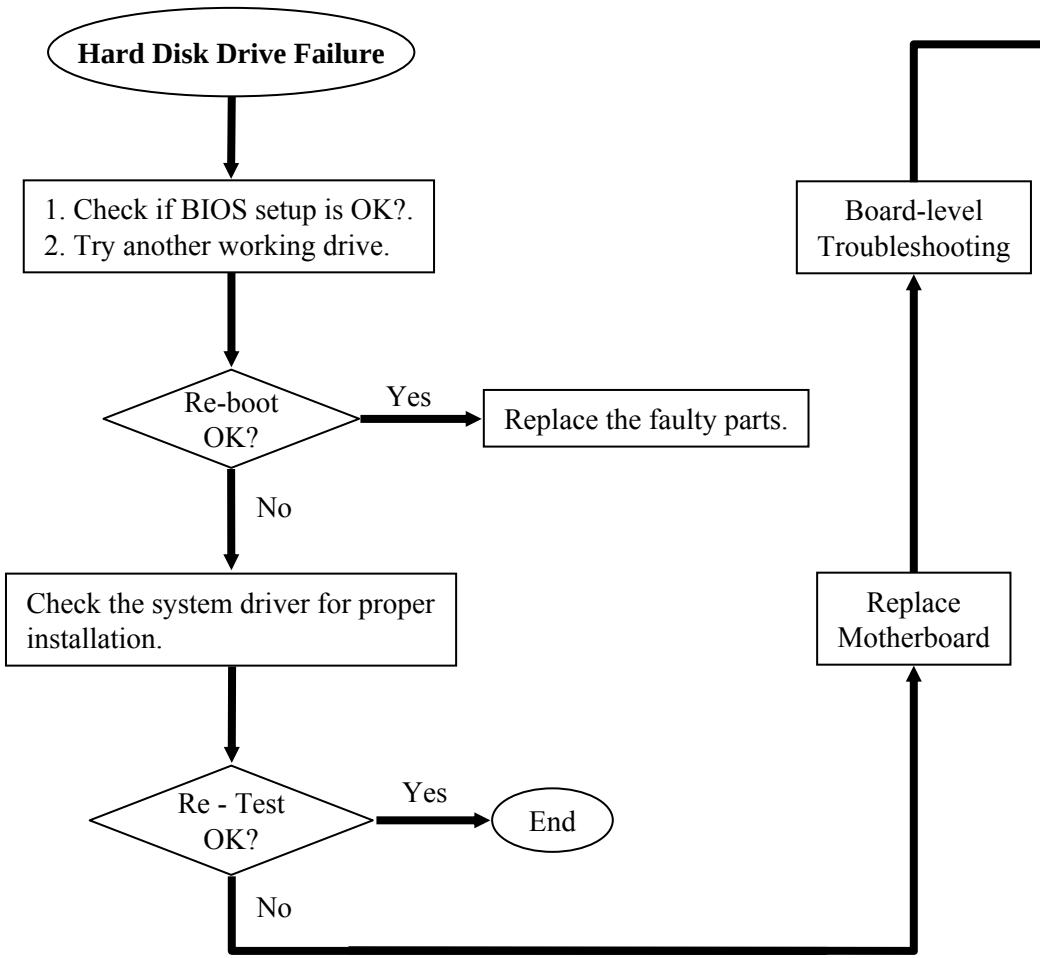
6.6 Keyboard (K/B) or Touch-Pad (T/P) Failure

Error message of keyboard or touch-pad test error is shown or any key does not work.



6.7 Hard Disk Drive Failure

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.

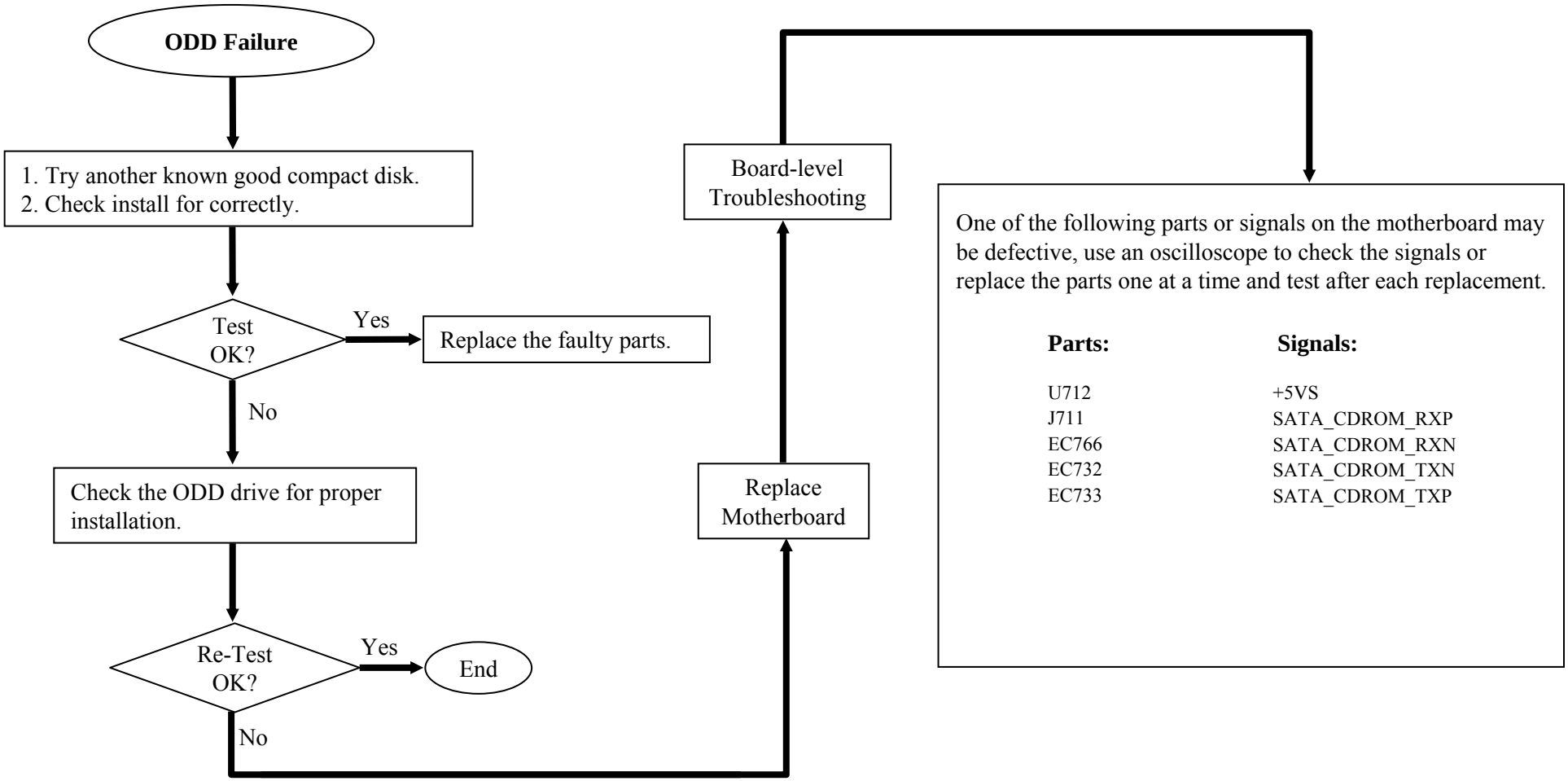


One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts		Signals
U712	EC749	+5VS
J715	EC750	+5VS_HDD
EL738		SATAHDD_RXP
EL740		SATAHDD_RXN
R912		SATAHDD_TXN
C1031		SATAHDD_TXP
C1032		
C1036		
C1038		
C1018		
C1013		
C1012		
C1025		
C1028		

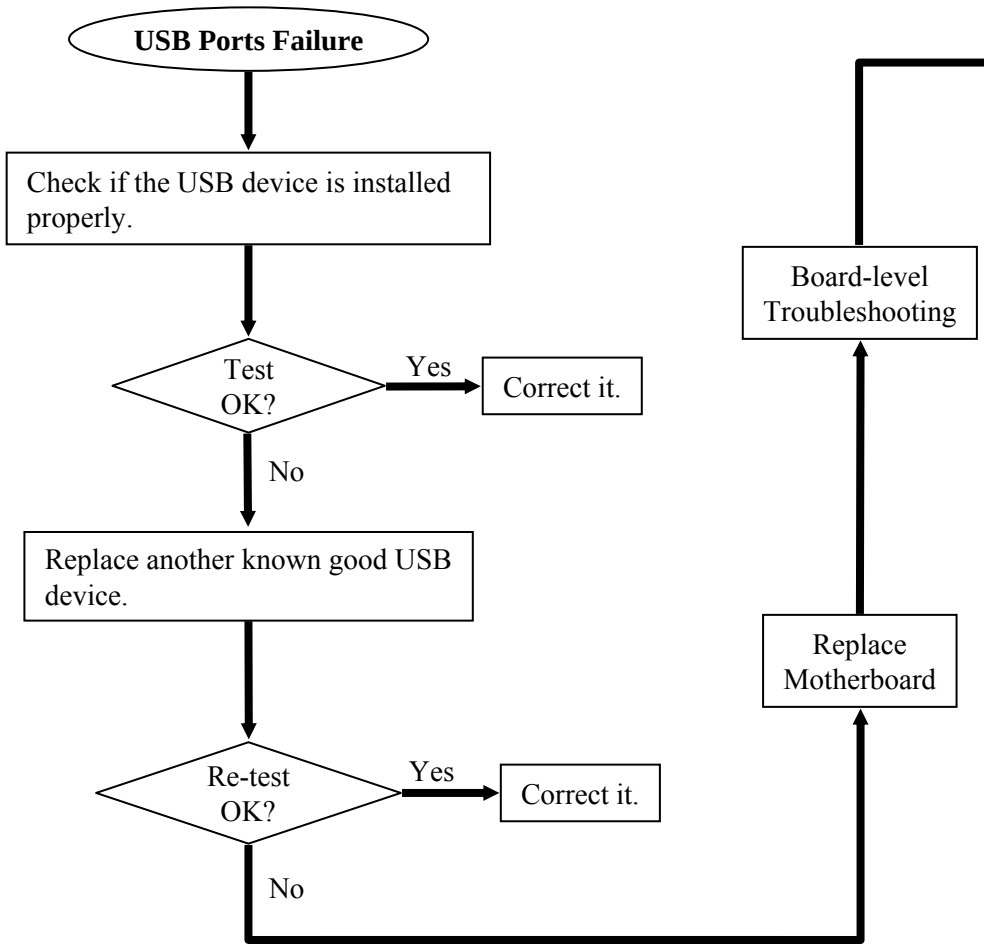
6.8 ODD Failure

An error message is shown when reading data from ODD drive.



6.9 USB Ports Failure

An error occurs when a USB I/O device is installed.

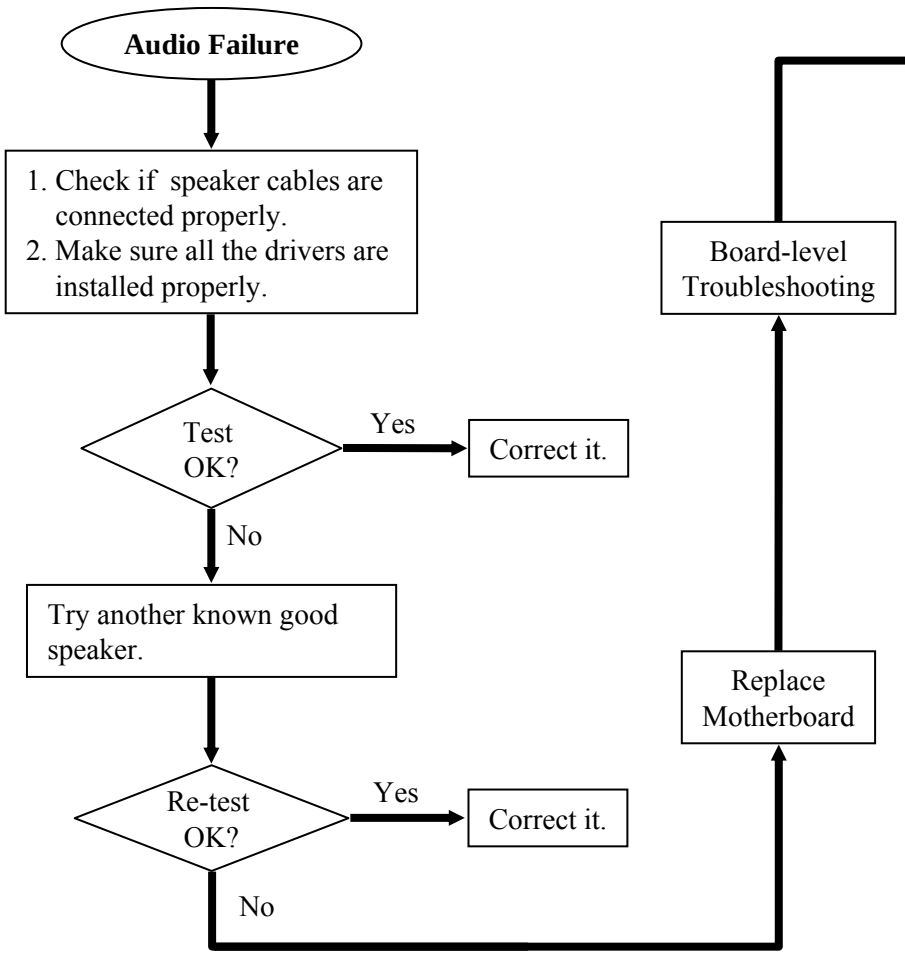


Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**
U712	+5V
J710	SUSC#
J713	USB_OC2#
BKJ701	USB_OC0#
EL46	USB_OC3#
EL64	USBPP3
U7	USBPN3
EL37	USBPP2
U711	USBPN2
EL730	USBBKPP0
U714	USBBKPN0
L714	
BKEL701	
BKEL701	

6.10 Audio Failure

No sound from speaker after audio driver is installed.



Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

1.If no sound cause of line out, check the following parts & signals:

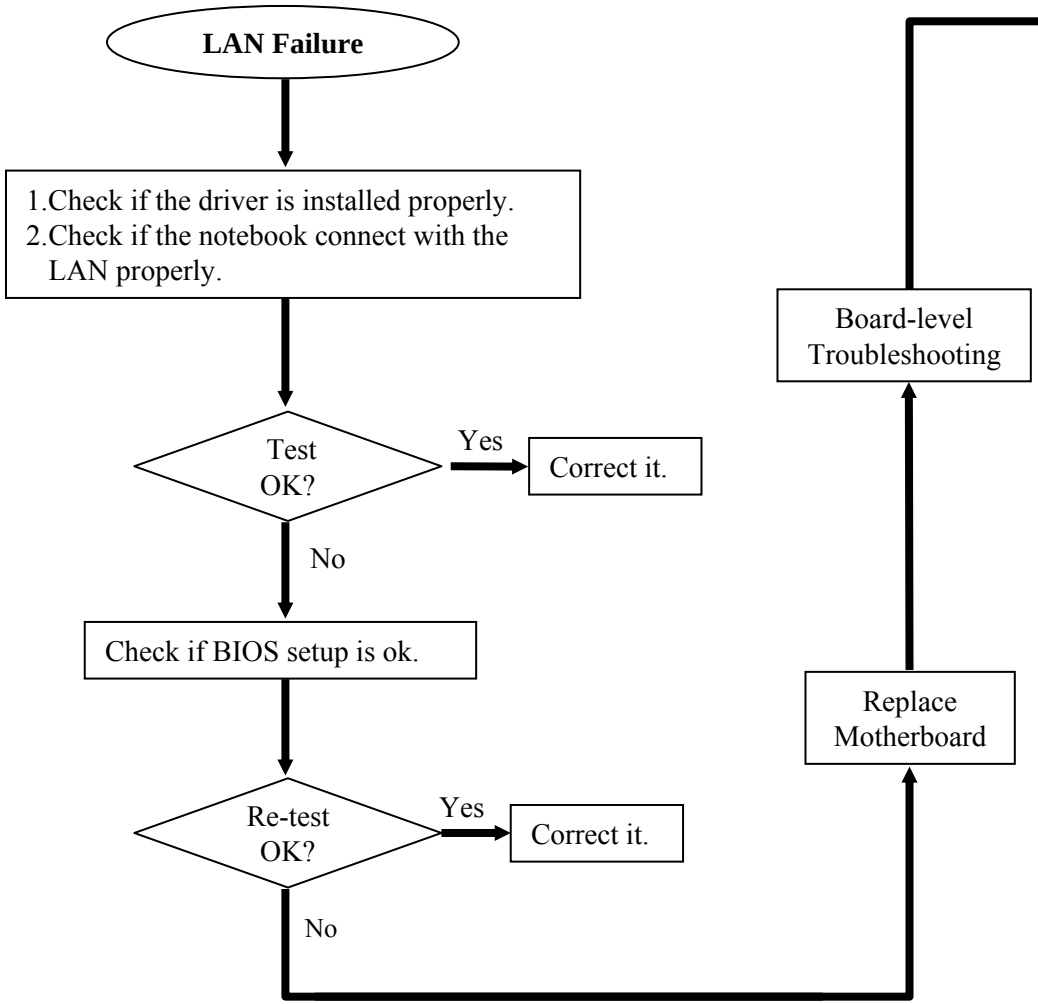
Parts:	Signals:
U712	AVDD
U15	SPDIFOUT
J9	PC_BEEP
J2	ACZ_RST#0
J706	ACZ_SYNC0
U18	ACZ_SDIN0
U19	ACZ_SDOUT0
Q38	AMP_LEFT
EL81	AMP_RIGHT
R349	
R334	

2. If no sound cause of MIC, check the following parts & signals:

Parts:	Signals:
U709	AVDD
U14	SPDIFOUT
Q33	AUDIO_PWR_ON
R309	PC_BEEP
Q29	ACZ_RST#0
EL18	ACZ_SYNC0
R267	ACZ_SDIN0
EL15	ACZ_SDOUT0
EL14	MIC2_R
R254	MIC2_L
R255	MIC2_VREF
R256	

6.11 LAN Failure

An error occurs when a LAN device is installed.

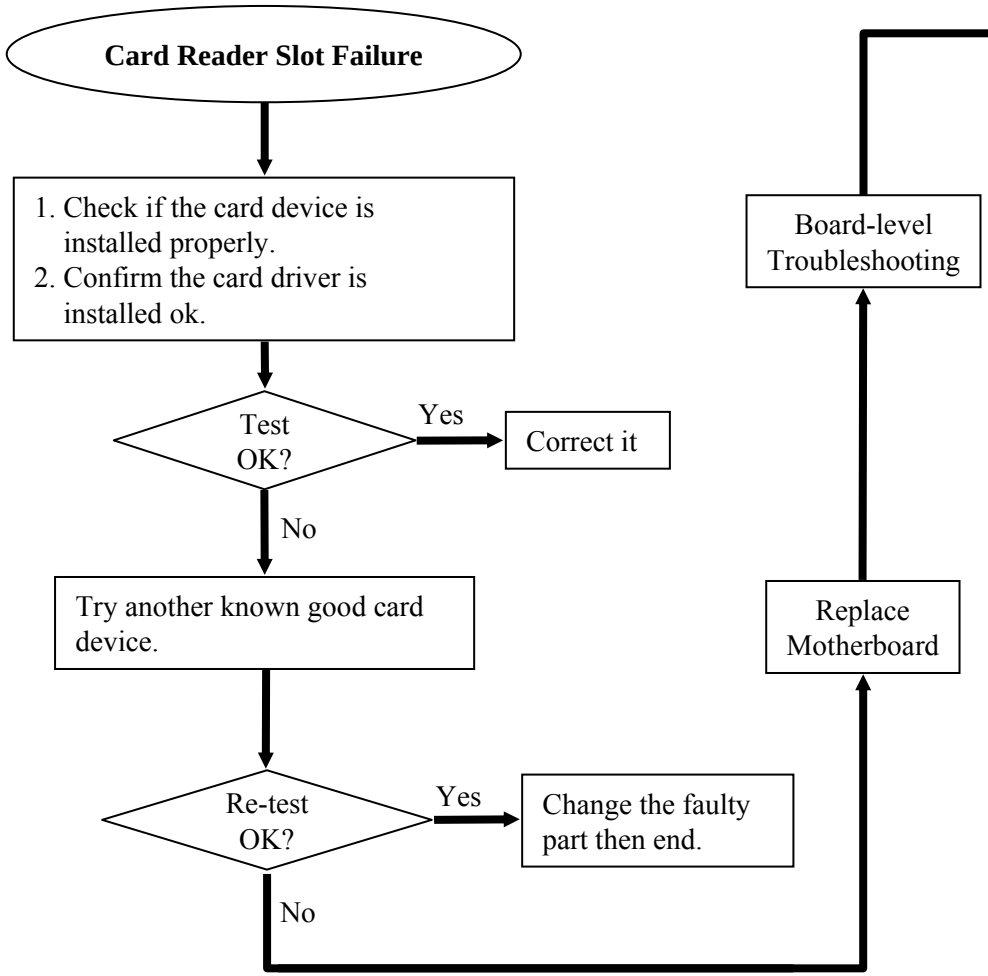


Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**
U712	PLT_RST#
U701	PCIE_WAKE#
J703	LAN_CLKREQ#
EL745	LAN_PCIE_RXN
EL706	LAN_PCIE_RXP
EL707	LAN_PCIE_TXP
EL708	LAN_PCIE_TXN
R716	CLK_PCIE_LANP
R715	CLK_PCIE_LANN
C728	LAN_ISOLATEB
C729	

6.12 Card Reader Slot Failure

An error occurs when a card device is installed.

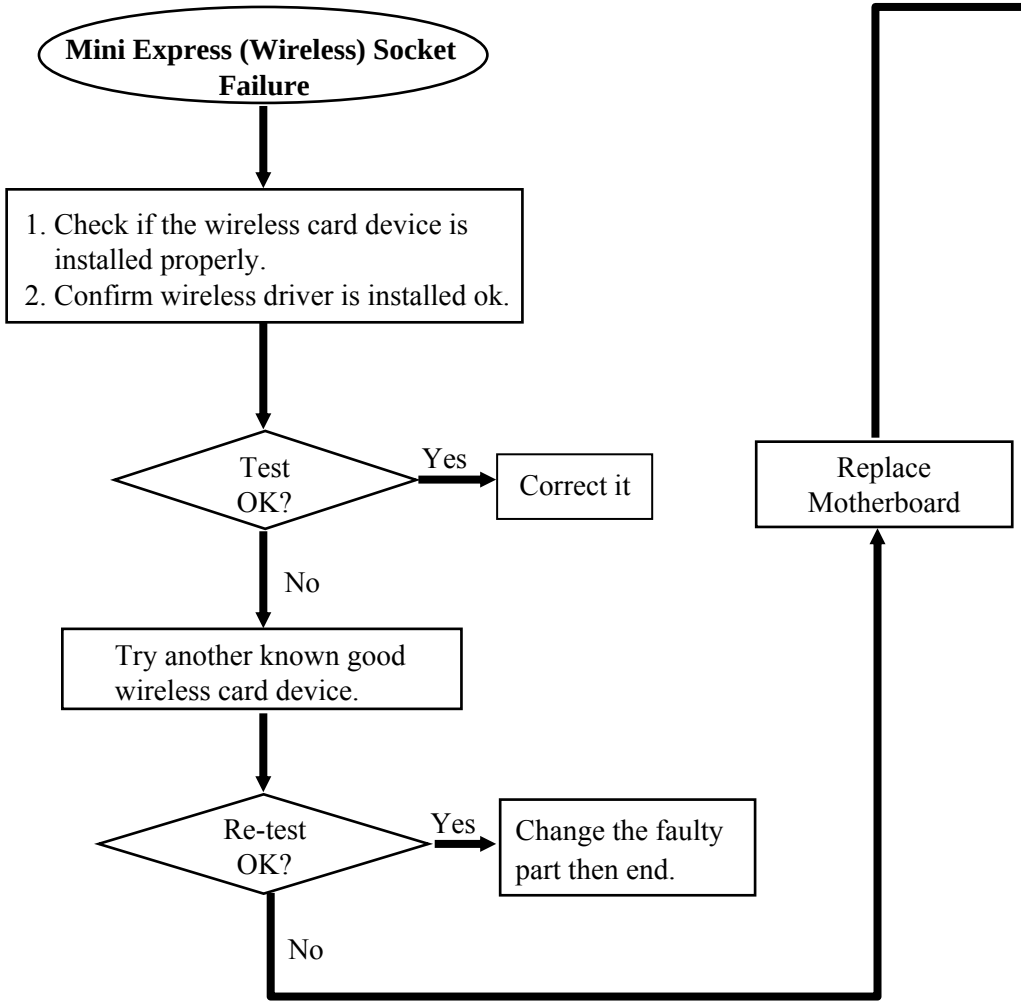


Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**
U712	CR_RST#
U717	SD_DATA2
J716	SD_DATA3
R933	SD_CMD
R900	MS_CLK
ER705	SD_CLK
ER706	MS_CD#
X705	SD_D0_MS_D0
C1045	MS_D1
C1046	MS_BS
	SD_D1
	SD_CD#
	SD_WP
	USBPN4
	USBPP4

6.13 Mini Express (Wireless) Socket Failure

An error occurs when a wireless card device is installed.

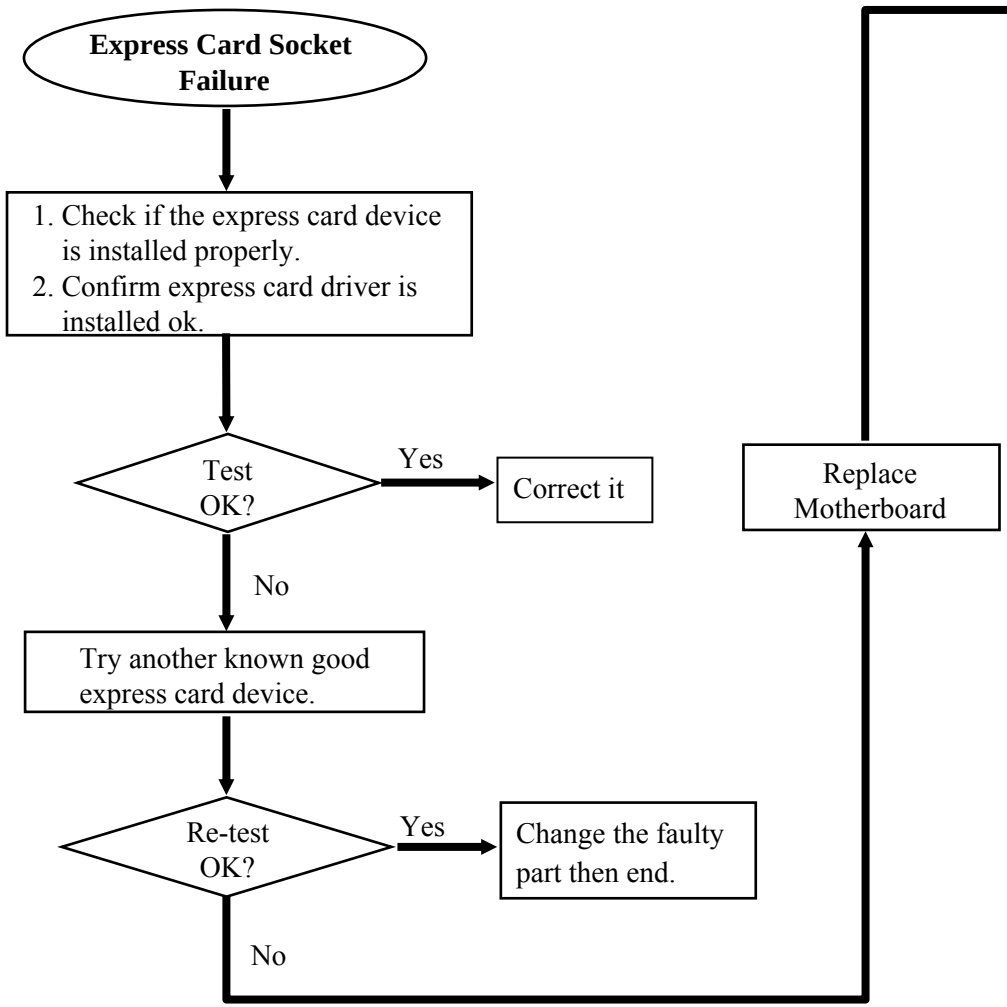


Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**
U712	PCIE_WAKE#
J714	PEC_CLKREQ_MINI#
R919	CLK_PCIE_MINI_N
R920	CLK_PCIE_MINI_P
R901	MINI_PCIE_RXN
R904	MINI_PCIE_RXP
R916	MINI_PCIE_TXN
	MINI_PCIE_TXP
	WLAN_PD#

6.14 Express Card Socket Failure

An error occurs when a express card device is installed.



Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**
U712	CPUSB#
J10	USBPN9
U716	USBPP9
R923	SMB_CLK
C1026	SMB_DATA
C1027	PCIE_WAKE#
C1023	CPERST#
C1024	CLKREQ_CARD#
Q708	CPPE#
R924	CLK_PCIE_CARDN
	CLK_PCIE_CARDP
	NEWCARD_PCIE_RXN

Reference Material

❖ Intel Arrandale Processor	Intel, INC
❖ Intel Ibex Peak chipset	Intel, INC
❖ ATI M96-PRO+ VGA Controller	AMD, INC
❖ Keyboard controller IT8502J	WIN, INC
❖ Hardware Engineering Specification	*Technology Corp*/MITAC

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