88-S4K Memory Board

Addenda Page

November, 1976

In order to make the 88-S4K Memory Board compatible with memory boards that use wait states (the 88-PMC or the 88-1MCS), the following modifications must be implemented. If neither of these boards are used, the modifications are not necessary. If your 88-S4K board was factory assembled, it can be returned to the factory for installation of these modifications. The only customer charge will be shipping costs.

1. There are four lands on the silkscreened side of the S4K board that must be cut. One land comes off IC N, pin 3. The other three come off IC V at pins 10, 8 and 13. The small arrows in Figure 1 point to each of the lands and small "x's" designate the exact points at which the lands should be cut.

2. There are six jumper connections that must be made on the back of the S4K board. They are:

   a) V10 and V13 to +5v (V14)
   b) K3 to G11
   c) N8 to G12
   d) V8 to N10
   e) G8 to M1
   f) G13 to F8

   The locations for these connections are shown by the screened lines in Figure 2.

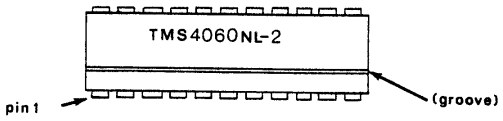
Refer to Figure 3 for a simplified diagram of where the land cuts and jumper connections should be made.

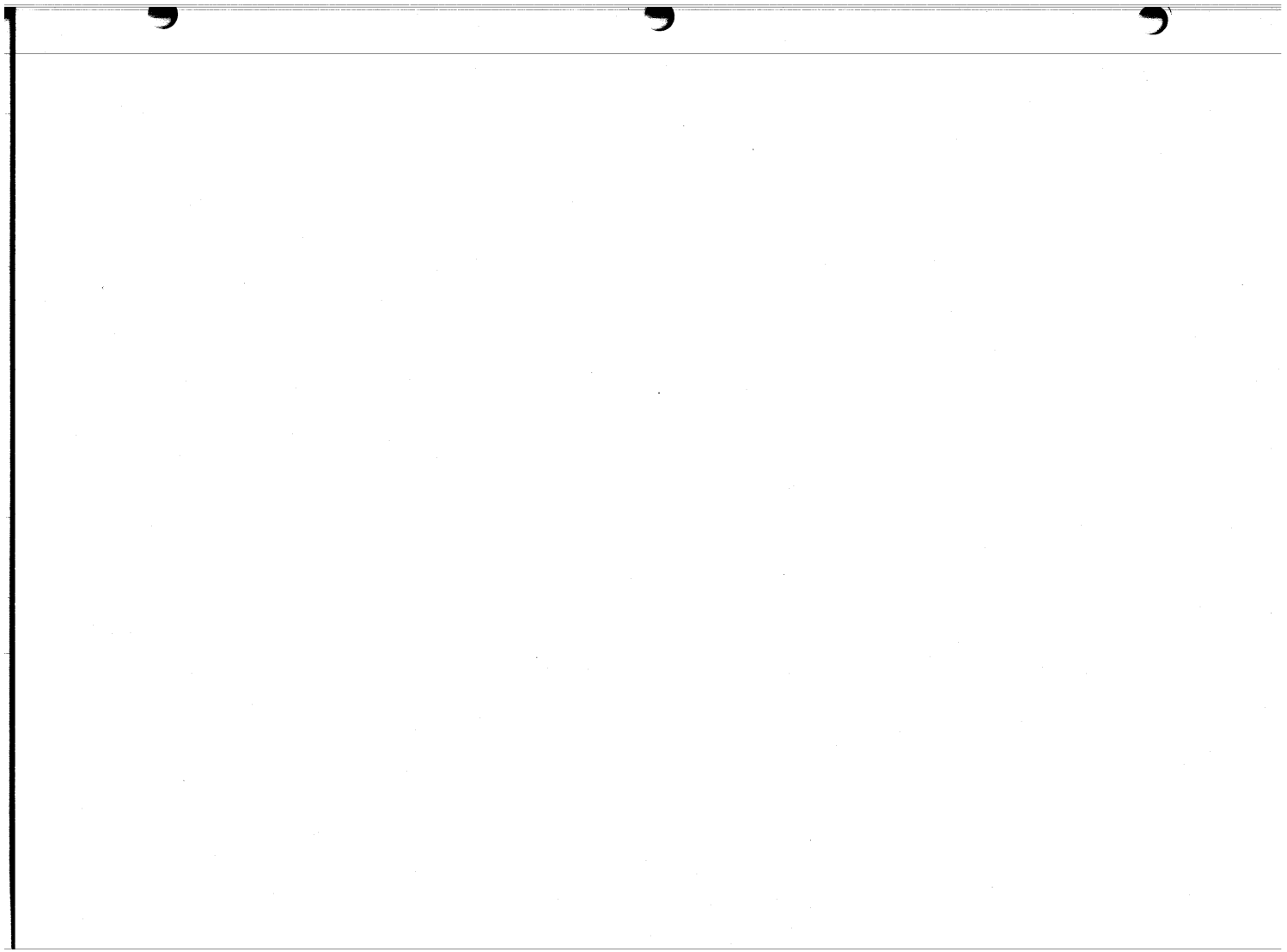
Figure 4 shows how the board should look when all of the modifications have been completed.

INSERT PAGE

IC Identification Chart

The IC Identification Chart included in this manual does not show pin 1 identification for the type of IC shown below. Use this diagram to identify pin 1 if ICs of this type have been supplied with your unit. (TMS 4060NL-2 is illustrated as an example)





ALTAIR 88-S4K

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2450 Alamo SE/Albuquerque, NM 87106/505-243-7821

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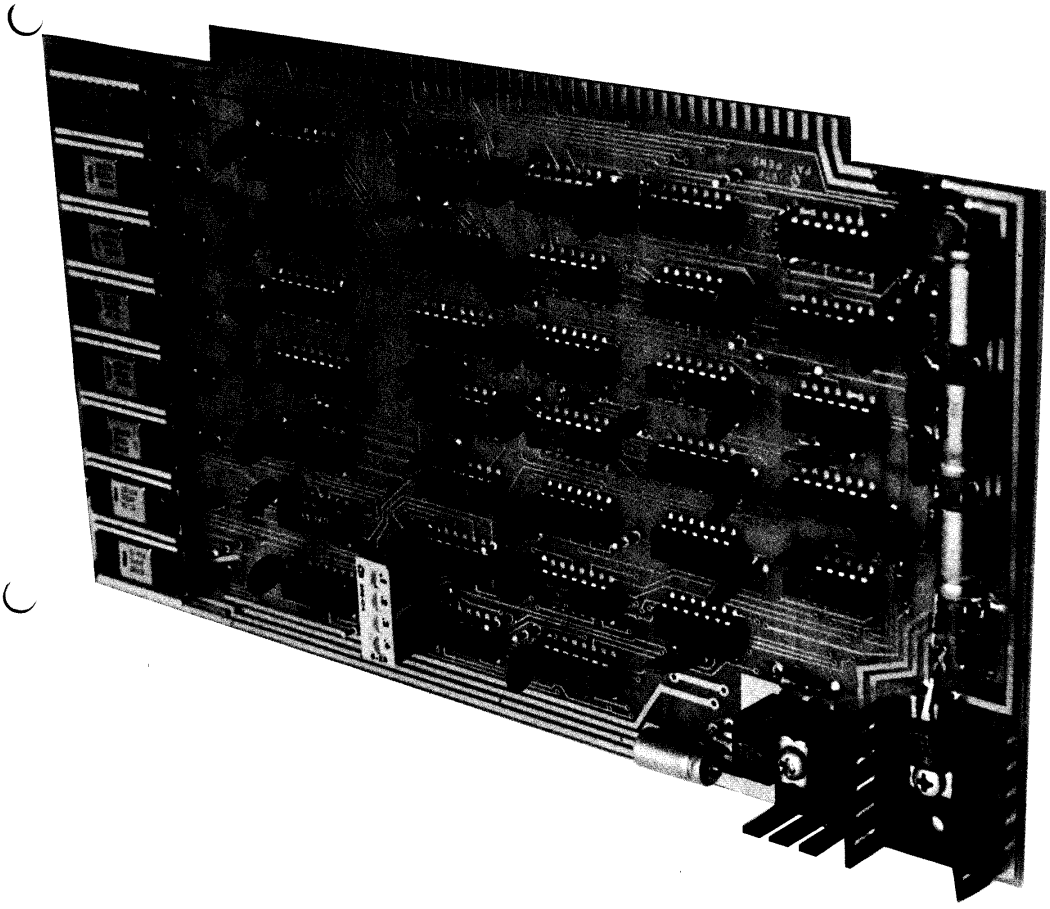


Figure 1-1. Synchronous 4K Memory Board

SECTION I

INTRODUCTION

1-1. SCOPE

The Altair 88-S4K documentation provides a general description of the Altair 88-S4K Synchronous 4K Memory Board and its detailed theory and assembly instructions. The board is compatible with the Altair 8800, 8800a and 8800b.

1-2. ARRANGEMENT

This manual contains three sections as follows.

Section I: General Description

Section II: Theory of Operation

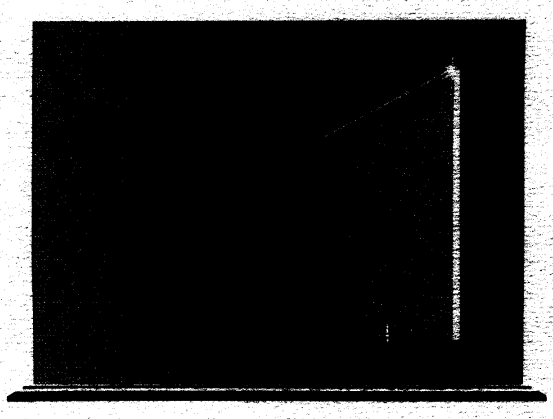
Section III: Assembly Instructions

1-3. DESCRIPTION

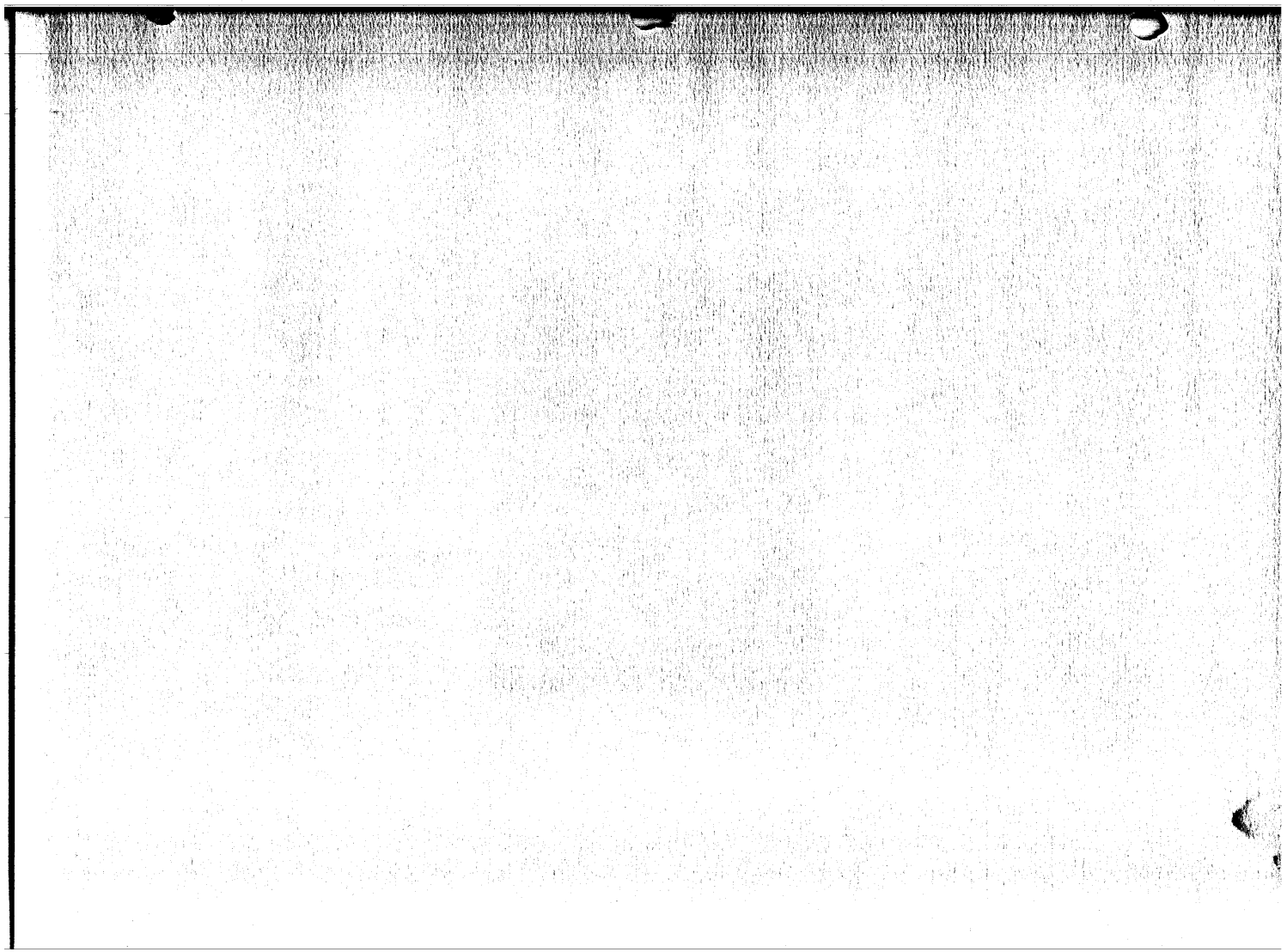
The Altair 88-S4K Synchronous 4K Memory Board provides 4,096 bytes of random access memory while consuming very low power. It contains memory protect circuitry for any one of 16 starting locations in increments of 4K. There are no wait states (CPU runs at full speed) and the access time is 200-300 nanoseconds.

altair 88-S4K

SECTION II



Theory of Operation



2-1. GENERAL

This section contains information needed to understand the operation of the MITS 88-S4K (Synchronous 4K Memory Board). It contains a description of logic symbols used in the S4K schematics and detailed theory of operation.

2-2. LOGIC CIRCUITS

The logic circuits used in the S4K drawings are presented in Table 2-1. The table is constructed to present the functional name, symbolic representation, and brief description of each logic circuit. Where applicable, a truth table is provided to aid in understanding circuit operation. Although Table 2-1 does not include every logic circuit used in the drawings, all unmentioned circuits (and their symbolic representations) are variations of the circuits presented and functional descriptions are fundamentally the same. The active state of the inputs and outputs of the logic circuits is graphically displayed by small circles. A small circle at an input to a logic circuit indicates that the input is an active LOW; that is, a LOW signal will enable the input. A small circle at the output of a logic circuit indicates that the output is an active LOW; that is, the output is LOW in the actuated state. Conversely, the absence of a small circle indicates that the input or output is active HIGH.

2-3. SCHEMATIC REFERENCING

The detailed schematics of the S4K Board are drawn to aid in determining signal direction and tracing. A solid arrow (→) on the signal line indicates direction, and the tracing of the signal through the schematics is referenced as it leaves the page. The reference is shown as a number - letter number (e.g. 2-A3), indicating sheet 2 and zone A3. The reference may be shown alone or in a bracket. If the reference is bracketed, the signal is going to another schematic which is referenced outside the bracket. If the reference is shown alone, the signal is going to another page of the multisheet schematic.

Table 2-1. Symbol Definitions

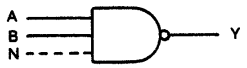
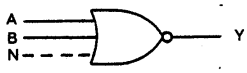
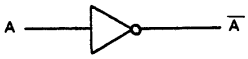
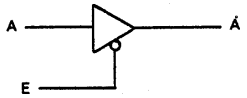
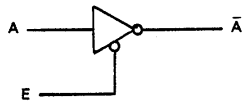
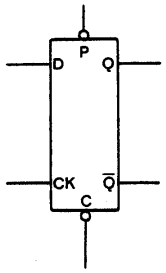
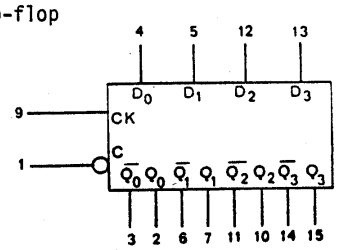
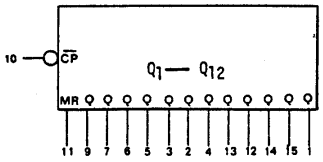
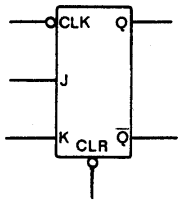
NAME	LOGIC SYMBOL	DESCRIPTION
NAND gate	 $Y = \overline{AB \ldots N}$	The NAND gate performs one of the common logic functions. All of the inputs have to be enabled (HIGH) to produce the desired (LOW) output.
NOR gate	 $Y = \overline{A + B \ldots + N}$	The NOR gate performs one of the common logic functions. Any of the inputs need be enabled (HIGH) to produce the desired (LOW) output.
Inverter		The inverter is an amplifier whose output is the opposite state of the input.
Non-Inverting Bus Driver		The non-inverting bus driver is an amplifier whose output is the same state as the input. Data is enabled through the device by applying a (LOW) signal to the E input.
Inverting Bus Driver		The inverting bus driver is an amplifier whose output is the opposite state of the input. Data is enabled through the driver by applying a (LOW) signal to the E input.

Table 2-1. Symbol Definitions

NAME	LOGIC SYMBOL	DESCRIPTION
Edge triggered D type flip-flop	 TRUTH TABLE	Applying a LOW signal to the preset input (P) sets the flip-flop with output Q HIGH and output $\overline{Q}$ LOW. Applying a LOW signal to the clear input (C) resets the flip-flop with Q LOW and $\overline{Q}$ HIGH. This method of setting and resetting the flip-flop is independent of the clock (asynchronous). If a signal is applied to the D input, the flip-flop Q output is directly affected on the positive edge of the clock (cf. truth table).
QUAD D flip-flop		The information on the D inputs is stored during the positive edge of the clock (CK). The clear (C) input, when LOW, resets all flip-flops independent of the clock or D inputs.

T_n	T_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

Table 2-1. Symbol Definitions

NAME	LOGIC SYMBOL	DESCRIPTION
12-Bit Binary Counter		The 12-bit counter advances on the negative edge of the clock input (CP). A HIGH on the master reset input (MR) clears all counter stages and forces all outputs (Q0-Q11) LOW which is independent of the clock input.
J-K Master-Slave Flip-Flop	 TRUTH TABLE LS73	Applying a LOW to clear input (CLR) resets the flip-flop with Q LOW and $\overline{Q}$ HIGH. This method of setting and resetting the flip-flop is independent of the clock (asynchronous). When inputs J and K are both HIGH, Q changes to the opposite logic state at each clock (CLK) pulse. In other words it toggles.

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0

2-4. BLOCK DIAGRAM DESCRIPTION (Figure 2-1)

The Central Processing Unit (CPU) controls the interpretation and execution of software instructions and the memory stores the software information to be used by the CPU. The S4K Memory is 4,096 8-bit words of Random Access Memory (RAM) and the logic used to interface the RAMs is totally synchronous in design, depending solely upon the CPU for the required timing sequences. The S4K block description explains the function of the status and control signals generated by the CPU to condition the memory for a Read/ Write or Refresh Operation.

2-5. CPU TO MEMORY DATA TRANSFER

The S4K memory requires several signals that allow for data transfer to and from memory. Address lines AØ-A15 condition a particular memory location for data transfer. The most significant bits (MSBs), address lines A12-A15, determine which of 16 possible memory boards is to be addressed. The least significant bits (LSBs), address lines AØ-A11, determine the exact address location on that board. The MSBs select the board to be addressed at $\overline{\text{RCS}}$ (RAM Chip Select).

The CPU generates control and status signals which enable a data transfer, and the Ø1 and Ø2 clocks are used to synchronize memory operations. SMEMR (Memory Read) and PDBIN (Data Bus In) outputs from the CPU control the Read Operation, enabling $\overline{\text{ENBL}}$ and STB which control the data bus drivers and latches. MWRITE (Memory Write) enables $\overline{\text{RWE}}$ (RAM Read/Write) LOW, conditioning the memory for a Write Operation. The S4K can be protected (Read-Only) by the front panel protect switch.

2-6. Refresh Circuits

An individual storage unit in a 4K IC stores a certain charge to maintain a logic HIGH or LOW level. To keep this charge, they must be refreshed within a certain period of time.

The 12-stage counter provides the refresh address, and the counter frequency is supplied by the Ø2 clock. Flip-flops A detect when it is time to refresh. Refresh occurs near the end of SM1 (Machine Cycle One) if the computer is running.

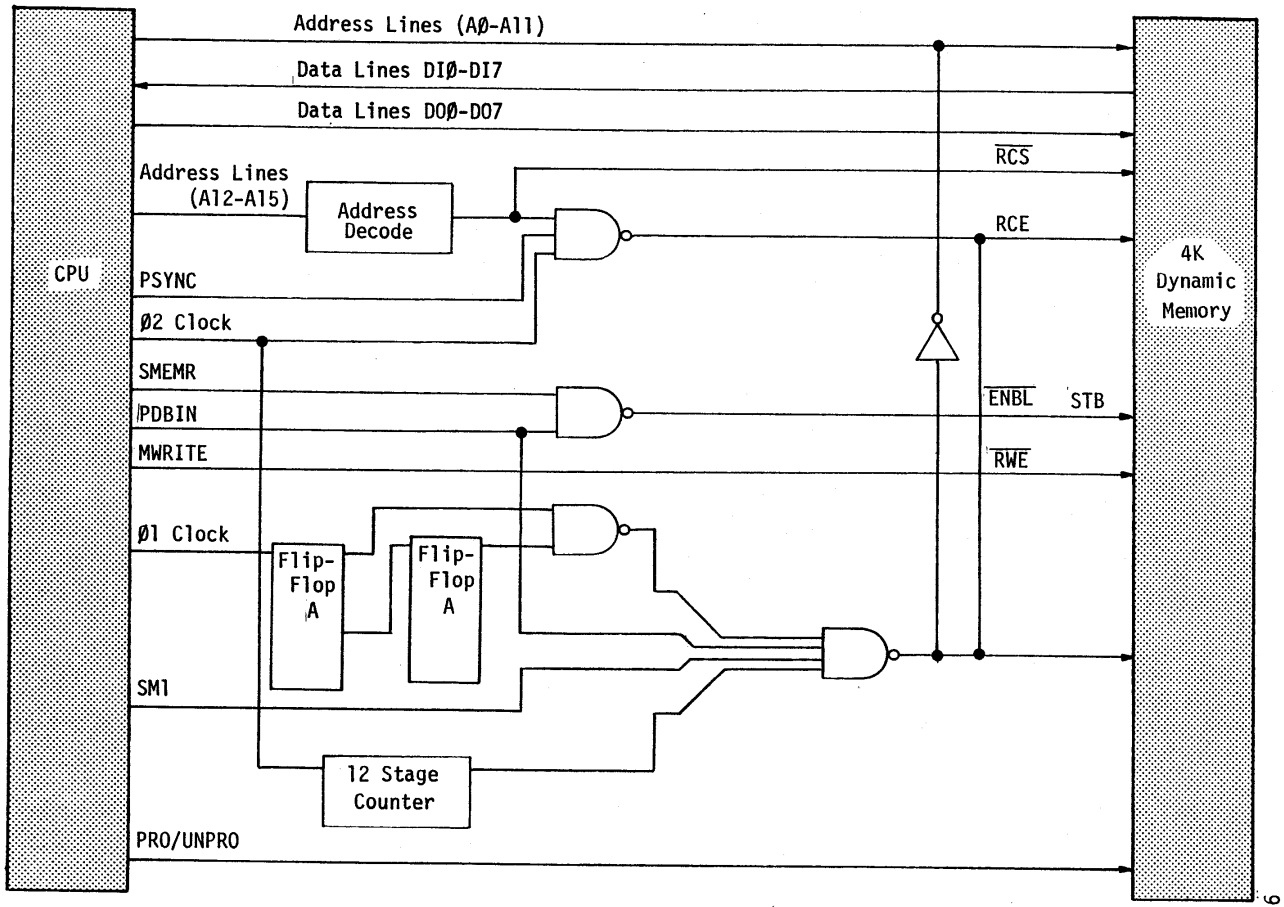


Figure 2-1. 88-S4K Memory Board Block Diagram

2-7. READ/WRITE OPERATIONS (Figure 2-2)

Refer to section C & D of sheet 2 of the schematic. Read and Write Cycles begin identically. The board is selected by the upper 4 address lines, A12-A15 (sheet 2, zone D8). These lines are decoded through SW-1 (zone D7), the board select switch. The 16 possible combinations of the four switches select the board at one of 16 starting locations. The remaining address lines (AØ-A11) are inverted and fed directly to the RAMs to select one of the 4,096 locations on that board. When the incoming address (A12-A15) matches the board address, V6 (zone D7) goes LOW. This forces $\overline{\text{RCS}}$ (RAM Chip Select) LOW to select the RAMs, and H8 (zone D6), G2 (zone D5), and M5 (zone D4) HIGH. When PSYNC goes HIGH and Ø2 LOW (zone C8), G toggles, forcing B11 (zone D5), M11 (zone D5), and J1 (zone C5) HIGH. B11 forces H2 (zone D4) LOW, B6 (zone D4) HIGH and C2 and C12 (zone D3) LOW. This LOW at the input of the level-shift circuit (Q1, R4, R5, and C2, zone D3) produces a very fast transition from 0 volts to +12 volts at C4 and C10 (zone D3). R8 (zone D2) is used to suppress overshoot and undershoot. This RCE signal (zone D1) is the RAM Chip Enable pulse. The RCE pulse width is determined by PSYNC, Ø1 (zone C8) and A (zone C5) and A (zone C4). At the beginning of each cycle, PSYNC clears flip-flops A. Once PSYNC has returned LOW, Ø1 begins clocking A (zone C5). Ø1 toggles A (zone C5) to the set condition, which toggles A (zone C4) to set condition. This state is defined only during Refresh (to be discussed in Section 2-11). The second Ø1 clock pulse toggles A (zone C5, but not A, zone C4) to the reset condition. This forces J11 (zone C4) LOW, B8 (zone C3) HIGH and H12 (zone C2) LOW to clear G (zone D5). Clearing G forces the RCE pulse back LOW to end the Read/Write Cycle.

2-8. READING DATA FROM MEMORY (Figure 2-2)

In order to view the data at a location during front panel operation, the data must be latched because it is only valid when the chip select pulse is present. A CPU Read Operation takes SMEMR (Read Memory) and, shortly afterwards, PDBIN (Data Bus In) HIGH. These signals are fed to gates M8 and M6 (zone D4). M5 and M11 (zone D4) are HIGH as described in the Read/Write Operation. M8 going LOW forces CC10 HIGH to force STB (zone D1) HIGH. This is the strobe pulse that latches the data from the RAMs into the 4-bit latches, FF and GG (sheet 1, zone B3). Data is latched on the falling edge of the STB pulse, which is essentially the falling edge of PDBIN. M6 going LOW enables the data buffers, JJ and HH ($\overline{\text{ENBL}}$), giving the memory board (sheet 1, zone B2) control of the data on the bus (DIØ-DI7).

Therefore, to read data, the RAMs require a valid address, a LOW at $\overline{\text{RCS}}$ (sheet 2, zone D1), a HIGH (+12 volts) at RCE (zone D1), and a HIGH at $\overline{\text{RWE}}$ (zone C1). $\overline{\text{RWE}}$ (RAM Read/Write) is LOW only during a Write Operation.

2-9. WRITING DATA INTO MEMORY (Figure 2-2)

During a Write Cycle, SMEMR and PDBIN are LOW so that the STB and $\overline{\text{ENBL}}$ pulses remain inactive. The CPU output data bus (DOØ-DO7, sheet 1, zone C1) is inverted through CC and DD (zone C2) and fed into the RAM data input lines. The data lines are inverted within the RAMs. During a Write Cycle, MWRITE (sheet 2, zone D8) goes HIGH forcing U2 (zone D8) LOW and K12 (zone D7) and J2 (zone C5) HIGH (as described in Read/Write Operation) forcing J3 LOW and N6 and N12 HIGH. If the board is unprotected (to be discussed in section 2-10), D1 will be HIGH. Thus, N11 (zone C4) will go LOW forcing $\overline{\text{RWE}}$ LOW to enable a RAM Data Write Cycle.

2-10. PROTECT CIRCUITS (Figure 2-2)

When the board is selected, D6 and D8 (sheet 2, zone C6) are LOW. When the PRO (Protect) signal goes HIGH, it is inverted LOW at D9 (zone C6). D10 and D2 (zone C5) go HIGH to force D1 (zone C4) LOW, disabling N13 (zone C4). N11 (zone D4) will never go LOW and a Write will never occur. Gates D1 and D12 (zone C4) are connected in a flip-flop mode. D1 also forces HH11 (zone C4) LOW to turn on the front panel protect indicator. R7-C4 and R10-C6 (zone C5) are integrators that reduce switch bounce. UNPRO (Unprotect) does the opposite of protect. $\overline{\text{POC}}$ (Power On Clear) is gated to D13 (zone C4) through U8, T3 (zone C7) and Diode D12 (zone C4) to insure that the memory boards are unprotected when power is turned on.

2-11. REFRESH (Figure 2-2)

The RAMs used in the S4K are configured in a 64 x 64 matrix. Address lines A6-A11 (sheet 1, zone D8) select one of 64 columns, and address lines AØ-A5 (sheet 1, zone C8) select one of 64 rows. Selection of a particular column and row accesses an individual memory location or cell. Each cell stores a certain charge to maintain a logic HIGH or LOW level. Selecting a row in a Read Operation restores the charge in each cell in the row. This restoration is referred to as Refresh and there is a finite period of time in which all the rows must be refreshed in order to maintain their charge. Most RAMs require that all 64 rows be accessed at least once every 2 milliseconds. This means that every 32 microseconds (2 milliseconds divided by 64) the next sequential row must be refreshed.

The S4K Refresh circuitry consists of a counter to provide the refresh address and two refresh generators: one for the front panel Stop/Halt Mode and one for the Run Mode.

2-12. REFRESH COUNTER/ADDRESSER (Figure 2-2)

The counter frequency is provided by Ø2 through U6 (sheet 2, zone C8). This 2 megahertz clock is divided by 2 in E6 (zone A7) and fed to the 12-stage CMOS counter, X (zone A6). Every 1 microsecond, X10 is pulled LOW to add one count. The fifth stage of the counter, X3, represents a division by 32, producing a positive pulse approximately once every 32 microseconds. Each stage of the counter is negative-edge triggered, so that a change in the count occurs only when the previous stage clocks LOW. This provides a 16-microsecond window for the 6 counter stages above stage five to change to the next sequential address before stage 5 transitions HIGH for the next Refresh Operation. When stage five (Q5) at X3 is HIGH, W12 (zone A5) goes LOW to toggle E12 (zone A5) HIGH.

2-13. REFRESH OPERATION - RUN MODE (Figure 2-2)

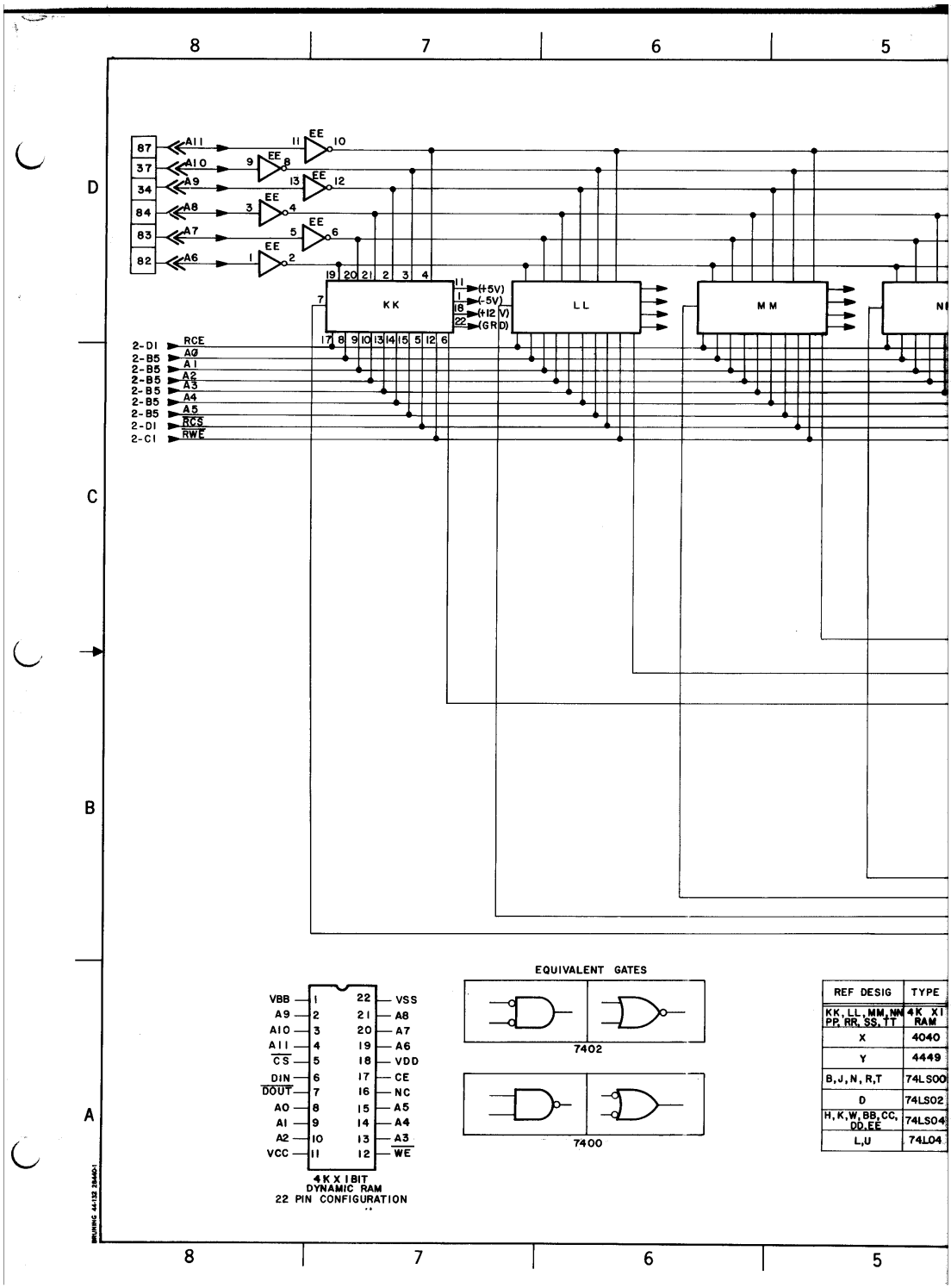
The first machine cycle (SM1) of each instruction is the Instruction Fetch Cycle (see 8800 Theory of Operation). This cycle takes either 4 or 5 states to complete. The first 3 states, T1, T2, and T3 are the instruction fetch and T4 and T5 are used internally by the CPU to decode the instruction. Since M1-T4 is used only by the CPU, it is an ideal time interval to accomplish a Refresh Cycle. Thus, refresh occurs during the first M1-T4 state following the refresh set-up (E12 HIGH).

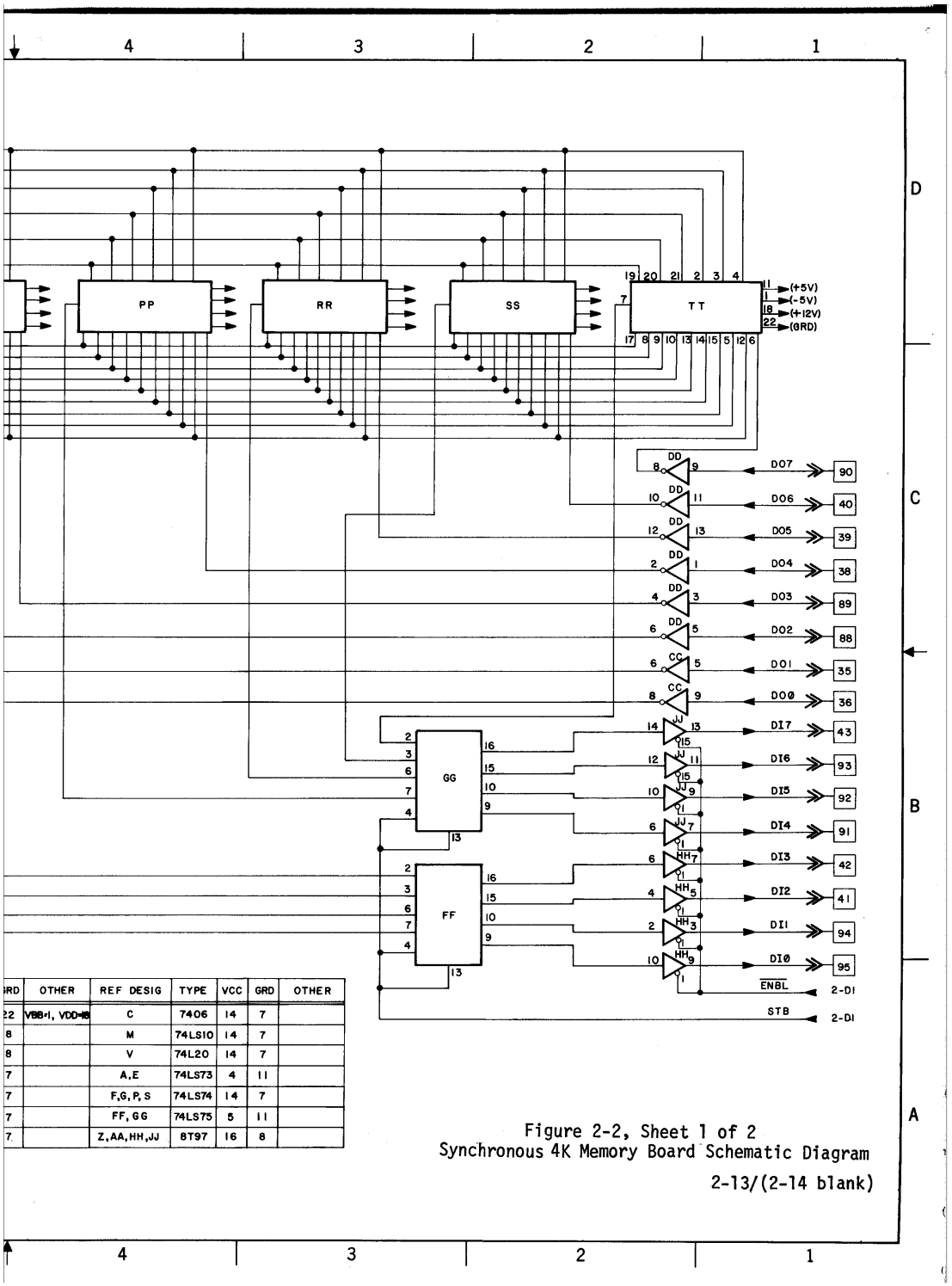
Flip-flops A (zone C5 and zone C4) are used to detect the end of T3 and this signal is gated with M1 and PDBIN to initiate refresh. In the above Read/Write Operations description, it was explained that the second Ø1 pulse after PSYNC cleared G (zone D5) to return RCE back to 0 volts. During a Refresh Cycle, RCE must be cleared earlier in order to set-up the refresh address and again force RCE HIGH for the Refresh Cycle. The first Ø1 clock following PSYNC forces A12 and A9 HIGH. This forces N3 (zone C4) LOW and N8 (zone C4) HIGH. V9 (zone C4) is HIGH if it is an SM1 cycle and V12 is HIGH if it is time to refresh. V10 goes HIGH once PDBIN has returned LOW, enabling V8. The LOW at V8 clears G through B8 (zone C3) and H12 (zone C2) to force $\overline{\text{RCE}}$ back LOW. V8 also forces M12 (zone C3) HIGH, forcing F5 (zone C2) HIGH with the falling edge of clock Ø2. F5 is fed to CC13 (zone B5) where it disables the incoming address by tri-stating AA (zone B7) and enables the refresh address, Z (zone A6). With the rising edge of Ø1, F8 (zone B5) is forced LOW, forcing B6 (zone D4) HIGH to enable the +12 volt level shifter (RCE) (zone D3) as described earlier. F8 (zone C1) also forces R3 HIGH and H6 (zone C2) LOW to clear E12 back LOW. This forces V8 HIGH and M12 (zone C12) LOW. With the falling edge of Ø2, F5 is cleared back LOW and with the rising edge of Ø1, F8 goes back HIGH to force RCE back LOW. This completes the M1-T4 Refresh Cycle.

2-14. REFRESH OPERATION - STOP MODE/HALT MODE

When the computer is in the Stop Mode, it is in the M1-T2 state acknowledging a Wait condition. RUN (zone A8) is LOW forcing R6 and S2 (zone A4) HIGH. When refresh is initiated at E12 (zone A5), S5 (zone A4) goes HIGH and S6 goes LOW. S6 forces P13 (zone A2) LOW to clear P9 (zone A1) LOW. If the board is selected (HH enabled by LOW at $\overline{RCS}$), PRDY goes LOW. It is essential that the PRDY signal remain LOW during this entire cycle to prevent the computer from running before the cycle is over. S6 at $\overline{XCE}$ (zone A1) also forces B11 (zone D5) LOW to allow a normal Read or Write Cycle to perform front panel deposit and examine operations. S5 forces S12 (zone A3) HIGH. On the falling edge of Ø2, S9 and P2 (zone A2) go HIGH. If deposit is active, T6 goes LOW to force $\overline{RWE}$ LOW through N6 and N11 (if protect is inactive). On the leading edge of Ø2, P6 goes LOW to end the Read or Write Cycle and begin the Refresh Cycle. P6 clears S6 at $\overline{XCE}$ back HIGH to force RCE back LOW. P6 forces R3 (zone B2) HIGH and H6 LOW to clear E12 LOW and force M12 (zone C3) HIGH to begin the Refresh Cycle. This sequence is identical to the M1-T4 Refresh except that when F (zone C2) returns back HIGH to end the Refresh Cycle, it clocks P9 back HIGH to force PRDY HIGH. Thus, the only Wait condition that can occur is at initial start-up.

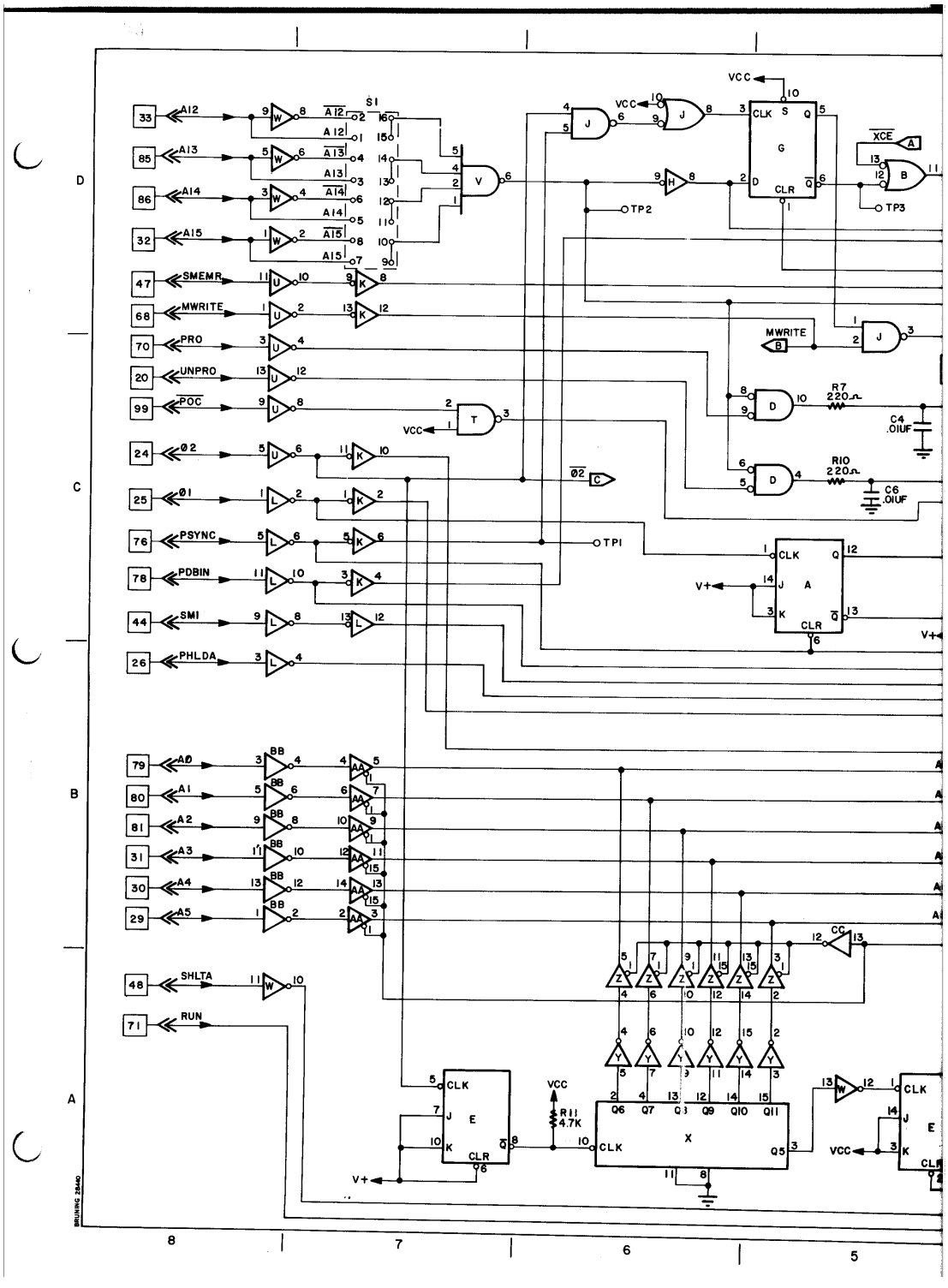
When the computer is in a Halt state, SHLTA forces S2 HIGH and the Refresh Operation is identical to the Stop Mode described above.


8
7
6
5
D
C
B
A
87
37
34
84
83
82
A11
A10
A9
A8
A7
A6
EE
KK
LL
MM
(+5V)
(-5V)
(+12 V)
(GRD)
2-DI RCE
2-B5 A0
2-B5 A1
2-B5 A2
2-B5 A3
2-B5 A4
2-B5 A5
2-DI RCS
2-CI RWE
VBB 1
A9 2
A10 3
A11 4
CS 5
DIN 6
DOUT 7
A0 8
A1 9
A2 10
VCC 11
22 VSS
21 A8
20 A7
19 A6
18 VDD
17 CE
16 NC
15 A5
14 A4
13 A3
12 WE
4K X 1BIT
DYNAMIC RAM
22 PIN CONFIGURATION
EQUIVALENT GATES
7402
7400
REF DESIG
TYPE
KK, LL, MM, NN, PP, RR, SS, TT
4K X1 RAM
X
4040
Y
4449
B,J,N,R,T
74LS00
D
74LS02
H,K,W,BB,CC,DD,EE
74LS04
L,U
74L04



RD	OTHER	REF DESIG	TYPE	VCC	GRD	OTHER
22	VBB=1, VDD=18	C	7406	14	7	
8		M	74LS10	14	7	
8		V	74L20	14	7	
7		A,E	74LS73	4	11	
7		F,G,P,S	74LS74	14	7	
7		FF, GG	74LS75	5	11	
7		Z,AA,HH,JJ	8T97	16	8	

Figure 2-2, Sheet 1 of 2
Synchronous 4K Memory Board Schematic Diagram


33 A12
85 A13
86 A14
32 A15
S1
47 SMEMR
68 MWRITE
70 PRO
20 UNPRO
99 POC
24 Ø2
25 Ø1
76 PSYNC
78 PDBIN
44 SMI
26 PHLDA
79 AØ
80 A1
81 A2
31 A3
30 A4
29 A5
48 SHLTA
71 RUN
VCC
TP1
TP2
TP3
MWRITE
XCE
R7 220
C4 .01UF
R10 220
C6 .01UF
R11 4.7K
V+
CLK
CLR
Q6 Q7 Q3 Q9 Q10 Q11 Q5
D
C
B
A
8
7
6
5

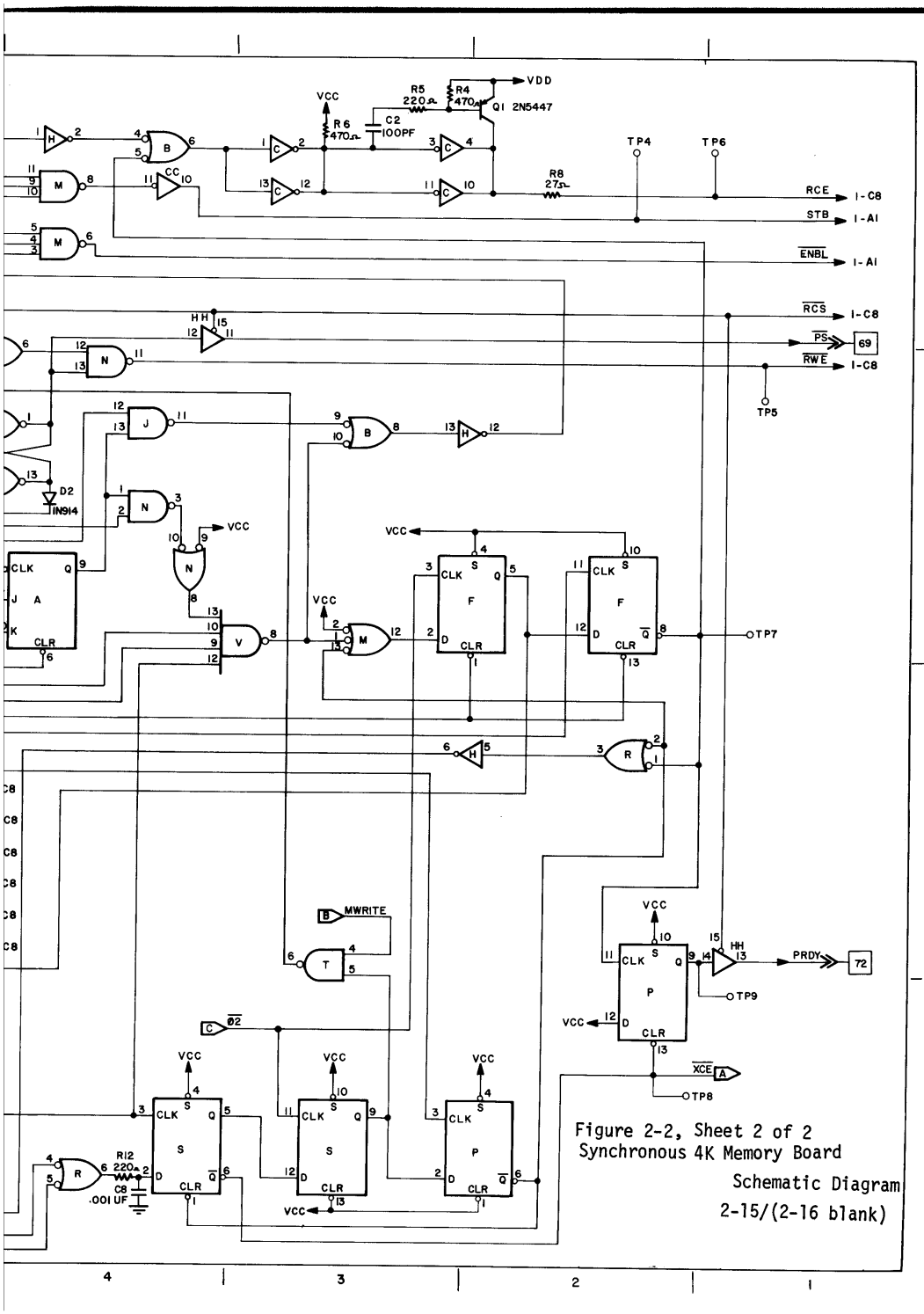
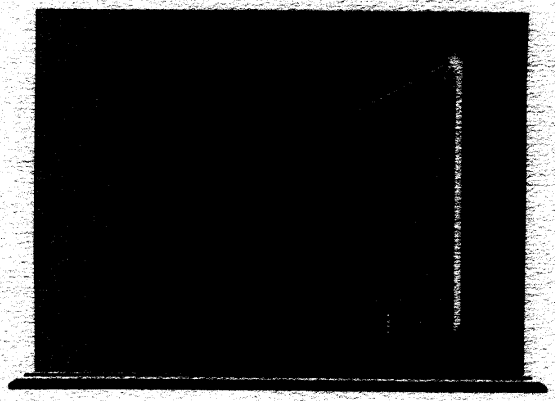


Figure 2-2, Sheet 2 of 2
Synchronous 4K Memory Board
Schematic Diagram

altair 88-S4K

SECTION III



Troubleshooting

3-1. INTRODUCTION TO TROUBLESHOOTING

This section is designed to aid in the location of failures that could be encountered after the 88-S4K Synchronous Memory Board is assembled and installed. It contains a visual inspection check list, a preliminary check to be sure the board is functioning properly, general procedures for troubleshooting TTL Logic, and procedures for troubleshooting specific problems including waveforms of the various test points and a timing diagram to assist in the location of component failure and assembly errors.

3-2. VISUAL INSPECTION CHECK LIST

Before an assembled board is installed, it should be checked for possible problems due to improper assembly. An extensive visual check should locate the cause of most malfunctions:

1. Look for leads that have not been soldered.
2. Check for solder bridges.
3. Check for cold solder connections.
4. Examine the PC board carefully for errors such as hair-line opens in lands.
5. Check IC chips for proper pin placement and good socket connections.
6. Examine electrolytic capacitors for proper polarity.
7. Examine diodes for proper polarity.
8. Be sure correct color code is observed on all resistors.

3-3. PRELIMINARY CHECK

After visual inspection and installation of the S4K board, check the address and data lines for shorts and opens. All the preliminary checks are done with the machine on and in the Stop mode. Each of the 16 address switches on the front panel should be in the down position initially and switched to the up position individually while positioning the EXAMINE/EXAMINE NEXT* switch on the front panel to EXAMINE for each address switch setting. Observe that the corresponding LED is on. After all the switches are up, return them individually to the down position, and observe that the adjacent LED is off. If one LED fails during this check,

*If the S4K is being used with the 8800b, the front panel will read EX NEXT.

or if several LEDs fail at the same time, there are possible problems on the S4K board. The board should be removed and a resistance check made on the bus pins corresponding to the address lines showing the incorrect indications. If the resistance reading indicates there is a short or open in the circuit, trace the land from the bus until the problem is isolated.

Data lines are checked in much the same manner. Address switches A0-A7 correspond to data lights D0-D7. These address switches are initially in the down position. Place A0 up and position DEPOSIT/DEPOSIT NEXT* switch on the front panel to DEPOSIT and observe that the D0 LED is on. Place each of the address switches individually HIGH while positioning DEPOSIT/DEPOSIT NEXT switch on the front panel to DEPOSIT NEXT and observe that each corresponding LED comes on. Return all front panel address switches to the LOW position. Position EXAMINE/EXAMINE NEXT switch on the front panel to EXAMINE to recall data stored in the first address. Repeatedly place EXAMINE/EXAMINE NEXT switch on front panel to EXAMINE NEXT. This will enable the machine to read the data that was stored in the successive memory locations to verify data was deposited.

If one LED fails during this check, or if more than one LED fails at the same time, there is a possible problem on the S4K board.

If a major malfunction is discovered, refer to Paragraphs 3-4 and 3-5 for general procedures for troubleshooting TTL logic and assistance in locating specific problems.

*If the S4K is being used with the 8800b, the front panel will read DEP NEXT.

3-4. GENERAL PROCEDURES FOR TROUBLESHOOTING TTL LOGIC

1. High level = logic 1 = 2 volts - 5 volts
   Low level = logic 0 = .8 volts - (-.5 volts)
2. Always work backward through the logic from the trouble area.
3. Always disconnect power when removing or installing ICs or cutting or resoldering PC lands.
4. When a gate element appears bad (an output is opposite of what it should be with a given input):
   a. Insure the IC package has correct voltage supplies and grounds.
   b. Re-check the output with the pin open (bend the pin up and re-insert the IC in its socket - if not socketed, cut the land that connects the pin to the external circuitry. If the output remains incorrect, replace the IC with a new part. If the output is now correct, look for shorts in nearby PC lands (visually and with an ohmmeter). If none are found, the probable cause is a defective input at one of the elements that the output feeds. Isolate each input in turn by disconnecting it from the external circuitry.
   c. If an input is between .8 volts and 2 volts, check continuity back to the driving output.

3-5. TROUBLESHOOTING SPECIFIC PROBLEMS

The first step in troubleshooting is identifying the problem. Schematic diagrams (Figure 2-2), waveforms (Figures 3-1 through 3-8) and timing diagram (Figure 3-9) should be used in isolating components or assembly errors that are possibly causing problems in the circuit.

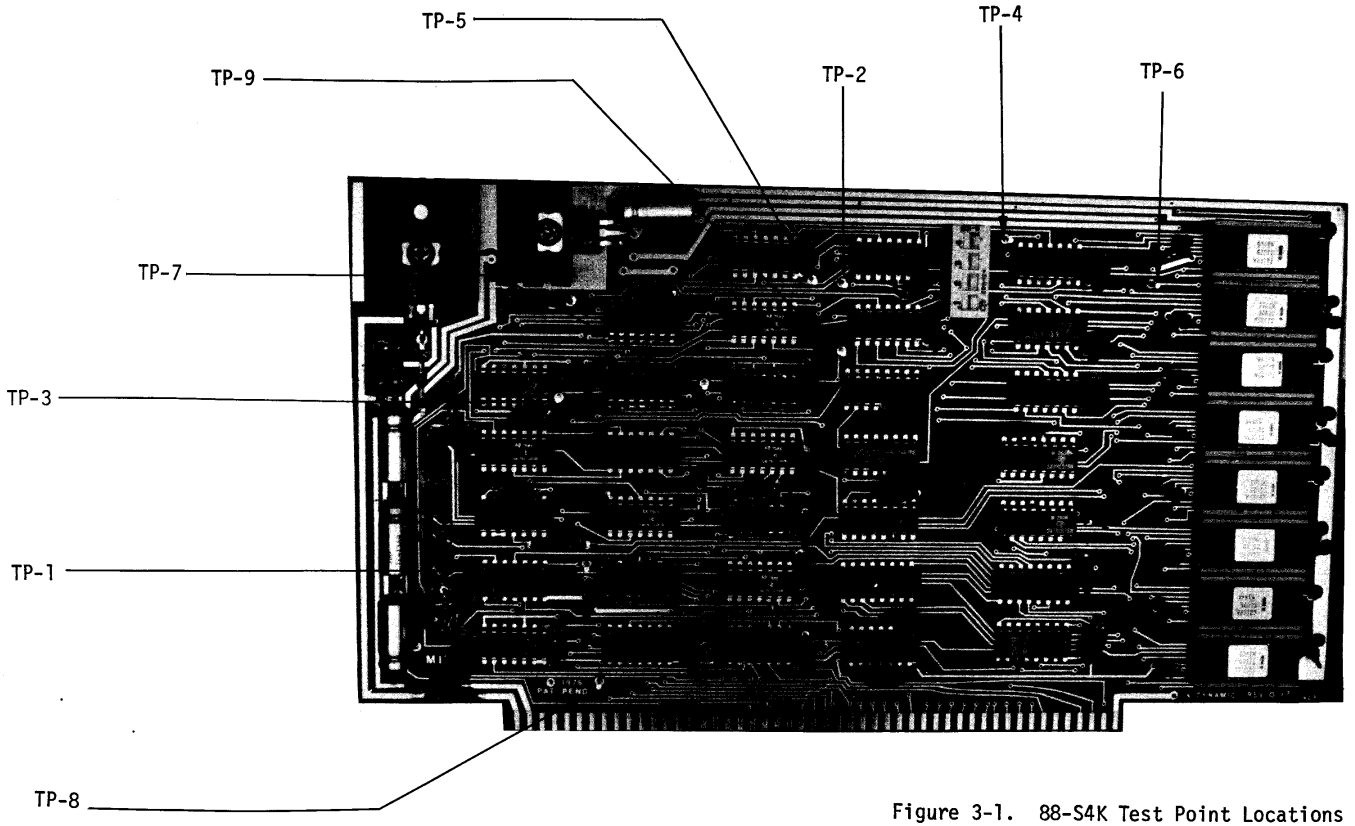
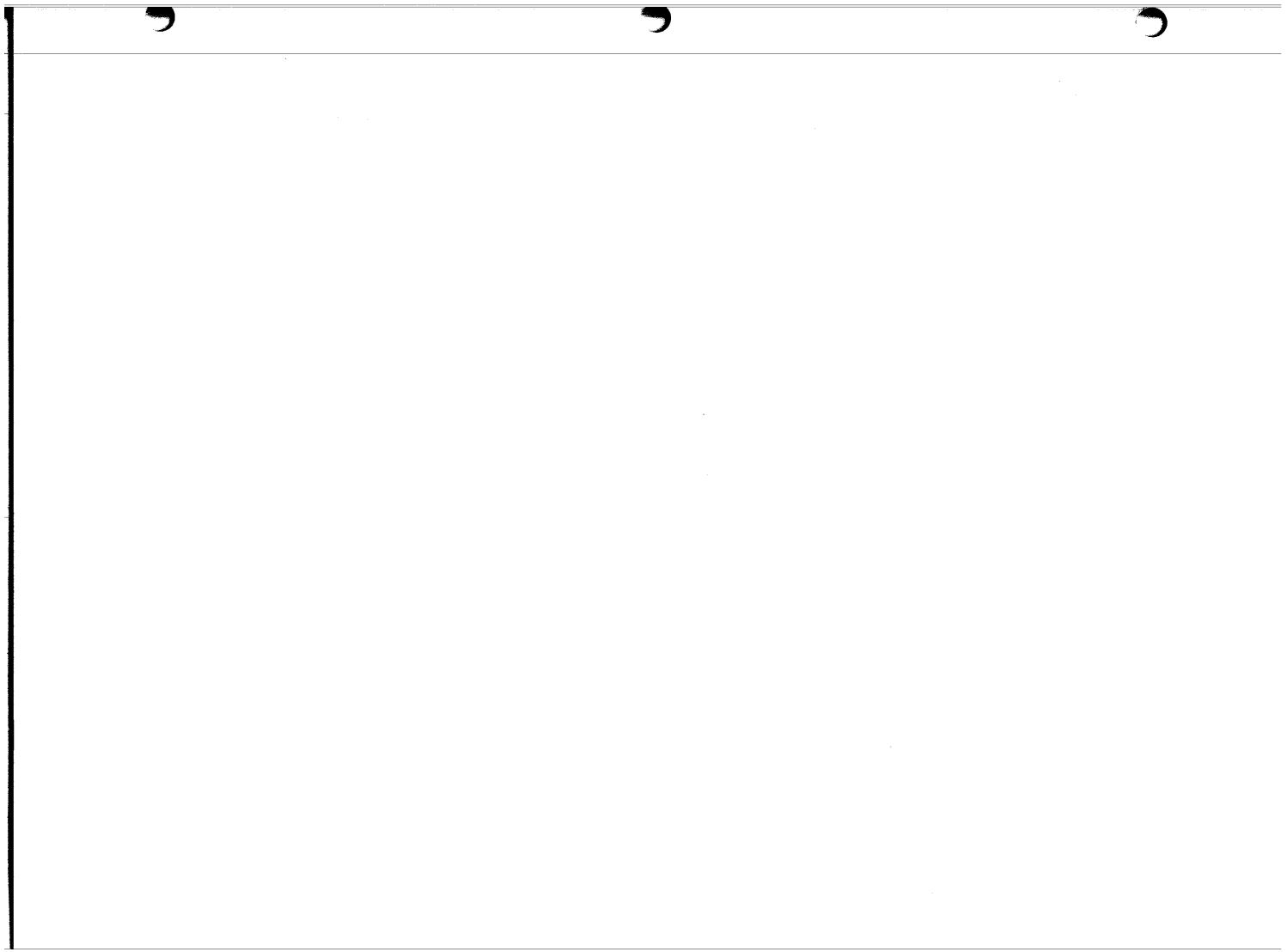


Figure 3-1. 88-S4K Test Point Locations



TP-3
2 V/CM
.5 uS/CM

TP-4
2 V/CM
.5 uS/CM

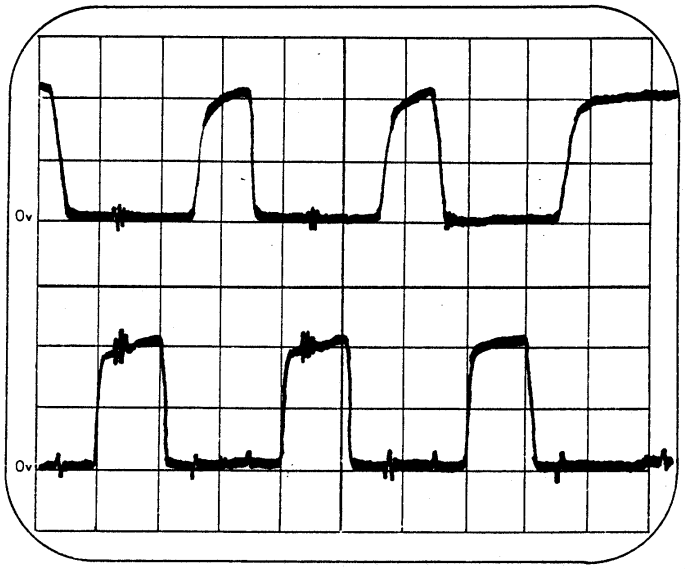


Figure 3-2. Waveforms for Test Points 3 and 4

TP-5
2 V/CM
1 us/CM

TP-1
2 V/CM
1 uS/CM

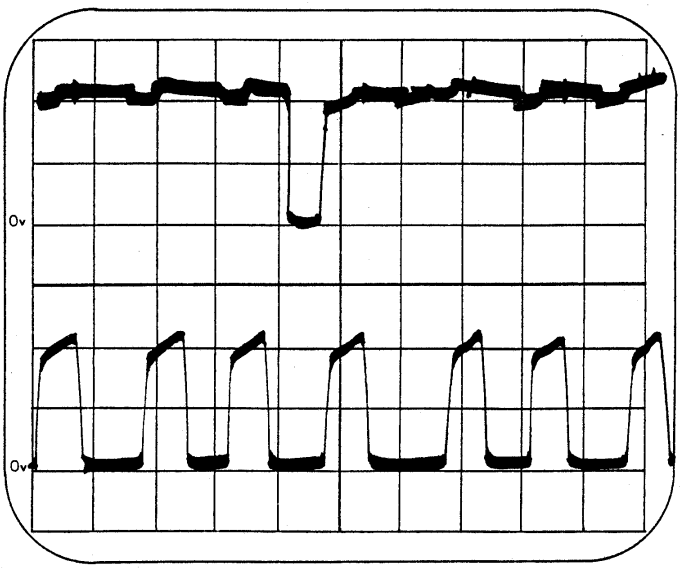


Figure 3-3. Waveforms for Test Points 5 and 1

TP-8
2 V/CM
200 NS/CM

TP-6
5 V/CM
200 NS/CM

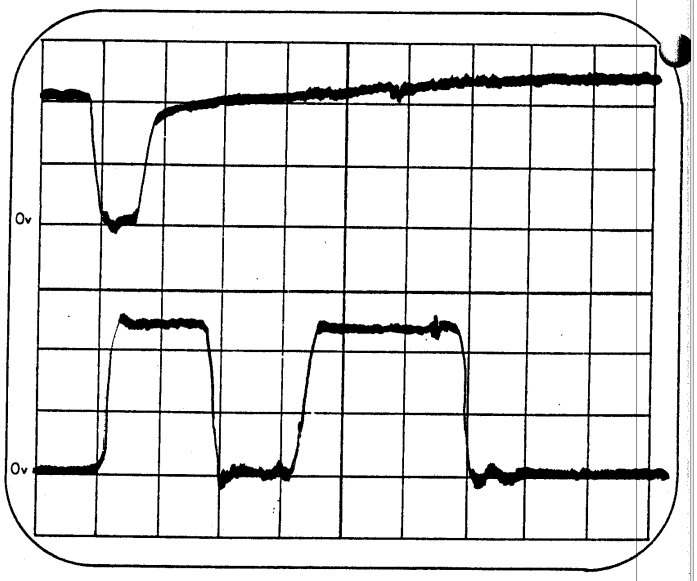


Figure 3-4. Waveforms for Test Points 8 and 6

TP-7
2 V/CM
10 uS/CM

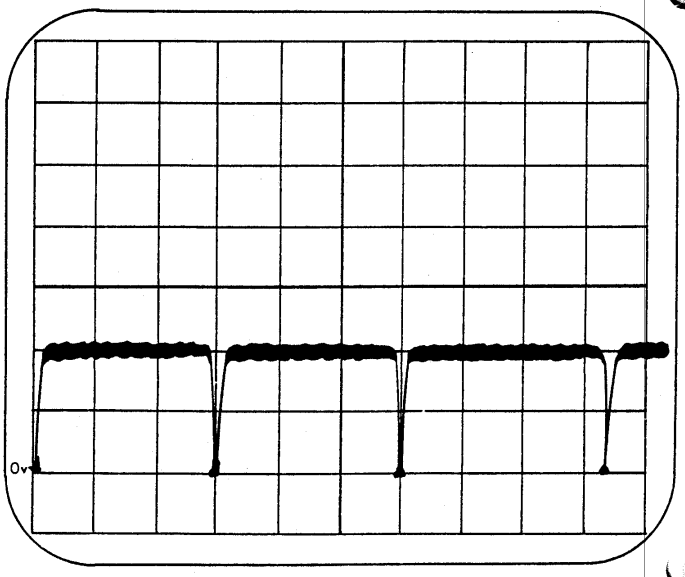


Figure 3-5. Waveform for Test Point 7

TP-6
2 V/CM
.5 uS/CM

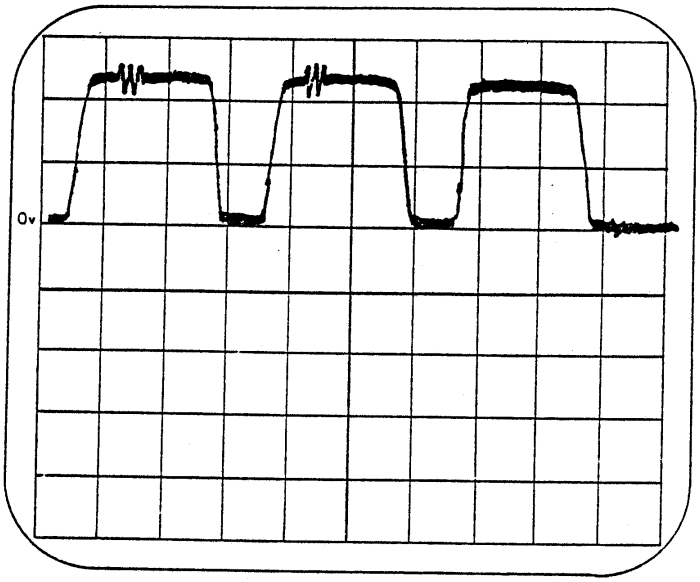


Figure 3-6. Waveform for Test Point 6

TP-9
2 V/CM
.5 µs/CM

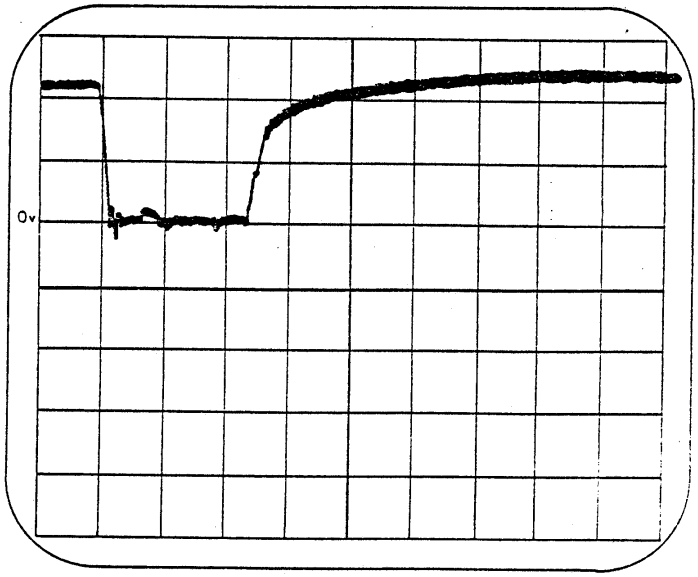


Figure 3-7. Waveform for Test Point 9

TP-6
5 V/CM
.5 uS/CM

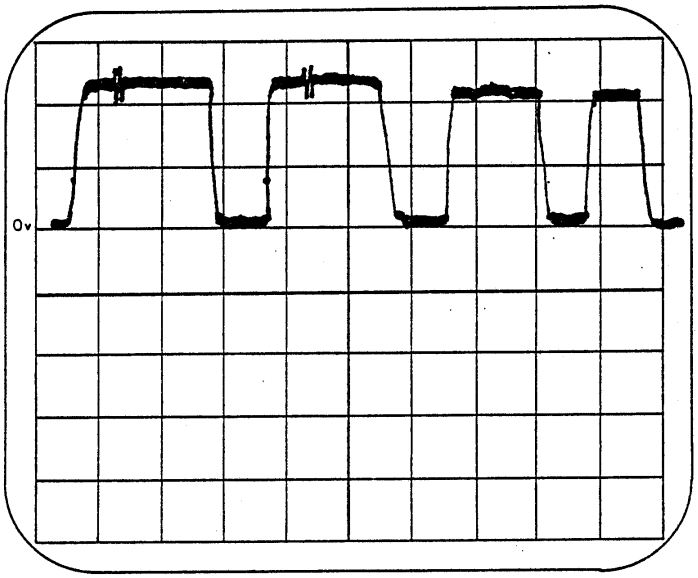


Figure 3-8. Waveform for Test Point 6

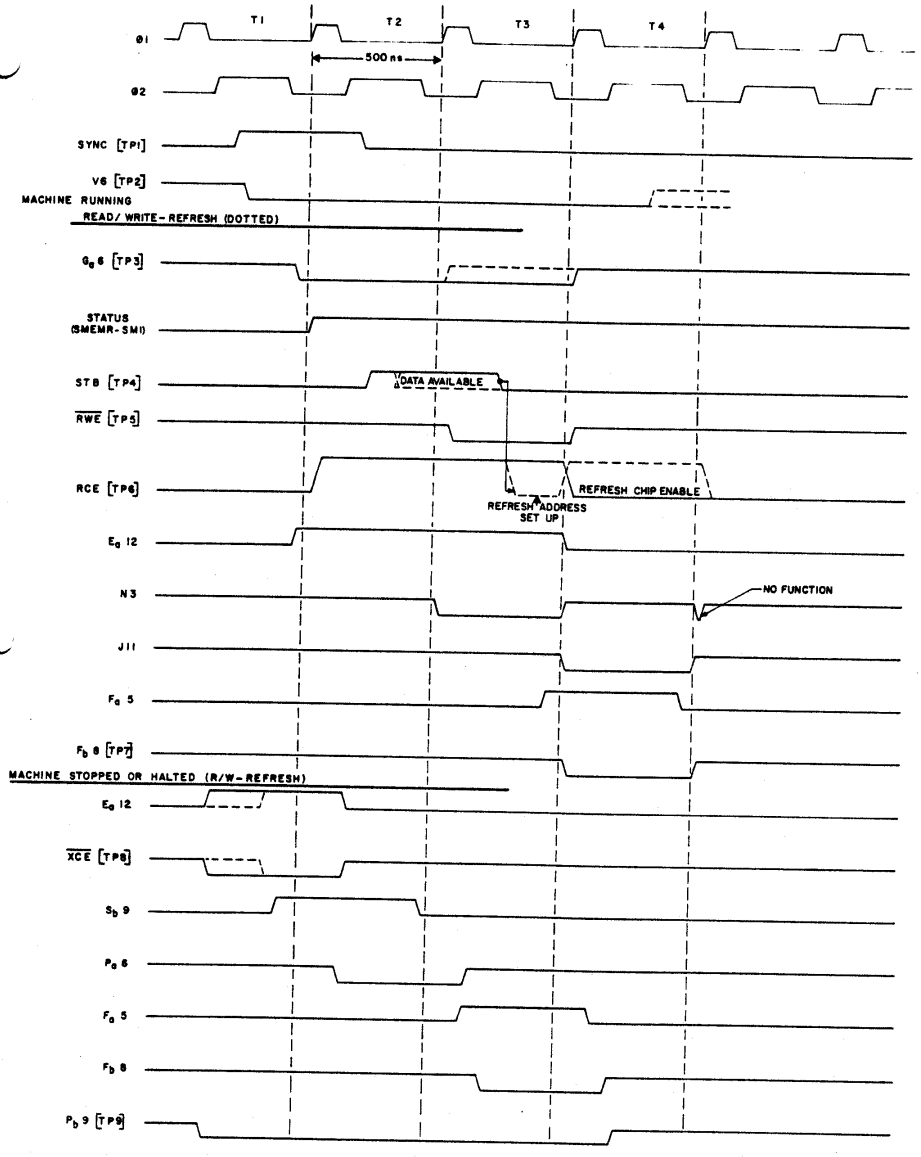


Figure 3-9. 88-S4K Timing Diagram

I. FRONT PANEL MODE

A. Cannot deposit, all data lights on (HIGH).

1. Examine several other locations within the 4K block to insure that this is the symptom.
2. $\overline{\text{ENBL}}$ (sheet 1, zone A1) should be LOW.
3. TP3 should be HIGH. (Refer to Figure 3-2).
4. M9 and M10 (sheet 2, zone D4) should be HIGH.
5. $\overline{\text{RCS}}$ (sheet 1, zone C8) should be LOW.

B. Cannot deposit, data lights are random.

1. Insure that the board is unprotected.
2. N4 (sheet 2, zone C5) should be HIGH.
3. N13 (sheet 2, zone C4) should be HIGH.
4. $\overline{\text{RCS}}$ (sheet 1, zone C8) should be LOW.
5. TP5 should appear as in Figure 3-3.

NOTE: Low-going pulse on TP5 appears only when S9 (sheet 2, zone A3) is HIGH due to activation of Front Panel DEPOSIT switch.

6. TP6 should appear as in Figure 3-4.

NOTE: The 2 pulses on TP6 occur once every 32 microseconds.

C. Deposits correctly, but data lost when location re-examined.

1. TP5 (sheet 2, zone B3) is HIGH except when MWRITE is Active (HIGH).
2. TP6 appears as in Figure 3-4.
3. CC13 (sheet 2, zone B5) goes HIGH and CC12 LOW, when F5 (zone C2) is HIGH (refer to Timing Diagram, Figure 3-9).
4. E12 (zone A5) should be pulsing every 32 microseconds.
5. X10 (zone A6) should be pulsing every 1 microsecond.
6. Insure address inputs at the RAMs are the inverse of the address switches.
   (Example: switch A10 HIGH, RAM pins 3 are LOW.)

D. One data light remains HIGH or LOW during deposit.

1. Check output at FF and GG. Work backwards to RAM output, then RAM input, etc. (Note that the RAM outputs are enabled only with the first pulse of each double pulse occurring 32 microseconds)

II. RUN MODE

Deposit the programs listed below into memory and check for proper operation in the RUN MODE. If there is a problem, check the test points indicated and follow the general procedures for troubleshooting TTL logic.

A. Read

1. Enter the following program in memory.

   NOTE: Locations and instructions are in octal.

Location	Instruction
000000	303
000001	000
000002	000

   Single step 3 times and the computer should jump back to location 0.

2. Activate RUN switch. Only address lights A0 and A1 should be lit. If they are, proceed to section II.

3. With machine running, trigger scope on TP2 falling edge and observe test points TP3 (zone D5, Figure 3-2), TP4 (zone D2, Figure 3-2), or TP6 (zone D2, Figure 3-6). Set the scope to .5 microseconds/division.

   NOTE: Each time TP2 goes LOW, the board is being accessed.

4. Trigger scope on M12 (zone C3) going HIGH and observe TP7 (zone C1, Figure 3-5). Set the scope at 10 microseconds/division.

   NOTE: Negative going pulses should be approximately .5 microseconds, occurring every 32 microseconds.

5. Set the scope at .5 microseconds/division and observe TP6 (zone D2, Figure 3-8), TP8 (zone A2, Figure 3-4), and TP9 (zone A1, Figure 3-7).

B. WRITE

1. Enter and run the program below:

Location	Instruction
0 0 0 0 0 0	0 7 6
0 0 0 0 0 1	2 5 2
0 0 0 0 0 2	0 6 2
0 0 0 0 0 3	0 4 0
0 0 0 0 0 4	0 0 0
0 0 0 0 0 5	3 0 3
0 0 0 0 0 6	0 0 2
0 0 0 0 0 7	0 0 0

This program loads the accumulator with a 252 (alternating bit pattern) and stores it at location 040. Each time the computer stores location 040, a .5 microsecond, negative pulse should occur at TP5. If only one bit appears to be bad, trigger the scope on the falling edge of TP5 and observe the particular data bit from the latch output back through the RAMs until the source of the problem is found. If a defective RAM is suspected, check all of the RAM pins for proper voltage levels.

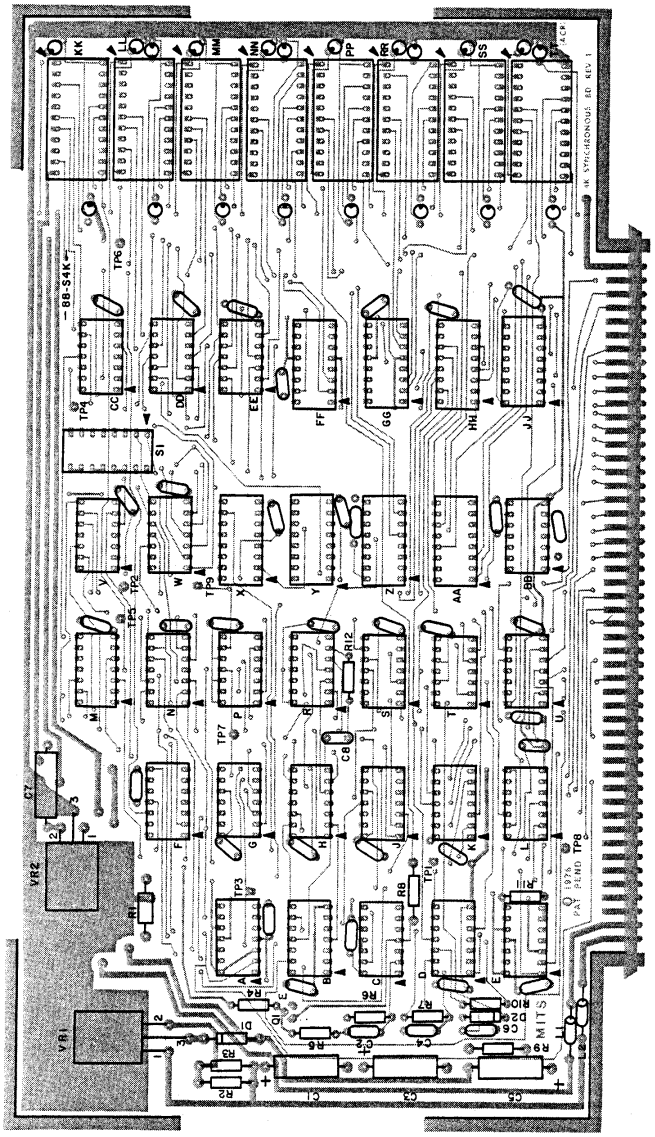


Figure 3-10. Synchronous 4K Memory Board (Top View)

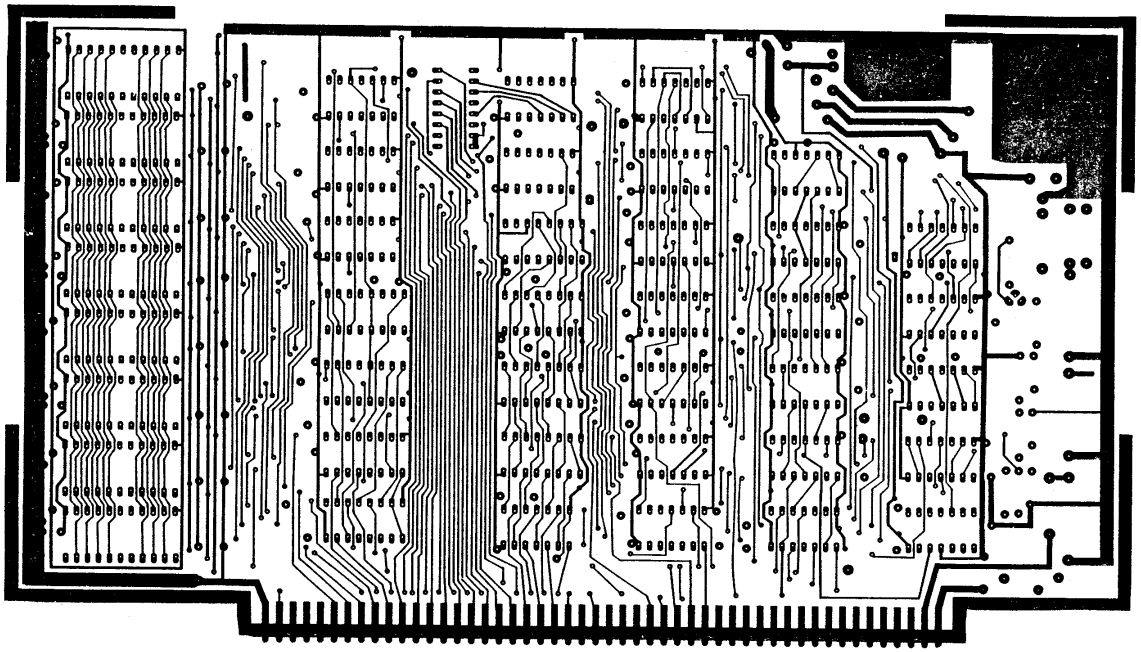
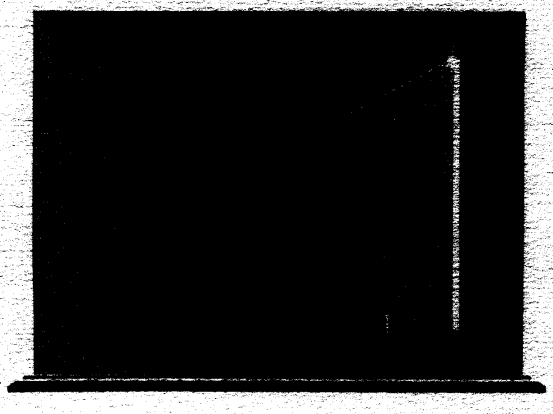


Figure 3-11. Synchronous 4K Memory Board (Bottom View)

altair 88-S4K

SECTION IV



Assembly

SECTION IV

ASSEMBLY

4-1. GENERAL

This section contains all the information needed for the circuit construction of the Altair 88-S4K Synchronous 4K Memory Board. It consists of helpful assembly hints and detailed instructions of component installation on the 88-S4K Memory Board.

4-2. ASSEMBLY HINTS

Before beginning the construction of your unit, it is important that you read the "MITS Kits Assembly Hints" booklet included with your kit. Pay particular attention to the section on soldering, because most problems occur as the result of poor soldering. It is essential that you use the correct type of soldering iron. A 25-30 watt iron with a chisel tip (such as an Ungar 776 with a 7155 tip) is recommended in the assembly hints booklet.

> NOTE
>
> Some important warnings are also included in the hints booklet. Read them carefully before you begin work on your unit -- failure to heed these warnings could cause you to void your warranty.

Check the contents of your kit against the appendix in this manual (Parts List) to make sure you have all the required components, hardware, and parts. The components are in plastic envelopes; do not open them until you need the components for an assembly step. You will need the tools called for in the "Kits Assembly Hints" booklet.

As you construct your kit, follow the instructions in the order they are presented in the assembly manual. Always complete each section before going on the next. Two organizational aids are provided throughout the manual to assist you: 1) Boxed off parts identification lists, with spaces provided to check off the components as they are installed; 2) reproductions of the silkscreens showing previously installed components, components being installed, and components yet to be installed (Figure 4-1).

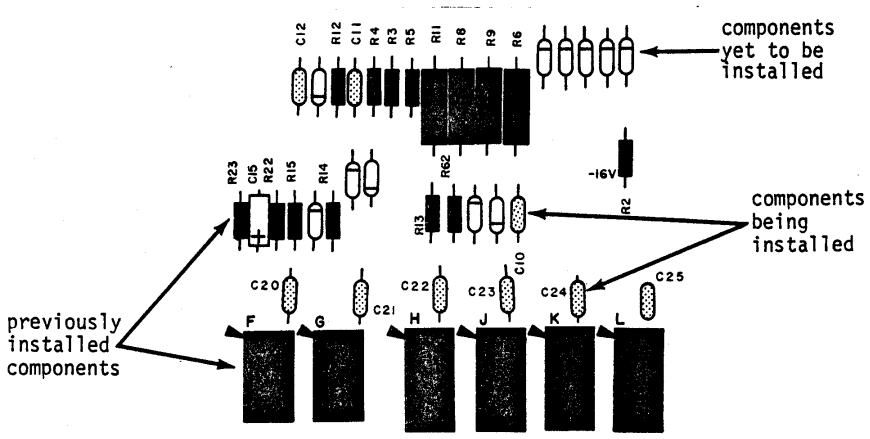


Figure 4-1. Typical Silkscreen

4-3. COMPONENT INSTALLATION INSTRUCTIONS

The following component installation instructions describe the proper procedures for installing various types of components in your kit. Read these instructions over very carefully and refer back to them whenever necessary. Failure to properly install components may cause permanent damage to the component or the rest of the unit; it will definitely void your warranty. More specific instructions, or procedures of a less general nature, will be included within the assembly text itself.

Under no circumstances should you proceed with an assembly step without fully understanding the procedures involved. A little patience at this stage will save a great deal of time and potential "headaches" later.

4-4. DIODE INSTALLATION INSTRUCTIONS

NOTE: Diodes are marked with a band on one end indicating the cathode end. Each diode must be installed so that the end with the band is oriented towards the band printed on the PC board. Failure to orient the diodes correctly may result in permanent damage to your unit.

DIODE

Use the following procedure to install diodes onto the board. Refer to the list of Diode Part Numbers included for each board to make sure you install the correct diode each time.

1. Bend the leads of the diode at right angles to match their respective holes on the board.

2. Insert the diode into the correct holes on the silk screen, making sure the cathode end is properly oriented. Turn the board over and bend the leads slightly outward.

3. Solder the two leads to the foil pattern on the back side of the board; then clip off any excess lead lengths.

4-5. TRANSISTOR INSTALLATION INSTRUCTIONS

To install transistors, use the following instructions.

NOTE: Always check the part number of each transistor before you install it. (See listing of Transistor Part Numbers for each board.) Some transistors look identical but differ in electrical characteristics, according to part number. If you have received substitute part numbers for the transistors in your kit, check the Transistor Identification Chart which follows these instructions to be sure you make the correct substitutions.

NOTE: Always make sure the transistor is oriented so that the emitter lead is installed in the hole on the PC board labeled with an "E". To determine which lead is the emitter lead, refer to the Transistor Identification Chart.

1. After the correct transistor has been selected and the leads have been properly oriented, insert the transistor into the holes on the silk-screened side of the board.

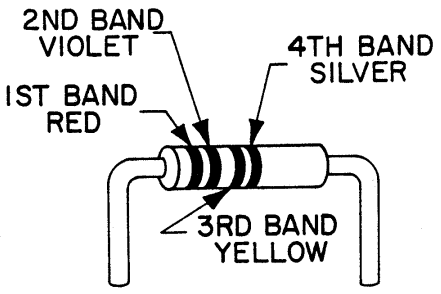
2. Holding the transistor in place, turn the board over and bend the three leads slightly outward.

3. Solder the leads to the foil pattern on the back side of the board; then clip off any excess lead lenghts.

4-6. RESISTOR INSTALLATION INSTRUCTIONS

Resistors have four (or possibly five) color-coded bands as represented in the chart below. The fourth band is gold or silver and indicates the tolerance. NOTE: In assembling a MITS kit, you need only be concerned with the three bands of color to the one side of the gold or silver (tolerance) band. These three bands denote the resistor's value in ohms. The first two bands correspond to the first two digits of the resistor's value and the third band represents a multiplier.

For example: a resistor with red, violet, yellow and silver bands has a value of 270,000 ohms and a tolerance of 10%. By looking at the chart below, you see that red is 2 and violet 7. By multiplying 27 by the yellow multiplier band (10,000), you find you have a 270,000 ohm (270K) resistor. The silver band denotes the 10% tolerance. Use this process to choose the correct resistor called for in the manual.



RESISTOR COLOR CODES		
COLOR	BANDS 1&2	3rd BAND (Multiplier)
Black	0	10^0
Brown	1	10^1
Red	2	10^2
Orange	3	10^3
Yellow	4	10^4
Green	5	10^5
Blue	6	10^6
Violet	7	10^7
Gray	8	10^8
White	9	10^9

Use the following procedure to install the resistors onto the boards. Make sure the colored bands on each resistor match the colors called for in the list of Resistor Values and Color Codes given in the assembly instructions.

1. Using needle-nose pliers, bend the leads of the resistor at right angles to match their respective holes on the PC board.

2. Install the resistor into the correct holes on the silk-screened side of the PC board.

3. Holding the resistor in place with one hand, turn the board over and bend the two leads slightly outward.

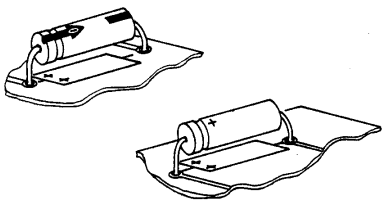
4. Solder the leads to the foil pattern on the back side of the board; then clip off any excess lead lengths.

4-7. CAPACITOR INSTALLATION INSTRUCTIONS

A. Electrolytic Capacitors

Polarity must be noted on electrolytic capacitors before they are installed.

The electrolytic capacitors contained in your kit may have one or possibly two of three types of polarity markings. To determine the correct orientation, look for the following.



ELECTROLYTIC CAPACITOR

One type will have plus (+) signs on the positive end; another will have a band or a groove around the positive side in addition to the plus signs. The third type will have an arrow on it; in the tip of the arrow there will be a negative (-) sign. The capacitor must be oriented so the arrow points to the negative side.

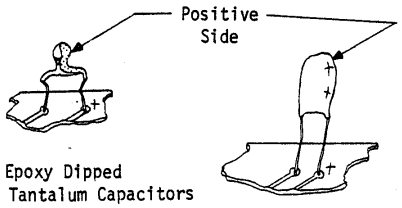
Install the electrolytic capacitors using the following procedure. Make sure you have the correct capacitor value before installing each one.

1. Bend the two leads of the capacitor at right angles to conform to their respective holes on the board. Insert the capacitor into the holes on the silk-screened side of the board, aligning the positive side with the "+" signs printed on the board.
2. Holding the capacitor in place, turn the board over and bend the two leads slightly outward. Solder the leads to the foil (bottom) side of the board and, clip off any excess lead lengths.

B. Epoxy Dipped Tantalum, Epoxy Dipped Ceramic, and Ceramic Disk Capacitors

Polarity must be noted on epoxy dipped tantalum capacitors before they are installed.

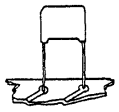
There are two types of epoxy dipped tantalum capacitors contained in you your kit. The first type is blue on the positive side. The second type is marked with "+" signs on the positive side. Both types of epoxy dipped tantalum capacitors are shown in the drawings below.



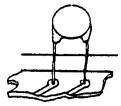
Epoxy Dipped Tantalum Capacitors

The epoxy dipped ceramic capacitors and the ceramic disk capacitors are non-polarized.

These two types of capacitors are shown in the drawings below.



Epoxy Dipped Ceramic Capacitor



Ceramic Disk Capacitor

Install these 4 types of capacitors using the following procedure. Make sure you have the correct capacitor value before installing each one.

1. Bend the two capacitor leads to conform to their respective holes on the board.
2. Insert the capacitor into the correct holes from the silk-screened side of the board. Holding the capacitor in place, turn the board over and bend the two leads slightly outward.
3. Solder the two leads to the foil (bottom) side of the board and, clip off any excess lead lengths.

4-8. IC INSTALLATION INSTRUCTIONS

All ICs must be oriented so that the notched end is toward the end with the arrowhead printed on the PC board. Pin 1 of the IC should correspond with the pad marked with the arrowhead. If the IC does not have a notch on one end, refer to the IC Identification Chart to identify Pin 1.

To prepare ICs for installation:
All ICs are damaged easily and should be handled carefully -- especially static-sensitive MOS ICs. Always try to hold the IC by the ends, touching the pins as little as possible. When you remove the IC from its holder, CAREFULLY straighten any bent pins using needle-nose pliers. All pins should be evenly spaced and should be aligned in a straight line, perpendicular to the body of the IC itself.

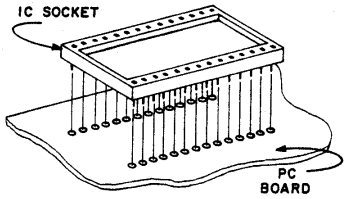
A. Installing ICs without sockets:

1. Orient the IC so that Pin 1 coincides with the arrowhead on the PC board.
2. Align the pins on one side of the IC so that just the tips are inserted into the proper holes on the board.
3. Lower the other side of the IC into place. If the pins don't go into their holes right away, rock the IC back, exerting a little inward pressure, and try again. Be patient. The tip of a small screwdriver may be used to help guide the pins into place. When the tips of all the pins have been started into their holes, push the IC into the board the rest of the way. Tape the IC to the board with a piece of masking tape.
4. Turn the board over and solder each pin to the foil pattern on the back side of the board. Be sure to solder each pin and be careful not to leave any solder bridges. Remove the masking tape.

WARNING:
Make sure none of the pins have been pushed underneath the IC during insertion.

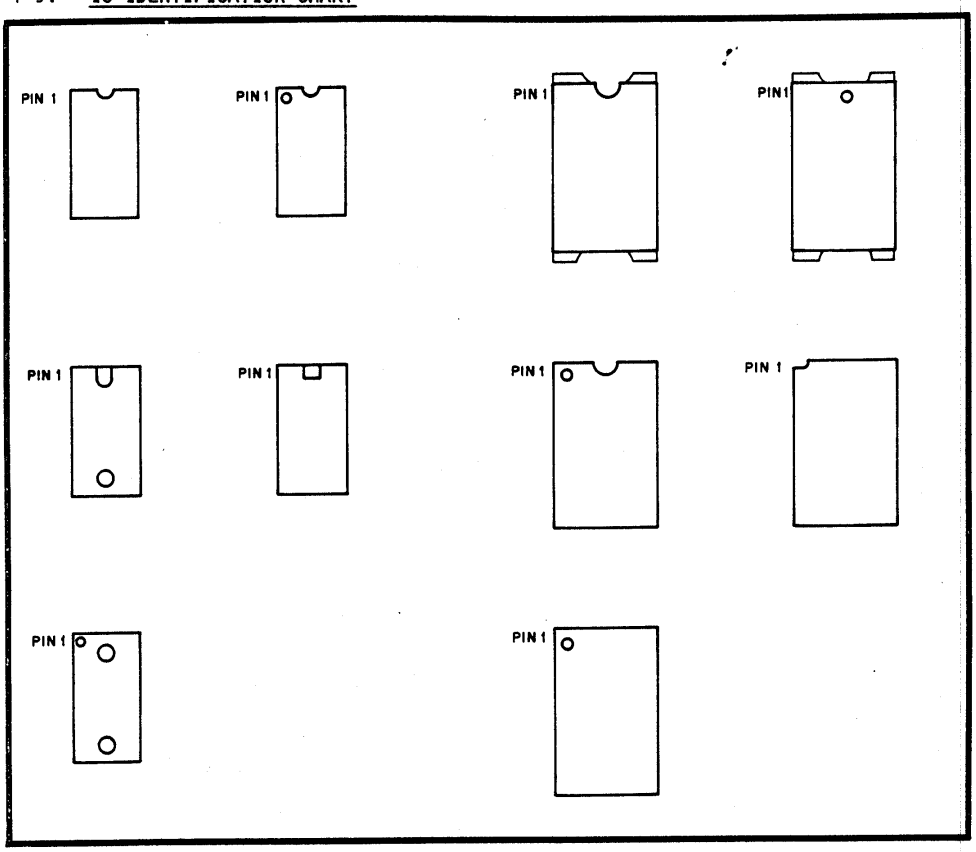
B. Installing ICs with sockets:

1. Referring to the drawing below, set the IC socket into the designated holes on the board and secure it with a piece of masking tape.



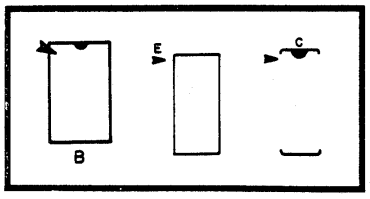
2. Turn the board over and solder each pin to the foil pattern on the back side of the board. Be sure to solder each pin and be careful not to leave any solder bridges. Remove the masking tape.
3. Orient the IC over the socket so that Pin 1 coincides with the arrowhead on the PC board.
4. Align the pins on one side of the socket so that just the tips are inserted into the holes.
5. Lower the other side of the IC into place. If the pins don't go into their holes right away, rock the IC back, exerting a little inward pressure, and try again. Be patient. When the tips of all the pins have been started into their holes, push the IC into the socket the rest of the way.

4-9. IC IDENTIFICATION CHART



INTEGRATED CIRCUITS (IC's) CAN COME WITH ANY ONE OF, OR A COMBINATION OF, SEVERAL DIFFERENT MARKINGS. THESE MARKINGS ARE VERY IMPORTANT IN DETERMINING THE CORRECT ORIENTATION FOR THE IC's WHEN THEY ARE PLACED ON THE PRINTED CIRCUIT BOARDS. REFER TO THE ABOVE DRAWING TO LOCATE PIN 1 OF THE IC's, THEN USE THIS INFORMATION IN CONJUNCTION WITH THE INFORMATION BELOW TO PROPERLY ORIENT EACH IC FOR INSTALLATION.

WARNING: INCORRECTLY ORIENTED IC's MAY CAUSE PERMANENT DAMAGE!



THE DRAWING ON THE LEFT INDICATES VARIOUS METHODS USED TO SHOW THE POSITION OF IC's ON THE PRINTED CIRCUIT BOARDS. THESE ARE SILK-SCREENED DIRECTLY ON THE BOARD. THE ARROWHEAD INDICATES THE POSITION FOR PIN 1 WHEN THE IC IS INSTALLED.

4-10. MOS IC SPECIAL HANDLING INSTRUCTIONS

There are several MOS integrated circuits contained in this kit. These IC's are very sensitive to static electricity and transient voltages. In order to prevent damaging these components, read over the following precautions and adhere to them as closely as possible. FAILURE TO DO SO MAY RESULT IN PERMANENT DAMAGE TO THE IC.

1) All equipment (soldering iron, tools, solder, etc.) should be at the same potential as the PC board, the assembler, the work surface and the IC itself along with its container. This can be accomplished by continuous physical contact with the work surface, the components, and everything else involved in the operation.

2) When handling the IC, develop the habit of first touching the conductive container in which it is stored before touching the IC itself.

3) If the IC has to be moved from one container to another, touch both containers before doing so.

4) Do not wear clothing which will build up static charges. Preferably wear clothing made of cotton rather than wool or synthetic fibers.

5) Always touch the PC board before touching the IC to the board. Try to maintain this contact as much as possible while installing the IC.

6) Handle the IC by the edges. Avoid touching the pins themselves as much as possible.

7) Dry air moving over plastic can result in the development of a significant static charge. Avoid placing the IC near any such area or object.

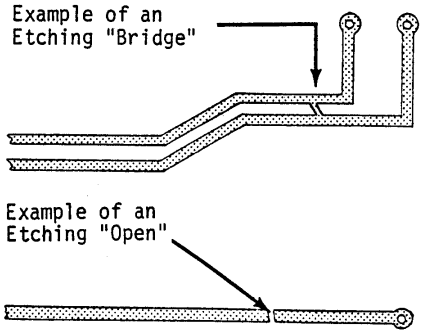
8) In general, never touch anything to the IC that you have not touched first while touching both it and the IC itself.

4.11. 88-S4K Synchronous 4K Memory Board Assembly

After reviewing the theory of operation, the component installation instructions, and the Assembly Hints Manual, construct the 88-S4K Memory Board according to the following instructions.

It is recommended that a visual inspection of the PC Board(s) in your kit be made before beginning the assembly procedures.

Look for etching "bridges" or etching "opens" in the printed circuit lands, as shown in the drawings below:



This could also appear as a "hairline" cut.

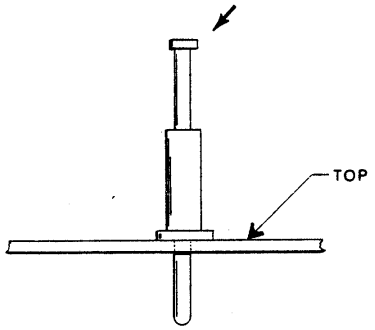
A thorough visual inspection will eliminate one possibility for errors, should the board not operate properly after it is assembled. Troubleshooting efforts may then be concentrated elsewhere.

4-12. TERMINAL TEST POINT INSTALLATION (Figure 4-2)

Install the nine test points, TP1 through TP9 (Bag 7), on the 88-S4K Memory Board according to the following instructions.

1. Insert the pin through the silk-screened (top) side of the board and solder it in place on the foil (bottom) side of the board.

2. Insure that the pin is straight.



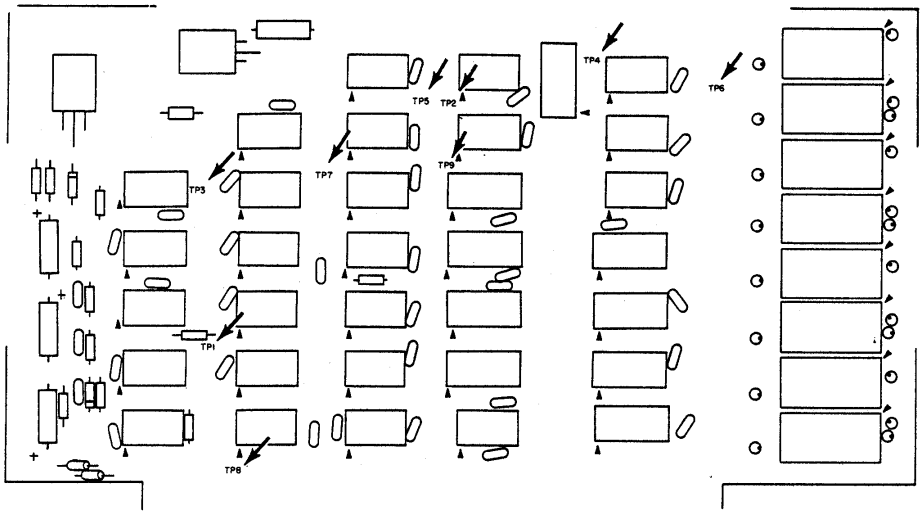


Figure 4-2. Terminal Test Point Installation

4-13. DIODE INSTALLATION (Figure 4-3)

Install the two diodes, D1 and D2 (Bag 8), on the 88-S4K Memory Board according to to the Diode Installation Instructions on page 4-4.

> NOTE
>
> If your kit is supplied with the 4030 RAM ICs install the Zener Diode IN746A, 3.3v (D1). For all other RAMs, install the 5v Zener Diode.

Diode	Part Number
( ) D1	Zener Diode, IN4733, 5v or Zener Diode, IN746A, 3.3v
( ) D2	IN914 or IN4143

4-14. TRANSISTOR INSTALLATION (Figure 4-3)

Install the transistor, Q1 (Bag 8), on the 88-S4K Memory Board according to the Transistor Installation Instructions on page 4-4.

Transistor	Part Number
( ) Q1	2N5447

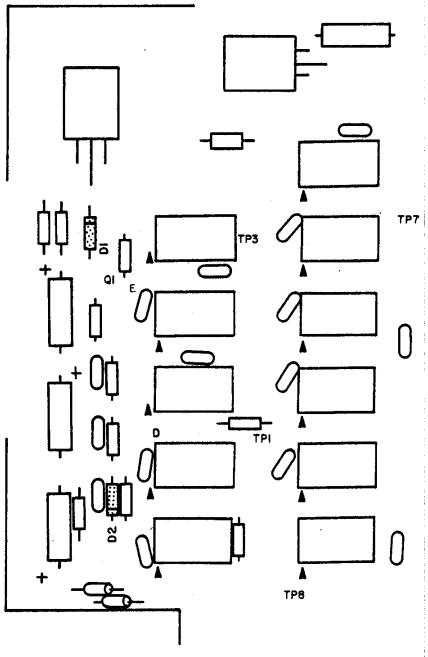


Figure 4-3. Diode and Transistor Installation

4-15. RESISTOR INSTALLATION (Figure 4-4)

Install the following twelve resistors (Bag 6) on the 88-S4K Memory Board according to the Resistor Installation Instructions on page 4-5.

> NOTE
>
> Save excess resistor leads for use in the Ferrite Bead Installation, paragraph 4-16.
>
> When installing R11, insert the leads into the board so that approximately 2/3 of the leads protrude through the foil(bottom) side of the board. Bend the resistor, R11, away from IC-E on the silkscreen to facilitate installation of IC-E in paragraph 4-20.

Resistor Values

( ) R1	1K ohm, 1/2w (brown, black, red)
( ) R2,R3	33 ohm, 1/2w (orange, orange, black)
( ) R4,R6	470 ohm, 1/4w (yellow, purple, brown)
( ) R5,R7,R10, R12	220 ohm, 1/4w (red, red, brown)
( ) R8	27 ohm, 1/4w (red, purple, black)
( ) R9	470 ohm, 1/2w (yellow, purple, brown)
( ) R11	4.7K ohm, 1/4w (yellow, purple, red)

4-16. FERRITE BEAD INSTALLATION (Figure 4-4)

Install the two ferrite beads, L1 and L2 (Bag 7), on the 88-S4K Memory Board according to the following instructions.

1. Using excess resistor leads, cut two 1-inch lead lengths.
2. Insert the lead through the bead and bend the ends so they conform to the designated holes on the 4K Dynamic Memory Board.
3. Insert the leads into the silk-screened (top) side of the board and solder to the foil(bottom) side of the board, being careful not to leave any solder bridges.
4. Clip off any excess lead lengths.

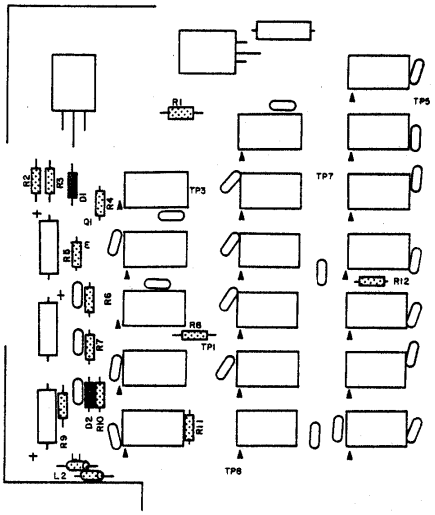


Figure 4-4. Resistor and Ferrite Bead Installation

4-17. SUPPRESSOR CAPACITOR INSTALLATION (Figure 4-5)

Install the thirty-three suppressor capacitors (Bag 4) on the 88-S4K Memory Board according to the Capacitor Installation Instructions, Section B, on page 4-6. All of these capacitors are ceramic disk and are marked only by an outline on the silkscreen.

Suppressor Capacitor Values	
( ) 33 suppressor capacitors	.1mf

C7 polarity not indicated on PC Board silkscreen. Orient as shown below.

4-18. CAPACITOR INSTALLATION (Figure 4-5)

Install the four ceramic disk capacitors and the four electrolytic capacitors (Bag 3) on the 88-S4K Memory Board according to the Capacitor Installation Instructions on page 4-6.

Capacitor Values	
( ) C2	100 pf, ceramic disk
( ) C4, C6	.01mf, ceramic disk
( ) C8	.001mf, ceramic disk
( ) C1,C3,C5,C7	33mf, 16v, electrolyti

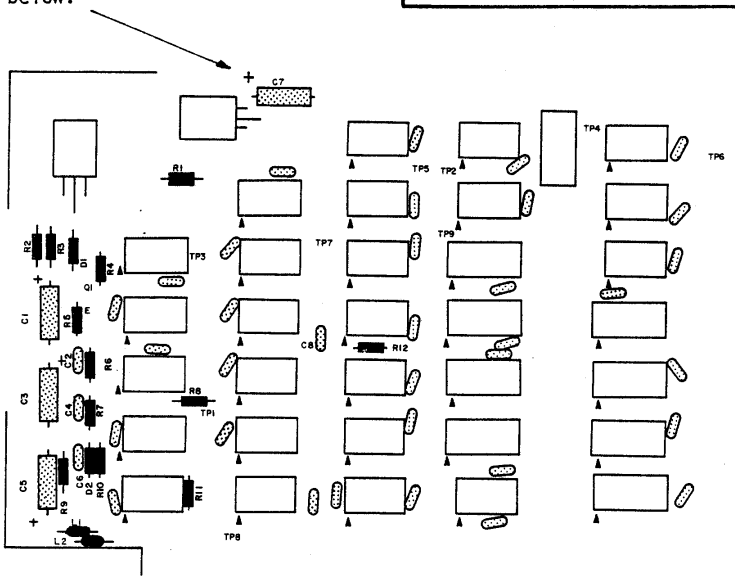


Figure 4-5. Suppressor Capacitor and Capacitor Installation

4-19. VOLTAGE REGULATOR INSTALLATION (Figure 4-6)

Install the voltage regulators, VR1 and VR2 with heat sinks (Bag 1), on the 88-S4K Memory Board according to the following instructions.

> NOTE
>
> The large heat sink should be installed with VR1 and the small heat sink with VR2.

1. Set the regulator in place on the silk-screened (top) side of the board, aligning the leads with their designated holes.
2. Use needle-nose pliers to bend each of the three leads at a right angle to conform to its proper hole on the board.

> NOTE
>
> Use heat sink grease when installing this component. Apply the grease to all surfaces which come in contact with each other.

3. Referring to Figure 4-6, set the regulator and heat sink in place on the silk-screened side of the board and secure them with a #6-32 x 3/8" screw and 6-32 nut.
4. Solder the three leads to the foil (bottom) side of the board, being careful not to leave any solder bridges.
5. Clip off any excess lead lengths.

Voltage Regulator	Part Number
( ) VR1 (large heat sink)	7805
( ) VR2 (small heat sink)	7812

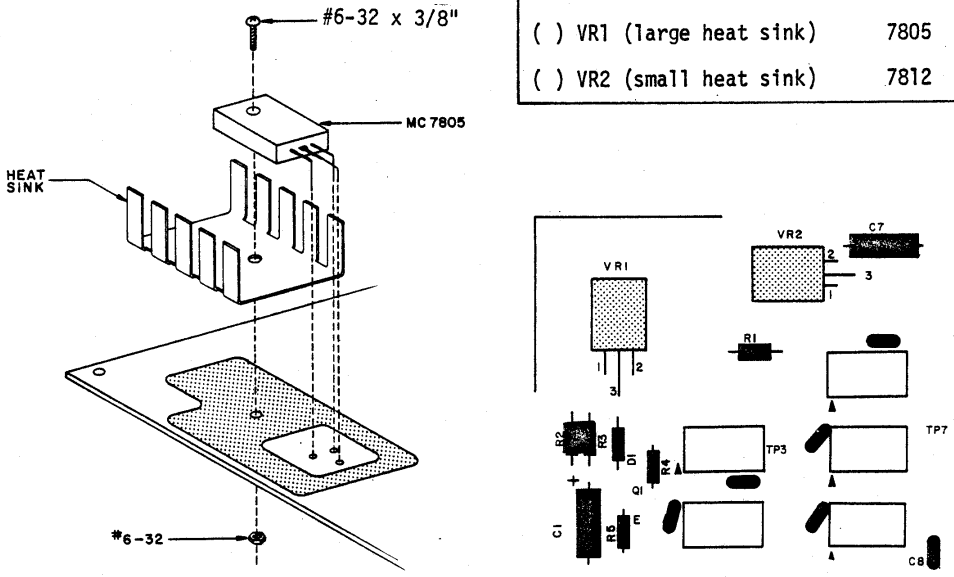


Figure 4-6. Voltage Regulator Installation

4-20. IC INSTALLATION (Figure 4-7)

Install the following thirty-two integrated circuits (Bag 1), without sockets, on the 88-S4K Memory Board according to the IC Installation Instructions, Section A, page 4-7.

> **CAUTION**
>
> Insure that solder bridges are not formed.

> **NOTE**
>
> ICs X and Y are static-sensitive MOS ICs. Refer to page 4-10 for special handling instructions. Failure to carefully follow these instructions may result in permanent damage to the static-sensitive ICs.

IC	Part Number
( ) A,E	74LS73
( ) B,J,N,R,T	74LS00
( ) C	7406
( ) D	74LS02
( ) F,G,P,S	74LS74
( ) H,K,W,BB,CC,DD,EE	74LS04
( ) L,U	74L04
( ) M	74LS10
( ) V	74L20/101039
( ) X	4040
( ) Y	4449
( ) Z,AA,HH,JJ	8T97/74367
( ) FF,GG	74LS75

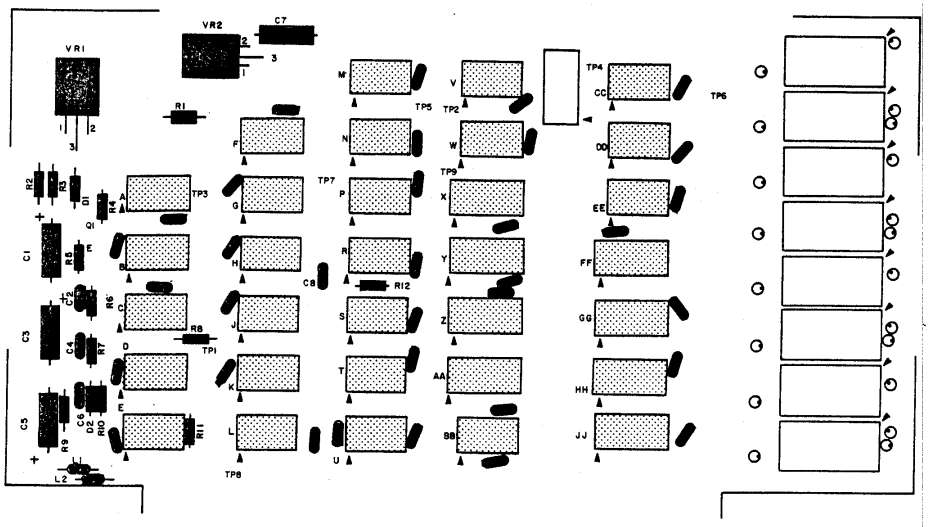


Figure 4-7. IC Installation

4-21. ADDRESS SWITCH INSTALLATION (Figure 4-8)

Install the 4-position address switch (Bag 1) on the 88-S4K Memory Board according to the following instructions.

1. Remove the 16-pin switch from its holder and straighten any bent pins with needle-nose pliers.

2. Orient the switch so that the numbers 1,2,3,4 are above S1 as shown in Figure 4-8.

3. Start the pins on one side of the switch onto their respective holes on the silk-screened (top) side of the board. DO NOT PUSH THE PINS IN ALL THE WAY. If you have difficulty getting the pins into the holes, use the tip of a small screwdriver to guide them.

4. Start the pins on the other side of the switch into their holes in the same manner and when all the pins have been started, set the switch into place by gently rocking it back and forth until it rests as close to the board as possible.

5. After you are sure that the switch is straight, tape it in place with a piece of masking tape.

6. Turn the board over and solder EACH pin to the foil (bottom) side of the board, being careful not to leave any solder bridges.

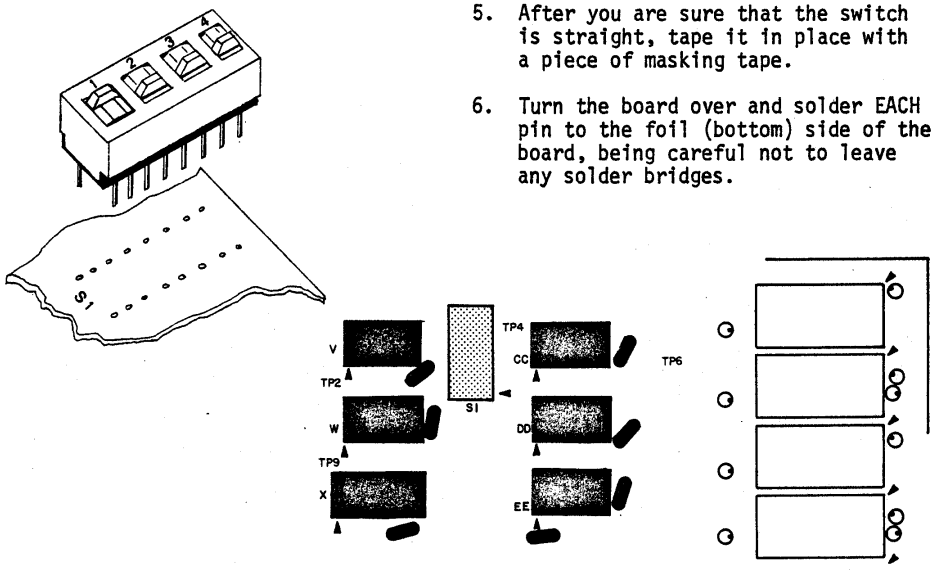


Figure 4-8. Address Switch Installation

4-22. ADDRESS SWITCH SETTING

Referring to Table 4-1, there are sixteen possible starting address selections beginning with 0 and ending at 60. The switch configuration depends on the starting address desired for this board. Each 4K of memory has a specific S1 setting.

Example: An 8K memory consisting of two 88-S4K Memory Board would be addressed as follows.

The first memory board would have a starting address of 0 and an S1 setting of OFF, OFF,OFF, OFF. The second memory board would have a starting address of 4K and an S1 setting of ON, OFF, OFF, OFF. The total amount of memory is from address 0 to address 8191.(Computer terminology defines 1K = 1 times 1024; 8K = 8 times 1024 = 8192. Since the first location is 0, the last location is 8192 - 1, or 8191.)

NOTE

A switch pressed toward 1,2,3,4 is considered to be ON. A switch pressed toward the opposite direction is considered to be OFF.

Table 4-1. 88-S4K Memory Board Address Selection for Switch Setting (S1)

S1 - OFF position connects to the inverted address signal ($\overline{A}$)
ON position connects directly to address line (A)

Board Number	Memory Addresses	Address Switch (S1)			
		1	2	3	4
1	0-4K	OFF	OFF	OFF	OFF
2	4-8K	ON	OFF	OFF	OFF
3	8-12K	OFF	ON	OFF	OFF
4	12-16K	ON	ON	OFF	OFF
5	16-20K	OFF	OFF	ON	OFF
6	20-24K	ON	OFF	ON	OFF
7	24-28K	OFF	ON	ON	OFF
8	28-32K	ON	ON	ON	OFF
9	32-36K	OFF	OFF	OFF	ON
10	36-40K	ON	OFF	OFF	ON
11	40-44K	OFF	ON	OFF	ON
12	44-48K	ON	ON	OFF	ON
13	48-52K	OFF	OFF	ON	ON
14	52-56K	ON	OFF	ON	ON
15	56-60K	OFF	ON	ON	ON
16	60-64K	ON	ON	ON	ON

4-23. RAM INSTALLATION (Figure 4-9)

Install the eight RAM ICs, with sockets (Bag 2), on the 88-S4K Memory Board according to the Integrated Circuit Instructions, Section B, on page 4-7. Refer to page 4-9 for special handling instrucitons of the RAMs. Failure to carefully follow these instructions may result in permanent damage to the static-sensitive ICs.

> CAUTION
>
> Insure that solder bridges are not formed.

> NOTE
>
> It is recommended that a piece of aluminum foil be placed along the card stab connector when installing the ICs so that the pins of the RAMs are at the same potential. This will reduce the possibility of static damage to the RAMs during assembly.
>
> The RAM part number will vary with your kit due to supply from different manufacturers.

IC	Part Number
( ) KK,LL,MM,NN, PP,RR,SS,TT	22-pin 88-S4K RAM

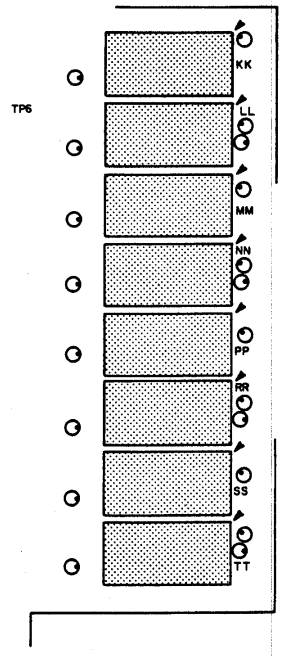


Figure 4-9. RAM Installation

4-24. TANTALUM CAPACITOR INSTALLATION (Figure 4-10)

Install the twenty tantalum capacitors (Bag 5) on the 88-S4K Memory Board according to the Capacitor Installation Instructions, Section A, on page 4-6.

NOTE

The positive side of the capacitor should be oriented towards the "+" sign on the silkscreen.

Tantalum Capacitor Values

( ) 20 tantalum capacitors 1mf,35v

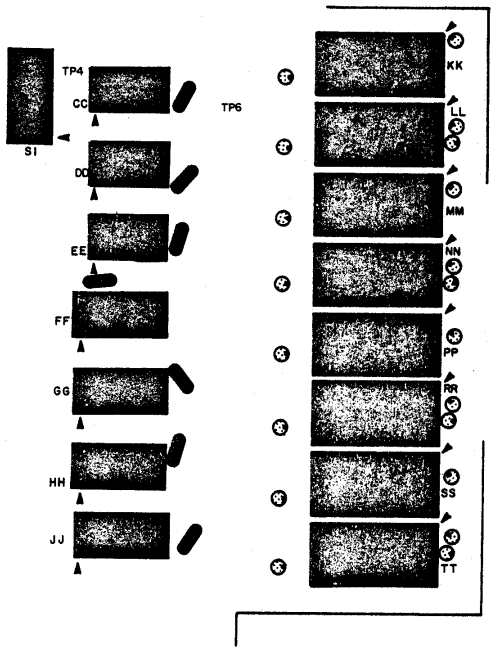


Figure 4-10. Tantalum Capacitor Installation

4-25. 4K DYNAMIC MEMORY BOARD INSTALLATION

Refer to Figure 4-11 to insure that the 88-S4K Memory Board is completely assembled before installing it into the Altair 8800 main frame according to the following instructions.

1. Remove the expander board from the Altair 8800 main frame.

2. Install the 100-pin edge connector and two card guides (Bag 7) as shown on pages 64-68 of the Altair 8800 and 8800a Assembly Manual or Section 5-71 of the Altair 8800b Assembly Manual.

> CAUTION
>
> Insure that solder bridges are not formed on the 100-pin edge connector. -

3. Replace the expander board onto the main frame and insert the card stab connector of the 88-S4K Memory Board onto the 100-pin edge connector.

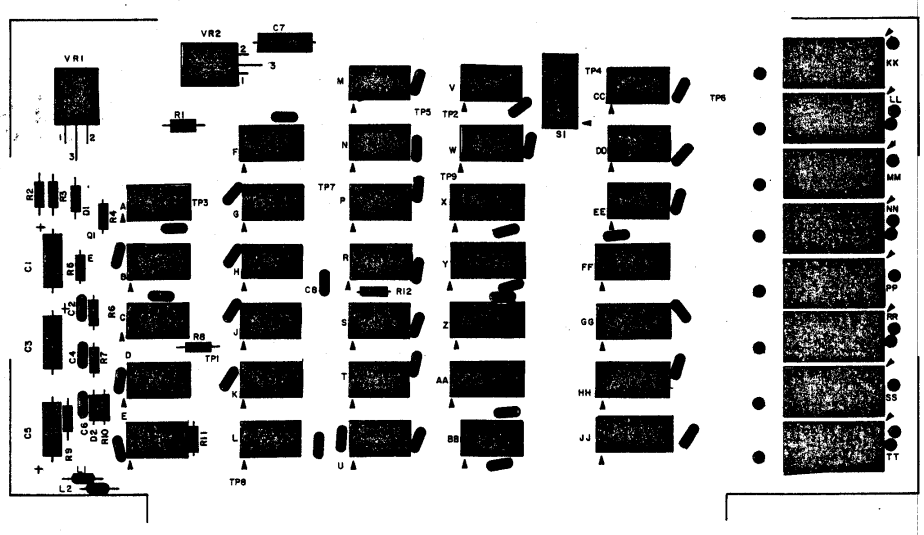


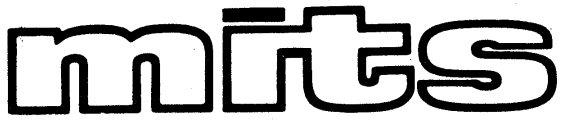
Figure 4-11. Completely Assembled 88-S4K Memory Board

appendix A

parts list

Bag	Quantity	Component	MITS Stock Number
1	5	74LS00 Integrated Circuit	101069
	1	74LS02 Integrated Circuit	101136
	2	74L04 Integrated Circuit	101073
	7	74LS04 Integrated Circuit	101042
	1	7406 Integrated Circuit	101054
	1	74LS10 Integrated Circuit	101133
	1	74L20 Integrated Circuit	101039
	2	74LS73 Integrated Circuit	101119
	4	74LS74 Integrated Circuit	101088
	2	74LS75 Integrated Circuit	101117
	1	4040 Integrated Circuit	101130
	1	4449 Integrated Circuit	101104
	4	8T97/74367 Integrated Circuit	101040
	1	7805 Voltage Regulator	101074
	1	7812 Voltage Regulator	101085
	1	4-Position DIP Switch	102321
2	8	4K RAM Integrated Circuit	101086 or 101076 or 101094
	8	22-pin Socket	102108
3	1	100pf Capacitor	100361
	2	.01mf Capacitor	100321
	1	.001mf Capacitor	100328
	4	33mf Capacitor	100326
4	33	.1mf Capacitor	100348
5	20	1mf Capacitor	100308

Bag	Quantity	Component	MITS Stock Number
6	1	27 ohm 1/4w Resistor	101916
	4	220 ohm 1/4w Resistor	101901
	2	470 ohm 1/4w Resistor	101902
	1	470 ohm 1/2w Resistor	101927
	1	1K ohm 1/2w Resistor	101928
	1	4.7K ohm 1/4w Resistor	101912
	2	33 ohm 1/2w Resistor	101921
7	9	Terminal (Test Point)	101663
	1	Heat Sink (large)	101870
	1	Heat Sink (small)	101667
	2	Ferrite Bead	101876
	1	100-pin Edge Connector	101864
	2	Card Guide	101714
	6	#6-32 x 3/8" Screw	100925
	2	#6-32 Nut	100933
	2	#6 Lockwasher	100942
8	1	IN4733 5v Zener Diode or IN746A 3.3v Zener Diode	100721 100708
	1	IN914 or IN4143 Diode	100705
	1	2N5447 Transistor	102815
MISC.	1	PC Board (4K RAM)	100210
	1	88-S4K Synchronous 4K Memory Board Documentation	101563



2450 Alamo SE
Albuquerque, NM 87106