(MS-6597) *Version: 1.0*

Nvidia (R) Crush11(nForce IGP 64) + MCP2/2H Chipset
AMD Althon/Duron/Morgan/Palomino Socket 462 Processor

CPU:

AMD Duron/Morgan/Athlon & XP Processor

System Chipset:

Nvidia nForce IGP 64 (North Bridge)
MCP2/2H Wep (South Bridge)

On Board Chipset:

BIOS -- LPC EEPROM
AC'97 Codec -- ALC650E
LPC Super I/O -- W83627HF-AW
LAN -- ICS1893 PHY
I1394 -- FW803 PHY (Option)

Expansion Slots:

AGP2.0 SLOT (1.5V) * 1
PCI2.2 SLOT * 3

PWM Controller:

L6911D

ACPI:

MS5

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Title	COVER SHEET	
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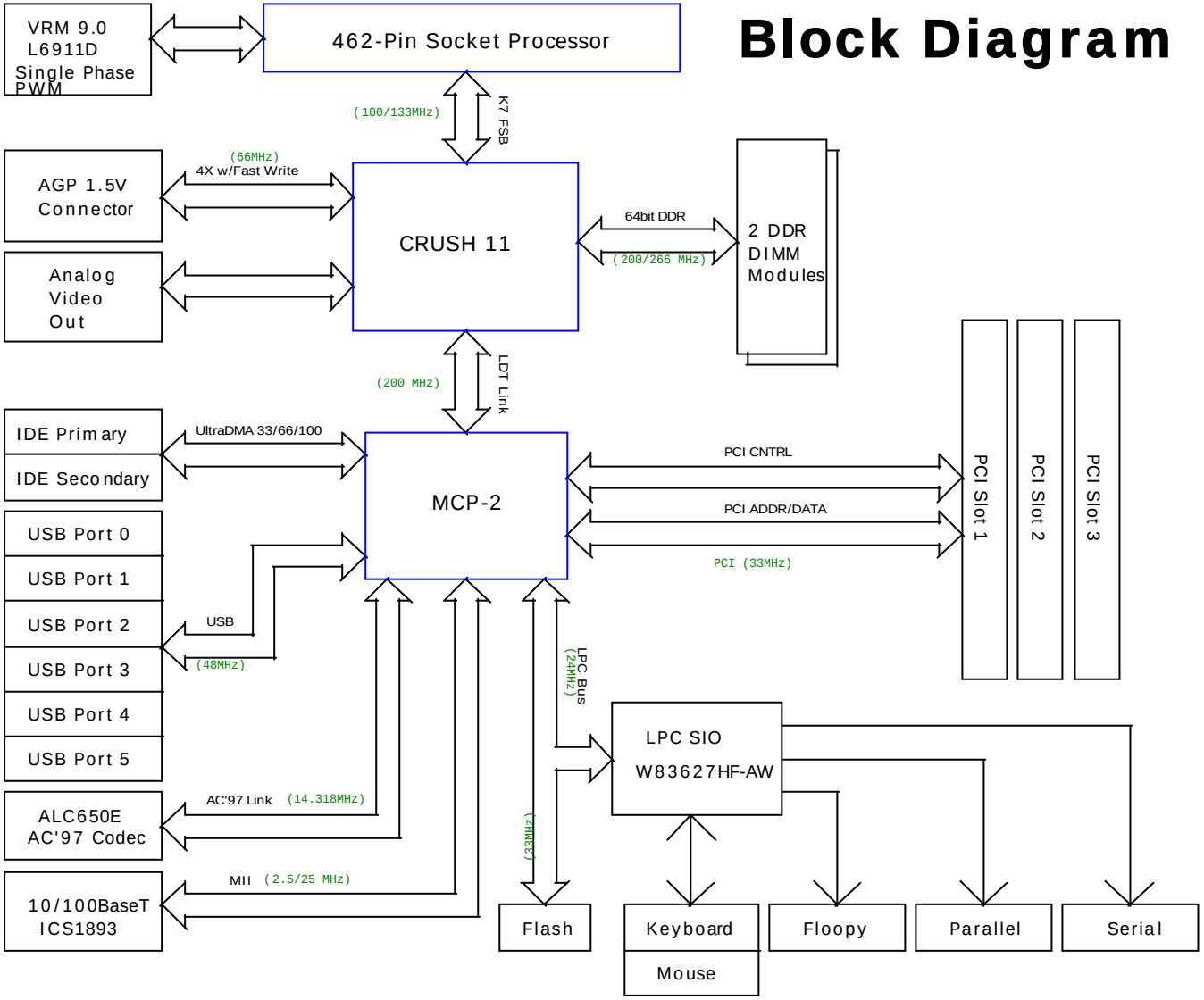
Date: Tuesday, October 22, 2002	Sheet 1 of 25	

Block Diagram



MSI	MICRO-STAR INt'L CO., LTD.	
Title	BLOCK DIAGRAM	
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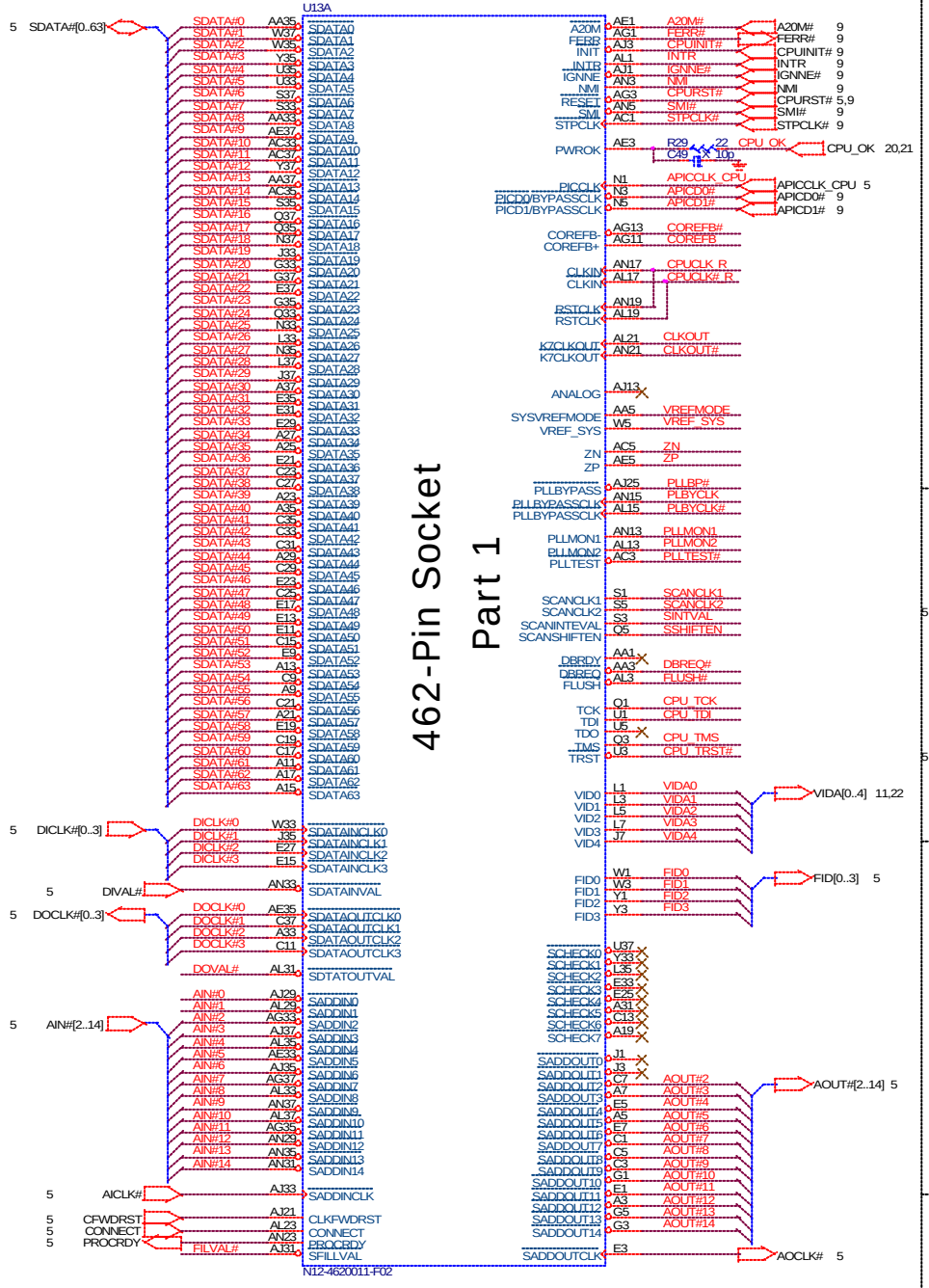
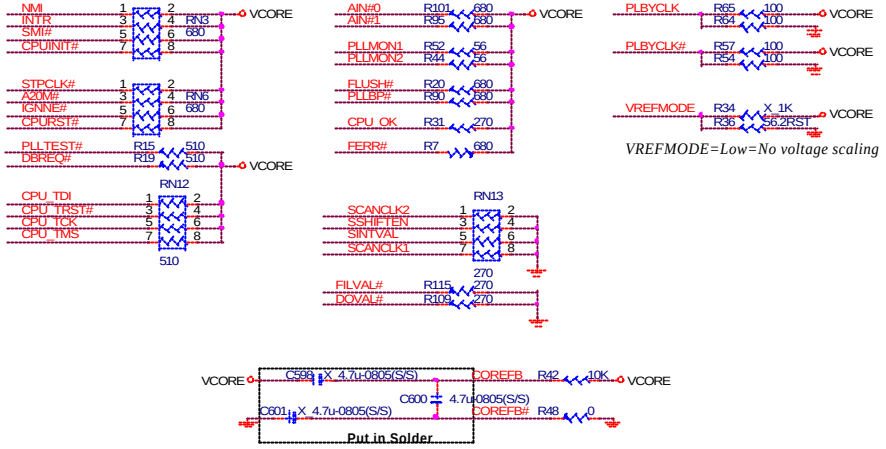
CPU SIGNAL BLOCK

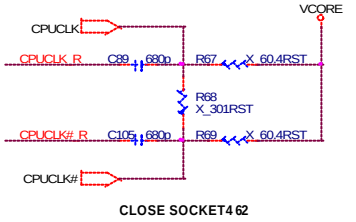


****All CPU interface are 2.5V tolerant****

CPU PULL-UP / DOWN BLOCK

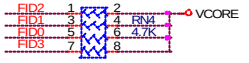


CPU SYSCLK BLOCK



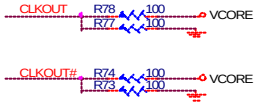
CLOSE SOCKET462

CPU Clock Multiplier



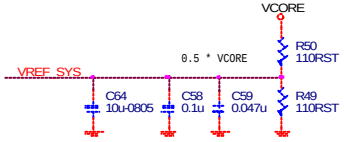
CFID[3:0] => CPU Clock Multiplier

CPU K7CLKOUT BLOCK



**** Trace lengths of CLKOUT and CLKOUT# are between 2" and 3"***

CPU SYSCLK REFERNCE BLOCK



CLOSE SOCKET462

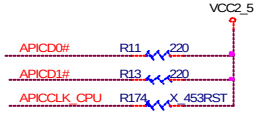
CPU ZN / ZP BLOCK

CLOSE SOCKET462

match the transmission line

Push-pull compensation circuit

CPU APIC BLOCK



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Title	AMD Socket462 CPU (Signal)	
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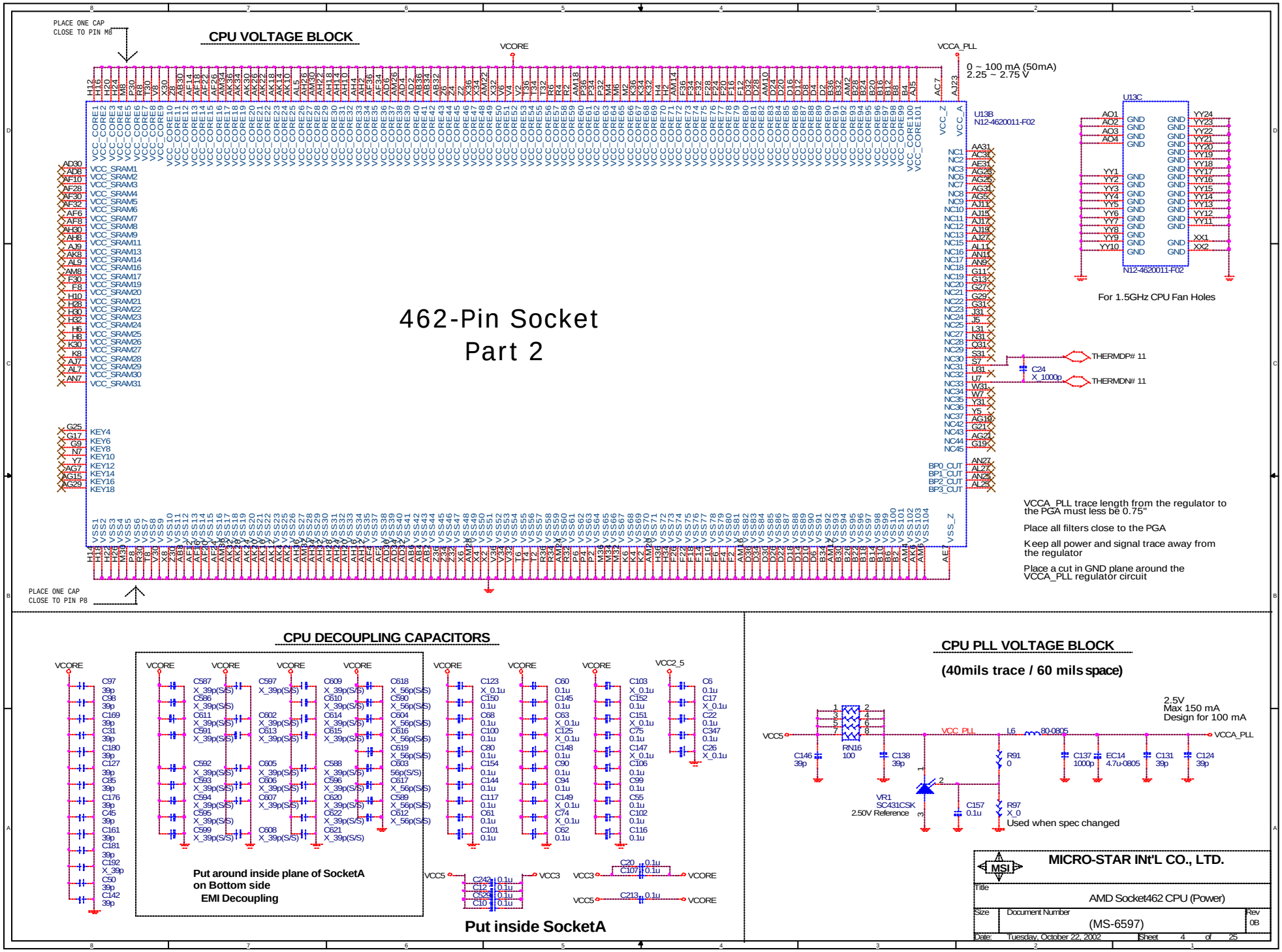
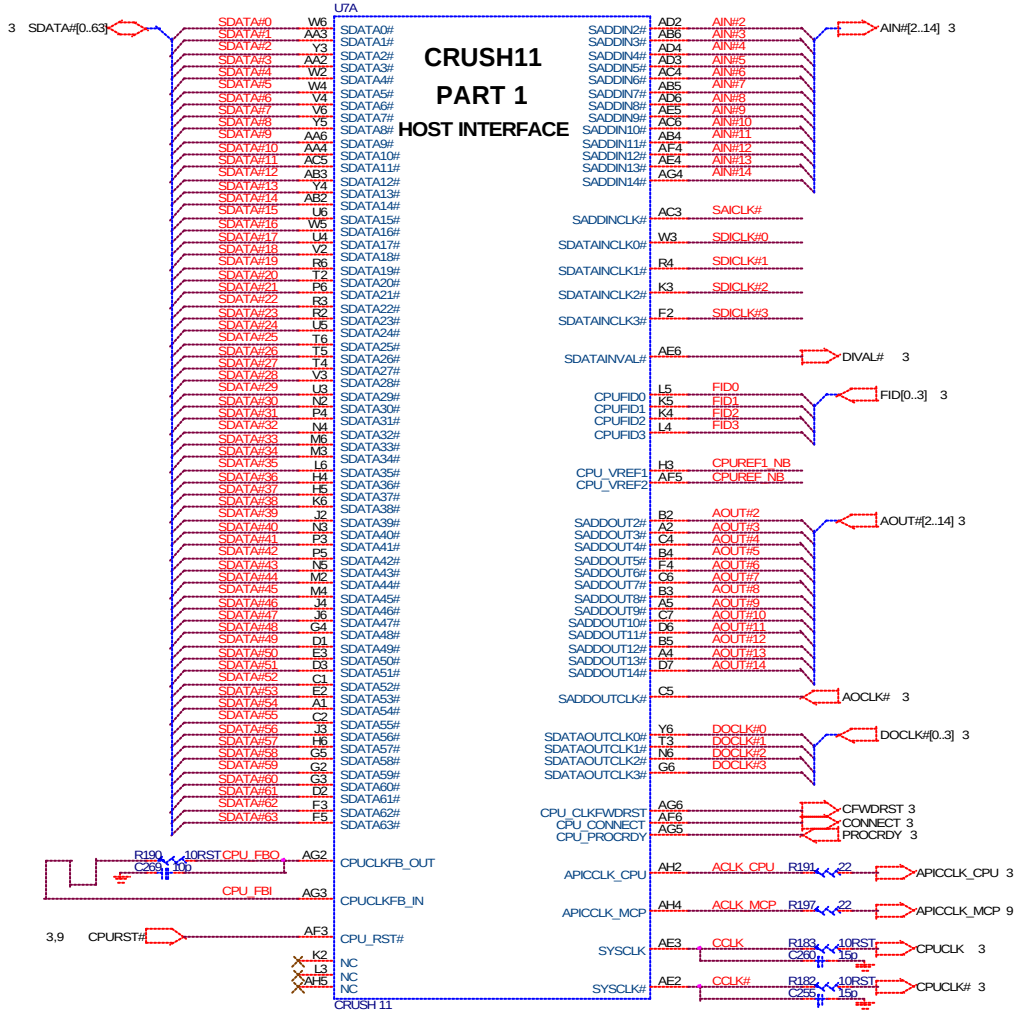
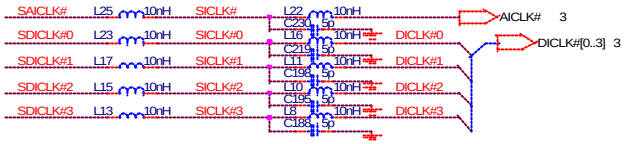

CPU VOLTAGE BLOCK
PLACE ONE CAP CLOSE TO PIN M8
PLACE ONE CAP CLOSE TO PIN P8
VCORE
VCCA_PLL
0 ~ 100 mA (50mA)
2.25 ~ 2.75 V
462-Pin Socket
Part 2
U13B
N12-4620011-F02
U13C
N12-4620011-F02
For 1.5GHz CPU Fan Holes
THERMDP# 11
THERMDN# 11
C24
X_1000p
VCCA_PLL trace length from the regulator to the PGA must less be 0.75"
Place all filters close to the PGA
Keep all power and signal trace away from the regulator
Place a cut in GND plane around the VCCA_PLL regulator circuit
CPU DECOUPLING CAPACITORS
Put around inside plane of SocketA on Bottom side
EMI Decoupling
Put inside SocketA
CPU PLL VOLTAGE BLOCK
(40mils trace / 60 mils space)
2.5V
Max 150 mA
Design for 100 mA
VR1
SC431CSK
2.50V Reference
Used when spec changed
MICRO-STAR INt'L CO., LTD.
AMD Socket462 CPU (Power)
(MS-6597)
Tuesday, October 22, 2002

CRUSH 11 HOST SIGNALS

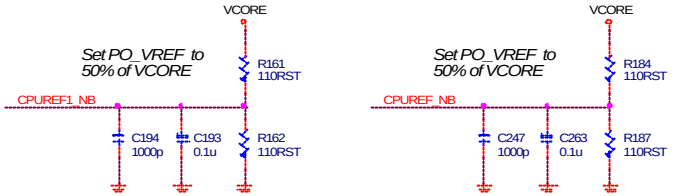


SYSTEM DATA-IN-CLK NOISE L/C BLOCK

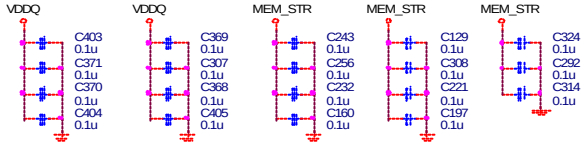


CLK must less DATA 1.5inchs

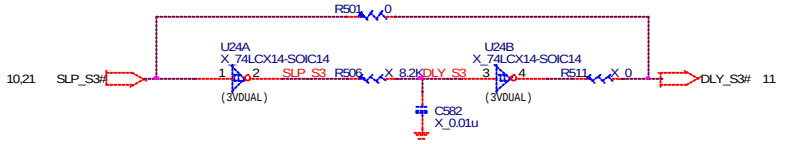
REFERNCE VOLTAGE BLOCK



Crush 11 Decoupling Capacitors



S3 Delay Block



BELONG TO CLKFWD GROUP[SADDIN] MATCH W/IN +/-10MILS OF GROUP 5/15, CLK:10/30

BELONG TO CLKFWD GROUP[SADDOUT] MATCH W/IN +/-10MILS OF GROUP 5/15, CLK:10/30

BELONG TO CLKFWD GROUP;MATCHED TO INDIVIDUAL CLKFWD GROUP

RESPECTIVELY.[SDATA0], [SDATA1], [SDATA2],[SDATA3] W/IN+/-10MILS OF GROUP

MICRO-STAR INt'L CO., LTD.

Title	Crush11 Host Signals	
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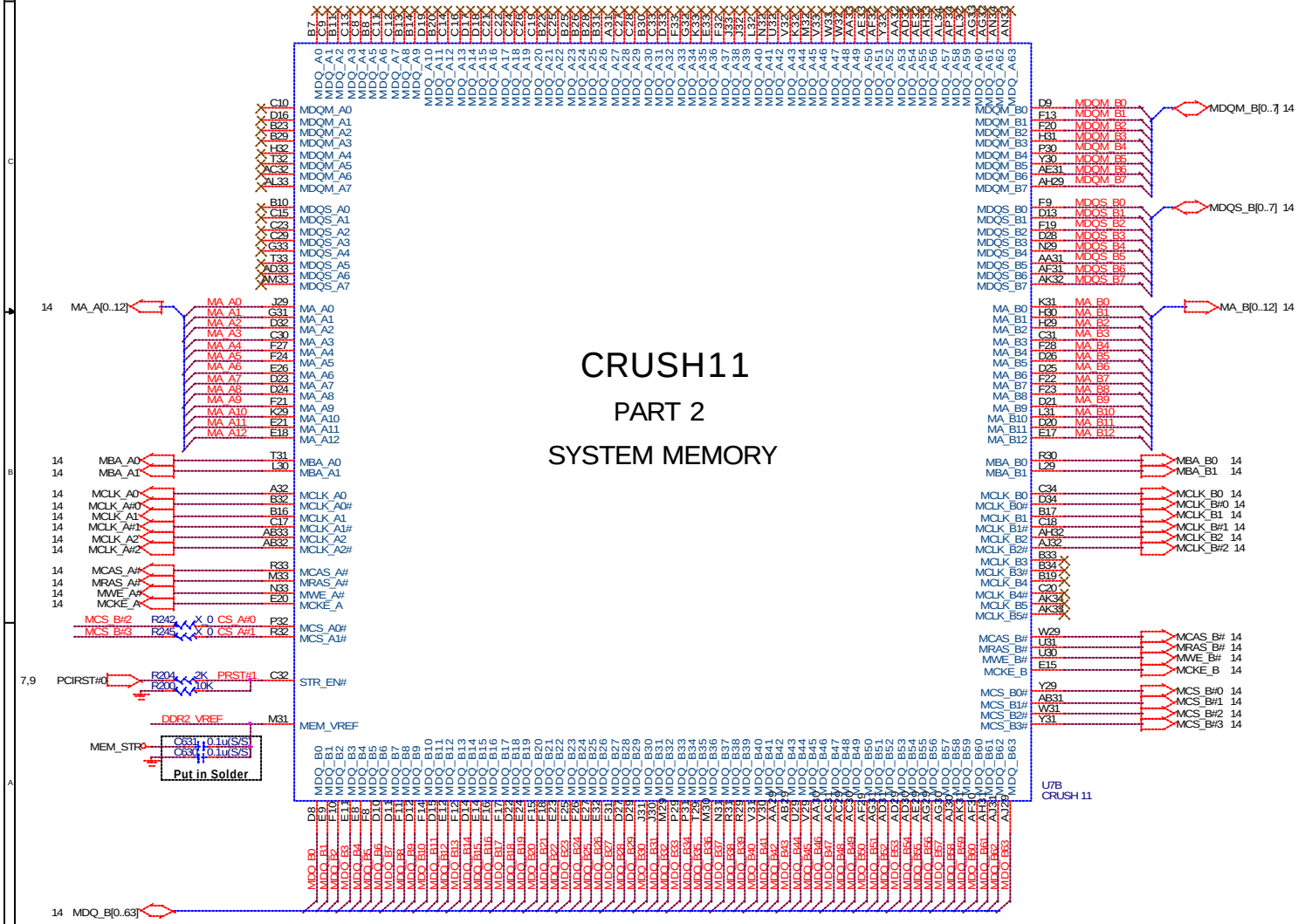
CRUSH 11 MEMORY SIGNALS

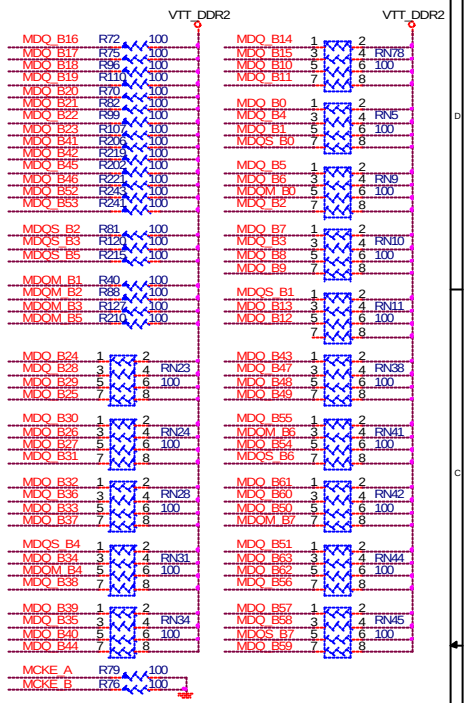
CRUSH11

PART 2

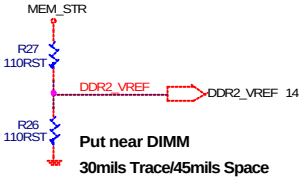
SYSTEM MEMORY



DDR Terminational Resisitors



DDR REFENCE VOLTAGE



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CRUSH 11 AGP & LDT SIGNALS

CRUSH11 PART 3 AGP 4X, VIDEO, AND LDT INTERFACE

U7C

15 GAD[0..31] — GAD0 AL19 … GAD31 AK10 — AGP_AD0 … AGP_AD31

15 GC_BE#[0..3] — GC_BE#0 AM18, GC_BE#1 AN16, GC_BE#2 AM13, GC_BE#3 AL11 — AGP_CBE0# … AGP_CBE3#

15 AD_STB0 AK17 — AGP_ADSTB0
15 AD_STB#0 AJ17 — AGP_ADSTB0#
15 AD_STB1 AM10 — AGP_ADSTB1
15 AD_STB#1 AN11 — AGP_ADSTB1#

15 GFRAME# AN14 — AGP_FRAME#
15 GDEVSEL# AM14 — AGP_DEVESEL#
15 GIRDY# AK14 — AGP_IRDY#
15 GTRDY# AJ14 — AGP_TRDY#
15 GSTOP# AM15 — AGP_STOP#
15 GPAR AL14 — AGP_PAR

15 GREQ# AM5 — AGP_REQ#
15 GGNT# AM4 — AGP_GNT#

15 SB_STB AL8 — AGP_SBSTB
15 SB_STB# AL7 — AGP_SBSTB#

15 SBA[0..7] — SBA0 AK8 … SBA7 AK9 — AGP_SBA0 … AGP_SBA7

15 ST[0..2] — ST0 AM3, ST1 AK6, ST2 AN5 — AGP_ST0 … AGP_ST2

15 PIPE# AK7 — AGP_PIPE#
15 RBF# AP5 — AGP_RBF#
15 WBF# AM6 — AGP_WBF#

15 VREF4X_IN — VREF4X_IN AN20 — AGP_VREF

15 AGPCLK — R231 22, C302 4.7p, GCLK AP4 — AGP_CLK

GCLK_FBI AL3 — AGP_CLK_FB_IN
R212 22, C287 10p, GCLK_FBO AN4 — AGP_CLK_FB_OUT

CRUSH 11

LDT_RSET AM28 — LDT_RSET
LDT_RST# AJ3 — LDT_RST# 9

LDT_RX_CLK AN23 — LDT_RX_CLK 9
LDT_RX_CLK# AM24 — LDT_RX_CLK# 9

LDT_RXD0 AJ21 … LDT_RXD15 AM26 — LDT_RXD0 9 … LDT_RXD#8 9
LTD_RXD0# AK21 … LTD_RXD8# AM26

LDT_TX_CLK AM30 — LDT_TX_CLK 9
LDT_TX_CLK# AL29 — LDT_TX_CLK# 9

LDT_TXD0 AN32 … LDT_TXD15 AN26 — LDT_TXD0 9 … LDT_TXD#8 9
LDT_TXD0# AP32 … LDT_TXD8# AN26

TEST AK3 — TEST

INTR_OUT# AK2 — PIRQ#E 9,16
PCI_RST# AN3 — PCIRST#0 6,9

CLK14318IN AJ4 — CLK14M 10

VDD_PLL AK1 — VDD_PLL_C12
C266 1000p

VDD_DAC AP3 — VDD_DAC — L42 80-0805 — VCC3
C284 1000p, C289 0.1u, C296 4.7u-0805, C298 0.1u

DACGND AM1

DACVREF AL1 — DVREF C278 0.01u

DACRSET AP2 — RSET R208 124RST

RED AN2 — R228 0, C299 X 10p — CRT_R 17
GREEN AP1 — G R229 0, C297 X 10p — CRT_G 17
BLUE AN1 — B R227 0, C291 X 10p — CRT_B 17
HSYNC AL2 — HSYNC R207 33 — CRT_HSYNC 17
VSYNC AM2 — VSYNC R209 33 — CRT_VSYNC 17

PIN AM1 "rounted GND"
Connect each routed GND to GND plane at one point only(one via)
Use surface mount caps, and placed closed aspossibleto power pins with short, wide direct connections.

CRUSH 11 Strapping Resistors

C312 0.1u, C318 X 1u-0805 — VREF4X_IN
LDT_RSET — R255 49.9RST
TEST — R192 10K

VDD — C319 0.1u, C385 0.1u

PLL Delay Block

20,21 PWOK — R480 10KST — Q43 2N3904S — R488 X_14.7KST, C574 1u
VCORE — R481 4.75KST — Q41 2N3904S — R490 30.1KST, C571 2.2u
VDD — R478 12.1KST — Q42 2N3904S — R487 30.1KST, C572 1u

+12V — R507 10K
5VSB — R479 10K, R483 4.7K, C573 1000p — Q40 YFET-NDS7002AS

VCC3 — Q37 YFET-NDS7002AS, C575 1000p
R414 X_0 — 3VDUAL
CP13 X_COPPER — FB9 X_80-0805 — VDD_PLL_MCP 9
C494 0.1u, C488 4.7u-0805
CLOSE TO MCP2

VCC3 — Q44 YFET-NDS7002AS, C585 1000p
CP8 X_COPPER — FB5 X_80-0805 — VDD_PLL_C12
C281 0.1u, C270 4.7u-0805, C259 0.1u
CLOSE TO C11

VCC3 — R505 4.7K — R508 1K — Q38 2N3904S — PLL_RST 20
R496 18.7KST — Q45 2N3904S, C579 1u
R495 10KST, C576 0.33u
R510 56.2KST — Q39 2N3904S
R512 30.1KST, C561 0.33u

Mounting Holes

MH7, MH5, MH1, MH4, MH6, MH8, MH9, MH10

Location Reference Hold

FM1 X_FM … FM22 X_FM

MICRO-STAR INt'L CO., LTD.

Title: Crush11 AGP , LDT Signals & PLL DELAY

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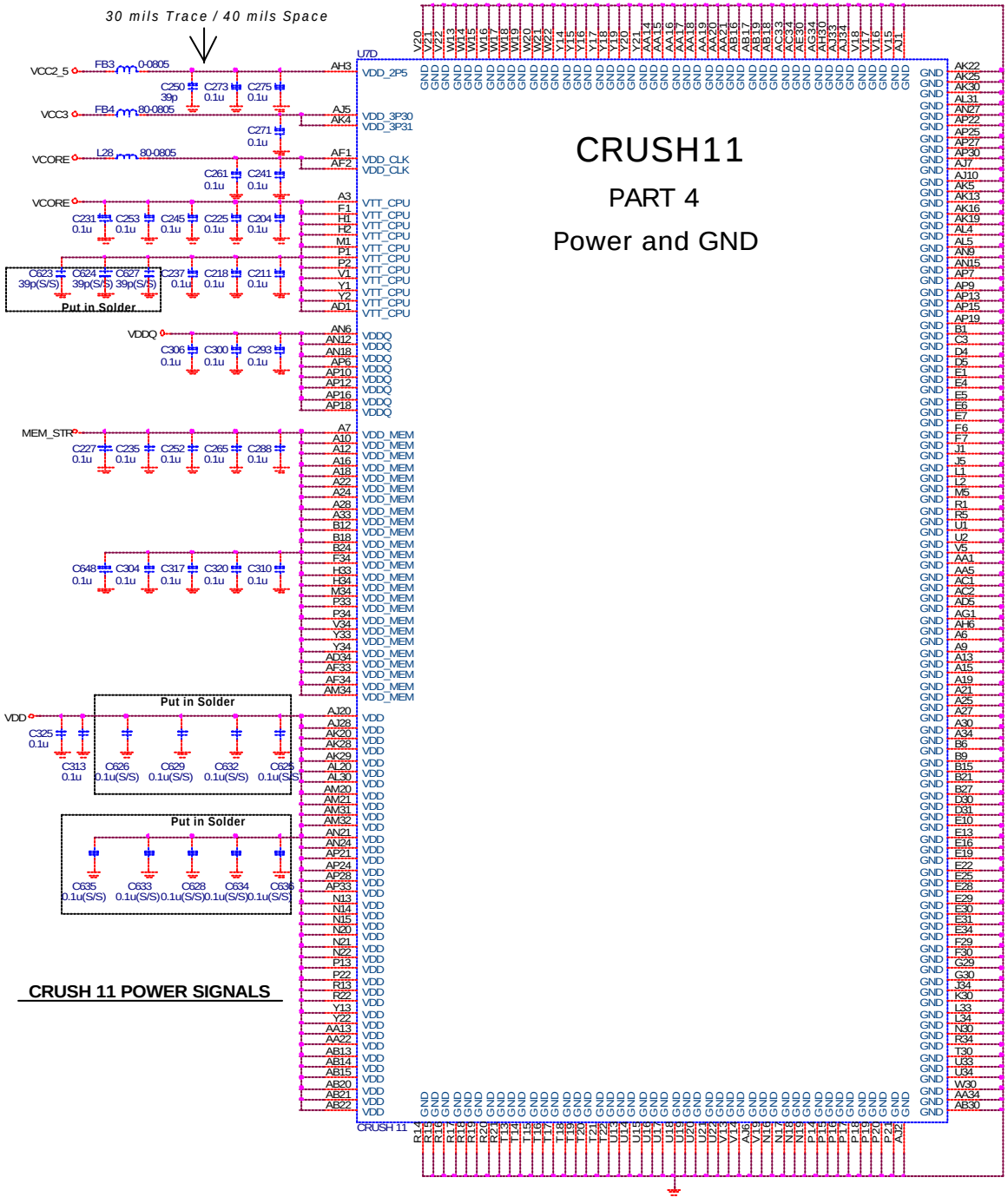

MICRO-STAR INt'L CO., LTD.

Title: Crush11 Power Signals

Size | Document Number: (MS-6597) | Rev: 0B

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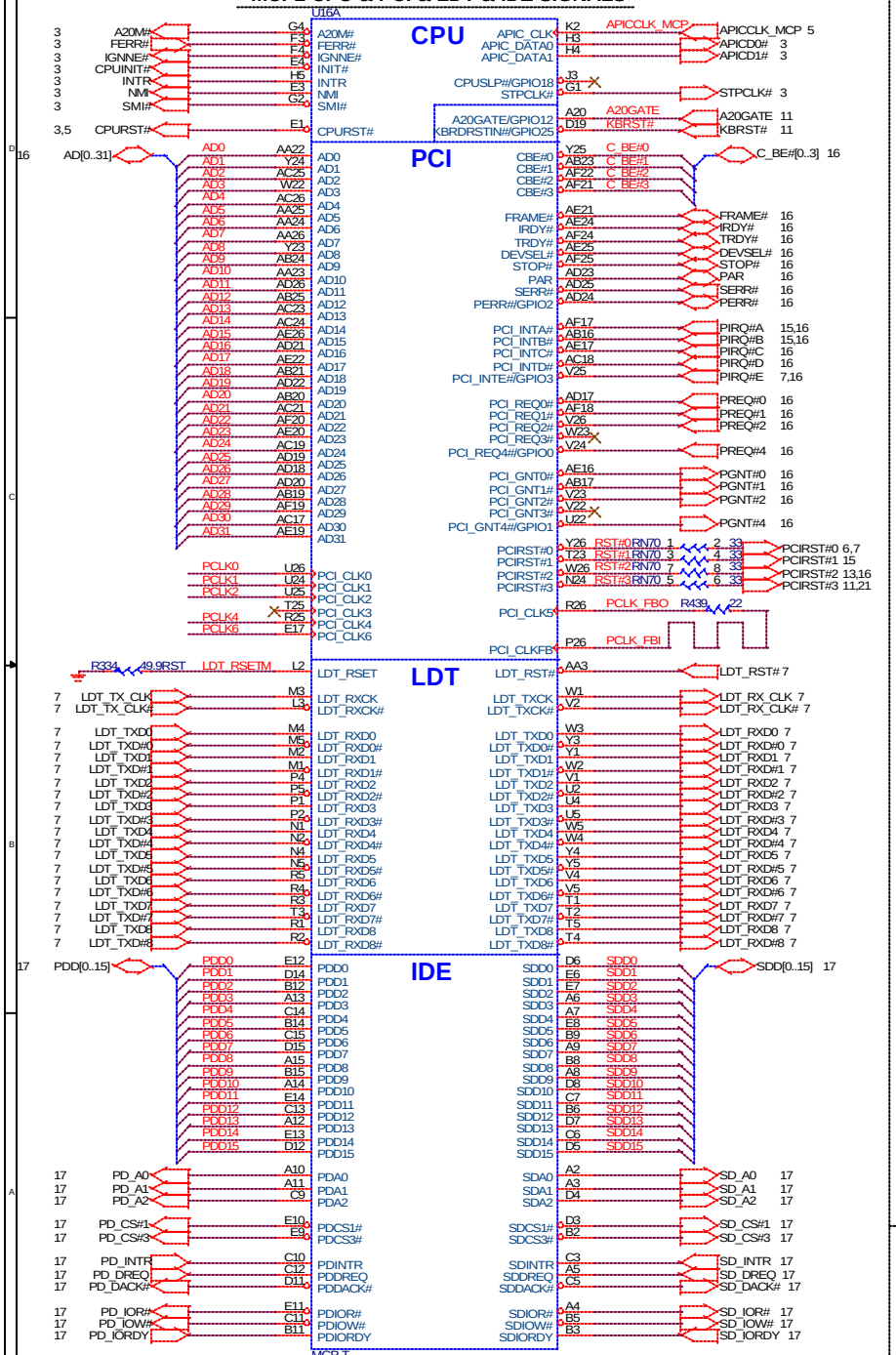
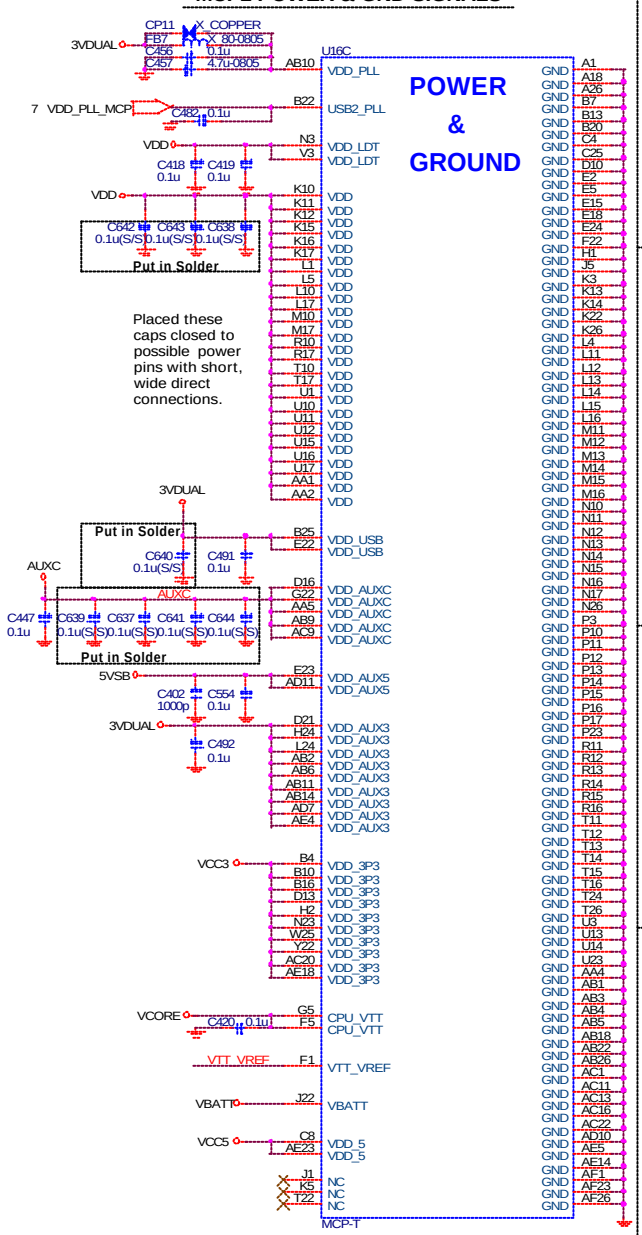
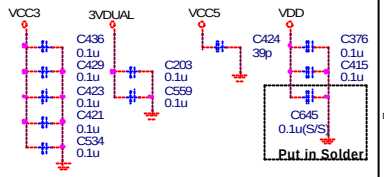
MCP2 CPU & PCI & LDT & IDE SIGNALS



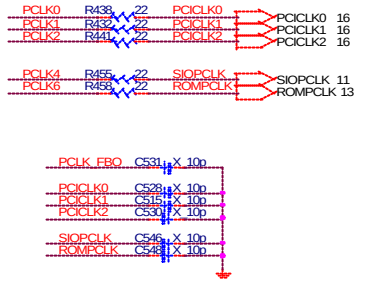
MCP2 POWER & GND SIGNALS



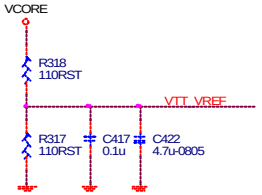
MCP Decoupling Capacitors



MCP2 PCI Clock



MCP2 REFERENCE VOLTAGE BLOCK



MCP2 STRAMPING RESISTORS

MICRO-STAR INt'L CO., LTD.

Title	MCP CPU & PCI & LDT & IDE Signals	
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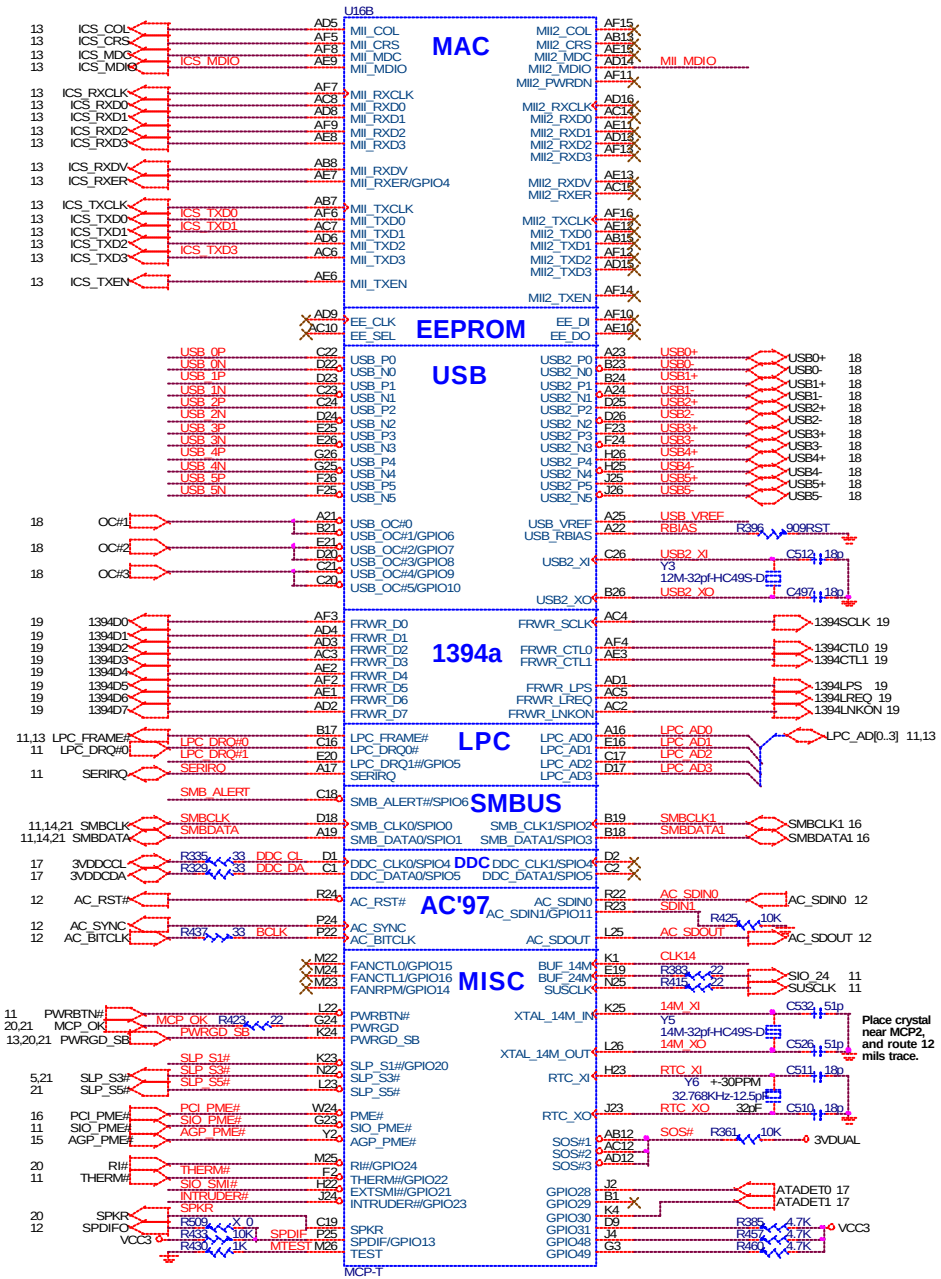
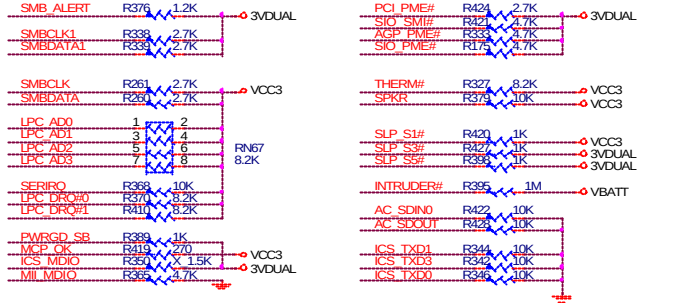
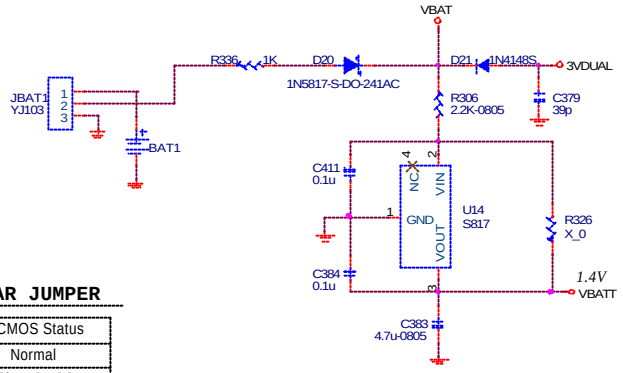
MCP2 MAC, USB, 1394A, LPC & AC'97 SIGNALS



MCP2 PULL-UP & DOWN RESISTORS



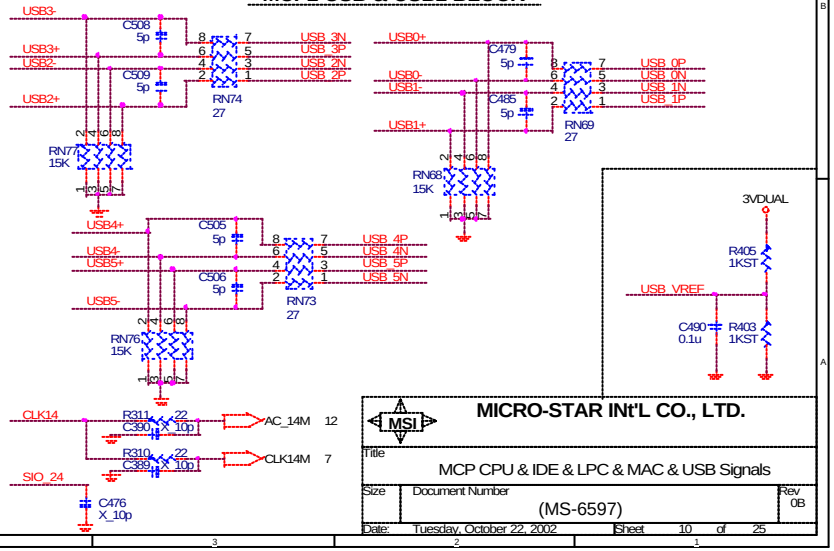
Battery



CMOS CLEAR JUMPER

JBAT1	CMOS Status
1 - 2	Normal
2 - 3	Clear CMOS

MCP2 USB & USB2 BLOCK



MICRO-STAR INt'L CO., LTD.

Title: MCP CPU & IDE & LPC & MAC & USB Signals

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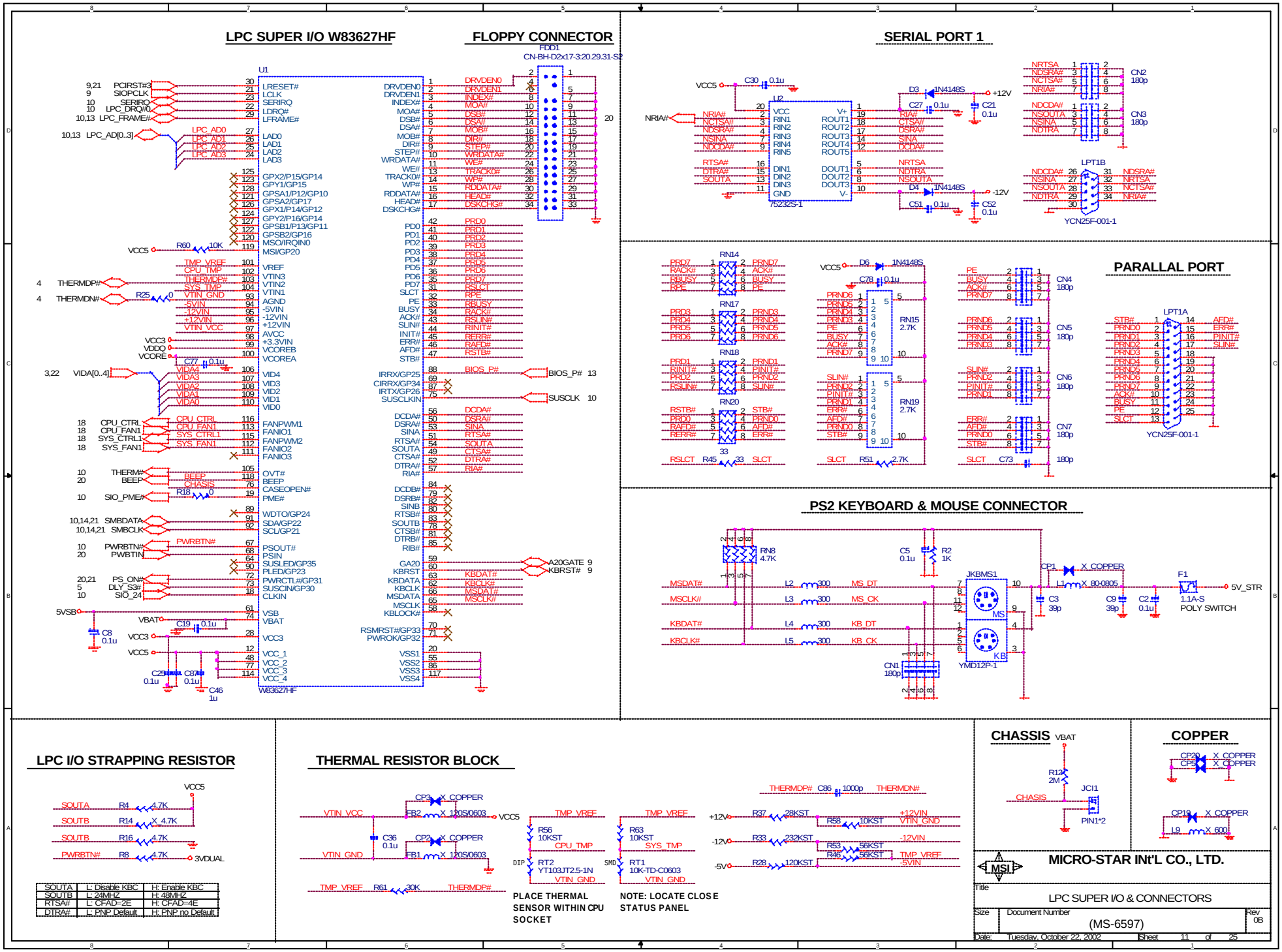
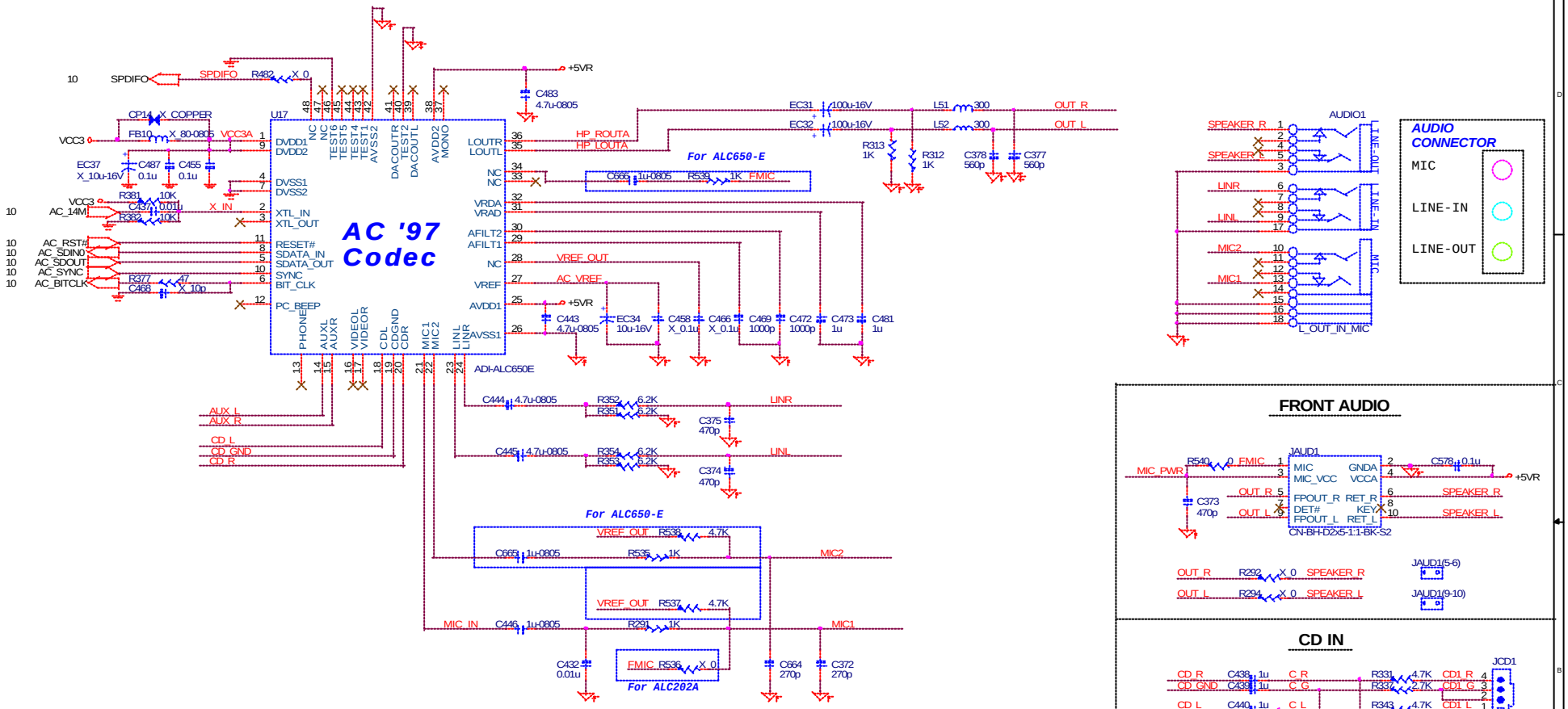
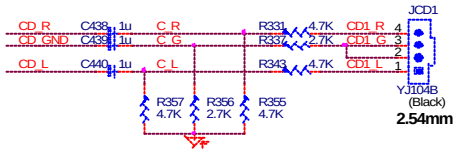

LPC SUPER I/O W83627HF
FLOPPY CONNECTOR
SERIAL PORT 1
PARALLAL PORT
PS2 KEYBOARD & MOUSE CONNECTOR
LPC I/O STRAPPING RESISTOR
THERMAL RESISTOR BLOCK
CHASSIS
COPPER
MICRO-STAR INt'L CO., LTD.
LPC SUPER I/O & CONNECTORS
(MS-6597)
PLACE THERMAL SENSOR WITHIN CPU SOCKET
NOTE: LOCATE CLOSE STATUS PANEL

AC'97 AUDIO CODEC

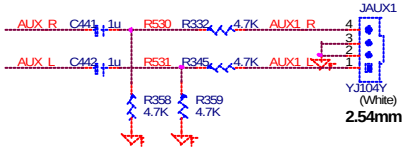


FRONT AUDIO

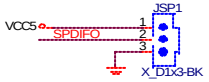
CD IN



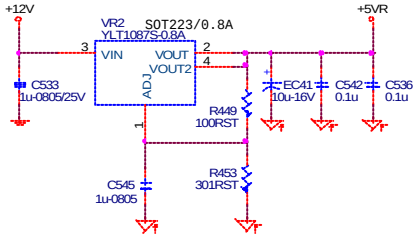
AUX IN



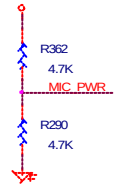
SPDIF CONNECTOR



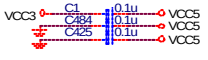
AUDIO CODE REGULATORS



MIC Power



COPPER



MSI

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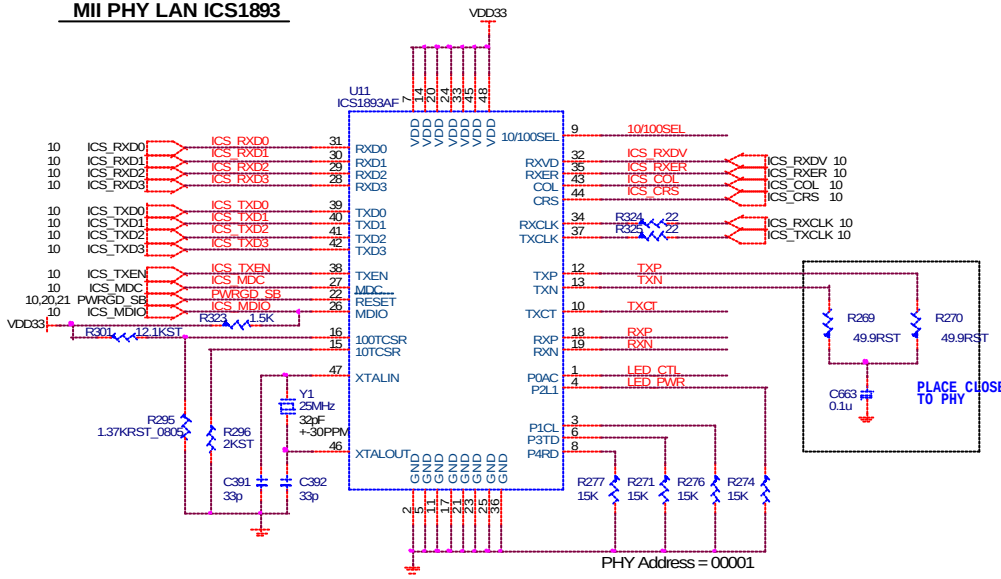
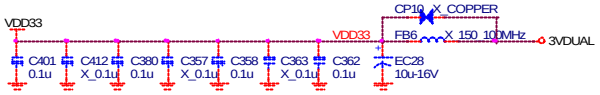
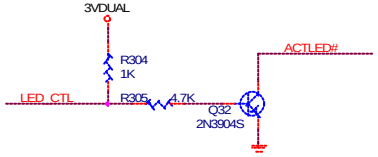
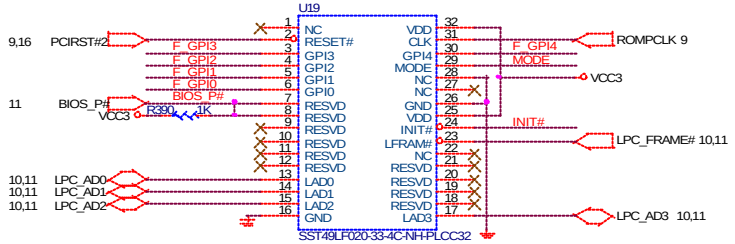
MII PHY LAN ICS1893





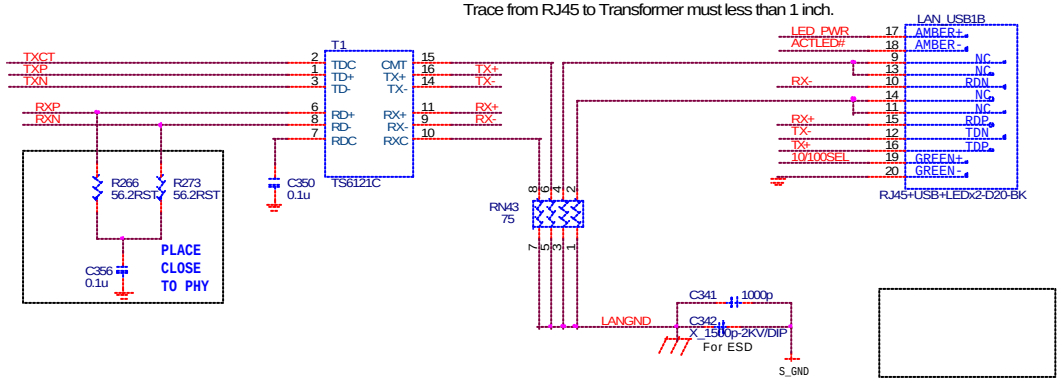


LPC Flash EEPROM

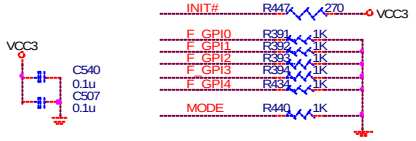


RJ45 Connector

Trace from RJ45 to Transformer must less than 1 inch.



EEPROM Strapping Resistors



Interface MODE Selection		
HIGH	Programmer mode	
LOW	LPC mode	Default

MICRO-STAR INt'L CO., LTD.

Title: MII LAN ICS1893AF & LPC Flash EEPROM

Size | Document Number: (MS-6597) | Rev: 0B

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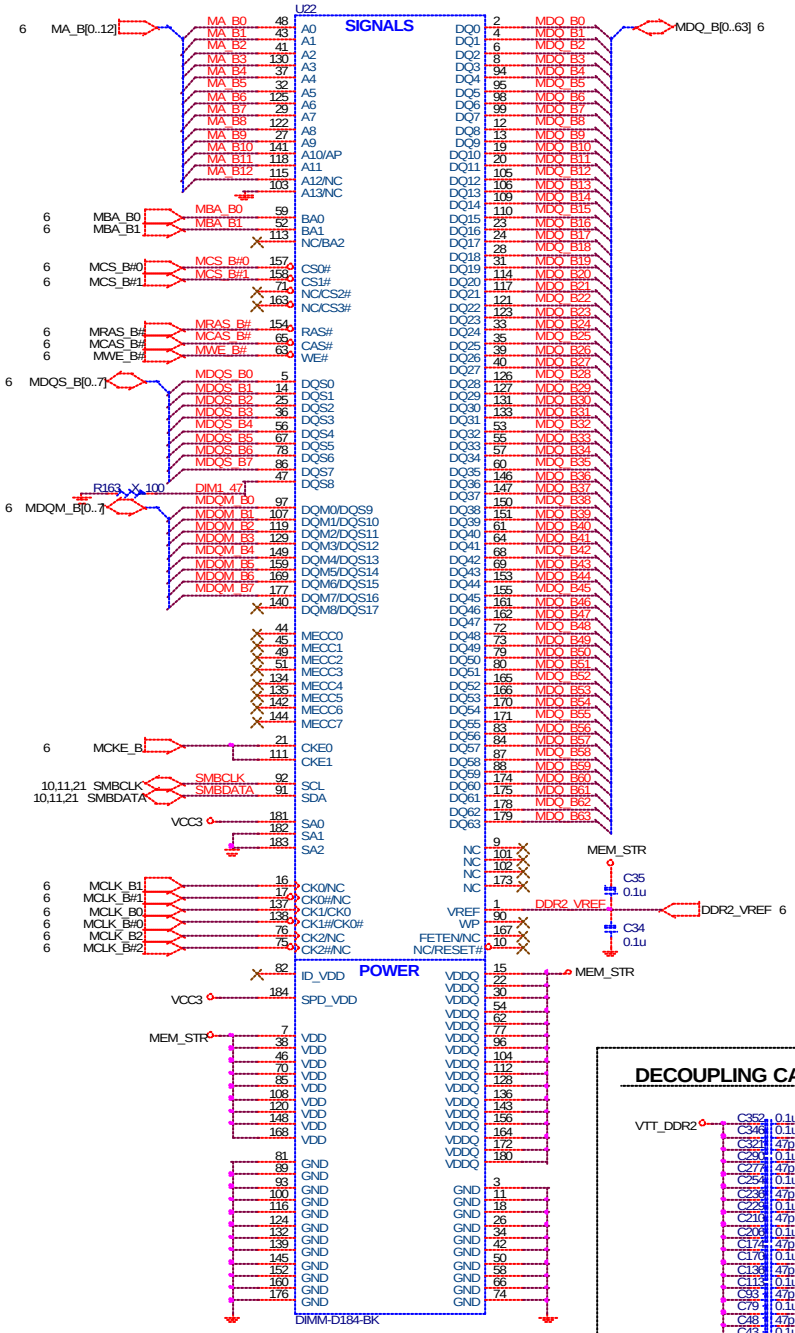
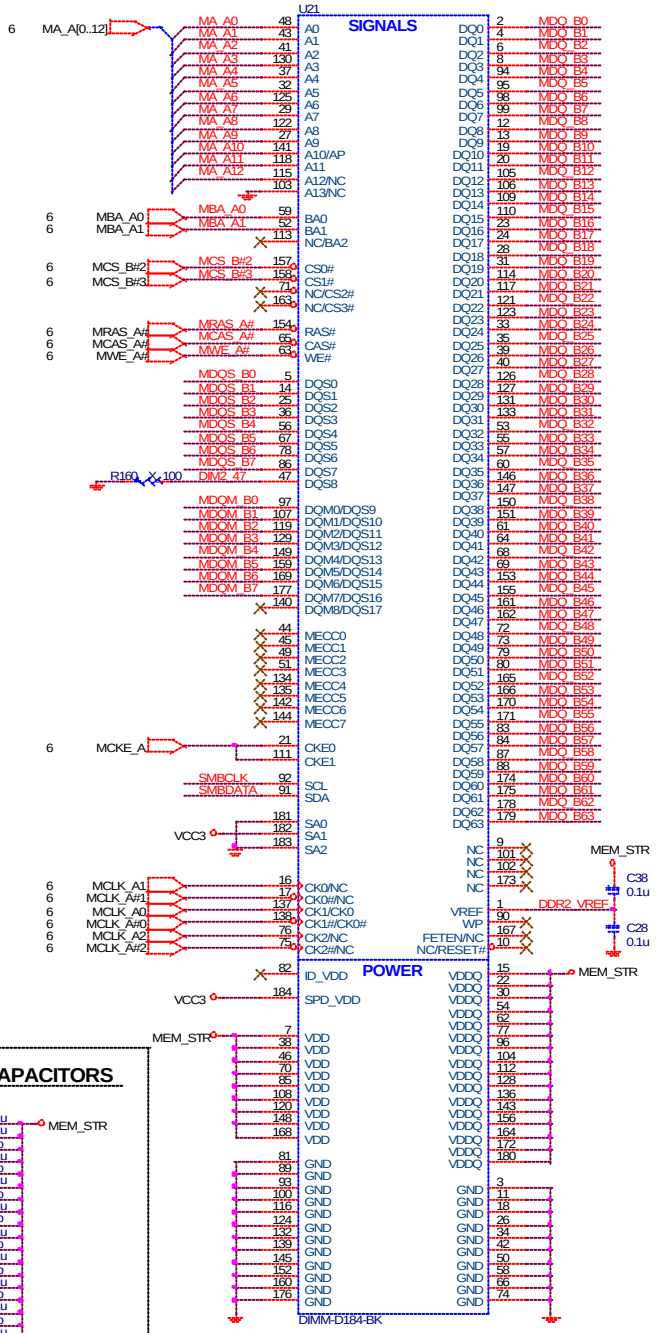
DDR DIMM1



ADDR.=1010001B

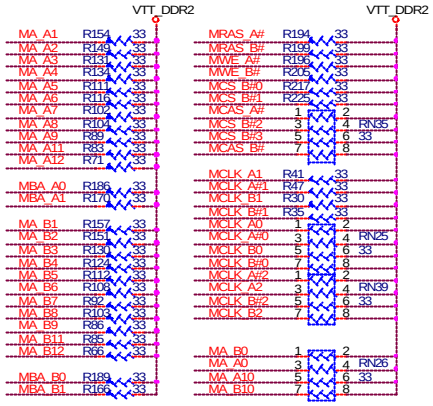
DDR DIMM2



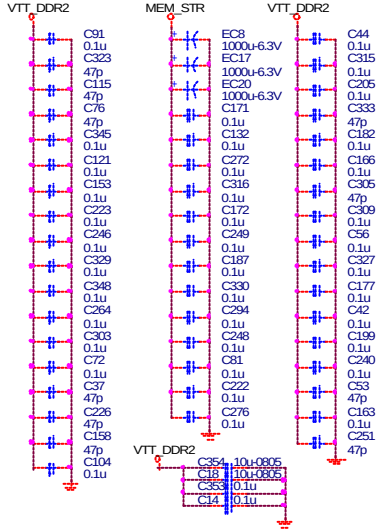
ADDR.=1010010B

DECOUPLING CAPACITORS

DDR Terminational Resistors



DECOUPLING CAPACITORS



Place these decoupling capacitors close to VTT_DDR termination resistors.

One decoupling capacitor for each R-pack.

MICRO-STAR INt'L CO., LTD.

Title	DDR DIMM 1 & 2	
Size	Document Number (MS-6597)	Rev 0B
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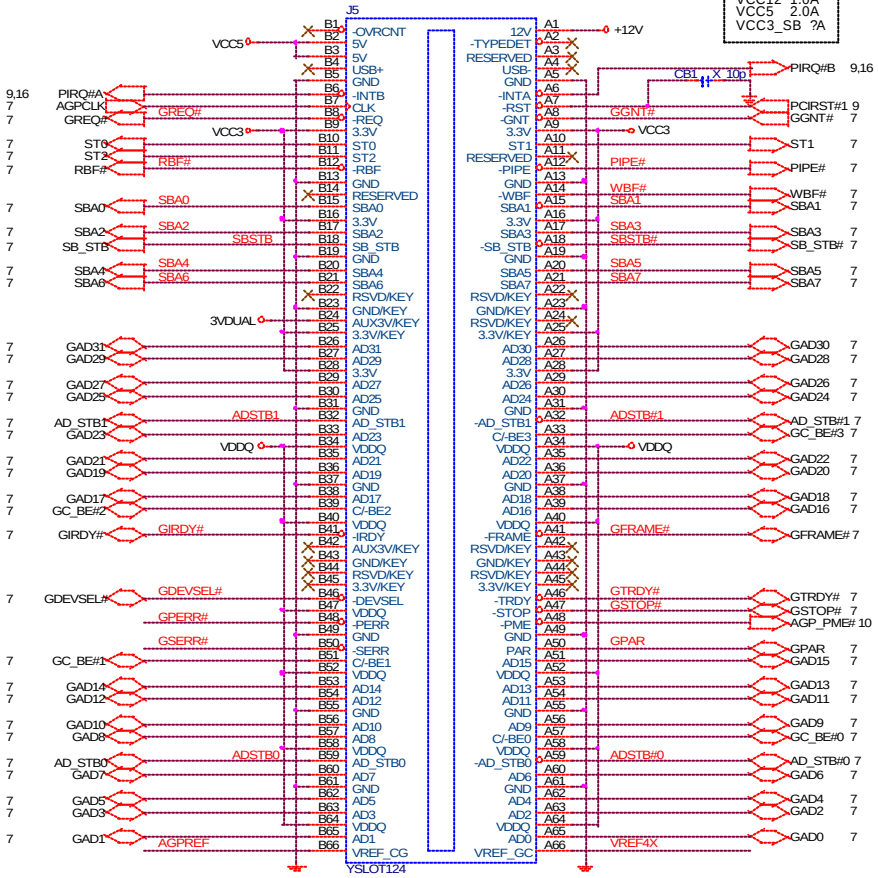
AGP 1.5V 2X/4X SLOT(AGP VER:2.0 COMPLY)

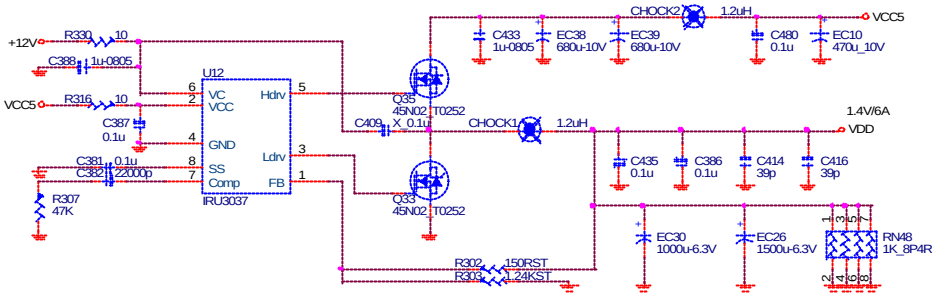
VCC5 = 60mils trace / 15 mils space

AGP Slot Imax

VCCg	8.0A
VCC3	6.0A
VCC12	1.0A
VCC5	2.0A
VCC3_SB	?A



LDT Voltage Regulator

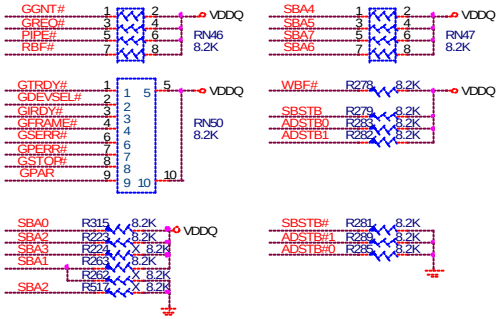


Host Freq.	SBA1	SBA0
100MHz	0	1
133MHz	1	1

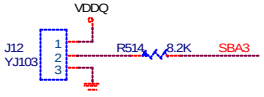
0 = Use values stored in ROM tables.
1 = AUTO detect by reading SBA[1:0]

FSB Set.	SBA2
ROM	0
AUTO	1

AGP TERMINATION RESISTORS

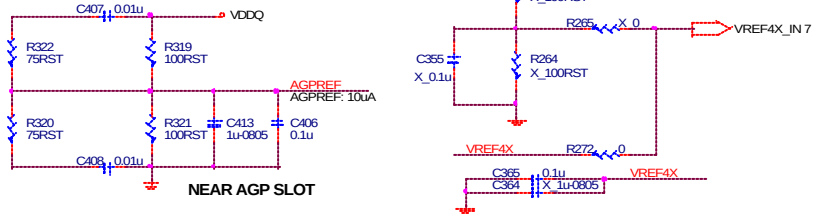


FSB Mode	SBA3	J12
100MHz	0	2-3
133MHz	1	1-2

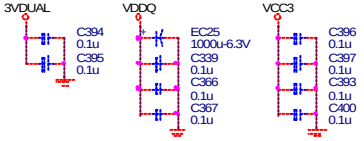


LESS 10MILS STUB TRACE LENGTH MUST BE FOLLOWING.
Place these resistors between PCI and AGP slot

AGP SIGNAL REFERENCE CIRCUIT



AGP SLOT DECOUPLING CAPACITORS



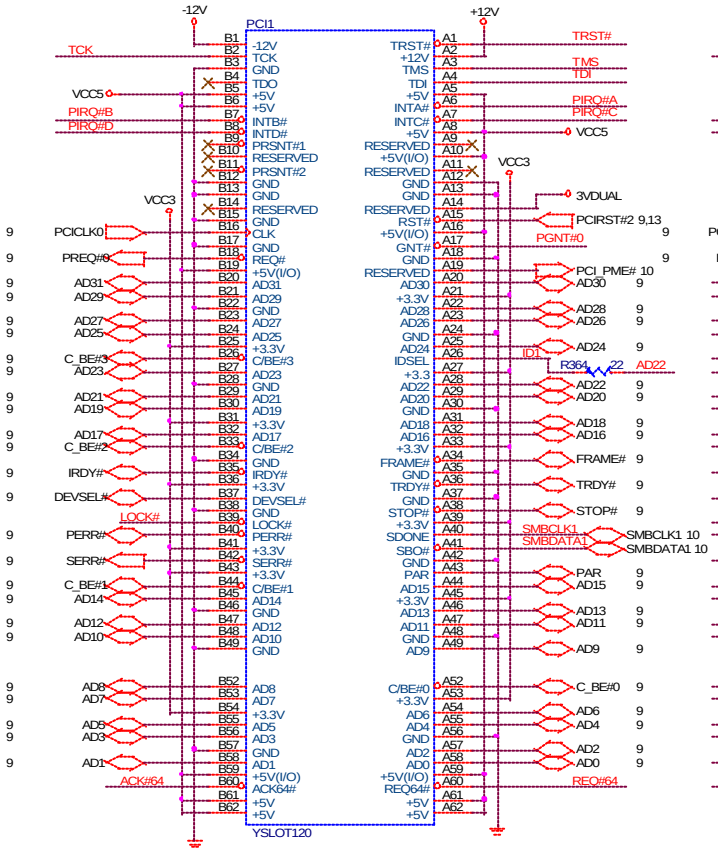
MICRO-STAR INt'L CO., LTD.

Title: AGP 1.5V SLOT,LDT Voltage Regulator & COM2

Size | Document Number: (MS-6597) | Rev: 0B

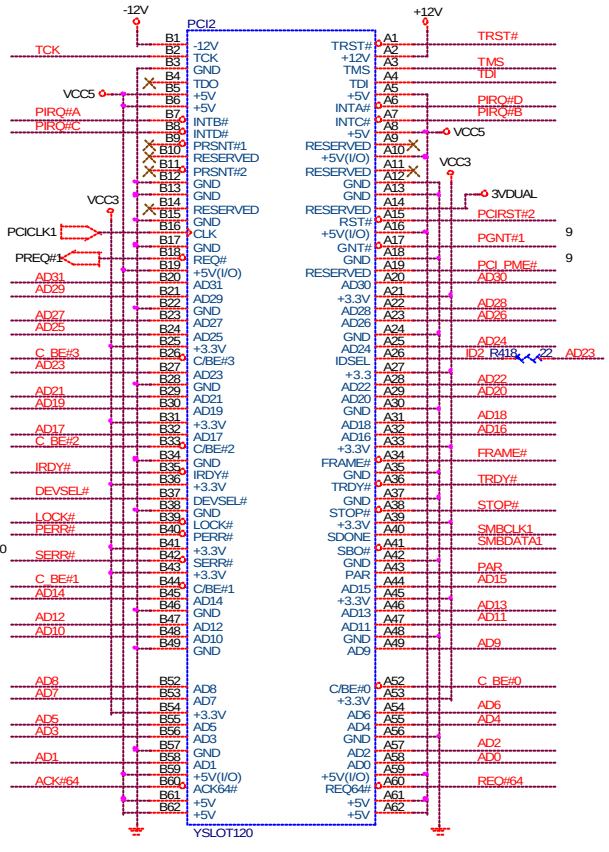
Date: Tuesday, October 22, 2002 | Sheet 15 of 25

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



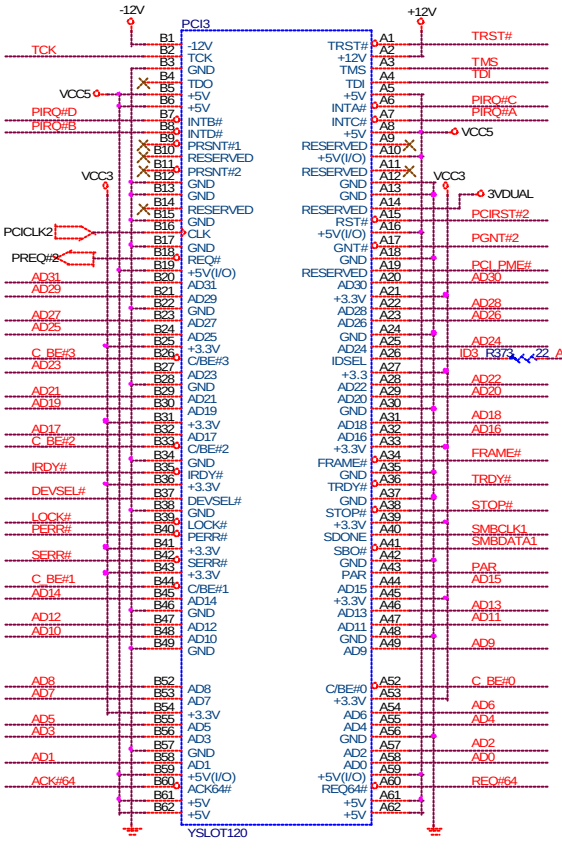
IDSEL = AD22
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



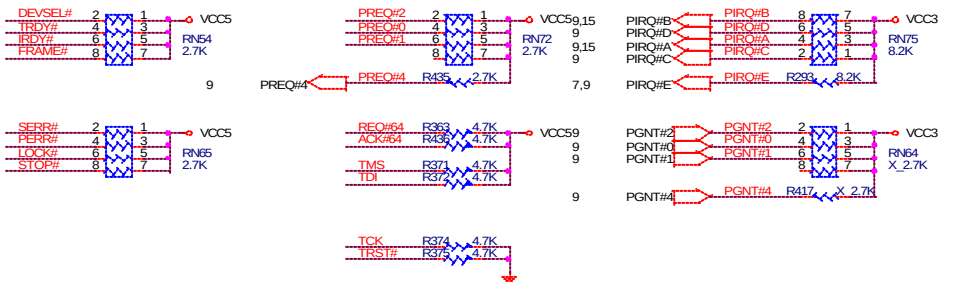
IDSEL = AD23
MASTER = PREQ#1
PIRQ#D

PCI SLOT 3 (PCI VER: 2.2 COMPLY)

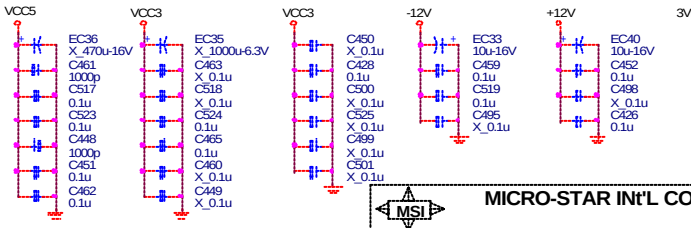


IDSEL = AD24
MASTER = PREQ#2
PIRQ#C

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



MSI **MICRO-STAR INt'L CO., LTD.**

Title: PCI 1& 2 & 3 Slots

Size | Document Number: (MS-6597) | Rev: 0B

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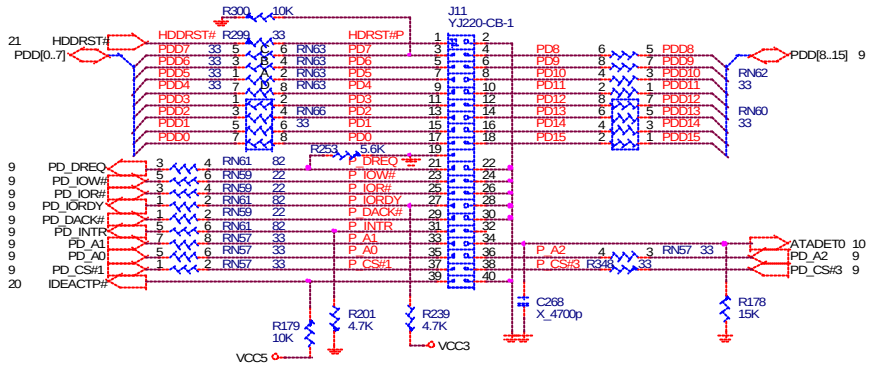
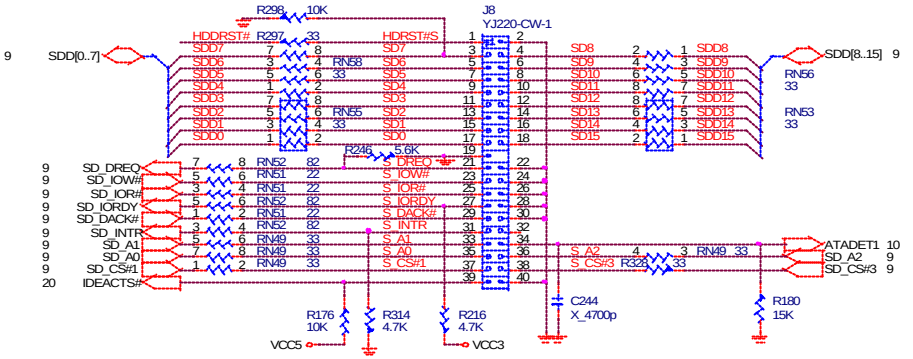
ATA 33/66/100 IDE Connectors

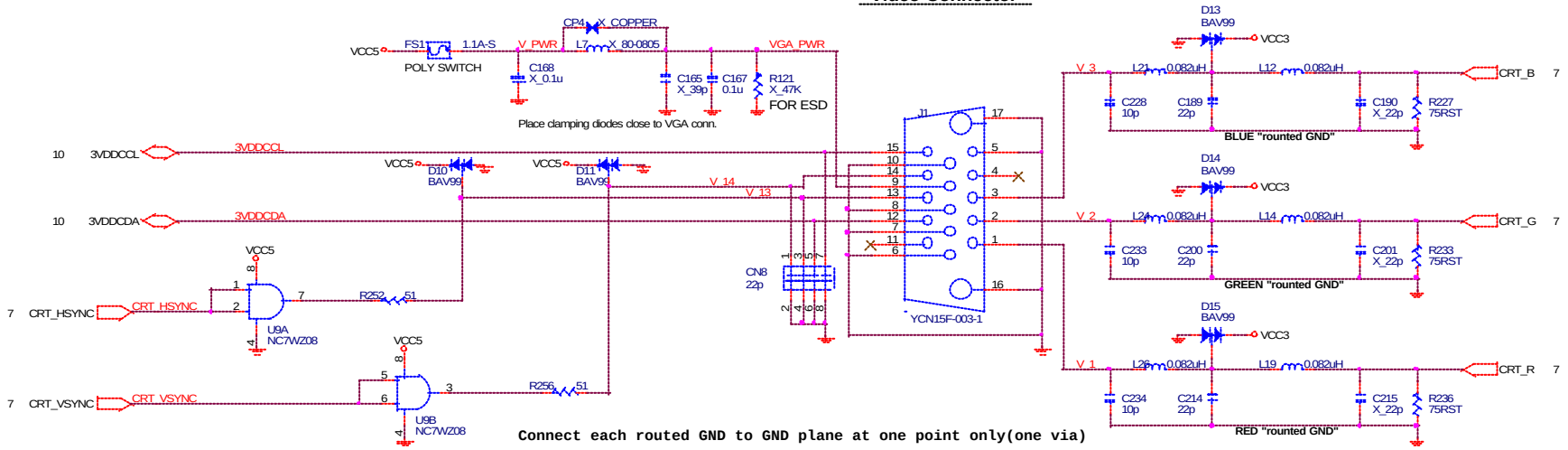
PRIMARY IDE BLOCK

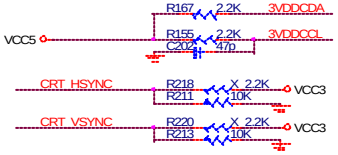


SECONDARY IDE BLOCK



Video Connector





Function		LDT internal terminations		CPU Type strapping	
		Enable	Disable	Intel	AMD
HSYNC	Buffered	0	1	X	X
	Non-Buffered	0*	1	X	X
VSYNC	Buffered	X	X	1	0
	Non-Buffered	X	X	1	0*

Use 10K pu/pd if VSYNC/HSYNC are buffered;
use 2.2K if VSYNC/HSYNC are un-buffered.
* Default

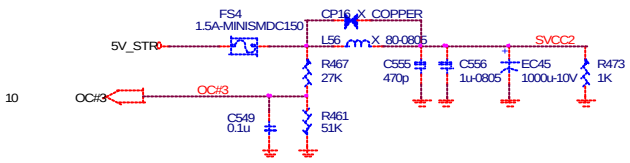
MICRO-STAR INt'L CO., LTD.

Title: ATA33/66/100 IDE & VIDEO Connectors

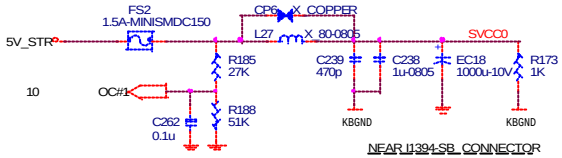
Size | Document Number: (MS-6597) | Rev: 0B

Date: Tuesday, October 22, 2002 | Sheet 17 of 25

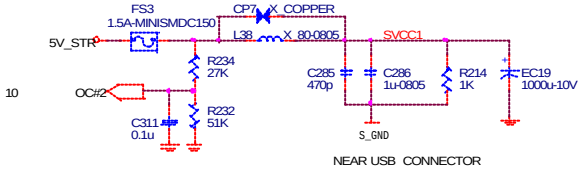
POWER CIRCUIT FOR LAN_USB PORT 4,5



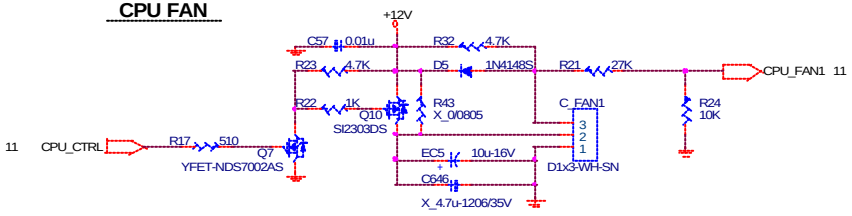
POWER CIRCUIT FOR I1394_USB PORT 0,1



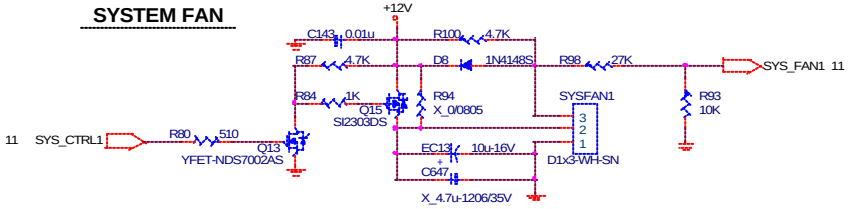
POWER CIRCUIT FOR USB PORT 0,1,2,3



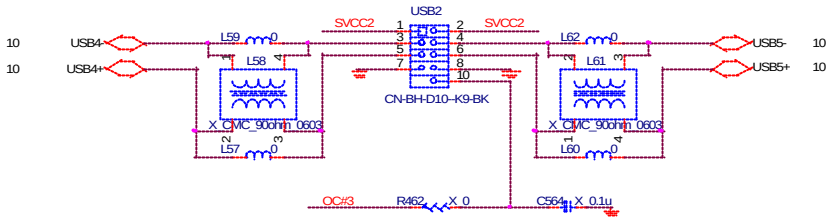
CPU FAN



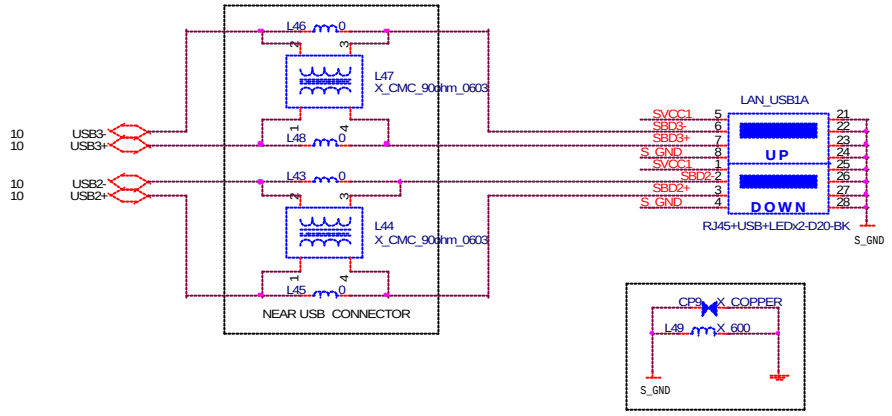
SYSTEM FAN



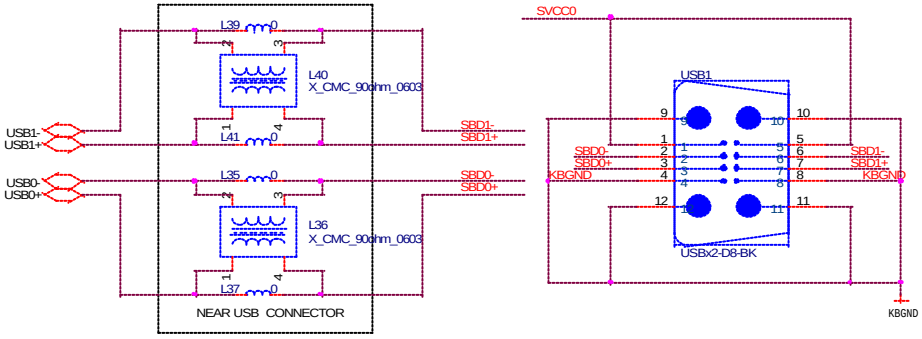
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



REAR PANEL LAN_USB CONNECTOR FOR USB PORT 2,3



REAR PANEL I1394_USB CONNECTOR FOR USB PORT 0,1



MSI

MICRO-STAR INt'L CO., LTD.

Title: FAN & USB Connectors

Size	Document Number	Rev
	(MS-6597)	0B

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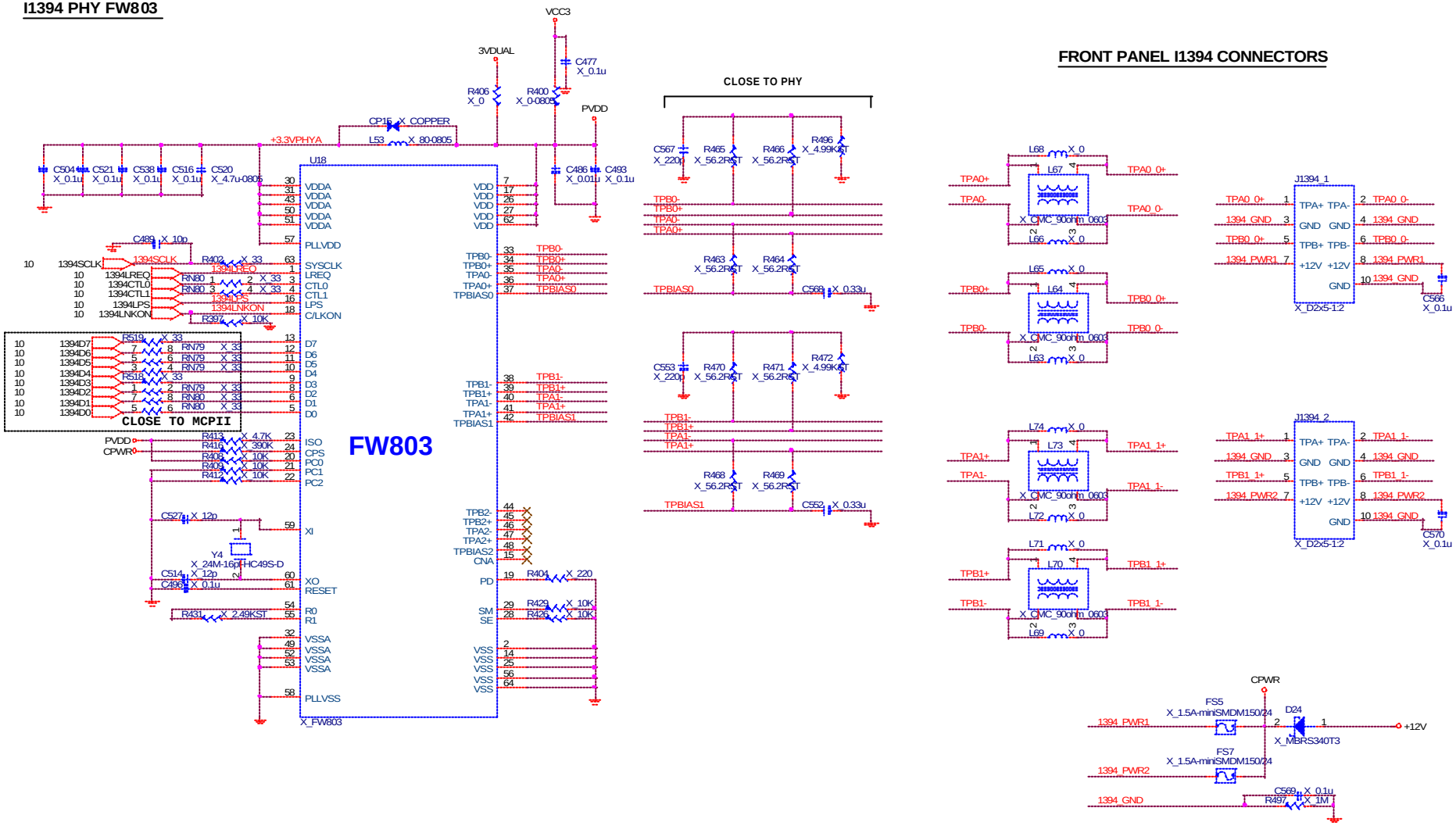
I1394 PHY FW803



FRONT PANEL I1394 CONNECTORS

MICRO-STAR INt'L CO., LTD.

Title: FW803(1394 PHY) & Connectors

Size | Document Number: (MS-6597) | Rev: 0B

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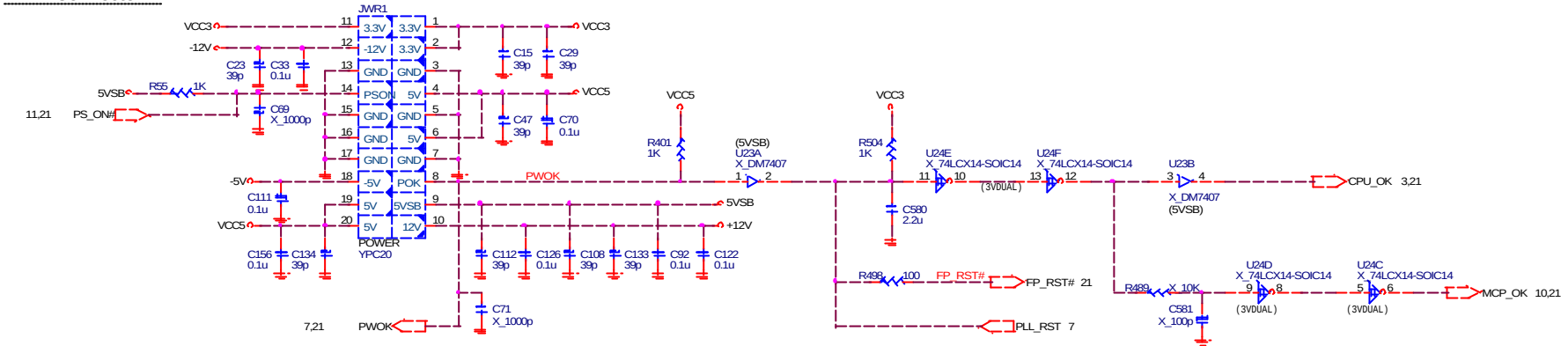
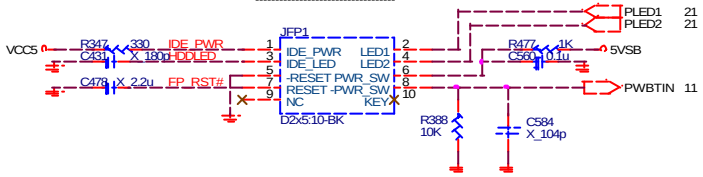
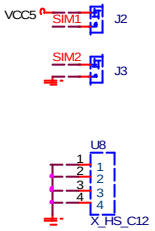
ATX Connector



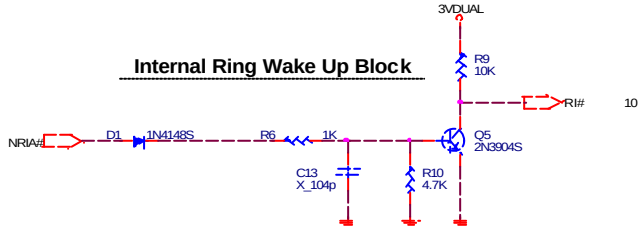
Front Panel



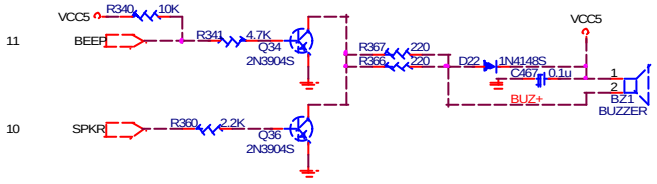
Simulation



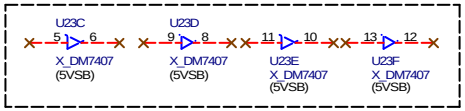
Internal Ring Wake Up Block



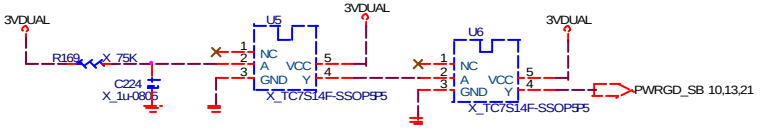
BUZZER



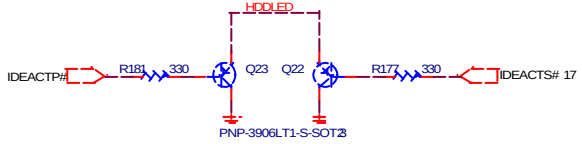
UNUSE LOGIC



RSMRST#



IDE LED



MICRO-STAR INt'L CO., LTD.

Title: ATX Connector & Front Panel

Size | Document Number: (MS-6597) | Rev: 0B

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ACPI (MS5)

SEL0	5VUSB
H	2 MOSFET
L	1 MOSFET

**S50# pin function(Hi level = 5V)
same as 5VUSB(Hi level = 12V)

Low RDS ON MOSFET

Dual FootPrint

CHARGE PUMP VOLTAGE OUTPUT

FOR 3VSB OR 3VSTR SETTING BY SEL1

SEL1	VRAM	VRAM_2.5
H	3.3VDUAL	2.5V
TRI-STATE	3.3VSB	2.5V
L	3.3VSTR	1.25V

System Decoupling Capacitors

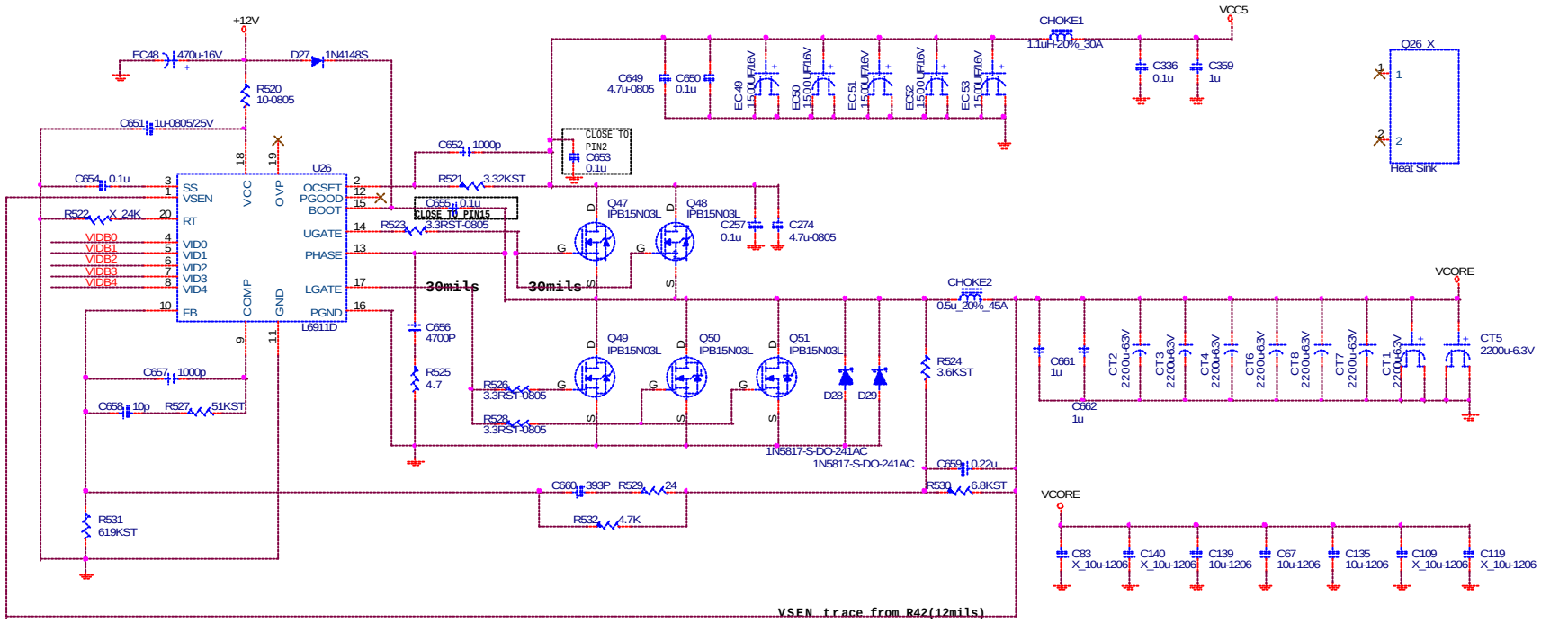
2.5V POWER TRANSLATOR

To DDR Clock Buffer

VCC2.5 POWER PLANE

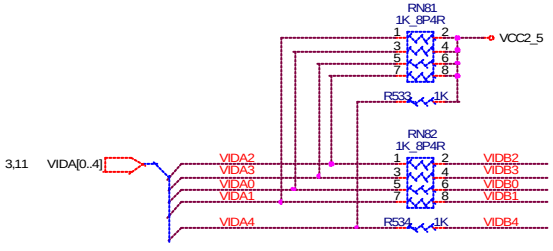
MICRO-STAR INt'L CO., LTD.

Title	System & DDR Regulators	
Size	Document Number (MS-6597)	Rev 0B
Date: Tuesday, October 22, 2002	Sheet 21 of 25	



VID4	VID3	VID2	VID1	VID0	VDC(V)
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475

VID4	VID3	VID2	VID1	VID0	VDC(V)
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850
1	1	1	1	1	OFF



MSI **MICRO-STAR INt'L CO., LTD.**

Title: VRM 9.0 - ST6911D

Size | Document Number: (MS-6597) | Rev: 0B

Date: Tuesday, October 22, 2002 | Sheet 22 of 25

MCP

GPIO Pin	Type	Function
GPIO 0	I	PCI_REQ#4 (multifunction pin)
GPIO 1	O	PCI_GNT#4 (multifunction pin)
GPIO 2	I/O	PCI_PERR# (multifunction pin)
GPIO 3	I	PCI_IRQ#E (multifunction pin)
GPIO 4	I	MII_RXER (multifunction pin)
GPIO 5	I	Pull up through 8.2K ohms (LPC_DRQ#1)
GPIO 6	I	USB_OC1# (multifunction pin)
GPIO 7	I	USB_OC2# (multifunction pin)
GPIO 8	I	USB_OC2# (multifunction pin)
GPIO 9	I	USB_OC3# (multifunction pin)
GPIO 10	I	USB_OC3# (multifunction pin)
GPIO 11	O	AC_SDIN1 (multifuntion pin)
GPIO 12	I	A20GATE (multifuntion pin)
GPIO 13	I	Pull up through 10K ohms (SPDIF)
GPIO 14	I/O	Unused
GPIO 15	I/O	Unused
GPIO 16	I/O	Unused
GPIO 17		Reserve
GPIO 18	I/O	Unused
GPIO 19	I	SIO_PME# (multifunction pin)
GPIO 20	O	SLP_S1# (multifunction pin)
GPIO 21	I	Pull up through 4.7K ohms (SIO_SMI#)
GPIO 22	I	THERM# (multifuntion pin)
GPIO 23	I	INTRUDER#
GPIO 24	I	RI# (multifuntion pin)
GPIO 25	I	KBRST# (multifuntion pin)
GPIO 26	O	SUSCLK (multifuntion pin)
GPIO 27	I	AGP_PME# (multifuntion pin)
GPIO 28	I	Primary IDE ATA66/100 detection (ATADET0)
GPIO 29	I	GPIO29 (Clear password indicator , Active Low)
GPIO 30	I	Secondary IDE ATA66/100 detection (ATADET1)
GPIO 31	I	GPIO31 (CMOS Clear , Active Low)
GPIO 32	O	Unused
GPIO 33	O	Unused
GPIO 34	O	Unused
GPIO 35	I	Unused
GPIO 36~38	I	Pull up through 10K ohms to 3VDUAL
GPIO 48	I	Pull up through 4.7K ohms to VCC3
GPIO 49	I	Pull up through 4.7K ohms to VCC3
SPIO 0	I/O	SM_CLK0 (multifuntion pin)
SPIO 1	I/O	SM_DATA0 (multifuntion pin)
SPIO 2	I/O	SM_CLK1 (multifuntion pin)
SPIO 3	I/O	SM_DATA1 (multifuntion pin)
SPIO 4	I/O	DDC_CLK (multifuntion pin)
SPIO 5	I/O	DDC_DATA (multifuntion pin)
SPIO 6	I	Pull up through 4.7K ohms (SMB_ALERT#)

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	INTA# INTB# INTC# INTD#	PCI_REQ#0 PCI_GNT#0	AD22	PCICLK0	MCP/AB20 (PCI_CLK0)
PCI Slot 2	INTD# INTA# INTB# INTC#	PCI_REQ#1 PCI_GNT#1	AD23	PCICLK1	MCP/AB18 (PCI_CLK1)
PCI Slot 3	INTC# INTD# INTA# INTB#	PCI_REQ#2 PCI_GNT#2	AD24	PCICLK2	MCP/AB12 (PCI_CLK2)

LPC Super I/O

GPIO Pin	Type	Function
GPIO 10	O	Unused
GPIO 11	O	Unused
GPIO 12	O	Unused
GPIO 13	O	Unused
GPIO 14	O	Unused
GPIO 15	O	Unused
GPIO 16	O	Unused
GPIO 17	O	Unused
GPIO 20	O	Unused
GPIO 21	I	SMBCLK
GPIO 22	I/O	SMBDATA
GPIO 23	O	Unused
GPIO 24	O	Unused
GPIO 25	I	BIOS Protect , Active Low
GPIO 26	O	Unused
GPIO 27	O	Floopy Driven Density Select , Active Low
GPIO 30	I	SLP_S3#
GPIO 31	O	PS_ON#
GPIO 32	O	Unused
GPIO 33	O	Unused
GPIO 34	O	PWR_FAN , High to turn ON FAN
GPIO 35	O	Unused

Flash ROM

GPIO Pin	Type	Function
GPI 0	I	Pull down through 1K ohms (unused)
GPI 1	I	Pull down through 1K ohms (unused)
GPI 2	I	Pull down through 1K ohms (unused)
GPI 3	I	Pull down through 1K ohms (unused)
GPI 4	I	Pull down through 1K ohms (unused)

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2	1010010B	MCLK_A0/MCLK_A0# MCLK_A1/MCLK_A1# MCLK_A2/MCLK_A2#
DIMM 1	1010001B	MCLK_B0/MCLK_B0# MCLK_B1/MCLK_B1# MCLK_B2/MCLK_B2#

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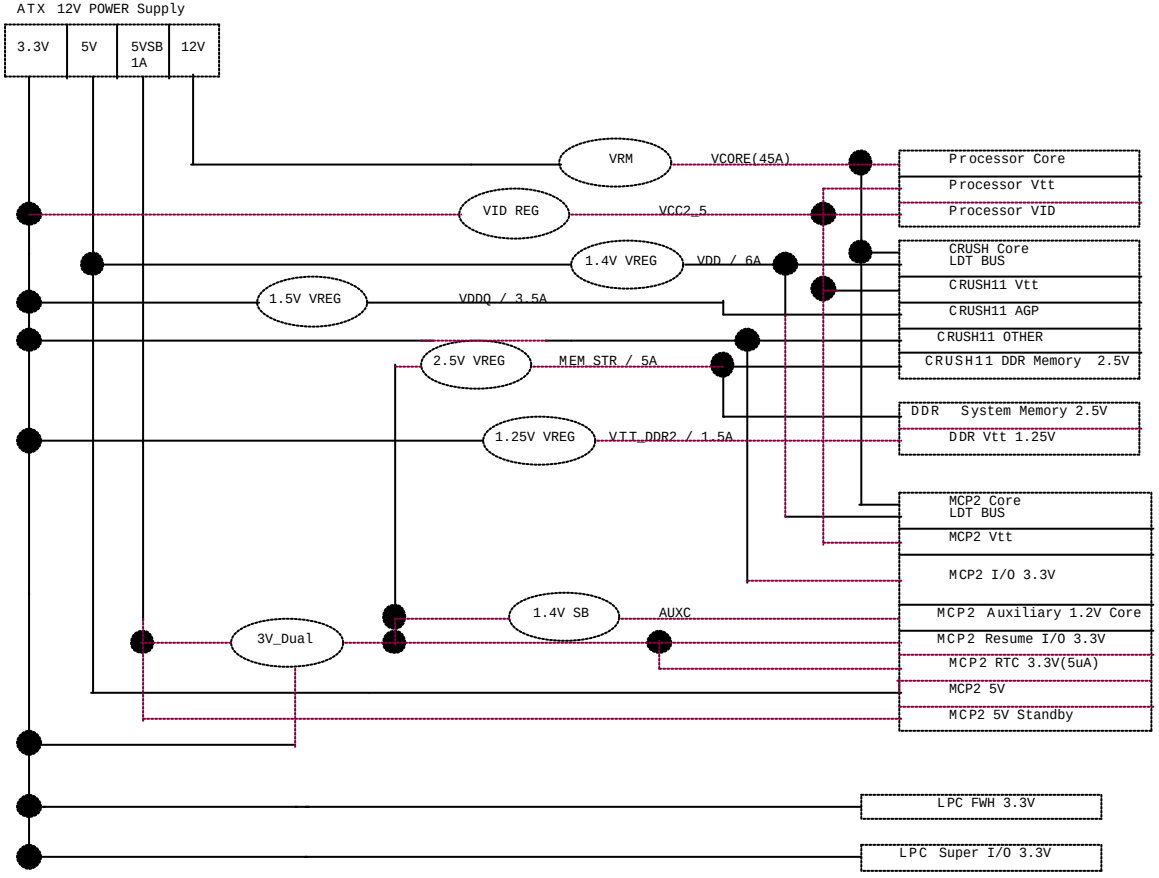
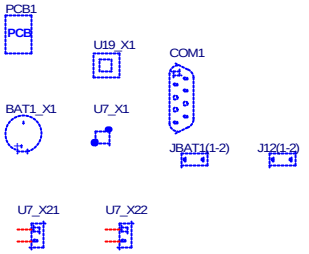
Power Delivery Map



Auto-BOM Manual Parts



JUMPER SETTING

CMOS CLEAR JUMPER

JBAT1	CMOS Status
1 - 2	Normal
2 - 3	Clear CMOS

FSB MODE JUMPER

FSB Mode	SBA3	J12
100MHz	0	2-3
133MHz	1	1-2

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0A-0B

CHANGE ALL I/O PLACEMENT.

Page:7 - Change MH7 pin5 from 'GND' to KBGND.

Page:8 - Add C648.

Page:9 - Del R369 . Add RN79. Add R513. Net 'AUXC' need trace wide ≧20mils.

Page:10- R419 connect to 'VCC3'.Add R509 connect to "SPDIFO".Add R515 & R516 for 'VDD_USB'(option).

Page:12- Place R401 for Audio. Add two 0O at 'SPDIFO'. Change placement of 'JCD1' & 'JAUX1' with 'EC31' & 'EC32'.

Page:13- Del U15 ,R349 from 'BOM'.

Page:15- Add 'J12' & 'R514'. Del U15 ,R349 from 'BOM'.

Page:17- R227, R233, R236 place close to VGA connector.

Page:18- Add C646, C647 for option.

Page:19- Del 'D18' & Add 'FS6', 'FS7'.Add CT14 at +12V.Change C489 connect to '1394SCLK' net. Change R402 from 0O to 33O.

Page:20- Change JFPT1 net. Del power button block.U23 remove from BOM.

Page:21- Add EC47 place near at 'Q9'. Change EC7 place close to 'C82'.Change 'D19' footprint from 1N4148S to SM5817.Place R147, R148 for 'MCP_OK' & 'CPU_OK'.Change Q31 Foot Print.

Page:22-'Q27', 'Q28'of 'S' pin need more VIA holes to 'GND'. Change library of 'CHOK1'& 'CHOK2'(DFM).

0B-0C

Page:4 - Change C123, C150, C68, C100, C80, C154, C144, C117, C61, C101, C60, C145, C63, C125, C148, C90, C94, C149, C74, C62, C103, C152, C151, C75, C147, C106, C99, C55, C102, C116 from 39p to 0.1U. C17, C26 change to NC.

Page:6 - Del R237, R230, R235, R249, R238, R240, R250, R251, R244, R247, R171, R168, RN37, RN36, RN32, RN33, RN30, RN27.

Page:9 - Del R515, R516. Change C492 from net "VDD_PLL_MCP" to "3VDUAL".

Page:10- R509 NC. Change R396 from 1K_1% to 909ohm_1%. Add R410. Change RN73, RN74, RN69 from 30ohm to 27ohm. Chnage C508, C509, C479, C485, C505, C509 from 10pf to 5pf.

Page:11- Del R62, R56, RT2 & Add "JCI1"(CHASSIS).

Page:12- Del R401, Internal Speaker.

Page:13- Change U19 from 4M Flash ROM to 2M.

Page:15- Change J5 'INTA#' from 'PIRQ#E' to 'PIRQ#B'.

Page:16- Del C463, C501, C495, C498.

Page:17- Change C190, C201, C215 from 10pf to 22pf. Change R252, R256 from 33ohm to 52ohm.

Page:18- Change EC18 from 'KBGND' to 'GND'. L58, L61, L47, L44, L40, L36 NC. Add L59, L57, L62, L60, L46, L48, L43, L45, L39, L41, L35, L37 0ohm.

Page:19- All Del.

Page:20- Del R169, C224, U5, U6.

Page:21- Add R150, Q46. Change EC1 from 470U to 1000U. Del RN71, RN40, RN29, RN21, RN22, R114, R118, R129, Q18, Q19, Q20, EC16.

Page:22- Change Q25, Q28 from 15N03L to 10N03L. Del 'HEAT SINK'. Change CHOK1, CHOK2 from 0.8U to 1.1U.

Version

Page:22 - Change VID trace

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