Mars ZX3 SoC Module

User Manual

Purpose

The purpose of this document is to present the characteristics of Mars ZX3 SoC module to the user, and to provide the user with a comprehensive guide to understanding and using the Mars ZX3 SoC module.

Summary

This document first gives an overview of the Mars ZX3 SoC module followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Number	Name
Product	MA-ZX3	Mars ZX3 SoC Module

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1 Overview

1.1 General

1.1.1 Introduction

The Mars ZX3 SoC module combines the Xilinx Zynq®-7020 All Programmable SoC (System-on-Chip) device with fast DDR3 SDRAM, NAND flash, quad SPI flash, a Gigabit Ethernet PHY, USB 2.0 On-The-Go PHY and a real-time clock, forming a complete and powerful embedded processing system.

The SO-DIMM form factor allows space-saving hardware designs and quick and simple integration of the module into the target application.

The use of the Mars ZX3 SoC module, in contrast to building a custom SoC hardware, significantly reduces development effort and redesign risk and improves time-to-market for the embedded system.

Together with Mars base boards, the Mars ZX3 SoC module allows the user to quickly build a system prototype and start with application development.

The Enclustra Build Environment [15] is available for the Mars ZX3 SoC module. This build system allows the user to quickly set up and run Linux on any Enclustra SoC module. It allows the user to choose the desired target and download all the required binaries, such as bitstream and FSBL (First Stage Boot Loader). It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

1.1.2 Warranty

Please refer to the General Business Conditions, available on the Enclustra website [1].

1.1.3 RoHS

The Mars ZX3 SoC module is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.1.4 Disposal and WEEE

The Mars ZX3 SoC module must be properly disposed of at the end of its life.

The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Mars ZX3 SoC module.

1.1.5 Safety Recommendations and Warnings

Mars modules are not designed to be "ready for operation" for the end-user. These can only be used in combination with suitable base boards. Proper configuration of the hardware before usage is required.

Ensure that the power supply is disconnected from the board before inserting or removing the Mars ZX3 SoC module, connecting interfaces, replacing SD cards and batteries, or connecting jumpers.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage; overvoltage on power or signal lines can also cause permanent damage to the module.

Warning!

Use the Mars ZX3 SoC module only with base boards designed for the Enclustra Mars module family. Inserting the Mars ZX3 SoC module into a SO-DIMM connector designed for memory (e.g. a computer main board) may damage the module and the carrier board.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Please ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Mars ZX3 SoC module is a Class A product and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Features

- Xilinx Zynq® -7020 All Programmable SoC, CLG484 package
  - Dual ARM® Cortex™-A9 MPCore™with CoreSight™ and NEON™ extension
  - Xilinx Artix-7 28 nm FPGA fabric
- 108 user I/Os up to 3.3 V
  - 12 ARM peripheral I/Os (SPI, SDIO, CAN, I2C, UART) shared with FPGA I/Os
  - 96 FPGA I/Os (single-ended, differential or analog)
- Up to 1 GB DDR3 SDRAM
- 512 MB NAND flash
- 64 MB quad SPI flash
- Gigabit Ethernet
- USB 2.0 On-The-Go (OTG)
- Real-time clock
- SO-DIMM form factor (30 × 67.6 mm, 200 pins)
- The module can be operated using a single 3.3 V supply voltage

1.3 Deliverables

- Mars ZX3 SoC module
- Mars ZX3 SoC module documentation, available via download:
  - Mars ZX3 SoC Module User Manual (this document)
  - Mars ZX3 SoC Module Reference Design [2]
  - Mars ZX3 SoC Module IO Net Length Excel Sheet [3]
  - Mars ZX3 SoC Module FPGA Pinout Excel Sheet [4]
  - Mars ZX3 SoC Module User Schematics (PDF) [5]
  - Mars ZX3 SoC Module Known Issues and Changes [6]
  - Mars ZX3 SoC Module Footprint (Altium, Eagle, Orcad and PADS) [7]
  - Mars ZX3 SoC Module 3D Model (PDF) [8]
  - Mars ZX3 SoC Module STEP 3D Model [9]
  - Module Pin Connection Guidelines [10]
  - Mars Master Pinout [11]
  - Enclustra Modules Heat Sink Application Note [17]
  - Enclustra Build Environment [15] (Linux build environment; refer to Section 1.4.2 for details)

1.4 Accessories

1.4.1 Reference Design

The Mars ZX3 SoC module reference design features an example configuration for the Zynq-7000 SoC device, together with an example top level HDL file for the user logic.

A number of software applications are available for the reference design, that show how to initialize the peripheral controllers and how to access the external devices. Pre-compiled binaries are included in the archive, so that the user can easily check that the hardware is functional.

The reference design can be downloaded from the Enclustra download page [2].

1.4.2 Enclustra Build Environment

The Enclustra Build Environment [15] enables the user to quickly set up and run Linux on any Enclustra SoC module. It allows the user to choose the desired target, and download all the required binaries, such as bitstream and FSBL. It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

The Enclustra Build Environment features a graphical user interface (GUI) and a command line interface (CLI) that facilitates the automatic build flow.

1.4.3 Mars PM3 Base Board

- Mars 200-pin SO-DIMM socket
- FMC LPC (Low Pin Count) connector (72 I/Os)
- 40-pin GPIO connector (optional, shared with FMC I/Os)
- RJ45 Gigabit Ethernet connector
- Mini HDMI connector for PCIe and LVDS applications (module dependent)
- Cypress FX3 USB 3.0 device controller (16-bit Slave-FIFO interface or 32-bit Slave-FIFO interface shared with FMC I/Os)
- USB 3.0 B device connector
- USB 2.0 A host connector
- Micro USB 2.0 B device connector with FTDI USB device controller
- Battery holder for the real-time clock
- microSD card holder
- Fan connector, various switches and LEDs
- Single 12 V DC supply voltage or USB bus-powered (with restrictions)
- Form factor: 100 × 72 mm (pico-ITX)

Please note that the available features depend on the equipped Mars module type.

1.4.4 Mars EB1 Base Board

- Mars 200-pin SO-DIMM socket
- 2 × Mini Camera Link connectors (requires FPGA support)
- HDMI 1.3 connector (requires FPGA support)
- 40-pin GPIO connector (Anios)
- 3 × 12-pin GPIO connector (two of the connectors with Pmod™ compatible pinout)
- RJ45 Ethernet connector
- USB 2.0 A host connector
- Micro USB 2.0 device connector (shared)
- FTDI USB 2.0 device controller with micro USB device connector
- microSD card holder
- Various switches and LEDs
- Integrated Xilinx compatible JTAG adapter

- Single 12 V DC supply voltage or USB bus-powered (with restrictions)
- Form factor: 120 × 80 mm

Please note that the available features depend on the equipped Mars module type.

1.5 Xilinx Tool Support

The SoC devices equipped on the Mars ZX3 SoC module are supported by the Vivado HL WebPACK Edition software, which is available free of charge. Please contact Xilinx for further information.

2 Module Description

2.1 Block Diagram

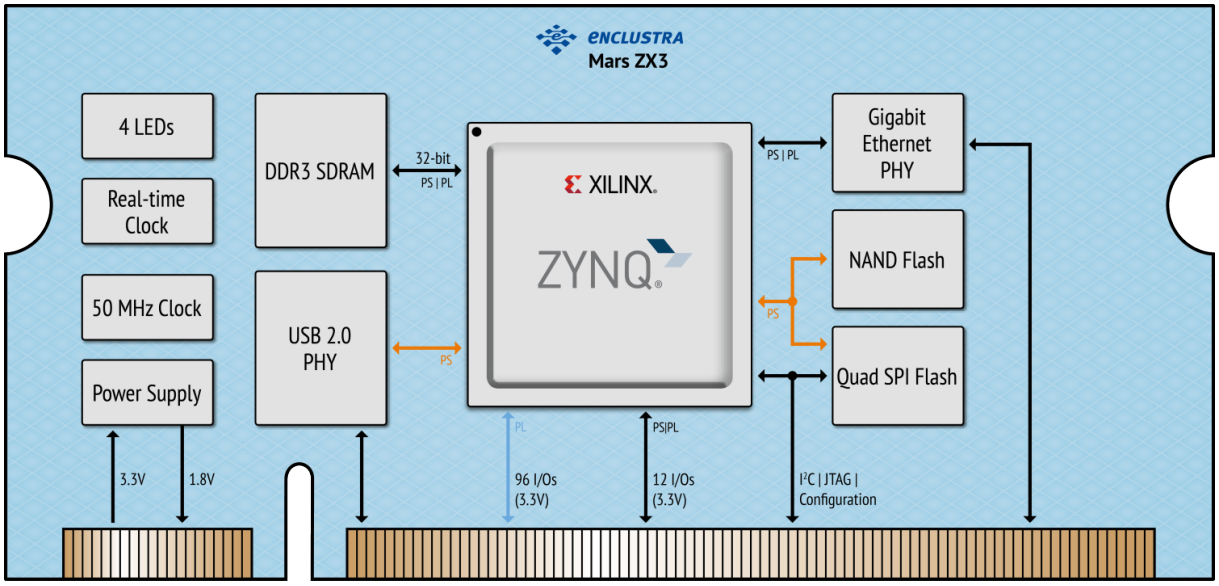

Figure 1: Hardware Block Diagram

The main component of the Mars ZX3 SoC module is the Xilinx Zynq-7000 SoC device. Most of its I/O pins are connected to the Mars module connector, making 108 user I/Os available to the user.

The SoC device can boot from the on-board QSPI flash, NAND flash or from an external SD card. For development purposes, a JTAG interface is connected to Mars module connector.

The available standard configurations include 512 MB NAND flash, a 64 MB quad SPI flash and 512 MB or 1 GB DDR3 SDRAM.

Further, the module is equipped with a Gigabit Ethernet PHY and a USB 2.0 OTG PHY, making it ideal for communication applications.

A real-time clock is available on the module and is connected to the global I2C bus.

On-board clock generation is based on a 33.33 MHz crystal oscillator.

The module can be operated using a single input supply of 3.3 V DC. All other necessary supply voltages are generated on-board. Some of these voltages are available on the Mars module connector to supply circuits on the base board.

Four LEDs are connected to the SoC pins for status signaling.

2.2 Module Configuration and Product Codes

Table 1 describes the available standard module configurations. Custom configurations are available; please contact Enclustra for further information.

Product Code	SoC	DDR3/DDR3L SDRAM	Temperature Range
MA-ZX3-20-1C-D9	XC7Z020-1CLG484C	512 MB	0 to +70° C
MA-ZX3-20-2I-D10	XC7Z020-2CLG484I	1024 MB	-40 to +85° C

Table 1: Standard Module Configurations

The product code indicates the module type and main features. Figure 2 describes the fields within the product code.

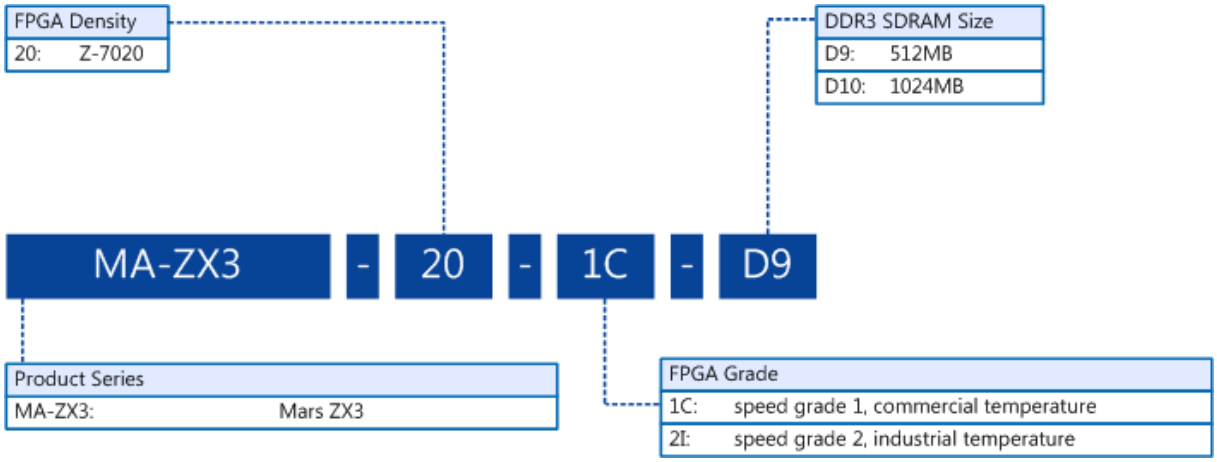

Figure 2: Product Code Fields

Please note that for the first revision modules or early access modules, the product code may not respect entirely this naming convention. Please contact Enclustra for details on this aspect.

2.3 Article Numbers and Article Codes

Every module is uniquely labeled, showing the article number and serial number. An example is presented in Figure 3.

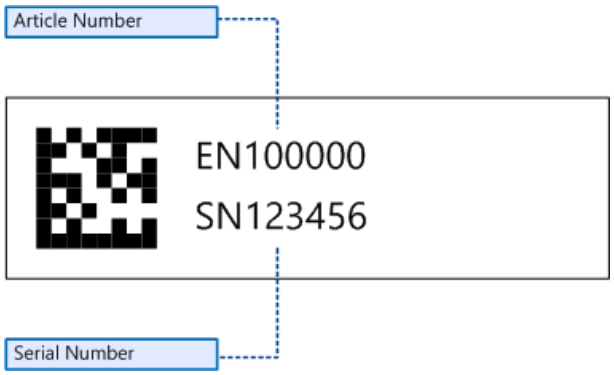

Figure 3: Module Label

The correspondence between article number and article code is shown in Table 2. The article code represents the product code, followed by the revision; the R suffix and number represent the revision number.

The revision changes and product known issues are described in the Mars ZX3 SoC Module Known Issues and Changes document [6].

Article Number	Article Code
EN100021	MA-ZX3-20-1C-D9-R2
EN100022	MA-ZX3-20-2I-D10-R2
EN100079	MA-ZX3-20-2I-D10-R3
EN100080	MA-ZX3-20-1C-D9-R3
EN100915	MA-ZX3-20-1C-D9-R4
EN100916	MA-ZX3-20-2I-D10-R4
EN101311	MA-ZX3-20-1C-D9-R5
EN101312	MA-ZX3-20-2I-D10-R5
EN101493	MA-ZX3-20-1C-D9-R6
EN101494	MA-ZX3-20-2I-D10-R6
EN101556	MA-ZX3-20-1C-D9-R6.1
EN101557	MA-ZX3-20-2I-D10-R6.1

Table 2: Article Numbers and Article Codes

2.4 Top and Bottom Views

2.4.1 Top View

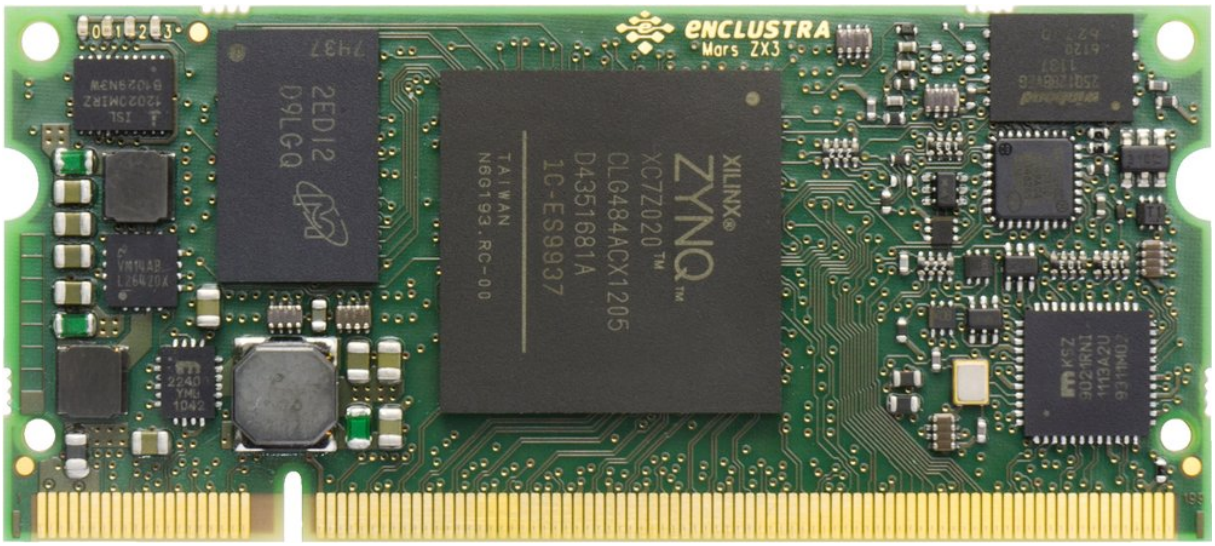

Figure 4: Module Top View

2.4.2 Bottom View

Figure 5: Module Bottom View

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.5 Top and Bottom Assembly Drawings

2.5.1 Top Assembly Drawing

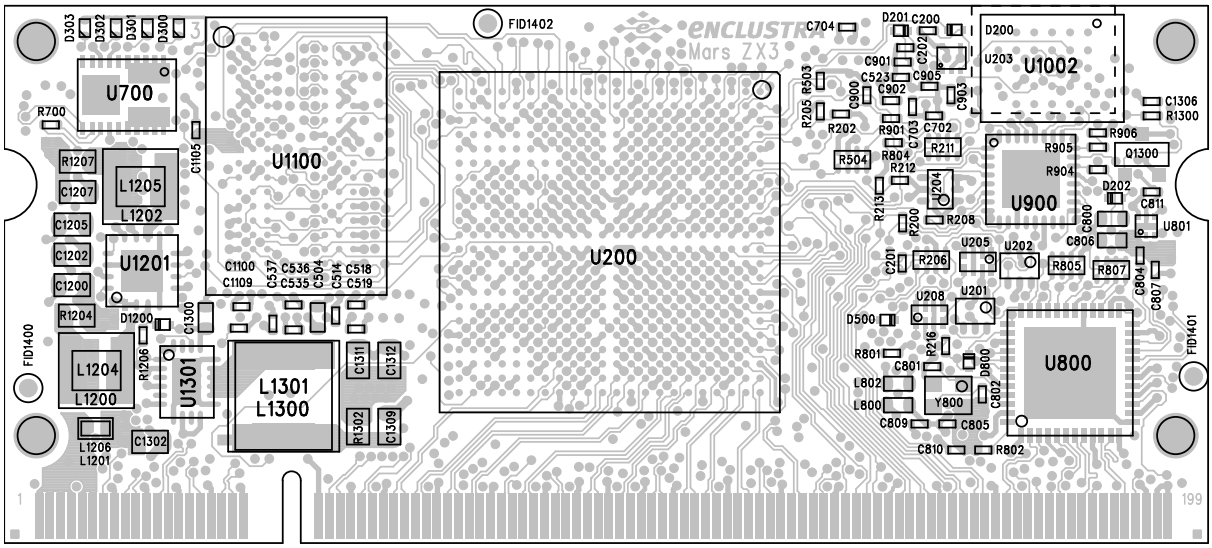

Figure 6: Module Top Assembly Drawing

2.5.2 Bottom Assembly Drawing

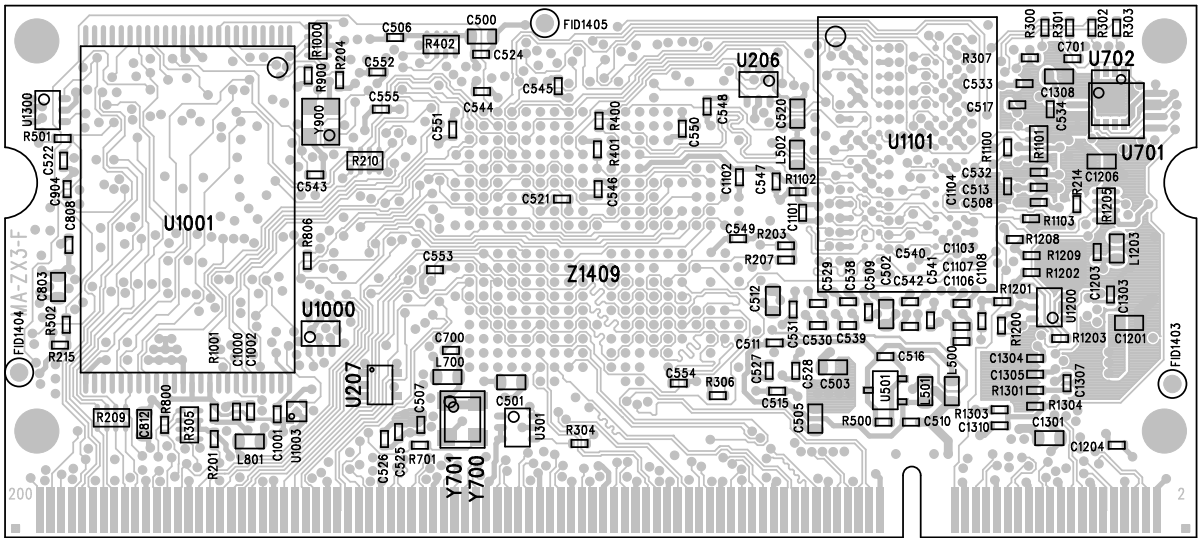

Figure 7: Module Bottom Assembly Drawing

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.6 Module Footprint

Figure 8 shows the dimensions of the module footprint on the base board.

The maximum component height under the module is dependent on the connector type - refer to Section 2.8 for detailed connector information.

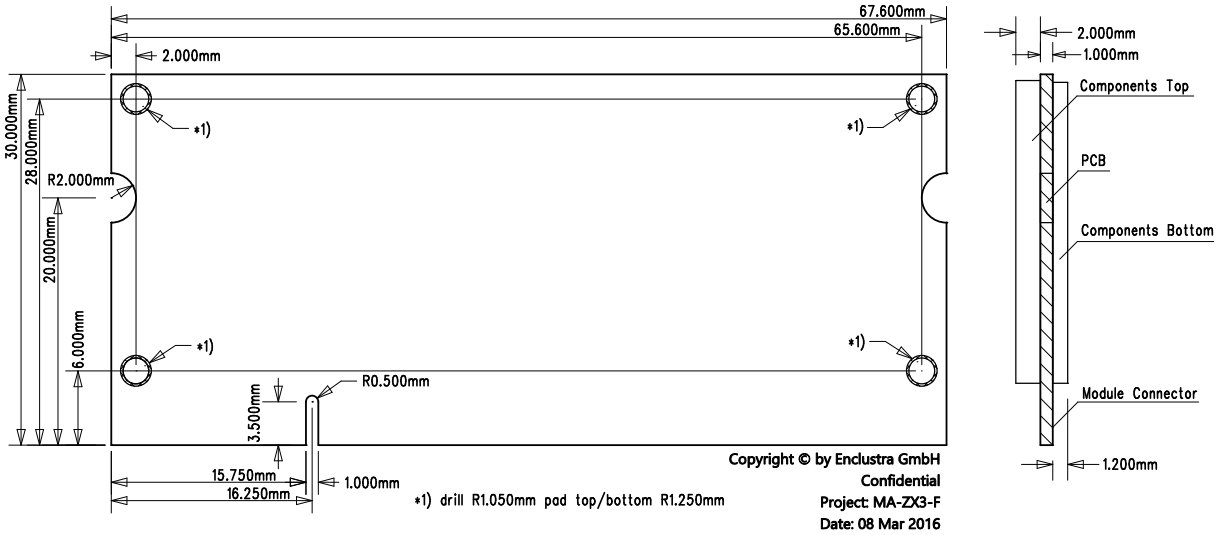

Figure 8: Module Footprint - Top View

The footprint of the module connector is available for different PCB design tools (Altium, Eagle, Orcad, PADS) [7].

2.7 Mechanical Data

Table 3 describes the mechanical characteristics of the Mars ZX3 SoC module. A 3D model (PDF) and a STEP 3D model are available [8], [9].

Symbol	Value
Size	67.6 × 30 mm
Component height top	2.0 mm
Component height bottom	1.2 mm
Weight	9 g

Table 3: Mechanical Data

2.8 Module Connector

The Mars ZX3 SoC module fits into a 200-pin DDR2 SO-DIMM (1.8 V) socket. Up to four M2 screws may be used to mechanically fasten the module to the base board. Do not use excessive force to tighten the screws, as this could damage the module.

The pinout of the module connector is found in the Mars Master Pinout Excel Sheet [11]. The connector to be mounted on the base board is available in different heights. Some examples are presented in Table 4. Please refer to the connector datasheet for more information.

Height	Type	Description	Max component height under the module
4.0 mm	TE 292406-4	DDR2-SODIMM, 1.8 V	0 mm
5.2 mm	TE 1565917-4	DDR2-SODIMM, 1.8 V	1 mm
6.5 mm	TE 5-1746530-4	DDR2-SODIMM, 1.8 V	2 mm
8.0 mm	TE 1827341-4	DDR2-SODIMM, 1.8 V	4 mm

Table 4: Module Connector Types

2.9 User I/O

2.9.1 Pinout

Information on the Mars ZX3 SoC module pinout can be found in the Enclustra Mars Master Pinout [11], and in the additional document Enclustra Module Pin Connection Guidelines [10].

The naming convention for the user I/Os is:
IO_B<BANK>_L<PAIR><_SPECIAL_FUNCTION>_<PACKAGE_PIN>_<POLARITY>.

For example, IO_B35_L1_AD0_F16_P is located on pin F16 of I/O bank 35, pair 1, it is an XADC auxiliary analog input capable pin and it has positive polarity, when used in a differential pair.

For the signal lines shared between Programmable Logic (PL) and Processing System (PS), the naming convention is:
IO_<MIO_PIN>_B<BANK>_L<PAIR>_<PACKAGE_PIN>

For example, IO_MIO44_B33_L16_U17 is connected to FPGA pin U17 and in parallel to the PS MIO pin 44.

Please note that for the shared pins only one of the driving pins (FPGA pin, MIO pin) may be active.

The multi-region clock capable pins are marked with "MRCC", while the single region clock capable pins are marked with "SRCC" in the signal name. For details on their function and usage, please refer to the Xilinx documentation.

Table 5 includes information related to the total number of I/Os available in each I/O bank and possible limitations.

Signal Name	Signals	Pairs	Differential	Single-ended	I/O Bank
IO_<MIO_PIN>_B33_<...>	12	6	In/Out	In/Out	33
IO_B34_<...>	48	24	In/Out	In/Out	34
IO_B35_<...>	48	24	In/Out	In/Out	35
Total	**108**	**54**	-	-	-

Table 5: User I/Os

Please note that for the 7 Series FPGAs there are restrictions on the VCCO voltage when using LVDS I/Os; refer to Xilinx AR# 43989 for details.

2.9.2 Differential I/Os

When using differential pairs, a differential impedance of 100 Ω must be matched on the base board, and the two nets of a differential pair must have the same length.

The information regarding the length of the signal lines from the SoC device to the module connector is available in Mars ZX3 SoC Module IO Net Length Excel Sheet [3]. This enables the user to match the total length of the differential pairs on the base board if required by the application.

2.9.3 I/O Banks

Table 6 describes the main attributes of the FPGA and PS I/O banks, and indicates which peripherals are connected to each I/O bank. All I/O pins within a particular I/O bank must use the same I/O (VCC_IO) and reference (VREF) voltages.

Bank	Connectivity	VCC_IO	VREF
Bank 0	Configuration	User selectable VCC_CFG_PS_B13_B33	-
Bank 13	Ethernet PHY Most pins shared with MIO 16-27	User selectable VCC_CFG_PS_B13_B33	-
Bank 33	Module connector Most pins shared with MIO 40-51	User selectable VCC_CFG_PS_B13_B33	-
Bank 34	Module connector	User selectable VCC_IO_B34	IO_B34_L6_VREF_M16_N IO_B34_L19_VREF_P15_N
Bank 35	Module connector	User selectable VCC_IO_B35	IO_B35_L6_VREF_F17_N IO_B35_L19_VREF_H20_N
PS MIO0	QSPI and NAND flash	User selectable[1] VCC_CFG_PS_B13_B33	-
PS MIO1	Ethernet PHY, USB PHY, Module connector	User selectable VCC_CFG_PS_B13_B33[2]	0.9 V
PS DDR	DDR3 SDRAM	User selectable[3] VCC_DDR3L	0.5 × VREF_DDR3L

Table 6: I/O Banks

[1] For modules of revision 4 or older, the MIO0 bank voltage is tied to 3.3 V.
[2] On modules of revision 4 or older, the name of this voltage supply signal is: VCC_CFG_MIO1_B13_B33.
[3] The DDR3 SDRAM supports voltages of 1.5 or 1.35 V. Please refer to Section 2.14 for details.

Warning!

Some of the I/Os are connected to MIO pins and to user logic I/Os in parallel - make sure that at least one of the two pins is configured to high impedance, and that pull-up or pull-down resistors are disabled on both if they are not used.

Some of the system pins must be defined as input or high impedance. Please refer to the Mars ZX3 SoC module reference design for details [2].

2.9.4 VREF Usage

I/O standards referenced using VREF can be used on the Mars module connector. The reference voltage has to be applied to all VREF pins of the respective I/O banks. If a bank is configured to use an I/O standard that does not need a reference voltage, the VREF pins of this bank on the module connector are available as user I/O pins.

The VREF pins are listed in the Mars Master Pinout Excel Sheet [11].

Warning!

Use only VREF voltages compliant with the equipped SoC device; any other voltages may damage the equipped SoC device, as well as other devices on the Mars ZX3 SoC module.

Do not leave a VREF pin floating when the used I/O standard requires a reference voltage, as this may damage the equipped SoC device, as well as other devices on the Mars ZX3 SoC module.

2.9.5 VCC_IO Usage

The VCC_IO voltages for the I/O banks located on the module connector are configurable by applying the required voltage to the VCC_IO_B[x], respectively VCC_CFG_[x] pins. All VCC_IO_B[x] or VCC_CFG_[x] pins of the same bank must be connected to the same voltage.

For compatibility with other Enclustra Mars base boards and modules, it is recommended to use a single I/O voltage.

Signal Name	SoC Pins	Supported Voltages	Connector Pins
VCC_CFG_PS_B13_B33	VCCO_13, VCCO_33, VCC_MIO0, VCC_MIO1	1.8 V[4], 2.5 V - 3.3 V[5] ±5%	137, 146
VCC_IO_B34	VCCO_34	1.8 V - 3.3 V[6] ±5%	53, 62, 73
VCC_IO_B35	VCCO_35	1.8 V - 3.3 V[7] ±5%	82, 117, 126

Table 7: VCC_IO Pins

[4] 1.8 V support is only available for modules of revision 5 and newer. NAND flash is disabled when VCC_CFG_PS_B13_B33 is 1.8 V.
[5] The RGMII Ethernet interface is specified only up to 2.5 V on the MIO pins by Xilinx. Please refer to Section 2.18 for details.
[6] I/O bank 34 can run down to 1.2 V if I2C bus access from the PL is not required.
[7] I/O bank 35 can run down to 1.2 V, but the FPGA LEDs will be always on in this case.

Note that the CFGBVS_0 pin is set automatically to GND (if VCC_CFG_PS_B13_B33 is less than or equal to 1.8 V) or to VCCO (if VCC_CFG_PS_B13_B33 is 2.5 V or 3.3 V).

Warning!

Use only VCC_IO voltages compliant with the equipped SoC device; any other voltages may damage the equipped SoC device, as well as other devices on the Mars ZX3 SoC module.

Do not leave a VCC_IO pin floating, as this may damage the equipped SoC device, as well as other devices on the Mars ZX3 SoC module.

Warning!

Do not power the VCC_IO pins when PWR_GOOD and PWR_EN signals are not active. If the module is not powered, you need to make sure that the VCC_IO voltages are disabled (for example, by using a switch on the base board, which uses PWR_GOOD as enable signal). Figure 9 illustrates the VCC_IO power requirements.

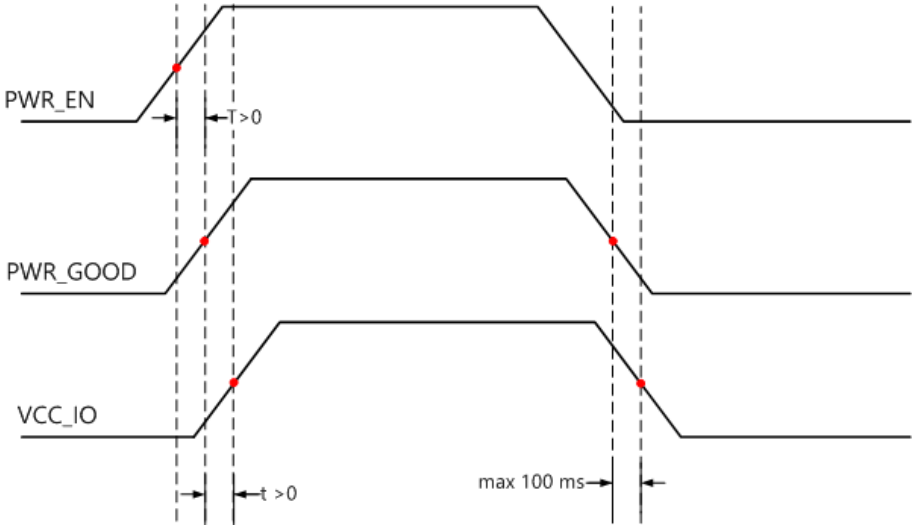

Figure 9: Power-Up Sequence - VCC_IO in Relation with PWR_GOOD and PWR_EN Signals

2.9.6 Signal Terminations

Differential Inputs

There are no external differential termination resistors on the Mars ZX3 SoC module for differential inputs. Differential input pairs on the module connector may be terminated either by external termination resistors on the base board (close to the module pins), or by the SoC device's internal termination resistors.

Internal differential termination is available only for certain VCCO voltages; please refer to Xilinx AR# 43989 for details.

Single-Ended Outputs

There are no series termination resistors on the Mars ZX3 SoC module for single-ended outputs. If required, series termination resistors may be equipped on the base board (close to the module pins).

2.9.7 Multiplexed I/O (MIO) Pins

Details on the MIO/EMIO terminology are available in the Zynq-7000 All Programmable SoC Technical Reference Manual [18].

Some of the MIO pins on the Mars ZX3 SoC module are connected to on-board peripherals, while others are available as GPIOs; the suggested functions below are for reference only - always verify your MIO pinout with the Xilinx device handbook.

Table 9 gives an overview over the MIO pin connections on the Mars ZX3 SoC module. Only the pins marked with "user functionality" are available on the module connector.

The MIO pins 52-53 have an external multiplexer that allows the pins to be switched either to the Ethernet MDIO interface, or to the on-board I2C bus; by default, MDIO is selected. In order to switch to I2C operation, MIO15 must be pulled low. Please refer to Table 8 for signal assignments.

It is recommended to use EMIO pins for I2C access. However, in situations where Ethernet is not used or when I2C access is needed before a bitstream is loaded into the FPGA, MIO pins 52-53 may be used for I2C.

MIO Pin	Function	
MIO15	MDIO select = 0	MDIO select = 1 (default)
MIO52	On-board I2C bus (I2C1.SCL)	Ethernet PHY MDC
MIO53	On-board I2C bus (I2C1.SDA)	Ethernet PHY MDIO

Table 8: Special MIO Pins

MIO Group	Function	Connection
0-14	QSPI and NAND flash	QSPI/NAND flash
15	MDIO select	I2C/MDIO multiplexer selection
16-27	Ethernet	Gigabit Ethernet PHY
28-39	USB	USB 2.0 OTG PHY
40-45	SD card/user functionality	Module connector
46 47	UART RX[8]/user functionality UART TX[8]/user functionality	Module connector
48-51	User functionality	Module connector
52-53	Ethernet MDIO/I2C	Gigabit Ethernet PHY/ On-board I2C bus and module connector via level shifter

Table 9: MIO Pins Connections Overview

[8] UART RX is an SoC input; UART TX is an SoC output.

2.9.8 Analog Inputs

The Zynq-7000 SoC devices provide a dual 12-bit ADC. The auxiliary analog inputs of the SoC device are connected to the module connector; these I/Os have the abbreviation "AD" followed by the ADC channel in the signal name.

The two dedicated ADC pins VP and VN are available on the module connector on pins 168 and 170 (FPGA_V_P/N). The ADC can also be used for internal voltage and temperature monitoring. For detailed information, refer to the Xilinx 7 Series XADC User Guide [19].

The ADC lines are always used differentially; for single-ended applications, the *_N line must be connected to GND.

Table 10 presents the ADC Parameters.

Parameter	Value
VCC_ADC	1.8 V
GND_ADC	0 V (connected to GND via ferrite)
VREF_ADC	1.25 V
ADC Range	0-1 V
Sampling Rate per ADC	1 MSPS
Total number of channels	17 (1 dedicated channel, 16 auxiliary inputs)

Table 10: ADC Parameters

2.10 Power

2.10.1 Power Generation Overview

The Mars ZX3 SoC module uses a 3.3 - 5.0 V DC power input for generating the on-board supply voltages (1.0 V, 1.35 V/1.5 V, 1.8 V). These internally-generated voltages are accessible on the module connector. In addition, a separate 3.3 V power input is used to supply peripherals, such as the Ethernet PHY, QSPI flash, oscillator, RTC, EEPROM and LEDs.

The Mars ZX3 SoC module can be powered using a single power supply. In this case, the two voltage supply inputs VCC_MOD and VCC_3V3 must be connected together to a 3.3 V supply. Please refer to Section 2.10.3 for details on the voltage supply inputs.

Table 11 describes the power supplies generated on the module.

Voltage Supply Name	Voltage Value	Rated Current	Voltage Source	Shut down via PWR_EN
VCC_1V0	1.0 V	4 A	VCC_MOD	Yes
VCC_DDR3L	1.35 V/1.5 V	2 A	VCC_MOD	Yes
VCC_1V8	1.8 V	2 A	VCC_MOD	Yes

Table 11: Generated Power Supplies

Please refer to the Enclustra Module Pin Connection Guidelines for general rules on the power pins [10].

2.10.2 Power Enable/Power Good

The Mars ZX3 SoC module provides a power enable input on the module connector. This input may be used to shut down the DC/DC converters for 1.0 V, 1.35 V/1.5 V and 1.8 V, leaving the SoC device and the DDR3 SDRAM unpowered, and detaching the separate 3.3 V power input from the peripherals.

The PWR_EN input is pulled to VCC_3V3 on the Mars ZX3 SoC module with a 10 kΩ resistor. The PWR_GOOD signal is pulled to VCC_3V3 on the Mars ZX3 SoC module with a 10 kΩ resistor.

PWR_GOOD is an open collector signal and must not be used to drive a load directly. This signal is pulled to GND if any of the on-board regulators fail or if the module is disabled via PWR_EN.

Pin Name	Module Connector Pin	Remarks
PWR_EN	13	Floating/3.3 V: Module power enabled Driven low: Module power disabled
PWR_GOOD	40	0 V: Module supply not ok 3.3 V: Module supply ok

Table 12: Module Power Status and Control Pins

Warning!

Do not apply any other voltages to the PWR_EN pin than 3.3 V or GND, as this may damage the Mars ZX3 SoC module. PWR_EN pin can be left unconnected.

Do not power the VCC_IO pins when PWR_EN is driven low to disable the module. In this case, VCC_IO needs to be switched off in the manner indicated in Figure 9.

2.10.3 Voltage Supply Inputs

Table 13 describes the power supply inputs on the Mars ZX3 SoC module. The VCC voltages used as supplies for the I/O banks are described in Section 2.9.5.

Pin Name	Module Connector Pins	Voltage	Description
VCC_MOD	1, 3, 5, 7, 9, 11	3.3 - 5.0 V ±10%	Supply for the 1.0 V, 1.35 V/1.5 V and 1.8 V voltage regulators. The input current is rated at 1.8 A (0.3 A per connector pin).
VCC_3V3	197, 199	3.3 V ±5%	Supply for Ethernet PHY, QSPI flash, oscillator, RTC, EEPROM and LEDs
VCC_BAT	200	2.0 - 3.6 V	Battery voltage for the RTC and SoC encryption key storage

Table 13: Voltage Supply Inputs

2.10.4 Voltage Supply Outputs

Table 14 presents the supply voltages generated on the Mars ZX3 SoC module, that are available on the module connector.

Pin Name	Module Connector Pins	Voltage	Maximum Current[9]
VCC_1V0	42	1.0 V ±5%	0.3 A
VCC_DDR3L	41	1.35 V/1.5 V ±5%	0.3 A
VCC_1V8	89, 94, 101, 106	1.8 V ±5%	1 A (and max 0.3 A per connector pin)

Table 14: Voltage Supply Outputs

The voltage supply for the DDR3 SDRAM can be set to 1.35 V for low power operation - for details, please refer to Section 2.14.5.

Warning!

Do not connect any power supply to the voltage supply outputs nor short circuit them to GND, as this may damage the Mars ZX3 SoC module.

2.10.5 Power Consumption

Please note that the power consumption of any SoC device strongly depends on the application (on the configured bitstream and I/O activity).

To estimate the power consumption of your design, please use the Xilinx Power Estimator available on the Xilinx website.

Table 15 lists the power consumption of a Mars ZX3 SoC module, for several applications.

The measurements are based on the reference design using a CPU frequency of 666 MHz, and the DDR3 memory operating in low power mode at 333 MHz.

[9] The maximum available output current depends on your SoC design. See sections 2.10.1 and 2.10.5 for details.

Supply	Uninitialized	Bare Metal U-Boot, no Ethernet Connection	Linux with Gigabit Ethernet Connection
VCC_MOD (5 V)	950 mW	1300 mW	1565 mW
VCC_3V3	76 mW	116 mW	142 mW
VCC_IO (2.5 V)	17 mW	165 mW	200 mW
Total	**1043 mW**	**1581 mW**	**1907 mW**

Table 15: Power Consumption - Reference Values

2.10.6 Heat Dissipation

High performance devices like the Xilinx Zynq-7000 SoC need cooling in most applications; always make sure the SoC is adequately cooled.

Information that may assist in selecting a suitable heat sink for the Mars ZX3 SoC module can be found in the Enclustra Modules Heat Sink Application Note [17].

For Enclustra Mars modules an Enclustra heat sink is available for purchase along with the product. It represents an optimal solution to cool the Mars ZX3 SoC module- it is low profile (less than 7 mm tall) and covers the whole module surface. It comes with a gap pad for the SoC device and four screws to attach it to the module PCB. With additional user configured gap pads, it is possible to cool other components on board as well. For details, please refer to the Enclustra website.

Warning!

Depending on the user application, the Mars ZX3 SoC module may consume more power than can be dissipated without additional cooling measures; always make sure the SoC is adequately cooled by installing a heat sink and/or providing air flow.

2.11 Clock Generation

A 33.33 MHz oscillator is used for the Mars ZX3 SoC module clock generation. The 33.33 MHz clock is fed to the PS and to the FPGA logic. Table 16 describes the clock connections.

Signal Name	Frequency	Package Pin	SoC Pin Type
CLK33	33.33 MHz	F7	PS_CLK
CLK33	33.33 MHz	Y6	IO_L13P_T2_MRCC_13

Table 16: Module Clock Resources

2.12 Reset

The power-on reset signal (POR) and the PS system reset signal (SRST) of the SoC device are available on the module connector.

Pulling PS_POR# low resets the SoC device, the Ethernet and the USB PHYs, and the flash devices. Please refer to the Enclustra Module Pin Connection Guidelines [10] for general rules regarding the connection of reset pins.

Pulling PS_SRST# low resets the SoC device. For details on the functions of the PS_POR_B and PS_SRST_B signals refer to the Zynq-7000 Technical Reference Manual [18].

Table 17 presents the available reset signals. Both signals, PS_POR# and PS_SRST#, have on-board 10 kΩ pull-up resistors to VCC_CFG_PS_B13_B33.

Signal Name	Connector Pin	Package Pin	FPGA Pin Type	Description
PS_POR#	196	B5	PS_POR_B	Power-on reset
PS_SRST#	192	C9	PS_SRST_B	System reset

Table 17: Reset Resources

Please note that PS_POR# is automatically asserted if PWR_GOOD is low.

2.13 LEDs

The four LEDs on the Mars ZX3 SoC module are connected to the FPGA logic, and they are active-low.

Signal Name	FPGA Pin	Remarks
LED0#	H18	User function/active-low
LED1#	AA14	User function/active-low; shared with MIO15
LED2#	AA13	User function/active-low
LED3#	AB15	User function/active-low

Table 18: LEDs

LED1# is shared between the PL (pin AA14) and PS (MIO15); for a correct status signaling the LED signal should be only driven from one side (PL or PS) low (for LED on) or set to high impedance (for LED off). Note that MIO15 is a dual-function pin and by changing the value of this signal, the MDIO/I2C selection circuit is also affected - please refer to Section 2.9.7 for details on the usage of this pin.

2.14 DDR3 SDRAM

There is a single DDR3 SDRAM channel on the Mars ZX3 SoC module attached directly to the PS side and is available only as a shared resource to the PL side.

The DDR3 SDRAM is operated at 1.35 V (low power mode) or at 1.5 V, depending on a selection signal. Two 16-bit memory chips are used to build a 32-bit wide memory.

The maximum memory bandwidth on the Mars ZX3 SoC module is:
1066 Mbit/sec × 32 bit = 4264 MB/sec

2.14.1 DDR3 SDRAM Type

Table 19 describes the memory availability and configuration on the Mars ZX3 SoC module.

Module	SDRAM Type	Density	Configuration	Manufacturer
MA-ZX3-D9	MT41K128M16JT-125	2 Gbit	128 M × 16 bit	Micron
MA-ZX3-D10	MT41K256M16HA-125 IT	4 Gbit	256 M × 16 bit	Micron
MA-ZX3-D9	NT5CC128M16FP-DI	2 Gbit	128 M × 16 bit	Nanya
MA-ZX3-D10	NT5CC256M16CP-DII	4 Gbit	256 M × 16 bit	Nanya

Table 19: DDR3 SDRAM Types

Warning!

Other DDR3 memory devices may be equipped in future revisions of the Mars ZX3 SoC module. Please check the user manual regularly for updates.

2.14.2 Signal Description

Please refer to the Mars ZX3 SoC Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR3 SDRAM connections.

2.14.3 Termination

Warning!

No external termination is implemented on the Mars ZX3 SoC module. Therefore, it is strongly recommended to enable the on-die termination (ODT) feature of the DDR3 SDRAM device.

2.14.4 Parameters

Please refer to the Mars ZX3 SoC module reference design [2] for DDR3 settings guidelines. The DDR3 SDRAM parameters and the DDR3 board timing information to be set in Vivado project are presented in Tables 20 and 21.

The values given in Table 20 are for reference only. Depending on the equipped memory device on the Mars ZX3 SoC module and on the DDR3 SDRAM frequency, the configuration may be different to the one in the reference design. Please refer to the memory device datasheet for details.

Parameter	Value
Memory type	DDR3/DDR3L
DRAM bus width	32 bit
Operating frequency	400-533 MHz
DRAM chip bus width	16 bit
DRAM chip capacity	2048-4096 Mbits
Speed bin	DDR3_1066F/DDR3L_1066F
Bank bits	3
Row bits	14-15 (depending on the module type)
Column bits	10
CAS latency	7
CAS write latency	6
RAS to CAS delay	7
Precharge time	7
tRC	50.625 ns
tRASmin	37.5 ns
tFAW	40.0 ns

Table 20: DDR3 SDRAM Parameters

Parameter	Byte 3	Byte 2	Byte 1	Byte 0
DQS to clock delay (ns)	0.0	0.0	0.012	0.0
Board delay (ns)	0.285	0.248	0.241	0.238

Table 21: DDR3 Board Timing

2.14.5 DDR3 Low Voltage Operation

The default voltage of the DDR3 is 1.5 V. In order to enable low voltage mode (1.35 V), DDR3_VSEL (pin AA22) must be driven logic 0, and DDR3L memory type must be selected in the PS configuration parameters in Vivado.

For 1.5 V operation, DDR3_VSEL must be set to high impedance (not driven logic 1).

2.15 QSPI Flash

The QSPI flash can be used to boot the PS, and to store the FPGA bitstream, ARM application code and other user data.

2.15.1 QSPI Flash Type

Table 22 describes the memory availability and configuration on the Mars ZX3 SoC module.

The bigger flash device introduced starting with revision 4 has bigger erase sectors (256 kB instead of 4 kB) and the 4 kB/32 kB/64 kB erase commands are not supported anymore. Further, the programming buffer is 512 bytes instead of 256 bytes. This may require adjustments of the programming algorithm.
As there is one QSPI flash chip equipped on the Mars ZX3 SoC module, type "single" must be selected when programming the flash from Vivado tools.

Module	Flash Type	Size	Manufacturer
MA-ZX3 - R1, R2 and R3	W25Q128FVEIG	128 Mbit	Winbond
MA-ZX3 - R4 and newer	S25FL512S	512 Mbit	Cypress (Spansion)

Table 22: QSPI Flash Types

Warning!

Other flash memory devices devices may be equipped in future revisions of the Mars ZX3 SoC module. Please check the user manual regularly for updates.

2.15.2 Signal Description

The QSPI flash is connected to the PS MIO pins 1-6. Some of the signals are available on the module connector, allowing the user to program the QSPI flash from an external master.

Note that MIO pins 2-6 pins are shared between NAND flash and QSPI flash on the Mars ZX3 SoC module, therefore only of the two memories may be used at once. However, it is possible to switch between them at runtime.

Please refer to Section 3 for details on programming the flash memory.

Warning!

Special care must be taken when connecting the QSPI flash signals on the base board. These signals are shared with the NAND flash and have to be high impedance during normal operation.

Long traces or high capacitance may disturb the data communication between the SoC and the flash devices.

Note that on the Mars ZX3 SoC module revision 4 and newer, the equipped flash device (Cypress/Spansion) has a reset signal, which is connected to PS_POR#. Hence, a new method to keep the FPGA in reset is required during the QSPI flash programming from an external SPI master. Please refer to Section 3.8 for details.

2.15.3 Configuration

The QSPI flash supports up to 50 MHz operation for standard read. For fast, dual and quad read speed values, please refer to the flash device datasheet.

Note that the "Feedback Clk" option on pin MIO8 must be enabled in the Zynq configuration for clock rates higher than 30 MHz.

24-bit Address Compatibility Mode

If the Zynq device boots from the QSPI flash and the 24-bit address compatibility mode of the QSPI flash is used to access the range above 16 MB, then the compatibility mode must be disabled before a system reset is executed. Otherwise, the Zynq device will not be able to boot from the QSPI flash again, as the address register is not pointing to the lower addressed part of the memory, in which the boot image is located.

The reset of the QSPI flash is connected to the PS_POR# power-on reset signal in order to avoid this issue after a power-on reset. The PS_SRST# signal should not be used in this setup.

Please refer to Zynq-7000 Technical Reference Manual [18] for details on booting from the QSPI flash.

2.16 NAND Flash

The NAND flash can be used to store ARM application code and other user data, and optionally to boot the PS and to store the FPGA bitstream. Refer to Section 3.3.2 for details.

The NAND flash is disabled when VCC_CFG_PS_B13_B33 is 1.8 V. The NAND_ENABLE signal, which controls the CE# pin of the NAND flash, is set automatically to GND (if VCC_CFG_PS_B13_B33 is less than or equal to 1.8 V) or to VCCO (if VCC_CFG_PS_B13_B33 is 2.5 V or 3.3 V).

2.16.1 NAND Flash Type

Table 23 describes the memory availability and configuration on the Mars ZX3 SoC module.

Flash Type	Size	Manufacturer
MT29F4G08ABADAWP	4 Gbit	Micron

Table 23: NAND Flash Type

2.16.2 Signal Description

The NAND flash is connected to the PS MIO pins 0, 2-14. The MIO pins 2-6 are shared between the QSPI and NAND flash.

The write protect pin (WP#) of the NAND flash is connected to pin V13, available from the FPGA logic, and has an on-board pull-up resistor.

2.16.3 Parameters

Please refer to the NAND flash memory device datasheet to extract the required parameter values. Reference values to be used in Vivado are given in Table 24.

The indicated parameter values may be used for booting from NAND flash memory on the Mars ZX3 SoC module.

Nand Cycle Parameter	CS0	CS0 Cycles	Description
T_RC	30	4	Read cycle time
T_WC	30	4	Write cycle time
T_REA	0	1	RE assertion delay
T_WP	20	3	WE deassertion delay
T_CLR	20	3	Page cycle time
T_AR	20	3	ID read time
T_RR	30	4	Busy to RE

Table 24: NAND Flash Parameters

2.17 SD Card

An SD card can be connected to the PS MIO pins 40-45 or 46-51, or alternatively via EMIO pins to the PL.

The corresponding MIO pins are available on the module connector. Note that only MIO pins 40-45 allow the Mars ZX3 SoC module to boot from the SD card. Information on this boot mode is available in Section 3.6.

Please note that external pull-ups are needed for SD card operation. Depending on the selected voltage for VCC_CFG_PS_B13_B33, a level shifter to 3.3 V may be required (some level shifters also have built-in pull-ups).

2.18 Gigabit Ethernet

A 10/100/1000 Mbit Ethernet PHY is available on the Mars ZX3 SoC module, connected to the PS and PL via RGMII interface.

Please note that Xilinx recommends operation at 1.8 V/2.5 V for the RGMII interface for the MIO pins [18]. Enclustra tests have shown that the RGMII is functional with a 3.3 V I/O voltage on the MIO pins, as long as the I/O voltage configured in Vivado matches the applied I/O voltage. However, in situations where a voltage of 3.3 V for VCC_CFG_PS_B13_B33 is required, it is recommended to assign the Ethernet PHY signals to FPGA logic and use the GMII to RGMII converter provided by Xilinx [21], instead of using 3.3 V on the MIO pins.

2.18.1 Ethernet PHY Type

Table 25 describes the equipped Ethernet PHY device type on the Mars ZX3 SoC module.

Module	PHY Type	Manufacturer	Type
MA-ZX3 - R1	KSZ9021RN	Micrel	10/100/1000 Mbit
MA-ZX3 - R2 and newer	KSZ9031RNX	Micrel	10/100/1000 Mbit

Table 25: Gigabit Ethernet PHY Type

2.18.2 Signal Description

The RGMII interface is connected to MIO pins 16-27 for use with the hard macro MAC, and in parallel to PL bank 13 pins for use with the FPGA logic. The interrupt output of the Ethernet PHY is connected to the I2C interrupt line, available on an EMIO pin.

The Gigabit Ethernet connections are presented in Table 26. All listed pins are operated at VCC_CFG_PS_B13_B33 I/O voltage.

Signal Name	MIO Pin	PL Pin
ETH_RST#	-	AB11
I2C_INT#	-	H17
ETH_MDC	MIO52[10]	AA12
ETH_MDIO	MIO53[10]	AB12
ETH_RXC	MIO22	Y9
ETH_RX_CTL	MIO27	Y8
ETH_RXD0	MIO23	U10
ETH_RXD1	MIO24	Y11
ETH_RXD2	MIO25	W11
ETH_RXD3	MIO26	U11
ETH_TXC	MIO16	W10
ETH_TX_CTL	MIO21	V10
ETH_TXD0	MIO17	V8
ETH_TXD1	MIO18	W8
ETH_TXD2	MIO19	U6
ETH_TXD3	MIO20	V9

Table 26: Gigabit Ethernet Signal Description

2.18.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details regarding the connection of Ethernet signals.

2.18.4 MDIO Address

The MDIO address assigned to the Gigabit Ethernet PHY is 3.

The MDIO interface is connected by default to MIO pins 52-53. These pins can also be used to access the I2C bus - for details, please refer to Section 2.9.7.

[10] MIO52 and MIO53 can be used for either MDIO or I2C. Please refer to Section 2.9.7 for details.

2.18.5 PHY Configuration

The configuration of the Ethernet PHY is bootstrapped when the PHY is released from reset. Make sure all I/Os on the RGMII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

The bootstrap options of the Ethernet PHY are set as indicated in Table 27.

Please note that the RGMII delays in the Ethernet PHY need to be configured before the Ethernet interface can be used. This is done in the source files within the First Stage Boot Loader (FSBL) application provided in the Mars ZX3 SoC module reference design [2].

Pin	Signal Value	Description
MODE[3-0]	1110	RGMII mode: advertise all capabilities (10/100/1000, half/full duplex) except 1000Base-T half duplex.
PHYAD[2-0]	011	MDIO address 3
Clk125_EN	0	125 MHz clock output disabled
LED_MODE	1	Single LED mode
LED1/LED2	1	Active-low LEDs

Table 27: Gigabit Ethernet PHY Configuration

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 1 MHz.

2.19 USB 2.0

The Mars ZX3 SoC module has an on-board USB 2.0 PHY connected to the SoC device. The USB interface can be configured for USB host, USB device and USB On-The-Go (host and device capable) operations.

2.19.1 USB PHY Type

Table 28 describes the equipped USB PHY device type on the Mars ZX3 SoC module.

PHY Type	Manufacturer	Type
USB3320C	Microchip	USB 2.0 PHY

Table 28: USB 2.0 PHY Type

2.19.2 Signal Description

The ULPI interface is connected to MIO pins 28-39 for use with the integrated USB controller.

2.20 Real-Time Clock (RTC)

A real-time clock is connected to the I2C bus. The RTC features a battery-buffered 128 bytes user SRAM and a temperature sensor. See Section 4 for details on the I2C bus on the Mars ZX3 SoC module.

VBAT pin of the RTC is connected to VCC_BAT on the module connector, and can be connected directly to a 3 V battery. Please refer to the Enclustra Module Pin Connection Guidelines [10] for details.

Note that the frequency output mode of the RTC must be disabled when using I2C interrupt system. Otherwise, I2C_INT# is periodically pulled down by the RTC. The disabling of this function can be done by setting bits [3:0] of the RTC register 8 to logic low.

2.20.1 RTC Type

Table 29 describes the equipped RTC device type on the Mars ZX3 SoC module.

Type	Manufacturer
ISL12020M	Intersil

Table 29: RTC Type

An example demonstrating how to use the RTC is included in the Mars ZX3 SoC module reference design [2].

2.21 Secure EEPROM

The secure EEPROM is used to store the module type and serial number, as well as the Ethernet MAC address and other information. It is connected to the I2C bus.

The secure EEPROM must not be used to store user data.

Please refer to Section 4.4 for details on the content of the EEPROM.

2.21.1 EEPROM Type

Table 30 describes the equipped EEPROM device type on the Mars ZX3 SoC module.

Type	Manufacturer
DS28CN01 (default)	Maxim
ATSHA204A-MAHDA-T (assembly option)	Atmel

Table 30: EEPROM Type

An example demonstrating how to read data from the EEPROM is included in the Mars ZX3 SoC module reference design [2].

2.22 Revision Detection

Starting from revision 4 of Mars ZX3 SoC module, a pull-down resistor has been mounted to easily detect the current revision.

The pin location of this resistor is noted in table 31.

Revision	Pin
4	AB21
5 and newer	Y21

Table 31: Pin Location of the Revision Detection Resistor

3 Device Configuration

3.1 Configuration Signals

The PS of the SoC needs to be configured before the FPGA logic can be used. Xilinx Zynq devices need special boot images to boot from QSPI flash or SD card. For more information, please refer to the Xilinx Zynq-7000: Concepts, Tools, and Techniques document [20].

Table 32 describes the most important configuration pins and their location on the module connector. These signals allow the SoC to boot from QSPI flash or SD card, and can be used to program the QSPI flash from an external master. Please refer to Section 3.8 for details.

Signal Name	SoC Pin Type	Mod. Conn. Pin	Description	Comments
FLASH_CLK/NAND_IO1	MIO6	182	SPI CLK	20 kΩ pull-down
FLASH_DO/NAND_WE#	MIO3	184	SPI MISO	20 kΩ pull-down
FLASH_DI/NAND_ALE	MIO2	186	SPI MOSI	20 kΩ pull-down
FLASH_CS#	MIO1	188	SPI CS#	10 kΩ pull-up to VCC_CFG_PS_B13_B33
FPGA_DONE	DONE_0	194	FPGA configuration done	1 kΩ pull-up to VCC_CFG_PS_B13_B33
FPGA_CFGBVS	CFGBVS_0	-	Configuration bank voltage select[11]	10 kΩ pull-up to VCC_CFG_PS_B13_B33
PS_POR#	PS_POR_B	196	Must be pulled to GND for a short period before QSPI flash programming. PS_SRST# must be low when PS_POR# is released.	10 kΩ pull-up to VCC_CFG_PS_B13_B33
PS_SRST#	PS_SRST_B	192	Must be pulled to GND during QSPI flash programming. When released, all other pins of the SPI interface must be high impedance.	10 kΩ pull-up to VCC_CFG_PS_B13_B33
BOOT_MODE	-	190	Boot mode selection	10 kΩ pull-up to VCC_CFG_PS_B13_B33

Table 32: SoC Configuration Pins

Warning!

All configuration signals except for BOOT_MODE must be high impedance as soon as the device is released from reset. Violating this rule may damage the equipped SoC device, as well as other devices on the Mars ZX3 SoC module.

3.2 Pull-Up During Configuration

Figure 10 illustrates the configuration of the I/O signals during power-up.

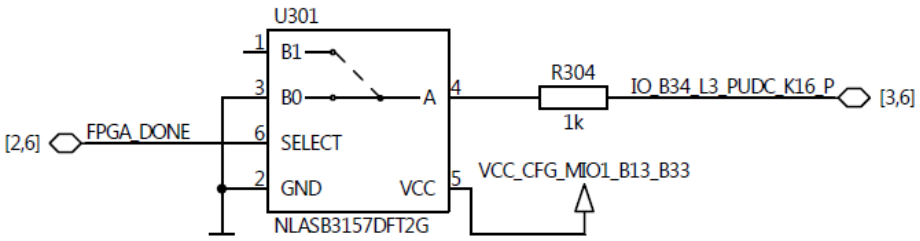

Figure 10: Pull-Up During Configuration (PUDC)

The Pull-Up During Configuration signal (PUDC) is configured using a multiplexer to low state during FPGA configuration, and to high impedance after this process is done.

If the user does not drive a high value on this signal during configuration, then the PUDC signal will be pulled to GND via a 1 kΩ resistor. As PUDC is an active-low signal, all FPGA I/Os will have the internal pull-up resistors enabled during device configuration.

If the application requires that all FPGA I/Os have the internal pull-up resistors disabled during device configuration, the user must attach to the module connector a driver capable to pull IO_B34_L3_PUDC#_K16_P signal high.

For details on the PUDC signal please refer to the Zynq-7000 All Programmable SoC Technical Reference Manual [18].

3.3 Boot Mode

The boot mode can be selected via a signal available on the module connector.

Table 33 describes the available boot modes on the Mars ZX3 SoC module.

BOOT_MODE	Description
0	Boot from QSPI flash
1	Boot from SD card

Table 33: Boot Modes

Additionally, JTAG and NAND flash boot modes are available. These are further presented in Sections 3.3.1 and 3.3.2.

[11]The CFGBVS_0 pin is set automatically to GND (if VCC_CFG_PS_B13_B33 is less than or equal to 1.8 V) or to VCCO (if VCC_CFG_PS_B13_B33 is 2.5 V or 3.3 V).

3.3.1 JTAG Boot Mode

For JTAG boot mode selection, the following steps must be followed:

- BOOT_MODE must be set to logic low
- MIO5 (NAND_IO0/FLASH_IO3) must be pulled to GND (refer to Table 34 for details)

Module	Hardware changes required to pull MIO5 to GND
MA-ZX3 - R1	R111 must be mounted
MA-ZX3 - R2 and R3	R111 must be short-circuited
MA-ZX3 - R4 and newer	R213 must be short-circuited

Table 34: Hardware Changes for JTAG and NAND Boot Modes

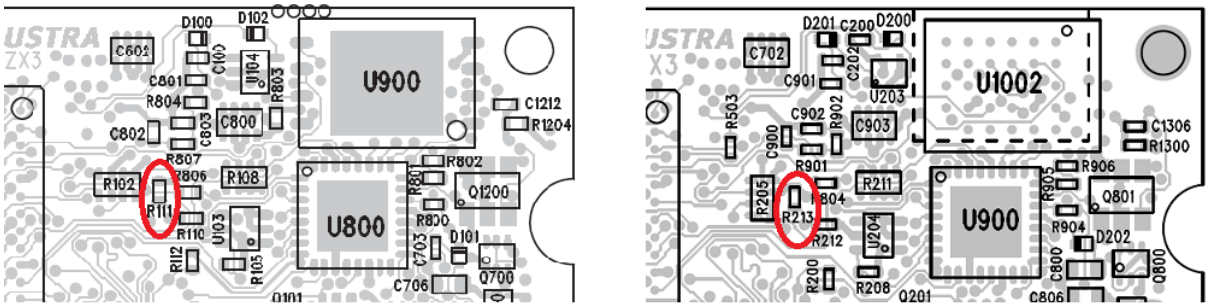

Figure 11: Boot Mode Resistor - Assembly Drawing Top View (Refer to Section 2.5 for the latest Assembly Drawing)

3.3.2 NAND Flash Boot Mode

For NAND flash boot mode selection, the following steps must be followed:

- BOOT_MODE must be set to logic high
- MIO5 (NAND_IO0/FLASH_IO3) must be pulled to GND (refer to Table 34 for details)

In the NAND boot mode, the PS boots from the NAND flash located on the module. The flash device is connected to the PS MIO pins 0 and 2-14.

In order to boot from the NAND flash, the user must enable the NAND controller in the Vivado block design and set the timing parameters as described in Section 2.16.3. After these changes, a new FSBL must be generated and used for the Zynq boot image creation.

3.4 JTAG

The FPGA and the PS JTAG interfaces are connected into one single chain available on the module connector. The SoC device, the QSPI flash, and the NAND flash can be configured via JTAG from Xilinx SDK or Xilinx Vivado Hardware Manager.

3.4.1 JTAG on Module Connector

Signal Name	Module Connector Pin	Resistor
JTAG_TCK	158	22 kΩ pull-up to VCC_CFG_PS_B13_B33
JTAG_TMS	162	SoC internal pull-up
JTAG_TDI	160	SoC internal pull-up
JTAG_TDO	164	-

Table 35: JTAG Interface

3.4.2 External Connectivity

JTAG signals can be connected directly on the base board to a JTAG connector. No pull-up/pull-down resistors are necessary. The VREF pin of the programmer must be connected to VCC_CFG_PS_B13_B33.

It is recommended to add 22 Ω series termination resistors between the module and the JTAG header, close to the source. Please refer to the Enclustra Module Pin Connection Guidelines for details on JTAG interface.

3.5 QSPI Boot Mode

In the QSPI boot mode, the PS boots from the QSPI flash located on the module. The flash device is connected to the PS MIO pins 1-6.

In order to boot from the QSPI flash, the user must enable the QSPI flash controller in the Vivado block design and generate a new FSBL to be used for the Zynq boot image creation.

3.6 SD Card Boot Mode

In the SD card boot mode the PS boots from the SD card located on the base board.

For this operation, the following requirements must be met:

- The SD card must be connected to MIO pins 40-45
- A Zynq boot image must be generated from an SoC design having the SDIO controller enabled
- The boot image must be named “boot.bin” and then copied to the SD card
- In software versions older than Vivado 2014.4, the card detect check in the Xilinx FSBL must be disabled. For details, please contact Enclustra Support team.
- The SDIO controller must be fed with a reasonable clock frequency. As some versions of the FSBL do not configure the clock divider in the SDIO controller, a 50 MHz clock is used in the reference design.

For details on SD card boot, please refer to the Xilinx Zynq documentation [18] [20].

3.7 QSPI Flash Programming via JTAG

The Xilinx Vivado and SDK software offer QSPI flash programming support via JTAG. For more information, please refer to the Xilinx documentation [22].

3.8 QSPI Flash Programming from an External SPI Master

The signals of the QSPI flash are directly connected to the module connector for flash access. As the flash signals are connected to the SoC device as well, the SoC device pins must be tri-stated while accessing the QSPI flash directly from an external device.

This is ensured by pulling the PS_SRST# signal to GND followed by a pulse on PS_POR#, which puts the SoC device into reset state and tri-states all I/O pins. PS_SRST# must be low when PS_POR# is released and kept low until the flash programming has finished. Afterwards, all SPI lines and PS_SRST# must be tri-stated and another reset impulse must be applied to PS_POR#.

Figure 12 shows the signal diagrams corresponding to flash programming from an external master.

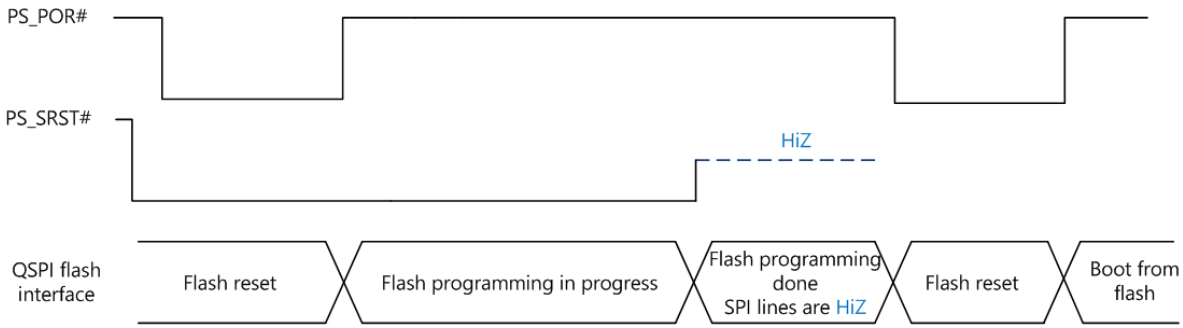

Figure 12: QSPI Flash Programming from an External SPI Master - Signal Diagrams

Warning!

Accessing the QSPI flash directly without putting the SoC device into reset may damage the equipped SoC device, as well as other devices on the Mars ZX3 SoC module.

3.9 NAND Flash Programming

The NAND flash on the Mars ZX3 SoC module can be programmed via JTAG or from u-boot.

The Xilinx SDK software offers NAND flash programming support via JTAG. For the programming operation, type "nand_8" must be selected. Please note that Vivado Hardware Manager does not support the NAND flash type equipped on the Mars ZX3 SoC module.

When programming the NAND flash in u-boot, the user must make sure that the NAND controller is enabled; the u-boot available in the Enclustra Linux build environment includes a built-in command to switch the current configuration to use NAND flash as storage:

```
zx_set_storage NAND
```

Note that for a successful programming the flash image must be written avoiding the bad sectors of the flash (by using nand.jffs2 command).

3.10 FPGA and QSPI Flash Programming using Xilinx Impact

For Zynq-7000 devices, Xilinx Impact requires JTAG boot mode to be selected in order to download the bitstream or program the QSPI flash.

As this operation on the Mars ZX3 SoC module requires hardware changes (please refer to Section 3.3.1), it is recommended to use Xilinx SDK or Vivado for FPGA or QSPI flash programming.

3.11 Enclustra Module Configuration Tool

In combination with an Enclustra base board, the QSPI flash can be programmed using the Enclustra Module Configuration Tool (MCT) [16].

Please note that the Xilinx Zynq devices do not support slave serial configuration, therefore only flash programming is supported by the Enclustra MCT for the Mars ZX3 SoC module.

4 I2C Communication

4.1 Overview

The I2C bus on the Mars ZX3 SoC module is connected to the SoC device, EEPROM and RTC, and is available on the module connector. This allows external devices to read the module type and to connect more devices to the I2C bus.

Please note that the RTC must be configured correctly to use I2C interrupts - for details, refer to Section 2.20.

The I2C clock frequency should not exceed 400 kHz.

Warning!

Maximum I2C speed may be limited by the routing path and additional loads on the base board.

Warning!

If the I2C traces on the base board are very long, 100 Ω series resistors should be added between module and I2C device on the base board.

4.2 Signal Description

Table 36 describes the signals of the I2C interface. All signals have on-board pull-up resistors to VCC_3V3.

All signals must be connected to open collector outputs and must not be driven high from any source. I2C_INT# is an input to the SoC and must not be driven from the SoC device.

For Mars ZX3 SoC module revision 4 and older, the I2C_INT# signal was inverted for the SoC device. It was an active-low signal for the entire system but active-high for the SoC. Modules of revision 5 and newer do not have this inversion, therefore I2C_INT# is also active-low at the SoC device. Refer to Section 2.22 on how to detect the module revision. The Mars ZX3 SoC module reference design includes the HDL code section for the revision detection and I2C_INT# inversion.

Level shifters are used between the I2C bus and the PS/PL pins, to allow I/O voltages lower than 3.3 V. Please make sure that all pins are configured correctly and no pull-down resistors are enabled.

Signal Name	PS Pin	PL Pin	Connector Pin	Resistor
I2C_SDA	MIO53[12]	H15	176	2.2 kΩ pull-up
I2C_SCL	MIO52[12]	R15	178	2.2 kΩ pull-up
I2C_INT#	-	H17	174	10 kΩ pull-up

Table 36: I2C Signal Description

[12] MIO52 and MIO53 are used for MDIO by default. Please refer to Section 2.9.7 for details.

4.3 I2C Address Map

Table 37 describes the addresses for several devices connected on I2C bus.

Address (7-bit)	Description
0x5C	Secure EEPROM
0x64	Secure EEPROM (assembly option, refer to Section 2.21)
0x57	RTC user SRAM
0x6F	RTC registers

Table 37: I2C Addresses

4.4 Secure EEPROM

The secure EEPROM is used to store the module serial number and configuration. In the future, the EEPROM will be used for copy protection and licensing features. Please contact us for further information.

An example demonstrating how to read the module information from the EEPROM memory is included in the Mars ZX3 SoC module reference design.

Warning!

The secure EEPROM is for Enclustra use only. Any attempt to write data to the secure EEPROM causes the warranty to be rendered void.

4.4.1 Memory Map

Address	Length (bits)	Description
0x00	32	Module serial number
0x04	32	Module product information
0x08	40	Module configuration
0x0D	24	Reserved
0x10	48	Ethernet MAC address
0x16	48	Reserved
0x1C	32	Checksum (only for DS28CN01 EEPROM type)

Table 38: EEPROM Sector 0 Memory Map

Module Serial Number

The module serial number is a unique 32-bit number that identifies the module. It is stored using big-endian byte order (MSB on the lowest address).

Module Product Information

This field indicates the type of module and hardware revision.

Module	Product Family	Reserved	Revision	Product Information
Mars ZX3 SoC module	0x0323	0x[XX]	0x[YY]	0x0323 [XX][YY]

Table 39: Product Information

Module Configuration

Addr.	Bits	Comment	Min. Value	Max. Value	Comment
0x08	7-4	SoC type	0	0	See SoC type table (Table 41)
	3-0	SoC device speed grade	1	3	
0x09	7	Temperature range	0 (Commercial)	1 (Industrial)	
	6	Power grade	0 (Normal)	1 (Low power)	
	5-4	Ethernet port count	0	1	
	3	Ethernet speed	0 (Fast Ethernet)	1 (Gigabit Ethernet)	
	2	RTC equipped	0	1	
	1-0	Reserved	-	-	
0x0A	7-2	Reserved	-	-	
	1-0	USB 2.0 port count	0	1	
0x0B	7-4	DDR3 RAM size (MB)	0 (0 MB)	8 (1 GB)	Resolution = 8 MB
	3-0	QSPI flash memory size (MB)	0 (0 MB)	7 (64 MB)	Resolution = 1 MB
0x0C	7-4	Reserved	-	-	
	3-0	NAND flash memory size (MB)	0 (0 MB)	10 (512 MB)	Resolution = 1 MB

Table 40: Module Configuration

The memory sizes are defined as Resolution$\times 2^{(Value-1)}$ (e.g. DRAM=0: not equipped, DRAM=1: 8 MB, DRAM=2: 16 MB, DRAM=3: 32 MB, etc).

Table 41 shows the available SoC types.

Value	SoC Device Type
0	XC7Z020

Table 41: SoC Device Types

Ethernet MAC Address

The Ethernet MAC address is stored using big-endian byte order (MSB on the lowest address). Each module is assigned two sequential MAC addresses; only the lower one is stored in the EEPROM.

5 Operating Conditions

5.1 Absolute Maximum Ratings

Table 42 indicates the absolute maximum ratings for Mars ZX3 SoC module. The values given are for reference only; for details please refer to the Zynq-7000 DC and AC Switching Characteristics Datasheet [23].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	-0.5 to 6	V
VCC_3V3	3.3 V supply voltage relative to GND	-0.5 to 3.6	V
VCC_BAT	Supply voltage for the RTC and encryption key storage	-0.3 to 3.6	V
VCC_IO_[x] VCC_CFG_[x]	Output drivers supply voltage relative to GND	-0.5 to 3.6	V
V_IO	I/O input voltage relative to GND	-0.5 to V_{CCO}+0.5	V
V_ADC	Analog I/O input voltage for the ADC	-0.5 to 2.3	V
Temperature	Temperature range for commercial modules (C)*	0 to +70	°C
	Temperature range for industrial modules (I)*	-40 to +85	°C

Table 42: Absolute Maximum Ratings

5.2 Recommended Operating Conditions

Table 43 indicates the recommended operating conditions for Mars ZX3 SoC module. The values given are for reference only; for details please refer to the Zynq-7000 DC and AC Switching Characteristics Datasheet [23].

Symbol	Description	Rating	Unit
VCC_MOD	Supply voltage relative to GND	3.0 to 5.5	V
VCC_3V3	3.3 V supply voltage relative to GND	3.15 to 3.45	V
VCC_BAT	Supply voltage for the RTC and encryption key storage	2.0 to 3.45	V
VCC_IO_[x] VCC_CFG_[x]	Output drivers supply voltage relative to GND	Refer to Section 2.9.5	V
V_IO	I/O input voltage relative to GND	-0.2 to V_{CCO}+0.2	V
V_ADC	Analog I/O input voltage for the ADC	0 to 1.5	V
Temperature	Temperature range for commercial modules (C)* Temperature range for industrial modules (I)*	0 to +70 -40 to +85	°C °C

Table 43: Recommended Operating Conditions

Warning!

** The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.*

6 Ordering and Support

6.1 Ordering

Please use the Enclustra online request/order form for ordering or requesting information:
`http://www.enclustra.com/en/order/`

6.2 Support

Please follow the instructions on the Enclustra online support site:
`http://www.enclustra.com/en/support/`

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References

[1] Enclustra General Business Conditions
`http://www.enclustra.com/en/products/gbc/`
[2] Mars ZX3 SoC Module Reference Design
→ Ask Enclustra for details
[3] Mars ZX3 SoC Module IO Net Length Excel Sheet
→ Ask Enclustra for details
[4] Mars ZX3 SoC Module FPGA Pinout Excel Sheet
→ Ask Enclustra for details
[5] Mars ZX3 SoC Module User Schematics
→ Ask Enclustra for details
[6] Mars ZX3 SoC Module Known Issues and Changes
→ Ask Enclustra for details
[7] Mars ZX3 SoC Module Footprint
→ Ask Enclustra for details
[8] Mars ZX3 SoC Module 3D Model (PDF)
→ Ask Enclustra for details
[9] Mars ZX3 SoC Module STEP 3D Model
→ Ask Enclustra for details
[10] Module Pin Connection Guidelines
→ Ask Enclustra for details
[11] Mars Master Pinout
→ Ask Enclustra for details
[12] Mars PM3 User Manual
→ Ask Enclustra for details
[13] Mars EB1 User Manual
→ Ask Enclustra for details
[14] Mars Starter User Manual
→ Ask Enclustra for details
[15] Enclustra Build Environment
→ Ask Enclustra for details
[16] Enclustra Module Configuration Tool
`http://www.enclustra.com/en/products/tools/module-configuration-tool/`
[17] Enclustra Modules Heat Sink Application Note
→ Ask Enclustra for details
[18] Zynq-7000 All Programmable SoC Technical Reference Manual, UG585, Xilinx, 2015
[19] 7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide, UG480, Xilinx, 2015
[20] Zynq-7000 All Programmable SoC: Concepts, Tools, and Techniques (CTT), UG873, Xilinx, 2013
[21] GMII to RGMII v4.0, PG160, Xilinx, 2015
[22] Vivado Design Suite User Guide, Programming and Debugging, UG908, Xilinx, 2016
[23] Zynq-7000 All Programmable SoC, DC and AC Switching Characteristics, DS187, Xilinx, 2015